

Telecom Datacom & System Timing

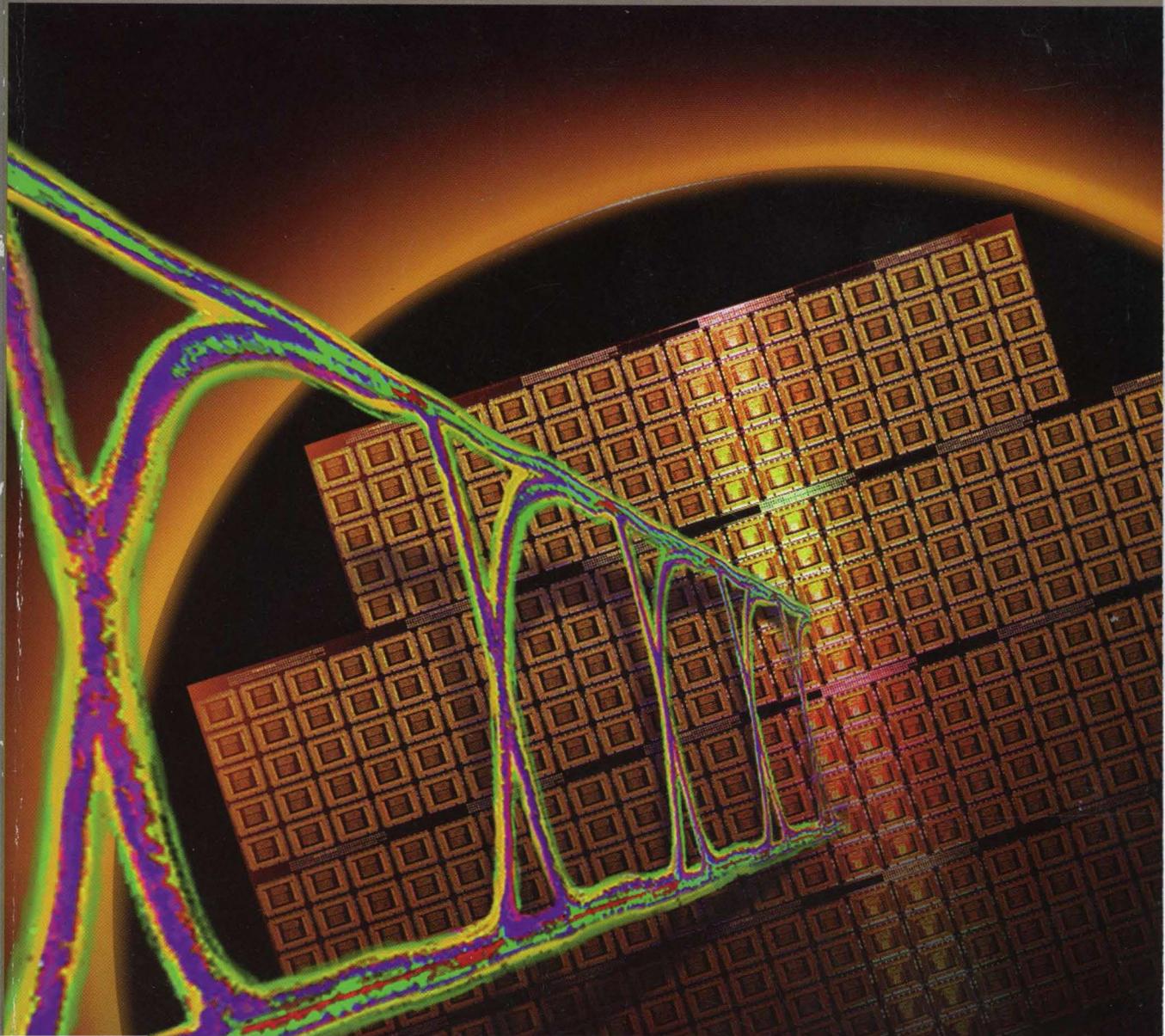
PRODUCT CATALOG

TriQuint 
SEMICONDUCTOR

Telecom Datacom & System Timing

1998

TriQuint 
SEMICONDUCTOR



Telecom, Datacom & System Timing

Product Catalog

PN 1003600

Revision 1.0.A
First printed October 1997



*An ISO-9001 Registered Company
TUV Certified Registration No. 09 100 4518*

Copyright © 1997 TriQuint Semiconductor, Inc. All rights reserved.

TriQuint and the TriQuint logo are registered trademarks of TriQuint, Inc. TriQuint product names are trademarks of TriQuint, Inc. All other trademarks are the property of their respective holders.

The information provided herein is believed to be reliable; TriQuint assumes no liability for inaccuracies or omissions. TriQuint assumes no responsibility for the use of this information, and all such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. TriQuint does not authorize or warrant any TriQuint product for use in life-support devices and/or systems.

Table of Contents

Overview	Section 1
Telecommunications Products	Section 2
Digital Switching Products	Section 3
Data Communications Products	Section 4
Mixed Signal Products	Section 5
System Timing Products	Section 6
Application Notes	Section 7
Sales and Distribution	Section 8



Section 1 — Overview

<i>Product Summary</i>	<i>1-3</i>
<i>Company Background</i>	<i>1-6</i>

Product Summary

Telecommunications Products

Part	Description	PLL Features	Low-Speed I/O	High-Speed I/O	Loopback	Page
TQ8101	622/155 Mb/s SONET/SDH 8:1 Mux and 1:8 Demux	Includes 622 Mb/s transmit PLL	TTL	ECL	Yes	2-3
TQ8103	622 Mb/s SONET/SDH Clock and Data Recovery	Includes 622 Mb/s PLL	TTL	ECL	—	2-17
TQ8105	622/155 Mb/s Enhanced SONET/SDH 8:1 Multiplexer, 1:8 Demultiplexer, Framer, and PLL (single supply)	Includes 622 Mb/s transmit PLL	TTL	ECL or PECL	Yes	2-27
TQ8106	TQ8105 with clock and data recovery	Includes 622 Mb/s CDR	TTL	ECL or PECL	Yes	2-27

Digital Switching Products

Part	Description	Propagation Delay	I/O	Skew (max.)	Jitter	Page
TQ8015	1.25 Gb/s/port 16x16 ECL Digital Crosspoint Switch	2000 ps	ECL	500 ps	150 ps pk-pk	3-3
TQ8016	1.3 Gb/s/port 16x16 ECL Digital Crosspoint Switch	2000 ps	ECL	400 ps		3-11
TQ8017	1.25 Gb/s/port 16x16 PECL Digital Crosspoint Switch	2000 ps	PECL	500 ps	150 ps pk-pk	3-21
TQ8025	2.5 Gb/s/port 16x16 PECL Digital Crosspoint Switch	2000 ps	PECL/CML	200 ps	100 ps pk-pk	3-29
TQ8032	800 Mb/s/port 32x32 ECL Digital Crosspoint Switch	2300 ps	ECL	500 ps	150 ps pk-pk	3-37
TQ8033	1.5 Gb/s/port 64x33 PECL Digital Crosspoint Switch	2500 ps	PECL	150 ps	150 ps pk-pk	3-45

Data Communications Products

Part	Description	Page
GA9101, GA9102	266/200 Mbaud Fibre-Channel ESCON Transmitter and Receiver	4-3
GA9103	266 Mbaud Fibre-Channel Encoder/Decoder	4-17
TQ9303	531/1063 Mbaud Fibre-Channel Encoder/Decoder	4-35
TQ9501, TQ9502	531/1063 Mbaud Fibre-Channel Transmitter and Receiver	4-61
TQ9525	2.5 Gb/s 20-bit Transceiver	4-77

Product Summary (continued)

Mixed Signal Products

Part	Description	Page
TQ6122	1 GS/s 8-Bit Digital-to-Analog Converter	5-3
TQ6124	1 GS/s 14-Bit Digital-to-Analog Converter	5-27

System Timing Products

Eleven-Output Clock Buffers

Part	Prop. Delay	Input Freq.	Output Freq.	Configuration	I/O	Skew (max.)	Jitter	Page
GA1085	-350 ps \pm 1000 (-MC1000)	24-105 MHz	24-105 MHz	2@1/2x $\frac{1}{2}$ phase shift, 4@1x, 4@1/2x or 2@1x $\frac{1}{2}$ phase shift,	TTL \pm 30 mA output drive	150 ps within group — 350 ps group-group	200 ps (max.) period-period — 400 ps (max.) random	6-3
GA1086	-350 ps \pm 500 (-MC500) or -350 ps \pm 1000 (-MC1000)	30-67 MHz	15-67 MHz	9@1x, 1@1/2x	TTL \pm 30 mA output drive	250 ps within group	75 ps (typ.)	6-13
GA1087	-350 ps \pm 500 (-MC500) or -350 ps \pm 700 (-MC700)	24-105 MHz	24-105 MHz	5@1x, 5@1/2x or 6@2x, 4@1x	TTL \pm 30 mA output drive	150 ps within group — 350 ps group-group	200 ps (max.) period-period — 400 ps (max.) random	6-25
GA1088	-350 ps \pm 500 (-MC500) or -350 ps \pm 700 (-MC700)	18-105 MHz	18-105 MHz	4@1x $\frac{1}{2}$ phase shift, 3@1x, 3@1/2x or 2@1x, 4@2x, 4@2x $\frac{1}{2}$ phase shift	TTL \pm 30 mA output drive	150 ps within group — 350 ps group-group	200 ps (max.) period-period — 400 ps (max.) random	6-35
TQ1089	-350 ps \pm 700 (-MC700)	130-180 MHz 65-90 MHz	130-180 MHz 65-90 MHz	1@1x, 9@1/2x or 2@2x, 8@1x	TTL \pm 30 mA output drive	150 ps within group — 350 ps group-group	200 ps (max.) period-period — 400 ps (max.) random	6-71
TQ1090	-350 ps \pm 700 (-MC700)	33-45 MHz 65-90 MHz 130-180 MHz	33-45 MHz 65-90 MHz 130-180 MHz	3@1x, 5@1/2x, 2@2x or 4@1x, 4@2x, 2@4x	TTL \pm 30 mA output drive	150 ps within group — 350 ps group-group	200 ps (max.) period-period — 400 ps (max.) random	6-81

Product Summary (continued)**System Timing Products** (continued)**Six-Output Clock Devices**

Part	Prop. Delay	Input Freq.	Output Freq.	Configuration	I/O	Skew (max.)	Page
GA1110E	±1 ns	-20: 20 MHz -25: 25 MHz -33: 33 MHz -40: 40 MHz -50: 50 MHz	20–50 MHz	6@1x $\frac{1}{2}$ phase shift	TTL ±24-mA output drive	1000 ps within group	6-45
GA1210E	±1 ns	-20: 20 MHz -25: 25 MHz -33: 33 MHz -40: 40 MHz -50: 50 MHz	20–100 MHz	2@1x, 4@2x or 2@1x, 2@2x, 2@1x $\frac{1}{2}$ phase shift	TTL ±24-mA output drive	1000 ps within group	6-59

High-Frequency Clock Generators

Part	Input Freq.	Output Freq.	I/O	Jitter	Page
TQ2059	20–35 MHz	200–350 MHz	TTL/PECL	30 ps (typ.) period–period	6-91
TQ2060	35–50 MHz	350–500 MHz	TTL/PECL	25 ps (typ.) period–period	6-97
TQ2061	25–35 MHz	500–700 MHz	TTL/PECL	25 ps (typ.) period–period	6-103

Wireless Communication Products and Foundry Services

For information on TriQuint's wireless communications products and foundry services, refer to the *Wireless Communications Products Data Book*.

Company Background

Introduction

TriQuint Semiconductor designs, develops, manufactures and markets a broad range of high-performance analog and mixed-signal gallium arsenide (GaAs) integrated circuits (ICs) for the telecommunications, data communications, computing, and wireless communications markets.

TriQuint engineers apply the company's proprietary GaAs technology to produce high-performance, low-cost ICs that give customers a competitive edge in their product strategies.

Inherent physical properties allow electrons to move approximately five times faster in GaAs than in silicon. This enables GaAs ICs to operate at much higher frequencies than silicon ICs — or to perform as fast while using substantially less power. GaAs also provides more linear amplification, can receive weaker signals due to its low-noise characteristics, and can transmit strong clean signals at lower voltages.

The company's major markets are currently growing at 35-50% annually. End-user customers include Alcatel, Cisco Systems, Digital Equipment, Ericsson, DSC Communications, Hughes, IBM, Lucent Technologies, Motorola, Nortel, Panasonic, Philips, Qualcomm, Siemens and StorageTek.

History

TriQuint Semiconductor was founded in 1985 at the Beaverton, Oregon, laboratories of Tektronix by a group who had undertaken the first GaAs research and development work in 1978.

Following a strong production-oriented approach from inception, TriQuint in 1988 became the first GaAs IC manufacturer to make the transition to 100 mm (4-inch) wafers.

In 1990, TriQuint was the first company to offer GaAs ICs in plastic packages for high-volume, low-cost radio frequency (RF) applications. That year the company also shipped its first space-qualified products for non-military communication satellite applications.

In 1991, three pioneering GaAs semiconductor companies — Gazelle Microcircuits, Gigabit Logic and TriQuint — merged under the TriQuint Semiconductor name. The focus of the new company was communications — cellular and other wireless phones, satellite communications, the long-distance fiber optic telecommunications market and computer networking. This focus has enabled TriQuint to average 30-35% annual growth.

TriQuint became a public company in December 1993, raising approximately \$17 million in its initial public offering. A follow-on stock offering in September 1995 raised a further \$48 million. TriQuint's stock trades under the symbol TQNT on NASDAQ.

In 1995, the overall growth rate increased to 50%, with year-end revenues of approx. \$46 million. Strong growth continued during 1996, as revenues increased to approximately \$60 million.

Also in 1996, TriQuint launched its Total Quality Management initiative, called Continuous Process Improvement (CPI). Quality Improvement Teams are formed from natural work groups or across departments to address specific quality issues, improve processes and increase the value to customers of TriQuint's services and products. Teams work on clearly defined tasks, document and analyze problems and processes, test and implement solutions, then track progress and monitor results.

In the fourth quarter of 1996, TriQuint became the first semiconductor company to install the innovative management information system designed by SAP. This leading-edge software combines real-time manufacturing, financial and sales information in a totally integrated on-line system to improve business efficiency and productivity.

In January 1997, TriQuint started moving operations to the new 27-acre corporate campus in Hillsboro. The 160,000 square foot complex includes a new wafer fabrication facility with greatly expanded production capability, with expanded sections for product testing and product and process development.

Output from the new facility is expected to meet anticipated demand through the year 2000. Additional space on the site will allow the company to further expand manufacturing operations in the future.

Technology and Markets

TriQuint has organized its GaAs design and manufacturing operations into two divisions, both addressing high-growth market segments: telecommunications/data communications and wireless communications.

TriQuint's Telecom/Datacom Division is one of two product divisions in the company. It serves the long-distance fiber optic telecommunications market, and also provides specialized products for general computing and electronics industries.

Telecom/Datacom is meeting the rising demand for GaAs solutions resulting from the increased bandwidth needs of new communications technologies, such as "fiber to the curb," asynchronous transfer mode (ATM), multimedia on the Internet and wireless local loop.

Computing products supplied by this Division are primarily targeted at high-speed serial data communication. Standard products include high-performance transmission and switching devices, high-speed digital-to-analog convertors, and system timing components.

The Wireless Communications Division serves the fast-growing markets for mobile telephones and computing. Wireless is moving to higher frequencies, requiring high-performance mobile phones. TriQuint's products and technology help meet the explosive global demand for portable, battery-powered communications devices.

Regulatory agencies around the world have created whole new communications markets by opening up additional frequencies for mobile telephony usage.

Many leading manufacturers of high-frequency digital wireless communications devices are implementing TriQuint's integrated gallium arsenide MESFET technology in wide variety of communications applications. GaAs' superior linearity and noise performance provide higher signal fidelity. Other benefits include more gain at low voltages and better power efficiency for longer battery life.

The higher levels of RF integration possible with TriQuint's GaAs technology reduces overall system costs by shortening the design cycle and speeding product development.

As cellular handsets become smaller and retail prices continue to plunge, a GaAs RFIC can replace the 20-30 discretes found in earlier generations of analog cellular phones, providing better performance, lower cost, smaller size, ease of manufacturing and faster time to market.

Manufacturing

TriQuint has recently relocated its manufacturing operations to an all new 160,000 square feet facility located on 27 acres in Hillsboro, Oregon. Fabrication facilities occupy 38,000 square feet and include 16,000 square feet of Class 10 clean room. The new facility will be capable of quadrupling current production rates by the year 2000. Product design, support and administrative offices are also located at the new site.

TriQuint's wafer fabrication facility produces 4-inch wafers using the company's high-volume, low-cost ion-implanted metal semiconductor field effect transistor (MESFET) processes. The company also provides foundry and manufacturing services. All TriQuint's operations are ISO 9001 certified.

TriQuint works with a number of strategic assembly and packaging houses in the US and overseas to meet demand for product. All wafer and final product testing is done at the TriQuint test facilities, primarily on high-volume automatic test equipment and associated handlers.

Partnerships

Since 1993, TriQuint has had a manufacturing partnership with Lucent Technologies, formerly AT&T Bell Labs. Under a joint development agreement, TriQuint has rights to certain intellectual property of Lucent. As part of a manufacturing services agreement, TriQuint processes GaAs wafers for Lucent.

TriQuint has ongoing manufacturing partnerships with Cirrus Logic, Cellnet and Motorola and in 1996 signed new agreements with Philips Semiconductors and Qualcomm.

Under a wafer sourcing and technology sharing agreement with Philips Semiconductors, TriQuint will manufacture a new range of GaAs monolithic microwave integrated circuit (MMIC) power amplifiers compatible with all emerging digital cellular and cordless telephone standards.

The agreement with Qualcomm is to jointly develop RFICs for CDMA PCS phones, including an RF receive component critical for compliance with the IS-95 CDMA standard and other RF ICs for wireless local loop and the Globalstar satellite system. Products and Services

TriQuint's standard products include high-performance, low-cost digital, analog and mixed-signal GaAs RFICs used in communications systems. The company also provides application-specific and custom circuit

solutions for major communication system original equipment manufacturers.

Telecommunications

TriQuint has a growing portfolio of products for broadband systems based on the system operation at synchronous optical network (SONET), synchronous digital hierarchy (SDH) and ATM standards. Typical functions include multiplexing and demultiplexing, clock generation and clock recovery.

Telecom and datacom applications include ATM, digital cross-connects, switch interfaces, wide area network (WAN) hubs and routers, SONET transmission and switching systems, workstations, servers, network interface cards, proprietary links and central office equipment.

TriQuint leads the market in low-jitter telecom products. Bellcore-compliant standard products at 622 Mbps provide unparalleled waveform fidelity with high edge rates, exceptionally wide eye openings and ultra-low jitter tolerance.

High quality mixed-signal phase-lock loop (PLL) technology enables TriQuint to produce telecommunications transceiver and serializer and deserializer chips with the best performance in the industry. These devices provide physical layer interfacing between industry-standard optoelectronic modules and industry-standard overhead processor and cellmapping products.

TriQuint is the world leader in crosspoint switches above 500 MHz, providing digital switching solutions with aggregate bandwidths of over 50 Gbps and channel bandwidths of up to 2.5 Gbps with standard crosspoint products.

In addition to telecom and datacom switches, TriQuint is a major supplier of switching products to the digital video market. Though operating at switching rates lower than maximum capacity, these products provide high video signal fidelity for greater design margins and higher-integrity data transfer.

The Telecom/Datacom Division's biggest market is SONET applications, where the company has established a strong market presence. TriQuint combines expertise in high-speed SONET circuit design with the proprietary process technology to deliver custom application-specific IC solutions.

Data Communications

In the datacom market, TriQuint focuses on high-speed serial data communications, the preferred method for high-volume data transfer. Data communication chipsets are available for the new 1 Gbps Fibre Channel standard and for proprietary serial links.

A broad range of serial communications devices incorporating exceptionally low-jitter, high-frequency PLL technology perform the serialization, CDR and deserialization functions. These support the physical interface requirements of Fibre Channel, ESCON, Gigabit Ethernet and proprietary links. In addition, TriQuint offers encoder/decoder (ENDEC) products for complete point-to-point serial communication links.

Operating at data rates from 200 Mb/s to 2.50 Gb/s, standard datacom products are compatible with copper and optical media drivers from original equipment manufacturers.

Combining high-noise immunity with low-jitter data transmission and exceptional jitter tolerance, TriQuint's

phase lock loop technology allows increased transmission length over fiber and copper transmission media at the low bit error rates required for advanced digital communication. Typical applications are disk arrays, high-speed ribbon cable replacement, data acquisition systems and other inter-system communications.

TriQuint also manufactures system timing components to synthesize and distribute precise clock signals in high-performance digital computing systems.

These products provide very low clock skew and increased timing margins for high-speed systems, using low-jitter, controlled-delay PLL technology and clock distribution buffers compatible with very high-fidelity transistor-transistor logic/complementary metal oxide semiconductor (TTL/CMOS) and positive emitter coupler logic (PECL).

TriQuint makes standard system timing products for designs based on Pentium™, PowerPC™ and Alpha AXP™ processors serving applications from 20 MHz to 700 MHz. Applications include low-skew clock distribution, board-to-board clock synchronization, multi-phase clocking and high-frequency clock generation.

Wireless Communications

Standard products supplied to wireless communications markets worldwide serve as the essential building blocks for multi-purpose applications in RF and microwave systems.

TriQuint applies its GaAs design and manufacturing technologies to supply industry-standard products for PCS networks, analog and digital cellular phones, satellite communication, satellite receivers for TV broadcast, wireless transceivers for data networks, hand-held navigation systems based on the global

positioning satellite (GPS) standard, wireless local area networks (WLANs) and wireless modems.

TriQuint's wireless communications standard products focus on simplifying the complex requirements of RF front end design. These devices address the essentials of radio frequency applications – power amplification, frequency conversion and switching.

Signal amplification is important for both transmit and receive functions. A receiver must be able to amplify weak incoming signals without adding noise. Above 500 MHz, as frequency increases, TriQuint power amplifiers generate less noise than silicon, while the power-added efficiency of GaAs enables them to operate at lower supply voltages and at higher efficiency.

TriQuint's GaAs technologies add significant value to frequency conversion functions. Incoming RF signals are down-converted to lower frequencies for easier processing and processed signals are up-converted before transmission. TriQuint downconverter and upconverter ICs reduce inter-signal interference and provide superior signal power gain during conversion, especially at higher operating frequencies.

Switches route signals between receiver, transmitter and other processing devices. TriQuint's low-loss switches minimize the loss of signal quality and signal strength. Switching devices are frequency integrated with frequency converters, low-noise amplifiers and power amplifiers.

Among TriQuint's newest wireless standard products is a dual-mode RF power amplifier IC for mobile phones operating in most of the cellular and PCS standards; a low-voltage RFIC downconverter for cellular and PCS frequencies; a monolithic transmit/receive amplifier/switch for spread-spectrum applications; a single-

supply single-pole double-throw (SPDT) RF switch; and dual-band products.

The company is also a world leader in foundry services to wireless markets, providing components for the global Groupe Speciale Mobile (GSM), DCS1800 and Personal Handyphone System (PHS) standards.

During 1996, TriQuint announced a total of 47 design wins in wireless handset applications involving 19 different customers. Most were for cellular and PCS applications and several were for wireless local loop systems, a new segment of the wireless communications market.

For more information on TriQuint's wireless communications products, refer to the *Wireless Communications Products Data Book*.

Contract Manufacturing Services

Electronics companies often need to integrate the functions of proprietary RF or high-speed mixed-mode systems into custom ICs to improve manufacturability, minimize component insertions, achieve higher yields and reduce costs. Since 1985, TriQuint engineers have developed the design tools and manufacturing infrastructure to serve the special needs of customers who design and develop their own GaAs circuits.

Manufacturing services range from wafer fabrication to test engineering and plastic packaging. Complete post-fabrication and product engineering services help customers better manage yields.

Expert staff guide customers through design to finished IC, providing full security for intellectual property while minimizing time to market. Design services include tools, training and support and referrals to design houses familiar with TriQuint's high-performance GaAs process technologies. Design tools include a digital and analog cell library of over 150 pre-designed components.

Several high-performance GaAs MESFET processes are available to implement IC designs. TriQuint's 1-micron enhancement/depletion mode MESFET processes is widely used for RF and mixed analog/digital circuits, supporting RF applications up to X-band and digital circuits of LSI complexity.

Newly available is the TQTRx, a next-generation 0.6-micron enhancement/depletion mode MESFET process that offers true integration of RF transmit and receive functions.

For more information on TriQuint's foundry services, refer to the *Wireless Communications Products Data Book*.



Section 2 — Telecommunications Products

<i>TQ8101C</i> SONET/SDH MDFP	<i>2-3</i>
<i>TQ8103</i> 622 Mb/s Clock & Data Recovery IC	<i>2-17</i>
<i>TQ8105/8106</i> SONET/SDH Transceiver/Transceiver with CDR	<i>2-27</i>

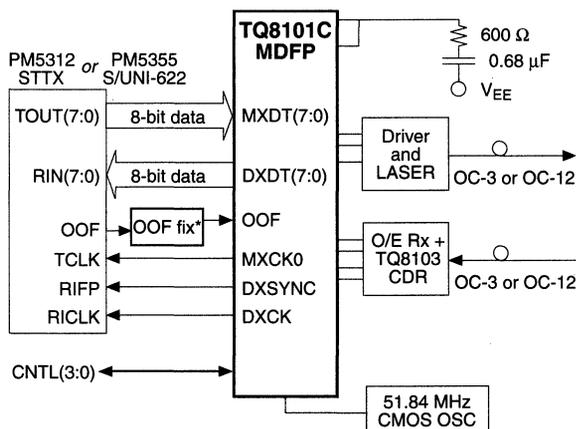
The TQ8101C is a SONET/SDH transceiver that integrates Multiplexing, Demultiplexing, SONET/SDH Framing, clock synthesis PLL (MDFP), and loopback functions in a single monolithic integrated circuit. Implementation with the TQ8101C requires only a simple external RC loop filter and standard TTL and ECL power supplies. For optimal performance, the TQ8101C MDFP is packaged in a 68-pin multilayer ceramic (MLC) surface-mount package with an integral CuW heat spreader. The TQ8101C provides an integrated solution for physical interfaces intended for use in STS-12/STM-4 (622.08-Mb/s) and STS-3/STM-1 (155.52-Mb/s) SONET/SDH systems.

The TQ8101C meets ANSI, Bellcore, and ITU requirements for a SONET/SDH device. With a 51.84-MHz reference clock, the phase-locked loop (PLL) provides 77.76-MHz or 19.44-MHz output for the multiplexer and 77.76-MHz or 19.44-MHz and 51.84-MHz output for the demultiplexer.

Typical SONET/SDH system applications for the TQ8101C include:

- Transmission system transport cards
- Switch and cross-connect line cards
- Repeaters
- ATM physical layer interfaces
- Test equipment
- Add/drop multiplexers

Figure 1. Logical Application



*Contact PMC-Sierra for application note.

TQ8101C

622/155 Mb/s SONET/SDH MDFP

Features

- Byte-wide Multiplexing, Demultiplexing, Framing, and PLL (MDFP) in one device
- Choice of STS-12/STM-4 or STS-3/STM-1 transmission rates
- Configurable master or slave reference clock generation and PLL bypass for external clocking
- 77.76 MHz or 19.44 MHz output for the multiplexer; 77.76 MHz or 19.44 MHz and 51.84 MHz output for the demultiplexer
- External RC loop filter
- Pass-through mode and three loopback modes for enhanced filed diagnostics
- Frame-synchronous and byte-aligned demultiplexer output, compliant with SONET and SDH
- Search, detect, and recovery of framing on out-of-frame input
- Standard TTL and differential or single-ended ECL I/O (except TXCK)
- Tristate TTL output for factory circuit-board testability
- 68-pin TriQuint MLC controlled-Z surface-mount package with integral heat spreader
- Dual-supply operation (+5V, -5.2V)
- Low power dissipation (2.3W nom.)

TQ8101C

Figure 2. TQ8101C Block Diagram

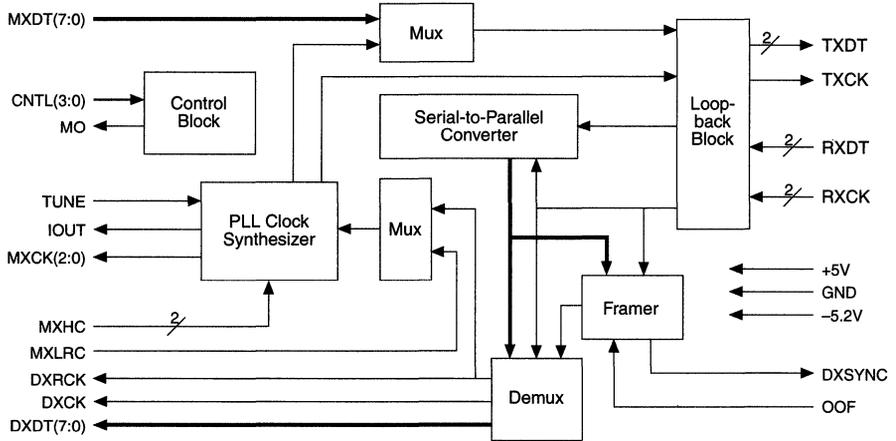
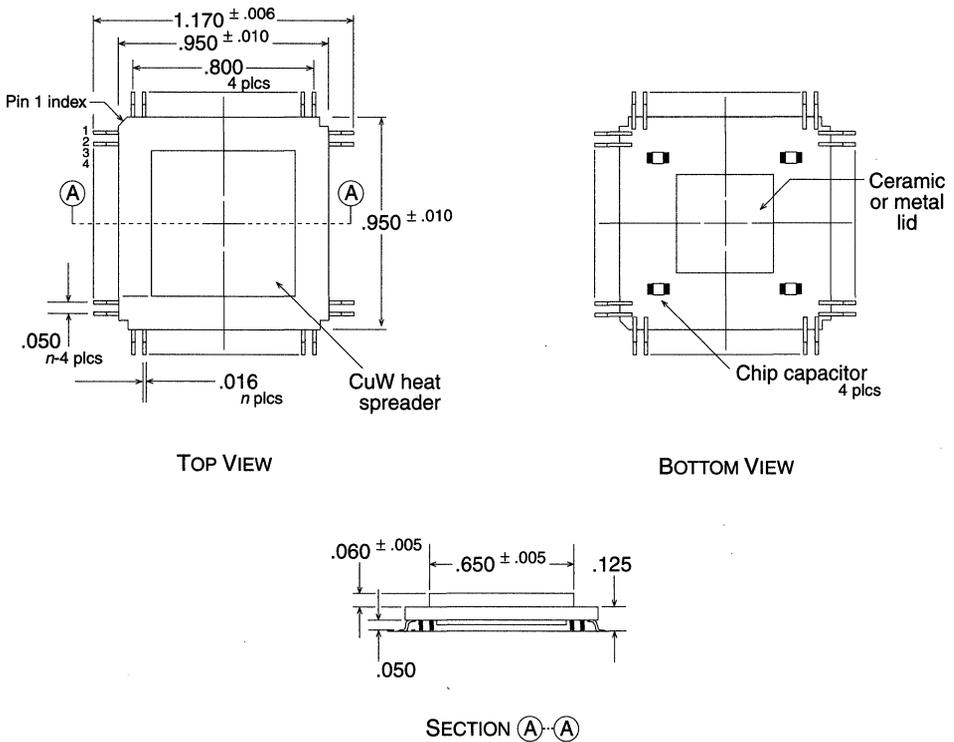


Figure 3. TQ8101C Package—68-pin MLC



Functional Description

Figure 2 shows a block diagram of the TQ8101C multiplexer, demultiplexer, framer, and PLL clock synthesizer (MDFP). The primary purpose of TQ8101C is to integrate the conversion of serial and parallel SONET/SDH data with bit alignment and clock synthesis in a single device.

Multiplexing

Byte-wide input data on MXDT(7:0)¹ is continuously strobed into the multiplexer on the rising edge of the multiplexer clock output, MXCK(2:0).² Any of these three MXCK pins may be used as a reference point for relative timing. (See Table 8 for setup, hold, and skew times. See Table 1 for clock selection options.)

Either an on-chip synthesized clock (see “PLL Clock Synthesis”) or an external high-speed multiplexer

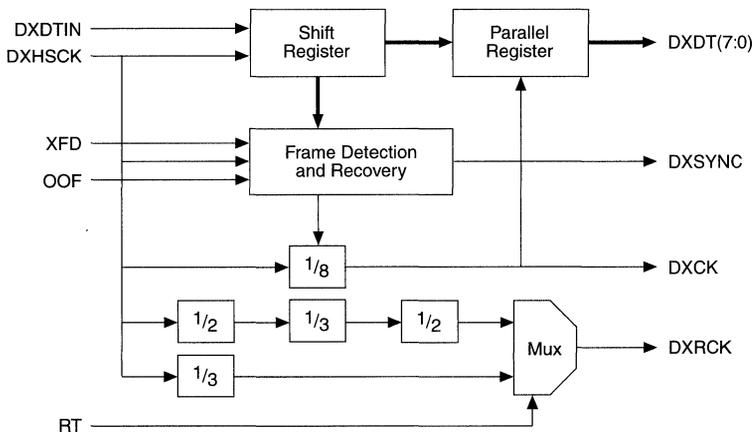
clock, MXHC, serializes the input data bytes. In the normal mode of operation, the serial data is then buffered as ECL-compatible output on TXDT. An ECL output is provided for the transmit clock, TXCK.

Demultiplexing

As shown in Figure 4, The demultiplexer block converts incoming serial data on DXDTIN³. Byte-wide output data is presented on DXDT(7:0)⁴ slightly after the falling edge of the output demultiplexer clock, DXCK. (See Table 8 for setup, hold, and skew times.)

The demultiplexer block also includes clock divider circuitry, which is used by the demultiplexer to control divide-by-8 output on DXCK. The MDFP provides a divide-by-3 or divide-by-12 output, DXRCK. (See Table 1 for mode selection options.)

Figure 4. Demultiplexer Functional Block



- Notes: 1. MXDT(0) is defined as the least significant bit.
- 2. MXCK(2:0) nominally runs at 77.76 MHz in STS-12/STM-4 mode, and at 19.44 MHz in STS-3/STM-1 mode.
- 3. Internal signal. See Figure 5, "TQ8101C Loopback Modes."
- 4. DXDT (0) is defined as the least significant bit.

TQ8101C

Framing

The demultiplexer block (see Figure 2) includes a frame-detection and recovery block. Regardless of the state of the OOF input signal, this block takes DXSYNC high for one period of DXCK whenever it detects a pattern of three "A1" bytes followed by three "A2" bytes.

Frame recovery is initiated by the rising edge of the OOF input signal. The recovery process involves a search for a bit rotation that satisfies the three-"A1"-three-"A2" byte pattern specified for SONET/SDH. Once the pattern is found, DXSYNC goes high and the bit rotation is synchronized to the correct byte boundaries. No further byte boundary adjustments are made, regardless of "A1"- "A2" indication, unless they have been preceded by an OOF rising edge.

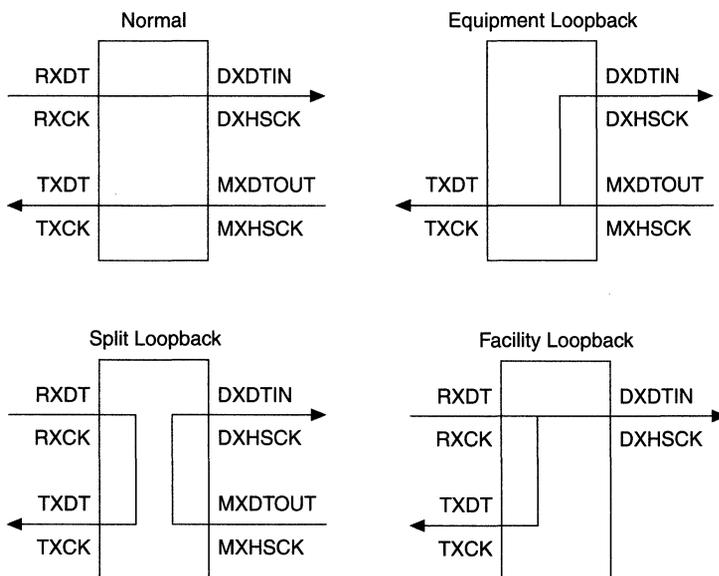
PLL Clock Synthesis

The PLL utilizes a monolithic voltage-controlled oscillator with a typical tuning constant of 50 to 100 MHz per volt on the TUNE input. This configuration provides jitter performance superior to other technologies. In a typical SONET/SDH application the TUNE input and charge pump output IOOUT are connected and tied to V_{EE} through a 600-ohm resistor and 0.68- μ F capacitor.

Loopback

The TQ8101C features four loopback modes: normal (pass-through), equipment loopback, split loopback, and facility loopback. Loopback modes are controlled by pins CNTL(3:0). Note that the loopback mode does not affect the latched selection of clock modes and rates. Note that the RXCK input is directly connected to the TXCK output in most loopback modes (see below).

Figure 5. TQ8101C Loopback Modes



Control

The signals on pins CNTL(3:0) can be used to control the clock rate, clock mode, loopback scheme, and tristate pins. Also, the internal PLL high-speed clock may be disabled, allowing an external clock source to be used on the MXHCN and MXHCP pins.

Note that the NAND tree enable normally is used only for device testing of the V_{IH} and V_{IL} parameters.

At power-up or during initialization, CNTL(3) should be set to logic 1. During reset, all internal counters, dividers, and loopback states, and the phase-frequency detector, are reset or deactivated. Note that frame search is initiated only by a rising edge on OOF.

Table 1. Modes of Operation

CNTL(3:0)	Modes of operation
0h	Reset
1h	Tristate all TTL outputs except DXRCK and MO
2h	NAND-tree test all TTL inputs except CNTL(3:0)
3h	DXRCK tristate
4h	Frame recovery disable
5h	Equipment loopback
6h	Facility loopback
7h	Split loopback
8h	Bypass, slave, internal VCO disabled, STS-3 rate
9h	Bypass, master, internal VCO disabled, STS-3 rate
Ah	Bypass, slave, internal VCO disabled, STS-12 rate
Bh	Bypass, master, internal VCO disabled, STS-12 rate
Ch	Normal, slave, internal VCO enabled, STS-3 rate
Dh	Normal, master, internal VCO enabled, STS-3 rate
Eh	Normal, slave, internal VCO enabled, STS-12 rate
Fh	Normal, master, internal VCO enabled, STS-12 rate

- Notes:
- "Bypass" indicates the use of the external high-speed clock in lieu of the internal transmit PLL.
 - "Normal" indicates use of the internal transmit PLL.
 - "Master" derives PLL timing from the reference 51.84-MHz oscillator input, MXLRC
 - "Slave" derives PLL timing from the demultiplexer clock input, RXCK.

TQ8101C

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Level	Minimum	Maximum	Unit
Positive supply	V_{CC}	—	0	7	V
Negative supply	V_{EE}	—	-7	0	V
Output voltage	V_O	ECL	$V_{EE} - 0.5$	+0.5	V
Output current	I_O	ECL	—	40	mA
Input voltage	V_I	ECL	$V_{EE} - 0.5$	+0.5	V
Input current	I_I	ECL	-1	1	mA
Output voltage	V_O	TTL	-0.5	$V_{CC} + 0.5$	V
Output current	I_O	TTL	—	20	mA
Input voltage	V_I	TTL	-0.5	$V_{CC} + 0.5$	V
Input current	I_I	TTL	-1	1	mA
Junction temperature	T_J	—	-55	+150	°C
Storage temperature	T_S	—	-65	+175	°C

Table 3. Recommended Operating Conditions

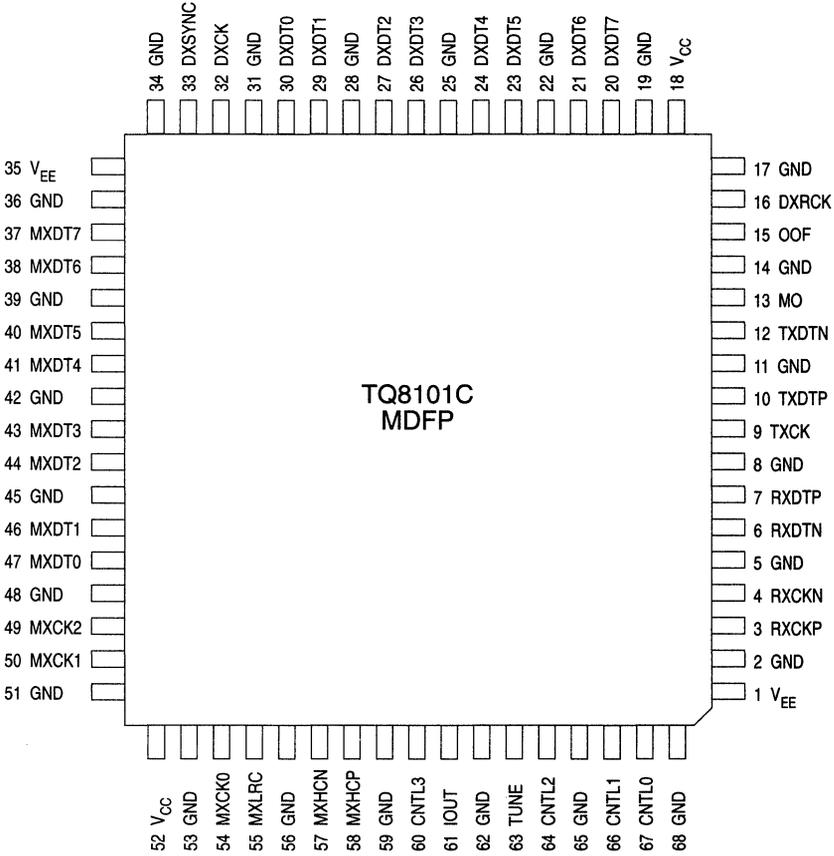
Parameter	Symbol	Minimum	Nominal	Maximum	Unit
Positive supply	V_{CC}	4.75	5	5.25	V
Negative supply	V_{EE}	-5.5	-5.2	-4.75	V
Operating ambient temperature	T_O	0		70	°C

Table 4. Power Consumption

Function	+5 V supply	-5.2 V supply	Unit
Nominal	40	320	mA
Max	55	420	mA

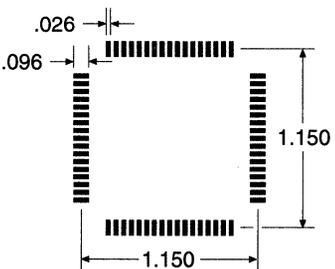
Parameter	Symbol	Level	Minimum	Maximum	Unit
Thermal resistance, junction-case	θ_{JC}			4	°C / W

Figure 6. Pinout Diagram
(heat spreader side—top view)



TELECOM
PRODUCTS

Figure 7. Recommended Package Footprint



TQ8101C

Table 5. Signal Descriptions

Pin	Signal	Type	Description
1	V _{EE}		Negative power supply input (-5.2V)
2	GND		Ground
3	RXCKP	In	Receive bit-serial clock; differential ECL, positive
4	RXCKN	In	Receive bit-serial clock; differential ECL, negative
5	GND		Ground
6	RXD _{TN}	In	Receive bit-serial data (MSB first); differential ECL, negative
7	RXD _{TP}	In	Receive bit-serial data (MSB first); differential ECL, positive
8	GND		Ground
9	TXCK	Out	Transmit bit-serial clock; single-ended ECL level
10	TXD _{TP}	Out	Transmit bit-serial data (MSB first); differential ECL, positive
11	GND		Ground
12	TXD _{TN}	Out	Transmit bit-serial data (MSB first); differential ECL, negative
13	MO	Out	NAND tree monitor output; TTL level
14	GND		Ground
15	OOF	In	Out of frame; TTL level; rising-edge initiated frame search
16	DXRCK	Tri Out	Demultiplexer reference clock; TTL level; 50-pF backplane driving capacity
17	GND		Ground
18	V _{CC}		Positive power supply input (+5.0V)
19	GND		Ground
20	DXDT7	Tri Out	Demultiplexer byte-serial data (bit 7); TTL level
21	DXDT6	Tri Out	Demultiplexer byte-serial data (bit 6); TTL level
22	GND		Ground
23	DXDT5	Tri Out	Demultiplexer byte-serial data (bit 5); TTL level
24	DXDT4	Tri Out	Demultiplexer byte-serial data (bit 4); TTL level
25	GND		Ground
26	DXDT3	Tri Out	Demultiplexer byte-serial data (bit 3); TTL level
27	DXDT2	Tri Out	Demultiplexer byte-serial data (bit 2); TTL level
28	GND		Ground
29	DXDT1	Tri Out	Demultiplexer byte-serial data (bit 1); TTL level
30	DXDT0	Tri Out	Demultiplexer byte-serial data (bit 0); TTL level
31	GND		Ground
32	DXCK	Tri Out	Demultiplexer byte-serial clock; TTL level
33	DXSYNC	Tri Out	Demultiplexer synchronization; TTL level
34	GND		Ground

(Continues on next page)

Table 5. Signal Descriptions (continued)

Pin	Signal	Type	Description
35	V _{EE}		Negative power supply input (-5.2V)
36	GND		Ground
37	MXDT7	In	Multiplexer byte-serial data (bit 7); TTL level
38	MXDT6	In	Multiplexer byte-serial data (bit 6); TTL level
39	GND		Ground
40	MXDT5	In	Multiplexer byte-serial data (bit 5); TTL level
41	MXDT4	In	Multiplexer byte-serial data (bit 4); TTL level
42	GND		Ground
43	MXDT3	In	Multiplexer byte-serial data (bit 3); TTL level
44	MXDT2	In	Multiplexer byte-serial data (bit 2); TTL level
45	GND		Ground
46	MXDT1	In	Multiplexer byte-serial data (bit 1); TTL level
47	MXDT0	In	Multiplexer byte-serial data (bit 0); TTL level
48	GND		Ground
49	MXCK2	Tri Out	Multiplexer byte-serial clock (bit 2); TTL level. See Table 1 for output rate.
50	MXCK1	Tri Out	Multiplexer byte-serial clock (bit 1); TTL level. See Table 1 for output rate.
51	GND		Ground
52	V _{CC}		Positive power supply input (+5.0V)
53	GND		Ground
54	MXCK0	Tri Out	Multiplexer byte-serial clock (bit 0); TTL level. See Table 1 for output rate.
55	MXLRC	In	Multiplexer low-speed reference clock (51.84 MHz); TTL level
56	GND		Ground
57	MXHCN	In	Multiplexer high-speed reference clock (max. 640 MHz); differential ECL, negative
58	MXHCP	In	Multiplexer high-speed reference clock (max. 640 MHz); differential ECL, positive
59	GND		Ground
60	CNTL3	In	Control (bit 3); TTL level
61	IOUT	Out	Tristate charge pump output (analog); connect to pin 63
62	GND		Ground
63	TUNE	In	VCO tune (analog); connect to external loop filter and pin 61
64	CNTL2	In	Control (bit 2); TTL level
65	GND		Ground
66	CNTL1	In	Control (bit 1); TTL level
67	CNTL0	In	Control (bit 0); TTL level
68	GND		Ground

TQ8101C

Table 6. DC Characteristics—ECL I/O (1)

Parameter	Condition	Symbol	Minimum	Nominal	Maximum	Unit
Internal ECL reference	(2)	V_{REF}	—	$0.26 V_{EE}$		mV
Common mode voltage	(3)	V_{COM}	-1500	—	-1100	mV
Differential voltage	(3)	V_{DIFF}	200	—	1200	mV
Input HIGH voltage	(4)	V_{IH}	-1100	—	-400	mV
Input LOW voltage		V_{IL}	V_{EE}	—	-1500	mV
Output HIGH voltage	(5)	V_{OH}	-1000	0	-500	mV
Output LOW voltage	(5)	V_{OL}	$V_{TT} - 100$	—	-1600	mV
Input HIGH current	$V_{IH (MAX)}$	I_{IH}	—	—	30	mA
Input LOW current	$V_{IL (MIN)}$	I_{IL}	—	—	-30	mA
Output HIGH current	(6)	I_{OH}	20	23	30	mA
Output LOW current	(6)	I_{OL}	-2	5	8	mA
Input capacitance		C_{IN}	—	3	—	pF
Output capacitance		C_{OUT}	—	3	—	pF
ESD breakdown	(1)	V_{ESD}	500	—	—	V

Table 7. DC Characteristics—TTL I/O (1)

Parameter	Condition	Symbol	Minimum	Nominal	Maximum	Unit
Input HIGH voltage		V_{IH}	2.0	—	V_{CC}	V
Input LOW voltage		V_{IL}	0	—	0.8	V
Input HIGH current	$V_{IH (MAX)}$	I_{IH}	—	—	100	mA
Input LOW current	$V_{IL (MIN)}$	I_{IL}	-100	—	—	mA
Output HIGH voltage	$I_{OH} = 3 \text{ mA}$	V_{OH}	2.4	—	V_{CC}	V
Output LOW voltage	$I_{OL} = -1 \text{ mA}$	V_{OL}	0	—	0.4	V
Tristate current		I_{OZ}	-100	—	100	mA
Input capacitance		C_{IN}	—	8	—	pF
Output capacitance		C_{OUT}	—	10	—	pF
ESD breakdown	(1)	V_{ESD}	1000	—	—	V

Notes (tables 6 and 7):

1. Specifications apply over recommended operating ranges.
2. Single-ended inputs
3. Differential inputs
4. $V_{REF} = -1300 \text{ mV}$
5. $R_{LOAD} = 50 \text{ ohms}$ to $V_{TT} = -2.0\text{V}$
6. Not tested; consistent with V_{OH} and V_{OL} tests

Table 8. AC Characteristics

Parameter	Symbol	Minimum	Nominal	Maximum	Unit
RXCK clock period	$T_{C(RXCK)}$	1.6	—	—	ns
MXHC clock period	$T_{C(MXHC)}$	1.6	—	—	ns
TXCK clock period	$T_{C(TXCK)}$	1.6	—	—	ns
MXCK clock period	$T_{C(MXCK)}$	12.8	—	—	ns
DXCK clock period	$T_{C(DXCK)}$	12.8	—	—	ns
MXLRC clock period	$T_{C(MXTRC)}$	18.87	19.29	19.61	ns
DXRCK clock period	$T_{C(DXRCK)}$	4.80	19.29	—	ns
RXCK clock duty cycle	$T_{DC(RXCK)}$	30	50	70	%
MXHC clock duty cycle	$T_{DC(MXHC)}$	30	50	70	%
TXCK clock duty cycle	$T_{DC(TXCK)}$	40	50	60	%
MXCK clock duty cycle	$T_{DC(MXCK)}$	40	50	60	%
DXCK clock duty cycle	$T_{DC(DXCK)}$	40	50	60	%
MXLRC clock duty cycle	$T_{DC(MXIRC)}$	30	50	70	%
DXRCK clock duty cycle	$T_{DC(DXRCK)}$	40	50	60	%
High-speed rise/fall time ¹ (more than 79 MHz)	$T_{H(R/F)}$	—	—	320	ps
Low-speed rise/fall time ¹ (less than 79 MHz)	$T_{L(R/F)}$	—	—	2.56	ns
CNTL(2:0) Setup Time to CNTL(3)	$T_{S(CNTL)}$	5500	—	—	ps
CNTL(2:0) Hold Time to CNTL(3)	$T_{H(CNTL)}$	2000	—	—	ps
RXDT setup time to RXCK	$T_{S(RXDT)}$	225	—	—	ps
RXDT hold time to RXCK	$T_{H(RXDT)}$	125	—	—	ps
OOF rising edge before A1 changes to A2	$T_{(OOFH)}$	51.44	—	—	ns
OOF pulse width	$T_{(OOFPW)}$	12.86	—	—	ns
DXSYNC rising edge from parallel data output change from A1 to A2	$T_{(DSYNC)}$	—	25.72	—	ns
DXSYNC pulse width	$T_{(DXSYNCPW)}$	12.86	—	—	ns
DXCK falling edge to valid parallel data output	$T_{P(DXDT)}$	$T_{C(RXCK)}$	$T_{C(RXCK)} + 0.5$	$T_{C(RSCK)} + 1.5$	ns
MXDT(0:7) setup time to MXCK	$T_{S(MXDT)}$	4500	—	—	ps
MXDT(0:7) hold time to MXCK	$T_{H(MXDT)}$	-2000	—	—	ps
TXCK falling edge to TXDT	$T_{P(TXDT)}$	—	—	500	ps

Notes: 1. 20% to 80% of min V_{OH} and max V_{OL} levels.

Figure 8. Input Timing

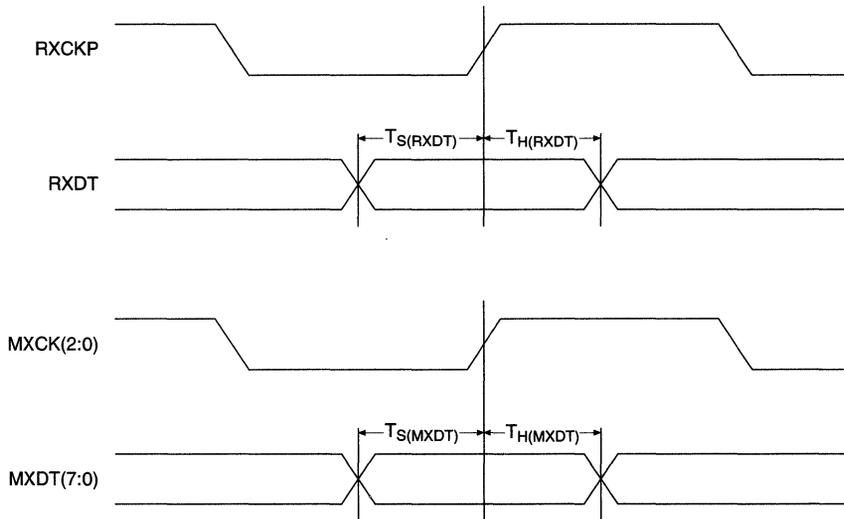


Figure 9. Output Timing

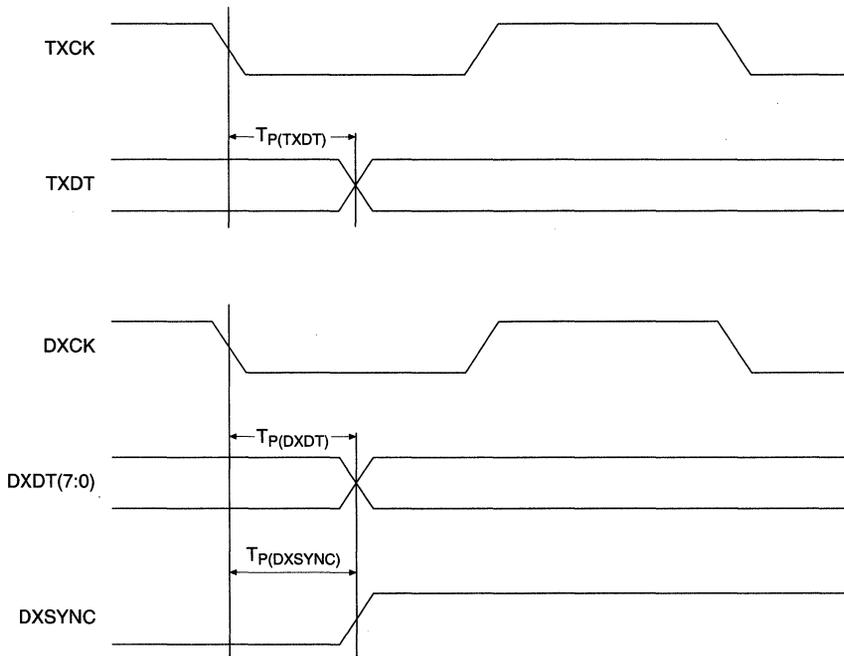


Figure 10. Multiplexer Timing

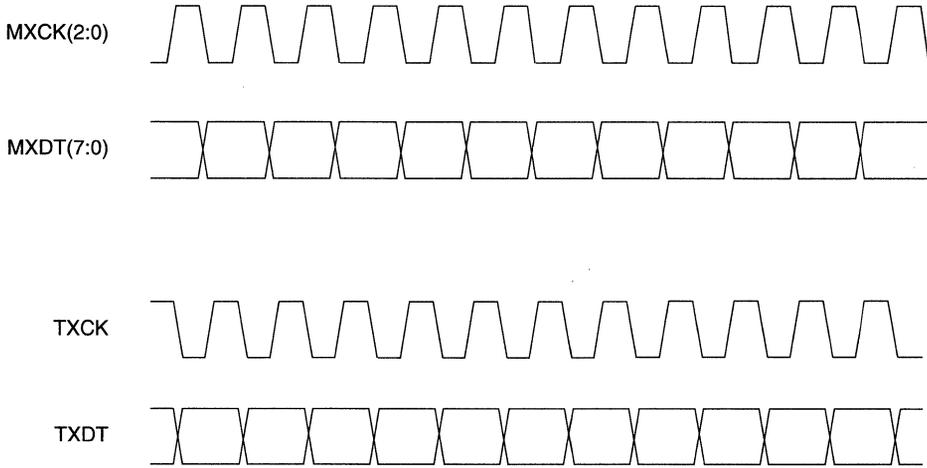
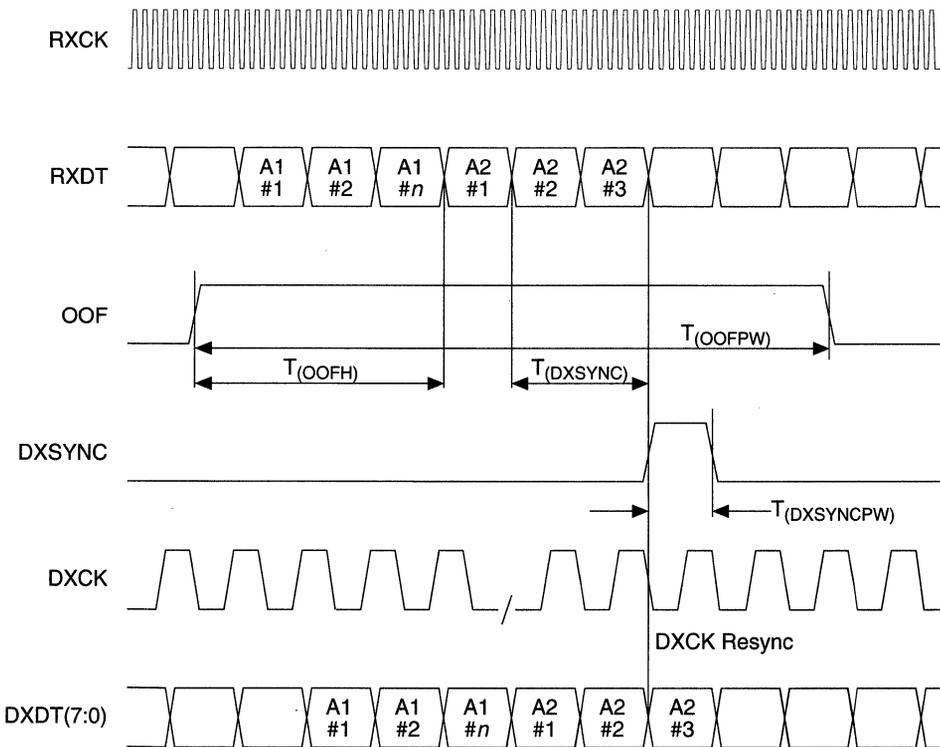


Figure 11. Demultiplexer Timing



SONET/SDH Considerations

Jitter Tolerance

This measurement does not apply to the TQ8101C, since data is transmitted from the input parallel bus relative to a TQ8101C-generated clock output (MXCK[2:0]). The user must meet setup and hold time requirements in order to ensure that data tracking is maintained.

Jitter Generation

By exploiting material characteristics, fully differential SCFL logic, and on-chip reactive elements, the TQ8101C typically has a jitter generation of 0.008 UI RMS (where 1 UI is 1/622.08E06) using recommended loop filter component values.

Ordering Information

TQ8101-M *SONET/SDH MDFP*

Evaluation Board Please contact a TriQuint representative or the factory for availability and pricing.

Additional Information

For latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com Tel: (503) 615-9000

Email: sales@tqs.com Fax: (503) 615-8900

For technical questions and additional information on specific applications:

Email: applications@tqs.com

The information provided herein is believed to be reliable; TriQuint assumes no liability for inaccuracies or omissions. TriQuint assumes no responsibility for the use of this information, and all such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. TriQuint does not authorize or warrant any TriQuint product for use in life-support devices and/or systems.

Copyright © 1997 TriQuint Semiconductor, Inc. All rights reserved.

Revision 1.0.A October 1997

A Principal Member of



The ATM Forum



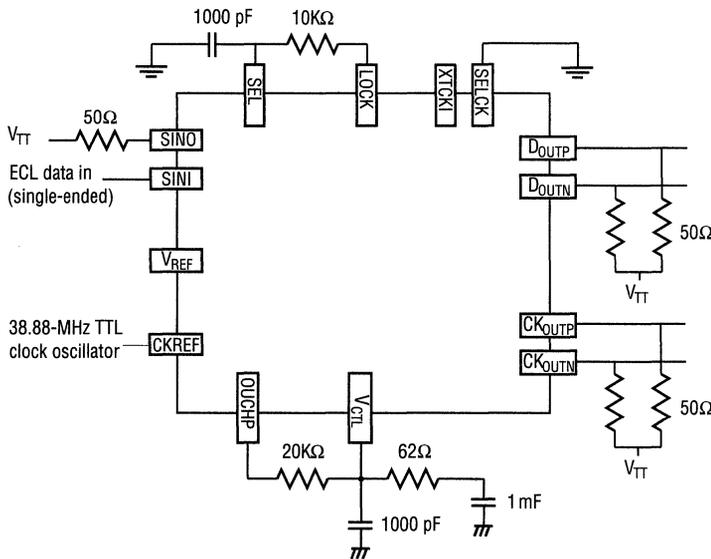
The TQ8103 is a monolithic clock and data recovery (CDR) IC that receives NRZ data, extracts the high-speed clock, and presents the separated data and clock as its outputs. This device is designed specifically for SONET OC-12 and SDH STM-4 applications at 622 Mb/s.

Its on-chip phase-locked loop (PLL) generates a stable 622.08 Mb/s reference based upon an external 38.88 MHz TTL reference. The PLL is based on a VCO constructed from integrated reactive components, which form a low-jitter, high-Q differential tank circuit. Both frequency- and phase-detect circuits reliably acquire and hold lock in worst-case SONET jitter conditions and scrambling patterns. The lock-detect circuitry signals when the CDR acquires frequency lock.

Typical SONET/SDH system applications for the TQ8103 include:

- Transmission system transport cards
- Switch and cross-connect line cards
- ATM physical layer interfaces
- Test equipment
- Add/drop multiplexers

Figure 1. Typical Application



TQ8103

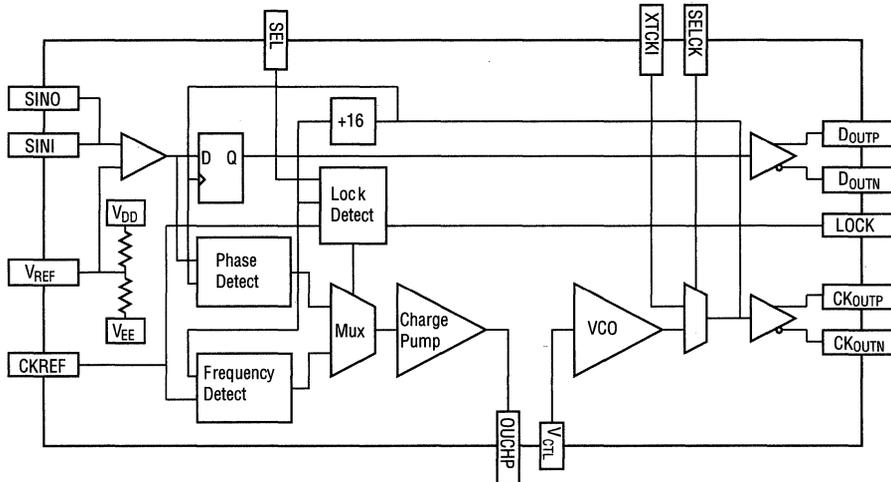
622 Mb/s Clock & Data Recovery

TELECOM PRODUCTS

Features

- Single-chip CDR circuit for 622 Mb/s data
- Exceeds Bellcore and ITU jitter tolerance maps
- Single-ended ECL input has loop-through path for external 50 ohm termination to minimize stubs and reflections
- Clock and data outputs are differential ECL
- Provides complete high-speed OC-12/STM-4 solution when used with TQ8101 or TQ8105 Mux/Demux/Framer/PLL
- External loop filter requires simple passive network
- Maintains clock in absence of data
- 28-pin leaded chip carrier
- Can be used with a high-speed external clock

Figure 2. TQ8103 Block Diagram



Functional Description

The TQ8103 CDR integrates separate detectors for acquiring frequency lock and maintaining precise phase lock. When the CDR is locked onto an incoming NRZ data stream, its phase-detect circuitry compares the phase of the incoming NRZ data and the phase of the generated 622.08 MHz clock. When they differ, the resulting error signal nulls the phase difference and puts the generated 622.08 MHz clock back in phase with the incoming data. In this mode, the LOCK output is high.

The phase-detect circuit operates only when the incoming NRZ data transitions between states. SONET and SDH employ scrambling, which provides an average transition density of 50 percent; however, some data patterns can generate legitimate scrambled signals with a significant number of consecutive ones or zeros. The TQ8103 maintains lock over bit sequences of over 100 consecutive zeros or ones.

When the input data is lost or too many bit times occur without a transition, the PLL (which generates the 622.08 MHz clock) eventually drifts. The lock-detect circuit constantly compares the generated 622.08 MHz clock (divided by 16) and the external 38.88 MHz

reference. When the PLL drifts more than 2000 PPM from the reference, the LOCK output goes low.

The SEL input selects between the phase-detect and frequency-detect circuits. When the PLL drifts out of lock, taking SEL low reverses the drift by switching in the frequency-detect circuit. Connecting the LOCK output directly to the SEL input should ensure that frequency lock is maintained in the absence of data. It is recommended, however, that a low-pass filter be added between LOCK and SEL to allow for orderly transitions between these circuits. Once the PLL frequency is within 500 PPM of the reference, the LOCK output returns high. As the SEL input goes high, the phase-detect circuit again maintains lock to the incoming NRZ data.

The TQ8103 can also be used as a standalone 622.08 MHz frequency reference. When SEL is held low, the PLL utilizes only the frequency-detect circuit. The PLL locks onto the external 38.88 MHz reference to generate the desired 622.08 MHz output.

Application Information

Loop Filter Design

The TQ8103 requires an external loop filter. Care should be taken in the implementation of the filter. Good high-frequency design techniques should be used, with the loop filter being connected into the analog ground. The analog supply should be well filtered.

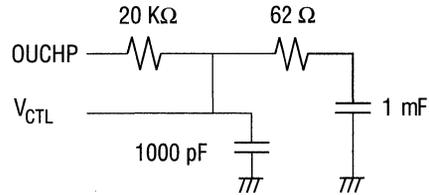
Data Input Considerations

The serial data input line is a high-frequency ECL signal, and should be kept in a 50 ohm controlled impedance environment. Reflections on the serial input are minimized through the use of a separate loopback termination pin, SINO. A 50 ohm chip resistor between SINO and V_{TT} minimizes stub length for the best signal quality. Another physical design consideration is to place the TQ8103 and its companion high-speed ICs as close as possible to the optics while observing good analog design practice on supply filtering and grounding.

External Frequency Reference

The externally supplied 38.88 MHz CKREF input needs to have low jitter with fast rise and fall times. Typical applications will use a telecom crystal oscillator such as the Connor-Winfield S14R6-38.88. SONET requires frequency sources to be accurate to ± 20 ppm over temperature, voltage, and aging. The CKREF input is a reference frequency for initial frequency lock and for the lock-detect circuit, so it can tolerate accuracies of up to ± 100 ppm.

Figure 3. External Loop Filter



Jitter Tolerance

Jitter tolerance describes the ability of the CDR circuit to track timing variations (jitter) in the received signal. The Bellcore and ITU specifications allow the received optical signal to contain jitter. The amount of jitter that must be tolerated is a function of the frequency content of the jitter. The CDR must tolerate many unit intervals (bit times) of low-frequency jitter, but is not asked to tolerate large amounts of jitter at higher frequency. The performance shown in the “Typical Performance Data” section shows that the TQ8103 offers a wide margin over the specification limits.

Jitter tolerance is a system-level issue that is directly affected by the quality of the optics, the quality of the layout (and decoupling), and the specific implementation of the loop filter. The recommended loop filter, described above, has been chosen to provide a robust margin on jitter tolerance.

TQ8103

Figure 4. TQ8103 Pinout

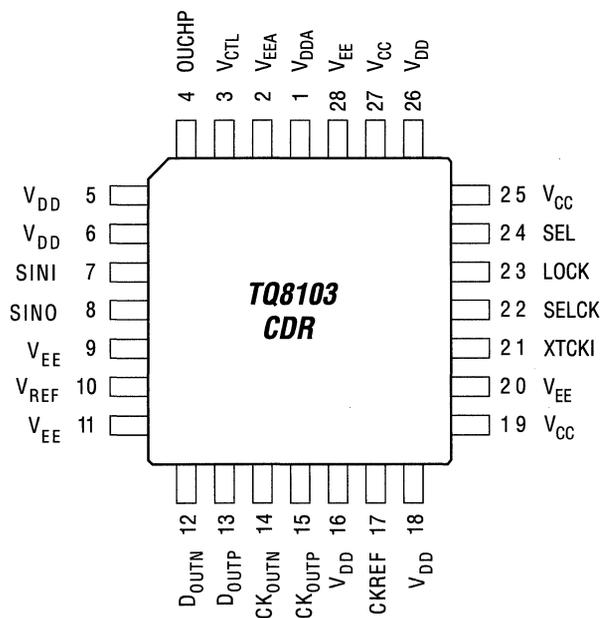


Table 1. Signal Descriptions

Pin	Signal	Type	Description
1	V _{DDA}	Supply	Analog ground for VCO
2	V _{EEA}	Supply	Analog -5V supply for VCO
3	V _{CTL}	Analog In	VCO control voltage input; connect to loop filter
4	OUCHP	Analog Out	Charge pump output; connect to loop filter
5	V _{DD}	Supply	Ground (0V)
6	V _{DD}	Supply	Ground (0V)
7	SINI	ECL In	Serial data input
8	SINO	ECL Term	Loopback of SINI for termination of serial data input; connect with 50 Ω to V _{TT}
9	V _{EE}	Supply	-5V supply
10	V _{REF}	Analog	Optional reference voltage for single-ended ECL input
11	V _{EE}	Supply	-5V supply
12	D _{OUTN}	ECL Out	Differential data output, complement
13	D _{OUTP}	ECL Out	Differential data output, true
14	CK _{OUTN}	ECL Out	Differential clock output, complement

(Continued on next page)

Table 1. Signal Descriptions (continued)

Pin	Signal	Type	Description
15	CK _{OUTP}	ECL Out	Differential clock output, true
16	V _{DD}	Supply	Ground (0V)
17	CKREF	TTL In	Reference clock input for frequency detect and lock detect
18	V _{DD}	Supply	Ground (0V)
19	V _{CC}	Supply	+5V supply
20	V _{EE}	Supply	-5V supply
21	XTCKI	ECL In	External clock input; selected using SELCK
22	SELCK	TTL In	External clock select: low = internal VCO, high = XTCLK
23	LOCK	TTL Out	Lock-detect output
24	SEL	TTL In	Detection circuit select; low = frequency-detect, high = phase-detect
25	V _{CC}	Supply	+5V supply
26	V _{DD}	Supply	Ground (0V)
27	V _{CC}	Supply	+5V supply
28	V _{EE}	Supply	-5V supply

Specifications

Table 2. Recommended Operating Conditions

Parameter	Symbol	Minimum	Nominal	Maximum	Unit
Positive supply	V _{CC}	4.5	5	5.5	V
Negative supply	V _{EE}	-5.5	-5	-4.75	V
Termination voltage	V _{TT}	-1.9	-2.0	-2.1	V
Operating ambient temperature	T _A	0		85	°C

Table 3. Power Consumption

Parameter	Symbol	Minimum	Nominal	Maximum	Unit
Positive supply current	I _{CC}			5	mA
Negative supply current	I _{EE}			210	mA
Thermal impedance	θ _{JA}		4.0		°C/W

Note: These values supersede the recommended operating conditions (Table 2) unless otherwise noted.

TQ8103

Table 4. DC Characteristics—ECL I/O (1)

Parameter	Condition	Symbol	Minimum	Nominal	Maximum	Unit
Internal ECL reference	(2)	V_{REF}		-1300		mV
Input HIGH voltage	(3)	V_{IH}	-1100		-700	mV
Input LOW voltage	(3, 4)	V_{IL}	V_{TT}		-1500	mV
Output HIGH voltage	(5)	V_{OH}	-1000	0	-700	mV
Output LOW voltage	(5)	V_{OL}	V_{TT}		-1600	mV
Input HIGH current	(6)	I_{IH}		10		μ A

Table 5. DC Characteristics—TTL I/O (1)

Parameter	Condition	Symbol	Minimum	Nominal	Maximum	Unit
Input HIGH voltage		V_{IH}	2.0		V_{CC}	V
Input LOW voltage		V_{IL}	0		0.8	V
Input HIGH current	$V_{IH(MAX)}$	I_{IH}			100	μ A
Input LOW current	$V_{IL(MIN)}$	I_{IL}	-100			μ A
Output HIGH voltage	$I_{OH} = 3$ mA	V_{OH}	2.4		V_{CC}	V
Output LOW voltage	$I_{OL} = -1$ mA	V_{OL}	0		0.4	V
Input capacitance	(6)	C_{IN}		8		pF
Output capacitance	(6)	C_{OUT}		10		pF

Table 6. AC Characteristics (1)

Parameter	Condition	Symbol	Minimum	Nominal	Maximum	Unit
Clock to data time	Figure 5	t_0	100		350	ps
Data output rise/fall times	(7)	t_R, t_F			350	ps
Clock output rise/fall times	(7)	t_R, t_F			300	ps
TTL output rise/fall times	(8)	t_R, t_F		5		ns
Acquire time	(9)			3		ms

Notes (Tables 4, 5, and 6):

1. Applies over recommended operating range
2. Single-ended inputs, $V_{EE} = -5V$
3. $V_{REF} = -1300$ mV
4. $V_{TT} = -2.0V$
5. $R_{LOAD} = 50$ ohms to $V_{TT} = -2.0V$
6. Not tested; consistent with V_{OH} and V_{OL} tests
7. 50 ohm load, 20% to 80% levels
8. 20 pF load, 0.8V to 2.0V
9. With recommended loop filter

Figure 5. Clock-to-Data Timing

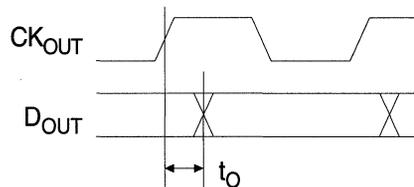


Table 7. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Nominal	Maximum	Unit
Positive supply	V_{CC}		0	7	V
Negative supply	V_{EE}		-7	0	V
Output voltage	V_O	ECL	$V_{EE} - 0.5$	+0.5	V
Output current	I_O	ECL	—	40	mA
Input voltage	V_I	ECL	$V_{EE} - 0.5$	+0.5	V
Input current	I_I	ECL	-1	1	mA
Output voltage	V_O	TTL	-0.5	$V_{CC} + 0.5$	V
Output current	I_O	TTL		20	mA
Input voltage	V_I	TTL	-0.5	$V_{CC} + 0.5$	V
Input current	I_I	TTL	-1	1	mA
Junction temperature	T_J		-55	+150	° C
Storage temperature	T_S		-65	+175	° C
Power dissipation	P_D			2	W

- Notes:
- If the device is subjected to the listed conditions, its reliability may be impaired.
 - Beyond the listed conditions, the safety of the device cannot be guaranteed.

Typical Performance Data

Figure 6. Jitter Tolerance

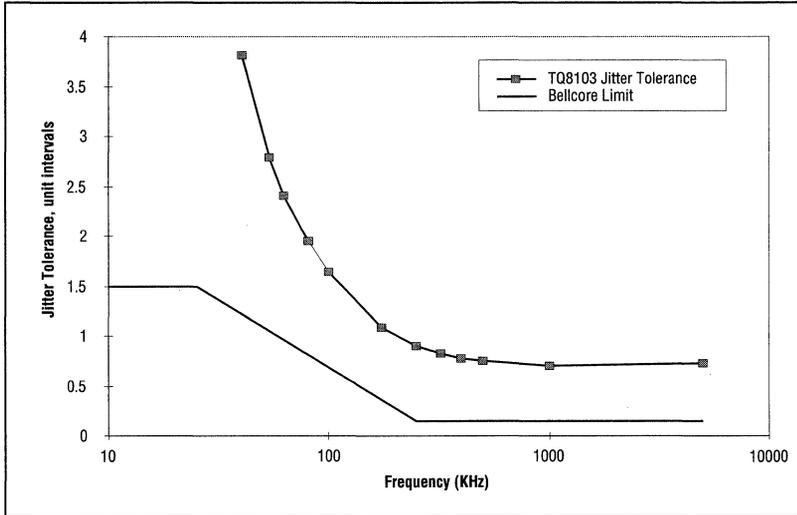


Figure 7. Output Eye Diagram with extracted clock

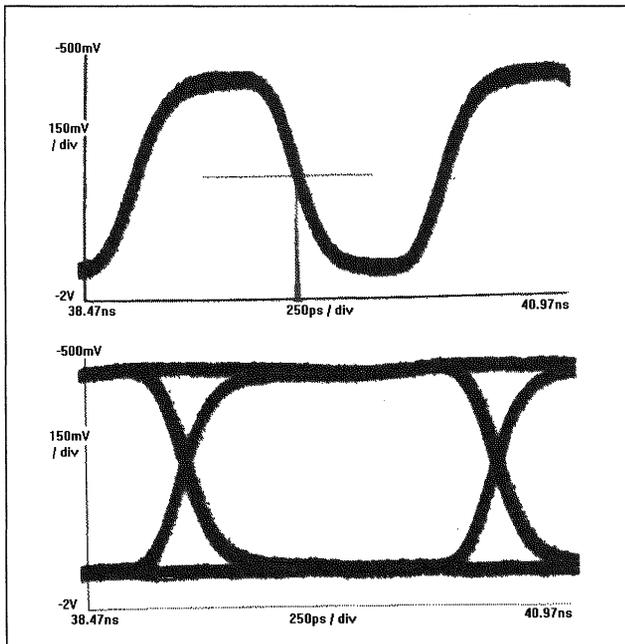
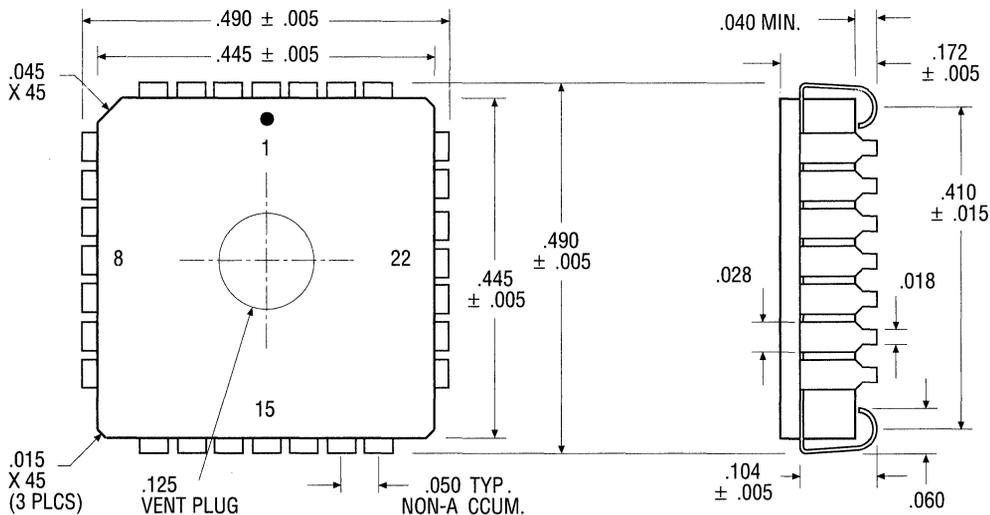


Table 8. Typical Performance Data

Waveforms	2012
PRBS data pattern	2 ⁻²³
RMS jitter	7.855 ps
Peak-to-peak jitter	55 ps

Mechanical Specifications

Figure 8. TQ8103 Package Dimensions



TELECOM
PRODUCTS

Ordering Information

TQ8103-Q 622 Mb/s Clock & Data Recovery IC in 28-pin MQuad Package

ETF-8103 Evaluation Board

Additional Information

For latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com Tel: (503) 615-9000
Email: sales@tqs.com Fax: (503) 615-8900

For technical questions and additional information on specific applications:

Email: applications@tqs.com

A Principal Member of

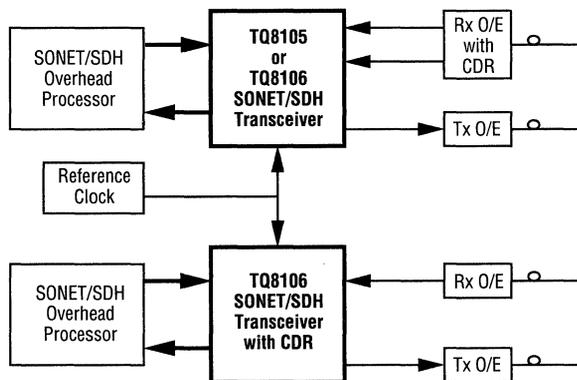


The ATM Forum

The information provided herein is believed to be reliable; TriQuint assumes no liability for inaccuracies or omissions. TriQuint assumes no responsibility for the use of this information, and all such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. TriQuint does not authorize or warrant any TriQuint product for use in life-support devices and/or systems.

Copyright © 1997 TriQuint Semiconductor, Inc. All rights reserved.

Revision 1.0.A October 1997



The TQ8105/TQ8106 are SONET/SDH transceivers that integrate multiplexing, demultiplexing, SONET/SDH framing, clock-synthesis PLL, and enhanced line and clock diagnostic functions into a single monolithic device. The TQ8106 is a pin-compatible upgrade of the TQ8105 that provides a Clock and Data Recovery (CDR) function. The TQ8105 and TQ8106 allow maximum flexibility in the selection of internal/external Clock and Data Recovery, Opto-Electronic (O/E) Module, and Reference Clock Sources.

On-chip PLLs use external RC-based loop filters to allow custom tailoring of loop response and support the wide range of reference clock frequencies found in SONET/SDH/ATM systems. For transmit clock synthesis or for CDR, the PLLs exceed ANSI, Bellcore, and ITU jitter specifications for systems when combined with industry-typical O/E devices such as Sumitomo, AT&T, HP, and AMP. The TQ8105/TQ8106 PLLs provide byte clocks and constant-rate 38.88 MHz and 51.84 MHz synthesized clock outputs, providing clocking for UTOPIA and other system busses. Transmit data may also be clocked into the devices with respect to the reference clock.

Operating from a single +5V supply, the TQ8105/TQ8106 provides fully compliant functionality and performance, utilizing direct-connected PECL levels (differential or single-ended) for high-speed I/O. As compared to AC-coupled schemes, the direct-coupled connections reduce jitter and switching-level offsets due to data patterns. The TQ8105/TQ8106 can also provide direct connection to high-speed I/O utilizing ECL levels with a -5V supply. Low-speed bus, control, and clock I/O utilize TTL levels. (An ECL/PECL reference clock input is also provided; at 155.52 MHz the input should be only PECL/ECL.) Output TTL pins can be tristated and may also be configured for 3.3V V_{OH} with a 3.3V supply connection.

TQ8105/8106

PRELIMINARY DATA SHEET

SONET/SDH Transceivers

Features

- Single-chip byte-wide Mux, Demux, Framers, and Tx clock-synthesis PLL with enhanced diagnostics
- TQ8106 includes monolithic Clock and Data Recovery
- SONET/SDH/ATM compliant for STS-12/STM-4 (622 Mb/s) or STS-3/STM-1 (155 Mb/s) rates
- 155.52, 77.76, 51.84, 38.88, or 19.44 MHz reference clock inputs with TTL, PECL, or ECL level
- 38.88 MHz and 51.84 MHz clock outputs for UTOPIA as well as byte clock rate (77.76 or 19.44 MHz)
- External RC-based loop filters
- Integrated loopbacks with enhanced line and reference clock diagnostics
- Direct-coupled standard PECL high-speed I/O with ECL option
- Clean TTL interface to PMC-Sierra devices
- 100-pin 14X14-mm JEDEC plastic package
- +5V-only supply for PECL I/O (-5.2V required for ECL I/O option)
- -40 to +125°C case operating temperature

TQ8105/TQ8106

PRELIMINARY DATA SHEET

The combination of a thermally enhanced 100-pin JEDEC metric plastic package, the low power dissipation of the device, and the wide case-temperature range permits operation without a heat sink in most designs.

The TQ8106 uses the same pinout as the TQ8105 and is reverse-compatible with it.

The TQ8105/TQ8106 provides comprehensive integrated loopback functionality and enhanced line and reference clock diagnostics required of SONET/SDH systems, minimizing additional external circuitry.

TQ8105/TQ8106 diagnostics include:

- Loss of Reference clock detector (LOR) output to indicate that the PLL Reference Clock is not toggling
- Lock indicator (RLOCK), which permits monitoring of the receiver clock frequency, flagging when the frequency drifts beyond approximately 500 ppm
- Loss of signal (LOS) detector output to indicate that the incoming data stream has no data transitions in 128-bit periods
- ECL/PECL input (NSOL) to allow LOS from an O/E module to force the data stream to all zeroes, eliminating the need for external glue logic

Figure 1. TQ8105 Block Diagram

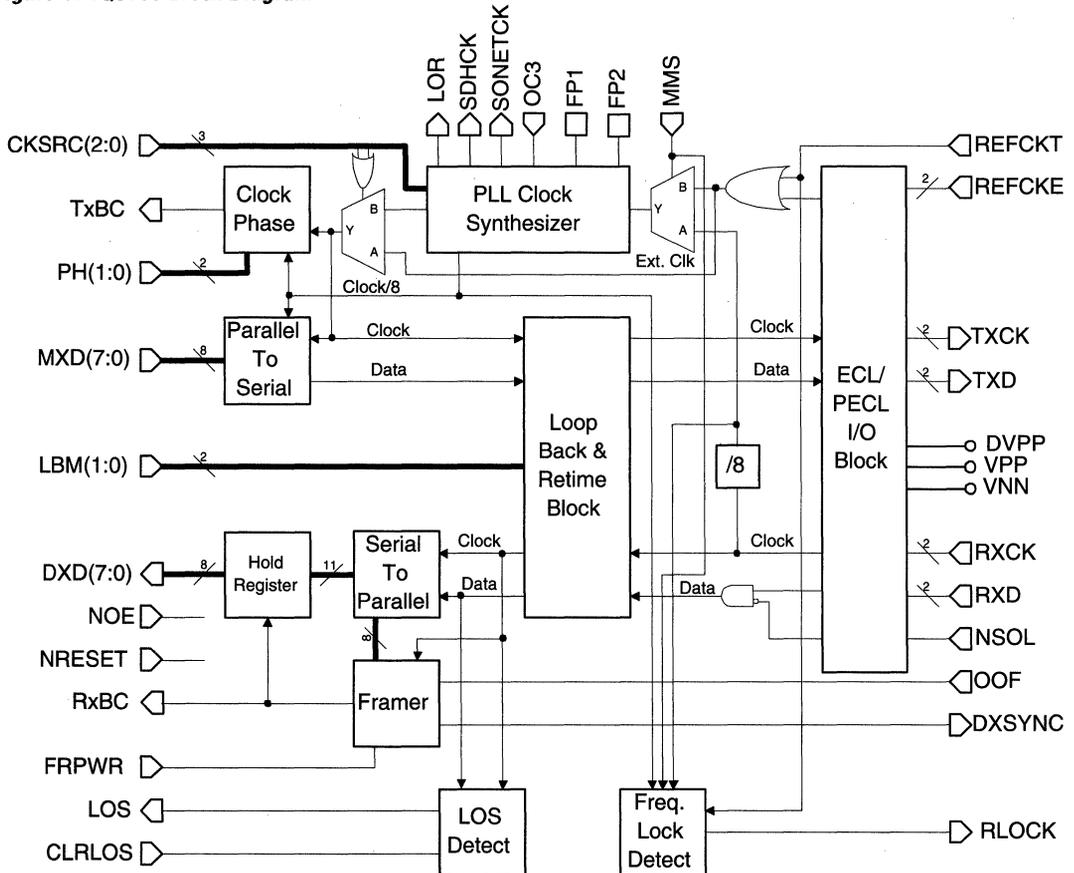
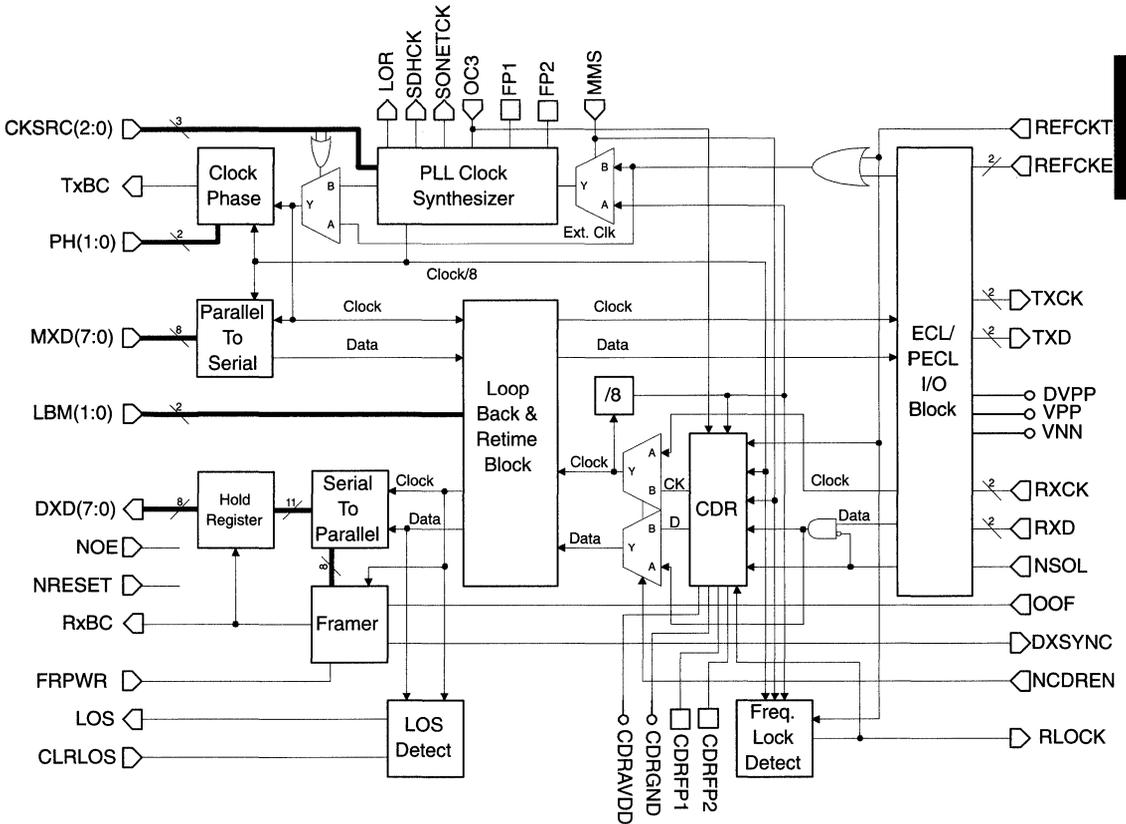


Figure 2. TQ8106 Block Diagram

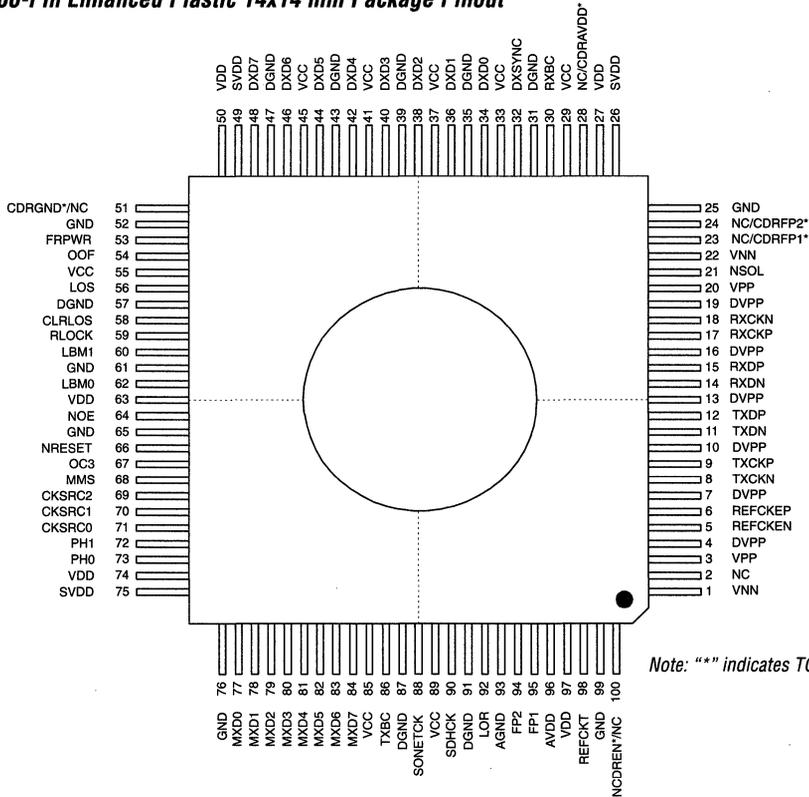


TELECOM
PRODUCTS

TQ8105/TQ8106

PRELIMINARY DATA SHEET

Figure 3. 100-Pin Enhanced Plastic 14x14 mm Package Pinout



Note: "*" indicates TQ8106-specific signal.

Table 1. Signal Descriptions (continues on next page)

Pin	Signal	Function	Description
1	VNN	-5.2V/Ground	ECL/PECL section power
2	NC	No Connect	Do not connect
3	VPP	Ground/+5V	ECL/PECL Positive Supply (see Table 6B)
4	DVPP	Ground/+5V	ECL/PECL Driver Return (see Table 6B)
5	REFCKEN	ECL/PECL Input	Tx Ref. Clock or Bypass Clock, Complement
6	REFCKEP	ECL/PECL Input	Tx Ref. Clock or Bypass Clock, True
7	DVPP	Ground/+5V	ECL/PECL Driver Return (see Table 6B)
8	TXCKN	ECL/PECL Out	Transmit Clock, Complement
9	TXCKP	ECL/PECL Out	Transmit Clock, True
10	DVPP	Ground/+5V	ECL/PECL Driver Return (see Table 6B)
11	TXDN	ECL/PECL Out	Transmit Data, Complement
12	TXDP	ECL/PECL Out	Transmit Data, True
13	DVPP	Ground/+5V	ECL/PECL Driver Return (see Table 6B)
14	RXDN	ECL/PECL Input	Receive Data, Complement
15	RXDP	ECL/PECL Input	Receive Data, True

Note: "*" indicates TQ8106-specific signal.

Table 1. Signal Descriptions (continued)

Pin	Signal	Function	Description
16	DVPP	Ground/+5V	ECL/PECL Driver Return (see Table 6B)
17	RXCKP	ECL/PECL Input	Receive Clock, True (Ignored when CDR used)
18	RXCKN	ECL/PECL Input	Receive Clock, Complement (Ignored when CDR used)
19	DVPP	Ground/+5V	ECL/PECL Driver Return (see Table 6B)
20	VPP	Ground/+5V	ECL/PECL Positive Supply (see Table 6B)
21	NSOL	ECL/PECL Input	Loss of Signal — zeroes serial data in when low; RXBC=TXCK/8
22	VNN	-5.2V/Ground	ECL/PECL section power (see Table 6B)
23	NC/CDRFP1*	Analog Output	CDR Loop Filter Pin 1 — Charge Pump Out (ignored by TQ8105)
24	NC/CDRFP2*	Analog Input	CDR Loop Filter Pin 2 — VCO Tune (ignored by TQ8105)
25	GND	GND	Core Ground
26	SVDD	+5V	Output Driver Internal Positive Supply
27	VDD	+5V	Core Positive Supply
28	CDRAVDD*	Analog +5V	TQ8106 CDR Analog +5V Supply (not connected if CDR not used; ignored by TQ8105)
29	VCC	+5V/+3.3V	TTL Driver Positive Supply
30	RxBC	Tristate TTL Out	Demultiplexer Byte Clock
31	DGND	GND	TTL Driver Ground
32	DXSYNC	Tristate TTL Out	Frame Synchronization Signal
33	VCC	+5V/+3.3V	TTL Driver Positive Supply
34	DXD0	Tristate TTL Out	Demultiplexer Data Bit 0 (LSB)
35	DGND	GND	TTL Driver Ground
36	DXD1	Tristate TTL Out	Demultiplexer Data Bit 1
37	VCC	+5V/+3.3V	TTL Driver Positive Supply
38	DXD2	Tristate TTL Out	Demultiplexer Data Bit 2
39	DGND	GND	TTL Driver Ground
40	DXD3	Tristate TTL Out	Demultiplexer Data Bit 3
41	VCC	+5V/+3.3V	TTL Driver Positive Supply
42	DXD4	Tristate TTL Out	Demultiplexer Data Bit 4
43	DGND	GND	TTL Driver Ground
44	DXD5	Tristate TTL Out	Demultiplexer Data Bit 5
45	VCC	+5V/+3.3V	TTL Driver Positive Supply
46	DXD6	Tristate TTL Out	Demultiplexer Data Bit 6
47	DGND	GND	TTL Driver Ground
48	DXD7	Tristate TTL Out	Demultiplexer Data Bit 7 (MSB)
49	SVDD	+5V	Output Driver Internal Positive Supply
50	VDD	+5V	Core Positive Supply
51	NC/CDRGND*	GND	GND for TQ8106 to powerup CDR (ignored by TQ8105)
52	GND	GND	Core Ground
53	FRPWR	TTL Input	Framer Power Control (power on when high)
54	OOF	TTL Input	Out-of-Frame: Initiates Frame Search/Bit Alignment
55	VCC	+5V/+3.3V	TTL Driver Positive Supply
56	LOS	Tristate TTL Output	Loss of Signal (high when > 128 bit periods without transitions)
57	DGND	GND	TTL Driver Ground

Note: "*" indicates TQ8106-specific signal.

TQ8105/TQ8106**PRELIMINARY DATA SHEET****Table 1. Signal Descriptions (continued)**

Pin	Signal	Function	Description
58	CLRLOS	TTL Input	Active-high Clear LOS output
59	RLOCK	Tristate TTL Output	Receive Clock meets lock criteria when high
60	LBM1	TTL Input	Loopback Mode Control (see Table 6B)
61	GND	GND	Core Ground
62	LBM0	TTL Input	Loopback Mode Control (see Table 6B)
63	VDD	+5V	Core Positive Supply
64	NOE	TTL Input	TTL tristate control (active low to enable)
65	GND	GND	Core Ground
66	NRESET	TTL Input	Global Reset (active low)
67	OC3	TTL Input	OC3/OC12 Mode Select
68	MMS	TTL Input	Master/Slave Mode Control
69	CKSRC2	TTL Input	Clock Source Select (see Table 6B)
70	CKSRC1	TTL Input	Clock Source Select (see Table 6B)
71	CKSRC0	TTL Input	Clock Source Select (see Table 6B)
72	PH1	TTL Input	TxBC Phase Select (see Table 6B)
73	PH0	TTL Input	TxBC Phase Select (see Table 6B)
74	VDD	+5V	Core Positive Supply
75	SVDD	+5V	Output Driver Internal Positive Supply
76	GND	GND	Core Ground
77	MXD0	TTL Input	Multiplexer Data Bit 0 (LSB)
78	MXD1	TTL Input	Multiplexer Data Bit 1
79	MXD2	TTL Input	Multiplexer Data Bit 2
80	MXD3	TTL Input	Multiplexer Data Bit 3
81	MXD4	TTL Input	Multiplexer Data Bit 4
82	MXD5	TTL Input	Multiplexer Data Bit 5
83	MXD6	TTL Input	Multiplexer Data Bit 6
84	MXD7	TTL Input	Multiplexer Data Bit 7 (MSB)
85	VCC	+5V/+3.3V	TTL Driver Positive Supply
86	TxBC	Tristate TTL Out	Transmit Byte Clock
87	DGND	GND	TTL Driver Ground
88	SONETCK	Tristate TTL Out	51.84 MHz Clock Output
89	VCC	+5V/+3.3V	TTL Driver Positive Supply
90	SDHCK	Tristate TTL Out	38.88 MHz Clock Output
91	DGND	GND	TTL Driver Ground
92	LOR	Tristate TTL Out	Indicates Reference Clock is Absent
93	AGND	Analog Ground	VCO Analog Ground
94	FP2	Analog Output	Transmit PLL Loop Filter, Charge Pump Out
95	FP1	Analog Input	Transmit PLL Loop Filter, VCO Tune
96	AVDD	Analog +5V	VCO & Filter Analog VDD Supply
97	VDD	+5V	Core Positive Supply
98	REFCKT	TTL Input	Tx Reference Clock or Bypass Clock
99	GND	GND	Core Ground
100	NC/NCDREN*	TTL Input	Internal Pull-up, Low = CDR receiver clock; Float = Pin 17/18 Rx Clk (ignored by TQ8105)

Note: "*" indicates TQ8106-specific signal.

Function Description

PLL

The TQ8105 & TQ8106 incorporate high-stability, low-jitter Phase Locked Loops (PLLs) running at 2488.32 MHz for the transmit side and, in the TQ8106, running at 1244.16 MHz for the clock recovery section. The PLLs use external surface mounted loop filters consisting of an RC network as shown in the diagrams that accompany the values shown in Table 2. Good analog design principles should be applied to the loop filter portions of the circuit to ensure the best jitter generation performance. To reduce cross-coupling of clocks, both CDR clocks and analog pins should be isolated from the transmit PLL clock and analog pins. An analog ground plane under the two capacitors and the resistor, along with guards around the filter pins is excellent practice, as is a well filtered analog supply (AVDD) and a clean analog ground (AGND). The loop filter values specified in this preliminary data sheet may change.

Reference clock sourcing can be through a variety of mechanisms. As shown in Table 3, the MMS pin determines whether the device operates in Master mode (where the PLL reference comes in on either a TTL or PECL/ECL pin), or a Slave mode (where the PLL reference is derived from the DEMUX high-speed line clock input). If the external reference clock pins are used, note that they are logical ORs and that the unused pin should be tied to (a) GND for unused REFCKT or (b) REFCKEN should be tied to VPP for TTL reference operation. The reference clock frequency can be selected from any number of values, as indicated in Table 3. Note that the PLL may be bypassed, allowing use of an external clock reference. See the note regarding high-speed I/O for PECL/ECL level selection.

Internal dividers determine the operating line rate, as shown in Table 3. The device is capable of operating at STM1/STS-3 or STM4/STS-12 rates. The transmit PLL provides the high performance and compliance with ITU/Bellcore requirements found in the first-generation TQ8101. Optionally, the TQ8106 receiver's CDR can be

disabled for backwards pin-compatibility with the TQ8105. For circuits not requiring the TQ8106's CDR, the CDR is disabled by floating NCDREN (pin 100). Further, the CDR section of the TQ8106 can be powered down by not connecting the CDRGND and CDRAVDD pins, reducing power consumption. If the TQ8106 CDR is not used, the CDR filter pins may be left unconnected.

The transmit PLL also provides constant-rate 38.88 MHz and 51.84 MHz TTL outputs which may be tristated. The 51.84 MHz output may also be derived from the high-speed receiver clock in Clock Source Mode 011 (see Table 3).

Framer

The TQ8105 and TQ8106 provide a clean interface to devices from PMC-Sierra and others. The Out Of Frame (OOF) input is a state (level) initiated event, rather than the edge-triggered event found on TriQuint's first-generation TQ8101 transceiver. When OOF is high, the TQ8105/TQ8106 initiates a frame search for a serial bit pattern that matches twelve A1s (three A1s in OC3 mode) followed by three A2s. If a match occurs, the device realigns byte boundaries and issues a logic high on the DXSYNC pin during the third A2. In the absence of OOF, the device will not realign byte boundaries, but will report any bit-level matching of twelve A1s (three A1s in OC3 mode) followed by three A2s as a DXSYNC pulse.

Framer circuit power may be switched off by a TTL low on the FRPWR pin, saving approximately 0.25W. No further DXSYNC pulses will be issued, though bit alignment is preserved in the demux. Note that the OOF and FRPWR pins may be tied together, powering the framer only when a bit realignment is required (this is not recommended practice, however, due to the inrush currents that may result).

Loopbacks

As part of the TQ8105 and TQ8106 on-chip diagnostics, four loopback modes are supported. These are selected by the dedicated pins LBM0 and LBM1, as shown in Table 3. The loopback modes are shown in Figure 5.

Functional Description (continued)

Enhanced Diagnostics

The TQ8105 and TQ8106 incorporate on-chip clock diagnostics, allowing fast, efficient fault detection and isolation at the systems level.

The LOR (Loss Of Reference) output goes high when the reference clock is absent. Note that this signal is not latched and is only high during the period which the reference clock is missing. A reference clock is required for the TQ8106 CDR to function correctly.

The NSOL (Loss of signal input, active low, PECL level) input allows the receiver to force zeroes onto the demux outputs. A TTL level signal may also be used for NSOL if the resistor network, shown in the applications section of this data sheet, is used. NSOL is useful when a Loss Of Signal occurs on the receive optics and a quieting of invalid data is desired. The receiver is clocked from the transmit clock when NSOL is active and the output RXBC clock is obtained from the transmit portion of the TQ8105/TQ8106. This ensures compatibility with devices, such as the PMC-Sierra S/UNI-622 and STTX components, which may contain dynamic registers that lose contents if clocks are removed. NSOL forces the CDR to lock to REFCLK, except when in slave mode.

The LOS (Loss Of Signal) output goes high whenever 128-bit periods occur without transitions on the data input to the demux. CLRLOS forces LOS low.

The RLOCK (Receiver LOCK) output goes low whenever the signal on RXCK or recovered clock drifts more than 500 ppm from the reference frequency. This output returns high whenever the frequency accuracy is within 100 ppm.

Demux

The TQ8105/TQ8106 demultiplexer converts an NRZ PECL/ECL data input, at either 155 Mb/s or 622 Mb/s, and its corresponding PECL/ECL clock into a byte-

parallel 78 MHz or 19 MHz tristatable TTL data bus. The timing is shown in Figures 6 through 8. See the previous "Framer" description for bit alignment details. The TQ8106 can recover both clock and data from an NRZ data stream, whereas the TQ8105 requires NRZ data and a recovered clock.

Mux

The TQ8105/TQ8106 multiplexer converts a 78 MHz or 19 MHz byte-wide bus to a serial NRZ PECL/ECL data stream. The bytes are clocked into the device with the TXBC byte clock output. The timing is shown in Figures 6 through 8. Note that the TXBC output can be adjusted in 90-degree phase increments to accommodate variations in interface requirements. See Table 3 for settings on the PH0 and PH1 pins controlling this function. Data may also be clocked into the TQ8105/TQ8106 by a 77 MHz reference oscillator clock source, provided the data is within the timing limits shown in the timing diagram labelled "Reference Clock Based Transmit Timing." The TQ8105 and TQ8106 do not require the transmit latch found on earlier TQ8101 reference designs and are backwards compatible with designs that have the latch incorporated.

High-Speed I/O and TTL Interfaces

The TQ8105 and TQ8106 contain unique circuitry that allows either PECL or ECL operation on its high-speed I/O. As a single +5V supply component, the TQ8105 interfaces directly to TTL and PECL (Positive Emitter Coupled Logic). By providing an additional -5.2V supply, the device's high-speed I/O becomes ECL, instead of PECL. The supply connections for PECL/ECL are shown in Table 6B.

The TTL outputs (Vcc) may be connected to either +5V or +3.3V supplies. True TTL may be obtained with the +5V connection; clamped operation, when connected to +3.3V ensures that maximum Voh levels do not exceed +3.3V.

TQ8105/TQ8106 Design Notes

These design notes are provided to assist the circuit designer in achieving the highest possible performance and reducing design time. Unless noted otherwise, references to the TQ8105 apply equally to the TQ8106.

Interfacing to PMC-Sierra Devices

The transmit timing of the TQ8105 is such that the PMC-Sierra byte outputs (POUT(0:7)) may be directly connected to the TQ8105 mux inputs (MXD(0:7)). The TQ8105 uses an Out-Of-Frame (OOF) input as a signal to reframe while high, allowing direct connection of the PM5355's OOF output to the TQ8105 OOF input. The following summarizes connectivity between the devices.

PM5355	TQ8105/TQ8106
POUT(0:7)	MXD(0:7)
PIN(0:7)	DXD(0:7)
OOF	OOF
PICLK	RXBC
FPIN	DXSYNC
TCLK	TXBC
POP(0:5)	Any TQ8105 modes to be programmable
PIP(0:3)	Any TQ8105 diag outputs to be readable

Reference Design

A reference design (see Figure 4) and evaluation board are available from TriQuint. They incorporate a 1x9 or 2x9 fiber optic transceiver with or without clock recovery, the PM5355 PMC Sierra framer device, and a TQ8105 or TQ8106.

Thermal Considerations

At 2.3 W, the TQ8105 requires a heat sink if operated in a still-air environment at either 70 °C or 85 °C ambient air temperature. At 100 lfm, only the 85 °C air temperature condition requires a heat sink. At 200 lfm and above, no heat sink is required. For example, a 1.1" x 1.1" x 0.6" standard pin-fin heat sink is appropriate for applications where a heat sink is necessary. To attach the sink, use

clips soldered to the board which accept a spring clip to cross and hold the heat sink. The holes in the board for the clips are at the corners of a 1.275" x 1.5" rectangle.

Power Supplies

Good decoupling practices should be observed, with a 0.1 uF decoupling capacitor at each supply pin, ideally on the component side of the board. Keep the analog supplies (Vdd and AVdd) pristine. Good design practice will isolate the supply groups using point grounding to tie supplies together (*all* grounds at a single point having multiple vias).

For the analog supply, flood copper under the loop filter on the component side of the board, tying the flood to the analog ground pin, with the point ground away from the filter and analog pin, so that any switching currents are kept away from these areas. If any switching power supply frequencies below 500 kHz are used in the system, use a supply filter on the analog supply pin. These practices help minimize the generation of jitter.

High-Speed Connections

Connections to E/O modules (and ECL clock reference, if used) are direct-coupled PECL and need to be terminated with decoupled 50 ohms to 3V at the receiving end of the 50 ohm transmission line. Ensure that each 50 ohm resistor (or Thevenin equivalent) has its own decoupling capacitor. Place the resistor at the end of a 50 ohm transmission line (use a controlled impedance layer), ideally with a minimal-length stub to either the resistor or the receiving device.

If there is no room for the resistor, use a minimal-length stub to drop the signal at the receiving device pins, continue the 50 ohm transmission line to an area where the termination resistors can be placed, and terminate at the endpoint of that line. If in doubt, contact factory applications for assistance.

Table 2A. TQ8105/TQ8106 Recommended Transmit Loop Filter Values
(Preliminary)

Reference Frequency (MHz)	Divide Ratio	Resistor Value R1 (ohms)	Capacitor Value C1 (μF)	Capacitor Value C2 (pF)
19.44	32	1200	0.082	82
38.88	16	620	0.15	150
51.84	12	470	0.22	220
77.76	8	300	0.33	330
155.52*	4	300	0.33	330

Note: *Internal divide by two on Reference

Table 2B. TQ8106 Recommended CDR Loop Filter Values
(Preliminary)

Incoming NRZ Data Rate (Mbs)	Resistor Value R2 (ohms)	Capacitor Value C3 (μF)	Capacitor Value C4 (μF)
155.52	22	68	0.015
622.08	91	4.7	0.001

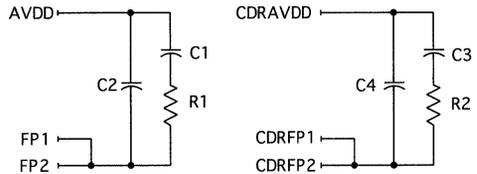
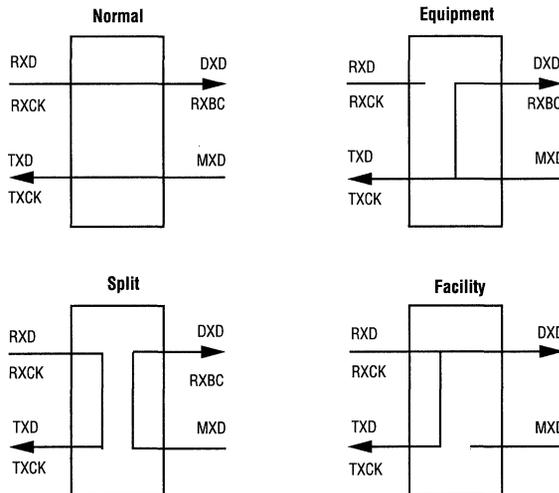


Figure 5. Loopback Modes



TQ8105/TQ8106

PRELIMINARY DATA SHEET

Table 3. Mode Selection

Signals	Mode
LBM(1:0)	Loopback: 00 = Normal, 01 = Equipment, 10 = Facility, 11 = Split
PH(1:0)	00 = 0 degrees delay, 01 = 90 degrees delay, 10 = 180 degrees delay, 11 = 270 degrees delay
MMS	1 = Master (use REFCKT/E as reference), 0 = Slave (use receive clock as reference)
CKSRC(2:0)	Clock Source: 000 = PLL bypass 001 = 51.84 MHz PLL reference, SONETCK & SDHCK tristate 010 = 155.52 MHz PLL reference 011 = 51.84 MHz PLL reference, SONETCK=RXCK/12, SDHCK=RXCK/16 100 = 77.76 MHz PLL reference 101 = 51.84 MHz PLL reference 110 = 38.88 MHz PLL reference 111 = 19.44 MHz PLL reference
OOF	1 = Initiate frame search, 0 = Do not permit reframing (see FRPWR pin in Table 1)
NSOL	1 = Pass receive data, 0 = Force receive data to 0
OC3	1 = Operate at STM1/STS-3 (or PLL bypass divided by 4), 0 = Operate at STM4/STS-12/PLL bypass
NRESET	1 = Normal operation, 0 = Reset internal counters
NCDREN	1 = TQ8105/CDR Off mode, 0 = Enable CDR (TQ8106 only)

Table 4. Absolute Maximum Ratings

Parameter	Symbol	Level	Minimum	Maximum	Unit
Positive supply	$V_{CC}, V_{PP}, V_{DD}, AV_{DD}$	GND	7	V	
Negative supply ($V_{PP} = 0$ V)	V_{NN}		-7	GND	V
Output voltage	V_O	ECL/PECL	$V_{NN}-0.5$	$V_{PP}+0.5$	V
Output current	I_O	ECL/PECL	—	40	mA
Input voltage	V_I	ECL/PECL	$V_{NN}-0.5$	$V_{PP}+0.5$	V
Input current	I_I	ECL/PECL	-1	1	mA
Output voltage	V_O	TTL	-0.5	$V_{CC}+0.5$	V
Output current	I_O	TTL	—	100	mA
Input voltage	V_I	TTL	-0.5	$V_{CC}+0.5$	V
Input current	I_I	TTL	-1	1	mA
Biased Junction temperature	T_J	—	-55	+150	°C
Storage temperature	T_S	—	-65	+150	°C

Table 5. Power Consumption

Symbol	Function	Minimum	Typical	Maximum	Unit
I_{DD}	+5 V supply	—	TBD	TBD	I
I_{CC}	+5V / +3 V supply	—	TBD	TBD	I
I_{PP}	+5 V / 0 V supply	—	TBD	TBD	I
I_{CC}	0 V / -5 V supply	—	TBD	TBD	I
P_{DF}	Power dissipation, Framer on, TQ8106 CDR off	—	1.9	2.3	W
P_D	Power dissipation, Framer off, TQ8106 CDR off	—	1.7	2.1	W
P	Power dissipation, Framer on, TQ8106 CDR on			2.75	W

Table 6A. Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Positive supply	V_{PP}	4.75	5.0	5.25	V
Output Driver Positive Supply	V_{CC}	3.0		5.25	V
Negative supply (ECL mode only)	V_{NN}	-5.5	-5.2	-4.75	V
Operating case temperature (see Figure 9)		-40		125	°C

Table 6B. Power Supply Connections

Pin	+5V TTL/PECL IO	+3.3V TTL/PECL IO	+5V TTL/ECL IO	+3.3V TTL/ECL IO
VDD	+5V	+5V	+5V	+5V
SVDD	+5V	+5V	+5V	+5V
VCC	+5V	+3.3V	+5V	+3.3V
AVDD	Filtered +5V	Filtered +5V	Filtered +5V	Filtered +5V
CDRAVDD	Filtered +5V	Filtered +5V	Filtered +5V	Filtered +5V
GND	0V (ground)	0V (ground)	0V (ground)	0V (ground)
AGND	0V (ground)	0V (ground)	0V (ground)	0V (ground)
CDRGND	0V (ground)	0V (ground)	0V (ground)	0V (ground)
VPP	+5V	+5V	0V (ground)	0V (ground)
VNN	0V (ground)	0V (ground)	-5.2V	-5.2V

TQ8105/TQ8106

PRELIMINARY DATA SHEET

Table 7. DC Characteristics—ECL/PECL I/O

(Specifications apply over recommended operating ranges).

Parameter	Condition	Symbol	Minimum	Nominal	Maximum	Unit
Internal ECL reference	Single-ended inputs	V_{REF}	—	$0.26 V_{NN} + 0.74 V_{PP}$		mV
Common mode voltage	Differential inputs	V_{COM}	$V_{PP} - 1500$	—	$V_{PP} - 1100$	mV
Differential voltage	Differential inputs	V_{DIFF}	200	—	1200	mV
Input HIGH voltage	$V_{REF} = 1300$ mV	V_{IH}	$V_{PP} - 1050$	—	$V_{PP} - 400$	mV
Input LOW voltage		V_{IL}	V_{TT}	—	$V_{PP} - 1550$	mV
Output HIGH voltage	$R_{LOAD} = 50$ ohms to $V_{TT} = V_{PP} - 2.0V$	V_{OH}	$V_{PP} - 1000$		$V_{PP} - 600$	mV
Output LOW voltage	$R_{LOAD} = 50$ ohms to $V_{TT} = V_{PP} - 2.0V$	V_{OL}	V_{TT}	—	$V_{PP} - 1600$	mV
Input HIGH current	$V_{IH(MAX)}$	I_{IH}	—	+130	335	uA
Input LOW current	$V_{IL(MIN)}$	I_{IL}	-265	-130	—	uA
Output HIGH current	(Not tested; consistent with V_{OH} and V_{OL} tests)	I_{OH}	20	23	30	mA
Output LOW current	(Not tested; consistent with V_{OH} and V_{OL} tests)	I_{OL}	0	5	8	mA
Input capacitance		C_{IN}	—	—	TBD	pF
Output capacitance		C_{OUT}	—	—	TBD	pF
ESD breakdown rating	(Design objective)	V_{ESD}	Class I	—	—	

Table 8. DC Characteristics—TTL I/O

(Specifications apply over recommended operating ranges)

Parameter	Condition	Symbol	Minimum	Nominal	Maximum	Unit
Input HIGH voltage		V_{IH}	2.0	—	V_{CC}	V
Input LOW voltage		V_{IL}	0	—	0.8	V
Input HIGH current	$V_{IH(MAX)}$	I_{IH}	—	—	200	uA
Input LOW current	$V_{IL(MIN)}$	I_{IL}	-400	-200	—	uA
Output HIGH voltage	$I_{OH} = 50$ mA	V_{OH}	2.4	—	V_{CC}	V
Output LOW voltage	$I_{OL} = -20$ mA	V_{OL}	0	—	0.4	V
Tristate current		I_{OZ}	-100	—	100	uA
Input capacitance		C_{IN}	—	—	TBD	pF
Output capacitance		C_{OUT}	—	—	TBD	pF
ESD breakdown rating	(Design objective)	V_{ESD}	Class I	—	—	

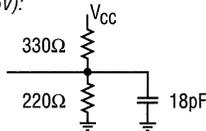
Table 9. AC Characteristics

(Specifications apply over recommended operating ranges)

Parameter	Symbol	Minimum	Nominal	Maximum	Unit
RXCK clock period	$T_{C(RXCK)}$	1.6	—	—	ns
REFCKE clock period	$T_{C(REFCKE)}$	1.6	—	—	ns
TXCK clock period	$T_{C(TXCK)}$	1.6	—	—	ns
REFCKT clock period	$T_{C(REFCKT)}$	12.8	—	—	ns
TXBC clock period	$T_{C(TXBC)}$	12.8	—	—	ns
RXBC clock period	$T_{C(RXBC)}$	12.8	—	—	ns
REFCKT/REFCKE clock duty cycle	$T_{C(REF)}$	40	—	60	%
REFCKT to TXBC skew ^{2,3,5}	$T_{SK(TXBC)}$	TBD	—	TBD	
SONETCK clock period	$T_{C(SONETCK)}$	—	19.29	—	ns
RXBC clock duty cycle ^{3,5}	$T_{DC(RXBC)}$	40	50	60	%
TXBC clock duty cycle ^{3,5}	$T_{DC(TXBC)}$	40	50	60	%
TXCK clock duty cycle ⁶	$T_{DC(TXCK)}$	40	50	60	%
SONETCK clock duty cycle ^{3,5}	$T_{DC(SONETCK)}$	40	50	60	%
SDHCK clock duty cycle ^{3,5}	$T_{DC(SDHCK)}$	40	50	60	%
RXCK clock duty cycle ⁶	$T_{DC(RXCK)}$	40	50	60	%
High-speed rise/fall time ⁴ (> 79 MHz), Data	$T_{H(R/F)}$	—	—	500	ps
High-speed rise/fall time ⁴ (>79 MHz), Clock	$T_{H(R/F)}$	—	—	320	ps
Low-speed rise/fall time ^{1,3,5} (< 79 MHz)	$T_{L(R/F)}$	—	—	3	ns
RXD setup time to RXCK ⁶ (see Figure 6)	$T_{S(RXD)}$	240	—	—	ps
RXD hold time to RXCK ⁶ (see Figure 6)	$T_{H(RXD)}$	20	—	—	ps
OOF rising edge before A1 changes to A2 ⁷ (see Figure 8)	$T_{(OOFH)}$	51.44	—	—	ns
DXSYNC rising edge from parallel data output change from A1 to A2 ⁷	$T_{(DSYNC)}$	—	25.72	—	ns
DXSYNC pulse width ^{3,5,7} (see Figure 8)	$T_{(DXSYNCPW)}$	11.0	—	—	ns
RXBC falling edge to valid parallel data output ³ (see Figure 7)	$T_{P(DXD)}$	0.5	—	1.0	ns
MXD(0:7) setup time to TXBC ^{2,3,5} (see Figure 6)	$T_{S(MXD)}$	600	—	—	ps
MXD(0:7) hold time to TXBC ^{2,3,5} (see Figure 6)	$T_{H(MXD)}$	600	—	—	ps
TXCK falling edge to TXD ⁶ (see Figure 7)	$T_{P(TXD)}$	200	—	400	ps

Notes: 1. At 0.8V/2.0V levels

2. With PH(1:0) set to 00, 18pF total loading

3. TTL outputs test load ($V_{CC} = +5V$):

4. 20% / 80% levels

5. At 1.4V logic threshold level

6. Differential measurement

7. OC12 mode

TQ8105/TQ8106

PRELIMINARY DATA SHEET

Figure 6. Input Timing

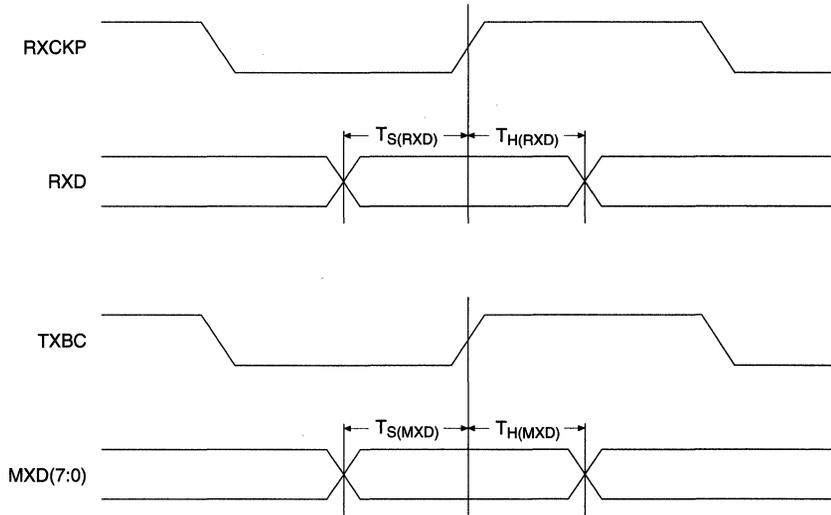


Figure 7. Output Timing

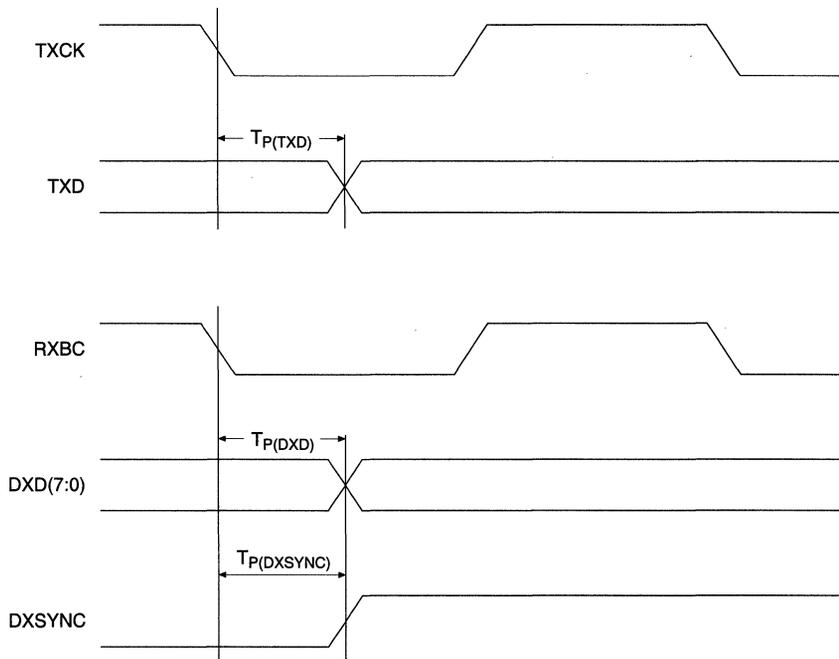
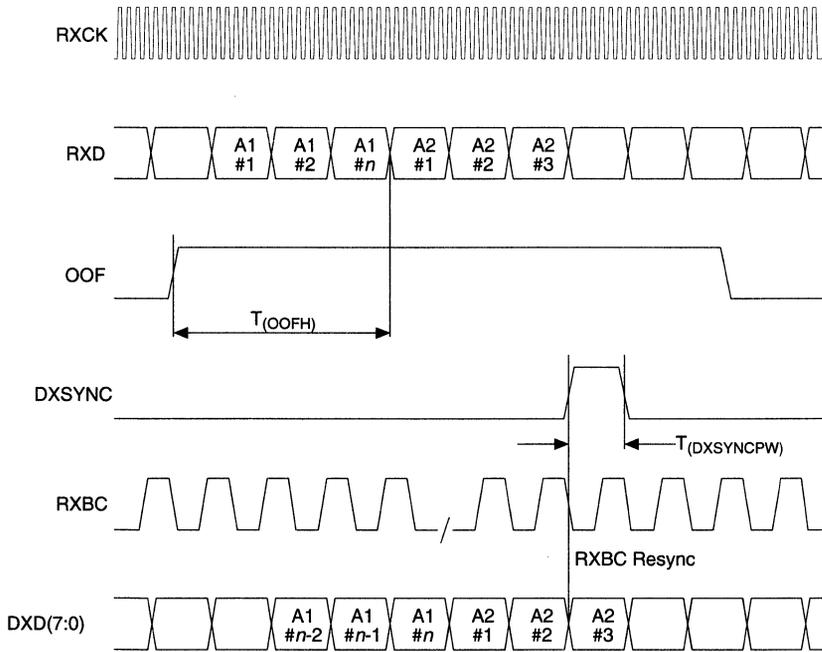
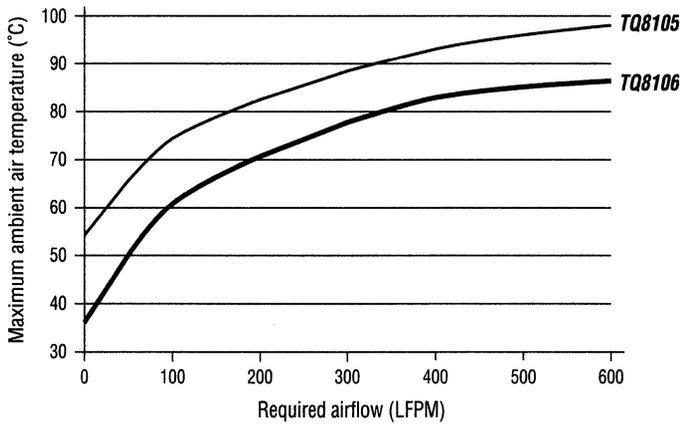


Figure 8. Demultiplexer Timing



TELECOM
PRODUCTS

Figure 9. Required Airflow for Operation without Heatsink

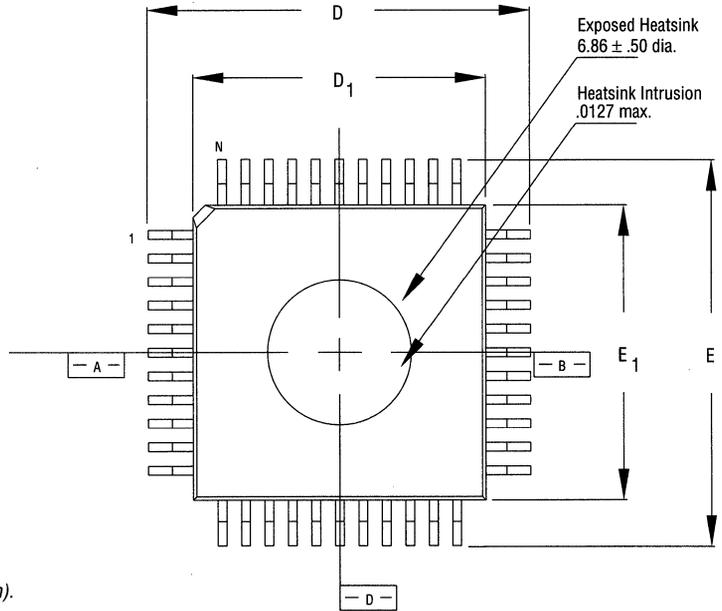


TQ8105/TQ8106

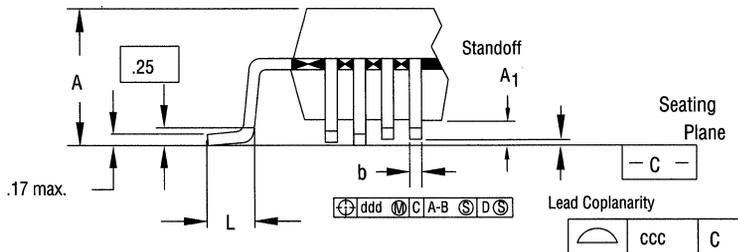
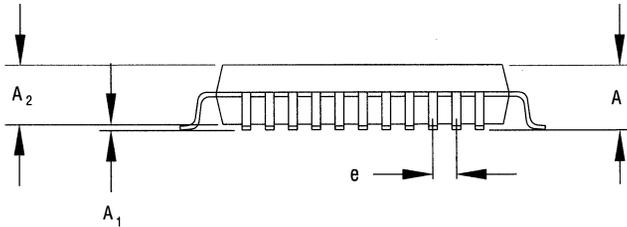
PRELIMINARY DATA SHEET

Figure 10. Mechanical Package (100 pins, 14x14 mm)

Dim.	Value
A	2.35
A ₁	0.25 max
A ₂	2.00
D	17.20
D ₁	14.00
E	17.20
E ₁	14.00
L	0.80
b	0.22
ccc	0.08
ddd	0.08 max
e	0.50
N	100 pins



Note: All dimensions in millimeters (mm).



Ordering Information

TQ8105	<i>SONET/SDH Transceiver</i>
TQ8106	<i>SONET/SDH Transceiver with Clock and Data Recovery</i>
ETF8105	<i>SONET/SDH Transceiver Evaluation Board</i>

Reference Designs

The following products are available for 14-day loan to qualified customers:

ATM SONET/SDH Line Interface Module

Supports OC12c/STM-4 (622.08 Mbps) and OC-3c/STM-1 (155.52 Mbps)

RDB810x-yz *Reference Design Circuit Board*

x = 5 for 8105 or **6** for 8106

y = S for Single-mode, **M** for multi-mode, or **X** for no optical module

z = 3 for OC3 or **12** for OC12

Example: *RDB8105-S12* is a TQ8105 configured for single-mode OC12

RDD-8105/6 *Documentation Package*

- Functional Partition Drawing Set, including block, state machine, and timing diagrams
- Schematics
- Programmable Logic Listings
- User's Manual / Product Specification
- PCB Artwork (all layers)
- Component Placement Drawing

Additional Information

For latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com **Tel:** (503) 615-9000

Email: sales@tqs.com **Fax:** (503) 615-8900

For technical questions and additional information on specific applications:

Email: applications@tqs.com

A Principal Member of



The ATM Forum

The information provided herein is believed to be reliable; TriQuint assumes no liability for inaccuracies or omissions. TriQuint assumes no responsibility for the use of this information, and all such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. TriQuint does not authorize or warrant any TriQuint product for use in life-support devices and/or systems.

Copyright © 1997 TriQuint Semiconductor, Inc. All rights reserved.

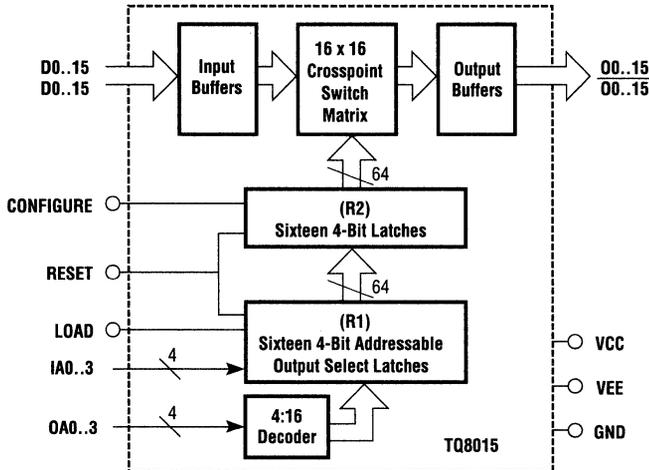
Revision 0.0.A October 1997

TQ8105/TQ8106

PRELIMINARY DATA SHEET

Section 3 — Digital Switching Products

<i>TQ8015</i>	<i>1.25 Gb/s 16x16 ECL Crosspoint Switch</i>	<i>3-3</i>
<i>TQ8016</i>	<i>1.3 Gb/s 16x16 ECL Crosspoint Switch</i>	<i>3-11</i>
<i>TQ8017</i>	<i>1.25 Gb/s 16x16 PECL Crosspoint Switch</i>	<i>3-21</i>
<i>TQ8025</i>	<i>2.5 Gb/s 16x16 PECL Crosspoint Switch</i>	<i>3-29</i>
<i>TQ8032</i>	<i>800 Mb/s 32x32 ECL Crosspoint Switch</i>	<i>3-37</i>
<i>TQ8033</i>	<i>1.5 Gb/s 64x33 PECL Crosspoint Switch</i>	<i>3-45</i>



The TQ8015 is a non-blocking 16 x 16 digital crosspoint switch capable of data rates greater than 1.25 Gigabits per second per port. Utilizing a fully differential internal data path and ECL I/O, the TQ8015 offers a high data rate with exceptional signal fidelity. The symmetrical switching and noise rejection characteristics inherent in differential logic result in low jitter and signal skew. The TQ8015 is ideally suited for digital video, data communications and telecommunication switching applications.

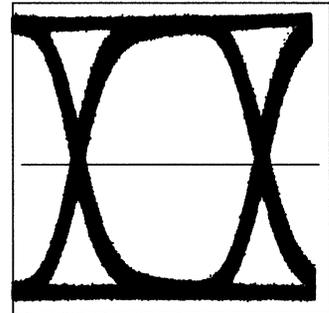
The non-blocking architecture uses 16 fully independent 16:1 multiplexers (see diagram on page 2), allowing each output port to be independently programmed to any input port. The switch is configured by sequentially loading each multiplexer's 4-bit program latch (OA0:3) with the desired input port address (IA0:3) and enabling the LOAD pin. When complete, the CONFIGURE pin is strobed and all new configurations are simultaneously transferred into the switch multiplexers. Data integrity is maintained on all unchanged data paths.

Electrical Characteristics

	Min	Max	Units
Data Rate/Port	1.25		Gb/s
Jitter		150	ps peak-peak
Channel Propagation Delay		2000	ps
Ch-to-Ch Propagation Delay Skew		500	ps

TQ8015

1.25 Gigabit/sec 16x16 Digital ECL Crosspoint Switch



Typical output waveform with all channels driven

Features

- >20 Gb/s aggregate BW
- 1.25 Gb/s/port NRZ data rate
- Non-blocking architecture
- 500 ps delay match
- Differential ECL-level data I/O; CMOS-level control inputs
- Low jitter and signal skew
- Fully differential data path
- Double buffered configuration latches
- 132-pin MQFP package

Applications

Telecom/Datacom Switching
Hubs and Routers
Video Switching

TQ8015

Figure 1. TQ8015 architecture.

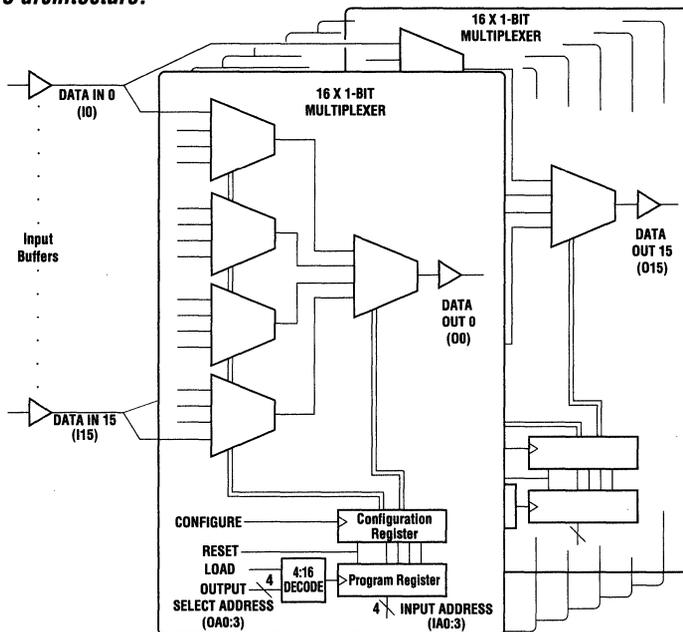


Table 1. Absolute Maximum Ratings⁵

Symbol	Parameter	Absolute Max. Rating	Notes
T _{STOR}	Storage Temperature	-65° C to +150° C	
T _{CH}	Junction (Channel) Temperature	-65° C to +150° C	1
T _C	Case Temperature Under Bias	-65° C to +125° C	2
V _{CC}	Supply Voltage	0 V to +7 V	3
V _{EE}	Supply Voltage	-7 V to 0 V	3
V _{TT}	Load Termination Supply Voltage	V _{EE} to 0 V	4
V _{IN}	Voltage Applied to Any ECL Input; Continuous	V _{EE} -0.5 V to +0.5 V	
I _{IN}	Current Into Any ECL Input; Continuous	-1.0 mA to +1.0 mA	
V _{IN}	Voltage Applied to Any CMOS Input; Continuous	-0.5 V to V _{CC} +0.5 V	
I _{IN}	Current Into Any CMOS Input; Continuous	-1.0 mA to +1.0 mA	
V _{OUT}	Voltage Applied to Any ECL Output	V _{EE} -0.5 V to +0.5 V	4
I _{OUT}	Current From Any ECL Output; Continuous	-40 mA	
P _D	Power Dissipation per Output P _{OUT} = (GND - V _{OUT}) x I _{OUT}	50 mW	

- Notes:
1. For die applications.
 2. T_C is measured at case top.
 3. All voltages specified with respect to GND, defined as 0V.
 4. Subject to I_{OUT} and power dissipation limitations.
 5. Absolute maximum ratings, as detailed in this table, are the ratings beyond which the device's performance may be impaired and/or permanent damage to the device may occur.

Table 2. Recommended Operating Conditions³

Symbol	Parameter	Min	Typ	Max	Units	Notes
T _C	Case Operating Temperature	0		85	°C	1
V _{CC}	Supply Voltage	4.5		5.5	V	
V _{EE}	Supply Voltage	-5.5		-4.5	V	
V _{TT}	Load Termination Supply Voltage		-2.0		V	2
R _{LOAD}	Output Termination Load Resistance		50		Ω	2
Θ _{JC}	Thermal Resistance Junction to Case			7	°C/W	

- Notes: 1. T_C measured at case top. Use of adequate heatsink is required.
 2. The V_{TT} and R_{LOAD} combination is subject to maximum output current and power restrictions.
 3. Functionality and/or adherence to electrical specifications is not implied when the device is subjected to conditions that exceed, singularly or in combination, the operating range specified.

Table 3. Pin Descriptions

Signal	Name/Level	Description																														
I0 to I15, NI0 to NI15	Data input true and complement. Differential ECL	Differential data input ports.																														
O0 to O15, NO0 to NO15	Data output true and complement. Differential ECL	Differential data output ports.																														
IA0:3	Input address, CMOS	Input port selection address that is written into the selected output port program latches (OA0:3). <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>IA3</th> <th>IA2</th> <th>IA1</th> <th>IA0</th> <th>Input port</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>2</td> </tr> <tr> <td>:</td> <td>:</td> <td>:</td> <td>:</td> <td>:</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>15</td> </tr> </tbody> </table>	IA3	IA2	IA1	IA0	Input port	0	0	0	0	0	0	0	0	1	1	0	0	1	0	2	:	:	:	:	:	1	1	1	1	15
IA3	IA2	IA1	IA0	Input port																												
0	0	0	0	0																												
0	0	0	1	1																												
0	0	1	0	2																												
:	:	:	:	:																												
1	1	1	1	15																												
OA0:3	Output select address, CMOS	Output port selection address. Selects the output port program latches to which the input port selection address (IA0:3) is written. <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>OA3</th> <th>OA2</th> <th>OA1</th> <th>OA0</th> <th>Output port</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>2</td> </tr> <tr> <td>:</td> <td>:</td> <td>:</td> <td>:</td> <td>:</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>15</td> </tr> </tbody> </table>	OA3	OA2	OA1	OA0	Output port	0	0	0	0	0	0	0	0	1	1	0	0	1	0	2	:	:	:	:	:	1	1	1	1	15
OA3	OA2	OA1	OA0	Output port																												
0	0	0	0	0																												
0	0	0	1	1																												
0	0	1	0	2																												
:	:	:	:	:																												
1	1	1	1	15																												
LOAD	CMOS	Enables the selected output port program latches while set 'high'. Latches the data when set to a 'low' level.																														
CONFIGURE	CMOS	Transfers the program latches data to the configuration latches and implements the switch changes while set 'high'. Latches the data when set to a 'low' level.																														
RESET	CMOS	Sets the switch into broadcast or pass-through configuration, overwriting existing configurations. Broadcast mode: All output ports are connected to data input port 0. This mode is selected by applying a RESET "high" pulse with CONFIGURE held "low".																														

TQ8015

Table 4. DC Characteristics¹ – Within recommended operating conditions, unless otherwise indicated.

Symbol	Parameter	Min	Max	Units	Test Cond.	Notes
V _{IH}	ECL Input Voltage High	-1100	-500	mV		
V _{IL}	ECL Input Voltage Low	V _{TT}	-1500	mV		
I _{IH}	ECL Input Current High		+30	μA	V _{IH} = -0.7 V	
I _{IL}	ECL Input Current Low	-30		μA	V _{IL} = -2.0 V	
V _{ICM}	ECL Input Common Mode Voltage	-1500	-1100	mV		
V _{IDIF}	ECL Input Differential Voltage (pk-pk)	400	1200	mV		
V _{IH}	CMOS Input Voltage High	3.5	V _{CC}	V		
V _{IL}	CMOS Input Voltage Low	0	1.5	V		
I _{IH}	CMOS Input Current High		+100	μA	V _{IH} = V _{CC}	
I _{IL}	CMOS Input Current Low		-100	μA	V _{IL} = 0 V	
V _{OCM}	ECL Output Common Mode	-1500	-1100	mV		
V _{ODIF}	ECL Output Differential Voltage	600		mV		
V _{OH}	ECL Output Voltage High	-1000	-600	mV		
V _{OL}	ECL Output Voltage Low	V _{TT}	-1600	mV		
I _{OH}	ECL Output Current High	20	27	mA		
I _{OL}	ECL Output Current Low	0	8	mA		
I _{CC}	Power Supply Current (+)		20	mA		
I _{EE}	Power Supply Current (-)		-950	mA		

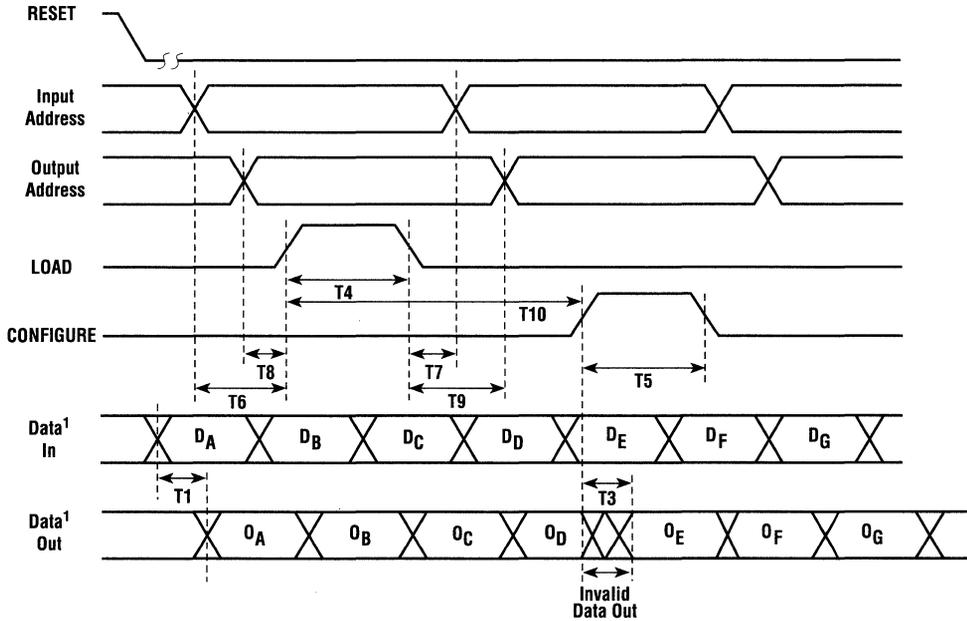
Notes: 1. Test conditions unless otherwise indicated: V_{TT} = -2.0 V, R_{LOAD} = 50 W to V_{TT}.

Table 5. AC Characteristics¹ – Within recommended operating conditions, unless otherwise indicated.

Symbol	Parameter	Min	Typ	Max	Units	Notes
	Maximum Data Rate/Port			1.25	Gb/s	1,2
	Jitter			150	ps pk-pk	1
T ₁	Channel Propagation Delay			2000	ps	
T ₂	Ch-to-Ch Propagation Delay Skew			500	ps	
T ₃	CONFIG to Data Out (Oi) Delay			5	ns	
T ₄	LOAD Pulse Width	7			ns	
T ₅	CONFIG Pulse Width	7			ns	
T ₆	IAi to LOAD High Setup Time	0			ns	
T ₇	LOAD to IAi Low Hold Time	3			ns	
T ₈	OAi to LOAD High Setup Time	0			ns	
T ₉	LOAD to OAi Low Hold Time	3			ns	
T ₁₀	Load ↑ to CONFIG ↑	0			ns	
T ₁₁	RESET Pulse Width	10			ns	
T _{R,F}	Output Rise or Fall Time		250	400	ps	3

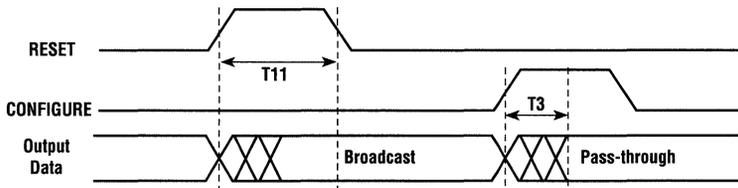
Notes: 1. Test conditions: V_{TT} = -2.0 V, R_{LOAD} = 50 W to V_{TT}; ECL inputs: V_{IH} = -1.1 V; V_{IL} = -1.5 V; CMOS inputs: V_{IH} = 3.5 V, V_{IL} = 1.5 V; ECL outputs: V_{OH} ≥ -1.0 V, V_{OL} ≤ -1.6 V; ECL inputs rise and fall times ≤ 1 ns; CMOS inputs rise and fall times ≤ 20 ns. A bit error rate of 1E-13 BER or better for 2²³-1PRBS pattern, jitter and rise/fall times are guaranteed through characterization.
 2. 1.2 Gb/s Non-Return-Zero (NRZ) data equivalent to 600 MHz clock signal.
 3. Rise and fall times are measured at the 20% and 80% points of the transition from V_{OL} max to V_{OL} min.

Figure 2. Switch Configuration Timing



Notes: 1. No data loss on unchanged paths.

Figure 5. Reset Timing



- Notes: 1. LOAD input must remain LOW to insure correct programming of the switch.
- 2. "Broadcast" is defined as data input 0 to all data outputs (0...15).
- 3. "Pass-through" is defined as data input 0 to data output 0, data input 1 to data output 1, and so on.

Typical Performance Data

Figure 4. Data Eye Closure

Percent RMS vs. Data Rate (typical)

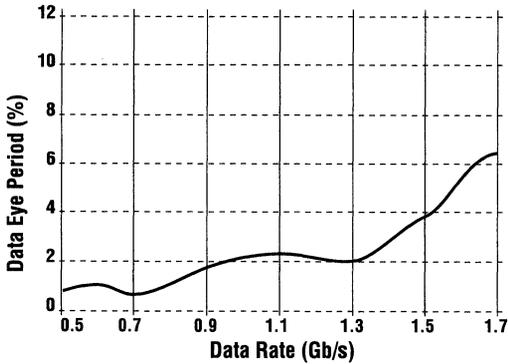


Figure 5. Data Eye Closure

Time & Amplitude vs. Data Rate (typical)

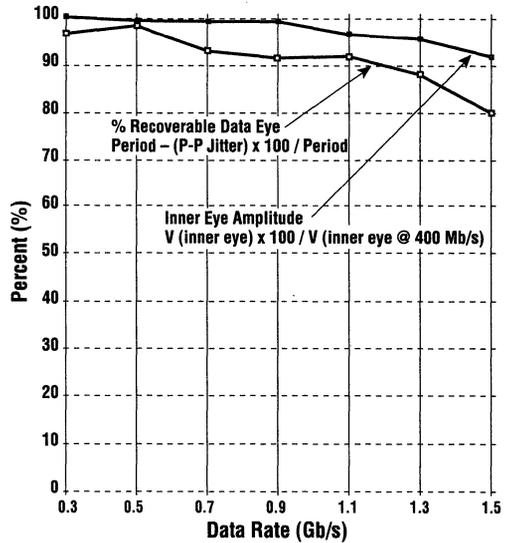
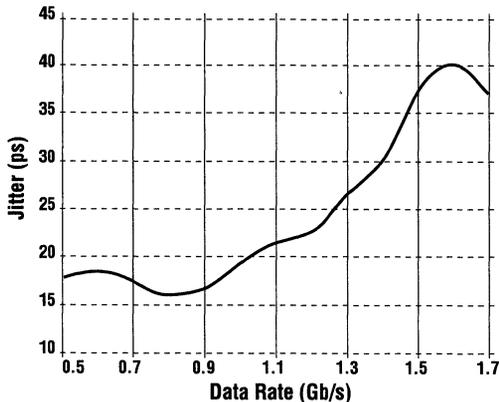


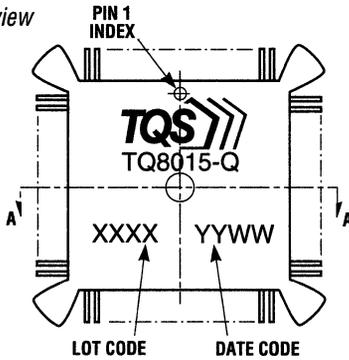
Figure 6. RMS Jitter vs. Data Rate (typical)



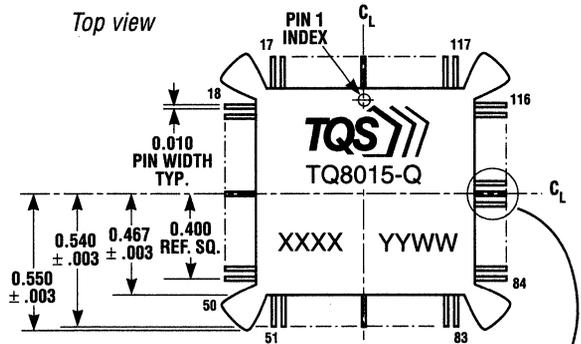
TQ8015

Figure 8. Mechanical Dimensions (in inches)

Bottom view

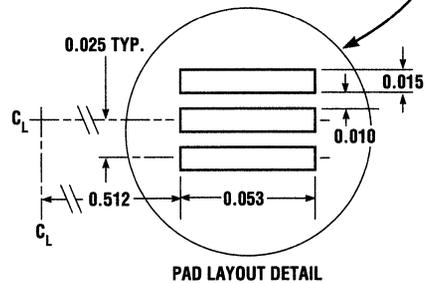
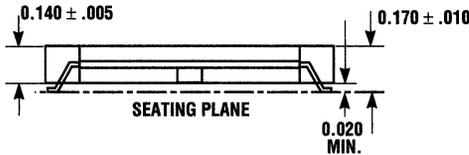


Top view



- Notes: 1. Part is symmetrical about the center axes.
- 2. Centerline bisects center pin in both directions.
- 3. See pad detail below.

Section A-A



Ordering Information

TQ8015-Q

1.25 16x16 Gb/s ECL Crosspoint Switch

Additional Information

For latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com Tel: (503) 615-9000

Email: sales@tqs.com Fax: (503) 615-8900

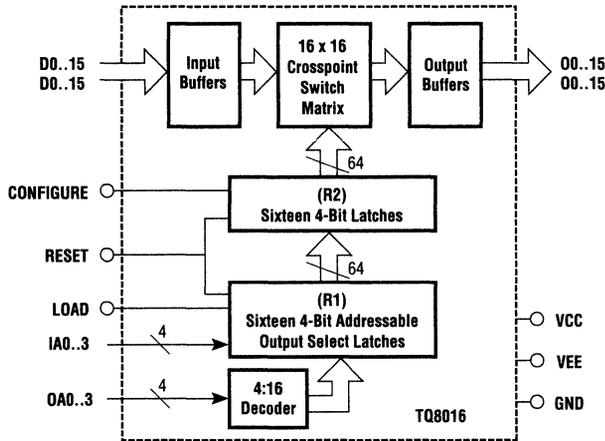
For technical questions and additional information on specific applications:

Email: applications@tqs.com

The information provided herein is believed to be reliable; TriQuint assumes no liability for inaccuracies or omissions. TriQuint assumes no responsibility for the use of this information, and all such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. TriQuint does not authorize or warrant any TriQuint product for use in life-support devices and/or systems.

Copyright © 1997 TriQuint Semiconductor, Inc. All rights reserved.

Revision 1.0.A October 1997



The TQ8016 is a 16 x 16 differential digital crosspoint switch capable of handling 1.3 Gbit/s data rate. The high data rate and exceptional signal fidelity is made possible with TriQuint's fully differential Source-Coupled FET Logic (SCFL) standard cells. The symmetrical switching characteristic inherent in differential logic results in low signal skew and crosstalk for maximum signal fidelity.

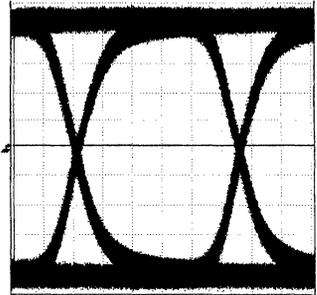
The user can independently configure any switch output to any input, including an input chosen by another output. To configure the switch, the 4-bit output address (OA0..3) is decoded to enable the loading of the 4-bit input selection data (IA0..3) on the rising edge of the LOAD signal. The process is repeated until all desired connections are programmed. By bringing the CONFIGURE signal high, the contents of the Output Select Latches are transferred in parallel to a second row of 4-bit latches (R2), causing the switch reconfiguration.

This double row architecture minimizes the time to completely reconfigure the switch since a new set of addresses can be loaded to the Output Select Latches (R1) while the switch is active (transmitting). At the time of reconfiguration, no data drop-out occurs for any output whose input connection does not change.

For applications which do not require synchronous configuration of the switch, the LOAD and CONFIGURE inputs may be tied together.

TQ8016

1.3 Gigabit/sec 16x16 Digital ECL Crosspoint Switch



Typical output waveform with all channels driven

Features

- >1.3 Gigabit/sec data rate
- Non-blocking architecture
- ± 200 ps delay match (one input to all outputs)
- ECL-level data inputs/outputs; CMOS-level control inputs
- Low crosstalk
- Fully differential data path
- Double row of output select latches minimizes reconfiguration time
- Available in 132-pin leaded chip carrier

TQ8016

Figure 1. TQ8016 Architecture

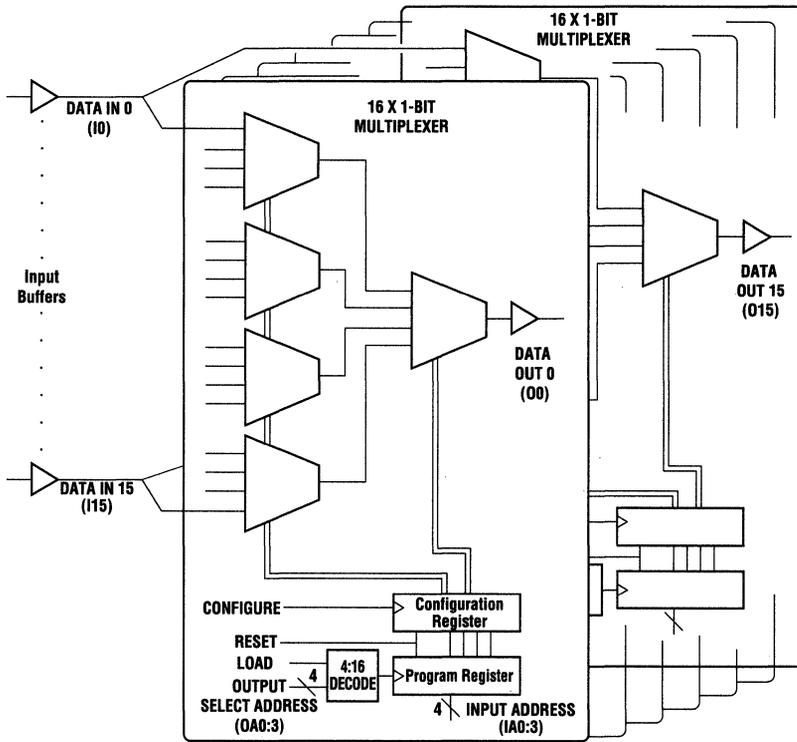
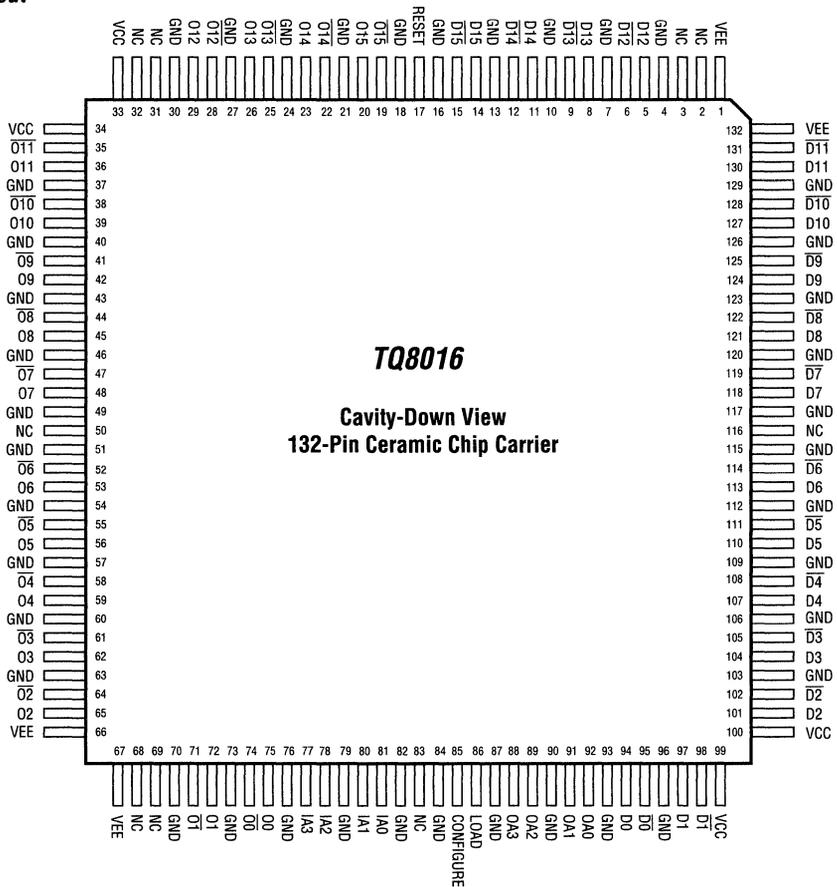


Table 1. Pin Descriptions

Pin Name	Levels	Description
D0–D15	ECL	Differential Data Inputs
D0–D15	ECL	Differential Data Inputs
D0–D15	ECL	Differential Data Inputs
O0–O15	ECL	Differential Data Outputs
O0–O15	ECL	Differential Data Outputs
IA0–IA3	CMOS	Input Address
OAO–OA3	CMOS	Output Address
CONFIGURE	CMOS	Switch Reconfiguration

Figure 2. Pinout



SWITCHING PRODUCTS

TQ8016
Cavity-Down View
132-Pin Ceramic Chip Carrier

Table 1. Pin Descriptions (continued)

Pin Name	Levels	Description
RESET	CMOS	Configures the switch to <i>Broadcast</i> or <i>Pass-Through</i> modes, overwriting existing configurations. Broadcast mode: All output ports are connected to data input port 0. This mode is selected by applying a RESET “high” pulse with CONFIGURE held “low.” Pass-through mode: I0 is connected to O0, I1 to O1, and so on. This mode is selected by applying a RESET “high” pulse with CONFIGURE held “high.”
LOAD	CMOS	Loads Input Address
GND	0 V.	Ground Reference
VEE	-5 V.	Power Supply
VCC	+5 V.	Power Supply

Table 2. Absolute Maximum Ratings⁴

Symbol	Parameter	Absolute Max. Rating	Notes
T _{STOR}	Storage Temperature	-65° C to +150° C	
T _J	Junction Temperature	-55° C to +150° C	
T _C	Case Temperature Under Bias	-55° C to +125° C	1
V _{CC}	Supply Voltage	0 V to +7 V	2
V _{EE}	Supply Voltage	-7 V to 0 V	2
V _{TT}	Load Termination Supply Voltage	V _{EE} to 0 V	3
V _{IN}	Voltage Applied to Any ECL Input; Continuous	V _{EE} -0.5 V to +0.5 V	
I _{IN}	Current Into Any ECL Input; Continuous	-1.0 mA to +1.0 mA	
V _{IN}	Voltage Applied to Any TTL/CMOS Input; Continuous	-0.5 V to V _{CC} +0.5 V	
I _{IN}	Current Into Any TTL/CMOS Input; Continuous	-1.0 mA to +1.0 mA	
V _{OUT}	Voltage Applied to Any ECL Output	V _{EE} -0.5 V to +0.5 V	3
I _{OUT}	Current From Any ECL Output; Continuous	-40 mA	
P _D	Power Dissipation per Output P _{OUT} = (GND - V _{OUT}) x I _{OUT}	50 mW	

- Notes: 1. T_C is measured at case top.
 2. All voltages specified with respect to GND, defined as 0V.
 3. Subject to I_{OUT} and power dissipation limitations.
 4. Absolute maximum ratings, as detailed in this table, are the ratings beyond which the device's performance may be impaired and/or permanent damage to the device may occur. Functionality and/or adherence to electrical specifications is not implied when the device is subjected to conditions that exceed, singularly or in combination, the operating range specified in the Recommended Operating Conditions table, below.

Table 3. Recommended Operating Conditions³

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
T _C	Case Operating Temperature	0	25	85	°C	1
GND	Ground Reference Voltage		0		V	
V _{CC}	Supply Voltage	4.5		5.5	V	
V _{EE}	Supply Voltage	-5.5		-4.5	V	
V _{TT}	Load Termination Supply Voltage		-2.0		V	2
R _{LOAD}	Output Termination Load Resistance		50			2

- Notes: 1. T_C measured at case top. Use of adequate heatsink is required.
 2. The V_{TT} and R_{LOAD} combination is subject to maximum output current and power restrictions.
 3. Functionality and/or adherence to electrical specifications is not implied when the device is subjected to conditions that exceed, singularly or in combination, the operating ranges specified.

Table 4. DC Characteristics¹ $T_C = 0^\circ\text{C to } 85^\circ\text{C}$, $V_{CC} = 4.5\text{ V to } 5.5\text{ V}$, $V_{EE} = -5.5\text{ V to } -4.5\text{ V}$, $GND = 0\text{ V}$, unless otherwise indicated.

Symbol	Parameter	Min	Typ	Max	Units	Test Cond.	Notes
V_{IH}	ECL Input Voltage High	-1100		-500	mV		
V_{IL}	ECL Input Voltage Low	V_{TT}		-1500	mV		
I_{IH}	ECL Input Current High			+30	μA	$V_{IH} = 0.7\text{ V}$	
I_{IL}	ECL Input Current Low	-30			μA	$V_{IL} = -2.0\text{ V}$	
V_{ICM}	ECL Input Common Mode Voltage	-1500		-1100	mV		
V_{IDIF}	ECL Input Differential Voltage (P-P)	400		1200	mV		
V_{IH}	CMOS Input Voltage High	3.5		V_{CC}	V		
V_{IL}	CMOS Input Voltage Low	0		1.5	V		
I_{IH}	CMOS Input Current High			+100	μA	$V_{IH} = V_{CC}$	
I_{IL}	CMOS Input Current Low	-100			μA	$V_{IL} = 0\text{ V}$	
V_{OCM}	ECL Output Common Mode	-1500		-1100	mV		
V_{ODIF}	ECL Output Differential Voltage	600			mV		
V_{OH}	ECL Output Voltage High	-1000		-600	mV		
V_{OL}	ECL Output Voltage Low	V_{TT}		-1600	mV		
I_{OH}	ECL Output Current High	20	23	27	mA		
I_{OL}	ECL Output Current Low	0	5	8	mA		
I_{CC}	Power Supply Current		15	20	mA		2
I_{EE}	Power Supply Current		730	950	mA		2

Notes: 1. Test conditions unless otherwise indicated: $V_{TT} = -2.0\text{ V}$, $R_{LOAD} = 50\ \Omega$ to V_{TT} .

2. Positive current is defined as flowing into the device and negative current as flowing out of the device.

I_{CC} typically flows into the device and I_{EE} flows out of the device.

Table 5. AC Characteristics¹ – Within recommended operating conditions, unless otherwise indicated.

Symbol	Parameter	Min	Typ	Max	Units	Notes
	Maximum Data Rate/Port			1.3	Gb/s	1,2
	Jitter			150	ps pk-pk	1
T_1	Channel Propagation Delay		1200	2000	ps	
T_2	Ch-to-Ch Propagation Delay Skew		400	500	ps	
T_3	CONFIG to Data Out (Oi) Delay			5	ns	
T_4	LOAD Pulse Width	7			ns	
T_5	CONFIG Pulse Width	7			ns	
T_6	IAi to LOAD High Setup Time	0			ns	
T_7	LOAD to IAi Low Hold Time	3			ns	
T_8	OAI to LOAD High Setup Time	0			ns	
T_9	LOAD to OAI Low Hold Time	3			ns	
T_{10}	Load \uparrow to CONFIG \uparrow	0			ns	
T_{11}	RESET Pulse Width	10			ns	
$T_{R,F}$	Output Rise or Fall Time		250	400	ps	3

Notes: 1. Test conditions: $V_{TT} = -2.0\text{ V}$, $R_{LOAD} = 50\ \Omega$ to V_{TT} ; ECL inputs: $V_{IH} = -1.1\text{ V}$; $V_{IL} = -1.5\text{ V}$; CMOS inputs: $V_{IH} = 3.5\text{ V}$, $V_{IL} = 1.5\text{ V}$; ECL outputs: $V_{OH} \geq -1.0\text{ V}$, $V_{OL} \leq -1.6\text{ V}$; ECL inputs rise and fall times $\leq 1\text{ ns}$; CMOS inputs rise and fall times $\leq 20\text{ ns}$. A bit error rate of 1E-13 BER or better for 2²³-1PRBS pattern, jitter and rise/fall times are guaranteed through characterization.

2. 1.2 Gb/s Non-Return-Zero (NRZ) data equivalent to 600 MHz clock signal.

3. Rise and fall times are measured at the 20% and 80% points of the transition from V_{OL} max to V_{OL} min.

Figure 3. Timing Diagram — Switch Configuration

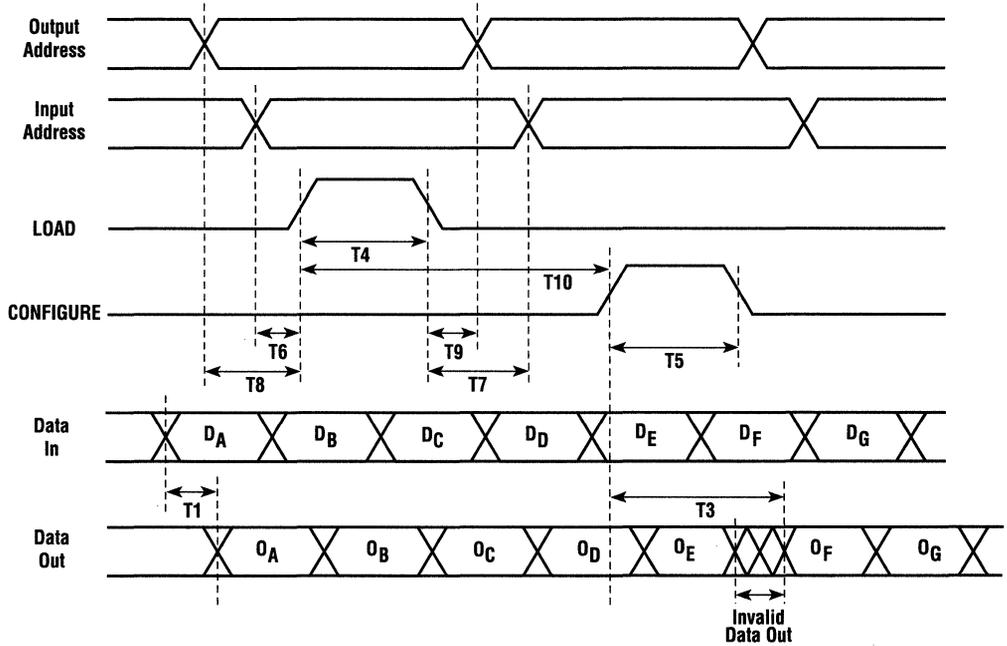
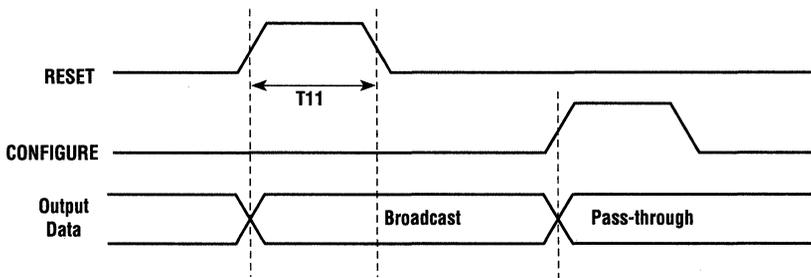
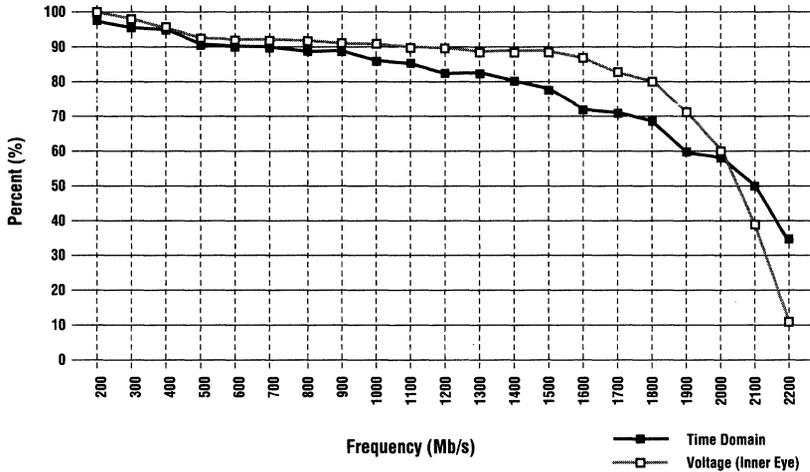


Figure 4. Timing Diagram — Reset



- Notes:
1. LOAD input must remain LOW to insure correct programming of the switch
 2. "Broadcast" is defined as data input 0 to all data outputs (0..15).
 3. "Pass-through" is defined as data input 0 to data output 0, data input 1 to data output 1, etc.

Figure 5. AC Performance Measurements
(Percent Recoverable "Eye" vs. Frequency 16 x 16)



SWITCHING PRODUCTS

Typical Error-Free Area

The graph in Figure 5 shows the typical error-free area of a $2^{23} - 1$ Pseudo-Random Bit Stream (PRBS) "eye" pattern. Data is provided for both time and voltage domains of the differential DINO to DOUT0 data path for various data rates. An interference pattern was applied to all other inputs in parallel to induce worst-case cross talk.

For the time domain, Peak-to-Peak Jitter was measured at the eye crossing.

An error-free percentage value was computed using the following formula:

$$(Data_Period - PPJitter) \times 100 / Data_Period$$

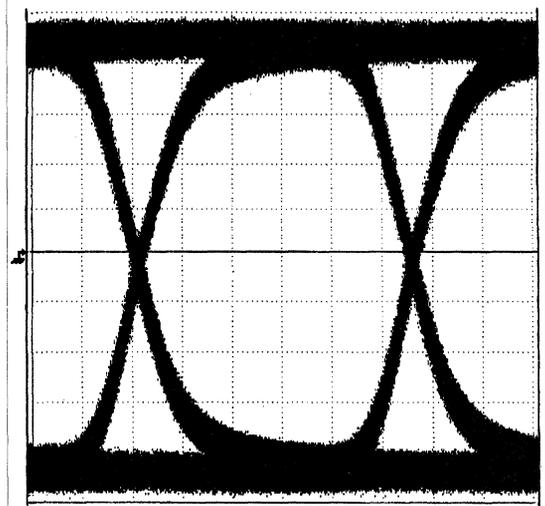
Voltage values are referenced to an initial inner eye measurement at 400 MBs. Subsequent percentage values were computed using the following formula:

$$V_{INNER} \times 100 / V_{INNER} @ 400\ MBs$$

Table 6. Typical Differential Waveform Characteristics
(OUT – OUT)

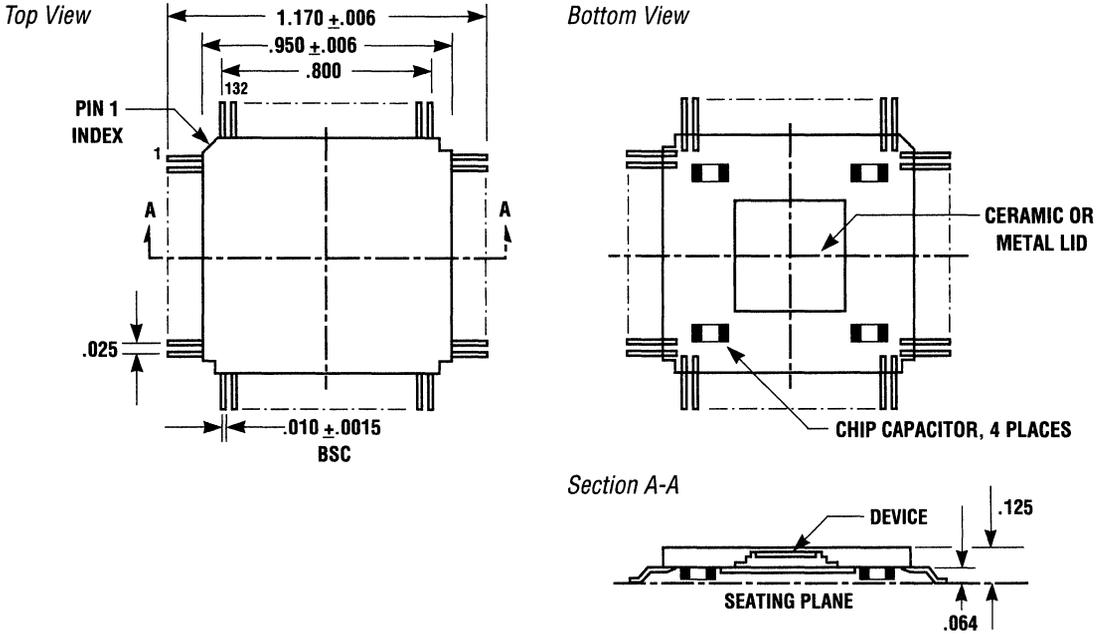
Frequency	1200 Mb/s
Fall Time (20% – 80%)	195 ps
Rise Time (20% – 80%)	1200 Mb/s
Jitter (peak-to-peak)	40 ps
Time/division	125 ps
Volts/division	250 mV

Figure 5. 1200 Mb/s Data "Eye" Pattern



Time/Div: 150 ps

Figure 6. Mechanical Dimensions



SWITCHING PRODUCTS

Ordering Information

TQ8016-M 1.3 Gb/s 16x16 ECL Crosspoint Switch

Additional Information

For latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com Tel: (503) 615-9000
 Email: sales@tqs.com Fax: (503) 615-8900

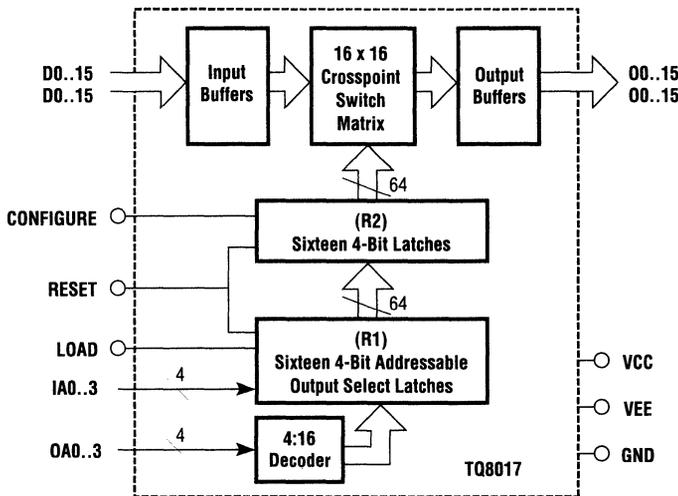
For technical questions and additional information on specific applications:

Email: applications@tqs.com

The information provided herein is believed to be reliable; TriQuint assumes no liability for inaccuracies or omissions. TriQuint assumes no responsibility for the use of this information, and all such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. TriQuint does not authorize or warrant any TriQuint product for use in life-support devices and/or systems.

Copyright © 1997 TriQuint Semiconductor, Inc. All rights reserved.

Revision 1.0.A October 1997



The TQ8017 is a non-blocking 16 x 16 digital crosspoint switch capable of data rates greater than 1.25 Gigabits per second per port. Utilizing a fully differential internal data path and PECL I/O, the TQ8017 offers a high data rate with exceptional signal fidelity. The symmetrical switching and noise rejection characteristics inherent in differential logic result in low jitter and signal skew. The TQ8017 is ideally suited for digital video, data communications and telecommunication switching applications.

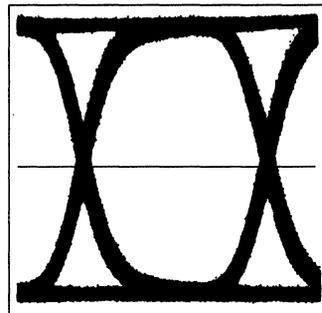
The non-blocking architecture uses 16 fully independent 16:1 multiplexers (see diagram on page 2), allowing each output port to be independently programmed to any input port. The switch is configured by sequentially loading each multiplexer's 4-bit program latch (OA0:3) with the desired input port address (IA0:3) and enabling the LOAD pin. When complete, the CONFIGURE pin is strobed and all new configurations are simultaneously transferred into the switch multiplexers. Data integrity is maintained on all unchanged data paths.

Electrical Characteristics

	Min	Max	Units
Data Rate/port	1.25		Gb/s
Jitter		150	ps pk-pk
Channel Propagation Delay		2000	ps
Ch-to-Ch Propagation Delay Skew		500	ps

TQ8017

**1.25 Gigabit/sec
16x16 Digital PECL
Crosspoint Switch**



Typical output waveform with all channels driven

Features

- >20 Gb/s aggregate BW
- 1.25 Gb/s/port NRZ data rate
- Non-blocking architecture
- 500 ps delay match
- Differential PECL-level data I/O; Selectable CMOS/TTL-level control inputs
- Low jitter and signal skew
- Fully differential data path
- Double-buffered configuration latches
- 132-pin MQFP package
- Single +5V supply

Applications

- Telecom/Datacom Switching
- Hubs and Routers
- Video Switching

SWITCHING PRODUCTS

TQ8017

Figure 1. TQ8017 Architecture

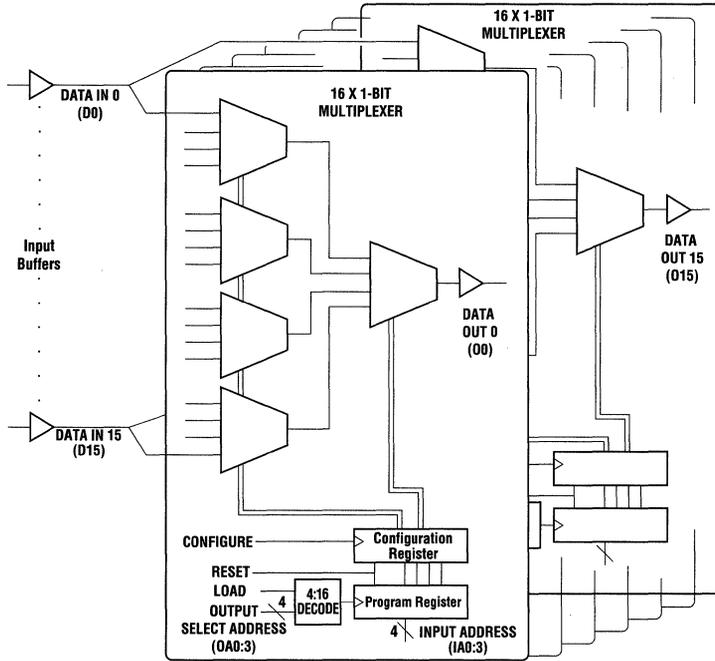


Table 1. Absolute Maximum Ratings⁵

Symbol	Parameter	Absolute Max. Rating	Notes
T _{STOR}	Storage Temperature	-65° C to +150° C	
T _{CH}	Junction (Channel) Temperature	-65° C to +150° C	1
T _C	Case Temperature Under Bias	-65° C to +125° C	2
V _{CC}	Supply Voltage	0 V to +7 V	3
V _{TT}	Load Termination Supply Voltage	V _{CC} to 0 V	4
V _{IN}	Voltage Applied to Any PECL Input; Continuous	GND -0.5 V to V _{CC} +0.5 V	
I _{IN}	Current Into Any PECL Input; Continuous	-1.0 mA to +1.0 mA	
V _{IN}	Voltage Applied to Any TTL/CMOS Input; Continuous	-0.5 V to V _{CC} +0.5 V	
I _{IN}	Current Into Any TTL/CMOS Input; Continuous	-1.0 mA to +1.0 mA	
V _{OUT}	Voltage Applied to Any PECL Output	GND -0.5 V to V _{CC} +0.5 V	4
I _{OUT}	Current From Any PECL Output; Continuous	-40 mA	
P _D	Power Dissipation per Output P _{OUT} = (GND - V _{OUT}) × I _{OUT}	50 mW	

- Notes:
1. For die applications.
 2. T_C is measured at case top.
 3. All voltages specified with respect to GND, defined as 0V.
 4. Subject to I_{OUT} and power dissipation limitations.
 5. Absolute maximum ratings, as detailed in this table, are the ratings beyond which the device's performance may be impaired and/or permanent damage to the device may occur.

Table 2. Recommended Operating Conditions⁴

Symbol	Parameter	Min	Typ	Max	Units	Notes
T _C	Case Operating Temperature	0		85	°C	1,3
V _{CC}	Supply Voltage	4.5		5.5	V	
V _{TT}	Load Termination Supply Voltage		V _{CC} - 2.0		V	2
R _{LOAD}	Output Termination Load Resistance		50		Ω	2
Θ _{JC}	Thermal Resistance Junction to Case			7	°C/W	

- Notes: 1. T_C measured at case top. Use of adequate heatsink is required.
 2. The V_{TT} and R_{LOAD} combination is subject to maximum output current and power restrictions.
 3. Contact the Factory for extended temperature range applications.
 4. Functionality and/or adherence to electrical specifications is not implied when the device is subjected to conditions that exceed, singularly or in combination, the operating range specified.

Table 3. Pin Descriptions

Signal	Name/Level	Description																														
D0 to D15, ND0 to ND15	Data input true and complement. Differential PECL	Differential data input ports.																														
O0 to O15, NO0 to NO15	Data output true and complement. Differential PECL	Differential data output ports.																														
IA0:3	Input address. CMOS/TTL	Input port selection address that is written into the selected output port program latches (OA0:3). <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>IA3</th> <th>IA2</th> <th>IA1</th> <th>IA0</th> <th>Input port</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>2</td> </tr> <tr> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>15</td> </tr> </tbody> </table>	IA3	IA2	IA1	IA0	Input port	0	0	0	0	0	0	0	0	1	1	0	0	1	0	2	⋮	⋮	⋮	⋮	⋮	1	1	1	1	15
IA3	IA2	IA1	IA0	Input port																												
0	0	0	0	0																												
0	0	0	1	1																												
0	0	1	0	2																												
⋮	⋮	⋮	⋮	⋮																												
1	1	1	1	15																												
OA0:3	Output select address. CMOS/TTL	Output port selection address. Selects the output port program latches to which the input port selection address (IA0:3) is written. <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>OA3</th> <th>OA2</th> <th>OA1</th> <th>OA0</th> <th>Output port</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>2</td> </tr> <tr> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>15</td> </tr> </tbody> </table>	OA3	OA2	OA1	OA0	Output port	0	0	0	0	0	0	0	0	1	1	0	0	1	0	2	⋮	⋮	⋮	⋮	⋮	1	1	1	1	15
OA3	OA2	OA1	OA0	Output port																												
0	0	0	0	0																												
0	0	0	1	1																												
0	0	1	0	2																												
⋮	⋮	⋮	⋮	⋮																												
1	1	1	1	15																												
LOAD	CMOS/TTL	Enables the selected output port program latches while set 'high'. Latches the data when set to a 'low' level.																														
CONFIGURE	CMOS/TTL	Transfers the program latches data to the configuration latches and implements the switch changes while set 'high'. Latches the data when set to a 'low' level.																														
RESET	CMOS/TTL	Configures the switch into Broadcast or Pass-Through mode, overwriting existing configurations. Broadcast mode: All output ports are connected to data input port 0. This mode is selected by applying a RESET "high" pulse with CONFIGURE held "low." Pass-through mode: IO is connected to O0, I1 to O1, etc. This mode is selected by applying a RESET "high" pulse with CONFIGURE held "high."																														
CNTRL LVL	Input level control. GND/Open	Selects the input levels for the input address (IA0:3), output address (OA0:3), CONFIGURE, LOAD and RESET inputs. Inputs are configured for TTL when tied to GND and CMOS when left unconnected.																														

TQ8017

Table 4. DC Characteristics^{1,2} – Within recommended operating conditions, unless otherwise indicated.

Symbol	Parameter	Min	Max	Units	Test Cond.	Notes
V _{IH}	PECL Input Voltage High	V _{CC} -1.1	V _{CC} -0.5	V		
V _{IL}	PECL Input Voltage Low	V _{TT}	V _{CC} -1.5	V		
I _{IH}	PECL Input Current High		+30	μA	V _{IH} = V _{CC} -0.7 V	
I _{IL}	PECL Input Current Low	-30		μA	V _{IL} = V _{CC} -2.0 V	
V _{ICM}	PECL Input Common Mode Voltage	V _{CC} -1.5	V _{CC} -1.1	V		
V _{IDIF}	PECL Input Differential Voltage (pk-pk)	400	1200	mV		
V _{IH}	CMOS/TTL Input Voltage High	3.5/2.0	V _{CC} /V _{CC}	V		2
V _{IL}	CMOS/TTL Input Voltage Low	0/0	1.5/0.8	V		2
I _{IH}	CMOS/TTL Input Current High		+200	μA	V _{IH} = V _{CC}	2
I _{IL}	CMOS/TTL Input Current Low		-100	μA	V _{IL} = 0 V	2
V _{OCM}	PECL Output Common Mode	V _{CC} -1.5	V _{CC} -1.1	V		
V _{ODIF}	PECL Output Differential Voltage	600		mV		
V _{OH}	PECL Output Voltage High	V _{CC} -1.0	V _{CC} -0.6	V		
V _{OL}	PECL Output Voltage Low	V _{TT}	V _{CC} -1.6	V		
I _{OH}	PECL Output Current High	20	27	mA		
I _{OL}	PECL Output Current Low	0	8	mA		
I _{CC}	Power Supply Current (+)		970	mA		

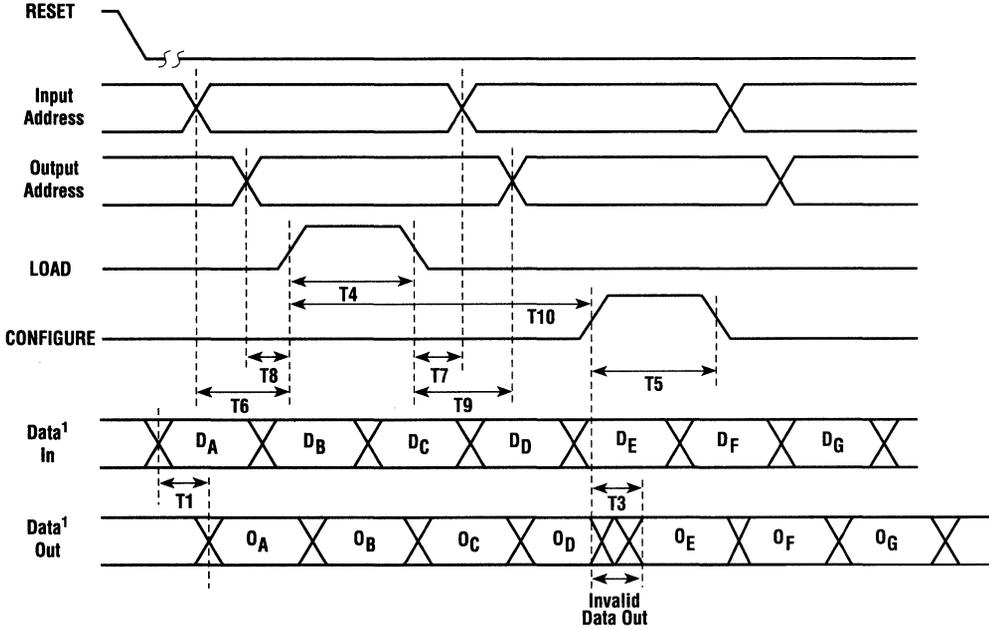
- Notes: 1. Test conditions unless otherwise indicated: V_{TT} = V_{CC} - 2.0 V, R_{LOAD} = 50 Ω to V_{TT}.
 2. Input level is selected by the CNTRL LVL input. Tying CNTRL LVL to GND selects TTL levels, leaving CNTRL LVL OPEN selects CMOS levels.

Table 5. AC Characteristics¹ – Within recommended operating conditions, unless otherwise indicated.

Symbol	Parameter	Min	Typ	Max	Units	Notes
	Maximum Data Rate/Port			1.25	Gb/s	1,2
	Jitter			150	ps pk-pk	1
T ₁	Channel Propagation Delay			2000	ps	3
T ₂	Ch-to-Ch Propagation Delay Skew			500	ps	
T ₃	CONFIG to Data Out (Oi) Delay			5	ns	
T ₄	LOAD Pulse Width	7			ns	
T ₅	CONFIG Pulse Width	7			ns	
T ₆	IAi to LOAD High Setup Time	0			ns	
T ₇	LOAD to IAi Low Hold Time	3			ns	
T ₈	OAI to LOAD High Setup Time	0			ns	
T ₉	LOAD to OAI Low Hold Time	3			ns	
T ₁₀	Load ↑ to CONFIG ↑	0			ns	
T ₁₁	RESET Pulse Width	10			ns	
T _{R,F}	Output Rise or Fall Time		250	400	ps	3

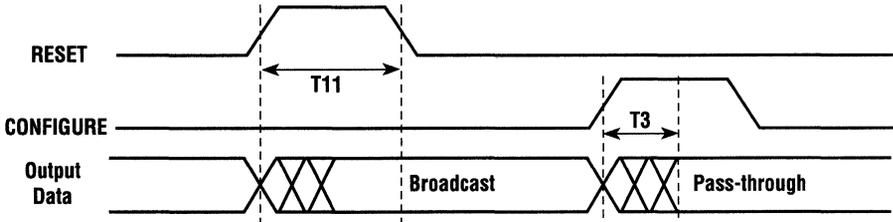
- Notes: 1. Test conditions: V_{CC} = 5.0 V; V_{TT} = 3.0 V, R_{LOAD} = 50 Ω to V_{TT}; PECL inputs: V_{IH} = 3.9 V; V_{IL} = 3.5 V; CMOS inputs: V_{IH} = 3.5 V, V_{IL} = 1.5 V; PECL outputs: V_{OH} ≥ 4.0 V, V_{OL} ≤ 3.4 V; PECL inputs rise and fall times ≤ 1 ns; CMOS inputs rise and fall times ≤ 20 ns. A bit error rate of 1E-13 BER or better for 2²³-1 PRBS pattern, jitter and rise/fall times are guaranteed through characterization.
 2. 1.2 Gb/s Non-Return-Zero (NRZ) data equivalent to 600 MHz clock signal.
 3. Rise and fall times are measured at the 20% and 80% points of the transition from V_{OL} max to V_{OL} min.

Figure 2. Timing Diagram – Switch Configuration



Notes: 1. No data loss on unchanged paths

Figure 3. Timing Diagram – Reset



- Notes: 1. LOAD input must remain LOW to insure correct programming of the switch.
- 2. "Broadcast" is defined as data input 0 to all data outputs (0...15).
- 3. "Pass-through" is defined as data input 0 to data output 0, data input 1 to data output 1, etc.

Typical Performance Data

Figure 4. Data Eye Closure

Percent RMS vs Data Rate (typical)

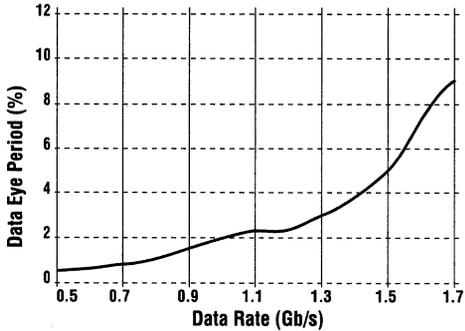


Figure 5. Data Eye Closure

Time & Amplitude vs Data Rate (typical)

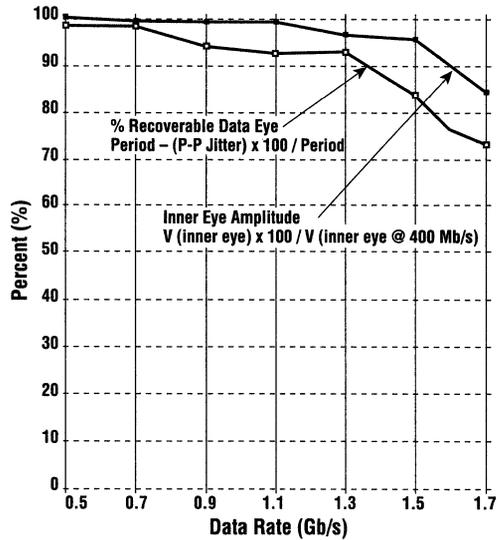


Figure 6. RMS Jitter vs. Data Rate (typical)

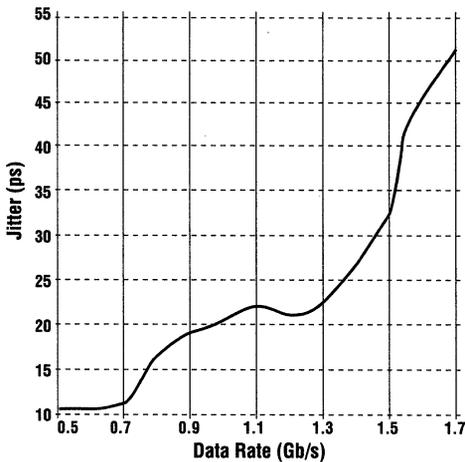
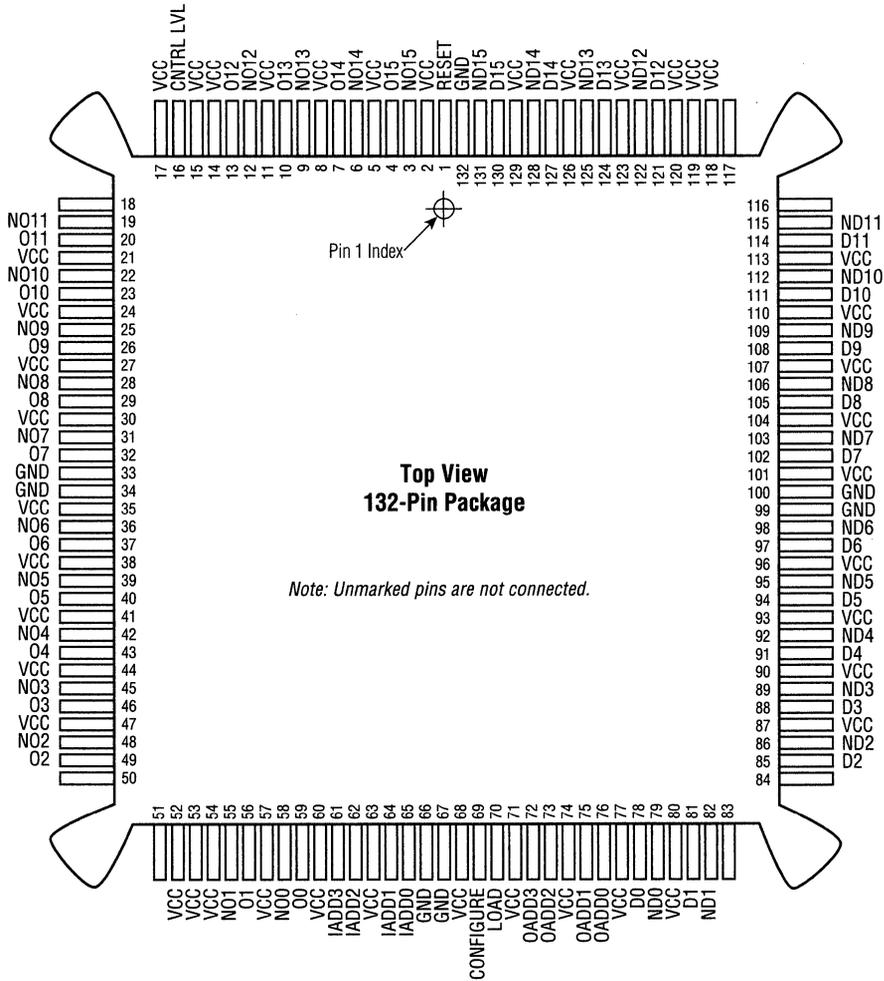


Figure 5. Package Pinout

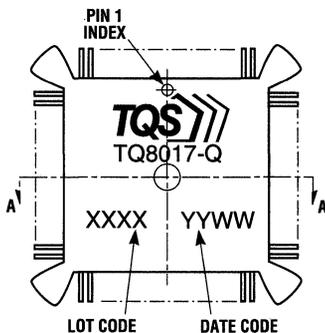


SWITCHING PRODUCTS

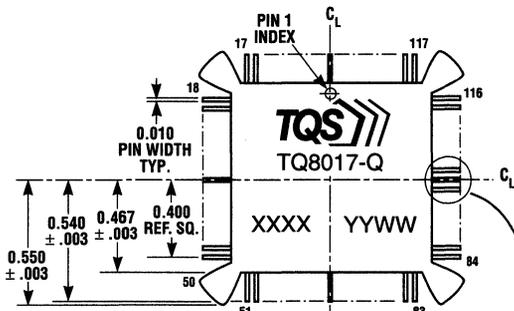
TQ8017

Figure 6. Mechanical Dimensions

Bottom View

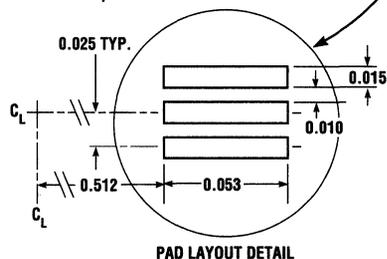
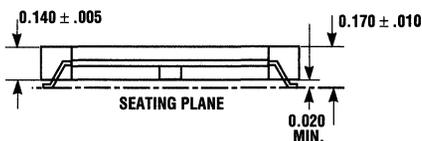


Top View



- Notes: 1. Part is symmetrical about the center axes.
 2. Centerline bisects center pin in both directions.
 3. See pad detail below.

Section A-A



Ordering Information

TQ8017-Q 1.25 Gb/s 16x16 PECL Crosspoint Switch

Additional Information

For latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com Tel: (503) 615-9000
 Email: sales@tqs.com Fax: (503) 615-8900

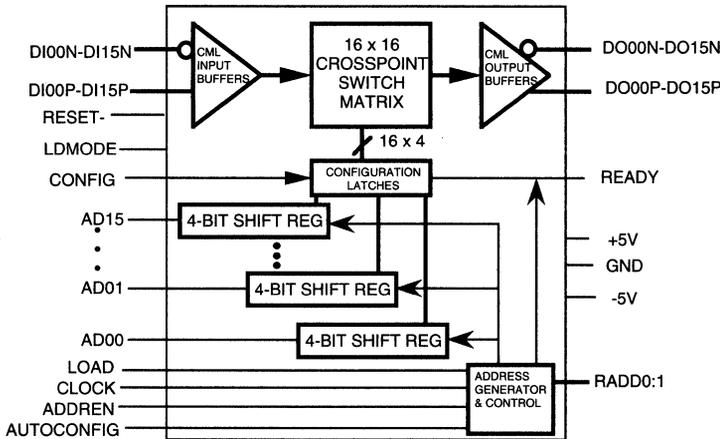
For technical questions and additional information on specific applications:

Email: applications@tqs.com

The information provided herein is believed to be reliable; TriQuint assumes no liability for inaccuracies or omissions. TriQuint assumes no responsibility for the use of this information, and all such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. TriQuint does not authorize or warrant any TriQuint product for use in life-support devices and/or systems.

Copyright © 1997 TriQuint Semiconductor, Inc. All rights reserved.

Revision 1.0.A October 1997



The TQ8025 is a non-blocking 16 x 16 digital crosspoint switch capable of data rates greater than 2.5 Gigabits per second per port. Utilizing a fully differential internal data path and PECL/CML I/O, the TQ8025 offers an extremely high data rate with exceptional signal fidelity. The use of fully differential logic results in low crosstalk, jitter, and signal skew. The TQ8025 is ideally suited for digital video, data communications, telecommunication switching, and cross-connect applications.

The non-blocking architecture uses 16 fully independent 16:1 multiplexers which allow each output port to be independently programmed to any input port. The TQ8025 offers two programming options: a flexible port-by-port option and a fast configuration option.

Using the fast configuration option, all 16 switch ports are programmed within 100ns by serially loading four 16-bit input port selection words. Two output pins (RADD0,1) are provided to drive an external RAM ($n \times 4 \times 16$ bits) used to store the switch configuration. An Autoconfigure option automatically transfers the new configurations into the switch core. Autoconfiguration occurs after the last input selection word is clocked into the programming registers.

Data integrity is maintained on all unchanged data paths for both the port-by-port and fast configuration options.

TQ8025

PRELIMINARY DATA SHEET

2.5 Gigabit/sec 16x16 Digital Crosspoint Switch

Features

- 16 PECL/CML fully differential (back-terminated) outputs
- >2.5 Gb/s data bandwidth per channel
- >40 Gb/s aggregate bandwidth
- Non-blocking architecture
- <100 ns configuration time
- Autonomous control of external RAM for configuration data
- Low jitter and signal skew
- ± 100 ps delay match (one input to all outputs)
- Fully differential data path
- 132-pin MLC package with heat spreader

Applications

- SONET OC-48 data path
- Double-speed Fibre Channel
- Hubs and routers
- High-definition video switching
- Parallel processing

TQ8025

PRELIMINARY DATA SHEET

Specifications

Table 1. Absolute Maximum Ratings ⁴

Storage temperature	T_{STORE}	-65 °C to +150 °C
Junction temperature	T_{CH}	150 °C
Case temperature with bias ¹	T_C	$T_J = 150 °C$
Supply voltage ²	V_{CC}	0 V to +7.0 V
Voltage to any input ²	V_{IN}	-0.5 V to $V_{CC} + 0.5 V$
Voltage to any output ²	V_{OUT}	-0.5 V to $V_{CC} + 0.5 V$
Current to any input ²	I_{IN}	-1.0 mA to +1.0 mA
Current from any output ²	I_{OUT}	40 mA
Power dissipation of output ³	P_{OUT}	50 mW

Notes: 1. T_C is measured at the case top.

2. All voltages are measured with respect to GND 0V and are continuous.

3. $P_{OUT} = (V_{CC} - V_{OUT}) \times I_{OUT}$.

4. Absolute maximum ratings in this table are those beyond which the device's performance may be impaired and/or permanent damage may occur.

Table 2. Recommended Operating Conditions ⁴

Symbol	Parameter	Min	Typ	Max	Units	Notes
T_C	Case Operating Temperature	0	—	85	°C	1, 3
V_{CC}	Supply Voltage	4.75	—	5.25	V	
V_{TT}	Load Termination Supply Voltage		$V_{CC} - 2.0$		V	2
I_{CC}	Current Positive Supply	—	—	2.1	A	
R_{LOAD}	Output Termination Load Resistance		50		Ω	2
Θ_{JC}	Thermal Resistance Channel to Case			5.9	°C/W	

Notes: 1. T_C measured at case top. Use of adequate heatsink is required.

2. The V_{TT} and R_{LOAD} combination is subject to maximum output current and power restrictions.

3. Contact the Factory for extended temperature range applications.

4. Functionality and/or adherence to electrical specifications is not implied when the device is subjected to conditions that exceed, singularly or in combination, the operating range specified.

Table 3. DC Characteristics — CML I/O⁵

Symbol	Description	Test Conditions	Min	Nom	Max	Unit
V _{COM}	Common mode voltage	(Note 1)	V _{CC} - 600	—	V _{CC}	mV
V _{DIFF}	Differential voltage	(Note 1)	400	—	1200	mV
V _{IH}	Input HIGH voltage	(Note 2)	—	—	V _{CC}	mV
V _{IL}	Input LOW voltage		V _{CC} - 1100	—	—	mV
V _{OH}	Output HIGH voltage	(Note 3)	V _{CC} - 100	—	V _{CC}	mV
V _{OL}	Output LOW voltage	(Note 3)	V _{CC} - 1100	—	V _{CC} - 600	mV
I _{OH}	Output HIGH current	(Note 3, 4)	20	23	30	mA
I _{OL}	Output LOW current	(Note 3, 4)	0	5	8	mA

Table 4. DC Characteristics — PECL I/O⁵

Symbol	Description	Test Conditions	Min	Nom	Max	Unit
V _{COM}	Common mode voltage	(Note 1)	V _{CC} - 1500	—	V _{CC} - 1100	mV
V _{DIFF}	Differential voltage	(Note 1)	400	—	1200	mV
V _{IH}	Input HIGH voltage	(Note 2)	—	—	V _{CC} - 500	mV
V _{IL}	Input LOW voltage		V _{CC} - 2100	—	—	mV
V _{OH}	Output HIGH voltage	(Note 3)	V _{CC} - 1100	—	V _{CC} - 600	mV
V _{OL}	Output LOW voltage	(Note 3)	V _{CC} - 2100	—	V _{CC} - 1600	mV
I _{OH}	Output HIGH current	(Note 4)	20	23	30	mA
I _{OL}	Output LOW current	(Note 4)	0	5	8	mA
C _{IN}	Input capacitance		—	—	TBD	pF
C _{OUT}	Output capacitance		—	—	TBD	pF
VESD	ESD breakdown rating	(Note 5)	Class I	—	—	

Table 5. DC Characteristics — TTL I/O⁵

Symbol	Description	Test Conditions	Min	Nom	Max	Unit
V _{IH}	Input HIGH voltage		2.0	—	V _{CC}	V
V _{IL}	Input LOW voltage		0	—	0.8	V
I _{IH}	Input HIGH current	V _{IHMAX}	—	—	200	μA
I _{IL}	Input LOW current	V _{ILMIN}	-400	-200	—	μA
V _{OH}	Output HIGH voltage	I _{OH} = 50 mA	2.4	—	V _{CC}	V
V _{OL}	Output LOW voltage	I _{OH} = -20 mA	0	—	0.4	V
C _{IN}	Input capacitance		—	—	TBD	pF
C _{OUT}	Output capacitance		—	—	TBD	pF
VESD	ESD breakdown rating	(Note 5)	Class I	—	—	

Notes (Tables 3, 4, and 5):

1. Differential inputs.
2. V_{REF} = 1300 mV.
3. R_{LOAD} = 50 ohms to V_{TT} = V_{CC} - 2.0 V.
4. Not tested; consistent with V_{OH} and V_{OL} tests.
5. Specifications apply over recommended operating ranges.

TQ8025

PRELIMINARY DATA SHEET

Table 6. AC Characteristics

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
T _{PW}	D(0:15) minimum pulse width	(Note 1)	360	—	—	ps
T _{R/F}	O(0:15) rise/fall time 20-80%	(Note 1)	—	—	150	ps
T _{PD}	D(0:15), O(0:15) delay time	(Note 1)	—	—	2.5	ns
T _{SKEW}	Path delay matching	(Note 1)	—	300	—	ps
T _{JITTER}	Jitter	(Note 2)	—	—	75	ps pk-pk

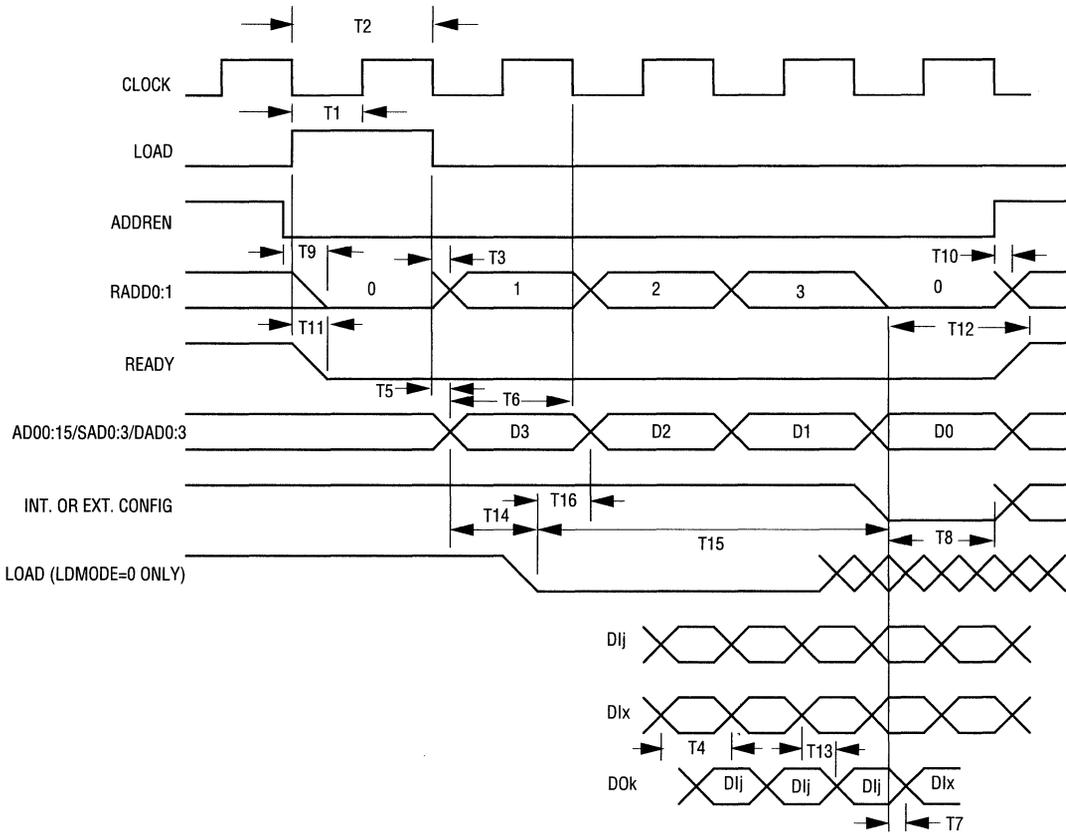
Notes: 1. Minimum V_{OH} to maximum V_{OL} levels.

2. Crossing of (On)—(NOn) measured with 2²³ - 1 PRBS, measured over extended time.

Table 7 TQ8025 Timing

Symbol	Parameter	Min.	Max.	Units
T1	CLOCK low	4	—	ns
T2	CLOCK period	20	—	ns
T3	LOAD to RADD delay	3	—	ns
T4	Data input pulse width	400	—	ps
T5	LOAD to ADO setup time	2	—	ns
T6	ADO to CLOCK setup time	18	—	ns
T7	CONFIG to D _{OUT} delay	4	—	ns
T8	CONFIG pulse width	10	—	ns
T9	ADDREN to RADD delay	3	—	ns
T10	ADDREN to RADD tristate	3	—	ns
T11	LOAD to READY delay	3	—	ns
T12	RADD to READY delay	3	—	ns
T13	Data in to D _{OUT} delay	2	—	ns
T14	SAD/DAD setup to LOAD	3	—	ns
T15	LOAD pulse width / time to CONFIG	3	—	ns

Figure 1. TQ8025 timing (LDMODE=1)



SWITCHING PRODUCTS

Table 8. TQ8025 Pin Descriptions

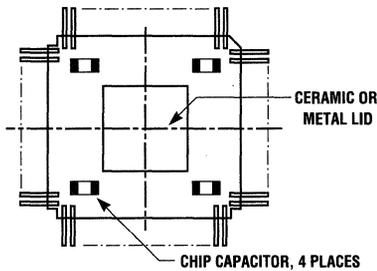
Signal	Name/Level	Description
DI00P-DI15P	Data input true and complement	Differential data input ports. $V_H = 0\text{ V}$, $V_L = -300\text{ mV max.}$
DI0N-DI15N	Differential CML/PECL input	Internal 50 ohm terminations to VTT (CML = 0 V; ECL = -2.0 V).
DO0P-DO15P, DO0N-DO15N	Data output true and complement Differential CML/PECL output	Differential data output ports. 600 mV min. differential swing.
AD00:15	Input address; TTL input	Serial input address, LSB first in time; ADn programs output port n.
RADD0:1	RAM address; TTL output, tristate	Used to generate address 0-3 during configure load from RAM.
ADDREN	Enable RADD0:2; TTL input	When low, enables RADD0:1; when high, forces RADD0:1 tristate.
CLOCK	Clock; TTL input	Controls cycle time of address generator and AUTOCONFIG.
AUTOCONFIG	Configure mode; TTL input	When high, internal CONFIGURE is automatically generated.
READY	READY; open-drain output	Indicates end of AUTOCONFIG or end of address LOAD cycle when high. Reset low by RESET-, CONFIG low, or LOAD rising. Requires external pullup to V_{CC} .
LOAD	LOAD; TTL input	For LDMODE=1, ADDREN=0: AUTOCONFIG=0, rising LOAD causes ADDR0:1 to generate RAM addresses, then READY is asserted after four clock ticks. For AUTOCONFIG=1, LOAD rising causes ADDR0:1 to generate addresses, causing an internal CONFIG to be generated, after which READY is asserted. For LDMODE=0, see SADO:3 and DADO:3.
CONFIGURE	CONFIGURE; PECL input Not internally terminated	Used to load address contents of internal address registers. Active LOW. Crosspoint will be configured within 4 ns (objective) of CONFIG falling low.
LDMODE	Load Mode; TTL input	When floated high, AD0-15 are used for configuration. When tied low, SADO-3 and DADO-3 are used for configuration. When AUTOCONFIG is disabled, and AD08-15 are ignored.
SADO:3	Source Address; TTL inputs	When LDMODE is low, specifies input address to be connected to output port specified by DADO:3. Latched by falling LOAD (LDMODE=0).
DADO:3	Destination Address; TTL input	When LDMODE is low, specifies output address to be connected to input port specified by SADO:3. Latched by falling LOAD (LDMODE=0).
VCC, GND, VTT	+5V, Ground; Termination Voltage	Power and ground pins. $V_{TT} = \text{GND}$ for CML inputs; $V_{TT} = V_{CC} - 2\text{V}$ for PECL inputs.
RESET-	Reset; TTL Input	While low, programs all output ports to connect to input port 0. Strobing CONFIG after reset restores user port programming if device power was stable since last user programming and during RESET-. Active low, schmitt triggered.

TQ8025

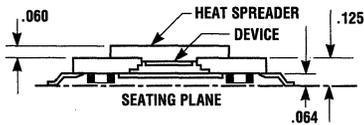
PRELIMINARY DATA SHEET

Figure 3. Mechanical Dimensions

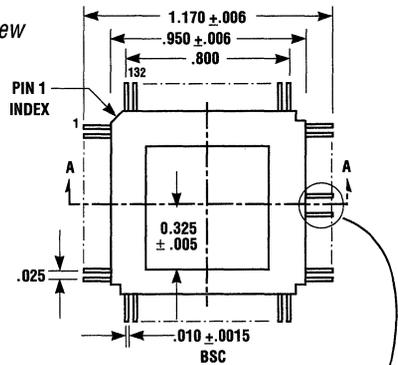
Bottom view



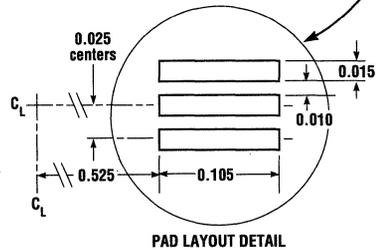
Section A-A



Top view



1. Part is symmetrical about the center axes.
2. Centerline bisects center pin in both directions.
3. See pad detail below.



Ordering Information

TQ8025

2.5 Gb/s 16x16 PECL Crosspoint Switch

Additional Information

For latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com **Tel:** (503) 615-9000

Email: sales@tqs.com **Fax:** (503) 615-8900

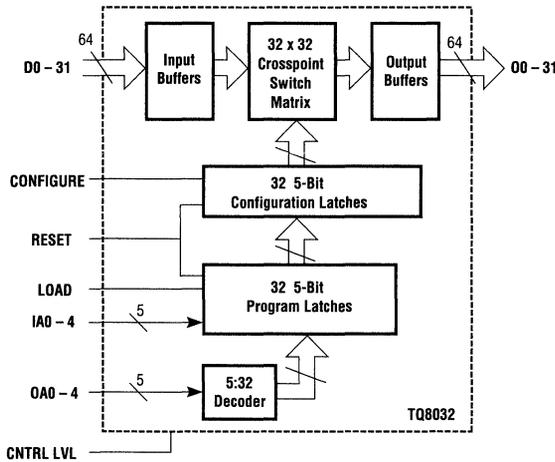
For technical questions and additional information on specific applications:

Email: applications@tqs.com

The information provided herein is believed to be reliable; TriQuint assumes no liability for inaccuracies or omissions. TriQuint assumes no responsibility for the use of this information, and all such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. TriQuint does not authorize or warrant any TriQuint product for use in life-support devices and/or systems.

Copyright © 1997 TriQuint Semiconductor, Inc. All rights reserved.

Revision 0.1.A October 1997



The TQ8032 is a non-blocking 32 x 32 digital crosspoint switch capable of 800 Megabits per second per port data rates. Utilizing a fully differential internal data path and ECL I/O, the TQ8032 offers a high data rate with exceptional signal fidelity. The symmetrical switching and noise rejection characteristics inherent in differential logic result in low jitter and signal skew. The TQ8032 is ideally suited for digital video, data communications and telecommunication switching applications.

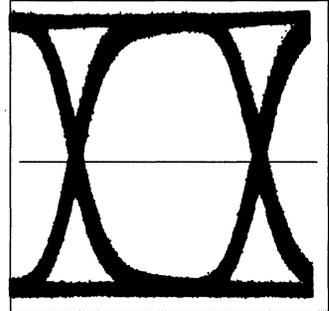
The non-blocking architecture uses 32 fully independent 32:1 multiplexers (see diagram on page 2), allowing each output port to be independently programmed to any input port. The switch is configured by sequentially loading each multiplexer's 5-bit program latch (OA0:4) with the desired input port address (IA0:4) and enabling the LOAD pin. When complete, the CONFIGURE pin is strobed and all new configurations are simultaneously transferred into the switch multiplexers. Data integrity is maintained on all unchanged data paths.

Electrical Characteristics

	Min	Max	Units
Data Rate/Port	800		Mb/s
Jitter		150	ps pk-pk
Channel Propagation Delay		2300	ps
Ch-to-Ch Propagation Delay Skew		500	ps

TQ8032

800 Megabit/sec 32x32 Digital ECL Crosspoint Switch



Typical output waveform with all channels driven

Features

- >25 Gb/s aggregate BW
- 800 Mb/s/port NRZ data rate
- Non-blocking architecture
- 500 ps delay match
- Differential ECL-level data I/O; Selectable CMOS/TTL-level control inputs
- Low jitter and signal skew
- Fully differential data path
- Double buffered configuration latches
- 196-pin CQFP package

Applications

- Telecom/Datacom Switching
- Hubs and Routers
- Video Switching

SWITCHING
PRODUCTS

TQ8032

Figure 1. Architecture

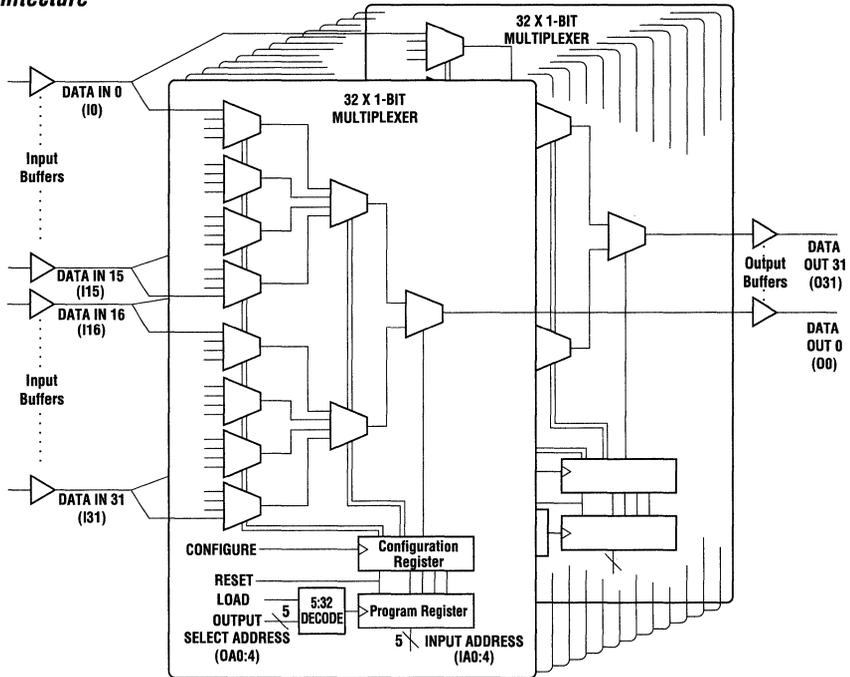


Table 2. Pin Descriptions

Signal	Name/Level	Description																																				
I0 to I31, NI0 to NI31	Data input true and complement. Differential ECL	Differential data input ports.																																				
O0 to O31, NO0 to NO31	Data output true and complement. Differential ECL	Differential data output ports.																																				
IA0:4	Input address. CMOS/TTL	Input port selection address that is written into the selected output port program latches (OA0:4). <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>IA4</th> <th>IA3</th> <th>IA2</th> <th>IA1</th> <th>IA0</th> <th>Input port</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>2</td></tr> <tr><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>31</td></tr> </tbody> </table>	IA4	IA3	IA2	IA1	IA0	Input port	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0	2	:	:	:	:	:	:	1	1	1	1	1	31
IA4	IA3	IA2	IA1	IA0	Input port																																	
0	0	0	0	0	0																																	
0	0	0	0	1	1																																	
0	0	0	1	0	2																																	
:	:	:	:	:	:																																	
1	1	1	1	1	31																																	
OA0:4 CMOS/TTL	Output select address.	Output port selection address. Selects the output port program latches to which the input port selection address (IA0:4) is written. <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>OA4</th> <th>OA3</th> <th>OA2</th> <th>OA1</th> <th>OA0</th> <th>Output port</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>2</td></tr> <tr><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>31</td></tr> </tbody> </table>	OA4	OA3	OA2	OA1	OA0	Output port	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0	2	:	:	:	:	:	:	1	1	1	1	1	31
OA4	OA3	OA2	OA1	OA0	Output port																																	
0	0	0	0	0	0																																	
0	0	0	0	1	1																																	
0	0	0	1	0	2																																	
:	:	:	:	:	:																																	
1	1	1	1	1	31																																	

TQ8032

Table 3. Absolute Maximum Ratings⁵

Symbol	Parameter	Absolute Max. Rating	Notes
T _{STOR}	Storage Temperature	-65° C to +150° C	
T _{CH}	Junction (Channel) Temperature	-65° C to +150° C	1
T _C	Case Temperature Under Bias	-65° C to +125° C	2
V _{CC}	Supply Voltage	0 V to +7 V	3
V _{EE}	Supply Voltage	-7 V to 0 V	3
V _{TT}	Load Termination Supply Voltage	V _{EE} to 0 V	4
V _{IN}	Voltage Applied to Any ECL Input; Continuous	V _{EE} -0.5 V to +0.5 V	
I _{IN}	Current Into Any ECL Input; Continuous	-1.0 mA to +1.0 mA	
V _{IN}	Voltage Applied to Any TTL/CMOS Input; Continuous	-0.5 V to V _{CC} +0.5 V	
I _{IN}	Current Into Any TTL/CMOS Input; Continuous	-1.0 mA to +1.0 mA	
V _{OUT}	Voltage Applied to Any ECL Output	V _{EE} -0.5 V to +0.5 V	4
I _{OUT}	Current From Any ECL Output; Continuous	-40 mA	
P _D	Power Dissipation per Output P _{OUT} = (GND - V _{OUT}) x I _{OUT}	50 mW	

Notes: 1. For die applications.

2. T_C is measured at case top.

3. All voltages specified with respect to GND, defined as 0V.

4. Subject to I_{OUT} and power dissipation limitations.

5. Absolute maximum ratings, as detailed in this table, are the ratings beyond which the device's performance may be impaired and/or permanent damage to the device may occur.

Table 4. Recommended Operating Conditions⁴

Symbol	Parameter	Min	Typ	Max	Units	Notes
T _C	Case Operating Temperature	0		85	°C	1,3
V _{CC}	Supply Voltage	4.5		5.5	V	
V _{EE}	Supply Voltage	-5.5		-4.5	V	
V _{TT}	Load Termination Supply Voltage		-2.0		V	2
R _{LOAD}	Output Termination Load Resistance		50		Ω	2
Θ _{JC}	Thermal Resistance Junction to Case			2	°C/W	

Notes: 1. T_C measured at case top. Use of adequate heatsink is required.

2. The V_{TT} and R_{LOAD} combination is subject to maximum output current and power restrictions.

3. Contact the Factory for extended temperature range applications.

4. Functionality and/or adherence to electrical specifications is not implied when the device is subjected to conditions that exceed, singularly or in combination, the operating range specified.

Table 5. DC Characteristics^{1,2} – Within recommended operating conditions, unless otherwise indicated.

Symbol	Parameter	Min	Max	Units	Test Cond.	Notes
V _{IH}	ECL Input Voltage High	-1100	-500	mV		
V _{IL}	ECL Input Voltage Low	V _{TT}	-1500	mV		
I _{IH}	ECL Input Current High		+30	μA	V _{IH} = -0.7 V	
I _{IL}	ECL Input Current Low		-30	μA	V _{IL} = -2.0 V	
V _{ICM}	ECL Input Common Mode Voltage	-1500	-1100	mV		
V _{IDIF}	ECL Input Differential Voltage (pk-pk)	400	1200	mV		
V _{IH}	CMOS/TTL Input Voltage High	3.5/2.0	V _{CC} /V _{CC}	V		2
V _{IL}	CMOS/TTL Input Voltage Low	0/0	1.5/0.8	V		2
I _{IH}	CMOS/TTL Input Current High		+100	μA	V _{IH} = V _{CC}	2
I _{IL}	CMOS/TTL Input Current Low		-100	μA	V _{IL} = 0 V	2
V _{OCM}	ECL Output Common Mode	-1500	-1100	mV		
V _{ODIF}	ECL Output Differential Voltage	600		mV		
V _{OH}	ECL Output Voltage High	-1000	-600	mV		
V _{OL}	ECL Output Voltage Low	V _{TT}	-1600	mV		
I _{OH}	ECL Output Current High	20	27	mA		
I _{OL}	ECL Output Current Low	0	8	mA		
I _{CC}	Power Supply Current (+)		20	mA		
I _{EE}	Power Supply Current (-)		-1950	mA		

Notes: 1. Test conditions unless otherwise indicated: V_{TT} = -2.0 V, R_{LOAD} = 50 Ω to V_{TT}.
 2. Input level is selected by the CNTRL_LVL input. Tying CNTRL_LVL to GND selects TTL levels, leaving CNTRL_LVL OPEN selects CMOS levels.

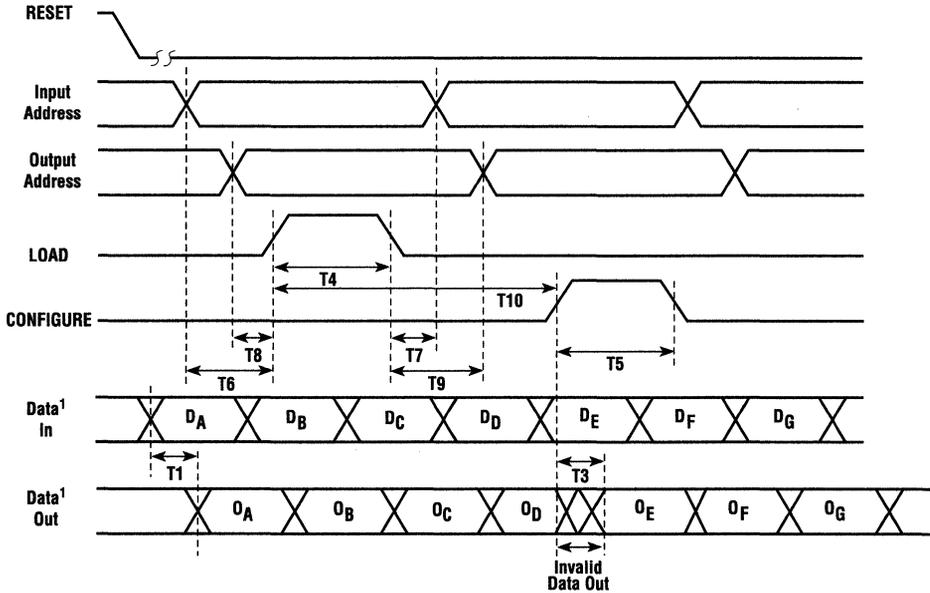
Table 6. AC Characteristics¹ – Within recommended operating conditions, unless otherwise indicated.

Symbol	Parameter	Min	Typ	Max	Units	Notes
	Maximum Data Rate/Port			800	Mb/s	1,2
	Jitter			150	ps pk-pk	1
T ₁	Channel Propagation Delay			2300	ps	
T ₂	Channel-to-Channel Delay Skew			500	ps	
T ₃	CONFIG to Data Out (O _i) Delay			5	ns	
T ₄	LOAD Pulse Width	7			ns	
T ₅	CONFIG Pulse Width	7			ns	
T ₆	IA _i to LOAD High Setup Time	0			ns	
T ₇	LOAD to IA _i Low Hold Time	3			ns	
T ₈	OAI to LOAD High Setup Time	0			ns	
T ₉	LOAD to OAI Low Hold Time	3			ns	
T ₁₀	Load ↑ to CONFIG ↑	0			ns	
T ₁₁	RESET Pulse Width	10			ns	
T _{R,F}	Output Rise or Fall Time		300	400	ps	3

Notes: 1. Test conditions: V_{TT} = -2.0 V, R_{LOAD} = 50 Ω to V_{TT}; ECL inputs: V_{IH} = -1.1 V; V_{IL} = -1.5 V; CMOS inputs: V_{IH} = 3.5 V, V_{IL} = 1.5 V; ECL outputs: V_{OH} = -1.0 V, V_{OL} = -1.6 V; ECL inputs rise and fall times 1 ns; CMOS inputs rise and fall times 20 ns. A bit error rate of 1E-13 BER or better for 2²³-1PRBS pattern, jitter and rise/fall times are guaranteed through characterization.
 2. 800 Mb/s Non-Return-Zero (NRZ) data equivalent to 400 MHz clock signal.
 3. Rise and fall times are measured at the 20% and 80% points of the transition from V_{OL} max to V_{OL} min.

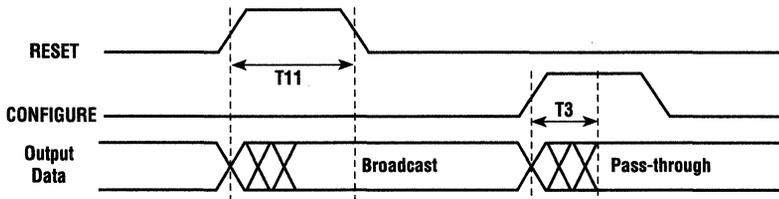
TQ8032

Figure 3. Timing Diagram – Switch Configuration



Note: 1. No data loss on unchanged paths

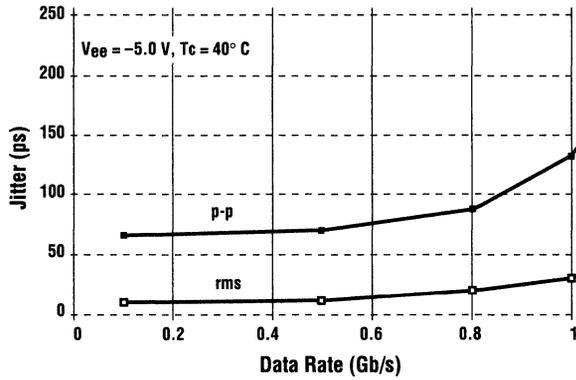
Figure 4. Timing Diagram – Reset



- Notes:
1. LOAD input must remain LOW to insure correct programming of the switch.
 2. "Broadcast" is defined as data input 0 to all data outputs (0..31).
 3. "Pass-through" is defined as data input 0 to data output 0, data input 1 to data output 1, etc.

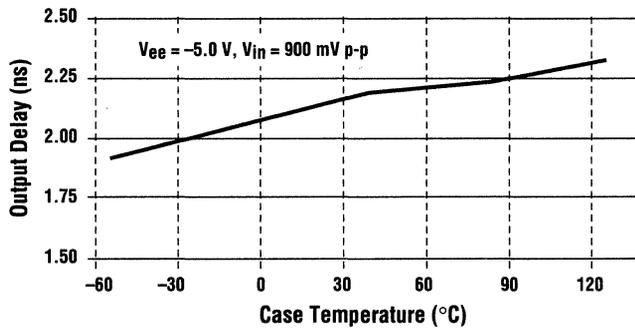
Typical Performance Data

Figure 5. Jitter – Single Channel



SWITCHING PRODUCTS

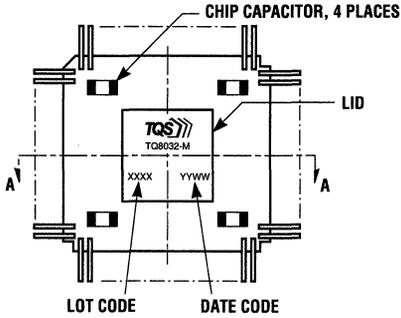
Figure 6. Output Delay



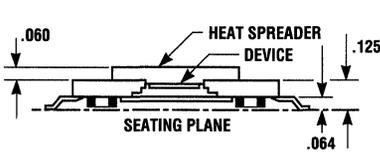
TQ8032

Figure 7. Mechanical Dimensions

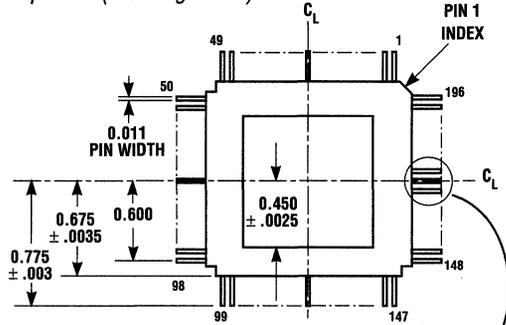
Bottom View (marking up)



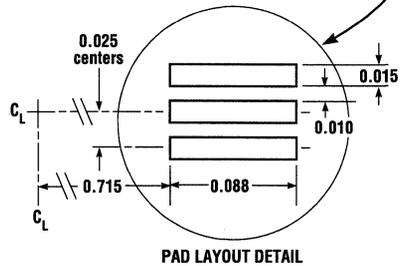
Section A-A



Top View (marking down)



1. Part is symmetrical about the center axes.
2. Centerline bisects center pin in both directions.
3. See pad detail below.



Ordering Information

TQ8032-M

800 Mb/s 32x32 ECL Crosspoint Switch

Additional Information

For latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com **Tel:** (503) 615-9000
Email: sales@tqs.com **Fax:** (503) 615-8900

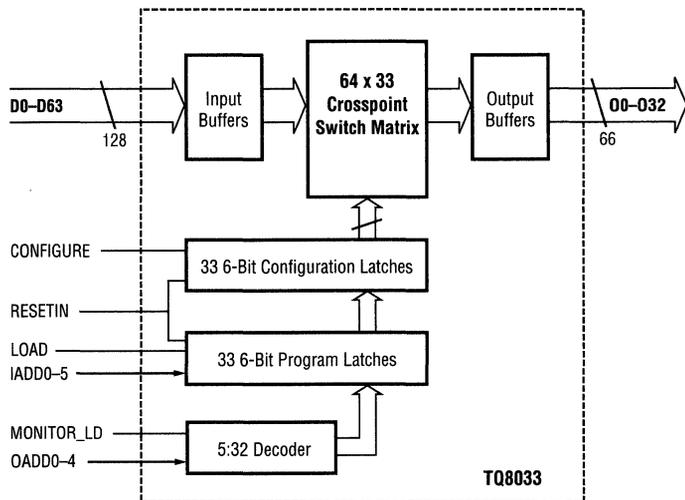
For technical questions and additional information on specific applications:

Email: applications@tqs.com

The information provided herein is believed to be reliable; TriQuint assumes no liability for inaccuracies or omissions. TriQuint assumes no responsibility for the use of this information, and all such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. TriQuint does not authorize or warrant any TriQuint product for use in life-support devices and/or systems.

Copyright © 1997 TriQuint Semiconductor, Inc. All rights reserved.

Revision 1.0.A October 1997



The TQ8033 is a non-blocking 64 x 33 digital crosspoint switch capable of data rates greater than 1.5 Gigabits per second per port. Utilizing a fully differential internal data path and PECL I/O, the TQ8033 offers a high data rate with exceptional signal fidelity. The symmetrical switching and noise rejection characteristics inherent in differential logic result in low jitter and signal skew. The TQ8033 is ideally suited for digital video, data communications and telecommunication switching applications.

The non-blocking architecture uses 33 fully independent 64:1 multiplexers, allowing each output port to be independently programmed to any input port. Port O32 is provided to support diagnostic monitoring.

The switch is configured by sequentially addressing each output multiplexer (OADD0:4) and loading it's 6-bit program latch with the desired input port address (IADD0:5) and then enabling the LOAD pin. When complete, the CONFIGURE pin is strobed and all new configurations are simultaneously transferred into the switch multiplexers. Data integrity is maintained on all unchanged data paths.

TQ8033

PRELIMINARY DATA SHEET

1.5 Gbit/sec 64x33 Digital PECL Crosspoint Switch

Features

- >1.5 Gb/s/port data bandwidth;
>50 Gb/s aggregate bandwidth
- Fully differential data path with
64 inputs and 33 outputs
- Non-blocking architecture
- 150 ps delay match
- Differential PECL-level data I/O;
TTL-level control inputs
- Low jitter and signal skew
- Double-buffered
configuration latches
- Dedicated, programmable full-
bandwidth monitor output for
diagnostics
- 304-pin BGA package
- Single +5V supply

Applications

- Telecom/Datacomm switching
- Hubs and routers
- Video switching

TQ8033

PRELIMINARY DATA SHEET

Specifications

Specifications subject to change without notice.

Table 1. Absolute Maximum Ratings⁴

Parameter	Condition	Symbol	Minimum	Nominal	Maximum	Unit
Storage Temperature		T _{store}	-65		150	°C
Junction Temperature		T _{CH}	-65		150	°C
Case Temperature w/bias	(1)	T _C	0		85	°C
Supply Voltage	(2)	V _{DD}	0		7.0	V
Voltage to any input	(2)	V _{in}	-0.5		V _{DD} + 0.5	V
Voltage to any output	(2)	V _{out}	-0.5		V _{DD} + 0.5	V
Current to any input	(2)	I _{in}	-1.0		1.0	mA
Current from any output	(2)	I _{out}			40.0	mA
Power Dissipation of output	(3)	P _{out}			50.0	mW

Notes: 1. T_C is measured at case top.

2. All voltages are measured with respect to GND (0V) and are continuous.

3. P_{out} = (V_{DD} - V_{out}) X I_{out}.

4. Absolute maximum ratings, as detailed in this table, are the ratings beyond which the device's performance may be impaired and/or permanent damage to the device may occur.

Table 2. Recommended Operating Conditions⁴

Symbol	Parameter	Min	Typ	Max	Units	Notes
T _C	Case Operating Temperature	0	—	85	°C	1, 3
V _{DD}	Supply Voltage	4.75	—	5.25	V	
V _{TT}	Load Termination Supply Voltage		V _{DD} - 2.0		V	2
I _{DD}	Current positive supply	—	—	3	A	
R _{LOAD}	Output Termination Load Resistance		50		Ω	2
Θ _{JC}	Thermal Resistance Junction to Case			4	°C/W	

Notes: 1. T_C measured at case top. Use of adequate heatsink is required.

2. The V_{TT} and R_{LOAD} combination is subject to maximum output current and power restrictions.

3. Contact the Factory for extended temperature range applications.

4. Functionality and/or adherence to electrical specifications is not implied when the device is subjected to conditions that exceed, singularly or in combination, the operating range specified.

Table 3. DC Characteristics—ECL/PECL I/O ^{4,5}

Parameter	Condition	Symbol	Minimum	Nominal	Maximum	Unit
Common mode voltage	(1)	V _{COM}	V _{DD} - 1500	—	V _{DD} - 1100	mV
Differential voltage	(1)	V _{DIFF}	400	—	1200	mV
Input HIGH voltage		V _{IH}		—	V _{DD} - 500	mV
Input LOW voltage		V _{IL}	V _{DD} - 2100	—		mV
Output HIGH voltage	(3)	V _{OH}	V _{DD} - 1000		V _{DD} - 600	mV
Output LOW voltage	(3)	V _{OL}	V _{DD} - 2100	—	V _{DD} - 1600	mV
Output HIGH current	(3)	I _{OH}	20	23	30	mA
Output LOW current	(3)	I _{OL}	0	5	8	mA
Input capacitance		C _{IN}	—	—	TBD	pF
Output capacitance		C _{OUT}	—	—	TBD	pF
ESD breakdown rating		V _{ESD}	Class I	—	—	

Table 4. DC Characteristics—TTL I/O ^{4,5}

Parameter	Condition	Symbol	Minimum	Nominal	Maximum	Unit
Input HIGH voltage		V _{IH}	2.0	—	V _{DD}	V
Input LOW voltage		V _{IL}	0	—	0.8	V
Input HIGH current	V _{IH(MAX)}	I _{IH}	—	—	200	μA
Input LOW current	V _{IL(MIN)}	I _{IL}	-400	-200	—	μA
Input capacitance		C _{IN}	—	—	TBD	pF
Output capacitance		C _{OUT}	—	—	TBD	pF
ESD breakdown rating		V _{ESD}	Class I	—	—	

Notes (Tables 3 and 4):

1. Differential inputs.
2. V_{REF} = 1300 mV.
3. R_{LOAD} = 50 ohms to V_{TT} = V_{DD} - 2.0V.
4. Specifications apply over recommended operating ranges.
5. Inputs are DC-biased to V_{DD} - 1.3V with 4 kΩ Thevenin input impedance.

TQ8033

PRELIMINARY DATA SHEET

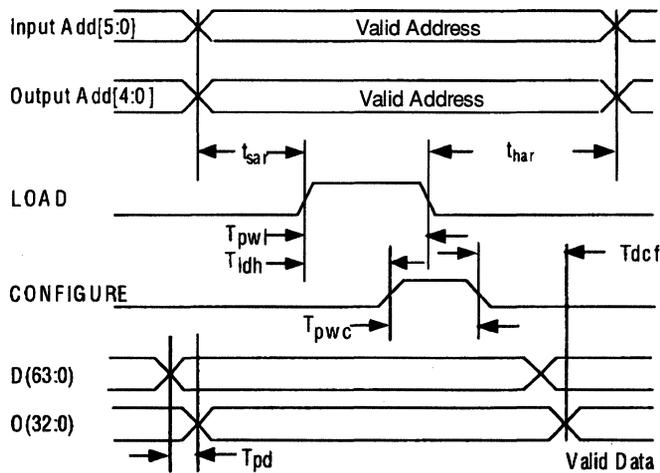
Table 5. AC Characteristics

Parameter	Condition	Symbol	Minimum	Nominal	Maximum	Unit
Data Rate/port			1.5			Gb/s
D0-63 minimum pulse width	(1)	T_{pw}	670	—	—	ps
O0-32 Rise/Fall time 20-80%	(1)	$T_{r/f}$	—	—	300	ps
Channel Propagation Delay (mean)	(1)	T_{pd}	—	—	2.5	ns
Ch-to-Ch Propagation Delay Skew	(1)	T_{skew}	—	—	150	ps
O0-32 Jitter	(2)	T_{jitter}	—	70	150	ps

Notes: 1. Min. V_{OH} to max V_{OL} levels

2. Crossing of (On)-(NO) measured with $2^{23}-1$ PRBS, measured over extended time.

Figure 1. TQ8033 Timing Diagram

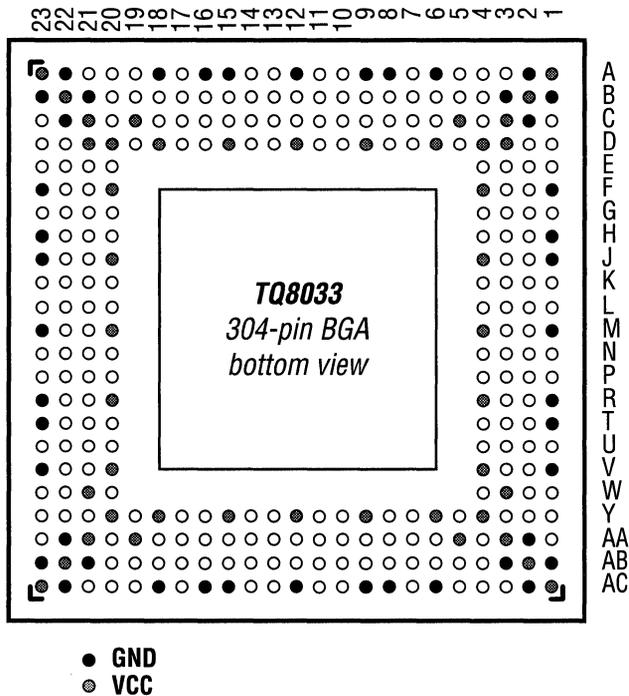


Note: No data loss on unchanged paths.

Table 6. Timing Specifications

Symbol	Parameter	Minimum	Maximum	Unit
t_{sar}	Address to Write Set-up time	10		ns
t_{har}	Address to Write Hold Time	5		ns
t_{pwl}	Min. Load pulse width	7		ns
t_{idh}	Load to Configure delay	0		ns
t_{pwc}	Min. Configure pulse width	7		ns
t_{dcf}	Configure to Data Valid		5	ns
t_{pd}	Data propagation delay		2.5	ns

Figure 2. TQ8033 Pinout —Bottom View



SWITCHING PRODUCTS

Table 7. TQ8033 Pin Descriptions

Signal	Type	Pin No.	Grid Ref.	Description
RESETIN	TTL Input	162	E20	The active high chip level reset signal initializes all internal chip circuitry to a known state.
LOAD	TTL Input	161	C23	Latch control for program data. LOAD enabled allows latches to take in new program data for a given output MUX.
CONFIGURE	TTL Input	160	D22	Active high. Transfers configuration program data from program registers into the configure registers and multiplexers. If the configuration does not change, the data path will not be disturbed with CONFIGURE going active.
IADD0	TTL Input	159	E21	Input address LSB. This is the program data which sets which input an output is to be connected to.
IADD1	TTL Input	158	D23	Input address.
IADD2	TTL Input	157	E22	Input address.
IADD3	TTL Input	156	F21	Input address.
IADD4	TTL Input	155	G20	Input address.
IADD5	TTL Input	154	E23	Input address MSB.
OADD0	TTL Input	153	F22	Output address LSB. This is the address data which specifies which output is to be programmed.

(Continued on next page)

TQ8033**PRELIMINARY DATA SHEET****Table 7. TQ8033 Pin Descriptions (cont.)**

Signal	Type	Pin No.	Grid Ref.	Description
OADD1	TTL Input	152	G21	Output address.
OADD2	TTL Input	151	H20	Output address.
OADD3	TTL Input	150	G22	Output address.
OADD4	TTL Input	149	H21	Output address MSB.
VCS2_BIAS	Input	2	C1	Used for internal biasing. Do not connect.
MONITOR_LD	TTL Input	1	E4	Directly loads the Monitor output port for programming. The OADD bus and the LOAD pin are not used to program this port. Once this pin is enabled, the data on the IADD port is held in the program register for the monitor output. The CONFIGURE signal enables the program data for this port (as well as for all the others).
D0, ND0	PECL Input	163, 164	C20, D19	High-speed input and complement. D0 and ND0 are addressed by IADD = "000000"; D63 and ND63 are addressed by IADD = "111111".
D1, ND1	PECL Input	165, 166	A21, B20	High-speed input and complement.
D2, ND2	PECL Input	167, 168	A20, B19	High-speed input and complement.
D3, ND3	PECL Input	169, 170	C18, D17	High-speed input and complement.
D4, ND4	PECL Input	171, 172	A19, B18	High-speed input and complement.
D5, ND5	PECL Input	173, 174	C17, D16	High-speed input and complement.
D6, ND6	PECL Input	175, 176	B17, A17	High-speed input and complement.
D7, ND7	PECL Input	177, 178	C16, B16	High-speed input and complement.
D8, ND8	PECL Input	179, 180	C15, B15	High-speed input and complement.
D9, ND9	PECL Input	181, 182	D14, C14	High-speed input and complement.
D10, ND10	PECL Input	183, 184	B14, A14	High-speed input and complement.
D11, ND11	PECL Input	185, 186	D13, C13	High-speed input and complement.
D12, ND12	PECL Input	187, 188	B13, A13	High-speed input and complement.
D13, ND13	PECL Input	189, 190	C12, B12	High-speed input and complement.
D14, ND14	PECL Input	191, 192	A11, B11	High-speed input and complement.
D15, ND15	PECL Input	193, 194	C11, D11	High-speed input and complement.
D16, ND16	PECL Input	195, 196	A10, B10	High-speed input and complement.
D17, ND17	PECL Input	197, 198	C10, D10	High-speed input and complement.
D18, ND18	PECL Input	199, 200	B9, C9	High-speed input and complement.
D19, ND19	PECL Input	201, 202	B8, A7	High-speed input and complement.
D20, ND20	PECL Input	205, 206	D8, C7	High-speed input and complement.
D21, ND21	PECL Input	207, 208	B6, A5	High-speed input and complement.
D22, ND22	PECL Input	209, 210	D7, C6	High-speed input and complement.
D23, ND23	PECL Input	211, 212	B5, A4	High-speed input and complement.
D24, ND24	PECL Input	213, 214	B4, A3	High-speed input and complement.
D25, ND25	PECL Input	215, 216	D5, C4	High-speed input and complement.
D26, ND26	PECL Input	3, 4	D2, E3	High-speed input and complement.
D27, ND27	PECL Input	5, 6	D1, E2	High-speed input and complement.
D28, ND28	PECL Input	7, 8	F3, G4	High-speed input and complement.
D29, ND29	PECL Input	9, 10	E1, F2	High-speed input and complement.

(Continued on next page)

Table 7. TQ8033 Pin Descriptions (cont.)

Signal	Type	Pin No.	Grid Ref.	Description
D30, ND30	PECL Input	11, 12	G3, H4	High-speed input and complement.
D31, ND31	PECL Input	13, 14	G2, G1	High-speed input and complement.
D32, ND32	PECL Input	49, 50	W2, Y1	High-speed input and complement.
D33, ND33	PECL Input	51, 52	Y2, AA1	High-speed input and complement.
D34, ND34	PECL Input	53, 54	W4, Y3	High-speed input and complement.
D35, ND35	PECL Input	55, 56	AA4, Y5	High-speed input and complement.
D36, ND36	PECL Input	57, 58	AC3, AB4	High-speed input and complement.
D37, ND37	PECL Input	59, 60	AC4, AB5	High-speed input and complement.
D38, ND38	PECL Input	61, 62	AA6, Y7	High-speed input and complement.
D39, ND39	PECL Input	63, 64	AC5, AB6	High-speed input and complement.
D40, ND40	PECL Input	65, 66	AA7, Y8	High-speed input and complement.
D41, ND41	PECL Input	67, 68	AB7, AC7	High-speed input and complement.
D42, ND42	PECL Input	69, 70	AA8, AB8	High-speed input and complement.
D43, ND43	PECL Input	71, 72	AA9, AB9	High-speed input and complement.
D44, ND44	PECL Input	73, 74	Y10, AA10	High-speed input and complement.
D45, ND45	PECL Input	75, 76	AB10, AC10	High-speed input and complement.
D46, ND46	PECL Input	77, 78	Y11, AA11	High-speed input and complement.
D47, ND47	PECL Input	79, 80	AB11, AC11	High-speed input and complement.
D48, ND48	PECL Input	81, 82	AA12, AB12	High-speed input and complement.
D49, ND49	PECL Input	83, 84	AC13, AB13	High-speed input and complement.
D50, ND50	PECL Input	85, 86	AA13, Y13	High-speed input and complement.
D51, ND51	PECL Input	87, 88	AC14, AB14	High-speed input and complement.
D52, ND52	PECL Input	89, 90	AA14, Y14	High-speed input and complement.
D53, ND53	PECL Input	91, 92	AB15, AA15	High-speed input and complement.
D54, ND54	PECL Input	93, 94	AB16, AC17	High-speed input and complement.
D55, ND55	PECL Input	97, 98	Y16, AA17	High-speed input and complement.
D56, ND56	PECL Input	99, 100	AB18, AC19	High-speed input and complement.
D57, ND57	PECL Input	101, 102	Y17, AA18	High-speed input and complement.
D58, ND58	PECL Input	103, 104	AB19, AC20	High-speed input and complement.
D59, ND59	PECL Input	105, 106	AB20, AC21	High-speed input and complement.
D60, ND60	PECL Input	107, 108	Y19, AA20	High-speed input and complement.
D61, ND61	PECL Input	109, 110	Y21, W20	High-speed input and complement.
D62, ND62	PECL Input	111, 112	AA23, Y22	High-speed input and complement.
D63, ND63	PECL Input	113, 114	Y23, W22	High-speed input and complement.
Not Connected		41	T3	
Not Connected		42	U2	
Not Connected		95	AA16	
Not Connected		96	AB17	
Not Connected		203	C8	
Not Connected		204	B7	

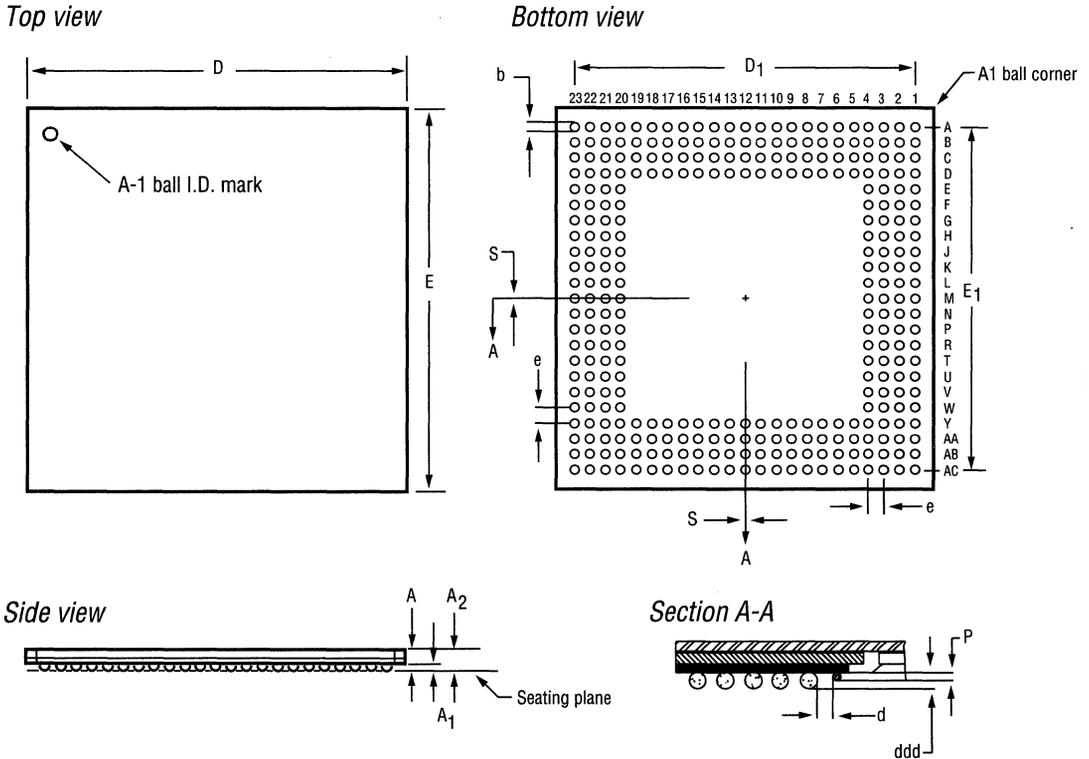
(Continued on next page)

TQ8033
PRELIMINARY DATA SHEET

Table 7. TQ8033 Pin Descriptions (cont.)

Signal	Type	Pin No.	Grid Ref.	Description
O0, NO0	PECL Output	15, 16	H3, H2	High-speed output and complement. O0 and NO0 are addressed by OADD = "00000". O31 and NO31 are addressed by OADD = "11111".
O1, NO1	PECL Output	17, 18	J3, J2	High-speed output and complement.
O2, NO2	PECL Output	19, 20	K4, K3	High-speed output and complement.
O3, NO3	PECL Output	21, 22	K2, K1	High-speed output and complement.
O4, NO4	PECL Output	23, 24	L4, L3	High-speed output and complement.
O5, NO5	PECL Output	25, 26	L2, L1	High-speed output and complement.
O6, NO6	PECL Output	27, 28	M3, M2	High-speed output and complement.
O7, NO7	PECL Output	29, 30	N1, N2	High-speed output and complement.
O8, NO8	PECL Output	31, 32	N3, N4	High-speed output and complement.
O9, NO9	PECL Output	33, 34	P1, P2	High-speed output and complement.
O10, NO10	PECL Output	35, 36	P3, P4	High-speed output and complement.
O11, NO11	PECL Output	37, 38	R2, R3	High-speed output and complement.
O12, NO12	PECL Output	39, 40	T2, U1	High-speed output and complement.
O13, NO13	PECL Output	43, 44	T4, U3	High-speed output and complement.
O14, NO14	PECL Output	45, 46	V2, W1	High-speed output and complement.
O15, NO14	PECL Output	47, 48	U4, V3	High-speed output and complement.
O16, NO16	PECL Output	145, 146	J22, J21	High-speed output and complement.
O17, NO17	PECL Output	143, 144	K21, K20	High-speed output and complement.
O18, NO18	PECL Output	141, 142	K23, K22	High-speed output and complement.
O19, NO19	PECL Output	139, 140	L21, L20	High-speed output and complement.
O20, NO20	PECL Output	137, 138	L23, L22	High-speed output and complement.
O21, NO21	PECL Output	135, 136	M21, M22	High-speed output and complement.
O22, NO22	PECL Output	133, 134	N22, N23	High-speed output and complement.
O23, NO23	PECL Output	131, 132	N20, N21	High-speed output and complement.
O24, NO24	PECL Output	129, 130	P22, P23	High-speed output and complement.
O25, NO25	PECL Output	127, 128	P20, P21	High-speed output and complement.
O26, NO26	PECL Output	125, 126	R21, R22	High-speed output and complement.
O27, NO27	PECL Output	123, 124	T21, T22	High-speed output and complement.
O28, NO28	PECL Output	121, 122	U22, U23	High-speed output and complement.
O29, NO29	PECL Output	119, 120	U21, T20	High-speed output and complement.
O30, NO30	PECL Output	117, 118	W23, V22	High-speed output and complement.
O31, NO31	PECL Output	115, 116	V21, U20	High-speed output and complement.
O32, NO32	PECL Output	147, 148	H22, G23	High-speed monitor output and complement.

Figure 3. TQ8033 BGA Mechanical Dimensions



SWITCHING
PRODUCTS

Table 8. TQ8033 BGA Dimensions (in millimeters)

Symbol	Parameter	Min.	Nom.	Max.
A	Overall thickness	1.41	1.54	1.67
A ₁	Ball Height	0.56	0.63	0.70
A ₂	Body thickness	0.85	0.91	0.97
D	Body size	30.90	31.00	31.10
D ₁	Ball footprint	27.84	27.94	28.04
E	Body size	30.90	31.00	31.10
E ₁	Ball footprint	27.84	27.94	28.04
b	Ball diameter	0.60	0.75	0.90
d	Distance encapsulation to balls		0.6	
e	Ball pitch		1.27	
ddd	Seating plane clearance	0.15	0.30	0.35
P	Encapsulation height	0.20	0.30	0.35
S	Solder ball placement	—	—	0.00

TQ8033

PRELIMINARY DATA SHEET

Ordering Information

TQ8033

1.5 Gbit/sec 64x33 PECL Crosspoint Switch

Additional Information

For latest specifications, additional product information,
worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com Tel: (503) 615-9000

Email: sales@tqs.com Fax: (503) 615-8900

For technical questions and additional information on specific applications:

Email: applications@tqs.com

The information provided herein is believed to be reliable; TriQuint assumes no liability for inaccuracies or omissions. TriQuint assumes no responsibility for the use of this information, and all such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. TriQuint does not authorize or warrant any TriQuint product for use in life-support devices and/or systems.

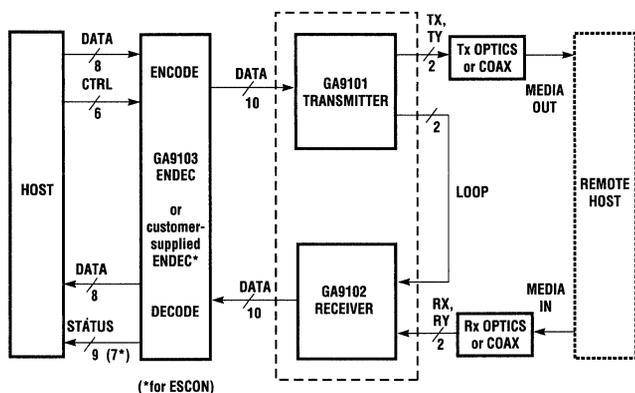
Copyright © 1997 TriQuint Semiconductor, Inc. All rights reserved.

Revision 0.1.A October 1997



Section 4 — Data Communications Products

<i>GA9101/9102</i> Transmitter/Receiver	4-3
<i>GA9103</i> Transmitter/Receiver	4-17
<i>TQ9303</i> Fibre Channel Encoder/Decoder	4-35
<i>TQ9501/9502</i> FC531/1063 Transmitter/Receiver	4-61
<i>TQ9525</i> 2.5 Gb/s 20-bit Transceiver	4-77



TriQuint's GA9101 Transmitter and GA9102 Receiver, in conjunction with the GA9103 ENDEC, provide a comprehensive electrical and physical interface in compliance with the ANSI Fibre Channel Standard. In conjunction with a customer-supplied ENDEC, the GA9101 and GA9102 also provide a fully-compliant interface with the ESCON™ standard. The GA9101/GA9102 chip set can also be used for local-area network applications operating at serial data rates of 194.4 Megabaud (payload at 155.52 Megabits/sec).

The Fibre Channel Specification is implemented as a standard I/O channel interface for either serial interconnection of peripherals to computers or for communication between computers. Fibre Channel links communicate over distances of up to 10 kilometers at baud rates from 132.8125 Megabaud to 1.0625 Gigabaud. GA9101 and GA9102 chips are designed to operate at serial baud rates of 194.4, 200.0, and 265.625 Megabaud.

The Fibre Channel standard provides a variety of physical media and data rates to accommodate different cost/performance needs. The framing protocol also provides flexibility, so different implementations can use various features of the standard to optimize system performance. GA9101 and GA9102 Transmitter/Receiver chips are designed using a TriQuint-proprietary 0.7 micron One-Up™ GaAs process. They interface either directly to an electrical medium or to a fiber-optic interface. The chips perform parallel-to-serial conversion, bit clock generation, receive clock/data recovery, and serial-to-parallel conversion.

Along with a fiber-optic module, this chip set will provide a complete FC-0 and FC-1 solution for a Fibre Channel data link. Additionally, the GA9101 and GA9102 can be used for serial SCSI, point-to-point serial communication, and other network applications.

GA9101/ GA9102

Fibre Channel Transmitter and Receiver

Features

- Fully Fibre-Channel- and ESCON™-compatible
- With fiber optics and ENDEC, makes a complete FC-0, FC-1 solution
- TTL-compatible 10-bit-wide data bus with 19.44, 20.00, or 26.5625 MHz byte clock
- Serial rate of 194.4, 200.0, or 265.625 Mbaud with on-chip bit clock generation
- On-chip clock and data-recovery PLL
- Automatic byte alignment to 8b/10b code
- Low power dissipation — 700 mW per chip (typical)
- 28-pin surface-mount package

The ESCON I/O interface provides an optical-fiber communication link between I/O devices and main storage of IBM or compatible computers implementing Enterprise Systems Architecture/390™ (ESA/390™). A customer-supplied ENDEC completes the interface by implementing the data and control encoding/decoding functions of the ESCON standard, and typically also provides CRC and parity generate/check functions.

The 10-bit data bus of the GA9101 and GA9102 chips interfaces with the GA9103 CMOS ENDEC chip, which provides data, ordered-set, and line-state encoding and decoding functions described in the Fibre Channel Physical Layer standard (FC_PH). In addition, it performs 32-bit CRC and parity generate/check functions.

Functional Description – GA9101 Transmitter

The XMT PLL block synthesizes the reference bit clock, XBITCLK, which is derived from the transmit clock input, TXCLK. The frequency of TXCLK is 19.44, 20.00, or 26.5625 MHz, which is multiplied by 10 through an internal Phase-Locked Loop to obtain an XBITCLK of 194.4, 200.0, or 265.625 MHz, respectively. The XBITCLK provides the bit timing to the transmit path.

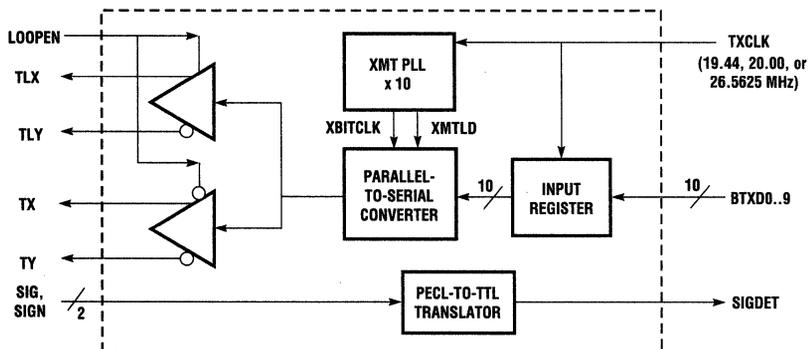
This data is then serialized using the XBITCLK from the PLL block. During serialization, the most-significant bit, BTXD9, is transmitted first, followed by BTXD8 . . . BTXD0. The serial data is sent out using the differential PECL driver. The LOOPEN input signal selects the transmit output as shown in the table. The unselected differential outputs are forced to a logic LOW state.

The INPUT REGISTER loads the 10-bit-wide input data, BTXD0..9, from the ENDEC on the positive edge of TXCLK. It sends the data out to the PARALLEL-TO-SERIAL block.

The SIG and SIGN differential PECL signals originate from the optical receiver and, when active, indicate the presence of input optical signals. SIGDET is an active-HIGH TTL signal derived from SIG and SIGN, through the PECL-to-TTL TRANSLATOR.

The XMTLD signal strobes the 10-bit-wide data into the PARALLEL-TO-SERIAL CONVERTER functional block.

Figure 1. GA9101 Transmitter



As required by the Fibre Channel standard, the GA9101/ GA9102 provide a Loopback mode for a system test at speed. When LOOPEN = 1, the TLX and TLY outputs of the GA9101 are enabled and are transmitted to the RLX and RLY inputs of the local receiver. In the normal mode (LOOPEN = 0), the TX and TY outputs of the transmitter are enabled.

Functional Description – GA9102 Receiver

The MUX block receives its inputs from the RX, RY differential inputs and the looped transmit outputs connected to RLX and RLY. Its output goes to the CLOCK/DATA RECOVERY block. The MUX output is selected by the LOOPEN pin as outlined in Table 2.

Table 2. Clock Recovery Input Selection

LOOPEN	MUX Output
0	RX, RY
1	RLX, RLY

The CLOCK/DATA RECOVERY (CDR) circuit recovers the clock information from the input data at serial transmission rates of 194.4, 200.0, or 265.625 Megabaud. The CDR block uses the REFCLK to aid in frequency acquisition of the recovered clock, called CLOCK, which is then used to retime the data,

Figure 2. GA9102 Receiver

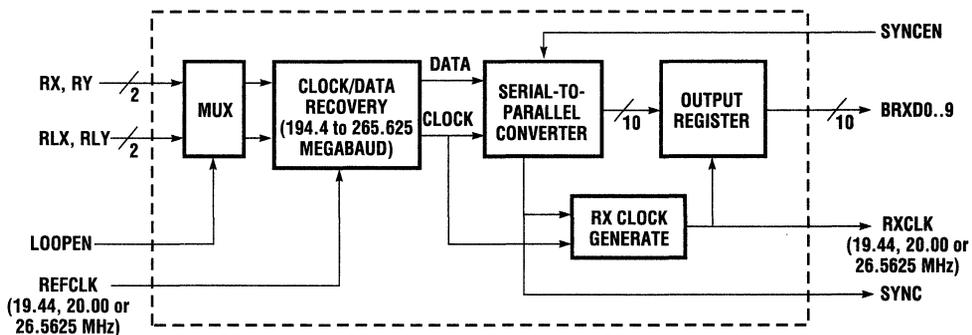


Table 3. Transmit Output Selection

LOOPEN	Tx Output
0	TX, TY
1	TLX, TLY

removing any jitter components. If REFCLK is present, the initial receiver bit-synchronization time to valid incoming data is less than 200 microseconds. The receiver is guaranteed to have valid outputs 1 ms after valid REFCLK and serial data are applied. Once synchronized, if a phase discontinuity occurs in the incoming data, the receiver resynchronizes in less than 2500 bit times, (with 95% probability).

The recovered data is converted to a 10-bit data word by the SERIAL-TO-PARALLEL CONVERTER (SPC) logic. The CLOCK signal is used by the SPC and the RX CLOCK GENERATE blocks to provide the necessary bit timing.

The SERIAL-TO-PARALLEL CONVERTER block does the serial-to-parallel conversion. The parallel conversion is to 10 bits, which corresponds to the

**DATACOM
PRODUCTS**

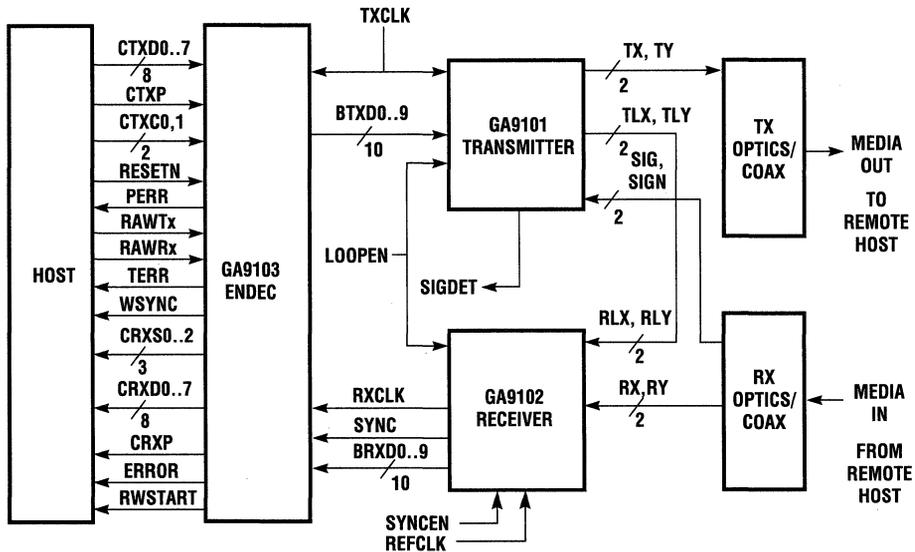
GA9101/9102

undecoded byte output of the 8b/10b coding scheme. The output of this block is sent to the OUTPUT REGISTER. The SPC also generates the SYNC signal upon receipt of a K28.5 byte, (001111 1010 or 110000 0101), provided the SYNCEN pin is HIGH. The SYNC signal is always LOW if SYNCEN is inactive. When the SYNCEN signal is LOW, the device retains the previous alignment for the incoming K28.5 byte. The SYNCEN signal is useful when the host decides to disable byte alignment to the incoming K28.5. Using this pin, the host may decide to align only under certain circumstances, such as power up or loss of word synchronization (see the GA9103 ENDEC data sheet). The SYNCEN pin can also be of use in non-Fibre-Channel applications where byte alignment to a different pattern may be done by the interfacing logic.

The RX CLOCK GENERATE block is used to generate the Receive Byte Clock, RXCLK. RXCLK is 19.44, 20.00, or 26.5625 MHz, corresponding to the serial baud rate of 194.4, 200.0, or 265.625 Megabaud, respectively. The RXCLK is realigned synchronous to the SYNC signal from the SERIAL-TO-PARALLEL CONVERTER. On power up, the RXCLK provides arbitrary alignment for the incoming data until the arrival of the first K28.5 byte while SYNCEN is HIGH.

The OUTPUT REGISTER takes in the 10-bit-wide output from the SERIAL-TO-PARALLEL CONVERTER block and generates output data BRXD0..9. BRXD0..9 interfaces to the ENDEC chip and can be strobed on the negative edge of RXCLK. The received bit sequence within each 10 bits of serial data is BRXD9 . . BRXD0.

Figure 3. System Block Diagram – Fibre Channel



Specifications

Figure 4. TTL Test Load, RXCLK

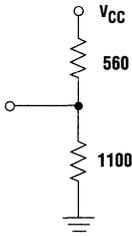


Figure 6. PECL Test Load

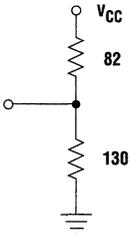


Figure 5. TTL Test Load, All Other TLL Outputs

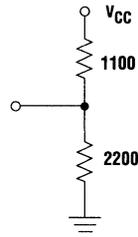


Table 4. Capacitance¹

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
C_{IN}	Input capacitance	$I_{IN} = 2.0 \text{ V}$ at $f = 1 \text{ MHz}$		6		pF
C_{OUT}	Output capacitance	$V_{OUT} = 2.0 \text{ V}$ at $f = 1 \text{ MHz}$		9		pF

Notes: 1. These parameters are not 100% tested, but are periodically sampled.

Table 5. Absolute Maximum Ratings¹

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
T_{storage}	Storage Temperature	-65		150		°C
T_{case}	Case Temperature	-55		125		°C
V_{CC}^1	Supply Voltage to ground	-0.5		7.0		V
V_I	DC Input voltage	-0.5		$V_{CC} + 0.5$		V
I_I	DC Input current	-30		+5		mA

Notes: 1. Exceeding the absolute maximum ratings may damage these devices.

Table 6. Operating Conditions¹

Parameter	Description	Min.	Typ.	Max.	Units
V _{CC}	Supply Voltage	5 (-5%)	5	5 (+5%)	V
T _A	Ambient Temperature	0		70	°C
I _{CC} ²	Power supply current		115	160	mA

Notes: 1. Proper functionality is guaranteed under these conditions.

2. With V_{CC} = Max, static.

DC Characteristics (Over operating range unless otherwise specified)

Table 7. GA9101 Transmitter TTL Signals (BTXDO..9, TXCLK, SIGDET, LOOPEN)

Symbol	Description	Test Conditions	Limits ¹			Unit
			Min.	Typ.	Max.	
V _{OH}	Output HIGH voltage	V _{CC} = Min I _{OH} = -1.6 mA V _{IN} ² = V _{IH} or V _{IL} I _{OH} = -3.2 mA ³	2.4	3.7		V
V _{OL}	Output LOW voltage	V _{CC} = Min I _{OL} = 4 mA V _{IN} ² = V _{IH} or V _{IL} I _{OL} = 8 mA ³		0.2	0.5	V
I _{SC} ⁴	Output short-circuit current	V _{CC} = Max V _{OUT} = 0.5 V	-15		-100	mA
I _{IL}	Input LOW current	V _{CC} = Max V _{IN} = 0.4 V			-400	µA
I _{IH}	Input HIGH current	V _{CC} = Max V _{IN} = 2.7 V			25	µA
I _I	Input HIGH current	V _{CC} = Max V _{IN} = 5.5 V			1	mA
V _{IH} ⁵	Input HIGH level	Guaranteed input logical HIGH voltage for all inputs	2.0			V
V _{IL} ⁵	Input LOW level	Guaranteed input logical LOW voltage for all inputs			0.8	V
V _I	Input clamp voltage	V _{CC} = Min I _{IN} = -18 mA			-1.2	V

Notes: 1. Typical limits are: V_{CC} = 5.0 V and T_A = 25 °C.

2. The TTL inputs could be high or low.

3. These are absolute values with respect to device ground.

4. No more than one output should be tested at a time. Duration of the short circuit should not exceed one second.

Table 8. GA9101 Transmitter PECL Signals (TX, TY, TLX, TLY, SIG, SIGN)

Symbol	Description	Test Conditions	Min.	Limits ¹		Unit
				Typ.	Max.	
I _{IL}	Input LOW current	V _{CC} = Max V _{IN} = 2.4 V	0.5			μA
I _{IH}	Input HIGH current	V _{CC} = Max V _{IN} = V _{CC} - 0.5 V			250	μA
V _{IHS}	Highest input HIGH voltage	V _{CC} = Max			V _{CC} - 0.50	V
V _{ILS}	Lowest input LOW voltage	V _{CC} = Min	2.4			V
V _{DIF}	Differential input voltage	V _{CC} = Min	0.4		1.2	V
V _{ICM}	Input common mode voltage	V _{CC} = Min	2.8		V _{CC} - 0.7	V
V _{OH}	Output HIGH voltage	V _{CC} = Min PECL load V _{CC} = V _{CC} - 1.025			V _{CC} - 0.5	V
V _{OL}	Output LOW voltage	V _{CC} = Min PECL load	V _{CC} = V _{CC} - 2.0		V _{CC} - 1.62	V
V _{CMO}	Output common mode voltage		V _{CC} - 1.6		V _{CC} - 1.2	V
DV _{OUT}	Output Differential voltage		0.75		1.2	V

Notes: 1. Typical limits are: V_{CC} = 5.0 V and T_A = 25°C.

2. The TTL inputs could be HIGH or LOW.

3. The RXCLK signal has an 8 mA I_{OL}. All other outputs have a 4 mA I_{OL}.

4. These are absolute values with respect to device ground.

5. No more than one output should be tested at a time. Duration of the short circuit should not exceed one second.

Table 9. GA9102 Receiver TTL Signals (BRXDO..9, RXCLK, SYNC, REFCLK, LOOPEN)

Symbol	Description	Test Conditions	Min.	Limits ¹		Unit
				Typ.	Max.	
V _{OH}	Output HIGH voltage	V _{CC} = Min I _{OH} = -1.6 mA V _{IN} ² = V _{IH} or V _{IL} = -3.2 mA ³	2.4	3.7		V
V _{OL}	Output LOW voltage	V _{CC} = Min I _{OL} = 4 mA V _{IN} ² = V _{IH} or V _{IL} = 8 mA ³		0.2	0.5	V
I _{SC} ⁵	Output short-circuit current	V _{CC} = Max V _{OUT} = 0.5 V	-15		-120	mA
I _{IL}	Input LOW current	V _{CC} = Max V _{IN} = 0.40 V			-400	μA
I _{IH}	Input HIGH current	V _{CC} = Max V _{IN} = 2.7 V			25	μA
I _I	Input HIGH current	V _{CC} = Max V _{IN} = 5.5 V			1	mA
V _{IH} ⁴	Input HIGH level	Guaranteed input logical HIGH voltage for all inputs	2.0			V
V _{IL} ⁴	Input LOW level	Guaranteed input logical LOW voltage for all inputs			0.8	V
V _I	Input clamp voltage	V _{CC} = Min I _{IN} = -18 mA			-1.2	V
I _{CC}	Power supply current	V _{CC} = Max		150	180	mA

Notes: 1. Typical limits are: V_{CC} = 5.0 V and T_A = 25°C.

2. The TTL inputs could be HIGH or LOW.

3. The RXCLK signal has an 8 mA I_{OL}. All other outputs have a 4 mA I_{OL}.

4. These are absolute values with respect to device ground.

5. No more than one output should be tested at a time. Duration of the short circuit should not exceed one second.

Table 10. GA9102 Receiver PECL Signals (RX, RY, RLX, RLY)

Symbol	Description	Test Conditions	Min.	Limits ¹		Unit
				Typ.	Max.	
I _{IL}	Input LOW current	V _{CC} = Max V _{IN} = 2.4 V	0.5			μA
I _{IH}	Input HIGH current	V _{CC} = Max V _{IN} = V _{CC} - 0.5 V			250	μA
V _{IHS}	Highest Input HIGH voltage	V _{CC} = Min			V _{CC} - 0.5	V
V _{ILS}	Lowest Input LOW voltage	V _{CC} = Max	2.4			V
V _{DIF}	Differential Input voltage	V _{CC} = Min	0.4		1.2	V
V _{ICM}	Input Common Mode voltage	V _{CC} = Min	2.8		V _{CC} - 0.7	V

- Notes: 1. Typical limits are: V_{CC} = 5.0 V and T_A = 25°C.
 2. The TTL inputs could be HIGH or LOW.
 3. These are absolute values with respect to device ground.
 4. No more than one output should be tested at a time. Duration of the short circuit should not exceed one second.

AC Specifications

Table 11. AC Specifications—GA9101 Transmitter

Parameter	Description	Min.	Typ.	Max.	Units
T ₁	BTXD0..9 Setup Time	2.50			ns
T ₂	BTXD0..9 Hold Time	2.50			ns
T ₃	TXCLK Pulse Width HIGH	15.00			ns
T ₄	TXCLK Pulse Width LOW	15.00			ns
T ₅ ¹	TXCLK Period (T)	37.30		52.00	ns
T ₆	TX, TY, TLX, TLY Rise Time	250		750	ps
T ₇	TX, TY, TLX, TLY Fall Time	250		750	ps
T ₈	TX ~ TY or TLX ~ TLY Skew			60	ps
T ₉ ²	TX, TY or TLX, TLY Output Jitter – Deterministic Jitter (DJ) – Random Jitter (RJ)			60 275	ps ps
T ₁₀	Propagation Delay SIG, SIGN to SIGDET			20	ns

- Notes: 1. TXCLK period = (10/ baud rate) ±0.01%, where baud rate is 194.4, 200.0, or 265.625 Mbaud.
 2. These numbers are measured single-ended, using the High Gain Method @ 25 MHz.
 3. The jitter numbers are for a BER of 10⁻¹².

Figure 7. Bus Timing—GA9101 Transmitter

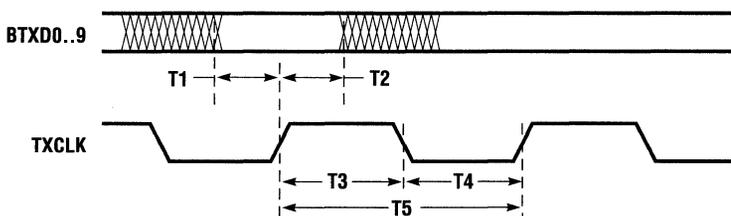


Figure 8. Serial Output Timing —GA9101

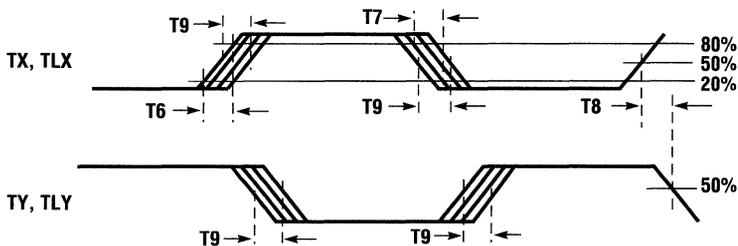
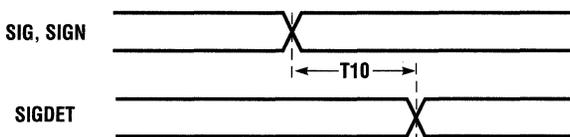


Figure 9. Serial Output Timing —GA9101



DATAKOM
PRODUCTS

Table 12. AC Specifications—GA9102 Receiver

Parameter	Description	Min.	Typ.	Max.	Units
T ₂₁	REFCLK Pulse width LOW	15.00			ns
T ₂₂	REFCLK Pulse width HIGH	15.00			ns
T ₂₃ ¹	REFCLK Period	37.30		52.00	ns
T ₂₄	BRXD0..9 Valid to RXCLK	T ₂₈ /5			ns
T ₂₅	BRXD0..9 Time from RXCLK	2.00			ns
T ₂₆	RXCLK Pulse width LOW	(T ₂₈ /2) - 2.50			ns
T ₂₇	RXCLK Pulse width HIGH	(T ₂₈ /2) - 2.50			ns
T ₂₈ ¹	RXCLK Period	37.30		52.00	ns
T ₂₉	SYNC Valid to RXCLK	T ₂₈ /5			ns
T ₃₀	SYNC Time from RXCLK	2.00			ns
T ₃₁ ²	RX, RY, RLX, RLY Rise time			1.50	ns
T ₃₂ ²	RX, RY, RLX, RLY Fall time			1.50	ns
T ₃₃	RX ~ RY or RX ~ RLY Skew			1.50	ns
T ₃₄	RX, RY, RLX, RLY, Peak-to-peak input jitter ³	0.07 * T ₂₈			ns

Notes: 1. REFCLK and RXCLK period = (10/baud rate) ±0.01%, where baud rate is 194.4, 200.0, or 265.625 Megabaud.
 2. Measured at V_{DIFF} = 0.4 V.
 3. The jitter numbers are for a BER of 10⁻¹².

Figure 10. Bus Timing—GA9102 Receiver

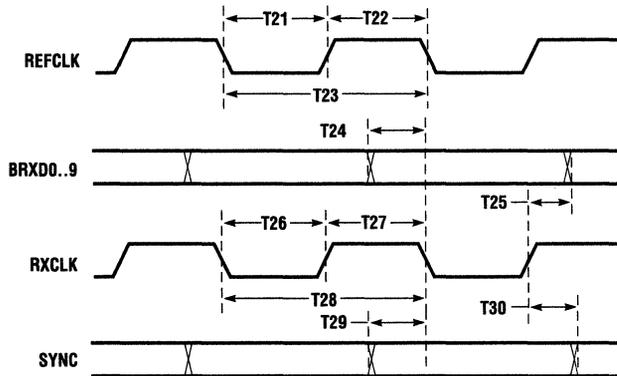
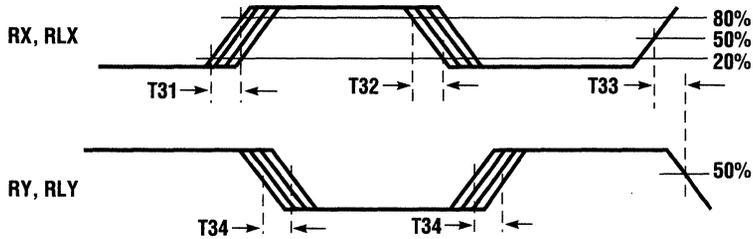


Table 13. Synchronization Times

<i>Description</i>	<i>Min.</i>	<i>Typ.</i>	<i>Max.</i>	<i>Units</i>
Power Up or application of REFCLK			1	ms
Application of valid data			200	μs
Resynchronization after phase shift on data			2500	bit times

Figure 11. Serial Input Timing —GA9102



DATACOM
 PRODUCTS

GA9101/9102

Pinouts

Figure 12. GA9101 and GA9102 Pinouts

The pinouts for the Transmitter and Receiver are arranged for easy interface to the ENDEC and optics.

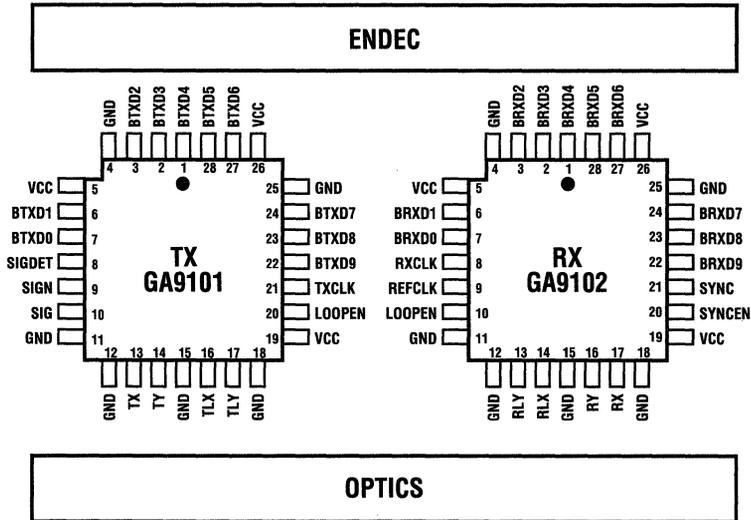


Table 14. GA9101 Pin Definitions

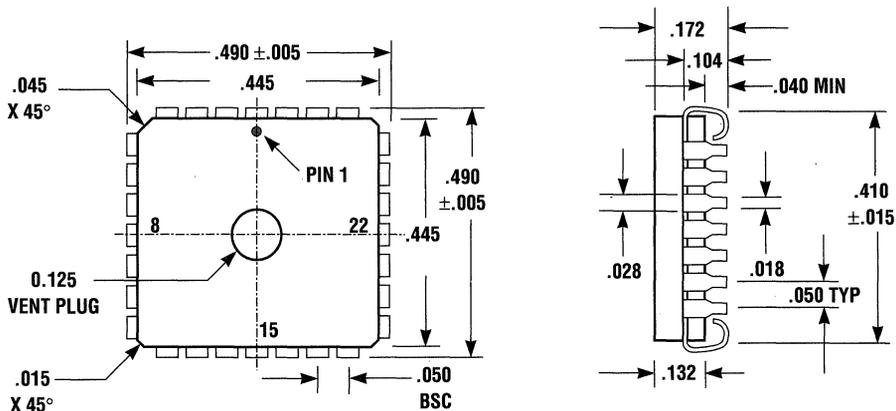
<i>Symbol</i>	<i>Pin #</i>	<i>I/O</i>	<i>Qty.</i>	<i>Logic Level</i>	<i>Active</i>	<i>Description</i>
TX, TY	13, 14	OUTPUT	2	PECL	NRZ	Differential Serial Data Output
TLX, TLY	16, 17	OUTPUT	2	PECL	NRZ	Diff. Serial Data Output, Loopback
SIGN, SIG	9, 10	INPUT	2	PECL	HIGH	Optical Signal Present
BTXDO..9	7, 6, 3-1, 28, 27, 24-22	INPUT	10	TTL	HIGH	Transmit Data Input
TXCLK	21	INPUT	1	TTL	HIGH	Transmit/PLL Reference Clock (19.44 to 26.5625 Mhz)
LOOPEN	20	INPUT	1	TTL	HIGH	Enable Loopback
SIGDET	8	OUTPUT	1	TTL	HIGH	Signal Detected
VCC	5, 19, 26	INPUT	3	N/A	N/A	+5 Volt Supply
GND	4, 11, 12, 15, 18, 25	INPUT	6	N/A	N/A	Ground

Table 15. GA9102 Pin Definitions

<i>Symbol</i>	<i>Pin #</i>	<i>I/O</i>	<i>Qty.</i>	<i>Logic Level</i>	<i>Active</i>	<i>Description</i>
RX, RY	17, 16	INPUT	2	PECL	NRZ	Differential Serial Data Input
RLX, RLY	14, 13	INPUT	2	PECL	NRZ	Diff. Serial Data Input, Loopback
BRXDO..9	7, 6, 3-1, 28, 27, 24-22	OUTPUT	10	TTL	HIGH	Receive Output Data
RXCLK	8	OUTPUT	1	TTL	HIGH	Receive Clock
SYNC	21	OUTPUT	1	TTL	HIGH	Receive Byte Sync
LOOPEN	10	INPUT	1	TTL	HIGH	Enable Loopback
REFCLK	9	INPUT	1	TTL	HIGH	Oscillator Clock (19.44 to 26.5625 MHz)
SYNCEN	20	INPUT	1	TTL	HIGH	Align to K28.5
VCC	5, 19, 26	INPUT	3	N/A	N/A	+5 Volt Supply
GND	4, 11, 12, 15, 18, 25	INPUT	6	N/A	N/A	Ground

Packaging

Figure 15. 28-Pin MQad J-leaded Package



Ordering Information

GA9101-2MC Transmitter
GA9102-2MC Receiver

Additional Information

For latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com Tel: (503) 615-9000
 Email: sales@tqs.com Fax: (503) 615-8900

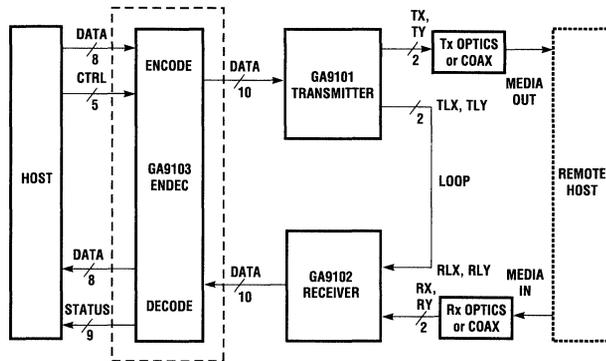
For technical questions and additional information on specific applications:

Email: applications@tqs.com

The information provided herein is believed to be reliable; TriQuint assumes no liability for inaccuracies or omissions. TriQuint assumes no responsibility for the use of this information, and all such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. TriQuint does not authorize or warrant any TriQuint product for use in life-support devices and/or systems.

Copyright © 1997 TriQuint Semiconductor, Inc. All rights reserved.

Revision 1.0.A October 1997



TriQuint's GA9103 is one of the three devices of the FC-265 chip set designed to support the requirements of Fibre Channel Standard X3T9.3. The GA9103 is an encoder/decoder (ENDEC) integrated circuit which implements the 8b/10b encoding/decoding scheme for data, ordered sets and line states associated with the Fibre Channel Physical Level Standard (FC-PH). In addition, the CMOS ENDEC chip performs 32-bit CRC and parity generate/check functions. It interfaces to TriQuint's GA9101 and GA9102 Transmitter and Receiver, respectively, and to either the fabric or the device link protocol controller.

The FC-265 (GA9101, GA9102 and GA9103) provides a comprehensive electrical and physical interface for Fibre Channel. These chips are designed to operate at 265.625 Megabaud, one of the operating speeds specified by the standard.

The Fibre Channel provides a transport vehicle for the upper-layer Intelligent Peripheral Interface (IPI) and Small Computer System Interface (SCSI) command sets, the High-Performance Parallel Interface (HIPPI) data link layer, and other user-defined command sets. The Fibre Channel is capable of replacing the SCSI, IPI, and HIPPI physical interfaces with a protocol-efficient alternative that provides performance improvements in distance and/or speed.

IPI and SCSI commands and HIPPI data link operations may all be intermixed on the Fibre Channel. Proprietary and other command sets may also use and share the Fibre Channel. See Figure 2.

GA9103

265 Mbaud Fibre Channel ENDEC

Features

- For Fibre Channel, point-to-point, network, and SCSI applications
- With fiber optics, the FC-265 chip set provides a complete FC-0, FC-1 solution
- 8b/10b Encode/Decode of data, ordered sets, and line states
- TTL-compatible 10-bit-wide Transmitter/Receiver interface with 26.5625 MHz byte clock
- CRC and Parity Generate/Check
- Common chip for fabric and device adapters
- Multiplexed data/control 8-bit system interface
- 68-pin PLCC

GA9103

The Fibre Channel is optimized for predictable transfers of large blocks of data such as those used in file transfers between processors (supercomputer, mainframe, super-mini, etc.), storage systems (disk and tape), communications, and output-only devices such as laser printers and raster-scan graphics terminals.

The Transmitter/Receiver chips, designed with TriQuint's proprietary 0.7 micron One-Up™ GaAs process, interface either directly to the electrical medium or to the fiber-optic interface. The chips implement parallel-to-serial conversion, bit clock generation, receive clock/data recovery, and serial-to-parallel conversion.

The Fibre Channel protocol is simple and economical and enhances system throughput. The transmission medium is isolated from the control protocol so that implementation of point-to-point links, multi-drop buses, rings, crosspoint switches, or other special implementations may be made in a technology best suited to the usage environment. Fibre channel is organized into five layers as shown in Figure 1. With this standard, the user may communicate over distances up to 10 km at baud rates of 132.8125 Megabaud to 1.0625 Gigabaud. This standard will support links over coaxial and fiber-optic cables.

Along with a fiber-optic module, this chipset will provide complete FC-0 and FC-1 solutions for a Fibre Channel data link.

Figure 1. GA9103 ENDEC Block Diagram

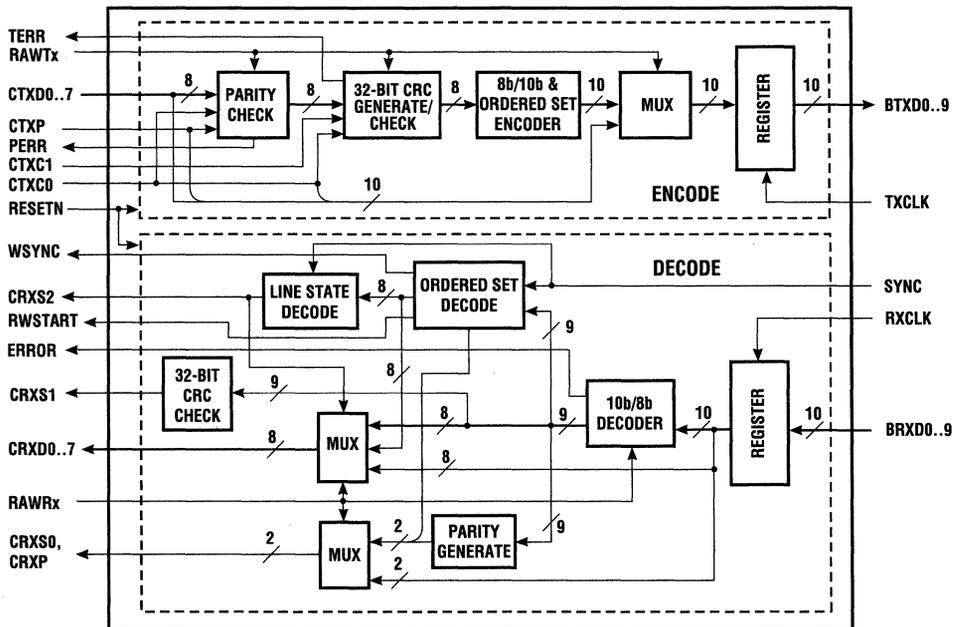
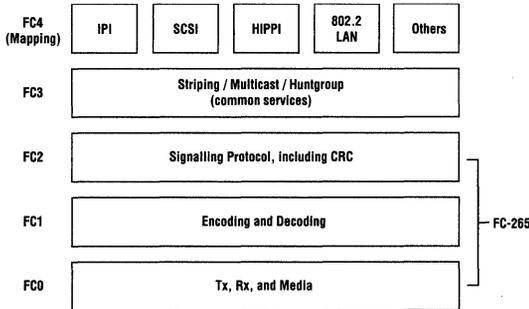


Figure 2. Layers of Fibre Channel



Functional Description

The GA9103 has an 8-bit inter-face to the host side and a 10-bit interface to the Transmitter (Tx) and the Receiver (Rx). The device has two major independent functional blocks, the ENCODE and the DECODE. The ENCODE block interfaces with the Tx and the DECODE with the Rx. Below are the details of the two functional blocks.

Encode

The PARITY CHECK block compares the input odd parity with that of the incoming data, CTXD0..7 and CTXCO. If the number of ones in the input is an even number, CTP will be HIGH. If the number of ones in the input data is odd, CTP will be LOW. If there is a parity error, it is flagged through the PERR signal. In the pass-through mode (RAWTx=1), PERR is forced to zero.

The 32-bit Generate/Check CRC block either generates or checks the 32-bit CRC for the incoming 8-bit bus, CTXD0..7. The methodology, polynomials, and equations for the 32-bit CRC are the same as the FDDI's Frame Check Sequence, as adopted by Fibre Channel. A 32-bit CRC is computed for every frame and the computation begins after the receipt of the Start-of-Frame (SOF) ordered set and finishes one byte before

the End-of-Frame (EOF). The CRC corresponds to the ones complement of the remainder obtained by dividing the frame sequence polynomial $H(x)$ by the following generator polynomial:

$$G(x) = X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$$

The frame sequence polynomial is formed as follows: the bits of the frame are treated as a coefficient of a polynomial $D(x)$ of order k , where k is one degree less than the total number of bits. The polynomial $H(x)$ is formed by multiplying $D(x)$ by X^{32} and inverting the 32 terms of the resulting polynomial starting at the $X(k+32)$ term. The order of computation within a byte is made starting with the least-significant bit (CTXD0) and continuing through to the most-significant bit (CTXD7). The CRC is appended to the incoming data, starting with the most significant coefficient (X^{31}) and continuing through to the least-significant coefficient.

The CRC check is performed by checking the remainder at the end of the incoming frame against the expected value. If the incoming CRC is correct, the remainder should be "C704DD7B" (Hex), in the order of reception. If an error occurs, it is flagged by the TERR pin. In the pass-through mode, the CRC function is disabled. The Generate CRC function is enabled at the device interface and the Check CRC function is enabled at the fabric interface by means of the CTXC1 input signal. A logic HIGH on the CTXC1 pin indicates the Generate CRC function is selected, while a logic LOW indicates that the Check CRC is selected. When initiated, the Generate/Check CRC commences after the Start-of-Frame signal, and ends prior to the End-of-Frame signal. (See Figures 3 and 4.)

To start the computation of the 32-bit Generate CRC mode in the ENCODE block, the following conditions must be met: CTXC1 is HIGH, the previous encoded

word was Start-of-Frame (SOF), and the CTXC0 signal goes from HIGH to LOW. The CRC computation is complete when the CTXC0 signal goes back HIGH. The CTXC0 signal must be HIGH for at least four byte clocks in order to append the CRC to the transmitted data. In the Generate CRC mode, the signal at the TERR pin (CRC Error) is LOW. The timing for the Generate CRC mode is shown in Figure 5. While the internal logic does check for parity during the CRC Append cycle, the four input bytes at CTXD0..7 are ignored.

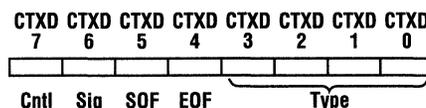
To initiate the 32-bit Check CRC mode in the ENCODE block, the following state is required: the CTXC0 signal goes from HIGH to LOW, the previous encoded ordered set was SOF, and CTXC1 is LOW. When the CTXC0 signal goes back to HIGH, the CRC computation is complete. The computed value is compared to "C704DD7B" (Hex) to see if an error occurred. If there is a CRC error, it is flagged through the TERR pin going HIGH for one byte time at the End-of-Frame. The timing for the Check CRC mode is shown in Figure 6.

The 8b/10b and Ordered Set ENCODER encodes the data as per the Fibre Channel rules for encoding. The encoding of valid data and special characters are shown in Tables 1 and 2. The tables have two columns of encoded output based on the current Running Disparity (R_D). The current Running Disparity may be positive or negative on power up, but on RESETN being activated, it is always negative. A new Running Disparity is calculated from the transmitted character. It is forced negative if: 1) Sig = 1, CTXC0 = 1, and the Ordered Set encode is a primitive, such as R-Rdy, etc., or 2) when the link exits the diagnostic (RAW) mode. The ordered sets are then encoded according to Table 3. Each ordered set is four bytes wide.

The ordered set encoding procedure is as follows: the ENCODER looks at the CXTD0..7 signal inputs while the Ordered Set, CXTC0, signal is HIGH and encodes four

bytes, based on the contents of CTXD0..7. The contents of CTXD0..7 in the next three bytes are ignored. The fields within the first byte, CTXD0..7, of the word for the Ordered Set Encoding are shown in Figure 3. CTXD7 corresponds to the Cntl signal. The Cntl signal,

Figure 3. Data Fields for Fibre Channel Ordered Set Encoding



when LOW, indicates Fibre Channel-defined ordered sets are being transmitted. When the Cntl signal is HIGH, undefined ordered sets are being transmitted. The Sig signal (CTXD6), when HIGH, indicates the Line State ordered set is being transmitted, and, when LOW, indicates an ordered set other than the Line State is being transmitted. SOF (CTXD5), when HIGH, indicates the Start-of-Frame ordered set is being transmitted, and EOF (CTXD4), when HIGH, indicates the End-of-Frame ordered set is being transmitted. Type (CTXD3..0) indicates the type of ordered sets within the SOF, EOF, Line States and Undefined categories that is being transmitted.

If PERR or TERR is HIGH within a frame, EOF_n and EOF_t for that particular frame are transmitted as EOF_{ni} (see Table 3). Similarly, if PERR or TERR is HIGH while EOF_{dt} is being transmitted, it is encoded as EOF_{dti} , to indicate an invalid condition at the node.

The MUX selects between the 8b/10b ENCODER output and the data inputs, CTXD0..7. When the RAWTx input signal is HIGH, the inputs CTXD0..7, CXP, and CTXC0 are selected, and TERR = 0. When the RAWTx input is LOW, the ENCODER output is selected. The output of the MUX is 10 bits wide and is clocked into the REGISTER using the transmit byte clock, TXCLK, from

the Transmitter chip, GA9101. The output of the REGISTER interface goes directly to the GA9101, the Transmitter I.C. of the FC-265.

The asynchronous RESETN input, when LOW, is used to clear all inter-*n*-al state machine registers. It will take

up to five byte clocks to clear the internal state machines after the RESETN input goes back HIGH.

The bit ordering for transmission in the RAW mode is CTXD0..7, CTPX1 and CTXC0. It corresponds to mapping these signals to BTXD9..0, respectively.

Figure 4. CRC Error Timing

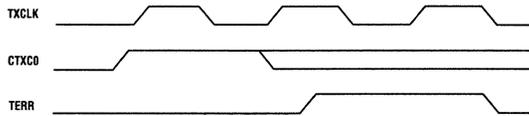


Figure 5. Generate CRC Mode Timing

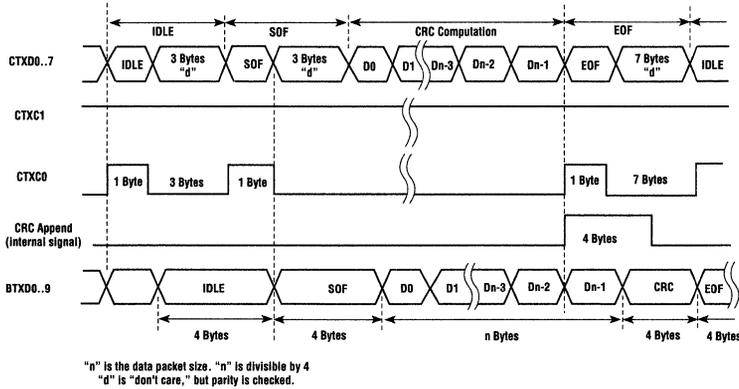
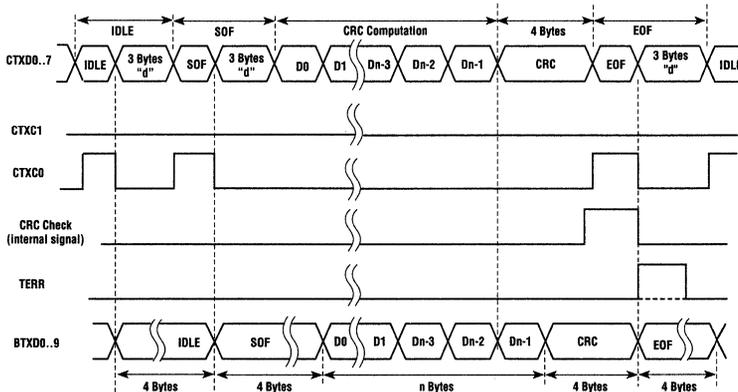


Figure 6. Check CRC Mode Timing



DATACOM PRODUCTS

Table 1. Valid Data Characters – Encoding

Data Byte		Bits		Current	RD -	Current	RD +	Data Byte		Bits		Current	RD -	Current	RD +
Name	HGF	EDCBA ¹	abcdei	fghj ²	abcdei	fghj ²		Name	HGF	EDCBA ¹	abcdei	fghj ²	abcdei	fghj ²	
D0.0	000	00000	100111	0100	011000	1011		D9.2	010	01001	100101	0101	100101	0101	
D1.0	000	00001	011101	0100	100010	1011		D10.2	010	01010	010101	0101	010101	0101	
D2.0	000	00010	101101	0100	010010	1011		D11.2	010	01011	110100	0101	110100	0101	
D3.0	000	00011	110001	1011	110001	0100		D12.2	010	01100	001101	0101	001101	0101	
D4.0	000	00100	110101	0100	001010	1011		D13.2	010	01101	101100	0101	101100	0101	
D5.0	000	00101	101001	1011	101001	0100		D14.2	010	01110	011100	0101	011100	0101	
D6.0	000	00110	011001	1011	011001	0100		D15.2	010	01111	010111	0101	101000	0101	
D7.0	000	00111	111000	1011	000111	0100		D16.2	010	10000	011011	0101	100100	0101	
D8.0	000	01000	111001	0100	000110	1011		D17.2	010	10001	100011	0101	100011	0101	
D9.0	000	01001	100101	1011	100101	0100		D18.2	010	10010	010011	0101	010011	0101	
D10.0	000	01010	010101	1011	010101	0100		D19.2	010	10011	110010	0101	110010	0101	
D11.0	000	01011	110100	1011	110100	0100		D20.2	010	10100	001011	0101	001011	0101	
D12.0	000	01100	001101	1011	001101	0100		D21.2	010	10101	101010	0101	101010	0101	
D13.0	000	01101	101100	1011	101100	0100		D22.2	010	10110	010101	0101	010101	0101	
D14.0	000	01110	011100	1011	011100	0100		D23.2	010	10111	111010	0101	000101	0101	
D15.0	000	01111	010111	0100	101000	1011		D24.2	010	11000	110011	0101	001100	0101	
D16.0	000	10000	011011	0100	100100	1011		D25.2	010	11001	100101	0101	100100	0101	
D17.0	000	10001	100011	1011	100011	0100		D26.2	010	11010	010101	0101	010101	0101	
D18.0	000	10010	010011	1011	010011	0100		D27.2	010	11011	110101	0101	001001	0101	
D19.0	000	10011	110010	1011	110010	0100		D28.2	010	11100	001110	0101	001110	0101	
D20.0	000	10100	001011	1011	001011	0100		D29.2	010	11101	011110	0101	010001	0101	
D21.0	000	10101	101010	1011	101010	0100		D30.2	010	11110	011110	0101	100001	0101	
D22.0	000	10110	010101	1011	011010	0100		D31.2	010	11111	101011	0101	010100	0101	
D23.0	000	10111	111010	0100	000101	1011		D0.3	011	00000	100111	0011	011000	1100	
D24.0	000	11000	110011	0100	001100	1011		D1.3	011	00001	011101	0011	100010	1100	
D25.0	000	11001	100110	1011	100110	0100		D2.3	011	00010	101101	0011	010010	1100	
D26.0	000	11010	010110	1011	010110	0100		D3.3	011	00011	110001	1100	110001	0011	
D27.0	000	11011	110110	0100	001001	1011		D4.3	011	00010	110101	0011	001010	1100	
D28.0	000	11100	001110	1011	001110	0100		D5.3	011	00010	101001	1100	101001	0011	
D29.0	000	11101	101110	0100	010001	1011		D6.3	011	00010	011001	1100	011001	0011	
D30.0	000	11110	011110	0100	100001	1011		D7.3	011	00011	111000	1100	000111	0011	
D31.0	000	11111	101011	0100	010100	1011		D8.3	011	01000	111001	0011	000110	1100	
D0.1	001	00000	100111	1001	011000	1001		D9.3	011	01001	100101	1100	100101	0011	
D1.1	001	00001	011101	1001	100010	1001		D10.3	011	01010	010101	1100	010101	0011	
D2.1	001	00010	101101	1001	010010	1001		D11.3	011	01011	110100	1100	110100	0011	
D3.1	001	00011	110001	1001	110001	1001		D12.3	011	01100	001101	1100	001101	0011	
D4.1	001	00100	110101	1001	001010	1001		D13.3	011	01101	101100	1100	101100	0011	
D5.1	001	00101	101001	1001	011001	1001		D14.3	011	01110	011100	1100	011100	0011	
D6.1	001	00110	011001	1001	011001	1001		D15.3	011	01111	010111	0011	101000	1100	
D7.1	001	00111	111000	1001	000111	1001		D16.3	011	10000	010101	0011	100100	1100	
D8.1	001	01000	111001	1001	000110	1001		D17.3	011	10001	100011	1100	100011	0011	
D9.1	001	01001	100101	1001	100101	1001		D18.3	011	10010	010011	1100	010011	0011	
D10.1	001	01010	010101	1001	010101	1001		D19.3	011	10011	110010	1100	110010	0011	
D11.1	001	01011	110100	1001	110100	1001		D20.3	011	10100	001011	1100	001011	0011	
D12.1	001	01100	001101	1001	001101	1001		D21.3	011	10101	101010	1100	101010	0011	
D13.1	001	01101	101100	1001	101100	1001		D22.3	011	10110	011010	1100	011010	0011	
D14.1	001	01110	011100	1001	011100	1001		D23.3	011	10111	111010	0011	000101	1100	
D15.1	001	01111	101011	1001	101000	1001		D24.3	011	11000	110011	0011	001100	1100	
D16.1	001	10000	011011	1001	100100	1001		D25.3	011	11001	100110	1100	100110	0011	
D17.1	001	10001	100011	1001	100011	1001		D26.3	011	11010	010110	1100	010110	0011	
D18.1	001	10010	010011	1001	010011	1001		D27.3	011	11011	110110	0011	001001	1100	
D19.1	001	10011	110010	1001	110010	1001		D28.3	011	11100	001110	1100	001110	0011	
D20.1	001	10100	001011	1001	001011	1001		D29.3	011	11101	101110	0011	010001	1100	
D21.1	001	10101	101010	1001	010101	1001		D30.3	011	11110	011110	0011	100001	1100	
D22.1	001	10110	010101	1001	010101	1001		D31.3	011	11111	101011	0011	010100	1100	
D23.1	001	10111	111010	1001	000101	1001		D0.4	100	00000	100111	0010	011000	1101	
D24.1	001	11000	110011	1001	001100	1001		D1.4	100	00001	011101	0010	100010	1101	
D25.1	001	11001	100110	1001	100110	1001		D2.4	100	00010	101101	0010	010010	1101	
D26.1	001	11010	010110	1001	010110	1001		D3.4	100	00011	110001	1101	110001	0010	
D27.1	001	11011	110101	1001	001001	1001		D4.4	100	00100	110101	0010	001010	1101	
D28.1	001	11100	001110	1001	001110	1001		D5.4	100	00101	101001	1101	101001	0010	
D29.1	001	11101	101110	1001	010001	1001		D6.4	100	00110	011001	1101	011001	0010	
D30.1	001	11110	011110	1001	100001	1001		D7.4	100	00111	111000	1101	000111	0010	
D31.1	001	11111	101011	1001	010100	1001		D8.4	100	01000	110101	0010	000110	1101	
D0.2	010	00000	100111	0101	011000	0101		D9.4	100	01001	100101	1101	100101	0010	
D1.2	010	00001	011101	0101	100010	0101		D10.4	100	01010	010101	1101	010101	0010	
D2.2	010	00010	101101	0101	010010	0101		D11.4	100	01011	110100	1101	110100	0010	
D3.2	010	00011	110001	0101	110001	0101		D12.4	100	01100	001101	1101	001101	0010	
D4.2	010	00100	110101	0101	001010	0101		D13.4	100	01101	101100	1101	101100	0010	
D5.2	010	00101	101001	0101	101001	0101		D14.4	100	01110	011100	1101	011100	0010	
D6.2	010	00110	011001	0101	011001	0101		D15.4	100	01111	010111	0010	101000	1101	
D7.2	010	00111	111000	0101	000111	0101		D16.4	100	10000	011011	0010	100100	1101	
D8.2	010	01000	111001	0101	000110	0101		D17.4	100	10001	100011	1101	100011	0010	

Table 1. Valid Data Characters – Encoding (cont.)

Data Byte Name	HGF	Bits	Current		RD -		Current		RD +	
			EDCBA ¹	abcdei	fgjh ²	abcdei	fgjh ²	abcdei	fgjh ²	
D18.4	100	10010	010011	1101	010011	0010				
D19.4	100	10011	110010	1101	110010	0010				
D20.4	100	10100	001011	1101	001011	0010				
D21.4	100	10101	101010	1101	101010	0010				
D22.4	100	10110	011010	1101	011010	0010				
D23.4	100	10111	111010	0010	000101	1101				
D24.4	100	11000	110011	0010	001100	1101				
D25.4	100	11001	100110	1101	100110	0010				
D26.4	100	11010	010110	1101	010110	0010				
D27.4	100	11011	110110	0010	001001	1101				
D28.4	100	11100	001110	1101	001110	0010				
D29.4	100	11101	101110	0010	010001	1101				
D30.4	100	11110	011110	0010	100001	1101				
D31.4	100	11111	101011	0010	010100	1101				
D0.5	101	00000	100111	1010	011000	1010				
D1.5	101	00001	011101	1010	100010	1010				
D2.5	101	00010	101101	1010	010010	1010				
D3.5	101	00011	110001	1010	110001	1010				
D4.5	101	00100	110101	1010	001010	1010				
D5.5	101	00101	101001	1010	101001	1010				
D6.5	101	00110	011001	1010	011001	1010				
D7.5	101	00111	111000	1010	000111	1010				
D8.5	101	01000	111001	1010	000110	1010				
D9.5	101	01001	100101	1010	100101	1010				
D10.5	101	01010	010101	1010	010101	1010				
D11.5	101	01011	110100	1010	110100	1010				
D12.5	101	01100	001101	1010	001101	1010				
D13.5	101	01101	101100	1010	101100	1010				
D14.5	101	01110	011100	1010	011100	1010				
D15.5	101	01111	010111	1010	101000	1010				
D16.5	101	10000	011011	1010	100100	1010				
D17.5	101	10001	100011	1010	100011	1010				
D18.5	101	10010	010011	1010	010011	1010				
D19.5	101	10011	110010	1010	110010	1010				
D20.5	101	10100	001011	1010	001011	1010				
D21.5	101	10101	101010	1010	101010	1010				
D22.5	101	10110	011010	1010	011010	1010				
D23.5	101	10111	111010	1010	000101	1010				
D24.5	101	11000	110011	1010	001100	1010				
D25.5	101	11001	100110	1010	100110	1010				
D26.5	101	11010	010110	1010	010110	1010				
D27.5	101	11011	110110	1010	001001	1010				
D28.5	101	11100	001110	1010	001110	1010				
D29.5	101	11101	101110	1010	010001	1010				
D30.5	101	11110	011110	1010	100001	1010				
D31.5	101	11111	101011	1010	010100	1010				
D0.6	110	00000	100111	0110	011000	0110				
D1.6	110	00001	011101	0110	100010	0110				
D2.6	110	00010	101101	0110	010010	0110				
D3.6	110	00011	110001	0110	110001	0110				
D4.6	110	00100	110101	0110	001010	0110				
D5.6	110	00101	101001	0110	101001	0110				
D6.6	110	00110	011001	0110	011001	0110				
D7.6	110	00111	111000	0110	000111	0110				
D8.6	110	01000	111001	0110	000110	0110				
D9.6	110	01001	100101	0110	100101	0110				
D10.6	110	01010	010101	0110	010101	0110				
D11.6	110	01011	110100	0110	110100	0110				
D12.6	110	01100	001101	0110	001101	0110				
D13.6	110	01101	101100	0110	101100	0110				
D14.6	110	01110	011100	0110	011100	0110				
D15.6	110	01111	010111	0110	101000	0110				
D16.6	110	10000	011011	0110	100100	0110				
D17.6	110	10001	100011	0110	100011	0110				
D18.6	110	10010	010011	0110	010011	0110				
D19.6	110	10011	110010	0110	110010	0110				
D20.6	110	10100	001011	0110	001011	0110				
D21.6	110	10101	101010	0110	101010	0110				
D22.6	110	10110	011010	0110	011010	0110				
D23.6	110	10111	111010	0110	000101	0110				
D24.6	110	11000	110011	0110	001100	0110				
D25.6	110	11001	100110	0110	100110	0110				
D26.6	110	11010	010110	0110	010110	0110				

Data Byte Name	HGF	Bits	Current		RD -		Current		RD +	
			EDCBA ¹	abcdei	fgjh ²	abcdei	fgjh ²	abcdei	fgjh ²	
D27.6	110	11011	110110	0110	001001	0110				
D28.6	110	11100	001110	0110	100110	0110				
D29.6	110	11101	101110	0110	010001	0110				
D30.6	110	11110	011110	0110	100001	0110				
D31.6	110	11111	101011	0110	010100	0110				
D0.7	111	00000	100111	0001	011000	1110				
D1.7	111	00001	011101	0001	100010	1110				
D2.7	111	00010	101101	0001	010010	1110				
D3.7	111	00011	110001	1110	110001	0001				
D4.7	111	00100	110101	0001	001010	1110				
D5.7	111	00101	101001	1110	101001	0001				
D6.7	111	00110	011001	1110	011001	0001				
D7.7	111	00111	111000	1110	000111	0001				
D8.7	111	01000	111001	0001	000110	1110				
D9.7	111	01001	100101	1110	100101	0001				
D10.7	111	01010	010101	1110	010101	0001				
D11.7	111	01011	110100	1110	110100	1000				
D12.7	111	01100	001101	1110	001100	1000				
D13.7	111	01101	101100	1110	101100	0001				
D14.7	111	01110	011100	1110	011100	1000				
D15.7	111	01111	010111	0001	100100	1110				
D16.7	111	10000	011011	0001	100100	1110				
D17.7	111	10001	100011	0111	100011	0001				
D18.7	111	10010	010011	0111	010011	0001				
D19.7	111	10011	110010	1110	110010	0001				
D20.7	111	10100	001011	0111	001011	0001				
D21.7	111	10101	101010	1110	101010	0001				
D22.7	111	10110	011010	1110	011010	0001				
D23.7	111	10111	111010	0001	000101	1110				
D24.7	111	11000	110011	0001	001100	1110				
D25.7	111	11001	100110	1110	100110	0001				
D26.7	111	11010	010110	1110	010110	0001				
D27.7	111	11011	110110	0001	001001	1110				
D28.7	111	11100	001110	1110	001110	0001				
D29.7	111	11101	101110	0001	010001	1110				
D30.7	111	11110	011110	0001	100001	1110				
D31.7	111	11111	101011	0001	010100	1110				

Table 2. Valid Special Characters – Encoding

Special Code Name	Current RD -		Current RD +	
	abcdei	fgjh ²	abcdei	fgjh ²
K28.0	001111	0100	110000	1011
K28.1	001111	1001	110000	0110
K28.2	001111	0101	110000	1010
K28.3	001111	0011	110000	1100
K28.4	001111	0010	110000	1101
K28.5	001111	1010	110000	0101
K28.6	001111	0110	110000	1001
K28.7	001111	0110	110000	0111
K29.7	111010	1000	000101	0111
K29.7	110110	1000	001001	0111
K30.7	011110	1000	100001	0111

Notes: 1. "HGF EDCBA" correspond to Data Inputs CTXD7..0, in that order.

2. "a" is to be transmitted first, followed by "b", "c", ..., "j". "abcdeifghj", in that order, correspond to BTXD9...BTXD0.

**DATA
COM
PRODUCTS**

Table 3. Ordered Set Encoding — Fibre Channel

Function	Cntl	C-Interface Signals (Mode: Raw)			Inputs (CTxD7..0)				BTx D 9..0	
		Byte 1 Sig	SOF	EOF	Type	Byte 2	Byte 3	Byte 4	Begin. RD	Output (four encoded bytes) Byte 1-Byte 2-Byte 3-Byte 4
SOFn1 ³	0	0	1	0	0001	$\bar{1}$	$\bar{1}$	$\bar{1}$	Neg	(K28.5–D21.5–D23.1–D23.1)
SOFn2	0	0	1	0	0010	$\bar{1}$	$\bar{1}$	$\bar{1}$	Neg	(K28.5–D21.5–D21.1–D21.1)
SOFn3	0	0	1	0	0011	$\bar{1}$	$\bar{1}$	$\bar{1}$	Neg	(K28.5–D21.5–D22.1–D22.1)
SOFi1	0	0	1	0	0101	$\bar{1}$	$\bar{1}$	$\bar{1}$	Neg	(K28.5–D21.5–D23.2–D23.2)
SOFi2	0	0	1	0	0110	$\bar{1}$	$\bar{1}$	$\bar{1}$	Neg	(K28.5–D21.5–D21.2–D21.2)
SOFi3	0	0	1	0	0111	$\bar{1}$	$\bar{1}$	$\bar{1}$	Neg	(K28.5–D21.5–D22.2–D22.2)
SOFc1	0	0	1	0	1101	$\bar{1}$	$\bar{1}$	$\bar{1}$	Neg	(K28.5–D21.5–D23.0–D23.0)
SOFf	0	0	1	0	1000	$\bar{1}$	$\bar{1}$	$\bar{1}$	Neg	(K28.5–D21.5–D24.2–D24.2)
EOFn ^{4,5}	0	0	0	1	0000	$\bar{1}$	$\bar{1}$	$\bar{1}$	Neg	(K28.5–D21.4–D21.6–D21.6)
									Pos	(K28.5–D21.5–D21.6–D21.6)
EOFt ⁵	0	0	0	1	0100	$\bar{1}$	$\bar{1}$	$\bar{1}$	Neg	(K28.5–D21.4–D21.3–D21.3)
									Pos	(K28.5–D21.5–D21.3–D21.3)
EOFdt ⁶	0	0	0	1	1100	$\bar{1}$	$\bar{1}$	$\bar{1}$	Neg	(K28.5–D21.4–D21.4–D21.4)
									Pos	(K28.5–D21.5–D21.4–D21.4)
EOFa	0	0	0	1	1001	$\bar{1}$	$\bar{1}$	$\bar{1}$	Neg	(K28.5–D21.4–D21.7–D21.7)
									Pos	(K28.5–D21.5–D21.7–D21.7)
EOFni	0	0	0	1	0001	$\bar{1}$	$\bar{1}$	$\bar{1}$	Neg	(K28.5–D10.4–D21.6–D21.6)
									Pos	(K28.5–D10.5–D21.6–D21.6)
EOFdti	0	0	0	1	1101	$\bar{1}$	$\bar{1}$	$\bar{1}$	Neg	(K28.5–D10.4–D21.4–D21.4)
									Pos	(K28.5–D10.5–D21.4–D21.4)
Idle	0	1	0	0	0000	$\bar{1}$	$\bar{1}$	$\bar{1}$	Neg	(K28.5–D21.4–D21.5–D21.5)
R-Rdy	0	1	0	0	0110	$\bar{1}$	$\bar{1}$	$\bar{1}$	Neg	(K28.5–D21.4–D10.2–D10.2)
NOS	0	1	0	0	1000	$\bar{1}$	$\bar{1}$	$\bar{1}$	Neg	(K28.5–D21.2–D31.5–D5.2)
OLS	0	1	0	0	1001	$\bar{1}$	$\bar{1}$	$\bar{1}$	Neg	(K28.5–D21.1–D10.4–D21.2)
LR	0	1	0	0	1010	$\bar{1}$	$\bar{1}$	$\bar{1}$	Neg	(K28.5–D9.2–D31.5–D9.2)
LRR	0	1	0	0	1011	$\bar{1}$	$\bar{1}$	$\bar{1}$	Neg	(K28.5–D21.1–D31.5–D9.2)
Undefined	1	0	0	0	0000	(XY _B) ²	(XY _C) ²	(XY _D) ²		(K28.0–DX.Y _B –DX.Y _C –DX.Y _D)
Undefined	1	0	0	0	0001	(XY _B) ²	(XY _C) ²	(XY _D) ²		(K28.1–DX.Y _B –DX.Y _C –DX.Y _D)
Undefined	1	0	0	0	0010	(XY _B) ²	(XY _C) ²	(XY _D) ²		(K28.2–DX.Y _B –DX.Y _C –DX.Y _D)
Undefined	1	0	0	0	0011	(XY _B) ²	(XY _C) ²	(XY _D) ²		(K28.3–DX.Y _B –DX.Y _C –DX.Y _D)
Undefined	1	0	0	0	0100	(XY _B) ²	(XY _C) ²	(XY _D) ²		(K28.4–DX.Y _B –DX.Y _C –DX.Y _D)
Undefined	1	0	0	0	0101	(XY _B) ²	(XY _C) ²	(XY _D) ²		(K28.5–DX.Y _B –DX.Y _C –DX.Y _D)
Undefined	1	0	0	0	0110	(XY _B) ²	(XY _C) ²	(XY _D) ²		(K28.6–DX.Y _B –DX.Y _C –DX.Y _D)
Undefined	1	0	0	0	0111	(XY _B) ²	(XY _C) ²	(XY _D) ²		(K28.7–DX.Y _B –DX.Y _C –DX.Y _D)
Undefined	1	0	0	0	1000	(XY _B) ²	(XY _C) ²	(XY _D) ²		(K23.7–DX.Y _B –DX.Y _C –DX.Y _D)
Undefined	1	0	0	0	1001	(XY _B) ²	(XY _C) ²	(XY _D) ²		(K27.7–DX.Y _B –DX.Y _C –DX.Y _D)
Undefined	1	0	0	0	1010	(XY _B) ²	(XY _C) ²	(XY _D) ²		(K29.7–DX.Y _B –DX.Y _C –DX.Y _D)
Undefined	1	0	0	0	1011	(XY _B) ²	(XY _C) ²	(XY _D) ²		(K30.7–DX.Y _B –DX.Y _C –DX.Y _D)

Notes: 1. Don't Care (any value).

2. Outputs for the data characters in the ordered set must be encoded to the correct data values.

3. SOF — Start-of-frame delimiter.

4. EOF — End-of-frame delimiter.

5. Encoded as EOFni if TERR or PERR = 1.

6. Encoded as EOFdti if TERR or PERR = 1.

Decode

The Decode block of the GA9103 is in the return path of a serial link from a remote transmitter to the host. It takes the encoded 10-bit data from the GA9102 (Rx) and decodes it into 8-bit data for the host. The 10-bit-wide input, BRXD0..9, is first clocked into the REGISTER, using the Receiver byte clock, RXCLK.

The 10b/8b DECODER decodes data and special characters according to Tables 1 and 2. Initially, the current Running Disparity is negative and each of the characters are decoded based on the received character. The DECODER also checks for the validity of received characters based on Tables 1 and 2.

The ERROR flag is set if there are code violations in any one of the four bytes of the word, or if the running disparity is in error. The ERROR signal is active for the entire duration of the word transmission, regardless of which byte was in error. The ERROR pin is also used to flag three other invalid conditions:

- A special character is detected in the second, third, or fourth character of a transmission word
- SYNC = 1 when BRXD0..9 is not a K28.5
- An ordered set is received with improper beginning running disparity

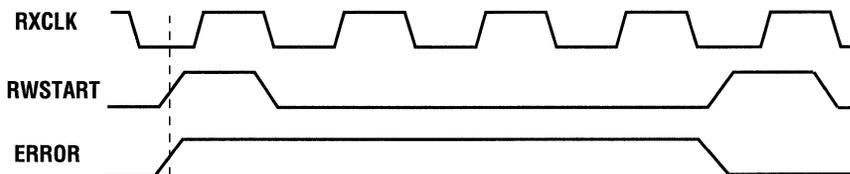
Examples of improper running disparity are: 1) SOF with positive running disparity, and 2) EOF content specified for positive running disparity, but received with BRD-. See Table 5.

Four bytes of the received signal must be analyzed in order to perform the ORDERED SET DECODE. For the purpose of ordered set decoding, the SYNC signal is used to align the four bytes of information to generate a word. The ordered sets are decoded according to Table 5 (Ordered Set Decoding).

The ORDERED SET DECODE block generates the Data/Ordered Set signal, CRXS0, along with the 8-bit decoded ordered set. A periodic signal, RWSTART, is also generated from this block. The SYNC signal is used to generate RWSTART, which is HIGH on the first byte output, CRXD0..7, of every word.

RWSTART is initialized by RESETN, RAWRx, or if K28.5 is followed by three valid data bytes (DX.Y_A, DX.Y_B, and DX.Y_C). The relationship between ERROR, RXCLK, and RWSTART is shown in Figure 7.

Figure 7. ERROR Signal Timing



The WSYNC signal from the ORDERED SET DECODE block is used to denote whether or not the link is word-synchronized.

As shown in the WSYNC State Diagram in Figure 8, WSYNC = 0 if the link loses word synchronization, is in a reset condition, or is in the "RAW" mode.

The link achieves word synchronization, (WSYNC = 1), only after three valid ordered sets are received without error and the first byte is a K28.5 character. Once synchronized, the link could lose synchronization if it receives a minimum of four invalid words within a consecutive set of seven words as per the sequence shown in the State Diagram.

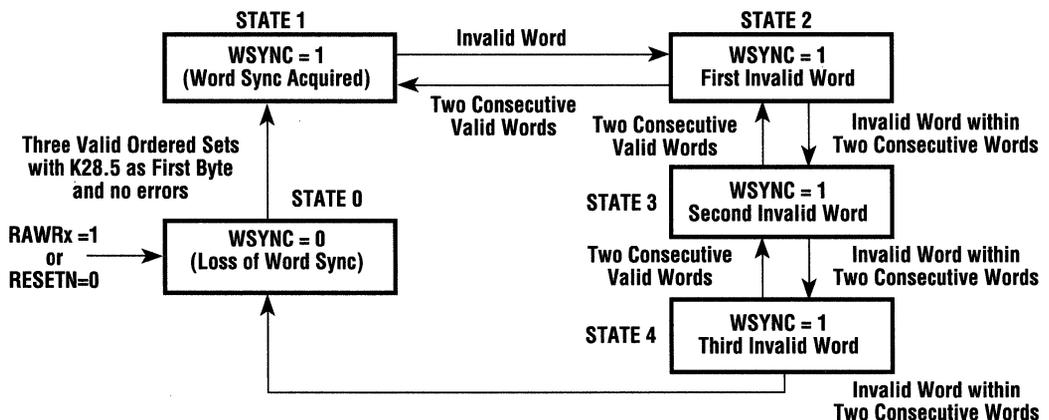
During this sequence, the link can reacquire word synchronization (State 1) if it receives two consecutive valid words in each of the States as shown in the State Diagram. If RAWRx = 1, WSYNC = 0.

If the ordered sets received correspond to a primitive sequence, the LINE STATE DECODER increments a counter using the SYNC signal. The primitive sequences, as defined by the Fibre Channel standard, are Offline State (OLS), Not-Operational State (NOS), Link Reset (LR), and Link Reset Response (LRR). These are transmitted to indicate a specific condition within a port.

Transmission of NOS indicates the port has detected a link failure condition. OLS indicates the port is preparing to either initialize, to go into the diagnostic mode, or to power down. LR is sent after a link timeout error has occurred or OLS is received. LRR is transmitted to recognize Link Reset.

If three consecutive ordered sets are received, the corresponding information is sent through CRXD0..7, according to the Ordered Set Decoding table (see Table 5).

Figure 8. WSYNC State Diagram

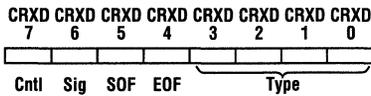


CRXS2 is active as long as one of the four possible line state signals, (OLS, NOS, LR, and LRR), is being received. Once active, CRXS2 remains active for the count of two line state ordered sets. On the third count, CRXS2 goes inactive and CRXS0 goes active. The proper line state output signals are flagged on CRXD0..7, as per Table 5. The figure below shows an example timing sequence for line states when RAWRx = 0.

The fields within the first byte, CRXD0..7, of the word for Ordered Set Decoding are shown in Figure 9.

CRXD7 corresponds to the Cntl signal which, when logic LOW, indicates the Fibre Channel-defined ordered set has been received. When the Cntl signal is HIGH, it indicates a non-Fibre Channel (undefined) ordered set has been received.

Figure 9. Data Fields for Ordered Set Decoding



The Sig signal (CRXD6), when HIGH, indicates the Line State ordered set, IDLE or R_RDY, has been received, and when LOW, the Sig signal indicates an ordered set other than Line State has been received.

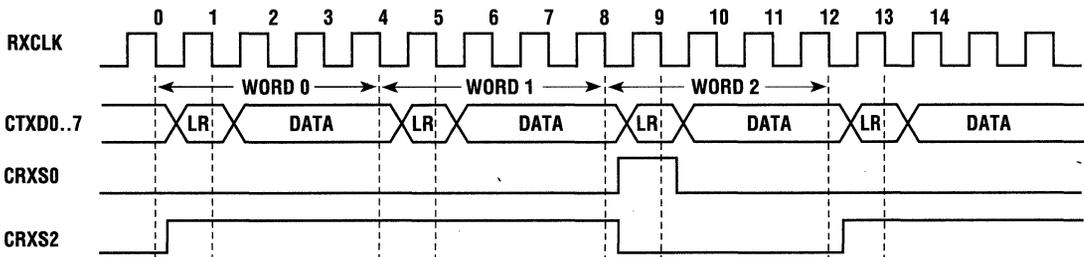
SOF (CRXD5), when HIGH, indicates the Start-of-Frame ordered set has been received and EOF (CRXD4), when HIGH, indicates the End-of-Frame ordered set.

Type (CRXD3..0) indicates the different types of ordered sets within the SOF, EOF, Line State and Undefined categories.

The CRC CHECK block performs a 32-bit Cyclic Redundancy Check on the received data. The CRC check begins after the Start-of-Frame Detect and finishes prior to End-of-Frame. CRC errors are flagged at the CRXS1 pin if RAWRx = 1 and CRXS1 = 0.

The RAW Rx mode is used whenever the 10-bit-wide input data to the receiver is to be passed through, undecoded, to the receive outputs, CRXD0..7, CRXP, and CRXS0. The MUX is used to choose between the decoded data/ordered set and the register output.

Figure 10. Example Timing Sequence for Line States



DATACOM PRODUCTS

When the RAWRx input signal is active, the undecoded data is selected; otherwise, the decoded data/ordered set/line state is chosen.

If CRXS2 and CRXS0 are LOW, decoded data output is selected through the MUX. If CRXS0 is HIGH and CRXS2 is LOW, the ordered set/line state is selected. If CRXS2 goes HIGH, the MUX output is disabled (that is, the output data is ignored). See Table 4.

The PARITY GENERATE block is used to generate the odd parity signal CRXP for every byte of data, CRXD0..7 and CRXS0. If the number of ones in the output, CRXD0..7

and CRXS0, is an even number, CRXP will be HIGH. If the number of ones in the output, CRXD0..7 and CRXS0, is odd, CRXP will be LOW.

Table 4. MUX Selection

RAW Rx	CRXS2	CRXS0	MUX Output
0	0	0	Decoded Data
0	0	1	Ordered set/line state
0	1	0	Decoded line state word
1	0	X	Undecoded data*

*Note: CRXS0 is part of this data.

Table 5. Ordered Set Decoding – Fibre Channel

Rx Input	C-Interface Signals (Mode: Raw) Outputs (CRXD7..0)								
	Cntl	Byte 1 Sig	SOF	EOF	Type	Byte 2 BR _D ⁻²	BR _D ⁺³	Byte 3	Byte 4
SOFn1	0	0	1	0	0001	(B5 ₁₆)	(37 ₁₆)	(37 ₁₆)	
SOFn2	0	0	1	0	0010	(B5 ₁₆)	(35 ₁₆)	(35 ₁₆)	
SOFn3	0	0	1	0	0011	(B5 ₁₆)	(36 ₁₆)	(36 ₁₆)	
SOFi1	0	0	1	0	0101	(B5 ₁₆)	(57 ₁₆)	(57 ₁₆)	
SOFi2	0	0	1	0	0110	(B5 ₁₆)	(55 ₁₆)	(55 ₁₆)	
SOFi3	0	0	1	0	0111	(B5 ₁₆)	(56 ₁₆)	(56 ₁₆)	
SOFc1	0	0	1	0	1101	(B5 ₁₆)	(17 ₁₆)	(17 ₁₆)	
SOFf	0	0	1	0	1000	(B5 ₁₆)	(58 ₁₆)	(58 ₁₆)	
EOFn	0	0	0	1	0000	(95 ₁₆)	(B5 ₁₆)	(D5 ₁₆)	(D5 ₁₆)
EOFt	0	0	0	1	0100	(95 ₁₆)	(B5 ₁₆)	(75 ₁₆)	(75 ₁₆)
EOFdt	0	0	0	1	1100	(95 ₁₆)	(B5 ₁₆)	(95 ₁₆)	(95 ₁₆)
EOFa	0	0	0	1	1001	(95 ₁₆)	(B5 ₁₆)	(F5 ₁₆)	(F5 ₁₆)
EOFni	0	0	0	1	0001	(8A ₁₆)	(AA ₁₆)	(D5 ₁₆)	(D5 ₁₆)
EOFdti	0	0	0	1	1101	(8A ₁₆)	(AA ₁₆)	(95 ₁₆)	(95 ₁₆)
Idle	0	1	0	0	0000	(95 ₁₆)	(B5 ₁₆)	(B5 ₁₆)	
R_Rdy	0	1	0	0	0110	(95 ₁₆)	(4A ₁₆)	(4A ₁₆)	
NOS	0	1	0	0	1000	(55 ₁₆)	(BF ₁₆)	(45 ₁₆)	
OLS	0	1	0	0	1001	(35 ₁₆)	(8A ₁₆)	(55 ₁₆)	

(Continued on next page)

- Notes:
1. Valid for any unrecognized control sequence starting with 'K28.5'. Not valid for acquiring Word Sync.
 2. BR_D⁻ – Beginning Running Disparity Negative.
 3. BR_D⁺ – Beginning Running Disparity Positive

Table 5. Ordered Set Decoding – Fibre Channel (continued)

Rx Input	C-Interface Signals (Mode: Raw) Outputs (CRXD7..0)							
	Cntl	Byte 1 Sig	SOF	EOF	Type	Byte 2 BR _D ⁻²	Byte 3 BR _D ⁺³	Byte 4
LR	0	1	0	0	1010	(49 ₁₆)	(BF ₁₆)	(49 ₁₆)
LRR	0	1	0	0	1011	(95 ₁₆)	(BF ₁₆)	(49 ₁₆)
(K28.0-DX.Y _B -DX.Y _C -DX.Y _D)	1	0	0	0	0000	(XY _B)	(XY _C)	(XY _D)
(K28.1-DX.Y _B -DX.Y _C -DX.Y _D)	1	0	0	0	0001	(XY _B)	(XY _C)	(XY _D)
(K28.2-DX.Y _B -DX.Y _C -DX.Y _D)	1	0	0	0	0010	(XY _B)	(XY _C)	(XY _D)
(K28.3-DX.Y _B -DX.Y _C -DX.Y _D)	1	0	0	0	0011	(XY _B)	(XY _C)	(XY _D)
(K28.4-DX.Y _B -DX.Y _C -DX.Y _D)	1	0	0	0	0100	(XY _B)	(XY _C)	(XY _D)
(K28.5-DX.Y _B -DX.Y _C -DX.Y _D) ¹	1	0	0	0	0101	(XY _B)	(XY _C)	(XY _D)
(K28.6-DX.Y _B -DX.Y _C -DX.Y _D)	1	0	0	0	0110	(XY _B)	(XY _C)	(XY _D)
(K28.7-DX.Y _B -DX.Y _C -DX.Y _D)	1	0	0	0	0111	(XY _B)	(XY _C)	(XY _D)
(K23.7-DX.Y _B -DX.Y _C -DX.Y _D)	1	0	0	0	1000	(XY _B)	(XY _C)	(XY _D)
(K27.7-DX.Y _B -DX.Y _C -DX.Y _D)	1	0	0	0	1001	(XY _B)	(XY _C)	(XY _D)
(K29.7-DX.Y _B -DX.Y _C -DX.Y _D)	1	0	0	0	1010	(XY _B)	(XY _C)	(XY _D)
(K30.7-DX.Y _B -DX.Y _C -DX.Y _D)	1	0	0	0	1011	(XY _B)	(XY _C)	(XY _D)

- Notes:
1. Valid for any unrecognized control sequence starting with 'K28.5'. Not valid for acquiring Word Sync.
 2. BR_D⁻ – Beginning Running Disparity Negative.
 3. BR_D⁺ – Beginning Running Disparity Positive

DATACOM PRODUCTS

Figure 11. System Block Diagram

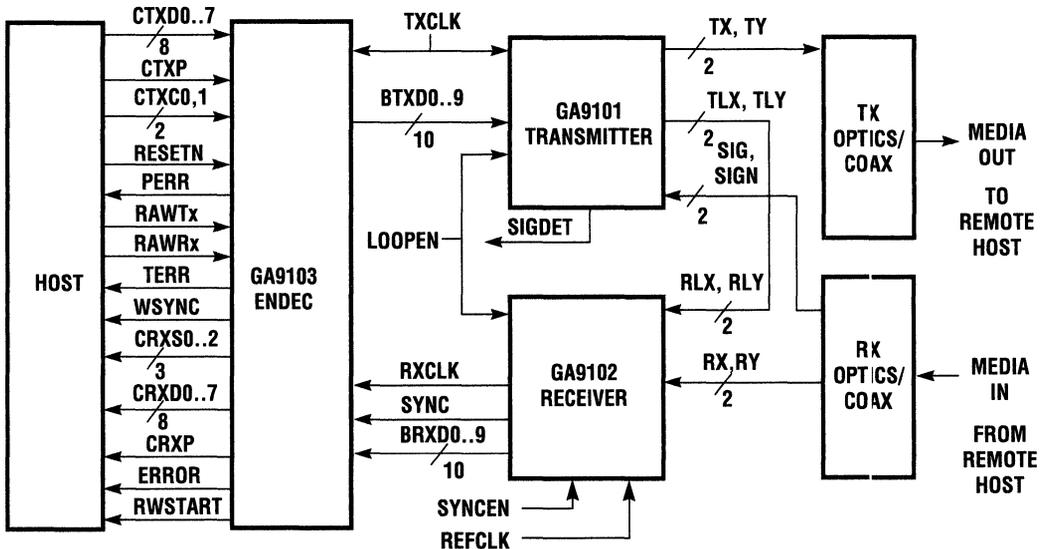


Table 6. Absolute Maximum Ratings

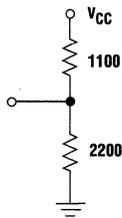
Exceeding the absolute maximum ratings may damage the device.

Storage temperature	-65°C to +150°C
Ambient temperature	-55°C to +125°C
Supply voltage to ground	-0.5 V to +7.0 V
DC input voltage	-0.5 V to ($V_{CC} + 0.5$ V)
DC input current	-30 mA to +5 mA

Table 7. Operating Conditions

(Proper functionality is guaranteed under these conditions.)

Supply voltage	5 V \pm 5%
Ambient temperature	0 to 70°C

Figure 12. TTL Test Load, TLL Outputs**Table 8. DC Characteristics**

(Over operating range unless otherwise specified.)

Symbol	Description	Test Conditions	Min.	Limits ¹ Typ.	Max.	Unit
V_{OH}	Output HIGH voltage	$V_{CC} = \text{Min}$ $I_{OH} = -4$ mA $V_{IN} = V_{IH}$ or V_{IL}		3.6		V
V_{OL}	Output LOW voltage	$V_{CC} = \text{Min}$ $I_{OL} = 4$ mA $V_{IN}^3 = V_{IH}$ or V_{IL}			0.37	V
V_{IH}^2	Input HIGH level	Guaranteed input logical HIGH voltage for all inputs	2.0			V
V_{IL}^2	Input LOW level	Guaranteed input logical LOW voltage for all inputs			0.8	V
I_{IL}	Input Leakage current	$V_{CC} = \text{Max}$ $V_{IN} = 0.40$ V		-150	-400	μ A

Notes: 1. Typical limits are: $V_{CC} = 5.0$ V and $T_A = 25^\circ$ C.

2. These are absolute values with respect to device ground, and all overshoots due to system or tester noise are included.

3. V_{IN} , the TTL input, can be HIGH or LOW.

Table 9. AC Characteristics – ENCODE

Parameter	Description	Min.	Typ.	Max.	Unit
T1	TXCLK Pulse Width HIGH	15.00			ns
T2	TXCLK Pulse Width LOW	15.00	T3 – T1		ns
T3	TXCLK Period	37.51	37.70	37.89	ns
T4	CTXD0..7; CTXP; CTXC0,1 Setup Time	2.00			ns
T5	CTXD0..7; CTXP; CTXC0,1 Hold Time	7.00			ns
T6	TXCLK ↑ to PERR, TERR	3.50		17.00	ns
T7	TXCLK ↑ to BTXD0..9	5.00		19.00	ns
T8	ENCODE Latency	2·T3 + 7		3·T3 + 12	ns

Figure 13. ENCODE Timing Diagram

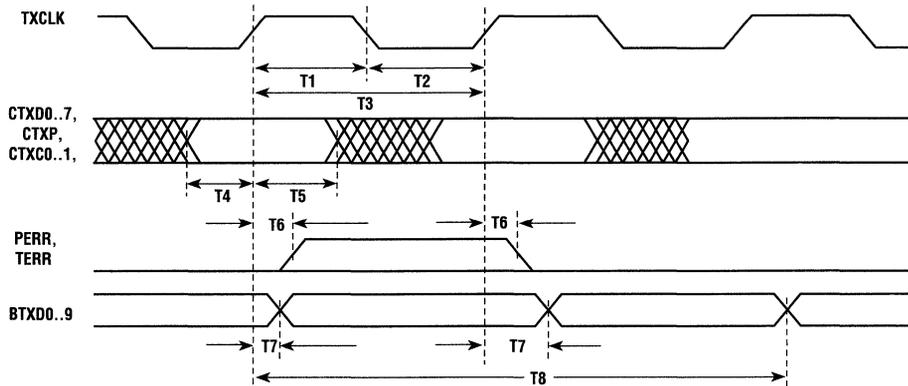


Table 10. AC Characteristics – DECODE

Parameter	Description	Min.	Typ.	Max.	Unit
T20	RXCLK Pulse Width HIGH	$(T22/2) - 3$			ns
T21	RXCLK Pulse Width LOW	$(T22/2) - 3$			ns
T22	RXCLK Period	37.51	37.70	37.89	ns
T23	BRXD0..9, SYNC Valid to RXCLK ↓	1.00			ns
T24	BRXD0..9, SYNC Valid from RXCLK ↓	8.00			ns
T25	CRXD0..7, CRXP, ERROR, CRXS0..2, RWSTART Valid to RXCLK ↑	4.70			ns
T26	CRXD0..7, CRXP, ERROR, CRXS0..2, RWSTART Valid from RXCLK ↑	18.25			ns
T27	CRXD0..7, CRXP, ERROR, CRXS0..2, RWSTART from RXCLK ↓	2.50		11.00	ns
T28	DECODE Latency	$6 \cdot T22$		$7 \cdot T22 + 10$	ns

Note: The DECODE functional block clocks off the negative edge of RXCLK.

Figure 14. DECODE Timing Diagram

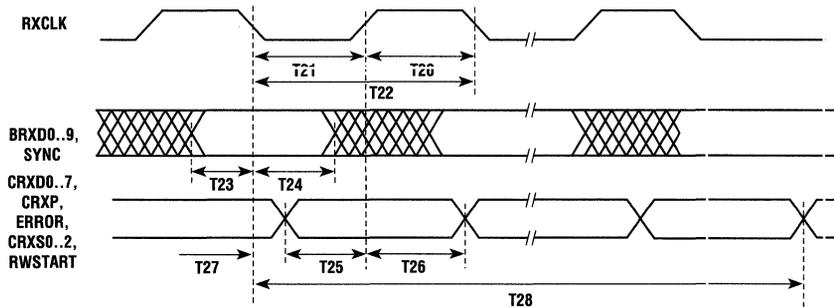


Table 11. AC Characteristics – Miscellaneous

Parameter	Description	Min.	Typ.	Max.	Unit
T29	RESETN Pulse Width LOW	10			ns

Figure 15. RESETN Timing Diagram

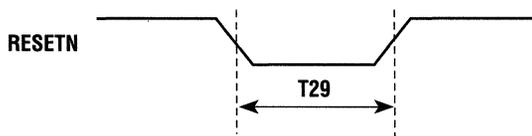


Figure 16. GA9103 Pinout

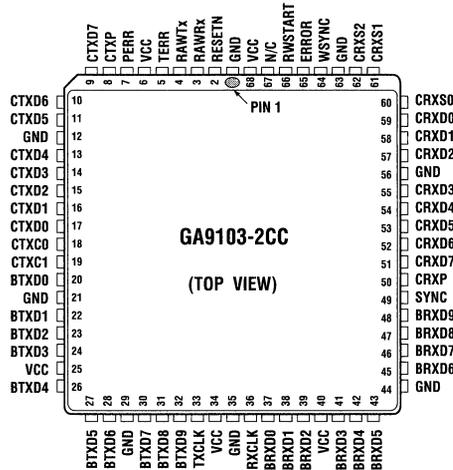
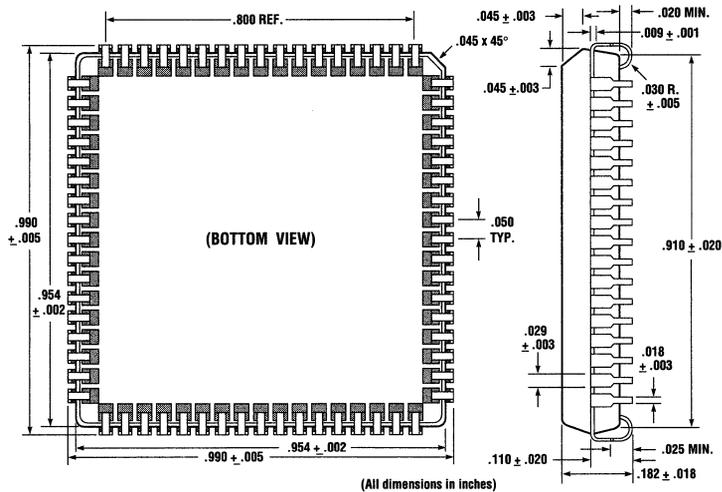


Table 12. Pin Definitions

Symbol	I/O	Quantity	Logic Level	Active	Description	Pin #
CRXD0..7	Output	8	TTL	HIGH	Receive Data Output	59–57, 55–51
CRXS0	Output	1	TTL	HIGH	Receive Control	60
CRXS1	Output	1	TTL	HIGH	Receive CRC Error	61
CRXS2	Output	1	TTL	HIGH	Line State	62
BRXD0..9	Input	10	TTL	HIGH	Receive Data Input	37–39, 41–43, 45–48
RXCLK	Input	1	TTL	HIGH	Receive Byte Clock	36
SYNC	Input	1	TTL	HIGH	Receive Byte Sync	49
TXCLK	Input	1	TTL	HIGH	Transmit Byte Clock	33
BTXD0..9	Output	10	TTL	HIGH	Transmit Data Output	20, 22–24, 26–28, 30–32
CTXD0..7	Input	8	TTL	HIGH	Transmit Data Input	17–13, 11–9
CTXC0	Input	1	TTL	HIGH	Transmit Control	18
TERR	Output	1	TTL	HIGH	Transmit CRC Error	5
RWSTART	Output	1	TTL	HIGH	Start of Word	66
CTXC1	Input	1	TTL	HIGH	Generate CRC	19
WSYNC	Output	1	TTL	HIGH	Word Synchronized	64
RAWTx	Input	1	TTL	HIGH	Raw Mode Transmit	4
RESETN	Input	1	TTL	LOW	System Reset	2
ERROR	Output	1	TTL	HIGH	Illegal Line Code or Disparity Received	65
PERR	Output	1	TTL	HIGH	Parity Error	7
CRXP	Output	1	TTL	HIGH	Odd Parity Output	50
CTXP	Input	1	TTL	HIGH	Odd Parity Input	8
RAWRx	Input	1	TTL	HIGH	Raw Mode Receive	3
VCC	Input	5	N/A	N/A	+5 Volt Supply	6, 25, 34, 40, 68
GND	Input	8	N/A	N/A	Ground	1, 12, 21, 29, 35, 44, 56, 63
RESERVED		1				67

GA9103

Figure 17. 68-Pin Plastic Leaded Chip Carrier (PLCC)



Ordering Information

GA9103-ENDEC 265 MBaud Fibre Channel ENDEC

Supporting Products

GA9101-2MC Transmitter

GA9102-2MC Receiver

Additional Information

For latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com Tel: (503) 615-9000

Email: sales@tqs.com Fax: (503) 615-8900

For technical questions and additional information on specific applications:

Email: applications@tqs.com

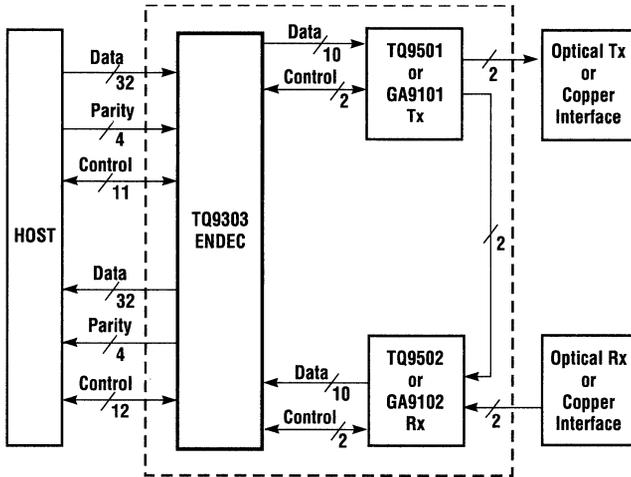
The information provided herein is believed to be reliable; TriQuint assumes no liability for inaccuracies or omissions. TriQuint assumes no responsibility for the use of this information, and all such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. TriQuint does not authorize or warrant any TriQuint product for use in life-support devices and/or systems.

Copyright © 1997 TriQuint Semiconductor, Inc. All rights reserved.

Revision 1.0.A October 1997



Figure 1. TQ9303 Block Diagram



The TQ9303 ENDEC (ENcoder/DECoder) implements 8b/10b encoding and decoding, ordered set encoding and decoding, and parity checking and generation as defined in the Fibre Channel Physical Signaling Interface Standard (FC-PH). The ENDEC fully implements the FC-1 layer of the Fibre Channel Standard. Implemented in a 0.8 μm CMOS process, the ENDEC also performs 32-bit CRC checking and generation as defined in the FC-2 layer of the Fibre Channel specification.

The TQ9303 ENDEC interfaces directly to TriQuint's FC-0 layer Fibre Channel Transmitter (Tx) and Receiver (Rx) chipsets at the speeds shown below:

FC Rate	Transmitter	Receiver	Data Rate (Mbaud)
FC-266	GA9101	GA9102	194-266
FC-531	TQ9501	TQ9502	500-625
FC-1063	TQ9501	TQ9502	1000-1250

TriQuint's Transmitter and Receiver devices are designed with TriQuint's proprietary 0.7-micron GaAs process. The Tx and Rx interface directly to copper-based electrical media or to a fiber-optic module. The Transmitter performs parallel-to-serial conversion on the encoded data and generates the internal high-speed clock for the serial output data stream. The Receiver recovers the clock and data from the input serial stream, performs serial-to-parallel conversion, and detects and aligns on the K28.5 character.

TQ9303

Fibre Channel Encoder/Decoder

Features

- Compliant with ANSI X3T11 Fibre Channel Standard
- Full implementation of Fibre Channel's FC-1 layer
- Interfaces directly with TriQuint's GA9101/GA9102 and TQ9501/TQ9502 FC-0 Fibre Channel chipsets
- Suitable for proprietary serial links (virtual ribbon cable)
- Implements 8b/10b encoding and decoding
- Implements ordered set encoding and decoding
- Checks and generates 32-bit CRC and parity
- 10-bit TTL-compatible interface to Transmitter and Receiver
- 32-bit interface to the host
- Fully synchronous operation
- 160-pin PQFP

DATACOM
 PRODUCTS

TQ9303

Fibre Channel provides a transport vehicle for Intelligent Peripheral Interface (IPI) and Small Computer System Interface (SCSI) upper layer command sets, High-Performance Parallel Interface (HIPPI) data link layer, and other user-defined command sets. Fibre Channel replaces the SCSI, IPI, and HIPPI physical interfaces with a protocol-efficient alternative that provides performance improvements over distance and speed.

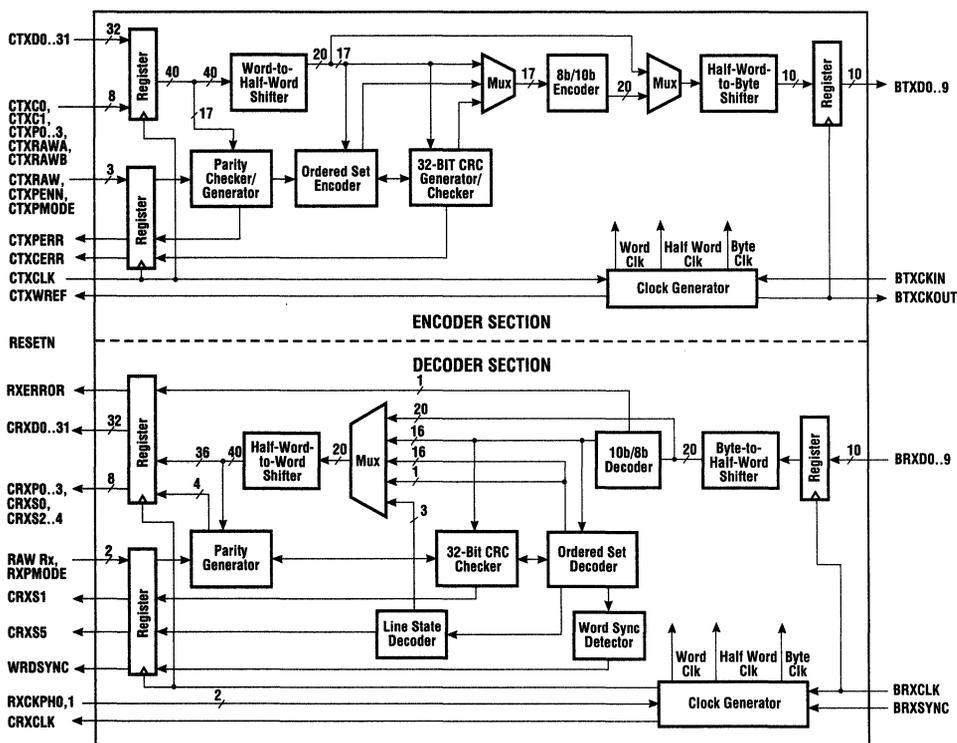
Fibre Channel is optimized for predictable transfers of large blocks of data such as those used in file transfers between processors (such as super computers, mainframes, and super minis), storage systems (such as disk and tape drives), communications devices, and output-only devices (such as laser printers and raster scan

graphics terminals). The Fibre Channel protocol is implemented in hardware, making it simple, efficient, and robust.

The lower level physical interface is decoupled from the higher level protocol, allowing Fibre Channel to be configured with various topologies. Point-to-point, multi-drop bus, ring, and cross-point switch topologies are permitted in Fibre Channel, optimizing it for specific applications.

Fibre Channel supports distances up to 10 Km at baud rates of 132.8125 Mbaud to 1.0625 Gbaud. Coax and STP (Shielded Twisted Pair) are used at lower data rates and shorter distances, while fiber-optic cables are used for higher data rates and longer distances.

Figure 2. TQ9303 ENDEC Block Diagram



Functional Description

The TQ9303 may be divided into two independent functional sections: the Encoder and Decoder, as shown in Figure 2. The Encoder section describes the flow of data from the host to the transmitter.

Conversely, the Decoder section describes the flow of data from the receiver to the host. Designed for full-duplex operation, the Encoder and Decoder will transmit and receive one at a time or simultaneously. The Encoder performs 8b/10b encoding of information from the host to the transmitter. The Decoder performs 10b/8b decoding of information from the receiver to the host. The host interface is denoted by a letter C (as in CTXP), and the transmit/receive interface is denoted by a letter B (as in BTXD0). Pins within the Encoder section are denoted with the letters TX (as in CTXP), and pins within the Decoder section are denoted with RX (as in CRXS1). At the host interface, the TQ9303 has a 32-bit transmit data bus and a 32-bit receive data bus, each with 4-bit parity and 8-bit control. The transmitter and receiver interfaces to the TQ9303 are 10-bit data buses. Table 5 includes all the pin descriptions. Detailed descriptions of the Encoder and Decoder sections follow.

Encoder Section

The Encoder has several functional blocks: Parity Check, 32-Bit CRC, Ordered Set generator, 8b/10b Encoder, and Clock Generator. The Encoder section has two modes of operation: Normal mode and Raw mode. In the Normal mode, the Encoder section receives a word from the host interface, checks parity, calculates CRC, divides the word into bytes, encodes them using 8b/10b, and generates a 10-bit output, as illustrated in Figure 2. In the Raw mode, the Encoder section receives a word from the host interface without parity check, CRC check, or 8b/10b encoding.

The following is the encode sequence data flow:

1. Word input
2. Parity check
3. Word-to-half-word conversion
4. Ordered set encoding
5. 32-bit CRC check or generate
6. Muxing between ordered set, 32-bit CRC, and unchanged input
7. 8b/10b encoding
8. Muxing between unchanged input and encoded word
9. Half-word-to-byte conversion
10. Byte output

Parity Check Block

Parity check depends on the TXPENN (Transmit Parity ENable Not) input. TXPENN high ignores parity, while TXPENN low checks parity for each byte on the data bus, CTXD0..31. There are four parity bits (CTXP0..3), each bit corresponding to a byte of data, as follows: CTXP0 to CTXD0..7, CTXP1 to CTXD8..15, CTXP2 to CTXD16..23, and CTXP3 to CTXD24..31. Control bit TXPMODE (Transmit Parity MODE) alters the normal meaning of CTXP3. TXPMODE low is the normal mode, where CTXP3 checks for parity for CTXD24..31. With TXPMODE high, CTXP3 checks for parity for CTXD24..31 and CTXC0. CTXC0 is a control input which indicates whether CTXD0..31 is data or an ordered set. An ordered set is a Fibre Channel word where the most significant byte is composed of a valid special character, K28.5, as defined in the standard. Appendix A includes a table of valid special characters. The parity bits follow odd parity convention, where it is high if the number of ones is even and low if the number of ones is odd.

CTXPERR (Transmit Parity ERROR) is driven high when an error is detected in the parity check mode. When parity checking is disabled, CTXPERR is driven low. In Raw Mode transmit, where the data flow bypasses the parity check, 32-bit CRC, 8b/10b encoder, and ordered set encoder, CTXPERR is driven low.

32-Bit CRC Block

32-bit Cyclic Redundancy Checking (CRC) generates or checks CRC, depending on CTXC1. CTXC1 high generates CRC, while CTXC1 low checks CRC for the incoming frame. The CRC used in Fibre Channel is the same as FDDI's frame check sequence, where a 32-bit CRC is computed for every frame, starting after SOF (Start Of Frame) and ending a byte before EOF (End Of Frame). The resulting 32-bit CRC is automatically inserted into the frame before EOF.

In the check CRC mode, CTXCERR (Transmit Crc ERROR) is driven high when a CRC error is detected.

In the generate CRC mode, CTXCERR is driven low. In Raw Mode transmit where the data flow bypasses the parity check, 32-bit CRC, 8b/10b encoder, and ordered set encoder, CTXCERR is driven low.

The Generate CRC mode timing diagrams are shown in Figure 3. CTXC1 is high for the entire frame, when generating CRC. CTXC0 is high only for the duration of SOF, indicating that the input word (CTXD0..31) is an ordered set. Similarly, CTXC0 is high for the duration of EOF, which is another ordered set. The 32-bit CRC block computes the CRC for data after SOF and before EOF. The resulting CRC is inserted between the last data word and EOF at the output (BTXD0..9).

The Check CRC mode timing diagrams are shown in Figure 4. CTXC1 is low for the whole frame when checking CRC. CTXC0 is high only for the duration of SOF, indicating that the input word (CTXD0..31) is an ordered set. Similarly, CTXC0 is high for the duration of EOF, another ordered set. 32-bit CRC begins after SOF

Figure 3. Generate CRC Mode Timing

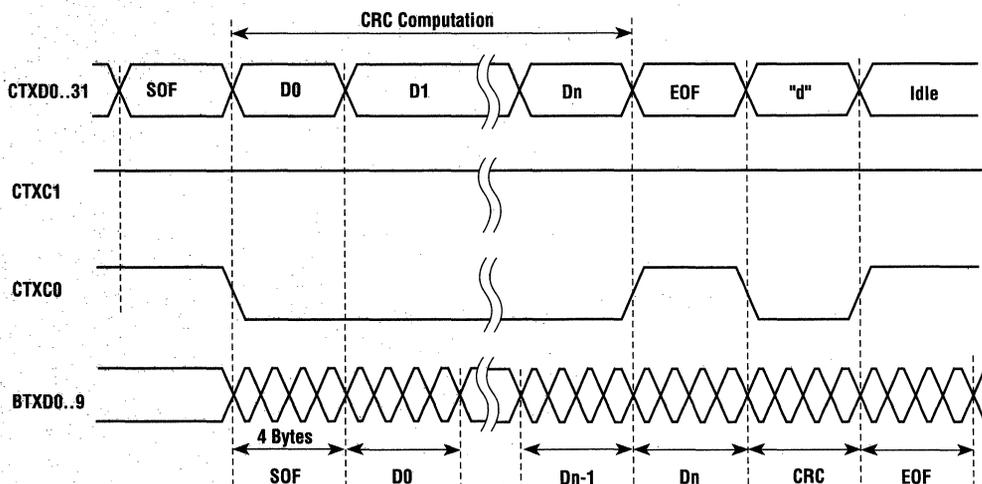
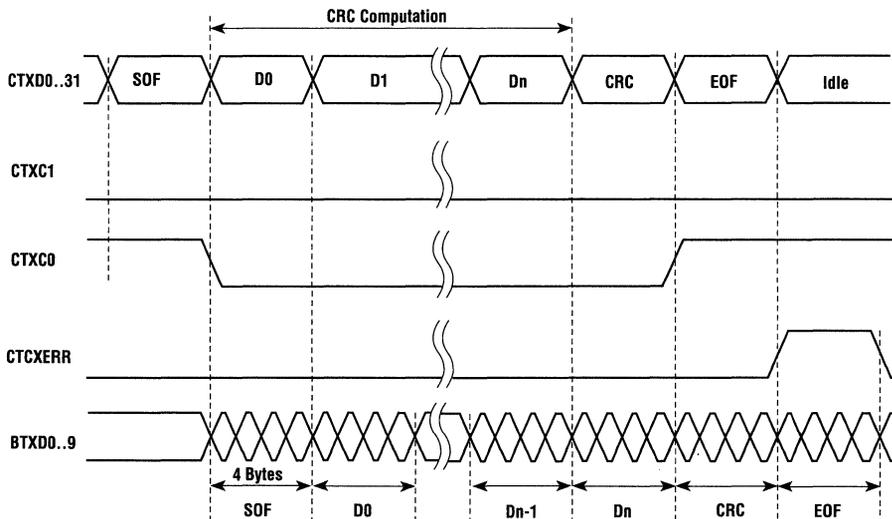


Figure 4. Check CRC Mode Timing



and ends before EOF. CTCXERR remains low if the computed CRC matches the CRC input on CTXD0..31. CTCXERR is driven high for one word cycle after the end of EOF.

If CTXC1 is high (generate CRC) then the ENDEC will add one word (the CRC) to the user's data frame before encoding the EOF. In this situation, when the user commands the ENDEC to encode an EOF, it is latched for one CTXCLK cycle while the ENDEC inserts the generated CRC in the data stream. Then the requested EOF is encoded. During the encoding of the EOF (that is, the one that was latched for encoding after the CRC was inserted) the ENDEC ignores the CTX inputs.

Ordered Set Generator Block

An ordered set is a Fibre Channel word in which the first byte is a K28.5 special character, followed by valid data characters. Appendix B contains tables for the ordered set coding scheme. When CTXC0 is high, the ordered set generator generates an ordered set from

the most significant byte of the input data, CTXD24..31. Although only the most significant byte of the input word is required for generating an ordered set, and lower order bits CTXD0..23 are "don't cares" for encoding the ordered set, parity checking is performed on the word. Valid word parity must be maintained to prevent parity errors.

If a parity or CRC error is detected within a frame, some EOF ordered sets are modified, indicating an invalid frame. Ordered sets EOF_N (EOF Normal) and EOF_T (EOF Terminate) are modified to EOF_{NI} (EOF Normal-Invalid).

Any ordered set can be sent or received. If the ordered set desired is not in the predefined set of Fibre Channel ordered sets, the user can create it using the "special" ordered set commands (see Appendix B). For instance, to send "K28.5, D0.0, D31.7, D0.0," the user would send 8500FF00h on CTXD0..31 while holding CTXC0 high. When receiving this same "special" ordered set

(which does not correspond to any predefined Fibre Channel ordered set) the ENDEC will send the user the same value, 8500FF00h, while holding CRXS0 high. It is up to the user to examine the second, third, and fourth bytes of “special” ordered sets to identify them.

8b/10b Encoder Block

The 8b/10b Encoder encodes 8-bit-wide data to 10-bit-wide data to improve its transmission characteristics. The 8b/10b coding scheme maintains the signal DC balance by keeping the same number of ones and zeros for easier receiver designs, provides good transition density for improved clock recovery, and improves error checking. It also forces the correct running disparity when encoding line states, idles, or receiver-ready ordered sets. Appendix A contains the lookup tables for the 8b/10b coding scheme.

Clock Generator Block

The Clock Generator generates word, half-word, and byte clocks required by other blocks in the Encoder. It uses BTXCKIN (a byte clock) from the transmitter as a reference clock. For example, using Fibre Channel data rates, BTXCKIN runs at 106.25 MHz using FC1063, 53.125 MHz using FC531, and 26.5625 MHz using FC266. The Clock Generator generates BTXCKOUT for clocking BTXD0..9. It also generates CTXWREF, a word clock used by the host to generate CTXCLK, which clocks the host I/O registers. CTXCLK runs at 25.5625 MHz using FC1063, 13.28125 MHz using FC531, and 6.640625 MHz using FC266.

Raw Mode Transmit

In Raw Mode Transmit where TXRAW is high for the whole frame, the input data word bypasses the parity check, ordered set generator, CRC, and 8b/10b, and is directly converted to bytes of data. The word-to-byte mapping of input to output is listed in Table 1. Note that

in raw mode, a “raw” word may be inserted into the data flow at any time, although running disparity will be forced negative and the word sync detector state machine will reset.

Proprietary Link Mode

The PL_IDLE (Proprietary Link IDLE) input can be used to simplify designs that do not have to conform to Fibre Channel standards. In such designs the CTXC0 input is driven low (that is, grounded) and the PL_IDLE pin is used to distinguish data from nondata. The PL_IDLE pin controls a bit logic in front of the input registers of the CTXC0 and CTXD24..31 inputs. It was added to make it easier for users who aren't concerned with the Fibre Channel protocol, but simply want to control the transmission of data without having to mux control information into their data paths in order to control the CTXD24..31 pins for ordered set control.

On the rising edge of CTXCLK on the first cycle of PL_IDLE going high, the input registers for CTXC0 and CTXD24..31 are “jammed” with the value that would make the ENDEC encode an EOFa. As long as PL_IDLE is held high, these input registers are jammed with the value that would make the ENDEC encode an IDLE ordered set. If CTXC1 is low (check mode) CTXERR will properly reflect the validity of CRC contained in the user's data (assuming the user's data contains CRC), or it can be ignored if no CRC is used. If CTXC1 is high (generate mode), the ENDEC will insert CRC before encoding the EOFa followed by IDLEs. This creates a situation in which the user's data will begin as soon as PL_IDLE is dropped (with no preceding SOF); but it does not present a problem for the ENDEC, because the CRC blocks in both Rx and Tx halves are initialized by any ordered set. Thus, the IDLE ordered set that precedes the user's data is sufficient to ensure proper CRC calculation.

Table 1. Raw Mode I/O Mapping

TRANSMISSION ORDER	Bit	ENCODE: Word to Bytes		DECODE: Bytes to Word	
FIRST BYTE	39	CTXC0	BTXD0	BRXD0	CRXS0
	38	CTXP3	BTXD1	BRXD1	CRXP3
	37	CTXD31	BTXD2	BRXD2	CRXD31
	36	CTXD30	BTXD3	BRXD3	CRXD30
	35	CTXD29	BTXD4	BRXD4	CRXD29
	34	CTXD28	BTXD5	BRXD5	CRXD28
	33	CTXD27	BTXD6	BRXD6	CRXD27
	32	CTXD26	BTXD7	BRXD7	CRXD26
	31	CTXD25	BTXD8	BRXD8	CRXD25
FIRST SERIAL BIT IN TX/RX	30	CTXD24	BTXD9	BRXD9	CRXD24
SECOND BYTE	29	CTXC1	BTXD0	BRXD0	CRXS2
	28	CTXP2	BTXD1	BRXD1	CRXP2
	27	CTXD23	BTXD2	BRXD2	CRXD23
	26	CTXD22	BTXD3	BRXD3	CRXD22
	25	CTXD21	BTXD4	BRXD4	CRXD21
	24	CTXD20	BTXD5	BRXD5	CRXD20
	23	CTXD19	BTXD6	BRXD6	CRXD19
	22	CTXD18	BTXD7	BRXD7	CRXD18
	21	CTXD17	BTXD8	BRXD8	CRXD17
THIRD BYTE	20	CTXD16	BTXD9	BRXD9	CRXD16
	19	CTXRAWA	BTXD0	BRXD0	CRXS3
	18	CTXP1	BTXD1	BRXD1	CRXP1
	17	CTXD15	BTXD2	BRXD2	CRXD15
	16	CTXD14	BTXD3	BRXD3	CRXD14
	15	CTXD13	BTXD4	BRXD4	CRXD13
	14	CTXD12	BTXD5	BRXD5	CRXD12
	13	CTXD11	BTXD6	BRXD6	CRXD11
	12	CTXD10	BTXD7	BRXD7	CRXD10
LAST SERIAL BIT IN TX/RX	11	CTXD9	BTXD8	BRXD8	CRXD9
FOURTH BYTE	10	CTXD8	BTXD9	BRXD9	CRXD8
	9	CTXRAWB	BTXD0	BRXD0	CRXS4
	8	CTXP0	BTXD1	BRXD1	CRXP0
	7	CTXD7	BTXD2	BRXD2	CRXD7
	6	CTXD6	BTXD3	BRXD3	CRXD6
	5	CTXD5	BTXD4	BRXD4	CRXD5
	4	CTXD4	BTXD5	BRXD5	CRXD4
	3	CTXD3	BTXD6	BRXD6	CRXD3
	2	CTXD2	BTXD7	BRXD7	CRXD2
	1	CTXD1	BTXD8	BRXD8	CRXD1
	0	CTXD0	BTXD9	BRXD9	CRXD0

DATAKOM
PRODUCTS

Proprietary Link Mode (continued)

When PL_IDLE is driven low, data words on CTXD0..31 are encoded just as in Fibre Channel operation. When PL_IDLE is driven high, the TQ9303 encodes one EOFa ordered set followed by IDLE ordered sets for as long as PL_IDLE remains high.

The EOFa ordered set is used to ensure proper running disparity. When using the PL_IDLE signal, IDLE ordered sets do not force proper running disparity. It is therefore necessary to transmit at least one word with PL_IDLE low followed by at least one word with PL_IDLE high in order to guarantee proper running disparity.

Without proper running disparity, the receiver portion of the TQ9303 may flag the IDLE ordered sets as errors and prevent the word sync state machine from reaching the synchronized state as long as the running disparity is incorrect.

Without proper running disparity, the receiver portion of the TQ9303 may flag the IDLE ordered sets as errors and prevent the word sync state machine from reaching the synchronized state as long as the running disparity is incorrect.

The contents and parity of CTXD0..31 and CTXP0..3 are ignored during the word cycles when PL_IDLE is held high. If CTXC1 is low, then CRC checking will occur, which may cause the TXCERR signal to indicate an error, which can be ignored in proprietary designs. If CTXC1 is driven high, then the TQ9303 will generate a 32-bit CRC word during the first word cycle of PL_IDLE high. During the second word cycle of PL_IDLE high, the EOFa will be encoded followed by IDLE ordered sets. Therefore, at least two word cycles of PL_IDLE high between data bursts must be provided when using CRC generation (that is, CTXC1 high). When using CRC

generation, the CRXS1 signal is used to indicate CRC errors. When not using the CRC, CRXS1 should be ignored. For non-Fibre Channel designs making use of the PL_IDLE input, the CRXS0 output can be used to distinguish received data from idle time.

Decoder Section

The Decoder has several functional blocks: 10b/8b Decoder, Ordered Set Decoder, Word Sync Detector, Line State Decoder, 32-bit CRC Checker, Parity Generator, and Clock Generator.

The Decoder section has two modes of operation: the Normal mode and Raw mode. In the Normal mode, the Decoder section takes 10 bits of data from the Receiver output, decodes it using 10b/8b, decodes ordered sets, checks CRC, combines four bytes into a single word output, and generates parity. In the Raw mode, the Decoder section directly combines the bytes into words, bypassing 10b/8b decoding, ordered set decoding, CRC checking, and parity generation.

The following is the decode sequence data flow:

1. Byte Input
2. Byte-to-Half-Word Conversion
3. 10b/8b Decoding
4. Ordered Set Decoding
5. Line State Decoding
6. Word Sync Generation
7. 32-Bit CRC Checking
8. Muxing between Ordered Set, Unchanged Input, 10b/8b Decoded Input, and Status Bits
9. Half-Word-to-Word Conversion
10. Parity Generation
11. Word Output

10b/8b Decoder Block

The 10b/8b Decoder decodes the 10-bit input (BRXD0..9) into 8 bits, as defined by the Fibre Channel 8b/10b coding scheme. The 10b/8b Decoder drives the RXERROR (Receiver ERROR) high whenever errors are detected. There are three types of errors: invalid characters, invalid running disparities, and special characters that are not positioned in the most significant byte of a word. When the 10b/8b Decoder receives a BRXSYNC of 1, it identifies the input data byte as a K28.5 character and realigns the data in the higher order byte of the half word. In Fibre Channel, K28.5 characters appear only in the most significant byte of a valid generated parity word. RXERROR remains high for the word cycle in which the error occurred.

Ordered Set Decoder Block

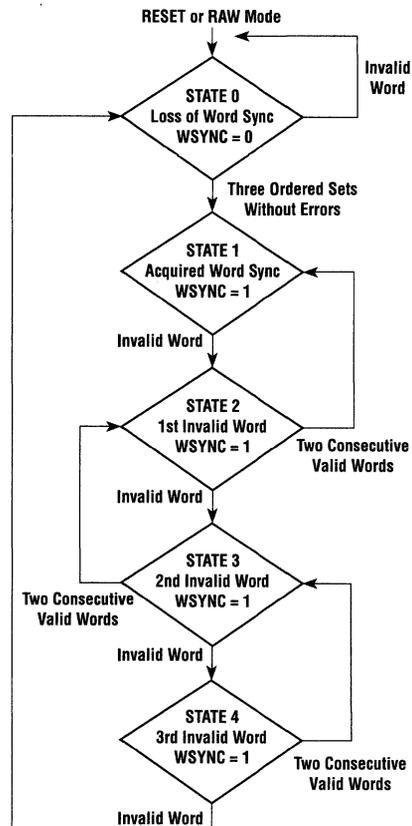
The Ordered Set Decoder decodes the ordered sets from the 10b/8b Decoder output. It generates the decoded ordered set, which is then fed into the mux along with CRXS0. CRXS0 is a status signal which is low for a data word and high for an ordered set. The ordered set decoding table is included in Appendix B.

Word Sync Detector Block

The Word Sync Detector contains a state machine that monitors the number of valid ordered sets and errors received. The Word Sync Detector drives WRDSYNCN low to indicate that word synchronization on the link has been established. It drives WRDSYNCN high when word synchronization has been lost.

Figure 5 illustrates how word synchronization is established and lost. The state machine has five states: State 0 – Loss of Word Sync, State 1 – Word Sync Acquired, State 2 – 1st Invalid Word, State 3 – 2nd Invalid Word, and State 4 – 3rd Invalid Word. Upon RESET or Raw mode at State 0, the initial condition of

Figure 5. Sync State Flow Diagram



WRDSYNCN is high. If the Word Sync Detector receives three consecutive ordered sets without errors, it acquires word synchronization and moves to State 1, where WRDSYNCN is driven low. If it receives an invalid word while in State 1, it moves to State 2 (1st Invalid Word). If the Word Sync Detector receives an invalid word while in State 2, it moves to State 3 (2nd Invalid Word). If, however, it receives two consecutive valid words, it moves back to State 1. This logic applies to State 3 and State 4. In State 4 (3rd Invalid Word) if the Decoder receives an invalid word, it moves to State 0 (Loss of Word Sync).

Line State Decoder Block

The state machine that indicates line state status simply looks for three consecutive line state primitives (that is, three of a kind in a row) to achieve a particular Fibre Channel line state. Line states are used in link initialization protocol, as described in the Fibre Channel specification (FC-PH). A subset of the ordered sets, line states are Fibre Channel primitive sequences which provide information regarding the condition of the link. The following are the four line states:

- **Off-Line State (OLS)** indicates either an internal port failure or a transmitter power down/ diagnostics performance / initialization.
- **Non-Operational State (NOS)** signals a link failure.
- **Link Reset (LR)** recognizes the OLS and port reset conditions.
- **Link Reset Response (LRR)** recognizes a link reset.

These line states are defined in Appendix B. The Line State Decoder generates CRXS2..3, the line state status bits which advise the host as to the state of the Sync State Machine, and CRXS4..5, the line state ID bits which signal the occurrence of certain primitive sequences. The status bits are shown in Tables 2 and 3.

32-Bit CRC Checker Block

The CRC Checker computes the 32-bit cyclic redundancy check on the received data. The CRC Error Status bit CRXS1 is driven high when an error is detected. In Raw mode, CRC is not checked, and CRXS1 is driven low.

Table 2. Line State Status Output

CRXS3	CRXS2	Line State Status
0	0	No State
0	1	Pending State
1	0	In State
1	1	Invalid Sequence

Parity Generator Block

Four parity bits (CTXP0..3) are generated by the Parity Generator. Each parity bit corresponds to a byte of data, as follows: CRXP0 to CRXD0..7, CRXP1 to CRXD8..15, CRXP2 to CRXD16..23, and CRXP3 to CRXD24..31.

Control bit RXPMODE (Receive Parity MODE) alters the normal meaning of CRXP3. RXPMODE low is the normal mode, where CRXP3 generates parity for CRXD24..31. With RXPMODE high, however, CRXP3 generates parity for CRXD24..31 and CRXS0. CRXS0 is a control output that indicates whether CTXD0..31 is data or an ordered set.

The parity bits follow odd parity convention, where it is high if the number of ones is even and low if the number of ones is odd.

In Raw mode, the Parity Generator does not generate parity, and the output parity bits are mapped with the input data as shown in Table 1.

Clock Generator Block

The Clock Generator generates word, half-word, and byte clocks required by other blocks in the Decoder. The Clock Generator uses the recovered clock, BRXCLK, generated by the TQ9502 Receiver. For example, using Fibre Channel data rates, BRXCLK (a byte clock) runs at 106.25 MHz using FC1063, 53.125 MHz using FC531, and 26.5625 MHz using FC266.

Table 3. Line State ID Output

CRXS5	CRXS4	Line State ID
0	0	NOS – Non-Operational State
0	1	OLS – Off-Line State
1	0	LR – Link Reset
1	1	LRR – Link Reset Response

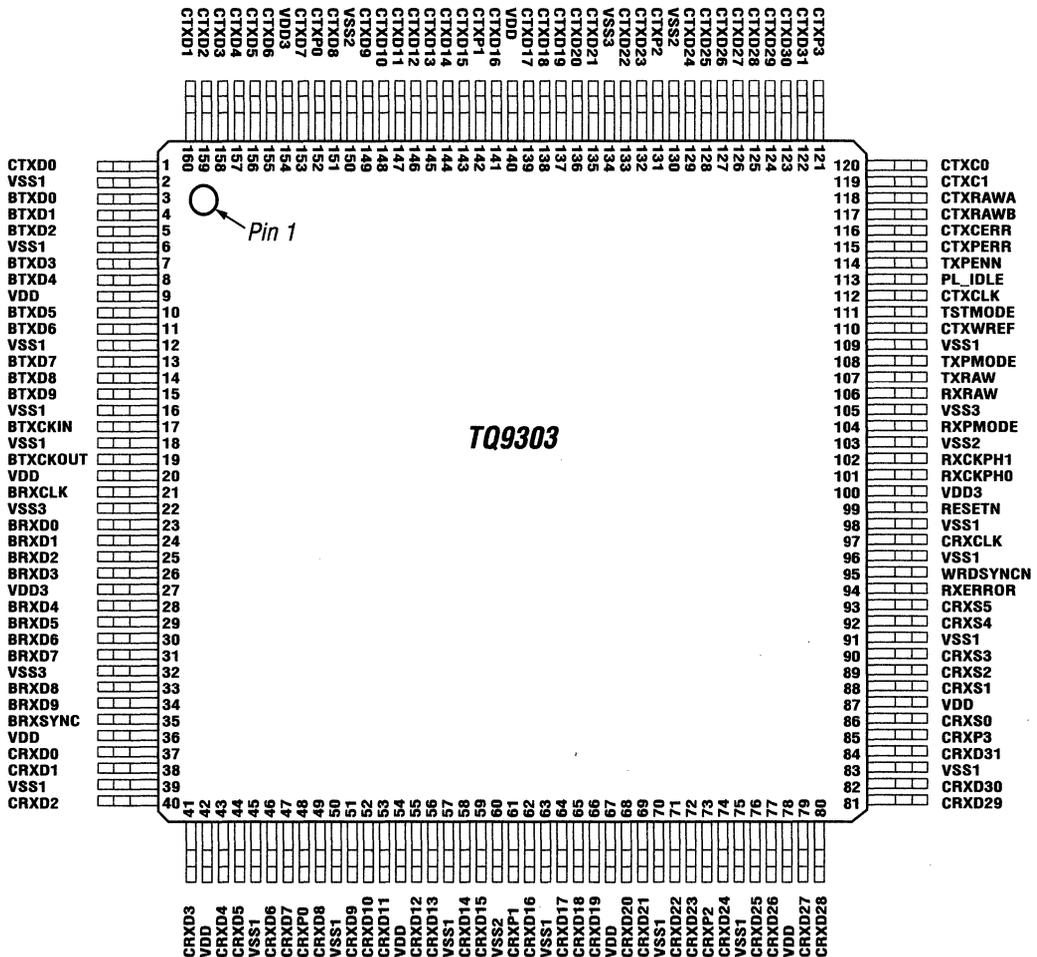
The Clock Generator generates CRXCLK, a word clock, which is used for clocking the host I/O registers. The user may place the clock edge, CRXCLK, in four places relative to the word input, thereby giving the user control of setup and hold times. Clock edge placement is selected via control pins RXCKPH0 and RXCKPH1 (Receiver Clock Phase). CRXCLK runs at 26.5625 MHz using FC1063 and 13.28125 MHz using FC531.

The Clock Generator also receives the BRXSYNC signal, which is used for byte alignment. The Receiver drives BRXSYNC high when detecting a K28.5 character.

Raw Mode Receive

In Raw Mode Receive where RXRAW is high for the whole frame, the input data word bypasses the parity check, ordered set generator, 32-bit CRC, and 8b/10b encoder, and is directly converted to data words. The byte-to-word mapping of data is listed in Table 1.

Figure 6. Pinout



DATACOM
 PRODUCTS

TQ9303

Table 4. Pin Names

<i>Pin</i>	<i>Description</i>	<i>Pin</i>	<i>Description</i>	<i>Pin</i>	<i>Description</i>	<i>Pin</i>	<i>Description</i>
1	CTXD0	41	CRXD3	81	CRXD29	121	CTXP3
2	VSS	42	VDD	82	CRXD30	122	CTXD31
3	BTXD0	43	CRXD4	83	VSS	123	CTXD30
4	BTXD1	44	CRXD5	84	CRXD31	124	CTXD29
5	BTXD2	45	VSS	85	CRXP3	125	CTXD28
6	VSS	46	CRXD6	86	CRXS0	126	CTXD27
7	BTXD3	47	CRXD7	87	VDD	127	CTXD26
8	BTXD4	48	CRXP0	88	CRXS1	128	CTXD25
9	VDD	49	CRXD8	89	CRXS2	129	CTXD24
10	BTXD5	50	VSS	90	CRXS3	130	VSS
11	BTXD6	51	CRXD9	91	VSS	131	CTXP2
12	VSS	52	CRXD10	92	CRXS4	132	CTXD23
13	BTXD7	53	CRXD11	93	CRXS5	133	CTXD22
14	BTXD8	54	VDD	94	RXERROR	134	VSS
15	BTXD9	55	CRXD12	95	WRDSYNCN	135	CTXD21
16	VSS	56	CRXD13	96	VSS	136	CTXD20
17	BTXCKIN	57	VSS	97	CRXCLK	137	CTXD19
18	VSS	58	CRXD14	98	VSS	138	CTXD18
19	BTXCKOUT	59	CRXD15	99	RESETN	139	CTXD17
20	VDD	60	VSS	100	VDD	140	VDD
21	BRXCLK	61	CRXP1	101	RXCKPH0	141	CTXD16
22	VSS	62	CRXD16	102	RXCKPH1	142	CTXP1
23	BRXD0	63	VSS	103	VSS	143	CTXD15
24	BRXD1	64	CRXD17	104	RXPmode	144	CTXD14
25	BRXD2	65	CRXD18	105	VSS	145	CTXD13
26	BRXD3	66	CRXD19	106	RXRAW	146	CTXD12
27	VDD	67	VDD	107	TXRAW	147	CTXD11
28	BRXD4	68	CRXD20	108	TXPmode	148	CTXD10
29	BRXD5	69	CRXD21	109	VSS	149	CTXD9
30	BRXD6	70	VSS	110	CTXWREF	150	VSS
31	BRXD7	71	CRXD22	111	TSTmode	151	CTXD8
32	VSS	72	CRXD23	112	CTXCLK	152	CTXP0
33	BRXD8	73	CRXP2	113	PL_IDLE	153	CTXD7
34	BRXD9	74	CRXD24	114	TXPENN	154	VDD
35	BRXSYNC	75	VSS	115	CTXPERR	155	CTXD6
36	VDD	76	CRXD25	116	CTXCERR	156	CTXD5
37	CRXD0	77	CRXD26	117	CTXRAWB	157	CTXD4
38	CRXD1	78	VDD	118	CTXRAWA	158	CTXD3
39	VSS	79	CRXD27	119	CTXC1	159	CTXD2
40	CRXD2	80	CRXD28	120	CTXC0	160	CTXD1

Table 5. Pin Descriptions

Symbol	I/O	# of I/O	Interface	Description	Pin Numbers
BTXCKIN	I	1	Transmitter	Takes clock from Transmitter to generate BTXCKOUT.	17
BTXCKOUT	O	1	Transmitter	Used by Transmitter to clock in BTXD0..9.	19
BTXD0..9	O	10	Transmitter	Data Output.	3-5, 7, 8, 10, 11, 13-15
CTXWREF	O	1	Host	Reference Word Clock which can be used in signaling the host to issue a CTXCLK.	110
CTXCLK	I	1	Host	Word Clock generated from CTXCLK to clock in/out host I/O registers. The following signals are latched by CTXCLK: CTXP0..3, CTXC0,1, CTXRAW, CTXPENN, CTXPMODE, CTXPERR, CTXCERR.	112
CTXC0	I	1	Host	High indicates CTXD0..31 is an Ordered Set; Low indicates data.	120
CTXC1	I	1	Host	High generates CRC; low checks CRC.	119
CTXD0..31	I	32	Host	Transmit data output (CTXD31 = MSB; CTXD0 = LSB).	1, 160-155, 153-151, 149-143, 141, 139-135, 133, 132, 129-122
CTXP0	I	1	Host	CTXD0..7 Odd Parity input.	152
CTXP1	I	1	Host	CTXD8..15 Odd Parity input.	142
CTXP2	I	1	Host	CTXD16..23 Odd Parity input.	131
CTXP3	I	1	Host	CTXD24..31 and optional CTXC0 Odd Parity input. If TXPMODE is high, CTP3 checks parity for CTXD24..31 and CTXC0. If TXPMODE is low, CTP3 checks parity for CTXD24..31 only.	121
CTXRAWA	I	1	Host	Raw data bit 19.	118
CTXRAWB	I	1	Host	Raw data bit 9.	117
CTXPERR	O	1	Host	CTXPERR high indicates CTXD0..31 Parity Error.	115
CTXCERR	O	1	Host	CTXCERR high indicates CRC Error. When in CRC Check mode, CTXC1 is low.	116
TSTMODE	I	1	Host	Normally GND. HIGH state used by vendor to monitor delay and threshold.	111
TXRAW	I	1	Host	High selects Raw Transmit Data mode.	107
TXPENN	I	1	Host	Active Low Transmit Parity Enable; Tx checks Parity when low.	114
TXPMODE	I	1	Host	If TXPMODE is high, CTP3 generates parity for CTXD24..31 and CTXC0. If TXPMODE is low, CTP3 generates parity for CTXD24..31 only.	108
PL_IDLE	I	1	Host	Proprietary link idle control	113
BRXCLK	I	1	Receiver	Driven by RXCLK. Clocks data from BRXD0..9.	21
BRXD0..9	I	10	Receiver	Receives RXD0..9 from Receiver.	23-26, 28-31, 33, 34
BRXSYNC	I	1	Receiver	SYNC.	35
CRXCLK	O	1	Host	CRXCLK latches CRXD0..31.	97

(Continued on next page)

TQ9303

Table 5. Pin Descriptions (continued)

Symbol	I/O	# of I/O	Interface	Description	Pin Numbers
CRXD0..31	0	32	Host	Receive data output (CRXD31 = MSB; CRXD0 = LSB).	37,38,40,41,43,44, 46,47,49,51–53,55, 56,58,59,62,64–66, 68,69,71,72,74, 76,77,79–82,84
CRXS0	0	1	Host	High indicates CRXD0..31 is an Ordered Set; Low indicates data.	86
CRXS1	0	1	Host	CRC error flag; high indicates a CRC error.	88
CRXS2,3	0	2	Host	Line state status bits. State equivalent for CRXS3 and CRXS2 from left to right, respectively: 00 - No State 01 - Pending 10 - State Rec. 11 - Bad Seq.	89,90
CRXS4,5	0	2	Host	Line state ID bits.	92,93
CRXP0	0	1	Host	CRXD0..7 Odd Parity output.	48
CRXP1	0	1	Host	CRXD8..15 Odd Parity output.	61
CRXP2	0	1	Host	CRXD16..23 Odd Parity output.	73
CRXP3	0	1	Host	CRXD24..31 and optional CRXS01 Odd Parity output. If RXPMODE is high, CRXP3 generates Parity for CRXD24..31 and CRXS0. If RXPMODE is low, CRXP3 generates Parity for CRXD24..31 only.	85
RXERROR	0	1	Host	Receive Error; high indicates invalid data from the Receiver.	94
RXRAW	1	1	Host	High selects Raw Receive Data mode.	106
WRDSYNCN	0	1	Host	Word Synchronization Status Flag; Low indicates Synchronization acquired. Can be connected to SYNCEN on TQ9502/GA9102 Receiver.	95
RXPMODE	1	1	Host	Receiver Parity mode. If RXPMODE is high, CRXP3 generates Parity for CRXD24..31 and CRXS0. If RXPMODE is low, CRXP3 generates Parity for CRXD24..31 only.	104
RXCKPH0,1	1	2	Host	CRXCLK Phase Select pin.	101,102
RESETN	1	1	Host	Active low.	99
VDD	—	—	—	+5 Volt supply.	9,20,27,36,42,54,67, 78,87,100,140,154
GND (V _{SS})	—	—	—	Ground.	2,6,12,16,18,22,32,39, 45,50,57,60,63,70,75, 83,91,96,98,103,105, 109,111,130,134,150

Table 6. Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
Storage temperature	-65	+150	°C
Ambient temperature	-55	+125	°C
Supply voltage to ground	-0.5	+7.0	V
DC input voltage	-0.5	$V_{DD} + 0.5$	V
DC input current	-30	+5	mA
Thermal resistance (θ_{JC})		5.6	°C / W

Note: Exceeding the absolute maximum ratings may damage the device.

Table 7. Operating Conditions

Parameter	Range	Unit
Supply voltage	+5 ± 5%	V
Ambient temperature	0-70	°C
Power @ 125 MHz	4.1	W
Power @ DC	0.3	W

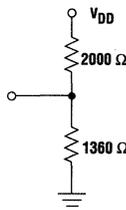
Note: Proper functionality is guaranteed under these conditions.

Table 8. DC Characteristics

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
V_{OH}	Output high voltage	$V_{DD} = \text{Min}$, $I_{OH} = -4 \text{ mA}$, $V_{IN} = V_{IH}$ or V_{IL}	3.6			V
V_{OL}	Output low voltage	$V_{DD} = \text{Min}$, $I_{OL} = 4 \text{ mA}$, $V_{IN} = V_{IH}$ or V_{IL}			0.37	V
V_{IH}	Input high level	Guaranteed input logical high voltage for all inputs	2.0			V
V_{IL}	Input low level	Guaranteed input logical low voltage for all inputs			0.8	V
I_{IL}	Input Leakage current	$V_{DD} = \text{Max}$, $V_{IN} = 0.40\text{V}$		-150	-400	μA

- Notes:
- Unless otherwise specified, these values apply over the recommended operating range.
 - Typical limits are: $V_{DD} = 5.0 \text{ V}$ and $T_A = 25 \text{ }^\circ\text{C}$.
 - Input levels (V_{IH} and V_{IL}) are absolute values with respect to device ground, and all overshoots due to system or tester noise are included.
 - V_{IN} , the TTL input, can be high or low.

TTL Test Load, TLL Outputs



TQ9303

Table 9. AC Characteristics—Transmit (CTX) Timing

Parameter	Description	Abs.Min.	Rel.Min.	Abs.Max.	Rel.Max.	Unit
T1	CTXCLK Pulse Width High	12	t + 4		3t - 4	ns
T2	CTXCLK Pulse Width Low	12	t + 4		3t - 4	ns
T3	CTXCLK Period	32	4t		4t	ns
T4	CTXD(0..31), CTXP(0..3), CTXRAWA, CTXRAWB, CTXPENN, CTXPMOD, CTXC0, and CTXRAW-to-CTXCLK↑ setup time	1.9				ns
T5	CTXCLK↑-to-CTXD(0..31), CTXP(0..3), CTXRAWA, CTXRAWB, CTXPENN, CTXPMOD, CTXC0, and CTXRAW hold time	0.9				ns
T6	CTXC0 and CTXC1-to-CTXCLK↑ setup time	0.8				ns
T7	CTXCLK↑-to-CTXC0 and CTXC1 hold time	2				ns
T8	CTXCLK↑-to-CTXCERR and CTXPERR Output	2.5		15.5		ns

Notes:

- "t" represents one (1) BTXCKIN period.
- Minimum setup and hold times are based on a 30-pf load on all outputs and a 50% duty cycle on CTXCLK.

Figure 7. Transmit (CTX) Timing

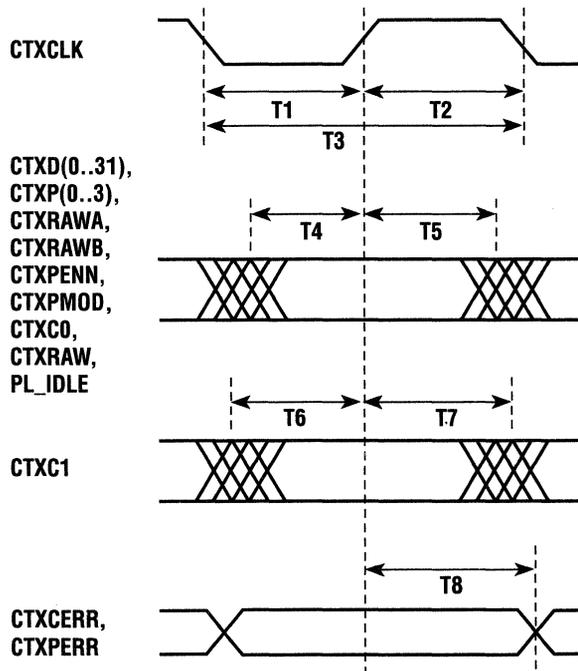
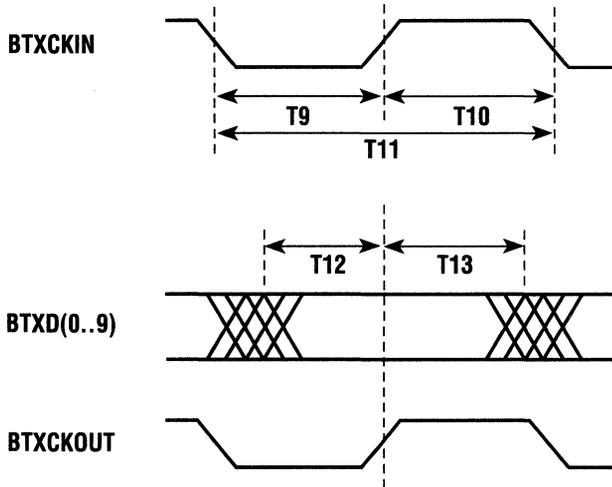


Table 10. AC Characteristics—Transmit (BTX) Timing ⁽¹⁾

Parameter	Description	Abs.Min.	Rel.Min.	Abs.Max.	Rel.Max.	Unit
T9	BTXCKN Pulse Width High	3.2	0.4t		0.6t	ns
T10	BTXCKIN Pulse Width Low	3.2	0.4t		0.6t	ns
T11	BTXCKIN Period	8	t		t	ns
T12	BTXD(0..9)-to-BTXCKOUT↑ setup time	(2)	(2)	(2)	(2)	
T13	BTXCKOUT↑-to-BTXD(0..9) hold time	(2)	(2)	(2)	(2)	

Notes: 1. "t" represents one (1) BTXCKIN period.
 2. See Table 11, "Transmit (BTX) Timing Formulas," below.

Figure 8. Transmit (BTX) Timing



DATACOM
 PRODUCTS

Table 11. Transmit (BTX) Timing Formulas

Parameter	Formula	t = 8 ns (125 MHz)	t = 9.41 ns (106.25 MHz)	t = 16 ns (62.5 MHz)	t = 18.821 ns (53.125 MHz)
T12	$d * t - 1.94 \text{ ns}$	2.06 ns (1.8 ns min.)	2.76 ns (2.5 ns min.)	6.06 ns	7.47 ns
T13	$(1 - d) * t - 1.42 \text{ ns}$	2.58 ns (3.4 ns min.)	3.28 ns (2.1 ns min.)	6.58 ns	7.99 ns

Note: "d" represents one (1) BTXCKIN duty cycle, $T9 / T11$ or $T9 / (T9 + T10)$. The calculations given above are made with $d = 0.5$ (50%). When BTXCKIN has other than a 50% duty cycle ($d > 0.5$), T_{SETUP} and T_{HOLD} are affected by the shift in clock edges. The rising edge of BTXCKOUT is triggered by the falling edge of BTXCKIN; thus, if the BTXCKIN high time is 2 ns less than the BTXCKIN low time, then 1 ns must be subtracted from the setup times given above, and 1 ns must be added to the hold times given above.

Table 12. AC Characteristics—Receive (BRX) Timing

Parameter	Description	Abs.Min.	Rel.Min.	Abs.Max.	Rel.Max.	Unit
T14	BRXCLK Pulse Width High	3.2	0.4t		0.6t	ns
T15	BRXCLK Pulse Width Low	3.2	0.4t		0.6t	ns
T16	BRXCLK Period	8	t		t	ns
T17	BRXD(0..9) and BRXSYNC-to-BTXCKOUT↑ setup time	1.25				ns
T18	BRXCLK↑-to-BRXD(0..9) and BRXSYNC hold time	0.25				ns

Note: "t" represents one (1) BRXCLK period.

Figure 9. Receive (BRX) Timing

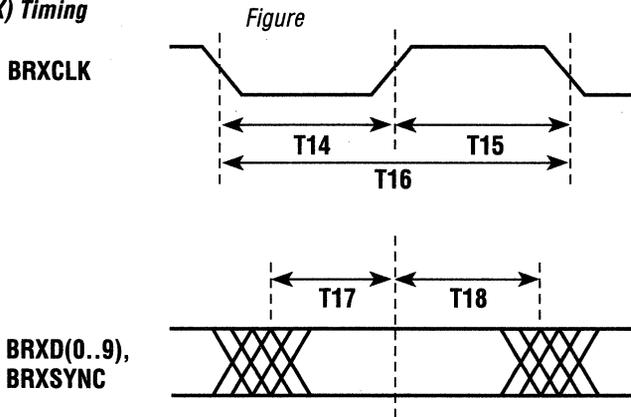
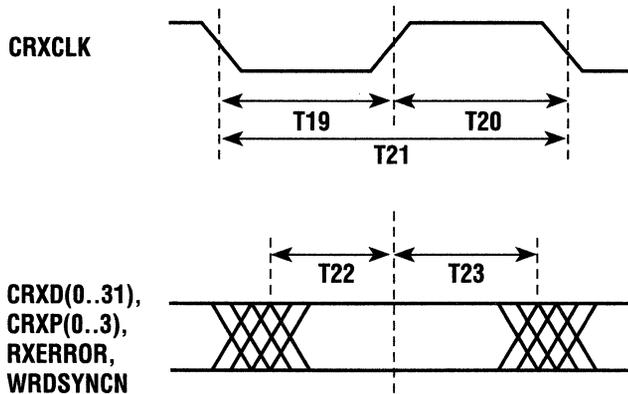


Table 13. AC Characteristics—Receive (CRX) Timing ⁽¹⁾

Parameter	Description	Abs.Min.	Rel.Min.	Abs.Max.	Rel.Max.	Unit
T9	CRXCLK Pulse Width High	13	2t – 3	19	2t + 3	ns
T10	CRXCLK Pulse Width Low	13	2t – 3	19	2t + 3	ns
T11	CRXCLK Period	32	4t		4t	ns
T12	CRXD*, CRXP*, and CRXS*–to–CRXCLK↑ setup time	(2)	(2)	(2)	(2)	
T13	CRXCLK↑–to–CRXD*, CRXP*, and CRXS* hold time	(2)	(2)	(2)	(2)	

Notes: 1. “t” represents one (1) BRXCLK period.
 2. See Table 14, “Receive (CRX) Timing Formulas,” below.

Figure 10. Receive (CRX) Timing



DATACOM
 PRODUCTS

Table 14. Receive (CRX) Timing Formulas

Parameter	RXCKPH(1:0)	Formula	t = 8 ns (125 MHz)	t = 9.41 ns (106.25 MHz)	t = 16 ns (62.5 MHz)	t = 18.821 ns (53.125 MHz)
	0:0	0.054t – 0.94 ns	–0.47 ns	–0.39 ns	0.00 ns	0.16 ns
	0:1	1.054t – 0.94 ns	7.53 ns	9.02 ns	16.00 ns	18.99 ns
	1:0	2.054t – 0.94 ns	15.53 ns	18.43 ns	32.00 ns	37.81 ns
	1:1	3.054t – 0.94 ns	23.53 ns	27.84 ns	48.00 ns	56.63 ns
	0:0	3.5t – 0.07 ns	28.07 ns	33.01 ns	56.07 ns	65.95 ns
	0:1	2.5t – 0.07 ns	20.07 ns	23.59 ns	40.07 ns	47.12 ns
	1:0	1.5t – 0.07 ns	12.07 ns	14.18 ns	24.07 ns	28.30 ns
	1:1	0.5t – 0.07 ns	4.07 ns	4.77 ns	8.07 ns	9.48 ns

TQ9303

Table A-1. Valid Data Characters

Data Byte Name	HGF	Bits EDCBA ¹	Current abcdei	RD – fghj ²	Current abcdei	RD + fghj ²	Data Byte Name	HGF	Bits EDCBA ¹	Current abcdei	RD – fghj ²	Current abcdei	RD + fghj ²
D0.0	000	00000	100111	0100	011000	1011	D7.2	010	00111	111000	0101	000111	0101
D1.0	000	00001	011101	0100	100010	1011	D8.2	010	01000	111001	0101	000110	0101
D2.0	000	00010	101101	0100	010010	1011	D9.2	010	01001	100101	0101	100101	0101
D3.0	000	00011	110001	1011	110001	0100	D10.2	010	01010	010101	0101	010101	0101
D4.0	000	00100	110101	0100	001010	1011	D11.2	010	01011	111000	0101	110100	0101
D5.0	000	00101	101001	1011	101001	0100	D12.2	010	01100	001101	0101	001101	0101
D6.0	000	00110	011001	1011	011001	0100	D13.2	010	01101	101100	0101	101100	0101
D7.0	000	00111	111000	1011	000111	0100	D14.2	010	01110	011100	0101	011100	0101
D8.0	000	01000	111001	0100	000110	1011	D15.2	010	01111	011011	0101	101000	0101
D9.0	000	01001	100101	1011	100101	0100	D16.2	010	10000	011011	0101	100100	0101
D10.0	000	01010	101010	1011	010101	0100	D17.2	010	10001	100011	0101	100011	0101
D11.0	000	01011	111000	1011	110100	0100	D18.2	010	10010	010011	0101	010011	0101
D12.0	000	01100	001101	1011	001101	0100	D19.2	010	10011	110010	0101	110010	0101
D13.0	000	01101	101100	1011	101100	0100	D20.2	010	10100	001011	0101	001011	0101
D14.0	000	01110	011100	1011	011100	0100	D21.2	010	10101	101010	0101	101010	0101
D15.0	000	01111	010111	0100	101000	1011	D22.2	010	10110	011010	0101	011010	0101
D16.0	000	10000	011011	0100	100100	1011	D23.2	010	10111	111010	0101	000101	0101
D17.0	000	10001	100011	1011	100011	0100	D24.2	010	11000	110011	0101	001100	0101
D18.0	000	10010	010011	1011	010011	0100	D25.2	010	11001	100110	0101	100110	0101
D19.0	000	10011	110010	1011	110010	0100	D26.2	010	11010	010110	0101	010110	0101
D20.0	000	10100	001011	1011	001011	0100	D27.2	010	11011	110110	0101	001001	0101
D21.0	000	10101	101010	1011	101010	0100	D28.2	010	11100	001110	0101	001110	0101
D22.0	000	10110	011010	1011	011010	0100	D29.2	010	11101	011110	0101	010001	0101
D23.0	000	10111	111010	0100	000101	1011	D30.2	010	11110	011110	0101	100001	0101
D24.0	000	11000	110011	0100	001100	1011	D31.2	010	11111	101011	0101	010100	0101
D25.0	000	11001	100110	1011	100110	0100	D0.3	011	00000	100111	0011	011000	1100
D26.0	000	11010	010110	1011	010110	0100	D1.3	011	00001	011101	0011	100010	1100
D27.0	000	11011	111010	0100	001001	1011	D2.3	011	00010	101101	0011	010010	1100
D28.0	000	11100	001110	1011	001110	0100	D3.3	011	00011	110001	1100	110001	0011
D29.0	000	11101	101110	0100	010001	1011	D4.3	011	00100	110101	0011	001010	1100
D30.0	000	11110	011110	0100	100001	1011	D5.3	011	00101	101001	1100	101001	0011
D31.0	000	11111	101011	0100	010100	1011	D6.3	011	00110	011001	1100	011001	0011
D0.1	001	00000	100111	0001	011000	1001	D7.3	011	00111	111000	1100	000111	0011
D1.1	001	00001	011101	0001	100010	1001	D8.3	011	01000	111001	0011	000110	1100
D2.1	001	00010	101101	0001	010010	1001	D9.3	011	01001	100101	1100	100101	0011
D3.1	001	00011	110001	0001	110001	1001	D10.3	011	01010	010101	1100	010101	0011
D4.1	001	00100	110101	0001	001010	1001	D11.3	011	01011	110100	1100	110100	0011
D5.1	001	00101	101001	0001	101001	1001	D12.3	011	01100	001101	1100	001101	0011
D6.1	001	00110	011001	0001	011001	1001	D13.3	011	01101	101100	1100	101100	0011
D7.1	001	00111	111000	0001	000111	1001	D14.3	011	01110	011100	1100	011100	0011
D8.1	001	01000	111001	0001	000110	1001	D15.3	011	01111	011011	0011	101000	1100
D9.1	001	01001	100101	0001	100101	1001	D16.3	011	10000	011011	0011	100100	1100
D10.1	001	01010	101010	0001	010101	1001	D17.3	011	10001	100011	1100	100011	0011
D11.1	001	01011	111000	0001	110100	1001	D18.3	011	10010	010011	1100	010011	0011
D12.1	001	01100	001101	0001	001101	1001	D19.3	011	10011	110010	1100	110010	0011
D13.1	001	01101	101100	0001	101100	1001	D20.3	011	10100	001011	1100	001011	0011
D14.1	001	01110	011100	0001	011100	1001	D21.3	011	10101	101010	1100	101010	0011
D15.1	001	01111	010111	0001	101000	1001	D22.3	011	10110	011010	1100	011010	0011
D16.1	001	10000	011011	0001	100100	1001	D23.3	011	10111	111010	0011	000101	1100
D17.1	001	10001	100011	0001	100011	1001	D24.3	011	11000	110011	0011	001100	1100
D18.1	001	10010	010011	0001	010011	1001	D25.3	011	11001	100110	1100	100110	0011
D19.1	001	10011	110010	0001	110010	1001	D26.3	011	11010	010110	1100	010110	0011
D20.1	001	10100	001011	0001	001011	1001	D27.3	011	11011	110110	0011	001001	1100
D21.1	001	10101	101010	0001	101010	1001	D28.3	011	11100	001110	1100	001110	0011
D22.1	001	10110	011010	0001	011010	1001	D29.3	011	11101	011110	0011	010001	1100
D23.1	001	10111	111010	0001	000101	1001	D30.3	011	11110	011110	0011	100001	1100
D24.1	001	11000	110011	0001	001100	1001	D31.3	011	11111	101011	0011	010100	1100
D25.1	001	11001	100110	0001	100110	1001	D0.4	100	00000	100111	0010	011000	1101
D26.1	001	11010	010110	0001	010110	1001	D1.4	100	00001	011101	0010	100010	1101
D27.1	001	11011	111010	0001	001001	1001	D2.4	100	00010	101101	0010	010010	1101
D28.1	001	11100	001110	0001	001110	1001	D3.4	100	00011	110001	1101	110001	0010
D29.1	001	11101	101110	0001	010001	1001	D4.4	100	00100	110101	0010	001010	1101
D30.1	001	11110	011110	0001	100001	1001	D5.4	100	00101	101001	1101	101001	0010
D31.1	001	11111	101011	0001	010100	1001	D6.4	100	00110	011001	1101	011001	0010
D0.2	010	00000	100111	0101	011000	0101	D7.4	100	00111	111000	1101	000111	0010
D1.2	010	00001	011101	0101	100010	0101	D8.4	100	01000	111001	0010	000110	1101
D2.2	010	00010	101101	0101	010010	0101	D9.4	100	01001	100101	1101	100101	0010
D3.2	010	00011	110001	0101	110001	0101	D10.4	100	01010	010101	1101	010101	0010
D4.2	010	00100	110101	0101	001010	0101	D11.4	100	01011	110100	1101	110100	0010
D5.2	010	00101	101001	0101	101001	0101	D12.4	100	01100	001101	1101	001101	0010
D6.2	010	00110	011001	0101	011001	0101	D13.4	100	01101	101100	1101	101100	0010

Notes: 1. "HGF, EDCBA" corresponds to data inputs CTXD7–CTXD0, in that order.
 2. "abcdei, fghj" corresponds to BTXD9–BTXD0, in that order; "a" is to be transmitted first, followed by "b," "c," ... "j."

Table A-1. Valid Data Characters (continued)

Data Byte Name	HGF	Bits EDCBA ¹	Current abcdei	RD - fghj ²	Current abcdei	RD + fghj ²
D14.4	100	01110	011100	1101	011100	0010
D15.4	100	01111	010111	0010	101000	1101
D16.4	100	10000	011011	0010	100100	1101
D17.4	100	10001	100011	1101	100011	0010
D18.4	100	10010	010011	1101	010011	0010
D19.4	100	10011	110010	1101	110010	0010
D20.4	100	10100	001011	1101	001011	0010
D21.4	100	10101	101010	1101	101010	0010
D22.4	100	10110	011010	1101	011010	0010
D23.4	100	10111	111010	0010	000101	1101
D24.4	100	11000	110011	0010	001100	1101
D25.4	100	11001	100110	1101	100110	0010
D26.4	100	11010	010110	1101	010110	0010
D27.4	100	11011	110110	0010	001001	1101
D28.4	100	11100	001110	1101	001110	0010
D29.4	100	11101	101110	0010	010001	1101
D30.4	100	11110	011110	0010	100001	1101
D31.4	100	11111	101111	0010	010100	1101
D0.5	101	00000	000111	1010	011000	1010
D1.5	101	00001	011101	1010	100010	1010
D2.5	101	00010	101101	1010	010010	1010
D3.5	101	00011	110001	1010	110001	1010
D4.5	101	00100	110101	1010	001010	1010
D5.5	101	00101	101001	1010	101001	1010
D6.5	101	00110	011001	1010	011001	1010
D7.5	101	00111	111000	1010	000111	1010
D8.5	101	01000	111001	1010	000110	1010
D9.5	101	01001	100101	1010	100101	1010
D10.5	101	01010	010101	1010	010101	1010
D11.5	101	01011	110100	1010	110100	1010
D12.5	101	01100	001101	1010	001101	1010
D13.5	101	01101	101100	1010	101100	1010
D14.5	101	01110	011100	1010	011100	1010
D15.5	101	01111	101110	1010	101000	1010
D16.5	101	10000	011011	1010	100100	1010
D17.5	101	10001	100011	1010	100011	1010
D18.5	101	10010	010011	1010	010011	1010
D19.5	101	10011	110010	1010	110010	1010
D20.5	101	10100	001011	1010	001011	1010
D21.5	101	10101	101010	1010	101010	1010
D22.5	101	10110	011010	1010	011010	1010
D23.5	101	10111	111010	1010	000101	1010
D24.5	101	11000	110011	1010	001100	1010
D25.5	101	11001	100110	1010	100110	1010
D26.5	101	11010	010110	1010	010110	1010
D27.5	101	11011	110110	1010	001001	1010
D28.5	101	11100	001110	1010	001110	1010
D29.5	101	11101	101110	1010	010001	1010
D30.5	101	11110	011110	1010	100001	1010
D31.5	101	11111	101111	1010	010100	1010
D0.6	110	00000	000111	0110	011000	0110
D1.6	110	00001	011101	0110	100010	0110
D2.6	110	00010	101101	0110	010010	0110
D3.6	110	00011	110001	0110	110001	0110
D4.6	110	00100	110101	0110	001010	0110
D5.6	110	00101	101001	0110	101001	0110
D6.6	110	00110	011001	0110	011001	0110
D7.6	110	00111	111000	0110	000111	0110
D8.6	110	01000	111001	0110	000110	0110
D9.6	110	01001	100101	0110	100101	0110
D10.6	110	01010	010101	0110	010101	0110
D11.6	110	01011	110100	0110	110100	0110
D12.6	110	01100	001101	0110	001101	0110
D13.6	110	01101	101100	0110	101100	0110
D14.6	110	01110	011100	0110	011100	0110
D15.6	110	01111	101110	0110	101000	0110
D16.6	110	10000	011011	0110	100100	0110
D17.6	110	10001	100011	0110	100011	0110
D18.6	110	10010	010011	0110	010011	0110
D19.6	110	10011	110010	0110	110010	0110
D20.6	110	10100	001011	0110	001011	0110
D21.6	110	10101	101010	0110	101010	0110
D22.6	110	10110	011010	0110	011010	0110
D23.6	110	10111	111010	0110	000101	0110
D24.6	110	11000	110011	0110	100011	0110
D25.6	110	11001	100110	0110	100110	0110
D26.6	110	11010	010110	0110	010110	0110
D27.6	110	11011	110110	0110	001001	0110
D28.6	110	11100	001110	0110	001110	0110
D29.6	110	11101	101110	0110	010001	0110
D30.6	110	11110	011110	0110	100001	0110
D31.6	110	11111	101111	0110	010100	0110

DATACOM PRODUCTS

Table A-2. Valid Special Characters

Special Code Name	Current abcdei	RD - fghj ⁽²⁾	Current abcdei	RD + fghj ⁽²⁾
K28.0	001111	0100	110000	1011
K28.1	001111	1001	110000	0110
K28.2	001111	0101	110000	1010
K28.3	001111	0011	110000	1100
K28.4	001111	0010	110000	1101
K28.5	001111	1010	110000	0101
K28.6	001111	0110	110000	1001
K28.7	001111	1000	110000	0111
K23.7	111010	1000	000101	0111
K27.7	101110	1000	001001	0111
K29.7	101110	1000	010001	0111
K30.7	011110	1000	100001	0111

Notes: 1. "HGF, EDCBA" corresponds to data inputs CTXD7-CTXD0, in that order.

2. "abcdei, fghj" corresponds to BTXD9-BTXD0, in that order. "a" is to be transmitted first, followed by "b," "c," ... "j."

TQ9303

Table B-1. TQ9303 Encoding

Ordered Set	32-Bit Word Encoder Input								Beg. RD	Ordered Set Output
	31 Cntl	30 Sig	29 SOF	28 EOF	27:24 Type	23:16	15:8	7:0		
SOFn1 ³	0	0	1	0	0001	$\bar{1}$	$\bar{1}$	$\bar{1}$	Neg	(K28.5–D21.5–D23.1–D23.1)
SOFn2	0	0	1	0	0010	$\bar{1}$	$\bar{1}$	$\bar{1}$	Neg	(K28.5–D21.5–D21.1–D21.1)
SOFn3	0	0	1	0	0011	$\bar{1}$	$\bar{1}$	$\bar{1}$	Neg	(K28.5–D21.5–D22.1–D22.1)
SOFi1	0	0	1	0	0101	$\bar{1}$	$\bar{1}$	$\bar{1}$	Neg	(K28.5–D21.5–D23.2–D23.2)
SOFi2	0	0	1	0	0110	$\bar{1}$	$\bar{1}$	$\bar{1}$	Neg	(K28.5–D21.5–D21.2–D21.2)
SOFi3	0	0	1	0	0111	$\bar{1}$	$\bar{1}$	$\bar{1}$	Neg	(K28.5–D21.5–D22.2–D22.2)
SOFc1	0	0	1	0	1101	$\bar{1}$	$\bar{1}$	$\bar{1}$	Neg	(K28.5–D21.5–D23.0–D23.0)
SOFf	0	0	1	0	1000	$\bar{1}$	$\bar{1}$	$\bar{1}$	Neg	(K28.5–D21.5–D24.2–D24.2)
EOFn ^{4,5}	0	0	0	1	0000	$\bar{1}$	$\bar{1}$	$\bar{1}$	Neg	(K28.5–D21.4–D21.6–D21.6)
									Pos	(K28.5–D21.5–D21.6–D21.6)
EOFt ⁵	0	0	0	1	0100	$\bar{1}$	$\bar{1}$	$\bar{1}$	Neg	(K28.5–D21.4–D21.3–D21.3)
									Pos	(K28.5–D21.5–D21.3–D21.3)
EOFdt ⁶	0	0	0	1	1100	$\bar{1}$	$\bar{1}$	$\bar{1}$	Neg	(K28.5–D21.4–D21.4–D21.4)
									Pos	(K28.5–D21.5–D21.4–D21.4)
EOFa	0	0	0	1	1001	$\bar{1}$	$\bar{1}$	$\bar{1}$	Neg	(K28.5–D21.4–D21.7–D21.7)
									Pos	(K28.5–D21.5–D21.7–D21.7)
EOFni	0	0	0	1	0001	$\bar{1}$	$\bar{1}$	$\bar{1}$	Neg	(K28.5–D10.4–D21.6–D21.6)
									Pos	(K28.5–D10.5–D21.6–D21.6)
EOFdti	0	0	0	1	1101	$\bar{1}$	$\bar{1}$	$\bar{1}$	Neg	(K28.5–D10.4–D21.4–D21.4)
									Pos	(K28.5–D10.5–D21.4–D21.4)
Idle ⁷	0	1	0	0	0000	$\bar{1}$	$\bar{1}$	$\bar{1}$	Neg	(K28.5–D21.4–D21.5–D21.5)
R-Rdy ⁷	0	1	0	0	0110	$\bar{1}$	$\bar{1}$	$\bar{1}$	Neg	(K28.5–D21.4–D10.2–D10.2)
NOS ⁷	0	1	0	0	1000	$\bar{1}$	$\bar{1}$	$\bar{1}$	Neg	(K28.5–D21.2–D31.5–D5.2)
OLS ⁷	0	1	0	0	1001	$\bar{1}$	$\bar{1}$	$\bar{1}$	Neg	(K28.5–D21.1–D10.4–D21.2)
LR ⁷	0	1	0	0	1010	$\bar{1}$	$\bar{1}$	$\bar{1}$	Neg	(K28.5–D9.2–D31.5–D9.2)
LRR ⁷	0	1	0	0	1011	$\bar{1}$	$\bar{1}$	$\bar{1}$	Neg	(K28.5–D21.1–D31.5–D9.2)
Undefined	1	0	0	0	0000	(XY _B) ²	(XY _C) ²	(XY _D) ²		(K28.0–DX.Y _B –DX.Y _C –DX.Y _D)
Undefined	1	0	0	0	0001	(XY _B) ²	(XY _C) ²	(XY _D) ²		(K28.1–DX.Y _B –DX.Y _C –DX.Y _D)
Undefined	1	0	0	0	0010	(XY _B) ²	(XY _C) ²	(XY _D) ²		(K28.2–DX.Y _B –DX.Y _C –DX.Y _D)
Undefined	1	0	0	0	0011	(XY _B) ²	(XY _C) ²	(XY _D) ²		(K28.3–DX.Y _B –DX.Y _C –DX.Y _D)
Undefined	1	0	0	0	0100	(XY _B) ²	(XY _C) ²	(XY _D) ²		(K28.4–DX.Y _B –DX.Y _C –DX.Y _D)
Undefined	1	0	0	0	0101	(XY _B) ²	(XY _C) ²	(XY _D) ²		(K28.5–DX.Y _B –DX.Y _C –DX.Y _D)
Undefined	1	0	0	0	0110	(XY _B) ²	(XY _C) ²	(XY _D) ²		(K28.6–DX.Y _B –DX.Y _C –DX.Y _D)
Undefined	1	0	0	0	0111	(XY _B) ²	(XY _C) ²	(XY _D) ²		(K28.7–DX.Y _B –DX.Y _C –DX.Y _D)
Undefined	1	0	0	0	1000	(XY _B) ²	(XY _C) ²	(XY _D) ²		(K23.7–DX.Y _B –DX.Y _C –DX.Y _D)
Undefined	1	0	0	0	1001	(XY _B) ²	(XY _C) ²	(XY _D) ²		(K27.7–DX.Y _B –DX.Y _C –DX.Y _D)
Undefined	1	0	0	0	1010	(XY _B) ²	(XY _C) ²	(XY _D) ²		(K29.7–DX.Y _B –DX.Y _C –DX.Y _D)
Undefined	1	0	0	0	1011	(XY _B) ²	(XY _C) ²	(XY _D) ²		(K30.7–DX.Y _B –DX.Y _C –DX.Y _D)

- Notes:
1. Don't care (any value).
 2. Outputs for the data characters in the ordered set must be encoded to the correct data values.
 3. SOF – Start-of-frame delimiter.
 4. EOF – End-of-frame delimiter

5. Encoded as EOF_{N1} if TERR or PERR = 1.
6. Encoded as EOF_{D11} if TERR or PERR = 1.
7. Proper running disparity is forced before encoding these ordered sets.

Table B-2. TQ9303 Decoding

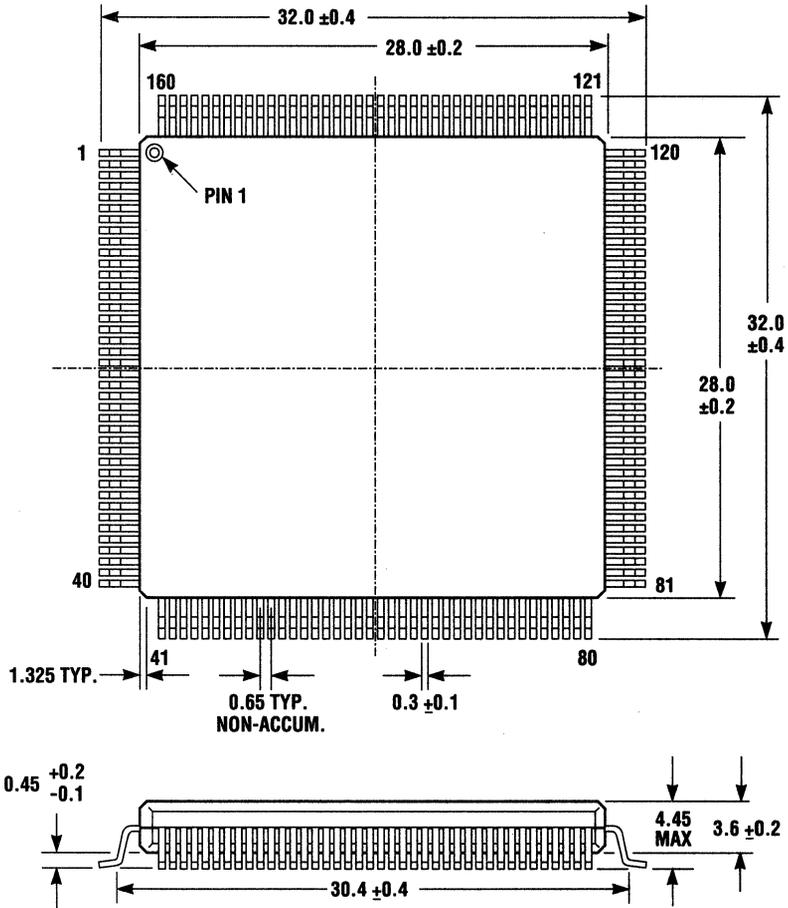
Ordered Set Input	Cntl	Sig	32-Bit Decoded Output					
			31:24		23:16		15:8	7:0
			SOF	EOF	Type	BR _D ⁻⁽²⁾		BR _D ⁺⁽³⁾
SOFn1	0	0	1	0	0001	(B5 ₁₆)	(37 ₁₆)	(37 ₁₆)
SOFn2	0	0	1	0	0010	(B5 ₁₆)	(35 ₁₆)	(35 ₁₆)
SOFn3	0	0	1	0	0011	(B5 ₁₆)	(36 ₁₆)	(36 ₁₆)
SOFi1	0	0	1	0	0101	(B5 ₁₆)	(57 ₁₆)	(57 ₁₆)
SOFi2	0	0	1	0	0110	(B5 ₁₆)	(55 ₁₆)	(55 ₁₆)
SOFi3	0	0	1	0	0111	(B5 ₁₆)	(56 ₁₆)	(56 ₁₆)
SOFc1	0	0	1	0	1101	(B5 ₁₆)	(17 ₁₆)	(17 ₁₆)
SOFf	0	0	1	0	1000	(B5 ₁₆)	(58 ₁₆)	(58 ₁₆)
EOFn	0	0	0	1	0000	(95 ₁₆)	(B5 ₁₆)	(58 ₁₆)
EOFt	0	0	0	1	0100	(95 ₁₆)	(B5 ₁₆)	(75 ₁₆)
EOFdt	0	0	0	1	1100	(95 ₁₆)	(B5 ₁₆)	(95 ₁₆)
EOFa	0	0	0	1	1001	(95 ₁₆)	(B5 ₁₆)	(F5 ₁₆)
EOFni	0	0	0	1	0001	(8A ₁₆)	(AA ₁₆)	(D5 ₁₆)
EOFdti	0	0	0	1	1101	(8A ₁₆)	(AA ₁₆)	(95 ₁₆)
Idle	0	1	0	0	0000	(95 ₁₆)	(B5 ₁₆)	(B5 ₁₆)
R_Rdy	0	1	0	0	0110	(95 ₁₆)	(4A ₁₆)	(4A ₁₆)
NOS	0	1	0	0	1000	(55 ₁₆)	(BF ₁₆)	(45 ₁₆)
OLS	0	1	0	0	1001	(35 ₁₆)	(8A ₁₆)	(55 ₁₆)
LR	0	1	0	0	1010	(49 ₁₆)	(BF ₁₆)	(49 ₁₆)
LRR	0	1	0	0	1011	(95 ₁₆)	(BF ₁₆)	(49 ₁₆)
(K28.0-DX.Y _B -DX.Y _C -DX.Y _D)	1	0	0	0	0000	(XY _B)	(XY _C)	(XY _D)
(K28.1-DX.Y _B -DX.Y _C -DX.Y _D)	1	0	0	0	0001	(XY _B)	(XY _C)	(XY _D)
(K28.2-DX.Y _B -DX.Y _C -DX.Y _D)	1	0	0	0	0010	(XY _B)	(XY _C)	(XY _D)
(K28.3-DX.Y _B -DX.Y _C -DX.Y _D)	1	0	0	0	0011	(XY _B)	(XY _C)	(XY _D)
(K28.4-DX.Y _B -DX.Y _C -DX.Y _D)	1	0	0	0	0100	(XY _B)	(XY _C)	(XY _D)
(K28.5-DX.Y _B -DX.Y _C -DX.Y _D) ¹	1	0	0	0	0101	(XY _B)	(XY _C)	(XY _D)
(K28.6-DX.Y _B -DX.Y _C -DX.Y _D)	1	0	0	0	0110	(XY _B)	(XY _C)	(XY _D)
(K28.7-DX.Y _B -DX.Y _C -DX.Y _D)	1	0	0	0	0111	(XY _B)	(XY _C)	(XY _D)
(K23.7-DX.Y _B -DX.Y _C -DX.Y _D)	1	0	0	0	1000	(XY _B)	(XY _C)	(XY _D)
(K27.7-DX.Y _B -DX.Y _C -DX.Y _D)	1	0	0	0	1001	(XY _B)	(XY _C)	(XY _D)
(K29.7-DX.Y _B -DX.Y _C -DX.Y _D)	1	0	0	0	1010	(XY _B)	(XY _C)	(XY _D)
(K30.7-DX.Y _B -DX.Y _C -DX.Y _D)	1	0	0	0	1011	(XY _B)	(XY _C)	(XY _D)

Notes: 1. Valid for any unrecognized control sequence starting with "K28.5." Not valid for acquiring Word Sync.
 2. BR_D - Beginning Running Disparity Negative.
 3. BR_D + Beginning Running Disparity Positive.

DATACOM
 PRODUCTS

Mechanical Specifications

Figure 11. TQ9303 PQFP Package Dimensions
 (All dimensions are in millimeters)



Ordering Information

TQ9303-QC *Fibre Channel Encoder/Decoder*

Supporting Products

TQ9501-MC *531/1063 Mbaud Transmitter*

TQ9502-MC *531/1063 Mbaud Receiver*

DATAQOM
PRODUCTS

Additional Information

For latest specifications, additional product information,
worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com **Tel:** (503) 615-9000
Email: sales@tqs.com **Fax:** (503) 615-8900

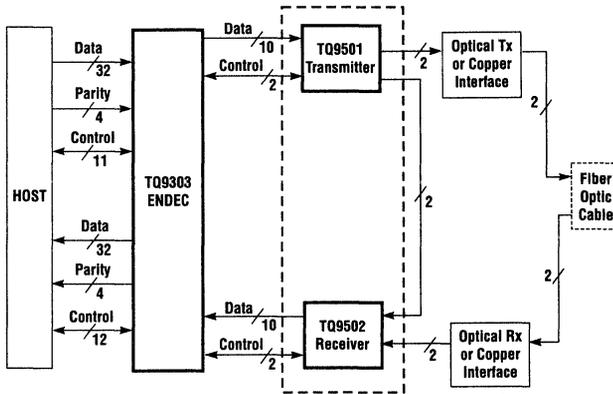
For technical questions and additional information on specific applications:

Email: applications@tqs.com

The information provided herein is believed to be reliable; TriQuint assumes no liability for inaccuracies or omissions. TriQuint assumes no responsibility for the use of this information, and all such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. TriQuint does not authorize or warrant any TriQuint product for use in life-support devices and/or systems.

Copyright © 1997 TriQuint Semiconductor, Inc. All rights reserved.

Revision 1.0.A October 1997



TriQuint's Fibre Channel transmitter (TQ9501) and receiver (TQ9502) are part of the FC531/FC1063 (Fibre Channel 531 and 1063 Megabaud) chip set. In addition to the transmitter and receiver, TriQuint offers the ENcoder/DECoder (TQ9303 ENDEC). The TQ9501, TQ9502, TQ9303 and a gigabit fiber optic module set provide a complete solution for Fibre Channel's FC0 and FC1 layers as well as partial support for the FC2 layer.

The TQ9501 and TQ9502 are designed in TriQuint's proprietary 0.7-micron GaAs process, enabling the transmitter and receiver to run at higher speeds and lower power than with conventional processes. The transmitter and receiver data interface has been selected to be 10 bits in order to conserve input/output power and to reduce pin count and package size. The transmitter performs the parallel-to-serial conversion and generates the internal high-speed clock for the serial output. The receiver performs serial-to-parallel conversion, recovers the clock and data from the serial input, and detects the K28.5 character (Fibre Channel standard "SYNC" transmission character).

The TQ9303 ENDEC implements 8b/10b encoding and decoding, ordered set encoding and decoding, parity checking and generation, 32-bit CRC checking and generation, and word synchronization as defined in the Fibre Channel Physical and Signaling Interface Standard (FC-PH).

Fibre Channel provides a high-speed physical layer for Intelligent Peripheral Interface (IPI) and Small Computer System Interface (SCSI) upper-layer command sets, High-Performance Parallel Interface (HIPPI) data link layer, and other user-defined command sets. Fibre Channel replaces the SCSI, IPI and HIPPI physical interfaces with a higher-speed interface capable of driving longer distances.

TQ9501/9502

531/1063 Mbaud Fibre Channel Transmitter and Receiver

Features

- Compliant with ANSI X3T11 Fibre Channel Standard
- Operates at 531.125 Mbaud and 1.0625 Gigabaud (1.25 Gigabaud max)
- Low power dissipation (2.25 W, typical)
- Low jitter
- No external PLL components
- 10-bit TTL-compatible data bus
- Synchronous Data Bus Interface
- Direct interface to TQ9303 ENDEC
- Single +5 V supply
- 48-pin MQuad package

TQ9501/TQ9502

Fibre Channel is optimized for predictable transfers of large blocks of data, such as those used in file transfers between processors (super computer, mainframe, super-mini, etc.), storage systems (disk and tape), and output-only devices such as laser printers and raster scan graphics terminals.

The Fibre Channel protocol is implemented in hardware, making it simple, efficient and robust. The lower-level physical interface is decoupled from the higher-level protocol allowing the Fibre Channel to be configured with various topologies, including point-to-point, multi-drop bus, ring, and cross point switch.

Fibre Channel supports distances up to 10 Km at baud rates of 132.8125 Mbaud to 1.0625 Gbaud. Copper media such as Coax and STP (Shielded Twisted Pair) are used for shorter distances while fiber optic cables are used for longer distances.

Applications for the TQ9501 and TQ9502 include serial SCSI, IPI, HIPPI, point-to-point serial communication, ATM and other networking applications.

TriQuint offers two chip sets for Fibre Channel: the TQ9501 and TQ9502 chip set for 531.125 Mbaud and 1.0625 Gbaud, and the GA9101 and GA9102 chip set for the 265.625 Mbaud rate.

Functional Description – TQ9501 Transmitter

The TQ9501 serializes a 10-bit TTL input into a differential PECL output. The TQ9501 is composed of an input register, a parallel-to-serial converter, a PLL clock generator, a differential output buffer and a PECL-to-TTL translator, as illustrated in Figure 1.

The self-contained PLL (Phase-Locked Loop) clock generator requires no external components. It generates an internal high-speed bit clock for the serial output, an internal byte clock for the parallel-to-serial converter and BYTECLK, based on REFCLK (REFERENCE CLock). BYTECLK is used by the TQ9303 ENDEC to generate TXCLK.

TXD0..9 are latched into the input register on the rising edge of TXCLK. The parallel-to-serial converter serializes the data into a differential PECL buffer. TXD9 is sent first and TXD0 is sent last.

Figure 1. TQ9501 Transmitter

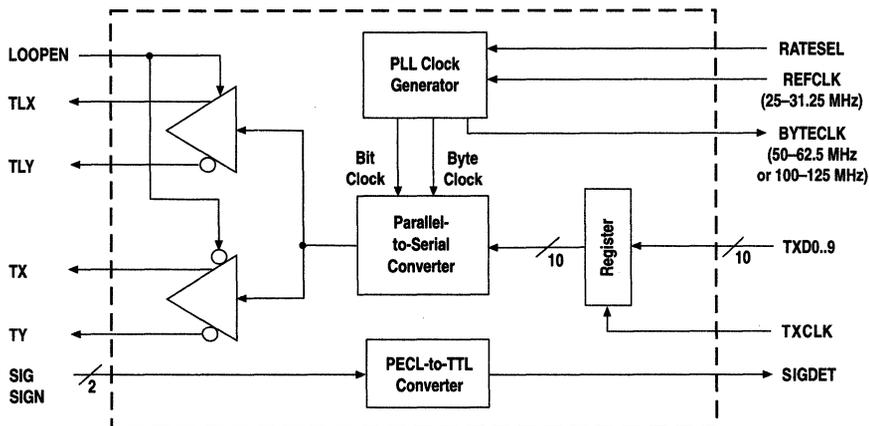
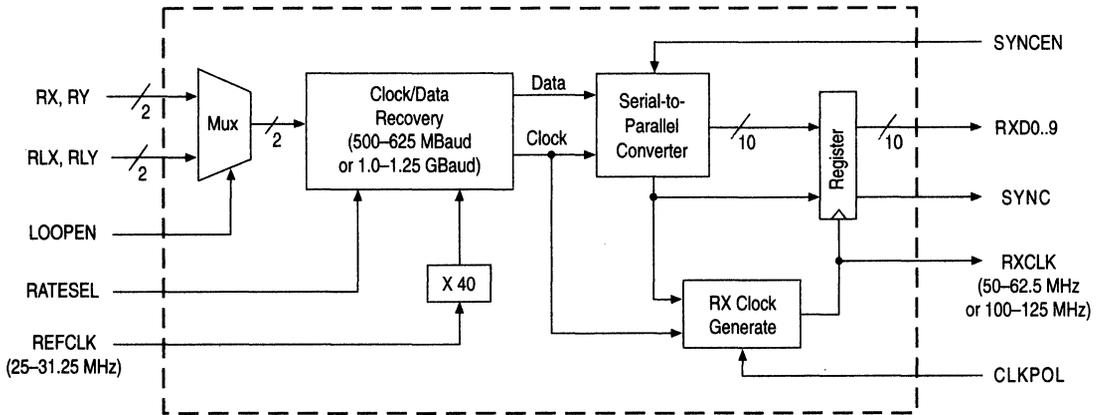


Figure 2. TQ9502 – Receiver



The LOOPEN (LOOP ENable) pin selects between the two differential output pairs, TLX and TLY, or TX and TY. LOOPEN = 1 selects the differential output TLX and TLY, setting TX = 0 and TY = 1. Conversely, LOOPEN = 0 selects TX and TY, setting TLX = 0 and TLY = 1. This relationship is shown in Table 1.

The PECL-to-TTL translator block is a differential PECL-to-TTL translator. It is normally used for translating PECL signals generated by optical receivers to TTL signals to drive control circuitry.

Table 1. LOOPEN Configuration

LOOPEN	Rx Input	Tx Output
0	RX, RY	TX, TY
1	RLX, RLY	TLX, TLY

Functional Description – TQ9502 Receiver

The TQ9502 consists of a clock and data recovery circuit, a multiplexer, and a serial-to-parallel converter block, as shown in Figure 3. The multiplexer selects between the RX and RY inputs or the RLX and RLY inputs. Outputs RTX, RTY, RLTX and RLTY, not shown on Figure 3, are provided for Fly-By™ termination, which allows termination resistors to be placed away from the chip. The multiplexer output is selected by the LOOPEN pin as shown in Table 1. The selected data goes to the CDR (Clock/Data Recovery) block.

The clock and data recovery block has two modes: clock recovery and frequency acquisition. In the clock input, it automatically switches to the frequency acquisition mode which causes the CDR to lock onto the REFCLK signal. This prevents the PLL from drifting away from the serial data rate and ensures that the CDR will properly lock onto the input serial data when it is reapplied.

The receiver synchronizes 1 ms after applying power, REFCLK and data. The receiver synchronizes 200 μ s after applying valid data if power and REFCLK has already been applied. The output of this block is latched into the output register. When SYNCEN is high (SYNCronization ENable), the serial-to-parallel converter monitors the serial data for the K28.5 character. When it sees a K28.5, it realigns the 10-bit register to the K28.5 character and drives SYNC high.

The clock generate block also detects SYNC going high, and delays the phase of the output RXCLK to coincide with the new alignment. Some bits may be lost during

the realignment. When SYNCEN is low, SYNC is driven low and the serial-to-parallel converter ignores the K28.5 character.

The output register takes in the 10-bit-wide output from the Serial-to-Parallel Converter and drives the RXD0..9 outputs. RXD0..9 are strobed on the rising edge of RXCLK. CLKPOL = 1 results in a longer setup time and shorter hold time than CLKPOL = 0. The first serial bit is placed in RXD9 and the tenth bit is placed in RXD0.

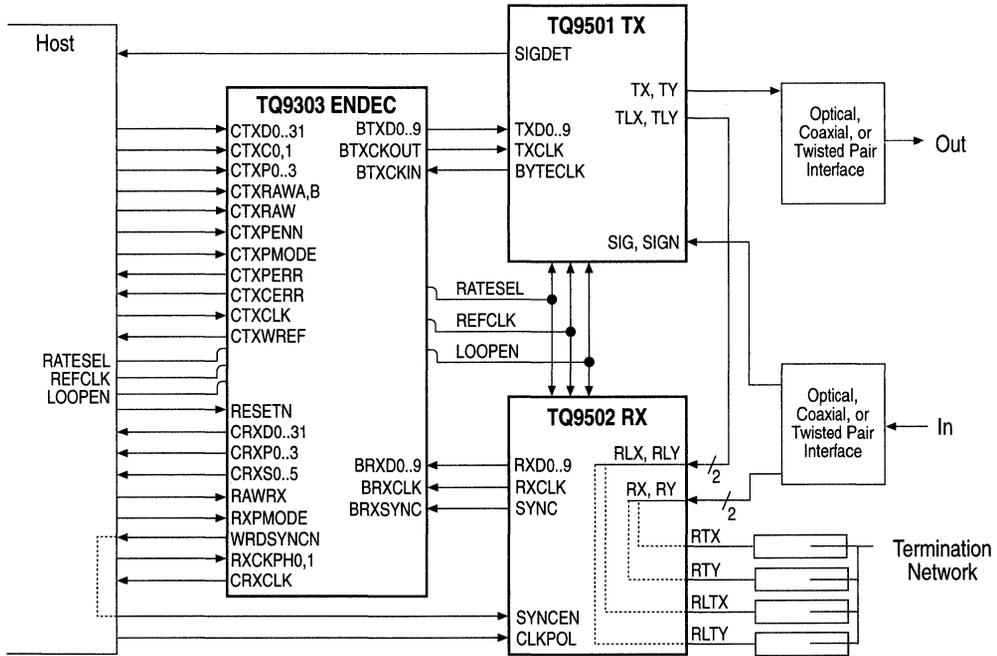
Fibre Channel Interface

Figure 3 illustrates a typical Fibre Channel physical layer block diagram using the TQ9501, TQ9502 and TQ9303 chip set. The interface between the host and ENDEC operates at 26.5625 MHz with a data width of 32-bits for the transmit path and a separate 32-bits for the receive path. The ENDEC performs the 8b/10b encoding and decoding; ordered set encoding and decoding; parity checking and generation; 32-bit CRC checking and generation; and word synchronization.

The interface between the TQ9303 and the TQ9501/TQ9502 operates at 531.25 or 106.250 MHz with an encoded data width of 10-bits. The serial interface operates from 531.125 Mbaud or 1.0625 Gbaud respectively, which is connected to an optical, coaxial or twisted pair interface.

For additional information on the ENDEC, please refer to the TQ9303 data sheet.

Figure 3. System Block Diagram – Fibre Channel



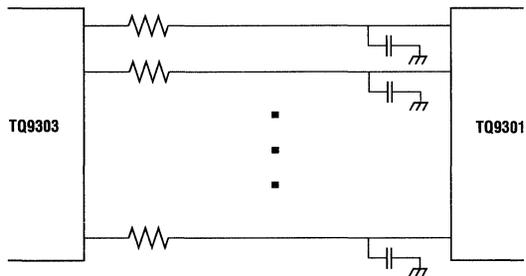
DATACOM
 PRODUCTS

Note that the fast edge rates of the TQ9303 TX bus outputs can affect the stability of the TQ9501 PLL. These edge rates can be effectively “slowed” by adding some series resistance of from 90 to 250 ohms to the TX data bus lines (TXD0..9) as shown in Figure 4. Resistance should also be added to TXCLK to maintain the correct timing relationship with the data lines. The resistors should be placed near the TQ9303.

In cases where the line capacitance of the bus traces is less than 3 pF, it may also be necessary to add from 1– 2 pf of capacitance to each trace near the TQ9501.

The purpose is to slow the edge rates enough to prevent potential undershoot from disturbing the power supplies in the PLL circuitry of the TQ9501.

Figure 4. Adding resistance and capacitance to the TX data bus.



TQ9501/TQ9502

Table 2. Transmitter Pin Descriptions

Symbol	Type	Description
TX, TY	0	Differential Transmitter Outputs connect to an optical transmitter, a coaxial interface or shielded twisted pair interface. LOOPEN low selects TY and TX outputs. LOOPEN high drives TX low and TY high.
TLX, TLY	0	Loopback Differential Transmitter Outputs connect to the Receiver RLX and RLY inputs. LOOPEN high selects TLY and TLX outputs. LOOPEN low drives TLX low and TLY high.
LOOPEN	I	Loopback Enable high selects the TLX and TLY as outputs. LOOPEN low selects the TX and TY as outputs.
REFCLK	I	The PLL multiplies the Reference Clock and generates the high speed clock for transmitting serial data. REFCLK shall be equal to 1/40 of the baud rate. REFCLK shall have a frequency tolerance of 100 ppm to guarantee clock and data recovery on the receiver. The REFCLK operating range is 25 MHz to 31.25 MHz.
BYTECLK	0	The ENDEC uses Byte Clock to synchronize to the Transmitter. The ENDEC generates TXCLK from BYTECLK simplifying the synchronization between the Transmitter and ENDEC.
TXD0..9	I	The Transmitter latches the 10 Encoded Data Bits at the rising edge of TXCLK. The Transmitter serially sends TXD9 first and TXD0 last.
TXCLK	I	The Transmitter Data Clock strobes TXD0..9 into the Transmitter. The ENDEC generates TXCLK from BYTECLK simplifying the synchronization between the Transmitter and ENDEC.
SIG, SIGN	I	The Differential Signal Present are inputs to a PECL to TTL translator. The translator is typically used to convert differential signals from a differential optical receiver output to TTL. The TTL equivalent of SIG and SIGN is SIGDET.
SIGDET	0	Signal Detect is the output of the PECL to TTL translator. The translator is typically used to convert differential signals from a differential optical receiver output to TTL. SIGDET is useful when implementing an OFC - Open Fibre Control protocol where the link activity or optical receiver outputs are monitored continuously.
RATESEL	I	Rate Select is used to select between 531 Mbaud (RATESEL=VDD) and 1063 Mbaud (RATESEL=GND) operation.

Figure 5. Fly-By™ Termination Schematic

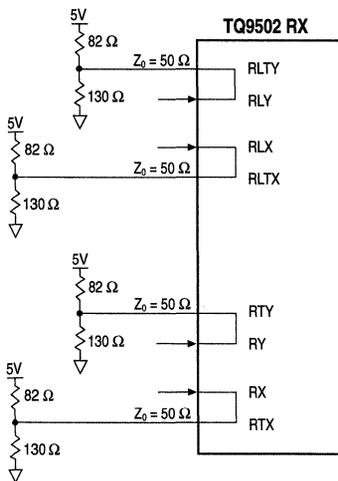


Figure 6. Transmitter Synchronization Circuit Block Diagram

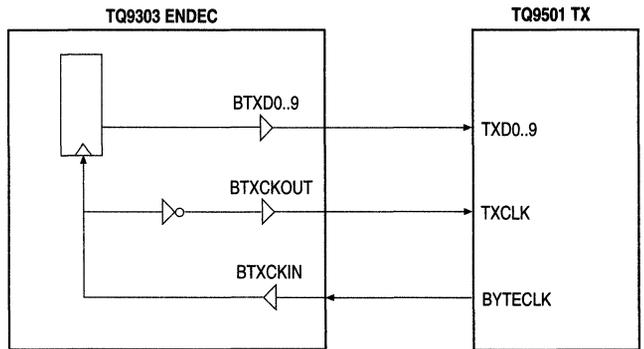


Table 3. Receiver Pin Descriptions

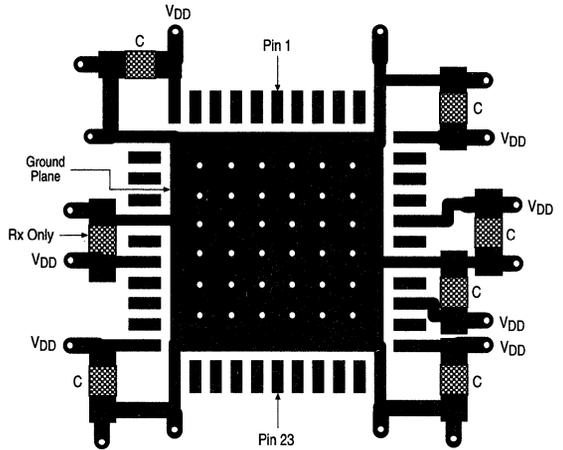
Symbol	Type	Description
RX, RY	I	The Receiver Differential Inputs connects to an optical, coaxial or shielded twisted pair interface. LOOPEN low selects the RX and RY inputs. LOOPEN high selects the RLX and RLY inputs.
RTX, RTY	I	The Receiver Differential Termination are used in Fly-By™ termination. RX is internally connected to RTX and RY is internally connected to RTY. A termination circuit connects to RTX and RTY instead of RX and RY. With Fly-By™ termination, the termination circuit can be located away from the Receiver instead of requiring termination directly at RX and RY. Both RTX and RTY must be terminated with a 50 chip resistor in series with 3V reference or Thevenin equivalent as shown in Figure 6.
RLX, RLY	I	The Looped Receiver Differential Inputs connect to the Transmitters TLX and TLY outputs providing a loop back path. LOOPEN high selects the RLX and RLY inputs. LOOPEN low selects the RX and RY inputs.
RLTX, RLTY	I	The Receiver Differential Termination are used in Fly-By™ termination. RLX is internally connected to RLTX and RLY is internally connected to RLTY. A termination circuit connects to RLTX and RLTY instead of RLX and RLY. With Fly-By™ termination, the termination circuit can be located away from the Receiver instead of requiring termination directly at the RLX and RLY. Both RLTX and RLTY must be terminated with a 50 chip resistor in series with 3V reference or Thevenin equivalent as shown on Figure 6.
LOOPEN	I	Loopback Enable high selects the RLX and RLY inputs. LOOPEN low selects the RX and RY inputs.
REFCLK	I	The Reference Clock provides the clock needed by the clock recovery circuit. The REFCLK frequency shall be chosen to equal 1/40 of the baud rate. REFCLK shall have a frequency tolerance of 100 ppm to guarantee clock and data recovery on the receiver. The receiver automatically locks onto the REFCLK during power-up and/or when no input signals are applied. This prevents the PLL from drifting away from the input data rate. The PLL automatically locks onto the input data stream when it is applied. The frequency range of REFCLK is 25 MHz to 31.25 MHz.
SYNCEN	I	When Sync Enable is high, the receiver searches for a K28.5 character from the input data stream and byte aligns the parallel register to this character as defined in the Fibre Channel standard. SYNCEN low disables byte alignment to a K28.5 character and drives SYNC low. The K28.5 character has a pattern of RXD9..0 = 001111 1010 or 110000 0101. Whenever the receiver detects the K28.5 pattern it byte aligns to this character and drives SYNC high for that byte cycle. SYNC is high only in byte cycle where a K28.5 character is present.
RXD0..9	0	These are 10 Encoded Data Bits where the first bit received from the serial data stream is RXD9 and the last bit received is RXD0. The receiver generates RXCLK to strobe RXD0..9.
SYNC	0	If SYNCEN is high, Synchronization to K28.5 goes high for the byte clock cycle in which a K28.5 character is present on the RXD0..9 output. If SYNCEN is low then SYNC is always low.
RXCLK	0	Receiver Data Clock is the strobe for RXD0..9 and SYNC. The phase of RXCLK with respect to RXD0..9 and SYNC changes depending on CLKPOL. CLKPOL high provides a longer setup time and a shorter hold time while CLKPOL low provides a shorter setup time and a longer hold time. The frequency range of RXCLK is 50 MHz to 62.5 MHz in FC531 mode and 100 MHz to 125 MHz in FC1063 mode.
CLKPOL	0	Clock Phase or Polarity controls the phase of RXCLK with respect to RXD0..9 and SYNC. CLKPOL high provides a longer setup time and a shorter hold time while CLKPOL low provides a shorter setup time and a longer hold time.
RATESEL	I	Rate Select is used to select between 531 Mbaud (RATESEL=VDD) and 1063 Mbaud (RATESEL=GND) operation.

Layout Guidelines

Multiple ground and power pins on the TQ9501/02 reduce ground bounce. Good layout techniques, however, are necessary to guarantee proper operation and to meet the specifications across the full operating range. TriQuint recommends bypassing each of the V_{DD} supply pins to the nearest ground pin, as close to the chip as possible.

Figure 7 shows the recommended power layout for the TQ9501/02. The bypass capacitors should be located on the same side of the board as the TQ9501/02. The V_{DD} traces connect to an inner-layer V_{DD} plane. All of the ground pins (GND) are connected to a small ground plane on the surface beneath the chip. Multiple through-holes connect this small surface plane to an inner-layer ground plane. The capacitors are 0.1 μF. TriQuint's test board uses X7R temperature-stable capacitors in 1206 SMD cases.

Figure 7. Example Top Layer Layout of Power Pins (Not to scale)



Note: Series resistors and small capacitors may be needed for the TX data bus and clock lines. See the previous "Fibre Channel Interface" section in this datasheet for details.

Table 4. Absolute Maximum Ratings

Parameter	Range
Storage temperature	-65 °C to +150 °C
Case temperature	-55 °C to +125 °C
Supply voltage to ground	-0.5 V to +7.0 V
DC input voltage	-0.5 V to (V _{DD} + 0.5 V)
DC input current	30 mA to +5 mA
Package Thermal Resistance	θ _{jA} = 40 °C/W; θ _{cA} = 8 °C/W
Die Junction Temperature	T _j = 150 °C

Note: Stresses above those listed in Absolute Maximum Rating may cause permanent damage to the device. This is a stress-only rating and operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied.

Table 5. Operating Conditions

Parameter	Range
Supply voltage	5 V ± 5
Ambient temperature	0 to 70 °C

Note: Proper functionality is guaranteed under these operating conditions.

Table 6. Test Loads

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Unit
C _{IN}	Input capacitance	V _{IN} = 2.0 V at f = 1 MHz		6		pF
C _{OUT}	Output capacitance	V _{OUT} = 2.0 V at f = 1 MHz		9		pF

Table 7. DC Characteristics—TQ9501 Transmitter TTL Signals (TXDD..9, TXCLK, BYTECLK, LOOPEN, SIGDET, REFCLK, RATESEL)
(Over operating range unless otherwise specified)

Symbol	Description	Test Conditions	Min.	Limits ¹		Unit	
				Typ.	Max.		
V _{OH}	Output HIGH voltage	V _{DD} = Min V _{IN} ² = V _{IH} or V _{IL}	I _{OH} = -1.6 mA I _{OH} = -3.2 mA ³	2.4	3.2	V	
V _{OL}	Output LOW voltage	V _{DD} = Min V _{IN} ² = V _{IH} or V _{IL}	I _{OL} = 4 mA I _{OL} = 8 mA ³		0.2	0.5	V
I _{SC} ⁴	Output short-circuit current	V _{DD} = Max	V _{OUT} = 0.5 V	-15		-120	mA
I _{IL}	Input LOW current	V _{DD} = Max	V _{IN} = 0.4 V			-400	μA
I _{IH}	Input HIGH current	V _{DD} = Max	V _{IN} = 2.7 V			25	μA
I _I	Input HIGH current	V _{DD} = Max	V _{IN} = 5.5 V			1	mA
V _{IH} ⁵	Input HIGH level	Guaranteed input logical HIGH voltage for all inputs, V _{DD} = Max		2.0			V
V _{IL} ⁵	Input LOW level	Guaranteed input logical LOW voltage for all inputs				0.8	V
V _I	Input clamp voltage	V _{DD} = Min	I _{IN} = -18 mA			-1.2	V
I _{DD}	Power supply current	V _{DD} = Max, static			175	220	mA

Table 8. DC Characteristics—TQ9501 Transmitter PECL Signals (TX, TY, TLX, TLY, SIG, SIGN)

Symbol	Description	Test Conditions	Min.	Limits ¹		Unit
				Typ.	Max.	
V _{OH}	Output HIGH voltage	V _{DD} = Min PECL load	V _{DD} - 1.200		V _{DD} - 0.50	V
V _{OL}	Output LOW voltage	V _{DD} = Min PECL load	V _{DD} - 2.00		V _{DD} - 1.60	V
V _{CMO}	Output common mode voltage		V _{DD} - 1.60		V _{DD} - 1.10	V
DV _{OUT}	Output differential voltage		0.60		1.2	V
I _{IL}	Input LOW current	V _{DD} = Max V _{IN} = 2.4 V			200	μA
I _{IH}	Input HIGH current	V _{DD} = Max V _{IN} = V _{DD} - 0.5 V			250	μA
V _{IHS}	Highest input HIGH voltage	V _{DD} = Min			V _{DD} - 0.5	V
V _{ILS}	Lowest input LOW voltage	V _{DD} = Max	2.4			V
V _{DIF}	Differential input voltage	V _{DD} = Min	0.4		1.2	V
V _{ICM}	Input common mode voltage	V _{DD} = Min	2.8		V _{DD} - 0.7	V

Notes: 1. Typical limits are: V_{DD} = 5.0 V and T_A = 25 °C.

2. The TTL inputs could be HIGH or LOW.

3. The I_{OL} and I_{OH} specifications are valid only for the BYTECLK.

4. These are absolute values with respect to device ground.

5. No more than one output should be tested at a time. Duration of the short circuit should not exceed one second.

TQ9501/TQ9502

Table 9. DC Characteristics—TQ9502 Receiver TTL Signals
(RXDD..9, RXCLK, SYNCEN, REFCLK, LOOPEN, SYNC, CLKPOL, RATESEL)
(Over operating range unless otherwise specified)

Symbol	Description	Test Conditions	Min.	Limits ¹		Unit
				Typ.	Max.	
V _{OH}	Output HIGH voltage	V _{DD} = Min V _{IN} ² = V _{IH} or V _{IL}	2.4	3.2		V
V _{OL}	Output LOW voltage	V _{DD} = Min I _{OL} = 4 mA = 8 mA ³	0.2	0.5	V	
I _{SC} ⁵	Output short-circuit current	V _{DD} = Max V _{OUT} = 0.5 V	-15		-120	mA
I _{IL}	Input LOW current	V _{DD} = Max V _{IN} = 0.40 V			-400	μA
I _{IH}	Input HIGH current	V _{DD} = Max V _{IN} = 2.7 V			25	μA
I _I	Input HIGH current	V _{DD} = Max V _{IN} = 5.5 V			1	mA
V _{IH} ⁴	Input HIGH level voltage for all inputs	Guaranteed input logical HIGH	2.0			V
V _{IL} ⁴	Input LOW level voltage for all inputs	Guaranteed input logical LOW			0.8	V
V _I	Input clamp voltage	V _{DD} = Min I _{IN} = -18 mA			-1.2	V
I _{DD}	Power supply current	V _{DD} = Max, static		280	350	mA

Table 10. DC Characteristics—TQ9502 Receiver PECL Signals (RX, RY, RTX, RTY, RLX, RLY, RLTX, RLTY)

Symbol	Description	Test Conditions	Min.	Limits ¹		Unit
				Typ.	Max.	
I _{IL}	Input LOW current	V _{DD} = Max V _{IN} = 2.4 V	0.5		200	μA
I _{IH}	Input HIGH current	V _{DD} = Max V _{IN} = V _{DD} - 0.5 V			250	μA
V _{IHS}	Highest input HIGH voltage	V _{DD} = Max			V _{DD} - 0.50	V
V _{ILS}	Lowest input LOW voltage	V _{DD} = Min	2.4			V
V _{DIF}	Differential input voltage	V _{DD} = Min	0.4		1.2	V
V _{ICM}	Input common mode voltage	V _{DD} = Min	2.8		V _{DD} - 0.7	V

- Notes:
1. Typical limits are: V_{DD} = 5.0 V and T_A = 25 °C.
 2. The TTL inputs could be HIGH or LOW.
 3. The I_{OL} and I_{OH} specifications are valid only for the RXCLK.
 4. These are absolute values with respect to device ground.
 5. No more than one output should be tested at a time. Duration of the short circuit should not exceed one second.

Table 12. AC Specifications—TQ9501 Transmitter

Parameters with dual values refer to 531Mbaud/1063Mbaud operation respectively.

Parameter	Description	Min.	Typ.	Max.	Units
T ₁	REFCLK pulse width HIGH	10.0			ns
T ₂	REFCLK pulse width LOW	10.0			ns
T ₃ ¹	REFCLK period (T)	32.0		40.0	ns
T ₄	TXD 9..0 setup time	2.0			ns
T ₅	TXD 9..0 hold time	2.0			ns
T ₆	BYTECLK, TXCLK pulse width HIGH	6.0/3.0			ns
T ₇	BYTECLK, TXCLK pulse width LOW	6.0/3.0			ns
T ₈	BYTECLK, TXCLK period (T)	16.0/8.0		20.0/10.0	ns
T ₉	TX, TY, TLX, TLY rise time	100		400/300	ps
T ₁₀	TX, TY, TLX, TLY fall time	100		400/300	ps
T ₁₁	TX ~ TY or TLX ~ TLY skew			100/60	ps
T ₁₂ ³	TX, TY or TLX, TLY output jitter – deterministic jitter (DJ) – random jitter (RJ)			100/75 200/150	ps

Notes: 1. REFCLK Tolerance = (20/baud rate) ± 0.01%, for baud rate of 500Mbaud to 625Mbaud and (40/baud rate) ± 0.01%, for baud rate of 1 Gbaud to 1.25 Gbaud.

2. baud time = 1/baud rate

3. The jitter numbers are for a BER of 10⁻¹².

DATACOM PRODUCTS

Figure 8. Bus Timing – TQ9501 Transmitter

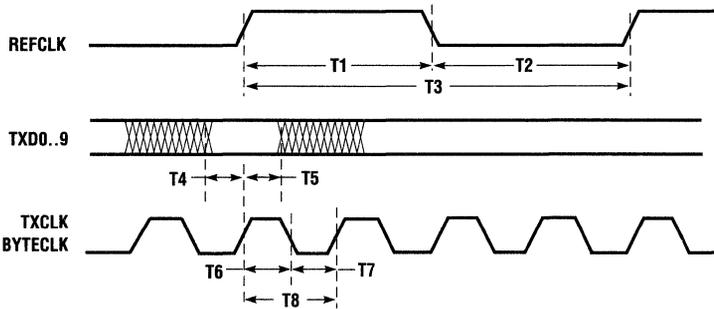
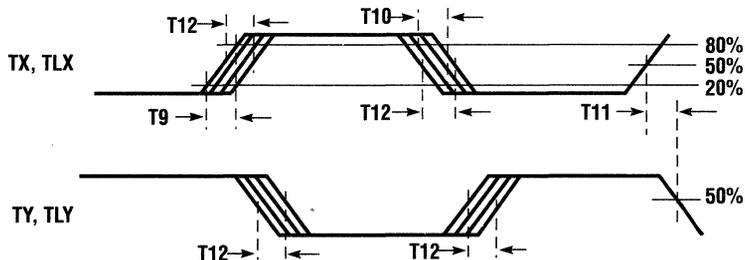


Figure 9. Serial Output Timing – TQ9501



TQ9501/TQ9502

Table 12. AC Specifications—TQ9502 Receiver

Parameters with dual values refer to 531Mbaud/1063Mbaud operation respectively.

Parameter	Description	Min.	Typ.	Max.	Units
T ₂₁	REFCLK pulse width LOW	10.0			ns
T ₂₂	REFCLK pulse width HIGH	10.0			ns
T ₂₃ ¹	REFCLK period	32.0	40.0	ns	
T ₂₄	Setup Time RXD 0..9 & SYNC	CLKPOL=0	4.0/2.0		ns
		CLKPOL=1	12.0/6.0		ns
T ₂₅	Hold Time RXD 0..9 & SYNC	CLKPOL=0	8.0/4.0		ns
		CLKPOL=1	0		ns
T ₂₆ ¹	RXCLK period	16.0/8.0		20.0/10.0	ns
T ₂₇ ¹	RXCLK pulse width HIGH	6.0/4.0			ns
T ₂₈ ¹	RXCLK pulse width LOW	6.0/4.0			ns
T ₂₉	RX, RY, RLX, RLY rise time			0.4 baud time	ns
T ₃₀	RX, RY, RLX, RLY fall time			0.4 baud time	ns
T ₃₁	RX ~ RY, RLX ~ RLY skew			0.3 baud time	ns
T ₃₂	RX, RY, RLX, RLY peak-to-peak input jitter			0.7 baud time	ns

- Notes: 1. REFCLK Tolerance = (20/baud rate) ± 0.01%, for baud rate of 500Mbaud to 625Mbaud and (40/baud rate) ± 0.01%, for baud rate of 1 Gbaud to 1.25 Gbaud.
 2. baud time = 1/baud Rate
 3. The jitter numbers are for a BER of 10⁻¹².

Table 13. Synchronization Times

Description	Min.	Typ.	Max.	Units
Power Up or application of REFCLK to receiver synchronization			1	ms
Application of valid data to receiver synchronization			200	µs
Receiver resynchronization after phase shift on data			2500	bit time

Figure 10. Bus Timing – TQ9502 Receiver

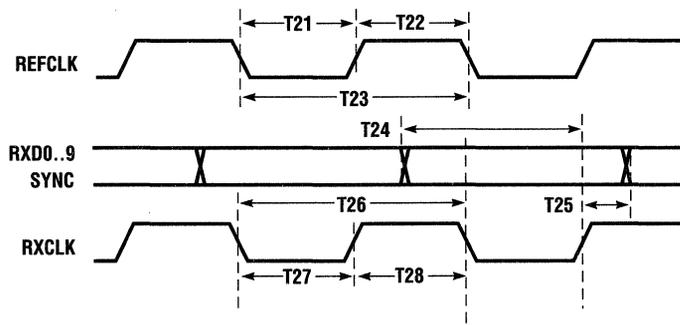


Figure 11. Serial Input Timing – TQ9502

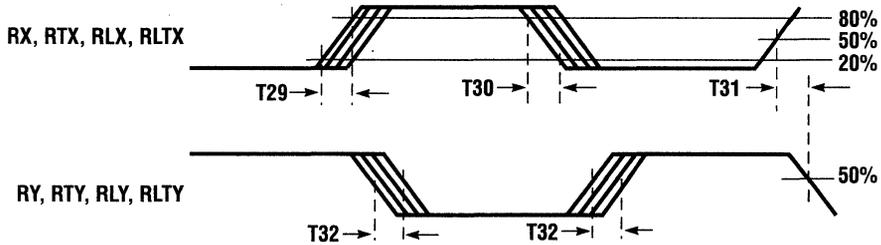


Figure 12a. TTL Test Load, RXCLK

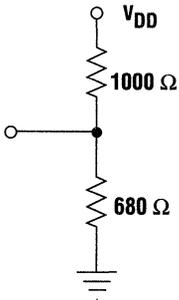


Figure 12b. TTL Test Load, All Other TLL Outputs

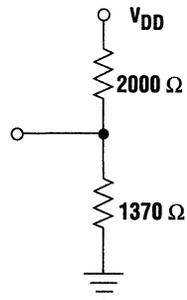
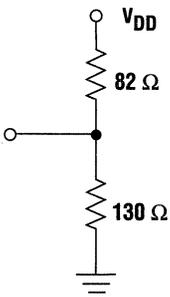


Figure 12c. PECL Test Load



TQ9501/TQ9502

Figure 13. Pinout for Transmitter

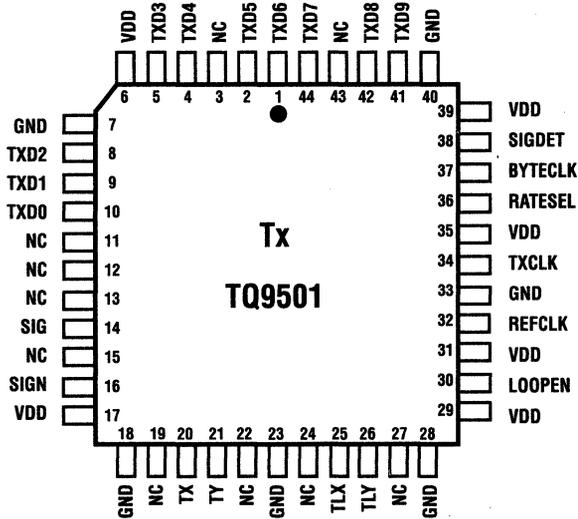
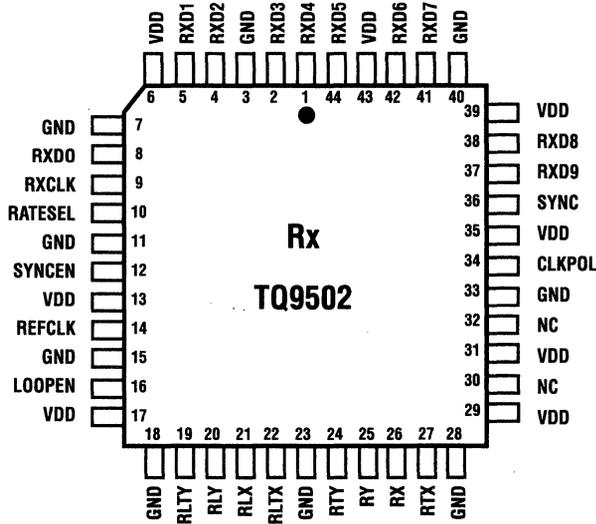


Table 14. Pin Definitions – TQ9501 Transmitter

Symbol	Pin #	I/O	# Pins	Logic Type	Active	Description
TX, TY	20, 21	Output	2	PECL	NRZ	Differential serial data output
TLX, TLY	25, 26	Output	2	PECL	NRZ	Loopback differential serial data output
SIG, SIGN	14, 16	Input	2	PECL	HIGH	Differential optical signal present
TXCLK	34	Input	1	TTL	HIGH	Transmit clock
TXD 0..9	10, 9, 8, 5, 4, 2, 1, 44, 42, 41	Input	10	TTL	HIGH	Transmit data input
LOOPEN	30	Input	1	TTL	HIGH	Enable loopback
SIGDET	38	Output	1	TTL	HIGH	Signal detect
REFCLK	32	Input	1	TTL	HIGH	Oscillator clock (25 to 31.25 MHz)
BYTECLK	37	Output	1	TTL	HIGH	Byte clock
VDD	6, 17, 29, 31, 35, 39	—	6	—	—	+5 Volt Supply
GND	7, 18, 23, 28, 33, 40	—	6	—	—	Ground
NC	3, 11, 12, 13, 15, 19, 22, 24, 27, 43	—	10	—	—	No Connect
RATESEL	36	Input	1	—	—	VDD (1) for 531Mbaud operation Ground (0) for 1063Mbaud operation

Figure 14. Pinout for Receiver



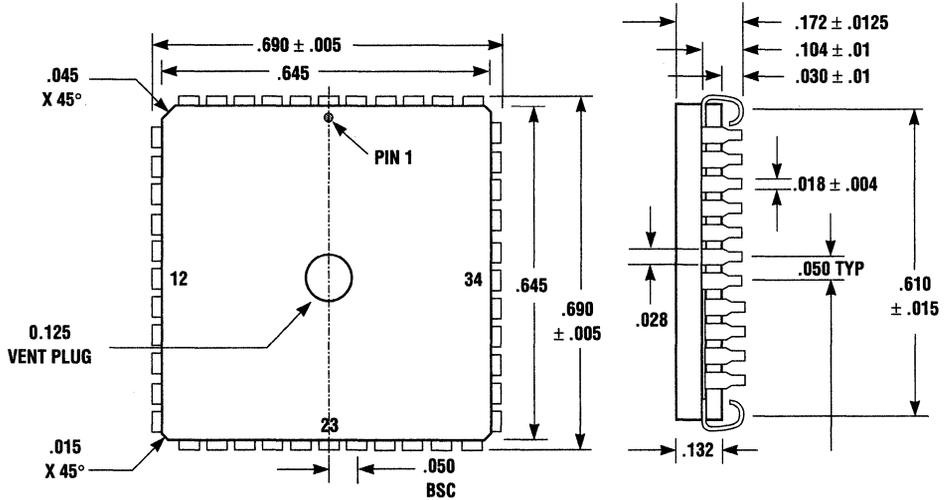
DATACOM
 PRODUCTS

Table 15. Pin Definitions - TQ9502 Receiver

Symbol	Pin #	I/O	# Pins	Logic Type	Active	Description
RX, RY	26, 25	I	2	PECL	NRZ	Differential serial data input
RLX, RLY	21, 20	I	2	PECL	NRZ	Differential serial data input, loopback
RTX, RTY	27, 24	I	2	PECL	NRZ	For fly-by termination
RLTX, RLTY	22, 19	I	2	PECL	NRZ	For fly-by termination
RXD 0..9	8, 5, 4, 2, 1, 44, 42, 41, 38, 37	O	10	TTL	HIGH	Receive output data
RXCLK	9	O	1	TTL	HIGH	Receive clock
REFCLK	14	I	1	TTL	HIGH	Oscillator clock (25 MHz to 31.25 MHz)
SYNC	36	O	1	TTL	HIGH	Receive byte sync
SYNCEN	12	I	1	TTL	HIGH	Sync Enable or Align to K28.5
LOOPEN	16	I	1	TTL	HIGH	Enable loopback
CLKPOL	34	I	1	TTL	LOW	RXCLK Clock Phase
VDD	6, 13, 17, 29, 31, 35, 39, 43	—	8	—	—	+5 V supply
GND	3, 7, 11, 15, 18, 23, 28, 33, 40	—	9	—	—	Ground
NC	30, 32	—	2	—	—	No connect
RATESEL	10	I	1	—	—	VDD(1) for 531Mbaud operation Ground(0) for 1063 Mbaud operation

TQ9501/TQ9502

Figure 15. 44-Pin MQuad J-leaded Package



Ordering Information

TQ9501-MC FC531/1063 Transmitter

TQ9502-MC FC531/1063 Receiver

Additional Information

For latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com **Tel:** (503) 615-9000

Email: sales@tqs.com **Fax:** (503) 615-8900

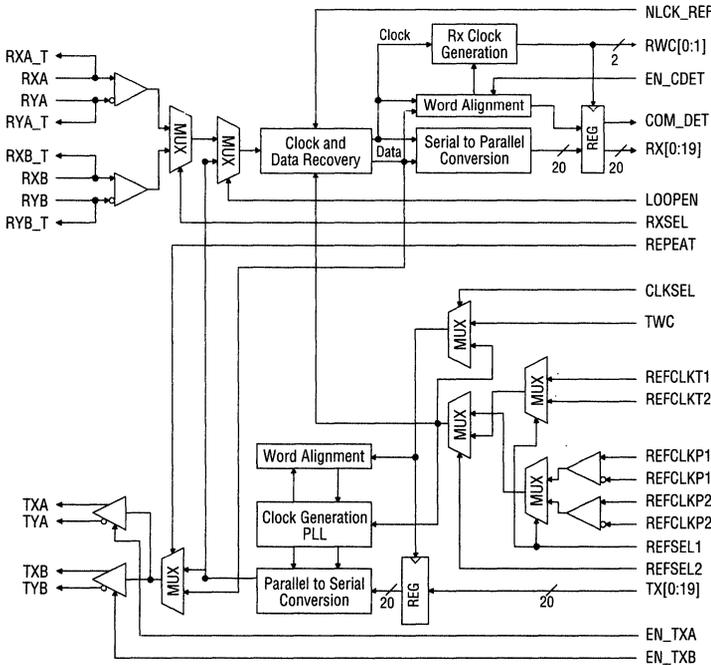
For technical questions and additional information on specific applications:

Email: applications@tqs.com

The information provided herein is believed to be reliable; TriQuint assumes no liability for inaccuracies or omissions. TriQuint assumes no responsibility for the use of this information, and all such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. TriQuint does not authorize or warrant any TriQuint product for use in life-support devices and/or systems.

Copyright © 1997 TriQuint Semiconductor, Inc. All rights reserved.

Revision 1.0.A October 1997



The TQ9525 is part of TriQuint's family of Datacom Transmission Products. The TQ9525 is a 2.5Gb/s transceiver which takes 20-bit, 8B/10B encoded data, serializes it and sends it out on a differential PECL data link. In addition it receives differential serial data, recovers the clock and deserializes the data, and presents it at the 20-bit receive data bus.

The TQ9525 receiver section performs frame alignment to the special Fibre Channel K28.5 "comma +" character. Maximum re-lock time due to a phase discontinuity is 100 bit periods. Receiver lock time following a Lock-to-Reference signal is 1 ms.

The TQ9525 offers selectable redundant high-speed PECL inputs and redundant high-speed PECL outputs with individual controls. Additionally, the TQ9525 offers the system designer multiple PECL and TTL reference clock inputs.

TQ9525

ADVANCE INFORMATION DATA SHEET

2.5 Gigabit/sec 20-bit Transceiver

Features

- 2.5 Gb/s data rate
- Operates with single 5V supply
- 20-bit TTL transmit and receive busses
- Dual differential PECL serial output buffers with individual enable control
- Dual differential PECL serial input buffers with fly-by terminations
- Internal loopback capability
- Repeater mode to transmit retimed receive data
- TTL receive-PLL-lock to reference-clock function with 1 ms maximum lock time
- Maximum receive-phase discontinuity re-lock time of 100 bit periods
- Receive word alignment to first seven bits of 8B/10B comma + character, with optional bypass
- Reference clock inputs selectable as dual TTL or dual differential PECL
- Optional use of separate 125 MHz TTL transmit-word clock input
- 125 MHz differential TTL receive-word clock outputs

DATA
COM
PRODUCTS

Circuit Descriptions

PECL Serial Data Inputs

High-speed serial inputs require PECL levels and external input termination resistors which can be located away from the device through the use of the fly-by termination signal pins. There are two differential serial receive ports, selected through the use of the TTL input RXSEL. The optional PECL REFCLK inputs do not have fly-by termination pins.

PECL Serial Data Outputs

High-speed serial outputs are PECL compatible with 50-ohm pull-down resistors required to +3V. All outputs are differential and require both true and complement to be terminated. If an output channel is not used, then the true and the compliment signals of that output may be left unterminated. Each set of serial outputs can be independently enabled by asserting the TTL input signals EN_TXA and EN_TX.

Internal Loopback

The transceiver contains an internal loopback function that bypasses the external high speed serial ports and internally feeds serialized transmit data directly to the clock and data recovery section of the deserializer. During loopback, which is enabled by asserting the LOOPEN TTL input signal, the external serial receive ports is deselected, but serial transmit data is available at the enabled transmit ports.

Repeat Mode

The transceiver contains a repeat function that retimes the received serial data using the internal clock and data recovery, and presents this data at the enabled transmit ports. This function is enabled by asserting the REPEAT TTL input signal. The repeat and loopback functions cannot be accessed simultaneously.

TTL Receiver PLL Lock to Reference Clock

The receive section of the transceiver requires the use of a lock-to-reference-clock (NLCK_REF) input to acquire frequency lock. The maximum time required for frequency lock is 1 ms.

While the NLCK_REF function is asserted, the receive section locks to the selected REFCLK and provides receive-word clock output signals (RWC0 and RWC1) that are in frequency lock with the reference clock input.

The NLCK_REF function is available at power-up, until a stable serial data stream is supplied to the device, or when the selected serial data stream has been absent or unstable in frequency for more than 50 bit times.

When NLCK_REF is deasserted, the receive section locks to the serial data stream supplied to the selected receive port, with a maximum lock time of 100 bit times, provided the frequency of the incoming bitstream is within 100 ppm of 20 times the frequency of the REFCLK signal.

Receiver Phase Discontinuity Re-lock Time

Phase discontinuities in the serial data stream will not require assertion of the NLCK_REF input. Serial data phase discontinuities will cause a loss of data integrity at the parallel receive port for no more than 100 bit times. During re-acquisition of the serial data stream, the receive word clock signals remain active. Re-lock time can be minimized by applying a high switching-density data pattern such as 101010101010101010.

Receive Word Alignment

The receive section performs word alignment to the first seven-bit of the standard 8B/10B comma + character. Word alignment may be enabled by asserting the TTL input signal EN_CDET. When word alignment occurs, RWC0 and RWC1 are not slivered or truncated, but may be stretched, and the TTL output signal COM_DET is asserted. Word alignment causes the comma + character to be output on RX(0:9).

**DATA COMM
PRODUCTS**

Table 1. Character Mapping Order

<i>Parallel TX Data</i>	<i>TX0</i>	<i>TX1</i>	<i>TX2</i>	<i>TX3</i>	<i>TX4</i>	<i>TX5</i>	<i>TX6</i>	<i>TX7</i>	<i>TX8</i>	<i>TX9</i>
<i>Parallel RX Data</i>	RX0	RX1	RX2	RX3	RX4	RX5	RX6	RX7	RX8	RX9
<i>8B/10B Position</i>	a	b	c	d	e	i	f	g	h	j
<i>Comma +</i>	0	0	1	1	1	1	1	x	x	x
<i>First Data Bit Transmitted</i>	*									

Transmit Bus Clock Modes

Parallel transmit data is presented to the transceiver on the 20-bit TTL bus TX(0:19). The transmit data is clocked into the transceiver on the rising edge of the reference clock input or on the rising edge of TWC, dependent on the logical state of the TTL input signal CLKSEL. If CLKSEL is 0, TWC is selected as the transmit data clock source. If CLKSEL is 1, the reference clock input is selected as the transmit data clock source.

Receive Bus Clocking

The parallel receive data is output from the transceiver on the 20-bit TTL bus RX(0:19). The transmit data is clocked into the host system using the TTL clock outputs RWC0 and RWC1. RWC0 and RWC1 are differential 125 MHz signals.

Reference Clock Inputs

The reference clock input is a 125 MHz input signal used for Transmit clock generation and Receive frequency lock. There are two TTL reference clock inputs (REFCLKT1 and REFCLKT2) and two pairs of differential PECL reference clock inputs (REFCLKP1P/N and REFCLKP2P/N), which allow the use of redundant reference clocks in both TTL and PECL formats. The logical state of the TTL input signals REFSEL1 and REFSEL2 determine which reference clock inputs are selected. If REFSEL1 is 0, the inputs with suffix 1 are selected; if REFSEL1 = 1, the inputs with suffix 2 are selected. If REFSEL2 is 0, the PECL inputs are selected; if REFSEL2 = 1, the TTL inputs are selected.

Signals

Table 2. Signal Descriptions

Signal	Type	Pin No.	Description
REFCLKT1	TTL Input	38	TTL reference clock 1 input for transmit and receive PLLs.
REFCLKT2	TTL Input	39	TTL reference clock 2 input for transmit and receive PLLs.
REFCLKP1P REFCLKP1N	PECL Input	42 41	Differential PECL reference clock 1 inputs for transmit and receive PLLs.
REFCLKP2P REFCLKP2N	PECL Input	45 44	Differential PECL reference clock 2 inputs for transmit and receive PLLs.
REFSEL1	TTL Input	34	Selects reference clock inputs. If REFSEL1 = 0, inputs with suffix 1 are selected. If REFSEL1 = 1, inputs with suffix 2 are selected.
REFSEL2	TTL Input	35	Selects reference clock inputs. If REFSEL2 = 0, the PECL inputs are selected. If REFSEL2 = 1, the TTL inputs selected.
TWC	TTL Input	37	Alternate clock input for parallel transmit data bus.
CLKSEL	TTL Input	33	Selects clock input for parallel transmit data. If CLKSEL = 0, transmit data is loaded on the rising edge of TWC. If CLKSEL = 1, transmit data is loaded on the rising edge of REFCLK.
RWC0 RWC1	TTL Output	61 60	Differential clock outputs for parallel receive data bus.

(Continued on next page)

TQ9525

ADVANCE INFORMATION DATA SHEET

Table 2. Signal Descriptions (continued)

Signal	Type	Pin No.	Description
COM_DET	TTL Output	67	Asserted when the receiver detects the 8B/10B comma + character and has realigned (if necessary) this character to the receive data outputs RX(0:9).
RXSEL	TTL Input	109	Selects one of two high speed serial receive ports. If RXSEL = 0, high speed receive port "A" is selected. If RXSEL = 1, high speed receive port "B" is selected.
REPEAT	TTL Input	30	Enables the repeat function which retimes the received serial data using internal clock and data recovery, and presents this data at the enabled transmit ports.
TXA	PECL Output	123	Port "A" differential (true and complement) serial transmit outputs.
TYA		122	
TXB	PECL Output	118	Port "B" differential (true and complement) serial transmit outputs.
TYB		117	
EN_TXA	TTL Input	126	Enable input for port "A" differential (true and complement) serial transmit outputs.
EN_TXB	TTL Input	125	Enable input for port "B" differential (true and complement) serial transmit outputs.
RXA	PECL Input	100	Port "A" differential (true and complement) serial receive inputs.
RYA		102	
RXA_T	PECL TERM	99	Port "A" differential (true and complement) serial receive termination outputs used for fly-by termination.
RYA_T		103	
RXB	PECL Input	105	Port "B" differential (true and complement) serial receive inputs.
RYB		107	
RXB_T	PECL TERM	104	Port "B" differential (true and complement) serial receive termination outputs used for fly-by termination.
RYB_T		108	
TX(0:19)	TTL Input	2-5, 8-11, 14-17, 20-23, 26-29	Parallel transmit data bus. TX0 is the first bit transmitted on the serial port.
RX(0:19)	TTL Output	68-71, 74-77, 80-83, 86-89, 92-95	Parallel receive data bus. RX0 is the first bit received on the serial port.
Not Used		49, 50, 51 52, 110	Connect these pins to V _{DD} .

Electrical Specifications

Table 3. Absolute Maximum Ratings⁽³⁾

Parameter	Condition	Symbol	Minimum	Nominal	Maximum	Unit
Storage Temperature		T_{store}	-65		150	°C
Junction Temperature		T_{CH}	-65		150	°C
Case Temperature w/bias	(Note 1)	T_C	0		TBD	°C
Supply Voltage	(Note 2)	V_{DD}	0		7.0	V
Voltage to any input	(Note 2)	V_{in}	- 0.5		$V_{DD} + 0.5$	V
Voltage to any output	(Note 2)	V_{out}	- 0.5		$V_{DD} + 0.5$	V
Current to any input	(Note 2)	I_{in}	- 1.0		1.0	mA
Current from any output	(Note 2)	I_{out}			40.0	mA

Notes: 1. T_c is measured at top of case.

2. All voltages are measured with respect to GND (0V) and are continuous.

3. Absolute maximum ratings in this table are those beyond which the device's performance may be impaired and/or permanent damage may occur.

Table 4. Recommended Operating Conditions—DC Characteristics, 0–85 °C Case

Parameter	Condition	Symbol	Minimum	Nominal	Maximum	Unit
Positive Supply		V_{DD}	4.75	—	5.25	V
Current Positive supply		I_{DD}	—	1	TBD	A

TQ9525

ADVANCE INFORMATION DATA SHEET

Table 5. DC Characteristics—ECL/PECL I/O (4)

Parameter	Condition	Symbol	Minimum	Nominal	Maximum	Unit
Input Common mode voltage	(Note 1)	V_{COM}	$V_{DD} - 1500$	—	$V_{DD} - 1100$	mV
Input Differential voltage	(Note 1)	V_{DIFF}	400	—	1200	mV
Output HIGH voltage	(Note 2)	V_{OH}	$V_{DD} - 1100$	—	$V_{DD} - 600$	mV
Output LOW voltage	(Note 2)	V_{OL}	$V_{DD} - 2100$	—	$V_{DD} - 1500$	mV
Input HIGH current	$V_{IH(MAX)}$	I_{IH}	—	—	TBD	uA
Input LOW current	$V_{IL(MIN)}$	I_{IL}	TBD	—	—	uA
Output HIGH current	(Note 3)	I_{OH}	20	23	30	mA
Output LOW current	(Note 3)	I_{OL}	0	5	8	mA
Input capacitance		C_{IN}	—	TBD	—	pF
Output capacitance		C_{OUT}	—	TBD	—	pF

Table 6. DC Characteristics—TTL I/O (4)

Parameter	Condition	Symbol	Minimum	Nominal	Maximum	Unit
Input HIGH voltage		V_{IH}	2.0	—	VDD	V
Input LOW voltage		V_{IL}	0	—	0.8	V
Input HIGH current	$V_{IH(MAX)}$	I_{IH}	—	—	200	uA
Input LOW current	$V_{IL(MIN)}$	I_{IL}	-400	-200	—	uA
Output HIGH voltage	$I_{OH} = -1 \text{ mA}$	V_{OH}	2.4	—	VDD	V
Output LOW voltage	$I_{OL} = 1 \text{ mA}$	V_{OL}	0	—	0.4	V
Output Available Current		I_{OAV}	TBD	—	—	mA
Output Source Current		I_{OSC}	TBD	—	—	mA
Input capacitance		C_{IN}	—	TBD	—	pF
Output capacitance		C_{OUT}	—	TBD	—	pF

Notes (Tables 3 and 4):

1. Differential inputs must be used.
2. $R_{LOAD} = 50 \text{ ohms}$ to $V_{TT} = V_{DD} - 2.0 \text{ V}$
3. Not tested; consistent with V_{OH} and V_{OL} tests.
4. Specifications apply over recommended operating ranges.

Table 7. AC Characteristics

Parameter	Condition	Symbol	Minimum	Nominal	Maximum	Unit
REFCLK or TWC Period	(Note 1)	T_{PERIOD_T}	—	8.00	—	ns
RWC(0:1) Period		T_{PERIOD_R}	—	8.00	—	ns
Serial Output Rise/Fall time	(Note 2)	$T_{R/F}$	—	—	TBD	ps
TTL Output Rise/Fall Time	(Note 3)	$T_{R/F}$	0.5	—	2.5	ns
TX Random Jitter	(Note 4)	T_{RJ}	—	—	0.1	Bit Times ⁽⁵⁾
TX Deterministic Jitter	(Note 4)	T_{DJ}	—	—	0.1	Bit Times ⁽⁵⁾
RX Jitter Tolerance	(Note 4)	T_{RJt}	—	—	TBD	Bit Times ⁽⁵⁾

Notes: 1. REFCLK must have a tolerance of 100 ppm or better. If TWC is used, it must be frequency-locked to REFCLK.

2. 20% - 80% levels. $R_{LOAD} = 50$ ohms to $V_{TT} = V_{DD} - 2.0$ V

3. Min. V_{IH} to max V_{IL} levels. $C_{LOAD} = 10$ pF

4. Peak-to-peak measurement.

5. One Bit Time = 400 ps @ 2.50 Gb/s.

Timing Specifications

Table 8. Transmit Interface Timing

Symbol	Parameter	Minimum	Maximum	Unit
$T_{SETUP-T}$	Data setup time to REFCLK/TWC rising edge	2.0		ns
T_{HOLD-T}	Data hold time from REFCLK/TWC rising edge	1.5		ns
T_{DUTY-T}	REFCLK/TWC duty cycle	40	60	%

Table 9. Receive Interface Timing

Symbol	Parameter	Minimum	Maximum	Unit
$T_{SETUP-R}$	Data valid time before RWC0 rising edge Data valid time before RWC1 falling edge	3.0		ns
T_{HOLD-R}	Data valid time after RWC0 rising edge Data valid time after RWC1 falling edge	1.5		ns
T_{DUTY-R}	RWC(0:1) duty cycle	40	60	%
T_{SKEW-R}	Skew from RWC0 rising edge to RWC1 falling edge		1.0	ns
$T_{LOCK1-R}$	Application of REFCLK to de-assertion of NLCK_REF		1.0	ms
$T_{LOCK2-R}$	Deassertion of NLCK_REF to bit synchronization (Frequency of incoming Bitstream within 100ppm of 20 x Frequency of REFCLK)		100	Bit Times ¹
$T_{LOCK3-R}$	Re-lock after serial data phase discontinuity		100	Bit Times ¹

Notes: 1. One Bit Time = 400 ps @ 2.50 Gb/s.

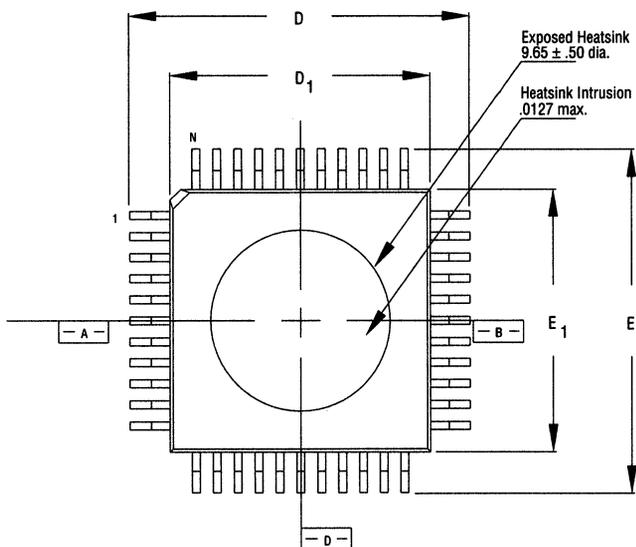
TQ9525

ADVANCE INFORMATION DATA SHEET

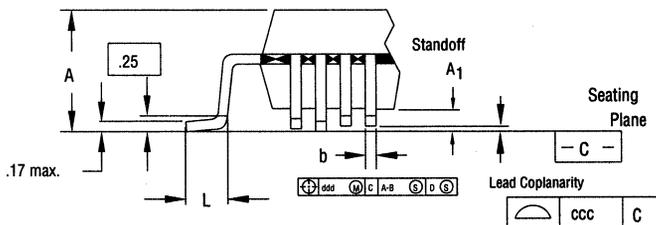
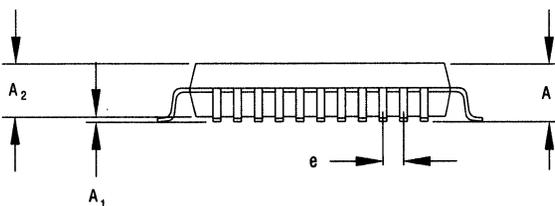
Mechanical Package

Figure 2. TQ9525 Dimensions (128 pins, 14x14 mm, thermally enhanced)

Dim.	Value
A	1.60 max.
A ₁	0.05 min. / 0.15 max.
A ₂	1.40 ± .05
D	16.0 ± .20
D ₁	14.00 ± .05
E	16.0 ± .20
E ₁	14.00 ± .05
L	0.75 max. / 0.50 min.
b	0.18 ± .05
ccc	0.08 max.
ddd	0.07 max.
e	0.40
N	128 pins



Note: All dimensions in millimeters (mm).



Ordering Information**TQ9525** *2.5 Gb/s 20-bit Transceiver***Additional Information**

For latest specifications, additional product information,
worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com **Tel:** (503) 615-9000
Email: sales@tqs.com **Fax:** (503) 615-8900

For technical questions and additional information on specific applications:

Email: applications@tqs.com

The information provided herein is believed to be reliable; TriQuint assumes no liability for inaccuracies or omissions. TriQuint assumes no responsibility for the use of this information, and all such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. TriQuint does not authorize or warrant any TriQuint product for use in life-support devices and/or systems.

Copyright © 1997 TriQuint Semiconductor, Inc. All rights reserved.

Revision A.0.A October 1997

TQ9525

ADVANCE INFORMATION DATA SHEET

Section 5 — Mixed Signal Products

TQ6122 1 Gs/s 8-bit Digital-to-Analog Convertor ***5-3***

TQ6124 1 Gs/s 14-bit Digital-to-Analog Convertor ***5-27***



TQ6122

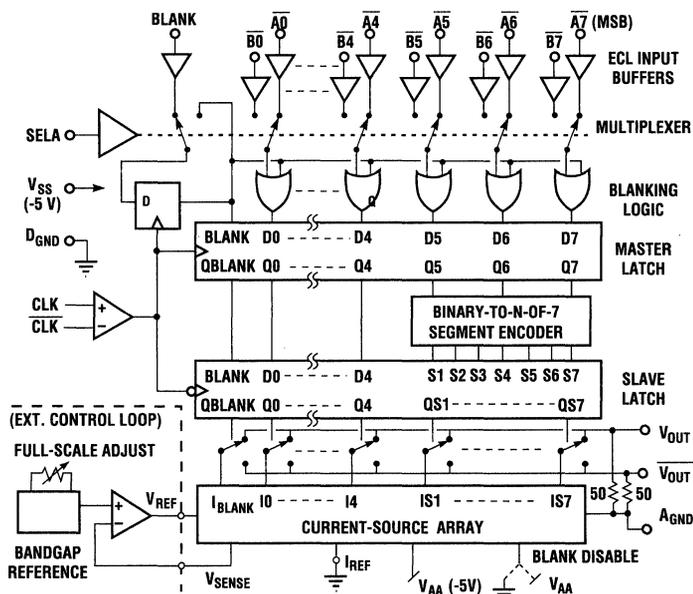
1 Gigasample/sec, 8-bit Digital-to-Analog Converter

Features

- 1 Gs/s conversion rate
- 8-bit resolution
- DC differential non-linearity $1/2$ LSB (0.2%)
- DC integral non-linearity 1 LSB (0.4%)
- Settling time 2 ns to 0.4% (est.)
- Spurious-free dynamic range (SFDR) 45 dBc typical
- ECL-compatible inputs
- Synchronous blanking input
- 1.3 W power dissipation
- 44-pin multilayer ceramic package or unpackaged die

Applications

- Display generation
- Waveform and signal synthesis
- Video signal reconstruction



TriQuint's TQ6122 GIGADAC™ is a monolithic, 8-bit digital-to-analog converter capable of conversion rates to at least 1000 Megasamples/second. The TQ6122 DAC may be used for display generation, waveform and signal synthesis, and video signal reconstruction. The TQ6122 features a 2:1 data MUX at the input for ease of interface and offers synchronous blanking capability for maximum ease of use in video applications. It drives complementary 1 V peak-to-peak swings into 50-ohm loads; on-chip 50-ohm reverse terminations provide extremely fast settling time.

Due to the inherently high speed of TriQuint's one-micron gate Enhancement / Depletion-mode gallium arsenide process, the TQ6122 offers guaranteed operation at clock rates of 1000 MHz, with typical room temperature conversion rates of 1.5 Gs/s without multiplexing and 1.3 Gs/s when using multiplexed inputs. The TQ6122 features output rise and fall times of 500 ps (10% – 90%), symmetric complementary output transitions, and glitch impulse values less than 10 pV/sec. When used for sine wave synthesis, typical spurious and harmonic free dynamic range is 45 dBc.

The TQ6122 may be retrofitted into designs which currently use TriQuint's TQ6111, 2, 3, 4M DACs with minimal changes to power supply levels and input and output connections. The part is available in a 44-pin ceramic package or as unpackaged die.

Specifications

Table 1. Absolute Maximum Ratings (1,2)

Symbol	Description	Min	Typ	Max	Units
A_{GND}, D_{GND}	Analog and digital ground	-2		+2	V
V_{SS}	Digital power	-7			V
V_{AA}	Analog power	-10			V
$V_O, \overline{V_O} (MAX)$	Analog output (1 V F.S.)	-2.5		+2.5	V
$V_I (MAX)$	Digital input levels	$V_{SS} - 0.5$		+0.5	V
$I_I (MAX)$	Digital input currents	-1		+1	mA
P_D	Power dissipation			3.0	W
T_C	Case backside temperature	-65		+135	°C
T_S	Storage temperature	-65		+150	°C

Notes: 1. Unless otherwise specified: $A_{GND} = D_{GND} = 0$ V, $V_{SS} = V_{AA} = -5$ V, $V_{FS} = 1$ V pk-pk, case temperature = 27 °C.

2. Exceeding the absolute maximum ratings may damage the device. The value shown for a particular parameter is determined with all other parameters at their nominal values.

Table 2. DC Characteristics (1)

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Unit
V_{AA}	Analog supply	Note 2	-5.25		-4.75	V
I_{AA}	V_{AA} current	$V_{FS} = 1$ V pk-pk	50	62	80	mA
V_{SS}	Digital supply	Note 2	-5.5		-4.5	V
I_{SS}	V_{SS} current		145	200	265	mA
P_D	Power dissipation		0.9	1.3	1.85	W
V_{ECLREF}	ECL reference level	Note 3, Figure 1	-1.5	-1.3	-1.1	V
I_{ECLREF}	ECL ref. input bias current	Note 3, Figure 1 $\Delta V_{ECLREF} = \pm 0.2$ V	-5	0	+5	mA
R_{ECLREF}	ECL ref. input resistance	Figure 1		50		
C_{ECLREF}	ECL ref. input capacitance			2		pF
$V_{IH(DC)}$	Data input HIGH (ECL)	DC value ($V_{ECLREF} = -1.3$ V)	-1100		-500	mV
$V_{IL(DC)}$	Data input LOW (ECL)	DC value ($V_{ECLREF} = -1.3$ V)	V_{TT}		-1500	mV
$V_{CLKH(DC)}, \overline{V_{CLKH(DC)}}$	Clock HIGH input	Differential clock, Note 4	$V_{ECLREF} + 0.3$		-0.7	V
$V_{CLKL(DC)}, \overline{V_{CLKL(DC)}}$	Clock LOW input	Differential clock, Note 4	V_{TT}		$V_{ECLREF} - 0.3$	V
I_{IN}	Data, clock input bias current	$V_{IH} = -800$ mV, $V_{IL} = -1800$ mV	-25		+25	uA
C_{IN}	Data, clock input capacitance	In multilayer ceramic package		0.5		pF
$\overline{V_{OUT(MAX)}}, V_{OUT(MAX)}$	Maximum absolute output level	Note 5			+1	V
$V_{OUT(MIN)}, \overline{V_{OUT(MIN)}}$	Minimum absolute output level	Note 5	-1.5			V

(Continued on next page)

Table 2. DC Characteristics ⁽¹⁾ (continued)

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
V _{FS}	Full-scale output swing	Data bits only, 0–0/1–1 input step R _L = 50 load	0	1	1.125	V pk–pk
V _{ZS}	Zero-scale offset	V _{FS} = 1 V, no external offset, V _{BLANK_DISABLE} = 0 V		–35		mV
D V _{BLANK}	Blanking interval	Blank input = 1, Notes 6, 7	9	10.4	12	%V _{FS}
V _{BLANK_DISABLE}	Blank current disable control	Blank current ON Blank current OFF		–5 (V _{AA}) 0 (A _{GND})		V V
V _{REF}	V _{REF} input voltage	V _{FS} = 1 V peak-to-peak V _{FS} = 0 V peak-to-peak	V _{AA} +0.7 V _{AA} –1	V _{AA} +1.0	V _{AA} +1.4	V V
V _{SENSE}	V _{SENSE} output	V _{FS} = 1 V peak-to-peak		V _{AA} +0.8	V _{AA} +1.1	V
I _{VREF}	V _{REF} input current	V _{REF} = V _{AA} + 0.65 V _{REF} = V _{AA} + 1.1		10	1	uA mA
I _{REF}	Ext. reference current output	V _{FS} = 1 V peak-to-peak	2	2.5	5	mA
V _{IREF}	I _{REF} terminal voltage		–1.5		+1	V
R _{OUT} , \overline{R}_{OUT}	V _{OUT} , \overline{V}_{OUT} output resistance Matching of R _{OUT} , \overline{R}_{OUT}		44	50 0.2	57 2.5	% %
C _{OUT}	V _{OUT} , \overline{V}_{OUT} output capacitance			0.3		pF
	Resolution				8	Bits
	Monotonicity		8			Bits
DNL	Differential non-linearity	(± 1/2 LSB)			0.2	% F.S.
INL	Integral non-linearity	(± 1 LSB)			0.4	% F.S.
	Full-scale symmetry	V _{FS} = 1 V peak-to-peak, Note 8	–4		+4	mV
	V _{FS} temperature coefficient	Note 9				

Notes: 1. Unless otherwise specified: V_{AA} = –5V ± 5%, V_{SS} = –5 V ± 10%, V_{TT} = –2V ± 5%, V_{FS} = 1 V pk–pk, T_{CASE} = 0 to +85 °C

2. See the "Power Supplies, Ground and Bypassing" section later in this datasheet for discussion of power supplies.

3. The ECL reference input establishes the switching point for the ECL line receivers used at the DATA, BLANK, and SELECT inputs. (See Figure 1.) I_{ECLREF} is the current required to change the internal ECLREF value by about ±200 mV.

4. Values shown are for differential clock drive, and apply to both CLOCK and \overline{CLOCK} inputs. For single-ended drive, the HIGH level should be at least (V_{ECLREF} + 0.5) volts, but must not exceed –700 mV. The LOW level should be (V_{ECLREF} – 0.5) volts, but must not go below V_{TT}, where V_{TT} is the ECL termination voltage (nominal V_{TT} = –2 V).

5. V_{OUT(MAX)}, $\overline{V}_{OUT(MAX)}$, V_{OUT(MIN)}, $\overline{V}_{OUT(MIN)}$ represent the limits on the absolute output levels, including offset.

6. Blanking interval is the voltage change (as a percentage of the full-scale output swing) added to V_{FS} when BLANK is asserted.

7. The BLANK DISABLE input turns OFF the blank current (DV_{BLANK} = 0) when held at A_{GND}, and turns it ON when pulled to V_{AA}.

8. Full-scale symmetry is a measure of the balance between V_{OUT} and \overline{V}_{OUT} . For a full-scale input change (00000000 → 11111111), the change in \overline{V}_{OUT} will match the change in V_{OUT} to within ± 4 mV (1 LSB @ 1 V peak-to-peak).

9. The VFS temperature coefficient is determined primarily by the external reference and loop control op amp.

Table 3. AC Characteristics (1,2)

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
$F_{CLK(MAX)}$	Maximum clock frequency	Unmuxed operation	1000	1500		MHz
		Muxed operation	1000	1300		MHz
$T_{RCLK,DATA}$	Clock, data input rise time	20% to 80%		300		ps
$T_{FCLK,DATA}$	Clock, data input fall time	20% to 80%		300		ps
T_{WH}	Duration of clock HIGH	Percentage of clock period	40	50	60	%
T_{WL}	Duration of clock LOW	Percentage of clock period	40	50	60	%
T_{SETUP}	Data, control setup time	See Figure 7				ps
T_{HOLD}	Data, control hold time	See Figure 7				ps
T_{ROUT}	Output rise time	10% to 90%		300		ps
T_{FOUT}	Output fall time	10% to 90%		300		ps
T_{SETTLE}	Output settling time	Within $\pm 0.4\%$ of final value		2		ns
	Glitch impulse				10	pV/sec

Notes: 1. Unless otherwise specified: $V_{AA} = -5V \pm 5\%$, $V_{SS} = -5V \pm 10\%$, $V_{FS} = 1V \rho\text{-}\rho$, $T_{CASE} = 0 \text{ to } +85^\circ\text{C}$,
 $V_{ECL} = -1.3V$, $V_{IH} = -0.8V$, $V_{IL} = -1.8V$
 2. Applies to packaged parts only.

Figure 1. ECL Reference Input Equivalent Circuit

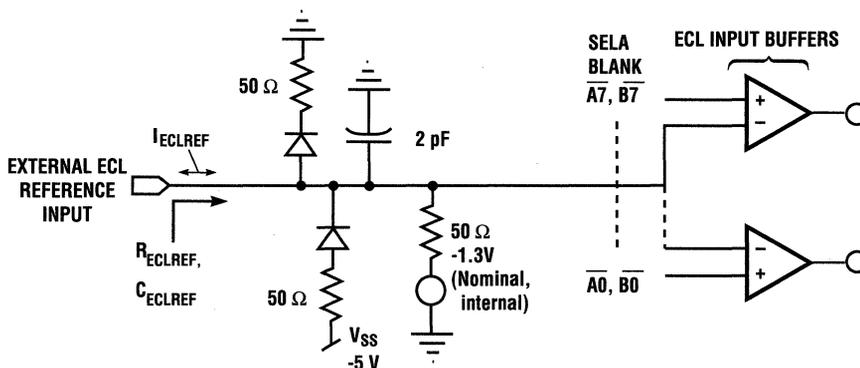


Figure 2. Definition of V_{IH} , V_{IL} for Data and BLANK Inputs

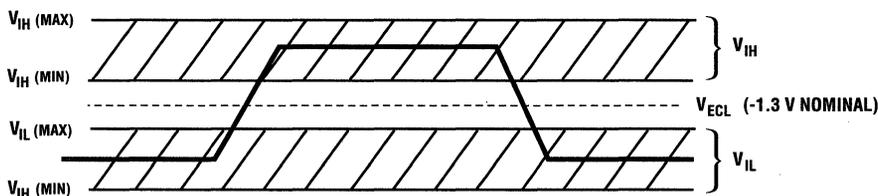
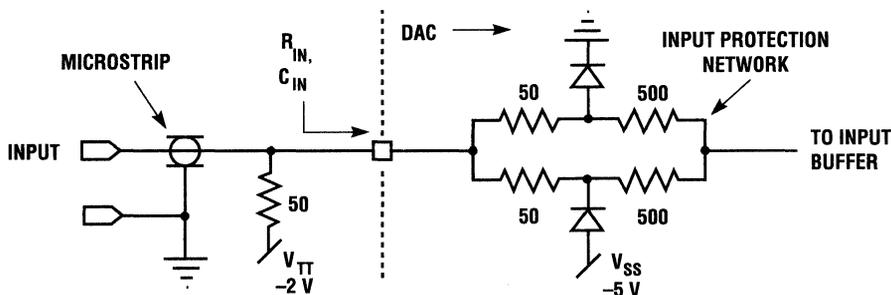


Figure 3. Typical Digital Input Circuit (Including CLOCK Inputs)

Figure 4. V_{OUT} , $\overline{V_{OUT}}$, and Input Code Relationships for (A) Typical Instrumentation and (B) Video Configurations**(A) TQ6122 Instrumentation DAC operation (1 V Full-Scale)**

Blanking current is shunted to ground by tying BLANK DISABLE to A_{GND} and forcing BLANK = 0.

	Input Code	$V_{OUT}^{(1)}$	$\overline{V_{OUT}}^{(1)}$
Full Scale	11111111	-0.996 V	0.000 V
Full Scale - 1 LSB	11111110	-0.992 V	-0.004 V
Half Scale + 1 LSB	10000001	-0.504 V	-0.492 V
Half Scale	10000000	-0.500 V	-0.496 V
Half Scale - 1 LSB	01111111	-0.496 V	-0.500 V
Zero Scale + 1 LSB	00000001	-0.004 V	-0.992 V
Zero Scale	00000000	0.000 V	-0.996 V

(B) TQ6122 Video DAC Operation (0.679 V Full-Scale)

Blanking current is enabled by connecting BLANK DISABLE to V_{AA} .

	Input Code	$V_{OUT}^{(1)}$	$\overline{V_{OUT}}^{(1)}$
Full Scale	11111111	-0.679 V	-0.071 V
Full Scale - 1 LSB	11111110	-0.676 V	-0.074 V
Half Scale + 1 LSB	10000001	-0.343 V	-0.407 V
Half Scale	10000000	-0.341 V	-0.409 V
Half Scale - 1 LSB	01111111	-0.338 V	-0.412 V
Zero Scale + 1 LSB	00000001	-0.003 V	-0.747 V
Zero Scale	00000000	0.000 V	-0.750 V
BLANK = HIGH	X X	-0.750 V	0.000 V

Notes: 1. All values shown for V_{OUT} and $\overline{V_{OUT}}$ assume identical load resistors ($RL1$ and $RL2$ in Figure 5), and no externally imposed output offset voltage (V_{OS} in Figure 5). Zero-scale offset is ignored.

Figure 5. Output Equivalent Circuit, Showing Terminated 50-ohm Transmission Line Loads

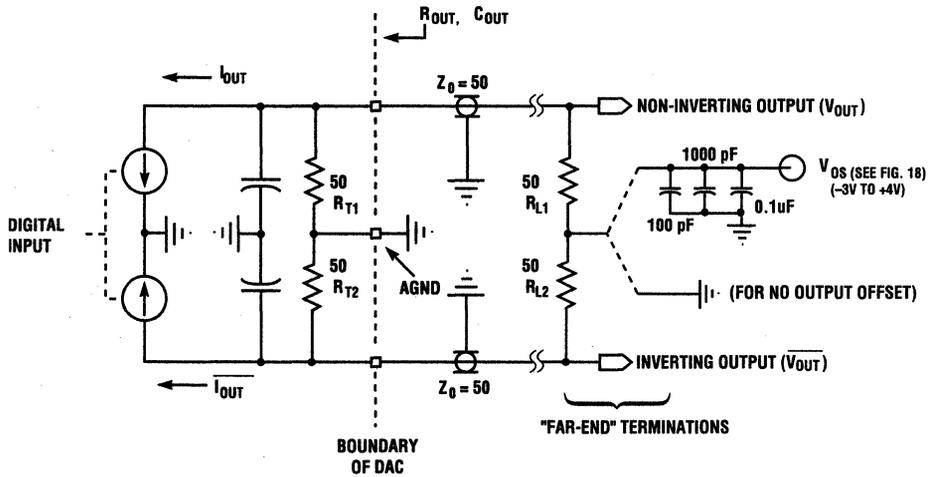


Figure 6. Definition of T_{WH} and T_{WL}

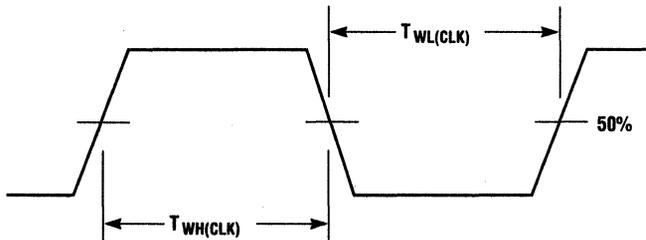
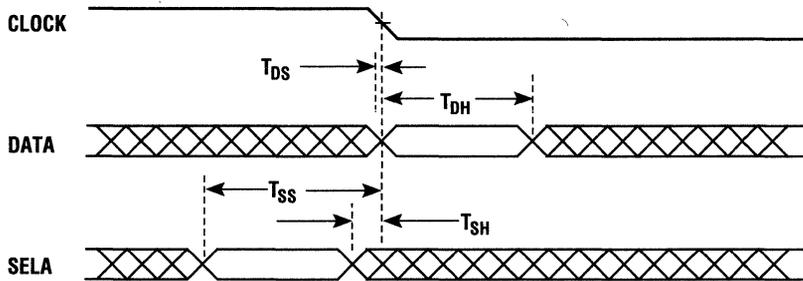


Figure 7. TQ6122 Data and Control Timing



Symbol	Description	Typical @ 25 °C	Unit
T_{DS}	Data setup time ⁽¹⁾	0	ps
T_{DH}	Data hold time ⁽²⁾	+325	ps
T_{SS}	SELA setup time ^(1,3)	+350	ps
T_{SH}	SELA hold time ^(2,3)	-100	ps

- Notes:
1. Setup time is defined to be positive for data or control transitions occurring before the negative-going edge of the clock.
 2. Hold time is defined to be positive for data or control transitions occurring after the negative-going edge of the clock.
 3. While SELA does not strictly have a setup and hold time, it is convenient to express its allowed transition region limits in these terms.

Figure 10. Package Dimensions

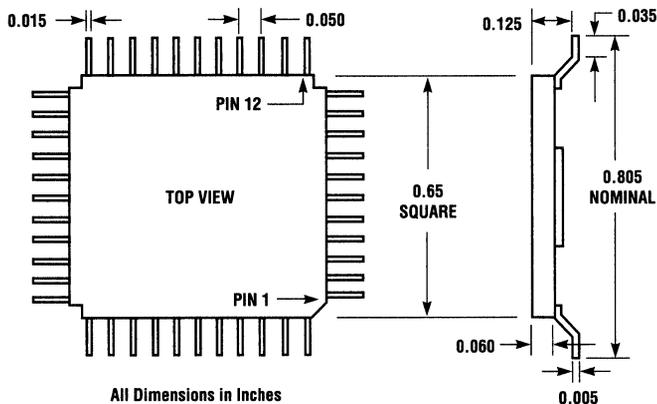


Figure 11. Mounting Footprint

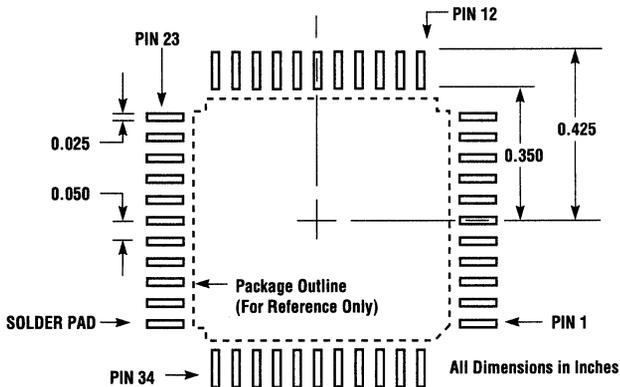
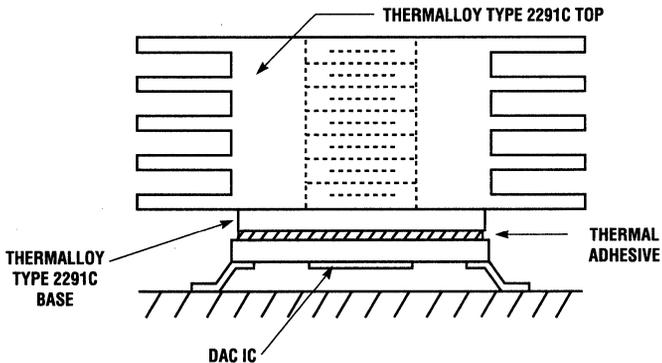


Figure 12. Heat-Sink Mounting Arrangement (heat sink not included)



Use Loctite "Output" Thermal Conductive Adhesive (Loctite item number 00241) or equivalent to attach heat sink base to IC.

MIXED SIGNAL PRODUCTS

Circuit Description

The TQ6122 DAC is based on a current-steering architecture in which weighted currents are switched by an array of differential-pair switches into either the V_{OUT} or $\overline{V_{OUT}}$ output, depending on the state of the input data and blanking bits. Essentially, the DAC is comprised of six circuit blocks: the input buffer, the data multiplexer, blanking logic, master/slave latch array with segment encode logic, differential-pair switches, and the current source array. (See figure on page 1.)

Input Buffers

The input buffers compare the ECL data and control input signals with the ECLREF level, amplify the difference, and translate this signal to the logic levels used within the IC. By default, the ECL reference is set by an internal generator; however, for best performance and maximum noise margin over temperature, power supply, and device-to-device variations, the user should provide an external level. For general-purpose applications, a simple resistive divider between D_{GND} and V_{TT} will suffice. For extreme environments or for maximum performance, the ECLREF level should be slaved to the centerpoint of the incoming data. Refer to the "Digital Inputs and Terminations" discussion later in this document for additional information.

Note that the data inputs are complemented to indicate that an increasing input value results in the V_{OUT} level moving more negative.

Data Multiplexer

The DAC makes provision for accepting data from either of two sources: from a single 8-bit-wide word at the full conversion rate, or from two 8-bit-wide half-speed words which are multiplexed together inside the DAC under the control of the SELA input. In use, the SELA input is set HIGH to select the A-Word data and

LOW to select the B-Word. It is generally best to use the A-Word input when operating the DAC unmultiplexed, although the B-Word supports full-rate transfers.

Blanking Logic

A separate BLANK input is included to allow the DAC to be used in video display applications. When asserted LOW, the BLANK input has no effect on the operation of the DAC, and the state of the input data words controls the positions of the current switches. When BLANK is asserted HIGH, however, all internal data bits and the internal blanking bit are synchronously forced HIGH at the next negative-going clock transition, causing the V_{OUT} output to go to its most negative level. This level is the sum of the normal level associated with an input code of 11111111 plus the increment due to the blanking current being steered away from the $\overline{V_{OUT}}$ output to V_{OUT} . See Figure 4 (B).

In order to provide more latitude in the timing of the BLANK signal, the BLANK input is sampled only when the A-Word is selected. When the B-Word is selected, the state of the BLANK input at the time the SELA control line goes LOW is held stable until SELA again goes HIGH. In situations where blanking is not used, it is important that the BLANK input be tied to a solid logic LOW to prevent accidental assertion of BLANK = HIGH. Note also that when the DAC is used in the unmultiplexed mode, the data should be brought in on the A-Word inputs, since with SELA = LOW (as would be the case for B-Word operation), a transient HIGH level at the BLANK input would never be cleared and the DAC would lock up.

The BLANK_DISABLE pin is normally tied to the V_{AA} rail, allowing I_{BLANK} to flow to the differential-pair switch and then to the selected output. For applications which do not use blanking, however, the standing offset in the $\overline{V_{OUT}}$ output due to the unswitched

blanking current would be undesirable. For cases such as these, the blanking current may be completely turned off by connecting the BLANK_DISABLE pin to A_{GND} .

Master/Slave Latch With Encode Logic

A nine-wide master latch registers the data coming from the multiplexer and blanking logic. The latch outputs are then split into two groups. The top three bits are translated into a seven-level thermometer code by a binary-to-N-of-seven encoder, while the lower five data bits and the blanking bit are simply delayed. The seven encoder outputs and the six delayed data and blanking bits are re-registered in a slave latch to minimize skew, which, in turn, reduces the glitch impulse. Latch timing is set up such that the slave latch is in the “sample” mode when the input clock is LOW, meaning that the analog output is updated at the falling edge of the clock.

Current Switches

The thermometer code outputs of the slave latch array drive seven switches, each of which steers a current equal to 1/8 of the full-scale step amplitude. The five encoded data bits, on the other hand, switch currents

with effective binary weightings from 1/16 of full scale down to 1/128 of full scale. The blanking bit steers a current which is nominally 10.4% of the full-scale amplitude.

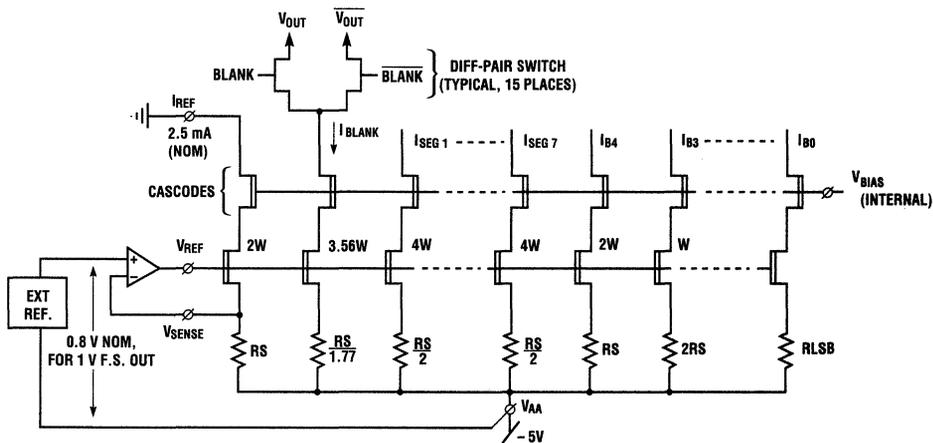
Current-Source Array

The current-source array is the heart of the DAC from an analog standpoint, and is responsible for generating the segment, bit, and blanking currents. The maximum full-scale current I_{FS} (less I_{BLANK}) is about 45 mA, providing a 1.125 volt maximum swing into the 50-ohm external load. The blanking current is nominally 10.4% of I_{FS} , corresponding to a 10-unit IRE blanking interval of 71 mV when the full-scale output is set to 0.679 volt. The I_{REF} current tracks I_{FS} , with a nominal value of 2.5 mA for $I_{FS} = 40$ mA (i.e., 6.25% of I_{FS}).

Figure 13 (A) illustrates the basic circuit of the current-source array, which consists of a set of current sources ranging from the 5 mA segment currents to the binary-weighted current sources for the lower-order bits. The circuit design utilizes source degeneration, averaging, and linear gradient cancellation techniques to obtain matching consistent with up to 10-bit linearity.

MIXED SIGNAL PRODUCTS

Figure 13 (A). Current-Source Array Circuit — V_{SENSE} -Based Control Method



TQ6122

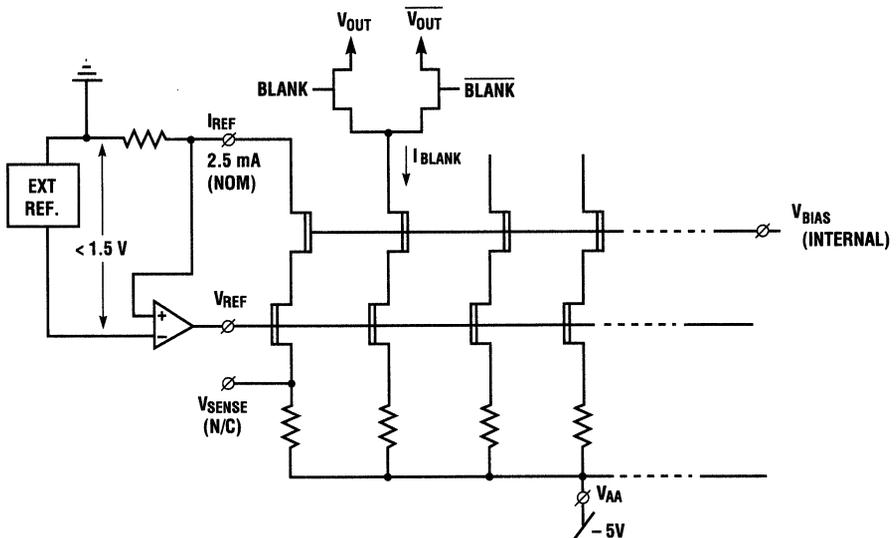
The absolute value of the current-source array output is determined using an off-chip (silicon) reference generator and op amp in a feedback-loop arrangement. In Figure 13 (A), the drop across the source degeneration resistors is compared with the level set by the external reference. Under conditions of 1 V peak-to-peak full-scale output swing, the voltage between the V_{SENSE} and V_{AA} pins of the DAC will be in the range of 0.8 V to 1.1 V, with V_{REF} being in the range of 0.7 V to 1.4 V (i.e., V_{REF} may lie above or below V_{SENSE} by several hundred millivolts). Note that, for this control method, the I_{REF} terminal must be connected to ground.

An alternative means of controlling the current-source array output is shown in Figure 13(B), with the advantage that now the reference current is being sensed *after* flowing through a path identical to that of the bit and segment currents. Thus, any error which may have occurred due to leakage will be directly corrected. Here, the V_{SENSE} pin is left disconnected and the I_{REF} current flows to ground through a stable

resistor. The value of the resistor should be chosen to drop about 1 volt under the desired operating conditions, but under no circumstances should the voltage at the I_{REF} pin be allowed to drop below -1.5 V, or the linear relationship between I_{REF} and I_{FS} will be degraded.

The primary limitation on the maximum output current is the adjustment range of V_{SENSE} : if the value of $(V_{SENSE} - V_{AA})$ exceeds about 1.2 V, the bottom current-source FETs begin to lose “headroom” by running up against the sources of the cascode transistors, causing the total current to begin limiting, as well as degrading, the linearity. If the designer is willing to accept somewhat degraded linearity and/or slightly higher power dissipation, V_{AA} may be taken down to -6 volts or so, allowing V_{REF} to be adjusted to give $(V_{SENSE} - V_{AA})$ a maximum value of about 1.5 V. This translates to an output current of about 50 mA or 1.25 V peak-to-peak into the load. Note that under these conditions, the device will not sustain any damage, but full-spec operation of the DAC is not guaranteed.

Figure 13 (B). Current-Source Array Circuit — I_{REF} -Based Control Method

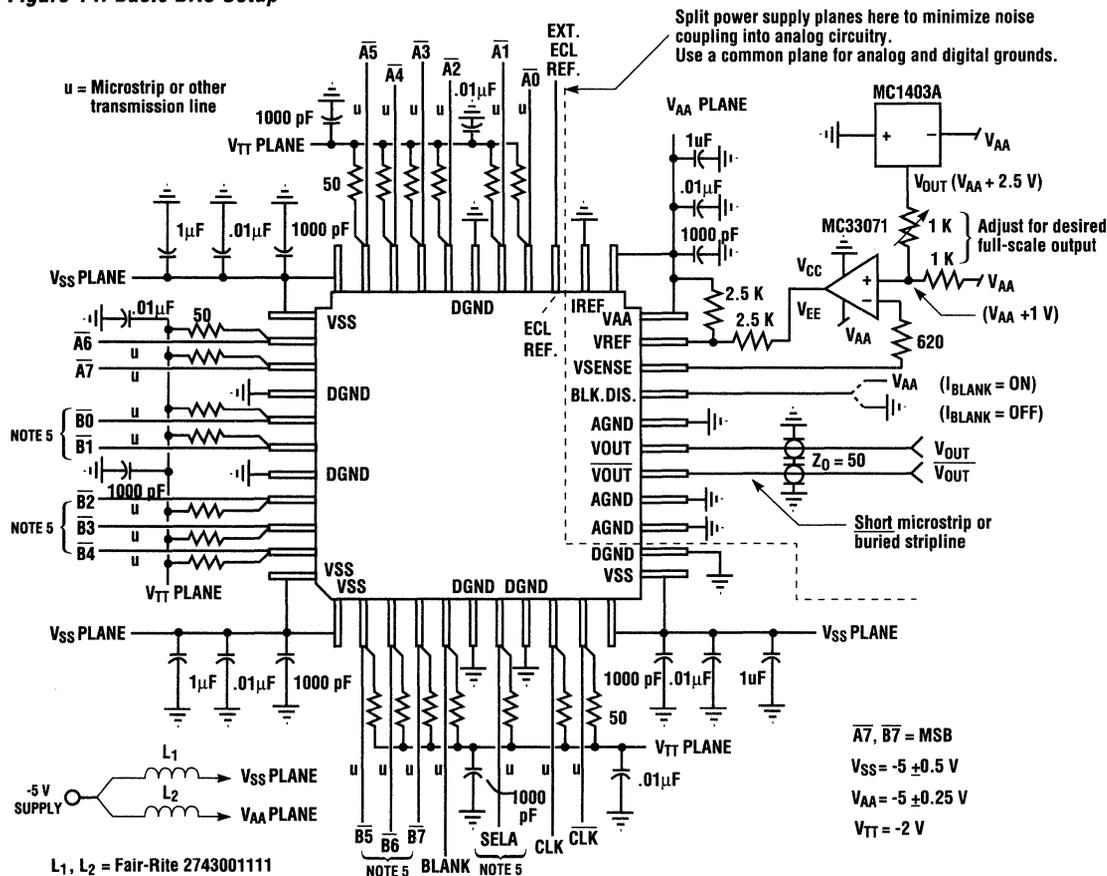


Application Information

Figure 14 illustrates the basic connection of the DAC, showing details for power supplies, data and clock inputs, and outputs terminated in 50-ohm transmission

line loads. Some issues relating to circuit board layout are also addressed.

Figure 14. Basic DAC Setup



- Notes: 1. All resistors to V_{TT} are 50-ohm, 1/8 Watt, surface-mount, mounted as close to the IC as possible.
- 2. All V_{SS} and V_{TT} capacitors are rated 15 V. All V_{AA} capacitors are rated 25 V.
- 3. Use either surface-mount components or keep minimum-length leads on all resistors and capacitors.
- 4. For best noise isolation, the analog supply (V_{AA}) and digital supply (V_{SS}) should connect at only one point, via decoupling networks such as ferrite beads.
- 5. The input circuitry for $\bar{B}0$ – $\bar{B}7$, BLANK, and SELA are the same as for $\bar{A}0$ – $\bar{A}7$.
- 6. For questions regarding board layout, please contact the factory.

Power Supplies, Ground and Bypassing

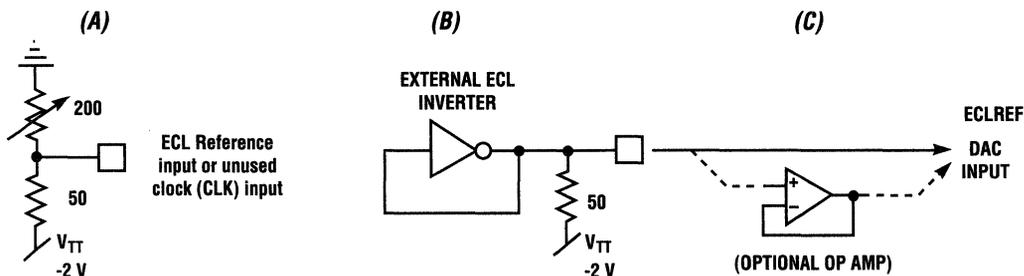
To minimize noise coupling, the digital and analog power supplies should be returned to a single-point ground, and power supply buses to the IC should have minimum impedance (power planes are best).

The supplies themselves should be well bypassed at high and low frequencies, which requires the use of several different parallel capacitors as shown. The values are not particularly critical; however, due to the fact that a capacitor looks inductive above its self-resonant frequency, one needs to use several different values in parallel, ranging from microfarads to nanofarads, in order to provide adequate wideband bypassing.

For best results, use leadless ceramic chip capacitors for bypassing, although leaded components will work satisfactorily if higher noise can be tolerated. A common ground plane has been found to give the best performance.

For best results and minimum noise, the digital and analog supplies should be physically separated on the circuit board. When using a common -5 V feed, the V_{SS} and V_{AA} planes should be isolated by ferrite beads (Fair-Rite P/N 2743001111 or equivalent) as shown in Figure 14. Using separate LM337MT regulators downstream of the ferrite beads will provide better isolation.

Figure 15. External ECL Reference Generator



Digital Inputs and Terminations

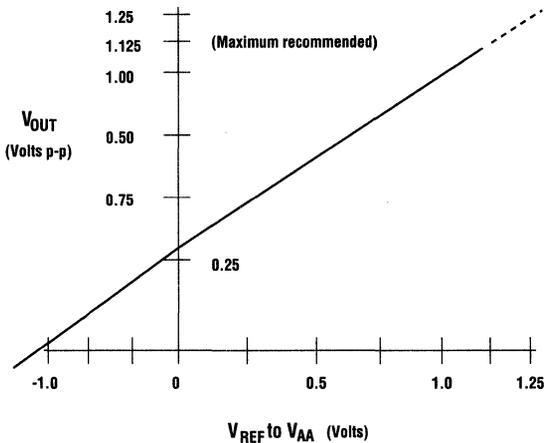
The TQ6122 DAC is designed to accept ECL logic levels at all data and control inputs. All ECL inputs, with the exception of the clock (see below), are single-ended and are compared to the ECL threshold reference of -1.3 Volts (nominal) in the input buffers of the DAC.

The ECL reference input equivalent circuit is shown in Figure 1. Several options are available to the user for externally setting the ECL reference level. The simplest option is that of a voltage divider between D_{GND} and V_{TT} , setting the ECL termination voltage as shown in Figure 15 (A). The nominal value for ECLREF is -1.3 V ; however, due to input offset variations among the input buffers or variations in V_{TT} , some adjustment above or below -1.3 V may give the best results.

A good way to settle ECLREF is to slave the ECL reference level to the center (switching) point of the input data signal. This may be accomplished in two ways: either use the V_{BB} generator output of the device which is generating the ECL signals supplied to the DAC, or use an inverter with input and output connected together to generate a level equal to the switching threshold. See Figure 15 (B). Note that the ECLREF generator should be able to source and sink up to approximately 5 mA , since the input resistance is about 50 ohms , against an internal -1.3 V (nominal) voltage source. An additional op amp may be used to give more flexibility or more robust drive. See Figure 15 (C).

op amp and reference generator, which may decrease the V_{AA} supply rejection. In circuits which use different negative rails for the DAC V_{AA} supply and the op amp, V_{REF} should be clamped to no more than two diode drops below V_{AA} , and a current-limiting resistor should be included at either the op amp output or between its negative supply input and supply input. In the event of turn-on transients and large excursions in the op amp supply before V_{AA} has settled out, these precautions will help prevent breakdown of circuitry within the DAC.

Figure 17. Typical V_{REF} -to- V_{AA} Transfer Characteristics



Full-Scale Output Adjust

The procedure for setting the full-scale output range is quite straightforward, and involves monitoring the output level(s) using a DVM. With the DAC connected to its actual V_{OUT} and $\overline{V_{OUT}}$ load(s), the output is alternately switched between steady state zero- and full-scale levels, and the reference is adjusted until the desired full-scale transition amplitude is obtained. The clock must be running and the BLANK input set to “0”. Alternatively, for a DDS application, a spectrum analyzer or a power meter may be used to monitor the full-scale output power.

Blanking Current Programming

The blanking current (I_{BLANK} in Figure 13) is turned off by connecting the BLANK_DISABLE pin to A_{GND} to divert the current away from the blank switch and the output of the DAC, and turned on by connecting BLANK_DISABLE to V_{AA} .

Output Equivalent Circuit

Figure 5 illustrates the equivalent circuit of the two DAC outputs. Each of the bit current sources is switched into either the V_{OUT} or the $\overline{V_{OUT}}$ output, depending on the data stored in the slave latches. A pair of internal 50-ohm resistors are connected from V_{OUT} and $\overline{V_{OUT}}$ to analog ground (A_{GND}), and provide reverse termination for the analog output transmission lines. Although in principle there is no restriction on the load impedance applied at the outputs, in practice, the best performance will be obtained when driving a 50-ohm terminated transmission line. This is very important from a settling standpoint, since reflections from non-50-ohm loads will superimpose with new transitions and interfere with settling. The general rule for terminating the outputs is “the cleaner, the better.”

Output Zero-Scale Adjust

The output baseline, or “zero-scale” level, may be adjusted by returning the far-end termination resistors to a well-bypassed supply level other than ground. For this general situation, reference Figure 5, the instantaneous output voltages V_{OUT} and $\overline{V_{OUT}}$ are given by:

$$V_{OUT} = V_{OS} \left(\frac{R_{T1}}{R_{L1} + R_{T1}} \right) - |I_{OUT}| (R_{L1} || R_{T1})$$

$$\overline{V_{OUT}} = V_{OS} \left(\frac{R_{T2}}{R_{L2} + R_{T2}} \right) - |\overline{I_{OUT}}| (R_{L2} || R_{T2})$$

$$I_{OUT} = \left(\frac{\text{Digital Input}}{255} \right) I_{FS}$$

$$\overline{I_{OUT}} = \left(1 - \frac{\text{Digital Input}}{255} \right) I_{FS}$$

I_{FS} = Summation of all individual bit currents
 Digital Input = Decimal equivalent of the binary input word

For the case of $R_{L1} = R_{L2} = R_{T1} = R_{T2} = 50$ ohms, V_{OS} is attenuated by 50%. An overriding factor in setting the output offset is the requirement that V_{OUT} and $\overline{V_{OUT}}$ always remain within the device's output compliance range of -1.5 V to $+1$ V. Note also that in the case of the video application of the DAC, the value of the blanking current I_{BLANK} and the state of the BLANK input must be included in the expressions for V_{OUT} and $\overline{V_{OUT}}$.

An alternative method of offsetting the output involves injecting an offset current at the output. This may be done using a current source in the form of either a resistor or a transistor as shown in Figure 18(A). The resistor has the advantage of minimizing perturbation of the transmission line impedance, with the

Figure 18(A). Alternate Output Offset Current Generators

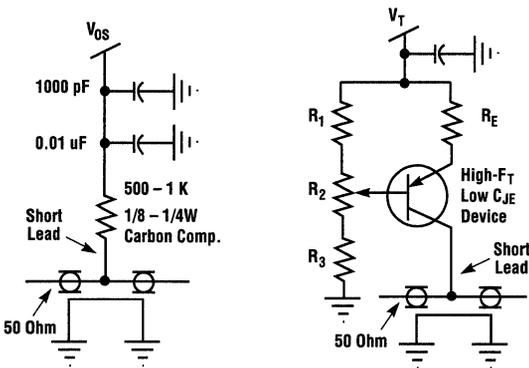
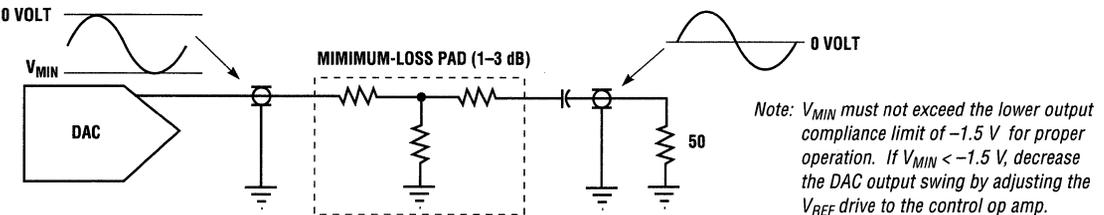


Figure 18(B). AC Coupling of Outputs



disadvantage of requiring a large supply voltage. In general, a 1/8 to 1/4 W carbon-composition resistor with a value of 500 to 1000 ohms will give good performance. Keep the lead lengths short when attaching to the circuit board and bypass the driven terminal of the resistors with a 1000 pF to 0.01 μ F SMT (surface-mount) capacitor network to the ground plane.

A transistor current source, on the other hand, requires much less power supply overhead, but adds more capacitance to the transmission line. If a transistor is used, it should be a high- F_T device with low C_{CB} or C_{DQ} (0.5 pF, if possible) and installed with short leads.

Capacitive coupling provides a means of obtaining an output centered on 0 volts. However, simply adding a coupling capacitor at one (or both) of the outputs will cause the DC output level to exceed the -1.5 V output compliance limit. The way to circumvent this problem is to add an offset current between the DAC output and the coupling capacitor (as discussed above), or to add a low-loss 50-ohm pad between the DAC and the capacitor, as shown in Figure 18(B). A "T" or " π " attenuator topology is acceptable, having 1 dB to 3 dB of attenuation. The characteristic impedance must be consistent with the overall system impedance, typically 50 ohms. This approach works, although the lower limit on the output level tends to be very close to the -1.5 V compliance limit for 1 V full-scale output swings, so some care and verification will be required.

MIXED SIGNAL PRODUCTS

Typical AC Performance

Figures 19 through 23 show typical AC performance of the TQ6122. Figures 19A and 19B illustrate the response of the DAC to an unmultiplied counter input at 1 Gs/s and 1.5 Gs/s, respectively. Blanking is enabled in both cases.

The small glitches appearing at 1/8 of full-scale intervals are shown in more detail in Figure 22.

Figure 19 (A). Unmuxed Ramp at 1000 Ms/s with Blanking (Guaranteed, 0 to +85 °C)

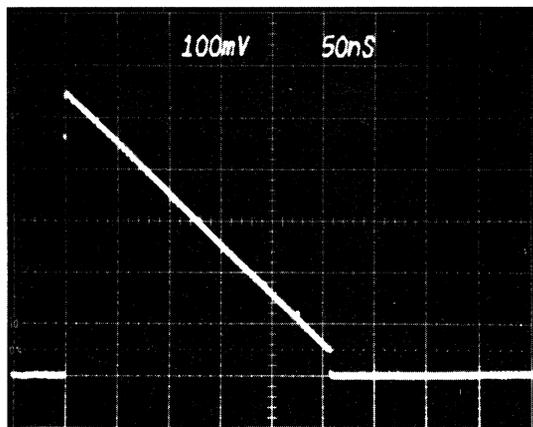
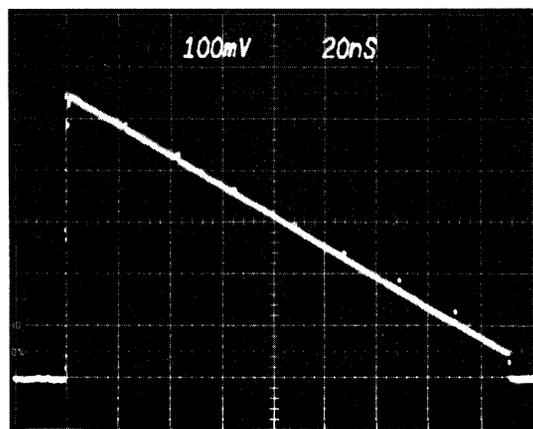


Figure 19(B). Unmuxed Ramp at 1500 Ms/s with Blanking (Typical, +25 °C)



Multiplexed behavior is shown in Figure 20A and 20B, with a counter input muxed against fixed levels at 1000 Ms/s and at 1350 Ms/s, respectively.

In Figure 20A, the ramp is muxed against a steady state mid-scale value, while in Figure 20B, the steady state input is 11111111. The apparent droop in the top level in Figure 20B is an artifact of the sampler.

Figures 19A, 19B, and 20A show the effects of blanking, while in Figure 20B, the BLANK input is held LOW, demonstrating the repetitive nature of the waveform.

Note: In Figure 20(A), A0–A7 are switched, B0–B6 are LOW, B7 is HIGH and BLANK is switched. In Figure 20(B), A0–A7 are switched, B0–B7 are HIGH, and BLANK is LOW.

Figure 20(A). Muxed Ramp at 1000 Ms/s with Blanking

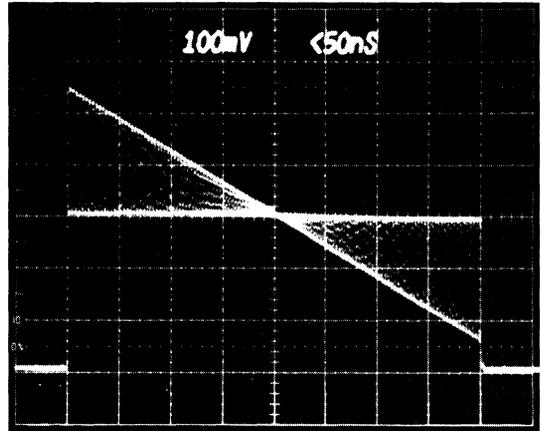


Figure 20(B). Muxed Ramp at 1350 Ms/s with Blanking Disabled

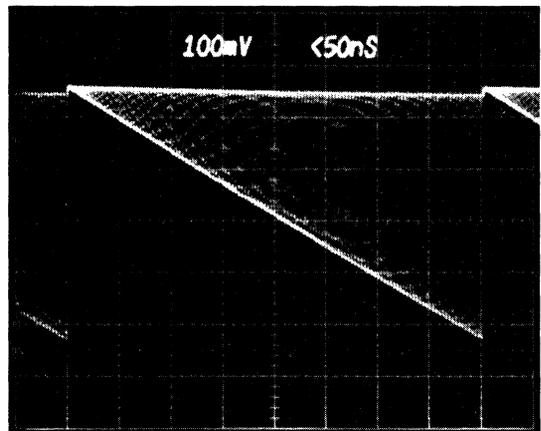


Figure 21 illustrates the symmetry of complementary full-scale transitions at V_{OUT} and $\overline{V_{OUT}}$, while Figure 22 depicts a typical worst-case glitch of 6 pV/sec.

Figure 21. Typical Full-Scale Transitions at V_{OUT} and $\overline{V_{OUT}}$ ($f_{CLK} = 1000$ MHz)

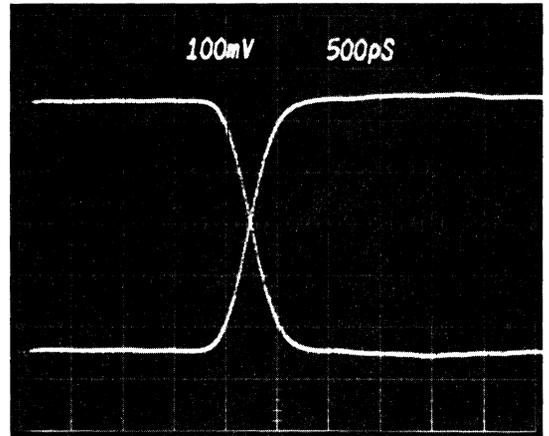


Figure 22. Typical Worst-Case Glitch Impulse ($f_{CLK} = 1000$ MHz)

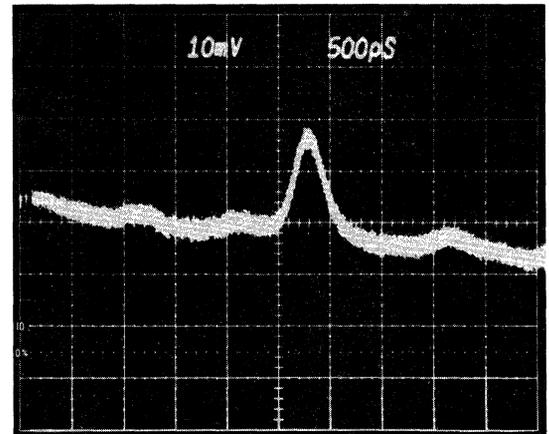


Figure 23(A). Synthesized Sine Wave Output

Figure 23(A) shows a 1 Gs/s, 58.6 MHz sine wave, and Figure 23B shows its corresponding spectrum. The spurious-free dynamic range is 46 dBc, a typical value for the device.

In Figure 23(B), the DAC output is attenuated by 6 dB going into a spectrum analyzer.

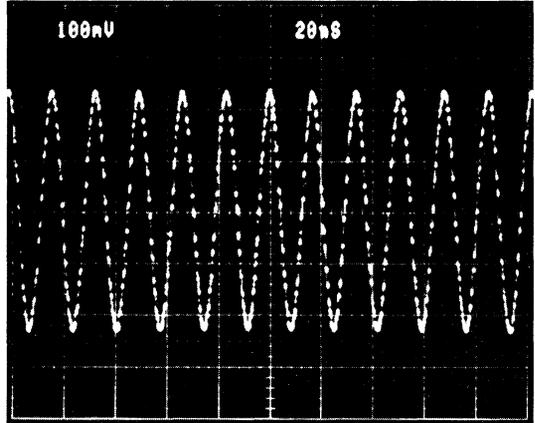
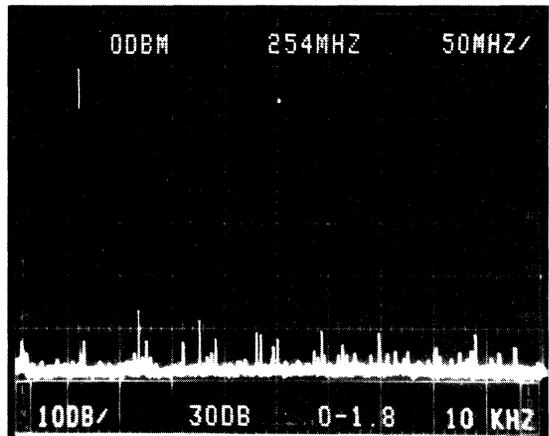


Figure 23(B). Spectrum of a 58.5 MHz Sine Wave at 1 Gs/s



MIXED SIGNAL
PRODUCTS

Figure 24 shows a modulated sine wave as an example of a more complex waveform.

Figure 24. Complex Modulated Sine Wave Pattern at 1000 Mb/s

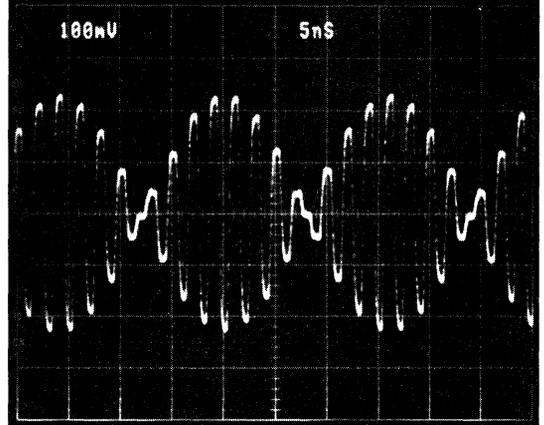
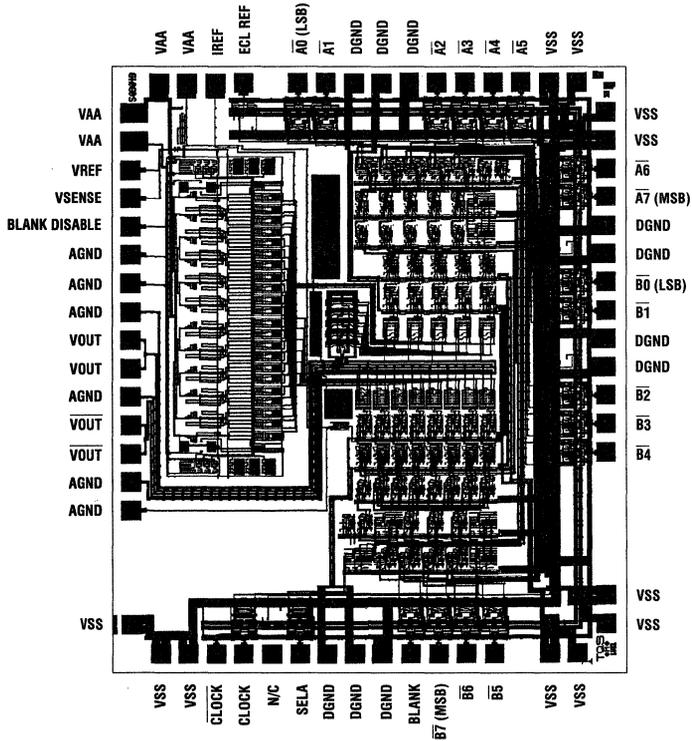


Figure 25. Chip Dimensions, Topography, and Padout

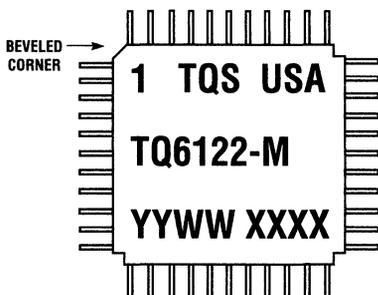


- Notes:
1. Dimensional limits unless otherwise specified: ± 2 mils ($\pm 51 \mu\text{M}$).
 2. Pins labeled N/C are not connected internally.

DIE SIZE: 129 Mils x 111 Mils (3110 μM x 2660 μM)

Figure 26. Package Labelling (44-pin packaged version)

See Figures 10, 11 and 12 for package dimensions and heat-sink mounting information.



YYWW – Date Code

XXXX - Lot Number

Component	Material
Lead	Kovar
Lead Plating	Lead/tin alloy

Ordering Information

TQ6122-M	<i>8-bit, 1 Gs/s DAC in 44-pin package</i>
TQ6122-D	<i>8-bit, 1 Gs/s DAC, die only</i>
ETF6122	<i>Engineering Test Fixture with 6122 device</i>

Additional Information

For latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com **Tel:** (503) 615-9000
Email: sales@tqs.com **Fax:** (503) 615-8900

For technical questions and additional information on specific applications:

Email: applications@tqs.com

The information provided herein is believed to be reliable; TriQuint assumes no liability for inaccuracies or omissions. TriQuint assumes no responsibility for the use of this information, and all such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. TriQuint does not authorize or warrant any TriQuint product for use in life-support devices and/or systems.

Copyright © 1997 TriQuint Semiconductor, Inc. All rights reserved.

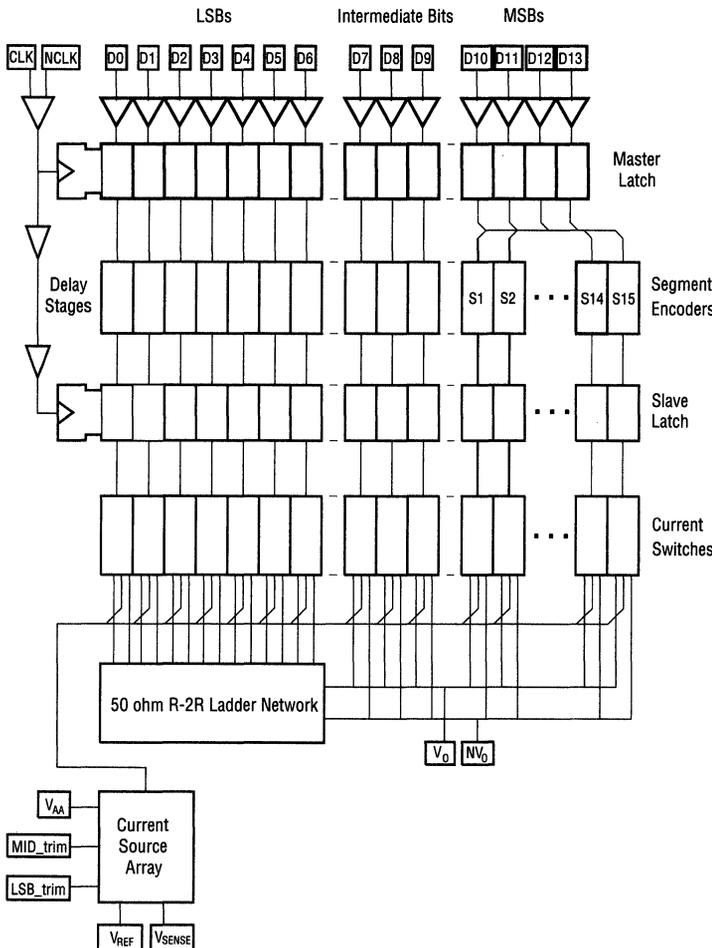
Revision 1.0.A October 1997



The TQ6124 is a 14-bit monolithic digital-to-analog converter. The TQ6124 achieves conversion accuracy by using a segmented architecture, precision current sources, and on-chip nichrome resistors. The only external components required are an external reference and loop control amplifier.

The TQ6124 is ideally suited for applications in direct digital synthesis, pixel generation for high-resolution monitors, broadband video generation, and high-speed arbitrary waveform generators.

Figure 1. TQ6124 Block Diagram



TQ6124

1 Giga-sample/sec, 14-bit Digital-to-Analog Convertor

Features

- 1 Gs/s aggregate BW
- 14-bit resolution
- RF front end
- ECL-compatible inputs
- 0.026% DC differential non-linearity
- 0.035% DC integral non-linearity
- SFDR: 52 dBc @ $F_{OUT} = 75$ MHz
48 dBc @ $F_{OUT} = 148$ MHz
45 dBc @ $F_{OUT} = 199$ MHz
- 1.4 W power dissipation
- 44-pin ceramic QFP package or die only

Applications

- Direct Digital Synthesis
- Pixel generation for workstations and high-end monitors
- Direct-generation of broadband video for cable TV
- High-speed arbitrary waveform generators

MIXED SIGNAL
PRODUCTS

Functional Description

The TQ6124 registers incoming bits in a master latch array. The value of the four most-significant bits is encoded into an n-of-15 thermometer code while the ten low-order bits pass through an equalizing delay stage. All 25 bits are re-registered in a 25-wide slave latch array which drives a set of 25 differential pair switches. These switches steer the corresponding segment and bit currents into the true (V_O) and complementary (NV_O) outputs. This architecture minimizes glitch impulses by eliminating large mid-scale current transitions.

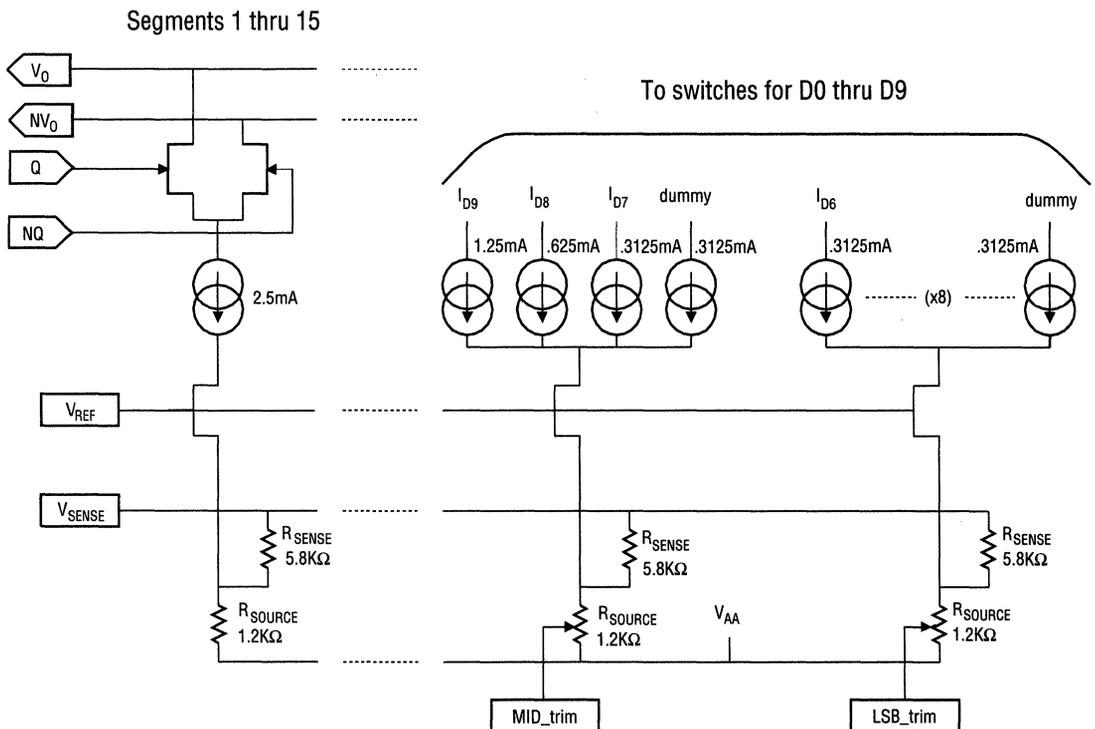
The most-significant bits generate the segment currents, which are of equal weight at $1/16$ of the full-scale output (I_{FS}). The ten lower-order bits are divided into two subgroups. The three intermediate bits steer

binary-weighted currents of magnitude $I_{FS}/32$, $I_{FS}/64$ and $I_{FS}/128$ to the outputs. The seven least-significant bits steer identical $I_{FS}/128$ currents into a differential R-2R ladder to generate effective bit currents of $I_{FS}/256$ to $I_{FS}/16384$. The DAC output is the sum of the outputs of the segments and the low-order bits.

Clock and data inputs are ECL-compatible. The outputs are designed to operate into a 50 load, with internal reverse termination to ground being provided by the R-2R network.

External compensation is utilized to minimize the effects of device mismatch. An external op amp senses the sum of the segment, the intermediate bit, and the LSB currents.

Figure 2. TQ6124 Currents



Electrical Specifications

Table 1. Recommended Operating Conditions

Symbol	Parameter	Min.	Nom.	Max.	Unit
V _{SS}	Negative Power Supply	-5.25	-5.0	-4.75	V
V _{AA}	Analog Power Supply	-15.5	-12	-11.5	V
T _C	Case Temperature	-20		85	°C

Table 2. DC Operating Characteristics

Unless otherwise specified, measured over Recommended Operating Conditions with balanced 50 loads, V_{FS} = 1.0 V.

Symbol	Parameter	Condition	Min.	Nom.	Max.	Unit
I _{AA}	V _{AA} Supply Current			-75	-90	mA
I _{SS}	V _{SS} Supply Current			-285	-450	mA
V _{REF}	Reference Voltage		V _{AA} + 2.5	V _{AA} + 3.0	V _{AA} + 3.75	V
I _{REF}	Reference input current		-25		25	mA
V _{IH}	ECL Input High Voltage	V _{REF} = -1.3 V	-1.1		-0.6	V
V _{IL}	ECL Input Low Voltage	V _{REF} = -1.3 V	-2.5		-1.5	V
I _I	ECL Input Current		-25		25	mA
V _{EREF}	ECL Reference Voltage	V _{SS} = -5.0 V		-1.34		V
R _{EREF}	ECL Reference Resistance			400		ohms
DNL	Differential non-linearity	(Note 2)	-0.05	0.026	0.05	%F.S.
INL	Integral non-linearity	(Note 2)	-0.05	0.035	0.05	%F.S.
	Full-scale symmetry	(Note 1)	-8	2	8	mV
V _{FS}	Full-scale output voltage	R _L = 50 ohms		-1.0	-1.125	V
R _{OUT}	V _O , NV _O , output resistance		44	50.9	57	ohms
	R _{OUT} Matching		-2.5	0.15	2.5	%
V _O , NV _O	Output Voltage		-1.125		0	V
V _{ZS}	Zero Scale Voltage		-50	-40	0	mV
V _{SENSE}	Sense output voltage		V _{AA} + 2.5		V _{AA} + 3.75	V
θ _{JC}	Thermal Impedance			15		°C/W

Notes: 1. Full-scale symmetry is a measure of the balance between V_O and NV_O. For a full-scale output transition, the change in V_O will match the change in NV_O to within the specified amount. Any imbalance in the output loads will affect symmetry.

2. Linearity can be interpreted as 10 bits at 1/2 LSB or as 11 bits at 1 LSB. The device is monotonic to 10 bits. Linearity is tested with the Mid_trim set for optimal DNL, with the LSB_trim pin open.

TQ6124

Table 3. AC Operating Characteristics

Unless otherwise noted, measured over DC operating characteristics with balanced 50 loads, $V_{FS} = 0.8V$, $V_{IN} = 0.8V_{p-p}$, input rise and fall times 300 ps.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{CLK}	Clock Frequency		50		1000	MHz
t_R, t_F	At full scale	10% to 90%			350	ps
t_{DS}	Data Setup Time		200			ps
t_{DH}	Data Hold Time		300			ps
t_{CLKHI}	Clock High Time		400			ps
t_{CLKLO}	Clock Low Time		400			ps
SFDR*	Spurious free dynamic range	$F_{OUT} = 75$ MHz	45	52		dBc
		$F_{OUT} = 148$ MHz	45	52		dBc
		$F_{OUT} = 199$ MHz	45	49		dBc

*Note: SFDR testing performed at $F_{CLK} = 600$ MHz only.

Table 4. Absolute Maximum Ratings

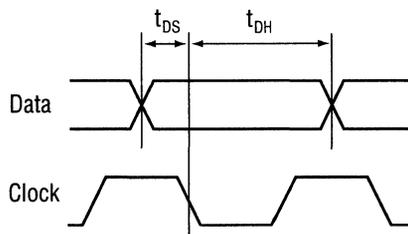
Symbol	Parameter	Min.	Max.	Unit
V_{SS}	Digital Supply	-7.0		V
V_{AA}	Analog Supply	-16.0		V
V_O, NV_O	Analog Output Voltage	-2.0	2.0	V
V_I	Digital Input Voltage	$V_{SS} - 0.5$	+0.5	V
I_I	Digital Input Current	-1.0	+1.0	mA
V_{REF}	Reference Voltage	$V_{AA} - 2$	0	V
I_{REF}	Reference Current	-1	1	mA
	Power Dissipation		5	W
T_{STG}	Storage Temperature	-65	150	°C
T_J	Operating Junction Temperature		150	°C

Note: Absolute Maximum Ratings are those beyond which the integrity of the device cannot be guaranteed. If the device is subjected to the limits in the absolute maximum ratings, its reliability may be impaired. The Electrical Specifications tables provide conditions for actual device operation.

AC Timing

The low-going transition of CLK latches the data. Production SFDR testing is performed with the clock transitioning in the center of the data eye. The timing of the clock transition with respect to the data can improve SFDR performance. Systems working to optimize SFDR can 'tune' this phase relationship to optimize the desired characteristic.

Figure 3. AC Timing Relationships



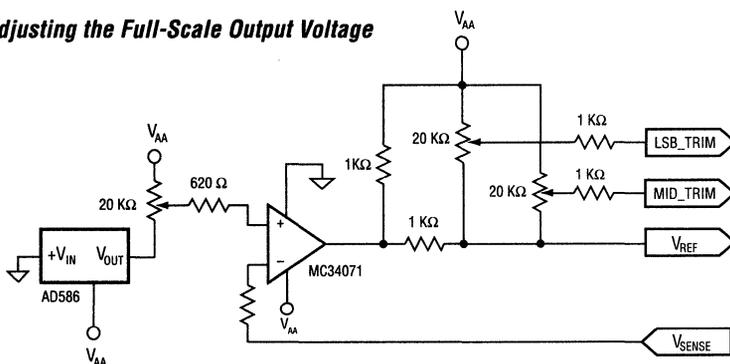
Operating Notes

Current Source Control Loop

The full scale output voltage is set through the use of an external op amp, as shown in Figure 4. Nominal full scale output voltage can be achieved by using a voltage source. With this, control voltages on the op amp of

around $V_{AA}+3V$ can be set. Adjusting the full scale output voltage can be achieved by toggling the inputs over full scale while adjusting the control voltage to achieve the desired level.

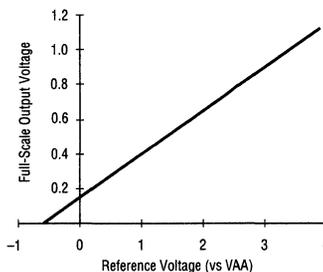
Figure 4. Adjusting the Full-Scale Output Voltage



V_{REF} Adjustment Range

The output full scale voltage range can be set through the V_{REF} input. Figure 5 shows the approximate relationship between V_{REF} and V_{FS} .

Figure 5. Full-Scale Output Voltage vs. V_{REF}



MIXED SIGNAL PRODUCTS

TQ6124

Operating Notes (continued)

Power Supplies

Optimized performance depends on clean supplies. Utilize very low impedance negative supplies that are decoupled over a wide frequency range. The analog and digital grounds should be isolated at the chip, connecting to a single point ground on the circuit board.

ECL Reference

The single-ended data inputs switch against an internal reference of -1.3V (nominal). Variations among input

buffers, or in V_{TT} , may benefit from adjustments in the reference. The ECL reference pin may be driven externally. Its equivalent load is 400 ohms to -1.3V (nominal).

Trim Adjustments

The external trim adjustments for the midrange bits and the LSBs is optional. Trimming is performed by monitoring the attribute of greatest concern (INL, DNL, Spurious levels) while minimizing the unwanted effects. Trim inputs should be left open if not used.

Signals

Figure 6. TQ6124 Pinout

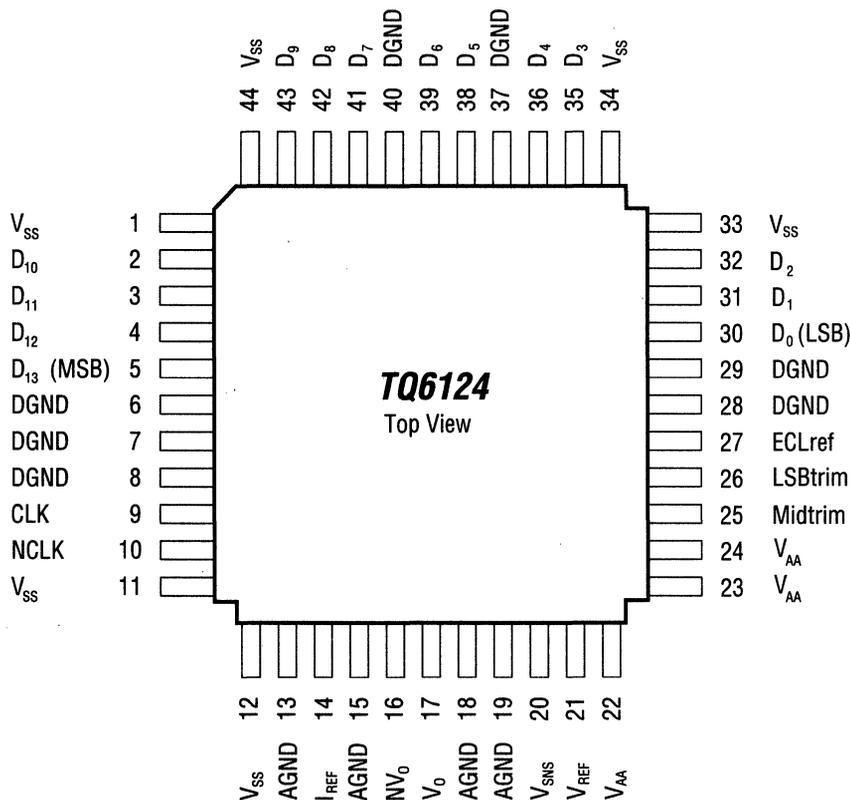


Table 5. Signal-Pin Descriptions

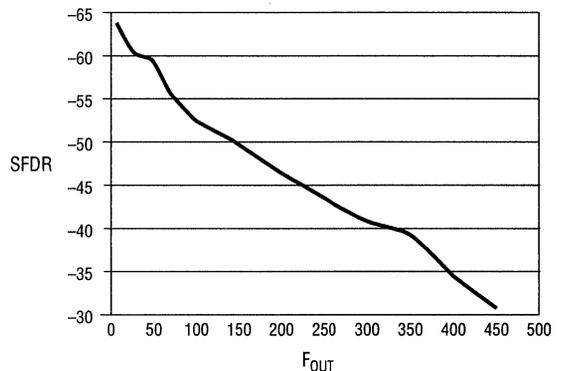
Signal	Pin(s)	Description
DGND	6, 7, 8, 28, 29, 37, 40	Ground connection for digital circuitry.
AGND	13, 15, 18, 19	Ground connection for analog circuitry.
D ₀ thru D ₁₃	30, 31, 32, 35, 36, 38, 39, 41, 42, 43, 2, 3, 4, 5	Data inputs. D ₀ is the least significant bit. ECL levels.
V _O , NV _O	17, 16	True and complementary analog outputs.
CLK, NCLK	9, 10	True and complementary clock inputs. ECL levels.
I _{REF}	14	Connect to AGND. Source of dummy currents in the switch array.
V _{SENSE}	20	Sense Output.
V _{REF}	21	Reference Input.
V _{SS}	1, 11, 12, 33, 34, 44	Digital negative power supply.
V _{AA}	22, 23, 24	Analog negative power supply.
Mid_trim	25	Trim terminal for mid range bits.
LSB_trim	26	Trim terminal for LSB range bits.
ECLref	27	Optional ECL reference level adjustment. Thevinin equivalent is 1.3V nominally into 400 ohms. Equivalent voltage tracks with digital supply.

Typical Performance Data

The graph in Figure 7 shows representative performance data of spurious free dynamic range (SFDR) vs. output frequency performance measured from TQ6124 devices.

Data was collected at room temperature; note, however, that SFDR is not strongly dependent on temperature. Optimum performance is obtained by utilizing as high a clock rate as practical.

Figure 7. SFDR vs. Output Frequency

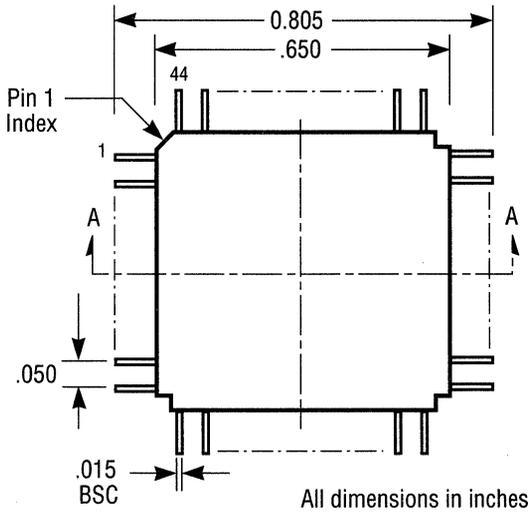


TQ6124

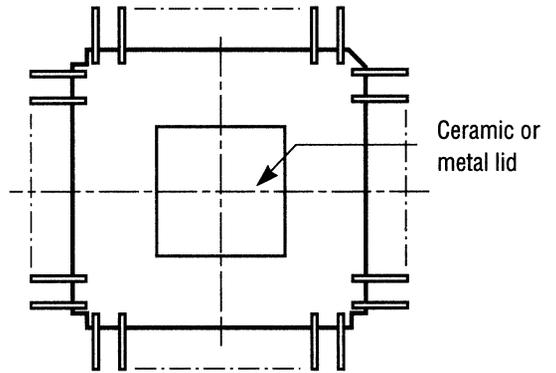
Packaging

Figure 8. 44-pin QFP Package Dimensions

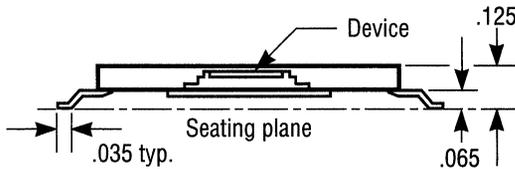
Top View



Bottom View



Section A-A



Ordering Information

TQ6124-CM	<i>1 GS/s 14-bit DAC in 44-pin ceramic QFP</i>
TQ6124-CD	<i>1 GS/s 14-bit DAC — die only</i>
ETF6124	<i>Engineering Test Fixture with TQ6124 device</i>

Additional Information

For latest specifications, additional product information,
worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com **Tel:** (503) 615-9000
Email: sales@tqs.com **Fax:** (503) 615-8900

For technical questions and additional information on specific applications:

Email: applications@tqs.com

The information provided herein is believed to be reliable; TriQuint assumes no liability for inaccuracies or omissions. TriQuint assumes no responsibility for the use of this information, and all such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. TriQuint does not authorize or warrant any TriQuint product for use in life-support devices and/or systems.

Copyright © 1997 TriQuint Semiconductor, Inc. All rights reserved.

Revision 1.0.A October 1997

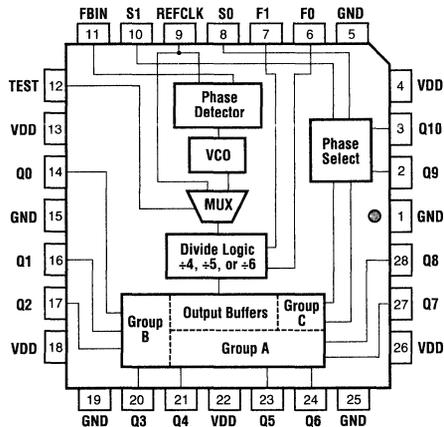
Section 6 — System Timing Products

GA1085	<i>11-Output Configurable Clock Buffer</i>	6-3
GA1086	<i>111-Output Configurable Clock Buffer</i>	6-13
GA1087	<i>11-Output Configurable Clock Buffer</i>	6-25
GA1088	<i>11-Output Configurable Clock Buffer</i>	6-35
GA1110E	<i>Multi-Phase Clock Buffer</i>	6-45
GA1210E	<i>Clock Doubler / Two-Phase Generator</i>	6-59
TQ1089	<i>11-Output Configurable Clock Buffer</i>	6-71
TQ1090	<i>11-Output Configurable Clock Buffer</i>	6-81
TQ2059	<i>High-Frequency Clock Generator</i>	6-91
TQ2060	<i>High-Frequency Clock Generator</i>	6-97
TQ2061	<i>High-Frequency Clock Generator</i>	6-103

TQS



Figure 1. Block Diagram



TriQuint's GA1085 is a configurable clock buffer which generates 11 outputs and operates over a wide range of frequencies—from 24 MHz to 105 MHz. The outputs are available at either 1x and 2x or at 1x and $1/2$ x the reference clock frequency, f_{REF} . When one of the Group A outputs (Q4–Q8) is used as feedback to the PLL, all Group A outputs will be at f_{REF} , and all Group B (Q0–Q3) and Group C (Q9, Q10) outputs will be at $1/2 \times f_{REF}$. When one of the Group B outputs is used as feedback to the PLL, all Group A outputs will be at $2 \times f_{REF}$ and all Group B and Group C outputs will be at f_{REF} . The Shift Select pins select the phase shift ($-2t$, $-t$, $+t$ or $+2t$) for Group C outputs (Q9, Q10) with respect to REFCLK. The phase shift increment (t) is equivalent to the VCO's period ($1/f_{VCO}$).

A very stable internal Phase-Locked Loop (PLL) provides low-jitter operation. This completely self-contained PLL requires no external capacitors or resistors. The PLL's Voltage-Controlled Oscillator (VCO) has a frequency range from 280 MHz to 420 MHz. By feeding back one of the output clocks to FBIN, the PLL continuously maintains frequency and phase synchronization between the reference clock (REFCLK) and each of the outputs.

TriQuint's patented output buffer design delivers a very low output-to-output skew of 150 ps (max). The GA1085's symmetrical TTL outputs are capable of sourcing and sinking 30 mA.

GA1085

11-Output Configurable Clock Buffer

Features

- Wide frequency range:
24 MHz to 105 MHz
- Output configurations:
Four outputs at f_{REF}
Four outputs at $f_{REF}/2$
Two outputs at $f_{REF}/2$
with adjustable phase
or
Five outputs at $2 \times f_{REF}$
Three outputs at f_{REF}
Two outputs at f_{REF}
with adjustable phase
- Selectable Phase Shift: $-2t$, $-t$,
 $+t$, and $+2t$ ($t = 1/f_{VCO}$)
- Low output-to-output skew: 150
ps (max) within a group
- Near-zero propagation delay:
 $-350 \text{ ps} \pm 1000 \text{ ps}$ (max)
- TTL-compatible with 30 mA
output drive
- 28-pin J-lead surface-mount
package

Functional Description

The core of the GA1085 is a Phase-Locked Loop (PLL) that continuously compares the reference clock (REFCLK) to the feedback clock (FBIN), maintaining a zero frequency difference between the two. Since one of the outputs (Q0–Q8) is always connected to FBIN, the PLL keeps the propagation delay between the outputs and the reference clock within $-350 \text{ ps} \pm 1000 \text{ ps}$.

The internal Voltage-Controlled Oscillator (VCO) has an operating range of 280 MHz to 420 MHz. The combination of the VCO and the Divide Logic enables the GA1085 to operate between 24 MHz and 105 MHz. The device features six divide modes: +4, +5, +6, +8, +10, and +12. The Frequency Select pins, F0 and F1, and the output used as feedback to FBIN set the divide mode as shown in Table 1.

The Shift Select pins, S0 and S1, control the phase shift of Q9 and Q10 relative to the other outputs. The user can select from four incremental phase shifts as shown in Table 2.

Table 1. Frequency Mode Selection

Feedback: Any Group A Output (Q4 – Q8)

Test	Select Pins		Mode	Reference Clock Frequency Range	Output Frequency Range	
	F0	F1			Group A: Q4–Q8	B: Q0–Q3, C: Q9–10
0	1	0	+ 4	70 MHz – 105 MHz	70 MHz – 105 MHz	35 MHz – 52 MHz
0	0	0	+ 5	56 MHz – 84 MHz	56 MHz – 84 MHz ¹	28 MHz – 42 MHz
0	0	1	+ 6	48 MHz – 70 MHz	48 MHz – 70 MHz	24 MHz – 35 MHz
0	1	1	Not Used	N.A.	N.A.	N.A.

Feedback: Any Group B Output (Q0 – Q3)

Test	Select Pins		Mode	Reference Clock Frequency Range	Output Frequency Range	
	F0	F1			Group A: Q4–Q8	B: Q0–Q3, C: Q9–Q10
0	1	0	+ 8	35 MHz – 52 MHz	70 MHz – 105 MHz	35 MHz – 52 MHz
0	0	0	+ 10	28 MHz – 42 MHz	56 MHz – 84 MHz ¹	28 MHz – 42 MHz
0	0	1	+ 12	24 MHz – 35 MHz	48 MHz – 70 MHz	24 MHz – 35 MHz
0	1	1	Not Used	N.A.	N.A.	N.A.

Note: 1. This mode produces outputs with 40/60 duty cycle for Q4 – Q8 only.

The phase-shift increment (t) is calculated using the following equation:

$$t = \frac{1}{(f_{\text{REF}})(n)}$$

where n is the divide mode.

In the test mode, the PLL is bypassed and REFCLK is connected directly to the Divide Logic block via the MUX, as shown in Figure 1. This mode is useful for debug and test purposes. The various test modes are outlined in Table 3. In the test mode, the frequency of the reference clock is divided by 4, 5, or 6.

The maximum rise and fall time at the output pins is 1.4 ns. All outputs of the GA1085 are TTL-compatible with 30 mA symmetric drive and a minimum V_{OH} of 2.4 V.

Power-Up/Reset Synchronization

After power-up or reset, the PLL requires time before it achieves synchronization lock. The maximum time required for synchronization (TSYNC) is 500 ms.

Table 2. Phase Shift Selection

S0	S1	Phase Difference (Q9, Q10)
0	0	+2t
0	1	+t
1	0	-t
1	1	-2t

Table 3. Test Mode Selection

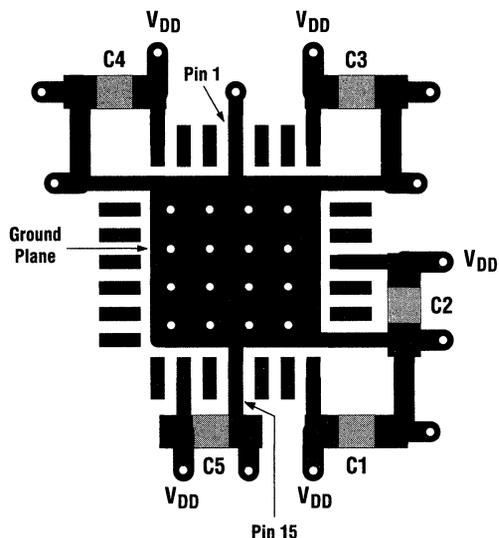
Test	F0	F1	Mode	Ref. Clock	Group A: Outputs Q4–Q8	Groups B, C: Q0–Q3, Q9, Q10
1	1	0	÷ 4	f_{REF}	$f_{REF} \div 4$	$f_{REF} \div 8$
1	0	0	÷ 5	f_{REF}	$f_{REF} \div 5$	$f_{REF} \div 10$
1	0	1	÷ 6	f_{REF}	$f_{REF} \div 6$	$f_{REF} \div 12$
1	1	1	—	—	—	—

Layout Guidelines

Multiple ground and power pins on the GA1085 reduce ground bounce. Good layout techniques, however, are necessary to guarantee proper operation and to meet the specifications across the full operating range. TriQuint recommends bypassing each of the V_{DD} supply pins to the nearest ground pin, as close to the chip as possible.

Figure 2 shows the recommended power layout for the GA1085. The bypass capacitors should be located on the same side of the board as the GA1085. The V_{DD} traces connect to an inner-layer V_{DD} plane. All of the ground pins (GND) are connected to a small ground plane on the surface beneath the chip. Multiple through-holes connect this small surface plane to an inner-layer ground plane. The capacitors (C1–C5) are 0.1 μF . TriQuint's test board uses X7R temperature-stable capacitors in 1206 SMD cases.

Figure 2. Top Layer Layout of Power Pins
(magnified approximately 3.3x)



GA1085

Absolute Maximum Ratings¹

Storage temperature	-65 °C to +150 °C
Ambient temperature with power applied²	-55 °C to +100 °C
Supply voltage to ground potential	-0.5 V to +7.0 V
DC input voltage	-0.5 V to (V _{DD} + 0.5) V
DC input current	-30 mA to +5 mA
Package thermal resistance (MQuad)	$\theta_{JA} = 45 \text{ }^{\circ}\text{C/W}$
Die junction temperature	T _J = 150 °C

DC Characteristics (V_{DD} = +5 V ± 5%, T_A = 0 °C to +70 °C)

Symbol	Description	Test Conditions	Min ³	Typ	Max ³	Unit
V _{OHT}	Output HIGH voltage	V _{DD} = Min I _{OH} = -30 mA V _{IN} = V _{IH} or V _{IL}	2.4	3.4		V
V _{OHC}	Output HIGH voltage	V _{DD} = Min I _{OH} = -1 mA V _{IN} = V _{IH} or V _{IL}	3.2	4.1		V
V _{OL}	Output LOW voltage	V _{DD} = Min I _{OL} = 30 mA V _{IN} = V _{IH} or V _{IL}		0.27	0.5	V
V _{IH} ⁴	Input HIGH level	Guaranteed input logical HIGH voltage for all Inputs	2.0			V
V _{IL} ⁴	Input LOW level	Guaranteed input logical LOW voltage for all inputs			0.8	V
I _{IL}	Input LOW current	V _{DD} = Max V _{IN} = 0.40 V		-156	-400	μA
I _{IH}	Input HIGH current	V _{DD} = Max V _{IN} = 2.7 V		0	25	μA
I _I	Input HIGH current	V _{DD} = Max V _{IN} = 5.5 V		2	1000	μA
I _{DD5} ⁵	Power supply current	V _{DD} = Max		119	160	mA
V _I	Input clamp voltage	V _{DD} = Min I _{IN} = -18 mA		-0.70	-1.2	V

Capacitance

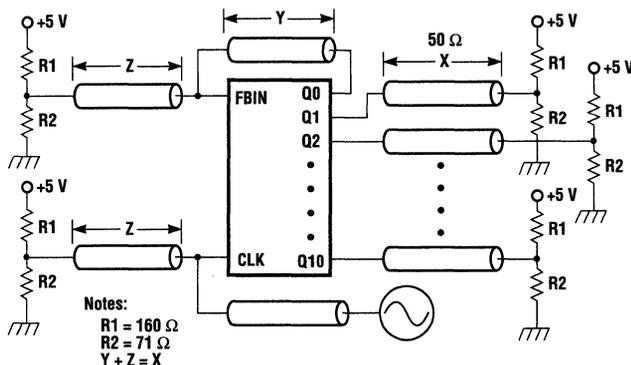
Symbol	Description	Test Conditions	Min	Typ	Max	Unit
C _{IN} ⁶	Input capacitance	V _{IN} = 2.0 V at f = 1 MHz		6		pF

- Notes:
1. Exceeding these parameters may damage the device.
 2. Maximum ambient temperature with device not switching and unloaded.
 3. Typical limits are at V_{DD} = 5.0 V and T_A = 25 °C.
 4. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
 5. This parameter is measured with device not switching and unloaded.
 6. These parameters are not 100% tested, but are periodically sampled.

AC Characteristics ($V_{DD} = +5\text{ V} \pm 5\%$, $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$)

Symbol	Input Clock (REFCLK)	Test Conditions (Figure 3) ¹	Min	Typ	Max	Unit
t_{CPWH}	CLK pulse width HIGH	Figure 4	3	---	---	ns
t_{CPWL}	CLK pulse width LOW	Figure 4	3	---	---	ns
t_{IR}	Input rise time (0.8 V – 2.0 V)		---	---	2.0	ns
Output Clocks (Q0–Q10)						
t_{OR} , t_{OF}	Rise/fall time (0.8 V–2.0 V)	Figure 4	350	---	1400	ps
t_{PD}^2	CLK \uparrow to FBIN \uparrow (GA1085-MC1000)	Figure 4	-1350	-350	+650	ps
t_{SKEW1}^3	Rise–rise, fall–fall (within group)	Figure 5	---	60	150	ps
t_{SKEW2}^3	Rise–rise, fall–fall (group-to-group, aligned)	Figure 6 (skew2 takes into account skew1)	---	75	350	ps
t_{SKEW3}^3	Rise–rise, fall–fall (group-to-group, non-aligned)	Figure 7 (skew3 takes into account skew1, skew2)	---	---	650	ps
t_{SKEW4}^3	Rise–fall, fall–rise (skew4 takes into account skew3)	Figure 8	---	---	1200	ps
t_{CYC}^4	Duty-cycle Variation	Figure 4	-1000	0	+1000	ps
t_{JP}^5	Period-to-Period Jitter	Figure 4	---	80	200	ps
t_{JR}^5	Random Jitter	Figure 4	---	190	400	ps
t_{SYNC}^6	Synchronization Time		---	10	500	μs

- Notes:
1. All measurements are tested with a REFCLK having a rise time of 0.5 ns (0.8 V to 2.0 V).
 2. The PLL maintains alignment of CLK and FBIN at all times. This specification applies to the rising edge only because the input duty cycle can vary while the output duty cycle is typically 50/50. The delay t_{PD} is measured at the 1.5 V level between CLK and FBIN.
 3. Skew specifies the width of the window in which outputs switch, and is measured at 1.5 V.
 4. This specification represents the deviation from 50/50 on the outputs.
 5. Jitter specifications refer to peak-to-peak value. t_{JR} is the jitter on the output with respect to the reference clock. t_{JP} is the jitter on the output with respect to the output's previous rising edge.
 6. t_{SYNC} is the time required for the PLL to synchronize; this assumes the presence of a CLK signal and a connection from one of the outputs to FBIN.

Figure 3. AC Test Circuit


Switching Waveforms

Figure 3. General Timing

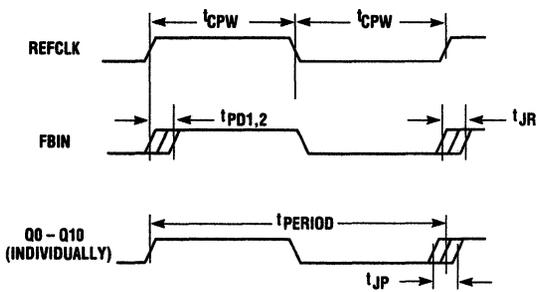


Figure 4. t_{SKEW1}

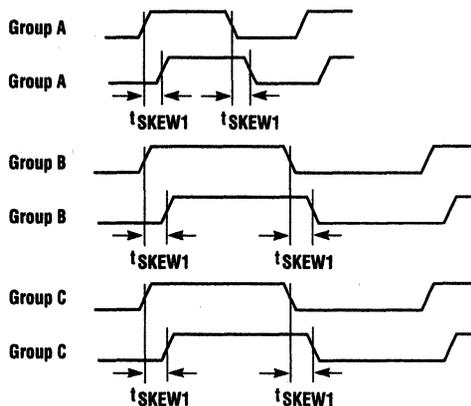


Figure 5. t_{SKEW2}

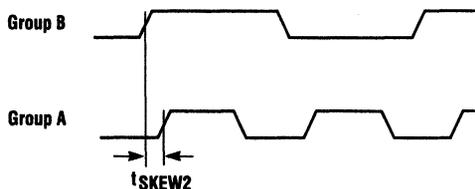
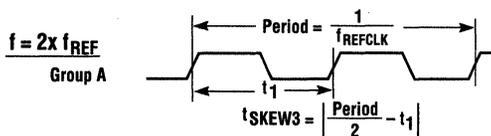
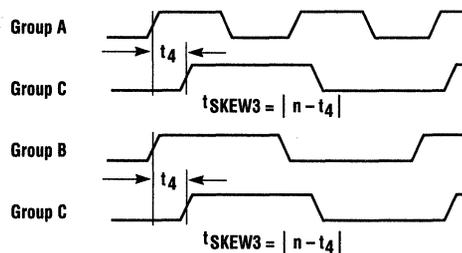


Figure 6. t_{SKEW3}

(For Group B Feedback)

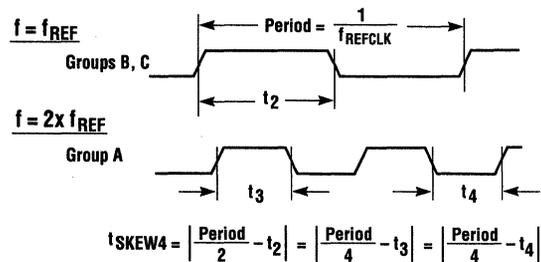


(For Group A or B Feedback)



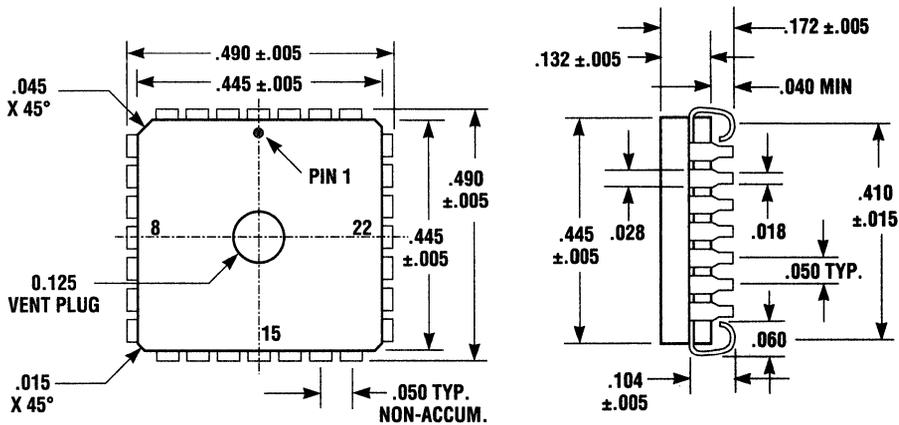
Note: "n" is the phase-shift increment: 2t, t, -t, -2t.

Figure 7. t_{SKEW4}



28-Pin MQuad J-Leaded Package Mechanical Specification

(All dimensions are in inches)



28-Pin MQuad Pin Description

Pin #	Pin Name	Description	I/O
1	GND	Ground	—
2	Q9	Output Clock 9 (C1)	O
3	Q10	Output Clock 10 (C2)	O
4	VDD	+5 V	—
5	GND	Ground	—
6	F0	Frequency Select 0	I
7	F1	Frequency Select 1	I
8	S0	Shift Select 0	I
9	REFCLK	Reference Clock	I
10	S1	Shift Select 1	I
11	FBIN	Feedback In	I
12	TEST	Test	I
13	VDD	+5 V	—
14	Q0	Output Clock 0 (B1)	O

Pin #	Pin Name	Description	I/O
15	GND	Ground	—
16	Q1	Output Clock 1 (B2)	O
17	Q2	Output Clock 2 (B3)	O
18	VDD	+5 V	—
19	GND	Ground	—
20	Q3	Output Clock 3 (B4)	O
21	Q4	Output Clock 4 (A1)	O
22	VDD	+5 V	—
23	Q5	Output Clock 5 (A2)	O
24	Q6	Output Clock 6 (A3)	O
25	GND	Ground	—
26	VDD	+5 V	—
27	Q7	Output Clock 7 (A4)	O
28	Q8	Output Clock 8 (A5)	O

Output Characteristics

The IV characteristics, transition times, package characteristics, device and bond-wire characteristics for the GA1085 are described in Tables 4 through 9 and Figures 9 through 11.

Figure 9. I_{OH} vs. V_{OH}

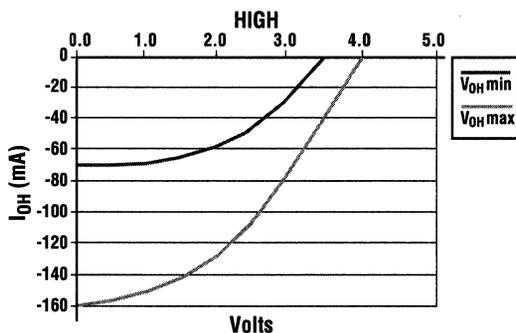


Table 4. I_{OH} vs. V_{OH}

V_{OH}	$I_{OH} \text{ min (mA)}$	$I_{OH} \text{ max (mA)}$
0.0	-70	-160
0.5	-70	-157
1.0	-68	-152
1.5	-65	-142
2.0	-59	-130
2.5	-48	-106
3.0	-29	-79
3.5	0	-42
4.0	0	0
4.5	0	0
5.0	0	0
6.0	0	0
7.0	0	0
8.0	0	0
9.0	0	1
10.0	0	5

These output characteristics are provided for modelling purposes only. TriQuint does not guarantee the information in these tables and figures.

Figure 10. I_{OL} vs. V_{OL}

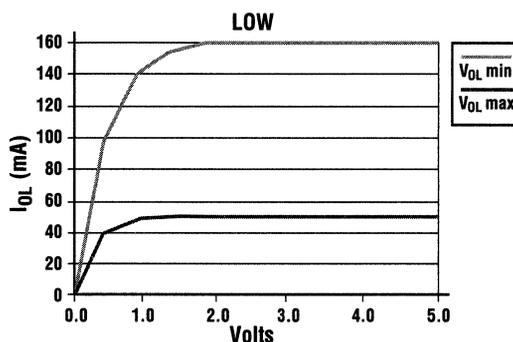


Table 5. I_{OL} vs. V_{OL}

V_{OL}	$I_{OL} \text{ min (mA)}$	$I_{OL} \text{ max (mA)}$
-2.5	-145	-435
-2.0	-135	-410
-1.5	-115	-350
-1.0	-90	-265
-0.5	-40	-120
0.0	0	0
0.5	37	97
1.0	49	140
1.5	53	155
2.0	54	157
2.5	54	159
3.0	54	160
3.5	54	160
4.0	54	160
4.5	54	160
5.0	54	160
10.0	54	160

Notes: 1. These are worst-case corners for process, voltage, and temperature.
2. Includes diode to ground current.

Table 6. Characteristics Above V_{DD} and Below Ground

Diode to GND V	I (mA)	Diode Stack to VDD V	I (mA)
0.0	0	5.0	0
-0.4	0	6.0	0
-0.5	0	7.0	0
-0.6	-5	8.0	0
-0.7	-15	9.0	0
-0.8	-35	10.0	1
-0.9	-55	11.0	5
-1.0	-75	12.0	9
-2.0	-300		
-2.5	-350		
-3.0	-360		

Note: TriQuint does not guarantee diode operation for purposes other than ESD protection.

Figure 11. Output Model

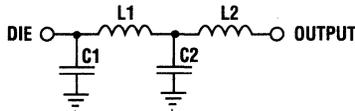


Table 7. Device and Bond-Wire Characteristics (Estimates)

L1	C1
2 nH	10 pF

Table 8. 28-Pin MQuad Package Characteristics

L2	C2
1.85 nH	0.40 pF

Table 9. Rise and Fall Times (Into 0 pF, 50 Ohms to 1.5 V)

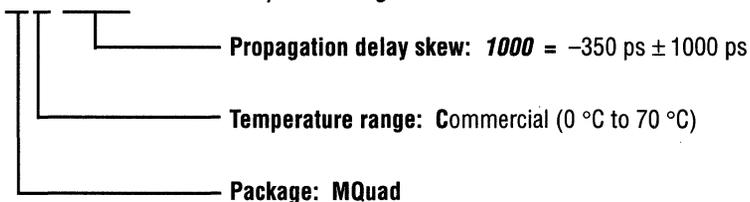
Time (ns)	T_R min (V)	T_R max (V)	T_F min (V)	T_F max (V)
0.0	0.15	0.32	3.20	3.04
0.1	0.15	0.32	3.20	3.04
0.2	0.16	0.32	3.06	2.95
0.3	0.18	0.32	2.86	2.90
0.4	0.23	0.32	2.62	2.68
0.5	0.26	0.32	2.38	2.50
0.6	0.34	0.32	2.17	2.36
0.7	0.46	0.34	2.00	2.22
0.8	0.67	0.39	1.85	2.09
0.9	0.89	0.49	1.69	1.95
1.0	1.12	0.63	1.52	1.86
1.1	1.32	0.86	1.38	1.68
1.2	1.50	1.09	1.26	1.59
1.3	1.73	1.27	1.12	1.49
1.4	1.93	1.45	0.96	1.36
1.5	2.15	1.64	0.83	1.23
1.6	2.75	2.23	0.52	0.95
1.7	2.58	2.00	0.61	1.00
1.8	2.75	2.23	0.52	0.95
1.9	2.90	2.41	0.45	0.91
2.0	3.02	2.50	0.39	0.86
2.1	3.12	2.64	0.33	0.77
2.2	3.17	2.77	0.29	0.73
2.3	3.19	2.86	0.24	0.68
2.4	3.20	2.95	0.21	0.64
2.5	3.20	2.99	0.19	0.59
2.6	3.20	3.02	0.17	0.55
2.7	3.20	3.02	0.16	0.53
2.8	3.20	3.04	0.16	0.50
2.9	3.20	3.04	0.15	0.45
3.0	3.20	3.04	0.15	0.41
3.1	3.20	3.04	0.15	0.40
3.2	3.20	3.04	0.15	0.37
3.3	3.20	3.04	0.15	0.36
3.4	3.20	3.04	0.15	0.32
3.5	3.20	3.04	0.15	0.32

SYSTEM TIMING PRODUCTS

Ordering Information

To order, please specify as shown below:

GA1085-MC nnnn *11-Output Configurable Clock Buffer*



For latest specifications, additional product information,
worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com Tel: (503) 615-9000
Email: sales@tqs.com Fax: (503) 615-8900

For technical questions and additional information on specific applications:

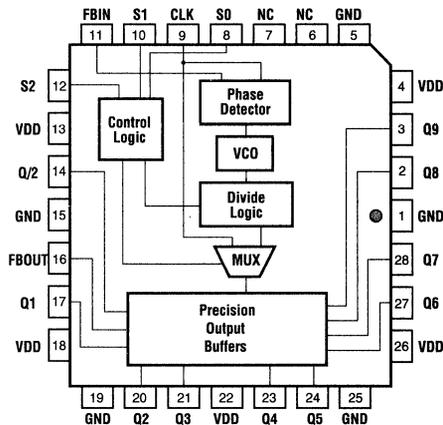
Email: applications@tqs.com

The information provided herein is believed to be reliable; TriQuint assumes no liability for inaccuracies or omissions. TriQuint assumes no responsibility for the use of this information, and all such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. TriQuint does not authorize or warrant any TriQuint product for use in life-support devices and/or systems.

Copyright © 1997 TriQuint Semiconductor, Inc. All rights reserved.

Revision 1.0.A October 1997

Figure 1. Block Diagram



TriQuint's GA1086 operates from 30 MHz to 67 MHz. This TTL-level clock buffer chip supports the tight timing requirements of high-performance microprocessors, with near zero input-to-output delay and very low pin-to-pin skew. The device offers 10 usable outputs synchronized in phase and frequency to a periodic clock input signal. One of the ten outputs is a one-half clock output ($CLK + \div 2$). With split termination, the GA1086 can be used to drive up to nineteen 15 pF loads, as shown in Figure 10.

The tight control over phase and frequency of the output clocks is achieved with a 400 MHz internal Phase-Locked Loop (PLL). By feeding back one of the output clocks to FBIN, the on-chip PLL continuously maintains synchronization between the input clock (CLK) and all ten outputs. Any drift or gradual variation in the system clock is matched and tracked at the ten outputs. The GA1086 output buffers are symmetric, each sourcing and sinking up to 30 mA of drive current. For diagnostic purposes, the device has a test mode which is used to test the device and associated logic by single-stepping through the control logic.

The GA1086 is fabricated using TriQuint's One-Up™ gallium arsenide technology to achieve precise timing control and to guarantee 100% TTL compatibility. The output frequency makes this device ideal for clock generation and distribution in a wide range of high-performance microprocessor-based systems. Many other CISC- and RISC-based systems will also benefit from its tight control of skew and delay.

GA1086

11-Output Clock Buffer

Features

- Operates from 30 MHz to 67 MHz
- Pin-to-pin output skew of 250 ps (max)
- Period-to-period jitter: 75 ps (typ)
- Near-zero propagation delay: $-350 \text{ ps} \pm 500 \text{ ps}$ or $-350 \text{ ps} \pm 1000 \text{ ps}$
- 10 symmetric, TTL-compatible outputs with 30 mA drive and rise and fall times of 1.4 ns (max)
- 28-pin J-lead surface-mount package
- Special test mode
- Meets or exceeds Pentium™ processor timing requirements
- Typical applications include low-skew clock distribution for:
 - RISC- or CISC-based systems
 - Multi-processor systems
 - High-speed backplanes

Functional Description

The GA1086 generates 10 outputs (Q1 – Q9 and FBOUT) which have the same frequency and zero phase delay relative to the reference clock input. In addition, there is one output (Q/2) that has $\frac{1}{2}$ the frequency of the reference clock. The GA1086 maintains frequency and zero phase delay using a Phase Detector to compare the output clock with the reference clock input. Phase deviations between the output clock and reference clock are continuously corrected by the PLL. Figure 1 shows a block diagram of the PLL, which consists of a Phase Detector, Voltage Controlled Oscillator (VCO), Divide Logic, Mux and Control Logic.

The Phase Detector monitors the phase difference between FBIN which is connected to FBOUT, and the reference clock (CLK). The Phase Detector adjusts the VCO such that FBIN aligns with CLK. The VCO has an operating range of 360 MHz to 402 MHz. The output clocks (Qn, FBOUT, and Q/2) are generated by dividing the VCO output.

The desired operating frequency determines the proper divide mode. There are 4 divide modes; +12, +10, +8 and +6. In each mode, the GA1086 operates across the frequency range listed in the Divide Mode Selection Table. The operating frequency is equivalent to the VCO frequency divided by the mode number.

Table 1 shows the input clock frequency (CLK), output clock frequency (Qn), $\frac{1}{2}$ output clock frequency (Q/2),

control bit settings, divide mode and VCO range. FBOUT is fed back to FBIN and has the same frequency as the Qn outputs.

The GA1086 has a test mode that allows for single stepping of the clock input for testing purposes. With S2 HIGH, S1 LOW and S0 HIGH, the signal at the CLK input goes directly to the outputs, bypassing the PLL circuitry.

The maximum rise and fall time at the output pins is 1.4 ns. All outputs of the GA1086 are TTL-compatible with 30 mA symmetric drive and a minimum V_{OH} of 2.4 V.

The GA1086-MC500 and GA1086-MC1000 are identical except for the propagation delay specification (see AC Characteristics table).

Breaking the Feedback Loop

There is no requirement that the external feedback connection be a direct hardwire from an output pin to the FBIN pin. As long as the signal at FBIN is derived directly from the FBOUT pin and maintains its frequency, additional delays can be accommodated. The internal phase-locked loop will adjust the output clocks on the GA1086 to ensure zero phase delay between the FBIN and CLK signals.

Note: the signal at FBIN must be continuous, i.e. not a gated or conditional signal.

Table 1. Divide Mode Selection Table

CLK	Qn	Q/2	Control			Divide Mode
			S2	S1	S0	
30 – 33 MHz	30 – 33 MHz	15 – 16.5 MHz	1	1	1	+12
36 – 40 MHz	36 – 40 MHz	18 – 20 MHz	1	1	0	+10
45 – 50 MHz	45 – 50 MHz	22.5 – 25 MHz	1	0	0	+8
60 – 67 MHz	60 – 67 MHz	30 – 33.5 MHz	0	1	1	+6
TSTCLK	TSTCLK	TSTCLK/2	1	0	1	—

Power-Up/Reset Synchronization

The GA1086 utilizes on-chip phase-locked loop (PLL) technology to maintain synchronization between inputs and outputs. Whenever the device is powered up, or the system clock (CLK) is reset, the phase-locked loop requires a synchronization time (t_{SYNC}) before lock is achieved. The maximum time required for synchronization is 500 ms.

Typical Applications

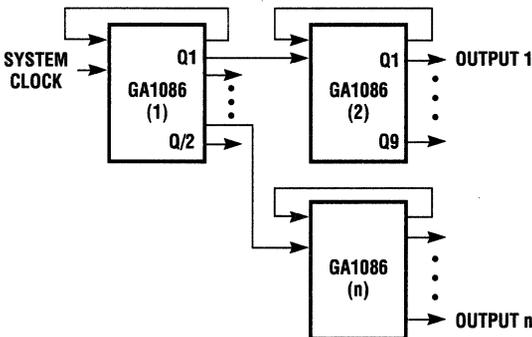
The GA1086 is designed to satisfy a wide range of system clocking requirements. Following are two of the most common clocking bottlenecks which can be solved using the GA1086.

1) Low-Skew Clock Distribution / Clock Trees

The most basic bottleneck to clocking high-performance systems is generating multiple copies of a system clock, while maintaining low skew throughout the system.

- The GA1086 guarantees low skew among all clocks in the system by controlling both the input-to-output delay and the skew among all outputs. In Figure 2, the worst-case skew from Output 1 to Output n, with reference to the system clock, is

Figure 2. Low-Skew Clock Distribution



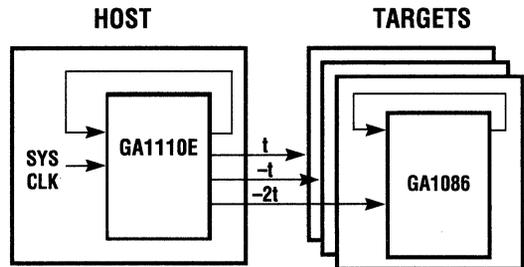
obtained by summing the various skews. The skew between the outputs of the GA1086 (1) which drive the GA1086 (2) and the GA1086 (n) is summed with the propagation delay of the GA1086 (2 or n), the skew between the outputs of the GA1086 (2), and the skew between the outputs of the GA1086 (n). This results in a total skew of 1.75 ns (250 ps + 1000 ps + 250 ps + 250 ps).

2) Board-to-Board Synchronization

Many computing systems today consist of multiple boards designed to run synchronously. The skew associated with routing clocks across a backplane presents a major hurdle to maximizing system performance.

- The edge placement feature of TriQuint's configurable custom clock generator (GA1110E) operating at 33 MHz, coupled with the tightly controlled input/output delay of the GA1086, ensures all boards in the system are running synchronously.

Figure 3. Board-to-Board Synchronization



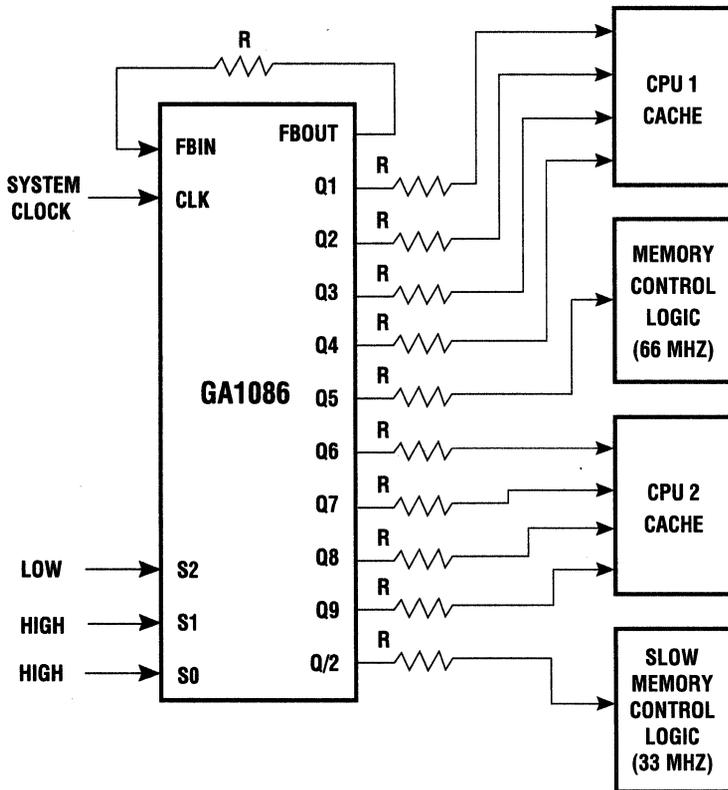
SYSTEM TIMING PRODUCTS

Multi-Processor Systems

The GA1086 can be effectively used to distribute clocks in RISC- or CISC-processor-based systems. Its 10 outputs support both single- and multi-processor systems. Following are three representative configurations which show how the 10 outputs can be used to synchronize the operation of CPU cache and memory banks operating at different speeds.

Figure 4 depicts a 2-CPU system in which the processors and associated peripherals are operating at 66 MHz. Each of the nine outputs operating at 66 MHz are fully utilized to drive the appropriate CPU, cache, and memory control logic. The 33 MHz output is used to synchronize the operation of the slower memory bank to the rest of the system.

Figure 4. Clocking a Dual-CPU System

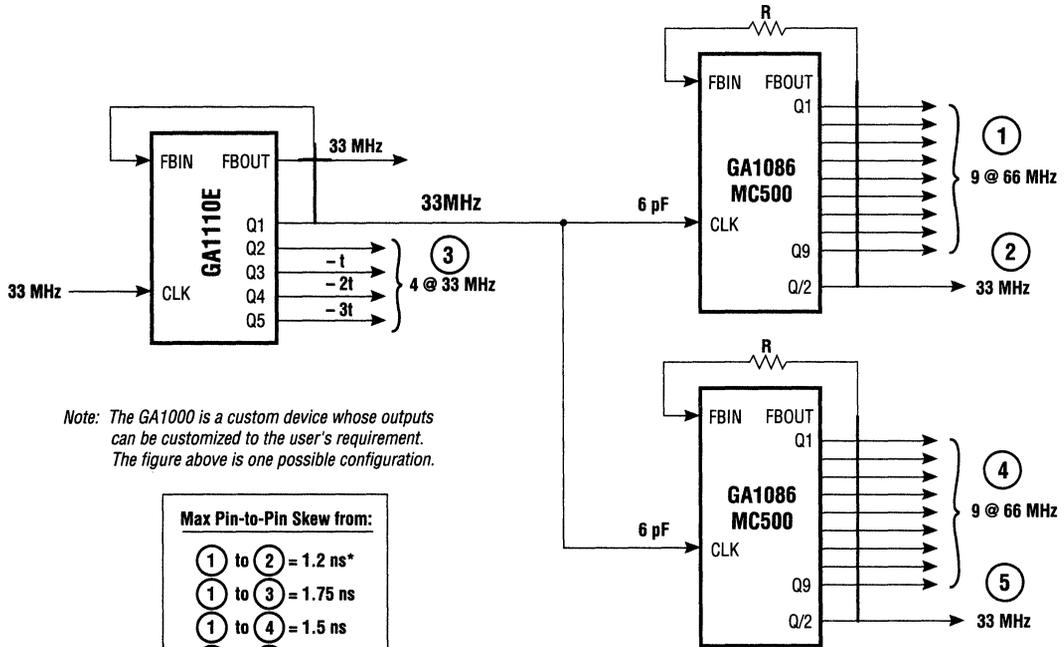


Multi-Processor Systems (cont.)

Figure 5 shows a 4-processor system with various 33 MHz memory banks synchronized to the 66 MHz CPUs. The GA1110E, a custom device whose six outputs can be individually configured, (see GA1110E data sheet), is used as the clock source for

the GA1086 devices. This configuration gives the user 18 copies of the 66 MHz clock and 7 copies of the 33 MHz clock. By using the configurability of the GA1110E, the user can also specify and control the placement of the edges of the outputs of the GA1110E.

Figure 5. Generating Multiple Outputs



Note: The GA1000 is a custom device whose outputs can be customized to the user's requirement. The figure above is one possible configuration.

Max Pin-to-Pin Skew from:	
① to ②	= 1.2 ns*
① to ③	= 1.75 ns
① to ④	= 1.5 ns
② to ③	= 2.7 ns*
② to ⑤	= 3.2 ns*
③ to ④	= 1.75 ns
③ to ⑤	= 2.7 ns*
④ to ⑤	= 1.2 ns*

* Assumes maximum skew between Q9 and Q/2 is 1.2 ns. See AC specifications.

SYSTEM TIMING PRODUCTS

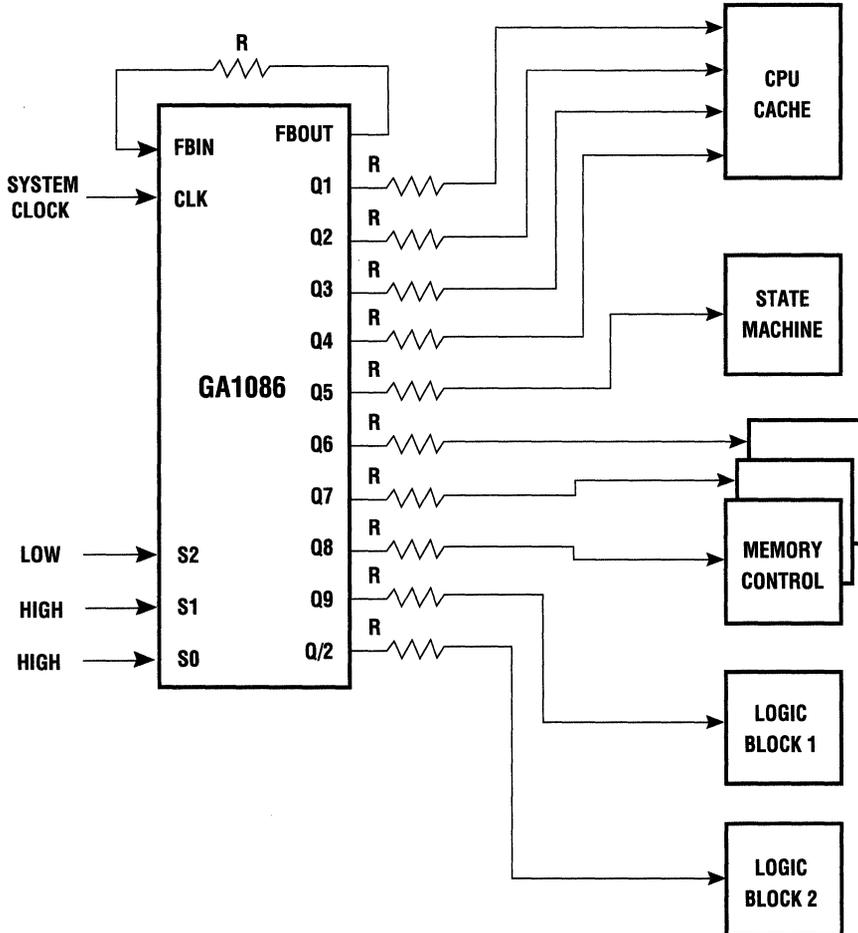
Single-Processor Systems

Figure 6 is an example of a single-CPU system. The nine 66MHz outputs of the GA1086 are used to drive the CPU and its related cache, the state machine, memory banks, and other general-purpose logic.

The table in Figure 5 also specifies the maximum pin-to-pin skew of various sets of outputs from the three clocking devices.

Please note that the GA1086s are series-terminated and that the feedback trace lengths for the two devices should be equal.

Figure 6. Clocking a Single-CPU System



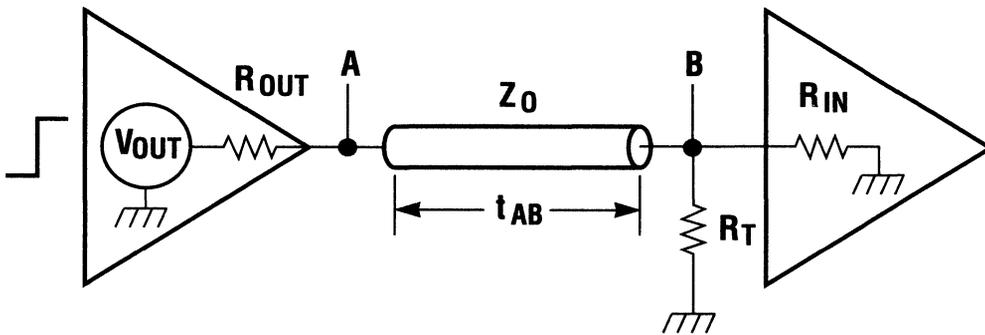
Parallel Termination of Outputs

The GA1086 can be terminated either in parallel or in series. If power dissipation is not of primary concern, then parallel termination can be the most effective mode of termination for the GA1086. An example of this termination is shown in Figure 7, along with the waveforms at an output pin and at the load.

the Thevenin equivalent using two resistors and +5 V supply can replace the 65 ohms to 1.5 V.

Unused outputs must be terminated.

Figure 7. Parallel Termination

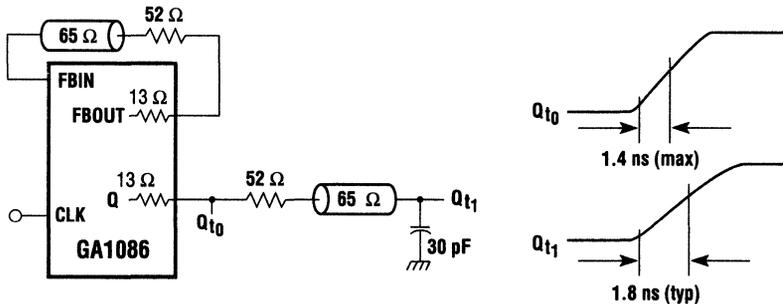


Series Termination of Outputs

The alternative to parallel termination is series termination. For applications where overshoots and undershoots of the clock signal are a concern, it is best

to use balanced termination as shown in Figure 8. This could, however, slow the rise time of the pulses arriving at the destination.

Figure 8. Balanced Termination



SYSTEM TIMING PRODUCTS

If rise times are critical and if overshoots and undershoots can be tolerated, then unbalanced termination may be used. Reflections due to unbalanced termination can cause ringing at the load. The transmission line lengths, therefore, must be long enough to cause the ringing to occur only after the waveform has completely switched to either the LOW or the HIGH state, (the round trip). The propagation time of the output signals should be greater than the switching time for LOW to HIGH or HIGH to LOW.

To double the number of loads (devices) driven by the GA1086, split termination may be used. Examples of three types of series termination and the resulting waveforms, measured between 0.8 V and 2.0 V, are shown in Figures 9 and 10 for one of the outputs. Unused outputs must be terminated.

Figure 9. Unbalanced Termination

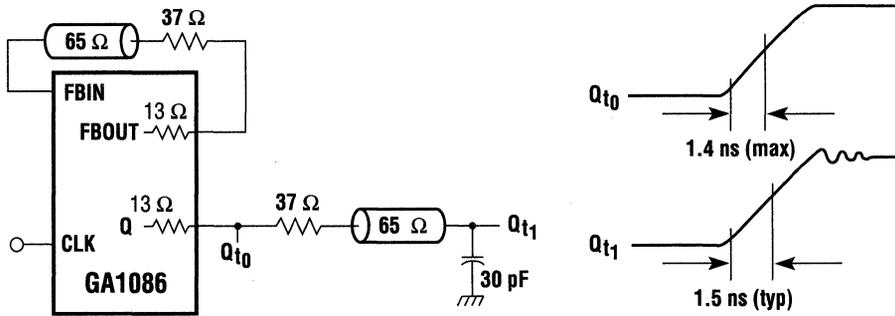
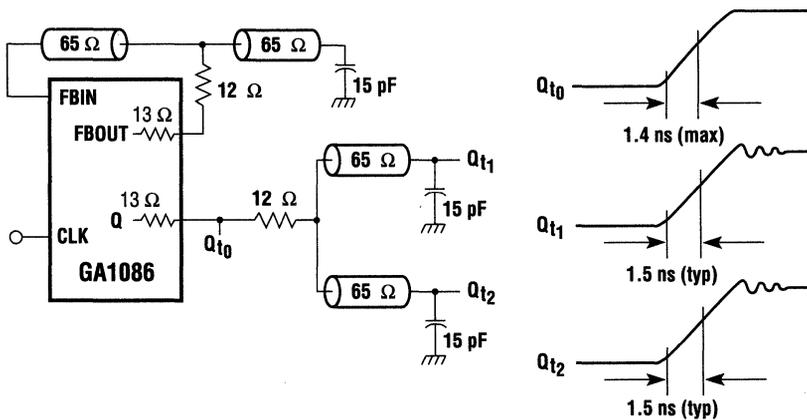


Figure 10. Split Unbalanced Termination



Note: Rise time at Q_{t1} is measured between 0.8 V and 2.0 V.

Absolute Maximum Ratings

Storage temperature	-65 °C to +150 °C
Ambient temperature with power applied	-55 °C to +100 °C
Supply voltage to ground potential	-0.5 V to +7.0 V
DC input voltage	-0.5 V to +(V _{DD} + 0.5)
DC input current	-30 mA to +5 mA

Caution: Damage to the device may occur if an output is shorted to ground or V_{DD}.

DC Characteristics

(Supply voltage: +5 V ± 5% Ambient temp: 0 °C to +70 °C) ¹

Symbol	Description	Test Conditions	Limits ²			Unit
			Min	Typ	Max	
V _{OH}	Output HIGH voltage	V _{DD} = Min I _{OH} = -30 mA V _{IN} = V _{IH} or V _{IL}	2.4	3.6		V
V _{OL}	Output LOW voltage	V _{DD} = Min I _{OL} = 30 mA V _{IN} = V _{IH} or V _{IL}		0.2	0.5	V
V _{IH} ³	Input HIGH level	Guaranteed input logical HIGH voltage for all inputs	2.0			V
V _{IL} ³	Input LOW level	Guaranteed input logical LOW voltage for all inputs			0.8	V
I _{IL}	Input LOW current	V _{DD} = Max V _{IN} = 0.40 V		-166	-400	μA
I _{IH}	Input HIGH current	V _{DD} = Max V _{IN} = 2.7 V		0	25	μA
I _I	Input HIGH current	V _{DD} = Max V _{IN} = 5.5 V		2	1000	μA
I _{DD} ⁴	Power supply current	V _{DD} = Max			115	160 mA
V _I	Input clamp voltage	V _{DD} = Min I _{IN} = -18 mA		-0.62	-1.2	V

Capacitance ^{1,5}

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
C _{IN}		Input capacitance	V _{IN} = 2.0 V at f = 1 MHz		6	pF

Notes: 1. These values apply to both the GA1086-MC500 and GA1086-MC1000.

2. Typical limits are at V_{DD} = 5.0 V and T_A = 25 °C.

3. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.

4. I_{DD} is measured with outputs LOW and unloaded.

5. These parameters are not 100% tested, but are periodically sampled.

AC Specifications

(Supply voltage: +5 V ± 5%, Ambient temp: 0°C to +70°C)

Input Clocks		Min	Typ	Max	Unit
F _{IN}	CLK frequency	30	—	67	MHz
t _{CP}	CLK period	14.9	—	33	ns
t _{CPW}	CLK pulse width	3.0	—	—	ns
t _{IR}	Input rise time (0.8 V – 2.0 V)	—	—	2.0	ns

Output Clocks		Min	Typ	Max	Unit
t _{OR}	Output rise time (0.8 V – 2.0 V)	0.15	—	1.4	ns
t _{OF}	Output fall time (0.8 V – 2.0 V)	0.15	—	1.4	ns
t _{PD1} ¹	CLK \hat{I} to FBIN \hat{I} (MC500)	-850	-350	+150	ps
t _{PD2} ^{1,2}	CLK \hat{I} to FBIN \hat{I} (MC1000)	-1350	-350	+650	ps
t _{SKEW1} ^{2,3}	Q1-Q9 and FBOUT (0.8V)	-125	—	+125	ps
t _{SKEW1} ^{2,3}	Q1-Q9 and FBOUT (1.5V)	-125	—	+125	ps
t _{SKEW1} ^{2,3}	Q1-Q9 and FBOUT (2.0V)	-125	—	+125	ps
t _{SKEW2} ^{2,3}	Q/2 Output skew	—	0.6	1.2	ns
t _W ⁴	Output window	—	100	250	ps
t _{CYC} ⁵	Duty-cycle variation	—	1.0	—	ns
t _{SYNC} ⁶	Synchronization time	—	200	500	μs
t _{JIT} ⁷	Period-to-period jitter	—	75	—	ps

Figure 11. Switching Waveforms
Buffer Configuration (FBIN = FBOUT)

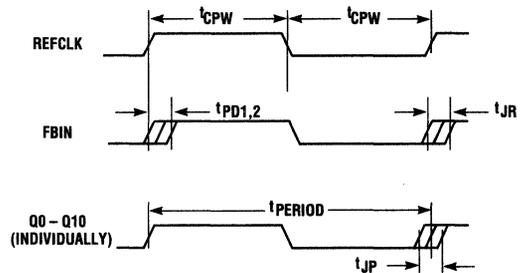
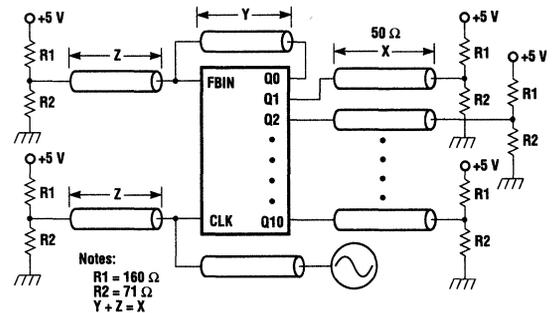


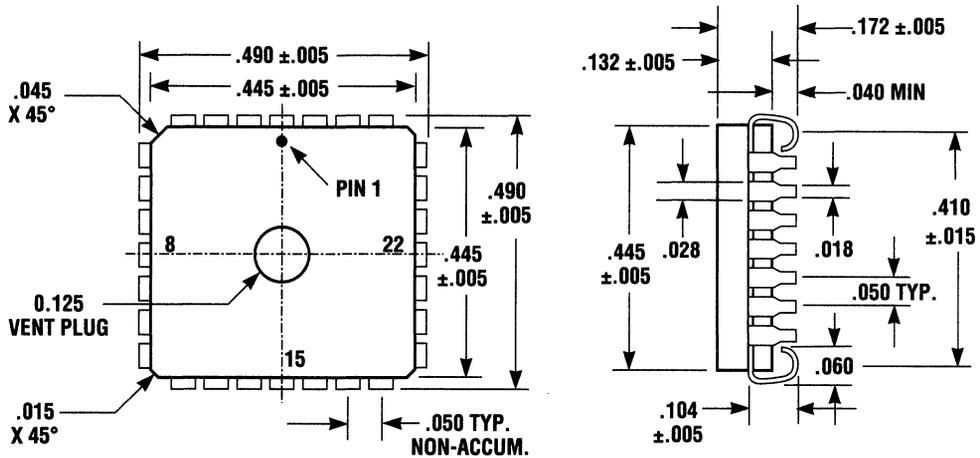
Figure 12. AC Test Circuit



- Notes: 1. The PLL maintains alignment of CLK and FBIN at all times. This specification applies to the rising edge only because the input duty cycle can vary while the output duty cycle is typically 50/50. The delay t_{PD} is measured at the 1.5 V level between CLK and FBIN.
2. t_{PD} and t_{SKEW} are tested with an input clock having a rise time of 0.5 ns (0.8 V to 2.0 V).
3. The output skew is measured from the middle of the output window, t_W. The maximum skew is guaranteed across all voltages and temperatures.
4. t_W specifies the width of the window in which outputs Q1-Q9 switch.
5. This specification represents the deviation from 50/50 on the outputs; it is sampled periodically but is not guaranteed.
6. t_{SYNC} is the time required for the PLL to synchronize; this assumes the presence of a CLK signal and a connection from one of the outputs to FBIN.
7. Jitter is specified as a peak-to-peak value.

28-Pin MQuad J-Leaded Package Mechanical Specification

(All dimensions are in inches)

**28-Pin MQuad Pin Description**

Pin #	Pin Name	Description	I/O
1	GND	Ground	-
2	Q8	Output Clock 8	0
3	Q9	Output Clock 9	0
4	VDD	+5 V	-
5	GND	Ground	-
6	N/C	No Connect	-
7	N/C	No Connect	-
8	S0	Select 0	I
9	CLK	Reference Clock	I
10	S1	Select 1	I
11	FBIN	Feedback In	I
12	S2	Select 2	I
13	VDD	+5 V	-
14	Q/2	Half-Clock Out	0

Pin #	Pin Name	Description	I/O
15	GND	Ground	-
16	FBOUT	Feedback Clock	0
17	Q1	Output Clock 1	0
18	VDD	+5 V	-
19	GND	Ground	-
20	Q2	Output Clock 2	0
21	Q3	Output Clock 3	0
22	VDD	+5 V	-
23	Q4	Output Clock 4	0
24	Q5	Output Clock 5	0
25	GND	Ground	-
26	VDD	+5 V	-
27	Q6	Output Clock 6	0
28	Q7	Output Clock 7	0

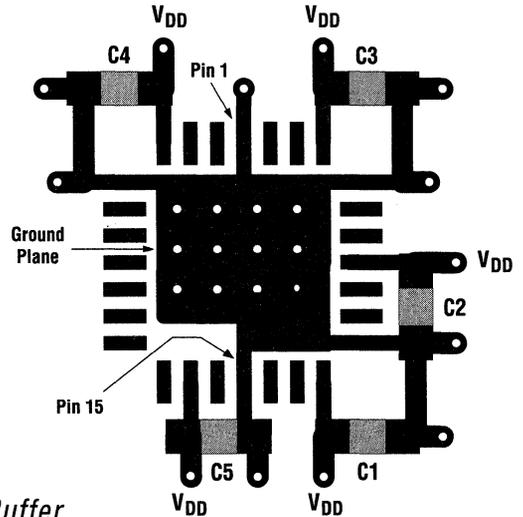
Layout Guidelines

Multiple ground and power pins on the GA1086 reduce ground bounce. Good layout techniques, however, are necessary to guarantee proper operation and to meet the specifications across the full operating range. TriQuint recommends bypassing each of the V_{DD} supply pins to the nearest ground pin, as close to the chip as possible.

Figure 13 shows the recommended power layout for the GA1086. The bypass capacitors should be located on the same side of the board as the GA1086. The V_{DD} traces connect to an inner-layer V_{DD} plane. All of the ground pins (GND) are connected to a small ground plane on the surface beneath the chip. Multiple

through-holes connect this small surface plane to an inner-layer ground plane. The capacitors (C1–C5) are 0.1 mF. TriQuint’s test board uses X7R temperature-stable capacitors in 1206 SMD cases.

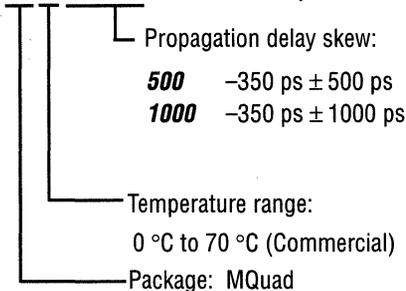
Figure 13. Top Layer Layout of Power Pins
(Approx. 3.3x)



Ordering Information

To order, please specify as shown below:

GA1086-MC n...n 11-Output Clock Buffer



Additional Information

For latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com **Tel:** (503) 615-9000
Email: sales@tqs.com **Fax:** (503) 615-8900

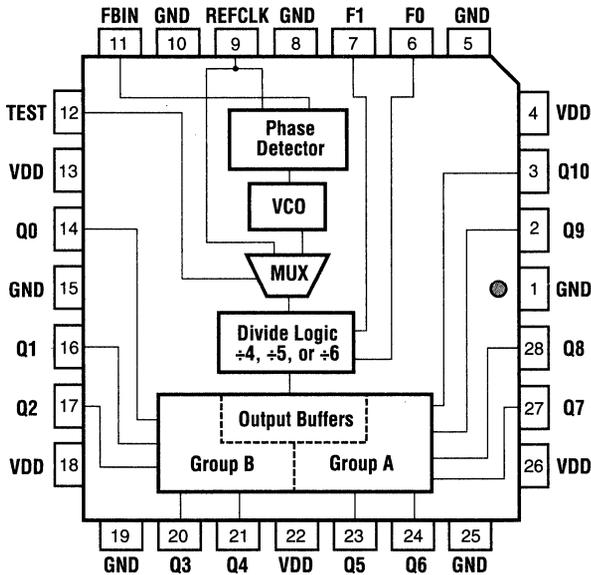
For technical questions and additional information on specific applications:

Email: applications@tqs.com

The information provided herein is believed to be reliable; TriQuint assumes no liability for inaccuracies or omissions. TriQuint assumes no responsibility for the use of this information, and all such information shall be entirely at the user’s own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. TriQuint does not authorize or warrant any TriQuint product for use in life-support devices and/or systems.

Copyright © 1997 TriQuint Semiconductor, Inc. All rights reserved.

Revision 1.0.A October 1997



GA1087

11-Output Configurable Clock Buffer

Features

- Wide frequency range: 24 MHz to 105 MHz
- Output configurations: five outputs at f_{REF} , five outputs at $f_{REF}/2$ or six outputs at $2x f_{REF}$, four outputs at f_{REF}
- Low output-to-output skew: 150 ps (max) within a group
- Near-zero propagation delay: $-350 \text{ ps} \pm 500 \text{ ps (max)}$ or $-350 \text{ ps} \pm 700 \text{ ps (max)}$
- TTL-compatible with 30 mA output drive
- 28-pin J-lead surface-mount package

TriQuint's GA1087 is a configurable clock buffer which generates 11 outputs, operating over a wide range of frequencies — from 24 MHz to 105 MHz. The outputs are available at either 1x and 2x or at 1x and $1/2$ x the reference clock frequency, f_{REF} . When one of the Group A outputs (Q5–Q10) is used as feedback to the PLL, all Group A outputs will be at f_{REF} , and all Group B outputs (Q0–Q4) will be at $1/2 \times f_{REF}$. When one of the Group B outputs is used as feedback to the PLL, all Group A outputs will be at $2x f_{REF}$ and all Group B outputs will be at f_{REF} .

A very stable internal Phase-Locked Loop (PLL) provides low-jitter operation. Completely self-contained, this PLL requires no external capacitors or resistors. The PLL's voltage-controlled oscillator (VCO) has a frequency range from 280 MHz to 420 MHz. By feeding back one of the output clocks to FBIN, the PLL continuously maintains frequency and phase synchronization between the reference clock (REFCLK) and each of the outputs.

TriQuint's patented output buffer design delivers a very low output-to-output skew of 150 ps (max). The GA1087's symmetrical TTL outputs are capable of sourcing and sinking 30 mA.

SYSTEM TIMING PRODUCTS

Functional Description

The core of the GA1087 is a Phase-Locked Loop (PLL) that continuously compares the reference clock (REFCLK) to the feedback clock (FBIN), maintaining a zero frequency difference between the two. Since one of the outputs (Q0–Q8) is always connected to FBIN, the PLL keeps the propagation delay between the outputs and the reference clock within $-350 \text{ ps} \pm 500 \text{ ps}$ for the GA1087-MC500, and within $-350 \text{ ps} \pm 700 \text{ ps}$ for the GA1087-MC700.

The internal voltage-controlled oscillator (VCO) has an operating range of 280 MHz to 420 MHz. The combination of the VCO and the Divide Logic enables the GA1087 to operate between 24 MHz and 105 MHz.

The device features six divide modes: +4, +5, +6, +8, +10, and +12. The Frequency Select pins, F0 and F1,

and the output used as feedback to FBIN set the divide mode as shown in Table 1.

In the test mode, the PLL is bypassed and REFCLK is connected directly to the Divide Logic block via the MUX, as shown in Figure 1. This mode is useful for debug and test purposes. The various test modes are outlined in Table 2. In the test mode, the frequency of the reference clock is divided by 4, 5, or 6.

The maximum rise and fall time at the output pins is 1.4 ns. All outputs of the GA1087 are TTL-compatible with 30 mA symmetric drive and a minimum V_{OH} of 2.4 V.

Power Up/Reset Synchronization

After-power-up or reset, the PLL requires time before it achieves synchronization lock. The maximum time required for synchronization (TSYNC) is 500 ms.

Table 1. Frequency Mode Selection

Feedback: Any Group A Output (Q5 – Q10)

Test	Select Pins		Mode	Reference Clock Frequency Range	Output Frequency Range	
	F0	F1			Group A: Q5–Q10	Group B: Q0–Q4
0	1	0	+4	70 MHz – 105 MHz	70 MHz – 105 MHz	35 MHz – 52 MHz
0	0	0	+5	56 MHz – 84 MHz	56 MHz – 84 MHz ¹	28 MHz – 42 MHz
0	0	1	+6	48 MHz – 70 MHz	48 MHz – 70 MHz	24 MHz – 35 MHz
0	1	1	Not Used	N.A.	N.A.	N.A.

Feedback: Any Group B Output (Q0 – Q4)

Test	Select Pins		Mode	Reference Clock Frequency Range	Output Frequency Range	
	F0	F1			Group A: Q5–Q10	Group B: Q0–Q4
0	1	0	+8	35 MHz – 52 MHz	70 MHz – 105 MHz	35 MHz – 52 MHz
0	0	0	+10	28 MHz – 42 MHz	56 MHz – 84 MHz ¹	28 MHz – 42 MHz
0	0	1	+12	24 MHz – 35 MHz	48 MHz – 70 MHz	24 MHz – 35 MHz
0	1	1	Not Used	N.A.	N.A.	N.A.

Notes: 1. This mode produces outputs with 40/60 duty cycle for Q5 – Q10 only.

Table 2. Test Mode Selection

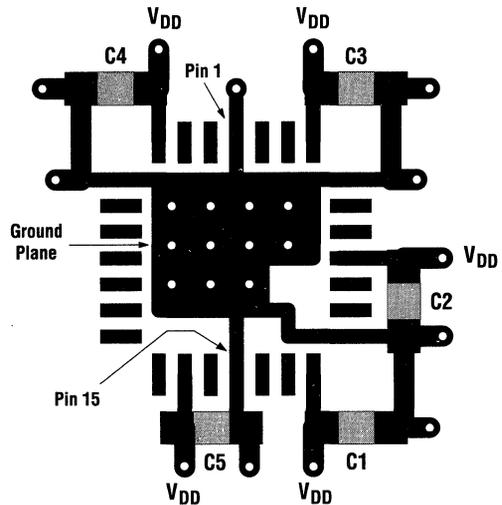
Test	F0	F1	Mode	Ref. Clock	Group B: Outputs Q0–Q4	Group A: Outputs Q5–Q10
1	1	0	+4	f_{REF}	$f_{REF} + 8$	$f_{REF} + 4$
1	0	0	+5	f_{REF}	$f_{REF} + 10$	$f_{REF} + 5$
1	0	1	+6	f_{REF}	$f_{REF} + 12$	$f_{REF} + 6$
1	1	1	—	—	—	—

Layout Guidelines

Multiple ground and power pins on the GA1087 reduce ground bounce. Good layout techniques, however, are necessary to guarantee proper operation and to meet the specifications across the full operating range. TriQuint recommends bypassing each of the V_{DD} supply pins to the nearest ground pin, as close to the chip as possible.

Figure 2 shows the recommended power layout for the GA1087. The bypass capacitors should be located on the same side of the board as the GA1087. The V_{DD} traces connect to an inner-layer V_{DD} plane. All of the ground pins (GND) are connected to a small ground plane on the surface beneath the chip. Multiple through holes connect this small surface plane to an inner-layer ground plane. The capacitors (C1–C5) are 0.1 mF. TriQuint’s test board uses X7R temperature-stable capacitors in 1206 SMD cases.

**Figure 2. Top Layer Layout of Power Pins
(approx. 3.3x)**



GA1087

Absolute Maximum Ratings ¹

Storage temperature	-65 °C to +150 °C
Ambient temperature with power applied ²	-55 °C to +100 °C
Supply voltage to ground potential	-0.5 V to +7.0 V
DC input voltage	-0.5 V to (V _{DD} + 0.5) V
DC input current	-30 mA to +5 mA
Package thermal resistance (MQuad)	θ _{JA} = 45 °C/W
Die junction temperature	T _J = 150 °C

DC Characteristics (V_{DD} = +5 V ± 5%, T_A = 0 °C to +70 °C) ³

Symbol	Description	Test Conditions	Min	Limits ⁴		Units	
				Typ	Max		
V _{OHT}	Output HIGH voltage	V _{DD} = Min V _{IN} = V _{IH} or V _{IL}	I _{OH} = -30 mA	2.4	3.4	V	
V _{OHC}	Output HIGH voltage V _{IN}	V _{DD} = Min = V _{IH} or V _{IL}	I _{OH} = -1 mA	3.2	4.1	V	
V _{OL}	Output LOW voltage V _{IN}	V _{DD} = Min = V _{IH} or V _{IL}	I _{OL} = 30 mA		0.27	0.5	V
V _{IH} ⁵	Input HIGH level Voltage for all Inputs	Guaranteed input logical HIGH	2.0			V	
V _{IL} ⁵	Input LOW level Voltage for all inputs	Guaranteed input logical LOW			0.8	V	
I _{IL}	Input LOW current	V _{DD} = Max V _{IN} = 0.40 V		-156	-400	μA	
I _{IH}	Input HIGH current	V _{DD} = Max V _{IN} = 2.7 V		0	25	μA	
I _I	Input HIGH current	V _{DD} = Max V _{IN} = 5.5 V		2	1000	μA	
I _{DD5} ⁶	Power supply current	V _{DD} = Max		119	160	mA	
V _I	Input clamp voltage	V _{DD} = Min I _{IN} = -18 mA		-0.70	-1.2	V	

Capacitance

Symbol	Description	Test Conditions	Min	Typ	Max	Units
C _{IN} ^{3,7}	Input capacitance	V _{IN} = 2.0 V at f = 1 MHz		6		pF

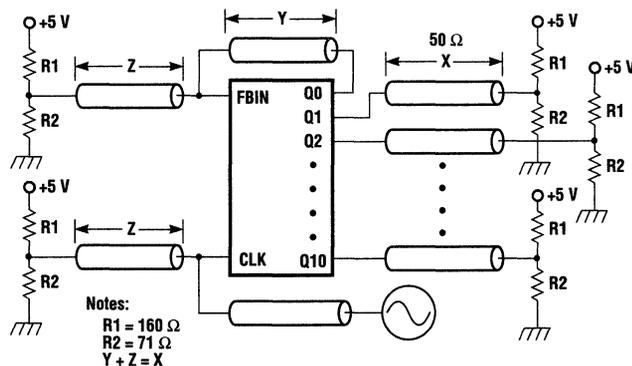
- Notes:
1. Exceeding these parameters may damage the device.
 2. Maximum ambient temperature with device not switching and unloaded.
 3. These values apply to both GA1087-MC500 and GA1087-MC700.
 4. Typical limits are at V_{DD} = 5.0 V and T_A = 25 °C.
 5. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
 6. This parameter is measured with device not switching and unloaded.
 7. These parameters are not 100% tested, but are periodically sampled.

AC Characteristics ($V_{DD} = +5 V \pm 5\%$, $T_A = 0^\circ C$ to $+70^\circ C$)

Symbol	Input Clock (REFCLK)	Test Conditions (Figure 3) ¹	Min	Typ	Max	Unit
t_{CPWH}	CLK pulse width HIGH	Figure 4	3	---	---	ns
t_{CPWL}	CLK pulse width LOW	Figure 4	3	---	---	ns
t_{IR}	Input rise time (0.8 V - 2.0 V)		---	---	2.0	ns

Symbol	Input Clock (Q0-Q10)	Test Conditions (Figure 3) ¹	Min	Typ	Max	Unit
t_{OR}, t_{OF}	Rise/fall time (0.8 V - 2.0 V)	Figure 4	350	---	1400	ps
t_{PD1} ²	CLK \uparrow to FBIN \uparrow (GA1087-MC500)	Figure 4	-850	-350	+150	ps
t_{PD2} ²	CLK \uparrow to FBIN \uparrow (GA1087-MC700)	Figure 4	-1050	-350	+350	ps
t_{SKEW1} ³	Rise-rise, fall-fall (within group)	Figure 5	---	60	150	ps
t_{SKEW2} ³	Rise-rise, fall-fall (group-to-group, aligned)	Figure 6 (skew2 takes into account skew1)	---	75	350	ps
t_{SKEW3} ³	Rise-rise, fall-fall (group-to-group, non-aligned)	Figure 7 (skew3 takes into account skew1, 2)	---	---	650	ps
t_{SKEW4} ³	Rise-fall, fall-rise	Figure 8 (skew4 takes into account skew3)	---	---	1200	ps
t_{CYC} ⁴	Duty-cycle Variation	Figure 4	-1000	0	+1000	ps
t_{JP} ⁵	Period-to-Period Jitter	Figure 4	---	80	200	ps
t_{JR} ⁵	Random Jitter	Figure 4	---	190	400	ps
t_{SYNC} ⁶	Synchronization Time		---	10	500	μ s

- Notes:
1. All measurements are tested with a REFCLK having a rise time of 0.5 ns (0.8 V to 2.0 V).
 2. The PLL maintains alignment of CLK and FBIN at all times. This specification applies to the rising edge only because the input duty cycle can vary while the output duty cycle is typically 50/50. The delay t_{PD} is measured at the 1.5 V level between CLK and FBIN.
 3. Skew specifies the width of the window in which outputs switch, and is measured at 1.5 V.
 4. This specification represents the deviation from 50/50 on the outputs.
 5. Jitter specifications refer to peak-to-peak value. t_{JR} is the jitter on the output with respect to the reference clock. t_{JP} is the jitter on the output with respect to the output's previous rising edge.
 6. t_{SYNC} is the time required for the PLL to synchronize; this assumes the presence of a CLK signal and a connection from one of the outputs to FBIN.

Figure 3. AC Test Circuit

Switching Waveforms

Figure 4. General Timing

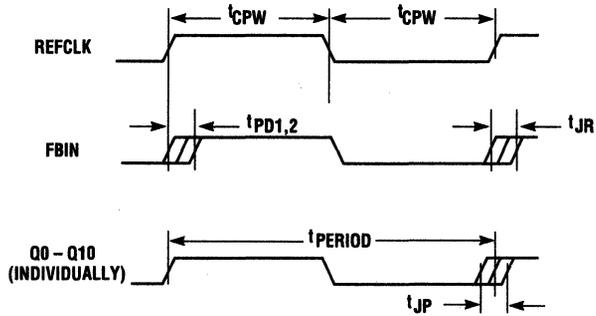


Figure 5. t_{SKEW1}

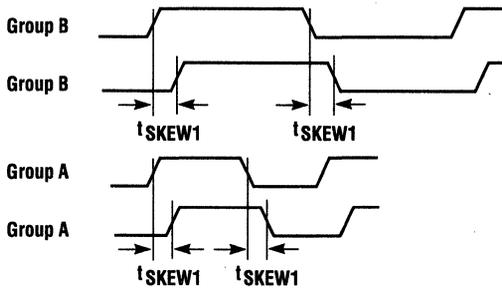


Figure 6. t_{SKEW2}

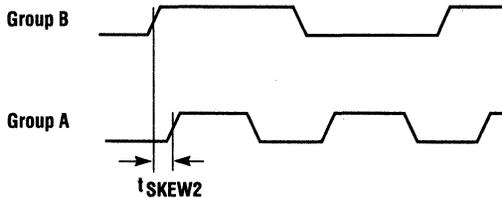


Figure 7. t_{SKEW3} (For Group B Feedback)

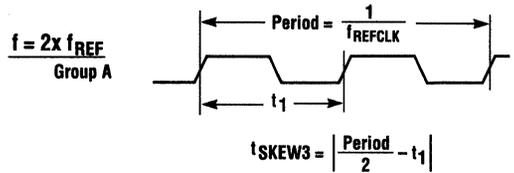
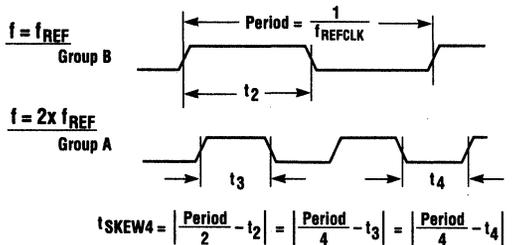
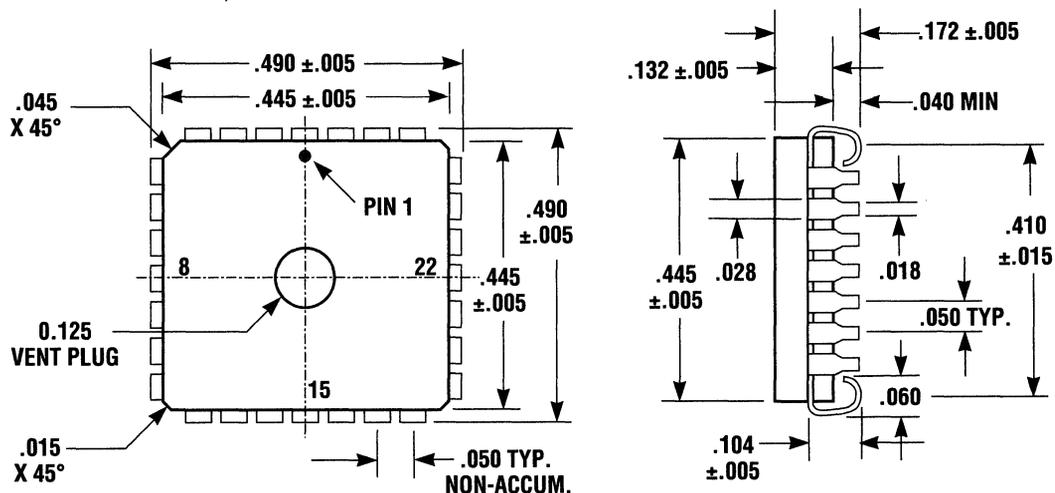


Figure 8. t_{SKEW4}



28-Pin MQuad J-Leaded Package Mechanical Specification

(All dimensions in inches)



28-Pin MQuad Pin Description

Pin #	Pin Name	Description	I/O
1	GND	Ground	—
2	Q9	Output Clock 9 (A5)	O
3	Q10	Output Clock 10 (A6)	O
4	VDD	+5 V	—
5	GND	Ground	—
6	F0	Frequency Select 0	I
7	F1	Frequency Select 1	I
8	GND	Ground	—
9	REFCLK	Reference Clock	I
10	GND	Ground	—
11	FBIN	Feedback In	I
12	TEST	Test	I
13	VDD	+5 V	—
14	Q0	Output Clock 0 (B1)	O

Pin #	Pin Name	Description	I/O
15	GND	Ground	—
16	Q1	Output Clock 1 (B2)	O
17	Q2	Output Clock 2 (B3)	O
18	VDD	+5 V	—
19	GND	Ground	—
20	Q3	Output Clock 3 (B4)	O
21	Q4	Output Clock 4 (B5)	O
22	VDD	+5 V	—
23	Q5	Output Clock 5 (A1)	O
24	Q6	Output Clock 6 (A2)	O
25	GND	Ground	—
26	VDD	+5 V	—
27	Q7	Output Clock 7 (A3)	O
28	Q8	Output Clock 8 (A4)	O

Output Characteristics

The IV characteristics, transition times, package characteristics, device and bond wire-characteristics for the QA1087 are described in Tables 4 through 9 and Figures 9 through 11.

Figure 9. I_{OH} vs. V_{OH}

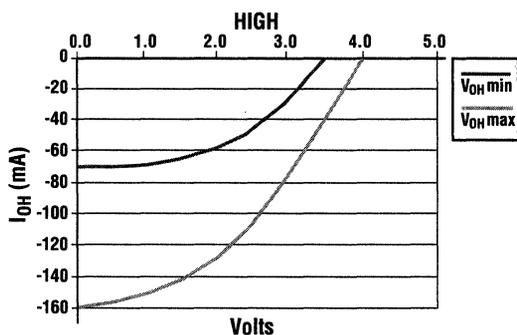


Table 4. I_{OH} vs. V_{OH}

V_{OL}	$I_{OL\ min}$ (mA)	$I_{OL\ max}$ (mA)
0.0	-70	-160
0.5	-70	-157
1.0	-68	-152
1.5	-65	-142
2.0	-59	-130
2.5	-48	-106
3.0	-29	-79
3.5	0	-42
4.0	0	0
4.5	0	0
5.0	0	0
6.0	0	0
7.0	0	0
8.0	0	0
9.0	0	1
10.0	0	5

These output characteristics are provided for modeling purposes only. TriQuint does not guarantee the information in these tables and figures.

Figure 10. I_{OL} vs. V_{OL}

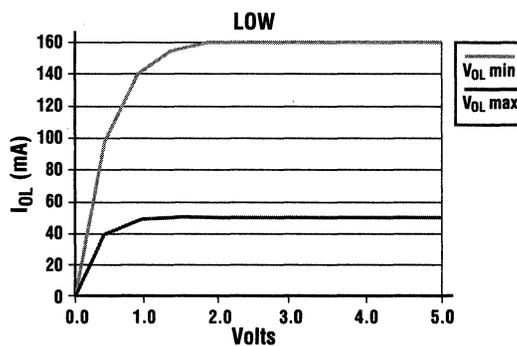


Table 5. I_{OL} vs. V_{OL}

V_{OL}	$I_{OL\ min}$ (mA)	$I_{OL\ max}$ (mA)
-2.5	-145	-435
-2.0	-135	-410
-1.5	-115	-350
-1.0	-90	-265
-0.5	-40	-120
0.0	0	0
0.5	37	97
1.0	49	140
1.5	53	155
2.0	54	157
2.5	54	159
3.0	54	160
3.5	54	160
4.0	54	160
4.5	54	160
5.0	54	160
10.0	54	160

Notes: 1. These are worst-case corners for process, voltage, and temperature.
2. Includes diode to ground current.

Table 6. Above- V_{DD} and Below-Ground Characteristics

Diode to GND		Diode Stack to VDD	
V	I (mA)	V	I (mA)
0.0	0	5.0	0
-0.4	0	6.0	0
-0.5	0	7.0	0
-0.6	-5	8.0	0
-0.7	-15	9.0	0
-0.8	-35	10.0	1
-0.9	-55	11.0	5
-1.0	-75	12.0	9
-2.0	-300		
-2.5	-350		
-3.0	-360		

Note: TriQuint does not guarantee diode operation for purposes other than ESD protection.

Figure 11. Output Model

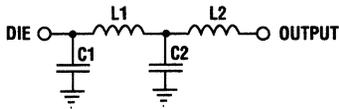


Table 7. Device and Bond-Wire Characteristics (Estimates)

L1	C1
2 nH	10 pF

Table 8. 28-Pin MQuad Package Characteristics

L1	C1
1.85 nH	0.40 pF

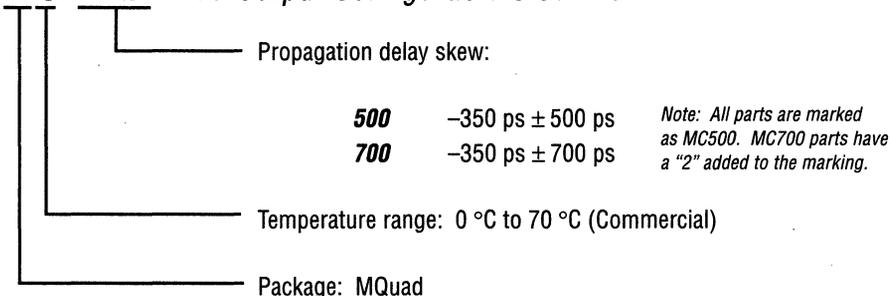
Table 9. Rise and Fall Times (Into 0 pF, 50 Ohms to 1.5 V)

Time (ns)	T_R min (V)	T_R max (V)	T_F min (V)	T_F max (V)
0.0	0.15	0.32	3.20	3.04
0.1	0.15	0.32	3.20	3.04
0.2	0.16	0.32	3.06	2.95
0.3	0.18	0.32	2.86	2.90
0.4	0.23	0.32	2.62	2.68
0.5	0.26	0.32	2.38	2.50
0.6	0.34	0.32	2.17	2.36
0.7	0.46	0.34	2.00	2.22
0.8	0.67	0.39	1.85	2.09
0.9	0.89	0.49	1.69	1.95
1.0	1.12	0.63	1.52	1.86
1.1	1.32	0.86	1.38	1.68
1.2	1.50	1.09	1.26	1.59
1.3	1.73	1.27	1.12	1.49
1.4	1.93	1.45	0.96	1.36
1.5	2.15	1.64	0.83	1.23
1.6	2.75	2.23	0.52	0.95
1.7	2.58	2.00	0.61	1.00
1.8	2.75	2.23	0.52	0.95
1.9	2.90	2.41	0.45	0.91
2.0	3.02	2.50	0.39	0.86
2.1	3.12	2.64	0.33	0.77
2.2	3.17	2.77	0.29	0.73
2.3	3.19	2.86	0.24	0.68
2.4	3.20	2.95	0.21	0.64
2.5	3.20	2.99	0.19	0.59
2.6	3.20	3.02	0.17	0.55
2.7	3.20	3.02	0.16	0.53
2.8	3.20	3.04	0.16	0.50
2.9	3.20	3.04	0.15	0.45
3.0	3.20	3.04	0.15	0.41
3.1	3.20	3.04	0.15	0.40
3.2	3.20	3.04	0.15	0.37
3.3	3.20	3.04	0.15	0.36
3.4	3.20	3.04	0.15	0.32

Ordering Information

To order, please specify as shown below:

GA1087-MC nnn 11-Output Configurable Clock Buffer



Additional Information

For latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com **Tel:** (503) 615-9000
Email: sales@tqs.com **Fax:** (503) 615-8900

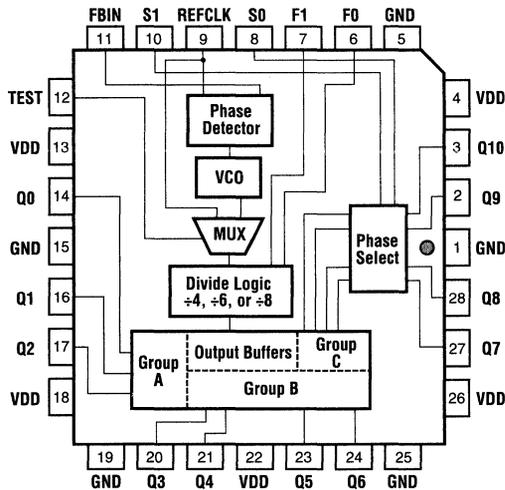
For technical questions and additional information on specific applications:

Email: applications@tqs.com

The information provided herein is believed to be reliable; TriQuint assumes no liability for inaccuracies or omissions. TriQuint assumes no responsibility for the use of this information, and all such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. TriQuint does not authorize or warrant any TriQuint product for use in life-support devices and/or systems.

Copyright © 1997 TriQuint Semiconductor, Inc. All rights reserved.

Revision 1.0.A October 1997



TriQuint's GA1088 is a configurable clock buffer which generates 11 outputs, operating over a wide range of frequencies — from 18 MHz to 105 MHz. The outputs are available at either 1x and 2x or at 1x and 1/2 x the reference clock frequency, f_{REF} . When one of the Group A outputs (Q0–Q2) is used as feedback to the PLL, all Group A outputs will be at f_{REF} , and all Group B (Q3–Q6) and Group C (Q7–Q10) outputs will be at $2x f_{REF}$. When one of the Group B outputs is used as feedback to the PLL, all Group A outputs will be at $1/2 x f_{REF}$ and all Group B and Group C outputs will be at f_{REF} .

A very stable internal Phase-Locked Loop (PLL) provides low-jitter operation. This completely self-contained PLL requires no external capacitors or resistors. The PLL's voltage-controlled oscillator (VCO) has a frequency range from 280 MHz to 420 MHz. By feeding back one of the output clocks to FBIN, the PLL continuously maintains frequency and phase synchronization between the reference clock (REFCLK) and each of the outputs. The Shift Select pins select the phase shift ($-2t$, $-t$, 0 , or $+t$) for Group C outputs (Q7–Q10) with respect to REFCLK. The phase shift increment (t) is equivalent to the VCO's period ($1/f_{VCO}$).

TriQuint's patented output buffer design delivers a very low output-to-output skew of 150 ps (max). The GA1088's symmetrical TTL outputs are capable of sourcing and sinking 30 mA.

GA1088

11-Output Configurable Clock Buffer

Features

- Wide frequency range: 18 MHz to 105 MHz
- Output configurations: three outputs at $1/2 f_{REF}$, three outputs at f_{REF} , four outputs at f_{REF} with adjustable phase or two outputs at f_{REF} , four outputs at $2x f_{REF}$, four outputs at $2x f_{REF}$ with adjustable phase
- Selectable Phase Shift: $-2t$, $-t$, 0 , and $+t$ ($t = 1/f_{VCO}$)
- Low output-to-output skew: 150 ps (max) within a group
- Near-zero propagation delay: $-350 \text{ ps} \pm 500 \text{ ps}$ (max) or $-350 \text{ ps} \pm 700 \text{ ps}$ (max)
- TTL-compatible with 30 mA output drive
- 28-pin J-lead surface-mount package

SYSTEM TIMING PRODUCTS

Functional Description

The core of the GA1088 is a Phase-Locked Loop (PLL) that continuously compares the reference clock (REFCLK) to the feedback clock (FBIN), maintaining a zero frequency difference between the two. Since one of the outputs (Q0–Q6) is always connected to FBIN, the PLL keeps the propagation delay between the outputs and the reference clock within $-350 \text{ ps} \pm 500 \text{ ps}$ for the GA1088-MC500, and within $-350 \text{ ps} \pm 700 \text{ ps}$ for the GA1088-MC700.

The internal voltage-controlled oscillator (VCO) has an operating range of 280 MHz to 420 MHz. The combination of the VCO and the Divide Logic enables the GA1088 to operate between 18 MHz and 105 MHz. The device features six divide modes: +4, +6, +8, +8, +12, and +16. The Frequency Select pins, F0 and F1, and the output used as feedback to FBIN set the divide mode as shown in Table 1.

The Shift Select pins, S0 and S1, control the phase shift of the Group C outputs (Q7–Q10), relative to the other outputs. The user can select from four

incremental phase shifts as shown in Table 2 (Phase Selection). The phase-shift increment (t) is calculated using the following equation (where n is the divide mode):

$$t = \frac{1}{(f_{\text{REF}})(n)}$$

In the test mode, the PLL is bypassed and REFCLK is connected directly to the Divide Logic block via the MUX, as shown in Figure 1. This mode is useful for debug and test purposes. The various test modes are outlined in Table 3. In the test mode, the frequency of the reference clock is divided by 4, 6, or 8.

The maximum rise and fall time at the output pins is 1.4 ns. All outputs of the GA1088 are TTL-compatible with 30 mA symmetric drive and a minimum V_{OH} of 2.4 V.

Power Up/Reset Synchronization

After power up or reset, the PLL requires time before it achieves synchronization lock. The maximum time required for synchronization (TSYNC) is 500 ms.

Table 1. Frequency Mode Selection

Feedback: Any Group A Output (Q0 – Q2)

Test	Select Pins		Mode	Reference Clock Frequency Range	Output Frequency Range	
	F0	F1			Group A: Q0–Q2	Group B,C: Q3–Q10
0	0	0	Not Used	N.A.	N.A.	N.A.
0	1	0	+ 8	35 MHz – 50 MHz	35 MHz – 50 MHz	70 MHz – 105 MHz
0	0	1	+ 12	24 MHz – 35 MHz	24 MHz – 35 MHz	48 MHz – 70 MHz
0	1	1	+ 16	18 MHz – 26 MHz	18 MHz – 26 MHz	35 MHz – 52 MHz

Feedback: Any Group B Output (Q3 – Q6)

Test	Select Pins		Mode	Reference Clock Frequency Range	Output Frequency Range	
	F0	F1			Group A: Q0–Q2	Group B,C: Q3–Q10
0	0	0	Not Used	N.A.	N.A.	N.A.
0	1	0	+ 4	70 MHz – 105 MHz	35 MHz – 50 MHz	70 MHz – 105 MHz
0	0	1	+ 6	48 MHz – 70 MHz	24 MHz – 35 MHz	48 MHz – 70 MHz
0	1	1	+ 8	35 MHz – 52 MHz	18 MHz – 26 MHz	35 MHz – 52 MHz

Table 2. Phase Selection

S0	S1	Phase Difference (Q9, Q10)
0	0	+t
1	0	0
0	1	-t
1	1	-2t

Table 3. Test Mode Selection

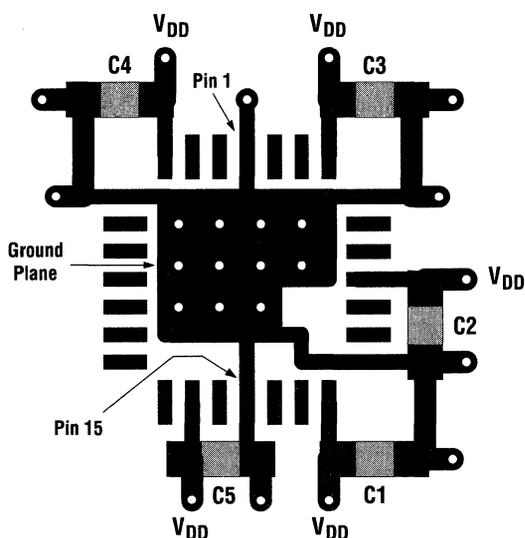
Test	F0	F1	Mode	Ref. Clock	Group A: Outputs Q0–Q2	Group B,C Outputs Q3–Q10
1	0	0	not used	—	—	—
1	1	0	+4	f_{REF}	$f_{REF} + 8$	$f_{REF} + 4$
1	0	1	+6	f_{REF}	$f_{REF} + 12$	$f_{REF} + 6$
1	1	1	+8	f_{REF}	$f_{REF} + 16$	$f_{REF} + 8$

Layout Guidelines

Multiple ground and power pins on the GA1088 reduce ground bounce. Good layout techniques, however, are necessary to guarantee proper operation and to meet the specifications across the full operating range. TriQuint recommends bypassing each of the V_{DD} supply pins to the nearest ground pin, as close to the chip as possible.

Figure 2 shows the recommended power layout for the GA1088. The bypass capacitors should be located on the same side of the board as the GA1088. The V_{DD} traces connect to an inner-layer V_{DD} plane. All of the ground pins (GND) are connected to a small ground plane on the surface beneath the chip. Multiple through-holes connect this small surface plane to an inner-layer ground plane. The capacitors (C1–C5) are 0.1 mF. TriQuint's test board uses X7R temperature-stable capacitors in 1206 SMD cases.

Figure 2. Top Layer Layout of Power Pins (approx. 3.3x)



Absolute Maximum Ratings¹

Storage temperature	-65 °C to +150 °C
Ambient temperature with power applied ²	-55 °C to +100 °C
Supply voltage to ground potential	-0.5 V to +7.0 V
DC input voltage	-0.5 V to (V _{DD} + 0.5) V
DC input current	-30 mA to +5 mA
Package thermal resistance (MQuad)	$\theta_{JA} = 45$ °C/W
Die junction temperature	T _J = 150 °C

DC Characteristics (V_{DD} = +5 V ± 5%, T_A = 0 °C to +70 °C)³

Symbol	Description	Test Conditions	Limits ⁴			Unit
			Min	Typ	Max	
V _{OHT}	Output HIGH voltage	V _{DD} = Min I _{OH} = -30 mA V _{IN} = V _{IH} or V _{IL}	2.4	3.4		V
V _{OHC}	Output HIGH voltage	V _{DD} = Min I _{OH} = -1 mA V _{IN} = V _{IH} or V _{IL}	3.2	4.1		V
V _{OL}	Output LOW voltage	V _{DD} = Min I _{OL} = 30 mA V _{IN} = V _{IH} or V _{IL}		0.27	0.5	V
V _{IH} ⁵	Input HIGH level	Guaranteed input logical HIGH Voltage for all Inputs	2.0			V
V _{IL} ⁵	Input LOW level	Guaranteed input logical LOW Voltage for all inputs			0.8	V
I _{IL}	Input LOW current	V _{DD} = Max V _{IN} = 0.40 V		-156	-400	μA
I _{IH}	Input HIGH current	V _{DD} = Max V _{IN} = 2.7 V		0	25	μA
I _I	Input HIGH current	V _{DD} = Max V _{IN} = 5.5 V		2	1000	μA
I _{DD5} ⁶	Power supply current	V _{DD} = Max		119	160	mA
V _I	Input clamp voltage	V _{DD} = Min I _{IN} = -18 mA		-0.70	-1.2	V

Capacitance

Symbol	Description	Test Conditions	Min	Typ	Max
C _{IN} ^{3,7}	Input capacitance	V _{IN} = 2.0 V at f = 1 MHz		6	pF

- Notes:
1. Exceeding these parameters may damage the device.
 2. Maximum ambient temperature with device not switching and unloaded.
 3. These values apply to both GA1088-MC500 and GA1088-MC700.
 4. Typical limits are at V_{DD} = 5.0 V and T_A = 25 °C.
 5. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
 6. This parameter is measured with device not switching and unloaded.
 7. These parameters are not 100% tested, but are periodically sampled.

AC Characteristics ($V_{DD} = +5 V \pm 5\%$, $T_A = 0^\circ C$ to $+70^\circ C$)

Symbol	Input Clock (REFCLK)	Test Conditions (Figure 3) ¹	Min	Typ	Max	Unit
t_{CPWH}	CLK pulse width HIGH	Figure 4	3	---	—	ns
t_{CPWL}	CLK pulse width LOW	Figure 4	3	---	—	ns
t_{IR}	Input rise time (0.8 V - 2.0 V)		—	—	2.0	ns

Symbol	Input Clock (Q0-Q10)	Test Conditions (Figure 3) ¹	Min	Typ	Max	Unit
t_{OR}, t_{OF}	Rise/fall time (0.8 V - 2.0 V)	Figure 4	350	—	1400	ps
t_{PD1} ²	CLK \uparrow to FBIN \uparrow (GA1088-MC500)	Figure 4	-850	-350	+150	ps
t_{PD2} ²	CLK \uparrow to FBIN \uparrow (GA1088-MC700)	Figure 4	-1050	-350	+350	ps
t_{SKEW1} ³	Rise-rise, fall-fall (within group)	Figure 5	—	60	150	ps
t_{SKEW2} ³	Rise-rise, fall-fall (group-to-group, aligned)	Figure 6 (skew2 takes into account skew1)	—	75	350	ps
t_{SKEW3} ³	Rise-rise, fall-fall (group-to-group, non-aligned)	Figure 7 (skew3 takes into account skew1, 2)	—	—	650	ps
t_{SKEW4} ³	Rise-fall, fall-rise	Figure 8 (skew4 takes into account skew3)	—	—	1200	ps
t_{CYC} ⁴	Duty-cycle Variation	Figure 4	-1000	0	+1000	ps
t_{JP} ⁵	Period-to-Period Jitter	Figure 4	—	80	200	ps
t_{JR} ⁵	Random Jitter	Figure 4	—	190	400	ps
t_{SYNC} ⁶	Synchronization Time		—	10	500	μ s

Notes: 1. All measurements are tested with a REFCLK having a rise time of 0.5 ns (0.8 V to 2.0 V).

2. The PLL maintains alignment of CLK and FBIN at all times. This specification applies to the rising edge only because the input duty cycle can vary while the output duty cycle is typically 50/50. The delay t_{PD} is measured at the 1.5 V level between CLK and FBIN.

3. Skew specifies the width of the window in which outputs switch, and is measured at 1.5 V.

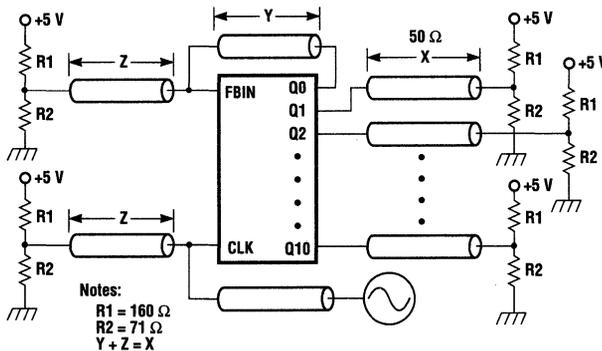
4. This specification represents the deviation from 50/50 on the outputs.

5. Jitter specifications refer to peak-to-peak value. t_{JR} is the jitter on the output with respect to the reference clock. t_{JP} is the jitter on the output with respect to the output's previous rising edge.

6. t_{SYNC} is the time required for the PLL to synchronize; this assumes the presence of a CLK signal and a connection from one of the outputs to FBIN.

SYSTEM TIMING PRODUCTS

Figure 3. AC Test Circuit



Switching Waveforms

Figure 4. General Timing

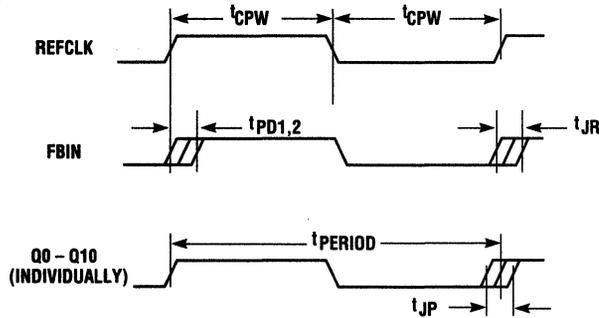


Figure 5. t_{SKEW1}

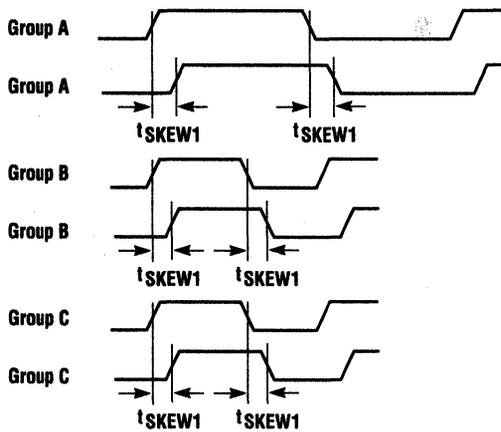


Figure 6. t_{SKEW2}

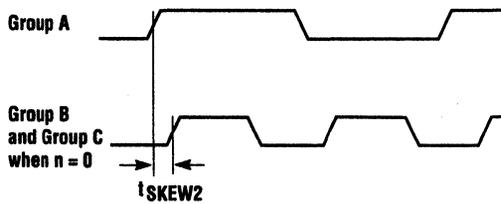
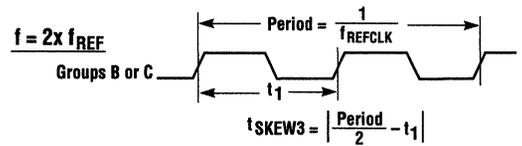
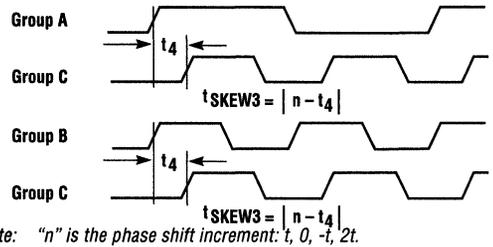


Figure 7. t_{SKEW3}

(For Group A Feedback)

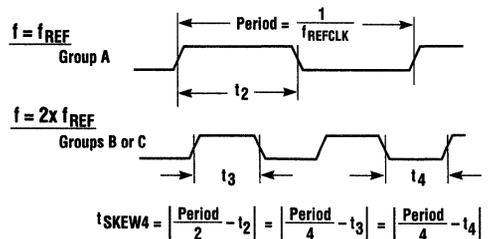


(For Group A or B Feedback)



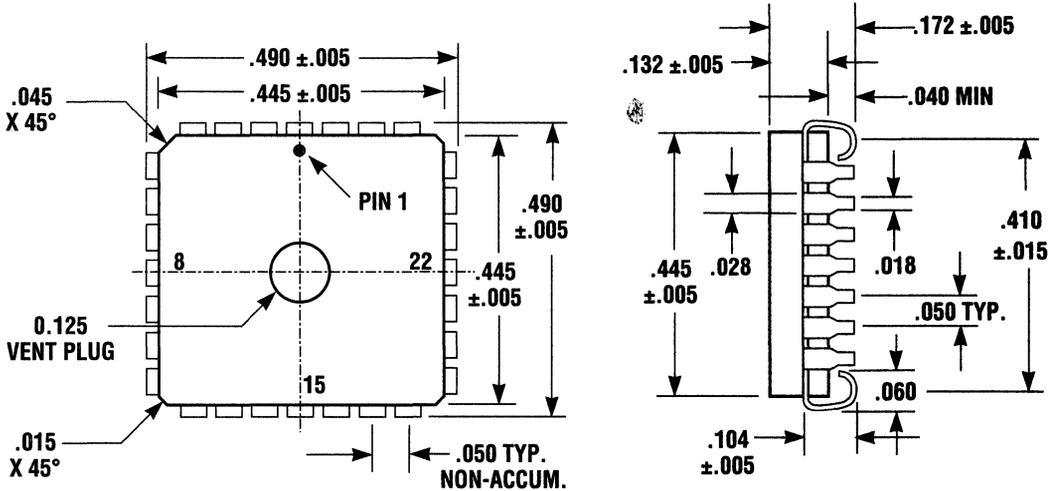
Note: "n" is the phase shift increment: t, 0, -t, 2t.

Figure 8. t_{SKEW4}



28-Pin MQuad J-Leaded Package Mechanical Specification

(All dimensions are in inches)



28-Pin MQuad Pin Description

Pin #	Pin Name	Description	I/O
1	GND	Ground	—
2	Q9	Output Clock 9 (C3)	O
3	Q10	Output Clock 10 (C4)	O
4	VDD	+5 V	—
5	GND	Ground	—
6	F0	Frequency Select 0	I
7	F1	Frequency Select 1	I
8	S0	Shift Select 0	I
9	REFCLK	Reference Clock	I
10	S1	Shift Select 1	I
11	FBIN	Feedback In	I
12	TEST	Test	I
13	VDD	+5 V	—
14	Q0	Output Clock 0 (A1)	O

Pin #	Pin Name	Description
15	GND	Ground
16	Q1	Output Clock 1 (A2)
17	Q2	Output Clock 2 (A3)
18	VDD	+5 V
19	GND	Ground
20	Q3	Output Clock 3 (B1)
21	Q4	Output Clock 4 (B2)
22	VDD	+5 V
23	Q5	Output Clock 5 (B3)
24	Q6	Output Clock 6 (B4)
25	GND	Ground
26	VDD	+5 V
27	Q7	Output Clock 7 (C1)
28	Q8	Output Clock 8 (C2)

SYSTEM TIMING PRODUCTS

Output Characteristics

The IV characteristics, transition times, package characteristics, device and bond wire characteristics for the GA1088 are described in Tables 4 through 9 and Figures 9 through 11.

Figure 9. I_{OH} vs. V_{OH}

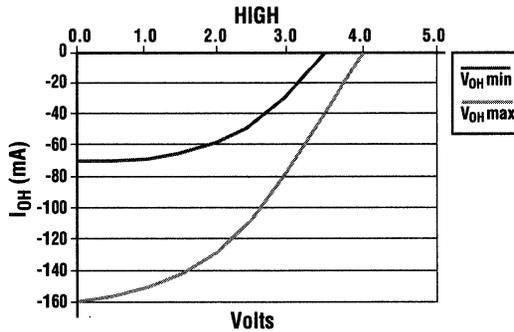


Table 4. I_{OH} vs. V_{OH}

V_{OL}	$I_{OL\ min}$ (mA)	$I_{OL\ max}$ (mA)
0.0	-70	-160
0.5	-70	-157
1.0	-68	-152
1.5	-65	-142
2.0	-59	-130
2.5	-48	-106
3.0	-29	-79
3.5	0	-42
4.0	0	0
4.5	0	0
5.0	0	0
5.5	40	120
6.0	90	265
6.5	115	350
7.0	135	410
7.5	145	435

These output characteristics are provided for modelling purposes only. TriQuint does not guarantee the information in these tables and figures.

Figure 10. I_{OL} vs. V_{OL}

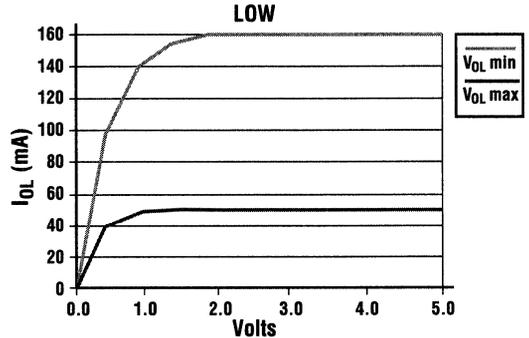


Table 5. I_{OL} vs. V_{OL}

V_{OL}	$I_{OL\ min}$ (mA)	$I_{OL\ max}$ (mA)
-2.5	-145	-435
-2.0	-135	-410
-1.5	-115	-350
-1.0	-90	-265
-0.5	-40	-120
0.0	0	0
0.5	37	97
1.0	49	140
1.5	53	155
2.0	54	157
2.5	54	159
3.0	54	160
3.5	54	160
4.0	54	160
4.5	54	160
5.0	54	160
10.0	54	160

Notes: 1. These are worst-case corners for process, voltage, and temperature.
2. Includes diode-to-ground current.

Table 6. Above- V_{DD} and Below-Ground Characteristics

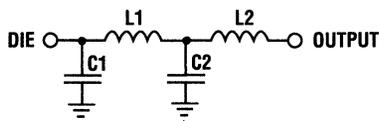
Diode to GND		Diode Stack to VDD	
V	I (mA)	V	I (mA)
0.0	0	5.0	0
-0.4	0	5.4	0
-0.5	0	5.5	0
-0.6	-5	5.6	5
-0.7	-15	5.7	15
-0.8	-35	5.8	35
-0.9	-55	5.9	55
-1.0	-75	6.0	75
-2.0	-300	7.0	300
-2.5	-350	7.5	350
-3.0	-360	8.0	360

Note: TriQuint does not guarantee diode operation for purposes other than ESD protection.

**Table 9. Rise and Fall Times
(Into 0 pF, 50 Ohms to 1.5 V)**

Time (ns)	T_R min (V)	T_R max (V)	T_F min (V)	T_F max (V)
0.0	0.15	0.32	3.20	3.04
0.1	0.15	0.32	3.20	3.04
0.2	0.16	0.32	3.06	2.95
0.3	0.18	0.32	2.86	2.90
0.4	0.23	0.32	2.62	2.68
0.5	0.26	0.32	2.38	2.50
0.6	0.34	0.32	2.17	2.36
0.7	0.46	0.34	2.00	2.22
0.8	0.67	0.39	1.85	2.09
0.9	0.89	0.49	1.69	1.95
1.0	1.12	0.63	1.52	1.86
1.1	1.32	0.86	1.38	1.68
1.2	1.50	1.09	1.26	1.59
1.3	1.73	1.27	1.12	1.49
1.4	1.93	1.45	0.96	1.36
1.5	2.15	1.64	0.83	1.23
1.6	2.75	2.23	0.52	0.95
1.7	2.58	2.00	0.61	1.00
1.8	2.75	2.23	0.52	0.95
1.9	2.90	2.41	0.45	0.91
2.0	3.02	2.50	0.39	0.86
2.1	3.12	2.64	0.33	0.77
2.2	3.17	2.77	0.29	0.73
2.3	3.19	2.86	0.24	0.68
2.4	3.20	2.95	0.21	0.64
2.5	3.20	2.99	0.19	0.59
2.6	3.20	3.02	0.17	0.55
2.7	3.20	3.02	0.16	0.53
2.8	3.20	3.04	0.16	0.50
2.9	3.20	3.04	0.15	0.45
3.0	3.20	3.04	0.15	0.41
3.1	3.20	3.04	0.15	0.40
3.2	3.20	3.04	0.15	0.37
3.3	3.20	3.04	0.15	0.36
3.4	3.20	3.04	0.15	0.32
3.5	3.20	3.04	0.15	0.32

Figure 11. Output Model



**Table 7. Device and Bond-Wire Characteristics
(Estimated)**

L1	C1
2 nH	10 pF

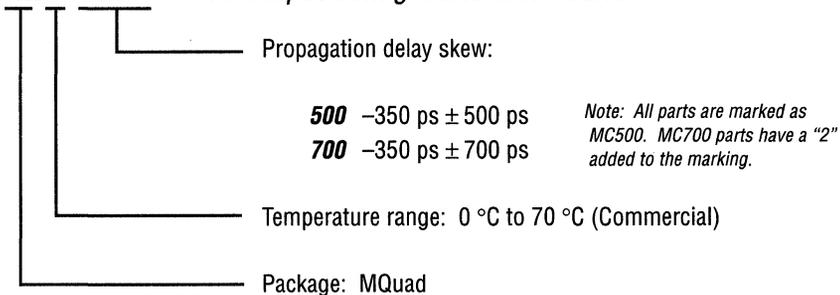
Table 8. 28-Pin MQuad Package Characteristics

L2	C2
1.85 nH	0.40 pF

Ordering Information

To order, please specify as shown below:

GA1088-MC nnn 11-Output Configurable Clock Buffer



Additional Information

For latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com **Tel:** (503) 615-9000
Email: sales@tqs.com **Fax:** (503) 615-8900

For technical questions and additional information on specific applications:

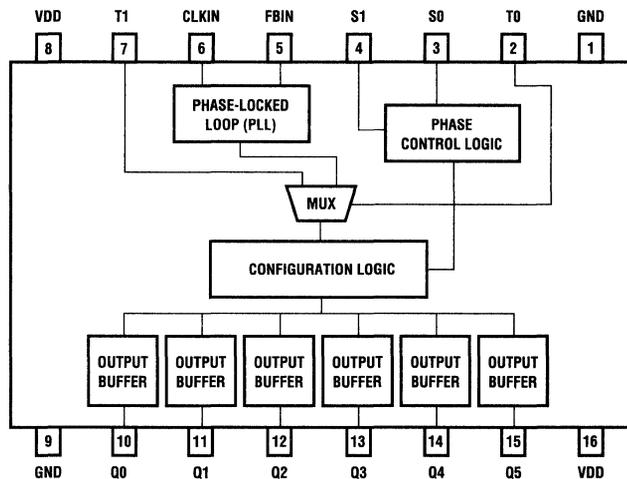
Email: applications@tqs.com

The information provided herein is believed to be reliable; TriQuint assumes no liability for inaccuracies or omissions. TriQuint assumes no responsibility for the use of this information, and all such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. TriQuint does not authorize or warrant any TriQuint product for use in life-support devices and/or systems.

Copyright © 1997 TriQuint Semiconductor, Inc. All rights reserved.

Revision 1.0.A October 1997

Figure 1. Block Diagram



TriQuint's GA1110E is a low-skew TTL-level clock buffer chip with multi-phase clock generation. It produces multiple clock outputs which are normally phase- and frequency-synchronized to a periodic clock input signal. It offers the user the additional flexibility to adjust the phase of the individual outputs in increments of ± 2.5 ns. With the precise placement of output clock edges relative to a system clock input, the GA1110E can provide a complete system clocking solution.

The tight control over the phase and frequency of the output clocks is achieved with a 400 MHz internal phase-locked loop (PLL). By feeding back one of the output clocks (to FBIN), the on-chip PLL can continuously maintain synchronization between the input clock (CLKIN) and all six outputs. Any drift or gradual variation in the system clock will be matched and tracked at the six outputs.

The GA1110E offers the user fourteen different output clock configurations. Using the external feedback capability and the two select pins (S1 and S0), the desired phase relationships (among the 14 possibilities) of the output clocks may be chosen to best solve the system's clocking requirements. The output clock edges are "placed" in precise, digitally-controlled ± 2.5 ns increments relative to the input and feedback clock phase. The fourteen "phase-relationship" options are listed in Table 1 and example waveforms and block diagrams are shown in Figures 5 through 8.

GA1110E

Multi-Phase Clock Buffer

Features

- Zero-propagation-delay clock buffer
- Output skew controlled to ± 250 ps (typ.), ± 500 ps (max.)
- Self-contained on-chip 400 MHz phase-locked loop (PLL)
- User-selectable phase shifting on the output clocks in 2.5 ns increments.
- Available in 20, 25, 33, 40 and 50 MHz versions
- High-drive, symmetric TTL-compatible outputs with rise time of 1.0 ns
- Special test mode
- 130 mA operating current (typ.), 160 mA (max.)
- Standard 16-pin DIP and 28-pin surface-mount packages

The GA110E is fabricated using TriQuint's One-Up™ gallium arsenide technology to achieve precise timing control and to guarantee 100% TTL-compatibility. The 20, 25, 33, 40 and 50 MHz input frequencies make this device ideal for clock distribution, phase adjustment, and clock skew control in a wide range of high-performance RISC- and CISC-based systems.

Functional Description

The GA110E TTL-level clock buffer/phase generator chip provides multiple outputs synchronized in phase and frequency to a periodic clock input. The chip utilizes two select pins and external feedback to allow the user to "phase-adjust" the outputs relative to the input clock. The phase adjustments can be made in increments of t_{PH} ; this value is given in the AC Characteristics table.

Table 1 enumerates the fourteen configurations available to the user. The first two columns specify the signal levels on the select pins S1 and S0. These are active-HIGH signals. The third column indicates which output (Q0..5) should be externally connected to the feedback input (FBIN) to achieve the desired phase relationship shown for a given configuration in the table. The last six columns specify the resulting phase relationship of each output to the user clock input (CLKIN). A negative value is the time by which the output rising edge precedes the input (CLKIN) rising edge, while a positive value is the time by which the output rising edge follows the input (CLKIN) rising edge.

Example: The system clocking requirements may specify several low-skew outputs, one early clock, one late clock, and one inverted clock.

Configuration 3 in Table 1 provides such a solution. With $S1 = LOW$, $S0 = HIGH$, and Q0 (or Q1 or Q4) connected back to FBIN, the required outputs will be generated. Q0, Q1 and Q4 will be phase-aligned to the input (CLKIN), Q3 will provide an early clock (by one t_{PH} , the phase-shift increment), Q2 will provide the late clock (by one t_{PH}), and Q5 will provide a phase-aligned, inverted copy of the input. The GA110E's PLL will maintain these phase relationships continually, as shown in Figure 6.

Several of the operating configurations in Table 1 include inverted clock outputs. If the inverted clock is aligned to the input (i.e. exactly 180 degrees out of phase), the table entry reads as "I". If this inverted clock is also phase-shifted, the phase shift is relative to CLKIN and is specified as "I+t" or "I-t."

Example: Configuration 5 of the table corresponds to $S1 = LOW$, $S0 = HIGH$ and Q3 connected to FBIN. In this case, Q3 is phase-aligned to the input clock (CLKIN), Q0, Q1 and Q4 are phase-delayed by one t_{PH} , Q2 is phase-delayed by two t_{PH} s, and the Q5 output is an inverted copy of CLKIN, phase-delayed by one t_{PH} .

Multiple-Chip Applications

Because of the tight input-output phase control, the GA110E can be easily cascaded to build low-skew clock chains and clock trees. The problem of clock fanout can be solved with minimal skew between any two clocks in the chain. This can be done on a single circuit board, as well as across a backplane to maintain synchronization throughout multiple boards in a system.

Breaking the Feedback Loop

There is no requirement that the external feedback connection be a direct hardwire from an output pin to the FBIN pin. So long as the signal at FBIN is derived directly from one of the output pins and maintains its frequency, additional logic incorporating any delay whatsoever can be accommodated. The internal phase-locked loop will adjust the output clocks on the GA1110E to ensure zero phase-delay between the FBIN and CLKIN signals. This feature is extremely valuable in synchronizing ASICs to the system clock.

Caution: The signal at FBIN must be continuous (i.e. not a gated or conditional signal), and must be derived directly from one of the GA1110E's outputs.

Power-Up/Reset Synchronization

The GA1110E utilizes on-chip phase-locked loop technology to maintain synchronization between inputs and outputs. Whenever the device is powered up, or the system clock (CLKIN) is reset, the phase-locked

loop requires a synchronization time (t_{SYNC}) before lock is achieved. The maximum time required is specified in the AC Characteristics table.

For lock to occur, one of the outputs must always be connected (either directly or through additional ICs) to the FBIN input.

Other TriQuint Clock Devices

TriQuint also offers the GA1210E, a low-skew TTL-level clock doubler. Using on-board PLL technology, the GA1210E generates multiple 2X clock outputs from a single input at 20, 25, 33, 40, or 50 MHz. By feeding back one of the outputs, a typical delay of ± 250 ps through the part is achieved. Skew across all six outputs is typically ± 250 ps.

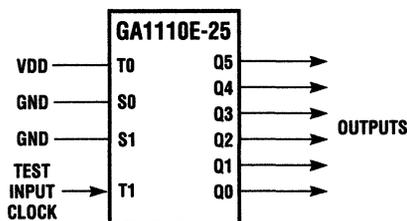
GA110E Test Mode

The GA110E has a test mode which can be enabled if the test pin T0 is HIGH. Under that condition, the clock signal from the test pin T1 is used as the clock input to the configuration logic, instead of the output from the PLL. This mode can be used to test only the internal state machine and associated logic. Each speed type and configuration has a unique signature which is present at the output after “n” number of input clock

pulses. [For the GA110E-25 there will be one output clock cycle for every 16 input clock cycles from t_0 .]

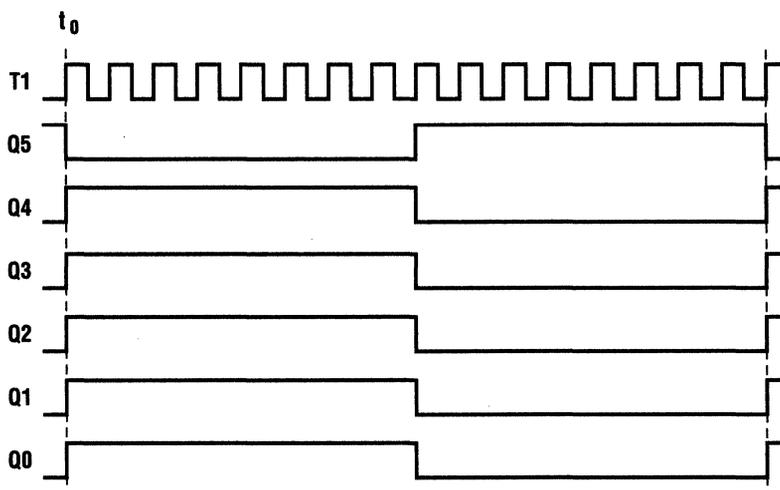
The figures below show the test mode and associated timing for Configuration 1 of the GA110E-25. (See Configuration 1 in Table 1.) When powered up, the Q0 through Q5 outputs can be in any state. It can take up to 16 clocks to get the outputs to the predetermined state at t_0 . The number of clock cycles at input T1 required for one output clock cycle is 20 for GA110E-20, 12 for the GA110E-33, 10 for the GA110E-40 and 8 for the GA110E-50.

Figure 2. Test Mode for the GA110E-25 (Configuration 1)



The test input clock at T1 can either be used to single-step the outputs, or it can be clocked at rates up to 200 MHz. Please note that for the normal mode of operation, T0 is LOW (GND) and T1 can be HIGH (V_{DD}) or No Connect (N/C).

Figure 3. GA110E-25 Test Mode Timing Waveform



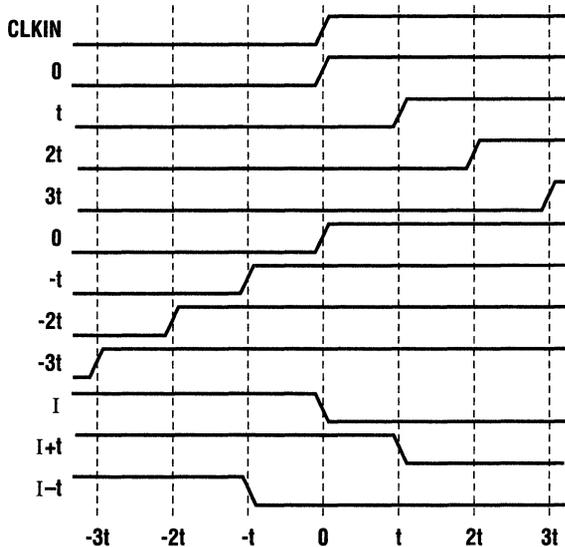
Note: The above timing applies to the case when $S1 = S0 = 0$ and $T0 = 1$ (test mode).

Table 1. Configuration Table

Configuration Number	Select Pins		Output Fed Back to FBIN	Output Phase Shift (see Figure 4)					
	S1	S0		Q0	Q1	Q2	Q3	Q4	Q5
1	0	0	Q0..Q4	0	0	0	0	0	1
2	0	0	Q5	1	1	1	1	1	0
3	0	1	Q0, Q1, Q4	0	0	t	-t	0	1
4	0	1	Q2	-t	-t	0	-2t	-t	1-t
5	0	1	Q3	t	t	2t	0	t	1+t
6	0	1	Q5	1	1	1+t	1-t	1	0
7	1	0	Q0, Q2, Q3	0	t	0	0	-t	-2t
8	1	0	Q1	-t	0	-t	-t	-2t	-3t
9	1	0	Q4	t	2t	t	t	0	-t
10	1	0	Q5	2t	3t	2t	2t	t	0
11	1	1	Q0	0	t	t	-t	-t	-2t
12	1	1	Q1, Q2	-t	0	0	-2t	-2t	-3t
13	1	1	Q3, Q4	t	2t	2t	0	0	-t
14	1	1	Q5	2t	3t	3t	t	t	0

- Notes: 1. "t" represents t_{PH} , the phase-shift increment specified on page 10.
 2. A "0" phase implies the output is aligned to CLKIN.
 3. A negative phase implies the output precedes CLKIN.
 4. A positive phase implies the output follows CLKIN.
 5. "1" implies an inverted version of CLKIN.

Figure 4. Legend

TABLE 1
ENTRYCORRESPONDING
WAVEFORMS*

* Each division represents one t_{PH} , the phase increment

Configuration Examples

Following are four sample configurations corresponding to Table 1.

Figure 5. Configuration 1

S1 = 0 S0 = 0
FBIN = Q0

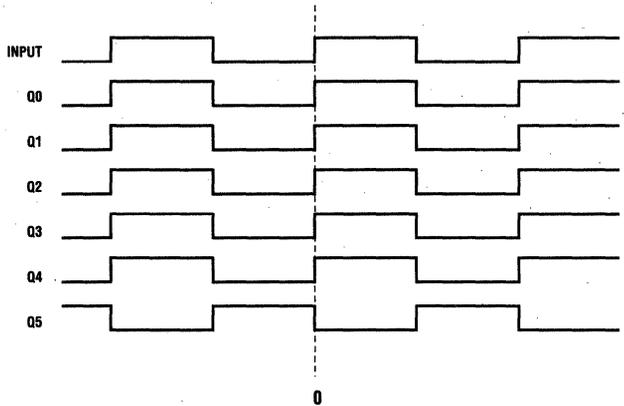
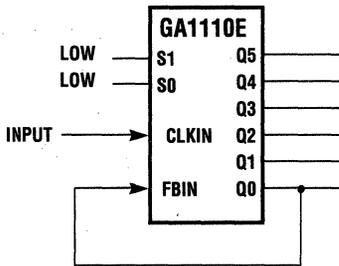


Figure 6. Configuration 3

S1 = 0 S0 = 1
FBIN = Q1

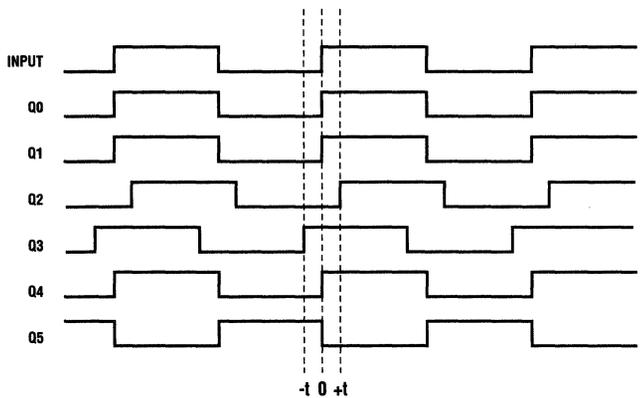
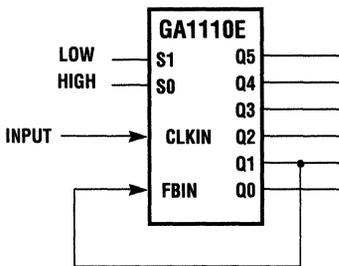


Figure 7. Configuration 8

S1 = 1 S0 = 0
FBIN = Q1

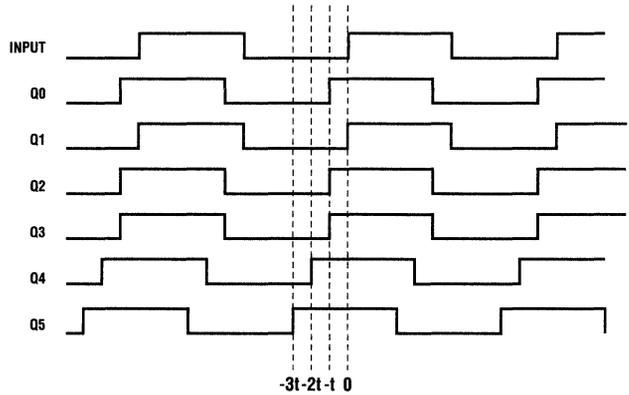
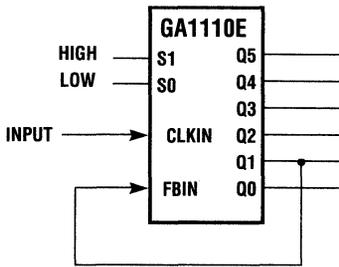
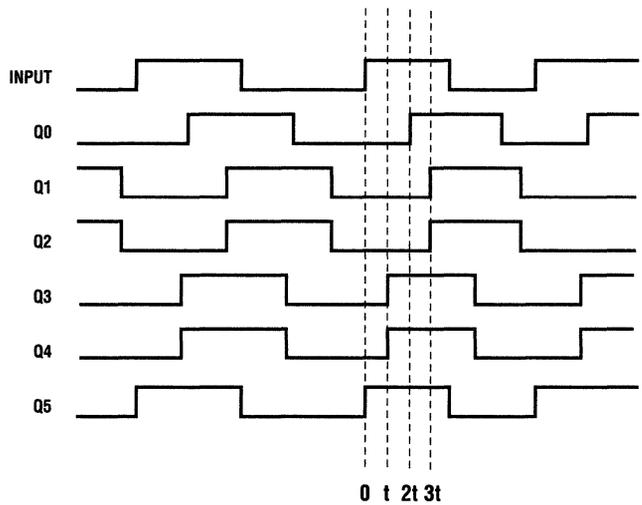
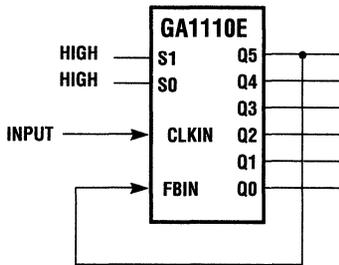


Figure 8. Configuration 14

S1 = 1 S0 = 1
FBIN = Q5



SYSTEM TIMING
PRODUCTS

Typical Applications

The GA110E is designed to satisfy a wide range of system clocking requirements. The following are four of the most common clocking bottlenecks which can be alleviated using the GA110E. These applications are illustrated in Figures 9A through 9D.

1) Low-Skew Clock Distribution / Clock Trees

The most basic bottleneck to clocking high-performance systems is generating multiple copies of a system clock, while maintaining low skew throughout the system.

- *The GA110E guarantees low skew among all clocks in the system by controlling both the input-to-output delay and the skew among all outputs.*

2) Board-to-Board Clock Synchronization

Many computing systems today consist of multiple boards and cards designed to run synchronously. The skew associated with routing clocks across a backplane presents a major hurdle to maximizing system performance.

- *The tightly controlled input/output delay of the GA110E ensures all boards in the system are running synchronously.*
- *The phase-shift feature on the device outputs can be used to compensate for the differing physical distances between multiple cards in a system.*

Figure 9A. Low-Skew Clocks

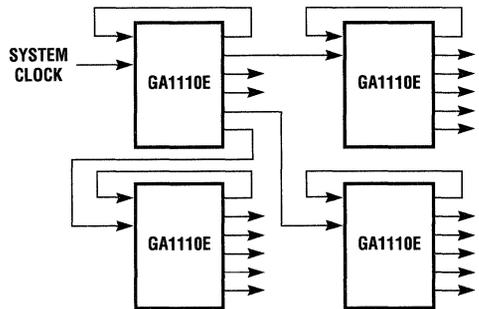
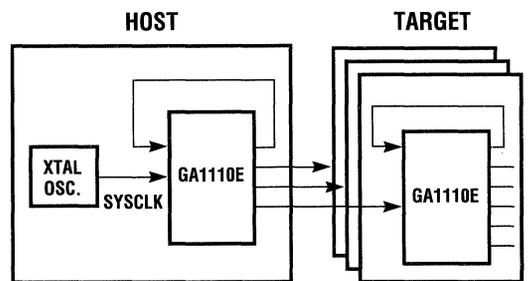


Figure 9B. Board-to-Board Synchronization



Typical Applications (continued)

3) Leading and Lagging Edge Clock Generation

In synchronous or state machine designs where clocks must be sequential, or where metastability becomes a concern, tight edge placement of clock signals becomes a primary requirement.

- The GA1110E, using its phase-control feature, can guarantee by design that clock signals are sequential in as little as 2.5 ns increments.
- This enables pipelined logic which is unbalanced to be clocked in different phases, alleviating setup/hold time requirements.

Figure 9C. Sequential Clock Signals

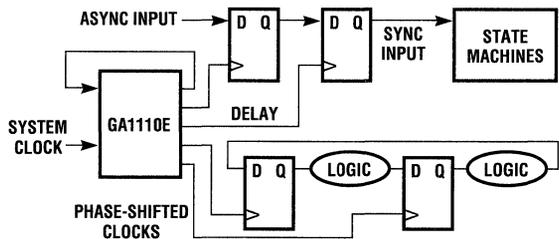
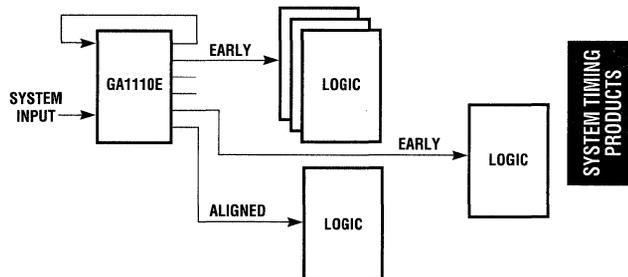


Figure 9D. Timing and Load Compensation



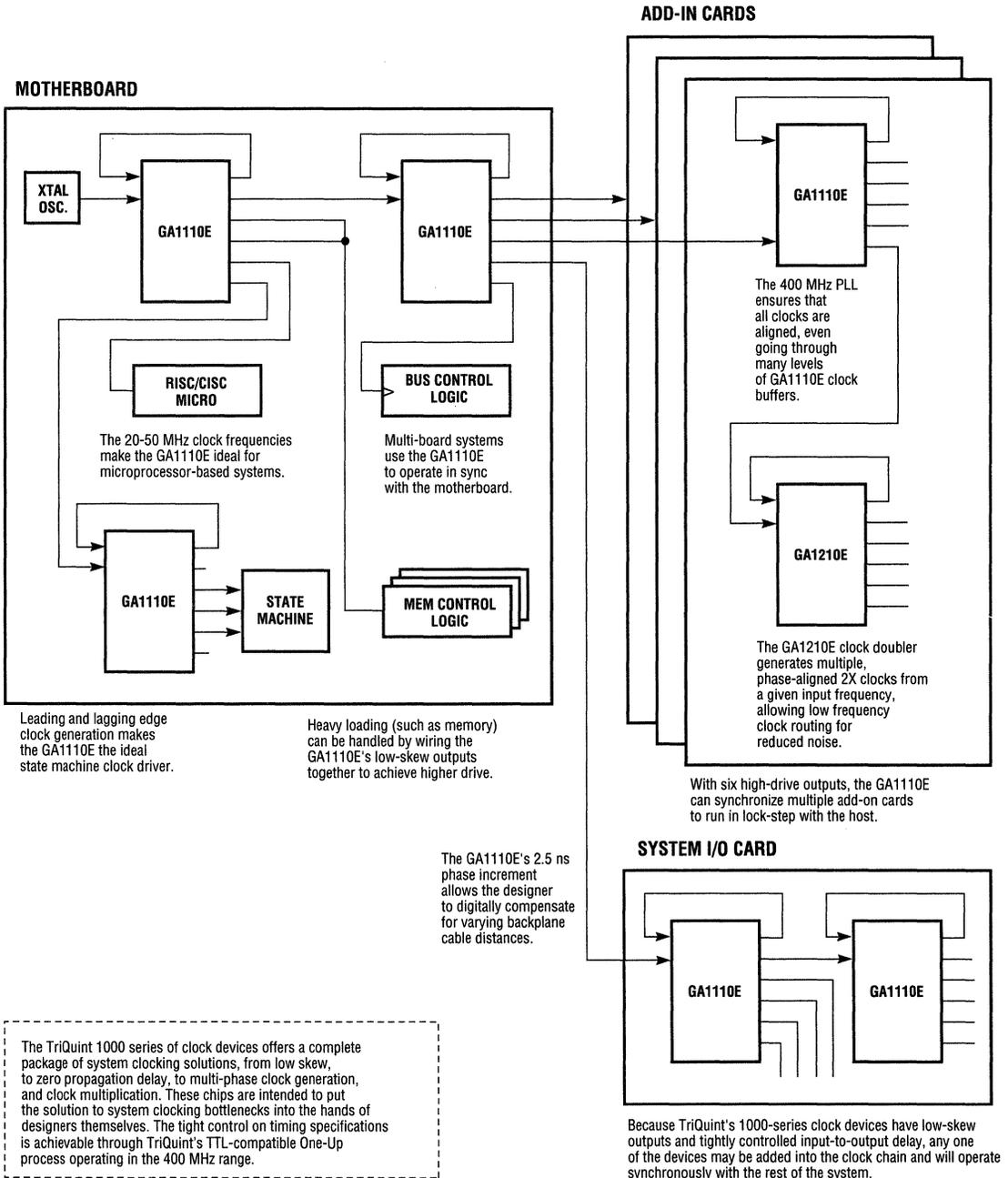
4) Trace Delay / Loading Compensation

System designers often rely on various board layout techniques to compensate for signals driving different distances and/or loads.

- The GA1110E can selectively “place” clock edges ahead or behind in 2.5 ns increments to compensate for severe mismatches.
- Because the output skew is tightly controlled, outputs of the same phase can be wired together to increase drive capability on heavily loaded clock signals.

GA110E

Figure 10. System Clocking Solutions



The TriQuint 1000 series of clock devices offers a complete package of system clocking solutions, from low skew, to zero propagation delay, to multi-phase clock generation, and clock multiplication. These chips are intended to put the solution to system clocking bottlenecks into the hands of designers themselves. The tight control on timing specifications is achievable through TriQuint's TTL-compatible One-Up process operating in the 400 MHz range.

Absolute Maximum Ratings

Storage temperature	-65 °C to +150 °C
Ambient temperature with power applied	-55 °C to +125 °C
Supply voltage to ground potential	-0.5 V to +7.0 V
DC input voltage	-0.5 V to +(V _{DD} + 0.5)
DC input current	-30 mA to +5 mA

DC Characteristics (Supply voltage: +5 V ± 5% Ambient temp: 0 °C to +70 °C)

Symbol	Description	Test Conditions	Min	Limits ¹		Unit
				Typ	Max	
V _{OH}	Output HIGH voltage	V _{DD} = Min I _{OH} = -24 mA V _{IN} = V _{IH} or V _{IL}	2.4	3.55		V
V _{OL}	Output LOW voltage	V _{DD} = Min I _{OL} = 24 mA V _{IN} = V _{IH} or V _{IL}		0.23	0.5	V
V _{IH} ²	Input HIGH level	Guaranteed input logical HIGH Voltage for all inputs	2.0			V
V _{IL} ²	Input LOW level	Guaranteed input logical LOW Voltage for all inputs			0.8	V
I _{IL}	Input LOW current	V _{DD} = Max V _{IN} = 0.40 V		-210	-400	μA
I _{IH}	Input HIGH current	V _{DD} = Max V _{IN} = 2.7 V		0	25	μA
I _I	Input HIGH current	V _{DD} = Max V _{IN} = 5.5 V		2	1000	μA
I _{SC} ³	Output short-circuit current	V _{DD} = Max V _{OUT} = 0.5 V		-80		mA
I _{DD}	Power supply current	V _{DD} = Max		130	160	mA
V _I	Input clamp voltage	V _{DD} = Min I _{IN} = -18 mA		-0.62	-1.2	V
I _{OLD}	Dynamic switching current	V _{DD} = Max V _{OLD} = 1.5 V		70		mA
I _{OHD}		V _{DD} = Max V _{OHD} = 1.5 V		-80		mA

Capacitance⁴

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
C _{IN}	Input capacitance	V _{IN} = 2.0 V at f = 1 MHz		6		pF
C _{OUT}	Output capacitance	V _{OUT} = 2.0 V at f = 1 MHz		9		pF

- Notes:
1. Typical limits are at V_{DD} = 5.0 V and T_A = 25 °C.
 2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
 3. No more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} has been chosen to avoid test problems caused by tester ground degradation.
 4. These parameters are not 100% tested, but are periodically sampled.

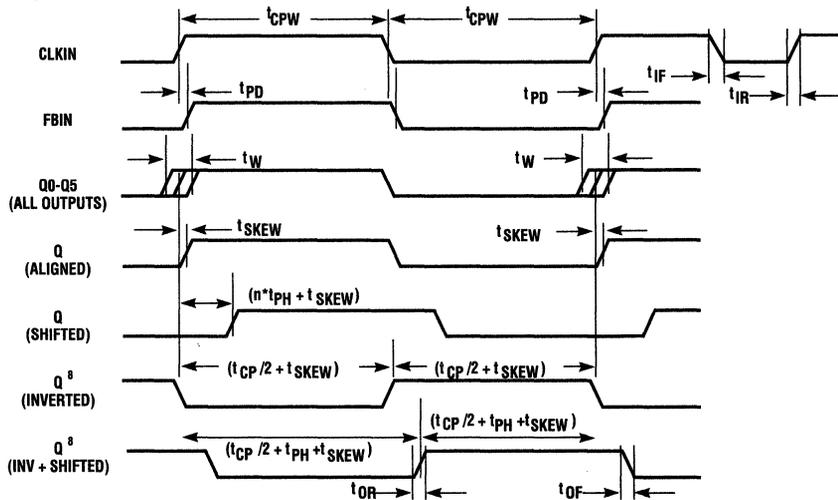
GA110E

AC Characteristics (Supply voltage: +5 V ± 5%; Ambient temp: 0 °C to 70 °C)

Description	-50			-40			-33			-25			-20			Unit
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
F_{IN} CLKIN frequency ¹	—	50	—	—	40	—	—	33	—	—	25	—	—	20	—	MHz
t_{CP} CLKIN period	—	20	—	—	25	—	—	30	—	—	40	—	—	50	—	ns
t_{CPW} CLKIN pulse width	5	10	—	6.25	12.5	—	7.5	15	—	10	20	—	12.5	25	—	ns
t_{IR}, t_{IF} Input rise/fall time (20 – 80%)	—	—	3.0	—	—	3.0	—	—	3.0	—	—	3.0	—	—	3.0	ns
t_{OR}, t_{OF} Output rise/fall time (80 – 20%)	—	1.0	3.0	—	1.0	3.0	—	1.0	3.0	—	1.0	3.0	—	1.0	3.0	ns
t_R Output rise time (0.8 V to 2.0 V)	—	0.5	1.5	—	0.5	1.5	—	0.5	1.5	—	0.5	1.5	—	0.5	1.5	ns
t_{PD} CLKIN \uparrow to FBIN \downarrow ²	—	± 250	±1000	—	± 250	±1000	—	± 250	±1000	—	± 250	±1000	—	± 250	±1000	ps
t_{SKEW} Output Skew ³	—	± 250	± 500	—	± 250	± 500	—	± 250	± 500	—	± 250	± 500	—	± 250	± 500	ps
t_W Output Window ⁴	—	0.5	1.0	—	0.5	1.0	—	0.5	1.0	—	0.5	1.0	—	0.5	1.0	ns
t_{PH} Phase-shift Increment ⁵	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	ns
t_{CYC} Duty-cycle Variation ⁶	—	1.0	—	—	1.0	—	—	1.0	—	—	1.0	—	—	1.0	—	ns
t_{SYNC} Synchronization Time ⁷	—	200	500	—	200	500	—	200	500	—	200	500	—	200	500	μs

Note: All AC specifications are measured with a 75 Ω transmission line load terminated with 75 Ω to 1.5 V. The skew specifications are guaranteed for equal loading at each output.

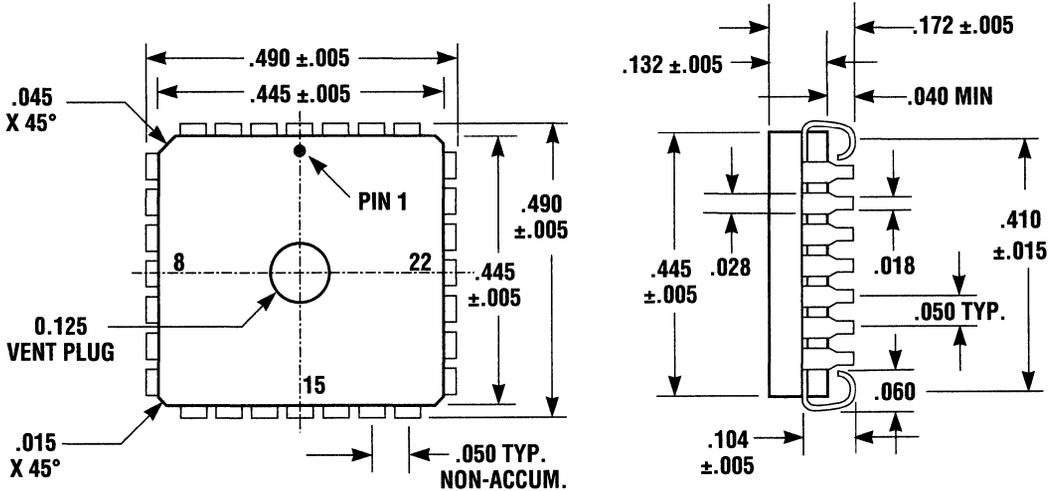
Figure 11. Switching Waveforms



- Notes:
1. The max, min range on CLKIN frequency is ± 5%.
 2. The PLL maintains alignment of CLKIN and FBIN at all times. This specification applies to the rising edge only because the input duty cycle can vary while the output duty cycle is typically 50/50.
 3. The output skew is measured from the middle of the output window. The maximum skew is guaranteed across all voltages and temperatures.
 4. t_W specifies the width of the window in which all outputs will switch.
 5. This increment is a digitally generated fraction of t_{CP} and will not vary with voltage or temperature. The specifications for t_{PH} given in the table are for 50, 40, 33, 25, and 20 MHz operation, respectively.
 6. This specification represents the deviation from 50/50 on the outputs; it is sampled periodically but is not guaranteed.
 7. t_{SYNC} is the time required for the PLL to synchronize; this assumes the presence of a CLKIN signal and a connection from one of the outputs to FBIN.
 8. All specifications for inverted outputs apply to the rising edge only.
 9. The device is AC tested only in the $S0 = S1 = 0$ mode.

28-Pin MQuad J-Leaded Package Mechanical Specifications

(All dimensions are in inches)



28-Pin MQuad Pin Description

Pin #	Pin Name	Description	I/O
1	N/C	No Connect	—
2	GND	Ground	—
3	T0	Test 0	I ¹
4	N/C	No Connect	—
5	N/C	No Connect	—
6	S0	Select 0	I
7	S1	Select 1	I
8	N/C	No Connect	—
9	FBIN	Feedback In	I
10	CLKIN	System Clock	I
11	N/C	No Connect	—
12	N/C	No Connect	—
13	T1	Test 1	I ¹
14	GND	Ground	—

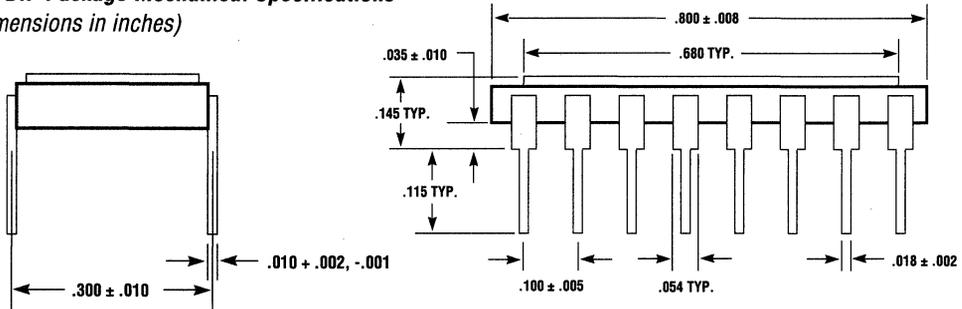
Pin #	Pin Name	Description	I/O
15	N/C	No Connect	—
16VDD	+5 V	—	—
17	Q0	Output Clock 0	O
18	N/C	No Connect	—
19	N/C	No Connect	—
20	Q1	Output Clock 1	O
21	Q2	Output Clock 2	O
22	Q3	Output Clock 3	O
23	Q4	Output Clock 4	O
24	Q5	Output Clock 5	O
25	N/C	No Connect	—
26	N/C	No Connect	—
27	VDD	+5 V	—
28	VDD	+5 V	—

Note: 1. For normal operation, T0 is GND and T1 is V_{DD} or N/C (No Connect). For Test Mode, T0 is HIGH and T1 is Clock Pulse(s).

GA110E

16-Pin DIP Package Mechanical Specifications

(All dimensions in inches)



16-Pin DIP Pin Description

Pin #	Pin Name	Description	I/O
1	GND	Ground	—
2	T0	Test 0	I ¹
3	S0	Select 0	I
4	S1	Select 1	I
5	FBIN	Feedback In	I
6	CLKIN	System Clock	I
7	T1	Test 1	I ¹
8	VDD	+5 V	—

Pin #	Pin Name	Description	I/O
9	GND	Ground	—
10	Q0	Output Clock 0	O
11	Q1	Output Clock 1	O
12	Q2	Output Clock 2	O
13	Q3	Output Clock 3	O
14	Q4	Output Clock 4	O
15	Q5	Output Clock 5	O
16	VDD	+5 V	—

Note: 1. For normal operation, T0 is GND and T1 is V_{DD} or N/C. For Test Mode, T0 is HIGH and T1 is Clock Pulse(s).

Ordering Information

To order, please specify as below shown:

GA110E - nn p C

Input Frequency

- 20 – 20 MHz input
- 25 – 25 MHz input
- 33 – 33 MHz input
- 40 – 40 MHz input
- 50 – 50 MHz input

Temperature

C – Commercial

Package

- S – 16-Pin DIP (side-brazed)
- M – 28-Pin MQuad Surface-Mount

For latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com

Tel: (503) 615-9000

Email: sales@tqs.com

Fax: (503) 615-8900

For technical questions and additional information on specific applications:

Email: applications@tqs.com

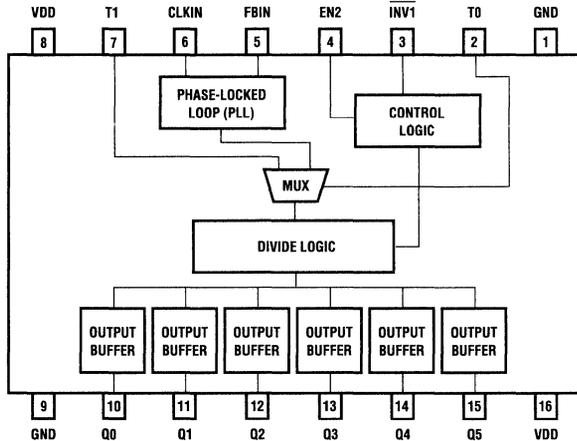
The information provided herein is believed to be reliable; TriQuint assumes no liability for inaccuracies or omissions. TriQuint assumes no responsibility for the use of this information, and all such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. TriQuint does not authorize or warrant any TriQuint product for use in life-support devices and/or systems.

Copyright © 1997 TriQuint Semiconductor, Inc. All rights reserved.

Revision 1.0.A October 1997



Figure 1. Block Diagram



TriQuint's GA1210E is a low-skew TTL-level clock doubler chip. It produces multiple clock outputs, at precisely 2X the input frequency, which are all phase-aligned to a periodic clock input signal. The GA1210E can generate clocks up to 100 MHz, making it an ideal solution for high-speed clock generation and routing.

The GA1210E guarantees precise clock control. The delay through the part is typically ± 250 ps. Skew at all six outputs is maintained to ± 250 ps, typically. When used with TriQuint's GA1110E multi-phase low-skew buffer, a complete system clocking solution can be achieved.

The capability to double clock signals while maintaining tight control over the phase and frequency of the output clocks is accomplished with the use of a 400 MHz internal phase-locked loop (PLL). By feeding back one of the 1X frequency output clocks (to FBIN), the on-chip PLL can continuously maintain synchronization between the input clock (CLKIN) and all six outputs. Any drift or variation in the system clock will be matched and tracked at the six outputs of the GA1210E.

The GA1210E offers several different configurations to accommodate the designer's high-speed clocking requirements. In addition to providing 2X outputs at 40–100 MHz frequencies, the GA1210E can also be configured to generate non-overlapping two-phase clocks. The combination of high speed and a selectable phase capability makes it ideal for clocking state machine and pipeline logic.

GA1210E

Clock Doubler / Two-Phase Generator

Features

- 2X clock multiple generator
- Two-phase clock generator
- Zero propagation delay
- Output skew controlled to ± 250 ps (typ) ± 500 ps (max)
- Available in 20, 25, 33, 40 and 50 MHz versions
- High-drive, symmetric TTL-compatible outputs with rise time of 1.0 ns
- Self-contained on-chip 400 MHz phase-locked loop (PLL)
- Special test mode
- 130 mA operating current (typ), 160 mA (max)
- Standard 16-pin DIP and 28-pin surface-mount packages

GA1210E

The GA1210E is fabricated using TriQuint's One-Up™ gallium arsenide technology to achieve precise timing control and to guarantee 100% TTL compatibility. The 20, 25, 33, 40, and 50 MHz input frequencies make this device ideal for high-speed clock generation and skew control in high-performance RISC- and CISC-based systems.

Functional Description

The GA1210E TTL-level clock doubler and two-phase generator chip is capable of generating multiple 2X outputs from a periodic clock input. Two control pins, EN2 and $\overline{\text{INV1}}$, provide additional flexibility by selecting two-phase and inverted clocks, respectively.

Table 1 enumerates the four available sets of output clock configurations generated by the GA1210E. The first two columns represent the signal levels for the two control signals. EN2 is an active-HIGH signal which enables the two-phase clocking on outputs Q4 and Q5. $\overline{\text{INV1}}$ is an active-LOW signal which inverts the Q1 output to provide a $\overline{1X}$ clock output. The six columns specify the resulting waveforms on each output; they are shown in detail in Figure 4. Specifications for the phase and skew parameters associated with the output clocks are listed in the AC Characteristics table.

The GA1210E's primary function is to offer precisely phase-aligned, low-skew 2X versions of the CLKIN input. Since the 2X clocks are all synchronous to the input, high-frequency clocks can be generated locally. This relieves the difficulty of routing high-frequency clocks on a board or across a backplane. They can also be cascaded with other GA1210E devices to generate synchronous 4X clocks.

The GA1210E also has the capability to generate non-overlapping two-phase clocks. By setting the EN2 pin HIGH, two-phase clocks are generated at outputs Q4 and Q5. This is ideal for state machines and other logic structures which can be optimized through two-phase clocking. The two-phase clocks are synchronous to the remaining outputs at 1X and 2X frequencies, providing maximum flexibility in board- and system-level clocking solutions.

In all configurations, the 1X clock must be fed back, either directly or indirectly, to the FBIN input, enabling the on-chip PLL to maintain phase and frequency synchronization.

Multiple-Chip Applications

Because of the tight input-output phase control, the GA1210E can be easily cascaded to build low-skew clock chains and clock trees. The generation and distribution of high-speed clocks can be accomplished with minimal skew allowance, permitting the system designer to obtain maximum performance from the microprocessor and other high-speed circuits in their designs. When combined with TriQuint's GA1110E low-skew, multi-phase clock buffer, a complete system clocking solution can be achieved. See Figure 5(Typical Applications).

Breaking the Feedback Loop

There is no requirement that the external feedback connection be a direct hardwire from an output pin to the FBIN pin. So long as the signal at FBIN is derived directly from the Q0 output pin and maintains its frequency, additional logic incorporating any delay whatsoever can be accommodated. The internal phase-

locked loop will adjust the output clocks on the GA1210E to ensure continuous phase alignment between the FBIN and CLKIN signals. This feature is extremely valuable in synchronizing ASICs to the system clock.

Caution: The signal at FBIN must be continuous (i.e. not a gated or conditional signal), and must be derived directly from one of the GA1210E's 1X outputs.

Power-Up/Reset Synchronization

The GA1210E utilizes on-chip phase-locked loop technology to maintain synchronization between inputs and outputs. Whenever the device is powered up, or the system clock (CLKIN) is reset, the phase-locked loop requires a synchronization time (t_{SYNC}) before lock is achieved. The maximum time required is specified in the AC Characteristics table.

For lock to occur, the Q0 output must always be connected (either directly or through additional ICs) to the FBIN input.

Table 1. Configuration Table

EN2	INV1	Q0	Q1	Q2	Q3	Q4	Q5
0	0	1X	1X	2X	2X	2X	2X
0	1	1X	1X	2X	2X	2X	2X
1	0	1X	1X	2X	2X	j1	j2
1	1	1X	1X	2X	2X	j1	j2

- Notes:
- 1X: The output clock is a phase-aligned 1X copy of the CLKIN signal.
 - 1X: The output clock is a 1X copy of CLKIN, 180 ° out of phase (i.e., inverted).
 - 2X: The output clock is a phase-aligned 2X frequency of the CLKIN signal.
 - j1, j2: The outputs are the first and second of two phases, synchronous to CLKIN.

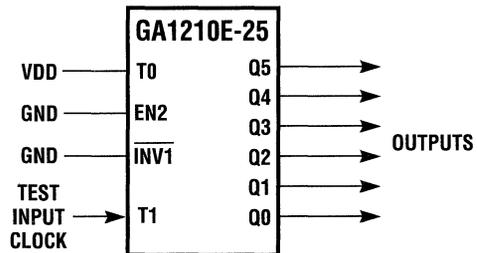
GA1210E Test Mode

The GA1210E has a test mode which can be enabled if the test pin T0 is HIGH. Under that condition, the clock signal from the test pin T1 is used as the clock input to the configuration logic, instead of the output from the PLL. This mode can be used to test only the internal state machine and associated logic. Each speed type and configuration has a unique signature which is present at the output after “n” number of input clock pulses. (For the GA1210E-25 there will be one output clock cycle for every 16 input clock cycles from t_0 .) Figures 2 and 3 show the test mode and associated timing for Configuration 1.

When powered up, the Q0 through Q5 outputs can be in any state. It can take up to 16 clocks to get the outputs to the predetermined state at t_0 . The number of clock cycles at input T1 required for one output clock cycle is 20 for GA1210E-20, 12 for the GA1210E-33, 8 for the GA1210E-40 and 8 for the GA1210E-50. The test input clock at T1 can either be used to single-step the outputs, or it can be clocked at rates up to 200 MHz. Please note that for the normal mode of operation, T0 is LOW (GND) and T1 is HIGH (V_{DD}) or No Connect (N/C).

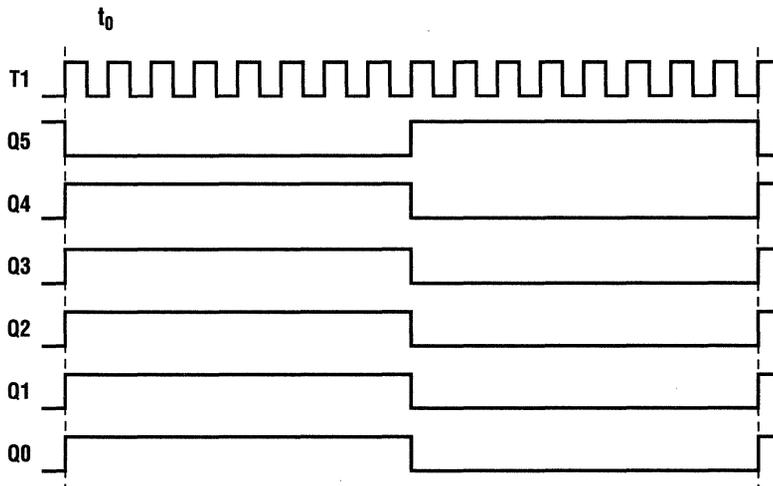
SYSTEM TIMING PRODUCTS

Figure 2. Test Mode for the GA1210E-25



GA1210E

Figure 3. GA1210E-25 Timing in Test Mode
(Configuration 1)

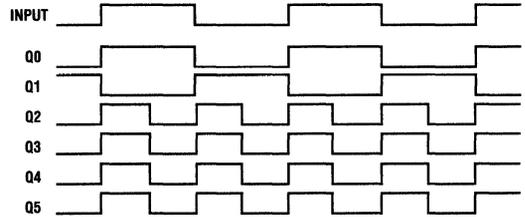
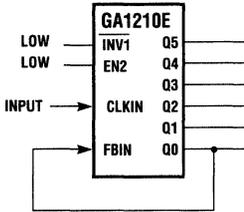


Note: The above timing applies to the case when $S1 = S0 = 0$ and $T0 = 1$ (test mode).

Figure 4. Possible Configurations

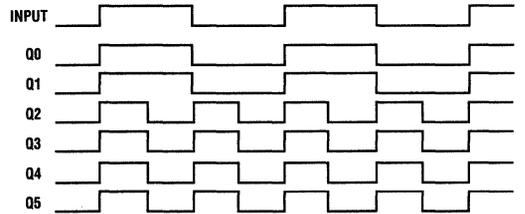
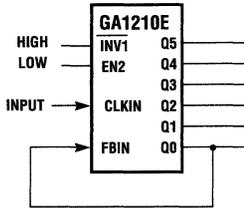
Configuration 1

INV1 = 0
EN2 = 0
FBIN = Q0



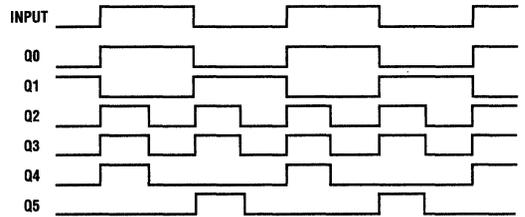
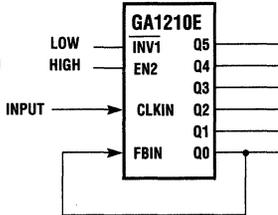
Configuration 2

INV1 = 1
EN2 = 0
FBIN = Q0



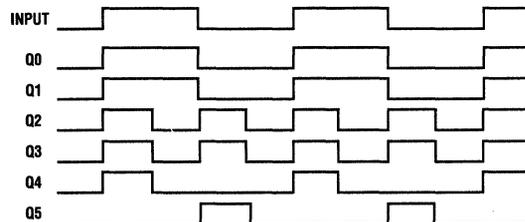
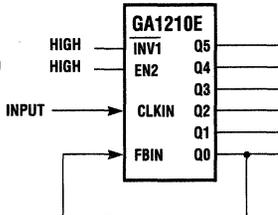
Configuration 3

INV1 = 0
EN2 = 1
FBIN = Q0



Configuration 4

INV1 = 1
EN2 = 1
FBIN = Q0



SYSTEM TIMING PRODUCTS

Typical Applications

The GA1210E is designed to satisfy a wide range of system clocking requirements. It provides an ideal companion to the GA1110E multi-phase clock generator. Several application examples are illustrated below.

1) High-Frequency Low-Skew Clock Generation

The GA1210E's basic capability is the generation of multiple phase-aligned, low-skew clocks at 2X the input frequency.

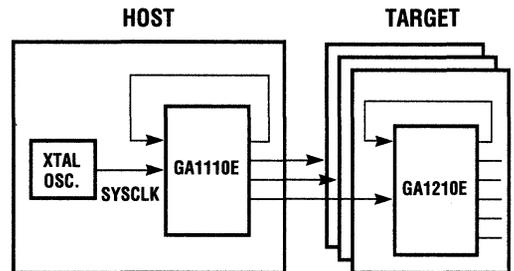
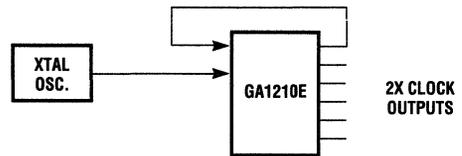
- *The GA1210E guarantees low skew among all clocks in the system by controlling both the input-to-output delay and the skew among all six clock outputs.*

2) Board-to-Board Clock Synchronization

Many computing systems today consist of multiple boards and cards designed to run synchronously. The skew associated with routing clocks across a backplane presents a major hurdle to maximizing system performance.

- *The tightly controlled input/output delay of the GA1210E ensures all boards in the system are running synchronously.*
- *The GA1210E can be used with the GA1110E to route lower frequency clocks across a backplane; the low-frequency signal is then doubled on the target boards, enabling them to run synchronously with the host board.*

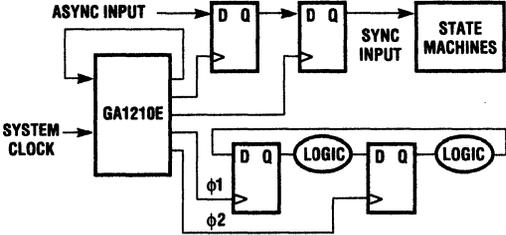
Figure 5. Typical Applications



3) Two-Phase Clocking

The GA1210E can be configured to generate synchronous two-phase clocks.

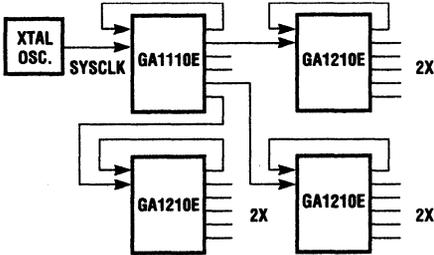
- *The two-phase clocks can be used for pipelined logic forms.*
- *Synchronous two-phase clocks can be used to eliminate metastability concerns by synchronizing asynchronous system inputs to the system clock.*



4) Clock Trees and Clock Chains

Used alone or with the GA1110E, the GA1210E distributes multiple copies of high-frequency clocks to the various blocks of a system. All of the clock signals at all of the destinations will run synchronously.

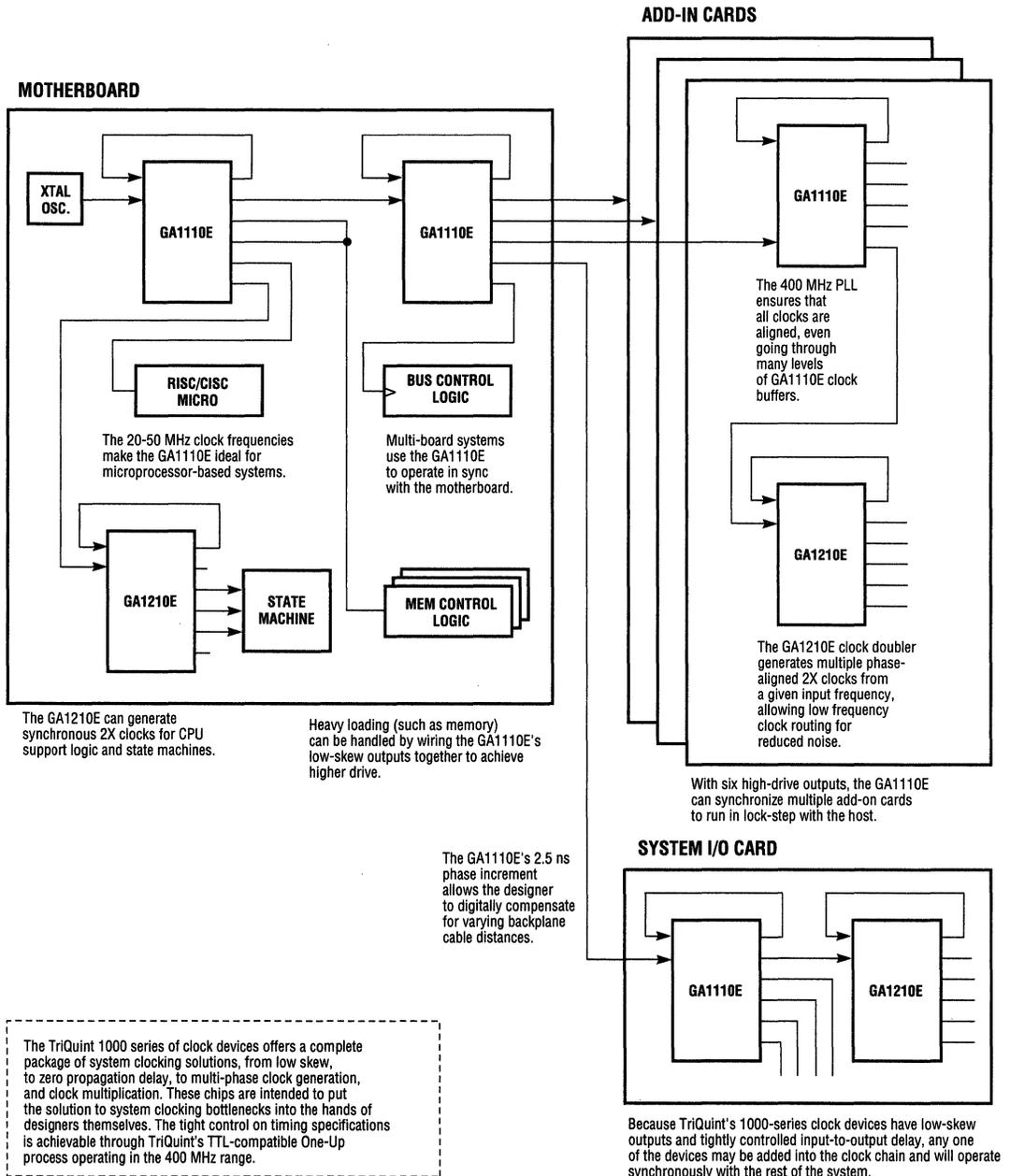
- *The controlled input-to-output delay allows long clock chains and trees*



SYSTEM TIMING PRODUCTS

GA1210E

Figure 6. System Clocking Solutions



Absolute Maximum Ratings

Storage temperature	-65 °C to +150 °C
Ambient temperature with power applied	-55 °C to +125 °C
Supply voltage to ground potential	-0.5 V to +7.0 V
DC input voltage	-0.5 V to +(V _{DD} + 0.5)
DC input current	-30 mA to +5 mA

DC Characteristics (Supply voltage: +5 V ± 5% Ambient temp: 0 °C to +70 °C)

Symbol	Description	Test Conditions	Min	Limits ¹		Unit
				Typ	Max	
V _{OH}	Output HIGH voltage	V _{DD} = Min I _{OH} = -24 mA V _{IN} = V _{IH} or V _{IL}	2.4	3.55		V
V _{OL}	Output LOW voltage	V _{DD} = Min I _{OL} = 24 mA V _{IN} = V _{IH} or V _{IL}		0.23	0.5	V
V _{IH} ²	Input HIGH level	Guaranteed input logical HIGH Voltage for all inputs	2.0			V
V _{IL} ²	Input LOW level	Guaranteed input logical LOW Voltage for all inputs			0.8	V
I _{IL}	Input LOW current	V _{DD} = Max V _{IN} = 0.40 V		-210	-400	μA
I _{IH}	Input HIGH current	V _{DD} = Max V _{IN} = 2.7 V		0	25	μA
I _I	Input HIGH current	V _{DD} = Max V _{IN} = 5.5 V		2	1000	μA
I _{SC} ³	Output short-circuit current	V _{DD} = Max V _{OUT} = 0.5 V		-80		mA
I _{DD}	Power supply current	V _{DD} = Max		130	160	mA
V _I	Input clamp voltage	V _{DD} = Min I _{IN} = -18 mA		-0.62	-1.2	V
I _{OLD}	Dynamic switching current	V _{DD} = Max V _{OLD} = 1.5 V		70		mA
I _{OH}		V _{DD} = Max V _{OH} = 1.5 V		-80		mA

Capacitance ⁴

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
C _{IN}	Input capacitance	V _{IN} = 2.0 V at f = 1 MHz		6		pF
C _{OUT}	Output capacitance	V _{OUT} = 2.0 V at f = 1 MHz		9		pF

- Notes:
1. Typical limits are at V_{DD} = 5.0 V and T_A = 25 °C.
 2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
 3. No more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} has been chosen to avoid test problems caused by tester ground degradation.
 4. These parameters are not 100% tested, but are periodically sampled.

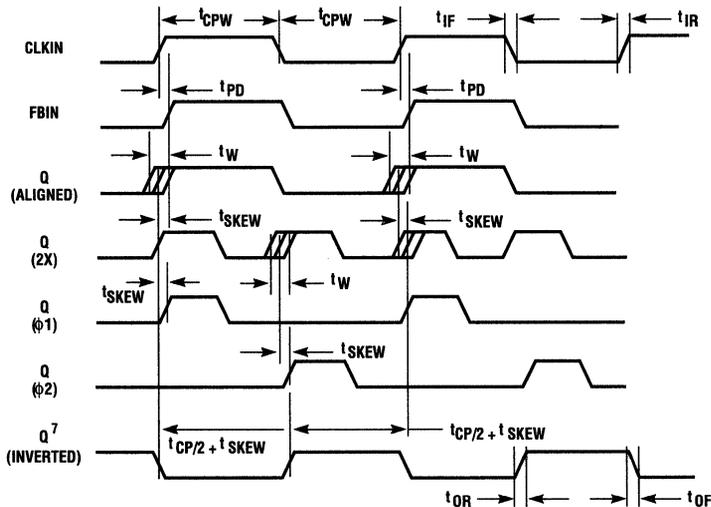
GA1210E

AC Characteristics (Supply voltage: +5 V ± 5%; Ambient temp: 0 °C to 70 °C)

Symbol	Description	-50			-40			-33			-25			-20			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
F_{IN}	CLKIN frequency ¹	—	50	—	—	40	—	—	33	—	—	25	—	—	20	—	MHz
t_{CP}	CLKIN period	—	20	—	—	25	—	—	30	—	—	40	—	—	50	—	ns
t_{CPW}	CLKIN pulse width	5	10	—	6.25	12.5	—	7.5	15	—	10	20	—	12.5	25	—	ns
t_{IR}, t_{IF}	Input rise/fall time (20 – 80%)	—	—	3.0	—	—	3.0	—	—	3.0	—	—	3.0	—	—	3.0	ns
t_{OR}, t_{OF}	Output rise/fall time (80 – 20%)	—	1.0	3.0	—	1.0	3.0	—	1.0	3.0	—	1.0	3.0	—	1.0	3.0	ns
t_R	Output rise time (0.8 V to 2.0 V)	—	0.5	1.5	—	0.5	1.5	—	0.5	1.5	—	0.5	1.5	—	0.5	1.5	ns
t_{PD}	CLKIN \hat{I} to FBIN \hat{I} ²	—	±250	±1000	—	±250	±1000	—	±250	±1000	—	±250	±1000	—	±250	±1000	ps
t_{SKEW}	Output Skew ³	—	±250	±500	—	±250	±500	—	±250	±500	—	±250	±500	—	±250	±500	ps
t_W	Output Window ⁴	—	0.5	1.0	—	0.5	1.0	—	0.5	1.0	—	0.5	1.0	—	0.5	1.0	ns
t_{CYC}	Duty-cycle Variation ⁶	—	1.0	—	—	1.0	—	—	1.0	—	—	1.0	—	—	1.0	—	ns
t_{SYNC}	Synchronization Time ⁷	—	200	500	—	200	500	—	200	500	—	200	500	—	200	500	μs

Note: All AC specifications are measured with a 75 Ω transmission line load terminated with 75 Ω to 1.5 V. The skew specifications are guaranteed for equal loading at each output.

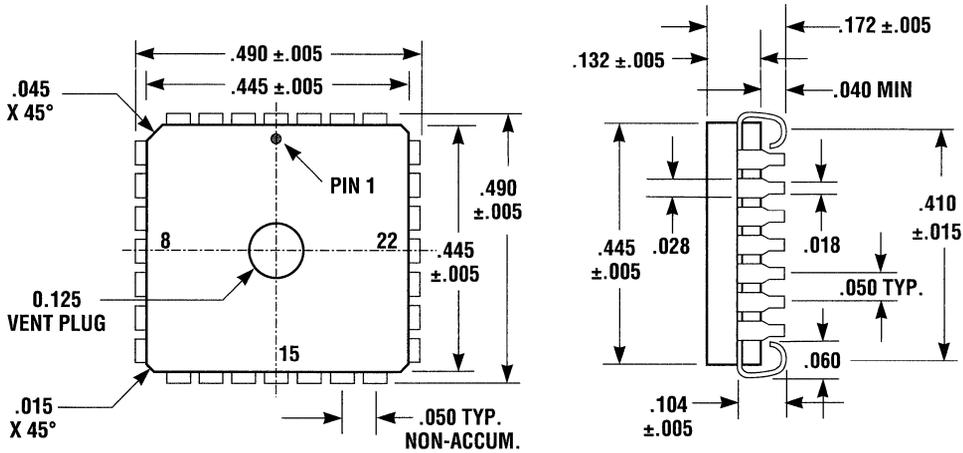
Figure 7. Switching Waveforms



- Notes:
1. The min, max range on CLKIN frequency is ±5%
 2. The PLL maintains alignment of CLKIN and FBIN at all times. This specification applies to the rising edge only because the input duty cycle can vary while the output duty cycle is typically 50/50.
 3. The output skew is measured from the middle of the output window. The maximum skew is guaranteed across all voltages and temperatures.
 4. t_W specifies the width of the window in which all outputs will switch.
 5. This specification represents the deviation from 50/50 on the outputs; it is sampled periodically but is not guaranteed.
 6. t_{SYNC} is the time required for the PLL to synchronize; this assumes the presence of a CLKIN signal and a connection from one of the outputs to FBIN.
 7. All specifications for inverted outputs apply to the rising edge only.
 8. The device is AC tested only in the EN2=0, INV1=1 mode.

28-Pin MQuad J-Leaded Package Mechanical Specifications

(All dimensions are in inches)



28-Pin MQuad Pin Description

Pin #	Pin Name	Description	I/O
1	N/C	No Connect	—
2	GND	Ground	—
3	T0	Test 0	I ¹
4	N/C	No Connect	—
5	N/C	No Connect	—
6	INV1	Inverted Clocks	I
7	EN2	2-Phase Clocks	I
8	N/C	No Connect	—
9	FBIN	Feedback In	I
10	CLKIN	System Clock	I
11	N/C	No Connect	—
12	N/C	No Connect	—
13	T1	Test 1	I ¹
14	GND	Ground	—

Pin #	Pin Name	Description	I/O
15	N/C	No Connect	—
16	VDD	+5 V	—
17	Q0	Output Clock 0	O
18	N/C	No Connect	—
19	N/C	No Connect	—
20	Q1	Output Clock 1	O
21	Q2	Output Clock 2	O
22	Q3	Output Clock 3	O
23	Q4	Output Clock 4	O
24	Q5	Output Clock 5	O
25	N/C	No Connect	—
26	N/C	No Connect	—
27	VDD	+5 V	—
28	VDD	+5 V	—

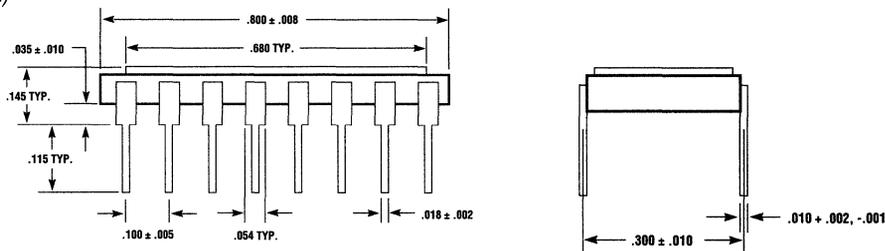
Note: 1. For normal operation, T0 is GND and T1 is V_{DD} or N/C (No Connect). For Test Mode, T0 is HIGH and T1 is Clock Pulse(s).

SYSTEM TIMING PRODUCTS

GA1210E

16-Pin DIP Package Mechanical Specifications

(All dimensions in inches)



16-Pin DIP Pin Description

Pin #	Pin Name	Description	I/O
1	GND	Ground	—
2	T0	Test 0	I ¹
3	INV1	Inverted Clock	I
4	EN2	2-Phase Clocks	I
5	FBIN	Feedback In	I
6	CLKIN	System Clock	I
7	T1	Test 1	I ¹
8	VDD	+5 V	—

Pin #	Pin Name	Description	I/O
9	GND	Ground	—
10	Q0	Output Clock 0	O
11	Q1	Output Clock 1	O
12	Q2	Output Clock 2	O
13	Q3	Output Clock 3	O
14	Q4	Output Clock 4	O
15	Q5	Output Clock 5	O
16	VDD	+5 V	—

Note: 1. For normal operation, T0 is GND and T1 is V_{DD} or N/C. For Test Mode, T0 is HIGH and T1 is Clock Pulse(s).

Ordering Information

To order, please specify as below shown:

GA1210E - nn P C

Input Frequency

- 20 – 20 MHz input
- 25 – 25 MHz input
- 33 – 33 MHz input
- 40 – 40 MHz input
- 50 – 50 MHz input

Temperature

C – Commercial

Package

- S – 16-Pin DIP (side-brazed)
- M – 28-Pin MQuad Surface-Mount

Additional Information

For latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com Tel: (503) 615-9000

Email: sales@tqs.com Fax: (503) 615-8900

For technical questions and additional information on specific applications:

Email: applications@tqs.com

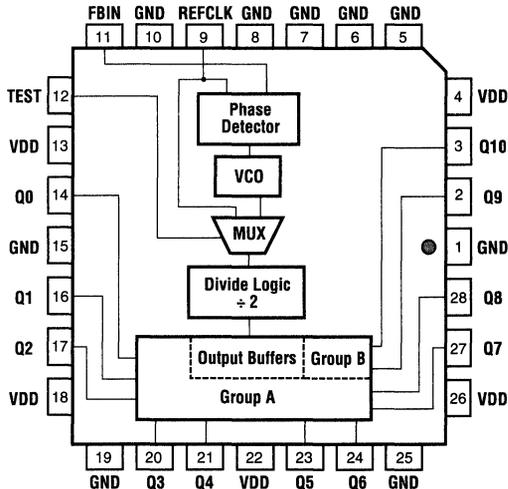
The information provided herein is believed to be reliable; TriQuint assumes no liability for inaccuracies or omissions. TriQuint assumes no responsibility for the use of this information, and all such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. TriQuint does not authorize or warrant any TriQuint product for use in life-support devices and/or systems.

Copyright © 1997 TriQuint Semiconductor, Inc. All rights reserved.

Revision 1.0.A October 1997



Figure 1. Block Diagram



TriQuint's TQ1089 is a configurable clock buffer which generates 11 outputs, operating over a wide range of frequencies from 65 MHz to 90 MHz and from 130 MHz to 180 MHz. The outputs are available at either 1x and 2x or at 1x and $\frac{1}{2}$ x the reference clock frequency, f_{REF} . When one of the Group A outputs (Q0–Q8) is used as feedback to the PLL, all Group A outputs will be at f_{REF} , and all Group B outputs (Q9, Q10) will be at $2x f_{REF}$. When one of the Group B outputs is used as feedback to the PLL, all Group A outputs will be at $\frac{1}{2} x f_{REF}$ and all Group B outputs will be at f_{REF} .

A very stable internal Phase-Locked Loop (PLL) provides low-jitter operation. This completely self-contained PLL requires no external capacitors or resistors. The PLL's Voltage-Controlled Oscillator (VCO) has a frequency range from 260 MHz to 360 MHz. By feeding back one of the output clocks to FBIN, the PLL continuously maintains frequency and phase synchronization between the reference clock (REFCLK) and each of the outputs.

TriQuint's patented output buffer design delivers a very low output-to-output skew of 150 ps (max). The TQ1089's symmetrical TTL outputs are capable of sourcing and sinking 30 mA.

TQ1089

11-Output Configurable Clock Buffer

Features

- Wide frequency range: 65 MHz to 90 MHz and 130 MHz to 180 MHz
- Output configurations: eight outputs at f_{REF} , two outputs at $2x f_{REF}$ OR nine outputs at $\frac{1}{2} x f_{REF}$, one output at f_{REF}
- Low output-to-output skew: 150 ps (max) within a group
- Near-zero propagation delay: $-350 \text{ ps} \pm 500 \text{ ps}$ (max) or $-350 \text{ ps} \pm 700 \text{ ps}$ (max)
- TTL-compatible with 30 mA output drive
- 28-pin J-lead surface-mount package
- Ideal for PowerPC™-based designs

Functional Description

The core of the TQ1089 is a Phase-Locked Loop (PLL) that continuously compares the reference clock (REFCLK) to the feedback clock (FBIN), maintaining a zero frequency difference between the two. Since one of the outputs is always connected to FBIN, the PLL keeps the propagation delay between the outputs and the reference clock within $-350 \text{ ps} \pm 500 \text{ ps}$ for the TQ1089-MC500, and within $-350 \text{ ps} \pm 700 \text{ ps}$ for the TQ1089-MC700.

The internal Voltage-Controlled Oscillator (VCO), has an operating range of 260 MHz to 360 MHz, as shown in Table 1. The combination of the VCO and the Divide Logic enables the TQ1089 to operate between 65 MHz and 90 MHz and from 130 MHz to 180 MHz.

In the test mode, the PLL is bypassed and REFCLK is connected directly to the Divide Logic block via the MUX, as shown in Figure 1. This mode is useful for debug and test purposes. The test mode is outlined in Table 2.

The maximum rise and fall time at the output pins is 1.4 ns. All outputs of the TQ1089 are TTL-compatible with 30 mA symmetric drive and a minimum V_{OH} of 2.4 V.

Power Up/Reset Synchronization

After power up or reset, the PLL requires time before it achieves synchronization lock. The maximum time required for synchronization (TSYNC) is 500 ms.

Table 1. Frequency Mode Selection

Test	Output Feedback	Mode	Reference Clock Frequency Range	Output Frequency Range	
				Group A: Q0-Q8	Group B: Q9, Q10
0	Group B	$\div 2$	130 MHz – 180 MHz	65 MHz – 90 MHz	130 MHz – 180 MHz
0	Group A	$\div 4$	65 MHz – 90 MHz	65 MHz – 90 MHz	130 MHz – 180 MHz

Table 2. Test Mode Selection

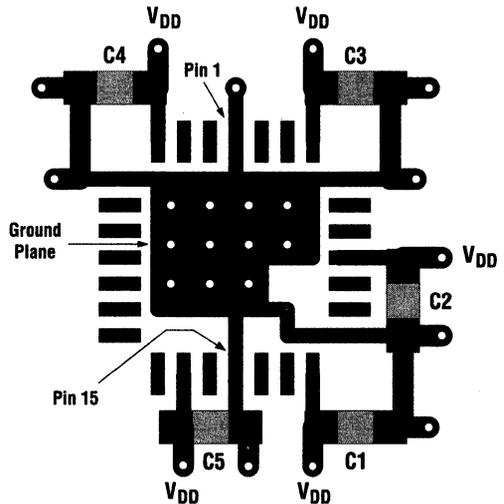
Test	Mode	Ref. Clock	Group A Outputs Q0-Q8	Group B Outputs Q9, Q10
1	$\div 2$	f_{REF}	$f_{REF} \div 4$	$f_{REF} \div 2$

Layout Guidelines

Multiple ground and power pins on the TQ1089 reduce ground bounce. Good layout techniques, however, are necessary to guarantee proper operation and to meet the specifications across the full operating range. TriQuint recommends bypassing each of the V_{DD} supply pins to the nearest ground pin, as close to the chip as possible.

Figure 2 shows the recommended power layout for the TQ1089. The bypass capacitors should be located on the same side of the board as the TQ1089. The V_{DD} traces connect to an inner-layer V_{DD} plane. All of the ground pins (GND) are connected to a small ground plane on the surface beneath the chip. Multiple through holes connect this small surface plane to an inner-layer ground plane. The capacitors (C1–C5) are 0.1 mF. TriQuint's test board uses X7R temperature-stable capacitors in 1206 SMD cases.

Figure 2. Top Layer Layout of Power Pins
(Approx. 3.3x)



TQ1089

Absolute Maximum Ratings ¹

Storage temperature	-65 °C to +150 °C
Ambient temperature with power applied ²	-55 °C to +100 °C
Supply voltage to ground potential	-0.5 V to +7.0 V
DC input voltage	-0.5 V to +(V _{DD} + 0.5)V
DC input current	-30 mA to +5 mA
Package thermal resistance (MQuad)	θ _{JA} = 45 °C/W
Die junction temperature	T _J = 150 °C

DC Characteristics

(V_{DD} = +5 V ± 5%, T_A = 0 °C to +70 °C)³

Symbol	Description	Test Conditions	Min	Limits ⁴		Unit
				Typ	Max	
V _{OHT}	Output HIGH voltage	V _{DD} = Min I _{OH} = -30 mA V _{IN} = V _{IH} or V _{IL}	2.4	3.4		V
V _{OHC}	Output HIGH voltage	V _{DD} = Min I _{OH} = -1 mA V _{IN} = V _{IH} or V _{IL}	3.2	4.1		V
V _{OL}	Output LOW voltage	V _{DD} = Min I _{OL} = 30 mA V _{IN} = V _{IH} or V _{IL}		0.27	0.5	V
V _{IH} ⁵	Input HIGH level	Guaranteed input logical HIGH Voltage for all Inputs	2.0			V
V _{IL} ⁵	Input LOW level	Guaranteed input logical LOW Voltage for all inputs			0.8	V
I _{IL}	Input LOW current	V _{DD} = Max V _{IN} = 0.40 V		-156	-400	µA
I _{IH}	Input HIGH current	V _{DD} = Max V _{IN} = 2.7 V		0	25	µA
I _I	Input HIGH current	V _{DD} = Max V _{IN} = 5.5 V		2	1000	µA
I _{DD5} ⁶	Power supply current	V _{DD} = Max		119	170	mA
V _I	Input clamp voltage	V _{DD} = Min I _{IN} = -18 mA		-0.70	-1.2	V

Capacitance

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
C _{IN} ^{3,7}	Input capacitance	V _{IN} = 2.0 V at f = 1 MHz		6		pF

Notes: 1. Exceeding these parameters may damage the device.

2. Maximum ambient temperature with device not switching and unloaded.

3. These values apply to both TQ1089-MC500 and TQ1089-MC700.

4. Typical limits are at V_{DD} = 5.0 V and T_A = 25 °C.

5. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.

6. This parameter is measured with device not switching and unloaded.

7. These parameters are not 100% tested, but are periodically sampled.

AC Characteristics

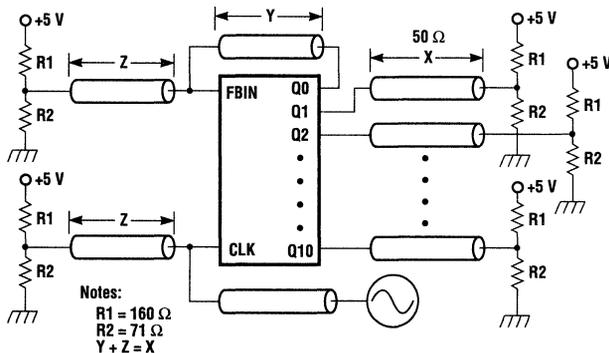
($V_{DD} = +5 V \pm 5\%$, $T_A = 0\text{ }^\circ\text{C to } +70\text{ }^\circ\text{C}$)

Symbol	Input Clock (REFCLK)	Test Conditions (Figure 3) ¹	Min	Typ	Max	Unit
t_{CPWH}	CLK pulse width HIGH	Figure 4	3	---	---	ns
t_{CPWL}	CLK pulse width LOW	Figure 4	3	---	---	ns
t_{IR}	Input rise time (0.8 V - 2.0V)		---	---	2.0	ns

Symbol	Output Clocks (Q0-Q10)	Test Conditions (Figure 3) ¹	Min	Typ	Max	Unit
t_{OR}, t_{OF}	Rise/fall time (0.8 V - 2.0V)	Figure 4	350	---	1400	ps
t_{PD1} ²	CLK \uparrow to FBIN \uparrow (TQ1089-MC500)	Figure 4	-850	-350	+150	ps
t_{PD2} ²	CLK \uparrow to FBIN \uparrow (TQ1089-MC700)	Figure 4	-1050	-350	+350	ps
t_{SKEW1} ³	Rise-rise, fall-fall (within group)	Figure 5	---	60	150	ps
t_{SKEW2} ³	Rise-rise, fall-fall (group-to-group, aligned)	Figure 6 (skew2 takes into account skew1)	---	75	350	ps
t_{SKEW3} ³	Rise-rise, fall-fall (group-to-group, non-aligned)	Figure 7 (skew3 takes into account skew1, 2)	---	---	650	ps
t_{SKEW4} ³	Rise-fall, fall-rise	Figure 8 (skew4 takes into account skew3)	---	---	1200	ps
t_{CYC} ⁴	Duty-cycle Variation	Figure 4	-1000	0	+1000	ps
t_{JP} ⁵	Period-to-Period Jitter	Figure 4	---	80	200	ps
t_{JR} ⁵	Random Jitter	Figure 4	---	190	400	ps
t_{SYNC} ⁶	Synchronization Time		---	10	500	μ s

- Notes:
1. All measurements are tested with a REFCLK having a rise time of 0.5 ns (0.8 V to 2.0 V).
 2. The PLL maintains alignment of CLK and FBIN at all times. This specification applies to the rising edge only because the input duty cycle can vary while the output duty cycle is typically 50/50. The delay t_{PD} is measured at the 1.5 V level between CLK and FBIN.
 3. Skew specifies the width of the window in which outputs switch, and is measured at 1.5 V.
 4. This specification represents the deviation from 50/50 on the outputs.
 5. Jitter specifications refer to peak-to-peak value. t_{JR} is the jitter on the output with respect to the reference clock. t_{JP} is the jitter on the output with respect to the output's previous rising edge.
 6. t_{SYNC} is the time required for the PLL to synchronize; this assumes the presence of a CLK signal and a connection from one of the outputs to FBIN.

Figure 3. AC Test Circuit



Switching Waveforms

Figure 4. General Timing

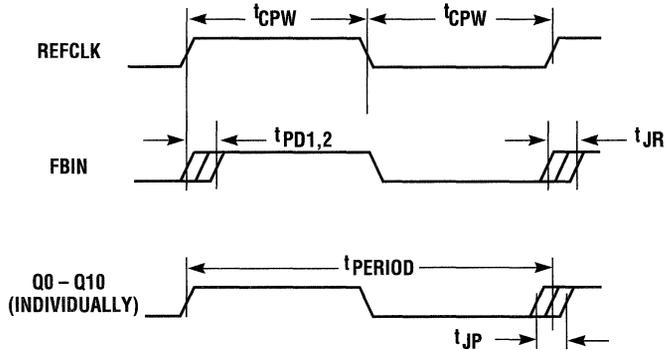


Figure 5. t_{SKEW1}

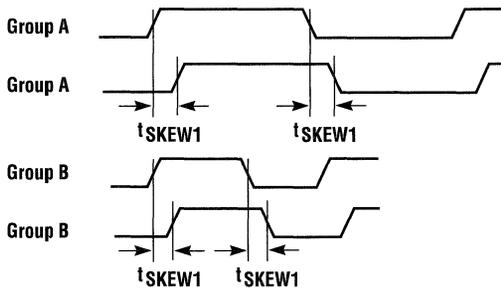


Figure 6. t_{SKEW2}

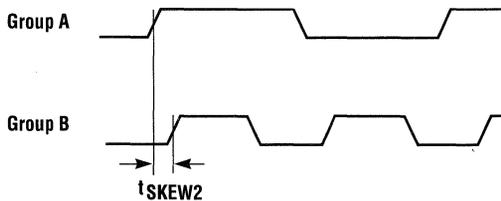


Figure 7. t_{SKEW3}

(For Group A Feedback)

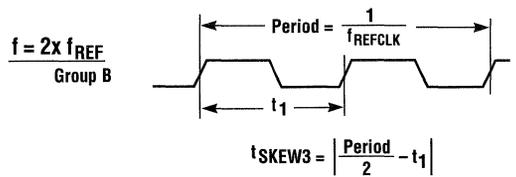
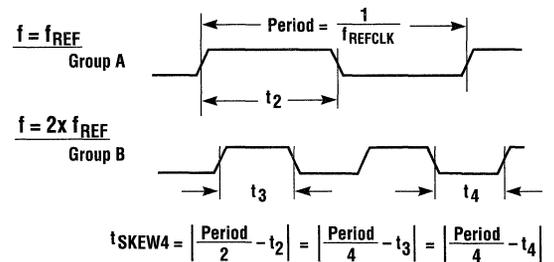
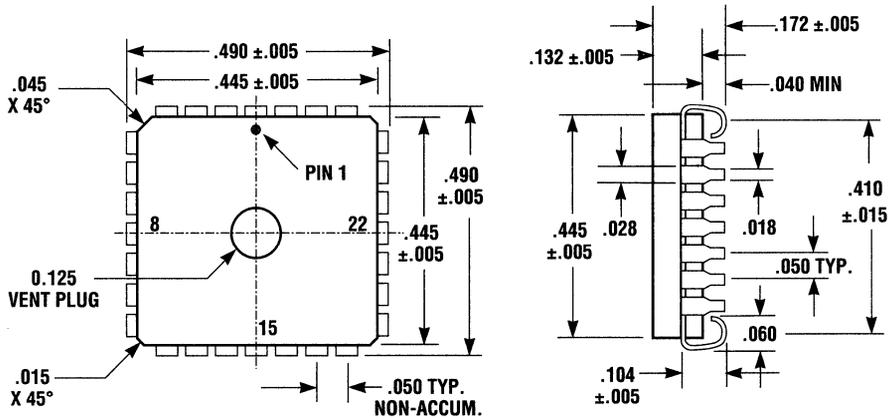


Figure 8. t_{SKEW4}



28-Pin MQuad J-Leaded Package Mechanical Specification

(All dimensions are in inches)



28-Pin MQuad Pin Description

Pin #	Pin Name	Description	I/O
1	GND	Ground	—
2	Q9	Output Clock 9 (B1)	0
3	Q10	Output Clock 10 (B2)	0
4	VDD	+5 V	—
5	GND	Ground	—
6	GND	Ground	—
7	GND	Ground	—
8	GND	Ground	—
9	REFCLK	Reference Clock	I
10	GND	Ground	—
11	FBIN	Feedback In	I
12	TEST	Test	I
13	VDD	+5 V	—
14	Q0	Output Clock 0 (A1)	0

Pin #	Pin Name	Description	I/O
15	GND	Ground	—
16	Q1	Output Clock 1 (A2)	0
17	Q2	Output Clock 2 (A3)	0
18	VDD	+5 V	—
19	GND	Ground	—
20	Q3	Output Clock 3 (A4)	0
21	Q4	Output Clock 4 (A5)	0
22	VDD	+5 V	—
23	Q5	Output Clock 5 (A6)	0
24	Q6	Output Clock 6 (A7)	0
25	GND	Ground	—
26	VDD	+5 V	—
27	Q7	Output Clock 7 (A8)	0
28	Q8	Output Clock 8 (A9)	0

SYSTEM TIMING PRODUCTS

Output Characteristics

The IV characteristics, transition times, package characteristics, device and bond wire characteristics for the TQ1089 are described in Tables 4 through 9 and Figures 9 through 11.

These output characteristics are provided for modelling purposes only. TriQuint does not guarantee the information in these tables and figures.

Figure 9. I_{OH} vs. V_{OH}

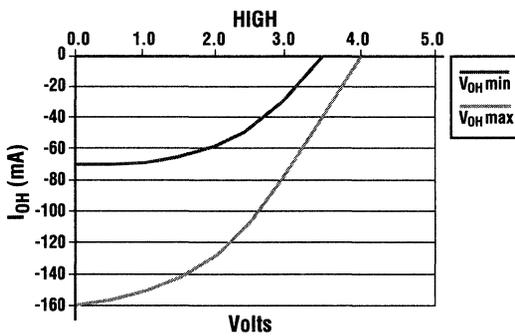


Figure 10. I_{OL} vs. V_{OL}

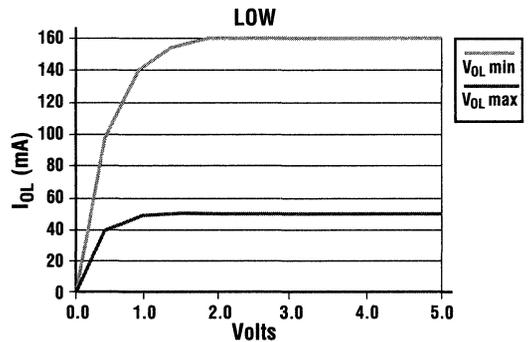


Table 4. I_{OH} vs. V_{OH}

V_{OH}	$I_{OH\ min}$ (mA)	$I_{OH\ max}$ (mA)
0.0	-70	-160
0.5	-70	-157
1.0	-68	-152
1.5	-65	-142
2.0	-59	-130
2.5	-48	-106
3.0	-29	-79
3.5	0	-42
4.0	0	0
4.5	0	0
5.0	0	0
5.5	40	120
6.0	90	265
6.5	115	350
7.0	135	410
7.5	145	435

Table 5. I_{OL} vs. V_{OL}

V_{OL}	$I_{OL\ min}$ (mA)	$I_{OL\ max}$ (mA)
-2.5	-145	-435
-2.0	-135	-410
-1.5	-115	-350
-1.0	-90	-265
-0.5	-40	-120
0.0	0	0
0.5	37	97
1.0	49	140
1.5	53	155
2.0	54	157
2.5	54	159
3.0	54	160
3.5	54	160
4.0	54	160
4.5	54	160
5.0	54	160
10.0	54	160

Table 6. Above- V_{DD} and Below-Ground Characteristics

Diode to GND		Diode Stack to VDD	
V	I (mA)	V	I (mA)
0.0	0	5.0	0
-0.4	0	5.4	0
-0.5	0	5.5	0
-0.6	-5	5.6	5
-0.7	-15	5.7	15
-0.8	-35	5.8	35
-0.9	-55	5.9	55
-1.0	-75	6.0	75
-2.0	-300	7.0	300
-2.5	-350	7.5	350
-3.0	-360	8.0	360

Note: TriQuint does not guarantee diode operation for purposes other than ESD protection.

Figure 11. Output Model

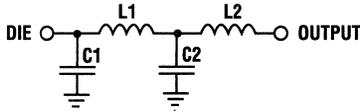


Table 7. Device and Bond-Wire Characteristics (Estimated)

L1	C1
2 nH	10 pF

Table 8. 28-Pin MQuad Package Characteristics

L2	C2
1.85 nH	0.40 pF

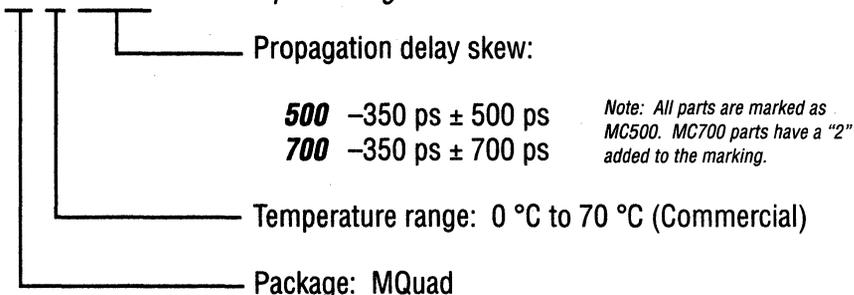
Table 9. Rise and Fall Times (Into 0 pF, 50 Ohms to 1.5 V)

Time (ns)	T_R min (V)	T_R max (V)	T_F min (V)	T_F max (V)
0.0	0.15	0.32	3.20	3.04
0.1	0.15	0.32	3.20	3.04
0.2	0.16	0.32	3.06	2.95
0.3	0.18	0.32	2.86	2.90
0.4	0.23	0.32	2.62	2.68
0.5	0.26	0.32	2.38	2.50
0.6	0.34	0.32	2.17	2.36
0.7	0.46	0.34	2.00	2.22
0.8	0.67	0.39	1.85	2.09
0.9	0.89	0.49	1.69	1.95
1.0	1.12	0.63	1.52	1.86
1.1	1.32	0.86	1.38	1.68
1.2	1.50	1.09	1.26	1.59
1.3	1.73	1.27	1.12	1.49
1.4	1.93	1.45	0.96	1.36
1.5	2.15	1.64	0.83	1.23
1.6	2.75	2.23	0.52	0.95
1.7	2.58	2.00	0.61	1.00
1.8	2.75	2.23	0.52	0.95
1.9	2.90	2.41	0.45	0.91
2.0	3.02	2.50	0.39	0.86
2.1	3.12	2.64	0.33	0.77
2.2	3.17	2.77	0.29	0.73
2.3	3.19	2.86	0.24	0.68
2.4	3.20	2.95	0.21	0.64
2.5	3.20	2.99	0.19	0.59
2.6	3.20	3.02	0.17	0.55
2.7	3.20	3.02	0.16	0.53
2.8	3.20	3.04	0.16	0.50
2.9	3.20	3.04	0.15	0.45
3.0	3.20	3.04	0.15	0.41
3.1	3.20	3.04	0.15	0.40
3.2	3.20	3.04	0.15	0.37
3.3	3.20	3.04	0.15	0.36
3.4	3.20	3.04	0.15	0.32
3.5	3.20	3.04	0.15	0.32

Ordering Information

To order, please specify as shown below:

TQ1089-MC nnn 11-Output Configurable Clock Buffer



Additional Information

For latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com **Tel:** (503) 615-9000
Email: sales@tqs.com **Fax:** (503) 615-8900

For technical questions and additional information on specific applications:

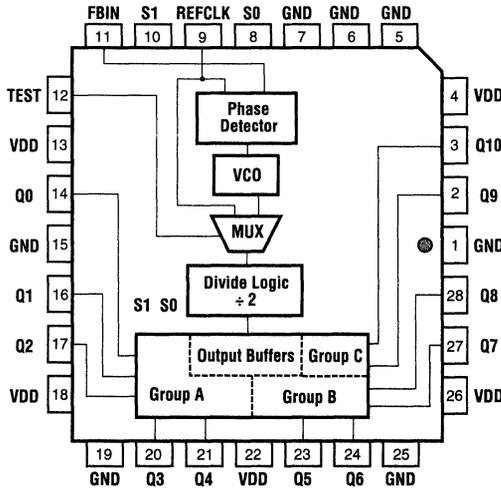
Email: applications@tqs.com

The information provided herein is believed to be reliable; TriQuint assumes no liability for inaccuracies or omissions. TriQuint assumes no responsibility for the use of this information, and all such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. TriQuint does not authorize or warrant any TriQuint product for use in life-support devices and/or systems. Copyright © 1997 TriQuint Semiconductor, Inc. All rights reserved.

Revision 1.0.A October 1997



Figure 1. Block Diagram



TriQuint's TQ1090 is a configurable clock buffer which generates 11 outputs, operating over a wide range of frequencies from 33 MHz to 45MHz, 65 MHz to 90 MHz and 130 MHz to 180 MHz. The outputs are available at 1x, 2x and 4x, or at $1/2x$, 1x and 2x, or at $1/4x$, $1/2x$ and 1x the reference clock frequency, f_{REF} .

When one of the Group A outputs (Q0–Q4) is used as feedback to the PLL, all Group A outputs will be at f_{REF} , all Group B outputs (Q5–Q8) will be at $2x f_{REF}$ and all Group C outputs (Q9,Q10) will be at $4x f_{REF}$. When one of the Group B outputs is used as feedback to the PLL, all Group A outputs will be at $1/2x f_{REF}$, all Group B outputs will be at f_{REF} and all Group C outputs will be at $2x f_{REF}$. When one of the Group C outputs is used as feedback to the PLL, all Group A outputs will be at $1/4x f_{REF}$, all Group B outputs will be at $1/2x f_{REF}$ and all Group C outputs will be at f_{REF} .

A very stable internal Phase-Locked Loop (PLL) provides low-jitter operation. This completely self-contained PLL requires no external capacitors or resistors. The PLL's Voltage-Controlled Oscillator (VCO) has a frequency range from 260 MHz to 360 MHz. By feeding back one of the output clocks to FBIN, the PLL continuously maintains frequency and phase synchronization between the reference clock (REFCLK) and each of the outputs.

TQ1090

11-Output Configurable Clock Buffer

Features

- Wide frequency range: 33 MHz to 45 MHz, 65 MHz to 90 MHz and 130 MHz to 180 MHz
- Output configurations: four outputs at f_{REF} , four outputs at $2x f_{REF}$, two output at $4x f_{REF}$ or five outputs at $1/2x f_{REF}$, three outputs at f_{REF} , two outputs at $2x f_{REF}$
- Selectable Phase Shift: $-2t$, $-t$, 0 , $+t$ ($t = 1/f_{VCO}$)
- Low output-to-output skew: 150 ps (max) within a group
- Near-zero propagation delay: $-350\text{ ps} \pm 500\text{ ps (max)}$ or $-350\text{ ps} \pm 700\text{ ps (max)}$
- TTL-compatible I/O with 30 mA output drive
- Ideal for Power PC™ designs
- 28-pin J-lead surface-mount package

SYSTEM TIMING PRODUCTS

TQ1090

The phase relationship of the Group A outputs to Group B and C are controlled by the phase-select pins S0 and S1. The phase difference can be varied from $-2t$, $-t$, 0 or $+t$, where $t = 1/fvco$.

TriQuint's patented output buffer design delivers a very low output-to-output skew of 150 ps (max). The TQ1090's symmetrical TTL outputs are capable of sourcing and sinking 30 mA.

Functional Description

The core of the TQ1090 is a Phase-Locked Loop (PLL) that continuously compares the reference clock (REFCLK) to the feedback clock (FBIN), maintaining a zero frequency difference between the two. Since one of the outputs is always connected to FBIN, the PLL keeps the propagation delay between the outputs and the reference clock within -350 ps \pm 500 ps for the TQ1090-MC500, and within -350 ps \pm 700 ps for the TQ1090-MC700.

The internal Voltage-Controlled Oscillator (VCO), has an operating range of 260 MHz to 360 MHz, as shown in Table 1. The combination of the VCO and the Divide Logic enables the TQ1090 to operate between 33 MHz and 45 MHz, 65 MHz and 90 MHz, and from 130 MHz to 180 MHz.

The Shift Select pins, S0 and S1, control the phase shift of the Group A outputs (Q0 – Q4), relative to the other outputs. The user can select from four incremental phase shifts as shown in Table 2 (Phase Selection). The phase shift increment (t) is calculated using the following equation, where n is the divide mode:

$$t = \frac{1}{(f_{REF}) (n)}$$

In the test mode, the PLL is bypassed and REFCLK is connected directly to the Divide Logic block via the MUX, as shown in Figure 1. This mode is useful for debug and test purposes. The test mode is outlined in Table 3.

The maximum rise and fall time at the output pins is 1.4 ns. All outputs of the TQ1090 are TTL-compatible with 30 mA symmetric drive and a minimum V_{OH} of 2.4 V.

Power-Up/Reset Synchronization

After power-up or reset, the PLL requires time before it achieves synchronization lock. The maximum time required for synchronization (TSYNC) is 500 ms.

Table 1. Frequency Mode Selection

Test	Output Feedback	Mode	Reference Clock Frequency Range	Output Frequency Range		
				Group A: Q0–Q4	Group B: Q5, Q08	Group c: Q9, Q10
0	Group A	$\div 8$	35 MHz – 45 MHz	35 MHz – 45 MHz	65 MHz – 90 MHz	130 MHz – 180 MHz
0	Group B	$\div 4$	65 MHz – 90 MHz	35 MHz – 45 MHz	65 MHz – 90 MHz	130 MHz – 180 MHz
0	Group C	$\div 2$	130 MHz – 180 MHz	35 MHz – 45 MHz	65 MHz – 90 MHz	130 MHz – 180 MHz

Table 2. Phase Shift Selection

S0	S1	Phase Shift (Group A: Q0 – Q4)
0	0	+t
1	0	0
0	1	-t
1	1	-2t

Table 2. Test Mode Selection

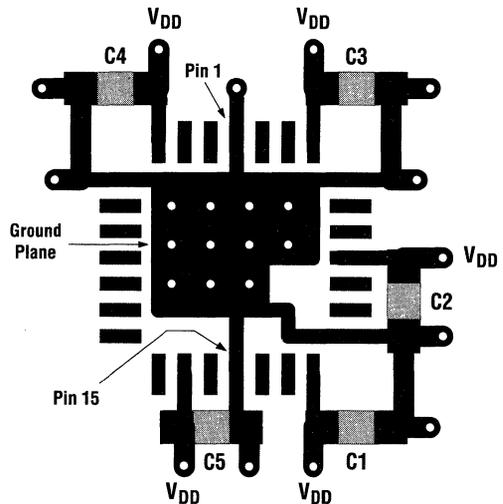
Test	Mode	Ref. Clock	Group A Outputs Q0–Q4	Group B Outputs Q5–Q18	Group C Outputs Q9–Q10
1	±2	f_{REF}	$f_{REF} \div 8$	$f_{REF} \div 4$	$f_{REF} \div 2$

Layout Guidelines

Multiple ground and power pins on the TQ1090 reduce ground bounce. Good layout techniques, however, are necessary to guarantee proper operation and to meet the specifications across the full operating range. We recommend bypassing each of the V_{DD} supply pins to the nearest ground pin, as close to the chip as possible.

Figure 2 shows the recommended power layout for the TQ1090. The bypass capacitors should be located on the same side of the board as the TQ1090. The V_{DD} traces connect to an inner-layer V_{DD} plane. All of the ground pins (GND) are connected to a small ground plane on the surface beneath the chip. Multiple through-holes connect this small surface plane to an inner-layer ground plane. The capacitors (C1–C5) are 0.1 mF. TriQuint’s test board uses X7R temperature-stable capacitors in 1206 SMD cases.

Figure 2. Top Layer Layout of Power Pins
(approx. 3.3x)



SYSTEM TIMING PRODUCTS

TQ1090

Absolute Maximum Ratings ¹

Storage temperature	-65 °C to +150 °C
Ambient temperature with power applied ²	-55 °C to +100 °C
Supply voltage to ground potential	-0.5 V to +7.0 V
DC input voltage	-0.5 V to +(V _{DD} + 0.5)V
DC input current	-30 mA to +5 mA
Package thermal resistance (MQuad)	$\theta_{JA} = 45 \text{ }^{\circ}\text{C/W}$
Die junction temperature	$T_J = 150 \text{ }^{\circ}\text{C}$

DC Characteristics

(V_{DD} = +5 V ± 5%, T_A = 0 °C to +70 °C)³

Symbol	Description	Test Conditions	Min	Limits ⁴		Unit
				Typ	Max	
V _{OHT}	Output HIGH voltage	V _{DD} = Min I _{OH} = -30 mA V _{IN} = V _{IH} or V _{IL}	2.4	3.4		V
V _{OHC}	Output HIGH voltage	V _{DD} = Min I _{OH} = -1 mA V _{IN} = V _{IH} or V _{IL}	3.2	4.1		V
V _{OL}	Output LOW voltage	V _{DD} = Min I _{OL} = 30 mA V _{IN} = V _{IH} or V _{IL}		0.27	0.5	V
V _{IH} ⁵	Input HIGH level	Guaranteed input logical HIGH Voltage for all inputs	2.0			V
V _{IL} ⁵	Input LOW level	Guaranteed input logical LOW Voltage for all inputs			0.8	V
I _{IL}	Input LOW current	V _{DD} = Max V _{IN} = 0.40 V		-156	-400	μA
I _{IH}	Input HIGH current	V _{DD} = Max V _{IN} = 2.7 V		0	25	μA
I _I	Input HIGH current	V _{DD} = Max V _{IN} = 5.5 V		2	1000	μA
I _{DDS} ⁶	Power supply current	V _{DD} = Max		119	170	mA
V _I	Input clamp voltage	V _{DD} = Min I _{IN} = -18 mA		-0.70	-1.2	V

Capacitance

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
C _{IN} ³	Input capacitance	V _{IN} = 2.0 V at f = 1 MHz		6		pF

- Notes:
1. Exceeding these parameters may damage the device.
 2. Maximum ambient temperature with device not switching and unloaded.
 3. These values apply to both TQ1089-MC500 and TQ1089-MC700.
 4. Typical limits are at V_{DD} = 5.0 V and T_A = 25 °C.
 5. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
 6. This parameter is measured with device not switching and unloaded.
 7. These parameters are not 100% tested, but are periodically sampled.

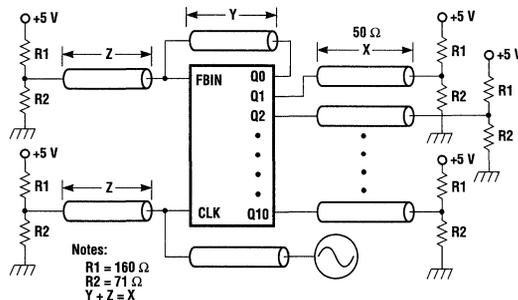
AC Characteristics

($V_{DD} = +5\text{ V} \pm 5\%$, $T_A = 0\text{ }^\circ\text{C}$ to $+70\text{ }^\circ\text{C}$)

Symbol	Input Clock (REFCLK)	Test Conditions (Figure 3) ¹	Min	Typ	Max	Unit
t_{CPWH}	CLK pulse width HIGH	Figure 4	2	---	---	ns
t_{CPWL}	CLK pulse width LOW	Figure 4	2	---	---	ns
t_{IR}	Input rise time (0.8 V - 2.0V)		---	---	2.0	ns
Symbol	Output Clocks (Q0-Q10)	Test Conditions (Figure 3) ¹	Min	Typ	Max	Unit
t_{OR}, t_{OF}	Rise/fall time (0.8 V - 2.0V)	Figure 4	350	---	1400	ps
t_{PD1}^2	CLK \uparrow to FBIN \uparrow (TQ1090-MC500)	Figure 4	-850	-350	+150	ps
t_{PD2}^2	CLK \uparrow to FBIN \uparrow (TQ1090-MC700)	Figure 4	-1050	-350	+350	ps
t_{SKEW1}^3	Rise-rise, fall-fall (within group)	Figure 5	---	60	150	ps
t_{SKEW2}^3	Rise-rise, fall-fall (group-to-group, aligned)	Figure 6 (skew2 takes into account skew1)	---	75	350	ps
t_{SKEW3}^3	Rise-rise, fall-fall (group-to-group, non-aligned)	(skew3 takes into account skews1, 2)	---	---	650	ps
t_{SKEW4}^3	Rise-fall, fall-rise	(skew4 takes into account skew3)	---	---	1200	ps
t_{CYC}^4	Duty-cycle Variation	Figure 4	-1000	0	+1000	ps
t_{JP}^5	Period-to-Period Jitter	Figure 4	---	80	200	ps
t_{JR}^5	Random Jitter	Figure 4	---	190	400	ps
t_{SYNC}^6	Synchronization Time		---	10	500	μs

- Notes: 1. All measurements are tested with a REFCLK having a rise time of 0.5 ns (0.8 V to 2.0 V).
 2. The PLL maintains alignment of CLK and FBIN at all times. This specification applies to the rising edge only because the input duty cycle can vary while the output duty cycle is typically 50/50. The delay t_{PD} is measured at the 1.5 V level between CLK and FBIN.
 3. Skew specifies the width of the window in which outputs switch, and is measured at 1.5 V.
 Skew 1 is a subset of skew 2. Skew 2 is a subset of skew 3. Skew 3 is a subset of skew 4.
 Definition of skew terms:
 Rise-rise: Skew between rising edges (low to high transitions).
 Fall-fall: Skew between falling edges (high to low transitions).
 Rise-fall, fall-rise: Skew between rising-to-falling and falling-to-rising edges.
 Within a group: Skew between outputs of the same group (for example, skew among Group A outputs)
 Group-to-group: Skew between outputs of any group (for example, skew between Group A to Group B outputs)
 Aligned: Skew between outputs that are in phase.
 Non-aligned: Skew between outputs that are not in phase.
 4. This specification represents the deviation from 50/50 on the outputs.
 5. Jitter specifications refer to peak-to-peak value. t_{JR} is the jitter on the output with respect to the reference clock. t_{JP} is the jitter on the output with respect to the same output's previous rising edge.
 6. t_{SYNC} is the time required for the PLL to synchronize; this assumes the presence of a CLK signal and a connection from one of the outputs to FBIN.

Figure 3. AC Test Circuit



SYSTEM TIMING PRODUCTS

Switching Waveforms

Figure 4. General Timing

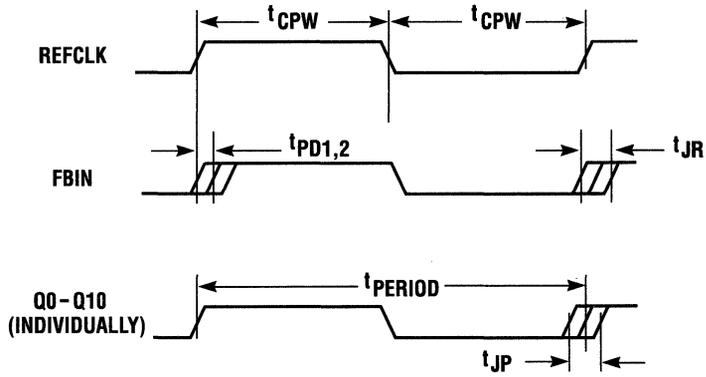
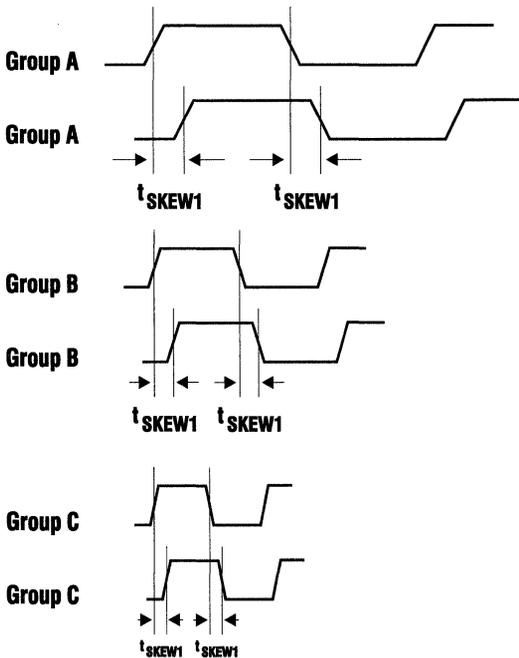


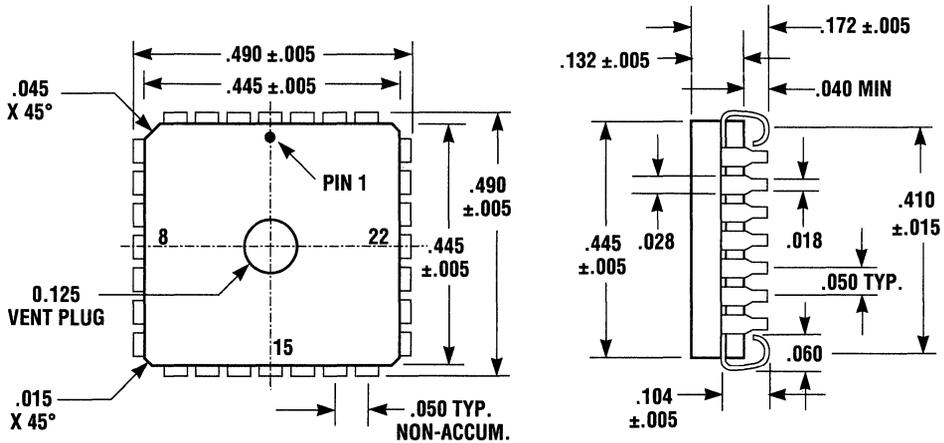
Figure 5. t_{SKEW1}

Figure 6. t_{SKEW2}



28-Pin MQuad J-Leaded Package Mechanical Specification

(All dimensions in inches)



28-Pin MQuad Pin Description

Pin #	Pin Name	Description	I/O
1	GND	Ground	—
2	Q9	Output Clock 9 (C1)	O
3	Q10	Output Clock 10 (C2)	O
4	VDD	+5 V	—
5	GND	Ground	—
6	GND	Ground	—
7	GND	Ground	—
8	GND	Ground	—
9	REFCLK	Reference Clock	I
10	GND	Ground	—
11	FBIN	Feedback In	I
12	TEST	Test	I
13	VDD	+5 V	—
14	Q0	Output Clock 0 (A1)	O

Pin #	Pin Name	Description	I/O
15	GND	Ground	—
16	Q1	Output Clock 1 (A2)	O
17	Q2	Output Clock 2 (A3)	O
18	VDD	+5 V	—
19	GND	Ground	—
20	Q3	Output Clock 3 (A4)	O
21	Q4	Output Clock 4 (A5)	O
22	VDD	+5 V	—
23	Q5	Output Clock 5 (B1)	O
24	Q6	Output Clock 6 (B2)	O
25	GND	Ground	—
26	VDD	+5 V	—
27	Q7	Output Clock 7 (B3)	O
28	Q8	Output Clock 8 (B4)	O

SYSTEM TIMING PRODUCTS

Output Characteristics

The IV characteristics, transition times, package characteristics, device and bond wire characteristics for the TQ1090 are described in Tables 4 through 9 and Figures 9 through 11.

Figure 9. I_{OH} vs. V_{OH}

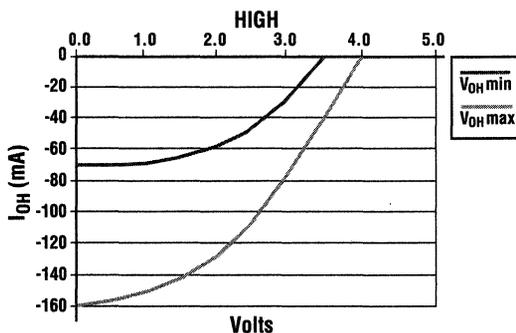


Table 4. I_{OH} vs. V_{OH}

V_{OH}	$I_{OH\ min}$ (mA)	$I_{OH\ max}$ (mA)
0.0	-70	-160
0.5	-70	-157
1.0	-68	-152
1.5	-65	-142
2.0	-59	-130
2.5	-48	-106
3.0	-29	-79
3.5	0	-42
4.0	0	0
4.5	0	0
5.0	0	0
5.5	40	120
6.0	90	265
6.5	115	350
7.0	135	410
7.5	145	435

These output characteristics are provided for modelling purposes only. TriQuint does not guarantee the information in these tables and figures.

Figure 10. I_{OL} vs. V_{OL}

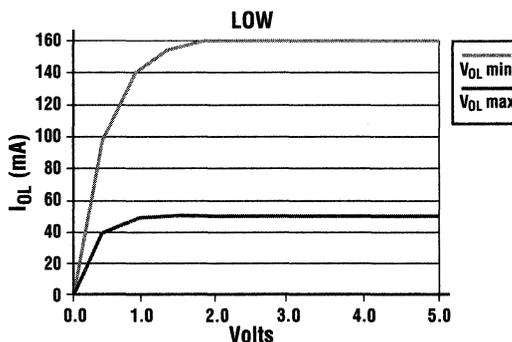


Table 5. I_{OL} vs. V_{OL}

V_{OL}	$I_{OL\ min}$ (mA)	$I_{OL\ max}$ (mA)
-2.5	-145	-435
-2.0	-135	-410
-1.5	-115	-350
-1.0	-90	-265
-0.5	-40	-120
0.0	0	0
0.5	37	97
1.0	49	140
1.5	53	155
2.0	54	157
2.5	54	159
3.0	54	160
3.5	54	160
4.0	54	160
4.5	54	160
5.0	54	160
10.0	54	160

Notes: 1. These are worst-case corners for process, voltage, and temperature.

2. Includes diode to ground current.

Table 6. Above- V_{DD} and Below-Ground Characteristics

Diode to GND		Diode Stack to VDD	
V	I (mA)	V	I (mA)
0.0	0	5.0	0
-0.4	0	5.4	0
-0.5	0	5.5	0
-0.6	-5	5.6	5
-0.7	-15	5.7	15
-0.8	-35	5.8	35
-0.9	-55	5.9	55
-1.0	-75	6.0	75
-2.0	-300	7.0	300
-2.5	-350	7.5	350
-3.0	-360	8.0	360

Note: TriQuint does not guarantee diode operation for purposes other than ESD protection.

Figure 11. Output Model

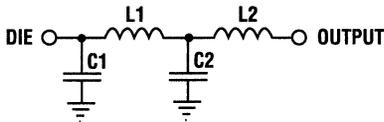


Table 7. Device and Bond Wire Characteristics (Estimated)

L1	C1
2 nH	10 pF

Table 8. 28-Pin MQuad Package Characteristics

L2	C2
1.85 nH	0.40 pF

Table 9. Rise and Fall Times (Into 0 pF, 50 Ohms to 1.5 V)

Time (ns)	T_R min (V)	T_R max (V)	T_F min (V)	T_F max (V)
0.0	0.15	0.32	3.20	3.04
0.1	0.15	0.32	3.20	3.04
0.2	0.16	0.32	3.06	2.95
0.3	0.18	0.32	2.86	2.90
0.4	0.23	0.32	2.62	2.68
0.5	0.26	0.32	2.38	2.50
0.6	0.34	0.32	2.17	2.36
0.7	0.46	0.34	2.00	2.22
0.8	0.67	0.39	1.85	2.09
0.9	0.89	0.49	1.69	1.95
1.0	1.12	0.63	1.52	1.86
1.1	1.32	0.86	1.38	1.68
1.2	1.50	1.09	1.26	1.59
1.3	1.73	1.27	1.12	1.49
1.4	1.93	1.45	0.96	1.36
1.5	2.15	1.64	0.83	1.23
1.6	2.75	2.23	0.52	0.95
1.7	2.58	2.00	0.61	1.00
1.8	2.75	2.23	0.52	0.95
1.9	2.90	2.41	0.45	0.91
2.0	3.02	2.50	0.39	0.86
2.1	3.12	2.64	0.33	0.77
2.2	3.17	2.77	0.29	0.73
2.3	3.19	2.86	0.24	0.68
2.4	3.20	2.95	0.21	0.64
2.5	3.20	2.99	0.19	0.59
2.6	3.20	3.02	0.17	0.55
2.7	3.20	3.02	0.16	0.53
2.8	3.20	3.04	0.16	0.50
2.9	3.20	3.04	0.15	0.45
3.0	3.20	3.04	0.15	0.41
3.1	3.20	3.04	0.15	0.40
3.2	3.20	3.04	0.15	0.37
3.3	3.20	3.04	0.15	0.36
3.4	3.20	3.04	0.15	0.32
3.5	3.20	3.04	0.15	0.32

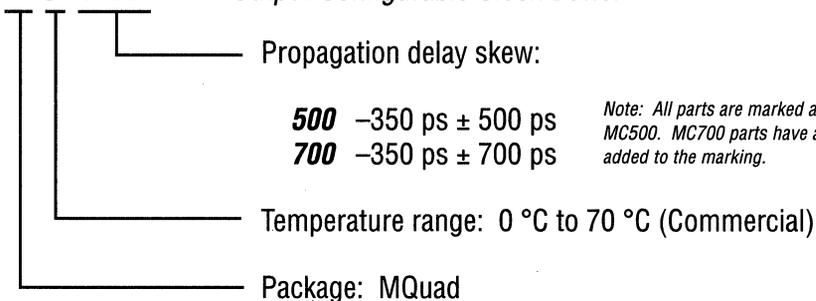
SYSTEM TIMING PRODUCTS

TQ1090

Ordering Information

To order, please specify as shown below:

TQ1090-MC nnn 11-Output Configurable Clock Buffer



Note: All parts are marked as MC500. MC700 parts have a "2" added to the marking.

Additional Information

For latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com **Tel:** (503) 615-9000
Email: sales@tqs.com **Fax:** (503) 615-8900

For technical questions and additional information on specific applications:

Email: applications@tqs.com

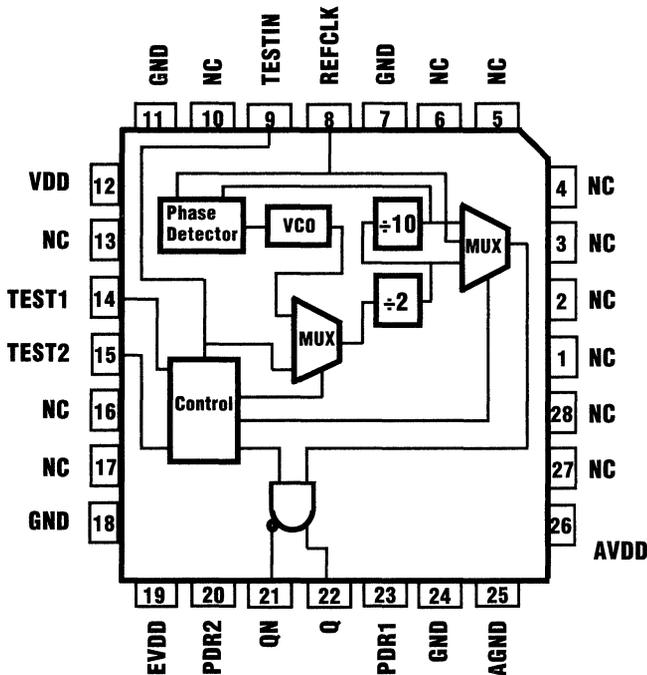
The information provided herein is believed to be reliable; TriQuint assumes no liability for inaccuracies or omissions. TriQuint assumes no responsibility for the use of this information, and all such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. TriQuint does not authorize or warrant any TriQuint product for use in life-support devices and/or systems.

Copyright © 1997 TriQuint Semiconductor, Inc. All rights reserved.

Revision 1.0.A October 1997



Figure 1. Pinout Diagram



TriQuint's TQ2059 is a high-frequency clock generator. It utilizes a 20 MHz to 35 MHz TTL input to generate a 200 MHz to 350 MHz PECL output. The TQ2059 has a completely self-contained Phase-Locked Loop (PLL) running at 400 MHz to 700 MHz. This stable PLL allows for a low period-to-period output jitter of 120 ps (max), and enables tight duty-cycle control of 55% to 45% (worst case).

The TQ2059 provides optional 200-ohm on-chip pull-down resistors which are useful if the output is AC-coupled to the device being driven. In order to use these resistors, pin 20 (PDR2) should be connected to pin 21 (QN), and pin 23 (PDR1) should be connected to pin 22 (Q).

Various test modes on the chip simplify debug and testing of systems by slowing the clock output or by bypassing the PLL.

TQ2059

High-Frequency Clock Generator

Features

- Output frequency range:
200 MHz to 350 MHz
- One differential PECL output:
600 mV (min) swing
- Common-mode voltage:
 $V_{DD} - 1.2\text{ V}$ (max),
 $V_{DD} - 1.6\text{ V}$ (min)
- Period-to-period output jitter:
30 ps peak-to-peak (typ)
120 ps peak-to-peak (max)
- Reference clock input:
20 MHz to 35 MHz TTL-level
crystal oscillator
- Self-contained loop filter
- Optional 200-ohm pull-down
resistors for AC-coupled outputs
- +5 V power supply
- 28-pin J-lead surface-mount
package
- Ideal for designs based on DEC
Alpha AXP™ processors

Figure 2. Simplified Block Diagram

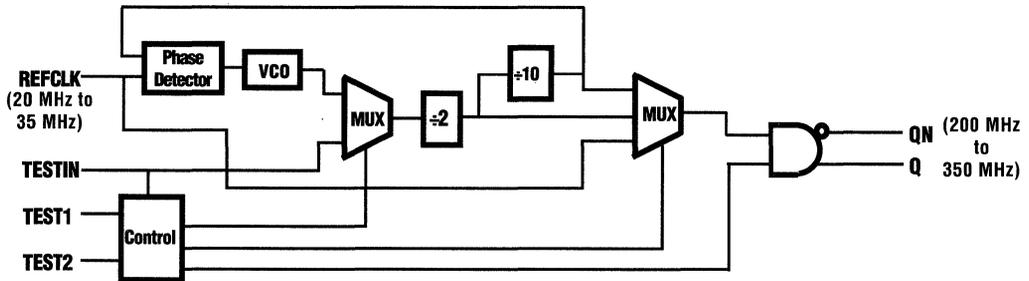


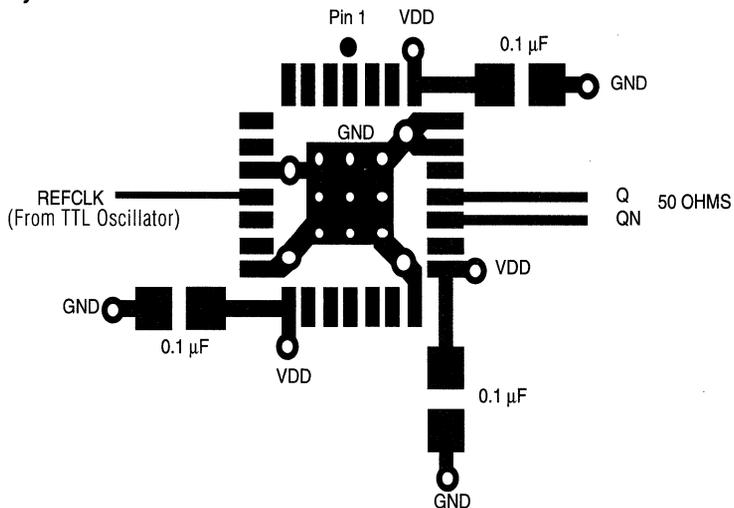
Table 1. Mode Selection

Mode	TEST1	TEST2	TESTIN ¹	REFCLK ²	Q, QN
1 (Test)	0	0	$f_{TESTCLK}$	"don't care"	$f_{TESTCLK} \div 20$
2 (Test)	0	1	"don't care"	"don't care"	0, 1
3 (Test)	1	0	$f_{TESTCLK}$	"don't care"	$f_{TESTCLK} \div 2$
4 (Bypass)	1	1	0	f_{REFCLK}	f_{REFCLK}
5 (Normal)	1	1	1	f_{REFCLK}	$10 \times f_{REFCLK}^3$

Note: 1. In modes 1 and 3, TESTIN may be used to bypass the PLL. A clock input at TESTIN will be divided as shown.
 2. REFCLK = 20 MHz to 35 MHz.
 3. Q, QN = 200 MHz to 350 MHz.

Recommended Layout

(Not to scale)



Absolute Maximum Ratings

Storage Temperature	-65°C to +150°C
Ambient temperature with power applied	-55°C to +110°C
Supply voltage to ground potential	-0.5 V to +7.0 V
DC input voltage	-0.5 V to ($V_{DD} + 0.5$) V
DC input current	-30 mA to +5 mA
Package thermal resistance (MQuad)	$\theta_{JA} = 45^{\circ}\text{C/W}$
Die junction temperature	$T_J = 150^{\circ}\text{C}$

Note: Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. The device should be operated only under the DC and AC conditions shown below.

DC Characteristics ($V_{DD} = +5\text{ V} \pm 5\%$, $T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$)¹

Symbol	Description	Test Conditions	Limits ¹			Unit
			Min	Typ	Max	
V_{OH}	Output HIGH voltage	$V_{CC} = \text{Min PECL load}$	$V_{CC}-1.20$		$V_{CC}-0.50$	V
V_{OL}	Output LOW voltage	$V_{CC} = \text{Min PECL load}$	$V_{CC}-2.00$		$V_{CC}-1.60$	V
V_{CMO}	Output common mode voltage	PECL	$V_{CC}-1.60$		$V_{CC}-1.20$	V
V_{OUT}	Output differential voltage	PECL	0.6		1.2	V
V_{IH}^2	Input HIGH level	Guaranteed input logical HIGH Voltage for all inputs	2.0			V
V_{IL}^2	Input LOW level	Guaranteed input logical LOW Voltage for all inputs			0.8	V
I_{IL}	Input LOW current	$V_{DD} = \text{Max}$ $V_{IN} = 0.40\text{ V}$		-150	-400	μA
I_{IH}	Input HIGH current	$V_{DD} = \text{Max}$ $V_{IN} = 2.7\text{ V}$		0	25	μA
I_I	Input HIGH current	$V_{DD} = \text{Max}$ $V_{IN} = 5.3\text{ V}$		2	1000	μA
I_{DD}^3	Power supply current	$V_{DD} = \text{Max}$		85	120	mA
V_I	Input clamp voltage	$V_{DD} = \text{Min}$ $I_{IN} = -18\text{ mA}$		-0.70	-1.2	V

Capacitance

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 2.0\text{ V}$ at $f = 1\text{ MHz}$		6		pF
C_{OUT}	Output Capacitance	$V_{OUT} = 2.0\text{ V}$ at $f = 1\text{ MHz}$		9		pF

- Notes: 1. Typical limits are at $V_{DD} = 5.0\text{ V}$ and $T_A = 25^{\circ}\text{C}$.
 2. These are absolute values with respect to device ground and include all overshoots due to system or tester noise.
 3. This parameter is measured with device not switching and unloaded.

TQ2059

AC Characteristics ($V_{DD} = +5 V \pm 5\%$, $T_A = 0\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$)

Symbol	Input Clock (REFCLK)	Test Conditions	Min	Typ	Max	Unit
t_{CPWH}	CLK pulse width HIGH	Figure 2	4	—	—	ns
t_{CPWL}	CLK pulse width LOW	Figure 2	4	—	—	ns
t_{IR}	Input rise time (0.8 V – 2.0 V)		—	—	2.0	ns

Symbol	Input Clock (REFCLK)	Test Conditions	Min	Typ	Max	Unit
t_{OR} , t_{OF}	Rise/fall time (20% – 80%)	Figure 2	100	220	350	ps
t_{CYC}	Duty-cycle	Figure 2	45	50	55	%
t_{JP}^2	Period-to-Period Jitter		—	30	120	ps
t_{SYNC}^3	Synchronization Time		—	10	500	μs

- Notes: 1. All measurements are tested with a REFCLK having a rise time of 0.5 ns (0.8 V to 2.0 V).
 2. Jitter specification is peak to peak. Period-to-Period jitter is the jitter on the output with respect to the output's previous crossing.
 3. t_{SYNC} is the time required for the PLL to synchronize and assumes the presence of a CLK signal.

Figure 1

PECL Test Load

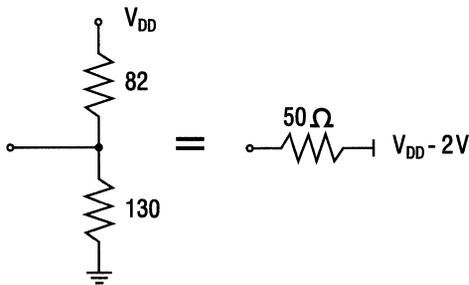
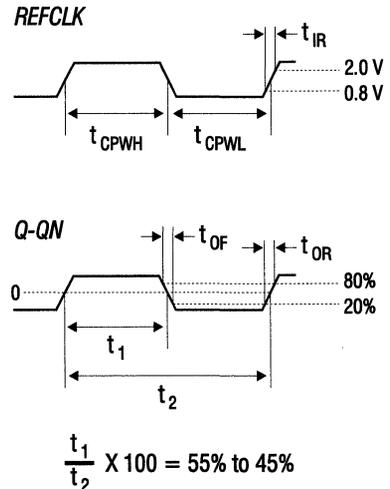
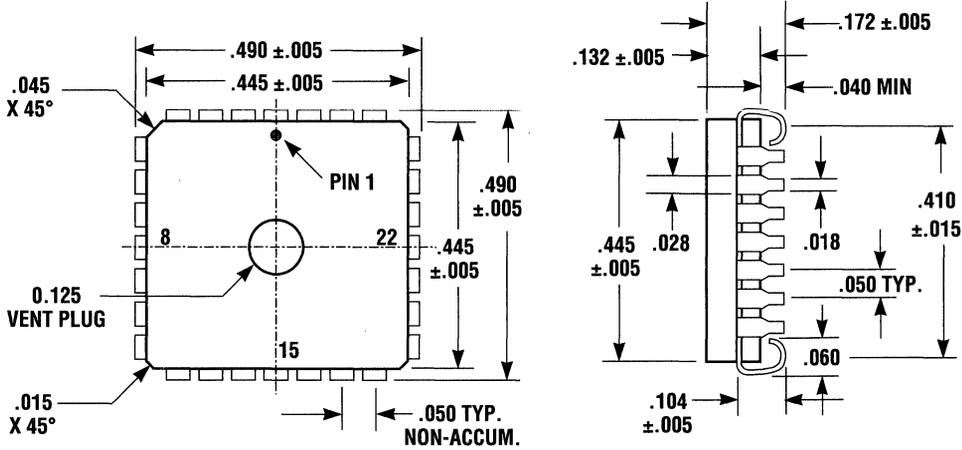


Figure 2



28-Pin MQuad J-Leaded Package Mechanical Specification
 (All dimensions in inches)



28-Pin MQuad Pin Description

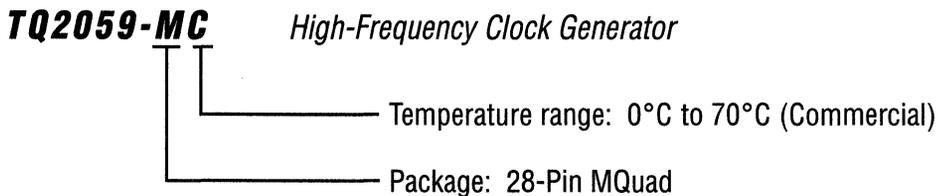
Pin #	Pin Name	Description	I/O
1	NC	No Connect	—
2	NC	No Connect	—
3	NC	No Connect	—
4	NC	No Connect	—
5	NC	No Connect	—
6	NC	No Connect	—
7	GND	Ground	—
8	REFCLK	Reference Clock	I
9	TESTIN	Test Input	I
10	NC	No Connect	—
11	GND	Logic Ground	—
12	VDD	Logic VDD (+5 V)	—
13	NC	No Connect	—
14	TEST1	Test Control 1	I

Pin #	Pin Name	Description	I/O
15	TEST2	Test Control 2	I
16	NC	No Connect	—
17	NC	No Connect	O
18	GND	Ground	—
19	EVDD	VDD for ECL Output (+5 V)	—
20	PDR2	Pull-down Resistor 2 (200 Ω)	I
21	QN	Differential PECL Output (-)	O
22	Q	Differential PECL Output (+)	O
23	PDR1	Pull-down Resistor 1 (200 Ω)	I
24	GND	Ground	—
25	AGND	Analog Ground	—
26	AVDD	Analog VDD (+5 V)	—
27	NC	No Connect	—
28	NC	No Connect	—

SYSTEM TIMING
PRODUCTS

Ordering Information

To order, please specify as shown below:



Additional Information

For latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com **Tel:** (503) 615-9000
Email: sales@tqs.com **Fax:** (503) 615-8900

For technical questions and additional information on specific applications:

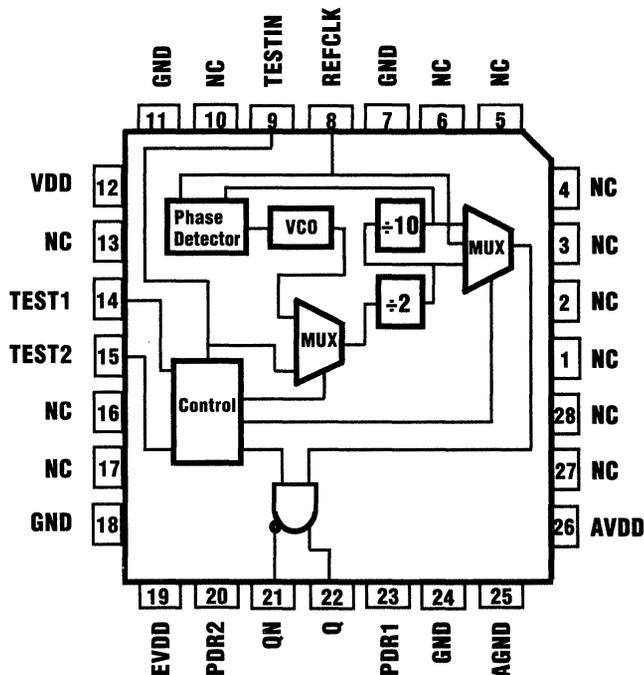
Email: applications@tqs.com

The information provided herein is believed to be reliable; TriQuint assumes no liability for inaccuracies or omissions. TriQuint assumes no responsibility for the use of this information, and all such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. TriQuint does not authorize or warrant any TriQuint product for use in life-support devices and/or systems.

Copyright © 1997 TriQuint Semiconductor, Inc. All rights reserved.

Revision 1.0.A October 1997

Figure 1. Pinout Diagram



TriQuint's TQ2060 is a high-frequency clock generator. It utilizes a 35 MHz to 50 MHz TTL input to generate a 350 MHz to 500 MHz PECL output. The TQ2060 has a completely self-contained Phase-Locked Loop (PLL) running at 700 MHz to 1000 MHz. This stable PLL allows for a low period-to-period output jitter of 70 ps (max), and enables tight duty cycle control of 55% to 45% (worst case).

The TQ2060 provides optional 200 ohm on-chip pull-down resistors which are useful if the output is AC-coupled to the device being driven. In order to use these resistors, pin 20 (PDR2) should be connected to pin 21 (QN), and pin 23 (PDR1) should be connected to pin 22 (Q).

Various test modes on the chip simplify debug and testing of systems by slowing the clock output or by bypassing the PLL.

TQ2060

High-Frequency Clock Generator

Features

- Output frequency range:
350 MHz to 500 MHz
- One differential PECL output:
600 mV (min) swing
- Common-mode voltage:
 $V_{DD} - 1.2$ V (max),
 $V_{DD} - 1.6$ V (min)
- Period-to-period output jitter:
25 ps peak-to-peak (typ)
70 ps peak-to-peak (max)
- Reference clock input:
35 MHz to 50 MHz TTL-level
crystal oscillator
- Self-contained loop filter
- Optional 200-ohm pull-down
resistors for AC-coupled outputs
- +5 V power supply
- 28-pin J-lead surface-mount
package
- Ideal for designs based on
DEC Alpha AXP™ processors

TQ2060

Figure 2. Simplified Block Diagram

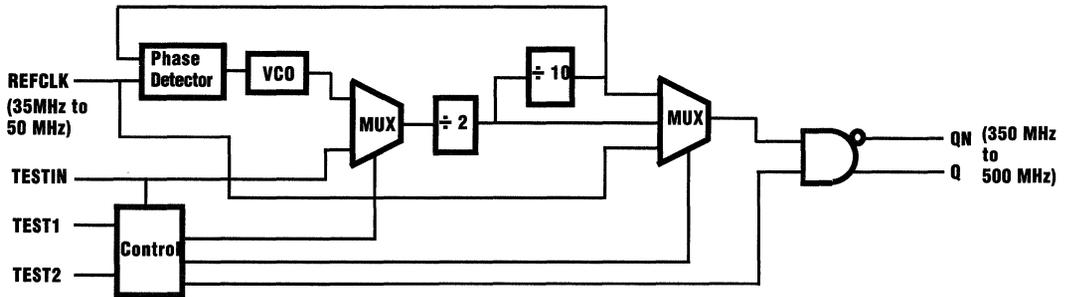


Table 1. Mode Selection

Mode	TEST1	TEST2	TESTIN ¹	REFCLK	Q, QN
1 (Test)	0	0	$f_{TESTCLK}$	"don't care"	$f_{REFCLK}^2 \div 20$
2 (Test)	0	1	"don't care"	"don't care"	0, 1
3 (Test)	1	0	$f_{TESTCLK}$	"don't care"	$f_{TESTCLK} \div 2$
4 (Bypass)	1	1	0	f_{REFCLK}	f_{REFCLK}
5 (Normal)	1	1	1	f_{REFCLK}	$10 \times f_{REFCLK}^3$

Notes: 1. In modes 1 and 3, TESTIN may be used to bypass the PLL. A clock input at TESTIN will be divided as shown.
 2. REFCLK = 35 MHz to 50 MHz.
 3. Q, QN = 350 MHz to 500 MHz.

Figure 3. Recommended Layout
(Not to scale)

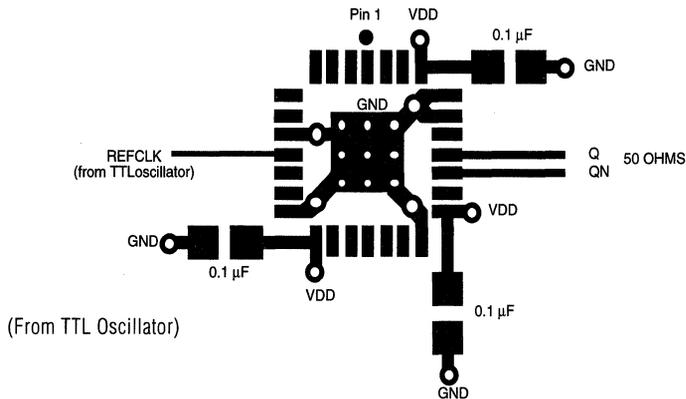


Table 2. Absolute Maximum Ratings

Storage Temperature	-65°C to +150°C
Ambient temperature with power applied	-55°C to +110°C
Supply voltage to ground potential	-0.5 V to +7.0 V
DC input voltage	-0.5 V to (V _{DD} + 0.5) V
DC input current	-30 mA to +5 mA
Package thermal resistance (MQuad)	θ _{JA} = 45°C/W
Die junction temperature	T _J = 150°C

Note: Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. The device should be operated only under the DC and AC conditions shown below.

Table 3. DC Characteristics (V_{DD} = +5 V ± 5%, T_A = 0 °C to +70 °C)¹

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
V _{OH}	Output HIGH voltage	V _{CC} = Min PECL load	V _{CC} -1.20		V _{CC} -0.50	V
V _{OL}	Output LOW voltage	V _{CC} = Min PECL load	V _{CC} -2.00		V _{CC} -1.60	V
V _{CMO}	Output common mode voltage	PECL	V _{CC} -1.60		V _{CC} -1.20	V
V _{OUT}	Output differential voltage	PECL	0.6		1.2	V
V _{IH} ²	Input HIGH level	Guaranteed input logical HIGH Voltage for all inputs	2.0			V
V _{IL} ²	Input LOW level	Guaranteed input logical LOW Voltage for all inputs			0.8	V
I _{IL}	Input LOW current	V _{DD} = Max V _{IN} = 0.40 V		-150	-400	μA
I _{IH}	Input HIGH current	V _{DD} = Max V _{IN} = 2.7 V		0	25	μA
I _I	Input HIGH current	V _{DD} = Max V _{IN} = 5.3 V		2	1000	μA
I _{DD} ³	Power supply current	V _{DD} = Max		85	120	mA
V _I	Input clamp voltage	V _{DD} = Min I _{IN} = -18 mA		-0.70	-1.2	V

Table 4. Capacitance

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
C _{IN}	Input Capacitance	V _{IN} = 2.0 V at f = 1 MHz		6		pF
C _{OUT}	Output Capacitance	V _{OUT} = 2.0 V at f = 1 MHz		9		pF

Notes: 1. Typical limits are at V_{DD} = 5.0 V and T_A = 25°C.
 2. These are absolute values with respect to device ground and include all overshoots due to system or tester noise.
 3. This parameter is measured with device not switching and unloaded.

TQ2060

Table 5. AC Characteristics ($V_{DD} = +5 V \pm 5\%$, $T_A = 0\text{ }^\circ\text{C}$ to $+70\text{ }^\circ\text{C}$)

Symbol	Input Clock (REFCLK)	Test Conditions (Figure 5)	Min	Typ	Max	Unit
t_{CPWH}	CLK pulse width HIGH	Figure 5	4	—	—	ns
t_{CPWL}	CLK pulse width LOW	Figure 5	4	—	—	ns
t_{IR}	Input rise time (0.8 V – 2.0 V)		—	—	2.0	ns

Symbol	Output Clock (Q, QN)	Test Conditions (Figures 4 & 5) ¹	Min	Typ	Max	Unit
t_{OR} , t_{OF}	Rise/fall time (20% – 80%)	Figure 5	100	220	350	ps
t_{CYC}	Duty-cycle	Figure 5	45	50	55	%
t_{JP}^2	Period-to-Period Jitter		—	25	70	ps
t_{SYNC}^3	Synchronization Time		—	10	500	μs

- Notes: 1. All measurements are tested with a REFCLK having a rise time of 0.5 ns (0.8 V to 2.0 V).
 2. Jitter specification is peak to peak. Period-to-Period jitter is the jitter on the output with respect to the output's previous crossing.
 3. t_{SYNC} is the time required for the PLL to synchronize and assumes the presence of a CLK signal.

Figure 4. PECL Test Load

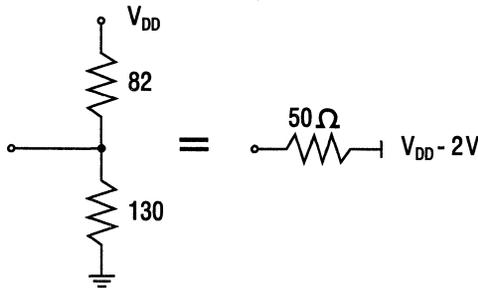


Figure 5. REFCLK and Q-QN Timing

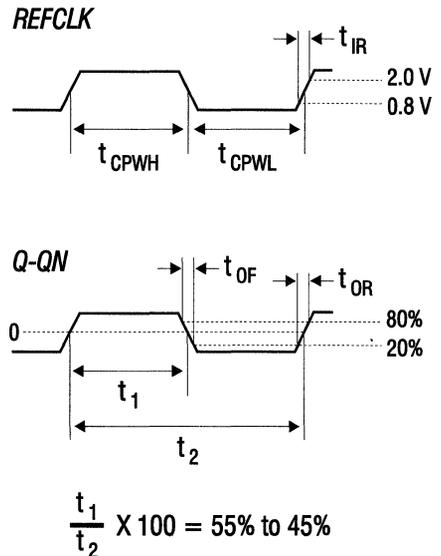
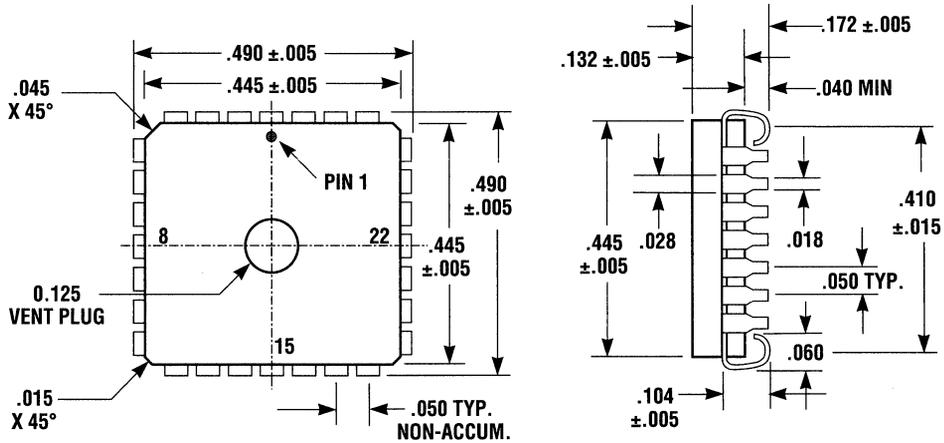


Figure 6. 28-Pin MQuad J-Leaded Package Mechanical Specification



(All dimensions in inches)

Table 6. 28-Pin MQuad Pin Description

Pin #	Pin Name	Description	I/O
1	NC	No Connect	—
2	NC	No Connect	—
3	NC	No Connect	—
4	NC	No Connect	—
5	NC	No Connect	—
6	NC	No Connect	—
7	GND	Ground	—
8	REFCLK	Reference Clock	I
9	TESTIN	Test Input	I
10	NC	No Connect	—
11	GND	Logic Ground	—
12	VDD	Logic VDD (+5 V)	—
13	NC	No Connect	—
14	TEST1	Test Control 1	I

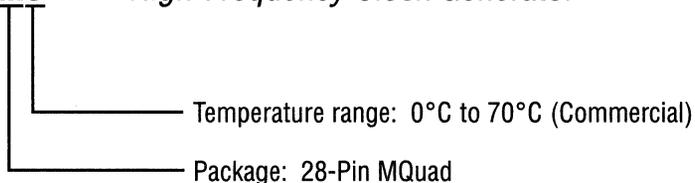
Pin #	Pin Name	Description	I/O
15	TEST2	Test Control 2	I
16	NC	No Connect	—
17	NC	No Connect	0
18	GND	Ground	—
19	EVDD	VDD for ECL Output (+5 V)	—
20	PDR2	Pull-down Resistor 2 (200 Ω)	I
21	QN	Differential PECL Output (-)	0
22	Q	Differential PECL Output (+)	0
23	PDR1	Pull-down Resistor 1 (200 Ω)	I
24	GND	Ground	—
25	AGND	Analog Ground	—
26	AVDD	Analog VDD (+5 V)	—
27	NC	No Connect	—
28	NC	No Connect	—

Ordering Information

To order, please specify as shown below:

TQ2060-MC

High-Frequency Clock Generator



Additional Information

For latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com Tel: (503) 615-9000

Email: sales@tqs.com Fax: (503) 615-8900

For technical questions and additional information on specific applications:

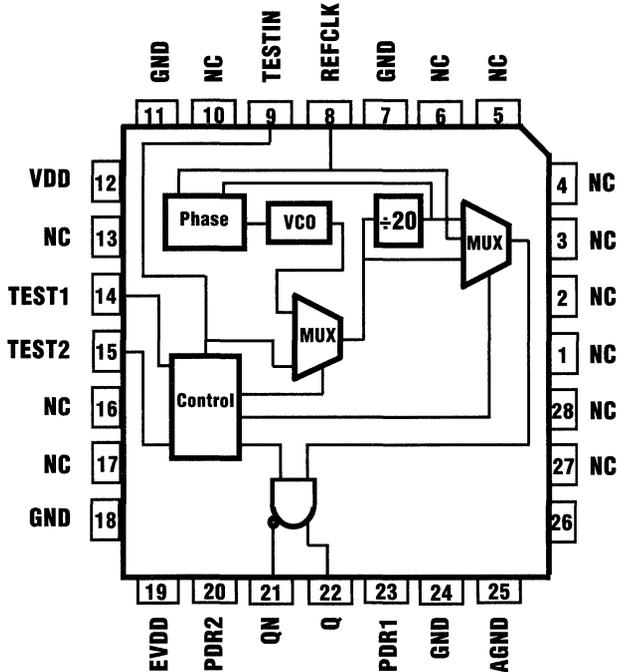
Email: applications@tqs.com

The information provided herein is believed to be reliable; TriQuint assumes no liability for inaccuracies or omissions. TriQuint assumes no responsibility for the use of this information, and all such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. TriQuint does not authorize or warrant any TriQuint product for use in life-support devices and/or systems.

Copyright © 1997 TriQuint Semiconductor, Inc. All rights reserved.

Revision 1.0.A October 1997

Figure 1. Pinout Diagram



TriQuint's TQ2061 is a high-frequency clock generator. It utilizes a 25 MHz to 35 MHz TTL input to generate a 500 MHz to 700 MHz PECL output. The TQ2061 has a completely self-contained Phase-Locked Loop (PLL) running at 500 MHz to 700 MHz. This stable PLL allows for a low period-to-period output jitter of 70 ps (max), and enables tight duty cycle control of 55% to 45% (worst case).

The TQ2061 provides optional 200-ohm on-chip pull-down resistors which are useful if the output is AC-coupled to the device being driven. In order to use these resistors, pin 20 (PDR2) should be connected to pin 21 (QN), and pin 23 (PDR1) should be connected to pin 22 (Q).

Various test modes on the chip simplify debug and testing of systems by slowing the clock output or by bypassing the PLL.

TQ2061

High-Frequency Clock Generator

Features

- Output frequency range:
500 MHz to 700 MHz
- One differential PECL output:
600 mV (min) swing
- Common-mode voltage:
 $V_{DD} - 1.2$ V (max),
 $V_{DD} - 1.6$ V (min)
- Period-to-period output jitter:
25 ps peak-to-peak (typ)
70 ps peak-to-peak (max)
- Reference clock input:
25 MHz to 35 MHz TTL-level
crystal oscillator
- Self-contained loop filter
- Optional 200 Ω pull-down
resistors for AC-coupled outputs
- +5 V power supply
- 28-pin J-lead surface-mount
package
- Ideal for designs based on DEC
Alpha AXP™ processors

Figure 2. Simplified Block Diagram

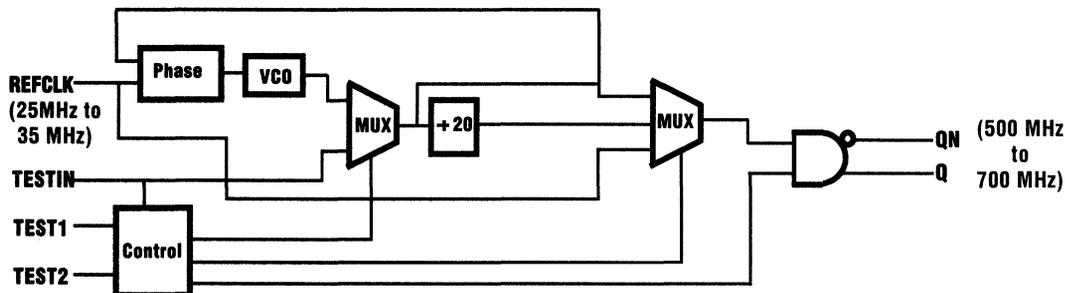


Table 1. Mode Selection

Mode	TEST1	TEST2	TESTIN ¹	REFCLK	Q, QN
1 (Test)	0	0	"don't care"	f_{REFCLK}	f_{REFCLK}^2
2 (Test)	0	1	"don't care"	"don't care"	0, 1
3 (Test)	1	0	$f_{TESTCLK}$	"don't care"	$f_{TESTCLK}$
4 (Bypass)	1	1	0	f_{REFCLK}	f_{REFCLK}
5 (Normal)	1	1	1	f_{REFCLK}	$20 \times f_{REFCLK}^3$

- Notes: 1. In mode 3, TESTIN may be used to bypass the PLL.
 2. REFCLK = 25 MHz to 35 MHz.
 3. Q, QN = 500 MHz to 700 MHz.

Figure 3. Recommended Layout
(Not to scale)

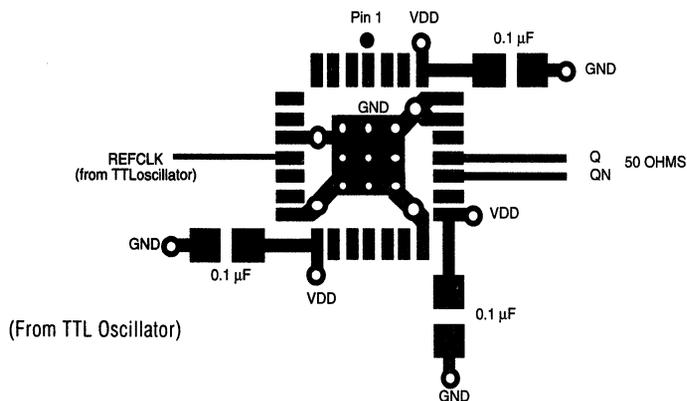


Table 2. Absolute Maximum Ratings

Storage Temperature	-65°C to +150°C
Ambient temperature with power applied	-55°C to +110°C
Supply voltage to ground potential	-0.5 V to +7.0 V
DC input voltage	-0.5 V to ($V_{DD} + 0.5$) V
DC input current	-30 mA to +5 mA
Package thermal resistance (MQuad)	$\theta_{JA} = 45^{\circ}\text{C/W}$
Die junction temperature	$T_J = 150^{\circ}\text{C}$

Note: Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device.
The device should be operated only under the DC and AC conditions shown below.

Table 3. DC Characteristics ($V_{DD} = +5\text{ V} \pm 5\%$, $T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$)¹

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH voltage	$V_{CC} = \text{Min PECL load}$	$V_{CC} - 1.20$		$V_{CC} - 0.50$	V
V_{OL}	Output LOW voltage	$V_{CC} = \text{Min PECL load}$	$V_{CC} - 2.00$		$V_{CC} - 1.60$	V
V_{CMO}	Output common mode voltage	PECL	$V_{CC} - 1.60$		$V_{CC} - 1.20$	V
V_{OUT}	Output differential voltage	PECL	0.6		1.2	V
V_{IH}^2	Input HIGH level	Guaranteed input logical HIGH Voltage for all inputs	2.0			V
V_{IL}^2	Input LOW level	Guaranteed input logical LOW Voltage for all inputs			0.8	V
I_{IL}	Input LOW current	$V_{DD} = \text{Max } V_{IN} = 0.40\text{ V}$		-150	-400	μA
I_{IH}	Input HIGH current	$V_{DD} = \text{Max } V_{IN} = 2.7\text{ V}$		0	25	μA
I_I	Input HIGH current	$V_{DD} = \text{Max } V_{IN} = 5.3\text{ V}$		2	1000	μA
I_{DDs}^3	Power supply current	$V_{DD} = \text{Max}$		85	120	mA
V_I	Input clamp voltage	$V_{DD} = \text{Min } I_{IN} = -18\text{ mA}$		-0.70	-1.2	V

Table 4. Capacitance

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 2.0\text{ V}$ at $f = 1\text{ MHz}$		6		pF
C_{OUT}	Output Capacitance	$V_{OUT} = 2.0\text{ V}$ at $f = 1\text{ MHz}$		9		pF

- Notes: 1. Typical limits are at $V_{DD} = 5.0\text{ V}$ and $T_A = 25^{\circ}\text{C}$.
2. These are absolute values with respect to device ground and include all overshoots due to system or tester noise.
3. This parameter is measured with device not switching and unloaded.

TQ2061

Table 5. AC Characteristics ($V_{DD} = +5\text{ V} \pm 5\%$, $T_A = 0\text{ }^\circ\text{C}$ to $+70\text{ }^\circ\text{C}$)

Symbol	Input Clock (REFCLK)	Test Conditions (Figure 5)	Min	Typ	Max	Unit
t_{CPWH}	CLK pulse width HIGH	Figure 5	4	—	—	ns
t_{CPWL}	CLK pulse width LOW	Figure 5	4	—	—	ns
t_{IR}	Input rise time (0.8 V – 2.0 V)		—	—	2.0	ns

Symbol	Output Clock (Q, QN)	Test Conditions (Figures 4 & 5) ¹	Min	Typ	Max	Unit
t_{OR}, t_{OF}	Rise/fall time (20% – 80%)	Figure 5	100	220	350	ps
t_{CYC}	Duty-cycle	Figure 5	45	50	55	%
t_{JP}^2	Period-to-Period Jitter		—	25	70	ps
t_{SYNC}^3	Synchronization Time		—	10	500	μs

Notes: 1. All measurements are tested with a REFCLK having a rise time of 0.5 ns (0.8 V to 2.0 V).
 2. Jitter specification is peak to peak. Period-to-Period jitter is the jitter on the output with respect to the output's previous crossing.
 3. t_{SYNC} is the time required for the PLL to synchronize and assumes the presence of a CLK signal.

Figure 4. PECL Test Load

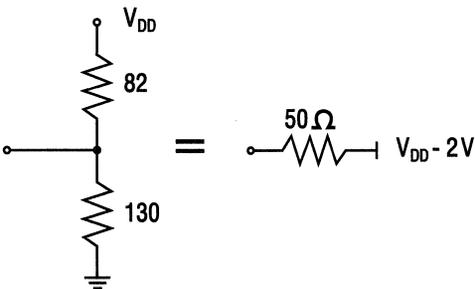


Figure 5. REFCLK and Q-QN Timing

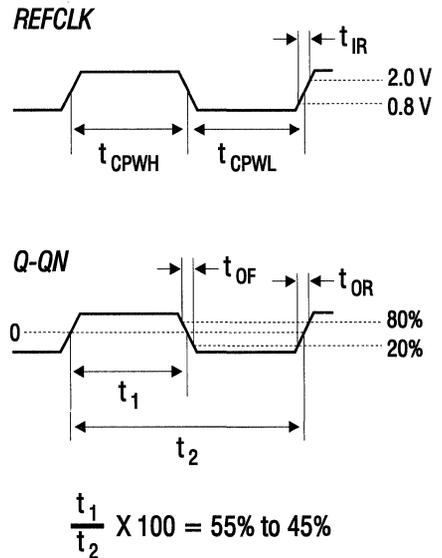
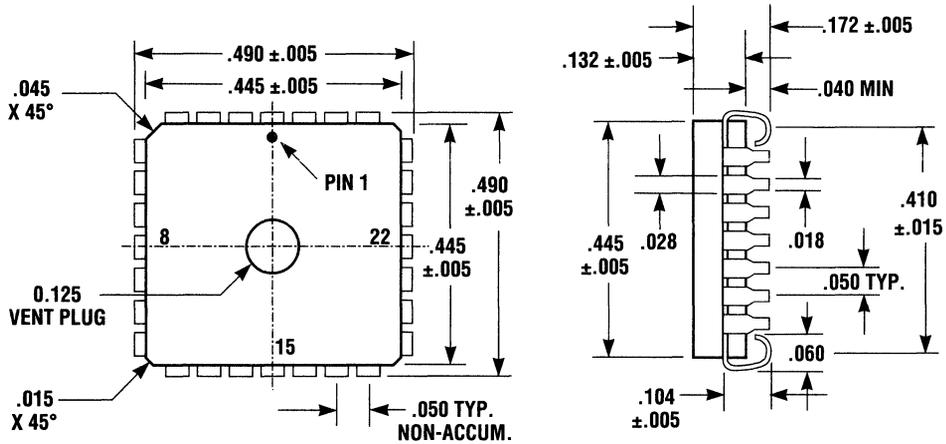


Figure 6. 28-Pin MQuad J-Leaded Package Mechanical Specification



(All dimensions in inches)

Table 6. 28-Pin MQuad Pin Description

Pin #	Pin Name	Description	I/O
1	NC	No Connect	—
2	NC	No Connect	—
3	NC	No Connect	—
4	NC	No Connect	—
5	NC	No Connect	—
6	NC	No Connect	—
7	GND	Ground	—
8	REFCLK	Reference Clock	I
9	TESTIN	Test Input	I
10	NC	No Connect	—
11	GND	Logic Ground	—
12	VDD	Logic VDD (+5 V)	—
13	NC	No Connect	—
14	TEST1	Test Control 1	I

Pin #	Pin Name	Description	I/O
15	TEST2	Test Control 2	I
16	NC	No Connect	—
17	NC	No Connect	0
18	GND	Ground	—
19	EVDD	VDD for ECL Output (+5 V)	—
20	PDR2	Pull-down Resistor 2 (200 Ω)	I
21	QN	Differential PECL Output (-)	0
22	Q	Differential PECL Output (+)	0
23	PDR1	Pull-down Resistor 1 (200 Ω)	I
24	GND	Ground	—
25	AGND	Analog Ground	—
26	AVDD	Analog VDD (+5 V)	—
27	NC	No Connect	—

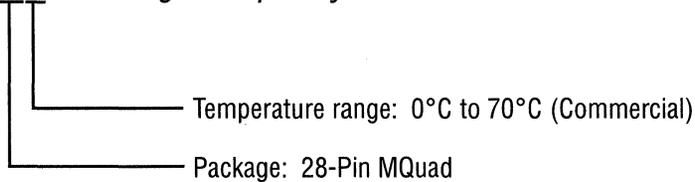
SYSTEM TIMING PRODUCTS

Ordering Information

To order, please specify as shown below:

TQ2061-MC

High-Frequency Clock Generator



Additional Information

For latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com Tel: (503) 615-9000
Email: sales@tqs.com Fax: (503) 615-8900

For technical questions and additional information on specific applications:

Email: applications@tqs.com

The information provided herein is believed to be reliable; TriQuint assumes no liability for inaccuracies or omissions. TriQuint assumes no responsibility for the use of this information, and all such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. TriQuint does not authorize or warrant any TriQuint product for use in life-support devices and/or systems.

Copyright © 1997 TriQuint Semiconductor, Inc. All rights reserved.

Revision 1.0.A October 1997



Section 7 — Application Notes

<i>Making High-Speed Measurements</i>	<i>7-3</i>
<i>Layout Principles for High-Speed Serial Data</i>	<i>7-7</i>
<i>Termination Schemes for Fibre Channel Tx/Rx Interfaces</i>	<i>7-11</i>
<i>Transmission Line Fundamentals</i>	<i>7-17</i>
<i>Terminating Clock Lines</i>	<i>7-21</i>
<i>Interfacing 5-Volt Clock Chips to 3-Volt ICs</i>	<i>7-31</i>
<i>Part-to-Part Skew</i>	<i>7-35</i>
<i>Clock Distribution Techniques Using the GA1110E</i>	<i>7-43</i>

Making High-Speed Measurements

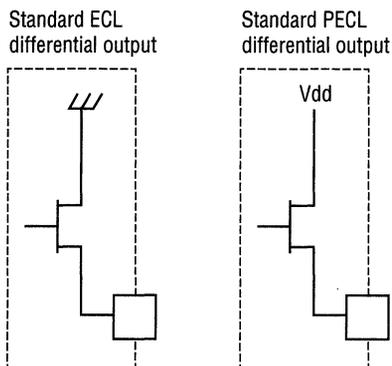
Much has been written about the critical nature of accurate high speed measurement. This application note is intended to be a supplement and aid in the process of making high-speed measurements quickly and accurately. Measurement of TriQuint ECL and PECL outputs are of particular interest, especially as they pertain to measurement in TriQuint's family of evaluation fixtures.

ECL and PECL Outputs at TriQuint

The standard TriQuint ECL output device is essentially an "open" source follower circuit. Current flows out of the source from the drain which is at "ground."

A PECL or positive ECL output is also an "open" source follower circuit. Current flows out of the source from the drain which is connected, instead, to the Positive Vdd power supply.

Figure 1. ECL and PECL Outputs



Measuring Differential ECL and PECL Outputs

To make single-ended measurements on differential outputs, attention should be given to the differential output interface. Both outputs must be terminated identically for optimum performance (the complement output should be terminated with an equivalent 50 ohms to $-2V$).

ECL Terminators

ECL signals are normally offset from ground. High-frequency test equipment generally provides a 50-ohm termination to ground. Direct connection of such signals to this test equipment could result in damage to the equipment.

An ECL terminator provides the interface between the ECL output and the test and measurement equipment. It will offset and attenuate the signal such that the equipment remains protected. High-bandwidth ECL terminators allow signals with rise times as small as 100 ps to be attenuated and observed without distortion.

ECL terminator products are available from at least two sources, as listed in the following table.

<i>Vendor</i>	<i>Model #</i>
Picosecond Pulse Labs	5620
Cascade Microtech	ECL-T1

TriQuint Evaluation Fixtures

When observing signals from circuits fixtured in TriQuint evaluation fixtures, it is crucial that special care be taken to terminate adjacent signal paths through 50 ohms to "ground." This eliminates any energy which may inadvertently couple into and reflect back to the signal under observation. If this is not done, the effect can be a small but noticeable perturbation of the observed signal at a location equal to the electrical length of the neighboring signal path.

Figure 2 shows an example of the way an ECL output interfaces to the ECL terminator and the scope. Figure 3 shows a setup for measuring PECL outputs.

All cables should be high-quality shielded 50-ohm type and cable lengths should be as short as is practical in the test lab environment.

Figure 2. Measuring ECL Outputs

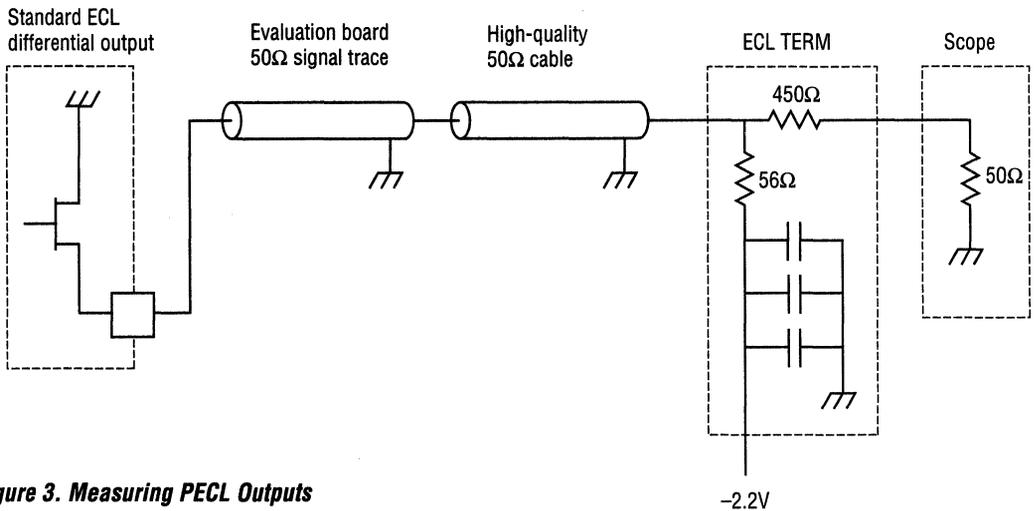
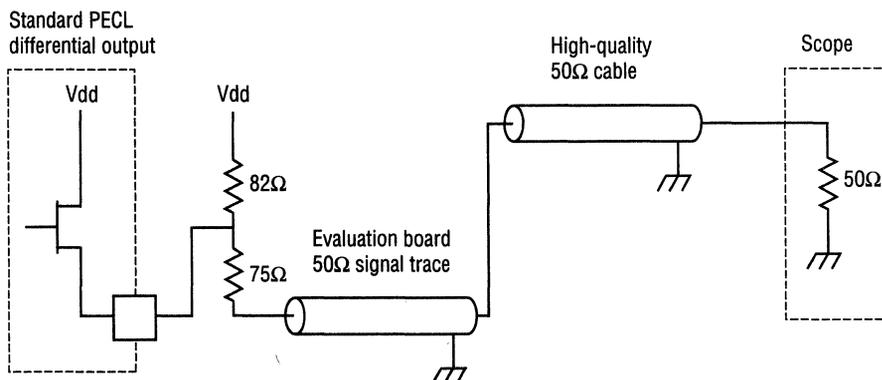
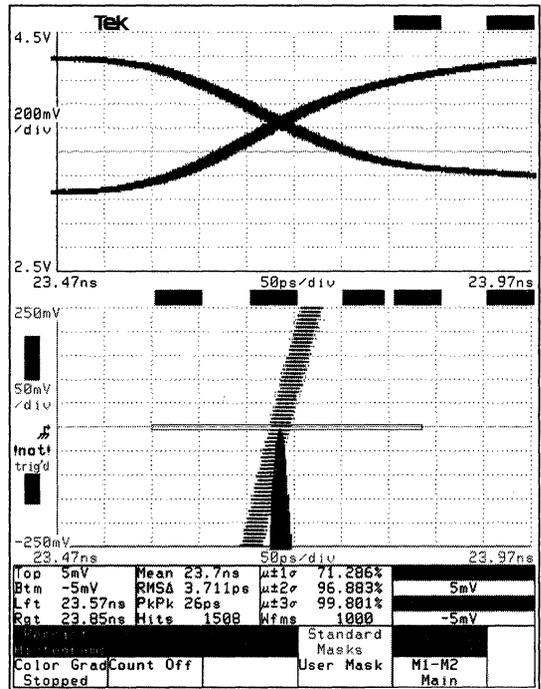


Figure 3. Measuring PECL Outputs



The ECL terminator should be connected directly to the 50 ohm scope input, and the scope should be a high-bandwidth sampling scope. For example, to measure a 100 ps rise time, the bandwidth of the scope must be at least 5GHz.

Figure 4. Typical Oscilloscope Image



APPLICATION NOTES

High-Speed Measurements

Additional Information

For latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com **Tel:** (503) 615-9000
Email: sales@tqs.com **Fax:** (503) 615-8900

For technical questions and additional information on specific applications:

Email: applications@tqs.com

The information provided herein is believed to be reliable; TriQuint assumes no liability for inaccuracies or omissions. TriQuint assumes no responsibility for the use of this information, and all such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. TriQuint does not authorize or warrant any TriQuint product for use in life-support devices and/or systems.

Copyright © 1997 TriQuint Semiconductor, Inc. All rights reserved.

Revision 1.0.A October 1997

Layout Principles for High-Speed Serial Data

This application note provides information to aid in the design and layout of printed circuitry for high-speed serial link applications. These design principles will help achieve successful operation at high data transfer rates.

Introduction

RF design principles must be factored into the design and implementation of systems that utilize high-speed serial architectures to transmit data at gigabit rates.

All high-speed data lines must be treated as controlled, constant-impedance transmission lines. They should be routed in a straight-line fashion as either stripline or microstrip signals.

The recommended method is to route data lines between power and ground layers (stripline). External layer routing (microstrip) is acceptable but stripline routing provides significant electromagnetic shielding which minimizes the radiative effects of the signals.

Skin effects have a much larger impact at these higher data rates. For this reason sharp bends, feed-through vias and any other sources of impedance discontinuity must be avoided if at all possible.

High-Speed Signal Trace Characteristics

Trace width and lamination thickness are the large determining factors of trace impedance. Long narrow traces will be more susceptible to impedance variations which will affect signal transmission quality. Wider traces will have less variation and therefore offer a higher transmission quality.

Trace separation must be considered to achieve a minimum radiating loop area for differential signal traces. This area is directly proportional to the trace separation. A trade-off has to be made between the need for minimum trace-to-trace capacitive coupling and the desired characteristic trace impedance.

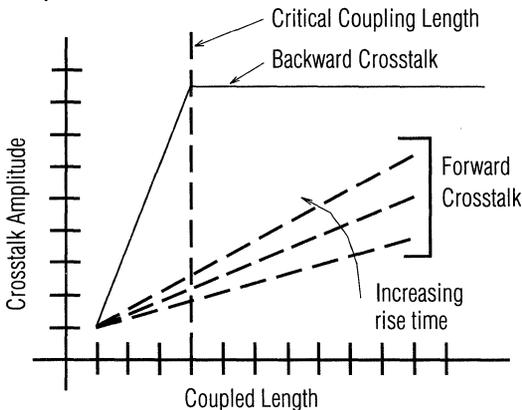
Capacitive coupling and characteristic impedance are inversely affected by trace separation. The general rule for edge-to-edge spacing is 2.5 times the width of the trace. Another method for providing enhanced isolation between traces, for the purpose of minimizing crosstalk, is to run a ground trace between the traces of concern. This must be evaluated as to its impact on radiating emissions.

Layout for High-Speed Data

Signal Coupling

Signal coupling can have a substantial impact on the noise generated in a gigabit signal line. There are at least two sources of coupling: capacitive coupling occurs when traces are routed over the top of the trace in question; inductive coupling occurs when traces are routed closely parallel (side-by-side) to the trace in question.

Factors affecting the amount of coupling are the distance from the trace to the power planes, the spatial separation of the traces and the length of the parallelism.

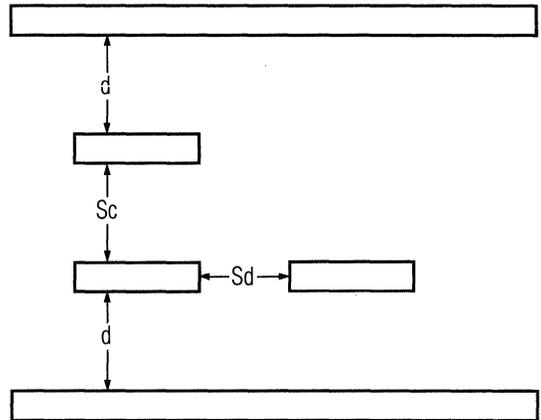


The magnitude of the inductive coupling between two parallel traces is the ratio of the spatial separation (S_d) to the distance (d) from the trace to the power / ground plane. The magnitude of the capacitive coupling between two overlapping traces is the ratio of the spatial separation (S_c) to the distance (d) from the trace to the power / ground plane.

If $\{S_d / d\} \cong \{S_c / d\} \cong 1$, then the coupling factor will be approximately 15% to 20% of the incident signal amplitude. If this ratio is increased to 2, the coupling factor will be reduced to approximately 5% to 10%. If this ratio is further increased to 3, the coupling factor will again be reduced to approximately 2% to 5%.

Coupling Ratio	Coupling Energy
1	15 - 20%
2	5 - 10%
3	2 - 5%

All traces in a high speed design should be widely separated (ratio 3) to minimize the noise on a high speed signal trace.



Signal Trace Crosstalk

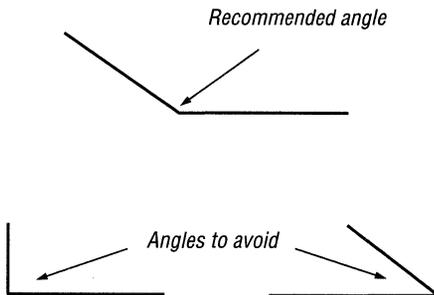
Every high-speed signal will be imaged in the ground plane by an equal return current. This return current will flow in a path of smallest impedance (and usually shortest distance spatially) on its return to the signal source. Running the traces over a ground plane already reduces the crosstalk by about 90%. The remaining 10% can be minimized by reducing the parasitic coupling capacitance mentioned above. The separation distance between traces determines the parasitic coupling capacitance.

There are two cases to be considered when thinking about crosstalk and there are several ways to handle these cases. The two cases are crosstalk between

unrelated signals and crosstalk in traces carrying a differential signal. For the case of differential signal traces, a ground trace which separates the differential traces can virtually eliminate differential crosstalk. For the case of unrelated signals, the parasitic capacitance and hence the spatial distance between traces is the only means of reducing the crosstalk.

Impedance Discontinuities

Trace routing should be carefully planned to provide for a smooth circuit flow with minimal interruptions. Every impedance discontinuity is a source of both signal reflections and of radiated emissions. The control of these factors can be achieved by minimizing the number and severity of impedance discontinuities and sharp corners (i.e. sharper than 135 degrees).



One common source of impedance discontinuity is a feed-through via. A feed-through via can add as much as 4 pF of parasitic capacitance unless the feed-through via structure is designed to minimize excess capacitance. Carefully selected placement and routing of components in the layout can help to greatly minimize feed-through vias.

If feed-through vias are unavoidable in high frequency gigabit signal paths, the parasitic capacitance of the via should be minimized to avoid an impedance discontinuity in the controlled impedance path. This is done by a careful design of the feed-through via to make its characteristic impedance look very similar to that of the trace. The following table shows the dimensional effect of the via on parasitic capacitance.

<i>Via Element</i>	<i>Low Cost Via</i>	<i>Recommended RF Via</i>
Hole	0.018"	0.010"
Pad	0.030"	0.020"
Relief	0.060"	0.100"
Capacitance	2 – 4 pF	1 – 2 pF

Another source of impedance discontinuity is the contact pad of a surface-mount device such as an AC coupling capacitor or a series terminating resistor. The effect on the impedance discontinuity can be minimized by distancing the closest "ground" plane from the contact pad. Routing of other signals through the areas where the ground plane has been altered must be avoided.

Signal Trace Skin Effects

As serial link data rates approach 1Gb/s, skin effects begin to dominate, making the surface area of the trace extremely important.

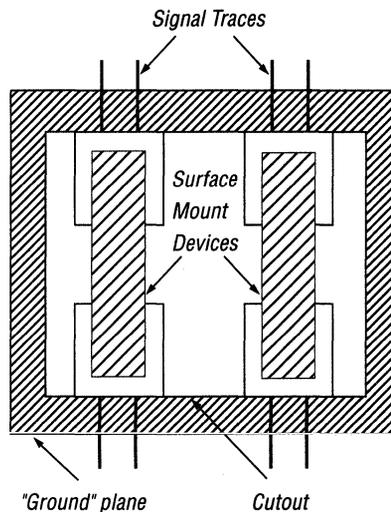
Skin depth is defined as the depth in a conductor at which the current is attenuated by a factor of e (2.718295) from its surface value. The following table is a comparative chart of skin depths at various frequencies.

Layout for High-Speed Data

Frequency	Skin Depth in mils
1 KHz	83
1 MHz	2.6
10 MHz	0.83
100 MHz	0.26
1 GHz	0.083

The skin depth δ is inversely proportional to the square root of the frequency. The distribution of current in the trace is exponential, dropping to very nearly zero after some 6 to 9 skin depths.

If the trace thickness is greater than $(6 * \delta)$ at the frequency of concern, the trace impedance will not change appreciably.



Additional Information

For latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com **Tel:** (503) 615-9000
Email: sales@tqs.com **Fax:** (503) 615-8900

For technical questions and additional information on specific applications:

Email: applications@tqs.com

The information provided herein is believed to be reliable; TriQuint assumes no liability for inaccuracies or omissions. TriQuint assumes no responsibility for the use of this information, and all such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. TriQuint does not authorize or warrant any TriQuint product for use in life-support devices and/or systems.

Copyright © 1997 TriQuint Semiconductor, Inc. All rights reserved.

Revision 1.0.A October 1997

Termination Schemes for Fibre Channel Tx/Rx Interfaces

Interfaces to TriQuint Fibre Channel transmitter and receiver devices can have a significant impact on the performance of the Fibre Channel Link in which they are placed. Careful design of these interfaces will eliminate the link as a problem source during the system debug phase. This application note discusses the various interfaces which need to be considered carefully during the system design and layout phases. Several termination schemes are shown to give a basic understanding of the types of schemes that are available.

Introduction

TriQuint Fibre Channel devices are a very high-speed serial communication interface solution. Interfacing to these serial link chips is critical when the maximum transfer rate is desired. Fibre Channel Transmission rates are now commonly being implemented into systems with the intention of full-rate 1.063 Gb/s operation. The link side of a Fibre Channel transmitter / receiver carries PECL-level data at rates between 1 and 1.25 Gb/s. Careful attention should be given to the design and layout of this link to avoid problems caused by improper termination impedance or voltage.

When interfacing to copper links or optical drivers, care must be taken to ensure that the interface to these devices is well matched, and that the impedance characteristics are maintained in order to minimize possible noise sources. Another important factor which must not be overlooked is the 10-bit TTL bus interface

between the transmitter / receiver and the Encoder / Decoder (ENDEC) to which they interface. Data rates at these interfaces can reach speeds as high as 125 Mb/s. At these interfaces great care must be taken to make sure signals remain as noise-free as possible.

The Transmitter I/O Interface

Normally, for a short link, the Transmitter (TX) is connected directly to either the copper link or to an optical driver device. For copper links, if the length of the link is greater than 20 feet, then a Line Driver Amplifier or equalized cable scheme is preferred. Interfacing circuitry should be such that the impedance seen looking out of the Transmitter is 50 ohms, with a termination voltage of 3 V.

The configurations shown in the figures on the following pages provide several examples of a balanced 50-ohm interface, as well as a specific example in which a particular line driver is shown. The resistor network is constructed such that the output of the TX is terminated into +3 V. There is a 4:1 attenuation of the signal going to the Line Driver Amplifier and the impedance looking back from the Line Driver Amplifier is also 50 ohms.

In the case of the differential interface, the lines out of the Line Driver Amplifier are AC-coupled to the coaxial cable. For the single-ended case, the Complement line out of the Line Driver Amplifier is AC-coupled to a 50-ohm resistor, which is tied to ground. The True side is

Termination for Fibre Channel

AC-coupled to the coaxial cable. This applies to circuits in which just the TX is used as the driver.

The Receiver I/O Interface

The Receiver interface is susceptible to losses along a copper link. These losses can be minimized by using a Line Driver Amplifier at the receiver end of the link. When interfacing to the receiver it is important to note that a PECL receiver input wants to see a 50-ohm source impedance. It is also important to ensure that

the input bias is set to the PECL logic threshold of +3.7 V. An AC-coupled signal then swings symmetrically about this threshold. The figure below shows a balanced 50-ohm input termination scheme which sets the input level (+3.68 V) at or near the PECL logic threshold. If the link is single-ended, the True side of the Line Driver Amplifier is AC-coupled to ground and the Complement side of the Line Driver Amplifier is AC-coupled to the Link. If the Link is differential, then both sides of the link are AC-coupled to the Line Driver Amplifier.

Figure 1. Fibre Channel Transmitter Coaxial Interface

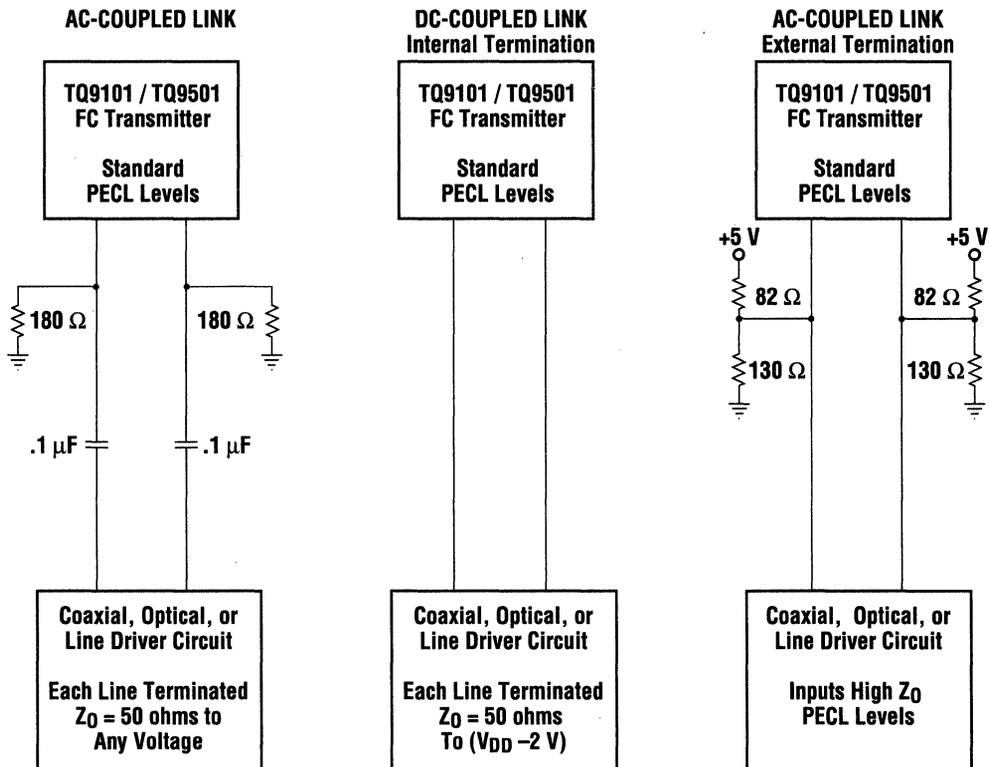
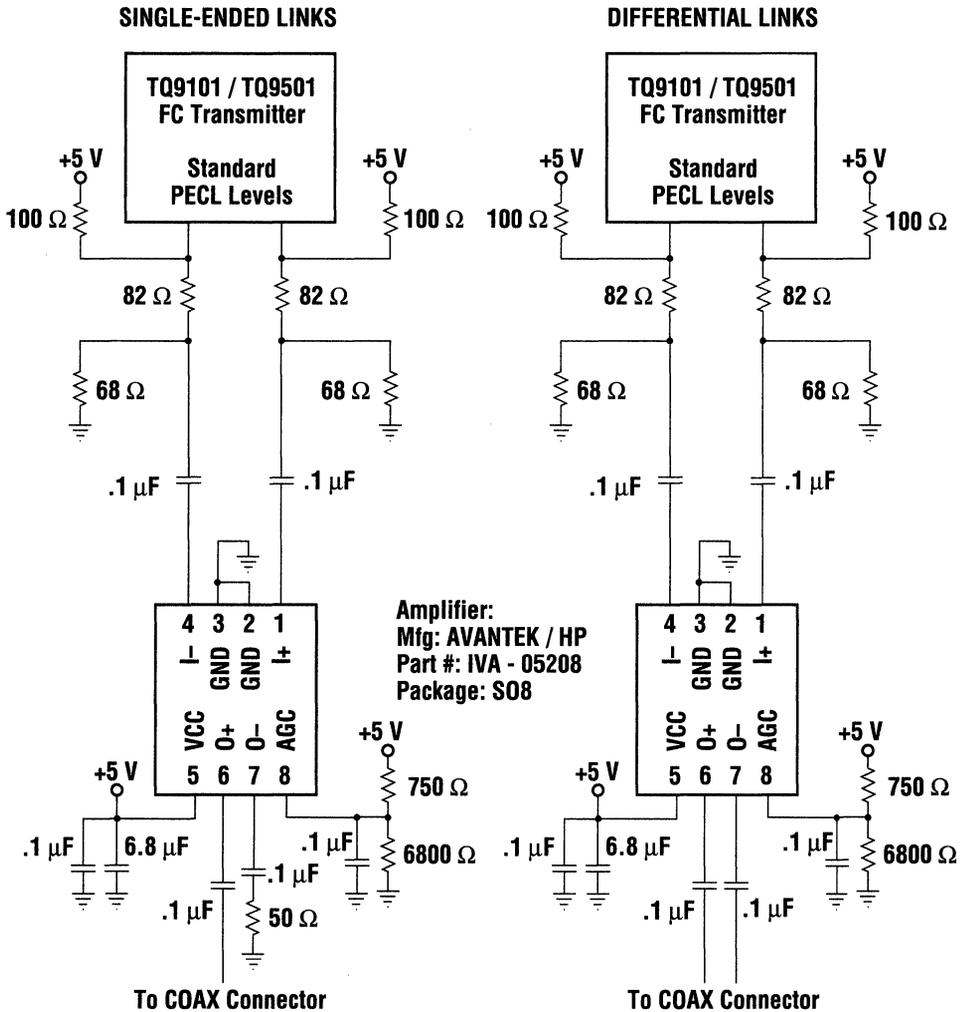


Figure 2. Fibre Channel Transmitter Coaxial Interface with Line Driver Amplifier



APPLICATION NOTES

Termination for Fibre Channel

Figure 3. Fibre Channel Receiver Coaxial Termination Interface

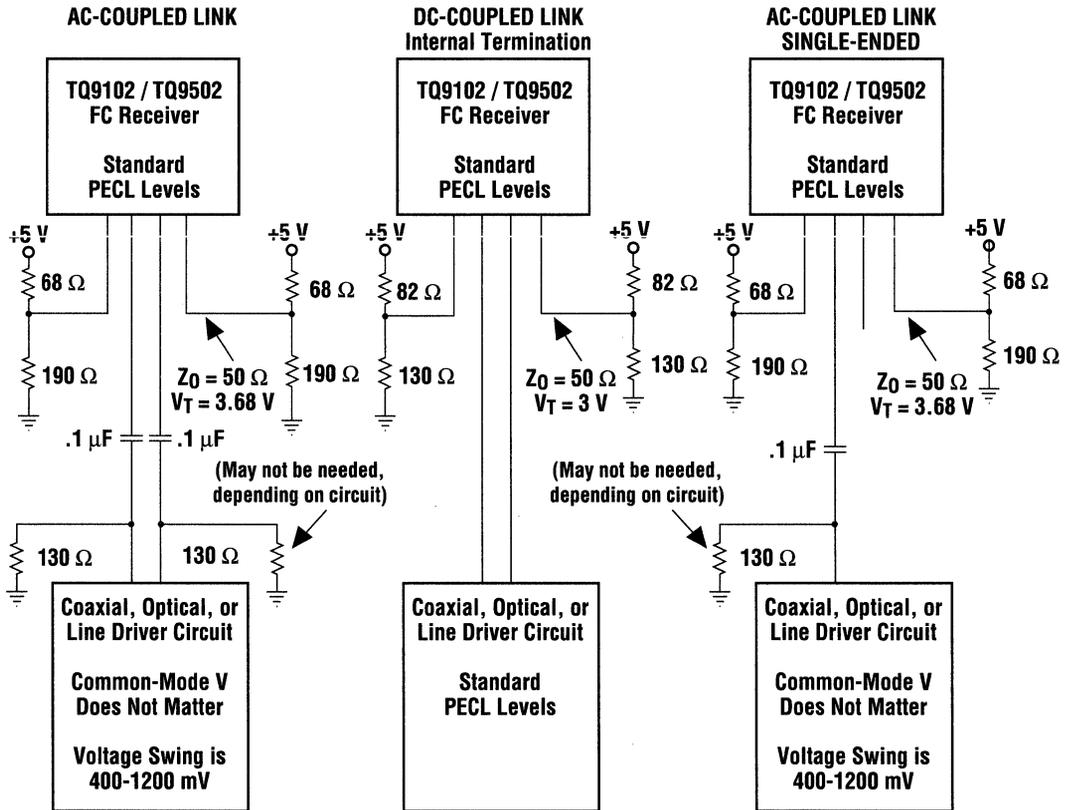
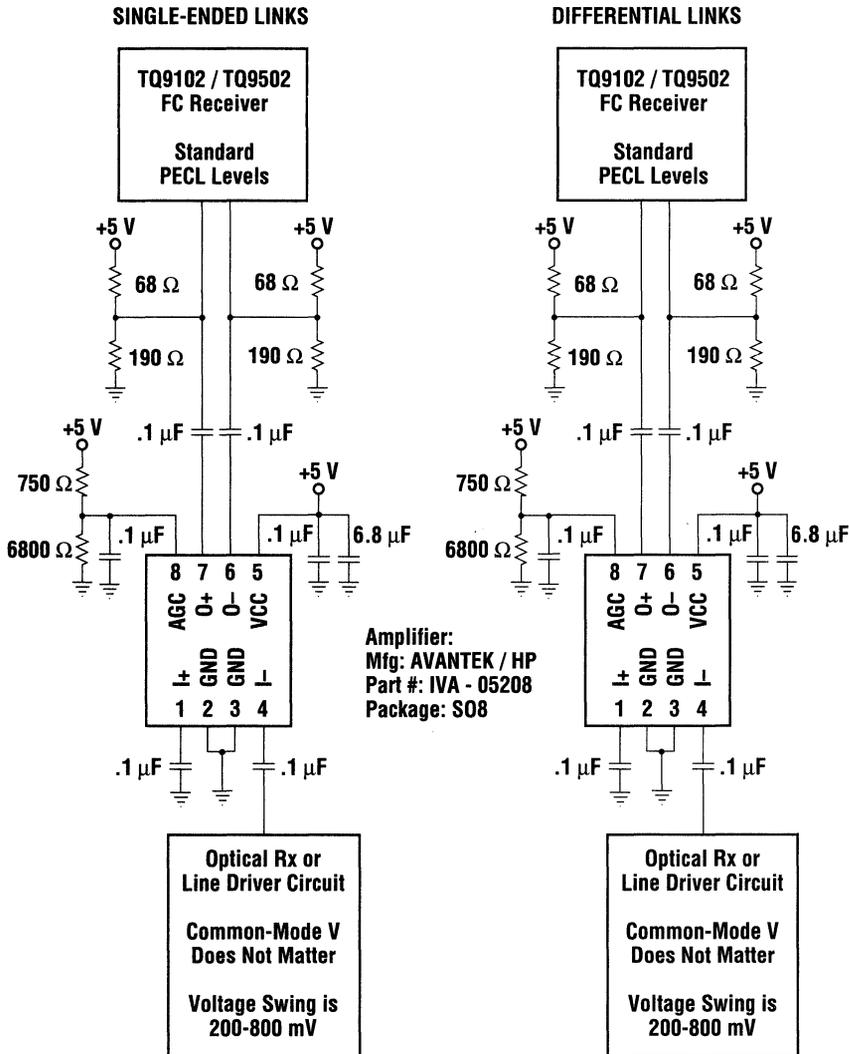


Figure 4. Fibre Channel Receiver Coaxial Interface with Line Driver Amplifier



APPLICATION NOTES

Termination for Fibre Channel

Additional Information

For latest specifications, additional product information,
worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com **Tel:** (503) 615-9000
Email: sales@tqs.com **Fax:** (503) 615-8900

For technical questions and additional information on specific applications:

Email: applications@tqs.com

The information provided herein is believed to be reliable; TriQuint assumes no liability for inaccuracies or omissions. TriQuint assumes no responsibility for the use of this information, and all such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. TriQuint does not authorize or warrant any TriQuint product for use in life-support devices and/or systems.

Copyright © 1997 TriQuint Semiconductor, Inc. All rights reserved.

Revision 1.0.A October 1997

Transmission Line Fundamentals

Introduction

A knowledge of transmission lines is critical when designing high-speed systems. Signal edge rates define the transition point where simple traces become transmission lines. As CPU data rates increase, edge rates get faster to keep up with the increase in frequency, which, in turn, worsens the transmission line effects.

By correctly identifying transmission lines and by designing the printed circuit board to address transmission line effects, a designer can prevent problems before the boards are manufactured.

Transmission Line Theory

A transmission line has a characteristic impedance (Z_0) and propagation delay (t_{P0}), which is given by:

$$Z_0 = \sqrt{\frac{L_0}{C_0}} \quad (\Omega) \quad (1)$$

$$t_{P0} = \sqrt{L_0 C_0} \quad \left(\frac{\text{ps}}{\text{in.}} \right) \quad (2)$$

Where C_0 = intrinsic capacitance
 L_0 = intrinsic inductance

The delay through the transmission line is given by:

$$t_{PD} = t_{P0} (\text{ps/in.}) \times l (\text{inches}) \quad (3)$$

Where l = the length of the transmission line.

The transmission line impedance decreases and the propagation delay increases with capacitive loading, as shown in Equations 4 and 5:

$$Z_L = \frac{Z_0}{\sqrt{1 + \frac{C_L}{C_0}}} \quad (\Omega) \quad (4)$$

$$t_{PL} = t_{P0} \sqrt{1 + \frac{C_L}{C_0}} \quad \left(\frac{\text{ps}}{\text{in.}} \right) \quad (5)$$

where Z_L = loaded impedance
 C_L = load capacitance
 t_{PL} = loaded propagation delay in ps/in

Whether or not a printed circuit board trace acts as a transmission line, exhibiting a characteristic impedance and propagation delay, depends upon the signal edge rates relative to the round-trip delay of the trace. Although faster signal frequencies tend to exacerbate transmission line effects, it is the signal edges, and not frequency, that define a transmission line.

A trace is determined to be a transmission line if it meets this criterion:

$$t_{R,F} < 2t_{PD} \quad (\text{ps}) \quad (6)$$

Where $t_{R,F}$ = edge rates, or rise and fall times in ps
 t_{PD} = one-way delay in ps
 $2t_{PD}$ = round-trip delay in ps

Transmission Lines

If the edge rates of the signal are less than the round-trip delay of the trace, the trace must be treated as a transmission line. For example, at what length will a trace having a propagation delay of 172 ps per inch begin exhibiting transmission line characteristics, assuming the signal has a minimum edge rate of 350 ps?

The GA1085, for example, has a minimum output rise time t_{OR} and fall time t_{OF} of 350 ps. Substituting the edge rates into equation 6 yields the following:

$$t_{R,F} \leq 2t_{PD} \quad (\text{From Equation 6})$$

$$t_{PD} \geq \frac{t_{R,F}}{2}$$

$$l * t_{PO} \geq \frac{t_{R,F}}{2}$$

$$l \geq \frac{t_{R,F}}{2t_{PO}} \quad (6)$$

$$l \geq \frac{350 \text{ ps}}{2(172 \text{ ps/in})}$$

$$l \geq 1.02 \text{ inches}$$

In this example, a trace longer than 1.02 inches is a transmission line. Traces shorter than 1.02 inches are not transmission lines and are treated as lumped loads.

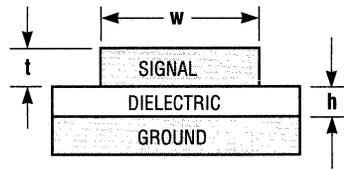
Microstrip Lines

The top and bottom signal layers of most printed circuit boards are microstrip lines. A microstrip line sits above a ground plane separated by a dielectric, as shown in Figure 1. The traces are copper and the dielectric is normally composed of resin epoxy fiberglass. The copper ground plane enables good impedance control. For a microstrip line, the characteristic impedance is given by the following equation:

$$Z_0 = \frac{87}{\sqrt{\epsilon_r + 1.41}} \ln \left(\frac{5.98 h}{0.8 w + t} \right) (\Omega) \quad (7)$$

Where ϵ_r = dielectric constant (FR-4/Glass = 4.1)
 t = trace thickness (1 oz. = 0.0015", 2 oz. = 0.003")
 w = trace width (mils)
 h = dielectric insulation (mils)

Figure 1. Microstrip Cross Section



The trace width (w) and height (h) are chosen to achieve the desired impedance.

The propagation delay for a microstrip line is given by:

$$t_{PO} = 84.75 \sqrt{0.475 \epsilon_r + 0.67} \left(\frac{\text{ps}}{\text{in.}} \right) \quad (8)$$

For example, a board with a dielectric constant of 4.1 will have a propagation delay given by:

$$t_{PO} = 84.75 \sqrt{0.475(4.1) + 0.67} \left(\frac{\text{ps}}{\text{in.}} \right)$$

$$t_{PO} = 137 \left(\frac{\text{ps}}{\text{in.}} \right)$$

Note that the propagation delay depends solely on the material of the dielectric, and not upon the geometry.

Strip Lines

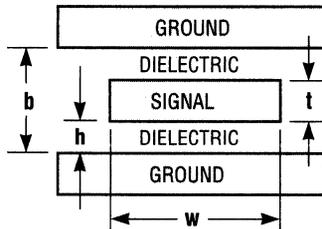
Strip lines are found in the inner layer of the board, sandwiched between two ground planes, as shown in Figure 2. For a strip line, the characteristic impedance is given by:

$$Z_0 = \sqrt{\frac{60}{\epsilon_r}} \ln \left(\frac{4b}{0.67 \pi w (0.8 + \frac{t}{w})} \right) \quad (9)$$

Where ϵ_r = dielectric constant
 t = trace thickness
 w = trace width
 h = dielectric insulation
 b = spacing between ground planes

Arriving at the desired impedance depends upon the correct combination of trace width (w), height (h), and ground plane spacing (b).

Figure 2. Strip Line Cross Section



The propagation delay for strip lines is given by :

$$t_{PO} = 84.75 \sqrt{\epsilon_r} \left(\frac{\text{ps}}{\text{in.}} \right) \quad (10)$$

It is interesting to note that signals move more slowly in a stripline than a microstrip for a given dielectric constant, which is apparent from comparing Equations 8 and 10.

Reflections

Reflections are well understood transmission line effects. They are sometimes misidentified as ringing, because they exhibit similar characteristics. Reflections appear whenever a signal encounters a mismatch in impedance. The impedance mismatch may be the result of a difference in trace geometry, capacitive loading on the trace (described in Equation 4), or improperly terminated traces. The reflection coefficient is given by:

$$\rho = \frac{Z_2 - Z_1}{Z_2 + Z_1} \quad (11)$$

Where ρ = reflection coefficient
 Z_1 = segment 1 impedance
 Z_2 = segment 2 impedance

Figure 3 shows a step generator driving a transmission line. The output impedance of the step generator is R_{OUT} . Various reflection coefficients are shown at Points A and B in the waveforms in Figure 4. When the reflection coefficient is zero, there are no reflections.

Figure 3. Impedance Mismatch

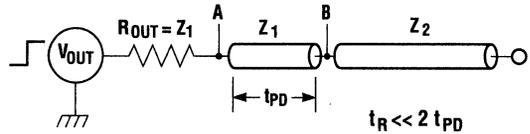
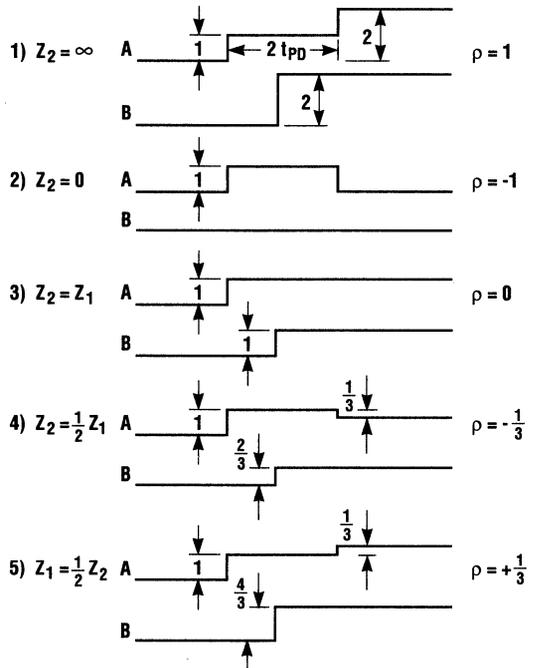


Figure 4. Reflection Waveforms

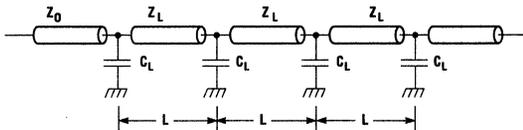


Transmission Lines

Daisy Chaining

The distributed capacitive loading on a trace as a result of daisy-chaining devices, shown in Figure 5, decreases the effective impedance of a trace, as described in Equation 5.

Figure 5. Daisy Chaining



All of the transmission line segments in Figure 5 have an initial impedance of Z_0 ; the loaded impedance is Z_L .

As an example, assume the following:

$$\begin{aligned} Z_0 &= 70 \Omega \\ C_0 &= 5 \frac{\text{pF}}{\text{in.}} \\ \left. \begin{aligned} C_L &= 5 \text{ pF} \\ L &= 1 \text{ inch} \end{aligned} \right\} &= 5 \frac{\text{pF}}{\text{in.}} \end{aligned}$$

Calculate Z_L :

$$\begin{aligned} Z_L &= \sqrt{1 + \frac{C_L}{C_0} \frac{Z_0^2}{L^2}} \\ &= \sqrt{1 + \frac{5 \text{ pF/in.}}{2.5 \text{ pF/in.}} \frac{(70 \Omega)^2}{(1 \text{ in.})^2}} \\ Z_L &= 40 \Omega \end{aligned} \quad (4)$$

Calculate t_{PL} :

$$\begin{aligned} t_{PL} &= t_{P0} \sqrt{1 + \frac{C_L}{C_0} \left(\frac{\text{ps}}{\text{in.}} \right)} \quad (5) \\ t_{PL} &= 137 \text{ ps/in.} \sqrt{1 + \frac{5 \text{ ps/in.}}{2.5 \text{ ps/in.}}} \\ t_{PL} &= 237 \text{ ps/in.} \end{aligned}$$

The impedance drops from 70 ohms to 40 ohms as a result of capacitive loading. While the propagation delay increases from 137 ps/in to 237 ps/in when loaded, changes in the characteristics of the line must be considered when driving multiple inputs along a trace.

Summary

Do not overlook the importance of transmission line effects when designing high-speed systems. By knowing the trace impedance, the designer can properly terminate the line. Knowing the trace propagation delay enables the designer to effectively manage the timing requirements of the system.

References

1. "Terminating Clock Lines," Joel Martinez, TriQuint Semiconductor, Inc., 1993
2. *MECL System Design Handbook*, Motorola, 1988
3. *ECL in PS Design Guide*, Motorola, 1991

The information provided herein is believed to be reliable; TriQuint assumes no liability for inaccuracies or omissions. TriQuint assumes no responsibility for the use of this information, and all such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. TriQuint does not authorize or warrant any TriQuint product for use in life-support devices and/or systems.

Copyright © 1997 TriQuint Semiconductor, Inc. All rights reserved.

Revision 1.0.A October 1997

Terminating Clock Lines

Introduction

The clock distribution circuitry is the heart of any system and requires special attention. Unterminated or improperly terminated lines may cause havoc in a system. Improper line termination results in uncontrolled reflections which can cause false triggering, induce Electro-Magnetic Interference (EMI) and generate noise in the system. The requirement for proper termination stems from the transmission line characteristics of traces in high-speed designs. Essentially, traces become transmission lines, exhibiting transmission line characteristics, (reflections, in particular).

Clock Line Terminations

When does a signal trace require termination? A trace is considered a transmission line when the propagation delays associated with the trace exceed the signal edge rates (rise and fall times). The rule of thumb for determining the point at which a trace becomes a transmission line is given by:

$$t_{\text{RISE, FALL}} < 2t_{\text{PD}} \quad (1)$$

Where $t_{\text{RISE, FALL}}$ = edge rates, rise and fall times
 t_{PD} = one-way delay of the trace
 $2t_{\text{PD}}$ = round-trip delay of the trace

If the signal edge rates are less than the round-trip delay of a trace, the trace is a transmission line and requires termination to minimize reflections.

Reflections

Reflections appear wherever a signal travelling through a trace encounters a mismatch or change in impedance. Figures 1 and 2 illustrate the principles of transmission line reflections. Assume that the trace is a transmission line with an impedance Z_0 and a propagation delay t_{AB} . The clock output voltage and impedance are V_{OUT} and R_{OUT} , respectively. The load impedance is R_{IN} . The clock generates a step voltage which results in an initial voltage at Point A, given by:

$$V_{\text{AO}} = \frac{Z_0}{R_{\text{OUT}} + Z_0} V_{\text{OUT}} \quad (2)$$

V_{AO} is the resistor divider between the trace and the clock output impedance. The signal propagates toward Point B, where it encounters a change in impedance with respect to the load input. The impedance mismatch generates a reflection, which propagates toward Point A, as shown in Figure 2. The magnitude of the reflected signal is described by the reflection coefficient as shown below:

$$\rho_{\text{B}} = \frac{R_{\text{IN}} - Z_0}{R_{\text{IN}} + Z_0} \quad (3)$$

With a reflection coefficient equal to one, the full amplitude (3.5 V) is reflected back toward point A. In general, the input impedance of a device is much higher than its associated trace, resulting in a reflection coefficient near one.

When the reflected signal reaches point A, it encounters another impedance mismatch between the clock output

Terminating Clock Lines

and the trace. The reflection coefficient at Point A is given by:

$$\rho_A = \frac{R_{OUT} - Z_0}{R_{OUT} + Z_0} \quad (4)$$

The reflection coefficient at point A is -0.74. The reflected signal will have an amplitude of -2.57 V as it travels toward point B.

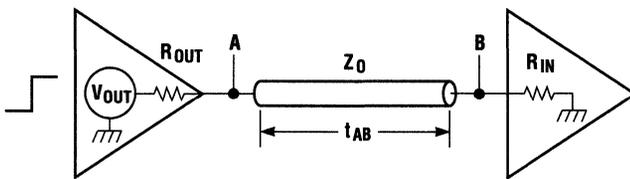
The lattice diagram illustrates how reflected signals bounce back and forth between Points A and B. With each successive reflection at Point A, the amplitude of the reflected signal gets smaller and eventually goes to zero.

The waveform at Point B shows the effect of reflections on an unterminated trace. The waveform oscillates for a long time before reaching the final value.

The step duration is equal to the trace round-trip delay. The longer the trace, the longer it will take for the signal to settle to its final value (4.0 V).

Such a waveform generates system noise and may even cause false triggering of the device being driven. It is not uncommon to see voltages above 6 Volts on unterminated traces, as shown in Figure 3.

Figure 1. Unterminated Trace



$$\begin{aligned} R_{OUT} &= \text{Clock driver output resistance (10-20 } \Omega) \\ R_{IN} &= \text{Device input resistance (10-20 M}\Omega \text{ for TTL)} \\ Z_0 &= \text{Trace impedance} \\ t_{AB} &= \text{Trace propagation delay} \\ V_{OUT} &= 4.0 \text{ Volts} \\ \rho_A &= \frac{R_{OUT} - Z_0}{R_{OUT} + Z_0} = \frac{15 - 100}{15 + 100} \approx -0.74 \\ \rho_B &= \frac{R_{IN} - Z_0}{R_{IN} + Z_0} = \frac{10M - 100}{10M + 100} \approx 1 \end{aligned}$$

Figure 2. Lattice Diagram: Unterminated

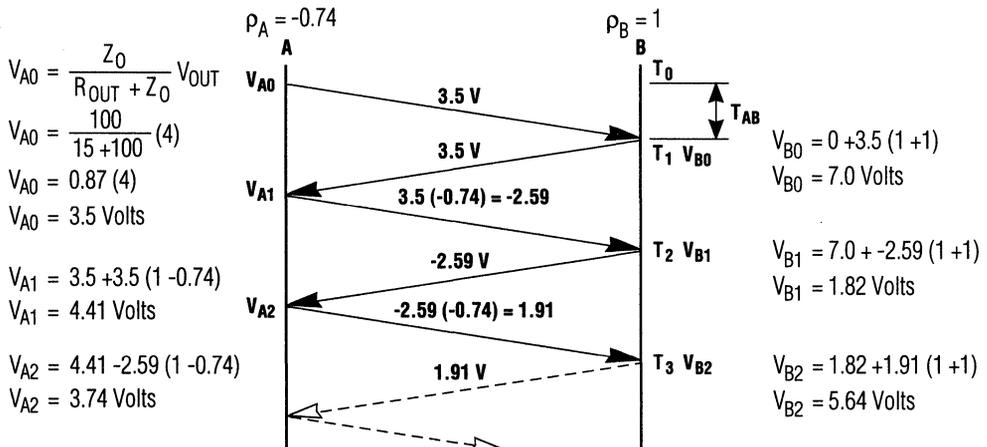
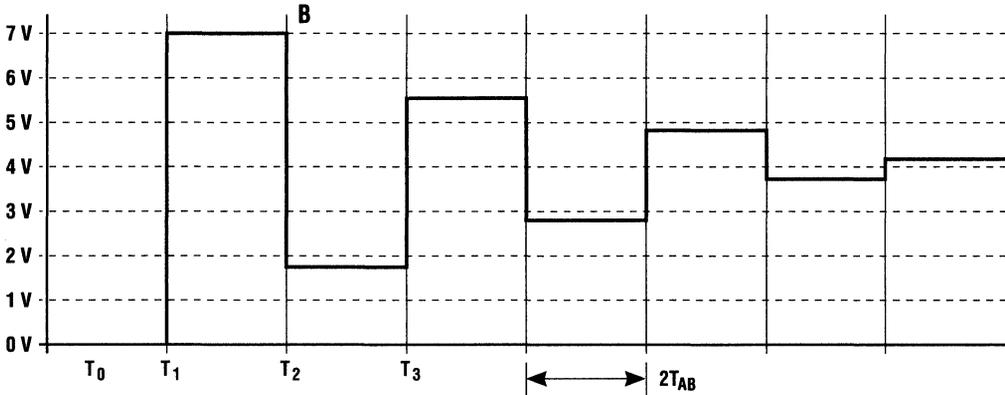


Figure 3. Waveform - Unterminated



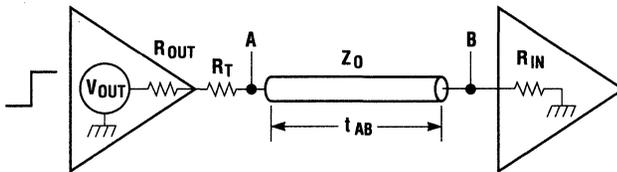
Series Termination

Series termination, as shown in Figure 4, is the most common termination scheme used in clock distribution schemes. It consumes less power than other termination techniques and requires only a single resistor. The second example illustrates the use of series termination to minimize reflections. The series termination resistor

(R_T) was chosen such that the reflection coefficient at Point A is zero. The reflection coefficient at Point B is one. The initial amplitude of the waveform is given by:

$$V_{AO} = V_{OUT} \frac{Z_0}{R_{OUT} + R_T + Z_0} \quad (5)$$

Figure 4. Series Termination



- R_{OUT} = Clock driver output impedance (10 - 20 Ω)
- R_{IN} = Device input impedance (10 $M\Omega$)
- Z_0 = Trace impedance (100 Ω)
- R_T = Series resistance (85 Ω)
- V_{OUT} = 4 Volts

$$\rho_A = \frac{(R_{OUT} + R_T) - Z_0}{R_{OUT} + R_T + Z_0} = 0$$

$$\rho_B = \frac{R_{IN} - Z_0}{R_{IN} + Z_0} \approx 1$$

APPLICATION NOTES

Terminating Clock Lines

Figure 5. Lattice Diagram: Ideal Series Termination

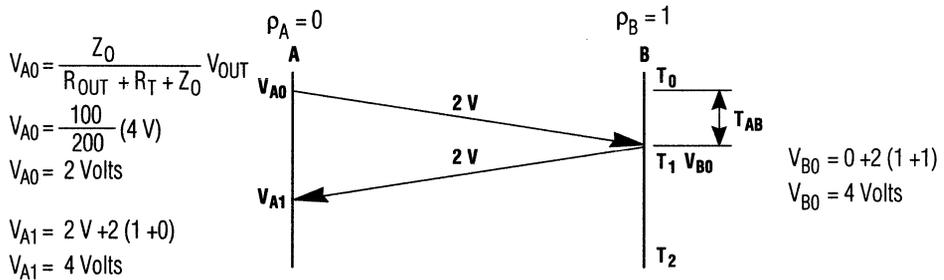
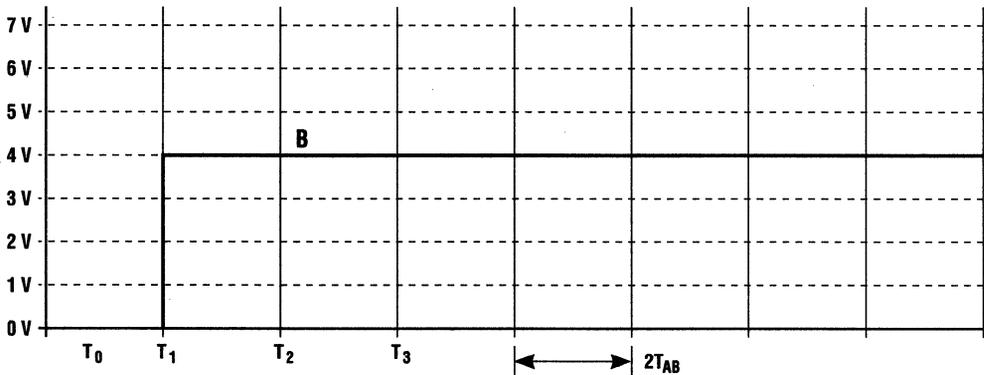


Figure 6. Ideal Waveform



In this example, the initial amplitude of V_A is 2 Volts, as shown in Figure 5. When the signal reaches Point B, where the reflection coefficient is one, the amplitude doubles to 4 Volts. The reflected signal with a 2-Volt amplitude reaches Point A, where the reflection coefficient is zero. The series termination value was chosen such that no reflection is generated at Point A.

The series termination value is given by the following:

$$R_T = Z_0 - R_{OUT} \quad (6)$$

Where Z_0 = trace impedance

R_{OUT} = clock-driven output impedance (10-20 Ω)

Figure 6 depicts an ideal waveform. Since the output impedance of clock generator outputs varies from part to part and with temperature, it is impossible to choose a resistor value perfect for all cases. Calculating R_T for the typical R_{OUT} , however, minimizes the reflection coefficient for the range of output impedance.

Exercise 1

A GA1087 is used to drive a 3-inch trace. Will the trace require termination? If so, what resistor value is needed for series termination?

1. Determine if the trace is a transmission line:
 - a. Check the data sheet for minimum edge rates:

$$T_{OR, OF} = 350 \text{ ps (min)}$$

- b. Estimate trace delay:

$$T_{AB} = 3 \text{ inches} \times 172 \text{ ps/inch} = 516 \text{ ps}$$

Note: 172 ps/inch is for board material with a dielectric constant of 4.1.

- c. Check rule of thumb equation:

$$T_{OR, OF} < 2t_{AB}$$

$$350 \text{ ps} < 2(516 \text{ ps}) = \text{True}$$

In this case, the trace is a transmission line. Had the equality been false, termination would not be required for the trace.

2. Determine clock output impedance. Use the I_{OL} vs. V_{OL} curves to determine the output impedance. The slope of the curve at a specific operating point is the impedance. TriQuint's clock generators characteristically have output impedances in the 10-ohm to 20-ohm range. Choose:

$$R_T = 15 \Omega$$

3. Use Time Domain Reflectometry (TDR) to determine trace impedance or calculate using the following equations:

Microstrip

$$Z_0 = \sqrt{\epsilon_r} \frac{87}{\ln \left(\frac{5.98 h}{0.8 w} \right)}$$

Stripline

$$Z_0 = \sqrt{\epsilon_r} \frac{60}{\ln \left(\frac{4 b}{0.67 \pi w} \right)}$$

Assume that Z_0 was measured:

$$Z_0 = 87 \Omega$$

4. Choose the value* of the series resistor.

$$R_T = Z_0 - R_S$$

$$R_T = 87 - 15$$

$$R_T = 72 \Omega \approx 71.5 \Omega \text{ (std. 1\% resistor value)}$$

**See the Table at the end of this application note for standard resistor values.*

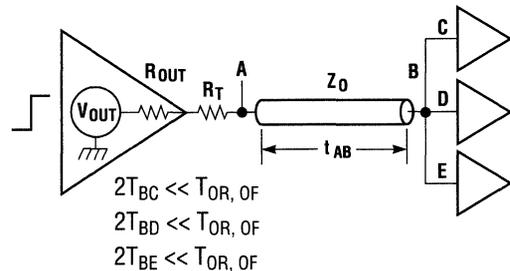
Advantages and Disadvantages of Series Termination

Because series termination does not require additional power, it is a good choice when power dissipation is a critical design concern. When driving CMOS inputs, the steady-state power at the output is near zero, since I_{IH} (input HIGH current) and I_{IL} (input LOW current) are negligible. Even TTL input currents are small; in the order of 10 μA to 40 μA .

With series termination, loads must be located at the end of the line as shown in Figure 7.

The daisy chaining of outputs is not allowed in series-terminated lines. An example of an improperly daisy-chained termination scheme is shown in Figure 8. The amplitude of the waveform at A, B, and C is one-half the steady-state value on the first wavefront. At point D, the reflection coefficient is one and the signal doubles and achieves steady state, as shown in Figure 9.

Figure 7. Series Termination (Loads Lumped at End)



Terminating Clock Lines

Figure 8. Daisy Chaining Outputs (Not Allowed)

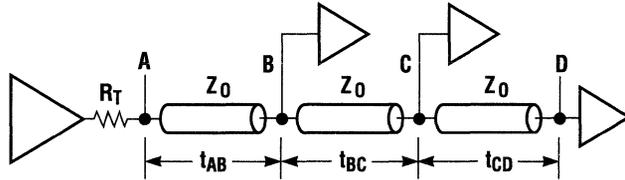
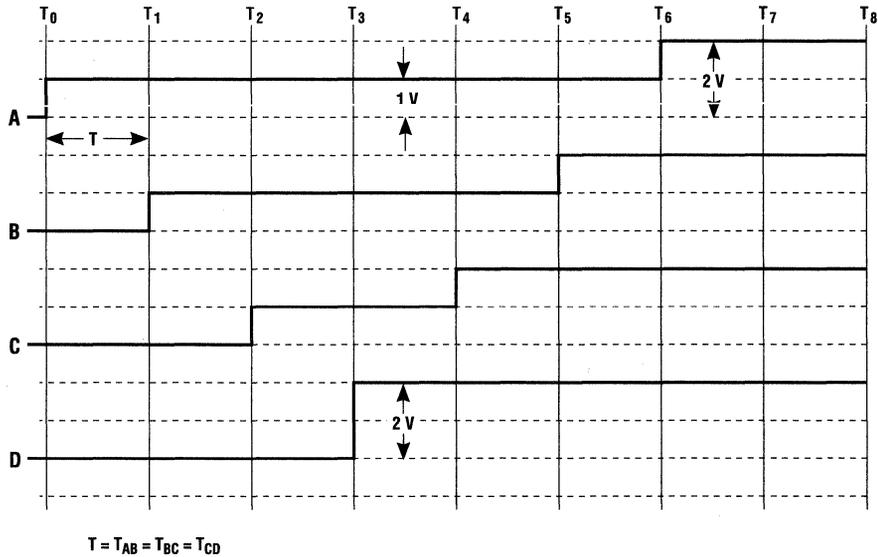


Figure 9. Daisy Chain Waveforms



Thevenin Termination

With Thevenin termination, the termination is located at the end of the trace as shown in Figure 10. The Thevenin equivalent of the two termination resistors are chosen to equal the trace impedance. For this example, the Thevenin voltage is chosen to equal 1.5 volts.

Solving equations 10 and 11:

$$\frac{1}{R_{T1}} + \frac{1}{R_{T1}} = \frac{1}{Z_0} \quad (10)$$

$$\left(\frac{R_{T2}}{R_{T1} + R_{T2}} \right) 5V = V_T = 1.5 \quad (11)$$

Reducing Equation 11:

$$R_{T2} = 0.3 R_{T1} + 0.3 R_{T2} \quad (12)$$

$$R_{T1} = \frac{0.7 R_{T2}}{0.3}$$

$$R_{T1} = 2.33 R_{T2}$$

Terminating Clock Lines

Substituting $2.33 R_{T2}$ for R_{T1} in Equation 10 yields:

$$\frac{1}{2.33 R_{T1}} + \frac{1}{R_{T1}} = \frac{1}{100}$$

$$R_{T2} = 100 \left(\frac{1}{2.33} + 1 \right)$$

$$R_{T2} = 142 \Omega \approx 143 \Omega$$

Substituting back into Equation 12 yields:

$$R_{T1} = 332 \Omega$$

Choosing R_{T1} and R_{T2} such that their Thevenin equivalent is equal to Z_0 yields a reflection coefficient of zero at B.

Advantages and Disadvantages of Thevenin Termination

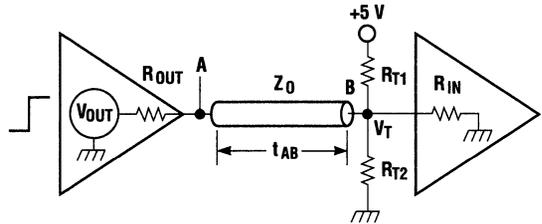
Daisy chaining is allowed for traces with Thevenin termination. Because the termination is located at the end of the trace, the voltage amplitude of the initial signal is higher than in a series-terminated case.

The Thevenin termination example illustrated in Figure 11 has an initial amplitude of 3.48 V, which exceeds TTL input requirements. The Thevenin resistor and voltage can be tuned to achieve the desired result. For example, if rise time and fall time symmetry is of primary importance, choose a Thevenin voltage

midway through the swing. A higher Thevenin voltage will result in a faster rise time, if desired.

The DC current requirement is a disadvantage because it requires additional power. The Thevenin termination load line should not violate the maximum V_{OL} and minimum V_{OH} requirements.

Figure 10. Thevenin Termination



R_{OUT}	= Clock output impedance	(10 - 20 Ω)
R_{IN}	= Device input impedance	(10 M Ω)
Z_0	= Trace impedance	(100 Ω)
R_{T1}	=	332 Ω
R_{T02}	=	143 Ω
$R_{T1} \parallel R_{T2}$	=	100 Ω
Z_{IN}	=	10 M $\Omega \parallel 100 \Omega$ 100 Ω

Where

$$R_{T1} \parallel R_{T2} = Z_0$$

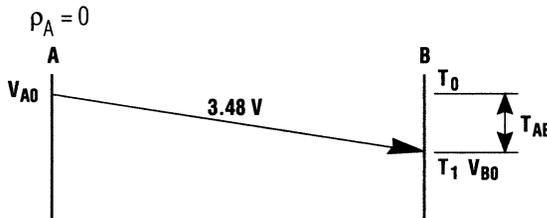
$$\frac{R_{T2}}{R_{T1} + R_{T2}} (5 V) = 1.5 V$$

Figure 11. Lattice Diagram - Thevenin Termination

$$V_{A0} = \frac{Z_0}{R_{OUT} + Z_0} V_{OUT}$$

$$V_{A0} = \frac{100}{100 + 15} (4 V)$$

$$V_{A0} = 3.48 \text{ Volts}$$



$$\rho_B = \frac{Z_{IN} - Z_0}{Z_{IN} + Z_0}$$

$$\rho_B = \frac{100 - 100}{200}$$

$$\rho_B = 0$$

$$V_{B0} = 0 + 3.48 (1 + 0)$$

$$V_{B0} = 3.48 \text{ Volts}$$

Terminating Clock Lines

Figure 12 shows the IV curve of the clock driver with a load line of a Thevenin resistor of 100 ohms and a voltage of 1.5 V. The load line intersects V_{OL} at 0.2 V, which is within specification.

Parallel Termination

Parallel termination is similar to the Thevenin termination scheme, where $R_T = Z_0$ and $V_T = 0$. The parallel termination load line should not violate the maximum V_{OL} and minimum V_{OH} requirements.

AC Termination

AC termination blocks the DC current that exists in a parallel termination scheme. The resistor and capacitor values are given by:

$$R_T = Z_0$$

$$C_T = \frac{2t_{AB}}{R_T}$$

Choose the capacitor such that the RC time constant is twice the round-trip delay.

The advantage of AC termination is less power than Thevenin or parallel termination. The disadvantage is that additional components are required.

Figure 12. I_{OL} vs. V_{OL}

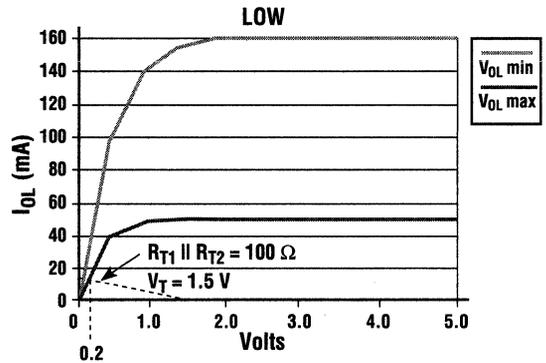


Figure 13. Parallel Termination

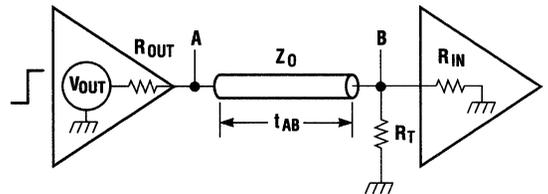
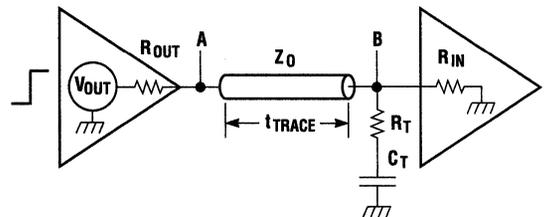


Figure 14. AC Termination



Terminating Clock Lines

Summary

The choice of a termination scheme depends on the system's design requirements. The cleanest waveforms come from parallel or Thevenin terminated lines.

Thevenin termination requires one more resistor than does parallel termination, but with Thevenin termination, the designer can set the Thevenin voltage higher to reduce rise time or lower to reduce fall time.

Series termination requires less power than parallel and Thevenin termination. A series termination is ideal when using clock devices with multiple outputs because it requires the least power dissipation of the four termination schemes. Series termination requires no DC current, therefore all the energy is used charging and discharging the capacitance on the line.

AC termination has low power at lower frequencies, but has only slightly lower power at higher frequencies, when compared to Thevenin termination.

References

1. "Transmission Line Fundamentals," Joel Martinez, TriQuint Semiconductor, Inc., 1993
2. *MECL System Design Handbook*, Motorola, 1988
3. *ECL in PS Design Guide*, Motorola, 1991

Appendix 1. Standard 1% Resistor Values

1% Resistor Values (ohms)				
4.02	17.8	30	49.9	82.5
10	18	30.1	51	84.5
10.2	18.2	30.9	51.1	86.6
10.5	18.7	31.6	52.3	88.7
10.7	19.1	32.4	53.6	90.9
11	19.6	33	54.9	91
11.3	20	33.2	56	93.1
11.5	20.5	34	56.2	95.3
11.8	21	34.8	57.6	97.6
12	21.5	35.7	59	100
12.1	22	36	60.4	102
12.4	22.1	36.5	61.9	105
12.7	22.6	37.4	62	107
13	23.2	38.3	63.4	110
13.3	23.7	39	64.9	113
13.7	24	39.2	66.5	115
14	24.3	40.2	68	118
14.3	24.7	41.2	68.1	
14.7	24.9	42.2	69.8	
15	25.5	43	71.5	
15.4	26.1	43.2	73.2	
15.8	26.7	44.2	75	
16	27	45.3	75.5	
16.2	27.4	46.4	76.8	
16.5	28	47	78.7	
16.9	28.7	47.5	80.6	
17.4	29.4	48.7	82	

The information provided herein is believed to be reliable; TriQuint assumes no liability for inaccuracies or omissions. TriQuint assumes no responsibility for the use of this information, and all such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. TriQuint does not authorize or warrant any TriQuint product for use in life-support devices and/or systems.

Copyright © 1997 TriQuint Semiconductor, Inc. All rights reserved.

Revision 1.0.A October 1997

Terminating Clock Lines

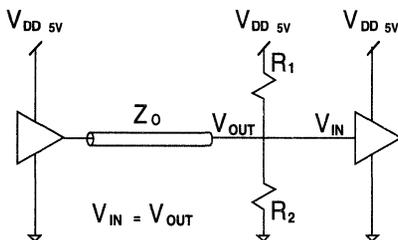
Interfacing 5-Volt Clock Chips to 3-Volt ICs

Today's high performance microprocessors are migrating to 3 V operation in order to offer high speeds without excessive power dissipation. Many of the peripheral, memory, and support ICs needed to build a complete system are not yet available in 3 V versions. System designers are required to integrate both 3 V and 5 V devices in the same system. Interfacing the two types requires some careful design considerations.

Input threshold levels are the same for both 3 V and 5 V TTL devices ($V_{IL} = 0.8 \text{ V}$ and $V_{IH} = 2.0 \text{ V}$). 3 V devices, however, specify a maximum V_{IN} of $V_{DD3V} + 0.3 \text{ V}$. For most 5 V output drivers, the maximum V_{OH} level can exceed this limit, leading to potentially dangerous overdrive conditions. This limitation can be easily overcome when using TriQuint's 5 V clock chips with a modified Thevenin termination as presented in note.

Figure 1 shows the standard Thevenin parallel termination scheme. ($R_1 + R_2$) is chosen to equal the trace impedance Z_0 . The ratio R_1 / R_2 is chosen to

Figure 1. Standard Thevenin Parallel Termination

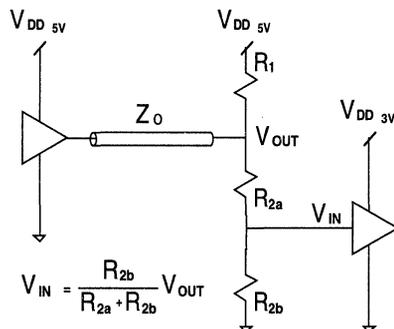


provide the proper Thevenin voltage (V_T) for termination. TriQuint's 10XX devices are rated to drive traces with impedance as low as 50Ω , and use $V_T = 1.5 \text{ V}$ for symmetrical rise and fall times. For these conditions, $R_1 = 167 \Omega$ and $R_2 = 71 \Omega$ (160Ω and 75Ω will work well when choosing common 5% resistor values).

Figure 2 shows a modified Thevenin parallel termination scheme. R_2 from Figure 1 is divided into two resistors, R_{2a} and R_{2b} , such that $R_2 = R_{2a} + R_{2b}$. The idea is to attenuate the output's V_{OH} level to the extent that the $V_{DD3V} + 0.3 \text{ V}$ limit on the 3 V IC's V_{IN} is not exceeded. Care must be taken to prevent V_{IN} from falling below the V_{IHmax} spec of 2.0 V . The following are reasonable targets:

- $V_{INmin} = 2.4 \text{ V}$ (Standard V_{OHmin} for TTL I/O. This provides 0.4 V guardband to V_{IHmax} of 2.0 V).
- $V_{INmax} = V_{DD3V} + 0.3 \text{ V} = 3.3 \text{ V}$ (3 V TTL spec is $V_{DD3V} = 3.0$ to 3.6 V . The worst case is for $V_{DD3Vmin}$, which is 3.0 V . $V_{DD3V} + 0.3 \text{ V}$ then is 3.3 V).

Figure 2. Modified Thevenin Parallel Termination

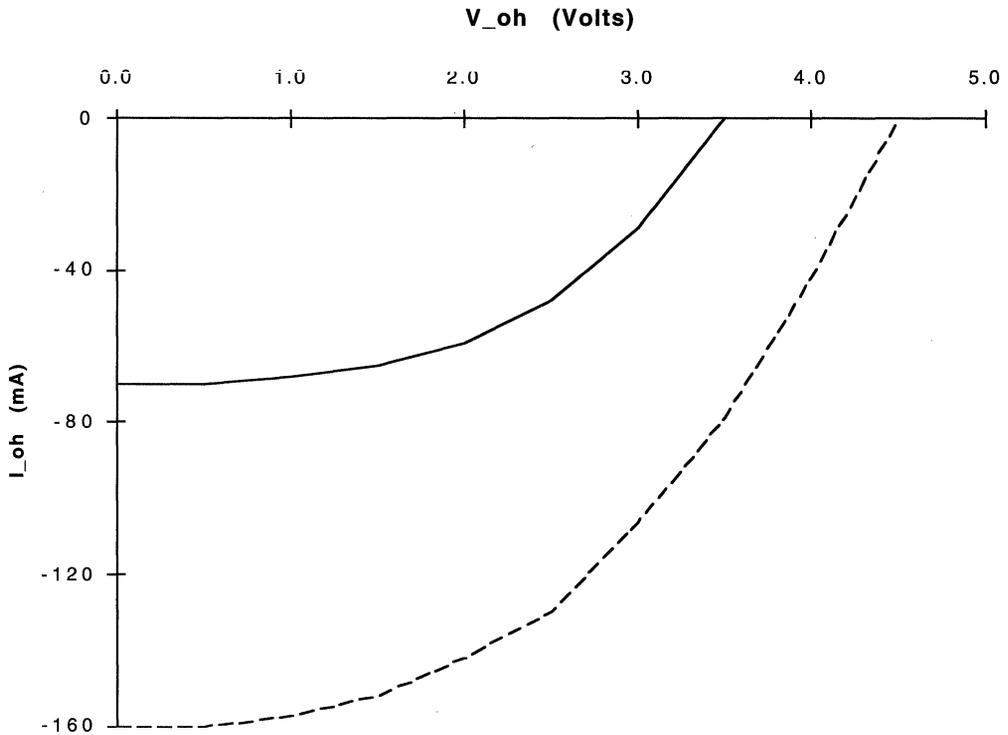


Interfacing 5V Clocks to 3V ICs

In order to guarantee compliance with the above constraints, the output buffer's characteristics must be well defined for best and worst cases over all process, V_{DD} , and temperature conditions. TriQuint provides this information for clock chips in the product's data sheet. The V_{OH} I-V characteristics for the 10XX devices are reproduced below in Figure 3.

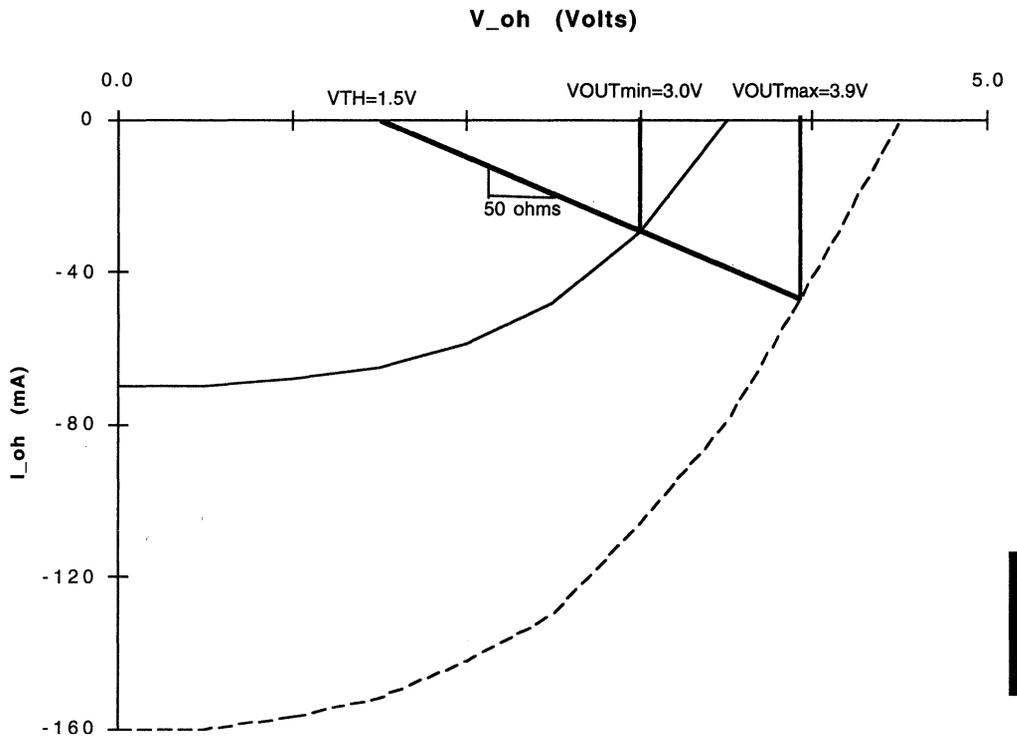
The solid line defines the "weakest" output characteristic. This represents the "slow" process corner, low temperature, and $V_{DD5V} = 4.75$ V. The dashed line represents the "strongest" output characteristics, representing the "fast" process corner, high temperature, and $V_{DD5V} = 5.25$ V.

Figure 3. V_{OH} I-V Characteristics for 10XX Devices



The min and max values of V_{oh} can be determined for any load by superimposing the load line on the I-V graph. Figure 4 shows this for the case of $Z_0 = 50 \Omega$ and $V_T = 1.5 V$.

Figure 4. Determining V_{OHmin} / V_{OHmax}



APPLICATION NOTES

Interfacing 5V Clocks to 3V ICs

We now have enough information to determine the values of R_{2a} and R_{2b} :

$$V_{INmin} = (R_{2b} / 71 \Omega) * V_{OUTmin}$$

$$R_{2a} + R_{2b} = 71 \Omega$$

$$2.4 V = (R_{2b} / 71 \Omega) * 3 V$$

$$R_{2b} = 57 \Omega \text{ (56 } \Omega \text{ will work well)}$$

$$R_{2a} = 71 \Omega - 57 \Omega = 14 \Omega \text{ (13 } \Omega \text{ will work well)}$$

We can check V_{INmax} to be sure we won't exceed 3.3 V:

$$V_{INmax} = (R_{2b} / R_2) * V_{OUTmax} = (0.8) * 3.9 V = 3.2 V$$

This indicates that we have 100 mV margin for ALL process/temperature/ V_{DD} corners, even the unlikely event $V_{DD5V} = 5.25 V$ and $V_{DD3V} = 3.0 V$.

The equations for use with any Thevenin parallel termination scheme can be summarized as follows:

- (1) $R_1 \parallel R_2 = Z_0$
 $Z_0 =$ trace impedance
- (2) $R_2 * V_{DD5V} / (R_1 + R_2) = V_T$
 $V_{DD5V} = 5 V$ supply value;
 $V_T =$ Thevenin termination voltage
- (3) $R_2 = R_{2a} + R_{2b}$
- (4) $V_{INmin} = R_{2b} * V_{OUTmin} / R_2$
 V_{OUTmin} from I-V curves;
 $V_{INmin} = 2.4 V$ for $V_{IHmax} = 2.0 V$
- (5) $V_{INmax} = R_{2b} * V_{OUTmax} / R_2$
 V_{OUTmax} from I-V curves

- (1) and (2) are used to determine R_1 and R_2 .
- (3) and (4) are used to determine R_{2a} and R_{2b} .
- (5) is used to verify V_{INmax} is less than $V_{DD3Vmin} + 0.3 V$.

Table 1 provides a number of solutions for $V_T = 1.5 V$ and various values of Z_0 .

Table 1. Termination Resistor Values*

$Z_0(\Omega)$	$R_1(\Omega)$	$R_{2a}(\Omega)$	$R_{2b}(\Omega)$
50	160	13	56
55	180	15	62
60	200	18	68
65	220	20	75
70	240	22	75
75	240	24	82

*Rounded to the nearest 5% standard value.

This scheme is useful for interfacing to both 5 V and 3 V CMOS inputs. 5 V CMOS inputs often require $V_{INmin} \geq 3.0 V$. The same clock chip can drive this input on a separate output by using the standard termination scheme shown in Figure 1. Both outputs remain identically loaded, thus minimizing skew between them.

The information provided herein is believed to be reliable; TriQuint assumes no liability for inaccuracies or omissions. TriQuint assumes no responsibility for the use of this information, and all such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. TriQuint does not authorize or warrant any TriQuint product for use in life-support devices and/or systems.

Copyright © 1997 TriQuint Semiconductor, Inc. All rights reserved.

Revision 1.0.A October 1997

Part-to-Part Skew

Part-to-part skew (t_{SKEWPP}) is important for system designs utilizing two or more clock chips where the outputs must be synchronized. A statistical study shows that t_{SKEWPP} can be much less than calculated from worst-case conditions. This data is presented in this application note to show system designers techniques for applying the information to their designs.

Definition

t_{SKEWPP} refers to the time difference between the rising edge of outputs on two different devices.

Figures 1 and 2 show two methods for configuring multiple PLL clock devices in the same system. Figure 1 shows two devices configured in a parallel manner, where skew can be represented as:

$$t_{SKEWPP} = 2 * t_{SKEW1} + |t_{PD1} - t_{PD2}| \quad (1)$$

Figure 2 shows two devices configured in a cascade manner, where skew can be represented as:

$$t_{SKEWPP} = 2 * t_{SKEW1} + |t_{PD2}| \quad (2)$$

The data presented here initially ignores the $2 * t_{SKEW1}$ term in calculating t_{SKEWPP} for both methods, to make the data more tractable. Trace lengths are adjusted carefully in Figure 2 in order to recenter the skew between devices to 0 ps. Methods for accounting for output skew and jitter are presented later in this application note.

Figure 1. Parallel Configuration

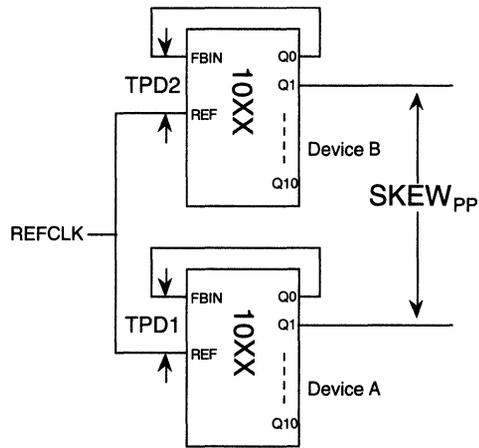
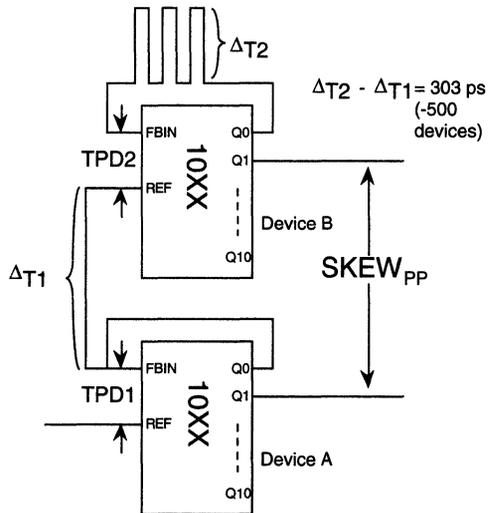


Figure 2. Cascade Configuration



Part-to-Part Skew

Skew Distributions

Figures 3 and 4 show standard distributions plotted with t_{SKEWPP} distributions. Since the t_{SKEWPP} distribution is very nearly a standard distribution in nature, it can be characterized to a large extent by its sigma value. At mean ± 3 sigma, more than 99.7% of the distribution falls within this range.

Figure 4 is not just the right half of Figure 3 in this example. It represents a distribution in which the absolute value of a parameter is plotted. This can be thought of as “folding” Figure 3 in half, or the addition of the left and right halves of Figure 3. This is the case, for example, when the skew between any two outputs is plotted as an absolute value. Table 1 shows the error rates for various ranges in increments of sigma.

Figure 3. Two-Sided Normal Distribution for t_{SKEWPP}

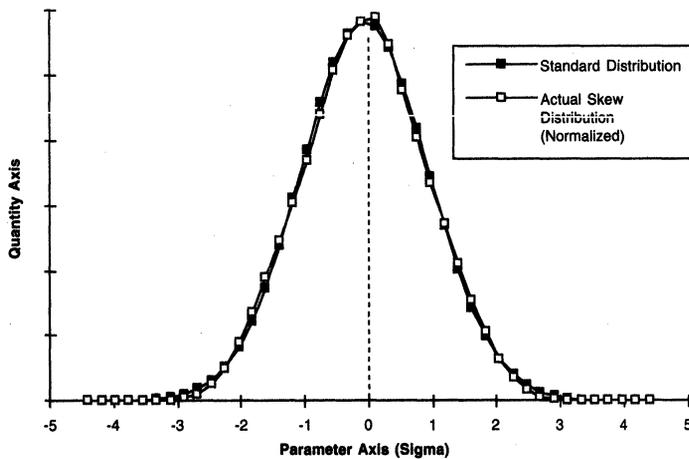


Figure 4. One-Sided Normal Distribution for t_{SKEWPP}

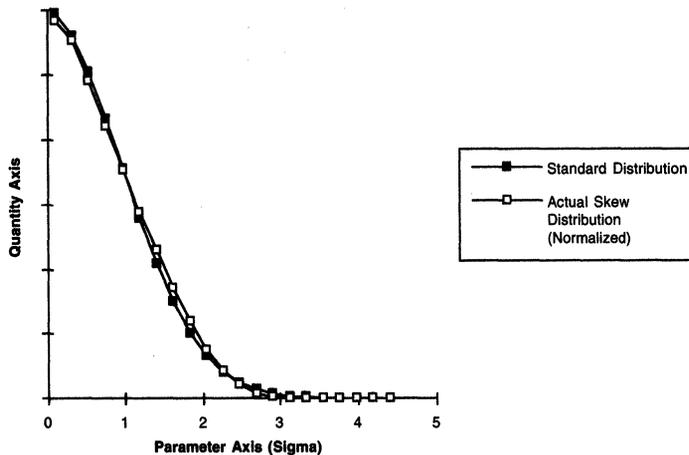


Table 1. Error Rates for Standard Distributions

Range	% distribution within range	Error rate
1 sigma	68.3	32 in 100
2 sigma	95.40	5 in 100
3 sigma	99.730	3 in 1000
4 sigma	99.99367	6 in 10 ⁵
5 sigma	99.9999426	6 in 10 ⁷
6 sigma	99.99999802	2 in 10 ⁹
7 sigma	99.99999999742	3 in 10 ¹²

Parallel Configuration

$|t_{PD1} - t_{PD2}|$ distributions are shown in Figures 5 and 6 for TriQuint's 10XX devices. The data was derived from characterization of t_{PD} over all temperature, voltage, and process corners. The data assumes that the two devices are operated at the same V_{CC} and temperature, but not necessarily the same frequency. This is a fair assumption for devices mounted on the same board, close to each other.

Figure 5. $|t_{PD1} - t_{PD2}|$ Histogram for 10XX-500 Devices

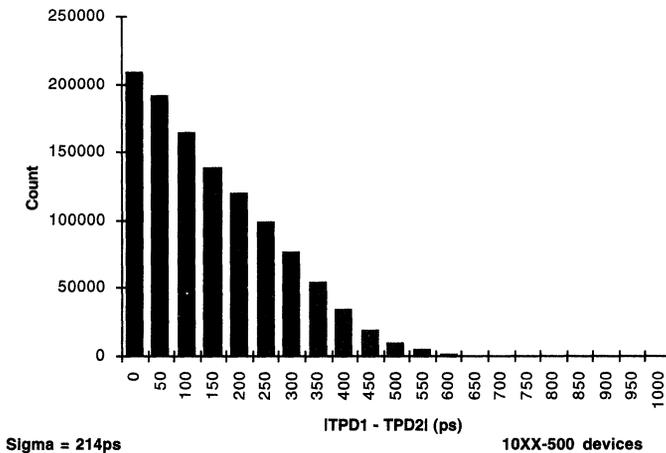
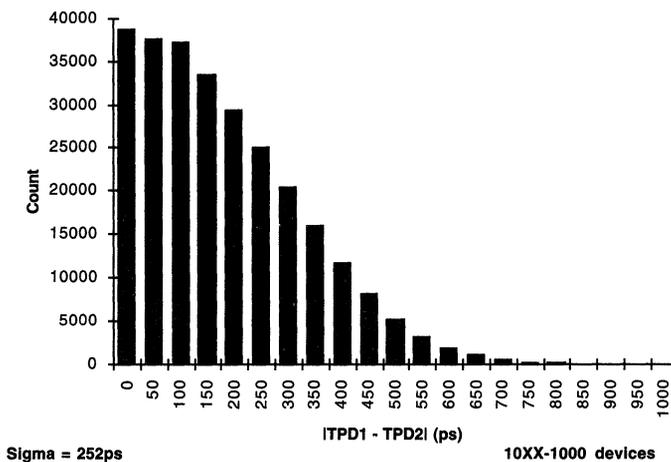


Figure 6. $|t_{PD1} - t_{PD2}|$ Histogram for 10XX-1000 Devices



APPLICATION NOTES

Part-to-Part Skew

How Much is Enough?

It is not a simple matter to determine how many sigma is “safe” to use for design calculations. It will be different for each system design. One factor to consider is the number of systems to be built. The more systems, the more conservative the designer should be.

As an example, consider a design targeted for 10,000 units. At 5 sigma, the failure rate is 0.6 ppm. This says that there is a one in 167 chance that one of the 10,000 units will fail (a pretty conservative number for most applications). If failures can be caught during system test, more aggressive values can be designed in. In some situations, more conservative values may be necessary. These and other factors must be considered early in the design process. It is up to the system designer to determine how much guardband is necessary for the system.

For 10XX-500 devices, 5 sigma is ~1070 ps for $|t_{PD1} - t_{PD2}|$. For 10XX-1000 devices, the 5 sigma value is 1260 ps. Making worst case calculations based on data sheet parameters, one would get 1000 ps for 10XX-500 devices, and 2000 ps for 10XX-1000 devices. So, no savings is realized for 10XX-500 devices, but 750 ps can be trimmed off worst case $|t_{PD1} - t_{PD2}|$ calculations for 10XX-1000 devices. For the 10XX-500 devices, t_{SKEW} would not ever exceed 1000 ps, as these would be downgraded to 10XX-1000 devices at TriQuint’s final test.

Output Skew ($t_{SKEW(1\sigma/2)}$) and Jitter (t_{JN})

As mentioned earlier, the overall t_{SKEWPP} is actually composed of two additional components, output skew and jitter. Output skew has been characterized to have the distributions shown in Figures 7 and 8 for the 10XX devices (excluding the GA1086).

Figure 7. Same Group Output Skew (t_{SKEW1}) Histogram

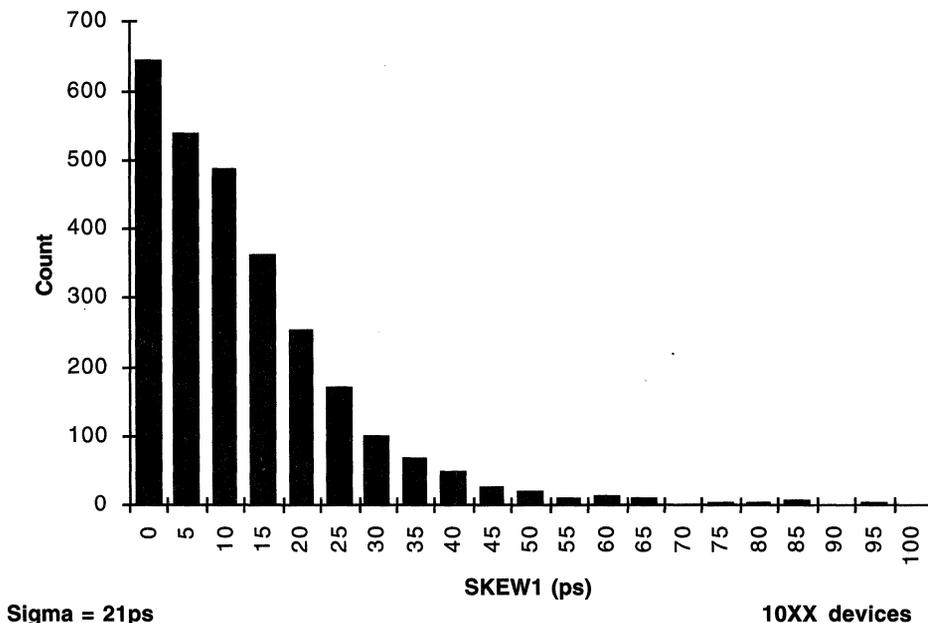
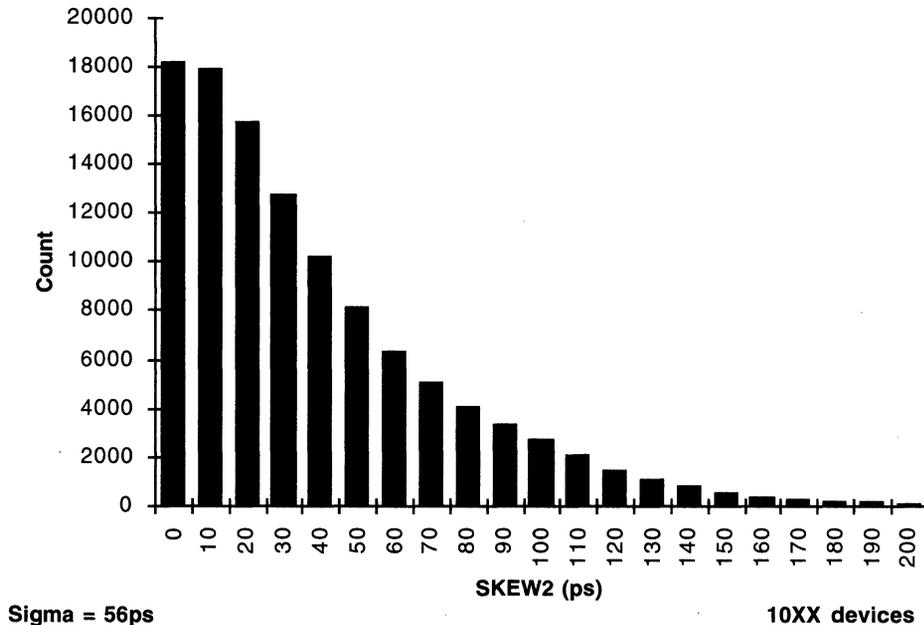


Figure 8. Group to Group Output Skew (t_{SKEW2}) Histogram



In determining t_{SKEWPP} , output skew is statistically summed with $(t_{PD1} - t_{PD2})$ by taking the square root of the sum of the squares:

$$t_{SKEWPP} = ((t_{PD1} - t_{PD2})^2 + 2 * (t_{SKEW (1or2)})^2)^{1/2} \quad (3)$$

Jitter cannot be treated statistically as an additional component to the overall skew. Jitter provides us information on the variation of edge placement with time, and is not directly related to the operating corner. The best way to include jitter is to add a peak-to-peak jitter number to the t_{SKEW} number.

An overall formula for t_{SKEWPP} that includes jitter can be written as:

$$t_{SKEWPP} ((t_{PD1} - t_{PD2})^2 + 2 * (t_{SKEW (1or2)})^2)^{1/2} + t_{JR} \quad (4)$$

$$5 \text{ sigma } t_{SKEWPP} = ((1000)^2 + 2 * (105)^2)^{1/2} + 400 = 1411 \text{ ps (for 10XX-500 devices)}$$

$$5 \text{ sigma } t_{SKEWPP} = ((1260)^2 + 2 * (105)^2)^{1/2} + 400 = 1669 \text{ ps (for 10XX-1000 devices)}$$

Cascade Configuration

The second method for configuring multiple devices shown in Figure 2 is useful only for PLL devices. In this case, it is the distribution of t_{PD} that is important, not the t_{PD} difference, as was the case in the method of Figure 1. The t_{PD} distributions for TriQuint's 10XX devices are shown in Figures 9 and 10.

Note that in Figure 2, the t_{PD} offset value of -350 ps is added to device B's feedback path. This essentially recenters the t_{PD} distribution about 0 ps from the perspective of the outputs.

Part-to-Part Skew

Because the distribution of t_{PD} is not very tight, a statistical approach is helpful only in reducing the $t_{SKEW(1\sigma/2)}$ parameter. In addition, the t_{PD} histograms

do not closely match the standard distribution, so the statistical methodology using t_{PD} is less accurate.

Figure 9. Propagation Delay Histogram (10XX-500 Devices)

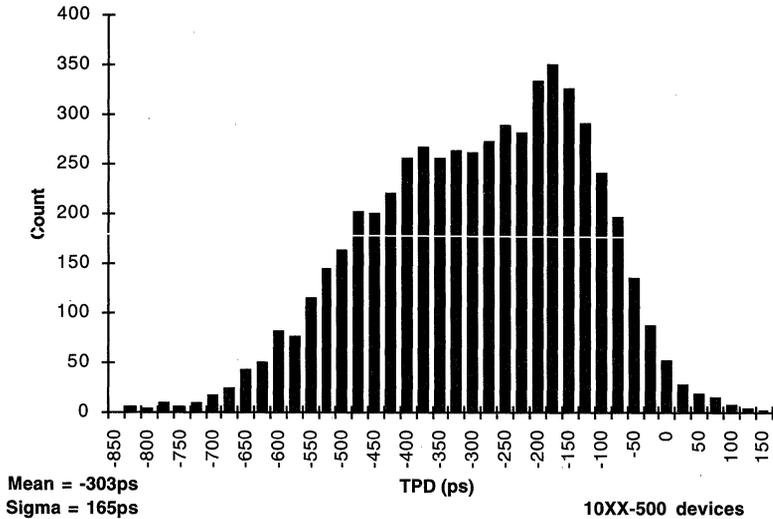
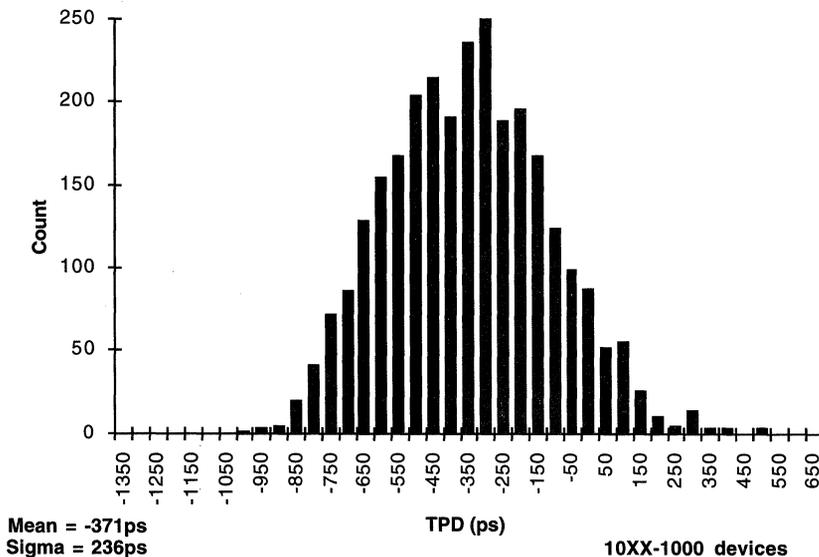


Figure 10. Propagation Delay Histogram (10XX-1000 Devices)



The random jitter t_{JR} of device B increases by up to 50% in the cascade configuration. The jitter of device A does not figure into the calculation of t_{SKEWPP} since all the outputs of device A jitter together. However, the full peak-to-peak jitter of device B must be accounted for.

An equation for determining t_{SKEWPP} for cascaded devices is given by:

$$t_{SKEWPP} = (t_{PD})^2 + 2 * (t_{SKEW(1or2)})^2)^{1/2} + 1.5 * t_{JR} \quad (5)$$

where the 1.5 factor accounts for the (up to) 50% increase in jitter of device B.

t_{SKEWPP} Tables

Table 2 uses equation (4) to calculate t_{SKEWPP} for various sigmas. The first two columns use t_{SKEW1} which gives the t_{SKEWPP} between outputs from the feedback groups. The third and fourth columns use t_{SKEW2} in place of t_{SKEW1} in equation (4) for the more general case of skew between any output of device A to any output of device B. Worst case calculations based on data sheet parameters are also shown for comparison.

Table 3 uses equation (5) to calculate t_{SKEW} for various sigmas. The format is the same as for Table 2.

Table 2. t_{SKEWPP} (Parallel Device Configuration as in Figure1)

Range	t_{SKEWPP} (using Skew 1)		t_{SKEWPP} (using t_{SKEW2})	
	10XX-500 devices	10XX-1000 devices	10XX-500 devices	10XX-1000 devices
1 sigma	616 ps	654	628	664
2 sigma	832	907	856	928
3 sigma	1048	1161	1085	1192
4 sigma	1264	1415	1313	1457
5 sigma	1411	1669	1476	1721
6 sigma	1416	1922	1507	1985
7 sigma	1421	2176	1543	2249
Worst case*	1700	2700	2100	3100

*Worst case calculation uses the following equation:

$$t_{SKEWPP} = (t_{PDmax} - t_{PDmin}) + 2 * t_{SKEW(1 or 2)} + t_{JR} \quad (6)$$

Part-to-Part Skew

Table 3. t_{SKEWPP} (Cascade Device Configuration Shown in Figure 2)

Range	t_{SKEWPP} (using t_{SKEW1})		t_{SKEWPP} (using t_{SKEW2})	
	10XX-500 devices	10XX-1000 devices	10XX-500 devices	10XX-1000 devices
1 sigma	786 ps	838	783	849
2 sigma	935	1076	966	1098
3 sigma	1103	1314	1149	1347
4 sigma	1114	1551	1192	1596
5 sigma	1122	1611	1238	1676
6 sigma	1131	1616	1290	1707
7 sigma	1141	1621	1347	1743
Worst Case*	14500	1900	1800	2300

Worst case calculation uses the following equation:

$$t_{SKEWPP} = (t_{PDmax} - t_{PDmin}) + 2 * t_{SKEW(1 \text{ or } 2)} + 1.5 * t_{JR} \quad (7)$$

Summary

t_{SKEWPP} is important in systems where several clock devices are required with synchronous outputs. It is shown to be composed of several parameters: t_{PD} , $t_{SKEW(1 \text{ or } 2)}$, and t_{JR} .

A statistical approach has been shown for determining t_{SKEWPP} based on characterization data. A significant savings can be realized, even for the most conservative designs. For most cases, a cascade configuration realizes the lowest achievable t_{SKEWPP} for the PLL clock devices discussed here.

The information provided herein is believed to be reliable; TriQuint assumes no liability for inaccuracies or omissions. TriQuint assumes no responsibility for the use of this information, and all such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. TriQuint does not authorize or warrant any TriQuint product for use in life-support devices and/or systems.

Copyright © 1997 TriQuint Semiconductor, Inc. All rights reserved.

Revision 1.0.A October 1997

Clock Distribution Techniques Using the GA1110E

In today's high-performance systems, one of the bigger challenges a designer faces is that of effective distribution of clocks to ensure reliable operation. This application note offers insights and suggestions to assist in the design task.

Introduction

The clock speeds of the new generations of CPUs, which can be either RISC or CISC, are continually increasing. To capitalize on the full performance of these CPUs, the designer needs to carefully interface the peripheral devices to the CPU without violating the stringent clock cycle time requirements or inserting "wait states."

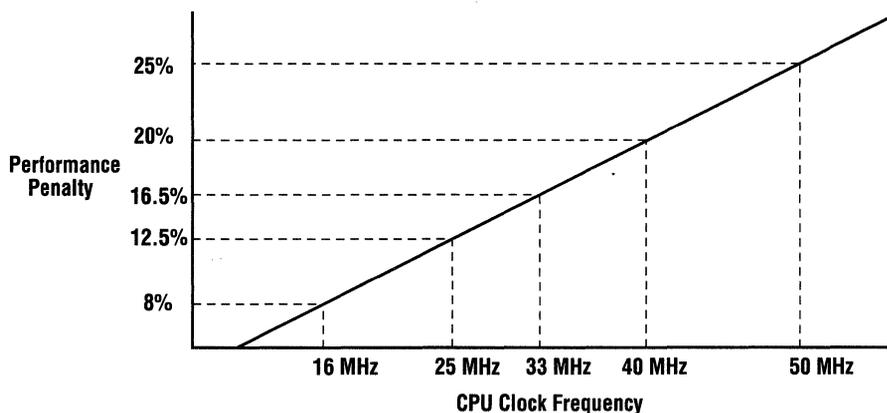
The timing of the various parts and functions of a system can be controlled by carefully planning the synchronous clock distribution, and by limiting the

overall clock skew between the various functional blocks. To attain this goal, however, the designer requires a very precise clock buffer with a low input-to-output delay, and with low skew between its outputs.

TriQuint's GA1110E is a Low-Skew Clock Buffer device which neatly and economically fills the need. This device has delays between the input and the output signals on the order of ± 250 ps (typical), with an output skew of ± 250 ps (typical). This clock buffer also offers the user the flexibility to adjust the phases of the outputs in 2.5 ns increments for applications which require load and trace-length matching.

In this application note, we will identify six typical ways to overcome clock distribution problems and we will show how the GA1110E solves them effectively and economically.

Figure 1. Performance Penalty vs. CPU Clock Frequency for 5 ns Clock Skew



Clock Distribution Techniques

System Performance and Clock Skew

Clock skew is defined as the time difference between the "ideal" and the "actual" edge of the clock, directly impacting the system bandwidth. The typical clock skew in today's high-performance system is on the order of 5 ns. As system performance increases and CPU clocks reach frequencies of 50 MHz and higher, a 5 ns skew becomes a significant limiting factor. The performance penalty, as a function of CPU frequency, "F", for a skew delay of "D" nanoseconds, can be described by the following formula:

$$\text{Performance penalty} = (10^{-9}) \times F \times D \times 100\%$$

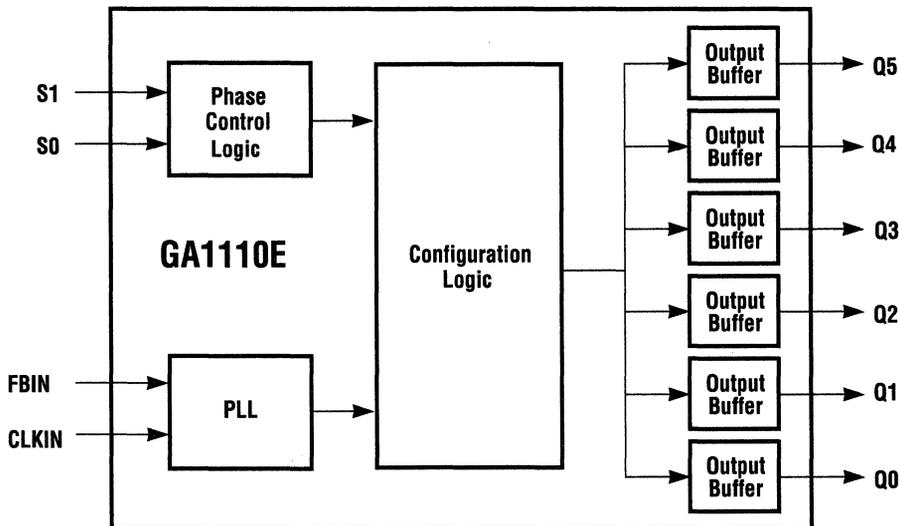
The graph representing the linear relationship above for a skew delay of 5 ns is depicted in Figure 1. As is evident from the figure, the performance penalty for a 25 MHz CPU is 12.5%, but for a 50 MHz CPU, it is 25%. Obviously, this is a serious problem that must be overcome.

Clock skew is a function of many different variables, including the number of loads per clock buffer output, trace length, temperature, power supply voltages, the relative phase difference between the clock outputs, the input-to-output delay of the clock buffers, and mismatch of equivalent ICs. Each of the parameters can vary from one section of the system to the next. To reduce the overall clock skew in the system, it is necessary to minimize the effects of each of the variables above. In later sections we will show how this can be accomplished by using the GA1110E.

GA1110E Functional Description

The functional block diagram of TriQuint's GA1110E, a Low-Skew TTL Clock Buffer, is shown in Figure 2. The GA1110E produces multiple clock outputs synchronized in phase and frequency to a periodic clock input. The chip has two select pins and an external feedback path to allow the user to phase adjust the outputs, Q0-Q5.

Figure 2. GA1110E – Functional Block Diagram



relative to the input clock, CLKIN. The phase can be adjusted in increments of t_{PH} , as specified in the AC characteristics of the data sheet.

The tight control over the phase and frequency of the output clocks is assured by a 400 MHz internal Phase-Locked Loop (PLL). The feedback loop from one of the output clocks, Q0–Q5, to FBIN helps the on-chip PLL to continuously maintain synchronization between the input clock (CLKIN) and all six outputs. The GA1110E offers the user an option of 14 different output clock configurations. Using the external feedback capability and the two select pins, (S1 and S0), the desired phase relationships of the output clocks can be chosen to best solve the system's clocking requirements. (Refer to the GA1110E data sheet for additional details.)

The delay between the input CLKIN and any of the feedback outputs, Q0–Q5, is restricted to between ± 250 ps (typical) ± 1000 ps (maximum). The skew between any two outputs is typically ± 250 ps ± 500 ps (maximum).

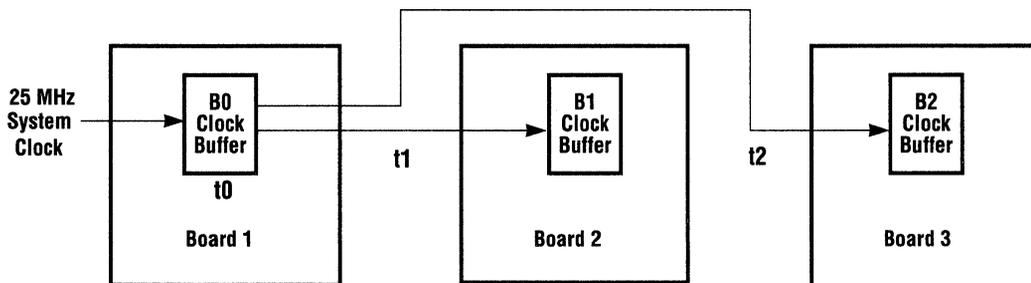
GA1110E Applications

The need to control clock skew normally arises out of a need to negate the skew inadvertently produced by functional partitioning and circuit implementation of a design. Listed below are six typical applications that demand rigid control over clock skews:

1. Clock distribution between boards
2. Clock distribution within a board
3. Clock distribution in very fast state machine designs
4. Balancing of trace lengths
5. Synchronization of device output clock to system clock
6. Fast de-metastabilization in synchronizers.

Each of these applications is discussed in the following pages. Corresponding to these applications, superior solutions using TriQuint's GA1110E are also described.

Figure 3. Clock Distribution Between Boards



Clock Distribution Between Boards

A typical implementation of clock distribution between boards is shown in Figure 3. As an example, assume that a system using a 25 MHz clock is designed using three boards: Board 1, Board 2, and Board 3. Assume also that Board 1 takes in the system clock directly; a clock buffer, B0, on Board 1 supplies the system clock to the clock buffers, B1 and B2, on the other two boards; and the skew budget between boards is 5 ns. Let “t0” be the input-to-output delay and the relative output skew of buffer B0. Time “t1” is the sum of the input trace length delay to Board 2, the input-to-output delay and the relative output skew of B1. Time “t2” is the sum of the input trace length delay to Board 3, the input-to-output delay, and the relative output skew of B2.

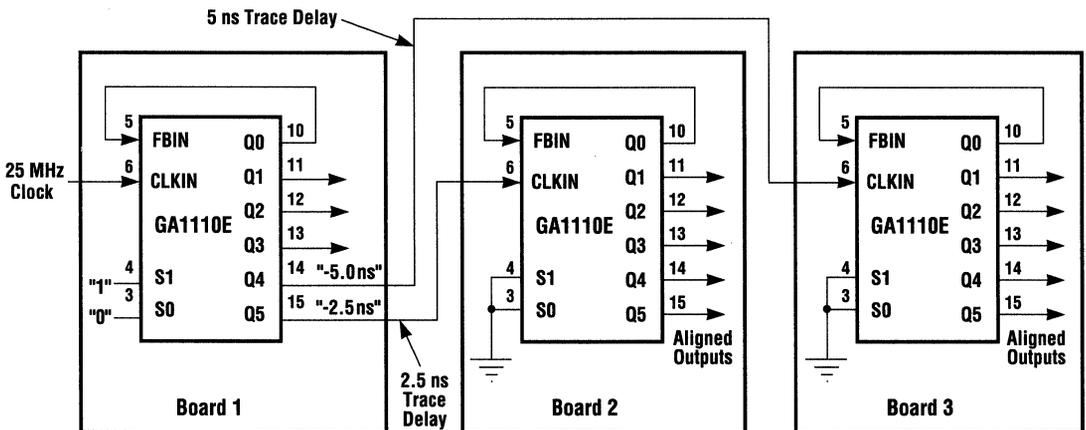
For this case, it is imperative that “t0 + t1” or “t0 + t2” be consistently within the 5 ns window. Using current silicon solutions, this is a complex and difficult goal to achieve because: 1) the designer must define a multi-dimensional envelope for the skew around the power supply, operating temperatures, and worst-case loading of the clock signals, and 2) the production flow must

manage the accuracy of components used, to stay within the envelope. For a 25 MHz system, this skew budget of 5 ns would still imply a 12.5% performance penalty.

Since TriQuint’s GA1110E provides a symmetric 24 mA drive with a ± 250 ps typical input-to-output delay and a ± 250 ps typical skew between outputs, it is ideal for distributing clocks between boards in the example represented by Figure 3.

The clock interconnection using the GA1110E is shown in Figure 4. It is assumed that the Board 1 to Board 2 trace delay is 2.5 ns, and the Board 1 to Board 3 trace delay is 5 ns. On Board 1, the GA1110E is configured as per the data sheet Configuration #7, wherein output Q0 is fed back through the FBIN input of the PLL, and the select pins, S1 and S0, are configured for “1” and “0”, respectively. This configuration utilizes the edge placement capability in discrete increments of 2.5 ns for a 25 MHz input clock. The Q4 output provides a 2.5 ns early edge, and it compensates for the trace length delay of 2.5 ns. Similarly, the Q5 output provides a 5 ns

Figure 4. Clock Distribution Between Boards using the GA1110E



early edge, and compensates for the trace length delay of 5 ns. Hence, the GA1110E output on Board 2 and Board 3 will be synchronized to the 25 MHz system clock, with a typical skew of ± 1.5 ns and a maximum skew of ± 4 ns (maximum input-to-output delay and relative output skew at Board 1 + the maximum input-to-output delay and relative output skew at Boards 2 or 3). With this implementation, the performance penalty will be reduced to within 10.0% for a 25 MHz system.

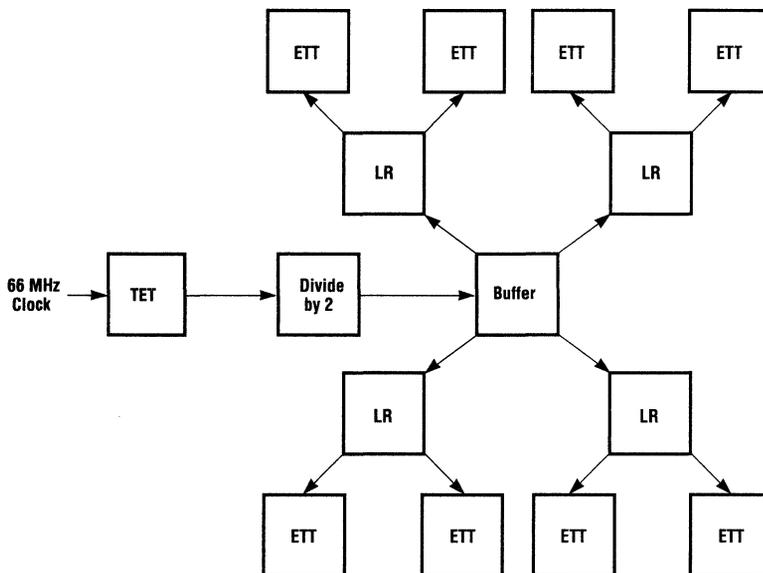
Clock Distribution Within a Board

An example of clock distribution strategy within a board is shown in Figure 5. In this design, the system clock branches out from the center of the board. An input from a crystal oscillator at twice the required frequency is used, and this clock is fed into a TTL-to-ECL translator (TET). The output of the translator is shaped into a system clock with a 50% duty cycle by a divide-by-2 circuit. This, in turn, is buffered by a set of line drivers that feed the system clock to the four corners of the board via differential transmission lines.

The differential transmission lines are used to minimize the effect of common mode noise in the system. The clock is received at the four corners by differential receivers (LR), and is converted back to TTL levels with the help of ECL-to-TTL translators (ETT). The outputs of the ETT are distributed to the TTL loads with careful balancing of the number of loads and trace lengths for each, in order to minimize the skew. This method of clock distribution is known as “star distribution”, and is typically used to minimize the skew between different sections of a large board.

The major disadvantage of this solution is that it needs TTL-to-ECL translators, dual power supplies in a TTL environment, buffers, differential receivers, differential transmission lines, and terminating resistors. This results in a total of 16 Dual-Inline Packages which could use up as much as 8% of the total board space available for a 200-IC board. Moreover, this configuration would still not guarantee a skew in the 2-3 ns range over the full temperature and voltage range.

Figure 5. 33 MHz Clock Distribution Within a Board



Clock Distribution Techniques

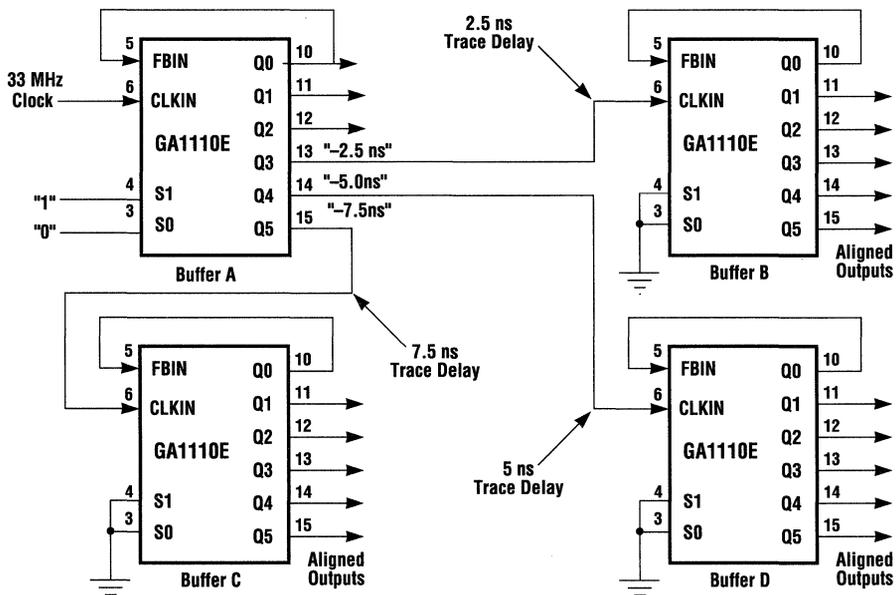
Since the GA1110E fulfills the dual requirements of low input-to-output delay and low skew between outputs, it can be effectively used to distribute the system clock within a board. In addition, the output of the GA1110E is symmetrical, even though the input may not be. This method of distribution provides a very reliable, simple and economical solution using only four components with consistent performance over full operating conditions. GA1110Es can be configured in clock trees with a typical skew of less than ± 500 ps per stage.

A typical clock distribution strategy to replace the "star configuration" on a board using the GA1110E is shown in Figure 6. In this figure, four GA1110E chips (Buffers A, B, C, and D) are used on a board to provide the clock distribution. Buffer A takes in the 33 MHz system clock and distributes it to Buffers B, C, D, and to a few of the clock loads on the board. Each of the buffer outputs can source and sink up to a maximum of 24 mA. In this

example, for Buffer A, the S1 and S0 select pins are chosen to be "1" and "0", respectively, and the Q1 output is used as the feedback input. This wiring corresponds to Configuration #8, mentioned in the data sheet. In this configuration, five of the outputs precede the rising edge of the input clock. Q0, Q2 and Q3 precede it by 2.5 ns, Q4 by 5 ns, and Q5 by 7.5 ns. As depicted in Figure 6, the Q3, Q4, and Q5 outputs compensate for 2.5 ns, 5.0 ns, and 7.5 ns of trace delays, respectively. Buffers B, C, and D have their select pins, S1 and S0, grounded and the Q0 output is fed back to the FBIN input, corresponding to Configuration #1 in the data sheet. These three buffers provide aligned outputs, and therefore are used for shorter distance applications where the delay due to the trace lengths and the loads are negligible.

Clock distribution using the GA1110E, as described above, provides a very reliable, simple, economical

Figure 6. Clock Distribution Within a Board using the GA1110E



solution, using fewer components and providing better performance than any traditional solutions. GA1110Es can be connected in a tree fashion, with less than 2.0 ns of skew in each stage. For the clock distribution shown in Figure 6, assume the trace length delays from Buffer A to Buffer B, Buffer C, and Buffer D are exactly 2.5 ns, 7.5 ns, and 5 ns, respectively. Under these conditions, the total clock skew on the board at any point is typically ± 1.5 ns and is ± 4 ns worst case, (consisting of two clock buffer skews). As discussed previously, an equivalent solution using a mix of TTL/ECL would take nearly four times as many packages, would need careful balancing of trace lengths, and would result in a very involved board layout and a larger skew.

Balancing Trace Lengths

As mentioned in the previous section, a common method to limit the skew between different clock signals is to balance the number of loads per clock buffer output and the trace lengths to each of the loads. In this situation, 74AS1808 or 74AS1804 drivers are typically used, and the outputs are carefully balanced with respect to the trace lengths and number of loads, as shown in Figure 7. The clock buffer has four outputs, with each output driving six loads over identical lengths, "L1". To achieve this, extra care is taken in laying out the board. In spite of this, the skew parameters continue to be susceptible to propagation delays of the AS parts, variations in temperature and the power supply. As an alternative, imprecise delay lines could be used to improve the performance of the system. Though active delay lines can be effective for a narrow range of operations, they are not stable over wide temperature and power supply variations.

Since the GA1110E provides outputs whose relative edges can be precisely controlled, it can be used to effectively compensate for varying trace lengths on its

output signals. This simplifies the task of laying out the board. An example of the compensation for trace length delays is shown in Figure 8. In this example, the GA1110E operates as per Configuration #8, defined in the data sheet. For a 50 MHz clock input, the phase increment t_{PH} , as per the GA1110E data sheet is 2.5 ns. Hence Q0 and Q2 will have 2.5 ns early edges and can be used to compensate for trace delays of 2.5 ns. For other cases of varying trace lengths, the GA1110E can be appropriately configured.

Figure 7. Clock Distribution using Trace Length Balancing

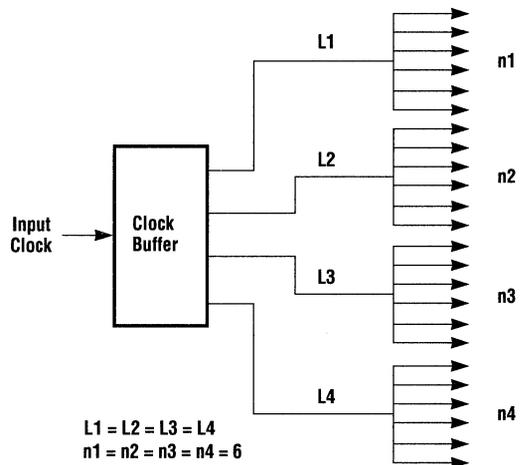
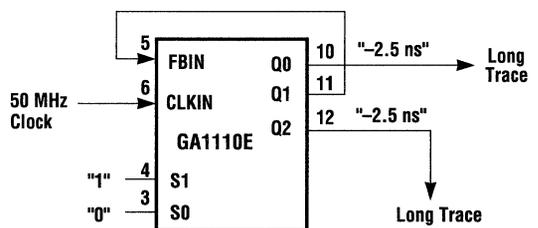


Figure 8. Clock Compensation for Trace Length Variations



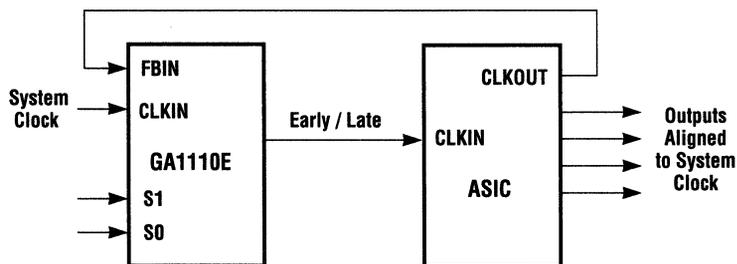
Clock Distribution Techniques

Synchronous Output Clock

The fourth area requiring controlled clock skew is in applications in which a device's output clock is intended to be synchronous to a system clock. In such applications, the delay of the clock through the device will reduce the timing margin available for the rest of the system to interface to the device. For example, an ASIC may have its output signals be a function of its output clock, which is an internally buffered and delayed version of the system clock; whereas the rest of the circuits on a board are clocked by the system clock. In such a case, it is necessary to make the output clock of the ASIC synchronous to the system clock, to ensure better timing margins for other parts interfacing to the ASIC.

An example of such an application using the GA1110E is shown in Figure 9. Here, one of the outputs from the GA1110E is fed into the ASIC, and the ASIC's output clock is then fed back through the FBIN pin. S1 and S0 are configured to provide the appropriate early or late edge to compensate the delay through the internal buffer of the ASIC. This simple loopback connection synchronizes the output clock of the ASIC to the system clock.

Figure 9. Synchronizing the Device Clock to the System Clock



Note: S1 and S0 are chosen depending upon the delay within the ASIC. The Early/Late output will match the internal delay within the ASIC.

Clock Distribution in Fast State Machines

A fifth application requiring a rigid control of clock skew is in high-speed state machine designs.

Quite often, a section of the state machine is slower than the rest of the design and becomes the limiting factor for overall performance. To overcome this, the clock to the slower stages can be delayed in precise increments. With delay lines, the delay cannot be guaranteed over temperature, voltage, or trace length. For a high-speed state machine design such as this, the GA1110E's ability to do precise edge placements of clocks becomes invaluable.

Figure 10 shows an example of a two-stage state machine operating at 40 MHz. Suppose the delay through the first stage is 18 ns and the delay through the second stage is 22.5 ns. If the setup time required for the flip-flop is 5 ns, one would need to use a 27.5 ns clock for the state machine, which translates into either a two-clock cycle or a "wait state." By using the GA1110E, however, the clock to the first stage can be delayed by 2.5 ns and thus meet the setup time requirement of the two stages.

Figure 10. Application of the GA1110E in State Machine Design

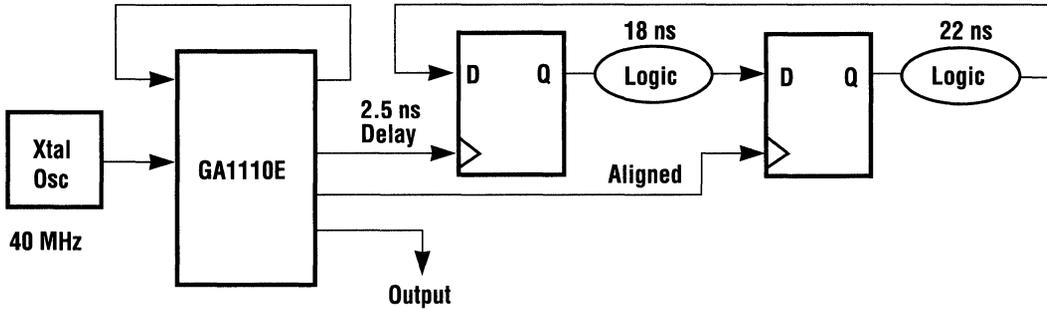
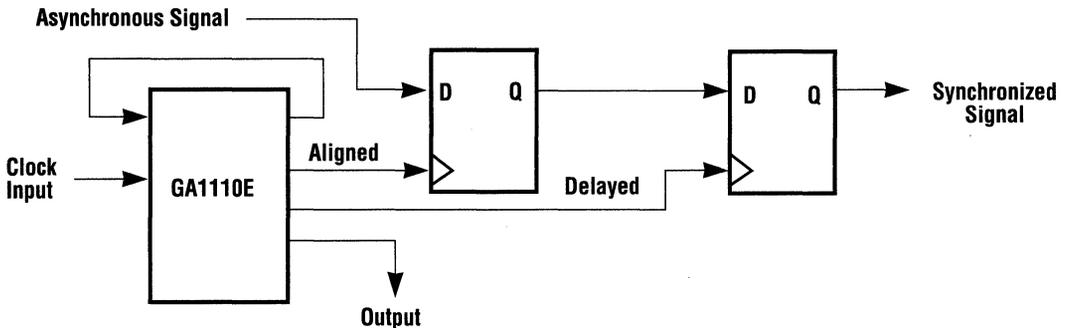


Figure 11. Application of the GA1110E in De-Metastabilization



Fast De-Metastabilization in Synchronizers

The sixth application for clock control arises in fast de-metastabilization of asynchronous events. Normally, this is accomplished by clocking the events in two stages. If the clock period is less than the time required for de-metastabilization, it may be prudent to delay the clock in fixed increments to the second stage, resolving the metastability faster than incurring an extra clock delay. This staggering of the clocks can be implemented using the GA1110E as shown in Figure 11.

Conclusion

This application note presents various clock distribution-related problems frequently encountered by the design community. TriQuint offers simple solutions to relatively complex clock problems using the versatility of the GA1110E. The GA1110E not only solves clock distribution problems, but it also offers consistent and predictable performance over the full standard commercial operating ranges.

Clock Distribution Techniques

Additional Information

For latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com Tel: (503) 615-9000

Email: sales@tqs.com Fax: (503) 615-8900

For technical questions and additional information on specific applications:

Email: applications@tqs.com

The information provided herein is believed to be reliable; TriQuint assumes no liability for inaccuracies or omissions. TriQuint assumes no responsibility for the use of this information, and all such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. TriQuint does not authorize or warrant any TriQuint product for use in life-support devices and/or systems.

Copyright © 1997 TriQuint Semiconductor, Inc. All rights reserved.

Revision 1.0.A October 1997



Section 8 — Sales and Distribution

<i>Sales Representatives – North America</i>	<i>8-3</i>
<i>Sales Representatives – International</i>	<i>8-7</i>
<i>Distributors – North America</i>	<i>8-8</i>
<i>TriQuint Semiconductor Inc. – Area Sales Offices</i>	<i>8-11</i>

Sales Representatives — North America

ALABAMA

Concord Component Reps, Inc.

190 Lime Quarry Road, Suite 102
Madison, AL 35758
(205) 772-8883 Fax (205) 772-8262
E-Mail: jeannie@us3.global.ibmmail.com

ARIZONA

Oasis Sales, Inc.

301 E Bethany Home Road, #A135
Phoenix, AZ 85012
(602) 277-2714 Fax (602) 263-9352
E-Mail: shelley@oasisales.com

ARKANSAS

Mil-Rep Associates

1755 N. Collins Boulevard, Suite 215
Richardson, TX 75080
(972) 644-6731 Fax (972) 644-8161
E-mail: rshed@earthlink.net

CALIFORNIA (Northern)

RF Associates North, Inc.

(Wireless products only)
1277 Borregas Avenue
Sunnyvale, CA 94089
(408) 752-7000 Fax (408) 752-7015
E-Mail: robxfan@ricochet.net
www.rfan.com

Paragon Technical

1740 Technology Drive, Suite 110
San Jose, CA 95110
(415) 562-3634 Fax (415) 598-0361
E-Mail: groff@slip.net

CALIFORNIA (Southern)

Centaur Corporation

(Digital products only)
17802 Sky Park Circle, Suite 100
Irvine, CA 92614
(714) 261-2123 Fax (714) 261-2905
E-Mail: Arlenemo@oal.com

26635 Agoura Rd., Suite 101
Calabasas, CA 91302
(818) 878-5800 Fax (818) 878-5818
E-Mail: Arlenemo@oal.com

3914 Murphy Canyon Road, Suite 125
San Diego, CA 92123
(619) 278-4950 Fax (619) 278-0649
E-Mail: Arlenemo@oal.com

S&S Technology

(Wireless products only)
17130 Devonshire St., Suite 202
Northridge, CA 91325
(818) 366-2866 Fax (818) 366-2486
E-Mail: Lwstille@aol.com

33021 Seawatch
Dana Point, CA 92629
(714) 661-4619 Fax (714) 661-6097
E-Mail: tcirillo@msn.com

1760 Oliver Avenue
San Diego, CA 92109
(619) 484-2996 Fax (619) 484-3144
E-Mail: cgerwig156@aol.com

2692 Main Way Dr.
Rossmoor, CA 90720
(310) 431-7000 Fax (310) 431-0285
E-Mail: Tritacco@msn.com

CANADA

Electrosources

230 Galaxy Boulevard
Rexdale, Ontario, Canada M9W 5RB
(417) 675-4490 Fax (416) 675-6871

6875 Royal Oak Ave
Burnaby, BC Canada V5J 4J3
(604) 435-2533 Fax (604) 435-2538

2635 37th Ave NE Suite 245
Calgary, Alberta Canada T1Y 5Z6
(403) 735-6230 Fax (403) 735-0599

300 March Road, Suite 203
Kanata, Ontario Canada K2k 2E2
(613) 592-3214 Fax (613) 592-4256

6600 Trans Canada Hwy Suite 420
Pointe Claire, Quebec Canada H9R 452
(514) 630-7486 Fax (514) 630-742

COLORADO

Elcom, Inc.

12200 E Briarwood Avenue, Suite 175
Englewood, CO 80112
(303) 792-3330 Fax (303) 792-2221
E-Mail: info@elcom-inc.com
www.elcom-inc.com

CONNECTICUT

Focus Sales, Inc.

(Digital products only)
645 County Street, Unit 6
Taunton, MA 02780
(800) 933-2771 Fax (508) 823-4692
E-Mail: focussales@mcimail.com
www.focussalesinc.com

Stone Components

(Wireless products only)
8 Frost St.
Natick, MA 01760
(508) 875-3266 Fax (508) 875-0537
E-Mail: sc2@ix.netcom.com

Ascor

40 Commerce Place
Suite 202
Hicksville, NY 11801
(516) 939-6161 Fax (516) 939-6174

DELAWARE

Nexus Technology Sales

200 Lakeside Drive, Suite 236
Horsham, PA 19044
(215) 675-9600 Fax (215) 675-9604
E-Mail: nexusp@aol.com

FLORIDA

Dyne-A-Mark Corporation

742 Penguin Ave NE
Palm Bay, FL 32907
(407) 725-7470 Fax (407) 984-2718
E-Mail: swdamc@interserv.com

508 Palm Dr.
Largo, FL 33770
(813) 586-3778 Fax (813) 586-3863
E-Mail: swdamc@interserv.com

500 Winderley Place, Suite 100
Maitland, FL 32751
(407) 660-1661 Fax (407) 660-9407
E-Mail: swdamc@interserv.com

3351 NW 55th Street
Ft. Lauderdale, FL 33309
(954) 485-3500 Fax (954) 485-6555
E-Mail: swdamc@interserv.com

Sales Representatives — North America (continued)

GEORGIA

Concord Component Reps, Inc.

6825 Jimmy Carter Boulevard, Suite 1303
Norcross, GA 30071
(770) 416-9597 Fax (770) 441-0790
E-Mail: jeannie@us3.global.ibmmail.com

IDAHO

Elcom, Inc.

12200 E Briarwood Avenue, Suite 175
Englewood, CO 80112
(303) 792-3330 Fax (303) 792-2221
E-Mail: info@elcom-inc.com
www.elcom-inc.com

ILLINOIS (Northern)

Oasis Sales

1101 Tonne Road
Elk Grove Village, IL 60007
(847) 640-1850 Fax (847) 640-9432
E-Mail: phodapp@oasis-sales.com

ILLINOIS (Southern)

Central Tech Sales

4 Holly Lane
Florissant, MO 63033
(314) 831-4069 Fax (314) 839-4686
E-Mail: klynch0514@aol.com

INDIANA

Applied Data Management

P.O. Box 213
Batesville, IN 47006-0213
(317) 257-8949 Fax (513) 579-8510
E-Mail: 73561.1365@compuservice.com

Applied Data Management

639 South Main St.
Chelsea, MI 48118
(313) 475-0523 Fax (313) 475-0329
E-Mail: 73561.1365@compuservice.com

IOWA

Oasis Sales Corp.

4905 Lakeside Drive NE, Suite 203
Cedar Rapids, IA 52402
(319) 377-8738 Fax (319) 377-8803
E-Mail: phodapp@oasis-sales.com

KANSAS

Central Tech Sales

4 Holly Lane
Florissant, MO 63033
(314) 831-4069 Fax (314) 839-4686
E-Mail: klynch0514@aol.com

KENTUCKY

Applied Data Management

435 Dayton Street
Cincinnati, OH 45214
(513) 579-8108 Fax (513) 579-8510
E-Mail: 73561.1365@compuservice.com

LOUISIANA

Mil-Rep Associates

13810 Champion Forest Dr., Suite 145
Houston, TX 77069
(281) 444-2557 Fax (281) 444-2751

MAINE

Focus Sales, Inc.

(Digital products only)
645 County Street, Unit 6
Taunton, MA 02780
(800) 933-2771 Fax (508) 823-4692
E-Mail: focussales@mcimail.com
www.focussalesinc.com

Stone Components

(Wireless products only)
8 Frost St.
Natick, MA 01760
(508) 875-3266 Fax (508) 875-0537
E-Mail: sc2@ix.netcom.com

MARYLAND

New Era Sales

890 Airport Park Road, Suite 103
Glen Burnie, MD 21061
(410) 761-4100 Fax (410) 761-2981
E-Mail: brucenes@aol.com

MASSACHUSETTS

Focus Sales, Inc.

(Digital products only)
645 County Street, Unit 6
Taunton, MA 02780
(800) 933-2771 Fax (508) 823-4692
E-Mail: focussales@mcimail.com
www.focussalesinc.com

Stone Components

(Wireless products only)
8 Frost St.
Natick, MA 01760
(508) 875-3266 Fax (508) 875-0537
E-Mail: sc2@ix.netcom.com

MICHIGAN

Applied Data Management

639 South Main Street
Chelsea, MI 48118
(313) 741-9292 Fax (313) 741-9292
E-Mail: 73561.1365@compuservice.com

MINNESOTA

Oasis Sales Corporation

4620 West 77th Street, Suite 100
Edina, MN 55435
(612) 841-1088 Fax (612) 841-1103
E-Mail: phodapp@oasis-sales.com

MISSISSIPPI

Concord Component Reps, Inc.

190 Lime Quarry Road, Suite 102
Madison, AL 35758
(205) 772-8883 Fax (205) 772-8262
E-Mail: jeannie@us3.global.ibmmail.com

MISSOURI

Central Tech Sales

4 Holly Lane
Florissant, MO 63033
(314) 831-4069 Fax (314) 839-4686
E-Mail: klynch0514@aol.com

MONTANA

Elcom, Inc.

12200 E Briarwood Avenue, Suite 175
Englewood, CO 80112
(303) 792-3330 Fax (303) 792-2221
E-Mail: info@elcom-inc.com
www.elcom-inc.com

NEBRASKA

Central Tech Sales

4 Holly Lane
Florissant, MO 63033
(314) 831-4069 Fax (314) 839-4686
E-Mail: klynch0514@aol.com

Sales Representatives — North America (continued)

NEVADA (Northern)

RF Associates North, Inc.
(Wireless products only)
1277 Borregas Avenue
Sunnyvale, CA 94089
(408) 752-7000 Fax (408) 752-7015
E-Mail: robrfan@ricochet.net
www.rfan.com

Paragon Technical

1740 Technology Drive, Suite 110
San Jose, CA 95110
(415) 562-3634 Fax (415) 598-0361
E-Mail: groff@slip.net

NEVADA (Southern)

Oasis, Sales Inc.
301 E Bethany Home Rd., Suite A-135
Phoenix, AZ 85012
(602) 277-2714 Fax (602) 263-9352
E-Mail: phodapp@oasis-sales.com

NEW HAMPSHIRE

Focus Sales, Inc.
(Digital products only)
645 County Street, Unit 6
Taunton, MA 02780
(800) 933-2771 Fax (508) 823-4692
E-Mail: focussales@mcimail.com
www.focussalesinc.com

Stone Components

(Wireless products only)
8 Frost St.
Natick, MA 01760
(508) 875-3266 Fax (508) 875-0537
E-Mail: sc2@ix.netcom.com

NEW JERSEY (Northern)

ASCOR Electronics, Inc.
40 Commerce Place, Suite 202
Hicksville, NY 11801
(516) 939-6161 Fax (516) 939-6174
E-Mail: ascorelec@aol.com

NEW JERSEY (Southern)

Nexus Technology Sales
200 Lakeside Drive, Suite 236
Horsham, PA 19044
(215) 675-9600 Fax (215) 675-9604
E-Mail: nexuspa@aol.com

NEW MEXICO

Nelco Electronix
3240 C Juan Tabo Blvd. NE
Albuquerque, NM 87111
(505) 293-1399 Fax (505) 293-1011
E-Mail: nelco@swcp.com

NEW YORK

ASCOR Electronics, Inc.
40 Commerce Place, Suite 202
Hicksville, NY 11801
(516) 939-6161 Fax (516) 939-6174
E-Mail: ascorelec@aol.com

Tri-Tech Electronics

1043 Front Street
Binghamton, NY 13905
(607) 722-3580 Fax (607) 722-3774
E-Mail: tritech@eznet.net

349 West Commercial St., Suite 2585
E. Rochester, NY 14445
(716) 385-6500 Fax (716) 385-7655
E-Mail: tritech@eznet.net

NORTH CAROLINA

New Era Sales, Inc.
1215 Jones Franklin Road, Suite 201
Raleigh, NC 27606-3351
(919) 859-4400 Fax (919) 859-6167
E-Mail: brucenes@aol.com

NORTH DAKOTA

Oasis Sales Corporation
7805 Telegraph Road, Suite 210
Bloomington, MN 55438
(612) 941-1917 Fax (612) 941-5701
E-Mail: phodapp@oasis-sales.com

OHIO

Applied Data Management
435 Dayton Street
Cincinnati, OH 45214
(513) 579-8108 Fax (513) 579-8510
E-Mail: 73561.1365@compuserve.com

277 Shelton Blvd.
East Lake, OH 44095
(216) 946-6812 Fax (216) 946-6812
E-Mail: 73561.1365@compuserve.com

OKLAHOMA

Mil-Rep Associates
1755 N. Collins Blvd., Suite 215
Richardson, TX 75080
(972) 644-6731 Fax (972) 644-8161
E-mail: rshed@earthlink.net

OREGON

Thorson Pacific, Inc.
9600 SW Oak Street, Suite 320
Portland, OR 97223
(503) 293-9001 Fax (503) 293-9007
E-Mail: info@thorsonor.com

PENNSYLVANIA (Western)

Applied Data Management
435 Dayton Street
Cincinnati, OH 45214
(513) 579-8108 Fax (513) 579-8510
E-Mail: 73561.1365@compuserve.com

PENNSYLVANIA (Eastern)

Nexus Technology Sales
200 Lakeside Drive, Suite 236
Horsham, PA 19044
(215) 675-9600 Fax (215) 675-9604
E-Mail: nexuspa@aol.com

PUERTO RICO

Dyne-A-Mark
500 Winderley Place, Suite 100
Maitland, FL 32751
(407) 660-1661 Fax (407) 660-9407
E-Mail: swdamc@interserv.com

RHODE ISLAND

Focus Sales, Inc.
(Digital products only)
645 County Street, Unit 6
Taunton, MA 02780
(800) 933-2771 Fax (508) 823-4692
E-Mail: focussales@mcimail.com
www.focussalesinc.com

Stone Components

(Wireless products only)
8 Frost St.
Natick, MA 01760
(508) 875-3266 Fax (508) 875-0537
E-Mail: sc2@ix.netcom.com

Sales Representatives — North America (continued)

SOUTH CAROLINA

New Era Sales, Inc.

1215 Jones Franklin Road, Suite 201
Raleigh, NC 27606-3351
(919) 859-4400 Fax (919) 859-6167
E-Mail: brucenes@aol.com

SOUTH DAKOTA

Oasis Sales Corporation

7805 Telegraph Road, Suite 210
Bloomington, MN 55438
(612) 941-1917 Fax (612) 941-5701
E-Mail: phodapp@oasis-sales.com

TENNESSEE

Concord Component Reps

190 Lime Quarry Road, Suite 102
Madison, AL 35758
(205) 772-8883 Fax (205) 772-8262
E-Mail: jeannie@us3.global.ibmmail.com

TEXAS

Mil-Rep Associates

1755 N. Collins Blvd., Suite 215
Richardson, TX 75080
(972) 644-6731 Fax (972) 644-8161
E-Mail: rshed@earthlink.net

13810 Champion Forest Dr., Suite 145
Houston, TX 77069
(281) 444-2557 Fax (281) 444-2751
E-Mail: skhart@swbell.net

9009 Mountain Ridge Drive, Suite 230
Austin, TX 78759
(512) 346-6331 Fax (512) 346-1975
E-Mail: teaneyk@aol.com

Nelco Electronix

(El Paso, Texas Only)
742 Moffat Drive
El Paso, TX 79912
(915) 833-7300 Fax (915) 833-1771
E-Mail: nelco@swcp.com

UTAH

Elcom, Inc.

3349 S. Main Street
Salt Lake City, UT 84115
(801) 486-7775 Fax (801) 486-7773
E-Mail: info@elcom-inc.com
www.elcom-inc.com

VERMONT

Focus Sales, Inc.

(Digital products only)
645 County Street, Unit 6
Taunton, MA 02780
(800) 933-2771 Fax (508) 823-4692
E-Mail: focussales@mcimail.com
www.focussalesinc.com

Stone Components

(Wireless products only)
8 Frost St.
Natick, MA 01760
(508) 875-3266 Fax (508) 875-0537
E-Mail: sc2@ix.netcom.com

VIRGINIA

New Era Sales

1711 Milton Road
Charlottesville, VA 22902
(804) 979-4997
E-Mail: nighnes@aol.com

WASHINGTON

Thorson Pacific, Inc.

14575 Bel-Red Road, Suite 102
Bellevue, WA 98007
(425) 603-9393 Fax (425) 603-9380
E-Mail: thorsonwa@aol.com

WASHINGTON, DC

New Era Sales

890 Airport Park Road, Suite 103
Glen Burnie, MD 21061
(410) 761-4100 Fax (410) 761-2981
E-Mail: brucenes@aol.com

WEST VIRGINIA

New Era Sales

890 Airport Park Road, Suite 103
Glen Burnie, MD 21061
(410) 761-4100 Fax (410) 761-2981
E-Mail: brucenes@aol.com

WISCONSIN

Oasis Sales Corporation

1305 N Barker Road
Brookfield, WI 53005
(414) 782-6660 Fax (414) 782-7921
E-Mail: phodapp@oasis-sales.com

WYOMING

Elcom, Inc.

12200 E Briarwood Avenue, Suite 175
Englewood, CO 80112
(303) 792-3330 Fax (303) 792-2221
E-Mail: info@elcom-inc.com
www.elcom-inc.com

Sales Representatives — International

BELGIUM/LUXEMBOURG

Nijkerk N.V. / S.A.

Noorderlaan 111
B-2030 Antwerpen, Belgium
+32 3 544 8112 Fax +32 3 544 9901
E-mail: ne@nijkerk.beCANADA

CANADA

(See Sales Representatives – North America)

DENMARK

Wyle Ginsbury Electronics A/S

Lerhoej 15
DK-2880 Bagsvaerd Denmark
+45 4444 6666 Fax +45 4444 6669
E-mail: ginsdk@datashopper.dk

GERMANY/AUSTRIA

Metronik

Leohardsweg 2
D-82002 Unterhaching
Germany
+49 89-61108-152 Fax +49 89-61108-155

HONG KONG AND CHINA

MEMEC (Asia Pacific) Ltd.

Unique Hong Kong Office
Unit 3607, Tower 1, Metroplaza
Hing Fong Road, Kwai Fong, N.T.
Hong Kong
852-2410 2778 Fax 852-2370 3247
E-mail: panson@memec-asiapacific.com

Unique Beijing Office
Rm 593, Pana Tower, 128 Zhichun Road
Haidan District, Beijing, China 100086
86-10-6262 8869 Fax 86-10-6262 8890

Unique Shanghai Office
Room 2361, West Building, Jin Jiang Hotel
59 Mao Ming Road South
Shanghai, China 200020
86-21-6258 2582 Ext. 2361
Fax 86-21-6445 0186

Unique Chengdu Office
Room 2008, Tong Mei Mansion
No. 76, Section 1, Jianshe North Road,
Chengdu, Sichuan, China
86-28-339-6639
86-28-339 6631

MEMEC (Asia Pacific) Ltd. (continued)

Unique Shenzhen Office
Room 705, Bao Hua Building
Hua Qiang North Road
Shenzhen, China
86-755-323 0460
86-755-323 0471

ISRAEL

RDT Components Ltd.

ATIDIM, Nevah Sharet
P.O. Box 58013
Tel-Aviv 61580 Israel
+972 3 645 0707 Fax +972 3 492 413
Email: mron@rdt.co.il

ITALY

MicroElit S.P.A.

Via Sardegna, 1
I-20146 Milano, Italy
+39 24 81 79 00 Fax +39 24 81 35 94

Via Marchesse, 10
I-00141 Roma, Italy
+39 68 68 94 323 Fax +39 66 82 75 270

JAPAN

Macnica, Inc.

Hakusan High-Tech Park
1-22-2 Hakusan, Midori-ku
Yokohama-city, 226 Japan
81 45 939 6140 Fax 81 45 939 6141
E-Mail: yoy@cg.macnica.co.jp

5-11-8 Nishinakashima, Yodogawa-ku
Osaka-city, 532 Japan
81 6 300 0810 Fax 81 6 300 0848
E-Mail: yoy@cg.macnica.co.jp

1-14-13 Aoi, Higashi-ku
Nagoya-city, 461 Japan
81 52 933 4541 Fax 81 52 933 4542
E-Mail: yoy@cg.macnica.co.jp

4-2-10 Odori
Utsunomiza-city, 320 Japan
81 286 27 5231 Fax 81 286 27 5274
E-Mail: yoy@cg.macnica.co.jp

KOREA

MEMEC (Asia Pacific) Ltd.

Unique Korea Branch
708-10 Daeha Building, 7/F
#14-11, Yoido-Dong,
Yongdeungpo-Ku,
Seoul, Korea
82-2 786 6540 Fax 82-2 786 6542
E-mail: essin@memec-korea.com

MEXICO

(See Distributors – North America)

NETHERLANDS

Nijkerk Electronika B.V.

Drentestraat 7, 1083HK Amsterdam
PO Box 7920, 1008 AC Amsterdam
The Netherlands
+31 20 504 1424 Fax +31 20 642 3948
E-Mail: ne@nijkerk.nl
www.nijkerk.nl
Semiconductor Sales Department
+31 20 504 1435TAIWAN

Jeritronics Ltd.

7F, No. 267, Sec. 3
Cheng-Teh Road
Taipei, Taiwan
886 2 585 1636 Fax 886 2 586 4736
E-Mail: jeritron@tpts1.seed.net.tw

UNITED KINGDOM

Pronto Electronic Systems, Ltd.

City Gate House, 399-425 Eastern Ave.
Gants Hill, Ilford
Essex, United Kingdom IG26LR
+44 181 55 46 222 Fax +44 181 51 83 222
E-Mail: 100126.2424@compuserve.com

Distributors – North America

ALABAMA

Nu Horizons Electronics

4825 University Square, Suite 8
Huntsville, AL 35816
(205) 722-9330 Fax (205) 722-9348
E-Mail: sales@nuhorizons.com
www.nuhorizons.com

Insight Electronics

4835 University Square, Suite 19
Huntsville, AL 35816
(205) 830-1222 Fax (205) 830-1225
E-Mail: marc-lampert@ins.memec.com
www.ikn.com

ARIZONA

Insight Electronics

1515 W University Drive, Suite 103
Tempe, AZ 85281
(602) 829-1800 Fax (602) 967-2658
E-Mail: marc-lampert@ins.memec.com
www.ikn.com

Nu Horizons

4651 S. Lakeshore Drive, Suite 4
Tempe, AZ 85282
(602) 730-8500 Fax (602) 730-1780

CALIFORNIA

Nu Horizons Electronics

4360 View Ridge Avenue, Suite B
San Diego, CA 92123
(619) 576-0088 Fax (619) 576-0990
E-Mail: sales@nuhorizons.com
www.nuhorizons.com

2070 Ringwood Avenue
San Jose, CA 95131
(408) 434-0800 Fax (408) 434-0935
E-Mail: sales@nuhorizons.com
www.nuhorizons.com

13900 Alton Parkway, Suite 123
Irvine, CA 92618
(714) 470-1011 Fax (714) 470-1104
E-Mail: sales@nuhorizons.com
www.nuhorizons.com

850 Hampshire Rd., Suite R
Thousand Oaks, CA 91361
(805) 370-1515 Fax (805) 370-1525
E-Mail: sales@nuhorizons.com
www.nuhorizons.com

Insight Electronics

9980 Huennekens Street
San Diego, CA 92121
1 (800) 677-6011 Fax (619) 677-3151
E-Mail: marc-lampert@ins.memec.com
www.ikn.com

2 Venture Plaza, Suite 340
Irvine, CA 92618
(714) 727-3291 Fax (714) 727-1804
E-Mail: marc-lampert@ins.memec.com
www.ikn.com

4333 Park Terrace Drive, Suite 101
Westlake Village, CA 91361
(818) 707-2101 Fax (818) 707-0321
E-Mail: marc-lampert@ins.memec.com
www.ikn.com

2460 N. First St., Suite 170
San Jose, CA 95131
(408) 526-2100 Fax (408) 526-0250
E-Mail: marc-lampert@ins.memec.com
www.ikn.com

CANADA

Insight Electronics

560-1212 31st Avenue NE
Calgary, Alberta Canada T2E 7T1
(403) 250-8822 Fax (403) 250-8851
E-Mail: marc-lampert@ins.memec.com
www.ikn.com

955 Boulevard St. Jean, Suite 301
Pointe Claire, Canada H9R 5K3
(514) 428-0060 Fax (514) 428-0070
E-Mail: marc-lampert@ins.memec.com
www.ikn.com

240 Catherine St., Suite 405
Ottawa, Ontario, Canada K2P 2G8
(613) 233-1799 Fax (613) 233-2843
E-Mail: marc-lampert@ins.memec.com
www.ikn.com

141-6151 Westminster Hwy.
Richmond, BC, Canada V7C 4V4
(604) 270-3232 Fax (604) 270-3356
E-Mail: marc-lampert@ins.memec.com
www.ikn.com

1 Eva Road, Suite 107
Etobicoke, Ontario, Canada M9C 4Z5
(416) 622-7006 Fax (416) 622-5155
E-Mail: marc-lampert@ins.memec.com
www.ikn.com

COLORADO

Insight Electronics

2 Inverness Drive East, Suite 102
Englewood, CO 80112
(303) 649-1800 Fax (303) 649-1818
E-Mail: marc-lampert@ins.memec.com
www.ikn.com

CONNECTICUT

Insight Electronics

16 W. Johnson Aveune, Suite 202
Cheshire, CT 06410
(203) 272-5843 Fax (203) 272-5853
E-Mail: marc-lampert@ins.memec.com
www.ikn.com

FLORIDA

Insight Electronics

6400 Congress Ave., Suite 1600
Boca Raton, FL 33487
(561) 997-2540 Fax (561) 997-2542
E-Mail: marc-lampert@ins.memec.com
www.ikn.com

600 North Lake Boulevard, Suite 250
Altamonte Springs, FL 32701
(407) 834-6310 Fax (407) 834-6461
E-Mail: marc-lampert@ins.memec.com
www.ikn.com

17757 US Hwy 19 N, Suite 520
Clearwater, FL 34624
(813) 524-8850 Fax 813 532-4252
E-Mail: marc-lampert@ins.memec.com
www.ikn.com

Nu Horizons Electronics

600 S North Lake Boulevard, Suite 210
Altamonte Springs, FL 32701
(407) 831-8008 Fax (407) 831-8862
E-Mail: sales@nuhorizons.com
www.nuhorizons.com

3421 NW 55th Street
Ft. Lauderdale, FL 33309
(954) 735-2555 Fax (954) 735-2880
E-Mail: sales@nuhorizons.com
www.nuhorizons.com

Distributors — North America (continued)

GEORGIA

Insight Electronics

3005 Breckinridge, Suite 210-A
Duluth, GA 30136
(770) 717-8566 Fax (770) 717-8588
E-Mail: marc-lampert@ins.memec.com
www.ikn.com

Nu Horizons Electronics

100 Pinnacle Way, Suite 155
Norcross, GA 30071
(770) 416-8666 Fax (770) 416-9060
E-Mail: sales@nuhorizons.com
www.nuhorizons.com

IDAHO

Nu Horizons

16399 Franklin Road
Nampa, ID 83687
(208) 465-0818 Fax (208) 465-0883

ILLINOIS

Insight Electronics

1365 Wiley Road, Suite 142
Schaumburg, IL 60173
(847) 885-9700 Fax (847) 885-9701
E-Mail: marc-lampert@ins.memec.com
www.ikn.com

INDIANA

Insight Electronics

4656 W. Jefferson, suite 200
Fort Wayne, IN 46804
(219) 436-4250 Fax (219) 436-4515
E-Mail: marc-lampert@ins.memec.com
www.ikn.com

KANSAS

Insight Electronics

8700 Monrovia, Suite 310
Lenexa, KS 66215
(913) 492-0408 Fax (913) 492-0708
E-Mail: marc-lampert@ins.memec.com
www.ikn.com

MARYLAND

Insight Electronics

6325 Woodside Ct. #130
Columbia, MD 21046
(410) 381-3131 Fax (410) 381-3141
E-Mail: marc-lampert@ins.memec.com
www.ikn.com

Nu Horizons Electronics

8965 Guilford Road, Suite 160
Columbia, MD 21046
(410) 995-6330 Fax (410) 995-6332
E-Mail: sales@nuhorizons.com
www.nuhorizons.com

MASSACHUSETTS

Insight Electronics

25 Corporate Drive, Suite 175
Burlington, MA 01880
(617) 270-9400 Fax (617) 270-3279
E-Mail: marc-lampert@ins.memec.com
www.ikn.com

Nu Horizons Electronics

19 Corporate Place
107 Audubon Road, Bldg. 1
Wakefield, MA 01880
(617) 246-4442 Fax (617) 246-4462
E-Mail: sales@nuhorizons.com
www.nuhorizons.com

MEXICO

Insight Electronics

Prol. Americas 1612 6to piso
Col. Country Club
Guadalajara, Jalisco C.P. MEXICO 44610
011 523 578 92 42 Fax 011 523 678 92 43
E-Mail: marc-lampert@ins.memec.com
www.ikn.com

Reforma 10 col. Centro
World Trade Center Montecito #38
Piso 19, OFNA Col. Napoles
CP. 03810 Mexico City, DF
011 525 488 01 19 Fax 011 528 488 01 79
E-Mail: marc-lampert@ins.memec.com
www.ikn.com

Rio Guadalquivir 322 OTE
Colonia Del Vall, San Pedro
Garza Garcia, NL MEXICO CP66220
011 528 356 64 90 Fax 011 528 356 94 95
E-Mail: marc-lampert@ins.memec.com
www.ikn.com

MICHIGAN

Insight Electronics

802 E Grand River, Suite 101
Brighton, MI 48116
(810) 229-7710 Fax (810) 229-6435
E-Mail: marc-lampert@ins.memec.com
www.ikn.com

Insight Electronics (continued)

1545 N. Riviera
Stevensville, MI 49127
(616) 429-1410 Fax (616) 429-7730
E-Mail: marc-lampert@ins.memec.com
www.ikn.com

MINNESOTA

Insight Electronics

5353 Gamble Drive, Suite 330
St. Louis Park, MN 55416
(612) 525-9999 Fax (612) 525-9998
E-Mail: marc-lampert@ins.memec.com
www.ikn.com

Nu Horizons Electronics

10907 Valley View Rd.
Eden Prairie, MN 55344
(612) 942-9030 Fax (612) 942-9144
E-Mail: sales@nuhorizons.com
www.nuhorizons.com

MISSOURI

Insight Electronics

1001 Craig Road, Suite 260
St. Louis, MO 63146
(314) 872-2182 Fax (314) 872-2169
E-Mail: marc-lampert@ins.memec.com
www.ikn.com

NEW JERSEY

Insight Electronics

2 Eves Drive, Suite 208
Marlton, NJ 08053
(609) 985-5556 Fax (609) 985-5895
E-Mail: marc-lampert@ins.memec.com
www.ikn.com

115 Rt. 46, Suite F-1000
Mountain Lakes, NJ 07046
(201) 316-6040 Fax (201) 335-1495
E-Mail: marc-lampert@ins.memec.com
www.ikn.com

Nu Horizons Electronics

18000 Horizon Way, Suite 200
Mt. Laurel, NJ 08054
(609) 231-0900 Fax (609) 231-9510
E-Mail: sales@nuhorizons.com
www.nuhorizons.com

Distributors — North America (continued)

Nu Horizons Electronics (continued)

39 US Route 46
Pine Brook, NJ 07058
(201) 882-8300 Fax (201) 882-8398
E-Mail: sales@nuhorizons.com
www.nuhorizons.com

NEW YORK

Insight Electronics

1373 Veterans Memorial Hwy.
Hauppauge, NY 11788
(516) 761-0960 Fax (516) 244-1570
E-Mail: marc-lampert@ins.memec.com
www.ikn.com

190 Linden Oaks Dr.
Rochester, NY 14625
(716)383-4271 Fax (716)383-4279
E-Mail: marc-lampert@ins.memec.com
WWW:www.ikn.com

Nu Horizons Electronics

70 Maxess Road
Melville, NY 11747
(516) 396-5000 Fax (516) 396-5050
E-Mail: sales@nuhorizons.com
www.nuhorizons.com

333 Metro Park
Rochester, NY 14625
(716) 292-0777 Fax (716) 292-0750
E-Mail: sales@nuhorizons.com
www.nuhorizons.com

NORTH CAROLINA

Insight Electronics

811 Spring Forest Rd. Suite 1000
Raleigh, NC 27609
(919) 873-9922 Fax (919) 873-9050
E-Mail: marc-lampert@ins.memec.com
www.ikn.com

Nu Horizons Electronics

2920 Highwood Blvd., Suite 125
Raleigh, NC 27604
(919) 954-0500 Fax (919) 954-0545
E-Mail: sales@nuhorizons.com
www.nuhorizons.com

OHIO

Insight Electronics

9700 Rockside Road, Suite 105
Valley View, OH 44125
(216) 520-4333 Fax (216) 520-4322
E-Mail: marc-lampert@ins.memec.com
www.ikn.com

4130 Linden Avenue, Suite 238
Dayton, OH 45432
(937) 253-7501 Fax (937) 253-7586
E-Mail: marc-lampert@ins.memec.com
www.ikn.com

Nu Horizons Electronics

2208 Enterprise E. Parkway
Twinsburg, OH 44087
(216) 963-9933 Fax (216) 963-9944
E-Mail: sales@nuhorizons.com
www.nuhorizons.com

OKLAHOMA

Insight Electronics

4150 S. 100th East Avenue, Suite 200G
Tulsa, OK 74146
(918) 655-4664 Fax (918) 665-4665
E-Mail: marc-lampert@ins.memec.com
www.ikn.com

OREGON

Insight Electronics

8705 SW Nimbus Avenue, Suite 200
Beaverton, OR 97008
(503) 644-3300 Fax (503) 641-4530

PENNSYLVANIA

Insight Electronics

365 N. Cottage Road, Suite D
Mercer, PA 16137
(412) 662-2707 Fax (412) 662-2708
E-Mail: marc-lampert@ins.memec.com
www.ikn.com

Nu Horizons Electronics

18000 Horizon Way, Suite 200
Mt. Laurel, NJ 08054
(215) 557-6450 Fax (609) 231-9510
E-Mail: sales@nuhorizons.com
www.nuhorizons.com

TEXAS

Insight Electronics

1778 Plano Road, Suite 210
Richardson, TX 75081
(972) 783-0800 Fax (972) 680-2402
E-Mail: marc-lampert@ins.memec.com
www.ikn.com

11500 Metric Boulevard, Suite 215
Austin, TX 78758
(512) 719-3090 Fax (512) 719-3091
E-Mail: marc-lampert@ins.memec.com
www.ikn.com

10777 Westheimer, Suite 1100
Houston, TX 77042
(713) 260-9614 Fax (512) 260-9602
E-Mail: marc-lampert@ins.memec.com
www.ikn.com

Nu Horizons

2081 Hutton Drive, Suite 119
Carrollton, TX 75006
(214) 488-2255 Fax (214) 488-2265
(800) 200-1586
E-Mail: sales@nuhorizons.com
www.nuhorizons.com

7801 North Lamar, Suite F-29
Austin, TX 78752
(512) 467-2292 Fax (512) 467-2466
E-Mail: sales@nuhorizons.com
www.nuhorizons.com

UTAH

Insight Electronics

4455 S. 700 E., Suite 301
Salt Lake City, UT 84107
(801) 288-9001 Fax (801) 288-9195
E-Mail: marc-lampert@ins.memec.com
www.ikn.com

VIRGINIA

Insight Electronics

6325 Woodside Ct., Suite 130
Columbia, MD 21046
(410) 381-3131 Fax (410) 381-3141
E-Mail: marc-lampert@ins.memec.com
www.ikn.com

Distributors — North America (continued)

WASHINGTON

Insight Electronics

12002 115th Avenue NE
Kirkland, WA 98034
(206) 820-8100 Fax (206) 821-2976
E-Mail: marc-lampert@ins.memec.com
www.ikn.com

WASHINGTON, DC

Nu-Horizons

8965 Guilford Road, Suite 160
Columbia, MD 21046
(301) 621-8244 Fax (401) 995-6332
E-Mail: sales@nuhorizons.com
www.nuhorizons.com

WISCONSIN

Insight Electronics

10855 W Potter Road, #14
Wauwatosa, WI 53226
(414) 258-5338 Fax (414) 258-5360
E-Mail: marc-lampert@ins.memec.com
www.ikn.com

TriQuint Semiconductor, Inc. — Area Sales Offices

Asia Pacific Sales Office

George Sanders
2300 NE Brookwood Parkway
Hillsboro, OR 97214
(503) 615-9115 Fax (503) 615-8901
E-Mail: george_sanders@tqs.com

Major Accounts

Mike Zyla
1637 Oakwood Drive, Suite S-419
Penn Valley, PA 19072
(610) 668-6781 Fax (610) 668-6782
E-Mail: mikez@tqs.com

Northwest Area Sales Office

George Herrmann
1999 S. Bascom Avenue, Suite 700
Campbell, CA 95008
(408) 879-2662 Fax (408) 879-2322
E-Mail: georgeh@tqs.com

European Sales Office

Graham Teague
Birkenweg 6
Bachmehring
D-83549 Eisinging
West Germany
++49 8071 93504
Fax ++49 8071 93505
E-Mail: 100446.2405@compuserve.com

Northeast Area Sales Office

Mark Lewis
International Trade Center
500 International Drive
Mount Olive, NJ 07828
(201) 426-8436 Fax (201) 426-8450
E-Mail: markl@tqs.com

Southwest Area Sales Office

Greg Peck
2250 East Imperial Highway, Suite 200
El Segundo, CA 90245
(310) 648-6681 Fax (310) 648-6687
E-Mail: gregp@tqs.com

Note: We try our best to keep this listing accurate and up to date, however phone numbers, addresses, and even company partnerships do change over time. If you should encounter any difficulties, please feel free to contact TriQuint at (503) 615-9000.



2300 N.E. Brookwood Parkway

Hillsboro, Oregon 97124

phone (503) 615-9000

fax (503) 615-8900

www.triquint.com