

TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT SILICON MONOLITHIC

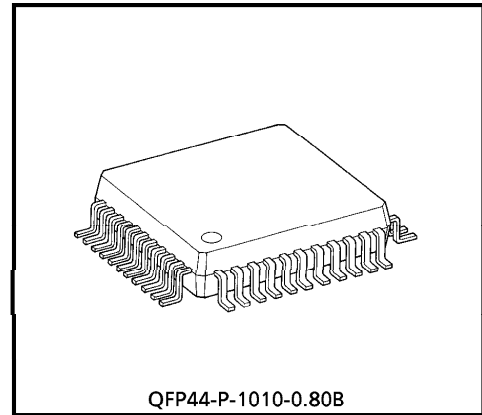
# TA8508AF

## R/W IC FOR FLOPPY DISK DRIVE

TA8508AF is a bipolar monolithic IC developed as a read/write IC for perpendicular floppy disk drives (PFD). TA8508AF consists of a floppy disk drive read circuit, a write circuit, and various control circuits, all integrated on a single chip to reduce disk drive size and power consumption.

### FEATURES

- Power save function which reduces power dissipation (to 9mW typ.) during non-operation (not reading, writing, or erasing).
- 5V single power supply (4.3V to 6.0V)
- Incorporates a diode switch for switching between read and write heads. The differential voltage gain of the read amp can be set to 200 times or 400 times using the gain select pin.
- The write current can be set to a maximum of 25mA<sub>DC</sub> using external resistance.
- A built-in write current switching circuit allows the current value to be switched between outer and inner tracks.
- Read, write, and erase circuits are incorporated in a single chip and can be controlled independently by  $\overline{WG}$  and  $\overline{EG}$  signals.
- A built-in power monitor circuit prevents writing in error at such times as when the power is turned on or abnormal voltage is applied.
- Incorporates a time constant capacitor for the time domain filter. Time constants can be set using an external resistor.
- Incorporates a time constant switching circuit for the time domain filter. Time constants can be switched between outer and inner tracks.
- Incorporates a differentiator constant switching circuit. The differentiator frequency characteristics can be switched.

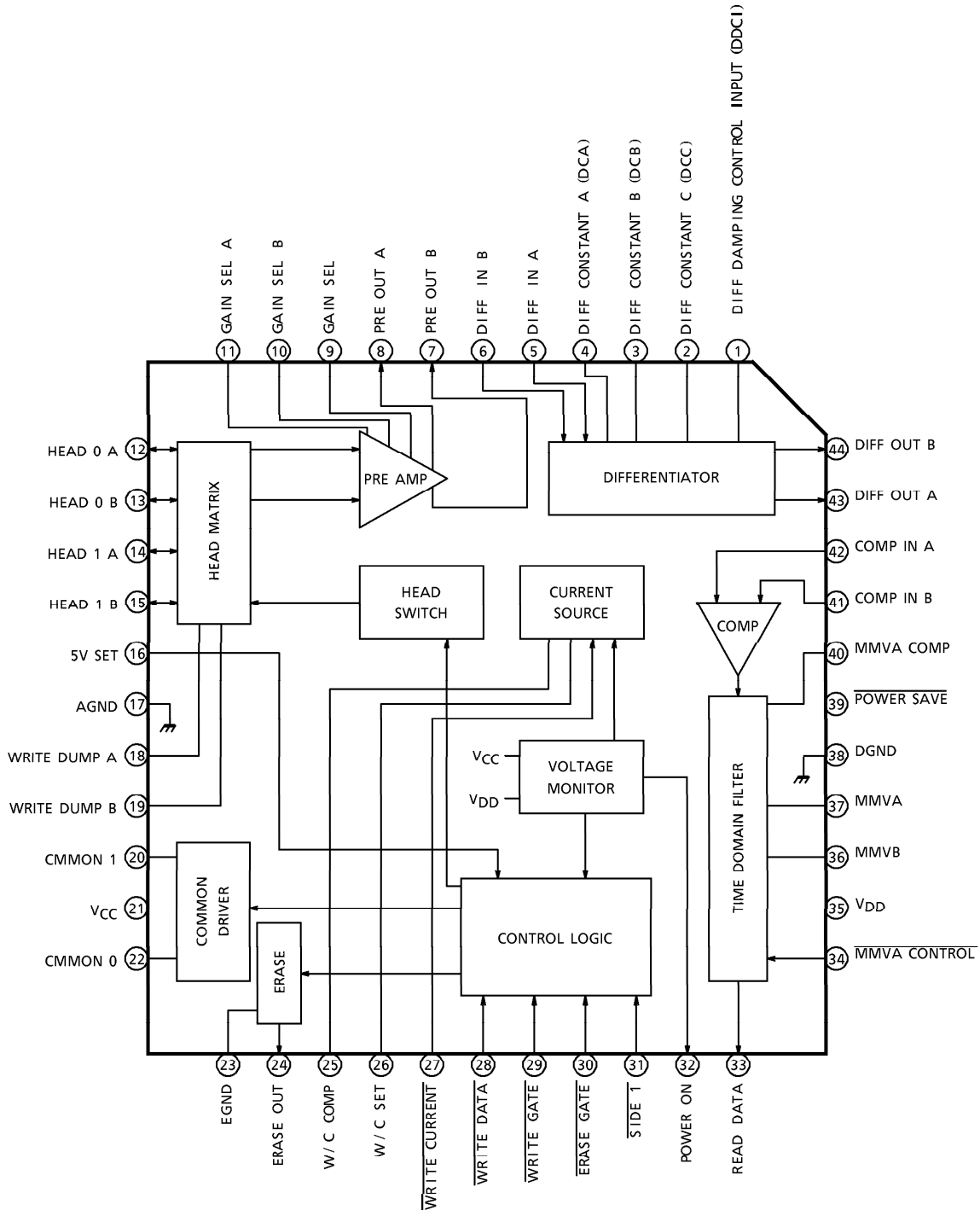


Weight: : 0.56g (Typ.)

961001EBA1

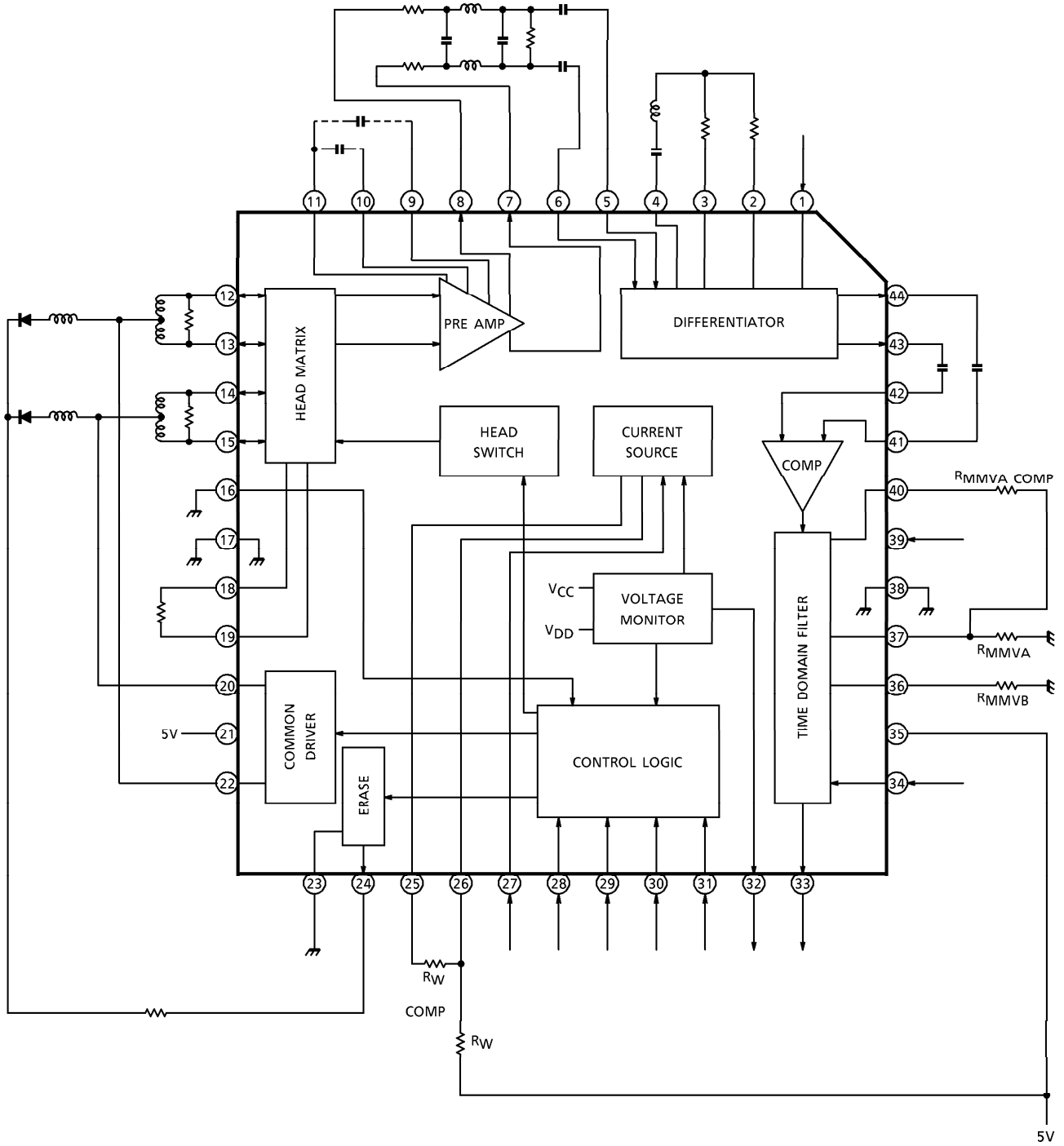
- TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.
- The products described in this document are subject to foreign exchange and foreign trade control laws.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
- The information contained herein is subject to change without notice.

PIN LAYOUT DIAGRAM/INTERNAL EQUIVALENT BLOCK DIAGRAM



Take care when using pins 9, 11, 12, 13, 14, and 15, as the allowable overvoltage surge margin is small (up to  $\pm 100V$ ).

EXTERNAL CONNECTION



## PIN FUNCTION

| PIN No. | PIN NAME                   | PIN FUNCTION   |
|---------|----------------------------|--|
| 1       | DIFF DUMPING CONTROL INPUT | Differentiator constant select pin<br>Inputting low logic voltage selects pins 3 (DCB) and 4 (DCA);<br>inputting high logic voltage selects pins 2 (DCC) and 4 (DCA).  |
| 2       | DIFF CONSTANT C            | Differentiator constant connecting pins<br>These pins connect the differentiator constants between pins 4 (DCA) and 2 (DCC), and between pins 4 (DCA) and 3 (DCB).   |
| 3       | DIFF CONSTANT B            |  |
| 4       | DIFF CONSTANT A            |  |
| 5       | DIFF IN A                  | Differentiator input pins.<br>These pins input a read signal from the pre-amp output pin to the differentiator via the filter circuit.   |
| 6       | DIFF IN B                  |  |
| 7       | PRE OUT B                  | Pre-amp output pins<br>These differential output pins output a read signal to the differentiator input pin via the filter circuit.   |
| 8       | PRE OUT A                  |  |
| 9       | GAIN SEL                   | Pre-amp gain select pins<br>AC coupling of pins 9 and 11 selects a 400-times pre-amp gain. AC coupling of pins 10 and 11 selects a 200-times pre-amp gain.   |
| 10      | GAIN SEL B                 |  |
| 11      | GAIN SEL A                 |  |
| 12      | HEAD 0 A                   | Magnetic head 0 input/output pins<br>These pins connect the write/read magnetic head with a center tap, and the damping resistor at a read.  |
| 13      | HEAD 0 B                   |  |
| 14      | HEAD 1 A                   | Magnetic head 1 input/output pins<br>Another pair of input/output pins like those above.   |
| 15      | HEAD 1 B                   |  |
| 16      | 5V SET                     | V <sub>CC</sub> power select input pin<br>Grounding this pin selects V <sub>CC</sub> = 5V mode.  |
| 17      | AGND                       | Analog GND connecting pin  |
| 18      | WRITE DUMP A               | Write dumping resistor connecting pins<br>The head dumping resistor is connected between these pins at a write.pin voltage at read and write.  |
| 19      | WRITE DUMP B               |  |
| 20      | COMMON 1                   | Head 1 common driver connecting pin<br>This pin connects to the center tap of magnetic head 1. It sets the head 1 pin voltage at read and write.   |
| 21      | V <sub>CC</sub>            | Analog power connecting pin  |
| 22      | COMMON 0                   | Head 0 common driver connecting pin<br>This pin connects to the center tap of magnetic head 0. It sets the head 0 pin voltage at read and write.   |
| 23      | EGND                       | Erase GND connecting pin   |
| 24      | ERASE OUTPUT               | Erase current sink pin<br>Open collector pin for the erase current sink.   |
| 25      | W/C COMP                   | Connecting pin for write current compensation resistor<br>Between this pin and pin 26, connect a write current compensation resistor R <sub>W COMP</sub> to set the write current increase (I <sub>WC</sub> ).<br><br>Equation $I_{WC} = \frac{1.3 - V_{WC}}{R_{W COMP} (\Omega)} \times 10 \text{ (ADC)}$ |
| 26      | W/C SET                    | Connecting pin for write current setting resistor<br>Between this pin and pin V <sub>DD</sub> 35, connect a write current setting resistor R <sub>W</sub> to set the write current value.<br><br>Equation $I_W = \frac{1.3}{R_W (\Omega)} \times 10 \text{ (ADC)}$   |

| PIN No. | PIN NAME                          | PIN FUNCTION   |
|---------|-----------------------------------|--|
| 27      | $\overline{\text{WRITE CURRENT}}$ | Write current control pin (digital input)<br>When low logic voltage is input, the write current is defined as the sum of $I_W$ and $I_{WC}$ . When high logic voltage is input, the write current is $I_{WY}$ only.  |
| 28      | $\overline{\text{WRITE DATA}}$    | Write data input pin (Schmitt digital input)<br>The write data input pin is triggered when digital input goes from high to low.  |
| 29      | $\overline{\text{WRITE GATE}}$    | Write gate signal input pin (digital input)<br>Inputting low logic voltage activates the write.  |
| 30      | $\overline{\text{ERASE GATE}}$    | Erase gate signal input pin (digital input)<br>Inputting low logic voltage activates the erase.  |
| 31      | $\overline{\text{SIDE 1}}$        | Head side switching signal input pin (digital input)<br>Inputting low logic voltage activates head 1; inputting high logic voltage activates head 0.   |
| 32      | POWER ON                          | Voltage drop detection output pin<br>This open collector pin outputs low while at least one/both of the $V_{DD}$ and $V_{CC}$ is/are below the specified value.  |
| 33      | READ DATA                         | Read data output pin<br>This pin outputs the read data (totem pole type).  |
| 34      | $\overline{\text{MMVA CONTROL}}$  | Time domain filter time constant switching signal input pin (digital input)<br>Inputting low logic voltage narrows the output width of the first monostable circuit.   |
| 35      | $V_{DD}$                          | Digital power connecting pin   |
| 36      | MMVB                              | Second monostable circuit R connecting pin for time domain filter<br>Connect the second monostable circuit time constant setting resistor $R_{MMVB}$ . The following equation determines the second monostable circuit's pulse width $t_2$ .<br>$t_2 = 27 \times (R_{MMVB} (\text{k}\Omega) + 0.1) (\text{ns})$  |
| 37      | MMVA                              | First monostable circuit R connecting pin for time domain filter.<br>Connect the first monostable circuit time constant setting resistor $R_{MMVA}$ . The following equation determines the first monostable circuit's pulse width $t_1$ .<br>$t_1 = 53.5 \times (R_A (\text{k}\Omega) + 0.1) (\text{ns})$<br>Note: When MMVA CONTROL logic input voltage is high, $R_A = R_{MMVA}$ . When MMVA CONTROL logic input voltage is high, $R_A = R_{MMVA} // R_{MMVA \text{ COMP}}$ . |
| 38      | DGND                              | Digital GND connecting pin   |
| 39      | $\overline{\text{POWER SAVE}}$    | Power save mode select signal input pin (digital input)<br>Inputting low logic voltage selects power save mode, which reduces R/W $I_C$ power dissipation. During power save mode, read, write, and erase operations are disabled.<br>(The power monitor circuit still functions.)   |
| 40      | MMVA COMP                         | Resistor connecting pin for time domain filter time constant switching. This open collector pin connects resistor $R_{MMVA \text{ COMP}}$ between this and pin 37 to compensate the output width of the time domain filter's first monostable circuit.   |
| 41      | COMP IN B                         | Comparator input pins  |
| 42      | COMP IN A                         | A read signal is input to these two pins from the differentiator output pins via the AC coupling capacitors.   |
| 43      | DIFF OUT A                        | Differentiator output pins   |
| 44      | DIFF OUT B                        | These two pins output a read signal to the comparator input pin via the AC coupling capacitors.  |

## MAXIMUM RATINGS (Ta = 25°C)

| CHARACTERISTICS  | SYMBOL           | RATING   | UNIT             |
|--|------------------|----------|------------------|
| Power Supply Voltage                                     | V <sub>CC</sub>  | 7        | V                |
| Supply Voltage   | V <sub>DD</sub>  | 7        | V                |
| Digital Signal Input Voltage<br>(Note 1)                 | —                | -0.5~5.5 | V                |
| Voltage Applied to Power On<br>Pin<br>(Note 2)           | —                | 7        | V                |
| Voltage Applied to Erase<br>Output Pin<br>(Note 3)       | —                | 7        | V                |
| Voltage Applied to Head 0 / 1<br>A / B Pins<br>(Note 4)  | —                | 7        | mA               |
| Common Drive Source<br>Current                           | I <sub>COM</sub> | 75       | mA               |
| Erase Drive Sink Current                                 | I <sub>E</sub>   | 50       | mA               |
| Write Drive Current<br>(Note 2)                          | I <sub>W</sub>   | 25       | mA <sub>DC</sub> |
| Sink Current on Power On<br>Pin                          | —                | 7        | mA               |
| Ambient Operating<br>Temperature                         | T <sub>a</sub>   | -20~75   | °C               |
| Junction Operating<br>Temperature                        | T <sub>j</sub>   | 150      | °C               |
| Storage Temperature                                      | T <sub>stg</sub> | -55~150  | °C               |
| Power Dissipation<br>(Ta = 25°C for IC only)<br>(Note 5) | P <sub>D</sub>   | 0.75     | W                |

(Note1) The WRITE CURRENT, WRITE DATA, WRITE GATE, ERASE GATE, SIDE1, MMVA CONTROL, POWER SAVE, DDCI signals are input to the 5V SET pin.

(Note2) Applies to POWER ON pin (pin 32).

(Note3) Applies to ERASE OUTPUT pin (pin 24).

(Note4) Applies to HEAD 0 A, HEAD 0 B, HEAD 1 A, and HEAD 1 B pins (pins 12, 13, 14, and 15).

(Note5) For device usage conditions, see Figure 1 Power Dissipation (P<sub>D</sub>)-Ambient Temperature (T<sub>a</sub>).

## RECOMMENDED OPERATING CONDITIONS

| CHARACTERISTICS                                  | CONDITIONS | UNIT |
|--|------------|------|
| V <sub>CC</sub> , V <sub>DD</sub> supply voltage | 4.3~6.0    | V    |
| Operating ambient<br>temperature                 | 0~60       | °C   |

## ELECTRICAL CHARACTERISTICS

(1) CURRENT DISSIPATION ( $T_a = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{V}$ ,  $V_{DD} = 5\text{V}$ )

| CHARACTERISTICS  |                              | SYMBOL      | TEST CIR-CUIT | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|------------------|------------------------------|-------------|---------------|-----------------|------|------|------|------|
| In Read          | $V_{DD}$ Current Dissipation | $I_{DDR}$   | 1             | —               | —    | 17.7 | 23.4 | mA   |
|                  | $V_{CC}$ Current Dissipation | $I_{CCR}$   | 1             | —               | —    | 7.5  | 8.6  | mA   |
| In Write         | $V_{DD}$ Current Dissipation | $I_{DDW}$   | 1             | (Note 1)        | —    | 9.5  | 15.4 | mA   |
|                  | $V_{CC}$ Current Dissipation | $I_{CCW}$   | 1             | —               | —    | 12.3 | 18.8 | mA   |
| In Erase         | $V_{DD}$ Current Dissipation | $I_{DDE}$   | 1             | —               | —    | 9.4  | 13.9 | mA   |
|                  | $V_{CC}$ Current Dissipation | $I_{CCE}$   | 1             | —               | —    | 12.6 | 19.2 | mA   |
| In write + Erase | $V_{DD}$ Current Dissipation | $I_{DDW+E}$ | 1             | (Note 1)        | —    | 12.3 | 19.4 | mA   |
|                  | $V_{CC}$ Current Dissipation | $I_{CCW+E}$ | 1             | —               | —    | 12.3 | 18.8 | mA   |
| In Power Save    | $V_{DD}$ Current Dissipation | $I_{DDPS}$  | 1             | —               | —    | 1.35 | 2.7  | mA   |
|                  | $V_{CC}$ Current Dissipation | $I_{CCPS}$  | 1             | —               | —    | 0.27 | 0.4  | mA   |
|                  | Total Power Dissipation      | $P_{DPS}$   | 1             | —               | —    | 8.1  | 15.5 | mW   |

(Note 1) When Write Current  $I_W = 0$ (2) POWER MONITOR ( $T_a = 25^\circ\text{C}$ ,  $V_{CC} = 0\sim 7\text{V}$ ,  $V_{DD} = 0\sim 7\text{V}$ )

| CHARACTERISTICS  |                    | SYMBOL          | TEST CIR-CUIT | TEST CONDITIONS                                   | MIN. | TYP. | MAX. | UNIT          |
|--|--------------------|-----------------|---------------|---|------|------|------|---------------|
| $V_{DD}$ , $V_{CC}$ Threshold Voltage                      | Positive Direction | $V_T^+$         | —             | —   | —    | 4.0  | 4.2  | V             |
|  | Negative Direction | $V_T^-$         | —             |   | 3.6  | 4.0  | —    |               |
| Threshold Voltage Width                                    |                    | $V_T^+ - V_T^-$ | —             | —   | —    | 150  | —    | mV            |
| Saturation Voltage When Power On Pin (Pin 32) Detection On |                    | —               | —             | $V_{DD} = 3.6\text{V}$<br>$I_{SINK} = 5\text{mA}$ | —    | —    | 0.4  | V             |
| Leakage Current When Power On Pin (Pin 32) Detection Off   |                    | —               | —             | $V_{DD} > 4.5\text{V}$                            | —    | —    | 10   | $\mu\text{A}$ |

## (3) PRE-AMP, DIFFERENTIATOR, COMPARATOR (Ta = 25°C, VCC = 5V, VDD = 5V)

| CHARACTERISTICS       |  | SYMBOL             | TEST CIR-CUIT | TEST CONDITIONS                                      | MIN. | TYP. | MAX. | UNIT              |
|-----------------------|--|--------------------|---------------|--|------|------|------|-------------------|
| Head Switcher/Pre-amp | Differential Voltage Gain                    | GV1                | 2             | Test Frequency f = 1MHz                              | 340  | 375  | 415  | V/V               |
|                       |  | GV2                | 2             | Test Frequency f = 1MHz                              | 170  | 185  | 200  |                   |
|                       | Gain Attenuation Bandwidth (-3dB)            | FC                 | 2             | —  | 8    | 12   | —    | MHz               |
|                       | COMMON MODE Rejection Ratio                  | CMRR               | —             | Input Sine Wave<br>f = 1MHz 200mV <sub>rms</sub>     | 50   | —    | —    | dB                |
|                       | Power Supply Rejection Ratio                 | RSRR               | —             | Multiplexed sine wave<br>f = 10kHz 1V <sub>p-p</sub> | 70   | —    | —    | dB                |
|                       | Differential Input Resistance                | R <sub>IN</sub>    | —             | f = 62.5~625kHz                                      | 6.0  | 9.0  | 16.0 | kΩ                |
|                       | Differential Input Capacitance               | C <sub>IN</sub>    | —             | f = 250kHz   | —    | 24   | —    | pF                |
| Pre-Amp               | Differential Input Voltage Amplitude         | V <sub>IN</sub>    | —             | At x 200 Gain  | 0.8  | —    | 7.5  | mV <sub>p-p</sub> |
|                       | Differential Output Voltage Amplitude        | V <sub>OUT</sub>   | 2             | —  | 2.0  | 3.0  | —    | V <sub>p-p</sub>  |
|                       | Differential Output Current Amplitude        | I <sub>OUT</sub>   | —             | —  | 3.0  | 4.0  | 5.0  | mA <sub>p-p</sub> |
|                       | Differential Output Offset Voltage           | V <sub>OFS</sub>   | —             | —  | —    | —    | 0.5  | V                 |
|                       | Input Equivalent Noise Voltage               | E <sub>N</sub>     | 2             | Head Connected<br>f = 400Hz to 1MHz                  | —    | 4.0  | 6.0  | μV <sub>rms</sub> |
| Differentiator        | Gain Attenuation Bandwidth (-3dB)            | F <sub>CD</sub>    | —             | —  | 20   | —    | —    | MHz               |
|                       | Differential Output Voltage Amplitude        | V <sub>OUTD</sub>  | —             | —  | —    | 2    | —    | V <sub>p-p</sub>  |
|                       | Differential Output Offset Voltage           | V <sub>OFD</sub>   | —             | —  | —    | 20   | —    | mV                |
|                       | Differential Input Resistance                | R <sub>IND</sub>   | —             | —  | 16   | 24   | —    | kΩ                |
|                       | Differential Output Resistance               | R <sub>OUTD</sub>  | —             | —  | —    | 200  | —    | Ω                 |
|                       | Sink Current (Pins 2, 3, 4)                  | I <sub>SINKD</sub> | —             | —  | 1.4  | 2.0  | —    | mA                |
| Comparator            | Maximum Differential Input Voltage Amplitude | V <sub>INC</sub>   | —             | —  | —    | 2    | —    | V <sub>p-p</sub>  |
|                       | Differential Input Resistance                | R <sub>INC</sub>   | —             | —  | 20   | 32   | —    | kΩ                |



(4) TIME DOMAIN/WAVEFORM SHAPING BLOCK (Ta = 25°C, VCC = 5V, VDD = 5V)

| CHARACTERISTICS  |                     | SYMBOL             | TEST CIR-CUIT | TEST CONDITIONS  | MIN. | TYP. | MAX. | UNIT |
|--|---------------------|--------------------|---------------|--|------|------|------|------|
| First Monostable Output Pulse Width                        |                     | t <sub>1</sub>     | 3             | —  | 200  | —    | 3000 | ns   |
| Second Monostable Output Pulse Width                       |                     | t <sub>2</sub>     | 3             | —  | 100  | —    | 1200 | ns   |
| Saturation Voltage On MMVA COMP Pin                        |                     | V <sub>MMC</sub>   | —             | I <sub>SINK</sub> = 10 $\mu$ A                                       | —    | —    | 50   | mV   |
| First Monostable Output Pulse Width Precision              |                     | E <sub>TM1</sub>   | 3             | —  | - 18 | —    | 18   | %    |
| Second Monostable Output Pulse Width Precision             |                     | E <sub>TM2</sub>   | 3             | —  | - 20 | —    | 20   | %    |
| First Monostable Output Pulse Width Compensation Precision |                     | E <sub>TM1C</sub>  | 3             | —  | - 15 | —    | 15   | %    |
| Peak Shift   |                     | PS                 | 3             | COMP Input<br>f = 62.5 to 500kHz<br>Differential<br>Input = 200mVp-p | —    | —    | 1    | %    |
| Read Output  | Low Output Voltage  | V <sub>L</sub> OUT | —             | I <sub>OL</sub> = 2mA  | —    | —    | 0.5  | V    |
|  | High Output Voltage | V <sub>H</sub> OUT | —             | I <sub>OH</sub> = - 10 $\mu$ A                                       | 3.5  | —    | —    | V    |
|  |                     |                    |               | I <sub>OH</sub> = - 0.4mA  | 2.8  | —    | —    |      |
|  | Sink Current        | I <sub>SI</sub> RD | —             | V <sub>OUT</sub> = 0.8V  | 2    | 4    | —    | mA   |
|  | Source Current      | I <sub>SO</sub> RD | —             | V <sub>OUT</sub> = 2.8V  | 0.4  | 1    | —    | mA   |
|  | Rising Time         | t <sub>r</sub>     | 3             | At Read Output = 0.5 to 2.2V With Load<br>Capacitance Of 20pF        | —    | —    | 25   | ns   |
| Falling Time   | t <sub>f</sub>      | —                  |               |  | —    | 25   | ns   |      |


(5) WRITE SYSTEM/ERASE SYSTEM (Ta = 25°C, VCC = 5V, VDD = 5V)

| CHARACTERISTICS                                   |  | SYMBOL             | TEST CIR-CUIT | TEST CONDITIONS                     | MIN.                              | TYP. | MAX. | UNIT             |                  |
|---|--|--------------------|---------------|-------------------------------------|-----------------------------------|------|------|------------------|------------------|
| Common Driver                                     | Output voltage in write selected                     | VWCMH              | —             | I <sub>W</sub> = 25mA <sub>DC</sub> | 4.4                               | —    | —    | V                |                  |
|   | Output voltage in write not-selected                 | VWCML              | —             | —                                   | —                                 | —    | 0.2  | V                |                  |
|   | Output voltage in read selected                      | VRCMH              | —             | —                                   | 2.3                               | 2.6  | 2.9  | V                |                  |
|   | Output voltage in read not-selected                  | VRCML              | —             | —                                   | —                                 | —    | 0.2  | V                |                  |
|   | Output current range                                 | I <sub>COM</sub>   | —             | —                                   | —                                 | —    | 75   | mA               |                  |
| Erase Driver                                      | ERASE OUTPUT pin output saturation voltage           | V <sub>ER</sub>    | —             | I <sub>Erase</sub> = 50mA           | —                                 | 0.2  | 0.5  | V                |                  |
|   | ERASE OUTPUT pin leakage current                     | I <sub>LKER</sub>  | —             | —                                   | —                                 | —    | 15   | μA               |                  |
|   | Erase current range                                  | I <sub>ERASE</sub> | —             | —                                   | —                                 | —    | 50   | mA               |                  |
| Write Driver                                      | Write current setting precision                      | E <sub>W</sub>     | —             | —                                   | - 8                               | —    | 8    | %                |                  |
|   |  | E <sub>WC</sub>    |               |                                     | - 10                              | —    | 10   |                  |                  |
|   | Write current output imbalance                       | D <sub>W</sub>     | —             | —                                   | —                                 | —    | 1    | %                |                  |
|   | Write current variable range (one side)              | I <sub>W</sub>     | —             | —                                   | V <sub>DD</sub> = 5.0V, Ta = 25°C | —    | —    | 20               | mA <sub>DC</sub> |
|   |  |                    |               |                                     |                                   | —    | —    | 28               |                  |
|   | Write current compensation variable range (one side) | I <sub>WC</sub>    | —             | —                                   | —                                 | —    | 5    | mA <sub>DC</sub> |                  |
| W/C COMP pin saturation voltage                   | V <sub>WC</sub>                                      | —                  | —             | I <sub>source</sub> = 0.5mA         | —                                 | 50   | 300  | mV               |                  |
| (Pins 12-13-14-15) in Write HEAD 0 / 1 A / B Pins | Leakage Current                                      | I <sub>LKW</sub>   | —             | —                                   | —                                 | —    | 10   | μA               |                  |
|   | Saturation voltage                                   | V <sub>SAT</sub>   | —             | —                                   | —                                 | 2    | —    | V                |                  |
|   | Differential output capacitance                      | C <sub>OUT</sub>   | —             | —                                   | —                                 | 23   | —    | pF               |                  |
|   | Differential output resistance                       | R <sub>OUT</sub>   | —             | —                                   | f = 1MHz                          | —    | 280  | —                | kΩ               |

## (6) LOGIC INPUT/OUTPUT BLOCK (Ta = 25°C, VCC = 5V, VDD = 5V)

| CHARACTERISTICS                   |  | SYMBOL                       | TEST CIR-CUIT | TEST CONDITIONS                        | MIN.         | TYP. | MAX. | UNIT    |         |
|-----------------------------------|--|------------------------------|---------------|--|--------------|------|------|---------|---------|
| Digital Signal Input              | Low Logic Input Voltage                            | $V_{LIN}$                    | —             | —                                      | —            | —    | 0.8  | V       |         |
|                                   | High Logic Input Voltage                           | $V_{HIN}$                    | —             | —                                      | 2.0          | —    | —    | V       |         |
|                                   | Low Logic Input Current                            | $\overline{PS}$ Pin (Pin 39) | $I_{LIN}$     | —                                      | 0.4V Applied | —    | —    | 50      | $\mu A$ |
|                                   |  | Others                       |               | —                                      | 0.4V Applied | —    | —    | 250     |         |
|                                   | High Logic Input Current (Pins 28, 29, 30, 31)     |                              | $I_{HIN1}$    | —                                      | 2.4V Applied | —    | —    | 10      | $\mu A$ |
|                                   | High Logic Input Current (Pin 27)                  |                              | $I_{HIN2}$    | —                                      | 2.4V Applied | —    | —    | 130     | $\mu A$ |
| High Logic Input Current (Pin 34) |  | $I_{HIN3}$                   | —             | 2.4V Applied                           | —            | —    | 80   | $\mu A$ |         |
| Schmitt Digital Signal Input      | Negative Direction Threshold Voltage (Input H → L) | $V_{LINS}$                   | —             | —                                      | 0.8          | 1.0  | —    | V       |         |
|                                   | Positive Direction Threshold Voltage (Input L → H) | $V_{HINS}$                   | —             | —                                      | —            | 1.6  | 2.0  | V       |         |
|                                   | Hysteresis Voltage Width                           | $V_{HINS} - V_{LINS}$        | —             | —                                      | 0.3          | 0.6  | —    | V       |         |
| Write Data                        | Write Data Maximum Input Frequency                 | $f_{IND}$                    | —             | $V_{IN} = 0.8 \sim 2.2V$<br>(50% Duty) | —            | —    | 12   | MHz     |         |

(7) SWITCHING CHARACTERISTICS (Ta = 25°C, VCC = 5V, VDD = 5V)

| CHARACTERISTICS  | SYMBOL | TEST CIR-CUIT | TEST CONDITIONS   | MIN. | TYP. | MAX. | UNIT |
|--|--------|---------------|---|------|------|------|------|
| Recovery Time From Power Save to Read Mode                                     | —      | —             | $\overline{PS}$ off→DIFF Output 90 to 110% (Note 1)   | —    | 1    | 2    | ms   |
| Head Switching Time  | —      | —             | $\overline{SIDE1}$ 50%→Selected VCOM 90%, Head Pin and Common Pin Connected                         | —    | —    | 4    | μs   |
| Read to write mode   | —      | —             | $\overline{WG}$ Off→Selected VCOM 90%   | —    | —    | 1    | μs   |
| WD-lw Delay  | —      | —             | $\overline{WD}$ 50%→ $I_{lW}$ 50%   | —    | —    | 0.3  | μs   |
| Write Current Rise Time  | —      | —             | $L_h = 0mH$   | —    | —    | 0.1  | μs   |
| Recovery Time From Erase Mode to Read Mode                                     | —      | —             | $\overline{EG}$ Off→DIFF Output 90 to 110%  | —    | —    | 20   | μs   |
| Read Recovery Time   | —      | —             | $\overline{WG}$ , $\overline{EG}$ Off→DIFF Output 90%   | —    | 30   | 40   | μs   |
| Sink Current Rise and Fall Time When Power Monitor Detection Turned Off or Off | —      | —             | Load (Pin 32)<br> | —    | —    | 100  | ms   |

Note 1 : When returning from power save to read mode, raise  $\overline{WG}$  and  $\overline{EG}$  to high level 10μs before  $\overline{PS}$  goes from low to high.

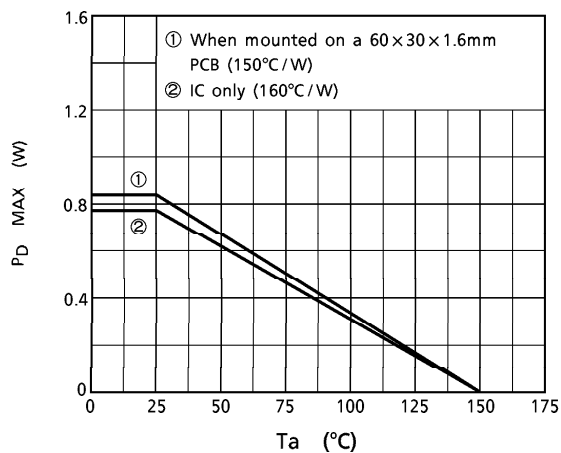
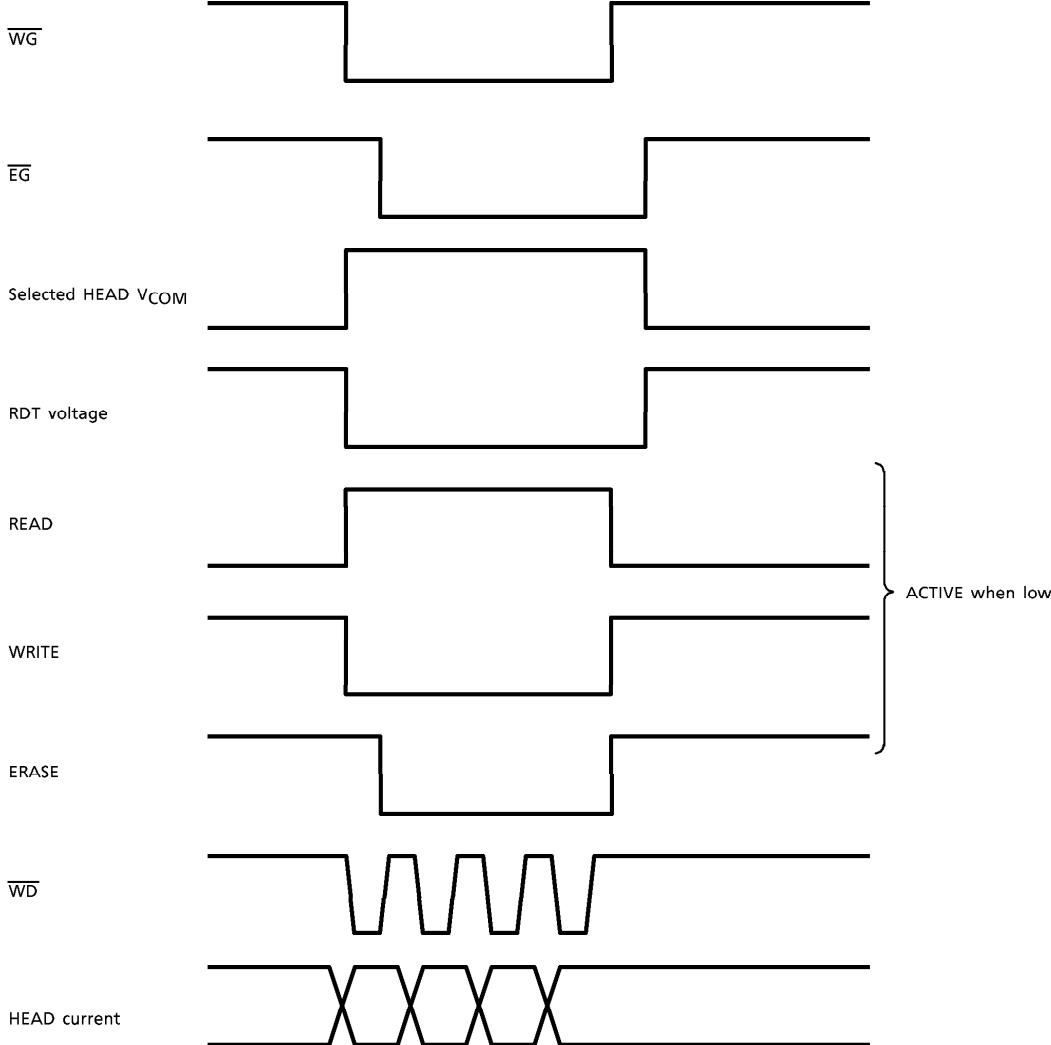


Fig.1 Power dissipation (PD) - Ambient Temperature (Ta)

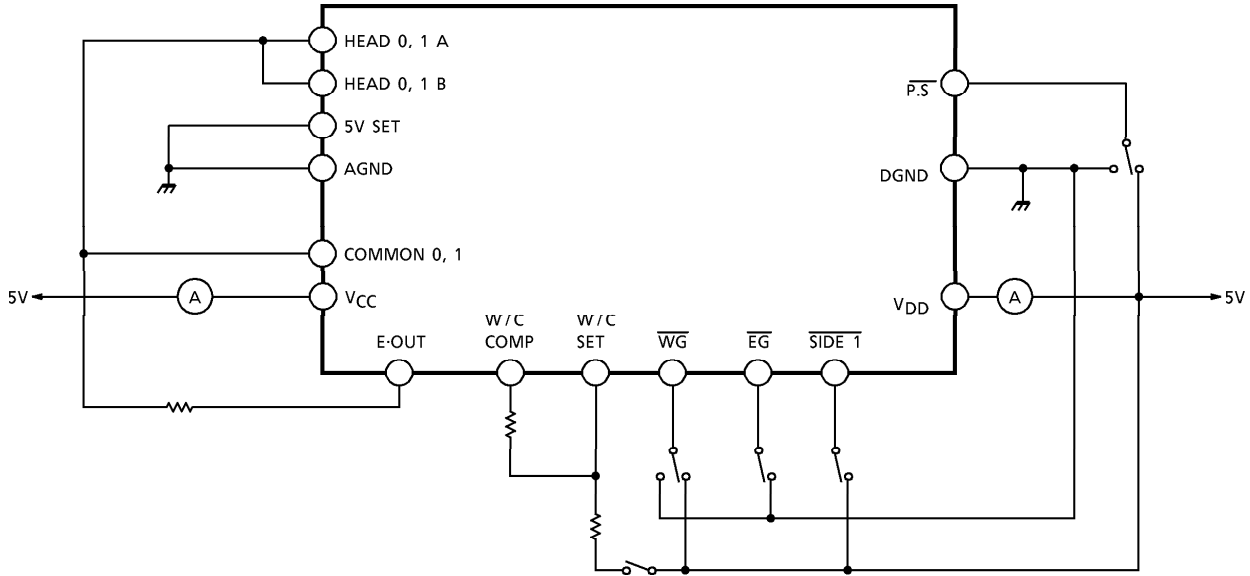
The TA8508AF maximum operating ambient temperature (Ta) is 75°C. However, refer to the above graph when using, as the package's power dissipation (PD) varies according to the ambient temperature.

TIMING CHART

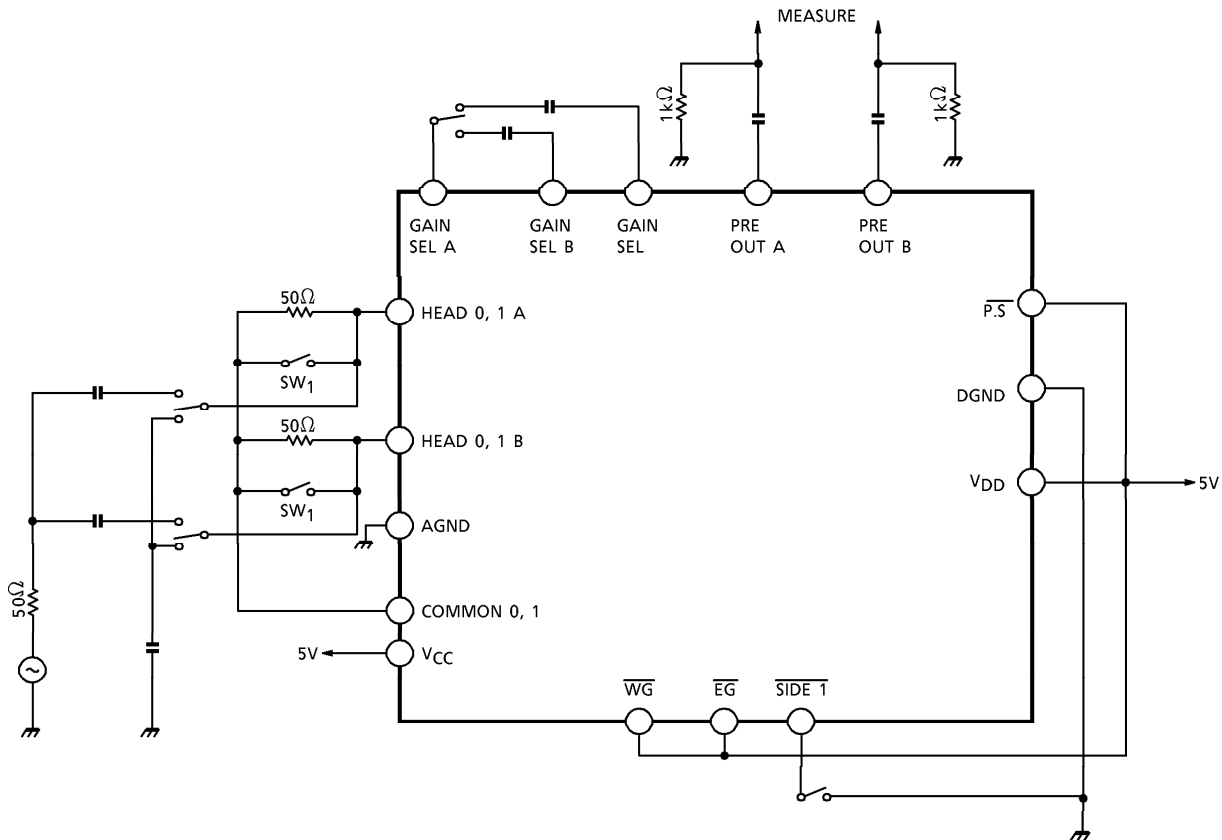


TEST CIRCUIT

1.  $I_{CC}$ ,  $I_{DD}$



2.  $G_V$ ,  $F_C$ ,  $V_{OUT}$ ,  $E_N$



Note1 : When  $G_V$ ,  $F_C$ , or  $V_{OUT}$  is measured, the signal is input to either of the HEAD 0, 1 A pins or HEAD 0, 1 B pins, whichever pair is selected.

Note2 : Turn  $SW_1$  off only when measuring  $E_N$ .

3.  $t_1$ ,  $t_2$ , ETM1, ETM2, ETM1C, PS,  $t_r$ ,  $t_f$

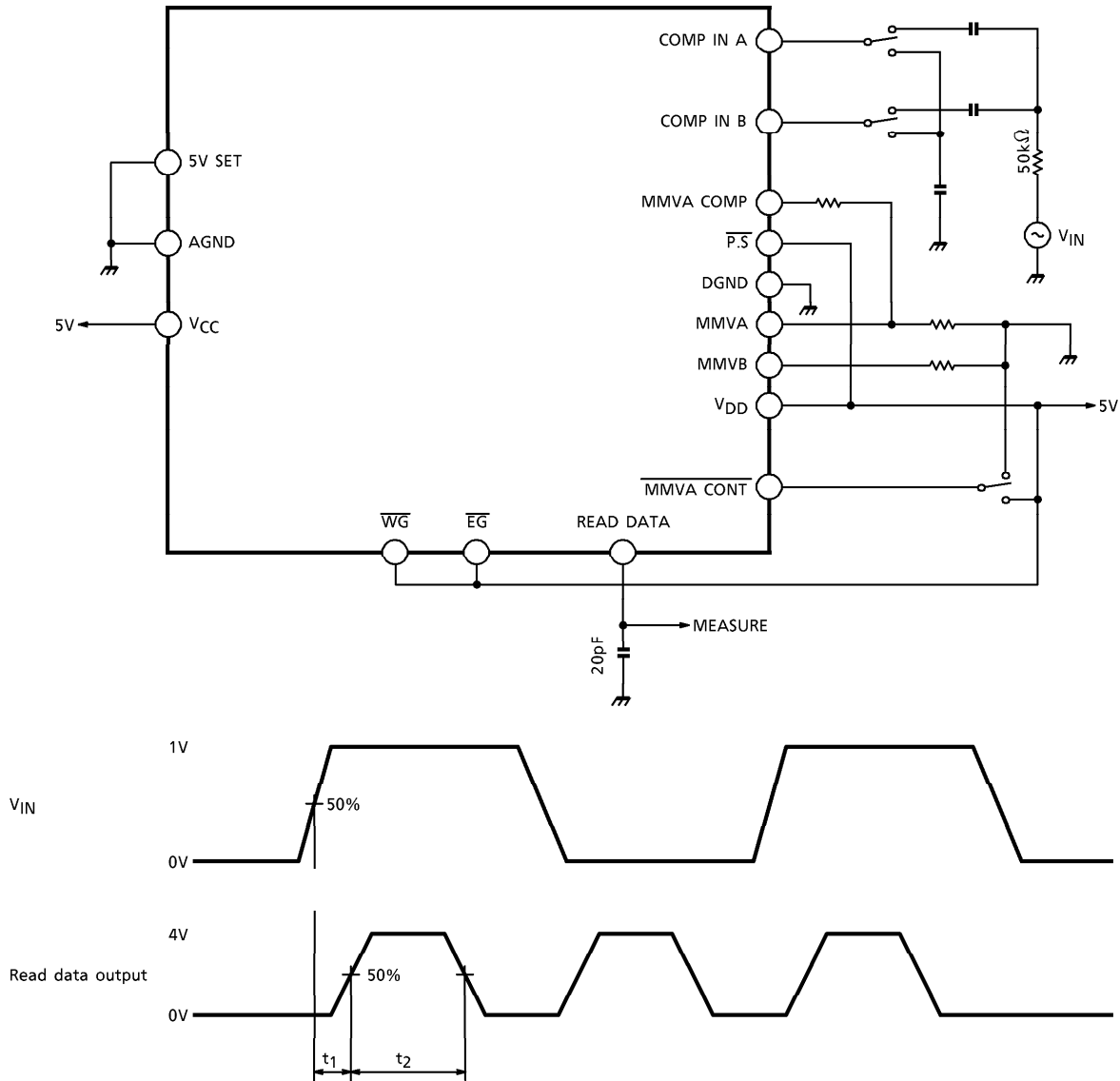


Figure 3-1  $t_1$ ,  $t_2$

(1) First and second monostable output pulse precision

Connect  $R_{MMVA}$  to set  $t_1$  to  $1\mu s$  and connect  $R_{MMVB}$  to set  $t_2$  to  $0.5\mu s$ . Observe  $t_1$  and  $t_2$  in the read data output.

ETM1 and ETM2 are defined as:

$$ETM1 = (1 - t_1 / 1) \times 100 (\%)$$

$$ETM2 = (1 - t_2 / 0.5) \times 100 (\%) \quad (t_1 (\mu s), t_2 (\mu s))$$

(2) First monostable output pulse width compensation precision

Connect R<sub>MMVA</sub>, R<sub>MMVA COMP</sub> so that t<sub>1</sub> to t'<sub>1</sub> (the difference between t<sub>1</sub> prior to pulse width compensation and t'<sub>1</sub> after pulse width compensation) is 1 μs.

Observe t'<sub>1</sub> and t<sub>1</sub> when 0.8V and 2.0V are applied to MMVA CONTROL.

EMT1C is defined as:

$$EMT1C = ( 1 - (t_1 - t'_1) / t_1 ) \times 100 (\%) (t_1 (\mu s), t'_1 (\mu s))$$

(3) Peak shift

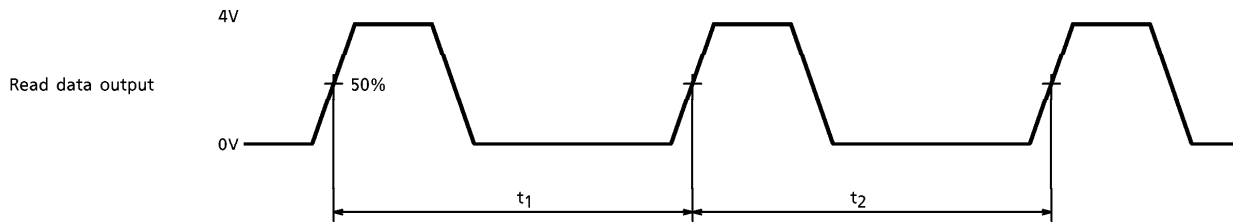


Figure3.2 P.S.

$$PS = \frac{1}{2} \times \left| \frac{t_1 - t_2}{t_1 + t_2} \right| \times 100 (\%)$$

(4) Read data output rise and fall times

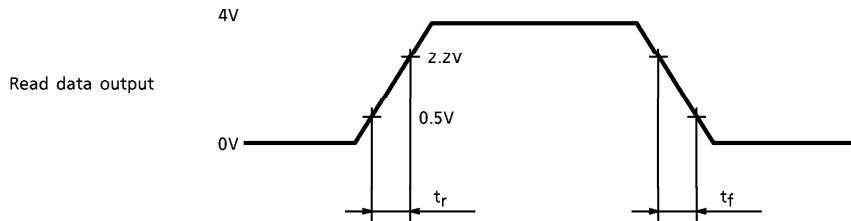
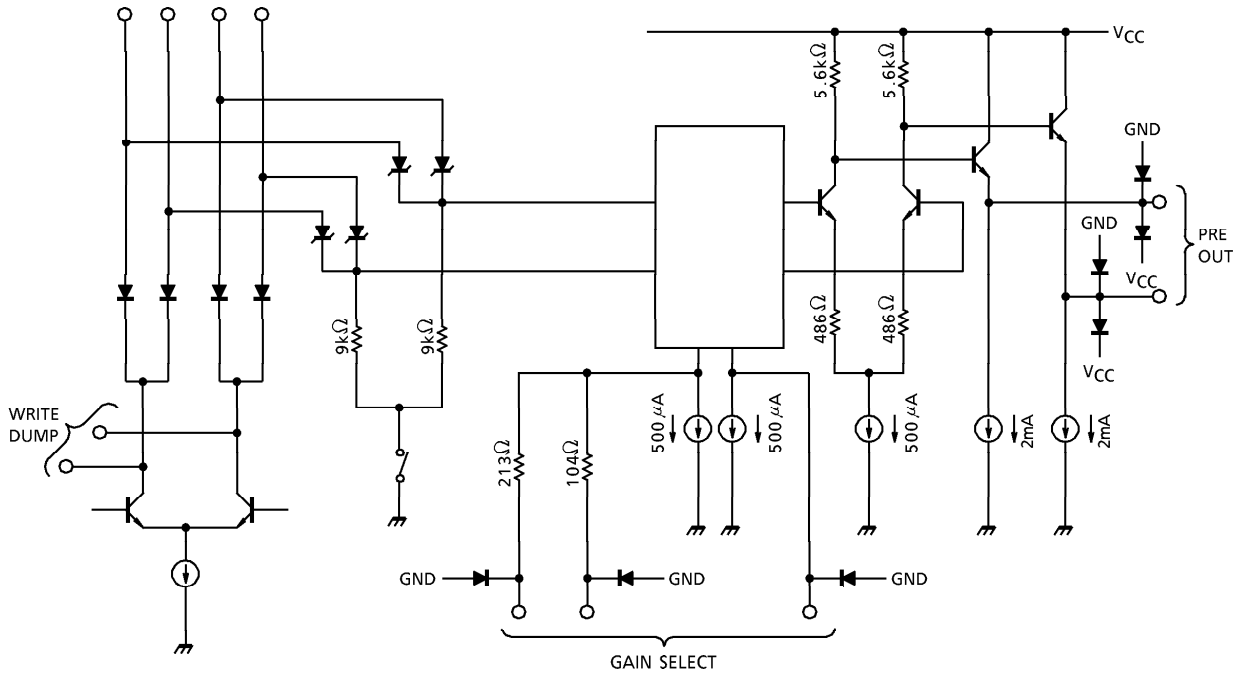


Figure3.3 tr and tf

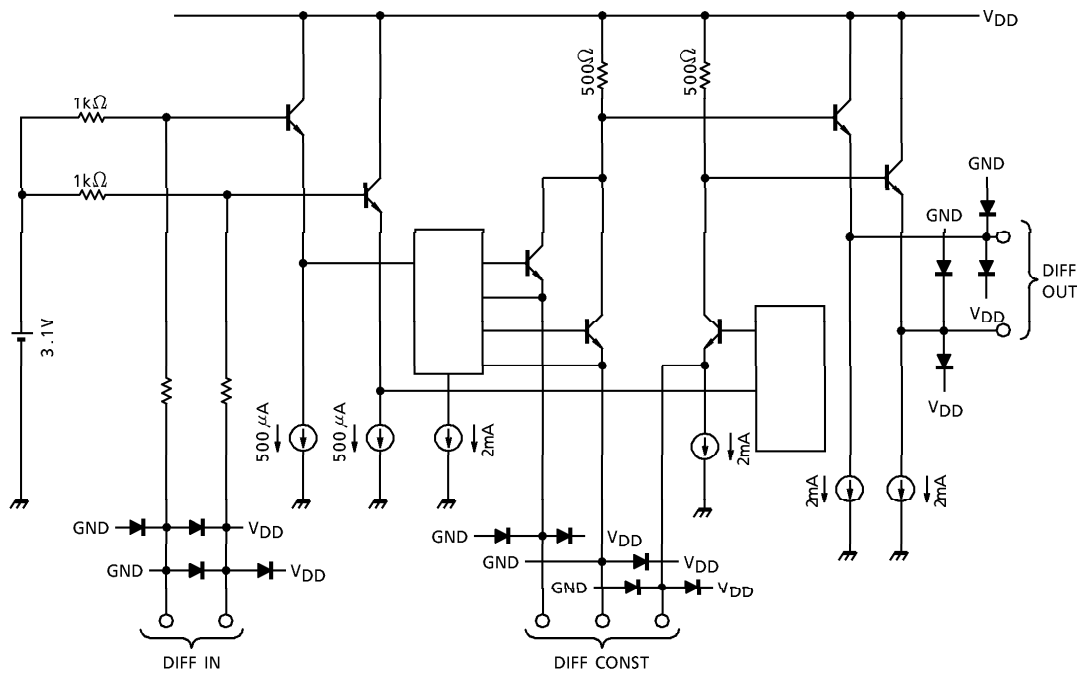


INTERNAL EQUIVALENT CIRCUITS

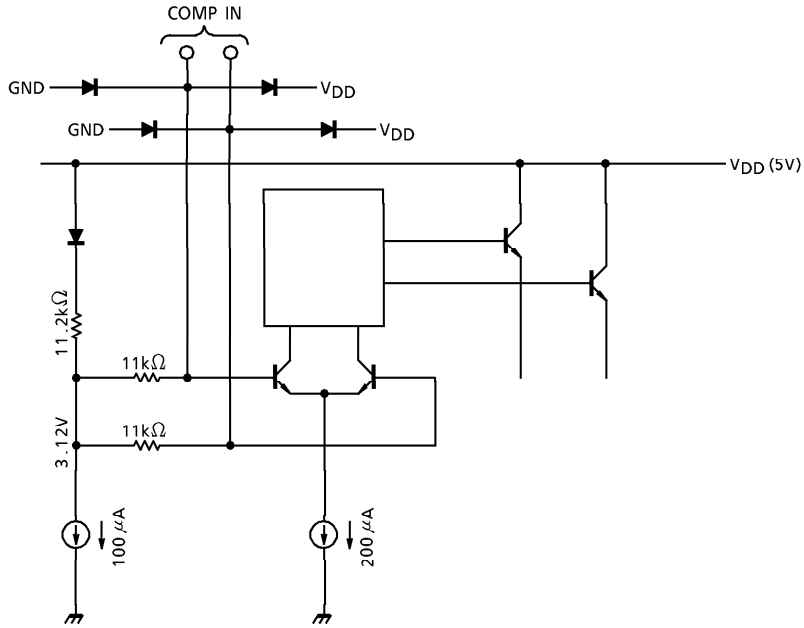
1. Pre-amp



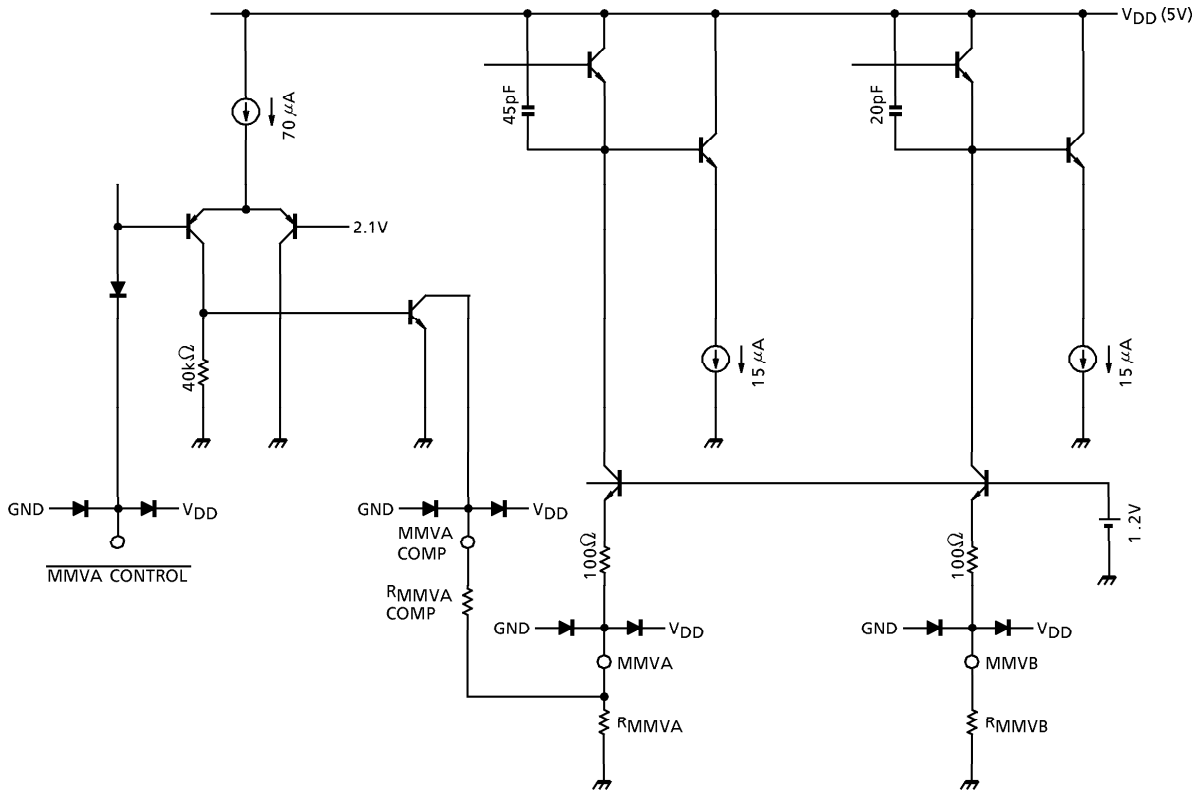
2. Differentiator



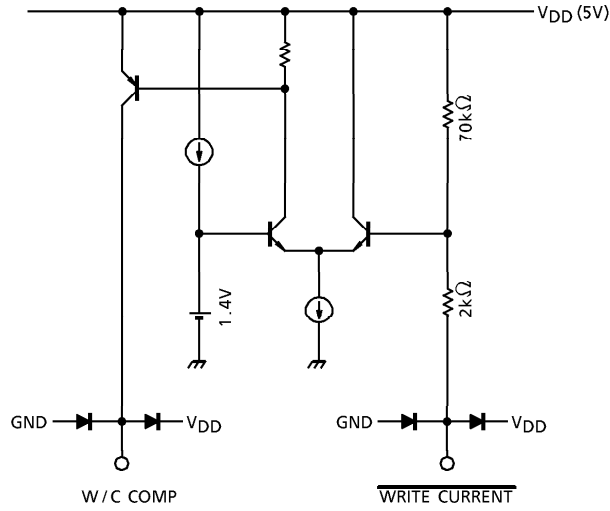
3. Comparator



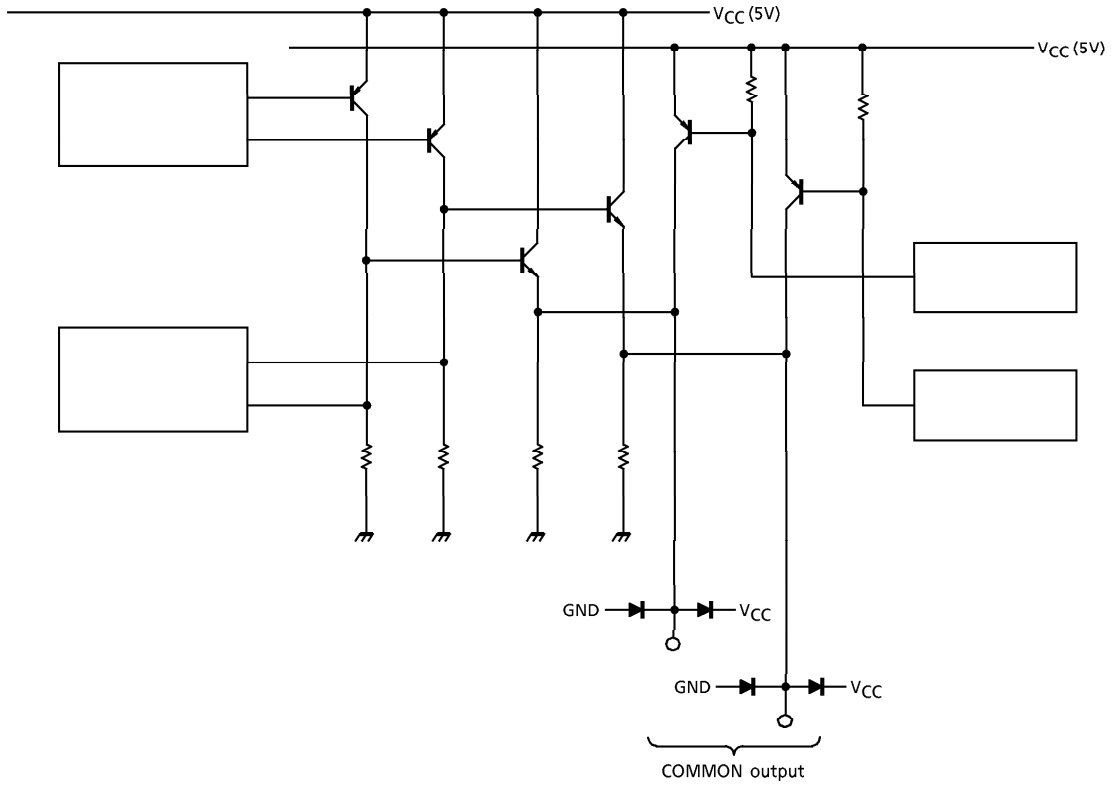
4. Time domain



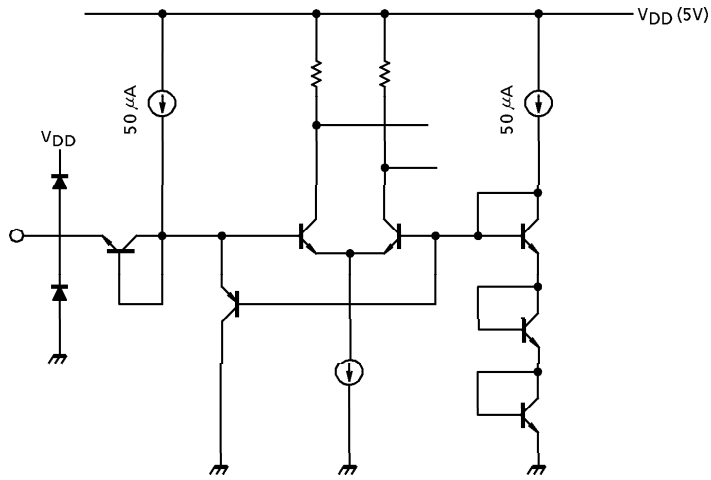
5. W/C control



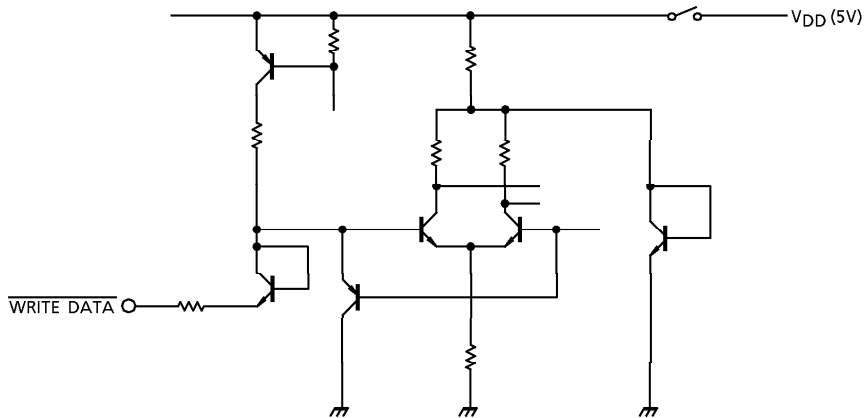
6. Common driver output



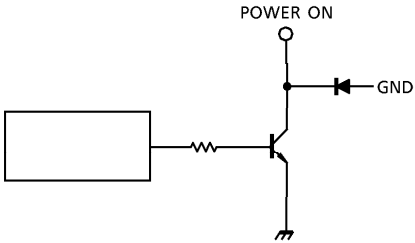
7.  $\overline{\text{WRITE GATE}}$ ,  $\overline{\text{ERASE GATE}}$ ,  $\text{SIDE1}$  interface pins



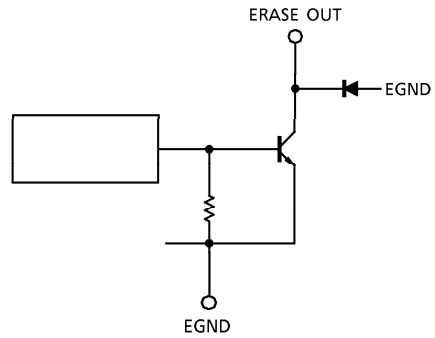
8.  $\overline{\text{WRITE DATA}}$  interface pin



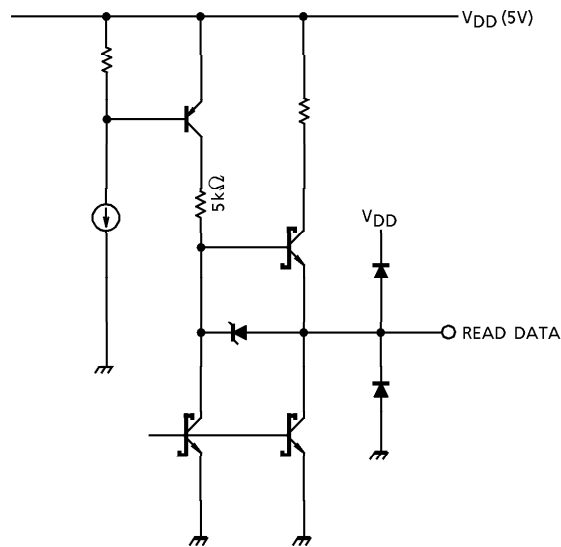
9. Power monitor output



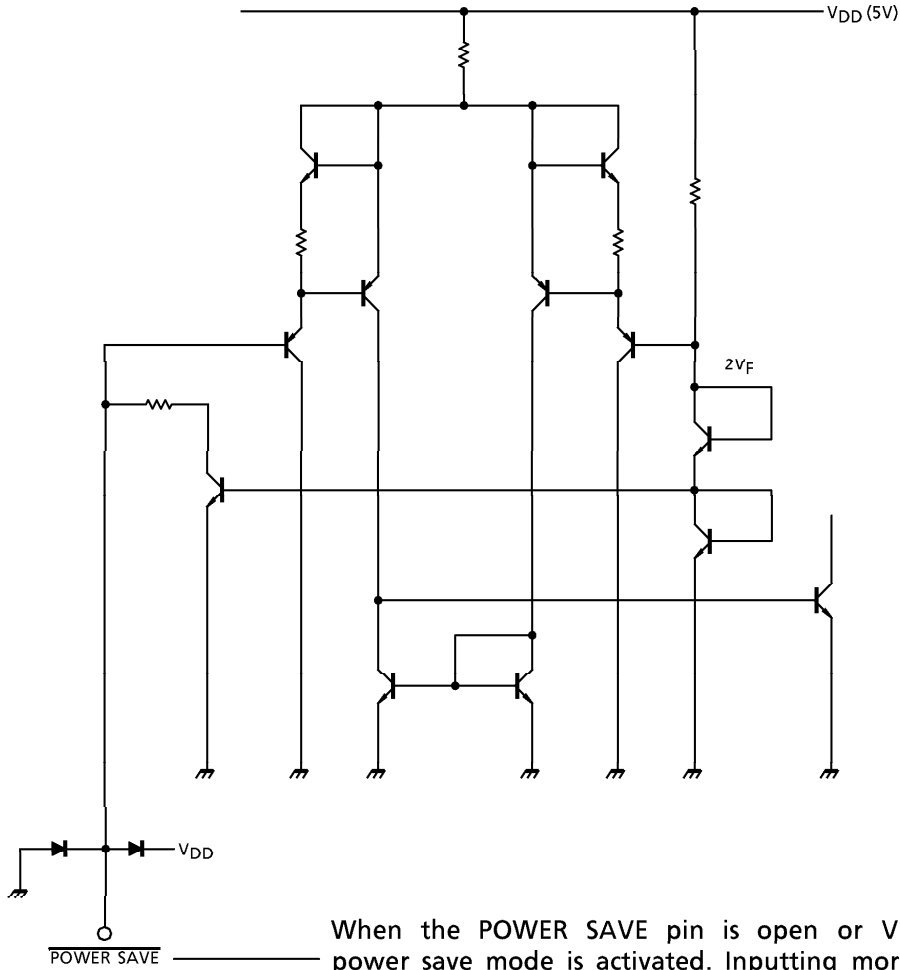
10. Erase output



11. Read data output



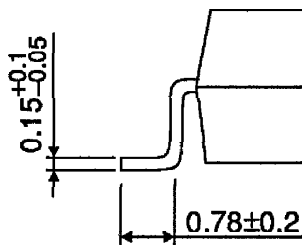
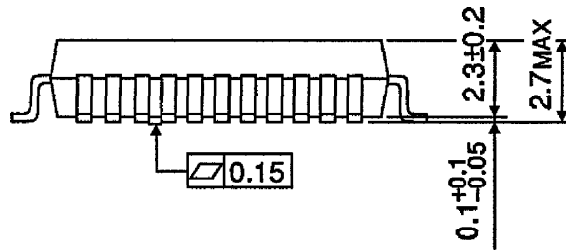
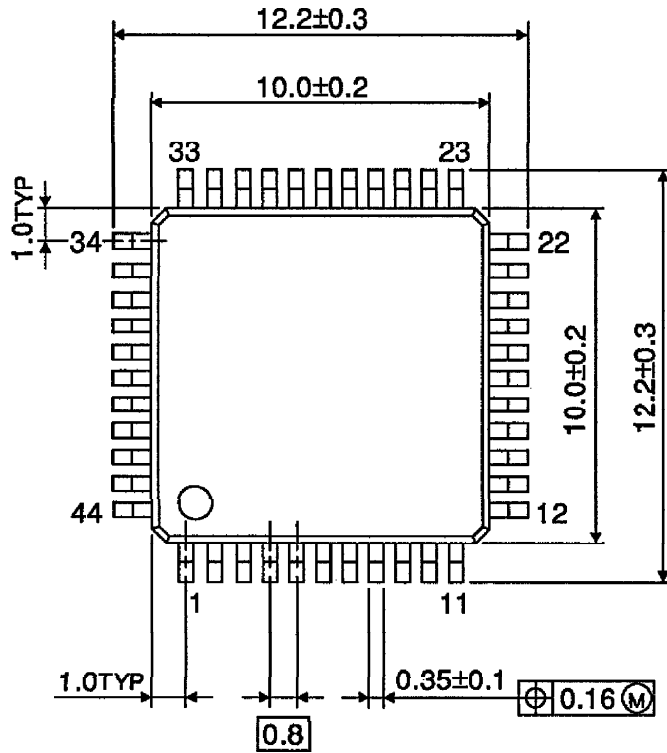
12. POWER SAVE interface pin



When the POWER SAVE pin is open or  $V_{LIN}$  or less  $V_{LIN}$  input, power save mode is activated. Inputting more than  $V_{HIN}$  deactivates power save mode.

OUTLINE DRAWING  
QFP44-P-1010-0.80B

Unit : mm



Weight : 0.56g (Typ.)