SDPD001

Field-Programmable Logic Data Book

1983

ALS Programmable Array Logic and ALS FPLs with Applications Data

TEXAS INSTRUMENTS

Field-Programmable Logic Data Book

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FIELD-PROGRAMMABLE LOGIC DATA BOOK
1983

TI invented the Integrated Circuit, the Microprocessor, and the Microcomputer, which made TI synonymous with reliability, affordability, and compactness. The products in this book carry on TI's tradition of technology leadership.

This data book describes TI's line of Field-Programmable Logic devices. Included are 20-pin and 24-pin fixed-OR-arrays (FOA) and FPLAs featuring user programmable sum-of-products.

The 20-pin fixed-OR-arrays are pin-compatible with other programmable logic array devices available. The FPL products combine the ALS technology and proven titanium-tungsten (TI-W) fuses for reliable, high performance.

The SN74PL839 and SN74PL840 field-programmable logic arrays contain 6 sum-of-products output functions that can be programmed either active high or active low depending on your system's needs.

TI's product plans include several high-complexity fixed-OR-array versions featuring registered inputs, registered-OR-latched outputs, Exclusive-OR, fixed-OR-arrays, and simple fixed-OR-arrays.

This volume offers design and specification data for Field-Programmable Logic, as well as application data. Complete technical data for any TI semiconductor product is available from your nearest TI field sales office, Information Services, Texas Instruments Incorporated, P.O. Box 225012, MS 308, Dallas, Texas 75265.

We sincerely hope you will find TI's Field-Programmable Logic Data Book a meaningful addition to your technical library.

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- **Choice of operating Speeds**
  - **—1 Parts . . . 35 MHz Max, Standard power**
  - **—2 Parts . . . 25 MHz Max, Half power**
- **Plug-In Compatible with Part Numbers: PAL16L8, PAL16R4, PAL16R6, PAL16R8**

DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
'PL16L8	10	2	0	6
'PL16R4	8	0	4 (3-state)	4
'PL16R6	8	0	6 (3-state)	2
'PL16R8	8	0	8 (3-state)	0

description

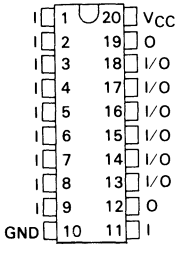
These fixed-OR arrays provide 3-state outputs for bus-oriented systems. They combine Advanced Low-Power Schottky technology with proven titanium-tungsten fuses for reliable, high-performance substitutes for conventional TTL logic. Standard arrays and programmability allow quick design of "custom" functions and more compact boards. The −1 and −2 parts offer a choice of operating frequency, switching times, and power dissipation.

The SN54PL16' is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74PL16' is characterized for operation from 0°C to 70°C.

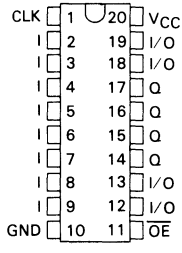
pin assignments in operating mode (voltages at pins 1 and 11 less than V_{IHH})

SN54PL' . . . J PACKAGE
SN74PL' . . . N PACKAGE
(TOP VIEWS)

'PL16L8



'PL16R4



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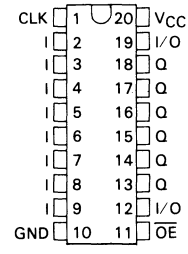

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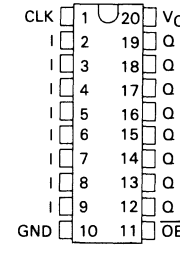
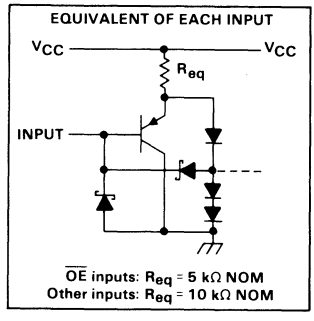
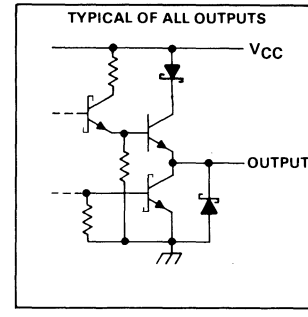


schematics of inputs and outputs



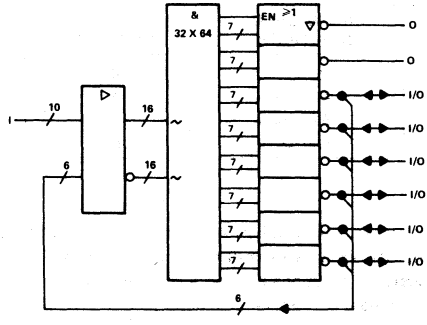


ADVANCE INFORMATION

This document contains information on a new product.
Specifications are subject to change without notice.

functional block diagrams (positive logic)

'PL16L8



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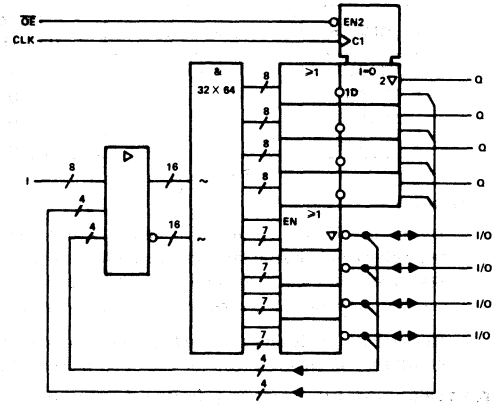

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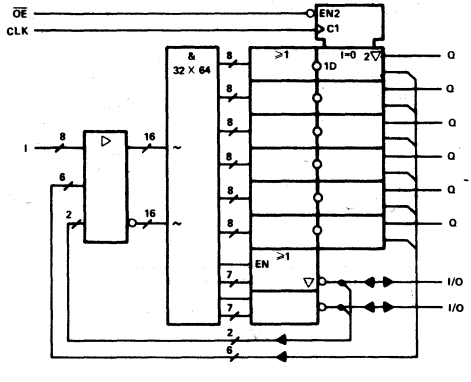

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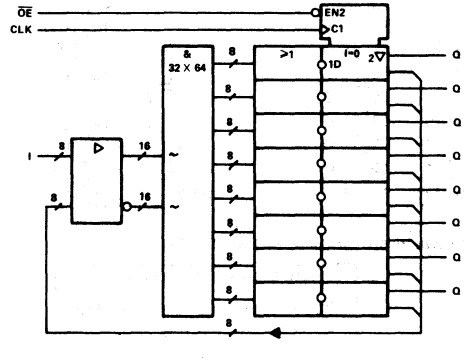


~ denotes fused inputs

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage (see Note 1) ..... 5.5 V
Voltage applied to a disabled output (see Note 1) ..... 5.5 V
Operating free-air temperature range: SN54PL' ..... −55°C to 125°C
SN74PL' ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

PARAMETER		SN54PL16'			SN74PL16'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2		5.5	2		5.5	V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−3.2	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics, over recommended free-operating temperature range

PARAMETER		TEST CONDITIONS†		SN54PL16'			SN74PL16'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}		V_{CC} = MIN, I_{OH} = MAX		2.4	3.2		2.4	3.3		V
V_{OL}		V_{CC} = MIN, I_{OL} = MAX			0.25	0.4		0.35	0.5	V
I_{OZH}	Outputs	V_{CC} = MAX, V_O = 2.7 V				20			20	μA
	I/O ports					100			100	
I_{OZL}	Outputs	V_{CC} = MAX, V_O = 0.4 V				−20			−20	μA
	I/O ports					−250			−250	
I_I		V_{CC} = MAX, V_I = 5.5 V				0.1			0.1	mA
I_{IH}		V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	$\overline{OE}$ input	V_{CC} = MAX, V_I = 0.4 V	−1 Parts			−0.4			−0.4	mA
	All others					−0.2			−0.2	
	$\overline{OE}$ input		−2 Parts			−0.2			−0.2	
	All others					−0.1			−0.1	
I_O§		V_{CC} = MAX, V_O = 2.25 V		−30		−125	−30		−125	mA
I_{CC}		V_{CC} = MAX, V_I = 0 V, $\overline{OE}$ at 4.5 V, Outputs open	−1 Parts		140	185		140	180	mA
			−2 Parts		75	95		70	90	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'PL16R4, 'PL16R6, 'PL16R8 timing requirements

		-1 PARTS			-2 PARTS			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
f_{clock}	Clock frequency	0		35				MHz
t_w	Pulse duration, clock high or low	12						ns
t_{su}	Setup time, input or feedback before CLK↑	15						ns
t_h	Hold time, input or feedback after CLK↑	0						ns

switching characteristics over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	-1 PARTS			-2 PARTS			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}			R_L = 500 Ω, C_L = 50 pf	35	45			35		MHz
t_{pd}	I, I/O	O, I/O			16	25		32		ns
t_{pd}	CLK↑	Q		7	10	15		20		ns
t_{en}	$\overline{OE}$↓	Q			18	25		36		ns
t_{dis}	$\overline{OE}$↑	Q			10	15		20		ns
t_{en}	I, I/O	O, I/O			18	25		36		ns
t_{dis}	I, I/O	O, I/O			14	25		28		ns

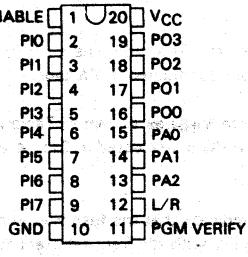
†All typical values are at V_{CC} = 5 V, T_A = 25°C.

programming parameters, T_A = 25°C

			MIN	NOM	MAX	UNIT
V_{CC}	Verify-level supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
V_{IHH}	Program-pulse input voltage		10.25	10.5	10.75	V
I_{IHH}	Program-pulse input current	PO		20	50	mA
		PGM ENABLE, L/R		10	25	
		PI, PA		1.5	5	
		V_{CC}		250	400	
t_{w1}	Program-pulse duration at PO pins		10		50	μs
t_{w2}	Pulse duration at PGM VERIFY		100			ns
	Program-pulse duty cycle at PO pins				25	%
t_{su}	Setup time		100			ns
t_h	Hold time		100			ns
t_{d1}	Delay time from V_{CC} to 5 V to PGM VERIFY ↑		100			μs
t_{d2}	Delay time from PGM VERIFY ↑ to valid output		200			ns
	Input voltage at pins 1 and 11 to open verify-protect (security) fuse		20	21	22	V
	Input current to open verify-protect (security) fuse				400	mA
	Pulse duration to open verify-protect (security) fuse		20		50	ms

pin assignments in programming mode (PGM ENABLE, pin 1 or pin 11, at V_{IHH})

PRODUCT TERMS 0 THRU 31
(TOP VIEW)



PRODUCT TERMS 32 THRU 63
(TOP VIEW)

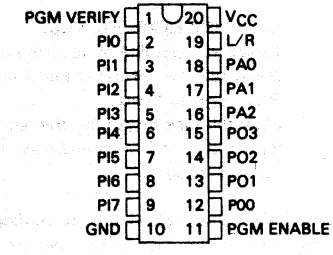


TABLE 1 — INPUT LINE SELECT

INPUT LINE NUMBER	PIN NAME								
	PI7	PI6	PI5	PI4	PI3	PI2	PI1	PI0	L/R
0	HH	HH	HH	HH	HH	HH	HH	L	Z
1	HH	HH	HH	HH	HH	HH	HH	H	Z
2	HH	HH	HH	HH	HH	HH	HH	L	HH
3	HH	HH	HH	HH	HH	HH	HH	H	HH
4	HH	HH	HH	HH	HH	HH	L	HH	Z
5	HH	HH	HH	HH	HH	HH	H	HH	Z
6	HH	HH	HH	HH	HH	HH	L	HH	HH
7	HH	HH	HH	HH	HH	HH	H	HH	HH
8	HH	HH	HH	HH	HH	L	HH	HH	Z
9	HH	HH	HH	HH	HH	H	HH	HH	Z
10	HH	HH	HH	HH	HH	L	HH	HH	HH
11	HH	HH	HH	HH	HH	H	HH	HH	HH
12	HH	HH	HH	HH	L	HH	HH	HH	Z
13	HH	HH	HH	HH	H	HH	HH	HH	Z
14	HH	HH	HH	HH	L	HH	HH	HH	HH
15	HH	HH	HH	HH	H	HH	HH	HH	HH
16	HH	HH	HH	L	HH	HH	HH	HH	Z
17	HH	HH	HH	H	HH	HH	HH	HH	Z
18	HH	HH	HH	L	HH	HH	HH	HH	HH
19	HH	HH	HH	H	HH	HH	HH	HH	HH
20	HH	HH	L	HH	HH	HH	HH	HH	Z
21	HH	HH	H	HH	HH	HH	HH	HH	Z
22	HH	HH	L	HH	HH	HH	HH	HH	HH
23	HH	HH	H	HH	HH	HH	HH	HH	HH
24	HH	L	HH	HH	HH	HH	HH	HH	Z
25	HH	H	HH	HH	HH	HH	HH	HH	Z
26	HH	L	HH	HH	HH	HH	HH	HH	HH
27	HH	H	HH	HH	HH	HH	HH	HH	HH
28	L	HH	HH	HH	HH	HH	HH	HH	Z
29	H	HH	HH	HH	HH	HH	HH	HH	Z
30	L	HH	HH	HH	HH	HH	HH	HH	HH
31	H	HH	HH	HH	HH	HH	HH	HH	HH

TABLE 2 — PRODUCT LINE SELECT

PRODUCT LINE NUMBER	PIN NAME						
	PO0	PO1	PO2	PO3	PA2	PA1	PA0
0, 32	Z	Z	Z	HH	Z	Z	Z
1, 33	Z	Z	Z	HH	Z	Z	HH
2, 34	Z	Z	Z	HH	Z	HH	Z
3, 35	Z	Z	Z	HH	Z	HH	HH
4, 36	Z	Z	Z	HH	HH	Z	Z
5, 37	Z	Z	Z	HH	HH	Z	HH
6, 38	Z	Z	Z	HH	HH	HH	Z
7, 39	Z	Z	Z	HH	HH	HH	HH
8, 40	Z	Z	HH	Z	Z	Z	Z
9, 41	Z	Z	HH	Z	Z	Z	HH
10, 42	Z	Z	HH	Z	Z	HH	Z
11, 43	Z	Z	HH	Z	Z	HH	HH
12, 44	Z	Z	HH	Z	HH	Z	Z
13, 45	Z	Z	HH	Z	HH	Z	HH
14, 46	Z	Z	HH	Z	HH	HH	Z
15, 47	Z	Z	HH	Z	HH	HH	HH
16, 48	Z	HH	Z	Z	Z	Z	Z
17, 49	Z	HH	Z	Z	Z	Z	HH
18, 50	Z	HH	Z	Z	Z	HH	Z
19, 51	Z	HH	Z	Z	Z	HH	HH
20, 52	Z	HH	Z	Z	HH	Z	Z
21, 53	Z	HH	Z	Z	HH	Z	HH
22, 54	Z	HH	Z	Z	HH	HH	Z
23, 55	Z	HH	Z	Z	HH	HH	HH
24, 56	HH	Z	Z	Z	Z	Z	Z
25, 57	HH	Z	Z	Z	Z	Z	HH
26, 58	HH	Z	Z	Z	Z	HH	Z
27, 59	HH	Z	Z	Z	Z	HH	HH
28, 60	HH	Z	Z	Z	HH	Z	Z
29, 61	HH	Z	Z	Z	HH	Z	HH
30, 62	HH	Z	Z	Z	HH	HH	Z
31, 63	HH	Z	Z	Z	HH	HH	HH

L = V_{IL}, H = V_{IH}, HH = V_{IHH}, Z = high impedance (e.g., 10 kΩ to 5 V)

programming procedure for array fuses

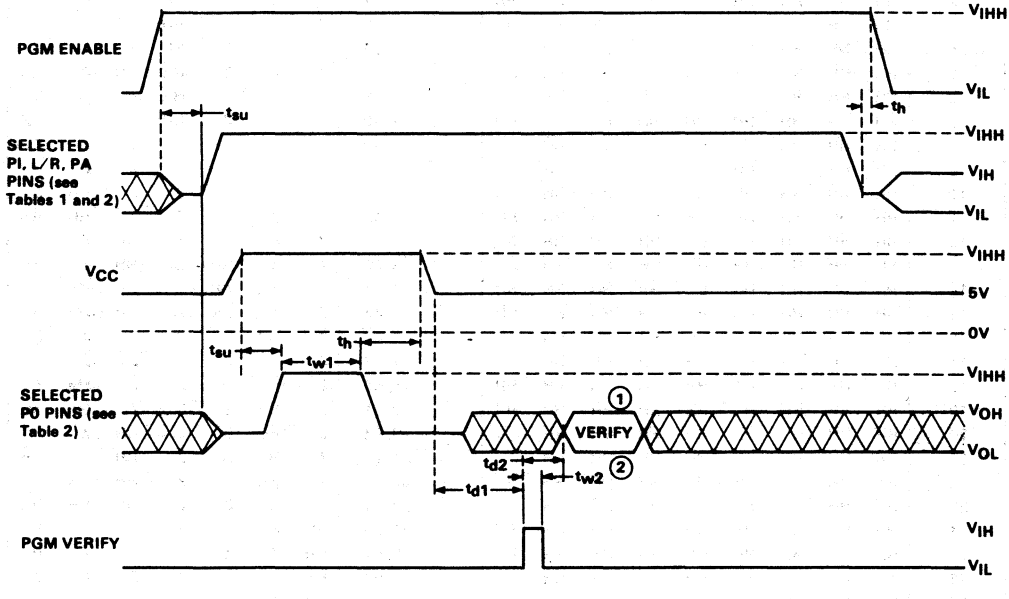
Array fuses are programmed using a linear select method. Each fuse can be opened by selecting the appropriate (one of 32) input line and then pulsing the correct (one of 64) product line. The levels for selecting input lines and product lines are shown in Tables 1 and 2.

Step 1	Raise PGM ENABLE to V_{IHH}.
Step 2	Select an input line by applying appropriate levels to L/R and PI pins.
Step 3	Begin selection of the output line with appropriate conditions on PA pins.
Step 4	Raise V_{CC} to V_{IHH}.
Step 5	Blow the fuse by pulsing the appropriate PO pin to V_{IHH} as shown in Table 2 for the product line.
Step 6	Return V_{CC} to 5 volts and pulse PGM Verify. The PO pin selected in Step 4 will be less than V_{OL} if the fuse is open.

Steps 1 through 6 may be repeated if the verification does not indicate that the fuse was successfully programmed (blown), but no more than four times. Verification is possible only with the verify-protect fuse intact.

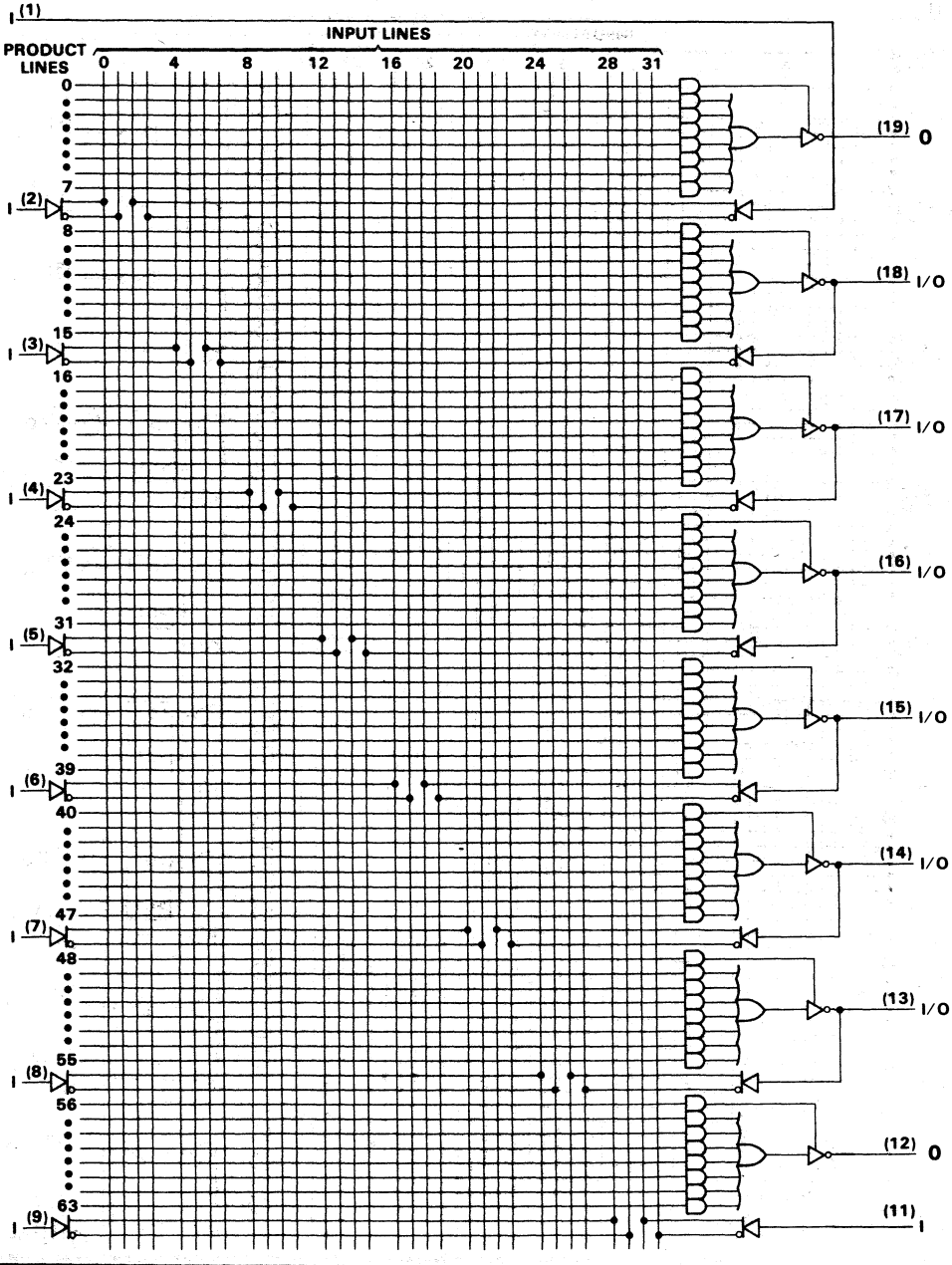
To prevent further verification, two last fuses may be blown by raising pin 1 and pin 11 to 21 volts ±1 volt. V_{CC} is required to be at 0 during this operation.

programming waveforms



① A high level during the verify interval indicates that programming has not been successful.
② A low level during the verify interval indicates that programming has been successful.

LOGIC DIAGRAM



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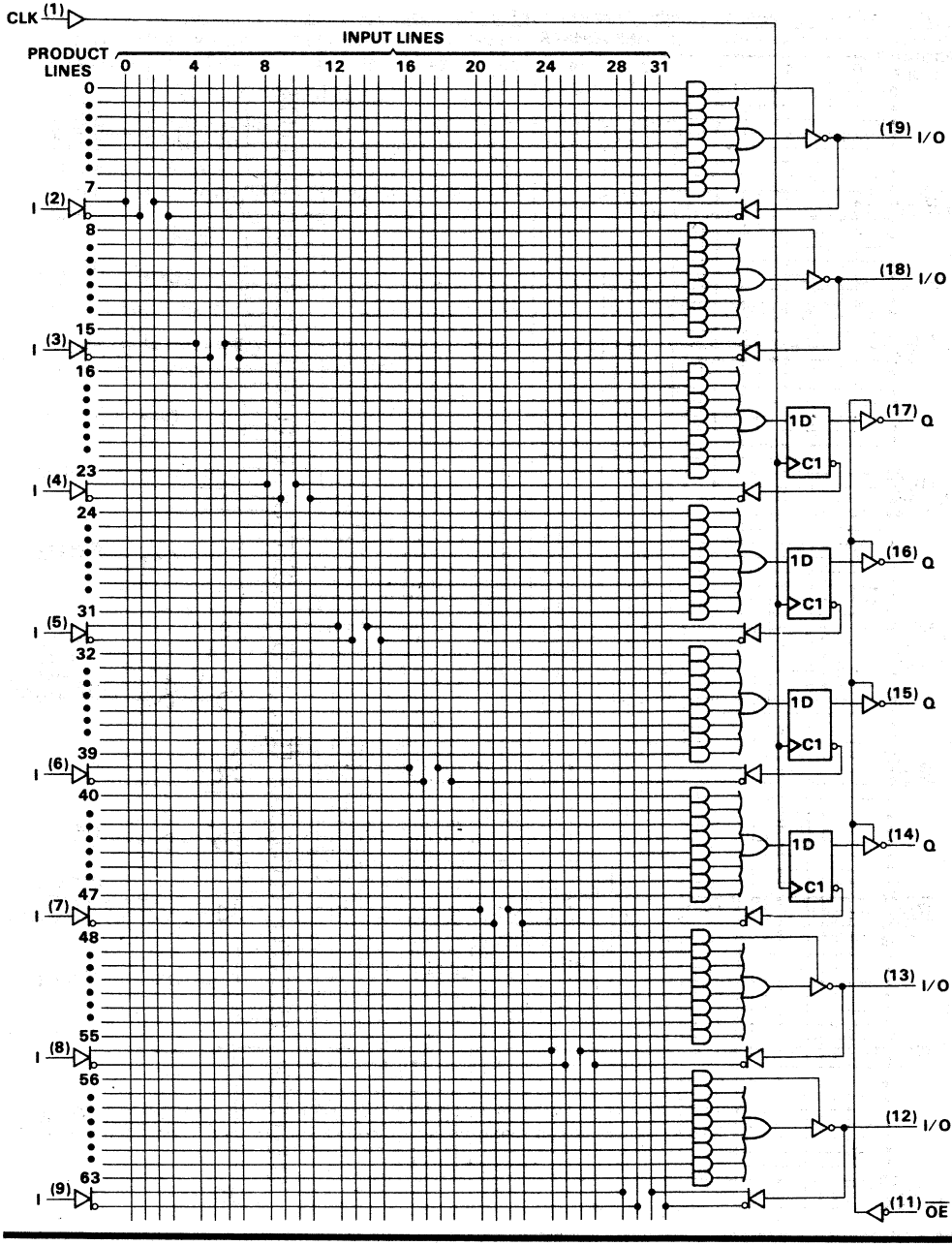
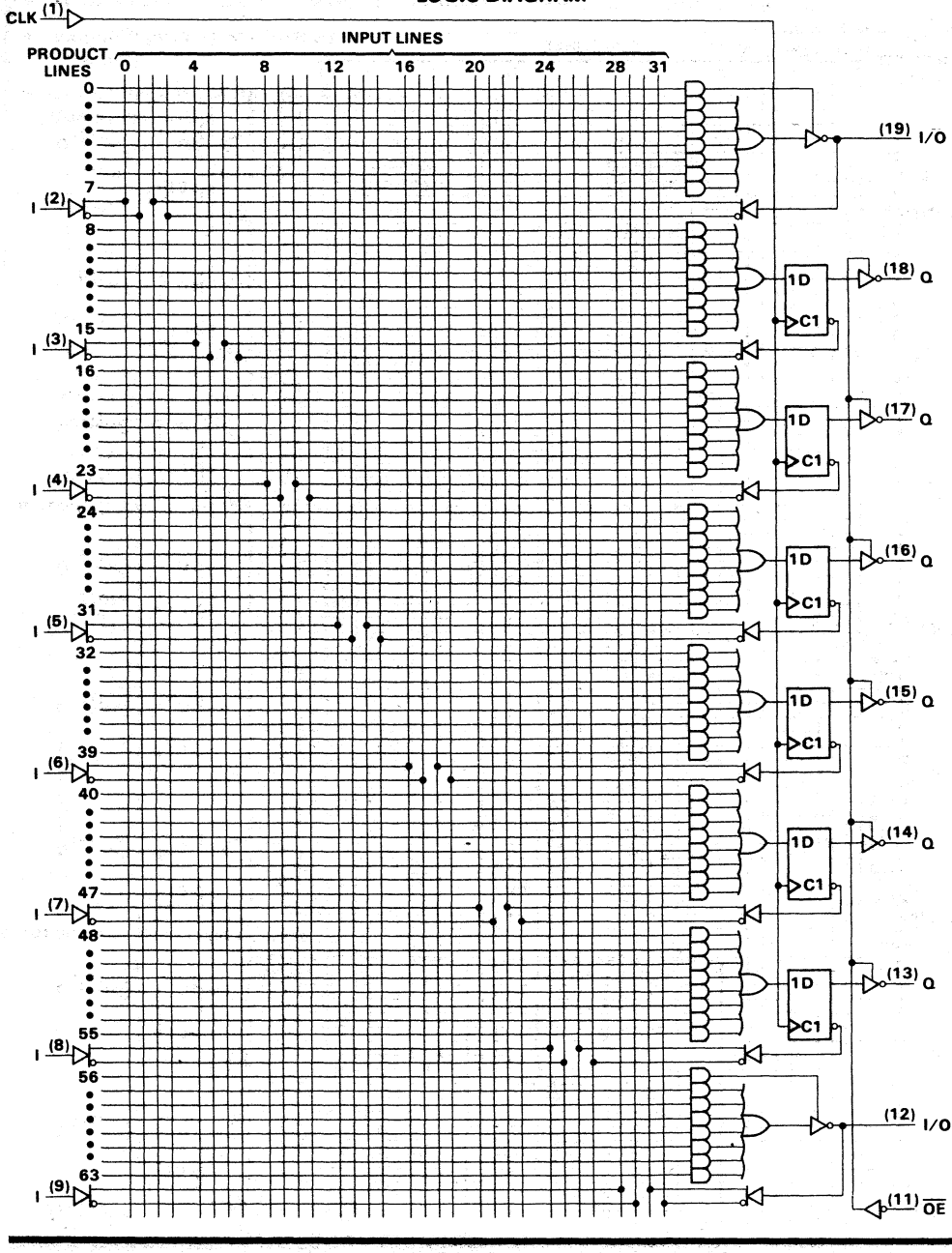
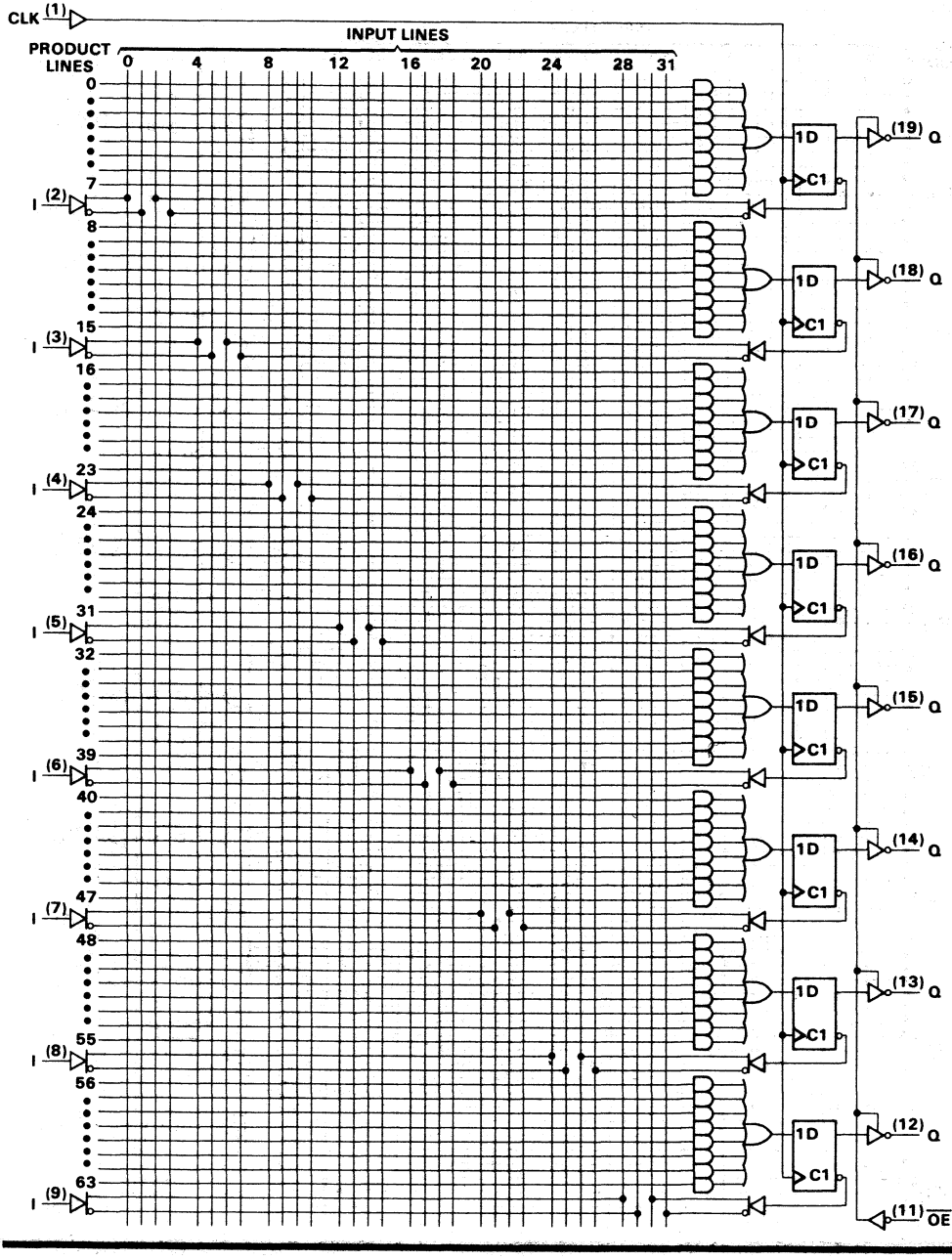
LOGIC DIAGRAM



LOGIC DIAGRAM



LOGIC DIAGRAM



TYPES SN54PL20L8, SN54PL20R4, SN54PL20R6, SN54PL20R8
SN74PL20L8, SN74PL20R4, SN74PL20R6, SN74PL20R8
FIXED-OR ARRAYS

D2706, DECEMBER 1982—REVISED SEPTEMBER 1983

- **Standard 24-Pin, 300-mil Packages**
- **Output Registers Have Preload Capability**
- **Output Registers Automatically Clear During Power-Up**
- **Choice of Operating Speeds**
  - **—1 Parts . . . 30 MHz Max, Standard power**
  - **—2 Parts . . . 20 MHz Max, Half power**

DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
'PL20L8	14	2	0	6
'PL20R4	12	0	4 (3-state buffers)	4
'PL20R6	12	0	6 (3-state buffers)	2
'PL20R8	12	0	8 (3-state buffers)	0

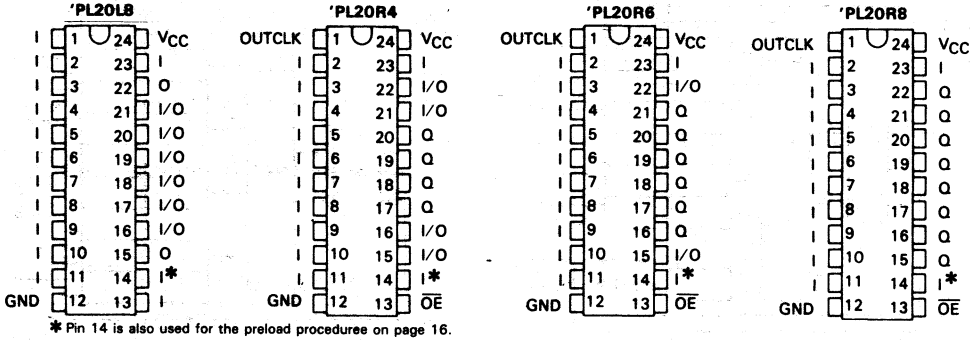
description

These fixed-OR arrays provide 3-state outputs for bus-oriented systems. The 'PL20L8, 'PL20R4, and 'PL20R6 have output registers that can be loaded from the I/O pins by a preload procedure. All the outputs are automatically set to a low level when power is applied. The —1 and —2 parts offer a choice of operating frequency, switching times, and power dissipation.

The SN54PL20' is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74PL20' is characterized for operation from 0°C to 70°C.

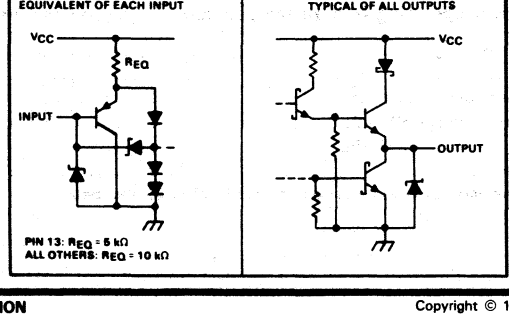
pin assignments in operating mode (voltages at pins 1 and 13 less than V_{IHH})

SN54' ... JT PACKAGE
SN74' ... NT PACKAGE
(TOP VIEW)



* Pin 14 is also used for the preload proceduree on page 16.

schematics of inputs and outputs



ADVANCE INFORMATION

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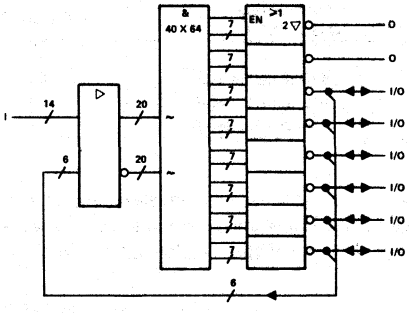
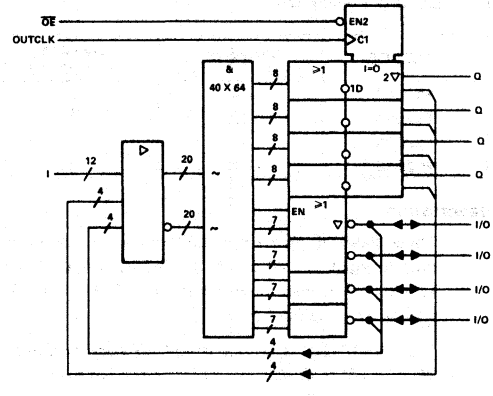
functional block diagrams (positive logic)

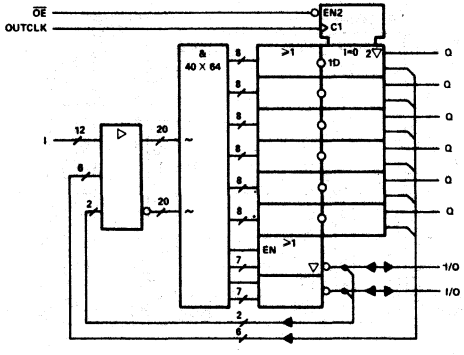
'PL20L8



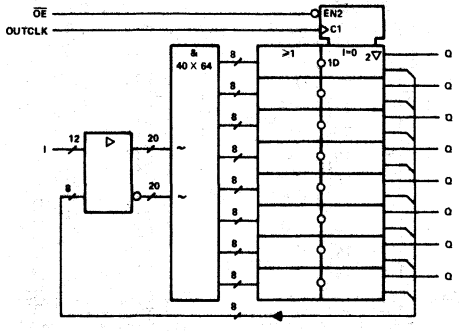
'PL20R4



'PL20R6



'PL20R8



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage (see Note 1) ..... 5.5 V
Voltage applied to a disabled output (see Note 1) ..... 5.5 V
Operating free-air temperature range: SN54PL' ..... −55°C to 125°C
SN74PL' ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during preload cycle.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

recommended operating conditions

		SN54PL19R'			SN74PL19R'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2		5.5	2		5.5	V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−3.2	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended free-air operating temperature range

PARAMETER		TEST CONDITIONS†		SN54PL20'			SN74PL20'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = MIN,	I_{OH} = MAX	2.4	3.2		2.4	3.3		V
V_{OL}		V_{CC} = MIN,	I_{OL} = MAX		0,25	0.4		0.35	0.5	V
I_{OZH}	O, Q outputs	V_{CC} = MAX,	V_{IH} = 2.7 V			20			20	μA
	I/O ports					100			100	
I_{OZL}	O, Q outputs	V_{CC} = MAX,	V_{IH} = 0.4 V			−20			−20	μA
	I/O ports					−250			−250	
I_I	$\overline{OE}$ input	V_{CC} = MAX,	V_I = 5.5 V			0.2			0.2	mA
	All others					0.1			0.1	
I_{IH}	$\overline{OE}$ input	V_{CC} = MAX,	V_I = 2.7 V			40			40	μA
	All others					20			20	
I_{IL}	$\overline{OE}$ input	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
	All others					−0.2			−0.2	
I_O§		V_{CC} = MAX,	V_O = 2.25 V	−30		−125	−30		−125	mA
I_{CC}	−1 Parts	V_{CC} = MAX,	V_I = 0 V,		150	200		150	200	mA
	−2 Parts	Outputs open,	$\overline{OE}$ at V_{IH}		75	100		75	100	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half the true short-circuit current, I_{OS}.

'PL20R4, 'PL20R6, 'PL20R8 timing requirements

		−1 PARTS		−2 PARTS		UNIT
		MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	30	0	20	MHz
t_w	Pulse duration, clock high or low	12		12		ns
t_{su}	Setup time, input or feedback before OUTCLK↑	15		15		ns
t_h	Hold time, input or feedback before OUTCLK↑	0		0		ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	−1 PARTS			−2 PARTS			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{max}			R_L = 500 Ω, C_L = 50 pF	30			20			MHz
t_{pd}	I, I/O	O, I/O			16			25		ns
t_{pd}	OUTCLK↑	Q			12			20		ns
t_{en}	$\overline{OE}$	Q			8			15		ns
t_{dis}	$\overline{OE}$↑	Q			6			12		ns
t_{en}	I, I/O	O, I/O			18			25		ns
t_{dis}	I, I/O	O, I/O			13			20		ns

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

PRELOAD PROCEDURES

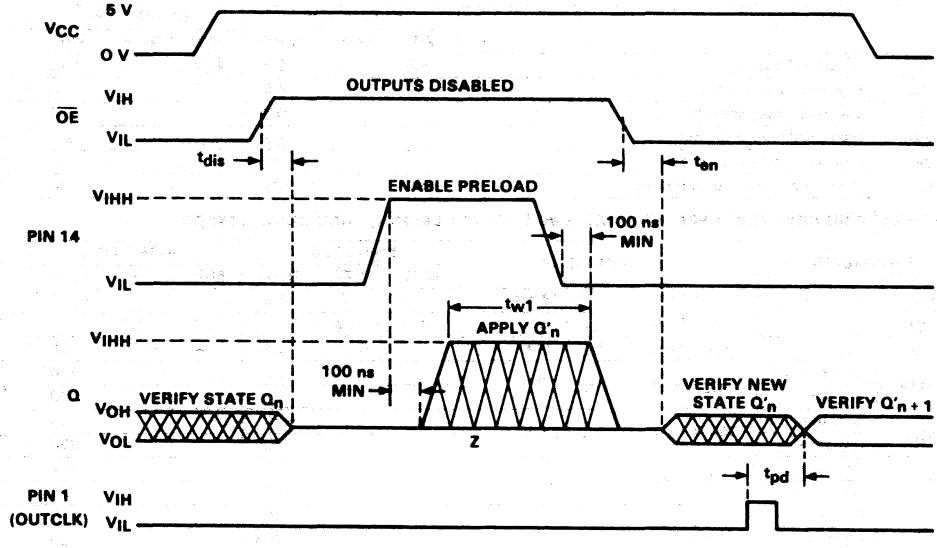


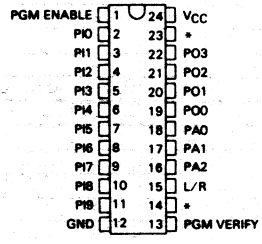
FIGURE 1—PRELOAD WAVEFORMS

preload procedure for registered outputs

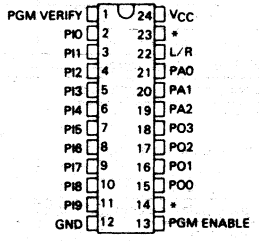
Step 1	Pin 13 to V_{IH}, Pin 1 to V_{IL}, and V_{CC} to 5 volts.
Step 2	Pin 14 to V_{IHH} for 10 to 50 microseconds.
Step 3	Apply an open circuit for a low and V_{IHH} for a high at the Q outputs.
Step 4	Pin 14 to V_{IL}.
Step 5	Remove the voltages applied to the outputs.
Step 6	Pin 13 to V_{IL}.
Step 7	Check the output states to verify preload.

pin assignments in programming mode (PGM ENABLE at V_{IHH})

PRODUCT TERMS 0 THRU 31
(TOP VIEW)



PRODUCT TERMS 32 THRU 63
(TOP VIEW)



*Pin 14 has no programming function. Make no connection.

TABLE 1—INPUT LINE SELECT

INPUT LINE NUMBER	PIN NAME										
	PI9	PI8	PI7	PI6	PI5	PI4	PI3	PI2	PI1	PI0	L/R
0	HH	HH	HH	HH	HH	HH	HH	HH	HH	L	Z
1	HH	HH	HH	HH	HH	HH	HH	HH	HH	H	Z
2	HH	HH	HH	HH	HH	HH	HH	HH	HH	L	HH
3	HH	HH	HH	HH	HH	HH	HH	HH	HH	H	HH
4	HH	HH	HH	HH	HH	HH	HH	HH	L	HH	Z
5	HH	HH	HH	HH	HH	HH	HH	HH	H	HH	Z
6	HH	HH	HH	HH	HH	HH	HH	HH	L	HH	HH
7	HH	HH	HH	HH	HH	HH	HH	HH	H	HH	HH
8	HH	HH	HH	HH	HH	HH	HH	L	HH	HH	Z
9	HH	HH	HH	HH	HH	HH	HH	H	HH	HH	Z
10	HH	HH	HH	HH	HH	HH	HH	L	HH	HH	HH
11	HH	HH	HH	HH	HH	HH	HH	H	HH	HH	HH
12	HH	HH	HH	HH	HH	HH	L	HH	HH	HH	Z
13	HH	HH	HH	HH	HH	HH	H	HH	HH	HH	Z
14	HH	HH	HH	HH	HH	HH	L	HH	HH	HH	HH
15	HH	HH	HH	HH	HH	HH	H	HH	HH	HH	HH
16	HH	HH	HH	HH	HH	L	HH	HH	HH	HH	Z
17	HH	HH	HH	HH	HH	H	HH	HH	HH	HH	Z
18	HH	HH	HH	HH	HH	L	HH	HH	HH	HH	HH
19	HH	HH	HH	HH	HH	H	HH	HH	HH	HH	HH
20	HH	HH	HH	HH	L	HH	HH	HH	HH	HH	Z
21	HH	HH	HH	HH	H	HH	HH	HH	HH	HH	Z
22	HH	HH	HH	HH	L	HH	HH	HH	HH	HH	HH
23	HH	HH	HH	HH	H	HH	HH	HH	HH	HH	HH
24	HH	HH	HH	L	HH	HH	HH	HH	HH	HH	Z
25	HH	HH	HH	H	HH	HH	HH	HH	HH	HH	Z
26	HH	HH	HH	L	HH	HH	HH	HH	HH	HH	HH
27	HH	HH	HH	H	HH	HH	HH	HH	HH	HH	HH
28	HH	HH	L	HH	HH	HH	HH	HH	HH	HH	Z
29	HH	HH	H	HH	HH	HH	HH	HH	HH	HH	Z
30	HH	HH	L	HH	HH	HH	HH	HH	HH	HH	HH
31	HH	HH	H	HH	HH	HH	HH	HH	HH	HH	HH
32	HH	L	HH	HH	HH	HH	HH	HH	HH	HH	Z
33	HH	H	HH	HH	HH	HH	HH	HH	HH	HH	Z
34	HH	L	HH	HH	HH	HH	HH	HH	HH	HH	HH
35	HH	H	HH	HH	HH	HH	HH	HH	HH	HH	HH
36	L	HH	HH	HH	HH	HH	HH	HH	HH	HH	Z
37	H	HH	HH	HH	HH	HH	HH	HH	HH	HH	Z
38	L	HH	HH	HH	HH	HH	HH	HH	HH	HH	HH
39	H	HH	HH	HH	HH	HH	HH	HH	HH	HH	HH

TABLE 2—PRODUCT LINE SELECT

PRODUCT LINE NUMBER	PIN NAME						
	PO0	PO1	PO2	PO3	PA2	PA1	PA0
0, 32	Z	Z	Z	HH	Z	Z	Z
1, 33	Z	Z	Z	HH	Z	Z	HH
2, 34	Z	Z	Z	HH	Z	HH	Z
3, 35	Z	Z	Z	HH	Z	HH	HH
4, 36	Z	Z	Z	HH	HH	Z	Z
5, 37	Z	Z	Z	HH	HH	Z	HH
6, 38	Z	Z	Z	HH	HH	HH	Z
7, 39	Z	Z	Z	HH	HH	HH	HH
8, 40	Z	Z	HH	Z	Z	Z	Z
9, 41	Z	Z	HH	Z	Z	Z	HH
10, 42	Z	Z	HH	Z	Z	HH	Z
11, 43	Z	Z	HH	Z	Z	HH	HH
12, 44	Z	Z	HH	Z	HH	Z	Z
13, 45	Z	Z	HH	Z	HH	Z	HH
14, 46	Z	Z	HH	Z	HH	HH	Z
15, 47	Z	Z	HH	Z	HH	HH	HH
16, 48	Z	HH	Z	Z	Z	Z	Z
17, 49	Z	HH	Z	Z	Z	Z	HH
18, 50	Z	HH	Z	Z	Z	HH	Z
19, 51	Z	HH	Z	Z	Z	HH	HH
20, 52	Z	HH	Z	Z	HH	Z	Z
21, 53	Z	HH	Z	Z	HH	Z	HH
22, 54	Z	HH	Z	Z	HH	HH	Z
23, 55	Z	HH	Z	Z	HH	HH	HH
24, 56	HH	Z	Z	Z	Z	Z	Z
25, 57	HH	Z	Z	Z	Z	Z	HH
26, 58	HH	Z	Z	Z	Z	HH	Z
27, 59	HH	Z	Z	Z	Z	HH	HH
28, 60	HH	Z	Z	Z	HH	Z	Z
29, 61	HH	Z	Z	Z	HH	Z	HH
30, 62	HH	Z	Z	Z	HH	HH	Z
31, 63	HH	Z	Z	Z	HH	HH	HH

L = V_{IL}, H = V_{IH}, HH = V_{IHH}, Z = high impedance (e.g., 10 kΩ to 5 V)

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programming parameters, T_A = 25°C

			MIN	NOM	MAX	UNIT
V_{CC}	Verify-level supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage		0		0.8	V
V_{OH}	High-level output voltage				5.5	V
V_{IHH}	Program-pulse input voltage		10.25	10.5	10.75	V
I_{IHH}	Program-pulse input current	PO			50	mA
		PGM ENABLE, L/R			25	
		PI, PA			5	
		V_{CC}			400	
t_{w1}	Program-pulse duration at PO pins		10		50	μs
t_{w2}	Pulse duration at PGM VERIFY		100			ns
t_{su}	Setup time		100			ns
t_h	Hold time		100			ns
t_{d1}	Delay time from V_{CC} to 5 V to PGM VERIFY ↑		100			μs
t_{d2}	Delay time from PGM VERIFY ↑ to valid output		200			ns
	Input voltage at pins 1 and 13 to open verify-protect (security) fuse)		20	21	22	V
	Input current to open verify-protect (security) fuse				400	mA
	Pulse duration to open verify-protect (security) fuse		20		50	ms

PROGRAMMING PROCEDURES

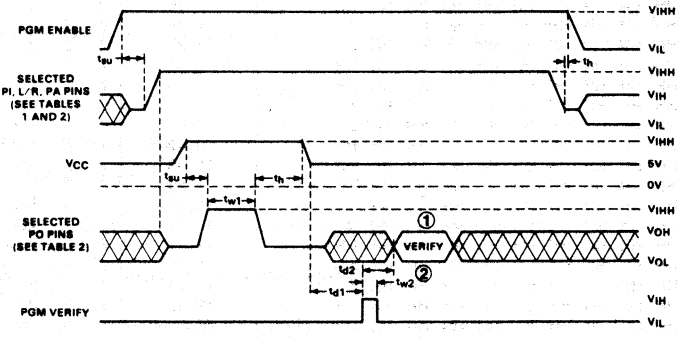


FIGURE 2—ARRAY PROGRAMMING WAVEFORMS

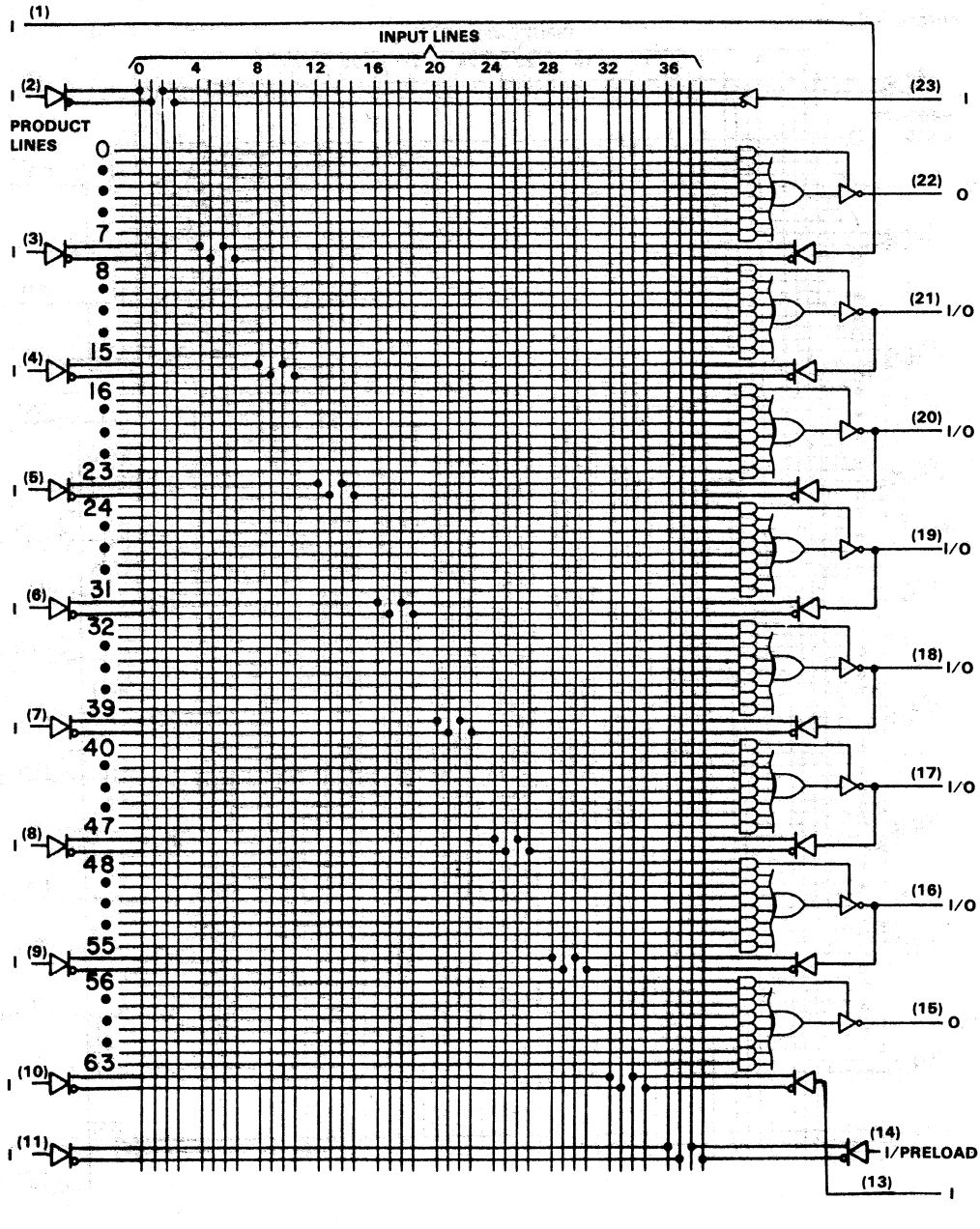
① A high level during the verify interval indicates that programming has not been successful.
② A low level during the verify interval indicates that programming has been successful.

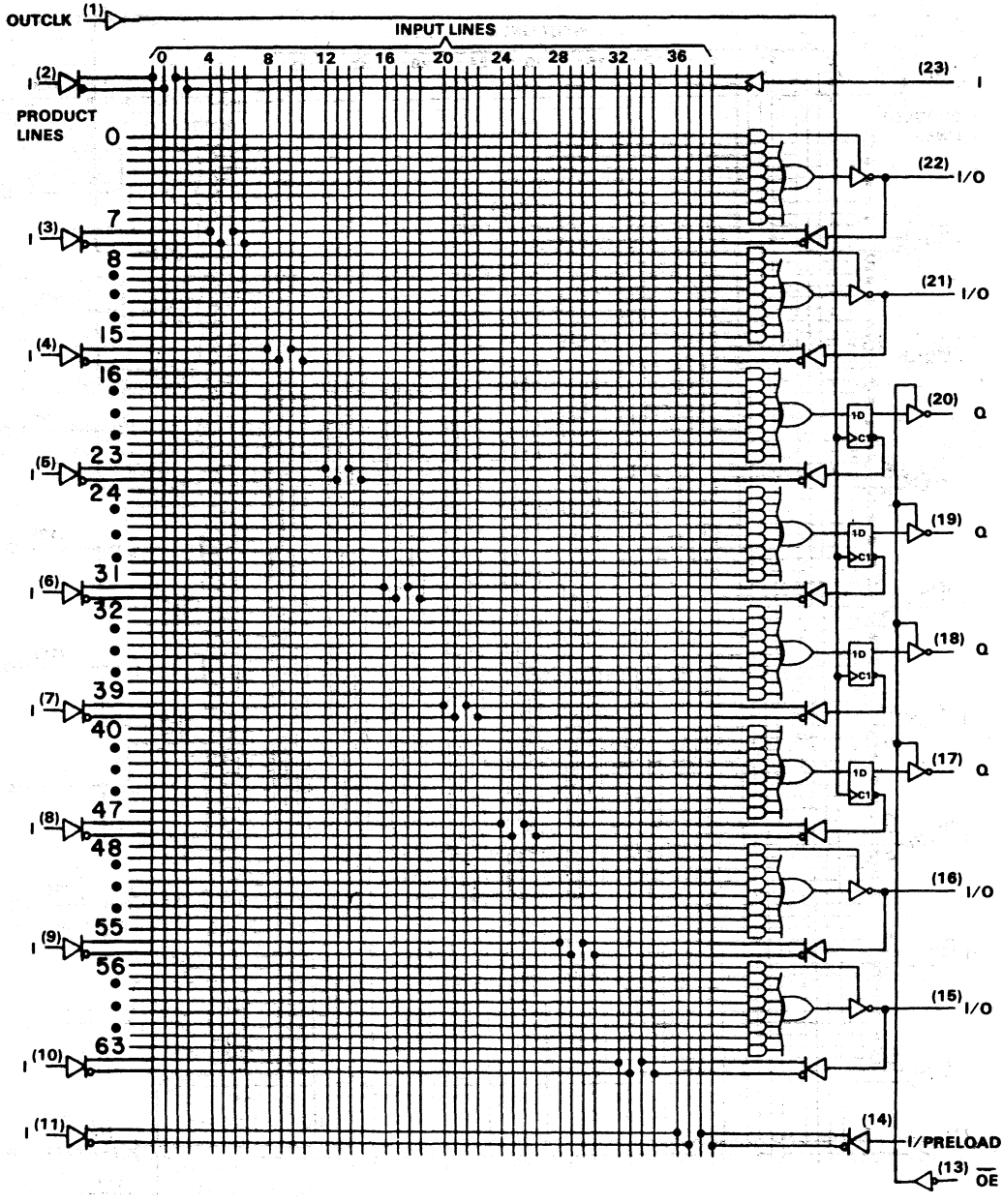
programming procedure for array fuses

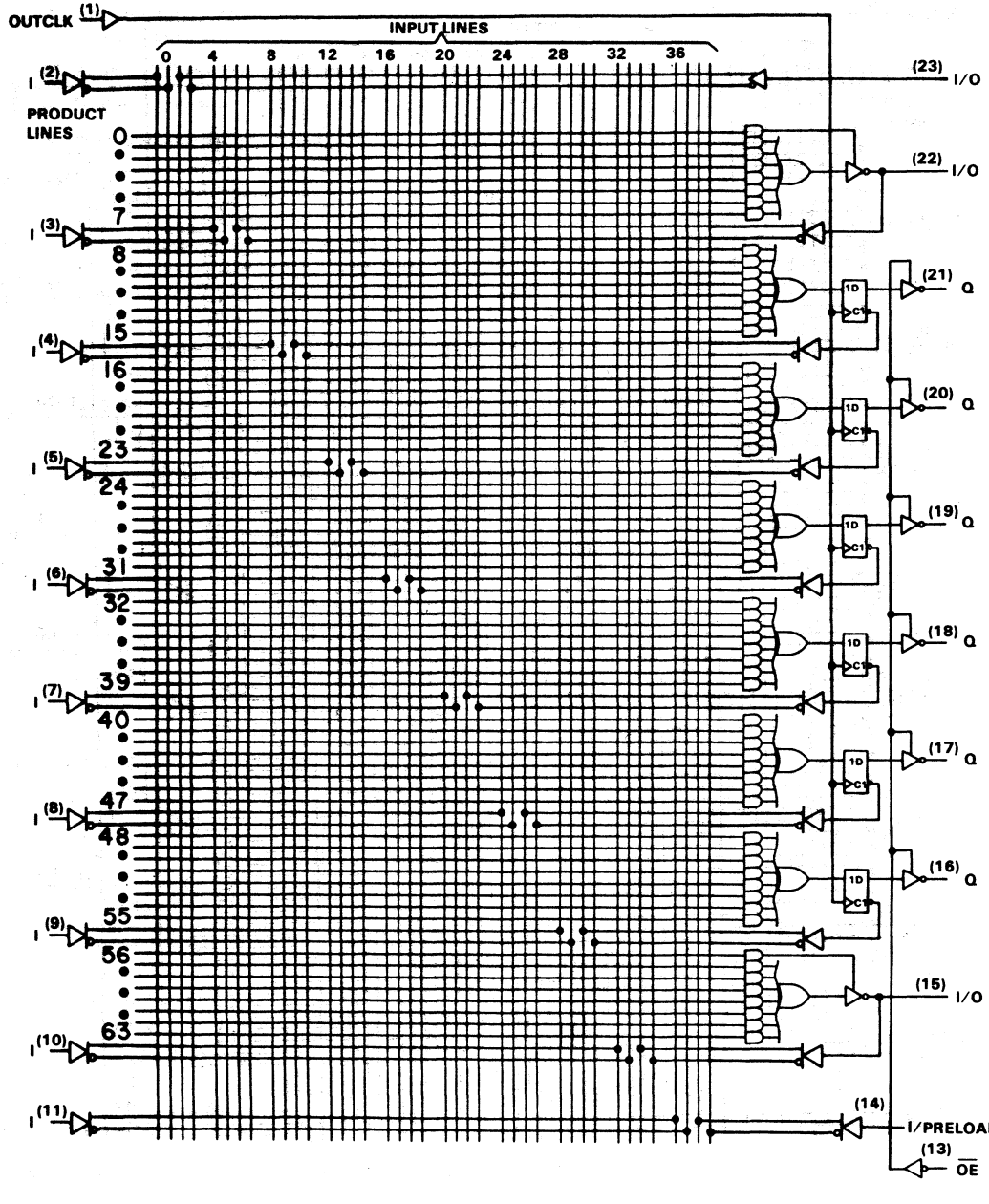
Array fuses are programmed using a linear select method. Each fuse can be opened by selecting the appropriate (one of 40) input line and then pulsing the correct (one of 64) product line. The levels for selecting input lines and product lines are shown in Tables 1 and 2.

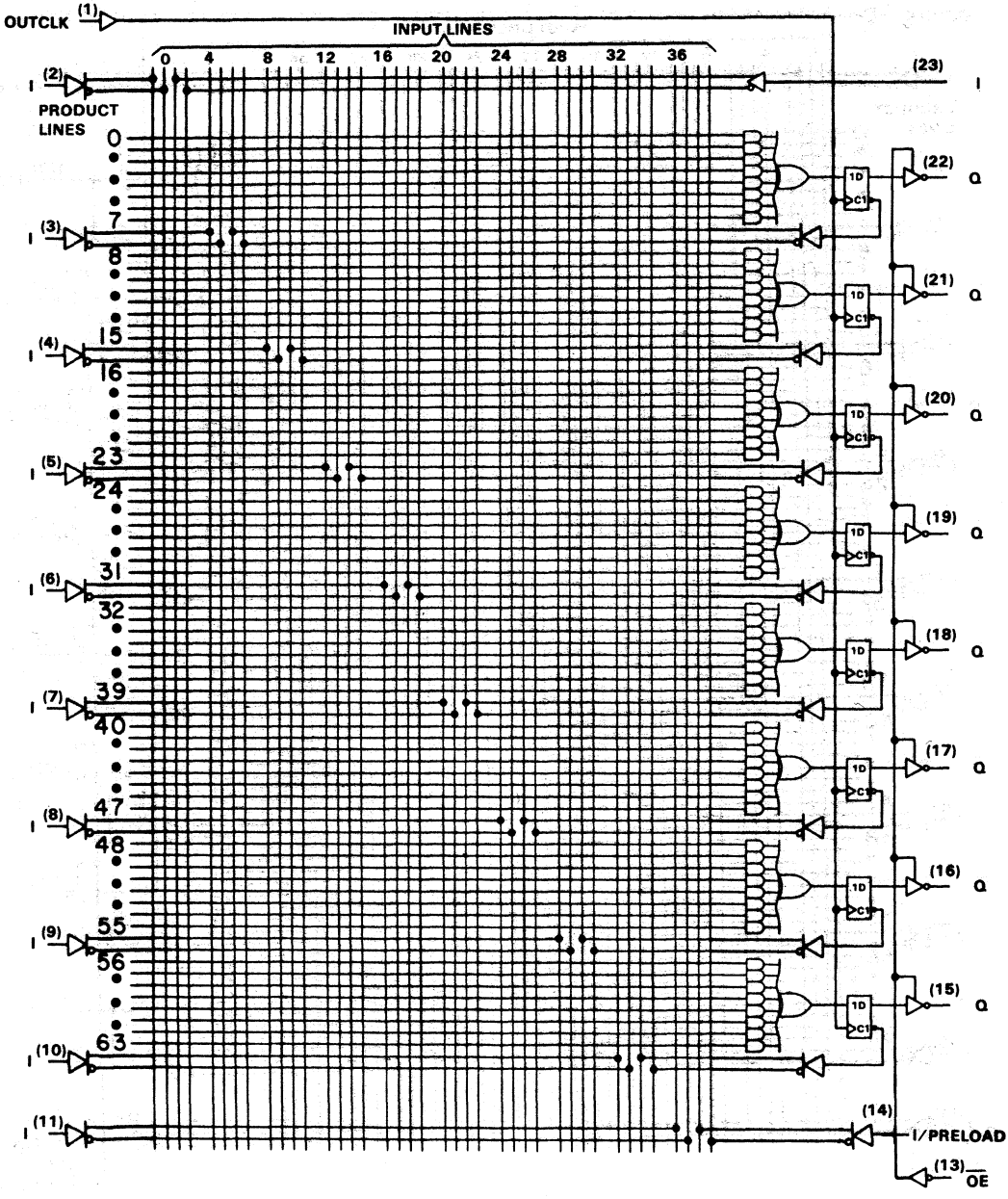
Step 1 — Raise PGM ENABLE to V_{IHH}.
Step 2 — Select an input line by applying appropriate levels to L/R and PI pins.
Step 3 — Begin selection of the output line with appropriate conditions on PA pins.
Step 4 — Raise V_{CC} to V_{IHH}.
Step 5 — Blow the fuse by pulsing the appropriate PO pin to V_{IHH} as shown in Table 2 for the product line.
Step 6 — Lower V_{CC} to 5 volts and pulse PGM VERIFY. The PO pin selected in Step 4 will be less than V_{OL} if the fuse is open.

Steps 1 thru 6 may be repeated if the verification does not indicate that the fuse was successfully programmed (blown), but no more than 4 times. Verification is possible only with the verify-protect fuse intact.


(1)
INPUT LINES
0 4 8 12 16 20 24 28 32 36
(2)
PRODUCT LINES
0
7
(3)
8
15
(4)
16
23
(5)
24
31
(6)
32
39
(7)
40
47
(8)
48
55
(9)
56
63
(10)
(11)
(23)
(22) O
(21) I/O
(20) I/O
(19) I/O
(18) I/O
(17) I/O
(16) I/O
(15) O
(14) I/PRELOAD
(13) I


OUTCLK (1)
INPUT LINES
0 4 8 12 16 20 24 28 32 36
(2) I
PRODUCT LINES 0
7
(3) I
8
15
(4) I
16
23
(5) I
24
31
(6) I
32
39
(7) I
40
47
(8) I
48
55
(9) I
56
63
(10) I
(11) I
(23) I
(22) I/O
(21) I/O
(20) Q
(19) Q
(18) Q
(17) Q
(16) I/O
(15) I/O
(14) I/PRELOAD
(13) OE
1D
C1


OUTCLK (1)
INPUT LINES
0 4 8 12 16 20 24 28 32 36
(2)
PRODUCT LINES
0
7
(3)
8
15
(4)
16
23
(5)
24
31
(6)
32
39
(7)
40
47
(8)
48
55
(9)
56
63
(10)
(11)
(23) I/O
(22) I/O
(21) Q
(20) Q
(19) Q
(18) Q
(17) Q
(16) Q
(15) I/O
(14) I/PRELOAD
(13) OE
1D
C1


OUTCLK
(1)
INPUT LINES
0
4
8
12
16
20
24
28
32
36
(2)
I
PRODUCT LINES
0
7
8
15
16
23
24
31
32
39
40
47
48
55
56
63
(3)
(4)
(5)
(6)
(7)
(8)
(9)
(10)
(11)
(23)
I
(22)
(21)
(20)
(19)
(18)
(17)
(16)
(15)
Q
1D
C1
(14)
I/PRELOAD
(13)
OE

TYPES SN54PL839, SN54PL840, SN74PL839, SN74PL840
14 X 32 X 6 FIELD-PROGRAMMABLE LOGIC ARRAYS

D2708, DECEMBER 1982—REVISED SEPTEMBER 1983

- **Input-to-Output Propagation Delay . . . 10 ns Typical**
- **24-Pin, 300-mil Slim Line Packages**
- **Power Dissipation . . . 650 mW Typical**
- **Programmable Output Polarity**

LOGIC FUNCTION

f(I) = P0 + P1 . . . P31 for polarity link intact
f(I) = $\overline{P0}$* $\overline{P1}$* . . . *$\overline{P31}$ for polarity link open
where P0 through P31 are product terms

description

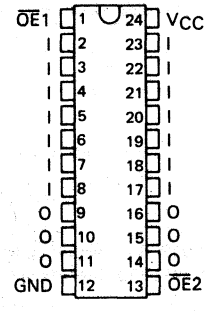
The 'PL839 (3-state outputs and the 'PL840 (open-collector outputs) are TTL field-programmable logic arrays containing 32 product terms (AND terms) and six sum terms (OR terms). Each of the six sum-of-products output functions can be programmed either high or low true. The true condition of each output function is activated by the programmed logical minterms of 14 input variables. The outputs are controlled by two chip-enable pins to allow output inhibit and expansion of terms.

These devices provide high-speed data-path logic replacement where several conventional SSI functions can be designed into a single package.

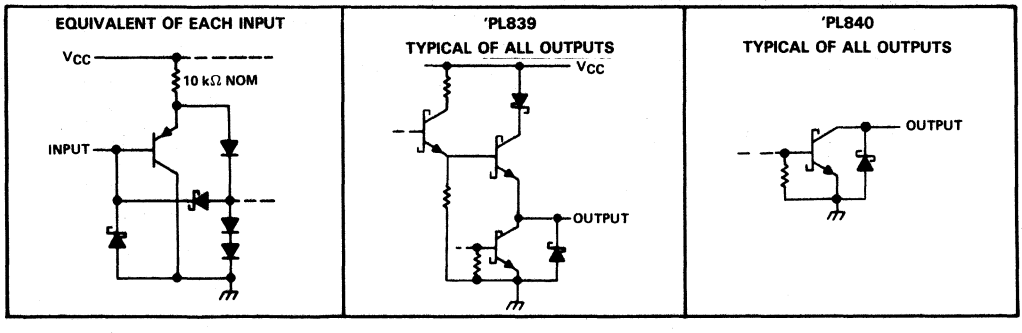
The SN54PL839 and SN54PL840 are characterized for operation over the full military temperature range of −55°C to 125°C. The NS74PL839 and SN74PL840 are characterized for operation from 0°C to 70°C.

pin assignments in operating mode (pin 1 is less than V_{IHH})

SN54PL' . . . JT PACKAGE
SN74PL' . . . NT PACKAGE
(TOP VIEW)



schematics of inputs and outputs



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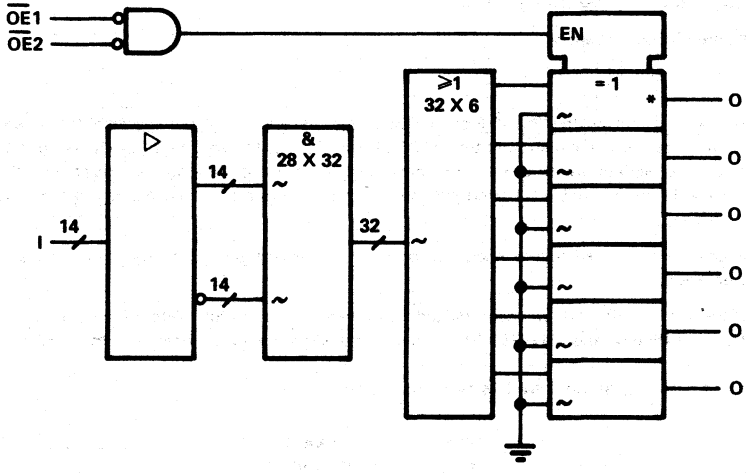
ADVANCE INFORMATION

This document contains information on a new product. Specifications are subject to change without notice.

functional block diagram (positive logic)



~ denotes fused inputs.
*'PL839 has 3-state (▽) outputs; 'PL840 has open-collector (Ω) outputs.

absolute maximum ratings

Supply Voltage, V_{CC}		7 V
Input Voltage		5.5 V
Off-State Output Voltage		5.5 V
Operating Free-air Temperature Range	SN54PL839, SN54PL840	−55°C to 125°C
	SN74PL839, SN74PL840	0°C to 70°C
Storage Temperature		−65°C to 150°C

recommended operating conditions

	SN54PL'			SN74PL'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			2			V
Low-level input voltage, V_{IL}			0.8			0.8	V
High-level output current, I_{OH}			−2			−3.2	mA
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		SN54PL'			SN74PL'			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = MIN,	I_{OH} = MAX	2.4	3.2		2.4	3		V
V_{OL}	V_{CC} = MIN,	I_{OL} = MAX		0.25	0.5		0.37	0.5	V
I_I	V_{CC} = MAX,	V_I = 5.5 V			0.1			0.1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
I_O§	V_{CC} = MAX,	V_O = 2.25 V	−30	−50	−112	−30	−50	−112	mA
I_{OZH}	V_{CC} = MAX,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = MAX,	V_O = 0.4 V			−20			−20	μA
I_{CC}	V_{CC} = MAX, $\overline{OE}$ inputs at V_{IH}	V_I = 0 V,		130	200		130	190	mA

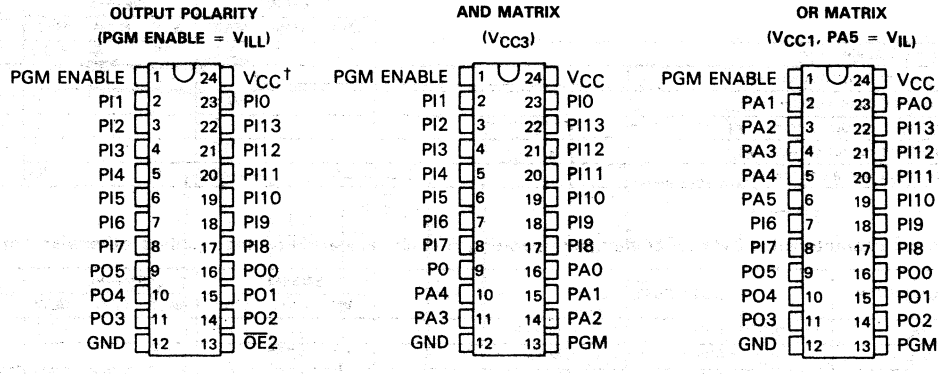
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit current, I_{OS}.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	SN54PL'			SN74PL'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{pd}	Input	Output	R_L = 500 to GND, C_L = 50 pF to GND		10	25		10	20	ns
t_{en}	Pin 1 or Pin 13	Output	R_{L1} = 500 to 7 V, R_{L2} = 500 to GND, C_L = 50 pF to GND		9	16		9	13	ns
t_{dis}					8	15		8	12	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

pin assignment in programming mode (pin 1 ≥ V_{IHH}) top views



†V_{CC} = V_{CC2} for program and V_{CC1} for verify

programming parameters, T_A = 25°C

PARAMETER		MEASURED AT	PROGRAMMING MODE	MIN	TYP	MAX	UNIT
V_{IHH}	Program high-level input voltage	PGM ENABLE	AND, OR	16.5	17	17.5	V
		PO pins	Polarity				
V_{ILL}	Program low-level input voltage	PGM ENABLE	Any	0		0.4	V
I_{IHH}	Program-level input current	PO pins	Polarity		100		mA
		PGM ENABLE	AND, OR		150		
V_{IX}	Program-level input voltage	PO0 thru PO5	Polarity	9.5	10	10.5	V
		PGM	AND, OR				
I_{IX}	Program-level input current	PI pins	AND		0.6	2	mA
		$\overline{OE2}$	Polarity			5	
		PO0 thru PO5	OR		5	10	
V_{CC1}	Programming supply voltage	V_{CC}	OR	8.5	8.75	9	V
I_{CC1}	Programming supply current	V_{CC}	OR		250	400	mA
V_{CC2}	Programming supply voltage	V_{CC}	Polarity		0	0.4	V
V_{CC3}	Programming supply voltage	V_{CC}	AND	4.75	5	5.25	V
V_{IH}	High-level input voltage	Any	Any	2			V
V_{IL}	Low-level input voltage	Any	Any	0		0.8	V
V_{OH}	High-level output voltage	Any	Any	2.4	3.2		V
V_{OL}	Low-level output voltage	Any	Any		0.25	0.5	V
t_w	Program pulse duration	PO0 thru PO5	Polarity		50	1000	μs
		PGM	AND, OR				
	Program pulse duty cycle	PO0 thru PO5	Polarity		10	50	%
		PGM	AND, OR				
t_d	Delay time	Any	Any	10			μs
t_r	Rise time	Any	Any		25		μs

PROGRAMMING PROCEDURE

OUTPUT POLARITY

Program

Load all output pins with a 10-kΩ resistor to 5 V and set pin 12 (GND) to 0 V. Program the output polarity before programming either the AND matrix or the OR matrix. An unprogrammed device has all six outputs noninverting. When the polarity link of an output is opened, the output function becomes inverting. Program one output at a time as follows:

Step 1: Set PGM ENABLE (pin 1) to V_{ILL}.
Step 2: Set V_{CC} (pin 24) to V_{CC2}; set $\overline{OE2}$ (pin 13) to V_{IH} and PI0 through PI13 to V_{IX}.
Step 3: Ramp the appropriate output to V_{IHH} and remove after t_w.
Step 4: Repeat step 3 for each output to be programmed low.

Verify

Step 1: Set PGM ENABLE (pin 1) to V_{ILL}; set V_{CC} (pin 24) to V_{CC2}; set PI0 through PI13 to V_{IX}.
Step 2: Wait t_d and raise V_{CC} (pin 24) to V_{CC1}.
Step 3: Enable the device by applying V_{IL} to $\overline{OE2}$ (pin 13).
Step 4: Sense the logic state of all six outputs. An output at V_{OH} has been programmed to be inverting, while an output at V_{OL} has remained noninverting.
Step 5: Remove V_{CC1}.

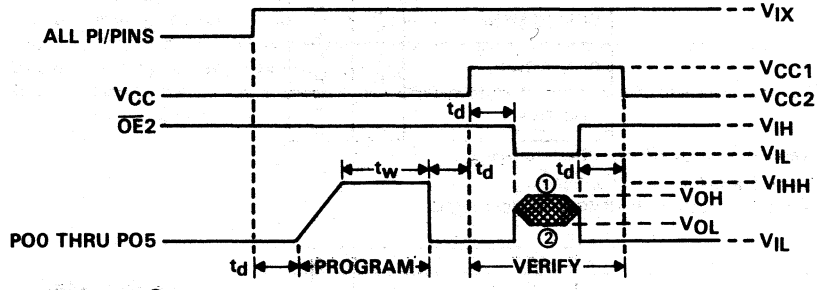


FIGURE 1 — OUTPUT POLARITY PROGRAMMING WAVEFORMS

AND MATRIX

Program

Program the output polarity before programming either the AND matrix or the OR matrix. Load all output pins with a 10-kΩ resistor to 5 V and set pin 12 (GND) to V_{IL}. Program each input separately for each product term, one fuse at a time. Unused terms do not require fusing, however, all input variables of a selected product term must be programmed either true, complement, or don't care (both links are blown), as follows:

Step 1: Set PGM ENABLE (pin 1) to V_{ILL}; set V_{CC} (pin 24) to V_{CC3}.
Step 2: Disable all outputs by applying V_{IH} to PGM (pin 13).
Step 3: Disable all inputs by applying V_{IX} to the I inputs.
Step 4: Address the product term to be programmed (0 through 31) by applying its binary code (V_{IH} for a high and V_{IL} for a low) to outputs PA0 through PA4 with PA0 as the least significant bit.

PROGRAMMING PROCEDURE

Step 5: Lower the voltage on the first input to V_{IH} for a true, or to V_{IL} for the complement.
Step 6: After t_d, raise PGM ENABLE to V_{IHH}.
Step 7: After additional t_d, pulse the PGM input to V_{IX} for t_w.
Step 8: After additional t_d delay, lower PGM ENABLE to V_{ILL}.
Step 9: Disable programmed input by raising it back to V_{IX}.
Step 10: Repeat steps 5 through 9 for each input.
Step 11: Repeat steps 4 through 10 for each product term.

Verify

Step 1: Set PGM ENABLE (pin 1) to V_{ILL}; set V_{CC} (pin 24) to V_{CC3}.
Step 2: Enable PO output by setting PGM to V_{IX}.
Step 3: Disable all inputs by applying V_{IX} to the I inputs.
Step 4: Address the product term to be verified (0 through 31) by applying its binary code on outputs PA0 through PA4.
Step 5: Lower the input voltage on the first input to V_{IH} and check the logic level of output PO, then lower the same input to V_{IL} and again check the level of PO. The input variable state contained in the product term is determined from the following table. Two tests are required to verify the programmed state of each variable.

STATE	I	PO
TRUE	L	L
	H	H
COMPLEMENT	L	H
	H	L
DON'T CARE	L	H
	H	H
INACTIVE	L	L
	H	L

Step 6: Disable verified input by raising it back to V_{IX}.
Step 7: Repeat steps 5 and 6 for all other inputs.
Step 8: Repeat steps 4 through 7 for all other product terms.

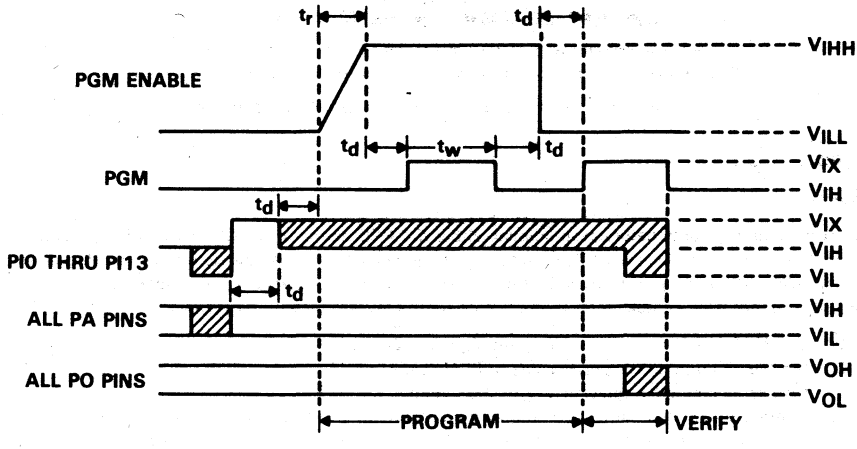


FIGURE 2– AND MATRIX PROGRAMMING WAVEFORMS

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PROGRAMMING PROCEDURE

OR MATRIX

Program

Program the output polarity before programming either the AND matrix or the OR matrix. Load all output pins with a 10-kΩ resistor to 5 V and set pin 12 (GND) to 0 V. If the product term is contained in the output function, no fusing is required. Unwanted terms are deleted by programming one at a time, as follows:

Step 1: Set PGM ENABLE (pin 1) to V_{ILL}. Disable the outputs by setting PGM (pin 13) to V_{IH}. Set V_{CC} to V_{CC3}. Set PI6 through PI13 and PA0 through PA5 to V_{IX}.
Step 2: Wait t_d and raise V_{CC} (pin 24) to the program level, V_{CC1}.
Step 3: Use the inputs PA0 through PA5 to address the product term (0 through 31) that is to be removed by applying the corresponding binary code with input PA0 as the least significant bit.
Step 4: Raise the output pin to V_{IX}.
Step 5: Wait t_d, then raise PGM ENABLE to V_{IHH}.
Step 6: Wait t_d, then pulse PGM to V_{IX} for a period of t_p.
Step 7: Wait t_d, then lower PGM ENABLE to V_{ILL}.
Step 8: Wait t_d, then remove V_{IX} from output pin.
Step 9: Repeat steps 4 through 8 for all other output functions.
Step 10: Repeat steps 3 through 9 for all other product terms.
Step 11: Lower V_{CC} to V_{CC3}.

Verify

Step 1: Set PGM ENABLE (pin 1) to V_{ILL}. Disable the outputs by setting PGM (pin 13) to V_{IH}. Set V_{CC} to V_{CC3}. Set PI6 through PI13 and PA0 through PA5 to V_{IX}.
Step 2: Wait t_d and set V_{CC} (pin 24) to the verify level, V_{CC1}.
Step 3: Address the product term to be verified (0 through 31) by applying its binary code to inputs PA0 through PA5.
Step 4: Wait t_d, and set PGM (pin 13) to V_{IL}.
Step 5: Monitor the state of all six outputs (PO0 through PO5) and determine the status of the OR matrix from the following table:

OUTPUT		OR FUSE LINK
ACTIVE HIGH	ACTIVE LOW	
L	H	FUSED
H	L	PRESENT

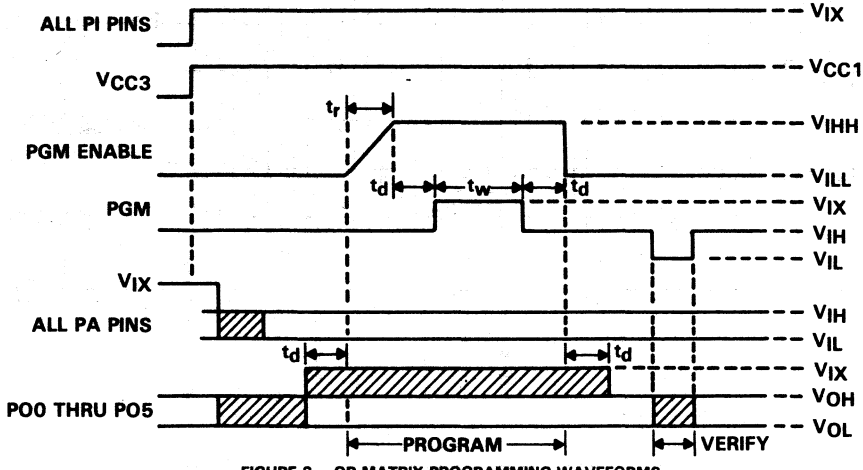
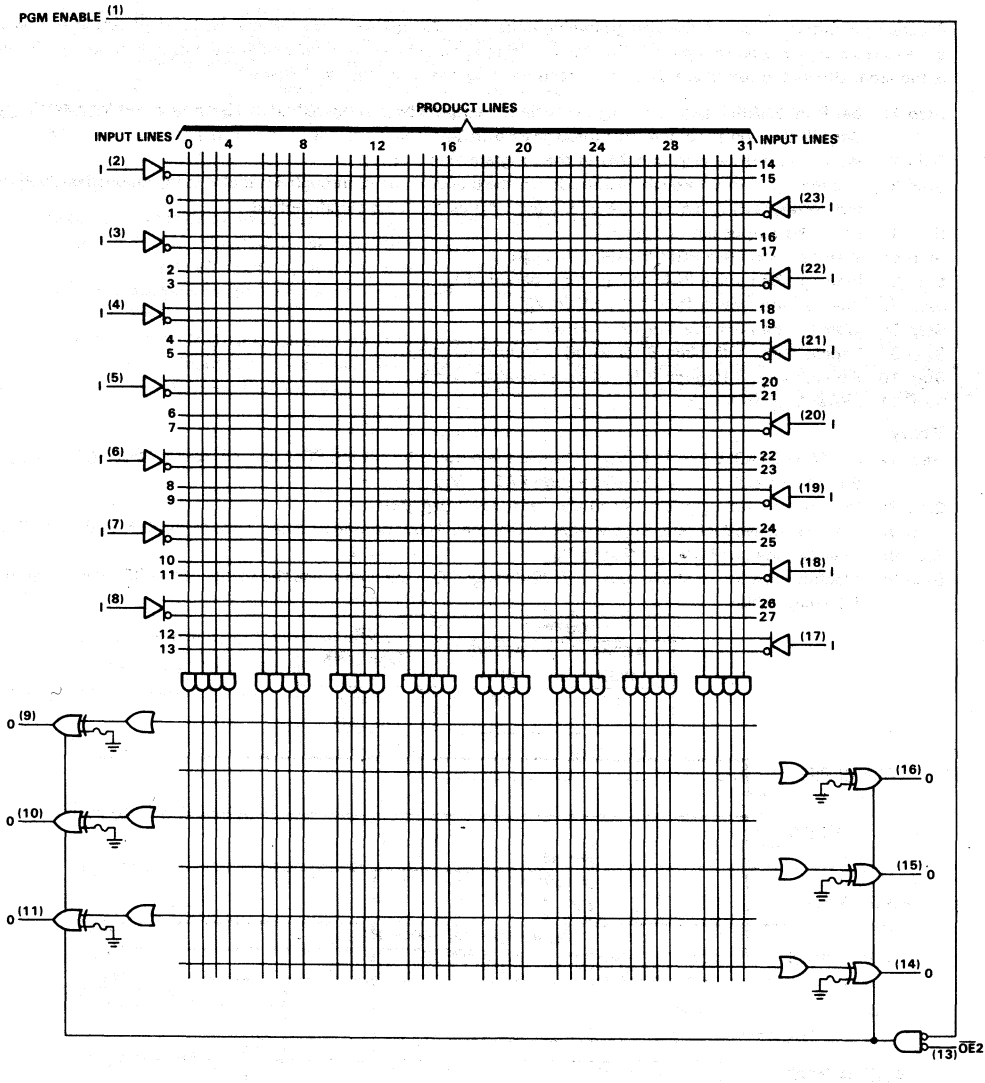


FIGURE 3— OR MATRIX PROGRAMMING WAVEFORMS

LOGIC DIAGRAM



TYPES SN54PLR19L8, SN54PLR19R4, SN54PLR19R6, SN54PLR19R8 SN74PLR19L8, SN74PLR19R4, SN74PLR19R6, SN74PLR19R8 REGISTERED-INPUT FIXED-OR ARRAYS

D2709, DECEMBER 1982—REVISED SEPTEMBER 1983

- Standard 24-Pin, 300-mil Packages
- Output Registers Have Preload Capability
- Output Registers Automatically Clear During Power-Up
- Choice of Operating Speeds
  - —1 Parts . . . 30 MHz Max, Standard power
  - —2 Parts . . . 20 MHz Max, Half power

DEVICE	I/D INPUTS	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
'PLR19L8	11	2	2	0	6
'PLR19R4	11	0	0	4 (3-state buffers)	4
'PLR19R6	11	0	0	6 (3-state buffers)	2
'PLR19R4	11	0	0	8 (3-state buffers)	0

description

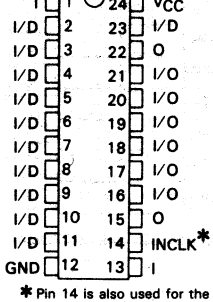
These fixed-OR arrays with eleven data inputs feature input registers that can be used as they are or be programmed into buffers. Some outputs of the 'PL19R8, 'PL19R6, and 'PL19R4 have registers that can be loaded from the I/O pins by a preload procedure, while others are I/O ports and standard 3-state outputs. All the outputs are automatically set to a low level when power is applied. The —1 and —2 parts offer a choice of operating frequency, switching times, and power dissipation.

The SN54PLR19' is characterized for operation over the full military temperature range of —55°C to 125°C. The SN74PLR19' is characterized for operation from 0°C to 70°C.

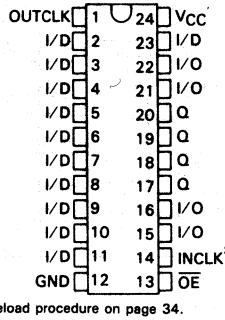
pin assignments in operating mode (voltages at pins 1 and 13 less than V_{IHH})

SN54' ... JT PACKAGE
SN74' ... NT PACKAGE
(TOP VIEW)

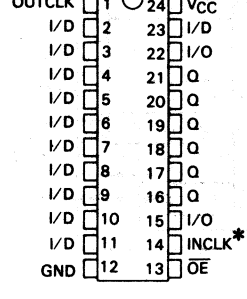
'PLR19L8



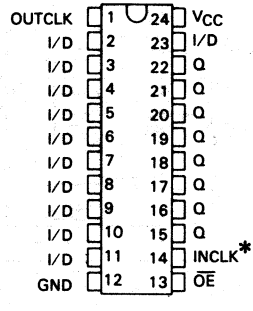
'PLR19R4



'PLR19R6

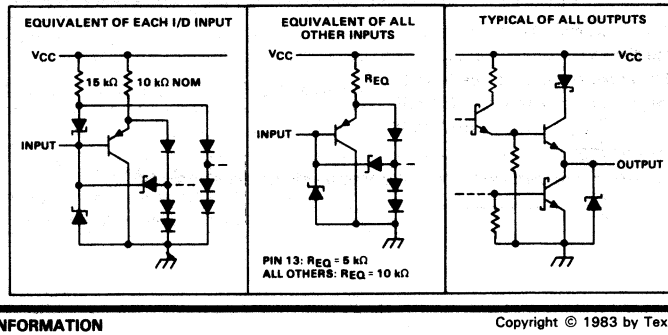


'PLR19R8



* Pin 14 is also used for the preload procedure on page 34.

schematics of inputs and outputs

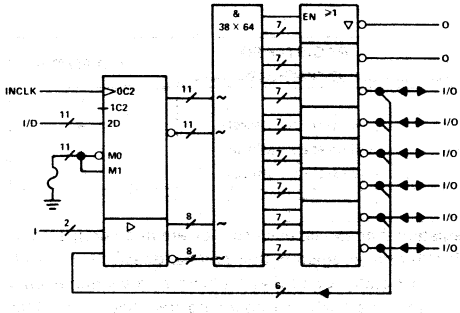


ADVANCE INFORMATION

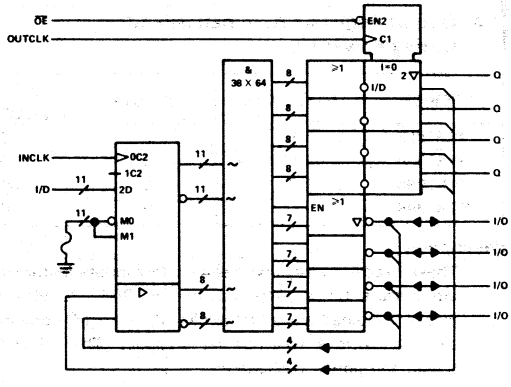
This document contains information on a new product. Specifications are subject to change without notice.

functional block diagrams (positive logic)

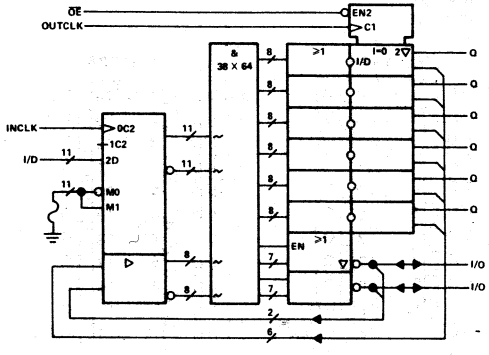
'PLR19L8



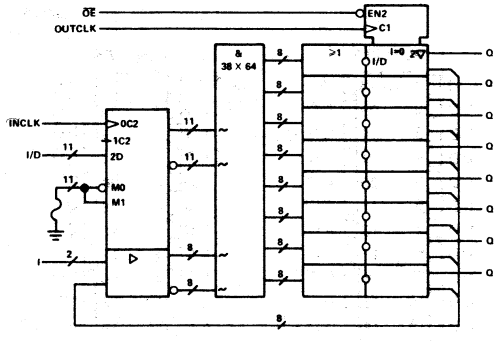
'PLR19R4



'PLR19R6



'PLR19R8



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage (see Note 1) ..... 5.5 V
Voltage applied to a disabled output (see Note 1) ..... 5.5 V
Operating free-air temperature range: SN54PLR' ..... −55°C to 125°C
SN74PLR' ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during a preload cycle.

recommended operating conditions

		SN54PLR19'			SN74PLR19'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2		5.5	2		5.5	V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−3.2	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended free-air operating temperature range

PARAMETER		TEST CONDITIONS†		SN54PLR19'			SN74PLR19'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = MIN,	I_{OH} = MAX	2.4	3.2		2.4	3.3		V
V_{OL}		V_{CC} = MIN,	I_{OL} = MAX		0.25	0.4		0.35	0.5	V
I_{OZH}	Outputs	V_{CC} = MAX,	V_{IH} = 2.7 V			20			20	μA
	I/O ports					100			100	
I_{OZL}	Outputs	V_{CC} = MAX,	V_{IH} = 0.4 V			−20			−20	μA
	I/O ports					−250			−250	
I_I	OE Input	V_{CC} = MAX,	V_I = 5.5 V			0.2			0.2	mA
	I/D Inputs					0.1			0.1	
	All others					0.1			0.1	
I_{IH}	OE Input	V_{CC} = MAX,	V_I = 2.7 V			40			40	μA
	I/D Inputs					20			0.1	
	All others					20			0.1	
I_{IL}	OE Input	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
	I/D Inputs					−0.6			−0.6	
	All others					−0.2			−0.2	
I_O§		V_{CC} = MAX,	V_O = 2.25 V	−30		−125	−30		−125	mA
I_{CC}	−1 Parts	V_{CC} = MAX,	V_I = 0 V,		150	200		150	200	mA
	−2 Parts	Outputs open			75	100		75	100	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half the true short-circuit current, I_{OS}.

input timing requirements

		MIN	MAX	UNIT
f_{clock}	Clock frequency	0	40	MHz
t_w	Clock pulse duration, clock high or low	10		ns
t_{su}	Setup time, I/D input before INCLK↑	12		ns
t_h	Hold time, I/D input before INCLK↑	0		ns

'PLR19R4, 'PLR19R6, 'PLR19R8 timing requirements

		MIN	MAX	UNIT
f_{clock}	Clock frequency	0	30	MHz
t_w	Clock pulse duration, clock high or low	12		ns
t_{su}	Setup time, input or feedback before OUTCLK↑	15		ns
t_h	Hold time, input or feedback before OUTCLK↑	0		ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	INPUT MODE	TEST CONDITIONS	−1 PARTS			−2 PARTS			UNIT
					MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}			Either	R_L = 500Ω, C_L = 50 pF	30			20			MHz
t_{pd}	I, I/O	I/O, O	Either			16			25		ns
t_{pd}	OUTCLK↑	Q	Either			12			20		ns
t_{en}	$\overline{OE}$↓	Q	Either			8			15		ns
t_{dis}	$\overline{OE}$↑	Q	Either			6			12		ns
t_{pd}	INCLK↑	I/O, O	Registered			23			32		ns
t_{en}	INCLK↑	I/O, O, Q	Registered			25			35		ns
t_{dis}	INCLK↑	I/O, O, Q	Registered			20			30		ns
t_{pd}	I/D	I/O, O	Buffered			20			30		ns
t_{en}	I/D, I/O	I/O	Buffered			22			32		ns
t_{dis}	I/D, I/O	I/O	Buffered			17			26		ns

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

PRELOAD PROCEDURES

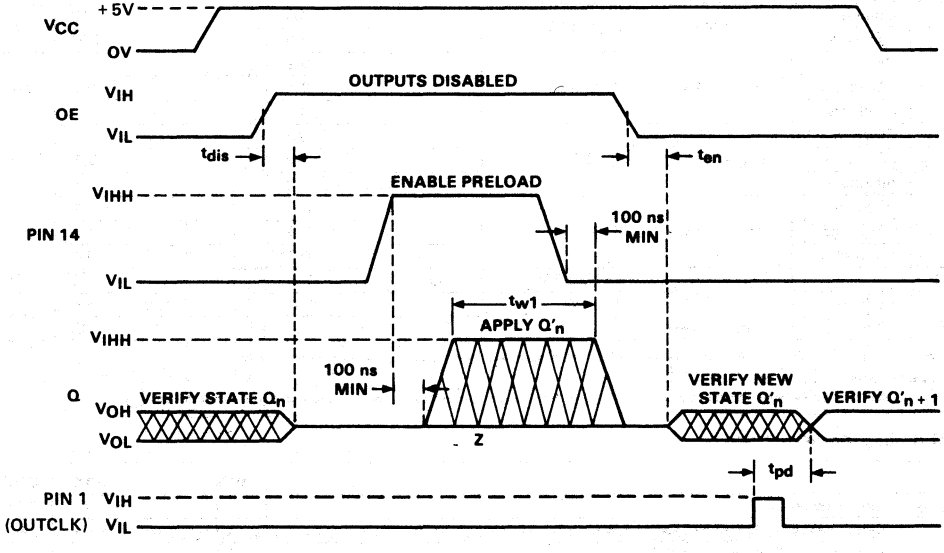


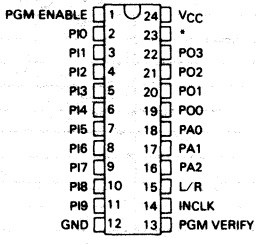
FIGURE 1—PRELOAD WAVEFORMS

preload procedure for registered outputs

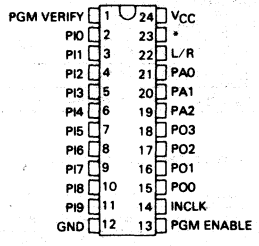
Step 1	Pin 13 to V_{IH}, Pin 1 to V_{IL}, and V_{CC} to 5 volts.
Step 2	Pin 14 to V_{IHH}.
Step 3	Apply an open circuit for a low and V_{IHH} for a high at the Q outputs.
Step 4	Pin 14 to V_{IL}.
Step 5	Remove the voltages applied to the outputs.
Step 6	Pin 13 to V_{IL}.
Step 7	Check the output states to verify preload.

pin assignments in programming mode (PGM ENABLE, pin 1 or 13, at V_{IHH})

PRODUCT TERMS 0 THRU 31
(TOP VIEW)



PRODUCT TERMS 32 THRU 63
(TOP VIEW)



*No programming function. Make no connection.

TABLE 1—INPUT LINE SELECT

INPUT LINE NUMBER	PIN NAME										
	PI9	PI8	PI7	PI6	PI5	PI4	PI3	PI2	PI1	PI0	L/R
0	HH	HH	HH	HH	HH	HH	HH	HH	HH	L	Z
1	HH	HH	HH	HH	HH	HH	HH	HH	HH	H	Z
2	HH	HH	HH	HH	HH	HH	HH	HH	HH	L	HH
3	HH	HH	HH	HH	HH	HH	HH	HH	HH	H	HH
4	HH	HH	HH	HH	HH	HH	HH	HH	L	HH	Z
5	HH	HH	HH	HH	HH	HH	HH	HH	H	HH	Z
6	HH	HH	HH	HH	HH	HH	HH	HH	L	HH	HH
7	HH	HH	HH	HH	HH	HH	HH	HH	H	HH	HH
8	HH	HH	HH	HH	HH	HH	HH	L	HH	HH	Z
9	HH	HH	HH	HH	HH	HH	HH	H	HH	HH	Z
10	HH	HH	HH	HH	HH	HH	HH	L	HH	HH	HH
11	HH	HH	HH	HH	HH	HH	HH	H	HH	HH	HH
12	HH	HH	HH	HH	HH	HH	L	HH	HH	HH	Z
13	HH	HH	HH	HH	HH	HH	H	HH	HH	HH	Z
14	HH	HH	HH	HH	HH	HH	L	HH	HH	HH	HH
15	HH	HH	HH	HH	HH	HH	H	HH	HH	HH	HH
16	HH	HH	HH	HH	HH	L	HH	HH	HH	HH	Z
17	HH	HH	HH	HH	HH	H	HH	HH	HH	HH	Z
18	HH	HH	HH	HH	HH	L	HH	HH	HH	HH	HH
19	HH	HH	HH	HH	HH	H	HH	HH	HH	HH	HH
20	HH	HH	HH	HH	L	HH	HH	HH	HH	HH	Z
21	HH	HH	HH	HH	H	HH	HH	HH	HH	HH	Z
22	HH	HH	HH	HH	L	HH	HH	HH	HH	HH	HH
23	HH	HH	HH	HH	H	HH	HH	HH	HH	HH	HH
24	HH	HH	HH	L	HH	HH	HH	HH	HH	HH	Z
25	HH	HH	HH	H	HH	HH	HH	HH	HH	HH	Z
26	HH	HH	HH	L	HH	HH	HH	HH	HH	HH	HH
27	HH	HH	HH	H	HH	HH	HH	HH	HH	HH	HH
28	HH	HH	L	HH	HH	HH	HH	HH	HH	HH	Z
29	HH	HH	H	HH	HH	HH	HH	HH	HH	HH	Z
30	HH	HH	L	HH	HH	HH	HH	HH	HH	HH	HH
31	HH	HH	H	HH	HH	HH	HH	HH	HH	HH	HH
32	HH	L	HH	HH	HH	HH	HH	HH	HH	HH	Z
33	HH	H	HH	HH	HH	HH	HH	HH	HH	HH	Z
34	HH	L	HH	HH	HH	HH	HH	HH	HH	HH	HH
35	HH	H	HH	HH	HH	HH	HH	HH	HH	HH	HH
36	L	HH	HH	HH	HH	HH	HH	HH	HH	HH	Z
37	H	HH	HH	HH	HH	HH	HH	HH	HH	HH	Z
38	L	HH	HH	HH	HH	HH	HH	HH	HH	HH	HH
39	H	HH	HH	HH	HH	HH	HH	HH	HH	HH	HH

TABLE 2—PRODUCT LINE SELECT

PRODUCT LINE NUMBER	PIN NAME						
	PO0	PO1	PO2	PO3	PA2	PA1	PA0
0, 32	Z	Z	Z	HH	Z	Z	Z
1, 33	Z	Z	Z	HH	Z	Z	HH
2, 34	Z	Z	Z	HH	Z	HH	Z
3, 35	Z	Z	Z	HH	Z	HH	HH
4, 36	Z	Z	Z	HH	HH	Z	Z
5, 37	Z	Z	Z	HH	HH	Z	HH
6, 38	Z	Z	Z	HH	HH	HH	Z
7, 39	Z	Z	Z	HH	HH	HH	HH
8, 40	Z	Z	HH	Z	Z	Z	Z
9, 41	Z	Z	HH	Z	Z	Z	HH
10, 42	Z	Z	HH	Z	Z	HH	Z
11, 43	Z	Z	HH	Z	Z	HH	HH
12, 44	Z	Z	HH	Z	HH	Z	Z
13, 45	Z	Z	HH	Z	HH	Z	HH
14, 46	Z	Z	HH	Z	HH	HH	Z
15, 47	Z	Z	HH	Z	HH	HH	HH
16, 48	Z	HH	Z	Z	Z	Z	Z
17, 49	Z	HH	Z	Z	Z	Z	HH
18, 50	Z	HH	Z	Z	Z	HH	Z
19, 51	Z	HH	Z	Z	Z	HH	HH
20, 52	Z	HH	Z	Z	HH	Z	Z
21, 53	Z	HH	Z	Z	HH	Z	HH
22, 54	Z	HH	Z	Z	HH	HH	Z
23, 55	Z	HH	Z	Z	HH	HH	HH
24, 56	HH	Z	Z	Z	Z	Z	Z
25, 57	HH	Z	Z	Z	Z	Z	HH
26, 58	HH	Z	Z	Z	Z	HH	Z
27, 59	HH	Z	Z	Z	Z	HH	HH
28, 60	HH	Z	Z	Z	HH	Z	Z
29, 61	HH	Z	Z	Z	HH	Z	HH
30, 62	HH	Z	Z	Z	HH	HH	Z
31, 63	HH	Z	Z	Z	HH	HH	HH

L = V_{IL}, H = V_{IH}, HH = V_{IHH}, Z = high impedance (e.g., 10 kΩ to 5V)

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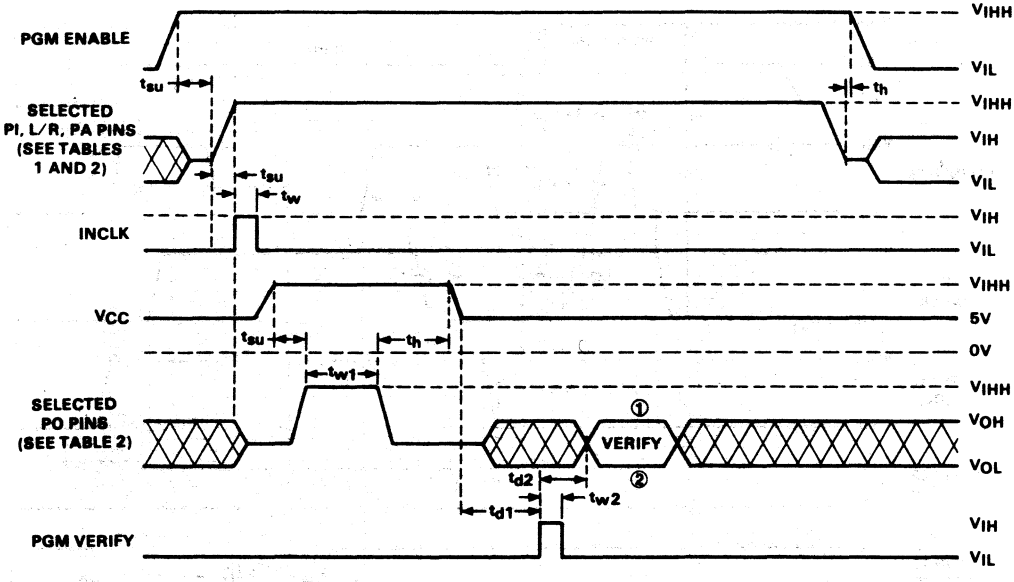
programming parameters, T_A = 25°C

			MIN	NOM	MAX	UNIT
V_{CC}	Verify-level supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
V_{OH}	High-level output voltage				5.5	V
V_{IHH}	Program-pulse input voltage		10.25	10.5	10.75	V
I_{IHH}	Program-pulse input current	PO			50	mA
		PGM ENABLE, L/R			25	
		PI, PA			5	
		V_{CC}			400	
t_{w1}	Program-pulse duration at PO or I/D pins		10		50	µs
t_{w2}	Pulse duration at PGM VERIFY and INCLK		100			ns
t_{su}	Setup time		100			ns
t_h	Hold time		100			ns
t_{d1}	Delay time from V_{CC} to 5 V to PGM VERIFY ↑		100			µs
t_{d2}	Delay time from PGM VERIFY ↑ to verification of output		200			ns
t_{d3}	Delay time		100			ns
	Input voltage at pins 1 and 13 to open verify-protect (security) fuse		20	21	22	V
	Input current to open verify-protect (security) fuse				400	mA
	Pulse duration to open verify-protect (security) fuse		20		50	ms



① A high level during the verify interval indicates that programming has not been successful.

② A low level during the verify interval indicates that programming ha been successful.

FIGURE 2 — PROGRAMMING WAVEFORMS FOR ARRAY FUSES

programming procedure for array fuses

Array fuses are programmed using a linear select method. Each fuse can be opened by selecting the appropriate (one of 40) input line and then pulsing the correct (one of 64) product line. The levels for selecting input lines and product lines are shown in Tables 1 and 2.

Step 1	Raise PGM ENABLE to V_{IHH}.
Step 2	Select an input line by applying appropriate levels to L/R and PI pins.
Step 3	Begin selection of the output line with appropriate conditions on PA pins.
Step 4	Pulse INCLK to V_{IH}.
Step 5	Raise V_{CC} to V_{IHH}.
Step 6	Blow the fuse by pulsing the appropriate PO pin to V_{IHH} as shown in Table 2 for the product line.
Step 7	Return V_{CC} to 5 volts and pulse PGM VERIFY. The PO pin selected in Step 4 will be less than V_{OL} if the fuse is open.

Steps 1 thru 7 may be repeated if the verification does not indicate that the fuse was successfully programmed (blown), but no more than 4 times. Verification is possible only with the verify-protect fuse intact.

To prevent further verification, two last fuses may be blown by raising pin 1 and pin 13 to 21 volts ±1 volt. V_{CC} is required to be at 0 during this operation.

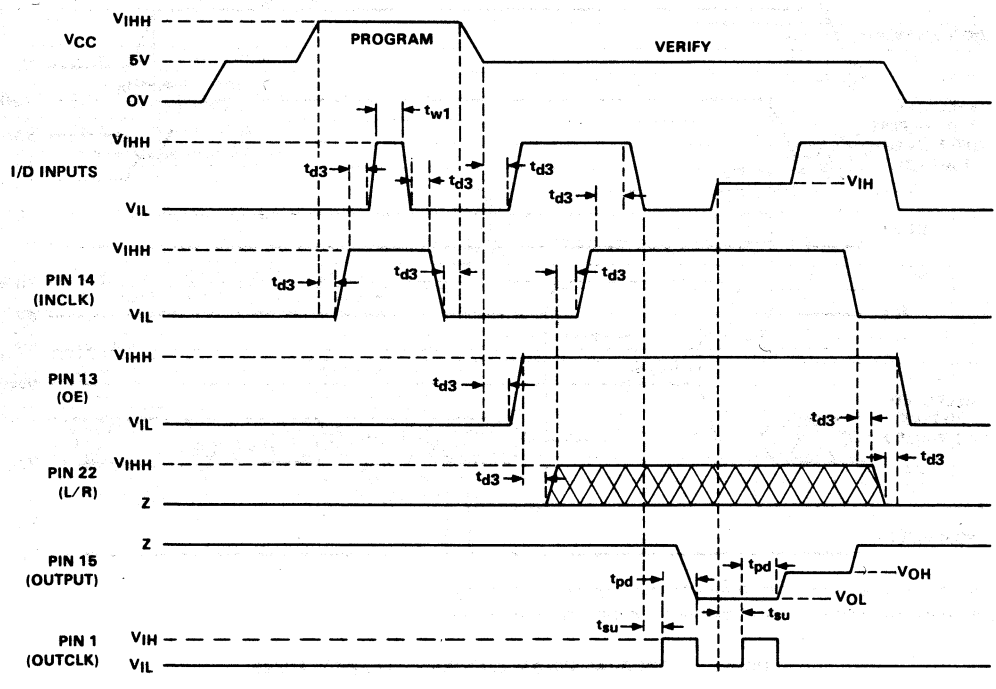
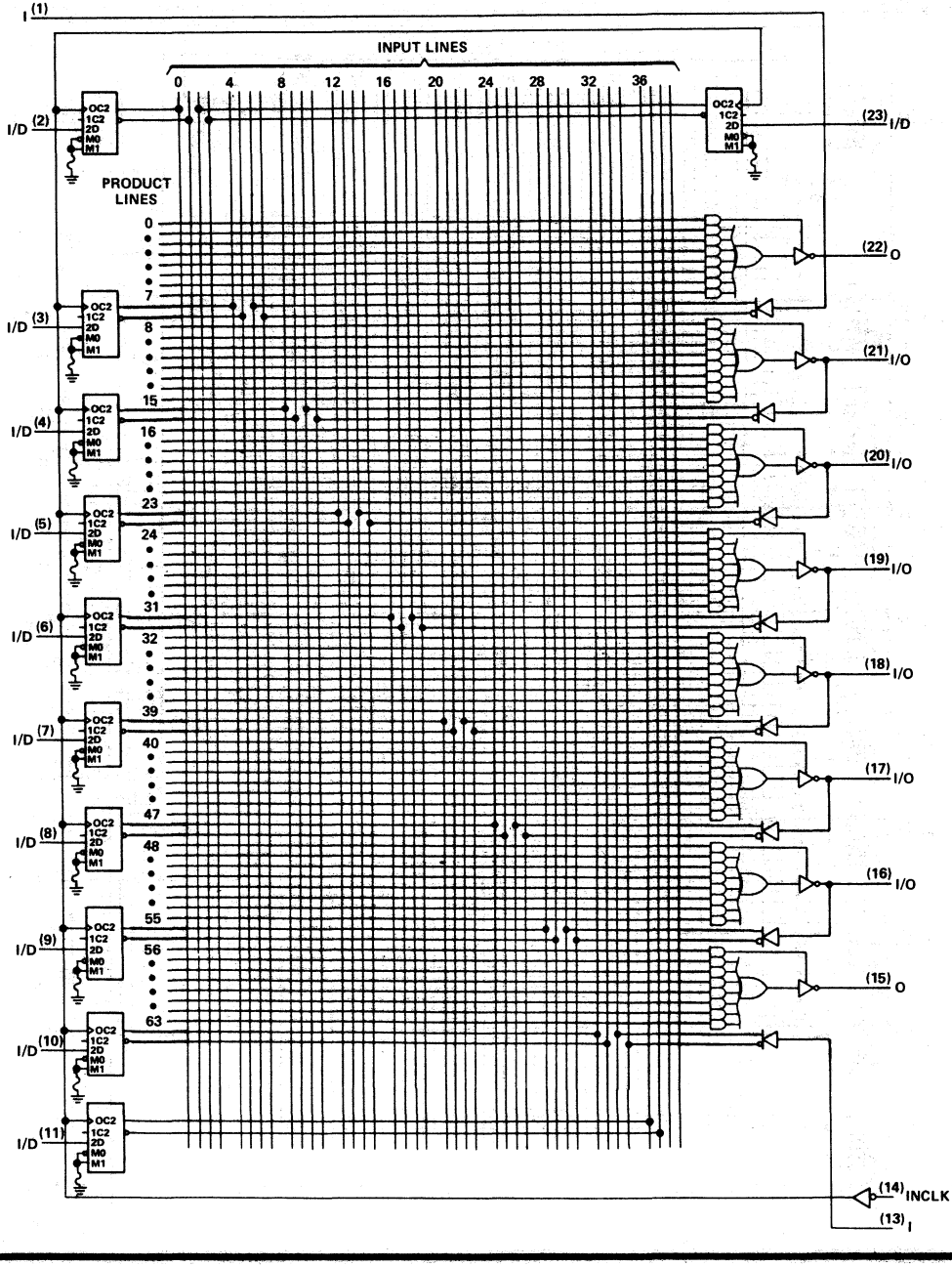


FIGURE 3 — ARCHITECTURAL FUSE PROGRAMMING WAVEFORMS

programming procedure for architectural fuses (see Note 2)

Step 1	Apply low levels to all I/D pins and 5 volts to the V_{CC} pin.
Step 2	Raise V_{CC} pin to V_{IHH}.
Step 3	Raise INCLK pin to V_{IHH}.
Step 4	To program a D input pin into an I input pin pulse the selected pin to V_{IHH}.
Step 5	Lower INCLK to V_{IL} and V_{CC} to 5 volts.
Step 6	Raise pin 13 and all I/D input pins to V_{IHH}.
Step 7	Set pin 22 to Z to select pins 2 thru 11 or set pin 22 to V_{IHH} to select pin 23.
Step 8	Raise INCLK to V_{IHH}.
Step 9	To verify that fuse has been blown, pulse selected I pin from V_{IHH} to V_{IL}, then to V_{IH} and back to V_{IHH} while clocking pin 1. If output at pin 15 follows the I input the fuse has been blown.
Step 10	Repeat above steps 1 thru 9 for each D input to be programmed into an I input.

NOTE 2: Refer to pin assignments in operating mode for programming selected I/D pins from D inputs to I inputs.


I (1)
INPUT LINES
0 4 8 12 16 20 24 28 32 36
I/D (2)
PRODUCT LINES
0
7
I/D (3)
8
15
I/D (4)
16
23
I/D (5)
24
31
I/D (6)
32
39
I/D (7)
40
47
I/D (8)
48
55
I/D (9)
56
63
I/D (10)
I/D (11)
OC2
1C2
2D
M0
M1
(23) I/D
(22) O
(21) I/O
(20) I/O
(19) I/O
(18) I/O
(17) I/O
(16) I/O
(15) O
(14) INCLK
(13) I

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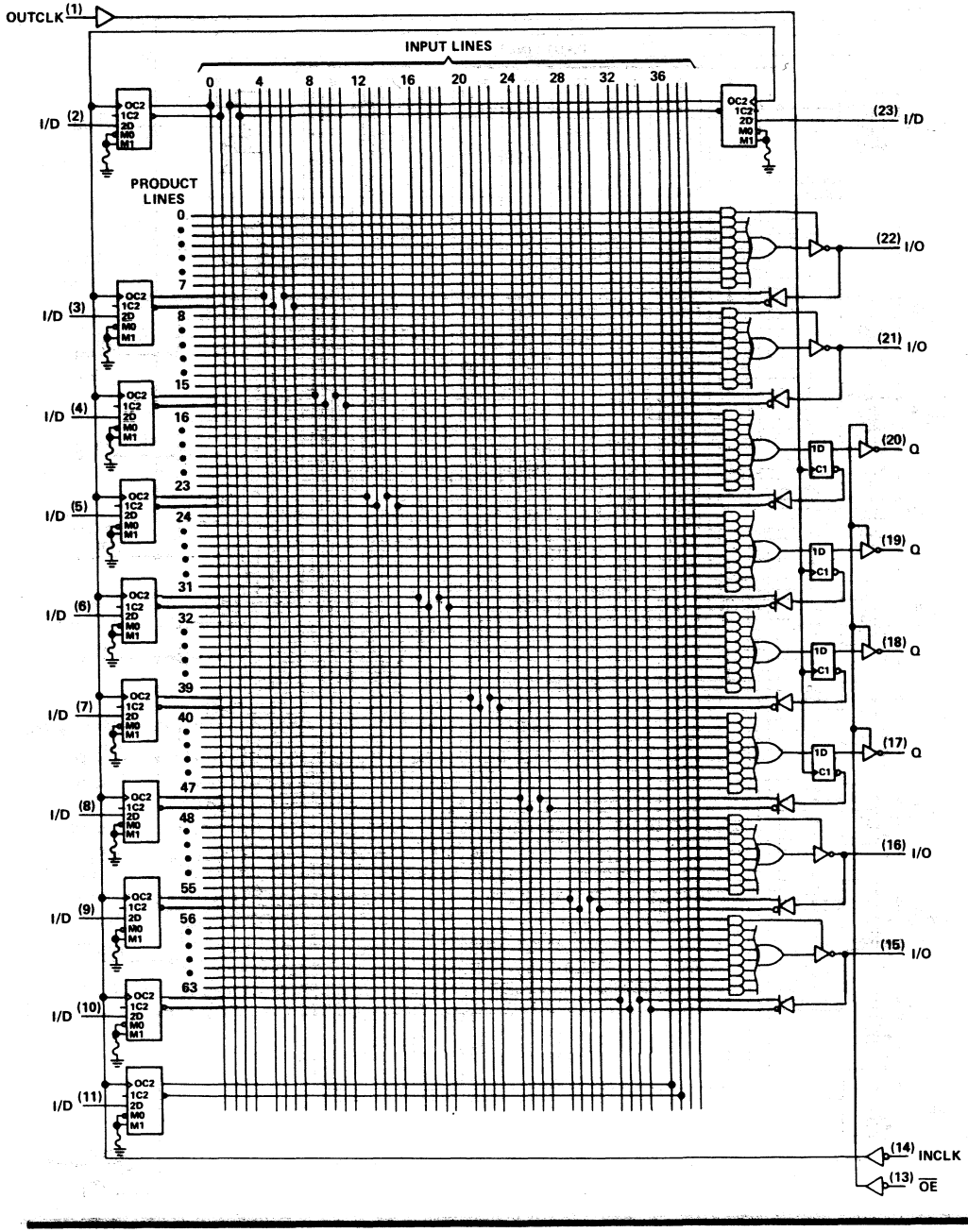

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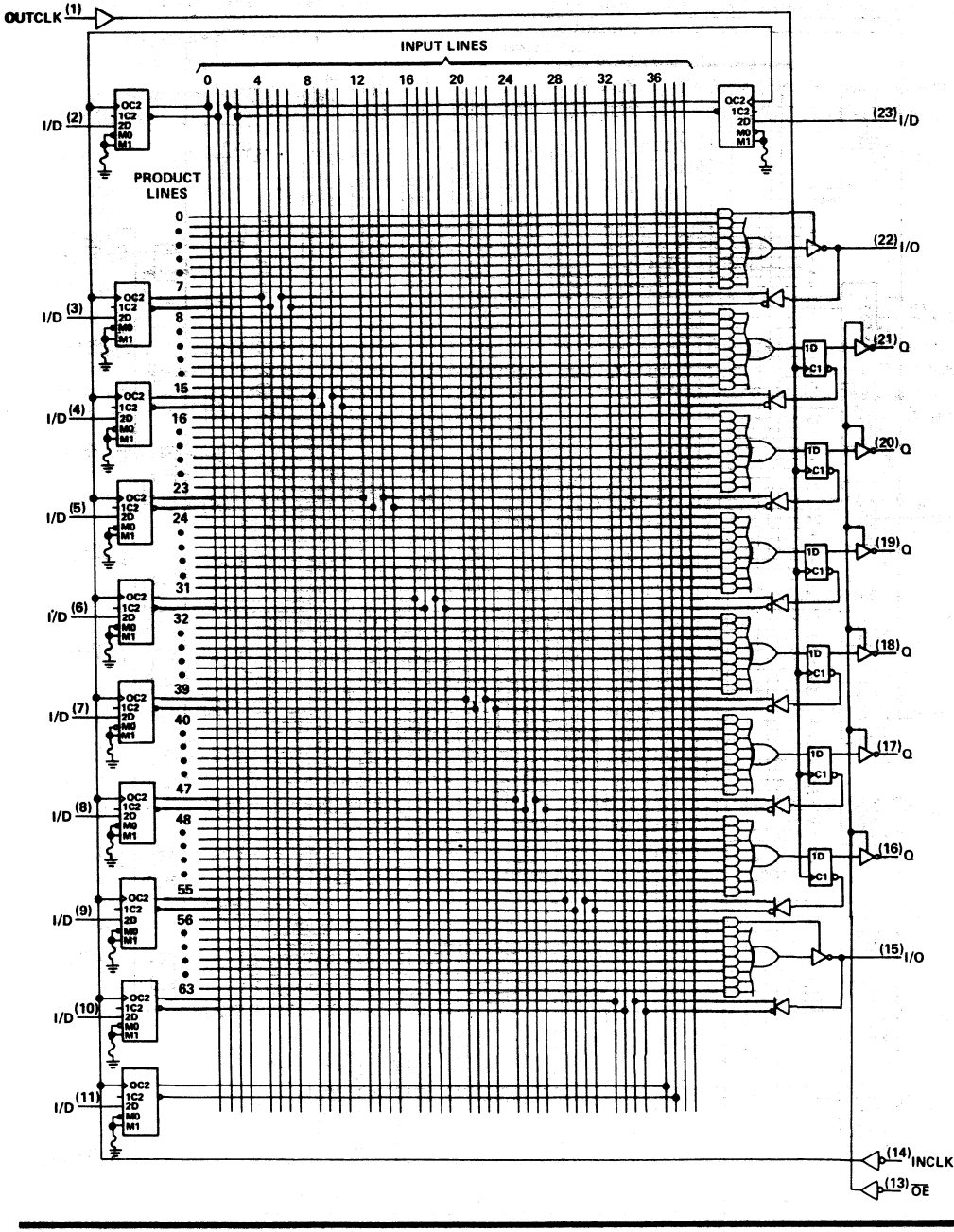
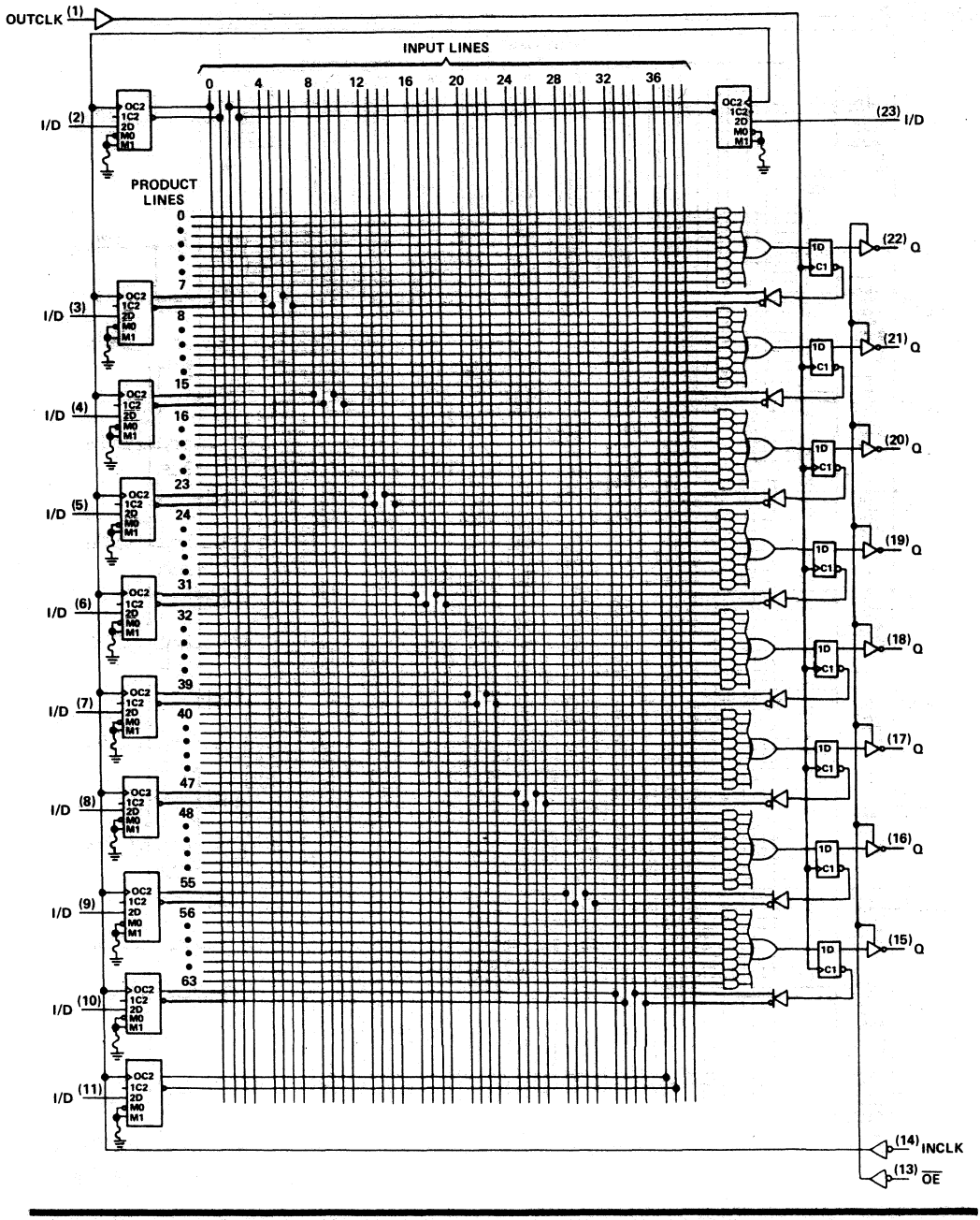

OUTCLK (1)
INPUT LINES
0 4 8 12 16 20 24 28 32 36
PRODUCT LINES
I/D (2)
I/D (3)
I/D (4)
I/D (5)
I/D (6)
I/D (7)
I/D (8)
I/D (9)
I/D (10)
I/D (11)
OC2 1C2 2D M0 M1
0 7 8 15 16 23 24 31 32 39 40 47 48 55 56 63
(23) I/D
(22) I/O
(21) Q
(20) Q
(19) Q
(18) Q
(17) Q
(16) Q
(15) I/O
1D C1
(14) INCLK
(13) OE



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TYPES SN54PLT19L8, SN54PLT19R4, SN54PLT19R6, SN54PLT19R8
SN74PLT19L8, SN74PLT19R4, SN74PLT19R6, SN74PLT19R8
LATCHED-INPUT FIXED-OR ARRAYS

D2710, DECEMBER 1982—REVISED SEPTEMBER 1983

- **Standard 24-Pin, 300-mil Packages**
- **Output Registers Automatically Clear During Power-Up**
- **Output Registers Have Preload Capability**
- **Data Input Registers Programmable to Buffers**
- **Choice of Operating Speeds**
  —1 Parts . . . 30 MHz Max, Standard power
  —2 Parts . . . 20 MHz Max, Half power

DEVICE	I/D INPUTS	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
'PLT19L8	11	2	2	0	6
'PLT19R8	11	0	0	8 (3-state buffers)	0
'PLT19R6	11	0	0	6 (3-state buffers)	2
'PLT19R4	11	0	0	4 (3-state buffers)	4

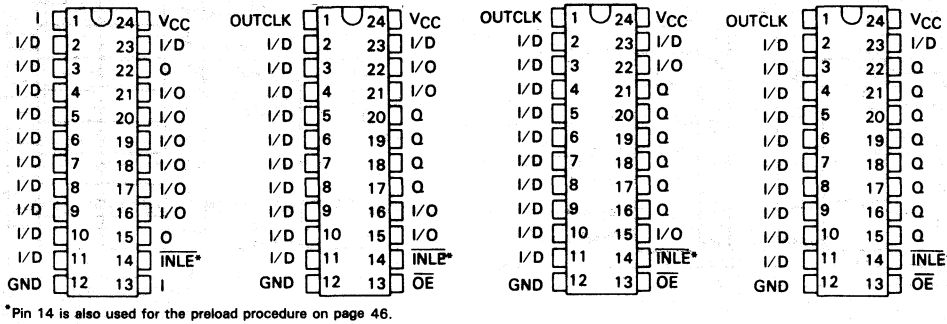
description

These fixed-OR arrays with eleven data inputs provide input registers that can be used as they are or be programmed into buffers. Some outputs of the 'PLT19R8, 'PLT19R6, and 'PLT19R4 have registers that can be loaded from the I/O pins by a preload procedure, while others are I/O ports and standard 3-state outputs. All the outputs are automatically set to a low level when power is applied. The —1 and —2 parts offer a choice of operating frequency, switching times, and power dissipation.

The SN54PLT19' is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74PLT19' is characterized for operation from 0°C to 70°C.

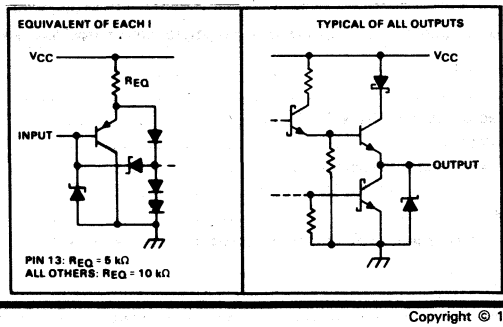
pin assignments in operating mode (voltages at pins 1 and 13 less than V_{IHH})

SN54' ... JT PACKAGE
SN74' ... NT PACKAGE
(TOP VIEW)



*Pin 14 is also used for the preload procedure on page 46.

schematics of inputs and outputs

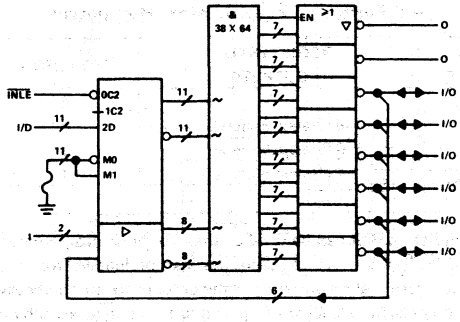


ADVANCE INFORMATION

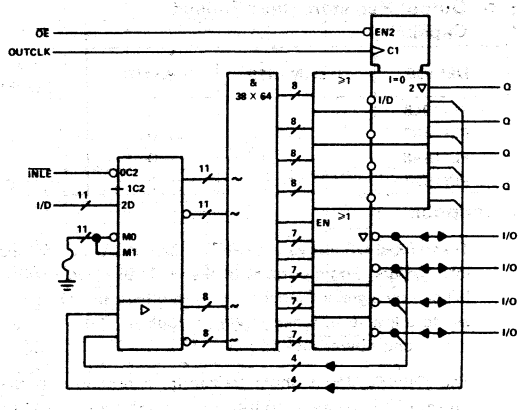
This document contains information on a new product. Specifications are subject to change without notice.

functional block diagrams

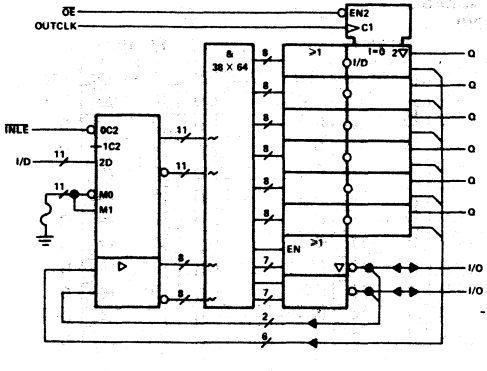
'PLT19L8



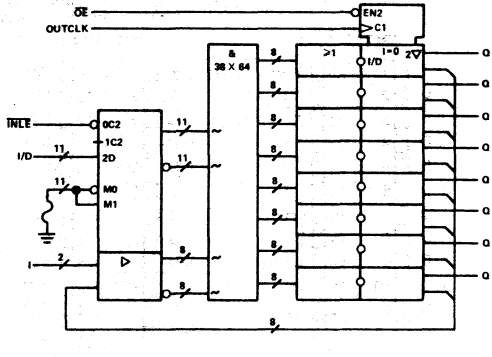
'PLT19R4



'PLT19R6



'PLT19R8



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage (see Note 1) ..... 5.5 V
Voltage applied to a disabled output (see Note 1) ..... 5.5 V
Voltage at any programming pin ..... 12 V
Operating free-air temperature range: SN54PLT' ..... −55°C to 125°C
SN74PLT' ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during a preload cycle.

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recommended operating conditions

		SN54PLT19'			SN74PLT19'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2		5.5	2		5.5	V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OH}	High-level output current			−2			−3.2	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended free-air operating temperature range

PARAMETER		TEST CONDITIONS†		SN54PLT19'			SN74PLT19'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = MIN,	I_{OH} = MAX	2.4	3.2		2.4	3.3		V
V_{OL}		V_{CC} = MIN,	I_{OL} = MAX		0.25	0.4		0.35	0.5	V
I_{OZH}	Outputs	V_{CC} = MAX,	V_O = 2.7 V			20			20	μA
	I/O ports					100			100	
I_{OZL}	Outputs	V_{CC} = MAX,	V_O = 0.4 V			−20			−20	μA
	I/O ports					−250			−250	
I_I	$\overline{OE}$ Input	V_{CC} = MAX,	V_I = 5.5 V			0.2			0.2	mA
	All others					0.1			0.1	
I_{IH}	$\overline{OE}$ Input	V_{CC} = MAX,	V_I = 2.7 V			40			40	μA
	All others					20			0.1	
I_{IL}	$\overline{OE}$ Input	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
	All others					−0.2			−0.2	
I_O§		V_{CC} = MAX,	V_O = 2.25 V	−30		−125	−30		−125	mA
I_{CC}	−1 Parts	V_{CC} = MAX,	V_I = 0 V,		150	200		150	200	mA
	−2 Parts	Outputs open			75	100		75	100	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are V_{CC} = 5 V, T_A = 25°C.

§The output conditions have been chosen to produce a current that closely approximates one half the true short-circuit current, I_{OS}.

'PLT19R8, 'PLT19R6, 'PLT19R4 timing requirements

		−1 PARTS		−2 PARTS		UNIT
		MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	30	0	30	MHz
t_w	Clock pulse duration, clock high or low	12		12		ns
t_{su}	Setup time, D input before $\overline{INLE}$↑					ns
t_{su}	Setup time, input or feedback before OUTCLK↑	15		15		ns
t_h	Hold time, input or feedback before OUTCLK↑	0		0		ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	INPUT MODE	TEST CONDITIONS	−1 PARTS			−2 PARTS			UNIT
					MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}			Either		30			20			MHz
t_{pd}	I, I/O	I/O, O	Either			16			25		ns
t_{pd}	OUTCLK↑	Q	Either			12			20		ns
t_{en}	$\overline{OE}$↓	Q	Either			8			15		ns
t_{dis}	$\overline{OE}$↑	Q	Either			6			12		ns
t_{pd}	$\overline{INLE}$	I/O, O	Latched			16			25		ns
t_{en}	$\overline{INLE}$	I/O, O, Q	Latched			25			35		ns
t_{dis}	$\overline{INLE}$	I/O, O, Q	Latched			20			30		ns
t_{pd}	I/D	I/O, O	Buffered			20			30		ns
t_{en}	I/D, I/O	I/O	Buffered			22			32		ns
t_{dis}	I/D, I/O	I/O	Buffered			17			26		ns

†All typical values are V_{CC} = 5 V, T_A = 25°C.

PRELOAD PROCEDURES

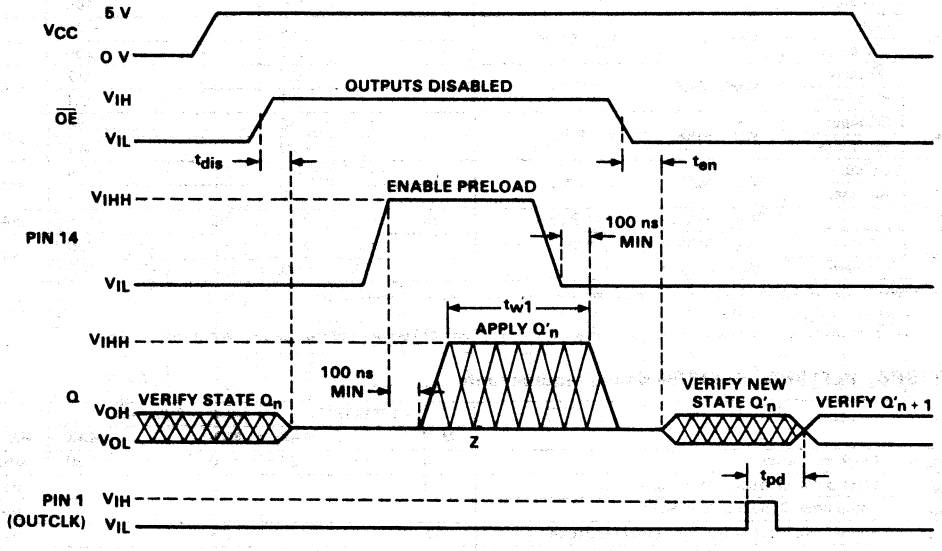

FIGURE 1—PRELOAD VOLTAGE WAVEFORMS

preload procedure for registered outputs

Step 1	Pin 13 to V_{IH}, Pin 1 to V_{IL}, and V_{CC} to 5 volts.
Step 2	Pin 14 to V_{IHH}.
Step 3	Apply an open circuit for a low and V_{IHH} for a high at the Q outputs.
Step 4	Pin 14 to V_{IL}.
Step 5	Remove the voltages applied to the outputs.
Step 6	Pin 13 to V_{IL}.
Step 7	Check the output states to verify preload.

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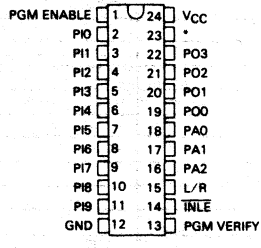
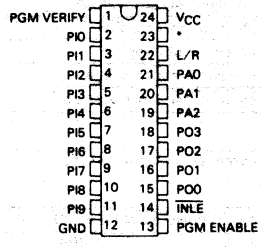
pin assignments in programming mode (PGM ENABLE, pin 1 or 11, at V_{IHH})

PRODUCT TERMS 0 THRU 31
(TOP VIEW)



PRODUCT TERMS 32 THRU 63
(TOP VIEW)



*No programming function. Make no connection.

TABLE 1—INPUT LINE SELECT

INPUT LINE NUMBER	PIN NAME										
	PI9	PI8	PI7	PI6	PI5	PI4	PI3	PI2	PI1	PI0	L/R
0	HH	HH	HH	HH	HH	HH	HH	HH	HH	L	Z
1	HH	HH	HH	HH	HH	HH	HH	HH	HH	H	Z
2	HH	HH	HH	HH	HH	HH	HH	HH	HH	L	HH
3	HH	HH	HH	HH	HH	HH	HH	HH	HH	H	HH
4	HH	HH	HH	HH	HH	HH	HH	HH	L	HH	Z
5	HH	HH	HH	HH	HH	HH	HH	HH	H	HH	Z
6	HH	HH	HH	HH	HH	HH	HH	HH	L	HH	HH
7	HH	HH	HH	HH	HH	HH	HH	HH	H	HH	HH
8	HH	HH	HH	HH	HH	HH	HH	L	HH	HH	Z
9	HH	HH	HH	HH	HH	HH	HH	H	HH	HH	Z
10	HH	HH	HH	HH	HH	HH	HH	L	HH	HH	HH
11	HH	HH	HH	HH	HH	HH	HH	H	HH	HH	HH
12	HH	HH	HH	HH	HH	HH	L	HH	HH	HH	Z
13	HH	HH	HH	HH	HH	HH	H	HH	HH	HH	Z
14	HH	HH	HH	HH	HH	HH	L	HH	HH	HH	HH
15	HH	HH	HH	HH	HH	HH	H	HH	HH	HH	HH
16	HH	HH	HH	HH	HH	L	HH	HH	HH	HH	Z
17	HH	HH	HH	HH	HH	H	HH	HH	HH	HH	Z
18	HH	HH	HH	HH	HH	L	HH	HH	HH	HH	HH
19	HH	HH	HH	HH	HH	H	HH	HH	HH	HH	HH
20	HH	HH	HH	HH	L	HH	HH	HH	HH	HH	Z
21	HH	HH	HH	HH	H	HH	HH	HH	HH	HH	Z
22	HH	HH	HH	HH	L	HH	HH	HH	HH	HH	HH
23	HH	HH	HH	HH	H	HH	HH	HH	HH	HH	HH
24	HH	HH	HH	L	HH	HH	HH	HH	HH	HH	Z
25	HH	HH	HH	H	HH	HH	HH	HH	HH	HH	Z
26	HH	HH	HH	L	HH	HH	HH	HH	HH	HH	HH
27	HH	HH	HH	H	HH	HH	HH	HH	HH	HH	HH
28	HH	HH	L	HH	HH	HH	HH	HH	HH	HH	Z
29	HH	HH	H	HH	HH	HH	HH	HH	HH	HH	Z
30	HH	HH	L	HH	HH	HH	HH	HH	HH	HH	HH
31	HH	HH	H	HH	HH	HH	HH	HH	HH	HH	HH
32	HH	L	HH	HH	HH	HH	HH	HH	HH	HH	Z
33	HH	H	HH	HH	HH	HH	HH	HH	HH	HH	Z
34	HH	L	HH	HH	HH	HH	HH	HH	HH	HH	HH
35	HH	H	HH	HH	HH	HH	HH	HH	HH	HH	HH
36	L	HH	HH	HH	HH	HH	HH	HH	HH	HH	Z
37	H	HH	HH	HH	HH	HH	HH	HH	HH	HH	Z
38	L	HH	HH	HH	HH	HH	HH	HH	HH	HH	HH
39	H	HH	HH	HH	HH	HH	HH	HH	HH	HH	HH

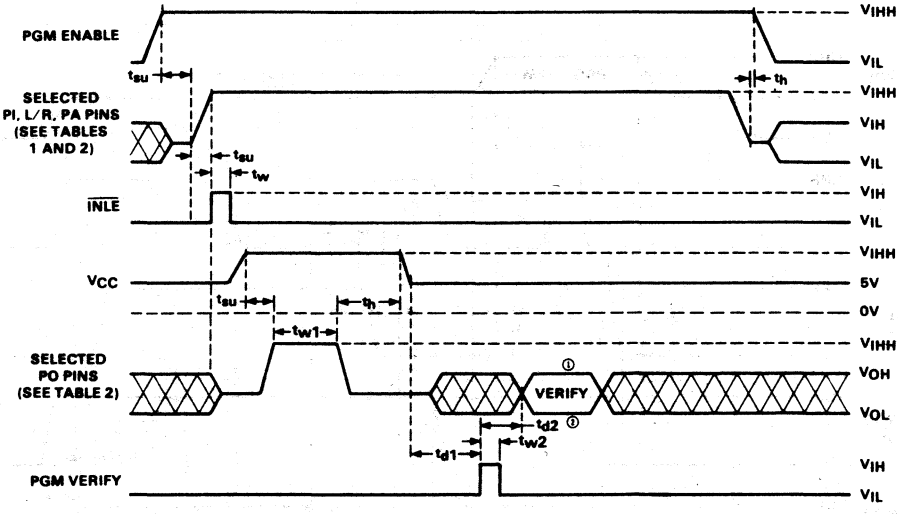
L = V_{IL}, H = V_{IH}, HH = V_{IHH}, Z = high impedance (e.g., 10 kΩ to 5 V)

TABLE 2—PRODUCT LINE SELECT

PRODUCT LINE NUMBER	PIN NAME						
	PO0	PO1	PO2	PO3	PA2	PA1	PA0
0, 32	Z	Z	Z	HH	Z	Z	Z
1, 33	Z	Z	Z	HH	Z	Z	HH
2, 34	Z	Z	Z	HH	Z	HH	Z
3, 35	Z	Z	Z	HH	Z	HH	HH
4, 36	Z	Z	Z	HH	HH	Z	Z
5, 37	Z	Z	Z	HH	HH	Z	HH
6, 38	Z	Z	Z	HH	HH	HH	Z
7, 39	Z	Z	Z	HH	HH	HH	HH
8, 40	Z	Z	HH	Z	Z	Z	Z
9, 41	Z	Z	HH	Z	Z	Z	HH
10, 42	Z	Z	HH	Z	Z	HH	Z
11, 43	Z	Z	HH	Z	Z	HH	HH
12, 44	Z	Z	HH	Z	HH	Z	Z
13, 45	Z	Z	HH	Z	HH	Z	HH
14, 46	Z	Z	HH	Z	HH	HH	Z
15, 47	Z	Z	HH	Z	HH	HH	HH
16, 48	Z	HH	Z	Z	Z	Z	Z
17, 49	Z	HH	Z	Z	Z	Z	HH
18, 50	Z	HH	Z	Z	Z	HH	Z
19, 51	Z	HH	Z	Z	Z	HH	HH
20, 52	Z	HH	Z	Z	HH	Z	Z
21, 53	Z	HH	Z	Z	HH	Z	HH
22, 54	Z	HH	Z	Z	HH	HH	Z
23, 55	Z	HH	Z	Z	HH	HH	HH
24, 56	HH	Z	Z	Z	Z	Z	Z
25, 57	HH	Z	Z	Z	Z	Z	HH
26, 58	HH	Z	Z	Z	Z	HH	Z
27, 59	HH	Z	Z	Z	Z	HH	HH
28, 60	HH	Z	Z	Z	HH	Z	Z
29, 61	HH	Z	Z	Z	HH	Z	HH
30, 62	HH	Z	Z	Z	HH	HH	Z
31, 63	HH	Z	Z	Z	HH	HH	HH

programming parameters, T_A = 25°C

			MIN	NOM	MAX	UNIT
V_{CC}	Verify-level supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
V_{OH}	High-level output voltage				5.5	V
V_{IHH}	Program-pulse input voltage		10.25	10.5	10.75	V
I_{IHH}	Program-pulse input current	PO			50	mA
		PGM ENABLE, L/R			25	
		PI, PA			5	
		V_{CC}			400	
t_{w1}	Program-pulse duration at PO or I/D pins		10		50	μs
t_{w2}	Pulse duration at PGM VERIFY		100			ns
t_{su}	Setup time		100			ns
t_h	Hold time		100			ns
t_{d1}	Delay time from V_{CC} to 5.5 V to PGM VERIFY ↑		100			μs
t_{d2}	Delay time from PGM VERIFY ↑ to valid output		200			ns
t_{d3}	Delay time		100			ns
	Input voltage at pins 1 and 13 to open verify-protect (security) fuse		20	21	22	V
	Input current to open verify-protect (security) fuse				400	mA
	Pulse duration to open verify-protect (security) fuse		20		50	ms



① A high level during the verify interval indicates that programming has not been successful.
② A low level during the verify interval indicates that programming has been successful.

FIGURE 2 — ARRAY PROGRAMMING WAVEFORMS

programming procedure for array fuses

Array fuses are programmed using a linear select method. Each fuse can be opened by selecting the appropriate (one of 40) input line and then pulsing the correct (one of 64) product line. The levels for selecting input lines and product lines are shown in Tables 1 and 2.

Step 1	Raise PGM ENABLE to V_{IHH}.
Step 2	Select an input line by applying appropriate levels to L/R and PI pins.
Step 3	Begin selection of the output line with appropriate conditions on PA pins (see Table 2).
Step 4	Pulse $\overline{INLE}$ to V_{IHH}.
Step 5	Raise V_{CC} to V_{IHH}.
Step 6	Blow the fuse by pulsing the appropriate PO pin to V_{IHH} as shown in Table 2 for the product line.
Step 7	Return V_{CC} to 5 volts and pulse PGM VERIFY. The PO pin selected in Step 4 will be less than V_{OL} if the fuse is open.

Steps 1 thru 7 may be repeated if the verification does not indicate that the fuse was successfully programmed (blown), but no more than 4 times. Verification is possible only with the verify-protect fuse intact.

To prevent further verification, two last fuses may be blown by raising pin 1 and pin 13 to 21 volts ±1 volt. V_{CC} is required to be at 0 during this operation.

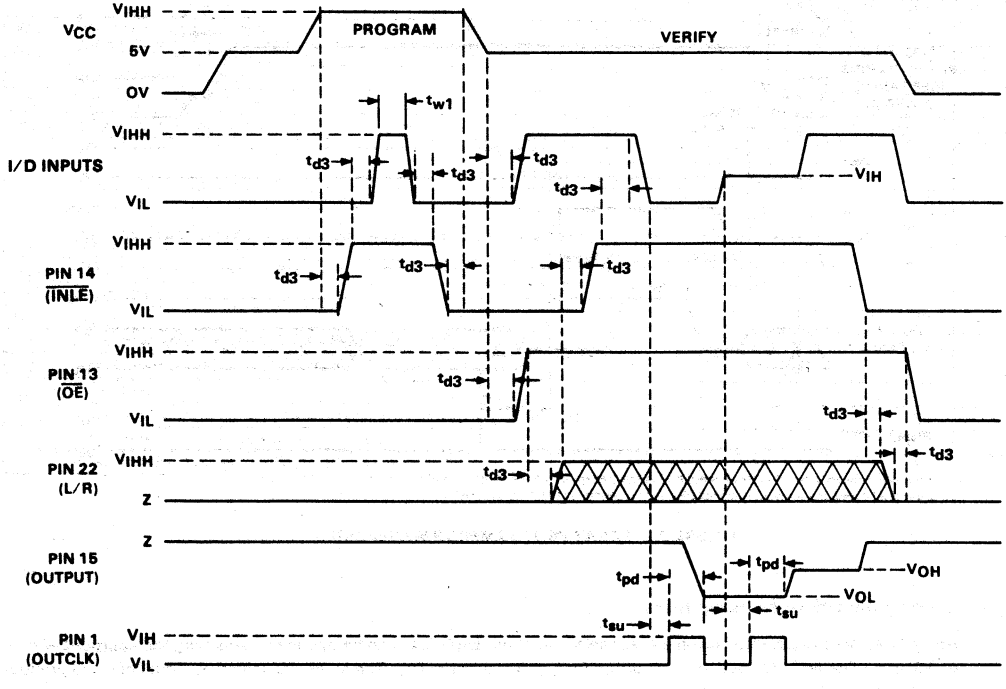
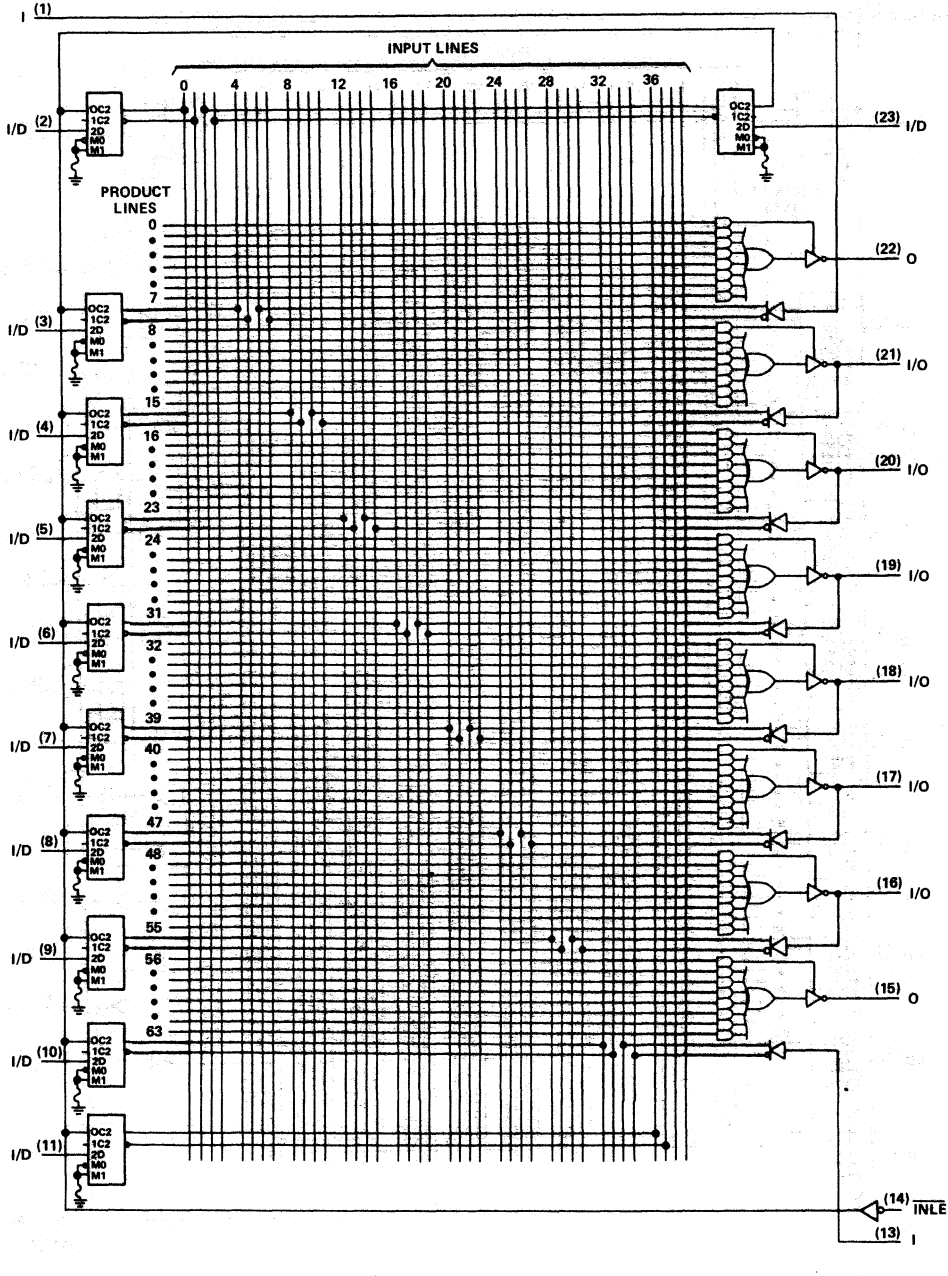


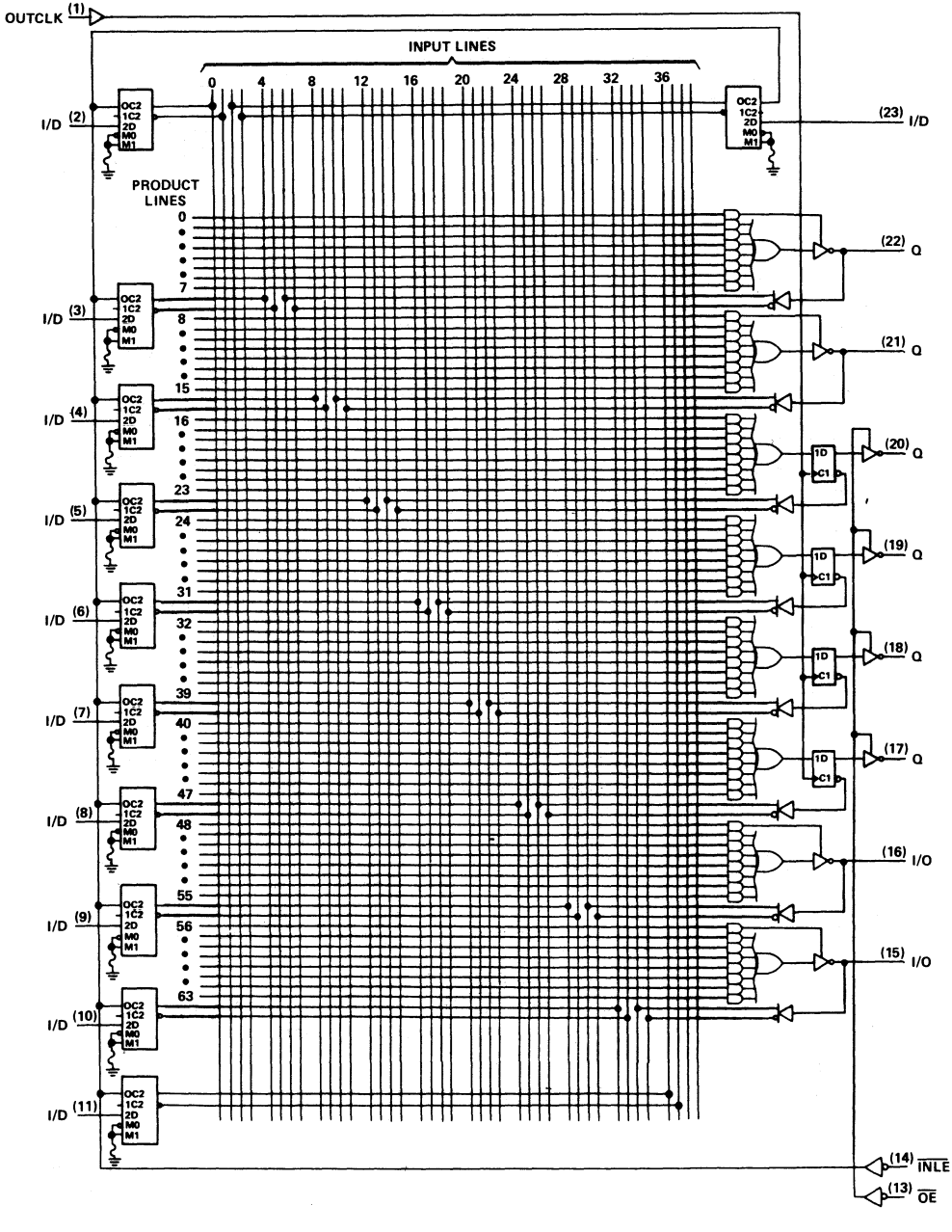
FIGURE 3 — ARCHITECTURAL FUSE PROGRAMMING WAVEFORMS

programming procedure for architectural fuses (see Note 2)

Step 1	Apply low levels to all I/D pins and 5 volts to the V_{CC} pin.
Step 2	Raise V_{CC} pin to V_{IHH}.
Step 3	Raise $\overline{INLE}$ pin to V_{IHH}.
Step 4	To program a D input pin into an I input pin pulse the selected pin to V_{IHH}.
Step 5	Lower $\overline{INLE}$ to V_{IL} and V_{CC} to 5 volts.
Step 6	Raise pin 13 and all I/D input pins to V_{IHH}.
Step 7	Set pin 22 to Z to select pins 2 thru 11 or set pin 22 to V_{IHH} to select pin 23.
Step 8	Raise $\overline{INLE}$ to V_{IHH}.
Step 9	To verify that fuse has been blown, pulse select I pin from V_{IHH} to V_{IL}, then to V_{IH} and back to V_{IHH} while clocking pin 1. If output at pin 15 follows the I input the fuse has been blown.
Step 10	Repeat above steps 1 thru 9 for each D input to be programmed into an I input.

NOTE 2: Refer to pin assignments in operating mode for programming selected I/D pins from D inputs to I inputs.


I (1)
INPUT LINES
0 4 8 12 16 20 24 28 32 36
I/D (2)
I/D (3)
I/D (4)
I/D (5)
I/D (6)
I/D (7)
I/D (8)
I/D (9)
I/D (10)
I/D (11)
PRODUCT LINES
0
7
8
15
16
23
24
31
32
39
40
47
48
55
56
63
(23) I/D
(22) O
(21) I/O
(20) I/O
(19) I/O
(18) I/O
(17) I/O
(16) I/O
(15) O
(14) INLE
(13) I



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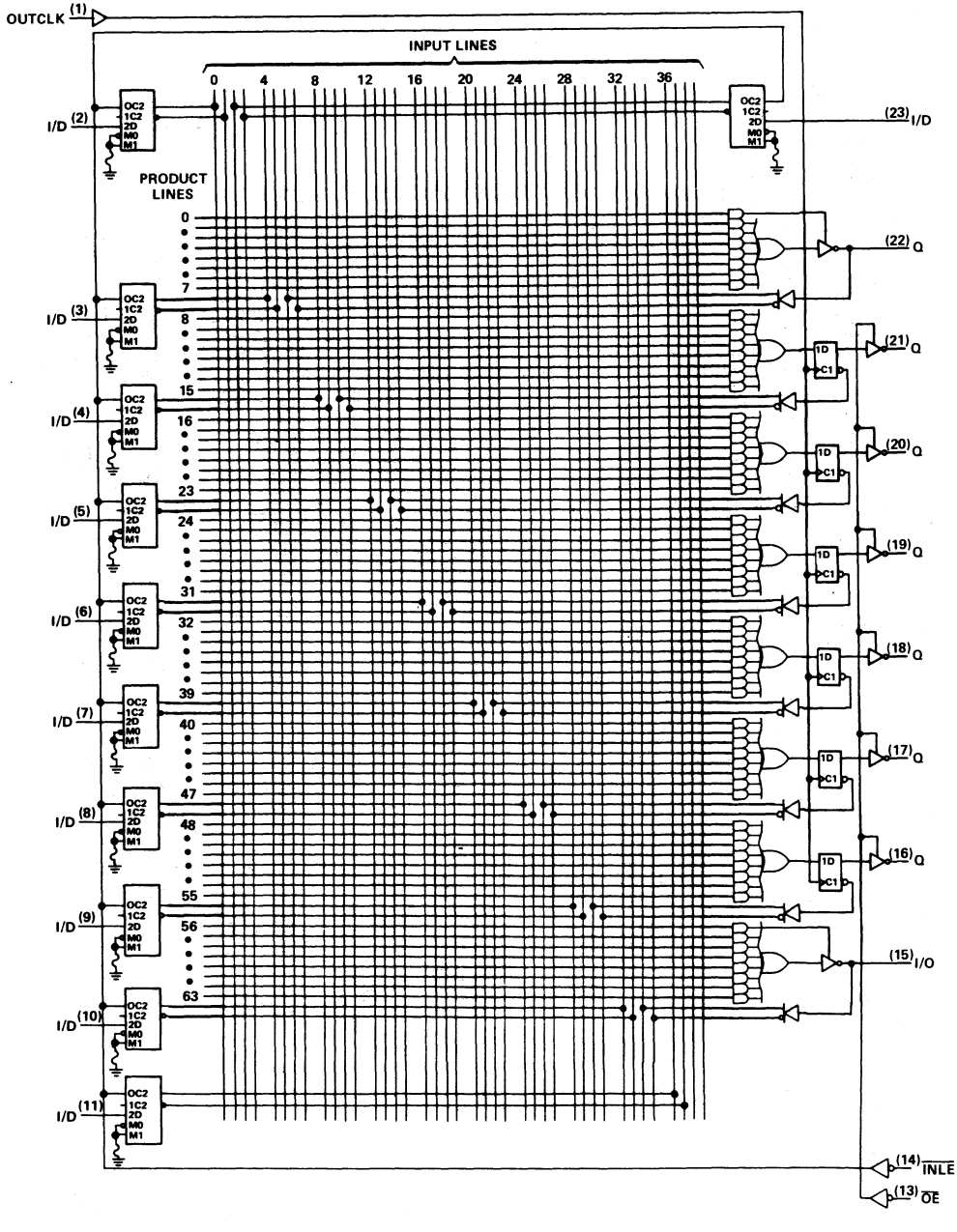
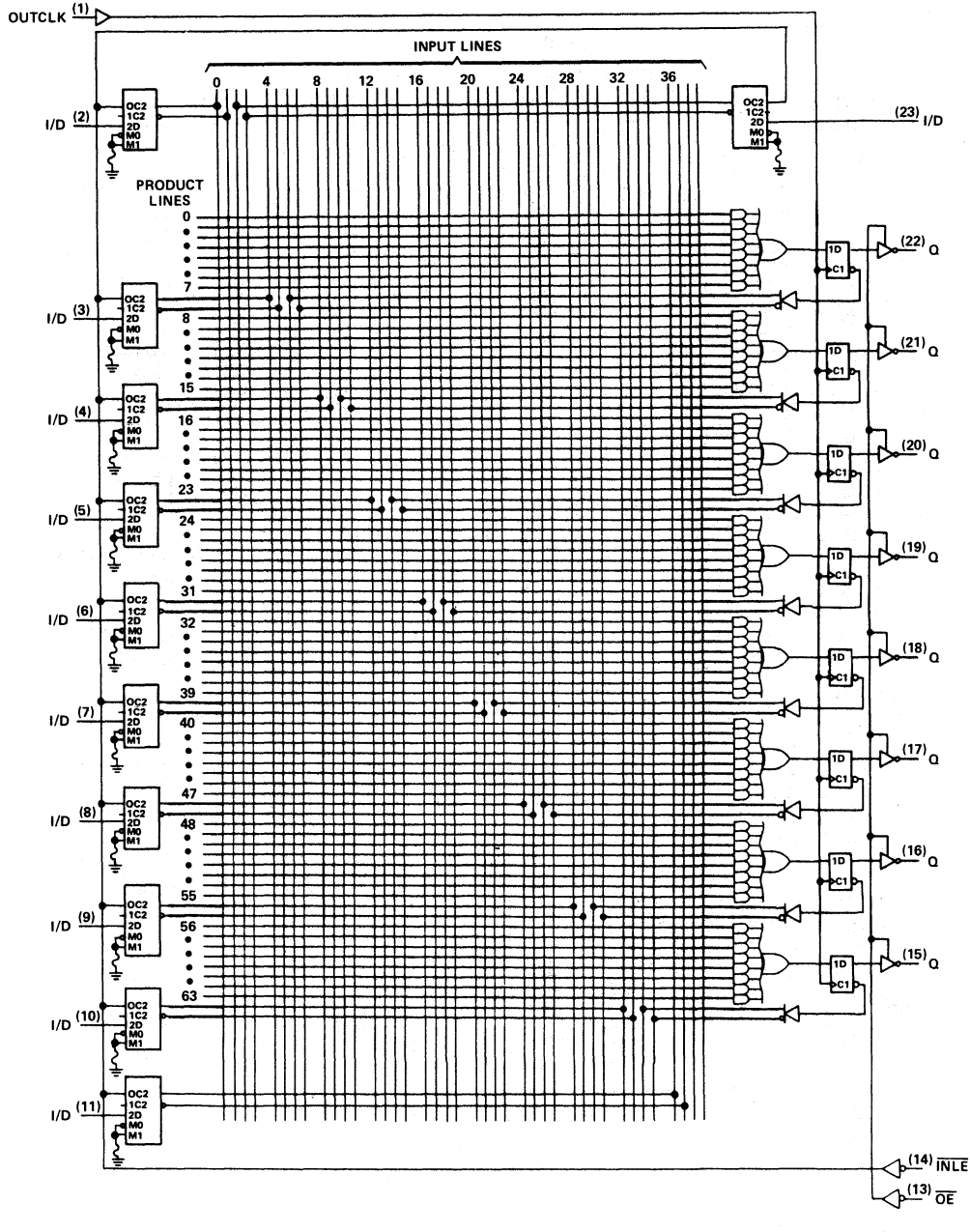

OUTCLK (1)
INPUT LINES
0 4 8 12 16 20 24 28 32 36
I/D (2)
(23) I/D
PRODUCT LINES
0
7
I/D (3)
(22) Q
8
15
I/D (4)
(21) Q
16
23
I/D (5)
(20) Q
24
31
I/D (6)
(19) Q
32
39
I/D (7)
(18) Q
40
47
I/D (8)
(17) Q
48
55
I/D (9)
(16) Q
56
63
I/D (10)
(15) I/O
I/D (11)
(14) INLE
(13) OE
OC2
1C2
2D
M0
M1
1D
C1



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PLA APPLICATIONS

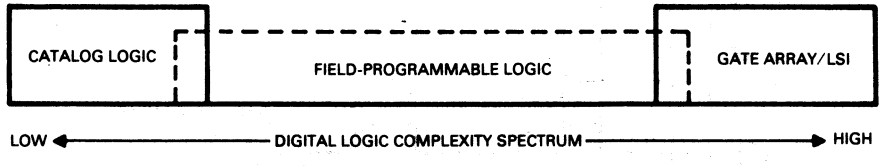
FIELD PROGRAMMABLE LOGIC

INTRODUCTION

Texas Instruments Field-Programmable Logic is the result of combining established Advanced Low-Power Schottky technology with the familiar Titanium-Tungsten (TiW) fuse-link technology used in PROMs to produce a family of powerful new user-programmed devices. Not everyone is familiar as yet with the Field-Programmable Fixed-OR Array (FOA), Logic Sequencer (FPLS), and Logic Array (FPLA). The highlights below are presented to start the process of familiarization by describing some of the unique advantages available to the designer who can create custom logic on demand to meet special requirements.

- *Package count reduction* compared to standard catalog SSI and MSI logic.
- *Lower cost* due to reduction in substrate or PC area, connectors, overall system size, and assembly labor.
- *Improved reliability* through fewer interconnects (IC bond wires, solder connections, through-holes in PC boards, connector contacts) and simplified substrate circuitry.
- *Circuit flexibility* that will adapt to custom applications.
- *Shorter design cycle* as compared to special-order devices.

Field-Programmable Logic is intended to integrate functions normally implemented with standard gates, flip-flops, and MSI. It can be used to reduce miscellaneous logic package count, or as "glue" around high-density LSI circuitry (i.e., microprocessors and gate arrays). It is positioned as a "gap filler" between standard catalog logic devices and large-scale integration.



DEFINITIONS AND SYMBOLOGY

Just as logic symbols simplified schematics, the new terms and symbology presented here will simplify array logic diagrams for programmable devices. New terms will be highlighted by italics throughout the text.

PLA APPLICATIONS

SYMBOLOGY

All the products presented are variations of a basic two-array architecture. A typical Field-Programmable Logic device may have over 100 gates and in excess of 1000 fuses. Because of this, it is necessary to devise a shorthand symbology to simplify logic diagrams. The logic diagrams used in this data book will adhere to the symbology presented below.

First, view a conventional two-input AND gate. Inputs are designated as A and B. The output function of the AND gate is the product of the inputs (F = A·B).

FIGURE 1

Now redraw the same logic element using array symbology (Figure 2). Notice that the AND gate is represented as having a single input called a *product line*. The *input terms* are shown as lines perpendicular to the product line. The output (*product term*) is the product of the input terms.

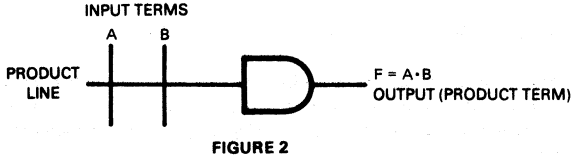


FIGURE 2

In the following figure we will extend the symbology to develop a simple programmable array element. First, notice that buffers have been added to the inputs. These buffers make available both true and complement states of any input to the product lines. Second, notice that another AND gate has been added. The intersection of the input terms and product lines form a 4 X 2 AND array.

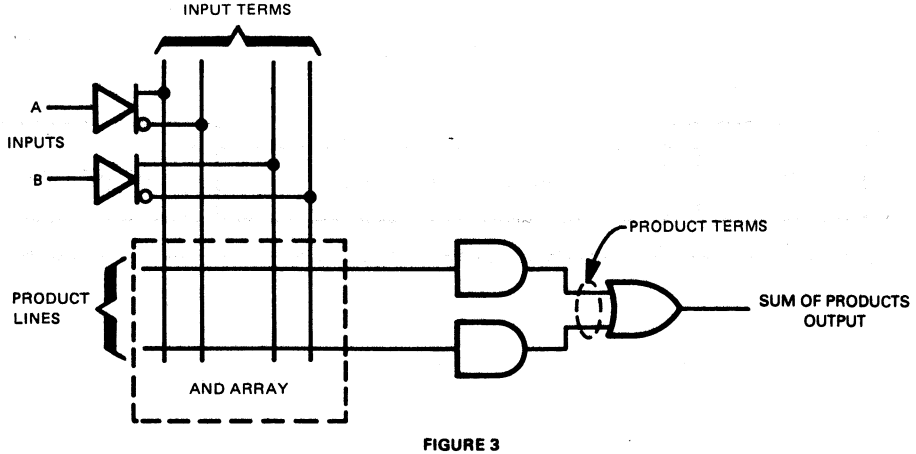


FIGURE 3

Third, the product terms of the AND gates are summed with an OR gate. The output function is now the sum of products of the input lines.

To make the structure in Figure 3 useful, provisions must be made to program the AND array. Programming is done by means of fusible TiW links. A fuse is located between the input term and the actual input to the AND gate (see Figure 4). In our special array symbology, a fuse is visualized to exist at each intersection of the input terms and product lines.

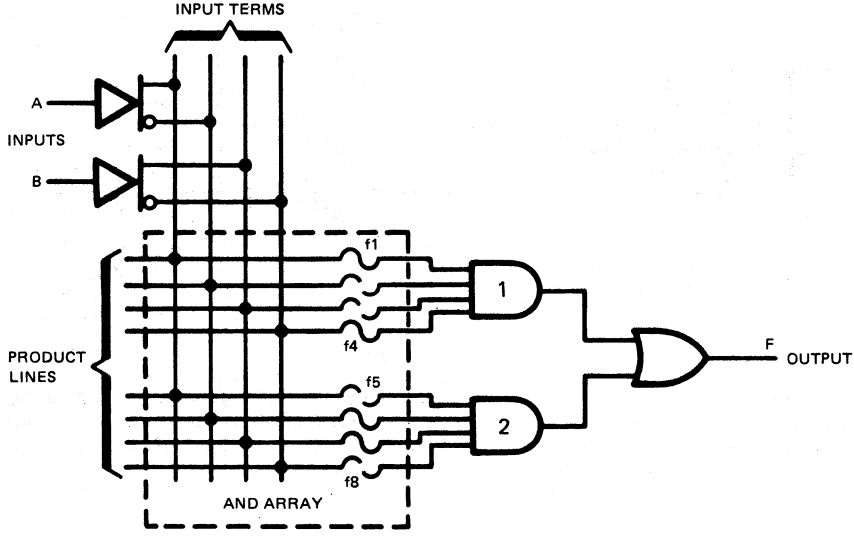


FIGURE 4

Now we can express the output function F in terms of the inputs. Notice that fuses f2, f3, f5, and f8 have been blown and A and $\overline{B}$ are still connected to AND gate #1 through fuses f1 and f4. Likewise, $\overline{A}$ and B are connected to AND gate #2 through fuses f6 and f7. The output can now be expressed as $F = A\overline{B} + \overline{A}B$.

A compact representation of the unprogrammed version of Figure 4 using the rules explained in Section 6 of the ALS/AS data book is shown in Figure 5.

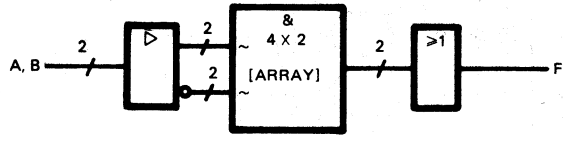


FIGURE 5

Figure 6 will further show how the function $F = A\overline{B} + \overline{A}B$ is represented in our array symbology and will present the convention used to show the fuse states in a programmed array. This convention simply places an X at the intersection of each input term and product line for which an intact fuse is required. Blown fuses will be represented by the absence of an X at the appropriate intersection.

Unused product lines, where all fuses are left intact, can be noted with an X in the AND symbol. This product term will always be inactive (i.e., have no affect on any sum term in which it appears). If all fuses are blown on a product line, the output containing this product term will be disabled (i.e., forced high). Exercise care in programming to avoid this condition.

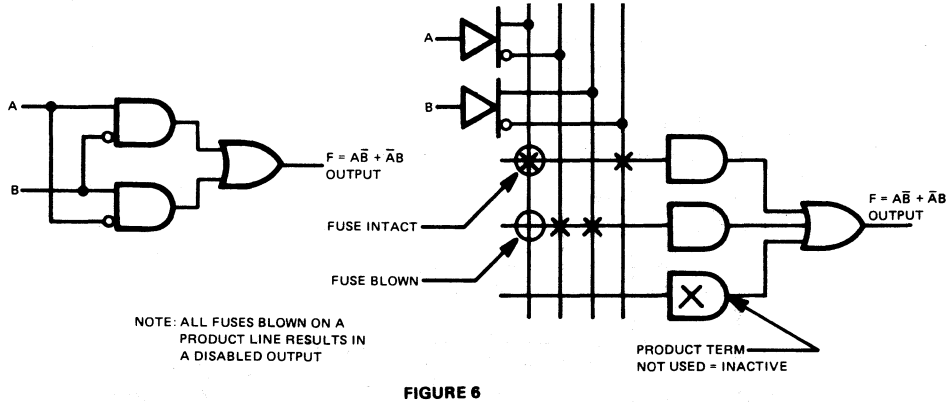


FIGURE 6

The symbology is further extended to include the two-array circuit structure, which is the basic Field-Programmable Logic architecture. Figure 7 is a two-array logic diagram. In earlier examples, the AND gates were summed in a single OR gate. In the two-array structure, the AND gate outputs enter a programmable OR array. The OR array allows any product term to be included in the sum term of any output or in all outputs.

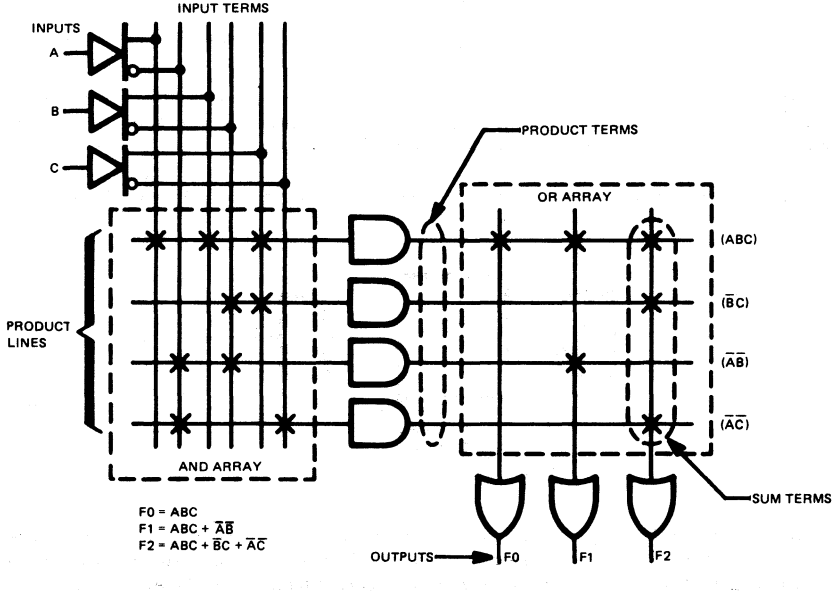


FIGURE 7

All of the Field Programmable Logic circuits described in this data book are variations of the two-array architecture. Variations will include output registers, internal feedback, feedback registers, and fixed OR arrays. Figures 8, 9, and 10 represent simplified versions of three specific families of Field-Programmable Logic.

FIELD-PROGRAMMABLE LOGIC ARRAY (FPLA)

The basic two-array structure developed in the symbology section is more commonly referred to as a *Field-Programmable Logic Array*. A useful addition to this structure would be an output-enable function as shown in the generalized FPLA diagram below.

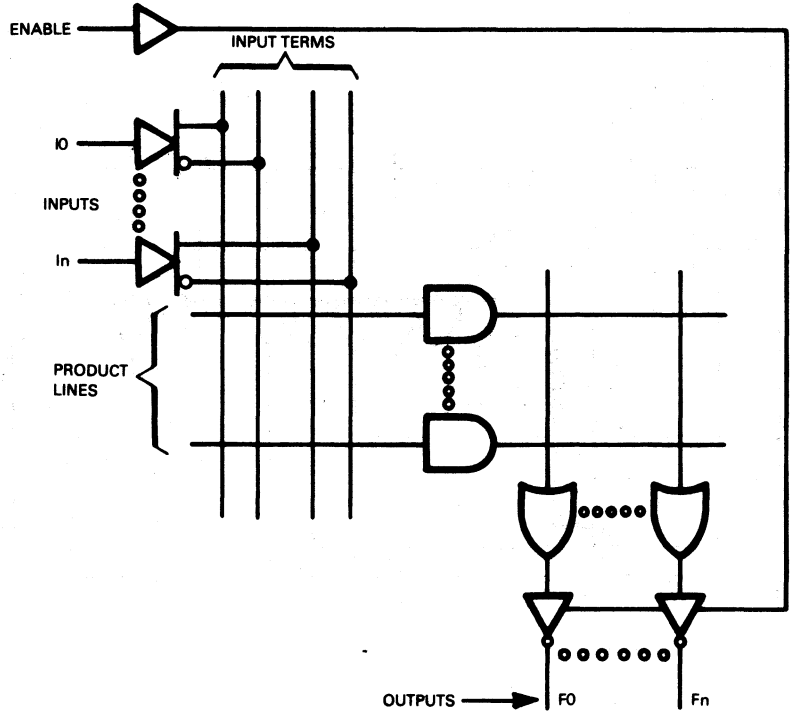


FIGURE 8

FIELD-PROGRAMMABLE LOGIC SEQUENCER (FPLS)

Field-Programmable Logic Sequencers (FPLS) are designed to solve state-machine problems of the Mealy type. Based on the FPLA structure, they include flip-flop elements in feedback paths between the OR and AND arrays as shown in Figure 9. These flip-flop elements can be of the D type or J-K type. Logic levels from the OR array can also be stored in flip-flop elements in each output.

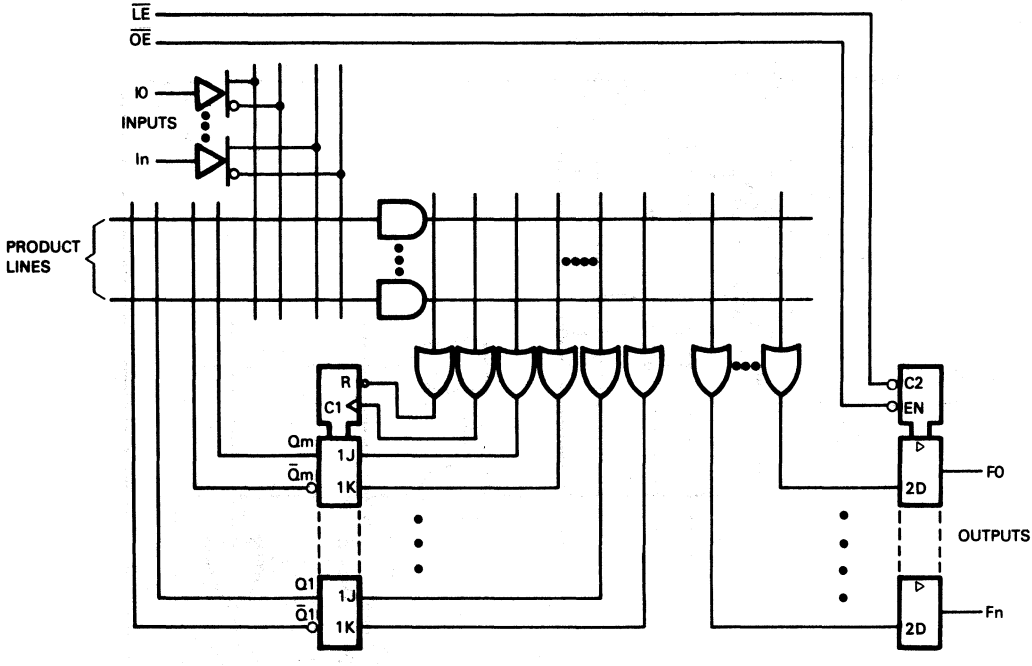


FIGURE 9

FIXED-OR ARRAYS (FOA)

The *Fixed-OR Array* is a special case of the FPLS that is capable of solving Mealy-type state-machine problems. The FOA does not have a Programmable-OR Array. Product terms are partitioned and allocated to specific outputs. All product terms allocated to an output are summed with a single OR gate. Output feedback, as well as registered inputs and outputs, are added to the structure to increase logic utility. Figure 10 includes generalized diagrams of various FOA structures.

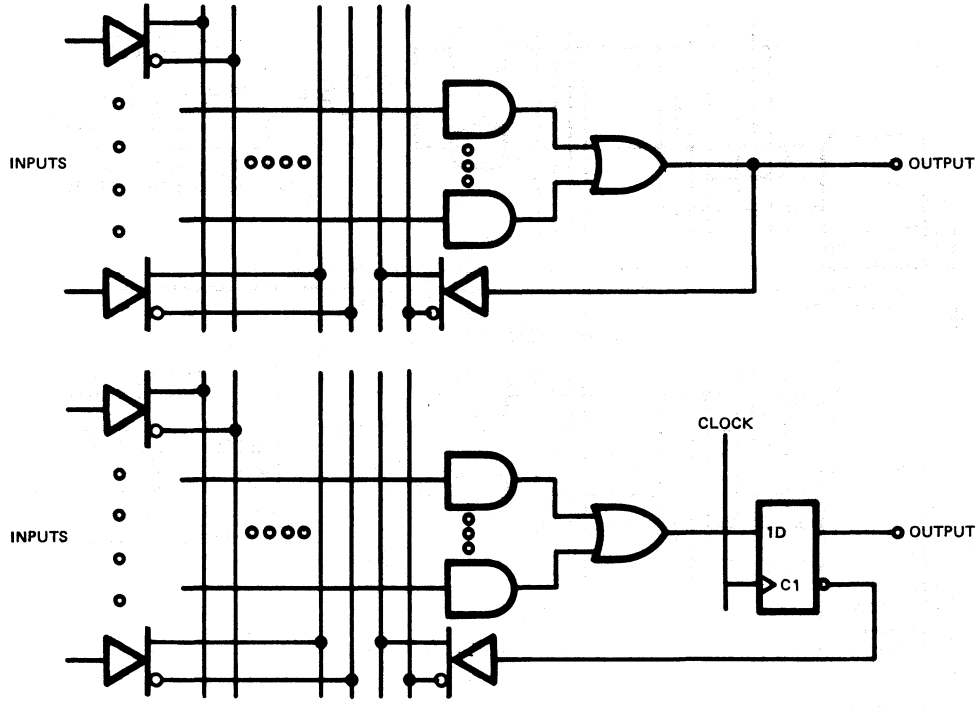


FIGURE 10

DESIGNING WITH FIELD-PROGRAMMABLE LOGIC ARRAYS

The basic logic implementation of Field-Programmable Logic devices is the previously developed AND-OR array. Additions to this structure provide unique functional capabilities. This section will review these logic structures.

INPUTS

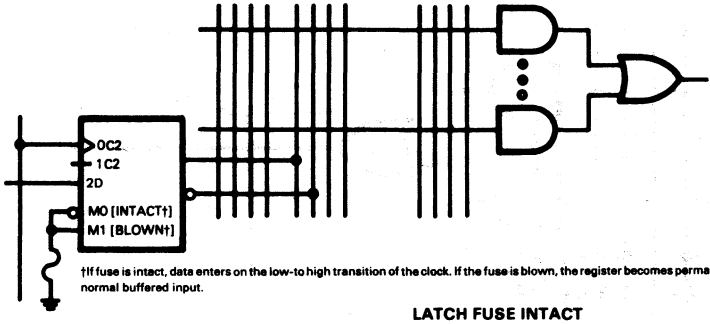
All data inputs are configured to provide both true and complement components to the AND array. These inputs are either buffered or registered. Control pins also exist for enable and clock functions.

PLA APPLICATIONS

The normal array input is through a buffer with true and complement outputs of the buffer made available to each product line through a TiW fuse.

Some device types in the Field-Programmable Logic family have programmable latched inputs. With the latch fuse intact, the input acts as an edge-triggered D-type register or transparent latch depending on device type. The true and complement outputs of the input latch are made available to each product line through a latch fuse. With the latch fuse blown, the input latch is converted into a normal buffered input (see Figure 11).

REGISTER FUSE INTACT



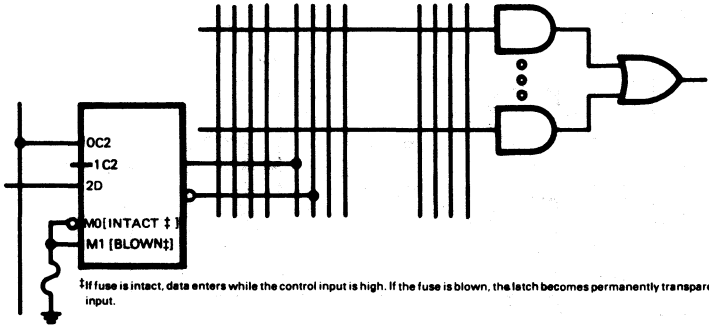
D-TYPE REGISTER FUNCTION TABLE

CLOCK	D	Q	$\overline{Q}$
↑	H	H	L
↑	L	L	H
L	X	Q_0	$\overline{Q}_0$

Q_0 = THE STATE OF Q BEFORE CLOCK ↑

†If fuse is intact, data enters on the low-to high transition of the clock. If the fuse is blown, the register becomes permanently transparent and is equivalent to a normal buffered input.

LATCH FUSE INTACT



TRANSPARENT LATCH FUNCTION TABLE

ENABLE	D	Q	$\overline{Q}$
H	L	L	H
H	H	H	L
L	X	Q_0	$\overline{Q}_0$

Q_0 = THE LEVEL OF Q BEFORE ENABLE ↓

‡If fuse is intact, data enters while the control input is high. If the fuse is blown, the latch becomes permanently transparent and is equivalent to a normal buffered input.

REGISTER/LATCH FUSE BLOWN

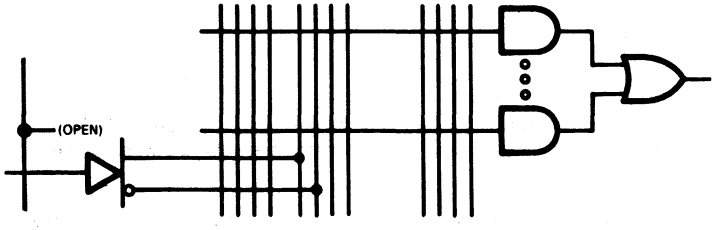


FIGURE 11

CONTROL PINS

Clock and latch-enable pins allow external control of input and output latches. Output enable controls the operation of the registered three-state outputs.

OUTPUTS

Various output configurations provide a design flexibility not previously available to the designer using catalog logic.

- PROGRAMMABLE I/O - The combinational output of the FOA incorporates 3-state drivers if the enable function is logically controlled by the AND array (see Figure 12). This allows the output to be programmed as an input, an output, or logic-controlled I/O.

- 3-STATE OUTPUTS - The FPLA and FPLS have output enable pins available for 3-state control, and the registered outputs of the FOA are controlled by a common output enable. Three-state control of the combinational outputs of the FOA is accomplished through programming as described earlier.

PROGRAMMABLE 3-STATE OPERATION
ALL FUSES BLOWN . . . NORMAL OUTPUT
ALL FUSES INTACT . . . OUTPUT IN HIGH-Z STATE
FUSES SELECTED . . . PROGRAMMED I/O

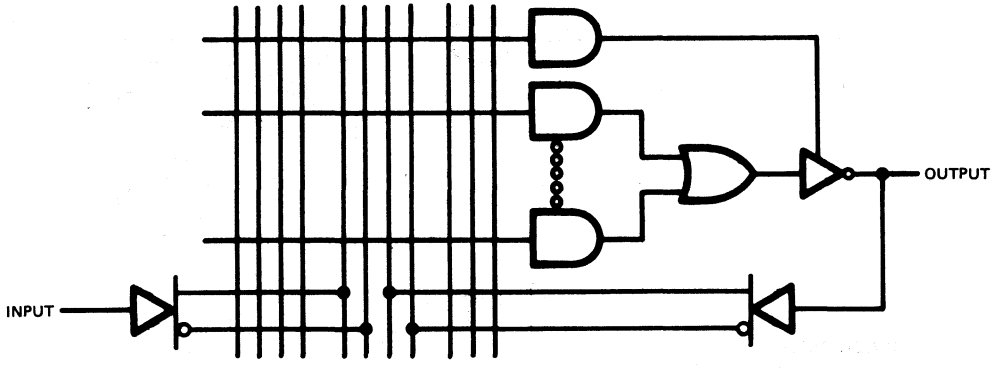


FIGURE 12

- REGISTERED OUTPUTS - The FPLS and some FOA's have latches on their outputs. The FPLS has a transparent latch on each of its 6 outputs. The output function levels are stored by a common asynchronous latch enable pin $\overline{LE}$.

TRANSPARENT LATCH
FUNCTION TABLE

$\overline{LE}$	D	Q
L	L	L
L	H	H
H	X	Q_0

Q_0 = THE LEVEL OF Q BEFORE $\overline{LE}$ ↑

The output (D) latch on the FOA stores output levels with a low-to-high transition of the clock. This structure also provides feedback of Q through a true and complement buffer to the Programmable AND array.

- OPEN-COLLECTOR OUTPUTS - Some devices have open-collector outputs available. These outputs may be wire-ANDed (active-high) or wire-ORed (active-low). This feature requires no external logic, which would add to the component count and propagation delay.

- POLARITY SELECT - Circuitry provides a polarity select fuse for each FPLA output. The function of these fuses is shown in Figure 13.

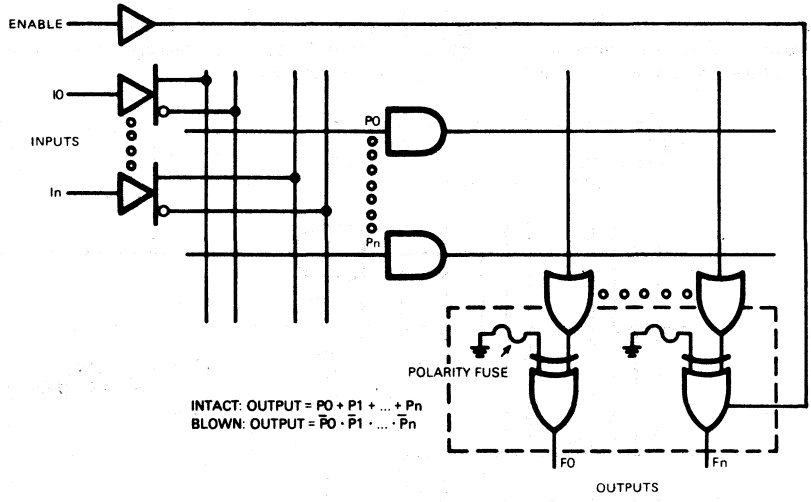
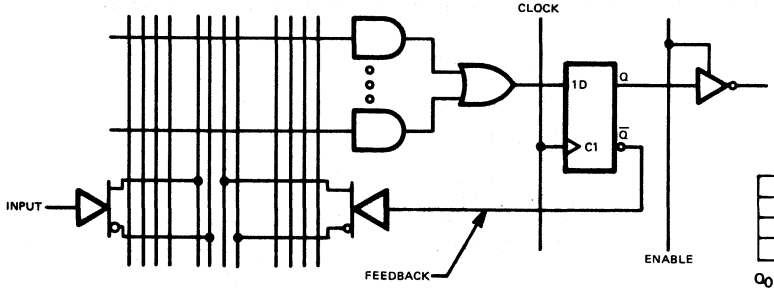


FIGURE 13

FEEDBACK PATHS

The $\overline{Q}$ feedback of the output register of the FOA (see Figure 14), provides the basis for implementing sequential functions. The FPLS (Figure 15), is designed to solve state-machine problems of the Mealy type. It contains four J-K flip-flops completely buried in the feedback path between the OR and AND arrays.



D-TYPE REGISTER FUNCTION TABLE

CLOCK	D	Q	$\overline{Q}$
↑	H	H	L
↑	L	L	H
L	X	Q_0	$\overline{Q}_0$

Q_0 = THE LEVEL OF Q BEFORE CLOCK ↑

FIGURE 14

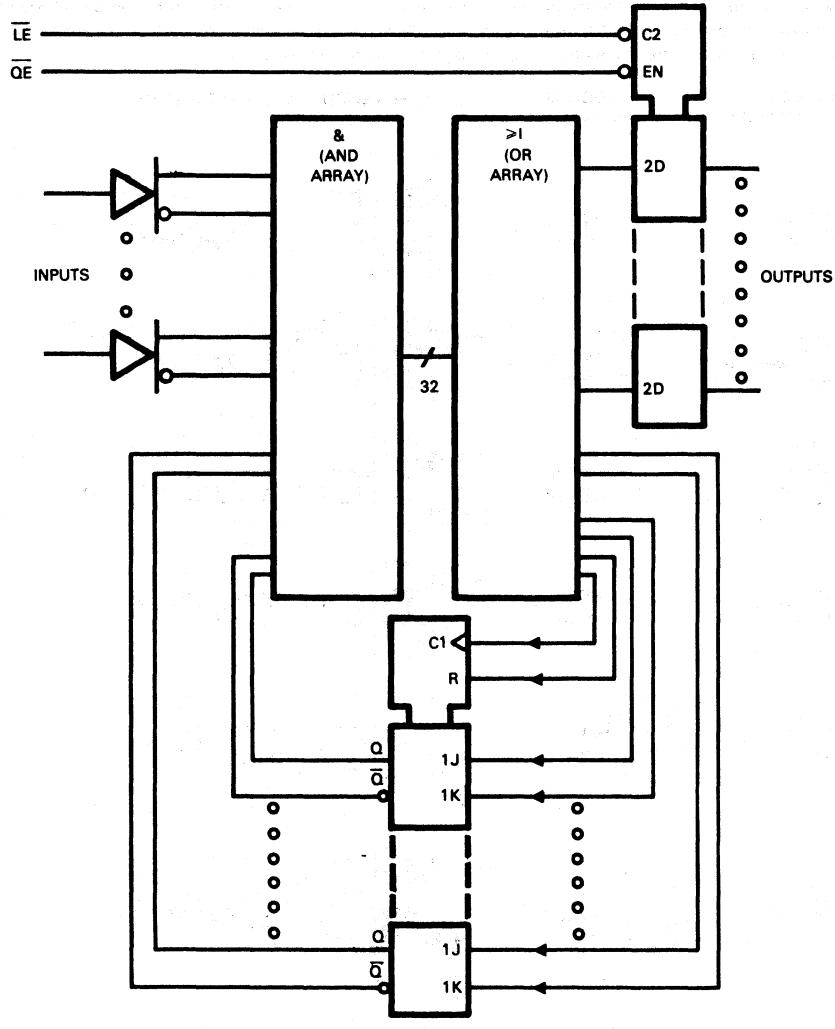
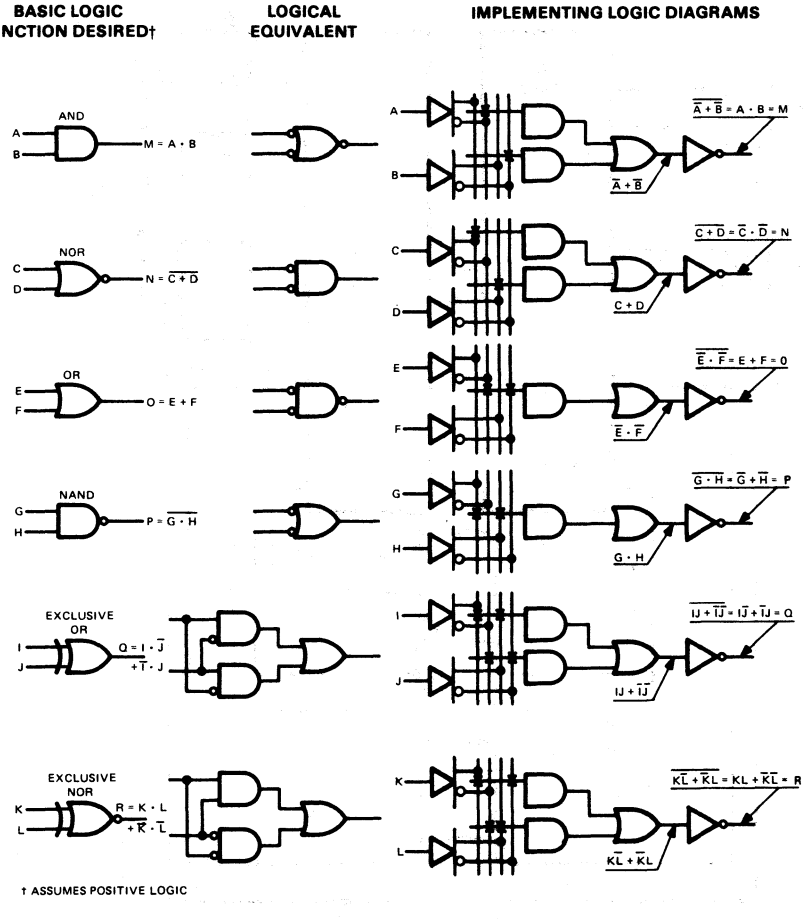

LE
QE
C2
EN
&
(AND
ARRAY)
≥1
(OR
ARRAY)
2D
INPUTS
OUTPUTS
32
2D
C1
R
Q
Q
1J
1K
Q
Q
1J
1K

FIGURE 15

LOGIC BLOCK EQUIVALENCE

Now that the individual circuit functions have been discussed, we will review the implementation of each of the basic logic functions (AND, OR, NAND, NOR, and exclusive OR). Figure 16 presents a comparison of basic logic function, the logical equivalent, and the implementing logic diagram for a nonregistered output.



† ASSUMES POSITIVE LOGIC

FIGURE 16. COMPARISON OF BASIC LOGIC FUNCTIONS

REFERENCE INFORMATION

Comprehensive comparisons of Low-Power Schottky (LS), Advanced Schottky (AS), and Advanced Low-Power Schottky (ALS), as well as details for circuit design, are presented in our Application Report Number B215, "Series 54ALS/74ALS Schottky TTL." Application Report B215, used in conjunction with the data sheets for the specific device, will allow confident designing with Field-Programmable Logic.

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PROGRAMMING FIELD-PROGRAMMABLE LOGIC

Each device data sheet includes a programming procedure that defines the conditions for programming. Programmers are commercially available for most devices with equipment for future devices in development. Listed below are some of the manufacturers of programming equipment.

- Cybernetic PGM Systems
- Data I/O
- Kontron
- Pro-Log
- Stag Systems
- Structured Design
- Curtis Electro Devices
- Valley Data Sciences
- Storey Systems
- Varix
- Sunrise Electronics

Device design has been coordinated with Data I/O and their Model 19 has been used throughout design and characterization. For a current list of certified programmers, please contact your local TI sales representative.

Programming FPLAs and FPLSs is largely manual. Computer-controlled programming capability currently exists for 20-pin Fixed-OR Arrays. Control is by means of computer software, which is available from the manufacturer. Software for 24-pin Fixed-OR Arrays is under development and will be included in later application notes.

PREPARATION AND PROGRAMMING

Regardless of the type of equipment to be used for actually programming devices (blowing fuses), the basic design and programming requirements are the same. Figure 17 presents a simplified flow chart of programming options.

Since the Fixed-OR Array affords the widest variety of parts and output options, it will be used for both the manual and computer-aided examples. First, we will describe the circuit selected for the example, then discuss the specific steps required prior to programming the parts.

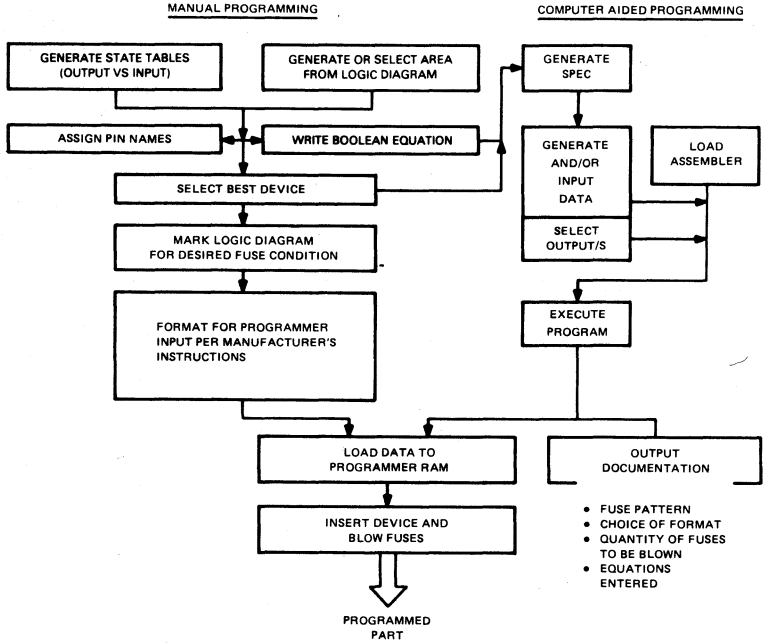

FIGURE 17. SIMPLIFIED FLOW CHART OF PROGRAMMING OPTIONS

PROGRAMMED EXAMPLE

Figure 18 is a partial schematic of the decoding portion of a commercially used video controller as implemented with standard catalog SSI logic. Circuit analysis reveals that this circuit is primarily a waveform generator designed to decode the state of the 5-bit counter. The edge-triggered latches are clocked and cleared with respect to the clock (CK) input. Figure 19 is the timing diagram generated to establish the individual waveforms. The labeling defined in the legend of Figure 18 will help understand the partitioning used to implement this circuit using Fixed-OR-Arrays. Most of the original circuit can be implemented by a direct function for function conversion, however, some rearrangement is required to take full advantage of the flexibility of the Fixed-OR-Arrays. Since the FOA has a common clock and no clear, $\overline{I}$ must be developed as shown in Figure 20.

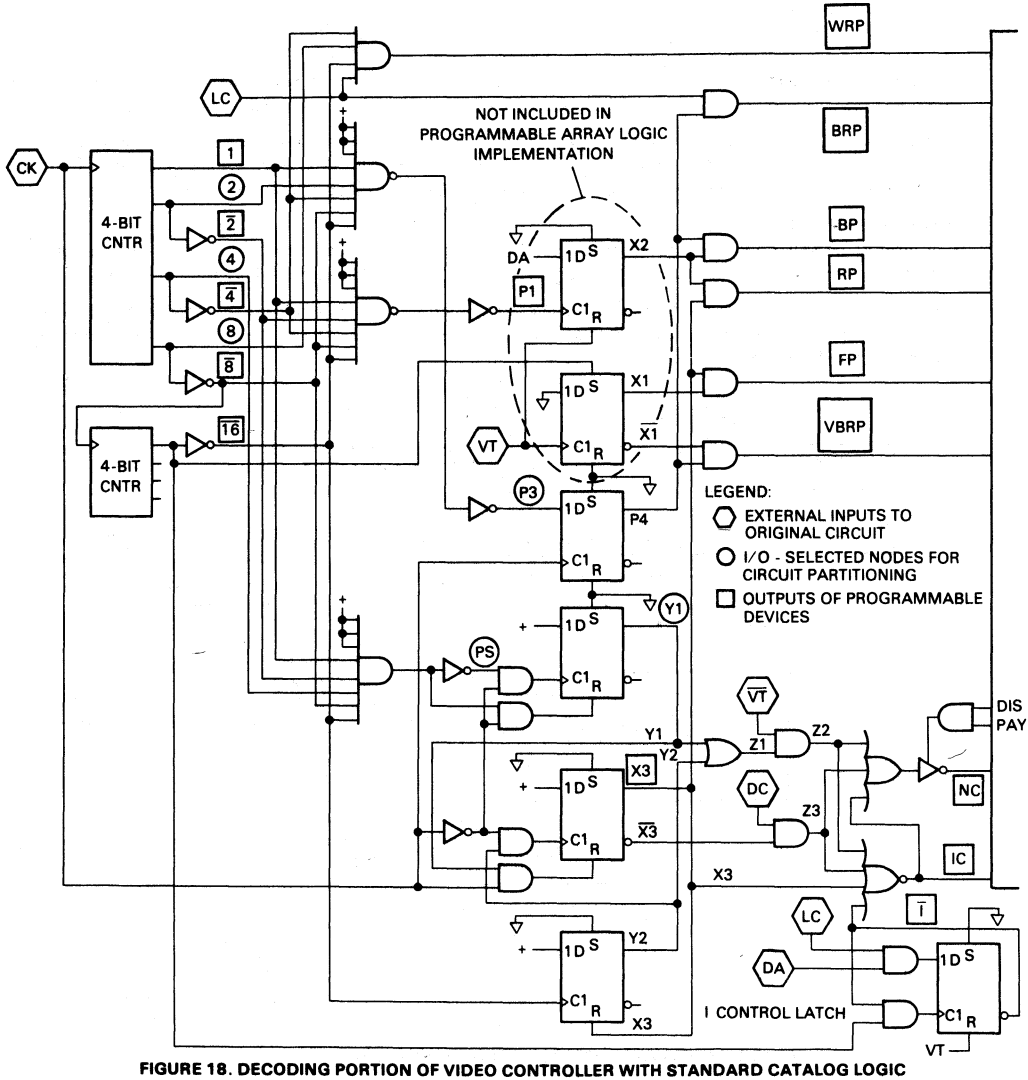

FIGURE 18. DECODING PORTION OF VIDEO CONTROLLER WITH STANDARD CATALOG LOGIC

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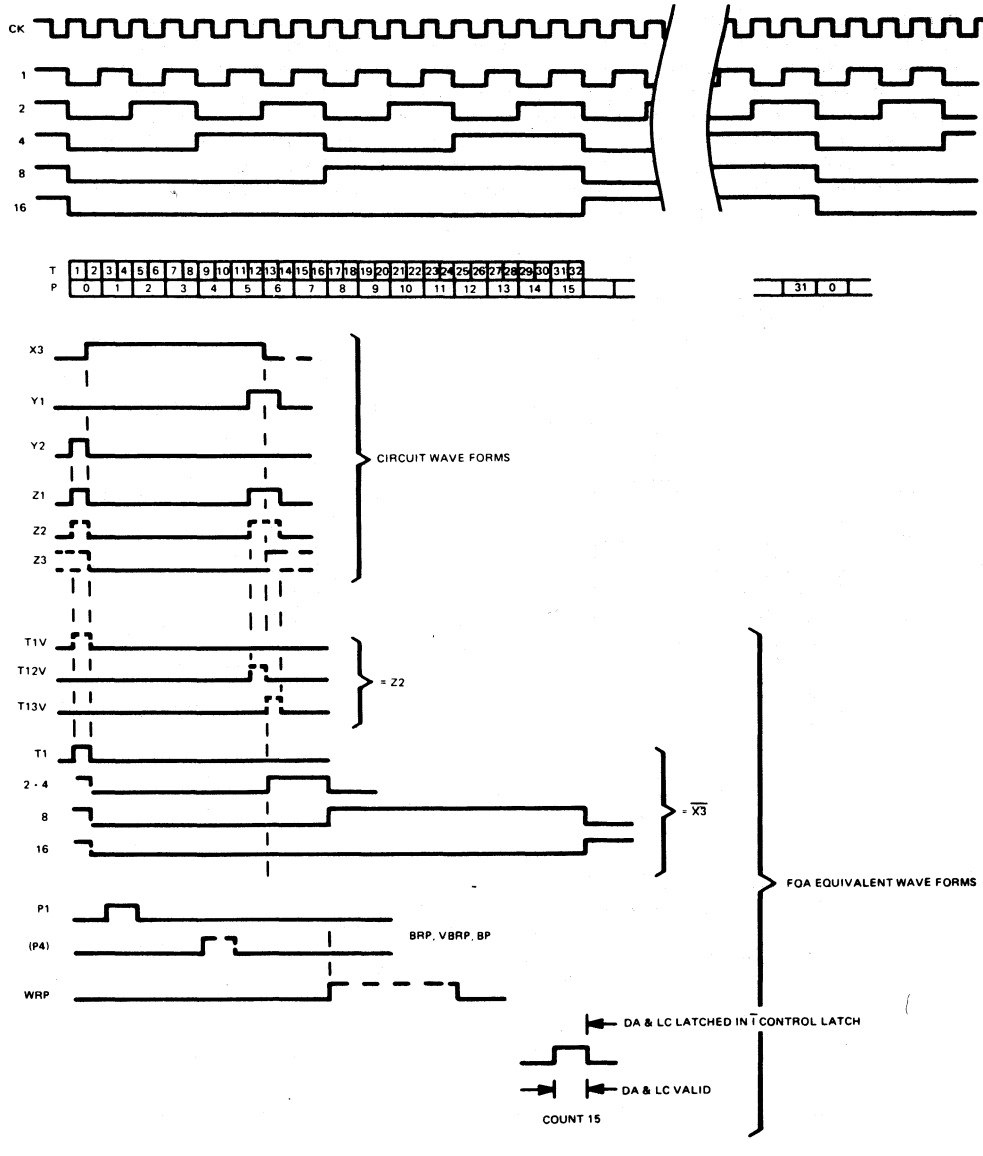

FIGURE 19. TIMING DIAGRAM FOR VIDEO CONTROLLER (SEE FIGURE 18)

PLA APPLICATIONS

By partitioning the circuit as shown in Figure 18, a pin assignment can be made and the most suited Fixed-OR Array selected. In this example, the 'PL16R6 and 'PL16L8 have been selected. The logic diagram for the equivalent circuit as implemented using the selected devices are shown in Figure 20 and Figure 21 respectively. Figure 22 presents the detailed schematic of the counter. The counter implementation is a part of the 'PL16R6 represented in Figure 20. Figure 21 is included only to complete the conversion example (programming is not shown). The combination of (1) feedback buffers as inputs with true and complement, (2) input true and complement, (3) common clock for D latches and the selectable use of each input allows the entire circuit shown in Figure 18 (excluding the one device circled) to be replaced by two array-logic devices. This results in a part count reduction of 17 to 2 (88%) and an interconnect reduction of 83% plus the reduction in printed circuit board complexity and area.

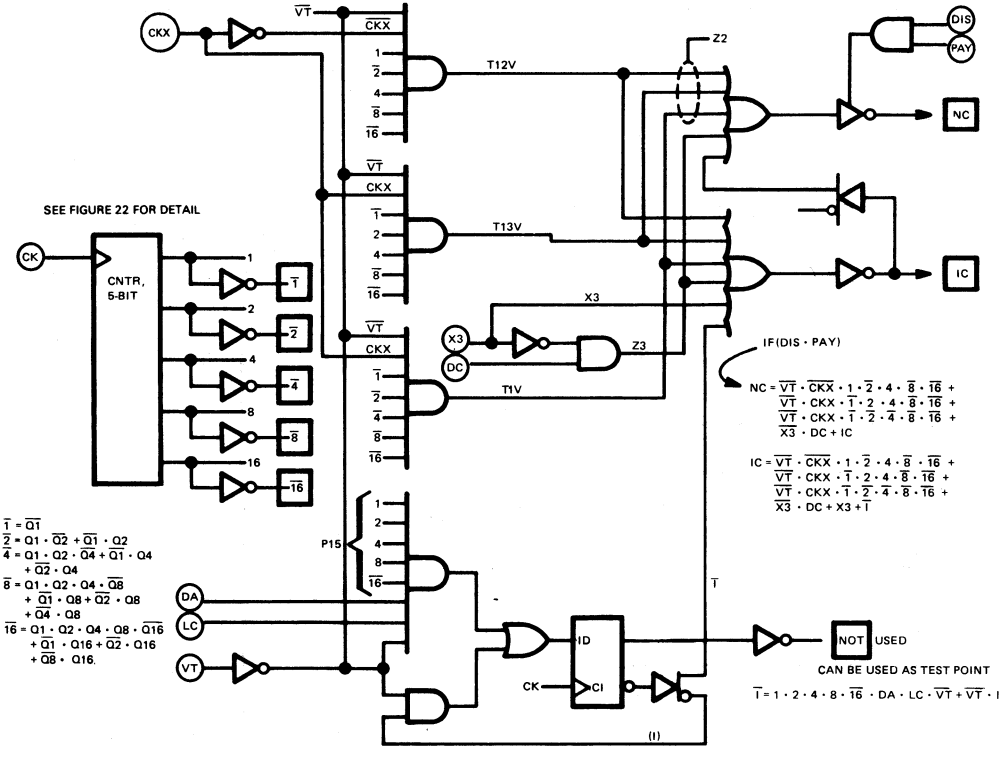

FIGURE 20. VIDEO CONTROLLER IMPLEMENTATION, DECODE NUMBER 1 FOR 'PL16R6

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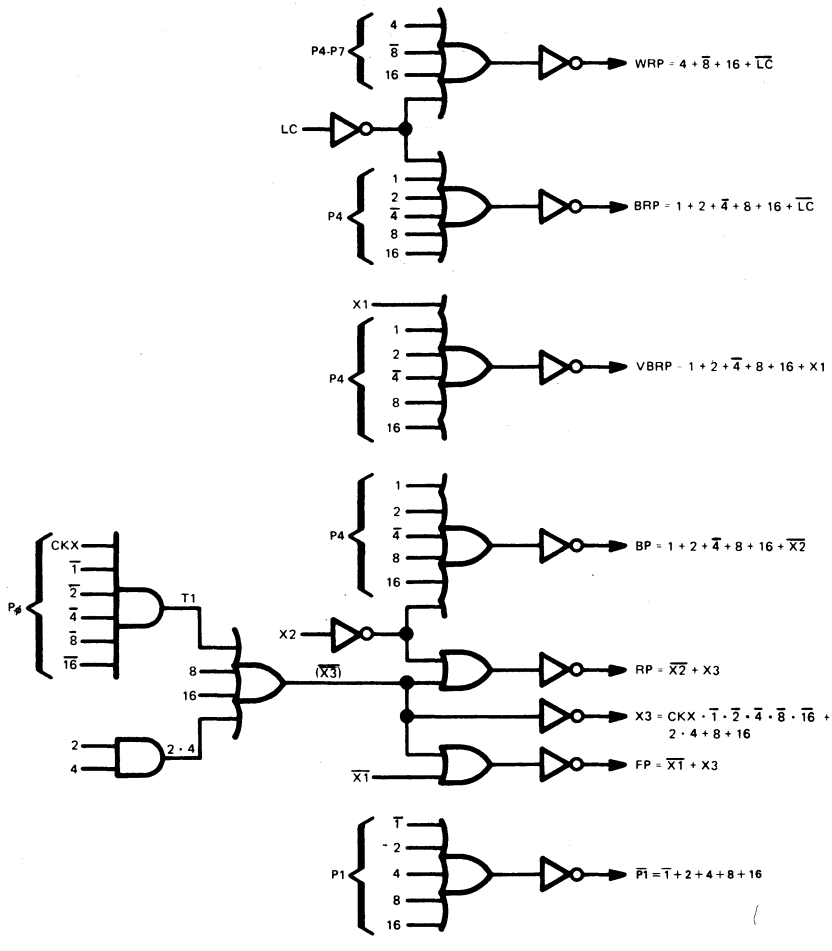

FIGURE 21. VIDEO CONTROLLER IMPLEMENTATION, DECODE NUMBER 2 FOR 'PL16L8

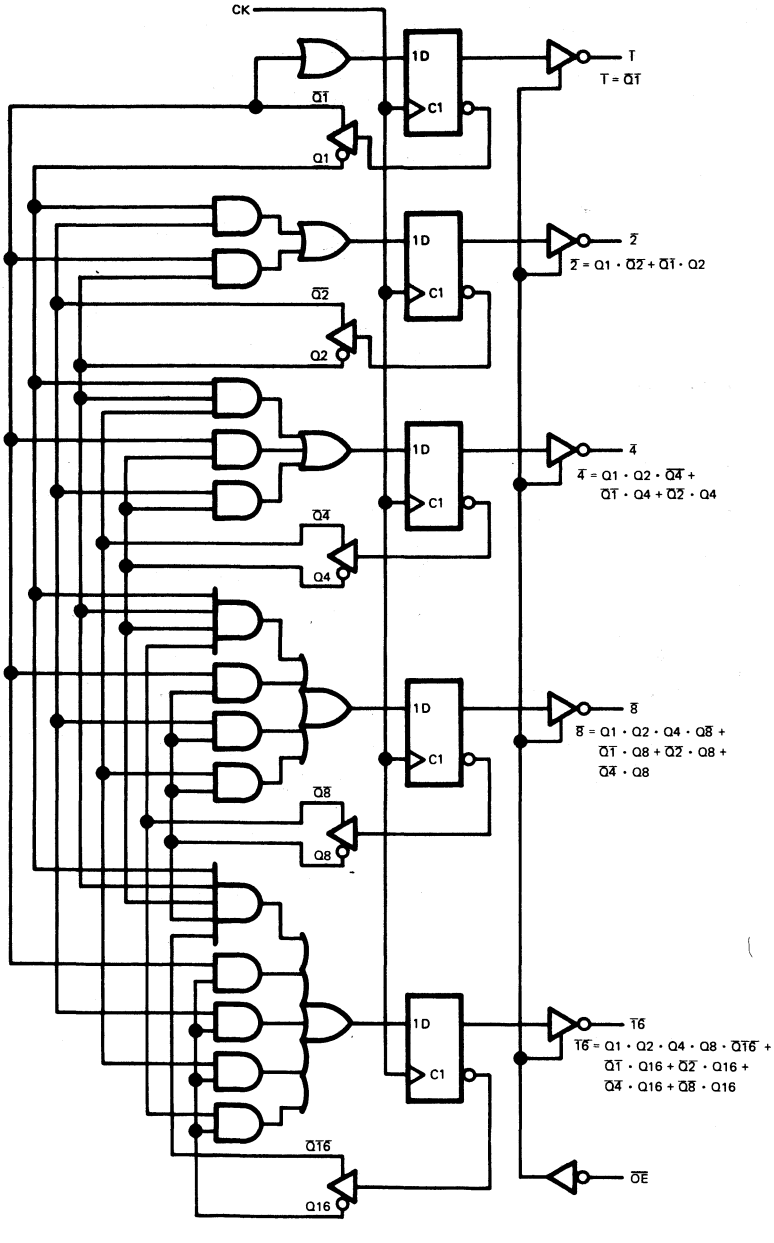

FIGURE 22. FIXED-OR ARRAY 5-BIT COUNTER IMPLEMENTATION

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MANUAL PROGRAMMING EXAMPLE

Now that logic equations have been generated in Figure 20 and Figure 21 as a result of the analysis and restructuring of the circuit implementation, we are ready to prepare for programming the devices as follows:

1. Take a copy of the logic diagram for the selected device (see Figure 23).
2. Label each output.
3. Assign names to each input. In Figure 20 the inputs are circled and the outputs enclosed by a square.
4. Mark the location of each fuse required to implement the equations. Note that all inputs to the array for outputs $\overline{1}$ through $\overline{16}$ are from the feedback buffers. Example: $\overline{2}$ on pin 17 is fed back to input lines 10 and 11.

To implement the equation $\overline{2} = Q1 \cdot \overline{Q2} + \overline{Q1} \cdot Q2$, place an X at the intersection of

INPUT LINE	PRODUCT LINE
7($Q1$)	16
10($\overline{Q2}$)	16
6($\overline{Q1}$)	17
11($Q2$)	17

NOTE: The inputs DIS and PAY are not on the original schematic. They have been used here to demonstrate (1) the simplicity of programming for three-state control, (2) the IF statement for the computer-aided program, and (3) the device versatility.

5. The preparation for programming the device is now complete except for formatting the fuse locations to comply with the input requirement of a particular programmer. Since equipment manufacturers have not yet standardized on address and data input formats, refer to the programming instructions for your particular programmer.

COMPUTER-AIDED PROGRAMMING

Programmers are available with interface packages that will allow the simplification of inputting data. Options vary from the ability to output from paper tape to direct terminal or computer control. Many data formats are also available for the remote controlled programmers. Examples of acceptable formats include HEX, BHLF, and BPNP.

NOTE: Since the programming results cannot be verified after the security fuses are blown, a separate test fixture is required to blow these two fuses (see the data sheet for instructions).

PLA APPLICATIONS

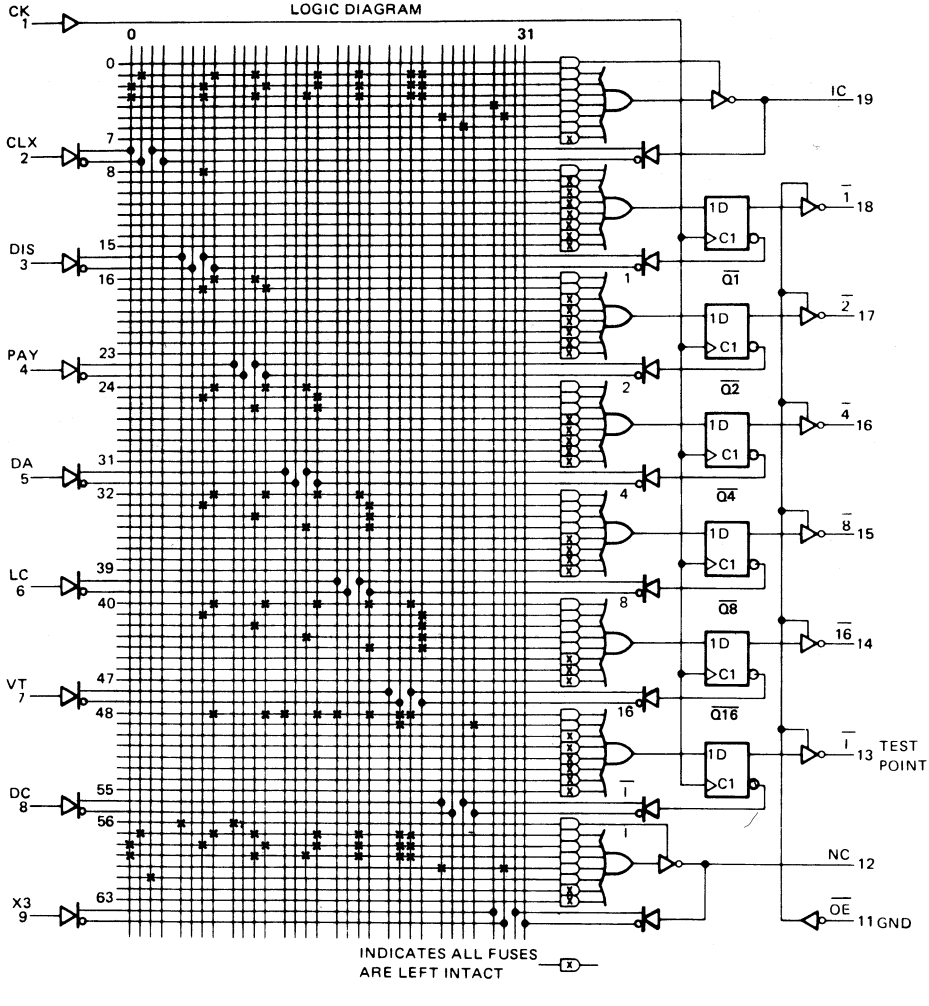
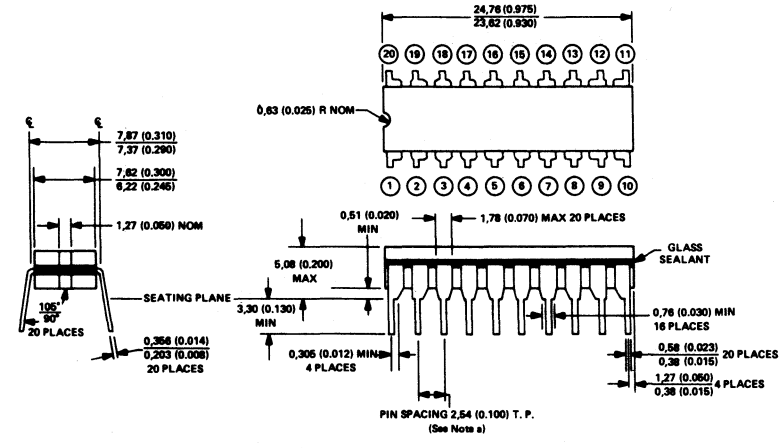


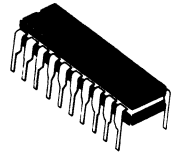
FIGURE 23. 'PL16R6 LOGIC DIAGRAM

MECHANICAL DATA

J ceramic dual-in-line packages

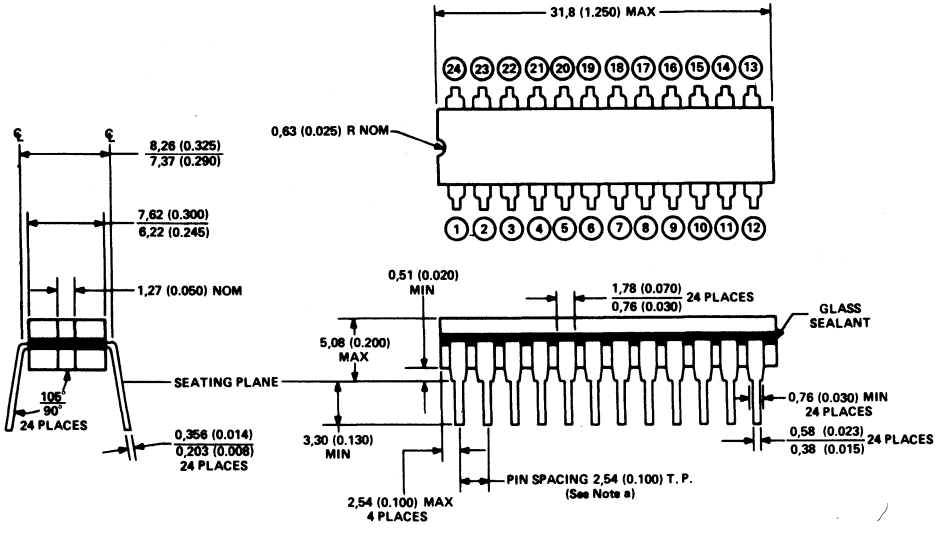
20-PIN J CERAMIC





ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

24-PIN JT CERAMIC



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

NOTE: a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

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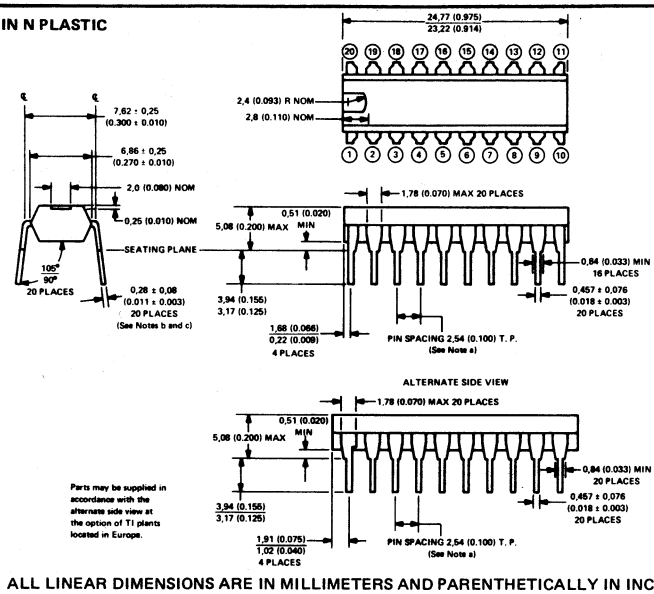
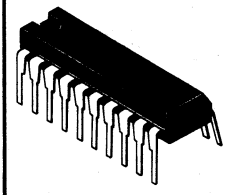
N plastic dual-in-line packages

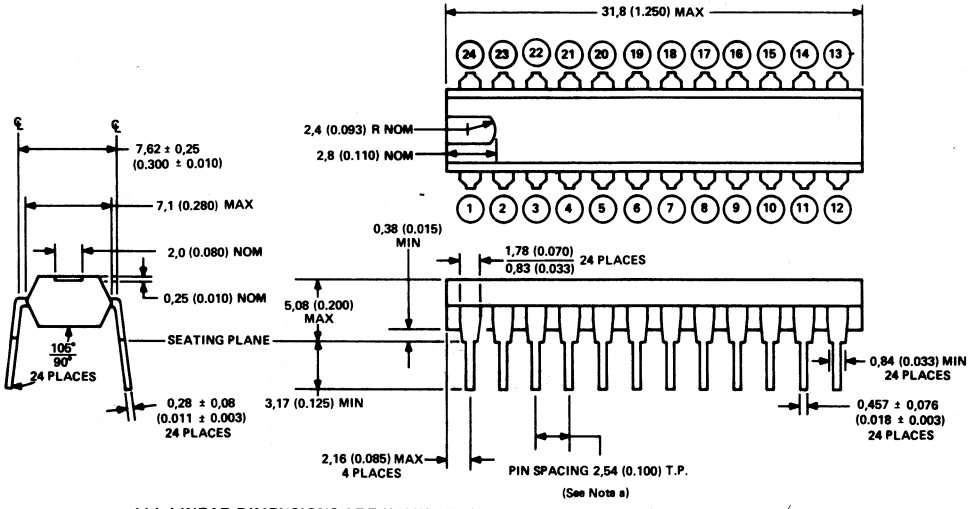
20-PIN N PLASTIC





ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

24-PIN NT PLASTIC



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

NOTES: a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

b. This dimension does not apply for solder-dipped leads.

c. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

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