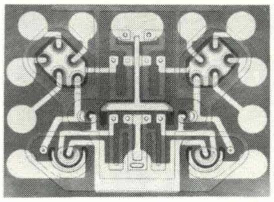
LOAD-COMPENSATED DTL INTEGRATED CIRCUIT

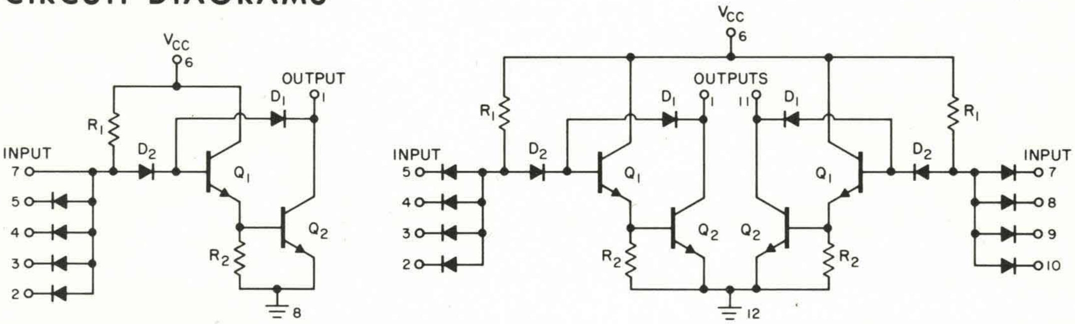
TYPES ZA01A AND ZA02A SINGLE AND DUAL NAND/NOR GATES

ONE OR TWO DIODE-TRANSISTOR LOGIC CIRCUITS IN A SINGLE CHIP OF SILICON

- Low Power-Speed Product - 60 pico-watt-sec
- Operates From Single Power Supply
- Typical Propagation Delay Time - 12 nsec
- Typical Power Dissipation - 5mw
- High Fan-Out-5 at -55 to 70°C



CIRCUIT DIAGRAMS



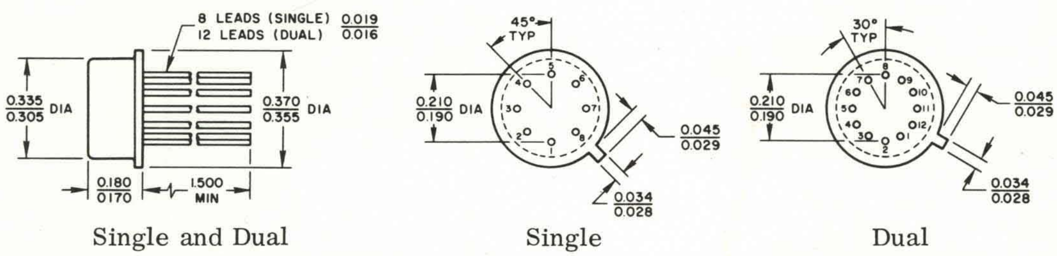
Single   Dual

The logic operation of this circuit is identical with conventional DTL. The unique emitter-follower diode-clamp arrangement provides high-speed switching, high gain and low-power operation.

MECHANICAL DATA

Single gate in modified 8-lead TO-5 package
Dual gate in modified 12-lead TO-5 package
(both available in flat package by July 1963)

Pin 8 (single) and pin 12 (dual) are in electrical contact with the case.



Single and Dual   Single   Dual

All dimensions in inches

PRODUCT CONDITIONING

Long life and mechanical reliability are ensured by subjecting each unit to the following tests:

- High Temperature Storage: 72 hours at 200°C
- Thermal Shock: +200°C to -65°C for 5 Cycles
- 30,000G Centrifuge in the Y_1 Plane
- Helium and Gross Leak Tests for Hermeticity
- Post-Bake Clean-Up to Assure Solderability

Siliconix incorporated

1140 West Evelyn Avenue
Sunnyvale, California
(408) 245-1000

OPERATIONAL CHARACTERISTICS AT V_{CC}=4v

Characteristic	Min	Typ	Max	Unit
Fan-in at -55 to +70°C			4†	
Fan-out at T_A = 70°C, ΔV = 0.1 v (see Note 1)			5	
Worst-Case DC Stability, ΔV, at 70°C Fan-out = 5	100			mv
Power Dissipation per Gate at 25°C (see Note 2)		5		mw
Average Propagation Delay per Gate (see pp. 3,4), When Fan-in = 1 and Fan-out = 1, at T_A = +25°C T_A = -55°C T_A = 70°C		 12 14 14	 15	 nsec nsec nsec

† Diode array available for single gate to improve fan-in.

ABSOLUTE MAXIMUM RATINGS AT 25° C

Power Supply Voltage, V_{CC}	6 v
Gate Input Voltage	6 v
Gate Output Voltage (Input Grounded)	6 v
Operating Temperature Range	-55 to +70°C
Storage Temperature Range	-55 to +200°C

STATIC CHARACTERISTICS (WORST-CASE) V_{CC}=4v

(See opposite page for test conditions)

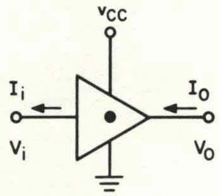
Characteristic		Temperature			Unit
		-55°C	+25°C	+70°C	
I_{OFF}	Maximum Output Current with Gate OFF	5*	10*	20*	μa
$I_{R(max)}$	Maximum Reverse Current per Input Diode	0.05*	0.10*	0.30*	μa
$I_{i(max)}$	Maximum Input Current with Gate OFF (Max Load Presented to Driving Stage), with V_i = V_F -100 mv	1.15*	1.30*	1.35*	ma
V_F	Maximum Voltage at any Input that will Ensure Turn-OFF (Max False Voltage)	1.38*	1.14*	0.95*	v
$V_{o(max)}$	Maximum Output Voltage When Fully Loaded at: Fan-out = 5 Fan-out = 25	 1.02 1.30*	 0.94*	 0.85*	 v v
V_T	Minimum Input Voltage that will Ensure Turn-ON (Minimum True Voltage) Fan-out = 5	2.00	1.78	1.62	v
ΔV	DC Stability Margin (V_F - V_o) Fan-out = 5	0.36*	0.20*	0.10*	v

*Characteristics so designated are tested on every unit

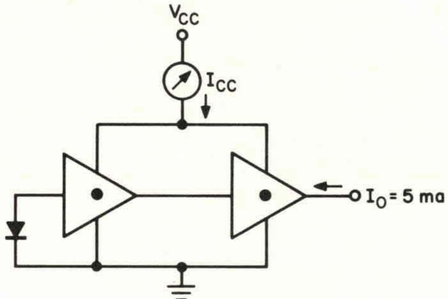
Notes:

1. This is the maximum fan-out permissible for worst-case logic design with a 4 v power supply when the d-c stability ΔV margin is 0.1 v.
2. Power dissipation is defined as power supply voltage times average current drawn per gate. (See test circuit, p. 3).

MEASUREMENT OF STATIC CHARACTERISTICS



General Test Circuit



Power Dissipation Test Circuit

Power dissipation per gate = $\frac{V_{CC} \times I_{CC}}{2}$

As measured above, the power dissipation is the average between the OFF stage and typically loaded ON stage and is equivalent to a 50% duty cycle for a single gate.

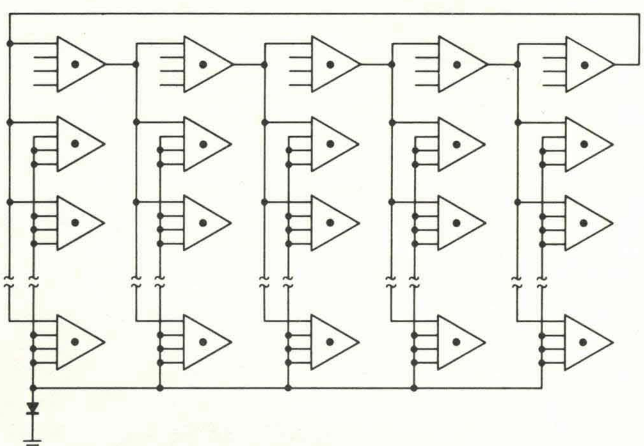
TEST CONDITIONS

Characteristic to be Determined	Set or Measure These Characteristics - e.g., to Determine V_F at 25°C, Set I_o at 10 μa, V_o at 4 v, Measure V_i.				Other Conditions
	I_i Input Current	V_i Input Voltage	I_o Output Current	V_o Output Voltage	
V_F		Measure	I_{OFF}*	4 v	Free inputs connected to V_{CC}
$I_{i(max)}$	Measure	V_F* -100 mv		4 v	Free inputs connected to V_{CC}
$I_{R(max)}$	Measure	4 v			Open circuit output One input grounded
$V_{o(max)}$	F.I. [I_{OFF}* + (F.O. - 1) $I_{R(max)}$*]		F.O. x $I^*_{i(max)}$	Measure	
V_T	I_{OFF} + (F.O. -1) $I_{R(max)}$*	Measure	F.O. x $I^*_{i(max)}$		Free inputs open

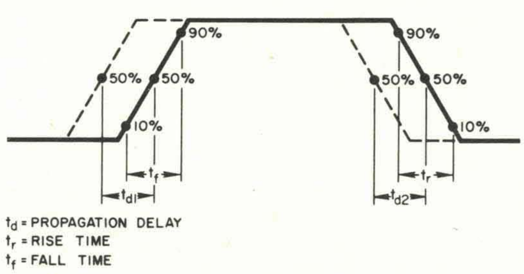
F.I. = fan-in F.O. = fan-out

* Definitions and values for temperatures from -55 to + 70°C obtained from table on opposite page.

MEASUREMENT OF DYNAMIC CHARACTERISTICS



Test Circuit for Propagation Delay/Fan-out Measurements



Waveform propagated through two stages. Average propagation delay per stage

$$t_{d(avg)} = \frac{t_{d1} + t_{d2}}{4}$$

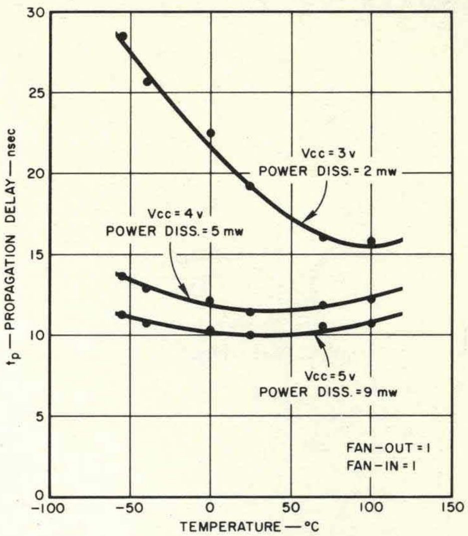
Waveforms and Time Delays

DYNAMIC CHARACTERISTICS

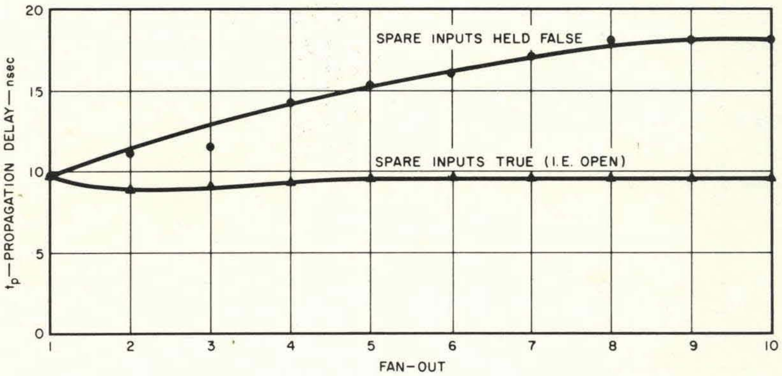
TIME	FAN-OUT			UNIT
	1	10 (FREE INPUTS OPEN)	10 (FREE INPUTS HELD FALSE)	
t_r (0-1 TRANSIENT)	10	18	30	nsec
t_f (1-0 TRANSIENT)	5	20	20	nsec

Typical Rise and Fall Times

V_{CC} = 4 volts, + 25°C

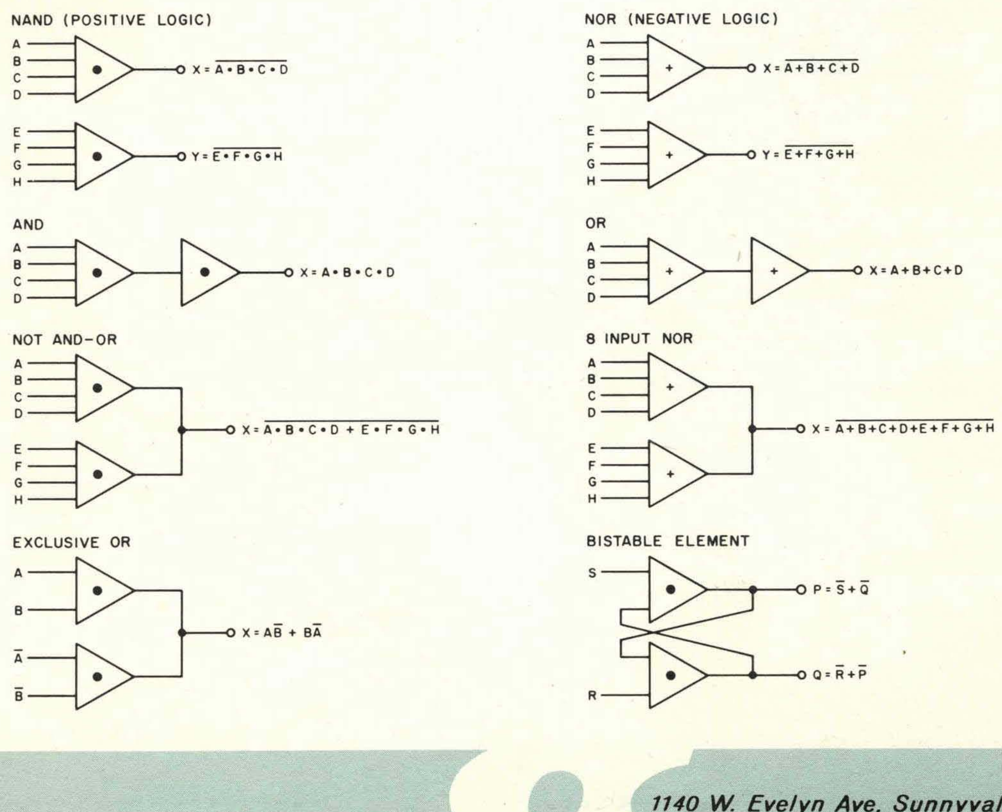


Typical Propagation Delay vs. Voltage and Temp



Effect of Loading on Propagation Delay

LOGIC DIAGRAMS



Printed in USA
May 1, 1963

1140 W. Evelyn Ave. Sunnyvale, Calif. (408) 245-1000

Siliconix incorporated