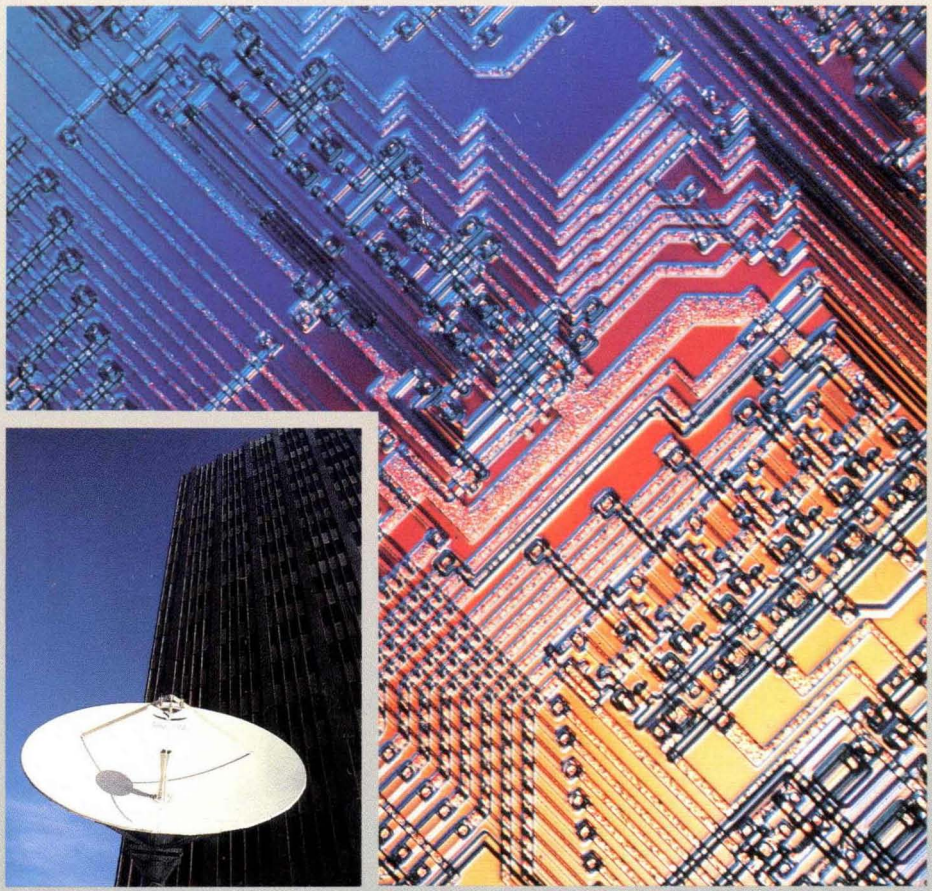
SIEMENS

Consumer IC

Data Book 1987/88



SIEMENS

Consumer IC

1987/88

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Consumer IC

Data Book 1987/88

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Summary of Types

Summary of Types

1.1 Types in Alphanumerical Order

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TDA 4605	SMPS controller	615
TDA 4814	Sinewave controller	635
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SDA 5200 N	6 bit A/D converter	263
SDA 5200 S	6 bit A/D converter	269
SDA 6020	6 bit A/D converter	275
SDA 8005	8 bit D/A converter	281
SDA 8010	8 bit A/D converter	293

Audible Signal Devices

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SAB 0601	Single tone chime	81
SAB 0602	Dual tone chime	81
SAE 0700	Audible signal device	89

IC's for Radio Communications

TBB 042 G	Mixer	337
TBB 200 ;G	PLL frequency synthesizer	343
TBB 469	FM receiver	359
TBB 1469	FM receiver	365
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S 353	Programmable diode matrix	65
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DC Motor Control

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SDA 2060	Microcontroller (6k ROM)	121
SDA 2080	Microcontroller (8k ROM)	121
SDA 2082	Microcontroller	131
SDA 2110	Microcontroller	145

Nonvolatile Memories

SDA 2506	128 x 8 EEPROM	201
SDA 2516	128 x 8 EEPROM IIC bus	207
SDA 2526	256 x 8 EEPROM IIC bus	213

Display Drivers

SDA 2131	Static LED driver	179
UAA 170	LED driver for dot display	911
UAA 180	LED driver for bar display	919

Video Sound IF

TDA 4282 T	Quasi parallel IF	553
TDA 5400-2	Video IF w/AFC	699
TDA 5830-2	Video IF & Q-P sound	759
TDA 5835	Video IF & Q-P w/AFC	775
TDA 5850	Video switch	791
TDA 6000	Video IF w/synch demodulator	795

Miscellaneous Entertainment

TDA 5660 P	VHF/UHF modulator	705
TDA 5660 X	VHF/UHF modulator	749

SMPS Control

TDA 4600-3	SMPS controller	573
TDA 4601 ;D	SMPS controller	589
TDA 4605	SMPS controller	615

Radio Tuners

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Radio IF		
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TDA 4210-3	FM IF for car radios	541
FM Stereo Decoders		
TCA 4500 A	FM Stereo decoder	495
TCA 4511	FM PLL stereo decoder	499
Audio Power Amplifiers		
TDA 1037	Audio power amplifier	507
TDA 4930	Audio power amplifier 2 x 10W	671
TDA 4935	Audio power amplifier 2 x 15W	685
Tone/Volume Control		
TDA 4292	DC Stereo tone control	553
TDA 6200	Sound control, IIC bus	799

General Information

2.1 Type-designation code for ICs

IC type designations are based on the European Pro Electron system. The code system is explained in the Pro Electron brochure D 15*), edition 1985.

*) Available from Pro Electron, Avenue Louise, 430 (B.12)
B-1060 Brussels, Belgium

2.2 Mounting instructions

2.2.1 Plastic package

The pins of the cases are bent downwards by an angle of 90° and fit into holes with a diameter of between 0.7 and 0.9 mm spaced 2.54 mm apart. The dimension x is given in the corresponding drawing.

The bottom of the package will not touch the PC board after insertion because the pins have shoulders just below the package **(see figure 1).**

After insertion of the package into the PC board it is advisable to bend the ends of two pins at an angle of approx. 30° to the board so that the package does not have to be pressed down during soldering. Plastic packages are soldered on that side of the PCB facing away from the package.

The maximum permissible soldering temperature is 300 °C (max. 5 s) for manual soldering and 260 °C (max. 10 s) for dip soldering and wave soldering.

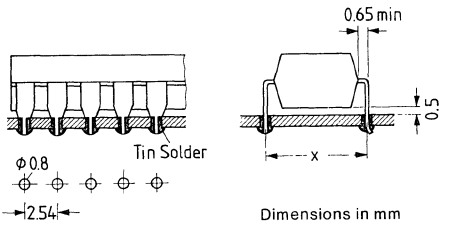


Figure 1

2.2.2 Power package with 5, 7, or 9 pins

Power packages generally have wider pins than stated in paragraph 2.2.1, meaning that the hole diameter on the PCB must be between 1.1 and 1.8 mm. If the pins are bent, there should be no stress between the pins and the package. The minimum distance between the package and the bending point is 2 mm.

Refer to paragraph 2.2.1 for soldering temperatures.

2.2.3 Plastic packages (SO and PLCC) for surface mounting (SMD)

Iron soldering:	soldering temperature 300 °C for max. 5 s; minimum distance between package and soldering point 1.5 mm package temperature max. 150 °C; no mechanical stress on the pins
Vapor phase soldering:	soldering temperature 215 °C, max. soldering time 30 s
Wave soldering: (pins and package are dipped into the tin bath)	soldering temperature 260 °C, max. soldering time 3 s.

2.2.4 5 H 8 DIN 41873 and similar packages

The package may be mounted in any position. The ends of the pins may be kinked up to a distance of 1.5 mm from the bottom of the package to suit the hole spacing **(fig. 2).**

Pins that are too long should be clipped before soldering.

Iron or dip soldering may be employed.

Maximum soldering duration for dip soldering at 250 °C bath temperature t_{max} = 5 s
at 300 °C bath temperature t_{max} = 4 s
for iron soldering at 250 °C iron temperature t_{max} = 15 s
at 300 °C iron temperature t_{max} = 12 s
at 350 °C iron temperature t_{max} = 8 s

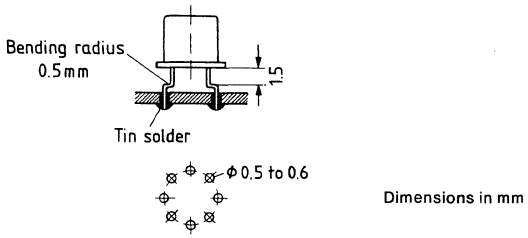


Figure 2

2.2.5 Other points to note

Ensure that no current is able to flow between the solder bath or soldering iron and the PCB. It is advisable to ground the pins that are to be soldered as well as the solder bath or soldering iron.

When they are being prepared and inserted in a PCB, circuits should be protected against static charging. Under no circumstances may the components be removed or inserted whilst the operating voltage is switched on.

The increase in chip temperature during the soldering process results in a temporary increase in electrostatic sensitivity of integrated circuits. Special precautions should therefore be taken against line transients, e.g. through the switching of inductances on magnetic chutes, etc.

2.2.6 MIKROPACK (SMD)

MIKROPACK components are delivered on film reels.

Mounting suggestions

a) We recommend vapor phase soldering: soldering temperature 215 °C, soldering time max. 30 s

b) For prototypes and small quantities (up to approximately 50.0 items/y), the hot table soldering method can also be used (fig. 3).

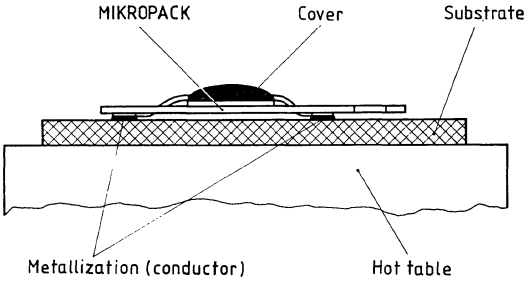


Figure 3

Required equipment and accessories

- cutting device
- hot table, temperature regulated (e.g. Weld-Equip, Unitek)
- stereo microscope (e.g. Wild, Zeiss, magnification 6 · · · 40 times)
- substrate material: epoxy resin; hard paper; ceramic (thick thin film)

Soldering data

- soldering temperature: 210 °C max.
- solder coating on substrate: Pb/Sn (e.g. 60/40) wave-tinned or electrodeposited
- soldering time: approx. 10 s
- flux: e.g. colophony, dissolved in alcohol
- cleaning agents (as required): e.g. Freon TP-35, TE, TF

c) For large quantities (e.g. more than 50.0 items/y) bar soldering is also suitable.

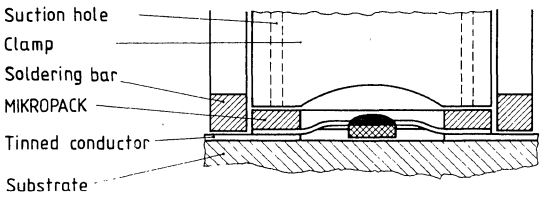


Figure 4

Required equipment

- soldering equipment (e.g. Weld-Equip, Farco, Jade)
- substrate material: epoxy resin; hard paper; flexible materials, e.g. polyamide

Soldering data

- soldering temperature: 210 °C max.
- solder coating on the substrate: Pb/Sn (e.g. 60/40), wave-tinned or electro-deposited
- soldering time: approx. 2 s
- flux: e.g. colophony dissolved in alcohol
- cleaning agents (as required): e.g. Freon TP-35, TE, TF

2.3 Processing guidelines for ICs

Integrated circuits (ICs) are **e**lectro**s**tatic-**s**ensitive (ESS) devices. The requirement for greater packing density has led to increasingly small structures on semiconductor chips, with the result that today every IC, whether bipolar, MOS, or CMOS, has to be protected against electrostatics.

MOS and CMOS devices generally have integrated protective circuits and it is hardly possible any more for them to be destroyed by purely static electricity. On the other hand, there is acute danger from **e**lectro**s**tatic **d**ischarges (ESD).

Of the multitude of possible sources of discharge, charged devices should be mentioned in addition to charged persons. With low-resistive discharges it is possible for peak power amounting to kilowatts to be produced.

For the protection of devices the following principles should be observed:

a) Reduction of charging voltage, below 200 V if possible.
   Means which are effective here are an increase in relative humidity to $\geq 60\%$ and the replacement of highly charging plastics by antistatic materials.
b) With every kind of contact with the device pins a charge equalization is to be expected. This should always be highly resistive (ideally $R = 10^6$ to $10^8\ \Omega$).

All in all this means that ICs call for special handling, because uncontrolled charges, voltages from ungrounded equipment or persons, surge voltage spikes and similar influences can destroy a device. Even if devices have protective circuits (e.g. protective diodes) on their inputs, the following guidelines for their handling should nevertheless be observed.

2.3.1 Identification

The packing of ESS devices is provided with the following label by the manufacturer: 

2.3.2 Scope

The guidelines apply to the storage, transport, testing, and processing of all kinds of ICs, equipped and soldered circuit boards that comprise such components.

2.3.3 Handling of devices

1. ICs must be left in their containers until they are processed.
2. ICs may only be handled at specially equipped work stations. These stations must have work surfaces covered with a conductive material of the order of 10^6 to $10^9\ \Omega$/cm.
3. With humidity of $> 50\%$ a coat of pure cotton is sufficient. In the case of chargeable synthetic fibers the clothing should be worn close-fitting. The wrist strap must be worn snugly on the skin and be grounded across a resistor of 50 to 100 kΩ.

4. If conductive floors, $R = 5 \times 10^4$ to 10^7 Ω are provided, further protection can be achieved by using so-called MOS chairs and shoes with a conductive sole ($R \approx 10^5$ to 10^7 Ω).
5. All transport containers for ESS devices and assembled circuit boards must first be brought to the same potential by being placed on the work surface or touched by the operator before the individual devices may be handled. The potential equalization should be across a resistor of 10^6 to 10^8 Ω.
6. When loading machines and production devices it should be noted that the devices come out of the transport magazine charged and can be damaged if they touch metal, e.g. machine parts.

   Example 1) conductive (black) tubes.
   The devices may be destroyed in the tube by charged persons or come out of the tube charged if this is emptied by a charged person.
   Conductive tubes may only be handled at ESS work stations (high-resistance work-station and person grounding).

   Example 2) anti-static (transparent) tubes.
   The devices cannot be destroyed by charged persons in the tube (there may be a rare exception in the case of custom ICs with unprotected gate pins). The devices can be endangered as in 1) when the tube is emptied if the latter, especially at low humidity, is no longer sufficiently anti-static after a long period of storage (> 1 year).

   In both cases damage can be avoided by discharging the devices across a grounded adapter of high-resistance material ($\approx 10^6$ to 10^8 Ω/cm) between the tube and the machine.

   The use of metal tubes – especially of anodized aluminum – is not advisable because of the danger of low-resistance device discharge.

2.3.4 Storage

ESS devices should only be stored in identified locations provided for the purpose. During storage the devices should remain in the packing in which they are supplied. The storage temperature should not exceed 60 °C.

2.3.5 Transport

ESS devices in approved packing tubes should only be transported in suitable containers of conductive or longterm anti-static-treated plastic or possibly unvarnished wood. Containers of high-charging plastic or very low-resistance materials are in like manner unsuitable.

Transfer cars and their rollers should exhibit adequate electrical conductivity ($R < 10^6$ Ω). Sliding contacts and grounding chains will not reliably eliminate charges.

2.3.6 Incoming inspection

In incoming inspection the above guidelines should be observed. Otherwise any right to refund or replacement if devices fail inspection may be lost.

2.3.7 Material and mounting

1. The drive belts of machines used for the processing of the devices, in as much as they come into contact with them (e.g. bending and cutting machines, conveyor belts), should be treated with anti-static spray (e.g. anti-static spray 100 from Kontaktchemie). It is better, however, to avoid the contact completely.
2. If ESS devices have to be soldered or desoldered manually, soldering irons with thyristor control may not be used. Siemens EMI-suppression capacitors of the type B 81711-B31...-B36 have proven very effective against line transients.
3. Circuit boards fitted and soldered with ESS devices are always to be considered as endangered.

2.3.8 Electrical tests

1. The devices should be processed with observation of these guidelines. Before assembled and soldered circuit boards are tested, remove any shorting rings.
2. Test sockets must not be conducting any voltage when individual devices or assembled circuit boards are inserted or withdrawn, unless works' specifications state otherwise. Ensure that the test devices do not produce any voltage spikes, either when being turned on and off in normal operation or if the power fuse blows or other fuses respond.
3. Signal voltages may only be applied to the inputs of ICs when or after the supply voltage is turned on. They must be disconnected before or when the supply voltage is turned off.
4. Observe any notes and instructions in the respective data books.

2.3.9 Packing of assembled PC boards or flatpack units

The packing material should exhibit low volume conductivity:
$10^5\ \Omega/cm < \rho < 10^{10}\ \Omega/cm$.

In most cases – especially with humidity of $> 40\%$ – this requirement is fulfilled by simple corrugated board. Better protection is obtained with bags of conductive polyethylene foam (e.g. RCAS 1200 from Richmond of Redlands, California).

One should always ensure that boards cannot touch.

In special cases it may be necessary to provide protection against strong electric fields, such as can be generated by conveyor belts for example. For this purpose a sheath of aluminum foil is recommended, although direct contact between the film and the PCB must be avoided. Cardboard boxes with an aluminum-foil lining, such as those used for shipping our devices, are available from Laber of Munich.

2.3.10 Ultrasonic cleaning of ICs

The following recommendation applies to plastic packages. For cavity packages (metal and also ceramic) separate regulations have to be observed.

Freon and isopropyl alcohol (trade name: propanol) can be used as solvents. These solvents can also be used for plastic packages because they do not eat into the plastic material.

An ultrasonic bath in double halfwave operation is advisable because of the low component stress.

The ultrasonic limits are as follows:

sound frequency	f	>40 kHz
exposure	t	<2 min
alternating sound pressure	p	<0.29 bar
sound power	N	<0.5 W/cm²/liter

2.4 Data classification

Maximum ratings

Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics will apply at $T_A = 25\,°C$ and for the given supply voltage.

Operating range

In the operating range the functions given in the circuit description will be fulfilled.

2.5 Quality Assurance

2.5.1 Quality Assurance System

The high quality and reliability of integrated circuits from Siemens is the result of a carefully arranged production which is systematically checked and controlled at each production stage.

The procedures are subject to a quality assurance system; full details are given in the brochure 'Siemens Quality Assurance System — Integrated Circuits' (SQS-IC).

Figure 1 shows the most important stages of the "SQS-IC". A quality assurance (QA) department which is independent of production and development, is responsible for the selected control measures, acceptance procedures, and information feedback loops. This department has state-of-the-art test and measuring equipment at its disposal, works according to approved methods of statistical quality control, and is provided with facilities for accelerated life and environmental tests used for both qualification and routine monitoring tests.

The latest methods and equipment for preparation and analysis are employed to achieve continuity of quality and reliability.

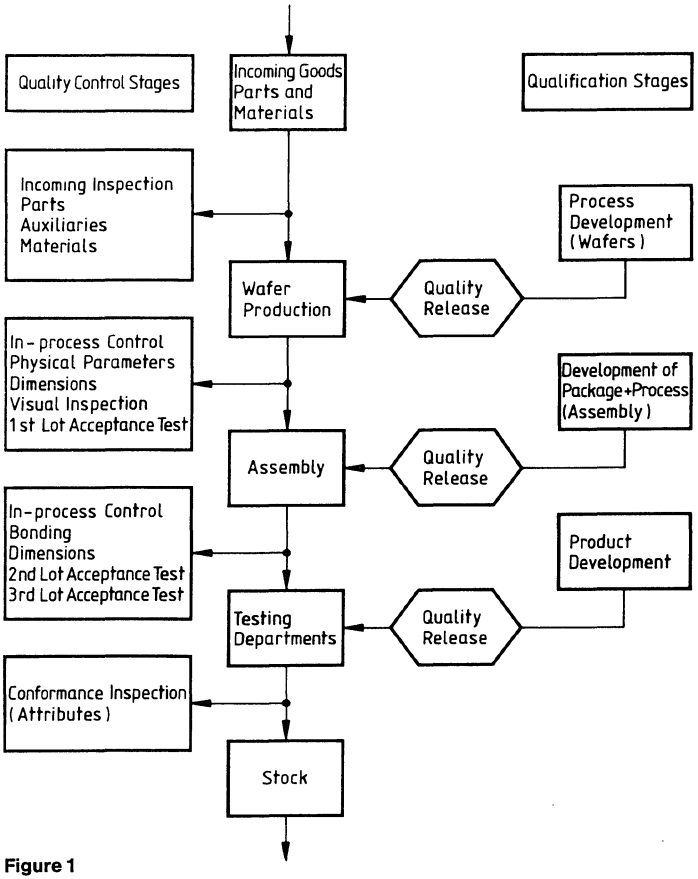


Figure 1

2.5.2 Conformance

Each integrated circuit is subjected to a final test at the end of the production process. These tests are carried out by computer-controlled, automatic test systems because hundreds of thousands of operating conditions as well as a large number of static and dynamic parameters have to be considered. Moreover, the test systems are extremely reliable and reproducible. The quality assurance department carries out a final check in the form of a lot-by-lot sampling inspection to additionally ensure this minimum percent defectives as well as the acceptable quality level (AQL). Sampling inspection is performed in accordance with the inspection plans of DIN 40080, as well as of the identical MIL-STD-105 or IEC 410.

The table shows the results of such sampling inspections performed with hundreds of thousands of ICs during 1985. These results correspond to the average outgoing quality (AOQ), and are specified as defectives per million (DPM).

	Inoperatives AOQ (DPM)	Sum of electrical defectives AOQ (DPM)	Sum of mechanical defectives AOQ (DPM)
SSI/MSI ≤ 1000 gate functions	40	200	100
LSI/VLSI ≥ 1000 gate functions	120	400	200

2.5.3 Reliability

2.5.3.1 Measures Taken during Development

The reliability of ICs is already considerably influenced at the development stage. Siemens has, therefore, fixed certain design standards for the development of circuit and layout, specifying e.g. minimum width and spacing of conductive layers on a chip, dimensions and electrical parameters of protective circuits for electrostatic charge, etc. An examination with the aid of carefully arranged programs operated on large-scale computers, guarantees the immediate identification and elimination of unintentional violations of these design standards.

2.5.3.2 In-Process Control during Production

The manufacturing of integrated circuits comprises several hundred production steps. As each step is to be executed with utmost accuracy, the in-process control is of outstanding importance. Some processes require more than a hundred different test measures. The tests have been arranged such that the individual process steps can be reproduced continuously.

The decreasing failure rates reflect the never ending effort in this direction; in the course of the years they have been reduced considerably despite an immense rise in the IC's complexity.

So in 1985 the typical random failure rates estimated for accelerated life tests with almost 2 million ICs of all complexities are found to be around 80 fit.

2.5.3.3 Reliability Monitoring

The general course of the IC's failure rate versus time is shown by a so-called "bathtub" curve (figure 2). The failure rate has its peak during the first few operating hours (early failure period). After the early failure period has decayed, the "constant" failure rate period starts during which the failures may occur at an approximately uniform rate. This period ends with a repeated rise of the curve during the wear-out failure period. For ICs, however, the latter period usually lies far beyond the service life specified for the individual equipment.

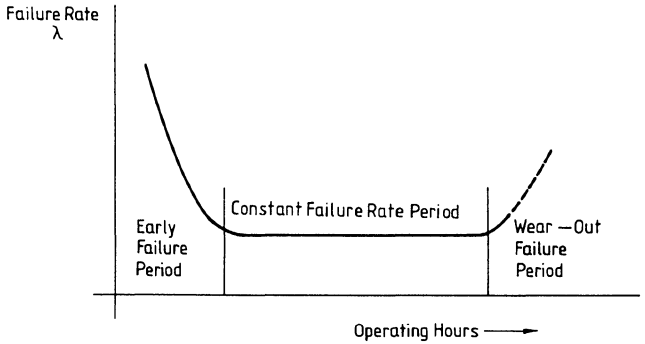


Figure 2

Reliability tests for ICs are usually destructive examinations. They are, therefore, carried out with samples. Most failure mechanisms can be accelerated by means of higher temperatures. Due to the temperature dependence of the failure mechanisms, it is possible to simulate future operational behavior within a short time by applying high temperatures; this is called life test.

The acceleration factor B for the life test can be obtained from the Arrhenius equation

$$B = \exp\left(\frac{E_A}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right)$$

where T_2 is the temperature at which the life test is performed, T_1 is the assumed operating temperature, and k is the Boltzmann constant.

Important for factor B is the activation energy E_A. It lies between 0.3 and 1.3 eV and differs considerably for individual failure mechanisms.

For all Siemens ICs, the reliability data from life tests is converted to an operating temperature of $T_A = 40\,°C$, assuming an average activation energy of 0.4 eV. The acceleration factor for life tests at 125 °C is thus 24, compared with operational behavior. This method considers also failure mechanisms with low activation energy, i.e. which are only slightly accelerated by the temperature effect.

Various reliability tests are periodically performed with IC types that are representative of a certain production line – this is described in the brochure "SQS-IC". Such tests are e.g. humidity test at 85 °C and 85% relative humidity, pressure cooker test, as well as life tests up to 1000 hours and more. Test results are available in the form of summary reports.

2.6 Summary of terms and symbols in alphabetical order

A, B	Indices for limit value
AC	Alternating current
AF	Audio frequency
AM	Amplitude modulation
B	Bandwidth
C	Capacitance
C_i, C_I	Input capacitance
C_{CLK}, $C_{Ø}$	Clock capacitor
CLK	Clock
DC	Direct current
D	Differential
f	Frequency
Δf	Frequency deviation
FM	Frequency modulation
f_i, f_I	Input frequency
f_q, f_Q	Output frequency
G	Gain
G	giga (10^9)
GND	Ground
Hy	Hysteresis
Hz	Cycles per second (Hertz)
i, I	Input
I, *i*	Current
I_S	Current consumption
IF	Intermediate frequency
k	kilo (10^3)
K	Kelvin
L	Inductance
m	Milli (10^{-3})
M	Mega (10^6)
m	Modulation factor
MW	Medium wave
N, n	Noise
o	Offset
OSC	Oscillator
P, P_V	Power dissipation
P_{tot}	Max. perm. power dissipation
pp	Peak-to-peak
q, Q	Output
Q, Q_B	Q-factor
R	Resistance
$R_{th\ JC}$	Thermal resistance (junction-case)
$R_{th\ SC}$	Thermal resistance (system-case)
$R_{th\ SA}$	Thermal resistance (system-air)
RF	Radio frequency

$\frac{S+N}{N}$	Signal-to-noise ratio
T	Cycle time
T	Temperature
TC	Temperature coefficient
t	Time
T_A	Ambient temperature in operation
T_{stg}	Storage temperature
T_j	Junction temperature
t_H	Hold time
t_I	Input pulse duration
t_n	Instant prior to clock pulse
t_{n+1}	Instant after clock pulse
t_P	Average pulse transit time
t_{pd}	Pulse delay time
$t_{P\,HL}$	HL pulse transit time
$t_{P\,LH}$	LH pulse transit time
t_{pI}	Input pulse duration
$t_{p\,Q}$	Output pulse duration
$t_{p\,R}$	Reset pulse duration
$t_{p\,S}$	Set pulse duration
$t_{p\,CLK}$	Clock pulse duration
$t_{p\,Z}$	Count pulse duration
t_s	Set-up time
t_T	Signal transition time
t_t	Dead time
t_Q	Output pulse duration
$t_{T\,HL}$	HL transition time
$t_{T\,LH}$	LH transition time
THD	Total harmonic distortion
V	Volt
V, v	Voltage, general
V_{Hy}	Hysteresis voltage
V_i, V_I	Input voltage
V_q, V_Q	Output voltage
V_R	Reverse voltage
V_S	Supply voltage
W	Watt
Z	Impedance
Z	Zener

Technical Data

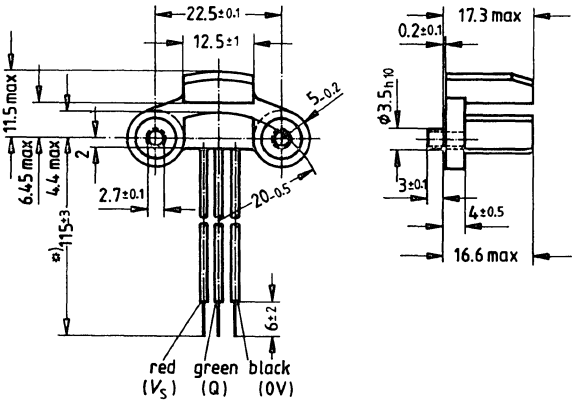
The Hall-effect vane switch HKZ 101 is a contactless switch consisting of a monolithic integrated Hall-effect circuit and a special magnetic circuit hermetically sealed in a plastic package. The switch is actuated by a shoft-iron vane which is passed through the air gap between magnet and Hall sensor.

The main application field is in cars, i.e. as a breakerless trigger in electronic ignition systems. Numerous industrial applications can be found in control engineering, especially in those areas where switches must operate maintenance-free under harsh environmetal conditions (e.g. rpm sensor, limit switch, position sensor, speed measurement, shaft encoder, scanning of coding disks, etc.).

Features

- Contactless switch with open collector output (40 mA)
- Static switching
- High switching frequency
- Hermetically sealed with plastic
- Unaffected by dirt, light, vibration
- Large temperature and voltage range
- Integrated overvoltage protection
- High interference immunity

Special package



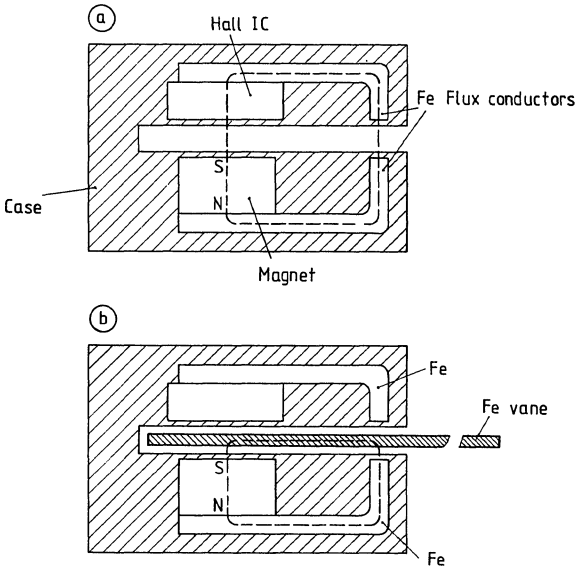
*) Change to 130±3 mm in preparation

Function

The Hall-effect switch is actuated by a soft-iron vane that passes through the air gap between magnet and Hall-effect sensor. The vane short-circuits the magnetic flux before the Hall-effect sensor, as shown in figure 1. The open collector output is conductive (LOW) when the vane is outside the air gap, and blocks (HIGH) when the vane is introduced into the air gap. The output remains HIGH as long as the vane remains in the air gap. This static function does not require a minimum operating frequency. The output signal shape is independent of the operating frequency.

The circuit features integrated overvoltage protection against most of the voltage peaks occurring in automotive and industrial applications. The output stage has a Schmitt trigger characteristic. Most electronic circuits can be driven directly due to the open collector output current of max. 40 mA.

Principle of operation



a) Magnetic flux through the Hall-effect switch with no vane in the gap

b) Magnetic flux short-circuited by the soft-iron vane

Figure 1

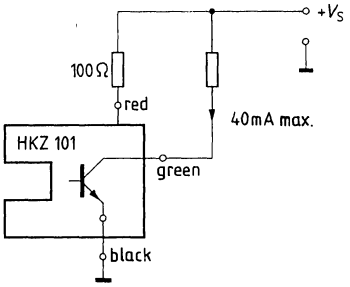
Mechanical characteristics

The Hall-effect vane switch is hermetically sealed in a special plastic, so that it can also be used under harsh environmental conditions. The package is waterproof, vibration-resistant and resistant to gasoline, oil and salt. Two tubular rivets are incorporated in the package to mount the sensor on its carrier plate. The circuit has three flexible leads for power supply and output.

Application notes

The output current of the "open collector" must be limited to the maximum permissible value by a load resistor adapted to the application.

For optimum efficiency of the integrated overvoltage protection, it is suggested that a resistor of approx. 100 Ω be provided in the component's power supply to limit the current.



Maximum ratings

		Test conditions	Lower limit B	Upper limit A	
Supply voltage	V_S		−1.2	24	V
		$T_{amb} = 25\,°C$		30	V
Output voltage in OFF-state	V_Q		−0.8	30	V
Inverse supply current (limited externally)	$-I_S$	$T_{amb} \leq 80\,°C$ $t \leq 1$ h		200	mA
Output current	I_Q	without vane		40	mA
Inverse output current	$-I_Q$			30	mA
Ambient temperature during operation	T_{amb}		−40	135	°C
Storage temperature	T_{stg}		−40	150	°C
Thermal resistance (system-air)	$R_{th\,SA}$			170	K/W

Operating range

Ambient temperature	T_{amb}		−40	130	°C
Supply voltage	V_S		4.5	24	V
Vane[1]: thickness	a		0.5		mm
width	b		8		mm
gap length	c		8		mm
immersion depth	h		4.6	9	mm
gap height	d		17.3−h		mm

1) see figure 3

Characteristics $V_S = 5$ V to 18 V; $T_{amb} = -30$ °C to 130 °C		Test conditions	Lower limit B	Upper limit A	
Output saturation voltage	$V_{Q\,sat}$	without vane $I_Q = 40$ mA			
		$T_{amb} = -30$ to 110 °C		0.4	V
		$T_{amb} = 110$ to 130 °C		0.6	V
Output reverse current	I_{QR}	with vane		10	µA
Supply current	I_S	without vane		12	mA
Delay time	t_{LH}, t_{HL}	$I_Q = 40$ mA		1	µs
Overvoltage protection					
– Supply voltage (V_S)	V_{SZ}	$I_S = 16$ mA	32	42	V
– Output (V_Q)	V_{SO}	$I_S = 16$ mA	32	42	V

Switching point characteristics

Definitions

In most applications, the switching point is set exactly by mechanical adjustment, thus compensating all mechanical tolerances in the system including the scatter of the Hall-effect vane switch. For the function of the device in operation, only the deviations of those characteristics depending on temperature and operating voltage are important.

The characteristic values of the switching points are, therefore, not directly referred to the mechanical dimensions of the vane switch, but to an electrically defined symmetry B_0 according to formula 1):

1) $B_0 = (ON_{left} + OFF_{left} + ON_{right} + OFF_{right}) : 4$
$B_0 = A_0 \pm 0.3$ mm

The definition of the operate and release points is shown in figure 2.

Operate point f_{ON} is obtained by subtracting the measured ON operate value from the reference point B_0:

2) $f_{ON} = ON_{right} - B_0 = B_0 - ON_{left}$

The release point f_{OFF} is calculated from the difference between the appropriate ON and OFF points:

3) $f_{OFF} = ON_{right} - OFF_{right} = OFF_{left} - ON_{left}$

$f_{ON\,0}$ and $f_{OFF\,0}$ are the switching points measured for the individual component under normal conditions ($V_S = 12$ V, $T_{amb} = 25$ °C) within the characteristic device deviation

The deviations of the operate and release points are defined according to 4):

4) $\Delta f_{ON} = f_{ON} - f_{ON\,0}$
$\Delta f_{OFF} = f_{OFF} - f_{OFF\,0}$

Switching point definitions

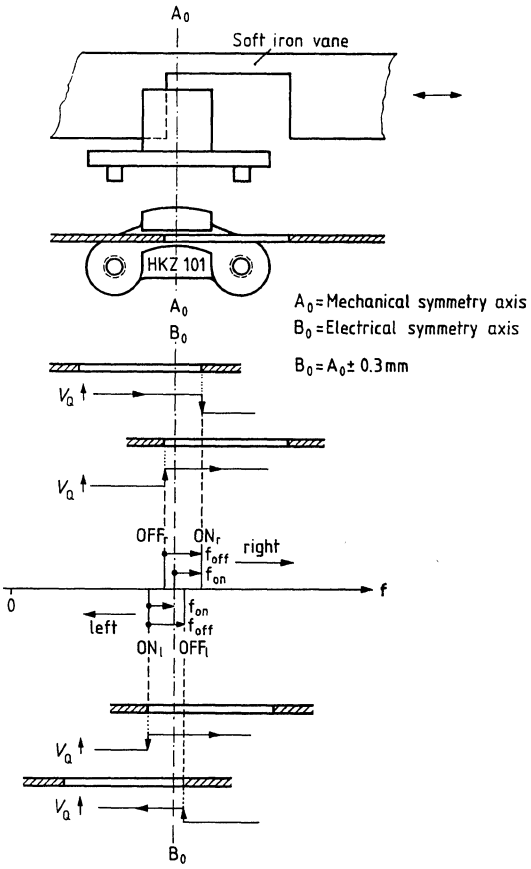


Figure 2

Mechanical measurement conditions

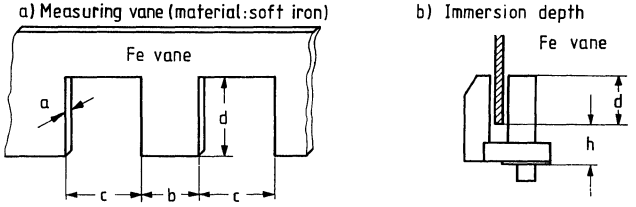


Figure 3

Switching point characteristics

Vane: a = 0.75 mm, b = 8 mm, c = 10 mm
Position: center of air gap
V_S = 5 V to 18 V

		Test conditions	Lower limit B	typ	Upper limit A	
HKZ 101						
Operate point	f_{ON0}	V_S = 12 V, T_{amb} = 25 °C	0.85	1.45	2.05	mm
Deviations	Δf_{ON}	T_{amb} = −30 to 25 °C	−0.4	+0.15	+0.7	mm
		T_{amb} = 25 to 80 °C	−0.2	+0.15	+0.4	mm
		T_{amb} = 80 to 130 °C	−0.4	+0.2	+0.7	mm
Release point	f_{OFF0}	V_S = 12 V, T_{amb} = 25 °C	1.54	2.54	3.54	mm
Deviations	Δf_{OFF}	T_{amb} = −30 to 25 °C	−0.8	+0.3	1.4	mm
		T_{amb} = 25 to 80 °C	−0.4	+0.3	0.8	mm
		T_{amb} = 80 to 130 °C	−0.8	+0.4	1.4	mm

DIP 16

S 041 P is a symmetrical, six-stage amplifier with symmetrical coincidence demodulator for amplifying, limiting, and demodulating frequency-modulated signals. The IC is particularly suited for sets where low current consumption is of importance, or where major supply fluctuations occur.

The pin configuration corresponds to the well-known TBA 120. Pin 5 of S 041 P, however, is not connected internally. These types are especially suited for applications in narrow-band FM systems (455 kHz) and in conventional or standard FM IF systems (10.7 MHz).

Features

- Good limiting properties
- Wide voltage range
- Low current consumption
- Few external components

Maximum ratings

Supply voltage	V_S	15	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)			
S 041 P	$R_{th\,SA}$	90	K/W

Operating range

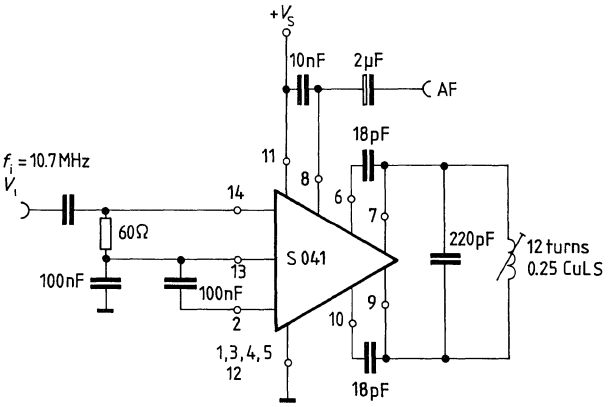
Supply voltage range	V_S	4 to 15	V
Frequency range	f_i	0 to 35	MHz
Ambient temperature range	T_{amb}	−25 to 85	°C

Characteristics (V_S = 12 V, Q approx. 35, f_{mod} = 1 kHz, T_{amb} = 25 °C)

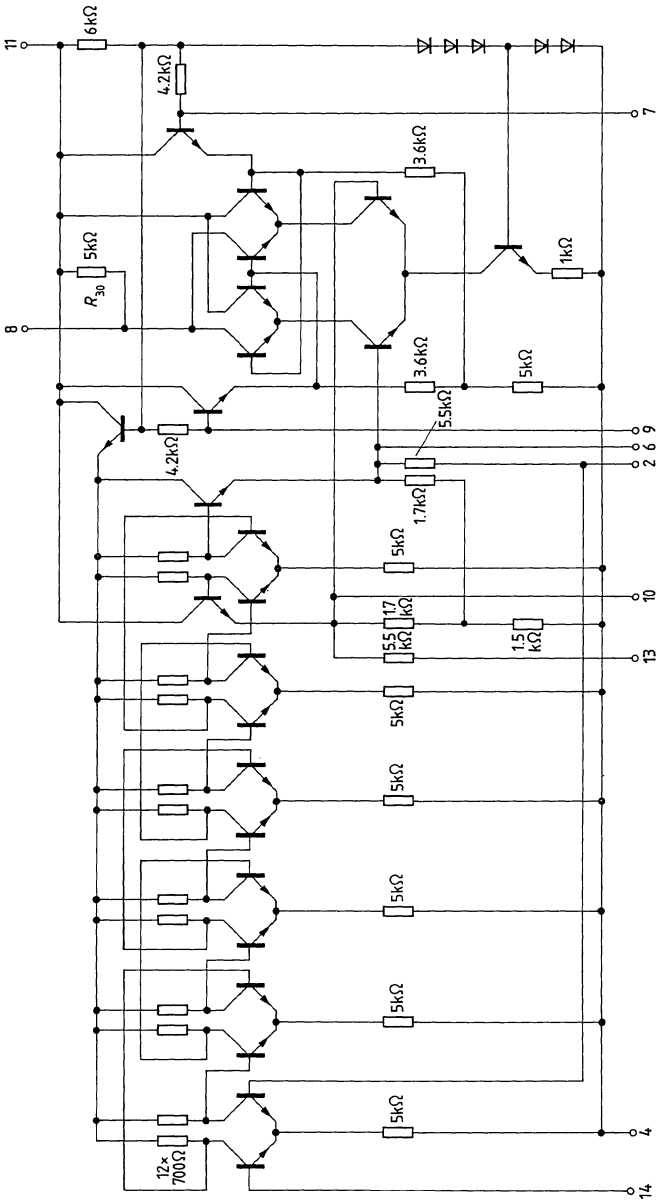
		min	typ	max	
Current consumption	I_S	4.0	5.4	6.8	mA
AF output voltage (f_i = 10.7 MHz, Δf = ± 50 kHz, V_i = 10 mV)	$V_{q\,rms}$	100	170		mV
Total harmonic distortion (f_i = 10.7 MHz, Δf = ± 50 kHz, V_i = 10 mV)	THD		0.55	1.0	%
Deviation of AF output voltage (V_S = 15 V → 4 V, f_i = 10.7 MHz, Δf = ± 50 kHz)	ΔV_q		1.5		dB
Input voltage for limiting (f_i = 10.7 MHz, Δf = ± 50 kHz)	$V_{i\,lim}$		30	60	µV
IF voltage gain (f_i = 10.7 MHz)	G_v		68		dB
IF output voltage for limiting (each output)	$V_{q\,pp}$		130		mV
Input impedance f_i = 10.7 MHz	Z_i		20/2		kΩ/pF
f_i = 455 kHz	Z_i		50/4		kΩ/pF
Output resistance (pin 8)	R_q	3.5	5	8.5	kΩ
Voltage drop at AF ballast resistance	V_{11-8}		1.5		V
AM suppression (V_i = 10 mV, Δf = ± 50 kHz, m = 30%)	a_{AM}		60		dB

All connections mentioned in the index refer to S 041 P (e.g. V_{11})

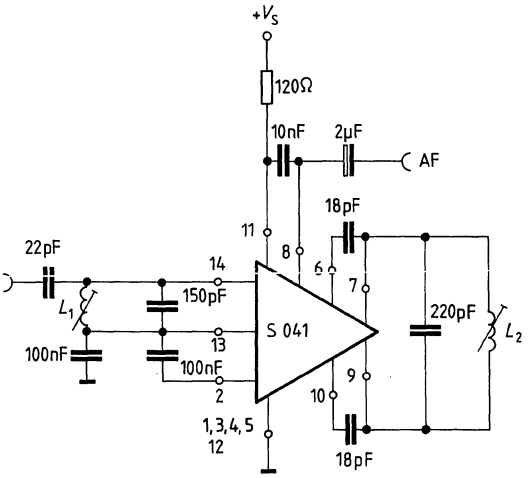
Test circuit



Circuit diagram



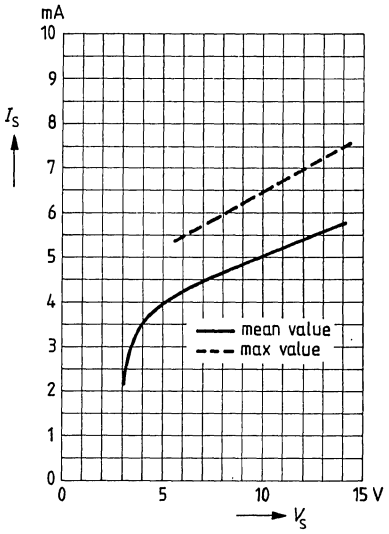
Application circuit for 10.7 MHz (FM IF)
and 455 kHz (narrow-band FM)



Data in parentheses for 455 kHz (narrow-band FM)

Coils	10.7 MHz	455 kHz
L_1	15 turns/0.15 CuLS	71.5 turns/12 x 0,04 CuLS
L_2	12 turns/0.25 CuLS	71.5 turns/12 x 0.04 CuLS
Coil set	D 41-2165	D 41-2393 of Messrs. Vogt

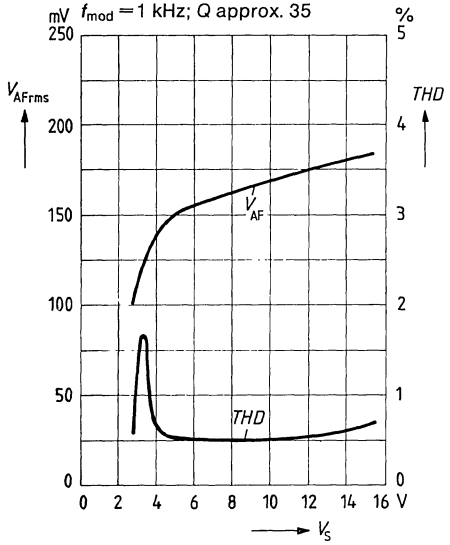
Current consumption versus supply voltage



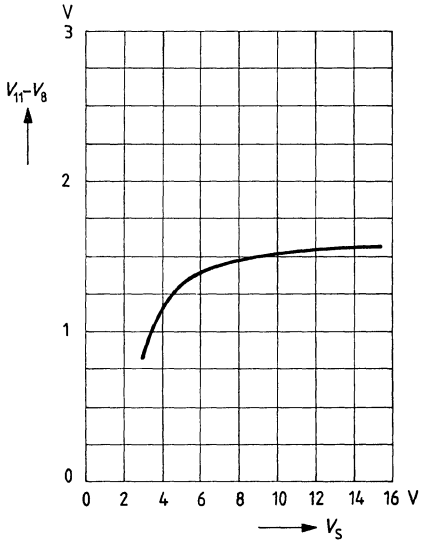
AF output voltage and total harmonic distortion versus supply voltage

$f_i = 10.7$ MHz; $\Delta f = \pm 50$ kHz

$f_{mod} = 1$ kHz; Q approx. 35



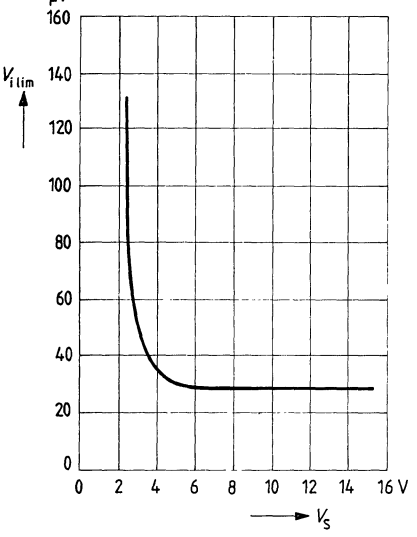
DC output voltage difference versus supply voltage
(without signal)



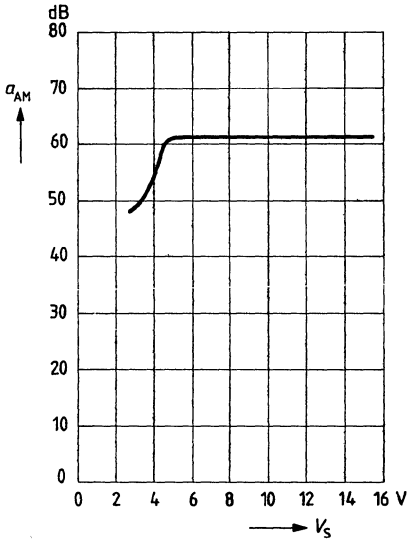
Input voltage for limiting versus supply voltage

$f_i = 10.7$ MHz; $\Delta f = \pm 50$ kHz

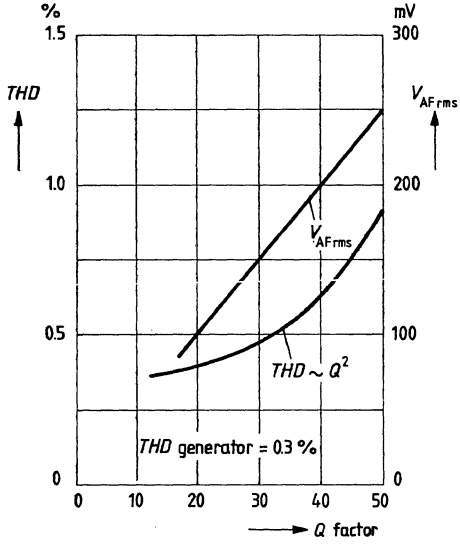
$f_{mod} = 1$ kHz; Q approx. 35



AM suppression versus supply voltage
$f_i = 10.7$ MHz; $\Delta f = \pm 50$ kHz;
$V_i = 10$ mV, $f_{mod} = 1$ kHz, $m = 30\%$



AF output voltage and total harmonic distortion versus Q-factor
$V_S = 12$ V; $f_i = 10.7$ MHz,
$\Delta f = \pm 50$ kHz, $f_{mod} = 1$ kHz



Mixer

S 042 P

DIP 14

Symmetrical mixer for frequencies up to 200 MHz. It can be driven by an external source or by the built-in oscillator. The input signals are suppressed at the outputs. In addition to the usual mixer applications in receivers, converters, and demodulators for AM and FM, the S 042 P can also be used as electronic polarity switches, multipliers, etc.

Features

- Versatile application
- Wide range of supply voltage
- Few external components
- High conversion transconductance
- Low noise figure

Maximum ratings

Supply voltage	V_S	15	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air) S 042 P:	$R_{th\ SA}$	90	K/W

Operating range

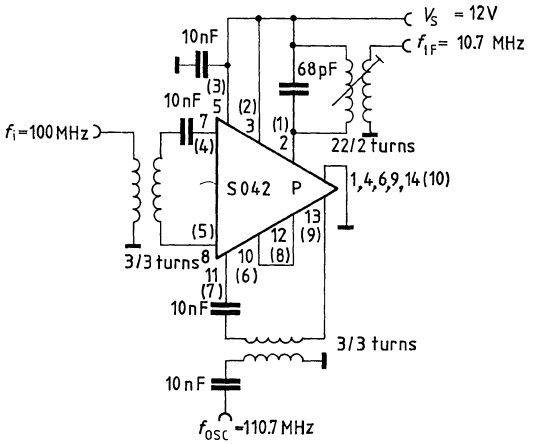
Supply voltage range	V_S	4 to 15	V
Ambient temperature range	T_{amb}	−15 to 70	°C

Characteristics ($V_S = 12$ V, $T_{amb} = 25$ °C)

		min	typ	max	
Current consumption	$I_S = I_2 + I_3 + I_5$	1.4	2.15	2.9	mA
Output current	$I_2 = I_3$	0.36	0.52	0.68	mA
Output current difference	$I_3 - I_2$	−60		60	mA
Supply current	I_5	0.7	1.1	1.6	mA
Power gain ($f_i = 100$ MHz, $f_{OSC} = 110.7$ MHz)	G_p	14	16.5		dB
Breakdown voltage ($I_{2,3} = 10$ mA; $V_{7,8} = 0$ V)	V_2, V_3	25			V
Output capacitance	$C_{2\text{-}M}$, $C_{3\text{-}M}$		6		pF
Conversion transconductance ($f = 455$ kHz)	$S = \frac{I_2}{V_7 - V_8} = \frac{I_3}{V_7 - V_8}$		5		mS
Noise figure	NF		7		dB

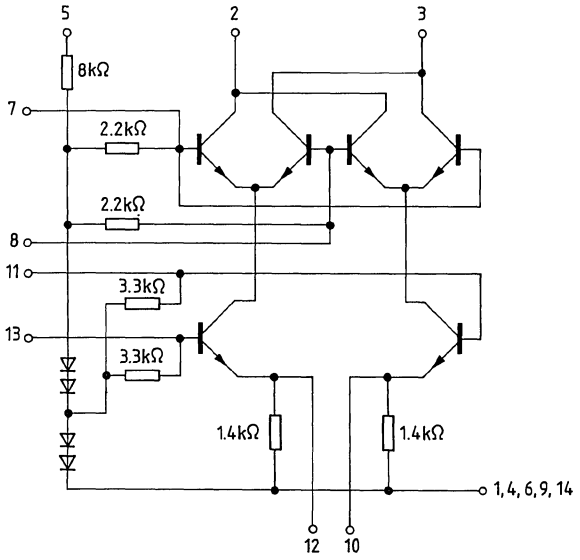
All connections mentioned in the index refer to S 042 P (e.g. I_2)

Test circuit



Connections in parentheses apply to S 042E

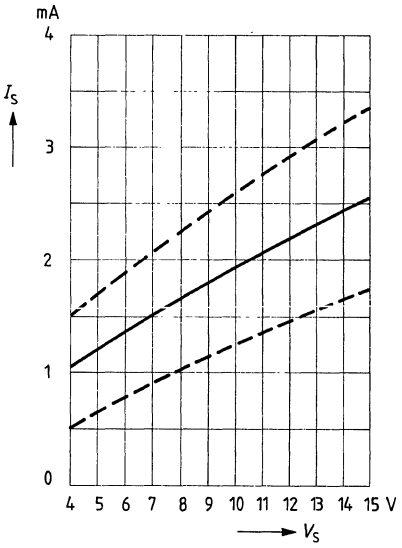
Circuit diagram



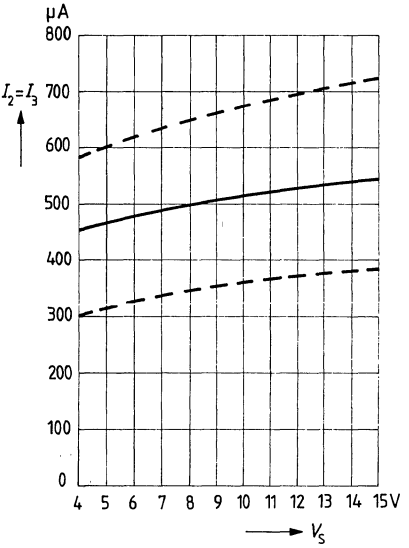
A galvanic connection between pins 7 and 8 and pins 11 and 13 through coupling windings is recommended.

Between pins 10 and 14 (ground) and between pins 12 and 14, one resistance each of at least 220 Ω may be connected to increase the currents and thus the conversion transconductance. Pins 10 and 12 may be connected through any impedance. In case of a direct connection between pins 10 and 12, the resistance from this pin to 14 may be at least 100 Ω. Depending on the layout, a capacitor (10 to 50 pF) may be required between pins 7 and 8 to prevent oscillations in the VHF band.

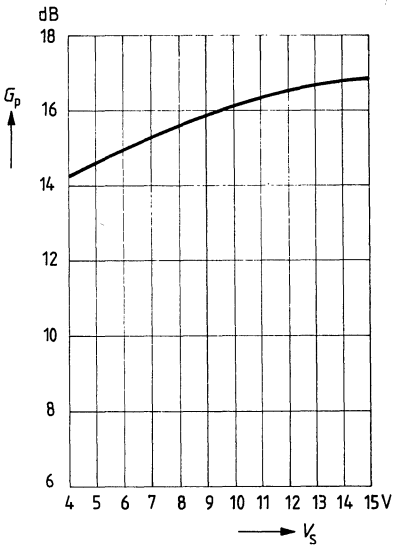
Total current consumption versus supply voltage



Output current versus supply voltage

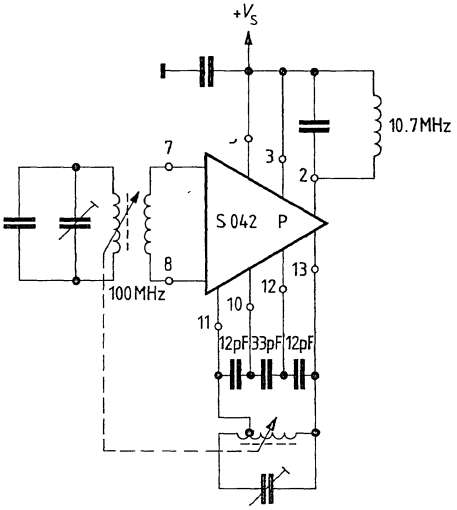


Power gain versus supply voltage

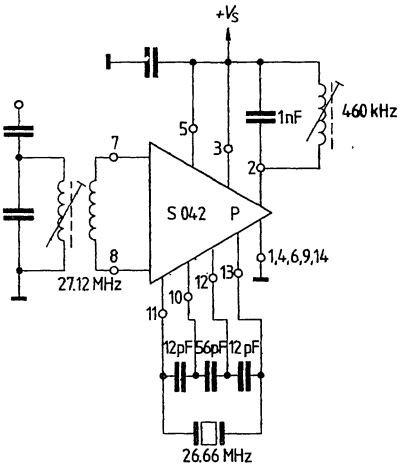


Application circuits

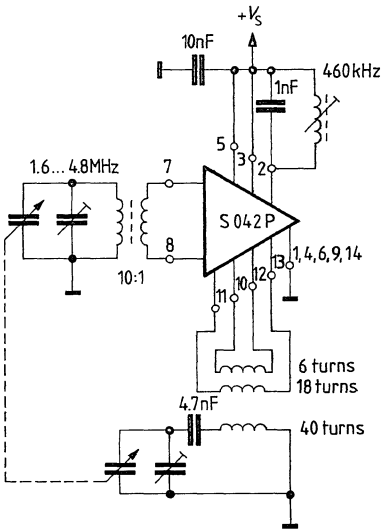
VHF mixer with inductive tuning



Mixer for remote control receivers
without oscillator

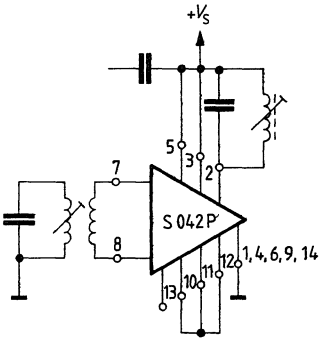


Mixer for short-wave application
in self-oscillating operation



For overtone crystals an adequate inductance is recommended between pins 10 and 12 to avoid oscillations to the fundamental tone.

Differential amplifier with internal neutralization, also suited for use as limiter for frequencies up to 50 MHz or at higher currents up to 100 MHz



DIP 28

The S 178 A is an MOS circuit using p-channel metal-gate-technology with enhancement and depletion transistors, featuring the following technical characteristics:

The **video pulse generator** produces the sync, control, and erase signals required for the control of cameras, mixers, and other equipment.

The following signals are generated:

- Gating signal A
- Sync signal S
- Horizontal pulse H
- Vertical pulse V
- Terminal pulse K_t
- Horizontal gating pulse A (H)
- Double line frequency $H/_2$ } → $H/_2 + V_R$ signal with external signal mixing
  half vertical frequency V_R }
- Vidicon gating signal V_A

Features

All pulses are derived digitally from an input frequency corresponding to a pulse scheme, with a duty cycle of 1 : 1.

Pulse width according to latest CCIR and EIA standards.

The following 6 pulse schemes have been programmed permanently (by 3-bit coding and line number coding):

525 lines (60 Hz) required input frequency 1.008 MHz
625 lines (50 Hz) required input frequency 1.000 MHz
735 lines (60 Hz) required input frequency 1.4112 MHz
875 lines (50 Hz) required input frequency 1.400 MHz
1023 lines (60 Hz) required input frequency 1.96416 MHz
1249 lines (50 Hz) required input frequency 1.9984 MHz

Deviating from the above, any line number between 512 and 1535 lines may be programmed.

It should be noted, however, that a frame frequency of 50 Hz (partial picture duration 20 ms) or 60 Hz (16.66) is achieved.

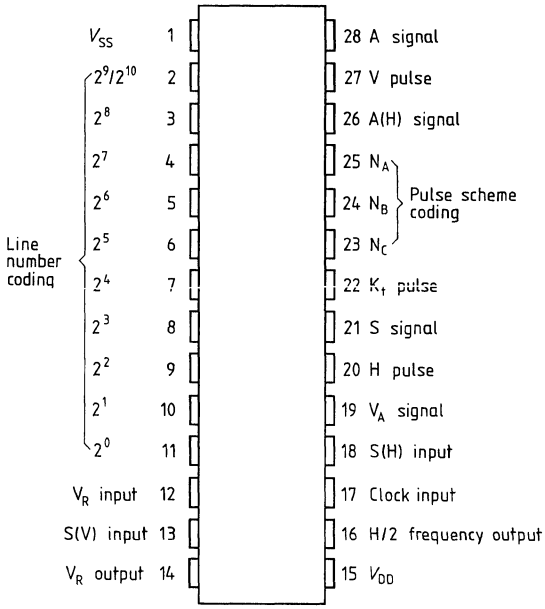
Within the operating frequency it is, however, possible to mix any standard position with any line number.

The following relation applies:

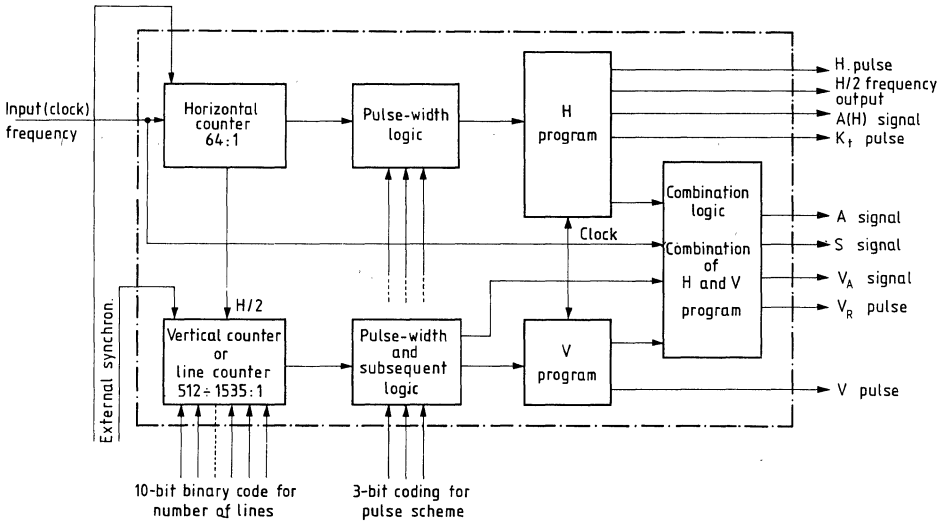
Input frequency f_I = 64: line period H
= 32: line number Z x frame frequency f_{fr}

Not for new design

Pin configuration
top view



Block diagram



Maximum ratings

		Lower limit B	Upper limit A	
Supply voltage } referred	V_{DD}	−12	0.3	V
Voltage at all inputs } to $V_{SS}=0$ V	V_I	−20	0.3	V
Input current	I_I		100	µA
($V_I=0.3$ V; $V_{SS}=0$ V)				
Output current	I_{QH}		−100	µA
	I_{QL}		2	mA
Junction temperature	T_j		125	°C
Storage temperature	T_{stg}	−55	125	°C
Ambient temperature during operation	T_{amb}	−25	75	°C

Characteristics

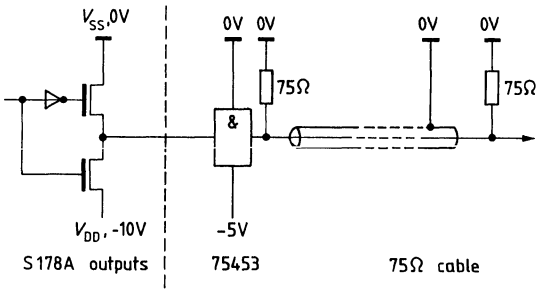
$T_{amb}=25$ °C

		Test conditions	Lower limit B	typ	Upper limit A	
Supply voltage	$-V_{DD}$		9.5	10	10.5	V
Supply current	I_{DD}			60	70	mA
Inputs		direct control with TTL output level				
H input voltage	V_{IH}		$V_{SS}-1.5$		V_{SS}	V
L input voltage	V_{IL}		$-V_{DD}$		$-V_{DD}+5.5$	V
Outputs		when loaded with one TTL input:				
H output voltage	V_{QH}	$I_{QH}=-40$ µA	$V_{SS}-2.6$			V
L output voltage	V_{QL}	$I_{QL}=1.6$ mA	TTL GND−0.7		TTL GND+0.4	V
		when loaded with 2 LPS inputs:				
H output voltage	V_{QH}	$I_{QH}=-40$ µA	$V_{SS}-2.6$			V
L output voltage	V_{QL}	$I_{QL}=0.8$ mA	LPS GND−0.7		LPS GND+0.4	V
		for capacitive load only:				
H output voltage	V_{QH}		$V_{SS}-2.6$			V
L output voltage	V_{QL}		V_{DD}		$V_{DD}+1$	V
Signal transition time of outputs	t_T	when loaded with 2 LPS inputs			100	ns
Input frequency	f_{CLK}		1		2	MHz
Propagation delay time	t_P	clock slope – signal output	0.2		0.4	µs

Interface to 75 Ω cable

A driver stage is required as the pulse generator outputs can be loaded with one TTL input, each. The circuit is to be designed according to the diagram below.

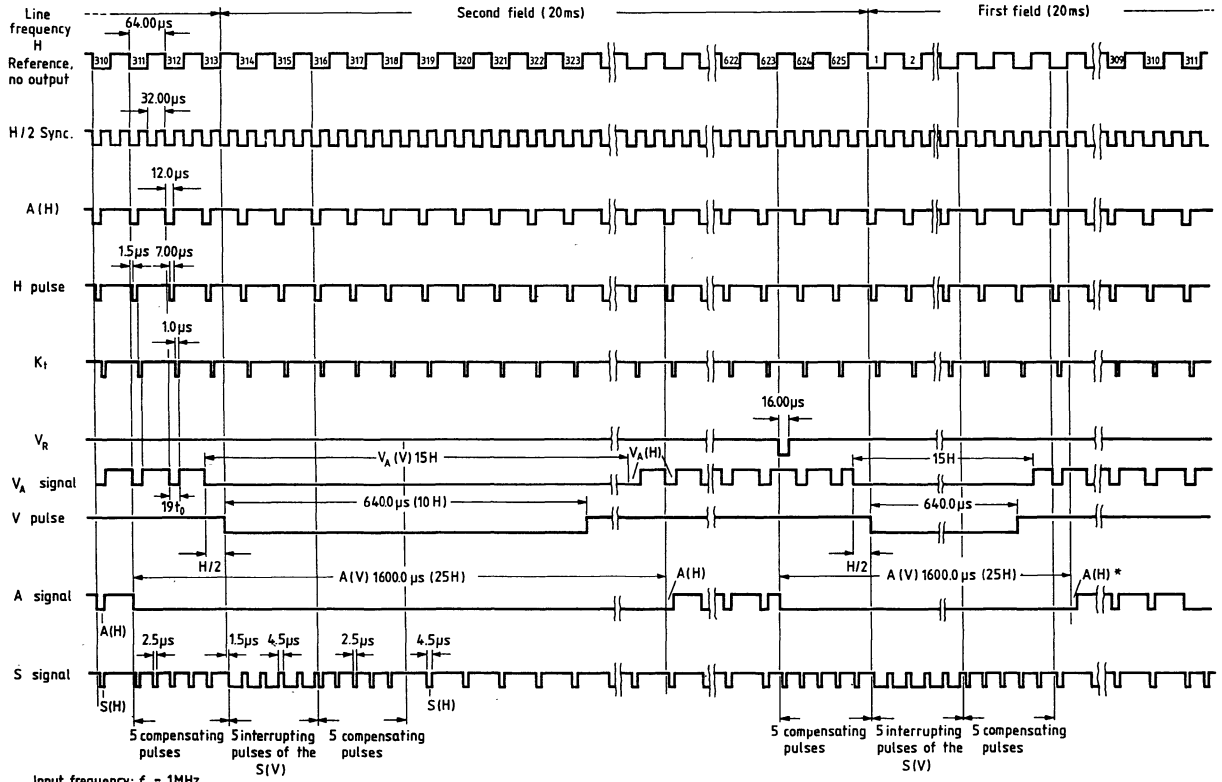
As a driver stage for the 75 Ω coaxial cable, the TTL circuit 75453 (maximum output current 300 mA; pulse delay 11 ns) is recommended.



Programming list for line number coding

Pin number	2	3	4	5	6	7	8	9	10	11	25	24	23
Line number	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	N_A	N_B	N_C
525	H	L	L	L	L	L	H	H	L	H	L	L	L
524	H	L	L	L	L	L	H	L	H	L			
625	H	L	L	H	H	H	L	L	L	H	L	L	H
624	H	L	L	H	H	L	H	H	H	L			
735	H	L	H	H	L	H	H	H	H	H	L	H	L
734	H	L	H	H	L	H	H	H	L	L			
875	H	H	L	H	H	L	H	L	H	H	L	H	H
874	H	H	L	H	H	L	H	L	L	L			
1023	H	H	H	H	H	H	H	H	H	H	H	L	L
1022	H	H	H	H	H	H	H	H	L	L			
1249	L	L	H	H	H	L	L	L	L	H	H	L	H
1248	L	L	H	H	L	H	H	H	H	L			

Pulse scheme for 625 lines



Pulse width table for the programmed line numbers

Pin No.		525 $f = 1.008$ MHz $t_0 = 0.49603\ \mu s$		625 $f = 1.000$ MHz $t_0 = 0.5\ \mu s$		735 $f = 1.4112$ MHz $t_0 = 0.3543\ \mu s$		875 $f = 1.400$ MHz $t_0 = 0.3514\ \mu s$		1023 $f = 1.96416$ MHz $t_0 = 0.25456\ \mu s$		1249 $f = 1.9984$ MHz $t_0 = 0.2502\ \mu s$	
		μs	t_0	μs	t_0	μs	t_0	μs	t_0	μs	t_0	μs	t_0
–	Line period H	63.492	128	64.00	128	45.3514	128	45.7142	128	32.583	128	32.0256	128
16	$H/_2$ synchronization	31.75	64	32.00	64	22.68	64	22.86	64	16.29	64	16.01	64
20	H pulse	6.45	13	7.0	14	4.96	14	4.99	14	2.54	10	2.5	10
26	Horizontal gating A (H)	10.91	22	12.0	24	7.08	20	8.57	24	7.13	28	6.0	24
21	Horizontal synchronization S (H)	4.46	9	4.5	9	2.83	7	2.85	7	2.54	10	2.5	10
20	Front porch	1.48	3	1.5	3	1.06	3	1.07	3	0.76	3	0.75	3
21	Equalizing pulses	2.48	5	2.5	5	1.414	4	1.42	4	1.02	4	1.00	4
21	Interruption of the V-synchronization pulse	4.46	9	4.5	9	2.48	7	2.5	7	1.78	7	1.75	7
22	Terminal pulse K_t	1.49	3	1	2	0.7	2	0.71	2	1.53	6	1.5	6
19	Vidicon gating V_A (H)	9.42	19	9.5	19	6.73	19	6.78	19	4.83	19	4.75	19
19	Vidicon gating V_A (V)	15 H +	$19t_0$	15 H +	$19t_0$	20 H +	$19t_0$	20 H +	$19t_0$	30 H +	$19t_0$	30 H +	$19t_0$
28	Vertical gating A (V)	20 H +	$22t_0$	25 H +	$24t_0$	30 H +	$20t_0$	30 H +	$24t_0$	40 H +	$28t_0$	40 H +	$24t_0$
14	V_R signal	15.87	32	16.0	32	11.34	32	11.43	32	8.15	32	8.01	32
27	V pulse	9.5 H		10 H		14.5 H		15 H		20 H		20 H	
21	Number of pre- and post equalizing pulses	6		5		6		5		6		6	

Duty cycle $f_1 = 50\% \frac{1}{f_1} = 2\ t_0$

Line programming

Any line number between 512 and 1535 lines is binary-programmable. A binary "1" is applied to the pins 2^0 to 2^9 with condition $V_{SS} \geq V_I \geq V_{SS} - 1.5$ V and a binary "0" with $V_{DD} \leq V_I \leq V_{SS} - 4.5$ V. The correct programming of the MSB 2^{10} is carried out automatically via pin 2^9 within the line number range of 512 to 1535.

Uneven line numbers (interlaced scanning method)

The binary form of the desired line number is switched to the corresponding pins.

Even line numbers

The desired line number is reduced by 1 and the binary form is switched to pins 2^0 to 2^9, the LSB (2^0) is switched invertedly.

Functional description

The principal units of the pulse generator are the horizontal and the vertical counter (see block diagram). The horizontal counter, divider ratio 64 :1, divides the input frequency down to twice the line frequency $H/_2$.

An additional logic ensures, that a defined condition of the switching stages is submitted to the counter after a maximum of one picture change. The vertical counter is externally programmable to a defined line number.

Due to the external 3-bit enconding, the desired pulse scheme is programmed internally; i.e. the appropriate switching units for realizing the H and V program, are enabled. The pulses are now fed either directly to the outside, or are logically mixed and masked in the combination logic. The pulse start or the pulse widths, respectively occur at $H/_2$ sync defined according to time. In the case of even line numbers, only the first field appears for all pulse schemes, preceded by a V_R pulse.

In the case of uneven line numbers with first and second fields (interlaced scanning), the V_R pulse precedes only the first field.

According to the CCIR standard, the first field starts, when the leading edge of the V pulse is synchronous with the leading edge of A (H).

External synchronization with $H/_2 + V_R$ or S signal

For video mixing and cross-fading, the BAS signals of the individual cameras or video recorders must be sycnrhonized, i.e. correspond in line and picture. In the case of external synchronization, these two components must be contained in the external signal: either the horizontal and vertical frequency in the case of the S signal: S (H) and S (V), or S (H), and half of the vertical frequency ($H/_2 + V_R$).

At the beginning of the leading edge, short pulses must be derived from these two H and V components, and thereby the defined setting of the horizontal and the vertical counter is accomplished.

(Standard value: H component 300 ns < clock period
V component 1 µs < $H/_2$)

Because of the time deviation of the front edges of the line frequency H and S (H), which is 1.5 periods of the input frequency, the horizontal counter would be set incorrectly. For this reason, an input S (H) has been selected for the horizontal component, which sets the counter to the correct position when activated.

The same is valid for the vertical components of $H/_2 + V_R$ and the S signal. The first frame frequency pulse follows 2.5 or 3 line periods behind the V_R pulse, depending on the scheme. The two inputs provided for the pulses from V_R or S (V), respectively, and the correspondingly encoded line scheme enable a proper setting of the vertical counter. Through the possibility of a defined setting of the counters it is ensured that a proper standard pulse scheme is obtained at the outputs even in the case of external synchronization involving different phase conditions of the synchronization signals.

Note:

At the time of setting the horizontal counter to a defined position, the phase relation of the input frequency is undefined and consequently the tolerance of the synchronization would be one clock period (i.e. ≤ 1 µs for 625 lines). By means of an external phase synchronization circuit with frequency multiplication, the input clock can be derived from the vertical component and, thereby, a defined phase relation of the reset pulse achieved relative to the input clock. Hence a common line deviation (jitter) of < 20 ns absolute value can be achieved.

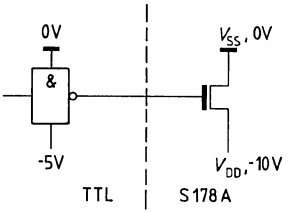
Control

The pulse generator derives the required pulses from the output frequency. As additionally half a clock period is used for the generation of the pulse widths, and as both the leading and trailing edges are used, an input duty cycle of 1 : 1 is required.

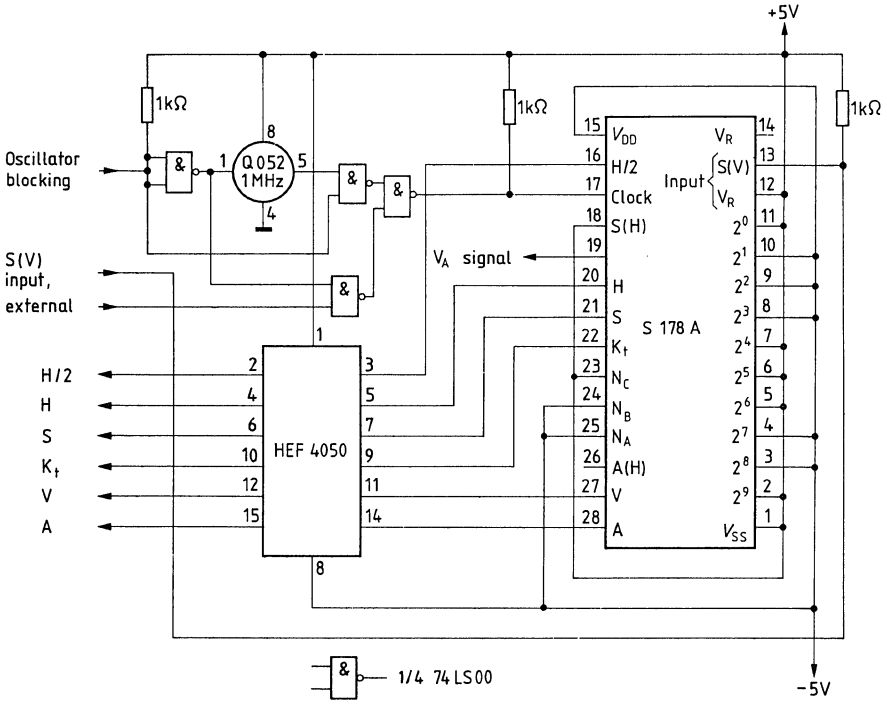
It is, therefore, recommended to operate the quartz oscillator at twice the input frequency and to divide it 2 : 1 by an external stage, thereby obtaining an accurate duty cycle of 1 : 1.

Inputs which are not used must be connected to V_{SS} (H level).

Control with TTL



A TV clock generator, externally synchronizable, using the integrated video pulse generator S 178 A.



Programmable Diode Matrix

S 353
S 1353
S 2353

DIP 28
DIP 14
SO 14

This S 353 contains 160 diodes arranged in a 10 x 16 matrix. The S 1353 contains 32 diodes arranged in a 4x8 matrix, the S 2353 contains 42 diodes arranged in a 7x6 matrix.

For programming, an NiCr fuse is connected in series with the diode.

The matrix is primarily suitable:

1. to replace the extensive wiring in preselection switches. Instead of the multipole wired switch, a single-pole model can be used. Switch and matrix are connected in series.
2. to be used as encoder, decoder, and recorder. The matrix is connected before or behind the appropriate components, or connected between them. The electrical level is only changed by the value of one diode voltage. The electrical connection remains.
3. The component requires MOS handling to avoid undesired programming.
   One of the most important applications is e.g., to enable the programming of frequencies or line numbers, respectively, in conjunction with the PLL component S 187 and the video pulse generator S 178 A.

Maximum ratings of the individual diodes including fuse

		Lower limit B	Upper limit A	
Reverse voltage	V_R	20		V
Voltage between I and 0_S, Q and 0_S[1)]	V_{I0}, V_{Q0}	0	20	V
Forward current	I_F		2	mA
Programming current	I_{prog}		70	mA
Junction temperature	T_j		125	°C
Storage temperature	T_{stg}	−40	125	°C
Ambient temperature range	T_A	−25	70	°C

1) $V_0 \leq V_I$; V_Q; example: if V_I, V_Q are positive 0_S must be grounded.

Electrical characteristics of the individual diodes including fuse
$T_A = 25\,°C$, if not otherwise specified

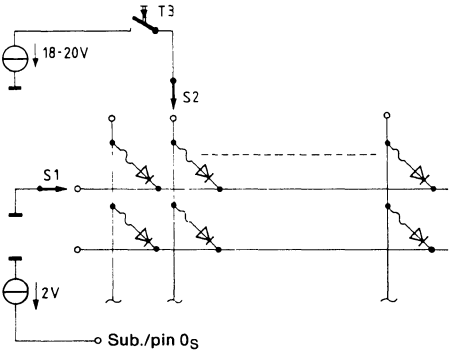
		Test conditions	Lower limit B	typ	Upper limit A	
Reverse voltage	V_R	$I_R = 100\,\mu A$	20			V
Forward voltage	V_F	$I_F = 1\,mA$		1	1.5	V
		$I_F = 50\,\mu A$ $T_A = -25\,°C$			1.0	V
		$I_F = 15\,\mu A$ $T_A = -10\,°C$		0.8	0.85	V
Reverse current I–Q	I_R	$V_R = 10\,V$		10	100	nA
Reverse current I–0_S[1]	I_{R0}	$V_I = 10\,V$			500	nA
Programming current	I_{prog}	$V_Q = 20\,V$ $V_I = 0\,V$ $V_0 = -2\,V$		50	70	mA
Resistance of the suitably programmed fuse	R	$\lvert V_Q - V_I \rvert \leq 5\,V$	20			MΩ
Capacitance I–Q	C	$V_R = 2\,V$		6	9	pF
Recovery time	t_{rr}	$I_F = 200\,\mu A$ $V_{Rmax} = 2\,V$ $R_L = 1\,k\Omega$ Test at $V_R = 0\,V$		13	25	ns

1) Reverse current of a single substrate diode

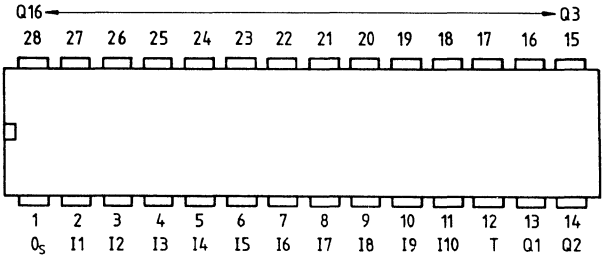
Programming conditions and simple programming circuit

Using the circuit shown, the matrix can be programmed in the following manner:

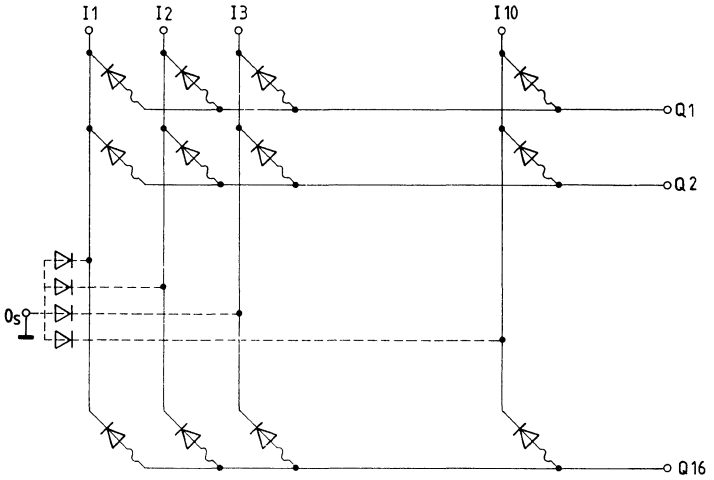
1. observe MOS handling
2. connect pin 0_S (substrate) to ground via a −2 V voltage source
3. connect desired input I to ground using switch S1
4. select desired output Q with switch S2
5. trigger programming process with button T3
6. the specified voltage source with 18 V to 20 V must be suited for a load of at least 300 Ω (fuse resistance), and must have a rise time from 0 V to 20 V of 1 µs
7. only one fuse may be programmed at a time
8. a current pulse duration of 5 ms to 10 ms is sufficient for programming.



Pin configuration
top view

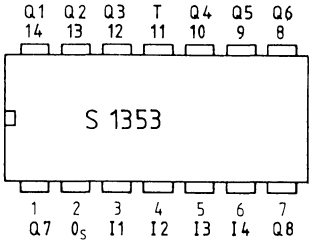


Circuit

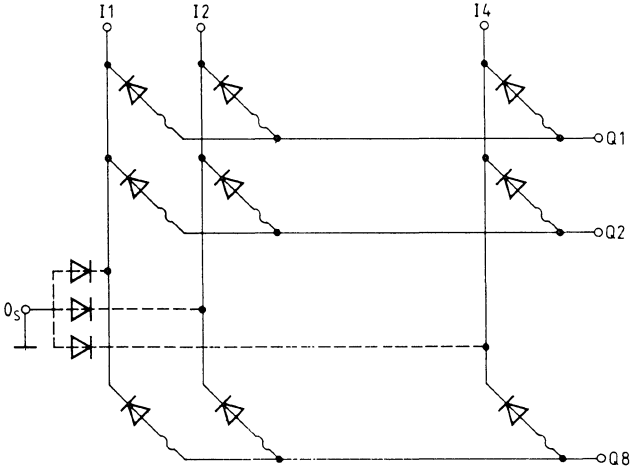


Note: Inputs must not be open $V_I < V_Q$
Test pin T must not be connected.

Pin configuration
(top view)

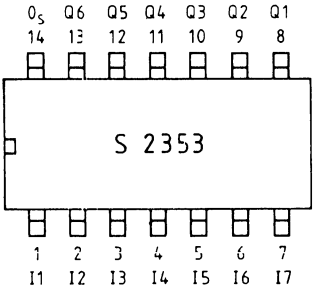


Circuit

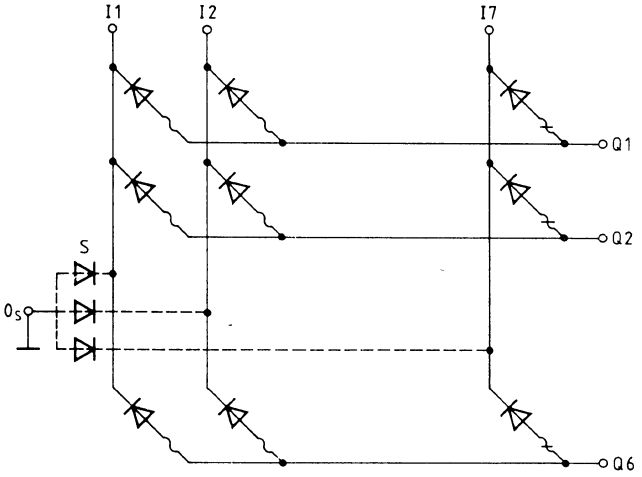


Note: Inputs must not be open
$V_I < V_Q$
Test pin T must not be connected

Pin configuration
(top view)



Circuit



Note: Inputs must not be open
$V_i < V_Q$
S = Substrate diodes

Electronic Dimmer
Electronic Light Switch

S 576 A, B, C
S 576 D

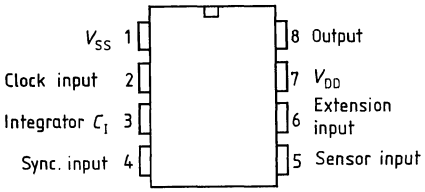
DIP 8

The IC S 576, constructed in PMOS depletion technology, permits the design of a digital electronic dimmer or light switch. Turning on and off as well as the setting of the required brightness are carried out via a single sensor or via an equivalent extension input, respectively.

Features

- Sensor operation – no mechanically moveable switching elements
- Operation is also possible from several extensions by means of sensors or push-buttons
- Can be interchanged with electromechanic wall switches in conventional light installations
- Easy connection to a wireless remote control
- Brightness control with a physiologically approximated linear characteristic
- Very high interference immunity
- The set brightness value remains stored during short line interruptions of < 1 s
- Low power dissipation
- Very few peripheral components
- Clock input provides for automatic dimming (slumber switch)

Pin configuration
top view



■ Not for new design

Maximum ratings
(without external protective circuitry)

		Lower limit B	Upper limit A	
Supply voltage	V_{DD}	−20	0.3	V
Input voltage	V_I	−20	0.3	V
Ambient temperature during operation	T_{amb}	0	80	°C
Junction temperature	T_j		125	°C
Storage temperature	T_{stg}	−55	125	°C
Thermal resistance (system-air)	$R_{th\,SA}$		135	K/W

Characteristics
$T_{amb} = 25$ °C, all voltage ratings are referred to $V_{SS} = 0$ V

		Test conditions	Lower limit B	typ	Upper limit A	
Supply voltage	V_{DD}		−18	−15	−13	V
Supply current	I_{DD}	$V_{DD} = -15$ V		1.0	1.4	mA
Supply current with missing sync signal	I_{DD}	$V_{DD} = -15$ V			0.85	mA
Input reverse current	I_I	$V_I = V_{SS} - 10$ V		< 0.1	3	µA
Input capacitance	C_I	$V_I = 0$V, f=1MHz			5	pF
Sensor input						
H input voltage	V_{IH}	with series resistor 10 MΩ from 220 V line	$V_{SS}-2$			V
L input voltage	V_{IL}				$V_{SS}-8$	V
Input current	I_{IH}				35	µA
HL transition time (trigger transition)	t_{THL}			line sine wave		
LH transition time	t_{TLH}					
Frequency with active signal	f	synchronized with 50/60 Hz clock at sync input		50/60		Hz
Extension input						
H input voltage	V_{IH}		$V_{SS}-2$			V
L input voltage	V_{IL}				$V_{SS}-8$	V
Input current	I_{IH}				35	µA

Characteristics (cont'd)		Test conditions	Lower limit B	typ	Upper limit A	
Sync input (pin 4)						
H input voltage	V_{IH}	with series	1/2 V_{DD}+2			V
L input voltage	V_{IL}	resistor 1.5 MΩ			1/2 V_{DD}−2	V
Input current	I_{IH}	from 220 V line			240	µA
HL transition time (trigger transition)	t_{THL}			line sine wave		
LH transition time	t_{TLH}					
Frequency	f			50/60		Hz
Clock input (pin 2)						
H input voltage	V_{IH}		V_{SS}−2		V_S+0.3	V
L input voltage	V_{IL}		V_{DD}		V_{SS}−8	V
HL transition (trigger transition)	t_{THL}				100	µs
LH transition	t_{TLH}				100	µs
Clock frequency	f_{CLK}		0		500	Hz
Without clock	V_{IO}		V_{SS}		V_{SS}+0.3	V
Integrator (pin 3)						
External components	C_I	compare with fig.1		47		nF
Output						
L output current	I_Q	V_{DD} = −15 V, V_{QL} = −3 V	25			mA
L pulse width	t_{QL}	50 Hz line		40		µs
H output voltage	V_{QH}	compare with text	V_{SS}		V_{SS}+0.5	V
HL transition time	t_{HLQ}				20	µs
LH transition time	t_{LHQ}				20	µs

Operation of the control inputs

Input potential during both half waves of the line phase:

Function	Line half wave	Sensor input	Extension input		
operated	positive	L	H		
	negative	0	H		
not operated	positive	H	L	or	0
	negative	0	0		L

H: V_{IH}
L: V_{IL}
0: any

Functional description

The type series S 576 permits the design of fully electronic dimmers and light switches for light bulbs (resistive loads) which are operated in each case via a single sensor.

In conventional lighting circuit installations it is possible to interchange this component with mechanic wall switches as well as to operate all functions from several switching points (extensions).

The brightness is set by phase control. Its digital logic is sychronized with the line frequency. It is possible to supply the IC via a two-wire-connection as the conduction angle is limited to a maximum of 152° of the half wave.

Operation

1. Dimmers S 576 A, S 576 B, S 576 C (see figure 1)

The integrated circuit can distinguish the instructions "turning ON/OFF" and "dimming" due to the duration of the control input operation.

Turning ON/OFF

Short touch (50 to 400 ms) of the sensor area turns the lamp on or off, depending on its preceding state. The switching process is activated at the end of touching.

Setting of the brightness (dimming)

If the sensor is touched for a longer period (> 400 ms), the conduction angle will be varied continuously. It runs across its control loop in approximately 7 s (e.g. bright-dark-bright) and continues this sequence until the finger is removed from the sensor.

The following process is carried out to enable an easy operation also in the lower brightness range: the phase control angle is controlled such that during the run across the control loops, the lamp brightness varies approximately physiological-linearly with the operating time, and rests for a short period when a minimum brightness is reached.

The conduction angle can be controlled in the half wave range between 35° and 152° by means of the sync input circuitry (R_2, C_4) specified in the application example.

By increasing the *RC* time constant it is possible to shift the control range towards smaller conduction angles (effects the minimum brightness).

Control behavior

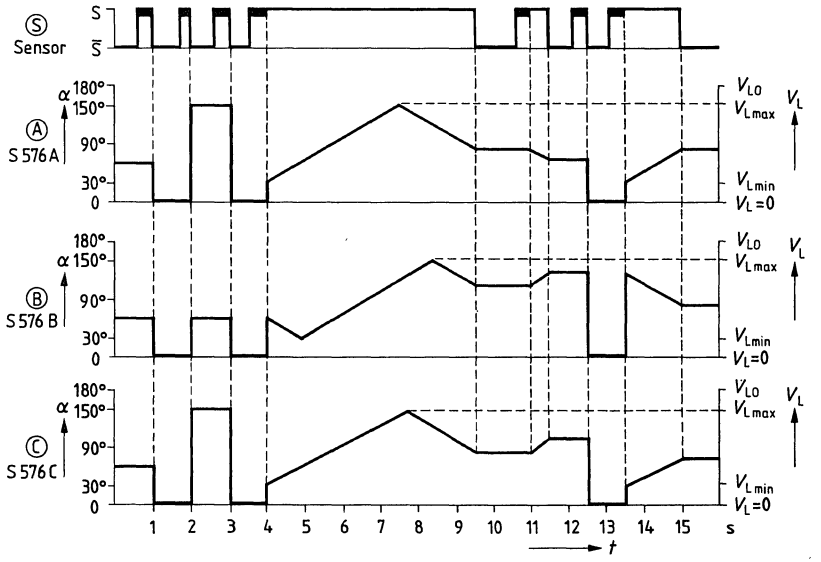
The three versions S 576 A, B, C, differ in their control behavior.

S 576 A With turning on, the maximum brightness is always set; with dimming, control is started from the minimum brightness. With repeated dimming, control is carried out in the same direction (e.g. "brighter").

S 576 B With turning off, the selected brightness is stored and again set when the switch is turned on. Dimming starts at that stored value and the control direction is reversed with repeated dimming.

S 576 C With turning on, the maximum brightness is always set; with dimming, control is started from the minimum brightness. The control direction is reversed with repeated dimming.

Control behavior of the electronic dimmers S 576 A, B, C (schematic)



α Conduction angle
V_L Lamp voltage
S Control signal: S Sensor touched (▬ <0,4s; ▬ >0,4s)
S̄ Sensor not touched
A S 576 A
B S 576 B
C S 576 C

Figure 1

2. Light switch S 576 D (see figure 2)

Upon touching the sensor area (> 50 ms) the lamp is turned on or off alternatively with maximum brightness. The switching process is activated at the start of touching.

Dimming or turning off the light via the clock input is also possible, as in the case with the dimmer.

Control behavior of the electronic light switch S 576 D (schematic)

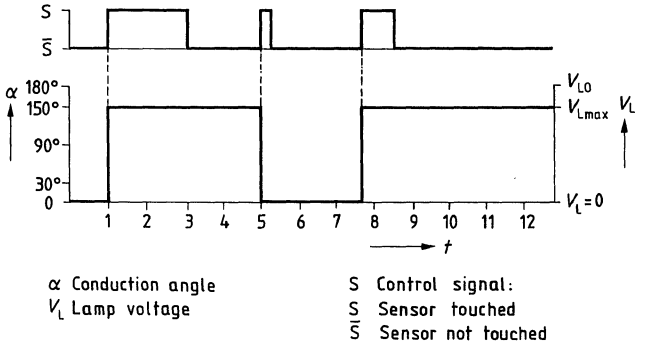


Figure 2

External circuitry (see figure 3)

The suggested circuit design of S 576 performs the following functions:

- current supply for the circuit (R_1, C_2, D 1, D 2, C_3)
- filtered signal for synchronization of the internal time base (PLL circuit) with line frequency (R_2, C_4)
- protection of the user (R_8, R_9)
- sensitivity setting of the sensor (R_7)
- current limitation in the case of incorrect polarization of the extension (R_5, R_6).

  Both resistors can be omitted if no extension is connected. In this case, pin 6 must be interconnected with V_{DD} (pin 7).
- D 3: reduction of positive voltages which may arise during the triggered state at the gate of some triacs, to values below $V_{SS}+0.5$ V (refer to characteristic data). If suitable triacs are used, diode D 3 can be omitted. (This feature of the triac depends on the anode current and on the internal resistance between G and A 1, and can be measured and specified by the manufacturer).

Application circuit S 576

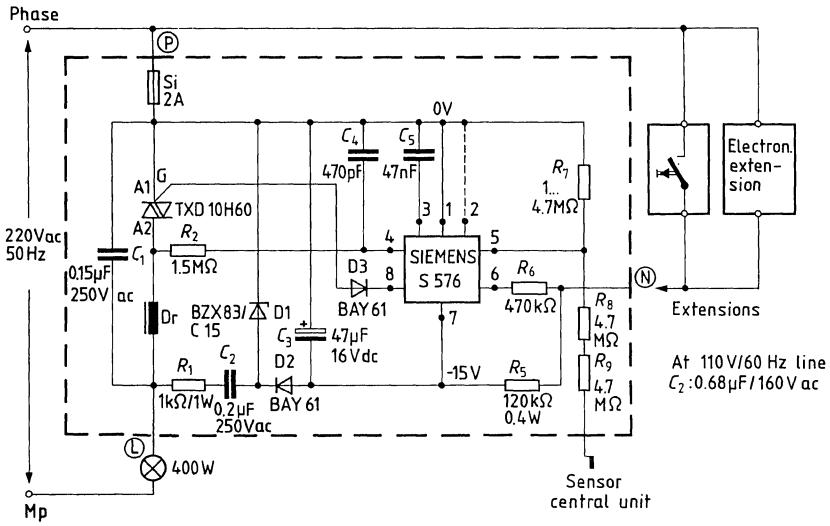


Figure 3

Extensions

All switching and control functions can also be performed from extensions which are connected to an extension input reserved for this purpose. The central unit and the extensions are equivalent. Electronic sensor switches or mechanical pushbutton switches can be connected to the extensions. During operation, H potential must be applied to the extension input for both line half waves.

An electronic circuit suitable for this purpose, is shown in the application example (figure 4). The circuit operates as return delay and takes over the triggering of the switching transistors during the negative line half wave.

- Response time approx. 2 ms
- Return delay time approx. 30 ms
- Protection against incorrect polarization (R_1, D 1, Si)

Application circuit: electronic extension

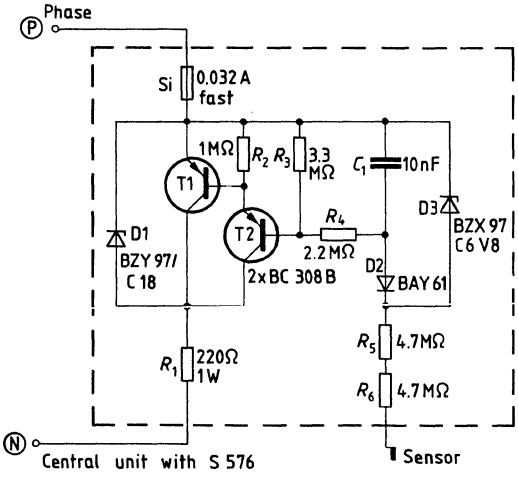


Figure 4

Wireless remote control

The connection of a wireless remote control to the extension is very easy. All functions of the S 576 can be performed with the aid of a single transmission channel.

Slumber switch (clock input)

In the unused state, the clock input is short-circuited to V_{SS}. A slumber switch can be obtained by applying an externally generated clock to this input. Each H L transition decrements the count of the internal brightness memory by one step. When the minimum brightness is reached, the clock turns the circuit to the OFF-state.

The application example (figure 5) shows an oscillator circuit which can also be connected to the power supply of the electronic dimmer or light switch by means of S 576.

The oscillator is enabled by touching the slumber switch sensor. Touching of the dimmer sensor disables the oscillator and, thereby, interrupts the automatic system.

Circuitry

- Oscillator with CMOS gates
- T1 and T2 provide a steep switching transition at the input of gate G3 in order to minimize current consumption (< 100 µA)
- Setting of the clock frequency and thus setting of the dimming time with the *RC* network (R_5, C_2)
- Sensitivity setting of the sensor area (R_1)

Application circuit: S 576 with a slumber switch

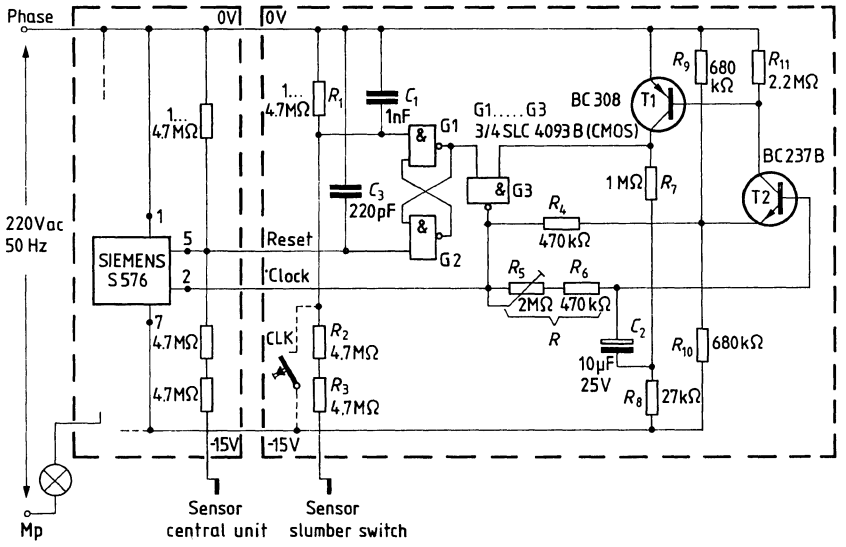


Figure 5

Interference immunity

A digitally determined immunity period of approximately 50 ms ensures a high interference immunity against electrical variations on the control inputs, and allows simultaneously an almost delay-free operation.

Due to the special logic of the extension input, even large ground capacitances of the control line will not lead to interference.

In the case of line interruption, the set switching state with the recommended external circuitry remains stored for about 1 s. After line interruptions for longer periods the circuit turns into the OFF-state.

General information

All stated time specifications refer to a line frequency of 50 Hz. In the case of a line frequency of 60 Hz, the periods are shortened accordingly.

Three-Tone Chime
Single-Tone Chime
Dual-Tone Chime

SAB 0600
SAB 0601
SAB 0602

DIP 8

Three-tone chime SAB 0600

This IC generates the tone sequence of a 3-tone chime. The sound pattern is created by three harmonically tuned frequencies which are switched in succession to a summing point and decay individually in amplitude.

The tone color is adjusted by an external *RC* network (R_1, C_1, and C_2). An 8 Ω loudspeaker can be connected directly via a 100 µF capacitor.

An appropriate design of the loudspeaker housing (shaped as tube or horn) enhances the volume and tone quality and contributes to a pleasant, melodious sound.

Features

- Melodious sound
- Few components required
- Integrated output stage for 8 Ω loudspeaker
- Standby current < 1 µA

Single-tone chime SAB 0601 and dual-tone chime SAB 0602

The two variants SAB 0601 and SAB 0602 were derived from type SAB 0600 by suppressing the last two tones or last tone, respectively, of the three-tone sequence. The SAB 0600 data applies correspondingly.

Maximum ratings

		Lower limit B	Upper limit A	
Supply voltage	V_S	−0.5	11	V
Input voltage at E	V_E	−0.5	V_S	V
Neg. input current at E	$-I_E$		2	mA
Load resistance at Q	R_L	7		Ω
Current consumption at start of tone sequence } refer to	I_{SM}		90	mA
end of tone sequence } measurement circuit	I_{SO}		35	mA
Oscillator frequency at C (due to power dissipation)	f_{OSC}	6		kHz
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	−55	125	°C
Thermal resistance (system-air)	$R_{th\,SA}$		120	K/W

Operating range

Supply voltage	V_S	7	11	V
Ambient temperature	T_{amb}	0	70	°C
Oscillator frequency at C	f_{OSC}	6	100	kHz

Characteristics

$V_S = 7$ V to 10 V; $T_{amb} = 25$ °C

		min	typ	max	
Standby input current	I_0		<1	10	µA
Supply current with open output	I_{SO}		20	35	mA
Max. output power at 8 Ω (tone 3)	P_Q		0.16		W
Max. output voltage at Q (tone 3)	V_{Qpp}		2.8	4.0	V
Deviation of the max. individual amplitudes referred to tone 3	ΔV_{QM}		± 5		%
Frequency variation of basic oscillator with R_1, C_1 = const.	Δf_o		± 5		%
Triggering voltage at E	V_E	1.5		V_S	V
Input current at E ($V_E = 6$ V)	I_E	500	700		µA
Noise voltage immunity at E	$V_{EN\,pp}$		0.3		V
Triggering delay at $f_o = 13.2$ kHz (t_d varies in inverse proportion to f_o)	t_d	2		5	ms
Min. value of external load resistor	R_1		10		kΩ
Max. value of external load resistor	R_1		100		kΩ

Measurement circuit

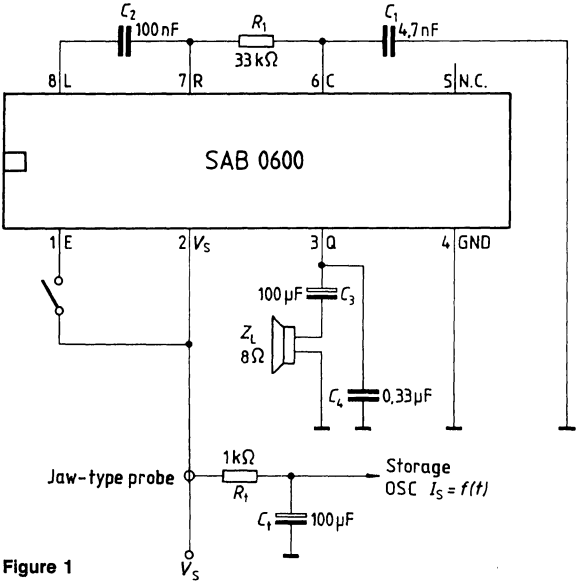


Figure 1

Integral current consumption in the measurement circuit

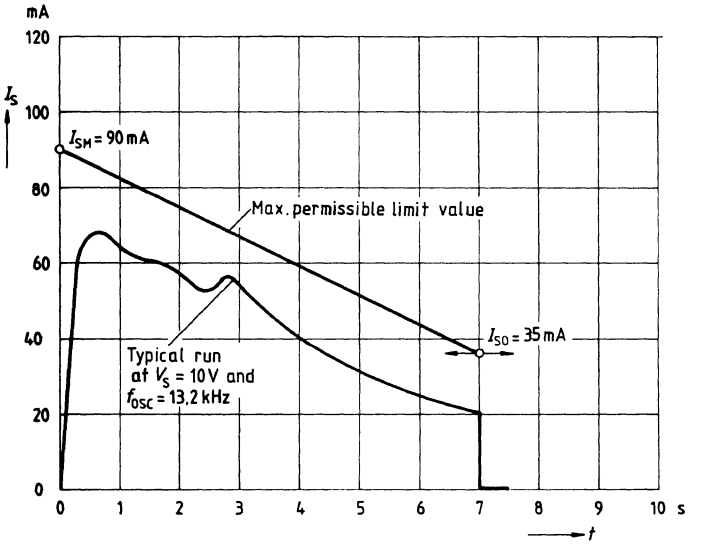


Figure 2

Block diagram

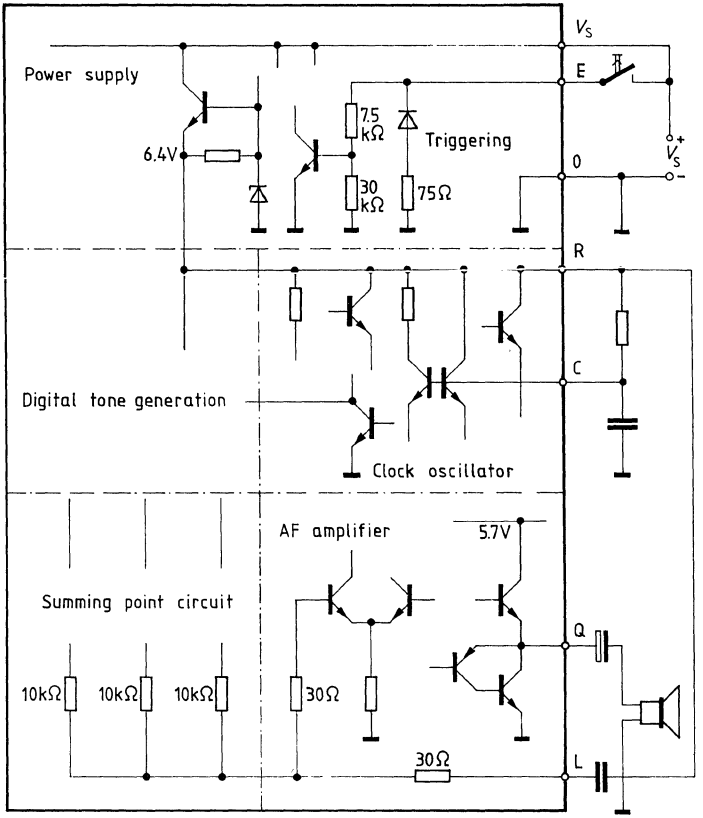


Figure 3

Typical application circuit

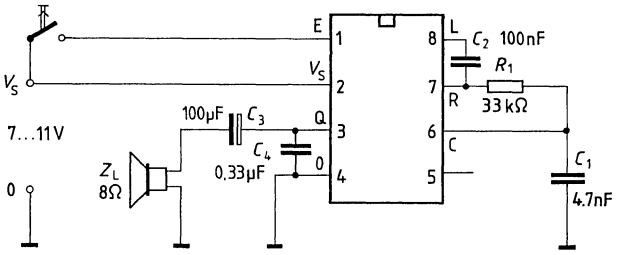


Figure 4

Functional description

The three frequencies – 660 Hz, 550 Hz, and 440 Hz – are obtained by dividing the output of a 13.2 kHz oscillator. One of these three frequencies is divided again to obtain the time base for the tone-decay process. From this time base, 4-bit D/A converters (one for each tone) generate the decay voltage with which the three tones are successively activated and, overlapping each other, are attenuated. The basic frequency is determined by an external *RC* network (pins R and C).

The output stage can drive an 8 Ω loudspeaker with approximately 0.16 W via 100 µF. The output voltage is of square shape. To obtain a melodions output tone as required, the higher harmonics may be reduced by shunting pin L through a suitable capacitor to ground. The output volume can be regulated here by means of a potentiometer.

The circuit only draws current in the active state, and automatically switches off after the tones have decayed. The circuit is activated by a short pulse, between 1.5 V and V_S in amplitude, applied to the triggering connection E (pin 1). If the trigger voltage is still, or again, present when the tones have decayed, the three tones are repeated.

The circuit is not activated when a trigger pulse on E is shorter than 2 ms (interference suppression).

To prevent triggering of the circuit by cross-talk voltages, especially in case of long input lines, the noise voltage peaks should be limited to 0.3 V at the IC input. For this purpose the control line (possibly in front of a series resistor) can be shunted to ground through a suitable capacitor.

Application for ac and dc triggering (figure 5)

The input can alternatively be triggered with direct or alternating current. An internal diode circuit hereby short-circuits the input for negative halfwaves.

The peak voltage of the positive halfwave is added to the battery voltage. A series resistor must be connected into the trigger line to limit the voltage at input E (pin 1) to a maximum value equal to V_S.

The minimum input current at pin E of the SAB 0600 (pin 1) is 500 µA at 6 V. If the voltage drop occurring at 500 µA at the series resistor R_3 (figure 5) amounts to at least the ac peak voltage between A and B ($\hat{V}_{AB}$ ~), the IC will be safe.

The formula $$R_{3\,min} = \frac{\hat{V}_{AB\,max.}}{500\ \mu A}$$

determines the lower limit for R_3.

The upper limit for R_3 is determined by the lowest trigger voltage between A and 0 (pin 4). In the application shown in figure 5, this will be the battery voltage if the device is also to be operated independently of the bell system (triggering by short circuit of A and B).

For reliable triggering, the SAB 0600 requires a current of at least 50 µA with approx. 1.5 V at pin E. Assuming this current, the voltage drop at R_3 must, therefore, not exceed $V_S - 1.5$ V.

The formula $$R_{3\,max} = \frac{V_{S\,min.} - 1.5\ V}{50\ \mu A}$$

results in the upper limit for R_3.

Calculation example for the circuit in figure 5

max. $V_{AB\,rms} = 25$ V max. $\hat{V}_{AB} = 25\ V \times \sqrt{2} = 35.4$ V

$$R_{3\,min} = \frac{35.4\ V}{500\ \mu A} = 70.8\ k\Omega$$

min. $V_S = 6$ V

(The operating range of the SAB 0600 may extend to 6 V for individual components).

$$R_{3\,max} = \frac{6\ V - 1.5}{50\ \mu A} = 90\ k\Omega$$

In this example, a value of 82 kΩ ± 10% would be suitable for R_3.

Circuit for SAB 0600 application in home chime installations utilizing ac and dc triggering; adjustable sound and volume

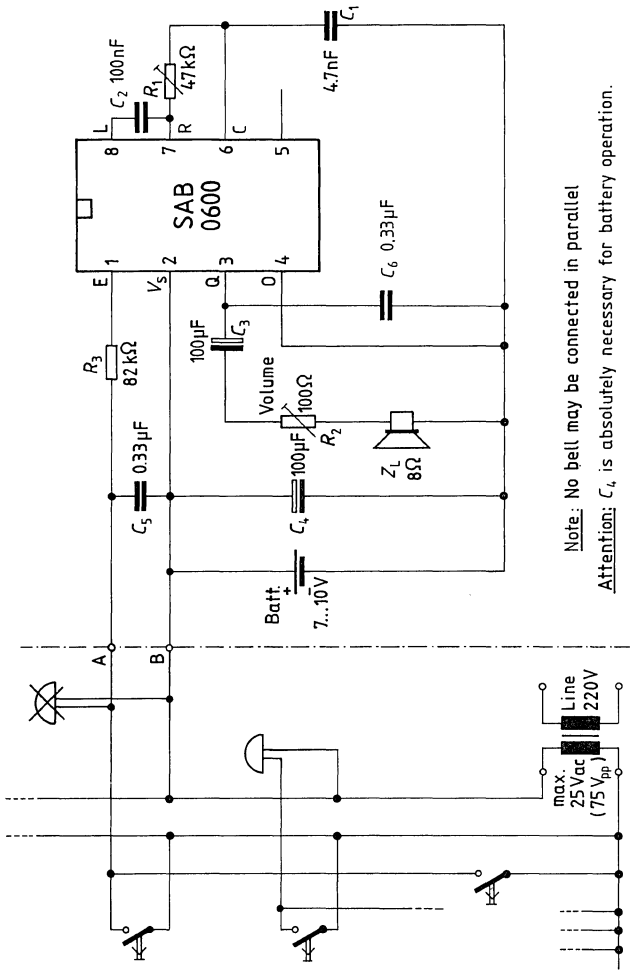


Figure 5

PCB layout information: Because of the high peak currents at V_S, Q, and 0 (ground) and to avoid RF oscillations, the lines should be designed in a flatspread way or as star pattern. Star points are the terminals of capacitor C_4.

Further details regarding the circuit in figure 5

Because an ohmic contact between A and B causes triggering of the chime, no bell may be connected in parallel to the chime. However, paralleling several chimes does not cause any problems.

In older batteries, the higher internal resistance of the battery may cause voltage drops becoming apparent as distortions. C_4 serves as a buffer element expanding the service life of the battery.

The trigger line connected to pin A acts – in open state – as antenna for noise pulses which could trigger the chime unintentionally. Capacitor C_5 will largely suppress such interference.

If there is the risk of incorrect polarity connection when changing the battery, the battery line should be protected by a diode.

For the selection of components, the following recommendations are given:

Capacitors:

C_1: 4.7 nF/≥ 10 V, ± 5%; e.g. MKT
C_2: 100 nF/≥ 10 V, ± 20%; e.g. MKT
C_3: 100 µF/≥6.3 V, ± 100/—10%; e.g. aluminum electrolytic
C_4: 100 µF/≥ 10 V, + 100/—10%; e.g. aluminum electrolytic
C_5, C_6: 330 nF/≥ 50 V, + 100/—20%; e.g. ceramic

Resistors:

R_3: 82 kΩ/0.1 W, ± 10%, carbon film resistor
R_1: When a fixed resistor is used, 0.1 W ± 5% metal film resistor.

DIP 8

The audible signal device SAE 0700 generates two tone frequencies in a ratio of approx. 1.4 : 1 that follow one another in a periodic sequence. The tone frequency can be varied throughout a range between 100 Hz and 15 kHz by an external resistor. The switching frequency of 0.5 to 50 Hz is set by an external capacitor. The SAE 0700 can be used to drive either a loudspeaker or a piezo-ceramic transducer. The SAE 0700 can be supplied with voltage in two ways:

1. rms ac voltage from 10 V
2. dc voltage from 9 to 25 V

The SAE 0700 issues the tone sequence for as long as the supply voltage is applied. After application of the supply voltage, the tone sequence commences with the higher of the two tones.

Features

- Direct ac-voltage feeding possible through integrated bridge rectifier
- Integrated overvoltage protection through Z diode, approx. 28 V
- Bridge rectifier provides for protection against incorrect polarity in dc operation
- Few external components (one resistor and one capacitor minimum)

Block diagram (with external components for dc supply)

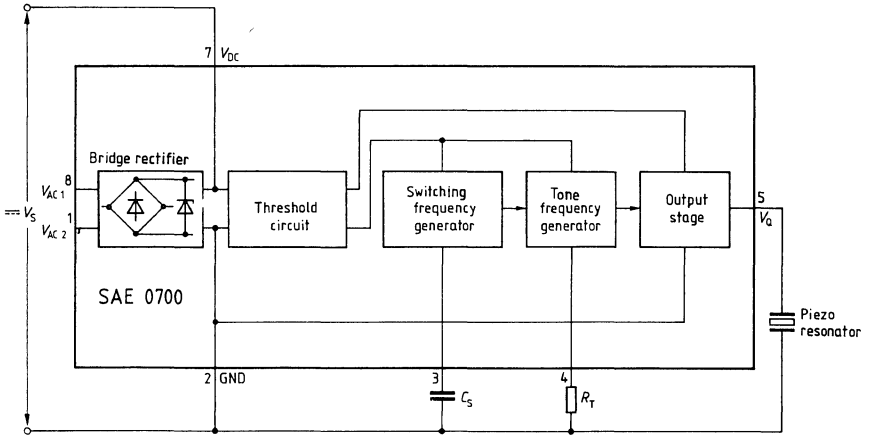


Figure 1

Functional description

The audible signal device SAE 0700 (see blcok diagram, **fig. 1**) includes the following functional blocks:

- bridge (for voltage supply) and overvoltage protection
- threshold circuit
- switching-frequency generator
- tone-frequency generator
- output stage

Bridge rectifier: The bridge rectifier enables direct feeding with ac voltage or dc voltage (independent of polarity). DC-voltage supply without integrated bridge is also possible via pins V_{DC} and GND.

If the voltage is supplied via the bridge, the input voltage $V_{8\,i}$ should be dimensioned such that at least 9 V appear at the pin V_{DC} (also with output loading). It should also be noted that in the case of voltage supply via the bridge, the maximum output current has to be limited to 50 mA.

Response of the SAE 0700 as a result of spikes on the AC line is prevented by a built-in initial resistance R_{INI}. In a voltageless condition R_{INI} provides for discharging the storage capacitor of V_{DC} to ground.

The Z diode following the bridge serves as overvoltage protection. The bridge circuitry shown in **figure 2** efficiently protects the SAE 0700 against damage as a result of the following voltage values:

- overvoltages in acc. with VDE 0433 (2 kV – 10/700 µs)
- ac voltages up to 220 V/50 Hz for a duration of 30 s

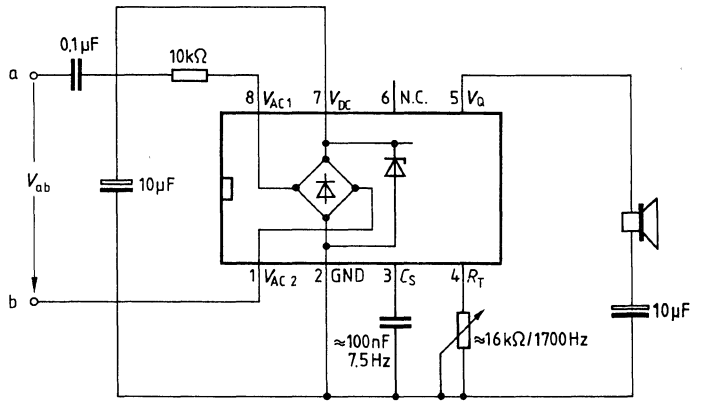


Figure 2

Threshold circuit: With a threshold voltage of typically 8.6 V this ensures that the SAE 0700 is not activated by noise pulses.

Switching-frequency generator: This switches periodically between the two frequencies produced by the tone-frequency generator. Wiring with a capacitor C_S produces a switching frequency f_S according to the following formula:

$$f_S\ [\text{Hz}] = \frac{750}{C\ [\text{nF}]} \pm 25\% \quad \text{(valid from 0.5 to 50 Hz)}$$

Tone-frequency generator: This generates a squarewave voltage with the two tone frequencies f_{T1} and f_{T2}. The basic frequency f_{T1} and the second tone frequency f_{T2} are calculated according to the following formulae:

$$f_{T1}\ [\text{Hz}] = \frac{2.72 \times 10^4}{R\ [\text{k}\Omega]} \pm 25\% \quad \text{(valid from 0.1 to 15 kHz)}$$

$$f_{T2}\ [\text{Hz}] = f_{T1} \times (0.725 \pm 5\%)$$

The tone-frequency generator is temperature-compensated for better stability.

Output stage: This boosts the generated tone voltage for direct driving of a piezo-ceramic transducer or a loudspeaker, possibly across a dropping resistor.

Pin configuration

Pin No.	Symbol	Function
1	V_{AC2}	AC-voltage input
2	GND	Ground
3	C_S	Connection for capacitor C_S
4	R_T	Connection for resistor R_T
5	Q	Output
6	N.C.	Not connected
7	V_{DC}	DC-voltage input
8	V_{AC1}	AC-voltage input

Maximum ratings

		Lower limit	Upper limit	
Voltage at pin 7	V_{DC}	−0.5	26	V
Voltage at pin 3	V_{32}	−0.5	5.5	V
Voltage at pin 4	V_{42}	−0.5	7	V
Output voltage at pin 5	V_Q	−0.5	V_{DC}+0.5	V
AC voltage at pin 8 and 1 (peak value)	V_{AC}		28	V
Input current of bridge	I_{81}	−50	50	mA
AC input current of bridge	$I_{81\,rms}$		25	mA
Output current (50 µs, duty cycle 1 : 10)	I_Q	−100	100	mA
Output current	$I_{Q\,rms}$		50	mA
Total power dissipation (T_{amb} = 25 °C)	P_{tot}		0.8	W
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	−40	125	°C
Thermal resistance (system-air)	$R_{th\,SA}$		120	K/W

Operating range

Supply voltage	V_{DC}	9	25	V
Tone frequency	f_{T1}	0.1	15	kHz
Ambient temperature	T_{amb}	−25	85	°C

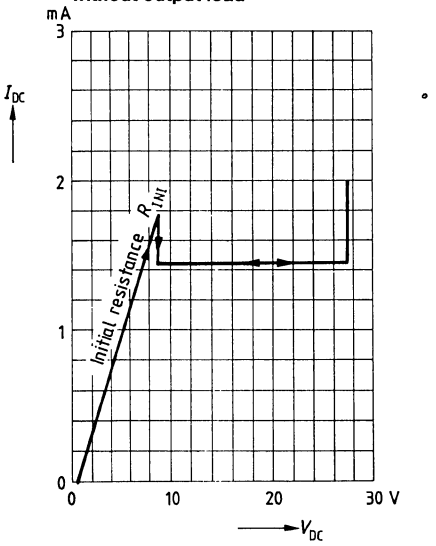
Characteristics

T_{amb} = −25 °C to 85 °C

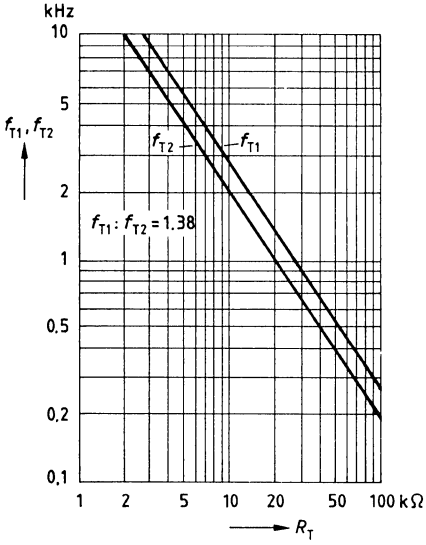
		Test conditions	Lower limit B	typ	Upper limit A	
Current consumption	I_{DC}	V_{DC} = 9 V to 25 V, w/o load		1.5	1.8	mA
Switching threshold	$V_{DC\,ON/OFF}$		8	8.6	9	V
Initial resistance	R_{INI}	see characteristic, figure 3	3.5	4.7	6	kΩ
Output-voltage swing	V_Q	I_Q = ± 10 mA	V_{DC}−3.7	V_{DC}−3		V
Tone frequency	f_{T1}	V_{DC} = 15 V, V_{32} = 0 V, R_T = 16 kΩ	1.275	1.700	2.125	kHz
Switching frequency	f_S	V_{DC} = 15 V, C_S = 100 nF	5.6	7.5	9.4	Hz
Tone frequency ratio	f_{T1}/f_{T2}		1.31	1.38	1.45	
Temperature coefficient of tone frequencies	TC_f			8×10^{-4}		K^{-1}

Characteristic curves

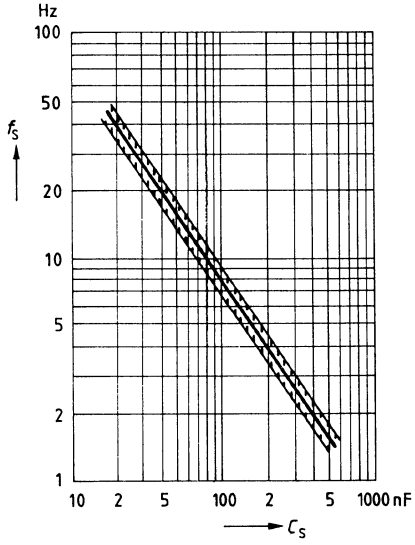
Current consumption versus supply voltage V_{DC} without output load



Tone frequencies f_{T1} and f_{T2} versus resistance R_T



Switching frequency f_S versus capacitance C_S



8 Bit CMOS Analog-to-Digital Converters with 8-Channel Multiplexers

SDA 0808 A
SDA 0808 B

Preliminary Data **DIP 28**

The SDA 0808 A;B is a monolithic CMOS device with a single supply of 5 V DC, 8 bit analog to digital converter, 8-channel analog multiplexer and microprocessor compatible control logic and 8 bit data bus. It is a pin to pin compatible device to the data acquisition component ADC 0808/0809.

The SDA 0808 A;B has the method of successive approximation with a capacitor network as the conversion technique. The converter features a temperature stabilized differential comparator, 8-channel multiplexer for 8 analog inputs and a sample & hold circuit. The device needs no external offset or gain adjustments. Easy interfacing to microprocessors is provided by 3 bit addresslatch, 8 bit data-outputlatch and 8 bit TRI STATE databus.

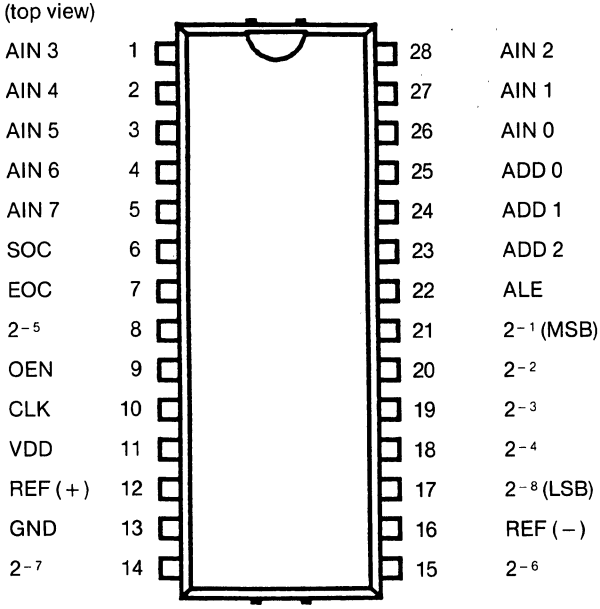
Features

- Resolution 8 bits
- Total unadjusted error ± 1/2 LSB
- No missing codes
- Conversion time 15μs
- Single supply 5 V DC
- 8-channel multiplexer with latched control logic
- Easy interface to all microprocessors, or operates stand alone
- 0 V to 5 V analog input voltage range
- No offset or gain adjust required
- Latched TRI STATE output
- Oututs meet TTL voltage level specifications
- CMOS low power consumption
- 28 pin P-DIP standard package

Pin Designation

Pin No.	Function	Symbol
1 to 5	Analog inputs	AIN 3 to AIN 7
6	Start of conversion	SOC
7	End of conversion	EOC
8	Digital output signal	2^{-5}
9	Output enable	OEN
10	External clock input	CLK
11	Pos. supply voltage	VDD
12	Pos. reference voltage	REF (+)
13	Ground	GND
14 to 15	Neg. reference voltage	REF (−)
17 to 21	Digital output signals	2^{-8} to 2^{-1}
22	Address latch enable	ALE
23 to 25	Address inputs	ADD 2 to ADD 0
26 to 28	Analog inputs	AIN 0 to AIN 2

Pin Configuration
(top view)



Functional Description

The Converter

The converter is partitioned into 3 major sections: An approx. 50 pF capacitor network as a sample & hold circut, the successive approximation register and the comparator. The capacitor network includes a correction, so that the first output transition occurs when the analog signal has reached + 1/2 LSB.

The A/D converter's successive approximation register (SAR) is reset on the positive edge of the start of the conversion (SOC) pulse. The conversion is begun after the falling edge of the start of conversion pulse with the next rising edge of the external clock signal. A conversion in progress will be interrupted by a new start of conversion pulse.

The logical end of conversion output (EOC) will go low after the rising edge of the start of conversion pulse. It is set to logical one with the first rising edge of the external clk after the internal latch pulse. The autozeroed, high resolution, low drift comparator makes the A/D converter extremely insensitive to temperature errors.

A/D Converter Timing

After a conversion has been started, the analog voltage at the selected input channel is sampled for 10 external clock cycles which will then be held at the sampled level for the rest of the conversion time. The external analog source must be strong enough to source the current in order to load the sample & hold capacitance, being approximately 50 pF, within those 10 clock cycles.

Conversion of the sampled analog voltage takes place between the 11th and 18th clock cycle after sampling has been completed. In the 19th clock cycle the converted result is moved to the output data latch. With the leading edge of the 20th clock cycle the end of conversion signal is set.

Multiplexer
The device provides eight multiplexed analog input channels. A particular input channel is selected by using the address decoder.

Table I shows the input states for the address lines to select any channel. The address is latched on the low to high transition of the ALE signal.

Table I:

Address lines			Selected Analog Channel
AD 2	AD 1	AD 0	AIN
L	L	L	AIN 0
L	L	H	AIN 1
L	H	L	AIN 2
L	H	H	AIN 3
H	L	L	AIN 4
H	L	H	AIN 5
H	H	L	AIN 6
H	H	H	AIN 7

Absolute maximum ratings

		Lower limit B	Upper limit A	
Supply voltage (see Note 1)	V_{CC}		6.5	V
Input voltage range	V_I	− 0.3	V_{CC} + 0.3	V
Continuous total power dissipation (at or below 25 °C free-air temperature range)			875	mW
Operating free-air temperature range				
SDA 0808A	T_A	− 40	85	°C
SDA 0808B	T_A	− 40	125	°C
Storage temperature range		− 65	150	°C

Note 1: All voltage values are with respect to network ground terminal

Recommended operating conditions
V_{CC} = 5V; T_A = 25 °C

	test cond.	min	typ	max	unit
Supply voltage	V_{CC}	4.5	5	6	V
Positive reference voltage	V_{REF+} (see Note 3)		V_{CC}	V_{CC} + 0.1	V
Negative reference voltage	V_{REF-}		0	− 0.1	V
Differential reference voltage	$^{\Delta}V_{REF} = V_{REF+} - V_{REF-}$		5		V
Start pulse duration	t_{wiSi}	200			ns
Address load control pulse width	$t_{w(ALC)}$	200			ns
Address setup time	t_{su}	50			ns
Address hold time	t_h	50			ns
Clock frequency	f_{clock}	10	640	1500	kHz

Note 3: Care must be taken that this rating is observed even during power up

Electrical characteristics over recommended operating free-air temperature range
V_{CC} = 4.75V to 5.25V (unless otherwise noted)

Total device

High-level input voltage, control inputs	V_{IH}	V_{CC} = 5V	V_{CC} − 1.5			V
Low-level input voltage, control inputs	V_{IL}	V_{CC} = 5V		1.5		V
High-level output voltage	V_{OH}	I_O = − 360μA	V_{CC} − 0.4			V
Low-level output voltage						
Data outputs	V_{OL}	I_O = 1.6mA		0.45		V
End of conversion	V_{OL}	I_O = 1.2mA		0.45		V
Off-state (High impedance-state) output current	I_{OZ}	V_O = 5V		3		μA
	I_{OZ}	V_O = 0		− 3		μA
Control input current at maximum input voltage	I_I	V_I = 5V		1		μA
Low-level control input current	I_{IL}	V_I = 0		− 1		μA
Supply Current	I_{CC}	f_{clock} = 640 kHz		0.3	3	mA
Input capacitance, control inputs	C_I	T_A = 25 °C		10	15	pF
Output capacitance, data outputs	C_O	T_A = 25 °C		10	15	pF
Resistance from pin 12 to pin 16			1	1000		kΩ

Analog multiplexer
$V_{CC} = 5V$; $T_A = 25°C$

		test cond.	min	typ	max	unit
Channel on-state current	I_{on}	$V_I = 5V$,				
(see Note 4)		$f_{clock} = 640kHz$			2	μA
		$V_I = 0V$,				
		$f_{clock} = 640kHz$			−2	μA
Channel off-state-current	I_{off}	$V_{CC} = 5V$,				
		$T_A = 25°C$, $V_I = 5V$		10	200	nA
		$V_{CC} = 5V$,				
		$T_A = 25°C$, $V_I = 0$		−200	nA	
		$V_{CC} = 5V$, $V_I = 5V$			1	μA
		$V_{CC} = 5V$, $V_I = 0$			−1	μA

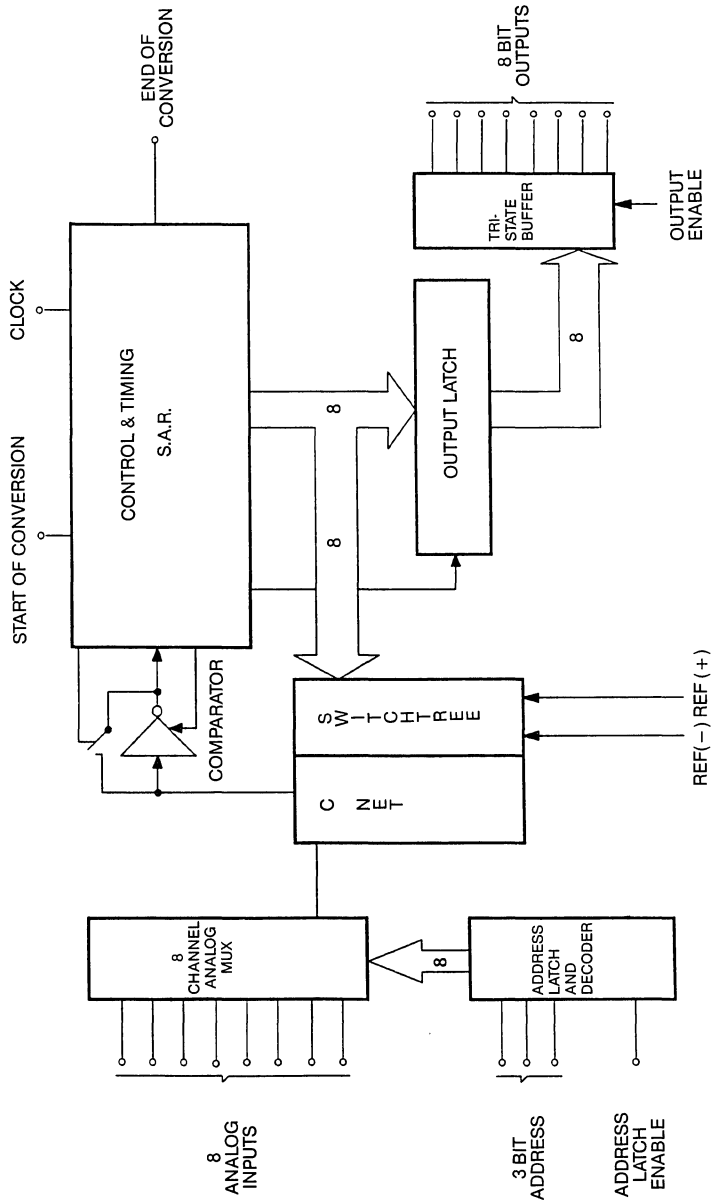
Note 4: Channel on state current is primarily due to the bias current into or out of the threshold detector, and it varies with clock frequency.

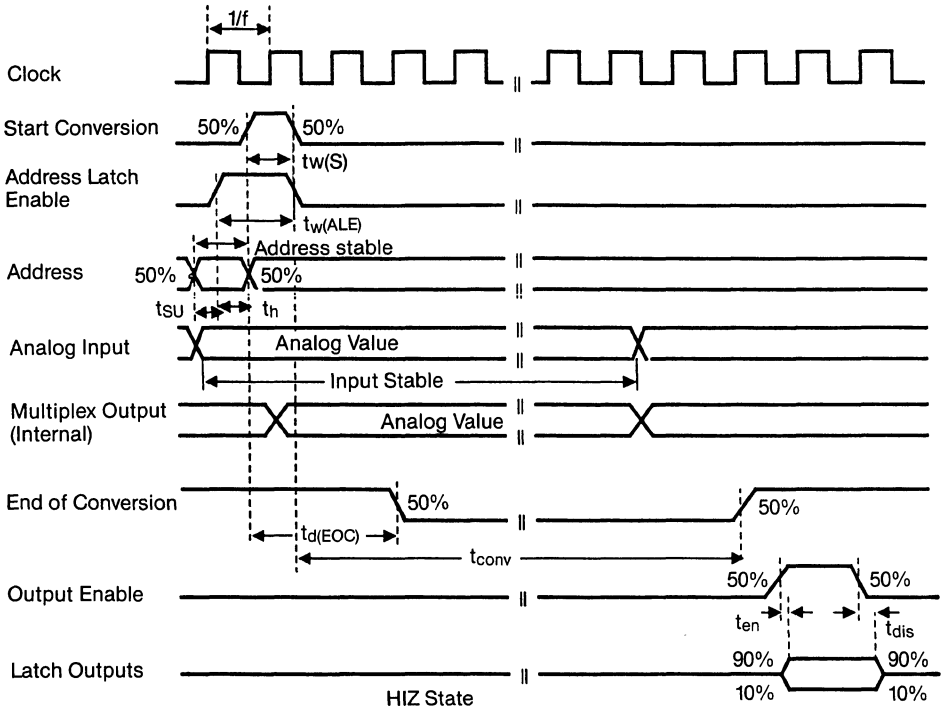
Operating characteristics
$T_A = 25°C$, $V_{CC} = V_{REF+} = 5V$, $V_{REF-} = 0V$, $f_{clock} = 640$ kHz (unless otherwise noted)

		test cond.	SDA 0808A min.	SDA 0808A typ.	SDA 0808A max.	SDA 0808B min.	SDA 0808B typ.	SDA 0808B max.	unit
Supply voltage sensitivity	k_{SVS}	$V_{CC} = V_{REF+} = 4.75V$ to 5.25V, $T_A = -40°C$ to 85°C, (see note 5)		±0.05			±0.05		%/V
Linearity error (see note 6)				±0.25			±0.25		LSB
Zero error (see note 7)				±0.25			±0.25		LSB
Total unadjusted error		$T_A = 25°C$		±0.25	±0.5		±0.25	±0.5	LSB
(see note 8)		$T_A = -40°C$ to $+85°C$		±0.5					LSB
		$T_A = -40°C$ to $+125°C$						±0.5	LSB
Output enable time	t_{en}	$C_L = 50pF$, $R_L = 10k\Omega$		80	250		80	250	ns
Output disable time	t_{dis}	$C_L = 10pF$, $R_L = 10k\Omega$		105	250		105	250	ns
Conversion time	t_{conv}	$f_{clock} = 1.5MHz$, (see note 10)		15	16		15	16	μs
Delay time, end of conversion output	$t_{d(EOC)}$	(see notes 9 and 10)	0		14.5	0		14.5	μs

Notes:
5 Supply voltage sensitivity relates to the ability of an analog to digital converter to maintain accuracy as the supply voltage varies. The supply and V_{REF+} are varied together and the change in accuracy is measured with respect to full-scale.
6 Linearity error is the maximum deviation from a straight line through the end points of the A/D transfer characteristic.
7 Zero error is the difference betweent he output of an ideal converter and the actual A/D converter for zero input voltage.
8 Total unadjusted error is the maximum sum of linearity error, zero error, and full scale error.
9 For clock frequencies other than 640 kHz, $t_{d(EOC)}$ maximum is 8 clock periods plus 2 μs.
10 Refer to the operating sequence diagram.

Functional Block Diagram




1/f
Clock
Start Conversion
50%
50%
tw(S)
Address Latch Enable
tw(ALE)
Address stable
Address
50%
50%
tSU
th
Analog Input
Analog Value
Input Stable
Multiplex Output (Internal)
Analog Value
End of Conversion
50%
50%
td(EOC)
tconv
Output Enable
50%
50%
ten
tdis
Latch Outputs
90%
90%
10%
10%
HIZ State

DIP 18

The SDA 2008 IC represents a follow-on development of the infrared transmitter IC SAB 3210. It includes a disconnectable 8-stage divider, thus enabling the oscillator to operate up to 500 kHz with a ceramic oscillator instead of an *LC* circuit.

Features

- Complete security of the keyboard against operating errors
- Instruction extension up to 60 instructions is possible by using diodes and by means of a shift key (keyboard changeover)
- Start bit programmable by external voltage
- Wide supply voltage range between 5 V and 16 V
- Low current consumption, typically 3 mA. The battery can be switched off by an external transistor
- No external column resistors necessary

Maximum ratings

all voltages referred to $V_{DD} = 0$ V

Supply voltage	V_{SS}	18	V
Input voltage	V_i	18	V
Power dissipation per output	P_q	100	mW
Total power dissipation	P_{tot}	500	mW
Storage temperature range	T_{stg}	−40 to 125	°C

Operating range

referred to $V_{DD} = 0$ V

Supply voltage	V_{SS1}	5 to 16	V
Supply voltage[1)]	V_{SS1}	5.5 to 16	V
Ambient temperature	T_A	0 to 70	°C

1) Instruction extension with diodes

Characteristics

all voltages referred to V_{DD}

		min	typ	max	
Supply current (outputs not connected)	I_6		3	7	mA
Leakage current, total current of outputs Ca, Cb, Cc, Cd, ETA, IRA (refer to test circuit)	$I_{2,3,4,5,7,8}$			1	µA
Inputs					
Oscillator input CLK I					
Operating frequency with prescaler	f_{17}	160		560	kHz
Operating frequency for external clock with disconnected prescaler	f_{17}	20		70	kHz
IRA remote control signal output					
H output voltage (refer to test circuit) $I = 4$ mA; $V_{SS} = 6$ V	V_{qH8}	V_{SS}–5			V
H resistor with respect to V_{SS}	R_{qH8}	100			Ω
ETA switch-on transistor output					
H output current $V_{q7} = V_{SS}$–4 V	I_{qH7}	100		10000	µA

Row input 1 to 8 (internal pull-high resistors)

Instructions can be transmitted by connecting the respective row input with the corresponding column output (refer to instruction set). Operating errors, such as connecting more than one respective row and column are recognized and transmission is interrupted. Only exception: instruction extension with row 8 (see input, keyboard).

The connection can include as max. resistance a silicon diode junction in forward direction and a 100 Ω resistance in series. Minimum resistance is zero.

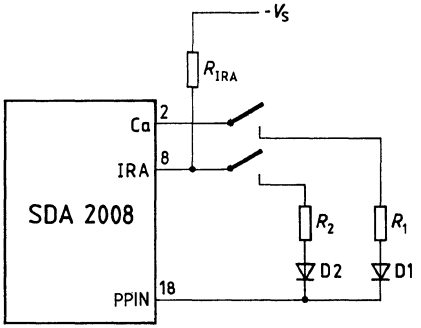
ETA input

The ETA input is connected to the supply voltage via the base-emitter diode of the NPN switching transistor for normal transmitting operations.

PPIN program input

If the PPIN input is joined with the corresponding column output or with the IRA output (in this case = 33 kΩ ≤ R_{IRA} ≤ 47 kΩ) the output mode can be changed in accordance with the table "PPIN connections".

Example



33 kΩ ≤ R_{IRA} ≤ 47 kΩ
R_1R_2 ≤ 100 Ω
D1, D2 = V_f ≤ 0-8 V at I_F = 0.1 mA and $T_{A\,min}$

Description of function

The SDA 2008 IC operates as a transmitter for the infrared remote control system IR 60.

The PMOS circuit contains a control output for an NPN transistor which deactivates the supply voltage if the keyboard is not activated (i.e. no row is in "low" state).

Input, keyboard

The transmitter contains an input matrix of 8 rows and 4 columns. In order to input an instruction, a row must be connected to a column. Thus, the transmitter is switched on and the appropriate instruction is sent. Without further measures it is possible to issue up to 32 instructions. The instruction set can be extended up to 60 either with the aid of additional diodes (for this purpose 2 diodes are required for each 4 additional instructions) or up to 62 instructions with a shift key. In both cases the additional connection (diodes to row 8 or shift key) is necessary prior to issuing the first instruction — after that the originally allocated instruction is sent independent of the additional connection.

As a fifth matrix column, $-V_S$ can be used to input the instructions 40 to 47 (without external diode connection using only one key, each).

Operating error

The circuit includes a security lock against multi-operations (several keys are depressed simultaneously). An exception is the double operation inside a column with one of the rows 1 to 7 and row 8, since this combination is used in order to extend the instruction set with the aid of diodes. After transmission of the first infrared instruction after the startbit, this double operation is locked as well.

Start instruction, end instruction

After the switch-on, the instruction No. 62 is issued as start instruction thus indicating to the receiver the start of the instruction transmission.

In case of an operating error, this instruction is generated by the security lock. If the key or keys are released, the selected instruction is sent once more (depending upon the exact instant of release) while the instruction No. 62 is sent once as stop before the supply voltage is switched off. Safety measures prevent to change an instruction to any other than instruction No. 62.

Output

The transmitter encodes the input in bi-phase code (refer to timing diagram). Prior to the 6 information bits, a presignal and a startbit which can be selected via PPIN, are sent. The presignal enables proper control of the preamplifier on the receiver side, whereas the startbit is used for receiver discrimination. Thus it is possible to control a TV set and a radio in one room independently of each other with the same remote control system.

The output signal is carried at 1/16 of the clock frequency ($f_{CLKI}/16$) and a pulse duty factor of 1:4. With the help of corresponding wiring of the program input PPIN, the carrier can be switched off. Thus any other external carrier can be used.

Instruction interval

The interval between two given instructions (except the start instruction) is approximately 12 times the instruction length (incl. presignal) or 35536 CLKI clocks, respectively. This interval can be reduced to 30976 CLKI clocks in order to obtain diminished instruction intervals at lower clock frequencies.

Operation at low clock frequency

The prescaler (divide by 8) can be switched off. Thus, operation is possible at a clock frequency of approx. 500 kHz or 62.5 kHz, as required. The prescaler can only be switched off if — at low resistance — the IRA output is not forced to low (by means of a base-emitter space), e.g. in the case of wiring for front-end control.

Operation without switching transistor

During operations with a fixed supply voltage (ETA = low), the columns a to d are periodically interrogated (H pulse) in the normal sequence (as if an instruction is emitted) in order to permit an external synchronization.

After the supply voltage began to rise at 0 V, the flow of control is brought into a definite state and starts column interrogation. After having recognized a row in the "low" state, the flow of control is reset – then the flow corresponds until disconnection to the flow present during battery operations. After transmission has ended, the flow of control continues column interrogation, however, without any further output to IRA.

Multitransmitter operation

Without great increase in external circuitry, it is possible to cascade two SDA 2008 ICs so that they can be multiplexed to give out the instructions. For this purpose, the automatic resetting of the flow control and the instruction register are utilized which become effective as soon as both columns a and b are on high.

PPIN connections

Connect with:	Function
Column a	Shift into second instruction group (bit F = "1")
Column b	Shortened instruction interval
Column c	Startbit = "0"
Column d	No carrier of the IRA signal
IRA	Bridging the prescaler

(In the case of combinations of these functions, decoupling with diodes according to figure PPIN connection is necessary).

ETA connection

ETA = V_{DD}	Operation at constant supply voltage. If no row is set to "low", IRA is without output, however permanent column interrogation.
ETA to base of the voltage commutation transistor	Normal battery operation including disconnection of the supply voltage after the end instruction at open row combination.

Instruction set

No diodes at row 8
unshifted

Instr. No.	Code FED	CBA	Key
0	000	000	1a
1	000	001	1b
2	000	010	1c
3	000	011	1d
4	000	100	2a
5	000	101	2b
6	000	110	2c
7	000	111	2d
8	001	000	3a
9	001	001	3b
10	001	010	3c
11	001	011	3d
12	001	100	4a
13	001	101	4b
14	001	110	4c
15	001	111	4d
16	010	000	5a
17	010	001	5b
18	010	010	5c
19	010	011	5d
20	010	100	6a
21	010	101	6b
22	010	110	6c
23	010	111	6d
24	011	000	7a
25	011	001	7b
26	011	010	7c
27	011	011	7d
28	011	100	8a
29	011	101	8b
30	011	110	8c
31	011	111	8d

No diodes at row 8
shifted

Instr. No.	Code FED	CBA
32	100	000
33	100	001
34	100	010
35	100	011
36	100	100
37	100	101
38	100	110
39	100	111
40	101	000
41	101	001
42	101	010
43	101	011
44	101	100
45	101	101
46	101	110
47	101	111
48	110	000
49	110	001
50	110	010
51	110	011
52	110	100
53	110	101
54	110	110
55	110	111
56	111	000
57	111	001
58	111	010
59	111	011
60	111	100
61	111	101
62	111	110 } end instructions
62	111	110 }

With diodes at row 8
unshifted/shifted

Instr. No.	Code FED	CBA	Key
32	100	000	81a
33	100	001	81b
34	100	010	81c
35	100	011	81d
36	100	100	82a
37	100	101	82b
38	100	110	82c
39	100	111	82d
40	101	000	83a
41	101	001	83b
42	101	010	83c
43	101	011	83d
44	101	100	84a
45	101	101	84b
46	101	110	84c
47	101	111	84d
48	110	000	85a
49	110	001	85b
50	110	010	85c
51	110	011	85d
52	110	100	86a
53	110	101	86b
54	110	110	86c
55	110	111	86d
56	111	000	87a
57	111	001	87b
58	111	010	87c
59	111	011	87d

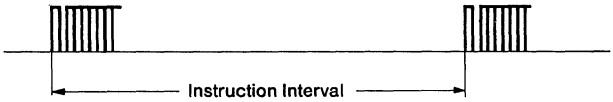
Special group
unshifted/shifted

Instr. No.	Code FED	CBA	Key
40	101	000	1L
41	101	001	2L
42	101	010	3L
43	101	011	4L
44	101	100	5L
45	101	101	6L
46	101	110	7L
47	101	111	8L

Instruction interval (prescaler switched on)

Interval	Interval in CLKI clocks	Interval in ms $f_{CLKI} = 500$ kHz	PPIN connected to column b
Normal	65536	approx. 131	———
Reduced	30976	approx. 62	X

Definition of the instruction interval



Hints for special functions

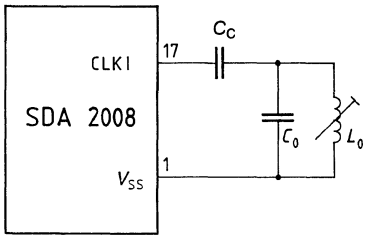
	IR remote control TV/radio sets	Front-end operation TV/radio sets	Transmission via AF cable	Remote control for model rail way	Typewriter keyboard	Time programmable remote control	TV games	Light switch remote control
Start bit changeover	X	X	X	X	X	X	X	
Shift into second group	X	X	X	X		X	X	
Diode matrix	X	X	X	X	X	X	X	
Special instruction group	X	X	X	X	X	X	X	
No carrier		X	X		X			
Bridged prescaler		X						
Shortened instruction interval			X	X				
No debounce delay								X
Special connection			X		X	X		

Pin description

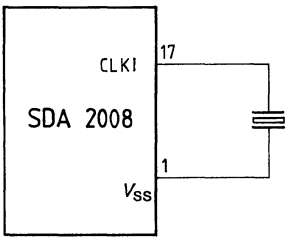
Pin	Function
1	V_{SS}, +supply voltage
2	Column a
3	Column b
4	Column c
5	Column d
6	V_{DD}, −supply voltage
7	ETA (switch-on transistor output)
8	IRA (infrared output)
9	Row 1
10	Row 2
11	Row 3
12	Row 4
13	Row 5
14	Row 6
15	Row 7
16	Row 8
17	CLKI (oscillator input)
18	PPIN (programming input)

Oscillator connection

1)

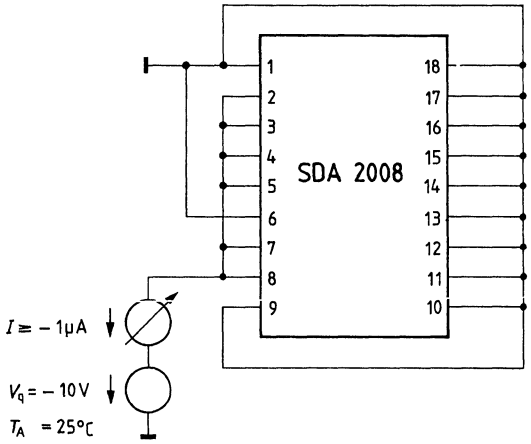


2)

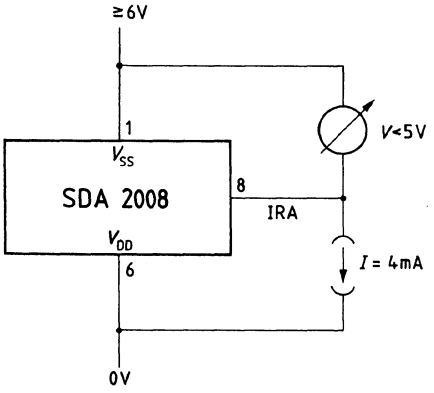


$C_C \geq 10\,nF \quad f_{CLKI} \approx \frac{1}{2\pi\sqrt{L_0\,C_0}}$

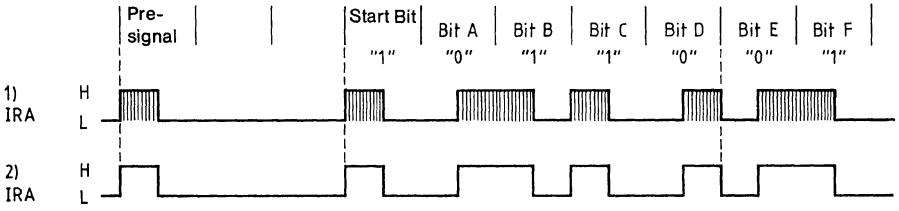
Leakage current, total current (test circuit)



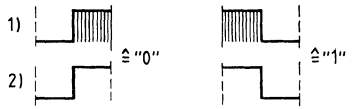
IRA remote control signal output (test circuit)



Biphase coding from instruction 011001

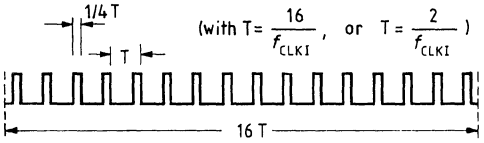


Def: for "0" and "1"

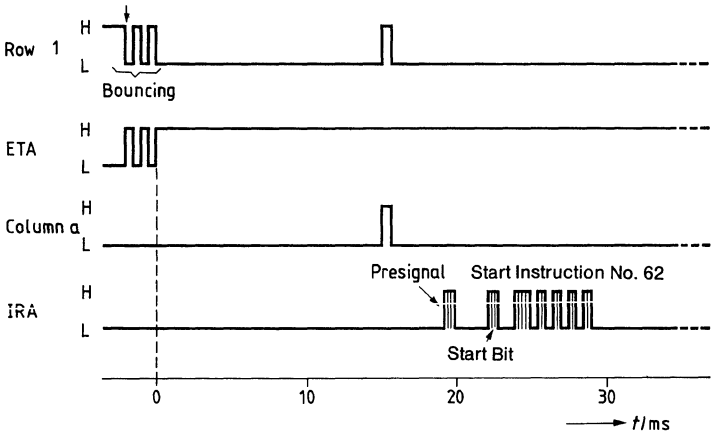


1) with Carrier
2) without Carrier

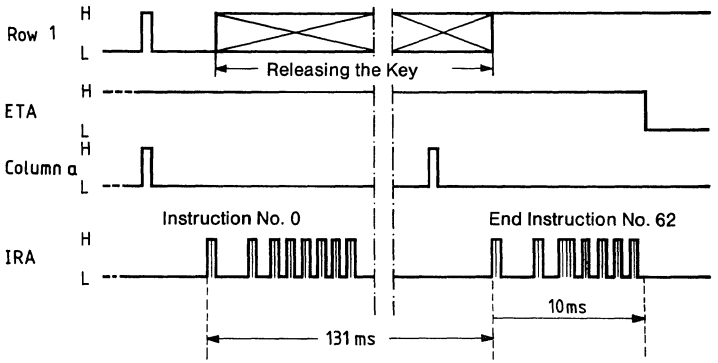
Exact Pulse Train of a Burst for 1):



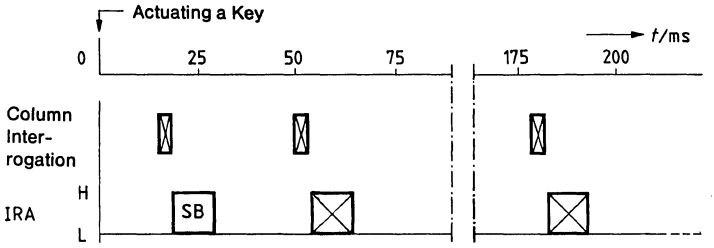
Actuating a key (e.g. 1a), f_{CLKI} = 500 kHz



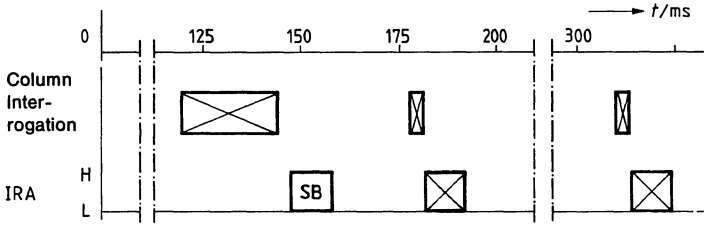
Releasing a key (1a), f_{CLKI} = 500 kHz



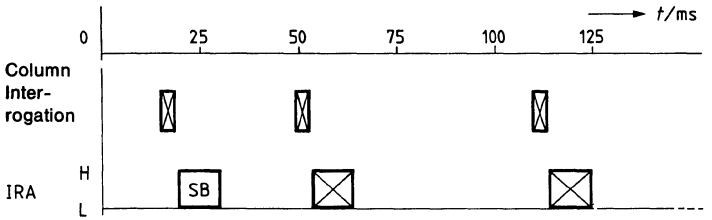
Instruction interval, f_{CLKI} = 500 kHz



PPIN at IRA (bridged prescaler) f_{CLKI} = 62.5 kHz

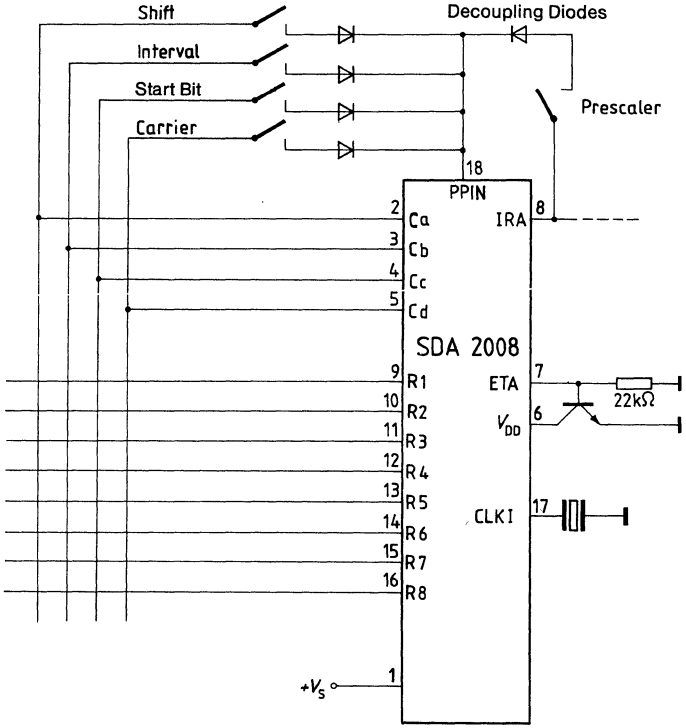


PPIN at column b (shortened instruction interval) f_{CLKI} = 500 kHz

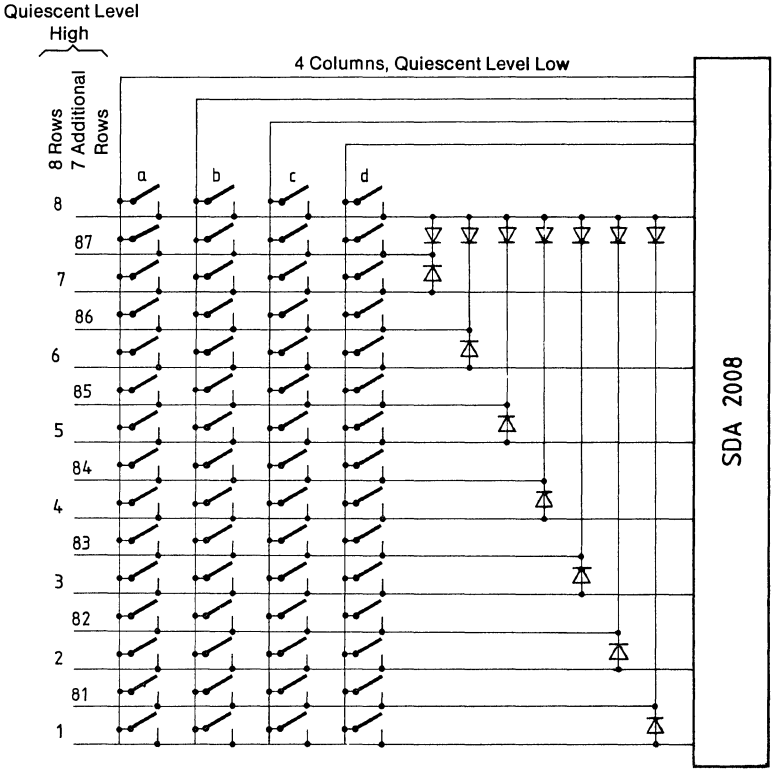


SB: = Instruction No. 62

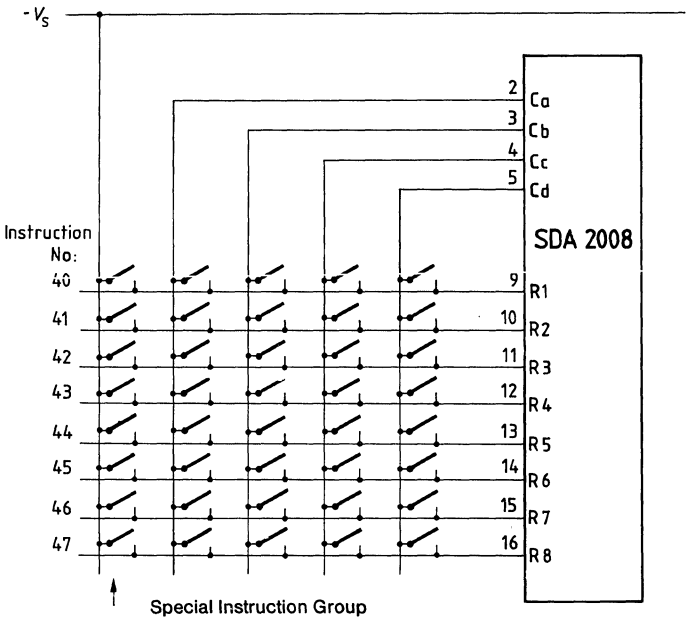
PPIN connection



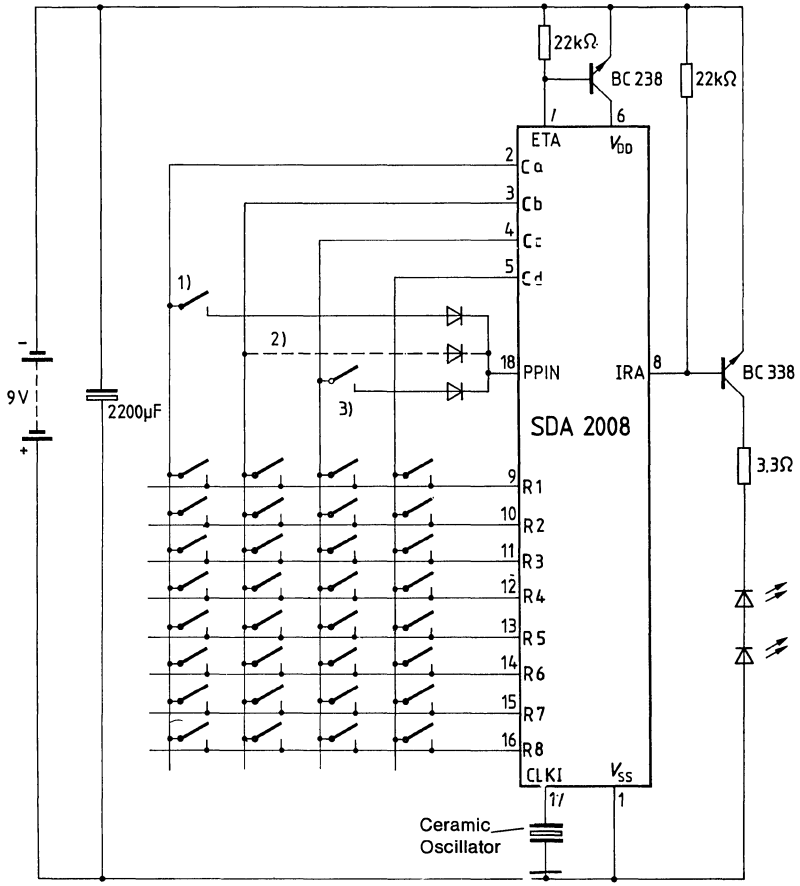
Extension for 60 instructions with additional diodes



$-V_S$ as fifth matrix column



Application circuit



1) Shift key
2) Connection for shortened instruction interval
3) Start bit changeover

If only one of these three possibilities is used, no diode is required.

Features

- Upgraded 8-bit CPU as compared to SAB 8051
- +5V supply voltage
- On-chip 4K/6K/8Kbyte ROM
- 128 byte internal RAM
  64 Kbyte RAM can be connected externally
  (internal and external RAM can be used simultaneously)
- 1 µs internal cycle with 12 MHz clock frequency
- 34 bidirectional I/O ports:
  - two 8-bit ports
  - one 8-bit multifunction port
  - one 8-bit port with 15 mA current sink per output
    (suited for direct LED MUX control)
- One serial I^2C bus interface (2-bit port open drain) suited for multi-master operation
- Input for direct modulated digital infrared signal processing
  (optimum carrier frequency is approx. 30 kHz)
- Powerful interrupt structure with 5 sources and 2 hierarchy levels
- Instruction set downward-compatible with existing programs for SDA 2010/2030/2110
- Power-down mode with internal RAM data retention and reduced power consumption
- Two 16-bit timers/counters
- Instructions for direct multiplication or division, execution time only 4 µs
- Boolean processor implementable for pure controlling tasks

Circuit description

The three components SDA 2040/2060/2080 are identical with respect to pin configuration and functions, they differ, however, in the size of the program memory.

This enables an individual matching to system requirements.

Software development is supported in two ways:

1) Replacement of functions with SDA 2082 and external program memory.
   Note: Usability of ports P0 and P2 is limited.
2) Replacement of functions and emulation with bond out chip SDA 3080 and piggyback.

A Siemens microcomputer development system (e.g. SME 232) can be used for SDA 2040/60/80 program development and system testing. Powerful edit, assembler and debug programs are available.

The SDA 2040/60/80, a successor type to the SAB 8051, belongs to the family of single-chip microcomputers, for which the operational emphasis is no longer placed on pure numeric control functions.

The SDA 2040/60/80, specially developed for entertainment electronic applications, can be recommended especially for those applications, where lowest component costs and high quantities are an essential requirement.

Architecture and instruction set are based on the SAB 8051 microcomputer. In the same manner as the SAB 8051, the SDA 2040/60/80 possesses a number of features that facilitate programming:

- variable allocation of RAM
- unrestricted stack location in RAM
- 4 register banks
- special function register
- memory mapped I/O

Individually addressable bits and a Boolean processor enable the programmer to improve software performance. Numeric problems can be solved in binary or in BCD arithmetic. The large number of instructions for processing binary functions also plays a part in increasing the performance of the computer as a controller. All of these features, when used appropriately, lead to a reduction of peripheral hardware, to a simplification of the software, and thus, to a reduction of development and component cost.

The SDA 2040/60/80 contains a 4K/6K/8Kbyte program memory (ROM), an internal 128 byte RAM (an additional 64Kbyte can be added externally, ref. SDA 2082 application example), two 16-bit timers/counters, a nested interrupt structure with two priority levels, and an integrated oscillator. Additionally, the computer can address 64Kbyte of external data memory. The 34 digital I/O ports comprise four 8-bit ports and a serial interface with data and clock lines. The serial I/O interface fully complies with the I^2C multimaster protocol. The IR input P3.0 can process modulated signals with a carrier frequency of approx. 30kHz. It contains a digital demodulator for deriving the envelope curve of modulated and inverted digital signals. As the digital demodulator is software enabled and disabled, it is also possible to use the IR port as a normal digital, quasi-bidirectional I/O port. The multifunction port P3 comprises two interrupt inputs and two counter inputs.

The instruction set, consisting of 49 one-byte, 46 two-byte, and 16 three-byte instructions, ensures efficient utilization of program memory. If a 12 MHz crystal is used, the execution time for the instructions is either 1 µs or 2 µs. The execution time for the very complex instructions for "multiply" and "divide" is only 4 µs. Information about the number of bytes and the execution time can be found in the instruction set summary for the SDA 2040/60/80.

Maximum ratings

Voltage between any pin and ground	V	−0.5 to 7	V
Total power dissipation	P_{tot}	2	W
Storage temperature range	T_{stg}	−40 to 125	°C

Operating range

Supply voltage	V_{CC}	5 ± 10%	V
Ambient temperature	T_A	0 to 70	°C

DC characteristics

$T_A = 0$ to 70 °C; $V_{CC} = 5$ V ±10%; $V_{SS} = 0$ V

		Test conditions	min	max	
L input voltage (all inputs except XTAL 2, P 4)	V_{IL}		−0.5	0.8	V
L input voltage (XTAL 2)	V_{IL1}		−0.5	0.6	V
L input voltage (P 4)	V_{IL2}		−0.5	1.5	V
H input voltage (except XTAL 2, RST/V_{PD}, P 4)	V_{IH}		2.0	$V_{CC}+0.5$	V
H input voltage (XTAL 2)	V_{IH1}		2.5	$V_{CC}+0.5$	V
H input voltage (RST)	V_{IH2}		2.5	$V_{CC}+0.5$	V
H input voltage (V_{PD})	V_{IH3}	$V_{CC} = 0$	4.5	5.5	V
H input voltage (P 4)	V_{IH4}		3.0	$V_{CC}+0.5$	V
L output voltage (port 0)	V_{qL}	$I_{qL} = 3.2$ A		0.45	V
L output voltage (port 0)	V_{qL1}	$I_{qL1} = 15$ mA		1.0	V
L output voltage (ports 1, 2 and 3)	V_{qL2}	$I_{qL2} = 1.6$ mA		0.45	V
L output voltage (ALE)	V_{qL2}	$I_{qL2} = 3.2$ mA		0.45	V
L output voltage (port1)	V_{qL3}	$I_{qL3} = 7.5$ mA		1.0	V
L output voltage (port 4)	V_{qL4}	$I_{qL4} = 3.0$ mA		0.4	V
H output voltage (ports 1, 2 and 3)	V_{qH}	$I_{qH} = -80$ µA	2.4		V
H output voltage (port 0 and ALE)	V_{qH1}	$I_{qH1} = -400$ µA	2.4		V
Current of internal pull-up resistance (P 1, P 2, P 3)	I_{LQ}	0.45 V = V_{IN} = V_{CC}	−800		µA
Leakage current of outputs	I_{LQ1}	0.45 V = V_{IN} = V_{CC}		± 10	µA
Current consumption (all outputs disconnected)	I_{CC}			150	mA
Current consumption (power-down mode)	I_{PD}	$V_{CC} = 0$ V		20	mA
Capacitance of inputs/outputs	C_{IQ}	$f_C = 1$ MHz		10	pF

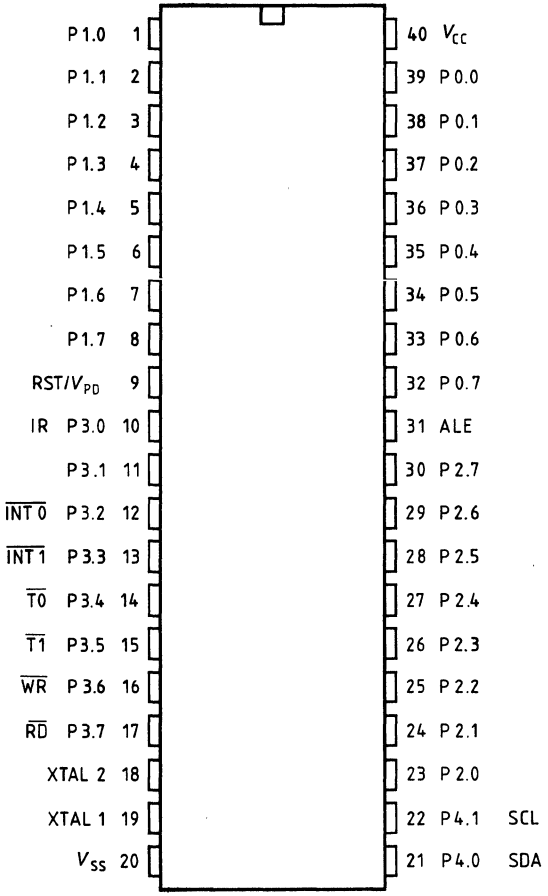
AC characteristics

$T_A = 0$ to 70 °C; $V_{CC} = 5$ V ± 10%; $V_{SS} = 0$ V

$C_L = 100$ pF (for port 0, and ALE output)
$C_L = 80$ pF (for all other outputs)

		Maximum ratings				
		Variable clock $1/t_{CLCL} = 1.2$–12 MHz		12 MHz clock		
		min	max	min	max	
Cycle time of oscillator	t_{CLCL}	83	833.3	83		ns
Min. cycle period	t_{CY}	12 t_{CLCL}	12 t_{CLCL}	1000		ns
ALE pulse width	t_{LHLL}	2 t_{CLCL}-40		127		ns
RD pulse width	t_{RLRH}	6 t_{CLCL}-100		400		ns
WR pulse width	t_{WLWH}	6 t_{CLCL}-100		400		ns

Pin configuration



Pin description

Symbol	Function
V_{SS}	GND 0 V
V_{CC}	+5 V
Port 0	Bidirectional 8-bit port with 3.2 mA current sink at 0.45 V and 15 mA current sink at 1.0 V for direct LED control (static or MUX operation).
Port 1	Bidirectional 8-bit port with 1.6 mA current sink at 0.45 V and 7.5 mA current sink at 1.0 V for direct LED display.
Port 2	Bidirectional 8-bit port with 1.6 mA current sink at 0.45 V.
Port 3	Bidirectional 8-bit port with 1.6 mA current sink at 0.45 V. Also includes the inputs of the interrupt and timer controls. For a program-controlled enabling of the function, the corresponding latch must be active high. The allocation of the special function registers is as follows: - $\overline{IR}$ (P 3.0) Input of the digital demodulator to generate an envelope curve of a standard modulated IR signal (inverted) - $\overline{INT\,0}$ (P 3.2) Input for interrupt 0 or for enabling/disabling the counter input T 0 - $\overline{INT\,1}$ (P 3.3) Input for interrupt 1 or for enabling/disabling the counter input T 1 - $\overline{T0}$ (P 3.4) Counter input T 0 - $\overline{T1}$ (P 3.5) Counter input T 1 - $\overline{WR}$ (P 3.6) Write strobe for external data memory (RAM) - $\overline{RD}$ (P 3.7) Read strobe for external data memory
Port 4	Bidirectional 2-bit port with open drain outputs, with 3 mA current sink at 0.4 V. Port 2 contains a bidirectional serial interface with DATA (SDA, pin 21) and CLOCK line (SCL, pin 22). The serial interface fully meets the requirements of the I^2C bus protocol.
RST/V_{PD}	At a connected supply voltage V_{CC} = 5 V, an edge transition from low to high (at approximately 3 V) resets the SDA 2040/60/80, i.e. the user program starts with address 0. When V_{PD} = high (approx. +5 V), a drop in V_{CC} triggers the processor's transition into the power-down mode. In this case, a current supply of max. 20 mA is provided to the RAM via pin RST/V_{PD}. In the case V_{PD} = 0 V and V_{CC} = 5 V, the RAM is supplied via V_{CC}.
ALE	Address Latch Enable output for controlling external memory access during normal operation.
XTAL1	Oscillator input for crystal operation. For external clock source connect to V_{SS}.
XTAL2	Oscillator output; required when crystal is used. Input during external clock supply.

SDA 2040/SDA 2060/SDA 2080 instruction set

Arithmetic operations

Mnemonic	Description	Bytes	Cycles
ADD A, Rn	Add register to Accumulator	1	1
ADD A, direct	Add direct byte to Accumulator	2	1
ADD A, @ Ri	Add indirect RAM to Accumulator	1	1
ADD A, # data	Add immediate data to Accumulator	2	1
ADDC A, Rn	Add register to Accumulator with Carry flag	1	1
ADDC A, direct	Add direct byte to A with Carry flag	2	1
ADDC A, @ Ri	Add indirect RAM to A with Carry flag	1	1
ADDC C, # data	Add immediate data to A with Carry flag	2	1
SUBB A, rn	Subtract register from A with Borrow	1	1
SUBB A, direct	Subtract direct byte from A with Borrow	2	1
SUBB A, @ Ri	Subtract indirect RAM from A with Borrow	1	1
SUBB A, # data	Subtract immediate data from A with Borrow	2	1
INC A	Increment Accumulator	1	1
INC Rn	Increment register	1	1
INC direct	Increment direct byte	2	1
INC @ Ri	Increment indirect RAM	1	1
DEC A	Decrement Accumulator	1	1
DEC Rn	Decrement register	1	1
DEC direct	Decrement direct byte	2	1
DEC @ Ri	Decrement indirect RAM	1	1
INC DPTR	Increment Data Pointer	1	2
MUL AB	Multiply A&B	1	4
DIV AB	Divide A&B	1	4
DA A	Decimal Adjust Accumulator	1	1

SDA 2040/SDA 2060/SDA 2080 instruction set

Logical operations

Mnemonic	Description	Bytes	Cycles
ANL A, Rn	AND register to Accumulator	1	1
ANL A, direct	AND direct byte to Accumulator	2	1
ANL A, @ Ri	AND indirect RAM to Accumulator	1	1
ANL A, # data	AND immediate data to Accumulator	2	1
ANL direct, A	AND Accumulator to direct byte	2	1
ANL direct, # data	AND immediate data to direct byte	3	2
ORL A, Rn	OR register to Accumulator	1	1
ORL A, direct	OR direct byte to Accumulator	2	1
ORL A, @ Ri	OR indirect RAM to Accumulator	1	1
ORL A, # data	OR immediate data to Accumulator	2	1
ORL direct, A	OR Accumulator to direct byte	2	1
ORL direct, # data	OR immediate data to direct byte	3	2
XRL A, Rn	Exclusive-OR register to Accumulator	1	1
XRL A, direct	Exclusive-OR direct byte to Accumulator	2	1
XRL A, @ Ri	Exclusive-OR indirect RAM to Accumulator	1	1
XRL A, # data	Exclusive-OR immediate data to Accumulator	2	1
XRL direct, A	Exclusive-OR Accumulatur to direct byte	2	1
XRL direct, # data	Exclusive-OR immediate data to direct byte	3	2
CRL A	Clear Accumulator	1	1
CPL A	Complement Accumulator	1	1
RL A	Rotate Accumulator left	1	1
RLC A	Rotate A left thorugh the Carry flag	1	1
RR A	Rotate Accumulator right	1	1
RRC A	Rotate A right through the Carry flag	1	1
SWAP A	Swap nibbles within the Accumulator	1	1

SDA 2040/SDA 2060/SDA 2080 instruction set

Data transfer operations

Mnemonic	Description	Bytes	Cycles
MOV A, Rn	Move register to Accumulator	1	1
MOV A, direct	Move direct byte to Accumulator	2	1
MOV A, @ Ri	Move indirect RAM to Accumulator	1	1
MOV A, # data	Move immediate data to Accumulator	2	1
MOV Rn, A	Move Accumulator to register	1	1
MOV Rn, direct	Move direct byte to register	2	2
MOV Rn, # data	Move immediate data to register	2	1
MOV direct, A	Move Accumulator to direct byte	2	1
MOV direct, Rn	Move register to direct byte	2	2
MOV direct, direct	Move direct byte to direct byte	3	2
MOV direct, @ Ri	Move indirect RAM to direct byte	2	2
MOV direct, # data	Move immediate data to direct byte	3	2
MOV @ Ri, A	Move Accumulator to indirect RAM	1	1
MOV @ Ri, direct	Move direct byte to indirect RAM	2	2
MOV @ Ri, # data	Move immediate data to indirect RAM	2	1
MOV DPTR, # data 16	Load Data Pointer with a 16-bit constant	3	2
MOVC A@A + DPTR	Move Code byte relative to DPTR to Accumulator	1	2
MOVC A@A + PC	Move Code byte relative to PC to Accumulator	1	2
MOVX A, @ Ri	Move External RAM (8-bit addr) to Accumulator	1	2
MOVX A, @ DPTR	Move External RAM (16-bit addr) to Accumulator	1	2
MOVX @ Ri, A	Move A to External RAM (8-bit addr)	1	2
MOVX @ DPTR, A	Move A to External RAM (16-bit addr)	1	2
PUSH direct	Push direct byte onto stack	2	2
POP direct	Pop direct byte from stack	2	2
XCH A, Rn	Exchange register with Accumulator	1	1
XCH A, direct	Exchange direct byte with Accumulator	2	1
XCH A, @ Ri	Exchange indirect RAM with Accumulator	1	1
XCHD A, @ Ri	Exchange low-order digital indirect RAM with A	1	1

SDA 2040/SDA 2060/SDA 2080 instruction set

Boolean variable manipulation

Mnemonic	Description	Bytes	Cycles
CLR C	Clear Carry flag	1	1
CLR bit	Clear direct bit	2	1
SETB C	Set Carry flag	1	1
SETB bit	Set direct bit	2	1
CPL C	Complement Carry flag	1	1
CPL bit	Complement direct bit	2	1
ANL C, bit	AND direct bit to Carry flag	2	2
ANL C,/bit	AND complement of direct bit to Carry	2	2
ORL C, bit	OR direct bit to Carry flag	2	2
ORL C,/bit	OR complement of direct bit to Carry	2	2
MOV C, bit	Move direct bit to Carry flag	2	1
MOV bit, C	Move Carry flag to direct bit	2	2

SDA 2040/SDA 2060/SDA 2080 instruction set

Program control operations

Mnemonic	Description	Bytes	Cycles
ACALL addr 11	Absolute subroutine call	2	2
LCALL addr 16	Long subroutine call	3	2
RET	Return from subroutine	1	2
RETI	Return from interrupt	1	2
AJMP addr 11	Absolute jump	2	2
LJMP addr 16	Long jump	3	2
SJMP rel	Short jump (relative addr)	2	2
JMP @ A + DPTR	Jump indirect relative to the DPTR	1	2
JZ rel	Jump if Accumulator is zero	2	2
JNZ rel	Jump if Accumulator is not zero	2	2
JC rel	Jump if Carry flag is set	2	2
JNC rel	Jump if Carry flag is not set	2	2
JB bit, rel	Jump if direct bit set	3	2
JNB bit, rel	Jump if direct bit not set	3	2
JBC bit, rel	Jump if direct bit is set and clear bit	3	2
CJNE A, direct, rel	Compare direct to A and jump if not equal	3	2
CJNE A, # data, rel	Compare immediate to A and jump if not equal	3	2
CJNE Rn, # data, rel	Compare immediate to register and jump if not equal	3	2
CJNE @ Ri, # data, rel	Compare immediate to indirect and jump if not equal	3	2
DJNZ Rn, rel	Decrement direct and jump if not zero	2	2
DJNZ direct, rel	Decrement direct and jump if not zero	3	2
NOP	No operation	1	1

Symbols and abbreviations

A	Accumulator	Rr	Register label (r=0-7)
adr	11-bit program memory address	Sn	S interface label (n = 0; 1)
CNT	Event counter	T	Timer
DA	D/A converter indication	T0, T1	Test 0, test 1
data	8-bit binary number	#	Refers to immediate data
P	Mnemonic for "in page" operation	@	Refers to indirect addressing
Pp	Port label (p = 0-3)		

PLCC 44

Features

- Upgraded 8-bit CPU as compared to SAB 8051
- +5 V supply voltage
- Program memory either 8 Kbyte internal ROM
  or 64 Kbyte external ROM
- Data memory 128 byte internal RAM
  64 Kbyte RAM can be connected externally
  (internal and external RAM can be used simultaneously)
- 1 µs internal cycle with 12 MHz clock frequency
- 34 bidirectional I/O ports:
  - two 8-bit ports
  - one 8-bit multifunction port
  - one 8-bit port with 15 mA current sink per output (suited for direct LED MUX control)
  - one serial I^2C bus interface, suited for multi-master operation
- Input for direct modulated digital infrared signal processing
  (optimum carrier frequency is approx. 30 kHz)
- Powerful interrupt structure with 5 sources and 2 hierarchy levels
- Instruction set downward-compatible with existing programs for SDA 2010/2030/2110
- Power-down mode with internal RAM data retention and reduced power consumption
- 16-bit timer/counter operation
- Instructions for direct multiplication or division, execution time only 4 µs
- Boolean processor implementable for pure controlling tasks

Circuit description

A special application of the SDA 2082 lies in program development support for the SDA 2040/60/80, the circuitry is shown in the application examples described in the following.

A Siemens microcomputer development system (e.g. SME 232) can be used for SDA 2082 program development and system testing. Powerful edit, assembler and debug programs are available.

An additional application of the SDA 2082 arises for individual control tasks and small quantity series, for which the development of a user-specific program for SDA 2040/60/80 operation is too expensive. An external program memory can be put to good use in this case, also offering short development times and more flexible possibilities for application.

Architecture and instruction set are based on the SAB 8051 microcomputer. In the same manner as the SAB 8051, the SDA 2082 possesses a number of features that facilitate programming:

- variable allocation of RAM
- unrestricted stack location in RAM
- 4 register banks
- special function register
- memory mapped I/O

Individually addressable bits and a Boolean processor enable the programmer to improve software performance. Numeric problems can be solved in binary or in BCD arithmetic. The large number of instructions for processing binary functions also plays a part in increasing the performance of the computer as a controller. All of these features, when used appropriately, lead to a reduction of peripheral hardware, to a simplification of the software, and thus, to a reduction of development and component cost.

The SDA 2082 contains an on-chip 8 Kbyte program memory. Operation is optionally with internal program memory ($\overline{EA}$ = high, pin 35) or external ($\overline{EA}$ = low, pin 35). Furthermore, the SDA 2082 contains an internal 128 byte RAM (an additional 64 Kbyte can be added externally, ref. application example), two 16-bit timers/counters, a nested interrupt structure with two priority levels, and an integrated oscillator. Additionally, the computer can address 64 Kbyte of external data memory. The 34 digital I/O ports comprise four 8-bit ports and a serial interface with data and clock lines. The serial I/O interface fully complies with the I^2C multimaster protocol. The IR input P3.0 can process modulated signals with a carrier frequency of approx. 30 kHz. It contains a digital demodulator for deriving the envelope curve of modulated and inverted digital signals. As the digital demodulator is software enabled and disabled, it is also possible to use the IR port as a normal digital, quasi-bidirectional I/O port. The multifunction port P3 comprises two interrupt inputs and two counter inputs.

The instruction set, consisting of 49 one-byte, 46 two-byte, and 16 three-byte instructions, ensures efficient utilization of program memory. If a 12 MHz cyrstal is used, the execution time for the instructions is either 1 µs or 2 µs. The execution time for the very complex instructions for "multiply" and "divide" is only 4 µs. Information about the number of bytes and the execution time can be found in the SDA 2082 instruction set summary.

Maximum ratings

Voltage between any pin and ground	V	−0.5 to 7	V
Total power dissipation	P_{tot}	2	W
Storage temperature range	T_{stg}	−40 to 125	°C

Operating range

Supply voltage	V_{CC}	5 ± 10%	V
Ambient temperature	T_A	0 to 70	°C

DC characteristics

$T_A = 0$ to 70 °C; $V_{CC} = 5$ V ±10%; $V_{SS} = 0$ V

		Test conditions	min	max	
L input voltage (all inputs except XTAL 2, P 4)	V_{iL}		−0.5	0.8	V
L input voltage (XTAL 2)	V_{iL1}		−0.5	0.6	V
L input voltage (P 4)	V_{iL2}		−0.5	1.5	V
H input voltage (except XTAL 2, RST/V_{PD}, P 4)	V_{iH}		2.0	$V_{CC}+0.5$	V
H input voltage (XTAL 2)	V_{iH1}		2.5	$V_{CC}+0.5$	V
H input voltage (RST)	V_{iH2}		2.5	$V_{CC}+0.5$	V
H input voltage (V_{PD})	V_{iH3}	$V_{CC} = 0$	4.5	5.5	V
H input voltage (P 4)	V_{iH4}		3.0	$V_{CC}+0.5$	V
L output voltage (port 0)	V_{qL}	$I_{qL} = 3.2$ A		0.45	V
L output voltage (port 0)	V_{qL1}	$I_{qL1} = 15$ mA		1.0	V
L output voltage (ports 1, 2, 3, PSEN and ALE)	V_{qL2}	$I_{qL2} = 1.6$ mA		0.45	V
L output voltage (port 1)	V_{qL3}	$I_{qL3} = 7.5$ mA		1.0	V
L output voltage (port 4)	V_{qL4}	$I_{qL4} = 3.0$ mA		0.4	V
H output voltage (ports 1, 2 and 3)	V_{qH}	$I_{qH} = -80$ µA	2.4		V
H output voltage (port 0, PSEN and ALE)	V_{qH1}	$I_{qH1} = -400$ µA	2.4		V
Current of internal pull-up resistance (P 1, P 2, P 3)	I_{LQ}	0.45 V ≤ $V_{IN} = V_{CC}$	−800		µA
Leakage current of outputs	I_{LQ1}	0.45 V ≤ $V_{IN} = V_{CC}$		± 10	µA
Current consumption (all outputs disconnected)	I_{CC}			150	mA
Current consumption (power-down mode)	I_{PD}	$V_{CC} = 0$ V, $V_{PD} = 5$ V		20	mA
Capacitance of inputs/outputs	C_{IQ}	$f_C = 1$ MHz		10	pF

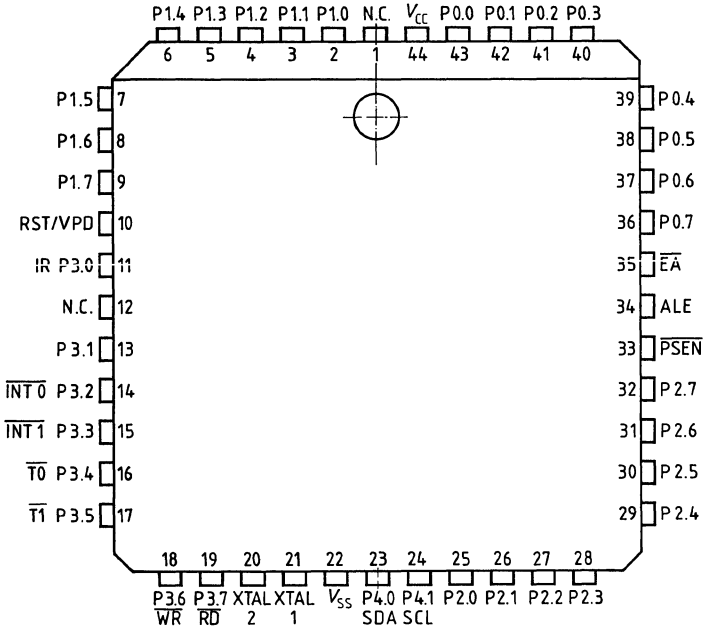
AC characteristics

$T_A = 0$ to 70 °C; $V_{CC} = 5$ V ±10%; $V_{SS} = 0$ V

$C_L = 100$ pF (for port 0, ALE and PSEN output)
$C_L = 80$ pF (for all other outputs)

		Maximum ratings				
		Variable clock $1/t_{CLCL} = 1.2$–12 MHz		12 MHz clock		
		min	max	min	max	
Cycle time of oscillator	t_{CLCL}	83	833.3	83		ns
Min. cycle period	t_{CY}	12 t_{CLCL}	12 t_{CLCL}	1000		ns
ALE pulse width	t_{LHLL}	2 t_{CLCL}-40		127		ns
RD pulse width	t_{RLRH}	6 t_{CLCL}-100		400		ns
WR pulse width	t_{WLWH}	6 t_{CLCL}-100		400		ns

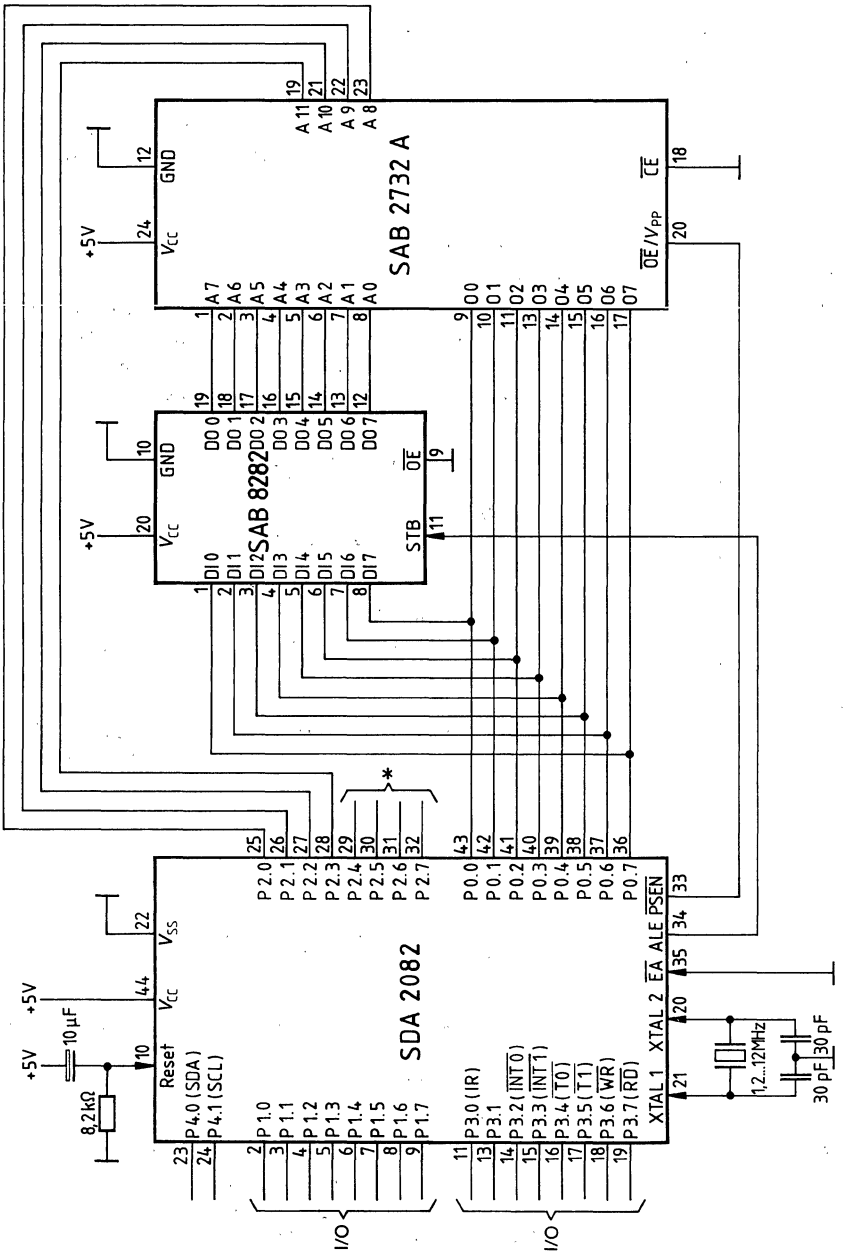
Pin configuration



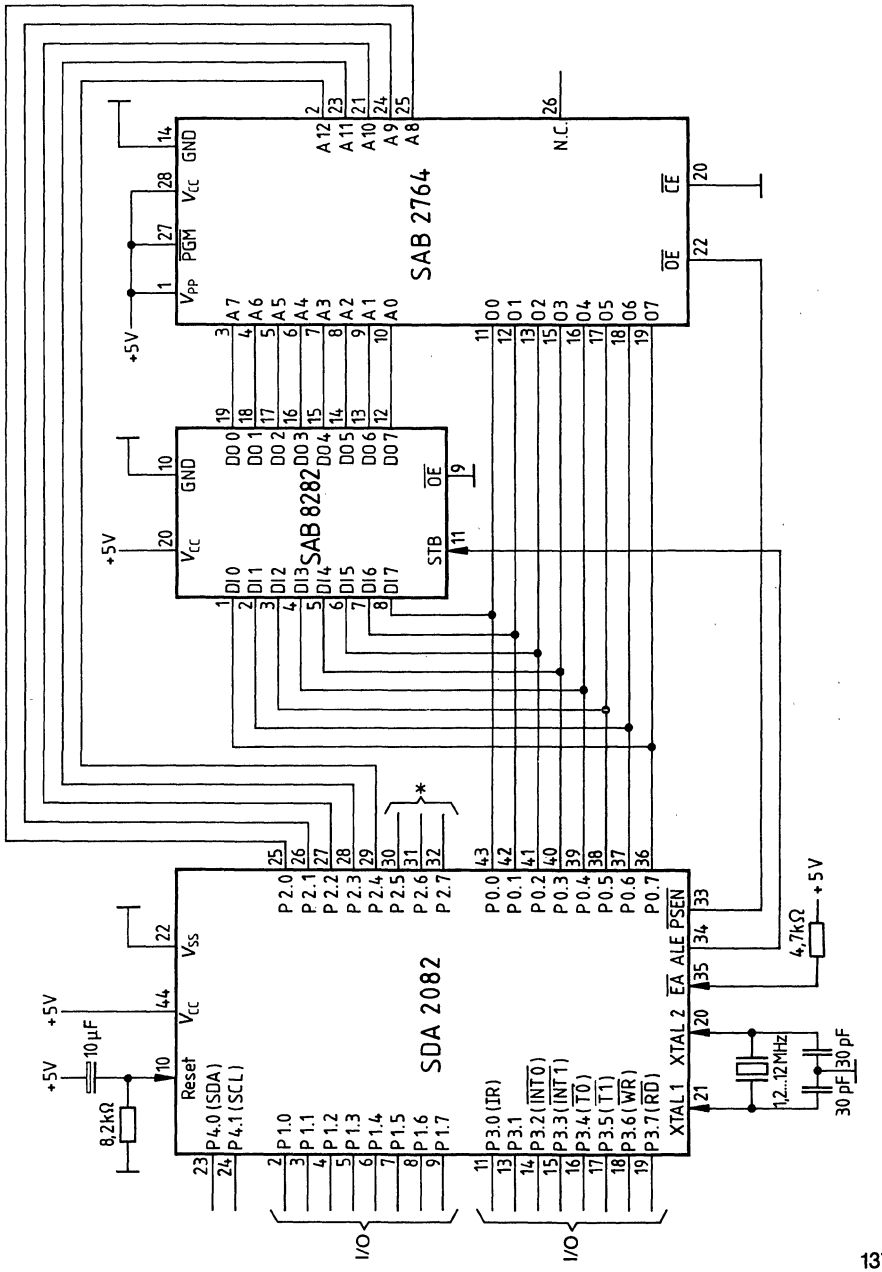
Pin description

Symbol	Function
V_{SS}	GND 0 V
V_{CC}	+5 V
Port 0	Bidirectional 8-bit port with open drain outputs with 3.2 mA current sink at 0.45 V and 15 mA current sink at 1.0 V for direct LED control (static or MUX operation).
Port 1	Bidirectional 8-bit port with 1.6 mA current sink at 0.45 V and 7.5 mA current sink at 1.0 V for direct LED display.
Port 2	Bidirectional 8-bit port with 1.6 mA current sink at 0.45 V.
Port 3	Bidirectional 8-bit port with 1.6 mA current sink at 0.45 V. Also includes the inputs of the various interrupt and time controls. For a program-controlled enabling of the function, the corresponding latch must be active high. Allocation of the special function registers is as follows: - IR (P 3.0) Input of the digital demodulator to generate an envelope curve of a standard modulated IR signal - $\overline{\text{INT 0}}$ (P 3.2) Input for interrupt 0 or for enabling/disabling the counter input T 0 - $\overline{\text{INT 1}}$ (P 3.3) Input for interrupt 1 or for enabling/disabling the counter input T 1 - $\overline{\text{T0}}$ (P 3.4) Counter input T 0 - $\overline{\text{T1}}$ (P 3.5) Counter input T 1 - $\overline{\text{WR}}$ (P 3.6) Write strobe for external data memory (RAM) - $\overline{\text{RD}}$ (P 3.7) Read strobe for external data memory
Port 4	Bidirectional 2-bit port with 3 mA current sink at 0.4 V. Port 2 contains a bidirectional, serial interface with DATA (SDA, pin 21) and CLOCK line (SCL, pin 22). The serial interfaces fully meet the requirements of the I²C bus protocol.
RST/V_{PD}	At a connected supply voltage V_{CC} = 5 V, an edge transition from low to high (at approximately 3 V) resets the SDA 2082, i.e. the user program starts with address 0. When V_{PD} = high (approx. +5 V), a drop in V_{CC} triggers the processor's transition into the power-down mode. In this case, a current supply of max. 20 mA is provided to the RAM via pin RST/V_{PD}. In the case V_{PD} = 0 V and V_{CC} = 5 V, the RAM is supplied via V_{CC}.
ALE	Address Latch Enable output for controlling external memory access during normal operation.
XTAL1	Oscillator input. Crystal or external source can be used
XTAL2	Oscillator output; required when crystal is used
$\overline{\text{PSEN}}$	Program Store Enable output for external memory access
$\overline{\text{EA}}$	External Access input; selects programm memory operating mode $\overline{\text{EA}}$ high means internal program memory (8 Kbytes), $\overline{\text{EA}}$ low means external program memory (max. 64 Kbytes)

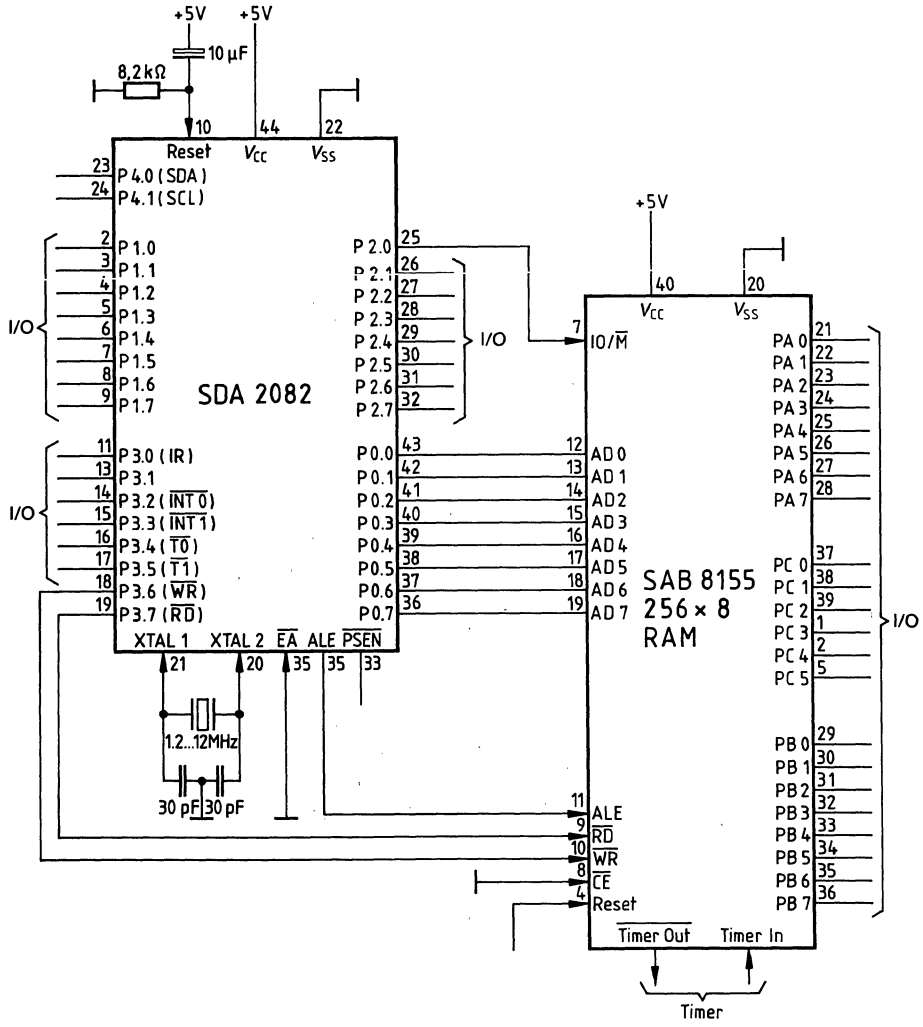
Application example for SDA 2082 with 4 Kbyte external program memory



Application example for SDA 2082 with 8 Kbyte external program memory



Application example for SDA 2082 with additional 256 byte external RAM and port expander



SDA 2082 instruction set

Arithmetic operations

Mnemonic	Description	Bytes	Cycles
ADD A, Rn	Add register to Accumulator	1	1
ADD A, direct	Add direct byte to Accumulator	2	1
ADD A, @ Ri	Add indirect RAM to Accumulator	1	1
ADD A, # data	Add immediate data to Accumulator	2	1
ADDC A, Rn	Add register to Accumulator with Carry flag	1	1
ADDC A, direct	Add direct byte to A with Carry flag	2	1
ADDC A, @ Ri	Add indirect RAM to A with Carry flag	1	1
ADDC C, # data	Add immediate data to A with Carry flag	2	1
SUBB A, Rn	Subtract register from A with Borrow	1	1
SUBB A, direct	Subtract direct byte from A with Borrow	2	1
SUBB A, @ Ri	Subtract indirect RAM from A with Borrow	1	1
SUBB A, # data	Subtract immediate data from A with Borrow	2	1
INC A	Increment Accumulator	1	1
INC Rn	Increment register	1	1
INC direct	Increment direct byte	2	1
INC @ Ri	Increment indirect RAM	1	1
DEC A	Decrement Accumulator	1	1
DEC Rn	Decrement register	1	1
DEC direct	Decrement direct byte	2	1
DEC @ Ri	Decrement indirect RAM	1	1
INC DPTR	Increment Data Pointer	1	2
MUL AB	Multiply A&B	1	4
DIV AB	Divide A&B	1	4
DA A	Decimal Adjust Accumulator	1	1

SDA 2082 instruction set

Logical operations

Mnemonic	Description	Bytes	Cycles
ANL A, Rn	AND register to Accumulator	1	1
ANL A, direct	AND direct byte to Accumulator	2	1
ANL A,@ Ri	AND indirect RAM to Accumulator	1	1
ANL A, # data	AND immediate data to Accumulator	2	1
ANL direct, A	AND Accumulator to direct byte	2	1
ANL direct, # data	AND immediate data to direct byte	3	2
ORL A, Rn	OR register to Accumulator	1	1
ORL A, direct	OR direct byte to Accumulator	2	1
ORL A, @ Ri	OR indirect RAM to Accumulator	1	1
ORL A, # data	OR immediate data to Accumulator	2	1
ORL direct, A	OR Accumulator to direct byte	2	1
ORL direct, # data	OR immediate data to direct byte	3	2
XRL A, Rn	Exclusive-OR register to Accumulator	1	1
XRL A, direct	Exclusive-OR direct byte to Accumulator	2	1
XRL A, @ Ri	Exclusive-OR indirect RAM to Accumulator	1	1
XRL A, # data	Exclusive-OR immediate data to Accumulator	2	1
XRL direct, A	Exclusive-OR Accumulator to direct byte	2	1
XRL direct, # data	Exclusive-OR immediate data to direct	3	2
CLR A	Clear Accumulator	1	1
CPL A	Complement Accumulator	1	1
RL A	Rotate Accumulator left	1	1
RLC A	Rotate A left through the Carry flag	1	1
RR A	Rotate Accumulator right	1	1
RRC A	Rotate A right through Carry flag	1	1
SWAP A	Swap nibbles within the Accumulator	1	1

SDA 2082 instruction set

Data transfer operations

Mnemonic	Description	Bytes	Cycles
MOV A, Rn	Move register to Accumulator	1	1
MOV A, direct	Move direct byte to Accumulator	2	1
MOV A, @ Ri	Move indirect RAM to Accumulator	1	1
MOV A, # data	Move immediate data to Accumulator	2	1
MOV Rn, A	Move Accumulator to register	1	1
MOV Rn, direct	Move direct byte to register	2	2
MOV Rn, # data	Move immediate data to register	2	1
MOV direct, A	Move Accumulator to direct byte	2	1
MOV direct, Rn	Move register to direct byte	2	2
MOV direct, direct	Move direct byte to direct byte	3	2
MOV direct, @ Ri	Move indirect RAM to direct byte	2	2
MOV direct, # data	Move immediate data to direct byte	3	2
MOV @ Ri, A	Move Accumulator to indirect RAM	1	1
MOV @ Ri, direct	Move direct byte to indirect RAM	2	2
MOV @ Ri, # data	Move immediate data to indirect RAM	2	1
MOV DPTR, # data 16	Load Data Pointer with a 16-bit constant	3	2
MOVC A @ A + DPTR	Move Code byte relative to DPTR to Accumulator	1	2
MOVC A @ A + PC	Move Code byte relative to PC to Accumulator	1	2
MOVX A, @ Ri	Move External RAM (8-bit addr) to Accumulator	1	2
MOVX A, @ DPTR	Move External RAM (16-bit addr) to Accumulator	1	2
MOVX @ Ri, A	Move A to External RAM (8-bit addr)	1	2
MOVX @ DPTR, A	Move A to External RAM (16-bit addr)	1	2
PUSH direct	Push direct byte onto stack	2	2
POP direct	Pop direct byte from stack	2	2
XCH A, Rn	Exchange register with Accumulator	1	1
XCH A, direct	Exchange direct byte with Accumulator	2	1
XCH A, @ Ri	Exchange indirect RAM with Accumulator	1	1
XCHD A, @ Ri	Exchange low-order digital indirect RAM with A	1	1

SDA 2082 instruction set

Boolean variable manipulation

Mnemonic	Description	Bytes	Cycles
CLR C	Clear Carry flag	1	1
CLR bit	Clear direct bit	2	1
SETB C	Set Carry flag	1	1
SETB bit	Set direct bit	2	1
CPL C	Complement Carry flag	1	1
CPL bit	Complement direct bit	2	1
ANL C, bit	AND direct bit to Carry flag	2	2
ANL C,/bit	AND complement of direct bit to Carry	2	2
ORL C, bit	OR direct bit to Carry flag	2	2
ORL C,/bit	OR complement of direct bit to Carry	2	2
MOV C, bit	Move direct bit to Carry flag	2	1
MOV bit, C	Move carry flag to direct bit	2	2

SDA 2082 instruction set

Program control operations

Mnemonic	Description	Bytes	Cycles
ACALL addr 11	Absolute subroutine call	2	2
LCALL addr 16	Long subroutine call	3	2
RET	Return from subroutine	1	2
RETI	Return from interrupt	1	2
AJMP addr 11	Absolute jump	2	2
LJMP addr 16	Long jump	3	2
SJMP rel	Short jump (relative addr)	2	2
JMP @ A + DPTR	Jump indirect relative to the DPTR	1	2
JZ rel	Jump if Accumulator is zero	2	2
JNZ rel	Jump if Accumulator is not zero	2	2
JC rel	Jump if Carry flag is set	2	2
JNC rel	Jump if Carry flag is not set	2	2
JB bit, rel	Jump if direct bit set	3	2
JNB bit, rel	Jump if direct bit not set	3	2
JBC bit, rel	Jump if direct bit is set and clear bit	3	2
CJNE A, direct, rel	Compare direct to A and jump if not equal	3	2
CJNE A, # data, rel	Compare immediate to A and jump if not equal	3	2
CJNE Rn, # data, rel	Compare immediate to register and jump if not equal	3	2
CJNE @ Ri, # data, rel	Compare immediate to indirect and jump if not equal	3	2
DJNZ Rn, rel	Decrement register and jump if not zero	2	2
DJNZ direct, rel	Decrement direct and jump if not zero	3	2
NOP	No operation	1	1

Symbols and abbreviations

A	Accumulator	Rr	Register label (r = 0-7)
adr	11-bit program memory address	Sn	S interface label (n = 0; 1)
CNT	Event counter	T	Timer
DA	D/A converter indication	T0, T1	Test 0, test 1
data	8-bit binary number	#	Refers to immediate data
P	Mnemonic for "in page" operation	@	Refers to indirect addressing
Pp	Port label (p = 0-3)		

Application-Oriented Single-Chip Microcomputer for Special Cost-Critical Applications

SDA 2110

DIP 28

Features

- 8-bit CPU, ROM, RAM, I/O in a DIP 28 package
- 21 digital I/O lines
  one serial interface
  one 8-bit interface
  two 4-bit interfaces
  one 1-bit interface
  two test inputs
- 1 Kbyte ROM
- 40 byte RAM
- 7.5 µs cycle time at 4 MHz crystal frequency – 1 or 2 cycles per instruction
- Zero passage detector
- Interface for modulated digital signal
- Interval timer/counter
- +5 V supply voltage
- RAM standby operation
- SAB 8048 instruction subset

Circuit description[1)]

The SDA 2110 introduces a new generation of highly economic single-chip computers with application-specific control functions. Considerable cost savings can be realized during the development and production stages, because the emphasis on specific applications reduces at the same time the number of additionally required hardware and simplifies the software tasks. Although the SDA 2110 was designed for electronic entertainment devices, it is equally suitable for mass-produced applications requiring highly economic components.

The SDA 2110 is eqipped with a 1 Kbyte program memory (ROM) and 40 byte data memory (RAM), which can be used in "standby" operation during heavily reduced output losses. The 21 digital I/O lines include one 8-bit port, two 4-bit ports, two test inputs, one serial interface and one single bit interface. Test input T0 processes signals modulated with approx. 30 kHz and is equipped with a digital demodulator, which derives the envelope curve from the modulated digital signal. Since the digital demodulator forwards an unmodulated signal without changing it, test input T0 can also function as a normal digital input during operation with standard H/L levels. Test input T1 includes a zero passage (crossing) detector and can also serve as a normal digital input. A data and pulse line comprise the serial interface. The component is equipped with its own oscillator and timer/counter.

1) Detailed description is available upon request

The instruction set includes 66 instructions (1-2 bytes) which can be processed in max. 2 cycles. Numerical problems can be processed in either binary or BCD arithmetic mode. The large number of bit-handling instructions increases the efficiency of the controller functions.

Program development and system testing for the SDA 2110 is carried out on the SME development system with the SDA 2110 emulator board EMB U21. The EMB U21 emulator consists of one 2K EPROM (SAB 2716) as well as a 40 pin socket which is used to insert an SAB 8035L type microprocessor or the ICE 48 plug. In addition, the EMB U21 contains all the necessary hardware to simulate the serial and parallel interfaces of the SDA 2110. A 28 wire cable is used to connect the U21 emulator with the user system.

A version without ROM (SDA 3110) is available which enables in-house software developments on an SME device.

Maximum ratings

Supply voltage range	V_{CC}	−0.5 to 7	V
Voltage between any pin and ground	V	−0.5 to 7	V
Total power dissipation	P_{tot}	1	W
Storage temperature range	T_{stg}	−40 to 125	°C

Operating range

Supply voltage	V_{CC}	5 ± 10%	V
Ambient temperature	T_A	0 to 70	°C

DC characteristics

$T_A = 0\,°C$ to $70\,°C$, $V_{CC} = V_{SB} = 5\,V \pm 10\%$; $V_{SS} = 0\,V$

			min	max	
L input voltage	(Ports, SS0, SS1, RESET, T0, T1, X1)	V_{iL}	−0.5	0.8	V
H input voltage	(Ports, SS0, SS1) $V_{CC} = 5.0\,V \pm 10\%$	V_{iH}	2.0	V_{CC}	V
H input voltage	(Ports, SS0, SS1) $V_{CC} = 6.0\,V \pm 0.5\,V$	V_{iH1}	2.4	V_{CC}	V
H input voltage	(RESET, X1, T0, T1)	V_{iH2}	3.5	V_{CC}	V
L output voltage	(Ports, ALE) $I_{qL} = 1.6\,mA$	V_{qL}		0.45	V
L output voltage	(SS0, SS1, SCP0, SCP1) $I_{qL} = 4\,mA$	V_{qL1}		0.45	V
H output voltage	(Ports, ALE) $I_{qH} = 50\,\mu A$	V_{qH}	2.4		V
H output voltage	(SS0, SS1, SCP1) $I_{qH} = 150\,\mu A$	V_{qH1}	2.4		V
H input current	(T0, T1) $V_{iH} = V_{CC}$	I_{iH}		10	µA
L input current	(Ports, SS0, SS1) $V_{iL} = 0.45\,V$	$-I_{iL}$	30	340	µA
Input voltage at T1	($C_i = 1\,\mu F$) (peak-to-peak)	V_{T1}	1	3	V
Zero passage detector current consumption		I_{CC}		60	mA

AC characteristics

$T_A = 0\,°C$ to $70\,°C$, $V_{CC} = V_{SB} = 5\,V \pm 10\%$; $V_{SS} = 0\,V$

Cycle time	3 MHz crystal = 10 µs	t_C	10	50	µs
ALE pulse width	$t_C = 10\,\mu s$	t_{ALE}	1.3		µs
Oscillator frequency deviation	$f = 2.5\,MHz$, $R = 15\,k\Omega$	Δf_{OSC}	−20	+20	%
Length of an unmodulated signal at the T0 test input	3 MHz crystal	t_{MT0}	60	—	µs
Frequency of a modulated signal at the T0 test input	3 MHz crystal	f_{TR}	30	35	kHz
Frequency range of the zero passage detector (input T1)		f_{T1}	0.03	1	kHz

Pin description

Pin	Symbol	Function
28	V_{CC}	+ 5 V
1	V_{SB}	+ 5 V standby supply
14	V_{SS}	GND 0 V
15, 16	X1, X2	Connection for crystal or similar
4–11	P0 0–7	Quasi-bidirectional 8-bit port
18–21	P2 0–3	Quasi-bidirectional 4-bit port
22–25	P3 0–3	Quasi-bidirectional 4-bit port
26	SS0	1-bit interface I/O pin
27	SS1	Serial interface S1 I/O pin
2	SCP1	Serial interface S1 clock pulse
17	RESET	Reset input for computer initialization (active H). Resets program counter, erases the status FFs, sets all digital outputs to H state.
3	T0	Input that can be tested with the conditional jump instruction JT0 and JNT0. The input contains a digital demodulator and can be used for the separation of the envelope curve from a modulated signal.
13	T1	Input that can be tested with the conditional jump instruction JT1 and JNT1. Serves simultaneously as an external counter input. (Selection of functions with instruction STRT CNT). The input can also be used for zero passage recognition of low frequency alternating voltages.
12	ALE	This output generates one clock pulse signal per cycle.

SDA 2110 instruction set

	Mnemonic	Description	Bytes	Cycles	Hexadecimal opcode
Accumulator	ADD A, Rr	Add register to A	1	1	68–6F
	ADD A, @ R	Add data memory to A	1	1	60–61
	ADD A, # data	Add immediate to A	2	2	03
	ADDC A, Rr	Add register with carry	1	1	78–7F
	ADDC A,@ R	Add data memory with carry	1	1	70–71
	ADDC A, # data	Add immediate with carry	2	2	13
	ANL A, Rr	And register to A	1	1	58–5F
	ANL A, @ R	And data memory to A	1	1	50–51
	ANL A, # data	And immediate to A	2	2	53
	ORL A, Rr	Or register to A	1	1	48–4F
	ORL A, @ R	Or data memory to A	1	1	40–41
	ORL A, # data	Or immediate to A	2	2	43
	XRL A, Rr	Exclusive Or register to A	1	1	D8–DF
	XRL A, @ R	Exclusive Or data memory to A	1	1	D0–D1
	XRL A, # data	Exclusive Or immediate to A	2	2	D3
	INC A	Increment A	1	1	17
	DEC A	Decrement A	1	1	07
	CLR A	Clear A	1	1	27
	CPL A	Complement A	1	1	37
	DA A	Decimal adjust A	1	1	57
	SWAP A	Swap nibbles of A	1	1	47
	RL A	Rotate A left	1	1	E7
	RLC A	Rotate A left through carry	1	1	F7
	RR A	Rotate A right	1	1	77
	RRC A	Rotate A right through carry	1	1	67

SDA 2110 instruction set

	Mnemonic	Description	Bytes	Cycles	Hexadecimal opcode
I/O	IN A, Pp	Input port to A	1	2	08, OC, OD
	OUT Pp, A	Output A to port	1	2	90, 3C, 3D
	IN A, S1	Input serial port to A0	1	2	OF
	IN A, S0	Input 1 bit port to A0	1	2	OE
	OUT S1, A	Output A0 to serial port	1	2	3F
	OUT S0, A	Output A0 to 1-bit port	1	2	3E
Sub-routines	CALL	Jump to subroutine	1	2	14, 34, 54, 74, 94, B4, D4, F4,
	RET	Return	1	2	83
Branches	JMP adr	Jump unconditional	2	2	04, 24, 44, 64, 84, A4, C4, E4
	JMPP @A	Jump indirect	1	2	B3
	DJNZ Rr, adr	Decrement register and jump on R not zero	2	2	E8–EF
	JC adr	Jump on carry = 1	2	2	F6
	JNC adr	Jump on carry = 0	2	2	E6
	JZ adr	Jump on A zero	2	2	C6
	JNZ adr	Jump on A not zero	2	2	96
	JT0 adr	Jump on T0 = 1	2	2	36
	JNT0 adr	Jump on T0 = 0	2	2	26
	JT1 adr	Jump on T1 = 1	2	2	56
	JNT1 adr	Jump on T1 = 0	2	2	46
	JTF adr	Jump on timer flag	2	2	16
Flags	CLR C	Clear carry	1	1	97
	CPL C	Complement carry	1	1	A7

SDA 2110 instruction set

	Mnemonic	Description	Bytes	Cycles	Hexadecimal opcode
Transfer instructions	MOV A, Rr	Move register to A	1	1	F8–FF
	MOV A,@ R	Move data memory to A	1	1	F0–F1
	MOV A, #data	Move immediate to A	2	2	23
	MOV Rr, A	Move A to register	1	1	A8–AF
	MOV@ R, A	Move A to data memory	1	1	A0–A1
	MOV Rr, # data	Move immediate to register	2	2	B8–BF
	MOV@R, # data	Move immediate to data memory	2	2	B0–B1
	XCH A, Rr	Exchange A and register	1	1	28–2F
	XCH A, @ R	Exchange A and data memory	1	1	20–21
	XCHD A, @ R	Exchange nibble of A and register	1	1	30–31
	MOVP A,@ A	Move to A from current page	1	2	A3
Timers/ Counters	MOV A, T	Read timer/counter	1	1	42
	MOV T, A	Load timer/counter	1	1	62
	STRT T	Start timer	1	1	55
	STRT CNT	Start counter	1	1	45
	STOP TCNT	Stop timer/counter	1	1	65
Re- gisters	INC Rr	Increment register	1	1	18–1F
	INC @ R	Increment data memory	1	1	10–11
	NOP	No operation	1	1	00

Symbols and abbreviations

A	Accumulator	Rr	Register label (r = 0–7)
adr	10-bit program memory address	Sn	S interface label (n = 0; 1)
CNT	Event counter	T	Timer
data	8-bit binary number	T0, T1	Test 0, Test 1
P	Mnemonic for "in page" operation	#	Refers to immediate data
Pp	Port label (p = 0, 2, 3)	@	Refers to indirect addressing

DIP 18

The SDA 2112-2 is fabricated in ASBC technology. In connection with a VCO (tuner) and a high-speed 1:64 divider, it forms a digitally programmable phase-locked loop for TV sets designed to use the PLL frequency sythesis tuning principle. The PLL enables crystal-controlled setting of the tuner oscillator frequency for a 125 kHz resolution in the frequency bands I/III, IV, and V.

A serial interface provides for simple connection to a microprocessor. The latter loads the programmable divider and the band-selection outputs with the appropriate information.

Features

- No external integrator necessary
- Internal buffer
- Microprocessor compatible

Maximum ratings

Supply voltage pin 18	V_{S1}	−0.3 to 7.5	V
Inputs			
Q 1, Q 2, F, $\overline{F}$ pin 1, 2, 15, 16	V_I	−0.3 to V_{S1} + 0.2	V
CPL, IFO, PLE pin 7, 8, 10	V_I	−0.3 to 5.5	V
Outputs			
UHF, VHF, Bd I/III pin 3, 4, 5	V_Q	−0.3 to 16	V
CLK (pin 6)	V_6	−0.3 to 16	V
	I_6	3	mA
$\overline{LDM}$ (pin 17)	V_{17}	−0.3 to 7.5	V
	I_{17}	3	mA
LOCK IND (pin 12)	V_{12}	−0.3 to V_{S1} + 0.2	V
PD (pin 14)	I_{14}	1	mA
V_D (pin 11)	V_{11}	−0.3 to 33	V
OSC (pin 13)	V_{13}	−0.3 to V_{S1} + 0.2	V
	I_{13}	8	mA
Junction temperature	T_j	140	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	80	K/W

Operating range

Supply voltage range	V_{S1}	4.5 to 7.15	V
Input frequency	$f_{F,\overline{F}}$	16	MHz
Divider factor	N	256 to 8191	
Crystal frequency	f_Q	3	MHz
Tuning voltage	V_D	0.3 to 33	V
Ambient temperature	T_A	0 to 70	°C

Characteristics

$V_{S1} = 5$ V; $T_A = 25$ °C

		Test circuit	min	typ	max	
Supply current, pin 18	I_{S1}			20	35	mA
Oscillator output, pin 13	V_{13H}	4	4.5			V
$R_{L2} = 3.5$ kΩ						
OSC	V_{13L}	4			0.7	V
$R_{L2} = 3.5$ kΩ						
Signal inputs F/$\bar{F}$, pin 15, 16						
Input voltage	V_{15H}	1	4.1		$V_{S1}+0.2$	V
	V_{15L}	1	3.8		$V_{S1}-0.1$	V
Input current	I_{15}	1			50	µA
$V_{15} = 5$ V						
Input sensitivity (peak-to-peak)	$V_{15,16}$	1	300		1200	mV
Sine push-pull $f = 16$ MHz						
Bus inputs CPL, IFO, PLE, pin 7, 8, 10						
Upper threshold voltage	V_{7u}	2	1.0	1.3	1.6	V
Lower threshold voltage	V_{7l}	2	0.5	0.7	1.0	V
Hysteresis	ΔV_7	2		0.6		V
H input current	I_{7H}	2			8	µA
$V_{7H} = 5$ V						
L input current	I_{7L}	2	−50			µA
$V_{7L} = 0.4$ V						
Band selection outputs UHF, VHF, Bd I/III pins 3, 4, 5						
Reverse current	I_{3H}	3			10	µA
$V_{3H} = 15$ V						
Forward current (current drain)	I_{3L}	3	0.8		1.7	mA
$2\text{V} \leq V_3 \leq 15$ V						
Clock output CLK, pin 6						
H output voltage	V_{6H}	4	14			V
$V_{S3} = 15$ V						
L output voltage	V_{6L}	4			1.5	V
$R_{L1} = 6.8$ kΩ						
Tuning section V_D, PD, pins 11, 14						
Tuning voltage	V_{11}	5	0.3		32.5	V
$V_{S2} = 33$ V						
Charge-pump current	I_{14}	5	−150	±100	150	µA
PLL locked						
PLL unlocked	I_{14}	5	−450	±300	450	µA

Characteristics (cont'd)
$V_{S1} = 15$ V; $T_A = 25$ °C

		Test circuit	min	typ	max	
Lock indication, pin 12						
H output voltage	$V_{12\,H}$	5	2.8			V
L output voltage	$V_{12\,L}$	5			0.4	V
Carry synchronous divider $\overline{\text{LDM}}$ Pin 17 (open collector)						
Reverse current $V_{17\,H} = 5$ V	I_{17}	1			10	µA
L output voltage $R_l = 5$ kΩ	$V_{17\,L}$				0.4	V
Switching times						
IFO, PLE						
Set-up time	t_S	2	2	1.5		µs
Hold time	t_H	2	2	1.5		µs
CLK						
H pulse width	t_{TH}	4		8.0		µs
L pulse width	t_{TL}	4		8.0		µs
HL transition time $R_{L1} = 6.8$ kΩ	t_{THL}	4	0		0.5	µs
LH transition time $C_{L1} = 50$ pF	t_{TLH}		0		1.5	µs
CPL						
H pulse width	t_{CH}	2	2	1.5		µs
L pulse width	t_{CLH}	2	2	1.5		µs
OSC						
H pulse width	t_{OH}	4	133			ns
L pulse width	t_{OL}	4			200	ns
HL transition time $R_{L2} = 3.5$ kΩ	t_{OHL}	4			20	ns
LH transition time $C_{L2} = 8$ pF	t_{OLH}	4			50	ns

Circuit description (refer to block diagram)

F, $\overline{F}$ A switchable 16/17 counter is triggered by the ECL signal inputs F/$\overline{F}$. The counter, in connection with a 4-bit and a 9-bit programmable, synchronous counter, forms a programmable, 13-bit synchronous divider using the dual-modulus technique, the 4-bit counter controlling the switchover from 16 to 17. Divider ratios of $N = 256$ to 8191 are possible. For test purposes the carry of the synchronous $\overline{LDM}$ divider is available at the $\overline{LDM}$ output (open collector).

The 16-bit shift register and latch is subdivided into 13 bits for storing the divider IFO ratio N and 3 bits for controlling the three band-selection outputs.

CPL The telegram is shifted in via the serial data input IFO with the HL edge of the PLE shift clock CPL when the enable input PLE is also on high level. First the complement of the divider ratio N, beginning with the LSB, is inserted in binary code, followed by the three control bits for the band-selection switching (see truth table). The 16-bit latch takes the data from the shift register when the enable input PLE is on low level.

Q1, Q2 The IC includes a crystal-controlled, 3-MHz clock oscillator. The output signal is divided down to 1.953125 kHz (reference signal) by a 1/1536 reference divider.

OSC The oscillator frequency appears at the TTL output OSC.

CLK The clock of 62.5 kHz is available at the open-collector output CLK.

PD The divided input signal is compared with the reference signal in a digital phase detector. If the falling edge of the input signal appears prior to the falling edge of the reference signal, the DOWN output of the phase detector turns to high level for the duration of this phase difference. In the reverse case the UP output turns to high level. If the two signals are in phase, both outputs remain at low level. The UP/DOWN outputs control the two current sources I^+ und I^- (charge pump). If the two outputs are low (PLL locked), the charge-pump output PD will turn to the high-impedance state (TRISTATE).

LOCK IND An L signal appears at the LOCK IND output if frequency and phase are synchronous. The current sources I^+ and I^- are then reduced from 300 to 100 µA.

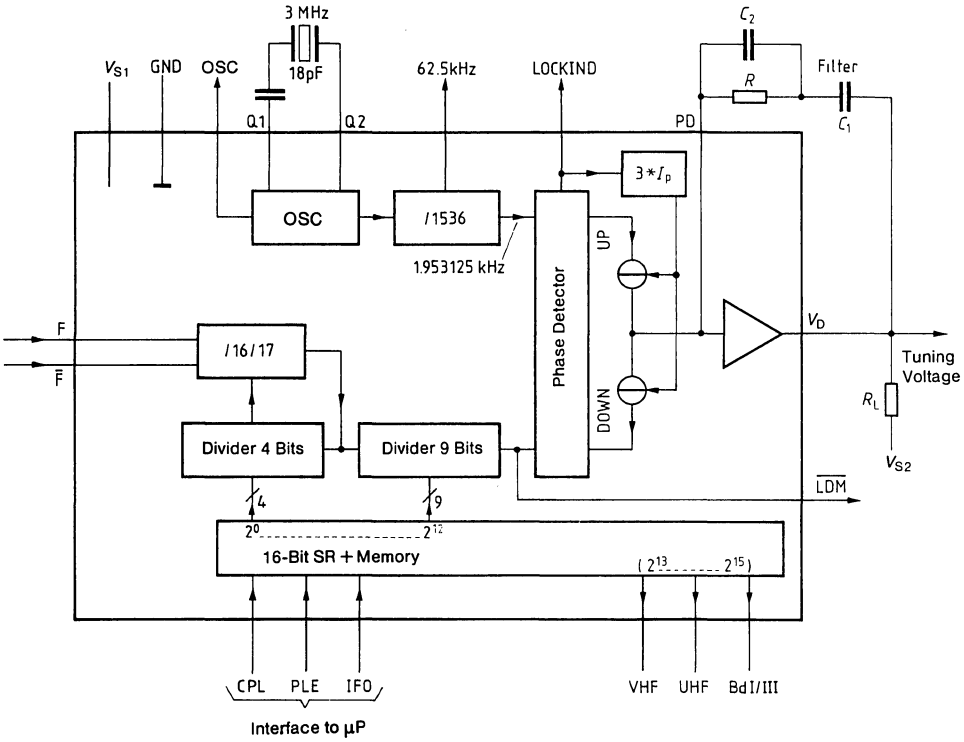
V_D The current pulses generated by the charge pump are integrated to form the tuning voltage by means of an active lowpass filter (external pull-up resistor to supply V_{S2} and external RC circuitry). The dc output signal appears at V_D and serves as a tuning voltage for the VCO.

UHF VHF Bd I/III The band-selection outputs (UHF, VHF, Bd I/III) contain current drains with open collectors. In this way PNP transistors working as band-selection switches can be connected directly without current-limiting resistors (see application circuit).

Pin description

Pin	Symbol	Function
1	Q 2	Crystal
2	Q 1	Crystal
3	UHF	} Band selection outputs
4	VHF	
5	Bd I/III	
6	CLK	Clock output
7	CPL	Clock input
8	IFO	Data input
9	GND	Ground
10	$\overline{PLE}$	Shift register enable input
11	V_D	Tuning voltage
12	LOCK IND	Lock indication output
13	OSC	Oscillator output
14	V_{PD}	Phase detector voltage
15	$\overline{F}$	Inverted input
16	F	Input
17	$\overline{LDM}$	Carry
18	V_{S1}	Supply voltage

Block diagram



Computation for loop filter

Loop bandwidth: $\omega_R = \sqrt{\frac{I_p \times K_{VCO}}{C_1 \times P \times N}}$

Attenuation: $\zeta = 0.5 \times \omega_R \times R \times C_1$

P = Prescaler
N = Programmable divider
I_p = Pump current
K_{VCO} = Tuner slope
R, C_1 = Loop filter

Example for channel 47:

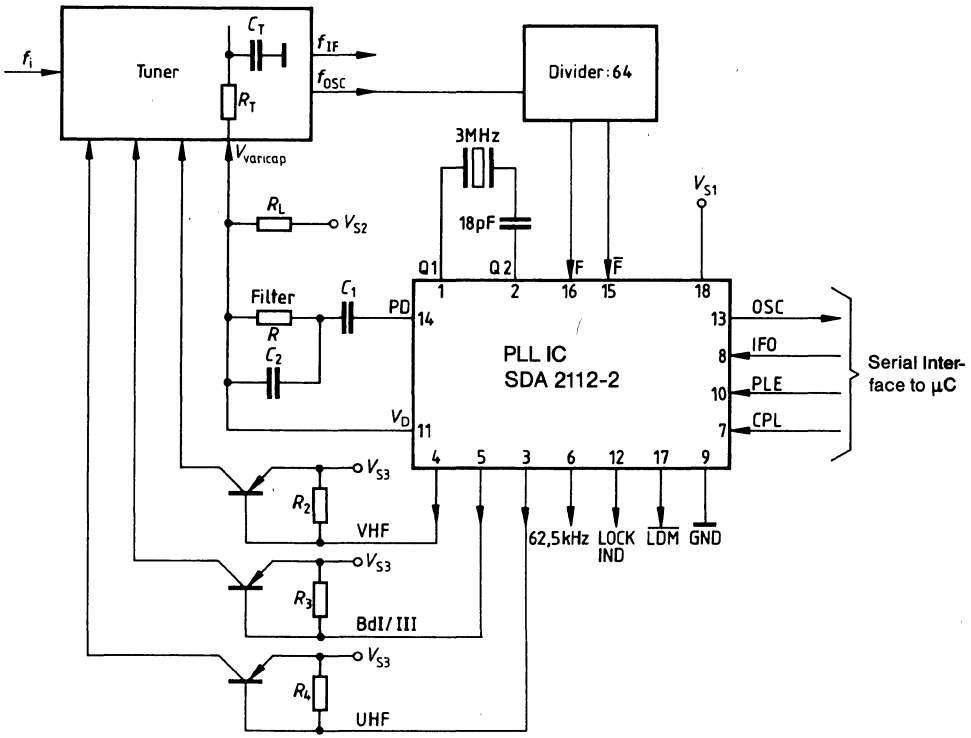
$P = 64$; $N = 5760$; $I_p = 100\ \mu A$; $K_{VCO} = 18.7$ MHz/V; $R = 33\ k\Omega$
$C_1 = 330$ nF; $\omega_R = 124$ Hz; $f_n = 20$ Hz; $\zeta = 0.675$

Post filter: $R_t = 10\ k\Omega$; $C_t = 47$ nF

Standard dimensioning: $C_2 = C_{1/5}$

$V_{S1} = 5$ V; $V_{S2} = 33$ V; $V_{S3} = 12$ V; R_2 to $R_4 = 22\ k\Omega$; $R_L = 22\ k\Omega$

Application circuit

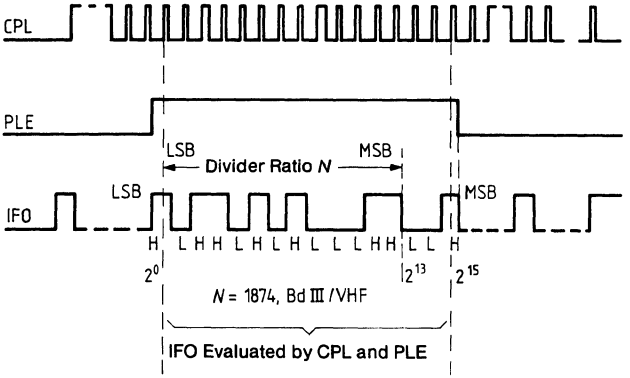


Truth table

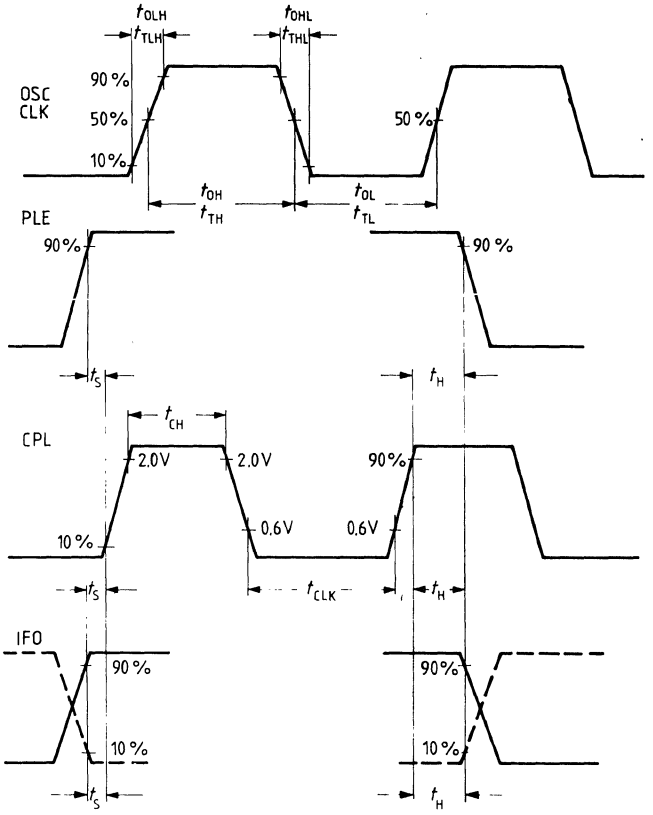
Input "IFO" bit			Outputs			Meaning
2^{13}	2^{14}	2^{15}	Bd I/III	VHF	UHF	
H	H	L	H	H	L	"UHF"
H	L	H	H	L	H	"Bd I/VHF"
L	L	H	L	L	H	"Bd III/VHF"
L	H	H	L	H	H	"Bd III/VHF"

At positive logic, the "IFO" bits $2^0 \ldots 2^{12}$ complement the dual code from divider ratio *N*.

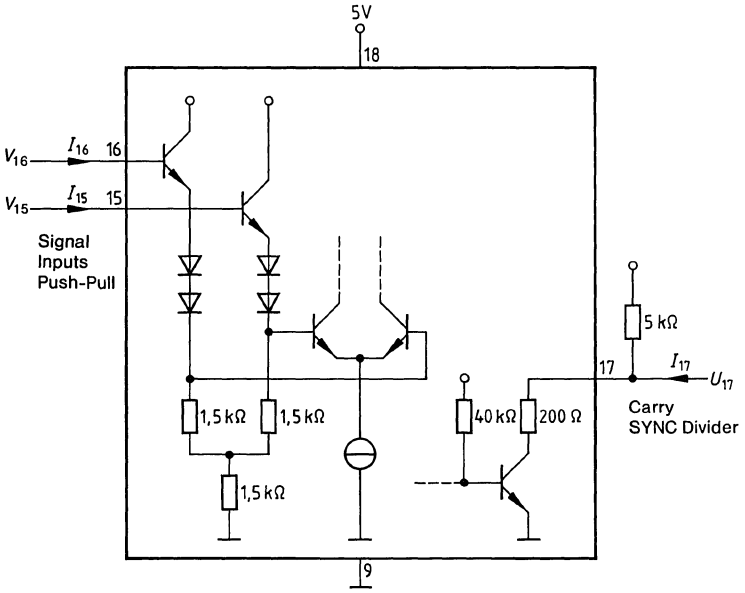
Pulse diagram



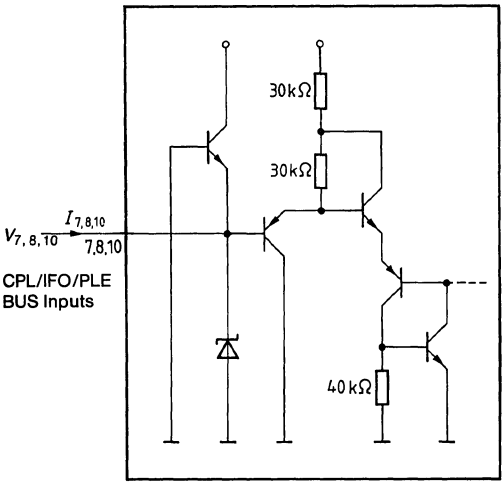
Pulse diagram



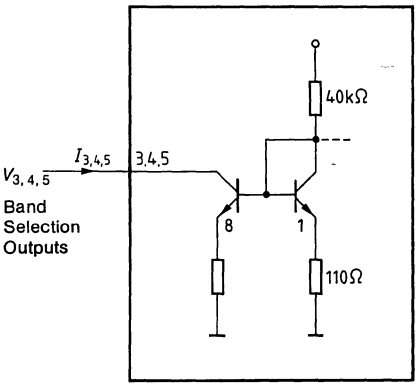
Test and measurement circuits



Test circuit 1

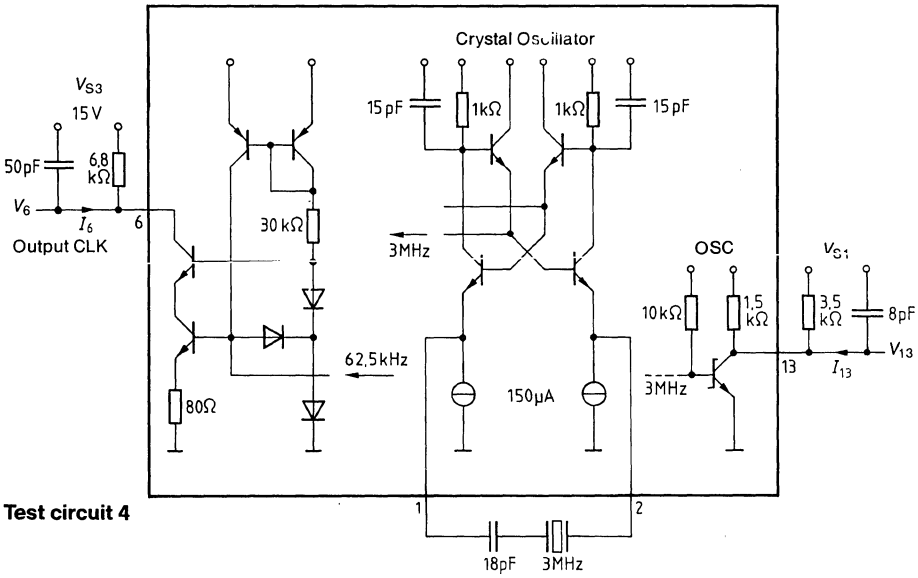


Test circuit 2

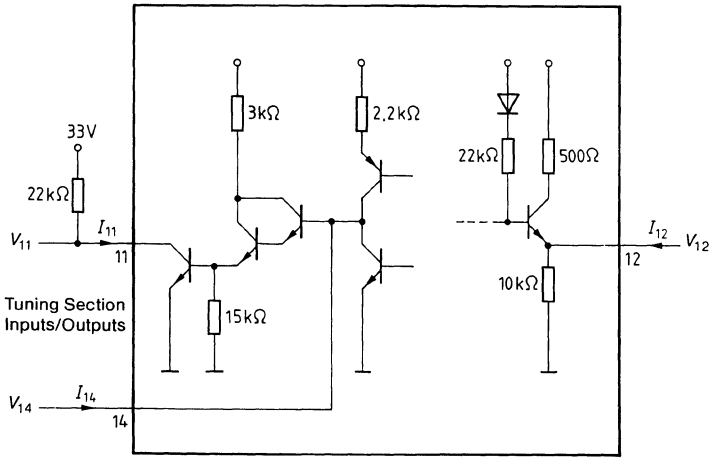


Test circuit 3

Test and measurement circuits



Test circuit 4



Test circuit 5

DIP 22

The SDA 2120 contains the complete digital section (reference oscillator, 20-bit shift register with memory, programmable divider, band select outputs as well as a phase detector, two charge pumps, one current multiplier, and two amplifiers) for tuning an AM/FM receiver by PLL frequency synthesis.

A serial interface facilitates connection to a microprocessor. The microprocessor will load the divider, the band select outputs, and the current multiplier with the suitable information.

Features

- Integrated prescaler
- Switch-selectable from AM to FM
- High frequency resolution FM = 12.5 kHz, AM = 0.5 kHz

Maximum ratings

Supply voltage	V_S	7.5	V
Tuning supply voltage	V_{SAM}/V_{SFM}	32	V
IFO, PLE, CPL	V_{iH}	5.5	V
Band select: UKW, SW, MW, LW	V_{BS}	18	V
AM, FM	$V_{AM/FM}$	5.5	V
F	V_F	5.5	V
Input current amplifier	I_{iV}	500	µA
Output current amplifier	$I_{DAM/FM}$	7	mA
Junction temperature	T_j	140	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	65	K/W

Operating range

Supply voltage	V_S	4.5 to 5.5	V
Ambient temperature range	T_{amb}	−25 to 85	°C
Resistance for charge pump current[1])	R_I	> 100	kΩ
Input frequency input AM	f_{iAM}	10	MHz
Input frequency input FM	f_{iFM}	120	MHz
Prescaler factor LW/MW	$N_{LW/MW}$	2 / 16383	
Prescaler factor SW/UKW	$N_{SW/UKW}$	4097 / 16383	

1) Multiplication factor $M = 15$

Characteristics ($V_S = 5$ V; $T_{amb} = 25$ °C)

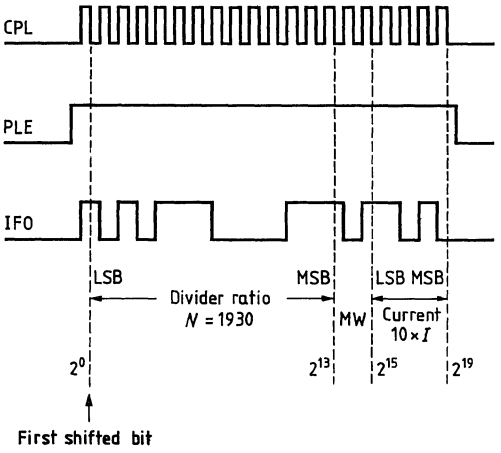
		min	typ	max	
Supply current	I_S		60		mA
L tuning voltage V_{tunAM}/V_{tunFM} ($I_{DL} = 2.5$ mA)	V_{DL}			0.5	V
H tuning voltage V_{tunAM} ($V_{S2} = 32$ V)	V_{tunHAM}	30			V
H tuning voltage V_{tunFM} ($V_{S2} = 32$ V)	V_{tunHFM}	30			V
Sensitivity input AM ($f = 10$ MHz)	$V_{iAM\,rms}$		10		mV
Sensitivity input FM ($f = 120$ MHz)	$V_{iFM\,rms}$		20		mV
Input resistance input AM ($f = 10$ MHz; $V_{iAMrms} = 100$ mV)	R_{iAM}		1		kΩ
Input resistance input FM ($f = 120$ MHz; $V_{IFMrms} = 100$ mV)	R_{iFM}		0.5		kΩ
input capacitance, input AM/FM	C_i		4		pF
Inputs IFO, PLE, CPL					
Upper threshold voltage	V_{Su}	2.0[1]			V
Lower threshold voltage	V_{Sl}			0.8[1]	V
H input current	I_{iH}			8	μA
L input current	I_{iL}			−50	μA
BS outputs: UKW, SW, MW, LW					
($V_{pp} = 15$ V)	I_{qH}			10	μA
($0.5\text{ V} \leq V_{pp} = 15$ V)	I_{qL}	0.8	1.2	3.0	mA
Oscillator output F					
($I_{FH} = -100$ μA)	V_{qFH}	4.5			V
($I_{FL} = 100$ μA)	V_{qFL}			0.7	V
Residual ripple of the tuning voltage ($f = 0$–1 kHz, test bandwidth 10 Hz)	V_{tunAM}		5		μV
($f = 1$–50 kHz, test bandwidth 100 Hz)	V_{tunFM}		1		μV
Charge pump output current AM/FM ($R_l = 130$ kΩ, $M = 15$,	I_{qAI}		±500		μA
I_{qAI} tested against 2.5 V) tristate			±5		nA
Switching times					
IFO, PLE					
Set-up time for enable	t_{SE}	0.3			μs
Set-up time for data	t_{SD}	0.4			μs
Hold time for enable	t_{HE}	3			μs
Hold time for data	t_{HD}	3			μs
CPL					
H pulse width	t_{CH}	2			μs
L pulse width	t_{CL}	2			μs
F					
H pulse width	t_{FH}	200			ns
L pulse width	t_{FL}			300	ns
H/L transition time ($C_{L2} = 10$ pF)	t_{FHL}			20	ns
L/H transition time ($C_{L2} = 10$ pF)	t_{FLH}			50	ns

1) Values apply throughout the operational range.

Truth table

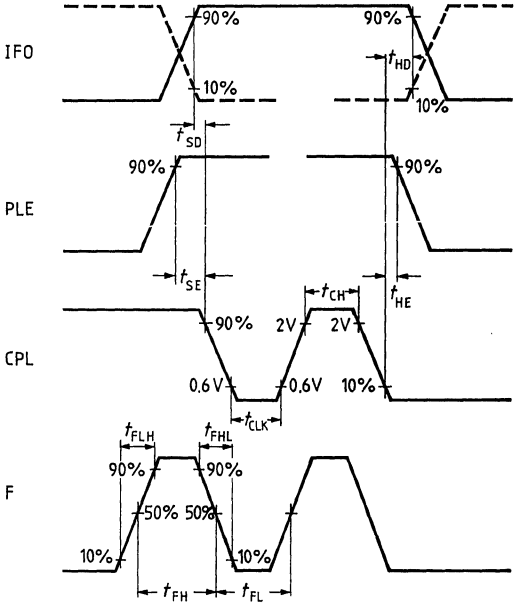
Function	"IFO" 2^{14}	bit 2^{15}	Band select outputs LW	MW	SW	UKW	f_{ref}/kHz	Active input	Active output
LW	L	L	H	H	H	H	0.5	AM	AI AM
MW	L	H	H	L	H	H	0.5	AM	AI AM
SW	H	L	H	H	L	H	0.5	AM	AI AM
UKW	H	H	H	H	H	L	12.5	FM	AI FM

Pulse diagram



Pulse diagram

Set-up and hold times



Circuit description

The component contains a 14 bit programmable synchronous divider (% P, % M, % S), which divides the frequency of a signal pending at input AM, or FM resp. by the factor N=2...16383 (LW/MW), or N = 4097...16383 (SW/VHF). The buffered inputs AM and FM can be directly connected to the VCO via capacitors due to their own prevoltage generation.

The input sensitivity of the inputs is 10 mV_{rms} (AM) or 20 V_{rms} (FM). The frequency divider input can be switched optionally to AM or FM per software switch. While the LW/MW signal is divided into a pure synchronous divider, the SW/VHF signal is divided into a modulo two divider followed by a synchronous divider. The shift register with latch, with a depth of 20 bits, is divided into 14 bits to store the divider ratio N of the synchronous divider; 2 bits to control the four band select outputs (VHF, SW, MW, LW); 4 bits for the current multiplier to select the optimum current for the charge pump.

The divider ratio N, the band selection, as well as the information for the current multiplier are loaded into the 20 bit shift register via the serial data input IFO. First, the complement of the divider ratio, beginning with the least significant bit, is loaded in a binary encoded form. This is followed by the band select control bits SB0 und SB1 (refer to table), finished by the information bits for the current multiplier. During FM operation, they are loaded in binary encoded form beginning with the LSB, during which the bit sequence 0000 is not permissible. During AM operation, the complement of the information bit is loaded in binary encoded form beginning with the LSB, during which the bit sequence 1111 is not permissible. The information is loaded with the HL slope of the shift pulse CPL. Acceptance of the data at the IFO input can only take place during the H state of the enable input PLE. The 20 bit latch accepts the data from the shift register during the L state of the enable input PLE. The component is equipped with its own crystal-controlled 4 MHz pulse oscillator.

A square-wave signal of 2 MHz derived from the pulse oscillator is available at output F, which can be used for the synchronization of peripheral devices (e.g. microprocessor). The output F is to be connected to ground in order to provide a high signal-to-noise ratio. The oscillator output signal (f_{OSC} = 4 MHz) is divided down to 0.5 kHz or 12.5 kHz respectively, by a switch-selectable reference divider (reference signal). The reference divider is switched by the same signal that also switches the inputs. The divided input signal is compared with the reference signal in a digital phase detector. If the falling edge of the divided input signal appears prior to the falling edge of the reference signal, the DOWN output of the phase detector goes into the H state for the duration of the phase difference. In the opposite case, the output UP goes into the L state. If both signals are in phase, the DOWN output remains in the L state and output UP in the H state.

The outputs UP/DOWN control the two current sources I^+ and I^- (charge pump). If output UP is in the L state, current source I^+ is activated; if output DOWN is in the H state, current source I^- is in effect. If DOWN is in the L state and UP is in the H state, the charge pump output changes into a high-ohmic state (TRI STATE). The current pulses generated by the charge pump are integrated with the aid of an active low pass (external FET op amp with *RC* circuitry). The DC output signal of the low pass is available at the FET op amp output and serves as tuning voltage for the VCO. If there are minor requirements to be met regarding the signal-to-noise ratio, an internal amplifier with a series-connected external darlington transistor can be used instead of the external FET op amp. The output stage of the internal amplifier comprises a transistor with open-collector output. The external collector resistor can then be connected to voltages up to 30 V. The output transistor is dimensioned such that a voltage drop of 0.5 V occurs at a 2.5 mA collector current.

The component contains two separate charge pumps and two separate amplifiers. Only one charge pump is active at a time. The switch-over is achieved by the same signal that also switches the AM/FM inputs. Thus, separate low passes can be set up for AM and FM. The output current of both charge pumps (source current = sink current) is $M \times I$. M is the multiplication factor that is given by the information bits for the current multiplier, M being an integer and $1 \leq M \leq 15$. I is the basic current of the charge pump that is set by means of an external resistor between pin I_{ref} and V_S. As the software monitors the current, a fast transient response of the PLL during band limit peaks and range changes (recharging the low pass) can be achieved, as well as a high signal-to-noise ratio in the steady state. The delay time between phase detector input and charge pump output is typically 20 ns. The phase detector with charge pump gain depends on the selected charge pump output current and is calculated as follows:

$$K_D = \frac{2\,I}{4\,\pi}\left[\frac{\mu A}{\text{rad}}\right].$$

The wiring of the charge pump output AI has to ensure that the DC voltage value at the output varies only between 1.2 V and 3.8 V (e.g. by applying a reference voltage of approx. 2.5 V when using the external operational amplifier. The band select outputs contain current drains (I_{QL} = 0.8 to 3.0 mA) with open collectors, in order to be able to switch voltages greater than the supply voltage of the component (5 V). Thus the transistors, operating as band select switches, can be directly driven without current limiting resistors (refer to application circuit).

During operation, pin 2 (N.C.) must be connected to ground.

Supplements to the circuit description

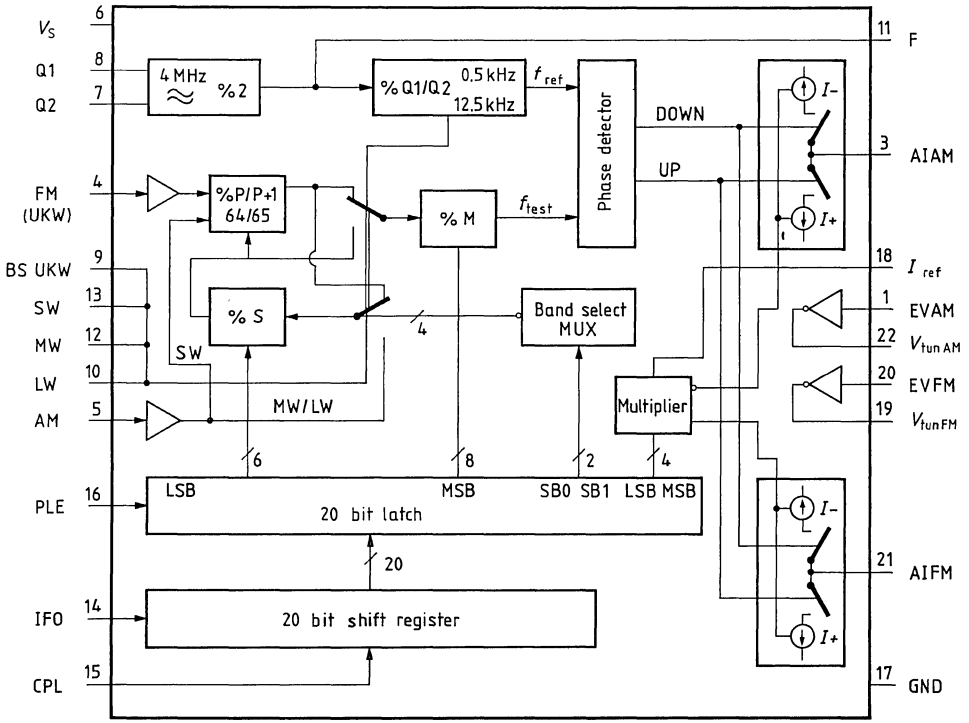
Relationship between IFO bits of current multiplier and multiplication factor for the output current of the charge pump.

IFO BIT				Multiplication factor *M*	Multiplication factor *M*
2^{16}	2^{17}	2^{18}	2^{19}	FM	AM
L	L	L	L	0	15
H	L	L	L	1	14
L	H	L	L	2	13
H	H	L	L	3	12
L	L	H	L	4	11
H	L	H	L	5	10
L	H	H	L	6	9
H	H	H	L	7	8
L	L	L	H	8	7
H	L	L	H	9	6
L	H	L	H	10	5
H	H	L	H	11	4
L	L	H	H	12	3
H	L	H	H	13	2
L	H	H	H	14	1
H	H	H	H	15	0

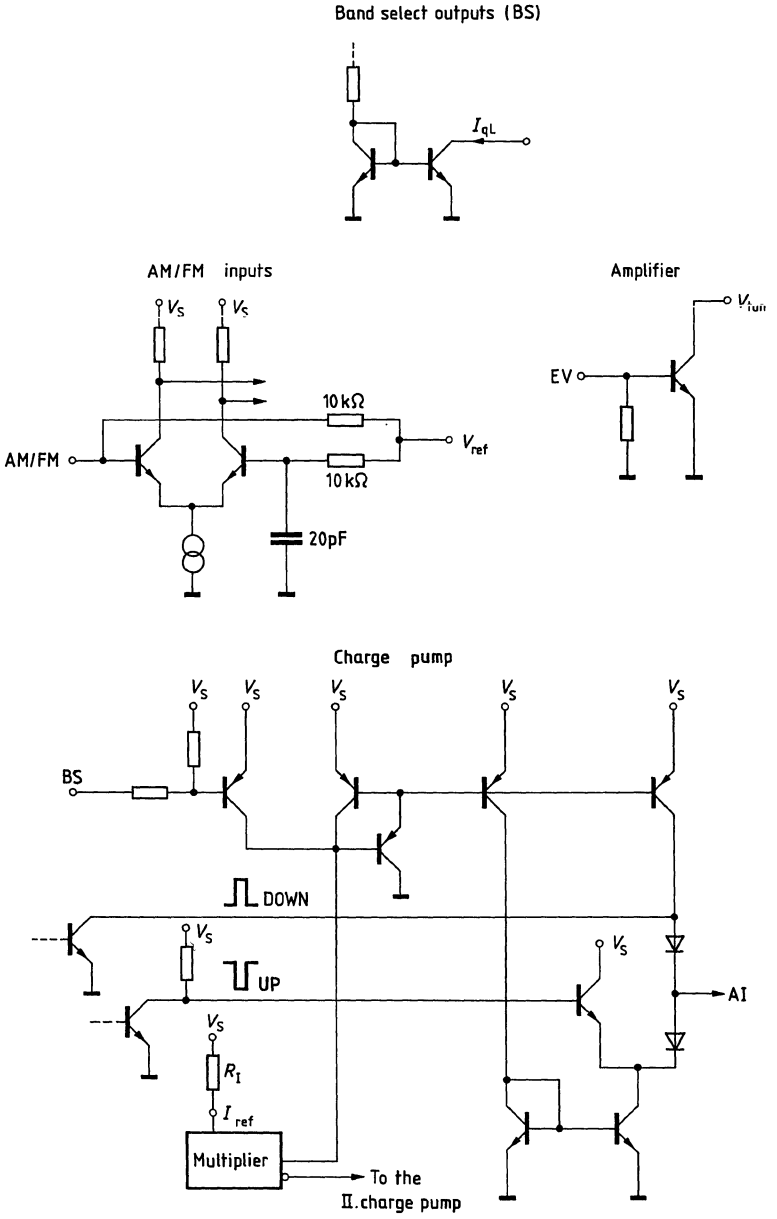
Pin configuration

Pin No.	Symbol	Function
1	EV AM	Amplifier input AM
2		N.C.
3	AI AM	Charge pump output AM
4	FM	Signal input VHF
5	AM	Signal input SW/MW/LW
6	V_S	Supply voltage
7	Q2	Crystal
8	Q1	Crystal
9	UKW	Band select output VHF
10	LW	Band select output LW
11	F	Oscillator output
12	MW	Band select output MW
13	SW	Band select output SW
14	IFO	Data input
15	CPL	Shift register input
16	PLE	Enable input for shift register
17	GND	Ground
18	I_{ref}	Current adjustment for charge pump
19	$V_{tun\,FM}$	Tuning voltage FM
10	EV FM	Amplifier input FM
21	AI FM	Charge pump output FM
22	$V_{tun\,AM}$	Tuning voltage AM

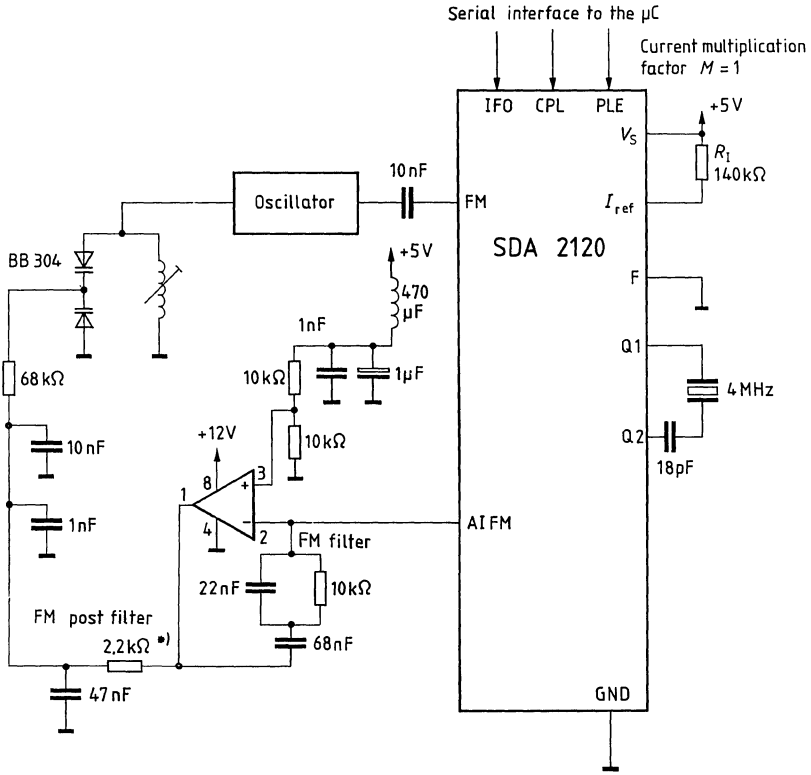
Block diagram



Circuitry of inputs and outputs (schematic)

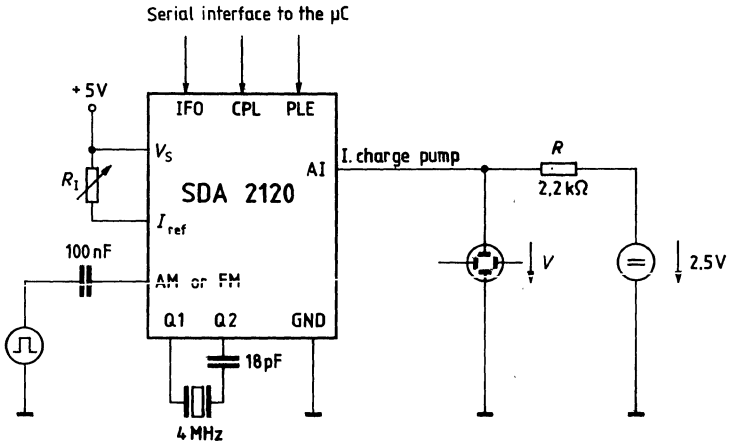


Test circuit for residual ripple of the FM tuning voltage



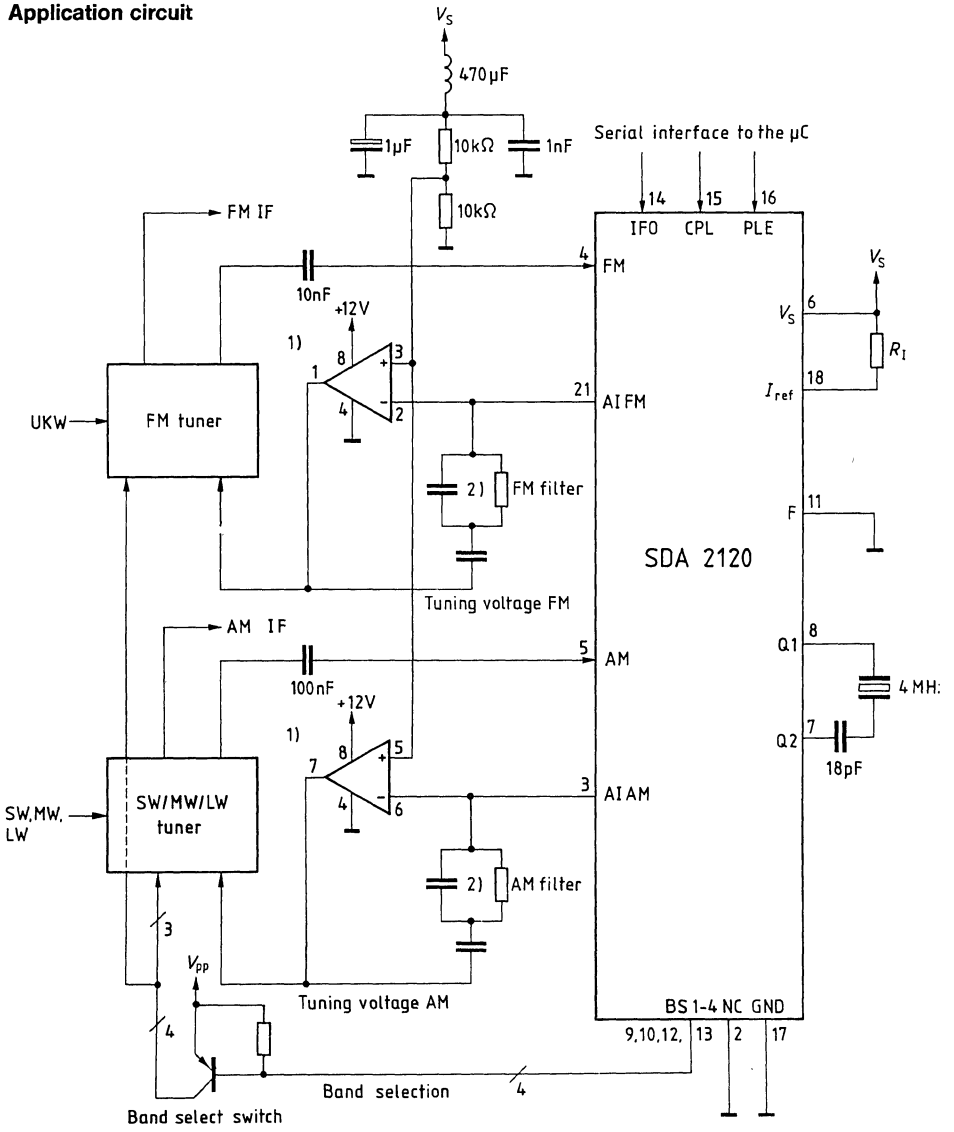
*) The mentioned filter constants are only approximate values.
They have to be matched to the actual tuner by the user.

Test circuit for charge pump output current



To activate the "charge pump", there must be a difference between the frequency of the AM/FM inputs and the frequency of the µC.

Application circuit



1) Double FET operating amplifier: MC 34002, CA 3240, TL 082, LF 353 or similar types.
2) The filter values must be matched to the actual tuner by the user.

DIP 22

The SDA 2131 includes a static display driver for 16 LEDs featuring a 10 mA output current, each. The serial data interface enables a simple connection to the microcomputer.

Features

- Integrated load resistances, thus few external components are required
- Number of LEDs software-selectable
- Blanking capability through DC-controlled input
- Simple connection to a microcomputer

Maximum ratings

Supply voltage range	V_{S7}	−0.3 to 7	V
Input voltage range	$V_{I4,5,6}$	−0.3 to 7	V
Output voltage range (outputs blocked) (pins 1 to 3, 9 to 16, 18 to 22)	V_{qH}	−0.3 to 7	V
Input voltage C range	V_{C8}	−0.3 to V_S	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	R_{thSA}	65	K/W

The anode voltage of the LEDs and the number of simultaneously active outputs should be selected so that a total power dissipation of 800 mW in the IC is not exceeded.

Operating range

Supply voltage range	V_{S7}	4.5 to 5.5	V
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics ($V_S = 5$ V; $T_{amb} = 25$ °C)

		min	typ	max	
Supply current (all LEDs ON) ($I_q = 10$ mA)	I_{S7}		10	15	mA
Quiescent current ($I_q = 0$; C = "L")	I_{S7}		2.5	3.5	mA
Switching voltage	$V_{S4,5,6}$	0.8	1.4	2.0	V
H input current ($V_H = 5.5$ V)	$I_{H4,5,6}$			1	µA
L input current ($V_L = 0.4$ V)	$-I_{L4,5,6}$			10	µA
Output current ($V_q = 2.9$ V) (pins 1 to 3, 9 to 16, 18 to 22)	I_q	8	10	12.5	mA
Output leakage current ($V_q = V_S$) (pins 1 to 3, 9 to 16, 18 to 22)	I_{ql}			10	µA
Switching voltage C	V_{S8}	1.5	2.1	2.7	V
H input current C ($V_{H8} = 5$ V)	I_{H8}		0.6	0.9	mA
L input current C ($V_{L8} = 0$ V)	$-I_{L8}$			1	µA
H input current C (at switching voltage)	I_{H8}			15	µA

Switching times

CLK (pin 5)	H pulse width	t_{HCLK}	1			µs
	L pulse width	t_{LCLK}	2			µs
	Set-up time	t_{SCLK}	0			µs
	Hold time	t_{hCLK}	0			µs
D (pin 4)	Set-up time	t_{SD}	0.5			µs
	Hold time	t_{hD}	0.5			µs
E (Pin 6)	H pulse width	t_{HE}	50			µs
	L pulse width	t_{LE}	0.5			µs
	Set-up time	t_{SE}	1.5			µs
	Hold time	t_{hE}	1			µs
A	delay time	t_A	10			µs

Circuit description

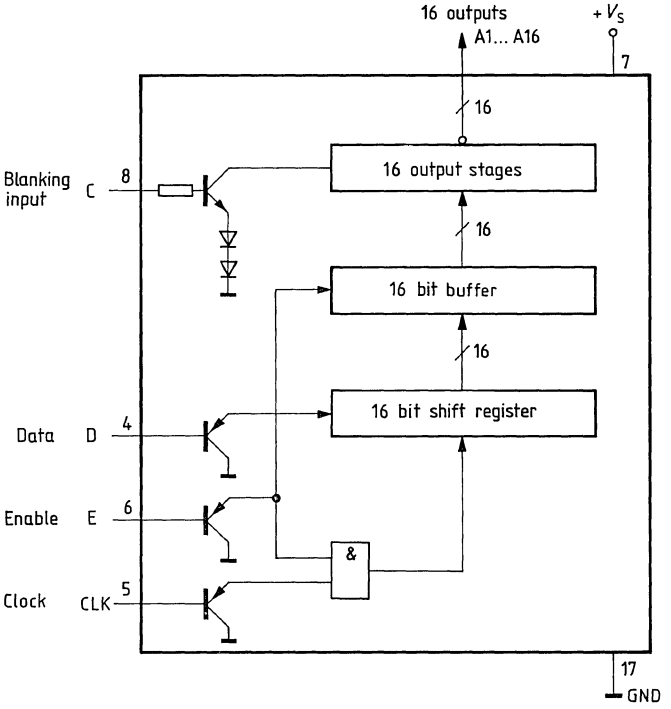
A serial interface consisting of data input D, enable input E, and clock input CLK, to connect the IC to a microprocessor. The 16 bit information ("H" at input D corresponds to the current flow at outputs A1 to A16) is loaded into a 16 bit shift register via the serial data input, beginning with LSB. Data transfer is initiated by the HL slope of the clock pulse at CLK. The data transfer D can take place only during the H state of the enable input E. A buffer accepts the data from the shift register during the HL slope of the enable input. The buffer directly drives the outputs A1 to A16.

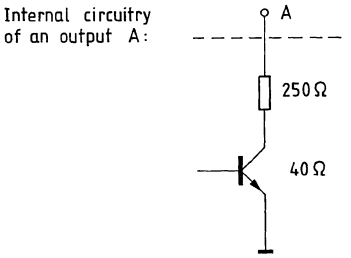
The output is limited by an internal resistor of 290 Ω.

Through input C the outputs can be switched off ($V_{C8} = 0$ V).

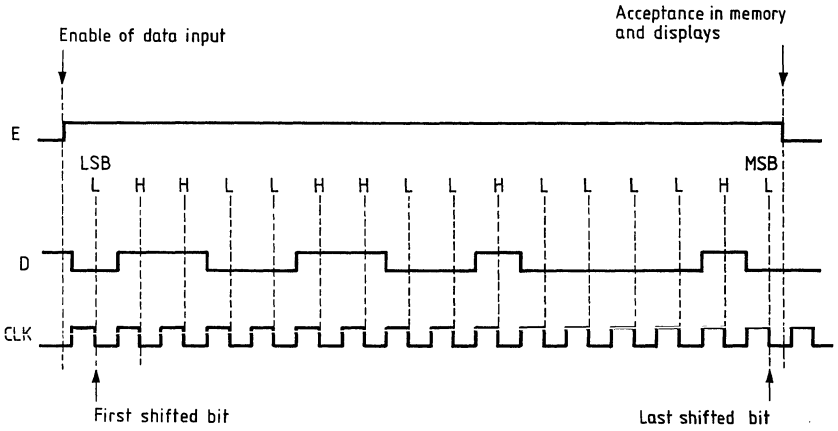
The inputs D, E, and CLK, and the input C are TTL-compatible.

Block diagram





Pulse diagram

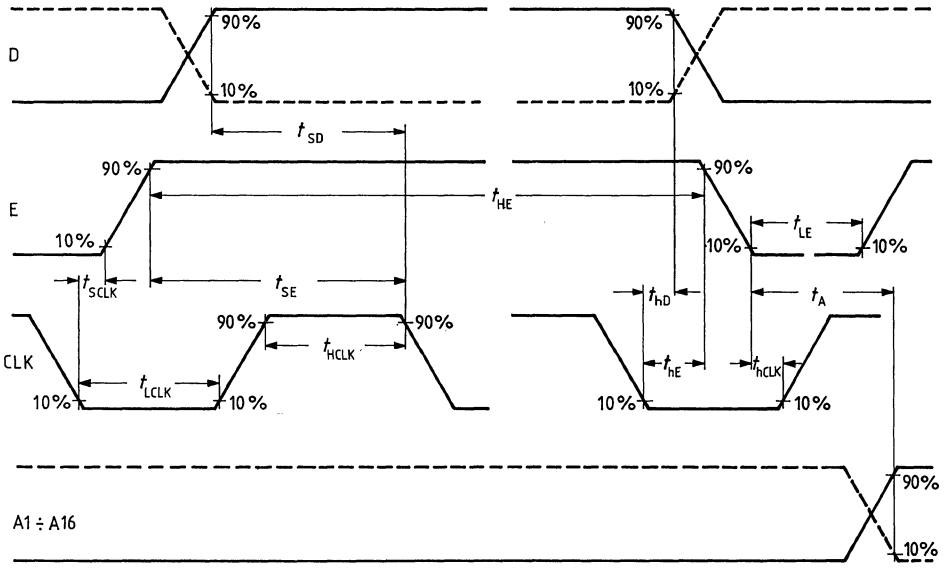


Memory contents after the falling edge of E

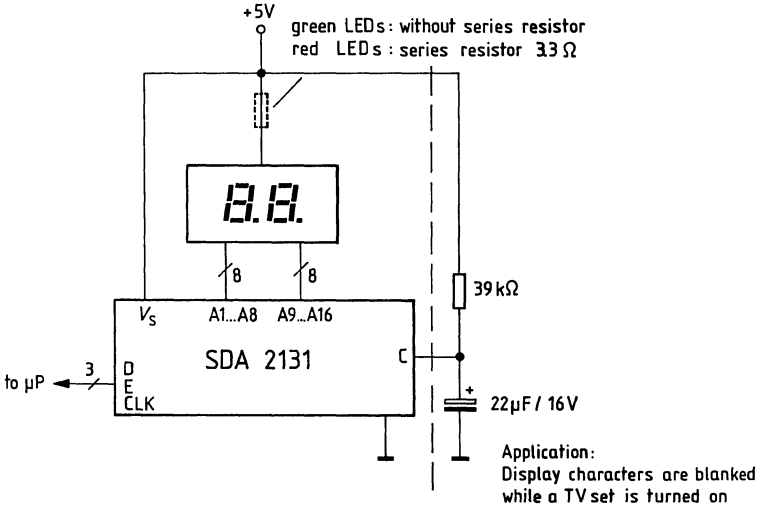
LSB MSB
L H H L L H H L L H L L L L H L

The first information shifted to D with CLK is displayed at A1.

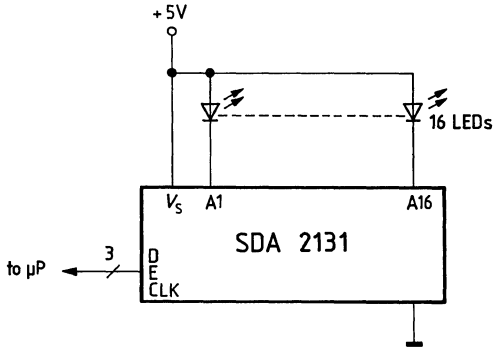
Pulse diagram



Application circuit 1
2 digit 7-segment display



Application circuit 2
Point display (1 of 16 diodes illuminated)



Pin configuration

Pin No.	Symbol	Function
1	A14	Output 14 for LED cathode
2	A15	Output 15 for LED cathode
3	A16	Output 16 for LED cathode
4	D	Input for data
5	CLK	Input for clock
6	E	Input for enable
7	V_S	Supply voltage
8	C	Input for blanking
9	A1	Output 1 for LED cathode
10	A2	Output 2 for LED cathode
11	A3	Output 3 for LED cathode
12	A4	Output 4 for LED cathode
13	A5	Output 5 for LED cathode
14	A6	Output 6 for LED cathode
15	A7	Output 7 for LED cathode
16	A8	Output 8 for LED cathode
17	GND	Ground
18	A9	Output 9 for LED cathode
19	A10	Output 10 for LED cathode
20	A11	Output 11 for LED cathode
21	A12	Output 12 for LED cathode
22	A13	Output 13 for LED cathode

DIP 20

The SDA 2208 is designed as a remote control transmitter for direct driving of infrared transmitter diodes. The instructions are generated by an input matrix (i.e. keyboard) in the form of biphase codes. Distributed over 8 levels, there are a max. of 512 instructions available.

Maximum ratings

Supply voltage range	V_S	−0.3 to 10.5	V
Matrix rows	V_{row}	−0.3 to U_S	V
Matrix columns	V_{col}	−0.3 to U_S	V
Programming pin (PPIN)	V_{PP}	−0.3 to U_S	V
Oscillator input (CLKI)	$V_{i\,OSC}$	−0.3 to 2	V
Infrared output (IRA)			
inhibited	V_q	−0.3 to 10.5	V
in operation	V_q	−0.3 to 8	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	60	K/W

Operating range

Supply voltage	V_S	4 to 10	V
Ambient temperature	T_A	0 to 70	°C
Oscillator frequency	f_{CLK}	430 to 530	kHz

Characteristics

$V_S = 7$ V; $T_A = 25$ °C

		min	typ	max	
Current consumption*)					
transmitting phase	I_S		19		mA
standby mode	I_S		< 1	10	µA
Output current IRA $2\,V < V_2 < 6\,V$	I_2	500	900	1000	mA
Connecting resistance (row-column or column-PPIN)	$R_{row\,col}$			500	Ω

*) Arithmetic mean value incl. transmitter diode

Pin description

Pin	Function
1	GND
2	Output IRA
3	Supply voltage V_S
4	R2
5	R7
6	R1
7	R6
8	R8
9	R4
10	R3
11	R5
12	PPIN
13	CH
14	CE
15	CB
16	CC
17	CG
18	CD
19	CF
20	Oscillator input CLKI

Description of functions

Voltage supply

Voltage consumption ceases in the quiescent state and is activated subsequent to connecting the component's matrix. When the matrix is disconnected, the IC automatically completes the message and returns into the quiescent state.

Clock input

The clock input is equipped with a ceramic resonator. This resonator oscillates with its parallel resonace. In addition, the clock signal can be injected at pin CLK I. The oscillator can be also operated by using an LC circuit with an isolating capacitor.

Input matrix

The matrix is comprised of 8 rows and 8 columns. Column A is used as supply voltage V_S. In order to transmit a message, the respective rows and columns have to be connected. The sender is switched on and a message is output. The length of the message depends on the duration of the matrix connection. A message is comprised of a start instruction, a variable number of information instructions (depending on the duration of the matrix connection) and an end instruction.

Programming via PPIN

The programming pin is used to provide access to all instruction sets or 512 instructions since the 8x8 matrix limits the use to one instruction set or 64 different instructions. By subdividing the instruction sets into 8 levels of 64 instructions each, a specific level can be selected by either keeping the PPIN open or by combining it with one of the seven column inputs (SPB to SPH). When connecting PPIN with one column alone, the standby supply current I_S does not increase.

Safety features against incorrect operation

As a prerequisite for an error-free message output with at least one information instruction, the matrix connection has to be free of interferences and its clock-frequency-dependent, minimal duration should be approx. 60 ms at a clock frequency of 500 kHz. The applied integrated circuit is equipped with a preventive mechanism (key bouncing) against erroneous outputs, which automatically resets the circuit during each detected interference. Equally, operating errors caused by connecting more than one row and one column are detected. The message will be ended through continuous transmitting of end instructions. Operating errors can be cancelled only by disconnecting all matrix connections. The level selection key (PPIN function) will be effective only if it is pressed prior to or simultaneously with the matrix key. Also, a simultaneous pressing of several selection keys has the same effect on the message as an erroneous matrix operation. The protective mechanism becomes effective at $V_S \geq 6\,V$.

Composition of a message

Subsequent to switch-on, the instruction No. 511 (10-bit word length with start bit) is output as start instruction to indicate to the receiver the onset of transmission. Depending on the duration of the matrix connection, a series of identical instructions will follow. If a message is ended by disconnecting the matrix connection, not more than one additional information instruction will be issued to be followed immediately by the end instruction. This end instruction is identical with the start instruction.

Instruction structure

Each instruction consists of a presignal, an infrared pause, a start bit and 9 information bits. During the duration of the presignal (256/fCLK), the receiver performs a simple amplitude adjustment of the input amplifier.

The infrared pause appears between the end of the presignal and the onset of the start bit. Again, the receiver is provided with enough time to recognize transmission distortions based on the limits of the transmission range.

The start bit has been permanently programmed as :1: and is used as synchronization support for the receiver.

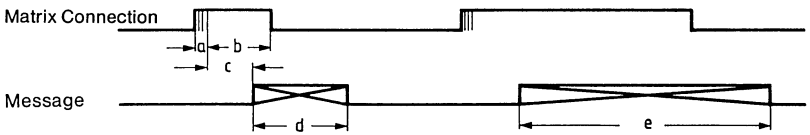
The bit structure has been illustrated in the pulse diagram.

Output driver stage

The fully integrated driver stage enables the direct connection of the infrared transmitter diodes to the infrared output IRA. The diode current is maintained at a constant level within a defined range to stabilize the transmitting power of the infrared diodes.

Pulse diagrams

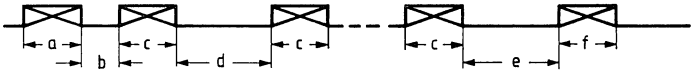
Basic operating process



for 500 kHz
b = 60.928 ms
c = 26.624 ms
d = 177.664 ms

a) bounce
b) minimum key operating time to complete message with one information instruction
c) delay between the on-set of interference-free matrix connection and begin of message transmission
d) message with one information instruction
e) message with several identical information instruction

Composition of message



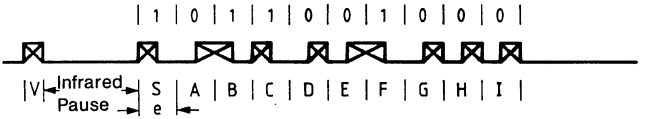
for 500 kHz
a = c = f = 13.312 ms
b = 19.968 ms
d = e = 177.76 ms

a) start instruction 10 bits
b) time interval between start and information instruction
c) information instruction 10 bits
d) time interval between identical information instruction
e) time interval between information and end instruction
f) end instruction 10 bits

The timespan of an interference-free matrix connection determines the number of identical information instructions.

Pulse diagrams

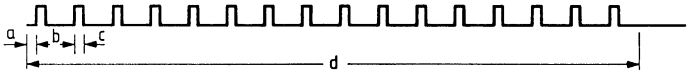
Instruction structure in biphase code



Time duration single bit e: $512/f_{CLK}$
presignal V: $256/f_{CLK}$
infrared pause: $5x256/f_{CLK}$

start bit S is always 1
bits A to I are addressable

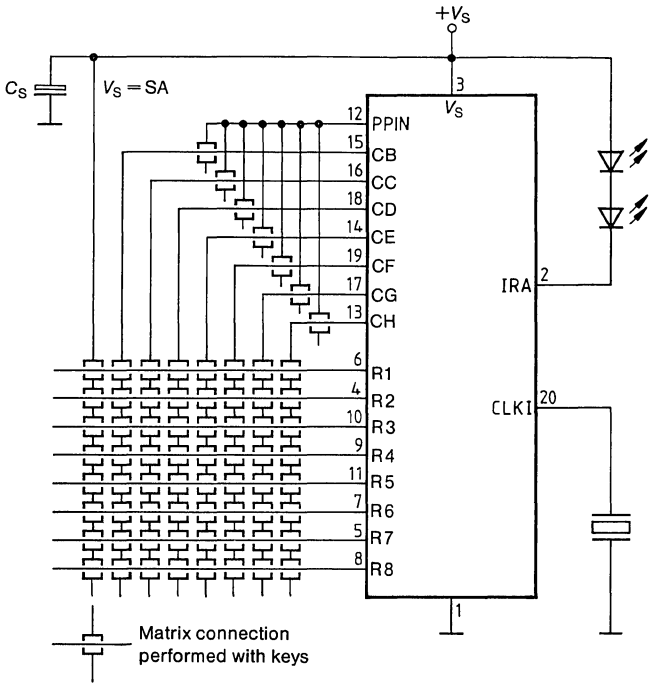
Structure of the modulated half bit (as well as the presignal)



$a = c = 4/f_{CLK}$
$b = 16/f_{CLK}$
$d = 256/f_{CLK}$
16 pulses per half bit

The H signal indicates a constant current source at Q_{IRA}. The infrared transmitter diode is then active.

Block diagram



Since the infrared transmitter diodes have to be driven with pulse currents of approx. 1 A, the following has to be complied with during the layout of the PC board:

1) The smoothing capacitor between V_S and ground should be located as closely as possible to the pins of the IC.
2) The supply line to the transmitter diodes is not to cause cross-talk in the key matrix.
3) No residual currents are to flow over the connection ceramic oscillator/ground pin.

Truth table

No. of the instruction	Matrix connection row–column	Binary code IRA information instruction A B C D E F G H I
0	1A	0 0 0 0 0 0 0 0 0
1	1B	1 0 0 0 0 0 0 0 0
2	1C	0 1 0 0 0 0 0 0 0
3	1D	1 1 0 0 0 0 0 0 0
4	1E	0 0 1 0 0 0 0 0 0
5	1F	1 0 1 0 0 0 0 0 0
6	1G	0 1 1 0 0 0 0 0 0
7	1H	1 1 1 0 0 0 0 0 0
8	2A	0 0 0 1 0 0 0 0 0
9	2B	1 0 0 1 0 0 0 0 0
10	2C	0 1 0 1 0 0 0 0 0
11	2D	1 1 0 1 0 0 0 0 0
12	2E	0 0 1 1 0 0 0 0 0
13	2F	1 0 1 1 0 0 0 0 0
14	2G	0 1 1 1 0 0 0 0 0
15	2H	1 1 1 1 0 0 0 0 0
16	3A	0 0 0 0 1 0 0 0 0
17	3B	1 0 0 0 1 0 0 0 0
18	3C	0 1 0 0 1 0 0 0 0
19	3D	1 1 0 0 1 0 0 0 0
20	3E	0 0 1 0 1 0 0 0 0
21	3F	1 0 1 0 1 0 0 0 0
22	3G	0 1 1 0 1 0 0 0 0
23	3H	1 1 1 0 1 0 0 0 0
24	4A	0 0 0 1 1 0 0 0 0
25	4B	1 0 0 1 1 0 0 0 0
26	4C	0 1 0 1 1 0 0 0 0
27	4D	1 1 0 1 1 0 0 0 0
28	4E	0 0 1 1 1 0 0 0 0
29	4F	1 0 1 1 1 0 0 0 0
30	4G	0 1 1 1 1 0 0 0 0
31	4H	1 1 1 1 1 0 0 0 0
32	5A	0 0 0 0 0 1 0 0 0
33	5B	1 0 0 0 0 1 0 0 0
34	5C	0 1 0 0 0 1 0 0 0
35	5D	1 1 0 0 0 1 0 0 0
36	5E	0 0 1 0 0 1 0 0 0
37	5F	1 0 1 0 0 1 0 0 0
38	5G	0 1 1 0 0 1 0 0 0
39	5H	1 1 1 0 0 1 0 0 0
40	6A	0 0 0 1 0 1 0 0 0

Truth table (cont'd)

No. of the instruction	Matrix connection row – column	Binary code IRA information instruction A B C D E F G H I
41	6B	1 0 0 1 0 1 0 0 0
42	6C	0 1 0 1 0 1 0 0 0
43	6D	1 1 0 1 0 1 0 0 0
44	6E	0 0 1 1 0 1 0 0 0
45	6F	1 0 1 1 0 1 0 0 0
46	6G	0 1 1 1 0 1 0 0 0
47	6H	1 1 1 1 0 1 0 0 0
48	7A	0 0 0 0 1 1 0 0 0
49	7B	1 0 0 0 1 1 0 0 0
50	7C	0 1 0 0 1 1 0 0 0
51	7D	1 1 0 0 1 1 0 0 0
52	7E	0 0 1 0 1 1 0 0 0
53	7F	1 0 1 0 1 1 0 0 0
54	7G	0 1 1 0 1 1 0 0 0
55	7H	1 1 1 0 1 1 0 0 0
56	8A	0 0 0 1 1 1 0 0 0
57	8B	1 0 0 1 1 1 0 0 0
58	8C	0 1 0 1 1 1 0 0 0
59	8D	1 1 0 1 1 1 0 0 0
60	8E	0 0 1 1 1 1 0 0 0
61	8F	1 0 1 1 1 1 0 0 0
62	8G	0 1 1 1 1 1 0 0 0
63	8H	1 1 1 1 1 1 0 0 0

	G H I
Instruction 0 to 63: PPIN free	0 0 0
Instruction 64 to 127: PPIN connected with CB	1 0 0
Instruction 128 to 191: PPIN connected with CC	0 1 0
Instruction 192 to 255: PPIN connected with CD	1 1 0
Instruction 256 to 319: PPIN connected with CE	0 0 1
Instruction 320 to 383: PPIN connected with CF	1 0 1
Instruction 384 to 447: PPIN connected with CG	0 1 1
Instruction 448 to 511: PPIN connected with CH	1 1 1

In every instruction set, the assignment instruction – matrix connection (row – column) is analogous to the group 0 to 63.

Example:

Instruction 64 is generated, when PPIN is connected with CB, and R1 with CA.

Pre-scaler 1:64 for 1.3 GHz with low current consumption SDA 2211

Preliminary data

DIP 8

The IC has been designed for application in TV receivers using the frequency control of the frequency synthesis rough copy concept. It includes a pre-amplifier and an ECL pre-scaler with a 1:64 scaling rate and symmetrical ECL push-pull outputs. The operating range of the IC extends to an input frequency of 1.3 GHz.

- Minimal current consumption
- High input sensitivity

Maximum ratings

Supply voltage	V_S	−0.3 to 6	V
Input voltage	$V_{I2,3}$	2.5	V_{PP}
Output voltage	$V_{Q6,7}$	V_S	V
Output current	$-I_{Q6,7}$	10	mA
Junction temperature	T_j	125	°C
Storage temperature range	T_{stg}	40 to 125	°C
Thermal resistance:			
System-air	R_{thSA}	115	K/W

Range of operation

Supply voltage	V_S	4.5 to 5.5	V
Input frequency	f	70 to 1300	MHz
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics (V_S = 4.5 - 5.5 V; T_{amb} = 0 - 70°C)

		min	typ	max	
Current consumption inputs blocked, outputs free	I_S		23	29	mA
Output voltage shift (at each output)	V_q				
$C_L \leq 15$ pF		0.5	1	1.2	dBm
$C_L = 60$ pF		0.35			dBm
Input level ("Input sensitivity")	V_I				
70 MHz		-26		3	dBm
80 MHz		-27		3	dBm
120 MHz		-30		3	dBm
250 MHz		-32		3	dBm
600 MHz		-27		3	dBm
1000 MHz		-27		3	dBm
1100 MHz		-27		3	dBm
1200 MHz		-21		3	dBm
1300 Mhz		-15		3	dBm

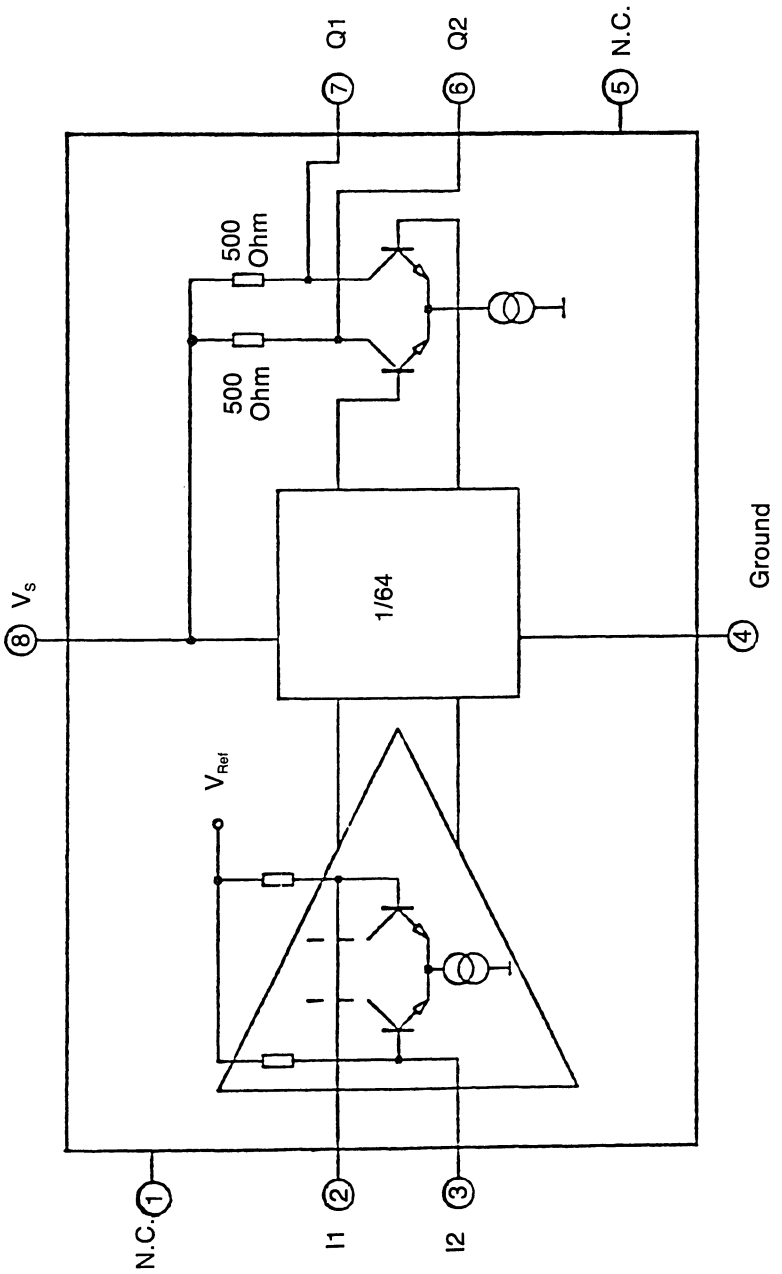
Circuit description

The pre-amplifier of the IC features symmetrical push-pull outputs. If one of the signal inputs is in an asymmetrical driving mode the other input should be grounded by a capacitor (≈1.5 nF) with low series inductivity. The pre-scaler of the IC consists of several status controlled master slave flip flops with a 1:64 scaling rate.
The asymmetrical push-pull outputs of the pre-scaler have been designed with an internal resistance of 500Ω each. The DC voltage level of the outputs is connected to the supply voltage V_S (output "high" = V_S). The typical shift is 1 V_{PP}.

Pin configuration

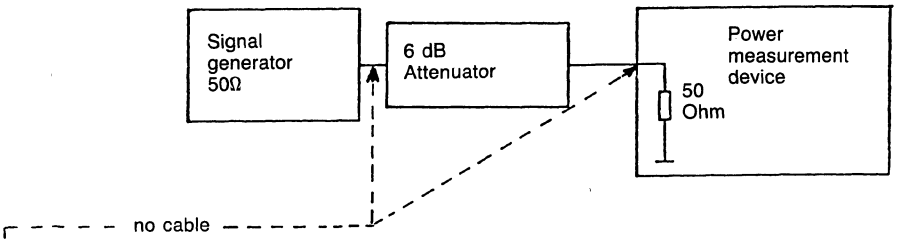
Pin-No.	Function
1	N.C.
2	Input I1
3	Input I2
4	Ground
5	N.C.
6	Output Q2
7	Output Q1
8	Supply voltage V_S

Block diagram

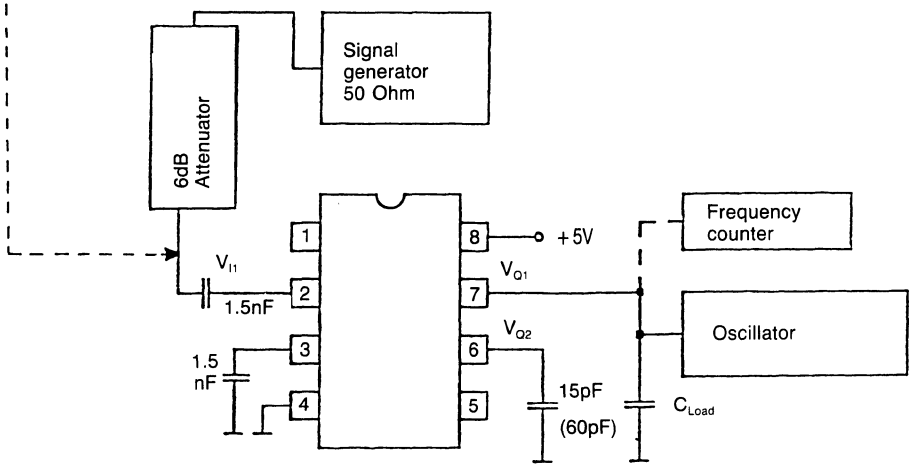


Test and measurement circuits

Signal generator calibration



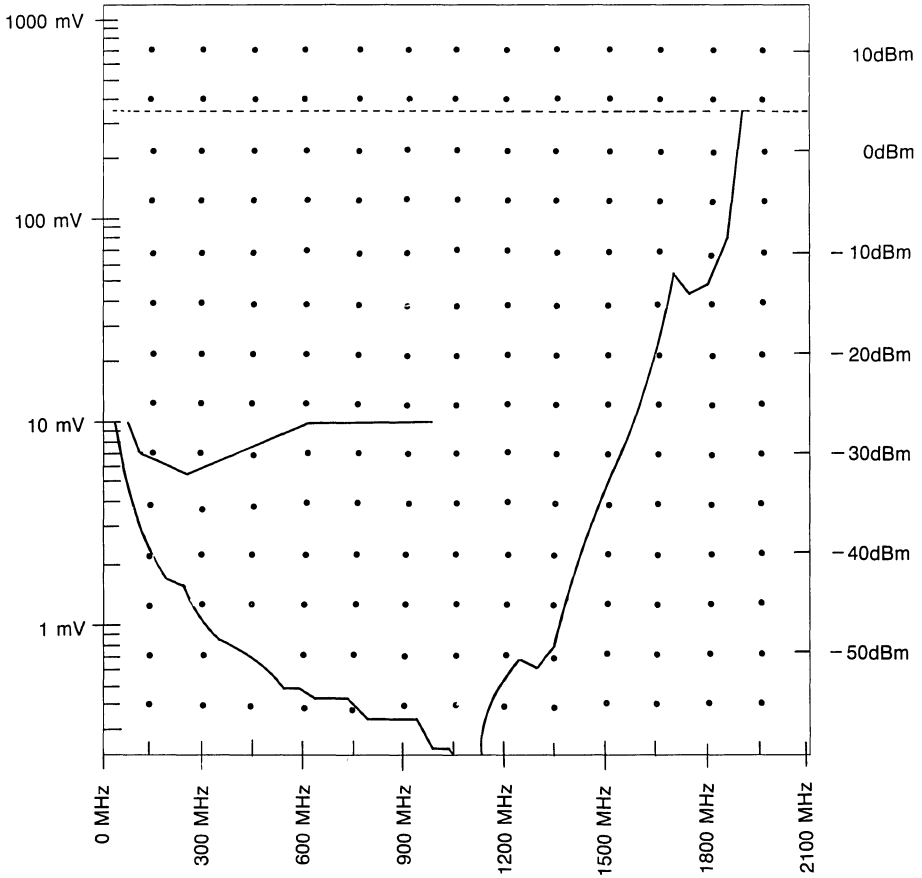
Measurement configuration for input sensitivity and the output voltage swing



Test circuit 1

Capacitive load definition for output voltage swing measurement:
C_{Load} + capacities of the measurement devices = 15 pF (60 pF)

Typical input sensitivity of pre-scaler
$V_S = 5$ V; $T_{amb} = 25$°C



Preliminary data DIP 8

Features

- Word-organized programmable nonvolatile memory in n-channel floating-gate technology
- 128 x 8 bit organization
- Supply voltage 5 V
- A total of three lines between control processor and the E²PROM for data transfer and chip control
- Data (8 bits), address (7 bits), and control information input (1 bit) as well as serial data output
- More than 10^4 reprogramming cycles per address
- Data retention in excess of 10 years (operating temperature range)
- Unlimited number of reads without refresh
- Erase and write in 10 ms

Maximum ratings

Supply voltage range	V_{DD}	−0.3 to 6	V
Input voltage range	V_i	−0.3 to 6	V
Power dissipation	P_V	40	mW
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	R_{thSA}	100	K/W

Operating range

Supply voltage	V_{DD}	4.75 to 5.25	V
Ambient temperature	T_A	0 to 70	°C

Static characteristics

		min	typ	max	
Supply voltage	V_{DD}	4.75	5	5.25	V
Supply current	I_{DD}			3	mA
Inputs	V_L			0.8	V
D, Φ, $\overline{CE}$	V_H	2.4			V
$V_H = 5.25$ V	I_H			10	µA
Data output D (open drain)					
$V_L = 0.8$ V	I_L			0.5	mA
$V_H = 5.25$ V	I_H			10	µA
Clock puise Φ					
High duration	Φ_H	2.5		60	µs
Low duration					
before/after Φ_H	Φ_L	5			µs
before/after $\overline{CE}$ transition	Φ_L	5			µs
before/after D change	Φ_L	2.5			µs
Data D					
before/after Φ trailing edge	D_H	2.5			µs
	D_L	2.5			µs
Time between rising and trailing edge					
$\overline{CE}$ referenced to D	Δt	2.5			µs
Erase time	t_{er}	10		20	ms
Write time	t_{wr}	10		20	ms

Data transfer and chip control

The total data transfer between the control processor and the E²PROM requires three lines, each of which has several functions:

a) Data line D
- bidirectional serial data transfer
- serial address input
- clocked input of control information
- direct control input

b) Clock line Φ
- data, address, and control bit input
- data output
- start of readout with transfer of data from memory into shift register and/or start of data change during reprogramming

c) Chip enable line $\overline{CE}$
- chip reset and data input (active high)
- chip enable (active low)

Prior to chip enable, the data, address, and control information is clocked via the bidirectional data bus. During the reprogramming and read process, this data is retained in the shift register up to the second clock pulse. The following data formats must be entered:

a) **Read memory:** one 8-bit control word comprising:
   — 7 address bits A0 to A6 (A0 goes first as LSB)
   — 1 control bit, SB = "0", after A6

b) **Reprogram memory:** (erase and/or write operation)
   16-bit input information comprising:
   — 8 bits, D0 to D7 new memory information (D0 goes first as LSB)
   — 7 bits, A0 to A6 address information (A0 as LSB goes first after D7)
   — 1 bit, control information, SB = "1", after A6

Read (figure 1)

Subsequent to data input and with SB = "0", the read process of the selected word address is started when $\overline{CE}$ changes from "1" to "0". The information on the data line is not effective during chip enable.

With the first clock pulse after $\overline{CE}$ = "0", the data word of the selected memory address is transferred into the shift register. After the first Φ pulse has ended, the data output becomes low in impedance and the first data bit can be read at the data pin. During each additional clock pulse, a data bit is shifted to the output. The data line returns to high-impedance mode when $\overline{CE}$ transitions from "0" to "1".

Reprogramming (figure 2)

A full reprogramming process comprises an erase and a subsequent write process. During the erase process, all bits of the selected word are set to the "1" state. During a write process, the "0" states are set according to the information in the shift register.

The reprogramming process is started after data input during chip enable when the information SB = "1" is available in the relevant cell of the shift register. The selection of an erase or write process depends on the information on data line D during chip enable.

An erase process in the "1" state requires a "1" at the data input when $\overline{CE}$ transitions to low. Similarly, a write process in the "0" state requires that a "0" be present on the data line during chip enable.

To start the programming process, a start pulse must be present at clock input Φ. The control information on D must remain stable up to the rising edge of the start pulse. The active data change begins with the trailing edge of the start pulse. The programming process is ended by terminating chip enable, that is, when $\overline{CE}$ = "1".

The reprogramming of a word begins during the start and execution of the erase process. The erase process is ended when $\overline{CE}$ = "1". The control bit SB = "1" also required for the write process remains stable in the shift register after the erase process is terminated. The writing of the selected word, therefore, requires nothing more than changing data line D from "1" to "0", enabling the chip again with $\overline{CE}$ = "0" and starting the data change with the start pulse.

The erase and write processes can be performed separately. In order to ensure a uniform "1" state for all eight bits of the selected memory address during the erase process, a data word with eight times "1" must be entered prior to the erase process. When writing a word which was not erased previously, the "0" states of old and new information are added up.

Reset

A non-selected memory is automatically in the reset state due to $\overline{CE}$ = "1". All flipflops of the process control are reset. However, the information in the shift register is retained and changed only by shifting the data. The rest state is also set by on-chip circuitry during memory power on.

Pin description

Pin	Symbol	Function
1	V_{SS}	GND
2	$\overline{CE}$	Chip enable
3	V_{DD}	Supply voltage 5 V
4	D	Data input/output
5	Φ	Clock input
6		N.C.
7	TP	Test input, at V_{SS}
8	TG	Test input, remains open

Read cycle (1-Kbit E²PROM)

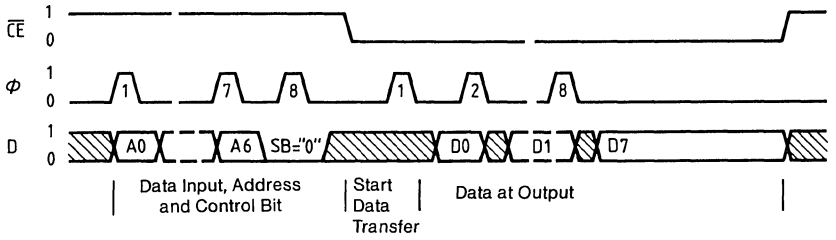


Figure 1

Reprogramming cycle (1-Kbit E²PROM)

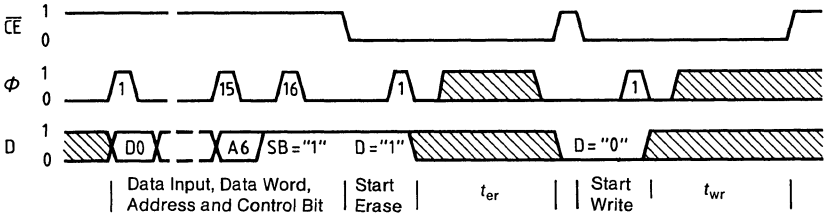


Figure 2

Nonvolatile Memory 1-Kbit E²PROM with I²C Bus Interface

SDA 2516

Preliminary data

DIP 8

Features

- Word-organized programmable nonvolatile memory in n-channel floating-gate technology (E²PROM)
- 128 x 8 bit organization
- Supply voltage 5 V
- Serial 2-line bus for data input and output (I²C bus)
- Reprogramming mode, 15 ms erase/write cycle
- Reprogramming by means of on-chip control (without external control)
- Data retention in excess of 10 years
- More than 10^4 reprogramming cycles per address

Maximum ratings

Supply voltage range	V_{DD}	−0.3 to 6	V
Input voltage range	V_i	−0.3 to 6	V
Power dissipation	P_V	50	mW
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	R_{thSA}	100	K/W

Operating range

Supply voltage	V_{DD}	4.75 to 5.25	V
Ambient temperature	T_A	0 to 70	°C

Characteristics

		min	typ	max	
Supply voltage	V_{DD}	4.75		5.25	V
Supply current	I_{DD}			8	mA
Inputs SCL/SDA					
Low level	V_{IL}			1.5	V
High level	V_{IH}	3.0		V_{DD}	V
High current ($V_{IH} = V_{DD\,max}$)	I_{IH}			10	µA
Output SDA					
Low current ($V_{QL} = 0.4$ V)	I_{QL}			3.0	mA
Leakage current ($V_{QH} = V_{DD\,max}$)	I_{QH}			10	µA
Inputs CS0, CS1, CS2/TP					
	V_{IL}			0.2	V
	V_{IH}	4.5		V_{DD}	V
High current	I_{IH}			100	µA
Clock frequency	f_{SCL}			100	kHz
Reprogramming duration (erasing and writing)	t_{prog}		15	30	ms
Input capacity	C_I			10	pF
Full erase duration (test mode full erase)	t_{er}			50	ms

I²C bus interface (figures 1 and 2)

The I²C bus is a bidirectional 2-line bus for the transfer of data between various integrated circuits. It consists of a serial data line SDA and a serial clock line SCL. Both lines require an external pull-up resistor to V_{DD} (open drain output stages).

The possible operational states of the I²C bus are shown in figure 1. In the quiescent state, both lines SDA and SCL are high, i.e. the output stages are disabled. As long as SCL remains "1", information changes on the data bus indicate the start or the end of a data transfer between two components. The transition on SDA from "1" to "0" is a start condition, the transition from "0" to "1" a stop condition. During a data transfer the information on the data bus will only change while the clock line SCL is "0". The information on SDA is valid as long as SCL is "1".

In conjunction with an I²C bus system, the memory component can operate as a receiver, and as a transmitter (slave receiver/listener, or slave transmitter/talker). Between a start and a stop condition, information is always transmitted in byte-organized form (8 bits). Between the trailing edge of the eighth transmission pulse and a ninth acknowledge clock pulse, the memory component sets the SDA line to low as a confirmation of reception, if the chip select conditions have been met. During the output of data, the data output becomes high in impedance if the master receiver leaves the SDA line high during the acknowledge clock pulse.

The signal timing required for the operation of the I²C bus is summarized in figure 2 (high-speed mode).

Control functions of the I²C bus

The memory component is controlled by the controller (master) via the I²C bus in two operating modes: read-out cycle, and reprogramming cycle, including erase and write to a memory address. In both operating modes, the controller, as transmitter, has to provide 3 bytes and an additional acknowledge clock pulse to the bus after the start condition. A rapid read mode enables the reading of data immediately after the slave address has been input. During a memory read, at least eight additional clock pulses are required to accept the data from the memory, before the stop condition may follow. In the programming case, the active programming process is only started by the stop condition after data input.

With a 3-bit chip select word (CS0, CS1, CS2) it is possible for the user to individually address 8 memory components connected in parallel. Chip select is achieved when the three control bits logically correspond to the selected conditions at the three select inputs CS0, CS1, CS2.

Memory read

After the input of the first two control words and 18 SCL pulses, a resetting of the start condition and the input of a third control word, the memory is set ready to read. During acknowledge clock nine, the memory information is transferred in parallel mode to the internal data register. Subsequent to the trailing edge of the acknowledge clock, the data output is low-ohmic and the first data bit can be sampled. With each shift clock, an additional bit reaches the output. After reading a byte, the internal address counter is automatically incremented through the master receiver acknowledge, so that any number of memory locations can be read one after the other. At address 127, an overflow to address 0 is initiated. With the stop condition, the data output returns to high-impedance mode. The internal sequence control of the memory component is reset from the read to the quiescent state with the stop condition.

Memory reprogramming

The reprogramming cycle of a memory word comprises an erase and a subsequent write process. During erase, all eight bits of the selected word are set into the "1" state. During write, "0" states are generated according to the information in the internal data register, i.e. according to the third input control word.

After the 27th and last clock of the control word input, the active programming process is started by the stop condition. The active reprogramming process is executed under on-chip control and can be terminated by addressing the component via SCL and SDA.

The time required for reprogramming depends on component deviation and data patterns. Therefore, with rated supply voltage the erase/write process extends over max. 30 ms or, more typically, 15 ms. For the input of a data word without write request (write request is defined as data bit in the data register set to "0"), the write process is suppressed and the programming time is shortened. During a subsequent programming of an already erased memory address, the erase process is suppressed again, so that the reprogramming time is also shortened.

Switch-on mode and chip reset

After the supply voltage V_{DD} has been connected, the data output will be in the high impedance mode. As a rule, the first operating mode to be entered should be the read

process of a word address. Subsequent to data output and the stop condition, the internal control logic is reset. However, in case of a subsequent active programming operation, the stop condition will not reset the control logic.

Test mode – total erase

The address register is loaded with address 0, the data register with FF (hex) by entering the control word "programming". However, immediately prior to generating the stop condition, input CS2/TP is connected from 0 V to 12 V. The subsequent stop condition triggers a total erase procedure which has to be performed under the component address 0 (CS0 = L, CS1 = L, CS2 = L).

Pin description

Pin	Symbol	Function
1	V_{SS}	GND
2	CS0	Chip select inputs / Test operation control
3	CS1	
4	CS2/TP	
5	SDA	Data line (I²C bus)
6	SCL	Clock line (I²C bus)
7		N.C.
8	V_{DD}	Supply voltage

Operational states of the I²C bus

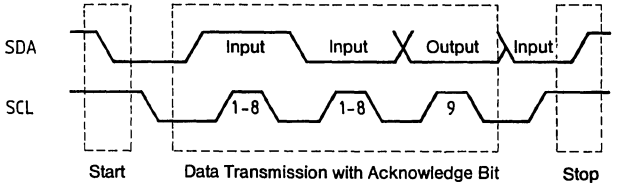


Figure 1

Timing conditions for the I²C bus (high-speed mode)

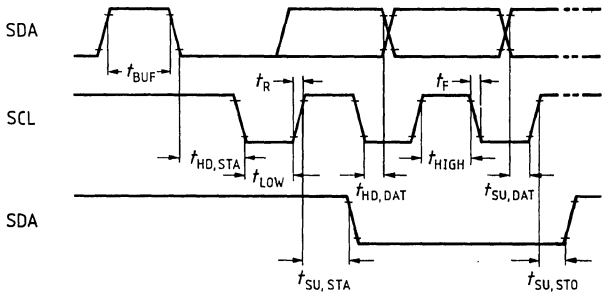


Figure 2

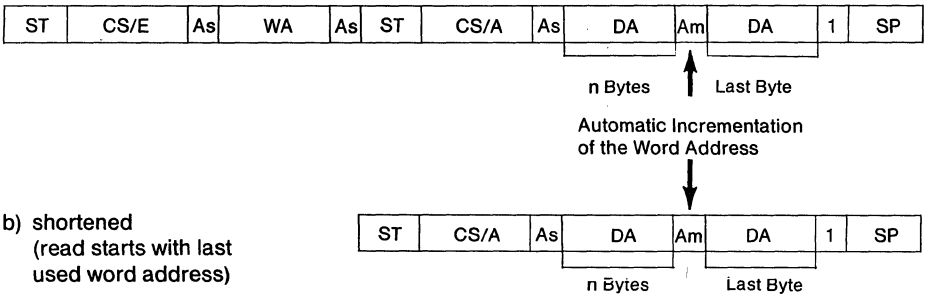
t_{BUF}	$t > t_{LOW\,min}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t > t_{HIGH\,min}$	Start condition hold time
$t_{LOW\,min}$	4.7 µs	Clock LOW period
$t_{HIGH\,min}$	4 µs	Clock HIGH period
$t_{SU;STA}$	$t > t_{LOW\,min}$	Start condition set-up time, only valid for reported start code
$t_{HD;DAT}$	$t > 0$ µs	Data hold time
$t_{SU;DAT}$	$t > 250$ ns	Data set-up time
t_R	$t < 1$ µs	Rise time of both the SDA and SCL line
t_F	$t < 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t > t_{LOW\,min}$	Stop condition set-up time

Note:

All values refer to V_{IH} and V_{IL} levels.

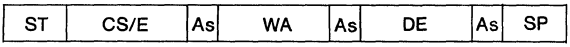
Control word input read

a) complete (with word address input)



b) shortened
(read starts with last
used word address)

Control word input program



(reprogramming starts
after this stop condition)

Control word table

Clock No.	1	2	3	4	5	6	7	8	9	(Acknowledge)
CS/E	1	0	1	0	CS2	CS1	CS0	0	0	through memory
CS/A	1	0	1	0	CS2	CS1	CS0	1	0	through memory
WA	X	A6	A5	A4	A3	A2	A1	A0	0	through memory
DE	D7	D6	D5	D4	D3	D2	D1	D0	0	through memory
DA	D7	D6	D5	D4	D3	D2	D1	D0	0	through master

Control word input key:

CS/E	Chip select for data input into memory
CS/A	Chip select for data output out of memory
WA	Memory word address
DE	Data word for memory
DA	Data word read out of memory
D0 to D7	Data bits
ST	Start condition
SP	Stop condition
As	Acknowledge bit from memory
Am	Acknowledge bit from master
CS0, CS1, CS2	Chip select bits
A0 to A6	Memory word address bits

Figure 3

Nonvolatile Memory 2 Kbit
E^2Prom with I^2C Bus Interface

SDA 2526

Preliminary Data

DIP 8

General characteristics

- Word-organized reprogrammable nonvolatile memory in n-channel-floating-gate technology (E^2PROM)
- 256 x 8 bit organization
- Supply voltage 5 V
- Serial 2-line data bus for data input and output (I^2C bus)
- Reprogramming mode, 15 ms erase/write cycle
- Reprogramming by means of chip-internal control without external control
- Data retention in excess of 10 years
- More than 10^4 reprogramming cycles per address

Maximum ratings*

Supply voltage range	V_{CC}	– 0.3 to 6	V
Input voltage range	V_i	– 0.3 to 6	V
Power dissipation	P_V	50	mW
Storage temperature range	T_{stg}	– 40 to 125	°C
Thermal resistance (System-air)	R_{thSA}	100	K/W

Range of operation

Supply voltage	V_{CC}	4.75 to 5.25	V
Ambient temperature	T_{amb}	0 to 70	V

* not valid for input CS2/TP in Test mode - full deletion

Characteristics

		min	typ	max	
Supply voltage	V_{DD}	4.75		5.25	V
Supply current	I_{DD}			8	mA
Inputs SCL/SDA					
Low level	V_{IL}			1.5	V
High level	V_{IH}	3.0		V_{DD}	V
High current ($V_{IH} = V_{DDmax}$)	I_{IH}			10	μA
Output SDA					
Low current ($V_{QL} = 0.4$ V)	I_{QL}			3.0	mA
Leakage current ($V_{QH} = V_{DDmax}$)	I_{QH}			10	μA
Inputs CSO, CS1, CS2/TP	V_{IL}			0.2	V
	V_{IH}	4.5		V_{DD}	V
High current	I_{IH}			100	μA
Clock frequency	f_{SCL}			100	kHz
Reprogramming duration (erasing and writing)	t_{prog}		15	30	ms
Input capacity	C_I			10	pF
Full deletion duration (test mode full selection)	t_{ED}			50	ms
Condition	$V_{CS"/TP}$	11	12	13	V

Pin Configuration

Pin	Symbol	Function
1	Ground	(Ground)
2	CS0	Chip select input
3	CS1	Chip select input
4	CS2/TP	Chip select/ Test operation control
5	SDA	Data line } I²C bus
6	SCL	Clock line } I²C bus
7		N.C.
8	V_{DD}	Supply voltage

I²C bus interface (fig. 1 and 2)
The I²C bus has been designed as a bidirectional 2-line bus for transferring data between different integrated circuits. Toward this end, the component is comprised of a serial data line SDA and a serial clock line SCL. Both lines require an external pull-up resistor to V_{DD} (open drain output stages).

The different operational stages of the I²C bus are described in fig. 1. In the quiescent condition both output lines SDA and SCL are on the logical potential "1", inhibiting the output stages. As long as SCL remains on "1", changes in the information on the data bus indicate the beginning and/or the end of data transfers between two integrated circuits. During actual data transfers, however, information on the data bus will change only if the clock output SCL lies on "0." With respect to SDA, changes provide either a start condition (from "1" to "0") or a stop condition (from "0" to "1"). The information on SDA continues to be valid as long as SCL remains on "1".

In conjunction with the I²C bus system, it is possible to operate the memory in a dual capacity as receiver and transmitter (slave receiver (listener) or slave transmitter (talker)). Between a start and a stop condition, information is always transmitted in byte-organized form (8 bits each). If the chip select conditions have been met, the memroy places the SDA line on "0" between the trailing edge of the eighth transmission pulse and the ninth acknowledge clock pulse to signal reception confirmation. While data is being transmitted, the data output will change into a high impedance mode, if the master receiver leaves the SDA output on "1" during the acknowledge clock pulse.

The signal process required for the operation of the I²C bus has been summarized in fig. 2 (high-speed-mode).

Control functions of the I²C bus
Via the I²C bus the memory is controlled by the controller (master) during two operating modes: a) read-out cycle and b) the reprogramming cycle, including the erasing and writing of a memory address. In both operating modes the controller functioning as transmitter has to provide 3 bytes and an additional acknowledge clock on the bus after the start condition.

In addition to the standard read-out cycle, a rapid read-out mode has been provided which enables the reading of data immediately after the salve addresses have been entered. In order to read the memory at least 8 additional clock pulses are required prior to the stop condition. With respect to programming, the active programming process will be started by the stop condition if the data has been entered.

With a 3 bit chip select word (CS0, CS1, CS2), which can be coded externally, it is possible for the user to individually address 8 memory components connected in parallel. The chip select requirements have been met, when the chip select bits CS0, CS1, CS2 of the external chip select word logically correspond with the chip select information made available via the I²C bus signal.

Memory read-out

The first two control words are entered during 18 SCL pulses. Subsequently, the memory is adjusted for read-out by resetting the start condition and by entering a third control word. During the ninth acknowledge clock, the information stored in the memory is transferred in parallel mode to the interal data register. Subsequent to the trailing edge of the acknowledge clock, the data output is in the low impedance mode, and the first data bit can be read. With each shift clock an additional data bit is forwarded to the output. After reading a byte, the internal address counter is automatically increased by 1 through the "acknowledge" of the selected listener. In this manner, a random number of memory locations can be read in successive order. In conjunction with address 127 an overflow to address 0 is initiated. With the stop condition the data output returns to the high impedance mode, and the internal control logic of the memory is reset from the read state into the quiescent state.

Memory reprogramming

The reprogramming cycle of a memory word is comprised of an erase and write process. During the erase process, each bit of the selected word is brought into the "1" state, while "0" states are generated during the write process based on the information in the internal data register, that is to say, in accordance with the third entered control word.

After the 27th and last clock of the control word input, the active programming operation is started by the stop condition. Regulated via internal chip control, the active programming operation can be interrupted by renewed addressing via SCL and SDA.

The duration of the reprogramming mode is based on spreads between units and data samples. Therefore, with standard supply voltages, the erase/write process may extend over max. 30 ms or, more typically, 15 ms. After the data word has been entered without write request (write request: data bit in the data register has been set on "0"), the write mode is suppressed, resulting in a shortened programming time (refer to rapid read-out mode). Should in an already erased memory address (all bits are on logic 1) be subsequently programmed, the erase mode will also be suppressed, leading again to a shortened reprogramming time.

Switch-on mode and chip reset

After the supply voltage V_{DD} has been connected, the data output will be in the high impedance mode. As a rule, the first operating mode to be entered should be the read-out process of a word address, since the chip does not accept the reprogramming mode immediately after activation of the supply voltage. Subsequent to data output and the stop condition, the internal control logic is reset. However, in the case of a subsequent active programming operation, the stop condition will not reset the control logic.

Test mode total erase

The address register is loaded with address 0, the data register with $FF_{(hex)}$ by entering the control word "programming". However, immediately prior to generating the stop condition, input CS2/TP is connected from 0V to 12V. The subsequent stop condition triggers a full deletion procedure which has to be performed under the component address 0 (CSO = L, CS1 = L, CS2 = L). When the full deletion procedure is completed, input CS2/TP must be connected from 12V to 0V again.

Operational states of the I²C bus

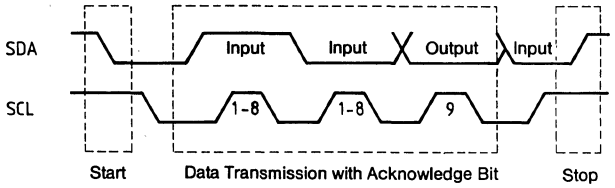


Figure 1

Timing conditions for the I²C bus (high-speed mode)

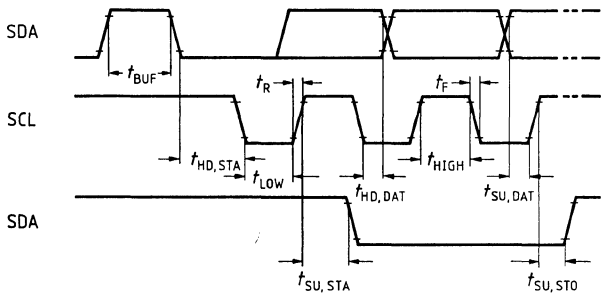


Figure 2

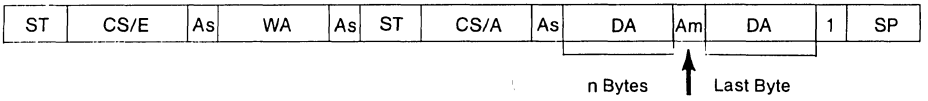
t_{BUF}	$t > t_{LOW\,min}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t > t_{HIGH\,min}$	Start condition hold time
$t_{LOW\,min}$	4.7 µs	Clock LOW period
$t_{HIGH\,min}$	4 µs	Clock HIGH period
$t_{SU;STA}$	$t > t_{LOW\,min}$	Start condition set-up time, only valid for reported start code
$t_{HD;DAT}$	$t > 0$ µs	Data hold time
$t_{SU;DAT}$	$t > 250$ ns	Data set-up time
t_R	$t < 1$ µs	Rise time of both the SDA and SCL line
t_F	$t < 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t > t_{LOW\,min}$	Stop condition set-up time

Note:

All values refer to V_{IH} and V_{IL} levels.

Control word input read

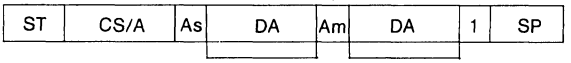
a) complete (with word address input)



n Bytes — Last Byte

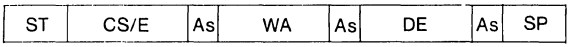
Automatic Incrementation of the Word Address

b) shortened (read starts with last used word address)



n Bytes — Last Byte

Control word input program



(reprogramming starts after this stop condition)

Control word table

Clock No.	1	2	3	4	5	6	7	8	9	(Acknowledge)
CS/E	1	0	1	0	CS2	CS1	CS0	0	0	through memory
CS/A	1	0	1	0	CS2	CS1	CS0	1	0	through memory
WA	X	A6	A5	A4	A3	A2	A1	A0	0	through memory
DE	D7	D6	D5	D4	D3	D2	D1	D0	0	through memory
DA	D7	D6	D5	D4	D3	D2	D1	D0	0	through master

Control word input key:

CS/E	Chip select for data input into memory
CS/A	Chip select for data output out of memory
WA	Memory word address
DE	Data word for memory
DA	Data word read out of memory
D0 to D7	Data bits
ST	Start condition
SP	Stop condition
As	Acknowledge bit from memory
Am	Acknowledge bit from master
CS0, CS1, CS2	Chip select bits
A0 to A6	Memory word address bits

Figure 3

DIP 18

The SDA 3112 is produced in ASBC technology. In connection with VCO (tuner) and a fast prescaler (prescaler factor 1:64), it represents a digitally programmable PLL for a TV set with frequency synthesis tuning. The PLL enables a crystal exact adjustment of the tuner oscillator frequencies for the TV ranges band III/IV/V in 125 kHz resolution (frequency range: 128 to 2000 MHz). A serial interface enables a simple connection to a microprocessor. This microprocessor loads the prescaler and band selection outputs with the appropriate information. At the output LOCK the PLL supplies a state information (locked/released).

Features

- No need for an external integrator
- Noise free telegram transmission
- Integration time constant controlled by software
- Microprocessor compatible

Maximum ratings

Supply voltage	V_S	−0.3 to 7.5	V
Inputs			
Q1, Q2, I_{ref}	V_I	−0.3 to V_S	V
IFC, CPL, PLE	V_I	−0.3 to V_S +0.5	V
PLE	V_I	−0.3 to 7.8	V
F, $\overline{F}$	V_I	−0.3 to V_S + 0.5	V
Outputs			
PD	V_Q	−0.3 to V_S	V
UD	V_Q	−0.3 to 33	V
	I_{QL}	−7	mA
$\overline{BS1}$ . . . . $\overline{BS5}$	V_Q	−0.3 to 16	V
LOCK	I_Q	−1 to 5	mA
Internal pull-up $R_L = 3$ kΩ			
Junction temperature	T_j	140	°C
Storage temperature range	T_{stg}	−55 to 150	°C
Thermal resistance (system-air)	R_{thSA}	80	K/W

Operating range

Supply voltage range	V_S	4.5 to 5.5	V
Input frequency	$f_F, f_{\overline{F}}$	32	MHz
Divider ratio	N	1024 to 16383	
Resistance for I_{ref} $I_{ref} = (V_S - 0.8)R_I$	R_I	80	kΩ
Tuning voltage range open collector	V_D	0.3 to 33	V
Ambient temperature range	T_{amb}	0 to 85	°C

Characteristics ($V_S = 5\ V \pm 0.5\ V$; $T_{amb} = 0$ to 70 °C)

		min	typ	max	
Supply current	I_S	15	22	35	mA
Crystal frequency Series C = 18 pf	f_q		4		MHz
Signal inputs F/$\overline{F}$					
Input voltage	V_{16H}	3.92		$V_S + 0.12$	V
	V_{16L}	3.8		V_S	V
Input current	I_{16}			50	µA
$V_{16} = 5$ V					
Input sensitivity at sine push-pull triggering; $f = 32$ MHz	V_{16}	120		1200	mV_{pp}
Inputs (IFO, CPL, PLE)					
Upper threshold voltage	V_{8H}	2.4			V
Lower threshold voltage	V_{8L}			0.8	V
Input current					
$V_{8H} = 5$ V	I_{8H}			8	µA
$V_{8L} = 0.4$ V	I_{8L}			−550	µA
$V_{8L} = 0.8$ V	I_{8L}			−500	µA
Band select outputs (BS1. . . . BS5)					
Reverse current	I_{3H}			10	µA
$V_{3H} = 15$ V					
Current drain	I_{3H}	0.5		3	mA
$2\ V \leqq V_3 \leqq 15\ V$					
Tuning section PD, UD, I_{ref}, LOCK					
Charge pump current	I_{13}	±250		±550	µA
$I_{pump} = 10 \times I_{ref}$; $R_I = 120$ kΩ; $V_S = 5V$					
Tuning voltage	V_{15L}			0.3	V
$I_{15L} = 1.5$ mA					
Reverse current	I_{15H}			20	µA
$V_{15H} = 33$ V					
Reference current	I_{14}	30		40	µA
ext. $R = 120$ kΩ					
Output voltage	V_{12H}	4.5			V
int. $R_L = 3$ kΩ					
$I_{12H} = -100$ µA					
$I_{12L} = 100$ µA	V_{12L}			0.7	V
IFO, PLE					
Set-up time for					
release	t_{VE}	2			µs
data	t_{VD}	2			µs
Hold time for:					
release	t_{HE}	2			µs
data	t_{HD}	2			µs
CPL					
H pulse width	t_{CH}	2			µs
L pulse width	t_{CL}	2			µs

Circuit description

Triggered by the ECl inputs F/$\overline{F}$ a switchable 32/33 counter operates as a 14 bit synchronous prescaler in the dual modulus method by combining it with a 5 and 9 bit programmable synchronous counter. In this combination the 5 bit counter controls the switch-over from 32 to 33 (block diagram 1). Dividing ratios of $N = 1024$ to 16383 are possible.

The 18 bit deep shift register latch is subdivided into 14 bits for storing the dividing ratio N, as well as 1 bit for selecting the pump current and 3 bits for controlling the 5 band selection outputs.

The telegram is inserted over the serial data input IFO with the H-L slope of the shift clock CPL, when the enable input is set at H. Beginning with LSB, the complement of the dividing ratio is inserted in binary code, then the select bit 2^{14} for the pump current and the band selection control bits 2^{15}, 2^{16}, 2^{17} (please refer to enclosed table).

An integrated control circuit checks the world length (18 bit) of the data telegram. The 18 bit latch accepts the data from the shift register during the L state of the enable input PLE.

A 4 MHz crystal controlled clock oscillator has been integrated in the IC. An internal reference divider divides the output signal of the crystal oscillator ($f_{OSC} = 4$ MHz) by 2048 resulting in 1.953125 kHz (reference signal), providing a frequency resolution of 125 kHz by means of the asynchronous permanent prescaler (dividing factor 1:64).

In a digital phase detector the divided VCO input signal is compared with the reference signal. If the falling slope of the VCO input signal appears before the falling slope of the reference signal, the output DOWN of the phase detector will be in the H state for the duration of the phase difference. However, if above signal sequence is reversed, the output UP will be in the H state instead. The outputs UP/DOWN control the two current sources I+ and I− (charge pump). In case both outputs are in the L state, the charge pump output will be in the high impedance mode (TRI-STATE). Information with respect to either the H or L state will be provided at the LOCK output by the logical "NOR" of the outputs UP/DOWN.

The output current of the charge pump (source current = drain current) is adjusted by an external resistor between pin I_{ref} and V_{CC}. In addition, this output current can be generated by the control bit for the pump current at the same value or at a value increased by a factor of 10 (refer to enclosed table).

The current pulses generated by the charge pump are integrated into the tuning voltage by means of an active low pass filter (on-chip loop amplifier and external RC circuit). The dc output signal of the low pass filter is available at V_D and is used as tuning voltage for the VCO. In order to provide tuning voltages higher than $V_{CC} = 5$ V, the output stage of the amplifier consists of a transistor with an open collector. The external collector resistor can be connected to voltages up to 33 V.

To switch voltages higher than $V_S = 5$ V, the band selection outputs (BS1, BS2, BS3, BS4, BS5) include current drains with open collectors. It is therefore possible to directly connect transistors operating as band selection switches without the use of current limiting resistors (please refer to enclosed application current).

Pin configuration

Pin No.	Symbol	Function
1	Q1	Crystal
2	Q2	Crystal
3	BS1	Standard switchover output
4	BS2	Band selection output BS
5	BS3	Band selection output VHF
6	BS4	Band selection output UHF
7	BS5	Band selection output I/III
8	PLE	Release input for shift register
9	GND	Ground
10	CPL	Shift clock pulse input
11	IFO	Data input
12	LOCK	Lock output
13	PD	Amplifier input/charge pump output
14	I_{ref}	Current adjustment for charge pump
15	V_D	Tuning voltage output
16	$\overline{F}$	Signal input
17	F	Signal input
18	V_S	Supply voltage

Loop-filter calculations

Loop bandwidth: $\sqrt{\frac{I_p \times K_{VCO}}{C_1 \times P \times N}} = \omega_R$

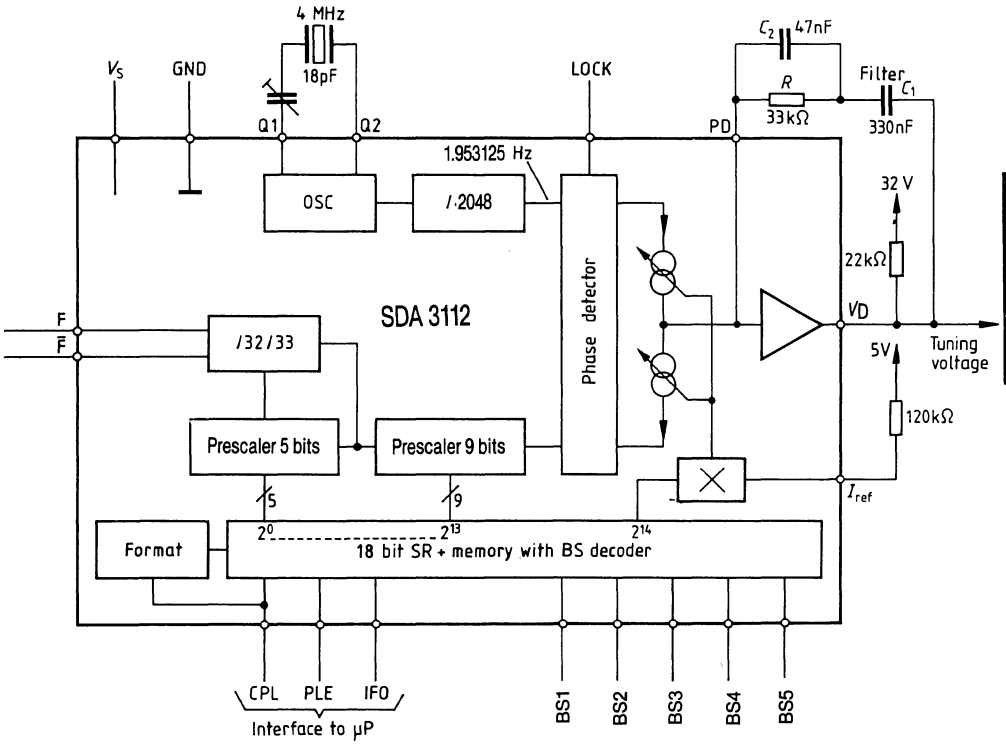
Attenuation $1/2 \times \omega_R \times R \times C_1 = \xi$

P = prescaler
N = programmable divider ratio
I_p = pump current
S_{VCO} = tuner voltage characteristic
R_1 C_1 = loop filter

Example for channel 47:

P = 64 N = 11520 I_p = 200 µA S_{VCO} = 18.7 MHz/V R = 33 kΩ C_1 = 330 nF
ω_R = 124 Hz f_R = 20 Hz ξ = 0.675 Standard dimensioning: $C_2 \approx$ C1/5

Block diagram

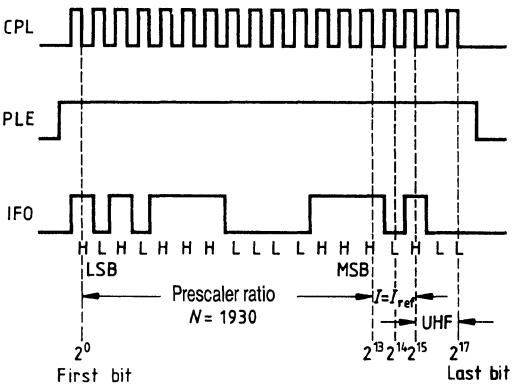


Truth Table

"IFO" bit 2^{14}	Pump Current I_p
L	I_{ref}
H	10 x I_{ref}

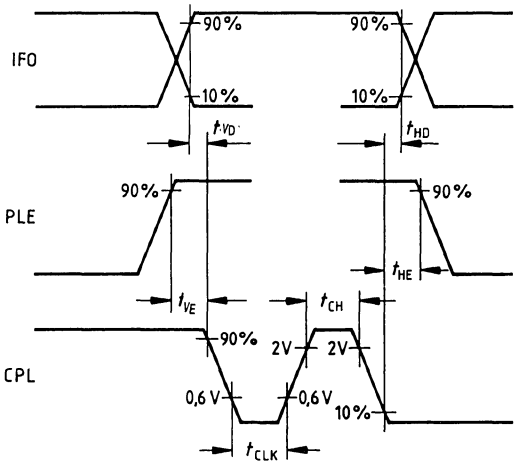
"IFO" bit			Band selection outputs (L = conducting, H = blocking)				
2^{15}	2^{16}	2^{17}	BS1	BS2	BS3	BS4	BS5
L	L	L	L	L	L	L	H
L	L	H	L	L	H	H	H
L	H	L	L	H	L	H	L
L	H	H	L	H	H	H	H
H	L	L	H	L	L	L	H
H	L	H	H	L	H	H	H
H	H	L	H	H	L	H	L
H	H	H	H	H	H	H	H

Pulse diagram

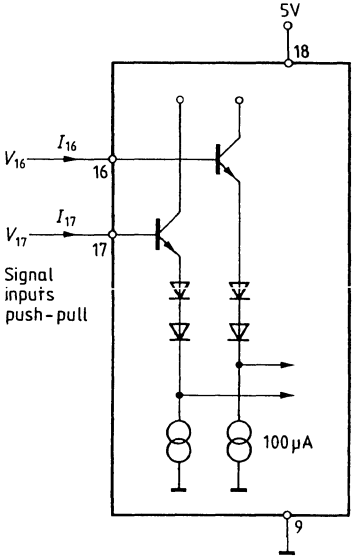


Pulse diagram

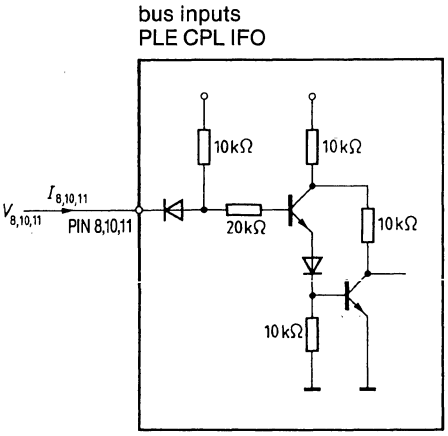
Set-up and hold times



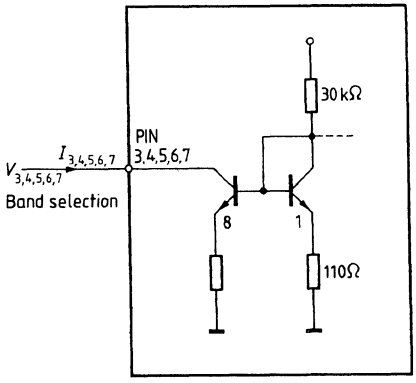
Test and measurement circuits



Test circuit 1

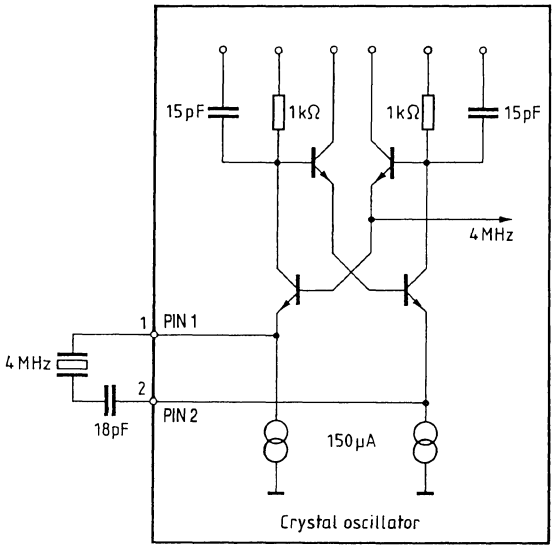


Test circuit 2

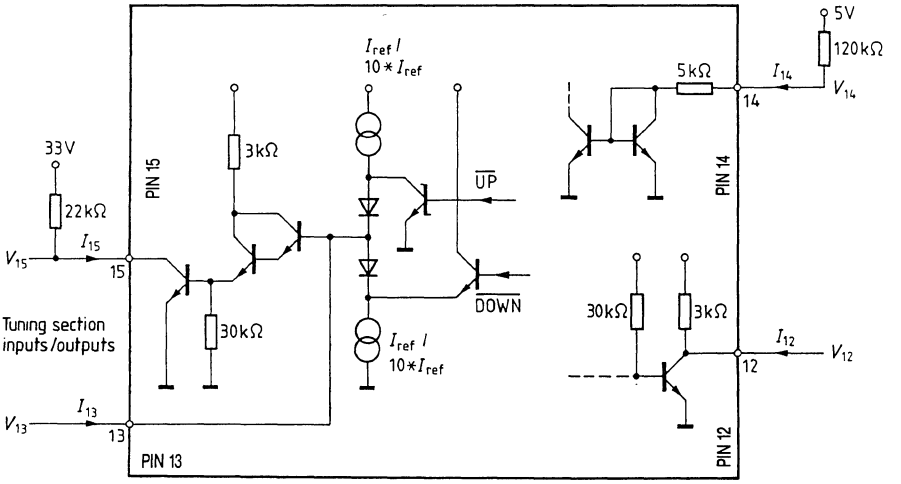


Test circuit 3

Test and measurement circuits



Test circuit 4

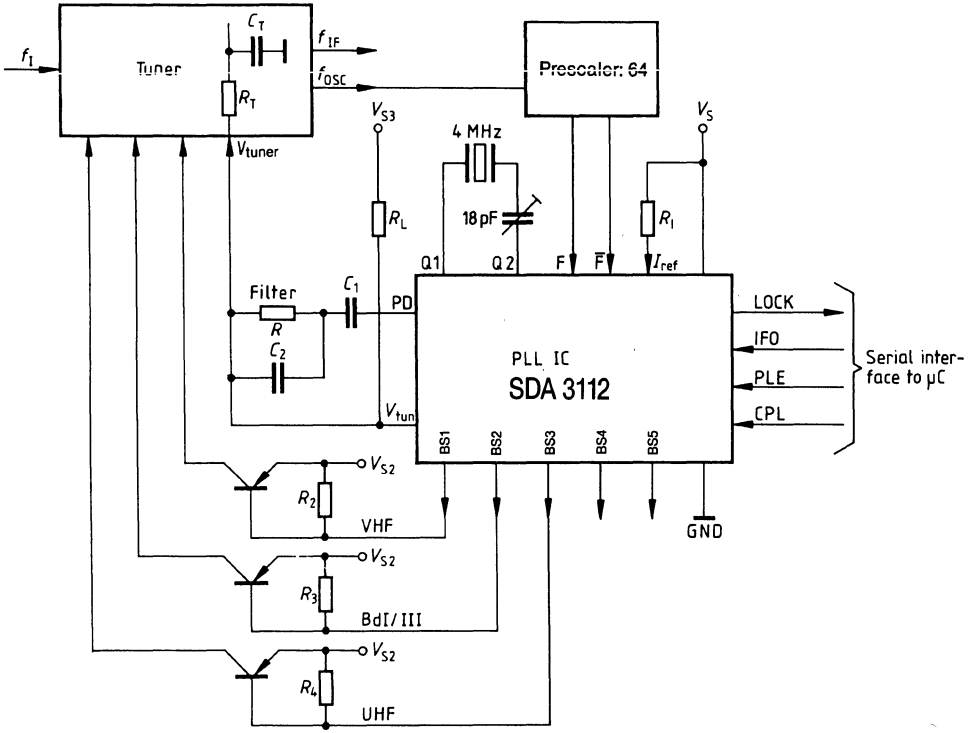


Test circuit 5

Application circuit

Design proposal

$R_I = 120\ k\Omega$ ($I_p = 35/350\ \mu A$)
$R_L = 22\ k\Omega$, $R_2 \ldots R_4 = 22\ k\Omega$
Loop filter: $R = 33\ k\Omega$, $C_1 = 330\ nF$, $C_2 = 47\ nF$
Post filter (in the tuner): $R_T = 10\ k\Omega$, $C_T = 47\ nF$



DIP 18

Combined with a VCO (tuner), the SDA 3203 comprises a digital programmable phase-locked loop for television devices designed to use the PLL frequency synthesis tuning principle.

The PLL provides a crystal-stable frequency for tuner oscillators between 16...1300 MHz in the 62.5 kHz raster. By including an external prescaler 1/2, the component can also be used for synthesizing applications of up to 2.4 GHz (e.g. satellite receivers). As a result, the resolution is doubled to 125 kHz. The tuning process is controlled via an I²C bus by the microprocessor.

Features

- Low current consumption
- Message transmission via I²C bus
- 4 software-controlled outputs
- Cost-effective and space-saving design
- Prescaler output frequency is free from interference radiation

Circuit description

Tuning section (refer to block diagram)

UHF/VHF The tuner signal is capacitively coupled at the UHF/VHF input and subsequently amplified.

REF The reference input REF should be disabled by a capacitor of low series inductance. The amplified signal passes through an asynchronous divider with a fixed ratio of $P = 8$ and an adjustable divider $N = 256...32767$. Subsequent to this process, the signal is compared in a digital frequency phase detector with a reference frequency $f_{REF} = 7.8125$ kHz.

Q1, Q2 This frequency has been derived from a 4 MHz crystal oscillator (pin Q1, Q2) by dividing its output signal by $Q = 512$.

The phase detector includes two outputs UP and DOWN which control the two current sources $I+$ and $I-$ of a charge pump. If the negative edge of the divided VCO signal appears prior to the negative edge of the reference signal, the current source $I+$ will pulsate for the duration of the phase difference. However, during the reversed sequence of the negative edges, the current source $I-$ will begin to pulsate.

PD, V_D If both signals are in phase, the charge pump output PD changes into the high impedance state (PLL in lock). An active low pass filter (internal amplifier, external output transistor at V_D, and RC combination) integrates the current pulses as the tuning voltage for the VCO.

With the control bit 5 *I* the pump current can be switched between two values per software. Through this switch-over, the control characteristics of the PLL during lock-in can be changed, i.e. varying tuner characteristics in the various TV bands can be adjusted.

P0..P3 The software-controllable outputs P0, P1, P2 and P3 can drive external PNP transistors (internal current limit) which operate as band selection switch.

P4..P7 The open collector outputs P4, P5, P6, P7 can be used for a variety of different applications.

I²C bus interface

SCL, SDA An asynchronous bidirectional data bus is used for data transfer between the processor and the PLL. As a rule, the clock pulse is supplied by the processor (input SCL), while pin SDA operates as input or output depending on the direction of data flow (open collector, external pull-up resistor).

The data from the processor pass through an I²C bus control. Depending on their function, the data are subsequently filed in registers (latch 0-3). If the bus is free, both lines will be in the marking state (SDA, SCL are High). Each message begins with the start conditions of SDA returning into Low, while SCL remains in High. All additional information transfer takes place during SCL = Low and the data is forwarded to the control with the positive clock edge. However, if SDA returns to High, while SCL is in High, the message is ended since the PLL acknowledges a stop condition.

For the following, also refer to table "Logic allocation".

All messages are transmitted byte-by-byte, followed by a 9. clock pulse, while the control returns the SDA line to Low (acknowledge conditions). The first byte is comprised of 7 address bits. These are used by the processor to select the PLL from several peripheral components (chip-select). The 8. bit is always Low.

In the data portion of the message the 1. bit of the 1. or 3. data byte determines whether a divider ratio or a control information is to follow. In each case, the 2. byte of the same data type or a stop condition has to follow the 1. byte.

V_S, GND When the supply voltage is injected, a Power on Reset circuit prevents the PLL from setting the SDA line at Low which would disable the bus.

Maximum ratings

		min	max		Remarks
Supply voltage	V_S	−0.3	6	V	
Output PD	V_1	−0.3	V_S	V	
Crystal Q1	V_2	−0.3	V_S	V	
Crystal Q2	V_3	−0.3	V_S	V	
Bus input/output SDA	V_4	−0.3	V_S	V	
Bus input SCL	V_5	−0.3	V_S	V	
Port output P7	V_6	−0.3	16	V	
Port output P6	V_7	−0.3	16	V	
Port output P5	V_8	−0.3	16	V	
Port output P4	V_9	−0.3	16	V	
Port output P3	V_{10}	−0.3	16	V	
Port output P2	V_{11}	−0.3	16	V	
Port output P1	V_{12}	−0.3	16	V	
Port output P0	V_{13}	−0.3	16	V	
Signal input UHF/VHF	V_{15}	−0.3	2.5	V	
Reference input REF	V_{16}	−0.3	2.5	V	
Output active filter V_D	V_{18}	−0.3	V_S	V	
Bus output SDA	I_{4L}	−1	5	mA	open collector
Port output P7	I_{6L}	−1	5	mA	open collector
Port output P6	I_{7L}	−1	5	mA	open collector
Port output P5	I_{8L}	−1	5	mA	open collector
Port output P4	I_{9L}	−1	5	mA	open collector
Junction temperature	T_j		125	°C	
Storage temperature range	T_{stg}	−40	125	°C	
Thermal resistance (system-air)	R_{thSA}		80	K/W	

Operating range

Supply voltage	V_S	4.5	5.5	V	
Ambient temperature	T_A	0	80	°C	
Input frequency	f_{15}	16	1300	MHz	
Crystal frequency	$f_{2,3}$		4	MHz	
Divider factor	N	256	32767		

Characteristics

$V_S = 5$ V; $T_A = 25$ °C

		Test conditions	Test circuit	min	typ	max	
Current consumption	I_S		1	35	55	75	mA
Crystal frequency	$f_{2,3}$	Series capacitance 18 pF	1	3.99975	4.000	4.00025	MHz
Input sensitivity UHF/VHF							
	a_{15}	f_{15} = 70... 500 MHz	2	−27/10		3/315	dBm/*
	a_{15}	f_{15} = 500...1000 MHz	2	−24/14		3/315	dBm/*
	a_{15}	f_{15} = 1100 MHz	2	− 20/22		3/315	dBm/*
Band selection outputs P0...P3		(current sinks with internal resistance $R_i = 12$ kΩ)					
Leakage current	I_{13H}	$V_{13H} = 13.5$ V	3			10	µA
Sink current	I_{13L}	$V_{13H} = 12$ V	3	0.7	1	1.5	mA
Port outputs P4...P7		(switch with open collector)					
Leakage current	I_{9H}	$V_{9H} = 13.5$ V	4			10	µA
Residual voltage	V_{9L}	$I_{9L} = 1.7$ mA	4			0.5	V
Phase detector output PD		($V_S = 5$ V)					
Charge pump current	I_{1H}	5 I = High; $V_1 = 2$ V	5	±90	±220	±300	µA
Charge pump current	I_{1H}	5 I = Low; $V_1 = 2$ V	5	±22	±50	±75	µA
Output voltage	V_{IL}	locked	5	1.5		2.5	V
Active filter output V_D		Test modus T0 = 1 PD = Tristate					
Output current	I_{18}	$V_{18} = 0.8$ V; $I_{14} = 90$ µA	5	− 500			µA
Output voltage	V_{18}	$V_{1L} = 0$ V	5			100	mV
Bus inputs SCL, SDA							
Input voltage	V_{5H}		6	3		5.5	V
	V_{5L}		6			1.5	V
Input current	I_{5H}	$V_{5H} = V_S$	6			50	µA
	I_{5L}	$V_{5L} = 0$ V	6			−100	µA
Output SDA (open collector)							
Output voltage	I_{4H}	$R_L = 5.5$kΩ	6			10	µA
	V_{4L}	$I_{4L} = 2$ mA	6			0.4	V
Edges SCL, SDA							
Rise time	t_R		6			1	µs
Fall time	t_F		6			0.3	µs
Shift register clock pulse SCL							
Frequency	f_5		6	0		100	kHz
H-pulse width	$t_{5\,HIGH}$		6	4			µs
L-pulse width	$t_{5\,LOW}$		6	4			µs

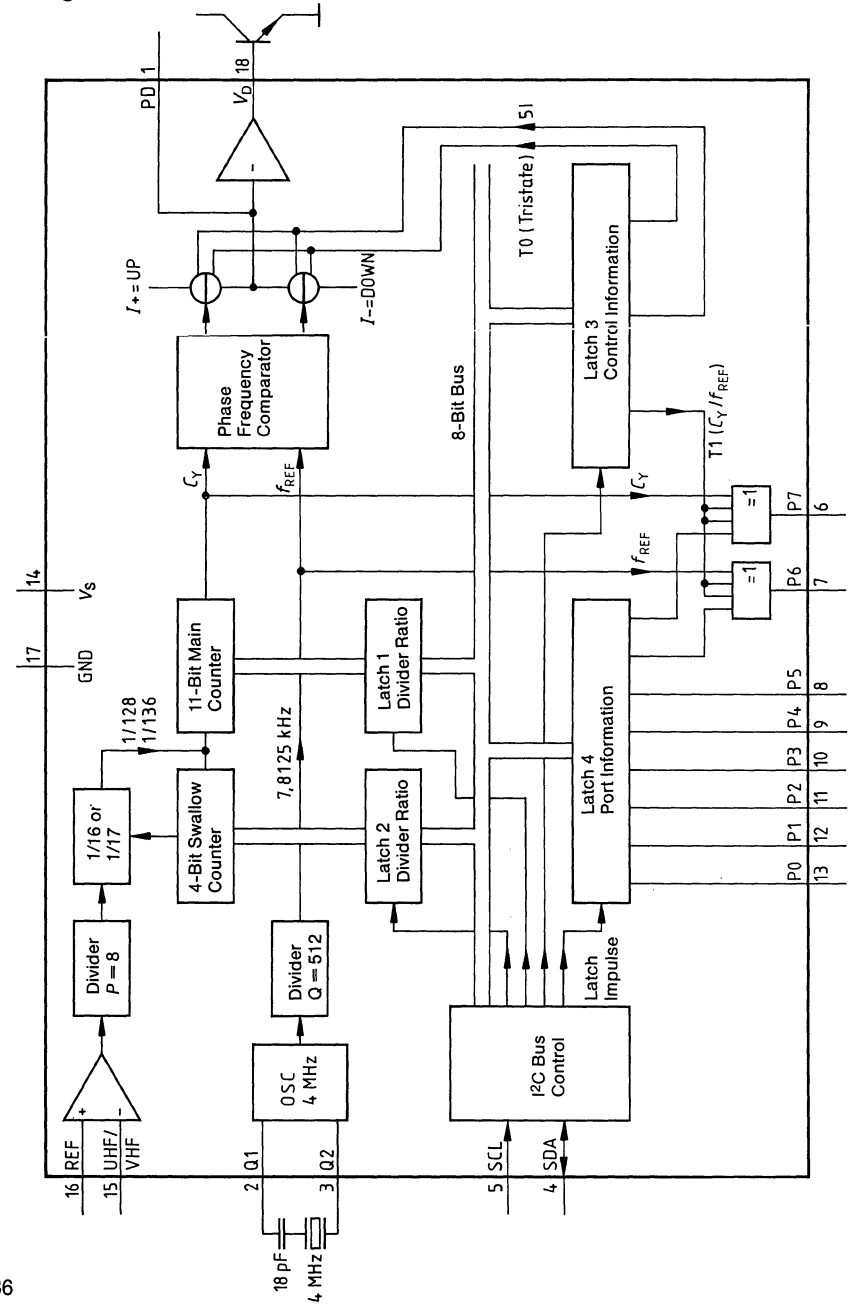
*) listed as mV_{rms} with 50Ω

Characteristics (cont'd.)		Test conditions	Test circuit	min	typ		max	
Start								
Set-up time	t_{SUSTA}		6	4				µs
Hold time	t_{HDSTA}		6	4				µs
STOP								
Set-up time	t_{SUSTO}		6	4				µs
Bus free time	t_{BUF}		6	4				µs
Data transfer								
Set-up time	t_{SUDAT}		6	0.3				µs
Hold time	t_{HDDAT}		6	0				µs

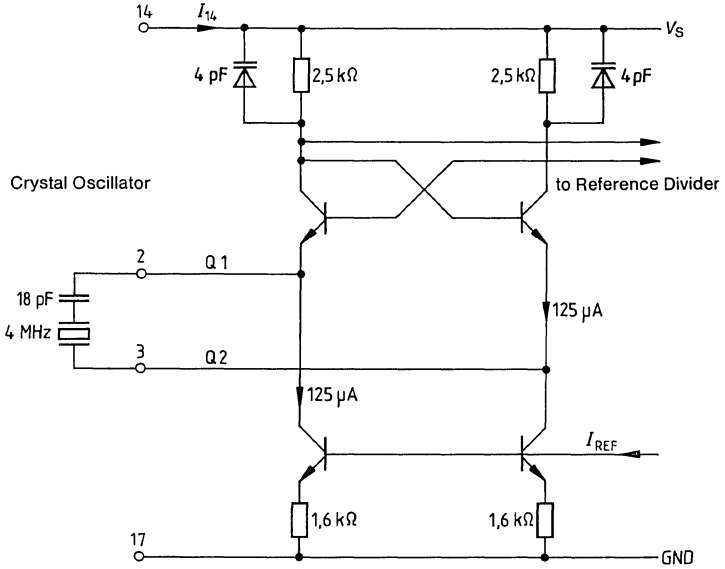
Pin description

Pin	Symbol	Function
1	PD	Input for active filter/output for charge pump
2	Q1	Crystal
3	Q2	Crystal
4	SDA	Data I/O for I^2C bus
5	SCL	Clock input for I^2C bus
6	P7	Port output (open collector)
7	P6	Port output (open collector)
8	P5	Port output (open collector)
9	P4	Port output (open collector)
10	P3	Port output (current sink)
11	P2	Port output (current sink)
12	P1	Port output (current sink)
13	P0	Port output (current sink)
14	V_S	Supply voltage
15	UHF/VHF	Signal input
16	REF	Amplifier-reference input
17	GND	Ground
18	V_D	Output of active filter

Block diagram

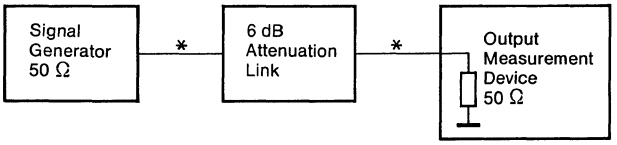


Measurement circuit 1

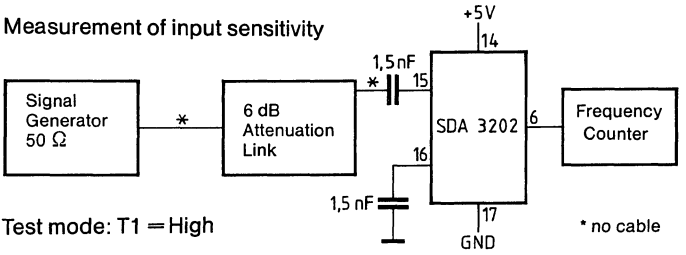


Measurement circuit 2

Calibration of signal generator



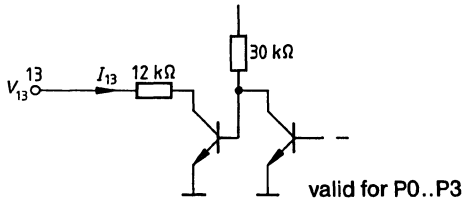
Measurement of input sensitivity



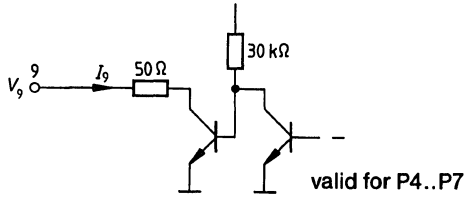
Test mode: T1 = High

* no cable

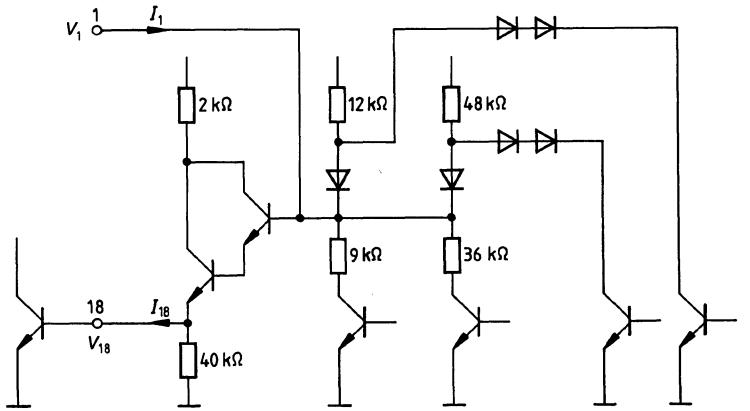
Measurement circuit 3



Measurement circuit 4

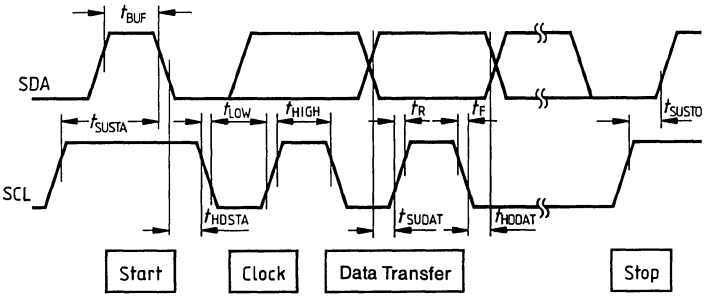


Measurement circuit 5



Measurement circuit 6a

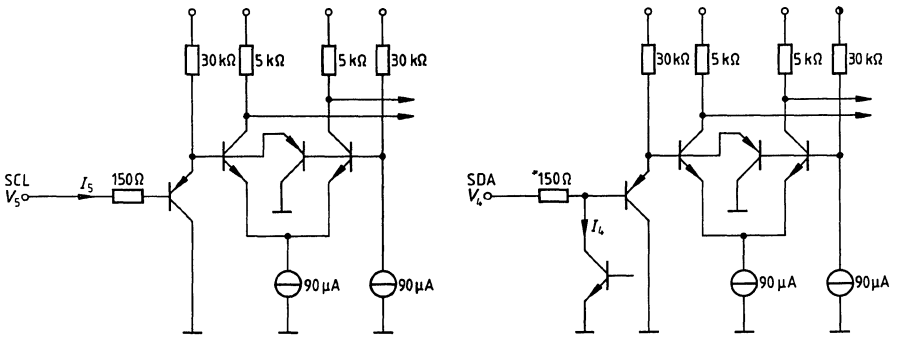
I²C bus time diagram



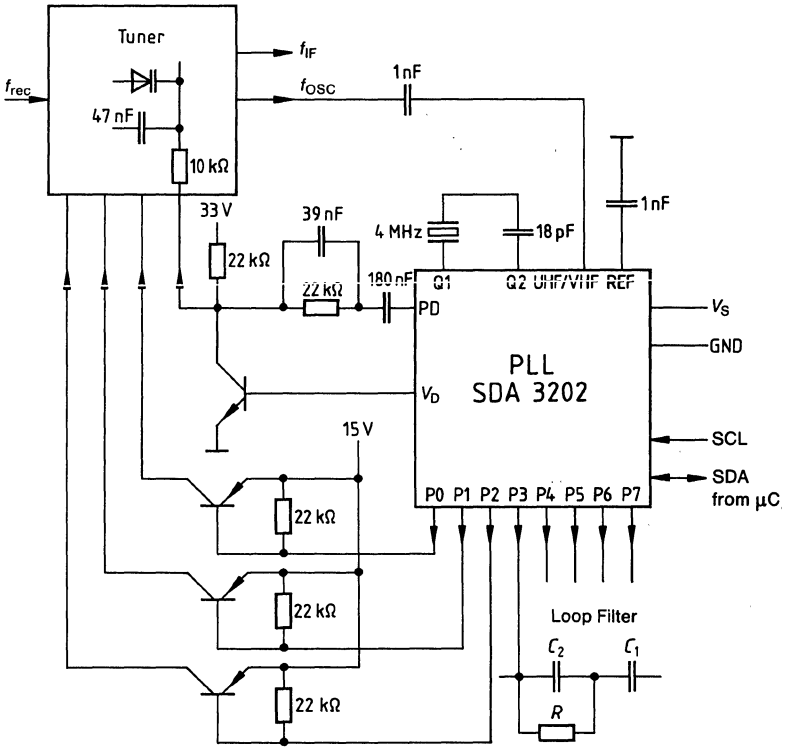
t_{SUSTA}	Set-up time (Start)
t_{HDSTA}	Hold time (Start)
t_{HIGH}	H-pulse width (Clock)
t_{LOW}	L-pulse width (Clock)
t_{SUDAT}	Set-up time (Data transfer)
t_{HDDAT}	Hold time (Data transfer)
t_{SUSTO}	Set-up time (Stop)
t_{BUF}	Bus free time
t_F	Fall time
t_R	Rise time

Above times are referenced to V_{IH} and V_{IL} values

Measurement circuit 6b



Application circuit



Computation for loop filter

Loop bandwidth: $\omega_R = \sqrt{\frac{I_p \times K_{VCO}}{C_1 \times P \times N}}$

Attenuation: $\xi = 0.5 \times \omega_R \times R \times C_1$

P	= Prescaler
N	= Progr. divider
I_P	= Pump current
K_{VCO}	= Tuner slope
R, C_1	= Loop filter

Example for channel 47

$P = 8$; $N = 11520$; $I_p = 100\ \mu A$; $K_{VCO} = 18.7$ MHz/V; $R = 22\ k\Omega$; $C_1 = 180$ nF
$\omega_R = 336$ Hz; $f_n = 54$ Hz; $\xi = 0.67$

Standard dimensioning: $C_2 = C_{1/5}$

Description of function, application and circuit

Logic allocation

	MSB								A = Acknowledge
Address byte	1	1	0	0	0	0	1	0	A
Prog. divider byte 1	0	n14	n13	n12	n11	n10	n9	n8	A
Prog. divider byte 2	n7	n6	n5	n4	n3	n2	n1	n0	A
Control info byte 1	1	5I	T1	T0	1	1	1	0	A
Control info byte 2	P7	P6	P5	P4	P3	P2	P1	P0	A

Divider ratio:

$$N = 16384 \times n14 + 8192 \times n13 + 4096 \times n12 + 2046 \times n11 + 1024 \times n10 + 512 \times n9 + 256 \times n8 + + 128 \times n7 + 64 \times n6 + 32 \times n5 + 16 \times n4 + 8 \times n3 + 4 \times n2 + 2 \times n1 + n0$$

Band selection:

P3...P0 = 1 Current sink is active

Port outputs:

P7...P4 = 1 Open collector output is active

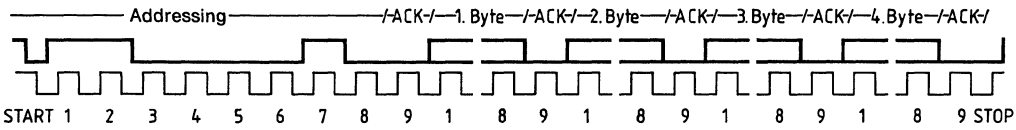
Switch-over of pump current:

5I = 1 High current

Test mode:

T1,T0 = 0,0 Normal operation
T1 = 1 P6 = f_{REF}; P7 = Cy
T0 = 1 Tristate charge pump

Pulse diagram



MESSAGE SAMPLES

Start-Adr-Tv1-Tv2-St1-St2-Stop
Start-Adr-St1-St2-Tv1-Tv2-Stop
Start-Adr-Tv1-Tv2-St1-Stop
Start-Adr-St1-St2-Tv1-Stop
Start-Adr-Tv1-Tv2-Stop
Start-Adr-St1-St2-Stop
Start-Adr-Tv1-Stop
Start-Adr-St1-Stop

Start = start condition
Adr = addressing
Tv1 = divider ratio 1. byte
Tv2 = divider ratio 2. byte
St1 = control word 1. byte
St2 = control word 2. byte
Stop = stop condition

DIP 20

Combined with a VCO (tuner), the SDA 3203 comprises a digital programmable phase-locked loop for television devices designed to use the PLL frequency synthesis tuning principle.

The PLL provides a crystal-stable frequency for tuner oscillators between 16...1300 MHz in the 62.5 kHz raster. By including an external prescaler 1/2, the component can also be used for synthesizing applications of up to 2.4 GHz (e.g. satellite receivers). As a result, the resolution is doubled to 125 kHz. The tuning process is controlled via a 3-wire bus by the microprocessor.

Features

- Low current consumption
- Message transmission via a 3-wire bus
- 4 software-controlled outputs
- Cost-effective and space-saving design
- Prescaler output frequency is free from interference radiation

Circuit Description

Tuning section (refer to block diagram)

UHF/VHF — The tuner signal is capacitively coupled at the UHF/VHF input and subsequently amplified.

REF — The reference input REF should be disabled by a capacitor of low series inductance. The amplified signal passes through an asynchronous divider with a fixed ratio of $P = 8$. An anti-oscillation circuitry prevents the first divider stage from oscillating when the input signal is missing. As a result, the PLL maintains the correct control direction should the tuner oscillation be terminated. Subsequently, a switchable 16/17 counter is activated. The combination of this counter with a 4-bit and 10-bit programmable counter provides an adjustable divider operating in the dual modulus mode. The 4-bit counter drives the switch-over from 17 to 16. Divider ratios of $N = 256...16383$ are possible. The divided signal is compared in a digital frequency phase detector with a frequency

Q1, Q2 — $f_{REF} = 7.8125$ kHz. This frequency has been derived from a 4 MHz crystal oscillator (pin Q1, Q2) by dividing its output signal by $Q = 512$.

The phase detector includes two outputs UP and DOWN which control the current sources $I+$ and $I-$ of a charge pump. If the negative edge of the divided VCO signal appears prior to the negative edge of the reference signal, the current source $I+$ will pulsate for the duration of the phase difference. However, during the reversed sequence of the negative edges, the current source $I-$ will begin to pulsate.

PD, V_D — If both signals are in phase, the charge pump output PD changes into the high impedance state (PLL in lock). An active low pass filter (internal amplifier, external output transistor at V_D, and RC combination) integrates the current pulses as the tuning voltage for the VCO.

P1...P4 — The software-controllable outputs P1, P2, P3 and P4 drive the external PNP transistors (internal current limiting) which operate as band selection switch.

TVSAT — In the TVSAT mode (pin TVSAT = 0 V), the message bit for P1 becomes the 15. divider bit providing divider ratios of $N = 256...32767$.

3-wire bus interface (refer to description of functions)

DATA
CLOCK
ENABLE — Via the serial data input DATA the message is read into an 18-bit deep shift register with the positive edge of the CLOCK supplied by the processor when the ENABLE input is also in High. To further ensure the prevention of interference products, a format control discards all messages which exceed eigtheen clock pulses during the Enable-High cycle.

Beginning with the MSB, the four band selection control bits for the port outputs and the divider ratio are inserted in binary code. An 18-bit latch accepts the data from the shift register with the negative edge of the Enable pulse.

TEST1 kHz 62.5 — During standard operation TEST1 = Low an eight-fold reference frequency 62.5 kHz is present at pin kHz 62.5 During test operation TEST 1 = High, a distiction is made between test mode 1 (ENABLE = Low) and test mode 2 (ENABLE = High).

DATA	CLOCK	kHz 62.5	Operating mode
Shift data	Shift clock	62.5 kHz	Standard operation
Output progr. divider	Output ref. divider	62.5 kHz	Test mode 1
Input phase detector var. frequency	Input phase detector ref. frequency	1/128 (fixed)	Test mode 2

Maximum ratings

		min	max	
Supply voltage	V_S	−0.3	6	V
Test input TEST1	V_1	−0.3	V_S	V
ENABLE	V_2	−0.3	6	V
DATA	V_3	−0.3	6	V
	I_3		3	mA
CLOCK	V_4	−0.3	6	V
	I_4		3	mA
Crystal Q1	V_6	−0.3	V_S	V
Crystal Q2	V_7	−0.3	V_S	V
Output active filter UD	V_9	−0.3	V_S	V
Output charge pump PD	V_{10}	−0.3	V_S	V
Port output P1	V_{11}	−0.3	16	V
Port output P2	V_{12}	−0.3	16	V
Port output P3	V_{13}	−0.3	16	V
Port output P4	V_{14}	−0.3	16	V
Signal input UHF/VHF	V_{15}	−0.3	3	V
Reference input REF	V_{20}	−0.3	3	V
Output 62.5 kHz	V	−0.3	V_S	V
Junction temperature	T_j		125	°C
Storage temperature range	T_{stg}	−40	125	°C
Thermal resistance (system-air)	R_{thSA}		60	K/W

Operating range

Supply voltage	V_S	4.5	5.5	V
Ambient temperature	T_A	0	70	°C
Input frequency	f_{15}	16	1300	MHz
Crystal frequency	$f_{6,7}$		4	MHz
Divider factor	N	256	32767	

Characteristics

$V_S = 5$ V; $T_A = 25$ °C

		Test conditions	Test circuit	min	typ	max	
Current consumption	I_S	$V_S = 5$ V	1	20	50	70	mA
Crystal frequency	$f_{6,7}$	Series capacity 18 pF	1			4	MHz
Input sensitivity UHF/VHF							
	a_{15}	$f_{15} = 80$-100 MHz	2	−24/14		3/315	dBm/*)
	a_{15}	$f_{15} = 100$-1000 MHz	2	−27/10		3/315	dBm/*)
	a_{15}	$f_{15} = 1300$ MHz	2	−15/40		3/315	dBm/*)
Input dc voltage	V_{15}	UHF/VHF and REF not connected	2		2		V
Band selection outputs P1...P4							
		(current sinks with internal resistance $R_l = 12$ kΩ)					
Leakage current	I_{11H}	$V_{11H} = 13.5$ V	3			10	µA
Sink current	I_{11L}	$V_{11L} = 12$ V	3	0.7	1.0	1.5	mA
Phase detector output PD							
		$V_S = 5$ V					
Pump current	I_{10}	lock in	5	±90	±150	±220	µA
Output voltage	V_{10}	lock in	5	1.5		2.5	V
Leakage current	I_{10}	lock in	5	−0.2		0.2	µA
Active filter output V_D							
Output current	I_9	$V_D = 0.8$ V	5	500			µA
Test input TEST1							
Input voltage	V_{1H}		6	3		V_S	V
	V_{1L}		6			0.8	V
Input current	I_{1H}	$V_{1H} = 5$ V	6			50	µA
	I_{1L}	$V_{1L} = 0$ V	6			−100	µA
Test outputs CLOCK, DATA (open collector)							
Output voltage	V_{2L}	$I_{2L} = 1$ mA	6			0.4	V
	V_{2H}		6			5.5	V
Leakage current	I_{2H}	$V_{2H} = 5$ V	6	10			µA
Output 62.5 kHz (current sink with open collector)							
Output voltage	V_{20}		4	0.4		5.5	V
Output current	I_{20}		4	100		200	µA

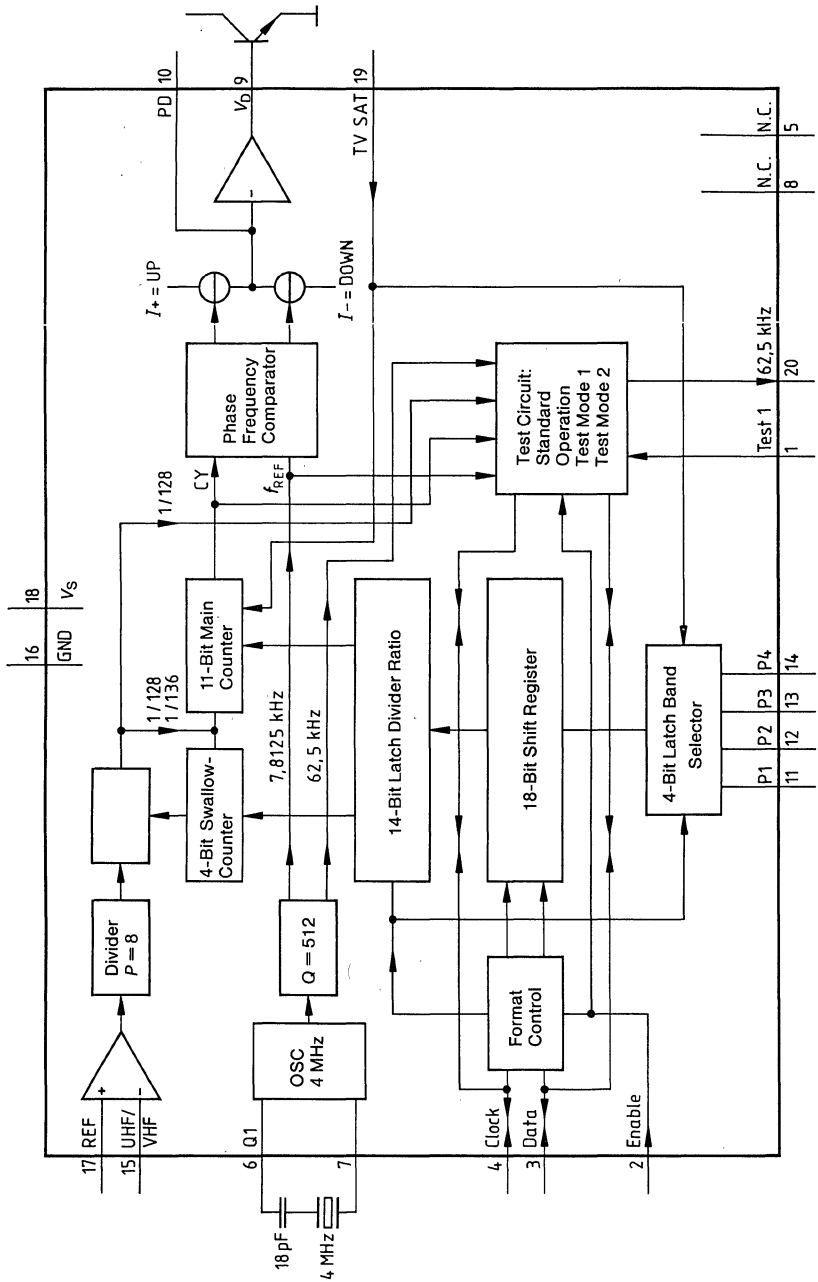
*) listed as mV_{rms} with 50 Ω

Characteristics (cont'd.)		Test conditions	Test circuit	min	typ	max	
Bus inputs CLOCK, DATA, ENABLE							
Input voltage	V_{2H}		6	3		V_S	V
	V_{2L}		6			0.8	V
Input current	I_{2H}	$V_{2H} = 5\,V$	6			50	µA
	I_{2L}	$V_{2L} = 0\,V$	6			−100	µA
Data transfer							
Set-up time	t_{SUDAT}	DATA	6	2			µs
Hold time	t_{HDDAT}	DATA	6	2			µs
CLOCK							
H-pulse width	t_{HIGH}	CLOCK	6	2			µs
ENABLE							
Set-up time	t_{SUEN}	ENABLE	6	2			µs
Hold time	t_{HDEN}	ENABLE	6	2			µs

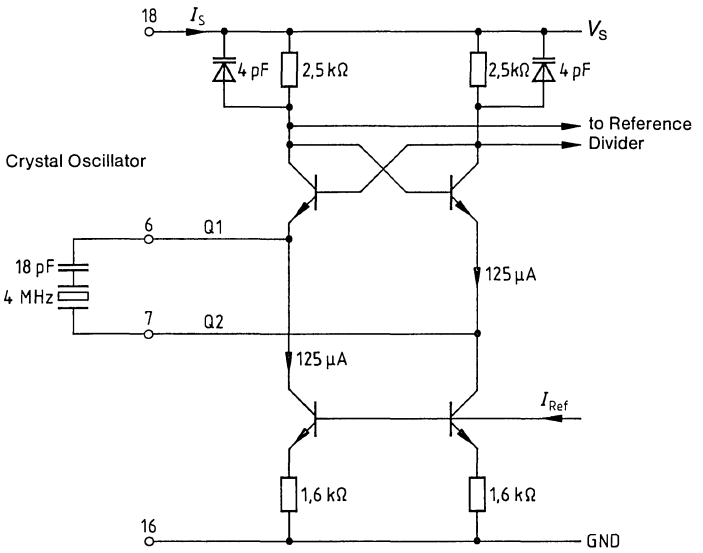
Pin description

Pin	Symbol	Function
1	TEST1	Test input 1
2	ENABLE	Enable input – shift register
3	DATA	Data input – shift register
4	CLOCK	Clock input — shift register
5	N.C.	
6	Q1	Crystal
7	Q2	Crystal
8	N.C.	
9	V_D	Auxiliary output for active filter
10	PD	Phase detector output
11	P1	Port output
12	P2	Port output
13	P3	Port output
14	P4	Port output
15	UHF/VHF	Signal input
16	GND	Ground
17	REF	Amplifier-reference input
18	V_S	Supply voltage
19	TVSAT	Switch-over TVSAT range
20	kHz 62.5	62.5 kHz output/test output

Block diagram

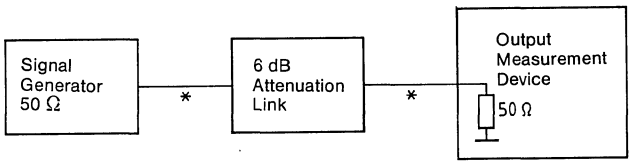


Measurement circuit 1

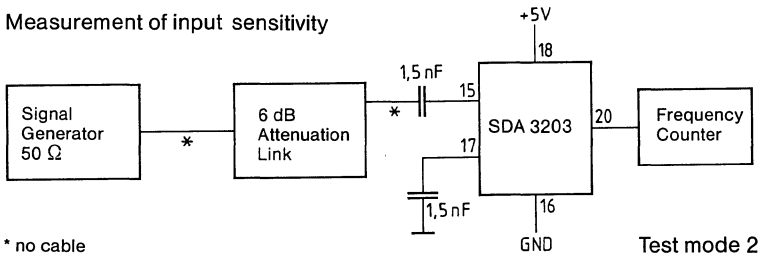


Measurement circuit 2

Calibration of signal generator



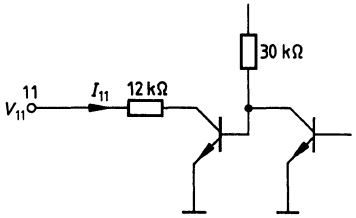
Measurement of input sensitivity



* no cable

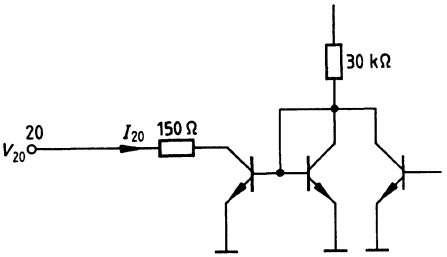
Test mode 2

Measurement circuit 3



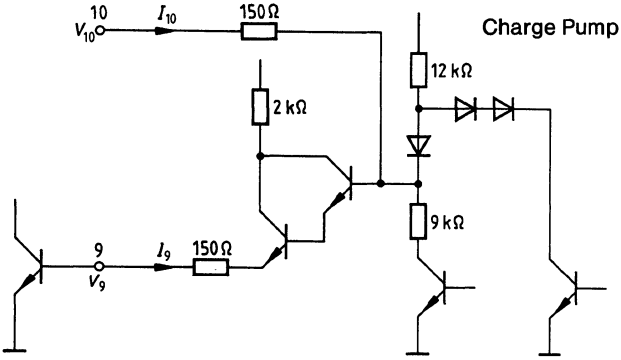
valid for P1..P4

Measurement circuit 4



62.5 kHz Output

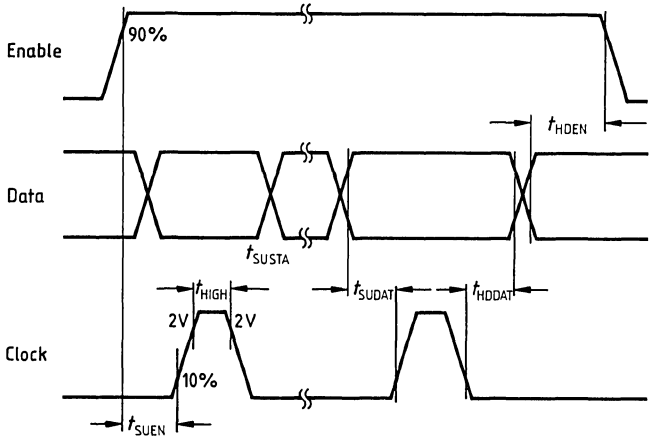
Measurement circuit 5



Charge Pump Outputs PD, V_D

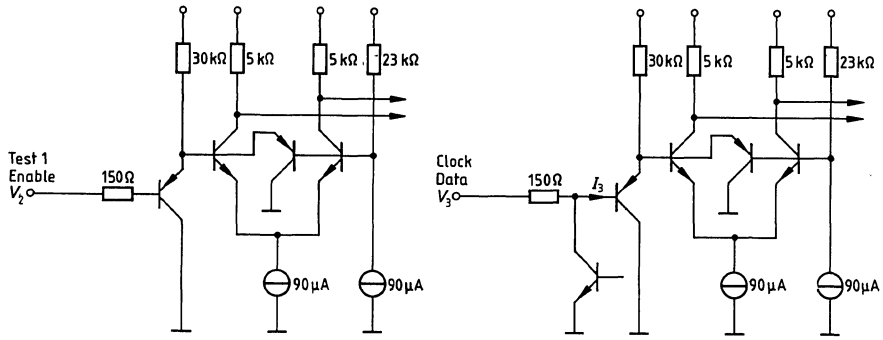
Measurement circuit 6a

I²C bus time diagram

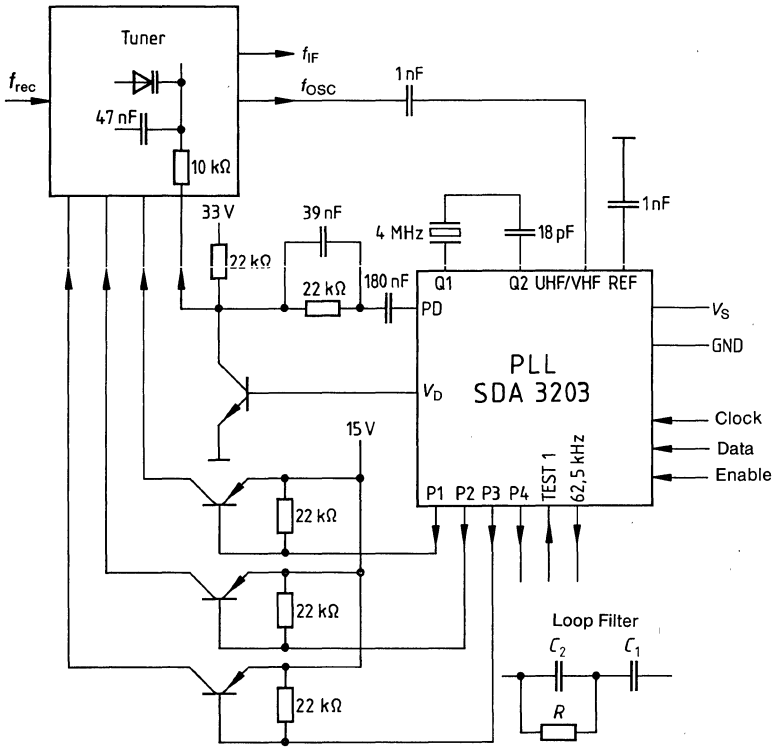


t_{SUEN}	Set-up time (Enable)
t_{HDEN}	Hold time (Enable)
t_{HIGH}	H pulse width (Clock)
t_{SUDAT}	Set-up time (Data transfer)
t_{HDDAT}	Hold time (Data transfer)

Measurement circuit 6b



Application circuit



Computation for loop filter

Loop bandwidth: $\omega_R = \sqrt{\frac{I_p \times K_{VCO}}{C_1 \times P \times N}}$

Attenuation: $\xi = 0.5 \times \omega_R \times R \times C_1$

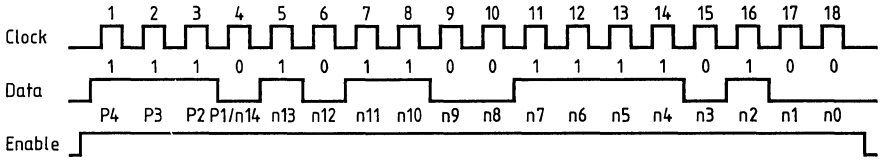
P = Prescaler
N = Progr. divider
I_P = Pump current
K_{VCO} = Tuner slope
R, C_1 = Loop filter

Example for channel 47

$P = 8$; $N = 11520$; $I_p = 100\ \mu A$; $K_{VCO} = 18.7$ MHz/V; $R = 22\ k\Omega$; $C_1 = 180$ nF
$\omega_R = 336$ Hz; $f_n = 54$ Hz; $\xi = 0.67$

Standard dimensioning: $C_2 = C_{1/5}$

Pulse diagram



Divider ratio $N = n13 \times 8192 + n12 \times 4096 + n11 \times 2048 + n10 \times 1024 + n9 \times 512 + n8 \times 256 + n7 \times 128 + n6 \times 64 + n5 \times 32 + n4 \times 16 + n3 \times 8 + n2 \times 4 + n1 \times 2 + n0$

Example: $N = 11508$

Band selection P1..P4 = 1 Current sinks are active

VCO (tuner) frequency $f_{VCO} = 8 \times N \times 7.8125$ kHz

Example: $f_{VCO} = 719.25$ MHz

TVSAT = N.C. bit 4 is P1
TVSAT = 0V bit 4 is n 14

Preliminary Data **DIP 8**

The SDA 4212 has been designed for application in television receivers operating according to the frequency synthesis tuning principle. The component includes a preamplifier and an ECL prescaler stage with symmetrical ECL push-pull outputs. It can be operated with a prescaler ratio of 1:64 or 1:256.

The component has been designed for a max. input frequency of 1.2 GHz.

Features:
- Pin programmable prescaler ratio of 1:64 or 1:256
- Symmetrical push-pull input
- Low harmonic wave
- Minimal current consumption of 23 mA

Circuit Description

The preamplifier of the component has been designed with symmetrical push-pull inputs. During the asymmetrical drive of one of the inputs, the other input has to be decoupled to ground by a a capacitor (approx. 1.5 nF) of low series inductance.

The prescaler stage of the component is comprised of several status controlled master slave flipflops. Their prescaler ratio can be set with the switch-over input M as follows:

M to V_S = 1:64
M to ground = 1:256

The symmetrical push-pull outputs of the prescaler include an internal resistor of 500Ω each. The dc voltage level at the outputs is connected to the supply voltage V_S (output "High" = V_S). Typical output deviation is 1.0 V_{pp}.

The harmonic wave in the outputs are very low. The typical output modulation is 0.6 V_{pp}.

Maximum Ratings

Maximum ratings cannot be exceeded without causing irreversible damage to the integrated ciruit.

Pos.	Maximum rating for $T_{amb} = 25°C$	Symbol	min	max	dim	remarks
1	Supply voltage	V_S	−0.3	6	V	
2	Input voltage (pin 2, pin 3)	V_I		2.5	V_{pp}	
3	Output voltage (pin 6, pin 7)	V_Q		V_S	V	
4	Output current (pin 6, pin 7)	$-I_Q$		10	mA	
5	Input voltage (pin 5)	V_M	−0.3	V_S	V	
6	Junction temperature	T_j		125	°C	
7	Storage temperature	T_{stg}	−55	125	°C	
8	Thermal resistance:					
9	system-air	R_{thSA}		180	K/W	mini 8-package
10	system-air	R_{thSA}		115	K/W	DIP 8-package
11	Overload resistance (ESD protection single discharge of 220 pF capacitor through a 1kΩ resistor to each pin)	V_{MOS}	−600	1000	V	not required pins float; pin 4 always to ground

Functional Range

Within the functional range, the integrated circuit operates as described; deviations from the characteristic data are possible.

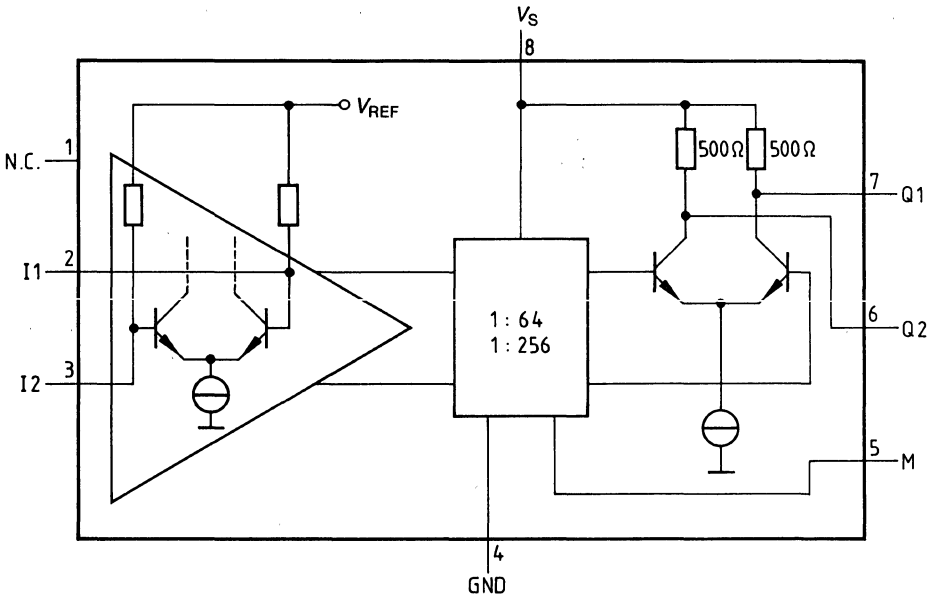
Pos.	Functional range	Symbol	min	max	dim	remarks
1	Supply voltage	V_S	4.5	5.5	V	
2	Input frequency	f	70	1200	MHz	
3	Ambient temperature	T_{amb}	0	80	°C	

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not stated otherwise, typical characteristics will apply at $t_{amb} = 25°C$ and the listed supply voltage.

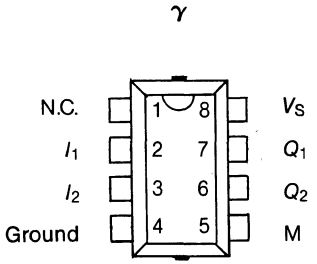
Pos.	Parameter	Symbol	Test conditions	Test circuit	Min	Typ	Max	Dim
	Supply voltage		$V_S = 12V$					
	Ambient temperature		$T_V = 25°C$					
1	Current consumption	I_S	inputs decoupled outputs enabled; M enabled			23.5	29.5	mA
2	Input level ("input sensitivity")	V_I	70 MHz	1	– 26/11		3/315	dBm/mV
			80 MHz	1	– 27/10		3/315	dBm/mV
			120 MHz	1	– 30/7		3/315	dBm/mv
			250 MHz	1	– 32/5.5		3/315	dBm/mV
			600 MHz	1	– 27/10		3/315	dBm/mV
			1000 MHz	1	– 27/10		3/315	dBm/mV
			1100 MHz	1	– 22/18		3/315	dBm/mV
			1200 MHz	1	– 15/40		3/315	dBm/mV
3	Output volt. deviation	V_Q	$C_L \leq 15pF$; $f \leq 1000$ MHz	1	0.4	0.6		V_{pp}
4	DC voltage offset	ΔV_Q		3			100	mV
5	M-input current "Low" (prescaler ratio 1:256)	I_M	M = ground	1		2	100	]A
6	M-input current "High" (prescaler ratio 1:64)	I_M	$M = V_S$	1		0	50	µA
7	M-input voltage "high"	V_{MH}		1	3.0			V
8	M-input voltage "low"	V_{ML}		1			0.2	V
9	Amplitude of the 3rd harmonic at output (referred to 1st harmonic)	A_3	f= 700-900 MHz; $M = V_S$	1.4 2.4		– 30 – 35		dB dB

Block diagram



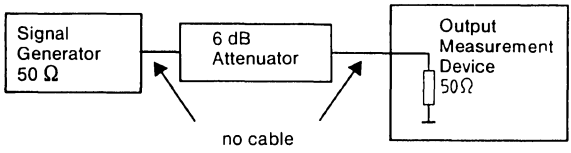
Pin configuration

1	Not connected
2	Input I_1
3	Input I_2
4	Ground
5	Switch-over input M for prescaler ratio
6	Output Q_2
7	Output Q_1
8	Supply voltage V_S

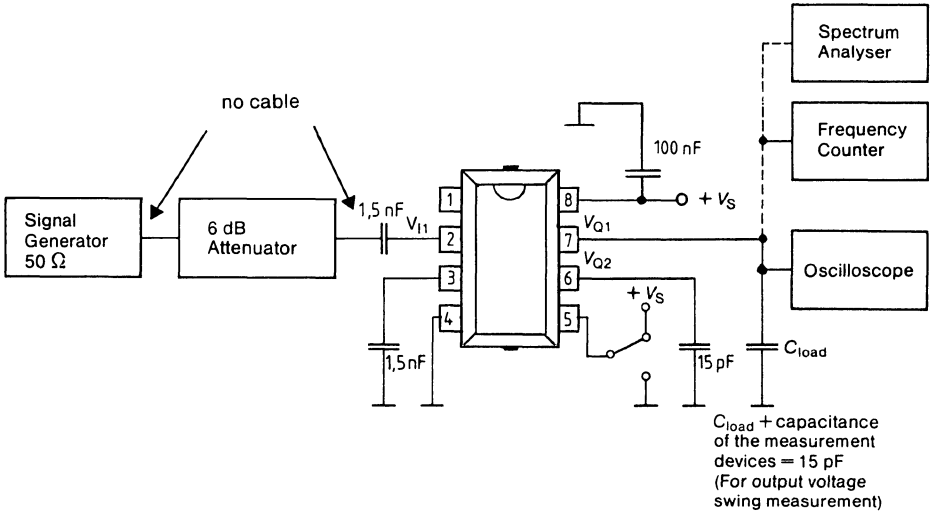


Measurement Circuit 1

Calibration of signal generator

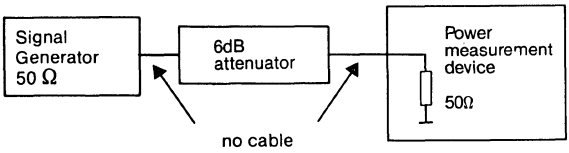


Measurement configuration for input sensitivity and output voltage deviation

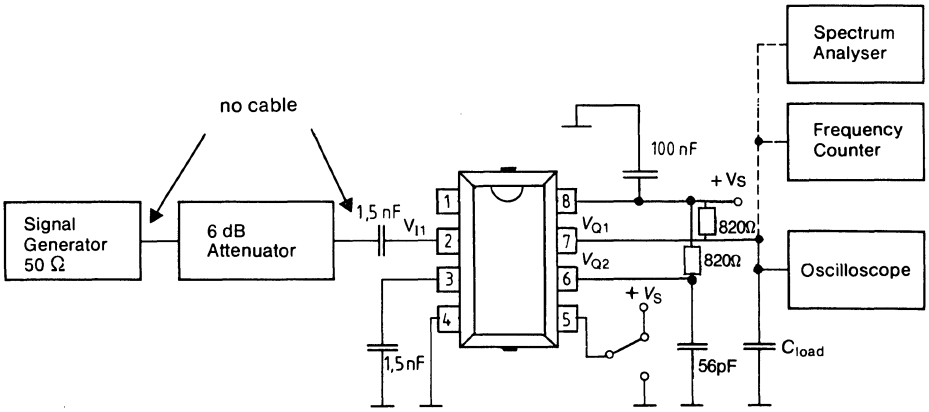


Measurement Circuit 2

Calibration of signal generator



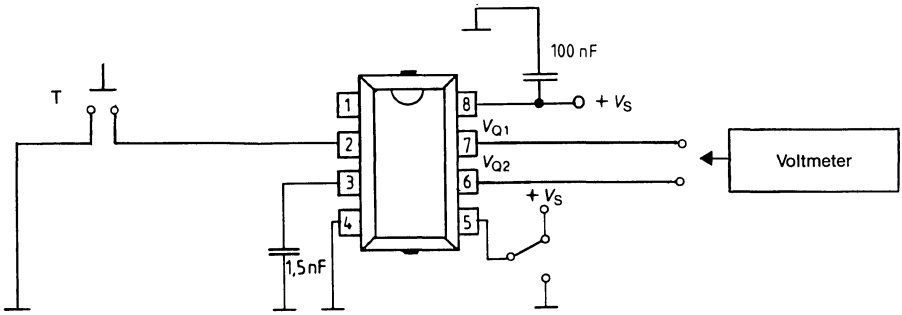
Measurement configuration for input sensitivity and output voltage deviation



C_{load} + capacities of the measurement devices = 56pF (for measurement of the output voltage deviation)

Measurement Circuit 3

DC voltage offset measurement of outputs



Note: press key T until outputs turn over

DIC 16

The SDA 5200 N is an ultrafast A/D converter with 6 bit resolution and overflow output. After cascading, it enables straightforward construction of 7 or 8 bit A/D converters, respecitively (refer to application circuit).

Apart from a guaranteed strobe frequency of 100 MHz and an excellent linearity, the SDA 5200 N is outstanding for a broad analog bandwidth which – from the analog side – enables application up to the limit of the Nyquist theorem.

The SDA 5200 N is pin-compatible to the ICs SDA 5010, SDA 6020, and SDA 5200 S (differing output code in the overflow).

Features

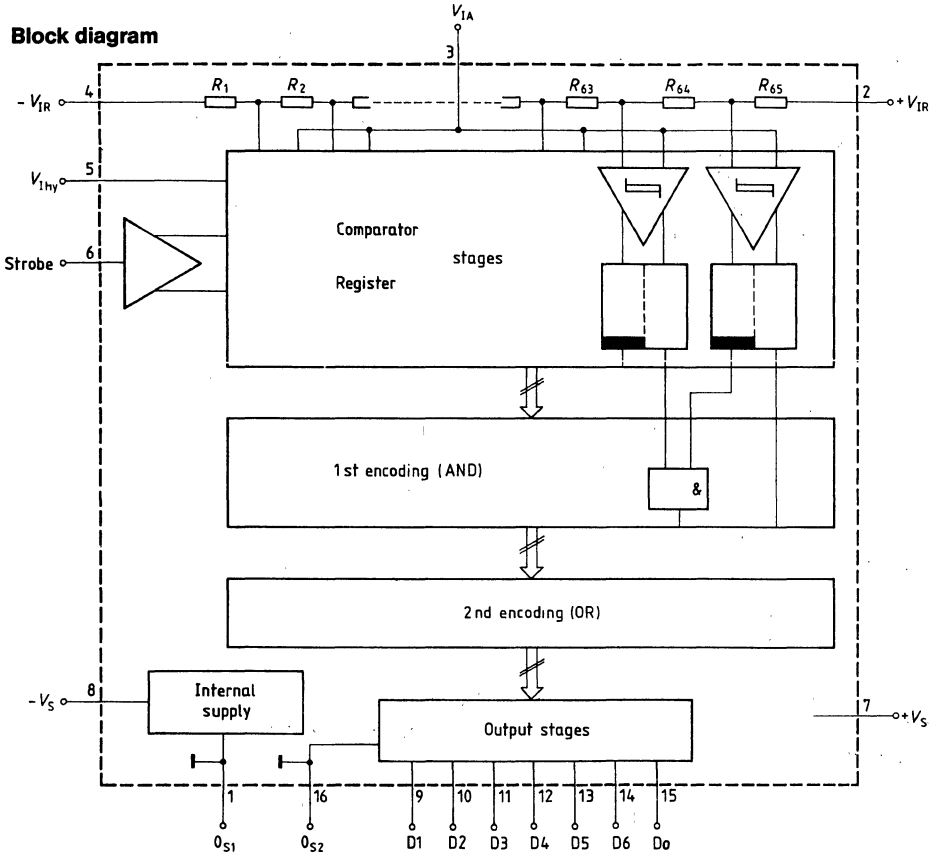
- Strobe frequency 100 MHz
- 6 bit resolution (1.6%)
- Overflow output (7th bit) at simultaneous blocking of the remaining outputs → simple cascading for 7 bit or 8 bit A/D converters
- Broad analog bandwidth (140 MHz)
- High slew rate of the input stages (typ. 0.5 V/ns)
- Processing of analog signals up to the Nyquist limit
- Linearity ± 1/4 LSB
- No sample and hold required
- Dynamic driving of reference inputs for analog addition and multiplication
- Power dissipation 550 mW
- ECL compatible
- Logic-compatible supply voltage +5 V; −5.2 V

The following versions[1] are available upon request:

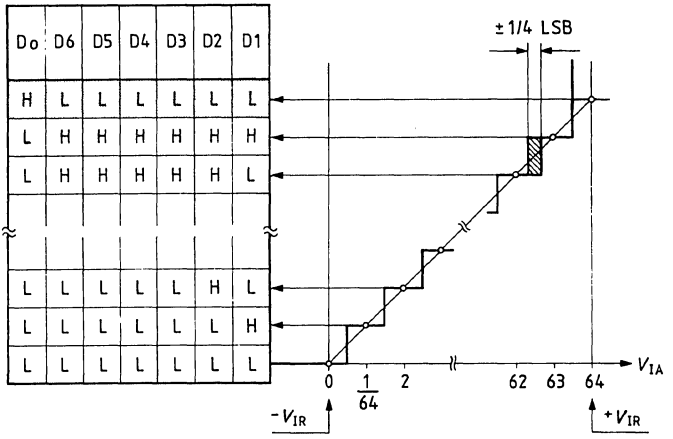
- IC with a nonlinear conversion characteristic of a given characteristic curve
- IC with any output code (e.g. gray code)

1) Conditions upon request.

Block diagram

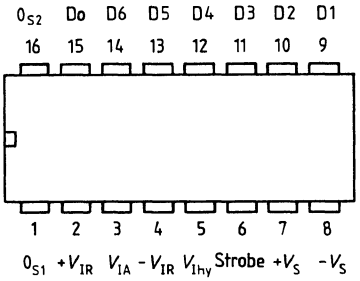


Transfer characteristic and truth table



Pin configuration

top view



Pin	Symbol	Function
1	0_{S1}	Digital ground 1
2	$+V_{IR}$	Positive reference voltage (+2 V)
3	V_{IA}	Analog signal input (max. +2 V; −3 V)
4	$-V_{IR}$	Negative reference voltage (−3 V)
5	V_{Ihy}	Hysteresis control (9 V to +2.5 V)
6	Strobe	Strobe input (ECL)
7	$+V_S$	Positive supply voltage (+5 V)
8	$-V_S$	Negative supply voltage (−5.2 V)
9 to 14	D1 to D6	Data outputs, bits 1 to 6 (ECL)
15	Do	Overflow output
16	0_{S2}	Digital ground 2

Maximum ratings

		Lower limit B	Upper limit A	
Supply voltage	$+V_S$	−0.3	6.0	V
Supply voltage	$-V_S$	−6.0	0.3	V
Input voltages	$V_{IA}, +V_{IR}, -V_{IR}$	−3.5	2.5	V
Strobe	V_{strobe}	$-V_S$	0	V
Hysteresis control	V_{Ihy}	0	3.0	V
Voltage difference	$0_{S1} - 0_{S2}$	−0.5	0.5	V
Ambient temperature	T_A	0	70	°C
Junction temperature	I_j		125	°C
Storage temperature	T_{stg}	−55	125	°C
Thermal resistance System-air	$R_{th\,SA}$		85	K/W

Characteristics

Power supply

		Lower limit B	typ	Upper limit A	
Pos. supply voltage	$+V_S$	4.5	5.0	5.5	V
Neg. supply voltage	$-V_S$	−5.7	−5.2	−4.7	V
Current consumption					
at $+V_S = +5.0$ V, $V_{IA} \leqq -V_{IR}$	I_{S+}		50	80	mA
at $-V_S = -5.2$ V, $V_{IA} \leqq -V_{IR}$	I_{S-}		55	80	mA

Analog section

Signal input

Max. input voltage	V_{IAmax}	$-V_{IRmin}$		$+V_{IRmax}$	V
$V_{IRmax} = \lvert (+V_{IRmax}) - (-V_{IRmin}) \rvert$				5	V
V_{IA} for 6 bit resolution			0.3		V
V_{IA} for 1/2 LSB linearity		1.2	0.6		V
V_{IA} for 1/4 LSB linearity		2.4	1.2		V
Input current					
at $V_{IA} = +V_{IR}$	I_{IA}		150	500	µA
at $V_{IA} < -V_{IR}$	I_{IA}	−500		500	nA
Input capacitance					
at $V_{IA} < -V_{IR}$	C_{IA}		25		pF

Reference inputs

Pos. reference voltage	$+V_{IR}$	−2.5		2	V
Neg. reference voltage	$-V_{IR}$	−3.0		1.5	V
Reference resistance	R_{ref}	96	128	195	Ω

Digital section

Strobe input

H input voltage	V_{IH}	−1.1	−0.9	−0.6	V
L input voltage	V_{IL}	−2.0	−1.7	−1.6	V
H input current	I_{IH}		6	50	µA
L-input current	I_{IL}		6	50	µA

Data outputs (100 Ω to −2 V)

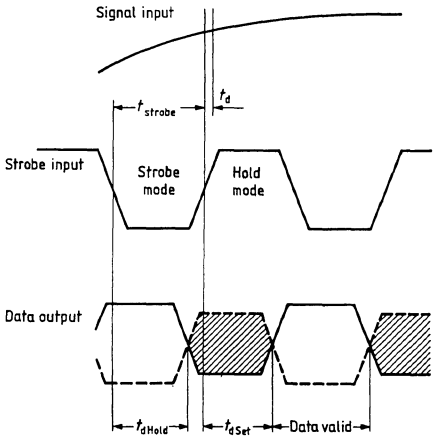
H output voltage	V_{QH}	−1.1	−0.9	−0.7	V
L output voltage	V_{QL}	−2.0	−1.7	−1.5	V

Characteristics (cont'd)

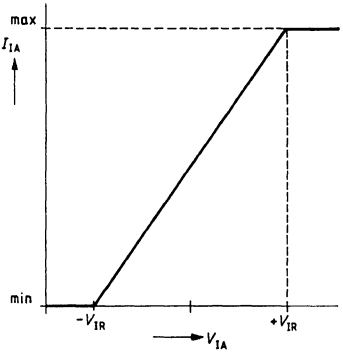
Dynamic parameters

		Lower limit B	typ	Upper limit A	
Aperture time	t_d		2		ns
Aperture jitter			25		ps
Strobe	t_{strobe}		5		ns
Signal transition time	$t_{d\,Hold}$		12	17	ns
Signal transition time	$t_{d\,Set}$		12	17	ns
Strobe frequency	f_{strobe}	100			MHz
Max. slew rate			0.5		V/ns
bandwidth (−3 dB)	B		140		MHz

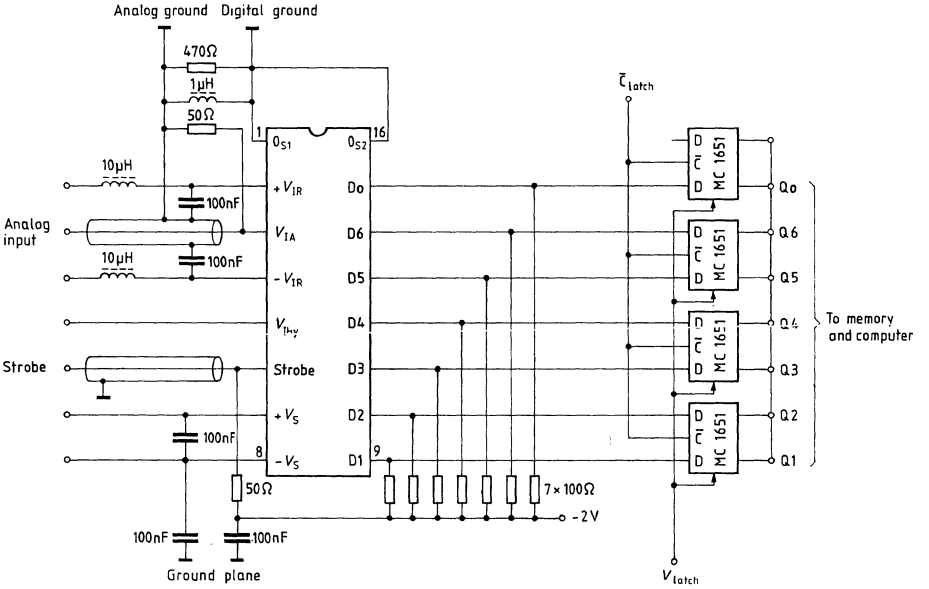
Pulse diagram of strobe input and data outputs



Input current versus input voltage

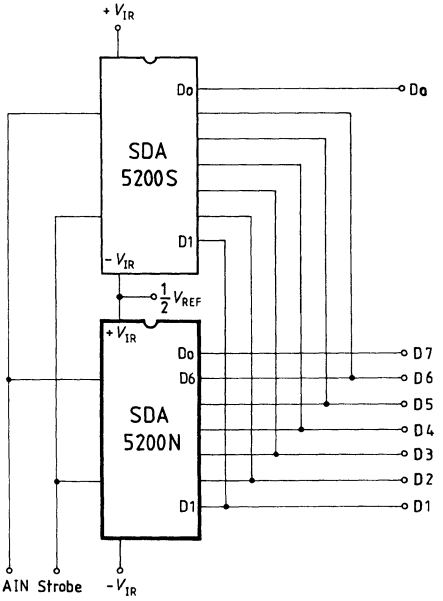


Measurement circuit



Application circuit

7 bit A/D converter with SDA 5200 S and SDA 5200 N



DIC 16

The SDA 5200 S is an ultrafast 6 bit A/D converter with overflow output. It has been designed as terminating device for a 7 bit or 8 bit A/D converter comprising several cascaded ICs (refer to application circuit), or exclusively for 6 bit operation.

Apart from a guaranteed strobe frequency of 100 MHz and an excellent linearity, the SDA 5200 S is outstanding for a broad analog bandwidth which – from the analog side – enables application up to the limit of the Nyquist theorem.

The SDA 5200 S is pin-compatible to the ICs SDA 5010, SDA 6020, and SDA 5200 N (differing output code in the overflow).

Features

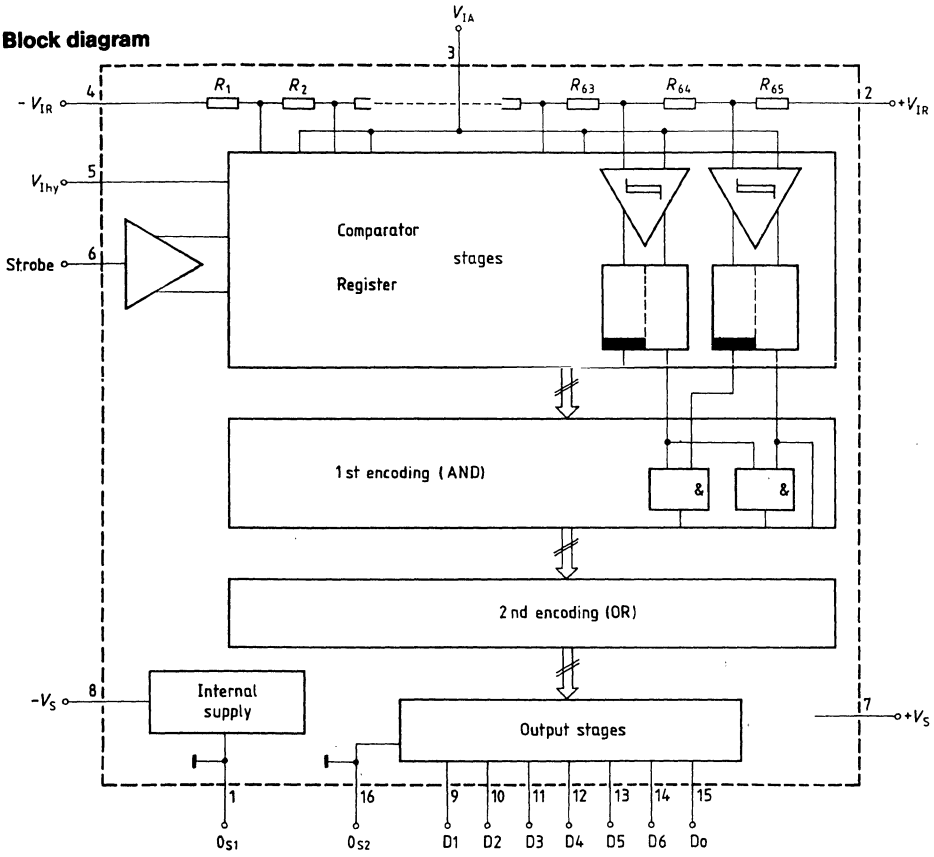
- Strobe frequency 100 MHz
- 6 bit resolution (1.6%)
- Overflow output (7th bit)
- Broad analog bandwidth (140 MHz)
- High slew rate of the input stages (typ. 0.5 V/ns)
- Processing of analog signals up to the Nyquist limit
- Linearity ± 1/4 LSB
- No sample and hold required
- Dynamic driving of reference inputs for analog addition and multiplication
- Power dissipation 550 mW
- ECL compatible
- Logic-compatible supply voltage +5 V; −5.2 V

The following versions[1] are available upon request:

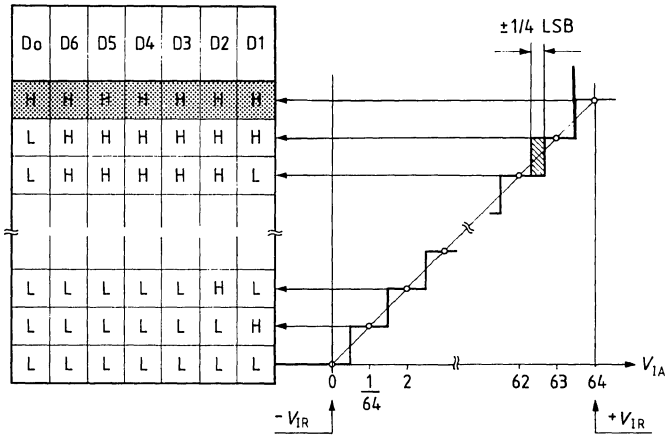
- IC with a nonlinear conversion characteristic of a given characteristic curve
- IC with any output code (e.g. gray code)

1) Conditions upon request.

Block diagram

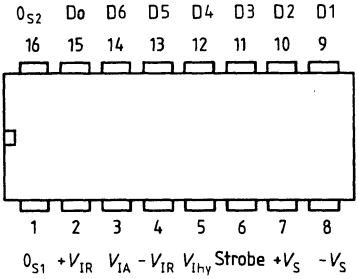


Transfer characteristic and truth table



Pin configuration

top view



Pin	Symbol	Function
1	0_{S1}	Digital ground 1
2	$+V_{IR}$	Positive reference voltage (+2 V)
3	V_{IA}	Analog signal input (max. +2 V; −3 V)
4	$-V_{IR}$	Negative reference voltage (−3 V)
5	V_{Ihy}	Hysteresis control (9 V to +2.5 V)
6	Strobe	Strobe input (ECL)
7	$+V_S$	Positive supply voltage (+5 V)
8	$-V_S$	Negative supply voltage (−5.2 V)
9 to 14	D1 to D6	Data outputs, bits 1 to 6 (ECL)
15	Do	Overflow output
16	0_{S2}	Digital ground 2

Maximum ratings

		Lower limit B	Upper limit A	
Supply voltage	$+V_S$	−0.3	6.0	V
Supply voltage	$-V_S$	−6.0	0.3	V
Input voltages	$V_{IA}, +V_{IR}, -V_{IR}$	−3.5	2.5	V
Strobe	V_{strobe}	$-V_S$	0	V
Hysteresis control	$V_{I\,hy}$	0	3.0	V
Voltage difference	$0_{S1} - 0_{S2}$	−0.5	0.5	V
Ambient temperature	T_A	0	70	°C
Junction temperature	T_j		125	°C
Storage temperature	T_{stg}	−55	125	°C
Thermal resistance System-air	$R_{th\,SA}$		85	K/W

Characteristics

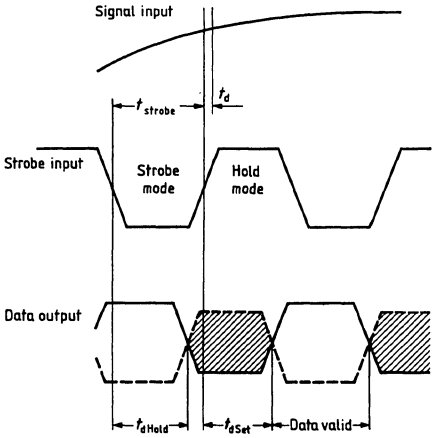
		Lower limit B	typ	Upper limit A	
Power supply					
Pos. supply voltage	$+V_S$	4.5	5.0	5.5	V
Neg. supply voltage	$-V_S$	−5.7	−5.2	−4.7	V
Current consumption					
at $+V_S = +5.0$ V, $V_{IA} \leqq -V_{IR}$	I_{S+}		50	80	mA
at $-V_S = -5.2$ V, $V_{IA} \leqq -V_{IR}$	I_{S-}		55	80	mA
Analog section					
Signal input					
Max. input voltage	$V_{I\,Amax}$	$-V_{I\,Rmin}$		$+V_{I\,Rmax}$	V
$V_{I\,Rmax} = \lvert(+V_{I\,Rmax}) - (-V_{I\,Rmin})\rvert$				5	V
V_{IA} for 6 bit resolution			0.3		V
V_{IA} for 1/2 LSB linearity		1.2	0.6		V
V_{IA} for 1/4 LSB linearity		2.4	1.2		V
Input current					
at $V_{IA} = +V_{IR}$	I_{IA}		150	500	µA
at $V_{IA} < -V_{IR}$	I_{IA}	−500		500	nA
Input capacitance					
at $V_{IA} < -V_{IR}$	C_{IA}		25		pF
Reference inputs					
Pos. reference voltage	$+V_{IR}$	−2.5		2	V
Neg. reference voltage	$-V_{IR}$	−3.0		1.5	V
Reference resistance	R_{ref}	96	128	195	Ω
Digital section					
Strobe input					
H input voltage	V_{IH}	−1.1	−0.9	−0.6	V
L input voltage	V_{IL}	−2.0	−1.7	−1.6	V
H input current	I_{IH}		6	50	µA
L-input current	I_{IL}		6	50	µA
Data outputs (100 Ω to −2 V)					
H output voltage	V_{QH}	−1.1	−0.9	−0.7	V
L output voltage	V_{QL}	−2.0	−1.7	−1.5	V

Characteristics (cont'd)

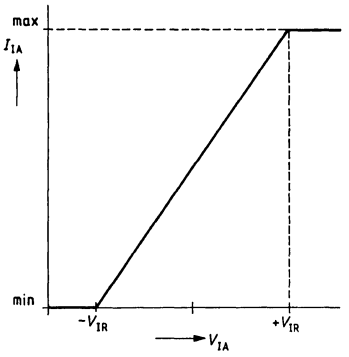
Dynamic parameters

		Lower limit B	typ	Upper limit A	
Aperture time	t_d		2		ns
Aperture jitter			25		ps
Strobe	t_{strobe}		5		ns
Signal transition time	$t_{d\,Hold}$		12	17	ns
Signal transition time	$t_{d\,Set}$		12	17	ns
Strobe frequency	f_{strobe}	100			MHz
Max. slew rate			0.5		V/ns
Bandwidth (−3 dB)	B		140		MHz

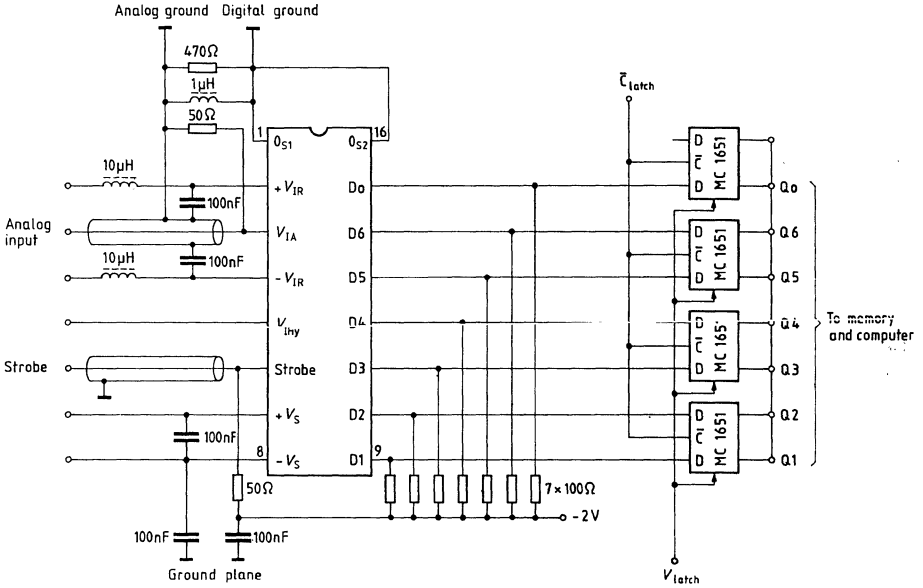
Pulse diagram of strobe input and data outputs



Input current versus input voltage

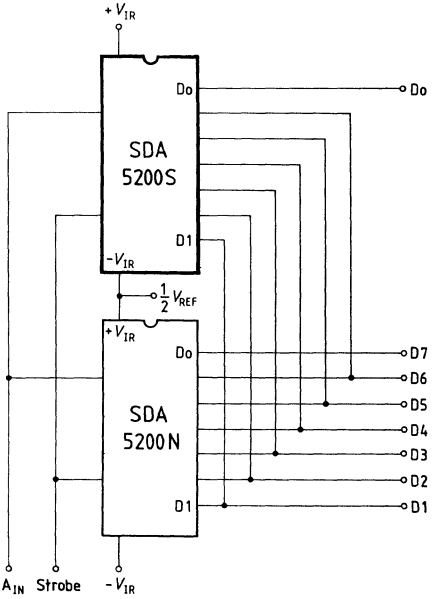


Measurement circuit



Application circuit

7 bit A/D converter with SDA 5200 S and SDA 5200 N



DIC 16

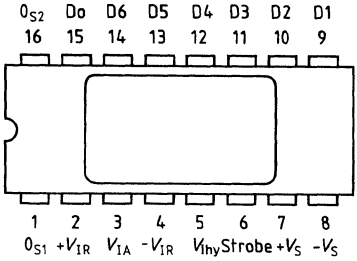
The SDA 6020 is an ultrafast A/D converter with 6 bit resolution. In addition to a scanning frequency of typically 50 MHz and excellent linearity, the SDA 6020 has the following outstanding features:

- 6-bit resolution (1.6%), simple expansion to 8 bits
- ±1/4 LSB linearity
- No sample and hold required
- Dynamic driving of reference inputs for analog addition and multiplication
- ECL compatible (ECL – TTL matching possible, e.g. with SH 100.255)
- Low power dissipation 450 mW
- Logic compatible supply voltage +5 V; –5.2 V

Maximum ratings

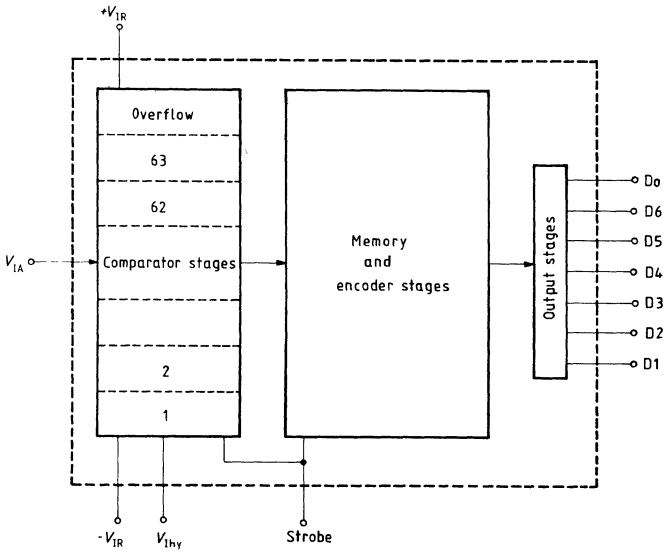
		Lower limit B	Upper limit A	Unit
Supply voltage	$+V_S$	–0.3	6.0	V
Supply voltage	$-V_S$	–6.0	0.3	V
Input voltages	V_{IA}, $+V_{IR}$, $-V_{IR}$	–3.0	3.0	V
Strobe	V_{Strobe}	$-V_S$	0	V
Hysteresis control	V_{IH}	0	3.0	V
Voltage difference	$O_A - O_D$	–0.5	0.5	V
Operating temperature	T_{amb}	0	70	°C
Storage temperature	T_s	–55	125	°C

Pin configuration
top view



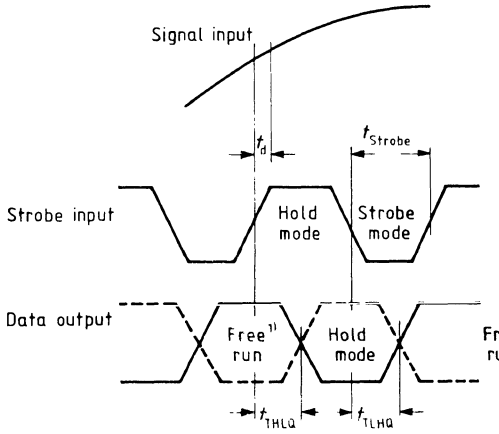
Pin	Symbol	Function
1	0_{S1}	Digital ground
2	$+V_{IR}$	Positive reference voltage (< +2.5 V)
3	V_{IA}	Analog signal input (max. ± 2.5 V)
4	$-V_{IR}$	Negative reference voltage (> −2.5 V)
5	V_{Ihy}	Hysteresis control (0 V to +2.5 V)
6	Strobe	Strobe input (ECL)
7	$+V_S$	Positive supply voltage (+5V)
8	$-V_S$	Negative supply voltage (−5.2 V)
9 to 14	D1 to D6	Data outputs, bits 1 to 6 (ECL)
15	Do	Overflow
16	0_{S2}	Digital ground of output stages

Block diagram



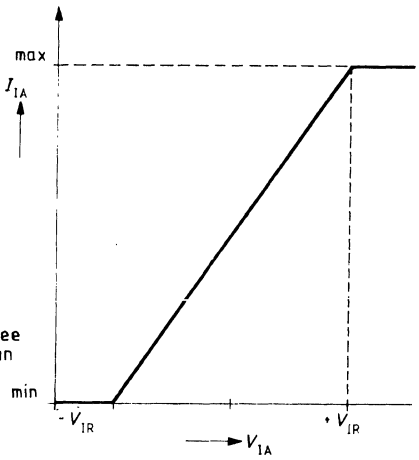
Characteristics		Lower limit B	typ	Upper limit A	
Power supply					
Positive supply voltage	$+V_S$	4.5	5.0	5.5	V
Negative supply voltage	$-V_S$	−5.7	−5.2	−4.7	V
Current consumption					
at $+V_S = +5.0$ V; $V_{IA} \leq -V_{IR}$	I_S		30	60	mA
at $-V_S = -5.2$ V; $V_{IA} \leq -V_{IR}$	I_S		55	80	mA
Analog section					
$T_A = 25$ °C; $+V_S = 5$ V; $-V_S = 5.2$ V					
Signal input					
Maximum input voltage	$V_{IA\,max}$	$-V_{IR\,min}$		$+V_{IR\,max}$	V
$V_{IA\,max} = \lvert (+V_{IR\,max}) - (-V_{IR\,min}) \rvert$				5	V
V_{IA} for 6-bit resolution	V_{IA}		0.3		V
V_{IA} for 1/2 LSB linearity	V_{IA}	1.2	0.6		V
V_{IA} for 1/4 LSB linearity	V_{IA}	2.4	1.2		V
Input current					
at $V_{IA} = +V_{IR}$ in sample mode	I_{IA}		200	800	µA
at $V_{IA} < -V_{IR}$ in sample mode	I_{IA}	−10		10	µA
$-V_{IR} < V_{IA} < +V_{IR}$ in hold mode	I_{IA}	−10		10	µA
Input capacitance					
at $V_{IA} < -V_{IR}$	C_{IA}			35	pF
Reference inputs					
Positive reference voltage	$+V_{IR}$	−2		2.5	V
Negative reference voltage	$-V_{IR}$	−2.5		2	V
Reference resistance	64 R	96	128	256	Ω
Digital section					
Strobe input					
H input voltage	V_{IH}	−1.1	−0.9	−0.6	V
L input voltage	V_{IL}	−2.0	−1.7	−1.5	V
H input current	I_{IH}	5	30	100	µA
L input current	I_{IL}	5	30	100	µA
Data outputs (100 Ω to −2 V)					
H output voltage	V_{QH}	−1.1	−0.9	−0.6	V
L output voltage	V_{QL}	−2.0	−1.7	−1.5	V

Pulse diagram of strobe inputs and data output

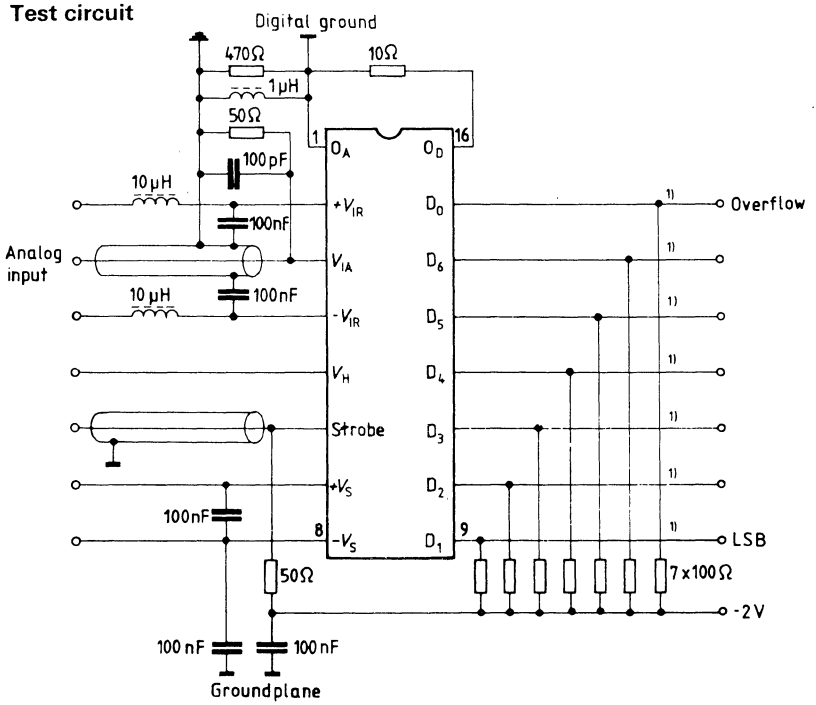


1) undefined output levels

Input current versus input voltage

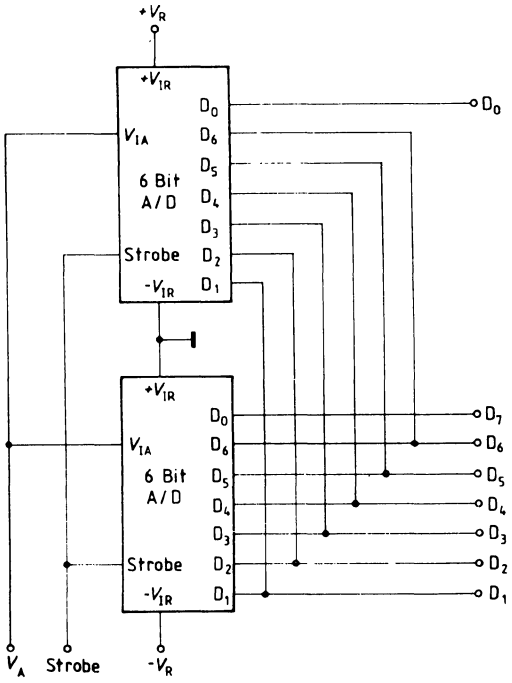


Test circuit

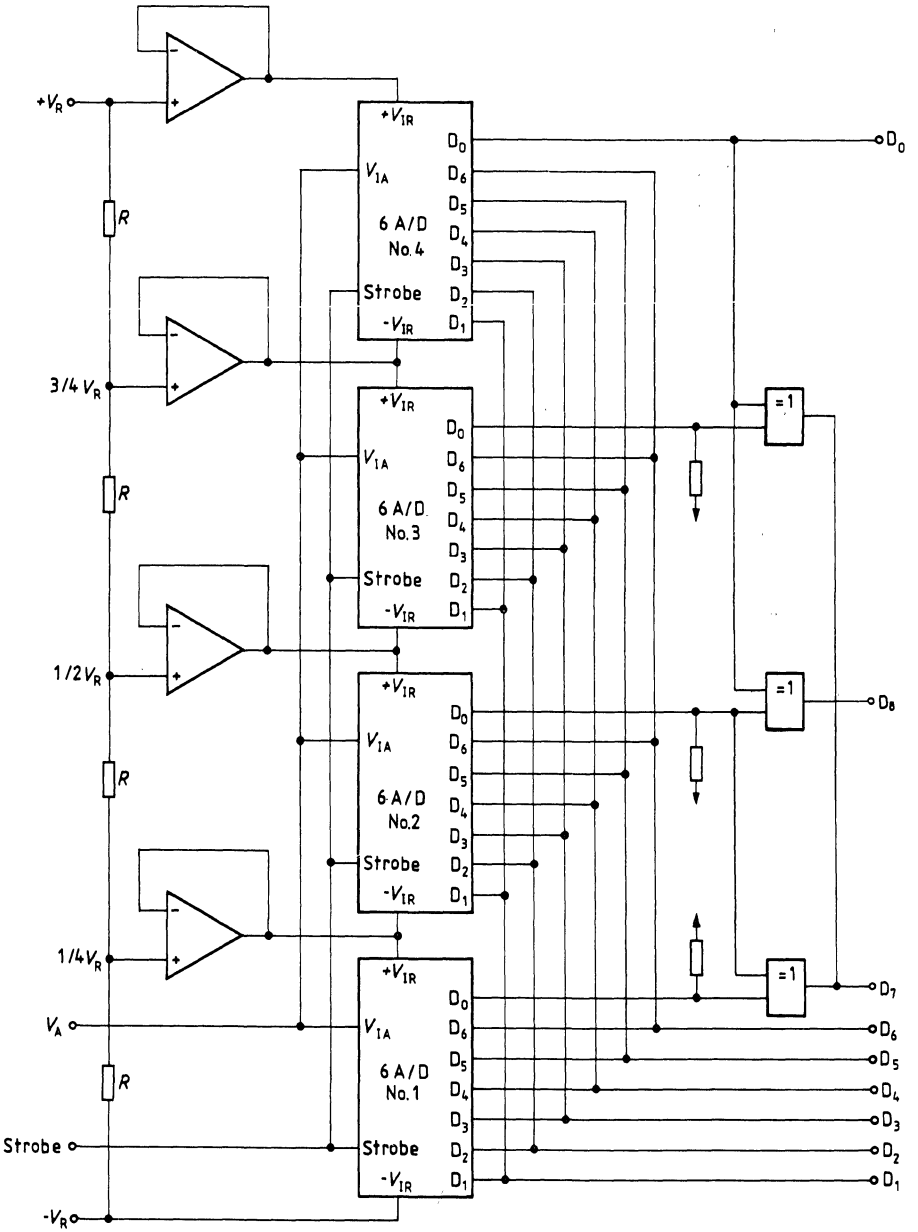


1) Lines effected as Microstrip

Circuit example for expansion to 7 bit



Circuit example for expansion to 8 bit



DIC 16

The SDA 8005 is a high-speed D/A converter with splendid dynamic qualities and offers the following features:

- Settling time typ. 7 ns
- Extremely small glitch area
- Digital input register
- Data inputs 10 K and 100 K ECL-compatible
- Single power supply −5.2 V
- Deglitch control input

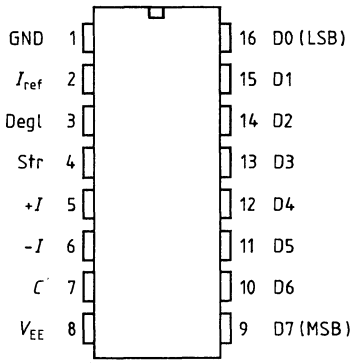
Functional description

The SDA 8005 is a high-speed 8-bit D/A converter with ECL-compatible data and strobe inputs.

The data word is received in the input buffer with the Low active strobe. An external reference voltage source with a reference resistor is needed. At a reference current of 2.5 mA the full-scale output current amounts to 40 mA.

The output glitches can be minimized by adjusting the deglitch input voltage between −2.3 V and −2.9 V. The deglitch input can also be left unwired.

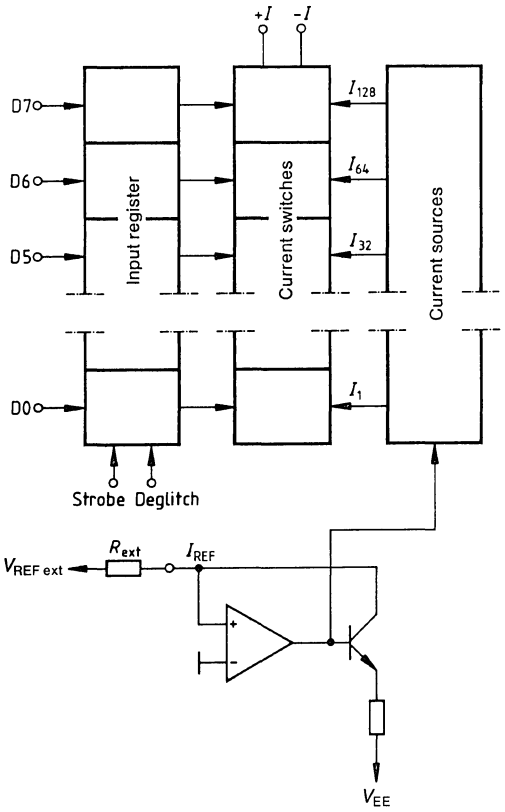
Pin configuration
(top view)



Pin description

Pin	Symbol	Function
1	GND	Ground
2	I_{ref}	Reference current input
3	Degl	Deglitch input
4	Str	Strobe
5, 6	$+I, -I$	Complementary current outputs $+I$: zero current if D0 to D7 are High
7	C	Stabilization
8	V_{EE}	Supply voltage −5.2 V
16 to 9	D0 to D7	Data input 0 (LSB) to 7 (MSB)

Block diagram



Maximum ratings

		Lower limit B	Upper limit A	
Supply voltage	V_{EE}	−6.0	0.3	V
Input voltage	$V_{D0...D7}$	−3.0	0	V
Strobe input voltage	V_{Str}	−4.0	0	V
Deglitch input voltage	V_{Degl}	−5.2	0	V
Output voltages, $+I$, $-I$	V_{QI+}, V_{QI-}	−1.9	5	V
Junction temperature	T_j		125	°C
Ambient temperature	T_A	−25	85	°C
Storage temperature	T_{stg}	−55	125	°C
Thermal resistance	$R_{th\,JA}$		85	K/W

Characteristics

Analog outputs

Static performance

		Lower limit B	typ	Upper limit A	
Ratio of full-scale output current to reference current	I_{QFS}/I_{ref}		16		
Absolute unadjusted error	ERR	−1		+1[2]	%
Integral nonlinearity	*I NL*		0.40[1]	0.55[2]	LSB
Differential nonlinearity	*D NL*		0.6[1]	1[2]	LSB
Full-scale temperature coefficient					
−25 °C to +25 °C	*TC*	80		120	ppm/°C
+25 °C to +85 °C	*TC*	50		80	ppm/°C
Zero-code output current	I_{Q0}		6[1]	30[3]	µA
Full-scale output current	I_{QFS}			40[2]	mA
Output voltage range	V_Q	−1.4		+5	V
Supply voltage sensitivity	S_{VS}		0.03[1]	0.04[2]	%/%

Dynamic performance[1]

Output rise time	t_{rQ}		1.3		ns
Output settling time	t_{sQ}		7		ns
Adjusted worst case glitch area			80		pVs
Digital crosstalk attenuation					
Data	α_{Data}		15[4]		pVs
Strobe	α_{Strobe}		30[4]		pVs

For comments see page 286.

Characteristics		Lower limit B	typ	Upper limit A	
Digital inputs					
DC characteristics					
H input voltage	V_{IH}	−1.105		−0.810	V
L input voltage	V_{IL}	−1.850		−1.505	V
Input capacitance D7	$C_{I\,D7}$		1.2		pF
D6	$C_{I\,D6}$		0.8		pF
D0 to D5	$C_{I\,D0...D5}$		0.5		pF
Strobe	$C_{I\,Str}$		1.5		pF
H input current D7	$I_{IH\,D7}$		25		µA
D6	$I_{IH\,D6}$		12		µA
D0 to D5	$I_{IH\,D0...D5}$		6		µA
Strobe	$I_{IH\,Str}$		75		µA
Input coding			binary		
Switching characteristics					
Setup time	t_{setup}	0.5			ns
Hold time	t_{Hold}	2.5			ns
Strobe time	t_{Str}	2			ns
(see **Fig. 1**)					
Deglitch input					
Deglitch input current at $V_{Degl} = 2.3$ V	I_{IDegl}			200	µA
at $V_{Degl} = 2.9$ V	I_{IDegl}	−150			µA
Deglitch voltage range	$-V_{Degl}$	+2.9		+2.3	V
Deglitch voltage (not connected)	V_{Dgl}		$0.5 \times V_{EE}$		V
Power supply[1]					
Supply voltage	V_{EE}	−5.46		−4.94	V
Supply current	I_{EE}		98	105	mA
Power consumption	P_D		495		mW

For comments see page 286.

Comments

[1]) Measured at: 25 °C
$V_{EE} = -5.2$ V
Full-scale output current $I_Q = 20$ mA
Output load = 50 Ω

[2]) Guaranteed at: −25 °C to +85 °C
−5.46 V to −4.94 V
Full-scale output current $I_Q = 1$ mA to 40 mA

[3]) Measured at 100 °C
Full-scale output current $I_Q = 20$ mA
$V_{Degl} = -2.3$ V
$V_{EE} = -5.2$ V

[4]) $V_{IH} = -0.95$ V
$V_{IL} = -1.6$ V
Input signal rise time $t_r = 3$ ns

Switching all inputs at the same time in the same direction (worst case).

The crosstalk attenuation can be reduced by using other input signals.

Pulse diagram of the inputs

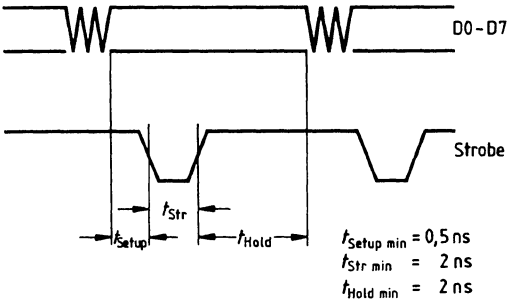


Figure 1

Terminology

Absolute unadjusted error

The full-scale output current with the same reference voltage and reference resistance is different for different chips. The variation results from the deviation of technology parameters. The specification is the maximum deviation from an average value.

Integral nonlinearity

The integral nonlinearity is the maximum deviation of the output of a linear regression from the output values of all possible input codes.

Differential nonlinearity

Differential nonlinearity is the difference between the actual and the ideal deviation between any two adjacent input codes, this being 1 LSB. A specified differential nonlinearity of ± 1 LSB max. over the entire operating temperature range ensures monotonicity.

Supply voltage sensitivity

The supply voltage sensitivity is the dependence of the analog output current on the supply voltage V_{EE} with all other parameters or conditions constant. It is specified in % per %.

Output rise time

The output rise time is the time between the 10% value and the 90% value of V_Q max. at the leading edge.

Output settling time

The output settling time is the time from the 50% point of the trailing strobe edge to the last entry of the analog output signal into an admissible error window of $\pm 1/2$ LSB.

The specified value is measured by using a comparator to detect the entry time point (see **fig. 2**).

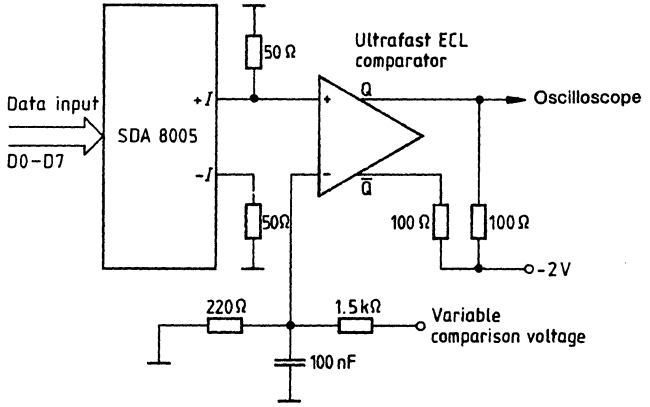
Adjusted worst case glitch area

Glitches which arise from input code switching can be minimized by varying the deglitch input voltage.

The specified value can be measured under the following conditions:

- Input code change from 01111111 to 10000000 and vice versa
- Input data are received with strobe
- Deglitch input voltage is optimized for switching in both directions

Figure 2 shows the test circuit and the timing diagram for the determination of the output settling time.



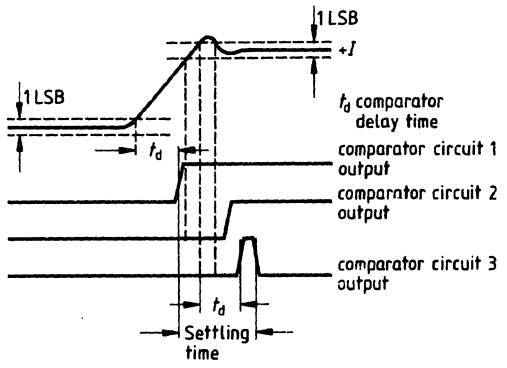


Figure 2

Application instructions

- Board with at least one ground area in its entirety.
- Ground pin should be connected very close to the large ground area by using contact studs or by direct soldering.
- Voltage supply must be blocked directly at the V_{EE} pin by using a 100-nF ceramic capacitor (preferably small chip capacitors).
- The analog outputs should be loaded with 50 Ω as near as possible to the package.
- Each of the DC voltages (V_{EE}, *DEGL*, V_{ref}) has to be checked for its suitability as regards ripple and noise.
- If a D/A output is connected to the 50-Ω input of a scope, an attenuator should be arranged on the D/A converter side of the connecting line to prevent the reflection from the oscilloscope from seeing the practically open line termination (output impedance of D/A converter approx. 20 kΩ); the ground connection between the board and the instrument should have a very low impedance.
- To minimize the crosstalk of used strobe to the output you can place a voltage divider at the strobe input to form an RC filter in combination with the input capacitance (see **figure**).

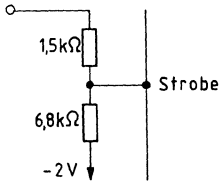


Figure 3 shows an application where the output signal is transmitted over a 50-Ω line to a receiver with a 50-Ω input, possibly a high-speed oscilloscope.

I_{ref} may be adjusted by varying V_{ref} between 0 V and 2.5 V, reference resistor R_{ref} being 1 kΩ.

Alternatively R_{ref} can be changed with V_{ref} constant.

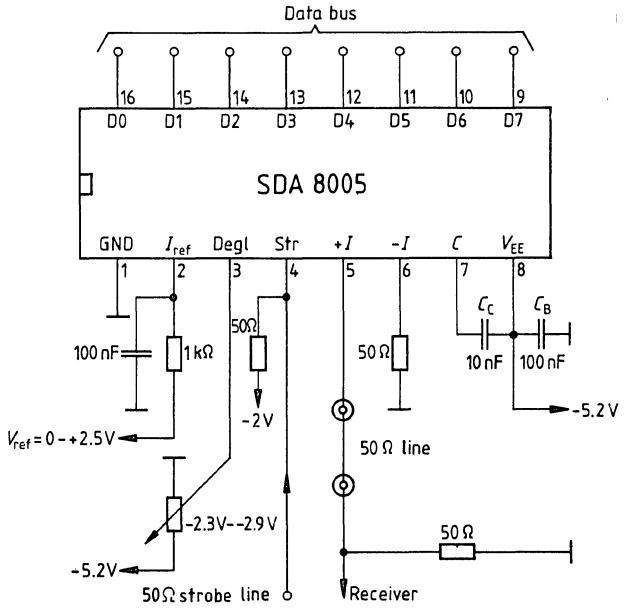


Figure 3

Here the strobe input is connected to a voltage divider, which forms an RC filter together with the input capacitance, and in this way reduces the digital crosstalk from strobe to output. The 100-Ω output line from $+I$ is terminated at both ends.

The high maximum, full-scale output current in this case also allows an acceptable voltage range.

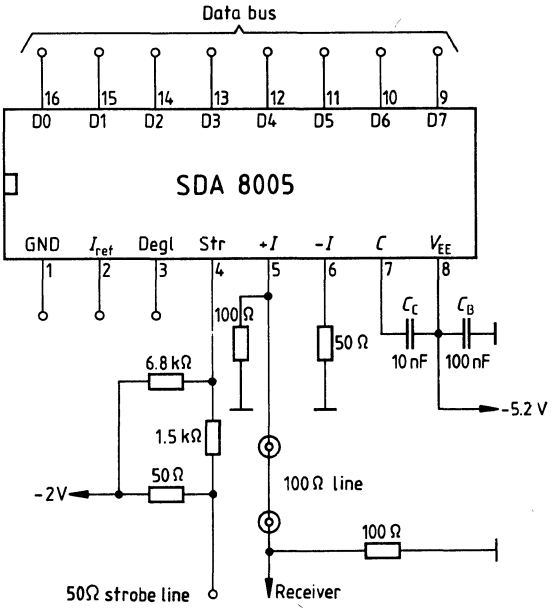


Figure 4

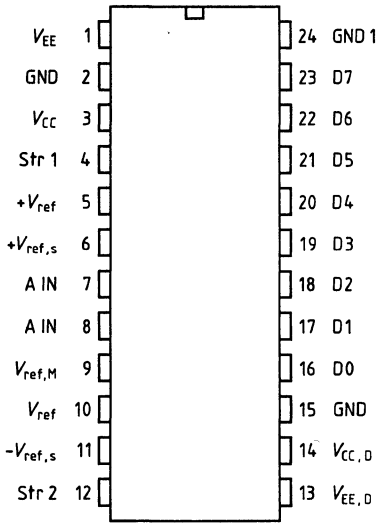
DIC 24

The SDA 8010 is an ultrafast A/D converter according to the parallel principle, with resolution of 8 bits and a guaranteed strobe frequency of 100 MHz. This device, comprising 11,000 components, is produced in state-of-the-art bipolar technology and features wide analog bandwidth, low input capacitance and an input voltage range balanced to ground.

Features

- Strobe frequency 100 MHz
- 8-bit resolution
- Excellent large-signal bandwidth
- High slew rate of input stages
- Balanced input voltage range
- Compatible with ECL 100 K
- Low power dissipation, approx. 1.4 W
- Logic-compatible supply voltage −4.5 V; +5 V

Pin configuration (top view)



Pin description

Pin	Symbol	Function
1	V_{EE}	Neg. supply voltage, analog section
2	GND	Ground
3	V_{CC}	Pos. supply voltage, analog section
4	Str 1	Strobe signal 1
5	$+V_{ref}$	Pos. reference voltage
6	$+V_{ref,s}$	Pos. reference voltage sense
7	A IN	Analog input
8	A IN	Analog input
9	$V_{ref,M}$	Center tap of volgage divider
10	$-V_{ref}$	Neg. reference voltage
11	$-V_{ref,s}$	Neg. reference voltage sense
12	Str 2	Strobe signal 2
13	$V_{EE,D}$	Neg. supply voltage, digital section
14	$V_{CC,D}$	Pos. supply voltage, digital section
15	GND	Ground
16 to 23	D0 to D7	Digital output signals
24	GND 1	Ground connection for output emitter follower

Functional description

The SDA 8010 is an ultrafast A/D converter according to the parallel principle and consists of a field of 255 comparators, three encoding stages and the output drivers (see block diagram).

The analog signal is routed via input A IN in parallel to all comparators and compared with 255 reference voltages spread linearly over the input voltage range. The result of this comparison, delivered in the so-called thermometer code, is converted into binary representation by three encoding stages and is available as a digital signal with ECL level at outputs D0 to D7.

The reference voltages are generated internally by means of a resistance divider. The potentials at its end points are set via the reference voltage inputs $+V_{ref}$ and $-V_{ref}$ and determine the input voltage range, which is resolved with a resolution of 8 bits. Additional potential terminals, $+V_{ref,\ sense}$ and $-V_{ref,\ sense}$, that enable precise adjustment of the input voltage, independently of transfer resistances, according to the principle of a Kelvin connection are provided at the reference voltage inputs. The assignment of the input signal, referred to 1 LSB $= |+V_{ref}| + |-V_{ref}|/256$, to the digital output code is shown in the signal table. As no overflow function is provided, the output signal will remain at a value of 255 after the input voltage range is exceeded.

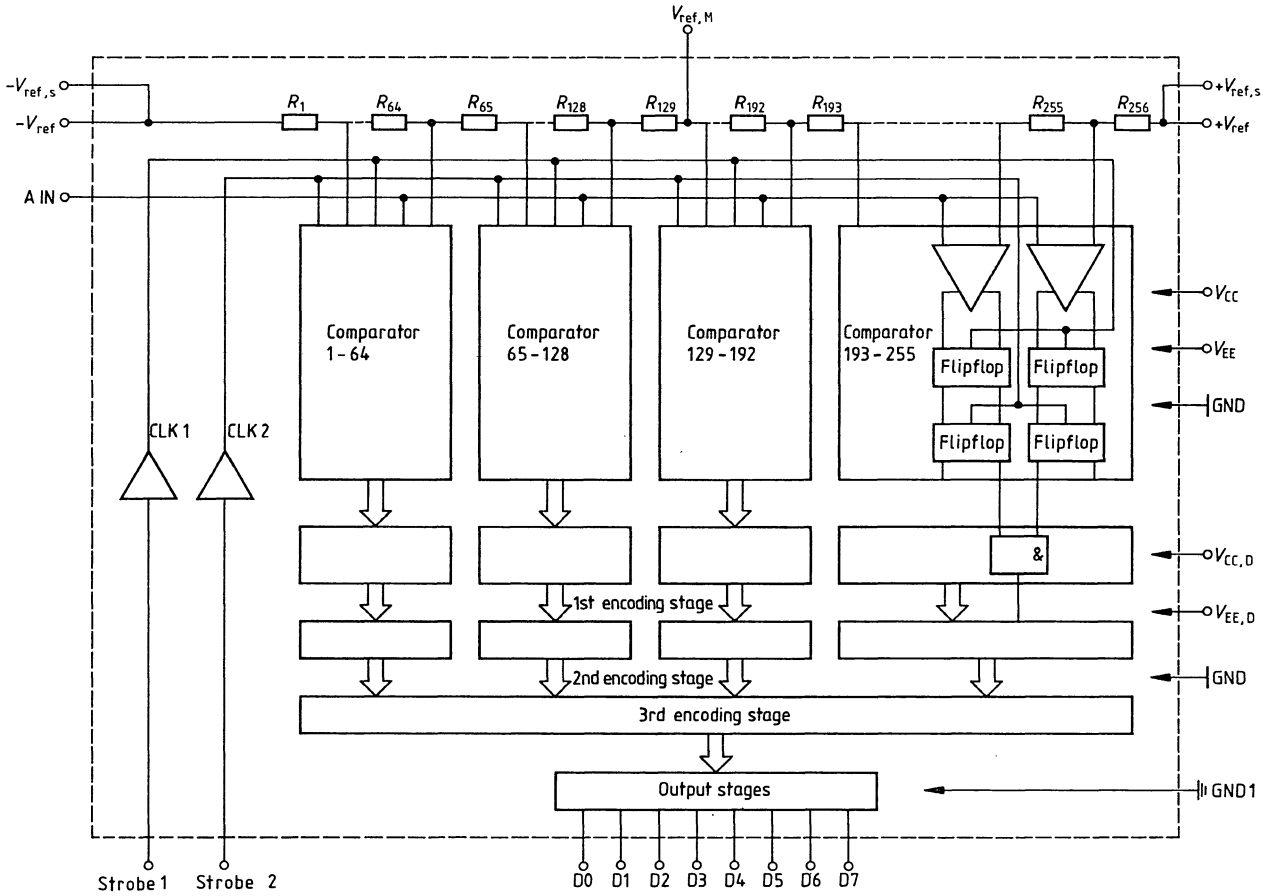
The individual comparators consist of a differential amplifier as the input and a register stage operating in master/slave operation which are activated alternately by strobe signals Str1 and Str2. The sequence of the conversion process is described with reference to the pulse diagram.

During the L phase of signal Str1, the analog signal is compared with the reference voltages. With the rising edge of Str1 the result of the comparison is passed into the first register stage and held there until the falling edge of the strobe. Toward the end of this hold period t_{H1}, the signal is accepted into the second flipflop with the L phase of the second strobe Str2 and stored with the rising edge. After a delay period t_d this data appears at the output.

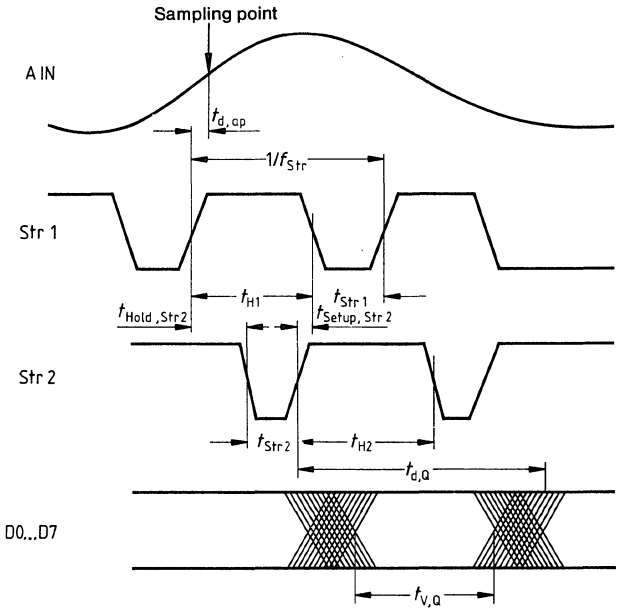
The validity range $t_{V,\ Q}$ of the output data depends on the duty cycle set at Str2. In general, data will also appear outside this interval $t_{V,\ Q}$. The second comparator latch is transparent in this phase, however, so transients of the first stage could reach the output for especially critical settings.

What is essential for the analog features is that the input differential amplifier of the comparators be currentless at no time during the strobe process so that, on the one hand, coupling of the strobe on to the input is prevented and, on the other hand, excellent large-signal bandwidths are achieved. The low input capacitance of 30 pF and the symmetrical input voltage range in many cases permit operation of the converter in 50-Ω systems. The dual design of the analog input A IN assures a low inductance lead and thus also contributes to achieving a flat frequency response up to 50 MHz.

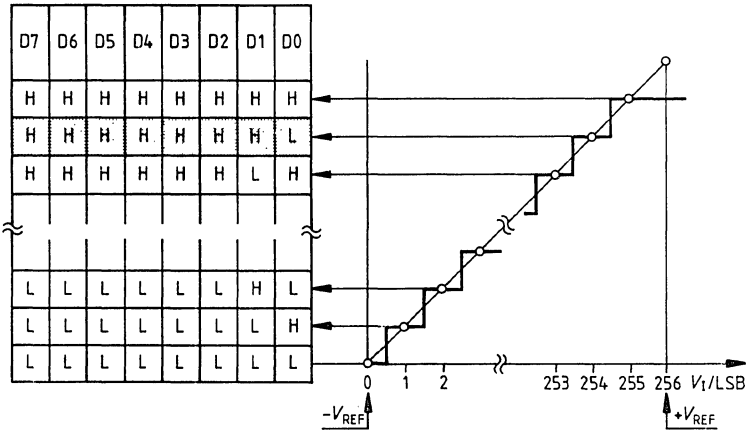
Connection $V_{ref,\ M}$ serves for RF decoupling the reference voltage divider. The use of two supply systems V_{CC}, V_{EE} and $V_{CC,\ D}$, $V_{EE,\ D}$ and an additional ground lead GND 1 for the output stages reduces the mutual influence of analog and digital signals to a minimum. Additionally, the separate return of the analog signal ground lead, the so-called analog ground, is recommended (see test circuit).


$V_{ref,M}$
$-V_{ref,s}$
$-V_{ref}$
A IN
R_1
R_{64}
R_{65}
R_{128}
R_{129}
R_{192}
R_{193}
R_{255}
R_{256}
$+V_{ref,s}$
$+V_{ref}$
Comparator 1 - 64
Comparator 65 - 128
Comparator 129 - 192
Comparator 193 - 255
Flipflop
Flipflop
Flipflop
Flipflop
V_{CC}
V_{EE}
GND
CLK 1
CLK 2
&
$V_{CC,D}$
$V_{EE,D}$
GND
1st encoding stage
2nd encoding stage
3rd encoding stage
Output stages
GND 1
Strobe 1
Strobe 2
D0
D1
D2
D3
D4
D5
D6
D7

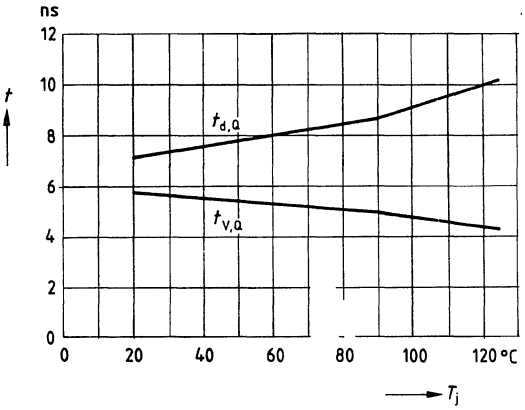
Pulse diagram



Transfer characteristic and truth table



Typical dependency of $t_{d,Q}$ and $t_{V,Q}$ on junction temperature T_j



Maximum ratings

		Lower limit B	Upper limit A	
Pos. supply voltages	V_{CC}, $V_{CC,D}$	−0.3	6.0	V
Neg. supply voltages	V_{EE}, $V_{EE,D}$	−6.0	0.3	V
Analog input voltages[1]	$+V_{ref}$, $-V_{ref}$	−2.5	1.5	V
	$V_{A\,IN}$			
Digital input voltages	$V_{Str\,1}$, $V_{Str\,2}$	−3.5	0	V
Junction temperature	T_j		125	°C
Thermal resistance				
Junction-air (without dissipator)	$R_{th\,JA}$		50	K/W

Characteristics

$4.75 < V_{CC} = V_{CC,D} < 5.25$ V
-4.75 V $< V_{EE} = V_{EE,D} < -4.25$ V
$T_j = 20$ to 125 °C

		Lower limit B	typ	Upper limit A	
Current consumption					
Pos. supply current	$I_{CC} + I_{CC,D}$		180	200	mA
Neg. supply current	$I_{EE} + I_{EE,D}$		90	100	mA
Reference inputs					
Pos. reference voltage	$+V_{ref}$	−1		1	V
Neg. reference voltage	$-V_{ref}$	−2		0	V
Reference resistance	$256\,R$		130		Ω
Signal input					
Voltage range	V	−2		1	V
Input current[2]	I_I		400	600	µA
Input capacitance	C_I		30		pF

For comments see page 302.

Characteristics		Lower limit B	typ	Upper limit A	
Strobe inputs					
H input voltage	V_{IH}	−1.165			V
L input voltage	V_{IL}			−1.475	V
Max. strobe frequency	$f_{Str,\,max}$	100			MHz
Strobe time 1[3]	$t_{Str\,1}$	3.5	5	6.5	ns
Strobe time 2[3]	$t_{Str\,2}$	4.0[4]	3.5	4.5	ns
Setup time Strobe 2[3]	$t_{Setup,\,Str\,2}$	0	−1.5	−2.5	ns
Hold time Strobe 2[3]	$t_{Hold,\,Str\,2}$	1	3		ns
Aperture delay[5]	$t_{d,\,ap}$		3		ns
Data outputs					
H output voltage	V_{QH}	−1.025			V
L output voltage	V_{QL}			−1.620	V
Signal transition time[6]	$t_{d,\,Q}$	7		10.5	ns
Time of valid output data[7]	$t_{V,\,Q}$	4			ns
Conversion characteristics					
Static nonlinearity[8]					
Integral nonlinearity	I NL			0.5	LSB
Differential nonlinearity	D NL		0.5		LSB
Dynamic performance[9]					
Large signal bandwidth[10]	$f_{3\,dB}$	80			MHz
Signal-to-noise ratio[11]					
f_{an} = 30 MHz	*SNR*	40			dB
45 MHz	*SNR*		33		dB
Total harmonic distortion[12]					
f_{an} = 30 MHz	*THD* 2		−35		dB
	THD 3		−38		dB

For comments see pages 302, 303.

Comments

1) $+V_{ref}$ always have to be more positive than $-V_{ref}$.

2) The input current is linearly dependent on the input voltage. The stated value represents the input current at $V_{A\,IN} = +V_{ref}$.

3) The timing of the two externally applied controlling signals Str1 and Str2 are defined by

$t_{Str\,1}$ — L-period of Str 1
$t_{Str\,2}$ — L-period of Str 2
$t_{Setup,\,Str\,2}$ — time interval from rising edge of Str 2 to falling edge of Str 1
$t_{Hold,\,Str\,2}$ — time interval from rising edge of Str 1 to falling edge of Str 2

4) This value applies to $T_j = 125\,°C$, at room temperature the minimum of strobe width $t_{Str\,2}$ is 3 ns.

5) Delay of the sampling moment (latching of first comparator stage) with respect to the positive transition of signal Str 1; it is caused by the internal strobe amplifiers.

6) Delay from the rising edge of Str 2 to the begin of validity of the associated output data.

7) Time interval, during that the conversion of a 30 MHz/2 V_{pp} signal at 100 MHz sampling rate yields an *SNR* of greater than 40 dB.

8) Deviation of the actual transfer characteristic (output code as a function of input voltage) from that of an ideal ADC. It is expressed in terms of the measured transition voltages V_i (input voltage, at which the output code transition (i − 1) → i occurs):

Integral nonlinearity *I NL* — maximum deviation of the mean input voltage associated with any output code from the ideal value (in LSB), so

$$I\,NL = \max\left(\frac{V_i + V_{i+1}}{2} - (-V_{ref})\right) \cdot \frac{256}{+V_{ref} - (-V_{ref})} - i$$

Differential nonlinearity *D NL* — maximum deviation of the input voltage range associated with any output code from the ideal value (in LSB), so

$$D\,NL = \max\,(V_{i+1} - V_i) \cdot \frac{256}{+V_{ref} - (-V_{ref})} - 1$$

Given values of *INL* and *DNL* are related to a reference voltage range $(+V_{ref} - (-V_{ref}))$ of 1.8 V.

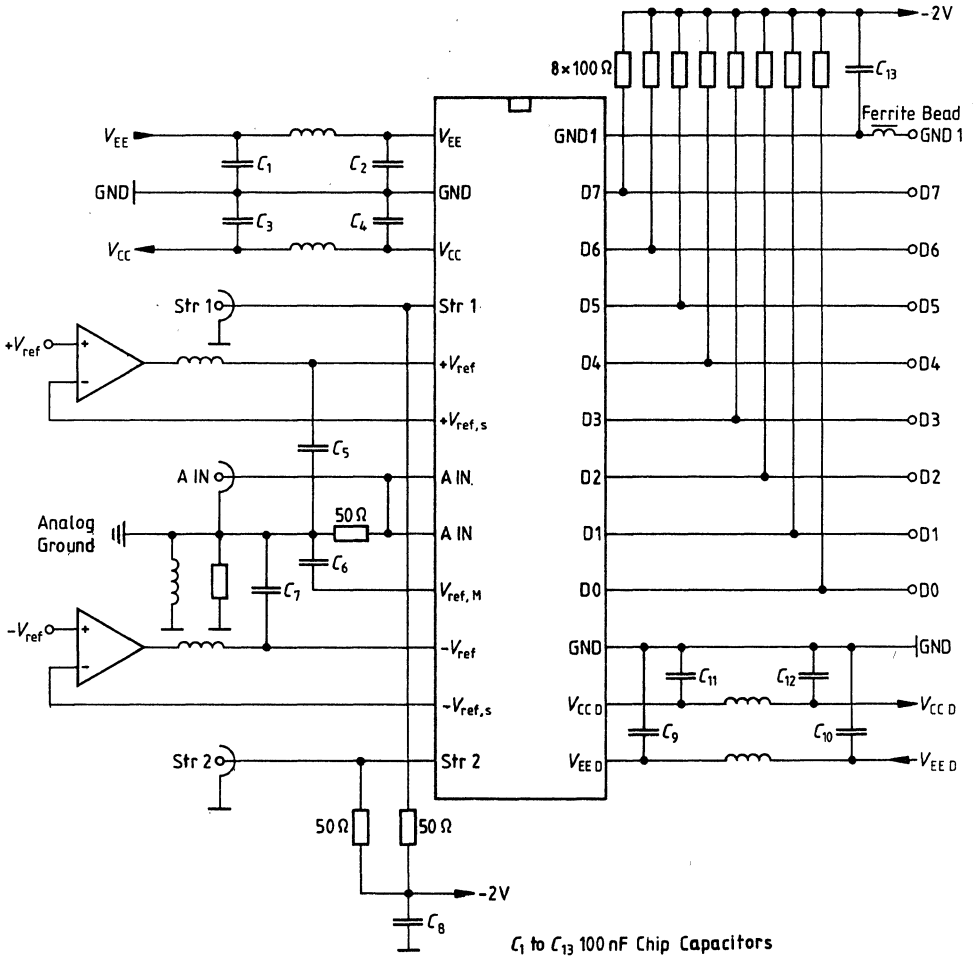
[9]) All parameters are measured at $f_{Str} = 100$ MHz

[10]) That frequency of a sinusoidal input signal of (peak-to-peak) 2 V, at which the amplitude of the signal derived from digital output data has decreased by 3 dB compared to the low-frequency value. The measurement is carried out at a sampling rate of 100 MHz in a 50 Ω system. As this impedance together with the input capacitance forms the main limitation, bandwidth could be further increased by driving the input from a low-impedance source.

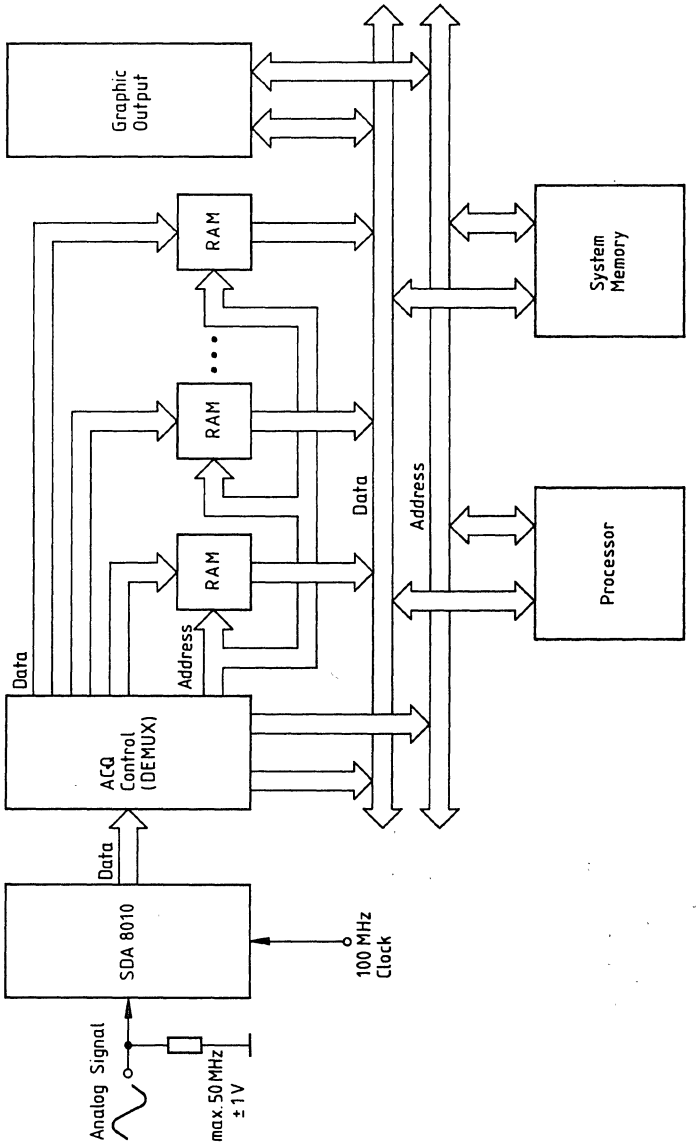
[11]) Energy ratio (in dB) of the fundamental to the sum of all other spectral components (except second and third harmonics) in the spectrum of the quantized representation resulting from the conversion of a peak-to-peak 2 V input sine wave at 100 MHz sampling rate.

[12]) Energy ratio of second (THD2) and third (THD3) order harmonics to the fundamental spectral component (see *SNR*).

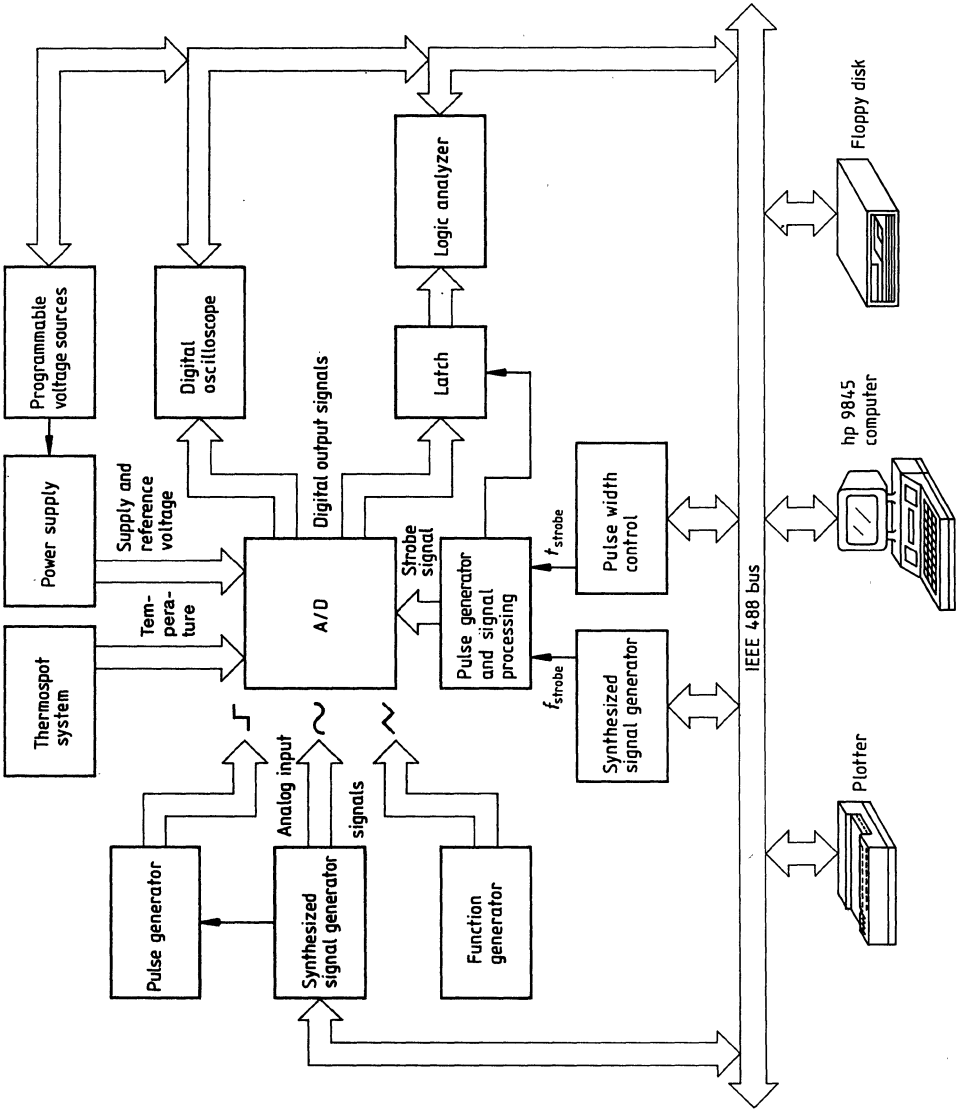
Measurement circuit



Application example



Computer-supported test setup



Preliminary Data

Type	Function	Package
SLE 5001	Transmitter	DIP 40
SLE 5001 K	Transmitter	Mikropack
SLE 5001 W	Transmitter	PLCC 44
SLE 5002	Receiver	DIP 40
SLE 5002 K	Receiver	Mikropack
SLE 5002 W	Receiver	PLCC 44
TDE 4060	Pre-amplifier	DIP 8
TDE 4060 G	Pre-amplifier	SO 8
TDE 4061	Pre-amplifier with Demodulator	DIP 14
TDE 4061 G	Preamplifier with Demodulator	SO 14

The CMOS components SLE 5001 and SLE 5002 have been designed as transmitter and receiver for an electronic remote-control system. The system offers over and above the usual characteristics, an almost unlimited number of channels.

Since both transmitter and receiver are available in Micropack, the smallest possible dimensions are attainable. The data from the transmitter to the receiver can be sent by the following means, according to the peripheral hardware:
- Infrared (cost effective)
- Galvanic connection (wire)
- Inductive coupling (Transformer principle)
- Radio
- Ultrasound

If infrared is chosen the IR-Pre-amplifier TDA 4060/TDE 4061 will be an important component to be considered.

Main System Characteristics
- 9.7 million different channels available
- CMOS technology
- Micropack housing
- Dynamic or static receiver operating-mode
- Minimum external component count
- High interference and operational reliability
- Power-on reset
- Standby operation/Wake up mode

Transmitter SLE 5001: (Fig. 2)
The SLE 5001 is a mask-encoded CMOS component.

On applying the operating voltage a power-on-reset occurs, and the transmitter enters stand-by operation. The instructions, entered by means of a push-button matrix, are converted into a 4-byte long impulse diagram and sent out via the output stage. The component requires a matrix to be provided with 10 row connections (P27 to P36) and 4 columns (P21 to P24).

Entering of an instruction is by means of a push-button which connects a row input with a column input. Pressure on the key activates the oscillator and the corresponding impulse message is sent out.

A 20 msec. software controlled key debounce is contained in the program. After a brief touch of the key the component delivers the corresponding codeword to the IR output stage.

In Fig. 1 the timing principle of the IR data transmission is shown.

An IR channel message consists of 4 bytes (of 8 bits each). In front of each byte a synchronising pulse is sent. Following each transmitted byte there is a pause, during which the newly received byte can be stored (1.5 msec.). The total IR transmission is 36 bits. [(1 + 8) − 4].

Each databit is modulated by a carrier frequency (125 kHz) and sent out as an infrared light pulse by means of an IRED (SFH 484). A databit consists of 12 IR pulses each of 2.4 μs duration, and with a peak current value of about 2A. The beginning of the next bit to be transmitted is at least 1.5 ms. later. There is therefore a maximum average transmission current of about 38 mA (12 • 2.5 μs / 1500 μs) • 2000 mA. During a logic bit "0" there is no output. In the worst possible case (all bits "1") a data word of 4 bytes will require a battery capacity of 2 mAs (12 • 2.4 μs • 200 mA • 36).

Fig. 3b: IR pre-amplifier

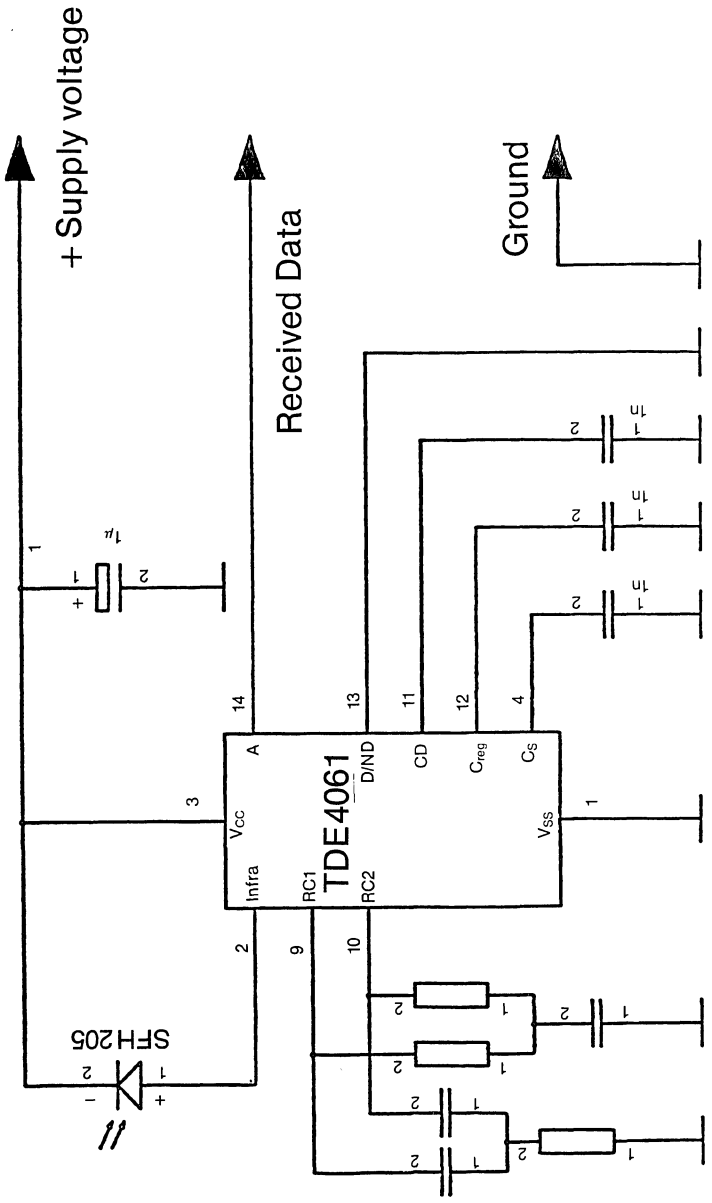


Fig. 3c: IR pre-amplifier with separate Demodulator

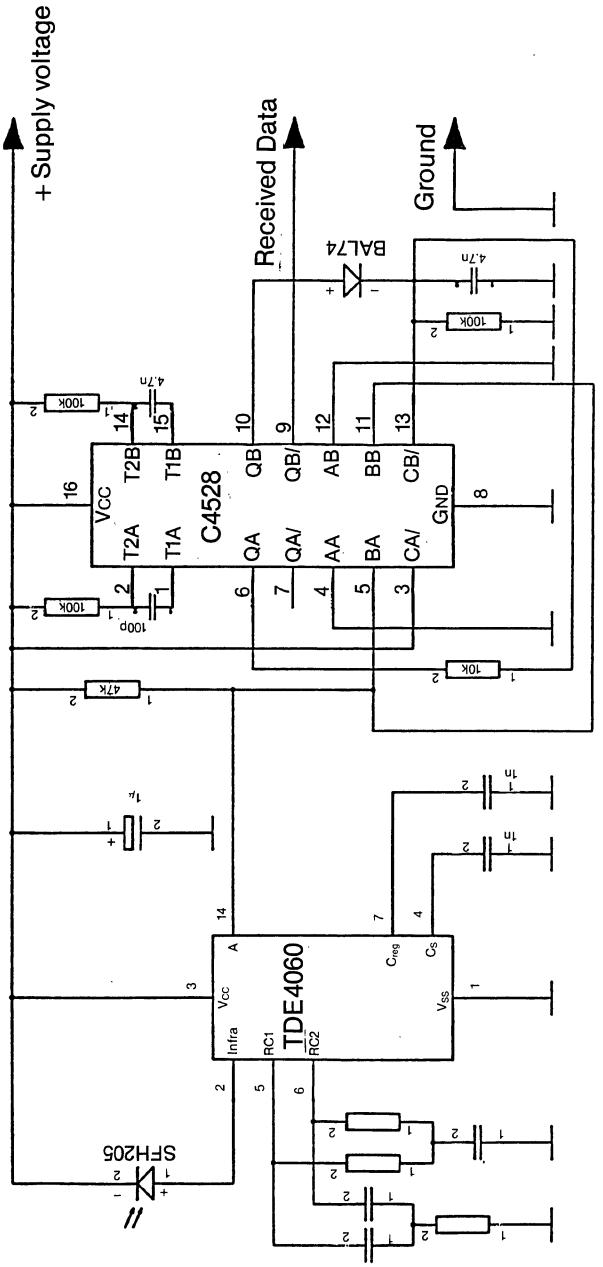
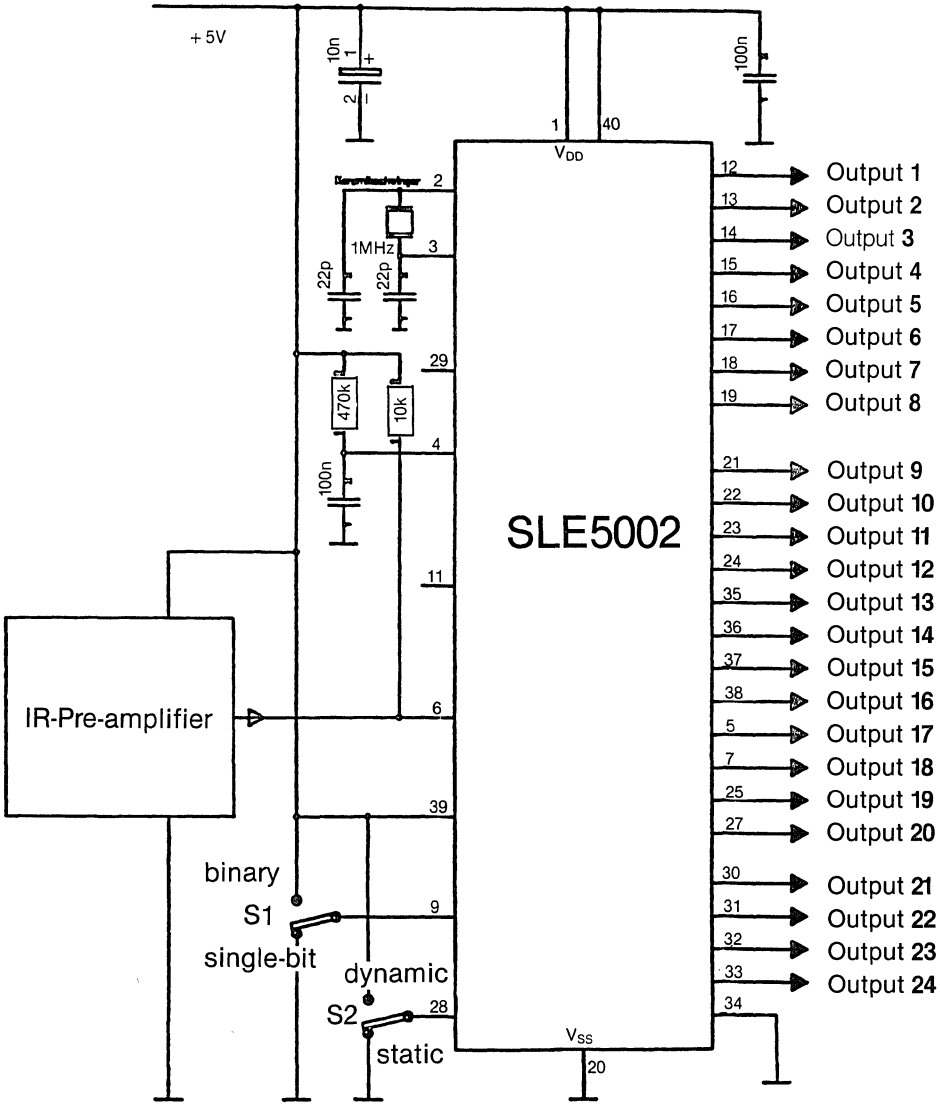


Fig. 4: Application of remote-control receiver with IR data transmission



DIP 14

The symmetrical 8-stage amplifier with symmetrical coincidence demodulator for amplifying, limiting, and demodulating frequency-modulated signals is especially suited for the sound IF section in TV sets and FM IF amplifiers in radio sets.

Features

- Outstanding limiting characteristics
- Wide range of operation (6 to 18 V)
- Few external components
- Voltage for AFC

Maximum ratings

Supply voltage[1])	V_S	18	V
Z current	I_{12}	15	mA
$t \leqq 1$ min	I_{12}	20	mA
Voltage	V_5	4	V
Current	I_3	5	mA
	I_4	2	mA
Storage temperature range	T_{stg}	−40 to 125	°C
Junction temperature	T_j	150	°C
Thermal resistance (system-air)	$R_{th\,SA}$	90	K/W

Operating range

Supply voltage range	V_S	6 to 18	V
Ambient temperature range	T_{amb}	−15 to 70	°C
Frequency range	f	0 to 12	MHz

1) The IC is not allowed to be plugged in or out when the supply voltage is switched on.

Characteristics (T_{amb} = 25 °C, V_S = 12 V; f_{IF} = 5.5 MHz or 10.7 MHz, respectively)

		min	typ	max	
Current consumption $R_5 = \infty$	I_S	10	14	18	mA
$R_5 = 0$	I_S	11	15.2	20	mA
IF voltage gain	G_V		68		dB
IF output voltage at limiting (each output)	$V_{q\,pp}$	170	250		mV
Output resistance (pin 8)	R_{q8}	1.9	2.6	3.3	kΩ
Bridging resistance	$R_{13\text{-}14}$			1	kΩ
AGC range of volume control	$\frac{V_{AF\,max}}{V_{AF\,min}}$	70	75		dB
DC level of output signal	V_8	6.2	7.4	8.5	V
Potentiometer resistance					
− 1 dB attenuation	R_5		3.7	4.7	kΩ
− 70 dB attenuation	R_5	1.0	1.4		kΩ
Voltage					
− 1 dB attenuation	V_5		2.4		V
− 70 dB attenuation	V_5		1.3		V
Signal-to-noise ratio (V_i = 10 mV, Δf = ± 50 kHz)	$a_{S/N}$	75	85		dB
Total harmonic distortion (V_i = 10 mV, Δf = ± 25 kHz)	THD		1.3	2.5	%
Noise voltage (in accordance with DIN 45405)	V_n		80	140	µV
Output resistance	$R_{q\,7\text{-}9}$		5.4		kΩ

Characteristics for f_{IF} = 5.5 MHz (T_{amb} = 25 °C, V_S = 12 V, f_{IF} = 5.5 MHz, Δf = ± 50 kHz, f_{mod} = 1 kHz, Q_B approx. 45)

AF output voltage (V_i = 10 mV)	$V_{AF\,rms}$	0.7	1		V
Input voltage for limiting	$V_{i\,lim}$		30	60	µV
AM suppression V_i = 500 µV, m = 30%	a_{AM}	45	55		dB
V_i = 10 mV, m = 30%	a_{AM}	60	68		dB
Input impedance	Z_i		40/4.5		kΩ/pF

Characteristics for 10.7 MHz (T_{amb} = 25 °C, V_S = 12, V, f_{IF} = 10.7 MHz, Δf = ± 75 kHz, f_{mod} = 1 kHz, Q_B approx. 45)

AF output voltage (V_i = 10 mV)	$V_{AF\,rms}$	0.4	0.7		V
Input voltage for limiting	$V_{i\,lim}$		50	100	µV
AM suppression V_i = 500 µV, m = 30%	a_{AM}	40	50		dB
V_i = 10 mV, m = 30%	a_{AM}	60	68		dB
Input impedance	Z_i		20/4		kΩ/pF

Characteristics of the additive circuit

		min	typ	max	
Z voltage ($I_{12} = 5$ mA)	V_{12}	11.2	12	13.2	V
Z resistance	R_Z		30	55	Ω
Breakdown voltage	V_{CBO}	26	40		V
Breakdown voltage ($I_3 = 500$ µA)	V_{CEO}	13			V
Current gain ($V_{CE} = 5$ V, $I_C = 1$ mA)	G_I	25	80		

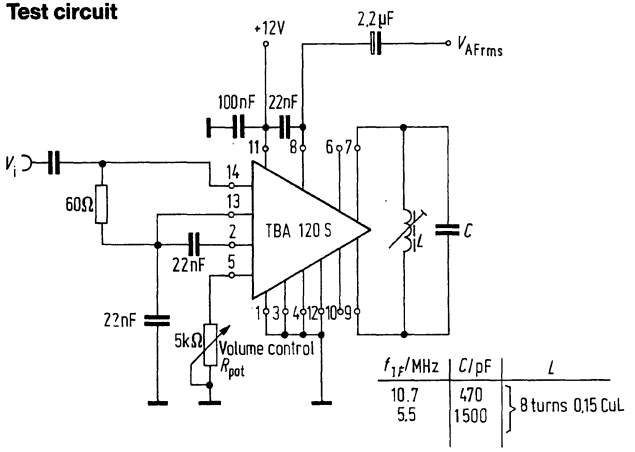
Pins 3 and 4 are connected to the collector or the base of a transistor, which may be used as an AF preamplifier ($I_C < 5$ mA) or as a bass/treble switch (dc on or off-switching of an *RC* circuit).

At pin 12, a Z diode (12 V) is accessible which can be used to stabilize the supply voltage of this IC or the voltage of other included circuit elements ($I_Z \leqq 15$ mA).

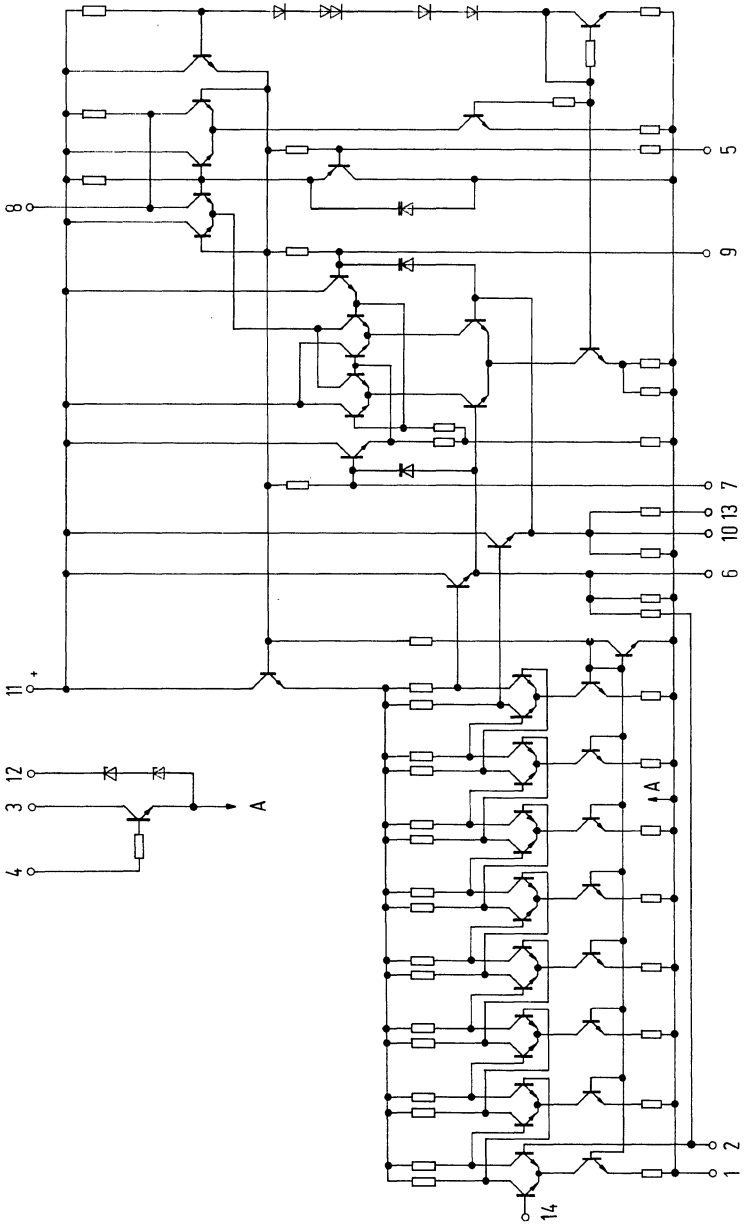
The IC TBA 120 S is manufactured in different groups according to the volume specifications. An attenuation of 30 dB requires a resistor to be switched to ground at pin 5 with a resistance value as allocated to the groups listed below. The group number is imprinted on the plastic package.

Group	II	III	IV	V
R_{pot}	1.9 to 2.2	2.1 to 2.5	2.4 to 2.9	2.8 to 3.3

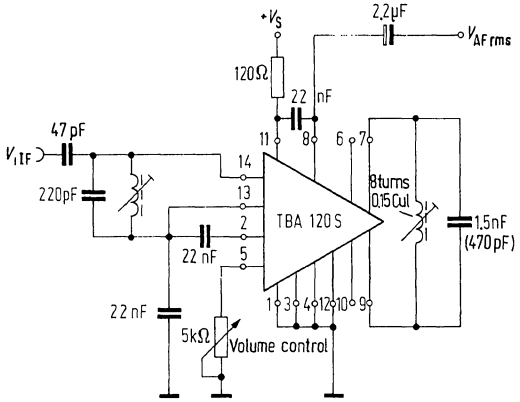
Test circuit



Circuit diagram



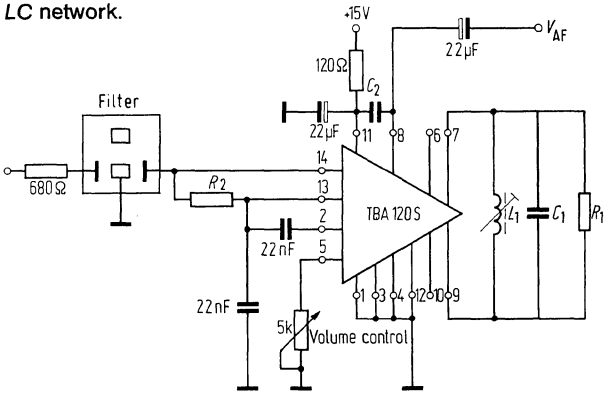
Application circuit 5.5 MHz (10.7 MHz)



Values in parentheses apply to 10.7 MHz

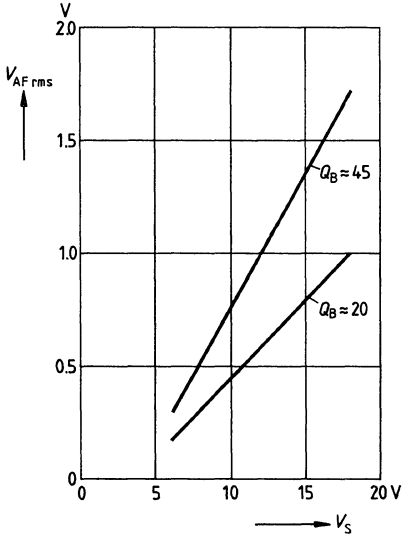
Application circuit with ceramic filter (Murata)

For good adjacent channel suppression the ceramic filter should be combined with an *LC* network.

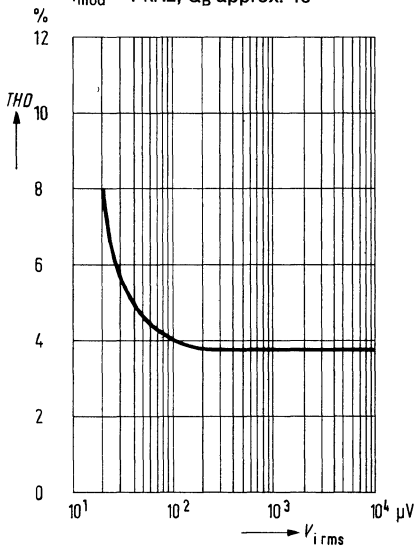


	Sound IF in TV sets	Sound IF in TV sets of American Std.	FM IF in radio mono sets	FM IF in RF stereo sets
C_1	1.5 nF	2.2 nF	470 pF	330 pF
C_2	22 nF	22 nF	22 nF	470 pF
L_1	8 turns, 0.15 CuL	8 turns, 0.15 CuL	8 turns, 0.15 CuL	12 turns, 0.15 CuL
R_1	∞	∞	∞	1 kΩ
R_2	680 Ω	1 kΩ	330 Ω	330 Ω
Filter (Murata)	SFE 5.5 MA	SFE 4.5 MA	SFE 10.7	SFE 10.7

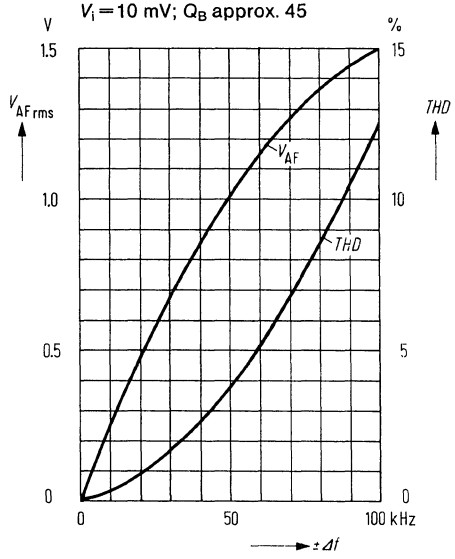
AF output voltage versus supply voltage
$f_Z = 5.5$ MHz; $\Delta f = \pm 50$ kHz,
$f_{mod} = 1$ kHz; $V_i = 10$ mV



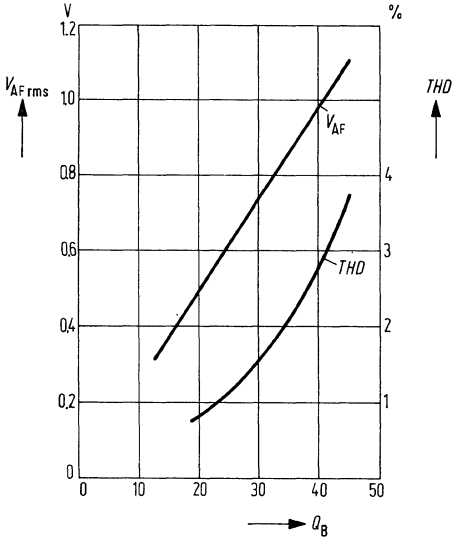
Total harmonic distortion versus input voltage
$V_S = 12$ V; $f_Z = 5.5$ MHz; $\Delta f = \pm 50$ kHz;
$f_{mod} = 1$ kHz; Q_B approx. 45



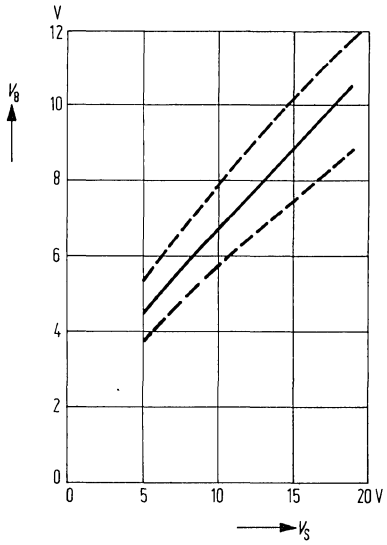
AF output voltage and total harmonic distortion v. frequency deviation
$V_S = 12$ V; $f_Z = 5.5$ MHz; $f_{mod} = 1$ kHz
$V_i = 10$ mV; Q_B approx. 45



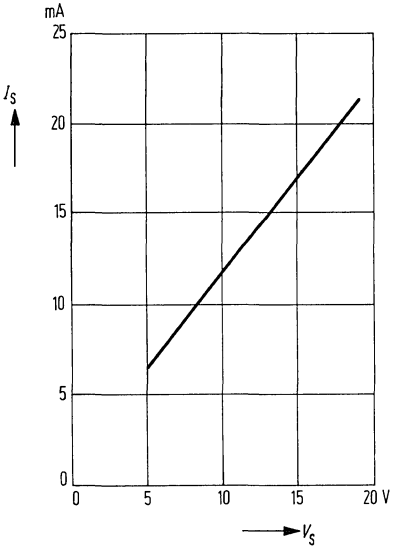
AF output voltage and total harmonic distortion versus Q_B factor
$V_S = 12$ V; $\Delta f = \pm 50$ kHz;
$f_{mod} = 1$ kHz; $V_i = 10$ mV



DC output voltage versus supply voltage

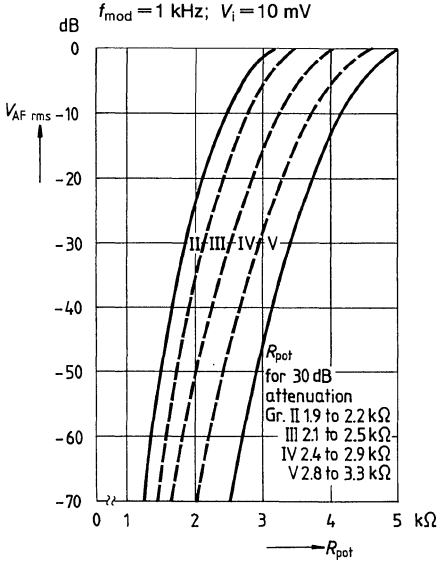


Current consumption versus supply voltage



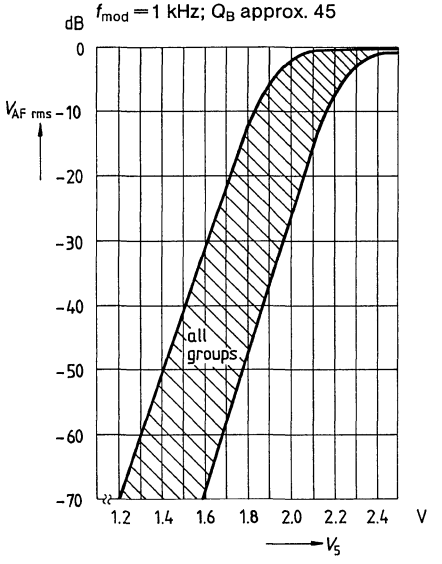
Volume control versus potentiometer resistance

$V_S = 12$ V; $f_Z = 5.5$ MHz; $\Delta f = \pm 50$ kHz
$f_{mod} = 1$ kHz; $V_i = 10$ mV

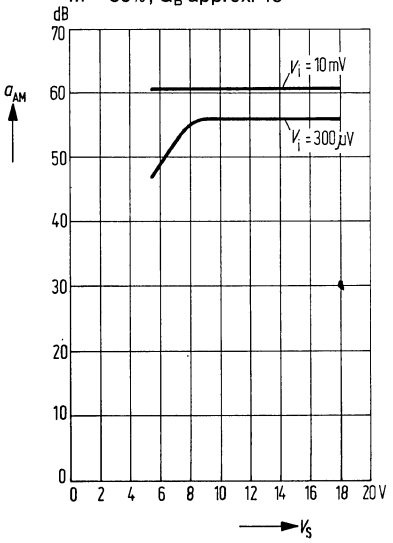


Volume control versus voltage to pin 5

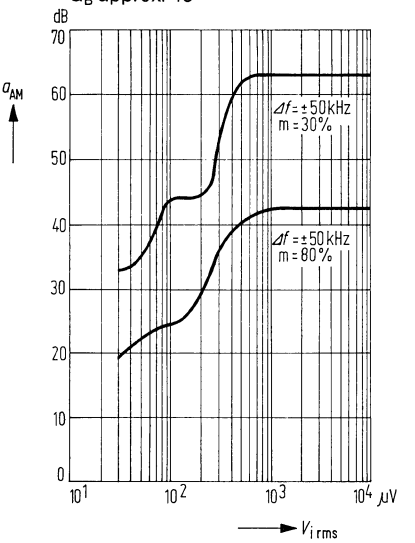
$V_S = 12$ V; $f_Z = 5.5$ MHz; $\Delta f = \pm 50$ kHz
$f_{mod} = 1$ kHz; Q_B approx. 45



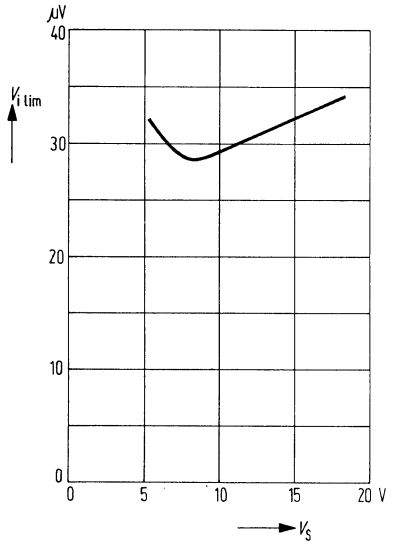
AM suppression versus supply voltage
$f_Z = 5.5$ MHz; $\Delta f = \pm 50$ kHz; $f_{mod} = 1$ kHz
$m = 30\%$; Q_B approx. 45



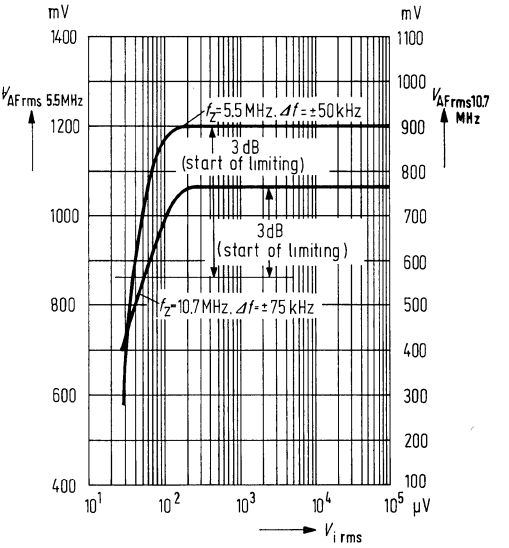
AM suppression versus input voltage
$V_S = 12$ V; $f_Z = 5.5$ MHz; $f_{mod} = 1$ kHz
Q_B approx. 45



Input voltage for limiting versus supply voltage
$f_Z = 5.5$ MHz; $\Delta f = \pm 50$ kHz;
$f_{mod} = 1$ kHz; Q_B approx. 45



AF output voltage versus input voltage
$V_S = 12$ V; $f_{mod} = 1$ kHz; Q_B approx. 45



FM IF Amplifier and Demodulator

TBA 120 T
TBA 120 U

DIP 16

The symmetrical 8-stage amplifier with symmetrical coincidence demodulator for amplifying, limiting, and demodulating frequency-modulated signals, is especially suited for the sound IF units in TV sets. In addition to the controlled AF output, an uncontrolled AF output and an AF input for the connection of video recorders is available.

Features

- Outstanding limiting qualities
- Few external components
- Terminal for video recorder
- AF output voltage independent of supply voltage
- Insensitive to hum
- Very little residual IF

TBA 120 T: Input and demodulator matched to ceramic resonators
TBA 120 U: Input and demodulator matched to *LC* networks.

Maximum ratings

Supply voltage	V_S	18	V
Voltage	V_5	6	V
Current	I_4	5	mA
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	90	K/W

Operating range

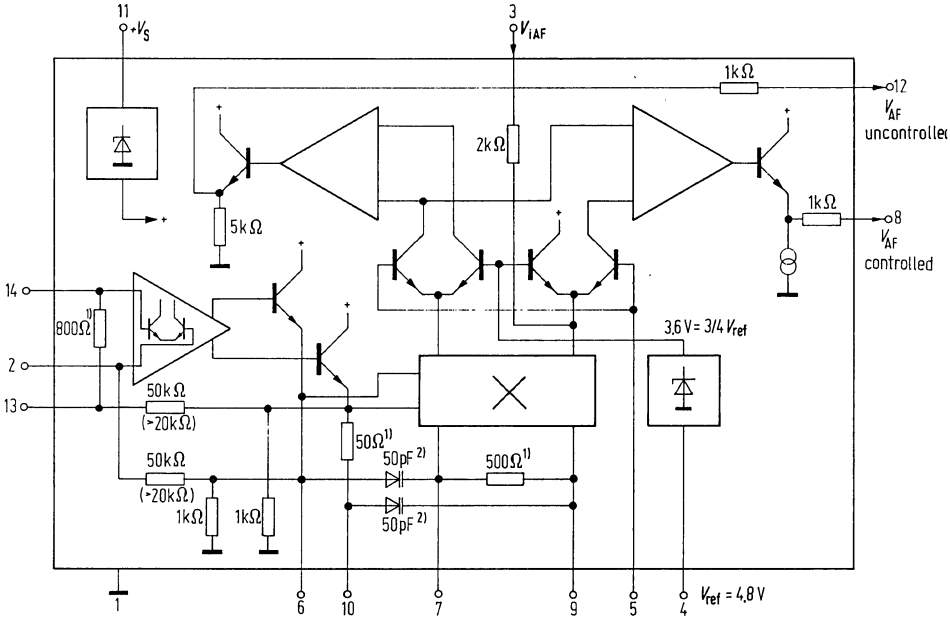
Supply voltage range	V_S	10 to 18	V
Ambient temperature range	T_{amb}	−15 to 70	°C
Frequency range	f	0 to 12	MHz

Characteristics ($V_S = 12$ V; $T_{amb} = 25$ °C, Q_B approx. 45, $f_{IF} = 5.5$ MHz)

		min	typ	max	
Current consumption	I_S	9.5	13.5	17.5	mA
IF voltage gain V_6/V_{14}	G_v		68		dB
IF output voltage with limiting at each output	V_{qpp}	175	250	325	mV
Output resistance	R_{q8}	0.8	1.1	1.4	kΩ
	R_{q12}	0.8	1.1	1.4	kΩ
Input resistance	R_{i3}	1.4	2.0	2.6	kΩ
Internal resistance	R_{i4}		12	16	Ω
DC level of output signal	V_8	3.4	4.0	4.7	V
($V_i = 0$)	V_{12}	4.4	4.9	6.3	V
Stabilized voltage	V_4	4.2	4.8	5.3	V
Residual IF voltage without deemphasis	V_8		20		mV
	V_{12}		30		mV
AF gain (AF not attenuated)	V_8/V_3	6	7.5	8.5	
Attenuation ($R_{4\text{-}5} = 5$ kΩ; $R_{5\text{-}1} = 13$ kΩ)	V_{AF8}	20	30	40	dB
Range of volume control	$\frac{V_{AF8\,max}}{V_{AF8\,min}}$	70	85		dB
Resistance	$R_{4\text{-}5}$[1]	1		10	kΩ
Input voltage for limiting ($\Delta f = \pm 50$ kHz; $f_{mod} = 1$ kHz)	$V_{i\,lim}$		30	60	µV
Hum suppression	V_8/V_{11}		35		dB
	V_{12}/V_{11}		30		dB
Signal-to-noise ratio ($V_i = 10$ mV)	$a_{S/N}$	80	85		dB
Noise voltage (in acc. with DIN 45405)	V_n			70	µV
Input impedance	$R_{q7\text{-}9}$		5.4		kΩ
TBA 120 T only:					
AF output voltage	$V_{8\,rms}$	650	900	1100	mV
($\Delta f = \pm 50$ kHz; $f_{mod} = 1$ kHz)	$V_{12\,rms}$	400	650	1000	mV
Input impedance	Z_i		800/5		Ω/pF
AM suppression	a_{AM}	50	60		dB
($V_i = 500$ µV; $\Delta f = \pm 50$ kHz; $m = 30\%$; $f_{mod} = 1$ kHz)					
Bridging resistance	$R_{13\text{-}14}$			1	kΩ
TBA 120 U only:					
AF output voltage	$V_{8\,rms}$	850	1200	1700	mV
($\Delta f = \pm 50$ kHz; $V_i = 10$ mV;	$V_{12\,rms}$	600	1000	1600	mV
$f_{mod} = 1$ kHz; $THD = 4\%$)					
Input impedance ($f_i = 5.5$ MHz)	Z_i	15/6	40/4.5		kΩ/pF
AM suppression	a_{AM}	50	60		dB
($\Delta f = \pm 50$ kHz; $V_i = 500$ µV; $f_{mod} = 1$ kHz; $m = 30\%$)					
Total harmonic distortion	THD		1.3	2.5	%
($\Delta f = \pm 25$ kHz; $V_i = 10$ mV; $f_{mod} = 1$ kHz)					

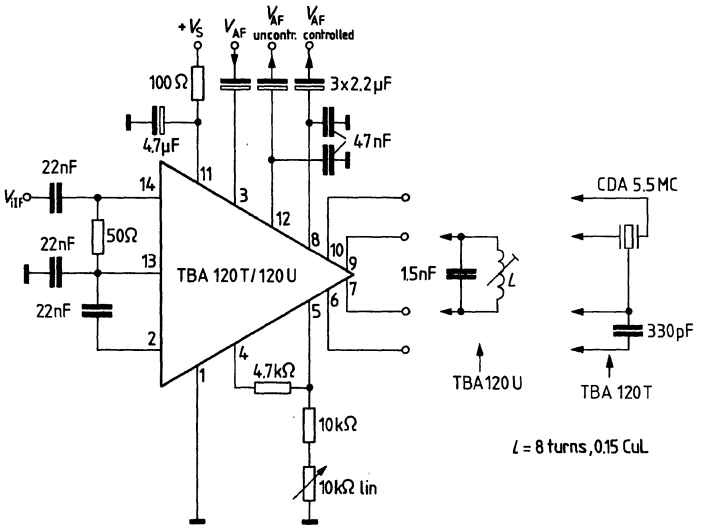
1) If DC volume control is not used, pin 4 has to be connected directly to pin 5

Block diagram

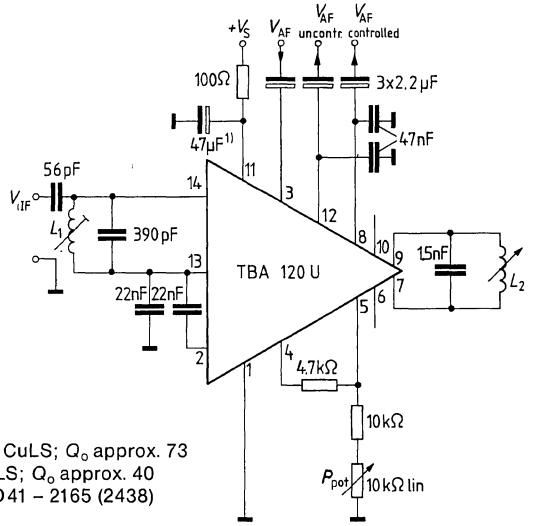


1) only TBA 120 T
2) only TBA 120 U

Test circuit (5.5 MHz)

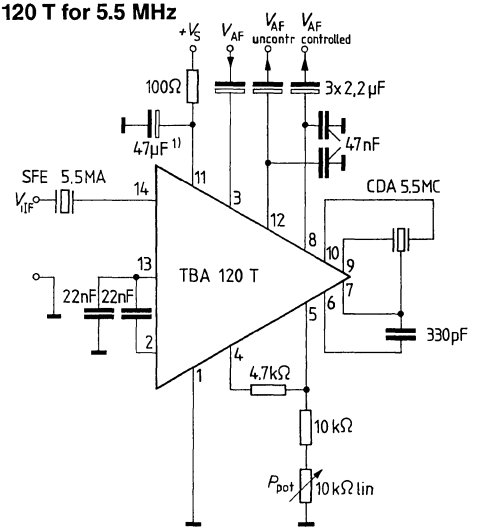


Application circuit TBA 120 U for 5.5 MHz



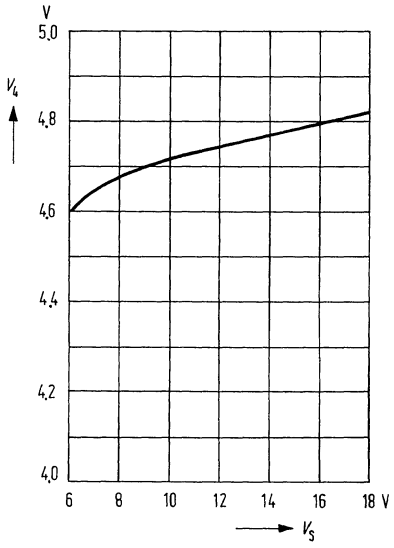
L_1: 20 turns 15x0.05 CuLS; Q_0 approx. 73
L_2: 9 turns 0.25 CuLS; Q_0 approx. 40
Coil assembly Vogt D41 – 2165 (2438)
without cup core

Application circuit TBA 120 T for 5.5 MHz

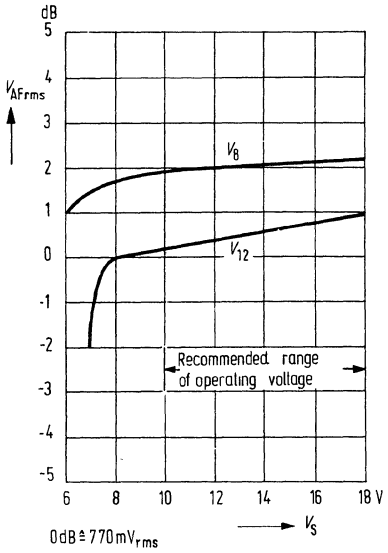


1) Omitting the electrolytic capacitor 47 µF at pin 11 changes the volume-control range.

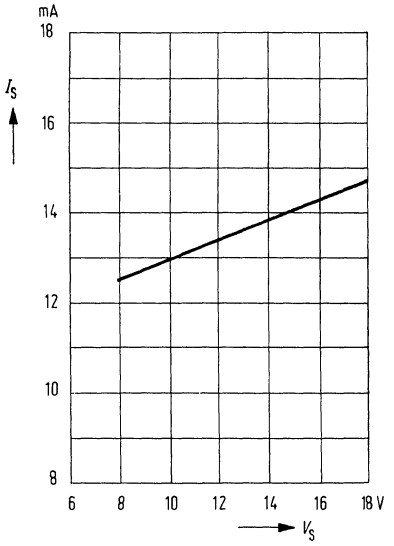
Z voltage versus supply voltage



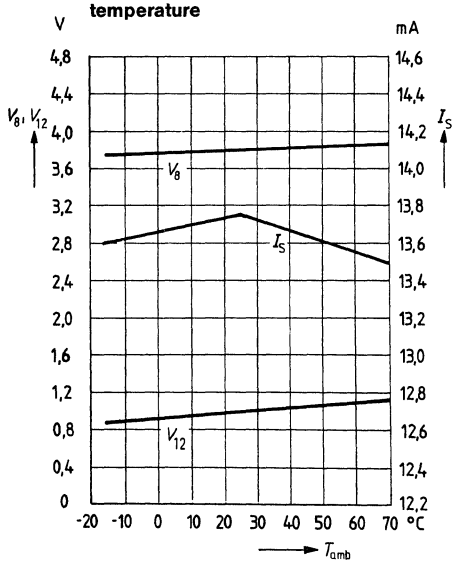
AF output voltage versus supply voltage



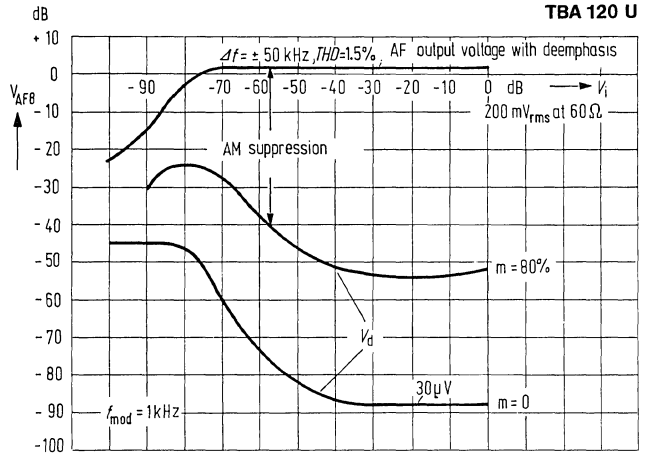
Current consumption versus supply voltage



AF output voltage and current consumption versus ambient temperature

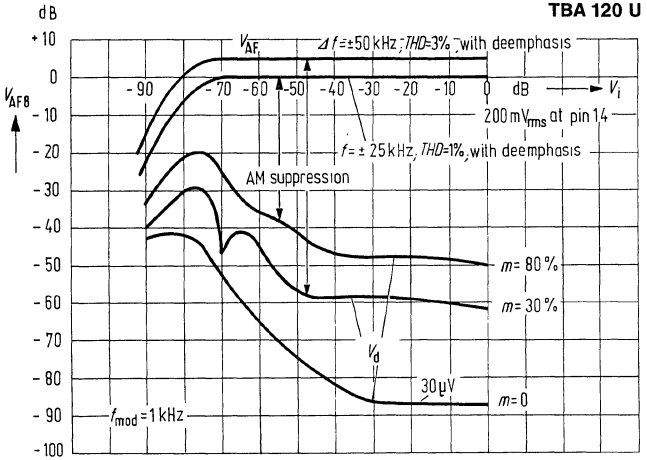


AF output voltage and disturbance voltage versus input voltage
(Input wired with SFE 5.5 MA/Murata)



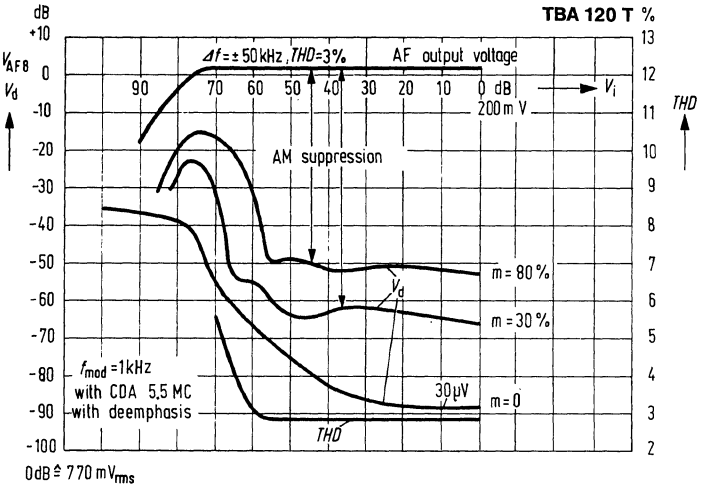
0dB ≙ 770 mV_{rms}

AF output voltage and disturbance voltage versus input voltage
(Input 60 Ω impedance broadband)

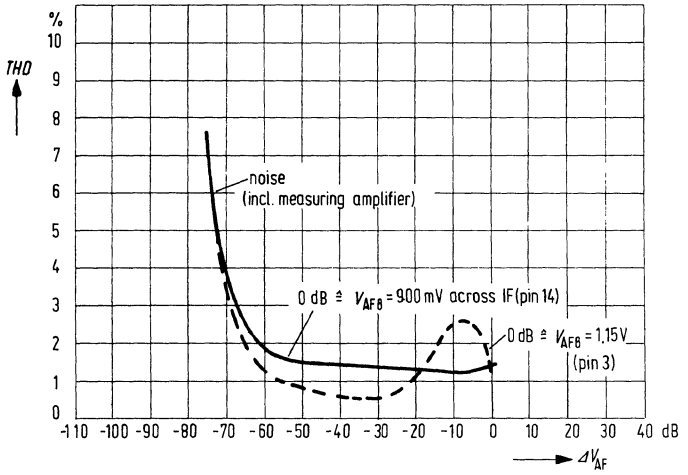


0dB = 770 mV_{rms}

AF output voltage (pin 8), disturbance voltage, and total harmonic distortion versus input voltage

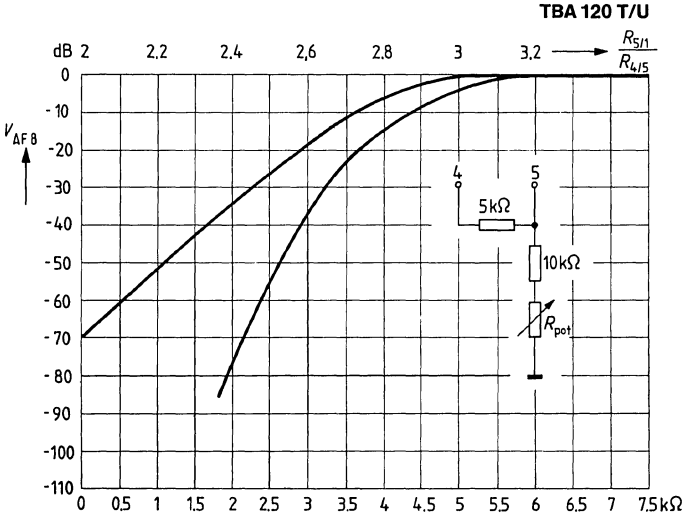


Total harmonic distortion versus volume control



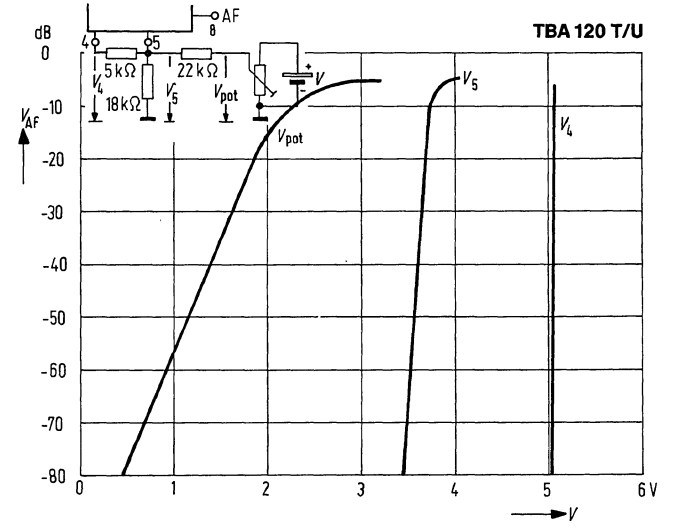
Spread

AF output voltage (pin 8) versus potentiometer resistance and versus ratio of resistance

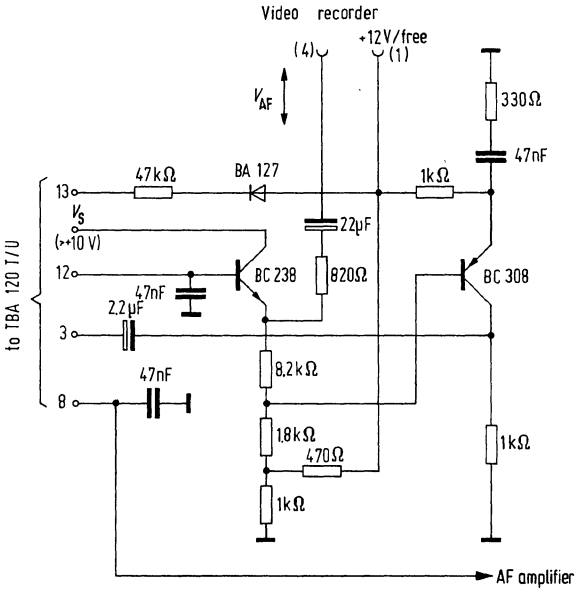


With 47 µF electrolytic capacitor at pin 11 to ground ⟶ R_x

AF output voltage (pin 8) versus voltage fed into pin 5



Circuit for direct connection to video recorders



Socket (1): Switching voltage: at playback +12 V
at recording: free
Socket (4): Simultaneous input and output for AF

Function

When the switching voltage is applied, the emitter follower BC 238 is blocked at the output, and the buffer stage BC 308 is switched on. A preemphasis is included to balance the deemphasis at the AF output. The IF amplifier becomes inoperable by means of the diode BA 127 and the 47 kΩ resistor. The remote-controlled volume regulator in the TBA 120 T/U is used for recording and playback.

SO 14

The TBB 042 G is a symmetrical mixer applicable for frequencies up to 200 MHz. It can be driven either by an external source or by a built-in oscillator.

Common applications are in receivers, converters, and demodulators for AM and FM signals.

Features

- Wide range of supply voltage
- Few external components
- High conversion transconductance
- High pulse strength
- Low noise

Maximum ratings

Supply voltage	V_S	15	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	–40 to 125	°C
Thermal resistance (system - air)	$R_{th\,SA}$	125	K/W

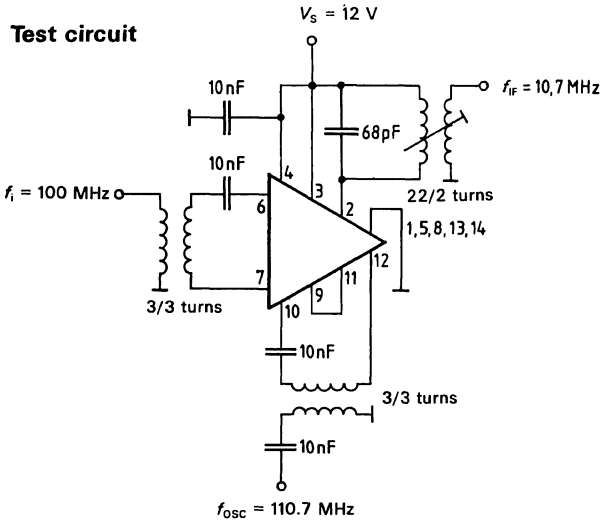
Operating range

Supply voltage range	V_S	4 to 15	V
Ambient temperature range	T_A	–15 to 70	°C

Characteristics
V_S = 12 V, T_A = 25°C

		min.	typ.	max.	
Current consumption	$I_S = I_2 + I_3 + I_5$	1.4	2.15	2.9	mA
Output current	$I_2 = I_3$	0.36	0.52	0.68	mA
Output current difference	$I_3 - I_2$	–60		60	mA
Supply current	I_5	0.7	1.1	1.6	mA
Power gain (f_i = 100 MHz, f_{OSC} = 110.7 MHz)	G_P	14	16.5		dB
Breakdown voltage ($I_{2,3}$ = 10 mA; $V_{7,8}$ = 0 V)	V_2, V_3	25			V
Output capacitance	$C_{2\text{-}M}$, $C_{3\text{-}M}$		6		pF
Conversion transductance (f = 455 kHz)	$S = \frac{I_2}{V_7\text{-}V_8} = \frac{I_3}{V_7\text{-}V_8}$		5		mS
Noise figure	NF		7		dB

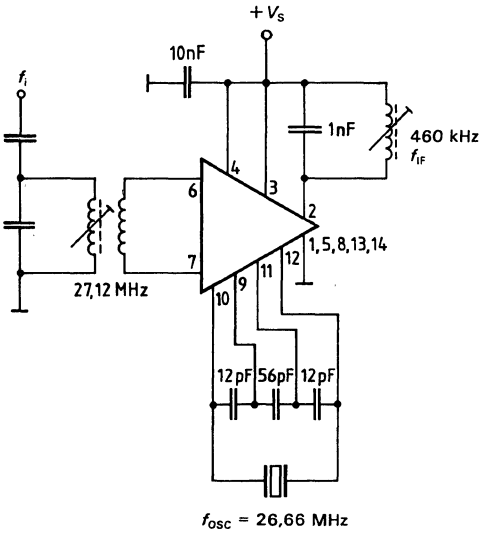
Test circuit



Application circuit

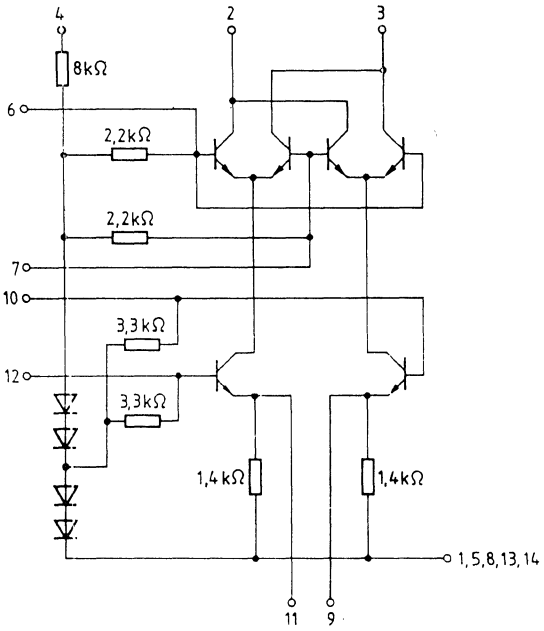
Mixer for remote control receiver

self-oscillating



For harmonic crystals, an inductor between pins 9 and 11 which will prevent oscillations on the fundamental is recommended.

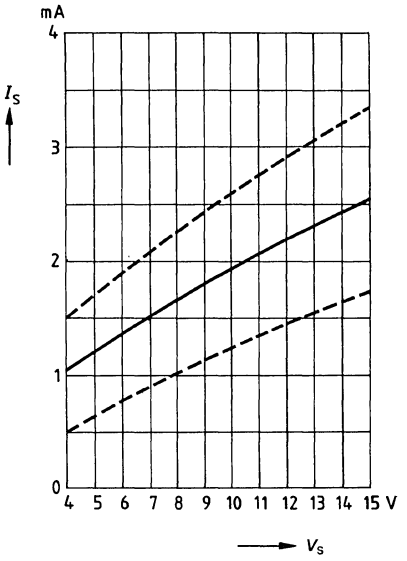
Circuit diagram



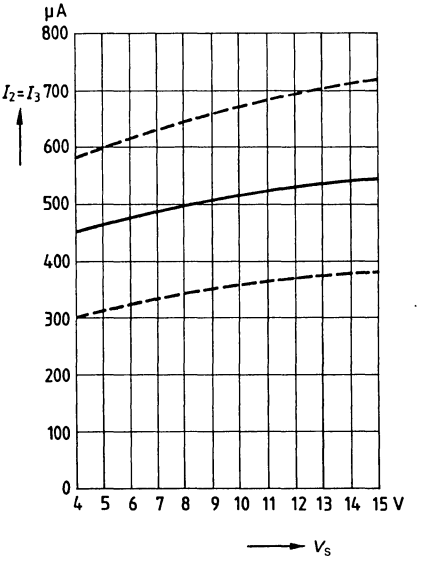
It is recommendable to establish a galvanic connection between pins 6 and 7 and pins 10 and 12 through coupling windings.

A resistor of at least 220 Ω may be connected between pins 9 and 14 (GND) and pins 11 and 14 to increase the currents and thus the conversion transconductance. Pins 9 and 11 may be connected via any impedance. In case of a direct connection between pins 9 and 11 the resistance from this connection to pin 14 may be at least 100 Ω. Depending on the layout, a capacitor (10 to 50 pF) may be required between pins 6 and 7 to prevent oscillations in the VHF band.

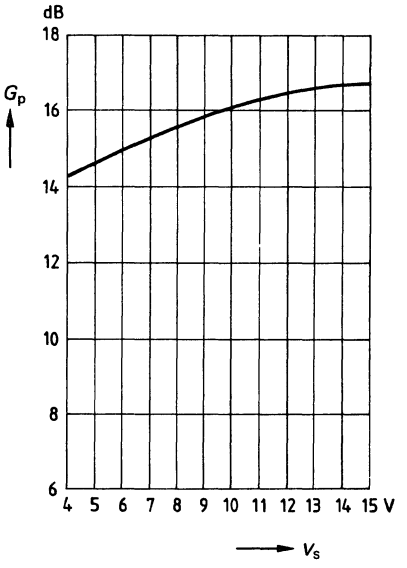
Total current consumption versus supply voltage



Output current versus supply voltage



Power gain versus supply voltage



PLL Frequency Synthesizer

TBB 200
TBB 200 G

Preliminary data

DIP 14
SO 14

TBB 200 is a CMOS IC which has been especially developed for use in radio equipment. It is suited to simple frequency synthesis as well as to dual modulus synthesis.

Features

- Bit serial control with 2 lines (I^2C bus)
- Modulus switching
- Voltage doubler for high phase-detector output voltage
- Direct VCO control without op amp
- High input sensitivity (10 mV), high input frequencies (70 MHz) in single modulus operation
- Low supply voltage, wide temperature range
- Standby circuit
- Extremely fast phase-detector with very short anti-backlash pulse
- Large dividing ratios
  - A divider 1 to 127
  - N divider 3 to 4095
  - R divider 3 to 65535
- Switchable phase-detector polarity
- Switchable phase-detector retuning rate of rise
- PORT output addressable via I^2C bus
  - for prescaler standby
  - for prescaler programming (128 or 64)

I^2C bus is a patented bus system of Philips.

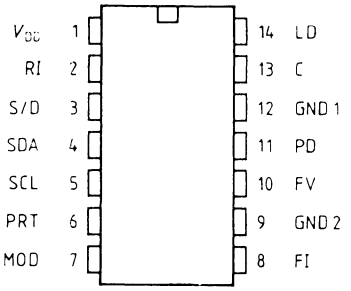
Circuit description

TBB 200 is a complex PLL component in CMOS technology for processor controlled frequency synthesis. Pin S/D selects **S**ingle or **D**ual modulus operation. Functions and dividing ratios are selected via an I²C bus interface at pins SDA and SCL. An output port PRT permits control (e.g. standby) of additional circuitry. The reference frequency is applied at input RI; its maximum value is 30 MHz. The VCO frequency is applied at input FI. Its maximum value in single modulus operation is 70 MHz and in dual modulus operation 30 MHz. The PLL can be operated optionally with or without internal voltage doubler, depending on the required frequency variation (Varicap). For operation with voltage doubler, a capacitance of typ. 1 µF (MKH) must be connected at pin C. C must be grounded when the voltage doubler is not in use. Output PD supplies the phase detector signal with especially short anti-backlash pulses to neutralize even the smallest phase deviations. Polarity and current of the PD output can be switched via the I²C bus. Output LD supplies a static lock detector signal, and output FV the divided VCO frequency. LD and FV are open drain outputs.

For test purposes, a switch-on reset is provided, which is discontinued by the first H pulse at RI. In the reset state, the dividers are switched to the programming mode.

Mode	S/D
Single modulus	L
Dual modulus	H

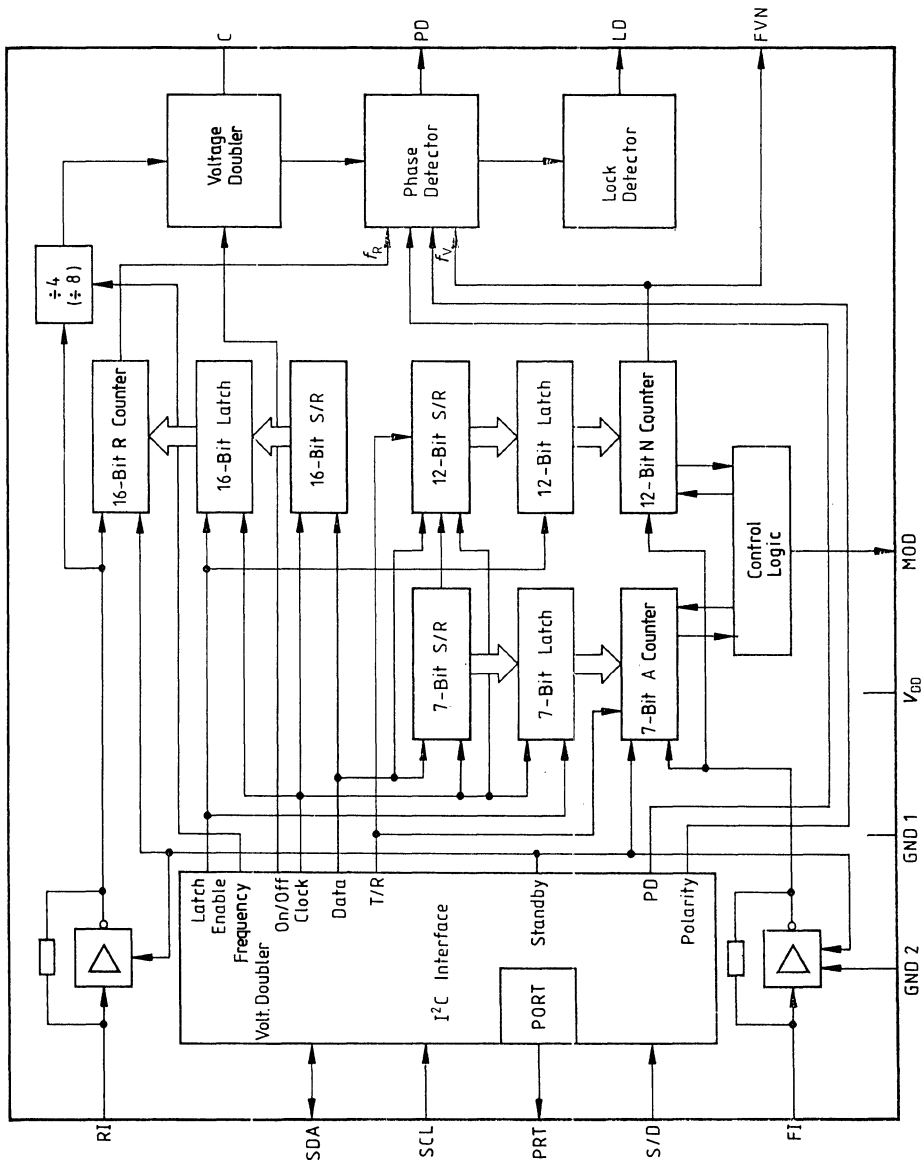
Pin configuration
(top view)



Pin description

Pin	Symbol	Function
1	V_{DD}	Supply voltage
2	RI	Reference frequency
3	S/D	Operating mode (single modulus/dual modulus)
4	SDA	I²C bus data
5	SCL	I²C bus clock
6	PRT	I²C PORT
7	MOD	Modulus control
8	FI	VCO frequency
9	GND 2	Ground
10	FV	Comparison frequency
11	PD	Phase detector
12	GND 1	Ground
13	C	Voltage-doubling capacitance
14	LD	Lock detector

Block diagram



Characteristics

		Test conditions	min	max	
Input signals SDA, SCL					
H input voltage	V_{IH}		0.7 x V_{DD}	V_{DD}	V
L input voltage	V_{IL}		0	0.3 x V_{DD}	V
Input capacitance	C_I			10	pF
Input current	I_{IM}	$V_I = V_{DD}$		10	µA
Input signal S/D					
Input voltage	V_{IH}		0.7 x V_{DD}	V_{DD}	V
L input voltage	V_{IL}		0	0.3 x V_{DD}	V
Input capacitance	C_I			10	pF
Input current	I_{IM}	$V_I = V_{DD}$		10	µA
Input signal RI					
Input frequency	f	$V_{DD} = 4.5$ V		30	MHz
Input voltage	$V_{I\,rms}$	(sine)	500		mV
Input capacitance	C_I			10	pF
Input current	I_{IM}	$V_I = V_{DD}$		10	µA
Input signal FI (dual modulus)					
Input frequency	f	$V_{DD} = 4.5$ V		30	MHz
Input voltage	$V_{I\,rms}$	(sine)	50		mV
Input current	I_{IM}	$V_I = V_{DD}$		10	µA
Input capacitance	C_I			10	pF
Input signal FI (single modulus)					
Input frequency	f	$V_{DD} = 4.5$ V		70	MHz
Input voltage	$V_{I\,rms}$	(sine)	10		mV
Input capacitance	C_I			10	pF
Input current	I_{IM}	$V_I = V_{DD}$		10	µA
Input frequency	f	$V_{DD} = 3$ V		35	MHz
Output signal SDA, LD (open-drain output)					
L output voltage	V_{QL}	$I_Q = 3.0$ mA $V_{DD} = 3$ V $C_L = 400$ pF		0.4	V

Maximum ratings

		min	typ	max		Notes
Supply voltage	V_{DD}	−0.3		6	V	
Input voltage	V_{IM1}	−0.3		V_{DD} +0.3	V	
Output voltage at C	V_{IM2}	$-V_{DD}$		0	V	Exception: C
Power dissipation per output	P_Q			10	mW	(internally
Total power dissipation	P_{tot}			300	mW	generated)
Storage temperature	T_{stg}	−50		125	°C	

Operating range

Supply voltage	V_{DD}	3	5	5.5	V	
Supply current	I_{DD}			7	mA	
Supply current: standby FI RI	I_{DD}			1	µA	
Supply current: standby counter	I_{DD}		4		mA	$V_{FI\,rms}$ = 10 mV
Supply current: standby counter	I_{DD}		3		mA	$V_{FI\,rms}$ = 100 mV
Supply current: standby counter	I_{DD}		2		mA	$V_{FI\,rms}$ = 500 mV
Ambient temperature	T_A	−40		85	°C	

Current measurement excluding output circuitry and voltage doubling.

Characteristics

V_{DD} = 4.5 V to 5.5 V; T_A = −40 to 85 °C

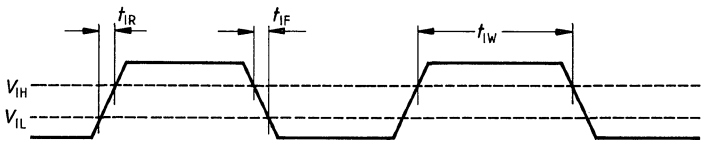
		Test conditions	min	max	
Output signal PD (Tri-state output)					
H current mode	I_{QH}			±1	mA
L current mode	I_{QL}			±0.1	mA
Tri-state	I_{Q3}	V_{PD} I V_{DD} I, 25 °C		50	nA
Output signal FV N (Open-drain output)		I_{QL} = 1 mA			
L output voltage	V_{qL}	C_L = 20 pF		0.4	V
L output pulse width		t_{QWL} = 1/FI			
Output signal MOD, PRT					
H output voltage	V_{QH}	I_{QH} = 0.5 mA	V_{DD} −0.4		V
L output voltage	V_{QL}	I_{QL} = 0.5 mA		0.4	V
Output current MOD*					
H output current	I_{QL}	V_{DD} = 3 V	500		µA

Dynamic characteristics

V_{DD} = 5 V; T_A = −40 to 85 °C

Input signal RI					
Rise time	t_{IR}	V_{DD} = 5 V	5		ns
Fall time	t_{IF}	V_{DD} = 5 V	5		ns
Pulse width	t_{IW}	V_{DD} = 5 V	10		ns
Input signal FI					
Rise time	t_{IR}	V_{DD} = 5 V	5		ns
Fall time	t_{IF}	V_{DD} = 5 V	5		ns
Pulse width	t_{IW}	V_{DD} = 5 V	10		ns
	t_{IW}	dual modulus V_{DD} = 5 V	10		ns
	t_{IW}	single modulus V_{DD} = 5 V	5		ns

Pulse diagram



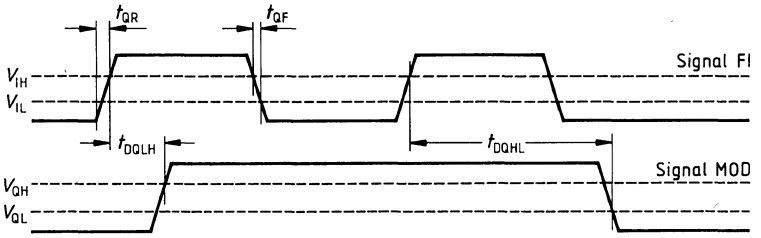
* Status bit 8 via I²C bus: 1

Dynamic Characteristics

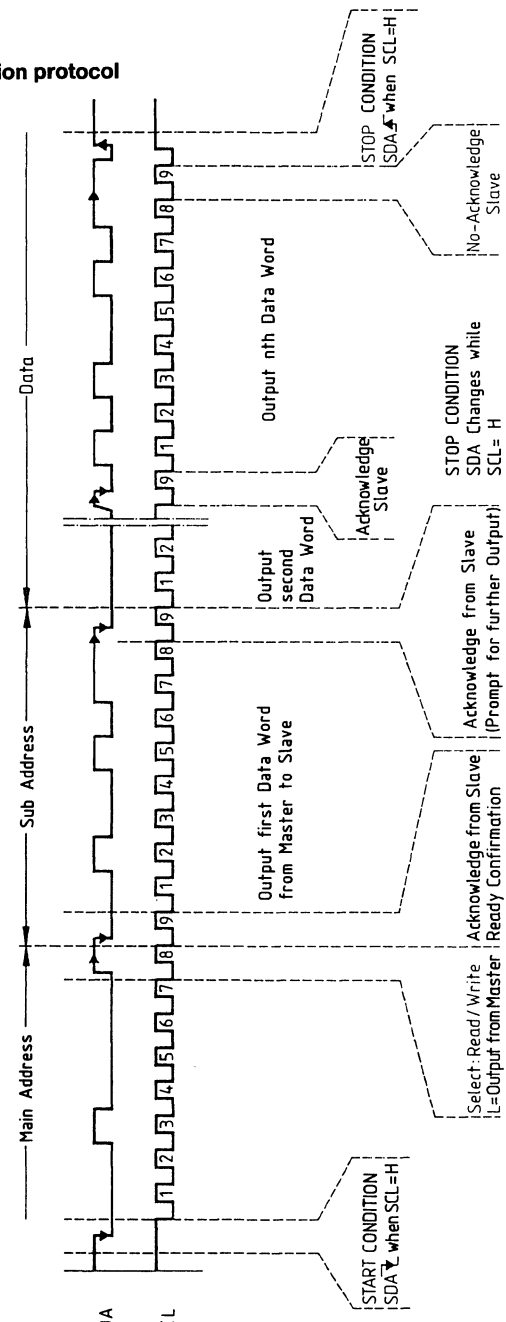
$V_S = 5$ V; $T_A = -40$ to 85 °C

		Test conditions	min	max	
Output signal PRT					
Rise time	t_{QR}	$V_{DD} = 5$ V, $C_L = 30$ pF		1	µs
Fall time	t_{QF}	$V_{DD} = 5$ V, $C_L = 30$ pF		1	µs
Output signal FV					
Fall time	t_{QF}	$V_{DD} = 5$ V, $C_L = 20$ pF		20	ns
Output signal MOD					
Rise time	t_{QR}	$V_{DD} = 5$ V, $C_L = 30$ pF		10	ns
Fall time	t_{QF}	$V_{DD} = 5$ V, $C_L = 30$ pF		10	ns
Delay time L-H to FI	t_{DQLH}	$V_{DD} = 5$ V, $C_L = 30$ pF		25	ns
Delay time H-L to FI	t_{QDHL}	$V_{DD} = 5$ V, $C_L = 30$ pF		15	ns

Pulse diagram



I²C bus transmission protocol



Transmission protocol for programming

	SDA		Single modulus	Dual modulus
	Start			
IC	1		1	1
A	2		1	1
D	3		0	0
D	4		0	0
R	5		0	0
E	6		1	1
S	7		0	1
S	8		0	0
	ACK			
SUB	1		0	0
A	2		0	0
D	3		0	0
D	4		0	0
R	5		1	1
E	6		0	0
S	7		0	1
S	8	R/W	0	0
	ACK			
	1			
S	2		PORT	
T	3		Counter	
A	4		FI, RI	
T	5		PD Polarity	
U	6		PD Current	
S	7		Voltage-Doubler Frequency	
	8		Voltage-Doubler Status	
	ACK		Modulus Output	
	Stop			

Status bit 0	1
Low***	High***
off*	on
off*	on
neg.	pos.
0.1 mA	1 mA
÷2	÷4
off	on
push pull	current source**

* standby
** matched to TBB 202
*** PORT output state

Transmission protocol for programming

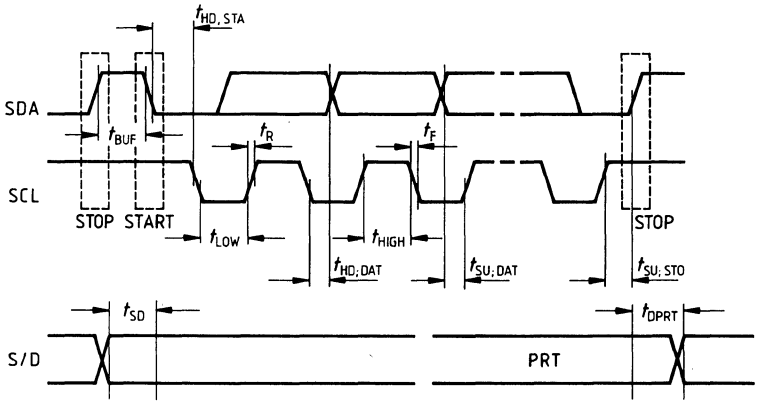
	SDA		R Counter Single Modulus	R Counter Dual Modulus	SDA		N Counter Single Modulus	SDA		A/N Counter Dual Modulus
	Start				Start			Start		
A	1		1	1	1		1	1		1
D	2		1	1	2		1	2		1
D	3		0	0	3		0	3		0
R	4		0	0	4		0	4		0
E	5		0	0	5		0	5		0
S	6		1	1	6		1	6		1
S	7		0	1	7		0	7		1
	8	R/W	0	0	8	R/W	0	8	R/W	0
	ACK				ACK			ACK		
S	1		0	0	1		0	1		0
U	2		0	0	2		0	2		0
B	3		0	0	3		0	3		0
A	4		0	0	4		0	4		0
D	5		0	0	5		1	5		1
D	6		1	1	6		1	6		1
R	7		0	1	7		0	7		1
	8	R/W	0	0	8	R/W	0	8	R/W	0
	ACK				ACK			ACK		
S	1			MSB	1		X	1		X
T	2				2		X	2		X
A	3				3		X	3		X
T	4				4		X	4		X
U	5			R	5		MSB	5		MSB
S	6				6			6		
	7			C	7			7		
	8			O	8		N	8		N
	ACK			U	ACK			ACK		
S	1			N	1		C	1		C
T	2			T	2		O	2		O
A	3			E	3		U	3		U
T	4			R	4		N	4		N
U	5				5		T	5		T
S	6				6		E	6		E
	7				7		R	7		R
	8			LSB	8		LSB	8		LSB
	ACK				ACK			ACK		
	Stop				Stop		S	1		X
							T	2		MSB
							A	3		A
							T	4		C
							U	5		O
							S	6		U
								7		N
								8		T
								ACK		E
								Stop		R
										LSB

X = don't care

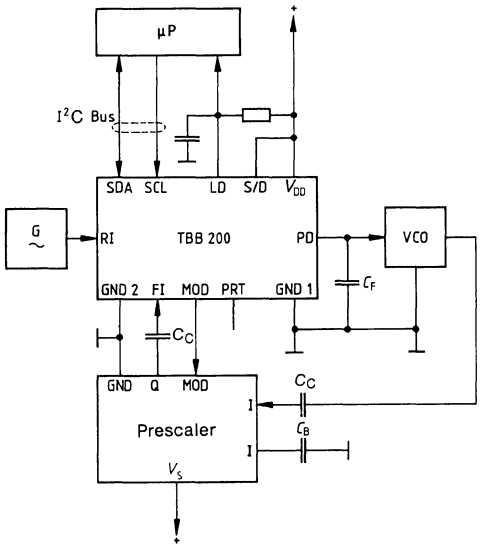
		min	max	
Clock frequency	f_{SCL}	0	100	kHz
	$t_{HD;DAT}$	0		µs
Inactive time prior to next transmission	t_{BUF}	4.7		µs
Start condition hold time				
(first CLOCK pulse is generated after this time period)	$t_{HD;STA}$	4.0		µs
Clock LOW phase	t_L	4.7		µs
Clock HIGH phase	t_H	4.0		µs
DATA set-up time	$t_{SU;DAT}$	250		ns
SDA and SCL signal rise time	t_R		1	µs
SDA and SCL signal fall time	t_F		300	ns
SCL pulse set-up time with Stop condition	$t_{SU;STO}$	4.7		µs
Status programming set-up time (S/D)	t_{SD}	500		ns
PRT delay time relative to Stop condition	t_{DPRT}		500	µs

All times with reference to specified input levels V_{IH} and V_{IL}.

Pulse diagrams for I²C bus, S/D, PRT

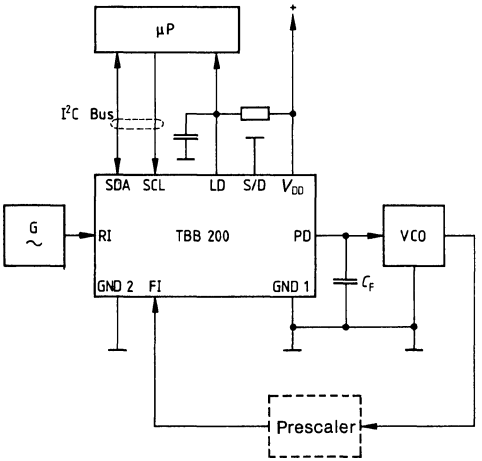


Application circuits



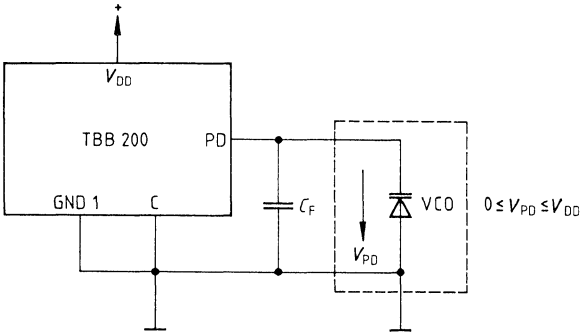
C_C = Coupling Capacitance
C_B = Blocking Capacitance

Operation: dual modulus (f_{max} = 30 MHz at FI)

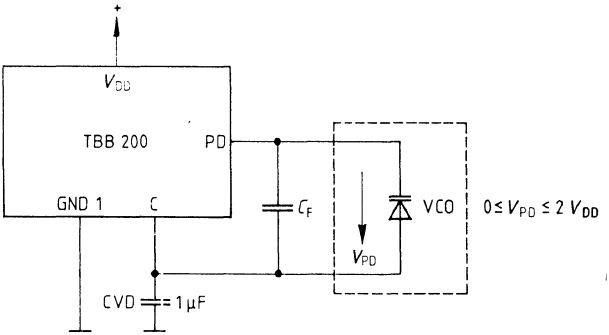


Operation: single modulus (f_{max} = 70 MHz at FI)
C_F: loop filter capacitance

Application circuits VCO coupling

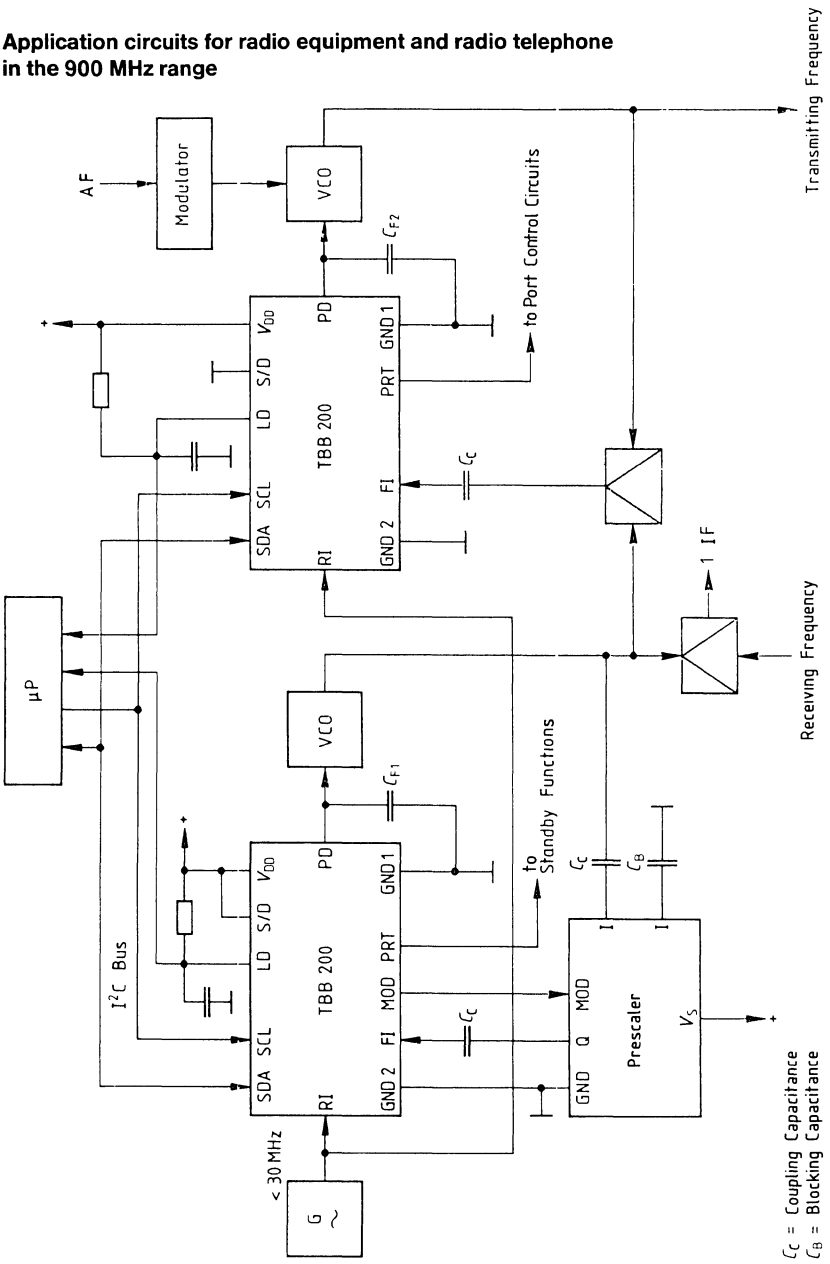


Operation without voltage doubler (status bit 7 = 0)



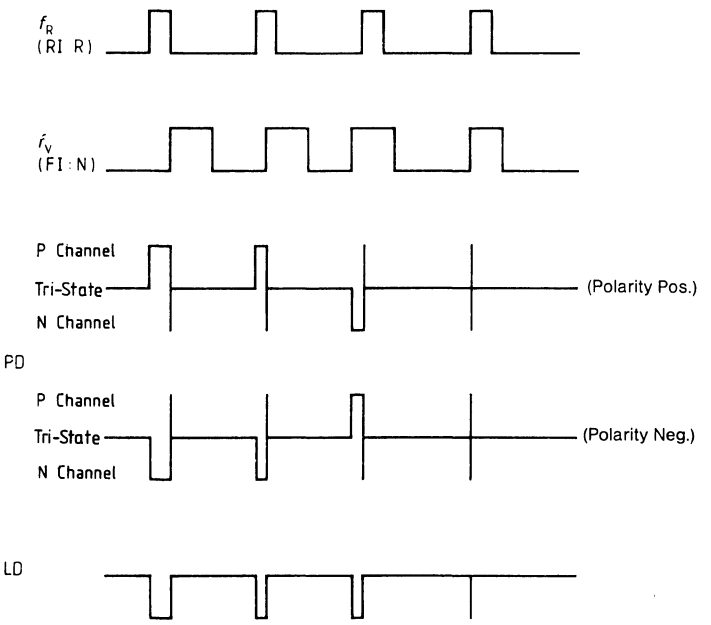
Operation with voltage doubler (status bit 7 = 1)
C_F: loop filter capacitance

Application circuits for radio equipment and radio telephone in the 900 MHz range



Pulse diagram

Phase detector



DIP 22

The TBB 469 is an FM narrow-band IC particularly intended for radio receivers. It is suited for the conversion, limiting, demodulation, and AF processing of an FM-modulated signal.

The input signal is routed via an RF amplifier to a crystal-controlled mixer. The IF signal is routed via an external selection to an adjustable limiter amplifier followed by a coincidence demodulator. The AF signal is routed via a low pass to an AF amplifier. Gain and frequency response of the first amplifier can be set externally. The second amplifier contains the volume control and a muting input for additional field strength-dependent regulation.

Maximum ratings

		Lower limit	Upper limit	
Supply voltage	V_S	0	15	V
Load current of V_{stab}	I_{stab}	0	50	µA
Junction temperature	T_j		125	°C
Storage temperature	T_{stg}	−55	125	°C
Thermal resistance (system-air)	$R_{th\,SA}$		70	K/W

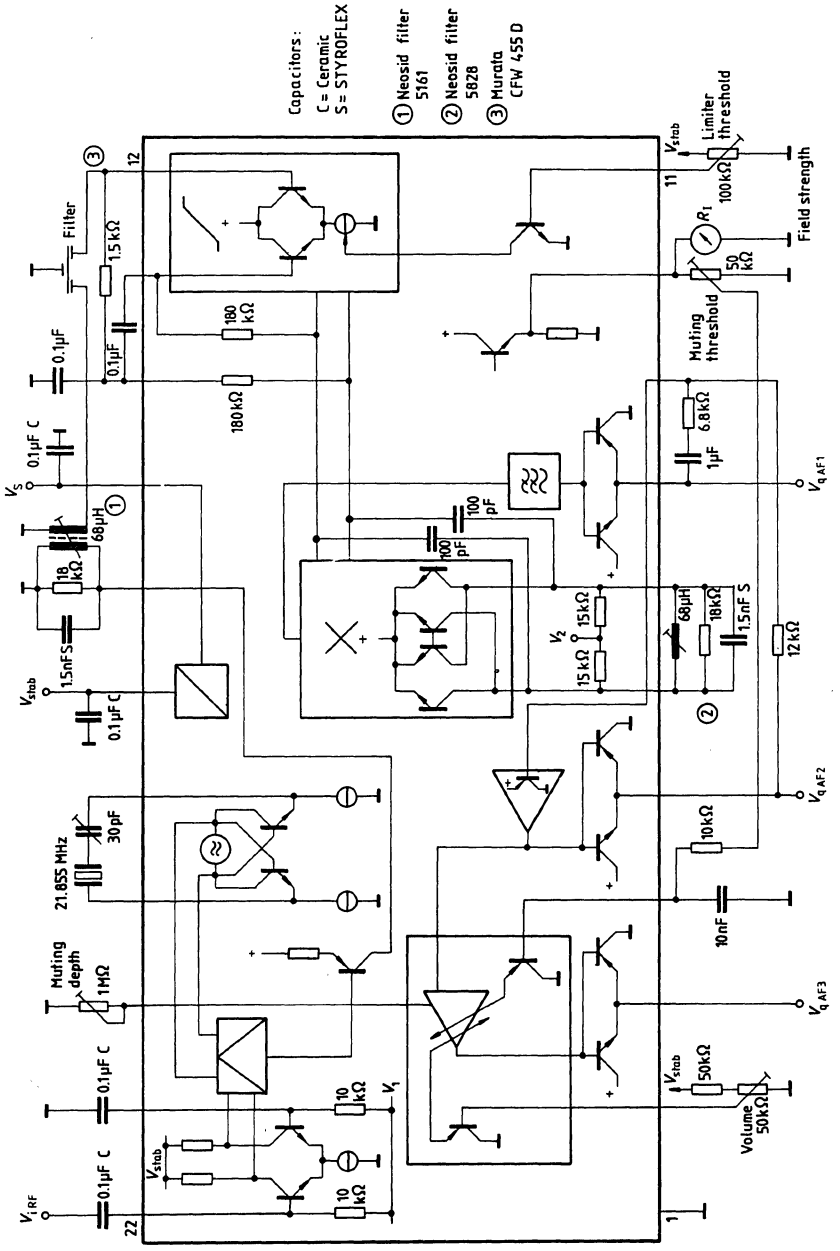
Operating range

Supply voltage	V_S	3	12	V
Ambient temperature	T_{amb}	−30	80	°C

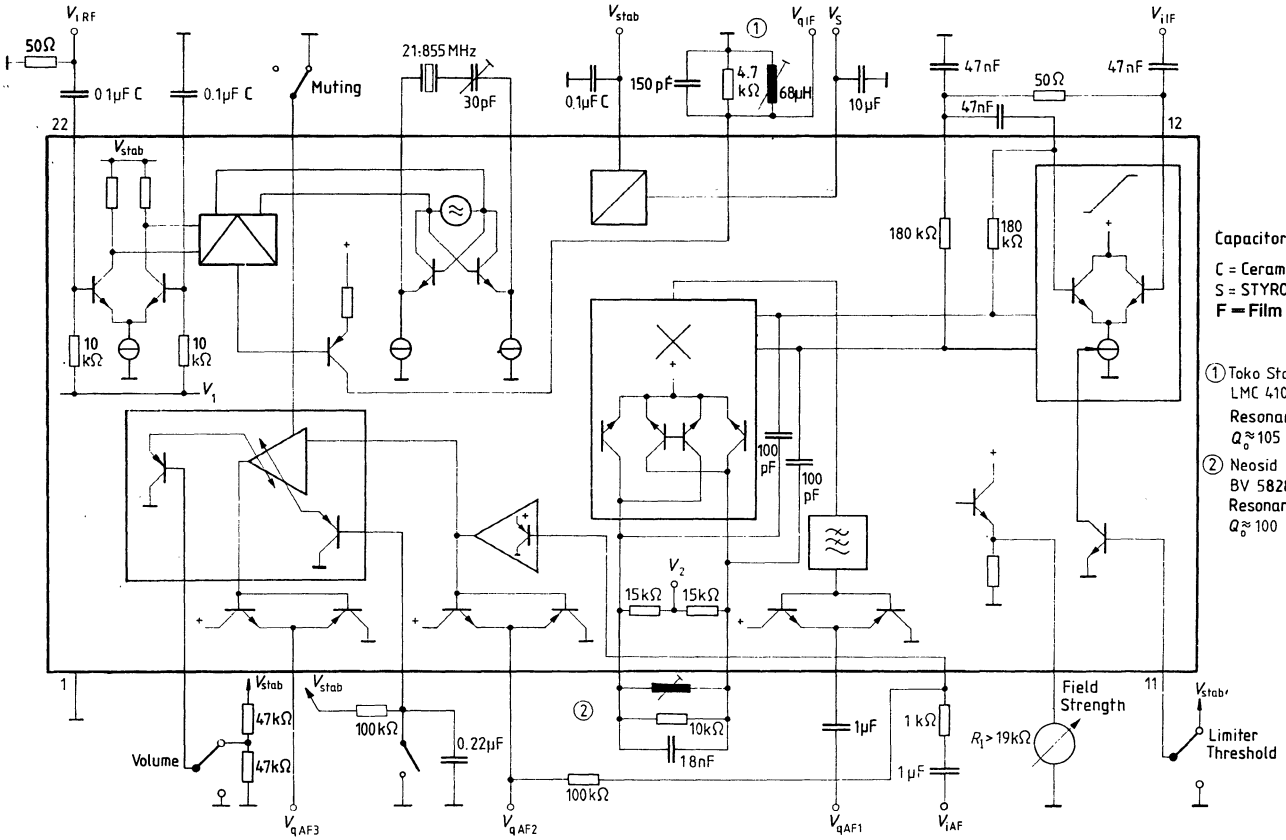
Characteristics $V_S = 4.5$ V; $T_A = -30$ °C to 60 °C		Test conditions	Lower limit	typ	Upper limit	
Supply current	I_S			3.0	5.0	mA
Reference voltage	V_{stab}		1.9	2.2	2.5	V
RF prestage						
Voltage gain	G_V	$f_I = 10...50$ MHz[1] (−3 dB)	36	42	48	dB
Input impedance	Z_i			10//3		kΩ//pF
Noise figure	NF			6		dB
IF limiter amplifier at $\Delta f = \pm 2.8$ kHz, $f_{i\,IF} = 455$ kHz $f_{mod} = 1$ kHz, $V_{i\,IF\,rms} = 10$ mV; Q factor approx. 15:						
Input resistance	R_I			20		kΩ
IF bandwidth	B_{IF}	$V_{qAF1} = -3$ dB	500			kHz
Limiter threshold	$V_{lim\,rms}$			10	20	µV
Setting range of the limiter threshold	ΔV_{lim}	$V_{10} = 0$ V/V_{stab}	14	20	22	dB
AM suppression	AMS	$m = 30\%$	40			dB
Signal-to-noise ratio	$a_{S/N}$			40		dB
Field strength	V_{10}	$V_{i\,IF} = 0$ V			100	mV
	V_{10}	$V_{i\,IF} = 10$ mV	0.8	1.2		V
AF output voltage	V_{QAF1}		30	60		mV
Min. load resistance	R_{q1}		300			Ω
AF bandwidth	B_{AF}	$V_{qAF1} = -3$ dB	20	35		kHz
Total harmonic distortion	THD			1	2	%
AF amplifier 2						
Voltage gain	G_V	$V_{i\,AF} = 1$ mV	31	37	43	dB
Min. load resistance	R_{q2}		1			kΩ
Input impedance	R_I		10			kΩ
Signal-to-noise ratio	$a_{S/N}$			40		dB
Total harmonic distortion[1]	THD			2		%
AF amplifier 3						
Voltage gain	G_V	$V_2 = 0$ V, $V_{11} = 1$ V		10		dB
Max. output voltage	$V_{q\,AF3\,rms}$	$THD = 10\%$			300	mV
Min. load resistance	R_{q3}		5			kΩ
Total harmonic distortion	THD			2		%
Volume control range	ΔG_{vol}			80		dB
Muting depth	M	$V_4 = 0$ V/1 V				
		$R_{mute} = \infty$	3	6	10	dB
		$R_{mute} = 0$	20	26	40	dB
Disturbance voltage in acc. with DIN 45405[2]	V_d	$V_2 = 1/2\ V_{stab}$		30		μV_{OS}

1) dependent on external components
2) AQL = 2.5

Application circuit



Measurement circuit



Capacitors :

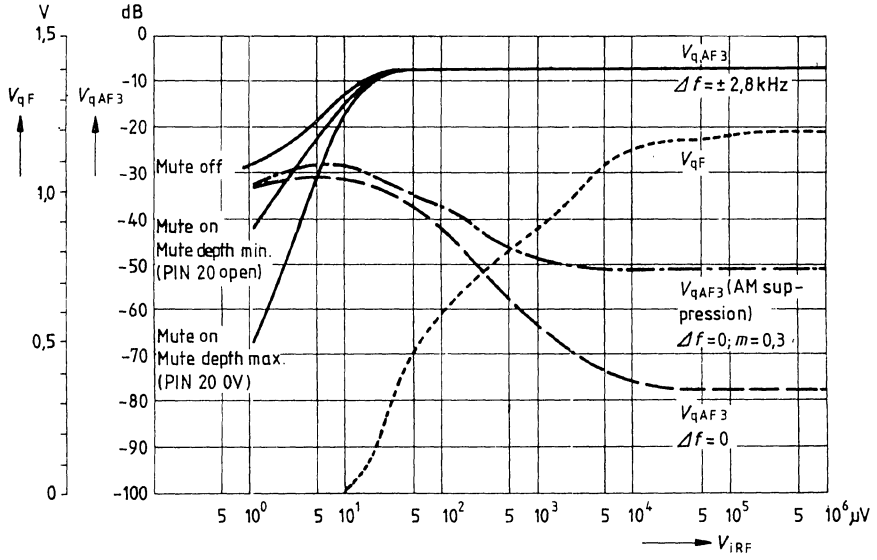
C = Ceramic
S = STYROFLEX
F = Film

① Toko Std. Coil LMC 4100A with Resonance: 455 kHz $Q_0 \approx 105$

② Neosid Filter BV 5828 Resonance: 455kHz $Q_0 \approx 100$

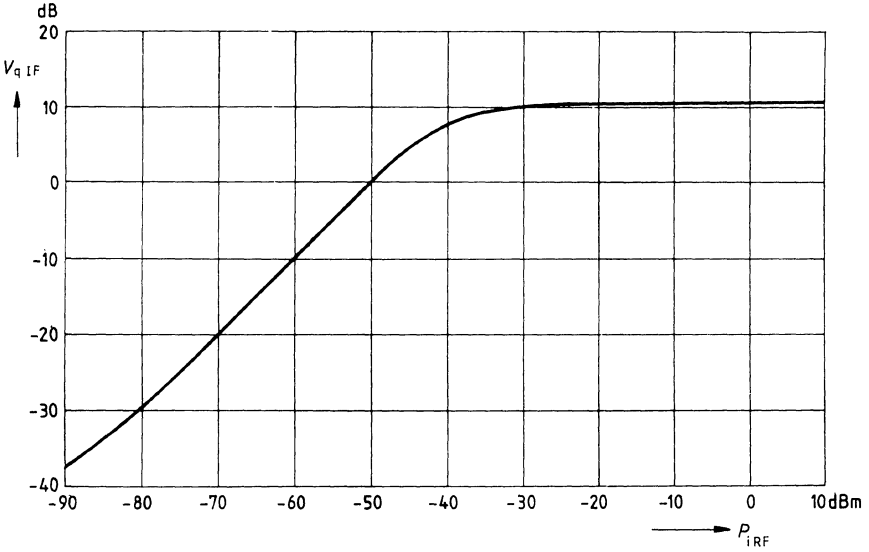
AF Output voltage $V_{q\,AF\,3}$ with reference to 775 mV_{rms} and field strength output voltage V_{qF} versus input voltage $V_{i\,RF}$

$V_S = 4.5$ V, $f_{mod} = 1$ kHz

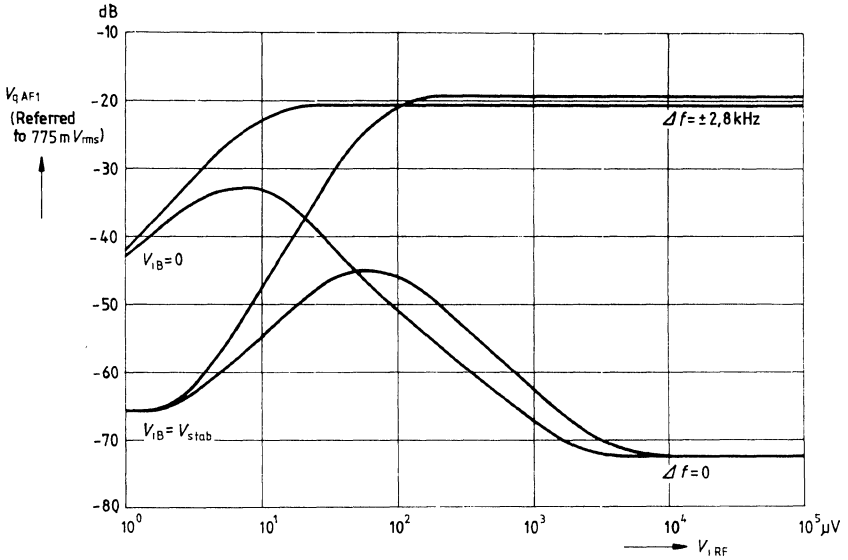


Mixer output voltage $V_{q\,IF}$ with reference to 775 mV_{rms} at 18 kΩ versus input level $P_{i\,RF}$

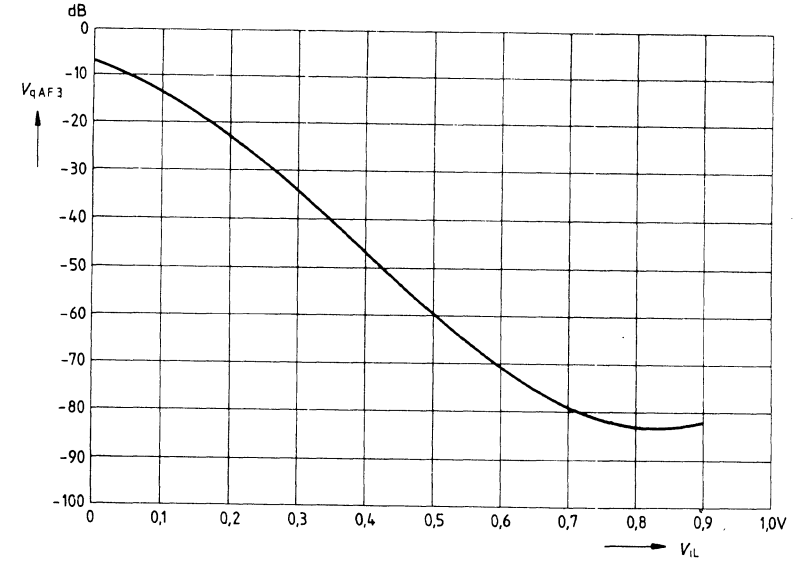
$V_S = 4.5$ V



IF Limiter characteristic
$V_S = 4.5$ V, $f_{mod} = 1$ kHz



AF Output voltage $V_{q\,AF3}$ with reference to 775 mV_{rms} versus control voltage V_{iL}
$V_S = 4.5$ V, $f_{mod} = 1$ kHz



DIP 16

The TBB 1469 is an FM narrow-band IC particularly intended for radio receivers. It is suited for the conversion, limiting, demodulation, and AF processing of an FM-modulated signal. The input signal is routed via an AF amplifier to a crystal-controlled mixer. The IF signal is routed via an external selection to a limiter amplifier followed by a coincidence demodulator. The AF signal is routed via a low pass to an externally adjustable AF amplifier. ESD protective diodes are internally connected to the RF inputs.

Maximum ratings

		Lower limit	Upper limit	
Supply voltage	V_S	0	15	V
Load current	I_{stab}	0	50	µA
Junction temperature	T_j		125	°C
Storage temperature	T_{stg}	−40	125	°C
Thermal resistance (system-air)	$R_{th\,SA}$		85	K/W

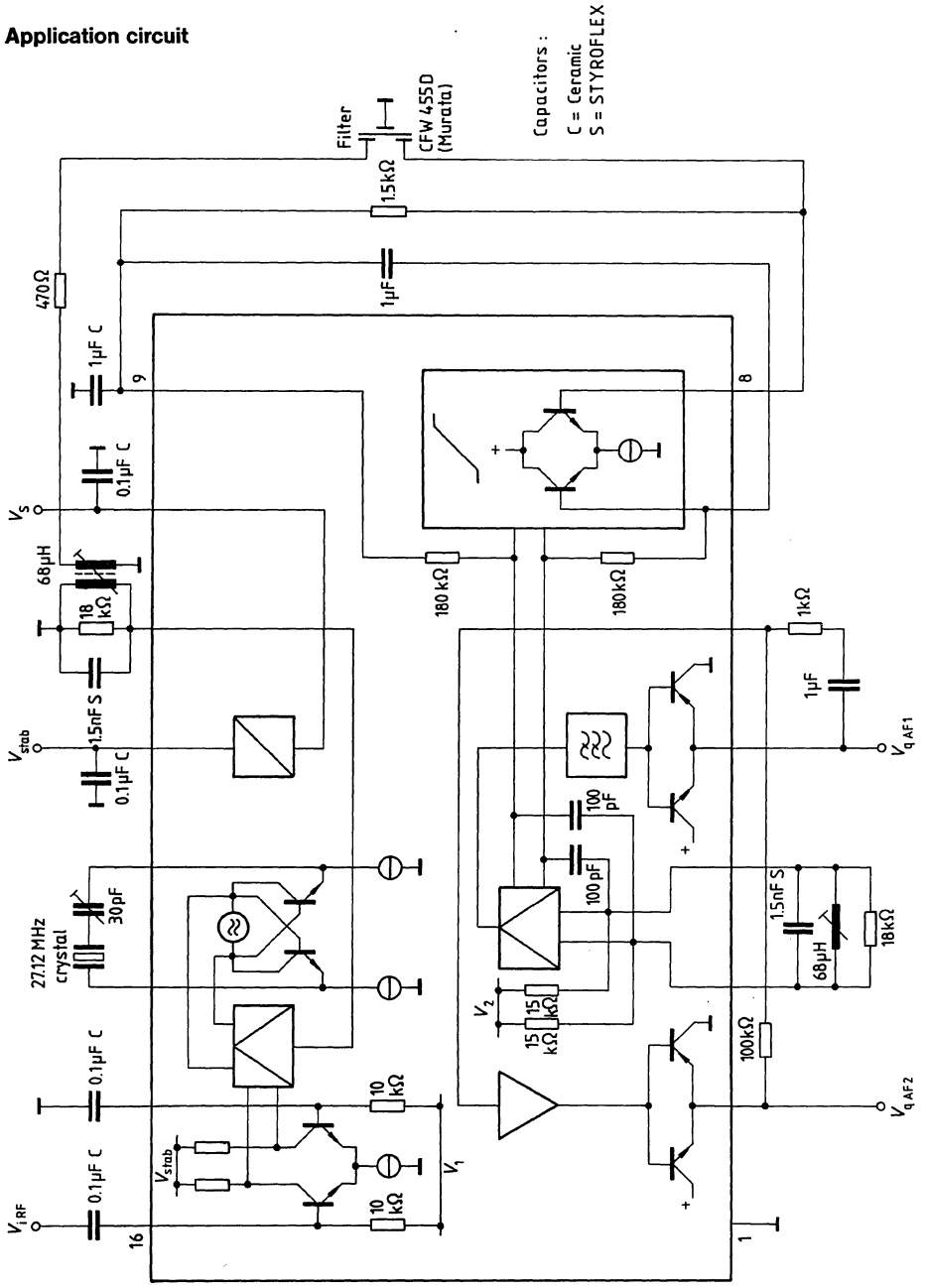
Operating range

Supply voltage	V_S	3	12	V
Ambient temperature	T_{amb}	−30	80	°C

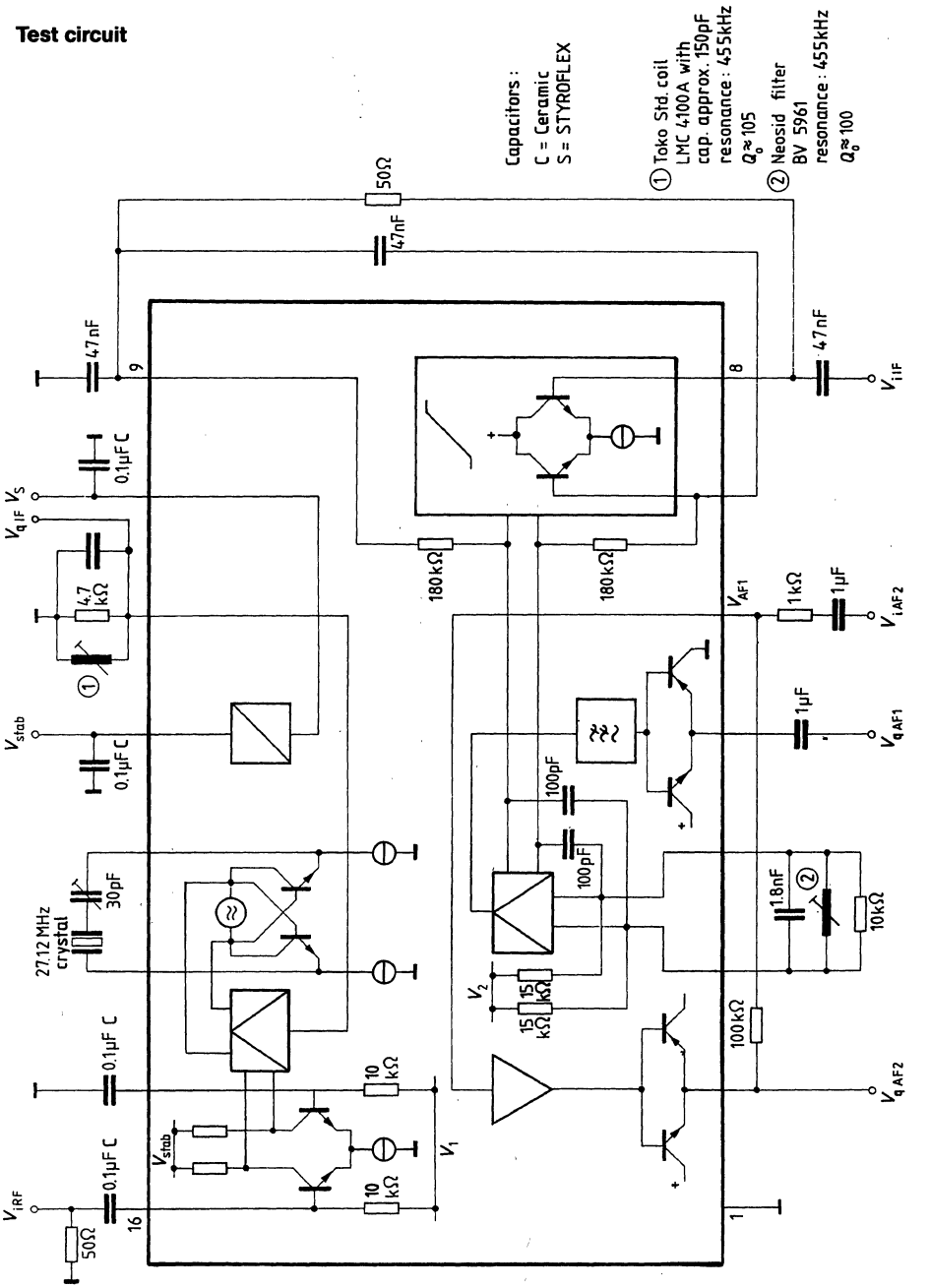
Characteristics V_S=4.5V; T_{amb}=−30 °C to 60 °C		Test conditions	Lower limit	typ	Upper limit	
Supply current	I_S			2.7	4.0	mA
Reference voltage	V_{stab}		1.4	1.9	2.6	V
RF prestage						
Voltage gain	G_V	f_i = 10...50 MHz[1] (−3 dB)	36	42	48	dB
Input impedance	Z_i			10//3		kΩ//pF
Noise figure	NF			6		dB
IF limiter amplifier at $\Delta f = \pm$ 2.8 kHz, $f_{i\,IF}$ = 455 kHz f_{mod} = 1 kHz, $V_{i\,IF\,rms}$ = 10 mV; Q factor approx. 15						
Input resistance	R_i			20		kΩ
IF bandwidth	B_{IF}	V_{qAF1} = −3 dB	500			kHz
Limiter threshold	$V_{lim\,rms}$			10	30	µV
AM suppression	AMS	m = 30%	40			dB
AF output voltage	V_{qaF1}		30	60		mV
Min. load resistance	R_q		300			Ω
Total harmonic distortion	THD			1	2	%
Signal-to-noise ratio	$a_{S/N}$			40		dB
AF bandwidth	B_{AF}	V_{qAF1} = −3 dB	20	35		kHz
AF amplifier						
Voltage gain	G_V	V_{iAF} = 1 mV	31	37	43	dB
Min. load resistance	R_L		1			kΩ
Input impedance	R_i		10			kΩ
Signal-to-noise ratio	$a_{S/N}$			40		dB

1) dependent on external components

Application circuit



Test circuit



SO-20L

The TBB 2469 G is an FM narrow-band IC particularly intended for radio receivers. It is suited for the conversion, limiting, demodulation, and AF processing of an FM-modulated signal.

The input signal is routed via an HF amplifier to a crystal-controlled mixer. The IF signal is routed via an external selection, to a limiter amplifier followed by a coincidence demodulator. The AF signal is routed via a low pass to an AF amplifier. Gain and frequency response of the first amplifier can be set externally. The second amplifier contains the volume control.

Maximum ratings

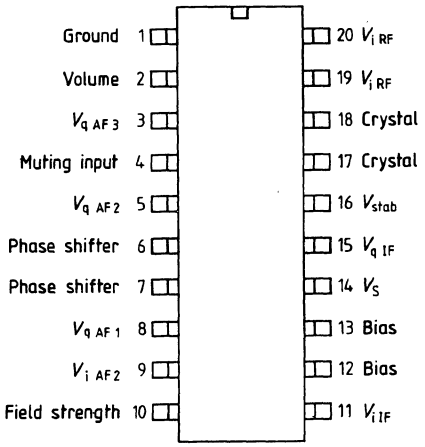
		Lower limit	Upper limit	
Supply voltage	V_S	0	15	V
Load current of V_{stab}	I_{Stab}	0	50	µA
Junction temperature	T_j		125	°C
Storage temperature	T_{stg}	−40	125	°C
Thermal resistance (system-air)	$R_{th\,SA}$		120	K/W

Operating range

Supply voltage	V_S	3	12	V
Ambient temperature	T_{amb}	−30	80	°C

Pin configuration

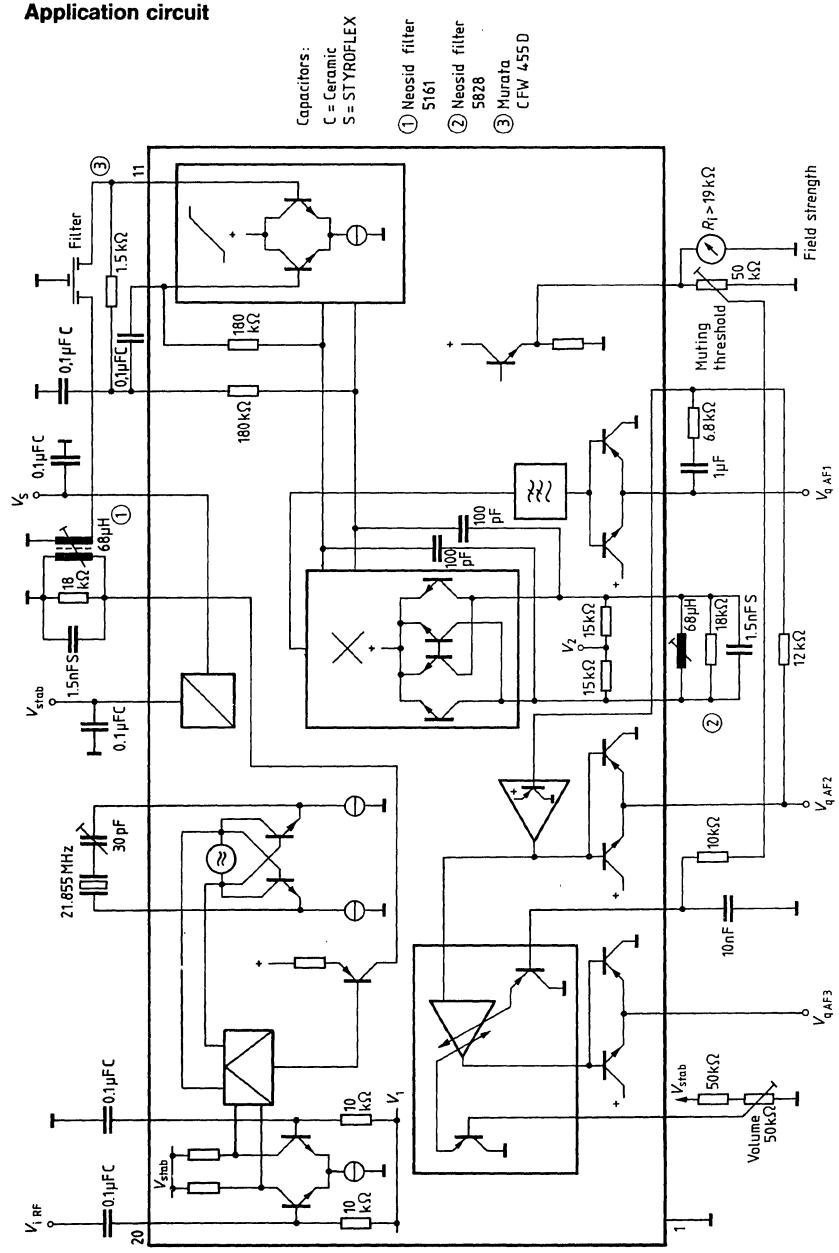
top view



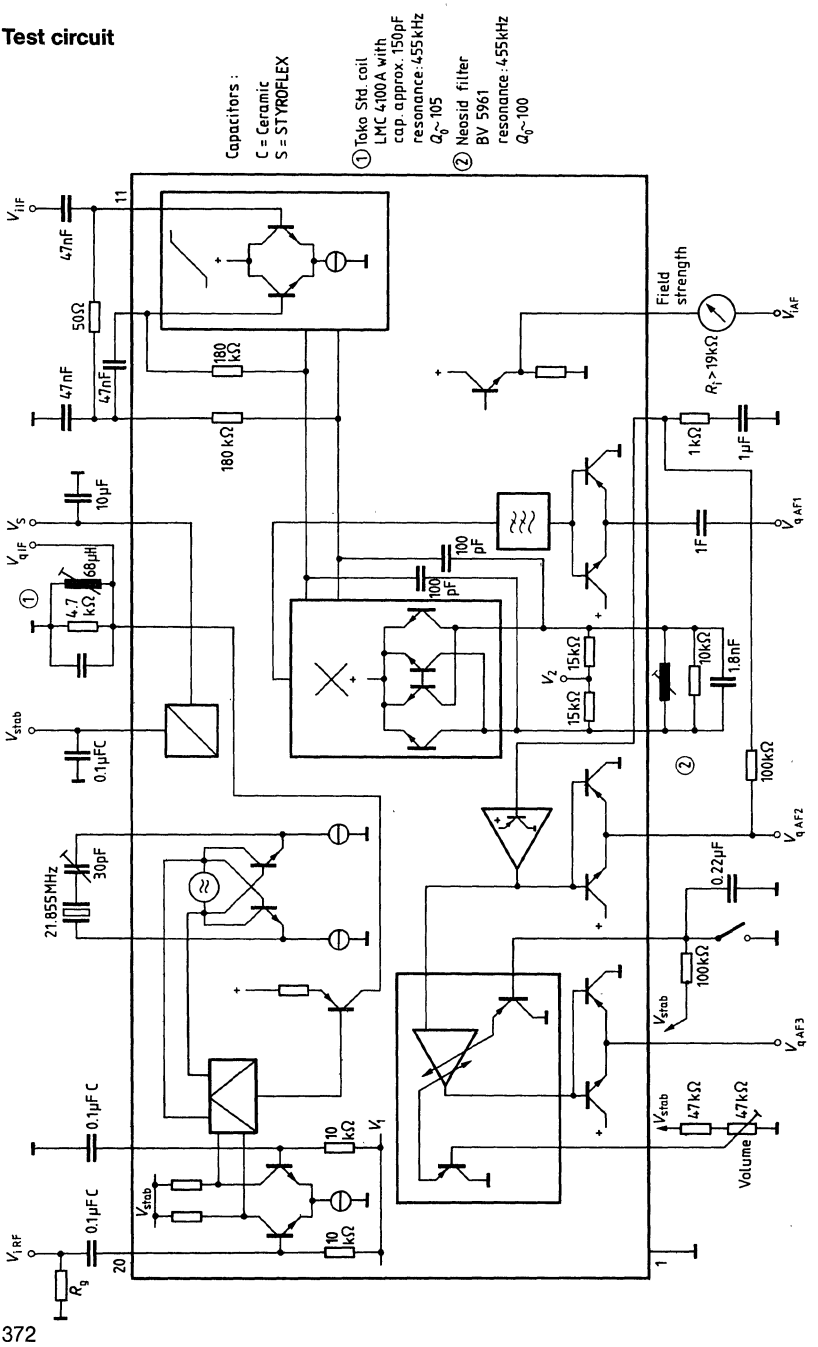
Characteristics at V_S=4.5V, T_{amb}=−30 °C to 60 °C		Test conditions	Lower limit	typ	Upper limit	
Current consumption	I_S			3.0	5.0	mA
Reference voltage	V_{stab}		1.4	1.9	2.6	V
RF prestage						
Voltage gain	G_V	f_i = 10...50 MHz[1] (−3 dB)	36	42	48	dB
Input impedance	Z_i			10//3		kΩ//pF
Noise figure	NF			6		dB
IF limiter amplifier at $\Delta f = \pm$ 2.8 kHz, $f_{i\,IF}$ = 455 kHz[1] f_{mod} = 1 kHz, $V_{i\,IF\,rms}$ = 10 mV, Q factor appr. 15						
Input resistance	R_i			20		kΩ
IF bandwidth	B_{IF}	$V_{q\,AF1}$ = −3 dB	500			kHz
AM suppression	AMS	m = 30%	40			dB
Signal-to-noise ratio	$a_{S/N}$			40		dB
Field strength	V_{10}	$V_{i\,IF}$ = 0 V			100	mV
	V_{10}	$V_{i\,IF}$ = 10 mV		1.9		V
AF output voltage	$V_{q\,AF1}$		30	60		mV
Min. load resistance	R_{q1}		300			Ω
AF bandwidth	B_{AF}	$V_{q\,AF1}$ = −3 dB	20	35		kHz
Total harmonic distortion[1]	THD			1	2	%
AF amplifier 2						
Voltage gain	G_V	$V_{i\,AF1}$ = 1 mV		37		dB
Min. load resistance	R_{q2}		1			kΩ
Input impedance	R_i		10			kΩ
Signal-to-noise ratio	$a_{S/N}$			40		dB
Total harmonic distortion[1]	THD			2		%
AF amplifier 3						
Voltage gain	G_V	V_2 = 0 V, V_{11} = 1 V		10		dB
Max. output voltage	$V_{q\,AF3\,rms}$	THD = 10%			300	mV
Min. load resistance	R_{q3}		5			kΩ
Total harmonic distortion[1]	THD			2		%
Volume control range	ΔG_{vol}			80		dB
Noise voltage in acc. with DIN 45405[2]	V_n	V_2 = 1/2 V_{stab}		20	50	μV_{0s}

1) dependent on external components
2) AQL = 2.5

Application circuit



Test circuit



The TCA 105 contains an oscillator stage, a threshold switch, and two anti-valent output stages. These ICs are especially suitable for application in proximity switches, light barriers, and other contactless switching applications.

Features

- Wide range of supply voltage, 4.5 to 30 V
- High output current, 50 mA
- TTL-compatible
- Triggerable with dc signal

Maximum ratings		**TCA 105; G**	**TCA 105 B**	
Supply voltage	V_S	30	20	V
Output voltage (pin 4, pin 5)	V_Q	30	20	V
Output current	I_Q	50	50	mA
Switching frequency	f_S	40	40	kHz
Input voltage	V_I	≥ 0*)	≥ 0*)	V
Junction temperature	T_j	125	125	°C
Storage temperature range	T_{stg}	−55 to 125	−55 to 125	°C
Thermal resistance (system-air)				
TCA 105, TCA 105 B	$R_{th\ SA}$	115	115	K/W
TCA 105 G	$R_{th\ SA}$	200	200	K/W
Operating range				
Supply voltage	V_S	4.75 to 30	4.75 to 20	V
Ambient temperature	T_A	−25 to 85	−25 to 85	°C
Oscillating frequency	f_{OSC}	1 to 4.5	1 to 4.5	MHz

*) Negative input voltages are not permitted

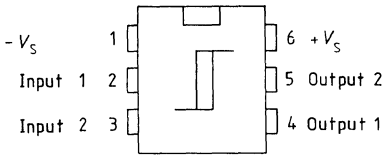
Characteristics

Static measurement, pins 3 and 1 interconnected
$V_S = 12$ V; $T_A = 25$ °C; $R_C = 5.6$ kΩ

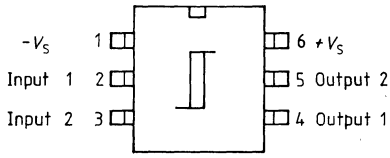
		min	typ	max	
Supply current	I_S		3.4	5	mA
Input threshold voltage with compensation resistor R_C	V_I	300	400	480	mV
Input threshold current	I_I		−60		µA
Hysteresis	V_{hy}	20	35	50	mV
L output voltage ($I_Q = 16$ mA)	V_{QL}		0.25	0.35	V
H output voltage	V_{QH}		corresponds to V_S		
Reverse current, $V_S = 30$ V and/or 20 V	I_{QH}			60	µA
L output voltage ($I_Q = 50$ mA)	V_{QL}		0.7	1.15	V
Switching time in TTL operation ($I_Q = 16$ mA)	t		3		µs

Pin configurations

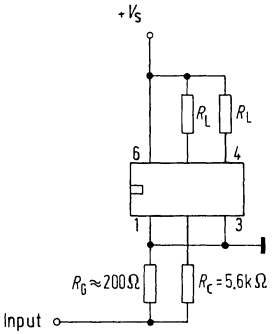
TCA 105, TCA 105 B



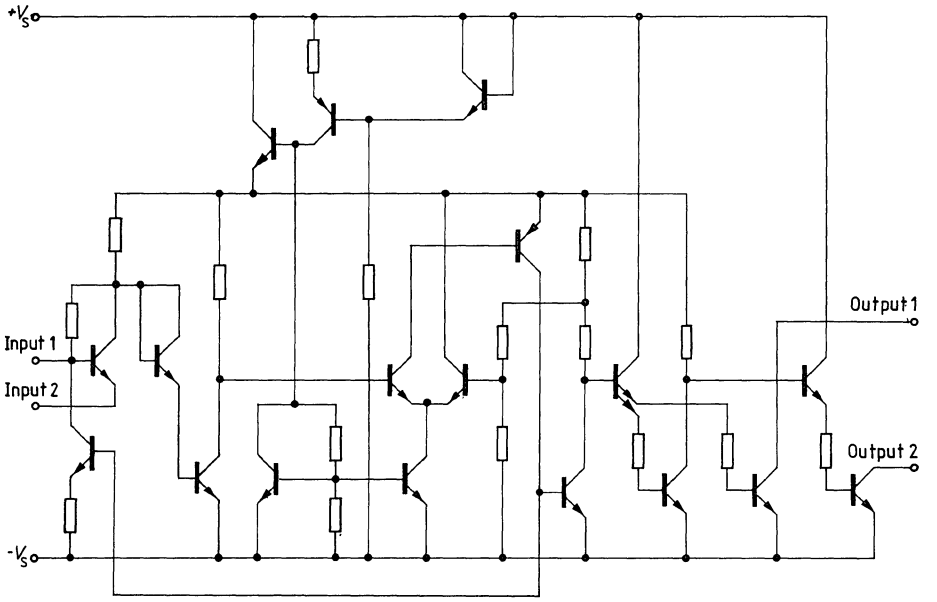
TCA 105 G



Measurement circuit

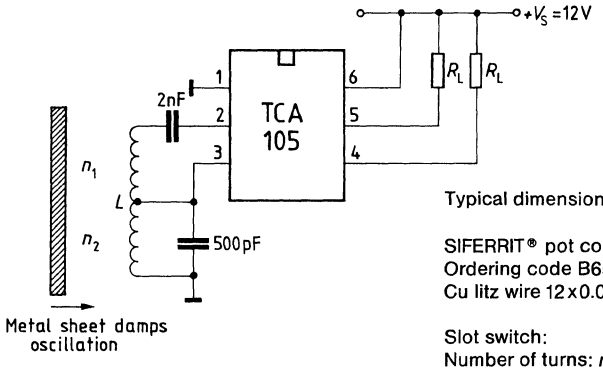


Circuit diagram



Application examples

Inductive slot switch or proximity switch



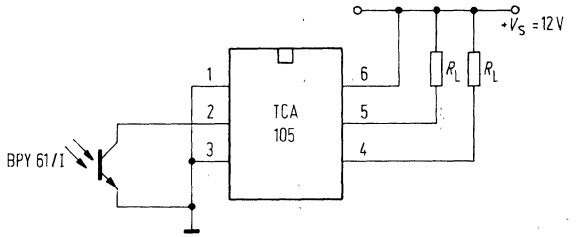
Typical dimensioning values:

SIFERRIT® pot cores, 9 mm dia.
Ordering code B65935-A-X25
Cu litz wire 12 x 0.04 mm

Slot switch:
Number of turns: $n = 2 \times 25$
Distance between pot core halves:
2.5 to 3.5 mm

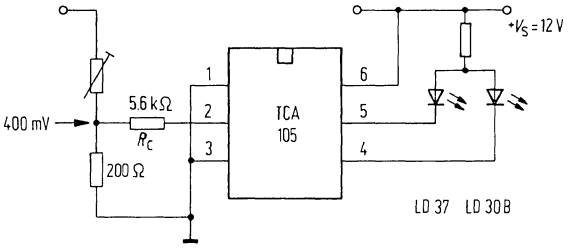
Proximity switch:
Number of turns: $n_1 = 8$, $n_2 = 40$
Distance: 2 to 3 mm

Light-operated switch (switching amplifier for phototransistor BPY 61)

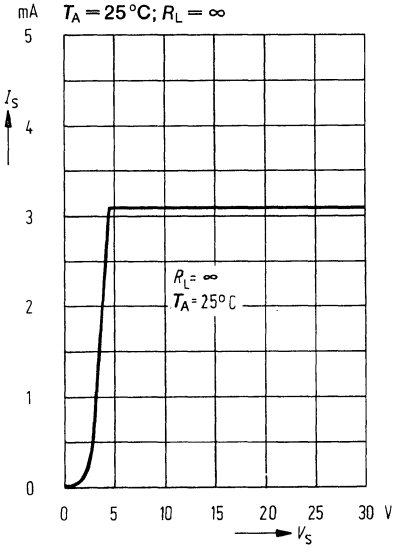


Application example

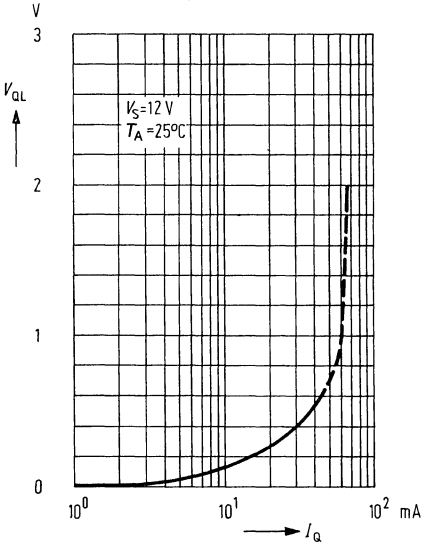
Voltage monitor



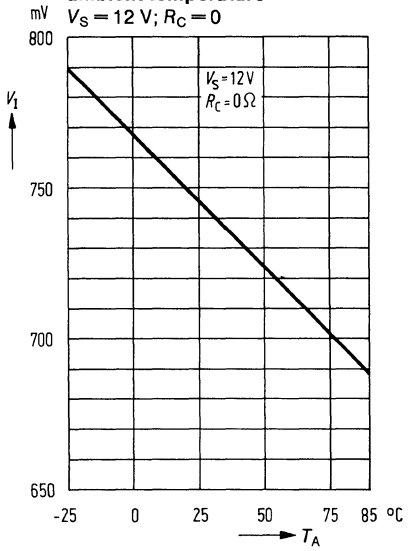
Current consumption
Supply current versus supply voltage
$T_A = 25\,°C$; $R_L = \infty$



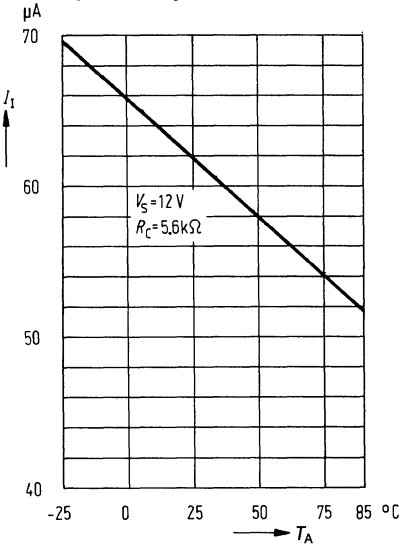
L output voltage versus output current
$T_A = 25\,°C$; $V_S = 12$ V



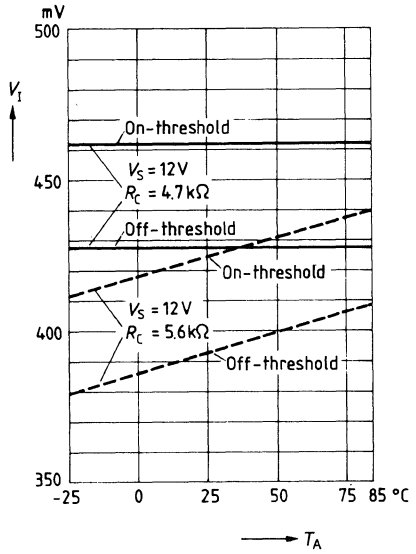
Switching threshold Input voltage versus ambient temperature



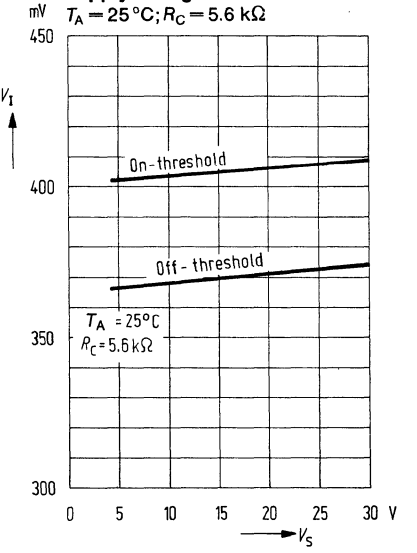
Input current versus ambient temperature
$V_S = 12$ V; $R_C = 5.6$ kΩ



Switching threshold Input voltage versus ambient temperature

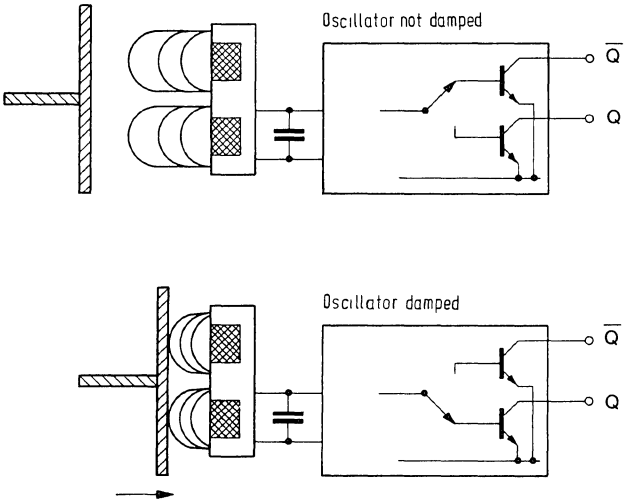


Switching threshold Input voltage versus supply voltage
$T_A = 25$ °C; $R_C = 5.6$ kΩ



This IC is intended for applications in inductive proximity switches. The outputs switch when the oscillation is damped, e.g. by the approach of a metal object.

Operation schematic



Features

- Large supply voltage range
- High output current
- Antivalent outputs
- Adjustable switching distance
- Adjustable hysteresis
- Turn-on delay

Maximum ratings

Supply voltage	V_S	30	V
Output voltage	V_Q	30	V
Output current	I_Q	50	mA
Junction temperature	T_j	125	°C
Storage temperature range	T_{stg}	−55 to 125	°C
Thermal resistance (system-air) TCA 205 A	$R_{th\,SA}$	85	K/W

Operating range

Supply voltage	V_S	4.75 to 30	V
Ambient temperature	T_A	−25 to 85	°C

Characteristics

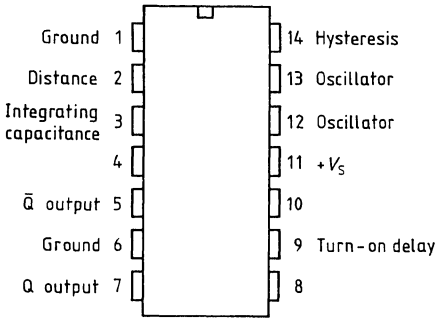
$V_S = 12$ V; $T_A = 25$ °C

		Test conditions	Lower limit B	typ	Upper limit A	
Open-loop supply current consumption	I_S	open pins		1	2	mA
L output voltage per output	V_{QL}	$I_{QL} = 5$ mA		0.8	1	V
	V_{QL}	$I_{QL} = 50$ mA		1.25	1.5	V
H output current per output	I_{QH}	$V_{QH} = 30$ V			10	µA
Integrating capacitance	C_I			10		nF
Internal resistance at 3	R_{j3}		200	350	660	kΩ
Threshold voltage at 3	V_{S3}			1.3	1.5	V
Distance adjustment (circuit 1)	R_{di}		6			kΩ
Hysteresis adjustment (circuit 1)	R_{hy}		0			kΩ
Distance adjustment (circuit 2)	R_{di}	$R_{hy} \rightarrow \infty$	6[1]			kΩ
Hysteresis adjustment (circuit 2)	R_{hy}	$R_{di} \rightarrow \infty$	6[1]			kΩ
Turn-on delay	t_{don}			200		ms/µF
Oscillating frequency	f_{OSC}		0.015		1.5	MHz
Switching frequency without C_I	f_s				5	kHz

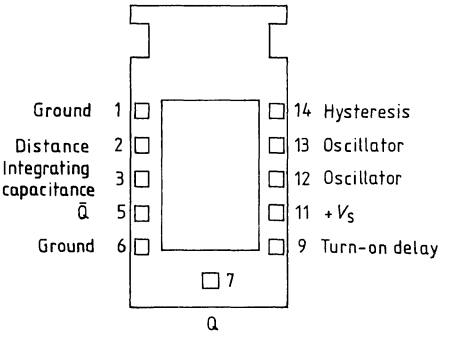
1) Parallel connection of R_{hy} to R_{di} may at least amount to 6 kΩ

Pin configurations

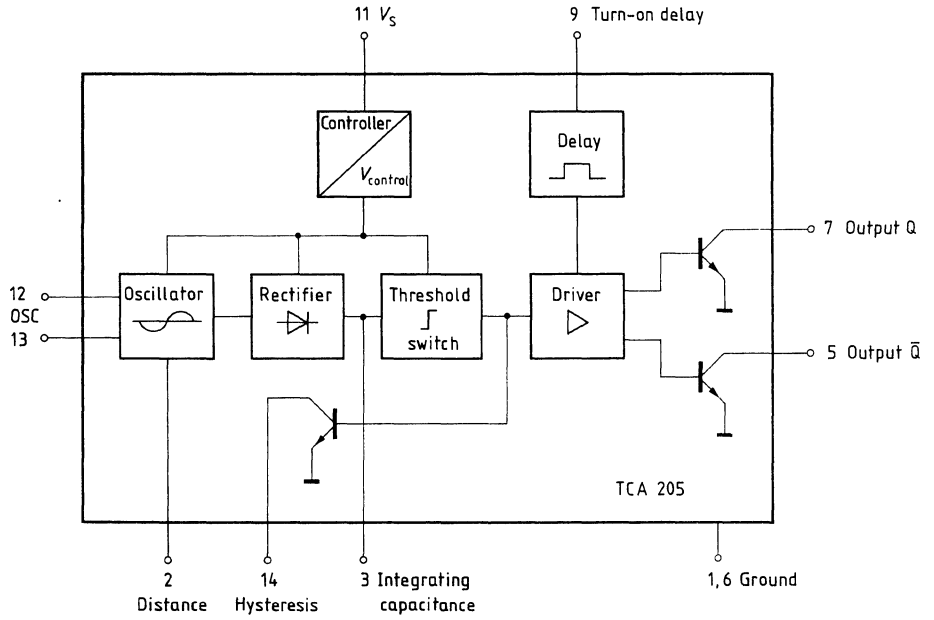
TCA 205 A



TCA 205 K

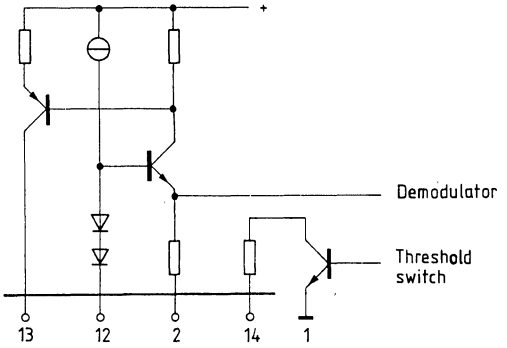


Block diagram

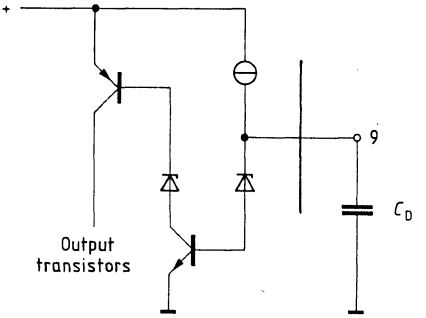


Schematic circuit diagrams

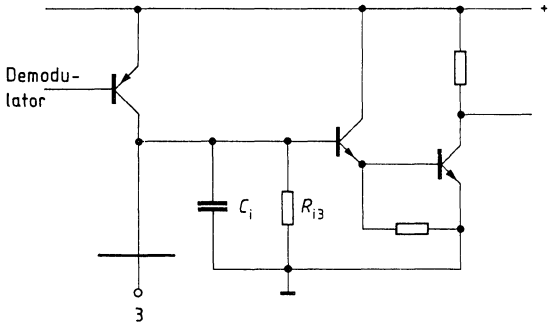
Oscillator



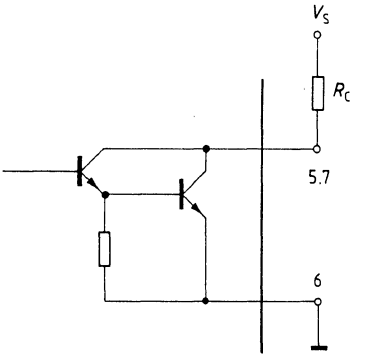
Turn-on delay



Integrating capacitor

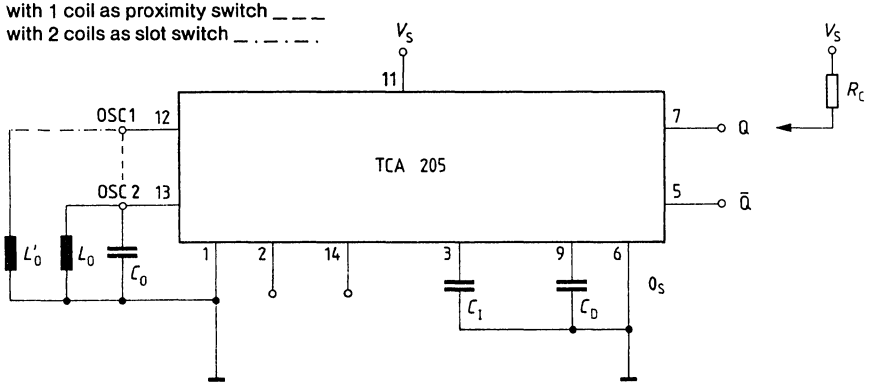


Outputs



Application circuit

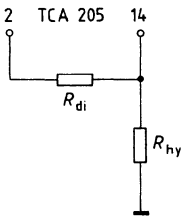
with 1 coil as proximity switch _ _ _
with 2 coils as slot switch _ . _ . _ .



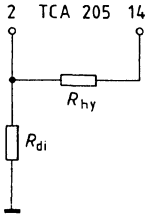
L_0, C_0	oscillator
R_{di}	distance adjustment
R_{hy}	hysteresis adjustment
C_I	integrating capacitor
C_D	delay capacitor

The resistance of distance and hysteresis R_{di} and R_{hy}, for proximity switch TCA 205 A; K may be applied as follows:

1. Series hysteresis



2. Parallel hysteresis

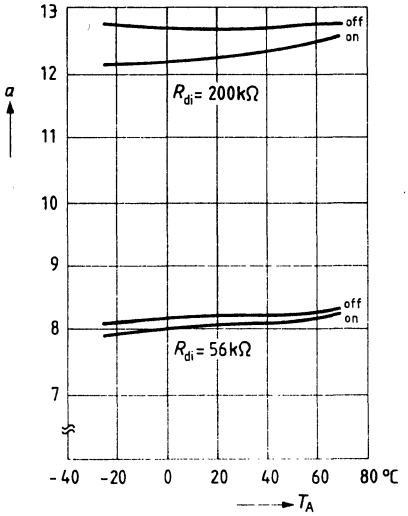


Circuit 1 is more suitable for proximity switches with oscillator frequencies of $f > 200$ kHz to 300 kHz, and small distances. Circuit 2 is more favorable for AF proximity switches having larger distances. This is due to the lower R_{hy} values enabled by circuit 1 (min. 0 Ω) compared with circuit 2 (min. 6 kΩ). Starting at frequencies of 200 kHz, high R_{hy} values effect in addition to the hysteresis also the oscillator phase. Practical applications, however, require little phase response to receive a clear evaluation.

Application example for a proximity switch

Coil data	pot core B65939-A-X22 coil former B65940-A-M1 Ø = 25 mm x 8.9 mm L = 642 µH n = 100 CuLS 30 x 0.05	
Measuring plate	30 mm x 30 mm x 1 mm, Fe	
Circuitry	R_{di} = 56 to 200 kΩ, metal layer R_{hy} = ∞ C_0 = 1500 pF, STYROFLEX f = 162 kHz	circuit 2

Switching distance versus ambient temperature



DIP 14; SO-14
DIP 8; SO-8

The devices TCA 305 and TCA 355 contain all the functions necessary to design inductive proximity switches. By approaching a standard metal plate to the coil, the resonant circuit is damped and the outputs are switched.

Operation schematic: see TCA 205

The types TCA 305 and TCA 355 have been developed from the type TCA 205 and are outstanding for the following characteristics:

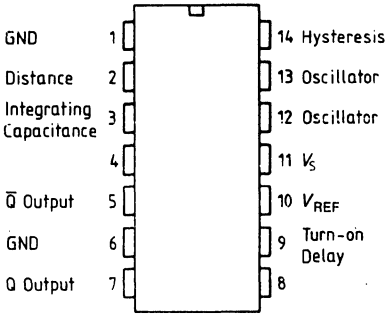
- Lower open-loop current consumption; $I_S < 1$ mA
- Lower output saturation voltage
- The temperature dependency of the switching distance is lower and the compensation of the resonant circuit TC (temperature coefficient) is more easily possible.
- The sensitivity is greater, so that larger switching distances are possible and coils of inferior quality can be used.
- The switching hysteresis remains constant as regards temperature, supply voltage and switching distance.
- The TCA 305 even functions without external integrating capacitance. With an external capacitance (or with RC combination) good noise suppression can be achieved.
- The outputs are temporarily short-circuit proof (approx. 10 s to 1 min depending on the package)
- The outputs are disabled when $V_S <$ approx. 4.5 V and they are enabled when the oscillator is working steadily (from $V_{S\,min} = 5$ V)
- Higher switching frequencies can be obtained.
- Miniature packages

Logic functions

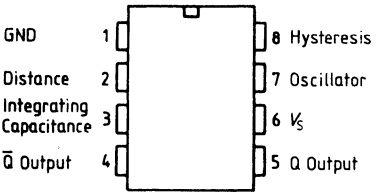
Oscillator	Outputs	
	Q	$\overline{Q}$
not damped	H	L
damped	L	H

Pin configuration

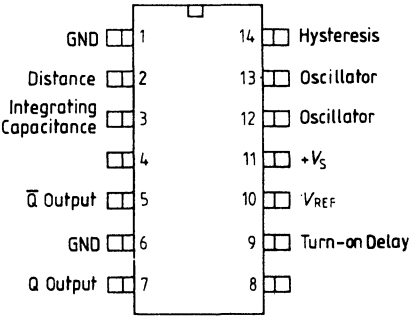
TCA 305 A



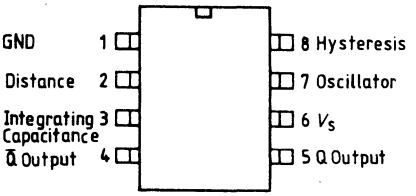
TCA 355 B



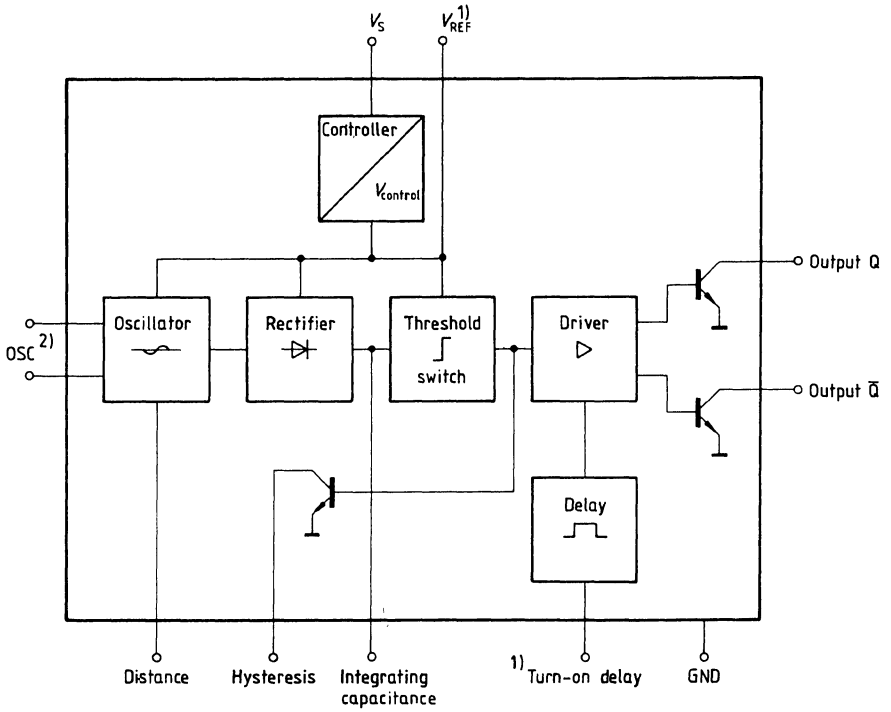
TCA 305 G



TCA 355 G



Block diagram



1) TCA 305 only
2) Connected internally in case of TCA 355

Maximum ratings

Supply voltage		V_S	35	V
Output voltage		V_Q	35	V
Output current		I_Q	50	mA
Distance, hysteresis resistance		R_{di}, R_{hy}	0	Ω
Capacitances		C_I, C_d	5	µF
Junction temperature		T_j	125	°C
Storage temperature range		T_{stg}	−55 to 125	°C
Thermal resistance (system-air)	TCA 305 A	$R_{th\,SA}$	85	K/W
	TCA 305 G	$R_{th\,SA}$	140	K/W

Operating range

Supply voltage	V_S	5 to 30	V
Oscillator frequency	f_{OSC}	0.015 to 1.5	MHz
Ambient temperature	T_A	−25 to 85	°C

Characteristics

$V_S = 12$ V, $T_A = -25$ °C to 85 °C

		Test conditions	Lower limit B	typ	Upper limit A	
Open-loop current consumption	I_S	outputs open		0.6	1.0	mA
Reference voltage	V_{ref}	$I_{ref} < 10$ µA		3.2		V
L output voltage	V_{QL}	$I_{QL} = 5$ mA		0.04	0.15	V
per output	V_{QL}	$I_{QL} = 25$ mA		0.10	0.35	V
	V_{QL}	$I_{QL} = 50$ mA		0.22	0.75	V
H output current per output	I_{QH}	$V_{QH} = 30$ V			10	µA
Threshold at 3	V_{S3}			2.1		V
Hysteresis at 3	V_{hy}		0.4	0.5	0.6	V
Turn-on delay	$t_{d\,on}$	$T_A = 25$ °C	−25%	600	−25%	ms/µF
Switching frequency w/o C_I	f_s				5	kHz

Maximum ratings

Supply voltage		V_S	35	V
Output voltage		V_Q	35	V
Output current		I_Q	50	mA
Distance, hysteresis resistance		R_{di}, R_{hy}	0	Ω
Junction temperature		T_j	125	°C
Storage temperature range		T_{stg}	−55 to 125	°C
Thermal resistance (system-air)	TCA 355 B	$R_{th\,SA}$	135	K/W
	TCA 355 G	$R_{th\,SA}$	200	K/W

Operating range

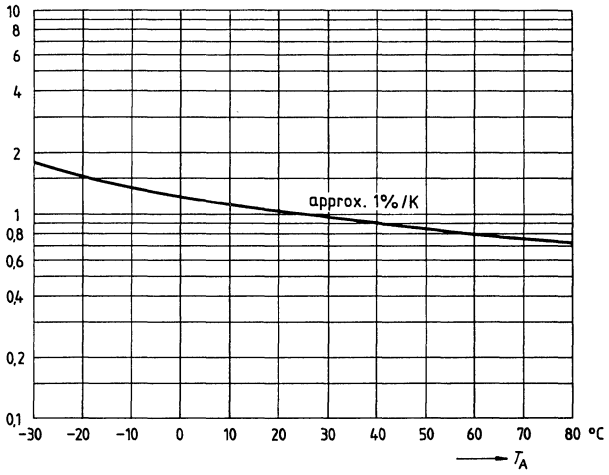
Supply voltage	V_S	5 to 30	V
Oscillator frequency	f_{OSC}	0.015 to 1.5	MHz
Ambient temperature	T_A	−25 to 85	°C

Characteristics

$V_S = 12$ V; $T_A = -25$ to 85 °C

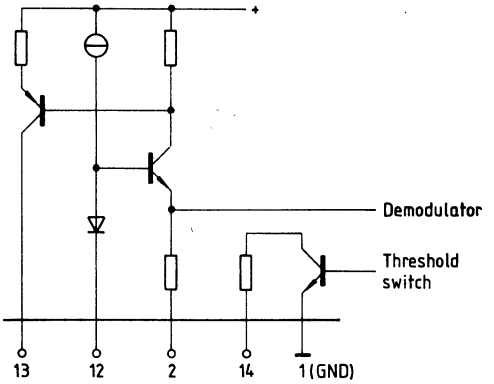
		Test conditions	Lower limit B	typ	Upper limit A	
Open-loop current consumption	I_S	outputs open		0.6	1.0	mA
L output voltage	V_{QL}	$I_{QL} = 5$ mA		0.04	0.15	V
per output	V_{QL}	$I_{QL} = 25$ mA		0.10	0.35	V
	V_{QL}	$I_{QL} = 50$ mA		0.22	0.75	V
H output reverse current per output	I_{QH}	$V_{QH} = 30$ V			10	µA
Threshold at 3	V_{S3}			2.1		V
Hysteresis at 3	V_{hy}		0.4	0.5	0.6	V
Switching frequency w/o C_I	f_s				5	kHz

Standard turn-on delay referred to $T_A = 25$ °C

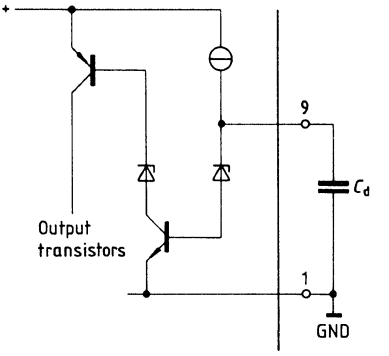


Schematic circuit diagrams

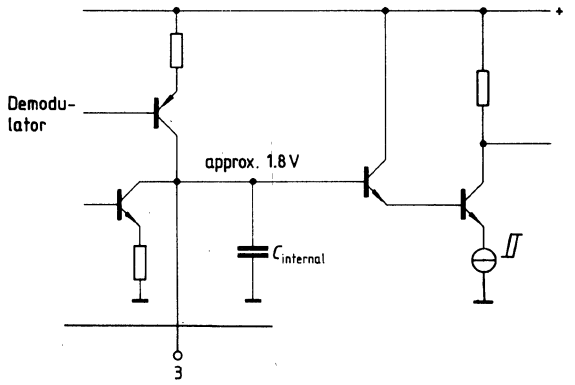
Oscillator



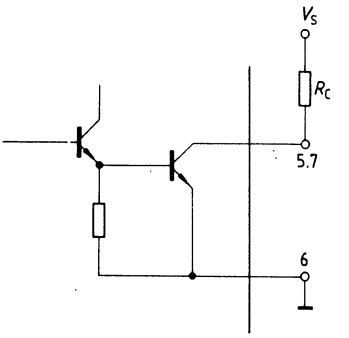
Turn-on delay for TCA 305



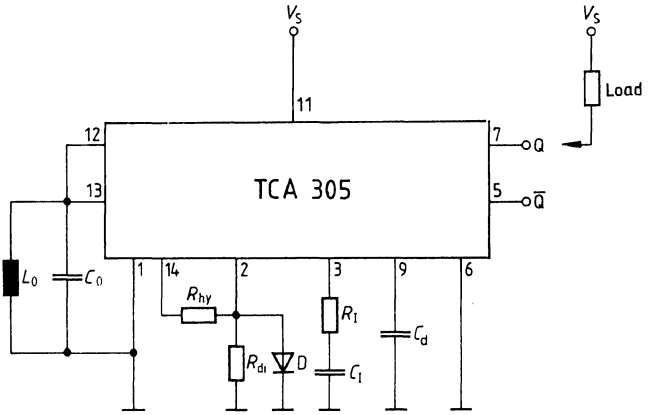
Integrating capacitor

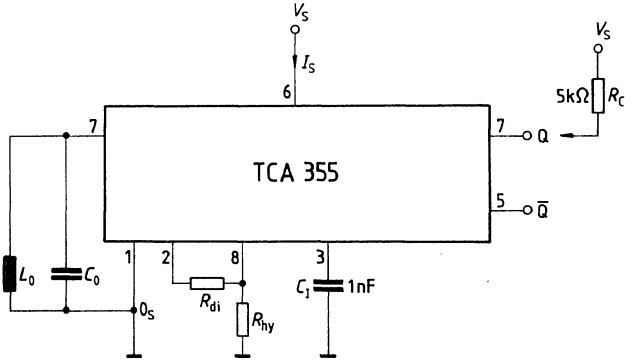


Outputs



Application circuits





L_0, C_0	Resonant circuit
R_{hy}	Hysteresis adjustment
R_{di}	Distance adjustment
D	Temperature compensation of the resonant circuit; possibly with series resistance for the purpose of adjustment. The diode is not absolutely necessary. Whether it is used or not depends on the temperature coefficient of the resonant circuit.
R_I; C_I	Integration element
C_d	Delay capacitor

Dimensioning examples in accordance with CENELEC Standard (flush)

	M 12	M 18	M 30
Ferrite pot core	M33 (7.35x3.6) mm	N22 (14.4x7.5) mm	N22 (25x8.9) mm
Number of turns	100	80	100
Cross section of wire	0.1 CuL	20x0.05	10x0.1
L_0	206 µH	268 µH	585 µH
C_0 (STYROFLEX®)	1000 pF	1.2 nF	3.3 nF
f_{osc}	appr. 350 kHz	appr. 280 kHz	appr. 115 kHz
Sn	4 mm	8 mm	15 mm
R_A (Metal)	8.2 kΩ + 330 Ω	33 kΩ	22 kΩ + 2.7 kΩ
C_d	100 nF	100 nF	100 nF

Note:

At pin 3 (integrating capacitance) we recommend a capacitor of typ. 1 nF. To increase noise immunity this capacitor can be substituted by an RC circuit with, e.g., R_I = 1 MΩ and C_I = 10 nF.

DIP 4

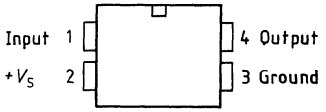
Threshold switches featuring linear, supply voltage-dependent threshold values. Inductive loads may be switched at the output without protective diode.

Features

- TTL-compatible
- High output current
- Very high input impedance
- Good stability due to hysteresis
- Few external components

Pin configurations

TCA 345 A



Maximum ratings

Supply voltage	V_S	10	V
Output current	I_Q	70	mA
Input voltage	V_I	0 to V_S	V
Inductance at the output	L_Q	500	mH
Storage temperature range	T_{stg}	−55 to 125	°C
Junction temperature	T_j	125	°C
Thermal resistance (system-air) TCA 345 A	$R_{th\,SA}$	140	K/W
TCA 345 W	$R_{th\,SA}$	200	K/W

Operating range

Supply voltage range	V_S	2 to 10	V
Ambient temperature range	T_{amb}	−25 to 85	°C

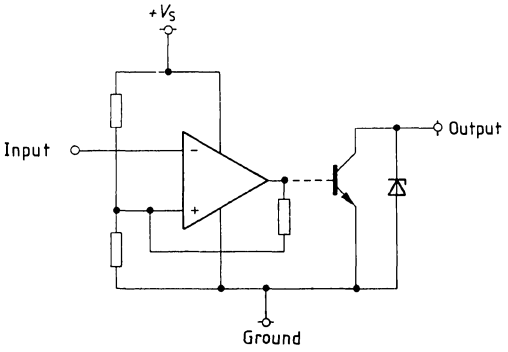
Characteristics

$T_{amb} = 25$ °C

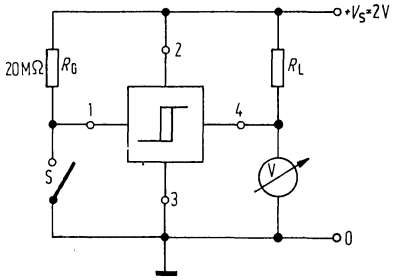
		min	typ	max	
Current consumption at output current					
$I_Q = 0$ mA; $V_S = 2$ V	$I_{S\,H}$		0.55	0.80	mA
$= 5$ V	$I_{S\,H}$		1.35	2.00	mA
$I_Q = 40$ mA; $V_S = 2$ V	$I_{S\,L}$		1.85	3.00	mA
$= 5$ V	$I_{S\,L}$		7.00	9.00	mA
L output voltage at $I_Q = 40$ mA $V_S = 2$ V	$V_{Q\,L}$		150	300	mV
Output reverse current $V_Q = 10$ V	I_{QH}			30	µA
Switching threshold ($V_S = 2$ to 10 V)[1]	V_I	$0.63 \times V_S$	$0.66 \times V_S$	$0.69 \times V_S$	V
Linearity error of the switching threshold (referred to $V_S = 2$ V)				3.0	%
Hysteresis (in % of V_S) $V_S = 2$ V	ΔV_I	6.0	10	15	%
Hysteresis (in % of V_S) $V_S = 5$ V	ΔV_I	6.0	20		%
Hysteresis (in % of V_S) $V_S = 10$ V	ΔV_I	6.0	20		%
Input current	I_I		10	30	nA
Z voltage via output	V	11.0	13.6	15.0	V
Temperature response of switching threshold			30		ppm/K

1) measured with increasing input voltage

Circuit diagram

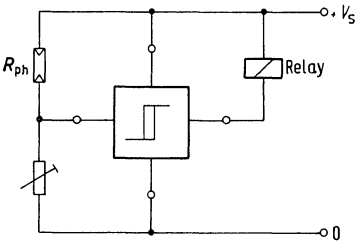


Test circuit

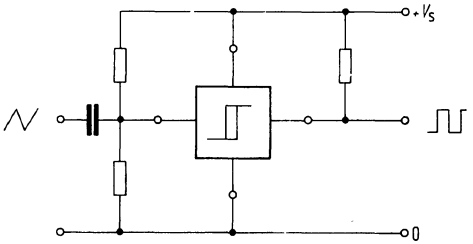


Application circuits

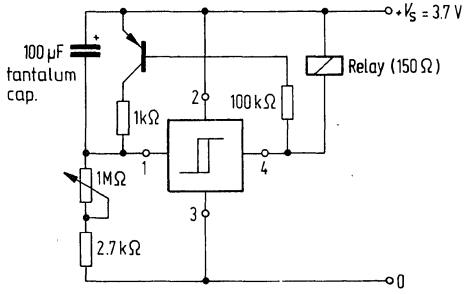
Twilight switch
(switches on light at nightfall)



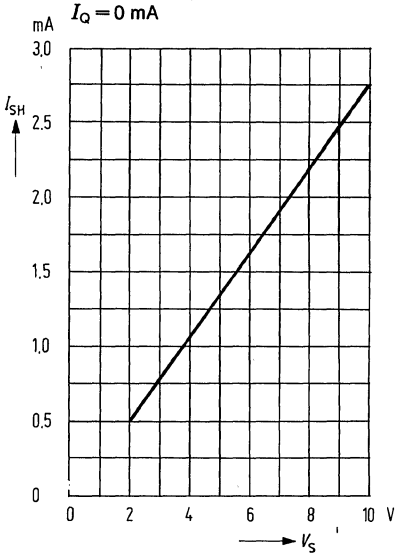
Triangle-square converter



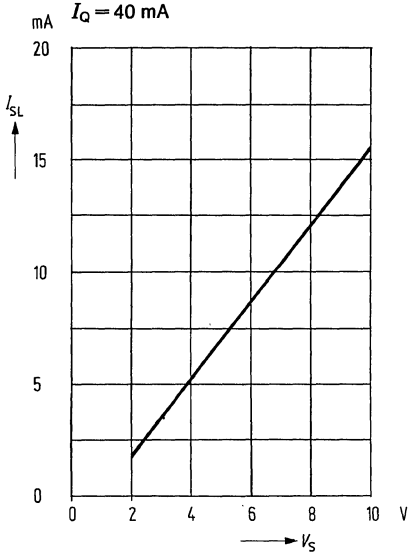
Clock generator



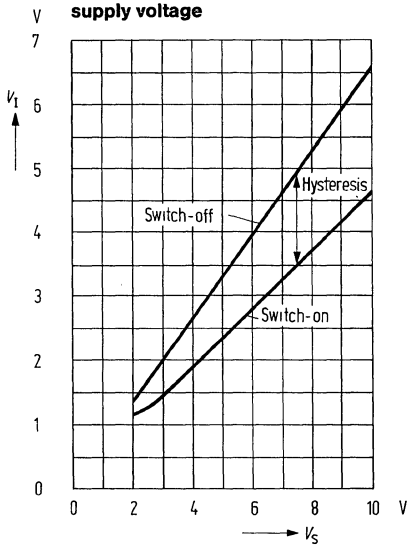
Current consumption I_{SH} versus supply voltage
$I_Q = 0$ mA



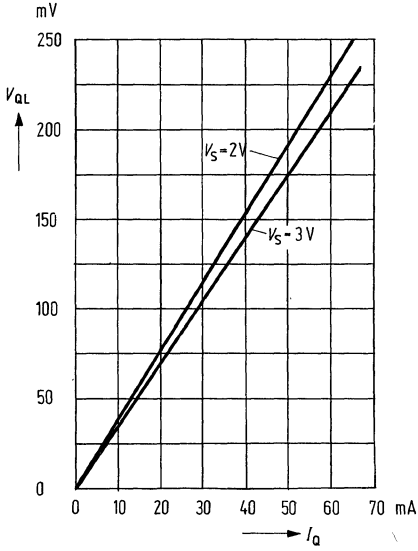
Current consumption I_{SL} versus supply voltage
$I_Q = 40$ mA



Switching threshold Input voltage versus supply voltage



L output voltage versus output current



TO-220

The TCA 365A is a power op amp in a plastic package which is similar to TO-220. At a maximum supply voltage of ± 21 V, the IC delivers a high output current of 3.5 A. The op amp is protected against thermal overload and short circuits.

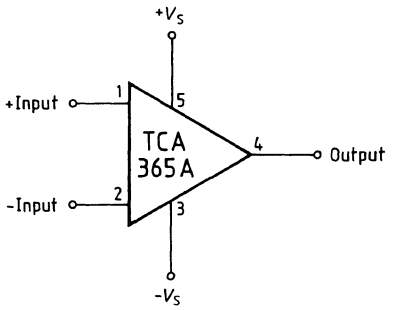
Features

- High peak output current, up to 3.5 A
- High supply voltage, up to 42 V
- Thermal overload protection
- Internal power limitation
- DC voltage short-circuit proof to $+V_S$ and $-V_S$

Applications

- Power comparator
- Power Schmitt trigger
- Speed control of dc motors

Pin configuration



Pin 3 is electrically connected to cooling fin.

Maximum ratings

Supply voltage	V_S	±21	V
Differential input voltage	V_{ID}	$\pm V_S$	V
Supply current	I_S	4.0	A
Ground current (min./max.)	I_{GND}	−4.0 to +3.5	A
Output voltage	V_Q	V_S +1	V
Peak output current	I_Q	3.5	A
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−50 to 150	°C
Total power dissipation (at $T_C = 85$ °C)	P_{tot}	13	W
Thermal resistance (system-case)	$R_{th\,SC}$	5	K/W

Operating range

Supply voltage	V_S	±3 to ±20	V
Case temperature	T_C	−25 to 85	°C
Voltage gain	G_{Vmin}	20	dB

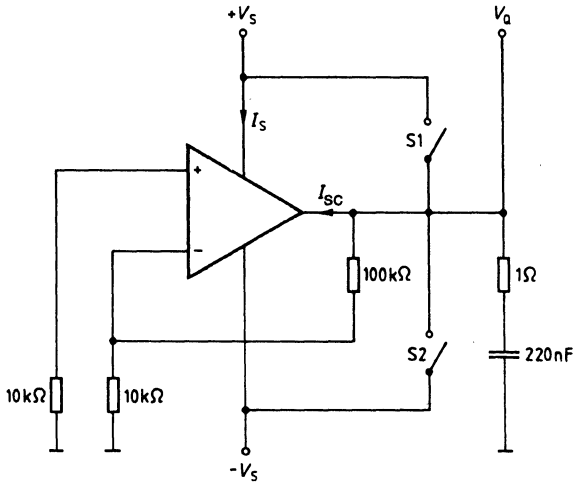
Characteristics

$V_S = \pm 15$ V; $T_C = 25$ °C

		Test circuit	min	typ	max	
Open-loop supply current consumption	I_S	1		20	40	mA
Input offset voltage	V_{IO}	2	−10		10	mV
Input offset current	I_{IO}	3	−100		100	nA
Input current	I_I	3		0.2	1	µA
Output voltage						
$R_L = 12\ \Omega$, $f = 1$ kHz	$V_{Q\,pp}$	4	±13.0	13.5		V
$R_L = 4\ \Omega$, $f = 1$ kHz	$V_{Q\,pp}$		±12.5	13.0		V
Input resistance $f = 1$ kHz	R_I	4	1	5		MΩ
Open-loop voltage gain $f = 100$ Hz	G_{V0}	5	70	80		dB
Common-mode input voltage range	V_{IC}	6	+13/−15	+13.5/−15.1		V
Common-mode rejection	k_{CMR}	6	70	80		dB
Supply voltage rejection	k_{SVR}	7	−70	−80		dB
Temperature coefficient of V_{IO} $-25 \le T_C \le 85$ °C	α_{VIO}	2		50		µV/K
Temperature coefficient of I_{IO} $-25 \le T_C \le 85$ °C	α_{IIO}	3		0.4		nA/K
Slew rate of V_Q for non-inverting operation	SR	8		2		V/µs
Slew rate of V_Q for inverting operation	SR	9		2		V/µs
Disturbance voltage referred to input DIN 45405	V_d	1		2	5	µV
Short-circuit current						
(S1 closed)	I_{SC}	1		0.75		A
(S2 closed)	I_{SC}	1		−0.75		A

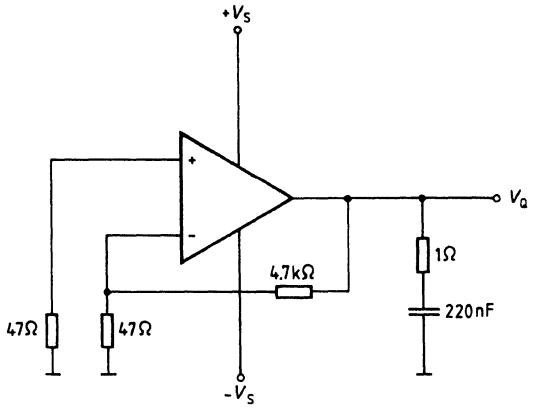
Test circuits

Figure 1 Open-loop supply current consumption, disturbance voltage



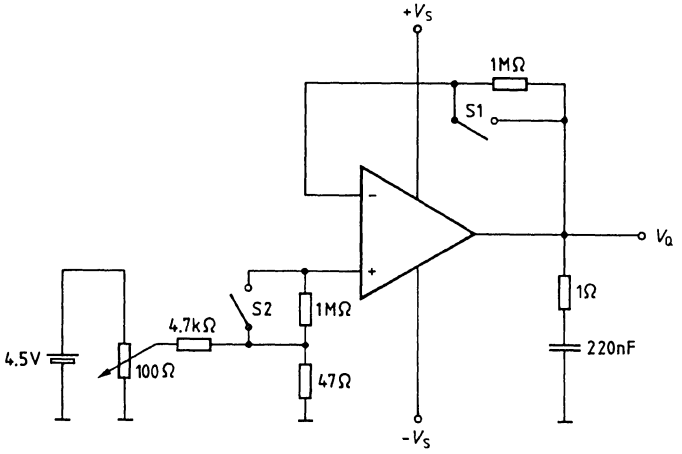
S1 and S2 as shown unless otherwise specified

Figure 2 Input offset voltage, temperature coefficient of V_{IO}



$V_Q = 100\ V_{IO}$

Figure 3 Input offset current; input current, temperature coefficient of I_{IO}



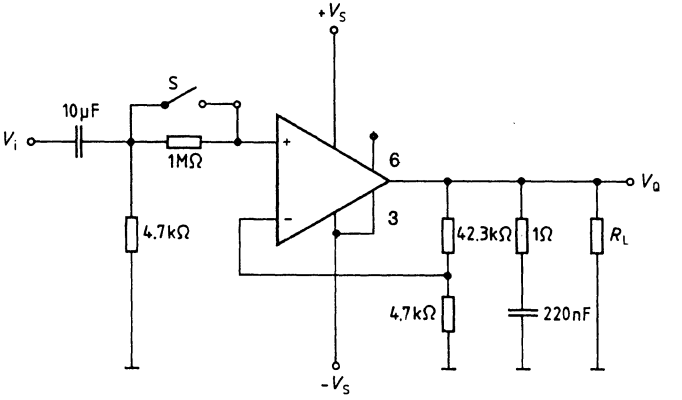
S1 open – S2 closed: $I_{I-} = \frac{V_Q}{1\,M\Omega}$

S2 open – S1 closed: $I_{I+} = \frac{V_Q}{1\,M\Omega}$

S1 open – S2 open: $I_{IO} = \frac{V_Q}{1\,M\Omega}$

S1 closed – S2 closed: offset alignment

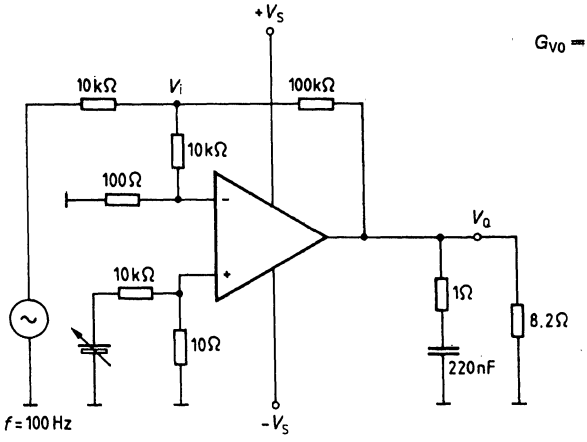
Figure 4 Output voltage, input resistance



S closed: to measure V_{Qpp}

S open/closed: to measure R_I

Figure 5 Open-loop voltage gain



$$G_{V0} = \left| 20 \log 101 \times \frac{V_Q}{V_i} \right|$$

Figure 6 Common-mode voltage gain G_{VC}
Common-mode rejection k_{CMR} (dB) = G_{V0} (dB) − G_{VC} (dB)

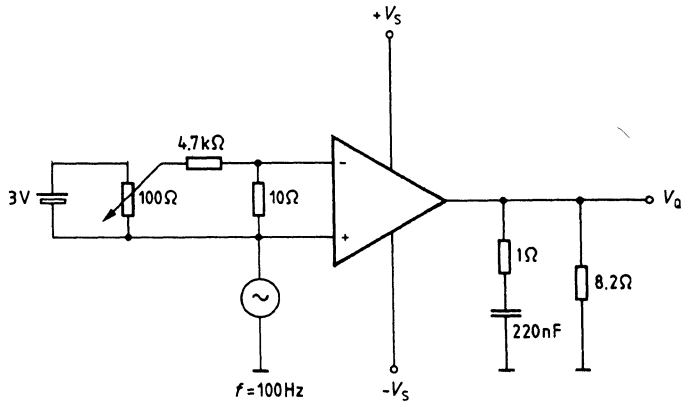
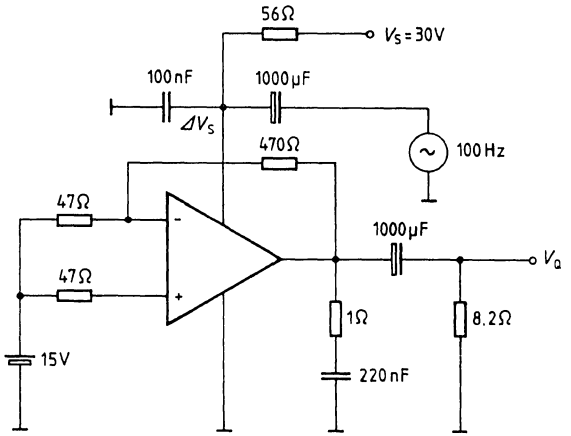


Figure 7 Supply voltage rejection



$$k_{SVR} = 20 \log \frac{\Delta V_Q}{G_V \times \Delta V_S} \text{ [dB]}$$

Figure 8 Slew rate for non-inverting operation

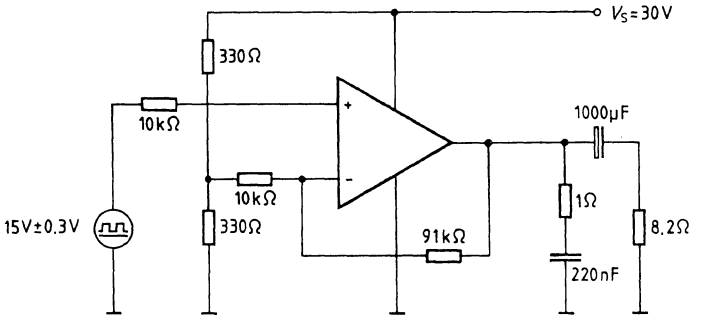
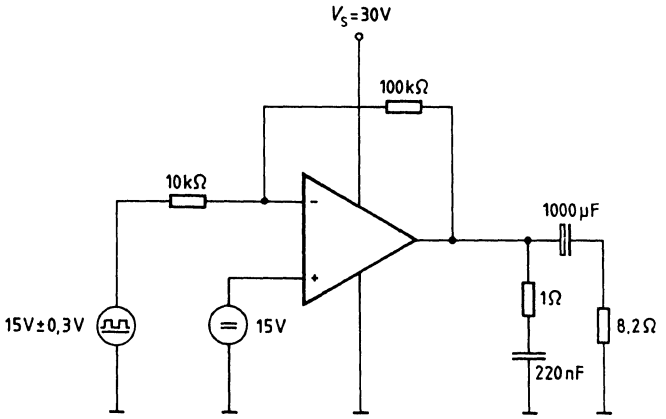
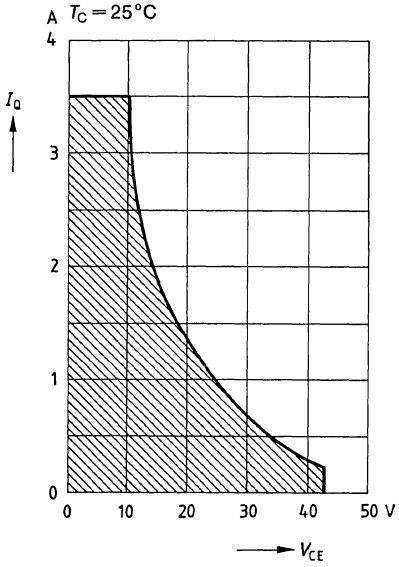


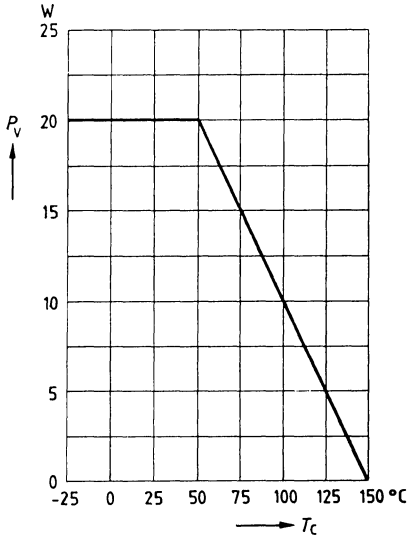
Figure 9 Slew rate for inverting operation



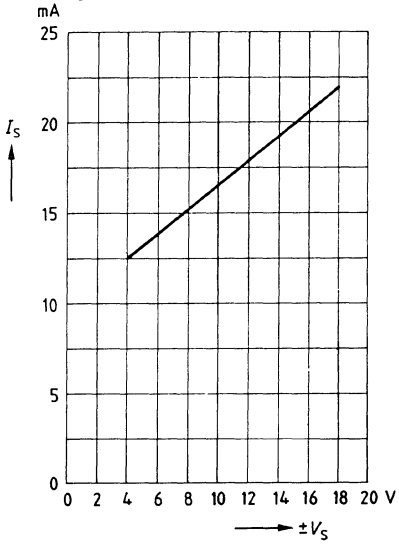
Safe operating area of output stage
Output current versus collector emitter voltage
$T_C = 25\,°C$



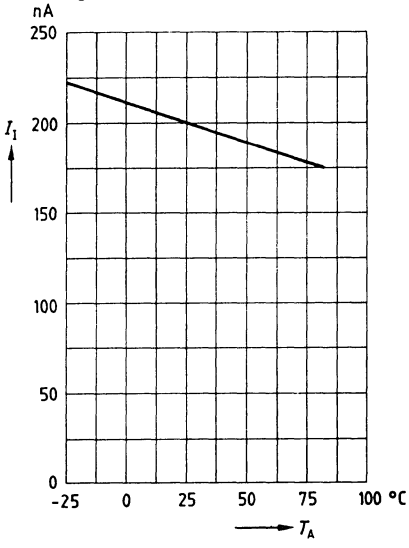
Maximum permissible power dissipation versus case temperature



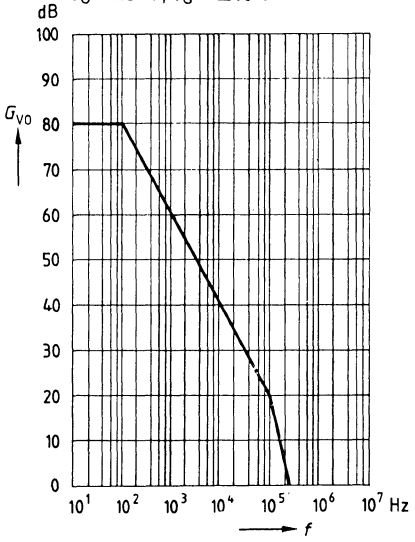
Supply current versus supply voltage
$T_C = 25\,°C$



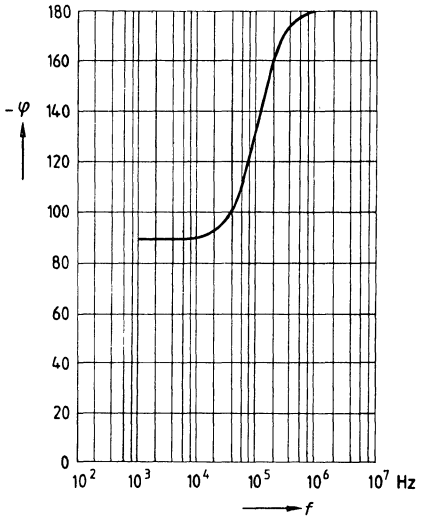
Input current versus ambient temperature
$V_S = \pm 15\,V$



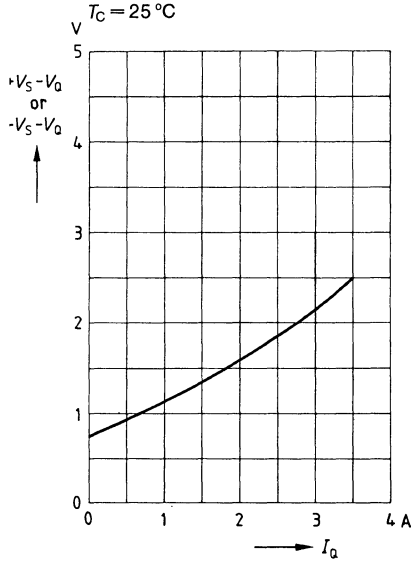
Open-loop voltage gain versus frequency
$T_C = 25\,°C$; $V_S = \pm 15$ V



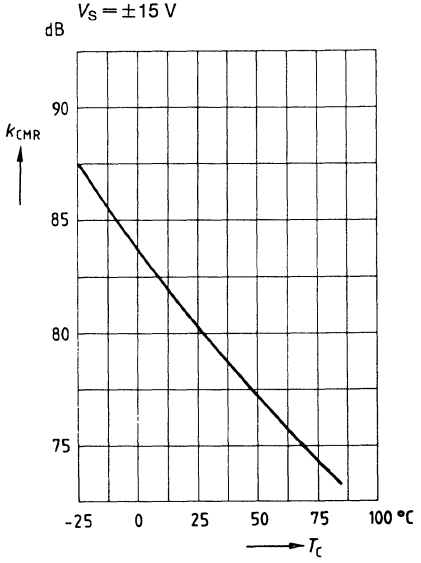
Phase response versus frequency
$T_C = 25\,°C$; $V_S = \pm 15$ V



Saturation voltage versus output current
$T_C = 25\,°C$



Common-mode rejection versus case temperature
$V_S = \pm 15$ V



DIP 16

AM receiver circuit for LW, MW, and SW in battery and line operated radio receivers. It includes an RF prestage with AGC, a balanced mixer, separate oscillator, and an IF amplifier with AGC. Because of its internal stabilization, all characteristics are largely independent of the supply voltage. For use in high quality radio sets the TDA 4001 should be preferred to the TCA 440.

Features

- Separately controlled prestage
- Multiplicative push-pull mixer with separate oscillator
- High large signal capability from 4.5 V supply voltage on
- 100 dB feedback control range in 5 stages
- Direct connection for tuning meter
- Few external components

Maximum ratings

Supply voltage	V_S	15	V
Storage temperature range	T_{stg}	−40 to 125	°C
Junction temperature	T_j	150	°C
Thermal resistance (system-air)	$R_{th\,SA}$	120	K/W

Operating range

Supply voltage	V_S	4.5 to 15	V
Ambient temperature	T_A	−15 to 80	°C

Characteristics

$V_S = 9$ V; $T_A = 25$ °C; $f_{iRF} = 600$ kHz; $f_{mod} = 1$ kHz

Total current consumption		I_S	10.5	mA
RF level deviation for	$\Delta V_{AF} = 6$ dB	ΔG_{RF}	65	dB
$m = 80\%$	$\Delta V_{AF} = 10$ dB	ΔG_{RF}	80	dB
AF output voltage for V_{iRF} (symm. measured at 1–2)				
for $m = 80\%$	$V_{iRF} = 20$ µV	$V_{AF\,rms}$	140	mV
	$V_{iRF} = 1$ mV	$V_{AF\,rms}$	260	mV
	$V_{iRF} = 500$ mV	$V_{AF\,rms}$	350	mV
for $m = 30\%$	$V_{iRF} = 20$ µV	$V_{AF\,rms}$	50	mV
	$V_{iRF} = 1$ mV	$V_{AF\,rms}$	100	mV
	$V_{iRF} = 500$ mV	$V_{AF\,rms}$	130	mV
Input sensitivity (measured at 60 Ω, $f_{iRF} = 1$ MHz, $m = 30\%/0\%$, $R_G = 540$ Ω)				
at signal-to-noise ratio $\frac{S+N}{N} = 6$ dB (in acc. with DIN 45405)		V_{iRF}	1	µV
	$\frac{S+N}{N} = 26$ dB	V_{iRF}	7	µV
	$\frac{S+N}{N} = 58$ dB	V_{iRF}	1	mV

RF stage

Input frequency range	f_{iRF}	0 to 50	MHz
Output frequency $f_{IF} = f_{OSC} - f_{iRF}$	f_{IF}	460	kHz
Control range	ΔG_V	38	dB
Input voltage (for 600 kHz, $m = 80\%$) for overdrive ($THD_{AF} = 10\%$), symmetrically measured at pins 1 and 2	$V_{iRF\,pp}$	2.6	V
(mean carrier value)	$V_{iRF\,rms}$	0.5	V
IF suppression between 1–2 and 15	a_{IF}	20	dB
RF input impedance			
a) unsymmetrical coupling			
at $G_{RF\,max}$	Z_i	2/5	kΩ/pF
at $G_{RF\,min}$	Z_i	2.2/1.5	kΩ/pF
b) symmetrical coupling			
at $G_{RF\,max}$	Z_i	4.5	kΩ/pF
at $G_{RF\,min}$	Z_i	4.5/1.5	kΩ/pF
Mixer output impedance (pins 15 or 16)	Z_q	250/4.5	kΩ/pF

IF stage

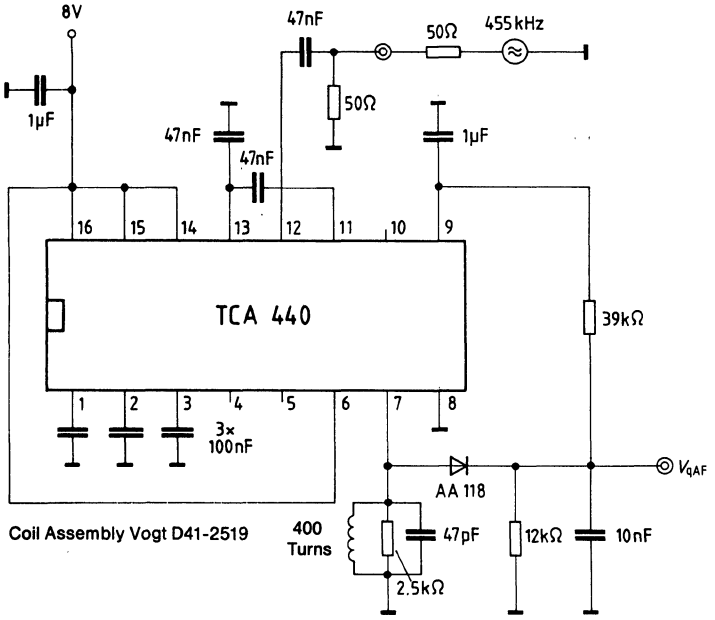
Input frequency range	f_{iIF}	0 to 2	MHz
Control range at 460 kHz	ΔG_V	62	dB
Input voltage (mean carrier value) at G_{min} for overdrive (THD_{AF} = 10%), measured at pin 12 (60 Ω to ground, f_{iIF} = 460 kHz, m = 80%; f_{mod} = 1 kHz)	$V_{IF\,rms}$	200	mV
AF output voltage for V_{iIF} at 60 Ω (pin 12)			
V_{iIF} = 30 µV, m = 80%; f_{mod} = 1 kHz	$V_{7\,AF\,rms}$	50	mV
V_{iIF} = 3 mV, m = 80%; f_{mod} = 1 kHz	$V_{7\,AF\,rms}$	200	mV
V_{iIF} = 3 mV, m = 30%; f_{mod} = 1 kHz	$V_{7\,AF\,rms}$	70	mV
V_{iIF} = 200 µV; m = 30%, f_{iF} = 455 kHz; $f_{q\,AF}$ = 1 kHz	$V_{7\,AF\,rms}$	35 to 60	mV
IF input impedance (unsymm. coupling)	Z_i	3/3	kΩ/pF
IF output impedance	Z_{q7}	200/8	kΩ/pF

Tuning meter

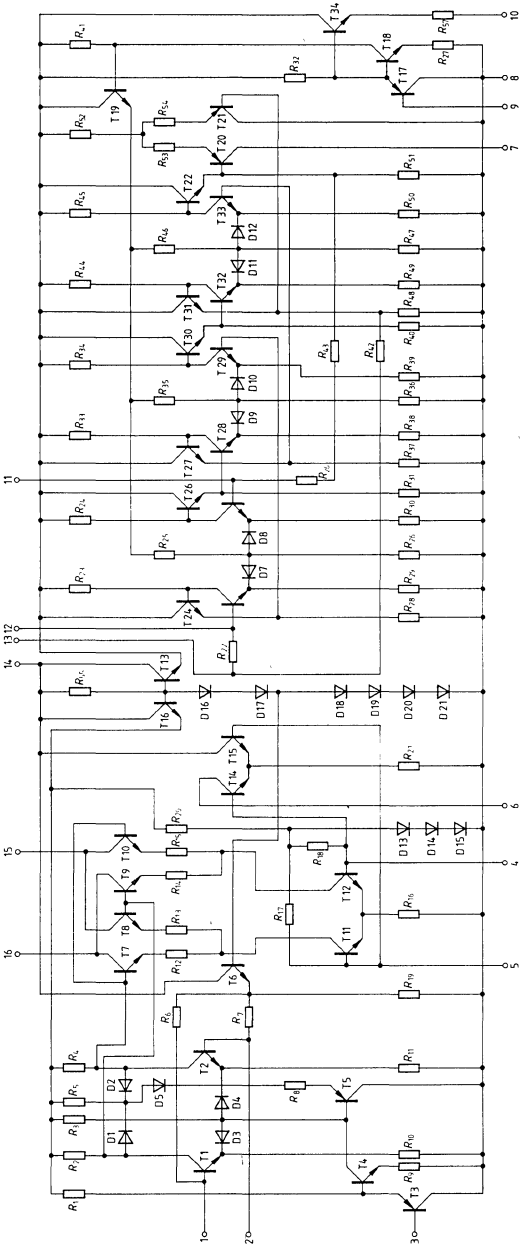
Recommended instruments: 500 µA (R_i = 800 kΩ)
or 300 µA (R_i = 1.5 kΩ)

The IC offers a tuning meter voltage of 600 mV_{EMF} max. with a source impedance of approx. 400 Ω.

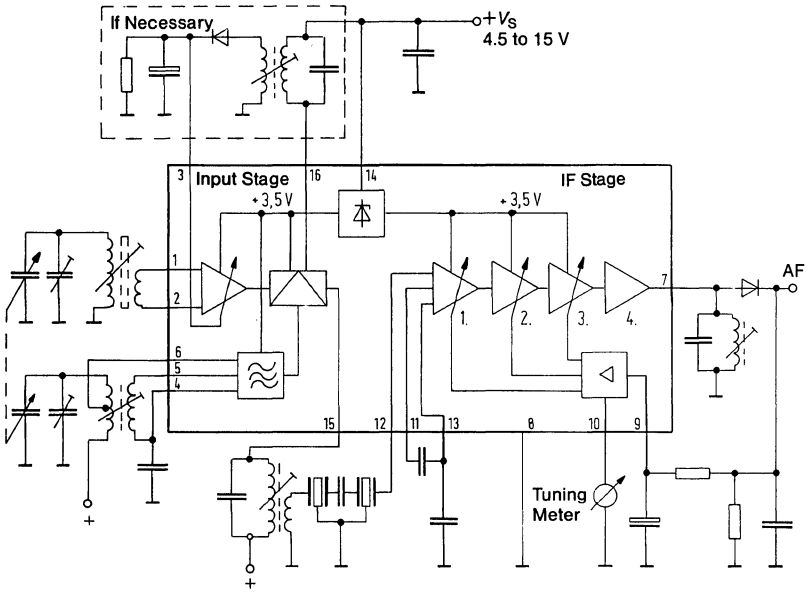
Measurement circuit for output voltage

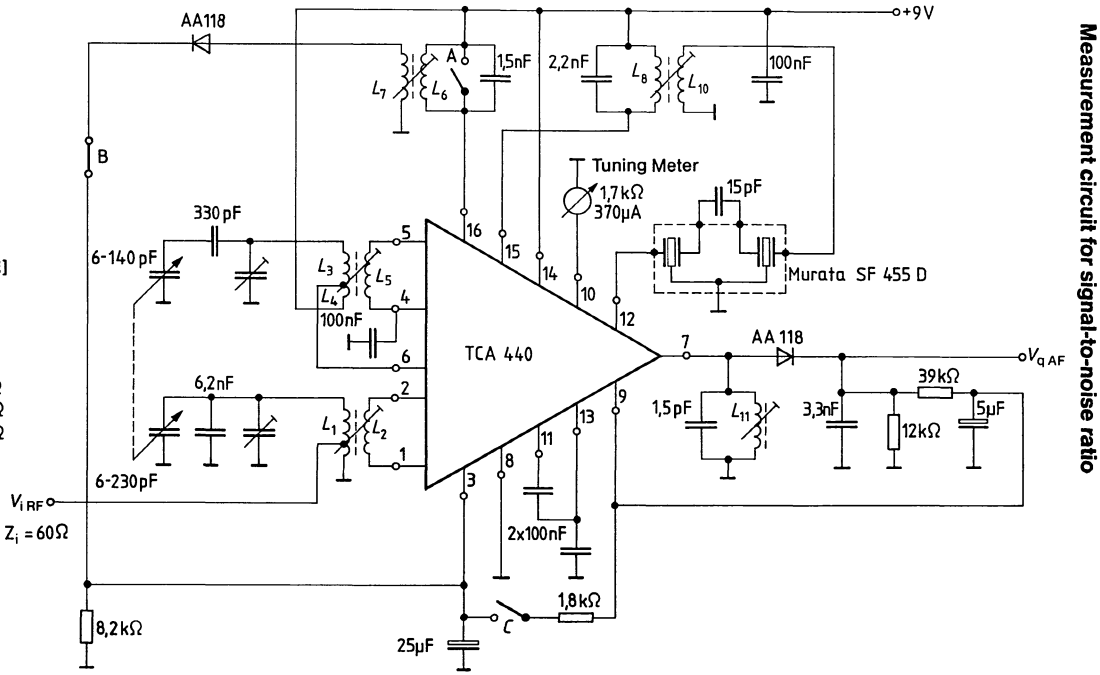


Circuit diagram



Block diagram





n[Turns]	R_G [Ω]
1	15
2	60
4	240
6	540
9	1,2kΩ
12	2,2kΩ
18	4,8kΩ

L_1-L_2 M 25 pot core
L_3-L_{11} with coil assembly Vogt D41-2519

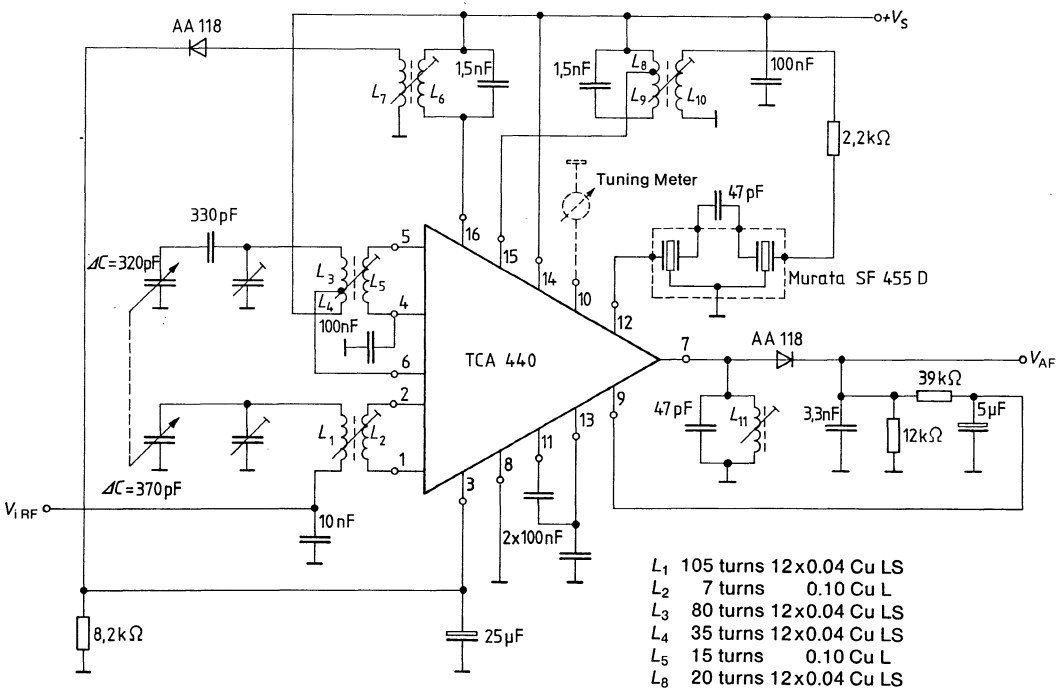
L_1 2+6 turns 6x12x0.04 Cu LS
L_2 n turns 0.15 Cu L
L_3 90 turns 12x0.04 Cu LS
L_4 35 turns 12x0.04 Cu LS
L_5 15 turns 0.10 Cu L
L_6 70 turns 12x0.04 Cu LS
L_7 35 turns 12x0.04 Cu LS
L_8 60 turns 12x0.04 Cu LS
L_{10} 22 turns 12x0.04 Cu LS
L_{11} 68 turns 0.06 CuL

Switch

A	B	C		
off	on	off	separate prestage control	①
on	off	on	prestage control voltage derived from IF control voltage	②

$f_i = 1$ MHz; $m = 30\%$

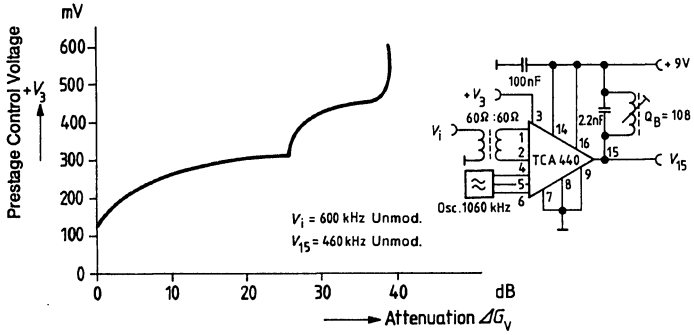
Application example for MW with TCA 440



L_1-L_2 with coil assembly Vogt D21-2375.1
L_3-L_{11} with coil assembly Vogt D41-2519

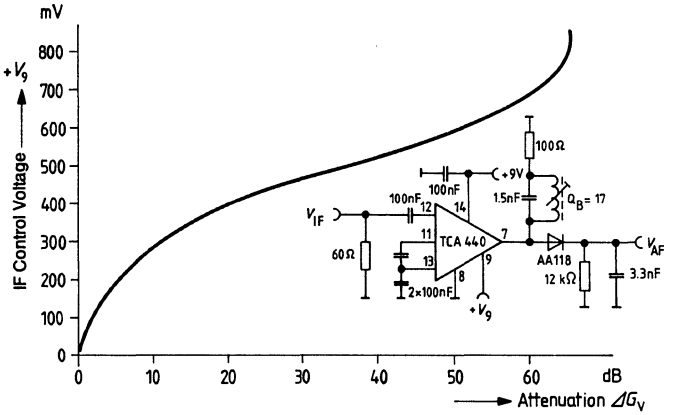
L_1	105 turns	12x0.04 Cu LS
L_2	7 turns	0.10 Cu L
L_3	80 turns	12x0.04 Cu LS
L_4	35 turns	12x0.04 Cu LS
L_5	15 turns	0.10 Cu L
L_8	20 turns	12x0.04 Cu LS
L_9	50 turns	12x0.04 Cu LS
L_{10}	22 turns	12x0.04 Cu LS
L_{11}	400 turns	0.06 Cu LS

Prestage control TCA 440



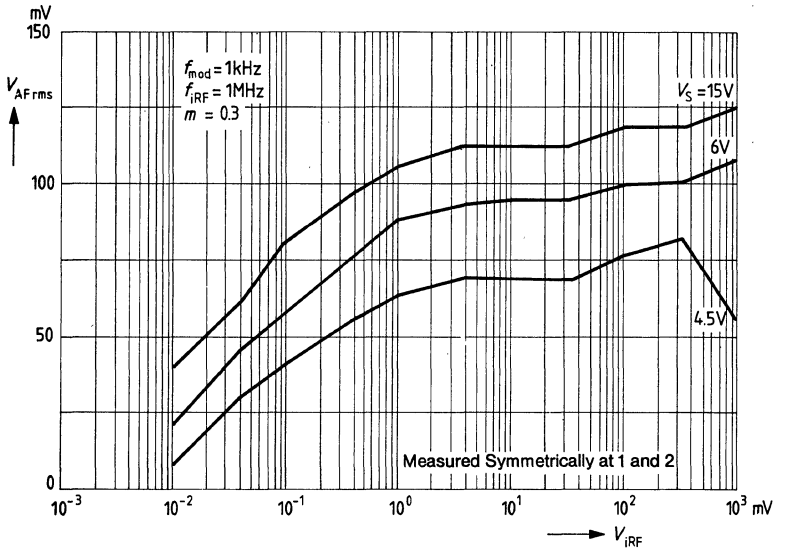
The input ist not power matched and can be driven with a higher resistance. The selected V_i ensures a constant V_{15} (50 mV peak-to-peak).

IF control



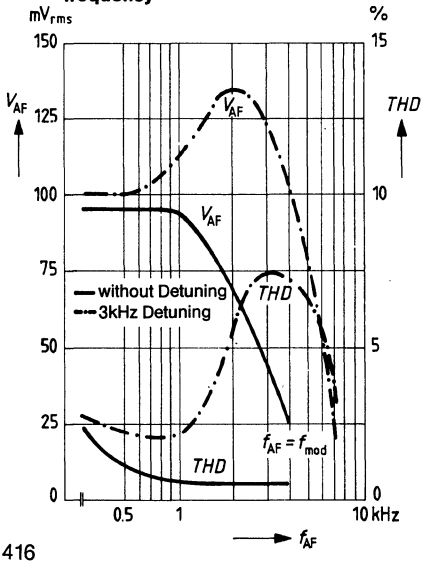
The selected V_{IF} (469 kHz; m = 80%; f_{mod} = 1 kHz) ensures a constant V_{AF} (200 mV, rms).

AF output voltage versus RF input voltage

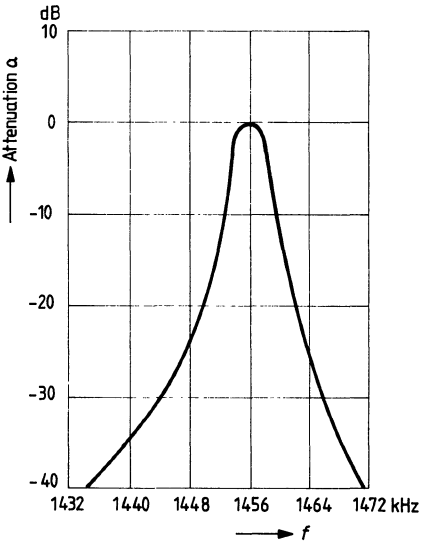


Example for medium wave applications

AF output voltage versus output frequency
Total harmonic distortion versus modulation frequency

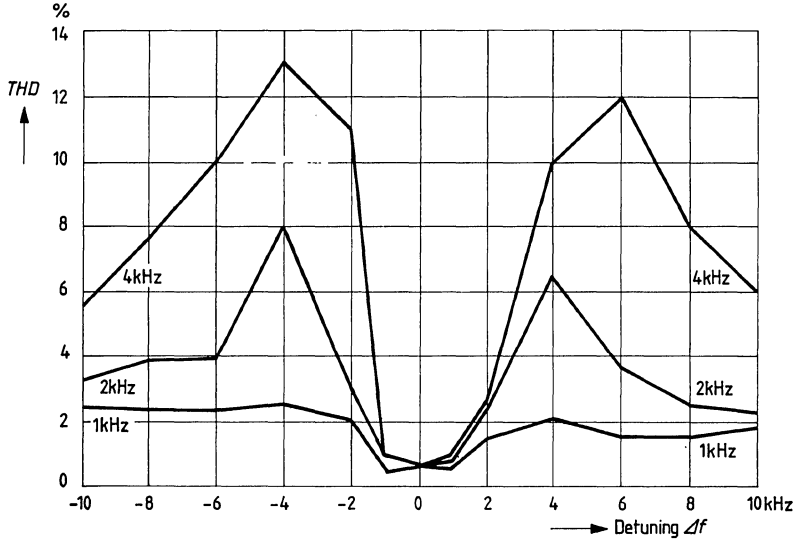


Passband characteristic versus input frequency, measured from input to output of the circuit

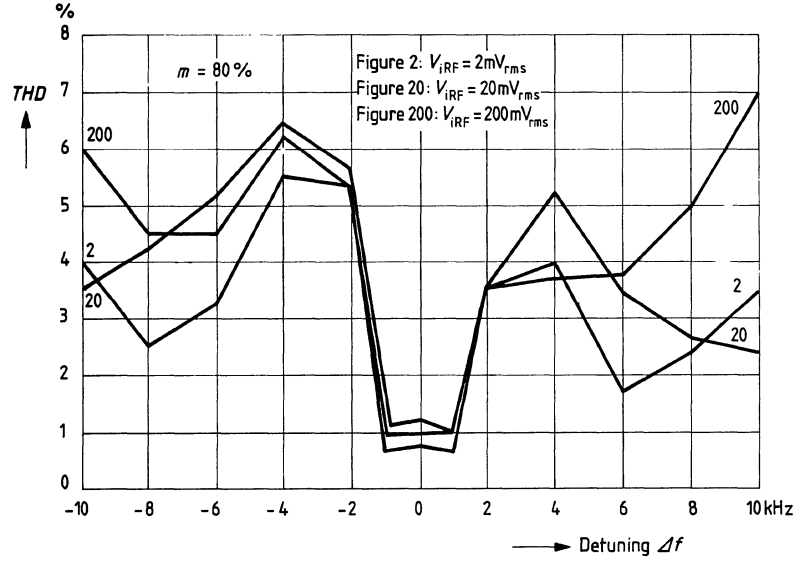


Total harmonic distortion versus detuning (parameter: modulation frequency)

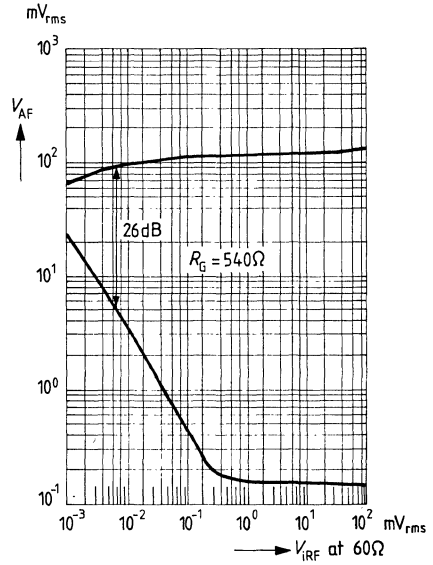
$V_S = 9$ V $f_{OSC} = 1.455$ MHz $\pm \Delta f$ $m = 30\%$
$f_{iRF} = 1$ MHz $f_{IF} = 455$ kHz $V_{iRF} = 20$ mV$_{rms}$



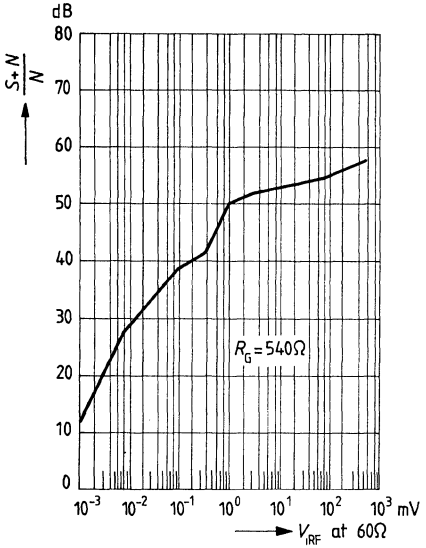
Total harmonic distortion versus detuning (parameter: RF input voltage)



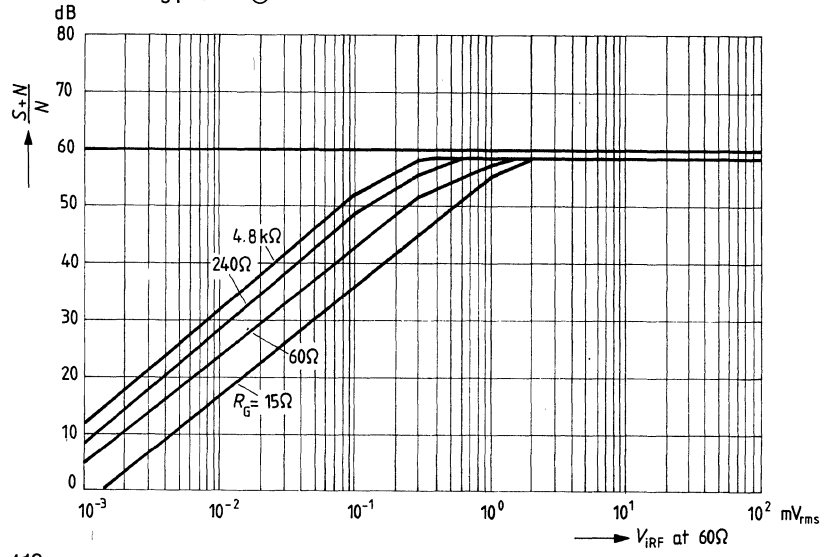
AF output voltage and noise figure versus RF input voltage
switching position ①



Signal-to-noise ratio versus RF input voltage
switching position ②

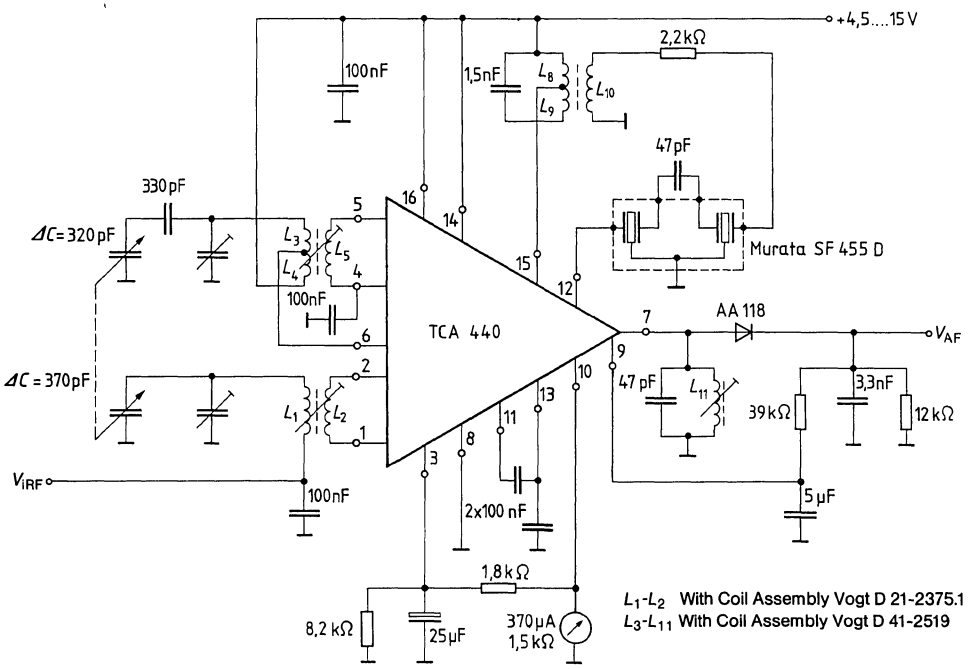


Signal-to-noise ratio versus RF input voltage
(parameter is generator impedance)
switching position ①



Application example for MW

Prestage control is derived from IF control

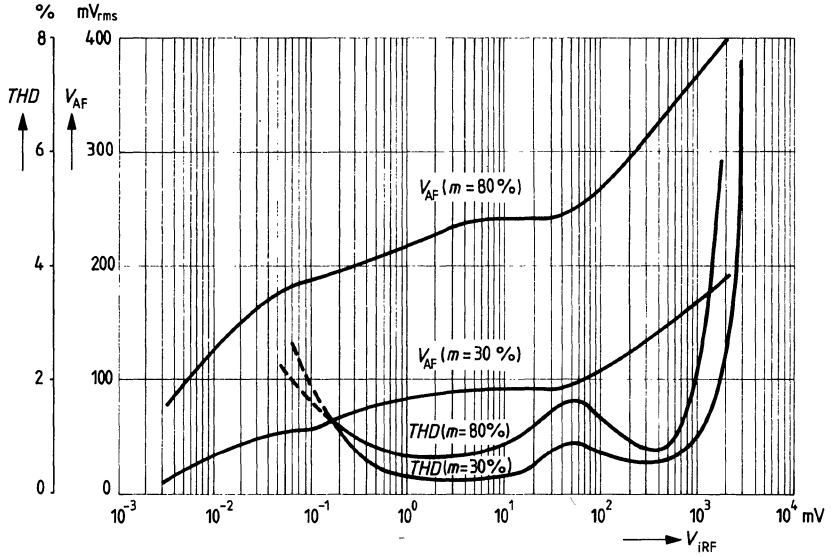


L_1-L_2 With Coil Assembly Vogt D 21-2375.1
L_3-L_{11} With Coil Assembly Vogt D 41-2519

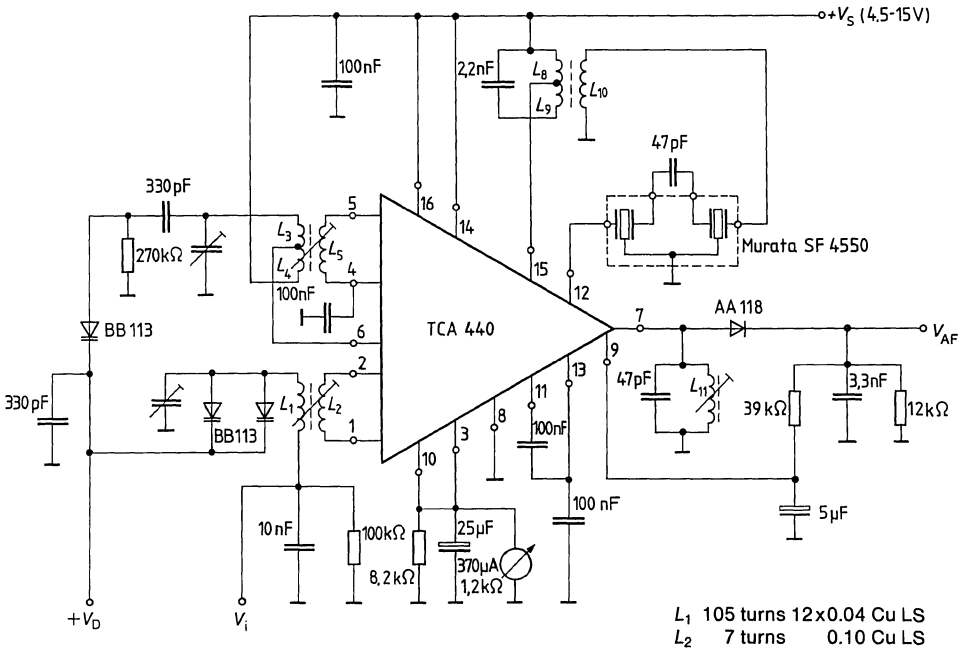
L_1 105 turns 12x0.04 Cu LS
L_2 7 turns 0.10 Cu L
L_3 80 turns 12x0.04 Cu LS
L_4 35 turns 12x0.04 Cu LS
L_5 15 turns 0.10 Cu L
L_8 20 turns 12x0.04 Cu LS
L_9 50 turns 12x0.04 Cu LS
L_{10} 22 turns 12x0.04 Cu LS
L_{11} 400 turns 0.04 Cu L

Test figures for application example for MW

Total harmonic distortion and AF output voltage versus RF input voltage measured symmetrically at pins 1 and 2
$f_i = 1$ MHz, $f_{mod} = 1$ kHz, $f_{IF} = 455$ kHz, $V_S = 9$ V



Application example for MW using BB 113 varicap diodes



L_1-L_2 With Coil Assembly Vogt D21-2375.1

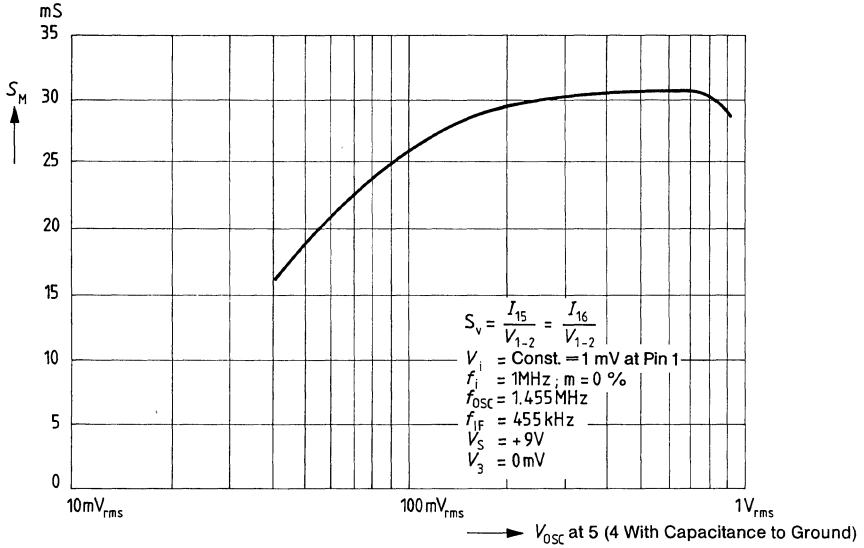
L_3-L_{11} With Coil Assembly Vogt D41-2519

V_{tun} = 8.5 V ⟶ f_i = 800 kHz

V_{tun} = 30 V ⟶ f_i = 1620 kHz

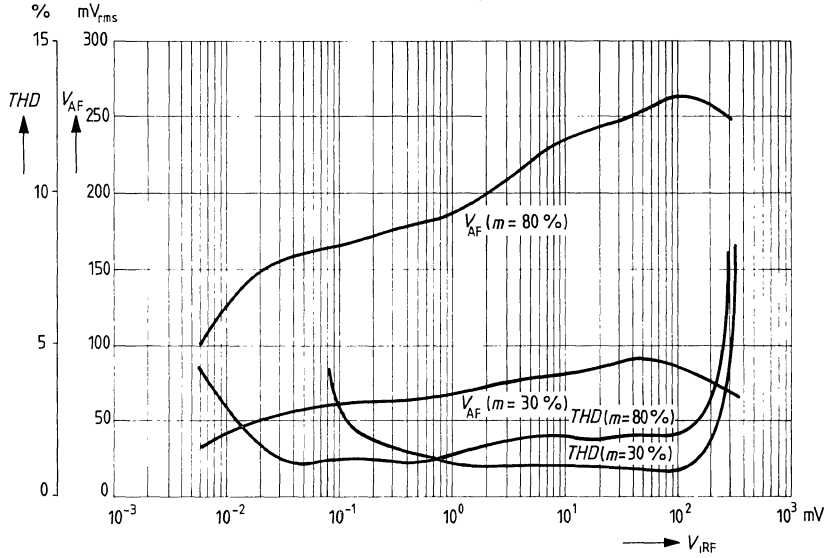
L_1	105 turns	12x0.04 Cu LS
L_2	7 turns	0.10 Cu LS
L_3	80 turns	12x0.04 Cu LS
L_4	35 turns	12x0.04 Cu LS
L_5	15 turns	0.10 Cu LS
L_8	20 turns	12x0.04 Cu LS
L_9	50 turns	12x0.04 Cu LS
L_{10}	22 turns	12x0.04 Cu LS
L_{11}	400 turns	0.06 Cu L

Conversion transconductance versus oscillator voltage

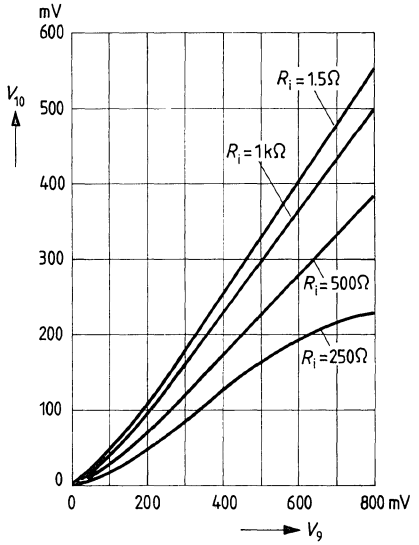


Measured values for application example for MW using diode BB 113

AF output voltage and total harmonic distortion versus RF input voltage
$f_i = 1$ MHz; $f_{mod} = 1$ kHz; $f_{IF} = 455$ kHz
$V_S = 9$ V; V_{iRF} symmetrically measured at pins 1 and 2



Tuning meter voltage versus IF control voltage
(parameter: impedance of tuning meter)



Example for moving coil instruments

R_i	Full-service deflection
1.5 kΩ	100 µA
1.5 kΩ	170 µA
2 kΩ	200 µA
350 Ω	500 µA

DIP 16

This phase control IC is intended to control thyristors, triacs, and transistors. The trigger pulses can be shifted within a phase angle between 0° and 180°. Typical applications include converter circuits, AC controllers and three-phase current controllers.

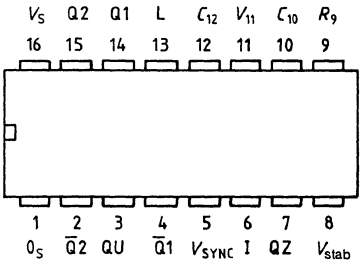
This IC replaces the previous types TCA 780 and TCA 780 D

Features

- Reliable recognition of zero passage
- Large application scope
- May be used as zero point switch
- LSL compatible
- Three-phase operation possible (3 ICs)
- Output current 250 mA
- Large ramp current range
- Large temperature range

Pin configuration

top view



Pin No.	Symbol	Function
1	0_S	Ground
2	$\overline{Q}2$	Output 2 inverted
3	QU	Output U
4	$\overline{Q}1$	Output 1 inverted
5	V_{SYNC}	Synchronous voltage
6	I	Inhibit
7	QZ	Output Z
8	V_{stab}	Reference voltage
9	R_9	Ramp resistance
10	C_{10}	Ramp capacitance
11	V_{11}	Control voltage
12	C_{12}	Pulse extension
13	L	Long pulse
14	Q1	Output 1
15	Q2	Output 2
16	V_S	Supply voltage

Functional description

The synchronization signal is obtained via a high-ohmic resistance from the line voltage (voltage V_5). A zero voltage detector evaluates the zero passages and transfers them to the synchronization register.

This synchronization register controls a ramp generator the capacitor C_{10} of which is charged by a constant current (determined by R_9). If the ramp voltage V_{10} exceeds the control voltage V_{11} (triggering angle φ), a signal is processed to the logic. Dependent on the magnitude of the control voltage V_{11}, the triggering angle φ can be shifted within a phase angle of 0° to 180°.

For every half wave, a positive pulse of approx. 30 µs duration appears at the outputs Q1 and Q2. The pulse duration can be prolonged up to 180° via a capacitor C_{12}. If pin 12 is connected to ground, pulses with a duration between φ and 180° will result.

Outputs $\overline{Q}1$ and $\overline{Q}2$ supply the inverse signals of Q1 and Q2.

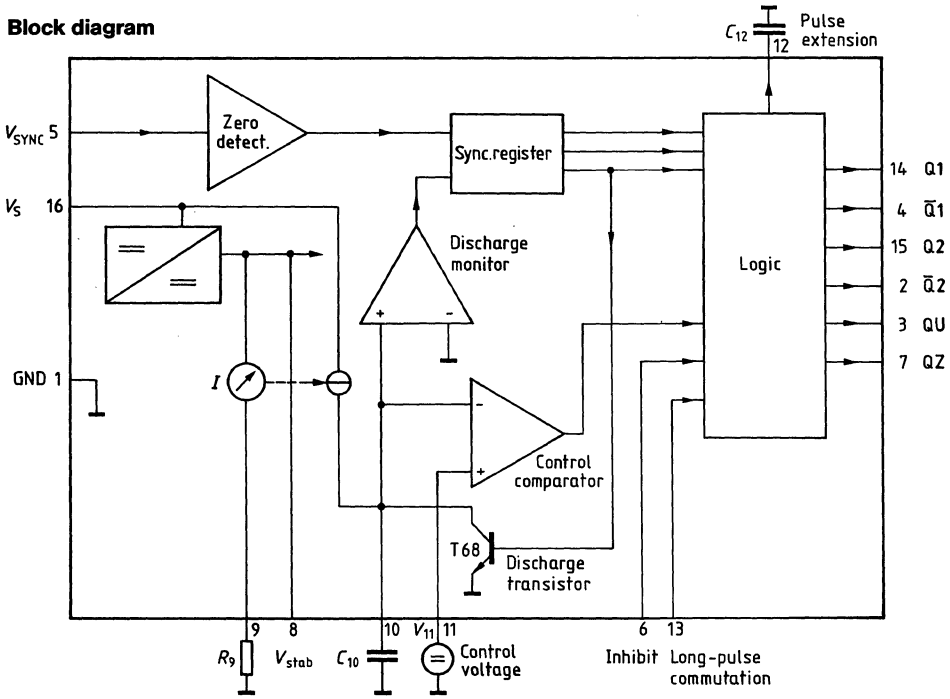
A signal of $\varphi + 180°$ which can be used for controlling an external logic, is available at pin 3.

A signal which corresponds to the NOR link of Q1 and Q2 is available at output QZ (pin 7).

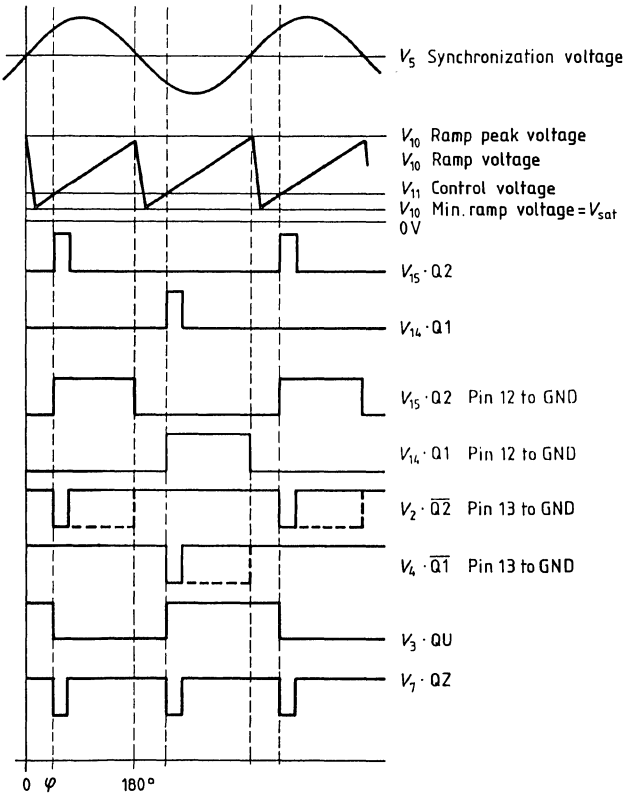
The inhibit input can be used to disable outputs Q1, Q2, $\overline{Q}1$, $\overline{Q}2$, QU.

Pin 13 can be used to extend the outputs $\overline{Q}1$ and $\overline{Q}2$ to full pulse length (180° − φ).

Block diagram



Pulse diagram



Maximum ratings

		Lower limit B	Upper limit A	
Supply voltage	V_S	−0.5	18	V
Output current at pin 14, 15	I_Q	−10	400	mA
Inhibit voltage	V_6	−0.5	V_S	V
Control voltage	V_{11}	−0.5	V_S	V
Voltage short-pulse circuit	V_{13}	−0.5	V_S	V
Synchronization input current	I_5	−200	± 200	µA
Output voltage at pin 14, 15	V_Q		V_S	V
Output current at pin 2, 3, 4, 7	I_Q		10	mA
Output voltage at pin 2, 3, 4, 7	V_Q		V_S	V
Junction temperature	T_j		125	°C
Storage temperature	T_{stg}	−55	125	°C
Thermal resistance (system-air)	$R_{th\,SA}$		80	K/W

Operating range

Supply voltage	V_S	8	18	V
Operating frequency	f	10	500	Hz
Ambient temperature range	T_{amb}	−25	85	°C

Characteristics
$8 \leq V_S \leq 18$ V; $-25\,°C \leq T_{amb} \leq 85\,°C$; $f = 50$ Hz

		Test circuit No.	Lower limit B	$f = 50$ Hz $V_S = 15$ V typ	Upper limit A	
Supply current consumption S 1...S 6 open $V_{11} = 0$ V $C_{10} = 47$ nF; $R_9 = 100$ kΩ	I_S	1	4.5	6.5	10	mA
Synchronization pin 5						
Input current R_2 varied	$I_{5\,rms}$	1	30		200	µA
Offset voltage	ΔV_5	4		30	75	mV
Control input pin 11						
Control voltage range	V_{11}	1	0.2		$V_{10\,peak}$	V
Input resistance	R_{11}	5		15		kΩ
Ramp generator						
Load current	I_{10}		10		1000	µA
Max. ramp voltage	V_{10}	1			$V_S - 2$	V
Saturation volt. at capacitor	V_{10}	1.6	100	225	350	mV
Ramp resistance	R_9	1	3		300	kΩ
Sawtooth return time	t_f	1		80		µs
Inhibit pin 6 switch-over of pin 7						
Outputs disabled	V_{6L}	1		3.3	2.5	V
Outputs enabled	V_{6H}	1	4	3.3		V
Signal transition time	t_r	1	1		5	µs
Input current $V_6 = 8$ V	I_{6H}	1		500	800	µA
Input current $V_6 = 1.7$ V	$-I_{6L}$	1	80	150	200	µA
Deviation of I_{10} $R_9 = $ const. $V_S = 12$ V; $C_{10} = 47$ nF	I_{10}	1	−5		5	%
Deviation of I_{10} $R_9 = $ const. $V_S = 8$ to 18 V	I_{10}	1	−20		20	%
Deviation of the ramp voltage between 2 following half-waves, $V_S = $ const.	$\Delta V_{10\,max}$			± 1		%

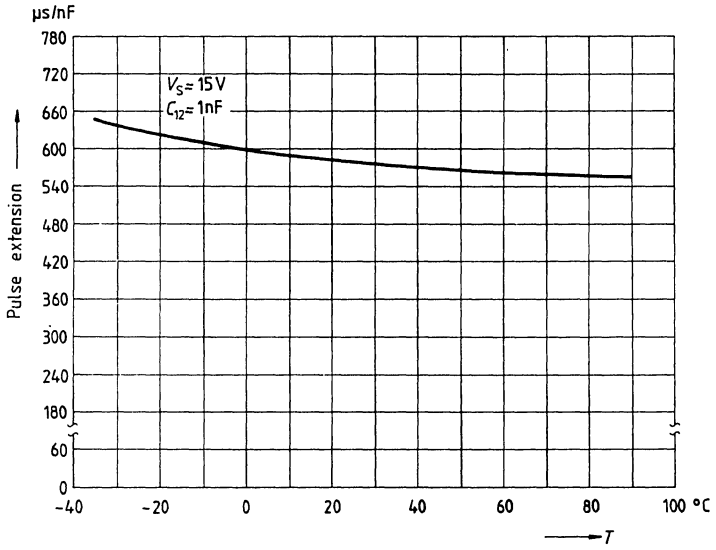
Characteristics $8 \leq V_S \leq 18$ V; $-25\,°C \leq T_{amb} \leq 85\,°C$; $f = 50$ Hz		Test circuit No.	Lower limit B	$f = 50$ Hz $V_S = 15$ V typ	Upper limit A	
Long pulse switch-over pin 13 switch-over of S 8						
Short pulse at output	$V_{13\,H}$	1	3.5	2.5		V
Long pulse at output	$V_{13\,L}$	1		2.5	2	V
Input current $V_{13} = 8$ V	$I_{13\,H}$	1			10	µA
Input current $V_{13} = 1.7$ V	$-I_{13\,L}$	1	45	65	100	µA
Outputs pin 2, 3, 4, 7						
Reverse current $V_Q = V_S$	I_{CE0}	2.6			10	µA
Saturation voltage $I_Q = 2$ mA	V_{sat}	2.6	0.1	0.4	2	V
Outputs pin 14, 15						
H output voltage $-I_Q = 250$ mA	$V_{14/15\,H}$	3.6	V_S-3	$V_S-2.5$	$V_S-1.0$	V
L output voltage $I_Q = 2$ mA	$V_{14/15\,L}$	2.6	0.3	0.8	2	V
Pulse width (short pulse) S 9 open	t_p	1	20	30	40	µs
Pulse width (short pulse) with C_{12}	t_p	1	530	620	760	µs/nF
Internal voltage control						
Reference voltage	V_{ref}	1	2.8	3.1	3.4	V
Parallel connection of 10 ICs possible						
TC of reference voltage	α_{ref}	1		2×10^{-4}	5×10^{-4}	1/K

Application hints for external components

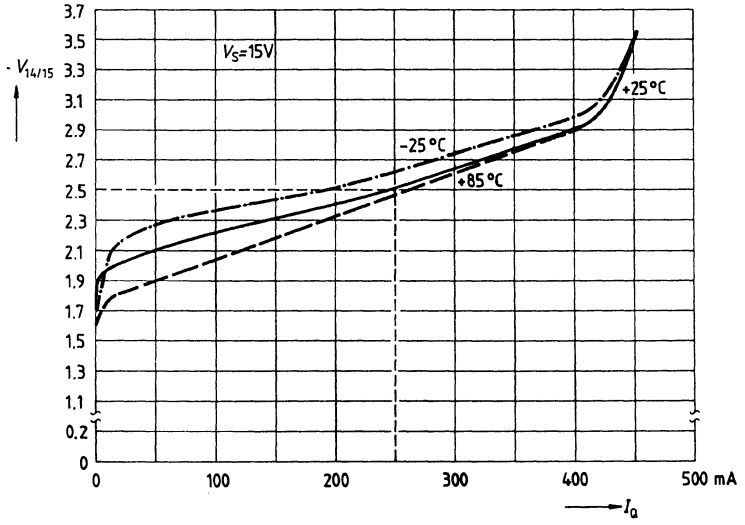
		min	max	
Ramp capacitance	C_{10}	500 pF	1 µF[1]	The minimum and maximum values of I_{10} are to be observed
Triggering point	$t_{Tr} = \frac{V_{11} \times R_9 \times C_{10}}{V_{ref} \times K}$		[2]	
Charging current	$I_{10} = \frac{V_{ref} \times K}{R_9}$		[2]	Ramp voltage $V_{10\,max} = V_S - 2$ V $V_{10} = \frac{V_{ref} \times K \times t}{R_9 \times C_{10}}$ [2]

1) Attenuation to flyback times
2) $K = 1.10 \pm 20\%$

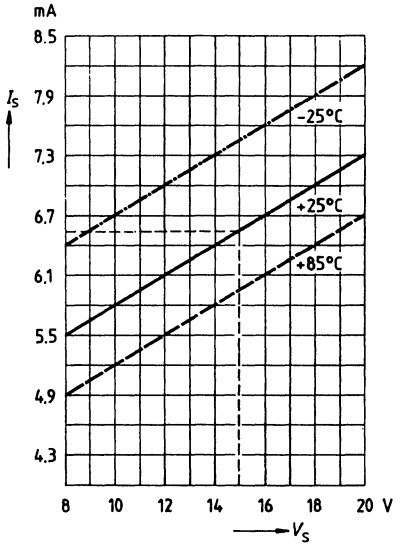
Pulse extension versus temperature



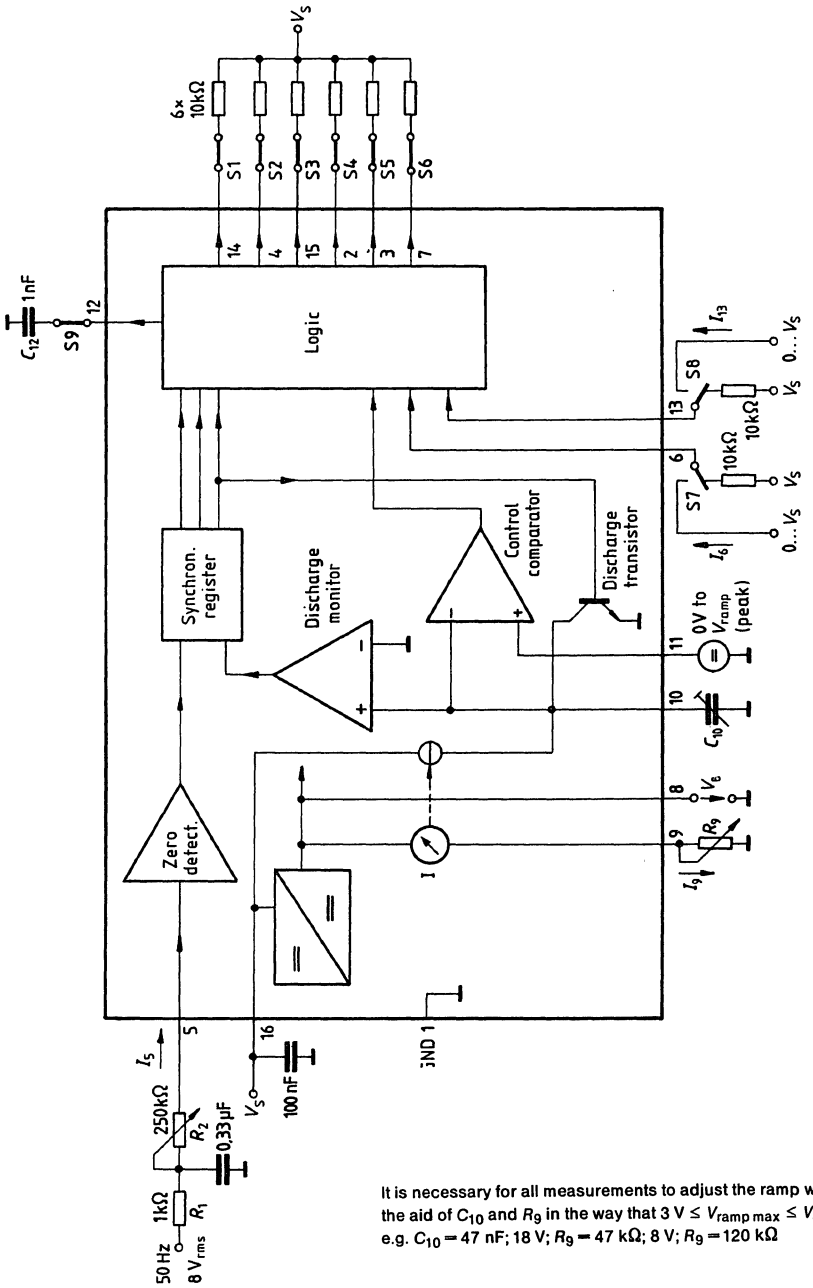
Output voltage measured to + V_S



Supply current versus supply voltage



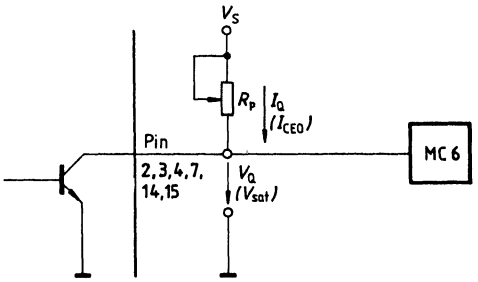
Test and measurement circuit 1



It is necessary for all measurements to adjust the ramp with the aid of C_{10} and R_9 in the way that $3\ V \leq V_{ramp\ max} \leq V_S - 2\ V$
e.g. $C_{10} = 47$ nF; 18 V; $R_9 = 47$ kΩ; 8 V; $R_9 = 120$ kΩ

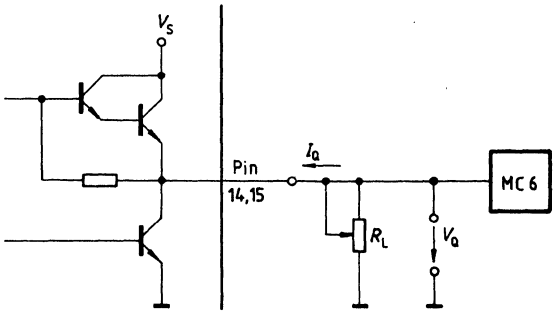
Test and measurement circuits

Measurement circuit 2



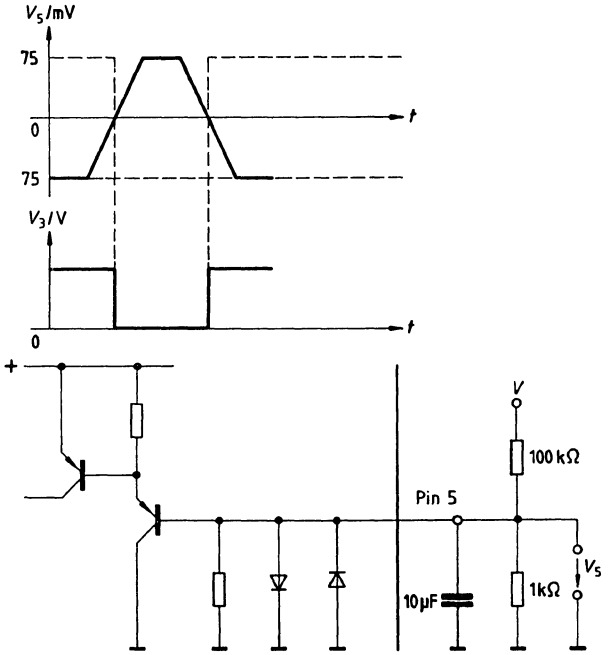
The residual pins are connected as in measurement circuit 1

Measurement circuit 3



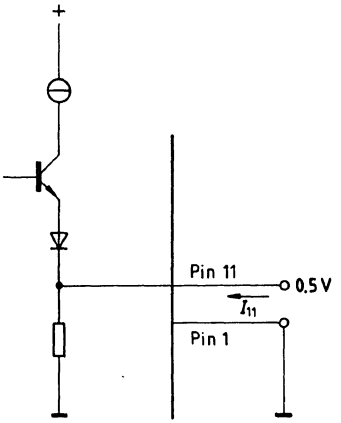
The residual pins are connected as in measurement circuit 1

Measurement circuit 4

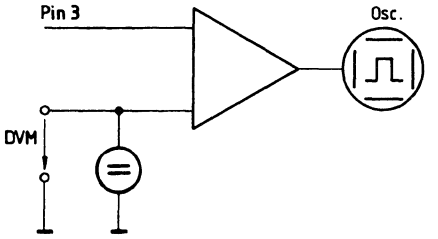


Residual pins are connected as in measurement circuit 1
The 10 µF capacitor at pin 5 serves only for test purposes

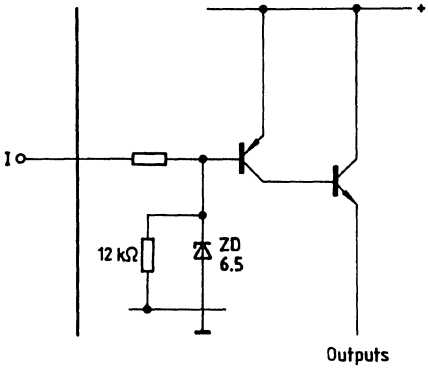
Measurement circuit 5



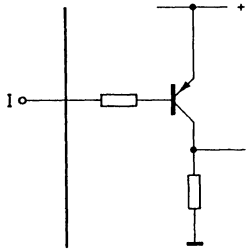
Measurement circuit 6



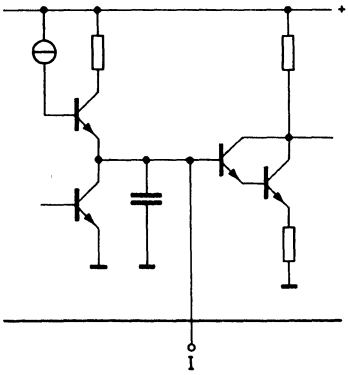
Inhibit 6



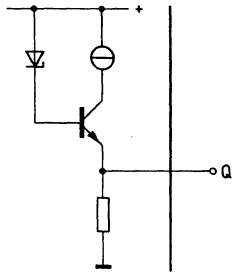
Long pulse 13



Pulse extension 12



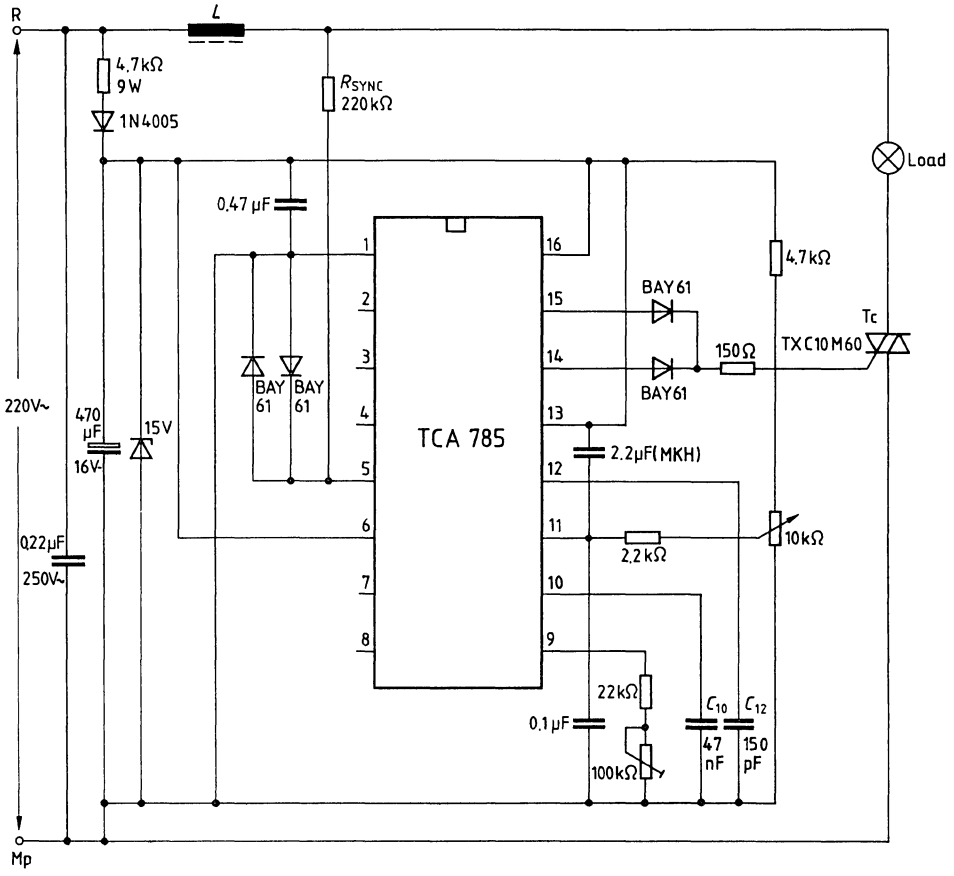
Reference voltage 8



Additional circuit description

Application examples

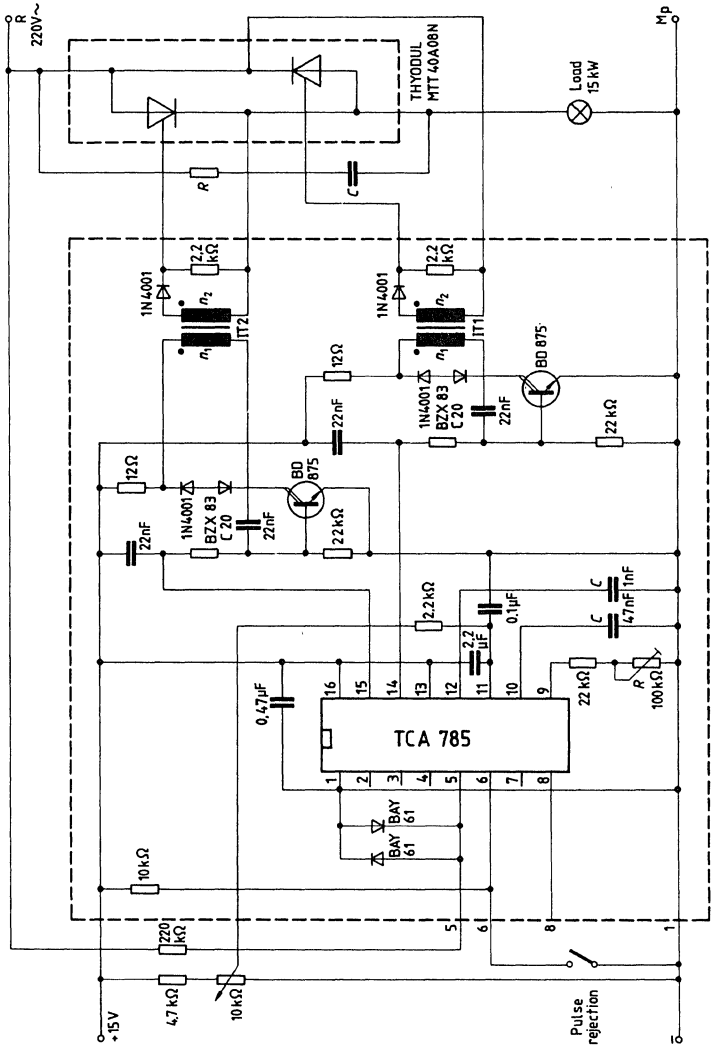
Triac control for up to 50 mA gate trigger current



A phase control with a diretly controlled triac is shown in the figure. The triggering angle of the triac can be adjusted continuously between 0° and 180° with the aid of an external potentiometer. During the positive half wave of the line voltage, the triac receives a positive gate pulse from the IC output pin 15. During the negative half wave, it receives also a positive trigger pulse from pin 14. Trigger pulse width is approx. 100 µs.

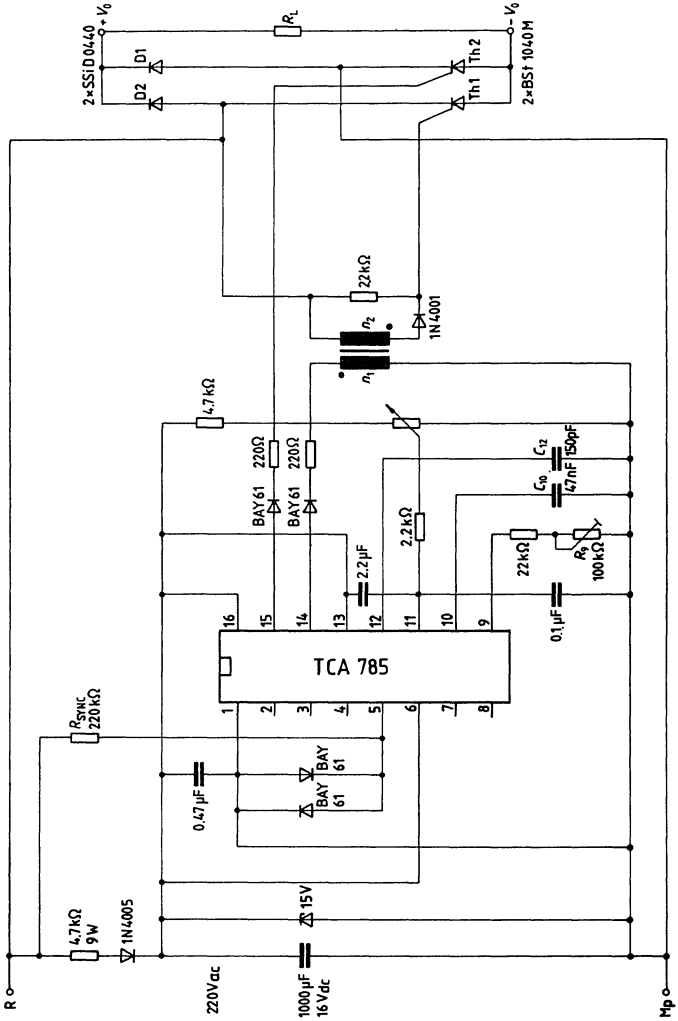
Fully controlled AC power controller

Circuit for two high-power thyristors

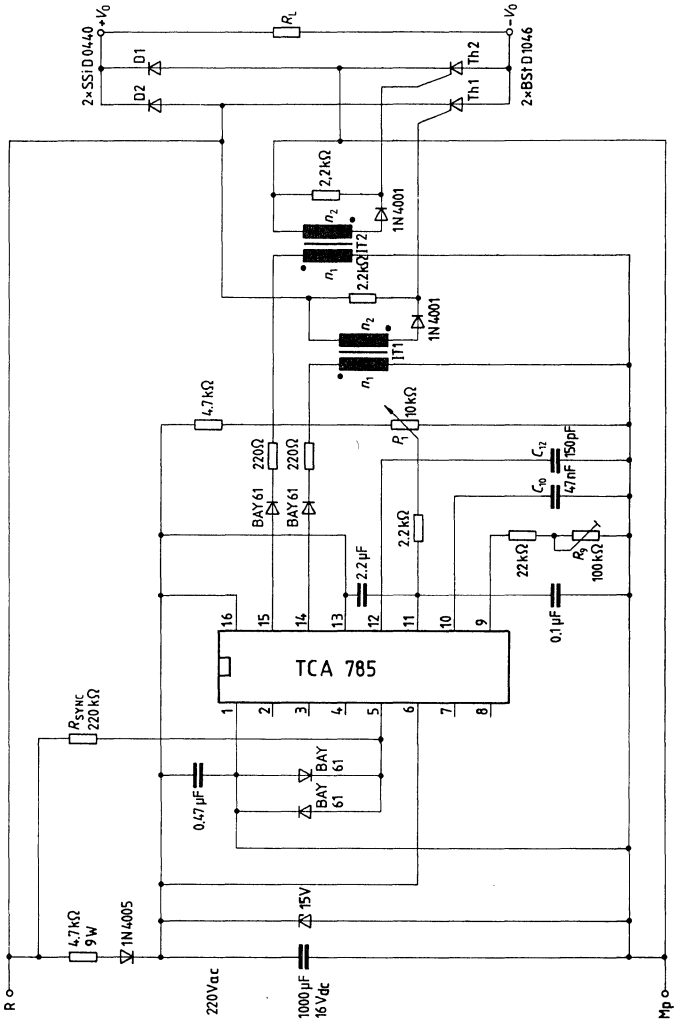


Shown is the possibility to trigger two antiparalleled thyristors with one IC TCA 785. The trigger pulses can be shifted continuously within a phase angle between 0° and 180° by means of a potentiometer. During the negative line half wave the trigger pulse of pin 14 is fed to the relevant thyristor via a trigger pulse transformer. During the positive line half wave, the gate of the second thyristor is triggered by a trigger pulse transformer at pin 15.

Half-controlled single-phase bridge circuit with trigger pulse transformer and direct control for low-power thyristors



Half-controlled single-phase bridge circuit with two trigger pulse transformers for low-power thyristors



DIP 16

The TCA 955 is suited for the speed control of dc motors. The principle corresponds to a clocked control. Outstanding features are its high control accuracy, its large supply voltage range, and the possible current saving. Additionally, the IC features a battery voltage indicator.

Typical applications

Speed control in

- tape recorders
- cassette recorders
- record players
- movie cameras
- control system drivers

Maximum ratings

Supply voltage	V_S	16	V
Supply voltage (pin 11 and pin 15 connected)	V_S	6	V
Output current pin 16	I_Q	200	mA
Output current pin 12 (LED output)	$I_{Q\,LED}$	15	mA
Power dissipation, LED output	$P_{Q\,LED}$	150	mW
Junction temperature	T_j	125	°C
Storage temperature range	T_{stg}	−55 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	85	K/W

Operating range

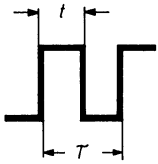
With internal short-circuit stabilization (pin 11 and pin 15 connected)	V_S	2 to 6	V
With internal stabilization (V_S to pin 15)	V_S	4.8 to 16.0	V
Ambient temperature range	T_{amb}	−25 to 85	°C

Characteristics

$T_{amb} = 25\,°C$; $V_S = 2.2\,V$ to $16.0\,V$

		min	typ	max	
Controller					
Current consumption $V_S = 4.8\,V$	I_S		8.3	12.0	mA
$V_S = 16\,V$	I_S		15.5	24.0	mA
Stabilized voltage $V_S = 4.8\,V$ to $16\,V$	V_{stab}	2.75	3.00	3.30	V
Input threshold (pin 3) to ground	V_I	$0.46 \times V_{11}$	$0.485 \times V_{11}$	$0.51 \times V_{11}$	V
Hysteresis of input threshold	ΔV_I		$0.015 \times V_{11}$	$0.03 \times V_{11}$	V
Offset voltage (pin 3 to pin 2)	V_{offset}		11	20	mV
Input current (pin 3)	I_I			1	µA
Output transistor saturation voltage					
$I_Q = 50\,mA$	$V_{Q\,sat}$		0.84	1.00	V
$I_Q = 100\,mA$	$V_{Q\,sat}$		0.92	1.25	V
Output transistor cutoff current	I_{QH}			30	µA
Duty cycle – control range[1]	ν	0		1	
Rated rpm[2]	n	$\frac{12{,}55}{p \cdot R_1 \cdot C_2}$	$\frac{14{,}85}{p \cdot R_1 \cdot C_2}$	$\frac{17{,}64}{p \cdot R_1 \cdot C_2}$	rpm
Error in rpm with duty cycle contrl[3] from 0 to 1				$\frac{0{,}224}{N \cdot p \cdot C_3}$	%
Switching oscillator					
Frequency	f		$\frac{1}{0{,}4 \cdot R_2 \cdot C_4}$		Hz
Average voltage pin 10	$V_{Q\,OSC}$		$0.48 \times V_{11}$		V
Voltage pin 11 peak to peak	$V_{Q\,OSC}$		$0.18 \times V_{11}$		V

1) Duty cycle



$\nu = \frac{t}{T}$

2) p = number of pole pairs of the tachometer generator.

3) in applications without switching oscillator.

Battery voltage indicator		min	typ	max	
Threshold voltage	$V_{I\,on}$			1.5	V
	$V_{I\,off}$	1.0			V
Hysteresis	V_{hy}		220		mV
Input current	I_I			0.2	µA
Saturation voltage	$V_{Q\,LED}$			0.5 + 500 x I_{LED}	V
LED output[1]					

Formulae:

Rate rpm $n = \dfrac{14{,}85}{p \cdot R_1 \cdot C_2}$ [rpm]

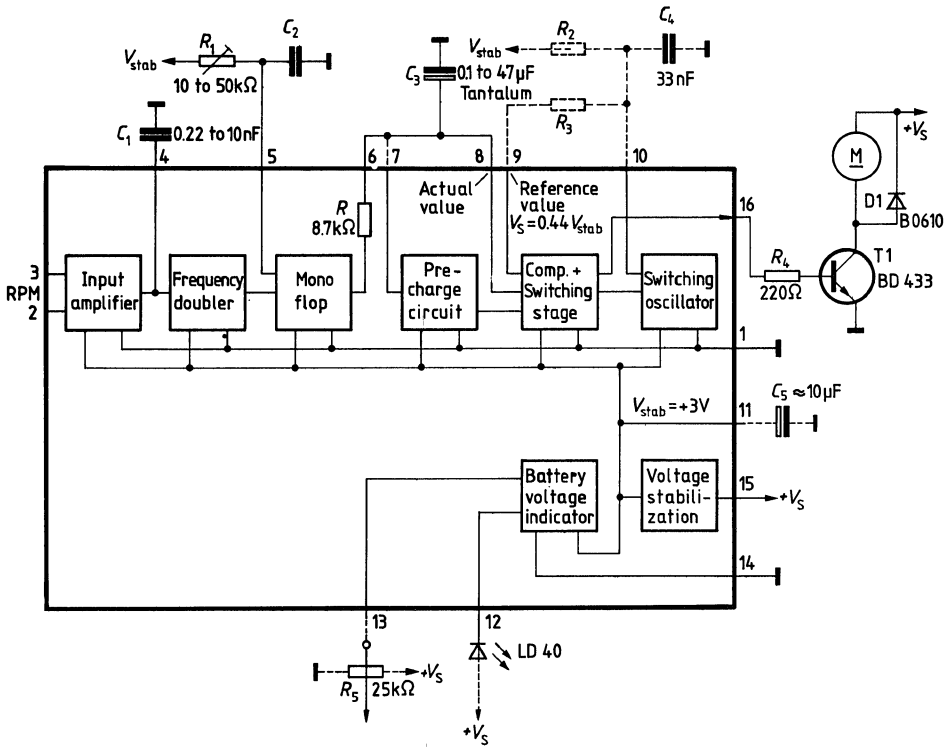
Switching frequency $f = \dfrac{n \cdot p}{30}$ [Hz]

in operation without switching oscillator.

Reference value $V_{ref} = 0.44 \times V_{11}$ [V]
Precharging voltage at C_3 $V_F = 0.87 \times V_{ref}$ [V]
(pin 6 and pin 7 connected)

1) A protective resistor of 500 Ω ± 20% is integrated inside the IC.

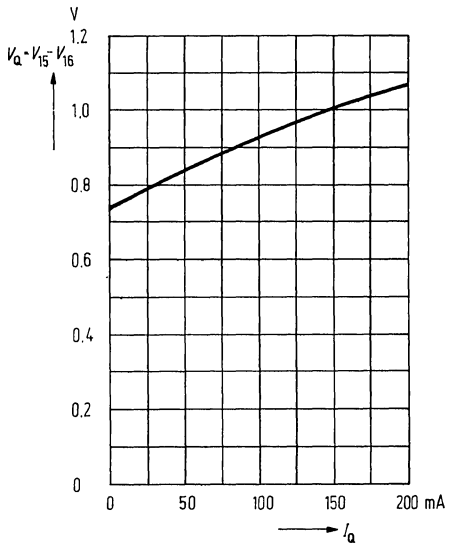
Block diagram for speed control with TCA 955



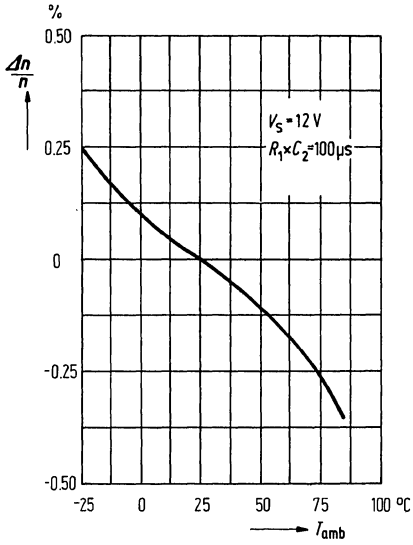
Dimensioning notes

1. The internal voltage stabilization offers the following advantages:
   — operation with highly varying supply voltage,
   — wide range of supply voltage.
2. In order to receive pulses with a steady duty cycle at the output, symmetrical pulses must be applied to the input.
3. It is recommended to use multipole tachometer generators as this improves the accuracy of control and possibly the power consumption.
4. The power consumption can considerably be reduced by means of the switching frequency oscillator at low electric motor time constants.
5. Higher accuracy can be obtained by using a second-order filter instead of C_3.
6. When using rapidly starting motors, the precharge circuitry reduces overshoots.

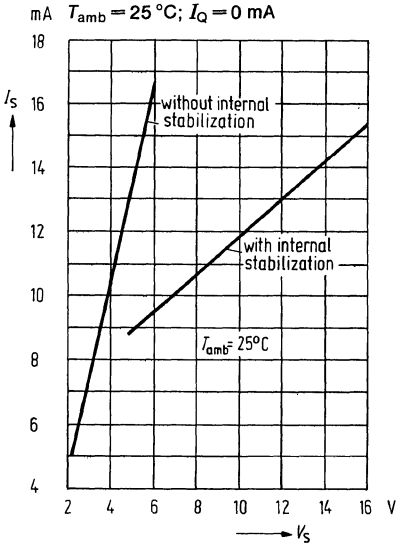
Saturation voltage of output transistor
Output voltage versus output current



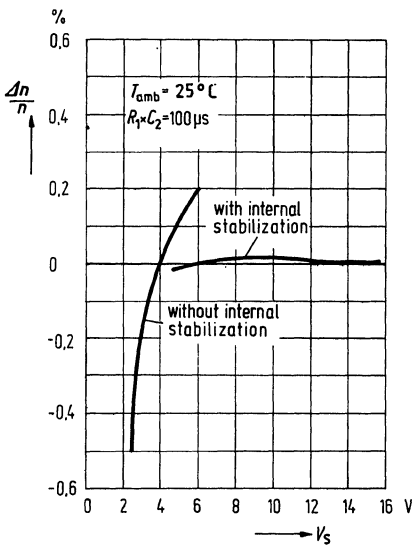
Rpm versus ambient temperature
$V_S = 12$ V; $R_1 \times C_2 = 100$ µs



Current consumption
versus supply voltage
$T_{amb} = 25$ °C; $I_Q = 0$ mA



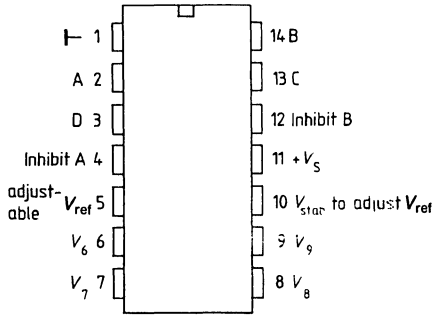
Rpm versus supply voltage
$T_{amb} = 25$ °C; $R_1 \times C_2 = 100$ µs



DIP 14

The TCA 965 window discriminator is particularly suited for control systems as follow-up and adjusting control device with dead space. It can also be used in measuring systems for the selection of elements whose dc values should remain within tolerated deviations from required values.

Pin configuration



Maximum ratings

Supply voltage	V_S	27	V
Input voltage difference between inputs 6, 7 and 8	V_I	15	V
Input voltage (pin 9)	V_I	30	V
Output current (pin 2, 3, 13, 14)	I_Q	50	mA
Stabilized voltage output current (pin 10)	I_Q	10	mA
Junction temperature	T_j	125	°C
Storage temperature range	T_{stg}	−55 to 125	°C
Thermal resistane (system-air)	$R_{th\ SA}$	80	K/W

Operating range

Supply voltage range	V_S	4.75 to 27	V
Ambient temperature range	T_{amb}	−25 to 85	°C

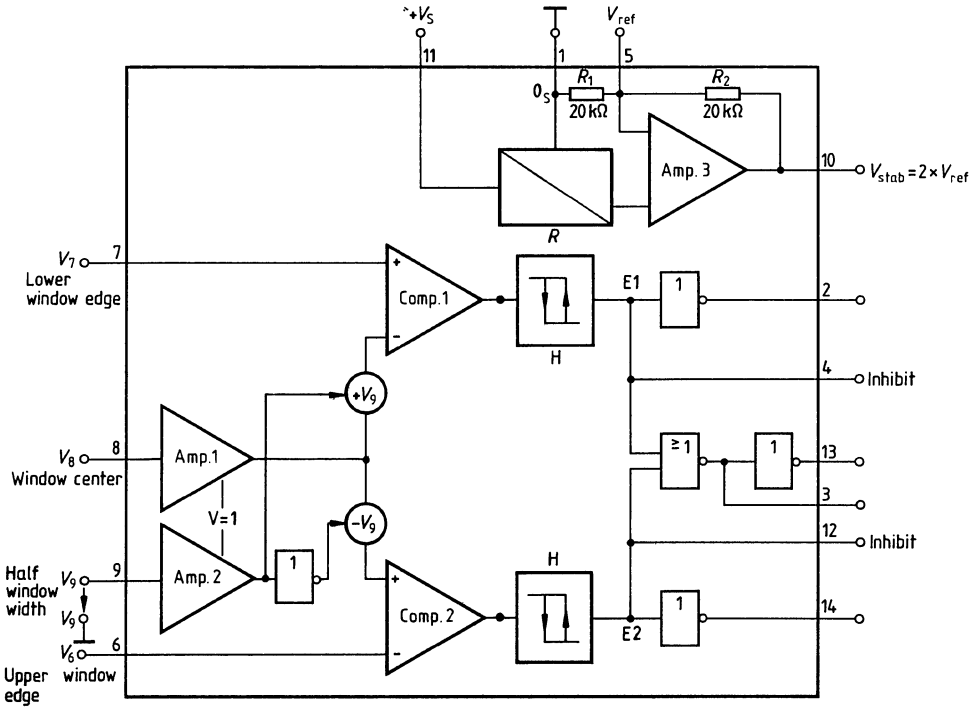
Characteristics

$V_S = 10$ V; $T_{amb} = 25$ °C

		Test conditions	min	typ	max	
Current consumption	I_S	V_2, $V_{13} = V_{QH}$		5	7	mA
Input current (pin 6, 7, 8)	I_I			20	50	nA
Input current (pin 9)	$-I_I$			400	3000	nA
Input offset voltage (pin 6/8, pin 7/8)	V_{IO}		−20	± 10	20	mV
Input voltage range (pin 6, 7, 8)	V_I	$\Delta V_I < 13$ V	1.5		V_S−1.0	V
Input voltage range (pin 9)	V_I		50		$\frac{V_S}{2}$	mV
Differential input voltage	$V_6-(V_8-V_9)$				13	V
	$(V_8+V_9)-V_7$				13	V
Reference voltage	V_5	$I_{ref} = 0$	2.8	3.0	3.2	V
Stabilized voltage	V_{10}	$V_S > 7.9$ V	5.5	6	6.5	V
Temperature coefficient of reference voltage	αV_5			0.5		mV/K
Sensitivity of reference voltage to supply voltage variations	$\frac{\Delta V_5}{\Delta V_S}$			3		mV/V
Output reverse current	I_{QH}				10	µA
L output voltage	V_{QL}	$I_Q = 10$ mA			200	mV
		$I_Q = 40$ mA			800	mV
Hysteresis (window edges)	V_{hy}		18	22	35	mV
Inhibit threshold[1]	$V_{4,12}$			1.5		V
Inhibit current	$I_{4,12}$			−100		µA

1) Inhibition occurs if pin 4 and 12 are grounded.

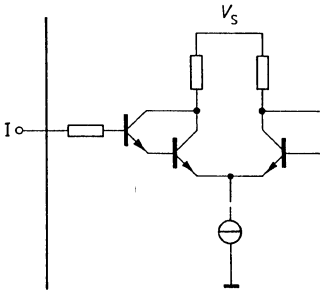
Block diagram



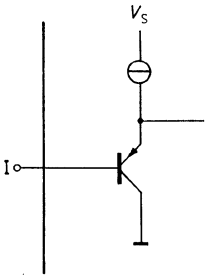
Schematic circuit diagrams

Inputs

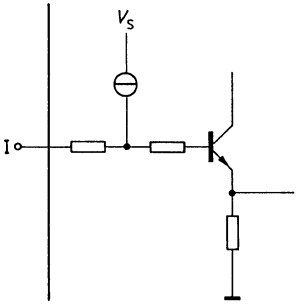
Pin 6, 7, 8



Pin 9

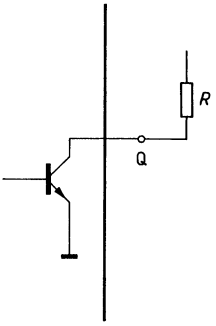


Pin 4, 12

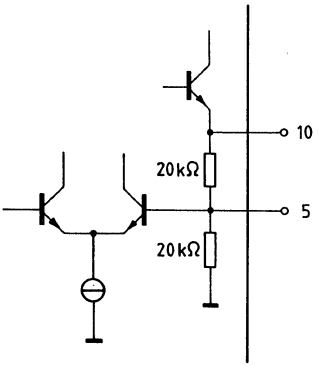


Outputs

Pin 2, 3, 13, 14



Pin 5, 10



Suggestions for application

The window discriminator analyzes the input voltage with reference to two limits that are input as voltages. The window, within which the circuit reacts »well« can be input either by an upper (V_6) and a lower limit (V_7), or by the window center (V_8) and depending upon that, by a voltage ΔV, (V_9), which corresponds to half window width and is available to ground. A Schmitt trigger characteristic with a small hysteresis is effective at the switching points. Four output signals are available having the following meanings: input signal inside, outside the window (good, bad), too high, too low. All outputs have open collectors that can carry up to 50 mA for the control of small relays, lamps, LEDs. All the usual logic families can be driven directly requiring only few external components.

Additionally, the IC contains a reference voltage source with adjustable amplifier (V_{ref}) for the generation of various reference voltages (V_{stab}) for the inputs. The reference voltage source is, to a large extent, independent of temperature and supply voltage. For stabilization purposes, it requires a capacitor of up to 10 µF (electrolytic capacitor) to ground at pin 10.

Truth table (for block diagram in connection with application circuit I and II).

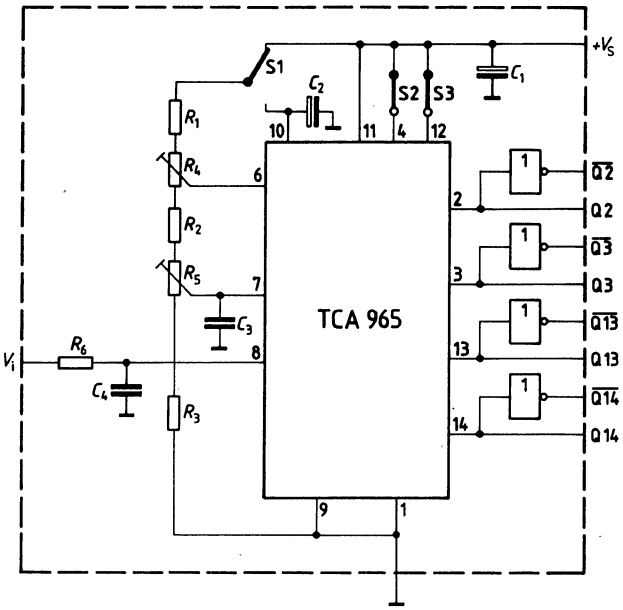
V_I	
Application circuit I $V_I = V_8$	Application circuit II $V_I = V_{6/7}$
$V_8 < (V_7 - V_9)$	$V_{6/7} > (V_8 + V_9)$
$V_8 > (V_6 + V_9)$	$V_{6/7} < (V_8 - V_9)$
$(V_6 + V_9) > V_8 > (V_7 - V_9)$	$(V_8 + V_9) > V_{6/7} > (V_8 - V_9)$
$V_6 + V_9$ – – – upper window edge $V_7 - V_9$ – – – lower window edge $(V_6 + V_9) - (V_7 - V_9)$ – – – – – window width	V_8 – – – window center V_9 – – – half window width (to ground)

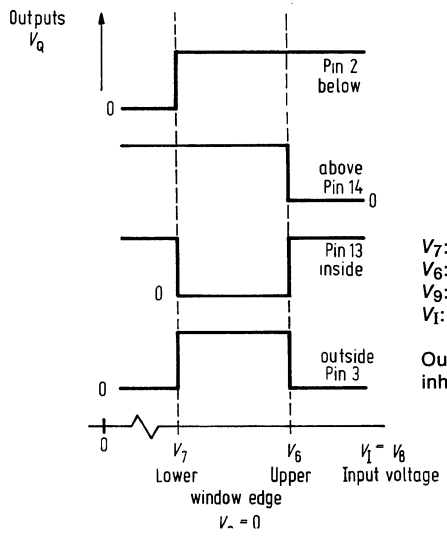
Outputs			
pin 2	14	13	3
L(H)	H(H)	H(L)	L(H)[1]
H(H)	L(H)	H(L)	L(H)[2]
H	H	L	H

Values in brackets refer to external inhibition via pin 4 and pin 12
[1] inhibition pin 4 to ground
[2] inhibition pin 12 to ground

Application circuit I

Outputs: pin 2 »below«
pin 3 »outside«
pin 13 »inside«
pin 14 »above«



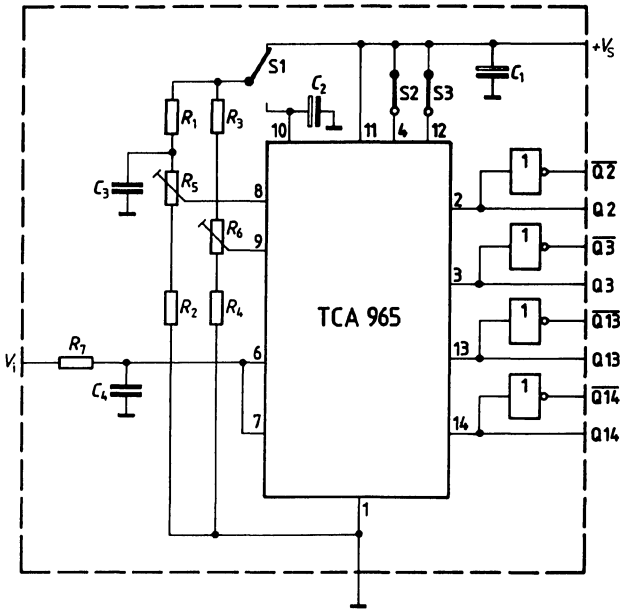


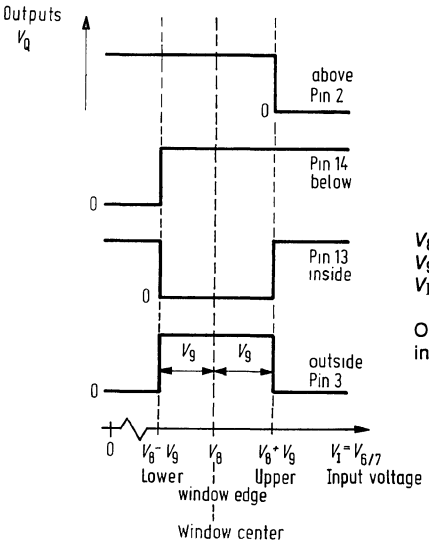
V_7: lower threshold
V_6: upper threshold
V_9: 0 V
V_I: at pin 8

Outputs pin 2 and pin 14 can be inhibited externally and are then H.

Application circuit II

Outputs: pin 2 »above«
pin 3 »outside«
pin 13 »inside«
pin 14 »below«





V_8: window center
V_9: ± half window width
V_I: pin 6 and pin 7 connected

Outputs pin 2 and pin 14 can be inhibited externally and are then H.

Examples of circuit-board design for application circuits I and II

The inputs of the TCA 965 window discriminator have a Schmitt-trigger characteristic. With an input voltage that crosses the switching threshold very slowly there is nevertheless a risk of the output concerned going into oscillation before it clearly assumes the new switching state. The following circuit boards were designed specially to allow for this factor and offer a maximum possible safeguard against oscillations.

The causes of the undesired response are as follows:

1. **Feedback effect** of the switched load on the window-edge voltage through loading or unloading of the supply voltage.
2. **Hum voltages** that are superimposed on the input signal or the window-edge voltages derived from the supply voltage.
3. Unfavorable **routing of the tracks** on the circuit board with the voltage dividers for the window edges connected to a point of the grounding that alters in potential as a result of load variations. Pin 1 of the TCA 965 can take a load current of 2 x 50 mA to ground.

Remedies for 1

Boundary conditions for non-oscillating operation	
Application circuit I $V_6 = k \cdot V_S$, $V_7 = k' \cdot V_S$	Application circuit II $V_8 = k \cdot V_S$, $V_9 = k' \cdot V_S$
Condition $k \cdot \Delta V_S < V_{hy\,min}$ $k' \cdot \Delta V_S < V_{hy\,min}$	Condition $(k + k') \cdot \Delta V_S < V_{hy\,min}$

If these conditions are not fulfilled, no holding up of the window-edge voltages with capacitors will help. Instead one of the following three measures must be taken:

use of V_{stab} for deriving the window-edge voltages,

- isolation of the supply voltage V'_S for the load from the supply voltage V_S of the TCA 965,
- increase of the edge hysteresis according to the technical note on the TCA 965.

Remedies for 2

Boundary condition

$V_{hum\ pp}/2 < V_{hy\ min}$

What decides fulfilment of the boundary condition is, depending on the particular application circuit, the sum of the hum voltages affecting the comparator concerned. The following interference suppression measures are suggested:

filtering of the input and window-edge voltage,

increase of the edge hysteresis[1].

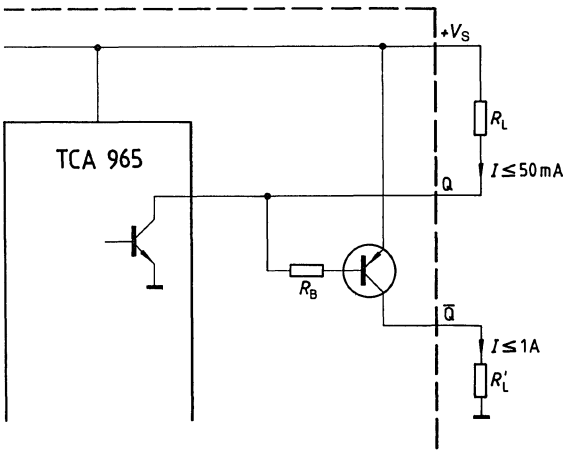
Remedies for 3

The circuit-board suggestions for the two application circuits have optimal grounding to the voltage dividers for the window edges with filtering of the supply voltage directly on the IC.

If several of the above-mentioned causes occur simultaneously, the remedies should be applied in the given sequence.

Output wiring

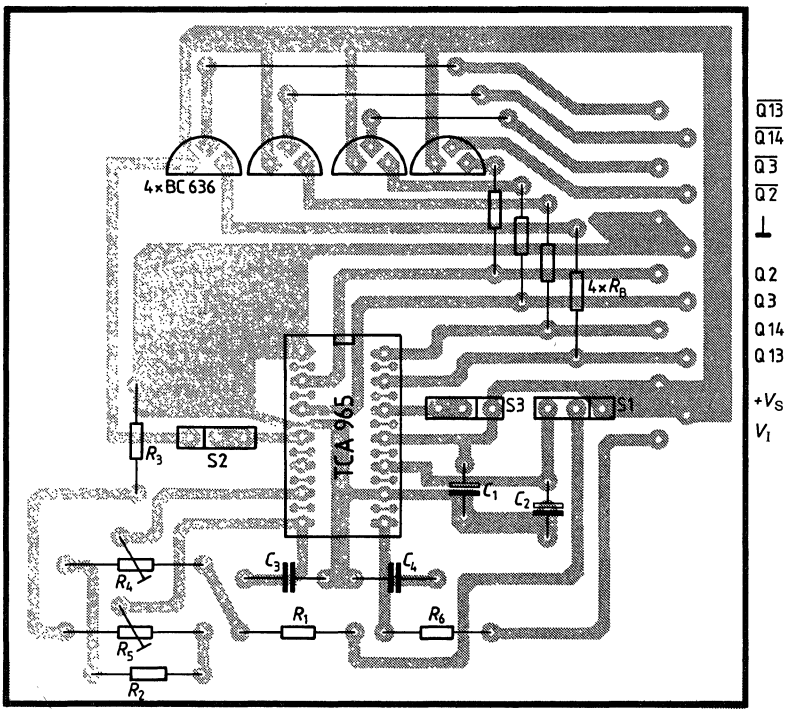
There are additional driver stages at the outputs of the TCA 965 as shown in the following diagram for switching load currents up to 1 A (outputs $\overline{Q}$)



1) Outputs 2, 3, 13, 14

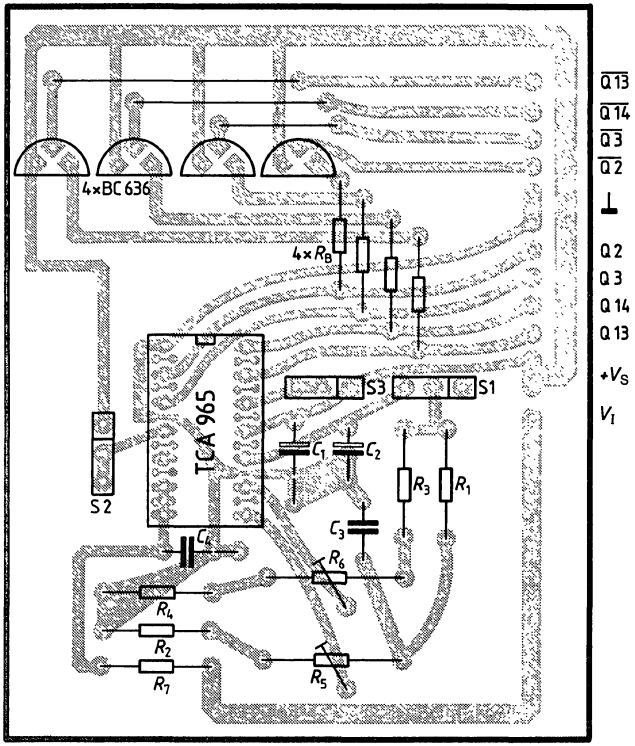
Circuit board and component layout

Application circuit I



Circuit board and component layout

Application circuit II



Preliminary data TO-220

The TCA 1365 is a power op amp in a plastic power package similar to TO 220. At maximum supply voltage of ±21 V it delivers a high output current of 3.5 A. The op amp is protected against short circuits and thermal overload.

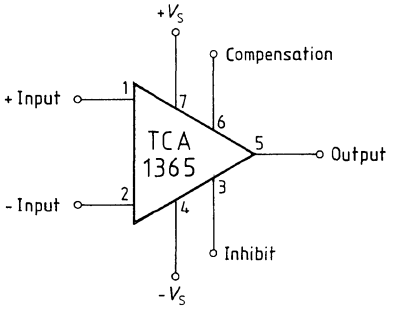
Features

- High peak output current up to 3.5 A
- High supply voltage up to 42 V
- Suitable up to gain of 1
- Thermal overload protection
- Internal power limiting
- External compensation
- Inhibit input (TTL-compatible)
- DC short-circuit protection to $+V_S$ and $-V_S$

Applications

- Power comparator
- Power Schmitt-trigger
- Speed control of dc motors
- Power buffer

Pin configuration



Pin 4 is electrically connected to cooling fin.

Maximum ratings

Supply voltage	V_S	±21	V
Differential input voltage	V_{ID}	$\pm V_S$	V
Supply current	I_S	4.0	A
Ground current (min./max.)	I_{GND}	−4.0 to +3.5	A
Output voltage	V_Q	V_S +1	V
Peak output current	I_Q	3.5	A
Current pin 3, 7	$I_{3,7}$	5	mA
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−50 to 150	°C
Power dissipation (at $T_C = 85$ °C)	P_{tot}	13	W
Thermal resistance (system-case)	$R_{th\,SC}$	5	K/W

Operating range

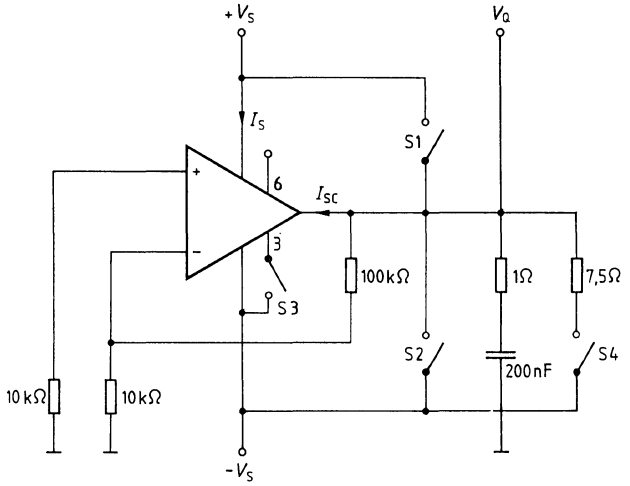
Supply voltage	V_S	±3 to ±20	V
Case temperature	T_C	−25 to 85	°C

Characteristics $V_S = \pm 15$ V, $T_C = 25$ °C		Test circuit	min	typ	max	
Open-loop supply current consumption	I_S	1		20	40	mA
Input offset voltage	V_{IO}	2	−10		10	mV
Input offset current	I_{IO}	3	−100		100	nA
Input current	I_I	3		0.2	1	µA
Output voltage						
$R_L = 12\ \Omega$, $f = 1$ kHz	V_{Qpp}	4	±13.0	±13.5		V
$R_L = 4\ \Omega$, $f = 1$ kHz	V_{Qpp}		±12.5	±13.0		V
Input resistance $f = 1$ kHz	R_I	4	1	5		MΩ
Open-loop voltage gain $f = 100$ Hz	G_{V0}	5	70	80		dB
Common-mode input voltage	V_{IC}	6	+13/−15	+13.5/−15.1		V
Common-mode rejection	k_{CMR}	6	70	80		dB
Supply voltage rejection	k_{SVR}	7	−70	−80		dB
Temperature coefficient of V_{IO} $-25 \le T_C \le 85$ °C	α_{VIO}	2		50		µV/K
Temperature coefficient of I_{IO} $-25 \le T_C \le 85$ °C	α_{IIO}	3		0.4		nA/K
Slew rate of V_Q for non-inverting operation	SR	8		0.5		V/µs
Slew rate of V_Q for inverting operation	SR	9		0.5		V/µs
Disturbance voltage referred to input DIN 45405	V_d	1		2	5	µV
Short-circuit current						
(S1 closed)	I_{SC}	1		0.75		A
(S2 closed)	I_{SC}	1		−0.75		A
Open-loop supply current consumption (S3 open; $V_3 \ge 2$ V)[3]	I_S	1		1.5	3.5	mA
Inhibit input (pin 3)						
V_3 for amp off V_3 for amp on } [3]	$V_{3\,off}$ $V_{3\,on}$	1 1	2		 0.5	V V } [1]
Turn-on time $I_Q \ge 1$ A	$t_{d\,on}$	1		2	5	µs } [2]
Turn-off time $I_Q \le 1$ A	$t_{d\,off}$	1		30	50	µs } [2]

[1] S3 open
[2] S4 closed
[3] referred to $-V_S$

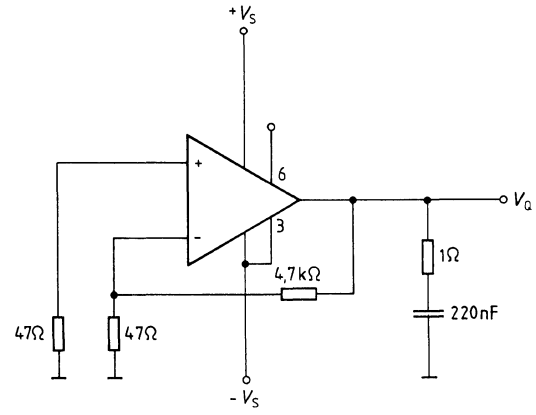
Test circuits

Figure 1 Open-loop supply current consumption; disturbance voltage



S1 to S4 as shown unless otherwise specified

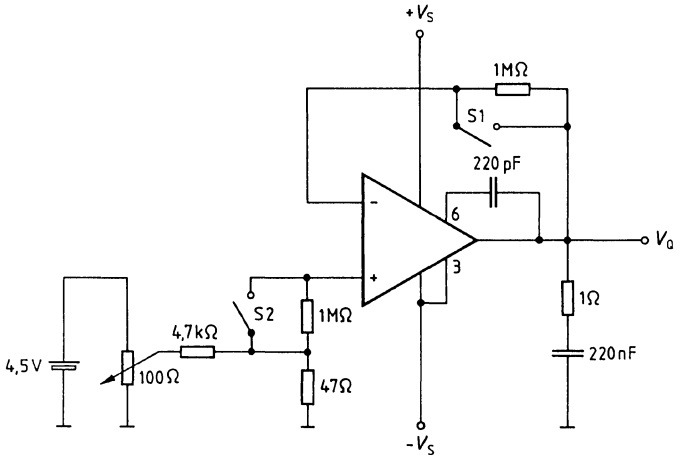
Figure 2 Input offset voltage, temperature coefficient of V_{IO}



$V_Q = 100\ V_{IO}$

Test circuits

Figure 3 Input offset current; input current, temperature coefficient of I_{IO}



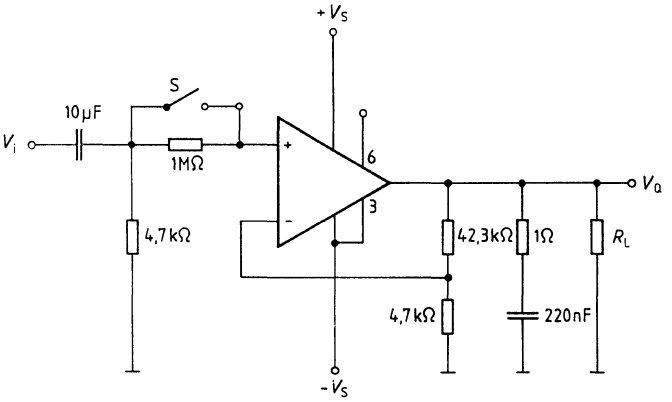
S1 open – S2 closed: $I_{I-} = \frac{V_Q}{1\ M\Omega}$

S2 open – S1 closed: $I_{I+} = \frac{V_Q}{1\ M\Omega}$

S1 open – S2 open: $I_{IO} = \frac{V_Q}{1\ M\Omega}$

S1 closed – S2 closed: offset alignment

Figure 4 Output voltage, input resistance



S closed: to measure V_{Qpp}
S open/closed: to measure R_I

Test circuits

Figure 5 Open-loop voltage gain

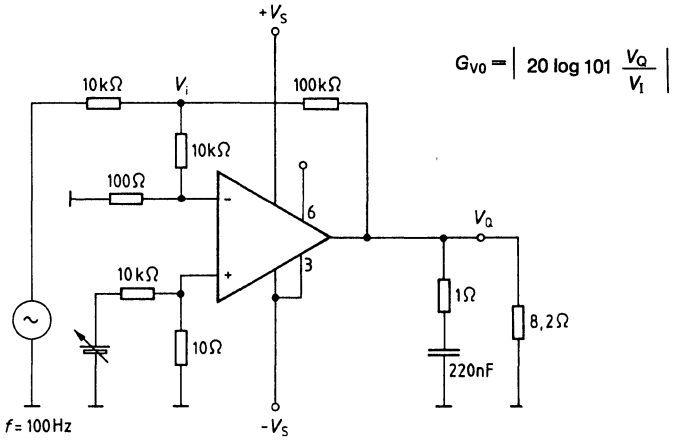
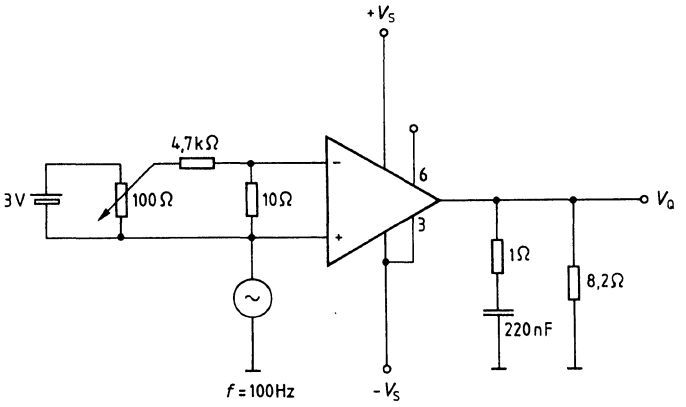
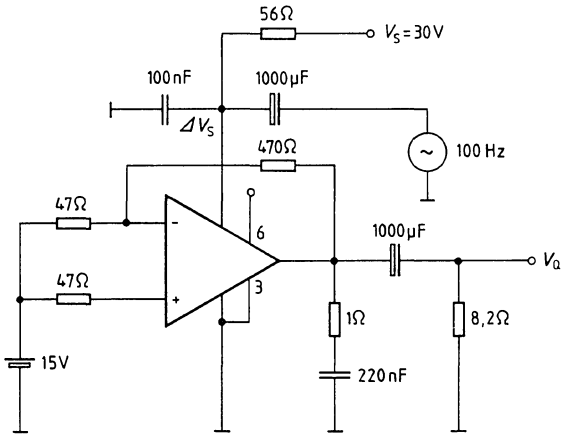


Figure 6 Common-mode voltage gain G_{VC}
Common-mode rejection k_{CMR} (dB) = G_{V0} (dB) −G_{VC} (dB)



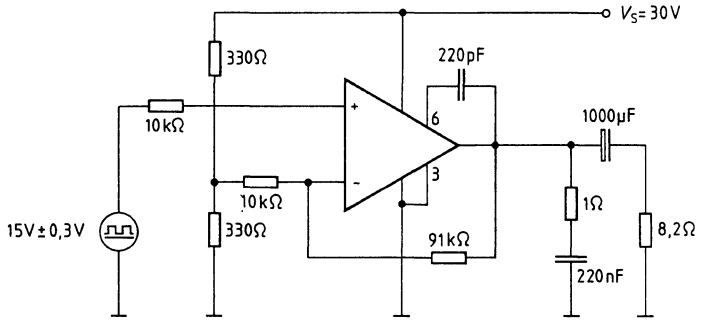
Test circuits

Figure 7 Supply-voltage rejection



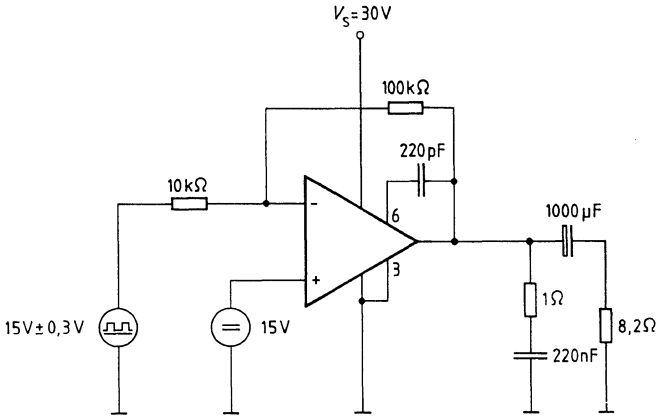
$$k_{SVR} = 20 \log \frac{\Delta V_Q}{G_V \times \Delta V_S} \text{ (dB)}$$

Figure 8 Slew rate for non-inverting operation

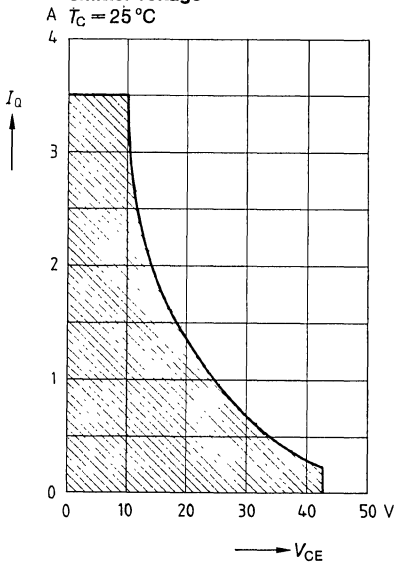


Test circuit

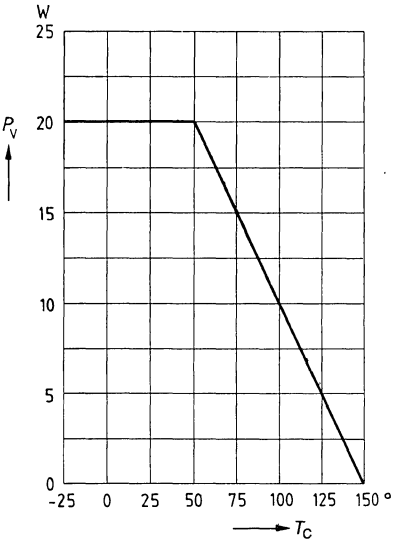
Figure 9 Slew rate for inverting operation



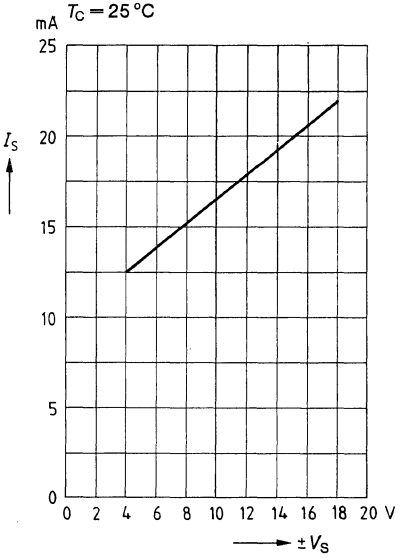
Safe operating area of output stage
Output current versus collector emitter voltage



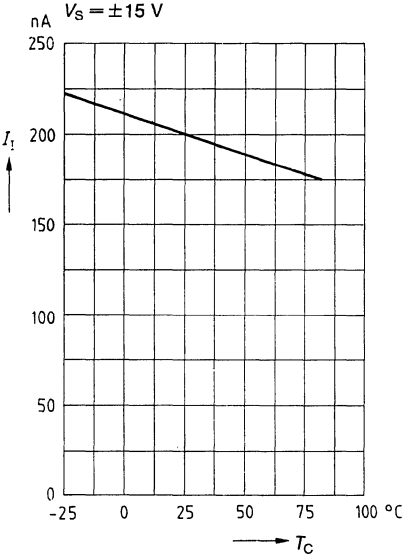
Maximum permissible power dissipation versus case temperature



Supply current versus supply voltage
$T_C = 25\,°C$

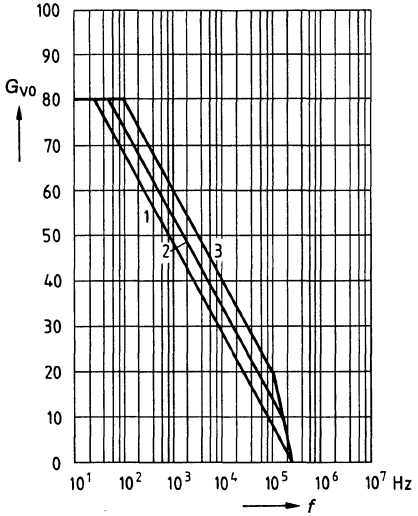


Input current versus case temperature
$V_S = \pm 15\,V$



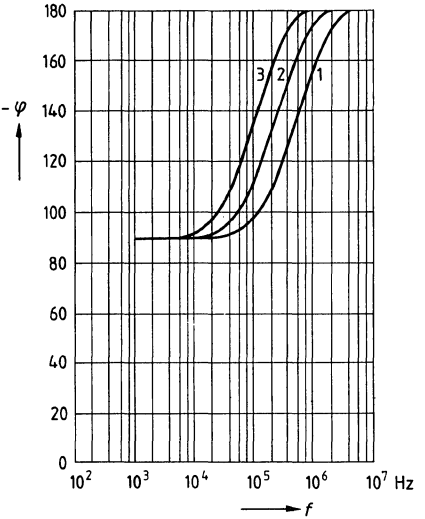
Open-loop voltage gain versus frequency

$T_C = 25\,°C$; $V_S = \pm 15$ V



Phase response versus frequency

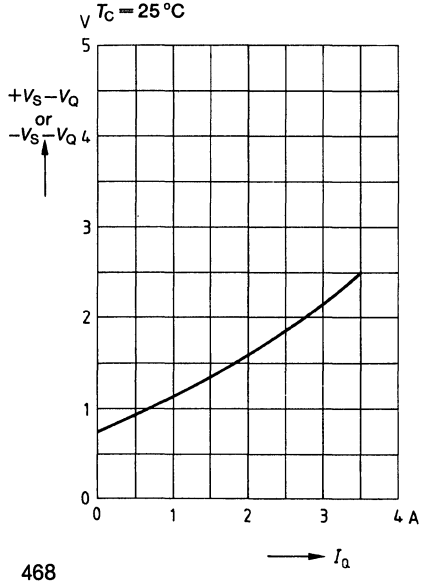
$T_C = 25\,°C$; $V_S = \pm 15$ V



1: $C_{5\text{-}6} = 220$ pF; 2: $C_{5\text{-}6} = 100$ pF; 3: $C_{5\text{-}6} = 0$ pF

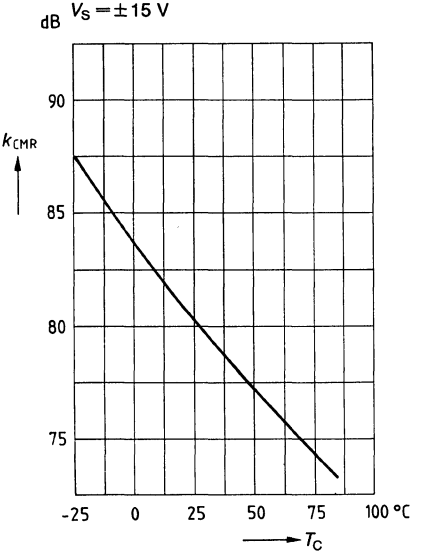
Saturation voltage versus output current

$T_C = 25\,°C$



Common-mode rejection versus case temperature

$V_S = \pm 15$ V



Preliminary data

DIP18
SIP 9

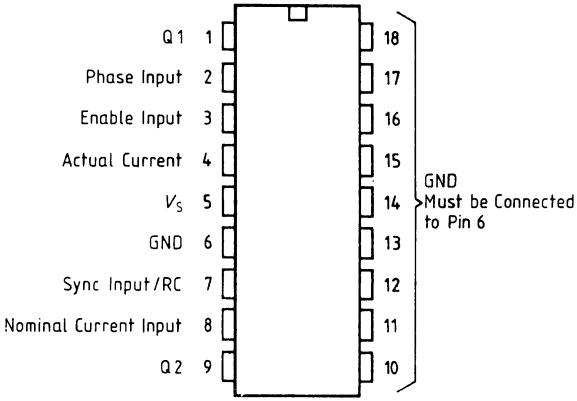
The TCA 1560/61 is a bipolar monolithic IC designed to control the motor current in one phase of a bipolar stepper motor.

It has TTL compatible logic inputs and contains a full-bridge driver with integrated, high-speed clamp diodes and chopper-operated dynamic motor current limiting. The nominal current is infinitely variable up to 2 A with a control voltage. Using minimum external components and a single supply voltage, two TCA 1561 ICs form a complete and directly MC-drivable system for two-phase bipolar stepper motors. TCA 1560 in DIP 18 package is functionally identical but with an output current up to 1A.

Features

- 2 A peak current
- high-speed integrated clamp diodes
- low saturation voltages
- thermal overload protection with hysteresis

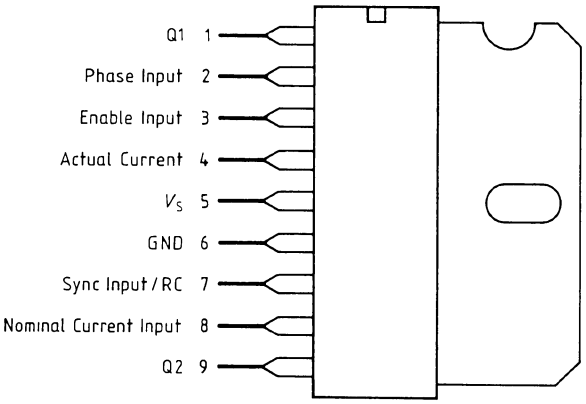
Pin configuration
(top view)



Pin description

Pin	Function
1	Output Q1
2	Phase input
3	Enable input
4	Actual current
5	Supply voltage
6	GND
7	Sync input/RC
8	Nominal current input
9	Output Q2
10–18	Ground: must be connected to pin 6

Pin configuration



Pin description

Pin	Function
1	Output Q1
2	Phase input
3	Enable input
4	Actual current
5	Supply voltage
6	GND
7	Sync input/RC
8	Nominal current input
9	Output Q2

The cooling fin is connected internally to pin 6 (ground).

Maximum ratings

		min	max	
Supply voltage, pin 5	V_S	−0.3	45	V
Supply current, pin 5	I_S	0	1.25	A
Output voltage, pins 1, 9	V_Q	−1.5	V_S +1.5	V
Output peak current, pins 1, 9	I_Q	−1	1	A
Input voltage, pins 2, 3, 7, 8	V_I	−0.3	6	V
Output current, pin 4	I_4	−0.003	1.25	A
Voltage, pin 4	V_4	−0.3	5	V
Ground current, pin 6	I_6		1	A
Chip temperature	T_C		150[1)]	°C
Storage temperature	T_{stg}	−40	125	°C
Thermal resistance				
System-environment	$R_{th\,SA}$		70	K/W
System-package (measured at pin 14)	$R_{th\,SC}$		15	K/W

Operating range

Supply voltage, pin 5	V_S	10	38	V
Package temperature	T_C	−25	85	°C
Input voltage, pins 2, 3, 7	V_I		5	V

[1)] ICs provide optimal reliability and service life if the junction temperature does not exceed 125 °C in operation. Operation up to the maximum permissible limit of the junction temperature at 150 °C is possible in principle. It should be noted, however, that exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Characteristics

$T_C = 25\,°C$; $V_S = 24\,V$

		Test conditions	min	typ	max	
Supply current, pin 5	I_S	$V_{I3} = V_{IH}$		18	30	mA
Standby current consumption, pin 5	I_S	$V_{I3} = V_{IL}$		0.5	1	mA
Outputs, pins 1, 9						
Output voltage: source	V_{QH}	$\lvert I_Q \rvert = 0.5\,A$			1.7	V
Output voltage: sink	V_{QL}	$\lvert I_Q \rvert = 0.5\,A$			1.1	V
Reverse current	$\lvert I_{QS} \rvert$				300	µA
Phase dead time	t_T	figure 1	0.1	0.3	1.0	µs
Forward voltage of clamp diodes	V_D	$I_D = 1\,A$			1.4	V
Inputs: enable, pin 3 and phase, pin 2						
H input voltage	V_{IH}		2			V
L input voltage	V_{IL}				0.8	V
H input current	I_{IH}	$V_{IH} = 5\,V$		50	100	µA
L input current	$-I_{IL}$	$V_{IL} = 0\,V$			100	µA
Rise and fall time	t_r, t_f				2	µs
Nominal current, pin 8						
Regulating range	V_{I8}		0		2	V
Input current	$-I_{I8}$	$V_{I8} = 0\,V$			5	µA
Input offset voltage	$V_{I(8-4)}$	figure 5		0		mV
Actual current, pin 4						
Regulating range	V_{I4}		0		2	V
Turn-off delay	t_d	figure 3		2	3	µs
Sync input/RC, pin 7						
Sync frequency	f	duty cycle: 0.5	1		100	kHz
Duty cycle	ν	$f = 40\,kHz$	0.1		0.9	
Rise and fall time	t_r, t_f				2	µs
Output current, pin 7	$-I_{Q7}$		1.2	1.6	2.0	mA
Trigger threshold, pin 7	V_{L7}	figure 2		0.6	0.8	V
Charging limit C_7	V_{G7}		2.2	2.4		V
Off period	t_s	figure 4		64		µs
Dynamic input resistance, pin 7	R_{i7}	$V_7 = 1.5\,V$		1		kΩ

Maximum ratings

		min	max	
Supply voltage, pin 5	V_S	−0.3	45	V
Supply current, pin 5	I_S	0	2.5	A
Output voltage, pins 1, 9	V_Q	−2	V_S +1.5	V
Output peak current, pins 1, 9[1]	I_Q	−2	2	A
Input voltage, pins 2, 3, 7, 8	V_I	−0.3	6	V
Output current, pin 4	I_4	−0.003	2.5	A
Voltage, pin 4	V_4	−0.3	5	V
Ground current, pin 6	I_6		2	A
Chip temperature[2]	T_C		150	°C
Storage temperature	T_{stg}	−40	125	°C
Thermal resistance				
System-environment	$R_{th\,SA}$		70	K/W
System-package	$R_{th\,SC}$		8	K/W

Operating range

Supply voltage, pin 5	V_S	10	38	V
Package temperature	T_C	−25	85	°C
Input voltage, pins 2, 3, 7	V_I		5	V

[1] In case of chopper operation with peak currents exceeding 1 A, one diode per output (pin 1, 9) has to be connected with the cathode to the supply voltage (pin 5)
The reverse-recovery time of diodes must not exceed 200 ns.

[2] ICs provide optimal reliability and service life if the junction temperature does not exceed 125 °C in operation. Operation up to the maximum permissible limit of the junction temperature at 150 °C is possible in principle. It should be noted, however, that exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Characteristics

$T_C = 25\,°C$; $V_S = 24$ V

		Test conditions	min	typ	max	
Supply current, pin 5	I_S	$V_{I3} = V_{IH}$		18	30	mA
Standby current consumption, pin 5	I_S	V_{I3}		0.5	1	mA
Outputs, pin 1, 9						
Output voltage: source	V_{QH}	$\lvert I_Q \rvert = 0.3$ A			1.6	V
Output voltage: source	V_{QH}	$\lvert I_Q \rvert = 1.3$ A			1.9	V
Output voltage: sink	V_{QL}	$\lvert I_Q \rvert = 0.3$ A			1.0	V
Output voltage: sink	V_{QL}	$\lvert I_Q \rvert = 1.3$ A			1.4	V
Reverse current	$\lvert I_{QS} \rvert$				300	µA
Phase dead time	t_T	figure 1	0.1	0.3	1.0	µs
Forward voltage of clamp diodes	V_D	$I_D = 1$ A			1.4	V
Inputs: enable, pin 3 and phase, pin 2						
H input voltage	V_{IH}		2			V
L input voltage	V_{IL}				0.8	V
H input current	I_{IH}	$V_{IH} = 5$ V		50	100	µA
L input current	$-I_{IL}$	$V_{IL} = 0$ V			100	µA
Rise and fall time	t_r, t_f				2	µs
Nominal current, pin 8						
Regulating range	V_{I8}		0		2	V
Input current	$-I_{I8}$	$V_{I8} = 0$ V			5	µA
Input offset voltage	$V_{I(8-4)}$	figure 5		0		mV
Actual current, pin 4						
Regulating range	V_{I4}		0		2	V
Turn-off delay	t_d	figure 3		2	3	µs
Sync input/RC, pin 7						
Sync frequency	f	duty cycle: 0.5	1		100	kHz
Duty cycle	ν	$f = 40$ kHz	0.1		0.9	
Rise and fall time	t_r, t_f				2	µs
Output current, pin 7	$-I_{Q7}$		1.2	1.6	2.0	mA
Trigger threshold, pin 7	V_{L7}	figure 2		0.6	0.8	V
Charging limit C_7	V_{G7}		2.2	2.4		V
Off period	t_s	figure 4		64		µs
Dynamic input resistance, pin 7	R_{i7}	$V_7 = 1.5$ V		1		kΩ

Circuit description

Outputs

Outputs Q1, Q2 (pins 1, 9) are fed by push-pull output stages. The two integrated clamp diodes, referred to ground or supply voltage respectively, protect the IC against flyback voltages from an inductive load.

Enable

Outputs Q1 and Q2 are turned off when voltage $V_{I3} \leq 0.8$ V is applied to pin 3. The supply current then decreases, typically to 500 µA. The same occurs if pin 3 is open. The sink transistors are turned on when $V_{I3} \geq 2$ V.

Phase

The voltage at pin 2 determines the phase position of the output current. Output Q1 acts as sink for $V_{I2} \leq 0.8$ V and as source for $V_{I2} \geq 2$ V.

Similarly output Q2 acts as
sink when $V_{I2} \geq 2$ V and
source when $V_{I2} \leq 0.8$ V

The sink transistors are current-chopped. An internal circuit avoids undesired cross-over currents at phase change.

Nominal current input

The peak current in the motor winding is determined by the voltage at pin 8. A comparator compares this with the voltage drop at the actual current sensor at pin 4. If the nominal current is exceeded, the output sink transistors are turned off by a logic circuit.

Sync input/RC

Outputs are turned on by a signal at pin 7. Two operation modes are possible: Synchronizing by a fed-in TTL signal or free running with the external *RC* combination.

Free-running operation

When the supply voltage is applied, capacitor C_7 at pin 7 charges to a limiting voltage, typically 2.4 V. With increasing current in the motor winding, the voltage rises at the actual current sensor R_4 (pin 4). After exceeding the predetermined value at the nominal current input (pin 8) the comparator, in conjunction with pulse suppression, resets an RS flip-flop. The logic turns off sink transistors T3 and T4. C_7 ceases charging and the parallel resistance R_7 then discharges C_7. The sink transistors remain turned off until the lower threshold voltage of the Schmitt trigger is reached. This off period is thus controlled by the time constant $t_s = R_7 \times C_7$. After the lower trigger threshold has been passed, the monoflop is triggered by the falling edge of the Schmitt trigger output and, provided the voltage at the actual current sensor (pin 4) is lower than the nominal value at pin 8, the RS flip-flop is reset. The logic circuit then turns on the sink transistor T3 or T4 and recharges capacitor C_7. If the voltage at pin 4 rises above the comparator value at pin 8, the sink transistors T3 and T4 are turned off again. Turn-on cannot be repeated until capacitor C_7 has discharged to the lower trigger threshold, the discharge time being a function of R_7 and C_7.

Synchronous operation

If a TTL level sync signal is fed to pin 7, the negative edge sets the RS flip-flop, via the Schmitt trigger/monoflop combination, provided that the voltage at pin 4 is below the nominal value at pin 8. As in the free-running operation mode, the relevant output transistors become conducting. Similarly they are cut off by resetting the RS flip-flop once the voltage at pin 4 is higher than the nominal value at pin 8.

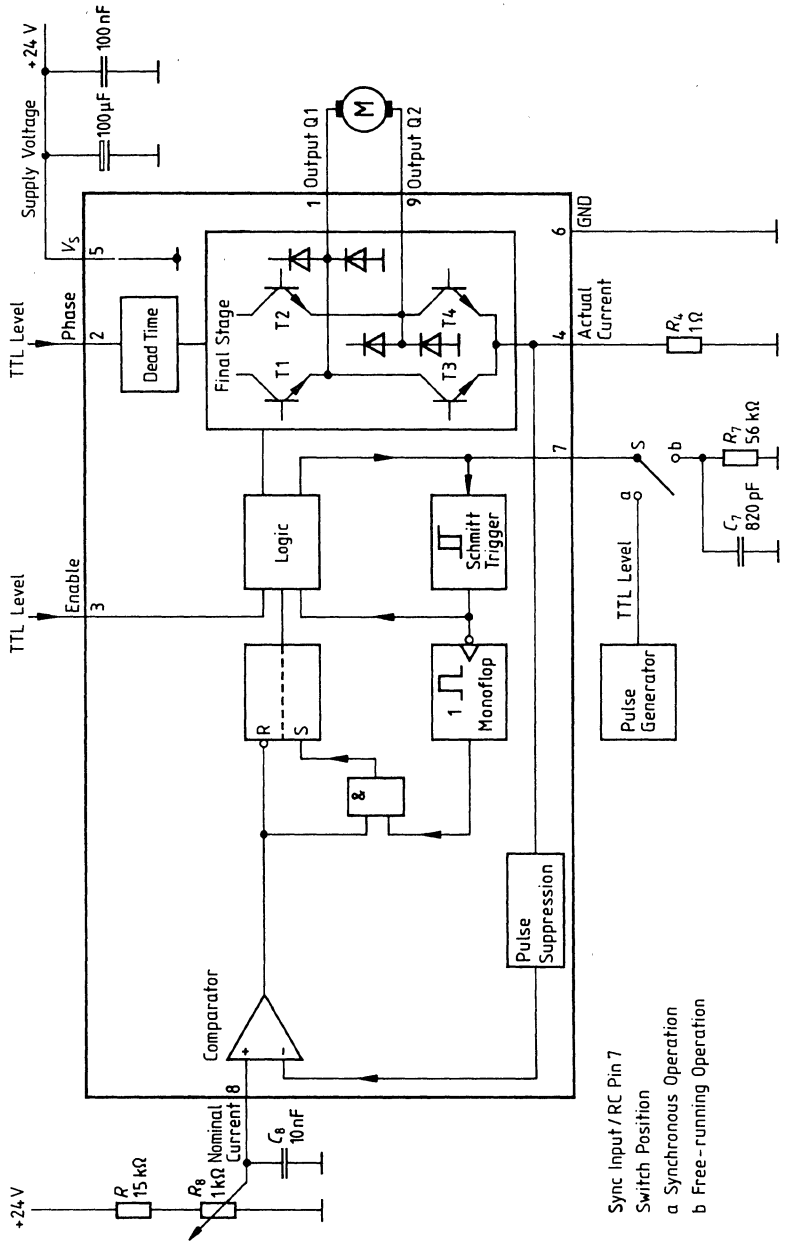
Pulse suppression

In all cases the pulse suppression circuit eliminates positive pulses, typically of 0.5 µs duration, at pin 4. These can result from cross-over currents in chopper operation through the integrated clamp diodes. As a result, the voltage at pin 4 rises well above the nominal value, and without pulse suppression this would lead to dynamic current limiting. The duration of these basically unavoidable cross-over currents is of the same order of magnitude as the reverse-recovery time of the clamp diodes.

Temperature safeguard

If the temperature of the IC rises to unacceptably high levels, the final stages are turned off.

Block diagram



Logic table

Enable		L	L	H	H
Phase		L	H	L	H
Output	Q1	/	/	L	H
Output	Q2	/	/	H	L
Transistor	T1	X	X	X	·
Transistor	T2	X	X	·	X
Transistor	T3	X	X	··	X
Transistor	T4	X	X	X	··

with:
$V_4 > 10$ mV
$R_4 > 0\ \Omega$

L = low voltage level, input open
H = high voltage level
X = transistor turned off
· = transistor conducting
·· = transistor conducting with current limiting turned on
/ = output high ohmic

Pulse diagram 1

Phase dead time

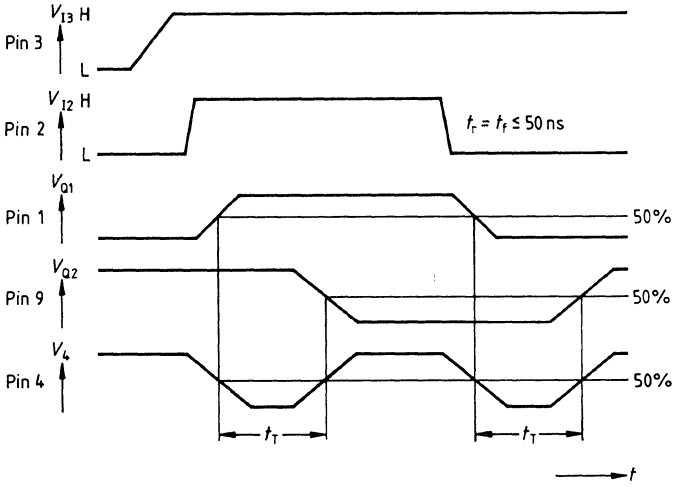


Figure 1

Pulse diagram 2

Trigger threshold

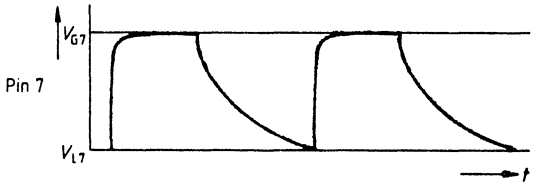


Figure 2

Turn-off delay

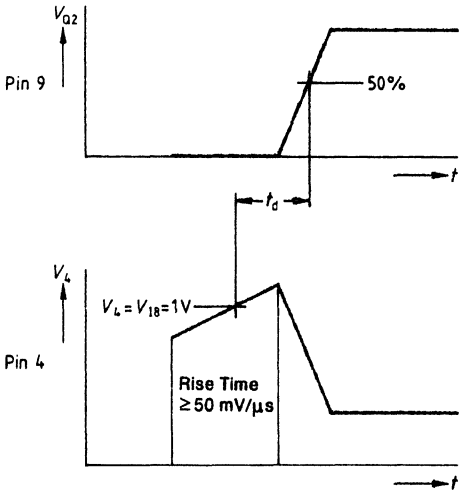


Figure 3

Off period $t_s = f(C_7)$

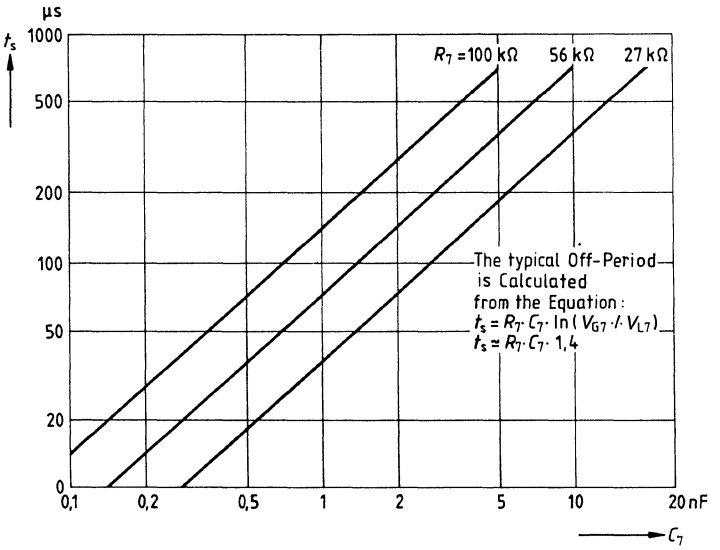


Figure 4

Control range, input offset voltage

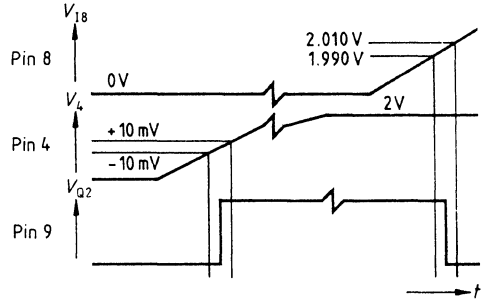
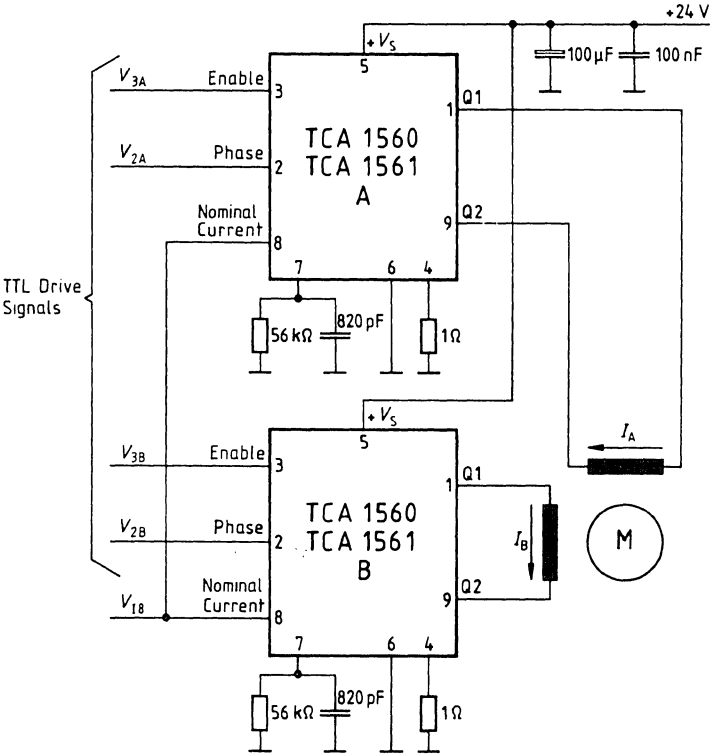
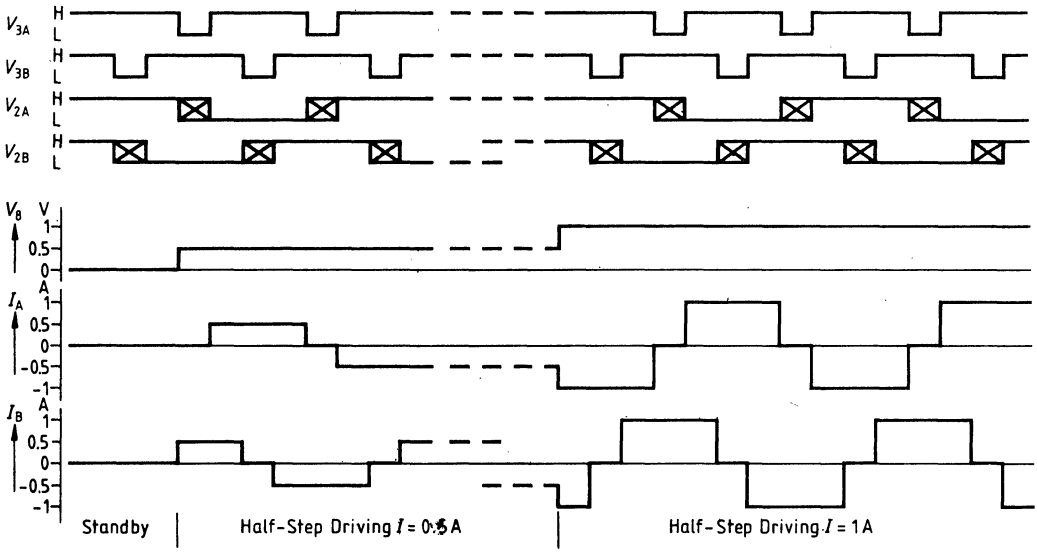


Figure 5

Application circuit



Pulse diagram for application circuit



Preliminary data

SIP 9
DIP 18

The TCA 2365 is a dual power op amp in a SIP 9 package. The IC contains two identical op amps, each supplying a high output current of 2.5 A at supply voltages between ± 4 V and ± 15 V. Both amplifiers can be disconnected simultaneously (tristate; $Z_Q \approx 4\,k\Omega$) via an inhibit input. Integrated protective circuits protect the outputs against short circuit to $+V_S$ and $-V_S$ and prevent a thermal overloading of the IC.

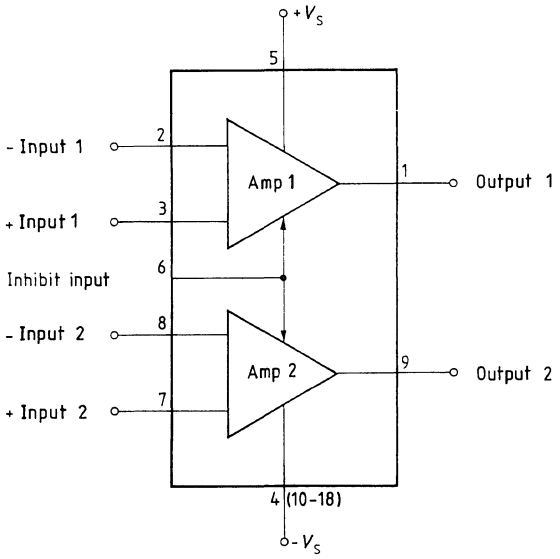
Features

- High output current of 2 times 2.5 A
- Large supply voltage range, 8 V to 32 V
- High slew rate 4 V/µs
- Outputs entirely protected (dc short-circuit proof)
- Thermal overload protection
- Inhibit input enables "tristate" outputs

Applications

- Power comparator
- Power Schmitt trigger
- Speed control of dc motors

Pin configuration TCA 2365 (TCA 2365 A)



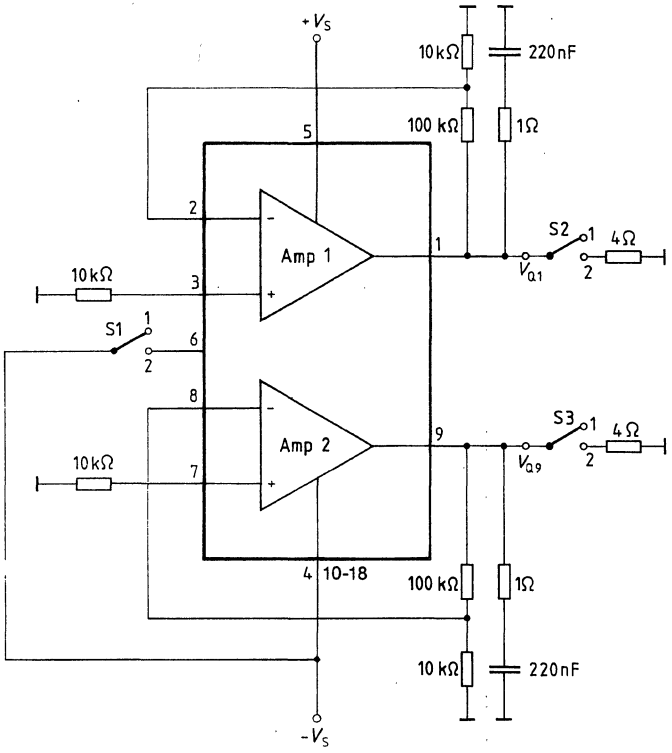
Pin 4 is electrically connected to cooling fin.
(Establish external connection between pin 4 and pin 10-18)

Maximum ratings		**TCA 2365**	**TCA 2365 A**	
Supply voltage	V_S	±16	±16	V
$t = 50$ ms	V_S	±18	±18	V
Differential input voltage	V_{ID}	$\pm V_S$	$\pm V_S$	V
Output voltage range	V_Q	$-V_S-1$ to $+V_S+1$		V
Peak output current	I_Q	±2.5	±2.5	A
Supply current	I_S	5.5	5.5	A
Junction temperature	T_j	150	150	°C
Storage temperature range	T_{stg}	−55 to 150	−55 to 150	°C
Thermal resistance				
System-air	$R_{th\ SA}$	65	60	K/W
System-case	$R_{th\ SC}$	6	10	K/W
Operating range				
Supply voltage	V_S	±4 to ±15	±4 to ±15	V
Case temperature	T_C	−25 to 85	−25 to 85	°C
($P_{tot} = 10.0$ W)				
Voltage gain	$G_{V\ min}$	10	10	dB

Characteristics $V_S = \pm 10$ V; $T_C = 25$ °C		Test circuit	min	typ	max	
Open-loop supply current consumption						
S1 in position 1	I_S	1		30	50	mA
S1 in position 2	I_{SM}	1		5	8	mA
Input offset voltage	V_{IO}	2	−10		10	mV
Input offset current	I_{IO}	3	−100		100	nA
Input current	I_I	3		0.25	1	µA
Output voltage						
$R_L = 12\ \Omega$; $f = 1$ kHz	$V_{Q\,pp}$	4	±8.5	±9.0		V
$R_L = 4\ \Omega$; $f = 1$ kHz	$V_{Q\,pp}$	4	±8.0	±8.5		V
$R_L = 470\ \Omega$; $f = 50$ kHz	$V_{Q\,pp}$	4		±6.0		V
Input resistance ($f = 1$ kHz)	R_I	4	1	5		MΩ
Open-loop voltage gain ($f = 100$ Hz)	G_{V0}	5	70	80		dB
Common-mode input voltage range	V_{IC}	6	+7/−10	+7.5/−10.5		V
Common-mode rejection	k_{CMR}	6	70	80		dB
Supply voltage rejection	k_{SVR}	7	70	80		dB
Temperature coefficient of V_{IO} $-25\ °C \le T_C \le +85\ °C$	α_{VIO}	2		50		µV/K
Temperature coefficient of I_{IO} $-25\ °C \le T_C \le +85\ °C$	α_{II0}	3		0.4		nA/K
Slew rate of V_q for non-inverting operation*	SR	8		4		V/µs
Slew rate of V_q for inverting operation*	SR	9		4		V/µs
Disturbance voltage referred to input	V_d	1		3		µV
Inhibit input (referred to $-V_S$)						
V_6 for IC turned off	$V_{6\,off}$	1	0		1.0	V
V_6 for IC turned on	$V_{6\,on}$	1	3.0		6	V
Turn-on time $\lvert I_{1;9}\rvert > 1$ A	$t_{d\,on}$	1		2	5	µs
Turn-off time $\lvert I_{1;9}\rvert < 1$ A (referred to $V_{6\,off/on}$)	$t_{d\,off}$	1		15	30	µs
S2 and S3 in position 2						

Test circuits

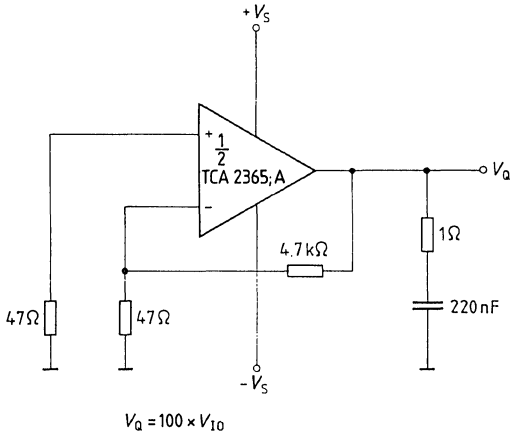
Figure 1 Open-loop supply current consumption, disturbance voltage, turn-off voltage



Switch as drawn unless otherwise specified

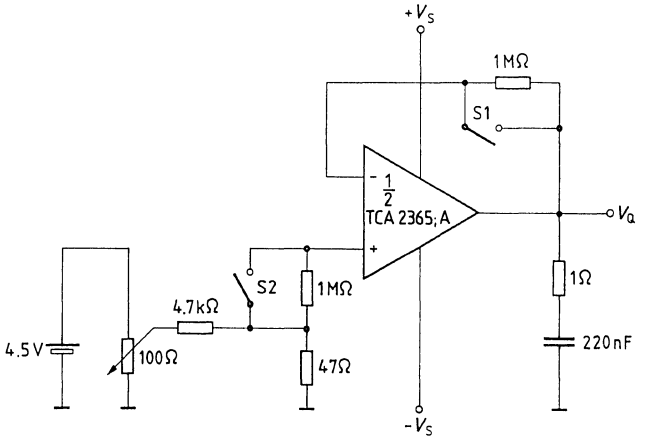
Test circuits

Figure 2 Input offset voltage, temperature coefficient of V_{IO}



$V_Q = 100 \times V_{IO}$

Figure 3 Input offset current, input current, temperature coefficient of I_{IO}



S1 open – S2 closed: $I_{I-} = \frac{V_Q}{1\ M\Omega}$

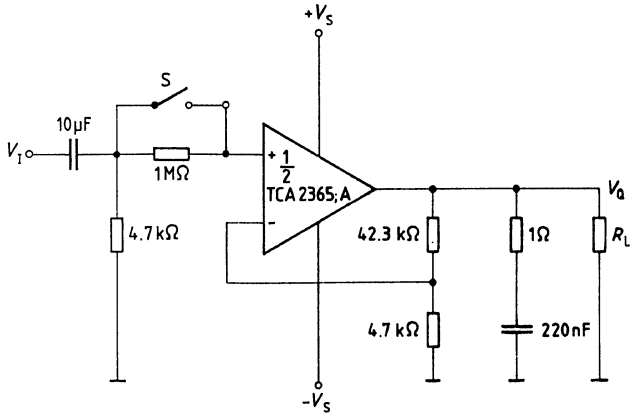
S2 open – S1 closed: $I_{I+} = \frac{V_Q}{1\ M\Omega}$

S1 open – S2 open: $I_{IO} = \frac{V_Q}{1\ M\Omega}$

S1 closed – S2 closed: offset alignment

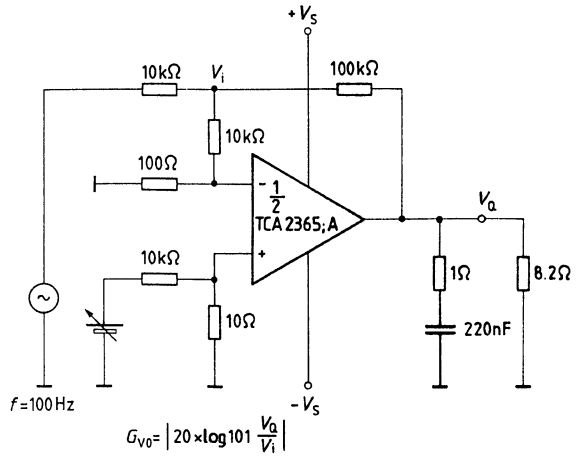
Test circuits

Figure 4 Output voltage, input resistance



S closed : to measure V_{Qpp}
S open / closed : to measure R_I

Figure 5 Open-loop voltage gain



$$G_{V0} = \left| 20 \times \log 101 \frac{V_Q}{V_i} \right|$$

Test circuits

Figure 6 Common mode voltage gain G_{VC}
Common mode rejection k_{CMR} (dB) = G_{V0} (dB) − G_{VC} (dB)

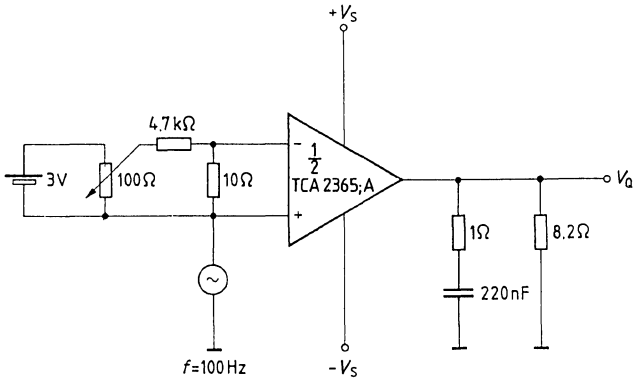
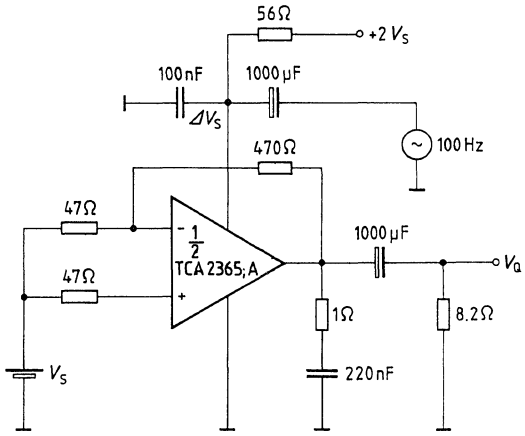


Figure 7 Supply voltage rejection



$$k_{SVR} = 20\log \frac{\Delta V_Q}{G_V \cdot \Delta V_S} \text{ [dB]}$$

Test circuits

Figure 8 Slew rate for non-inverting operation

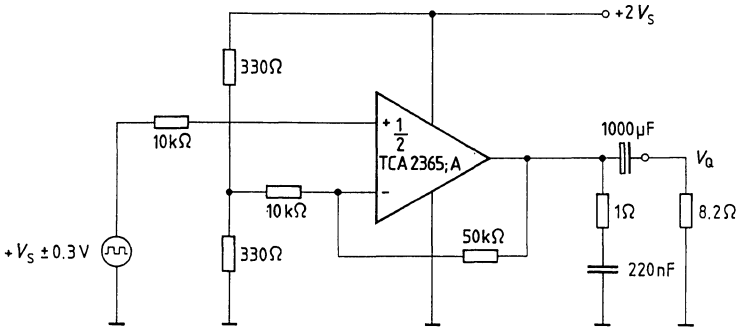
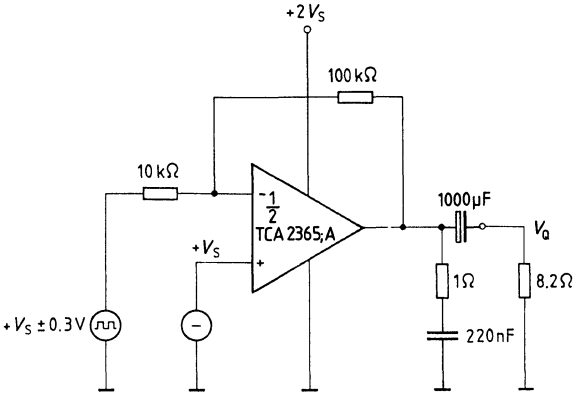
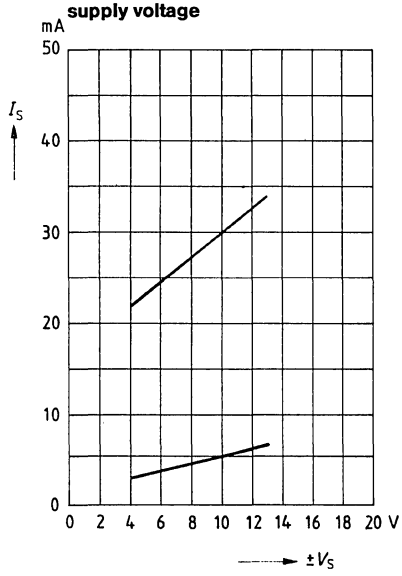


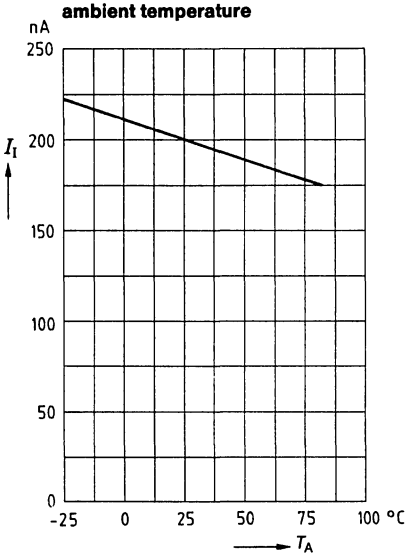
Figure 9 Slew rate for inverting operation



Supply current I_S and I_{SM} versus supply voltage

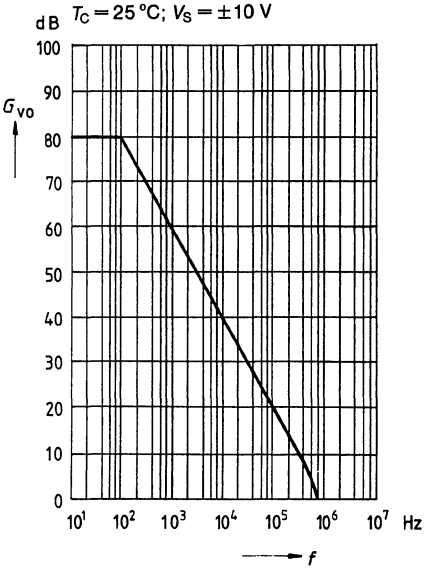


Input current versus ambient temperature



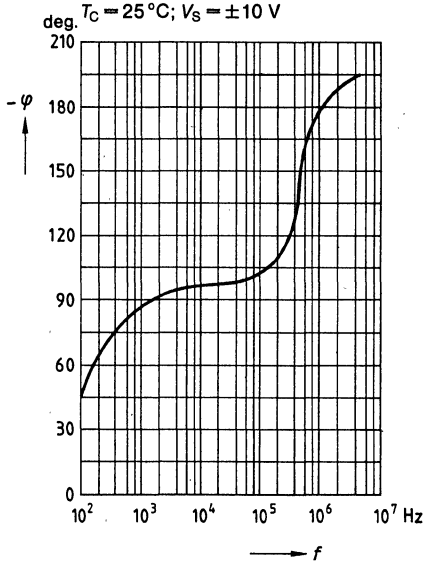
Open-loop voltage gain versus frequency

$T_C = 25$ °C; $V_S = \pm 10$ V

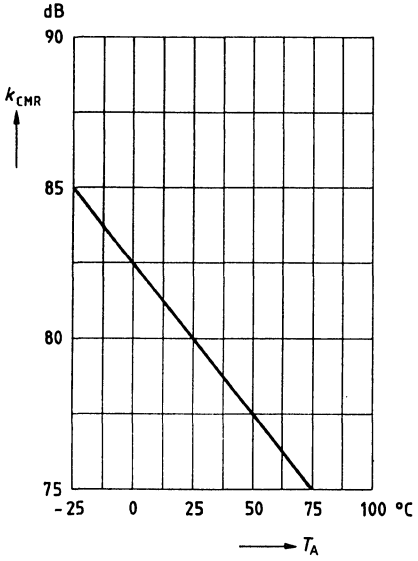


Phase response versus frequency

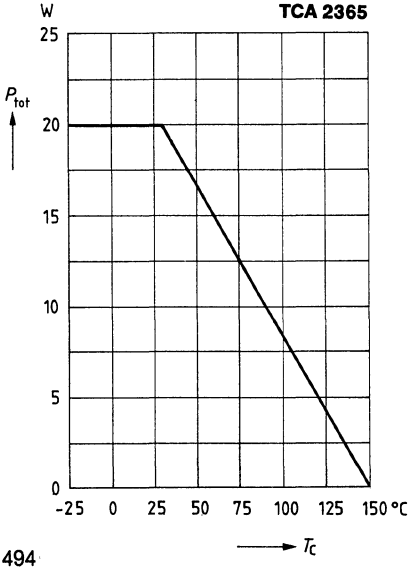
$T_C = 25\,°C$; $V_S = \pm 10\,V$



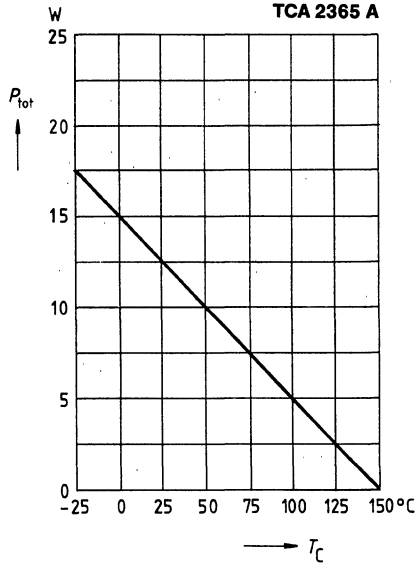
Common-mode rejection versus ambient temperature



Max. permissible power dissipation versus case temperature



Max. permissible power dissipation versus case temperature



DIP 16

The TCA 4500 A is a phase-locked loop stereo decoder which incorporates a variable channel separation control. In this IC, the sensitivity to the third harmonics of both the pilot and subcarrier frequencies has been eliminated due to the use of appropriate, digitally generated waveforms in the phase-locked loop and decoder sections.

Features

- Low distortion
- Excellent rejection of ARI subcarrier and pilot tone harmonics
- No need for coils

Maximum ratings

Supply voltage	V_S	16	V
Lamp drive voltage (lamp OFF)	V_7	30	V
Lamp current	I_7	100	mA
Channel separation control voltage	V_{11}	10	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	90	K/W

Operating range

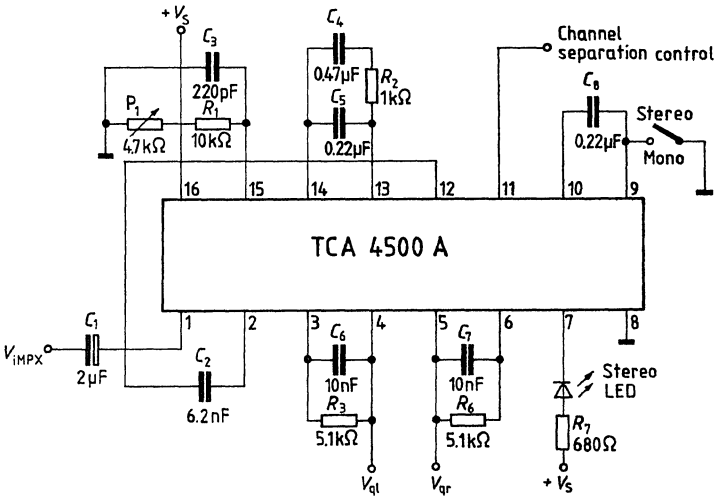
Supply voltage range	V_S	8 to 16	V
Ambient temperature range	T_{amb}	−25 to 85	°C

Characteristics

($V_S = 12$ V; $T_{amb} = 25$ °C; $V_{i(MPX)} = 2.5\ V_{pp}$; $f_{mod} = 1$ kHz; $V_{pilot} = 10\%\ V_i$)

		min	typ	max	
Current consumption ($I_7 = 0$)	I_{16}		35		mA
Stereo channel separation					
unadjusted	a	30			dB
optimized on other channel	a_{opt}	40			dB
Monaural voltage gain	G	0.8	1	1.2	
THD at 2.5 V_{pp}	*THD*			0.3	%
THD at 1.5 V_{pp}	*THD*		0.2		%
Signal-to-noise ratio in acc. with DIN 45405	$a_{S/N}$		85		dB
rms value 20 Hz – 15 kHz	$a_{S/N}$		90		dB
Frequency rejection 19 kHz	a		31		dB
38 kHz	a		50		dB
Pilot tone harmonic rejection 57 kHz ARI	a		60		dB
Subcarrier harmonic rejection 76 kHz	a		45		dB
114 kHz	a		50		dB
152 kHz	a		50		dB
Input voltage for stereo switching threshold (19 kHz input signal for lamp "ON"	$V_{i1\,rms}$	12	16	20	mV
Hysteresis for stereo switching threshold	H		6		dB
Quiescent output voltage change with mono/stereo switching	ΔV_{ql}, ΔV_{qr}		5	20	mV
Channel separation control voltage					
3 dB separation	V_{11}		0.7		V
30 dB separation	V_{11}		1.7		V
Minimum channel separation ($V_{11} = 0$ V)	a			1	dB
Monaural channel inbalance (pilot tone off)	$\Delta V_{ql,r}$			0.3	dB
Hum suppression	a_{hum}		55		dB
Input resistance	R_{i1}		50		kΩ
Output resistance	R_{q4}, R_{q5}		100		Ω
Channel separation control current	I_{11}			−300	µA
Capture range	$\Delta f/f_0$		±5		%

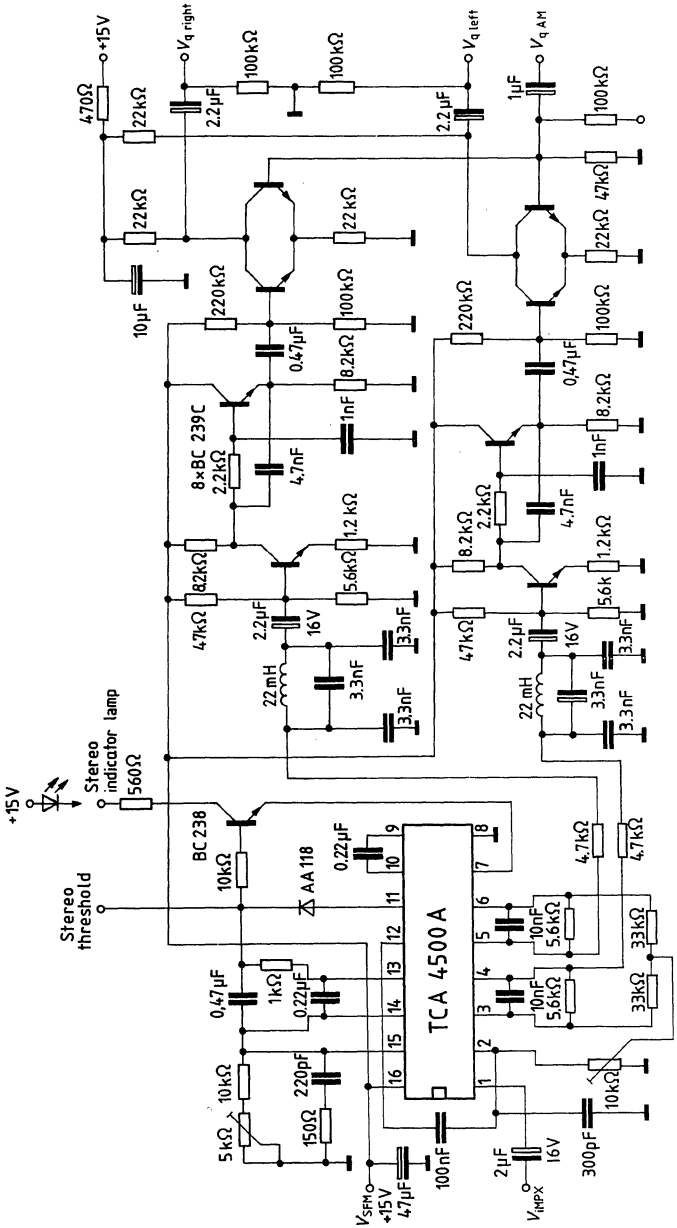
Measurement circuit



Pin configuration

Pin No.	Function
1	Input
2	Preamplifier output
3	Left amplifier input
4	Left channel output
5	Right channel output
6	Right amplifier input
7	Stereo indicator lamp
8	Ground
9	Switching threshold
10	Switching threshold
11	19 kHz output/channel separation control
12	Modulator input
13	Loop filter
14	Loop filter
15	Oscillator *RC* network
16	Supply voltage $+V_S$

Application circuit with low-pass filter



DIP 18

The TCA 4511 decodes the transmitter side stereo information in both L and R channels. Stereo transmission is shown by means of an indicator lamp. A continual blending of mono and stereo signals is possible. The switching frequencies are controlled by a phase-locked loop. The stereo decoder can be used in time multiplex (switching) or in frequency multiplex (matrix) mode of operation.

Features

- Good channel separation
- No need for coils
- Automatically adjustable bandwidth
- Good suppression of ARI subcarrier and pilot tone harmonics

Maximum ratings

Supply voltage	V_S	18	V
Lamp voltage	V_{LP}	18	V
Current for stereo indicator lamp ($V_{18} \cdot I_{LP} \leqq 300$ mW)	I_{LP}	50	mA
Minimum values at all pins	V	0	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	78	K/W
(junction-case)	$R_{th\,JC}$	45	K/W

Operating range

Supply voltage range	V_S	8 to 18	V
Ambient temperature range	T_{amb}	−25 to 85	°C

Characteristics for switch operation ($V_S = 12$ V; $T_{amb} = 25$ °C)

		min	typ	max	
Total current (FM operation) S1 closed	I_S		14	20	mA
Total current (AM operation) S1 open	I_S		10	15	mA
Lamp current adjustment range ($V_{18} \cdot I_{LP} \leqq 300$ mW)	I_{LP}	10		25	mA
Lamp current short circuit ($V_{18} \cdot I_{LP} \leqq 300$ mW)	I_{LP}			50	mA
Input amplifier					
Op amp input signal	V_{16pp}			1.6	V
Op amp output signal[1])	V_{14pp}		V_{16}		V
Input resistance	R_I	90	125		kΩ
Feedback resistance	R_F		10		kΩ
Reference voltage	V_{13}		1.75		V
Stereo matrix					
Output voltage (stereo)[1,6]) for modulated output	V_{qAFpp}	0.9	1.2	1.6	V
Output voltage (mono)[2,6]) L or R modulated	V_{qAFpp}	0.45	0.6	0.8	V
Output resistance	R_q		1.5	2	kΩ
Crosstalk attenuation[1]) ($f_{AF} = 1$ kHz)	a_{CR}	34	40		dB
Reduction 19 kHz Test circuit 1	a_{19}	30	32		dB
Reduction 38 kHz Test circuit 1	a_{38}	30	40		dB
Reduction 57 kHz Test circuit 1	a_{57}	30	45		dB
Reduction 76 kHz Test circuit 1	a_{76}	30	40		dB
Hum suppression[3])	a_{hum}	40	45		dB
Noise voltage[4])	V_{qn}		30	80	μV
Total harmonic distortion[1,6]) ($f_{AF} = 1$ kHz)	THD			0.5	%
Channel balance[2])	B			0.5	dB
Switching noise mono/stereo S1 closed/open	$\Delta V_9, \Delta V_{10}$			60	mV
Oscillator					
Output resistance for f_{OSC} measurement	R_8		200		kΩ
Oscillator basic frequency	f_{OSC}		19		kHz
Capture and hold range[1])	$f_{C/H}$	±0.4	±1	±2.0	kHz
Balancing resistance ($f_{OSC} = 19$ kHz)	R_{OSC}	13		18	kΩ
Function of the oscillator S1 closed	V_{18}	1.0			V
Switch off of the oscillator[8]) S1 open	V_{18}			0.4	V
Function of the oscillator ($I_{18} = 10$ mA)	V_{18}	0.9			V

Characteristics for switch operation ($V_S = 12$ V; $T_{amb} = 25$ °C) (cont'd)

		min	typ	max	
Phase comparisons					
Input voltage[1])	V_{5pp}	0.5	0.7	0.9	V
Input resistance	R_5		3.3		kΩ
Input voltage	V_{5pp}			1.6	V
Stereo switch					
Threshold stereo ON[5]) ($f = 19$ kHz)	V_{iPTpp}		30	55	mV
Threshold stereo OFF[5]) ($f = 19$ kHz)	V_{iPTpp}	12	15		mV
Hysteresis	H_y	3	6	9	dB
Mono/stereo blending					
Mono ($V_H = V_8 = 0.5$ V)[7])	a_{bl}	3	6	9	dB
Stereo ($V_H = V_8 = 0.9$ V)[7])	a_{bl}	34			dB

[1]) $V_{ipp} = 1.2$ V MPX; $V_H \geqq 1$ V; S1 closed; $f_{AF} = 1$ kHz
[2]) $V_{ipp} = 1.2$ V MPX; S1 open; $f_{AF} = 1$ kHz
[3]) $V_S = 12$ V + V_n; $V_{nrms} = 200$ mV; 200 Hz
[4]) CCIR DIN 45405; unweighted; S1 open
[5]) S1 closed
[6]) After TP with $f_{co} = 6.5$ kHz; reduction 36 dB/octave
[7]) $V_{16pp} = 0.75$ V MPX; S1 closed; $f_{AF} = 1$ kHz
[8]) The oscillator is switched off, if pin 18 is connected with a voltage ≦ 0.4 V or S1 is open.

Circuit description (switching operation)

The MPX input signal is corrected in amplitude and phase by an operational amplifier. For this purpose an *RC* circuit is connected at pin 15.

Subsequently, the (L+R) and (L−R) signals are processed in separate stages. The (L−R) signal is demodulated and can be reduced by the factor a through mono/stereo blending. In the final matrix circuit the aggregate signal (L+R) is added to the demodulated signal a (L−R) according to the following formulae:

$$(L+R) + a\,(L-R) = L(1+a) + R(1-a)$$
$$(L+R) - a\,(L-R) = L(1-a) + R(1+a)$$

$$\underset{\text{Mono}}{0} \leq \underset{\text{Blending}}{a} \leq \underset{\text{Stereo}}{1}$$

The generated output signals are then forwarded to two external *RC* low-passes for deemphasis.

The required frequency to demodulate the L−R signal is obtained by a phase-locked loop (PLL) from the divider. By means of a pilot tone applied to pin 5, the oscillator is synchronized by phase comparison 1. An additional phase comparison 2 provides mono or stereo information. Based on this information, the indicator lamp is activated and lights up when a sufficiently strong signal is present at the input. Moreover, the (L−R) reduction is eliminated.

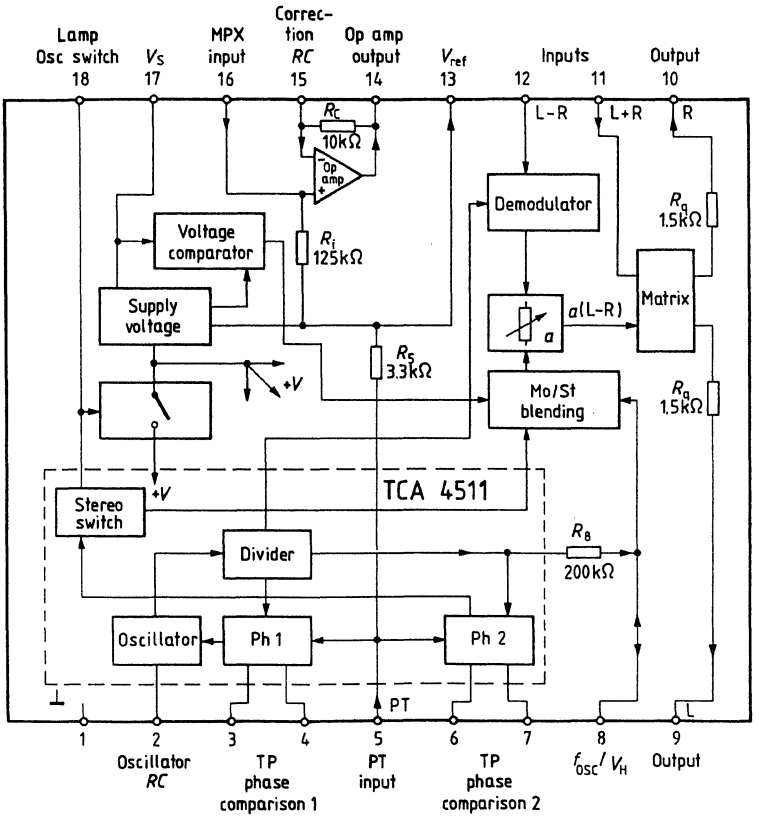
If switch S1 is open, the IC switches the oscillator off, whereby the stereo switch and the mono/stereo blending suppress the L−R signal. The supply current is thus reduced. Also, since the oscillator does not resonate when switch S1 is open, AM receiver signals can be forwarded without interference via the IC.

If pin 8 is not connected, the oscillator frequency can be measured. For normal operating functions, the blending voltage V_H is applied to pin 8 or pin 8 must be blocked by a capacitor. Otherwise, cross-talk is affected by the oscillator frequency.

Pin configuration

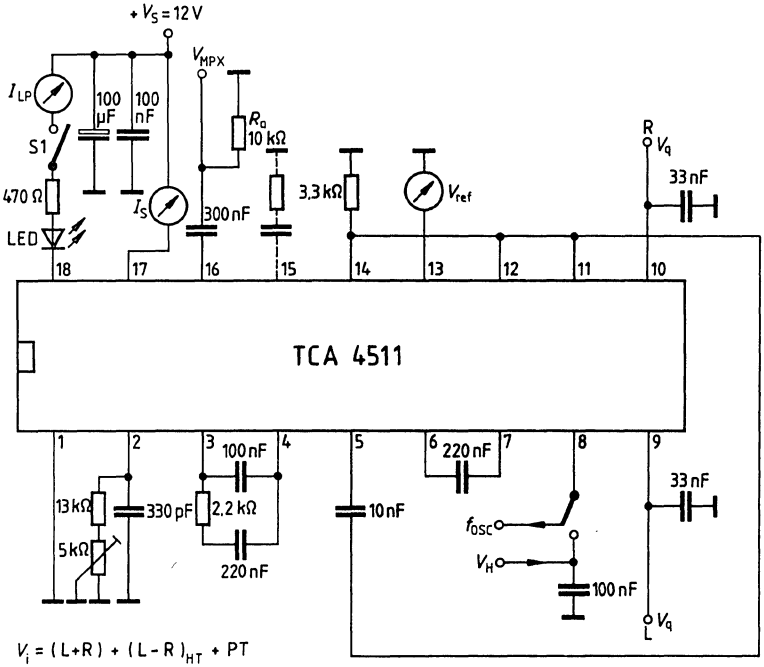
Pin No.	Function
1	Ground
2	Oscillator *RC*
3	TP phase comparison 1
4	TP phase comparison 1
5	Pilot tone (PT) input
6	TP phase comparison 2
7	TP phase comparison 2
8	f_{OSC} output/St-Mo blending V_H
9	Output L
10	Output R
11	(L+R) input
12	(L−R) input
13	Reference voltage
14	Output op amp
15	− input op amp
16	+ input op amp
17	Supply voltage
18	Lamp connection/oscillator switch

Block diagram



Test circuit

Switching operation

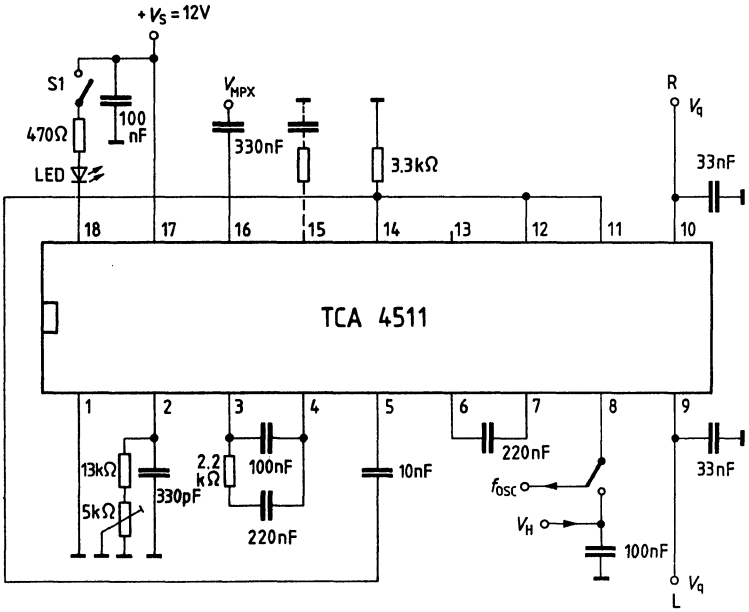


$V_i = (L+R) + (L-R)_{HT} + PT$
L = 100 % ; R = 0 % or
R = 100 % ; L = 0 %

S1 open = AM
S1 closed = FM

Application circuit

Switching operation



S1 open = AM
S1 closed = FM

SIP 9

AF power amplifier designed for a wide range of supply voltages to enable versatile application in entertainment electronics. The amplifier operates in the push-pull B mode and is available in the SIP 9 package. The integrated shutdown protects the IC from overheating.

Features

- Wide supply voltage range: 4 V to 28 V
- High output power up to 8 W
- Large output current up to 2.5 A
- Simple mounting

Maximum ratings

Supply voltage $R_L \geq 16\ \Omega$	V_S	30	V
$R_L \geq 8\ \Omega$	V_S	24	V
$R_L \geq 4\ \Omega$	V_S	20	V
Output peak current (not repetitive)	I_q	3.5	A
Output current (repetitive)	I_q	2.5	A
Junction temperature[1])	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance			
junction-case	R_{thJC}	12	K/W
system-air	R_{thSA}	70	K/W

Operating range

Supply voltage	V_S	4 to 28	V
Ambient temperature	T_A	−25 to 85	°C

*) May not be exceeded even as instantaneous value.

Characteristics

with reference to test circuit

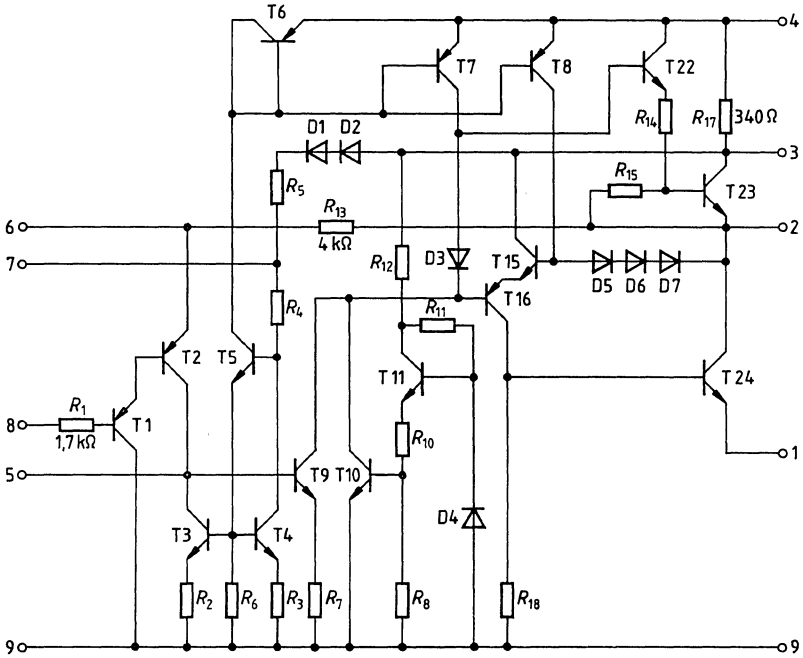
1. $V_S = 12$ V; $R_L = 4\ \Omega$; $C_1 = 1000\ \mu$F; $f_i = 1$ kHz; $T_A = 25\,^\circ$C

		min	typ	max	
Quiescent output voltage	V_{q2}	5.4	6.0	6.6	V
Quiescent drain current	$I_3 + I_4$		12	20	mA
Input DC current	I_{i8}		0.4	4	μA
Output power $THD = 1\%$	P_q	2.5	3.5		W
$THD = 10\%$	P_q	3.5	4.5		W
Voltage gain (closed loop)	G_V	37	40	43	dB
Voltage gain (open loop)	G_{V0}		80		dB
Total harmonic distortion ($P_q = 0.05$ to 2.5 W)	THD		0.2		%
Noise voltage referred to input ($f_i = 3$ Hz to 20 kHz)	V_n		3.8	10	μV_S
Disturbance voltage in acc. with DIN 45405 referred to input	V_d		2.5		μV
Hum suppression ($f_{hum} = 100$ Hz)	a_{hum}		48		dB
Frequency range (–3 dB)					
$C_4 = 560$ pF	f	40		20,000	Hz
$C_4 = 1000$ pF	f	40		10,000	Hz
Input resistance	R_{i8}	1	5		MΩ

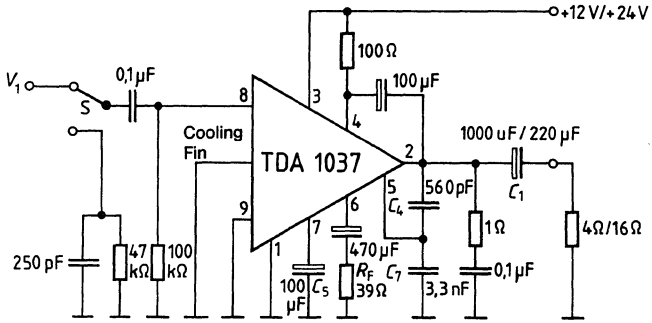
2. $V_S = 24$ V; $R_L = 16\ \Omega$; $C_1 = 220\ \mu$F; $f_i = 1$ kHz; $T_A = 25\,^\circ$C

Quiescent output voltage	V_{q2}	11	12	13	V
Quiescent drain current	$I_3 + I_4$		18	30	mA
Input DC current	I_{i8}		0.8	8	μA
Output power $THD = 1\%$	P_q		3.5		W
$THD = 10\%$	P_q	4.5	5.0		W
Voltage gain (closed loop)	G_V	37	40	43	dB
Voltage gain (open loop)	G_{V0}		80		dB
Total harmonic distortion ($P_q = 0.05$ to 3 W)	THD		0.2	0.5	%
Noise voltage with reference to input $f_i = 3$ Hz to 20 kHz	V_n		5	15	μV_S
Disturbance voltage in acc. with DIN 45405 referred to input	V_d		3.8		μV
Hum suppression ($f_{hum} = 100$ Hz)	a_{hum}		40		dB
Frequency range (–3 dB)					
$C_4 = 560$ pF	f	40		20,000	Hz
$C_4 = 1000$ pF	f	40		10,000	Hz
Input resistance	R_{i8}	1	5		MΩ

Circuit diagram

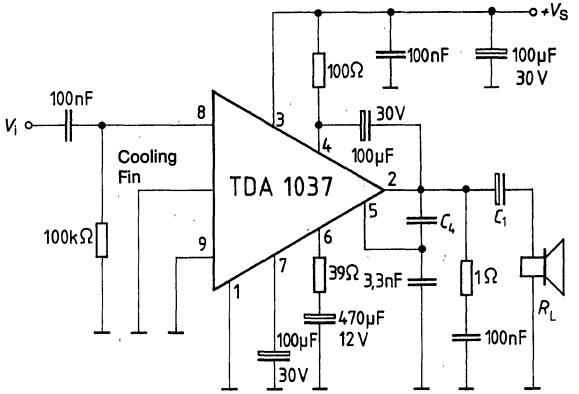


Measurement circuit



S Closed for Noise Measurement

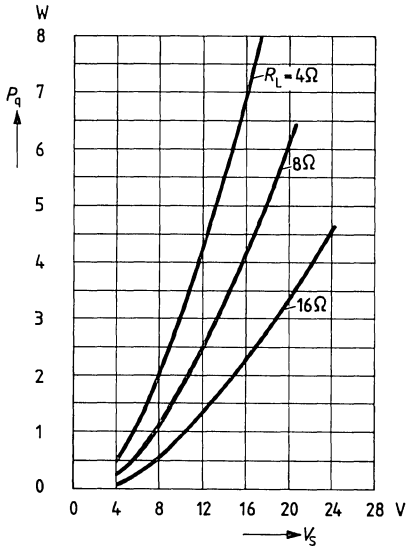
Application circuit



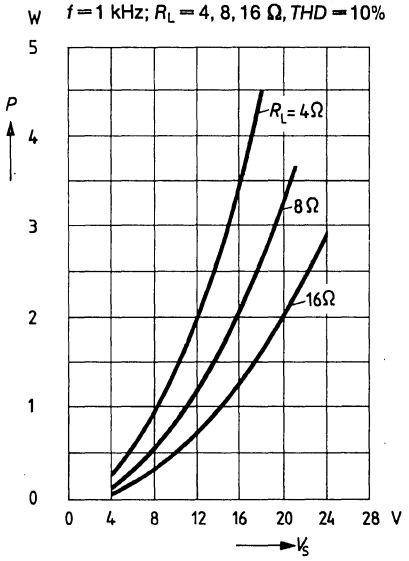
V_S	12 V	18 V	24 V
R_L	4 Ω	8 Ω	16 Ω
C_1	1000 µF	470 µF	220 µF

f_{max}	10 kHz	20 kHz
C_4	1000 pF	560 pF

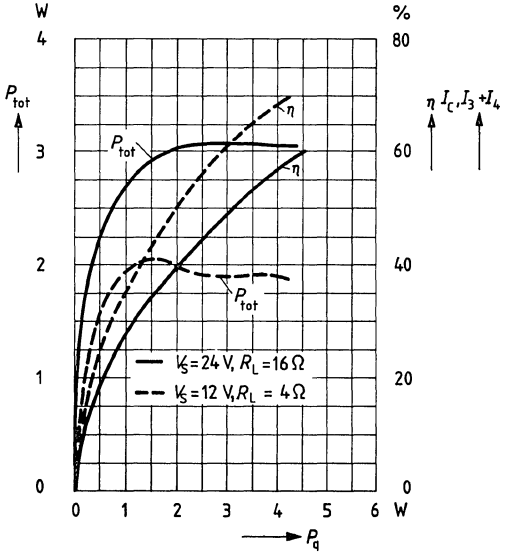
Output power versus supply voltage
THD = 10%; R_L = 4, 8, 16 Ω; *f* = 1 kHz



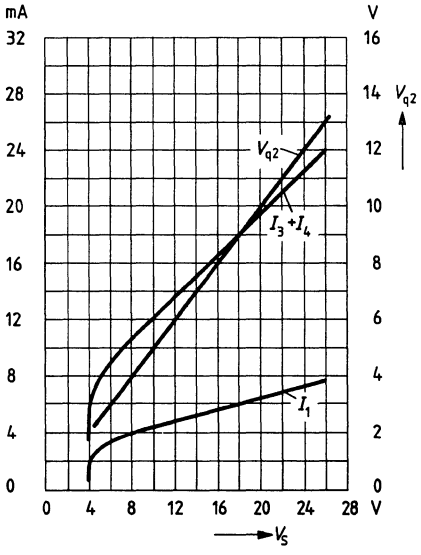
Max. power dissipation versus supply voltage at sine-shaped driving
f = 1 kHz; R_L = 4, 8, 16 Ω, *THD* = 10%



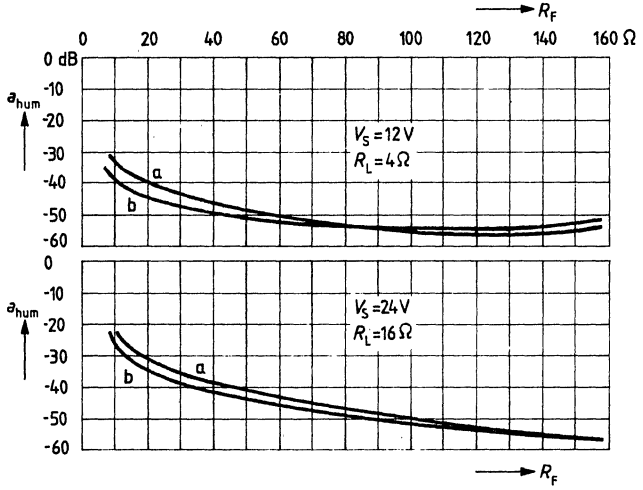
Total power dissipation and efficiency versus output power
THD = 10%; *f* = 1 kHz



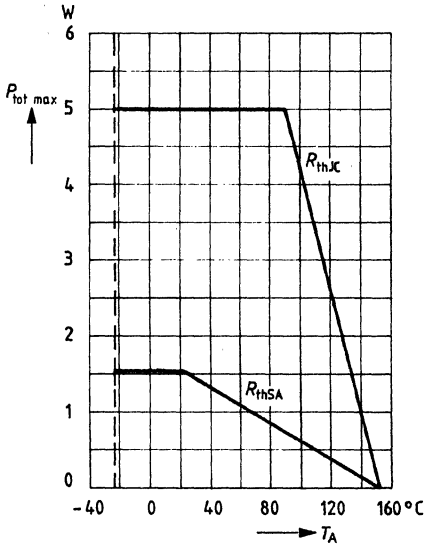
Quiescent drain current, quiescent current of output transistors, quiescent output voltage versus supply voltage



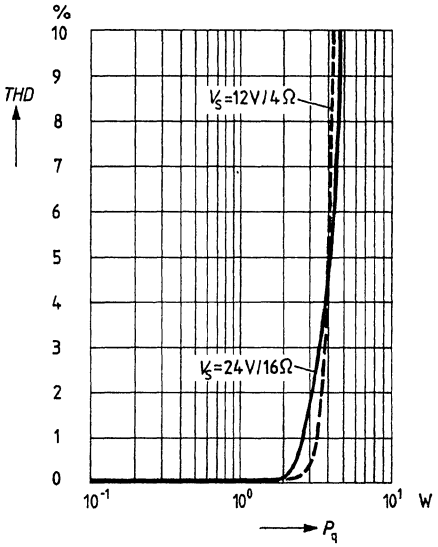
Hum suppression versus feedback resistance
f_{hum} = 100 Hz; C_5 = 100 µF
a: input short-circuited
b: input open



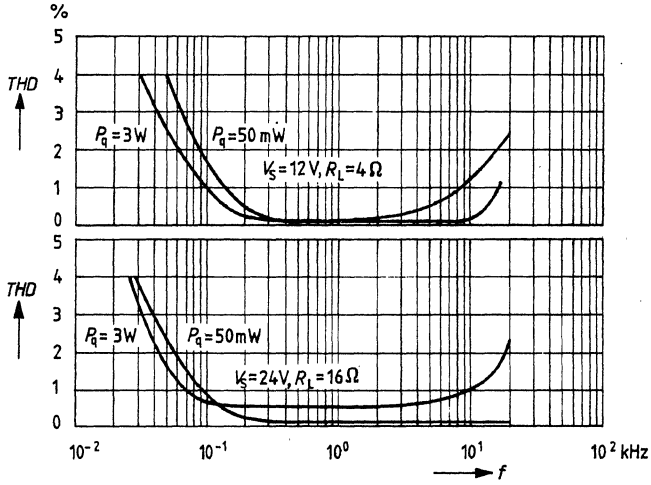
Max. total power dissipation versus ambient temperature



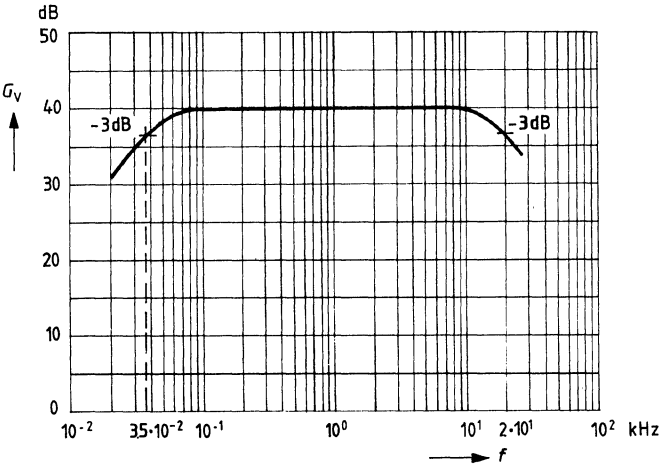
Total harmonic distortion versus output power
$f = 1$ kHz



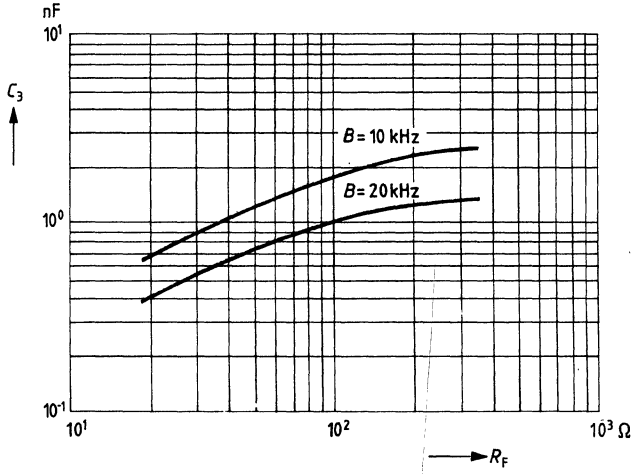
Total harmonic distortion versus frequency



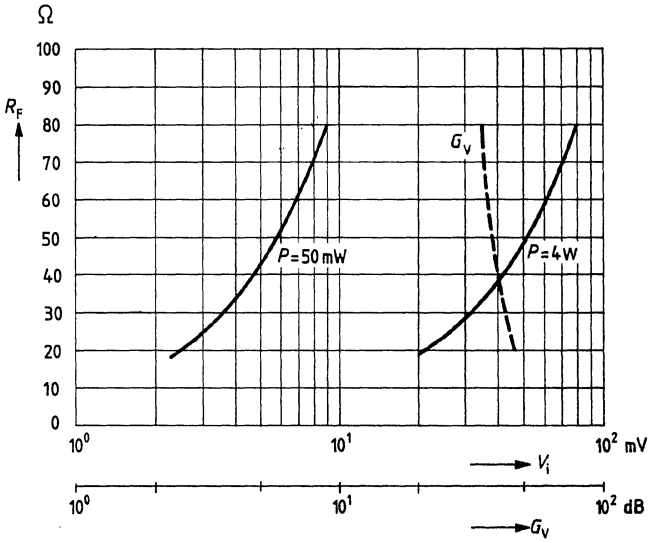
Voltage gain versus frequency
$V_S = 12$ V; $R_L = 4\ \Omega$



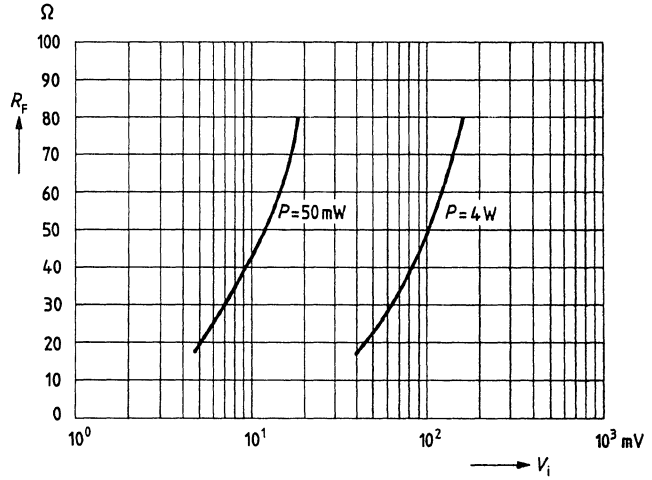
Bandwidth C_3 versus feedback resistance
$V_S = 12$ V; $R_L = 4\ \Omega$, $G_V = 40$ dB
$C_1 = 5 \cdot C_4$



Output power and voltage gain versus feedback resistance and input voltage
$V_S = 12$ V; $R_L = 4\ \Omega$; $f = 1$ kHz



Output power versus feedback resistance and input voltage
$V_S = 24$ V; $R_L = 16\ \Omega$; $f = 1$ kHz



DIP 18

The TDA 4001 has been designed to convert, amplify, and demodulate AM signals. In addition, the component provides a search tuning stop pulse.

Features

- Internal demodulation
- Search tuning stop signal
- Low total harmonic distortion
- Minimal IF leakage at the AF output
- 2-stage integrated low pass filter

Maximum ratings

Supply voltage	V_S	15	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	70	K/W

Operating range

Supply voltage	V_S	7 to 15	V
Ambient temperature	T_A	−25 to 85	°C

Characteristics

$V_S = 12$ V; $T_A = 25$ °C; $V_{iRF\,rms} = 1$ mV; $R_g = 50$ V; $f_{iRF} = 1$ MHz; referred to measurement circuit

		min	typ	max	
Current consumption	I_S		15		mA
AF output voltage $m = 0.8\,\%$	V_{qAFrms}		800		mV
$m = 0.3\,\%$	V_{qAFrms}		300		mV
$V_{iRFrms} = 15\ \mu V$; $m = 0.8\,\%$	V_{qAFrms}	150		320	mV
$20 \lg \left(\frac{V_1}{V_2}\right)$ $V_1 = V_{qAF}$ at 30 mV				3	dB
$V_2 = V_{qAF}$ at 1 mV					
Total harmonic distortion $m = 0.8\,\%$	THD			2	%
$m = 0.3\,\%$	THD			1	%
$V_{iRFrms} = 30$ mV; $m = 0.8\,\%$	THD			5	%
Signal-to-noise ratio					
$m = 0.3$; $V_{iRFrms} = 10\ \mu V$	$\frac{S+N}{N}$		6		dB
$m = 0.3$; $V_{iRFrms} = 1$ mV	$\frac{S+N}{N}$		46		dB
Reference voltage	V_{stab}		4.8		V
Oscillator voltage	$V_{OSC\,pp}$		100		mV
Counter output voltage	$V_{qC\,pp}$		100		mV
Input impedance RF input	Z_{iRF}		10/1.5		kΩ/pF
IF amplifier	Z_{iIF}		3.3/1.5		kΩ/pF
AFC offset current without signal	I_{AFC}			±10	µA
AFC offset current in the whole control range	ΔI_{AFC}			±10	µA
AFC output current	I_{AFC}		±80		µA
$f_{iRF} = 1$ MHz ± 3 kHz					
Search tuning stop output current	I_{q13}		2		mA
Search tuning stop output voltage	V_{q13}			0.4	V
Search tuning stop output voltage					
$V_{iRF} = 0$ V	V_{q13}	11			V
$f_{iRF} > 1$ MHz + 3 kHz	V_{q13}	11			V
$f_{iRF} < 1$ MHz − 3 kHz	V_{q13}	11			V

Additional data with respect to application[1])

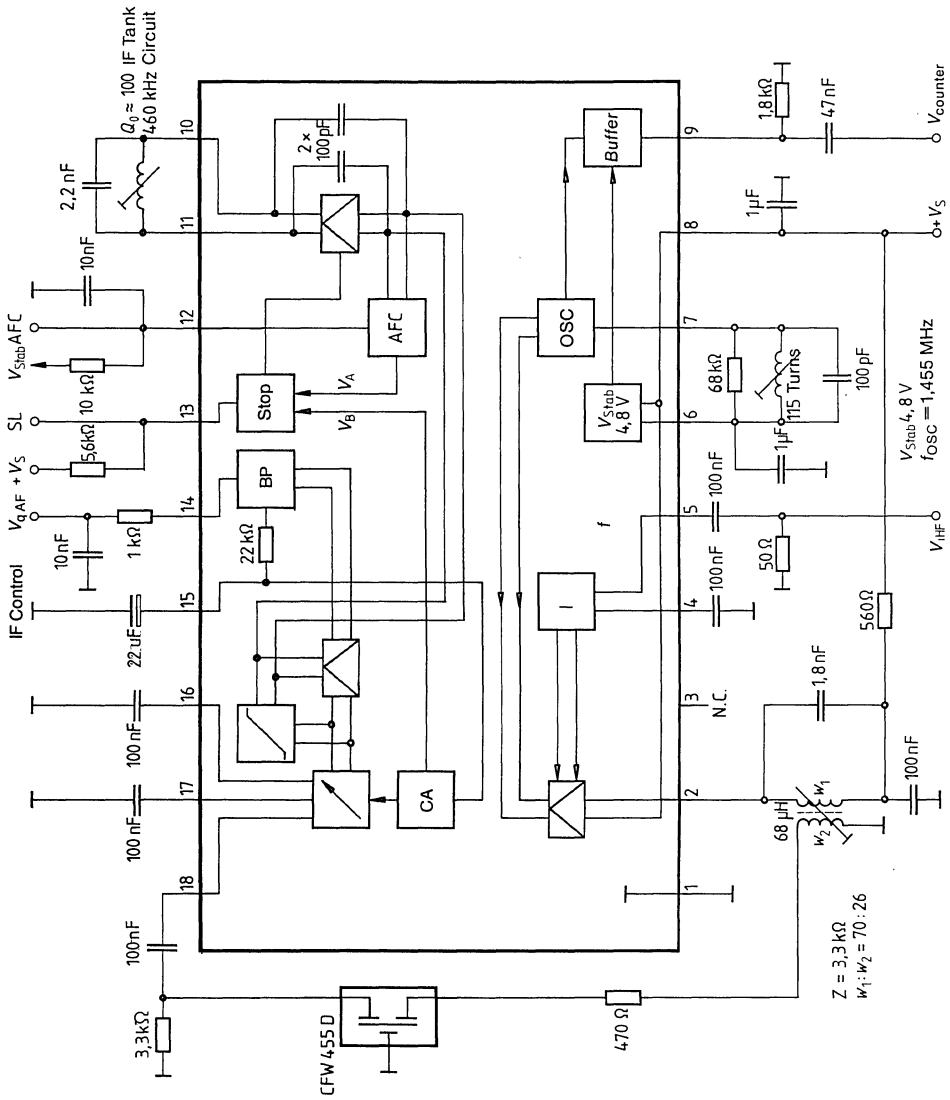
IF suppression	a_{IF}		40		dB
3 dB limit frequency of the integrated TP	f_G		5		kHz
Conversion gain	G_C		30		dB
AGC IF amplifier	V_{iIFrms}		100		µV
Control range ($\Delta V_{qAF} = 6$ dB)	a		60		dB
Input sensitivity	V_{iRFrms}		30		µV
V_{qAF} at $V_{iRF} \geq 0\,7$; V_{qAF} at $V_{iRF} = 1$ mV					

Circuit description

The impedance converter forwards the input signal V_{iRF} to the symmetrical double balanced mixer. Subsequently the signal is converted to IF with the amplitude-controlled oscillator. An external filter forwards the IF signal to the controlled IF amplifier. The amplifier IF signal and the carrier signal will be converted to AF in the subsequent synchronous demodulator (SD). The 2-stage low pass filter forwards the available AF to the AF output. Via an additional limiter amplifier (LA), the AF uses the carrier signal to control the coincidence demodulator (CD). The output signal of the coincidence demodulator provides the stop pulse during exact tuning and sufficient field strength.

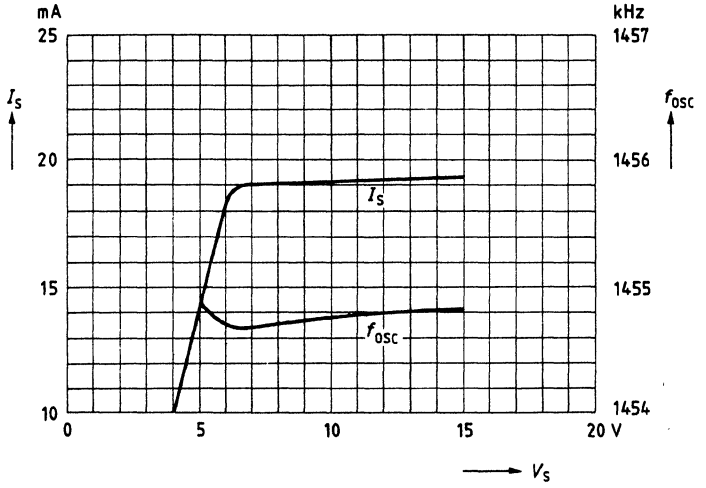
1) Data does not apply to series measurement processes.

Block diagram and measurement circuit



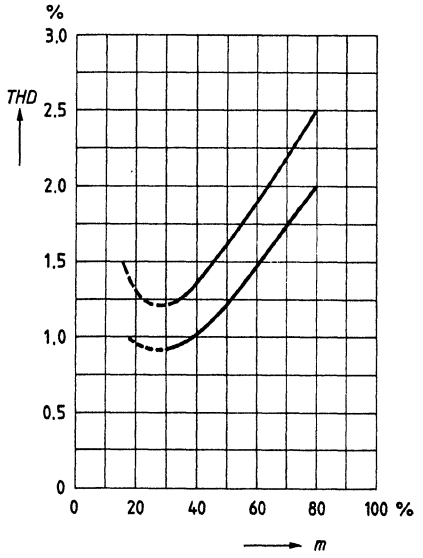
CA = Control Amplifier
BP = Band Pass
I = Impedance Converter

Oscillator frequency versus current consumption

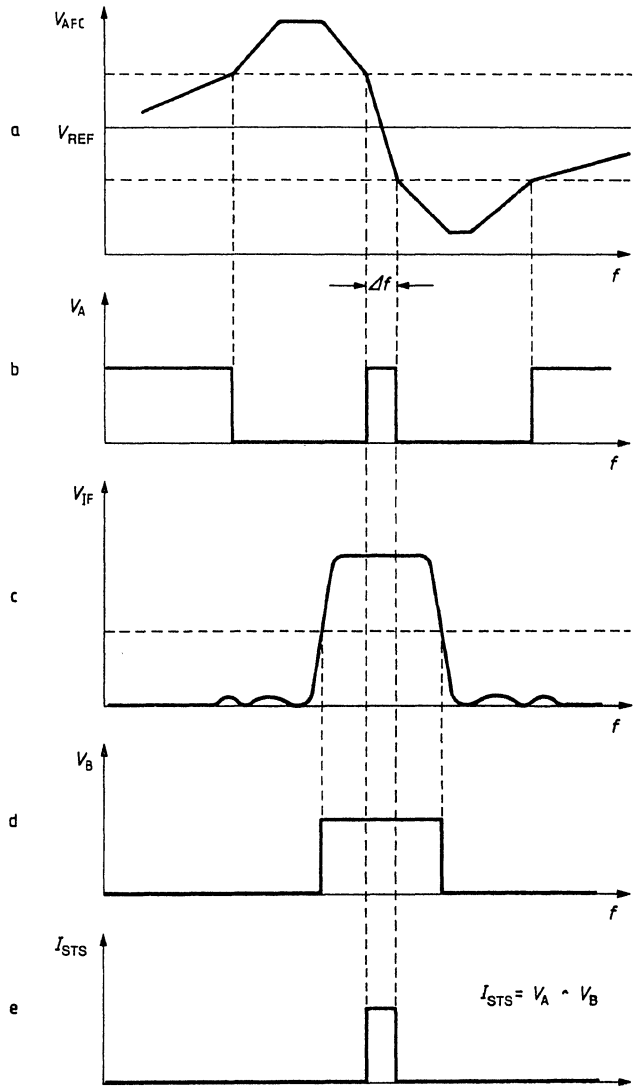


Total harmonic distortion versus modulation factor

V_S = 15 V; f_{mod} = 1 kHz; V_I = 1 mV



Derivation of the AM-SL stop criterion



S Curve Simulation
(Pin 12)

--- Comparator Threshold A

Δf = Stop Bandwidth

V_A = Output Voltage, Window Discriminator A

IF Selection
(e.g. CFW 455)

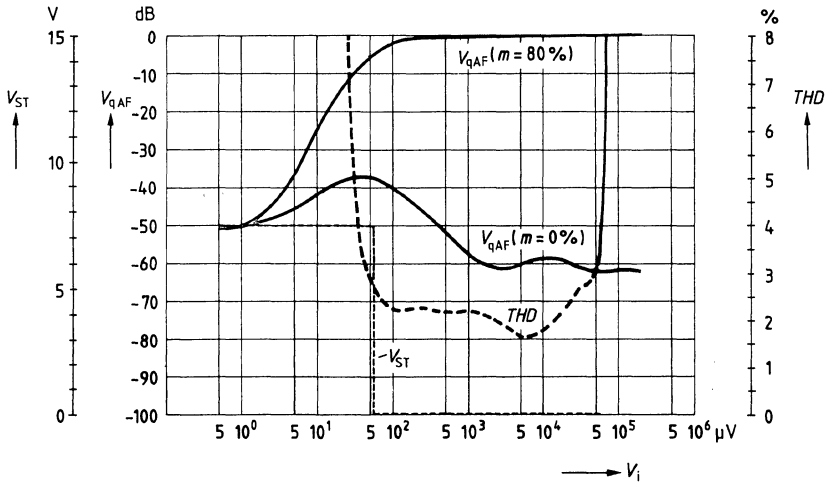
--- Comparator Threshold B

V_B = Output Voltage, Window Discriminator B

Search Tuning Stop Pulse
(Pin 13)

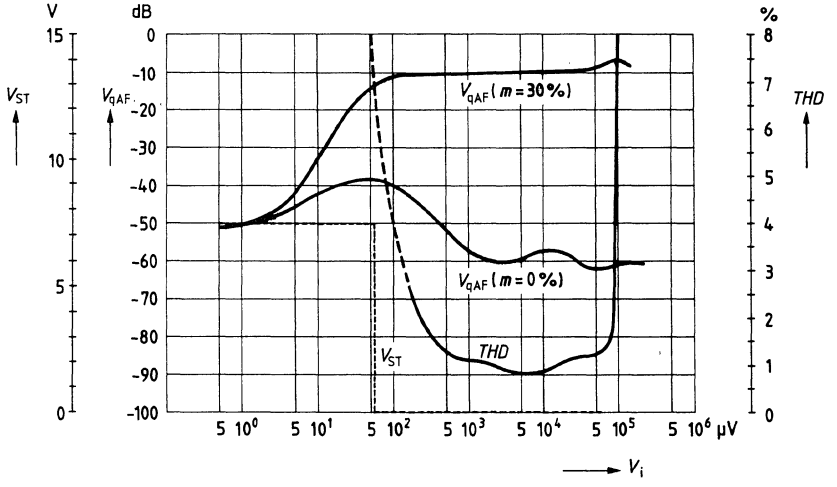
AF output voltage, total harmonic distortion, search tuning stop versus input voltage
$V_S = 15$ V, $f_{mod} = 1$ kHz, $f_i = 1$ MHz

0dB ≙ 775mV (rms)

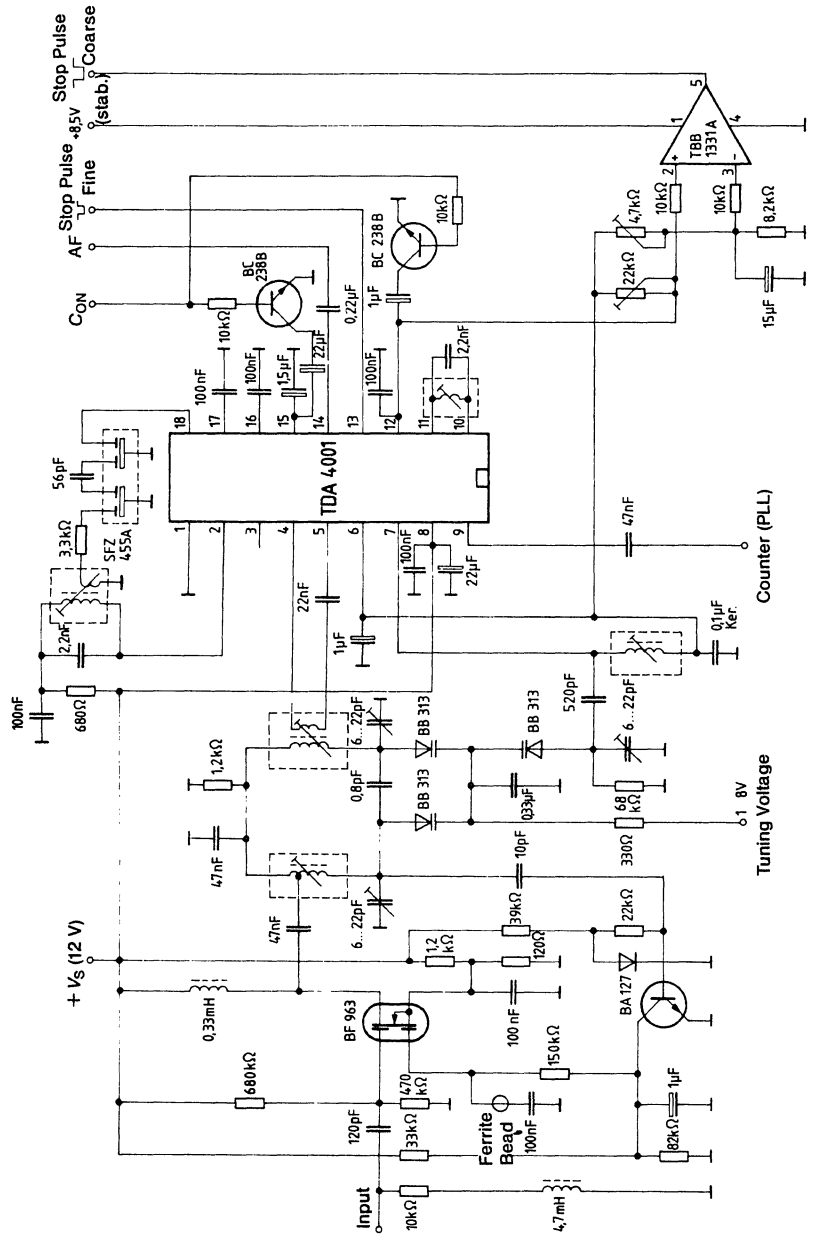


AF output voltage, total harmonic distortion, search tuning stop versus input voltage
$V_S = 15$ V; $f_{mod} = 1$ kHz, $f = 1$ MHz

0dB ≙ 775 mV (rms)

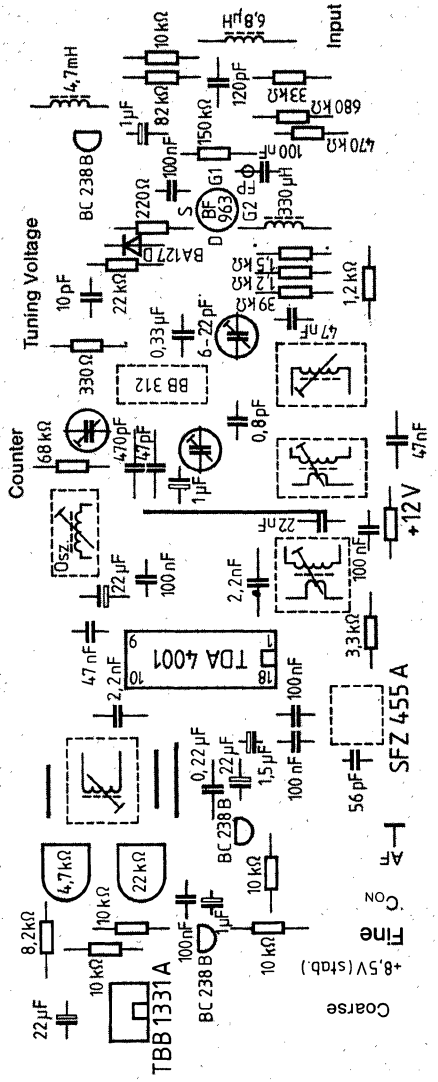


Application circuit



Plug-in location plan

Medium wave receiver with search tuning stop pulse



Preliminary Data **DIP 18**

Compare to TDA 4001 the TDA 4010 is an extended AM-receiver. This type is suitable for applications in car radios.

The IF-output V_{IQF} is at pin 15.

Features
- Internal demodulation
- Search tuning stop signal
- Low total harmonic distortion
- Minimal IF leakage at the AF output
- 2-stage ingrated low pass
- Standard IF-output

Function description
The monolithic integrated bipolar receiver has been designed to convert, amplify and demodulate AM - signals. In addition, the component provides a search tuning pulse.

The search tuning stop pulses are processed from the input signal.

The standard AM-IF signal is available at the output of the IR-receiver.

Circuit description
The impedance converter forwards the input signal V_{IRF} to the symmetrical double balanced mixer. Subsequently the signal is converted to IF with the amplitude-controlled oscillator. An external filter forwards the IF signal to the controlled IF amplifier. The amplifier IF signal and the carrier signal will be converted to AF in the subsequent synchronous demodulator. The 2-stage low pass filter forwards the available AF to the AF output.

Via an additional limiter amplifier (LA), the AF uses the carrier signal to control the coincidence demodulator (CD). The output signal of the coincidence demodulator provides the stop pulse during exact tuning and sufficient field strength.

Maximum Ratings

Maximum ratings cannot be exceeded without causing irreversible damage to the integrated ciruit.

Pos.	Maximum rating for $T_{amb} = 25\,°C$	Symbol	min	max	dim	remarks
1	Operating voltage	V_S		15.6	V	
2	Current consumption	I_S		33.0	mA	
3	Junction temperature	T_j		150	°C	
4	Storage temperature	T_S	− 40	+ 125	°C	
	Thermal resistance					
5	chip ambient	R_{thSU}		78	K/W	
6	chip package	R_{thSG}				

Functional Range

Within the functional range, the integrated circuit operates as described; deviations from the characteristic data are possible.

Pos.	Maximum rating for $T_{amb} = 25\,°C$	Symbol	min	max	dim	remarks
1	Operating voltage	V_{Batt}	7	15	V	
2	Temperature range	$\Delta\delta$	− 25	+ 85	°C	

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not stated otherwise, typical characteristics will apply at $t_{amb} = 25°C$ and the listed supply voltage.

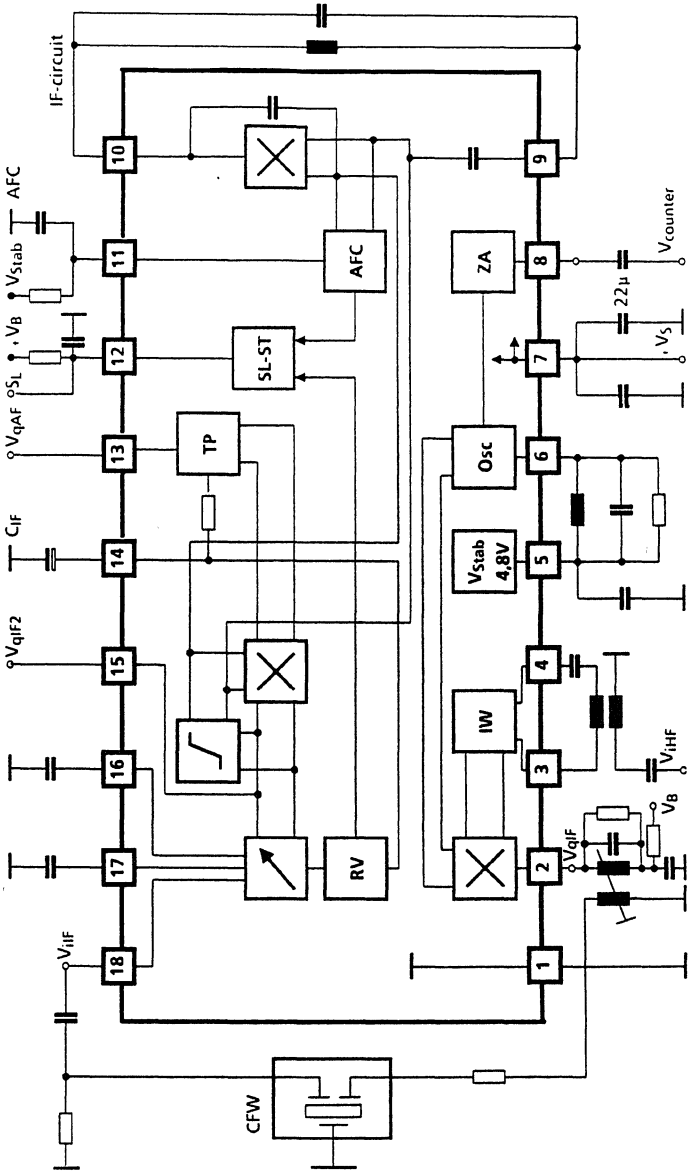
Pos.	Parameter	Symbol	Test conditions	Test circuit	Min	Typ	Max	Dim
Supply voltage			$V_S = 12V$					
Ambient temperature			$T_V = 25°C$					
1	Current consumption	I_S				15		mA
2	Reference voltage	V_{STAB}				4.8		V
3	IF-output voltage	V_{qNF}	m = 0.8			800		mV_{eff}
			m = 0.3					
4	Total harmonic		k	m = 0.8				2%
			m = 0.3				1	%
5	IF-output voltage	V_{qNF}	$20 \cdot \lg (V_{qNF}/30mV: V_{qNF}/1mV$				+3	dB
6	Input sensitivity	V_{iHF}	V_{qNF} for V_{iHF} = 1mV – 3dB			30		μV_{eff}
7	Signal-to-noise ratio	$\frac{S+N}{N}$	m = 0.3 $V_{iHF} = 10\mu V_{eff}$			6		dB
8	Signal-to-noise	$\frac{S+N}{N}$	m = 0.3 V_{iHF} = 1mV			46		dB
9	Oscillator voltage	V_{Osc}				100		mV_{SS}
10	Counter output voltage	V_{qZ}					100	mV_{SS}
11	Control range (ΔV_{qIF} = 6dB)	a				60		dB
12	3dB limit frequency of the integrated TP	f_g				5		kHz

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not stated otherwise, typical characteristics will apply at $t_{amb} = 25°C$ and the listed supply voltage.

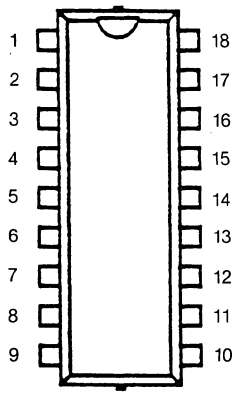
Pos.	Parameter	Symbol	Test conditions	Test circuit	Min	Typ	Max	Dim
Supply voltage			$V_S = 12V$					
Ambient temperature			$T_V = 25°C$					
13	IR-suppression	A_{IF}				40		dB
14	Conversion gain	V_m				30		dB
15	IF-output Pin 15	V_{qIF}				10		m_{eff}
16	AFC-Offset current without signal	I_{AFC}				± 10		µA
17	AFC-Offset current over control range	ΔI_{AFC}					± 10	µA
18	AFC-current	I_{AFC}	$f_{IHF} = 1MHz \pm 3kHz$				± 80	µA
19	SLS-output voltage	V_{12}	$f_{ZF} = 455kHz$				0.4	V
20	SLS-output voltage	V_{12}	$F_{ZF} = 0V$		11			V
21	SLS-output voltage	V_{12}	$f_{ZF} > 455kHz + 3kHz$		11			C
22	SLS-output voltage	V_{12}	$f_{ZF} > 455kHz - 3kHz$		11			V
23	Input impedance	Z_{IHF}	Pin 3, 4			10/1.5		kΩ//pF
24	Input impedance	Z_{IHF}	Pin 18			3.3/1.5		kΩ//pF

Block diagram

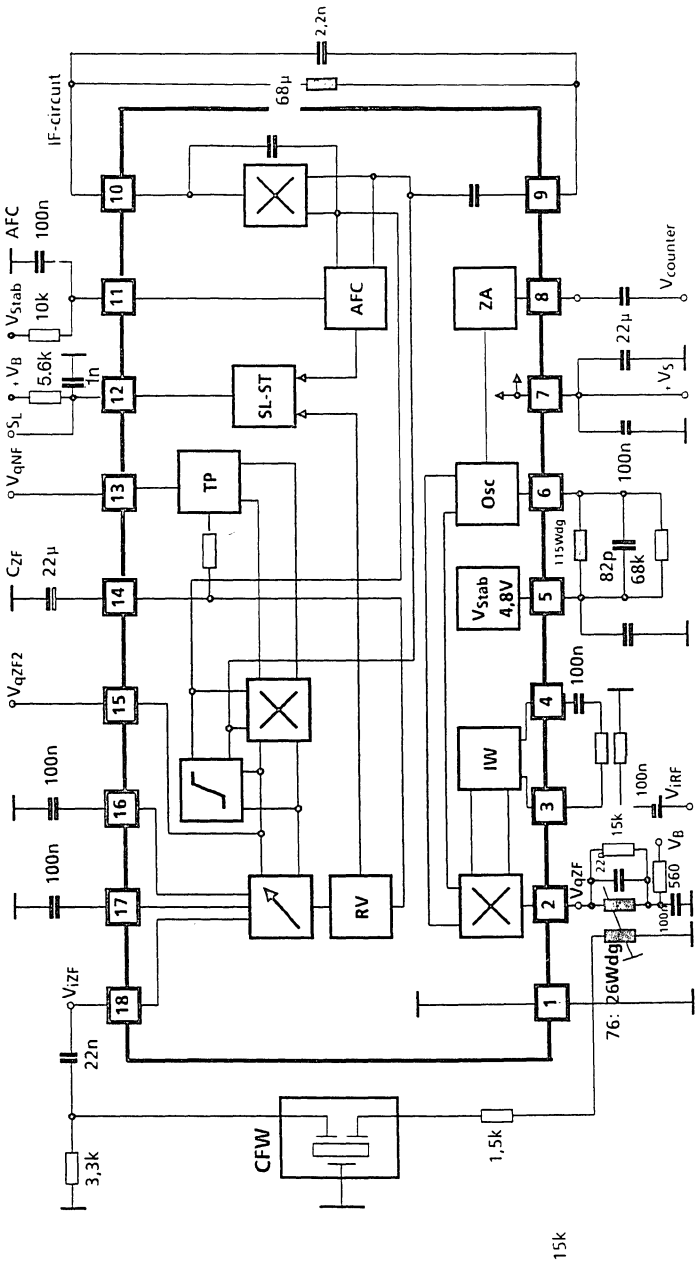


Pin configuration

Pin-Nr.	pin function
1	Ground
2	Mixer output, IF-circuit
3	RF-input
4	RF-input
5	V_{Stap}
6	Oscillator
7	Supply voltage
8	counter output
9	FM-Demodulator circuit IF-circuit
10	FM-Demodulator circuit IF-circuit
11	AFC-output
12	Search tuning stop output
13	AF-output
14	IF-time constant
15	min. IF-output
16	IF-AP follow up device
17	IF-AP follow up device
18	IF-input



measuring circuit



DIP 8

The TDA 4050 B is suitable for use as infrared preamplifier in remote control facilities for radio and TV sets.

The IC includes a controlled driver stage with subsequent amplifier stage as well as an amplifier for the threshold value. The circuit is largely balanced.

Features

- Internal AGC
- Superior large signal stability
- Short-circuit proof signal output
- Simple connection for an active band filter
- Few external components

Maximum ratings

Supply voltage	V_S	16[1])	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	140	K/W

Operating range

Supply voltage range	V_S	9 to 16	V
Ambient temperature range	T_{amb}	0 to 70	°C
Input frequency range	f_i	0 to 100	kHz

1) intermittently 17.5 V

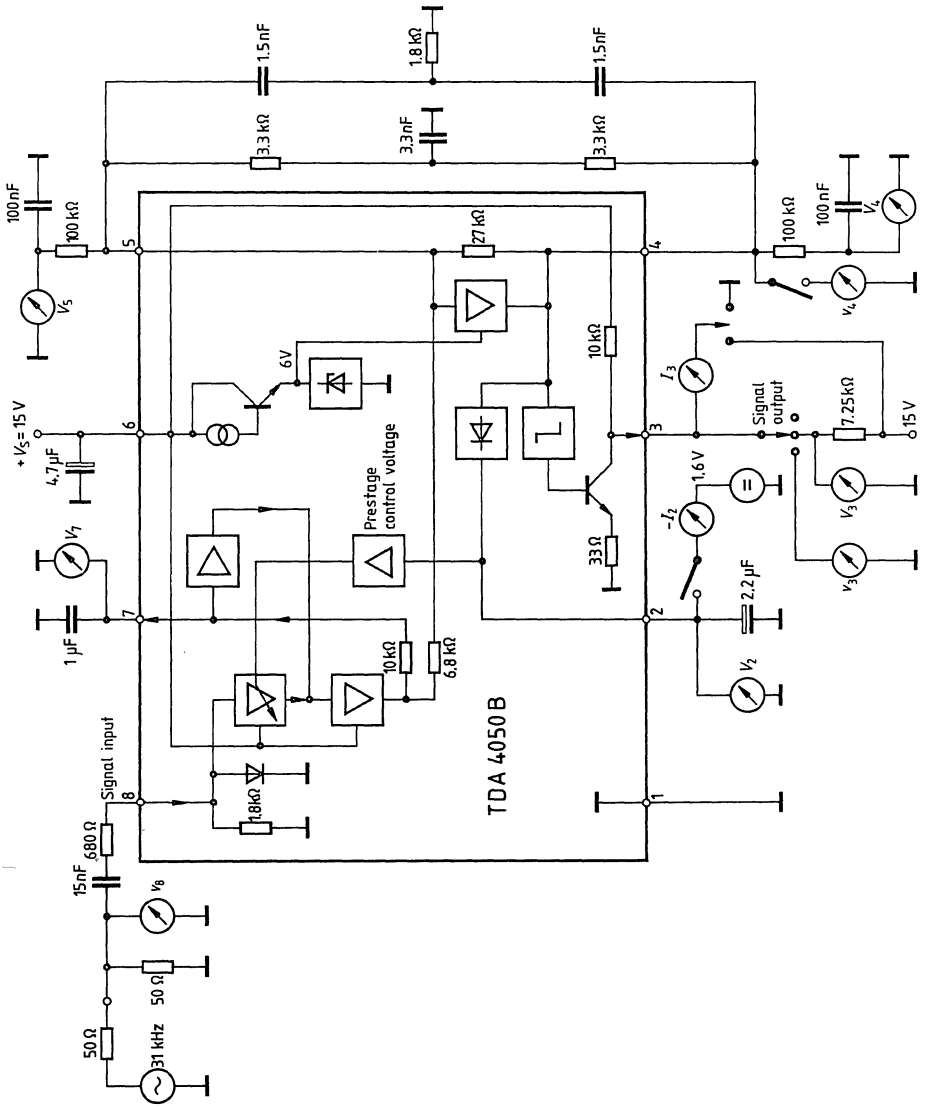
Characteristics ($V_S = 15$ V; $T_{amb} = 25$ °C; $f_{IR} = 31$ kHz) referred to measurement circuit

		min	typ	max	
Current consumption ($R_L \geq 10$ kΩ)	I_6	6	9	12	mA
Input voltage for control start	$v_{8\,rms}$		50		µV
Input voltage for output signal	$v_{8\,rms}$			85	µV
Filter output voltage (in control range)	$v_{4\,rms}$	350	450	550	mV
Gain	$G_{4/8}$	74	77	85	dB
Gain	$G_{3/4}$		21		dB
Total control range	ΔG	74	77	85	dB
Control voltage without input signal	V_2	1325	1425	1525	mV
Control voltage ($v_{8\,rms} = 100$ µV)	V_2	1.5		2.1	mV
Control voltage ($v_{8\,rms} = 10$ mV)	V_2	1.9		2.45	V
Control voltage ($v_{8\,rms} = 1$ V)	V_2	2.1		2.6	V
Operating points	$V_{4/5/7}$	2.2		2.8	V
Output current ($V_3 = V_S$)	I_3		20		mA
Output dc voltage for L level	V_{3L}		150	500	mV
Output dc voltage for H level	V_{3H}	14.6			V
Charge current ($v_{8\,rms} = 100$ mV; $V_2 = 1.6$ V)	$-I_2$	0.4		1.0	mA
Discharge current ($v_{8\,rms}$ from 1 mV to 0) ($T = 50$ ms)	I_2	0.4		3.0	µA
Input resistance	R_{i8}		1.8		kΩ
Output resistance	R_{q3}		10		kΩ
Rated resistance of the double-T network at pin 4 (unbalanced to ground)	R_4	2			kΩ

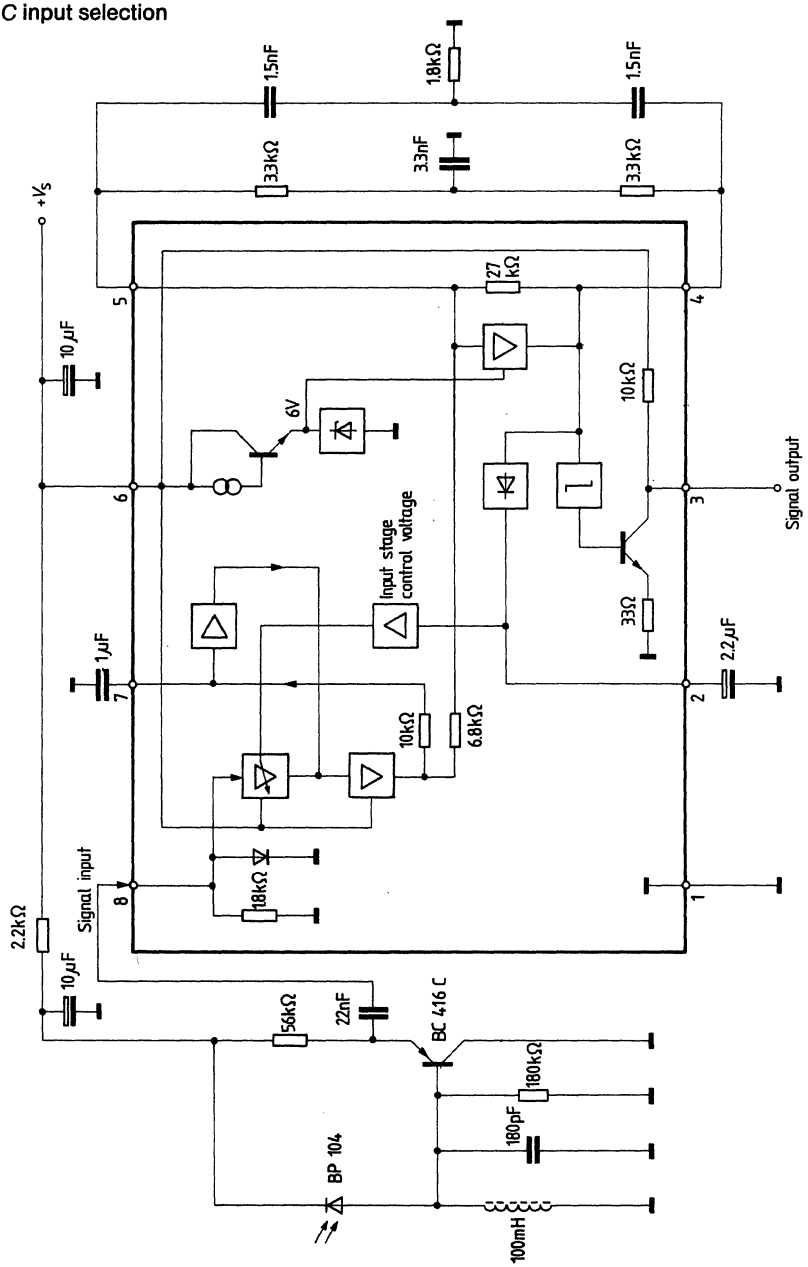
Pin configuration

Pin No.	Function
1	Ground
2	Connection for capacitance for prestage control
3	Output threshold amplifier
4	Output active filter
5	Input active filter
6	Supply voltage, positive
7	Unlocking of operating point control
8	Signal input

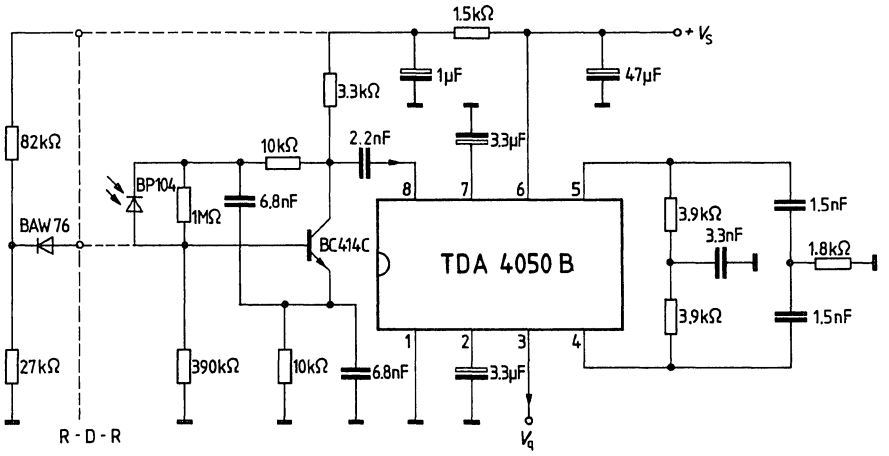
Measurement circuit and block diagram



Application circuit I
incl. *LC* input selection



Application circuit II
without coil



Notes

Circuit I uses an LC resonant circuit and is of superior quality due to its high selectivity feature (approx. 3 kHz bandwidth at −3 dB).

Circuit 2 offers the lower cost solution without coil incl. broadband input selection. Higher requirements as to steady radiation and large signal stability can be met by means of resistor-diode-resistor connection (RDR).

Preliminary Data DIP 8

The TDA 4060 is a pre-amplifier suitable for use in radio, TV, automotive and other electronics systems where infrared signal transmission is utilized.

Features

- Low voltage operation
- Wide operating frequency
- Few external components

Maximum Ratings

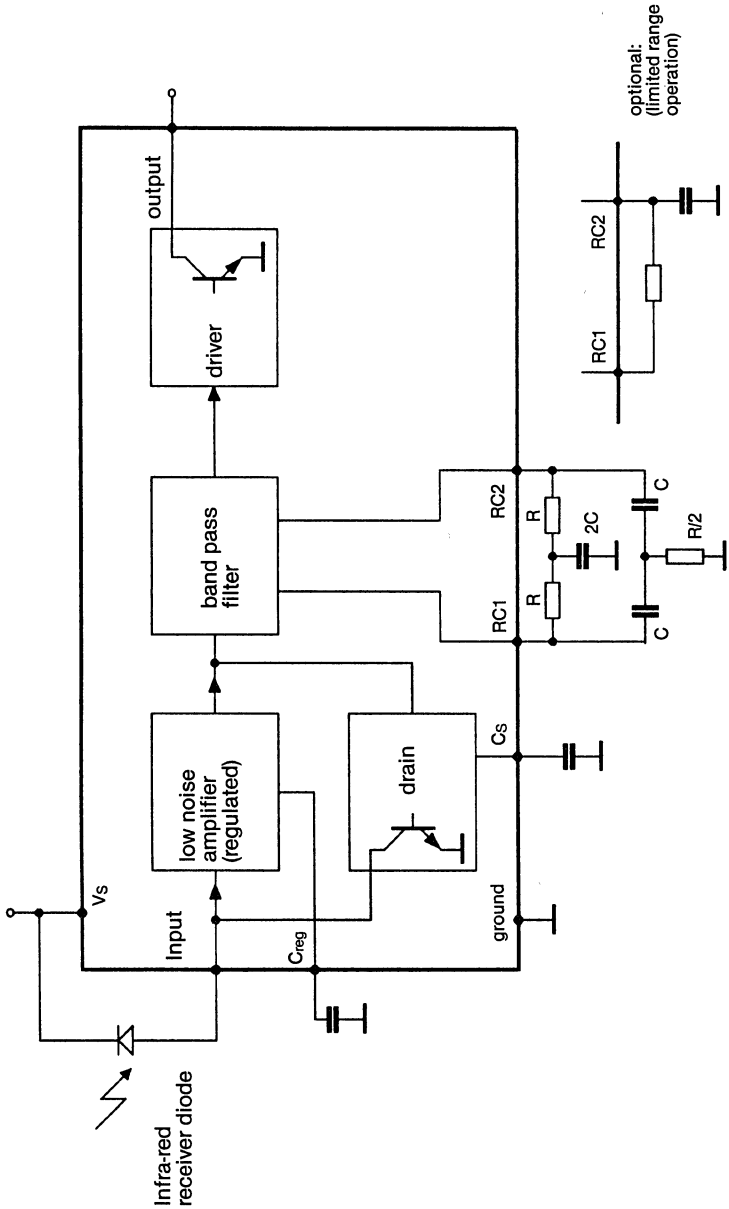
Supply voltage	V_S	7	V
Junction temp.	T_j	150	°C
Storage temp. range	T_S	− 40 to + 125	°C

Operating range

Supply voltage	V_S	3.5 - 6.5	V
Ambient temp.	T_{amb}	− 40 to + 110	°C
Input freq.	f_i	20 - 200	kHz

Additional data available on request.

Block diagram with application circuitry



FM IF IC with Search Tuning Stop Pulse, Field Strength Indicator, Mute Setting and Multipath Detector

TDA 4210-3

DIP 18

The TDA 4210-3 has been designed as FM IF component with a special demodulator for application in car radios. The sensitivity level of the input amplifier can be adjusted for applications with search tuning mode. In addition, a search tuning stop pulse is generated. Moreover, the included multipath identification circuit activates an interference suppression circuit in case of multipath interference. The TDA 4210-3 is especially suitable for application in car radios and home receivers which require a search tuning stop pulse and include an interference suppression circuit.

Features

- Multipath identification circuit
- 7-stage limiter amplifier
- Product demodulator
- AFC output
- Field strength dependent volume control
- Generation of search tuning stop pulse
- Adjustable limiter threshold
- Adjustable muting depth

Circuit description

The integrated circuit includes a 7-stage limiter amplifier with demodulator and non-controlled AF output. The limiter threshold can be raised by approx. 44 dB by means of external circuitry. Within this range the AF output signal can be continuously attenuated by max. 39 dB to eliminate the usually occurring noise products.

To suppress variable interference products, e.g. multipath interference, the TDA 4210-3 includes an identification circuit with an externally adjustable time constant.

Also included are a field strength output, an AFC output, as well as an open collector output. The latter will be activated at the zero crossing of the detector S-curve.

Maximum ratings

Ground	V_1	0	V
MUTE input	V_2	V_S	V
Muting depth	V_3	V_S	V
AF output	V_4	V_S	V
Search tuning stop signal output	I_5	5	mA
AFC output	V_6	V_S	V
Reference voltage output	I_7	5	mA
Phase shift	V_8	V_S	V
Phase shift	V_9	V_S	V
Field strength	I_{10}	5	mA
Identification output	I_{11}	5	mA
Demodulator time constant	V_{12}	V_S	V
Supply voltage	V_S	18	V
Identification input	V_{14}	V_8	V
Limiter threshold	V_{15}	V_8	V
Operating point feedback	$V_{16,17}$	V_8	V
IF input	V_{18}	V_8	V
Junction temperature	T_j	125	°C
Storage temperature range	T_{stg}	−40 to 125	°C

Operating range

Supply voltage	V_S	7.5 to 15	V
IF section demodulator	f_{iF}	0.4 to 15	MHz
Overall frequency	f	0.4 to 15	MHz
AF (V_{qAF} = 1 dB)	f_{AF}	0.02 to 150	kHz
Ambient temperature	T_A	−25 to 85	°C

Characteristics

$V_S = 8.5\,V$; $V_{i\,IF\,rms} = 10\,mV$; $f_{i\,IF} = 10.7$ MHz; $\Delta f = \pm 75$ kHz; $f_{mod} = 1$ kHz; $Q_B \approx 20$; $T_A = 25$ °C; adjustment when $I_7 = 0$; test circuit 1

		Test conditions	min	typ	max	
Current consumption	I_{13}			27	33	mA
Field strength output voltage	V_{10} V_{10}	$V_{i\,IF\,rms} = 50$ mV $V_{i\,IF\,rms} = 0$ V	3.0	3.8 0	 0.1	V V
AF output voltage	$V_{q4\,rms}$		270	380	520	mV
Total harmonic distortion during FM IF mode	THD	$I_{AFC} = 0$		0.7	1.5	%
Input voltage for limiter threshold	$V_{i\,IF\,rms}$	$V_{q4} - 3$ dB		15	30	µV
AM suppression	a_{AM}	$m = 30\%$	60			dB
Signal-to-noise ratio	$a_{S/N}$		70			dB
Current deviation of AFC output	ΔI_7	$f = f_{i\,IF} \pm 50$ kHz		± 110		µA
AFC offset	Δf_{off}	$V_i = 20$ µV..10 mV			± 15	kHz
Search tuning stop window	Δf_{ST}	$R_{6-7} = 22$ kΩ		± 18		kHz
Search tuning stop threshold FM	$V_{i\,ST}$	$V_6 = V_{S/2}$			70	µV
Search tuning stop threshold AM	$V_{i\,ST}$	$V_6 = V_{S/2}$			500	µV
Stabilized voltage	V_7		3.6	4.1	4.6	V
Adjustable range of limiter threshold via pin 15	$V_{i\,IF}$	$V_{15} = 0$; $V_{15} = V_{REF}$		44		dB
AF mute	a_{AF} a_{AF}	$V_2 = 0$; $R_{3-1} = \infty$ $V_2 = 0$; $R_{3-1} = 0$	3 31	7 39	11 47	dB dB
AF mute switch-off voltage	V_2			0.5	0.75	V
MP sensitivity for full drive at pin 1	$V_{i\,14\,rms}$	$f = 20$ kHz		5		mV
Charge current pin 12	I_{12}	pin 14 to ground		3		mA
Discharge current pin 12	I_{12}	pin 14 open, $V_{12} < 1$ V		10		µA

Additional data with respect to application

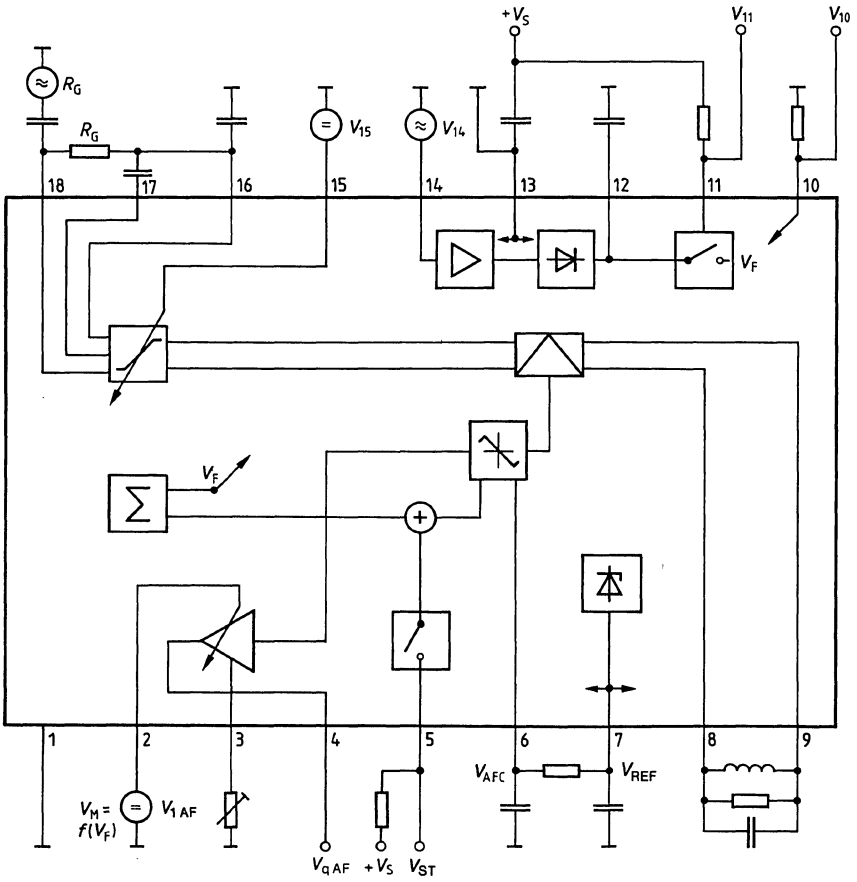
(data does not apply to series measurement)

DC voltage AF output	V_{q5}		2.8	3.8	4.8	V
Internal DC current of emitter follower output	I_4		0.75	1		mA
Input resistance for demodulator circuit	R_{9-10}		27	35		kΩ
Search tuning stop "low"	V_6				1.3	V
Search tuning stop "high"	V_6		7			V

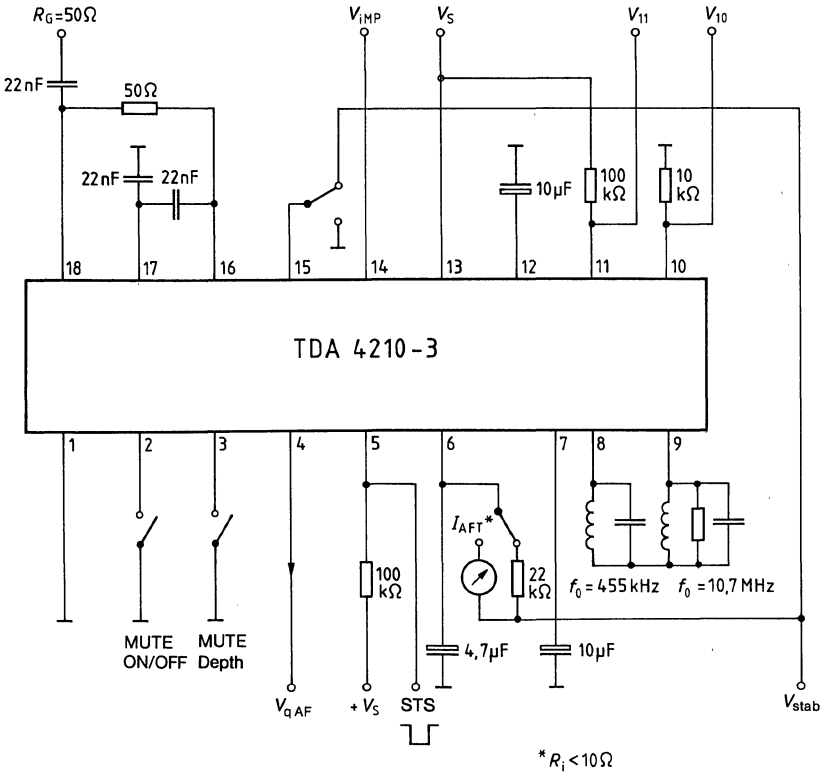
Pin description

Pin	Function
1	Ground: capacitors for operating point feedback, V_S, and V_{REF} decoupling are to be connected directly to pin 1
2	Mute input for (usually derived from field strength output voltage) dc voltage which attenuates the AF output voltage by the set muting depth (pin 4). Max. attenuation when $V_2 = 0$ V, no attenuation when $V_2 \geq 0.75$ V
3	Muting depth adjustment: by connecting a resistor to ground the requested muting depth can be set. Maximal attenuation of AF output voltage with $R = 0$ (approx. 39 dB), minimal attenuation with $R = \infty$ (approx. 7 dB)
4	AF output for demodulated FM-IF
5	Search tuning stop (ST) output is connected when the input field strength exceeds the search tuning stop pulse threshold and the input frequency lies within the search tuning stop pulse window.
6	AFC output: push-pull current output, referenced via a resistor connected to a fixed voltage source (e.g. V_{REF}). The voltage generated at the resistor is in proportion to the deviation from the nominal input frequency and can be applied for retuning purposes.
7	Reference voltage: should be RF decoupled to pin 1. The AFC resistor and the potentiometer for the limiter threshold are referenced to V_{REF}.
8/9	Demodulator tank circuit: driven via two integrated capacitors (approx. 40 pF $\pm$25%). The circuit voltage should be approx. 200 mV (peak-to-peak)
10	Field strength output: supplies a dc voltage proportional to the input level, which quickly adjusts to changes in the input voltage
11	Identification output: designed as an open NPN collector output, which connects an additional time constant in parallel to pin 2 during multipath interference, or activates another circuit to suppress variable interference.
12	Demodulator time constant: determines the response and hold time of the identification circuit.
13	Supply voltage: to be RF decoupled to pin 1
14	Identification input: high impedance input ($R_i \sim 10$ kΩ). This input receives variable interference forwarded on the field strength voltage via a high-pass filter.
15	Input for setting limiter threshold: with a potential between V_{REF} and 0 V, the limiter threshold can be varied by approx. 44 dB.
16/17	Operating point feedback to be RF decoupled. For efficient push-push suppression, pin 16 should be blocked against pin 17 and latter to ground (pin 1).
18	IF input: frequency modulated IF voltage is injected at pin 18.

Block diagram



Measurement circuit



Quasi-Parallel sound IC with FM IF, sym. Input and Volume Control

TDA 4282 T

DIP 22

The TDA 4282 T is a controlled AM amplifier with FM demodulator (to produce an intercarrier) and subsequent sound-IF limiting amplifier with coincidence demodulator, standard VCR connection and separate AF-output with volume control.

- Outstanding limiting qualities
- Connection for video recorder
- Little external circuitry

Maximum ratings

Supply voltage	V_S	15	V
$t \leq 1$ min	V_S	16.5	V
Thermal resistance (system-ambient air)	$R_{th\,SA}$	65	K/W
Junction temperature	T_j	150	°C
Storage temperature	T_{stg}	−40 to 125	°C

Operational range

Supply voltage	V_S	11 to 15	V
Frequency range AM part	f_{AM}	10 to 60	MHz
FM part	f_{FM}	0.01 to 12	MHz
Control voltage AM part	V_2	0 to 5	V
Switch current FM part	I_8	0.3 to 1	mA
Ambient temperature in operation	T_{amb}	0 to 60	°C

Characteristics (V_S = 15 V, T_{amb} = 25°C)

		min	typ	max	
Current consumption	I_5		60	80	mA
AM-part:					
AGC-range	ΔG		55		dB
AGC-voltage	V_2	0		5	V
Input resistance	$R_{i\,3\text{-}4}$		10		kΩ
Input impedance at max. gain	$Z_{i\,20\text{-}21}$		1.8/2		kΩ/pF
at min. gain	$Z_{i\,20\text{-}21}$		1.9/0		kΩ/pF
Output resistance	$R_{q\,6}$		500		Ω
	$R_{q\,7}$		500		Ω
FM-part: (f_r = 5.5 MHz; f_{mod} = 1 kHz)					
Input impedance	$Z_{i\,9\text{-}10}$		800		Ω
AM-suppression	a_{AM}		42		dB
($V_{i\,9\text{-}10}$ = 1 mV; f = 12.5 MHz; m = 30%)					
Signal-to-noise ratio ($V_{i\,9\text{-}10}$ = 10 mV)	$a_{S/N}$		85		dB
Input voltage for limiting	$V_{i\,lim.}$		60		µV
(Δf = 30 kHz)					
Demodulator output resistance	$R_{q\,15\text{-}16}$		5.4		kΩ
Output resistance for VCR-recording	$R_{q\,12}$			500	Ω
Input resistance for VCR-playback	$R_{i\,12}$	10			kΩ
Integrated resistor for deemphasis	R_{17}		10		kΩ
AF-output voltage	$V_{q\,12}$		600		mV_{rms}
(V_i = 10 mV; with CDA 5.5 MC 10, $R_{q\,11}$ = 2.9 Ω)	$V_{q\,11}$	260	300		mV_{rms}
(Δf = 12.5 kHz)					
AF-gain during VCR-playback	$V_{12\text{-}11}$		0.5		
Total harmonic distortion	THD_{12}		1		%
Cross talk (V_i = 1 mV)					
V_{12} = 2 V_{rms}	$C_{12\text{-}11}$	50	52		dB
V_{12} = 0.3 V_{rms}	$C_{12\text{-}11}$	60	65		dB
Range of volume control	$\frac{V_{AF\,max}}{V_{AF\,min}}$	70	85		dB

Circuit description

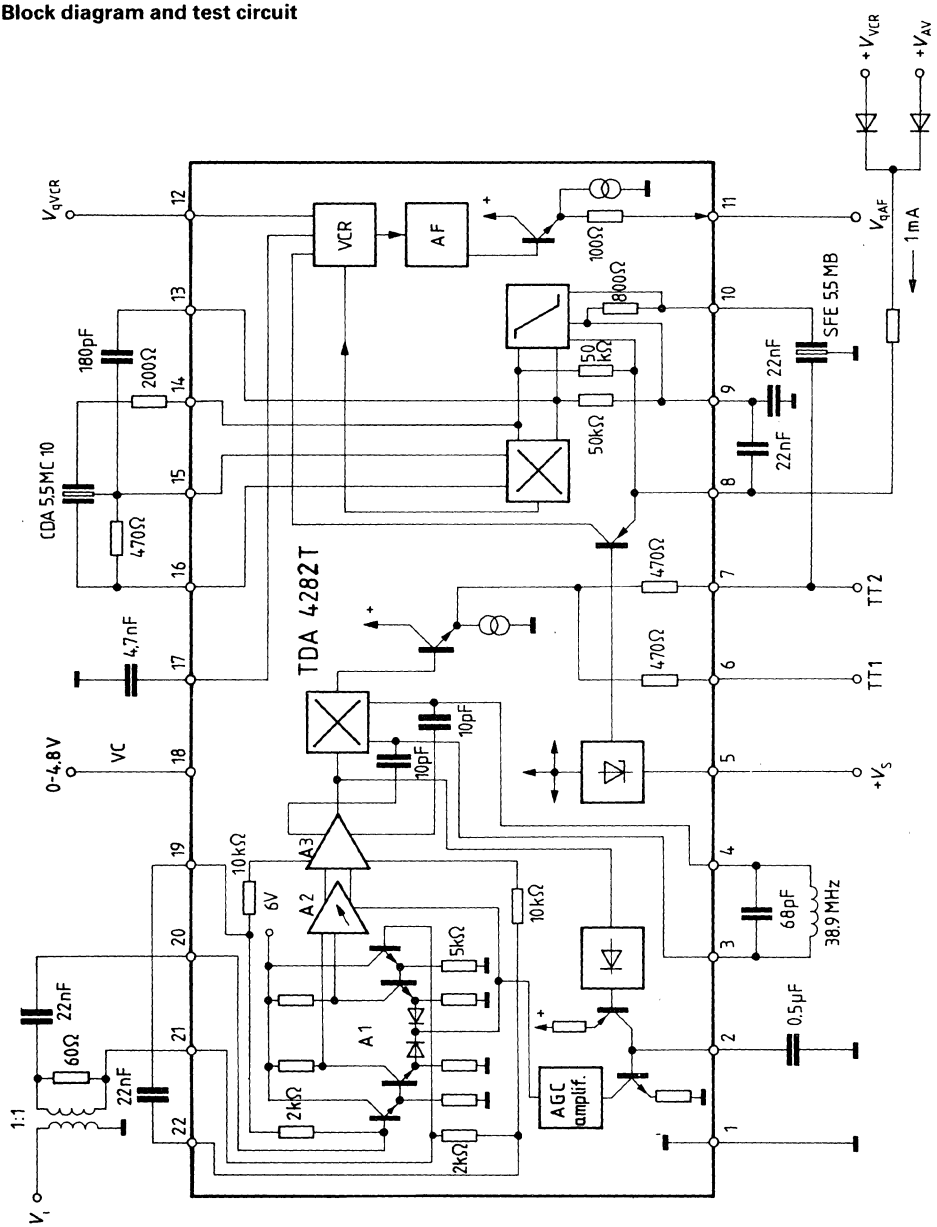
The TDA 4282 T contains essentially two functional blocks:

1. A regulated AM amplifier with a peak rectifier to generate the AGC voltage. The AM amplifier drives an FM demodulator, at the output of which the differential sound carrier (38.9 MHz–33.4 MHz = 5.5 MHz) is available. The double sideband portions close to the carrier are suppressed. The 5.5 MHz carrier reaches the functional block via an external selection.
2. An FM limiter amplifier with coincidence demodulator, a standard VCR connector and a separate AF output with volume control.

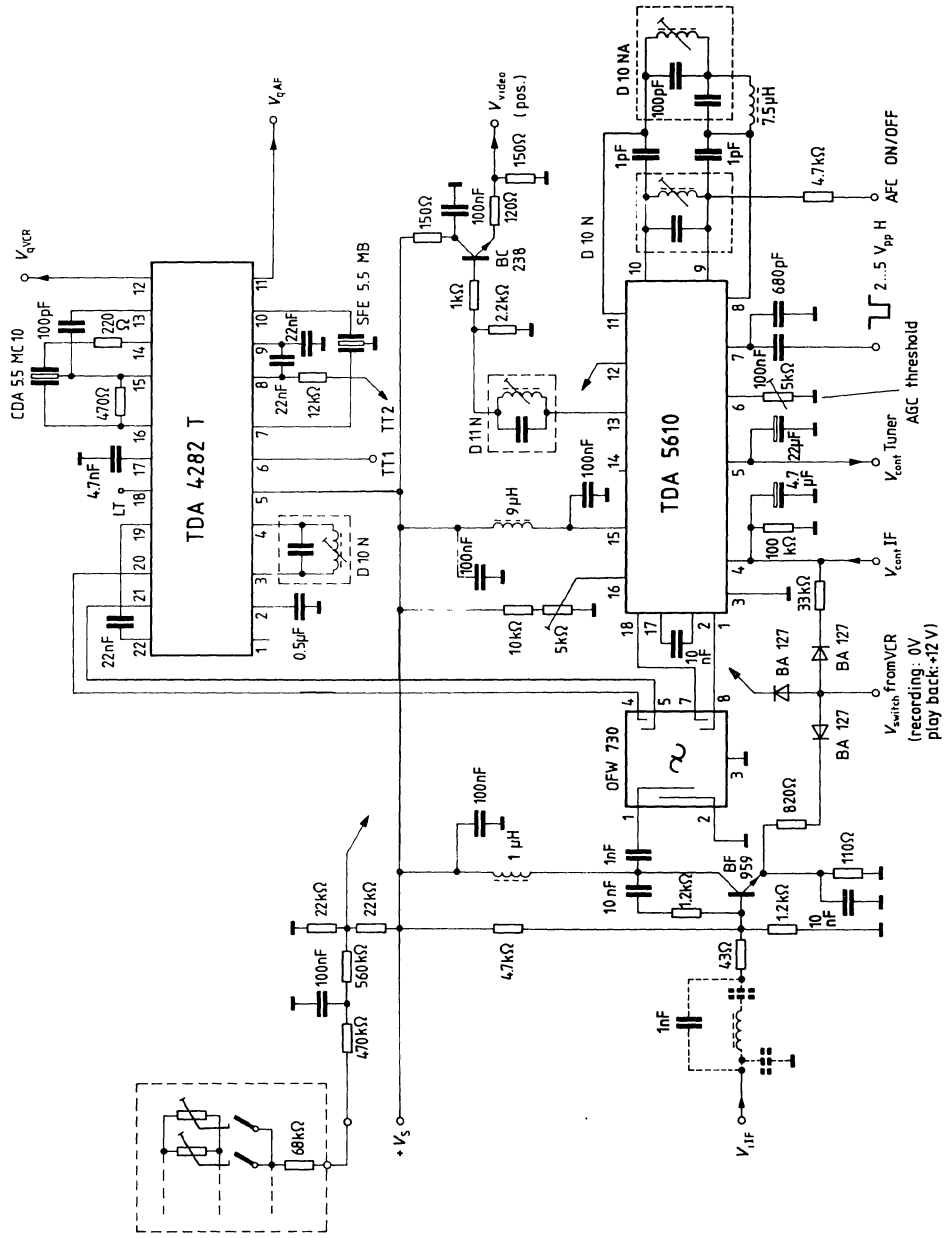
Pin assignment

Pin No.	Pin designation
1	Ground
2	AM-IF control
3	AM amplifier demodulator
4	AM amplifier demodulator
5	Supply voltage (plus)
6	AM amplifier sound carrier output TT 1
7	AM amplifier sound carrier output TT 2
8	AM-IF amplifier negative feedback for working point
9	AM-IF amplifier negative feedback for working point
10	FM-IF amplifier IF input
11	AF output
12	VCR connection
13	FM-IF amplifier emitter follower output
14	FM-IF amplifier emitter follower output
15	FM amplifier demodulator
16	FM amplifier demodulator
17	Deemphasis condensator
18	Volume control
19	AM-IF negative feedback for working point
20	AM-IF amplifier IF input
21	AM-IF amplifier IF input
22	AM-IF negative feedback amplifier for working point

Block diagram and test circuit



Application circuit



DIP 24

Stereo tone control IC for controlling the trebles, basses, balance, volume, physiology, bandwidth of the AF signals by the aid of dc voltages.

It is in compliance with the standards DIN 45500 and IEC 268-3.

The component is especially suited for application in TV stereo devices.

Features

- Few external components
- Low total harmonic distortion
- Large output signal capability

Maximum ratings

Supply voltage	V_{S16}	0 to 18	V
Reference current	I_{REF}	5	mA
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	70	K/W

Operating range

Supply voltage	V_{S16}	8 to 15.75	V
Ambient temperature	T_A	0 to 70	°C

Characteristics

$T_A = 25\,°C$

		min	typ	max	
Current consumption P1...P4 = 22 kΩ	I_{S16}		40	70	mA
Reference voltage	V_{REF}	4.5	4.8	5.2	V
Input resistance	$R_{i\,4;22}$	10	14	18	kΩ
Gain for $V_{24} = V_{REF}$ [1] $V_{3,2,23} = V_{REF}/2$	V_q/V_i	−4	−1	2	dB
Gain for $V_{24} = 0$ [1] any position of S3; S4 open	V_q/V_i	−75	−85		dB
Control range balance [1] $V_{24} = V_{REF}$; $V_{2,3} = V_{REF}/2$	$V_{B\,max}$ $V_{B\,min}$	1.5 −20	4 −30	6	dB dB
Bass emphasis [1] $V_3 = V_{REF}$; $f_i = 40$ Hz	$V_{B\,max}$	+9	+12	+16	dB
Bass deemphasis $V_3 = 0$; $f_i = 40$ Hz	$V_{B\,min}$	−10	−12		dB
Treble emphasis [1] $V_2 = V_{REF}$; $f_i = 15$ Hz	$V_{T\,max}$	+8.5	+11.5	+14.5	dB
Treble deemphasis $V_2 = 0$; $f_i = 15$ kHz	$V_{T\,min}$	−10	−12		dB
Channel separation S4 open	$a_{L\text{-}R}$	60			dB
Channel separation (antiphased) for S4 closed	$a_{L\text{-}R}$	3	5		dB
Input voltage [1]					
$V_{2,3}$ = any	$V_{i\,rms\,4,22}$			1	V
$V_{2,3} = V_{REF}/2$	$V_{i\,rms\,4,22}$			3.5	V
Total harmonic distortion [1] $V_{2,3}$ = as applied; $V_{i\,rms} = 1$ V $f_i = 60$ Hz to 12 kHz	THD		0.5	1	%
Total harmonic distortion DIN 45500 [1] $V_{2,3} = V_{REF}/2$; $V_{i\,rms} = 1$ V	THD		0.3	0.6	%
Flutter and wow L-R $f_i = 1$ kHz, $V_q/V_i = 0$ to 40 dB $f_i = 20$ Hz to 20 kHz	$\Delta a_{L\text{-}R}$			2	dB
Any regulator	$\Delta a_{L\text{-}R}$			4	dB
Disturbance voltage spacing according to DIN 45405 $f_i = 20$ Hz to 20 kHz; $V_{i\,rms} = 1$ V	$a_{S+N/N}$	73	76		dB
Noise voltage with reference to output $f_i = 20$ Hz to 20 kHz $V_i/V_q = 0$ dB [2]	$V_{n\,rms}$		155	230	μV
$V_i/V_q = 50$ dB	$V_{n\,rms}$		10	20	μV
Output resistance	$R_{q\,11,12,14,15}$		0.2	0.3	kΩ
Input current for adjusters $V_{st} = 0$ to V_{REF}	$I_{i\,2,3,23,24}$	−20		0	μA
Input current for switches	$I_{i\,8,18}$	−60	−13	0	μA

Electrical data identified with [1] is only applicable at $V_S = 15$ V +5% and $V_{rms} = 1$ V. Furthermore, the maximum input voltage decreases in accordance with lower supply voltages.

[2] Inputs terminated with 1 kΩ.

Characteristics

$V_S = 15$ V; $T_A = 25$ °C

		min	typ	max	
Level of the switches	$V_{sw\,H}$	$V_{REF} - 1$		V_{REF}	V
H or open	$V_{sw\,L}$	0		1	V
Downcontrol diff. of the AF outputs	ΔV_q	14	21	28	dB
S3 open					
$V_{24} = 3/4\ V_{REF}$					
Disturbance voltage at the output (DIN 45405)	V_d		35	50	µV
$f_i = 20$ Hz to 20 kHz; $V_i/V_q = -20$ dB					
Noise voltage CCIR; (DIN 45405)	$V_{n\,pp}$			650	µV
$V_{24} = V_{REF}$; $V_2 = 0$					
Amplitude variation trebles,			±0.5	±1.5	dB
basses in middle position					
$V_{23} = V_{REF}/2$; $f_i = 40$ Hz, 1 kHz, 15 kHz					
Output voltage deviation	$\Delta V_{qL\,n\,pp}$			300	mV

Pin description

Pin	Function
1	Reference voltage
2	Treble control input
3	Bass control input
4	Input right
5	Cutoff frequency bass
6	Right
7	Cutoff frequency treble right
8	Switch input physiology
9	Start frequency base width right
10	GND
11	Output right
12	Output right
13	Blockage
14	Output left
15	Output left
16	Supply voltage
17	Start frequency base width left
18	Switch input base width
19	Cutoff frequency treble left
20	Cutoff frequency bass
21	Left
22	Input left
23	Balance control input
24	Volume control input

Circuit description

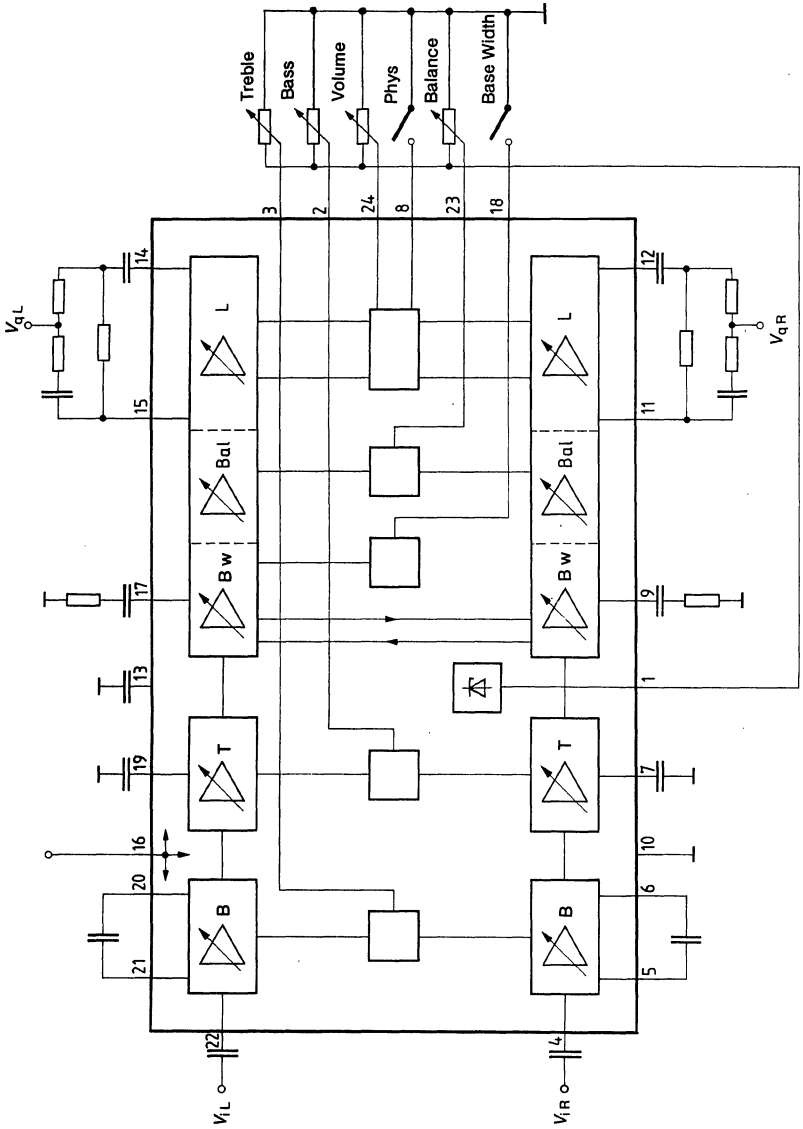
The component includes 5 operational amplifiers per stereo channel. The operational amplifiers are equipped with either dc voltage controlled attenuators or switches. By applying potentiometers to the externally connected capacitors, the emphasis or deemphasis of low or high frequencies can be controlled. The base width can be switched by the subsequent stage. This stage will not respond during open switch status. However, with a closed switch, antiphased crosstalk of estimated 66% occurs at a frequency of approx. 300 Hz, which has been determined by one of the external capacitors. To ensure that the base width effect remains independent of the balance setting, balance control is performed subsequently to the base width control. The volume control is comprised of 2 stages. The identical configuration and parallel layout of these stages, designed to affect base width, balance, and volume, provide at the same time simultaneous electrical and thermical tracking. In the volume stage the rising incline of the volume characteristic can be switched to lower values. Both outputs have been equipped with a resistor capacitor network for physiologically correct amplification adjustment. Frequency independent (linear) amplification adjustment is obtained during the identical rise of the volume characteristic at both outputs.

In order to prevent disruptive clicking noises, the delay switch releases the AF output voltage subsequently to the supply voltage and voltage stabilization in the component.

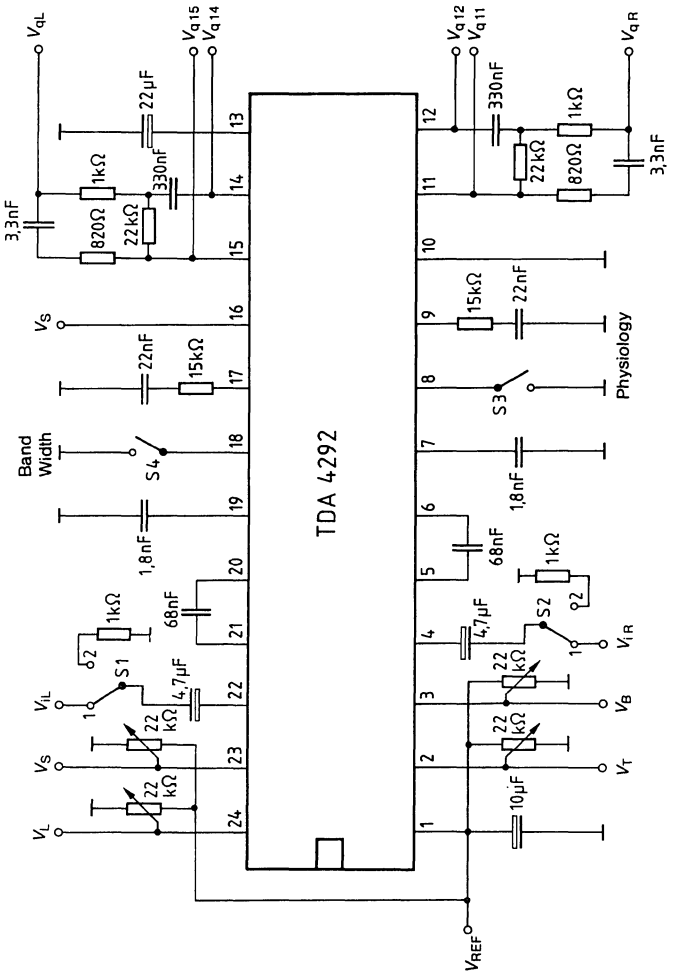
Pin description

Pin	Function
1	Reference voltage, typ. 4.8 V
2	Adjusting input for treble control. Adjusting range 0 V to V_1. PNP transistor input, the base current flows out.
3	Adjusting input for bass control. Features like pin 2.
4	Signal input right. The dc socket is approx. $V_{16}/2$ −0.7 V. The input resistance is frequency-dependent (minimum at high frequencies) and dependent on the position of the bass control (minimum at full low-frequency peaking)
5, 6	Connections for external capacitance of the right bass control $f_{3dB} \approx 1/C_{5,6}$.
7	Connection for ext. capacitance of the right treble control. $f_{3dB} \approx 1/C_7$
8	Switching input for physiology. Internal pull-up resistance against V_1 is available. Physiology "ON" for not connected pin or $V_8 \geq V_1 - 1$ V.
9	Connection for network of the stereo basewidth enlargement. Crosstalk ≈ 1/Rg. $f_{3dB} = \frac{1}{2\pi C_9 (R_9 + 3\,k\Omega)}$
10	GND
11, 12	AF outputs right. (NPN emitter follower). At physiology "OFF" both outputs supply the same level. At physiology "ON" a level difference dependent on the volume adjustment occurs. (Pin 11 is on a higher level).
13	Blocking for internal dc operating points. The capacitance determines also the duration of the switch-on delay after applying V_{16}.
14,15	AF outputs left. The function corresponds to the function of pin 11, 12. (pin 11 ≡ pin 15, pin 12 ≡ pin 14)
16	Supply voltage
17	Like pin 9, left
18	Switching input for basewidth. Internal pull-up resistance against V_1 is available. Basewidth "OFF" for not connected pin or $V_{18} \geq V_1 - 1$ V.
19	Like pin 7, left
20, 21	Like pin 5, 6, left
22	Input left, features like pin 4.
23	Adjusting input for balance control. Features like pin 2.
24	Adjusting input for volume control. Features like pin 2.

Block diagram

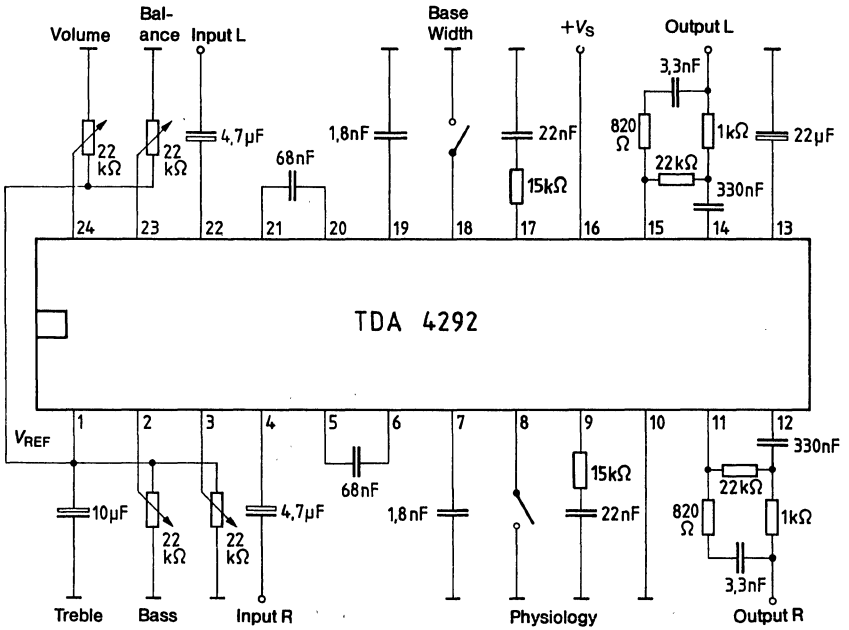


Measurement circuit

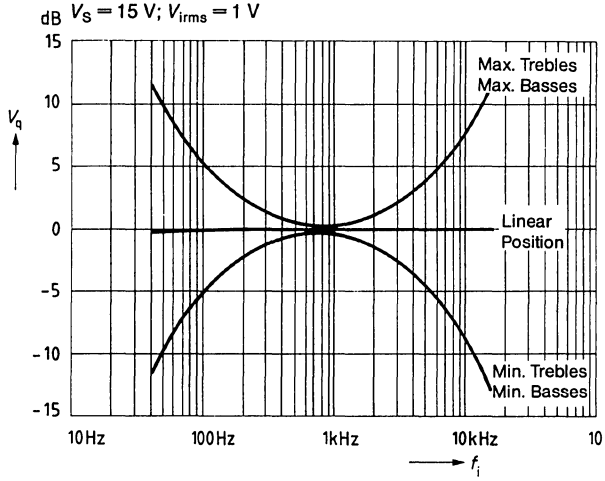


S1, S2 in position 2 during noise measurement

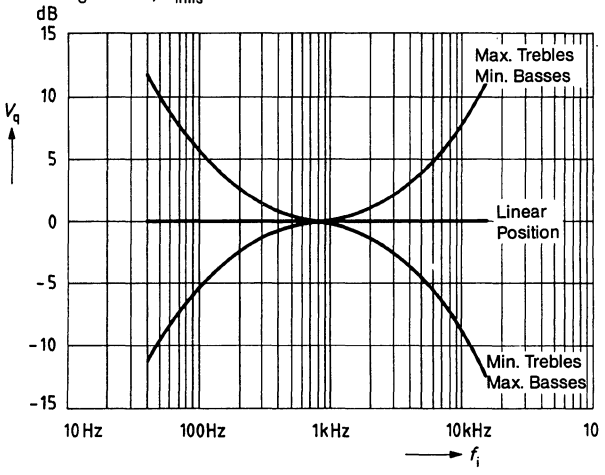
Application circuit



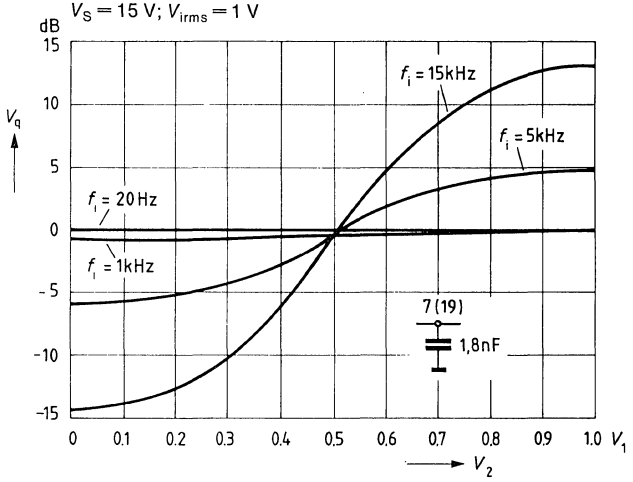
Bass and treble control
S3 closed, S4 open
$V_S = 15$ V; $V_{irms} = 1$ V



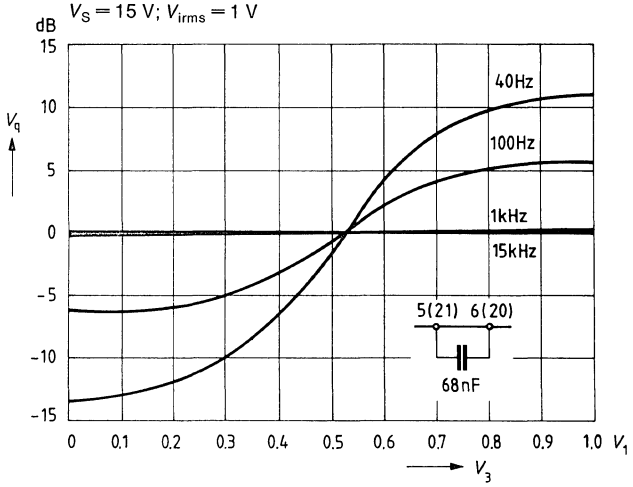
Bass and treble control
S3 closed, S4 open
$V_S = 15$ V; $V_{irms} = 1$ V



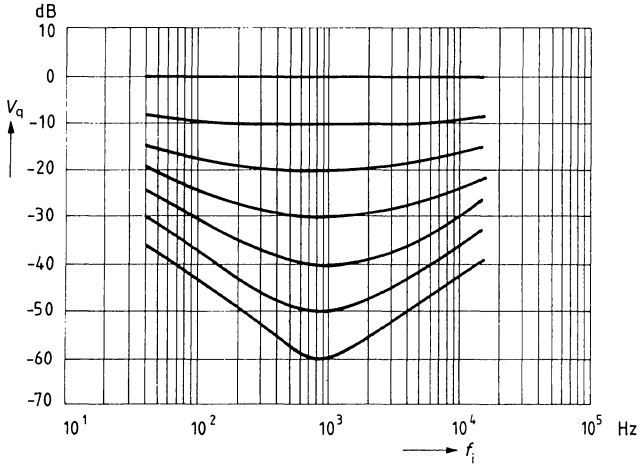
Treble control
S3 closed, S4 open
$V_S = 15$ V; $V_{irms} = 1$ V



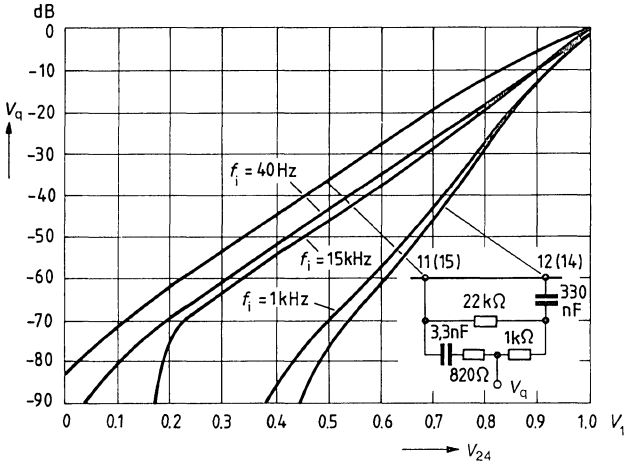
Bass control
S3 closed, S4 open
$V_S = 15$ V; $V_{irms} = 1$ V



Physiological volume control
$V_S = 15$ V; $V_{irms} = 1$ V



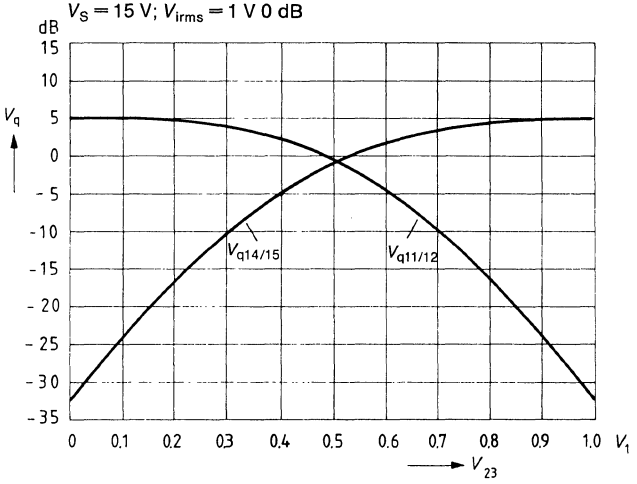
Volume control with physiology
$V_S = 15$ V; $V_{irms} = 1$ V



Balance

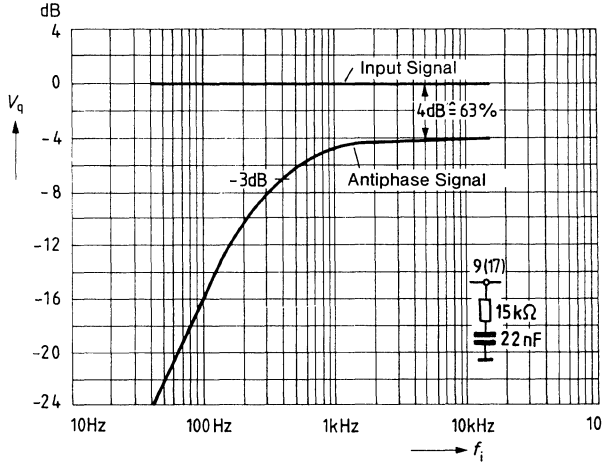
S3 closed, S4 open

$V_S = 15$ V; $V_{irms} = 1$ V 0 dB

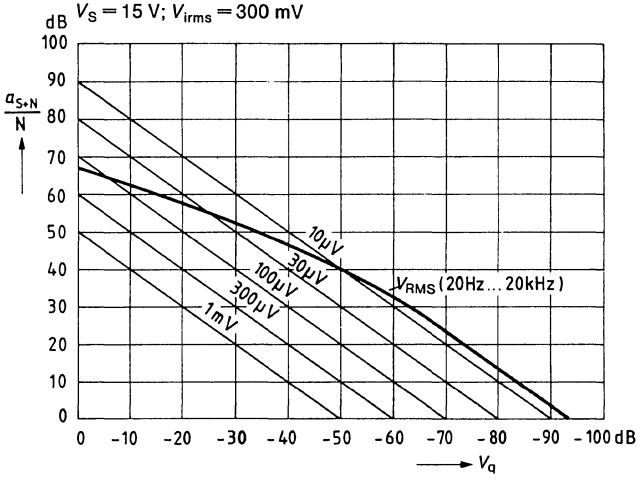


Base width

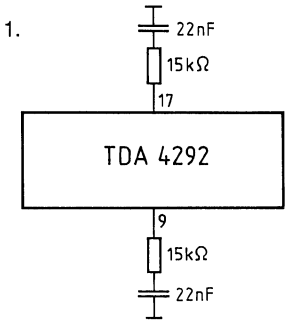
$V_S = 15$ V; $V_{irms} = 1$ V



Disturbance voltage spacing
S3 closed, S4 open
$V_S = 15$ V; $V_{irms} = 300$ mV



Base width circuits



a) **Stereo reception**

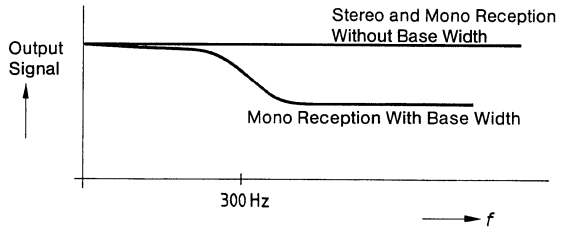
i.e. normal linear frequency response and stereo sensation with closely spaced loudspeakers.

With the base width ON the base-width effect has a time constant of 22 nF/15 kΩ, i.e. the subjective spacing between the loudspeakers is greater.

b) **Mono reception** (with base width ON)

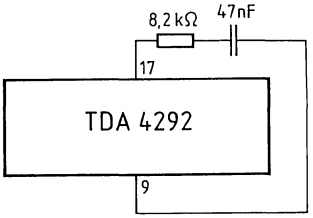
Normal linear frequency response and mono sensation.

With the base width ON there is a deemphasis of approx. −5 dB from about 300 Hz onwards. This causes slight treble deemphasis and the acoustic impression is duller and somewhat quieter.



Effect: At mono signal: trebles approx. −5 dB
At stereo signal: cross-talk over 300 Hz

2.

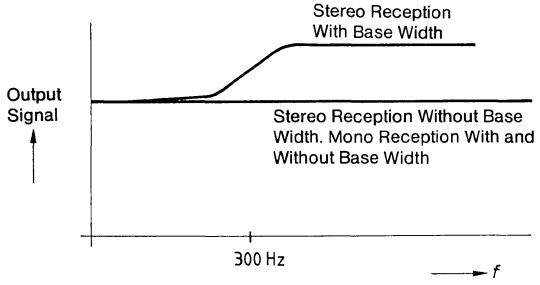


a) **Stereo reception and base width ON**

The trebles are emphasized from 300 Hz onwards by up to +5 dB (time constant 8.2 kΩ and 4 nF), i.e. with the base width switched on there is simultaneously a slight change in the timbre of the acoustic impression.

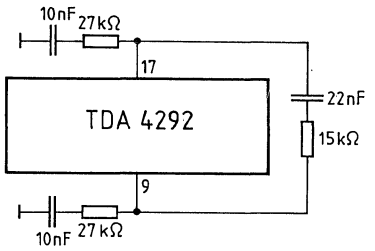
b) **Mono reception and base width ON**

Switching on the base width produces no change at all in the acoustic impression.



Effect: At mono signal: no influence
At stereo signal: trebles approx. +5 dB

3.



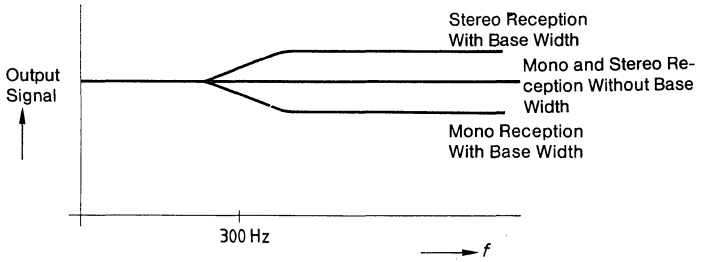
a) **Stereo reception and base width ON**

From 300 Hz onwards emphasis of the trebles by +2.5 dB with the corresponding time constants.

b) **Mono reception and base width ON**

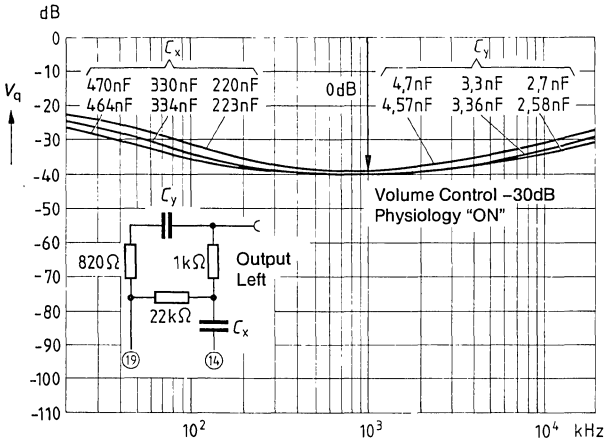
From about 300 Hz onwards deemphasis by about -2.5 dB.

With the corresponding time constants this produces a slight loss of treble and makes the acoustic impression darker and quieter.

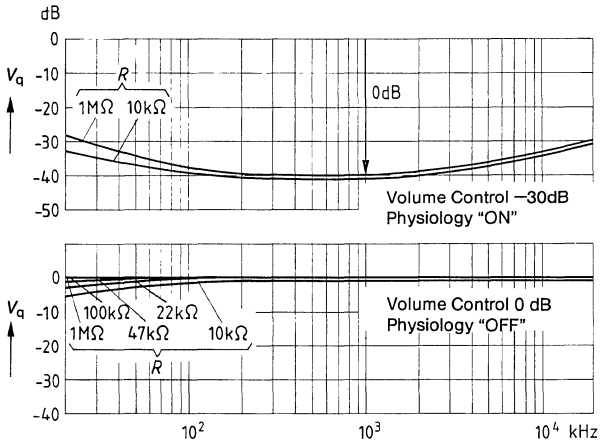


Effect: At mono signal: trebles approx. −2.5 dB
At stereo signal: trebles approx. +2.5 dB

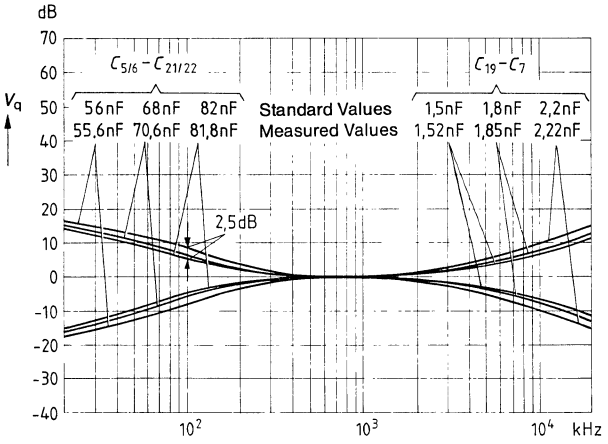
Physiological volume control (loudness) versus frequency and capacitance values C_x G_V deviations for different capacitances (R_L at output 1 MΩ).



Physiological volume control (loudness) versus frequency and load resistance R Output loaded with R ($C_y = 3.3$ nF; $C_x = 680$ nF).



Bass and treble control versus frequency
G_V deviations for different capacitances (load at output 1 MΩ)



Alteration of frequency response through component tolerances

- **Bass control**

Capacitor	Pin 21/20 – 5/6	C = 68 nF
68 nF – 20%	G_V = + 1.5 dB	
68 nF	G_V = 0 dB	f = 100 Hz
68 nF + 20%	G_V = – 1 dB	

- **Treble control**

Capacitor	Pin 19 – 7	C = 1.8 nF
1.8 nF – 20%	G_V = – 1 dB	
1.8 nF	G_V = 0 dB	f = 10 kHz
1.8 nF + 20%	G_V = + 1.5 dB	

- **Physiology network**

Capacitor for bass emphasis C_x = 330 nF

330 nF – 30%	G_V = – 3 dB	
330 nF	G_V = 0 dB	f = 100 Hz
330 nF + 40%	G_V = + 2 dB	

Capacitor for treble emphasis C_y = 3.3 nF

3.3 nF – 20%	G_V = 1 dB	
3.3 nF	G_V = 0 dB	f = 10 kHz
3.3 nF + 40%	G_V = + 2 dB	

- **Terminating resistor**

R_A = 10 kΩ	G_V = – 5 dB	
R_A = 22 kΩ	G_V = – 2.5 dB	
R_A = 47 kΩ	G_V = – 1 dB	f = 20 Hz
R_A = 100 kΩ	G_V = – 0.5 dB	
R_A = 1 MΩ	G_V = 0 dB	

Preliminary data SIP 9

The integrated circuit TDA 4600-3 is designed for driving, controlling, and protecting the switching transistor in self-oscillating flyback converter power supplies. In addition to its application in TV receivers and video tape recorders, this IC can also be used in hifi devices and active loud speakers due to its wide control range and high voltage stability.

- Direct control of the switching transistor
- Low start-up current
- Reversing linear overload characteristic
- Base current drive proportional to collector current

Description of function

This IC is designed for driving a bipolar power transistor and for performing all necessary control and protective functions in self-oscillating flyback converter power supplies. Owing to the IC's outstanding voltage stability, which is maintained even at major load fluctuations, the IC is suited for consumer as well as for industrial applications. The rectified line voltage is applied to the series connection of the power transistor and the primary winding of the flyback transformer. During the on-phase of the transistor, energy is stored in the primary winding and released to the consumer via the secondary winding.

The IC controls the power transistor in such a way that the secondary voltage is kept at a constant value independently of changes in the line voltage or load. The control information required is derived from the rectified line voltage during the on-phase as well as from a secondary winding during the off-phase.

Load differences are compensated by altering the frequency, line voltage fluctuations are additionally counteracted by changing the pulse duty factor. This results in the following load-dependent modes of the SMPS:

– Open-loop or small load:	Secondary voltage slightly above the desired value
– Control:	Load-independent secondary voltage
– Overload:	In case of a secondary overload or short circuit, the secondary voltage is decreased at the point of return as a function of the load current, following a reversing characteristic.

Description of use

A flyback converter designed for color TV sets, applicable between 30 W and 120 W and for line voltages ranging from 160 V to 270 V, is described on one of the following pages. On the subsequent pages the major pulses and diagrams can be found. The line voltage is rectified by bridge rectifier Gr1 and smoothed by C_3. During start-up the IC current is supplied via the combination Gr2+R_{11} while, in the post-transient condition, it is additionally supplied via winding 13/11 and rectifier Gr3. The size of filter capacitor C_9 determines the turn-on behavior.

Switching transistor T1 is a BU 208. Parallel capacitance C_{11} and primary winding 1/7 form a resonant circuit, thus limiting the frequency and amplitude of collector-emitter voltage overshoots upon turn-off of T1. R_{12}, Gr4, C_{10}, R_{15} and Dr2 are elements to improve the switching behavior of T1.

The inductance of the primary winding determines the current increase in T1. This sawtooth-shaped current rise is simulated at network R_5C_8 and applied to pin 4 of the IC. Depending of the dimensions of the primary inductance, timing element R_5C_8 is to be adapted to the current rise angle in T1. Thus, during the on-phase, the IC receives control information at pin 4 in the form of the simulated energy content of the primary winding as a function of the line voltage versus time.

Fluctuations at pin 3 are recognized by control winding 9/15. This measure requires fixed coupling to secondary winding 2/16. The control winding is also used for feedback and permits self-oscillating conditions in parallel circuit C_{11}/primary inductance if power transistor T1 is blocked. In this way the maximum open-loop frequency is determined.

The control voltage required at pin 3 is rectified by diode Gr5 and smoothed by capacitor C_6. Furthermore, resistor R_8 and C_6 form a timing element. Due to these circumstances, fast changes in the control voltage are filtered out, i.e. the controlling element does not respond until several periods have occured. The secondary voltage can be set by means of the voltage divider formed of resistors R_7, R_6, R_3 and R_2. Reason: in the IC the control voltage at pin 3 is compared with a stable, internal reference voltage.

According to the result of this comparison, frequency and pulse duty factor are corrected until the secondary voltage selected by R_7 has established itself.

In the case of overload or short circuit on the secondary side, only a small voltage portion is passed to control winding 9/15; the reference voltage at pin 1 becomes directly active at control input pin 3 and activates an overload amplifier (point of return), which drives power transistor T1 down to a smaller pulse duty factor. The line power output is reduced to 6 VA.

For all operating ranges of the SMPS, the zero passages of the voltage at the control winding contain information on pulse duty factor and switching frequency of switching transistor T1, or on the open-loop frequency. Conditioning of the corresponding signal at pin 2 is performed by series resistor R_4, and by integrated limiter diodes. Timing network R_8C_4 suppresses HF spikes at pin 2.

Before the line voltage drops below its minimum value, the SMPS must be switched off in order to obtain defined on/off conditions. Winding 11/13 is configured in such a way that the voltage at pin 9 changes linearly with the rectified line voltage. The IC goes into on-state if $V_9 \geq 12.3$ V, and into off-state if $V_9 \leq 5.7$ V. The drive of the power transistor will be blocked as soon as $V_9 \leq 6.7$ V.

Pin 5 is connected to pin 9 via resistor R_9, since the IC's output is not enabled until voltages $V_5 \geq 2.7$ V prevail.

On the secondary side start-up voltages from V_{1sec} to V_{4sec} are available. If switch S1 is put into open position, standby is set automatically, with a secondary effective power of approx. 3 W being tapped from winding 12/16. Resistors R_{13} and R_{14} form a basic load of voltages V_{1sec} and V_{2sec}. They contribute to maintaining standby conditions, i.e. V_{sec} rise $\leq$ 20%. Capacitors C_{12} through C_{15} prevent spikes caused by reversing rectifiers Gr6 and Gr9. The secondary voltages are smoothed by the charging electrolytic capacitors C_{16} through C_{19}. After the line voltage has been applied at time t_0, the following voltages start to increase:

- V_9 according to the half-cycle charge via R_{11}.
- V_4 to $V_{4\,max}$ (typ. 6.2 V)
- V_5 to the value determined by R_9

In this case the current consumption of the IC is smaller than 3.2 mA. If V_9 reaches the threshold 12.3 V, the IC will switch on the reference voltage of pin 1. The current consumption rises to typically 80 mA. The primary current voltage transformer adjusts V_4 down to $V_{REF/2}$ and the start pulse generator produces the start pulse. Feedback to pin 2 starts a subsequent pulse and so forth.

The width of all pulses, including the start pulse, is controlled by the control voltage at pin 3. During turn-on the control voltage corresponds to standby conditions, i.e. $V_3 = V_{REF/2} + 50$ mV. The IC begins with narrow pulses, which become wider depending on the feedback control voltage. Instantly, the IC operates in the control mode. The control loop is in a post-transient state. If, during start-up, voltage V_9 drops below the turn-off threshold $V_9 \leq 7.8$ V, the start-up phase will be terminated (pin 8 is switched to Low). Since the IC remains in the on-state, V_9 drops further to $V_9 \leq 5.7$ V. The IC switches to the off-state, V_9 is now able to rise again and a new start-up phase may begin. After the IC has been started, it will operate in the control mode. The voltage at pin 3 is typically $V_{REF/2} + 0.2$ V.

If the output is loaded, the control amplifier allows wider charge pulses to occur (V_8 = H). The peak value of the voltage at pin 4 rises to $V_4 = V_{REF}$. Upon an increase in the secondary load the overload amplifier begins adjusting the pulse width down. Since altering of the pulse width is reversed, this is referred to as the reverse point of the SMPS or point of return. In case of a short circuit on the secondary side, the overload amplifier will adjust the pulse width to typically 1.6 µs and reduces the pulse duty factor to <1:100. The SMPS decreases the line power consumption to typically 6 VA. A small pulse duty factor entails a drop in supply voltage V_9 below the threshold $V_9 \leq 6.7$ V causing a drive interrupt of the switching transistor and a continued drop of supply voltage V_9. If supply voltage $V_9 \leq 5.7$ V, the IC is turned off and enters into a new start-up phase.

This intermittent periodic duty operation is continued until the short circuit on the secondary side has been eliminated.

If the secondary side is unloaded (standby), the control pulse width becomes narrower. The frequency rises. During open-loop operation the approximate natural frequency of the system (75 kHz) is obtained; pulse duty factor 1:11. The rise of the secondary voltages is approx. 20%. If resistors R_{13}/R_{14} were absent, the IC would have to perform adjustment beyond the natural frequency of the system, with the zero passage identification only recognizing every 2nd, 3rd or 4th zero passage as a pulse start, i.e. the frequency would divide down to the 2nd, 3rd or 4th subharmonic. The pulse duty factor is thus diminished to 1:22, 1:33, or 1:44, respectively. The pulse width remains constant at approx. 1.2 µsec. A certain small pulse duty factor causes supply voltage V_9 to drop below the threshold voltage $V_9 \leq 6.7$ V. Then, the interrogation intermittent periodic duty operation begins as already described for the short circuit case. Constant open-loop operation will not continue until resistors R_{13}/R_{14} have been loaded.

Circuit description

Pin 1: Reference voltage output, overload-protected.
I_{1max} = 5 mA. All modules, excluding the IC's output stage, are supplied by the internal reference voltage.

Pin 2: The zero passage identification driving the control logic identifies the discharged status of the transformer at the zero passage of voltage V_2 from negative to positive values and enables the logic for pulse start, which is driven by trigger start.

Pin 3: The control voltage supplied to this pin is compared with two stable reference potentials in the control amplifier, in overload identification and during standby. The outputs of these stages operate onto the trigger hold, thus terminating the pulse.

Pin 4: A voltage proportional to the collector current of the switching transistor is generated on the basis of the external RC combination in conjunction with the collector current simulation block. This voltage introduces the beginning of a pulse at a stable voltage via trigger start and determines at a second stable voltage (reverse point) the absolute maximum pulse (with respect to time length) in trigger hold. At the same time the rise angle of the voltage proportional to the collector current of the switching transistor is impressed onto the base current amplifier, and, in accordance with the smallest current amplification B of the switching transistor to be expected, the base of the switching transistor is driven via pin 8.

Pin 5: If a voltage ≥ 2.7 V is applied, the control logic is enabled via the trigger. Pins 7/8 are driven by the coupling capacitor charge circuit and the base current. In case a voltage ≤ 1.8 V prevails, base current switch-off pin 7 is clamped at a voltage $V_7 \leq 1.3$ V; driving of the switching transistor is impossible. The IC will not be enabled again until the voltage at pin 9 has dropped below 5.7 V, the IC has been turned off and the SMPS has entered a new start-up phase.

Pin 6: GND

Pin 7/8: Via the voltage controller and the coupling capacitor charge circuit, the output stage of the IC is dc-adjusted to the switching transistor. The switching transistor is driven via a base current amplifier and pin 8, while it is blocked via the basic current switch-off and pin 7.

Pin 9: Current supply of the IC.

Maximum ratings

		min	max	
Supply voltage	V_9	0	20	V
Voltages				
Reference output	V_1	0	6	V
Identification input	V_2	−0.6	0.6	V
Control amplifier	V_3	0	3	V
Collector current simulation	V_4	0	8	V
Blocking input	V_5	0	8	V
Base current cut-off point	V_7	0	V_9	V
Base current amplifier output	V_8	0	V_9	V
Currents				
Feedback zero passage	$I_{i\,2}$	−5	5	mA
Control amplifier	$I_{i\,3}$	−3	3	mA
Collector current simulation	$I_{i\,4}$	0	5	mA
Base current cut-off point	$I_{q\,7}$	0	1.5	A
Base current amplifier output	$I_{q\,8}$	−1.5	0	A
Junction temperature	T_j		125	°C
Storage temperature range	T_{stg}	−40	125	°C
Thermal resistances				
junction-air	$R_{th\,JA}$		70	K/W
junction-case	$R_{th\,JC}$		15	K/W
Operating range				
Supply voltage	V_9	7.8	18	V
Case temperature	T_c	0	85	°C

Characteristics

$T_A = 25\,°C$; according to measurement circuit 1 and diagram

		min	typ	max	
Start operation					
Current consumption (V_1 not yet switched on)					
$V_9 = 2$ V	I_9			0.5	mA
$V_9 = 5$ V	I_9		1.5	2.0	mA
$V_9 = 10$ V	I_9		2.4	3.2	mA
Switching point for V_1	V_9	11.0	11.8	12.3	V
Normal operation					
$V_9 = 10$ V; $V_{cont} = -10$ V; $V_{clock} = \pm 0.5$ V; $f = 20$ kHz; pulse duty factor 1:2 after switch-on					
Current consumption					
$V_{cont} = -10$ V	I_9	110	135	160	mA
$V_{cont} = 0$ V	I_9	50	75	110	mA
Reference voltage					
$I_1 < 0.1$ mA	V_1	4.0	4.2	4.5	V
$I_1 = 5$ mA	V_1	4.0	4.2	4.4	V
Temperature coefficient of reference voltage	TC_1		10^{-3}		1/K
Control voltage $V_{cont} = 0$ V	V_3	2.3	2.6	2.9	V
Collector current simulation voltage					
$V_{cont} = 0$ V	V_4*)	1.8	2.2	2.5	V
$V_{cont} = 0$ V/−10 V	ΔV_4*)	0.3	0.4	0.5	V
Blocking input voltage	V_5	6.0	7.0	8.0	V
Output voltages					
$V_{cont} = 0$ V	V_{q7}*)	2.7	3.3	4.0	V
$V_{cont} = 0$ V	V_{q8}*)	2.7	3.4	4.0	V
$V_{cont} = 0$ V/−10 V	ΔV_{q8}*)	1.6	2.0	2.4	V
Feedback voltage	V_2		0.2		V
Protective operation					
$V_9 = 10$ V; $V_{cont} = -10$ V; $V_{clock} = \pm 0.5$ V; $f = 20$ kHz; pulse duty factor 1:2					
Current consumption					
$V_5 < 1.8$ V	I_9	14	22	28	mA
Turn-off voltage					
$V_5 < 1.8$ V	V_{q7}	1.3	1.5	1.8	V
Turn-off voltage					
$V_5 < 1.8$ V	V_4	1.8	2.1	2.5	V
External blocking input					
Enable voltage					
$V_{cont} = 0$ V	V_5		2.4	2.7	V
Blocking voltage					
$V_{cont} = 0$ V	V_5	1.8	2.2		V
Supply voltage blocked for V_8					
$V_{cont} = 0$ V	V_9	6.7	7.4	7.8	V
V_1 turned off (if V_9 is further decreased)	ΔV_9	0.3	0.6	1.0	V

*) DC component only

Characteristics

$T_A = 25\,°C$; according to measurement circuit 2

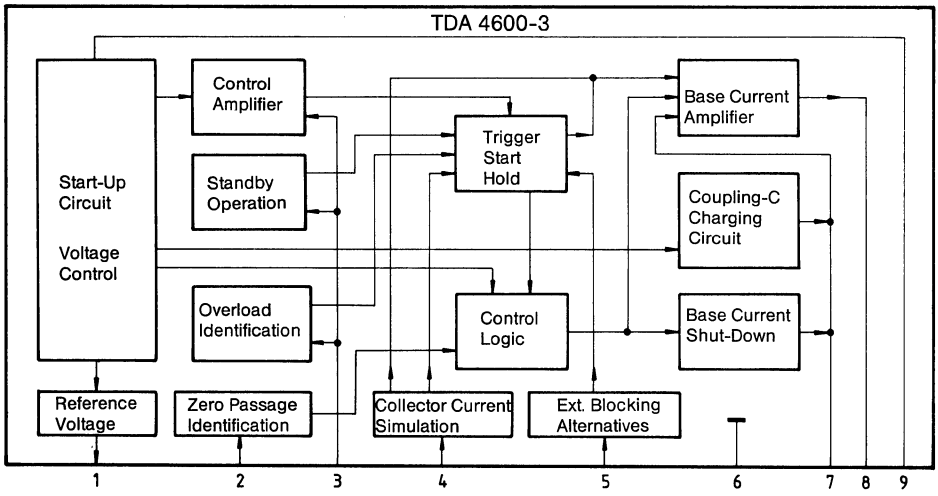
		Test conditions	min	typ	max	
Turn-on time (secondary voltage)	t_{on}			350	450	ms
Voltage change (S3 = closed)	$\Delta V_{2\,sec}$	$\Delta N_3 = 20$ W		100	500	mV
Sound output power (S2 = closed)	$\Delta V_{2\,sec}$	$\Delta N_2 = 15$ W		500	1000	mV
Standby operation (S1 = open)	$\Delta V_{2\,sec}$	Sec. useful load = 3W		20	30	V
	f		70	75		kHz
	$N_{primary}$			10	12	VA

Pin description

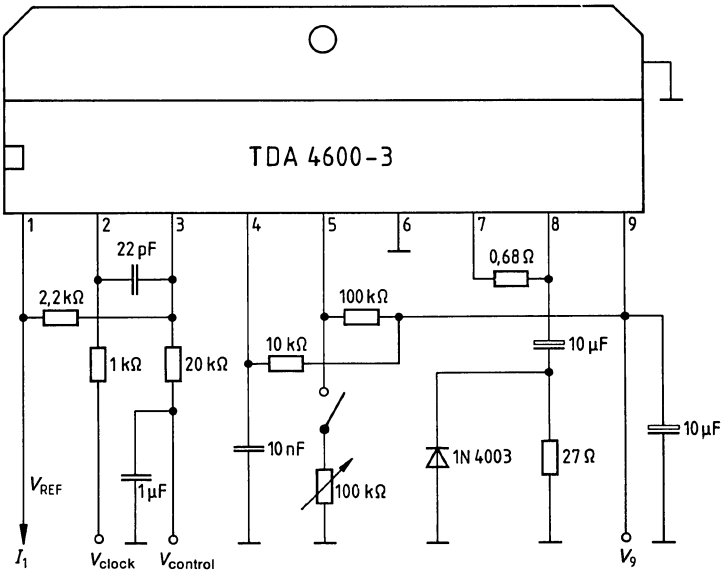
Pin	Designation	Function
1	V_{REF} output	The IC adjusts the secondary voltage of the SMPS to a multiple of the reference voltage V_{REF}.
2	Zero passage identification	Input for oscillator feedback. After build-up, each zero passage of the feedback voltage (rising edge) triggers an output pulse at pin 8. The trigger threshold is typically −30 mV.
3	Control amplifier and overload amplifier input	Information input for secondary voltage. The output pulse width at pin 8 is adapted to the load on the secondary side by comparing the control voltage gained from the control winding of the transformer to the reference voltage (normal, overload, short-circuit, open-loop operation).
4	Collector current simulation	Information input for primary voltage. The rise of the primary current in the primary winding is simulated as voltage increase at pin 4 by means of an external RC element. If a value derived from the control voltage at pin 3 is reached, the compensating pulse at pin 8 is terminated. The RC element serves for setting the maximum power at the point of return. In this point, the amplitude of the sawtooth-shaped voltage at pin 4 rises to the value of V_{REF}.

Pin	Designation	Function
5	Protective input	For response of the oscillator a voltage of at least 2.7 V must be applied at pin 5. In case of disturbance, an additional secondary pulse at pin 8 is prevented if the voltage drops below 1.8 V, which is the protective threshold value.
6	Ground	The capacitor at pin 4 is to be directly connected to pin 6. The primary current of the transformer is not to be routed through this connection.
7	DC voltage output for charging coupling capacitor	Current sink after an output pulse and charging source for the coupling capacitor before an output pulse.
8	Pulse output drive of switching transistor	Current source for output pulse. The output current is adjusted according to the voltage rise at pin 4 with the aid of the resistor between pins 7 and 8. Thus, oversaturation of the external power transistor is prevented.
9	Current supply	For start-up of the SMPS the following conditions must be met: — The reference voltage at pin 1 is turned off — Subsequently, at pin 9, a rise of the supply voltage up to a value exceeding 12.3 V — At pin 5 the voltage is above 2.7 V. During operation the supply voltage is monitored for undervoltage. For values below 6.7 V the output pulses at pin 8 are blocked and for values below 5.7 V the reference voltage is turned off as an additional measure. These are the preconditions for a new oscillator start-up.

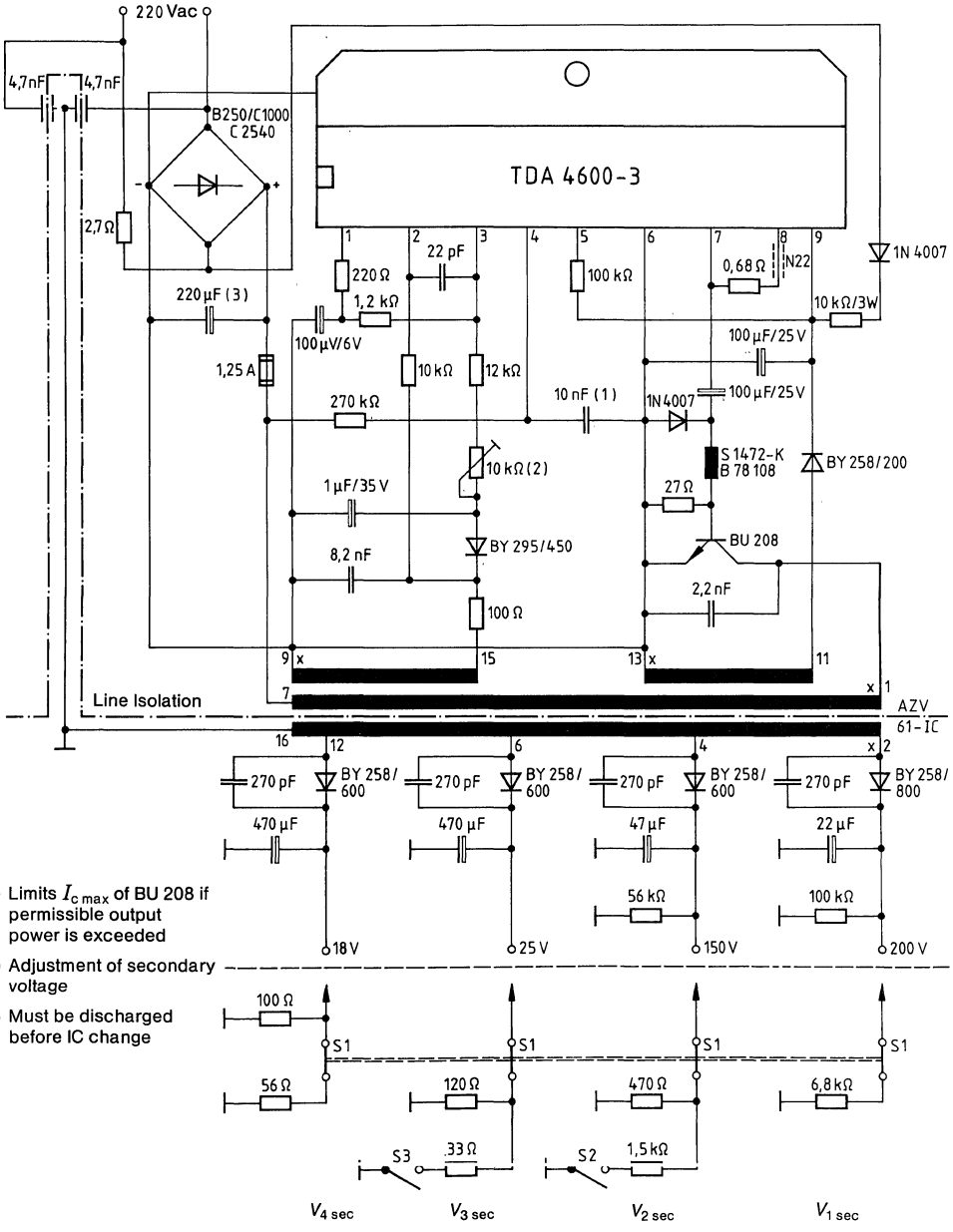
Block diagram



Measurement circuit 1



Measurement circuit 2

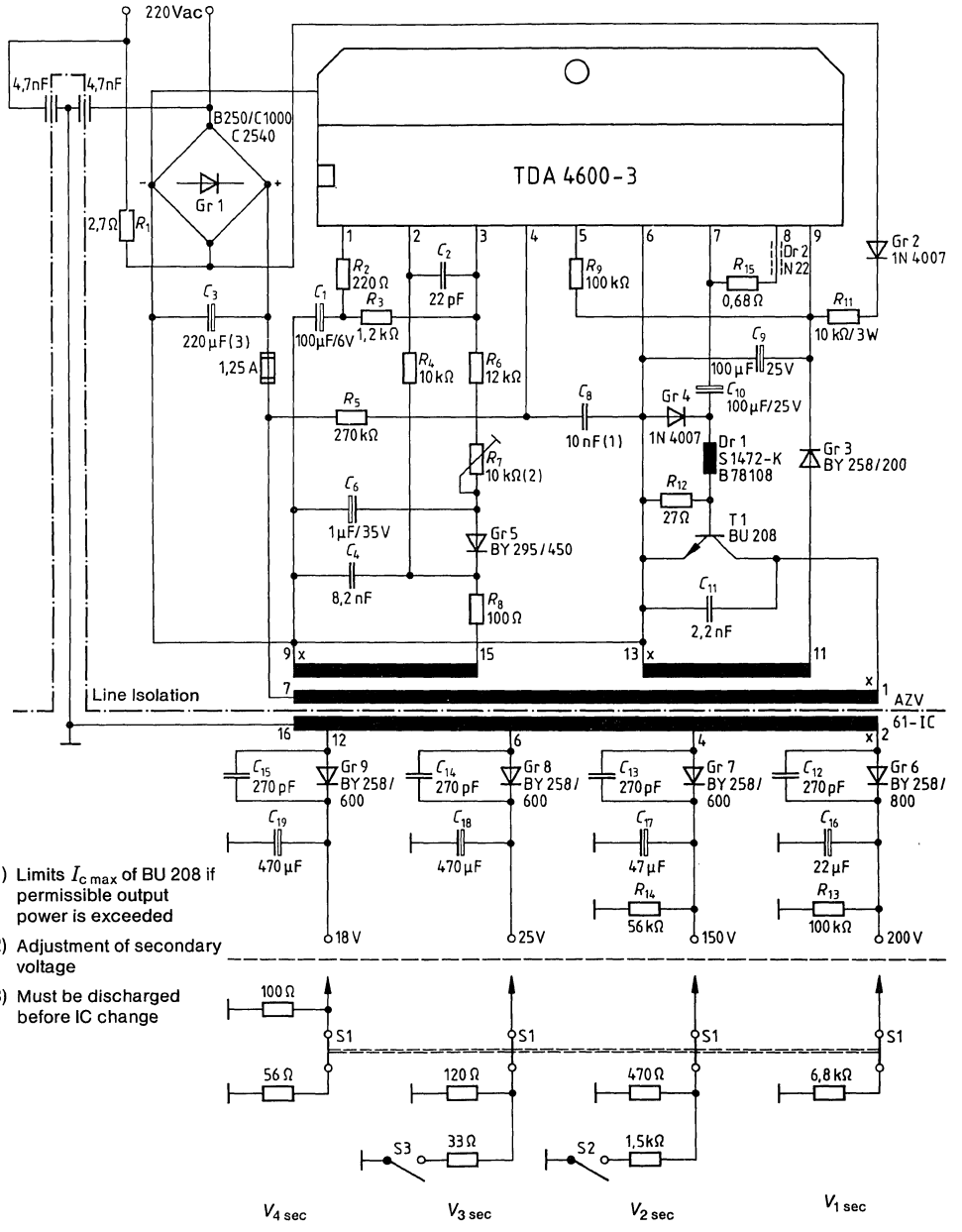


(1) Limits $I_{c\,max}$ of BU 208 if permissible output power is exceeded

(2) Adjustment of secondary voltage

(3) Must be discharged before IC change

Application circuit



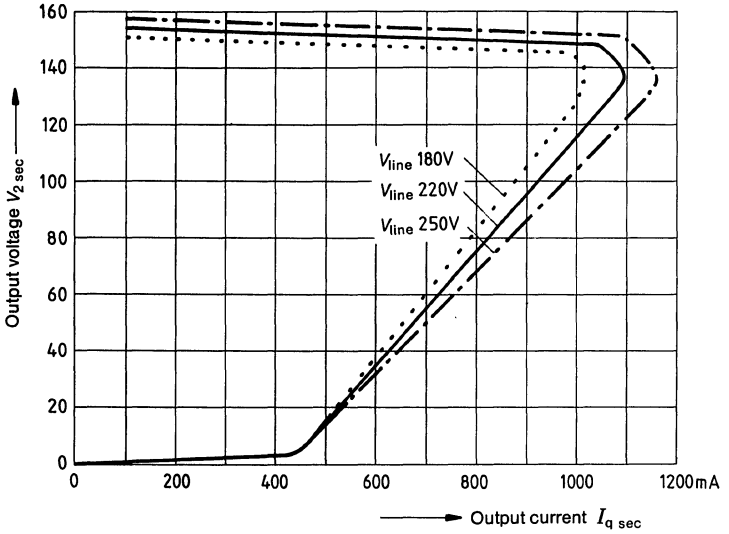
(1) Limits $I_{c\,max}$ of BU 208 if permissible output power is exceeded

(2) Adjustment of secondary voltage

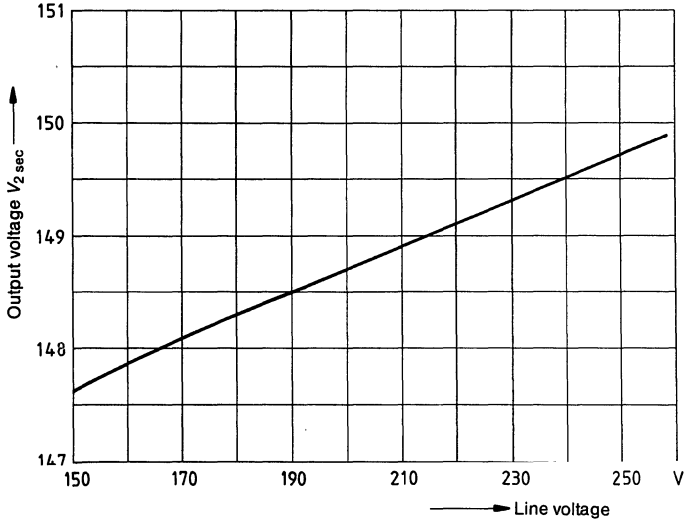
(3) Must be discharged before IC change

Supplements to test and measurement circuit 2

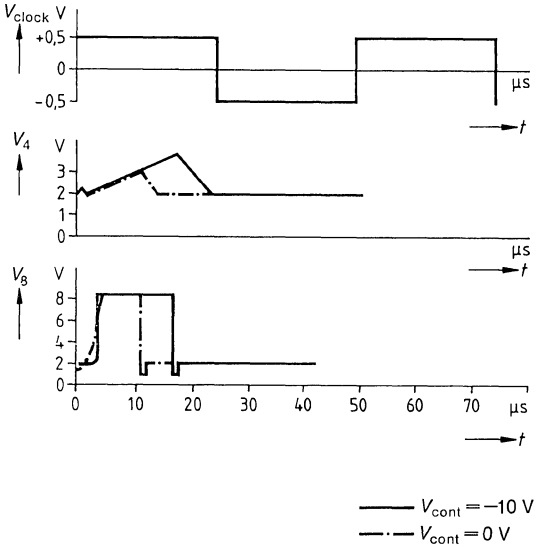
Load characteristic
Output voltage versus output current



Output voltage versus line voltage



Measurement diagram for overload operation, measurement circuit 1



SIP 9
DIP 18

The integrated circuit TDA 4601/D is designed for driving, controlling and protecting the switching transistor in self-oscillating flyback converter power supplies as well as for protecting the overall power supply unit. In case of disturbance, the rise of the secondary voltage is prevented. In addition to the IC's application range including TV receivers, video tape recorders, hifi devices and active loudspeakers, it can also be used in power supply units for professional applications due to its wide control range and high voltage stability during increased load changes.

Features

- Direct control of the switching transistor
- Low start-up current
- Reversing linear overload characteristic
- Base current drive proportional to collector current
- Protective circuit for case of disturbance

Maximum ratings

		min	max	
Supply voltage	V_9	0	20	V
Voltages				
Reference output	V_1	0	6	V
Zero passage identification	V_2	−0.6	0.6	V
Control amplifier	V_3	0	3	V
Collector current simulation	V_4	0	8	V
Blocking input	V_5	0	8	V
Base current cut-off point	V_7	0	V_9	V
Base current amplifier output	V_8	0	V_9	V
Currents				
Zero passage identification	I_{i2}	−5	5	mA
Control amplifier	I_{i3}	−3	3	mA
Collector current simulation	I_{i4}	0	5	mA
Blocking input	I_{i5}	0	5	mA
Base current cut-off point	I_{q7}	−1	1.5	A
Base current amplifier output	I_{q8}	−1.5	0	A
Junction temperature	T_j		125	°C
Storage temperature range	T_{stg}	−40	125	°C
Thermal resistances:				
system-air TDA 4601	R_{thSA}	70		K/W
system-case TDA 4601	R_{thSC}	15		K/W
system-air[1] TDA 4601 D	R_{thSA}	60		K/W
system-air[2] TDA 4601 D	R_{thSA1}	44		K/W
Operating range				
Supply voltage	V_9	7.8 to 18		V
Case temperature TDA 4601	T_C	0 to 85		°C
Ambient temperature range[3] TDA 4601 D	T_A	0 to 70		°C

[1] Case soldered on PC board without cooling surface
[2] Case soldered on PC board with copper-clad 35 µm layer, cooling surface 25 cm²
[3] $R_{thSA1} = 44$ K/W and $P_V = 1$ W

Characteristics

$T_A = 25\,°C$
according to measurement circuit 1 and diagram

		min	typ	max	
Start operation					
Current consumption (V_1 not yet switched on)					
$V_9 = 2$ V	I_9			0.5	mA
$V_9 = 5$ V	I_9		1.5	2.0	mA
$V_9 = 10$ V	I_9		2.4	3.2	mA
Switching point for V_1	V_9	11.0	11.8	12.3	V
Normal operation					
$V_9 = 10$ V; $V_{cont} = -10$ V; $V_{clock} = \pm 0.5$ V; $f = 20$ kHz; duty cycle 1 : 2 after switch-on					
Current consumption					
$V_{cont} = -10$ V	I_9	110	135	160	mA
$V_{cont} = 0$ V	I_9	50	75	100	mA
Reference voltage					
$I_1 < 0.1$ mA	V_1	4.0	4.2	4.5	V
$I_1 = 5$ mA	V_1	4.0	4.2	4.4	V
Temperature coefficient of reference voltage	TC_1		10^{-3}		1/K
Control voltage $V_{cont} = 0$ V	V_3	2.3	2.6	2.9	V
Collector current simulation voltage					
$V_{cont} = 0$ V	V_4*)	1.8	2.2	2.5	V
$V_{cont} = 0$ V/−10 V	ΔV_4*)	0.3	0.4	0.5	V
Clamping voltage	V_5	6.0	7.0	8.0	V
Output voltages					
$V_{cont} = 0$ V	V_{q7}*)	2.7	3.3	4.0	V
$V_{cont} = 0$ V	V_{q8}*)	2.7	3.4	4.0	V
$V_{cont} = 0$ V/−10 V	ΔV_{q8}	1.6	2.0	2.4	V
Feedback voltage	V_2*)		0.2		V
Protective operation					
$V_9 = 10$ V; $V_{cont} = -10$ V; $V_{clock} = \pm 0.5$ V; $f = 20$ kHz; duty cycle 1 : 2					
Current consumption					
$V_5 < 1.9$ V	I_9	14	22	28	mA
Switch -off voltage					
$V_5 < 1.9$ V	V_{q7}	1.3	1.5	1.8	V
Switch-off voltage					
$V_5 < 1.9$ V	V_4	1.8	2.1	2.5	V
Blocking input					
Blocking voltage					
$V_{cont} = 0$ V	V_5	$\frac{V_1}{2} - 0.1$	$\frac{V_1}{2}$		V
Supply voltage blocked for V_8	V_9	6.7	7.4	7.8	V
$V_{cont} = 0$ V					
V_1 off (with further reduction of V_9)	ΔV_9	0.3	0.6	1.0	V

*) DC component only

Characteristics

$T_A = 25\,°C$; according to measurement circuit 2

		min	typ	max	
Switching time (secondary voltage)	t_{on}		350	450	ms
Voltage variation S3 = closed $\Delta N_3 = 20$ W	ΔV_{2sec}		100	500	mV
Voltage deviation S2 = closed $\Delta N_2 = 15$ W	ΔV_{2sec}		500	1000	mV
Standby operation S_1 = open secondary useful load = 3 W	ΔV_{2sec}		20	30	V
	f	70	75		kHz
	$N_{primary}$		10	12	VA

The cooling conditions have to be optimized with regard to maximum ratings (T_A; T_j; R_{thJC}; R_{thSA}).

Circuit description

The TDA 4601 is designed for driving, controlling and protecting the switching transistor in flyback converter power supplies during start-up, normal and overload operations as well as during disturbed operation. In case of disturbance the drive of the switching transistor is inhibited and a secondary voltage rise is prevented.

I. Start-up

The start-up procedures (on-mode) include three consecutive operating phases as follows:

1. **Build-up of internal reference voltage**
   The internal reference voltage supplies the voltage regulator and effects charging of the coupling electrolytic capacitor connected to the switching transistor. Current consumption will remain at $I_9 < 3.2$ mA with a supply voltage up to V_9 approx. 12 V.
2. **Enabling of internal voltage – reference voltage $V_1 = 4$ V**
   Simultaneously with V_9 reaching approx. 12 V, an internal voltage becomes available, providing all component elements, with the exception of the control logic, with a thermally stable and overload-resistant current supply.
3. **Enabling of control logic**
   In conjunction with the generation of the reference voltage, the current supply for the control logic is activated by means of an additional stabilization circuit. The integrated circuit is then ready for operation.

The above described start-up phases are necessary for ensuring the charging of the coupling electrolytic capacitor, which in turn supplies the switching transistor. Only then is it possible to ensure that the transistor switches accurately.

II. **Normal operating mode/control operating mode**

At the input of pin 2 the zero passages of the frequency provided by the feedback coil are registered and forwarded to the control logic. Pin 3 (control input, overload and standby identification) receives the rectified amplitude fluctuations of the feedback coil. The control amplifier operates with an input voltage of approx. 2 V and a current of approx. 1.4 mA. Depending on the internal voltage reference, the overload identification limits in conjunction with collector current simulator pin 4 the operating range of the control amplifier. The collector current is simulated by an external RC combination present at pin 4 and internally set threshold voltages. The largest possible collector current applicable with the switching transistor (point of return) increases in proportion to the increased capacitance (10 nF). Thus the required operating range of the control amplifier is established. The range of control lies between a dc voltage clamped at 2 V and a sawtooth-shaped rising ac voltage, which can vary up to a max. amplitude of 4 V (reference voltage). During secondary load reduction to approx. 20 W, the switching frequency is increased (approx. 50 kHz) at an almost constant pulse duty factor (1:3). During additional secondary load decreases to approx. 1 W, the switching frequency increases to approx. 70 kHz and pulse duty factor to approx. 1:11. At the same time collector peak current is reduced to < 1 A.

The output levels of the control amplifier as well as those of the overload identification and collector current simulator are compared in the trigger and forwarded to the control logic. Via pin 5 it is possible to externally inhibit the operations of the IC. The output at pin 8 will be inhibited when voltages of $\leq \frac{V_{REF}}{2} - 0.1$ V are present at pin 5.

Flipflops for controlling the base current amplifier and the base current shut-down are set in the control logic depending on the start-up circuit, the zero passage identification as well as on the enabling by the trigger. The base current amplifier forwards the sawtooth-spahed V_4 voltage to the output of pin 8. A current feedback with an external resistor ($R = 0.68\ \Omega$) is present between pin 8 and pin 7. The applied value of the resistor determines the max. amplitude of the base driving current for the switching transistor.

III. **Protective operating mode**

The base current shut-down activated by the control logic clamps the output of pin 7 to 1.6 V. As a result, the drive of the switching transistor is inhibited. This protective measure is enabled if the supply voltage at pin 9 reaches a value ≤ 6.7 V or if voltages of $\frac{V_{REF}}{2} - 0.1$ V are present at pin 5.

In case of short-circuits occurring in the secondary windings of the switched-mode power supply, the integrated circuit continuously monitors the fault conditions. During secondary, completely load-free operation only a small pulse duty factor is set. As a result the total power consumption of the power supply is held at $N = 6...10$ W during both operating modes. After the output has been inhibited for a voltage supply of ≤ 6.7 V, the reference voltage (4 V) is switched off if the voltage supply is further reduced by $\Delta V_9 = 0.6$ V.

Protective operating mode at pin 5 in case of disturbance

The protection against disturbances such as primary undervoltages and/or secondary overvoltages (e.g. by changes in the component parameters for the switched-mode power supply) is realized as follows:

● **Protective operating mode with continuous fault condition monitoring**

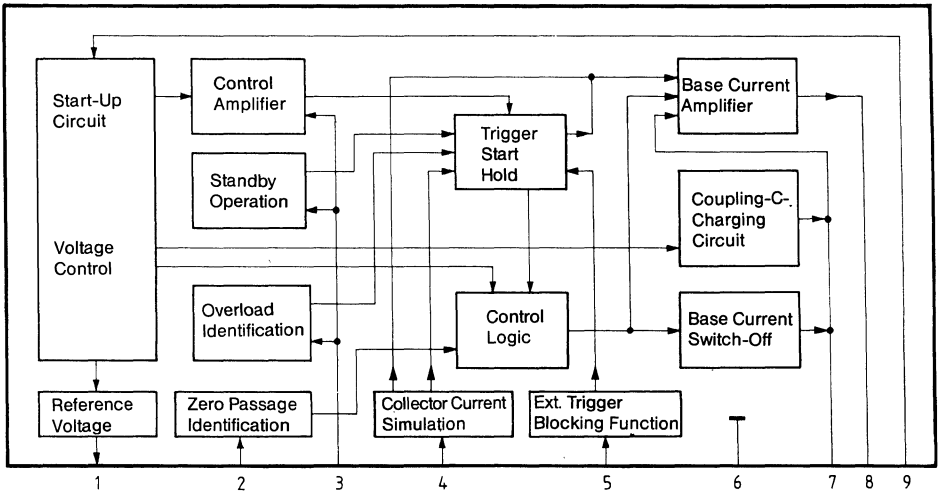
In case of disturbance the output pulses at pin 8 are inhibited by falling below the protective threshold V_5, with a typical value of $V_1/2$. As a result current consumption is reduced ($I_9 \geq 14$ mA at $V_9 = 10$ V).

With a corresponding **high-impedance** start-up resistor*), supply voltage V_9 will fall below the minimum shut-down threshold (5.7 V) for reference voltage V_1. V_1 will be switched off and current consumption is further reduced to $I_9 \leq 3.2$ mA at $V_9 \leq 10$ V.

Because of these reductions in current consumption, the supply voltage can rise again to reach the switch-on threshold of $V_9 \geq 12.3$ V. The protective threshold at pin 5 (is released and the power supply is again ready for operation.

In case of continuing problems of disturbance ($V_5 \leq V_1/2 - 0.1$ V) the switch-on mode is interrupted by the periodic protective operating mode described above, i.e. pin 8 is inhibited and V_9 is falling, etc.

Block diagram



*) in application circuit 1 10 kΩ/3W

IV. Switch-on in the wide range power supply (90 Vac to 270 Vac)
(application circuit 2)

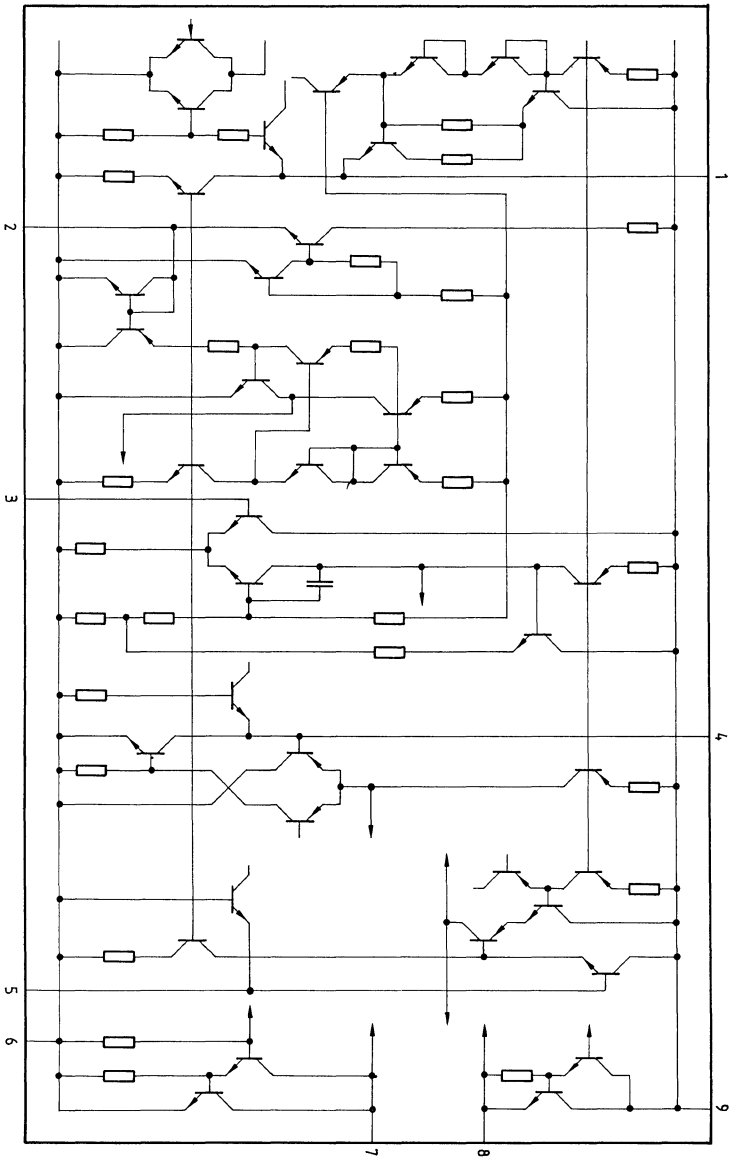
Self-oscillating flyback-converters designed as wide range power supplies require a power source independent of the rectified line voltage for TDA 4601. Therefore the winding polarity of winding 11/13 corresponds to the secondary side of the flyback converter transformer. Start-up is not as smooth as with an immediately available supply voltage, because TDA 4601 has to be supplied by the start-up circuit until the entire secondary load has been charged. This leads to long switch-on times, especially if low line voltages are applied.

However, the switch-on time can be shortened by applying the special start-up circuit (dotted line). The uncontrolled phase of feedback control winding 15/9 is used for activating purposes. Subsequent to activation, the transistor T1 begins to block when winding 11/13 generates the current supply for TDA 4601. Therefore, the control circuit cannot be influenced during operation.

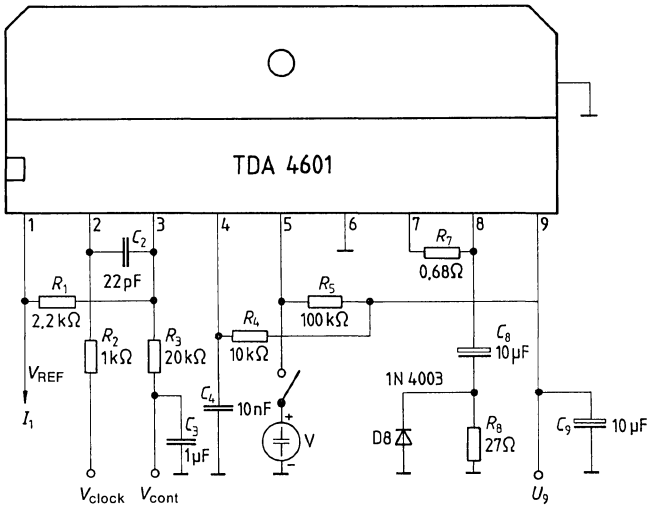
Pin description

Pin	Function
1	V_{REF} output
2	Zero passage identification
3	Input control amplifier, overload amplifier
4	Collector current simulation
5	Connection for additional protective circuit
6	Ground (rigidly connected to substrate mounting plate)
7	DC outupt for charging coupling capacitor
8	Pulse output—driving of switching transistor
9	Supply voltage
10-18	Ground (TDA 4601 D only)

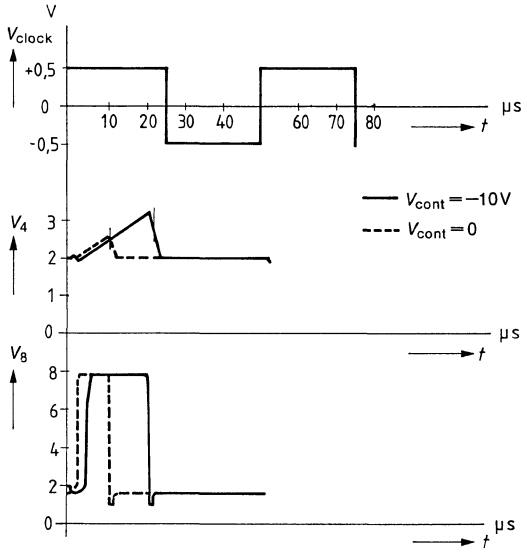
Circuit diagram



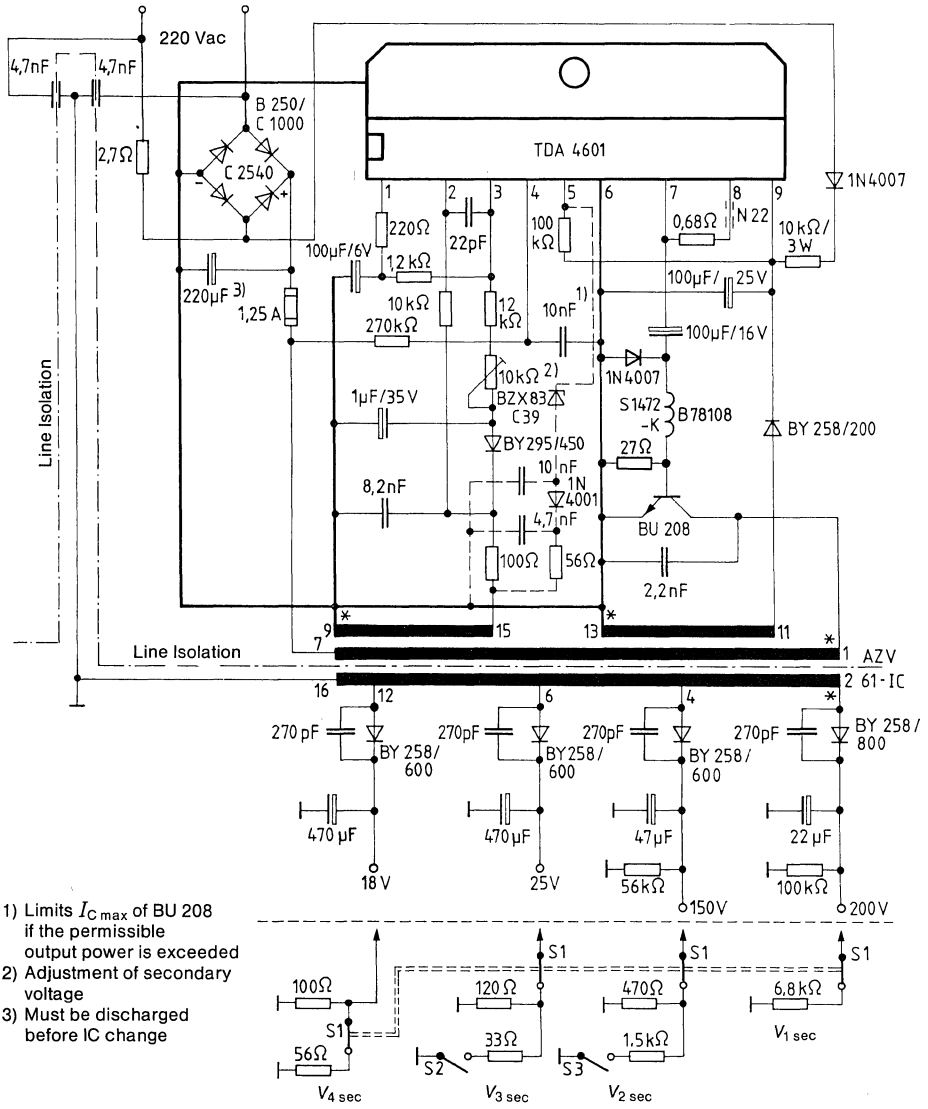
Test and measurement circuit 1



Test diagram: overload operation



Test and measurement circuit 2



1) Limits $I_{C\,max}$ of BU 208 if the permissible output power is exceeded
2) Adjustment of secondary voltage
3) Must be discharged before IC change

– – – Protective circuit against rise of secondary voltage in case of disturbance

Notes on application circuit 1

Protective circuit against secondary voltage rise even in case of disturbance

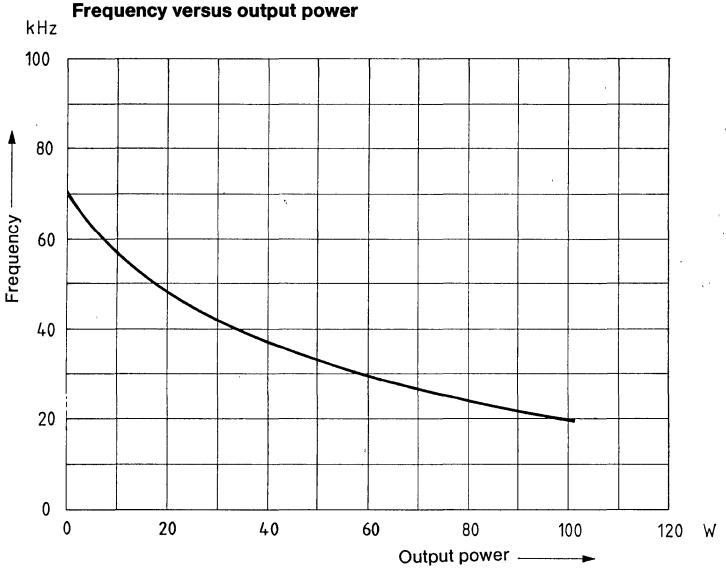
During standby this circuit type is necessary only under certain conditions. If switch S1 is open and the secondary side is loaded with no more than 1 to 5 W, a secondary voltage overshoot of approx. 20% will occur.

In case of disturbance (e.g. if the potentiometer is loosely contacted resulting in 10 kΩ (2), if the capacitor exhibits a 1 µF loss in capacitance, or if the 2 kΩ resistor increases to a high-impedance value of 32 kΩ), the protective effect of the standard turn-off is not active before the point of return has been reached. The result is that during disturbance energy is pumped into the secondary side, which will not ease off before reaching the point of return and, in the worst case, entails an instantaneous doubling of the voltage to 300 V (endangering the secondary electrolytic capacitors).

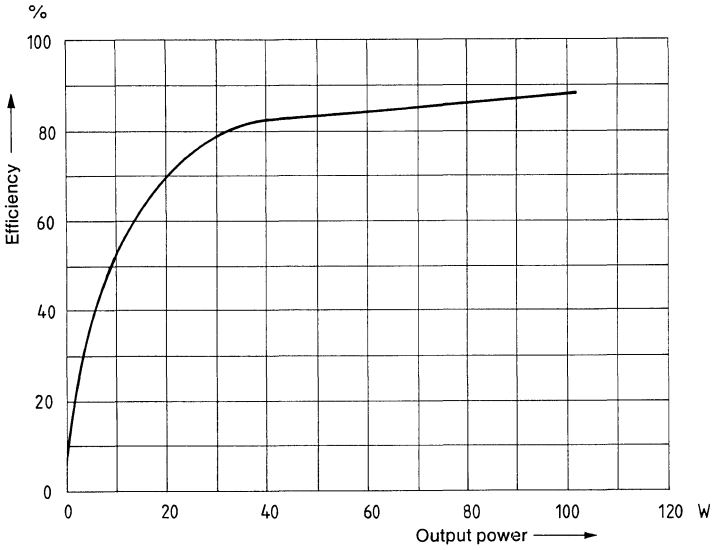
This additional protective circuit, which identifies the energy surge as voltage overshoot, is directly active at control winding 9/15. Through the 56 Ω resistor and the 1N4001 rectifier the negative portion is deducted and stored in the 10 µF capacitor. If the amplitude exceeds the voltage of Z-diode BZX 83/39, pin 5 is drawn below the turn-off threshold, inhibiting further control pulses at pin 8. During disturbance conditions the voltage overshoot on the secondary side will assume maximum values of approx. 30%.

Supplements to test and measurement circuit 2

Frequency versus output power

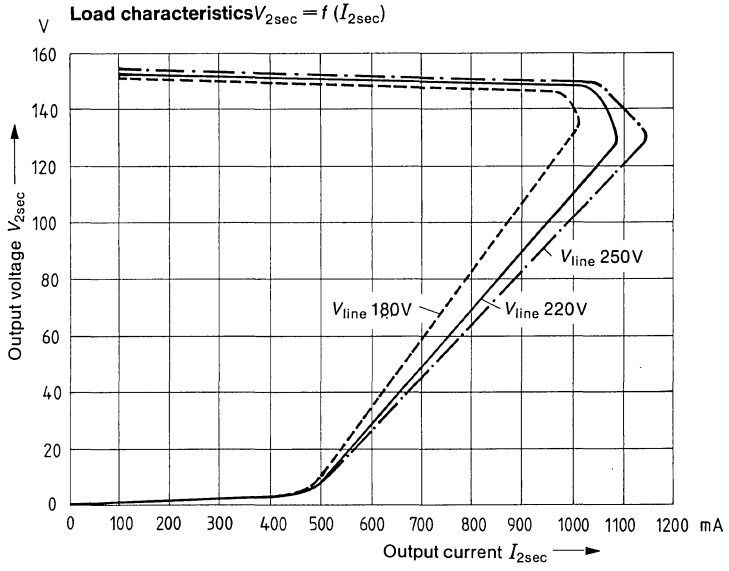


Efficiency versus output power

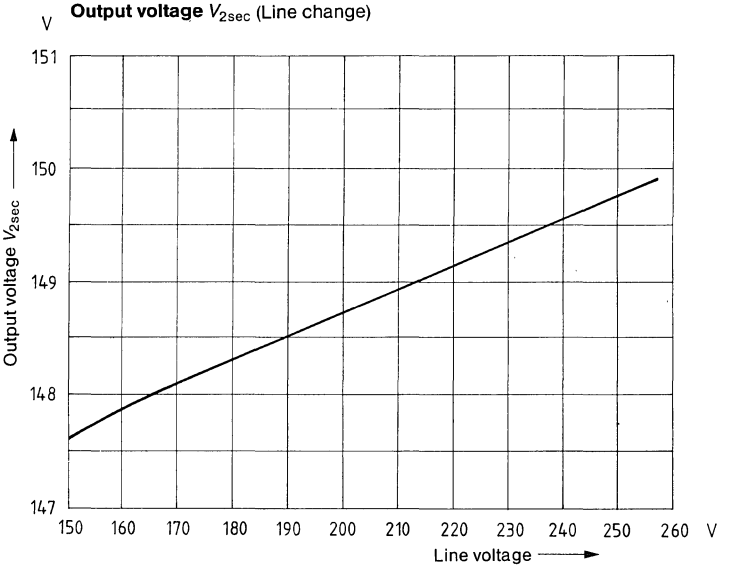


Supplements to test and measurement circuit 2

Load characteristics $V_{2sec} = f(I_{2sec})$

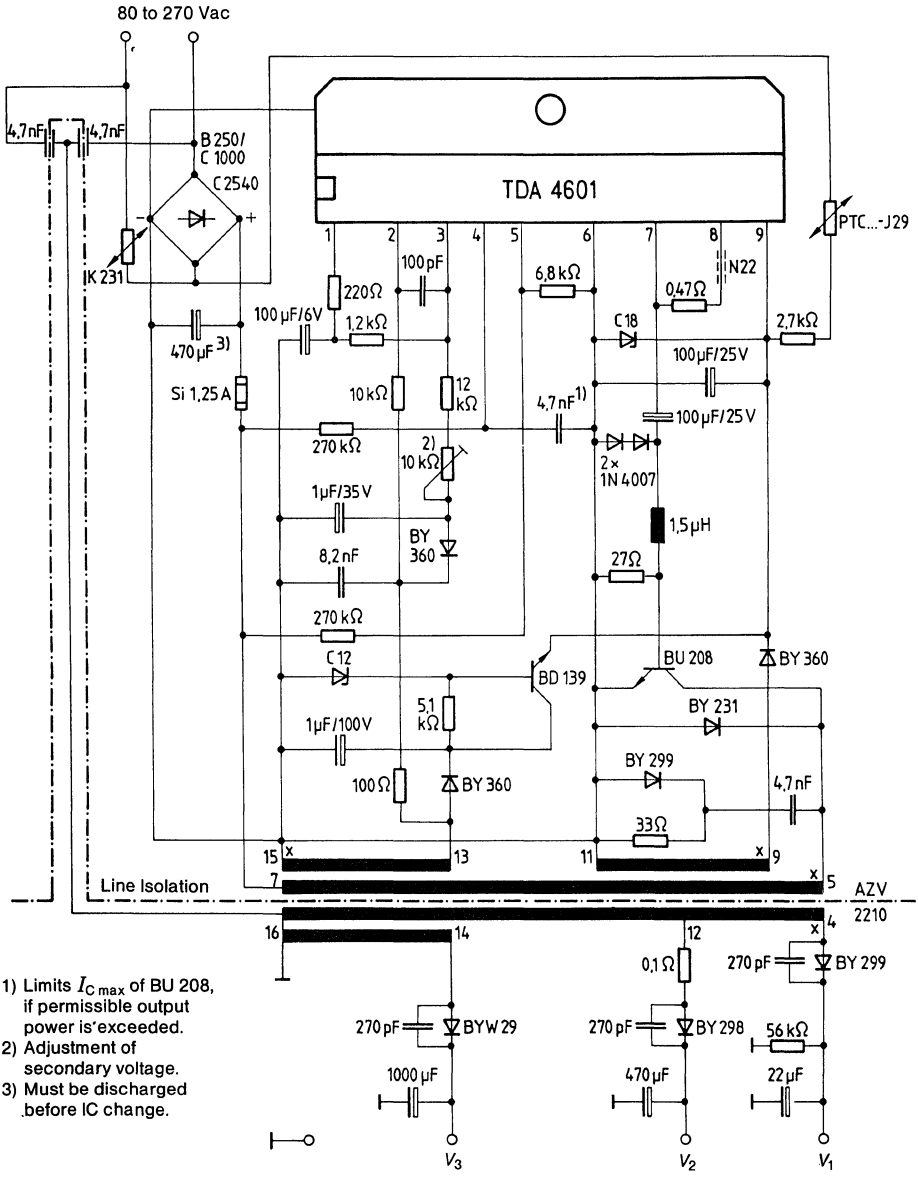


Output voltage V_{2sec} (Line change)



Application circuit 2

Wide range from 80 to 270 Vac



1) Limits $I_{C\,max}$ of BU 208, if permissible output power is exceeded.
2) Adjustment of secondary voltage.
3) Must be discharged before IC change.

Notes on application circuit 2

Wide range SMPS

Filtering of the rectified ac voltage has been increased up to 470 µF to ensure a constant and hum-free supply at V_{line} = 80 Vac. The stabilized phase is tapped for supplying the IC. In order to ensure good start-up conditions for the SMPS in the low voltage range, the non-stabilized phase of winding 13/15 is used as a starting aid (BD 139), which is turned off after start-up by means of Z diode C12.

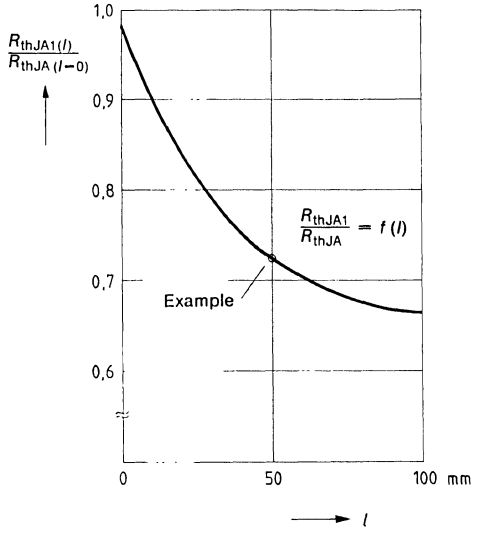
In comparison to the 220 Vac standard circuit, however, the collector-emitter circuit had to be altered to improve the switching behavior of BU 208 for the entire voltage range (80 to 270 Vac.) Diode BY 231 is necessary to prevent inverse operation of BU 208 and may be integrated for switching times with a secondary power < 75 W (BU 208 D).

Compared to the IC TDA 4600-2, the TDA 4601 has been improved in turn-off during undervoltage at pin 5. The TDA 4601 is additionally provided with a differential amplifier input at pin 5 enabling precise turn-off at the output of pin 8 accompanied by hysteresis. For wide range SMPS, TDA 4601 is recommendable instead of TDA 4600-2. If a constant quality standard like that of the standard circuit is to be maintained, wide range SMPS (80 to 270 Vac) with secondary power of 120 W can only be implemented at the expense of time.

Thermal resistance

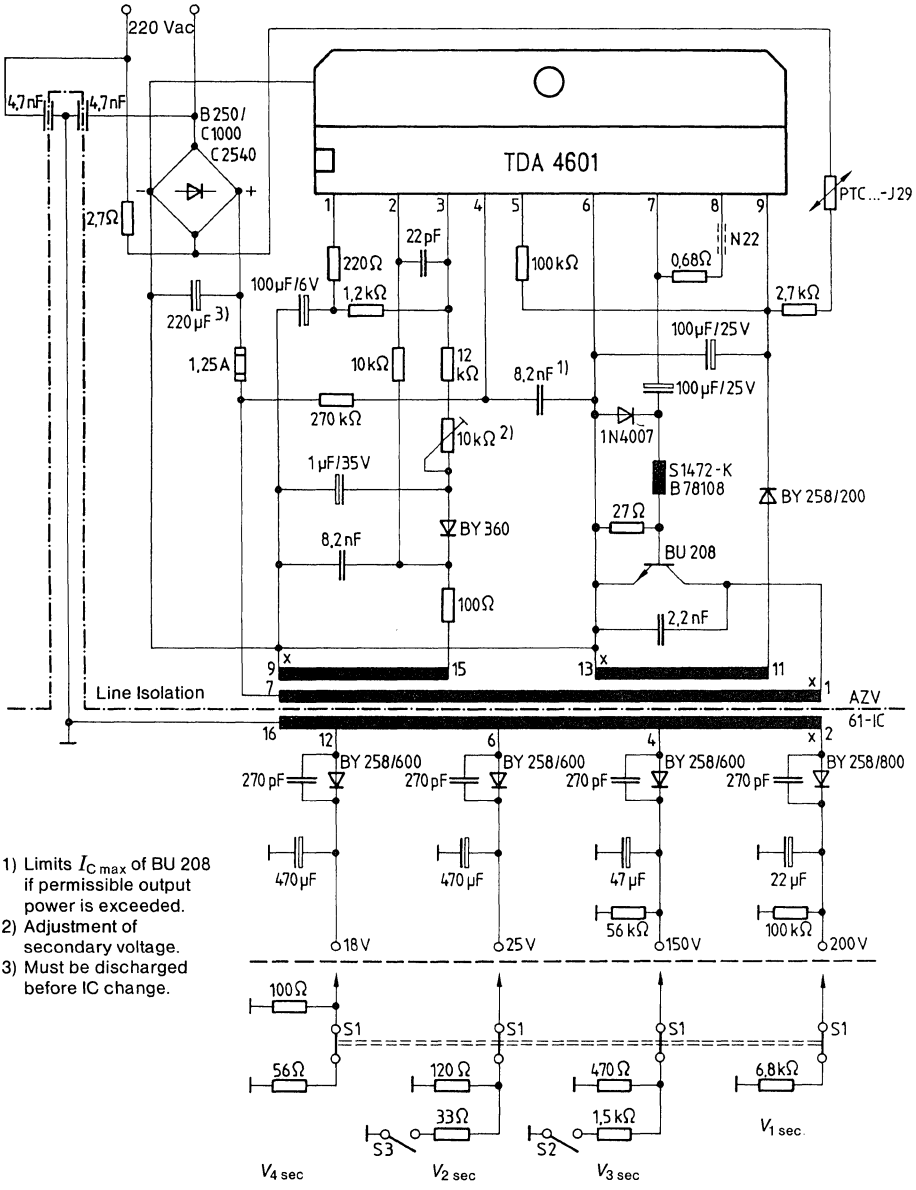
Standardized, ambient-related thermal resistance R_{thJA1} versus lateral length l of a square copper-clad cooling area (35 µm copper cladding)

R_{thJA} (l = 0) = 60 K/W
T_A = 70 °C
P_d = 1 W
PC board in vertical position
Circuit in vertical position
Still air



Further application circuits

Application circuit 3



1) Limits $I_{C\,max}$ of BU 208 if permissible output power is exceeded.
2) Adjustment of secondary voltage.
3) Must be discharged before IC change.

Notes on application circuit 3

Fully insulated, clamp-contacted PTC thermistor suitable for SMPS applications at increased start-up currents

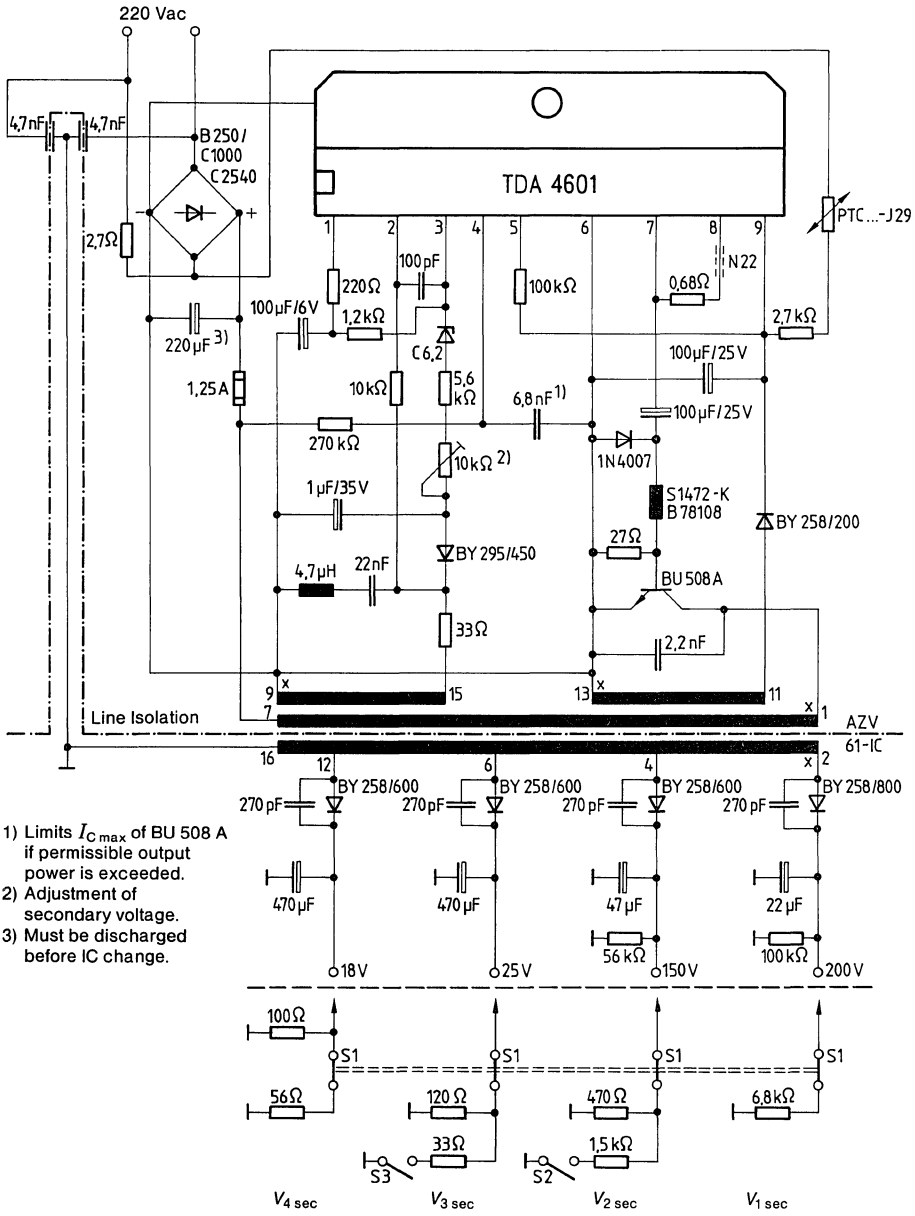
The newly developed PTC thermistor **Q63100-P2462-J29** is designed for applications in SMPS as well as in various other electronic circuits, which, for example, receive the supply voltage directly from the rectified line voltage and require an increased current during turn-on. Used in the flyback converter power supply of TV sets, an application proved millions of times over, the new PTC thermistor in the auxiliary circuit branch has resulted in a power saving of no less than 2 W. This increase in efficiency has a highly favorable effect on the standby operation of TV sets.

The required turn-on current needs only 6 to 8 s until the operating temperature of the PTC thermistor is reached. Low thermal capacitance of the PTC thermistor allows the circuit to be operated again after no more than 2 s. Another positive feature is the improved short-circuit strength. The clamp contacts permit more or less unlimited switching operations and thus guarantee high reliability. A flame-retardant plastic package and small dimensions are additional advantages of this newly developed PTC thermistor.

Technical data

Breakdown voltage at $T_A = 60\,°C$	$V_{BD\,rms}$	350	V
Resistance at $T_A = 25\,°C$	R_{25}	5	kΩ
Resistance tolerance	ΔR_{25}	25	%
Trip current (typ.)	I_K	20	mA
Residual current at $V_{A\,max}$	I_R	2	mA
Max. application voltage	$V_{op\,max\,rms}$	265	V
Reference temperature (typ)	T_{ref}	190	°C
Temperature coefficient (typ)	TC	26	%/K
Max. operating current	I_{max}	0.1	A
Storage temperature range	T_{stg}	−25 to 125	°C

Application circuit 4



1) Limits $I_{C\,max}$ of BU 508 A if permissible output power is exceeded.
2) Adjustment of secondary voltage.
3) Must be discharged before IC change.

Notes on application circuit 4

Improved load control and short-circuit characteristics

Turn-on is the same as for circuit 3.

To make the price more attractive, switching transistor BU 508A was selected.

To ensure optimum standby conditions, the capacitance between pins 2 and 3 was increased to 100 pF.

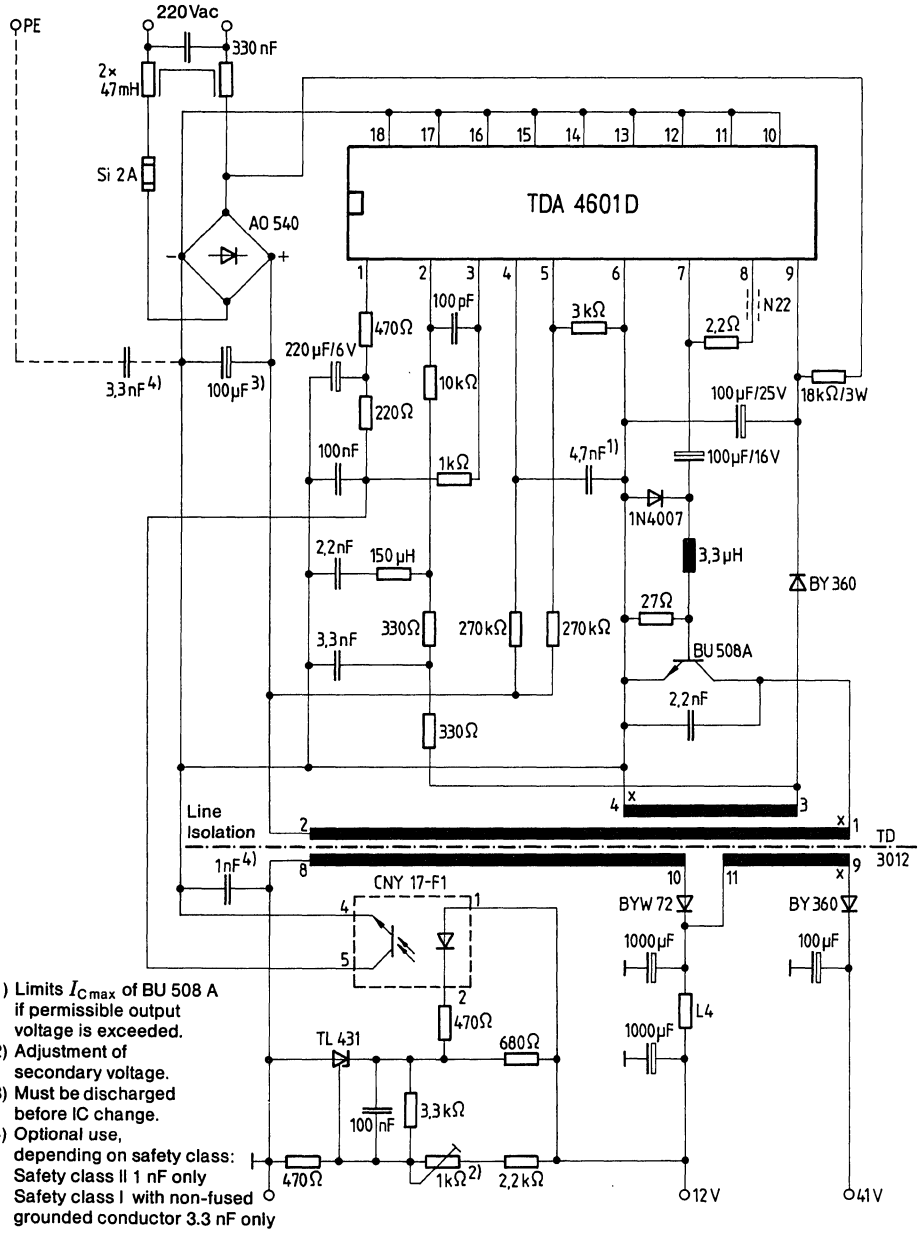
Z diode C6.2 transfers control voltage ΔV_{cont} directly to pin 3 resulting in improved load control.

Design and coupling conditions of various flyback transformers were sometimes a reason for overshoot spectra, which, despite the RC attenuating element 33 Ω x 22 nF and the 10 kΩ resistor, even penetrated across the feedback winding 9/15 to the zero passage indicator input (pin 2) and activated double and multiple pulses in the IC. Double and multiple pulses, however, lead to magnetic saturation in the flyback transformer and thus increase the risk of damaging the switched-mode power supply.

The larger the quantities of power to be passed, the more easily overshoots are generated. This can be observed around the point of return. The switched-mode power supply, however, reduces its own power to a minimum for all cases of overload or short-circuit. A series resonant circuit, whose resonance corresponds to the transformer's self-oscillation, was created through combination of the 4.7 µH inductance and the 22 nF capacitance. This resonant circuit short-circuits overshoots via a 33 Ω resistor.

$$\left(f = \frac{1}{2\pi\sqrt{LC}} \text{approx. 500 kHz}\right)$$

Application circuit 5



1) Limits $I_{C\,max}$ of BU 508 A if permissible output voltage is exceeded.
2) Adjustment of secondary voltage.
3) Must be discharged before IC change.
4) Optional use, depending on safety class: Safety class II 1 nF only Safety class I with non-fused grounded conductor 3.3 nF only

Notes on application circuit 5

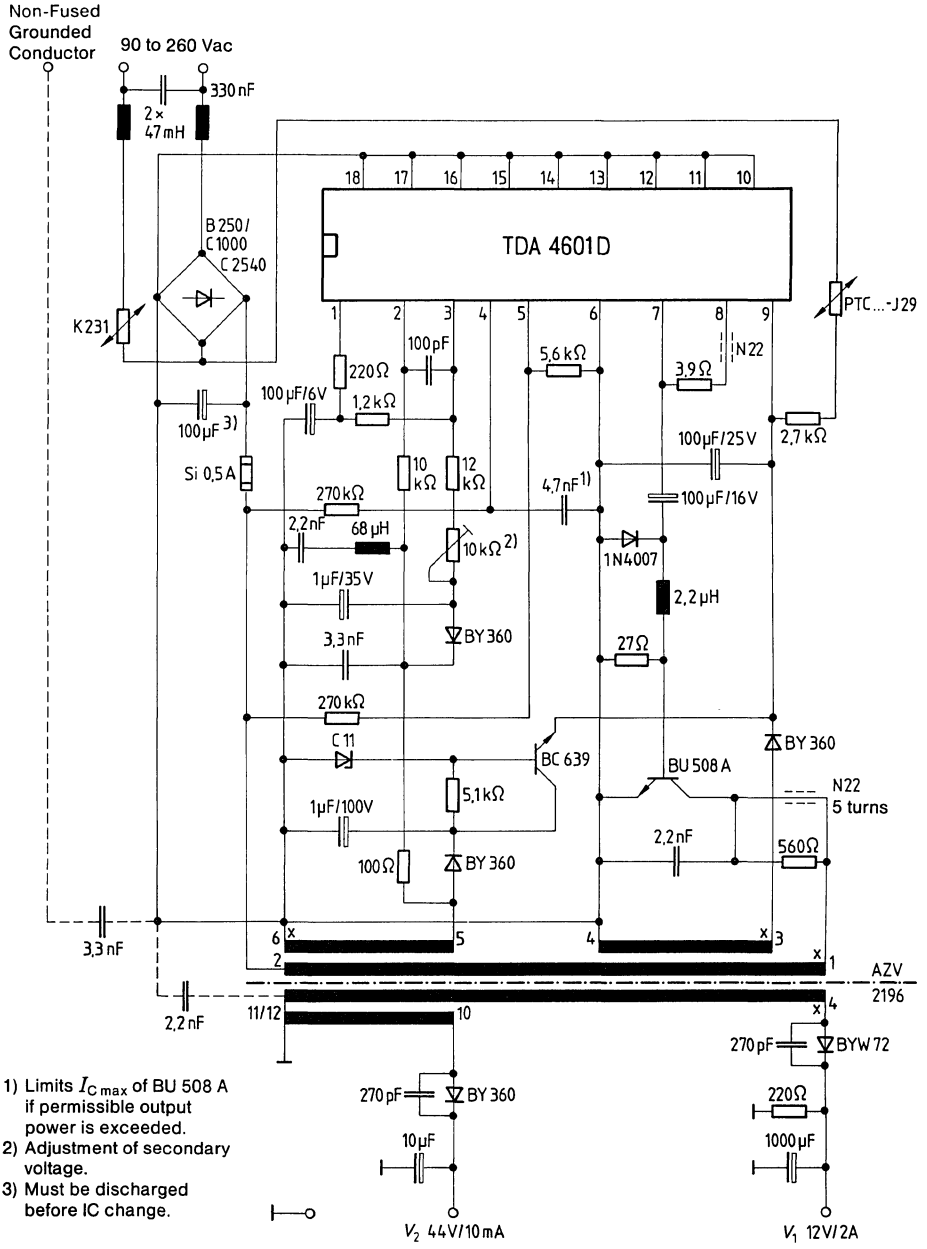
Highly stable secondary side

Power supplies for commercial purposes require highly constant low voltages and high currents which, on the basis of the flyback converter principle, can be realized only under certain conditions, but, on the other hand, are implemented for economical reasons. An electrically isolated flyback converter with a highly stable secondary side must receive the control information from this secondary side. There are only two possibilities of meeting this requirement: either through a transformer which is magnetically isolated from the flyback converter or by means of an optocoupler. The development of CNY 17 has enabled the manufacture of a component suitable for electrical isolation and characterized by high reliability and long-term stability.

The IC TDA 4601 D is the sucessor of the TDA 4600 D. It is compatible with its predecessor in all operational functions and in the control of a self-oscillating flyback converter. Pin 3 is the input for the control information, where the latter is compared with the reference voltage prevailing at pin 1 and the control information from the optocoupler and subsequently transformed into a frequency/pulse width control.

The previous feedback and control information winding is not necessary. The feedback information (zero passage) is obtained from winding 3/4 – supply winding. The time constant chain 330 Ω/3.3 nF and 330 Ω/2.2 nF was implemented in series with 150 µH to prevent interference at pin 2. The LC element forms a series resonant circuit for overshoots of the flyback converter and short-circuits them.

Application circuit 6



1) Limits $I_{C\,max}$ of BU 508 A if permissible output power is exceeded.
2) Adjustment of secondary voltage.
3) Must be discharged before IC change.

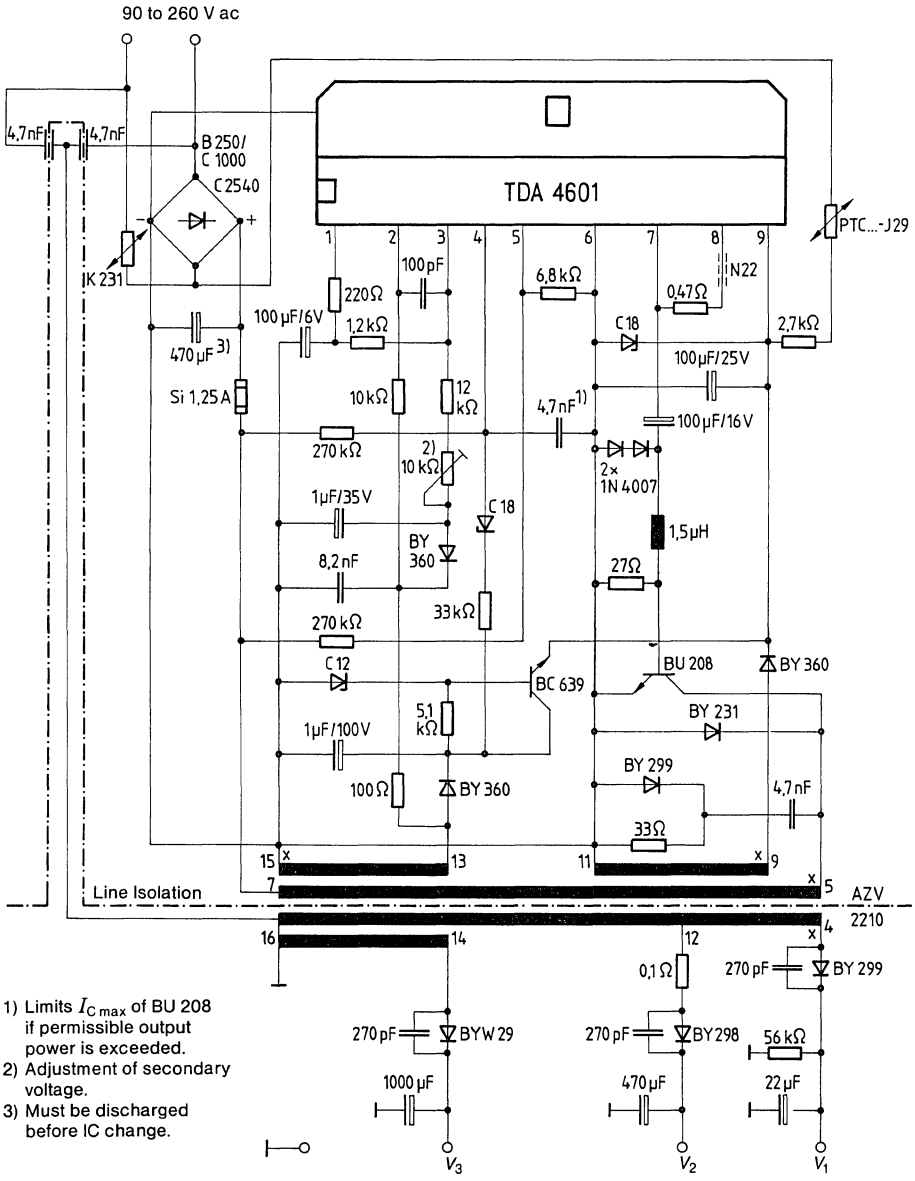
Notes on application circuit 6

Wide range plug SMPS up to 30 W

Due to their volume and weight, plug SMPS have so far been limited to a restricted primary voltage and a secondary power of no more than 6 W.

The line-isolated wide range flyback converter presented here has a variable frequency and is capable of producing a secondary power of 30 W. It is characterized by a compact design with an approx. weight of 400 g. The entire line voltage range of 90 to 260 Vac is stabilized to ±1.5% on the secondary side. Load fluctuations between 0.1 and 2 A are regulated to within 5%. The output (secondary side) is overload, short-circuit, and open-loop proof.

Application circuit 7



1) Limits $I_{C\,max}$ of BU 208 if permissible output power is exceeded.
2) Adjustment of secondary voltage.
3) Must be discharged before IC change.

Notes on application circuit 7

Wide range SMPS with reducing peak collector current $I_{C\ BU\ 208}$ for rising line voltage (variable point of return)

Wide range SMPS have to be dimensioned at line voltages of 90 to 260 Vac. The difference between the maximum collector current $I_{C\ BU\ 208\ max}$ and the largest possible limit current $I_{C\ BU\ 208\ limit}$ which causes magnetic saturation of the flyback transformer and flows through the primary inductance winding 5/7 is to be determined at Vac_{min} ($I_{C\ BU\ 308\ limit} \geq 1.2 \times I_{C\ BU\ 208\ max}$). Then, the transmissible power of the flyback transformer and its value at Vac_{max} is to be determined. In the standard circuit the collector current $I_{C\ BU\ 208\ max}$ is almost constant at the point of return independently of the line voltage. The transmissible power on the secondary side, however, increases at the point of return in proportion to the rising rectified line voltage applied (figures 1 and 2).

In the wide range SMPS a line voltage ratio of 270/90 = 3/1 is obtained causing doubling of the transmissible power on the secondary side, i.e. in the wide range SMPS a flyback transformer had to be implemented that was much too large.

The point of return protecting the SMPS against overloads or short circuits, is derived from the time constant at pin 4 τ_4 = 270 kΩ x 4.7 nF. Thus, the largest possible pulse width is determined.

With the introduction of the 33 kΩ resistor this time constant is reduced as a function of the control voltage applied to winding 13/15, rectified by diode BY 360 and filtered by the 1 µF capacitance, which means that the pulse time becomes shorter. By means of the Z diode C18 the line voltage level can be defined at which the influence of the time constant correction becomes noticeable. The change in the rectified voltage of winding 13/15 is proportional to the change in the rectified line voltage.

At the point of return $I_{C\ BU\ 208}$ the peak collector current has been reduced with the aid of the given values from 5.2 A at 90 Vac to 3.3 A at 270 Vac. The transmissible power at the point of return remains stable between 125 and 270 Vac due to the set activation point of the point of return correction (unbroken curve in fig. 2).

SMPS IC for Control of SIPMOS Transistors — TDA 4605

Preliminary data — **DIP 8**

This IC is designed for controlling an MOS power transistor and performing all necessary protective and control functions in self-oscillating flyback converter power supplies. Owing to the IC's outstanding voltage stability, which is maintained even at substantial fluctuations, the IC is suited for consumer as well as for industrial applications.

- Direct control of the switching transistor
- Reversing linear overload characteristic

Description of function

The power transistor and primary winding of the flyback transformer, which are connected in series, receive direct supply of the input voltage. During the on-phase of the transistor, energy is stored in the primary winding and during the off-phase it is released to the consumer via the secondary winding. The IC controls the power transistor in such a way that the secondary voltages are kept at constant values independently of input or load changes. The control information required is obtained from the input voltage during the on-phase and from a control winding (secondary winding) during the off-phase. Load differences are compensated by altering the frequency, input voltage fluctuations are additionally counteracted by altering the pulse duty factor. This results in the following load-dependent modes of the SMPS:

- Open-loop or small load: output voltage slightly above set value
- Control: load-independent output voltage
- Overload: in case of overload or short-circuit, the secondary voltage is decreased from the point of return as a function of the load current, following a reversing characteristic

Typical values of pulse duty factor ν, switching frequency f and duration of primary phase t of the power transistor:

Mode	ν	f/kHz	t/µs
Open-loop	0.1	150	0.7
Small load (5 W)	0.33	80	2.5
Control mode (30-100 W)	0.33	40	5.6
Reversing point 150 W	<0.5	20	<25
Short-circuit	0.02	1.5	<15

Description of use

A flyback converter designed for color TV sets, applicable between 30 W and 120 W and for line voltages ranging from 90 to 140 V, is shown in one of the following figures. On the subsequent pages the major pulses can be found.

The line voltage is rectified by bridge rectifier Gr1 and smoothed by C_3.

During start-up the IC current is supplied via resistors R_2 and R_3, and in the post-transient condition it is additionally supplied via winding 13/11 and rectifier D3. The size of filter capacitor C_6 determines the turn-on behavior.

Switching transistor T1 is a BUZ 45. Parallel capacitance C_9 and primary winding 1/7 form a resonant circuit, thus limiting the frequency and amplitude of drain-source voltage overshoots during turn-off of T1. Self-oscillation is attenuated by R_{14}. Diode D5 limits positive overshoots. R_{12} prevents static charging of the gate of T1. D1 improves the turn-off behavior. The current rise in T1 is determined by the inductance of the primary winding. This sawtooth-shaped rise is simulated at network R_7C_4 and applied to pin 2 of the IC.

Depending on the dimensioning of the primary inductance, timing element R_7C_4 is to be adapted to the current rise angle in T1. Thus, during the on-phase, the IC receives the control information in the form of the simulated energy content of the primary winding at pin 2 as a function of line voltage versus time.

The control deviation at pin 1 is recorded by control winding 9/15. This measure requires fixed coupling with the secondary winding 2/16. The control winding is also used for feedback and permits self-oscillation of the parallel circuit C_9/primary inductance if the power transistor is inhibited. Thus, the maximum possible open-loop frequency is determined.

The control voltage required for pin 1 is rectified by diode D4 and smoothed by capacitor C_7. Furthermore, R_{13} and C_8 form a timing element, which serves for filtering fast changes in the control voltage, i.e. the final element does not become active until several periods have occurred. By means of the voltage divider formed of resistors R_8, R_9, R_{10}, the secondary voltage can be set. Reason: in the IC the control voltage produced at pin 1 is compared with a stable, internal reference voltage.

According to the result of this comparison, frequency and pulse duty factor are corrected until the secondary voltage selected by R_{10} has established itself. For all operating modes of the SMPS, the zero passages of the voltage at the control winding contain information on pulse duty factor and switching frequency of the switching transistor T1, or the open-loop frequency. Conditioning of the corresponding signal at pin 8 is performed by series resistor R11 and by integrated limiter diodes.

An SMPS based on these principles would have a point of return dependent on the line voltage. With respect to the distance to the saturation point, the transformer must be dimensioned for maximum power, i.e. for maximum line voltage and the power then occurring at the point of return.

In order to keep the size of the transformer as small as possible, the IC makes the point of return largely independent of the rectified line voltage. If necessary, the reverse point correction of the IC can be altered by a network from pin 7 to ground. The information on the line voltage is applied to pin 3. Before the line voltage falls below its minimum value, the SMPS must be turned off by the IC in order to obtain defined turn-off conditions.

During undervoltage, the information required for turn-off is applied to pin 3 via the resistive divider R_4/R_5. On the secondary side the output voltages $V_{1\ sec}$ to $V_{4\ sec}$ are available. If the secondary side is further deloaded, standby is set automatically. Resistor R_{15} forms a basic load of voltage $V_{1\ sec}$ and contributes to maintaining standby conditions (V_{sec} rise 20%). Capacitors C_{10} and C_{13} prevent spikes generated by reversing the rectifiers D7 through D9. The secondary voltages are smoothed by charging electrolytic capacitors C_{14} through C_{17}.

Circuit description

Pin 1 In the control and overload amplifier the control voltage supplied to this pin is compared with two stable, internal reference potentials — in the control and overload mode with V_{cont}, in the case of a short-circuit with V_{short}. The output of this stage operates on the stop comparator.

Pin 2 By means of the external RC combination in conjunction with the primary current voltage converter, a voltage is generated which is proportional to the collector current of the switching transistor. Controlled by the control logic and referred to the internal stable voltage V_{2B}, the output of this converter operates on the stop comparator and the output stage. If voltage V_2 exceeds the output voltage of the control amplifier, the control logic is set back by the stop comparator and, as a result, the output of pin 5 is put to low potential. Other inputs for the logic stage are the output for the start pulse generator with a stable reference potential V_{st} as well as the operating voltage monitoring.

Pin 3 The applied, scaled down primary voltage stabilizes the point of return. Furthermore, in case of undervoltage, the control logic is blocked by comparison with the internal stable voltage V_V in the primary voltage monitoring block.

Pin 4 GND

Pin 5 In the output stage the output signals generated by the control logic are converted into driving suitable for MOS power transistors.

Pin 6 For the operating voltage monitoring, a stable internal reference voltage V_{REF} and the switching thresholds V_{6A}, V_{6E}, $V_{6\ max}$ and $V_{6\ min}$ are derived from the supply voltage at pin 6. V_{REF} is the basis for all reference magnitudes (V_{cont}, V_{short}, V_{4B}, V_{st}). If $V_6 > V_{6E}$, V_{REF} is switched on; if $V_6 < V_{6A}$, it is turned off. Furthermore, the control logic is enabled only with $V_{6\,min} < V_6 < V_{6\,max}$.

Pin 7 In the reverse point correction block, the rectified, scaled down line voltage of pin 3 serves for correction. If required, the correction can be altered by a network from pin 7 to ground. The output of this block influences the primary current voltage converter and stop comparator stages.

Pin 8 The zero passage detector, which drives the control logic block, recognizes the discharged state of the transformer by means of the zero passage of voltage V_8 from positive to negative values and enables the control logic for the pulse start.

At the end of the pulse parasitic oscillations at pin 8 may occur (ringing of transformer), which cannot cause a new pulse start (double pulse) however, since an internal circuit makes the zero passage detector inactive for a limited period of time.

1. Start-up behavior

On page 61 the start-up behavior of the application circuit is illustrated for a line voltage that is barely above the value for undervoltage.

After application of the line voltage at the point in time t_0, the following voltages build up:

- V_6 according to the halfwave charge across R_2 and R_3
- V_2 to V_{2max} (typ. 6.2 V)
- V_3 to the value given by divider R_4/R_5

The current consumption of the IC in this mode of operation is smaller than 1.5 mA. When V_6 reaches the threshold V_{6E} (time t_1), the IC turns on the internal reference voltage. The current consumption increases to typically 12 mA. The primary-current voltage transformer reduces V_2 to V_{2B} and between time t_5 and t_6 the start-pulse generator will produce the start pulse. The feedback at pin 8 starts the next pulse and so on. All pulses, including the start pulse, are controlled in width by the control voltage at pin 1. Upon turn-on this corresponds to the case of short-circuit, i.e. $V_1 = 0$ V. Thus, the IC starts with "short-circuit pulses" that widen according to the feed-back control voltage. The IC operates in the point of return. Afterwards the peak values rapidly drop to V_2 because the IC is operating in the control range. The control loop is stabilized. If voltage V_6 falls below the cutout threshold V_{6min} before the point of return is reached, the start will be interrupted (pin 5 goes Low). The IC remains turned on, so V_6 drops further to V_{6A}. Then the IC turns off, V_6 can build up again (time t_4) and a new turn-on attempt begins at time t_1. If the rectified line ac voltage (primary voltage) breaks down because of the load, V_3 can, as happens at time t_3, fall below V_{3A} (turn-on attempt with undervoltage). The primary-voltage monitoring then clamps V_3 to V_{3S} until the IC turns off ($V_6 < V_{6A}$). Then a new turn-on attempt is started at time t_1.

2. Control, overload and open-circuit behavior

When the IC has started up, it operates in the control range. The voltage on pin 1 is typically 400 mV.

When the output is loaded, the control amplifier permits wider charge pulses (V_5 = H). The peak value of the voltage at pin 2 increases to V_{25max}. If the secondary load is increased further, the overload amplifier will start to reduce the pulse width. Because the change in pulse width reverses, this is called the point of return of the power supply. The IC supply voltage V_6 is directly proportional to the secondary voltage, so it breaks down according to the overload control response. If V_6 falls below the value V_{6min}, the IC will go into sampling operation. The time constant of the halfwave start-up is relatively large, so the short-circuit power remains small. The overload amplifier reduces to the pulse width t_{psh}. This pulse width must remain possible so that the IC can start without any problems from the virtual short-circuit, i.e. the turn-on with $V_1 = 0$.

If the load is reduced on the secondary side, the charge pulses (V_5 = H) become narrower. The frequency increases up to the natural frequency of the system. If the load is reduced further, the secondary voltages build up to V_6. At $V_6 = V_{6max}$ the logic is blocked. The IC goes into sampling operation. Thus the circuit is absolutely open-circuit-proof.

3. Overtemperature response

An integrated temperature cutout blocks the logic if the chip temperature becomes inadmissibly high. The IC automatically samples the temperature and starts as soon as it drops to an admissible level.

Maximum ratings

		min	max		Remarks
Voltages					
Pin 1	V_1	−0.3	3	V	
Pin 2	V_2	−0.3		V	
Pin 3	V_3	−0.3		V	
Pin 5	V_5	−0.3	V_6	V	
Pin 6	V_6	−0.3	20	V	Supply voltage
Pin 7	V_7	−0.3		V	
Pin 8	V_8	−0.3		V	
Currents					
Pin 1	I_1	−3	1	mA	
Pin 2	I_2	−3	3	mA	
Pin 3	I_3	−3	3	mA	
Pin 4	I_4	−1.5		A	$t_p \leq 50\ \mu s; \nu \leq 0.5$
Pin 5	I_5	−1.5	1.5	A	$t_p \leq 50\ \mu s; \nu \leq 0.5$
Pin 6	I_6	−0.01	1.5	A	$t_p \leq 50\ \mu s; \nu \leq 0.5$
Pin 7	I_7	−3	1	mA	
Pin 8	I_8	−3	3	mA	
Junction temperature	T_j		125	°C	
Storage temperature range	T_{stg}	−40	125	°C	
Thermal resistances					
junction-air	R_{thJA}		100	K/W	
junction-case measured at pin 4	R_{thJC}		70	K/W	

Operating range

Supply voltage	V_6	7.5	15	V
Case temperature	T_C	−20	85	°C

Characteristics $T_A = 25\,°C$		Measurement circuit	min	typ	max	
Start-up hysteresis						
Start-up current consumption $V_6 = 5$ V	$I_{6/5}$	1		0.5	0.75	mA
Start-up current consumption $V_6 = 8$ V	$I_{6/8}$	1		1	1.5	mA
Turn-on voltage	V_{6E}	1	11	12	13	V
Turn-off voltage	V_{6A}	1	6	6.5	7	V
Turn-on current $V_6 = V_{6E}$	I_{6E}	1		12	16	mA
Turn-off current $V_6 = V_{6A}$	I_{6A}	1		10		mA
Voltage limiter ($V_6 = 10$ V, IC turned off) at pin 2 ($V_6 < V_{6E}$) $I_2 = 1$ mA	V_{4max}	1	5.6	6.6	7.6	V
at pin 3 ($V_6 < V_{6E}$) $I_3 = 1$ mA	V_{5max}	1	5.6	6.6	7.6	V
Control range						
Control input voltage	V_{1cont}	2		400		mV
Gain in control range $G_{cont} = \frac{d\,(V_{2S} - V_{2B})}{dV_1}$	G_{cont}	2		−400		
Primary-current simulation voltage						
Basic value	V_{2B}	2		1		V
Maximum peak value $G_1 = V_{1cont}\,(2\,V/V_{cont})$	$V_{2S\,max}$	2		3		V
Overload and short-circuit operation						
Overload range upper limit	V_{1U}	2		400		mV
Overload range lower limit	V_{1L}	2		150		mV
Gain in overload range $G_{over} = \frac{d(V_{2S} - V_{2B})}{dV_1}$	G_{over}	2		2		
Input voltage in overload range $V_{cont} = 3.5$ V	V_1	2		360		mV
Input current in short-circuit operation $V_{cont} = 0$ V	I_1	2		−140		µA
Peak value in overload range $V_{cont} = 3.5$ V	V_{2over}	2		3.0		V
Peak value in short-circuit operation $V_{cont} = 0$ V	V_{2sh}	2		2.7		V
Output pulse width in overload range $V_{cont} = 3.5$ V	$t_{p\,over}$	2		8.5		µs
Output pulse width in short-circuit operation $V_{cont} = 0$ V	$t_{p\,sh}$	2		7.5		µs
Current consumption in overload range $V_{cont} = 3.5$ V	I_6	2		12		mA
Current consumption in short-circuit operation $V_{cont} = 0$ V	I_6	2		10		mA

Characteristics

$T_A = 25\,°C$

		Measurement circuit	min	typ	max	
Generally valid data						
($V_6 = 10$ V)						
Point-of-return correction						
Point-of-return correction voltage $V_3' = 5$ V; $V_2' = 0$ V	V_7	2		5		V
Point-of-return correction current $V_3' = 5$ V; $V_2' = 0$ V	I_4	1		−460		µA
Zero-passage detector voltage						
Positive value	V_{8P}	2		0.7		V
Negative value	V_{8N}	2		−0.2		V
Delay between V_8 and V_2	t_{d4}	2		2		µs
Output-stage data						
Saturation voltages S in setting 1						
of upper transistor $I_5 = -1.5$ A	V_{satU}	1		2		V
of lower transistor $I_5 = +1.5$ A	V_{satL}	1		2		V
Slew rate of output voltage						
Rising edge $V_{cont} = 3.5$ V	$+dV_5/dt$	2		10		V/µs
Falling edge $V_{cont} = 3.5$ V	$-dV_5/dt$	2		50		V/µs

Characteristics

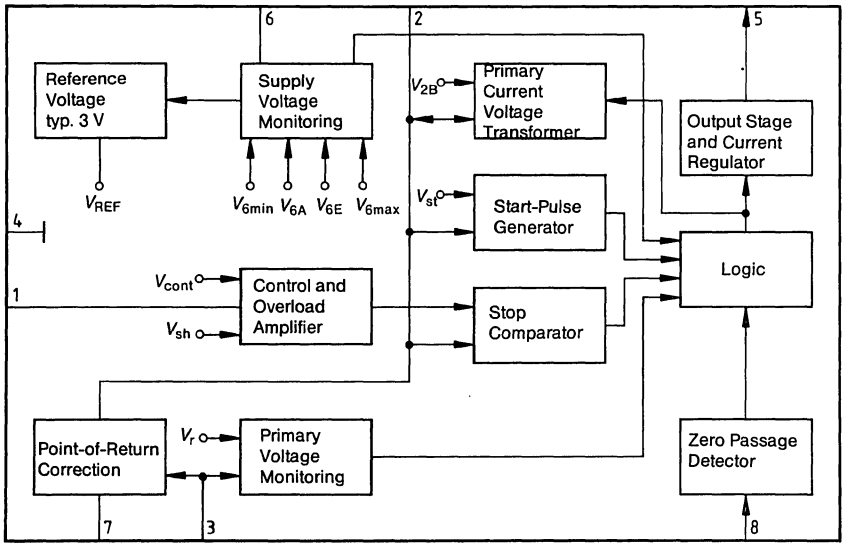
$T_A = 25\,°C$

		Measurement circuit	min	typ	max	
Protective circuits						
1. Undervoltage protection for V_6: voltage on pin 5 = V_{5min} when $V_6 < V_{6min}$ (with $V_{6min} = V_{6A} + \Delta V_6$)	ΔV_6	2	0.3	0.5	1	V
2. Overvoltage protection for V_6: voltage on pin 5 = V_{5min} when $V_6 < V_{6max}$	V_{6max}		14	15	16	V
3. Undervoltage protection for V_{line}: voltage on pin 5 = V_{5min} when $V_3 > V_{3A}$ $V_2' = 0$ V	V_{3A}	1		1		V
4. Overtemperature: chip temperature at which IC switches V_5 to V_{5min}	T_j	2		125		°C
Voltage on pin 3 after response of protective function (V_3 is clamped until $V_6 < V_{6A}$) $I_3 = 3$ mA	V_3	1		0.2	0.4	V
Sampling current consumption $V_3 = V_2 = 0$ V	I_6	1		12		mA

Characteristics

		Measurement circuit	min	typ	max	
Normal operation (V_{line} = 220 V; S1, S2, S3, S4 closed)						
1. Secondary voltage	V_{1S}	3		95		V
2. Secondary voltage	V_{2S}	3		26		V
3. Secondary voltage	V_{3S}	3		15		V
4. Secondary voltage	V_{4S}	3		8.5		V
Turn-on time for secondary voltages	t_{on}	3		120		ms
Voltage alteration between S5 open and S5 closed	ΔV_{1S}	3		100	500	mV
Load variation cross-talk Voltage alteration between S6 open and S6 closed	ΔV_{1S}	3		500	1000	mV
Standby operation (V_{line} = 220 V; $P_{sec} \leq 2$ W)						
Voltage build-up	ΔV_{1S}	3		20	30	V
Frequency	f	3	75	80		kHz
Power consumption	P_{prim}	3		10	15	VA
Point-of-return stability						
Max. secondary current (secondary point of return) S1 closed I_{1Smax} is set with R_{17} V_{1S} = 85 V	I_{1Smax}	3		1.85		A
Relative alteration of I_{1Smax} 80 V < V_{line} < 140 V	ΔI_{1Smax}	3			±10	%

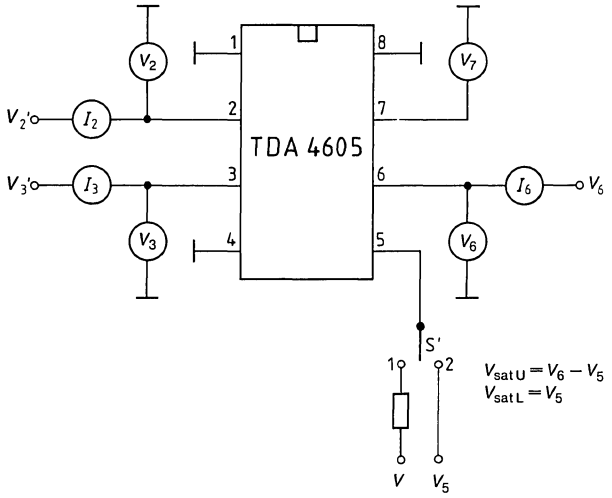
Block diagram

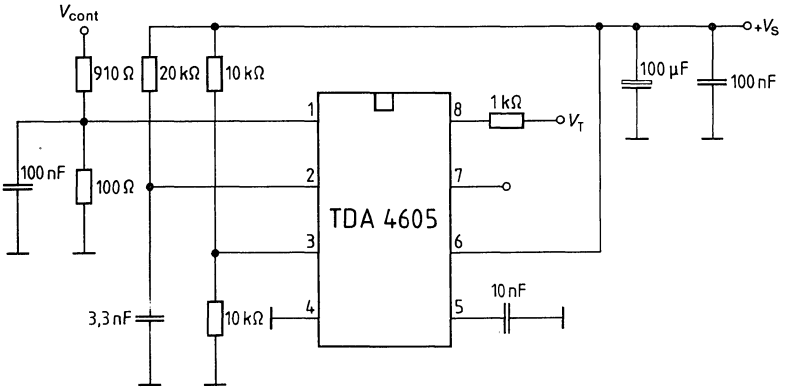


Pin description

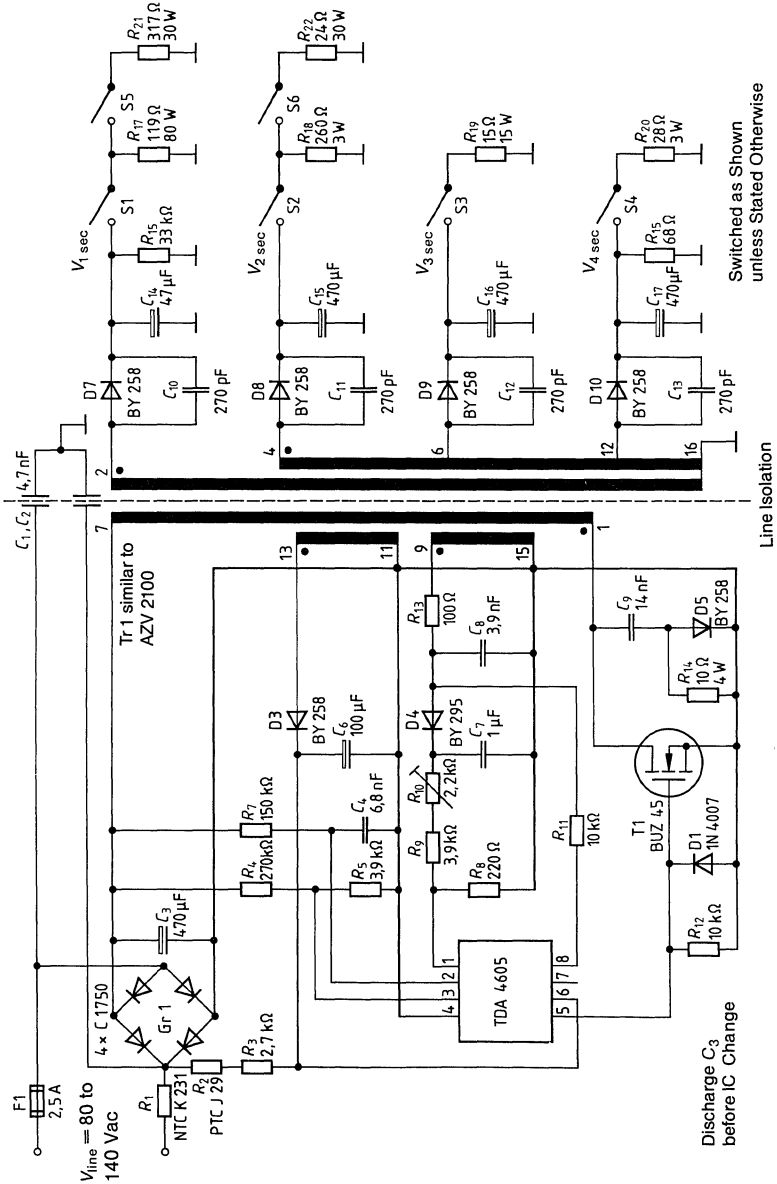
Pin	Designation	Function
1	Control voltage	Information input for secondary voltage. By comparison of the control voltage derived from the control winding of the transformer with the internal reference voltage the output pulse width at pin 5 is matched to the load on the secondary side (normal, overload, short-circuit, open-circuit).
2	Primary-current simulation	Information input for primary voltage. The primary-current rise in the primary winding is simulated as a voltage rise at pin 2 by means of an external RC network. When a value derived from the control voltage at pin 1 is reached, the output pulse at pin 5 is terminated. The maximum power in the point of return is set with the RC network.
3	Undervoltage detector	Input for primary-voltage monitoring. The IC is cut out upon line undervoltage by comparison with an internal reference. The voltage at pin 3 is used for point-of-return correction.
4	Ground	
5	Output	Push-pull C output supplies ±1.5 A for fast charge reversal of the gate capacitances of the power MOS transistor.
6	Supply voltage	Input for the supply voltage. From this a stable internal reference V_{REF} and the switching thresholds V_{6A}, V_{6E}, V_{6max} and V_{6min} for monitoring of the operating voltage are derived. V_{REF} is turned on for $V_6 < V_{6E}$ and turned off for $V_6 < V_{6A}$. The logic is only enabled for $V_{6min} < V_6 < V_{6max}$.
7	Point-of-return correction	Input for point-of-return correction. The network on this pin to ground influences internal correction (slope and response).
8	Zero-passage detector	Input for oscillator feedback. After build-up each zero passage of the feedback voltage (falling edge) triggers an output pulse at pin 5. The trigger threshold is typ. +50 mV.

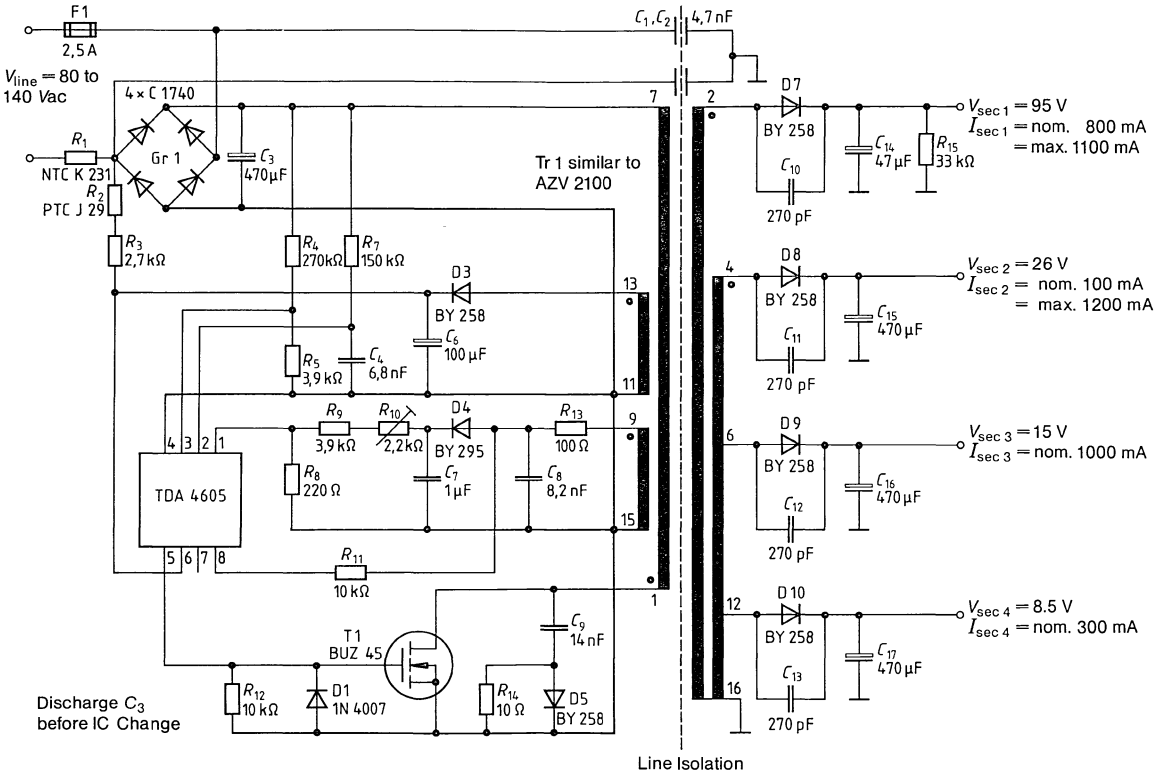
Measurement circuit 1



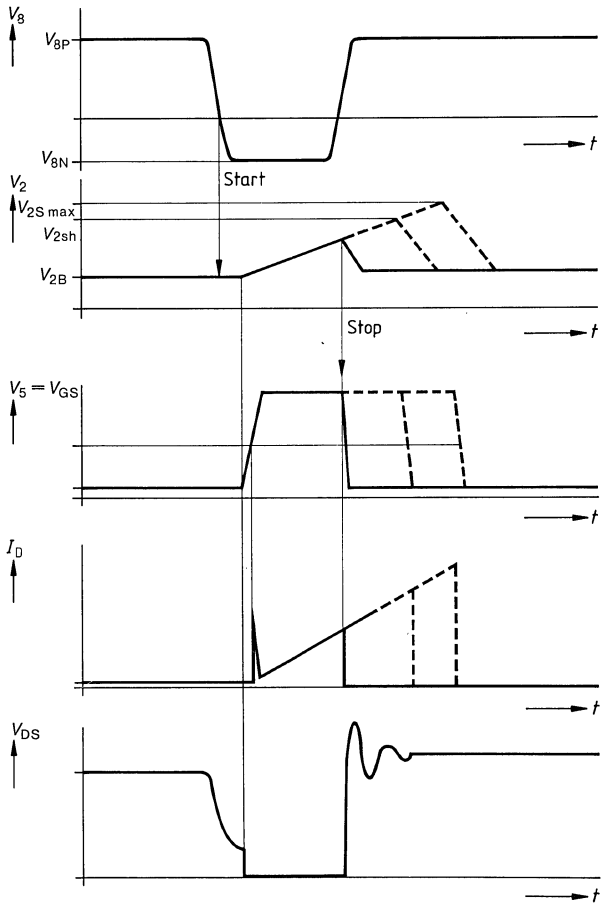


Measurement circuit 3

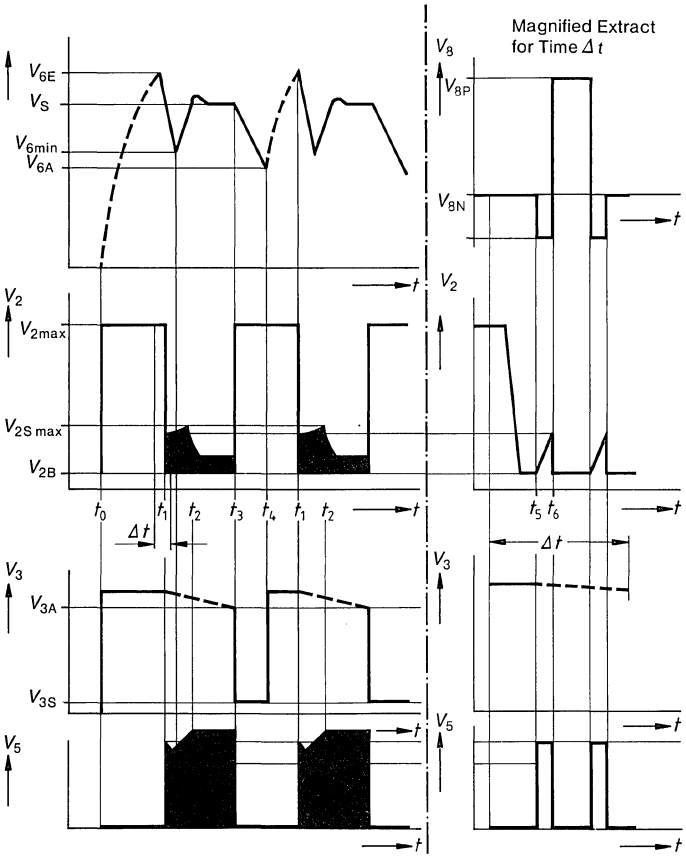



F1
2,5 A
V_{line} = 80 to 140 Vac
4 × C 1740
Gr 1
R_1
NTC K 231
R_2
PTC J 29
C_3 470 µF
R_3 2,7 kΩ
R_4 270 kΩ
R_7 150 kΩ
Tr 1 similar to AZV 2100
C_1, C_2 4,7 nF
D3 BY 258
C_6 100 µF
R_5 3,9 kΩ
C_4 6,8 nF
R_9 3,9 kΩ
R_{10} 2,2 kΩ
D4 BY 295
R_{13} 100 Ω
C_7 1 µF
C_8 8,2 nF
R_8 220 Ω
TDA 4605
R_{11} 10 kΩ
T1 BUZ 45
C_9 14 nF
R_{12} 10 kΩ
D1 1N 4007
R_{14} 10 Ω
D5 BY 258
Discharge C_3 before IC Change
Line Isolation
D7 BY 258
C_{10} 270 pF
C_{14} 47 µF
R_{15} 33 kΩ
$V_{sec\,1}$ = 95 V
$I_{sec\,1}$ = nom. 800 mA
= max. 1100 mA
D8 BY 258
C_{11} 270 pF
C_{15} 470 µF
$V_{sec\,2}$ = 26 V
$I_{sec\,2}$ = nom. 100 mA
= max. 1200 mA
D9 BY 258
C_{12} 270 pF
C_{16} 470 µF
$V_{sec\,3}$ = 15 V
$I_{sec\,3}$ = nom. 1000 mA
D10 BY 258
C_{13} 270 pF
C_{17} 470 µF
$V_{sec\,4}$ = 8.5 V
$I_{sec\,4}$ = nom. 300 mA

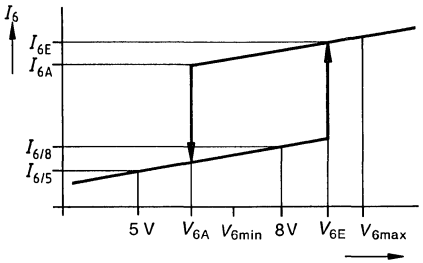
Diagram



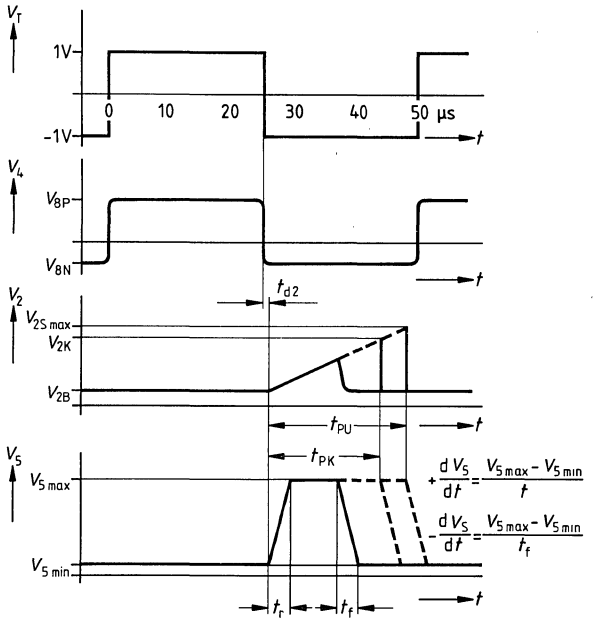
Diagram


Magnified Extract
for Time Δ t
V6E
VS
V6min
V6A
V8
V8P
V8N
t
V2
V2max
V2S max
V2B
V2
t0
t1
t2
t3
t4
t1
t2
t5
t6
Δ t
V3
V3A
V3S
V3
V5
V5

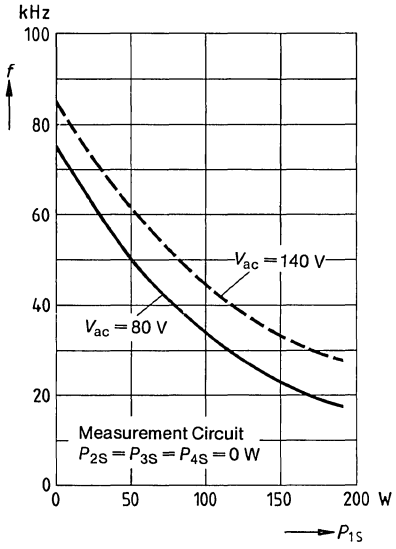
1. Start-up hysteresis



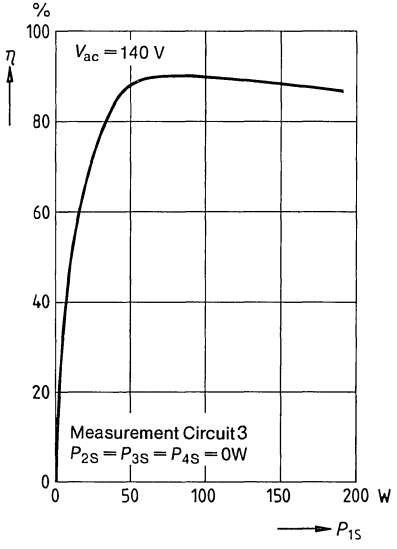
2. Operation in measurement circuit 2



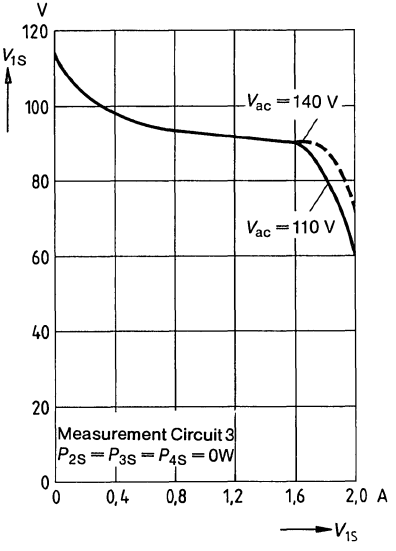
Frequency f versus secondary power P_{1S}



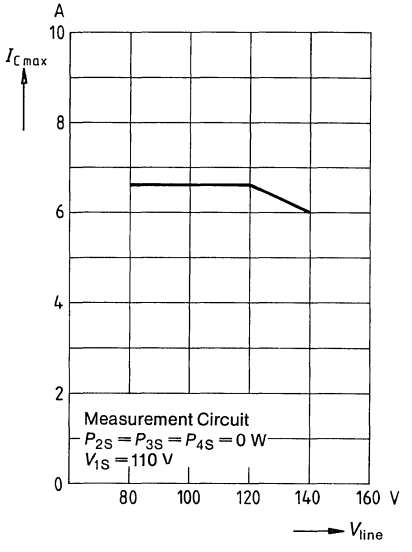
Efficiency η versus secondary power P_{1S}



Secondary voltage V_{1S} versus secondary current I_{1S}



Peak collector current $I_{c\,max}$ of switching transistor versus primary voltage V_{line}

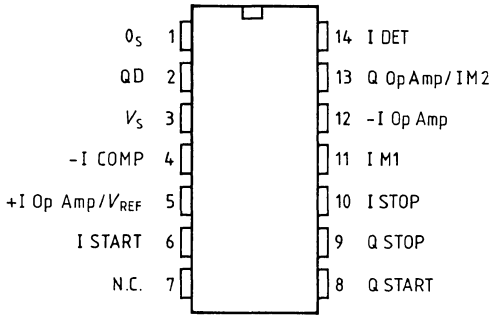


DIP 14

This device contains the components for designing a switched-mode power supply with sinusoidal line-current consumption. Sinusoidal line current is drawn from the supply network in particular when there is high power consumption. One possible application is in electronic ballasts for fluorescent lamps, especially when a large number of these lamps are concentrated on one supply point. This IC is additionally suitable for general driving of switched-mode power supplies. The possibility of regulating the output voltage will enable operation on different line voltages (110 Vac/220 Vac) without any switchover.

A monitoring circuit makes it possible to control various turn-on and turn-off functions of different units of equipment.

Pin configuration
(top view)



Pin description

Pin	Function
1	Ground 0_S
2	Driver output QD
3	Supply voltage V_S
4	Negative comparator input —I COMP
5	Positive input Op Amp/V_{REF}
6	Start input I START
7	N.C.
8	Start output Q START
9	Stop output Q STOP
10	Stop input I STOP
11	Multiplier input M1 IM1
12	Negative input Op Amp
13	Op Amp output/multiplier input M2 Q Op Amp/I M2
14	Detector input I DET

Circuit description

The IC switches from standby to full current consumption when the turn-on threshold on V_S is exceeded. Turn-off is controlled by hysteresis. The integrated Z diode limits the voltage on V_S when impressed current is fed.

The operational amplifier (op amp) can be wired as a control amplifier. It will then compare the divided output voltage V_Q to a reference voltage V_{REF} that is stable with temperature. The output voltage of the op amp that is produced in this way is multiplied by a sine-magnitude voltage in the multiplier (M). At the output of the latter a sine-magnitude voltage then appears that is variable in amplitude. This nominal voltage is applied to the plus input of the comparator. The nominal voltage at the multiplier output can then be compared via the comparator to a voltage derived from the actual line current. The output of the comparator feeds the reference signal via a logic circuit to the driver that switches the SIPMOS transistor. No current gaps may appear in the choke, otherwise the line current would no longer be sinusoidal. To achieve that, the detector input I DET senses when the choke current has fallen to zero after turn-off of the SIPMOS transistor. This ensures that the SIPMOS transistor does not turn on too early and that no current gaps occur.

When the detector input I DET is on High potential, the SIPMOS driver output QD is blocked. At the same time the flipflop can be set by the comparator.

When I DET is Low, the Q output is enabled and can be disabled again by the comparator by resetting the flipflop.

Consequently the choke is always currentless when the SIPMOS transistor turns on and no current gaps appear in the choke.

Driver output QD for SIPMOS transistors

The output driver is designed as a push-pull stage. There is a resistor of 10 Ω in series with the output for the purpose of current limiting. Between Q and ground there is a resistor of 10 kΩ. This keeps the SIPMOS transistor reliably turned off during standby.

The Q output is additionally connected to the supply voltage V_S and to ground by way of diodes.

When the supply voltage to the switched-mode power supply is turned on, the diode towards V_S conducts the capacitive displacement currents from the gate of the SIPMOS transistor into the smooting capacitor on V_S. The voltage V_S may not exceed 0.7 V if the SIPMOS transistor is to remain turned off.

The diode towards ground clamps negative voltages on Q to −0.7 V. Capacitive currents produced by voltage incursion on the drain of the SIPMOS transistor are thus able to flow away unhindered.

Reference voltage (V_{REF})

The reference-voltage source is highly stable with temperature. It can be used if additional, external components are wired.

Monitoring circuit (I START, I STOP, Q START, Q STOP)

The monitoring circuit guarantees the secure operation of a unit of equipment. Any circuitry that is shut down because of a fault, for instance, cannot be started up again until the monitoring start (I START/Q START) has turned on and a positive voltage pulse has been impressed on Q START.

If there is a defect present, the monitoring stop (I STOP/Q STOP) will turn on and shut down either the entire unit or simply the circuitry that has to be protected. No restart is then possible until the hold current impressed on I START or I STOP has been interrupted (e.g. by a power-down).

Maximum ratings

		Notes	Lower limit B	Upper limit A	
Supply voltage	V_S	V_Z = Z voltage	−0.3	V_Z	V
Inputs					
Comparator	$V_{I\,COMP}$		−0.3	33	V
	$V_{-I\,COMP}$		−0.3	33	V
Op Amp	$V_{I\,Op\,Amp}$		−0.3	6	V
	$V_{-I\,Op\,Amp}$		−0.3	6	V
Multiplier	V_{M1}		−0.3	33	V
Output Op Amp	$V_{Q\,Op\,Amp}/I_{M2}$		−0.3	6	V
Z current V_S GND	I_Z	Observe P_{max}	0	300	mA
Driver output	V_Q		−0.3	V_S	V
Q clamping diodes	$I_{Q\,D}$	$V_Q > V_S$ or $V_Q < -0.3$ V	−10	10	mA
Input START	$V_{I\,START}$	see characteristics	−0.3	25	V
STOP	$V_{I\,STOP}$	see characteristics	−0.3	33	V
Output START	$V_{Q\,START}$		−10	3	V
STOP	$V_{Q\,STOP}$		−0.3	6	V
Detector input	$V_{I\,DET}$		0.9	6	V
Detector clamping diodes	$I_{I\,DET}$	$V_{I\,DET} > 6$ V or $V_{I\,DET} < 0.9$ V	−10	10	mA
Capacitance at I START to ground	$C_{I\,START}$			150	µF
Junction temperature	T_j			125	°C
Storage temperature	T_{stg}		−55	125	°C
Thermal resistance system-air	$R_{th\,SA}$			65	K/W

Operating range

Supply voltage	V_S	Values for $V_{S\,ON}$, V_Z: see characteristics	$V_{S\,ON}$	V_Z	V
Z current	I_Z	Observe P_{max}	0	200	mA
Driver current	$I_{Q\,D}$		−300	300	mA
Operating temperature	T_A		−25	85	°C

Characteristics ($V_{S\,ON}$* < V_S < V_Z; −25 °C < T_A < +85 °C)

		Lower limit B	typ	Upper limit A	
Current consumption					
Without load on driver Q and V_{REF}; Q Low 0 V < V_S < $V_{S\,ON}$	I_S			0.5	mA
$V_{S\,ON}$ < V_S < V_Z	I_S	2.5	5	6.5	mA
Load on QD with SIPMOS gate; dynamic operation 50 kHz V_S = 12 V load on Q = 10 nF	I_S			15	mA
Hysteresis on V_S					
Turn-on threshold for V_S rising	$V_{hy\,H}$	9.6	10.4	11.2	V
Switching hysteresis	$V_{S\,hy}$	1.0		1.7	V
Comparator (COMP)					
Input offset voltage	V_{IO}	−10		10	mV
Input current	$-I_I$			2	µA
Common-mode input voltage range	V_{IC}	0		3.5	V
Operational amplifier (Op Amp)					
Open-loop voltage gain	G_{V0}	60	80		dB
Input offset voltage	V_{IO}	−30		−10	mV
Input current	$-I_I$			2	µA
Common-mode input voltage	V_{IC}	0		3.5	V
Output current	$I_{Q\,Op\,Amp}$	−3		1.5	mA
Output voltage	$V_{Q\,Op\,Amp}$	1.2		4	V
Transition frequency	f_T		2		MHz
Transition phase	φ_T		120		deg.

Characteristics ($V_{S\,ON}{}^* < V_S < V_Z$; $-25\,°C < T_A < +85\,°C$)

		Lower limit B	typ	Upper limit A	
Output driver (QD)					
Output voltage high $I_Q = -10$ mA	V_{QH}	5			V
Output voltage low $I_Q = +10$ mA	V_{QL}			1	V
Output current					
rising edge $C_L = 10$ nF	$-I_Q$	200	300	400	mA
falling edge $C_L = 10$ nF	I_Q	250	350	450	mA
Reference-voltage source					
Voltage $0 < I_{REF} < 3$ mA	V_{REF}	1.8	2	2.2	V
Load current	$-I_L$	0		3	mA
Voltage change $10\,V < V_S < V_Z$	ΔV_{REF}			5	mV
Voltage change $0\,mA < I_{REF} < 3\,mA$	ΔV_{REF}			20	mV
Temperature response	$\Delta V_{REF}/\Delta T$	−0.5		+0.5	mV/K
Z Diode (V_S − GND)					
Z voltage $I_Z = 200$ mA Observe P_{max}	V_Z	13	15.5	17	V
Multiplier (M1)[1]					
Quadrant for input voltages			1		qu.
Input voltage M1	V_{M1}	0		1	V
Reference level for M1	$V_{REF\,M1}$		0		V
Input voltage M2	V_{M2}	V_{REF}		$V_{REF}+1$	V
Reference level for M2	$V_{REF\,M2}$		V_{REF}		V
Input current M1, M2	$-I_I$	0		2	µA
Coefficient for output-voltage source	C_Q	0.4	0.6	0.8	I/V
Temperature response of output-voltage coefficient	$\Delta TC/C_Q$	−0.3	−0.1	0.1	%/K

For explanations refer to page 642.

Characteristics ($V_{S\,ON}{}^{*} < V_S < V_Z$; $-25\,°C < T_A < +85\,°C$)

		Lower limit B	typ	Upper limit A	
Monitoring circuit					
Input I START					
Turn-on voltage	$V_{I\,ON\,START}$	17	22	26	V
Turn-on current	$I_{I\,ON\,START}$	50	90	130	µA
Turn-off voltage	$V_{I\,OFF\,START}$	2	3.5	5	V
Turn-off current	$I_{I\,OFF\,START}$	70	110	150	µA
Input I STOP[3)]					
Turn-on voltage	$V_{I\,ON\,STOP}$	27	30	3	V
Turn-on current	$I_{I\,ON\,STOP}$	50	90	130	µA
Turn-off voltage	$V_{I\,OFF\,STOP}$	3	5	7	V
Turn-off current	$I_{I\,OFF\,STOP}$	70	110	150	µA
Transfer I START – Q START					
Output current on Q START					
$V_{START} = 15$ V;					
$V_{Q\,START} = 2$ V	$-I_{Q\,START}$	400	600	800	mA
Transfer I STOP – Q STOP					
Output current on Q STOP					
$I_{STOP} = 1.5$ mA;	$-I_{Q\,STOP}$	0.9	1.2		mA
$V_{STOP} = 18$ V;					
$V_{Q\,STOP} = 1.2$ V					
$I_{STOP} = 0.4$ mA;	$-I_{Q\,STOP}$	90	150		µA
$V_{STOP} \approx 7$ V;					
$V_{Q\,STOP} = 1.2$ V					
Detector (I DET)					
Upper switching voltage for voltage rising (H)	$V_{DET\,H}$	1	1.3	1.6	V
Lower switching voltage for voltage falling (L)	$V_{DET\,L}$	0.95			V
Switching hysteresis	$V_{S\,hy}$	50		300	mV
Input current $0.9\,V < V_{DET} < 6$ V	$-I_{DET}$		5		µA
Clamping-diode current $V_{DET} > 6$ V or $V_{DET} < 0.9$ V	I_{DET}	−3		3	mA

For explanations refer to page 642.

Characteristics ($V_{S\,ON}$* < V_S < V_Z; −25 °C < T_A < +85 °C)

		Lower limit B	typ	Upper limit A	
Delay times					
Input comparator → Q[2]	t		200	500	ns

1) Calculation of the output voltage V_{QM}: $V_{QM} = C \cdot V_{M1}{}^{1)} \cdot V_{M2}{}^{2)}$ in V.
The voltages $V_{M1}{}^{1)}$ and $V_{M2}{}^{2)}$ are referred to the particular reference level.
2) Step functions at comparator input $\Delta V_{COMP} = -100$ mV → $\Delta V_{COMP} = +100$ mV.
3) The turn-on voltage of I_{STOP} exceeds the turn-on voltage of I_{START} by at least 3 V.
*) $V_{S\,ON}$ means that V_{SH} has been exceeded but that the voltage is still greater than V_{SL}.

Use and advantages of IC TDA 4814 in SMPS and electronic ballasts

1 Switched mode power supplies

The "active harmonics filter" consists of a rectifier arrangement in a bridge circuit followed by an up-converter. Through a controller action it is possible to draw a virtually sinusoidal current from the single-phase line and produce a regulated dc voltage at the output.

In the case of an SMPS with conventional line rectification it is possible to achieve a power factor (ratio of active power to apparent power) of 0.5 to 0.7. The active harmonics filter serves for improving the power factor, which reaches a value of almost 1, and for reducing the load on the line produced by harmonics. The losses caused by the active harmonics filter are more than compensated by the fact that a subsequent converter can constantly be operated at an optimal operating point because of the input control of the operating voltage.

The extra effort that is necessary, compared to an SMPS without an active harmonics filter, is made good upwards of about 500 W by savings elsewhere (e.g. smaller smoothing capacitance and transistors of a higher resistance in the SMPS). With the wide-ranging power supplies that are in increasing demand, i.e. power supplies that can work on a line of 90 through 240 Vac without any sfwitching changes, the power pay-off limit reduces markedly.

2 Electronic ballasts for fluorescent lamps

The VDE and the EVUs require of **industrial** consumers that they take "sinusoidal current" from the line, i.e. exhibit a purely ohmic response. This is the case with incandescent lamps, cooker rings and heating fixtures.

In all electronic devices with rectification and a CR load the current drain is pulsed, i.e. afflicted by a large harmonic content and impermissible according to VDE. The reflected current ripple can interfere with installations for AF power-line carrier control for instance, i.e. lead to faulty switching. The harmonic content of the current consequently may not exceed certain values.

The line current for a ballast operating with a stable fluorescent lamp must be such that the share of harmonics in relation to the fundamental does not exceed the values given in table 1.

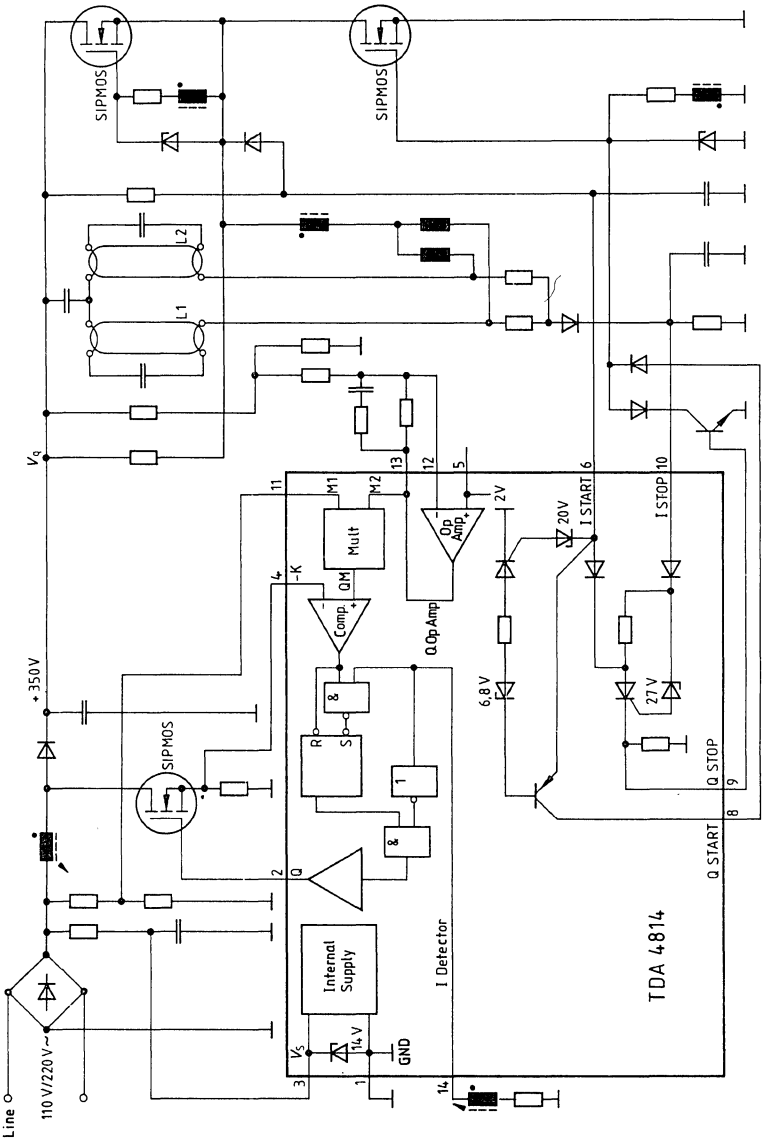
Table 1 Line-current harmonic content in acc. with VDE 0712, part 2

Harmonics	Permissible harmonic content[1] in %
3rd harmonic	$25 \times \frac{\lambda}{0.9}$
5th harmonic	7
7th harmonic	4
9th harmonic	3
11th harmonic	2
13th harmonic and higher	1

1) λ is the power factor

The values given here are achieved using the TDA 4814 to drive a SIPMOS in an up-converter regulating circuit.

Application example
Electronic ballast



Remark
Kindly note that the SIEMENS AG holds patents on electronic ballasts for fluorescent lamps, published in "Siemens Energy and Automation", Vol. II, No. 2, March/April 1985

IC for Push-Pull Switched-Mode Power Supplies with SIPMOS Driver Output

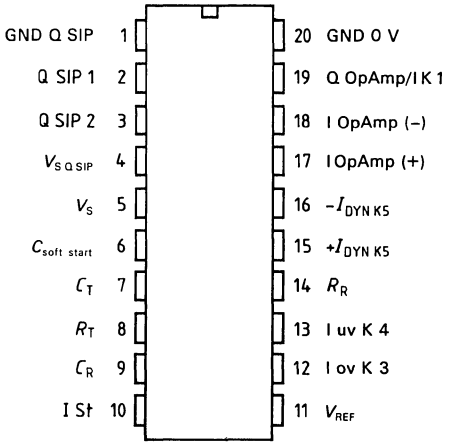
TDA 4918 A

Preliminary data

DIP 20

This versatile switched-mode power supply control IC for the control of SIPMOS power transistors comprises digital and analog functions. These functions are required in the design of high quality flyback and forward converters in single-phase and push-pull operation in normal, half-bridge and full bridge circuits. The component can also be used for single-ended voltage multipliers and speed-controlled motors. Malfunctions in the electrical operation of the switched-mode power supply are recognized by the comparators in the SMPS IC and activate protective functions.

Pin configuration
(top view)



Pin names

Pin no.	Function
1	GND Q SIP
2	Output SIPMOS driver Q SIP 1
3	Output SIPMOS driver Q SIP 2
4	Supply voltage $V_{S\,Q\,SIP}$
5	Supply voltage V_S
6	Soft start $C_{soft\ start}$
7	VCO C_T
8	VCO R_T
9	Ramp generator C_R
10	Input standby I St
11	Reference voltage V_{REF}
12	Input overvoltage K 3
13	Input undervoltage K 4
14	Ramp generator R_R
15	Input dynamic current limitation K 5 (+)
16	Input dynamic current limitation K 5 (–)
17	Input operational amplifier (+)
18	Input operational amplifier (–)
19	Output operational amplifier Q OpAmp/I COMP K 1
20	GND 0 V

Circuit description

The various functional units of the component and their interaction are described in the following.

Supply voltage V_S

The IC enables the two outputs not before the turn-on threshold (V_{SON}) at V_S is exceeded. The duty cycle (active time/disable time) at the enabled outputs can then rise from zero to the value set with K1 in the time specified by the soft start.

An undervoltage at the standby input causes the current consumption I_S to remain at the very low standby current level independent of the voltage V_S.

Voltage controlled oscillator (VCO)

The VCO is connected with the capacitor C_T and the resistor R_T. The charge current at C_T flows continuously and is set with resistor R_T. The discharge current is active during the discharge of C_T and is set internally.

In the typical mode of operation the duration of the rising edge is considerably greater than that of the falling edge. During the falling edge the VCO passes a trigger signal to the ramp generator thus discharging the ramp generator capacitance. Additionally, the trigger signal is routed to other parts of the IC.

Ramp generator

The ramp generator is controlled by the VCO and operates at the same frequency as the VCO. The duration of the ramp generator falling edge must be shorter than the VCO fall time. Only then do the ramp generator upper and lower switching levels reach their rated values.

To control the pulse width at the output, the voltage of the ramp generator rising edge is compared with an externally adjustable dc voltage at comparator K1. The slope of the rising edge is adjusted via the current by means of R_R. This provides the possibility of an additional superimposed control of the output duty cycle. This control capability (feed-forward control) permits the compensation of known interference (e.g. input voltage ripple). A superimposed load current control **(current mode control)** however, can also be implemented.

Push-pull flipflop

The push-pull flipflop is switched by the falling edge of the VCO. This ensures that only one output of the two push-pull outputs is enabled at a time.

Comparator K1 (duty cycle control)

The two plus inputs of the comparator are switched such that the lower plus level is always compared with the level of the minus input. As soon as the voltage of the rising sawtooth edge (minus input) exceeds the lower level of the two plus inputs, the currently active output is disabled via the turn-off flipflop. The "high"-duration of the respectively active output can thus be infinitely varied. As the frequency remains constant, this process corresponds to a change in duty cycle.

Operational amplifier (op amp)

The op amp is a high quality operational amplifier. It can be used in the control circuit to transmit the amplified variations of the voltage to be regulated to the free plus input of comparator K1. A voltage change is thus converted to a duty cycle change.

Turn-off flipflop

The falling edge of the VCO causes a pulse at the turn-off flipflop set input. It can, however, only be actually set if no reset signal is pending. With the turn-off flipflop set, the two outputs are enabled and one of them can be active. Upon an error signal from K 5 or upon a turn-off signal from K1 the flipflop disables the outputs.

Z diode

The Z diode limits the voltage at capacitor $C_{\text{soft start}}$ to a maximum of 5 V. The ramp generator voltage can reach 5.5 V. For an appropriate slope of the rising ramp generator edge, the duty cycle can be limited to a desired maximum value. This can be a possible advantage in flyback converter operation.

Comparator K2

The comparator has its switching threshold at 1.5 V at the plus input, and with its output sets the error flipflop if the voltage at capacitor $C_{\text{soft start}}$ is below 1.5 V. The error flipflop, however, will only accept the set pulse if no reset pulse (error) is pending. This prevents a restart of the outputs as long as an error signal is pending.

Soft start

The lower of the two voltages at the K1 plus inputs – compared with the ramp generator voltage – is a measure for the duty cycle at the output. At component turn-on, the voltage at capacitor $C_{\text{soft start}}$ is equal to 0 V. As long as no error exists, the capacitor will be charged to the maximum value of 5 V with a current of 6 µA.

In the case of an error, $C_{\text{soft start}}$ is discharged with a current of 2 µA. The currently active output, however, is immediately disabled by the error flipflop. Below a charge voltage of 1.5 V, a set signal is pending at the error flipflop and the outputs are enabled if no reset signal is pending at the same time. As the minimum ramp generator voltage, however, is 1.8 V, the duty cycle at the outputs is actually only increased slowly and continuously after the voltage at $C_{\text{soft start}}$ exceeds 1.8 V.

Error flipflop

Error signals, routed to the error flipflop reset input, cause an immediate disabling of the output (low), and after elimination of the error, a restart of the component by soft start.

Comparators K3 (overvoltage), V_{REF} overcurrent, V_S undervoltage

These are error detectors that on error, cause the error flipflop to immediately disable the outputs. After elimination of the error, the duty cycle is raised again using the soft start. Upon overvoltage, a current is impressed at the input of K 3, that can be used to enable an adjustable hysteresis or a holding function.

Comparator K4 (undervoltage)

Comparator K4 switches with an adjustable hysteresis. The value of the hysteresis is derived from the internal resistance of the external control source and the current impressed internally at the input of K4. In the undervoltage case, the set current flows into the component in the technical direction of current flow.

In the error case (undervoltage), both outputs are disabled. The component restarts by soft start.

Comparator K5 (dynamic current limiter)

K5 serves to recognize overcurrents at the switching transistors. Both inputs of the comparator are externally accessible. After elimination of the error, the outputs are enabled with the VCO trigger pulse at the turn-off flipflop. The delay time between occurrence of an error and disabling of the outputs is only approximately 250 ns.

Standby input (I St)

This input switches with voltage and current hysteresis. The voltage levels for switching from standby to active operation can be set with an external voltage divider between V_S – standby input – ground.

Reference voltage (V_{REF})

The reference voltage source is a highly constant source with regard to its temperature behavior. It can be used for the external wiring of the op amp; the error comparators, the ramp generator, or other external components.

SIPMOS driver output (QSIP)

The two outputs operate in the push-pull mode. They are active high. The duration during which one of the outputs is active, can be varied infinitely. The duration of the falling edge at the frequency generator is equal to the minimum duration during which both outputs are simultaneously low.

The output driver is designed as a push-pull stage. The output current is internally limited to the specified values.

A 10 kΩ resistor is connected between the output and ground. This resistor holds the SIPMOS transistor reliably disabled during standby operation (undervoltage at I St.)

Output QSIP is connected with the supply voltage V_{SQSIP} and with ground via diodes.

The diode connected to V_{SQSIP} routes the capacitive shift currents from the SIPMOS transistor gate to the filter capacitor at V_{SQSIP} during turning on the SMPS supply voltage. The voltage at V_{SQSIP} can reach approximately 2.3 V without the SIPMOS transistor being turned on.

The diode connected to ground connects negative voltages at QSIP to –0.7 V. This provides an unimpeded flow off of capacitive currents occurring during voltage breakdown at the SIPMOS transistor drain connection.

For supply voltages starting at approx. 2 V, both outputs are active low in the disabled state. The function of the diode connected to V_{SQSIP} is then taken over by the pull-down source.

Maximum ratings

		Lower limit B	Upper limit A	
Supply voltage				
Inputs K 1, Op Amp, K 3, K 4, K 5, I St	V_S	−0.3	33	V
Frequency generator (VCO)				
Voltage at R_T/C_T	V_{CT}, V_{RT}	−0.3	6	V
$V_{CT} > 6$ V	I_{CT}		3	mA
Ramp generator				
Voltage at C_R/R_R	V_{CR}, V_{RR}	−0.3	6	V
Reference voltage	V_{REF}	−0.3	6	V
Output Op Amp	$V_{Q\,op\,amp}$	−0.3	6	V
Driver output QSIP[1])	V_{QSIP}	−0.3	V_S	V
QSIP clamp diodes at QSIP	I_{QSIP}	−10	10	mA
$V_{QSIP} > V_S$ or $V_{QSIP} < -0.3$ V				
Soft start	$V_{C\ soft\ start}$	−0.3	6	V
Junction temperature[2])	T_j		125	°C
Storage temperature	T_{stg}	−65	125	°C
Thermal resistance (system-air)	$R_{th\,SA}$		63	K/W
Operating range				
Supply voltage[3])	V_S	$V_{S\,ON}$	30	V
Driver current at QSIP 1, 2	I_{QSIP}	−1000	+300	mA
Frequency generator (VCO)	f_{VCO}		300	kHz
Ramp generator	f_R		300	kHz
Ambient temperature	T_A	−40	85	°C

[1]) With this, the max. power dissipation or junction temperature must be taken into account!
[2]) At a planned max. operating time of 70 000 hours a continuous max. junction temperature of 150°C is permitted.
[3]) For $V_{S\,ON}$ values refer to characteristic data.

Characteristics
$V_{S\,ON}$[1]) < V_S < 30 V; T_A = −40 to + 85°C

		Test conditions	Lower limit B	typ	Upper limit A	
Current consumption						
without load at V_{REF} QOP, QSIP 1, 2	I_S	C_T = 1 nF frequency generator with 100 kHz			20	mA
Standby operation	I_{St}				2	mA
Hysteresis at V_S						
Turn-on threshold for V_S rising	V_{SH}	$V_{on\text{-}THR} \geq V_{on\text{-}THR\,H}$		8.3	9.6	V
Turn-off threshold for V_S falling	V_{SL}			7.6		V
Reference voltage						
Voltage	V_{REF}	I_{REF} = 1 mA T_A = 25°C V_S = 15 V	2.475	2.5	2.525	V
Load current	$-I_{REF}$		0		3	mA
Voltage change	ΔV_{REF}	V_S ± 20%			10	mV
Voltage change	ΔV_{REF}	I_{REF} ± 20%			5	mV
Temperature response	$\Delta V_{REF}/\Delta T$		−0.3		+0.3	mV/K
Reponse threshold for I_{REF} overcurrent	I_{OV}			7		mA
Short-circuit current	I_{SC}	V_{REF} = 0 V		10		mA
Frequency generator (VCO)						
Frequency range	f_{VCO}				300	kHz
Frequency change	$\Delta f/fo$	V_S ± 20%			1	%
Tolerance	$\Delta f/fo$	C_T = 0.2 nF R_T = 50 kΩ T_A = 25°C	−5		+5	%

[1]) $V_{S\,ON}$ means that $V_{S\,HIGH}$ has been exceeded, while $V_{S\,LOW}$ has not yet been exceeded.

Characteristics

$V_{SON} < V_S < 30$ V; $T_A = -40$ to + 85°C

		Test conditions	Lower limit B	typ	Upper limit A	
Charging current for C_T (perm.) = current at pin R_T	I_{RT}	$I_{RT} = V_{REF/RT}$	0		1	mA
Discharging current for C_T	I_{dch}	internally fixed	2.1	3	3.9	mA
C_T range		[1]	0.2		1000	nF
Upper switching threshold	V_u			5		V
Lower switching threshold	V_l			2		V
Ramp generator						
Frequency range	f_R				300	kHz
Maximum voltage at C_R	V_{CRH}			5.5		V
Minimum voltage at C_R	V_{CRL}		1.7	1.8	1.9	V
Charging current for C_R (perm) = current at pin R_R	I_{ch}	V_{RR} approx. 0.7 V	0		3	mA
Discharging current for C_R	I_{dch}	internally fixed	2.8	4	5.2	mA
Ratio $I_{RR}/I_{CR\ charge}$		$I_{RR} = 0.5$ mA	0.95		1.05	
Comparator K1						
Input current	I_{IK1}				2	µA
Turn-off delay time[2] (signal transit time input K1 to QSIP)					500	ns
Common-mode input voltage range	V_{IC}		0		5.5	V

[1] $C_T = 0.2$ nF corresponds to a fall time of 0.2 µs (±30%) if the discharge current largely exceeds the charge current. The fall time equals the minimum dead time at the output.

[2] Step function $\Delta V = -100$ mV ⎍⎺ $\Delta V = +100$ mV, for transit time from input comparator to QSIP

Characteristics
$V_{SON} < V_S < 30$ V; $T_A = -40$ to $+85$°C

		Test conditions	Lower limit B	typ	Upper limit A	
Operational amplifier						
Open-loop voltage gain	G_{VO}		60	80		dB
Input offset voltage	V_{IO}	Pin 10 n.c.	−10		+10	mV
Input current	$-I_{I\,op\,amp}$				2	µA
Common-mode input voltage range	V_{IC}		0		4	V
Output current	$I_{Q\,op\,amp}$		0		2	mA
Output voltage range	$V_{Q\,op\,amp}$	0 mA$<I_Q<$2 mA	0.5		5.5	V
Transition frequency	f_T			3		MHz
Transition phase	φ_T			120		degrees
Temperature coefficient of V_{IO}	TC		−30		+30	µV/K
Source current at Q Op Amp	$I_{op\,amp}$	0.5 V$<V_Q<$5.5 V		120		µA
Soft start						
Charging current for $C_{soft\,start}$	$-I_{ch}$			6		µA
Discharging current for $C_{soft\,start}$	I_{dch}			2		µA
Upper limiting voltage	V_{lim}			5		V
Switching voltage of K 2	V_{K2}			1.5		V
Dynamic current limitation K5						
Input current	$-I_{I\,DYN}$				2	µA
Input offset voltage	V_{IO}		−10		+10	mV
Common-mode input voltage range	V_{IC}		0		V_S-3	V
Turn-off delay time[3])	t	Rated load 3 nF at QSIP		250	400	ns
Undervoltage K4						
Input current at K 4	$-I_{IK4}$				0.2	µA
Switching voltage at K 4	V_{sw}		V_{REF} −20 mV		V_{REF} +20 mV	V
Hysteresis current	I_{Hy4H}	$V_{(+K4)}$ V_{sw}	10	15	20	µA
	I_{Hy4L}	$V_{(+K4)}$ V_{sw}			0.1	µA
Turn-off delay time[2])	t				3	µs

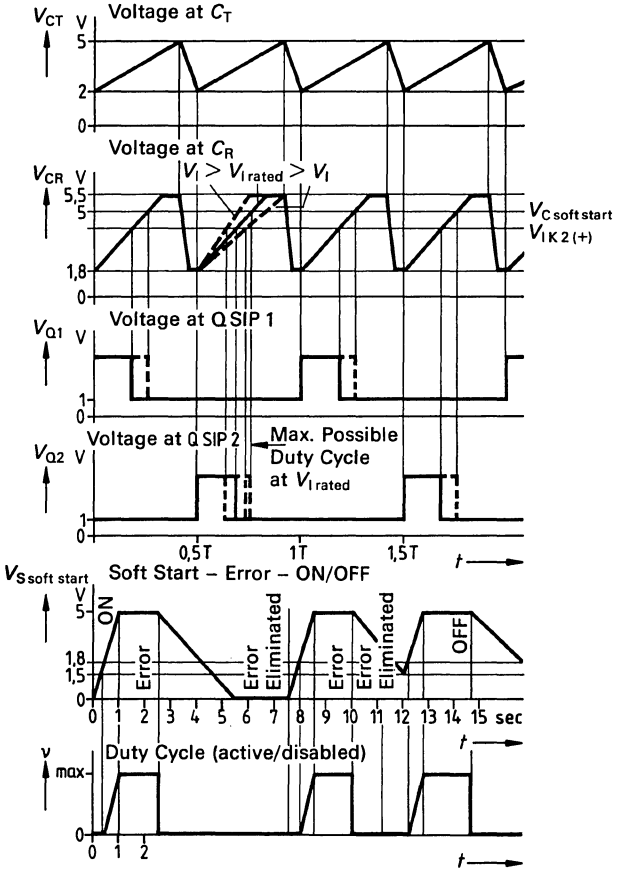
For footnotes refer to page 652.

Characteristics
$V_{SON} < V_S < 30$ V; $T_A = -40$ to $+85$°C

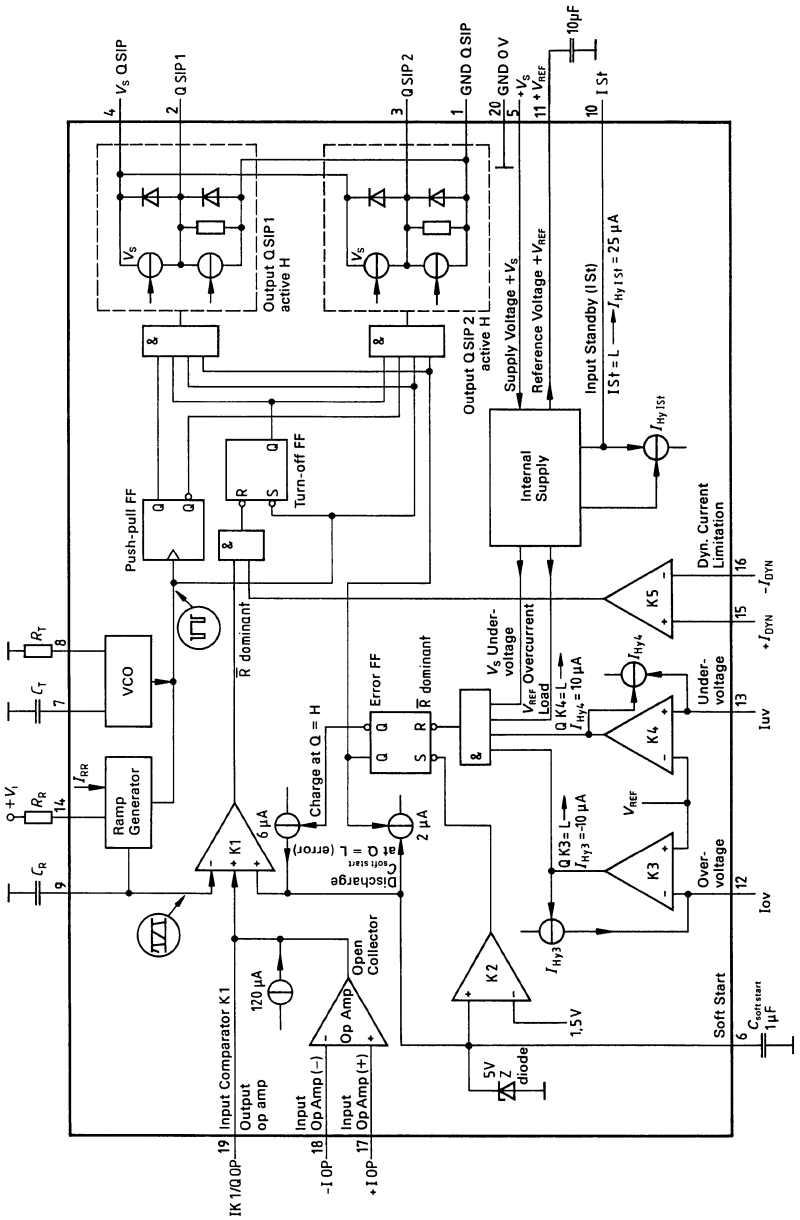
		Test conditions	Lower limit B	typ	Upper limit A	
Overvoltage K3						
Input current	$-I_{IK3}$				0.2	µA
Switching voltage	V_{Sw}		V_{REF} −20 mV		V_{REF} +20 mV	V
Turn-off delay time[2])	t				3	µs
Hysteresis current	$-I_{Hy3H}$	$V_{(-K3)} > V_{sw}$	7	10	13	µA
	$-I_{Hy3L}$	$V_{(-K3)} < V_{sw}$			0.1	µA
Output driver QSIP 1, 2						
Output voltage high	V_{QH}	$I_{QSIP} = -300$ mA	$V_S - 3$			V
Output voltage low	V_{QL}	$I_{QSIP} = +300$ mA			1.8	V
	V_{QL}	$I_{QSIP} = +10$ mA			1.4	V
Output current	I_{QSIP}	[1])	500	700	1000	mA
	$-I_{QSIP}$	[1])	300			mA
Input standby I St						
Turn-on threshold for V_{ISt} rising	V_{IStH}	$V_S > V_{SON}$	6.3	6.9	7.5	V
Turn-off threshold for V_{ISt} falling	V_{IStL}		5.6	6.2	6.8	V
Hysteresis current	$-I_{HyStH}$	$V_{ISt} > V_{IStH}$			5	µA
	I_{HyStL}	$V_{ISt} < V_{IStL}$	18	25	32	µA

[1]) Dynamic maximum current during rising of falling edge
[2]) Step function $V_{REF} = -100$ mV ⌐→ $V_{REF} = +100$ mV } for transit time from
[3]) Step function $\Delta V = -100$ mV ⌐→ $\Delta V = +100$ mV } input comparator to QSIP

Pulse diagram



Block diagram

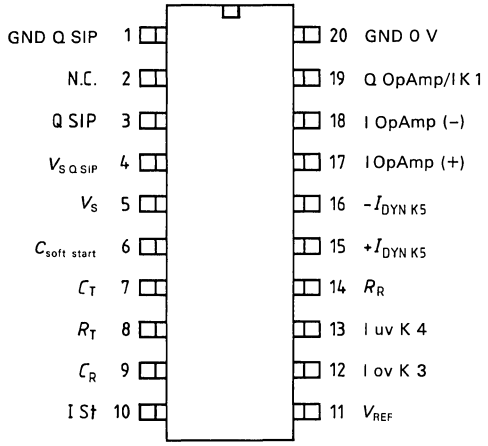


Preliminary data

SO 20L

This versatile single-phase switched-mode power supply control IC for the direct control of SIPMOS power transistors comprises digital and analog functions. These functions are required in the design of high quality flyback, forward, and choke converters with switching frequencies up to 300 kHz. The IC can also be used for single-ended voltage multipliers and speed-controlled motors. Malfunctions in the electrical operation of the switched-mode power supply are recognized by the comparators in the SMPS IC and activate protective functions.

Pin configuration
(top view)



Pin names

Pin no.	Function
1	GND Q SIP
2	N.C.
3	SIPMOS driver Q SIP
4	Supply voltage $V_{S\,Q\,SIP}$
5	Supply voltage V_S
6	Soft start $C_{soft\ start}$
7	VCO C_T
8	VCO R_T
9	Ramp generator C_R
10	Input standby I St
11	Reference voltage V_{REF}
12	Input overvoltage K 3
13	Input undervoltage K 4
14	Ramp generator R_R
15	Input dynamic current limitation (+) K 5
16	Input dynamic current limitation (–) K 5
17	Input operational amplifier (+)
18	Input operational amplifier (–)
19	Output operational amplifier/input comparator K1
20	GND 0 V

Circuit description

The various functional units of the component and their interaction are described in the following.

Supply voltage V_S

The IC enables the output not before the turn-on threshold ($V_{S\,ON}$) at V_S is exceeded. The duty cycle (active time/disable time) at the output can then rise from zero to the value set with K1 in the time specified by the soft start.

An undervoltage at the standby input causes the current consumption I_S to remain at the very low standby current level independent of the voltage V_S.

Voltage controlled oscillator (VCO)

The VCO is connected with the capacitor C_T and the resistor R_T. The charge current at C_T flows continuously and is set with resistor R_T. The discharge current is active during the discharge of C_T and is set internally.

In the typical mode of operation the duration of the rising edge is considerably greater than that of the falling edge. During the falling edge the VCO passes a trigger signal to the ramp generator thus discharging the ramp generator capacitance. Additionally, the trigger signal is routed to other parts of the IC.

Ramp generator

The ramp generator is controlled by the VCO and operates at the same frequency as the VCO. The duration of the ramp generator falling edge must be shorter than the VCO fall time. Only then do the ramp generator upper and lower switching levels reach their rated values.

To control the pulse width at the output, the voltage of the ramp generator rising edge is compared with an externally adjustable dc voltage at comparator K1. The slope of the rising edge is adjusted via the current by means of R_R. This provides the possibility of an additional superimposed control of the output duty cycle. This control capability (feed-forward control) permits the compensation of known interference (e.g. input voltage ripple). A superimposed load current control **(current mode control)** however, can also be implemented.

Comparator K1 (duty cycle control)

The two plus inputs of the comparator are switched such that the lower plus level is always compared with the level of the minus input. As soon as the voltage of the rising sawtooth edge (minus input) exceeds the lower level of the two plus inputs, the output is disabled via the turn-off flipflop. The "high"-duration of the output can thus be infinitely varied. As the frequency remains constant, this process corresponds to a change in duty cycle.

Operational amplifier (Op Amp)

The op amp is a high quality operational amplifier. It can be used in the control circuit to transmit the amplified variations of the voltage to be regulated to the free plus input of comparator K1. A voltage change is thus converted to a duty cycle change.

Turn-off flipflop

The falling edge of the VCO causes a pulse at the turn-off flipflop set input. It can, however, only be actually set if no reset signal is pending. With the turn-off flipflop set, the output is enabled and can be active. Upon an error signal from K 5 or upon a turn-off signal from K 1 the flipflop disables the output.

Z diode

The Z diode limits the voltage at capacitor $C_{\text{soft start}}$ to a maximum of 5 V. The ramp generator voltage can reach 5.5 V. For an appropriate slope of the rising ramp generator edge, the duty cycle can be limited to a desired maximum value. This can be a possible advantage in flyback converter operation.

Comparator K 2

The comparator has its switching threshold at 1.5 V at the plus input, and with its output sets the error flipflop if the voltage at capacitor $C_{\text{soft start}}$ is below 1.5 V. The error flipflop, however, will only accept the set pulse if no reset pulse (error) is pending. This prevents a restart of the output as long as an error signal is pending.

Soft start

The lower of the two voltages at the K 1 plus inputs – compared with the ramp generator voltage – is a measure for the duty cycle at the output. At component turn-on, the voltage at capacitor $C_{\text{soft start}}$ is equal to 0 V. As long as no error exists, the capacitor will be charged to the maximum value of 5 V with a current of 6 µA.

In the case of an error, $C_{\text{soft start}}$ is discharged with a current of 2 µA. The output, however, is immediately disabled by the error flipflop. Below a charge voltage of 1.5 V, a set signal is pending at the error flipflop and the output is enabled if no reset signal is pending at the same time. As the minimum ramp generator voltage, however, is 1.8 V, the duty cycle at the outputs is actually only increased slowly and continuously after the voltage at $C_{\text{soft start}}$ exceeds 1.8 V.

Error flipflop

Error signals, routed to the error flipflop reset input, cause an immediate disabling of the output (low), and after elimination of the error, a restart of the component by soft start.

Comparators K 3 (overvoltage), V_{REF} overcurrent, V_{S} undervoltage

These are error detectors that on error, cause the error flipflop to immediately disable the output. After elimination of the error, the duty cycle is raised again using the soft start. Upon overvoltage, a current is impressed at the inputs of K 3 and K 4, that can be used to enable an adjustable hysteresis or a holding function.

Comparator K4 (undervoltage)

Comparator K4 switches with an adjustable hysteresis. The value of the hysteresis is derived from the internal resistance of the external control source and the current impressed internally at the input of K4. In the undervoltage case, the set current flows into the component in the technical direction of current flow.

In the error case (undervoltage), the output is disabled. The component restarts by soft start.

Comparator K5 (dynamic current limiter)

K5 serves to recognize overcurrents at the switching transistor. Both inputs of the comparator are externally accessible. After elimination of the error, the output is enabled with the VCO trigger pulse at the turn-off flipflop. The delay time between occurrence of an error and disabling of the output is only approximately 250 ns.

Standby input (I St)

This input switches with voltage and current hysteresis. The voltage levels for switching from standby to active operation can be set with an external voltage divider between V_S – standby input – ground.

Reference voltage (V_{REF})

The reference voltage source is a highly constant source with regard to its temperature behavior. It can be used for the external wiring of the op amp; the error comparators, the ramp generator, or other external components.

SIPMOS driver output (Q SIP)

The output is active high. The duration during which the output is active, can be varied infinitely. The duration of the falling edge at the frequency generator is equal to the minimum duration during which the output is low (dead time).

The output driver is designed as a push-pull stage. The output current is internally limited to the specified values.

A 10 kΩ resistor is connected between the output and ground. This resistor holds the SIPMOS transistor reliably disabled during standby operation (undervoltage at I St.)

Output Q SIP is connected with the supply voltage V_{SQSIP} and with ground via diodes.

The diode connected to V_{SQSIP} routes the capacitive shift currents from the SIPMOS transistor gate to the filter capacitor at V_{SQSIP} during turning on the SMPS supply voltage. The voltage at V_{SQSIP} can reach approximately 2.3 V without the SIPMOS transistor being turned on.

The diode connected to ground connects negative voltages at Q SIP to –0.7 V. This provides an unimpeded flow off of capacitive currents occurring during voltage breakdown at the SIPMOS transistor drain connection.

For supply voltages starting at approx. 2 V, the output is active low in the disabled state. The function of the diode connected to V_{SQSIP} is then taken over by the pull-down source.

Maximum ratings

		Lower limit B	Upper limit A	
Supply voltage				
Inputs K 1, Op Amp, K 3, K 4, K 5, I St	V_S	−0.3	33	V
Frequency generator (VCO)				
Voltage at R_T/C_T	V_{CT}, V_{RT}	−0.3	6	V
$V_{CT} > 6$ V	I_{CT}		3	mA
Ramp generator				
Voltage at C_R/R_R	V_{CR}, V_{RR}	−0.3	6	V
Reference voltage	V_{REF}	−0.3	6	V
Output Op Amp	$V_{Q\,op\,amp}$	−0.3	6	V
$V_{Q\,op\,amp} > 6$ V	$I_{Q\,op\,amp}$		2	mA
Driver output QSIP[1])	V_{QSIP}	−0.3	V_S	V
QSIP clamp diodes at QSIP	I_{QSIP}	−10	10	mA
$V_{QSIP} > V_S$ or $V_{QSIP} < -0.3$ V				
Soft start	$V_{C\,soft\,start}$	−0.3	6	V
$V_{C\,soft\,start} > 6$ V	$I_{C\,soft\,start}$		100	µA
Junction temperature	T_j		125	°C
Storage temperature	T_{stg}	−65	125	°C
Thermal resistance (system-air) (SO-20 L)	$R_{th\,SA}$		90	K/W
Operating range				
Supply voltage[2])	V_S	$V_{S\,ON}$	30	V
Driver current at QSIP	I_{QSIP}	−1000	+300	mA
Take P_{max} into account!				
Frequency generator (VCO)	f_{VCO}		300	kHz
Ramp generator	f_R		300	kHz
Ambient temperature	T_A	−40	85	°C

[1]) With this, the max. power dissipation or junction temperature must be taken into account.
[2]) For $V_{S\,ON}$ values refer to characteristic data.

Characteristics
$V_{S\,ON}$[1]) < V_S < 30 V; T_A = −40 to + 85°C

		Test conditions	Lower limit B	typ	Upper limit A	
Current consumption						
without load at V_{REF} DOP, DSIP	I_S	C_T = 1 nF frequency generator with 100 kHz			20	mA
Standby operation	I_{St}				2	mA
Hysteresis at V_S						
Turn-on threshold for V_S rising	V_{SH}	$V_{on\text{-}THR} \geq V_{on\text{-}THR\,H}$		8.3	9.6	V
Turn-off threshold for V_S falling	V_{SL}			7.6		V
Reference voltage						
Voltage	V_{REF}	I_{REF} = 1 mA T_A = 25°C V_S = 15 V	2.475	2.5	2.525	V
Load current	$-I_{REF}$		0		3	mA
Voltage change	ΔV_{REF}	$V_S \pm 20\%$			10	mV
Voltage change	ΔV_{REF}	$I_{REF} \pm 20\%$			5	mV
Temperature response	$\Delta V_{REF}/\Delta T$		−0.3		+0.3	mV/K
Reponse threshold for I_{REF} overcurrent	I_{OV}			7		mA
Short-circuit current	I_{SC}	V_{REF} = 0 V		10		mA

[1]) $V_{S\,ON}$ means that $V_{S\,HIGH}$ has been exceeded, while $V_{S\,LOW}$ has not yet been exceeded.

Characteristics

$V_{SON} < V_S < 30$ V; $T_A = -40$ to $+85$°C

		Test conditions	Lower limit B	typ	Upper limit A	
Frequency generator (VCO)						
Frequency range	f_{VCO}				300	kHz
Frequency change	$\Delta f/fo$	$V_S \pm 20\%$			1	%
Tolerance	$\Delta f/fo$	$C_T = 0.2$ nF $R_T = 50$ kΩ $T_A = 25$°C	−5		+5	%
Charging current for C_T (perm.) = current at pin R_T	I_{RT}	$I_{RT} = V_{REF/RT}$	0		1	mA
Discharging current for C_T	I_{dch}	internally fixed	2.1	3	3.9	mA
C_T range		[1]	0.2		1000	nF
Upper switching threshold	V_u			5		V
Lower switching threshold	V_l			2		V
Ramp generator						
Frequency range	f_R				300	kHz
Maximum voltage at C_R	V_{CRH}			5.5		V
Minimum voltage at C_R	V_{CRL}		1.7	1.8	1.9	V
Charging current for C_R (perm) = current at pin R_R	I_{ch}	V_{RR} approx. 0.7 V	0		3	mA
Discharging current for C_R	I_{dch}	internally fixed	2.8	4	5.2	mA
Ratio $I_{RR}/I_{CR\ charge}$		$I_{RR} = 0.5$ mA	0.95		1.05	
Comparator K1						
Input current	I_{IK1}				2	µA
Turn-off delay time[2] (signal transit time input K1 to QSIP)					500	ns
Common-mode input voltage range	V_{IC}		0		5.5	V

[1] $C_T = 0.2$ nF corresponds to a fall time of 0.2 µs (± 30%) if the discharge current largely exceeds the load current. The fall time equals the minimum dead time at the output.

[2] Step function $\Delta V = -100$ mV ⌐→ $\Delta V = +100$ mV, for transit time from input comparator to QSIP

Characteristics

$V_{SON} < V_S < 30$ V; $T_A = -40$ to $+85$°C

		Test conditions	Lower limit B	typ	Upper limit A	
Operational amplifier						
Open-loop voltage gain	G_{VO}		60	80		dB
Input offset voltage	V_{IO}	Pin 10 n.c.	−10		+10	mV
Input current	$-I_{I\,op\,amp}$				2	µA
Common-mode input voltage range	V_{IC}		0		4	V
Output current	$I_{Q\,op\,amp}$		0		2	mA
Output voltage range	$V_{Q\,op\,amp}$	$0\,mA < I_Q < 2\,mA$	0.5		5.5	V
Transition frequency	f_T			3		MHz
Transition phase	φ_T			120		degrees
Temperature coefficient of V_{IO}	TC		−30		+30	µV/K
Source current at Q Op Amp	$I_{op\,amp}$	$0.5\,V < V_Q < 5.5\,V$		120		µA
Soft start						
Charging current for $C_{soft\,start}$	$-I_{ch}$			6		µA
Discharging current for $C_{soft\,start}$	I_{dch}			2		µA
Upper limiting voltage	V_{lim}			5		V
Switching voltage of K 2	V_{K2}			1.5		V
Dynamic current limitation K 5						
Input current	$-I_{I\,DYN}$				2	µA
Input offset voltage	V_{IO}		−10		+10	mV
Common-mode input voltage range	V_{IC}		0		$V_S - 3$	V
Turn-off delay time[3])	t	Rated load 3 nF at Q SIP		250	400	ns
Undervoltage K 4						
Input current at K 4	$-I_{IK4}$				0.2	µA
Switching voltage at K 4	V_{sw}		V_{REF} −20 mV		V_{REF} +20 mV	V
Hysteresis current	I_{Hy4H} I_{Hy4L}	$V_{(+K4)} < V_{sw}$ $V_{(+K4)} > V_{sw}$	10	15	20 0.1	µA µA
Turn-off delay time[2])	t				3	µs

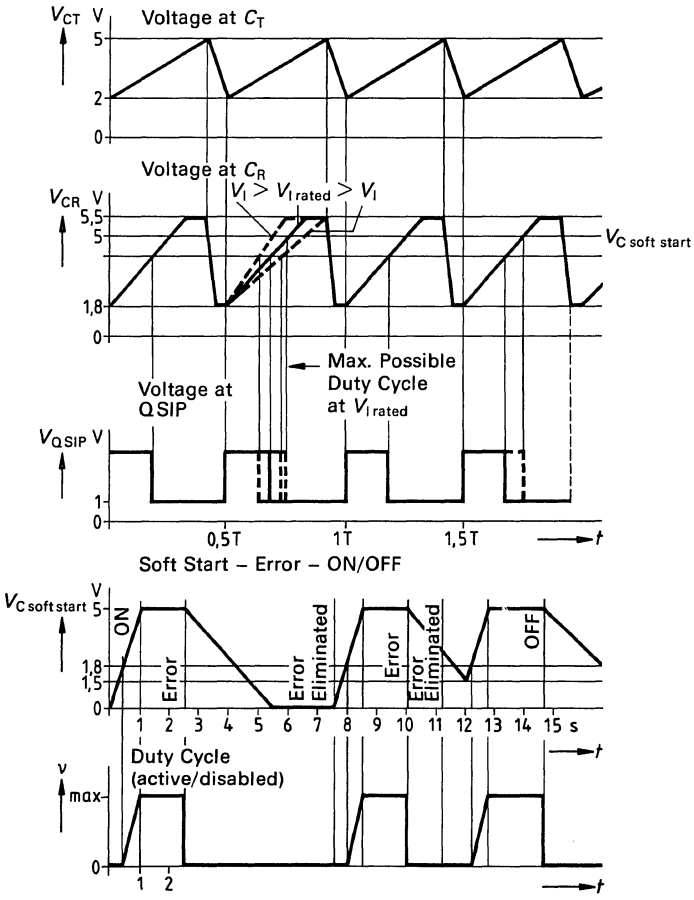
For footnotes refer to page 666.

Characteristics
$V_{SON} < V_S < 30$ V; T_A = −40 to +85°C

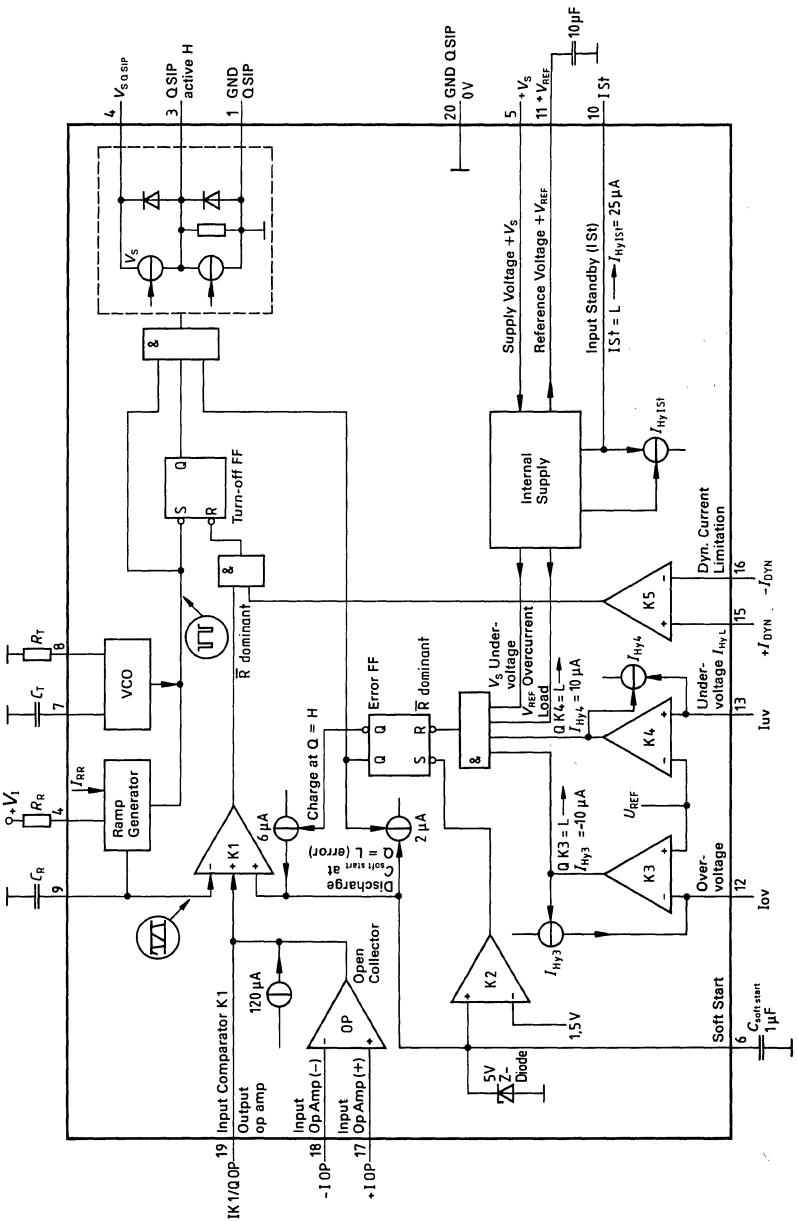
		Test conditions	Lower limit B	typ	Upper limit A	
Overvoltage K3						
Input current	$-I_{IK3}$				0.2	µA
Switching voltage	V_{sw}		V_{REF} −20 mV		V_{REF} +20 mV	V
Turn-off delay time[2])	t				3	µs
Hysteresis current	$-I_{Hy3H}$	$V_{(-K3)} > V_{sw}$	7	10	13	µA
	$-I_{Hy3L}$	$V_{(-K3)} < V_{sw}$			0.1	µA
Output driver QSIP						
Output voltage high	V_{QH}	$I_{QSIP} = -300$ mA	$V_S - 3$			V
Output voltage low	V_{QL}	$I_{QSIP} = +300$ mA			1.8	V
	V_{QL}	$I_{QSIP} = +10$ mA			1.4	V
Output current	I_{QSIP}	$C_{QSIP} = 10$ nF	500	700	1000	mA[1])
	$-I_{QSIP}$		300			mA[1])
Input standby ISt						
Turn-on threshold for V_{ISt} rising	V_{IStH}	$V_S > V_{SON}$	6.3	6.9	7.5	V
Turn-off threshold for V_{ISt} falling	V_{IStL}		5.6	6.2	6.8	V
Hysteresis current	$-I_{HyStH}$	$V_{ISt} > V_{IStH}$			5	µA
	I_{HyStL}	$V_{ISt} < V_{IStL}$	18	25	32	µA

[1]) Dynamic maximum current during rising or falling edge
[2]) Step function V_{REF} = −100 mV ⌐→ V_{REF} = +100 mV ⎫ for transit time from
[3]) Step function ΔV = −100 mV ⌐→ ΔV = +100 mV ⎭ input comparator to QSIP

Pulse diagram



Block diagram



SIP 9

The TDA 4930 can be applied as a class B stereo amplifier or mono amplifier in bridge configuration for AF signals. In addition, the component is provided with a protective circuitry against overtemperature and overload.

Features

- Universal application as stereo amplifier or mono amplifier in bridge configuration
- Wide supply voltage range
- Minimum of external components
- Outputs AC and DC short-circuit resistant

Maximum ratings

Supply voltage	V_S	32	V
Output peak current	I_1; $I_{9\,pp}$	2.5	A
Input voltage range	V_2; V_3; V_7	−0.3 to V_S	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-case)	$R_{th\,JC}$	6	K/W

Operating range

Supply voltage			
$R_L \geq 8\ \Omega$	V_S	8 to 26	V
$R_L = 4\ \Omega$	V_S	8 to 22	V
Case temperature	T_C	−20 to 85	°C
$P_V = 10$ W			

Characteristics

$V_S = 19$ V; $T_A = 25$ °C

		Test circuit	min	typ	max	
Quiescent current ($V_i = 0$)	I_5	1		30	60	mA
Output voltage ($V_i = 0$)	$V_{q\,9;1}$	1	9	9.5	10	V
Input resistance[1]	$R_{i\,7;3}$	1		20		kΩ
Output power ($f = 1$ kHz)						
– stereo operation						
$THD = 1\%$	$P_{q\,9;1}$	1	7	8		W
$THD = 10\%$	$P_{q\,9;1}$	1	9	10		W
– bridge operation						
$THD = 1\%$	$P_{q\,9;1}$	2	14	16		W
$THD = 10\%$	$P_{q\,9;1}$	2	18	20		W
Line hum suppression[2] $f_r = 100$ Hz; $V_r = 0.5$ V	a_{hum}	1	40	46		dB
Current consumption $P_9 = P_1 = 10$ W; $f_i = 1$ kHz	I_5	1		1.5		A
Efficiency $P_9 = P_1 = 10$ W; $f_i = 1$ kHz	η	1		70		%
Total harmonic distortion $P_{9/1} = 0.05$ to 6 W $f_i = 40$ Hz to 15 kHz	THD	1		0.2	0.5	%
Cross-talk rejection $f_i = 1$ kHz; P_9 or $P_1 = 10$ W	a_{cr}	1		50		dB
Transmission range[3]	B	1	40 Hz to 60 kHz			
Disturbance voltage ($B = 30$ Hz to 20 kHz) in acc. with DIN 45405 referred to input[4]	V_d	1		5		μV
Noise voltage (CCIR filter) in accordance with DIN 45405 referred to the input[4]	V_n	1		15		μV_S
Difference in transmission measure $P_9 = P_1 = 7$ W $f_i = 40$ Hz to 20 kHz	ΔG_V	1			1	dB
Voltage gain stereo	G_V	1		30		dB
Voltage gain bridge configuration	G_V	2		36		dB
DC output voltage at active DC protection if S1/9 is closed; $V_S \geq 10$ V	$V_{q\,9;1}$	2		0.15	0.30	V

1) S2a(b) open/closed
2) S1a(b) and S3 in position 2
3) $P_{9/1} = 6$ W; –3 dB referred to 1 kHz
4) S1a(b) in position 2

Circuit description

The IC contains 2 complete amplifiers and can be used for a wide variety of applications with a minimum of external circuitry.

The TDA 4930 can be applied as stereo amplifier or amplifier in bridge configuration for operating voltages ranging between 8 V and 26 V, with speakerload impedance from 1 to 16 Ω.

The prestages are differential amplifiers with strong negative feedback. Internal frequency compensation in the driver amplifier limits the gain-bandwidth product to 4.5 MHz.

The power output stages are comprised of quasi PNP transistors (small saturation voltage).

Each power element is equipped with an independent protective circuit, rendering the outputs of the amplifiers AC and DC short-circuit resistant.

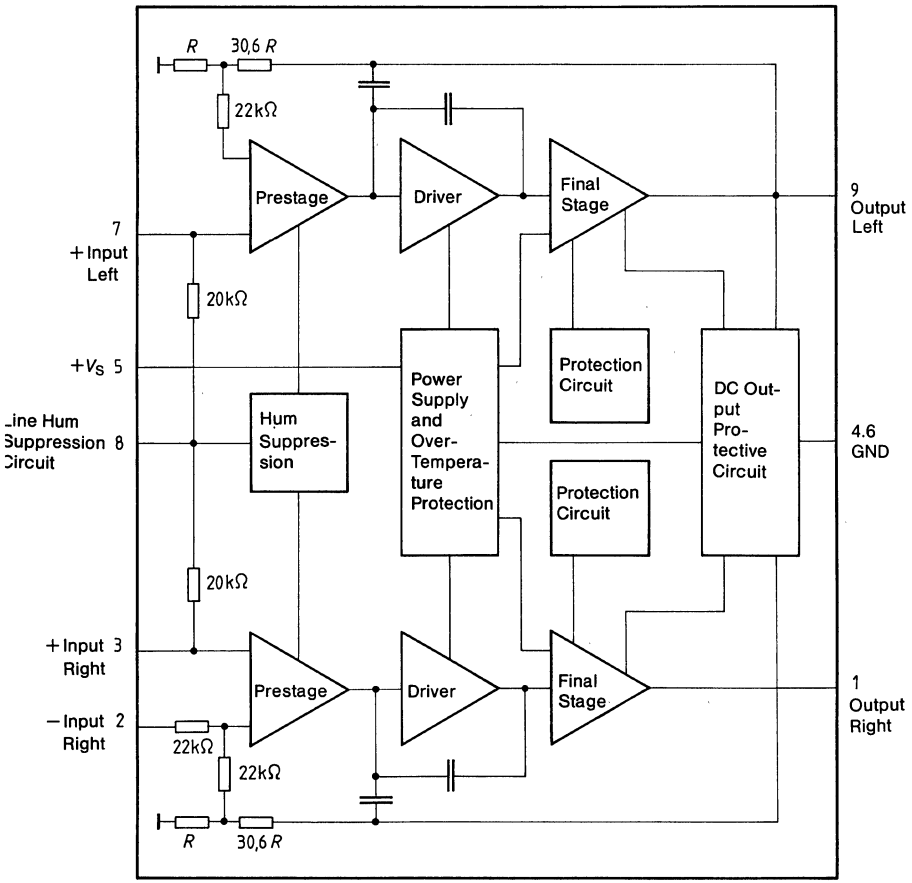
A DC protective circuit of the outputs prevents overloading of the loudspeakers, if ground connections become apparent during bridge operations. To avoid overheating, a temperature fuse affecting both amplifiers prevents current supply to the power output stages during inadmissibly high chip temperatures.

As a special economic feature, the negative feedback resistances for $G_V = 30$ dB and the input voltage reference divider have been integrated.

Pin description

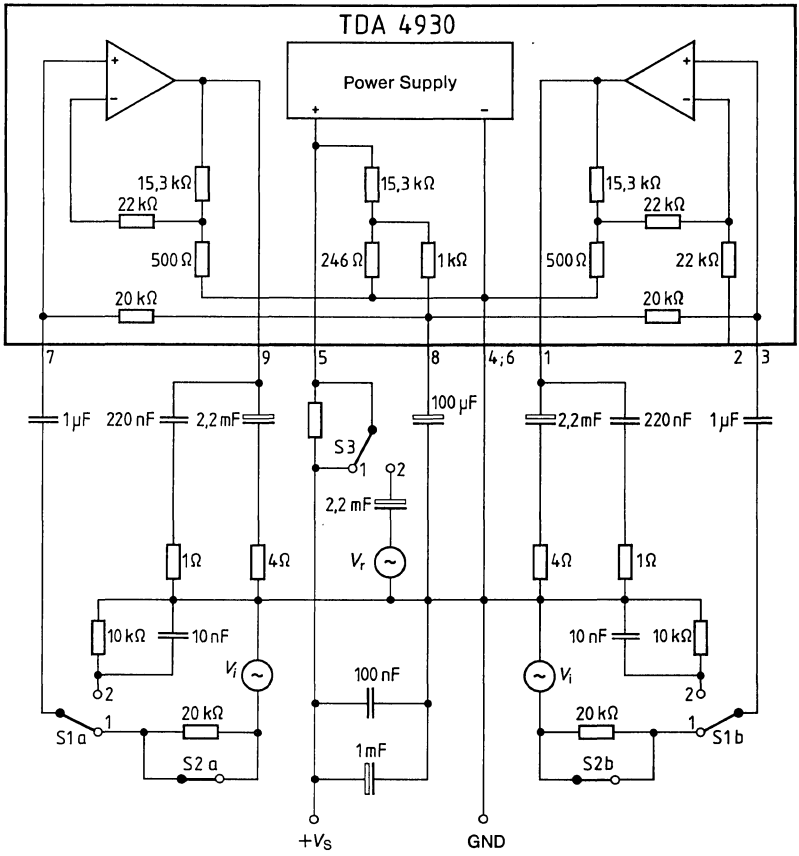
Pin	Function
1	Output right channel
2	Inverting input right channel (more than 22 kΩ)
3	Non-inverting input right channel
4	GND
5	$+V_S$
6	GND
7	Non-inverting input left channel
8	Line hum suppression right and left channel
9	Output left channel

Block diagram



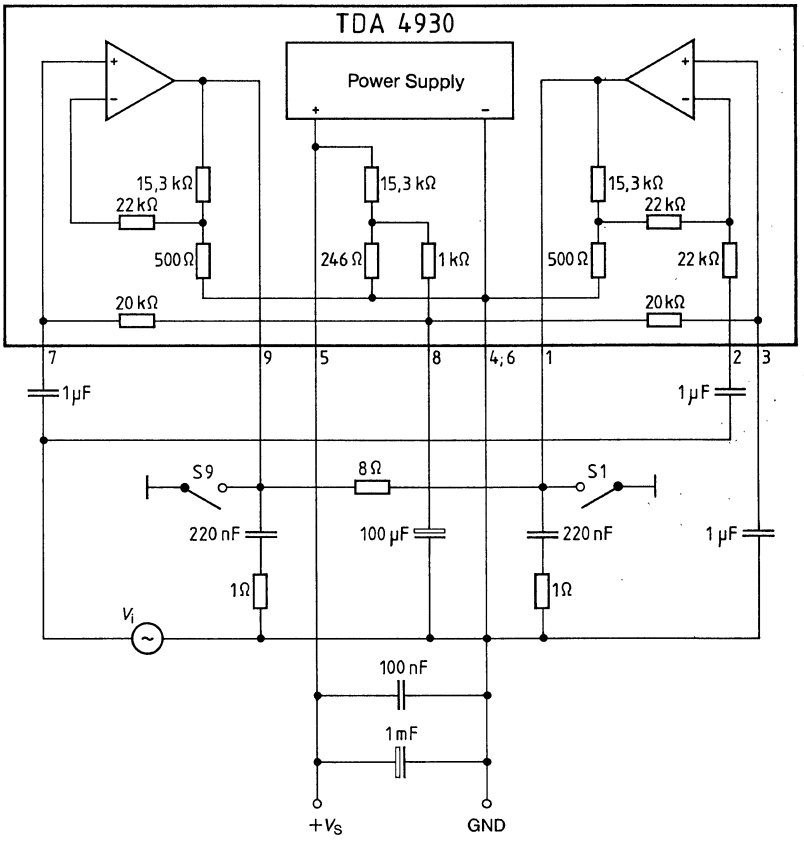
Test and measurement circuit

1. Stereo operation



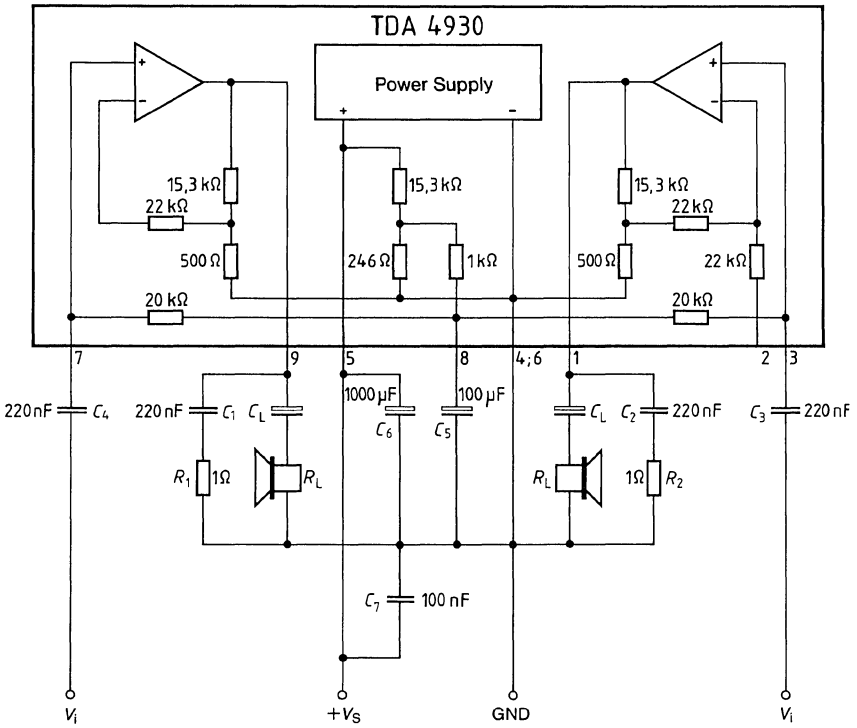
Test and measurement circuit

2. Bridge operation



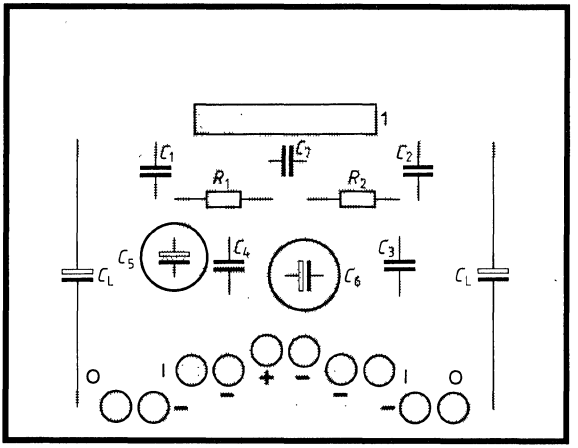
Application circuit

1. Stereo operation



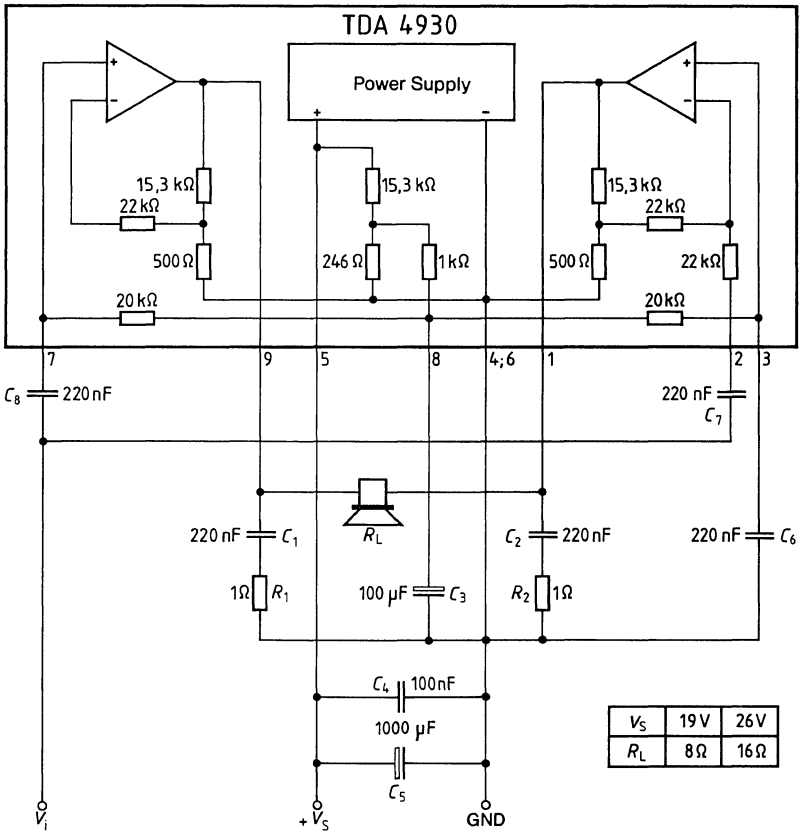
V_S	19 V	26 V
R_L	4Ω	8Ω
C_L	1000µF	470µF

Layout/Plug-in location plan



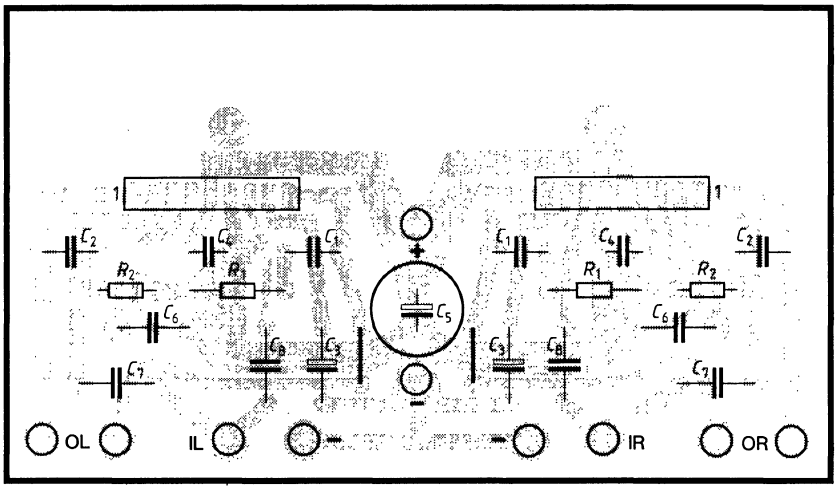
Application circuit

2. Bridge operation (only one channel)

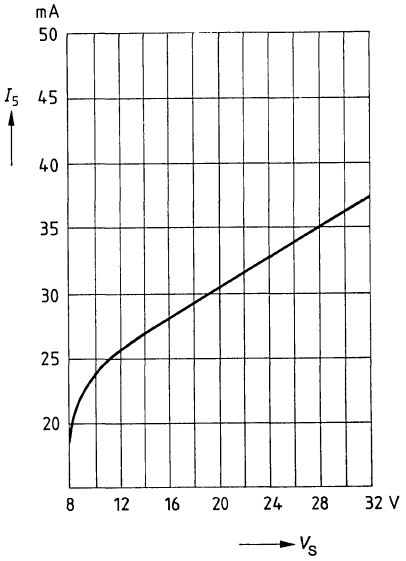


V_S	19 V	26 V
R_L	8 Ω	16 Ω

Layout/Plug-in location plan

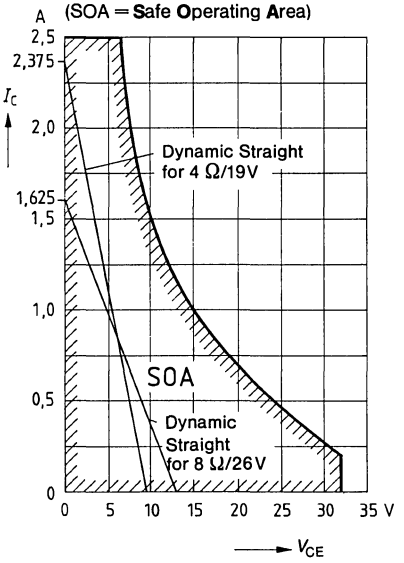


Quiescent current versus supply voltage



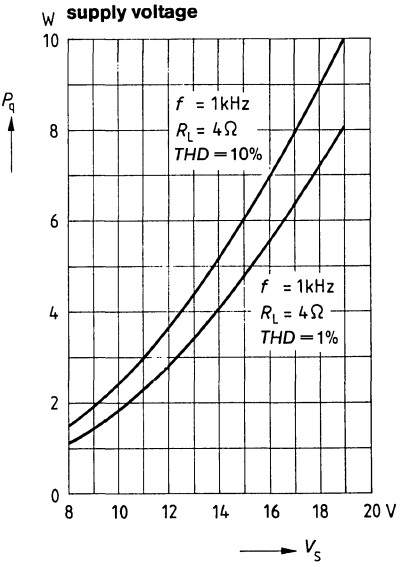
Typical operating range of the final transistors adjusted by internal protective circuits

(SOA = Safe Operating Area)



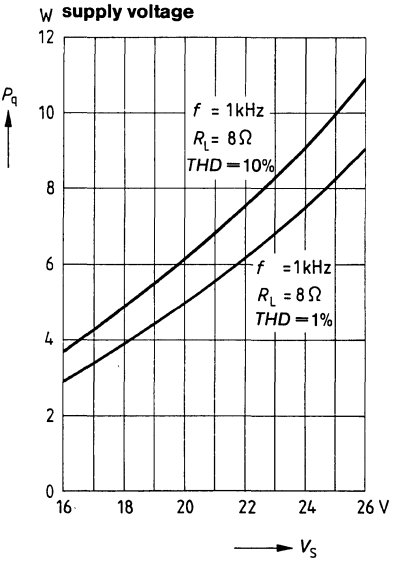
Stereo operation

Output power versus supply voltage



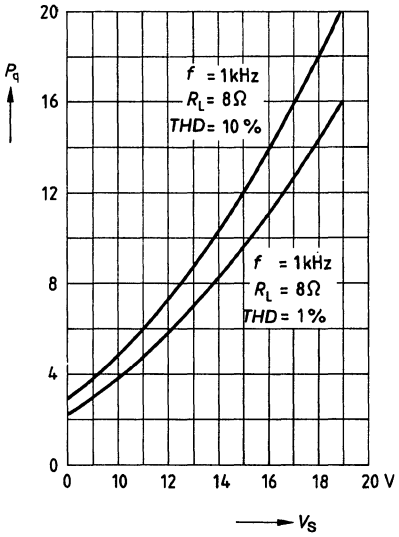
Stereo operation

Output power versus supply voltage



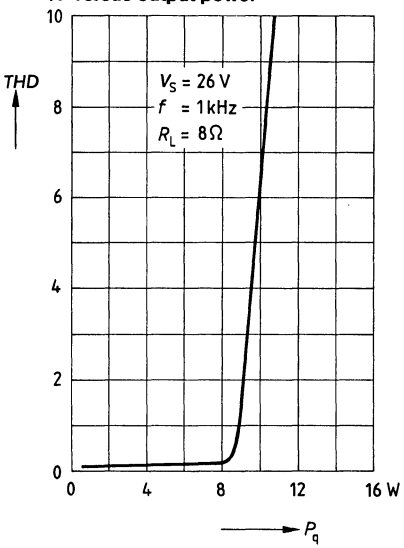
Bridge operation

Output power versus supply voltage



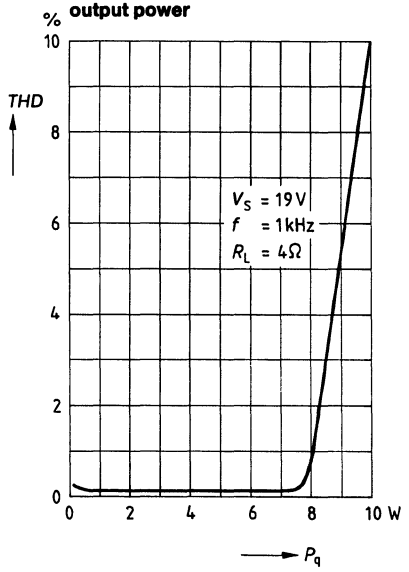
Stereo operation

Total harmonic distortion versus output power



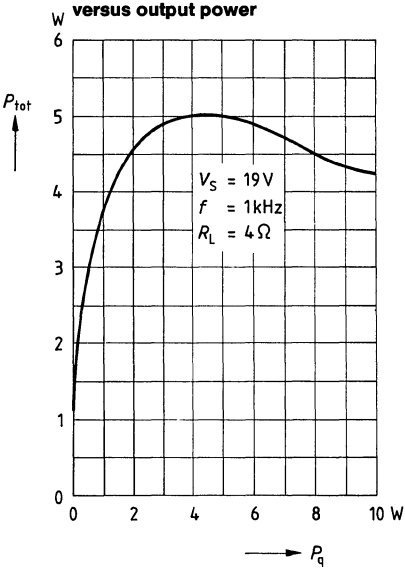
Stereo operation

Total harmonic distortion versus output power



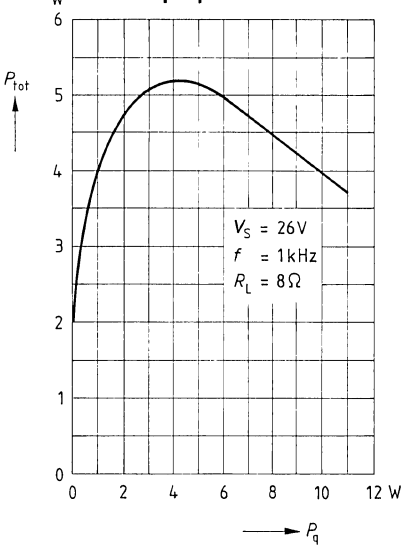
Stereo operation

Power dissipation (each channel) versus output power



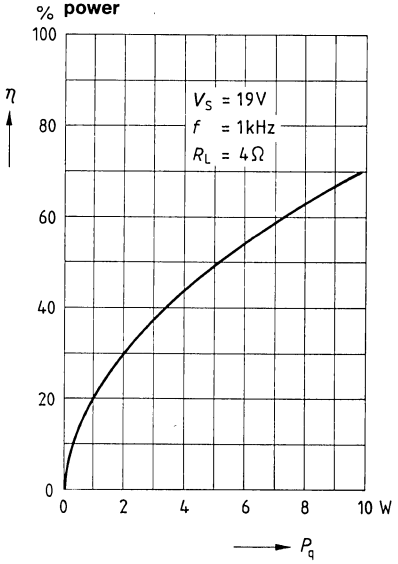
Stereo operation

Power dissipation (each channel) versus output power



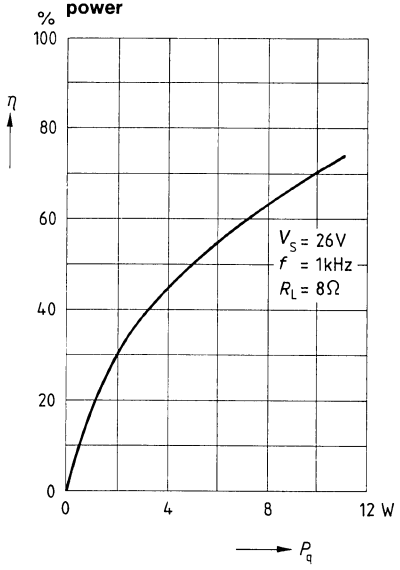
Stereo operation

Efficiency versus output power



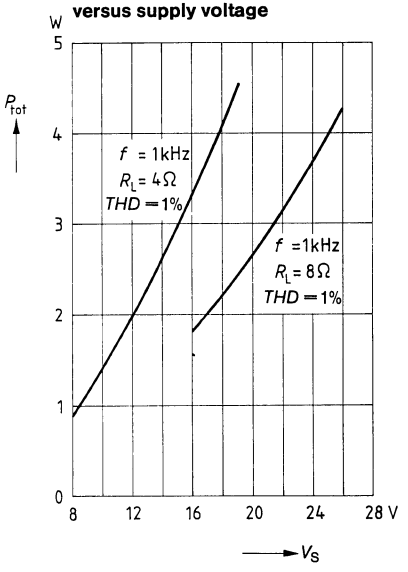
Stereo operation

Efficiency versus output power



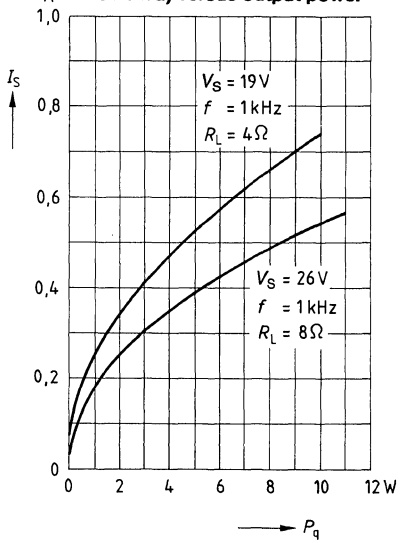
Stereo operation

Power dissipation (each channel) versus supply voltage



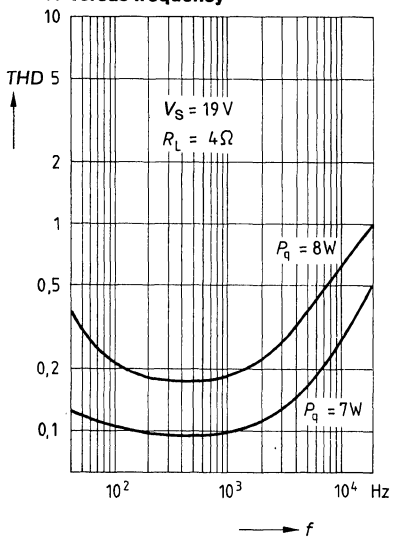
Stereo operation

Supply current (one channel modulated) versus output power

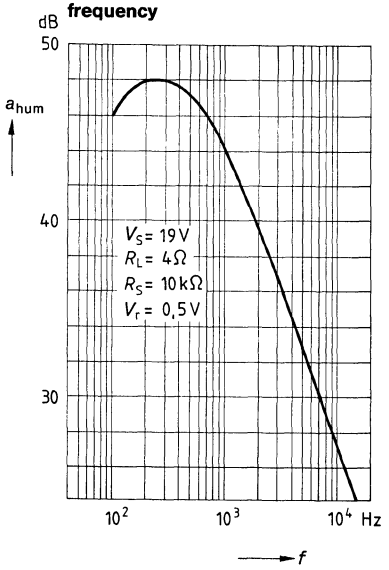


Stereo operation

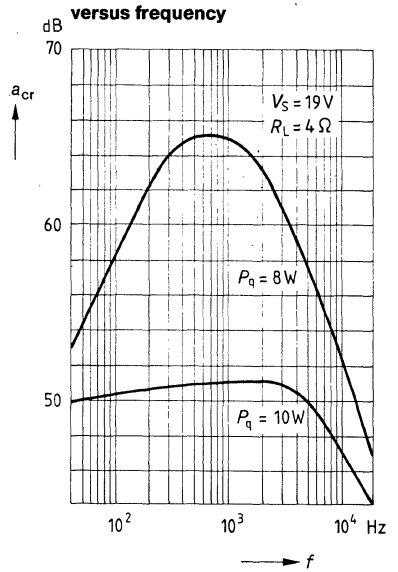
Total harmonic distortion % versus frequency



Line hum suppression versus frequency



Cross-talk rejection versus frequency



SIP 9

The TDA 4935 can be applied as a class B stereo amplifier or mono amplifier in bridge configuration for AF signals. In addition, the component is provided with a protective circuitry against overtemperature and overload.

Features

- Universal application as stereo amplifier or mono amplifier in bridge configuration
- Wide supply voltage range
- Minimum of external components

Maximum ratings

Supply voltage	V_S	32	V
Output peak current	I_1; I_9	2.8	A
Input voltage range	V_2; V_3; V_7	−0.3 to V_S	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-case)	$R_{th\,JC}$	4	K/W

Operating range

Supply voltage	V_S		
$R_L \geq 8\ \Omega$	V_S	8 to 30	V
$R_L = 4\ \Omega$	V_S	8 to 24	V
Case temperature	T_C	−20 to 85	°C
$P_V = 15$ W			

Characteristics

$V_S = 24$ V; $T_C = 25$ °C

		Test circuit	min	typ	max	
Quiescent current $V_i = 0$	I_5	1		40	80	mA
Output voltage $V_i = 0$	$V_{q1;9}$	1	11	12	13	V
Input resistance[1]	$R_{i3;7}$	1		20		kΩ
Output power $f = 1$ kHz						
– stereo operation						
$THD = 1\%$	$P_{q1;9}$	1	10	12		W
$THD = 10\%$	$P_{q1;9}$	1	13	15		W
– bridge operation						
$THD = 1\%$	$P_{q1;9}$	2	20	24		W
$THD = 10\%$	$P_{q1;9}$	2	26	30		W
Line hum suppression[2] $f_R = 100$ Hz; $V_R = 0.5$ V	a_{hum}	1	40	46		dB
Current consumption $P_9 = P_1 = 15$ W; $f_i = 1$ kHz	I_5	1		1.8		A
Efficiency $P_9 = P_1 = 10$ W; $f_i = 1$ kHz	η	1		70		%
Total harmonic distortion $P_{9/1} = 0.05 - 10$ W $f_i = 40$ Hz to 15 kHz	THD	1		0.2	0.5	%
Cross-talk rejection $f_i = 1$ kHz; P_9 or $P_1 = 15$ W	a_{cr}	1		50		dB
Transmission range[3]	B	1		40 Hz to 60 kHz		
Disturbance voltage (B = 30 Hz to 20 kHz) in acc. with DIN 45405 referred to input[4]	V_d	1		5		μV
Noise voltage (CCIR filter) in acc. with DIN 45405 referred to the input[4]	V_n	1		15		μV_S
Difference in transmission measure $P_9 = P_1 = 10$ W $f_i = 40$ Hz to 20 kHz	ΔG_V	1			1	dB
Voltage gain						
stereo	G_V	1		30		dB
bridge configuration	G_V	2		36		dB

[1] S2a (b) open/closed
[2] S1a (b) and S3 in position 2
[3] $P_{9/1} = 6$ W; −3 dB referred to 1 kHz
[4] S1a (b) in position 2

Circuit description

The IC contains 2 complete amplifiers and can be used for a wide variety of applications with a minimum of external circuitry.

The TDA 4935 can be applied as stereo amplifier or amplifier in bridge configuration for operating voltages ranging between 8 V and 26 V.

The prestages are differential amplifiers with strong negative feedback. Internal frequency compensation in the driver amplifier limits the gain-bandwidth product to 4.5 MHz.

The power output stages are comprised of quasi PNP transistors (small saturation voltage).

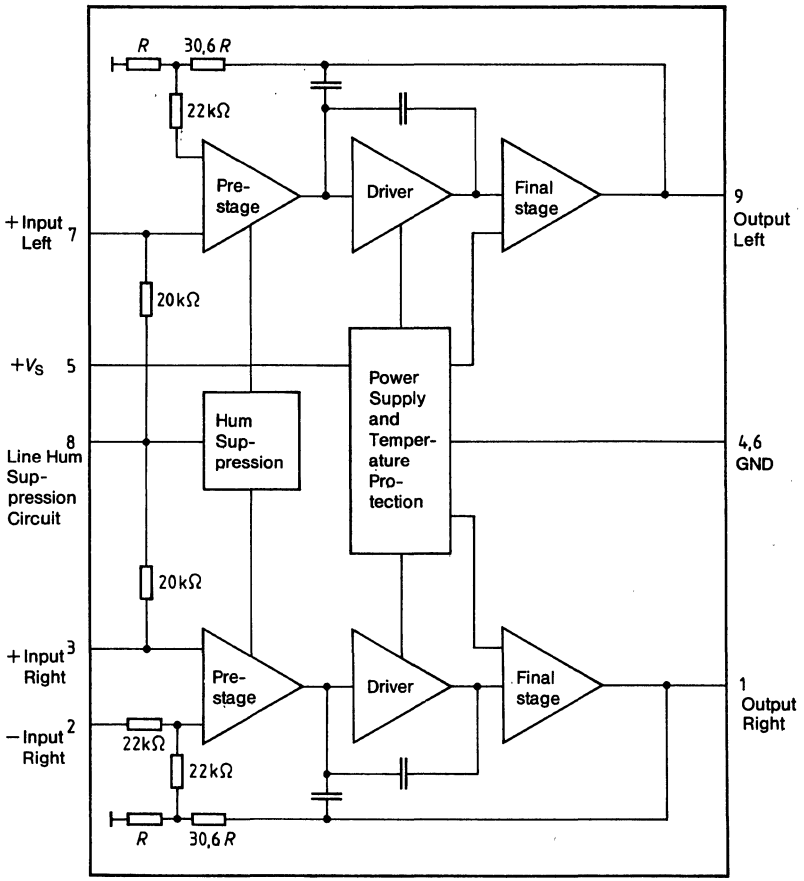
To avoid overheating, a temperature fuse affecting both amplifiers prevents current supply to the power output stages during inadmissibly high chip temperatures.

As a special economic feature, the negative feedback resistances for $G_V = 30$ dB and the input voltage reference divider have been integrated.

Pin description

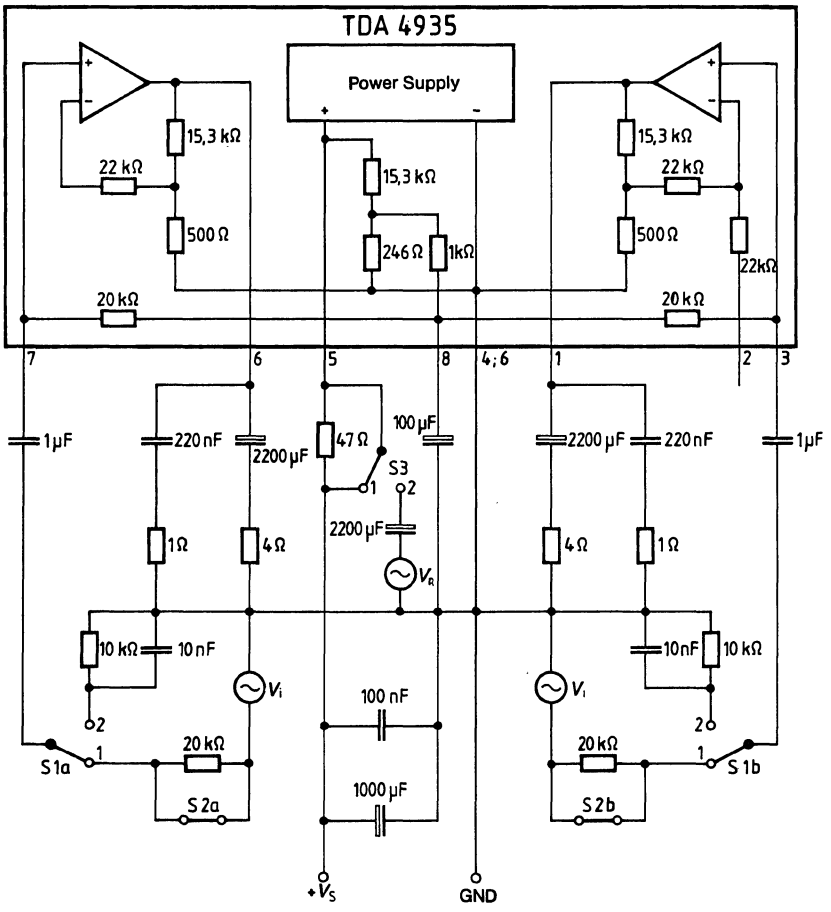
Pin	Function
1	Output right channel
2	Inverting input right channel (more than 22 kΩ)
3	Non-inverting input right channel
4	GND
5	$+V_S$
6	GND
7	Non-inverting input left channel
8	Line hum suppression right and left channel
9	Output left channel

Block diagram



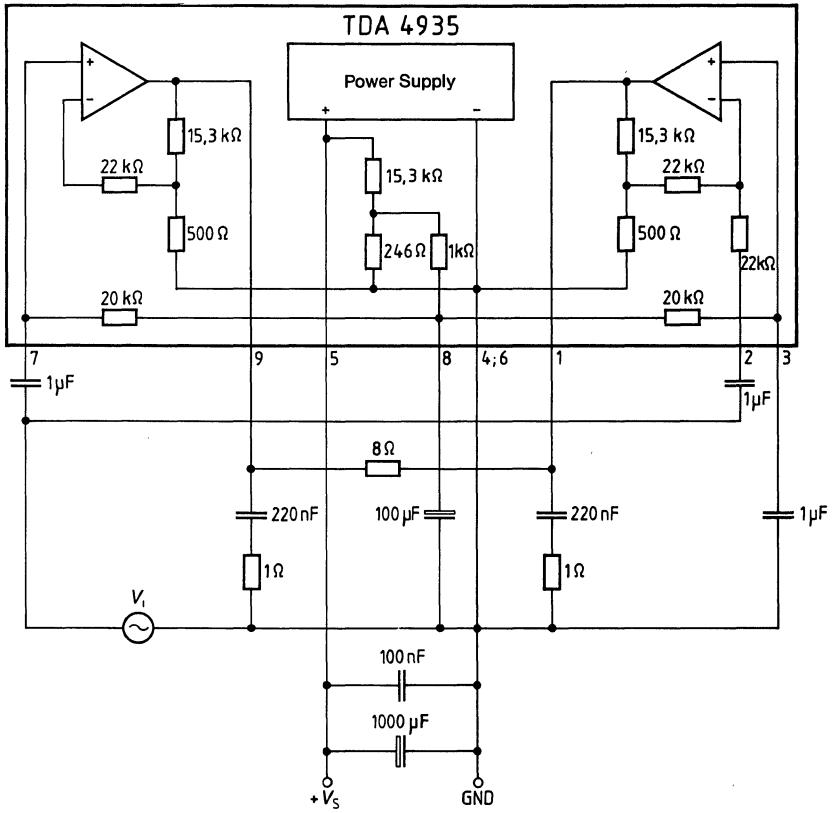
Test and measurement circuit

1. Stereo operation



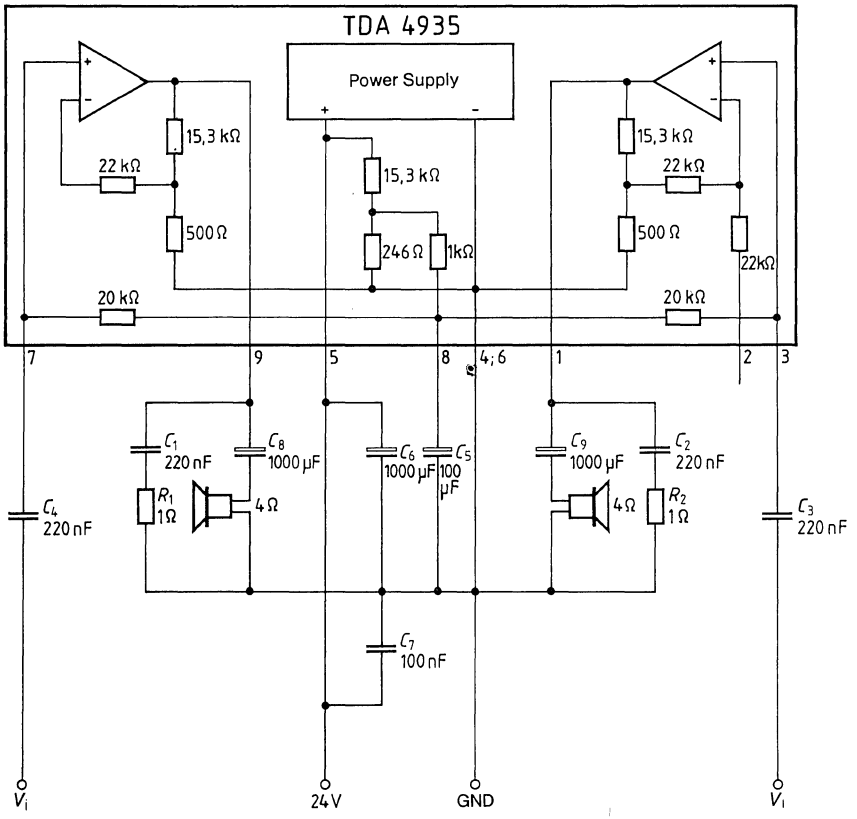
Test and measurement circuit

2. Bridge operation

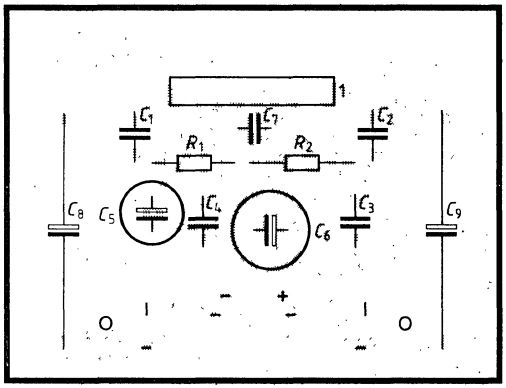


Application circuit

1. Stereo operation

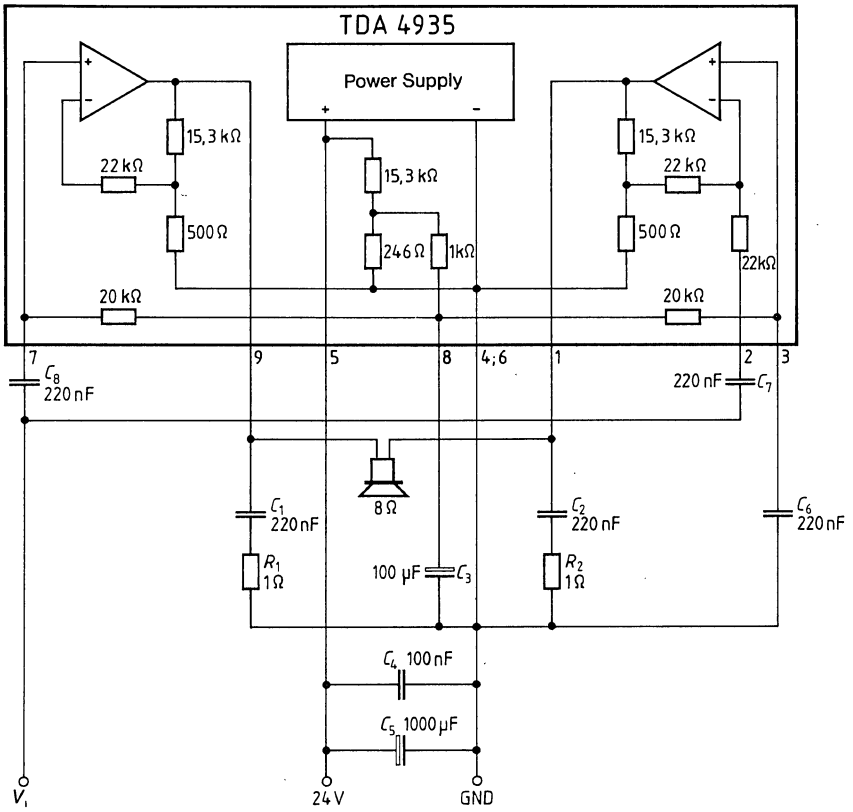


Layout/Plug-in location plan

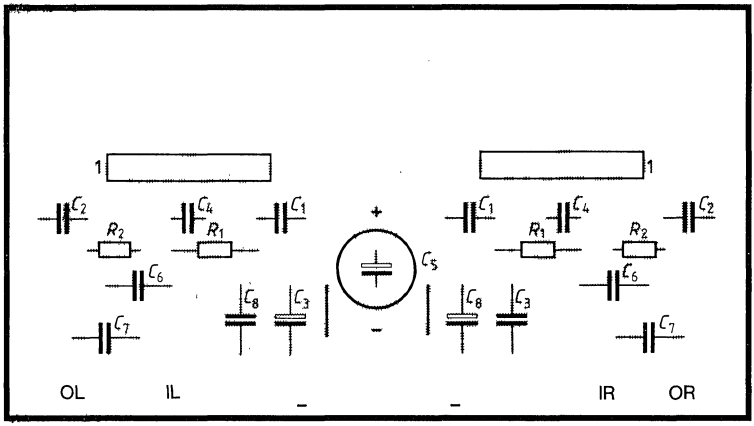


Application circuit

2. Bridge operation (only one channel)

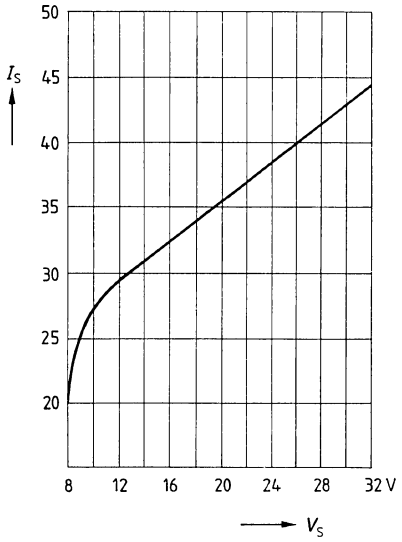


Layout/Plug-in location plan



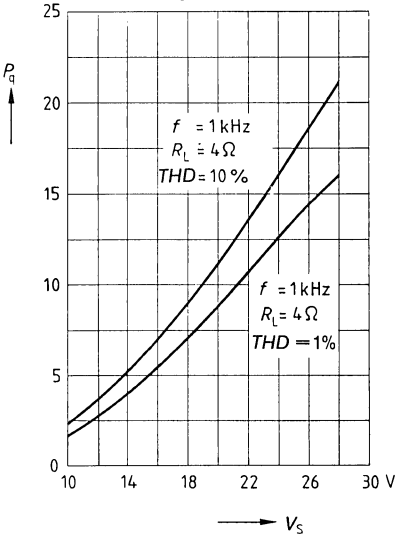
2 x 30W

Quiescent current versus supply voltage



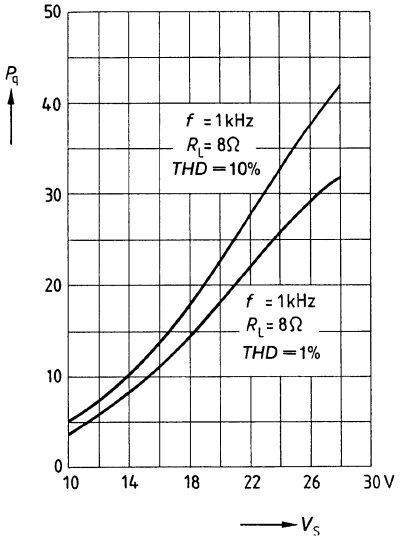
Stereo operation

Output power versus supply voltage



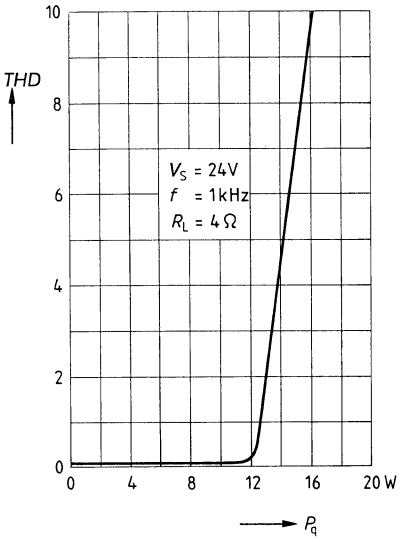
Bridge operation

Output power versus supply voltage



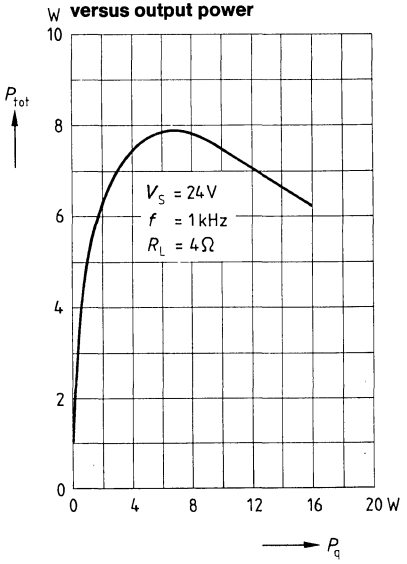
Stereo operation

Total harmonic distortion % versus output power



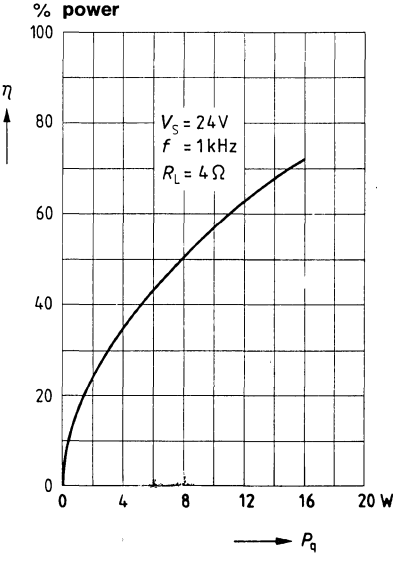
Stereo operation

Power dissipation (each channel) versus output power



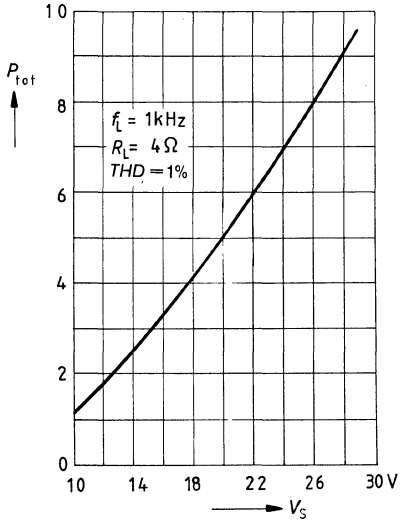
Stereo operation

Efficiency versus output power



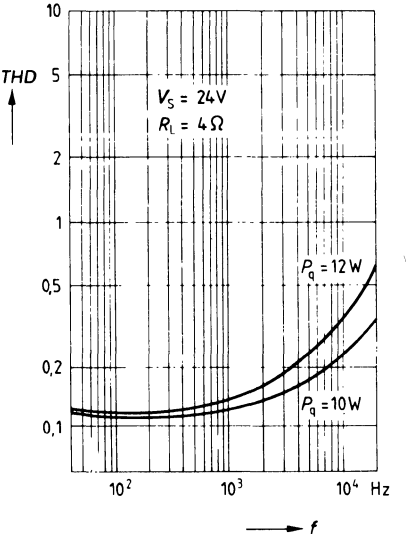
Stereo operation

Power dissipation (each channel) versus supply voltage



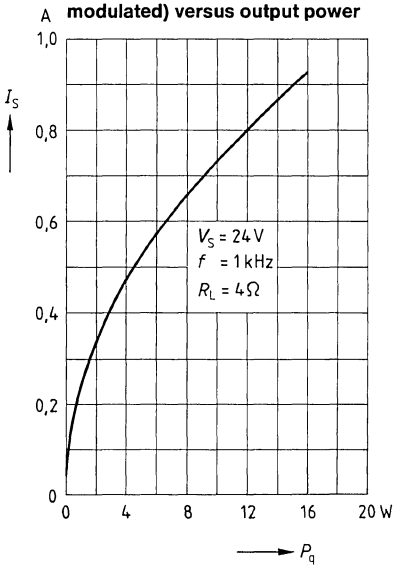
Stereo operation

Total harmonic distortion versus frequency



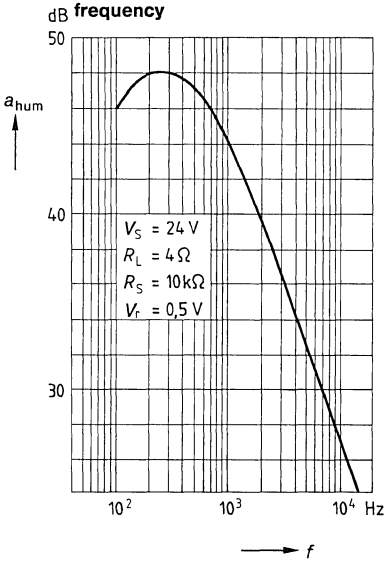
Stereo operation

Supply current (one channel) modulated) versus output power

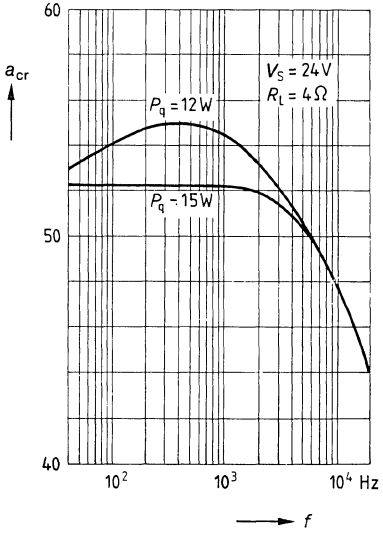


Stereo operation

Line hum suppression versus frequency



Cross-talk rejection versus frequency



The high gain, controlled video IF amplifier with controlled demodulator includes low-impedance outputs for the positive and negative video signal, gated control as well as delayed tuner control and an AFC output.

TDA 5400-2: for PNP tuners

Features

- High degree of integration
- Extensive control range
- High input sensitivity

Maximum ratings

Supply voltage	V_S	16.5	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	70	K/W

Operational range

Supply voltage	V_S	10 to 15.8	V
IF frequency	f_{IF}	15 to 75	MHz
Ambient temperature	T_A	0 to 70	°C

Characteristics

$V_S = 13$ V; $T_A = 25$ °C

Current consumption	I_{13}	60	mA
Stabilized reference voltage	$V_{14/12}$	6.0	Vdc
Control current for tuner $V_{16} = 0.5\ V_{13}$	I_{16}	4.0	mA
Tuner AGC threshold	$V_{15/12}$	0 to 4	Vdc
Gating pulse voltage			
pos. gating pulse	V_1	+3.0	V
neg. gating pulse	V_1	−3.0	V
Input voltage at G_{max} $V_3 = 3\ V_{pp}$	$V_{i17/18}$	max 100	µV
AGC range	ΔG	60	dB
IF control voltage			
V_{max}	$V_{2/12}$	min 0	Vdc
V_{min}	$V_{2/12}$	max 4.0	Vdc
AFC output current	I_{q6}	±1.0	mA
AFC switching			
$V_8 = V_9; R = 10$ kΩ OFF	$V_{8/12}$	max 4.0	Vdc
$V_8 = V_9; R = \infty$ ON	$V_{8/12}$	6.0	Vdc
AFC direction			
$di/df > 0$	$V_{5/12}$	4.0 to V_{13}	Vdc
$di/df < 0$	$V_{5/12}$	0 to 1.0	Vdc
Video output voltage (pos.) $R_L = \infty$	$V_{q3\,pp}$	3.0	V
Sync pulse level	$V_{3/12}$	2.0	Vdc
DC voltage $V_2 = 4$ V; $V_{17/18} = 0$	$V_{3/12}$	5.3	Vdc
Output current			
to ground through R	I_{q3}	−5.0	mA
to plus $V_3 = 7$ V	I_{q3}	+2.0	mA
Video output voltage (neg.) ($R_L = \infty$)	$V_{q4\,pp}$	3.0	V
Sync pulse level	$V_{4/12}$	$V_{13} - 2.0$	Vdc
DC voltage ($V_2 = 4$ V; $V_{17/18} = 0$)	$V_{4/12}$	$V_{13} - 5.3$	Vdc
Output current			
to ground through R	I_{q4}	−5.0	mA
to plus $V_4 = V_{13}$	I_{q4}	+1.0	mA

Additional application data[1])

Input impedance	$Z_{i17/18}$	1.8/2	kΩ/pF
Output impedance	$Z_{q10/11}$	6.6/2	kΩ/pF
AFC input impedance	$Z_{i8/9}$	20	kΩ
Output resistance	R_{q3}	150	Ω
Output resistance	R_{q4}	150	Ω
Residual IF (basic frequency)	$V_3; V_4$	10	mV
Video bandwidth (−3 dB)	B_{video}	6.0	MHz
Intermodulation ratio with reference to f_{CC} (sound-color-beat frequency)	a	45	dB

1) not measured

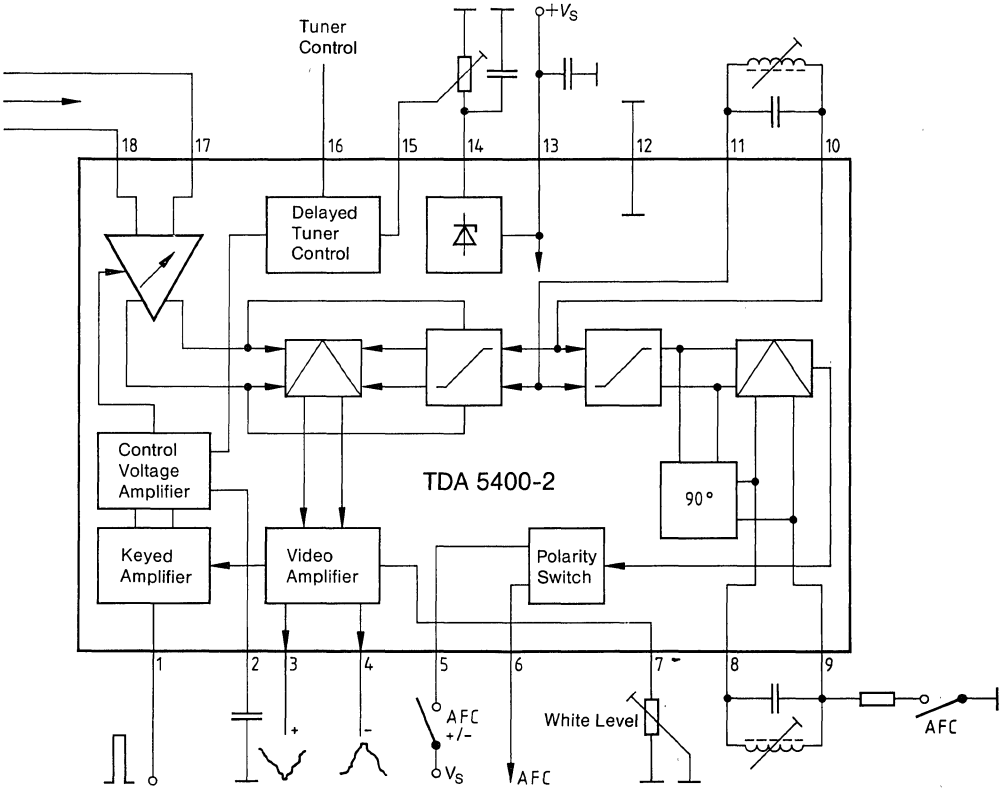
Circuit description

The integrated circuit is comprised of a 4-stage controlled AM amplifier, a limiter and mixer for synchronous demodulation of the video signals as well as an FM demodulator to generate positive or negative AFC voltages. In addition, an amplifier for both the positive and negative video output signal is included. The positive video signal together with the positive flyback pulse are used for gated control.

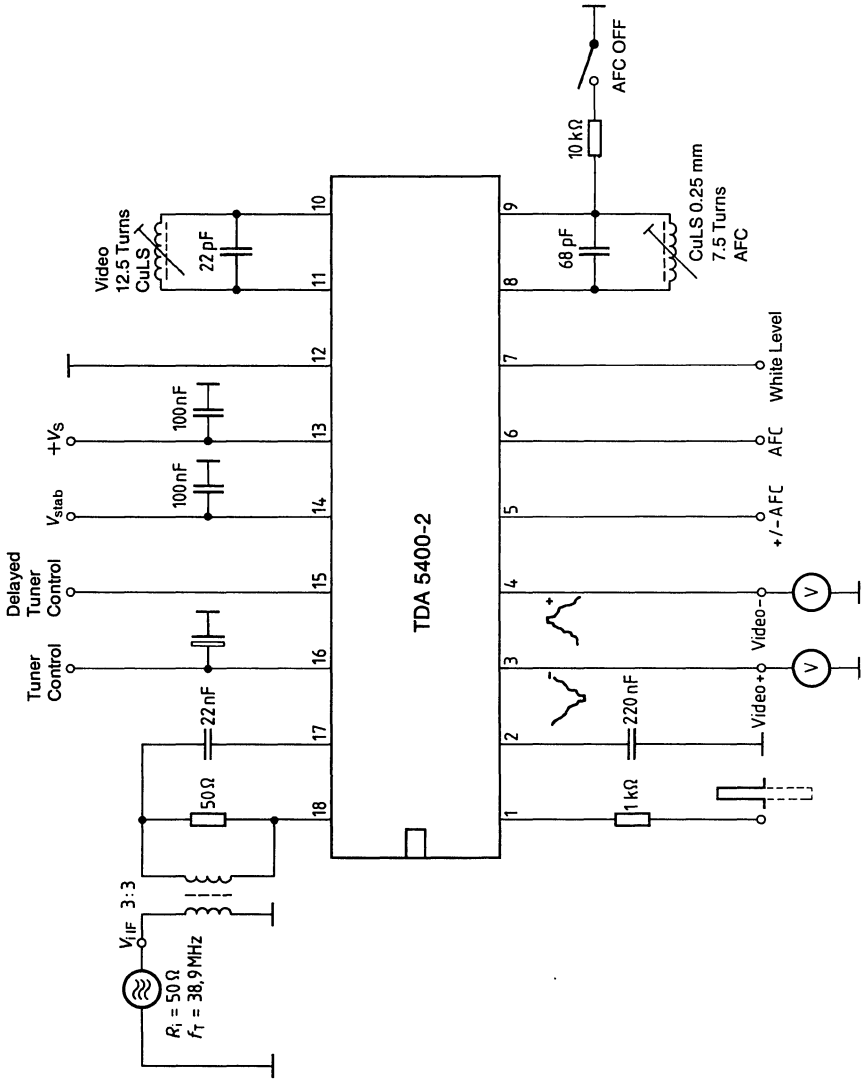
Pin description

Pin	Function
1	Gating pulse
2	Time constant AGC
3	Positive video output
4	Negative video output
5	AFC polarity switch
6	AFC output
7	White level adjustment
8	AFC circuit
9	AFC circuit
10	Tank circuit
11	Tank circuit
12	GND
13	Supply voltage
14	Reference voltage
15	Tuner AGC
16	Delayed AGC output
17	Video IF input
18	Video IF input

Block diagram



Measurement circuit



Modulator for TV, Video and Sound Signals — TDA 5660 P

DIP 18

The monolithically integrated circuit TDA 5660 P is especially suitable as modulator for the 48 to 860 MHz frequency range and is applied e.g. in video recorders, cable converters, TV converter installations, demodulators, video generators, video security systems, amateur TV applications, as well as personal computers.

- Synchronizing level-clamping circuit
- Peak white value gain control
- Continuous adjustment of modulation index for positive and negative modulation
- Dynamic residual carrier setting
- FM sound modulator
- AM sound modulator
- Picture carrier to sound carrier adjustment
- Symmetrical mixer output
- Symmetrical oscillator with own RF ground
- Low radiation
- Superior frequency stability of main oscillator
- Superior frequency stability of sound oscillator
- Internal reference voltage

Circuit description

Via pin 1, the sound signal is capacitively coupled to the AF input for the FM modulation of the oscillator. An external circuitry sets the preemphasis. This signal is forwarded to a mixer which is influenced by the AM modulation input of pin 16. The picture to sound carrier ratio can be changed by connecting an external voltage to pin 16, which deviates from the internal reference voltage. In case, the sound carrier should not be FM but AM modulated, pin 1 should be connected to pin 2, while the AF signal is capacitively coupled to pin 16. Through an additional external dc voltage at pin 16, the set AM modulation index can be changed by overriding the internally adjusted control voltage for a fixed AM modulation index. At the output of the above described mixer the FM and/or AM modulated sound signal is added to the video signal and mixed with the oscillator signal in the RF mixer. A parallel resonant circuit is connected to the sound carrier oscillator at pin 17, 18. The unloaded Q of the resonant circuit must be $Q = 25$ and the parallel resistor $R_T = 6.8$ kΩ to ensure a picture to sound carrier ratio of 12.5 dB. At the same time, the capacitative and/or inductive reactance for the resonance frequency should have a value of $X_C \approx X_L \approx 800\ \Omega$.

The video signal with the negative synchronous level is capacitively connected to pin 10. The internal clamping circuit is referenced to the synchronizing level. Should the video signal change by 6 dB, this change will be compensated by the resonant circuit which is set to the peak white value. At pin 11, the current pulses of the peak white detector are filtered through the capacitor which also determines the control time constant. When pin 12 is connected to ground, the RF carrier switches from negative to positive video modulation.

With the variable resistor of $R = \infty \ldots . 0\ \Omega$ at pin 12, the modulation depth, beginning with $R = \infty$ and a negative modulation of $m_{D/N} = 80\%$, can be increased to $m_{D/N} = 100\%$ and continued with a positive modulation of $m_{D/P} = 100\%$ down to $m_{D/P} = 88\%$ with $R = 0\ \Omega$. The internal reference voltage has to be capacitively blocked at pin 2.

The amplifier of the RF oscillator is available at pins 3-7. The oscillator operates as a symmetrical ECO circuit. The capacitive reactance for the resonance frequency should be $X_C \approx 70\ \Omega$ between pins 3, 4 and 6, 7 and $X_C \approx 26\ \Omega$ between pins 4, 6. In order to set the required residual carrier suppression, pin 9 is used to compensate for any dynamic asymmetry of the RF mixer during high frequencies of > 300 MHz. The oscillator chip ground, pin 5, should be connected to ground at the oscillator resonant circuit shielding. Via pin 3 and 7 an external oscillator signal can be injected inductively or capacitively. The peripheral layout of the pc board should be provided with a minimum shielding attenuation of approx. 80 dB between the oscillator pins 3-7 and the modulator outputs 13-15.

For optimum residual carrier suppression, the symmetric mixer outputs at pins 13, 15 should be connected to a matched balanced-to-unbalanced broadband transformer with excellent phase precision at 0 and 180 degrees, e.g. a Guanella transformer. The transmission loss should be less than 3 dB. In addition, an LC low pass filter combination is required at the output. The cut-off frequency of the low pass filter combination must exceed the maximum operating frequency.

If the application circuit according to figure 1, 2 is used, a multiplication factor V/RF (application) = V/RF (data sheet) 3.9 must be used to convert a 300 Ω symmetrical impedance to an asymmetrical impedance of 75 Ω for the stated RF output voltage V_q of the type specification in order to ensure a transmission attenuation of 0 dB for the balanced-to-unbalanced mixer.

Maximum ratings

		min	max		Remarks
Supply voltage	V_S	−0.3	14.5	V	
Current from pin 2	$-I_2$	0	2	mA	$V_2 = 7$ to 8 V $V_S = 9.5$ to 13.5 V
Voltage at pin 1	V_1	$V_2 - 2$	$V_2 + 2$	V	$V_S = 9.5$ to 13.5 V
Voltage at pin 9	V_9	−4	1	V	
Voltage at pin 10	$V_{10\,pp}$		1.5	V	only via C (max. 1 µF)
Capacitance at pin 2	C_2	0	100	nF	
Capacitance at pin 11	C_{11}	0	15	µF	
Voltage at pin 12	V_{12}	−0.3	1.4	V	
Voltage at pin 13	V_{13}	V_2	V_S	V	
Voltage at pin 15	V_{15}	V_2	V_S	V	
Voltage at pin 16	V_{16}	$V_2 - 1.5$	$V_2 + 1.5$	V	$V_S = 9.5$ to 13.5 V
Only the external circuitry shown in application circuits 1 and 2 may be connected to pins 3, 4, 6, 7, 17 and 18					
Junction temperature	T_j		150	°C	
Storage temperature	T_{stg}	−40	125	°C	
Thermal resistance (system-air)	$R_{th\,SA}$		80	K/W	

Operating range

Supply voltage	V_S	9.5	13.5	V	
Video input frequency	f_{VIDEO}	0	5	MHz	
Sound input frequency	f_{AF}	0	20	kHz	
Output frequency	f_q	48	860	MHz	depending on the oscillator circuitry at pins 3-7
Ambient temperature	T_A	0	70	°C	
Sound oscillator	f_{OSC}	4	7	MHz	
Voltage at pin 13, 15	$V_{13,15}$	V_2	V_S	V	

Characteristics

V_S = 11 V; T_A = 25 °C

		Test conditions	Figure	min	typ	max	
Current consumption	I_8	I_2 = 0 mA	1; 2	22	30	40	mA
Reference voltage	V_2	$0 \leq I_2 \leq 1$ mA	1; 2	7	7.5	8	V
Oscillator frequency range	f_{OSC}	External circuitry adjusted to frequency		48		860	MHz
Turn-on start-up drift	Δf_{OSC}	TC value of capacitor in osc. circuit is 0; drift is referenced only to self-heating of the component t = 0.5-10 s; T_A = const.					
		Ch 30	1; 2	0	−50	−500	kHz
		Ch 40	1; 2	0	−200	−500	kHz
Frequency drift as function of V_S	$-\Delta f_{OSC}$	V_S = 9.5-13.5 V; T_A = const.	1; 2	0			
		Ch 40		−150		150	kHz
Video input current at pin 10	$-I_{10}$	$C_{10} \leq 1$ µF	5	0		10	µA
Video input voltage at pin 10	$V_{10\,pp}$	at coupling capac. $C \leq 1$ µF $I_{leak} \leq \pm 0.3$ µA	21; 22	0.7		1.4	V
Modulation depth	$m_{D/N}$	neg. mod.	1; 16	75	80	85	%
$V_{VIDEO\,pp}$ = 1 V; f_{VIDEO} = 200 kHz sine signal	$m_{D/P}$	pos. mod.	2; 16	83	88	93	%
Output impedance	Z_{13}; Z_{15}	static	24	10			kΩ
RF output voltage Modulation signal in neg. modulation pin 12 open	$V_{q\,rms}$	Ch 40	1b	2.5	3.5	5.5	mV
Output capacitance	C_{13}=C_{15}		25	0.5	1	2.0	pF
S parameter at pins 3, 4 and 6, 7			26				
RF output phase	$\alpha_{13,15}$			140	180	220	degrees
RF output voltage change; adjustment range	ΔV_q	f = 543.25-623.25 Δf = 80 MHz Ch 30-Ch 40	1	0		1.5	dB
RF output voltage change	ΔV_q	f = 100-300 MHz	6	0		1.5	dB
RF output voltage change	ΔV_q	f = 48-100 MHz	6	0		1.5	dB
Oscillator interference FM caused by AM modulation and coupling of the modulator output with the oscillator resonant circuit; $V_{VIDEO\,pp}$ = 1 V; f_{VIDEO} = 10 kHz; sine signal							
	Ch 30		1; 9	0	5	15	kHz
	Ch 40		1; 9	0	7	21	kHz

Characteristics

$V_S = 11$ V; $T_A = 25$ °C

		Test conditions	Figure	min	typ	max	
Intermodulation ratio	a_{MR}	$f_P + 1.07$ MHz	1; 7; 15	54	75		dB
Harmonic wave ratio	a_H	$f_P + 8.8$ MHz without video signal 19, 20, 21 unmodulated video and sound carrier, measured with the spectrum analyzer as difference between video carrier signal level and sideband signal level without video and sound modulation.	1; 7; 15	35			dB
Harmonic wave ratio	a_H	$f_P + 2f_S$	1; 7	35	48		dB
Harmonic wave ratio	a_H	$f_P + 3f_S$ V_q with spectrum analyzer; loaded Q factor Q_L of the sound oscillator resonant circuit adjusted by R_S to provide the required picture to sound carrier ratio of 12.5 dB; $R_S = 6.8$ kΩ; $Q_U = 25$ of the sound oscillator circuit.	1; 7	42	48		dB
Sound carrier ratio	$a_{P/S}$		1; 7; 17	10	12.5	15	dB
Color picture to sound carrier ratio	a_P	$f_P + 4.4$ MHz (dependent on video signal)	1		17		dB
All remaining harmonic waves	a	Multiple of fundamental wave of picture carrier, without video signal, measured with spectrum analyzer; $f_{P/S} = 523.25$-623.25 MHz	1	15			dB
Amplitude response of the video signal	a_V	$V_{VIDEO\,pp} = 1$ V with additional modulation $f = 15$ kHz-5 MHz sine signal between black and white	1; 13	0		1.5	dB
Residual carrier suppression	a_R	With adjustment at pin 9 Ch 30...Ch 40	1; 12	32			
Static mixer balance characteristic	$\Delta V_{13/15}$	V_9 adjusted to $\Delta V_{13/15}$ minimum	21; 23	−100	0	+100	mV
Dynamic mixer balance characteristics	$V_{13\,rms}$	V_9 adjusted to $V_{13\,rms}$ minimum	21; 23		0	10	mV
Stability of set modulation depth	Δm_D	Video input voltage changes with sine signals $f = 0.2$ MHz; $\Delta V_{VIDEO\,pp} = 1$ V ± 3 dB; Ch 30...Ch 40; $V_S = 12$ V; $T_A =$ const.			1	±2.5	%
Stability of set modulation depth	Δm_D	$f = 48...100$ MHz	6		1	±2.5	%
Stability of set modulation depth	Δm_D	$f = 100...300$ MHz	6		2	±4	%
Stability of set modulation depth	Δm_D	$T_A = 0$-60 °C; $V_S = 12$ V	1		1	±2.5	%

Characteristics

$V_S = 11$ V; $T_A = 25$ °C

		Test conditions	Figure	min	typ	max	
Stability of set modulation depth	Δm_D	$V_S = 9.5\text{-}13$; 5 V; T_A = const.	1		1	±2.5	%
Interference product ratio sound in video; sound carrier FM mod.	$a_{S/P}$	Ch 30...Ch 40	1;11	48	60		dB
Signal-to-noise ratio in video; sound carrier unmodulated	$a_{N/P}$	Ch 30...Ch 40	1;11	48	74		dB
Interference product ratio sound in video sound carrier AM mod.	$a_{S/P}$	Ch 30...Ch 40	1;11	20	33		dB
Umweighted FM noise level ratio video in sound; FuBK test picture as video signal	$a_{P/S}$	Ch 39	1a; 8	48	54		dB
Unweighted FM noise level ratio video in sound	$a_{P/S}$	Ch 39; test picture VU G-Y; U/V	2; 8	48	56		dB
		Ch 39; color bar	2; 8	46	52		dB
		Ch 39; uniform red level	2; 8	48	58		dB
		Ch 39; uniform white level	2; 8	45	51		dB
		Ch 39; test pattern	2; 8	48	55		dB
		Ch 39; white bar	2; 8	46	52		dB
		Ch 39; bar	2; 8	45	50.8		dB
		Ch 39; 20T/2T	2; 8	43	49		dB
		Ch 39; 30% white level	2; 8	48	58		dB
		Ch 39; 250 kHz	2; 8	46	52		dB
		Ch 39; multiburst	2; 8	46	53		dB
		Ch 39; ramp	2; 8	44	50		dB
Signal-to-noise ratio of sound oscillator	$a_{S/N}$		1a; 8	48	54		dB
Differential gain	G_{dif}	measured with measurement demodulator, video test signals and vector scope	1			10	%
Differential phase	φ_{dif}		1			15	%
Period required for peak white detector to reach steady state for full modulation depth with 1 white pulse per half frame with control in steady state	t	C at pin 11 = 10 µF; $I_{leak} \leq 2$ µA	1		6	50	µs

Characteristics

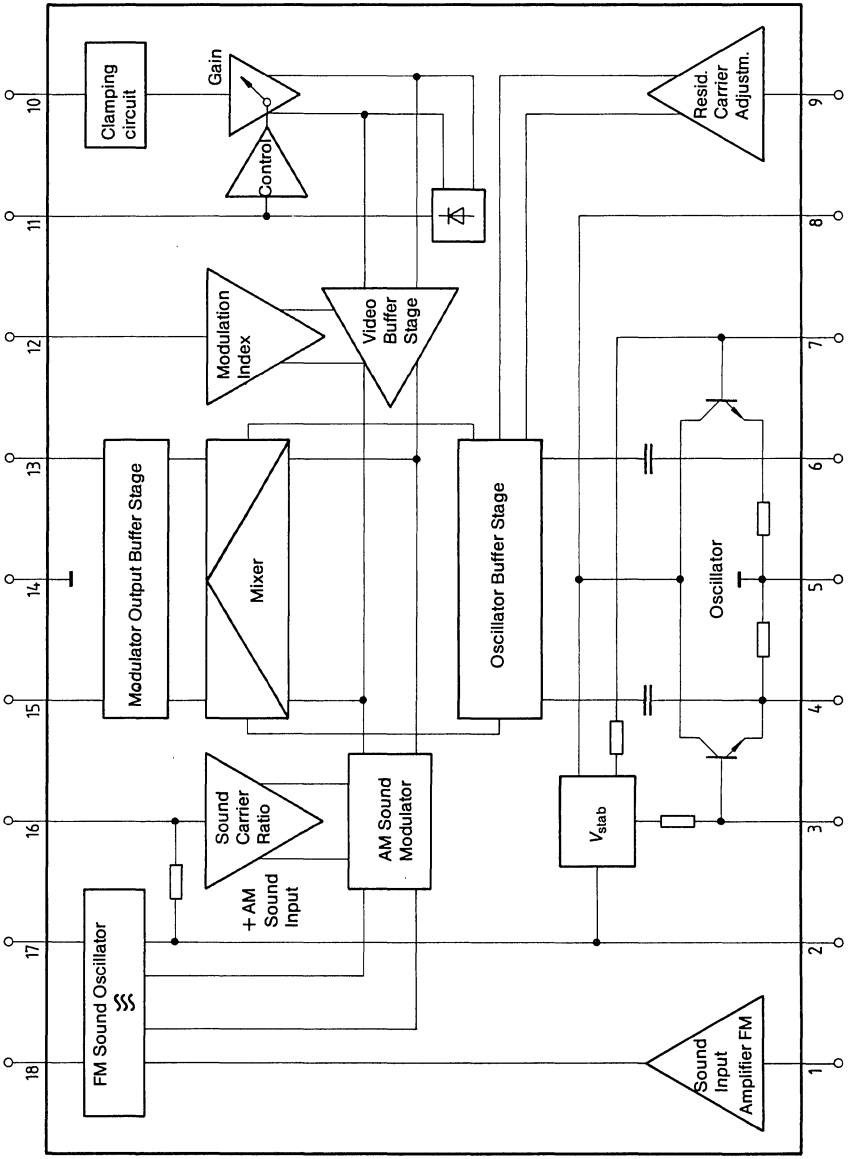
$V_S = 11$ V; $T_A = 25$ °C

		Test conditions	Figure	min	typ	max	
Setting time for video signal change from 0 V_{pp} to 1.4 V_{pp}	t	Video blanking signal content is uniform white level	1		120	500	µs
Setting time for video blanking signal from 100% white level to 42% grey level with subsequent rise in grey level to 71% of video blanking signal (due to decontrol process)	t		1		2.25	5	s
Sound oscillator frequency range	$f_{S/OSC}$	Unloaded Q factor of resonant circuit $Q_U = 25$; resonance frequency 5.66 MHz	1	4		7	MHz
Turn-on start-up drift	$\Delta f_{S/OSC}$	Capacitor TC value in sound oscillator circuit is 0, drift is based only on component heating T_A = const.; $f_{S/OSC} = 5.5$ MHz	1		5	15	kHz
Sound oscillator frequency operating voltage	$\Delta f_{S/OSC}$	$V_S = 9.5$-13.5 V; $f_{S/OSC} = 5.5$ MHz; T_A = const.; $Q_U = 25$	1		5	15	kHz
FM mod. harmonic distortion	THD_{FM}	$V_{1\,rms} = 150$ mV	19; 19a		0.6	1.5	%
Audio preamplifier input impedance (dyn.); FM operation	Z_1		1	200			kΩ
FM sound modulator, static modulation characteristic	$\Delta f_{S/OSC}$	$\Delta V_{1/2} = V_1$-$V_2 = \pm 1$ V; $f_{S/OSC} = 5.5$ MHz; $Q_U = 25$	1; 14	±210	±270	±330	kHz
FM sound modulation characteristic (dynamic)	$\Delta f_M/\Delta V_1$		1a; 10a	0.3	0.38	0.46	kHz/mV
AM sound modulation factor	m	$V_{AF} = 0.3$ V	2; 3; 4a, b	30	40	50	%
AM sound modulation harmonic distortion	THD_{AM}	$m = 86\%$; $V_{AF} = 0.64$ V; $f_{AF} = 1$ kHz			0.7	3	%
AM audio preamplifier input impedance	Z_{16}		2	25	50	75	kΩ
AM sound modulator input voltage	V_{AF}	$m = 90\%$; $f_{AF} = 1$ kHz	2	0.5	0.67	0.84	V

Pin description

Pin	Function
1	AF input for FM modulation
2	Internal reference voltage
3	Symmetrical oscillator input
4	Symmetrical oscillator output
5	Oscillator ground
6	Symmetrical oscillator output
7	Symmetrical oscillator input
8	Supply voltage
9	Dynamic residual carrier adjustment
10	Video input with clamping
11	Connection for smoothing capacitor for video control loop
12	Switch for positive and negative modulation as well as residual carrier control
13	Symmetrical RF output
14	Remaining ground of component
15	Symmetrical RF output
16	Picture to sound carrier ratio (adjustment and AM sound input)
17	Sound oscillator symmetrical input for tank circuit
18	Sound oscillator symmetrical input for tank circuit

Block diagram



Test and measurement circuit 1 for FM sound carrier and negative video modulation

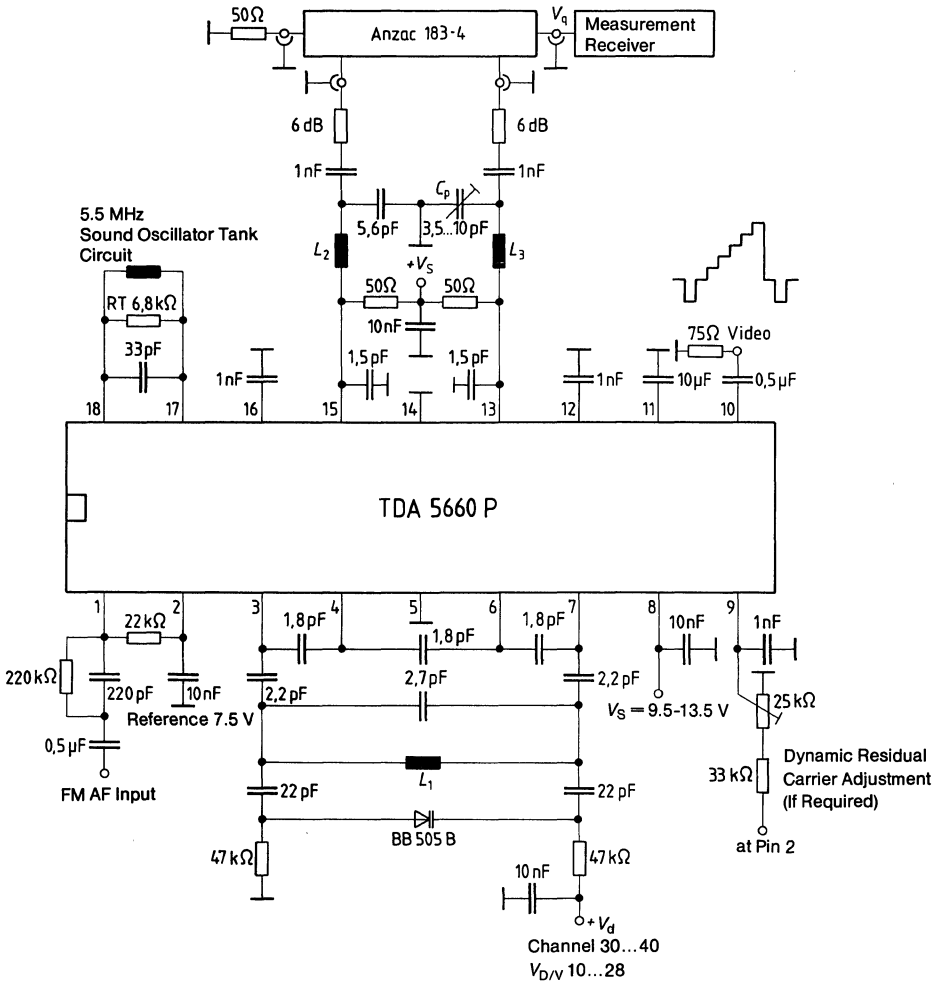


Figure 1

Test and measurement circuit 1 for FM sound carrier and negative video modulation

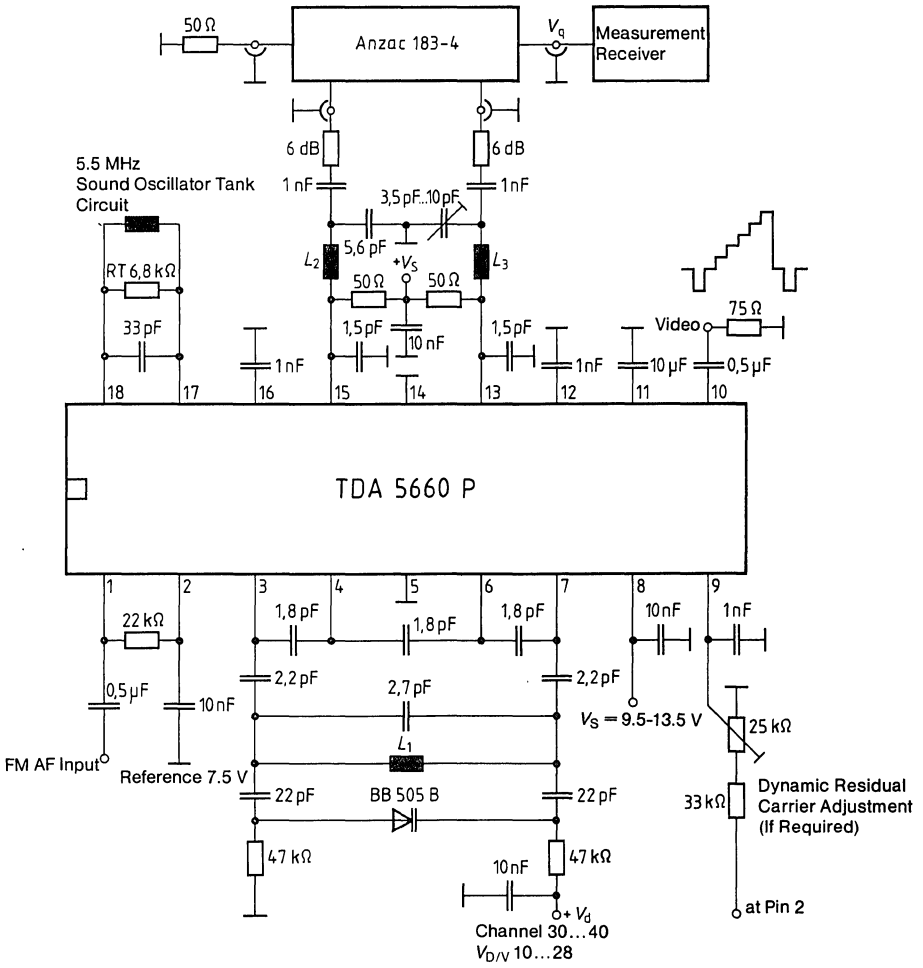


Figure 1a

Test and measurement circuit 1 for FM sound carrier and negative video modulation

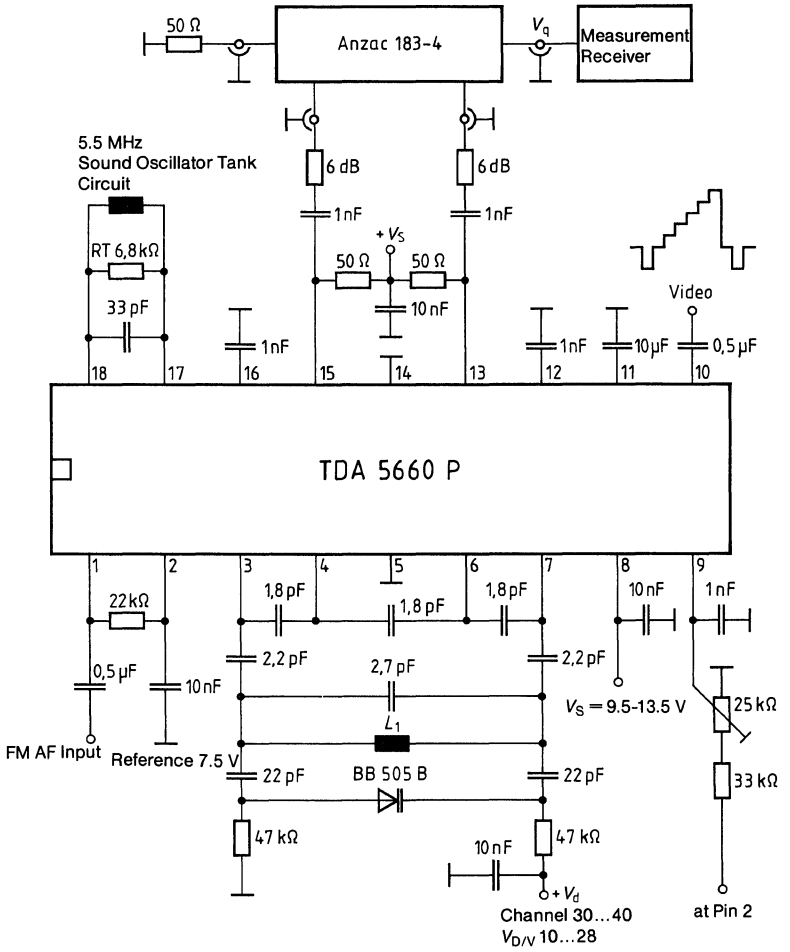


Figure 1b

Test and measurement circuit 2 for FM sound carrier and negative video modulation

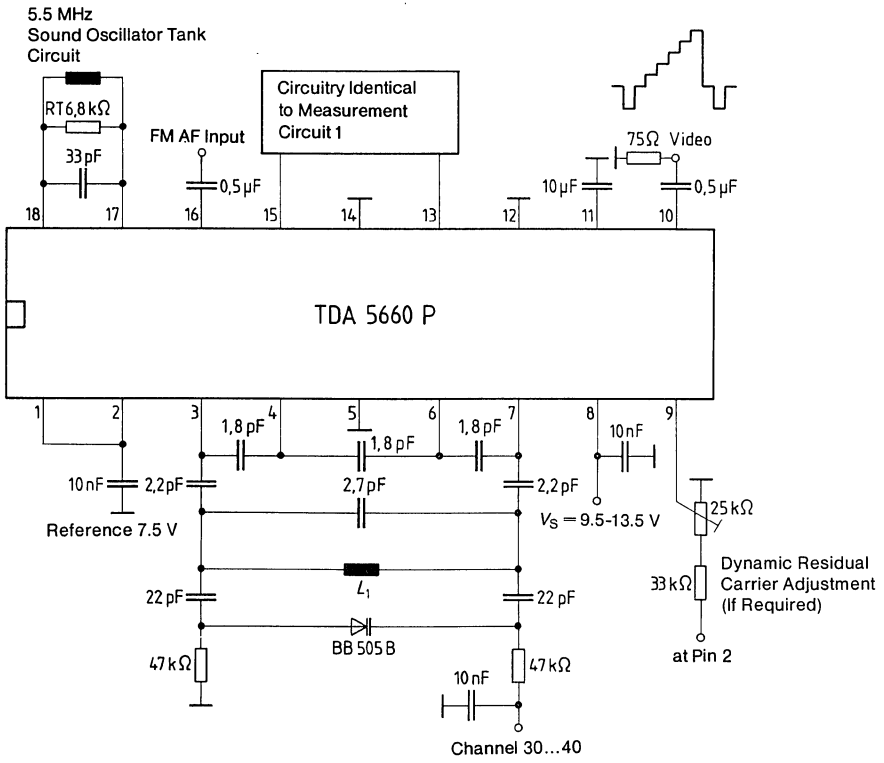


Figure 2

AM sound modulation measurement

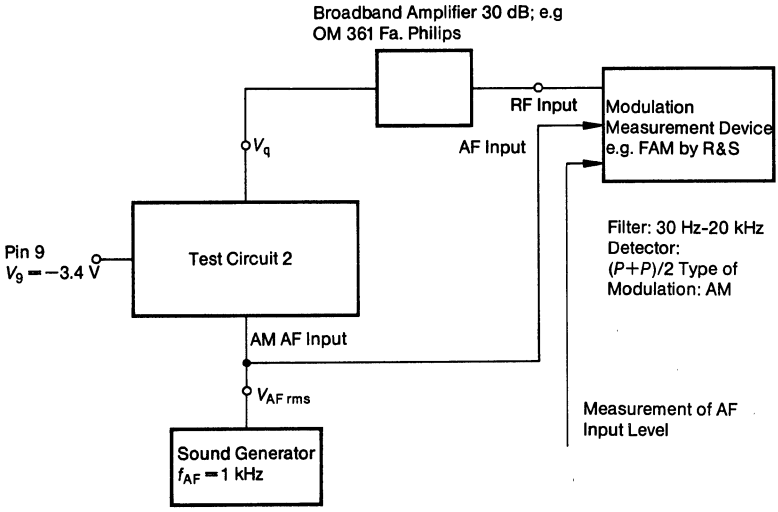


Figure 3

AM sound carrier modulation index versus AF input voltage at pin 16

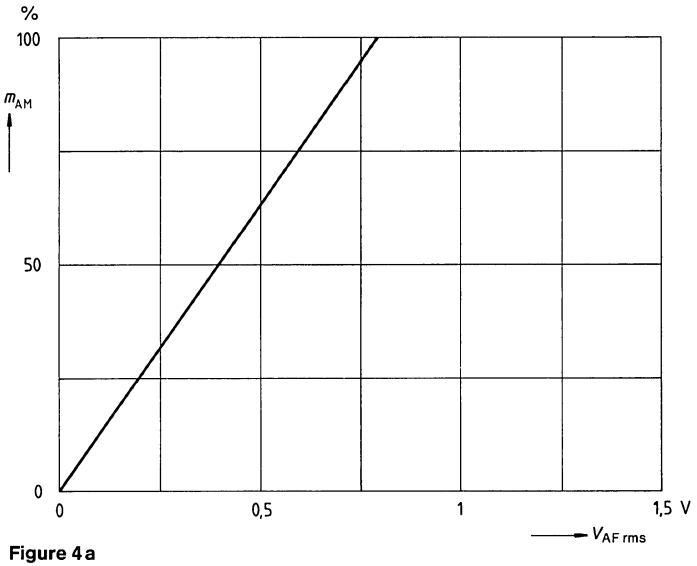


Figure 4a

AM sound carrier modulation index versus dc voltage offset at pin 16

$V_{AF\ rms} \doteq 0.6$ V; $\Delta V_{16/2}$ (V) $= V_2 - V_{16}$

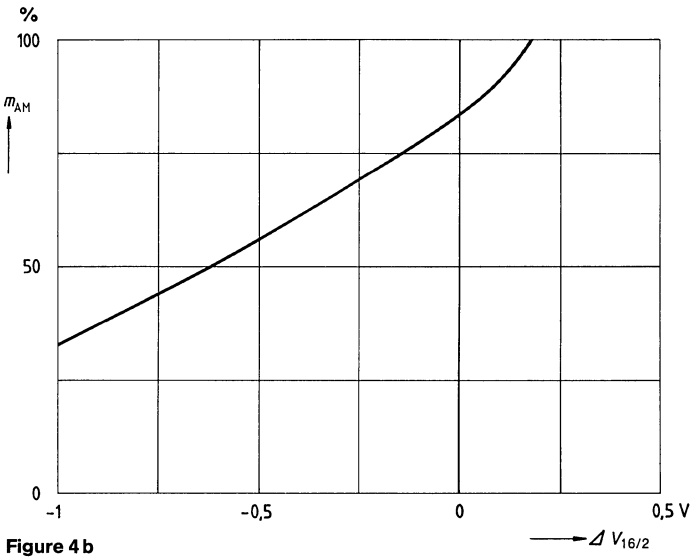


Figure 4b

Measurement circuits

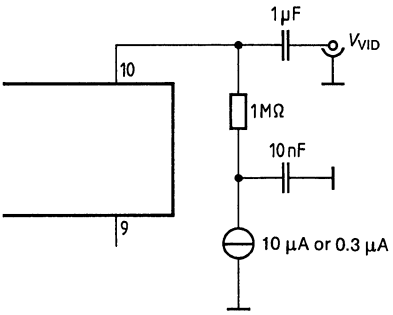
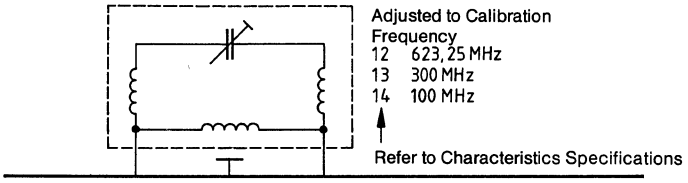


Figure 5



TDA 5660 P Remaining External Circuitry as Fig. 1

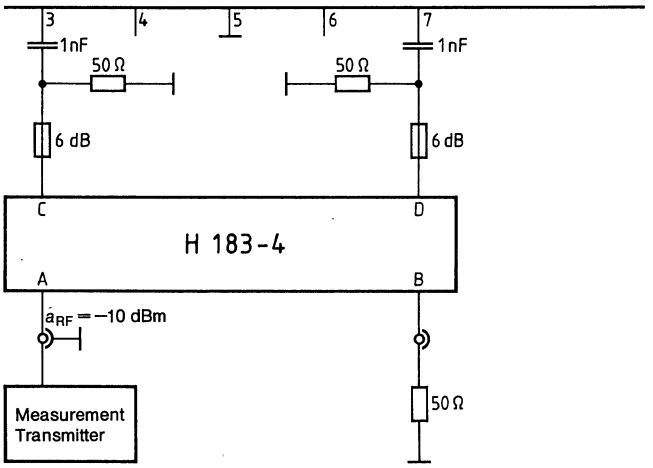


Figure 6

Frequency spectrum above the video carrier, measured at clamp V_q with a spectrum analyzer

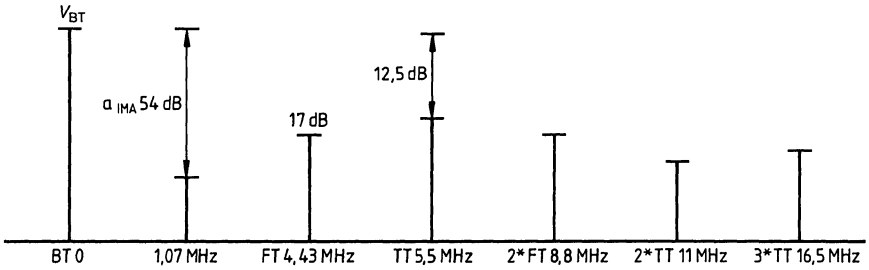


Figure 7

BT = Video Carrier
FT = Frequency Carrier
TT = Sound Carrier

Description of the measurement configuration to measure the noise voltage, video in sound

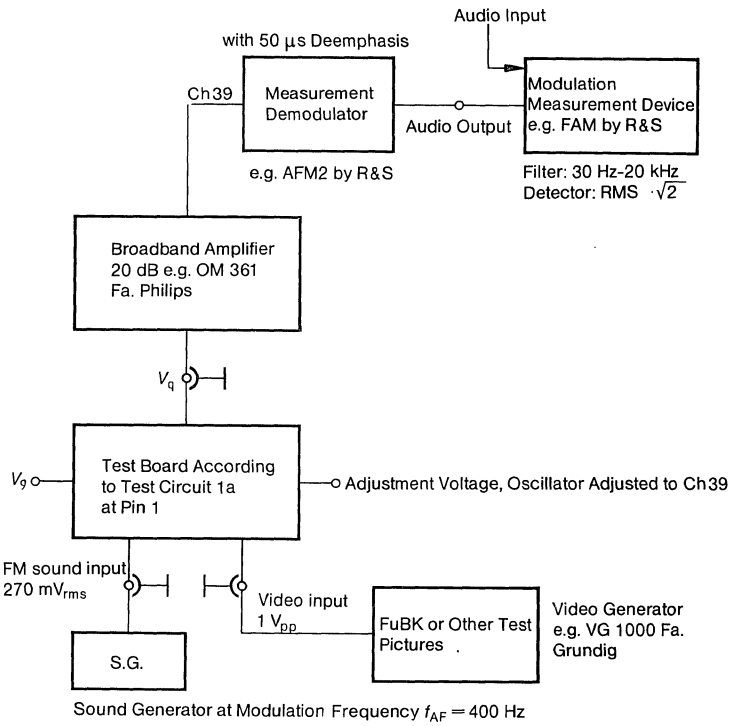


Figure 8

Calibration: A signal of $V_{AF\ rms} = 270$ mV and $f = 0.4$ kHz, corresponding to a nominal deviation of 30 kHz, is connected to the sound input, and the demodulated AF reference level at the audio measurement device is defined as 0 dB. No video signal is pending.

Measurement: 1) The AF signal is switched off and the FuBK video signal is connected to the video input with $V_{VIDEO\ pp} = 1$ V. The audio level in relation to the reference calibration level is measured as ratio $a_{p/s} = 20 \log (V_{FUBK}) / (V_{nominal})$.

2) AF and video signal are switched off. The noise ratio in relation to the AF reference calibration level is measured as signal-to-noise ratio $a_{S/N}$.

Description of the measurement configuration to measure the oscillator interference FM

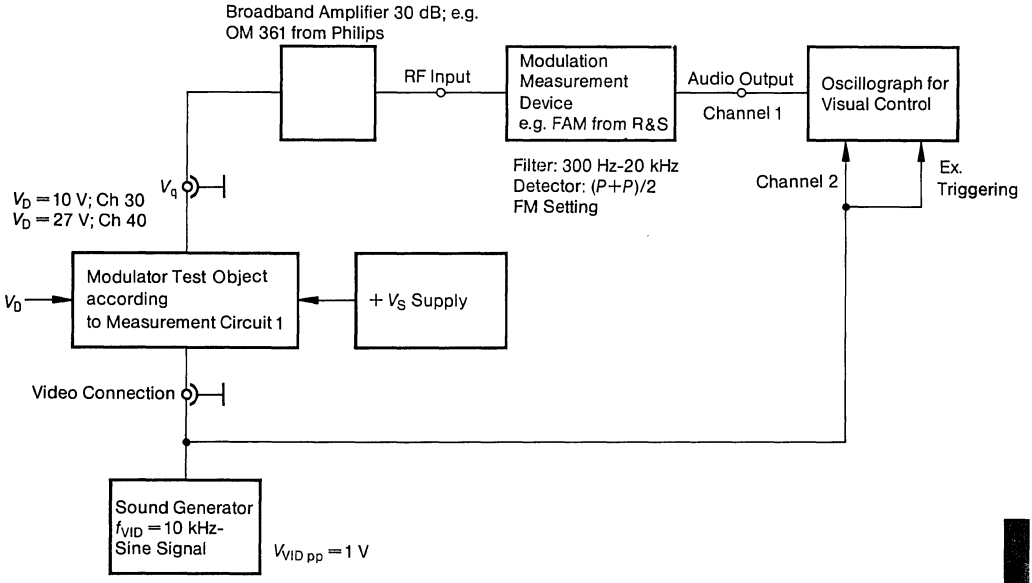


Figure 9

Description of the measurement configuration to measure the total harmonic distortion during FM operation of the sound carrier

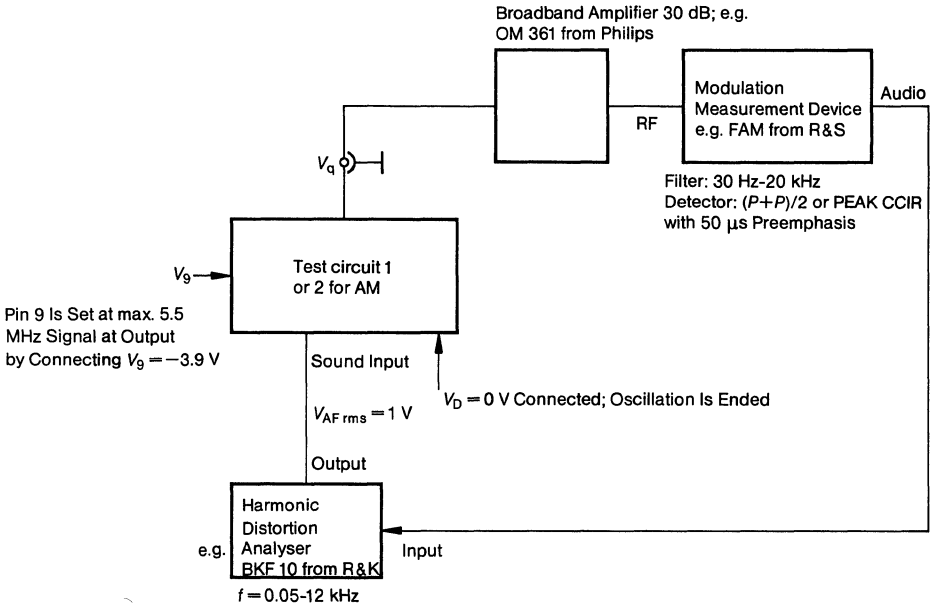


Figure 10

Description of the measurement configuration to measure the total harmonic distortion during FM operation of the sound carrier

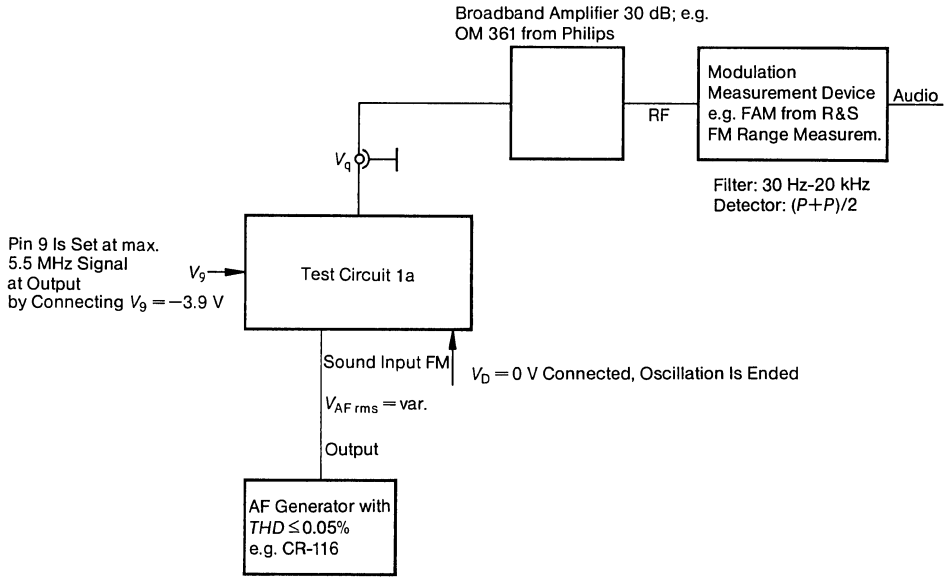


Figure 10 a

Description of the measurement configuration to measure the sound and/or noise in video during FM and/or AM sound carrier modulation

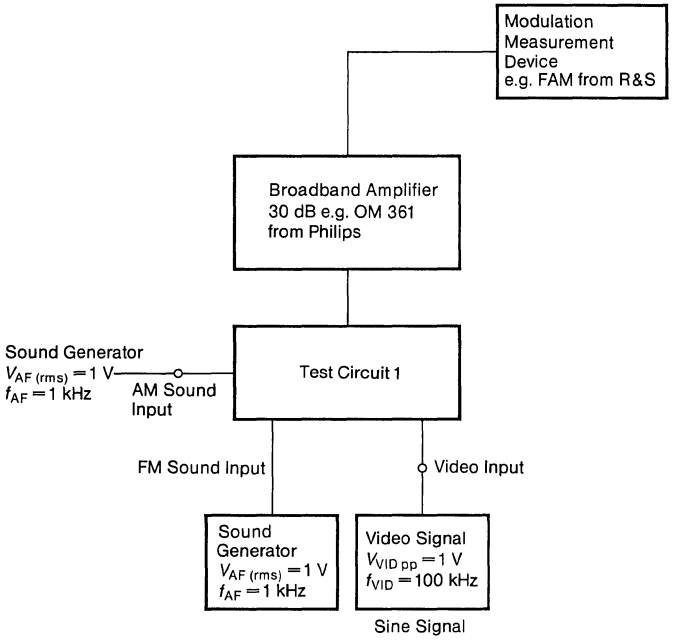


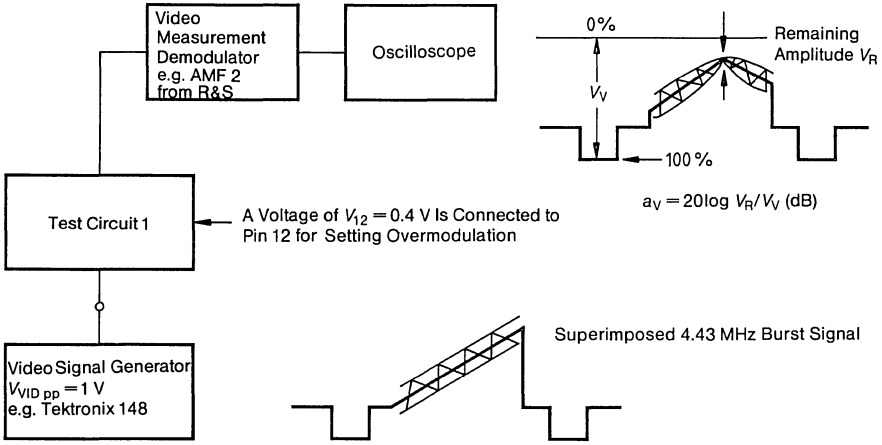
Figure 11

Calibration: AF signals are switched off; video signal is pending at the video input; device to measure modulation set at AM is adjusted to video carrier; filter: 300 Hz...200 kHz; detector $(P+P)/2$; resulting modulation index is defined as $m_V = 0$ dB.

Measurement:

1) Measurement of interference product ratio sound in video during FM modulation of the sound carrier: AF signal is connected to FM sound input; video signal is switched off; device to measure modulation is set to AM; filter: 300 Hz...3 kHz; detector: $(P+P)/2$; a ratio of $a_{S/P} = 20$ log $m_{V/S}$/mV) is derived from the resulting modulation index $m_{V/S}$.
2) Measurement of interference product ratio sound in video during AM modulation of sound carrier: AF signal is connected to AM sound input; otherwise identical with measurement 1.
3) Measurement of signal-to-noise ratio in video without AM/FM modulation of sound carrier: AF signals are switched off; video signal is switched off; control voltage at pin 11 is clamped to value present during connected video signal; modulation device is set to AM; filter: 300 Hz...3 kHz; detector: RMS $\sqrt{2}$; readout in dB to reference level of calibration is $a_{S/P}$.

Description of the measurement configuration to measure the residual carrier suppression



Adjust Cp in Circuit 1 and Dynamic Residual Carrier Suppression to Suppression Maximum.

Figure 12

Description of the measurement configuration to measure the video amplitude response

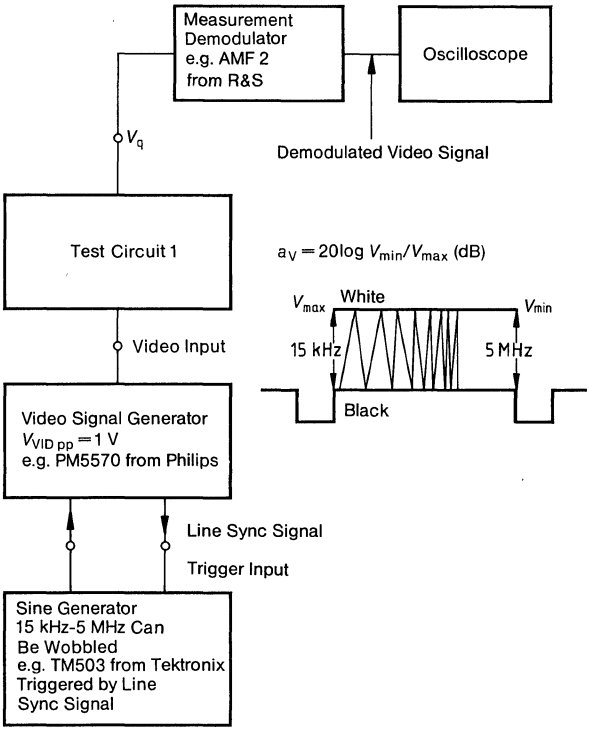
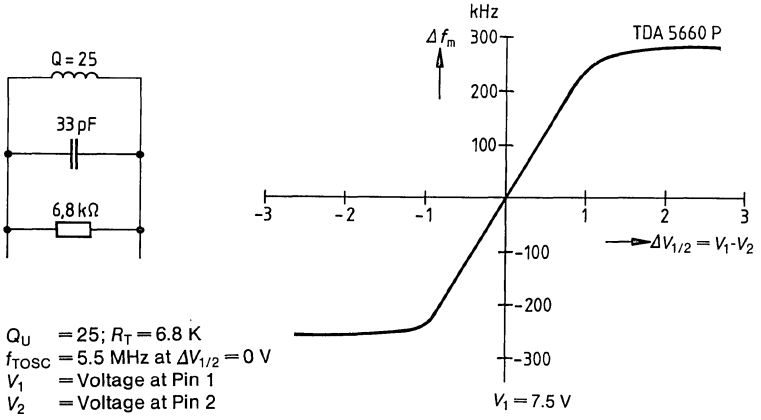


Figure 13

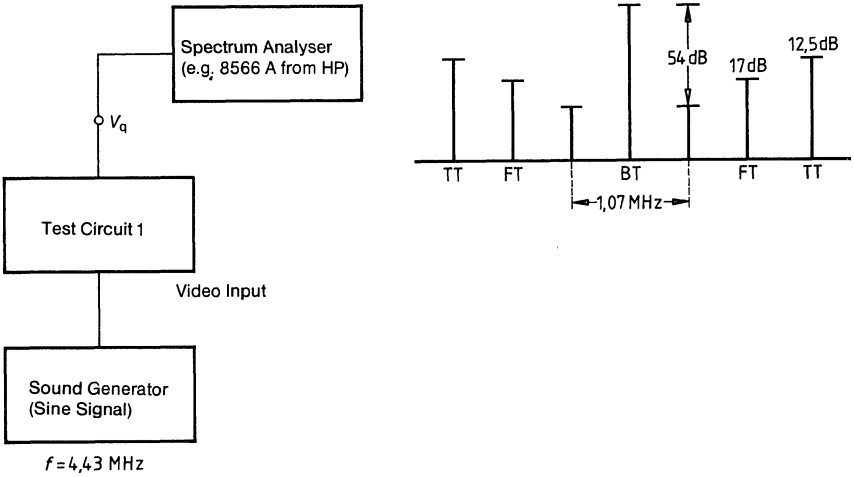
Static modulation characteristic of the FM sound modulator



Q_U = 25; R_T = 6.8 K
f_{TOSC} = 5.5 MHz at $\Delta V_{1/2}$ = 0 V
V_1 = Voltage at Pin 1
V_2 = Voltage at Pin 2

Figure 14

Description of the measurement configuration to measure the 1.07 MHz moires



$V_{VID\ pp}$ = 250 mV: Frequency carrier level lies below the activation point of the video amplitude control and has been set to provide a ratio of 17 dB with respect to the video carrier.

Figure 15

Modulation index during negative video modulation and/or the voltage at pin 12 versus current at pin 12

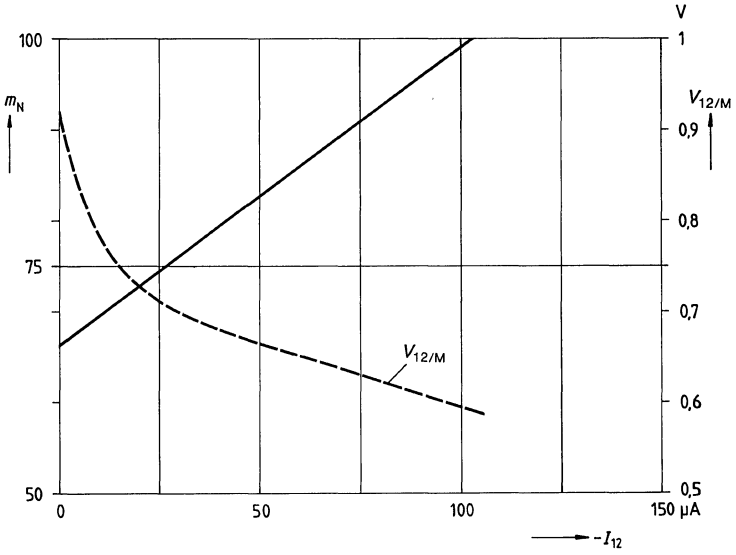


Figure 16a

Modulation depth is calculated as $m_D = (2 \times m)/(1 + m)$ from the modulation index. Prerequisite is a sine-shaped modulation.

m_N = modulation index for negative modulation
m_P = modulation index for positive modulation

If a resistor is connected to ground at pin 12 to adjust modulation depth, the resistor is calculated as $R_{12/M} = (V_{12/M})/I_{12}$.

Modulation index during positive video modulation and/or the voltage at pin 12 versus current at pin 12

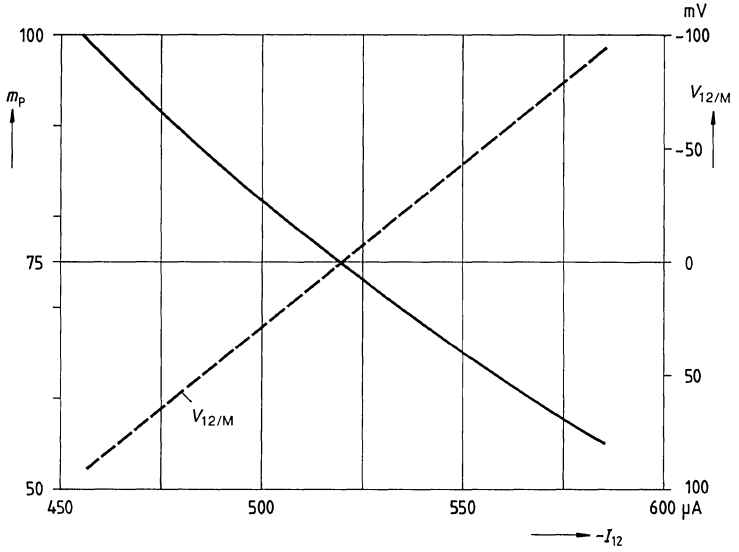


Figure 16

Modulation depth is calculated as $m_D = (2 \times m)/(1 + m)$ from the modulation index. Prerequisite is a sine-shaped modulation.

m_N = modulation index for negative modulation
m_P = modulation index for positive modulation

If a resistor is connected to ground at pin 12 to adjust modulation depth, the resistor is calculated as $R_{12/M} = (V_{12/M})/I_{12})$.

Picture to sound carrier ratio versus dc voltage offset at pin 16
unloaded Q factor of resonant circuit $Q_U = 25$, $R_T = 6.8$ k; $f = 5.5$ MHz.
The picture to sound carrier ratio of $a_{P/S} = 13$ dB was set via the loaded Q factor Q_L without external voltage at pin 16.

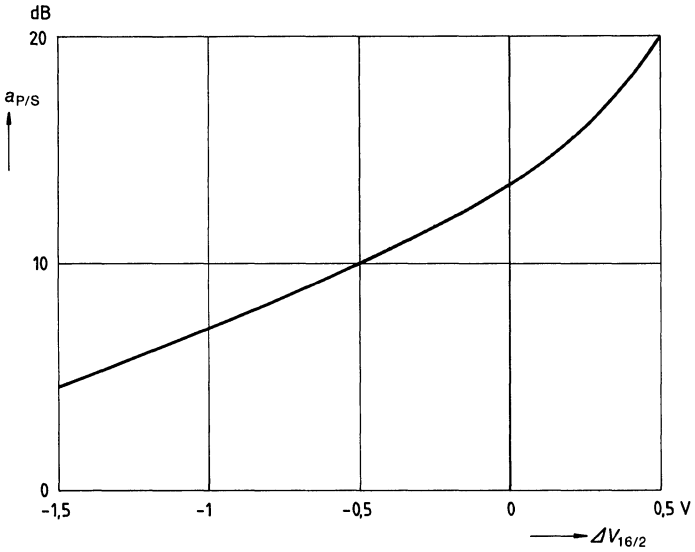


Figure 17

To adjust the picture to sound carrier ratio, a component was used with a resistance of typ. 11.5 kΩ at pins 17, 18.
The loaded Q factor of the resonant circuit was derived from the internal resistance $R_{17/18}$ connected in parallel with the external resistor R_s.

Measurement of the sound oscillator FM deviation without preemphasis and deemphasis; f_{AF} = 1 kHz; modulation deviation, sensitivity $(\Delta f_{AF})/(\Delta V_{AF})$ = 0.38 kHz/mV; V_{AF} = var; detector (P+P)/2; AF filter 30 Hz to 20 kHz, measurement in accordance with CCIR 468-2 DIN 45405; test circuit 1a.

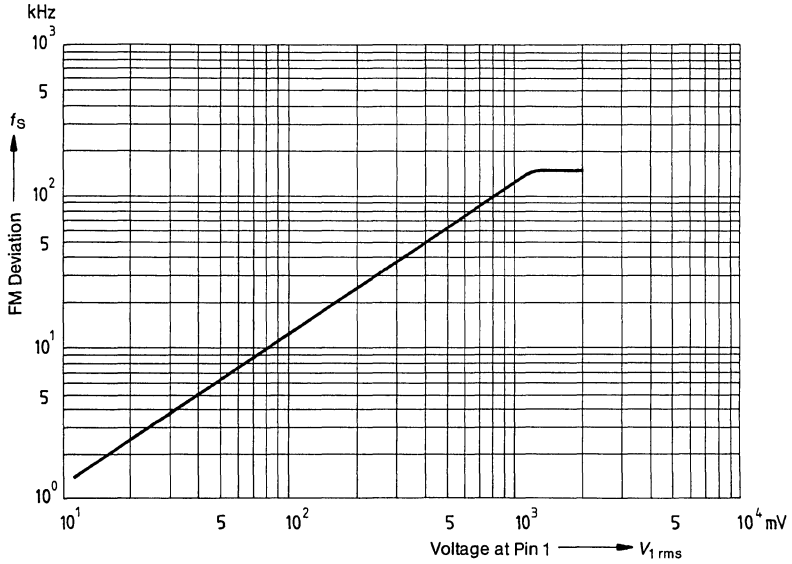


Figure 18

Measurement of the sound oscillator FM deviation without preemphasis and deemphasis; f_{AF} = 1 kHz; modulation deviation, sensitivity $(\Delta f_{AF})/(\Delta V_{AF})$ = 0.38 kHz/mV; V_{AF} = var; detector (P+P)/2; AF filter 30 Hz to 20 kHz, measurement in accordance with CCIR 468-2 DIN 45405; test circuit 1a

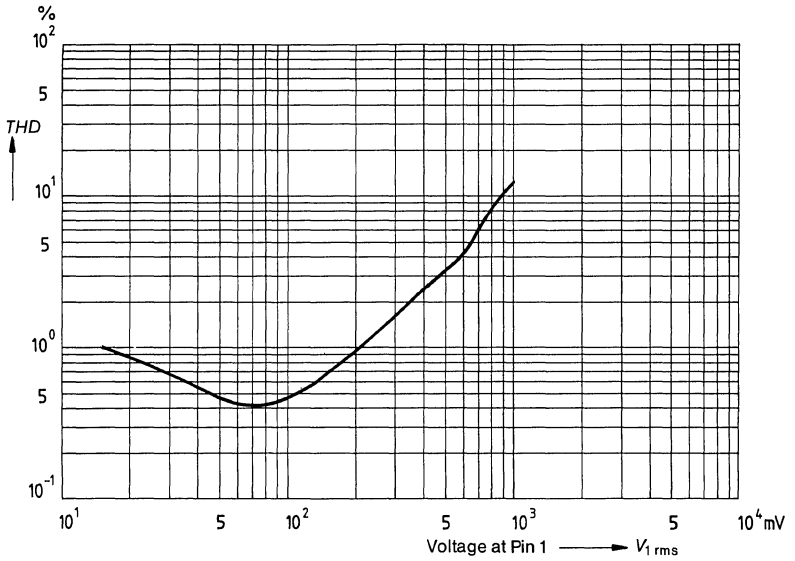


Figure 18a

Sound oscillator harmonic distortion without preemphasis and deemphasis;
AF signal routed in at pin 1; AF amplitude = 150 mV_{rms}; AF filter 30 Hz to 20 kHz; detector (*P*+*P*)/2; measurement in accordance with CCIR 468-2 DIN 45405; test circuit 1a

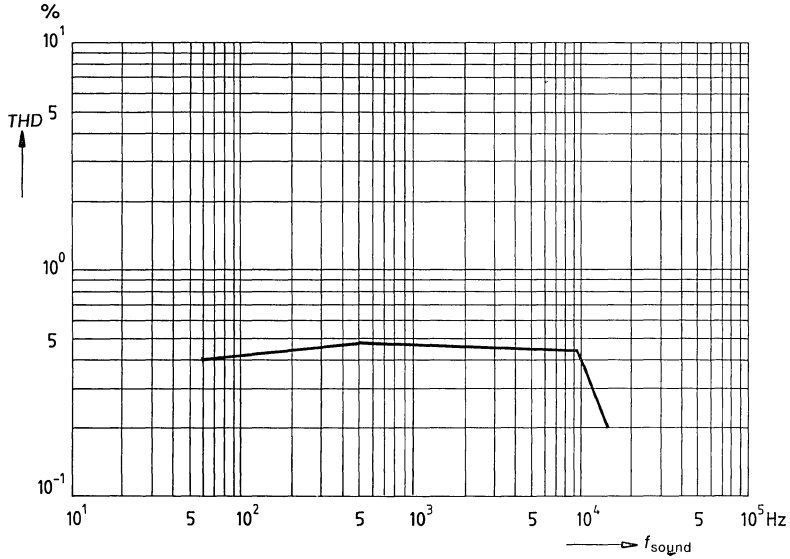


Figure 18 b

Sound oscillator frequency without preemphasis and deemphasis;
AF signal routed in at pin 1; AF amplitude = 150 mV_{rms}; AF filter 30 Hz to 20 kHz; detector (P+P)/2; measurement in accordance with CCIR 468-2 DIN 45405; test circuit 1a

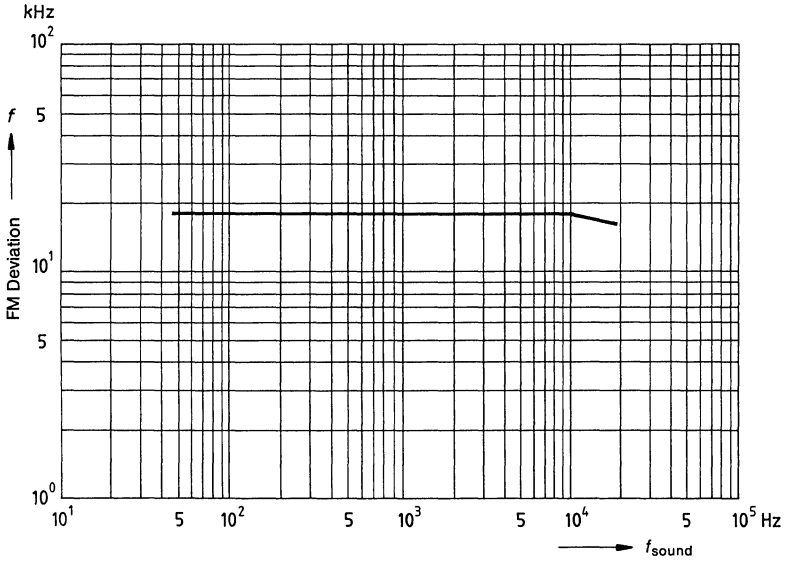


Figure 18 c

Sound oscillator frequency with pre-/deemphasis;
AF filter 30 Hz to 20 kHz; measurement in accordance with CCIR 468-2 DIN 45405; test circuit 1; $V_{AF} = 1\ V_{rms}$

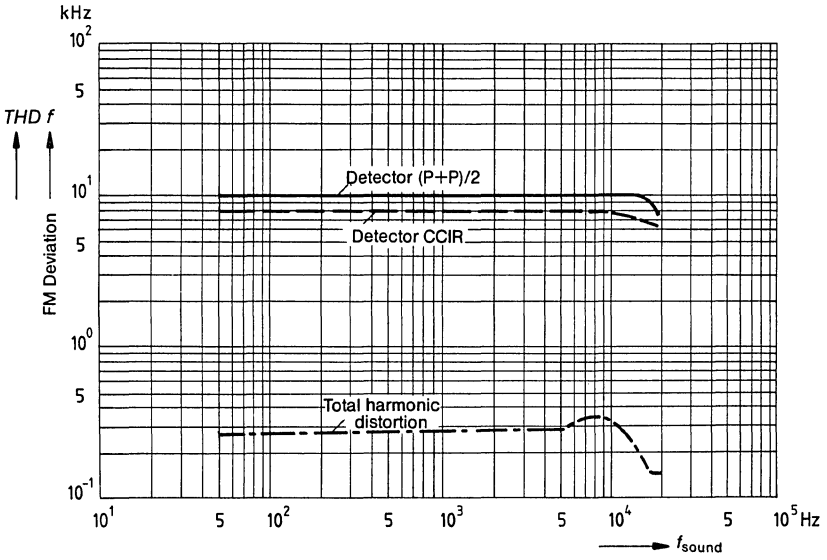


Figure 18 d

Description of the measurement configuration to measure the video signal control characteristics and the dynamic signal suppression in video frequencies

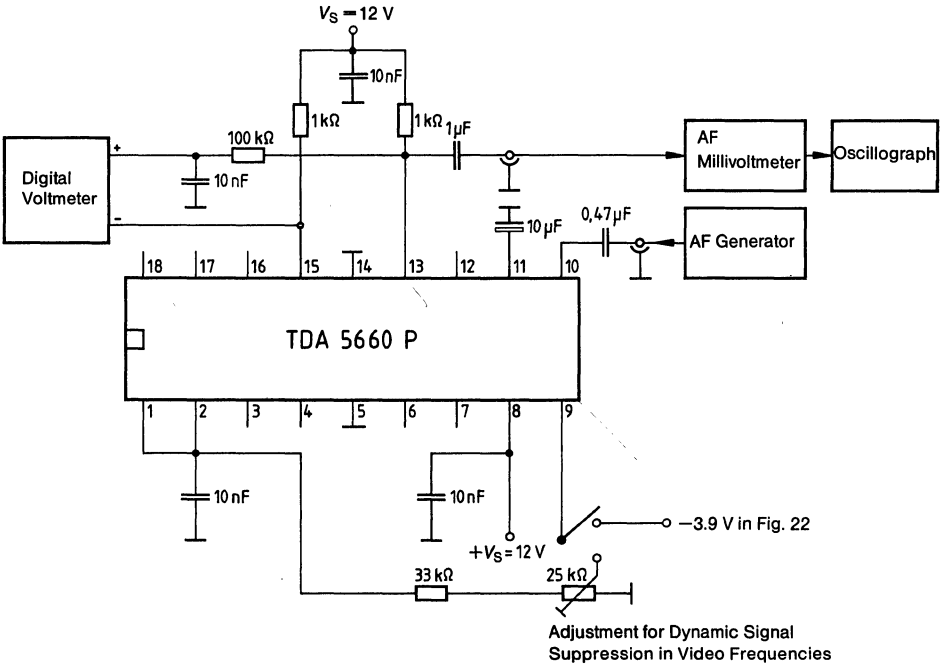
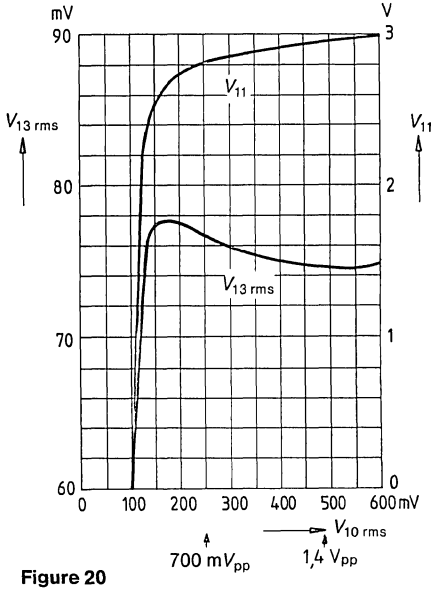


Figure 19

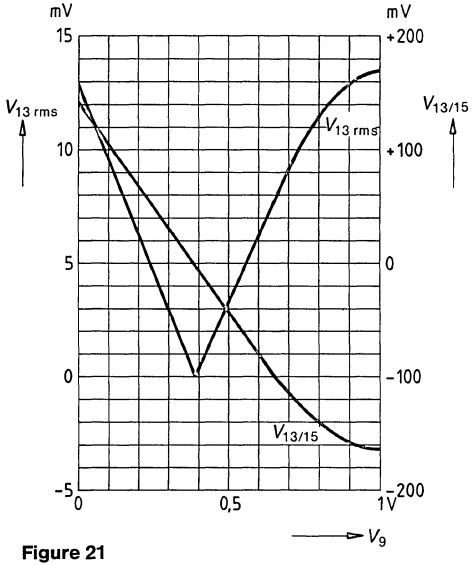
Characteristic of the video signal control circuit



a) $V_{13\,rms} = f(V_{10\,rms})$; $f_{mod} = 100$ kHz
b) $V_{11} = f(V_{10\,rms})$; $V_9 = 3.9$ V

Figure 20

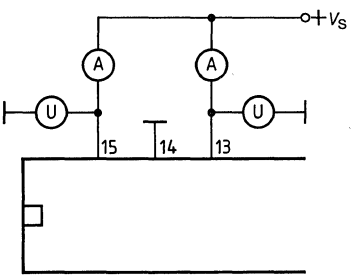
Static and dynamic mixer test with respect to balance characteristics based on a typical component



$V_{13/15} = f(V_9)$
$V_{13\,rms} = f(V_9)$
$f = 10$ kHz

Figure 21

Measurement of the static output impedance



$$Z_{15} = \frac{\Delta V_{15}}{\Delta I_{15}}$$

$$Z_{13} = \frac{\Delta V_{13}}{\Delta I_{13}}$$

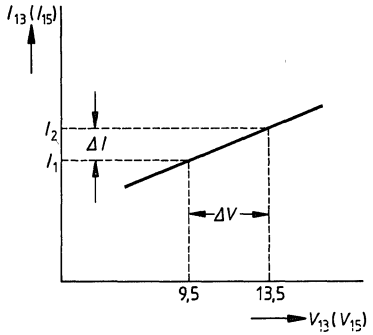
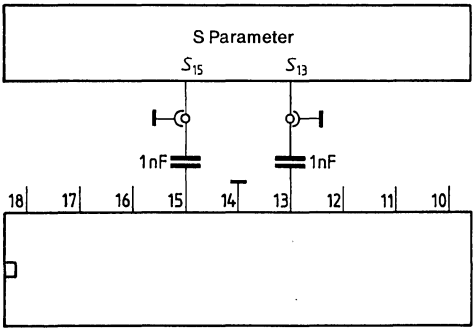


Figure 22

Output circuit S parameter



Typ. output capacity is approx. 1 pF

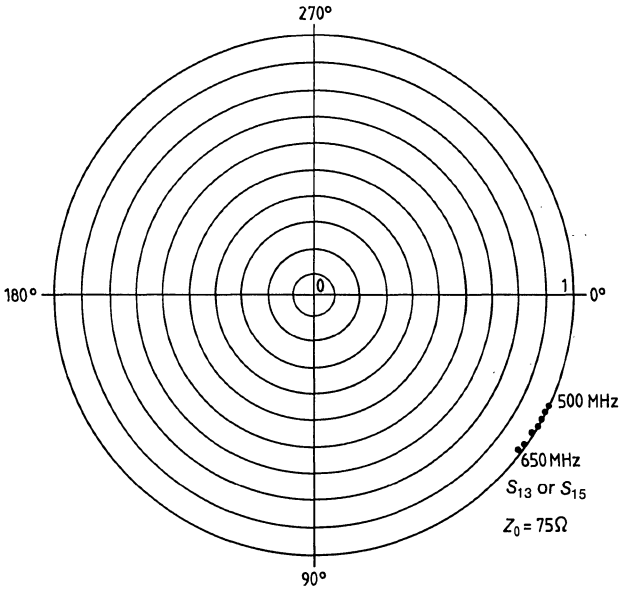
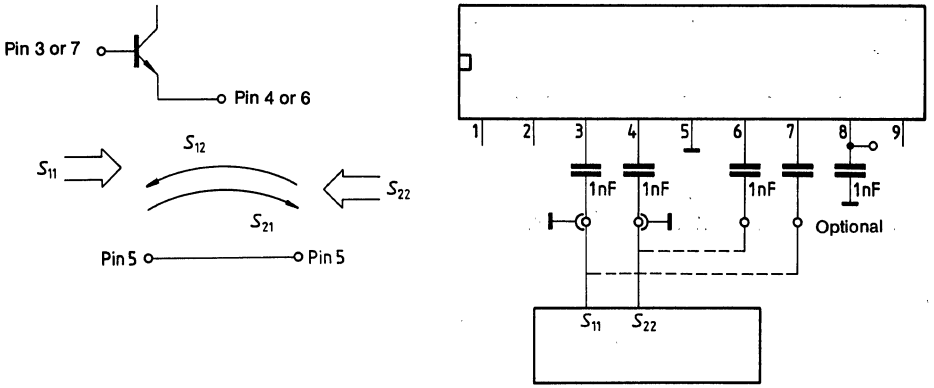


Figure 23

Oscillator section S parameter



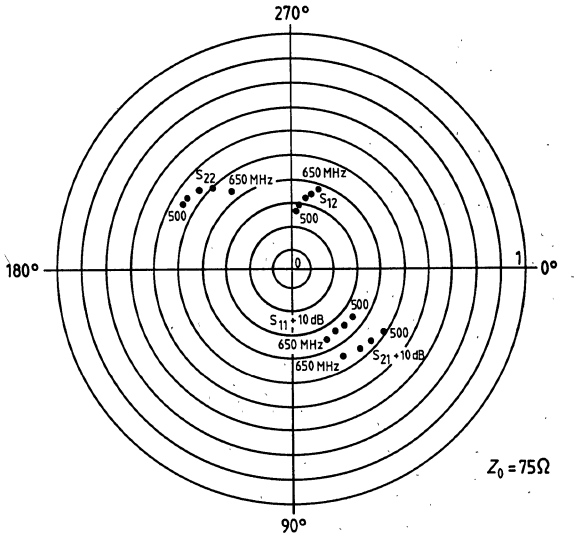
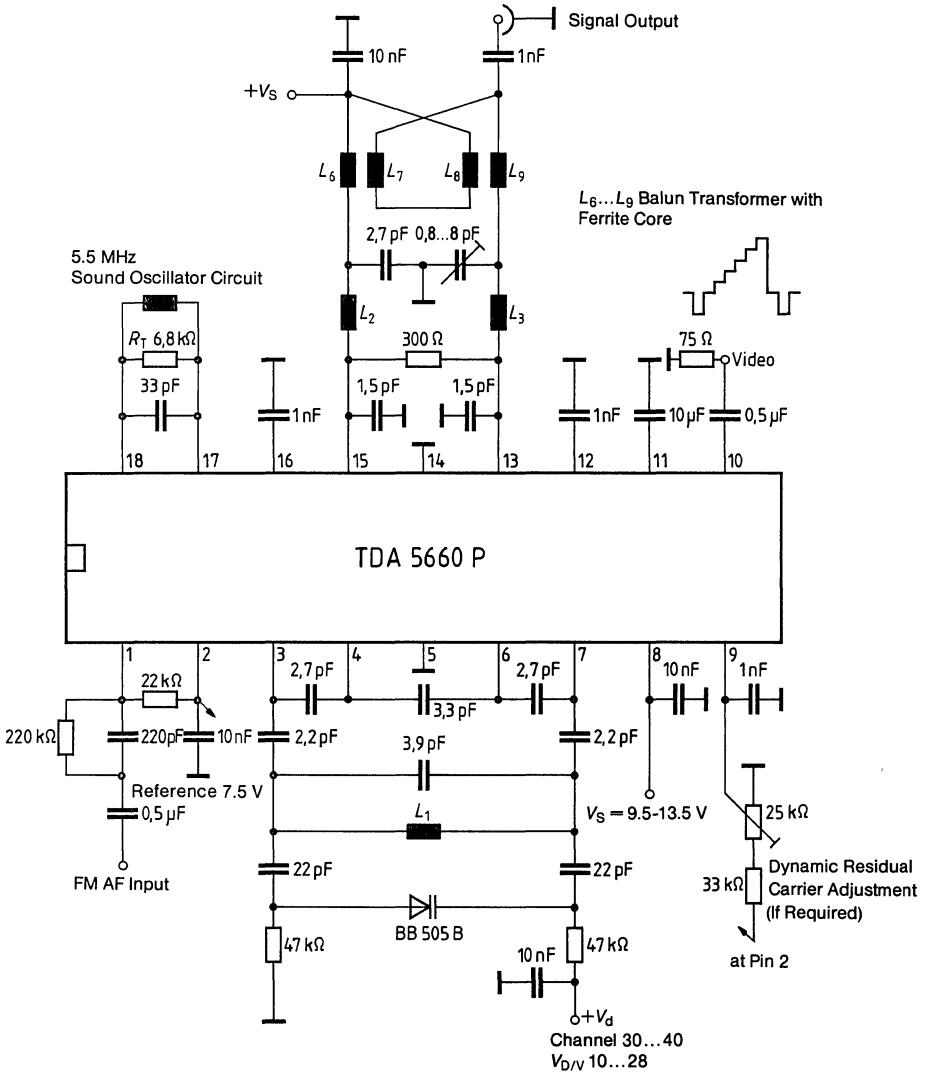
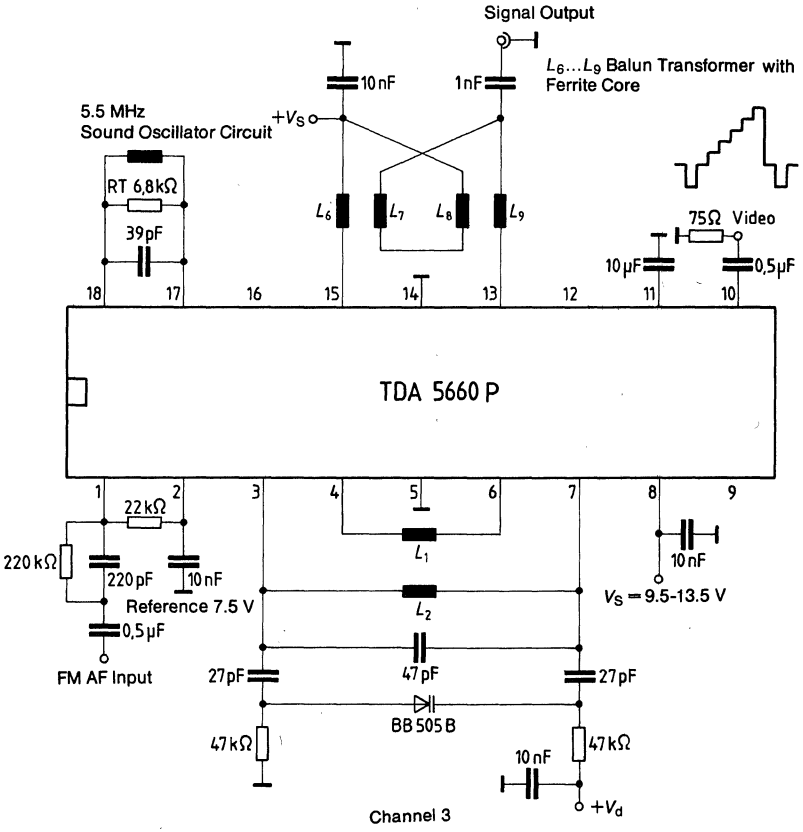


Figure 24

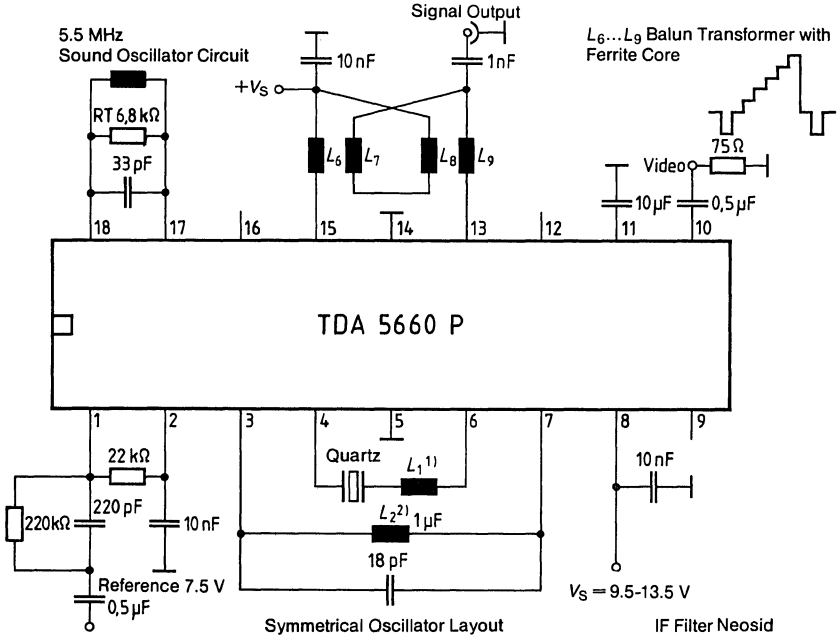
Application circuit 1



Application circuit 2



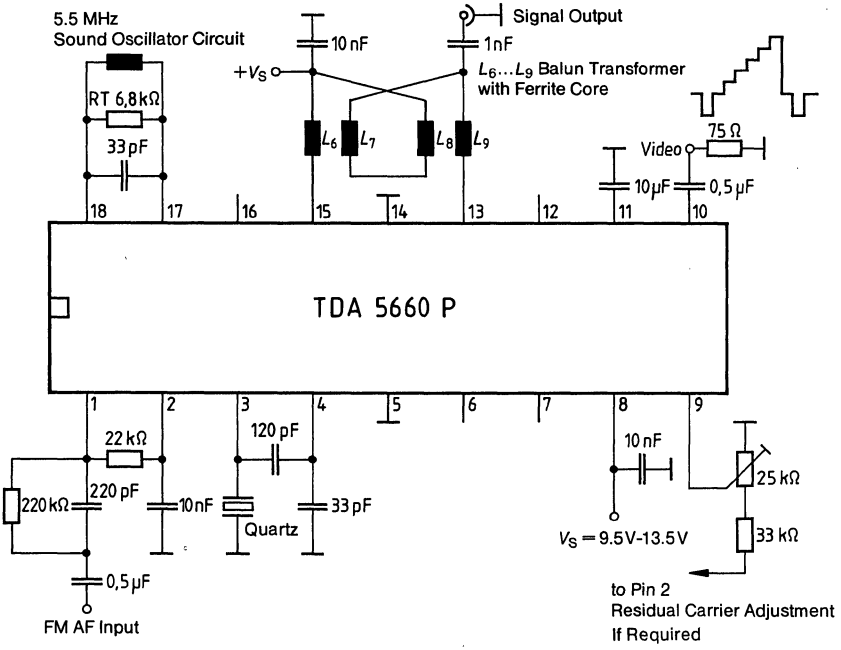
Application circuit 3



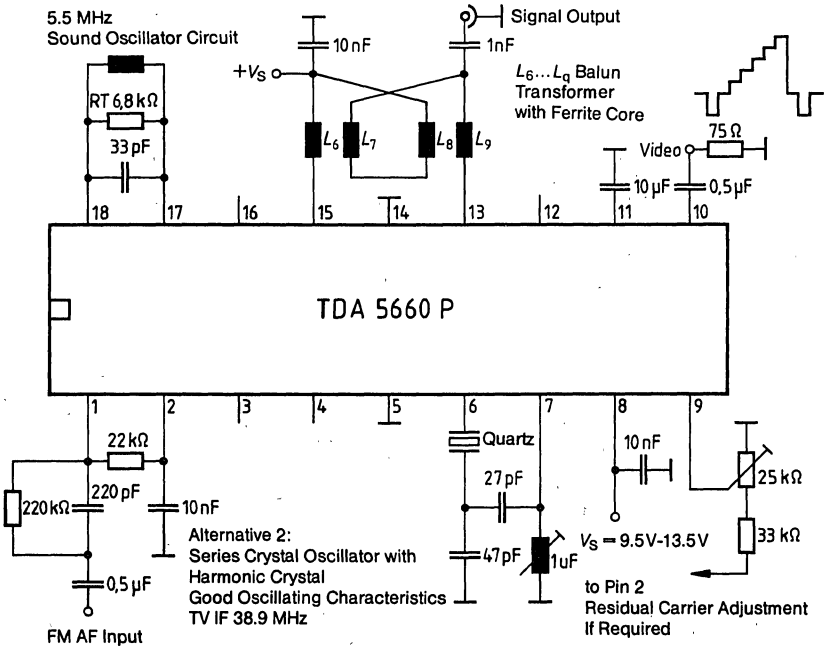
Symmetrical Oscillator Layout
Harmonic Crystal
Operated in Series Resonance
TV IF 38.9 MHz

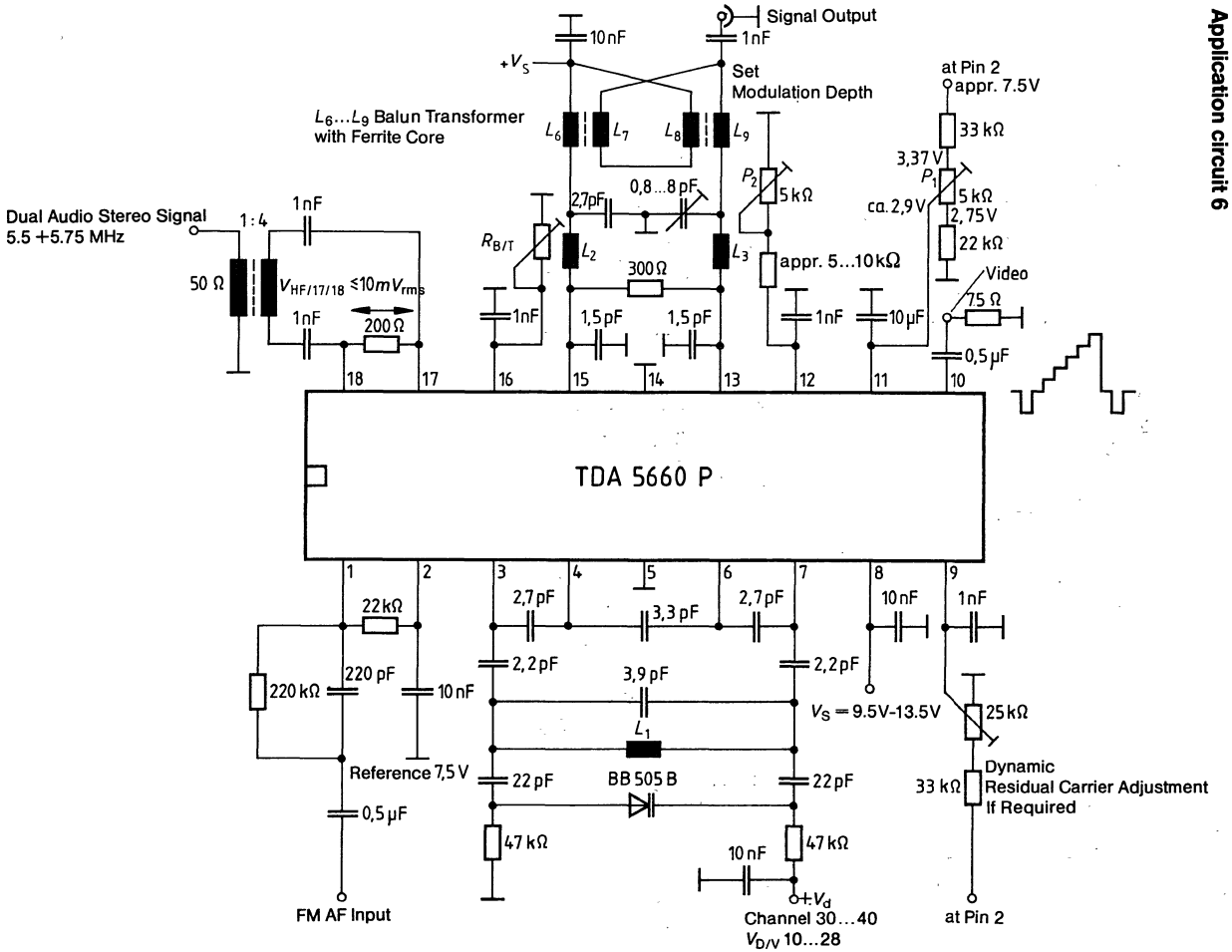
IF Filter Neosid
1) 2 Turns
2) 12 Turns

Application circuit 4



Application circuit 5




Signal Output
10nF
1nF
+V_S
Set
Modulation Depth
at Pin 2
appr. 7.5V
L_6...L_9 Balun Transformer
with Ferrite Core
L_6
L_7
L_8
L_9
33 kΩ
3,37 V
P_1
5 kΩ
ca. 2,9 V
2,75 V
22 kΩ
P_2
5 kΩ
2,7pF
0,8...8 pF
Dual Audio Stereo Signal
5.5 +5.75 MHz
1:4
1nF
$R_{B/T}$
L_2
L_3
appr. 5...10 kΩ
Video
75 Ω
50 Ω
$V_{HF/17/18}$ ≤10mV_{rms}
300 Ω
1nF
1,5 pF
1,5 pF
1nF
10µF
0,5µF
1nF
200 Ω
18
17
16
15
14
13
12
11
10
TDA 5660 P
1
2
3
4
5
6
7
8
9
22 kΩ
2,7 pF
3,3 pF
2,7 pF
10nF
1nF
220 kΩ
220 pF
10nF
2,2 pF
3,9 pF
2,2 pF
V_S = 9.5V-13.5V
L_1
25 kΩ
Reference 7,5 V
22 pF
BB 505 B
22 pF
33 kΩ
Dynamic
Residual Carrier Adjustment
If Required
0,5µF
47 kΩ
10nF
47 kΩ
+V_d
FM AF Input
Channel 30...40
$V_{D/V}$ 10...28
at Pin 2

Modulator for TV, Video and Sound Signals — TDA 5660 X

SO 20

The monolithically integrated circuit TDA 5660 X is especially suitable as modulator for the 48 to 860 MHz frequency range and is applied e.g. in video recorders, cable converters, TV converter installations, demodulators, video generators, video security systems, amateur TV applications, as well as personal computers.

- Synchronizing level-clamping circuit
- Peak white value gain control
- Continuous adjustment of modulation index for positive and negative modulation
- Dynamic residual carrier setting
- FM sound modulator
- Picture carrier to sound carrier adjustment
- Symmetrical mixer output
- Symmetrical oscillator with own RF ground
- Low radiation
- Superior frequency stability of main oscillator
- Superior frequency stability of sound oscillator
- Internal reference voltage

Circuit description

Via pin 2, the sound signal is capacitively coupled to the AF input for the FM modulation of the oscillator. An external circuitry sets the preemphasis. This signal is forwarded to a mixer. At the output of the mixer the FM modulated sound signal is added to the video signal and mixed with the oscillator signal in the RF mixer. A parallel resonant circuit is connected to the sound carrier oscillator at pin 18, 19. The unloaded Q of the resonant circuit must be $Q = 25$ and the parallel resistor $R_T = 6.8\ k\Omega$ to esnure a picture to sound carrier ratio of 12.5 dB. At the same time, the capacitative and/or inductive reactance for the resonance frequency should have a value of $X_C \approx X_L \approx 800\ \Omega$.

The video signal with the negative synchronous level is capacitively connected to pin 10. The internal clamping circuit is referenced to the synchronizing level. Should the video signal change by 6 dB, this change will be compensated by the resonant circuit which is set to the peak white value. At pin 12, the current pulses of the peak white detector are filtered through the capacitor which also determines the control time constant. When pin 13 is connected to ground, the RF carrier switches from negative to positive video modulation.

With the variable resistor of $R = \infty \ldots 0\ \Omega$ at pin 13 the modulation depth, beginning with $R = \infty$ and a negative modulation of $m_{D/N} = 80\%$, can be increased to $m_{D/N} = 100\%$ and continued with a positive modulation of $m_{D/P} = 100\%$ down to $m_{D/P} = 88\%$ with $R = 0\ \Omega$. The internal reference voltage has to be capacitively blocked at pin 2.

The amplifier of the RF oscillator is available at pins 4-8. The oscillator operates as a symmetrical ECO circuit. The capacitive reactance for the resonance frequency should be $X_C \approx 70\ \Omega$ between pins 4, 5 and 7, 8 and $X_C \approx 26\ \Omega$ between pins 5, 7. In order to set the required residual carrier suppression, pin 10 is used to compensate for any dynamic asymmetry of the RF mixer during high frequencies of > 300 MHz. The oscillator chip ground, pin 6, should be connected to ground at the oscillator resonant circuit shielding. Via pin 4 and 8 an external oscillator signal can be injected inductively or capacitively. The peripheral layout of the pc board should be provided with a minimum shielding attenuation of approx. 80 dB between the oscillator pins 4-8 and the modulator outputs 14–16.

For optimum residual carrier suppression, the symmetric mixer outputs at pins 14-16 should be connected to a matched balanced-to-unbalanced broadband transformer with excellent phase precision at 0 and 180 degrees, e.g. a Guanella transformer. The transmission loss should be less than 3 dB. In addition, an LC low pass filter combination is required at the output. The cut-off frequency of the low pass filter combination must exceed the maximum operating frequency.

If the application circuit according to figure 1, 2 is used, a multiplication factor V/RF (application) = V/RF (data sheet) 3.9 must be used to convert a 300 Ω symmetrical impedance to an asymmetrical impedance of 75 Ω for the stated RF output voltage V_q of the type specification in order to ensure a transmission attenuation of 0 dB for the balanced-to-unbalanced mixer.

Maximum ratings

		min	max		Remarks
Supply voltage	V_S	−0.3	14.5	V	
Current from pin 2	$-I_2$	0	2	mA	$V_2 = 7$ to 8 V $V_S = 9.5$ to 13.5 V
Voltage at pin 1	V_1	$V_2 - 2$	$V_2 + 2$	V	$V_S = 9.5$ to 13.5 V
Voltage at pin 9	V_9	−4	1	V	
Voltage at pin 10	$V_{10\,pp}$		1.5	V	only via C (max. 1 µF)
Capacitance at pin 2	C_2	0	100	nF	
Capacitance at pin 11	C_{11}	0	15	µF	
Voltage at pin 12	V_{12}	−0.3	1.4	V	
Voltage at pin 13	V_{13}	V_2	V_S	V	
Voltage at pin 15	V_{15}	V_2	V_S	V	
Voltage at pin 16	V_{16}	$V_2 - 1.5$	$V_2 + 1.5$	V	$V_S = 9.5$ to 13.5 V
Only the external circuitry shown in application circuits 1 and 2 may be connected to pins 3, 4, 6, 7, 17 and 18					
Junction temperature	T_j		150	°C	
Storage temperature	T_{stg}	−40	125	°C	
Thermal resistance (system-air)	$R_{th\,SA}$		80	K/W	

Operating range

Supply voltage	V_S	9.5	13.5	V	
Video input frequency	f_{VIDEO}	0	5	MHz	
Sound input frequency	f_{AF}	0	20	kHz	
Output frequency	f_q	48	860	MHz	depending on the oscillator circuitry at pins 3-7
Ambient temperature	T_A	0	70	°C	
Sound oscillator	f_{OSC}	4	7	MHz	
Voltage at pin 13, 15	$V_{13,15}$	V_2	V_S	V	

Characteristics

V_S = 11 V; T_A = 25 °C

		Test conditions	Figure	min	typ	max	
Current consumption	I_8	I_2 = 0 mA	1; 2	22	30	40	mA
Reference voltage	V_2	$0 \leq I_2 \leq 1$ mA	1; 2	7	7.5	8	V
Oscillator frequency range	f_{OSC}	External circuitry adjusted to frequency		48		860	MHz
Turn-on start-up drift	Δf_{OSC}	TC value of capacitor in osc. circuit is 0; drift is referenced only to self-heating of the component t = 0.5-10 s; T_A = const.					
		Ch30	1; 2	0	−50	−500	kHz
		Ch 40	1; 2	0	−200	−500	kHz
Frequency drift as function of V_S	$-\Delta f_{OSC}$	V_S = 9.5-13.5 V T_A = const.	1; 2	0			
		Ch 40		−150		150	kHz
Video input current at pin 10	$-I_{10}$	$C_{10} \leq 1$ µF	5	0		10	µA
Video input voltage at pin 10	$V_{10\,pp}$	at coupling capac. $C \leq 1$ µF $I_{leak} \leq \pm 0.3$ µA	21; 22	0.7		1.4	V
Modulation depth	$m_{D/N}$	neg. mod.	1; 16	75	80	85	%
$V_{VIDEO\,pp}$ = 1 V; f_{VIDEO} = 200 kHz sine signal	$m_{D/P}$	pos. mod.	2; 16	83	88	93	%
Output impedance	Z_{13}; Z_{15}	static	24	10			kΩ
RF output voltage	$V_{q\,rms}$	Ch 40	1b	2.5	3.5	5.5	mV
Modulation signal in neg. modulation pin 12 open							
Output capacitance	C_{13}=C_{15}		25	0.5	1	2.0	pF
S parameter at pins 3, 4 and 6, 7			26				
RF output phase	$\alpha_{13,15}$			140	180	220	degrees
RF output voltage change; adjustment range	ΔV_q	f = 543.25-623.25 Δf = 80 MHz Ch 30-Ch 40	1	0		1.5	dB
RF output voltage change	ΔV_q	f = 100-300 MHz	6	0		1.5	dB
RF output voltage change	ΔV_q	f = 48-100 MHz	6	0		1.5	dB
Oscillator interference FM caused by AM modulation and coupling of the modulator output with the oscillator resonant circuit; $V_{VIDEO\,pp}$ = 1 V; f_{VIDEO} = 10 kHz; sine signal							
	Ch 30		1; 9	0	5	15	kHz
	Ch 40		1; 9	0	7	21	kHz

Characteristics

$V_S = 11$ V; $T_A = 25$ °C

		Test conditions	Figure	min	typ	max	
Intermodulation ratio	a_{MR}	$f_P + 1.07$ MHz	1; 7; 15	54	75		dB
Harmonic wave ratio	a_H	$f_P + 8.8$ MHz without video signal 19, 20, 21 unmodulated video and sound carrier, measured with the spectrum analyzer as difference between video carrier signal level and sideband signal level without video and sound modulation.	1; 7; 15	35			dB
Harmonic wave ratio	a_H	$f_P + 2f_S$	1; 7	35	48		dB
Harmonic wave ratio	a_H	$f_P + 3f_S$ V_q with spectrum analyzer; loaded Q factor Q_L of the sound oscillator resonant circuit adjusted by R_S to provide the required picture to sound carrier ratio of 12.5 dB; $R_S = 6.8$ kΩ; $Q_U = 25$ of the sound oscillator circuit.	1; 7	42	48		dB
Sound carrier ratio	$a_{P/S}$		1; 7; 17	10	12.5	15	dB
Color picture to sound carrier ratio	a_P	$f_P + 4.4$ MHz (dependent on video signal)	1		17		dB
All remaining harmonic waves	a	Multiple of fundamental wave of picture carrier, without video signal, measured with spectrum analyzer; $f_{P/S} = 523.25$-623.25 MHz	1	15			dB
Amplitude response of the video signal	a_V	$V_{VIDEO\,pp} = 1$ V with additional modulation $f = 15$ kHz-5 MHz sine signal between black and white	1; 13	0		1.5	dB
Residual carrier suppression	a_R	With adjustment at pin 9 Ch 30...Ch 40	1; 12	32			
Static mixer balance characteristic	$\Delta V_{13/15}$	V_9 adjusted to $\Delta V_{13/15}$ minimum	21; 23	−100	0	+100	mV
Dynamic mixer balance characteristics	$V_{13\,rms}$	V_9 adjusted to $V_{13\,rms}$ minimum	21; 23		0	10	mV
Stability of set modulation depth	Δm_D	Video input voltage changes with sine signals $f = 0.2$ MHz; $\Delta V_{VIDEO\,pp} = 1$ V ± 3 dB; Ch 30...Ch 40; $V_S = 12$ V; $T_A = $ const.			1	±2.5	%
Stability of set modulation depth	Δm_D	$f = 48$...100 MHz	6		1	±2.5	%
Stability of set modulation depth	Δm_D	$f = 100$...300 MHz	6		2	±4	%
Stability of set modulation depth	Δm_D	$T_A = 0$-60 °C; $V_S = 12$ V	1		1	±2.5	%

Characteristics

$V_S = 11$ V; $T_A = 25$ °C

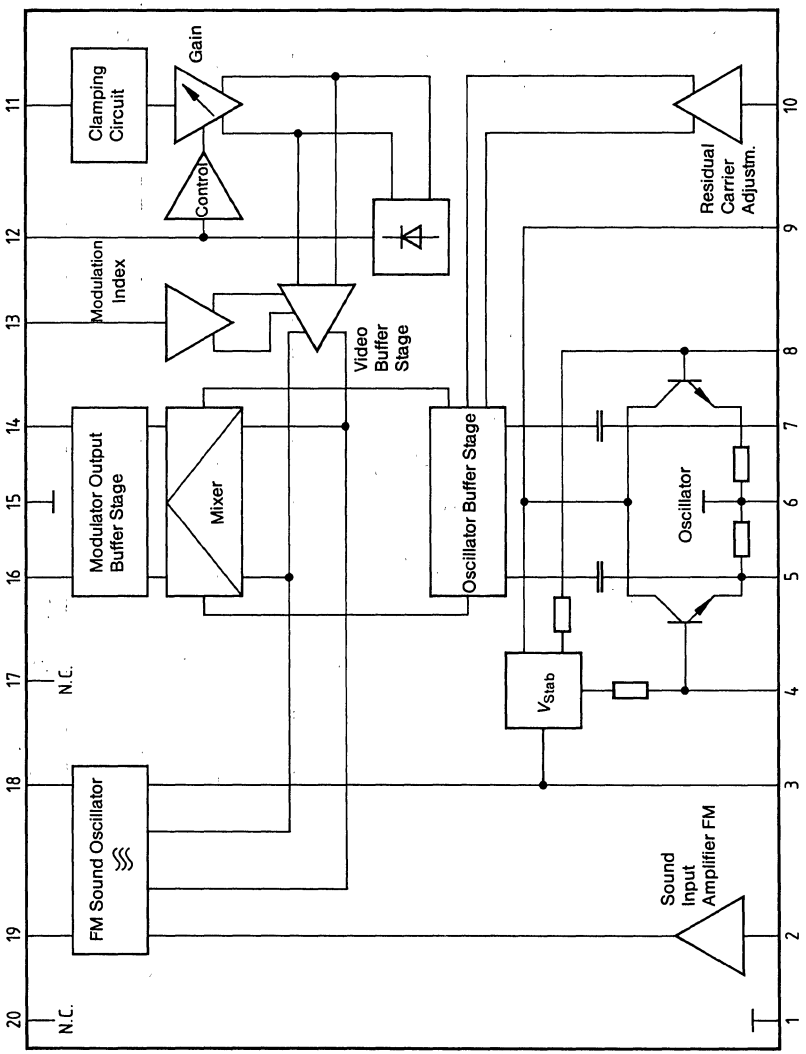
		Test conditions	Figure	min	typ	max	
Stability of set modulation depth	Δm_D	$V_S = 9.5\text{-}13$; 5 V; T_A = const.	1		1	±2.5	%
Interference product ratio sound in video; sound carrier FM mod.	$a_{S/P}$	Ch 30...Ch 40	1; 11	48	60		dB
Signal-to-noise ratio in video; sound carrier unmodulated	$a_{N/P}$	Ch 30...Ch 40	1; 11	48	74		dB
Unweighted FM noise level ratio video in sound; FuBK test picture as video signal	$a_{P/S}$	Ch 39	1a; 8	48	54		dB
Unweighted FM noise level ratio video in sound	$a_{P/S}$	Ch 39; test picture VU G-Y; U/V	2; 8	48	56		dB
		Ch 39; color bar	2; 8	46	52		dB
		Ch 39; uniform red level	2; 8	48	58		dB
		Ch 39; uniform white level	2; 8	45	51		dB
		Ch 39; test pattern	2; 8	48	55		dB
		Ch 39; white bar	2; 8	46	52		dB
		Ch 39; bar	2; 8	45	50.8		dB
		Ch 39; 20T/2T	2; 8	43	49		dB
		Ch 39; 30% white level	2; 8	48	58		dB
		Ch 39; 250 kHz	2; 8	46	52		dB
		Ch 39; multiburst	2; 8	46	53		dB
		Ch 39; ramp	2; 8	44	50		dB
Signal-to-noise ratio of sound oscillator	$a_{S/N}$		1a; 8	48	54		dB
Differential gain	G_{dif}	measured with measurement demodulator, video test signals and vector scope	1			10	%
Differential phase	φ_{dif}		1			15	%
Period required for peak white detector to reach steady state for full modulation depth with 1 white pulse per half frame with control in steady state	t	C at pin 11 = 10 µF; $I_{leak} \leq 2$ µA	1		6	50	µs

Characteristics

$V_S = 11$ V; $T_A = 25$ °C

		Test conditions	Figure	min	typ	max	
Setting time for video signal change from 0 V_{pp} to 1.4 V_{pp}	t	Video blanking signal content is uniform white level	1		120	500	µs
Setting time for video blanking signal from 100% white level to 42% grey level with subsequent rise in grey level to 71% of video blanking signal (due to decontrol process)	t		1		2.25	5	s
Sound oscillator frequency range	$f_{S/OSC}$	Unloaded Q factor of resonant circuit $Q_U = 25$; resonance frequency 5.66 MHz	1	4		7	MHz
Turn-on start-up drift	$\Delta f_{S/OSC}$	Capacitor TC value in sound oscillator circuit is 0, drift is based only on component heating T_A = const.; $f_{S/OSC} = 5.5$ MHz	1		5	15	kHz
Sound oscillator frequency operating voltage	$\Delta f_{S/OSC}$	$V_S = 9.5$-13.5 V; $f_{S/OSC} = 5.5$ MHz; T_A = const.; $Q_U = 25$	1		5	15	kHz
FM mod. harmonic distortion	THD_{FM}	$V_{1\,rms} = 150$ mV	19; 19a		0.6	1.5	%
Audio preamplifier input impedance (dyn.); FM operation	Z_1		1	200			kΩ
FM sound modulator, static modulation characteristic	$\Delta f_{S/OSC}$	$\Delta V_{1/2} = V_1 - V_2 = \pm 1$ V; $f_{S/OSC} = 5.5$ MHz; $Q_U = 25$	1; 14	±210	±270	±330	kHz
FM sound modulation characteristic (dynamic)	$\Delta f_M/\Delta V_1$		1a; 10a	0.3	0.38	0.46	kHz/mV

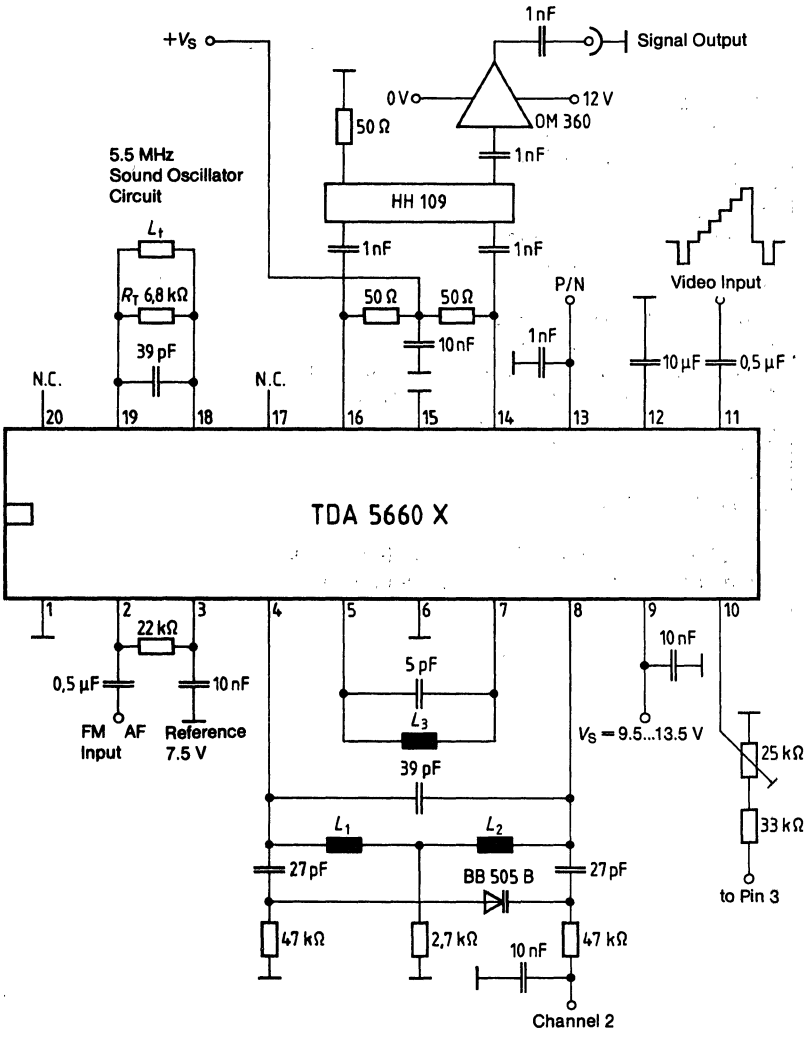
Block diagram



Pin description

Pin	Function
1	GND
2	AF input for FM modulation
3	Intenal reference voltage
4	Symmetrical oscillator input
5	Symmetrical oscillator output
6	Oscillator ground
7	Symmetrical oscillator output
8	Symmetrical oscillator input
9	Supply voltage
10	Dynamic residual carrier adjustment
11	Video input with clamping
12	Connection for smoothing capacitor for video control loop
13	Switch for positive and negative modulation as well as for residual carrier control
14	Symmetrical RF output
15	GND
16	Symmetrical RF output
17	N.C.
18	Sound oscillator symmetrical input for tank circuit
19	Sound oscillator symmetrical input for tank circuit
20	N.C.

Measurement circuit



Video IF section

Controlled AM broadband amplifier with synchronous demodulator, video amplifier, VTR input and output, and AGC voltage generation for the video IF amplifier and tuner.

Quasi-parallel sound section

Controlled AM broadband amplifier with quadrature demodulator, sound carrier output, and internal AGC voltage generation.

The TDA 5830-2 is especially suitable for application with black and white or color television receivers and/or VTR systems with PNP/MOS tuners for TV standards with negative video modulation and FM sound.

Circuit description

The video IF section is comprised of a 4-stage controllable AM amplifier, a limiter, and a mixer for the synchronous demodulation of video signals as well as an amplifier for the positive video output signal.

The positive video signal is used for gated control. In addition, the IC includes a standard VTR connection via an external transistor. The delayed tuner AGC is generated by a threshold amplifier driven by the control voltage.

The quasi-parallel sound section also includes a 4-stage AM amplifier, a limiter, and a mixer for the quadrature demodulation of the 1st sound IF with subsequent sound carrier output for the 2nd sound IF. The control voltage is generated by a peak value rectifier from the 1st sound IF signal.

Maximum ratings

		min	max	
Supply voltage	V_1		13	V
Max. dc voltage	$V_{2,3}$	V_5	V_1	V
Max. dc voltage	V_4	0	V_1	V
Max. dc current	I_5	−2	2	mA
Max. dc voltage	$V_{6,7}$	V_5	V_1	V
Max. dc voltage	$V_{8,9}$	0	V_1	V
Max. dc current	I_{10}	−1	3	mA
Max. dc current	$-I_{11}$	−1	3	mA
Max. dc voltage	V_{12}	−10	V_1	V
Max. dc voltage	$V_{13,14}$	0	V_1	V
Max. dc voltage	$V_{15,16}$	0	V_1	V
Max. dc voltage	$V_{18,19,20}$	0	V_1	V
Max. dc current	I_{21}	−1	2	mA
Junction temperature	T_j		150	°C
Storage temperature range	T_{stg}	−40	125	°C
Thermal resistance (system-air)	$R_{th\ SA}$		55	K/W

Operating range

Supply voltage	V_S	10.5	12.6	V
IF frequency	f_{IF}	15	75	MHz
Ambient temperature	T_A	0	70	°C

Characteristics

$V_S = 12$ V; $T_A = 25$ °C

		Test conditions	min	typ	max	
Current consumption	I_1			95		mA
Stab. reference voltage	$V_{5/22}$			6.7	7.0	V
Video IF						
Control current for tuner	I_{14}			4.5		mA
Tuner AGC threshold	$V_{4/22}$		0		4.0	V
Gating pulse voltage	V_{12}	pos. gating pulse	4.0		V_1	V
	V_{12}	neg. gate pulse	−10		−4.0	V
Input voltage at G_{max}	$V_{i15/16}$	$V_{11\,pp} = 3$ V		30	60	µV
AGC range	ΔG			60		dB
IF control voltage	$V_{13/22}$	G_{max}	0			V
	$V_{13/22}$	G_{min}			4.0	V
Video output voltage	$V_{q\,11\,pp}$	$R_L = \infty$		3.0		V
Sync pulse level	$V_{11/22}$			2.0		V
DC voltage						
$V_{13} = 4$ V; $V_{15/16} = 0$ V	$V_{11/22}$			5.3		V
Output current	$I_{q\,11}$	to ground via R		−5.0		mA
	$I_{q\,11}$	to plus $V_{11} = 7$ V		+2.0		mA
VTR output voltage (neg.)	$V_{q\,10\,pp}$	VTR record. $R_L = \infty$		2.0		V
Sync pulse level	$V_{10/22}$	VTR record. $R_L = \infty$		$V_1 - 1.6$		V
DC voltage						
$V_{13} \leq 5$ V; $V_{15/16} = 0$ V	$V_{10/22}$	VTR recording		$V_1 - 3.8$		V
DC voltage $V_{13} = 8$ V	$V_{10/22}$	VTR playback		$V_1 - 0.9$		V
Output current	$I_{q\,10}$	to ground via R		−5.0		mA
	$I_{q\,10}$	to plus $V_{10} = V_1$		+1.0		mA
Video amplifier	V_{video}	$V = V_{11}/V_9$;		3.0		
(VTR playback)		$V_{9\,pp} = 1$ V				
Quasi-parallel sound						
Sound carrier output voltage	V_{21}	$V_{i\,VC} = 1$ mV	10			mV
		$V_{i\,SC} = 300$ µV				
Input voltage at G_{max}	$V_{i18/19}$	$V_{21} = V_{21} - 3$ dB		50	100	µV
AGC range	ΔG	$V_{21} = V_{21} \pm 3$ dB		60		dB
Signal-to-noise-ratio		IEC 468				
White/staircase signal		Peak weighting		61		dB
Black picture				66		dB
Test conditions						
Video carrier/sound carrier				10		dB
Modulation frequency				1		kHz
Frequency deviation				50		kHz
IF input voltage				20		mV

Characteristics

$V_S = 12$ V; $T_A = 25$ °C

		Test conditions	min	typ	max	
Design-related characteristics						
Input impedance	$Z_{i\,15/16}$			1.8/2		kΩ/pF
	$Z_{i\,18/19}$			1.8/2		kΩ/pF
Output impedance	$Z_{q\,2/3}$			6.6/2		kΩ/pF
	$Z_{q\,6/7}$			6.6/2		kΩ/pF
Output resistance	R_{11}			150		Ω
Residual IF (fundamental wave)	V_{11}			10		mV
Video bandwidth (−3 dB)	B_{video}			6.0		MHz
Intermodulation ratio with reference to f_{CC}	α_{iM}	sound color interference		50		dB
Output resistance	$R_{q\,21}$			200		Ω
IF control voltage	$V_{20/22}$	G_{max}	0			V
	$V_{20/22}$	G_{min}			4	V

Alignment procedures

a) Video IF

At a video carrier input level of $V_{15/16\ rms} = 10$ mV and a superimposed AGC voltage of $V_{13} = 3$ V, the demodulator tank circuit is preliminary aligned so that the demodulated video signal $V_{11\ pp}$ reaches its maximum output level at the positive video output. Any suitable video test signal can be used for modulation. Subsequently, the AGC voltage V_{13} is reduced until the video signal equals approx. 3 V (peak-to-peak). By fine-aligning the demodulator tank circuit, the maximum output level of the video signal is reached. The flat response characteristic of the demodulator ensures a non-critical alignment procedure.

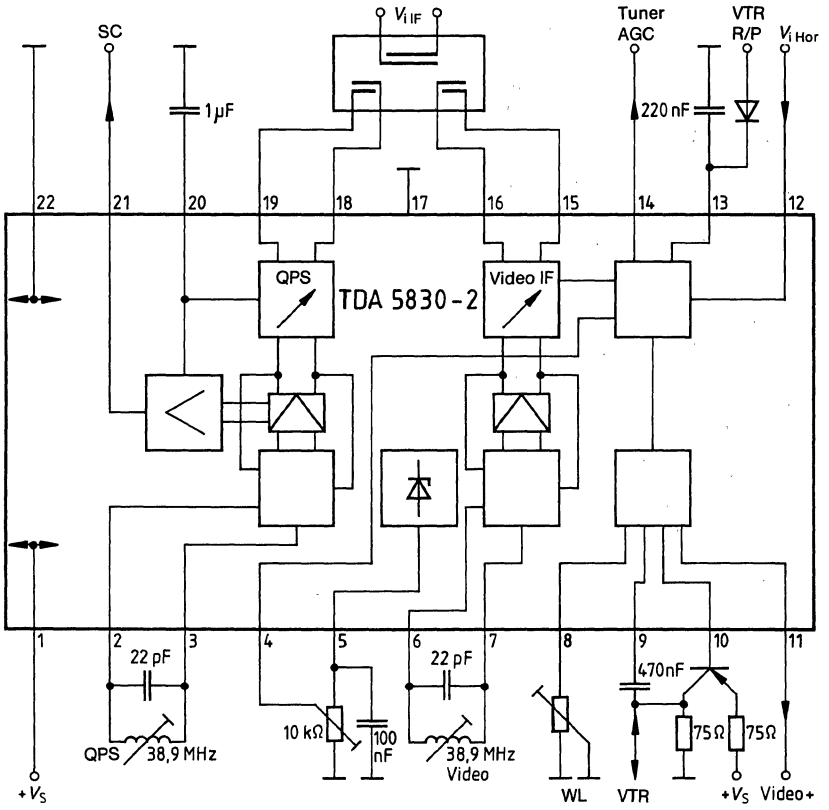
b) QPS

At an input signal of $V_{18/19\ rms} = 10$ mV, the demodulator tank circuit is preliminarily aligned until a max. AM suppression of the demodulated video signal V_{21} is reached at the sound carrier output. A video signal critical for the sound-interference ratio should be used for modulation (white/staircase, FuBK). Subsequent fine-aligning is performed by measuring the sound-interference ratio at the output of a FM demodulator and fine-aligning the demodulator tank circuit for a max. interference ratio. If several sound carriers are used in a device, the sound carrier with the lowest level should be used for alignment purposes.

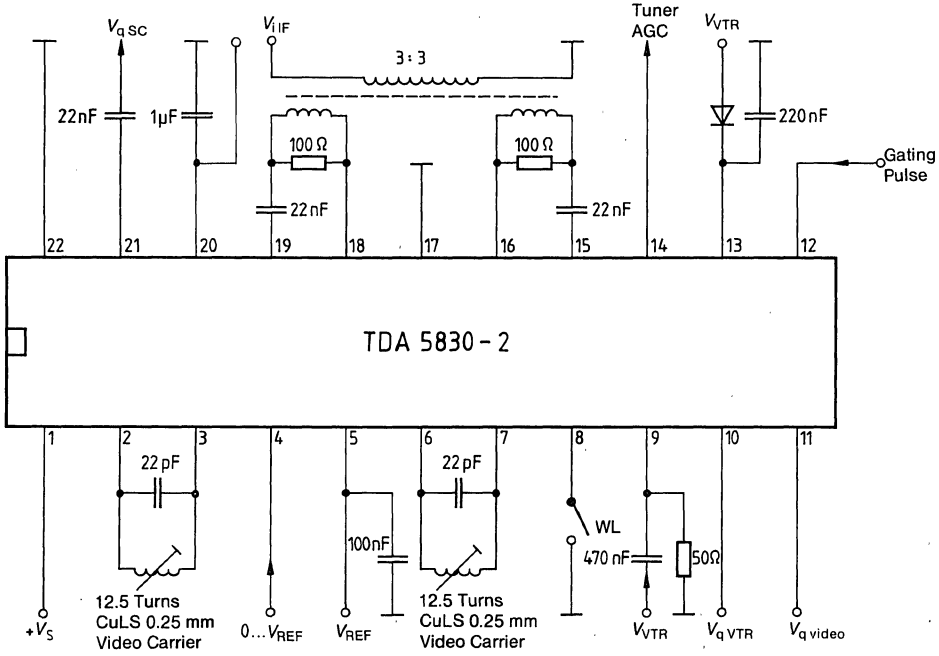
Pin description

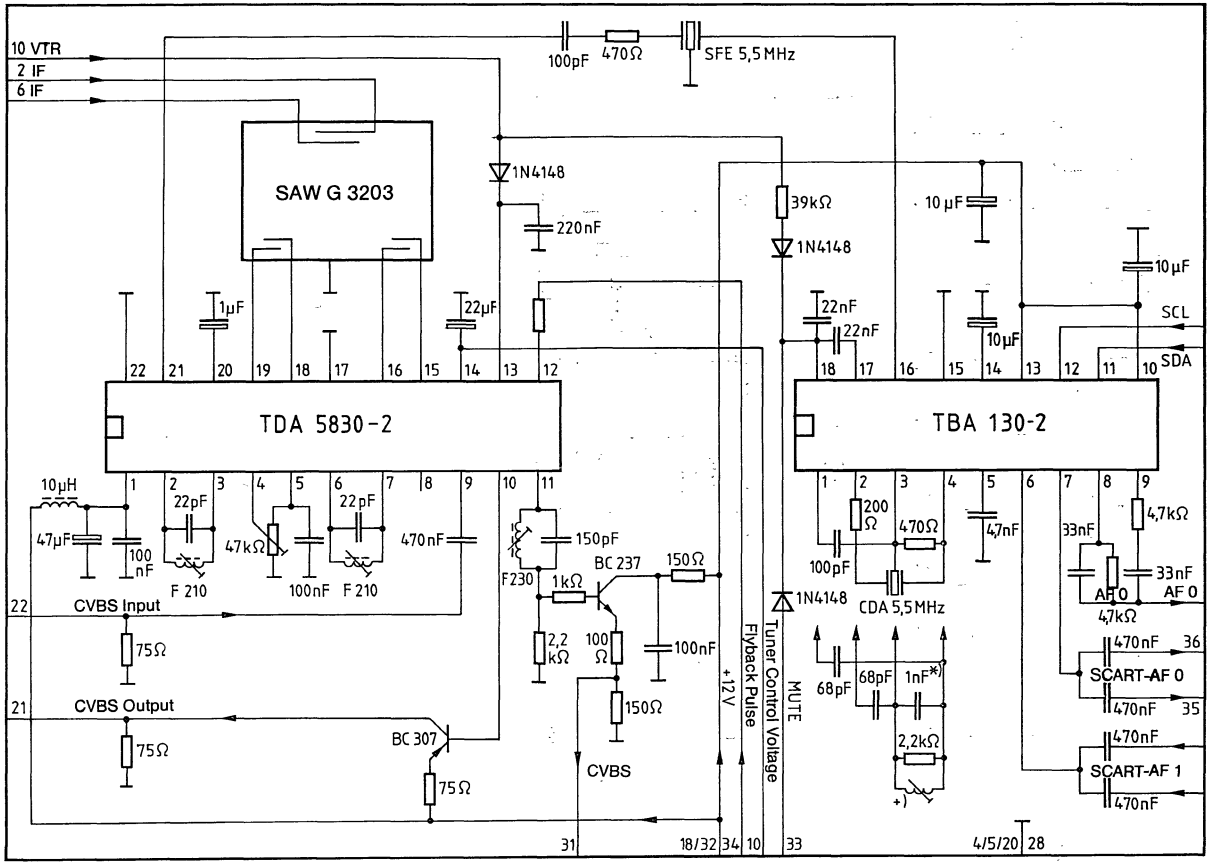
Pin	Function
1	Supply voltage
2	Demodulator tank circuit QPS
3	Demodulator tank circuit QPS
4	Tuner AGC threshold
5	Reference voltage
6	Demodulator tank circuit video IF
7	Demodulator tank circuit video IF
8	White level setting
9	VTR input
10	VTR output
11	Video output
12	Gating pulse input
13	AGC time constant video IF
14	Delayed tuner AGC
15	Video IF input
16	Video IF input
17	GND
18	QPS IF input
19	QPS IF input
20	AGC time constant QPS
21	Sound carrier output
22	GND

Block diagram

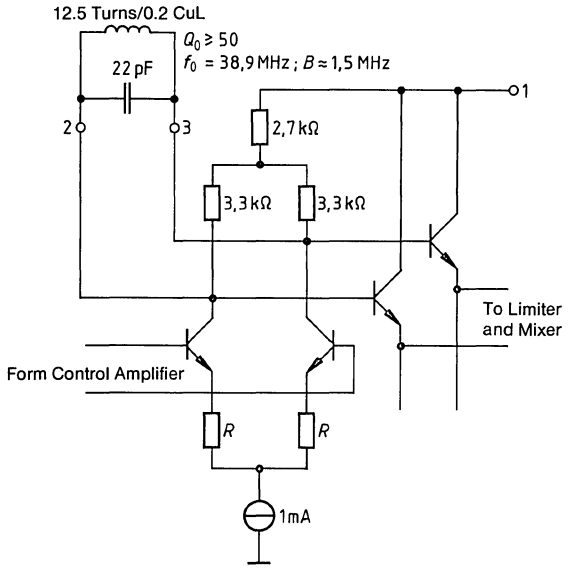


Measurement circuit

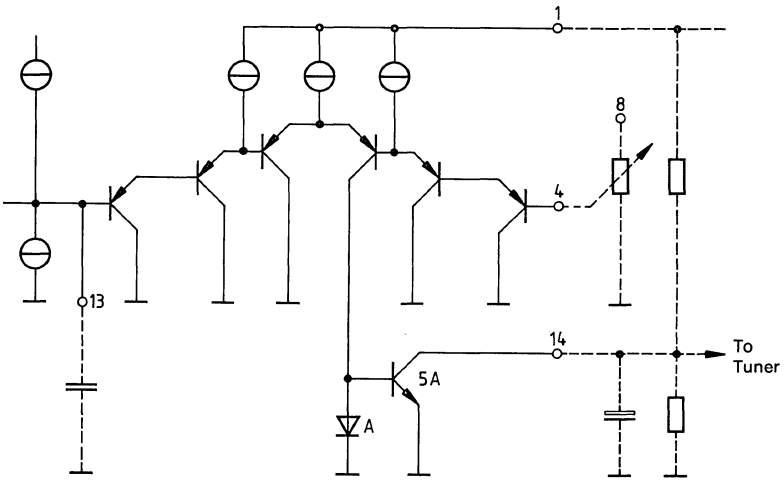



10 VTR
2 IF
6 IF
100pF
470Ω
SFE 5,5 MHz
SAW G 3203
1N4148
220nF
39kΩ
1N4148
10 µF
10µF
SCL
SDA
1µF
22µF
22nF
22nF
10µF
TDA 5830-2
TBA 130-2
10µH
47µF
100 nF
22pF
F 210
47kΩ
100nF
22pF
F 210
470nF
150pF
F230
BC 237
150Ω
1kΩ
2,2 kΩ
100 Ω
100nF
150Ω
CVBS Input
75Ω
CVBS Output
75Ω
BC 307
75Ω
CVBS
+12V
Flyback Pulse
Tuner Control Voltage
MUTE
1N4148
200 Ω
470Ω
100pF
CDA 5,5 MHz
68pF
68pF
1nF*)
2,2kΩ
+)
4,7nF
33nF
4,7kΩ
33nF
AF 0
AF 0
4,7kΩ
470nF
SCART-AF 0
470nF
470nF
SCART-AF 1
470nF
*) STYROFLEX Capacitor
*) L = 10 Turns, 0,2 CuL, $Q_L \approx 25$
e.g. with Vogt Coil Assembly 5171200000

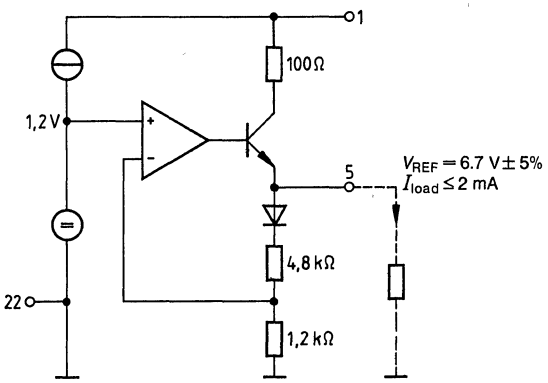
Demodulator tank circuit QPS



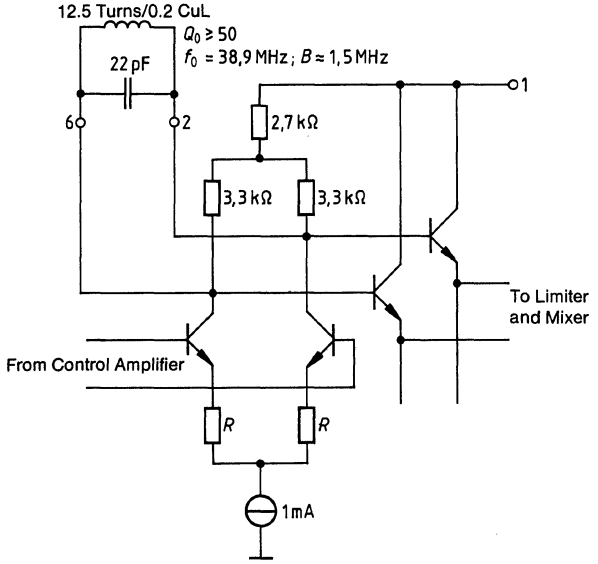
Tuner AGC threshold and output



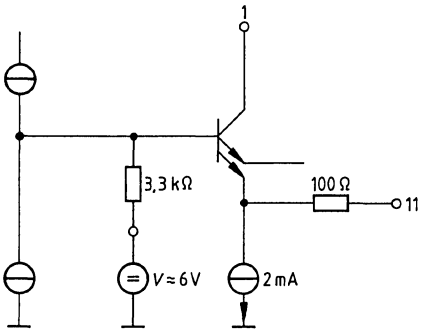
Reference voltage



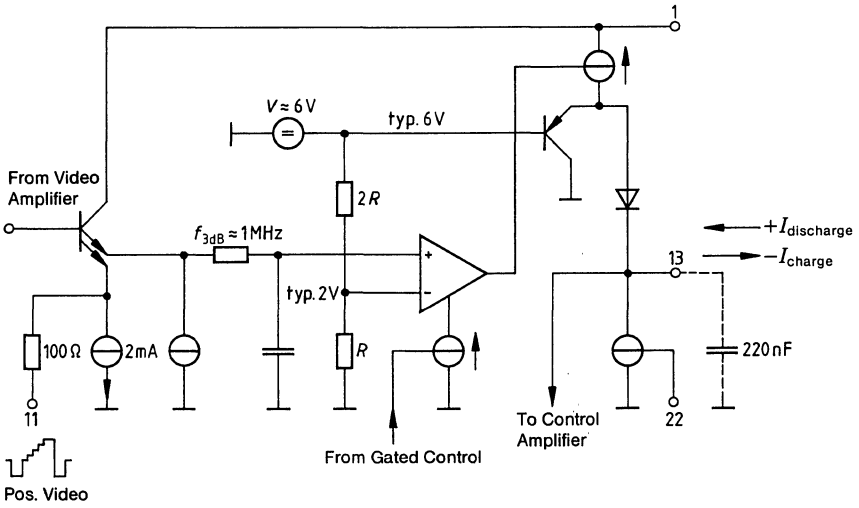
Demodulator tank circuit video IF



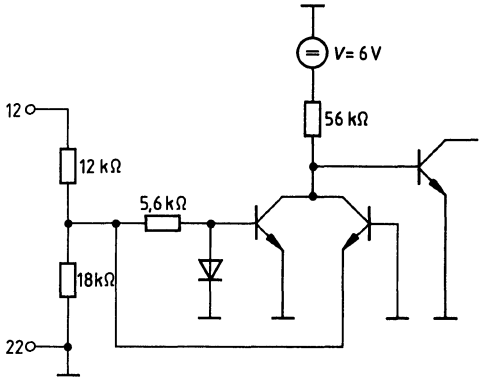
Positive video output



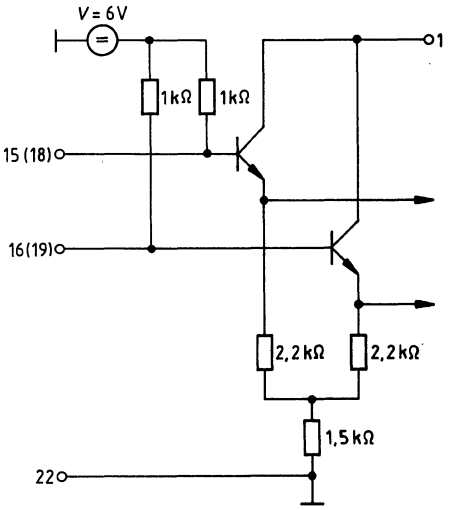
AGC time constant video IF



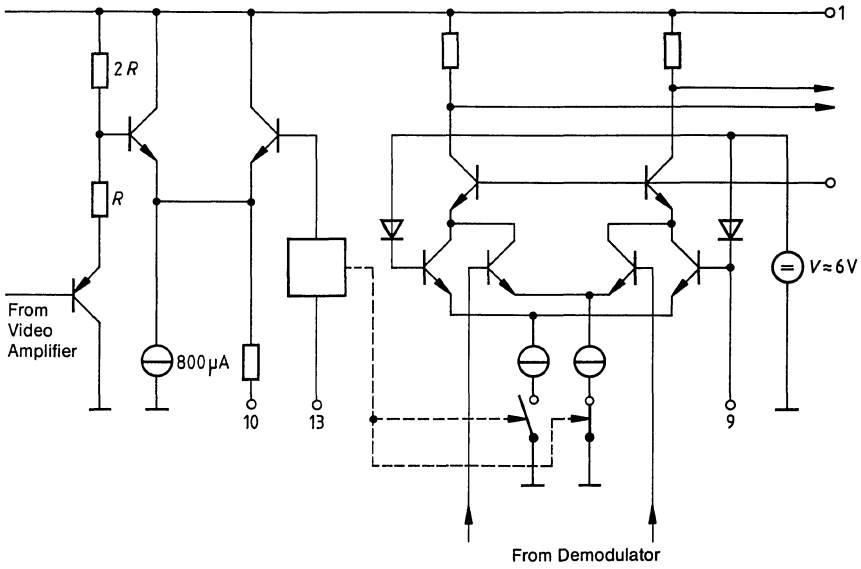
Gating pulse input



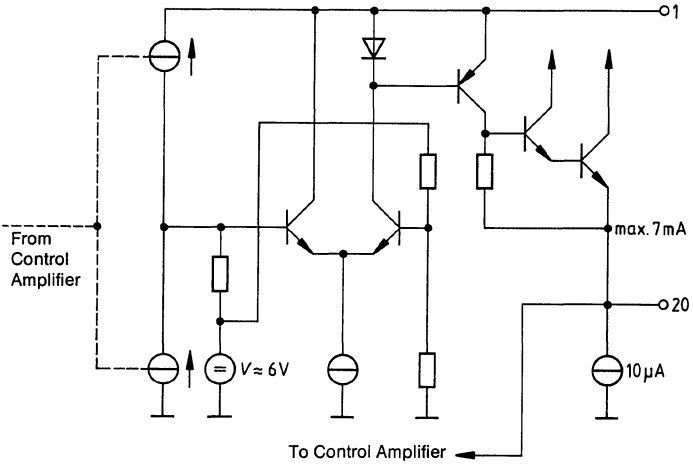
IF input video IF
IF input QPS



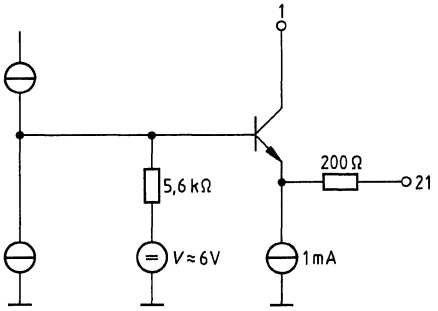
VTR interface



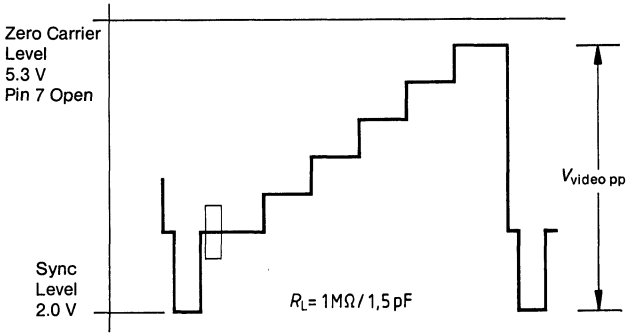
AGC time constant QPS



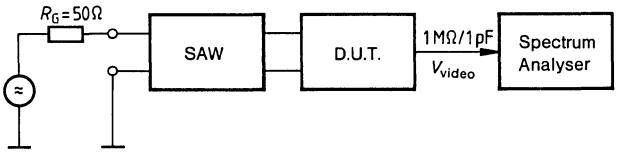
Sound carrier output QPS



AGC time constant QPS

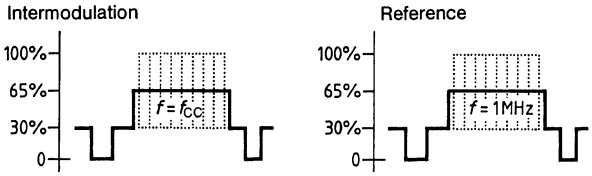


Measurement configuration



(SAW 351 D)
(SAW 361 S)

Test signal: $f_{VC} = 38.9$ MHz with test signal modulated with 10% residual carrier; sound carrier −13 dB (transmitter side)



Intermodualtion ratio $a_{IM} = 20 \log \frac{V_{video\,(f=1\,MHz)}}{V_{video\,(f=f_{SC}-f_{CC})}}$

The 50% IRE signal with ±50% IRE color carrier corresponds to Cyan with 75% color saturation.

DIP 22

Video IF section

Controlled AM broadband amplifier with synchronous demodulator, video amplifier, and AGC voltage generation for the video IF amplifier and tuner.

Quasi-parallel sound section

Controlled AM broadband amplifier with quadrature demodulator, sound carrier output, internal AGC voltage generation, and an AFC section which can be disabled.

The TDA 5835 is especially suitable for application with black and white or color television receivers and/or VTR systems with PNP/MOS tuners for TV standards with negative video modulation and FM sound.

Circuit description

The video IF section is comprised of a 4-stage controllable AM amplifier, a limiter, and a mixer for the synchronous demodulation of video signals as well as an amplifier for the positive video output signal. The positive signal is used for gated control and a threshold amplifier to derive the delayed tuner AGC from the AGC voltage.

The quasi-parallel sound section also includes a 4-stage AM amplifier, a limiter, and a mixer for the quadrature demodulation of the 1st sound IF with subsequent sound carrier output for the 1st sound IF. The control voltage is generated by a peak value rectifier from the 2nd sound IF signal. The quasi-parallel sound also drives the AFC section.

Maximum ratings

		min	max	
Supply voltage	V_1		13	V
Max. dc voltage	$V_{2,3}$	V_8	V_1	V
Max. dc voltage	V_4	0	V_1	V
Max. dc voltage	$V_{5,6}$	V_8	V_1	V
Max. dc voltage	V_7	0	V_1	V
Max. dc current	I_8	−2	2	mA
Max. dc voltage	$V_{9,10}$	V_8	V_1	V
Max. dc current	$-I_{11}$	−1	3	mA
Max. dc voltage	V_{12}	−10	V_1	V
Max. dc voltage	$V_{13,14,15}$	0	V_1	V
Max. dc voltage	$V_{16,18}$	0	V_1	V
Max. dc voltage	$V_{19,20}$	0	V_1	V
Max. dc current	I_{21}	−1	2	mA
Junction temperature	T_j		150	°C
Storage temperature range	T_{stg}	−40	125	°C
Thermal resistance (system-air)	$R_{th\,SA}$		55	K/W

Operating range

Supply voltage	V_S	10.5	12.6	V
IF frequency	f_{IF}	15	75	MHZ
Ambient temperature	T_A	0	70	°C

Characteristics

$V_S = 12$ V; $T_A = 25$ °C

		Test conditions	min	typ	max	
Current consumption	I_1			102	134	mA
Stab. reference voltage	$V_{8/22}$			6.7	7.0	V
Video IF						
Control current for tuner	I_{14}			4.5		mA
Tuner AGC threshold	$V_{7/22}$		0		4.0	V
Gating pulse voltage	V_{12}	pos. gating pulse	4.0		V_1	V
	V_{12}	neg. gating pulse	−10		−4.0	V
Input voltage at G_{max}	$V_{i\,15/16}$	$V_{11\,pp} = 3$ V		30	60	µV
AGC range	ΔG			60		dB
IF control voltage	$V_{13/22}$	G_{max}	0			V
	$V_{13/22}$	G_{min}			4.0	V
Video output voltage	$V_{q\,11\,pp}$	$R_L = \infty$		3.0		V
Sync pulse level	$V_{11/22}$			2.0		V
DC voltage						
$V_{13} = 4$ V; $V_{15/16} = 0$ V	$V_{11/22}$			5.3		V
Output current	$I_{q\,11}$	to ground via R		−5.0		mA
	$I_{q\,11}$	to plus $V_{11} = 7$ V		+2.0		mA
AFC output current	$I_{q\,4}$	di/df < 0		±1		mA
AFC OFF	$V_{5/22}$	$V_5 = V_6$; $R = 10$ kΩ	0		4.0	V
ON	$V_{5/22}$	$V_5 = V_6$; $R = \infty$		6.0		V
Quasi-parallel sound						
Sound carrier output voltage	$V_{q\,21}$	$V_{i\,PC} = 1$ mV				
		$V_{i\,SC} = 300$ µV	10			mV
Input voltage at G_{max}	$V_{i\,18/19}$	$V_{21} = V_{21} - 3$ dB		50	100	µV
AGC range	ΔG	$V_{21} = V_{21} \pm 3$ dB		60		dB
Signal-to-noise-ratio		IEC 468				
White/staircase signal		peak weighting		61		dB
Black picture				66		dB
Test conditions						
Video carrier/sound carrier				10		dB
Modulation frequency				1		kHz
Frequency deviation				50		kHz
IF input voltage				20		mV

Characteristics

$V_S = 12$ V; $T_A = 25$ °C

		Test conditions	min	typ	max	
Design-related characteristics						
Input impedance	$Z_{i\,15/16}$			1.8/2		kΩ/pF
	$Z_{i\,18/19}$			1.8/2		kΩ/pF
Output impedance	$Z_{q\,2/3}$			6.6/2		kΩ/pF
	$Z_{q\,9/10}$			6.6/2		kΩ/pF
	$Z_{q\,5/6}$			20		kΩ
Output resistance	$R_{q\,11}$			150		Ω
Residual IF (fundamental wave)	V_{11}			10		mV
Video bandwidth (−3 dB)	B_{video}			6.0		MHz
Intermodulation ratio with reference to f_{cc}	α_{IM}	sound color interference		50		dB
Output resistance	$R_{q\,21}$			200		Ω
IF control voltage	$V_{20/22}$	G_{max}	0			V
	$V_{20/22}$	G_{min}			4	V

Alignment procedures

a) Video IF

At a video carrier input level of $V_{15/16\ rms} = 10$ mV and a superimposed AGC voltage of $V_{13} = 3$ V, the demodulator tank circuit is preliminarily aligned so that the demodulated video signal $V_{11\,pp}$ reaches its maximum output level at the positive video output. Any suitable video test signal can be used for modulation. Subsequently, the AGC voltage V_{13} is reduced until the video signal equals approx. 3 V (peak-to-peak). By fine-aligning the demodulator tank circuit, the maximum output level of the video signal is reached.

The flat response characteristic of the demodulator ensures a non-critical alignment procedure.

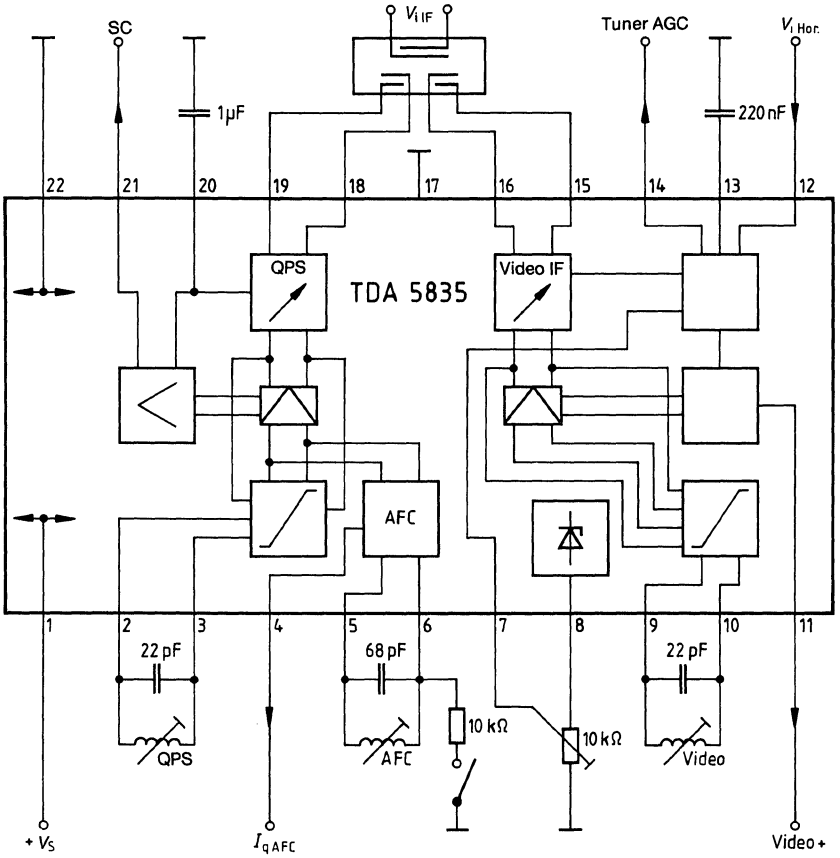
b) QPS

At an input signal of $V_{18/19\ rms} = 10$ mV the demodulator tank circuit is preliminarily aligned until a max. AM suppression of the demodulated video signal V_{21} is reached at the sound carrier output. A video signal critical for the sound-interference ratio should be used for modulation (white/staircase, FuBK). Subsequent fine-aligning is performed by measuring the sound-interference ratio at the output of a FM demodulator and fine-aligning the demodulator tank circuit for a max. interference ratio. If several sound carriers are used in a device, the sound carrier with the lowest level should be used for alignment purposes.

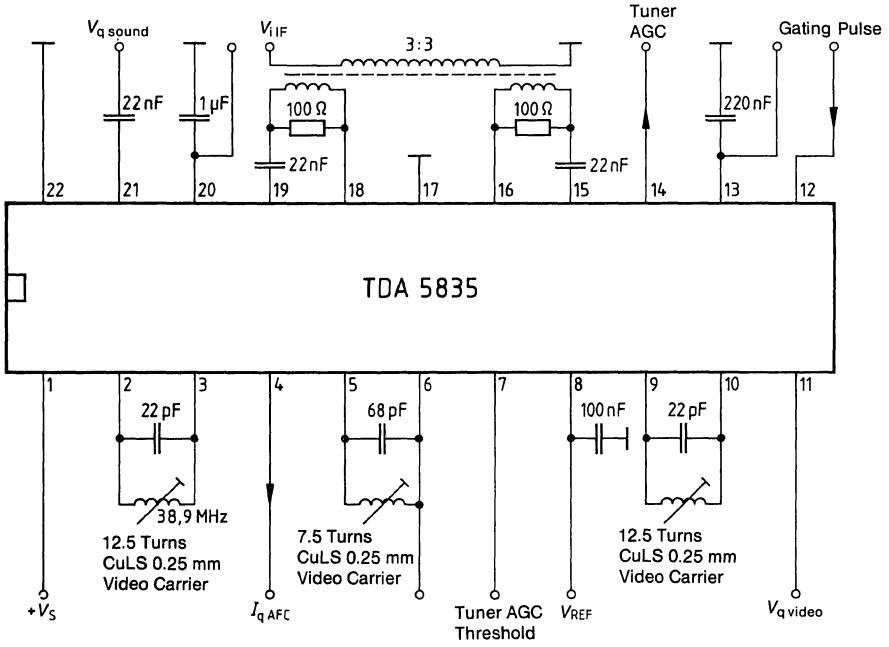
Pin description

Pin	Function
1	Supply voltage
2	Demodulator tank circuit QPS
3	Demodulator tank circuit QPS
4	Push-pull current output AFC
5	Demodulator tank circuit AFC
6	Demodulator tank circuit AFC and switch-off
7	Tuner AGC threshold
8	Reference voltage
9	Demodulator tank circuit video IF
10	Demodulator tank circuit video IF
11	Video output
12	Gating pulse input
13	AGC time constant video IF
14	Delayed tuner AGC
15	Video IF input
16	Video IF input
17	GND
18	QPS IF input
19	QPS IF input
20	AGC time constant QPS
21	Sound carrier output
22	GND

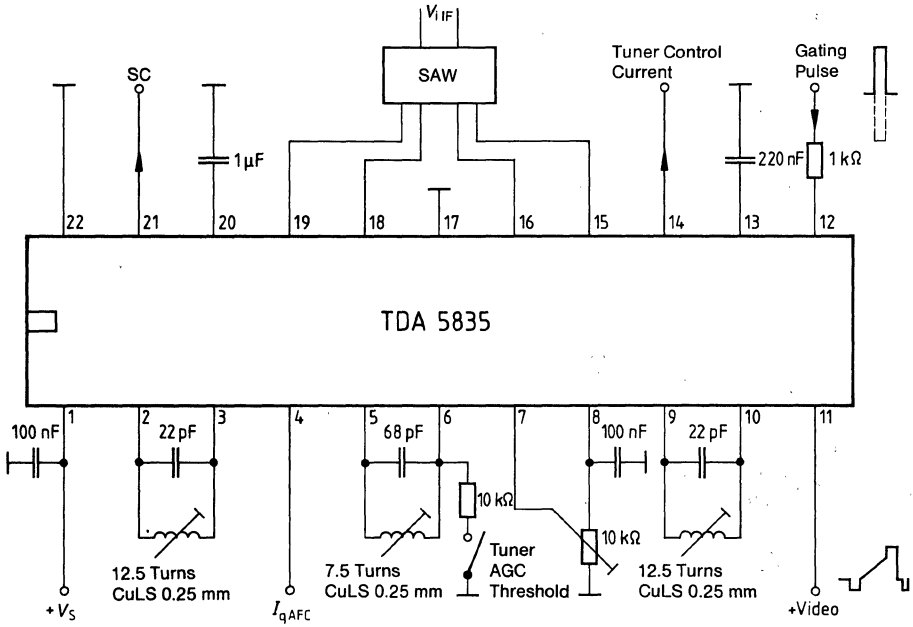
Block diagram



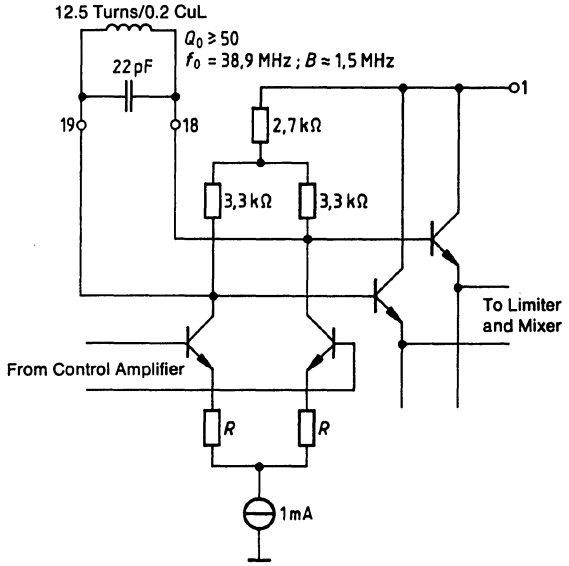
Measurement circuit



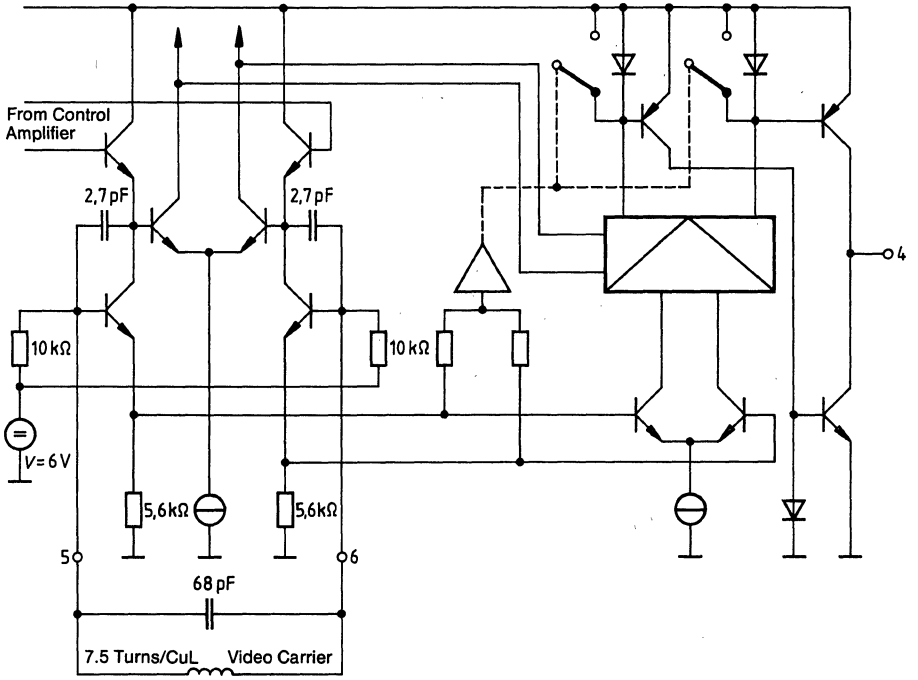
Application circuit



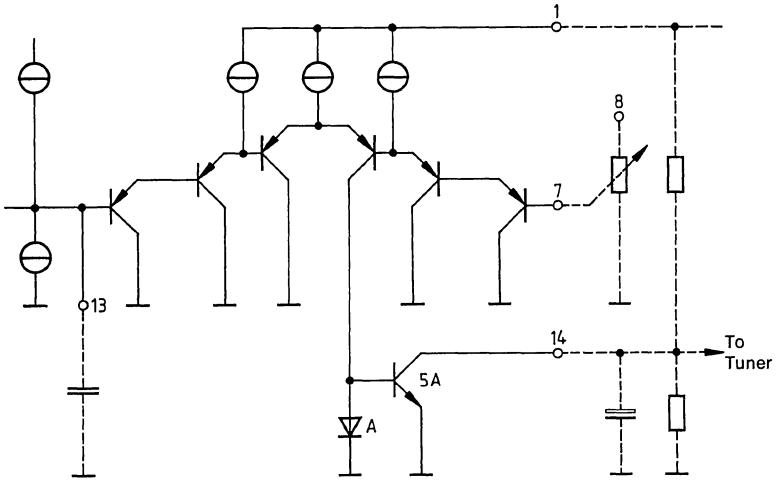
Demodulator tank circuit QPS



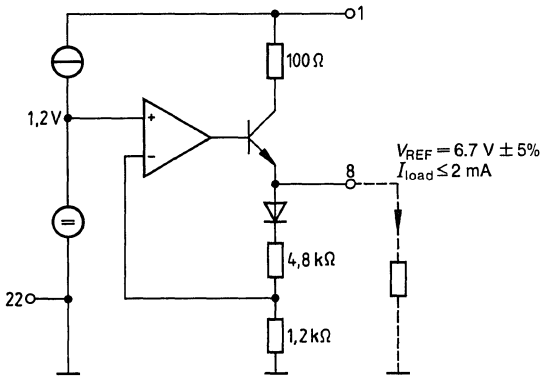
Demodulator tank circuit AFC



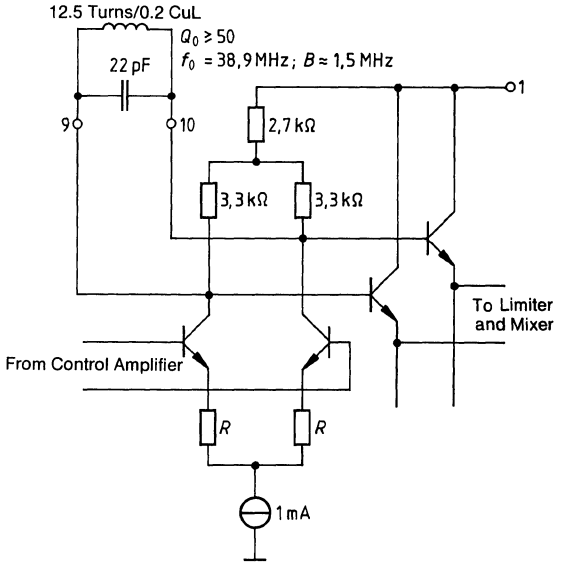
Tuner AGC threshold and output



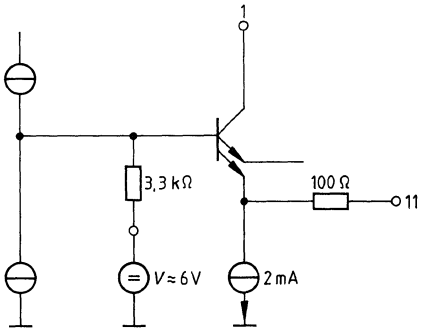
Reference voltage



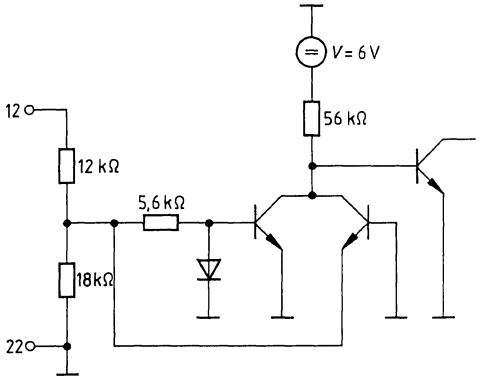
Demodulator tank circuit video IF



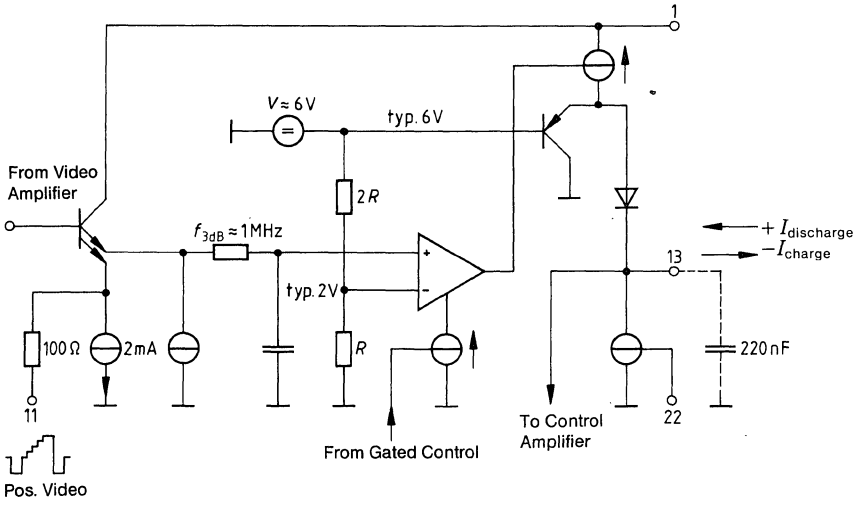
Positive video output



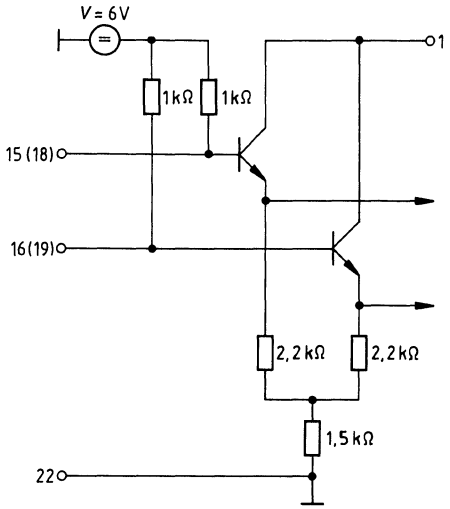
Gating pulse input



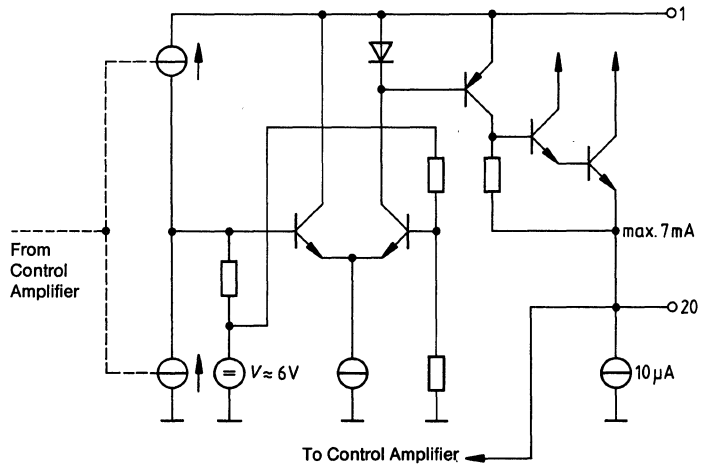
AGC time constant video IF



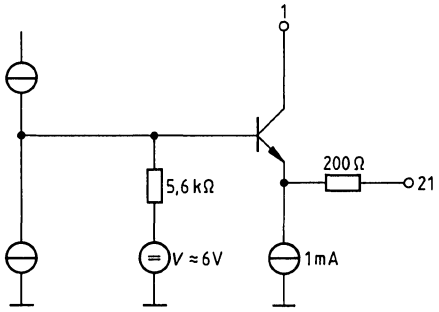
IF input video IF
IF input QPS



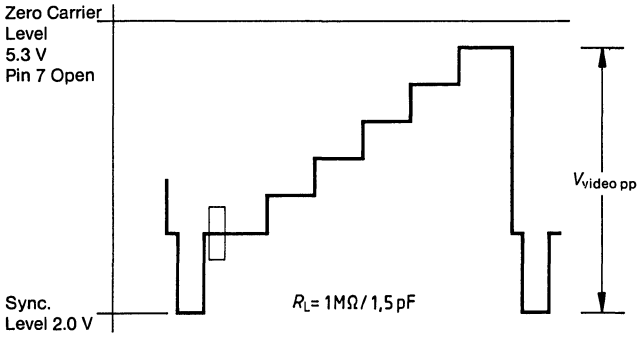
AGC time constant QPS



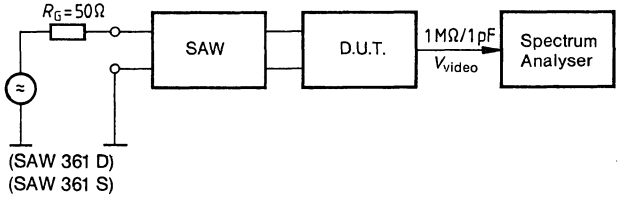
Sound carrier output QPS



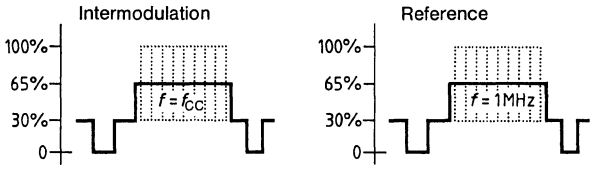
Pos. video output



Measurement configuration



Test signal: $f_{VC} = 38.9$ MHz with test signal modulated with 10% residual carrier; sound carrier −13 dB (transmitter side)



Intermodulation ratio: $a_{IM} = 20 \log \frac{V_{video\,(f=1\,MHz)}}{V_{video\,(f=f_{SC}-f_{CC})}}$

The 50% IRE signal with ±50% IRE color carrier corresponds to Cyan with 75% color saturation.

DIP 8

The TDA 5850 is a switchable video amplifier with connections for the French and IEC VCR standards.

Features

- Standard connection for VCR (CCIR) and Peri TV sets
- Input clamping
- Positive and negative video outputs

Maximum ratings

Supply voltage	V_S	16.5	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	70	K/W

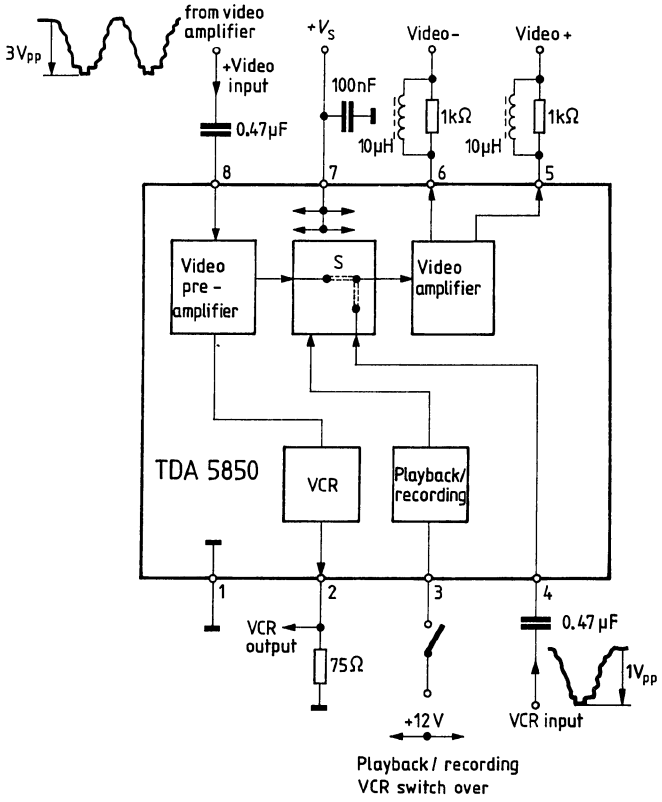
Operating range

Supply voltage range	V_S	10 to 15.8	V
Video bandwidth	B_{video}	6	MHz
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics ($V_S = 13$ V; $T_{amb} = 25$ °C)

		min	typ	max	
Current consumption (pin 2 open)	I_7		23.0		mA
Switch input VCR recording	$V_{3/1}$	0		1.2	Vdc
Switch input VCR playback	$V_{3/1}$	3.0		V_7	Vdc
Switch input $V_{3/1} = 15$ V	I_3			1.0	mA
Video output voltage pos. ($V_3 = 1.2$ V; $V_{8\,pp} = 3$ V)	$V_{5\,pp}$		3.0		V
Video output voltage pos. ($V_3 \geqq 3$ V; $V_4 = 1$ V_{pp})	$V_{5\,pp}$		3.0		V
Sync pulse level	$V_{5/1}$		2.0		Vdc
Output current (to ground)	I_5		−5.0		mA
Output current (to +)	I_5		2.0		mA
Output resistance	R_5		150		Ω
Video output voltage neg. ($V_3 = 1.2$ V; $V_8 = 3$ V_{pp})	$V_{6\,pp}$		3.0		V
Video output voltage neg. ($V_3 \geqq 3$ V; $V_4 = 1$ V_{pp})	$V_{6\,pp}$		3.0		V
Sync pulse level	$V_{6/1}$		$V_7 - 2$		Vdc
Output current (to ground)	I_6		−5.0		mA
Output current (to +)	I_6		1.0		mA
Output resistance	R_6		150		Ω
Video output voltage pos. ($V_{8\,pp} = 3$ V; $R_{2/1} = 75$ Ω)	$V_{2\,pp}$		1.0		V
Sync pulse level ($R_{2/1} = 75$ Ω)	$V_{2/1}$		1.0		Vdc
Output current (to ground)	I_2		−30.0		mA
Output current (to +)	I_2		2.0		mA
Output resistance	R_2		75		Ω
Video input current ($V_{8\,pp} = 3$ V)	I_8			40	µA
Video input current ($V_{4\,pp} = 1$ V)	I_4			20	µA
Video gain ($V_{8\,pp} = 3$ V; $R_{2/1} = 75$ Ω)	$G_{2/8}$		1/3		
Video gain ($V_{8\,pp} = 3$ V; $V_3 = 1.2$ V)	$G_{5/8}$		1		
Video gain ($V_{8\,pp} = 3$ V; $V_3 = 1.2$ V)	$G_{6/8}$		−1		
Video gain ($V_{4\,pp} = 1$ V; $V_3 \geqq 3$ V)	$G_{5/4}$		3		
Video gain ($V_{4\,pp} = 1$ V; $V_3 \geqq 3$ V)	$G_{6/4}$		−3		
Video bandwidth (−3 dB)	B_{video}	6.0			MHz
Cross talk rejection referred to $V_{5\,pp} = 3$ V ($f = 50$ Hz . . 6.0 MHz; $V_3 = 1.2$ V; $V_{4\,pp} = 1$ V)	a		50		dB

Block diagram, test circuit and application circuit



Preliminary data **Bipolar circuit**

The controlled AM broadband amplifier includes a PLL synchronous demodulator, a video amplifier as well as a control voltage generation for the IF amplifier and tuner.

TDA 6000: for PNP tuner

Features

- True synchronous demodulation
- Large control range
- High input sensitivity
- Very low luma-chroma crosstalk
- Positive and negative video signal
- Extremely low differential phase and gain errors
- Reduced phase errors for chroma processing

Maximum ratings

Supply voltage	V_S	16.5	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	70	K/W

Operating range

Supply voltage range	V_S	10.5 to 15.8	V
IF frequency	f_{IF}	60	MHz
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics ($V_S = 13$ V; $T_{amb} = 25$ °C)

		min	typ	max	
Current consumption	I_{11}		70		mA
Stab. reference voltage	V_{12}		6.0		Vdc
Control current for tuner ($V_{14} = 0.5\ V_{11}$)	I_{14}		4.0		mA
Tuner AGC threshold	$V_{13/1}$	0		4.0	Vdc
Gating pulse voltage					
pos. gating pulse	V_1		+3.0		V
neg. gating pulse	V_1		−3.0		V
Input voltage at G_{max} ($V_{3\,pp} = 3$ V)	$V_{i15/16}$			100	μV
AGC range	V		60		dB
Video output voltage (pos.) ($R_L = \infty$)	$V_{q3\,pp}$		3.0		V
Sync pulse level	V_{q3}		2.0		Vdc
DC voltage ($V_2 = 4$ V; $V_{15/16} = 0$)	$V_{3/1}$		5.3		Vdc
Output current					
to ground across R	I_{q3}		−5.0		mA
to plus $V_3 = 7$ V	I_{q3}		+2.0		mA
Video output voltage (neg.) ($R_L = \infty$)	$V_{q4\,pp}$		3.0		V
Sync pulse level	$V_{4/10}$		V_{11}−2.0		Vdc
DC voltage ($V_2 = 4$ V; $V_{15/16} = 0$ V)	$V_{4/10}$		V_{11}−5.3		Vdc
Output current					
to ground across R	I_{q4}		−5.0		mA
to plus $V_4 = V_{11}$	I_{q4}		+1.0		mA
IF control voltage G_{max}	$V_{2/10}$	0			Vdc
G_{min}	$V_{2/10}$			4.0	Vdc
Additional application data					
Input impedance	$Z_{i15/16}$		1.8/2		kΩ/pF
Output impedance	$Z_{q8/9}$		6.6/2		kΩ/pF
Output resistance	R_{q3}		150		Ω
Output resistance	R_{q4}		150		Ω
Residual IF (basic frequency)	$V_3; V_4$		10		mV
Video bandwidth (−3 dB)	B_{video}		6.0		MHz
Intermodulation ratio with reference to f_{FT} (1.07 MHz)	a		45		dB

DIP 16

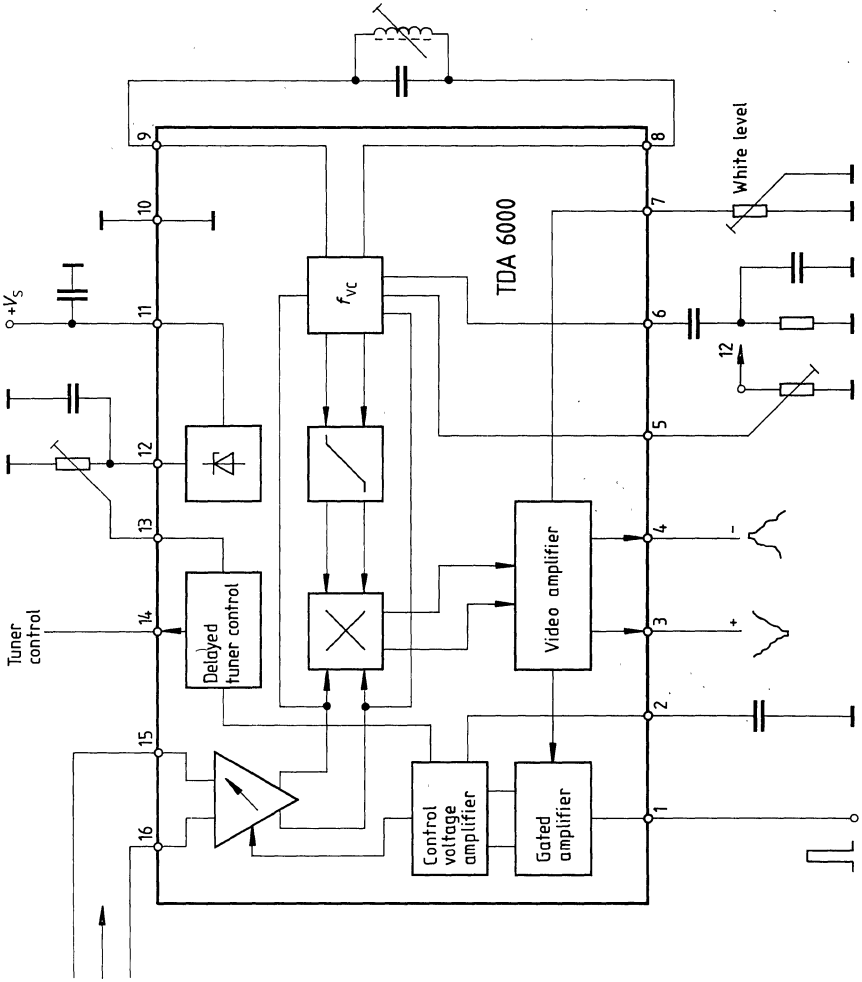
Circuit description

This integrated circuit consists of a 4-stage controlled gain AM amplifier and a PLL circuit for video carrier regeneration. The synchronous demodulator features very low intermodulation distortion between video IF and color carrier (1.1 MHz or 920 kHz beat). Also included are a mixer for the synchronous demodulation of the video signals and an amplifier for the positive and negative video output signal. The positive signal is used for gate control of the AGC amplifier. The delayed tuner AGC is derived from the control voltage via a threshold amplifier.

Pin configuration

Pin No.	Function
1	Gating pulse
2	Time constant AGC
3	Positive video output
4	Negative video output
5	Offset adjustment
6	PLL time constant
7	White level adjustment
8	Tank circuit
9	Tank circuit
10	Ground
11	Supply voltage
12	Reference voltage
13	AGC threshold
14	Tuner control
15	Video IF input
16	Video IF input

Block diagram



TV Stereo Tone Control IC with Quasi-Stereo Section, Channel 1/2 Switch, SCART Input, and I²C Bus Control

TDA 6200

Preliminary data

DIP 28

The TDA 6200 is comprised of a SCART switch-over, channel 1/2 switch-over, quasi-stereo circuit, stereo basewidth expansion, physiological volume control, a treble, bass, and volume control of the injected AF signals as well as an LED driver. The IC is controlled by means of an I²C bus serial interface as well as by the bidirectional 4 level line from the TDA 6600. The component is used for AF sound signal processing in stereo TV sets.

Features

- Treble, bass, balance, and volume control by means of an integrated digital-to-analog converter
- Quasi-stereo circuit during mono operation
- Stereo basewidth expansion during stereo operation
- Physiological volume control
- Channel 1/2 switch-over during dual audio transmission
- SCART connection
- Control of all functions via the I²C bus and the bidirectional 4 level line of the TDA 6600 (stereo demodulator IC)
- LED driver
- Volume control range 80 dB
- Treble, bass control ±12 dB
- Channel separation min. 60 dB, cross-talk rejection min. 60 dB
- Parasitic voltage spacing up to 78 dB

Circuit description

The monolithically integrated circuit is comprised of three sections:

1. AF input analog switch for SCART and channel 1/2 switch-over
2. Sound and volume control with quasi-stereo, physiology and stereo basewidth expansion section
3. Control section including the I²C bus, 4 level line and digital-to-analog converter

1. A two-channel AF analog switch is used to switch from standard TV operation to the SCART playback mode. An additional analog switch is applied for the channel 1/2 switch-over during multichannel transmission. During standard TV operations, this switch will be functional during two-channel transmission and/or SCART playback if the Kbit has been set accordingly.
2. The quasi-stereo section in the signal path is applied to generate an acoustic sound impression similar to stereo during the mono signal. This circuitry section is comprised of one op amplifier per channel. While one amplifier is provided with an internally regulated gain factor of −1, the second amplifier can be switched between a gain factor of −1 and a freely selectable gain factor provided by means of external components. The quasi-stereo effect is achieved by forwarding two different types of signals to the input of the second amplifier. While a standard phase AF signal is forwarded via an external band stop filter, a phase inverted signal is forwarded via an external band filter. The attenuation of these networks is compensated by the op amplifier. The result is the generation of a largely amplitude-linear signal, however, turned by 180° in its phase during medium frequencies. This section of the circuit can be switched off.

   The sound and volume control section is comprised per stereo channel of 3 op amplifiers with electronic potentiometers and/or switches. By using one external capacitor each for the bass and treble control, 31 different levels for emphasis and deemphasis can be set for the bass and treble control during low and/or high frequencies. The subsequent stage enables a switch-controlled expansion of the basewidth. When the basewidth expansion has been switched on, an anti-phase cross-talk of approx. 60% will occur at an input frequency of approx. 300 Hz. The frequency to be applied as well as the percentage of cross-talk are determined by an external RC combination. The volume control, separate for each channel, is comprised of 64 stages each. As a result, the balance control can be realized by using different settings for the channels.

   A physiological volume characteristic is achieved by connecting the volume setting with the treble/bass control. For this purpose, the mean value of the two volume control settings is used. The physiology section can be switched off.

   Subsequent to the connection of the supply voltage, the AF output voltage will be delayed by a delay circuit until all voltages are stabilized. In this manner, interfering crackling noises are prevented.

3. The integrated circuit is controlled by means of an I²C bus interface and a 4 level line from the stereo decoder TDA 6600. Via this line the evaluation circuit of the TDA 6600 provides the necessary information with respect to the 3 modes mono, dual audio, and stereo by means of three different dc voltage levels. For a compulsory (manual) mono mode, a fourth dc voltage level in opposite direction can be used by the TDA 6600. This dc voltage level is programmed via the I²C bus interface of the TDA 6200. The system clock for the input SCL of the I²C bus interface is provided by the processor. Pin SDA functions as data input. It can also supply the setting of the identification signal decoder established via the 4 level output and/or an acknowledge message.

   The data forwarded by the processor are controlled by the I²C bus and subsequently filed in registers according to their functions (latch 1-6).

   If the bus is free (t off time), both lines will be in the marking state (SDA, SCL are HIGH). Each message begins with the start conditions of SDA returning into LOW, while SCL remains HIGH. All additional information transfer takes place during SCL = LOW, and the data is forwarded to the control with the positive clock edge. However, if SDA returns to HIGH, while SCL is in HIGH, the message is ended since the circuit acknowledges a stop condition.

   The logic functions according to the tables on pages 725-727. All messages are transmitted byte-by-byte, followed by a 9th clock pulse, while the control returns the SDA line to LOW (acknowledge condition). In the read mode, the processor transmits the acknowledge bit (will not be checked by the tone control). The first byte is comprised of 7 address bits used by the processor to select the tone control among several peripheral components (chip select). The 8. bit establishes the direction of the subsequent data flow (read/write bit). The 1. and 2. bit of the data bytes determine which latch will be called up (sub-address).

   The volume information is set with 6 bits (64 positions); the treble and bass control with 5 bits of which the 1. bit (4. bit of the byte) is the sign bit. The 4 bits of the digital-to-analog converter provide 31 different setting levels. The two volume bytes (left, right) and/or treble and bass bytes have to be transmitted in successive order, since they have the same sub-address. The two bytes for the switching function are subdivided into an AF setting byte and a byte for the operation of the SCART jack.

   If the R/W bit = 1 is set during chip addressing, the I²C bus operates in the transmission mode. The momentary position of the stereo decoder (corresponds with the status of the 4 level line) is transmitted.

   The two LED driver outputs enable the display of stereo, mono or dual audio transmission and/or the SCART playback mode.

Maximum ratings

		min	max	
Supply voltage	V_S	0	16	V
Reference current	I_{26}	0	2	mA
DC voltage	$V_{1,2,3}$	0	V_S	V
DC voltage	$V_{6,8,9}$	0	V_S	V
DC voltage	$V_{10,14,18}$	0	V_S	V
DC voltage	$V_{19,20,22}$	0	V_S	V
DC voltage	$V_{23,24,25}$	0	V_S	V
DC voltage	$V_{27,28}$	0	V_S	V
DC current	$I_{4,5,7}$	0	2	mA
DC current	$I_{11,13,15}$	0	2	mA
DC current	$I_{17,21}$	0	2	mA
Junction temperature	T_j		150	°C
Storage temperature range	T_{stg}	−40	125	°C
Thermal resistance (system-air)	$R_{th\,SA}$		60	K/W

Operating range

Supply voltage	V_S	8	15.75	V
Ambient temperature	T_A	0	70	°C
Input frequency	f_i	0	20	kHz

Characteristics

$V_S = 15$ V; $T_A = 25$ °C

		Test conditions	min	typ	max	
Current consumption	I_{16}	LEDs OFF		55	80	mA
Reference voltage	V_{26}		5.4	6	6.6	V
Max. gain						
AF input/AF output L byte = BF; KL[2] byte = C0	G_{max}	SC = 0; phys = 0; RK[1] = 0; Q-S/Bw = 0	−2	0	2	dB
SCART input/ AF output L byte = BF; KL byte = C0	G_{max}	SC = 1; phys = 0; RK = 0; Q-S/Bw = 0	−2	0	2	dB
Min. gain						
AF input/AF output L byte = 80; KL byte = C0	G_{min}	SC = 0; phys = 0; RK = 0; Q-S/Bw = 0			−80	dB
SCART input/ AF output L byte = 80; KL byte = C0	G_{min}	SC = 1; phys = 0; RK = 0; Q-S/Bw = 0			−80	dB
Flutter and wow L-R	Δa_{L-R}				−2	dB
Bass emphasis*) KL byte = C0 + DF	$G_{B\,max}$	$f_i = 40$ Hz	9	12		dB
Bass deemphasis KL byte = C0 + CF	$G_{B\,min}$	$f_i = 40$ Hz		−12	−10	dB
Treble emphasis*) KL byte = DF + C0	$G_{T\,max}$	$f_i = 15$ Hz	8.5	12		dB
Treble deemphasis KL byte = CF + C0	$G_{T\,min}$	$f_i = 15$ Hz		−12	−10	dB
Input voltage*) SCART, AF	$V_{i\,rms}$	any KL byte	1			V
Input voltage*) SCART, AF	$V_{i\,rms}$	KL byte = CX	3.5			V
Permissible gain quasi-stereo op	$G_{7/6}$	Q-S/Bw = 1			30	dB
Channel separation	a_{L-R}	Q-S/Bw = 0; RK = 0	60			dB
Antiphased cross talk with basewidth ON	CT_{L-R}	stereo; RK = 1	45	60	75	%

[1]) RK ≙ room acoustics
[2]) KL ≙ tone

Characteristics

$V_S = 15$ V; $T_A = 25$ °C

		Test conditions	min	typ	max	
Cross-talk rejection						
SCART switch	$a_{AF/SF}$	$V_{i\,rms} = 2$ V	60			dB
Ch1/Ch2 switch	$a_{CH1/2}$	$V_{i\,rms} = 2$ V; dual audio	60			dB
Total harmonic distortion	$THD_{13/15}$	any KL[1] byte $V_{i\,rms} = 1$ V			1	%
Total harmonic distortion DIN 45500*)	$THD_{13/15}$	KL byte = CX; $V_{i\,rms} = 1$ V		0.3	0.6	%
Disturbance voltage spacing $f_i = 20$ Hz-20 kHz	$a_{S/N}$	DIN 45405; $V_{i\,rms} = 1$ V L byte = BF; KL byte = C0			78	dB
Disturbance voltage at output $f = 20$ Hz-20 kHz	$a_{S/N}$	L byte = BF; KL byte = C0		120	150	µV
		L byte = AC; KL byte = C0			50	µV
		L byte = 94; KL byte = C0		10	20	µV
Noise voltage CCIR DIN 45405	V_n	L byte = BF KL byte = DF + C0			650	µV
Deviation in amplitude when tone control is in linear position	ΔG	KL byte = C0 $f_i = 40$ Hz-15 kHz		±0.5	±1.5	dB
Volume decontrol for max. phys.	V_q/V_i	phys = 1		−30		dB
Attenuation during mute mode	a_{MUTE}	M1 = 1	80			dB
Switching output	$V_{4\,on}$	$I_L = 1$ mA			0.5	V
	$I_{4\,off}$				1	µA
LED driver	$I_{22,23}$	LED ON			7.5	mA
	$V_{22,23}$	$I_{22/23} = 7.5$ mA			1.5	V
	$I_{22,23}$	LED OFF			50	µA
4 level line						
Input voltage	$V_{i\,2}$	recognizes mono	0		1.8	V
	$V_{i\,2}$	recognizes dual	2.4		3.9	V
	$V_{i\,2}$	recognizes stereo	5.2		6.6	V
Input current	$V_{i\,2}$				3	µA
Compulsory mono	$V_{q\,2}$	M2 = 1; $I_2 = 1$ mA			0.2	V

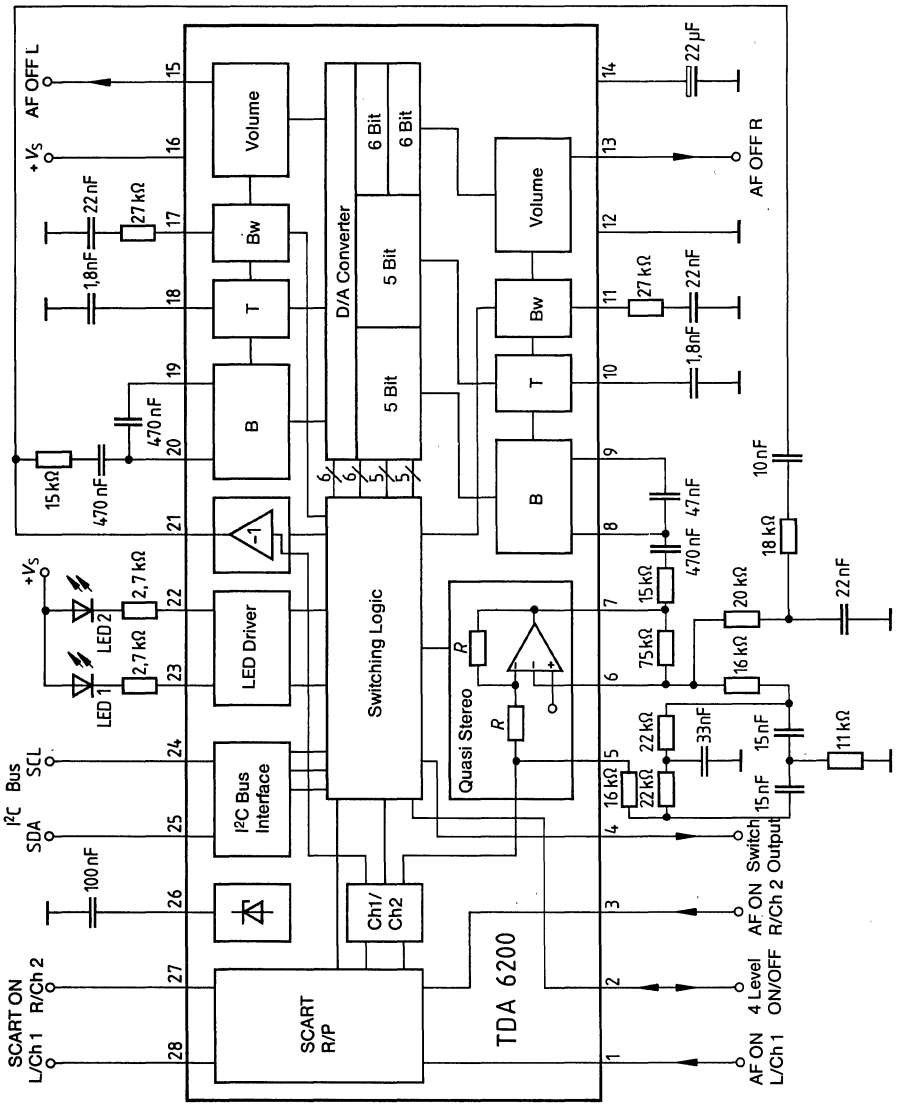
Characteristics

$V_S = 15$ V; $T_A = 25$ °C

		min	typ	max	
I²C bus (SCL, SDA)					
SCL, SDA edges					
Rise time	t_R			1	µs
Fall time	t_F			0.3	µs
Shift register clock pulse SCL					
Frequency	f_{SCL}	0		100	kHz
H pulse width	t_{HIGH}	4			µs
L pulse width	t_{LOW}	4			µs
Start					
Set-up time	t_{SUSTA}	4			µs
Hold time	t_{HDDAT}	4			µs
Stop					
Set-up time	t_{SUSTO}	4			µs
Bus free time	t_{BUF}	4			µs
Data transfer					
Set-up time	t_{SUDAT}	1			µs
Hold time	t_{HDDAT}	1			µs
Inputs SCL, SDA					
Input voltage	V_{iH}	2.4		5.5	V
	V_{iL}	0.3		1	V
Input current	I_{iH}			50	µA
	I_{iL}			100	µA
Output SDA (open collector)					
Output voltage	V_{qH}	4.5		5.5	V
$R_L = 2.5$ kΩ; $I_{qL} = 2$ mA	V_{qL}			0.4	V
Design-related characteristics					
Input impedance SCART	$R_{i\,27,28}$	35			kΩ
Input impedance AF	$R_{i\,1,3}$	35			kΩ
Output impedance	$R_{q\,5,7,21}$			200	Ω
Output impedance AF output	$R_{q\,13,15}$			200	Ω
Internal resistance Bw	$R_{i\,11,17}$			1	kΩ

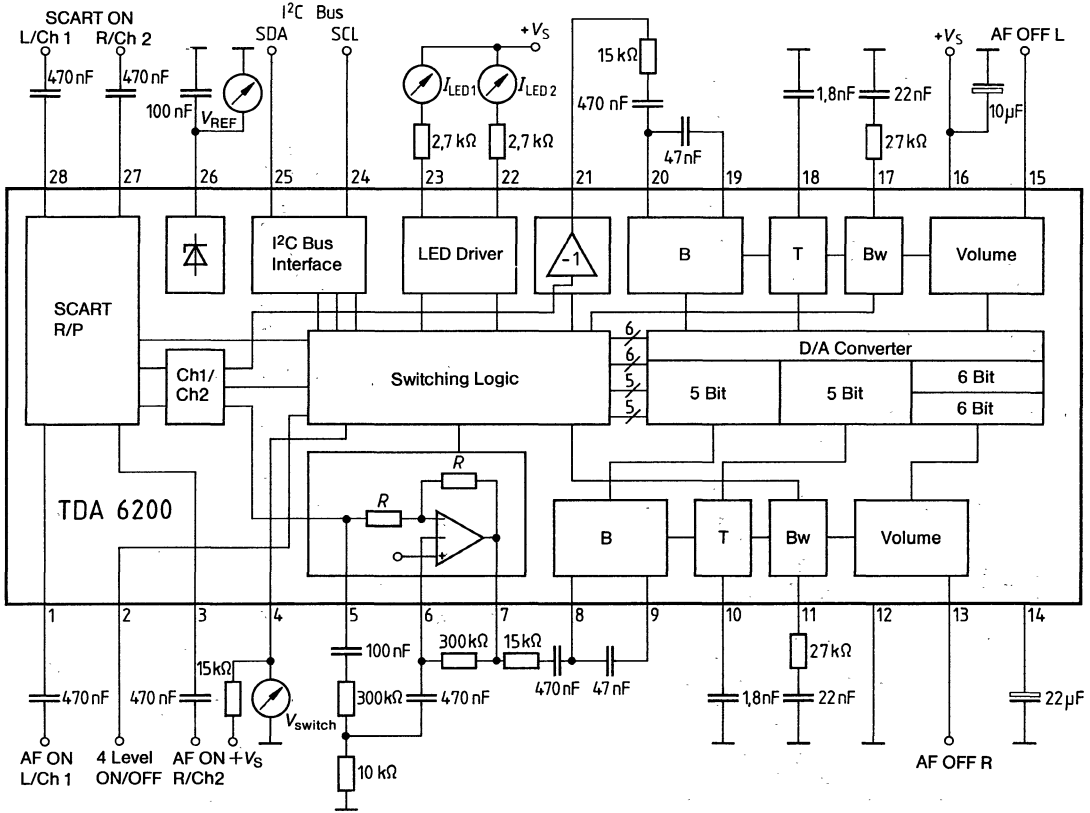
The data marked with an asterisk*) depend on the supply voltage.
With lower V_S the input voltage decreases accordingly.

Block diagram

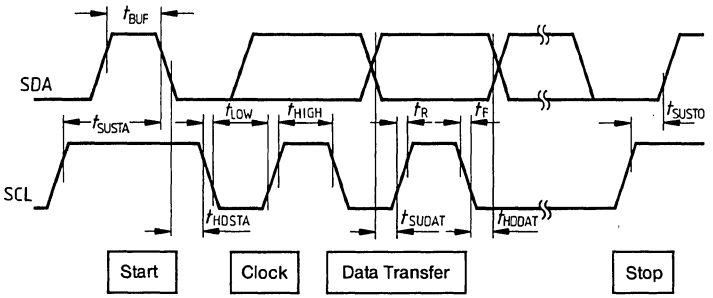


Pin description

Pin	Function
1	AF input for signal from matrix section of TDA 6600
2	Bidirectional 4 level control line between TDA 6200 and TDA 6600 used to transmit information with respect to dual audio, mono, stereo and compulsory mono mode
3	AF input for signal from matrix section of TDA 6600
4	Switching output to control additional functions (open collector), in turn controlled via I^2C bus
5	Low-impedance output to control the quasi-stereo network
6	Inverted input of the quasi-stereo op
7	Low-impedance output of quasi-stereo op, controls bass control
8, 9	Connections for external capacitor for right bass control $f_{-3\,dB} \sim 1/C_{8,9}$
10	Connection for external capacitor for right treble control $f_{-3\,dB} \sim 1/C_{10}$
11	Connection for network of stereo basewidth expansion percentage of cross-talk $\sim 1/R_{11}$ $$f_{-3\,dB} = \frac{1}{2\pi C_{11}\,(R_{11} + 1\,k\Omega)}$$
12	GND
13	AF output right (emitter follower)
14	Decoupling for internal dc operation points. Capacitor also determines the duration of the switch-on delay when connecting V_{16}.
15	AF output left (emitter follower)
16	Supply voltage
17	Connection for network of stereo basewidth expansion percentage of cross-talk $\sim 1/R_{17}$ $$f_{-3\,dB} = \frac{1}{2\pi C_{17}(R_{17} + 1\,k\Omega)}$$
18	Connection for external capacitor of left treble control $f_{-3\,dB} \sim 1/C_{18}$
19, 20	Connections for external capacitor of left bass control $f_{-3\,dB} \sim 1/C_{19,20}$
21	Low-impedance output to control the quasi-stereo network and the left bass control
22	LED driver output for LED 2 (open collector with current limiter)
23	LED driver output for LED 1 (open collector with current limiter)
24	Clock frequency input of I^2C bus control (Inter-IC)
25	Data input/output of I^2C bus control
26	Reference voltage of typ. 6 V
27	AF input of SCART interface
28	AF input of SCART interface


SCART ON
L/Ch 1
R/Ch 2
I²C Bus
SDA
SCL
+VS
AF OFF L
470 nF
470 nF
100 nF
VREF
ILED1
ILED2
2,7 kΩ
2,7 kΩ
15 kΩ
470 nF
47nF
1,8nF
22nF
27 kΩ
10µF
28
27
26
25
24
23
22
21
20
19
18
17
16
15
SCART R/P
I²C Bus Interface
LED Driver
-1
B
T
Bw
Volume
Ch1/ Ch2
Switching Logic
6
6
5
5
D/A Converter
5 Bit
5 Bit
6 Bit
6 Bit
R
R
TDA 6200
B
T
Bw
Volume
1
2
3
4
5
6
7
8
9
10
11
12
13
14
470 nF
470 nF
15kΩ
Vswitch
100 nF
300kΩ
300kΩ
470 nF
15kΩ
470 nF
47 nF
10 kΩ
27kΩ
1,8nF
22nF
22µF
AF ON L/Ch 1
4 Level ON/OFF
AF ON R/Ch2
+VS
AF OFF R

I²C bus time diagram



t_{SUSTA}	Set-up time (start)
t_{HDSTA}	Hold time (start)
t_{HIGH}	Pulse width (clock)
t_{LOW}	Pulse width (clock)
t_{SUDAT}	Set-up time (data transfer)
t_{HDDAT}	Hold time (data transfer)
t_{SUSTO}	Set-up time (stop)
t_{BUF}	Bus free time
t_F	Fall time
t_R	Rise time

The listed times are referenced to the V_{IH} and V_{IL} values.

Software

The following data format is used:

1) **Chip address**

MSB							LSB	
1	0	0	0	0	0	0	R/W	ack.

MSB will be transmitted first
R/W = 0 IC in the receiving mode

2) **Data bytes with sub-addresses**

a) Volume

MSB							LSB	
1	0	V05	V04	V03	V02	V01	V00	(left) +
1	0	V15	V14	V13	V12	V11	V10	(right)

The two bytes are always transmitted in successive order
V x 5 = MSB
V x 0 = LSB

1	0	0	0	0	0	0	0	min. volume
1	0	1	1	1	1	1	1	max. volume

b) Tone

MSB							LSB	
1	1	X	HV	H3	H2	H1	H0	+
1	1	X	TV	T3	T2	T1	T0	

The two bytes are always transmitted in successive order
HV or TV are sign bits
H3 or T3 = MSB
H0 or T0 = LSB

1	1	X	0	1	1	1	1	min. treble or bass
1	1	X	X	0	0	0	0	linear treble or bass
1	1	X	1	1	1	1	1	max. treble or bass

Software

c) AF set byte

MSB							LSB
0	0	M1	M2	Ch1/2	RK	Phys	Q-S/Bw

M1 = 1 Muting for AF output
M1 = 0 AF ON
M2 = 1 Compulsory mono (via 4 level line)
M2 = 0 Standard operation for identification signal decoder
Ch1/2 = 0 During dual audio mode, channel 1 at AF output
Ch1/2 = 1 During dual audio mode, channel 2 at AF output
(only active with dual audio via 4 level line or during SCART playback and Kbit = 1)
RK = 1 Room acoustics ON;
TV operating mode: Quasi-stereo during mono and dual audio or stereo basewidth expansion during stereo transmission — automatic switch-over via 4 level line
SCART playback mode: stereo basewidth expansion ON
RK = 0 Stereo basewidth expansion and quasi-stereo OFF
Phys = 1 Physiological volume control ON
Phys = 0 Physiological volume control OFF
Q-S/Bw = 1 TV operating mode: Quasi-stereo and stereo basewidth expansion ON
SCART playback mode: stereo basewidth expansion ON
Q-S/Bw = 0 Quasi-stereo and stereo basewidth expansion OFF

d) SCART set byte

MSB							LSB
0	1	SC	Sch	Ch	X	X	X

SC = 1 SCART playback mode; SCART input connected with AF output
SC = 0 Standard operation
Sch = 1 Switching output ON (open collector)
Sch = 0 Switching output OFF (output can e.g. be used for switch-over from recording to playback mode in the video section)
Ch = 1 Playback of SCART dual transmission; channel selection via Ch1/2 bit for AF output
Ch = 0 AF output operates in stereo mode. Playback of SCART stereo (mono) transmission.

Note:

The AF section is automatically controlled by the 4 level line. Compulsory mono M2 is given priority. After Power-ON-Reset all latches are set at 0 (volume min., tone linear,...); only the function Q-S/Bw is set at 1.

Software

3) **Transmission mode**

requires new chip addressing with R/W bit = 1.

MSB							LSB
St	D	X	X	X	X	X	X

St	D	
1	1	Decoder recognizes mono
0	1	Decoder recognizes stereo
1	0	Decoder recognizes dual
0	0	Does not occur (internally suppressed)

The transmission function is not required for the operation of the IC. Instead this function is used to inform the µC about the status of the identification signal decoder to enable additional functions.

LED driver

TV operating mode:

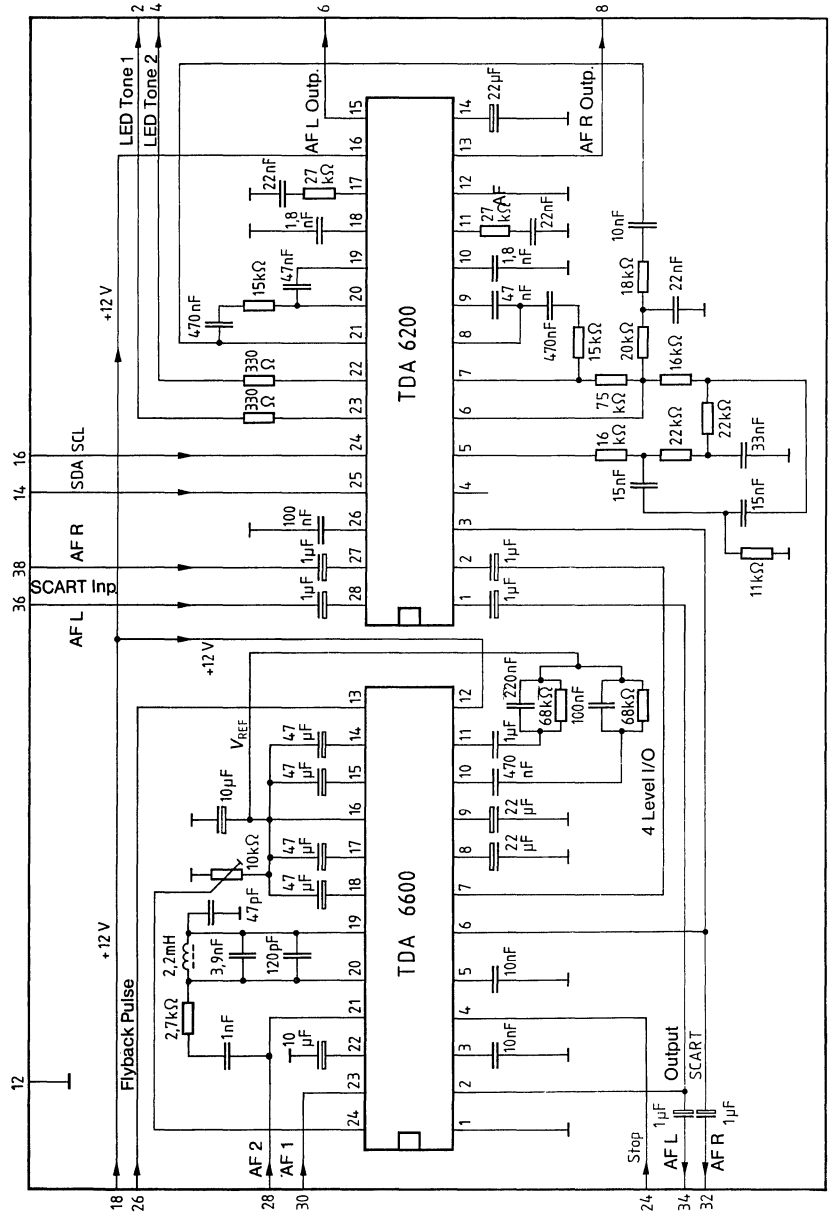
4 level line	Ch1/2 bit	LED 1	LED 2
Mono	X	OFF	OFF
Stereo	X	ON	ON
Dual	0	ON	OFF
Dual	1	OFF	ON

SCART playback mode:

SC bit	Ch bit	Ch1/2 bit	LED 1	LED 2
1	0	X	ON	ON
1	1	0	ON	OFF
1	1	1	OFF	ON

Application circuit

Stereo decoder, matrix and tone control



MIN 6

The bipolar IC TFA 1001 W contains a photodiode and an amplifier. At its output (open NPN collector), the TFA 1001 W supplies a current directly proportional to the illuminance. Another pin permits a linearized characteristic curve at low illuminances and can be used to inhibit the output.

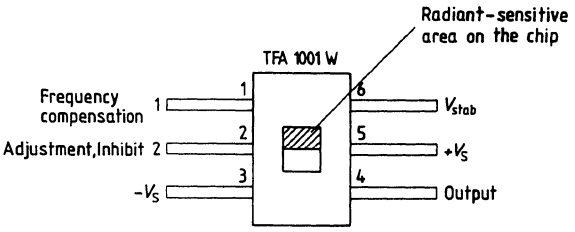
Application

- Exposure meters
- Exposure control systems
- Electronic flashes
- Optical follow-up control
- Smoke detectors
- Linear optocouplers
- Color identification

Features

- High sensitivity
- High output current linearity
- Good spectral sensitivity
- Low current consumption
- Wide modulation range
- Large operating voltage range

Pin configuration



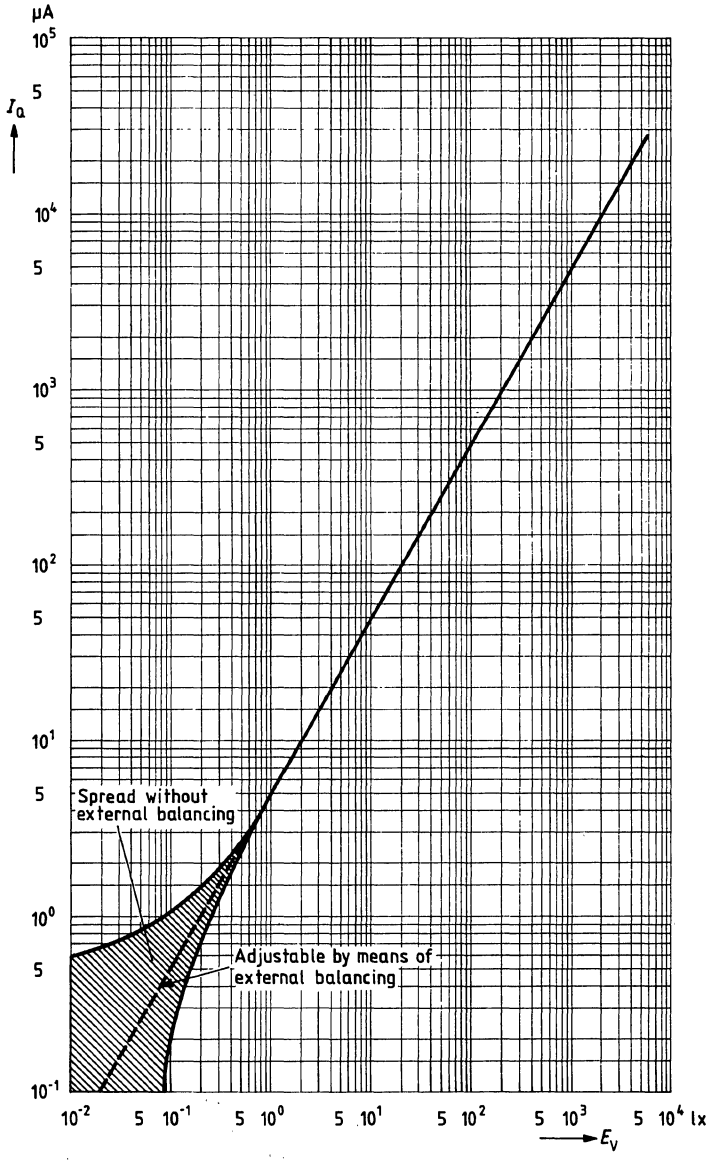
Maximum ratings

		Lower limit B	Upper limit A	
Supply voltage	V_S		15	V
Output current	I_Q		50	mA
Power dissipation	P_{tot}		200	mW
Junction temperature	T_j		100	°C
Storage temperature	T_{stg}	−40	85	°C
Thermal resistance (system-air)	$R_{th\,SA}$		250	K/W

Characteristics at $T_{amb} = 25$ °C, supply voltage applied to pin 5

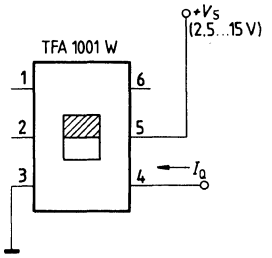
		Lower limit B	typ	Upper limit A	
Supply voltage	V_S	2.5		15	V
Current consumption at $E_v = 0$ lx	I_S	−10		1	mA
Ambient temperature (during operation)	T_{amb}			70	°C
Illuminance	E_v	0		5000	lx
Sensitivity in range					
$E_v = 1$ lx to 1000 lx	S	2.5	5	7.5	µA/lx
Output current at					
$E_v = 0.05$ lx	I_Q		0.25		µA
$E_v = 1$ lx	I_Q	2.5	5	7.5	µA
$E_v = 1000$ lx	I_Q	2.5	5	7.5	mA
$E_v = 5000$ lx	I_Q		25		mA
Stabilized voltage at pin 6	V_{stab}	1.2	1.35	1.5	V
Supply voltage dependence of stabilized voltage V_{stab}	$\Delta V_{stab}/\Delta V_S$		2		mV/V
Temperature dependence of stabilized voltage V_{stab}	$\Delta V_{stab}/\Delta T_{amb}$		−0.3		mV/°C

Photocurrent versus illuminance

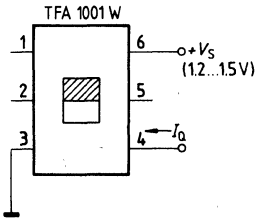


Possible applications of TFA 1001 W as light/current transducer

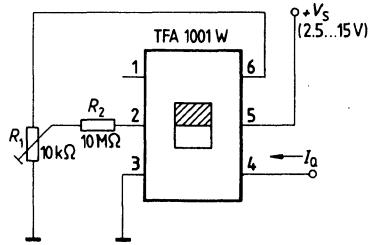
1) for operating voltage 2.5 to 15 V



2) for low operating voltage 1.2 to 1.5 V

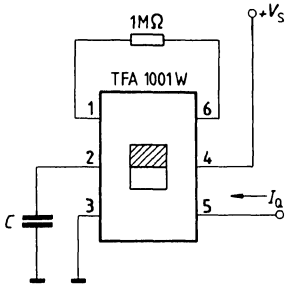


3) for especially low illuminance down to 0.01 lx

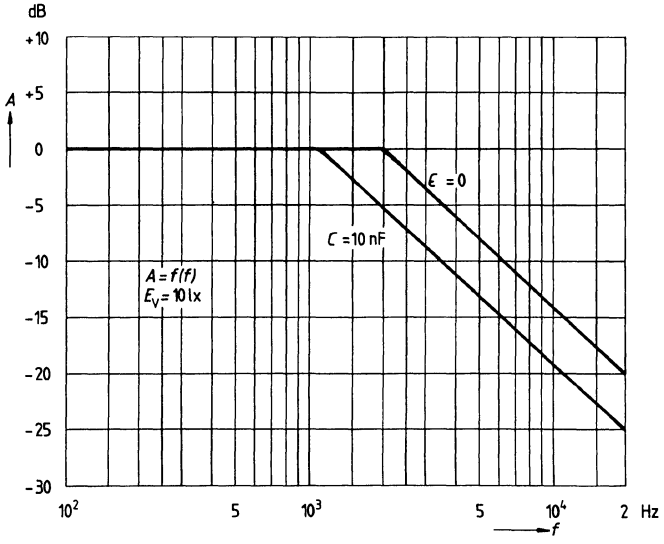


In case of low illuminance (see characteristic: output current versus illuminance), the output current can be balanced by means of the adjustment control R_1. The lower range of the output characteristic can be linearized even more by setting a dark current of about 5 nA.

Dynamic behavior

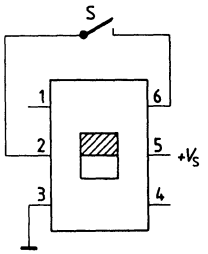


The dynamic behavior can be influenced at connection 2 by connecting capacitors.



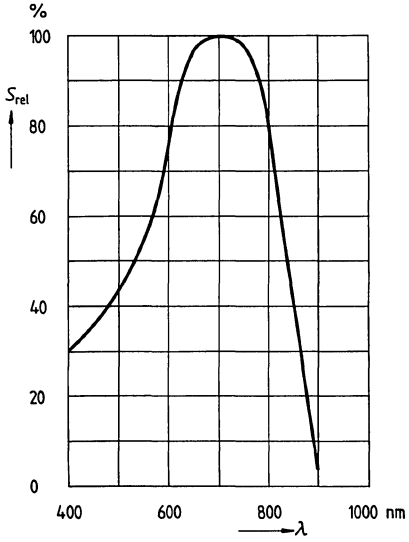
Attenuation $A = \frac{I_Q(f)}{I_Q(f=0)}$

Inhibiting the output

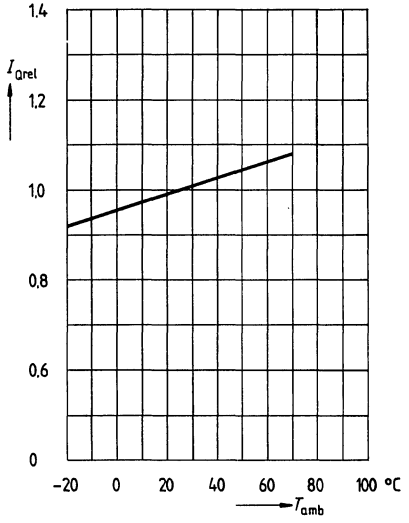


The output can be inhibited by connecting the balancing input with the stabilized voltage (switch, PNP transistor, FET).

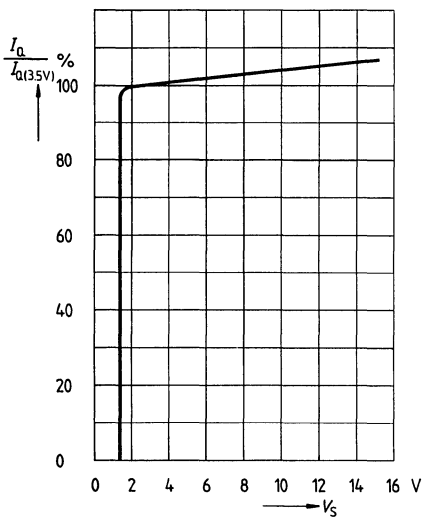
Relative spectral sensitivity versus wavelength



Relative output current versus ambient temperature
in range $E_v = 1$ lx to 1000 lx

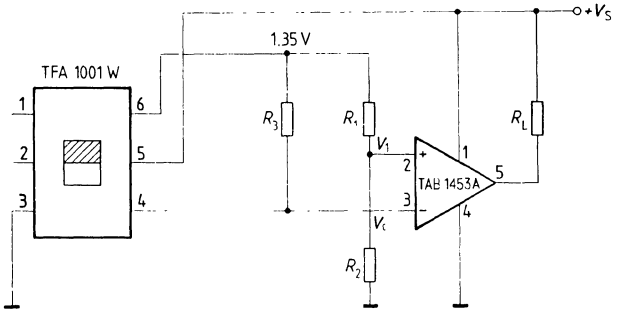


Output current versus supply voltage



Application examples

Simple threshold switch with TAB 1453 A op amp

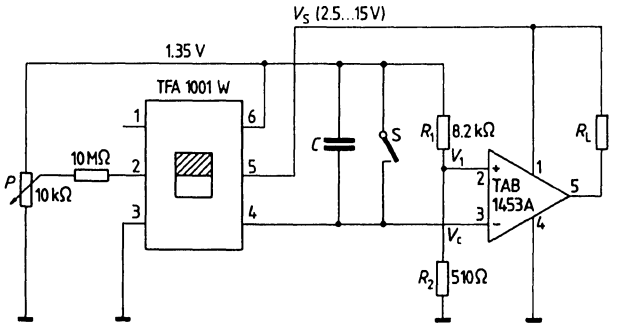


The illustration shows a simple threshold switch as can, for example, be used in cameras to change the aperture or indicate the illuminance. Operational amplifier TAB 1453 A serves as comparator. It has a PNP input and is able to operate at very low supply voltage.

The output is an open collector which can switch currents up to 70 mA.

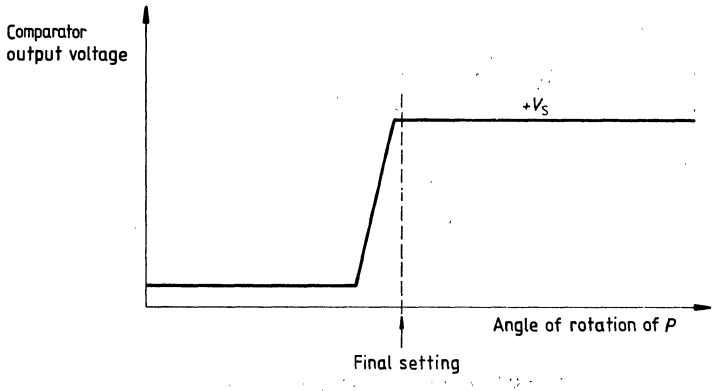
Since the stabilized voltage at pin 6 is used as reference voltage, the circuit is highly independent of the supply voltage.

Shutter speed or exposure control

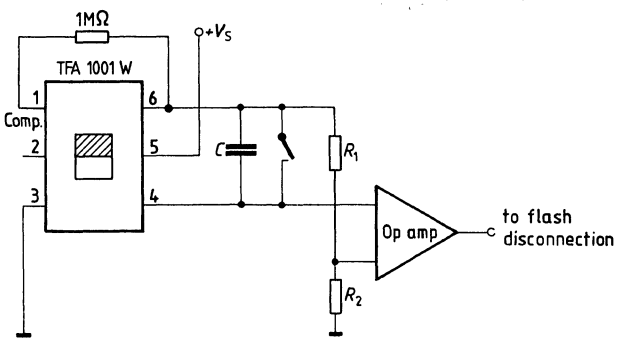


The illustration above shows a light/time control which can, e.g. be used to control the shutter speed in cameras or for exposure time control in enlargers. This circuit operates also largely independently of the supply voltage. A further essential advantage is, that for the major part of the exposure time the comparator input current is insignificant as the corresponding input transistor remains fully off-state. By means of potentiometer P, the operating range can be extended to lower illuminance values. Opening the switch starts the exposure, and capacitor C is charged from pin 4 of the photo IC. The comparator switches if the voltage V_C falls below the reference voltage determined by resistors R_1 and R_2. The relationship between illuminance and time is defined by capacitor C and precision adjustment is possible by means of V_1; V_1, however, must not become less than 0.4 V.

The dark current may be set in the circuit by means of potentiometer *P*. For this purpose, capacitor *C* is removed. *P* is then adjusted in darkness such that the output of the comparator is just blocked. Capacitor *C* is then inserted. (See illustration below).

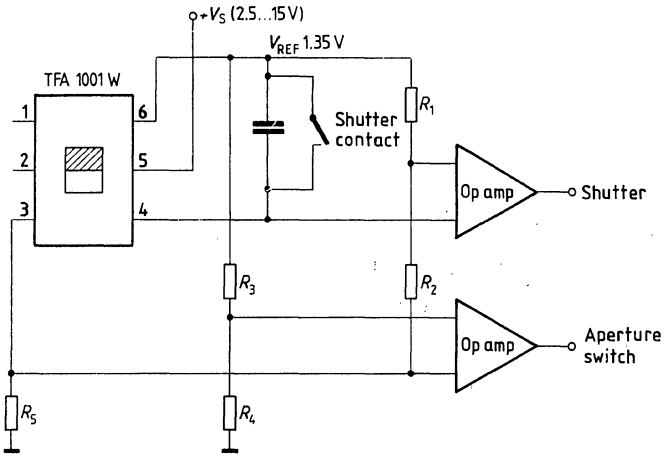


Schematic circuit diagram for an electronic flash control



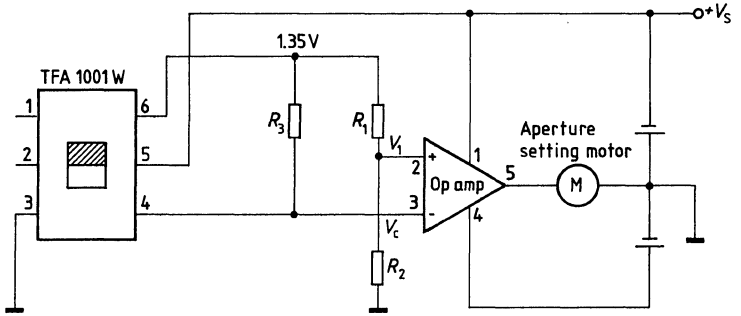
TFA 1001 W can also be used for electronic flash control. It must, however, be ensured that the illuminance does not exceed 5 klx; use a grey filter if necessary. To be able to control very short times, it is useful to connect an additional capacitor to pin 1.

Combined aperture and exposure control



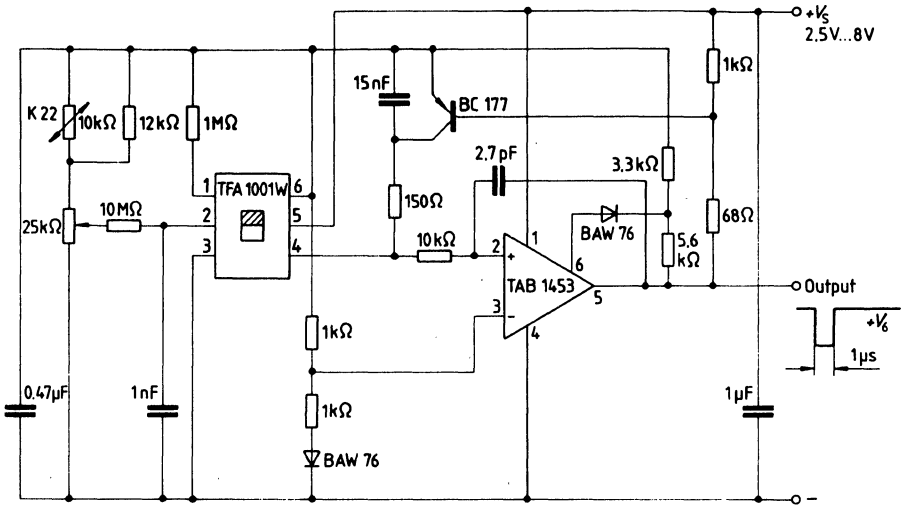
The aperture and exposure control may be combined, with the information for aperture switching being taken from the total current of the photo IC (voltage drop at R_5).

Aperture follow-up control for cine cameras



The op amp compares the voltage drop at R_3, generated by the photoelectric current, with a reference voltage derived from the stabilized voltage, and controls the aperture via motor M.

Light/frequency transducer



Sensitivity: approx. 600 Hz/lx
Range: 4 Hz to 400 000 Hz

- High resolution
- Fully temperature-compensated
- Wide operating voltage range
- High operating voltage suppression
- Wide dynamic range (5 decades)

Particularly suitable for digital processing.

Integrated Hall-Effect Switch for Alternating Magnetic Field

TLB 4902 F

Preliminary data

Plastic Flat Pack

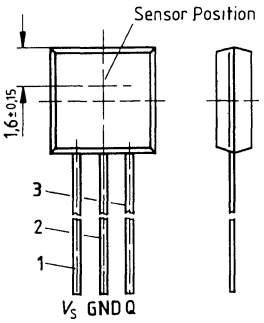
The Hall-effect IC TLB 4902 F is a static contactless switch operated by an alternating magnetic field. The outputs are switched to the conducting state by the south pole of the magnetic field and are blocked by its north pole.

The IC is particularly intended as rpm sensor in consumer applications or as commutation sensor in brushless dc motors.

Features

- Low switching thresholds
- Miniature plastic package
- Suited to low cost applications

Pin configuration

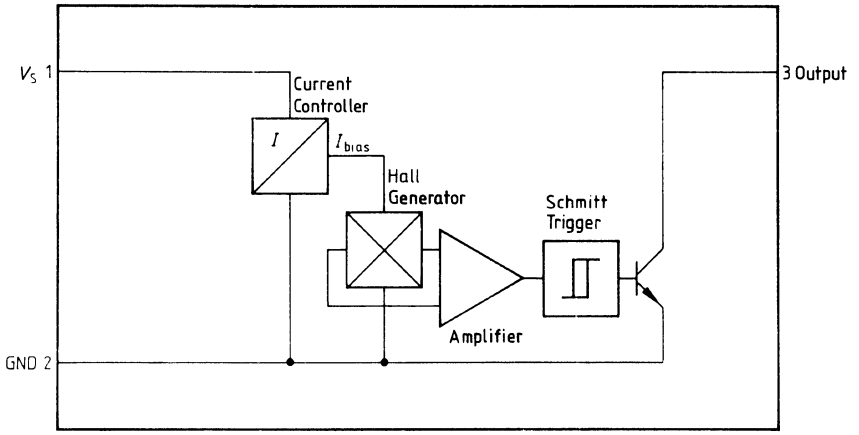


Dimensions in mm

Pin description

Pin	Symbol	Function
1	V_S	Supply voltage
2	GND	Ground
3	Q	Output

Block diagram



Maximum ratings

$T_A = 70\,°C$

		min	max	
Supply voltage	V_S	−0.5	6	V
Output current	I_Q		20	mA
Junction temperature	T_j		125	°C
Storage temperature	T_{stg}	−40	125	°C
Thermal resistance system-air	$R_{th\,SA}$		240	K/W
Flux density	B	$-\infty$	$+\infty$	
Output voltage $B < B_{OFF}$	V_Q		30	V

Operating range

Supply voltage	V_S	4.5	5.5	V
Output current	I_Q		20	mA
Ambient temperature	T_A	0	70	°C

Characteristics

$V_S = 5\,V$; $T_A = 0$ to $70\,°C$

		Test conditions	Test circuit	min	typ	max	
Magnetic flux density[1]							
Operate point	B_{ON}	$T_A = 25\,°C$	2			17	mT[2]
		$T_A = 0$ to $70\,°C$				25	mT
Release point	B_{OFF}	$T_A = 25\,°C$		−17			mT
		$T_A = 0$ to $70\,°C$		−25			mT
Hysteresis B_{ON}-B_{OFF}	B_{Hy}		2	5		15	mT
Output leakage current	I_{Qlk}	$B < B_{OFF}$; V_{QH}=30 V $T_A = 25\,°C$				10	µA
Supply current	I_S	$B < B_{OFF}$		2		5.5	mA
		$B > B_{ON}$		3		6.5	mA
Output saturation voltage	$V_{Q\,sat}$	$I_Q = 16\,mA$	2			0.4	V
Rise time	t_{LH}	$I_Q = 5\,mA$	1		0.3	1	µs
Fall time	t_{HL}	$I_Q = 5\,mA$	1		0.5	1	µs

Reliability and life time of the IC are assured as long as the junction temperature does not exceed 125 °C. Though operation of the IC at the given max. junction temperature of 150 °C is possible a continuous operation at this rating could nevertheless impair the reliability of the IC considerably.

1) The magnetic parameters are specified for a homogenous magnetic field at the sensor center as per fig. 3

2) 1 mT = 10 G

Measurement circuits

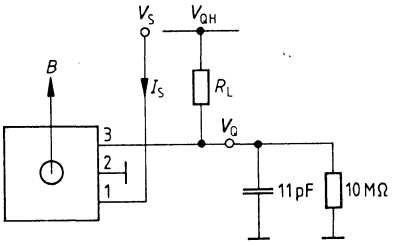


Figure 1

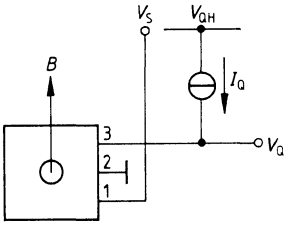


Figure 2

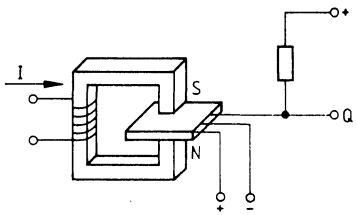
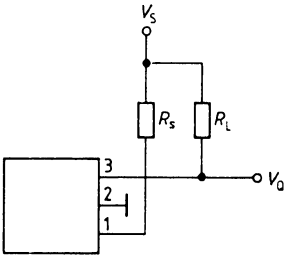


Figure 3

Application circuit



For optimum efficiency of the integrated overvoltage protection, it is suggested, that a resistance R_S of approx. 100 Ω be provided in the component's power supply to limit the current.

Figure 4

Pulse diagram

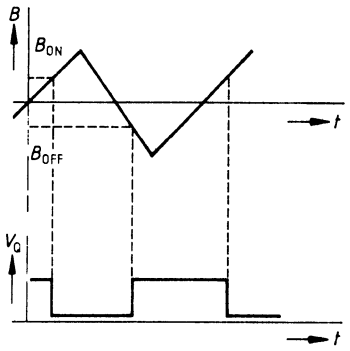


Figure 5

Flux density	V_Q
$B > B_{ON}$	L
$B < B_{OFF}$	H

TLE 3101
TLE 3102
TLE 3103
TLE 3104

DIP 18
DIP 14
DIP 14
DIP 8

These bipolar phase control ICs require, for most applications, only a minimum number of external components. Typical applications are motor control, brightness control, temperature control, cos φ optimization for squirrel-cage motors, and starting current limitation.

Thanks to their high efficiency, the TLE 310x ICs are particularly suitable for consumer goods, such as kitchen equipment and washing machines, vacuum cleaners, electric irons and hobbyist appliances.

A special feature is the soft start which requires only straightforward wiring, and is e.g. used in portable drills for center punching.

Features

- Direct supply from ac line possible
- Low power consumption, typically 2.4 mA
- Only one capacitor for trigger pulse width and phase angle
- Highly stabilized reference voltage
- Negative triac gate trigger current, 100 mA max.
- No triac drive pulses during supply undervoltage
- Optional voltage or current synchronization

- TLE 3101 with independent on-chip op amp OP and comparator K3

The following versions were produced from that basic IC:

- TLE 3102 without comparator K3
- TLE 3103 without op amp OP
- TLE 3104 without K3, enable input E/A, control input $V_{control}$, and without Z diode output.

These simplified versions are provided for less complex low cost applications.

Functional description

The following is a description of the individual functional units (refer to block diagram) and their interactions:

Operational amplifier OP

Two inputs and the output are available. The op amp is internally compensated and has a push-pull output. Should be op amp not be required, the +input is to be connected to ground (the TLE 3101 and TLE 3102 then consume minimum current).

Comparator K 3

Comparator K3 ist not frequency-compsensated. The output is an open NPN collector which may drive e.g. an LED in switching operation. Should the comparator not be required, the −input is to be connected to ground. K3 then has minimum current consumption.

Reference voltage source

A temperature-stabilized voltage source is available for control and regulating circuits.

Sawtooth generator

In this unit, a sawtooth synchronized to the line is generated by the external R_S and C_S. The phase angle of the triac is determined by comparison of the sawtooth voltage and the control voltage. The trigger pulse width for the driver is provided by the falling edge of the sawtooth generator. The charge of C_S determines the trigger pulse width. A special circuit ensures the release of only one trigger pulse per line half period.

Comparators K1, K2

Sawtooth voltage and control voltage are compared by means of comparators K1 and K2. Comparator K2 receives only half the sawtooth voltage. The phase angle limit can be adjusted within the complete phase angle range by applying a reduced reference voltage to input "$V_{\varphi max}$". Comparator K2 provides starting current limitation and/or phase angle limitation for inductive loads. Both comparator outputs are fed to the logic and driver unit.

The comparator with the smaller conduction angle is the dominating one. With $V_{\varphi max}$ dominating, the trigger pulse width is doubled – compared with the trigger pulse width in case of a dominating $V_{control}$.

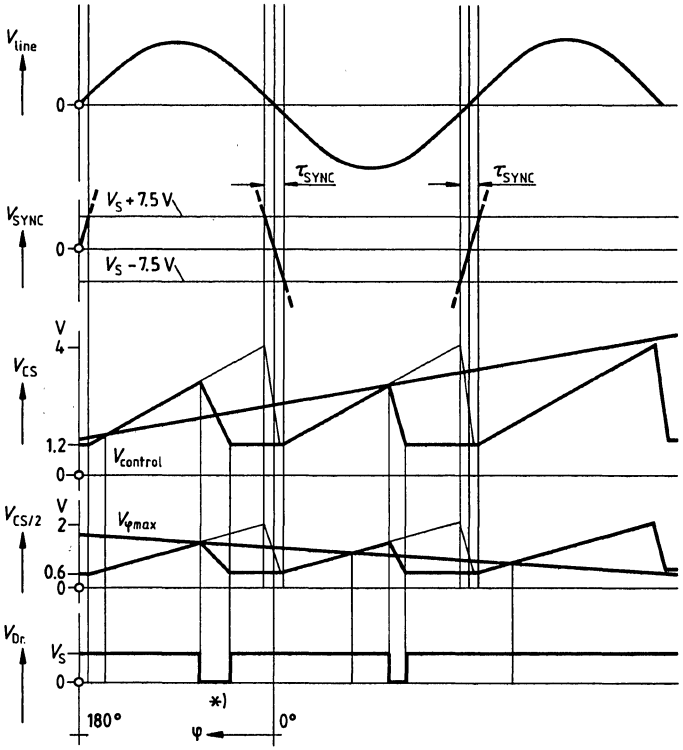
Logic + driver

The logic and driver unit for triac triggering is controlled by comparators K1, K2, and the enable input E/A. The E/A input is TTL-compatible and may disable or enable the trigger pulse. Logic +driver obtain information on the trigger pulse width from the sawtooth. The undervoltage monitoring enables the driver output only if the IC's supply voltage has reached the permissible minimum value. The driver output to the triac supplies negative pulses.

Synchronization

At the sync input, the phase angle is synchronized to the zero crossing point of the line voltage. The sync pulse width τ_{SYNC} has to be twice as large as the trigger pulse width.

Pulse diagram



Conduction angle (with resistive load)

*) With $V_{\varphi max}$ dominating, the trigger pulse width is doubled.

Maximum ratings $T_{amb} = -25$ to 85 °C		Lower limit B	Upper limit A	
Supply voltage	V_S	−0.3	33	V
Inputs op amp K3	V_I	−0.3	33	V
Output op amp	V_{Q1}	−0.3	V_S	V
	I_{Q1}	−5	3	mA
Output K3 (disabled)	V_{Q2}	−0.3	33	V
(enabled)	I_{Q2}	0	40	mA
Output V_{ref}	V_{ref}	−0.3	5	V
Z diode	I_Z	−35	35	mA
Input sync	I_{sync}	−10	10	mA
Input R_S	V_{RS}	−0.3	5	V
Input C_S	V_{CS}	−0.3	5	V
Input $V_{control}$	$V_{control}$	−0.3	V_S	V
Input $V_{\varphi max}$	$V_{\varphi max}$	−0.3	V_S	V
Enable input E/A	$V_{E/A}$	−0.3	33	V
Output driver (disabled)	$V_{Q dr}$	−0.3	33	V
(enabled)	$I_{Q dr}$	0	120	mA
Total power dissipation (time integral)	P_{tot}		700	mW
Junction temperature	T_j		125	°C
Storage temperature	T_{stg}	−55	125	°C
Thermal resistance (system-air)				
TLE 3104	$R_{th SA}$		100	K/W
TLE 3102, TLE 3103	$R_{th SA}$		70	K/W
TLE 3101	$R_{th SA}$		70	K/W

Operating range				
Supply voltage	V_S	10	30	V
Ambient temperature	T_{amb}	−25	85	°C
Input sync	I_{SYNC}	−3.5	3.5	mA

Characteristics $V_S = 10$ to 30 V, $T_{amb} = -25$ to 85 °C		Test conditions	Lower limit B	typ	Upper limit A	
Current consumption						
without output load at op amp, K3, driver, V_{ref} without R_{SYNC} current	I_S	$V_S = 14.5$ V		2.4	3.2	mA
Reference voltage	V_{ref}		1.8	2.0	2.2	V
Load current	$-I_L$		0		3	mA
Stability $V_S = 10$ to 30 V	ΔV_{ref}				10	mV
$I_{ref} = 0$ to 3 mA	ΔV_{ref}				20	mV
Temperature coefficient	$\Delta V_{ref}/\Delta T$		−0.5		0.5	mV/K
Operational amplifier OP						
Open-loop voltage gain	G_{V0}		60	90		dB
Input offset voltage	V_{IO}		−10		10	mV
Input current	$-I_I$				2	µA
Common-mode input voltage range	V_{IC}		0		V_S−3	V
Output current	I_{Q1}		−3		1.5	mA
Transition frequency	f_T			2		MHz
Transition phase	φ_T			120		degrees
Output voltage	V_{Q1}		1.0		V_S−3	V
Comparator K3						
Input current	$-I_I$				2	µA
Input offset voltage	V_{IO}		−20		20	mV
Output enabled	V_{Q2}	$I_{Q2} = 20$ mA		1.0	1.5	V
disabled	I_{Q2}	$V_{Q2} = 30$ V			5	µA
Common-mode input voltage range	V_{IC}		0		V_S−3	V
Input K1 ($V_{control}$)						
Input current	$-I_S$				2	µA
Control range:						
Conduction angle = 0°				4		V
(dependent on R_S and C_S)						
Conduction angle = 175°				1.2		V
Max. perm. conduction angle					SYNC pulse end −5	degrees
Input K2 ($V\varphi_{max}$)						
Input current	$-I_S$				2	µA
Control range:						
Conduction angle = 0°				2		V
(dependent on R_S and C_S)						
Conduction angle = 175°				0.6		V
Max. perm. conduction angle					SYNC pulse end −5	degrees

Characteriscs $V_S = 10$ to 30 V, $T_{amb} = -25$ to 85 °C		Test conditions	Lower limit B	typ	Upper limit A	
Z diode						
Z voltage	V_Z	$I_Z = 5$ mA	13	14.5	16	V
Enable input E/A						
Input current	$-I_I$				2	µA
H input voltage for driver output, active	V_{IH}		2.8			V
L driver output, disabled	V_{IL}				0.8	V
Triac trigger output						
Output, enabled	V_L	$I_Q = 10$ mA	1.4	2	2.5	V
		20 mA	1.4	2	2.5	V
		50 mA	1.4	2	3.0	V
		100 mA	1.4	4	6.0	V
Output, disabled	I_Q	$V_Q = 30$ V			10	µA
Input SYNC						
Switching current	I_{SYNC}			± 20		µA
Switching threshold	V_{SYNC}			$V_S \pm 7.5$		V
Output disconnection at V_S undervoltage	V_S		7.5	8	10	V
Input R_S, C_S (refer to calculation formulae)						
Limit value C_S	C_S		5		100	nF
Limit value R_S	R_S		33			kΩ

Dimensioning notes and calculation formulae

1. Select trigger pulse width according to triac type and load.

2. **Calculate** C_S (for a $V_{control}$ domination)
   C_S (nF) = trigger pulse width (µs) x 0.2
   The formula yields the typical value
   e.g. T = 50 µs results in C_S = 10 nF

3. **Calculate** R_S (for 4 V max. sawtooth voltage)

$$R_S\ (k\Omega) = \frac{1}{\text{trigger pulse width } (\mu s)} \times 2 \times 10^4$$

   The formula yields the typical value
   e.g. T = 50 µs results in R_S = 400 kΩ

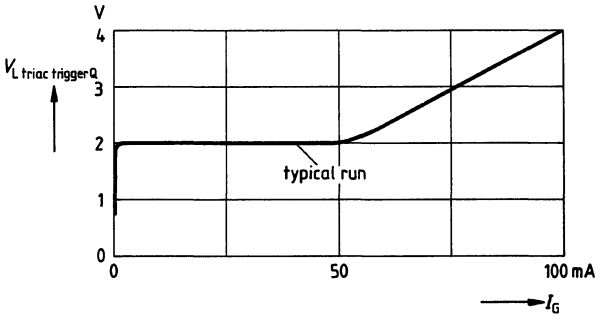
4. **Select R_{SYNC} resistance at SYNC input**
   The sync pulse width (from V_S ± 7.5 V, I_{SYNC} = ± 20 µA) has to be twice as large as the trigger pulse width.

4.1 Sync pulse width ≥ 2 x trigger pulse width x safety factor (according to component deviation and line voltage variation)

4.2 R_{SYNC} (kΩ) = [sync pulse width (µs) x line voltage (V rms) x 2.23×10^{-4} – 7.5] x 50.
e.g. 560 µs sync pulse width and 220 V rms result in R_{SYNC} = 1 MΩ.
With 220 V rms line voltage, the minimum permissible resistance R_{SYNC} is 100 kΩ corresponding to a pulse width of 195 µs.

5. **Calculate** R_G

$$R_G = \frac{V_S - \text{triac gate voltage} - \text{low-voltage triac trigger output}}{I_G}$$



6. **Calculate R_S**

6.1 Calculation of R_S requires first of all the determination of the total current consumption. Insert the arithmetic mean values of the currents for one line cycle.

6.2 $\bar{I}_{tot} = \bar{I}_S = 3.2\ mA + \bar{I}(V_{ref}) + \bar{I}_{Q1}\ (OP) + \bar{I}_{Q2}\ (K3) + \bar{I}$(driver output) $+ \bar{I}$ (additional external circuit currents) $+ |\bar{I}|\ (R_{SYNC})$.

6.3 $R_S\ (k\Omega) = \dfrac{\text{rms line voltage (V)}}{\bar{I}_{tot}\ (mA)} \times 0.455 \times \text{safety factor}$

(corresponding to component deviation and line voltage variation)

e.g. $\bar{I}_{tot} = 5$ mA und $V_{line} = 220$ V result in $R_S = 20\ k\Omega$.

Employing the internal Z diode reduces the IC's V_S voltage to 14.5 V.

7. **Calculate C_G**

7.1 Selection of the maximum permissible ripple at the V_S input, based on the desired functional quality and the special external components.

7.2 The ripple amplitude at the V_S input of the unit should not exceed $V_{pp} = 2$ V.

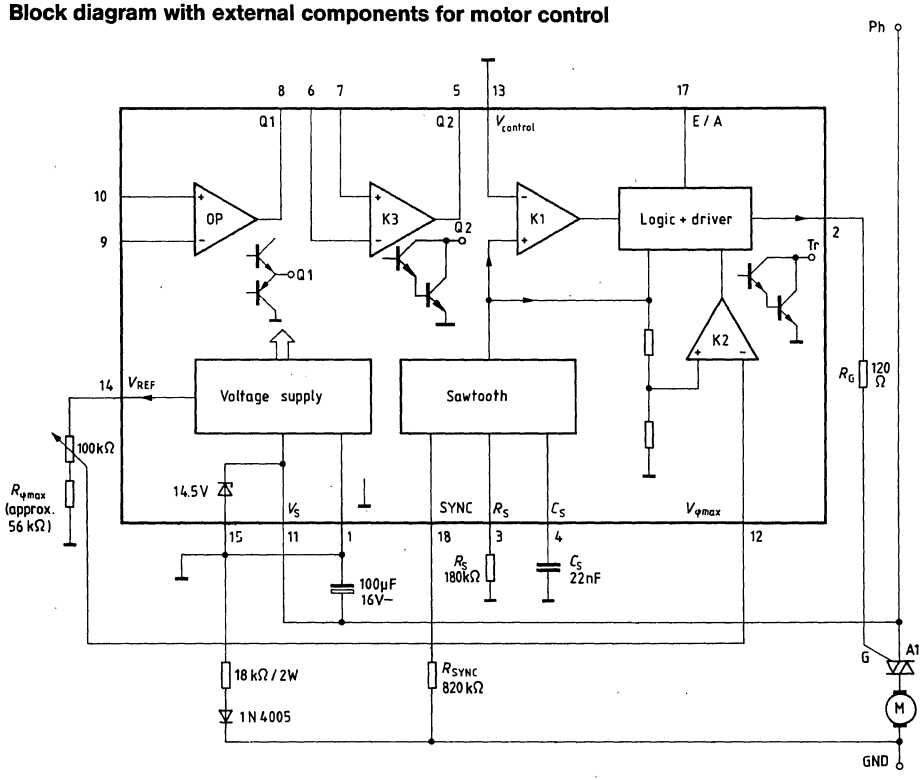
7.3 $C_G\ (\mu F) \geq \dfrac{\bar{I}_{tot}\ (mA)}{V_{pp}} \times 15$

e.g. ripple $V_{pp} = 0.75$ V; $\bar{I}_{tot} = 5$ mA results in $C_G = 100\ \mu F$

Pin configuration for TLE 3101

Pin No.	Function	Pin No.	Function
1	Ground	10	+ input op amp
2	Triac trigger output	11	V_S
3	R_S	12	$V_{\varphi max}$
4	C_S	13	$V_{control}$, K1
5	Output Q2, K3	14	V_{ref}
6	− input K3	15	Z diode
7	+ input K3	16	N.C.
8	Output Q1, op amp	17	Enable input E/A
9	− input op amp	18	Synchronization input (SYNC)

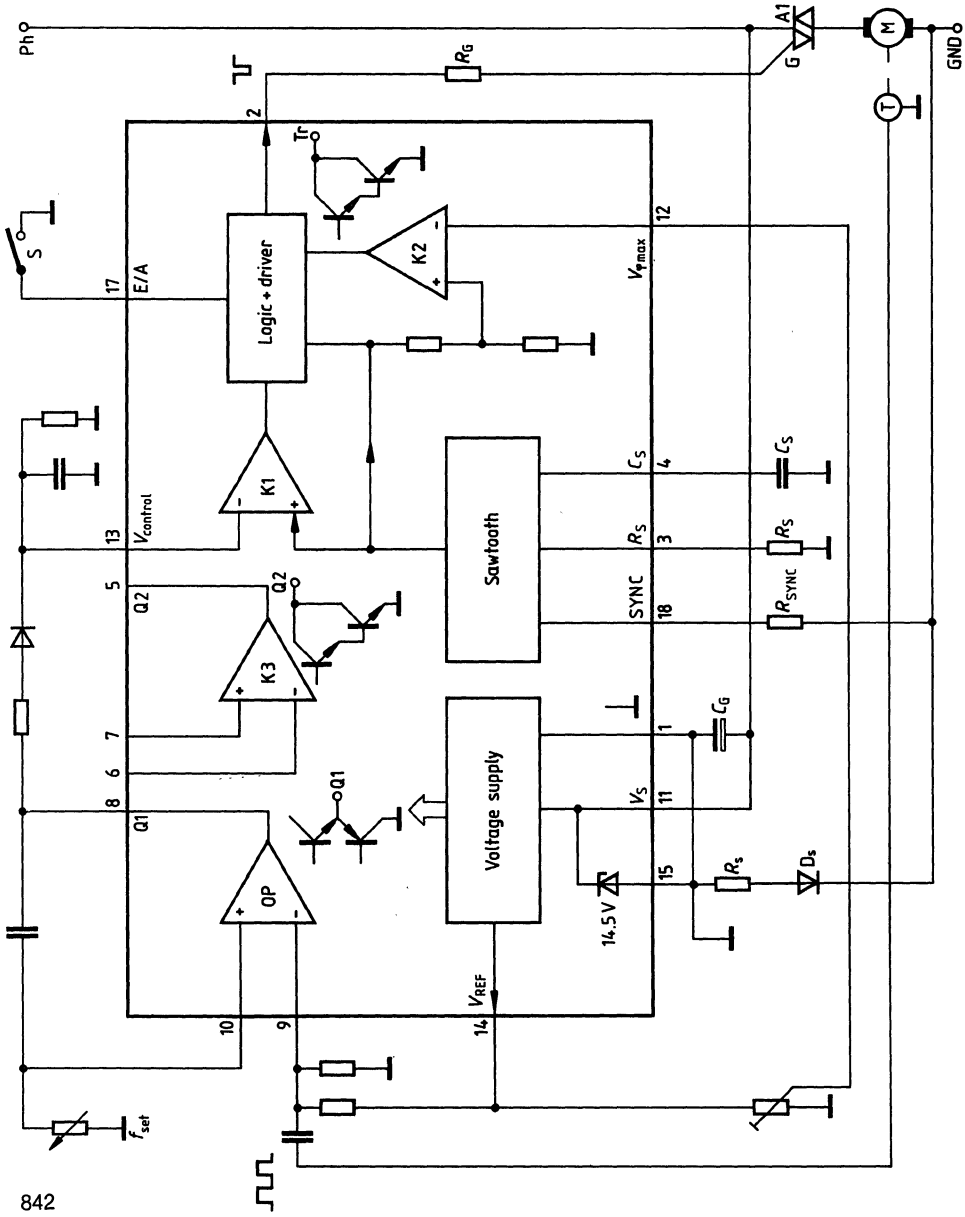
Block diagram with external components for motor control



Application examples

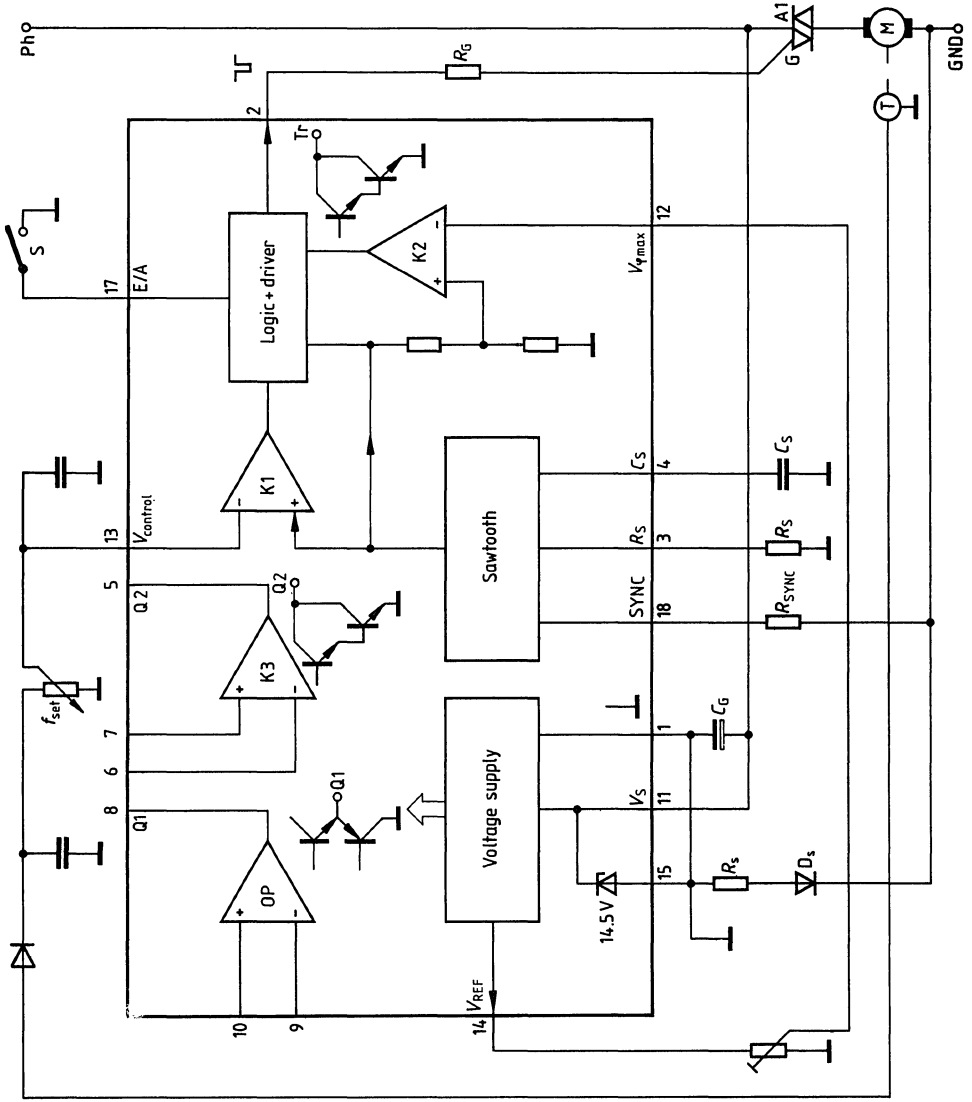
Schematic circuit diagram for motor control using TLE 3101

The tachogenerator provides a **frequency** being processed by the op amp (monoflop).



Schematic circuit diagram for motor control using TLE 3101

The tachogenerator provides a **voltage** which is rectified and stabilized, and then fed to input $V_{control}$.

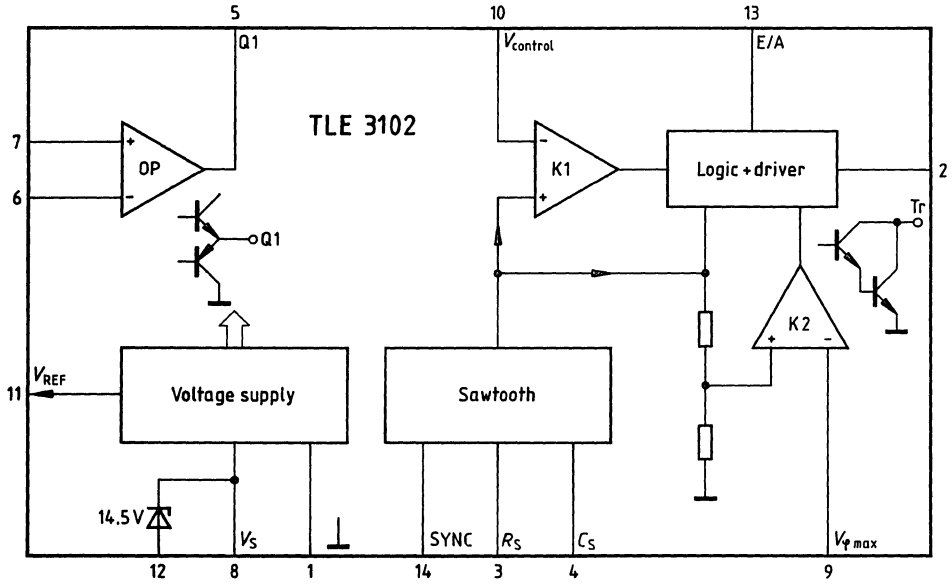


The **TLE 3102** with on-chip op amp for external use is particularly suitable as a speed controller with P, PI, or PID characteristic; the op amp serves as adjustable gain amplifier. An actual value which is proportional to speed can be formed by rectification of the tacho amplitude.

Pin configuration

Pin No.	Function	Pin No.	Function
1	Ground	8	V_S
2	Triac trigger output	9	$V_{\varphi max}$
3	R_S	10	$V_{control}$, K1
4	C_S	11	V_{ref}
5	Output Q1, op amp	12	Z diode
6	− input op amp	13	Enable input E/A
7	+ input op amp	14	Synchronization input (SYNC)

Block diagram

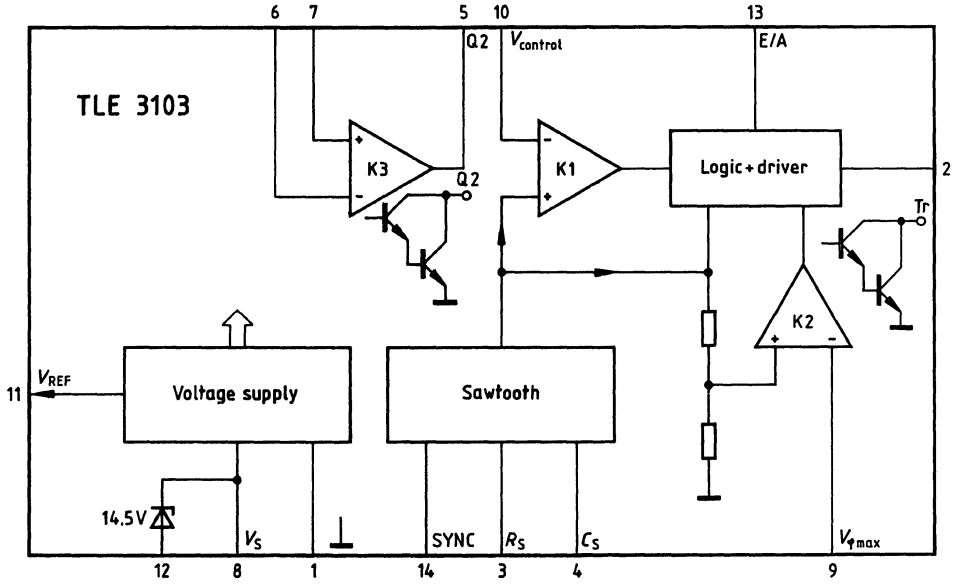


The **TLE 3103** with on-chip comparator for external use is particularly suitable for phase control systems in which special functions, such as blocking protection or overtemperature protection, are required.

Pin configuration

Pin No.	Function	Pin No.	Function
1	Ground	8	V_S
2	Triac trigger output	9	$V_{\varphi max}$
3	R_S	10	$V_{control}$, K1
4	C_S	11	V_{ref}
5	Output Q2, K3	12	Z diode
6	− input K3	13	Enable input E/A
7	+ input K3	14	Synchronization input (SYNC)

Block diagram

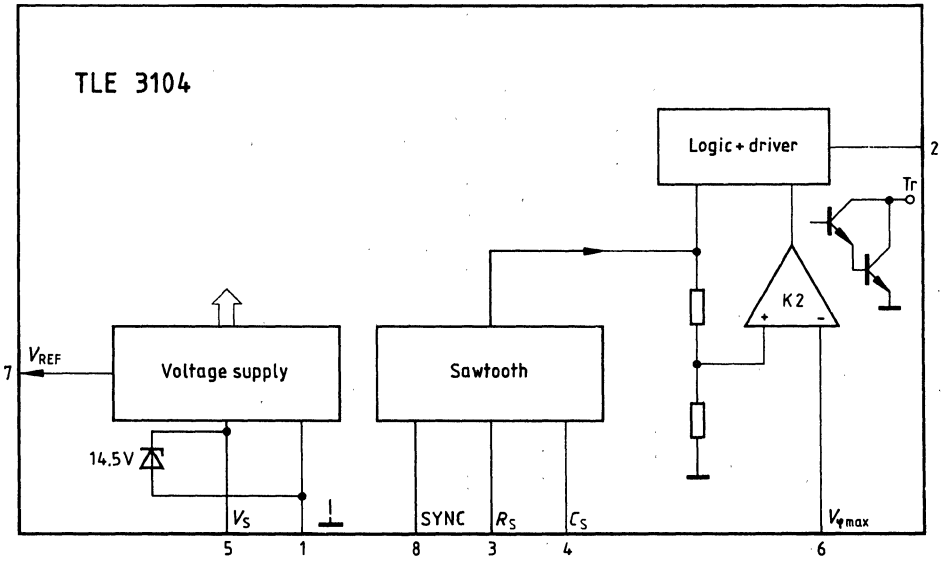


The **TLE 3104** is particularly suitable for simple, low-cost phase control and motor control systems, in which the actual value is formed by rectification of the tacho amplitude.

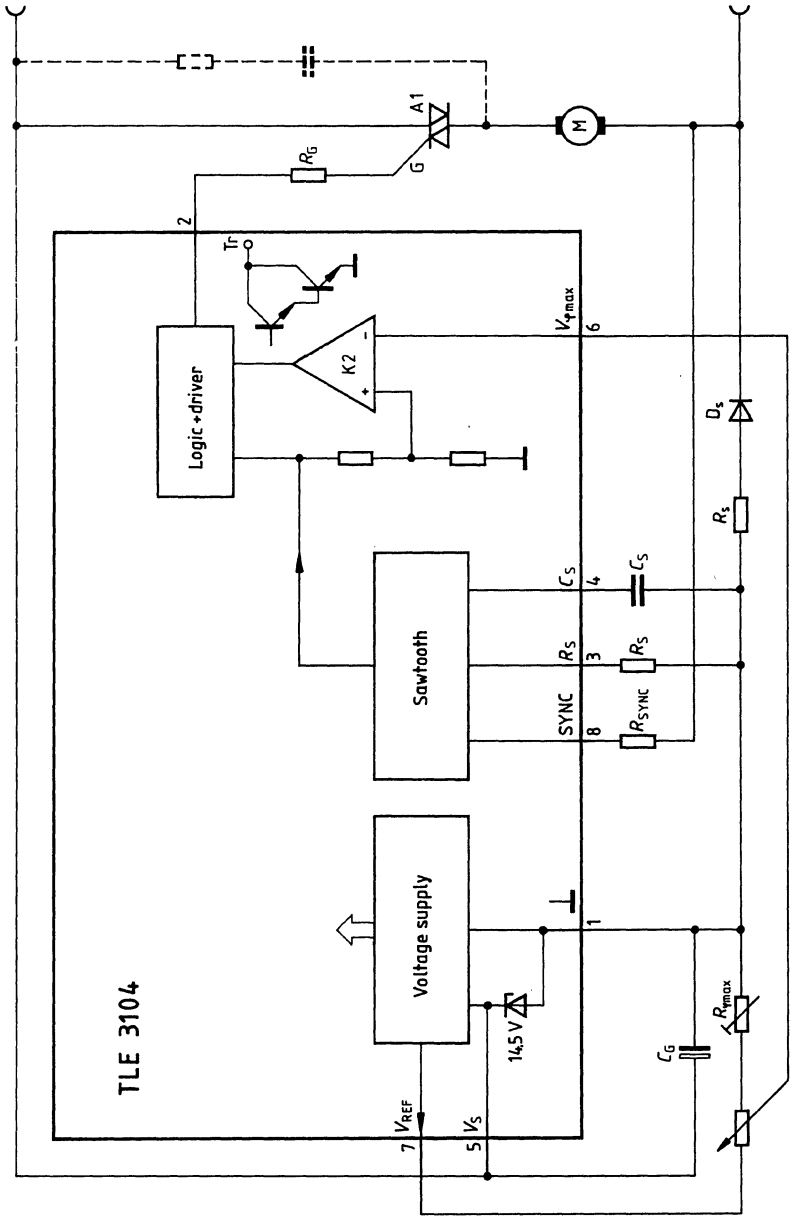
Pin configuration

Pin No.	Function	Pin No.	Function
1	Ground	5	V_S
2	Triac trigger output	6	$V_{\varphi\,max}$
3	R_S	7	V_{ref}
4	C_S	8	Synchronization input (SYNC)

Block diagram

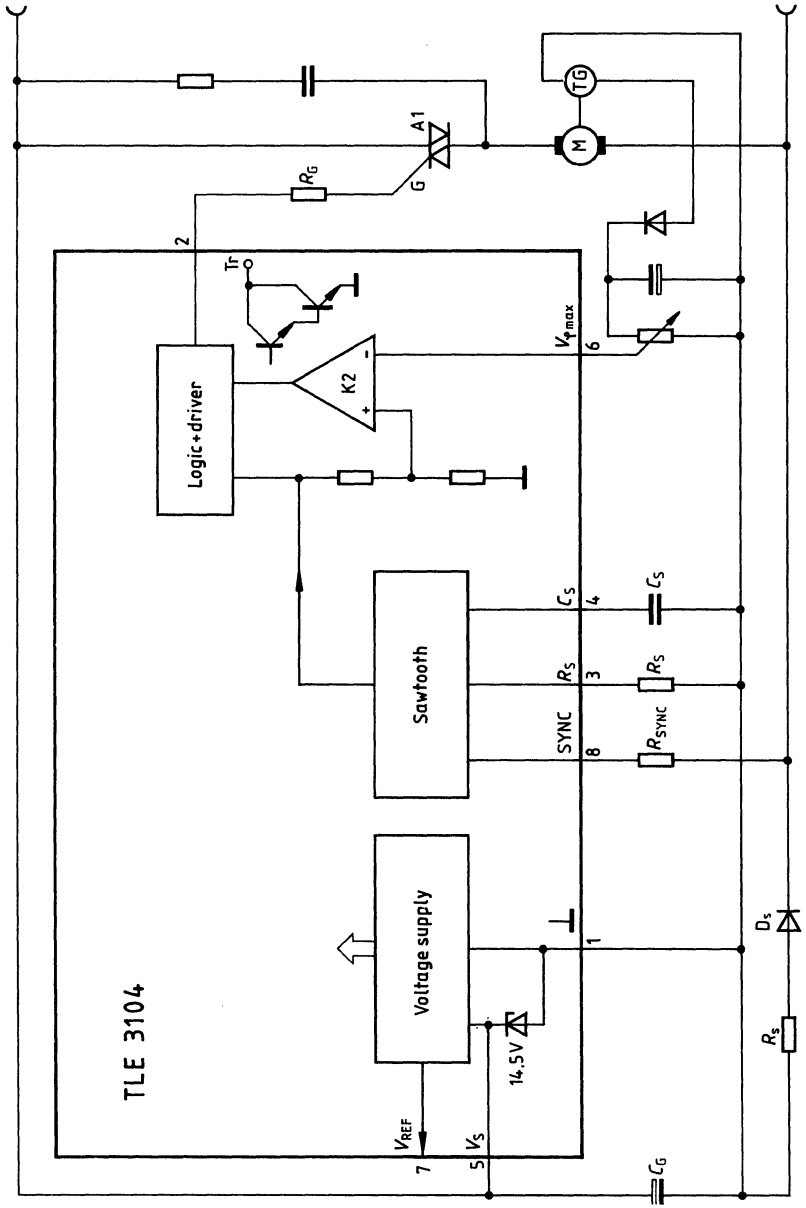


Schematic circuit diagram for motor control using TLE 3104



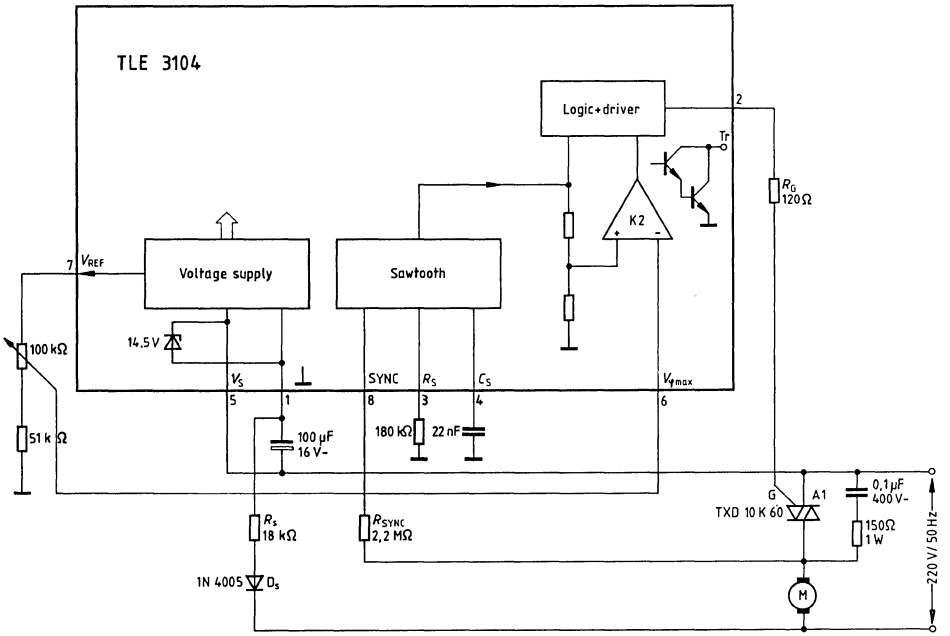
Schematic circuit diagram for motor control using TLE 3104

The tachogenerator supplies a **voltage,** which is rectified and stabilized and then fed to input $V_{control}$.



Current synchronization in case of inductive load control using TLE 3104

Particularly in case of phase control of inductive loads, such as transformers and shaded-pole motors, there is a risk of half-wave operation as a result of the phase shift between voltage and current. In order to avoid this condition, the synchronization resistor is connected to A 2 of the triac (this method cannot be applied in the event of severe brush sparking of the motor).



Notes:

The pulse width selected for the trigger pulse must be so great that the triac reaches its holding current, even with a great phase angle (critical: positive half-wave). For this reason, it may be necessary to select a lower value for the ac line series resistor.

The sync pulse must be at least twice as wide as the trigger pulse (see also page 323 and page 327/para. 4).

DIP 18
SIP 9

The TLE 4201 IC is a dual comparator that is particularly suitable as a driver for reversible dc motors and may also be used as a versatile power driver.

The push-pull power-output stages work in a switch mode and can be combined into a full bridge configuration.

The driving of the comparators may be analog in the form of a window discriminator, or it can be accomplished very simply with digital logic.

Typical applications are follow-up controls, servo drives, servo motors, drive mechanisms, etc.

Features

- Max. output current 2.5 A
- Open-loop gain 80 dB typ.
- PNP input stages
- Large common-mode input-voltage range
- Wide control range
- Low saturation voltages
- SOA protective circuit
- Temperature protection

The TLE 4201 IC comes in two different packages: with the SIP 9 package it is possible to remove the heat by way of a cooling fin to a suitable heatsink, whereas with the DIP 18-L9 package the pins 10 through 18 are thermally linked to the chip and provide for heat dissipation by way of the circuit board.

Block diagram

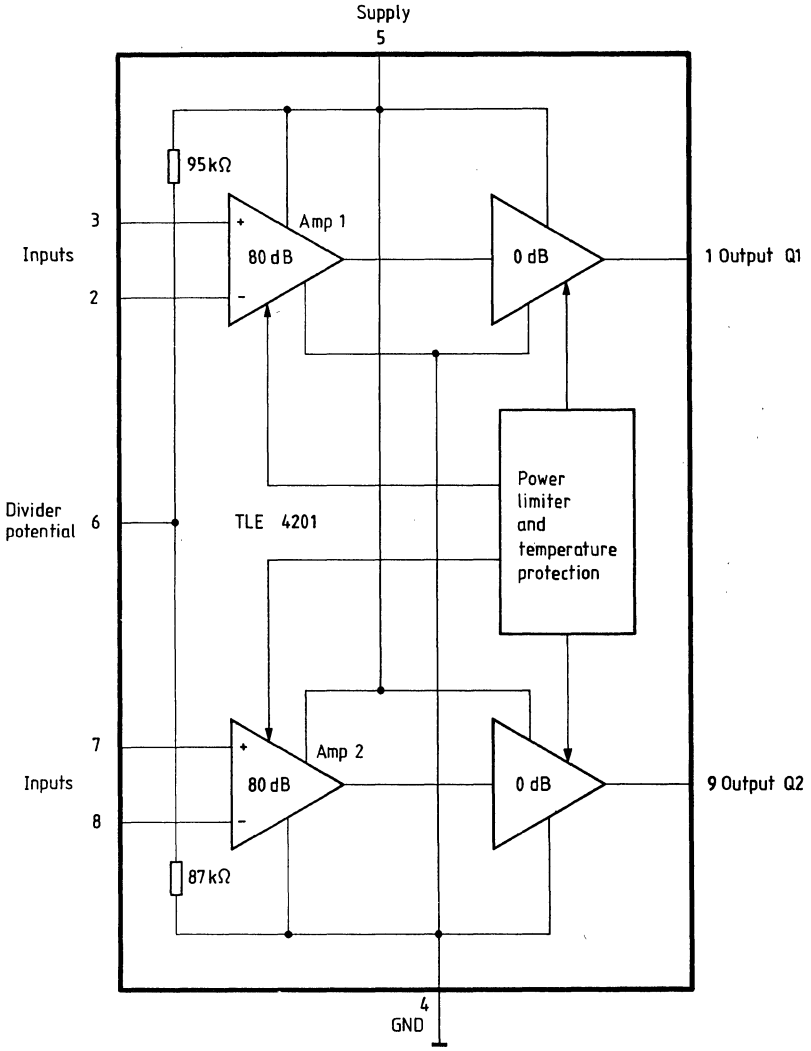


Figure 1

Pin configuration

TLE 4201 A Pin No.	TLE 4201 S Pin No.	Function
1	1	Output of 1st amplifier
2	2	Inverting input of 1st amplifier
3	3	Non-inverting input of 1st amplifier
4	4	Ground
5	5	Supply voltage
6	6	Divider potential
7	7	Non-inverting input of 2nd amplifier
8	8	Inverting input of 2nd amplifier
9	9	Output of 2nd amplifier
10 to 18	—	Ground; to be connected to pin 4

Circuit description

The IC contains two amplifiers featuring a typical open-loop voltage gain of 80 dB at 500 Hz. The input stages are PNP differential amplifiers. This results in a common-mode input voltage range from 0 V to almost the value of V_S, and in a maximum input differential voltage of I V_S I. To obtain low saturation voltages, the sink transistor (lower transistor) of the push-pull AB output stage is internally bootstrapped. An SON protective circuit protects the IC against motor short circuits and ground short circuits. An internal overtemperature protection protects the IC against overheating in case of failure due to insufficient cooling or overload.

For logic control, a divider potential of approx. $V_S/2$ is available at pin 6 (see application circuit 2). This makes the IC particularly suitable for digital circuits, as power driver.

Application

Figure 2 shows a window discriminator operation with the control voltage V_I.
The window within which the motor is to stop is set by R_2.

Figure 3 shows driving by logic inputs A and B. The motor is controlled according to the following truth table.

A	B	Output
L	L	Motor stopped (slowed down)
L	H	Motor turns right
H	L	Motor turns left
H	H	Motor stopped (slowed down)

Application circuits

Operated as window discriminator

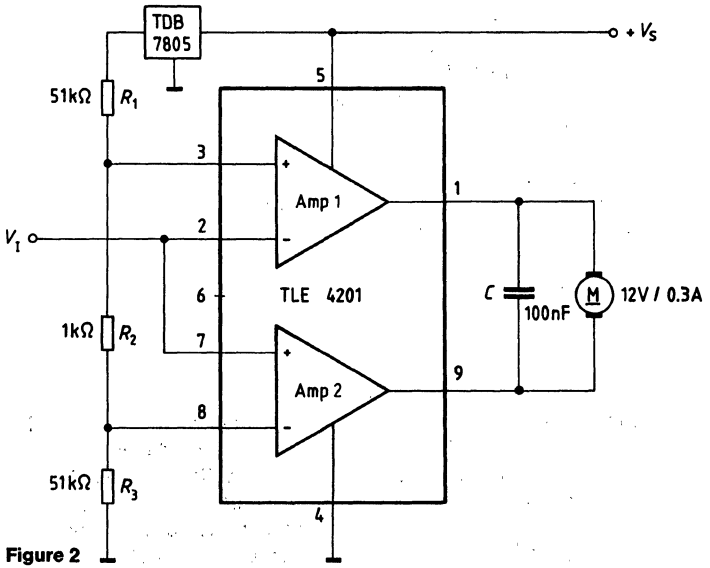


Figure 2

Digital control

for input signals applies: H ≥ 0.6 V_S
L ≤ 0.3 V_S

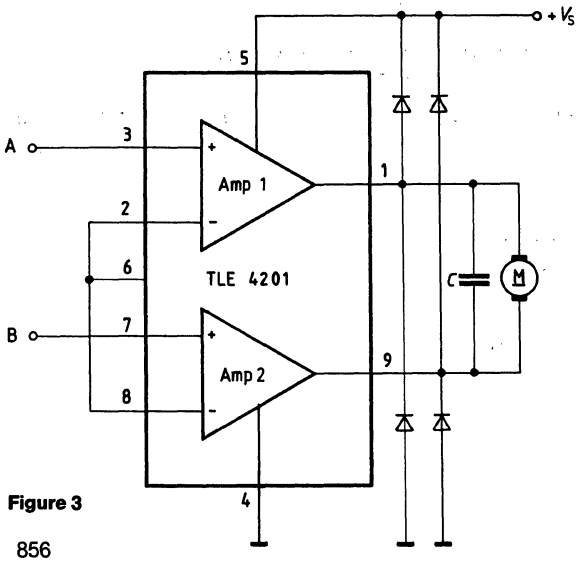


Figure 3

Maximum ratings

$T_{case} = -35$ °C to 85 °C

		Lower limit B	Upper limit A	
Supply voltage	V_S		25	V
Supply voltage ($t \leq 50$ ms)	V_S		36	V
Output current	I_Q		2.5	A
Voltage of pins 2, 3, 6, 7, 8	V	−0.3	V_S	V
Voltage of pins 1, 9	V	−0.3		V
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	−55	125	°C
Thermal resistance				
TLE 4201 S: system-air	$R_{th\,JA}$		65	K/W
system-case	$R_{th\,JC}$		8	K/W
TLE 4201 A: system-air[1]	$R_{th\,JA}$		60	K/W
system-PC board[1]	$R_{th\,JA1}$		44[1]	K/W

Operating range

Supply voltage	V_S	3.5	17	V
Case temperature	T_{case}	−35	85	°C
Voltage gain (at negative feedback with external components)	G_V	25		dB

Characteristics

$V_S = 13$ V, $T_{case} = 25$ °C

		Test conditions	S1	Lower limit B	typ	Upper limit A	
Supply current	I_S	Figure 4: S = 1			20	30	mA
Open-loop voltage gain	G_{V0}	$f = 500$ Hz			80		dB
Input resistance	R_I	$f = 1$ kHz		1	5		MΩ
Saturation voltages,		Figure 5:	S1				
source operation	$V_{Q\,10}$	$I_Q = 0.3$ A	1		1.0	1.1	V
		$I_Q = 1.0$ A	1		1.2	1.6	V
sink operation	$V_{Q\,20}$	$I_Q = -0.3$ A	2		0.35	0.5	V
		$I_Q = -1.0$ A	2		0.7	1.0	V
Rise time of V_Q	t_r	Figure 4 and 6			1.5		µs
Fall time of V_Q	t_f	Figure 4 and 6			1.5		µs
Turn-on delay time	t_{on}	Figure 4 and 6			3.0		µs
Turn-off delay time	t_{off}	Figure 4 and 6			1.5		µs
Input current		Figure 5					
(pins 2, 3, 7, 8)	I_I	$V_{2,3,7,8} = 0$			1.5	3.0	µA
Input offset voltage	V_{IO}	Figure 7		−20		20	mV

1) see figure 8

Test circuits

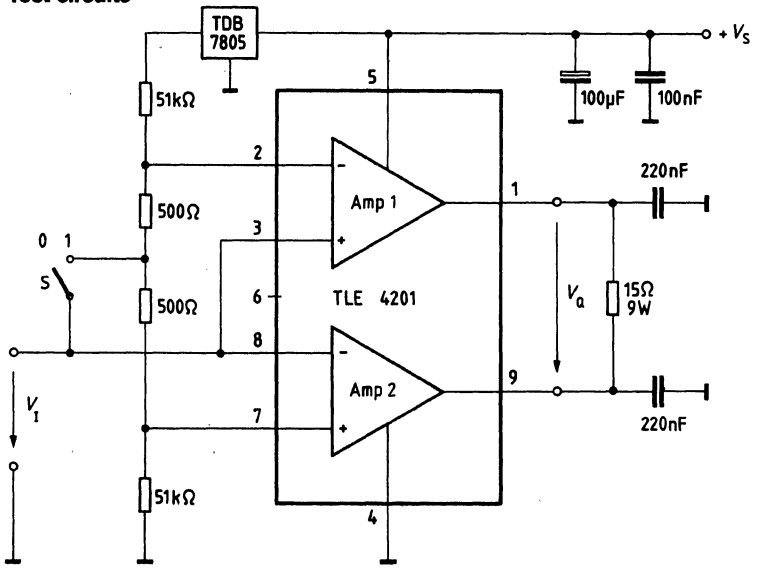


Figure 4

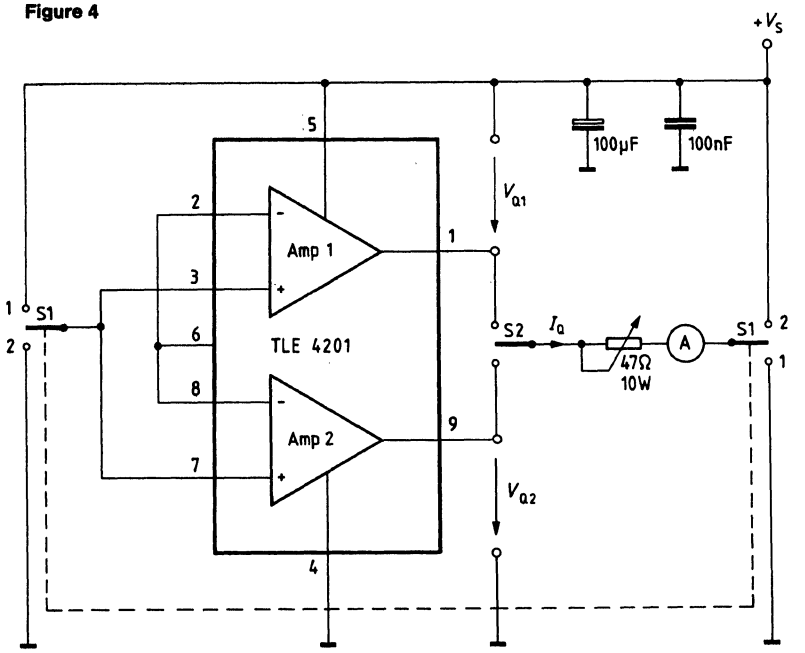


Figure 5

Pulse diagram

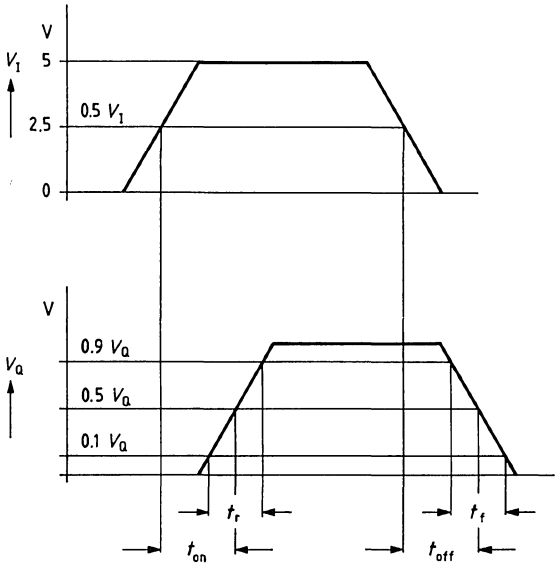


Figure 6

Test and measurement circuit

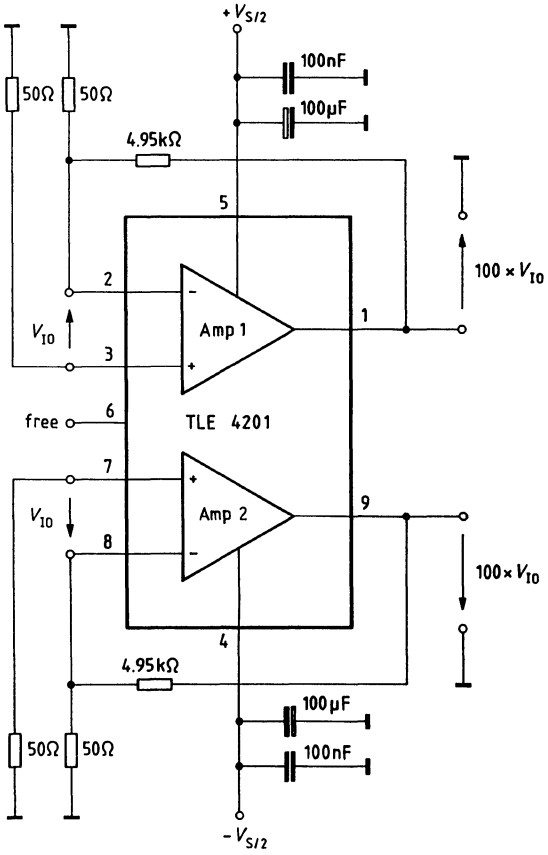


Figure 7

Thermal resistance of TLE 4201 A

Thermal resistance, junction-air, $R_{th\ JA\ 1}$ (standard) versus side length l of a square copper-clad cooling surface (35 µm copper plate)

$R_{th\ JA}$ $(l = 0) = 60$ K/W
$T_{amb} \leq 70$ °C
$P_V = 1$ W
substrate vertical
circuit vertical
static air

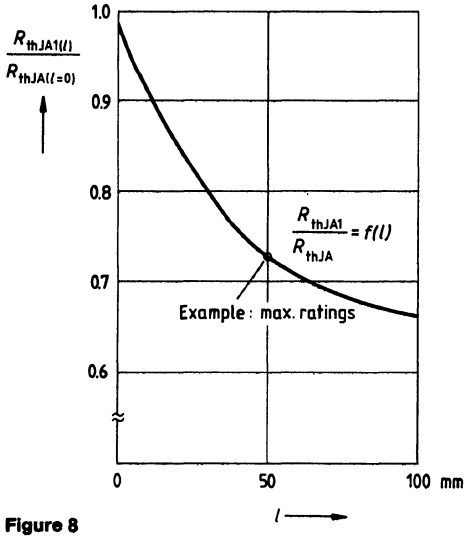


Figure 8

Integrated Hall-Effect Switch for Alternating Magnetic Field

TLE 4901 F TLE 4901 K

Preliminary data

The Hall-effect IC TLE 4901 is a static contactless switch operated by an alternating magnetic field. The outputs are switched to the conducting state by the south pole of the magnetic field and blocked by its north pole.

The IC includes an integrated overvoltage protection against most of the transients occurring in automotive and industrial applications.

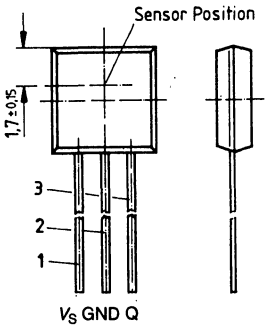
The IC is particularly intended as rpm sensor or shaft encoder. The IC along with a multiple pole ring magnet is especially suited to high-speed applications: speedometer, pickups, rpm indicators, angle indicators, etc.

Features

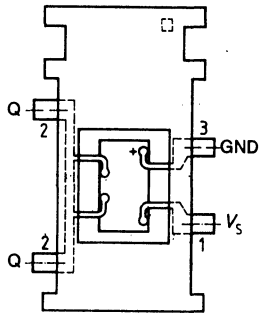
- Low switching thresholds
- High interference immunity
- Overvoltage protection
- Large temperature range

Pin configurations

TLE 4901 F



TLE 4901 K



Dimensions in mm

Pin description

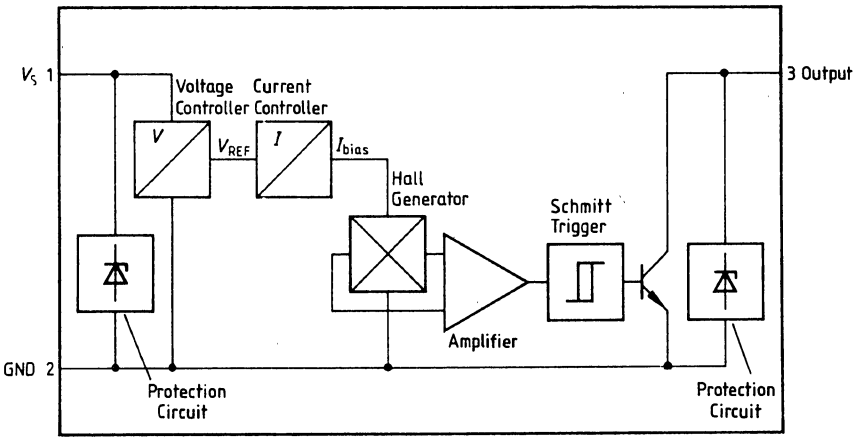
TLE 4901 F

Pin	Symbol	Function
1	V_S	Supply voltage
2	GND	Ground
3	Q	Output

TLE 4901 K

Pin	Symbol	Function
1	V_S	Supply voltage
2	Q	Output
3	GND	Ground

Block diagram



Maximum ratings

$T_A = -30$ to 125 °C

		min	max	
Supply voltage	V_S	−1.2	30	V
Output current	I_Q		40	mA
Junction temperature	T_j	−40	150	°C
Storage temperature	T_{stg}	−40	135	°C
Thermal resistance system-air	$R_{th\,SA}$		240	K/W[1]
Flux density	B	$-\infty$	$+\infty$	
Output voltage $B < B_{OFF}$	V_Q		30	V

Operating range

Supply voltage	V_S	4.5	30	V
Output current	I_Q		32	mA
Ambient temperature	T_A	−30	130	°C

Characteristics

$V_S = 14$ V; $T_A = -30$ to 125 °C

		Test conditions	Test circuit	min	typ	max	
Magnetic flux density[2]							
Operate point	B_{ON}	$T_A = 0$ to 70 °C				20	mT[3]
		$T_A = -30$ to 100 °C				22	mT
		$T_A = -30$ to 125 °C	2			25	mT
Release point	B_{OFF}	$T_A = 0$ to 70 °C		−20			mT
		$T_A = -30$ to 100 °C		−22			mT
		$T_A = -30$ to 125 °C	2	−25			mT
Hysteresis TLE 4901F	B_{Hy}		2	2		15	mT
(B_{ON}-B_{OFF}) TLE 4901K				4		15	mT
Output leakage current	I_{Qlk}	$B < B_{OFF}$; V_{OH}=30 V $T_A = 25$ °C				10	µA
Supply current	I_S	$B < B_{OFF}$	1			13	mA
		$B > B_{ON}$				14	mA
Output saturation voltage	$V_{Q\,sat}$	$I_Q = 10$ mA	2			0.4	V
Rise time	t_{LH}	$I_Q = 10$ mA				1	µs
Fall time	t_{HL}	$I_Q = 10$ mA				1	µs

An optimal reliability and life time of the IC are assured as long as the junction temperature does not exceed 125 °C. Though operation of the IC at the given max. junction temperature of 150 °C is possible a continuous operation at this rating could nevertheless impair the reliability of the IC considerably.

1) Thermal resistance of TLE 4901 K depends on type of mounting.

2) The magnetic parameters are specified for a homogenous magnetic field at the sensor center as per fig. 3.

3) 1 mT = 10 G

Measurement circuits

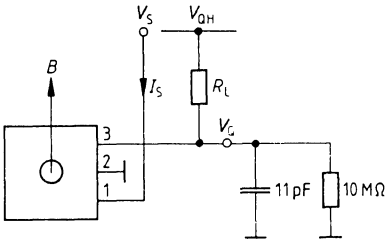


Figure 1

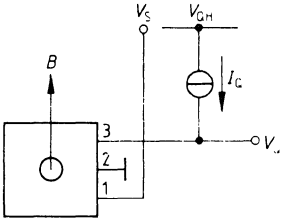


Figure 2

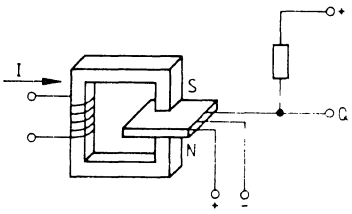
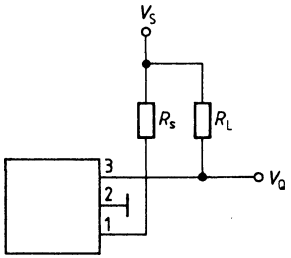


Figure 3

Application circuit



For optimum efficiency of the integrated overvoltage protection, it is suggested that a resistance R_S of approx. 100Ω be provided in the component's power supply to limit the current.

Figure 4

Pulse diagram

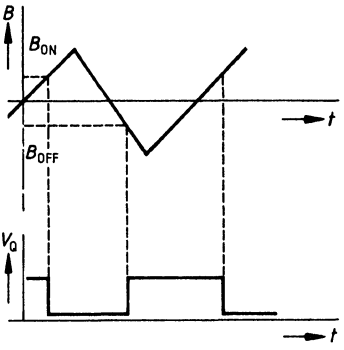


Figure 5

Integrated Hall-Effect Switch for Unipolar Magnetic Field

TLE 4903 F

Preliminary data

Plastic Flat-Pack

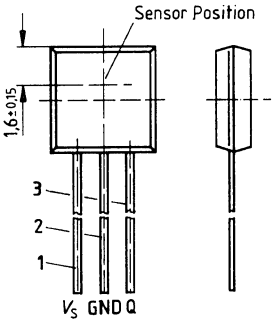
The integrated Hall-effect switch TLE 4903 F is a contactless "normally-off" switch operated by a magnetic field. The open collector output is switched to conducting state by the south pole of the magnetic field.

The IC is provided with an integrated overvoltage protection against most of the transients occurring in automotive and industrial applications.

Features

- Low switching thresholds
- High interference immunity
- Overvoltage protection
- Large temperature range

Pin configuration

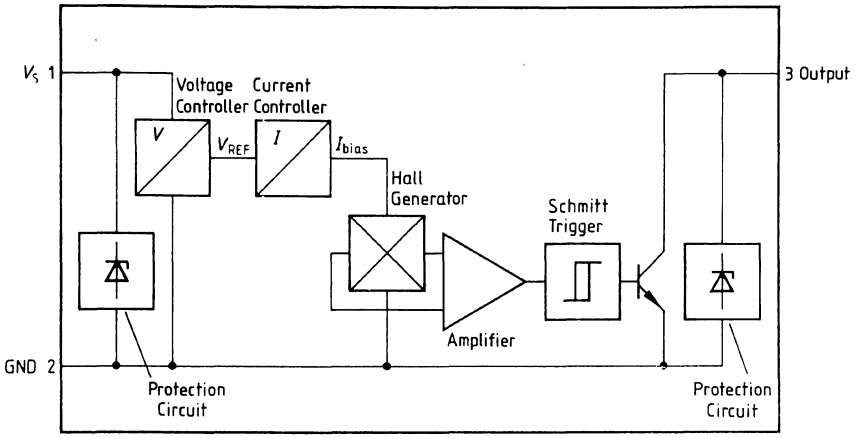


Dimensions in mm

Pin description

Pin	Symbol	Function
1	V_S	Supply voltage
2	GND	Ground
3	Q	Output

Block diagram



Maximum ratings

$T_A = -30$ to 125 °C

		min	max	
Supply voltage	V_S	−1.2	30	V
Output current	I_Q		40	mA
Junction temperature <70000 h	T_j	−40	150	°C
Storage temperature	T_{stg}	−55	125	°C
Thermal resistance system-air	$R_{th\,SA}$		240	K/W
Flux density	B	$-\infty$	$+\infty$	
Output voltage	V_Q		30	V

Operating range

Supply voltage	V_S	4.3	30	V
Output current	I_Q		25	mA
Ambient temperature	T_A	−30	125	°C

Characteristics

$V_S = 14$ V; $T_A = -30$ to 125 °C

		Test conditions	Test circuit	min	typ	max	
Magnetic flux density[1]							
Operate point	B_{ON}	$T_A = 0$ to 70 °C		24		46	mT[2]
		$T_A = -30$ to 100 °C		18		52	mT
		$T_A = -30$ to 125 °C	2	17		53	mT
Release point	B_{OFF}	$T_A = 0$ to 70 °C		17		31	mT
		$T_A = -30$ to 100 °C		11		37	mT
		$T_A = -30$ to 125 °C	2	10		38	mT
Hysteresis B_{ON}-B_{OFF}	B_{Hy}		2	7		15	mT
Output leakage current	I_{Qlk}	$B < B_{OFF}$; $V_{QH} = 24$ V $T_A = 25$ °C				10	µA
Supply current	I_S	$B < B_{OFF}$	1			13	mA
		$B > B_{ON}$	1			14	mA
Output saturation voltage	$V_{Q\,sat}$	$I_Q = 30$ mA	2			0.4	V
Rise time	t_{LH}	$I_Q = 10$ mA				1	µs
Fall time	t_{HL}	$I_Q = 10$ mA				1	µs

Reliability and life time of the IC are assured as long as the junction temperature does not exceed 125 °C. Though operation of the IC at the given max. junction temperature of 150 °C is possible, a continuous operation at this rating could nevertheless impair the reliability of the IC considerably.

1) The magnetic parameters are specified for a homogenous magnetic field at the sensor center as per fig. 3.

2) 1 mT = 10 G

Measurement circuits

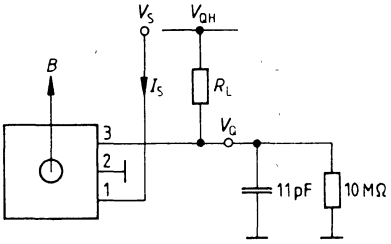


Figure 1

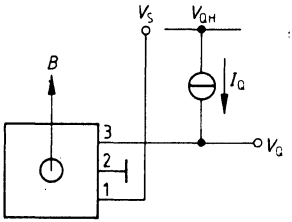


Figure 2

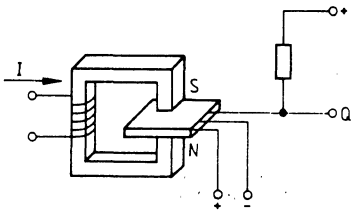
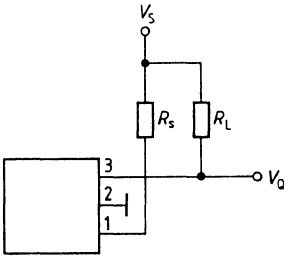


Figure 3

Application circuit



For optimum efficiency of the integrated overvoltage protection, it is suggested that a resistance R_S of approx. 100 Ω be provided in the component's power supply to limit the current.

Figure 4

Pulse diagram

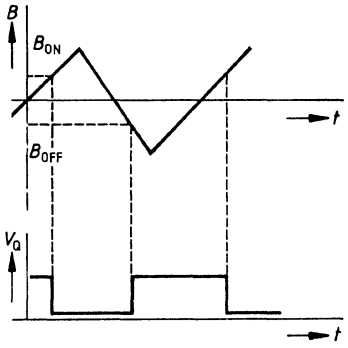


Figure 5

Preliminary Data **DIP 18**

The TUA 1574 has been designed as monolithic integrated tuner with strictly symmetrical RF parts for use in car radios and home receivers. In addition the IC provides a pre-stage control by means of narrow and wideband information and IF post amplification.

Features
- double-balanced mixer
- AGC generation
- strictly symmetrical RF parts
- Stand-by switch
- decoupled counter output

Description of function and applications

Description of functions:
The TUA 1574 has been designed as a monolithic integrated tuner with strictly symmetrical RF parts for use in car radios and home receivers. In addition the IC rovides a pre-stage control by means of narrow and wideband information and an IF post amplificication.

- double-balanced mixer
- AGC generation
- strictly symmetrical RF parts
- stand-by switch
- decoupled counter output

Description of applications:
The TUA 1574 is especially suitable for use in car radios and home receivers with pre-stage control and distributed IF selection.

Description of circuitry:
The integrated circuit includes an oscillator with symmetrical input, buffered output and a double balanced mixer for frequency conversion. The resulting IF is post-amplified in a linear IF driver. The AGC stage integrated for pre-stage control generates combined wide and narrowband information. The IC also includes a reference voltage source and a stand-by switch.

Maximum Ratings
Exceeded maximum ratings cause irreversible damage to the IC.

Pos.	Maximum rating for ambient temperature $T_{amb} = +25\,°C$	Symbol	min	max	unit
1	Supply voltage	V_{15}	−0.3	+13.5	V
2	Mixer	V_{16}, V_{17}		+25	V
3	Stand-by switch	V_{11}	−0.3	+13.5	V
4	Reference voltage	V_5	−0.3	+7	V
5	Currents: all pins are short-circuit protected against ground.				

Functional Range

Within the functional range, the IC operates as described; deviations from the characteristic data are possible.

Pos.	functional range	Symbol	min	max	unit
1	Supply voltage	V_{15}	7	12	V
2	Ambient temperature	T_{amb}	− 25	85	°C

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not stated otherwise, typical characteristics will apply at t_{amb} = 25°C and V_S 8.5V.

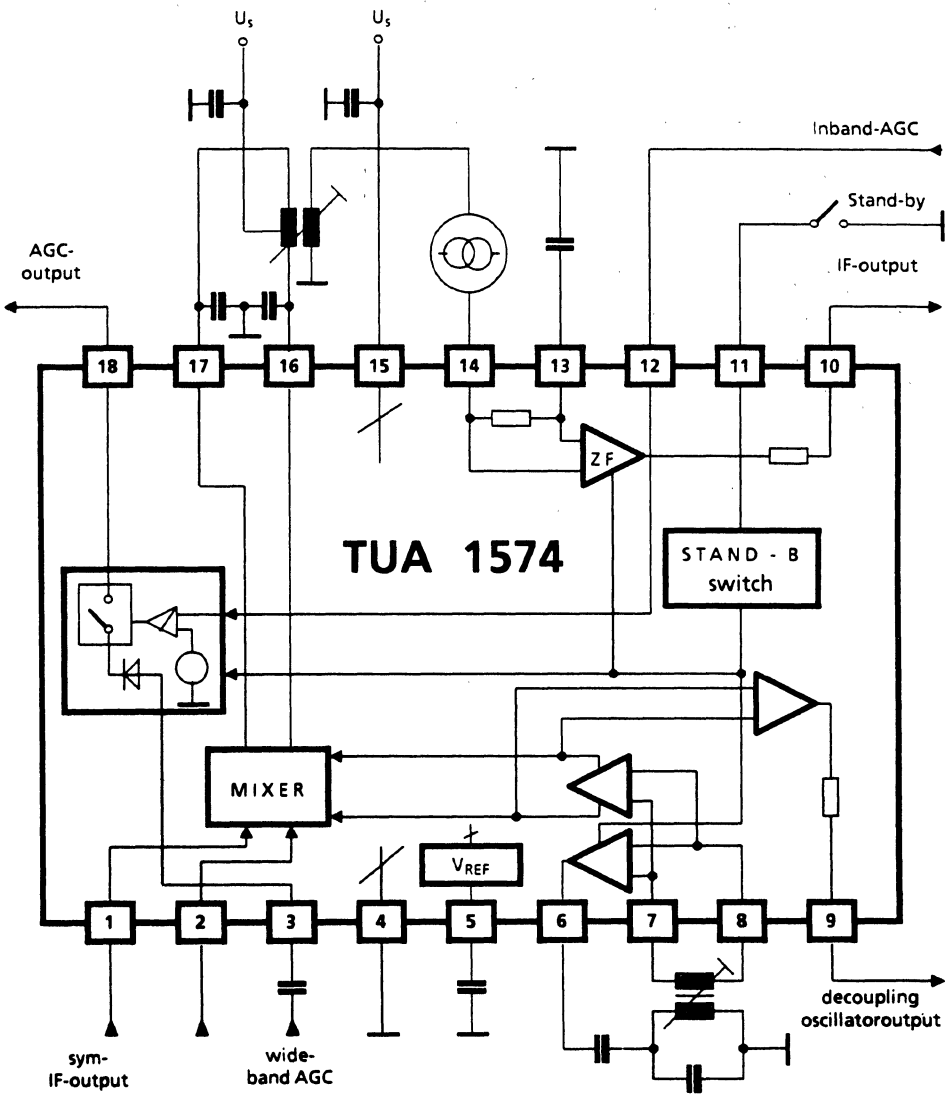
Pos.	Parameter	Symbol	Measurement circuit	Min	Typ	Max	Unit
1	Current Consumption (without mixer)	I_{15}		14	23	28	mA
2	Reference voltage				4.2		V
Mixer							
3	Third order	I_{P3}			115		dB/µV
4	Noise figure	F			11		dB
5	Mixer gain	V			14		dB
Oscillator							
6	DC characteristics	V_7, V_8			1.3		V
7	DC characteristics	U_6			2		V
8	Interference	Δf			2.2		Hz
9	Output signal 75Ω			25		MV_{eff}	
10	Output signal open	V_9			110	mV_{eff}	
11	Output impedance	R_9			2.9		kΩ
Control voltage generation							
12	Control voltage for prestage	V_{18}	0.5		(VP - 0.3)	0.3	V
13	Output current (V_3 = 0 or V_{12} = 550V and V_{18} = $V_{P/2}$)	$-I_{18}$			50		µA
14	Output current (V_3 = 2V and V_{12} = 1V)	I_{18}			2...5	mA	
15	Narrowband-control threshold when V_3 = 2V)	V_{12}			500		mV

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not stated otherwise, typical characteristics will apply at $t_{amb}=25°C$ and V_S≙8.5V.

Pos.	Parameter	Symbol	Measurement circuit	Min	Typ	Max	Unit
16	Wideband control threshold when $V_{12}=0.7V$		$V_{IHF\ EMK2}$		19		mV
Linear IF amplifier							
17	Input DC voltage	$V_{13,14}$			1.2		V
18	Output DC voltage	V_{10}			3.5		V
19	Input resistance	$R_{I\ 13}$			300		Ω
20	Input capacitance	$C_{I\ 13}$			13		pF
21	Output impedance	R_{10}			300		Ω
22	Output capacitance	C_{10}			3		pF
23	Voltage gain	G_V			30		dB
24	Noise figure at $R_S=300Ω$	F			6.5		dB
25	Reference voltage	V_5			4.2		V
26	Stand-by	V_{11}			3.3...VS		V

Block diagram



Pin functions

Pin 1/2: *RF input for mixer:*
low impedance (basic circuitry) input directly to the mixer pair.

Pin 3: *Input for wideband information:*
RF signal is present after pre-stage selection. Strong adjacent channel transmitter activates control.

Pin 4: *Ground:*
Decoupling should be referenced to this pin.

Pin 5: *Reference voltage:*
To be decouple to pin 4.

Pin 6/7/8: *Oscillator:*
3 point oscillator with low levels especially for tuning vector diodes.

Pin 9: *Decoupled oscillator output:*
Buffered output specially designed for synthesizer.

Pin 10: *Output IR driver:*
Output with 300Ω corresponding to impedance of conventional IF ceramic filters.

Pin 11: *Stand-by switch:*
The tuner is activated when this pin is tied to ground.

Pin 12: *Input for narrowband information:*
Field strength information of inband signal is forwarded to this pin for use in pre-stage control.

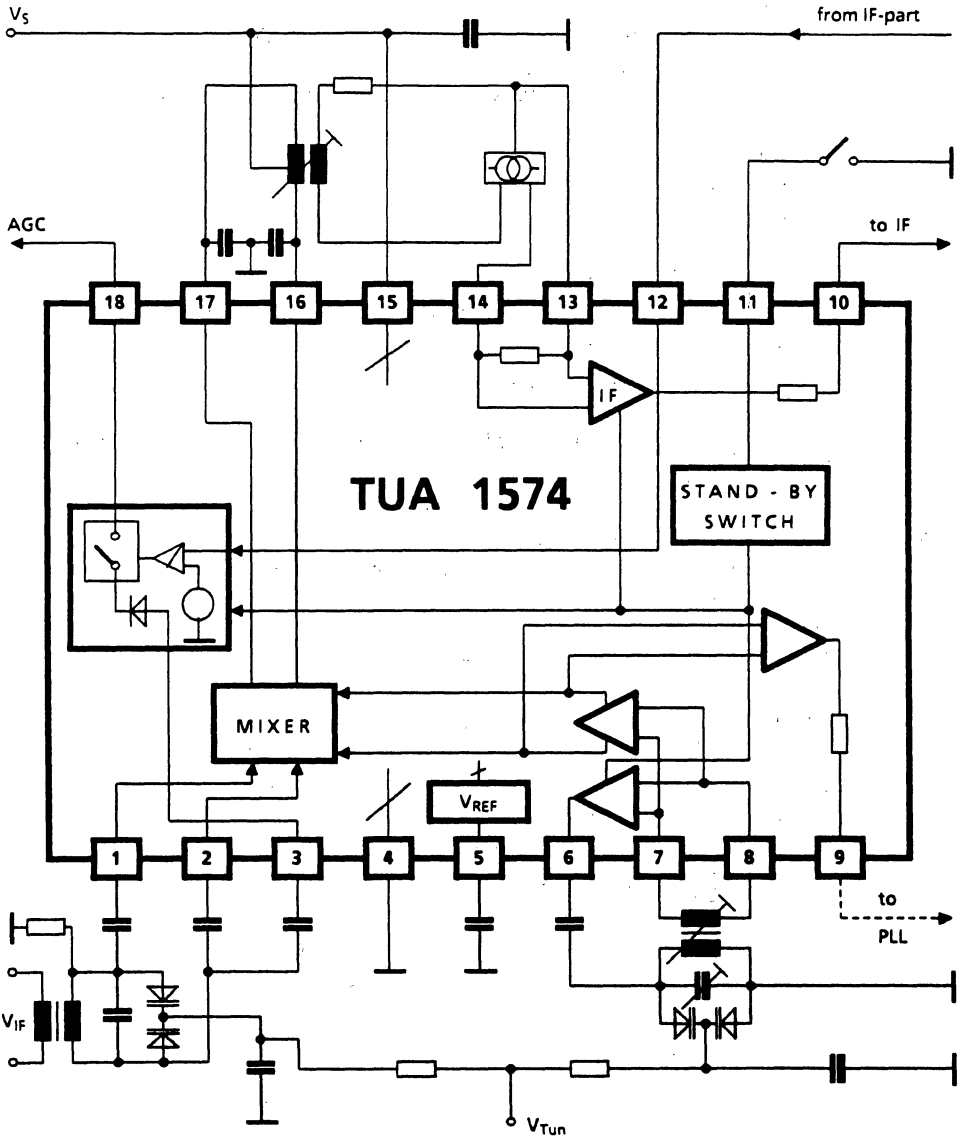
Pin 13/14: *IF driver input:*
IF signal is forwarded to mixer via selection.

Pin 15: *Supply voltage:*
Pin should be RF decoupled against pin 4.

Pin 16/17: *Mixer output:*
Symmetrical open collector output.

Pin 18: *C output:*
Output can be used as current output (pin diodes)
or as voltage output (for bipolar
and/or field effect transistors.

Application circuit



DIP 16

The TUA 2000-4 is a monolithically integrated circuit and suitable as a tuner for the VHF range up to 400 MHz, e.g. for TV tuners.

RF section

- Few external components
- Stable oscillator frequency and amplitude with very low interference radiation
- Optimal rejection of oscillator and input frequencies at the IF output due to a decoupled active ring mixer circuit
- High interference voltage resistance
- High-impedance mixer input, for symmetrical and asymmetrical connections
- IF post-amplifier for the UHF IF signal

IF section

- Optimal cross-talk rejection
- Large signal-modulation range
- Low noise figure with wide minimum over large load-impedance range

Maximum ratings

Supply voltage range $V_3 \leq V_S$	V_S	−0.3 to 16.5	V
Reference voltage $V_S \geq V_3$	V_3	−0.3 to 8.3	V
Voltage at pin 1, 2 $V_3 \leq V_{1,2}$	$V_{1,2}$	−0.3 to 16.5	V
Voltage at pin 8, 9 $V_3 \leq V_{8,9}$	$V_{8,9}$	−0.3 to 16.5	V
Voltage at pin 14 $V_{14} \leq V_S$	V_{14}	−0.3 to 16.5	V
AC voltage at pin 4, 5, 6, 11, 12, 13, 15	V_{rms}	0 to 0.5	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\ SA}$	80	K/W

Only the specified external circuitry may be applied to pins 4, 5, 6, 11, 12, 13, 15.

Operating range

Supply voltage	V_S	9 to 15	V
Reference voltage	V_3	7.2 to 8.2	V
Input frequency — mixer section	$f_{M\ 12/13}$	10 to 400	MHz
Input frequency of the UHF IF amplifier	$f_{UHF\ 11}$	10 to 400	MHz
Input frequency of the SAW amplifier	$f_{IF\ 15}$	10 to 400	MHz
Oscillator amplifier depending on the oscillator circuitry at pin 4, 5	$f_{OSC\ 4,5}$	10 to 400	MHz
Voltage at pin 1, 2, 8, 9	$V_{1,2,8,9}$	9 to 15	V
Output frequency of the mixer/UHF	$f_{IF\ M/UHF\ 8/9}$	10 to 400	MHz
Output frequency of the SAW amplifier	$f_{IF\ 1,2}$	10 to 400	MHz
Ambient temperature	T_A	0 to 70	°C

Characteristics

$V_S = 12$ V; $V_3 = 7.5$ V; $T_A = 25$ °C

		min	typ	max	
Total current consumption	$I_{10,1,2,8,9,3}$				
$I_{14} = 0$; $V_3 = 7.2$ V; $V_S = 9$ V		37	49	60	mA
$I_{14} = 0$; $V_S = 12$ V		40	52	64	mA
Current consumption at pin 3	I_3	14	19	25	mA
$I_{14} = 0$					
Output characteristic	$\Delta I_{8,9}$			100	µA
$V_{8,9} = 9$–15 V; $V_3 = 7.8$ V					
Output characteristic	$\Delta I_{1,2}$			200	µA
$V_{1,2} = 9$–15 V; $V_3 = 7.8$ V					
UHF switching voltage	$V_{14\,UHF}$	7		V_S	V
$V_{I(u)} = -25$ dBm					
$V_Q \geq -5$ dBm; $f_{IF} = 36.15$ MHz					
VHF switching voltage	$V_{14\,VHF}$	0		3	V
$V_{I(u)} = -25$ dBm					
$V_Q \leq -30$ dBm; $f_{IF} = 36.15$ MHz					
Mixer gain	G_{60}	25	27	29	dB
Bd I; $V_{I(RF)} = -40$ dBm;					
$f_{RF} = 60$ MHz; $f_{IF} = 36.15$ MHz;					
$R_{G\,12/13} = 100\ \Omega$;					
refer to response characteristic page 750					
Mixer gain	G_{220}	25	27	29	dB
Bd III; $V_{I(RF)} = -40$ dBm;					
$f_{IF} = 36.15$ MHz; $R_{G\,12/13} = 100\ \Omega$;					
refer to response characteristic page 751					
Mixer noise	NF_{60}			13	dB
Bd I, white noise					
$R_{G\,12/13} = 100\ \Omega$; refer to response characteristic page 750					
Mixer noise	NF_{220}			14	dB
Bd III; white noise					
$R_{G\,12/13} = 100\ \Omega$; refer to response characteristic page 751					
Gain UHF input	V_{UHF}	31	33	35	dB
$V_{I(u)} = -40$ dBm; $V_{14} = V_S = 12$ V					
$f_{RFU} = f_{IF} = 36.15$ MHz;					
$R_{G\,11} = 200\ \Omega$; refer to response characteristic page 751					
Noise figure UHF input	NF_{UHF}			7	dB
$V_{14} = V_S = 12$ V; white noise					
$R_{G\,11} = 200\ \Omega$; refer to response characteristic page 751					
Oscillator turn-on drift	f_{OSC}	−10		−250	kHz
$V_D = 28$ V; $t = 0$–500 ms;					
Bd II; $f_{OSC} = 216$ MHz					
Oscillator turn-on drift	f_{OSC}	−10		−450	kHz
$V_D = 28$ V; $t = 0$–10 s;					
Bd II; $f_{OSC} = 216$ MHz					

		min	typ	max	
Additional application data					
Differential input resistance[1]	$R_{12/13}$		3		kΩ
Differential input capacitance[1]	$C_{12/13}$		2.7		pF
IF input resistance[1]	R_{15}		2		kΩ
IF input capacitance[1]	C_{15}		3.9		pF
UHF input resistance[1]	R_{11}		2.2		kΩ
UHF input capacitance[1]	C_{11}		3.4		pF
Interference voltage resistance Bd I[2] $m_N = 1\%$; $m_{int} = 80\%$; $f_{int} = f_N \pm 15$ MHz $f_{mod} = 1$ kHz; $f_N = 65$ MHz refer to response characteristic	$V_{int\,(EMF/2)\,rms}$		38		mV
Interference voltage resistance Bd II[2] $m_N = 1\%$; $m_{int} = 80\%$; $f_{int} = f_N \pm 15$ MHz $f_{mod} = 1$ kHz; $f_N = 220$ MHz refer to response characteristic	$V_{int\,(EMF/2)\,rms}$		30		mV

Note on characteristics

Due to quasi no-load of the transformer output and 2x50 Ω source impedance, the interference voltage at pins 12/13 is calculated by

$$V_{int\,12/13} \approx V_{int\,(source/2)} \times 2 \times \sqrt{2}$$

[1] Measured S parameter values converted to Y parameters

[2] See: Measurement configuration to measure cross modulation

Circuit description

The TUA 2000-4 contains a symmetrical mixer input, as well as a multiplicative mixer. The oscillator amplitude is regulated. All oscillator operating currents and voltages are stabilized, so that the oscillator's amplitude and frequency are largely independent of temperature and operating voltage changes.

The IF amplifier has been provided with a high impedance input.

The output has two open collector connections.

During UHF operation, oscillator and mixer are switched off and the UHF IF input coupling stage is activated.

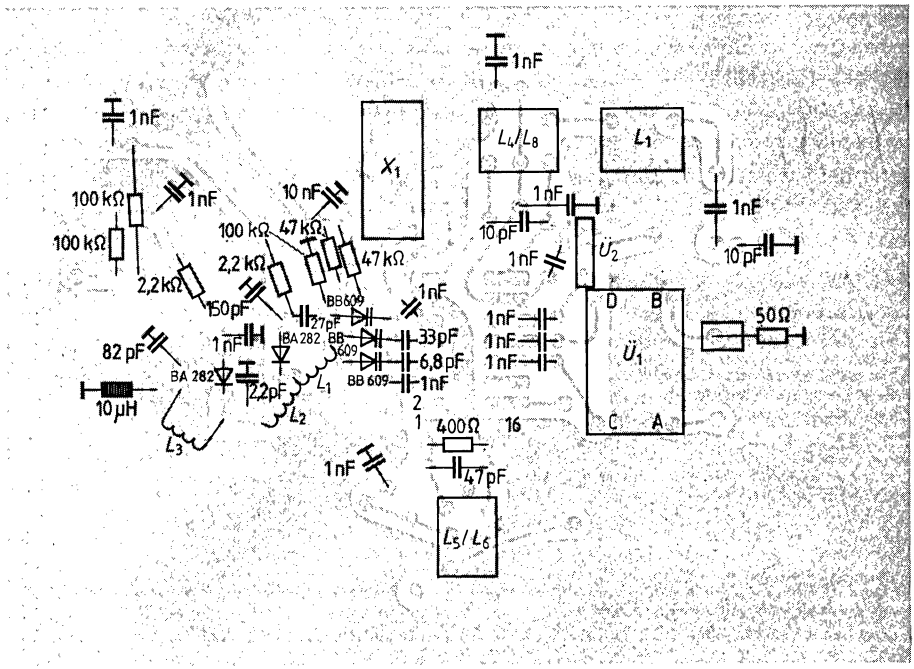
RF section

- Few external components
- Stable oscillator frequency and amplitude with very low interference radiation
- Optimal rejection of oscillator and input frequencies at the IF output due to a decoupled active ring mixer circuit
- High interference voltage resistance
- High-impedance mixer input, for symmetrical and asymmetrical connections
- IF post-amplifier for the UHF IF signal

IF section

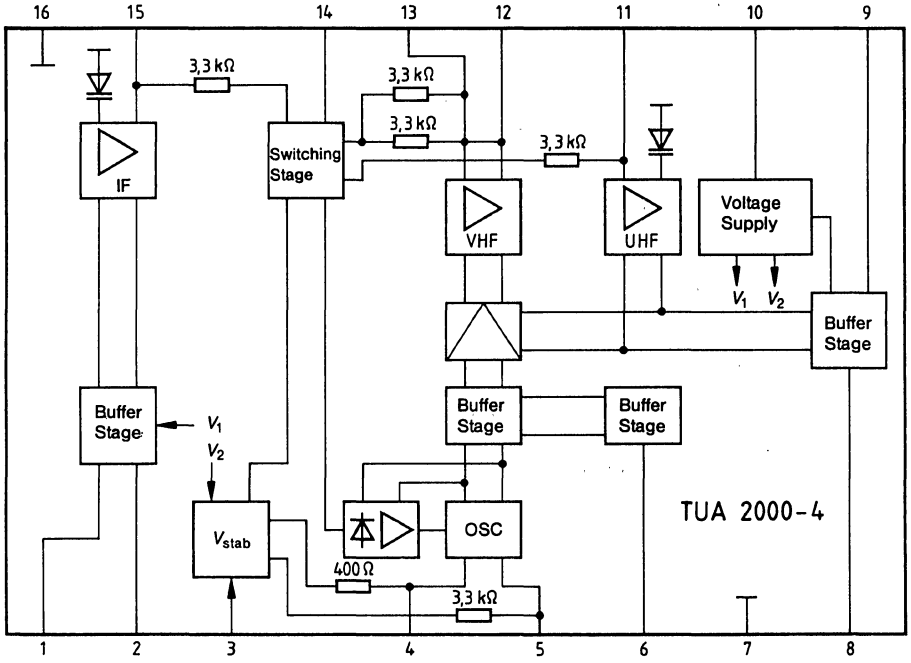
- Optimal cross-talk rejection
- Large signal-modulation range
- Low noise figure with wide minimum over large load-impedance range

Plug-in location plan



PCB layout of test and measurement circuit 1

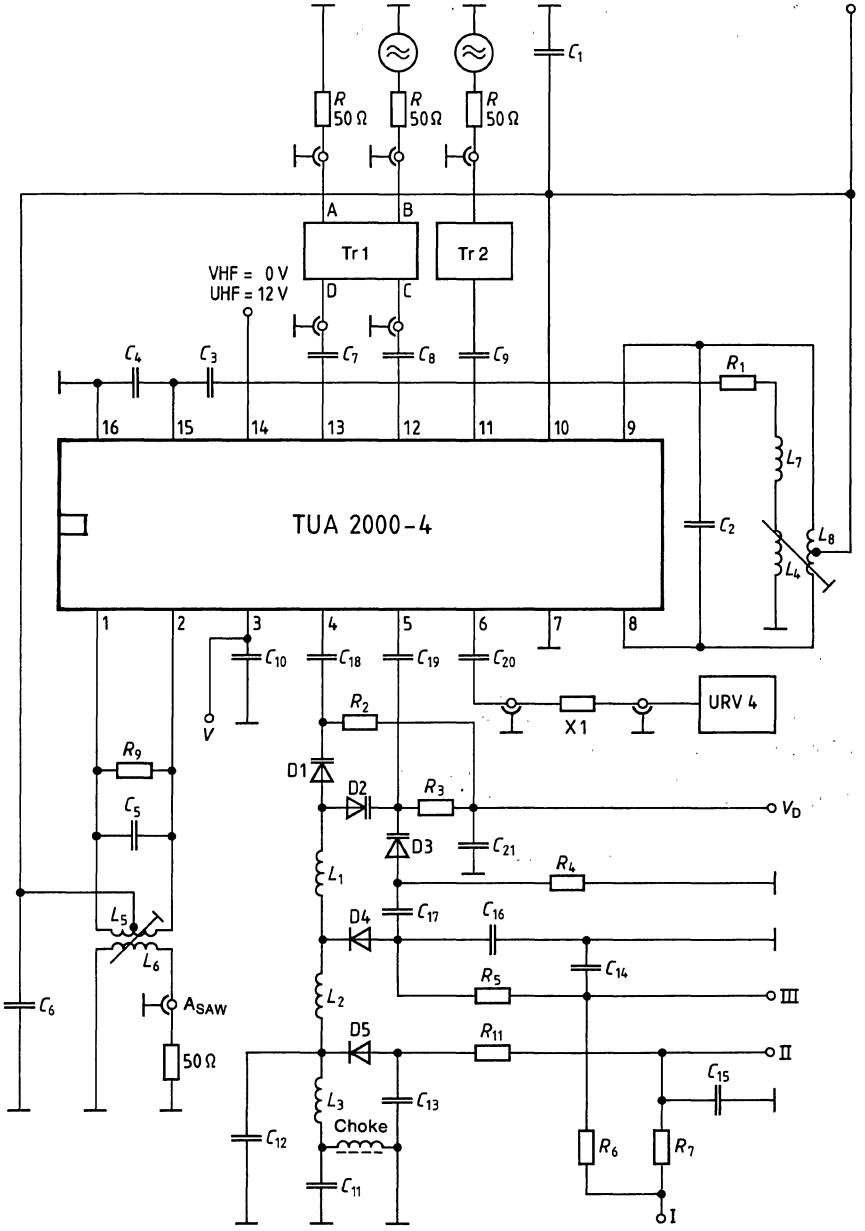
Block diagram



Pin description

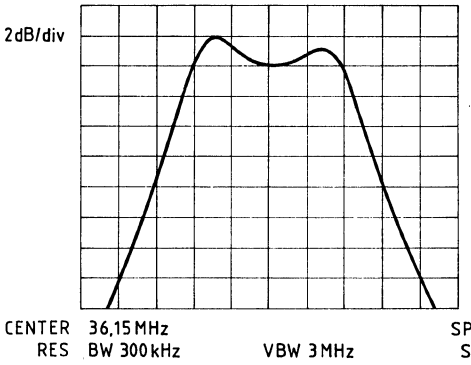
Pin	Function
1	"Open collector" output of the IF SAW driver
2	"Open collector" output of the IF SAW driver
3	Input for external reference voltage
4	Low-ohmic collector output to the high reference point of a parallel resonant circuit
5	High-ohmic base input to the high reference point of a parallel resonant circuit
6	Oscillator signal output for counter connection
7	GND
8	"Open collector" output of the mixer
9	"Open collector" output of the mixer
10	Supply voltage
11	Asymmetrical IF signal input for the UHF IF signal
12	Mixer high-impedance differential input
13	Mixer high-impedance differential input
14	Switching voltage input for the VHF-UHF switch selection
15	Asymmetrical signal input of the IF SAW amplifier
16	GND

Test and measurement circuit 1



Notes on test and measurement circuit 1

Response of passband curve for operation in VHF band I
f_{RF} = 60 MHz ± 10 MHz; V_{14} = 0 V; $V_{I\,(REF)}$ = −40 dBm; ref. level = −10 dBm
gain test point f_{RF} = 60 MHz; f_{IF} = 36.15 MHz

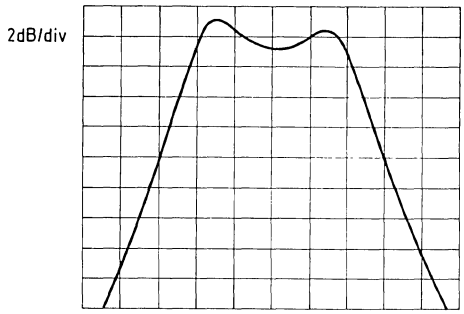


Explanations to diagrams

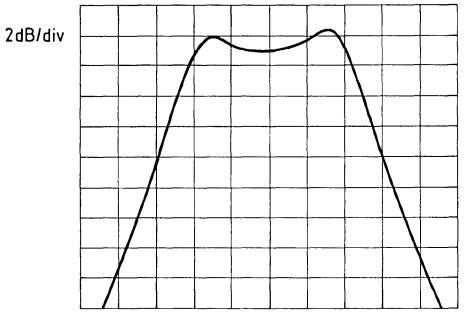
2 dB/div	= 2 dB/division of Y axis
Center 36.15 MHz	= center frequency of display at IF = 36.15 MHz
RES BW 300 kHz	= resolution bandwidth of spectrum analyzer is 300 kHz in its IF section
VBW 3 MHz	= video bandwidth in IF section of spectrum analyzer is 3 MHz
SPAN 20.00 MHz	= overall display range of diagram is 20 MHz, i.e. 2 MHz/division on X axis
SWP 75	= sweep time on X axis is 75 s
Ref. level	= reference level is top horizontal line of diagram

Notes on test and measurement circuit 1

Response of passband curve for operation in VHF band III
f_{RF} = 220 MHz ±10 MHz; V_{14} = 0 V; $V_{I\,(RF)}$ = −40 dBm; ref. level = −10 dBm
gain test point f_{RF} = 220 MHz; f_{IF} = 36.15 MHz



Response of passband curve for operation in VHF IF position
f_{RFU} = 36.15 MHz ±10 MHz; V_{14} = 12 V; $V_{I\,(RF)}$ = −40 dBm; ref. level = 0 dBm
gain test point $f_{RFU} = f_{IF}$ = 36.15 MHz



Notes on test and measurement circuit 1

Between pin 4 – C18 – D1 – D2 – C19 – pin 5 ensure minimal lead inductance for the suppression of parasitic series resonance outside the oscillator's useful band.

Transformer Tr 1:

Tr 1 = anzac = HH-109 30 to 500 MHz
C = 0°; R_{gC} = 50 Ω
D = 180°; R_{gD} = 50 Ω

Transformer Tr 2:

50/200 Ω unbalanced
3 turns bifilar on core material
B62152-A7-X1

Attenuator: X1 = 6 dB

Bd I 58 to 85 MHz
Bd II 110 to 216 MHz
Bd III 200 to 400 MHz

	I	II	III
Band I	−12 V	X	X
Band II	−12 V	+12 V	X
Band III	−12 V	+12 V	+12 V

Notes on test and measurement circuit 1

Part list

Resistors:

R_1 – 10 Ω
R_2 – 47 kΩ
R_3 – 47 kΩ
R_4 – 10 kΩ
R_5 – 2.2 kΩ
R_6 – 100 kΩ
R_7 – 100 kΩ
R_8 – 100 kΩ
R_9 – 400 Ω
R_{11} – 2.2 kΩ

Capacitors:

C_1 – 1 nF Chip capacitor
C_2 – 15 pF STYROFLEX
C_3 – 1 nF STYROFLEX
C_4 – 10 pF STYROFLEX
C_5 – 47 pF STYROFLEX
C_6 – 1 nF Chip capacitor
C_7 – 1 nF Chip capacitor
C_8 – 1 nF Chip capacitor
C_9 – 1 nF Chip capacitor
C_{10} – 10 nF Chip capacitor
C_{11} – 82 pF Chip capacitor
C_{12} – 2.2 pF Chip capacitor
C_{13} – 1 nF Chip capacitor
C_{14} – 1 nF Chip capacitor
C_{15} – 1 nF Chip capacitor
C_{16} – 150 pF Chip capacitor (Trapezoidal cap.)
C_{17} – 27 pF Chip capacitor (Chip capacitor)
C_{18} – 6.8 pF Chip capacitor (Chip capacitor)
C_{19} – 33 pF Chip capacitor (Chip capacitor)
C_{20} – 1 nF Chip capacitor
C_{21} – 10 nF Chip capacitor

Diodes:

D1 – BB 505 G
D2 – BB 609
D3 – BB 609
D4 – BA 282
D5 – BA 282
D6 – BZX 97 C 75 V

IC:

TUA 2000-4

Coils:

L_1 – 4 turns; core Ø 2 mm; wire Ø 0.5 mm; CuL
L_3 – 5 turns; core Ø 4 mm; wire Ø 0.5 mm; CuL
L_3 – 9 turns; core Ø 4 mm; wire Ø 0.5 mm; CuL
L_1, L_2, L_3 – air-core coils
L_4 – 2.5 turns; CuLs wire Ø 0.25 mm
L_8 – 2*6 turns; CuLs wire Ø 0.25 mm
L_7 – 15 turns; CuLs wire Ø 0.25 mm
L_5 – 2*4.5 turns; CuLs wire 0.25 mm
L_6 – 3 turns; CuLs wire Ø 0.25 mm
Coil formers of L_4/L_8, L_7, L_5/L_6
Vogt filter set 10*12
51405000 00
Catalog p. 41-8

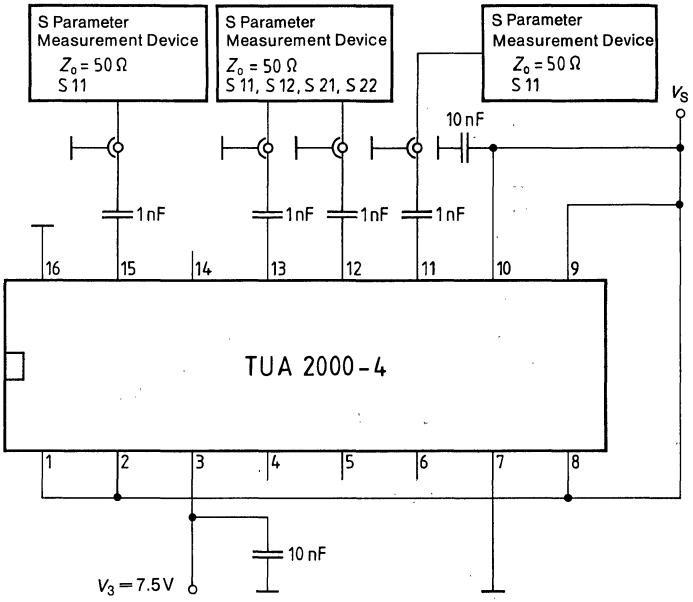
Chokes:

Ch – 10 µH

Please note that the chip capacitors may be damaged if the board is subjected to mechanical stress; thus overall functioning can no longer be guaranteed.

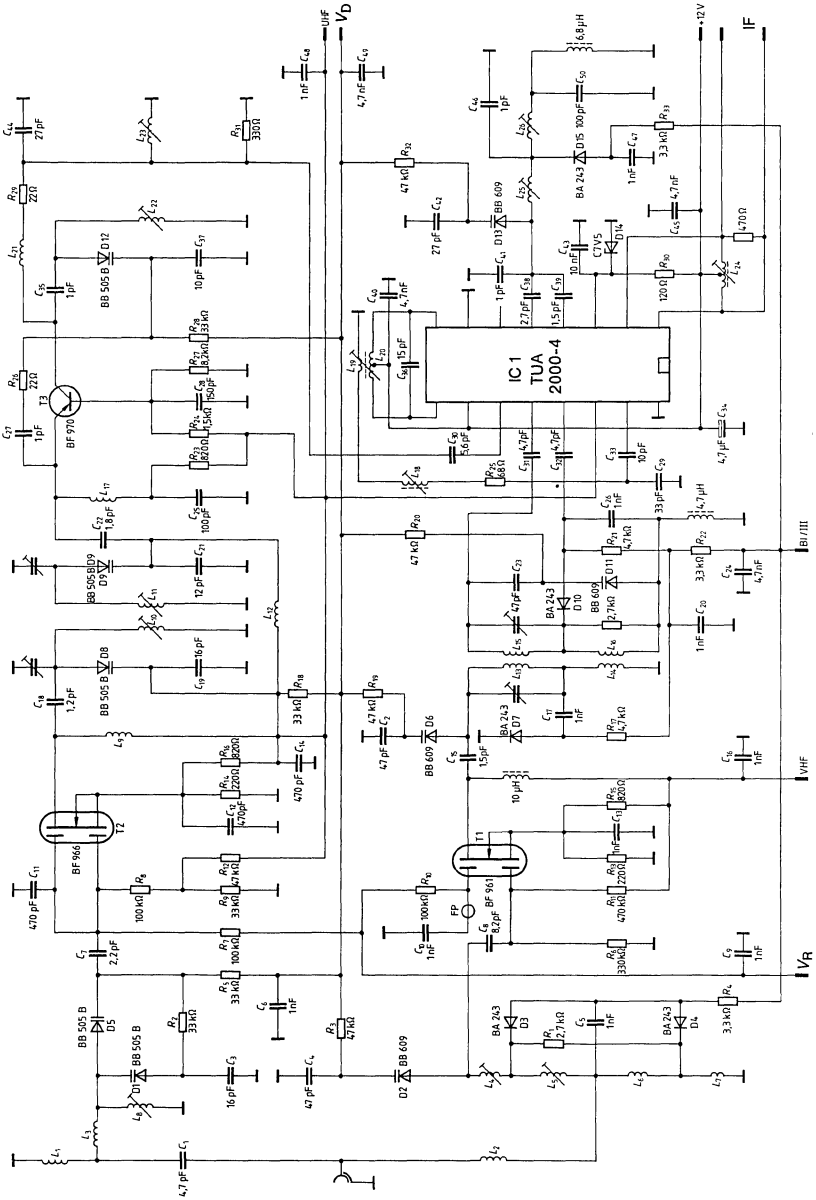
During the operating mode the PC board is adjusted without the socket. When the socket is inserted in the socket connector, the parameters for the oscillator frequency and amplitude as well as gain and noise will change.

Test and measurement circuit 2

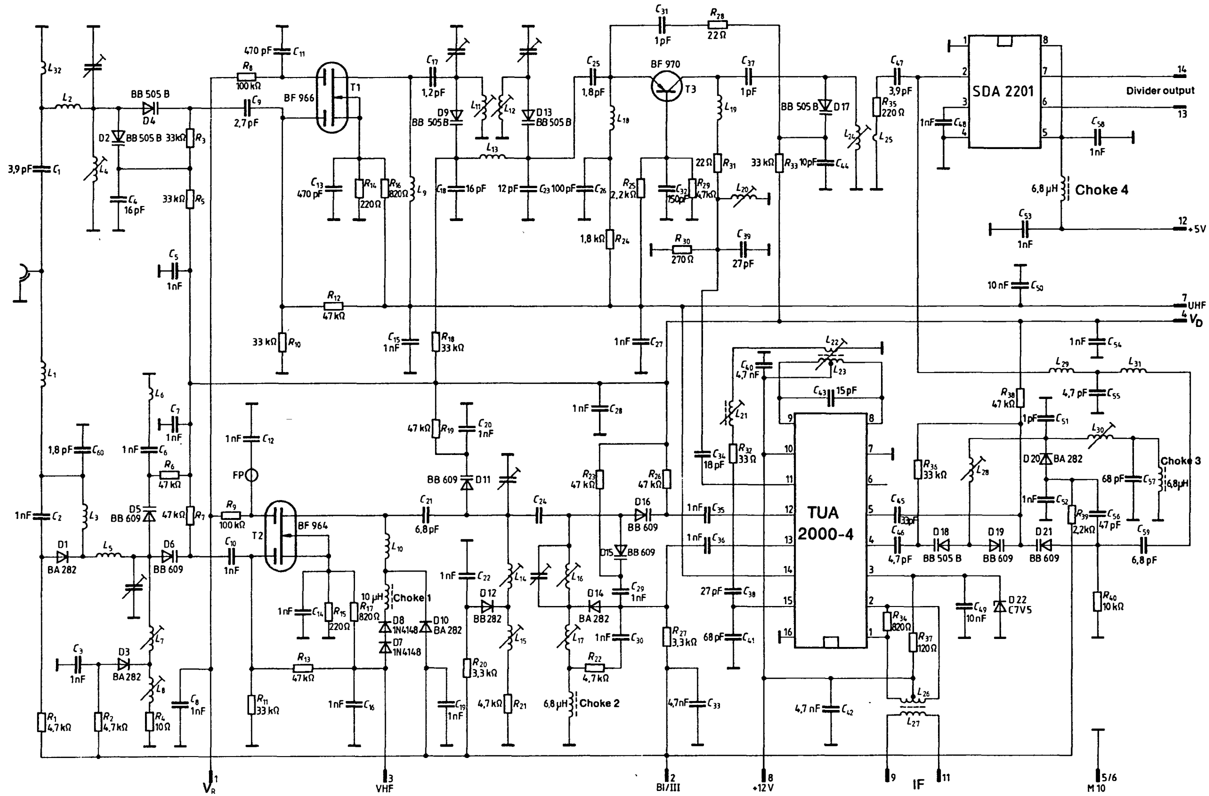


For the determination of the input admittance values of pins 11, 12, 13, 15

Application circuit 1

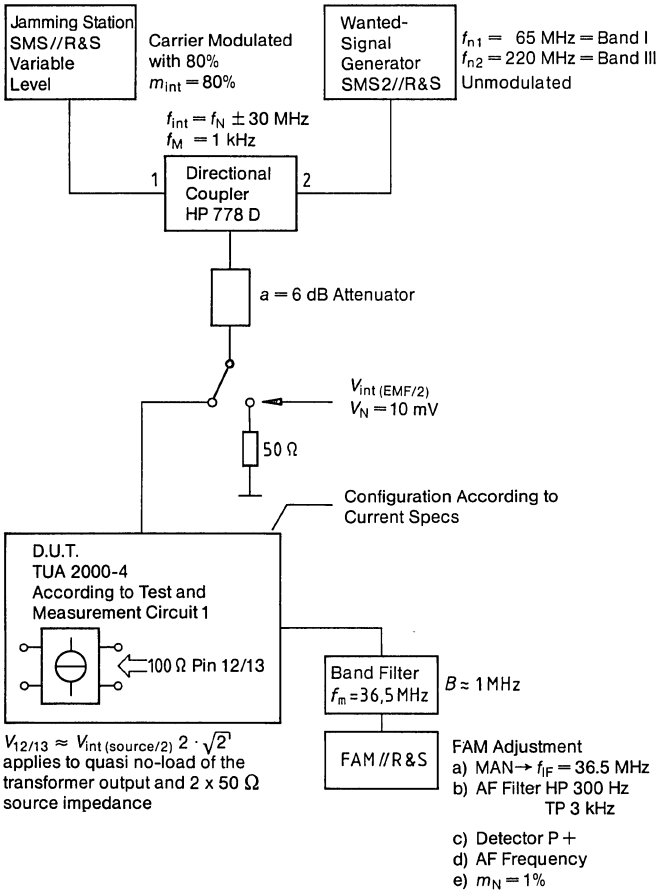


Application circuit 2



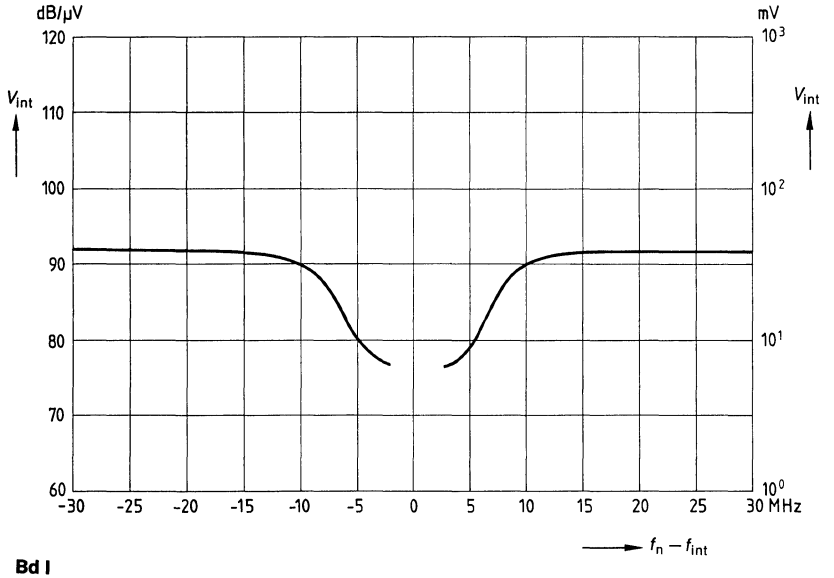
Test and measurement circuit 3

Measurement configuration to measure cross modulation

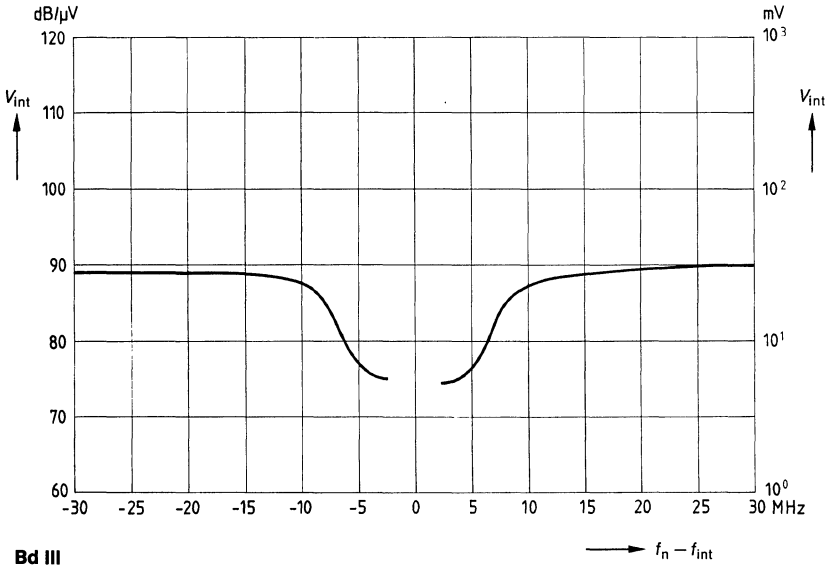


$V_{12/13} \approx V_{int\ (source/2)}\ 2 \cdot \sqrt{2}$
applies to quasi no-load of the transformer output and 2 x 50 Ω source impedance

Interference voltage for 1% cross modulation
V_{int} = EMF/2; m_{int} = 80%



Bd I



Bd III

Television Tuner for Frequency Ranges up to 700 MHz

TUA 2005

Preliminary data **DIP 16**

The TUA 2005 has been designed as monolithically integrated circuit suitable as TV tuner for a CATV frequency range extended to 700 MHz.

RF section

- Few external components
- Frequency and amplitude-stable oscillator
- Optimal suppression of oscillator and input frequency at IF output
- High resistance to interference voltages
- High-impedance symmetrical mixer input
- IF post-amplifier for UHF IF signal
- Symmetrical mixer output
- Low-noise, internal reference voltage

IF SAW driver section

- Optimal cross-talk rejection
- High-impedance, asymmetrical input with high signal modulation capability
- Low-impedance symmetrical output for driving SAW filters

Circuit description

RF section

The integrated circuit includes a symmetrical high-impedance, low-noise mixer input and a multiplicative mixer.

The amplitude of the oscillator is controlled for maintaining suitable resonant circuit voltages of the oscillator circuit. All operating currents and voltages of the oscillator are internally stabilized. The amplitude and the frequency of the oscillator are therefore largely independent of changes in temperature or operating voltages.

During UHF operation the oscillator and the mixer are disabled and the asymmetrical, low-noise UHF IF coupling stage is activated.

IF SAW driver section

The IF SAW driver includes a high-impedance, asymmetrical input. The low-impedance symmetrical output of the IF SAW driver has two open collectors. The basic volume and the output resistance can be further reduced by an ohmic symmetrical load resistor. When the operating voltage is not connected to the collectors, the current consumption of the IF SAW driver section is zero. The signal modulation capability of the IC depends on the connected supply voltage.

Maximum ratings

		min	max		Remarks
Supply voltage	V_S	−0.3	14	V	
Current from pin 15	$-I_{15}$	0	2	mA	V_S = 10 to 13.5 V
Voltage at pin 1	V_1	−0.3	V_S	V	V_S = 10 to 13.5 V
Voltage at pin 2	V_2	−0.3	V_S	V	V_S = 10 to 13.5 V
Voltage at pin 8	V_8	V_{14}	V_S	V	V_S = 10 to 13.5 V
Voltage at pin 9	V_9	V_{14}	V_S	V	V_S = 10 to 13.5 V
Voltage at pin 10	V_{10}	−0.3	V_S	V	V_S = 10 to 13.5 V
Capacitance at pin 15	C_{15}	0	100	nF	
Capacitance at pin 7	C_3	0	1	µF	

Only the specified external components can be connected to pins 4, 5, 6, 11, 12, 13, 16.

Junction temperature	T_j		150	°C
Storage temperature range	T_{stg}	−40	125	°C
Thermal resistance (system-air)	R_{thSA}		80	K/W

Operating range

Supply voltage	V_S	10	13.5	V
Mixer input frequency	f_M	20	650	MHz
UHF IF input frequency	f_{UHF}	20	650	MHz
Mixer IF output frequency	f_{MIF}	20	650	MHz
Oscillator frequency	f_{OSC}	20	700	MHz
Voltage at pin 8, 9	$V_{8,9}$	V_{14}	V_S	V
Voltage at pin 1, 2	$V_{1,2}$	5	V_S	V
Ambient temperature	T_A	0	70	°C

Characteristics

$V_S = 12$ V, $T_A = 25$ °C

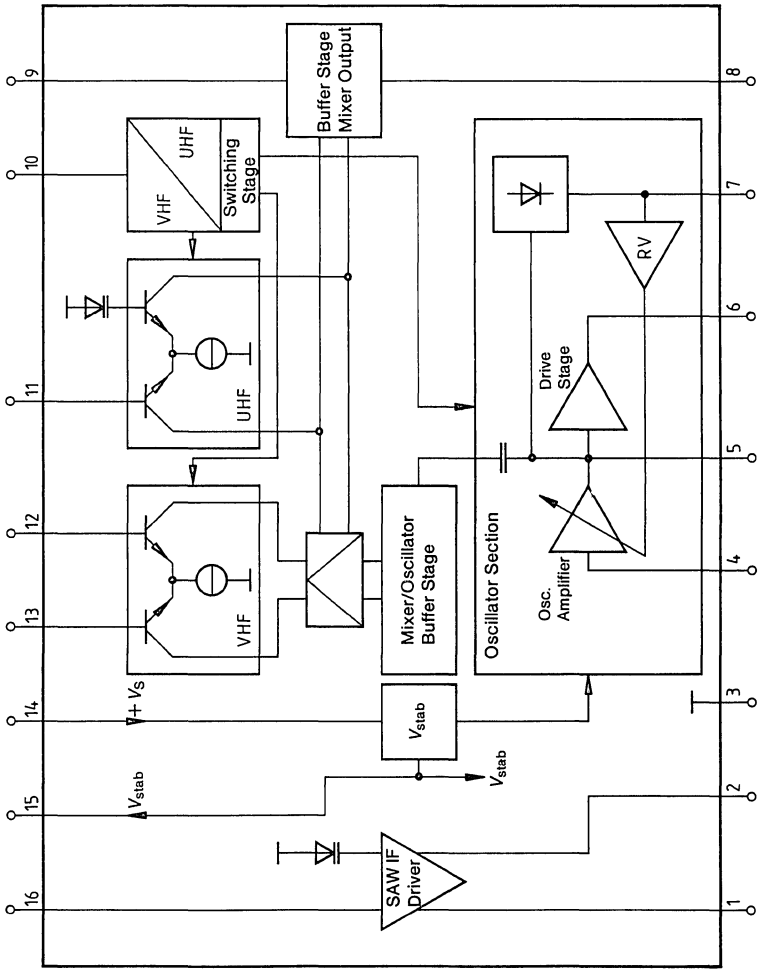
		Test conditions	Test circuit	min	typ	max	
RF section							
Current consumption	I_{14}	$I_{15} = 0$ mA; $V_{10} = V_S$	1	18	28	37	mA
Reference voltage	V_{15}	$0 \leq I_{15} \leq 1$ mA	1	7.5	8	8.5	V
Oscillator frequency range	f_{OSC}	ext. circuitry tuned to frequency		48		700	MHz
Turn-on start-up drift	Δf_{OSC}	*TC* value of cap. in osc. circuit is 0; drift is only referenced to self-heating of component. $t = 0.5$ to 10 s channel S20	1	0	−100	−500	kHz
Frequency drift versus V_S	$-\Delta f_{OSC}$	$V_S = 10$ to 13.5 V S20	1	−250		250	kHz
UHF switching voltage	V_{10}	$V_{I(U)} = -25$ dBm; $V_Q \geq -5$ dBm;	1	7		V_S	V
VHF switching voltage	V_{10}	$V_{I(U)} = -25$ dBm; $V_Q \leq -30$ dBm;	1	0		3	V
Output impedance	Z_8; Z_9	static	7	10			kΩ
Output capacitance	$C_8 = C_9$		6	0.5	1	2.0	pF
RF output phase	$\alpha_{8,9}$			140	180	220	degree
Mixer gain	G_3	channel 3; $R_G = 100\ \Omega$	1	25	27	29	dB
Mixer gain		channel 9; $R_G = 100\ \Omega$ $f = 294\ 25$ MHz					
Mixer gain	G_{S20}	channel S20; $R_G = 100\ \Omega$ $f = 294.25$ MHz	1	25	27	29	dB
Mixer gain	G_{21} Wt21	channel Wt21; $R_G = 100\ \Omega$ $f = 421.25$ MHz	1	25	27	29	dB
UHF IF gain	UHF	$R_G = 200\ \Omega$; $f_{IF} = 36.5$ MHz	1	31	33	35	dB
Mixer noise figure	NF_9	channel 9; $R_G = 100\ \Omega$ $f = 203.25$ MHz					
Mixer noise figure	NF_3	channel 3; $R_G = 100\ \Omega$	1			8	dB
Mixer noise figure	NF_{S20}	channel S20; $R_G = 100\ \Omega$	1			10	dB
Mixer noise figure	NF_{21}	channel 21; $R_G = 100\ \Omega$	1			14	dB
UHF IF noise figure	NF_{UHF}	$R_G = 200\ \Omega$	1			7	dB
Oscillator output signal for PLL or frequency divider	V_6	$R_L = 200\ \Omega$; channel 3 S20	1	−27		−17	dBm

Characteristics

$V_S = 12$ V, $T_A = 25$ °C

		Test conditions	Test circuit	min	typ	max	
SAW IF driver							
Current consumption	$I_1 + I_2$	$V_S = 12$ V		17	22	28	mA
Input impedance	Z_{16}	S-parameter measurement	2		3		kΩ
Input capacitance	C_{16}	S-parameter measurement	2		1.5		pF
Symmetrical output resistance	$\lvert Z_{1/2} \rvert$	S-parameter measurement	5	50	100	200	Ω
Linearity (permissible input signal)	V_{16}	$m_s = 80\%$; $f_S = 36.5$ MHz total harmonic distortion of output signal V_Q is $THD = 1\%$	3		250		mV
Noise figure	NF	$R_G = 200$ Ω	4		10		dB
Gain	G	$R_L = R_G = 50$ Ω	3		−16		dB

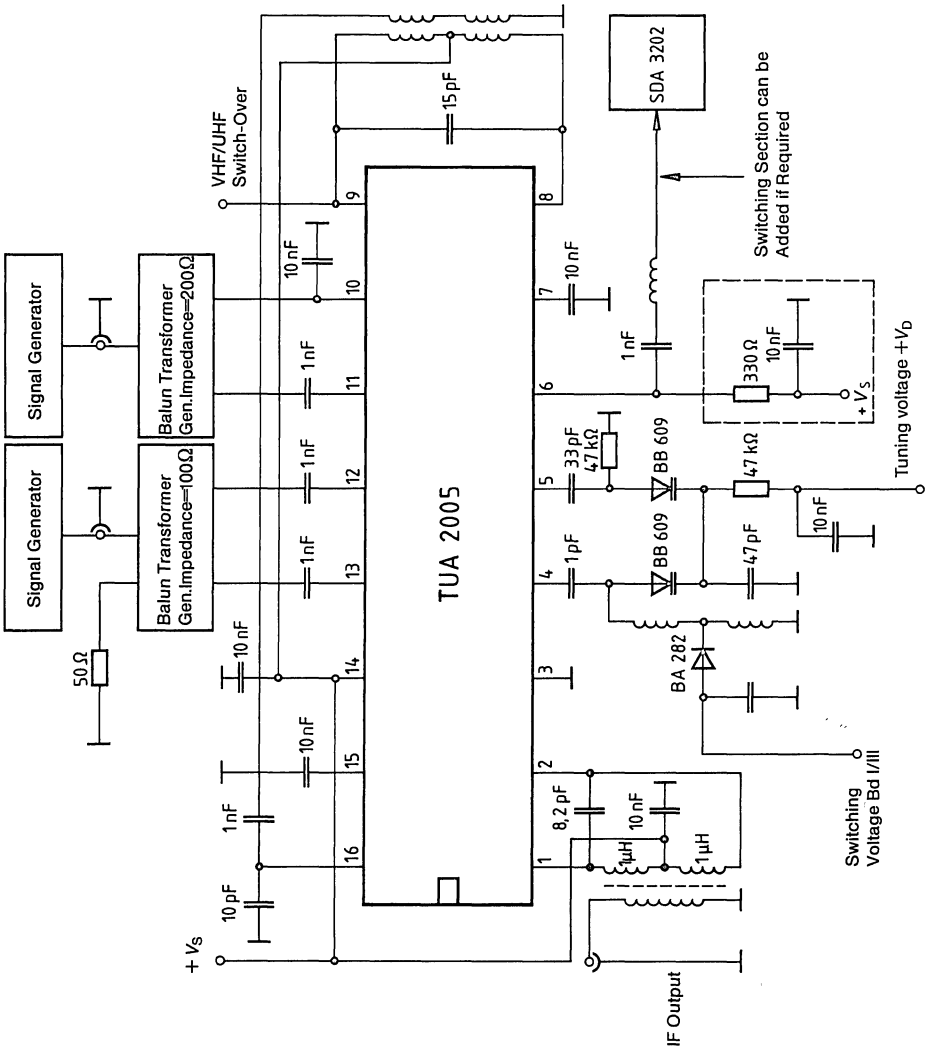
Block diagram



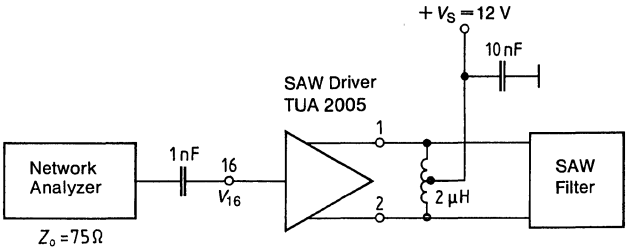
Pin description

Pin	Function
1	Low-impedance symmetrical output of SAW driver
2	Low-impedance symmetrical output of SAW driver anti-phased to pin 1
3	GND
4	High-impedance input of oscillator amplifier
5	Low-impedance output of oscillator amplifier
6	Oscillator signal output for PLL systems with possible open collector output
7	Blocking capacitor for controlling oscillator amplitude
8	Symmetrical mixer output
9	Symmetrical mixer output anti-phased to pin 8
10	Switching voltage input for VHF/UHF switch-over
11	High-impedance asymmetrical RF input for UHF IF signal
12	High-impedance symmetrical RF input of VHF mixer
13	High-impedance symmetrical RF input of VHF mixer, anti-phased to pin 12
14	Supply voltage
15	Blocking point of internal reference voltage
16	High-impedance asymmetrical IF input of SAW driver

Measurement circuit 1

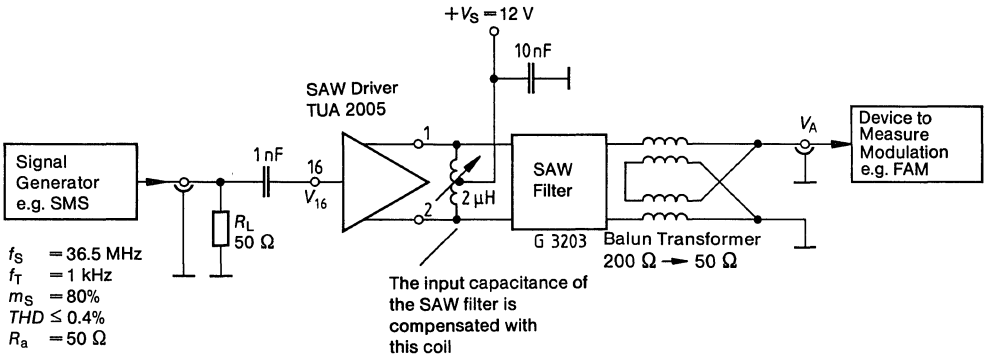


Measurement circuit 2

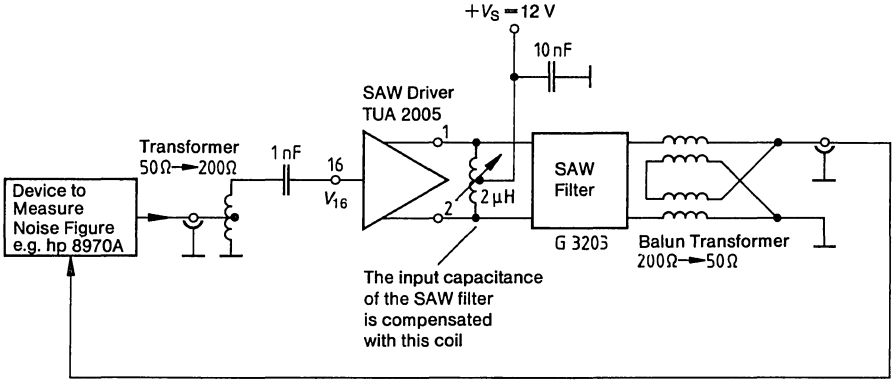


The input reflection factor S_{16} is measured at 36.5 MHz for computing the parallel equivalent circuit.

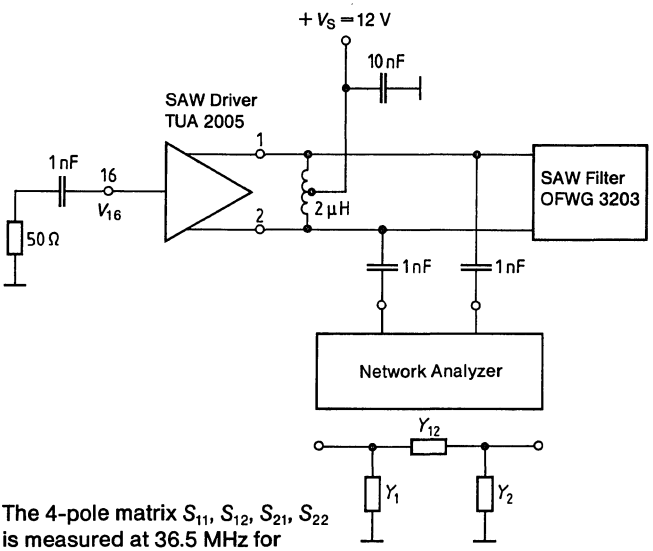
Measurement circuit 3



Measurement circuit 4

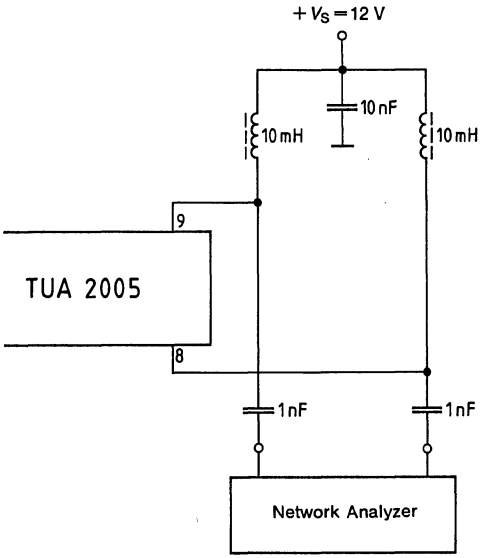


Measurement circuit 5



The 4-pole matrix S_{11}, S_{12}, S_{21}, S_{22} is measured at 36.5 MHz for computing the π equivalent circuit.

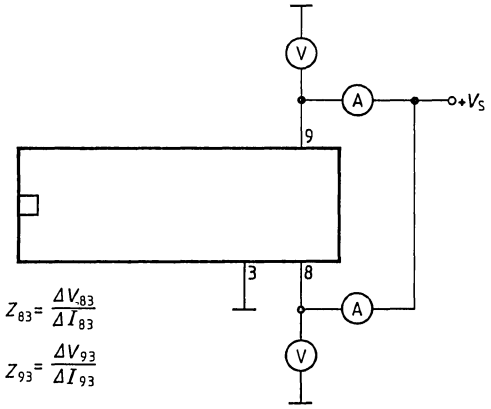
Measurement circuit 6

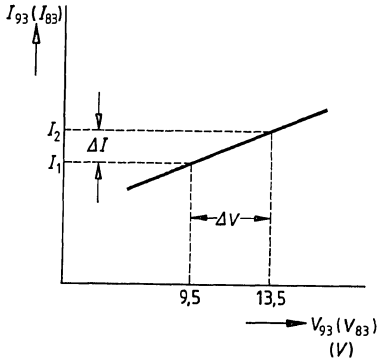


The 4-pole matrix S_{81}, S_{82}, S_{91}, S_{92} is measured at 100 MHz for computing the output capacitance.

Measurement circuit 7

Measurement of static output impedance





DIP 16

IC for driving 16 light emitting diodes. Depending on the input voltage, the individual LEDs are driven within one row in form of a light spot. The UAA 170 provides a linear relation between control voltage and the driven LED.

By using an appropriate circuitry, the brightness of the LEDs can be varied and the crossing over of the light spot can be set between "smooth" and "abrupt". By connecting two ICs in parallel, up to 30 LEDs can be driven.

Maximum ratings

Supply voltage	V_S	18	V
Input voltages	V_{11}, V_{12}, V_{13}	6	V
Load current	I_{14}	5	mA
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	90	K/W

Operating range

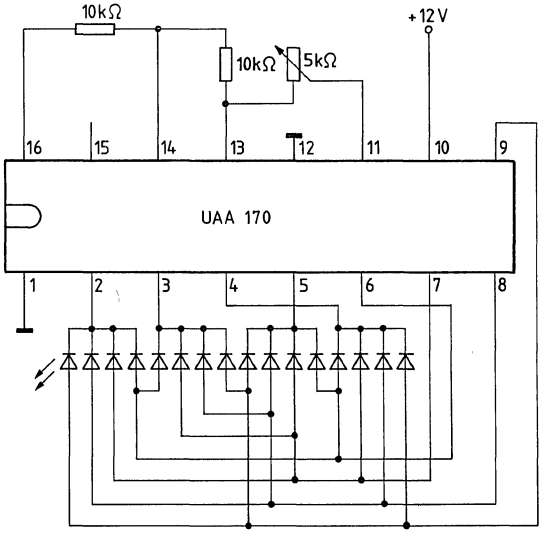
Supply voltage range (LED red)[1]	V_S	11 to 18	V
Ambient temperature range	T_{amb}	−25 to 85	°C

1) The lower limit only applies to a forward voltage of the LEDs of approx. 1.5 V (red LEDs); the lower limit increases with higher forward voltage

Characteristics ($V_S = 12$ V; $T_{amb} = 25$ °C)

		min	typ	max	
Current consumption ($I_{14} = 0$; $I_{16} = 0$)	I_S	2	4	10	mA
Control input current	I_{11}	−2			µA
Reference input current	I_{12}, I_{13}	−2			µA
Voltage difference	$\Delta V_{12/13}$	1.4		6	V
Voltage difference for smooth light transition	$\Delta V_{12/13}$	1.4			V
Voltage difference for abrupt light transition	$\Delta V_{12/13}$	4			V
Voltage difference	$\Delta V_{12/13}$	4			V
Stabilized voltage $I_{14} = 300$ µA	V_{14}		5	6	V
$I_{14} = 5$ mA	V_{14}	4.5			V
Reference input voltage	$V_{ref\,max}$	1.4		6	V
	$V_{ref\,min}$	0		4.6	V
Tolerance of forward voltages of LEDs, mutually	ΔV_D			0.5	V
Output current for LEDs	ΣI_D		25		mA

Test circuit



Scale display with light emitting diodes

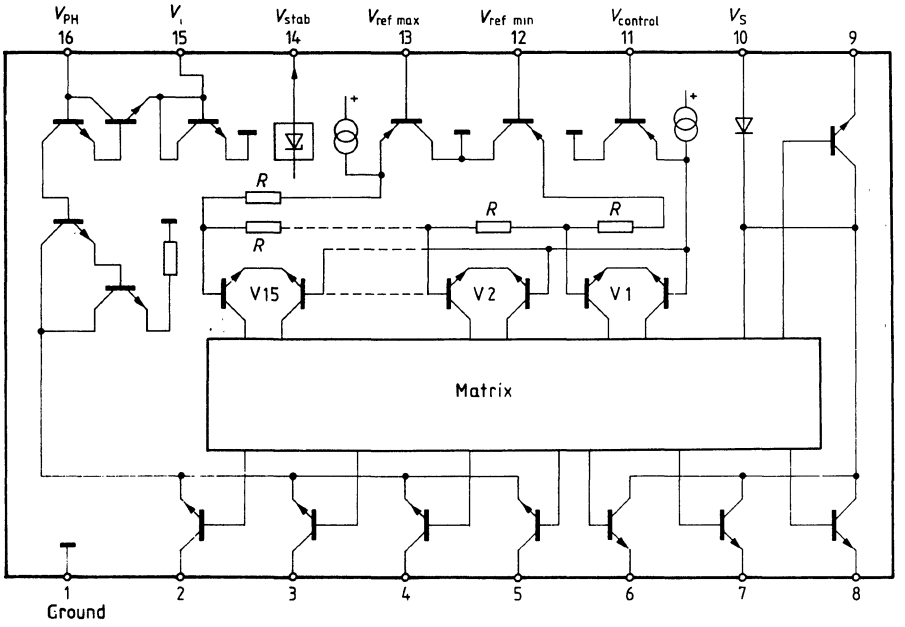
Scale displays by means of a wandering light spot are particularly suitable for indicating approximate values. Applications of this kind are level sensors, VU-meters, tachometers, radio scales etc. When applying the displays in measuring equipment, multicolored light emitting diodes can be used as range limitation. Ring scales are obtained by a circular arrangement of the diodes. The IC UAA 170 has especially been developed for driving a scale of 16 LEDs.

The input voltages at pins 11, 12 and 13 are freely selectable between 0 and 6 V. Any kind of adjustment becomes possible by suitable voltage drivers. The DC value $V_{control}$ is always assigned to a certain spot of the diode chain.

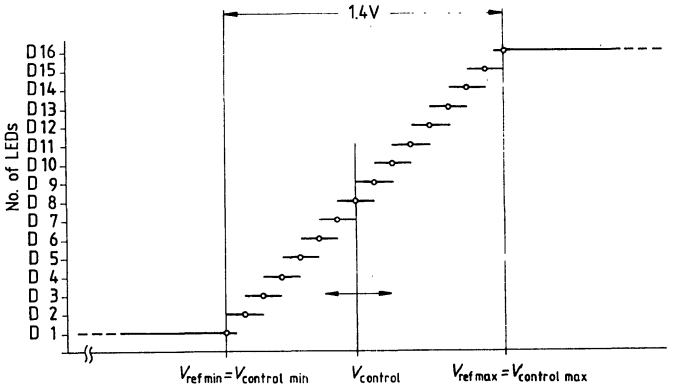
The voltage difference between pins 12 and 13 thereby corresponds to the possible indication range. $\Delta V_{12/13}$ defines at the same time the light transition between two diodes. With $\Delta V_{12/13}$ approx. 1.4 V, the light point glides smoothly along the scale. With increasing voltage difference, the passage becomes more abrupt. With $\Delta V_{12/13}$ approx. 4 V, the light point jumps from diode to diode.

Input voltages beyond the selected indication range cause the diodes D1 or D16 respectively, to light up, identifying only that the range has been exceeded.

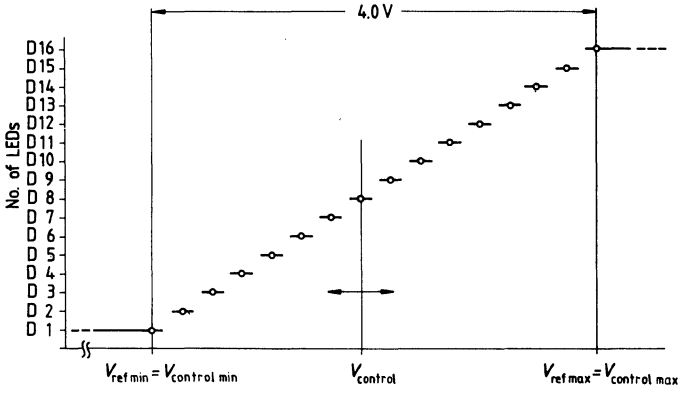
Block diagram



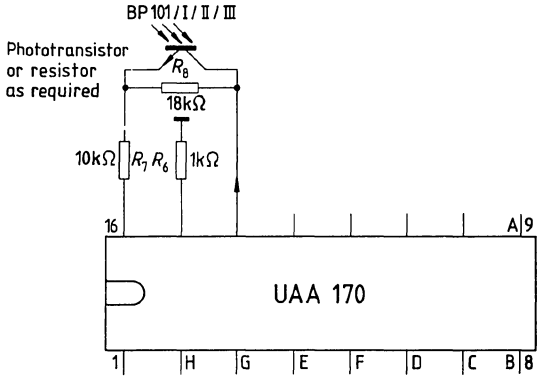
Indication for smooth transition UAA 170



Indication for abrupt transition UAA 170



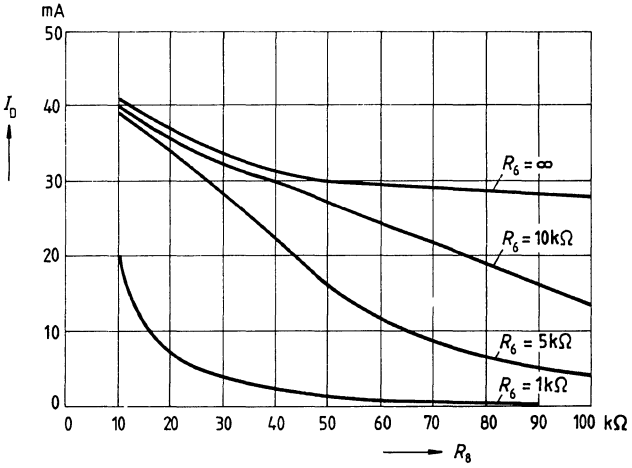
Brightness control



Pins 14, 15, and 16 serve to determine the diode current. Corresponding to the desired light intensity, the forward current of the diodes is linearly variable in the range I_f approx. 0 to 50 mA. The resistance at pin 15 defines the adjusting range. The resistances between pin 14 and 16 determine the current.

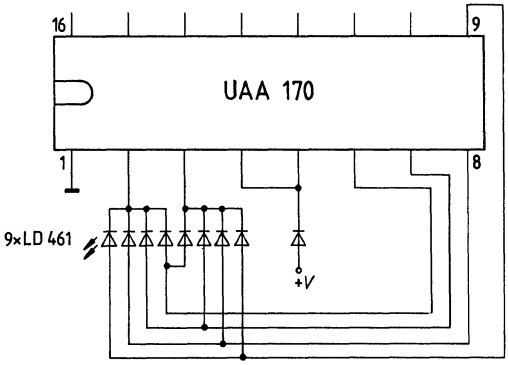
With the aid of a phototransistor, such as BP 101, the light intensity of the LEDs can be adjusted to the light fluctuations of the environment.

Diode current versus base emitter resistance
$V_S = 12$ V; $T_{amb} = 25$ °C; $V_{14} = 5.4$ V; red LEDs

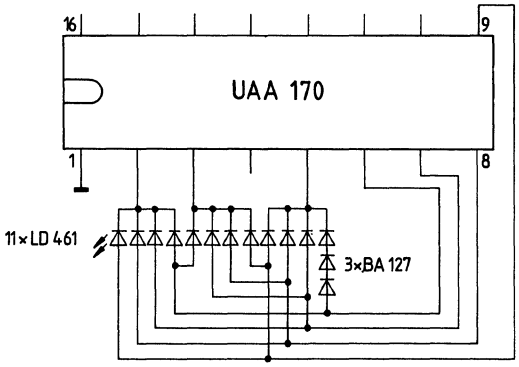


Operation of less than 16 LEDs

Control of 9 LEDs

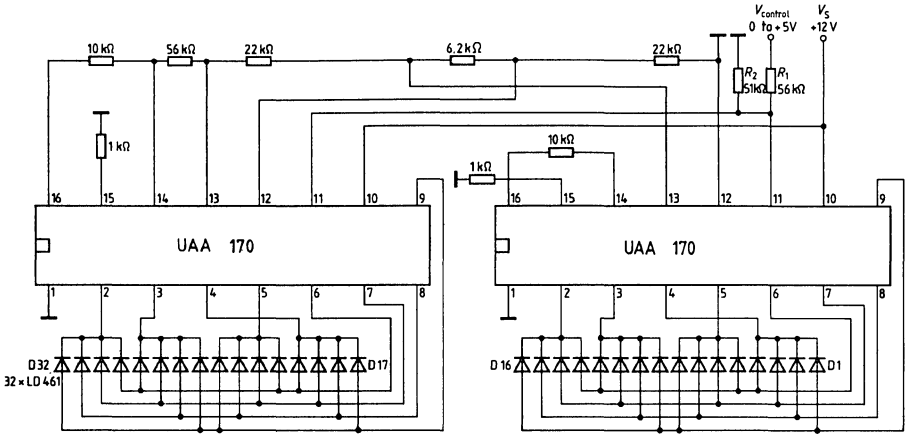


Control of 11 LEDs



Application circuit for the control of 30 LEDs with 2 x UAA 170

Range of control voltage $V_{control} = 0$ to 5 V
Voltage difference $V_{12/13} = 2 \times 1.2\ V = 2.4\ V$
Since the diodes D16 or D17 are permanently lit when the maximum or minimum voltages V_{13} or V_{12} adjusted by R_3, R_4, R_5, are exceeded or fall short the diodes should be covered, if necessary.



The figure shows an expansion of the circuit to 30 diodes with 2 ICs UAA 170. The diodes D16 or D17 light permanently, when the reciprocal absolute ratings are exceeded. They should be covered. The reference voltage $\Delta V_{12/13} = 2 \times 1.2 = 2.4$ V is derived from a stabilized dc voltage of typ. 5 V available at pin 14. A resistance of 6.2 kΩ provides an overlapping of the ranges in order to ensure a smooth transition from D15 to D18. The control voltage $V_{control}$ is forwarded in a parallel mode to pins 11 via a divider $R_1 : R_2$. The voltage divider is to be dimensioned according to the desired input voltage. With a divider current of $I = 100$ µA and a control voltage of $V_{control} = 10$ V, the following is valid:

$$R_2 = \frac{\Delta V_{12/13}}{I} = \frac{2.4}{0.1} = 24\ k\Omega \text{ and}$$

$$R_1 = \frac{V_{control} - \Delta V_{12/13}}{I} = \frac{7.6}{0.1} = 76\ k\Omega$$

The nearest standard value is $R_1 = 75$ kΩ. The voltage difference for switching an incremental step is then $\Delta V_{control} = \frac{10\ V}{30} = 0.16\ V$.

DIP 18

Integrated circuit for driving 12 light emitting diodes. Corresponding to the input voltage the LEDs forming a light band are controlled similar to a thermometer scale.

By using an appropriate circuitry the brightness of the LEDs can be varied and the light passage between two adjacent LEDs can be arranged between "smooth" and "abrupt".

Maximum ratings

Supply voltage	V_S	18	V
Input voltage	V_3	6	V
	V_{16}	6	V
	V_{17}	6	V
Storage temperature range	T_{stg}	−40 to 125	°C
Junction temperature	T_j	150	°C
Thermal resistance (system-air)	$R_{th\,SA}$	78	K/W

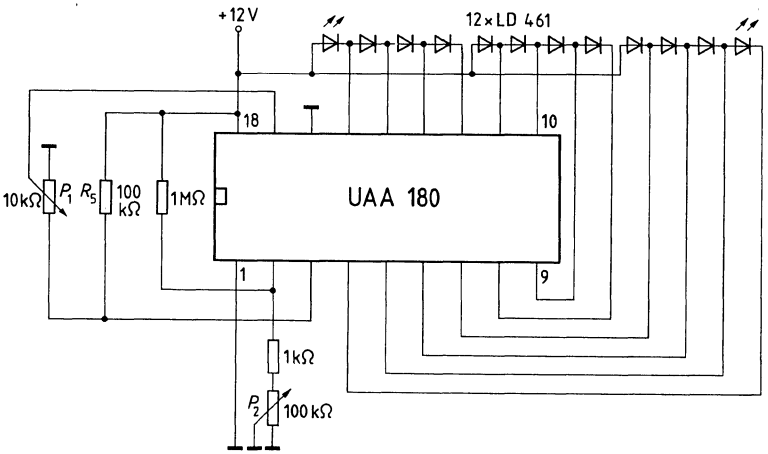
Operating range

Supply voltage range	V_S	10 to 18	V
Ambient temperature range	T_{amb}	−25 to 85	°C

Characteristics ($V_S = 12$ V, $T_{amb} = 25$ °C)

		min	typ	max	
Current consumption ($I_2 = 0$) (without LED current)	I_{18}		5.5	8.2	mA
Input currents ($V_3 - V_{16} < 2$ V)	I_3		0.3	1	µA
	I_{16}		0.3	1	µA
	I_{17}		0.3	1	µA
Voltage difference for smooth light transition	$V_{16/3}$	1			V
Voltage difference for abrupt light transition	$V_{16/3}$	4			V
Diode current per diode	I_D		10		mA
Tolerance of LED forward voltages	ΔV_D			1	V

Measurement circuit



P_1 light band test
P_2 brightness test

Scale display with light emitting diodes

Scale displays by means of a growing light band are particularly suitable for the measuring of approximate values. Applications of this kind are level sensors, VU meters, tachometers, field strength indicators etc. When applying the displays in measuring equipment, multi-colored LEDs can be used as range limitation.

The voltage difference between pins 16 and 3 thereby corresponds to the possible indication range. $\Delta V_{16/3}$ defines at the same time the light passage between two diodes. With $\Delta V_{16/3} \geqq 1$ V, the light band glides smoothly along the scale. With increasing voltage difference, the passage becomes more abrupt. With $\Delta V_{16/3}$ approx. 4 V, the light band jumps from diode to diode.

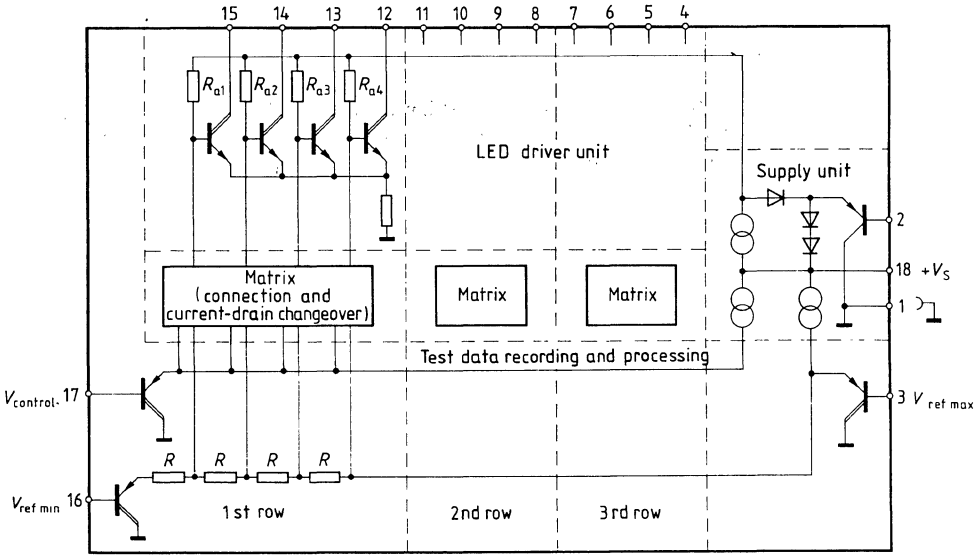
Each quartet must consist of identical diodes in order to maintain its functional characteristics.

It is therefore possible to design the first and third quartet as diodes emitting the color red and the second quartet as diodes emitting the color green to delineate a certain operational area.

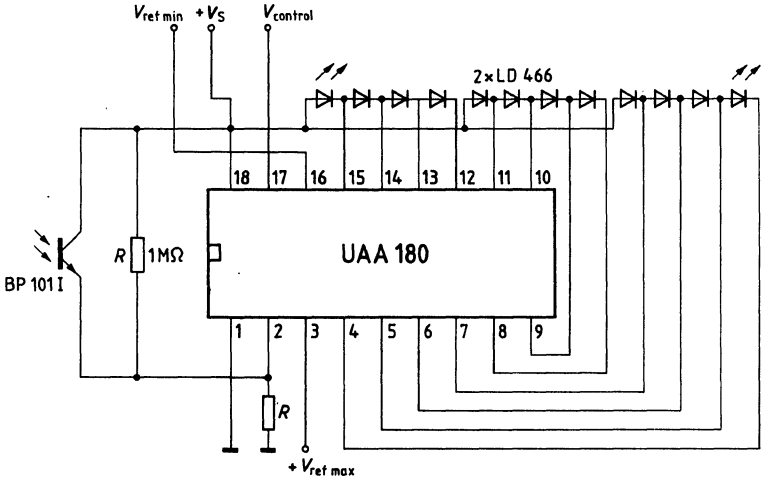
Pin 2 serves to determine the diode current. Corresponding to the desired light intensity, the forward current of the diodes is variably linear in the range I_f approx. 0 to 10 mA.

Application circuit 1 shows the possibility of designing this resistance, adjustable by means of a phototransistor BP 101, in order to adapt the light intensity to changing ambient brightness. The adjusting range of the diode current lies between I_f approx. 5 mA (BP 101 not lit) and I_f approx. 10 mA (BP 101 fully lit). If pin 2 is open the diode current is 10 mA.

Block diagram



Application circuit 1

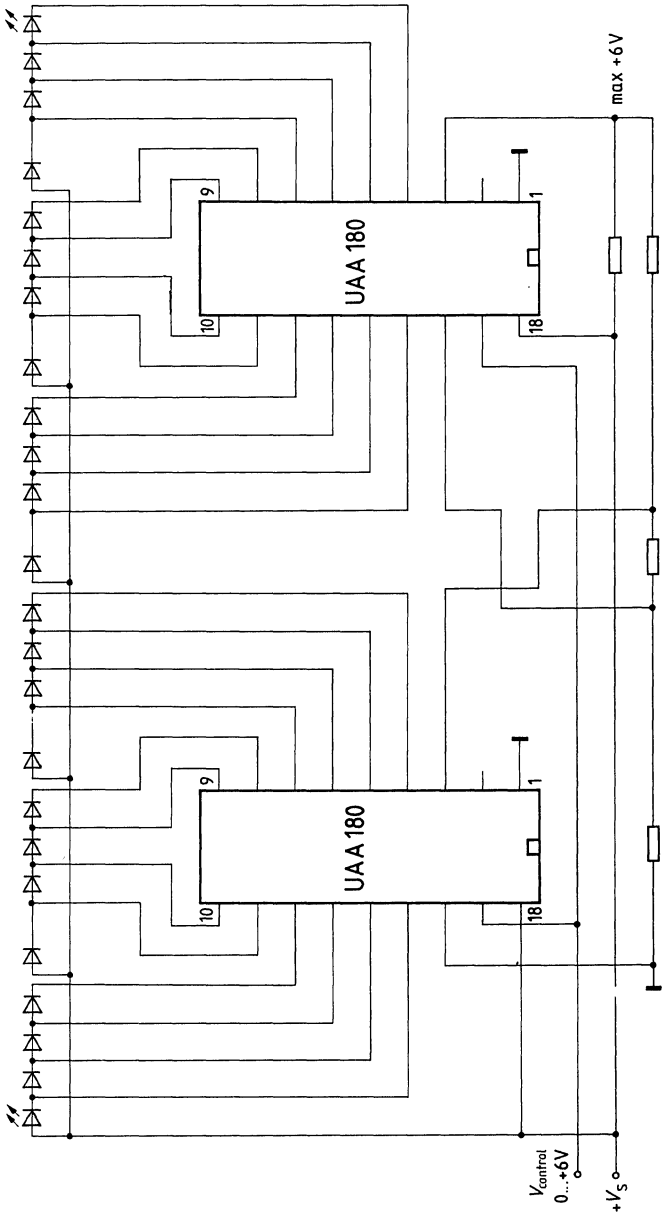


Depending on the actual maximum ratings, the resistances R_1 to R_7 can be varied widely as follows:

$R_3 = 820\ \Omega$
$R_4 = 56\ k\Omega$
$R_5 = 220\ k\Omega$
$R_6 = 2.2\ k\Omega \ldots 100\ k\Omega$

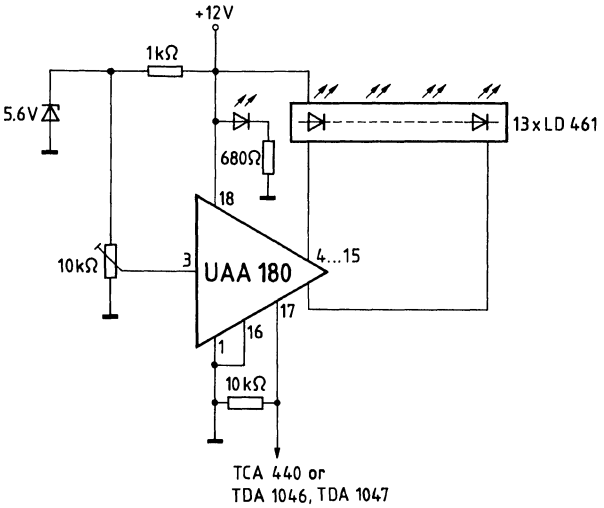
If a quartet does not need the full number of display diodes and if the first wired diodes shall be left luminous at full driving, bridges have to be inserted replacing the missing LEDs. Otherwise the first diodes of the quartet switch off when their display range is exceeded.

Application circuit 2
for cascading several UAA 180 ICs (up to 7)



Application circuit 3

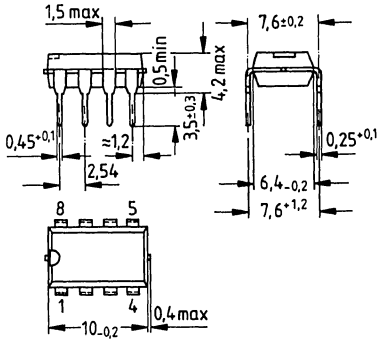
for field strength indication



Package Outlines

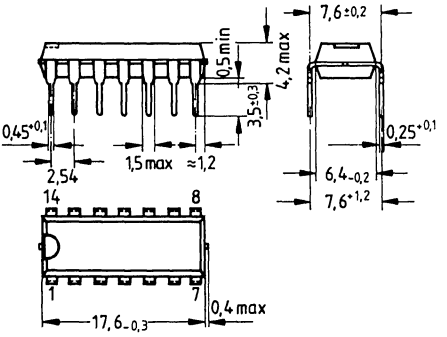
Package Outlines

Plastic plug-in package 20 A 8 DIN 41866
8 pins, DIP



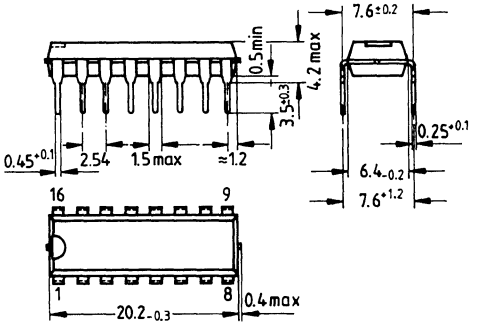
Approx. weight 0.7 g

Plastic plug-in package 20 A 14 DIN 41866
14 pins, DIP



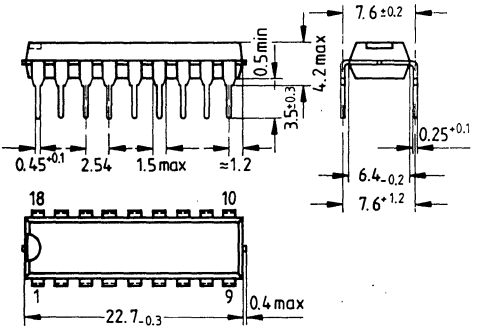
Approx. weight 1.1 g

Plastic plug-in package 20 A 16 DIN 41866
16 pins, DIP



Approx. weight 1.2 g

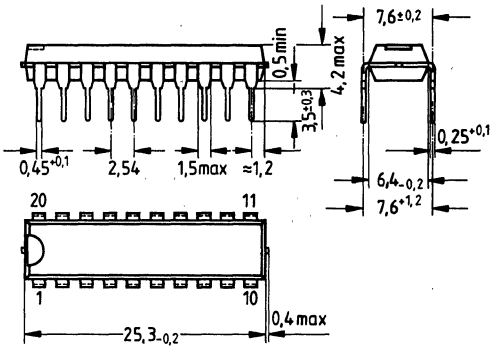
Plastic plug-in package 20 A 18 DIN 41866
18 pins, DIP



Approx. weight 1.3 g

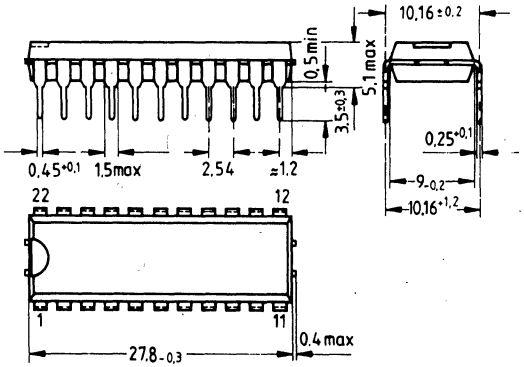
Dimensions in mm

Plastic plug-in package 20 A 20 DIN 41866
20 pins, DIP



Approx. weight 1.5 g

Plastic plug-in package 20 D 22 DIN 41866
22 pins, DIP

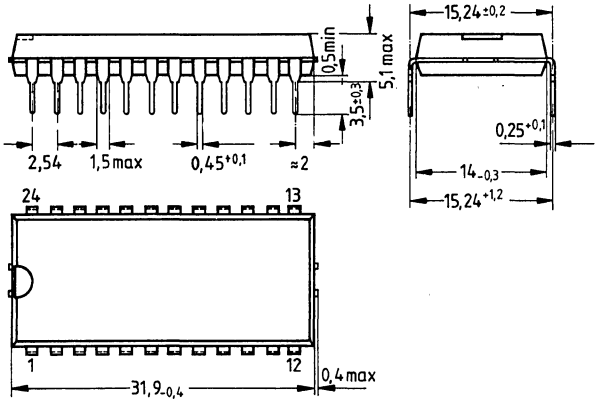


Approx. weight 2.1 g

Dimensions in mm

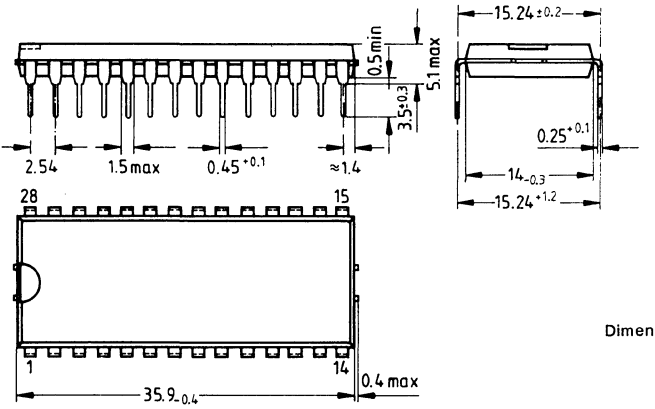
Package Outlines

Plastic plug-in package 20 B 24 DIN 41866
24 pins, DIP



Approx. weight 2.5 g

Plastic plug-in package 20 B 28 DIN 41866
28 pins, DIP

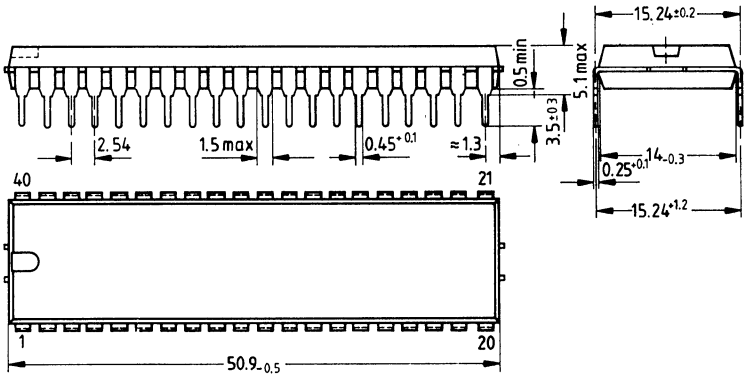


Dimensions in mm

Approx. weight 3 g

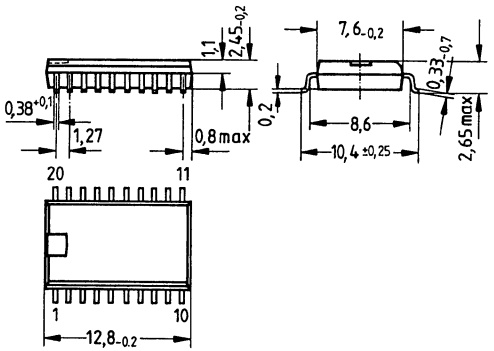
Package Outlines

Plastic plug-in package 20 B 40 DIN 41866
40 pins, DIP



Approx. weight 5.9 g

Miniature plastic package (G)
20 pins (SO 20 L)

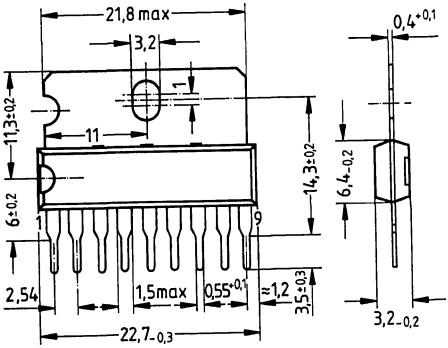


Approx. weight 0.6 g

Dimensions in mm

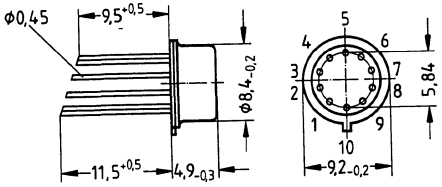
Package Outlines

Plastic power package
with cooling fin and 9 pins, SIP



Approx. weight 1.9 g

Metal package 5 J 10 DIN 41873
(similar to TO 100)

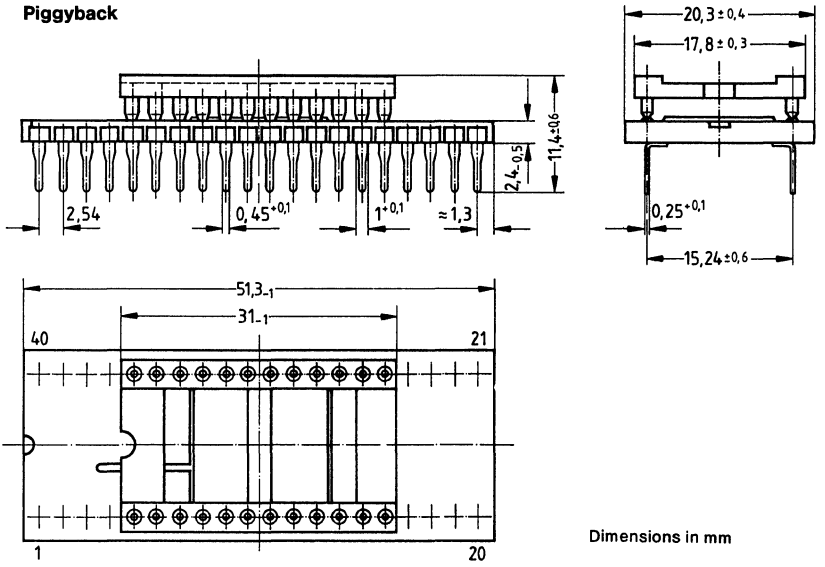


Dimensions in mm

Approx. weight 1.1 g

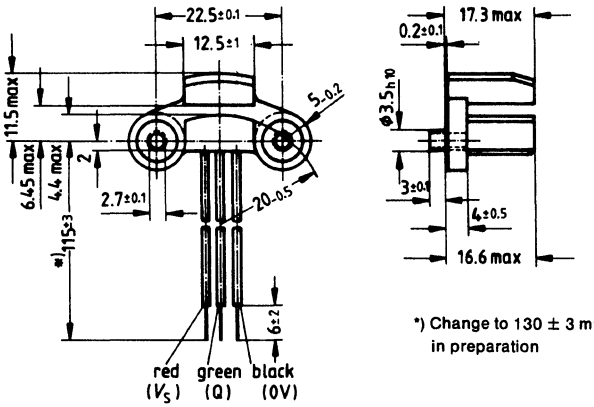
Package Outlines

Piggyback



Dimensions in mm

Special package

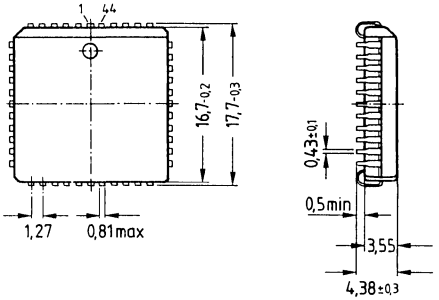


*) Change to 130 ± 3 mm in preparation

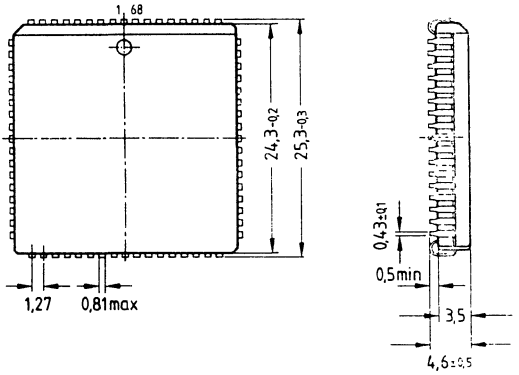
Approx. weight 8.5 g

Package Outlines

Plastic package
44 pins, PLCC



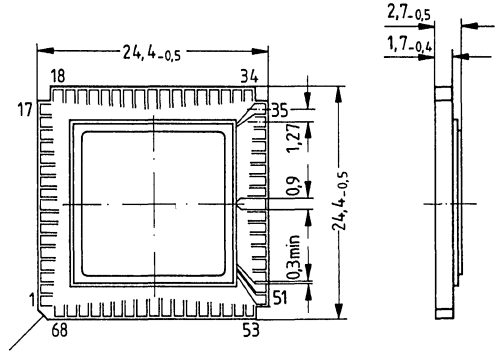
Plastic package
68 pins, PLCC



Dimensions in mm

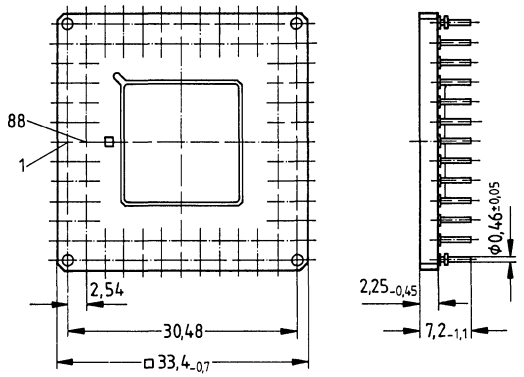
Package Outlines

Ceramic package
68 pins, C-CC



Identification for Pin 1

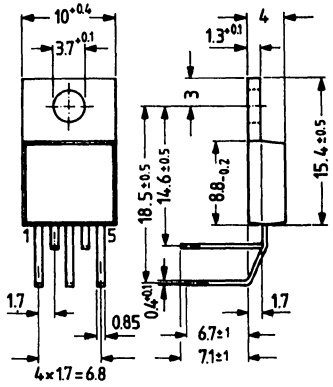
Ceramic package
88 pins, PGA



Dimensions in mm

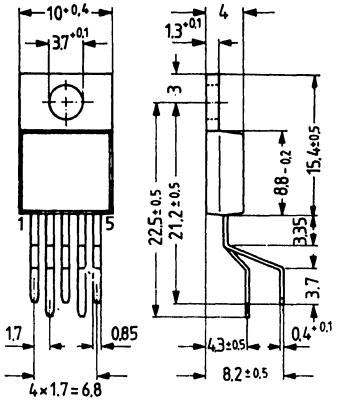
Package Outlines

Plastic power package, similar to TO-220
(with cooling strip and 5 pins)



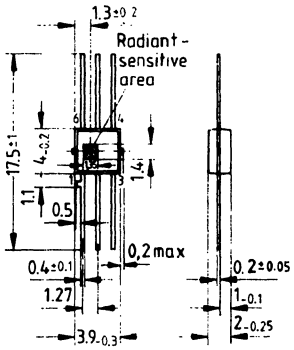
Approx. weight 2.1 g

Plastic power package, similar to TO-220
(with cooling strip and 5 pins)



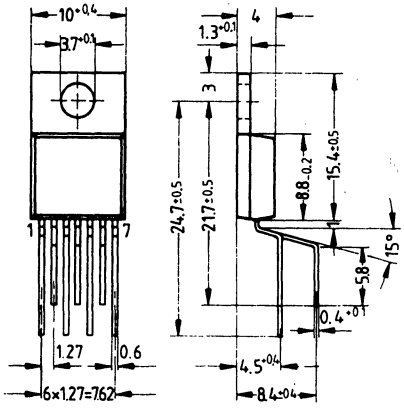
Approx. weight 2.1 g

Transparent **plastic miniature package**
6 pins



Approx. weight 0.1 g

Plastic power package, similar to TO-220
(with cooling strip and 7 pins)

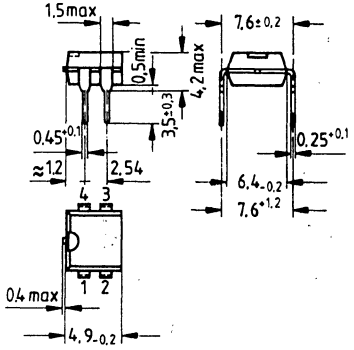


Approx. weight 2.1 g

Dimensions in mm

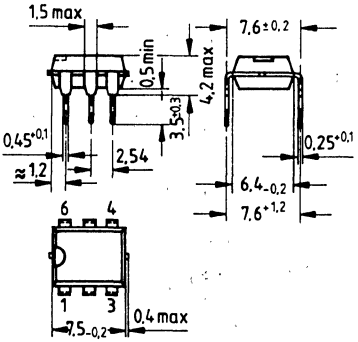
Package Outlines

Plastic package, P-DIP, 4 pins
20 A 4 DIN 41866



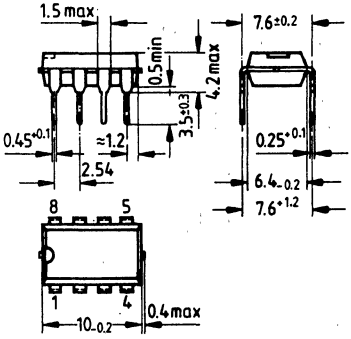
Approx. weight 0.5 g

Plastic package, P-DIP, 6 pins,
20 A 6 DIN 41866



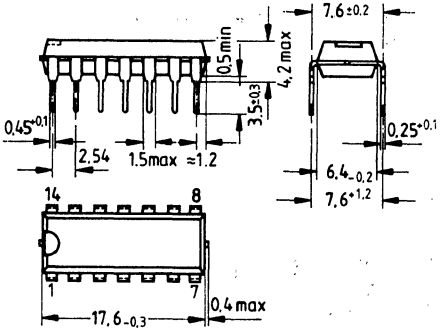
Approx. weight 0.7 g

Plastic package, P-DIP, 8 pins
20 A DIN 41866



Approx. weight 0.7 g

Plastic package, P-DIP, 14 pins
20 A 14 DIN 41866

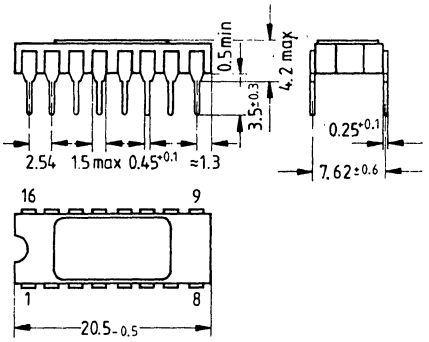


Approx. weight 1.1 g

Dimensions in mm

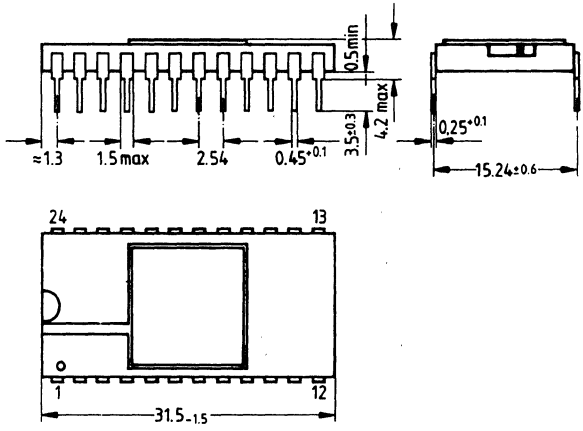
Package Outlines

Ceramic package, C-DIP, 16 pins



Approx. weight 1.4 g

Ceramic package, C-DIP, 24 pins

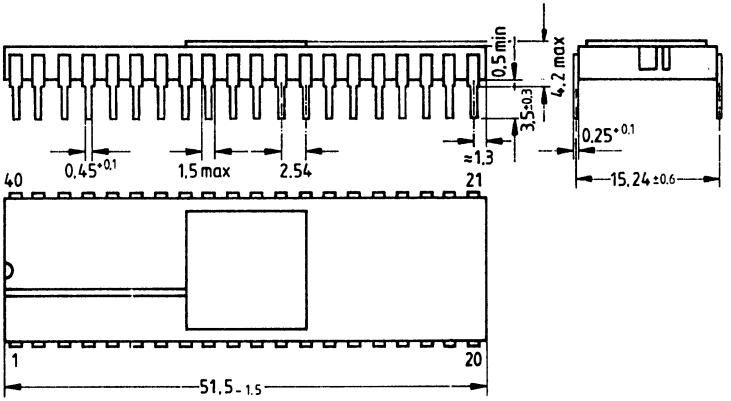


Approx. weight 3 g

Dimensions in mm

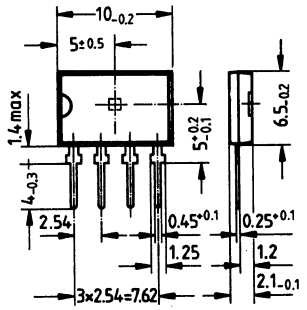
Package Outlines

Ceramic package, C-DIP, 40 pins



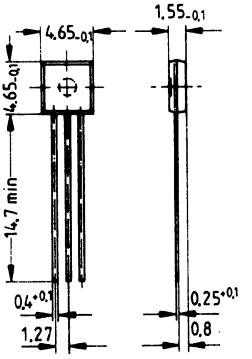
Approx. weight 6.8 g

Plastic flatpack, 4 pins



Approx. weight 0.5 g

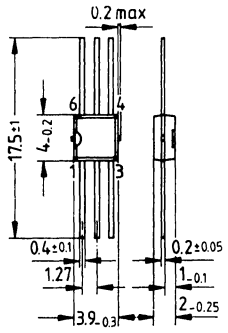
Plastic flatpack, 3 pins



Dimensions in mm

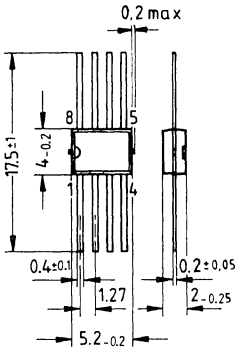
Package Outlines

Miniature plastic package
6 pins



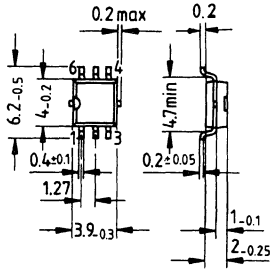
Approx. weight 0.1 g

Miniature plastic package
8 pins



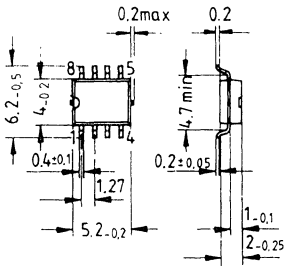
Approx. weight 0.15 g

Miniature plastic package (SMD)
6 pins (similar to SO 6)



Approx. weight 0.1 g

Miniature plastic package (SMD)
8 pins (similar to SO 8)

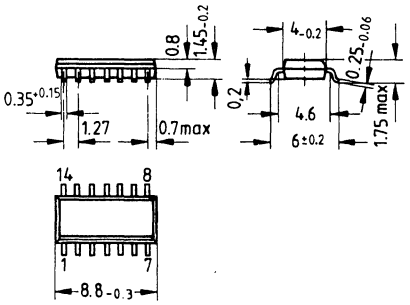


Approx. weight 0.15 g

Dimensions in mm

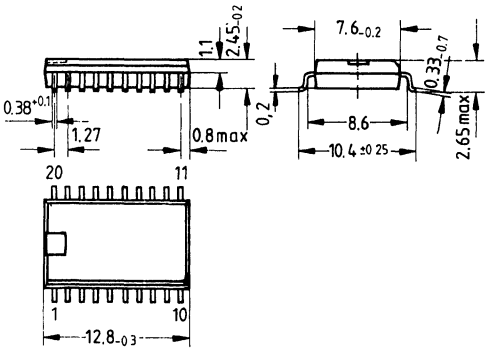
Package Outlines

Miniature plastic package (SMD)
14 pins (SO 14)



Approx. weight 0.13 g

Miniature plastic package (SMD)
20 pins (SO 20 L)



Approx. weight 0.6 g

Dimensions in mm

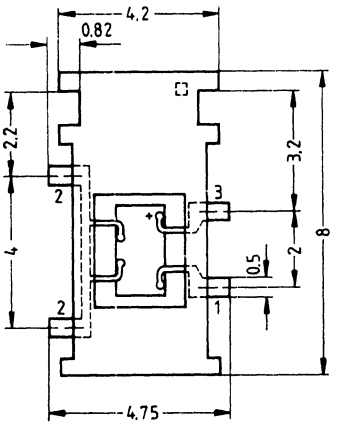
Package Outlines

MIKROPACK (SMD)

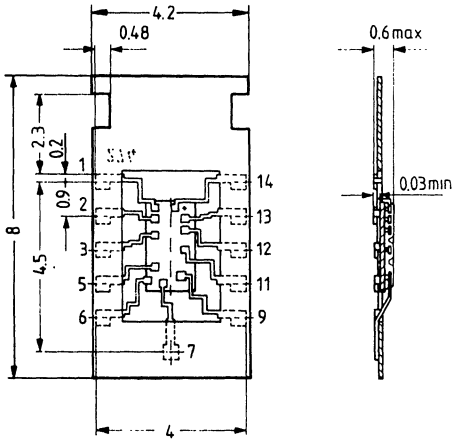
MIKROPACKs are delivered exclusively in taped form.

Dimensions of perforation in acc. with DIN 15851, sheet 2 (Super 8)

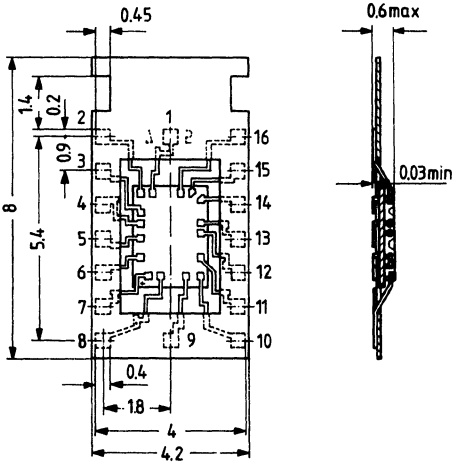
TCA 205 K



TLE 4901 K



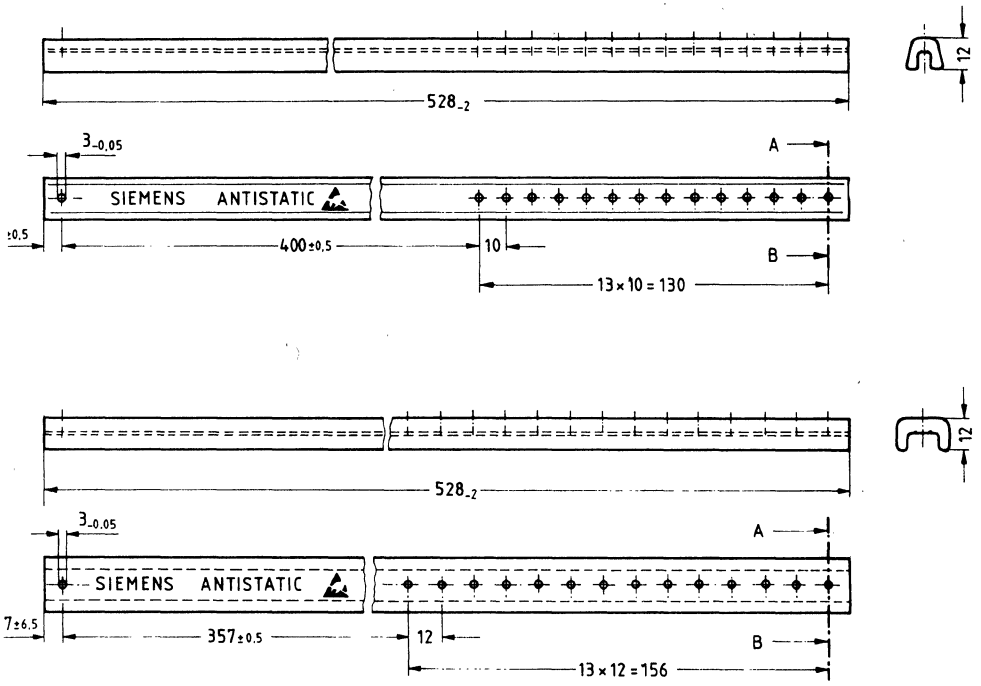
TCA 955 K



Dimensions in mm

Package Outlines

Packaging tubes



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