



# R6500 Microcomputer System APPLICATION NOTE

## Interfacing R6500 Microprocessors To a Floppy Disk Controller

### PURPOSE

Microprocessors in the R6500 family can operate with a wide variety of special-purpose peripheral controller devices. This Application Note describes the interface between an R6500 microprocessor and either of two Western Digital Floppy Disk Formatter/Controller devices, FDC 1781 or FDC 1791. The interface to the FDC 1781 requires a pair of one-shots, whereas the FDC 1791 can be interfaced directly. In both cases, the processor access time is one cycle.

### DESCRIPTION

The basic interface for both Western Digital devices is shown in Figure 1. Data is passed between the R6500 microprocessor and the floppy disk controller on an 8-bit, bi-directional data bus. Address bus lines A0 and A1 select the FDC registers to be accessed. The remaining Address Bus lines, A2 through A15, can be used to generate a Chip Select signal ( $\overline{CS}$ ) when the FDC has been addressed. The  $\phi_2$  clock from the processor is used to generate strobes  $\overline{RE}$  and  $\overline{WE}$ , for reading and writing the FDC registers.

### TIMING

R6500 processors that run on a 1-MHz clock with 50-percent duty cycle will produce  $\phi_2$  pulse widths ( $PHW_{\phi_2}$ ) of 470 ns minimum. Since the Western Digital FDC 1791 device requires Read and Write pulse widths ( $\overline{RE}$  and  $\overline{WE}$ , respectively) of 400 ns, the  $\phi_2$  clock is adequate to generate these pulses directly. However, the FDC 1781 requires a minimum pulse width of 500 ns for both  $\overline{RE}$  and  $\overline{WE}$ , so some additional strobe-generation circuitry must be included in that interface.

This circuitry is comprised of two one-shots,  $t_{W1}$  and  $t_{W2}$ , in which  $t_{W1}$  determines the start of the pulse and  $t_{W2}$  determines the width of the pulse. The limiting equation for  $t_{W1}$  is:

$$T_{ADS} + T_{ADD} + 50 < t_{W1} < 475 \text{ ns} \quad (\text{Equation 1})$$

where  $T_{ADS}$  = Address Setup Time from R6500 (225 ns max)

$T_{ADD}$  = Address Detect Delay Time

and the limiting equation for  $t_{W2}$  is:

$$500 \text{ ns} < t_{W2} < 1000 \text{ ns} - t_{W1} \quad (\text{Equation 2})$$

A simple way to guarantee that the timing requirements are met is to make  $t_{W1}$  and  $t_{W2}$  approach their respective

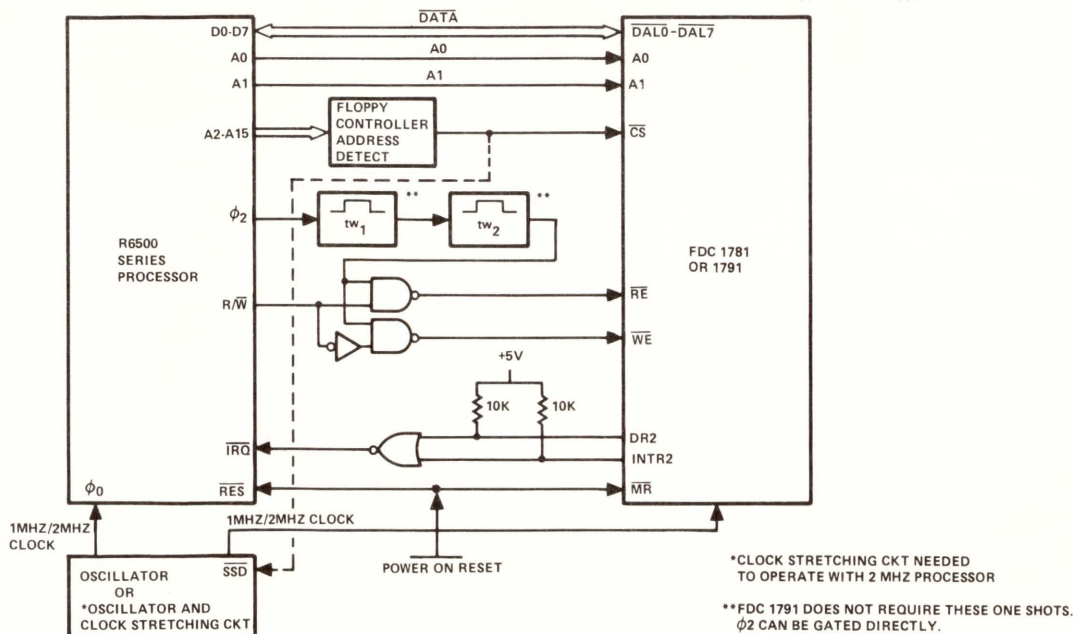


Figure 1. Interface Block Diagram

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lower bounds. The Write cycle timing is satisfied when the Read cycle timing is satisfied, except that the  $t_{W2}$  pulse should be made wide enough to allow the Write data to have adequate setup time. The constraints are reflected in this equation:

$$975 \text{ ns} < t_{W1} + t_{W2} \quad (\text{Equation 3})$$

Time  $t_{W1}$  should be made as narrow as possible, with  $t_{W2}$  widened to satisfy Equations 1 and 2. Figure 2 summarizes the timing relationships.

## INTERFACING 2-MHZ R6500 MICROPROCESSORS

The interface described is based on a 1-MHz R6500 microprocessor. To use a 2-MHz microprocessor (R6500A series), a clock stretching circuit is necessary. This circuit is described in a separate Application Note, "R650X Clock Stretching for Use with Slower Peripherals", Rockwell Document No. R6500N07.

### WESTERN DIGITAL TIMING SPECIFICATIONS

Characteristic	Symbol	Min	Max	Units
Read Data Access Time, from $\overline{RE}$ ↓	$T_{DACC}$		350	ns
Read Data Hold Time, from $\overline{RE}$ ↑	$T_{DOH}$	50		ns
$\overline{RE}$ Pulse Width For FDC 1781 For FDC 1791	$T_{RE}$	500 400		ns
Write Data Hold Time, from $\overline{WE}$ ↑	$T_{DH}$	20		ns
Data Setup Time to $\overline{WE}$	$T_{DS}$	250		ns
$\overline{WE}$ Pulse Width For FDC 1781 For FDC 1791	$T_{WE}$	350 350		ns
Setup Address and $\overline{CS}$ to $\overline{WE}$	$T_{SET}$	50		ns

**NOTE:** For R6500 timing specifications, refer to the R6500 Microprocessors Data Sheet, Rockwell Document No. 29000D39.

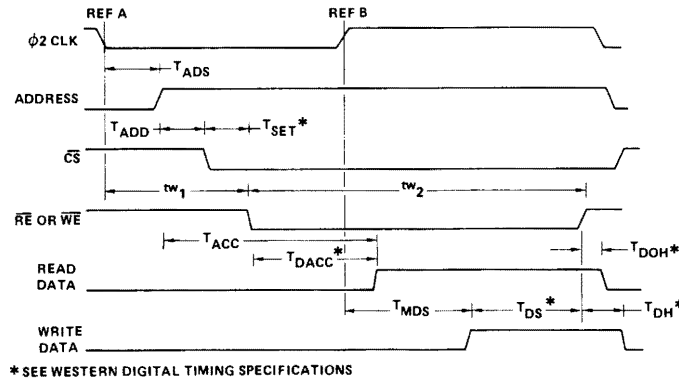


Figure 2. Read/Write Timing

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