Rockwell

PARALLEL PROCESSING SYSTEM (PPS)

PRODUCT BULLETIN

PPS 4/2 TWO-CHIP MICROCOMPUTER SYSTEM

Rockwell introduces two new microcomputer circuit devices which provide a flexible system for cost sensitive applications. The two circuits comprise a CPU chip and a combination Memory and I/O chip. These chips may be used as a complete two chip microprocessor or with other Rockwell circuits of the PPS-4 family to provide a broad spectrum of system functions at lower costs than previously attainable.

FEATURES

PPS4 2 CPU CIRCUIT

- Self-contained Clock
- PPS-4 Instruction Set
- Expanded I/O Using Discrete I/O Commands
- Direct LED Segment or Fluorescent Display Compatibility
- PPS-4 Bus System Compatibility
- 5 Microsecond Cycle Time
- 100 pf Bus Drive Capability

PPS4/2 MEMORY/IO SYSTEM CIRCUIT:

- 2048 x 8 Read-only Program Memory (ROM)
- 128 x 4 Data Memory (RAM)
- 16 One-bit Input/Output Ports
- Option of Using Two Memory/IO Circuits per System

SYSTEM DESCRIPTION

The PPS-4 2 System has been designed to provide a basic two circuit microcomputer which is optimized for applications requiring low cost and high performance. The two circuits provide all the computing power and applications flexibility which would require five or more of the conventional PPS-4 circuits to implement. The PPS-4 2 may be expanded to more complex applications by using any of the large family of PPS-4 circuits so that the cost of more complex systems may be reduced. The basic PPS-4 2 system is shown in Figure 1.

PPS-4/2 CPU (PN 11660)

The PPS-4 2 CPU uses an identical instruction set as the PPS-4 CPU but includes the clock generator function within the CPU circuit as well. When a conventional NTSC color TV crystal (3.579545 MHz) is connected to the XTAL I and XTAL O pins and the VCLOCK pin is connected to VDD, the CPU circuit will generate the 198.864 KHz system clock signals. These signals, A and $\bar{B}$, are used internally in the CPU and are made available to all of the PPS-4/2 and PPS-4 circuits in the system.

An additional feature in the PPS-4 2 CPU is an expanded discrete output capability. This capability is achieved by using the same instruction (DOA) as in the PPS-4 CPU but providing more I/O control. In the PPS-4 the DOA instruction causes the contents of the accumulator (A) to be transferred to an output buffer and then retained until another DOA instruction is executed. The contents of this buffer controls the output drivers. In the PPS-4 2 CPU this same function is performed but, additionally, the contents of the X register are transferred to a similar second set of buffers and drivers (DIO) so that the DOA instruction causes 8 bits to be available to external devices.

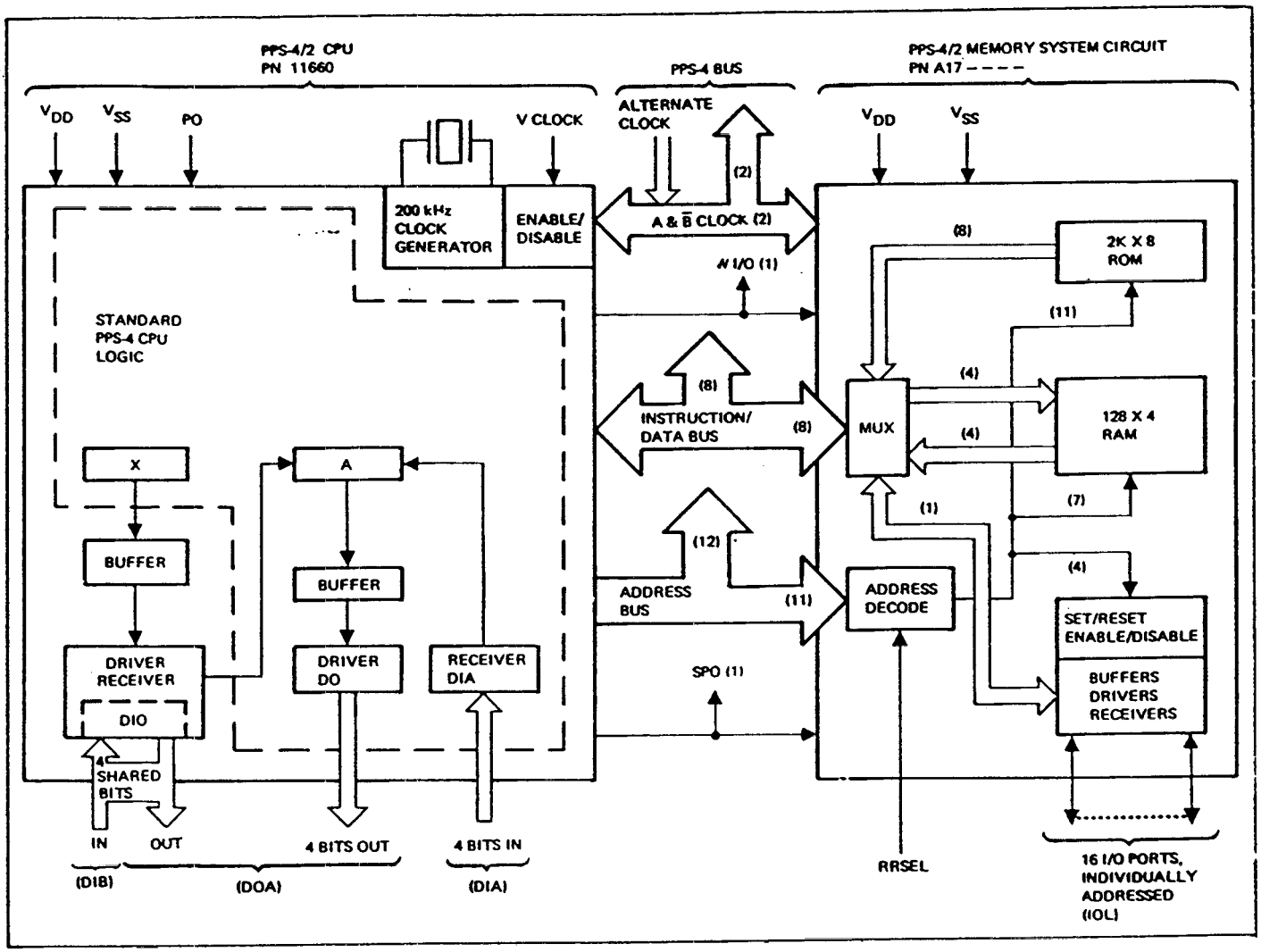


Figure 1. PPS-4/2 Two Chip Minimum Configuration

PPS-4/2 CPU (PN 11660) Continued

The discrete input commands functionally are identical in both CPU's but in the PPS-4/2 the DIB input pins are shared with the output lines loaded from the X register. The output discrete signals are all supplied from drivers which are open drain MOS transistors to VSS. If the DIO pins are being used for inputs, then the DIB instruction has the potential of providing a "masked" input if the external circuits are properly designed. The masking may be accomplished by outputting zeros from the X register with the DOA command. Where the zeros occur, the input lines will be clamped to VSS. Consequently, when the DIB instruction is executed, only the unmasked bits are loaded into the accumulator. When used in this mode, the external circuits must be designed to limit the current so that no damage can occur when the signal is tied to VSS. When all four bits are to be read, no special circuit considerations are necessary if, prior to the DIB instruction, all "one's" are output from the X register by a DOA command.

The PPS-4/2 CPU automatically floats all output lines when power is turned on. Functionally there are no other differences between the PPS-4 and the PPS-4/2 CPU's. However, the PPS-4/2 CPU also has the capability of directly driving low-power LED display segments. Fluorescent displays can also be driven if the system includes the appropriate power supply for the higher voltage display.

PPS-4/2 MEMORY/IO CIRCUIT (PN A17---)

The Memory/IO Circuit, also shown in simplified form in Figure 1, has a full 2K bytes of program storage in ROM and 128 x 4-bit words of data storage in RAM. This circuit also includes an input/output capability which allows the individual control of 16 one-bit I/O ports. All of the functions in the Memory/IO Circuit make common usage of the address decoding circuitry.

Read-Only-Memory (ROM) Section

The Read-Only-Memory is addressed in the same manner as the PPS-4 during phase 2 time, by a combination of the eleven address bits brought into the circuit and the matching of either a "1" or a "0" on the ROM/RAM Select (RRSEL) pin and an internal code established in the ROM pattern. In effect the RRSEL signal may be used as a twelfth address bit or may be used to "bank select" additional ROM's beyond the 4K direct addressing capability of the 12-bit address bus.

Data Memory (RAM) Section

The Data Memory is addressed during phase 4 time. In this circuit the state of the RRSEL during phase 4, the internal code established during fabrication, and the A/B 8 signal will establish if the RAM in the memory circuit is being accessed. Both the A/B 8 signal and the RRSEL signal must match the internal code to select the RAM. The lower 7-bits of the address will then establish which 4-bit word is being accessed and the WI/O line performs the same function as in the PPS-4 to signal that a read or a read and simultaneous write is being commanded.

Input/Output Section

In the Memory/IO Circuit, the input/output section is commanded by the same technique used by all PPS-4 I/O devices. First an IOL instruction is executed in the CPU which causes the WI/O line to signal all I/O devices in the system that the next instruction byte contains a device identification (4-bits) and the specific command to be executed (4-bits). The IOL instruction, via the WI/O line, also tells the RAM to stay off the data bus so that the input/output data may be transmitted.

In this circuit the I/O section may be encoded during fabrication to be identified as device 0, 2, 4, or 6 so that any conflict with other I/O device addresses used in the specific system may be avoided.

There are two basic instructions interpreted by the I/O section, Select Enable Status (SES) and Select Output Status (SOS), but the I/O section also makes use of information from the accumulator and from the address bus to actually generate a total of 64 unique instructions.

The address logic in the device decodes the lower 6-bits of the address bus and makes use of the lowest 16 unique addresses to address I/O lines 0 through 15. Consequently, the lower two-bits in the BM portion of the data address register must be zero. Then the BL portion will identify the I/O port.

Each port has a driver similar to the drivers on the PPS-4/2 CPU which consists of an open drain to the VSS MOS transistor and a holding flip-flop. The addressed holding flip-flop is set to the same state as the most significant bit in the accumulator if a Select Output Status command is executed. Also whenever any I/O command is executed, the state of the signal on the addressed I/O port at the prior bit time causes the most significant bit in the accumulator to be set to the same state simultaneous with the output function.

The second basic instruction, Select Enable Status (SES), controls all 16 I/O ports simultaneously. When SES is executed, if the most significant bit in the accumulator is a zero all outputs are disabled (floated), and conversely, if it is a one all of the outputs are made available from the holding flip-flops. With this instruction, as with the SOS instruction, the status of the port addressed by BL is loaded into the accumulator. All of the input-output functions in the Memory/IO Circuit are summarized in Table 1.

The SPO signal generated when power comes on causes the enable flip-flop to be set to zero so that all 16 I/O ports are floated. The individual holding flip-flops are not set automatically.

POTENTIAL APPLICATIONS

The basic PPS-4/2 two circuit system may be used for many applications without requiring any other PPS-4 devices and minimal amounts of external hardware. The 16-ports from the Memory System Circuit may be used as strobe lines for a keyboard and the DIA, or DIA and DIB, inputs can be used for up to 64 or 128 key keyboards. The 8-bits obtained from a DOA instruction may be used to directly drive a 7- or 8-segment display and the strobe signals can also be derived from the same outputs as were used for the keyboard strobing. A block diagram of a 16-digit direct drive display and 64-key keyboard system is shown in Figure 2. In fluorescent displays using the tubes as pull up resistors, no other circuit devices are required. LED displays may require a current sink transistor for each digit. Other configurations are possible. For instance if the DIA and DIB inputs are used for a 128-key keyboard, the 4-bits of output obtained from the DO lines could drive a BCD-to-7 segment decoder. Also, a cash register-type-printer could be operated by using the 16-output lines, controlled by the SES instruction, to signal which print solenoids shold be activated to print all of the characters in a line while timing and output control signals are provided from the PPS-4/2 CPU.

Many options are possible. One option would be to use the basic PPS-4/2 circuit input/output for a keyboard display function and use a printer controller circuit to control the printer. This is illustrated in the block diagram shown in Figure 3. Another option would be to use a keyboard printer circuit and generate the display function in the microcomputer set. Still another option would be to use a general purpose keyboard display circuit and control the printer from software and the basic I/O. The basic I/O is flexible enough so that the PPS-4/2 two circuit system can provide the capabilities for sophisticated controllers for a variety of industrial applications. Sequencers and sophisticated timing systems, set point controllers with complex control functions, automotive controllers, electronic games, etc., all provide potential areas of application for the low cost PPS-4/2 System.

TABLE 1. I/O SECTION INSTRUCTIONS

Mnemonic	Command Name	I/D Bus 8 7 6 5 4 3 2 1	Accumulator A4 A3 A2 A1	Description
SES	Select Enable Status	0 S S 0 X X X 0	1 X X X	Enable All Outputs (Enable F/F←1) Accumulator←1XXX if I/O(00BL)=1 Accumulator←0XXX if I/O(00BL)=0
SES	Select Enable Status	0 S S 0 X X X 0	0 X X X	Disable All Outputs (Enable F/F←0) Accumulator←1XXX if I/O(00BL)=1 Accumulator←0XXX if I/O(00BL)=0
SOS	Select Output Status	0 S S 0 X X X 1	1 X X X	I/O(00BL) F/F ←1 Accumulator←1XXX Accumulator←0XXX if I/O(00BL)=0
SOS	Select Output Status	0 S S 0 X X X 1	0 X X X	I/O(00BL) F/F ←0 Accumulator←1XXX if I/O(00BL)=1 Accumulator←0XXX if I/O(00BL)=0

SYSTEM INTERFACE

The timing and bus characteristics of the PPS-4/2 System are identical to the PPS-4 System with a reduced capability in the total number of circuits which can be driven from the CPU. Capability is provided for driving up to ten PPS circuits. The signals for each of the circuits with their pin numbers are identified in Tables 2 and 3. All discrete output signals have approximately twice the current drive capability of the PPS-4 CPU.

The PPS-4/2 System is thoroughly compatible with all standard PPS-4 devices including the ROM, RAM, EEROM, Bus Interface (BI), RAM Interface, and complete family of I/O devices.

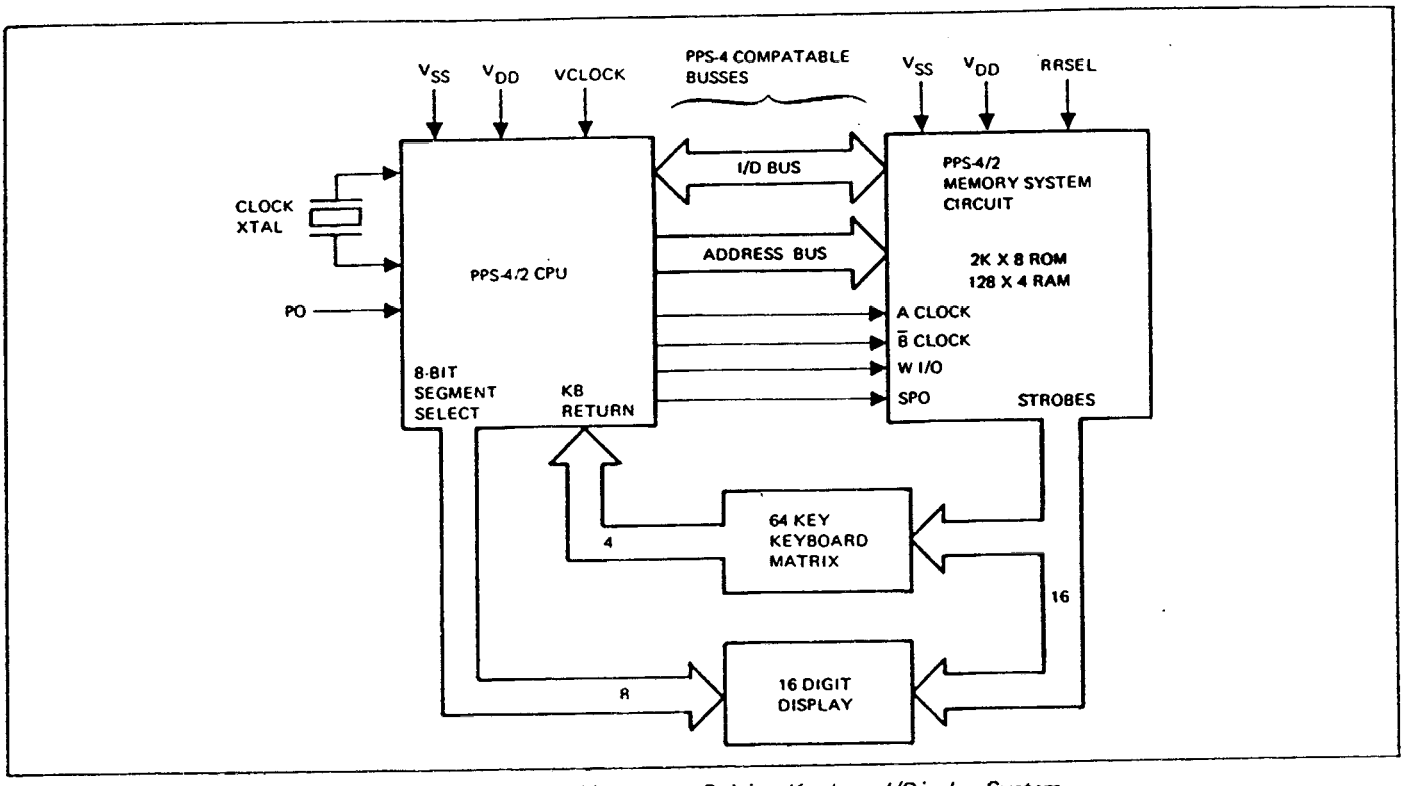


Figure 2. Basic PPS-4/2 System Driving Keyboard/Display System

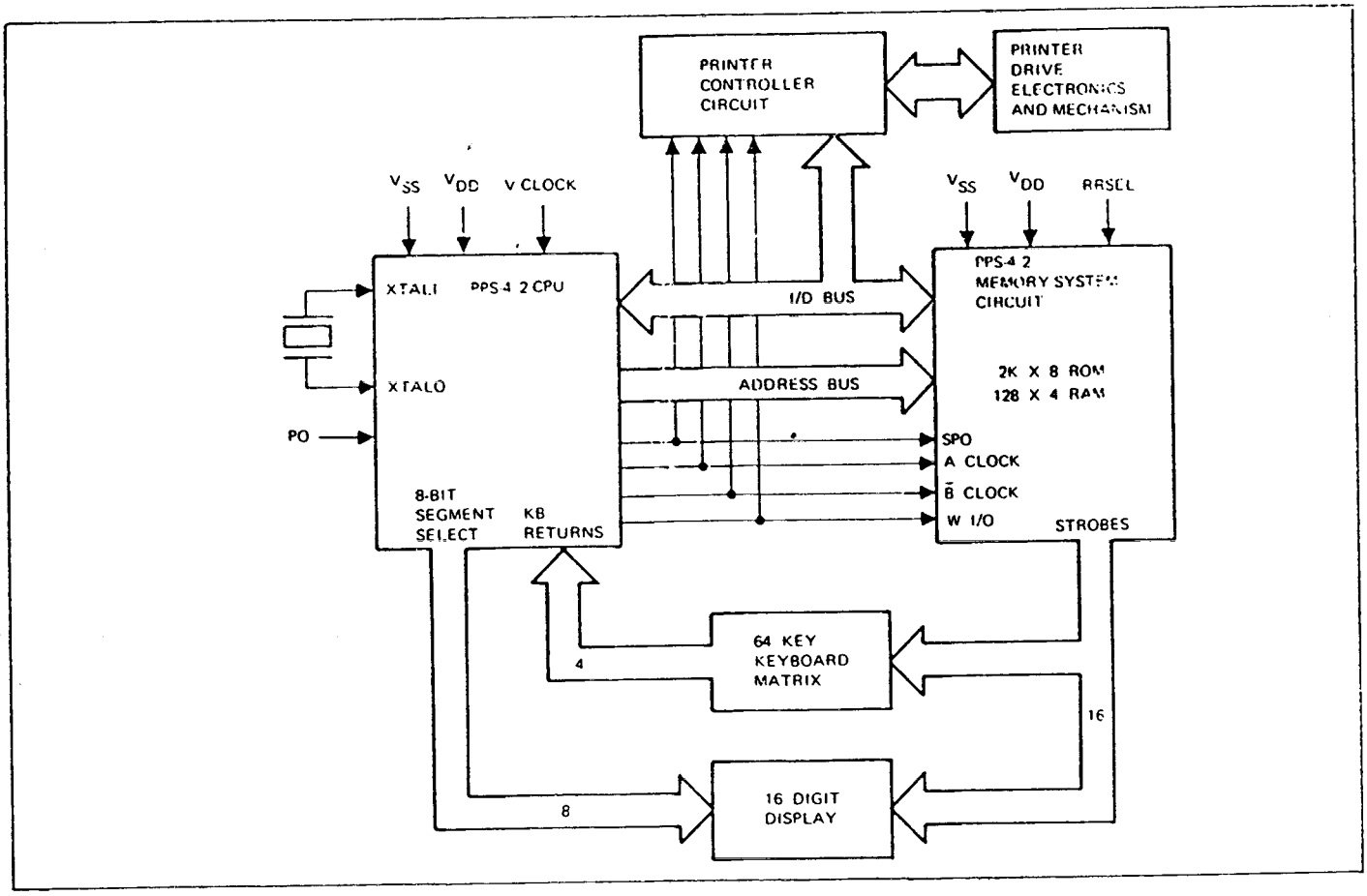


Figure 3. Low Cost Cash Register Block Diagram

TABLE 2. PPS-4/2 CPU SIGNALS(PN11660)

Pin No	Signal Name	Function
39	VDD	System Power
20	VSS	System Power
22	PO	Power On Reset
21	SPO	Synchronized Power On
14	W/IO	Write Command and I/O Enable
16	CLKA	System Clock
15	CLK$\overline{B}$	System Clock
17	VCLK	Clock Enable/Disable
19	XTAL I	Crystal In
18	XTAL O	Crystal Out
10	I/D1	Instruction/Data Bus
12	I/D2	Instruction/Data Bus
13	I/D3	Instruction/Data Bus
11	I/D4	Instruction/Data Bus
6	I/D5	Instruction/Data Bus
7	I/D6	Instruction/Data Bus
8	I/D7	Instruction/Data Bus
9	I/D8	Instruction/Data Bus
27	A/B12	Address Bus
28	A/B11	Address Bus
29	A/B10	Address Bus
30	A/B9	Address Bus
31	A/B8	Address Bus
32	A/B7	Address Bus
33	A/B6	Address Bus
34	A/B5	Address Bus
35	A/B4	Address Bus
36	A/B3	Address Bus
37	A/B2	Address Bus
38	A/B1	Address Bus
2	DIA4	Discrete Input Group A
3	DIA3	Discrete Input Group A
4	DIA2	Discrete Input Group A
5	DIA1	Discrete Input Group A
26	DO4	Discrete Output
25	DO3	Discrete Output
24	DO2	Discrete Output
23	DO1	Discrete Output
1	DIO4	Discrete Input/Output
42	DIO3	Discrete Input/Output
41	DIO2	Discrete Input/Output
)	DIO1	Discrete Input/Output

TABLE 3. MEMORY/IO SYSTEM CIRCUIT SIGNALS (PN A17--)

Pin No	Signal Name	Function
28	A/B1	Address Bus
29	A/B2	Address Bus
30	A/B3	Address Bus
31	A/B4	Address Bus
32	A/B5	Address Bus
33	A/B6	Address Bus
34	A/B7	Address Bus
20	A/B8	Address Bus
23	A/B9	Address Bus
21	A/B10	Address Bus
24	A/B11	Address Bus
16	I/D1	Instruction Data Bus
17	I/D2	Instruction Data Bus
18	I/D3	Instruction Data Bus
19	I/D4	Instruction Data Bus
15	I/D5	Instruction Data Bus
10	I/D6	Instruction Data Bus
11	I/D7	Instruction Data Bus
12	I/D8	Instruction Data Bus
26	VDD	Power
22	VSS	Power
9	SPO	Synchronized Power On
27	CLK A	System Clock
25	CLK $\overline{B}$	System Clock
8	I/O 0	Input/Output Port
7	I/O 1	Input/Output Port
6	I/O 2	Input/Output Port
5	I/O 3	Input/Output Port
4	I/O 4	Input/Output Port
3	I/O 5	Input/Output Port
2	I/O 6	Input/Output Port
1	I/O 7	Input/Output Port
42	I/O 8	Input/Output Port
41	I/O 9	Input/Output Port
40	I/O 10	Input/Output Port
39	I/O 11	Input/Output Port
38	I/O 12	Input/Output Port
37	I/O 13	Input/Output Port
36	I/O 14	Input/Output Port
35	I/O 15	Input/Output Port
13	W/IO	Write Command and I/O Enable
14	RRSEL	ROM/RAM Select

SYSTEM SUPPORT

Since the PPS-4/2 software is identical to that of the PPS-4, all of the software development aids on the GE, TYMESHARE, c IBM TSO timesharing systems are directly applicable to the PPS-4/2 System. The existing PPS-4MP Assemulator can be use for assembly and program debugging functions which are independent of the I/O. An evaluation board for the PPS-4/2 Syste which will replace the evaluation board in the PPS-4MP Assemulator will be available to allow the same unit to be used for a system debugging and development. The evaluation board will also be made available to be used in prototype development.

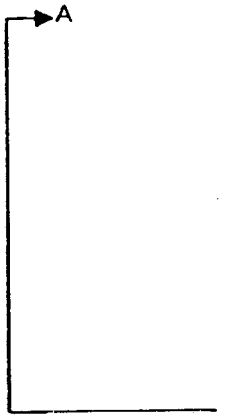
AVAILABILITY

Engineering samples of the PPS-4/2 System will be available in early fall of 1975. The evaluation boards will be available in la fall of 1975 and full production quantities will be available starting in early 1976. Contact Rockwell Internation Microelectronic Device Division for further information.

SAMPLE INPUT/OUTPUT PROGRAMS

The following sample routines show the philosophy of using the PPS-4/2 System input/output capability to control printers ar displays.

PARALLEL PRINTER DRIVER ROUTINE (DRUM TYPE PRINTER)




```
Start with printface row number in "X"        Data to be output is in "PRTDAT"
        LDI 0
        IOL SES                               (DISABLE OUTPUTS)
        .
        .
        .
        LB PRIDAT                             OBTAIN IST DIGIT
A       LAX
        EOR                                   COMPARE WITH PRINTFACE ROW
        SKZ
        LDI 8                                 NO MATCH
        LDI 0                                 MATCH SO ARM HAMMER
        IOL SOS                               VIA IOL
        .
        .
        .
        DECB                                  SEQUENCE TO NEXT DIGIT
        T A
        .
        .
        .
        LDI 8                                 AT PROPER TIME PRINT
        IOL SES                               (ENABLE OUTPUTS)
        .
        .
        .
        RET
```

NOTE

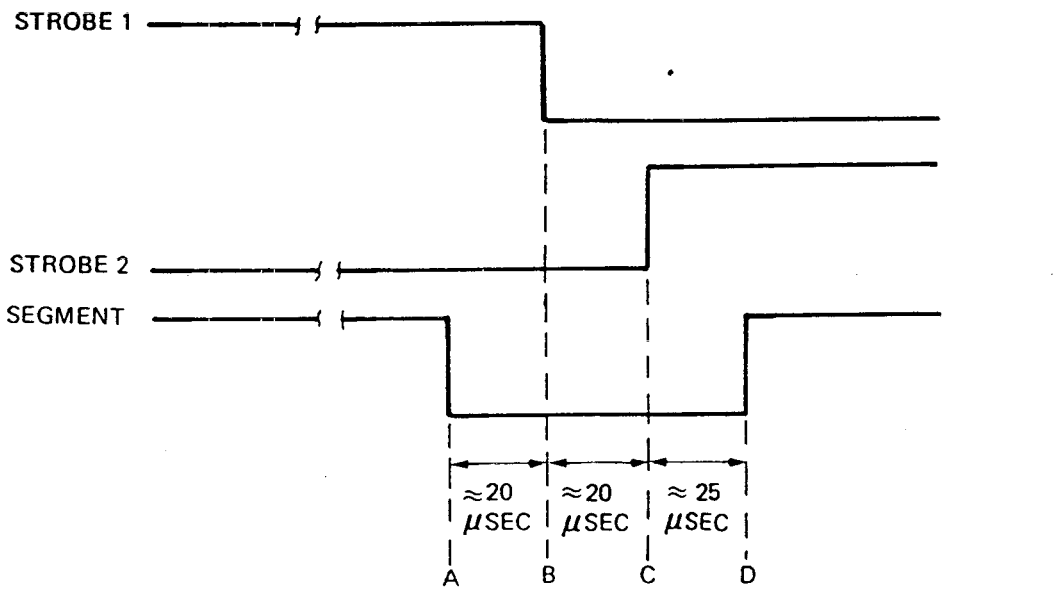
TOTAL TIME TO SET UP 16 COLUMNS

IS 16 x 9 x 5μSEC = 720μSEC

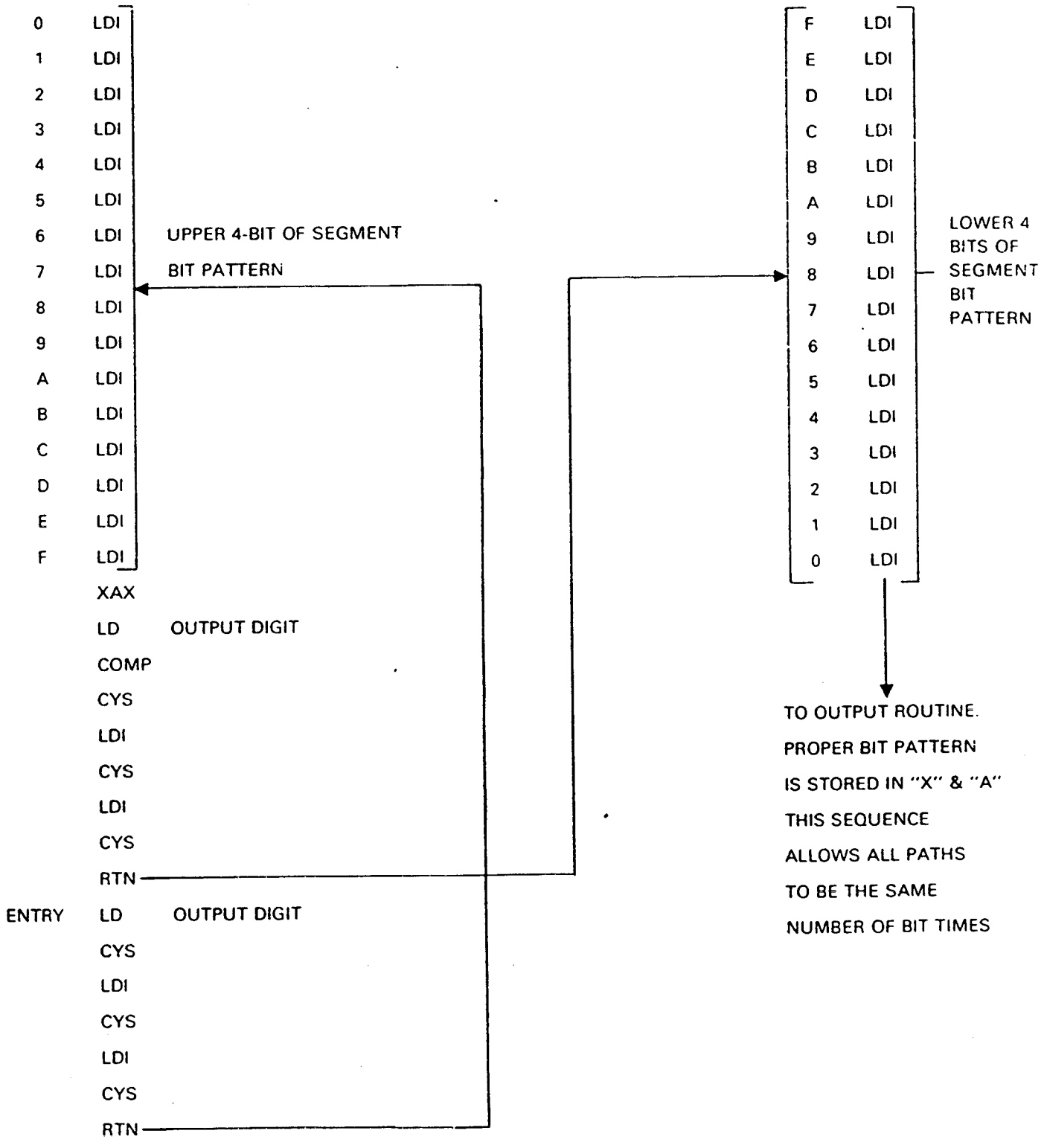
DISPLAY DRIVER ROUTINE

Segment pattern previously determined and stored in RAM at this point.

```
LDI 15          ALL ONES TO A AND X
LXA
DOA             A ←—TURN SEGMENTS OFF
DECB            POINT TO LAST STROBE
LDI 8
IOL SOS         B ←———TURN LAST STROBE OFF
.
.
.
INCB            POINT TO NEW STROBE
LDI 0
IOL SOS         C ←———TURN NEW STROBE ON
.
.
.
LB SEG
EXD             LOAD MOST SIGNIFICANT 4 BITS
LXA             INTO X
LD              LOAD LEAST SIG 4-BITS IN A
DOA             D ←—TURN NEW SEGMENT PATTERN ON
```



PPS SOFTWARE SEGMENT DECODING



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