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RCA Solid State

Microprocessors • Memories • Peripherals



RCA CMOS LSI

Microprocessors, Memories, Peripherals

This DATABOOK contains full information on CMOS LSI products (microprocessors, memories, and peripherals) currently available from RCA Solid State Division. An Index to Products provides a complete listing of types.

The Index to Products is followed by several pages of general product information that includes photographs showing the package options available for RCA CMOS LSI products, a Product Overview that summarizes the basic features and complement of each category of products, and a Product Classification Chart that groups integrated circuits and systems according to product type and intended function. Next, a Cross-Reference Guide lists popular memory integrated circuits supplied by other manufacturers together with a recommended RCA replacement type. The DATABOOK then includes a general discussion of Operating and Handling Considerations for CMOS Integrated Circuits.

Five separate data sections provide definitive ratings, electrical characteristics, and user information for the (1) 1800 series of microprocessors and microcomputers, (2) 1800 series memories, (3) 1800 series peripherals, (4) general-purpose memories, and (5) 6805 series LSI products.

Within each data section, the data pages for individual integrated circuits are grouped in alphabetical sequence of type numbers.

The DATABOOK also contains selected application note abstracts on RCA LSI products and dimensional outlines of all packages in which RCA LSI products are supplied.

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The device data shown for some types are indicated as preliminary, advance, or objective. **Preliminary data** are intended for guidance purposes in evaluating devices for equipment design. Such data are shown for types currently being designed for inclusion in our standard line of commercially available products. **Advance** or **Objective data** are intended for engineering evaluation of types in the initial stages of design. The type designations and data are subject to change, unless otherwise arranged. No obligations are assumed for notice of change or future manufacture of these devices. For current information on the status of preliminary or objective programs, please contact your local RCA sales office.

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Printed in USA/10-82

General Guide to RCA LSI Products **1**

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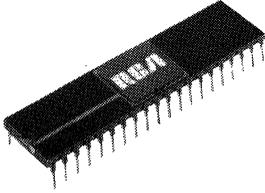
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CDP6805E2	442	8-Bit Micropro/RAM/Ctr/Tmr	1363	MWS5101EL3	412	256 x 4 RAM	1106
CDP6805F2	477	8-Bit Microcomp/ROM/RAM/ Ctr/Tmr	1369	MWS5101ADL2	419	256 x 4 RAM	1207
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Package and Ordering Information

Packages

D Suffix
Dual-In-Line Size-Brazed Ceramic Packages



16-, 18-, 22-, 24-, 28-, and 40-lead versions

D Suffix
Dual-In-Line Welded-Seal Ceramic Packages



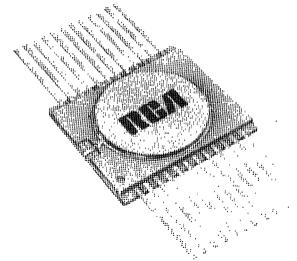
16- and 24-lead versions

E Suffix
Plastic Dual-In-Line Packages

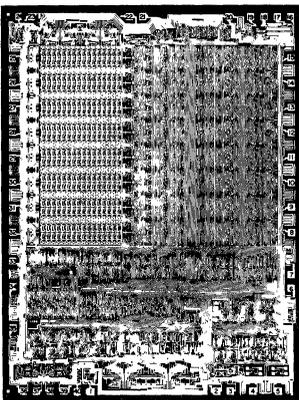


16-, 18-, 22-, 24-, and 40-lead versions

K Suffix
24-Lead Ceramic Flat Pack

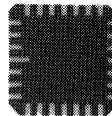
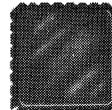


H Suffix Chip



CD4036A and CD4039A only

L SUFFIX — LEADLESS-CHIP-CARRIER CERAMIC PACKAGE



Ordering Information

RCA CMOS microprocessor and memory integrated circuits are available in one or more of the following package styles and are identified by the Suffix Letters indicated: dual-in-line size-brazed ceramic, dual-in-line welded-seal ceramic, dual-in-line plastic, flat-pack ceramic, leadless chip-carrier ceramic and in chip form. The available package styles for any specific type are given in the technical data for that type.

When ordering CMOS devices, it is important that the appropriate suffix letter be affixed to the type number of the device required. For example a CDP1802A in a dual-in-line ceramic package will be identified as the CDP1802AD.

PACKAGE	SUFFIX LETTERS
Dual-In-Line Welded-Seal or Side-Brazed Ceramic	D
Dual-In-Line Plastic	E
Chip	H
Ceramic Flat Pack (CD4036A and CD4039A only)	K
Ceramic Leadless Chip-Carrier	L

Product Overview

RCA offers an all CMOS line of microprocessor, memory and peripheral integrated circuits for use in a broad range of diverse industrial, consumer, and military applications. These devices offer the user all the advantages unique to CMOS technology, including:

- **Low power drain**—makes CMOS integrated circuits a natural choice for battery-operated systems, battery backed-up systems, and systems in which heat dissipation is a prime consideration.
- **High noise immunity and wide operating temperature range (-55° C to +125° C)**—allows CMOS integrated circuits to be used in the most demanding industrial environments.
- **Wide operating voltage range**—reduces the need for expensive regulated power supplies and thereby allows the design engineer greater freedom to concentrate on other aspects of system design.

CDP1800 Series

The RCA CDP1800 series offers the most complete line of CMOS microprocessor and associated memory and peripheral devices in the industry. The heart of the series is the CDP1802A central processing unit (CPU). This unit, which features CMOS register-based architecture, offers 16 internal registers to facilitate data manipulation and to reduce the need for additional devices. The need for external devices is even further reduced by use of an on-chip clock, DMA, and single-phase operation.

The CDP1804A microcomputer, currently under development, incorporates all the features of the CDP1802 augmented by additional hardware and increased performance capabilities. The additional hardware includes 2 kilobytes of ROM, a 64-byte RAM array, an 8-bit presettable down-counter, and 32 additional software instruction, which add subroutine call and return capability, enhance data transfer manipulation, control counter modes and interrupt arbitration, and provide BCD arithmetic capability.

Also available, are four other 8-bit microprocessors that are functional and performance enhancements of the CDP1802. The CDP1805 and CDP1805A feature an on-board RAM and Counter/Timer. The CDP1806 and CDP1806A have all the features of the CDP1805 and CDP1805A, respectively, but contain no on-board RAM.

The microcomputer and microprocessor devices use the CMOS technology, designed on a single chip to maintain low power drain.

RCA's large and expanding CDP1800-series LSI product line offers the system designer exceptional flexibility in hardware/software tradeoffs. In addition to microprocessors and microcomputers, this product line includes a hardware multiply/divide unit (MDU), a programmable I/O, video and keyboard interface circuits, latches and decoders, a universal asynchronous receiver-transmitter (UART), buffers, separators, and a broad complement of directly interfaceable random-access memories (RAM's) and read-only memories (ROM's).

CDP6800 Series

RCA also offers the CDP6800 family, a new series of pin-for-pin replacements for the Motorola MC146805 Series of CMOS microprocessors and peripherals primarily intended for single-chip system applications. This family of parts includes the CDP6805E2 8-bit microprocessor; the CDP6805F2 8-bit microcomputer (1K ROM); the CDP6805G2 8-bit microcomputer (2K ROM); the CDP6818 Real-Time

Clock plus RAM; the CDP6823 Parallel Interface I/O; and the CDP65516 2Kx8 Mask Programmable ROM. Additional types will be added as they become available.

General-Purpose Memories

In addition to the memories designed to interface directly with CDP1800-series microprocessors, RCA also offers a line of general-purpose memories. These memories include small scratchpad types in the CD4000 series, and types in the MWS5000 and CDM series.

Leadless Chip Carrier

RCA's broad CMOS LSI product line now includes 12 standard CDP1800 series chips in leadless chip-carrier packages. This basic chip set will consist of 20, 28, and 44-lead packages on 50-mil lead centers.

Extra-Value Product

Most RCA CDP1800 series parts are offered with burn-in (EVP - Extra-Value Program) and are designated by an "X", "Y" or "Q" suffix added to the part number, e.g., CDM5332EX.

Microprocessor Development Systems and Microboard Computer Modules

For the designers of microprocessor-based equipment and in support of the CDP1800-series microprocessors and associated memory and peripheral circuits, RCA provides a strong and extensive line of systems, system support components, system support software, system modules (including Microboard milliwatt computer systems), and other development aids. The support-system line includes development systems ranging from a minimum tape-based system to a full development system having floppy-disk mass memory storage and operating system software. This line also includes two evaluation systems that serve as convenient learning tools for design, hardware interfacing, and programming of microcomputer systems. These systems can also be used as the basis for breadboarding and prototyping user-designed microcomputer systems.

The RCA Microboard milliwatt computer systems form an extensive line of fully coordinated products based on a standard, simple-to-use 4.5 by 7.5 inch module. These modules feature the inherent CMOS advantages of low power consumption, wide operating voltage range, and excellent noise immunity. The microboard systems are all designed with the microboard universal backplane and are compatible with RCA Development Systems. User-developed systems, therefore, can be readily developed and easily modified.

As a convenient starting point for the user, two microboard prototyping systems are available. These systems include an expandable 5-card chassis, a microboard computer-system module, a microboard control-and-display module, ROM-based utility software, and ample room for user-designed expansion. These prototyping systems enable the user to reduce his hardware concerns to a minimum and to maximize his efforts in custom design and software development to meet the specific requirements of his application.

The RCA Microsystems DATABOOK SSD-270 provides detailed information on RCA Microprocessor-based development systems and Microboard computer modules and in the product description booklets and user manuals available on specific types. (A list of these publications are included at the end of this DATABOOK).

Product Classification Chart

Part Number	Description	Page No.	Part Number	Description	Page No.
Microprocessors			ROMs (Cont'd)		
CDP1802A	8-Bit	14	CDP1834	Mask-programmable ROM 1K x 8	174
CDP1802B	8-Bit	36	CDP1835	Mask-programmable ROM 2K x 8	177
CDP1805C	8-Bit with RAM	84	CDP1837	Mask-programmable ROM 4K x 8	183
CDP1805AC	8-Bit with RAM	103	CDP65516	Mask-programmable ROM 2K x 8	434
CDP1806C	8-Bit with Counter-Timer	84			
CDP1806AC	8-Bit with Counter-Timer	103			
CDP6805E2	8-Bit with RAM/I-O/Counter-Timer	442			
Microcomputers			Input/Output Circuits		
CDP1804A	8-Bit with RAM/ROM/Counter-Timer	56	CDP1851	Programmable I/O (PIO)	190
CDP6805F2	8-Bit with RAM/ROM/I-O/Counter-Timer	477	CDP1852	Byte I/O - 8-Bit I/O Port	203
CDP6805G2	8-Bit with RAM/ROM/I-O/Counter-Timer	503	CDP1853	Decoder - 1 of 8	210
RAMs			CDP1855	Multiply/Divide Unit (MDU)	323
CDP1821	1K x 1	128	CDP1856	Buffer - 4-Bit	245
CDP1822	256 x 4	134	CDP1857	Buffer - 4-Bit	250
CDP1823	128 x 8	141	CDP1858	Latch/Decoder - 4-Bit	250
CDP1824	32 x 8	147	CDP1859	Latch/Decoder - 4-Bit	250
CDP1826	64 x 8	153	CDP1861	Video Display, Controller (VDC)	258
CDM6116	2K x 8	407	CDP1862	Color Generator Circuit	266
MWS5101	256 x 4	412	CDP1863	Programmable Frequency Generator	271
MWS5101A	256 x 4	419	CDP1864	PAL Video Display Controller (VDC)	277
MWS5114	1K x 4	426	CDP1866	Latch/Decoder - 4-Bit	286
CD4036A	4 x 8	376	CDP1867	Latch/Decoder - 4-Bit	286
CD4039A	4 x 8	376	CDP1868	Latch/Decoder - 4-Bit	286
CD4061A	256 x 1	383	CDP1869	Video Interface System (VIS)	295
CD40061A	256 x 1	391	CDP1870	Video Interface System (VIS)	295
CD40114B	16 x 4	396	CDP1871A	Keyboard Encoder, ASCII/Hex	312
ROMs			CDP1872	High-Speed Input Port - 8-Bit	320
CDM5332	Mask-programmable ROM 512 x 8	401	CDP1873	High-Speed Decoder - 1 of 8	325
CDM5333	Mask-programmable ROM 512 x 8	401	CDP1874	High-Speed Input Port - 8-Bit	320
CDP1831	Mask-programmable ROM 512 x 8	160	CDP1875	High-Speed Output Port	320
CDP1832	Mask-programmable ROM 512 x 8	164	CDP1876	Video Interface System (VIS)	295
CDP1833	Mask-programmable ROM 1K x 8	168	CDP1877	Programmable Interrupt Controller	329
CDP1833B	Mask-programmable ROM 1K x 8	168	CDP1878	Dual Counter-Timer	338
			CDP1879	Real Time Clock	351
			CDP1881	Latch/Decoder - 4-Bit	365
			CDP1882	Latch/Decoder - 4-Bit	365
			CDP6818	Real Time Clock with RAM	529
			CDP6823	Parallel Interface	547
			UARTs		
			CDP1854A	UART	214
			CDP6402	Industry Standard UART	367

Cross-Reference Guide

Note: An RCA equivalent type may not be identical with other manufacturer's type in every detail. Refer to published data for further information.

Manufacturer/Type	Description	RCA Nearest Equiv. Type	Pin-for-Pin Compatible
AMI			
S5614	1K x 4 RAM	MWS5114	Yes
S5101	256 x 4 RAM	CDP1822/ MWS5101	Yes
S6508	1K x 1 RAM	CDP1821	Yes
FUJITSU			
MB8414E	1K x 4 RAM	MWS5114	Yes
HARRIS			
6402	UART	CDP6402	Yes
HM6551	256 x RAM	CDP1822/ MWS5101	Yes
HM6508	1K x 1 RAM	CDP1821	Yes
HM6514	1K x 4 RAM	MWS5114	Yes
HITACHI			
HM435101	256 x 4 RAM	CDP1822/ MWS5101	Yes
HM4334	1K x 4 RAM	MWS5114	Yes
HUGHES			
HCMP1802	CPU	GDP1802	Yes
HCMP1822	256 x 4 RAM	CDP1822/ MWS5101	Yes
HCMP1824	32 x 8 RAM	CDP1824	Yes
HCMP1831	512 x 8 ROM	CDP1831	Yes
HCMP1832	512 x 8 ROM	CDP1832	Yes
HCMP1833	1K x 8 ROM	CDP1833	Yes
HCMP1834	1K x 8 ROM	CDP1834	Yes
HCMP1835	2K x 8 ROM	CDP1835	Yes
HCMP1851	I/O Interface	CDP1851	Yes
HCMP1852	I/O Port	CDP1852	Yes
HCMP1853	N-Bit Decoder	CDP1853	Yes
HCMP1854	UART	CDP1854	Yes
HCMP1855	8-Bit MDU	CDP1855	Yes
HCMP1856/ 1857	Bus Buffer	CDP1856/ CDP1857/	Yes
HCMP1858/ 1859	Latch/ Decoder	CDP1858/	Yes
HCMP1861	VDC	CDP1861	Yes
HCMP1871	Keyboard Encoder	CDP1871	Yes

Manufacturer/Type	Description	RCA Nearest Equiv. Type	Pin-for-Pin Compatible
INTERSIL			
IM6402	UART	CDP6402	Yes
IM6551	256 x 4 RAM	CDP1822/ MWS5101	Yes
IM6514C	1K x 4 RAM	MWS5114	Yes
IM6316	2K x 8 ROM	CDP1835	No
MITEL			
MD74SC138A	Decoder	CDP1873C	Yes
MD74SC373A	I/O Port	CDP1872C/ CDP1874C	No
MOTOROLA			
MCM6508	1K x 1 RAM	CDP1821	Yes
MCM5101	256 x 4 RAM	CDP1822/ MWS5101	Yes
MCM65114	1K x 4 RAM	MWS5114	Yes
NATIONAL			
MM74C920	256 x 4 RAM	CDP1822/ MWS5101	No
MM74C929	1K x 1 RAM	CDP1821	Yes
NEC			
PD5101	256 x 4 RAM	CDP1822/ MWS5101	Yes
PD44/6514	1k x 4 RAM	MWS5114	Yes
OKI			
MSM5114	1K x 4 RAM	MWS5114	Yes
SSS			
SCM5101	256 x 4 RAM	CDP1822/ MWS5101	Yes
SCM5114	1K x 4 RAM	MWS5114	Yes
	2K x 8 ROM	CDP1835	No
SUPERTEX			
CM1600	2K x 8 ROM	CDP1835	No
TOSHIBA			
TC5514P	1K x 4 RAM	MWS5114	Yes
TC5501P	256 x 4 RAM	CDP1822/ MWS5101	Yes
TC5508P	1K x 1 RAM	CDP1821	No
TC5507AP	1K x 4 RAM	MWS5114	No

Operating and Handling Considerations

RCA CMOS Integrated Circuits

This Note summarizes important operating recommendations and precautions which should be followed in the interest of maintaining the high standards of performance of solid state devices.

The ratings included in RCA Solid State Devices data bulletins are based on the Absolute Maximum Rating System, which is defined by the following Industry Standard (JEDEC) statement:

Absolute-Maximum Ratings are limiting values of operating and environmental conditions applicable to any electron device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

The device manufacturer chooses these values to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in device characteristics.

The equipment manufacturer should design so that initially and throughout life no absolute-maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in device characteristics.

It is recommended that equipment manufacturers consult RCA whenever device applications involve unusual electrical, mechanical or environmental operating conditions.

General Considerations

The design flexibility provided by these devices makes possible their use in a broad range of applications and under many different operating conditions. When incorporating these devices in equipment, therefore, designers should anticipate the rare possibility of device failure and make certain that no safety hazard would result from such an occurrence.

The small size of most solid state products provides obvious advantages to the designers of electronic equipment. However, it should be recognized that these compact devices usually provide only relatively small insulation area between adjacent leads and the metal envelope. When these devices are used in moist or contaminated atmospheres, therefore, supplemental protection must be provided to prevent the development of electrical conductive paths across the relatively small insulating surfaces.

The metal shells of the TO-5 style package often used for integrated circuits usually has the substrate or most negative supply voltage connected to the case. Therefore, consideration should be given to the possibility of shock hazard if the shells are to operate at voltages appreciably above or below ground potential. In general, in any application in which devices are operated at voltages which may be dangerous to personnel, suitable

precautionary measures should be taken to prevent direct contact with these devices.

Devices should not be connected into or disconnected from circuits with the power on because high transient voltages may cause permanent damage to the devices.

TESTING PRECAUTIONS

In common with many electronic components, solid-state devices should be operated and tested in circuits which have reasonable values of current limiting resistance, or other forms of effective current overload protection. Failure to observe these precautions can cause excessive internal heating of the device resulting in destruction and/or possible shattering of the enclosure.

Mounting

Integrated circuits are normally supplied with lead-tin plated leads to facilitate soldering into circuit boards. In those relatively few applications requiring welding of the device leads, rather than soldering, the devices may be obtained with gold or nickel plated Kovar[■] leads.* It should be recognized that this type of plating will not provide complete protection against lead corrosion in the presence of high humidity and mechanical stress.

■Trade Name: Westinghouse Corp.

*Mil-M-38510A, paragraph 3.5.6.1(a), lead material

The aluminum-foil-lined cardboard "sandwich pack" employed for static protection of the flat-pack also provides some additional protection against lead corrosion, and it is recommended that the devices be stored in this package until used.

When integrated circuits are welded onto printed circuit boards or equipment, the presence of moisture between the closely spaced terminals can result in conductive paths that may impair device performance in high-impedance applications. It is therefore recommended that conformal coatings or potting be provided as an added measure of protection against moisture penetration.

In any method of mounting integrated circuits which involves bending or forming of the device leads, it is extremely important that the lead be supported and clamped between the bend and the package seal, and that bending be done with care to avoid damage to lead plating. In no case should the radius of the bend be less than the diameter of the lead, or in the case of rectangular leads, such as those used in RCA 14-lead and 16-lead flat-packages, less than the lead thickness. It is also extremely important that the ends of the bent leads be straight to assure proper insertion through the holes in the printed-circuit board.

Handling

All CMOS gate inputs have a resistor/diode gate protection network. All transmission gate inputs and all outputs have diode protection provided by inherent p-n junction diodes. These diode networks at input and

Operating and Handling Considerations (Cont'd)

output interfaces protect CMOS devices from gate-oxide failure in handling environments where static discharge is not excessive. In low-temperature, low-humidity environments, improper handling may result in device damage. See ICAN-6525, "Handling and Operating Considerations for MOS Integrated Circuits", for proper handling procedures.

Operating

Unused Inputs

All unused input leads must be connected to either V_{SS} or V_{DD} , whichever is appropriate for the logic circuit involved. A floating input on a high-current type not only can result in faulty logic operation, but can cause the maximum power dissipation of 200 milliwatts to be exceeded and may result in damage to the device. Inputs to these types, which are mounted on printed-circuit boards that may temporarily become unterminated, should have a pull-up resistor to V_{SS} or V_{DD} . A useful range of values for such resistors is from 10 kilohms to 1 megohm.

Input Signals

Signals shall not be applied to the inputs while the device power supply is off unless the input current is limited to a steady state value of less than 10 milliamperes. Input currents of less than 10 milliamperes prevent device damage; however, proper operation may be impaired as a result of current flow through structural diode junctions.

Output Short Circuits

Shorting of outputs to V_{SS} or V_{DD} can damage many of the higher-output-current CMOS types. In general, these types can all be safely shorted for supplies up to 5 volts, but will be damaged (depending on type) at higher power-supply voltages. For cases in which a short-circuit load, such as the base of a p-n-p or an n-p-n bipolar transistor,

is directly driven, the device output characteristics given in the published data should be consulted to determine the requirements for a safe operation below 200 milliwatts.

For detailed CMOS IC operating and handling considerations, refer to Application Note ICAN-6525 "Handling and Operating Considerations for MOS Integrated circuits".

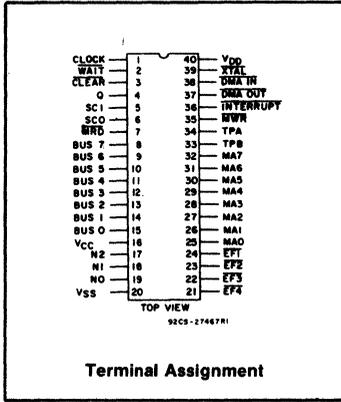
IC Chips

Integrated-circuit chips, unlike packaged devices, are non-hermetic devices, normally fragile and small in physical size, and therefore, require special handling considerations as follows:

1. Chips must be stored under proper conditions to insure that they are not subjected to a moist and/or contaminated atmosphere that could alter their electrical, physical, or mechanical characteristics. After the shipping container is opened, the chip must be stored under the following conditions:
 - A. Storage temperature, 40° C.
 - B. Relatively humidity, 50% max.
 - C. Clean, dust-free environment.
2. The user must exercise proper care when handling chips to prevent even the slightest physical damage to the chip.
3. During mounting and lead bonding of chips the user must use proper assembly techniques to obtain proper electrical, thermal, and mechanical performance.
4. After the chip has been mounted and bonded, any necessary procedure must be followed by the user to insure that these non-hermetic chips are not subjected to moist or contaminated atmosphere which might cause the development of electrical conductive paths across the relatively small insulating surfaces. In addition, proper consideration must be given to the protection of these devices from other harmful environments which could conceivably adversely affect their proper performance.

**1800-Series
Microprocessors and Microcomputers
Technical Data** **2**

CDP1802A, CDP1802AC



CMOS 8-Bit Microprocessor

Features:

- Minimum instruction fetch-execute time of 5 μ s or 7.5 μ s at $V_{DD}=5$ V: 2.5 μ s or 3.75 μ s at $V_{DD}=10$ V
- Any combination of standard RAM and ROM up to 65,536 bytes
- Operates with slow memories, up to 1 μ s access time at $f_{CL}=4$ MHz
- 8-bit parallel organization with bidirectional data bus and multiplexed address bus
- 16 x 16 matrix of registers for use as multiple program counters, data pointers, or data registers
- On-chip DMA, interrupt, and flag inputs
- Programmable single-bit output port
- 91 easy-to-use instructions

The RCA-CDP1802A LSI CMOS 8-bit register-oriented central-processing unit (CPU) is designed for use as a general-purpose computing or control element in a wide range of stored-program systems or products.

The CDP1802A includes all of the circuits required for fetching, interpreting, and executing instructions which have been stored in standard types of memories. Extensive input/output (I/O) control features are also provided to facilitate system design.

The 1800 series architecture is designed with emphasis on the total microcomputer system as an integral entity so that systems having maximum flexibility and minimum cost can be realized. The 1800 series CPU also provides a syn-

chronous interface to memories and external controllers for I/O devices, and minimizes the cost of interface controllers. Further, the I/O interface is capable of supporting devices operating in polled, interrupt-driven, or direct memory-access modes.

The CDP1802A and CDP1802AC are functionally identical. They differ in that the CDP1802A has a recommended operating voltage range of 4 to 10.5 volts, and the CDP1802AC a recommended operating voltage range of 4 to 6.5 volts.

These types are supplied in 40-lead dual-in-line side-braced ceramic packages (D suffix), and 40-lead dual-in-line plastic packages (E suffix). The CDP1802AC is also available in chip form (H suffix).

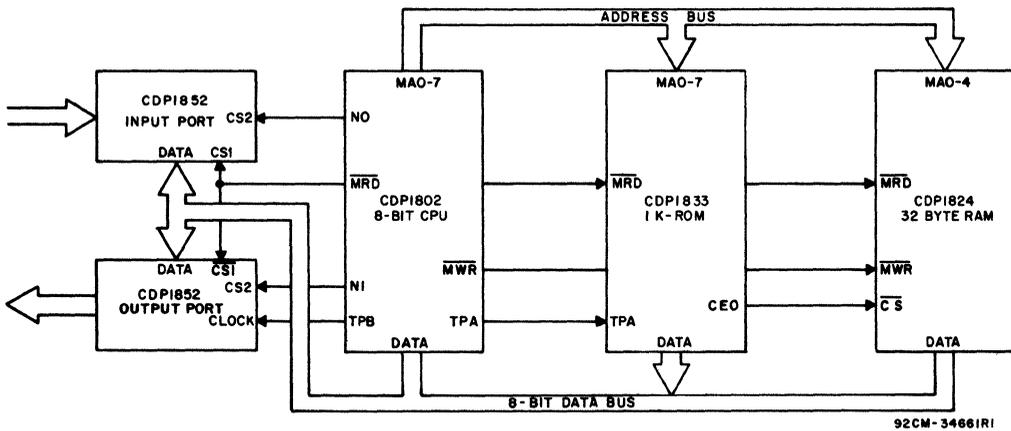


Fig. 1 - Typical CDP1802A small microprocessor system.

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD}):

(All voltages referenced to V_{SS} terminal)

CDP1802A	-0.5 to +11 V
CDP1802AC	-0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to V _{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA

POWER DISSIPATION PER PACKAGE (P_D):

For T _A =-40 to +60°C (PACKAGE TYPE E)	500 mW
For T _A =+60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T _A =-55 to +100°C (PACKAGE TYPE D)	500 mW
For T _A =+100 to +125°C (PACKAGE TYPE D)	Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T _A =FULL PACKAGE-TEMPERATURE RANGE	100 mW
--	--------

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPE D	-55 to +125°C
PACKAGE TYPE E	-40 to +85°C

STORAGE TEMPERATURE RANGE (T_{stg})

.....	-65 to +150°C
-------	---------------

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16±1/32 in. (1.59±0.79 mm) from case for 10 s max.	+265°C
---	--------

OPERATING CONDITIONS at T_A=-40°C to +85°C

For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	CONDITIONS		LIMITS				UNITS
	V _{CC1} (V)	V _{DD} (V)	CDP1802A		CDP1802AC		
			Min.	Max.	Min.	Max.	
DC Operating Voltage Range	—	—	4	10.5	4	6.5	V
Input Voltage Range	—	—	V _{SS}	V _{DD}	V _{SS}	V _{DD}	
Maximum Clock Input Rise or Fall Time, t _r , t _f	4 to 10.5	4 to 10.5	—	1	—	1	μs
Minimum Instruction Time ²	5	5	5	—	5	—	
	5	10	4	—	—	—	
Maximum DMA Transfer Rate	5	5	—	400	—	400	KBytes per second
	5	10	—	500	—	—	
	10	10	—	800	—	—	
Maximum Clock Input Frequency, f _{CL} , Load Capacitance (C _L)=50 pF	5	5	DC	3.2	DC	3.2	MHz
	5	10	DC	4	—	—	
	10	10	DC	6.4	—	—	

¹V_{CC} must never exceed V_{DD}.

²Equals 2 machine cycles—one Fetch and one Execute operation for all instructions except Long Branch and Long Skip, which require 3 machine cycles—one Fetch and two Execute operations.

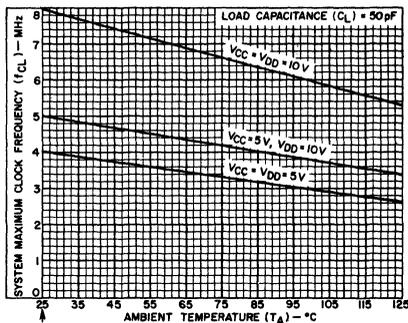


Fig. 2 - Typical maximum clock frequency as a function of temperature.

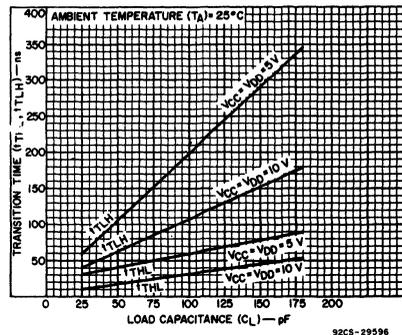


Fig. 3 - Typical transition time vs. load capacitance.

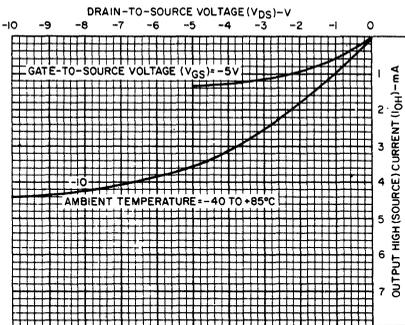
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CDP1802A, CDP1802AC

STATIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, except as noted.

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
	V _{OUT} (V)	V _{IN} (V)	V _{CC} , V _{DD} (V)	CDP1802A			CDP1802AC			
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device Current I _{DD}	—	—	5	—	0.1	50	—	1	200	μA
	—	—	10	—	1	200	—	—	—	
Output Low Drive (Sink) Current I _{OL} (Except XTAL)	0.4	0.5	5	1.1	2.2	—	1.1	2.2	—	mA
	0.5	0.10	10	2.2	4.4	—	—	—	—	
XTAL I _{OL}	0.4	5	5	170	350	—	170	350	—	μA
Output High Drive (Source) Current I _{OH} (Except XTAL)	4.6	0.5	5	-0.27	-0.55	—	-0.27	-0.55	—	mA
	9.5	0.10	10	-0.55	-1.1	—	—	—	—	
XTAL I _{OH}	4.6	0	5	-125	-250	—	-125	-250	—	μA
Output Voltage Low-Level V _{OL}	—	0.5	5	—	0	0.1	—	0	0.1	V
	—	0.10	10	—	0	0.1	—	—	—	
Output Voltage High Level V _{OH}	—	0.5	5	4.9	5	—	4.9	5	—	V
	—	0.10	10	9.9	10	—	—	—	—	
Input Low Voltage V _{IL}	0.5, 4.5	—	5	—	—	1.5	—	—	1.5	V
	0.5, 4.5	—	5, 10	—	—	1	—	—	—	
	1.9	—	10	—	—	3	—	—	—	
Input High Voltage V _{IH}	0.5, 4.5	—	5	3.5	—	—	3.5	—	—	V
	0.5, 4.5	—	5, 10	4	—	—	4	—	—	
	1.9	—	10	7	—	—	—	—	—	
CLEAR Input Voltage Schmitt Hysteresis V _H	—	—	5	0.4	0.5	—	0.4	0.5	—	V
	—	—	5, 10	0.3	0.4	—	—	—	—	
	—	—	10	1.5	2	—	—	—	—	
Input Leakage Current I _{IN}	Any Input	0.5	5	—	$\pm 10^{-4}$	± 1	—	$\pm 10^{-4}$	± 1	μA
		0.10	10	—	$\pm 10^{-4}$	± 1	—	—	—	
3-State Output Leakage Current I _{OUT}	0.5	0.5	5	—	$\pm 10^{-4}$	± 1	—	$\pm 10^{-4}$	± 1	μA
	0.10	0.10	10	—	$\pm 10^{-4}$	± 1	—	—	—	
Operating Current, I _{DD1} ^Δ f=3.2 MHz	—	—	5	—	2	4	—	2	4	mA
Minimum Data Retention Voltage V _{DR}	V _{DD} =V _{DR}			—	2	2.4	—	2	2.4	V
Data Retention Current I _{DR}	V _{DD} =2.4 V			—	0.05	—	—	0.5	—	μA
Input Capacitance C _{IN}				—	5	7.5	—	5	7.5	pF
Output Capacitance C _{OUT}				—	10	15	—	10	15	

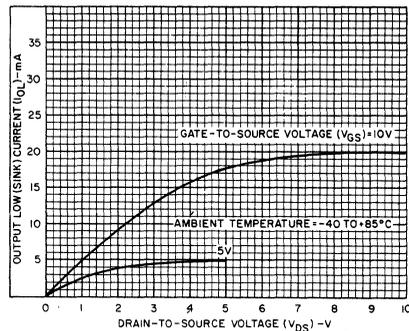
*Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD}.

^ΔIdle "00" at M(0000), C_L=50 pF.



92CS-31863

Fig. 4 - Minimum output high (source) current characteristics.

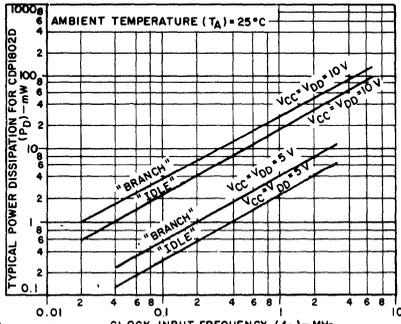


92CS-31864

Fig. 5 - Minimum output low (sink) current characteristics.

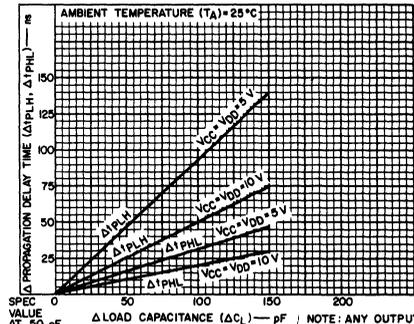
1800-Series Microprocessors and Microcomputers

CDP1802A, CDP1802AC



NOTES:
 IDLE = "00" AT M(0000)
 BRANCH = "3707" AT M(8107)
 CL = 50 pF
 92CS-29549

Fig. 6 - Typical power dissipation as a function of clock frequency for BRANCH instruction and IDLE instruction.



NOTE: ANY OUTPUT EXCEPT XTAL
 92CS-29598

Fig. 7 - Typical change in propagation delay as a function of a change in load capacitance.

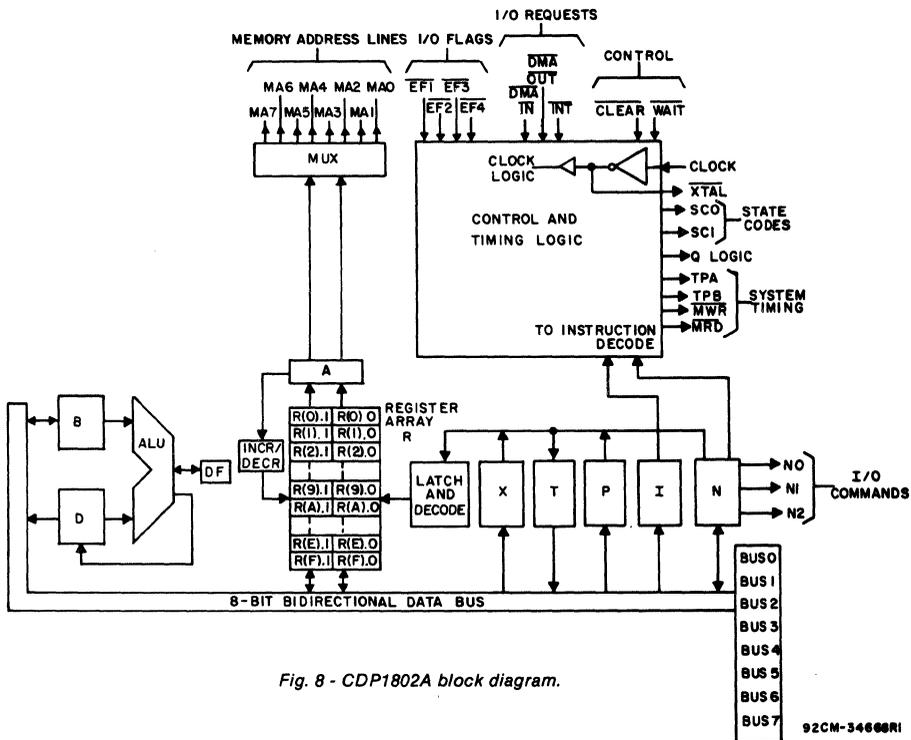


Fig. 8 - CDP1802A block diagram.

92CM-34668R1

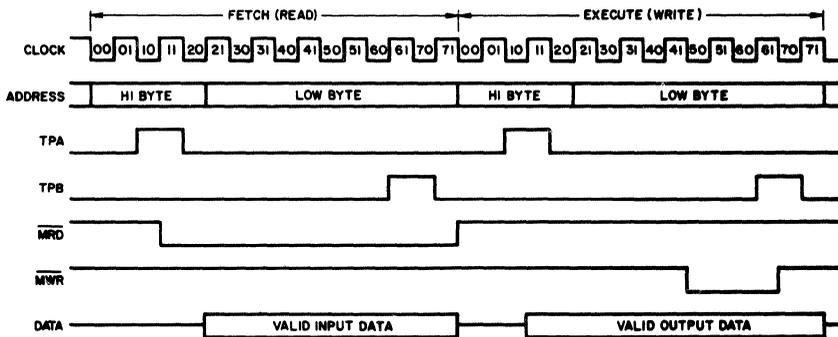


Fig. 9 - Basic dc timing waveforms, one instruction cycle.

92CM-33368

SIGNAL DESCRIPTIONS

BUS 0 to BUS 7 (Data Bus):

8-bit bidirectional DATA BUS lines. These lines are used for transferring data between the memory, the microprocessor, and I/O devices.

N0 to N2 (I/O Lines):

Activated by an I/O instruction to signal the I/O control logic of a data transfer between memory and I/O interface. These lines can be used to issue command codes or device selection codes to the I/O devices (independently or combined with the memory byte on the data bus when an I/O instruction is being executed). The N bits are low at all times except when an I/O instruction is being executed. During this time their state is the same as the corresponding bits in the N register.

The direction of data flow is defined in the I/O instruction by bit N3 (internally) and is indicated by the level of the MRD signal.

MRD=VCC: Data from I/O to CPU and Memory

MRD=VSS: Data from Memory to I/O

EF1 to EF4 (4 Flags):

These inputs enable the I/O controllers to transfer status information to the processor. The levels can be tested by the conditional branch instructions. They can be used in conjunction with the INTERRUPT request line to establish interrupt priorities. These flags can also be used by I/O devices to "call the attention" of the processor, in which case the program must routinely test the status of these flag(s). The flag(s) are sampled at the beginning of every S1 cycle.

INTERRUPT, DMA-IN, DMA-OUT (3 I/O Requests)

These inputs are sampled by the CDP1802A during the interval between the leading edge of TPB and the leading edge of TPA.

Interrupt Action: X and P are stored in T after executing current instruction; designator X is set to 2; designator P is set to 1; interrupt enable is reset to 0 (inhibit); and instruction execution is resumed. The interrupt action requires one machine cycle (S3).

DMA Action: Finish executing current instruction; R(0) points to memory area for data transfer; data is loaded into or read out of memory; and increment R(0).

Note: In the event of concurrent DMA and Interrupt requests, DMA-IN has priority followed by DMA-OUT and then Interrupt.

SC0, SC1, (2 State Code Lines):

These outputs indicate that the CPU is: 1) fetching an instruction, or 2) executing an instruction, or 3) processing a DMA request, or 4) acknowledging an interrupt request. The levels of state code are tabulated below. All states are valid at TPA. H=VCC, L=VSS.

State Type	State Code Lines	
	SC1	SC0
S0 (Fetch)	L	L
S1 (Execute)	L	H
S2 (DMA)	H	L
S3 (Interrupt)	H	H

TPA, TPB (2 Timing Pulses):

Positive pulses that occur once in each machine cycle (TPB follows TPA). They are used by I/O controllers to interpret codes and to time interaction with the data bus. The trailing edge of TPA is used by the memory system to latch the higher-order byte of the 16-bit memory address. TPA is suppressed in IDLE when the CPU is in the load mode.

MA0 to MA7 (8 Memory Address Lines):

In each cycle, the higher-order byte of a 16-bit CPU memory address appears on the memory address lines MA0-7 first. Those bits required by the memory system can be strobed into external address latches by timing pulse TPA. The low-order byte of the 16-bit address appears on the address lines after the termination of TPA. Latching of all 8 higher-order address bits would permit a memory system of 64K bytes.

MWR (Write Pulse):

A negative pulse appearing in a memory-write cycle, after the address lines have stabilized.

MRD (Read Level):

A low level on MRD indicates a memory read cycle. It can be used to control three-state outputs from the addressed memory which may have a common data input and output bus. If a memory does not have a three-state high-impedance output, MRD is useful for driving memory/bus separator gates. It is also used to indicate the direction of data transfer during an I/O instruction. For additional information see Table I.

Q:

Single bit output from the CPU which can be set or reset under program control. During SEQ or REQ instruction execution, Q is set or reset between the trailing edge of TPA and the leading edge of TPB.

CLOCK:

Input for externally generated single-phase clock. A typical clock frequency is 6.4 MHz at VCC=VDD=10 volts. The clock is counted down internally to 8 clock pulses per machine cycle.

XTAL:

Connection to be used with clock input terminal, for an external crystal, if the on-chip oscillator is utilized. The crystal is connected between terminals 1 and 39 (CLOCK and XTAL) in parallel with a resistance (10 megohms typ.). Frequency trimming capacitors may be required at terminals 1 and 39. For additional information, see ICAN-6565.

WAIT, CLEAR (2 Control Lines):

Provide four control modes as listed in the following truth table:

CLEAR	WAIT	MODE
L	L	LOAD
L	H	RESET
H	L	PAUSE
H	H	RUN

VDD, VSS, VCC (Power Levels):

The internal voltage supply VDD is isolated from the Input/Output voltage supply VCC so that the processor may operate at maximum speed while interfacing with peripheral devices operating at lower voltage. VCC must be less than or equal to VDD. All outputs swing from VSS to VCC. The recommended input voltage swing is VSS to VCC.

ARCHITECTURE

The CPU block diagram is shown in Fig. 8. The principal feature of this system is a register array (R) consisting of sixteen 16-bit scratchpad registers. Individual registers in the array (R) are designated (selected) by a 4-bit binary code from one of the 4-bit registers labeled N, P, and X. The contents of any register can be directed to any one of the following three paths:

1. the external memory (multiplexed, higher-order byte first, on to 8 memory address lines);
2. the D register (either of the two bytes can be gated to D);
3. the increment/decrement circuit where it is increased or decreased by one and stored back in the selected 16-bit register.

The three paths, depending on the nature of the instruction, may operate independently or in various combinations in the same machine cycle.

With two exceptions, CPU instructions consist of two 8-clock-pulse machine cycles. The first cycle is the fetch cycle, and the second—and third if necessary—are execute cycles. During the fetch cycle the four bits in the P designator select one of the 16 registers R(P) as the current program counter. The selected register R(P) contains the address of the memory location from which the instruction is to be fetched. When the instruction is read out from the memory, the higher-order 4 bits of the instruction byte are loaded into the I register and the lower-order 4 bits into the N register. The content of the program counter is automatically incremented by one so that R(P) is now "pointing" to the next byte in the memory.

The X designator selects one of the 16 registers R(X) to "point" to the memory for an operand (or data) in certain ALU or I/O operations.

The N designator can perform the following five functions depending on the type of instruction fetched:

1. designate one of the 16 registers in R to be acted upon during register operations;
2. indicate to the I/O devices a command code or device-selection code for peripherals;
3. indicate the specific operation to be executed during the ALU instructions, types of tests to be performed during the Branch instructions, or the specific operation required in a class of miscellaneous instructions (70-73 and 78-7B);
4. indicate the value to be loaded into P to designate a new register to be used as the program counter R(P);
5. indicate the value to be loaded into X to designate a new register to be used as data pointer R(X).

The registers in R can be assigned by a programmer in three different ways: as program counters, as data pointers, or as scratchpad locations (data registers) to hold two bytes of data.

Program Counters

Any register can be the main program counter; the address of the selected register is held in the P designator. Other registers in R can be used as subroutine program counters. By a single instruction the contents of the P register can be changed to effect a "call" to a subroutine. When interrupts are being serviced, register R(1) is used as the program counter for the user's interrupt servicing routine. After reset, and during a DMA operation, R(0) is used as the program counter. At all other times the register designated as program counter is at the discretion of the user.

Data Pointers

The registers in R may be used as data pointers to indicate a location in memory. The register designated by X (i.e., R(X)) points to memory for the following instructions (see Table I):

1. ALU operations F1-F5, F7, 74, 75, 77;
2. output instructions 61 through 67;
3. input instructions 69 through 6F;
4. certain miscellaneous instructions — 70-73, 78, 60, F0.

The register designated by N (i.e., R(N)) points to memory for the "load D from memory" instructions 0N and 4N and the "Store D" instruction 5N. The register designated by P (i.e., the program counter) is used as the data pointer for ALU instructions F8-FD, FF, 7C, 7D, 7F. During these instruction executions, the operation is referred to as "data immediate".

Another important use of R as a data pointer supports the built-in Direct-Memory-Access (DMA) function. When a DMA-In or DMA-Out request is received, one machine cycle is "stolen". This operation occurs at the end of the execute machine cycle in the current instruction. Register R(0) is always used as the data pointer during the DMA operation. The data is read from (DMA-Out) or written into (DMA-In) the memory location pointed to by the R(0) register. At the end of the transfer, R(0) is incremented by one so that the processor is ready to act upon the next DMA byte transfer request. This feature in the 1800-series architecture saves a substantial amount of logic when fast exchanges of blocks of data are required, such as with magnetic discs or during CRT-display-refresh cycles.

Data Registers

When registers in R are used to store bytes of data, four instructions are provided which allow D to receive from or write into either the higher-order- or lower-order-byte portions of the register designated by N. By this mechanism (together with loading by data immediate) program pointer and data pointer designations are initialized. Also, this technique allows scratchpad registers in R to be used to hold general data. By employing increment or decrement instructions, such registers may be used as loop counters.

The Q Flip Flop

An internal flip flop, Q, can be set or reset by instruction and can be sensed by conditional branch instructions. The output of Q is also available as a microprocessor output.

Interrupt Servicing

Register R(1) is always used as the program counter whenever interrupt servicing is initiated. When an interrupt request occurs and the interrupt is allowed by the program (again, nothing takes place until the completion of the current instruction), the contents of the X and P registers are stored in the temporary register T, and X and P are set to new values; hex digit 2 in X and hex digit 1 in P. Interrupt Enable is automatically de-activated to inhibit further interruptions. The user's interrupt routine is now in control; the contents of T may be saved by means of a single instruction (78) in the memory location pointed to by R(X). At the conclusion of the interrupt, the user's routine may restore the pre-interrupted value of X and P with a single instruction (70 or 71). The Interrupt-Enable flip flop can be activated to permit further interrupts or can be disabled to prevent them.

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CDP1802A, CDP1802AC

CPU Register Summary

D	8 Bits	Data Register (Accumulator)
DF	1 Bit	Data Flag (ALU Carry)
B	8 Bits	Auxiliary Holding Register
R	16 Bits	1 of 16 Scratchpad Registers
P	4 Bits	Designates which register is Program Counter
X	4 Bits	Designates which register is Data Pointer

N	4 Bits	Holds Low-Order Instr. Digit
I	4 Bits	Holds High-Order Instr. Digit
T	8 Bits	Holds old X, P after Interrupt (X is high nibble)
IE	1 Bit	Interrupt Enable
Q	1 Bit	Output Flip Flop

CDP1802 Control Modes

The **WAIT** and **CLEAR** lines provide four control modes as listed in the following truth table:

CLEAR	WAIT	MODE
L	L	LOAD
L	H	RESET
H	L	PAUSE
H	H	RUN

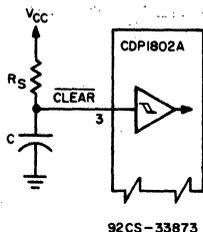
The function of the modes are defined as follows:

Load

Holds the CPU in the IDLE execution state and allows an I/O device to load the memory without the need for a "bootstrap" loader. It modifies the IDLE condition so that DMA-IN operation does not force execution of the next instruction.

Reset

Registers I, N, Q are reset, IE is set and 0's (V_{SS}) are placed on the data bus. TPA and TPB are suppressed while reset is held and the CPU is placed in S1. The first machine cycle after termination of reset is an initialization cycle which requires 9 clock pulses. During this cycle the CPU remains in S1 and registers X, P, and R(0) are reset. Interrupt and DMA servicing are suppressed during the initialization cycle. The next cycle is an S0, S1, or an S2 but never an S3. With the use of a 71 instruction followed by 00 at memory locations 0000 and 0001, this feature may be used to reset IE, so as to preclude interrupts until ready for them. Powerup reset can be realized by connecting an RC network directly to the CLEAR pin, since it has a Schmitt-triggered input, see Fig. 10.



The RC time constant should be greater than the oscillator start-up time (typically 20 ms).

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Fig. 10 - Reset diagram.

Pause

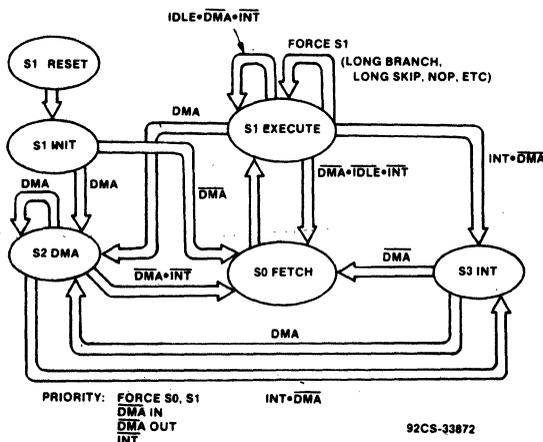
Stops the internal CPU timing generator on the first negative high-to-low transition of the input clock. The oscillator continues to operate, but subsequent clock transitions are ignored.

Run

May be initiated from the Pause or Reset mode functions. If initiated from Pause, the CPU resumes operation on the first negative high-to-low transition of the input clock. When initiated from the Reset operation, the first machine cycle following Reset is always the initialization cycle. The initialization cycle is then followed by a DMA (S2) cycle or fetch (S0) from location 0000 in memory.

RUN-MODE STATE TRANSITIONS

The CDP1802A CPU state transitions when in the RUN and RESET modes are shown in Fig. 11. Each machine cycle requires the same period of time, 8 clock pulses, except the initialization cycle, which requires 9 clock pulses. The execution of an instruction requires either two or three machine cycles, S0 followed by a single S1 cycle or two S1 cycles. S2 is the response to a DMA request and S3 is the interrupt response. Table II shows the conditions on Data Bus and Memory-Address lines during all machine states.



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Fig. 11 - State transition diagram.

INSTRUCTION SET

The CPU instruction summary is given in Table I. Hexadecimal notation is used to refer to the 4-bit binary codes.

In all registers bits are numbered from the least significant bit (LSB) to the most significant bit (MSB) starting with 0.

R(W): Register designated by W, where
W=N or X, or P

R(W).0: Lower-order byte of R(W)
R(W).1: Higher-order byte of R(W)

Operation Notation
 $M(R(N)) \rightarrow D; R(N) + 1 \rightarrow R(N)$

This notation means: The memory byte pointed to by R(N) is loaded into D, and R(N) is incremented by 1.

TABLE I — INSTRUCTION SUMMARY (See Notes following table, pp. 11 and 12)

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
MEMORY REFERENCE			
LOAD VIA N	LDN	0N	$M(R(N)) \rightarrow D$; FOR N NOT 0
LOAD ADVANCE	LDA	4N	$M(R(N)) \rightarrow D$; $(R(N)+1) \rightarrow R(N)$
LOAD VIA X	LDX	F0	$M(R(X)) \rightarrow D$
LOAD VIA X AND ADVANCE	LDXA	72	$M(R(X)) \rightarrow D$; $R(X)+1 \rightarrow R(X)$
LOAD IMMEDIATE	LDI	F8	$M(R(P)) \rightarrow D$; $R(P)+1 \rightarrow R(P)$
STORE VIA N	STR	5N	$D \rightarrow M(R(N))$
STORE VIA X AND DECREMENT	STXD	73	$D \rightarrow M(R(X))$; $R(X)-1 \rightarrow R(X)$
REGISTER OPERATIONS			
INCREMENT REG N	INC	1N	$R(N)+1 \rightarrow R(N)$
DECREMENT REG N	DEC	2N	$R(N)-1 \rightarrow R(N)$
INCREMENT REG X	IRX	60	$R(X)+1 \rightarrow R(X)$
GET LOW REG N	GLO	8N	$R(N).0 \rightarrow D$
PUT LOW REG N	PLO	AN	$D \rightarrow R(N).0$
GET HIGH REG N	GHI	9N	$R(N).1 \rightarrow D$
PUT HIGH REG N	PHI	BN	$D \rightarrow R(N).1$
LOGIC OPERATIONS			
OR	OR	F1	$M(R(X))$ OR $D \rightarrow D$
OR IMMEDIATE	ORI	F9	$M(R(P))$ OR $D \rightarrow D$; $R(P)+1 \rightarrow R(P)$
EXCLUSIVE OR	XOR	F3	$M(R(X))$ XOR $D \rightarrow D$
EXCLUSIVE OR IMMEDIATE	XRI	FB	$M(R(P))$ XOR $D \rightarrow D$; $R(P)+1 \rightarrow R(P)$
AND	AND	F2	$M(R(X))$ AND $D \rightarrow D$
AND IMMEDIATE	ANI	FA	$M(R(P))$ AND $D \rightarrow D$; $R(P)+1 \rightarrow R(P)$
SHIFT RIGHT	SHR	F6	SHIFT D RIGHT, $LSB(D) \rightarrow DF$, $0 \rightarrow MSB(D)$
SHIFT RIGHT WITH CARRY	SHRC	76§	SHIFT D RIGHT, $LSB(D) \rightarrow DF$, $DF \rightarrow MSB(D)$
RING SHIFT RIGHT	RSHR	FE	SHIFT D LEFT, $MSB(D) \rightarrow DF$, $0 \rightarrow LSB(D)$
SHIFT LEFT	SHL		
SHIFT LEFT WITH CARRY	SHLC	7E§	SHIFT D LEFT, $MSB(D) \rightarrow DF$, $DF \rightarrow LSB(D)$
RING SHIFT LEFT	RSHL		

TABLE I — INSTRUCTION SUMMARY (Cont'd)

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
ARITHMETIC OPERATIONS			
ADD	ADD	F4	$M(R(X))+D \rightarrow DF, D$
ADD IMMEDIATE	ADI	FC	$M(R(P))+D \rightarrow DF, D; R(P)+1 \rightarrow R(P)$
ADD WITH CARRY	ADC	74	$M(R(X))+D+DF \rightarrow DF, D$
ADD WITH CARRY, IMMEDIATE	ADCI	7C	$M(R(P))+D+DF \rightarrow DF, D$ $R(P)+1 \rightarrow R(P)$
SUBTRACT D	SD	F5	$M(R(X))-D \rightarrow DF, D$
SUBTRACT D IMMEDIATE	SDI	FD	$M(R(P))-D \rightarrow DF, D;$ $R(P)+1 \rightarrow R(P)$
SUBTRACT D WITH BORROW	SDB	75	$M(R(X))-D-(NOT DF) \rightarrow DF, D$
SUBTRACT D WITH BORROW, IMMEDIATE	SDBI	7D	$M(R(P))-D-(NOT DF) \rightarrow DF, D;$ $R(P)+1 \rightarrow R(P)$
SUBTRACT MEMORY	SM	F7	$D-M(R(X)) \rightarrow DF, D$
SUBTRACT MEMORY IMMEDIATE	SMI	FF	$D-M(R(P)) \rightarrow DF, D;$ $R(P)+1 \rightarrow R(P)$
SUBTRACT MEMORY WITH BORROW	SMB	77	$D-M(R(X))-(NOT DF) \rightarrow DF, D$
SUBTRACT MEMORY WITH BORROW, IMMEDIATE	SMBI	7F	$D-M(R(P))-(NOT DF) \rightarrow DF, D$ $R(P)+1 \rightarrow R(P)$
BRANCH INSTRUCTIONS—SHORT BRANCH			
SHORT BRANCH	BR	30	$M(R(P)) \rightarrow R(P).0$
NO SHORT BRANCH (SEE SKP)	NBR	38§	$R(P)+1 \rightarrow R(P)$
SHORT BRANCH IF D=0	BZ	32	IF D=0, $M(R(P)) \rightarrow R(P).0$ ELSE $R(P)+1 \rightarrow R(P)$
SHORT BRANCH IF D NOT 0	BNZ	3A	IF D NOT 0, $M(R(P)) \rightarrow R(P).0$ ELSE $R(P)+1 \rightarrow R(P)$
SHORT BRANCH IF DF=1	BDF	33§	IF DF=1, $M(R(P)) \rightarrow R(P).0$ ELSE $R(P)+1 \rightarrow R(P)$
SHORT BRANCH IF POS OR ZERO	BPZ		
SHORT BRANCH IF EQUAL OR GREATER	BGE		
SHORT BRANCH IF DF=0	BNF	3B§	IF DF=0, $M(R(P)) \rightarrow R(P).0$ ELSE $R(P)+1 \rightarrow R(P)$
SHORT BRANCH IF MINUS	BM		
SHORT BRANCH IF LESS	BL		
SHORT BRANCH IF Q=F	BQ	31	IF Q=1, $M(R(P)) \rightarrow R(P).0$ ELSE $R(P)+1 \rightarrow R(P)$
SHORT BRANCH IF Q=0	BNQ	39	IF Q=0, $M(R(P)) \rightarrow R(P).0$ ELSE $R(P)+1 \rightarrow R(P)$
SHORT BRANCH IF EF1=1 ($\overline{EF1}=V_{SS}$)	B1	34	IF EF1=1, $M(R(P)) \rightarrow R(P).0$ ELSE $R(P)+1 \rightarrow R(P)$
SHORT BRANCH IF EF1=0 ($\overline{EF1}=V_{CC}$)	BN1	3C	IF EF1=0, $M(R(P)) \rightarrow R(P).0$ ELSE $R(P)+1 \rightarrow R(P)$
SHORT BRANCH IF EF2=1 ($\overline{EF2}=V_{SS}$)	B2	35	IF EF2=1, $M(R(P)) \rightarrow R(P).0$ ELSE $R(P)+1 \rightarrow R(P)$
SHORT BRANCH IF EF2=0 ($\overline{EF2}=V_{CC}$)	BN2	3D	IF EF2=0, $M(R(P)) \rightarrow R(P).0$ ELSE $R(P)+1 \rightarrow R(P)$
SHORT BRANCH IF EF3=1 ($\overline{EF3}=V_{SS}$)	B3	36	IF EF3=1, $M(R(P)) \rightarrow R(P).0$ ELSE $R(P)+1 \rightarrow R(P)$
SHORT BRANCH IF EF3=0 ($\overline{EF3}=V_{CC}$)	BN3	3E	IF EF3=0, $M(R(P)) \rightarrow R(P).0$ ELSE $R(P)+1 \rightarrow R(P)$

TABLE I — INSTRUCTION SUMMARY (Cont'd)

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
BRANCH INSTRUCTIONS—SHORT BRANCH			
SHORT BRANCH IF EF4=1 (EF4=VSS)	B4	37	IF EF4=1, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH IF EF4=0 (EF4=VCC)	BN4	3F	IF EF4=0, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
BRANCH INSTRUCTIONS—LONG BRANCH			
LONG BRANCH	LBR	C0	M(R(P))→R(P).1 M(R(P)+1)→R(P).0
NO LONG BRANCH (SEE LSKP)	NLBR	C8§	R(P)+2→R(P)
LONG BRANCH IF D=0	LBZ	C2	IF D=0, M(R(P))→R(P).1 M(R(P)+1)→R(P).0 ELSE R(P)+2→R(P)
LONG BRANCH IF D NOT 0	LBNZ	CA	IF D NOT 0, M(R(P))→R(P).1 M(R(P)+1)→R(P).0 ELSE R(P)+2→R(P)
LONG BRANCH IF DF=1	LBDF	C3	IF DF=1, M(R(P))→R(P).1 M(R(P)+1)→R(P).0 ELSE R(P)+2→R(P)
LONG BRANCH IF DF=0	LBNF	CB	IF DF=0, M(R(P))→R(P).1 M(R(P)+1)→R(P).0 ELSE R(P)+2→R(P)
LONG BRANCH IF Q=1	LBQ	C1	IF Q=1, M(R(P))→R(P).1 M(R(P)+1)→R(P).0 ELSE R(P)+2→R(P)
LONG BRANCH IF Q=0	LBNQ	C9	IF Q=0, M(R(P))→R(P).1 M(R(P)+1)→R(P).0 ELSE R(P)+2→R(P)
SKIP INSTRUCTIONS			
SHORT SKIP (SEE NBR)	SKP	38§	R(P)+1→R(P)
LONG SKIP (SEE NLBR)	LSKP	C8§	R(P)+2→R(P)
LONG SKIP IF D=0	LSZ	CE	IF D=0, R(P)+2→R(P) ELSE CONTINUE
LONG SKIP IF D NOT 0	LSNZ	C6	IF D NOT 0, R(P)+2→R(P) ELSE CONTINUE
LONG SKIP IF DF=1	LSDF	CF	IF DF=1, R(P)+2→R(P) ELSE CONTINUE
LONG SKIP IF DF=0	LSNF	C7	IF DF=0, R(P)+2→R(P) ELSE CONTINUE
LONG SKIP IF Q=1	LSQ	CD	IF Q=1, R(P)+2→R(P) ELSE CONTINUE
LONG SKIP IF Q=0	LSNQ	C5	IF Q=0, R(P)+2→R(P) ELSE CONTINUE
LONG SKIP IF IE=1	LSIE	CC	IF IE=1, R(P)+2→R(P) ELSE CONTINUE

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TABLE I — INSTRUCTION SUMMARY (Cont'd)

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
CONTROL INSTRUCTIONS			
IDLE	IDL	00#	WAIT FOR DMA OR INTERRUPT; M(R(0))→BUS
NO OPERATION	NOP	C4	CONTINUE
SET P	SEP	DN	N→P
SET X	SEX	EN	N→X
SET Q	SEQ	7B	1→Q
RESET Q	REQ	7A	0→Q
SAVE	SAV	78	T→M(R(X))
PUSH X,P TO STACK	MARK	79	(X,P)→T; (X,P)→M(R(2)) THEN P→X; R(2)←1→R(2)
RETURN	RET	70	M(R(X))→(X,P); R(X)+1→R(X) 1→IE
DISABLE	DIS	71	M(R(X))→(X,P); R(X)+1→R(X) 0→IE
INPUT-OUTPUT BYTE TRANSFER			
OUTPUT 1	OUT 1	61	M(R(X))→BUS; R(X)+1→R(X); N LINES=1
OUTPUT 2	OUT 2	62	M(R(X))→BUS; R(X)+1→R(X); N LINES=2
OUTPUT 3	OUT 3	63	M(R(X))→BUS; R(X)+1→R(X); N LINES=3
OUTPUT 4	OUT 4	64	M(R(X))→BUS; R(X)+1→R(X); N LINES=4
OUTPUT 5	OUT 5	65	M(R(X))→BUS; R(X)+1→R(X); N LINES=5
OUTPUT 6	OUT 6	66	M(R(X))→BUS; R(X)+1→R(X); N LINES=6
OUTPUT 7	OUT 7	67	M(R(X))→BUS; R(X)+1→R(X); N LINES=7
INPUT 1	INP 1	69	BUS→M(R(X)); BUS→D; N LINES=1
INPUT 2	INP 2	6A	BUS→M(R(X)); BUS→D; N LINES=2
INPUT 3	INP 3	6B	BUS→M(R(X)); BUS→D; N LINES=3
INPUT 4	INP 4	6C	BUS→M(R(X)); BUS→D; N LINES=4
INPUT 5	INP 5	6D	BUS→M(R(X)); BUS→D; N LINES=5
INPUT 6	INP 6	6E	BUS→M(R(X)); BUS→D; N LINES=6
INPUT 7	INP 7	6F	BUS→M(R(X)); BUS→D; N LINES=7

Notes

§THE ARITHMETIC OPERATIONS AND THE SHIFT INSTRUCTIONS ARE THE ONLY INSTRUCTIONS THAT CAN ALTER THE DF. AFTER AN ADD INSTRUCTION:

- DF=1 DENOTES A CARRY HAS OCCURRED
- DF=0 DENOTES A CARRY HAS NOT OCCURRED

AFTER A SUBTRACT INSTRUCTION:

- DF=1 DENOTES NO BORROW. D IS A TRUE POSITIVE NUMBER
- DF=0 DENOTES A BORROW. D IS TWO'S COMPLEMENT
- THE SYNTAX "--(NOT DF)" DENOTES THE SUBTRACTION OF THE BORROW

§THIS INSTRUCTION IS ASSOCIATED WITH MORE THAN ONE MNEMONIC. EACH MNEMONIC IS INDIVIDUALLY LISTED.

*AN IDLE INSTRUCTION INITIATES A REPEATING S1 CYCLE. THE PROCESSOR WILL CONTINUE TO IDLE UNTIL AN I/O REQUEST (INTERRUPT, DMA-IN, OR DMA-OUT) IS ACTIVATED. WHEN THE REQUEST IS ACKNOWLEDGED, THE IDLE CYCLE IS TERMINATED AND THE I/O REQUEST IS SERVICED, AND THEN NORMAL OPERATION IS RESUMED.

Notes for TABLE I

1. Long-Branch, Long-Skip and No Op instructions are the only instructions that require three cycles to complete (1 fetch + 2 execute).

Long-Branch instructions are three bytes long. The first byte specifies the condition to be tested; and the second and third byte, the branching address.

The long-branch instructions can:

- a) Branch unconditionally
- b) Test for $D=0$ or $D=1$
- c) Test for $DF=0$ or $DF=1$
- d) Test for $Q=0$ or $Q=1$
- e) effect an unconditional no branch

If the tested condition is met, then branching takes place; the branching address bytes are loaded in the high- and low-order bytes of the current program counter, respectively. This operation effects a branch to any memory location.

If the tested condition is not met, the branching address bytes are skipped over, and the next instruction in sequence is fetched and executed. This operation is taken for the case of unconditional no branch (NLBR).

2. The short-branch instructions are two bytes long. The first byte specifies the condition to be tested, and the second specifies the branching address.

The short-branch instruction can:

- a) Branch unconditionally
- b) Test for $D=0$ or $D=1$
- c) Test for $DF=0$ or $DF=1$
- d) Test for $Q=0$ or $Q=1$
- e) Test the status (1 or 0) of the four EF flags
- f) Effect an unconditional no branch

If the tested condition is met, then branching takes place; the branching address byte is loaded into the low-order byte position of the current program

counter. This effects a branch within the current 256-byte page of the memory, i.e., the page which holds the branching address. If the tested condition is not met, the branching address byte is skipped over, and the next instruction in sequence is fetched and executed. This same action is taken in the case of unconditional no branch (NBR).

3. The skip instructions are one byte long. There is one Unconditional Short-Skip (SKP) and eight Long-Skip instructions.

The Unconditional Short-Skip instruction takes 2 cycles to complete (1 fetch + 1 execute). Its action is to skip over the byte following it. Then the next instruction in sequence is fetched and executed. This SKP instruction is identical to the unconditional no-branch instruction (NBR) except that the skipped-over byte is not considered part of the program.

The Long-Skip instructions take three cycles to complete (1 fetch + 2 execute).

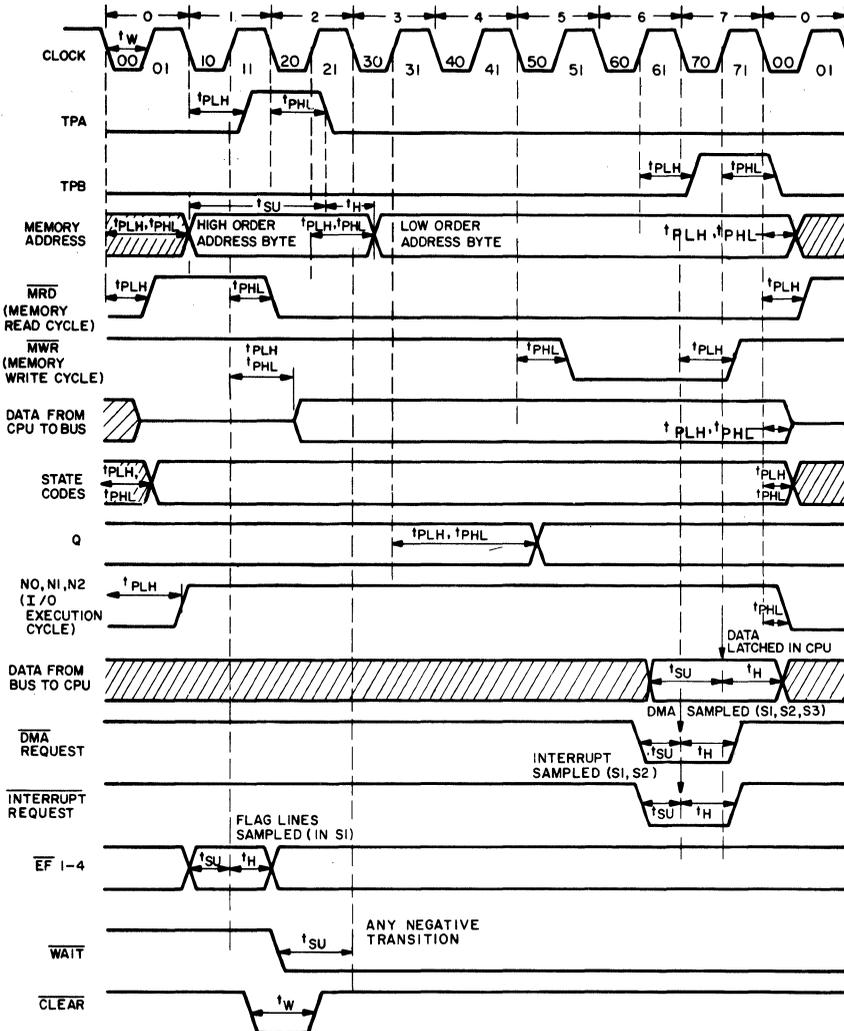
They can:

- a) Skip unconditionally
- b) Test for $D=0$ or $D=1$
- c) Test for $DF=0$ or $DF=1$
- d) Test for $Q=0$ or $Q=1$
- e) Test for $IE=1$

If the tested condition is met, then Long Skip takes place; the current program counter is incremented twice. Thus two bytes are skipped over and the next instruction in sequence is fetched and executed. If the tested condition is not met, then no action is taken.

Execution is continued by fetching the next instruction in sequence.

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NOTES:

1. THIS TIMING DIAGRAM IS USED TO SHOW SIGNAL RELATIONSHIPS ONLY AND DOES NOT REPRESENT ANY SPECIFIC MACHINE CYCLE
2. ALL MEASUREMENTS ARE REFERENCED TO 50% POINT OF THE WAVEFORMS
3. SHADED AREAS INDICATE "DON'T CARE" OR UNDEFINED STATE; MULTIPLE TRANSITIONS MAY OCCUR DURING THIS PERIOD

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Fig. 12 - Timing waveforms.

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DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $C_L = 50$ pF, $V_{DD} \pm 5\%$, except as noted.

CHARACTERISTIC	VCC (V)	VDD (V)	LIMITS		UNITS
			Typ.*	Max.	
Propagation Delay Times:					
Clock to TPA, TPB t _{PLH} , t _{PHL}	5	5	200	300	ns
	5	10	150	250	
	10	10	100	150	
Clock-to-Memory High-Address Byte t _{PLH} , t _{PHL}	5	5	600	850	
	5	10	400	600	
	10	10	300	400	
Clock-to-Memory Low-Address Byte Valid t _{PLH} , t _{PHL}	5	5	250	350	
	5	10	150	250	
	10	10	100	150	
Clock to $\overline{\text{MRD}}$ t _{PHL}	5	5	200	300	
	5	10	150	250	
	10	10	100	150	
Clock to $\overline{\text{MRD}}$ t _{PLH}	5	5	200	350	
	5	10	150	290	
	10	10	100	175	
Clock to $\overline{\text{MWR}}$ t _{PLH} , t _{PHL}	5	5	200	300	
	5	10	150	250	
	10	10	100	150	
Clock to (CPU DATA to BUS) Valid t _{PLH} , t _{PHL}	5	5	300	450	
	5	10	250	350	
	10	10	100	200	
Clock to State Code t _{PLH} , t _{PHL}	5	5	300	450	
	5	10	250	350	
	10	10	150	250	
Clock to Q t _{PLH} , t _{PHL}	5	5	250	400	
	5	10	150	250	
	10	10	100	150	
Clock to N (0-2) t _{PLH} , t _{PHL}	5	5	300	550	
	5	10	200	350	
	10	10	150	250	
Minimum Setup and Hold Times:					
Data Bus Input Setup t _{SU}	5	5	-20	25	
	5	10	0	50	
	10	10	-10	40	
Data Bus Input Hold t _H [■]	5	5	150	200	
	5	10	100	125	
	10	10	75	100	
$\overline{\text{DMA}}$ Setup t _{SU}	5	5	0	30	
	5	10	0	20	
	10	10	0	10	
$\overline{\text{DMA}}$ Hold t _H [■]	5	5	150	250	
	5	10	100	200	
	10	10	75	125	
Interrupt Setup t _{SU}	5	5	-75	0	
	5	10	-50	0	
	10	10	-25	0	

*Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .

■Maximum limits of minimum characteristics are the values above which all devices function.

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DYNAMIC ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	VCC (V)	VDD (V)	LIMITS		UNITS
			Typ.*	Max.	
Minimum Setup and Hold Times:					
Interrupt Hold t_H^{\blacksquare}	5	5	100	150	ns
	5	10	75	100	
	10	10	50	75	
WAIT Setup t_{SU}	5	5	10	50	
	5	10	-10	15	
	10	10	0	25	
EF1-4 Setup t_{SU}	5	5	-30	20	
	5	10	-20	30	
	10	10	-10	40	
EF1-4 Hold t_H^{\blacksquare}	5	5	150	200	
	5	10	100	150	
	10	10	75	100	
Minimum Pulse Width Times:					
CLEAR Pulse Width t_{WL}^{\blacksquare}	5	5	150	300	
	5	10	100	200	
	10	10	75	150	
CLOCK Pulse Width t_{WL}	5	5	125	150	
	5	10	100	125	
	10	10	60	75	

*Typical values are for $T_A=25^\circ\text{C}$ and nominal V_{DD} .

■Maximum limits of minimum characteristics are the values above which all devices function.

TIMING SPECIFICATIONS as a function of T ($T=1/f_{CLOCK}$) at $T_A=-40$ to $+85^\circ\text{C}$.

CHARACTERISTIC	VCC (V)	VDD (V)	LIMITS		UNITS
			Min.	Typ.*	
High-Order Memory-Address Byte Set Up to TPA t_{SU} Time	5	5	2T-550	2T-400	ns
	5	10	2T-350	2T-250	
	10	10	2T-250	2T-200	
High-Order Memory-Address Byte Hold after TPA Time t_H	5	5	T/2-25	T/2-15	
	5	10	T/2-35	T/2-25	
	10	10	T/2-10	T/2+0	
Low-Order Memory-Address Byte Hold after WR Time t_H	5	5	T-30	T+0	
	5	10	T-20	T+0	
	10	10	T-10	T+0	
CPU Data to Bus Hold after WR Time t_H	5	5	T-200	T-150	
	5	10	T-150	T-100	
	10	10	T-100	T-50	
Required Memory Access Time Address to Data t_{ACC}	5	5	5T-375	5T-250	
	5	10	5T-250	5T-150	
	10	10	5T-190	5T-100	

*Typical values are for $T_A=25^\circ\text{C}$ and nominal V_{DD} .

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TABLE II. CONDITIONS ON DATA BUS AND MEMORY ADDRESS LINES DURING ALL MACHINE STATES

STATE	I	N	MNEMONIC	OPERATION	DATA BUS	MEMORY ADDRESS	$\overline{\text{MRD}}$	$\overline{\text{MWR}}$	N LINES	NOTES ^G
S1			RESET	0-I,N,Q,X,P; 1-IE	00	XXXX	1	1	0	A
S1			INITIALIZE NOT PROGRAMMER ACCESSIBLE	0000-R	00	XXXX	1	1	0	B
S0			FETCH	MRP-I, N; RP+1-RP	MRP	RP	0	1	0	C
S1	0	0	IDL	IDLE	MR0	R0	0	1	0	D,3
	0	1-F	LDN	MRN-D	MRN	RN	0	1	0	3
	1	0-F	INC	RN+1-RN	FLOAT	RN	1	1	0	1
	2	0-F	DEC	RN-1-RN	FLOAT	RN	1	1	0	1
	3	0-F	SHORT BRANCH	TAKEN; MRP-RP,0 NOT TAKEN; RP+1-RP	MRP	RP	0	1	0	3
	4	0-F	LDA	MRN-D; RN+1-RN	MRN	RN	0	1	0	3
	5	0-F	STR	D-MRN	D	RN	1	0	0	2
	6	0	IRX	RX+1-RX	MRX	RX	0	1	0	2
	6	1	OUT 1	MRX-BUS; RX+1-RX	MRX	RX	0	1	1	6
		2	OUT 2						2	
		3	OUT 3						3	
		4	OUT 4						4	
		5	OUT 5						5	
		6	OUT 6						6	
		7	OUT 7						7	
	6	9	INP 1	BUS-MRX,D	DATA FROM I/O DEVICE	RX	1	0	1	5
		A	INP 2						2	
B		INP 3	3							
C		INP 4	4							
D		INP 5	5							
E		INP 6	6							
F		INP 7	7							
7	0	RET	MRX-(X,P); RX+1-RX; 1-IE	MRX	RX	0	1	0	3	
	1	DIS	MRX-(X,P); RX+1-RX; 0-IE	MRX	RX	0	1	0	3	
	2	LDXA	MRX-D; RX+1-RX	MRX	RX	0	1	0	3	
	3	STXD	D-MRX; RX-1-RX	D	RX	1	0	0	2	
	4	ADC	MRX+D+ DF-DF,D	MRX	RX	0	1	0	3	

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TABLE II. CONDITIONS ON DATA BUS AND MEMORY ADDRESS LINES DURING ALL MACHINE STATES (CONT'D)

STATE	I	N	MNEMONIC	OPERATION	DATA BUS	MEMORY ADDRESS	$\overline{\text{MRD}}$	$\overline{\text{MWR}}$	N LINES	NOTES ^Q
S1	7	5	SDB	MRX-D- DFN-DF,D	MRX	RX	0	1	0	3
		6	SHRC	LSB(D)-DF; DF-MSB(D)	FLOAT	RX	1	1	0	1
		7	SMB	D-MRX- DFN-DF,D	MRX	RX	0	1	0	3
		8	SAV	T-MRX	T	RX	1	0	0	2
		9	MARK	(X,P)-T, MR2; P-X; R2-1-R2	T	R2	1	0	0	2
		A	REQ	0-Q	FLOAT	RP	1	1	0	1
		B	SEQ	1-Q	FLOAT	RP	1	1	0	1
		C	ADCI	MRP+D+ DF-DF,D; RP+1	MRP	RP	0	1	0	3
		D	SDBI	MRP-D- DFN-DF,D; RP+1	MRP	RP	0	1	0	3
		E	SHLC	MSB(D)-DF; DF-LSB(D)	FLOAT	RP	1	1	0	1
	F	SMBI	D-MRP- DFN-DF,D; RP+1	MRP	RP	0	1	0	3	
	8	0-F	GLO	RN.0-D	RN.0	RN	1	1	0	1
	9	0-F	GHI	RN.1-D	RN.1	RN	1	1	0	1
A	0-F	PLO	D-RN.0	D	RN	1	1	0	1	
B	0-F	PHI	D-RN.1	D	RN	1	1	0	1	
S1#1	C	0-3, 8-B	LONG BRANCH	TAKEN: MRP-B; RP+1-RP	MRP	RP	0	1	0	4
#2				TAKEN: B-RP.1; MRP-RP.0	M(RP+1)	RP+1	0	1	0	4
S1#1				NOT TAKEN: RP+1-RP	MRP	RP	0	1	0	4
#2				NOT TAKEN: RP+1-RP	M(RP+1)	RP+1	0	1	0	4
S1#1		5 6 7 C D E F	LONG SKIP	TAKEN: RP+1-RP	MRP	RP	0	1	0	4
#2				TAKEN: RP+1-RP	M(RP+1)	RP+1	0	1	0	4
S1#1				NOT TAKEN: NO OPERATION	MRP	RP	0	1	0	4
#2				NOT TAKEN: NO OPERATION	MRP	RP	0	1	0	4
S1#1				NO OPERATION	MRP	RP	0	1	0	4
#2				NO OPERATION	MRP	RP	0	1	0	4
S1#1		4	NOP	NO OPERATION	MRP	RP	0	1	0	4
#2				NO OPERATION	MRP	RP	0	1	0	4

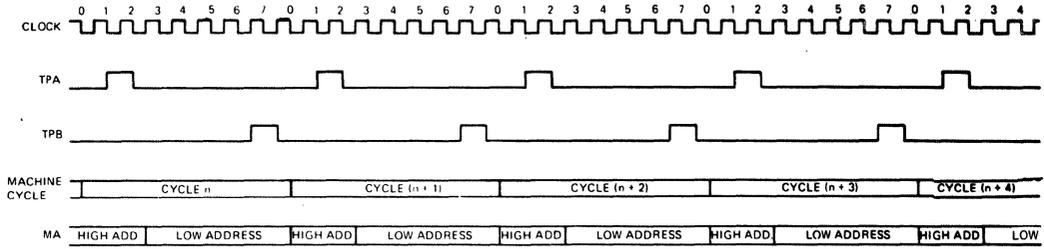
TABLE II. CONDITIONS ON DATA BUS AND MEMORY ADDRESS LINES DURING ALL MACHINE STATES (CONT'D)

STATE	I	N	MNEMONIC	OPERATION	DATA BUS	MEMORY ADDRESS	MRD	MWR	N LINES	NOTES ^a	
S1	D	0-F	SEP	N-P	NN	RN	1	1	0	1	
	E	0-F	SEX	N-X	NN	RN	1	1	0	1	
	F	0	LDX	MRX-D	MRX	MRX	RX	0	1	0	3
		1	OR	MRX OR D-D	MRX	RX	0	1	0	3	
		2	AND	MRX AND D-D							
		3	XOR	MRX XOR D-D							
		4	ADD	MRX+D-DF,D							
		5	SD	MRX-D-DF,D							
		7	SM	D-MRX-DF,D							
		6	SHR	LSB(D)-DF; 0-MSB(D)	FLOAT	RX	1	1	0	1	
		8	LDI	MRP-D; RP+1-RP	MRP	RP	0	1	0	3	
		9	ORI	MRP OR D-D; RP+1-RP							
	A	ANI	MRP AND D-D; RP+1-RP								
	B	XRI	MRP XOR D-D; RP+1-RP								
C	ADI	MRP+D-DF,D; RP+1-RP									
D	SDI	MRP-D-DF,D; RP+1-RP									
F	SMI	D-MRP-DF,D; RP+1-RP									
E	SHL	MSB(D)-DF; 0-LSB(D)	FLOAT	RP	1	1	0	1			
S2	DMA IN		BUS-MR0; R0+1-R0	DATA FROM I/O DEVICE	R0	1	0	0	F, 7		
	DMA OUT		MR0-BUS; R0+1-R0	MR0	R0	0	1	0	F, 8		
S3	INTERRUPT		X,P-T; 0-IE 1-P; 2-X	FLOAT	RN	1	1	0	9		
S1	LOAD		IDLE (CLEAR, WAIT=0)	M(R0-1)	R0-1	0	1	0	E,3		

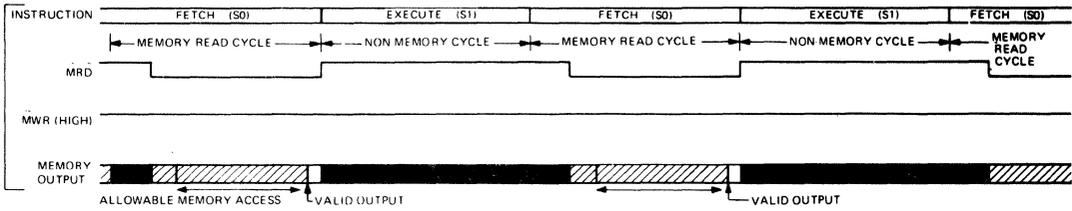
NOTES:

- A. IE=1, TPA, TPB suppressed, state=S1.
- B. BUS=0 for entire cycle.
- C. Next state always S1.
- D. Wait for DMA or INTERRUPT.
- E. Suppress TPA, wait for DMA.
- F. IN REQUEST has priority over OUT REQUEST.
- G. Number refers to machine cycle. See Fig. 14 timing waveforms for machine cycles 1 through 9.

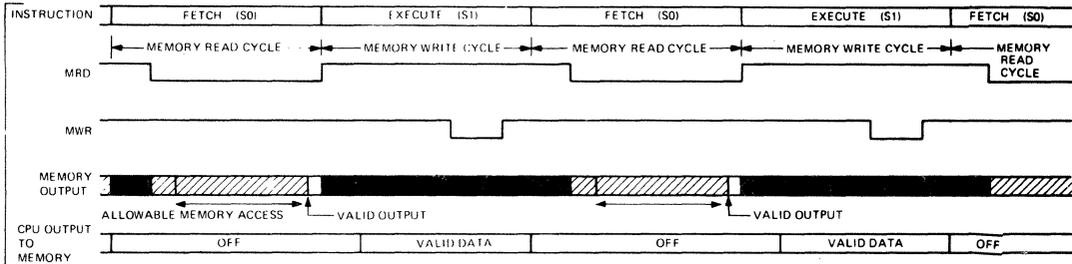
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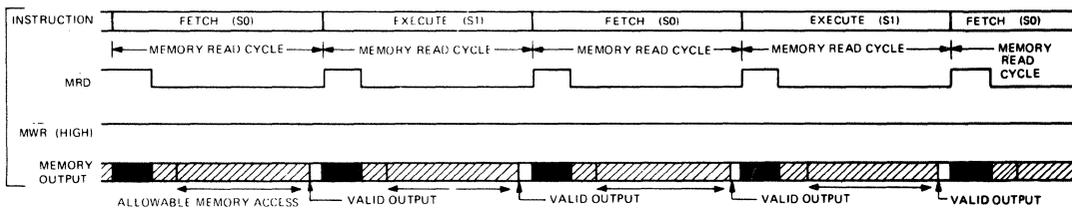
General timing waveforms.



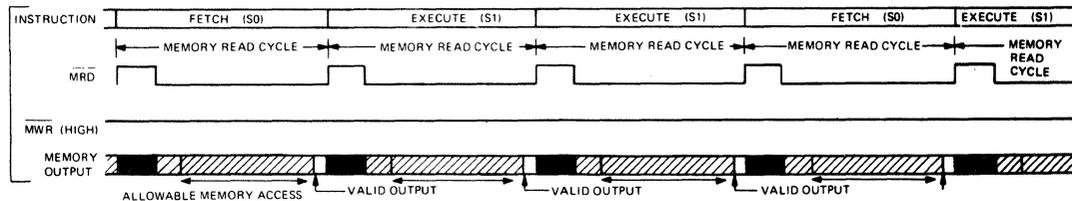
No. 1 Non-memory-cycle timing waveforms.



No. 2 Memory write-cycle timing waveforms.



No. 3 Memory read-cycle timing waveforms.

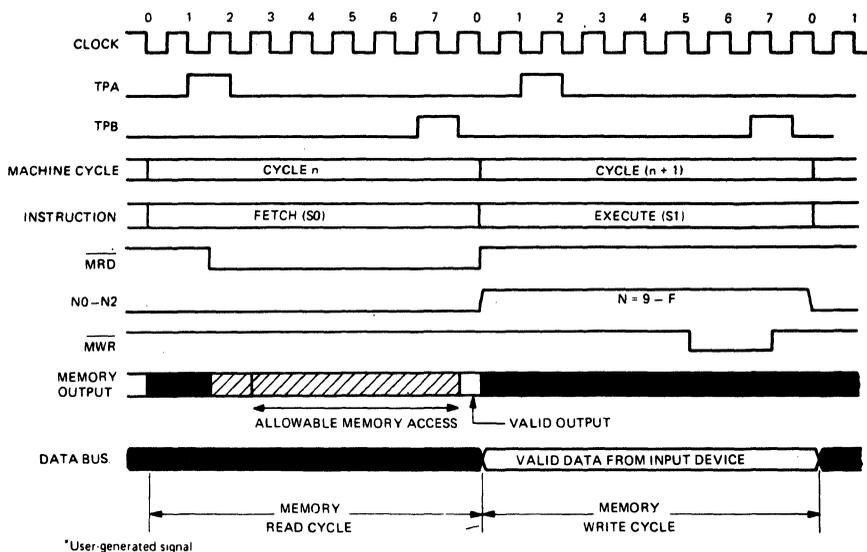


No. 4 Long-branch or long-skip-cycle timing waveforms.

 "Don't Care" or internal delays
 High impedance state

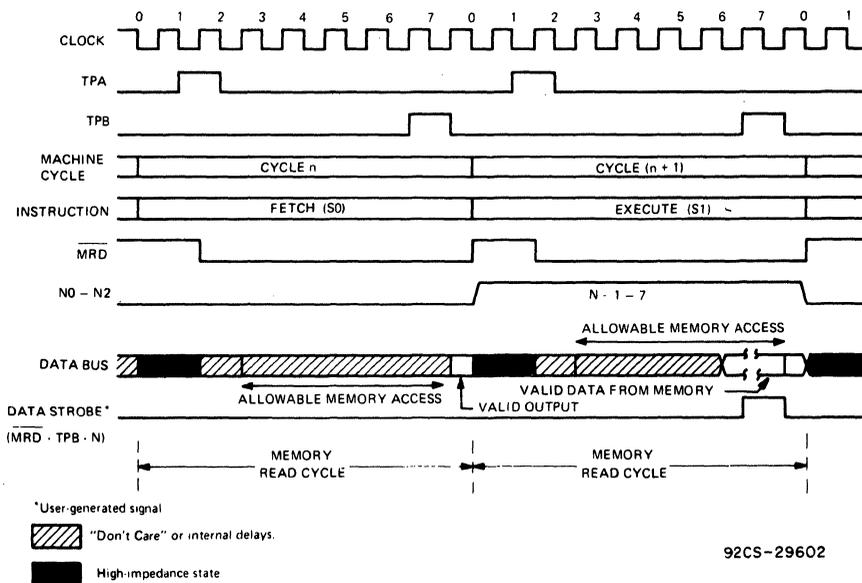
92CL-29600

Fig. 13 - Machine-cycle timing waveforms (propagation delays not shown).



92CS-29601

No. 5 Input-cycle timing waveforms.



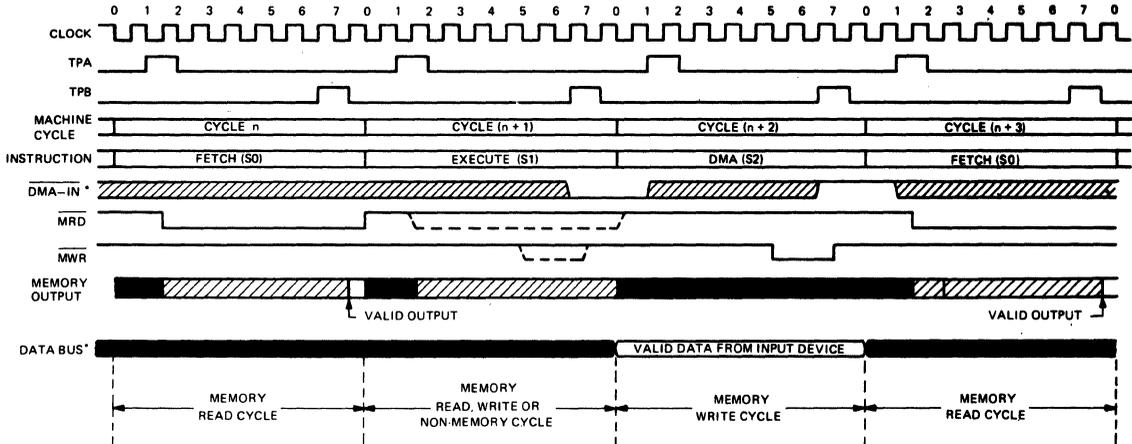
92CS-29602

No. 6 Output-cycle timing waveforms.

Fig. 13 - Machine-cycle timing waveforms (propagation delays not shown). Continued.

RCA CMOS LSI Products

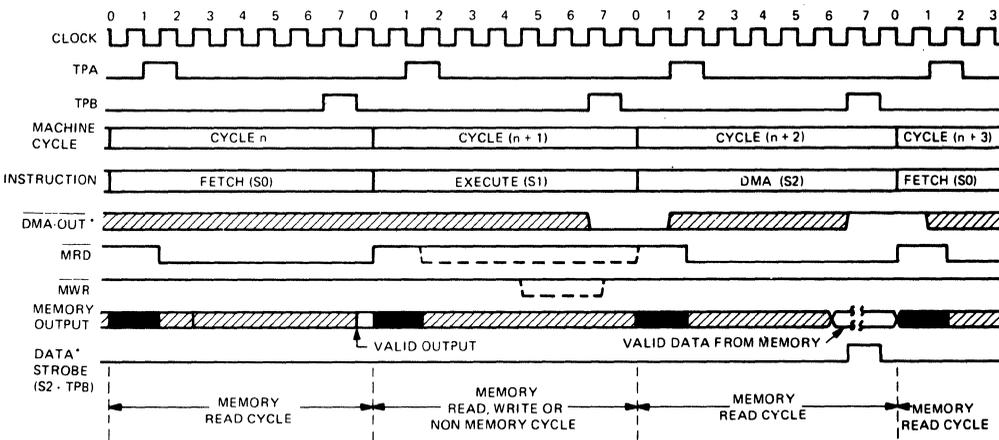
CDP1802A, CDP1802AC



*User-generated signal

92CS-29603

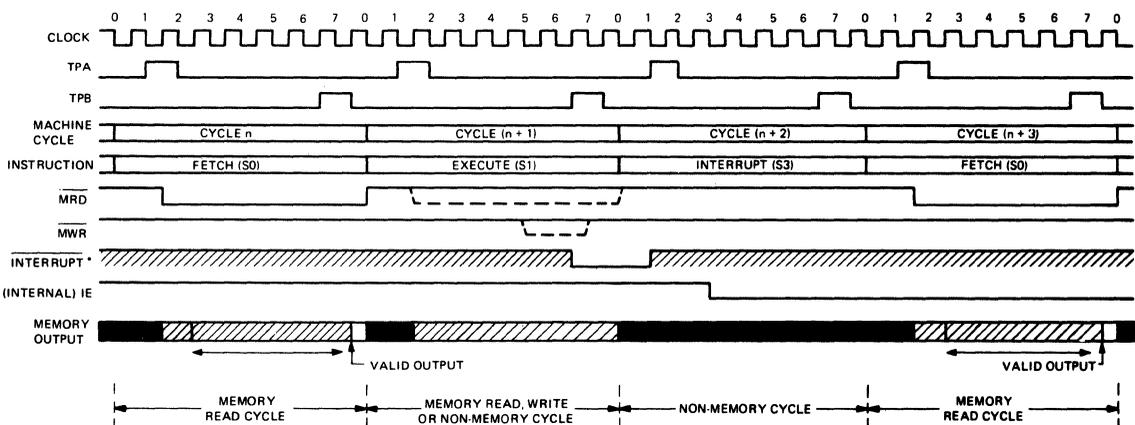
No. 7 DMA-IN-cycle timing waveforms.



*User-generated signal

92CM-29604RI

No. 8 DMA-OUT-cycle timing waveforms.



*User-generated signal

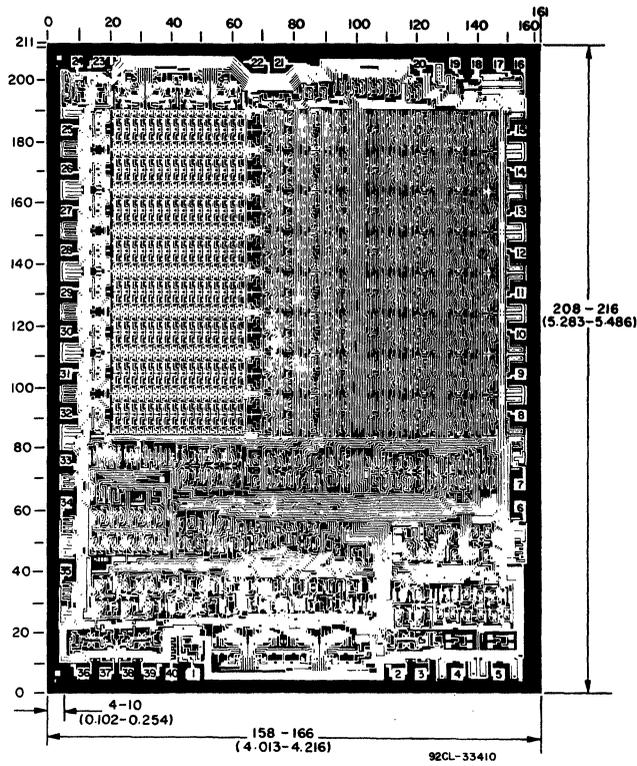
▨ "Don't Care" or internal delays. ■ High-impedance state

No. 9 INTERRUPT-cycle timing waveforms.

92CM-29605

Fig. 13 - Machine-cycle timing waveforms (propagation delays not shown). Continued.

1800-Series Microprocessors and Microcomputers
CDP1802A, CDP1802AC

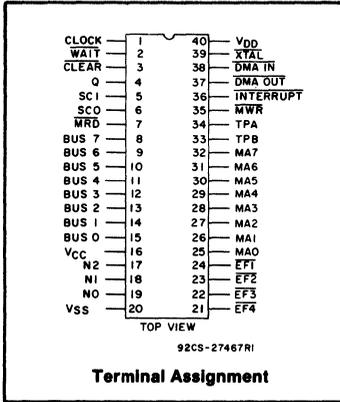


Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions and pad layout for CDP1802ACH.

Preliminary Data
CMOS 8-Bit Microprocessor



Features:

- Minimum instruction fetch-execute time of 3.2 μ s (maximum clock frequency=5 MHz) at $V_{DD}=5$ V
- Any combination of standard RAM and ROM up to 65,536 bytes
- Operates with slow memories, up to 775 ns access time at $f_{CL}=5$ MHz
- 8-bit parallel organization with bidirectional data bus and multiplexed address bus
- 16 x 16 matrix of registers for use as multiple program counters, data pointers, or data registers
- On-chip DMA, interrupt, and flag inputs
- Programmable single-bit output port
- 91 easy-to-use instructions

The RCA-CDP1802BC LSI CMOS 8-bit register-oriented central-processing unit (CPU) is designed for use as a general-purpose computing or control element in a wide range of stored-program systems or products.

The CDP1802BC includes all of the circuits required for fetching, interpreting, and executing instructions which have been stored in standard types of memories. Extensive input/output (I/O) control features are also provided to facilitate system design.

The 1800 series architecture is designed with emphasis on the total microcomputer system as an integral entity so that

systems having maximum flexibility and minimum cost can be realized. The 1800 series CPU also provides a synchronous interface to memories and external controllers for I/O devices, and minimizes the cost of interface controllers. Further, the I/O interface is capable of supporting devices operating in polled, interrupt-driven, or direct memory-access modes.

The CDP1802BC has a recommended operating voltage range of 4 to 6.5 volts. These types are supplied in 40-lead dual-in-line side-braced ceramic packages (D suffix), and 40-lead dual-in-line plastic packages (E suffix).

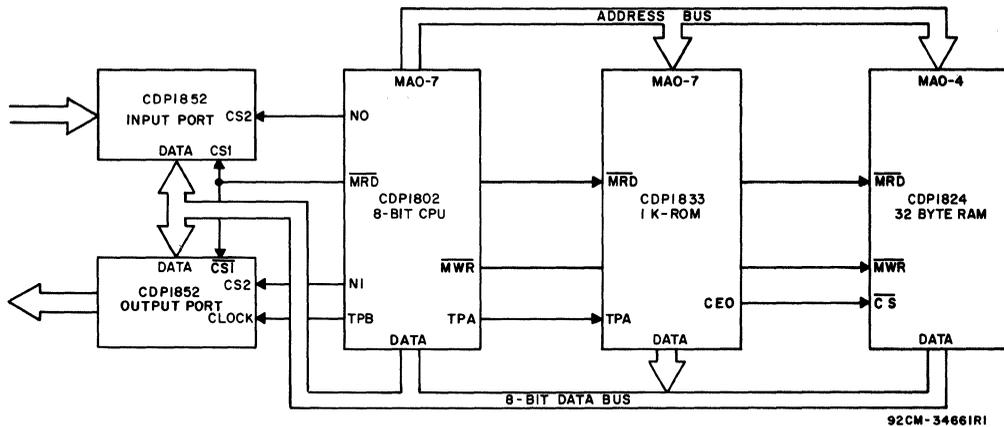


Fig. 1 - Typical CDP1802BC small microprocessor system.

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD}):

(All voltages referenced to V_{SS} terminal)

CDP1802BC -0.5 to +7 V

INPUT VOLTAGE RANGE, ALL INPUTS -0.5 to V_{DD} +0.5 V

DC INPUT CURRENT, ANY ONE INPUT ±10 mA

POWER DISSIPATION PER PACKAGE (P_D):

For T_A=-40 to +60°C (PACKAGE TYPE E) 500 mW

For T_A=+60 to +85°C (PACKAGE TYPE E) Derate Linearly at 12 mW/°C to 200 mW

For T_A=-55 to +100°C (PACKAGE TYPE D) 500 mW

For T_A=+100 to +125°C (PACKAGE TYPE D) Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A=FULL PACKAGE-TEMPERATURE RANGE 100 mW

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPE D -55 to +125°C

PACKAGE TYPE E -40 to +85°C

STORAGE TEMPERATURE RANGE (T_{stg}) -65 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16±1/32 in. (1.59±0.79 mm) from case for 10 s max. +265°C

OPERATING CONDITIONS at T_A=-40°C to +85°C

For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	CONDITIONS		LIMITS		UNITS
	V _{CC1} (V)	V _{DD} (V)	CDP1802BC		
			Min.	Max.	
DC Operating Voltage Range	—	—	4.0	6.5	V
Input Voltage Range	—	—	V _{SS}	V _{DD}	
Maximum Clock Input Rise or Fall Time, t _r , t _f	4 to 6.5	4 to 6.5	—	1	μs
Minimum Instruction Time ²	5	5	3.2	—	
Maximum DMA Transfer Rate	5	5	—	667	KBytes/s
Maximum Clock Input Frequency, Load Capacitance (C _L)=50 pF	f _{CL} 5	5	DC	5	MHz

¹V_{CC} must never exceed V_{DD}.

²Equals 2 machine cycles—one Fetch and one Execute operation for all instructions except Long Branch and Long Skip, which require 3 machine cycles—one Fetch and two Execute operations.

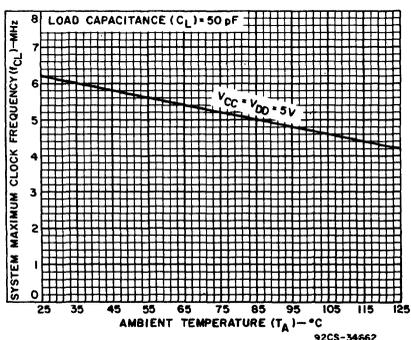


Fig. 2 - Typical maximum clock frequency as a function of temperature.

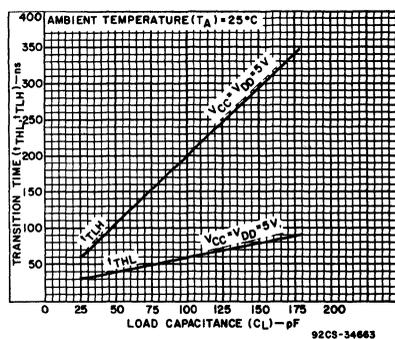


Fig. 3 - Typical transition time vs. load capacitance.

RCA CMOS LSI Products

CDP1802BC

STATIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, except as noted.

CHARACTERISTIC		CONDITIONS			LIMITS			UNITS
		V _{OUT} (V)	V _{IN} (V)	V _{CC} , V _{VDD} (V)	CDP1802BC			
					Min.	Typ.*	Max.	
Quiescent Device Current	I _{DD}	—	—	5	—	1	200	μA
Output Low Drive (Sink) Current (Except XTAL)	I _{OL}	0.4	0.5	5	1.1	2.2	—	mA
		XTAL	0.4	5	5	170	350	—
Output High Drive (Source) Current (Except XTAL)	I _{OH}	4.6	0.5	5	-0.27	-0.55	—	mA
		XTAL	4.6	0	5	-125	-250	—
Output Voltage Low-Level	V _{OL}	—	0.5	5	—	0	0.1	V
Output Voltage High Level	V _{OH}	—	0.5	5	4.9	5	—	
Input Low Voltage	V _{IL}	0.5, 4.5	—	5	—	—	1.5	
Input High Voltage	V _{IH}	0.5, 4.5	—	5	3.5	—	—	
CLEAR Input Voltage Schmitt Hysteresis	V _H	—	—	5	0.4	0.5	—	
Input Leakage Current	I _{IN}	Any Input	0.5	5	—	$\pm 10^{-4}$	± 1	μA
3-State Output Leakage Current	I _{OUT}	0.5	0.5	5	—	$\pm 10^{-4}$	± 1	μA
Total Power Dissipation, $f=5\text{ MHz}$		—	—	5	—	15	30	mW
Minimum Data Retention Voltage	V _D R	V _{DD} =V _D R			—	2	2.4	V
Data Retention Current	I _D R	V _{DD} =2.4 V			—	0.5	—	μA
Input Capacitance	C _{IN}				—	5	7.5	pF
Output Capacitance	C _{OUT}				—	10	15	

*Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD}.

Δ Idle "00" at M(0000), C_L=50 pF.

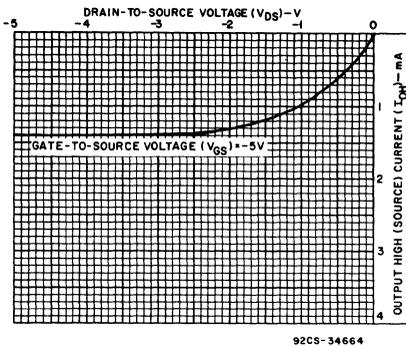


Fig. 4 - Minimum output high (source) current characteristics.

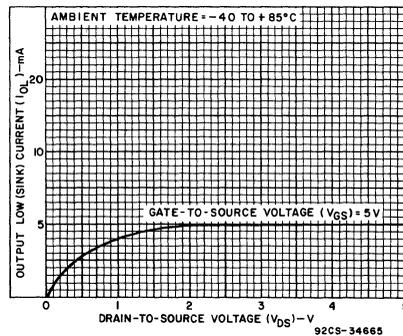


Fig. 5 - Minimum output low (sink) current characteristics.

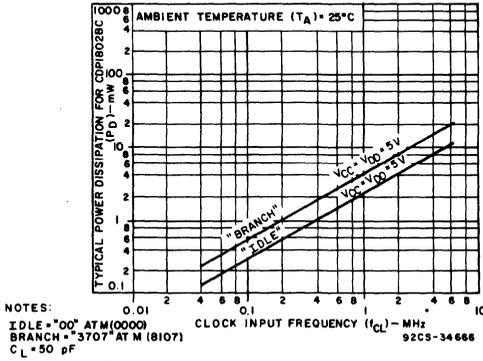


Fig. 6 - Typical power dissipation as a function of clock frequency for BRANCH instruction and IDLE instruction.

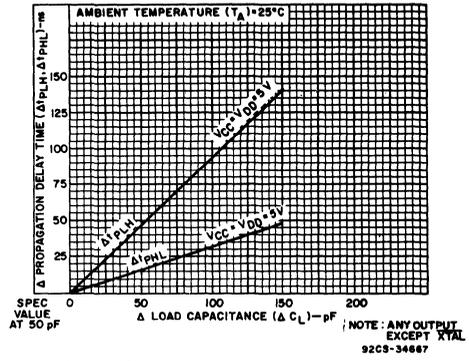


Fig. 7 - Typical change in propagation delay as a function of a change in load capacitance.

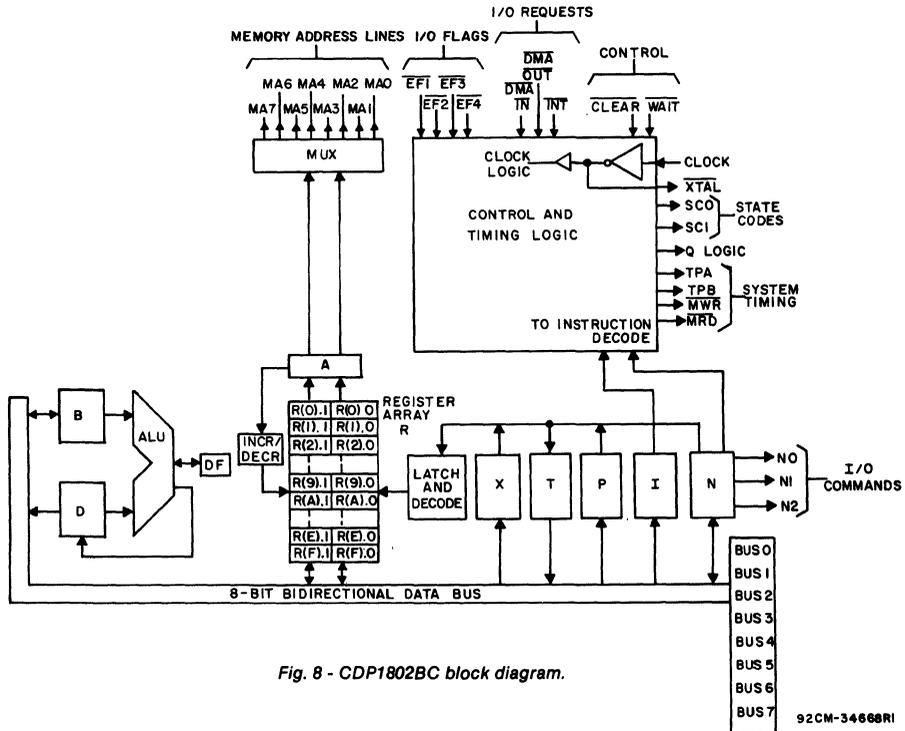


Fig. 8 - CDP1802BC block diagram.

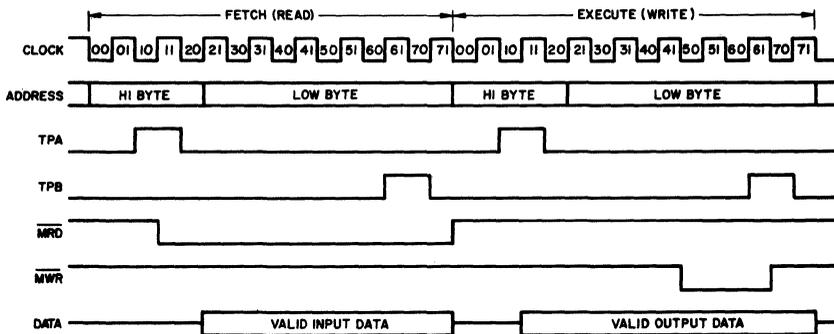


Fig. 9 - Basic dc timing waveforms, one instruction cycle.

SIGNAL DESCRIPTIONS

BUS 0 to BUS 7 (Data Bus):

8-bit bidirectional DATA BUS lines. These lines are used for transferring data between the memory, the microprocessor, and I/O devices.

N0 to N2 (I/O) Lines):

Activated by an I/O instruction to signal the I/O control logic of a data transfer between memory and I/O interface. These lines can be used to issue command codes or device selection codes to the I/O devices (independently or combined with the memory byte on the data bus when an I/O instruction is being executed). The N bits are low at all times except when an I/O instruction is being executed. During this time their state is the same as the corresponding bits in the N register.

The direction of data flow is defined in the I/O instruction by bit N3 (internally) and is indicated by the level of the MRD signal.

MRD=V_{CC}: Data from I/O to CPU and Memory
 MRD=V_{SS}: Data from Memory to I/O

EF1 to EF4 (4 Flags):

These inputs enable the I/O controllers to transfer status information to the processor. The levels can be tested by the conditional branch instructions. They can be used in conjunction with the INTERRUPT request line to establish interrupt priorities. These flags can also be used by I/O devices to "call the attention" of the processor, in which case the program must routinely test the status of these flag(s). The flag(s) are sampled at the beginning of every S1 cycle.

INTERRUPT, DMA-IN, DMA-OUT (3 I/O Requests)

These inputs are sampled by the CDP1802BC during the interval between the leading edge of TPB and the leading edge of TPA.

Interrupt Action: X and P are stored in T after executing current instruction; designator X is set to 2; designator P is set to 1; interrupt enable is reset to 0 (inhibit); and instruction execution is resumed. The interrupt action requires one machine cycle (S3).

DMA Action: Finish executing current instruction; R(0) points to memory area for data transfer; data is loaded into or read out of memory; and increment R(0).

Note: In the event of concurrent DMA and Interrupt requests, DMA-IN has priority followed by DMA-OUT and then Interrupt.

SC0, SC1, (2 State Code Lines):

These outputs indicate that the CPU is: 1) fetching an instruction, or 2) executing an instruction, or 3) processing a DMA request, or 4) acknowledging an interrupt request. The levels of state code are tabulated below. All states are valid at TPA. H=V_{CC}, L=V_{SS}.

State Type	State Code Lines	
	SC1	SC0
S0 (Fetch)	L	L
S1 (Execute)	L	H
S2 (DMA)	H	L
S3 (Interrupt)	H	H

TPA, TPB (2 Timing Pulses):

Positive pulses that occur once in each machine cycle (TPB follows TPA). They are used by I/O controllers to interpret codes and to time interaction with the data bus. The trailing edge of TPA is used by the memory system to latch the higher-order byte of the 16-bit memory address. TPA is suppressed in IDLE when the CPU is in the load mode.

MA0 to MA7 (8 Memory Address Lines):

In each cycle, the higher-order byte of a 16-bit CPU memory address appears on the memory address lines MA0-7 first. Those bits required by the memory system can be strobed into external address latches by timing pulse TPA. The low-order byte of the 16-bit address appears on the address lines after the termination of TPA. Latching of all 8 higher-order address bits would permit a memory system of 64K bytes.

MWR (Write Pulse):

A negative pulse appearing in a memory-write cycle, after the address lines have stabilized.

MRD (Read Level):

A low level on MRD indicates a memory read cycle. It can be used to control three-state outputs from the addressed memory which may have a common data input and output bus. If a memory does not have a three-state high-impedance output, MRD is useful for driving memory/bus separator gates. It is also used to indicate the direction of data transfer during an I/O instruction. For additional information see Table I.

Q:

Single bit output from the CPU which can be set or reset under program control. During SEQ or REQ instruction execution, Q is set or reset between the trailing edge of TPA and the leading edge of TPB.

CLOCK:

Input for externally generated single-phase clock. A typical clock frequency is 5 MHz at V_{CC}=V_{DD}=5 volts. The clock is counted down internally to 8 clock pulses per machine cycle.

XTAL:

Connection to be used with clock input terminal, for an external crystal, if the on-chip oscillator is utilized. The crystal is connected between terminals 1 and 39 (CLOCK and XTAL) in parallel with a resistance (10 megohms typ.). Frequency trimming capacitors may be required at terminals 1 and 39. For additional information, see ICAN-6565.

WAIT, CLEAR (2 Control Lines):

Provide four control modes as listed in the following truth table:

CLEAR	WAIT	MODE
L	L	LOAD
L	H	RESET
H	L	PAUSE
H	H	RUN

VDD, VSS, VCC (Power Levels):

The internal voltage supply V_{DD} is isolated from the Input/Output voltage supply V_{CC} so that the processor may operate at maximum speed while interfacing with peripheral devices operating at lower voltage. V_{CC} must be less than or equal to V_{DD}. All outputs swing from V_{SS} to V_{CC}. The recommended input voltage swing is V_{SS} to V_{CC}.

ARCHITECTURE

The CPU block diagram is shown in Fig. 8. The principal feature of this system is a register array (R) consisting of sixteen 16-bit scratchpad registers. Individual registers in the array (R) are designated (selected) by a 4-bit binary code from one of the 4-bit registers labeled N, P, and X. The contents of any register can be directed to any one of the following three paths:

1. the external memory (multiplexed, higher-order byte first, on to 8 memory address lines);
2. the D register (either of the two bytes can be gated to D);
3. the increment/decrement circuit where it is increased or decreased by one and stored back in the selected 16-bit register.

The three paths, depending on the nature of the instruction, may operate independently or in various combinations in the same machine cycle.

With two exceptions, CPU instructions consist of two 8-clock-pulse machine cycles. The first cycle is the fetch cycle, and the second—and third if necessary—are execute cycles. During the fetch cycle the four bits in the P designator select one of the 16 registers R(P) as the current program counter. The selected register R(P) contains the address of the memory location from which the instruction is to be fetched. When the instruction is read out from the memory, the higher-order 4 bits of the instruction byte are loaded into the I register and the lower-order 4 bits into the N register. The content of the program counter is automatically incremented by one so that R(P) is now "pointing" to the next byte in the memory.

The X designator selects one of the 16 registers R(X) to "point" to the memory for an operand (or data) in certain ALU or I/O operations.

The N designator can perform the following five functions depending on the type of instruction fetched:

1. designate one of the 16 registers in R to be acted upon during register operations;
2. indicate to the I/O devices a command code or device-selection code for peripherals;
3. indicate the specific operation to be executed during the ALU instructions, types of tests to be performed during the Branch instructions, or the specific operation required in a class of miscellaneous instructions (70-73 and 78-7B);
4. indicate the value to be loaded into P to designate a new register to be used as the program counter R(P);
5. indicate the value to be loaded into X to designate a new register to be used as data pointer R(X).

The registers in R can be assigned by a programmer in three different ways: as program counters, as data pointers, or as scratchpad locations (data registers) to hold two bytes of data.

Program Counters

Any register can be the main program counter; the address of the selected register is held in the P designator. Other registers in R can be used as subroutine program counters. By a single instruction the contents of the P register can be changed to effect a "call" to a subroutine. When interrupts are being serviced, register R(1) is used as the program counter for the user's interrupt servicing routine. After reset, and during a DMA operation, R(0) is used as the program counter. At all other times the register designated as program counter is at the discretion of the user.

Data Pointers

The registers in R may be used as data pointers to indicate a location in memory. The register designated by X (i.e., R(X)) points to memory for the following instructions (see Table I):

1. ALU operations F1-F5, F7, 74, 75, 77;
2. output instructions 61 through 67;
3. input instructions 69 through 6F;
4. certain miscellaneous instructions — 70-73, 78, 80, F0.

The register designated by N (i.e., R(N)) points to memory for the "load D from memory" instructions 0N and 4N and the "Store D" instruction 5N. The register designated by P (i.e., the program counter) is used as the data pointer for ALU instructions F8-FD, FF, 7C, 7D, 7F. During these instruction executions, the operation is referred to as "data immediate".

Another important use of R as a data pointer supports the built-in Direct-Memory-Access (DMA) function. When a DMA-In or DMA-Out request is received, one machine cycle is "stolen". This operation occurs at the end of the execute machine cycle in the current instruction. Register R(0) is always used as the data pointer during the DMA operation. The data is read from (DMA-Out) or written into (DMA-In) the memory location pointed to by the R(0) register. At the end of the transfer, R(0) is incremented by one so that the processor is ready to act upon the next DMA byte transfer request. This feature in the 1800-series architecture saves a substantial amount of logic when fast exchanges of blocks of data are required, such as with magnetic discs or during CRT-display-refresh cycles.

Data Registers

When registers in R are used to store bytes of data, four instructions are provided which allow D to receive from or write into either the higher-order- or lower-order-byte portions of the register designated by N. By this mechanism (together with loading by data immediate) program pointer and data pointer designations are initialized. Also, this technique allows scratchpad registers in R to be used to hold general data. By employing increment or decrement instructions, such registers may be used as loop counters.

The Q Flip Flop

An internal flip flop, Q, can be set or reset by instruction and can be sensed by conditional branch instructions. The output of Q is also available as a microprocessor output.

Interrupt Servicing

Register R(1) is always used as the program counter whenever interrupt servicing is initiated. When an interrupt request occurs and the interrupt is allowed by the program (again, nothing takes place until the completion of the current instruction), the contents of the X and P registers are stored in the temporary register T, and X and P are set to new values; hex digit 2 in X and hex digit 1 in P. Interrupt Enable is automatically de-activated to inhibit further interruptions. The user's interrupt routine is now in control; the contents of T may be saved by means of a single instruction (78) in the memory location pointed to by R(X). At the conclusion of the interrupt, the user's routine may restore the pre-interrupted value of X and P with a single instruction (70 or 71). The Interrupt-Enable flip flop can be activated to permit further interrupts or can be disabled to prevent them.

CPU Register Summary

D	8 Bits	Data Register (Accumulator)
DF	1 Bit	Data Flag (ALU Carry)
B	8 Bits	Auxiliary Holding Register
R	16 Bits	1 of 16 Scratchpad Registers
P	4 Bits	Designates which register is Program Counter
X	4 Bits	Designates which register is Data Pointer

N	4 Bits	Holds Low-Order Instr. Digit
I	4 Bits	Holds High-Order Instr. Digit
T	8 Bits	Holds old X, P after Interrupt (X is high nibble)
IE	1 Bit	Interrupt Enable
Q	1 Bit	Output Flip Flop

CDP1802 Control Modes

The $\overline{\text{WAIT}}$ and $\overline{\text{CLEAR}}$ lines provide four control modes as listed in the following truth table:

$\overline{\text{CLEAR}}$	$\overline{\text{WAIT}}$	MODE
L	L	LOAD
L	H	RESET
H	L	PAUSE
H	H	RUN

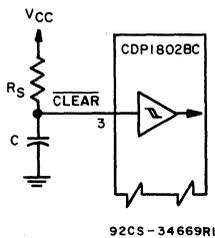
The function of the modes are defined as follows:

Load

Holds the CPU in the IDLE execution state and allows an I/O device to load the memory without the need for a "bootstrap" loader. It modifies the IDLE condition so that DMA-IN operation does not force execution of the next instruction.

Reset

Registers I, N, Q are reset, IE is set and 0's (V_{SS}) are placed on the data bus. TPA and TPB are suppressed while reset is held and the CPU is placed in S1. The first machine cycle after termination of reset is an initialization cycle which requires 9 clock pulses. During this cycle the CPU remains in S1 and registers X, P, and R(0) are reset. Interrupt and DMA servicing are suppressed during the initialization cycle. The next cycle is an S0, S1, or an S2 but never an S3. With the use of a 71 instruction followed by 00 at memory locations 0000 and 0001, this feature may be used to reset IE, so as to preclude interrupts until ready for them. Powerup reset can be realized by connecting an RC network directly to the CLEAR pin, since it has a Schmitt-triggered input, see Fig. 10.



The RC time constant should be greater than the oscillator start-up time (typically 20 ms).

Fig. 10 - Reset diagram.

Pause

Stops the internal CPU timing generator on the first negative high-to-low transition of the input clock. The oscillator continues to operate, but subsequent clock transitions are ignored.

Run

May be initiated from the Pause or Reset mode functions. If initiated from Pause, the CPU resumes operation on the first negative high-to-low transition of the input clock. When initiated from the Reset operation, the first machine cycle following Reset is always the initialization cycle. The initialization cycle is then followed by a DMA (S2) cycle or fetch (S0) from location 0000 in memory.

RUN-MODE STATE TRANSITIONS

The CDP1802BC CPU state transitions when in the RUN and RESET modes are shown in Fig. 11. Each machine cycle requires the same period of time, 8 clock pulses, except the initialization cycle, which requires 9 clock pulses. The execution of an instruction requires either two or three machine cycles, S0 followed by a single S1 cycle or two S1 cycles. S2 is the response to a DMA request and S3 is the interrupt response. Table II shows the conditions on Data Bus and Memory-Address lines during all machine states.

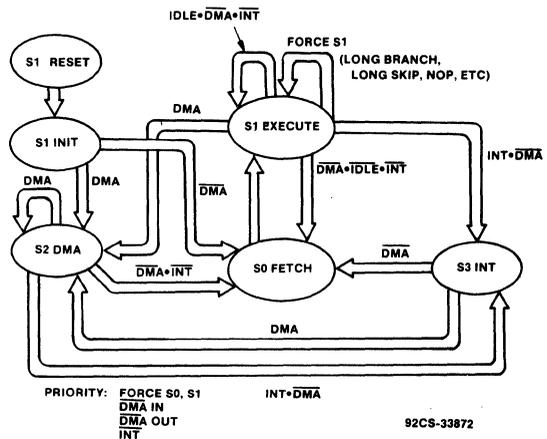


Fig. 11 - State transition diagram.

INSTRUCTION SET

The CPU instruction summary is given in Table I. Hexadecimal notation is used to refer to the 4-bit binary codes.

In all registers bits are numbered from the least significant bit (LSB) to the most significant bit (MSB) starting with 0.

R(W): Register designated by W, where W=N or X, or P

R(W).0: Lower-order byte of R(W)
R(W).1: Higher-order byte of R(W)

Operation Notation

$M(R(N)) \rightarrow D; R(N) + 1 \rightarrow R(N)$

This notation means: The memory byte pointed to by R(N) is loaded into D, and R(N) is incremented by 1.

TABLE I — INSTRUCTION SUMMARY (See Notes following table, pp. 11 and 12)

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
MEMORY REFERENCE			
LOAD VIA N	LDN	0N	$M(R(N)) \rightarrow D; \text{FOR } N \text{ NOT } 0$
LOAD ADVANCE	LDA	4N	$M(R(N)) \rightarrow D; (RN)+1 \rightarrow R(N)$
LOAD VIA X	LDX	F0	$M(R(X)) \rightarrow D$
LOAD VIA X AND ADVANCE	LDXA	72	$M(R(X)) \rightarrow D; R(X)+1 \rightarrow R(X)$
LOAD IMMEDIATE	LDI	F8	$M(R(P)) \rightarrow D; R(P)+1 \rightarrow R(P)$
STORE VIA N	STR	5N	$D \rightarrow M(R(N))$
STORE VIA X AND DECREMENT	STXD	73	$D \rightarrow M(R(X)); R(X)-1 \rightarrow R(X)$
REGISTER OPERATIONS			
INCREMENT REG N	INC	1N	$R(N)+1 \rightarrow R(N)$
DECREMENT REG N	DEC	2N	$R(N)-1 \rightarrow R(N)$
INCREMENT REG X	IRX	60	$R(X)+1 \rightarrow R(X)$
GET LOW REG N	GLO	8N	$R(N).0 \rightarrow D$
PUT LOW REG N	PLO	AN	$D \rightarrow R(N).0$
GET HIGH REG N	GHI	9N	$R(N).1 \rightarrow D$
PUT HIGH REG N	PHI	BN	$D \rightarrow R(N).1$
LOGIC OPERATIONS †			
OR	OR	F1	$M(R(X)) \text{ OR } D \rightarrow D$
OR IMMEDIATE	ORI	F9	$M(R(P)) \text{ OR } D \rightarrow D;$ $R(P)+1 \rightarrow R(P)$
EXCLUSIVE OR	XOR	F3	$M(R(X)) \text{ XOR } D \rightarrow D$
EXCLUSIVE OR IMMEDIATE	XRI	FB	$M(R(P)) \text{ XOR } D \rightarrow D;$ $R(P)+1 \rightarrow R(P)$
AND	AND	F2	$M(R(X)) \text{ AND } D \rightarrow D$
AND IMMEDIATE	ANI	FA	$M(R(P)) \text{ AND } D \rightarrow D;$ $R(P)+1 \rightarrow R(P)$
SHIFT RIGHT	SHR	F6	SHIFT D RIGHT, LSB(D) → DF, 0 → MSB(D)
SHIFT RIGHT WITH CARRY	SHRC	76§	SHIFT D RIGHT, LSB(D) → DF, DF → MSB(D)
RING SHIFT RIGHT	RSHR		
SHIFT LEFT	SHL	FE	SHIFT D LEFT, MSB(D) → DF, 0 → LSB(D)
SHIFT LEFT WITH CARRY	SHLC	7E§	SHIFT D LEFT, MSB(D) → DF, DF → LSB(D)
RING SHIFT LEFT	RSHL		

TABLE I — INSTRUCTION SUMMARY (Cont'd)

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
ARITHMETIC OPERATIONS †			
ADD	ADD	F4	$M(R(X))+D \rightarrow DF, D$
ADD IMMEDIATE	ADI	FC	$M(R(P))+D \rightarrow DF, D; R(P)+1 \rightarrow R(P)$
ADD WITH CARRY	ADC	74	$M(R(X))+D+DF \rightarrow DF, D$
ADD WITH CARRY, IMMEDIATE	ADCI	7C	$M(R(P))+D+DF \rightarrow DF, D$ $R(P)+1 \rightarrow R(P)$
SUBTRACT D	SD	F5	$M(R(X))-D \rightarrow DF, D$
SUBTRACT D IMMEDIATE	SDI	FD	$M(R(P))-D \rightarrow DF, D;$ $R(P)+1 \rightarrow R(P)$
SUBTRACT D WITH BORROW	SDB	75	$M(R(X))-D-(NOT DF) \rightarrow DF, D$
SUBTRACT D WITH BORROW, IMMEDIATE	SDBI	7D	$M(R(P))-D-(NOT DF) \rightarrow DF, D;$ $R(P)+1 \rightarrow R(P)$
SUBTRACT MEMORY	SM	F7	$D-M(R(X)) \rightarrow DF, D$
SUBTRACT MEMORY IMMEDIATE	SMI	FF	$D-M(R(P)) \rightarrow DF, D;$ $R(P)+1 \rightarrow R(P)$
SUBTRACT MEMORY WITH BORROW	SMB	77	$D-M(R(X))-(NOT DF) \rightarrow DF, D$
SUBTRACT MEMORY WITH BORROW, IMMEDIATE	SMBI	7F	$D-M(R(P))-(NOT DF) \rightarrow DF, D$ $R(P)+1 \rightarrow R(P)$
BRANCH INSTRUCTIONS—SHORT BRANCH			
SHORT BRANCH	BR	30	$M(R(P)) \rightarrow R(P).0$
NO SHORT BRANCH (SEE SKP)	NBR	38§	$R(P)+1 \rightarrow R(P)$
SHORT BRANCH IF D=0	BZ	32	IF D=0, $M(R(P)) \rightarrow R(P).0$ ELSE $R(P)+1 \rightarrow R(P)$
SHORT BRANCH IF D NOT 0	BNZ	3A	IF D NOT 0, $M(R(P)) \rightarrow R(P).0$ ELSE $R(P)+1 \rightarrow R(P)$
SHORT BRANCH IF DF=1	BDF	33§	IF DF=1, $M(R(P)) \rightarrow R(P).0$ ELSE $R(P)+1 \rightarrow R(P)$
SHORT BRANCH IF POS OR ZERO	BPZ		
SHORT BRANCH IF EQUAL OR GREATER	BGE		
SHORT BRANCH IF DF=0	BNF	3B§	IF DF=0, $M(R(P)) \rightarrow R(P).0$ ELSE $R(P)+1 \rightarrow R(P)$
SHORT BRANCH IF MINUS	BM		
SHORT BRANCH IF LESS	BL		
SHORT BRANCH IF Q=F	BQ	31	IF Q=1, $M(R(P)) \rightarrow R(P).0$ ELSE $R(P)+1 \rightarrow R(P)$
SHORT BRANCH IF Q=0	BNQ	39	IF Q=0, $M(R(P)) \rightarrow R(P).0$ ELSE $R(P)+1 \rightarrow R(P)$
SHORT BRANCH IF EF1=1 ($\overline{EF1}=V_{SS}$)	B1	34	IF EF1=1, $M(R(P)) \rightarrow R(P).0$ ELSE $R(P)+1 \rightarrow R(P)$
SHORT BRANCH IF EF1=0 ($\overline{EF1}=V_{CC}$)	BN1	3C	IF EF1=0, $M(R(P)) \rightarrow R(P).0$ ELSE $R(P)+1 \rightarrow R(P)$
SHORT BRANCH IF EF2=1 ($\overline{EF2}=V_{SS}$)	B2	35	IF EF2=1, $M(R(P)) \rightarrow R(P).0$ ELSE $R(P)+1 \rightarrow R(P)$
SHORT BRANCH IF EF2=0 ($\overline{EF2}=V_{CC}$)	BN2	3D	IF EF2=0, $M(R(P)) \rightarrow R(P).0$ ELSE $R(P)+1 \rightarrow R(P)$
SHORT BRANCH IF EF3=1 ($\overline{EF3}=V_{SS}$)	B3	36	IF EF3=1, $M(R(P)) \rightarrow R(P).0$ ELSE $R(P)+1 \rightarrow R(P)$
SHORT BRANCH IF EF3=0 ($\overline{EF3}=V_{CC}$)	BN3	3E	IF EF3=0, $M(R(P)) \rightarrow R(P).0$ ELSE $R(P)+1 \rightarrow R(P)$

TABLE I — INSTRUCTION SUMMARY (Cont'd)

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
BRANCH INSTRUCTIONS—SHORT BRANCH			
SHORT BRANCH IF EF4=1 (EF4=V _{SS})	B4	37	IF EF4=1, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH IF EF4=0 (EF4=V _{CC})	BN4	3F	IF EF4=0, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
BRANCH INSTRUCTIONS—LONG BRANCH			
LONG BRANCH	LBR	C0	M(R(P))→R(P).1 M(R(P)+1)→R(P).0
NO LONG BRANCH (SEE LSKP)	NLBR	C8§	R(P)+2→R(P)
LONG BRANCH IF D=0	LBZ	C2	IF D=0, M(R(P))→R(P).1 M(R(P)+1)→R(P).0 ELSE R(P)+2→R(P)
LONG BRANCH IF D NOT 0	LBNZ	CA	IF D NOT 0, M(R(P))→R(P).1 M(R(P)+1)→R(P).0 ELSE R(P)+2→R(P)
LONG BRANCH IF DF=1	LBDF	C3	IF DF=1, M(R(P))→R(P).1 M(R(P)+1)→R(P).0 ELSE R(P)+2→R(P)
LONG BRANCH IF DF=0	LBNF	CB	IF DF=0, M(R(P))→R(P).1 M(R(P)+1)→R(P).0 ELSE R(P)+2→R(P)
LONG BRANCH IF Q=1	LBQ	C1	IF Q=1, M(R(P))→R(P).1 M(R(P)+1)→R(P).0 ELSE R(P)+2→R(P)
LONG BRANCH IF Q=0	LBNQ	C9	IF Q=0, M(R(P))→R(P).1 M(R(P)+1)→R(P).0 ELSE R(P)+2→R(P)
SKIP INSTRUCTIONS			
SHORT SKIP (SEE NBR)	SKP	38§	R(P)+1→R(P)
LONG SKIP (SEE NLBR)	LSKP	C8§	R(P)+2→R(P)
LONG SKIP IF D=0	LSZ	CE	IF D=0, R(P)+2→R(P) ELSE CONTINUE
LONG SKIP IF D NOT 0	LSNZ	C6	IF D NOT 0, R(P)+2→R(P) ELSE CONTINUE
LONG SKIP IF DF=1	LSDF	CF	IF DF=1, R(P)+2→R(P) ELSE CONTINUE
LONG SKIP IF DF=0	LSNF	C7	IF DF=0, R(P)+2→R(P) ELSE CONTINUE
LONG SKIP IF Q=1	LSQ	CD	IF Q=1, R(P)+2→R(P) ELSE CONTINUE
LONG SKIP IF Q=0	LSNQ	C5	IF Q=0, R(P)+2→R(P) ELSE CONTINUE
LONG SKIP IF IE=1	LSIE	CC	IF IE=1, R(P)+2→R(P) ELSE CONTINUE

TABLE I — INSTRUCTION SUMMARY (Cont'd)

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
CONTROL INSTRUCTIONS			
IDLE	IDL	00#	WAIT FOR DMA OR INTERRUPT; M(R(0))—BUS
NO OPERATION	NOP	C4	CONTINUE
SET P	SEP	DN	N→P
SET X	SEX	EN	N→X
SET Q	SEQ	7B	1→Q
RESET Q	REQ	7A	0→Q
SAVE	SAV	78	T→M(R(X))
PUSH X,P TO STACK	MARK	79	(X,P)→T; (X,P)→M(R(2)) THEN P→X; R(2)→1→R(2)
RETURN	RET	70	M(R(X))→(X,P); R(X)+1→R(X) 1→IE
DISABLE	DIS	71	M(R(X))→(X,P); R(X)+1→R(X) 0→IE
INPUT-OUTPUT BYTE TRANSFER			
OUTPUT 1	OUT 1	61	M(R(X))→BUS;R(X)+1→R(X); N LINES=1
OUTPUT 2	OUT 2	62	M(R(X))→BUS;R(X)+1→R(X); N LINES=2
OUTPUT 3	OUT 3	63	M(R(X))→BUS;R(X)+1→R(X); N LINES=3
OUTPUT 4	OUT 4	64	M(R(X))→BUS;R(X)+1→R(X); N LINES=4
OUTPUT 5	OUT 5	65	M(R(X))→BUS;R(X)+1→R(X); N LINES=5
OUTPUT 6	OUT 6	66	M(R(X))→BUS;R(X)+1→R(X); N LINES=6
OUTPUT 7	OUT 7	67	M(R(X))→BUS;R(X)+1→R(X); N LINES=7
INPUT 1	INP 1	69	BUS→M(R(X)); BUS→D; N LINES=1
INPUT 2	INP 2	6A	BUS→M(R(X)); BUS→D; N LINES=2
INPUT 3	INP 3	6B	BUS→M(R(X)); BUS→D; N LINES=3
INPUT 4	INP 4	6C	BUS→M(R(X)); BUS→D; N LINES=4
INPUT 5	INP 5	6D	BUS→M(R(X)); BUS→D; N LINES=5
INPUT 6	INP 6	6E	BUS→M(R(X)); BUS→D; N LINES=6
INPUT 7	INP 7	6F	BUS→M(R(X)); BUS→D; N LINES=7

§THE ARITHMETIC OPERATIONS AND THE SHIFT INSTRUCTIONS ARE THE ONLY INSTRUCTIONS THAT CAN ALTER THE DF. AFTER AN ADD INSTRUCTION:

- DF=1 DENOTES A CARRY HAS OCCURRED
- DF=0 DENOTES A CARRY HAS NOT OCCURRED

AFTER A SUBTRACT INSTRUCTION:

- DF=1 DENOTES NO BORROW. D IS A TRUE POSITIVE NUMBER
- DF=0 DENOTES A BORROW. D IS TWO'S COMPLEMENT
- THE SYNTAX "--(NOT DF)" DENOTES THE SUBTRACTION OF THE BORROW

§THIS INSTRUCTION IS ASSOCIATED WITH MORE THAN ONE MNEMONIC. EACH MNEMONIC IS INDIVIDUALLY LISTED.

*AN IDLE INSTRUCTION INITIATES A REPEATING S1 CYCLE. THE PROCESSOR WILL CONTINUE TO IDLE UNTIL AN I/O REQUEST (INTERRUPT, DMA-IN, OR DMA-OUT) IS ACTIVATED. WHEN THE REQUEST IS ACKNOWLEDGED, THE IDLE CYCLE IS TERMINATED AND THE I/O REQUEST IS SERVICED, AND THEN NORMAL OPERATION IS RESUMED.

Notes for TABLE I

1. Long-Branch, Long-Skip and No Op instructions are the only instructions that require three cycles to complete (1 fetch +2 execute).

Long-Branch instructions are three bytes long. The first byte specifies the condition to be tested; and the second and third byte, the branching address.

The long-branch instructions can:

- a) Branch unconditionally
- b) Test for D=0 or D≠0
- c) Test for DF=0 or DF=1
- d) Test for Q=0 or Q=1

e) effect an unconditional no branch

If the tested condition is met, then branching takes place; the branching address bytes are loaded in the high- and low-order bytes of the current program counter, respectively. This operation effects a branch to any memory location.

If the tested condition is not met, the branching address bytes are skipped over, and the next instruction in sequence is fetched and executed. This operation is taken for the case of unconditional no branch (NLBR).

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $C_L = 50$ pF, $V_{DD} \pm 5\%$, except as noted.

CHARACTERISTIC	VCC (V)	VDD (V)	LIMITS		UNITS	
			Typ.*	Max.		
Propagation Delay Times:						
Clock to TPA, TPB	t_{PLH}, t_{PHL}	5	5	200	300	ns
Clock-to-Memory High-Address Byte	t_{PLH}, t_{PHL}	5	5	475	525	
Clock-to-Memory Low-Address Byte Valid	t_{PLH}, t_{PHL}	5	5	175	250	
Clock to MRD	t_{PLH}, t_{PHL}	5	5	175	275	
Clock to MWR	t_{PLH}, t_{PHL}	5	5	175	225	
Clock to (CPU DATA to BUS) Valid	t_{PLH}, t_{PHL}	5	5	250	375	
Clock to State Code	t_{PLH}, t_{PHL}	5	5	250	400	
Clock to Q	t_{PLH}, t_{PHL}	5	5	200	300	
Clock to N (0-2)	t_{PLH}, t_{PHL}	5	5	275	350	
Minimum Setup and Hold Times:						
Data Bus Input Setup	t_{SU}	5	5	-20	0	
Data Bus Input Hold	t_{H}^{\square}	5	5	125	150	
DMA Setup	t_{SU}	5	5	0	30	
DMA Hold	t_{H}^{\square}	5	5	100	150	
Interrupt Setup	t_{SU}	5	5	-75	0	
Interrupt Hold	t_{H}^{\square}	5	5	75	125	
WAIT Setup	t_{SU}	5	5	20	40	
EF1-4 Setup	t_{SU}	5	5	-30	0	
EF1-4 Hold	t_{H}^{\square}	5	5	100	150	
Minimum Pulse Width Times:						
CLEAR Pulse Width	t_{WL}^{\square}	5	5	100	150	
CLOCK Pulse Width	t_{WL}	5	5	90	100	

*Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .

■Maximum limits of minimum characteristics are the values above which all devices function.

Notes for TABLE I (Continued)

2. The short-branch instructions are two bytes long. The first byte specifies the condition to be tested, and the second specifies the branching address.

The short-branch instruction can:

- Branch unconditionally
- Test for $D=0$ or $D \neq 0$
- Test for $DF=0$ or $DF=1$
- Test for $Q=0$ or $Q=1$
- Test the status (1 or 0) of the four EF flags
- Effect an unconditional no branch

If the tested condition is met, then branching takes place; the branching address byte is loaded into the low-order byte position of the current program counter. This effects a branch within the current 256-byte page of the memory, i.e., the page which holds the branching address. If the tested condition is not met, the branching address byte is skipped over, and the next instruction in sequence is fetched and executed. This same action is taken in the case of unconditional no branch (NBR).

3. The skip instructions are one byte long. There is one Unconditional Short-Skip (SKP) and eight Long-Skip instructions.

The Unconditional Short-Skip instruction takes 2 cycles to complete (1 fetch + 1 execute). Its action is to skip over the byte following it. Then the next instruction in sequence is fetched and executed. This SKP instruction is identical to the unconditional no-branch instruction (NBR) except that the skipped-over byte is not considered part of the program.

The Long-Skip instructions take three cycles to complete (1 fetch + 2 execute).

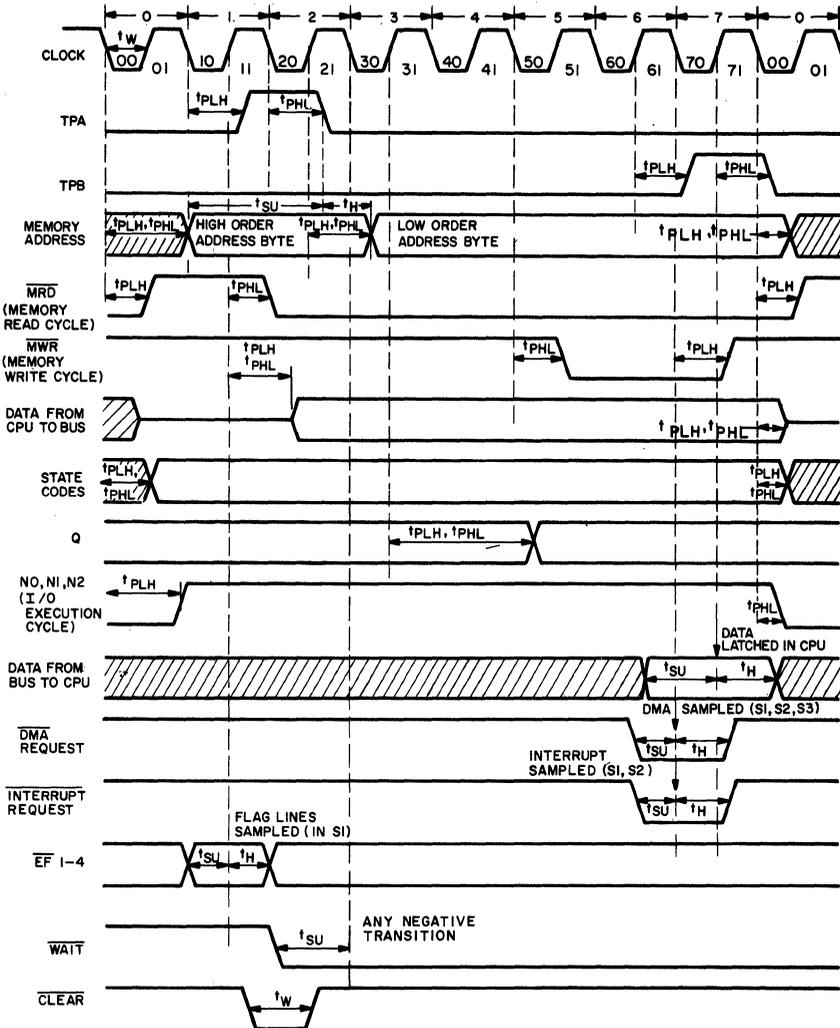
They can:

- Skip unconditionally
- Test for $D=0$ or $D \neq 0$
- Test for $DF=0$ or $DF=1$
- Test for $Q=0$ or $Q=1$
- Test for $IE=1$

If the tested condition is met, then Long Skip takes place; the current program counter is incremented twice. Thus two bytes are skipped over and the next instruction in sequence is fetched and executed. If the tested condition is not met, then no action is taken.

Execution is continued by fetching the next instruction in sequence.

RCA CMOS LSI Products
CDP1802BC



- NOTES:
1. THIS TIMING DIAGRAM IS USED TO SHOW SIGNAL RELATIONSHIPS ONLY AND DOES NOT REPRESENT ANY SPECIFIC MACHINE CYCLE
 2. ALL MEASUREMENTS ARE REFERENCED TO 50% POINT OF THE WAVEFORMS
 3. SHADED AREAS INDICATE "DON'T CARE" OR UNDEFINED STATE; MULTIPLE TRANSITIONS MAY OCCUR DURING THIS PERIOD

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Fig. 12 - Timing waveforms.

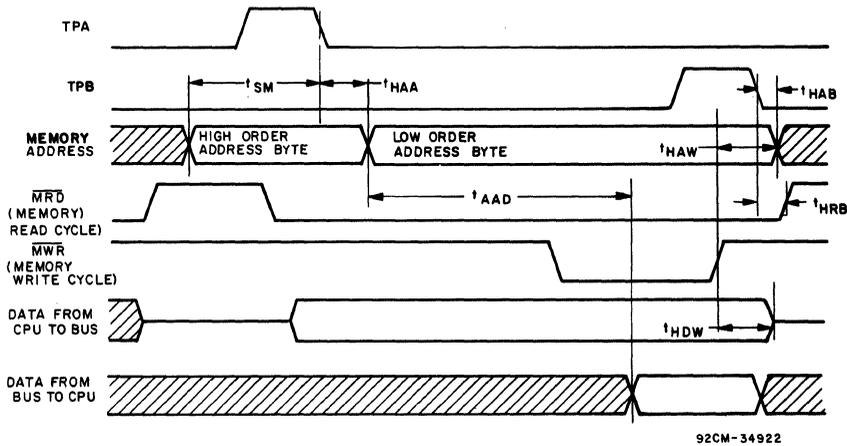


Fig. 13 - Clock frequency dependent relative timing waveforms.

TIMING SPECIFICATIONS as a function of T ($T=1/f_{CLOCK}$) at $T_A=-40$ to $+85^\circ\text{C}$.

CHARACTERISTIC	VCC (V)	VDD (V)	LIMITS		UNITS
			Min.	Typ.*	
High-Order Memory-Address Byte Set Up to TPA Time	5	5	2T-325	2T-275	ns
High-Order Memory-Address Byte Hold after TPA Time	5	5	T/2-25	T/2-15	
Low-Order Memory-Address Byte Hold after WR Time	5	5	T-30	T+0	
CPU Data to Bus Hold after WR Time	5	5	T-175	T-125	
Low-Order Memory-Address Byte Hold after TPB Time	5	5	T/2+0	T/2+100	
MRD Hold after TPB Time	5	5	T/2-25	T/2+0	
Required Memory Access Time Address to Data	5	5	5T-225	5T-175	

*Typical values are for $T_A=25^\circ\text{C}$ and nominal V_{DD} .

TABLE II. CONDITIONS ON DATA BUS AND MEMORY ADDRESS LINES DURING ALL MACHINE STATES

STATE	I	N	MNEMONIC	OPERATION	DATA BUS	MEMORY ADDRESS	$\overline{\text{MRD}}$	$\overline{\text{MWR}}$	N LINES	NOTES ^G
S1			RESET	0-I,N,Q,X,P; 1-IE	00	XXXX	1	1	0	A
S1			INITIALIZE NOT PROGRAMMER ACCESSIBLE	0000-R	00	XXXX	1	1	0	B
S0			FETCH	MRP-I, N; RP+1-RP	MRP	RP	0	1	0	C
S1	0	0	IDL	IDLE	MR0	R0	0	1	0	D,3
	0	1-F	LDN	MRN-D	MRN	RN	0	1	0	3
	1	0-F	INC	RN+1-RN	FLOAT	RN	1	1	0	1
	2	0-F	DEC	RN-1-RN	FLOAT	RN	1	1	0	1
	3	0-F	SHORT BRANCH	TAKEN; MRP-RP,0 NOT TAKEN; RP+1-RP	MRP	RP	0	1	0	3
	4	0-F	LDA	MRN-D; RN+1-RN	MRN	RN	0	1	0	3
	5	0-F	STR	D-MRN	D	RN	1	0	0	2
	6	0	IRX	RX+1-RX	MRX	RX	0	1	0	2
	6	1	OUT 1	MRX-BUS; RX+1-RX	MRX	RX	0	1	1	6
		2	OUT 2						2	
		3	OUT 3						3	
		4	OUT 4						4	
		5	OUT 5						5	
		6	OUT 6						6	
		7	OUT 7						7	
	6	9	INP 1	BUS-MRX,D	DATA FROM I/O DEVICE	RX	1	0	1	5
		A	INP 2						2	
B		INP 3	3							
C		INP 4	4							
D		INP 5	5							
E		INP 6	6							
F		INP 7	7							
7	0	RET	MRX-(X,P); RX+1-RX; 1-IE	MRX	RX	0	1	0	3	
	1	DIS	MRX-(X,P); RX+1-RX; 0-IE	MRX	RX	0	1	0	3	
	2	LDXA	MRX-D; RX+1-RX	MRX	RX	0	1	0	3	
	3	STXD	D-MRX; RX-1-RX	D	RX	1	0	0	2	
	4	ADC	MRX+D+ DF-DF,D	MRX	RX	0	1	0	3	

TABLE II. CONDITIONS ON DATA BUS AND MEMORY ADDRESS LINES DURING ALL MACHINE STATES (CONT'D)

STATE	I	N	MNEMONIC	OPERATION	DATA BUS	MEMORY ADDRESS	$\overline{\text{MRD}}$	$\overline{\text{MWR}}$	N LINES	NOTES ^G
S1	7	5	SDB	MRX-D- DFN-DF,D	MRX	RX	0	1	0	3
		6	SHRC	LSB(D)-DF; DF-MSB(D)	FLOAT	RX	1	1	0	1
		7	SMB	D-MRX- DFN-DF,D	MRX	RX	0	1	0	3
		8	SAV	T-MRX	T	RX	1	0	0	2
		9	MARK	(X,P)-T, MR2; P-X; R2-1-R2	T	R2	1	0	0	2
		A	REQ	0-Q	FLOAT	RP	1	1	0	1
		B	SEQ	1-Q	FLOAT	RP	1	1	0	1
		C	ADCI	MRP+D+ DF-DF,D; RP+1	MRP	RP	0	1	0	3
		D	SDBI	MRP-D- DFN-DF,D; RP+1	MRP	RP	0	1	0	3
	E	SHLC	MSB(D)-DF; DF-LSB(D)	FLOAT	RP	1	1	0	1	
	F	SMBI	D-MRP- DFN-DF,D; RP+1	MRP	RP	0	1	0	3	
	8	0-F	GLO	RN.0-D	RN.0	RN	1	1	0	1
	9	0-F	GHI	RN.1-D	RN.1	RN	1	1	0	1
A	0-F	PLO	D-RN.0	D	RN	1	1	0	1	
B	0-F	PHI	D-RN.1	D	RN	1	1	0	1	
S1#1	C	0-3, 8-B	LONG BRANCH	TAKEN: MRP-B; RP+1-RP	MRP	RP	0	1	0	4
#2				TAKEN: B-RP.1; MRP-RP.0	M(RP+1)	RP+1	0	1	0	4
S1#1				NOT TAKEN: RP+1-RP	MRP	RP	0	1	0	4
#2				NOT TAKEN: RP+1-RP	M(RP+1)	RP+1	0	1	0	4
S1#1		5 6 7 C D E F	LONG SKIP	TAKEN: RP+1-RP	MRP	RP	0	1	0	4
#2				TAKEN: RP+1-RP	M(RP+1)	RP+1	0	1	0	4
S1#1				NOT TAKEN: NO OPERATION	MRP	RP	0	1	0	4
#2				NOT TAKEN: NO OPERATION	MRP	RP	0	1	0	4
S1#1				NO OPERATION	MRP	RP	0	1	0	4
#2				NO OPERATION	MRP	RP	0	1	0	4
S1#1		4	NOP	NO OPERATION	MRP	RP	0	1	0	4
#2				NO OPERATION	MRP	RP	0	1	0	4

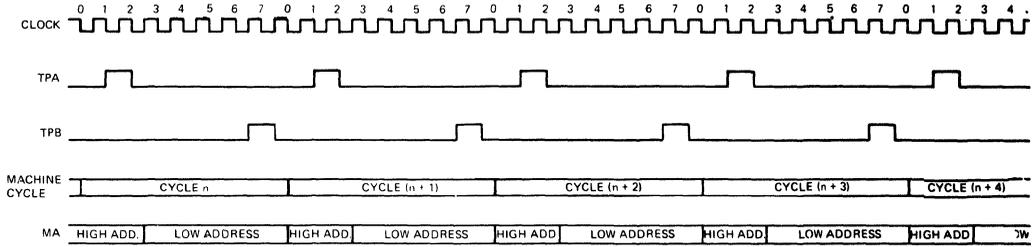
RCA CMOS LSI Products
CDP1802BC

TABLE II. CONDITIONS ON DATA BUS AND MEMORY ADDRESS LINES DURING ALL MACHINE STATES (CONT'D)

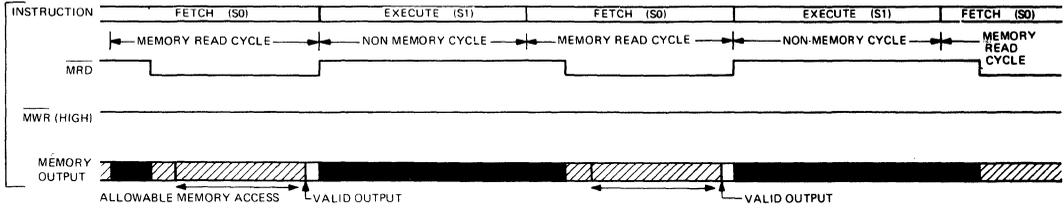
STATE	I	N	MNEMONIC	OPERATION	DATA BUS	MEMORY ADDRESS	MRD	MWR	N LINES	NOTES ^G
S1	D	0-F	SEP	N-P	NN	RN	1	1	0	1
	E	0-F	SEX	N-X	NN	RN	1	1	0	1
	F	0	LDX	MRX-D	MRX	RX	0	1	0	3
		1	OR	MRX OR D-D	MRX	RX	0	1	0	3
		2	AND	MRX AND D-D						
		3	XOR	MRX XOR D-D						
		4	ADD	MRX+D-DF,D						
		5	SD	MRX-D-DF,D						
		7	SM	D-MRX-DF,D						
		6	SHR	LSB(D)-DF; 0-MSB(D)	FLOAT	RX	1	1	0	1
		8	LDI	MRP-D; RP+1-RP	MRP	RP	0	1	0	3
		9	ORI	MRP OR D-D; RP+1-RP						
	A	ANI	MRP AND D-D; RP+1-RP							
	B	XRI	MRP XOR D-D; RP+1-RP							
	C	ADI	MRP+D-DF,D; RP+1-RP							
D	SDI	MRP-D-DF,D; RP+1-RP								
F	SMI	D-MRP-DF,D; RP+1-RP								
E	SHL	MSB(D)-DF; 0-LSB(D)	FLOAT	RP						
S2	DMA IN			BUS-MR0; R0+1-R0	DATA FROM I/O DEVICE	R0	1	0	0	F, 7
	DMA OUT			MR0-BUS; R0+1-R0	MR0	R0	0	1	0	F, 8
S3	INTERRUPT			X,P-T; 0-IE 1-P; 2-X	FLOAT	RN	1	1	0	9
S1	LOAD			IDLE (CLEAR, WAIT=0)	M(R0-1)	R0-1	0	1	0	E,3

NOTES:

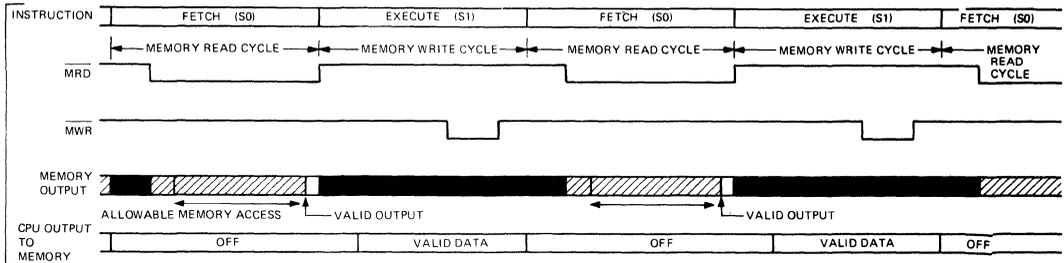
- A. IE=1, TPA, TPB suppressed, state=S1.
- B. BUS=0 for entire cycle.
- C. Next state always S1.
- D. Wait for DMA or INTERRUPT.
- E. Suppress TPA, wait for DMA.
- F. IN REQUEST has priority over OUT REQUEST.
- G. Number refers to machine cycle. See Fig. 14 timing waveforms for machine cycles 1 through 9.



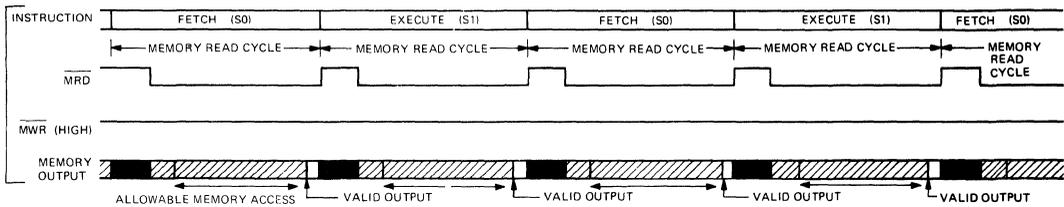
General timing waveforms.



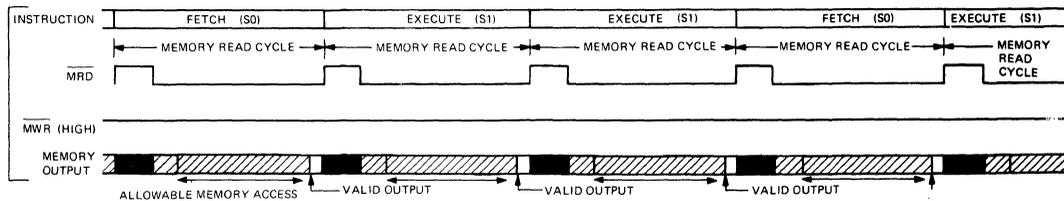
No. 1 Non-memory-cycle timing waveforms.



No. 2 Memory write-cycle timing waveforms.



No. 3 Memory read-cycle timing waveforms.



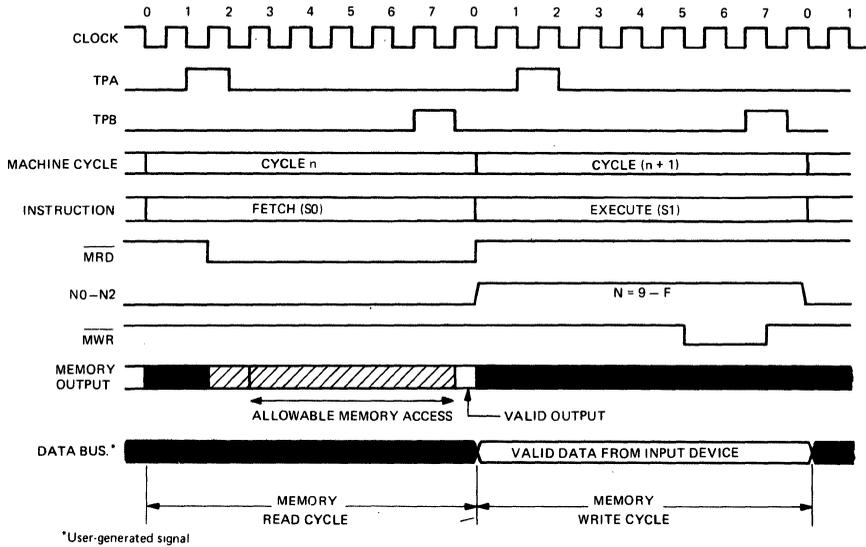
No. 4 Long-branch or long-skip-cycle timing waveforms.

"Don't Care" or internal delays.
 High-impedance state

92CL-29600

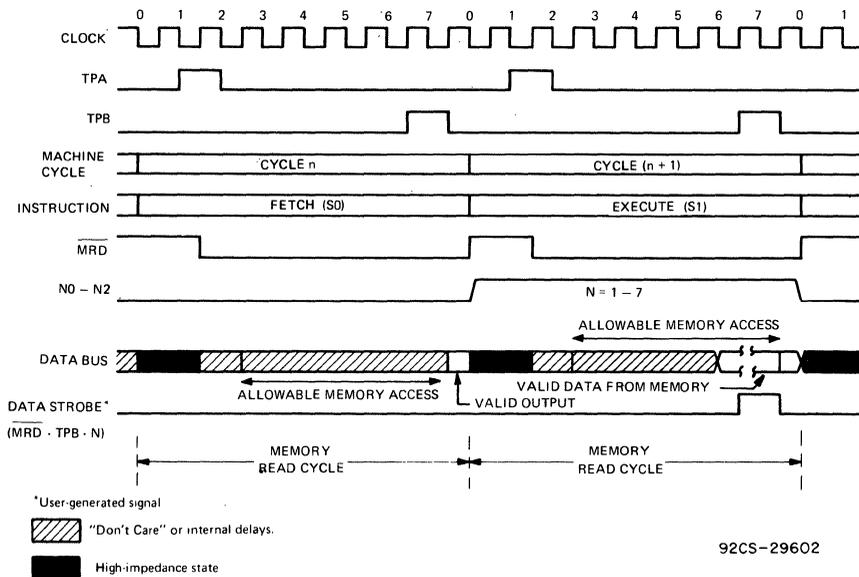
Fig. 14 - Machine-cycle timing waveforms (propagation delays not shown).

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92CS-29601

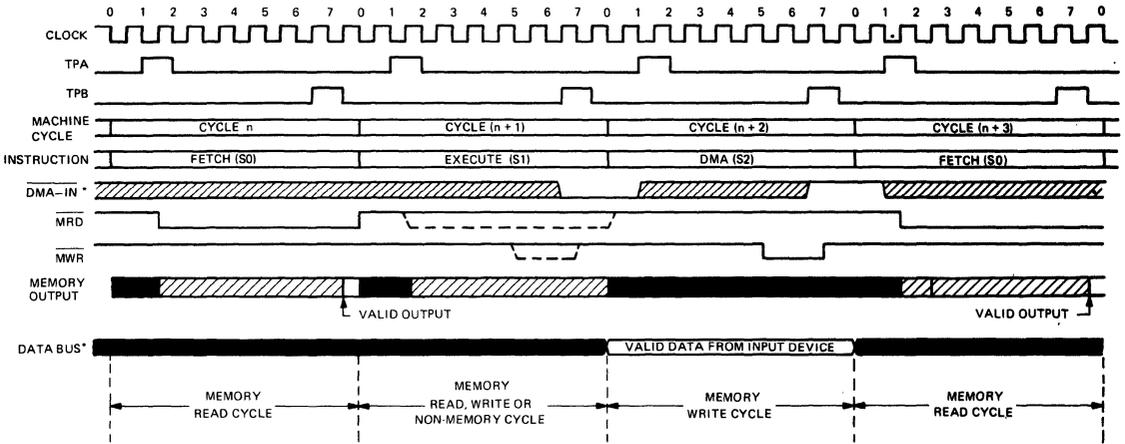
No. 5 Input-cycle timing waveforms.



92CS-29602

No. 6 Output-cycle timing waveforms.

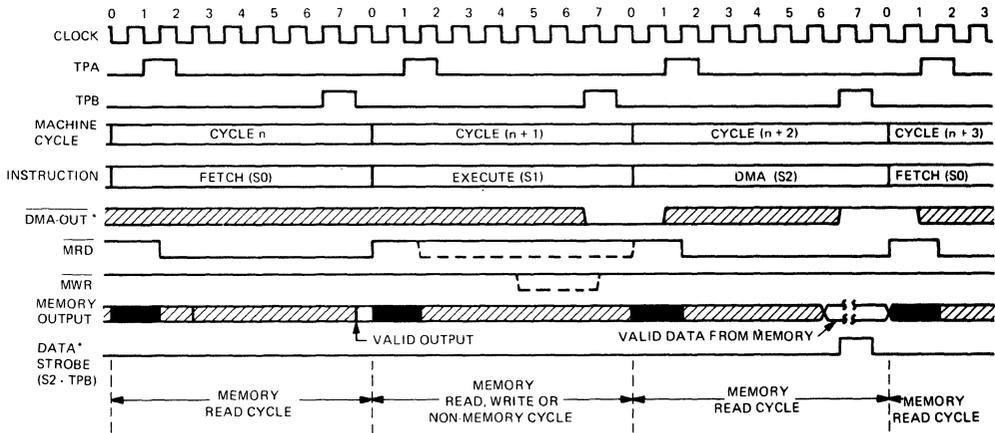
Fig. 14 - Machine-cycle timing waveforms (propagation delays not shown). Continued.



*User-generated signal

92CS-29603

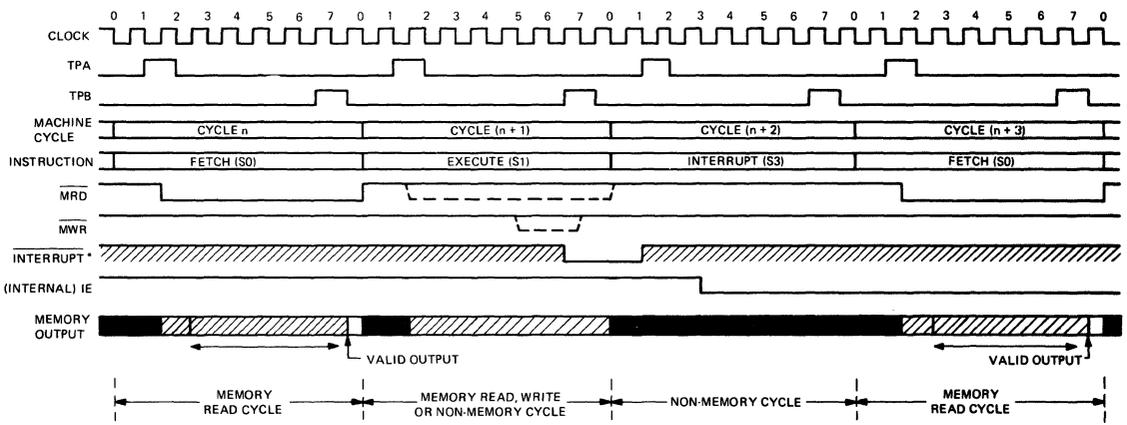
No. 7 DMA-IN-cycle timing waveforms.



*User-generated signal

92CM-29604R1

No. 8 DMA-OUT-cycle timing waveforms.



*User-generated signal

▨ "Don't Care" or internal delays. ■ High-impedance state

92CM-29605

No. 9 INTERRUPT-cycle timing waveforms.

Fig. 14 - Machine-cycle timing waveforms (propagation delays not shown). Continued.

CMOS 8-Bit Microcomputer With On-Chip RAM, ROM, and Timer/Counter

CLOCK	1	40	V _{DD}
WAIT	2	39	XTAL
CLEAR	3	38	DMA IN
Q	4	37	DMA OUT
SCI	5	36	INTERRUPT
SCO	6	35	MWR
MRD	7	34	TPA
BUS 7	8	33	TPB
BUS 6	9	32	MA7
BUS 5	10	31	MA6
BUS 4	11	30	MA5
BUS 3	12	29	MA4
BUS 2	13	28	MA3
BUS 1	14	27	MA2
BUS 0	15	26	MA1
EMS/M _E	16	25	MA0
N ₂	17	24	EFT
N ₁	18	23	EF2
N ₀	19	22	EF3
V _{SS}	20	21	EF4

TOP VIEW
 92CS-34980

TERMINAL ASSIGNMENT

Performance Features:

- Instruction time of 3.2 μs, -40 to +85°C
- 123 instructions-upwards software compatible with CDP1802, CDP1805, and CDP1806
- BCD arithmetic instructions
- Low-power IDLE mode
- Pin compatible with CDP1802, CDP1805, and CDP1806, except for V_{CC} terminal
- 64K-byte memory address capability

The RCA-CDP1804AC is a functional and performance enhancement of the CDP1802, CDP1805C, and CDP1806C LSI CMOS 8-bit register-oriented microprocessor series and is designed for use in a wide variety of general-purpose applications.

The CDP1804AC hardware enhancements include a 2K-byte ROM array, a 64-byte RAM array, and a 8-bit presetable down counter. The timer/counter, which generates an internal interrupt request, can be programmed for use in time-base, event-counting, and pulse-duration measurement applications. The timer/counter underflow output can also be directed to the Q output terminal.

The CDP1805AC and CDP1806AC which are identical to the CDP1804AC, except for the on-chip memory, should be used for CDP1804AC development purposes.

The CDP1804AC software enhancements include 22 more instructions than the CDP1802 and 10 more instructions than the CDP1805AC and CDP1806AC. The 32 new software

- 2K bytes of on-chip ROM
- 64 bytes of on-chip RAM
- 16 x 16 matrix of on-board registers
- On-chip crystal or RC controlled oscillator
- 8-bit timer/counter

instructions add subroutine call and return capability, enhanced data transfer manipulation, timer/counter control, improved interrupt handling, single-instruction loop counting, and BCD arithmetic.

Upwards software and hardware compatibility are maintained when substituting a CDP1804AC for other CDP1800-series microprocessors. Pinout is identical except for the replacement of V_{CC} with EMS/M_E.

The CDP1804AC has an operating voltage range of 4 V to 6.5 V and is supplied in a 40-lead hermetic dual-in-line ceramic package (D suffix), and in a 40-lead dual-in-line plastic package (E suffix).

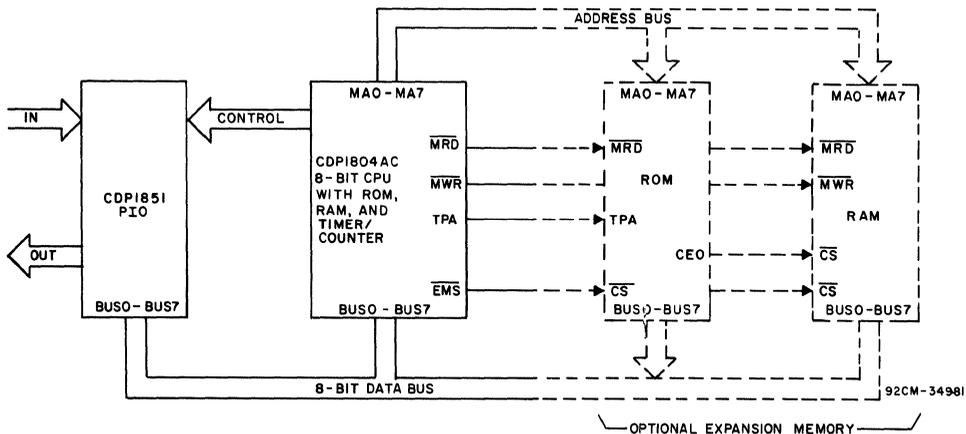


Fig. 1 - Typical CDP1804AC microprocessor system.

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD}):
 (Voltage referenced to V_{SS} Terminal) -0.5 to +7 V

INPUT VOLTAGE RANGE, ALL INPUTS -0.5 to V_{DD} +0.5 V

DC INPUT CURRENT, ANY ONE INPUT ± 10 mA

POWER DISSIPATION PER PACKAGE (P_D):
 For $T_A = -40$ to $+60^\circ\text{C}$ (PACKAGE TYPE E) 500 mW
 For $T_A = +60$ to $+85^\circ\text{C}$ (PACKAGE TYPE E) Derate Linearly at 12 mW/ $^\circ\text{C}$ to 200 mW
 For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE D) 500 mW
 For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE D) Derate Linearly at 12 mW/ $^\circ\text{C}$ to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR
 For $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$ 100 mW

OPERATING-TEMPERATURE RANGE (T_A):
 PACKAGE TYPE D -55 to $+125^\circ\text{C}$
 PACKAGE TYPE E -40 to $+85^\circ\text{C}$

STORAGE TEMPERATURE RANGE (T_{stg}) -85 to $+150^\circ\text{C}$

LEAD TEMPERATURE (DURING SOLDERING):
 At distance $1/16 \pm 1/32$ in. (1.59 ± 0.79 mm) from case for 10 s max. $+265^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS at $T_A = -40$ to $+85^\circ\text{C}$

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	CONDITION	LIMITS		UNITS
		CDP1804ACD CDP1804ACE		
		MIN.	MAX.	
DC Operating Voltage Range	—	4	6.5	V
Input Voltage Range	—	V_{SS}	V_{DD}	
Minimum Instruction Time* ($f_{CL}=5$ MHz)	5	3.2	—	μs
Maximum DMA Transfer Rate	5	—	0.625	Mbytes/s
Maximum Clock Input Frequency, Load Capacitance (CL) = 50 pF	5	DC	5	MHz
Maximum External Counter/Timer Clock Input Frequency to $\overline{EF1}$, $\overline{EF2}$ t_{CLX}	5	DC	2	

*Equals 2 machine cycles - one Fetch and one Execute operation for all instructions except Long Branch, Long Skip, NOP, and "68" family instructions, which are more than two cycles.

RCA CMOS LSI Products

CDP1804AC

STATIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} \pm 5\%$, Except as noted

CHARACTERISTIC		CONDITIONS			LIMITS			UNITS
		V_O (V)	V_{IN} (V)	V_{DD} (V)	CDP1804ACD, CDP1804ACE			
					Min.	Typ.*	Max.	
Quiescent Device Current	I_{DD}	—	0, 5	5	—	50	200	μA
Output Low Drive (Sink) Current (Except XTAL)	I_{OL}	0.4	0, 5	5	1.6	4	—	mA
XTAL Output	I_{OL}	0.4	5	5	0.2	0.4	—	
Output High Drive (Source) Current (Except XTAL)	I_{OH}	4.6	0, 5	5	-1.6	-4	—	
XTAL	I_{OH}	4.6	0	5	-0.1	-0.2	—	V
Output Voltage Low-Level	V_{OL}	—	0, 5	5	—	0	0.1	
Output Voltage High Level	V_{OH}	—	0, 5	5	4.9	5	—	
Input Low Voltage (BUS 0 — BUS 7, EMS/ME)	V_{IL}	0.5, 4.5	—	5	—	—	1.5	V
Input High Voltage (BUS 0 — BUS 7, EMS/ME)	V_{IH}	0.5, 4.5	—	5	3.5	—	—	
Schmitt Trigger Input Voltage (Except BUS 0 — BUS 7, EMS/ME)								
Positive Trigger Threshold	V_P				2.2	2.9	3.6	
Negative Trigger Threshold	V_N	0.5, 4.5	—	5	0.9	1.9	2.8	V
Hysteresis	V_H				0.3	0.9	1.6	
Input Leakage Current	I_{IN}	—	0.5	5	—	± 0.1	± 5	μA
3-State Output Leakage Current	I_{OUT}	0, 5	0, 5	5	—	± 0.2	± 5	μA
Input Capacitance	C_{IN}	—	—	—	—	5	7.5	pF
Output Capacitance	C_{OUT}	—	—	—	—	10	15	
Total Power Dissipation (f=5 MHz) Idle "00" at M(0000), $C_L = 50$ pF		—	—	5	—	1.5	3	mW
Minimum Data Retention Voltage	V_{DR}		$V_{DD} = V_{DR}$		—	2	2.4	V
Data Retention Current	I_{DR}		$V_{DD} = 2.4$		—	25	100	μA

*Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .

OPERATING AND HANDLING CONSIDERATIONS

1. Handling

All inputs and outputs of RCA CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in ICAN-6525 "Guide to Better Handling and Operation of CMOS Integrated Circuits."

2. Operating

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause $V_{DD} - V_{SS}$ to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{CC} nor less than V_{SS} . Input currents must not exceed 10 mA even when the power supply is off.

Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{CC} or V_{SS} , whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} , V_{CC} , or V_{SS} may damage CMOS devices by exceeding the maximum device dissipation.

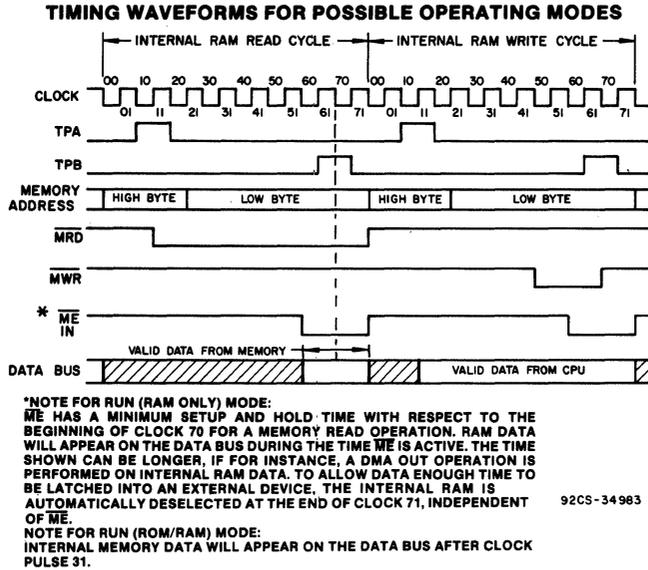


Fig. 3 - Internal memory operation timing waveforms for CDP1804AC.

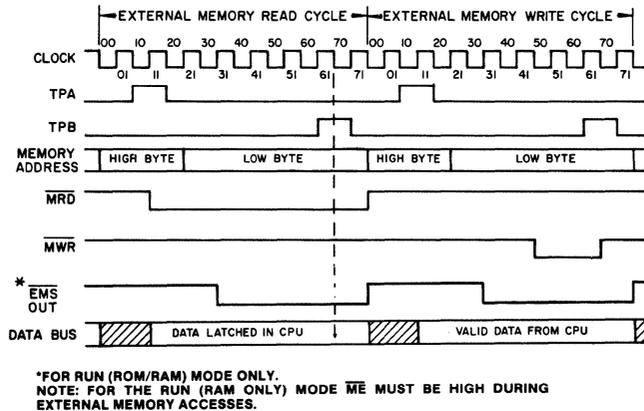


Fig. 4 - External memory operation timing waveforms for CDP1804AC.

SIGNAL DESCRIPTIONS

BUS 0 to BUS 7 (Data Bus):

8-bit bidirectional DATA BUS lines. These lines are used for transferring data between the memory, the microprocessor, and I/O devices.

N0 to N2 (I/O) Lines:

Activated by an I/O instruction to signal the I/O control logic of a data transfer between memory and I/O interface. These lines can be used to issue command codes or device

selection codes to the I/O devices. The N bits are low at all times except when an I/O instruction is being executed. During this time their state is the same as the corresponding bits in the N register. The direction of data flow is defined in the I/O instruction by bit N3 (internally) and is indicated by the level of the MRD signal:

- $\overline{MRD} = V_{DD}$: Data from I/O to CPU and Memory
- $\overline{MRD} = V_{SS}$: Data from Memory to I/O

SIGNAL DESCRIPTIONS (Cont'd)

EF1 to EF4 (4 Flags):

These inputs enable the I/O controllers to transfer status information to the processor. The levels can be tested by the conditional branch instructions. They can be used in conjunction with the INTERRUPT request line to establish interrupt priorities. The flag(s) are sampled at the end of every S0 cycle. One additional use for EF1 and EF2 is event counting and pulse-width measurement in conjunction with the Timer/Counter.

INTERRUPT, DMA-IN, DMA-OUT (3 I/O Requests)

These inputs are sampled by the CDP1804AC during TPB.

Interrupt Action: X and P are stored in T after executing current instruction; designator X is set to 2; designator P is set to 1; interrupt enable is reset to 0 (inhibit); and instruction execution is resumed. The interrupt action requires one machine cycle (S3).

DMA Action: Finish executing current instruction; R(0) points to memory area for data transfer; data is loaded into or read out of memory; and increment R(0).

Note: In the event of concurrent DMA and INTERRUPT requests, DMA-IN has priority followed by DMA-OUT and then INTERRUPT.

SC0, SC1, (2 State Code Lines):

These outputs indicate that the CPU is: 1) fetching an instruction, or 2) executing an instruction, or 3) processing a DMA request, or 4) acknowledging an interrupt request. The levels of state code are tabulated below. All states are valid at TPA.

State Type	State Code Lines	
	SC1	SC0
S0 (Fetch)	L	L
S1 (Execute)	L	H
S2 (DMA)	H	L
S3 (Interrupt)	H	H

H = V_{DD}, L = V_{SS}.

TPA, TPB (2 Timing Pulses):

Positive pulses that occur once in each machine cycle (TPB follows TPA). They are used by I/O controllers to interpret codes and to time interaction with the data bus. The trailing edge of TPA is used by the memory system to latch the high-order byte of the 16-bit memory address.

MA0 to MA7 (8 Memory Address Lines):

In each cycle, the higher-order byte of a 16-bit memory address appears on the memory address lines MA0-7 first. Those bits required by the memory system can be strobed into external address latches by timing pulse TPA. The low-order byte of the 16-bit address appears on the address lines 1/2 clock after the termination of TPA.

MWR (Write Pulse):

A negative pulse appearing in a memory-write cycle, after the address lines have stabilized.

MRD (Read Level):

A low level on MRD indicates a memory read cycle. It can be used to control three-state outputs from the addressed memory and to indicate the direction of data transfer during an I/O instruction.

Q:

Single bit output from the CPU which can be set or reset, between the trailing edge of TPA and the leading edge of TPB, under program control. The Enable Toggle Q command connects the Q-line flip-flop to the output of the counter, such that each time the counter decrements from 01 to its next value, the Q line changes state. This command is cleared by a LOAD COUNTER (LDC) instruction, a CPU reset, or a BRANCH COUNTER INTERRUPT (BCI) instruction with the counter interrupt flip-flop set.

CLOCK:

Input for externally generated single-phase clock. The maximum clock frequency is 5 MHz at V_{DD} = 5 V. The clock is counted down internally to 8 clock pulses per machine cycle.

XTAL:

Connection to be used with clock input terminal, for an external crystal, if the on-chip oscillator is utilized.

WAIT, CLEAR (2 Control Lines):

Provide four control modes as listed in the following truth table:

CLEAR	WAIT	MODE
L	L	RUN (ROM/RAM)
L	H	RESET
H	L	PAUSE
H	H	RUN (RAM ONLY)

ME (Memory Enable) RUN (RAM ONLY) Mode

This active low signal line is used to select or deselect the internal RAM. It must be active prior to clock 70 for an internal RAM access to take place. Internal RAM data will appear on the data bus during the time that ME is active (after clock 31). Thus, if this data is to be latched into an external device (i.e., during an OUTPUT instruction or DMA OUT cycle), ME should be wide enough to provide enough time for valid data to be latched.

In the RUN (RAM ONLY) mode the internal RAM is not internally mask-decoded. Decoding of the starting address is performed externally, and may reside in any 64-byte block of memory.

EMS (External Memory Select) RUN (ROM/RAM) Mode

This signal line is used for external memory expansion. It is low when external memory is being addressed and high at all other times. It is initiated 1.5 clock periods after TPA (at which time all addresses are stable) and terminates at the end of the cycle. Use of EMS for memory selection allows 3.5 clock cycles for data access.

V_{DD}, V_{SS} (Power Levels):

V_{SS} is the most negative supply voltage terminal and is normally connected to ground. V_{DD} is the positive supply voltage terminal. All outputs swing from V_{SS} to V_{DD}. The recommended input voltage swing is from V_{SS} to V_{DD}.

ARCHITECTURE

Fig. 2 shows a block diagram of the CDP1804AC. The principal feature of this system is a register array (R) consisting of sixteen 16-bit scratchpad registers. Individual registers in the array (R) are designated (selected) by a 4-bit binary code from one of the 4-bit registers labeled N, P, and X. The contents of any register can be directed to any one of the following three paths:

1. the external memory (multiplexed, higher-order byte first on to 8 memory address lines)
2. the D register (either of the two bytes can be gated to D)
3. the increment/decrement circuit where it is increased or decreased by one and stored back in the selected 16-bit register.

The three paths, depending on the nature of the instruction, may operate independently or in various combinations in the same machine cycle.

Most instructions consist of two 8-clock-pulse machine cycles. The first cycle is the fetch cycle, and the second—and more if necessary—are execute cycles. During the fetch cycle the four bits in the P designator select one of the 16 registers R(P) as the current program counter. The selected register R(P) contains the address of the memory location from which the instruction is to be fetched. When the instruction is read out from the memory, the higher-order 4 bits of the instruction byte are loaded into the I register and the lower-order 4 bits into the N register. The content of the program counter is automatically incremented by one so that R(P) is now "pointing" to the next byte in the memory.

The X designator selects one of the 16 registers R(X) to "point" to the memory for an operand (or data) in certain ALU or I/O operations.

The N designator can perform the following five functions depending on the type of instruction fetched:

1. designate one of the 16 registers in R to be acted upon during register operations
2. indicate to the I/O devices a command code or device-selection code for peripherals
3. indicate the specific operation to be executed during the ALU instructions, types of tests to be performed during the Branch instructions, or the specific operation required in a class of miscellaneous instructions
4. indicate the value to be loaded into P to designate a new register to be used as the program counter R(P)
5. indicate the value to be loaded into X to designate a new register to be used as data pointer R(X).

The registers in R can be assigned by a programmer in three different ways as program counters, as data pointers, or as scratchpad locations (data registers) to hold two bytes of data.

Program Counters

Any register can be the main program counter; the address of the selected register is held in the P designator. Other registers in R can be used as subroutine program counters. By a single instruction the contents of the P register can be changed to effect a "call" to subroutine. When interrupts are being serviced, register R(1) is used as the program

counter for the user's interrupt servicing routine. After reset, and during a DMA operation, R(0) is used as the program counter. At all other times the register designated as program counter is at the discretion of the user.

Data Pointers

The registers in R may be used as data pointers to indicate a location in memory. The register designated by X (i.e., R(X)) points to memory for the following instructions (see Table I):

1. ALU operations
2. output instructions
3. input instructions
4. register — — memory transfer
5. interrupt and subroutine handling.

The register designated by N (i.e., R(N)) points to memory for the "load D from memory" instructions 0N and 4N and the "Store D" instruction 5N. The register designated by P (i.e., the program counter) is used as the data pointer for ALU instructions F8-FD, FF, 7C, 7D, 7F, and the RLDI instruction 68CN. During these instruction executions, the operation is referred to as "data immediate".

Another important use of R as a data pointer supports the built-in Direct-Memory-Access (DMA) function. When a DMA-In or DMA-Out request is received, one machine cycle is "stolen". This operation occurs at the end of the execute machine cycle in the current instruction. Register R(0) is always used as the data pointer during the DMA operation. The data is read from (DMA-Out) or written into (DMA-In) the memory location pointed to by the R(0) register. At the end of the transfer, R(0) is incremented by one so that the processor is ready to act upon the next DMA byte transfer request. This feature in the CDP1804AC architecture saves a substantial amount of logic when fast exchanges of blocks of data are required, such as with magnetic discs or during CRT-display-refresh cycles.

Data Registers

When registers in R are used to store bytes of data, instructions are provided which allow D to receive from or write into either the higher-order- or lower-order-byte portions of the register designated by N. By this mechanism (together with loading by data immediate) program pointer and data pointer designations are initialized. Also, this technique allows scratchpad registers in R to be used to hold general data. By employing increment or decrement instructions, such registers may be used as loop counters. The new RLDI, RLXA, RSXD, and RNX instructions also allow loading, storing, and exchanging the full 16-bit contents of the R registers. The new DBNZ instruction allows decrementing and branching-on-not-zero of any 16-bit R register without affecting the D register.

The Q Flip-Flop

An internal flip-flop, Q, can be set or reset by instruction and can be sensed by conditional branch instructions. It can also be driven by the output of the timer/counter. The output of Q is also available as a microprocessor output.

ARCHITECTURE (Cont'd)

Register Summary

D	8 Bits	Data Register (Accumulator)
DF	1 Bit	Data Flag (ALU Carry)
B	8 Bits	Auxiliary Holding Register
R	16 Bits	1 of 16 Scratchpad Registers
P	4 Bits	Designates which Register is Program Counter
X	4 Bits	Designates which Register is Data Pointer
N	4 Bits	Holds Low-Order Instr. Digit
I	4 Bits	Holds High-Order Instr. Digit
T	8 Bits	Holds old X, P after Interrupt (X is high nibble)
Q	1 Bit	Output Flip-Flop
CH	8 Bits	Holds Counter Jam Value
MIE	1 Bit	Master Interrupt Enable
CIE	1 Bit	Counter Interrupt Enable
XIE	1 Bit	External Interrupt Enable
CIL	1 Bit	Counter Interrupt Latch

Interrupt Servicing

Register R(1) is always used as the program counter whenever interrupt servicing is initialized. When an interrupt request occurs and the interrupt is allowed by the program (again, nothing takes place until the completion of the current instruction), the contents of the X and P registers are stored in the temporary register T, and X and P are set to new values; hex digit 2 in X and hex digit 1 in P. Master Interrupt Enable is automatically deactivated to inhibit further interrupts. The user's interrupt routine is now in control; the contents of T may be saved by means of a single SAV instruction (78) in the memory location pointed to by R(X) or the contents of T, D, and DF may be saved using a single DSAV instruction (6876). At the conclusion of the interrupt, the user's routine may restore the pre-interrupted value of X and P with either a RET instruction (70) which permits further interrupts, or a DIS instruction (71), which disables further interrupts.

Interrupt Generation and Arbitration
(See Fig. 5)

Interrupt requests can be generated from the following sources:

- Externally through the interrupt input (Request not latched)
- Internally due to timer/counter response (Request is latched)
 - On the transition from count (01)₁₆ to its next value (counter underflow)
 - On the \nearrow transition of $\overline{EF1}$ in pulse measurement mode 1
 - On the \nearrow transition of $\overline{EF2}$ in pulse measurement mode 2

For an interrupt to be serviced by the CPU, the appropriate Interrupt Enable flip-flops must be set. Thus, the External Interrupt Enable flip-flop must be set to service an external interrupt request, and the Counter Interrupt Enable flip-flop must be set to service an internal timer/counter interrupt request. In addition, the Master Interrupt Enable flip-flop (as used in the CDP1802) must be set to service either type of request. All 3 flip-flops are initially enabled with the application of a hardware reset, and, can be selectively enabled or disabled with software: CIE, CID instructions for the CIE flip-flop; XIE, XID instructions for the XIE flip-flop; RET, DIS instructions for the MIE flip-flop.

Short branch instructions on Counter Interrupt (BCI) and External Interrupt (BXI) can be placed in the user's interrupt service routine to provide a means of identifying and prioritizing the interrupt source. Note, however, that since the External Interrupt request is not latched, it must remain active until the short branch is executed if this priority arbitration scheme is used.

Interrupt requests can also be polled if automatic interrupt service is not desired (MIE=0). With the Counter Interrupt and External Interrupt short branch instructions, the branch will be taken if an interrupt request is pending, regardless of the state of any of the 3 Interrupt Enable flip-flops. The latched counter interrupt request signal will be reset when the branch is taken, when the CPU is reset, or with a LDC instruction with the Counter stopped.

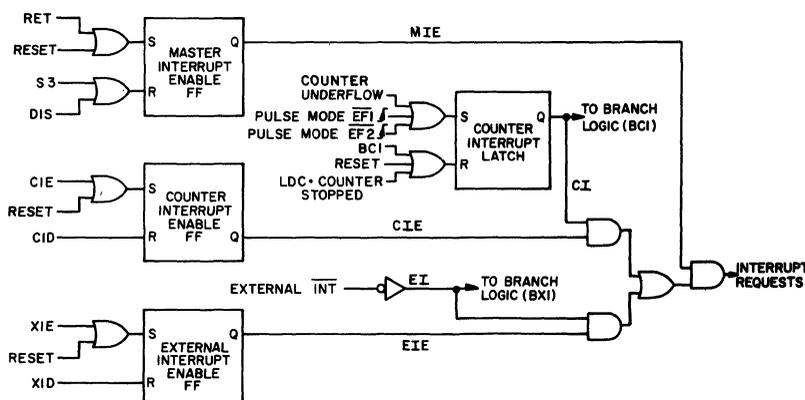


Fig. 5 - Interrupt logic-control diagram for CDP1804AC.

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ARCHITECTURE (Cont'd)

Timer/Counter and Controls (see Fig. 6)

This logic consists of a presettable 8-bit down-counter (Modulo N type), and a conditional divide-by-32 prescaler. After counting down to (01)₁₆ the counter returns to its initial value at the next count and sets the Counter Interrupt Latch. It will continue decrementing on subsequent counts. If the counter is preset to (00)₁₆ a full 256 counts will occur.

During a Load Counter instruction (LDC) if the counter was stopped with a STPC instruction, the counter and its holding register (CH) are loaded with the value in the D register and any previous counter interrupt is cleared. If the LDC is executed when the counter is running, the contents of the D register are loaded into the holding register (CH) only and any previous counter interrupt is not cleared. After counting down to (01)₁₆ the next count will load the new initial value into the counter, set the Counter Interrupt Latch, and operation will continue.

The timer/counter has the following five programmable modes:

1. Event Counter 1: Input to counter is connected to the EF1 terminal. The high-to-low transition decrements the counter.
2. Event Counter 2: Input to counter is connected to the EF2 terminal. The high-to-low transition decrements the counter.
3. Timer: Input to counter is from the divide-by-32 prescaler clocked by TPA. The prescaler is decremented on the low-to-high transition of TPA. The divide-by-32 prescaler is reset when the counter is in a mode other than the Timer mode or stopped by a STPC.
4. Pulse Duration Measurement 1: Input to counter connected to TPA. Each low-to-high transition of TPA

decrements the counter if the input signal at EF1 terminal (gate input) is low. On the transition of EF1 to the positive state, the count is stopped, the mode is cleared, and the interrupt request latched. If the counter underflows while the input is low, interrupt will also be set, but counting will continue.

5. Pulse Duration Measurement 2: Operation is identical to Pulse Duration Measurement 1, except EF2 is used as the gate input.

The modes can be changed without affecting the stored count.

Those modes which use EF1 and EF2 terminals as inputs do not exclude testing these flags for branch instructions.

The Stop Counter (STPC) instruction clears the counter mode and stops counting. The STPC instruction should be executed prior to a GEC instruction, if the counter is in the Event Counter Mode 1 or 2.

In addition to the five programmable modes, the Decrement Counter instruction (DTC) enables the user to count in software. In order to avoid conflict with counting done in the other modes, the instruction should be used only after the mode has been cleared by a Stop Counter instruction.

The Enable Toggle Q instruction (ETQ) connects the Q-line flip-flop to the output of the counter, such that each time the counter decrements from 01 to its next value, the Q output changes state. This action is independent of the counter mode and the Interrupt Enable flip-flops. The Enable Toggle Q condition is cleared by an LDC with the timer/counter stopped; system Reset, or a BCI with CI=1.

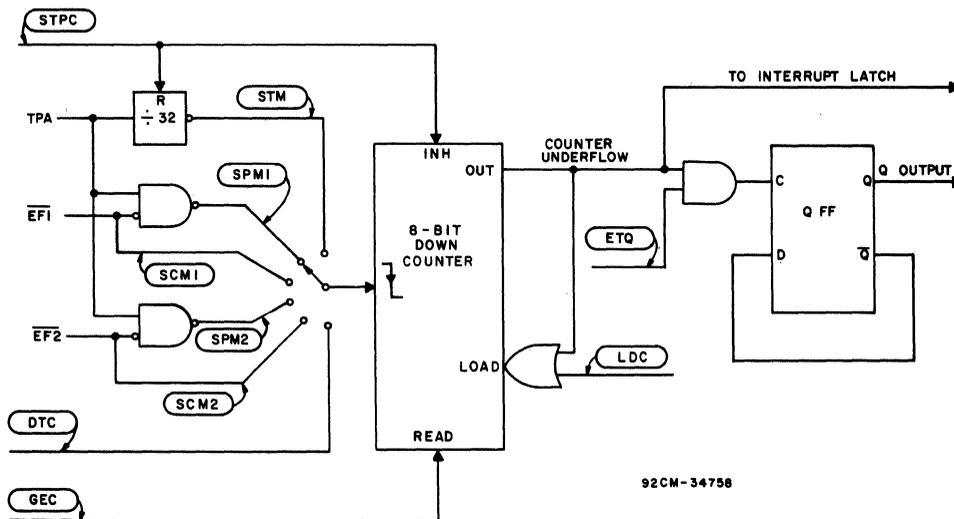


Fig. 6 - Timer/Counter diagram for CDP1804AC.

ARCHITECTURE (Cont'd)

On-Board Clock (see Fig. 7 and 8)

Clock circuits may use either an external crystal or an RC network.

The crystal is connected between terminals 1 and 39 (CLOCK and XTAL) in parallel with a resistance (1 megohm typ.).

Frequency trimming capacitors may be required at terminals 1 and 39. For additional information on crystal oscillators, see ICAN-6565. Because of the Schmitt Trigger input, an RC oscillator can be used as shown in Fig. 7. The frequency is approximately $1/RC$ (see Fig. 8).

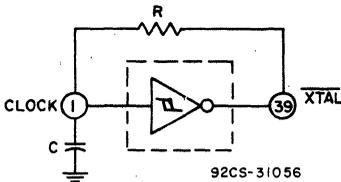


Fig. 7 - RC network for oscillator.

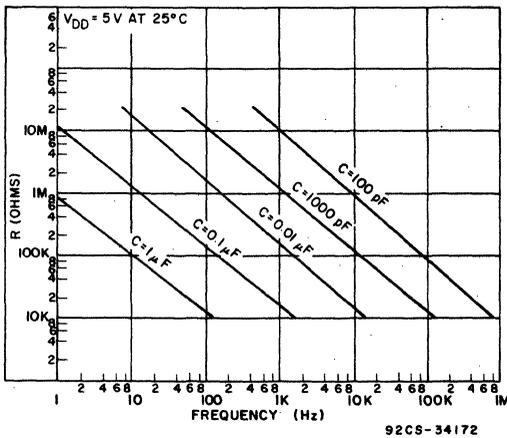


Fig. 8 - Nominal component values as a function of frequency for the RC oscillator.

CONTROL MODES

CLEAR	WAIT	MODE
L	L	RUN (ROM/RAM)
L	H	RESET
H	L	PAUSE
H	H	RUN (RAM ONLY)

The function of the modes are defined as follows:

RESET

Registers I, N, Q, counter prescaler, and Counter Interrupt Latch are reset. XIE and CIE are set and 0's (V_{SS}) are placed on the data bus. TPA and TPB are suppressed while reset is held and the CPU is placed in S1. The state of the timer/counter is unaffected by the RESET operation.

The first machine cycle after termination of reset is an initialization cycle which requires 9 clock pulses. During this cycle the CPU remains in S1, X, P-T, and then registers X, P, R(0) are reset, and MIE is set. Interrupt and DMA servicing suppressed during the initialization cycle. The next cycle is an S0 or an S2 but never an S1 or S3. The use of a 71 instruction followed by 00 at memory locations 0000 and 0001, may be used to reset MIE, so as to preclude interrupts until ready for them. Power-up reset/run (ROM/RAM) can be realized by connecting an RC network to WAIT (See Fig. 9).

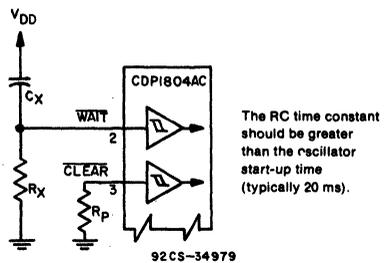


Fig. 9 - Reset/Run (ROM/RAM) diagram.

The RC time constant should be greater than the oscillator start-up time (typically 20 ms).

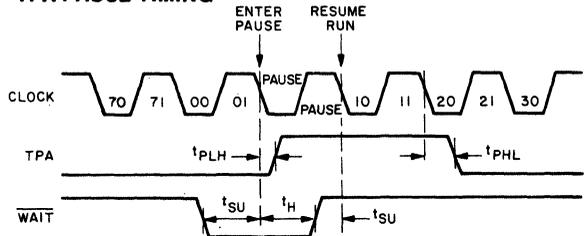
PAUSE

Stops the internal CPU timing generator, freezing the state of the processor. Pause can occur at two points in a machine cycle, on the low-to-high transition of either TPA or TPB.

The oscillator continues to run but subsequent clock transitions are ignored. TPA and TPB remain at their previous state (see Fig. 10).

If Pause is entered while in the event counter mode, the appropriate Flag transitions will continue to decrement the counter.

TPA PAUSE TIMING



INSTRUCTION SET

The CDP1804AC instruction summary is given in Table I. Hexadecimal notation is used to refer to the 4-bit binary codes.

In all registers bits are numbered from the least significant bit (LSB) to the most significant bit (MSB) starting with 0.

R(W): Register designated by W, where
W=N or X, or P

R(W).0: Lower-order byte of R(W)
R(W).1: Higher-order byte of R(W)

Operation Notation

$M(R(N)) \rightarrow D; R(N) + 1 \rightarrow R(N)$

This notation means: The memory byte pointed to by R(N) is loaded into D, and R(N) is incremented by 1.

TABLE I — INSTRUCTION SUMMARY (For Notes, see also page 17)

INSTRUCTION	NO. OF MACHINE CYCLES	MNEMONIC	OP CODE	OPERATION
MEMORY REFERENCE				
LOAD IMMEDIATE	2	LDI	F8	$M(R(P)) \rightarrow D; R(P)+1 \rightarrow R(P)$
REGISTER LOAD IMMEDIATE	5	RLDI	68CN [■]	$M(R(P)) \rightarrow R(N).1; M(R(P))+1 \rightarrow R(N).0; R(P)+2 \rightarrow R(P)$
LOAD VIA N	2	LDN	0N	$M(R(N)) \rightarrow D; \text{FOR } N \text{ NOT } 0$
LOAD ADVANCE	2	LDA	4N	$M(R(N)) \rightarrow D; R(N)+1 \rightarrow R(N)$
LOAD VIA X	2	LDX	F0	$M(R(X)) \rightarrow D$
LOAD VIA X AND ADVANCE	2	LDXA	72	$M(R(X)) \rightarrow D; R(X)+1 \rightarrow R(X)$
REGISTER LOAD VIA X AND ADVANCE	5	RLXA	686N [■]	$M(R(X)) \rightarrow R(N).1; M(R(X))+1 \rightarrow R(N).0; R(X)+2 \rightarrow R(X)$
STORE VIA N	2	STR	5N	$D \rightarrow M(RN))$
STORE VIA X AND DECREMENT	2	STXD	73	$D \rightarrow M(R(X)); R(X)-1 \rightarrow R(X)$
REGISTER STORE VIA X AND DECREMENT	5	RSXD	68AN [■]	$R(N).0 \rightarrow M(R(X)); R(N).1 \rightarrow M(R(X)-1); R(X)-2 \rightarrow R(X)$
REGISTER OPERATIONS				
INCREMENT REG N	2	INC	1N	$R(N)+1 \rightarrow R(N)$
DECREMENT REG N	2	DEC	2N	$R(N)-1 \rightarrow R(N)$
DECREMENT REG N AND LONG BRANCH IF NOT EQUAL 0	5	DBNZ	682N	$R(N)-1 \rightarrow R(N); \text{IF } R(N) \text{ NOT } 0, M(R(P)) \rightarrow R(P).1, M(R(P))+1 \rightarrow R(P).0, \text{ELSE } R(P)+2 \rightarrow R(P)$
INCREMENT REG X	2	IRX	60	$R(X)+1 \rightarrow R(X)$
GET LOW REG N	2	GLO	8N	$R(N).0 \rightarrow D$
PUT LOW REG N	2	PLO	AN	$D \rightarrow R(N).0$
GET HIGH REG N	2	GHI	9N	$R(N).1 \rightarrow D$
PUT HIGH REG N	2	PHI	BN	$D \rightarrow R(N).1$
REGISTER N TO REGISTER X COPY	4	RNX	68BN [■]	$R(N) \rightarrow R(X)$
LOGIC OPERATIONS (Note 5)				
OR	2	OR	F1	$M(R(X)) \text{ OR } D \rightarrow D$
OR IMMEDIATE	2	ORI	F9	$M(R(P)) \text{ OR } D \rightarrow D; R(P)+1 \rightarrow R(P)$
EXCLUSIVE OR	2	XOR	F3	$M(R(X)) \text{ XOR } D \rightarrow D$
EXCLUSIVE OR IMMEDIATE	2	XRI	FB	$M(R(P)) \text{ XOR } D \rightarrow D; R(P)+1 \rightarrow R(P)$
AND	2	AND	F2	$M(R(X)) \text{ AND } D \rightarrow D$
AND IMMEDIATE	2	ANI	FA	$M(R(P)) \text{ AND } D \rightarrow D; R(P)+1 \rightarrow R(P)$
SHIFT RIGHT	2	SHR	F6	SHIFT D RIGHT, $LSB(D) \rightarrow DF, 0 \rightarrow MSB(D)$
SHIFT RIGHT WITH CARRY	2	SHRC	76 [▲]	SHIFT D RIGHT, $LSB(D) \rightarrow DF, DF \rightarrow MSB(D)$
RING SHIFT RIGHT	2	RSHR		
SHIFT LEFT	2	SHL	FE	SHIFT D LEFT, $MSB(D) \rightarrow DF, 0 \rightarrow LSB(D)$

[■]Previous contents of T register are destroyed during instruction execution.

[▲]This instruction is associated with more than one mnemonic. Each mnemonic is individually listed.

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Table I — INSTRUCTION SUMMARY (Cont'd)

INSTRUCTION	NO. OF MACHINE CYCLES	MNEMONIC	OP CODE	OPERATION
LOGIC OPERATIONS (Note 5) (Cont'd)				
SHIFT LEFT WITH CARRY	2	SHLC	7EA	SHIFT D LEFT, MSB(D)→DF, DF→LSB(D)
RING SHIFT LEFT	2	RSHL		
ARITHMETIC OPERATIONS (Note 5)				
ADD	2	ADD	F4	M(R(X))+D→DF, D
DECIMAL ADD	4	DADD	68F4	M(R(X))+D→DF, D DECIMAL ADJUST→DF, D
ADD IMMEDIATE	2	ADI	FC	M(R(P))+D→DF, D; R(P)+1→R(P)
DECIMAL ADD IMMEDIATE	4	DADI	68FC	M(R(P))+D→DF, D R(P)+1→R(P) DECIMAL ADJUST→DF, D
ADD WITH CARRY	2	ADC	74	M(R(X))+D+DF→DF, D
DECIMAL ADD WITH CARRY	4	DADC	6874	M(R(X))+D+DF→DF, D DECIMAL ADJUST→DF, D
ADD WITH CARRY, IMMEDIATE	2	ADCI	7C	M(R(P))+D+DF→DF, D R(P)+1→R(P)
DECIMAL ADD WITH CARRY, IMMEDIATE	4	DACI	687C	M(R(P))+D+DF→DF, D R(P)+1→R(P) DECIMAL ADJUST→DF, D
SUBTRACT D	2	SD	F5	M(R(X))-D→DF, D
SUBTRACT D IMMEDIATE	2	SDI	FD	M(R(P))-D→DF, D; R(P)+1→R(P)
SUBTRACT D WITH BORROW	2	SDB	75	M(R(X))-D-(NOT DF)→DF, D
SUBTRACT D WITH BORROW, IMMEDIATE	2	SDBI	7D	M(R(P))-D-(NOT DF)→DF, D; R(P)+1→R(P)
SUBTRACT MEMORY	2	SM	F7	D-M(R(X))→DF, D
DECIMAL SUBTRACT MEMORY	4	DSM	68F7	D-M(R(X))→DF, D DECIMAL ADJUST→DF, D
SUBTRACT MEMORY IMMEDIATE	2	SMI	FF	D-M(R(P))→DF, D; R(P)+1→R(P)
DECIMAL SUBTRACT MEMORY, IMMEDIATE	4	DSMI	68FF	D-M(R(P))→DF, D R(P)+1→R(P) DECIMAL ADJUST→DF, D
SUBTRACT MEMORY WITH BORROW	2	SMB	77	D-M(R(X))-(NOT DF)→DF, D
DECIMAL SUBTRACT MEMORY WITH BORROW	4	DSMB	6877	D-M(R(X))-(NOT DF)→DF, D DECIMAL ADJUST→DF, D
SUBTRACT MEMORY WITH BORROW, IMMEDIATE	2	SMBI	7F	D-M(R(P))-(NOT DF)→DF, D R(P)+1→R(P)
DECIMAL SUBTRACT MEMORY WITH BORROW, IMMEDIATE	4	DSBI	687F	D-M(R(P))-(NOT DF)→DF, D R(P)+1→R(P) DECIMAL ADJUST→DF, D
BRANCH INSTRUCTIONS — SHORT BRANCH				
SHORT BRANCH	2	BR	30	M(R(P))→R(P).0
NO SHORT BRANCH (SEE SKP)	2	NBR	38 [▲]	R(P)+1→R(P)
SHORT BRANCH IF D = 0	2	BZ	32	IF D = 0, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH IF D NOT 0	2	BNZ	3A	IF D NOT 0, M(R(P))→R(P).0 ELSE R(P)+1→R(P)

▲This instruction is associated with more than one mnemonic. Each mnemonic is individually listed.

Table I — INSTRUCTION SUMMARY (Cont'd)

INSTRUCTION	NO. OF MACHINE CYCLES	MNEMONIC	OP CODE	OPERATION
BRANCH INSTRUCTIONS — SHORT BRANCH (Cont'd)				
SHORT BRANCH IF DF = 1	2	BDF	33 ^A	IF DF = 1, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH IF POS OR ZERO	2	BPZ		
SHORT BRANCH IF EQUAL OR GREATER	2	BGE		
SHORT BRANCH IF DF = 0	2	BNF	3B ^A	IF D = 0, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH IF MINUS	2	BM		
SHORT BRANCH IF LESS	2	BL		
SHORT BRANCH IF Q = 1	2	BQ	31	IF Q = 1, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH IF Q = 0	2	BNQ	39	IF Q = 0, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH IF EF1 = 1 (EF1 = V _{SS})	2	B1	34	IF EF1 = 1, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH IF EF1 = 0 (EF1 = V _{DD})	2	BN1	3C	IF EF1 = 0, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH IF EF2 = 1 (EF2 = V _{SS})	2	B2	35	IF EF2 = 1, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH IF EF2 = 0 (EF2 = V _{DD})	2	BN2	3D	IF EF2 = 0, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH IF EF3 = 1 EF3 = V _{SS})	2	B3	36	IF EF3 = 1, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH IF EF3 = 0 EF3 = V _{DD})	2	BN3	3E	IF EF3 = 0, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH IF EF4 = 1 EF4 = V _{SS})	2	B4	37	IF EF4 = 1, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH IF EF4 = 0 (EF4 = V _{DD})	2	BN4	3F	IF EF4 = 0, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH ON COUNTER INTERRUPT	3	BCI	683E*	IF CI = 1, M(R(P))→R(P).0; 0→CI ELSE R(P)+1→R(P)
SHORT BRANCH ON EXTERNAL INTERRUPT	3	BXI	683F	IF XI = 1, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
BRANCH INSTRUCTIONS — LONG BRANCH				
LONG BRANCH	3	LBR	C0	M(R(P))→R(P).1, M(R(P)+1)→R(P).0
NO LONG BRANCH (SEE LSKP)	3	NLBR	C8 ^A	R(P)+2→R(P)
LONG BRANCH IF D = 0	3	LBZ	C2	IF D = 0, M(R(P))→R(P).1 M(R(P)+1)→R(P).0 ELSE R(P)+2→R(P)
LONG BRANCH IF D NOT 0	3	LBNZ	CA	IF D NOT 0, M(R(P))→R(P).1 M(R(P)+1)→R(P).0 ELSE R(P)+2→R(P)
LONG BRANCH IF DF = 1	3	LBDF	C3	IF DF = 1, M(R(P))→R(P).1 M(R(P)+1)→R(P).0 ELSE R(P)+2→R(P)
LONG BRANCH IF DF = 0	3	LBNF	CB	IF DF = 0, M(R(P))→R(P).1 M(R(P)+1)→R(P).0 ELSE R(P)+2→R(P)
LONG BRANCH IF Q = 1	3	LBQ	C1	IF Q = 1, M(R(P))→R(P).1 M(R(P)+1)→R(P).0 ELSE R(P)+2→R(P)
LONG BRANCH IF Q = 0	3	LBNQ	C9	IF Q = 0, M(R(P))→R(P).1 M(R(P)+1)→R(P).0 ELSE R(P)+2→R(P)

^AThis instruction is associated with more than one mnemonic. Each mnemonic is individually listed.
*ETQ cleared by LDC, reset of CPU, or BCI (CI = 1). CI = Counter Interrupt, XI = External Interrupt.

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Table I — INSTRUCTION SUMMARY (Cont'd)

INSTRUCTION	NO. OF MACHINE CYCLES	MNEMONIC	OP CODE	OPERATION
SKIP INSTRUCTIONS				
SHORT SKIP (SEE NBR)	2	SKP	38 [▲]	R(P)+1→R(P)
LONG SKIP (SEE NLBR)	3	LSKP	C8 [▲]	R(P)→R(P)
LONG SKIP IF D = 0	3	LSZ	CE	IF D = 0, R(P)+2→R(P) ELSE CONTINUE
LONG SKIP IF D NOT 0	3	LSNZ	C6	IF D NOT 0, R(P)+2→R(P) ELSE CONTINUE
LONG SKIP IF DF = 1	3	LSDF	CF	IF DF = 1, R(P)+2→R(P) ELSE CONTINUE
LONG SKIP IF DF = 0	3	LSNF	C7	IF DF = 0, R(P)+2→R(P) ELSE CONTINUE
LONG SKIP IF Q = 1	3	LSQ	CD	IF Q = 1, R(P)+2→R(P) ELSE CONTINUE
LONG SKIP IF Q = 0	3	LSNQ	C5	IF Q = 0, R(P)+2→R(P) ELSE CONTINUE
LONG SKIP IF IE = 1	3	LSIE	CC	IF IE = 1, R(P)+2→R(P) ELSE CONTINUE
CONTROL INSTRUCTIONS				
IDLE	2	IDL	00 [#]	STOP ON TPB; WAIT FOR DMA OR INTERRUPT; BUS FLOATS
NO OPERATION	3	NOP	C4	CONTINUE
SET P	2	SEP	DN	N→P
SET X	2	SEX	EN	N→X
SET Q	2	SEQ	7B	1→Q
RESET Q	2	REQ	7A	0→Q
PUSH X, P TO STACK	2	MARK	79	(X, P)→T; (X, P)→M(R(2)) THEN P→X; R(2)→1→R(2)
TIMER/COUNTER INSTRUCTIONS				
LOAD COUNTER	3	LDC	6806 [*]	D→COUNTER; 0→CI; (IF COUNTER IS STOPPED)
GET COUNTER	3	GEC	6808	COUNTER→D
STOP COUNTER	3	STPC	6800	STOP COUNTER CLOCK; 0→32 PRESCALER
DECREMENT TIMER/COUNTER	3	DTC	6801	COUNTER-1→COUNTER
SET TIMER MODE AND START	3	STM	6807	TPA÷32→COUNTER CLOCK
SET COUNTER MODE 1 AND START	3	SCM1	6805	EF1→COUNTER CLOCK
SET COUNTER MODE 2 AND START	3	SCM2	6803	EF2→COUNTER CLOCK
SET PULSE WIDTH MODE 1 AND START	3	SPM1	6804	TPA.EF1→COUNTER CLOCK; EF1 ✗ STOPS COUNT
SET PULSE WIDTH MODE 2 AND START	3	SPM2	6802	TPA.EF2→COUNTER CLOCK; EF2 ✗ STOPS COUNT
ENABLE TOGGLE Q	3	ETQ	6809 [*]	IF COUNTER = 01 · NEXT COUNTER CLOCK ✗ : Q→Q

[▲]This instruction is associated with more than one mnemonic. Each mnemonic is individually listed.

[#]An IDLE instruction initiates an S1 cycle. All external signals, except the oscillator, are stopped on the low-to-high transition of TPB. All outputs remain in their previous states, MRD is set to a logic '1' and the data bus floats. The processor will continue to IDLE until an I/O request (INTERRUPT, DMA-IN, or DMA-OUT) is activated. When the request is acknowledged, the IDLE cycle is terminated and the I/O request is serviced, and then normal operation is resumed. (To respond to an INTERRUPT during an IDLE, MIE must be enabled.)

^{*}ETQ cleared by LDC, reset of CPU or BCI (CI = 1).

CI = Counter Interrupt, XI = External Interrupt.

Table I — INSTRUCTION SUMMARY (Cont'd)

INSTRUCTION	NO. OF MACHINE CYCLES	MNEMONIC	OP CODE	OPERATION
INTERRUPT CONTROL				
EXTERNAL INTERRUPT ENABLE	3	XIE	680A	1→XIE
EXTERNAL INTERRUPT DISABLE	3	XID	680B	0→XIE
COUNTER INTERRUPT ENABLE	3	CIE	680C	1→CIE
COUNTER INTERRUPT DISABLE	3	CID	680D	0→CIE
RETURN	2	RET	70	M(R(X))→X, P; R(X)+1→R(X); 1→MIE
DISABLE	2	DIS	71	M(R(X))→X, P; R(X)+1→R(X); 0→MIE
SAVE	2	SAV	78	T→M(R(X))
SAVE T, D, DF	6	DSAV	6876 [■]	R(X)-1→R(X), T→M(R(X)), R(X)-1→R(X), D→M(R(X)), R(X)-1→R(X), SHIFT D RIGHT WITH CARRY, D→M(R(X))
INPUT-OUTPUT BYTE TRANSFER				
OUTPUT 1	2	OUT 1	61	M(R(X))→BUS; R(X)+1→R(X); N LINES = 1
OUTPUT 2	2	OUT 2	62	M(R(X))→BUS; R(X)+1→R(X); N LINES = 2
OUTPUT 3	2	OUT 3	63	M(R(X))→BUS; R(X)+1→R(X); N LINES = 3
OUTPUT 4	2	OUT 4	64	M(R(X))→BUS; R(X)+1→R(X); N LINES = 4
OUTPUT 5	2	OUT 5	65	M(R(X))→BUS; R(X)+1→R(X); N LINES = 5
OUTPUT 6	2	OUT 6	66	M(R(X))→BUS; R(X)+1→R(X); N LINES = 6
OUTPUT 7	2	OUT 7	67	M(R(X))→BUS; R(X)+1→R(X); N LINES = 7
INPUT 1	2	INP 1	69	BUS→M(R(X)); BUS→D; N LINES = 1
INPUT 2	2	INP 2	6A	BUS→M(R(X)); BUS→D; N LINES = 2
INPUT 3	2	INP 3	6B	BUS→M(R(X)); BUS→D; N LINES = 3
INPUT 4	2	INP 4	6C	BUS→M(R(X)); BUS→D; N LINES = 4
INPUT 5	2	INP 5	6D	BUS→M(R(X)); BUS→D; N LINES = 5
INPUT 6	2	INP 6	6E	BUS→M(R(X)); BUS→D; N LINES = 6
INPUT 7	2	INP 7	6F	BUS→M(R(X)); BUS→D; N LINES = 7
CALL AND RETURN				
STANDARD CALL	10	SCAL	688N [■]	R(N).0→M(R(X)); R(N).1→M(R(X)-1); R(X)-2→R(X); R(P)→R(N); THEN M(R(N))→R(P).1; M(R(N)+1)→R(P).0; R(N)+2→R(N)
STANDARD RETURN	8	SRET	689N [■]	R(N)→R(P); M(R(X)+1)→R(N).1; M(R(X)+2)→R(N).0; R(X)+2→R(X)

[■] Previous contents of T register are destroyed during instruction execution.

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NOTES FOR TABLE I

1. Long-Branch, Long-Skip and No Op instructions require three cycles to complete (1 fetch + 2 execute).

Long-Branch instructions are three bytes long. The first byte specifies the condition to be tested; and the second and third byte, the branching address.

The long-branch instructions can:

- a. Branch unconditionally
- b. Test for D=0 or D≠0
- c. Test for DF=0 or DF=1
- d. Test for Q=0 or Q=1
- e. Effect an unconditional no branch

If the tested condition is met, then branching takes place; the branching address bytes are loaded in the high-and-low-order bytes of the current program counter, respectively. This operation effects a branch to any memory location.

If the tested condition is not met, the branching address bytes are skipped over, and the next instruction in sequence is fetched and executed. This operation is taken for the case of unconditional no branch (NLBR).

2. The short-branch instructions are two or three bytes long. The first byte specifies the condition to be tested, and the second specifies the branching address, except for the branches on interrupt. For those, the first two bytes specify the condition to be tested and the third byte specifies the branching address.

The short branch instruction can:

- a. Branch unconditionally
- b. Test for D=0 or D≠0
- c. Test for DF=0 or DF=1
- d. Test for Q=0 or Q=1
- e. Test the status (1 or 0) of the four EF flags
- f. Effect an unconditional no branch
- g. Test for counter or external interrupts (BCI, BXI)

If the tested condition is met, then branching takes place; the branching address byte is loaded into the low-order byte position of the current program counter. This effects a branch within the current 256-byte page of the memory, i.e., the page which holds the branching address. If the tested condition is not met, the branching address byte is skipped over, and the next instruction in sequence is fetched and executed. This same action is taken in the case of unconditional no branch (NBR).

3. The skip instructions are one byte long. There is one Unconditional Short-Skip (SKP) and eight Long-Skip instructions.

The Unconditional Short-Skip instruction takes 2 cycles to complete (1 fetch + 1 execute). Its action is to skip over the byte following it. Then the next instruction in sequence is fetched and executed. This SKP instruction is identical to the unconditional no-branch instruction (NBR) except that the skipped-over byte is not considered part of the program.

The Long-Skip instructions take three cycles to complete (1 fetch + 2 execute).

They can:

- a. Skip unconditionally
- b. Test for D=0 or D≠0
- c. Test for DF=0 or DF=1
- d. Test for Q=0 or Q=1
- e. Test for MIE=1

If the tested condition is met, then Long Skip takes place; the current program counter is incremented twice. Thus two bytes are skipped over and the next instruction in sequence is fetched and executed. If the tested condition is not met, then no action is taken. Execution is continued by fetching the next instruction in sequence.

4. Instruction 6800 through 68FF take a minimum of 3 machine cycles and up to a maximum of 10 machine cycles. In all cases, the first two cycles are fetches and subsequent cycles are executes. The first byte (68) of these two-byte op codes is used to generate the second fetch, the second byte is then interpreted differently than the same code without the 68 prefix. DMA and INT requests are not serviced until the end of the last execute cycle.

5. Arithmetic Operations:

The arithmetic and shift operations are the only instructions that can alter the content of DF. The syntax '(NOT DF)' denotes the subtraction of the borrow.

Binary Operations:

After an ADD instruction —

DF=1 denotes a carry has occurred. Result is greater than FF₁₆.

DF=0 denotes a carry has not occurred.

After a SUBTRACT instruction —

DF=1 denotes no borrow. D is a true positive number.

DF=0 denotes a borrow. D is in two's complement form.

Binary Coded Decimal Operations:

After a BCD ADD instruction —

DF=1 denotes a carry has occurred. Result is greater than 99₁₀.

DF=0 denotes a carry has not occurred.

After a BCD SUBTRACT instruction —

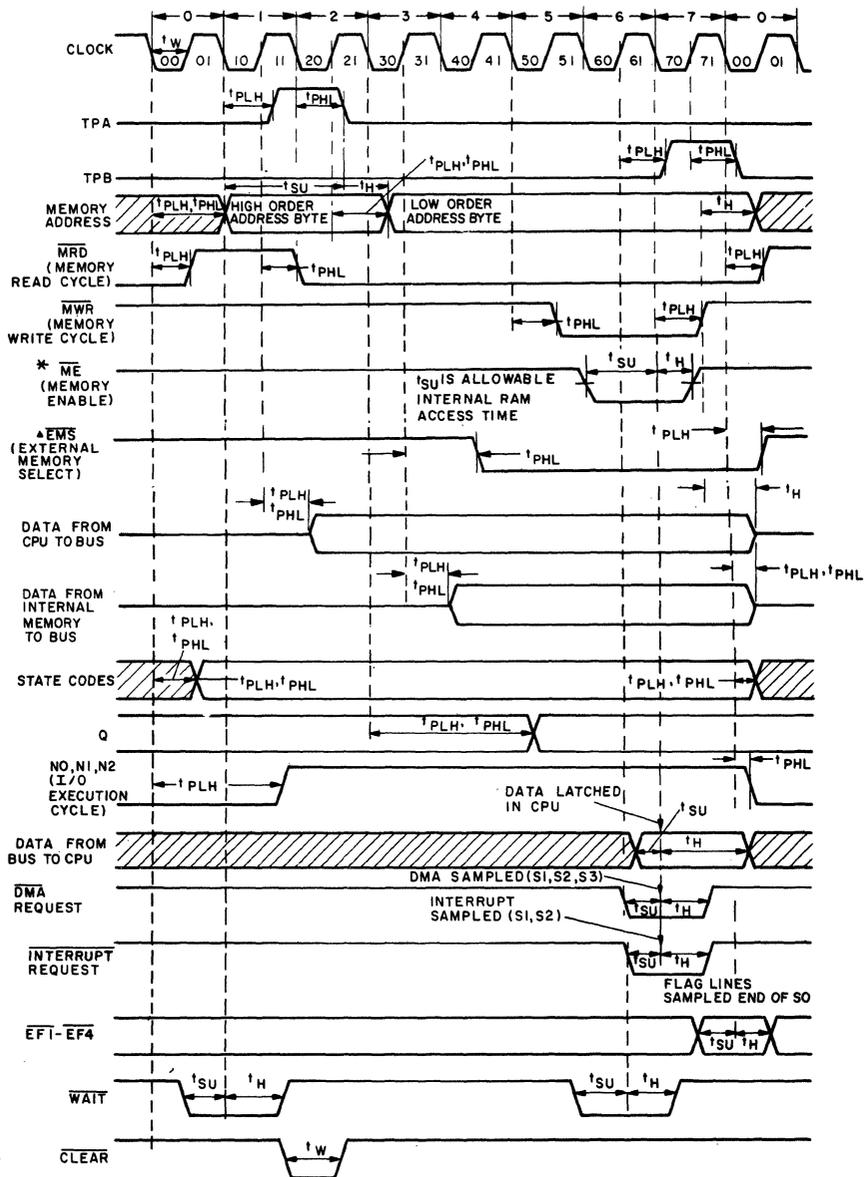
DF=1 denotes no borrow. D is a true positive decimal number.

(Example)	99	D	
	-88	M(R(X))	
	11	D	DF=1

DF=0 denotes a borrow. D is in ten's complement form.

(Example)	88	D	
	-99	M(R(X))	
	89	D	DF=0

89 is the ten's complement of 11, which is the correct answer (with a minus value denoted by DF=0).



- * NOTES:**
1. THIS TIMING DIAGRAM IS USED TO SHOW SIGNAL RELATIONSHIPS ONLY AND DOES NOT REPRESENT ANY SPECIFIC MACHINE CYCLE.
 2. ALL MEASUREMENTS ARE REFERENCED TO 50% POINT OF THE WAVEFORMS.
 3. SHADED ARE AS INDICATED "DON'T CARE" OR UNDEFINED STATE. MULTIPLE TRANSITIONS MAY OCCUR DURING THIS PERIOD.
- 92CL-34986
- * FOR THE RUN (RAM ONLY) MODE ONLY.
 - ^ FOR THE RUN (RAM/ROM) MODE ONLY.

Fig. 12 - Objective dynamic timing waveforms for CDP1804AC.

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DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $C_L = 50$ pF, $V_{DD} = 5$ V, $\pm 5\%$.

CHARACTERISTIC	LIMITS		UNITS	
	CDP1804AC			
	Typ.*	Max.		
Propagation Delay Times:				
Clock to TPA, TPB	t_{PLH}, t_{PHL}	150	275	ns
Clock-to-Memory High-Address Byte	t_{PLH}, t_{PHL}	325	550	
Clock-to-Memory Low-Address Byte	t_{PLH}, t_{PHL}	275	450	
Clock to $\overline{\text{MRD}}$	t_{PLH}, t_{PHL}	200	325	
Clock to $\overline{\text{MWR}}$	t_{PLH}, t_{PHL}	150	275	
Clock to (CPU DATA to BUS)	t_{PLH}, t_{PHL}	375	625	
Clock to State Code	t_{PLH}, t_{PHL}	225	400	
Clock to Q	t_{PLH}, t_{PHL}	250	425	
Clock to N	t_{PLH}, t_{PHL}	250	425	
Clock to Internal RAM Data to BUS	t_{PLH}, t_{PHL}	420	650	
Clock to $\overline{\text{EMS}}$	t_{PLH}, t_{PHL}	275	450	
Minimum Set Up and Hold Times:■				
Data Bus Input Set-Up	t_{SU}	-100	0	ns
Data Bus Input Hold	t_H	125	225	
DMA Set-Up	t_{SU}	-75	0	
DMA Hold	t_H	100	175	
$\overline{\text{ME}}$ Set-Up	t_{SU}	-25	0	
$\overline{\text{ME}}$ Hold	t_H	90	150	
Interrupt Set-Up	t_{SU}	-100	0	
Interrupt Hold	t_H	100	175	
WAIT Set-Up	t_{SU}	20	50	
$\overline{\text{EF1-4}}$ Set-Up	t_{SU}	-125	0	
$\overline{\text{EF1-4}}$ Hold	t_H	175	300	
Minimum Pulse Width Times:■				
$\overline{\text{CLEAR}}$ Pulse Width	t_{WL}	100	175	ns
CLOCK Pulse Width	t_{WL}	75	125	

*Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .

■Maximum limits of minimum characteristics are the values above which all devices function.

TIMING SPECIFICATIONS as a function of T ($T = 1/f_{\text{Clock}}$) at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = 5$ V, $\pm 5\%$.

CHARACTERISTIC	LIMITS		UNITS	
	CDP1804AC			
	Min.	Typ.*		
High-Order Memory-Address Byte Set-Up to TPA Time	T_{SU}	2T-275	2T-175	ns
High-Order Memory-Address Byte Hold after TPA Time	t_H	T/2-50	T/2-15	
Low-Order Memory-Address Byte Hold after WR Time	t_H	T+0	T+100	
CPU Data to Bus Hold after WR Time	t_H	T-200	T-100	
Required Memory Access Time Address to Data	t_{ACC}	4.5T-400	4.5T-175	

*Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .

TABLE II. CONDITIONS ON DATA BUS AND MEMORY ADDRESS LINES DURING ALL MACHINE STATES

STATE	I	N	MNEMONIC	OPERATION	DATA BUS	MEMORY ADDRESS	MRD	MWR	N LINES	
S1	RESET			0→Q,I,N, COUNTER PRESCALER, CIL; 1→CIE, XIE	00	UNDEFINED	1	1	0	
	INITIALIZE NOT PROGRAMMER ACCESSIBLE			X, P→T THEN 0→X, P; 1→MIE, 0000→R0	00A	UNDEFINED	1	1	0	
S0	FETCH			MRP→1, N; RP+1→RP	MRP	RP	0	1	0	
S1	0	0	IDL	STOP AT TPB WAIT FOR DMA OR INT	FLOAT	RO	1	1	0	
	0	1-F	LDN	MRN→D	MRN	RN	0	1	0	
	1	0-F	INC	RN+1→RN	FLOAT	RN	1	1	0	
	2	0-F	DEC	RN-1→RN	FLOAT	RN	1	1	0	
	3	0-F	SHORT BRANCH	TAKEN: MRP→RP.0 NOT TAKEN: RP+1→RP	MRP	RP	0	1	0	
	4	0-F	LDA	MRN→D; RN+1→RN	MRN	RN	0	1	0	
	5	0-F	STR	D→MRN	D	RN	1	0	0	
	6	0	IRX	RX+1→RX	MRX	RX	1	1	0	
	6	1	2	OUT 1	MRX→BUS; RX+1→RX	MRX	RX	0	1	1
		2	3	OUT 2						2
		3	4	OUT 3						3
		4	5	OUT 4						4
		5	6	OUT 5						5
		6	7	OUT 6						6
		7	7	OUT 7						7
	S1	9	A	INP 1	BUS→MRX, D	DATA FROM I/O DEVICE	RX	1	0	1
		A	B	INP 2						2
B		C	INP 3	3						
C		D	INP 4	4						
D		E	INP 5	5						
E		F	INP 6	6						
F		F	INP 7	7						
7	0		RET	MRX→X,P; RX+1→RX 1→MIE	MRX	RX	0	1	0	
	1		DIS	MRX→X,P; RX+1→RX 0→MIE	MRX	RX	0	1	0	
	2		LDXA	MRX→D; RX+1→RX	MRX	RX	0	1	0	
	3		STXD	D→MRX; RX-1→RX	D	RX	1	0	0	
	4		ADC	MRX+D+DF→DF, D	MRX	RX	0	1	0	
	5		SDB	MRX→D→DFN→DF, D	MRX	RX	0	1	0	
	6		SHRC	LSB(D)→DF; DF→MSB(D)	FLOAT	RX	1	1	0	
	7		SMB	D→MRX→DFN→DF, D	MRX	RX	0	1	0	
	8		SAV	T→MRX	T	RX	1	0	0	
	9		MARK	X,P→T, MR2; P→X R2-1→R2	T	R2	1	0	0	
	A		REQ	0→Q	FLOAT	RP	1	1	0	
	B		SEQ	1→Q	FLOAT	RP	1	1	0	
	C		ADCI	MRP+D+DF→DF, D; RP+1	MRP	RP	0	1	0	
	D		SDBI	MRP→D→DFN→DF, D; RP+1	MRP	RP	0	1	0	
	E		SHLC	MSB(D)→DF; DF→LSB(D)	FLOAT	RP	1	1	0	
	F		SMBI	D→MRP→DFN→DF, D; RP+1	MRP	RP	0	1	0	
	8	0-F	GLO	RN.0→D	RN.0	RN	1	1	0	
9	0-F	GHI	RN.1→D	RN.1	RN	1	1	0		
A	0-F	PLO	D→RN.0	D	RN	1	1	0		
B	0-F	PHI	D→RN.1	D	RN	1	1	0		

▲ = Data bus floats for first 2-1/2 clocks of the 9 clock initialization cycle; all zeros for remainder of cycle.

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TABLE II. CONDITIONS ON DATA BUS AND MEMORY ADDRESS LINES DURING ALL MACHINE STATES (Cont'd)

STATE	I	N	MNEMONIC	OPERATION	DATA BUS	MEMORY ADDRESS	$\overline{\text{MRD}}$	$\overline{\text{MWR}}$	N LINES		
S1#1	C	0-3, 8-B	LONG BRANCH	TAKEN: MRP→B; RP+1→RP	MRP	RP	0	1	0		
#2				TAKEN: B→RP.1; MRP→RP.0	M(RP+1)	RP+1	0	1	0		
S1#1		5 6 7 C D E F	LONG SKIP	NOT TAKEN: RP+1→RP	MRP	RP	0	1	0		
#2				NOT TAKEN: RP+1→RP	M(RP+1)	RP+1	0	1	0		
S1#1				TAKEN: RP+1→RP	MRP	RP	0	1	0		
#2				TAKEN: RP+1→RP	M(RP+1)	RP+1	0	1	0		
S1#1				4	NOP	NOT TAKEN: NO OPERATION	MRP	RP	0	1	0
#2						NOT TAKEN: NO OPERATION	M(RP+1)	RP+1	0	1	0
S1#1				4	NOP	NO OPERATION	MRP	RP	0	1	0
#2						NO OPERATION	M(RP+1)	RP+1	0	1	0
S1	D	0-F	SEP	N→P	NN	RN	1	1	0		
	E	0-F	SEX	N→X	NN	RN	1	1	0		
	F	0	LDX	MRX→D	MRX	RX	0	1	0		
		1	OR	MRX OR D→D	MRX	RX	0	1	0		
		2	AND	MRX AND D→D							
		3	XOR	MRX XOR D→D							
		4	ADD	MRX+D→DF, D							
		5	SD	MRX-D→DF, D							
		7	SM	D-MRX→DF; D							
		6	SHR	LSB(D)→DF; 0→MSB(D)	FLOAT	RX	1	1	0		
	8	LDI	MRP→D; RP+1→RP	MRP	RP	0	1	0			
	9	ORI	MRP OR D→D; RP+1→RP								
	A	ANI	MRP AND D→D; RP+1→RP								
	B	XRI	MRP XOR D→D; RP+1→RP								
C	ADI	MRP+D→DF, D; RP+1→RP									
D	SDI	MRP-D→DF, D; RP+1→RP									
F	SMI	D-MRP→DF, D; RP+1→RP									
E	SHL	MSB(D)→DF; 0→LSB(D)	FLOAT	RP	1	1	0				
S2	DMA IN			BUS→MR0; R0+1→R0	DATA FROM I/O DEVICE	R0	1	0	0		
	DMA OUT			MR0→BUS; R0+1→R0	MR0	R0	0	1	0		
S3	INTERRUPT			X,P→T; 0→MIE 1→P; 2→X	FLOAT	RN	1	1	0		

TABLE II. CONDITIONS ON DATA BUS AND MEMORY ADDRESS LINES DURING ALL MACHINE STATES (Cont'd)

STATE	I	N	MNEMONIC	OPERATION	DATA BUS	MEMORY ADDRESS	$\overline{\text{MRD}}$	$\overline{\text{MWR}}$	N LINES
THE FOLLOWING ARE ALL LINKED INSTRUCTIONS									
"68" PRECEDES ALL THE OP CODES, SO THERE IS A DOUBLE FETCH									
S1	0	0	STPC	STOP COUNTER CLOCK; 0 \rightarrow 32 PRESCALER	FLOAT	R0	1	1	0
		1	DTC	CNTR-1-CNTR	FLOAT	R1	1	1	0
		2	SPM2	CNTR-1 ON EF2 AND TPA	FLOAT	R2	1	1	0
		3	SCM2	CNTR-1 ON EF2 0 TO 1	FLOAT	R3	1	1	0
		4	SPM1	CNTR-1 ON EF1 AND TPA	FLOAT	R4	1	1	0
		5	SCM1	CNTR-1 ON EF1 0 TO 1	FLOAT	R5	1	1	0
		6	LDC	D-CNTR;0-CIL (IF CNTR IS STOPPED)	D	R6	1	1	0
		7	STM	CNTR-1 ON TPA \div 32	FLOAT	R7	1	1	0
		8	GEC	CNTR-D	CNTR	R8	1	1	0
		9	ETQ	IF CNTR THRU 0: \overline{Q} - \overline{Q}	FLOAT	R9	1	1	0
		A	XIE	1-XIE	FLOAT	RA	1	1	0
		B	XID	0-XIE	FLOAT	RB	1	1	0
		C	CIE	1-CIE	FLOAT	RC	1	1	0
D	CID	0-CIE	FLOAT	RD	1	1	0		
S1#1	2	0-F	DBNZ	RN-1-RN	FLOAT	RN	1	1	0
#2				MRP-B; RP+1-RP	MRP	RP	0	1	0
#3				TAKEN: B-RP.1; MRP-- RP.0 NOT TAKEN: RP+1-RP	M(RP+1)	RP+1	0	1	0
S1	3	E	BCI	TAKEN: MRP-RP.0; 0-CI NOT TAKEN: RP+1-RP	MRP	RP	0	1	0
		F	BXI	TAKEN: MRP-RP.0 NOT TAKEN: RP+1-RP	MRP	RP	0	1	0
S1#1	6	0-F	RLXA	MRX-B, RX+1-RX	MRX	RX	0	1	0
#2				B-T; MRX-B; RX+1-RX	M(RX+1)	RX+1	0	1	0
#3				B, T-RN.0, RN.1	FLOAT	RN	1	1	0
S1#1	7	4	DADC	MRX+D+DF-DF, D	MRX	RX	0	1	0
#2				DECIMAL ADJUST-DF, D	FLOAT	RP	1	1	1
S1#1	7	6	DSAV	RX-1-RX	FLOAT	RX	1	1	0
#2				T-MRX; RX-1-RX	T	RX-1	1	0	0
#3				D-MRX; RX-1-RX SHIFT D RIGHT WITH CARRY	D	RX-2	1	0	0
#4				D-MRX	D	RX-3	1	0	0
S1#1	7	7	DSMB	D-MRX-(NOT DF)-DF, D	MRX	RX	0	1	0
#2				DECIMAL ADJUST-DF, D	FLOAT	RP	1	1	0
S1#1	7	C	DACI	MRP+D+DF-DF, D; RP+1-RP	MRP	RP	0	1	0
#2				DECIMAL ADJUST-DF, D	FLOAT	RP+1	1	1	0
S1#1	7	F	DSBI	D-MRP-(NOT DF)-DF, D; RP+1-RP	MRP	RP	0	1	0
#2				DECIMAL ADJUST-DF, D	FLOAT	RP+1	1	1	0

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TABLE II. CONDITIONS ON DATA BUS AND MEMORY ADDRESS LINES DURING ALL MACHINE STATES (Cont'd)

STATE	I	N	MNEMONIC	OPERATION	DATA BUS	MEMORY ADDRESS	MRD	MWR	N LINES
THE FOLLOWING ARE ALL LINKED INSTRUCTIONS									
"68" PRECEDES ALL THE OP CODES, SO THERE IS A DOUBLE FETCH									
S1#1	8	0-F	SCAL	RN.0, RN.1→T, B	FLOAT	RN	1	1	0
#2				T→MRX; RX-1→RX	RN.0	RX	1	0	0
#3				B→MRX, RX-1→RX	RN.1	RX-1	1	0	0
#4				RP.0, RP.1→T, B	FLOAT	RP	1	1	0
#5				B, T→RN.1, RN.0	FLOAT	RN	1	1	0
#6				MRN→B; RN+1→RN	MRP	RP	0	1	0
#7				B→T; MRN→B; RN+1→RN	M(RP+1)	RP+1	0	1	0
#8				B, T→RP.0, RP.1	FLOAT	RP	1	1	0
S1#1	9	0-F	SRET	RN.0, RN.1→T, B	FLOAT	RN	1	1	0
#2				RX+1→RX	FLOAT	RX	1	1	0
#3				B, T→RP.1, RP.0	FLOAT	RP	1	1	0
#4				MRX→B; RX+1→RX	M(RX+1)	RX+1	0	1	0
#5				B→T; MRX→B	M(RX+1)	RX+2	0	1	0
#6				B, T→RN.0, RN.1	FLOAT	RN	1	1	0
S1#1	A	0-F	RSXD	RN.0, RN.1→T, B	FLOAT	RN	1	1	0
#2				T→MRX; RX-1→RX	RN.0	RX	1	0	0
#3				B→MRX; RX-1→RX	RN.1	RX-1	1	0	0
S1#1	B	0-F	RNX	RN.0, RN.1→T, B	FLOAT	RN	1	1	0
#2				B, T→RX.1, RX.0	FLOAT	RX	1	1	0
S1#1	C	0-F	RLDI	MRP→B; RP+1→RP	MRP	RP	0	1	0
#2				B→T; MRP→B; RP+1→RP	M(RP+1)	RP+1	0	1	0
#3				B, T→RN.0, RN.1; RP+1→RP	FLOAT	RN	1	1	0
S1#1	F	4	DADD	MRX+D→DF, D	MRX	RX	0	1	0
#2				DECIMAL ADJUST→DF, D	FLOAT	RP	1	1	0
S1#1	F	7	DSM	D→MRX→DF, D	MRX	RX	0	1	0
#2				DECIMAL ADJUST→DF, D	FLOAT	RP	1	1	0
S1#1	F	C	DADI	MRP+D→DF, D; RP+1→RP	MRP	RP	0	1	0
#2				DECIMAL ADJUST→DF, D	FLOAT	RP+1	1	1	0
S1#1	F	F	DSMI	D→MRP→DF, D; RP+1→RP	MRP	RP	0	1	0
#2				DECIMAL ADJUST→DF, D	FLOAT	RP+1	1	1	0

Instruction Summary

N

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0	IDL	LDN															
1	INC																
2	DEC																
3	BR	BQ	BZ	BDF	B1	B2	B3	B4	SKP	BNQ	BNZ	BNF	BN1	BN2	BN3	BN4	
4	LDA																
5	STR																
6	IRX	OUT							*	INP							
7	RET	DIS	LDXA	STXD	ADC	SDB	SHRC	SMB	SAV	MARK	REQ	SEQ	ADCI	SDBI	SHLC	SMBI	
8	GLO																
9	GHI																
A	PLO																
B	PHI																
C	LBR	LBQ	LBZ	LBDF	NOP	LSNQ	LSNZ	LSNF	LSKP	LBNO	LBNZ	LBNF	LSIE	LSQ	LSZ	LSDF	
D	SEP																
E	SEX																
F	LDX	OR	AND	XOR	ADD	SD	SHR	SM	LDI	ORI	ANI	XRI	ADI	SDI	SHL	SMI	
'68' LINKED OPCODES (DOUBLE FETCH)																	
0	STPC	DTC	SPM2	SCM2	SPM1	SCM1	LDC	STM	GEC	ETQ	XIE	XID	CIE	CID	—	—	
2	DBNZ																
3	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BCI	BXI
6	RLXA																
7	—	—	—	—	DADC	—	DSAV	DSMB	—	—	—	—	DACI	—	—	DSBI	
8	SCAL																
9	SRET																
A	RSXD																
B	RNX																
C	RLDI																
F	—	—	—	—	DADD	—	—	DSM	—	—	—	—	DADI	—	—	DSMI	

* '68' IS USED AS A LINKING OPCODE FOR THE DOUBLE FETCH INSTRUCTIONS.

IMPORTANT NOTICE

Early versions of the CDP1804AC (with NLBJ5, NLBT5, or NR appearing in the bottom brand) fully execute all CDP1802 family, CDP1805C, and CDP1806C instructions, plus the additional eight BCD arithmetic instructions and the new DBNZ instruction described in the CDP1804AC data sheet. They do not, however, execute the new DSAV instruction.

CDP1804AC

CDP1804AC Mask-Programming

The ROM pattern for the CDP1804AC may be submitted on a suitable media, such as a punched card deck, floppy diskette, or EPROM as outlined below in the Programming Options.

In addition to specifying the 2K-byte ROM pattern, the address space for the ROM and RAM must also be defined. The locations of ROM and RAM in the CDP1804AC are determined by AND-gate decoders which decode the upper memory addresses and are programmable at the time of ROM pattern masking during device fabrication. The logical

values of the decoder inputs are selectable as 1 or P (positive), 0 or N (negative), or X (don't care). A 5-bit decoder is used for the ROM selection, so the ROM can be placed at one or more of the 32 available 2K-byte blocks within the 65,536 locations of memory. Similarly, the RAM has a 10-bit decoder and can be selected at one or more of the available 64-byte blocks. If the RAM is located within the ROM space, the RAM will be enabled at the locations where both are mapped. The RAM may also be selectively disabled.

Programming Options

Address Options

The logic levels of high-order address bits are mask programmable in the CDP1804AC. The high (1), low (0), or "don't care" (X) logic status of the high-order address bits is dependent upon the desired starting address of the 2K-byte ROM block and the 64-byte RAM block. The desired logic levels for the high-order address bits (A15 through A6) can be selected by use of the ROM information sheet, as follows:

1. Translate the upper five hexadecimal starting address of the ROM block into binary.

2. Translate the upper ten hexadecimal starting addresses of the RAM block into binary.
3. Circle the corresponding 1 or 0 in columns 28 through 43 on the ROM Information Sheet, Part B.

Multiple mapping can be achieved by choosing X (don't care) for one or more of the high-order address lines; this choice will cause the ROM or RAM block to appear in more than one location in the 64K memory space. The RAM may also be disabled completely by programming the RAM enable bit (Col. 43) to a 0.

SPECIAL NOTE

Indicate your RAM starting address on the ROM information sheet, circling the address blocks under the RAM heading.

Data Programming Instructions

When a customer submits instructions for programming RCA custom ROM's, the customer must also complete the relevant parts of the ROM information sheet and submit this sheet together with the programming instruction. Programming instructions may be submitted in any one of three ways, as follows:

1. Computer card deck — use standard 80-column computer punch cards.
2. Floppy diskette — diskette information must be generated on an RCA CDP1800-series microprocessor development system.

3. Master device — a ROM, PROM, or EPROM that contains the required programming information.

The requirements for each method are explained in detail in the following paragraphs:

Computer Card Method

Use standard 80-column computer cards. Each card deck must contain, in order, a title card, an option card, a data-format card, and data cards. Punch the cards as specified in the following charts:

Title Card

Column No.	Data
1	Punch T
2-5	leave blank
6-30	*Customer Name (start at 6)
31-34	*leave blank
35-54	*Customer Address or Division (start at 35)
55-58	*leave blank
59-63	*RCA custom selection number (5 digits) (Obtained from RCA Sales Office)
64	*leave blank
65-71	*RCA device type, without CDP prefix (e.g., 1804ACE)
72	Punch an opening parenthesis (
73	Punch 8
74	Punch a closing parenthesis)
75-78	leave blank
79-80	Punch a 2-digit decimal number to indicate the deck number; the first deck should be numbered 01

• See ROM Information Sheet (Part A)

Data Programming Instructions (Cont'd)

Option Card

Use the ROM Information Sheet to select the polarity options, P, N, or X, for the desired ROM type.	
Column No.	Data
1-6	Punch the word OPTION
7	leave blank
8-17	Punch CDP1804A
18-27	leave blank
28-43	Punch 1, 0, X, or leave blank per ROM Information Sheet (Part B)
44-78	leave blank
79-80	Punch the deck number (the 2-digit number in columns 79-80 of the title card)

Data-Format Card

The data-format card specifies the form in which the data is to be entered into ROM.	
Column No.	Data
1-11	Punch the words DATA FORMAT
12	leave blank
13-15	Punch the letters HEX
16	leave blank
17-19	Punch POS
20-78	leave blank
79-80	Punch the deck number (the 2-digit number in columns 79-80 of the title card)

Data Cards

The data cards contain the hexadecimal data to be programmed into the ROM device. Each card must contain the starting address plus sixteen words of data in clusters of four hex digits.			
Column No.	Data	Column No.	Data
1-4	Punch the starting address in hexadecimal for the following data.*	26-27	2 hex digits of 9th WORD
5	Blank	28-29	2 hex digits of 10th WORD
6-7	2 hex digits of 1st WORD	30	Blank
8-9	2 hex digits of 2nd WORD	31-32	2 hex digits of 11th WORD
10	Blank	33-34	2 hex digits of 12th WORD
11-12	2 hex digits of 3rd WORD	35	Blank
13-14	2 hex digits of 4th WORD	36-37	2 hex digits of 13th WORD
15	Blank	38-39	2 hex digits of 14th WORD
16-17	2 hex digits or 5th WORD	40	Blank
18-19	2 hex digits of 6th WORD	41-42	2 hex digits of 15th WORD
20	Blank	43-44	2 hex digits of 16th WORD
21-22	2 hex digits of 7th WORD	45	Semicolon, blank if last card
23-24	2 hex digits of 8th WORD	46-78	Blank
25	Blank	79-80	Punch 2 decimal digits as in title card

*The address block must be contiguous starting at an even-numbered address. (See Sample Card-Deck Printout on page 28.)
Column 4 must be zero.

To minimize power consumption, all unused ROM locations should contain zeros.

Data Programming Instructions (Cont'd)

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80
TITLE CARD																				OPTION CARD																				DATA FORMAT CARD																																							
																				RCA																				SMYL MZ 1111																																							
																				100100000000000001																				81236 1804ACE(8)																																							
DATA FORMAT HEX POS																																																																															
92FE 331D FEFF FA7F A816 43FE 3349 92F9;																																																																															
8082 F872 3C08 0EF2 F630 AE30 4487 FA10;																																																																															
3229 92FA 56F8 0630 8EF4 FA40 3A26 92F9;																																																																															
4082 0684 8FB2 52D5 3B72 56F6 F6F6 3A17;																																																																															
																																								DATA CARDS																																							
132F CFFC 02FE FEFS 33EF 06F6 8830 F18F;																																																																															
56E0 71P4 8FA4 20D3 40A3 30F7 FFFF FFFF;																																																																															
ADDRESS																				DATA																																																											

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Sample Card-Deck Printout

Floppy-Diskette Method

The diskette contains the ROM address and data information. Title, option, and data-format information, which would otherwise be punched on computer cards, must be submitted on the ROM Information Sheet. In addition, specify the RCA Development System used to generate the diskette (CDP18S005, CDP18S007, or CDP18S008) and supply a track number or file name. If possible, include a printout of the program for verification purposes. The format of the address and data information is essentially the same as that shown on the Sample Card-Deck Printout with the addition of a carriage-return character at the end of each line and an end-of-file character (DC3) at the end of the file.

Master-Device Method

Data may be submitted on a master ROM, PROM, or EPROM device. Title, option, and data-format information, which would otherwise be punched on computer cards, must be submitted on the ROM Information Sheet. In addition, specify the master device type; RCA will select Intel types 1702, 2332A, 2704, 2708, 2716, 2732, 2758, Supertex CM3200, TI 4732, Motorola MCM68732, and Motorola MCM68A332, or their equivalents as well as RCA type CDP18U42. If more than one ROM pattern is stored in the master device, the starting address and size of each pattern must be stated on separate ROM Information Sheets. If the master-device is smaller than 2K bytes, the starting address of each master-device must be clearly identified.

ROM Information Sheet

How is ROM pattern being submitted to RCA?

- check one **Computer Cards** (Complete parts B and C)
Floppy Diskette (Complete parts A, B, C, and E)
Master Device (PROM) (Complete parts A, B, C, and D)

PART A	6-30	Customer Name (start at left)														
	35-54	Address or Division														
	59-63	RCA Custom Number (obtained from RCA Sales Office)														
	65-71	ROM Type without CDP prefix (e.g., 1804ACE)														

PART B	INTERNAL MEMORY	ROM					RAM										RAM
	INTERNAL ADDRESS	A15	A14	A13	A12	A11	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	ENABLE
	COL#	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43
	OPTIONS (circle one) 1=active high 0=active low X=don't care	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	-	

PART C	Starting address of CDP1804AC ROM and RAM blocks (in Hex)
	ROM <input type="text"/> <input type="text"/> <input type="text"/> <input type="text"/> <input type="text"/> RAM <input type="text"/> <input type="text"/> <input type="text"/> <input type="text"/> <input type="text"/>

PART D	If a master device is submitted, state type of ROM/PROM:
	Starting and last address of data block in the Master Device (in Hex).
	<input type="text"/>

PART E	If a diskette is submitted, check type of RCA Development System used.
	<input type="checkbox"/> CDP18S005 <input type="checkbox"/> CDP18S007
	Specify: Track# <input type="text"/> <input type="text"/> <input type="checkbox"/> CDP18S008
	Specify: File Name: _____
	Software program used: (check one) <input type="checkbox"/> ROM SAVE <input type="checkbox"/> SAVE PROM
Software program used: (check one) <input type="checkbox"/> MEM SAVE <input type="checkbox"/> SAVE PROM	

CMOS 8-Bit Microprocessor With On-Chip RAM[▲] and Timer/Counter

CLOCK	1	40	V _{DD}
WAIT	2	39	XTAL
CLEAR	3	38	DMA IN
Q	4	37	DMA OUT
SC1	5	36	INTERRUPT
SC0	6	35	MWR
MRD	7	34	TPA
BUS 7	8	33	TPB
BUS 6	9	32	MA7
BUS 5	10	31	MA6
BUS 4	11	30	MA5
BUS 3	12	29	MA4
BUS 2	13	28	MA3
BUS 1	14	27	MA2
BUS 0	15	26	MA1
* ME	16	25	MA0
N1	17	24	EFT
N2	18	23	EF2
NO	19	22	EF3
V _{SS}	20	21	EF4

TOP VIEW 92CS-34767

TERMINAL ASSIGNMENT

Performance Features:

- Instruction time of 4 μ s -40° to +85° C
- 113 instructions - upwards software compatible with CDP1802
- Pin compatible with CDP1802 except for V_{cc} terminal
- 16 x 16 matrix of registers for use as memory pointers (program counters, data pointers, stack pointers) or as data storage registers
- On-chip crystal or RC controlled oscillator
- 64K memory address capability

▲ CDP1805C only

* ME FOR CDP1805C
V_{DD} FOR CDP1806C

The RCA-CDP1805C and CDP1806C are functional and performance enhancements of the CDP1802 LSI CMOS 8-bit register-oriented microprocessor series and are designed for use in a wide variety of general-purpose applications.

The CDP1805C enhancements include a 64-byte RAM array, an 8-bit presettable down-counter, and 22 additional software instructions, that add subroutine call and return capability, enhanced data transfer manipulation, and control over the counter modes and interrupt arbitration.

The timer/counter generates an internal interrupt request on underflow that can be directed to the Q output line can be used in time-base, event-counting, and pulse duration measurement applications.

The CDP1806C enhancements are identical to those of the CDP1805C, but the CDP1806C contains no on-chip RAM.

Upwards software and hardware compatibility are maintained when substituting a CDP1805C, CDP1806C for other CDP1800-series microprocessors. Pinout is identical except for the replacement of V_{cc} with ME on the CDP1805C and the replacement of V_{cc} with V_{DD} on the CDP1806C.

Timing for the CDP1805C and CDP1806C is the same, except that 4.5 clock pulses are provided for memory access, Q changes 1/2 cycle earlier during SEQ and REQ instructions, and the FLAG LINES are sampled at the end of the SO machine cycle. Schmitt Triggers are provided on all control inputs, except ME. The only CDP1802 feature not retained is the LOAD MODE (WAIT = 0), which is not allowed on the CDP1805C and CDP1806C.

The CDP1805C and CDP1806C have an operating voltage range of 4 V to 6.5 V, and is supplied in a 40-lead hermetic dual-in-line ceramic package (D suffix) and in a 40-lead dual-in-line plastic package (E suffix).

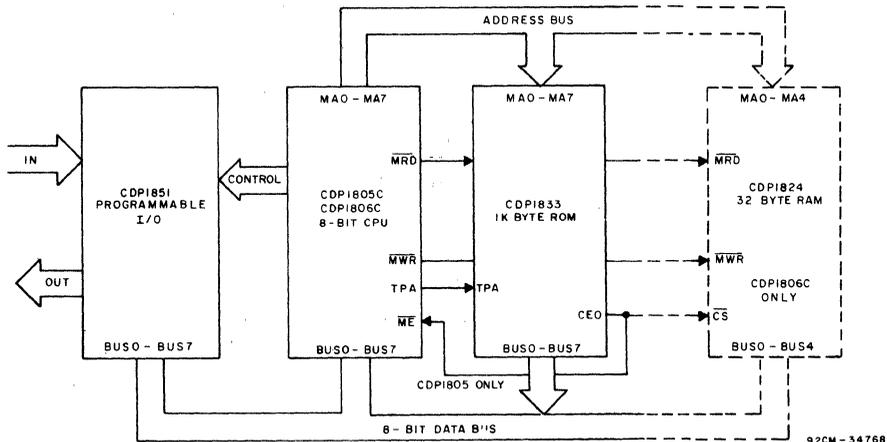


Fig. 1 - Typical CDP1805C, CDP1806C small microprocessor system.

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD}):
 (Voltage referenced to V_{SS} Terminal) -0.5 to +7 V

INPUT VOLTAGE RANGE, ALL INPUTS -0.5 to V_{DD} +0.5 V

DC INPUT CURRENT, ANY ONE INPUT ± 10 mA

POWER DISSIPATION PER PACKAGE (P_D):

For T_A = -40 to +60°C (PACKAGE TYPE E) 500 mW
 For T_A = +60 to +85°C (PACKAGE TYPE E) Derate Linearly at 12 mW/°C to 200 mW

For T_A = -55 to +100°C (PACKAGE TYPE D) 500 mW
 For T_A = +100 to +125°C (PACKAGE TYPE D) Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100 mW

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPE D -55 to +125°C
 PACKAGE TYPE E -40 to +85°C

STORAGE TEMPERATURE RANGE (T_{stg}) -65 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = -40 to +85°C

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	CONDITION	LIMITS		UNITS
		CDP1805CD, CDP1805CE CDP1806CD, CDP1806CE		
		MIN.	MAX.	
DC Operating Voltage Range	—	4	6.5	V
Input Voltage Range	—	V _{SS}	V _{DD}	
Minimum Instruction Time * (f _{CL} = 4 MHz)	5	4	—	μs
Maximum DMA Transfer Rate	5	—	0.5	MBytes/s
Maximum Clock Input Frequency, Load Capacitance (CL) = 50 pF	5	DC	4	MHz
Maximum External Counter/Timer Clock Input Frequency to EF1, EF2 t _{CLX}	5	DC	2	

* Equals 2 machine cycles - one Fetch and one Execute operation for all instructions except Long Branch, Long Skip, NOP, and "68" family instructions, which are more than two cycles.

RCA CMOS LSI Products

CDP1805C, CDP1806C

STATIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = 5\text{V} \pm 5\%$, Except as noted

CHARACTERISTIC		CONDITIONS			LIMITS			UNITS
		V_O (V)	V_{IN} (V)	V_{DD} (V)	CDP1805CD, CDP1805CE CDP1806CD, CDP1806CE			
					MIN.	TYP.*	MAX.	
Quiescent Device Current	I_{DD}	—	0, 5	5	—	50	200	μA
Output Low Drive (Sink) Current (Except XTAL)	I_{OL}	0.4	0, 5	5	1.6	4	—	mA
XTAL Output	I_{OL}	0.4	5	5	0.2	0.4	—	
Output High Drive (Source) Current (Except XTAL)	I_{OH}	4.6	0, 5	5	-1.6	-4	—	mA
XTAL	I_{OH}	4.6	0	5	-0.1	-0.2	—	
Output Voltage Low-Level	V_{OL}	—	0, 5	5	—	0	0.1	V
Output Voltage High Level	V_{OH}	—	0, 5	5	4.9	5	—	
Input Low Voltage (BUS 0 — BUS 7, \overline{ME})	V_{IL}	0.5, 4.5	—	5	—	—	1.5	
Input High Voltage (BUS 0 — BUS 7, \overline{ME})	V_{IH}	0.5, 4.5	—	5	3.5	—	—	
Schmitt Trigger Input Voltage (Except BUS 0 — BUS 7, \overline{ME})								
Positive Trigger Threshold	V_P				2.2	2.9	3.6	
Negative Trigger Threshold	V_N	0.5, 4.5	—	5	0.9	1.9	2.8	
Hysteresis	V_H				0.3	0.9	1.6	
Input Leakage Current	I_{IN}	—	0, 5	5	—	± 0.1	± 5	μA
3-State Output Leakage Current	I_{OUT}	0, 5	0, 5	5	—	± 0.2	± 5	μA
Input Capacitance	C_{IN}	—	—	—	—	5	7.5	pF
Output Capacitance	C_{OUT}	—	—	—	—	10	15	
Total Power Dissipation (f=4 MHz) Idle "00" at M(0000), $C_L = 50\text{pF}$		—	—	5	—	15	30	mW
Minimum Data Retention Voltage	V_{DR}	$V_{DD} = V_{DR}$			—	2	2.4	V
Data Retention Current	I_{DR}	$V_{DD} = 2.4$			—	25	100	μA

*Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .

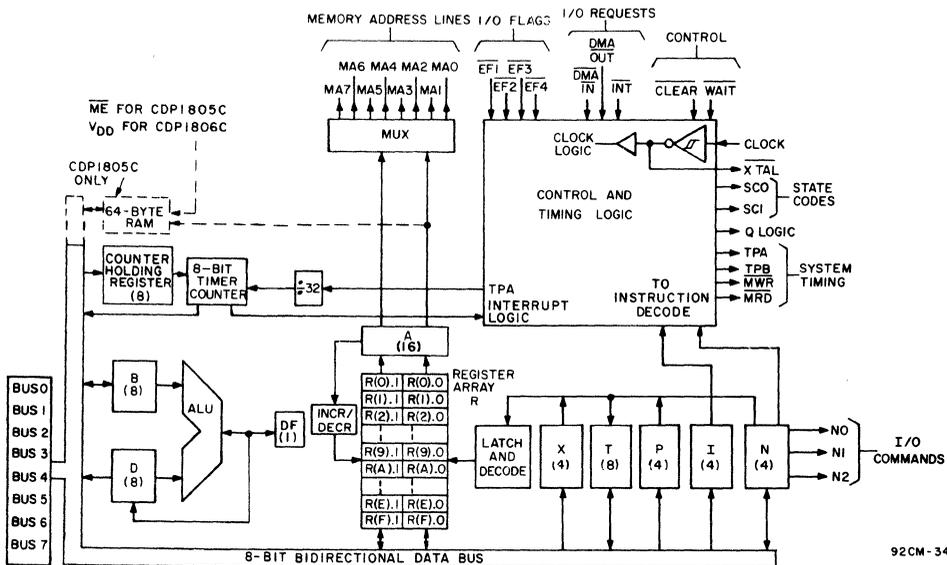
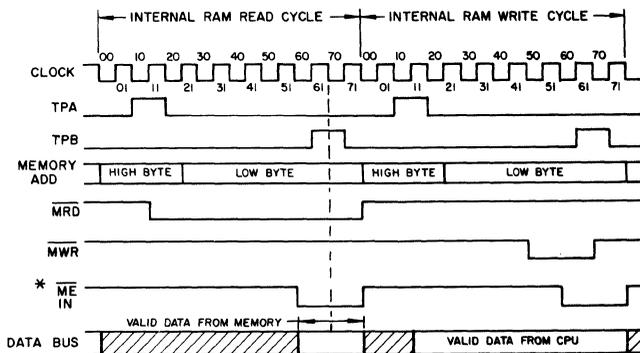


Fig. 2 - Block diagram for CDP1805C and CDP1806C.

92CM-34769

TIMING WAVEFORMS FOR POSSIBLE OPERATING MODES



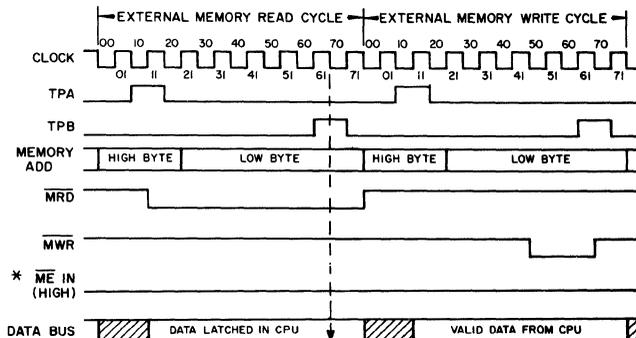
92CS-33684R1

NOTE:

ME HAS A MINIMUM SETUP AND HOLD TIME WITH RESPECT TO THE BEGINNING OF CLOCK 70. FOR A MEMORY READ OPERATION, RAM DATA WILL APPEAR ON THE DATA BUS DURING THE TIME ME IS ACTIVE. THE TIME SHOWN CAN BE LONGER, IF FOR INSTANCE, A DMA OUT OPERATION IS PERFORMED ON INTERNAL RAM DATA, TO ALLOW DATA ENOUGH TIME TO BE LATCHED INTO AN EXTERNAL DEVICE. THE LIMITATION ON ME PULSE WIDTH IS POSSIBLE BUS CONTENTION, WHICH CAN OCCUR NO EARLIER THAN CLOCK PULSE 31 OF THE NEXT MACHINE CYCLE.

* FOR CDP1805C ONLY

Fig. 3 - Internal memory operation timing waveforms for CDP1805C and CDP1806C.



* FOR CDP1805C ONLY

92CS-34771

Fig. 4 - External memory operation timing waveforms for CDP1805C and CDP1806C.

SIGNAL DESCRIPTIONS

BUS 0 to BUS 7 (Data Bus):

8-bit bidirectional DATA BUS lines. These lines are used for transferring data between the memory, the microprocessor, and I/O devices.

N0 to N2 (I/O) Lines:

Activated by an I/O instruction to signal the I/O control logic of a data transfer between memory and I/O interface.

These lines can be used to issue command codes or device selection codes to the I/O devices. The N bits are low at all times except when an I/O instruction is being executed. During this time their state is the same as the corresponding bits in the N register. The direction of data flow is defined in the I/O instruction by bit N3 (internally) and is indicated by the level of the MRD signal:

MRD = V_{DD}: Data from I/O to CPU and Memory

MRD = V_{SS}: Data from Memory to I/O

RCA CMOS LSI Products

CDP1805C, CDP1806C

SIGNAL DESCRIPTIONS (Cont'd)

EF1 to EF4 (4 Flags):

These inputs enable the I/O controllers to transfer status information to the processor. The levels can be tested by the conditional branch instructions. They can be used in conjunction with the INTERRUPT request line to establish interrupt priorities. The flag(s) are sampled at the end of every SO cycle. One additional use for EF1 and EF2 is event counting and pulse width measurement in conjunction with the Timer/Counter.

INTERRUPT, DMA-IN, DMA-OUT (3 I/O Requests)

These inputs are sampled by the CDP1805C and CDP1806C during TPB.

Interrupt Action: X and P are stored in T after executing current instruction; designator X is set to 2; designator P is set to 1; interrupt enable is reset to 0 (inhibit); and instruction execution is resumed. The interrupt action requires one machine cycle (S3).

DMA Action: Finish executing current instruction; R(0) points to memory area for data transfer; data is loaded into or read out of memory; and increment R(0).

Note: In the event of concurrent DMA and INTERRUPT requests, DMA-IN has priority followed by DMA-OUT and then INTERRUPT.

SCO, SC1, (2 State Code Lines):

These outputs indicate that the CPU is: 1) fetching an instruction, or 2) executing an instruction, or 3) processing a DMA request, or 4) acknowledging an interrupt request. The levels of state code are tabulated below. All states are valid at TPA.

State Type	State Code Lines	
	SC1	SC0
S0 (Fetch)	L	L
S1 (Execute)	L	H
S2 (DMA)	H	L
S3 (Interrupt)	H	H

H = V_{DD}, L = V_{SS}.

TPA, TPB (2 Timing Pulses):

Positive pulses that occur once in each machine cycle (TPB follows TPA). They are used by I/O controllers to interpret codes and to time interaction with the data bus. The trailing edge of TPA is used by the memory system to latch the high-order byte of the 16-bit memory address.

MA0 to MA7 (8 Memory Address Lines):

In each cycle, the higher-order byte of a 16-bit memory address appears on the memory address lines MA0-7 first. Those bits required by the memory system can be strobed into external address latches by timing pulse TPA. The low-order byte of the 16-bit address appears on the address lines after the termination of TPA.

MWR (Write Pulse):

A negative pulse appearing in a memory-write cycle, after the address lines have stabilized.

MRD (Read Level):

A low level on MRD indicates a memory read cycle. It can be used to control three-state outputs from the addressed memory and to indicate the direction of data transfer during an I/O instruction.

Q:

Single bit output from the CPU which can be set or reset, between the trailing edge of TPA and the leading edge of TPB, under program control. The Enable Toggle Q command connects the Q-line flip-flop to the output of the counter, such that each time the counter decrements from 01 to its next value, the Q line changes state. This command is cleared by a LOAD COUNTER (LDC) instruction, a CPU reset, or a BRANCH COUNTER INTERRUPT (BCI) instruction with the counter interrupt flip-flop set.

CLOCK:

Input for externally generated single-phase clock. The maximum clock frequency is 4 MHz at V_{DD} = 5 V. The clock is counted down internally to 8 clock pulses per machine cycle.

XTAL:

Connection to be used with clock input terminal, for an external crystal, if the on-chip oscillator is utilized.

WAIT, CLEAR (2 Control Lines):

Provide four control modes as listed in the following truth table:

CLEAR	WAIT	MODE
L	L	NOT ALLOWED
L	H	RESET
H	L	PAUSE
H	H	RUN

ME (Memory Enable CDP1805C Only):

This active low signal line is used to select or deselect the internal RAM. It must be active at the beginning of clock 70 for an internal RAM access to take place. Internal RAM data will appear on the data bus during the time that ME is active (after clock 31). Thus, if this data is to be latched into an external device (i.e.; during an OUTPUT instruction or DMA OUT cycle), ME should be wide enough to provide enough time for valid data to be latched.

The internal RAM is not internally mask-decoded. Decoding of the starting address is performed externally, and may reside in any 64 byte block of memory.

VDD (CDP1806C Only):

This input replaces the ME signal of the CDP1805C and must be connected to the positive power supply.

VDD, VSS, (Power Levels):

V_{SS} is the most negative supply voltage terminal and is normally connected to ground. V_{DD} is the positive supply voltage terminal. All outputs swing from V_{SS} to V_{DD}. The recommended input voltage swing is from V_{SS} to V_{DD}.

ARCHITECTURE

Fig. 1 shows a block diagram of the CDP1805C and CDP1806C. The principal feature of this system is a register array (R) consisting of sixteen 16-bit scratchpad registers. Individual registers in the array (R) are designated (selected) by a 4-bit binary code from one of the 4-bit registers labeled N, P, and X. The contents of any register can be directed to any one of the following three paths:

1. the external memory (multiplexed, higher-order byte first on to 8 memory address lines)
2. the D register (either of the two bytes can be gated to D)
3. the increment/decrement circuit where it is increased or decreased by one and stored back in the selected 16-bit register.

The three paths, depending on the nature of the instruction, may operate independently or in various combinations in the same machine cycle.

Most instructions consist of two 8-clock-pulse machine cycles. The first cycle is the fetch cycle, and the second—and more if necessary—are execute cycles. During the fetch cycle the four bits in the P designator select one of the 16 registers R(P) as the current program counter. The selected register R(P) contains the address of the memory location from which the instruction is to be fetched. When the instruction is read out from the memory, the higher-order 4 bits of the instruction byte are loaded into the I register and the lower-order 4 bits into the N register. The content of the program counter is automatically incremented by one so that R(P) is now "pointing" to the next byte in the memory.

The X designator selects one of the 16 registers R(X) to "point" to the memory for an operand (or data) in certain ALU or I/O operations.

The N designator can perform the following five functions depending on the type of instruction fetched:

1. designate one of the 16 registers in R to be acted upon during register operations
2. indicate to the I/O devices a command code or device-selection code for peripherals
3. indicate the specific operation to be executed during the ALU instructions, types of tests to be performed during the Branch instructions, or the specific operation required in a class of miscellaneous instructions
4. indicate the value to be loaded into P to designate a new register to be used as the program counter R(P)
5. indicate the value to be loaded into X to designate a new register to be used as data pointer R(X).

The registers in R can be assigned by a programmer in three different ways as program counters, as data pointers, or as scratchpad locations (data registers) to hold two bytes of data.

Program Counters

Any register can be the main program counter; the address of the selected register is held in the P designator. Other registers in R can be used as subroutine program counters. By a single instruction the contents of the P register can be changed to effect a "call" to subroutine. When interrupts are being serviced, register R(1) is used as the program counter for the user's interrupt servicing routine. After reset, and during a DMA operation, R(0) is used as the program counter. At all other times the register designated as program counter is at the discretion of the user.

Data Pointers

The registers in R may be used as data pointers to indicate a location in memory. The register designated by X (i.e. R(X)) points to memory for the following instructions (see Table 1):

1. ALU operations
2. output instructions
3. input instructions
4. register -- memory transfer
5. interrupt and subroutine handling.

The register designated by N (i.e. R(N)) points to memory for the "load D from memory" instructions 0N and 4N and the "Store D" instruction 5N. The register designated by P (i.e.; the program counter) is used as the data pointer for ALU instructions F8-FD, FF, 7C, 7D, 7F, and the RLDI instruction 68CN. During these instruction executions, the operation is referred to as "data immediate".

Another important use of R as a data pointer supports the built-in Direct-Memory-Access (DMA) function. When a DMA-In or DMA-Out request is received, one machine cycle is "stolen". This operation occurs at the end of the execute machine cycle in the current instruction. Register R(0) is always used as the data pointer during the DMA operation. The data is read from (DMA-Out) or written into (DMA-In) the memory location pointed to by the R(0) register. At the end of the transfer, R(0) is incremented by one so that the processor is ready to act upon the next DMA byte transfer request. This feature in the CDP1805C and CDP1806C architecture saves a substantial amount of logic when fast exchanges of blocks of data are required, such as with magnetic discs or during CRT-display-refresh cycles.

Data Registers

When registers in R are used to store bytes of data, instructions are provided which allow D to receive from or write into either the higher-order- or lower-order-byte portions of the register designated by N. By this mechanism (together with loading by data immediate) program pointer and data pointer designations are initialized. Also, this technique allows scratchpad registers in R to be used to hold general data. By employing increment or decrement instructions, such registers may be used as loop counters.

Register Summary

D	8 Bits	Data Register (Accumulator)
DF	1 Bit	Data Flag (ALU Carry)
B	8 Bits	Auxiliary Holding Register
R	16 Bits	1 of 16 Scratchpad Registers
P	4 Bits	Designates which register is Program Counter
X	4 Bits	Designates which register is Data Pointer
N	4 Bits	Holds Low-Order Instr. Digit
I	4 Bits	Holds High-Order Instr. Digit
T	8 Bits	Holds old X, P after interrupt (X is high nibble)
MIE	1 Bit	Master Interrupt Enable
Q	1 Bit	Output Flip Flop
CH	8 Bits	Holds Counter Jam Value

ARCHITECTURE (Cont'd)

On-Chip Clock (See Fig. 7 and 8)

Clock circuits may use either an external crystal or an RC network.

The crystal is connected between terminals 1 and 39 (CLOCK and XTAL) in parallel with a resistance (1 megohm typ.).

Frequency trimming capacitors may be required at terminals 1 and 39. For additional information on crystal oscillators, see ICAN-6565. Because of the Schmitt Trigger input, an RC oscillator can be used as shown in Fig. 7. The frequency is approximately 1/RC (See Fig. 8).

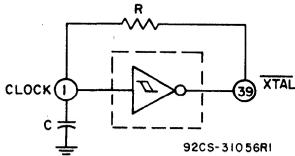


Fig. 7 - RC network for oscillator.

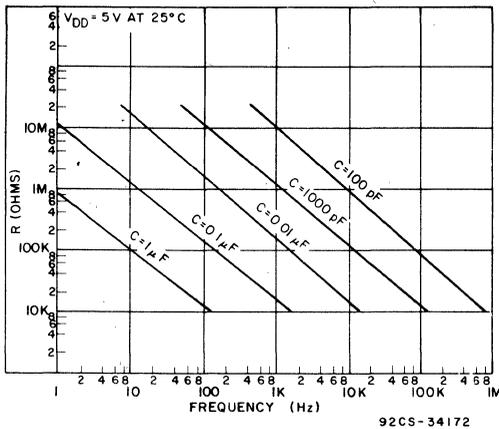


Fig. 8 - Nominal component values as a function of frequency for the RC oscillator.

CONTROL MODES

CLEAR	WAIT	MODE
L	L	NOT ALLOWED
L	H	RESET
H	L	PAUSE
H	H	RUN

The function of the modes are defined as follows:

RESET

Registers I, N, Q, counter prescaler, and counter interrupt latch are reset. MIE, XIE, and CIE are set and 0's (V_{SS}) are placed on the data bus. TPA and TPB are suppressed while reset is held and the CPU is placed in S1. The state of the counter/timer is unaffected by the RESET operation.

The first machine cycle after termination of reset is an initialization cycle which requires 9 clock pulses. During this cycle the CPU remains in S1, X, P, T, and then registers

X, P, and R(0) are reset. Interrupt and DMA servicing suppressed during the initialization cycle. The next cycle is an S0 or an S2 but never an S1 or S3. The use of a 71 instruction followed by 00 at memory locations 0000 and 0001, may be used to reset MIE, so as to preclude interrupts until ready for them. Power-up reset run can be realized by connecting an RC network to CLEAR (See Fig. 9).

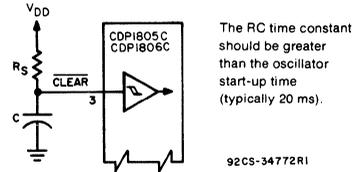


Fig. 9 - Reset diagram.

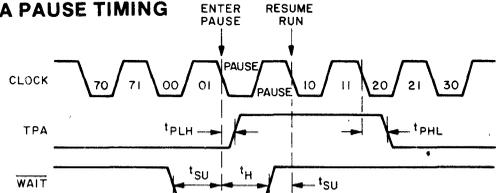
PAUSE

Stops the internal CPU timing generator, freezing the state of the processor. Pause can occur at two points in a machine cycle, on the low-to-high transition of either TPA or TPB.

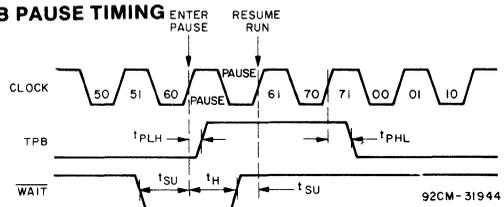
The oscillator continues to run but subsequent clock transitions are ignored. TPA and TPB remain at their previous state (See Fig. 10).

If Pause is entered while in the event counter mode, the appropriate Flag transitions will continue to decrement the counter.

TPA PAUSE TIMING



TPB PAUSE TIMING



NOTE: PAUSE (IN CLOCK WAVEFORM) WHILE REPRESENTED HERE AS ONE CLOCK CYCLE IN DURATION, COULD BE INFINITELY LONG.

Fig. 10 - Pause mode timing waveforms.

RUN

May be initiated from the Pause or Reset mode functions. If initiated from Pause, the CPU resumes operation at the point it left off. If paused at TPA, it will resume on the next high-to-low clock transition, while if paused at TPB, it will resume on the next low-to-high clock transition (See Fig. 9). When initiated from the Reset operation, the first machine cycle following Reset is always the initialization cycle. The initialization cycle is then followed by a DMA (S2) cycle or fetch (S0) from location 0000 in memory.

SCHMITT TRIGGER INPUTS

All inputs except BUS 0 — BUS 7 and \overline{ME} contain a Schmitt Trigger circuit, which is especially useful on the CLEAR input as a power-up RESET (See Fig. 10) and the CLOCK input (See Fig. 7).

STATE TRANSITIONS

The CDP1805C and CDP1806C state transitions are shown in Fig. 11. Each machine cycle requires the same period of

time, 8 clock pulses, except the initialization cycle (INIT) which requires 9 clock pulses.

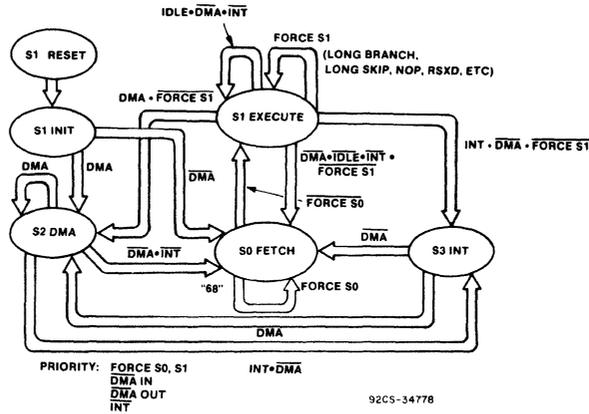


Fig. 11 - State transition diagram.

Additional Timing Waveform Notes (See Fig. 12)

The CDP1805C and CDP1806C timing specification for latching external data into the CPU requires some additional clarification.

As specified data is latched at the beginning of clock pulse 70, with a data setup time required before that edge. While this is generally true, there may be some extremely slow applications where data will be required at an earlier time.

As shown in Fig. 12, valid data must be present during the time that clock 61 • INTERNAL STROBE is valid.

INTERNAL STROBE provides a worst-case fixed width of 50 μs at 5 volts over the full temperature range, rather than a

width dependent on crystal-clock frequency. This width overlaps Clock 61 for frequencies above 10 kHz (50 μs is 1/2 clock pulse at 10 kHz), and data is latched on the high-to-low transition of clock 61. If the clock frequency used is less than 10 kHz, the high-to-low transition of INTERNAL STROBE becomes the Latch control and data must be present during the time that INTERNAL STROBE is valid.

If the CDP1805C and CDP1806C are used in the pause mode, clock timing will stop at the leading edge of TPB (or TPA). Any data which changes after this time must be valid within 50 μs of the beginning of clock 61 for proper latching into the CPU.

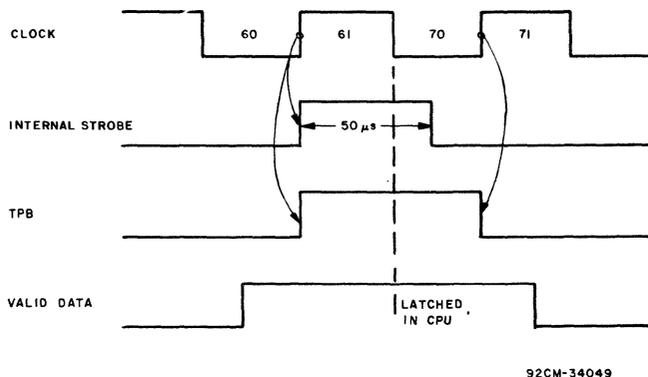


Fig. 12 - Control-timing waveforms for CDP1805C and CDP1806C.

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INSTRUCTION SET

The CDP1805C and CDP1806C instruction summary is given in Table I. Hexadecimal notation is used to refer to the 4-bit binary codes.

R(W) 0: Lower-order byte of R(W)
R(W) 1: Higher-order byte of R(W)
Operation Notation

$$M(R(N)) \rightarrow D; R(N) + 1 \rightarrow R(N)$$

In all registers bits are numbered from the least significant bit (LSB) to the most significant bit (MSB) starting with 0.

This notation means: The memory byte pointed to by R(N) is loaded into D, and R(N) is incremented by 1.

R(W): Register designated by W, where
W=N or X, or P

TABLE I — INSTRUCTION SUMMARY (For Notes, see also page 15)

INSTRUCTION	NO. OF MACHINE CYCLES	MNEMONIC	OP CODE	OPERATION
MEMORY REFERENCE				
LOAD IMMEDIATE	2	LDI	F8	M(R(P)) → D; R(P)+1 → R(P)
REGISTER LOAD IMMEDIATE	5	RLDI	68CN■	M(R(P)) → R(N).1; M(R(P)+1 → R(N).0; R(P)+2 → R(P)
LOAD VIA N	2	LDN	0N	M(R(N)) → D; FOR N NOT 0
LOAD ADVANCE	2	LDA	4N	M(R(N)) → D; R(N)+1 → R(N)
LOAD VIA X	2	LDX	F0	M(R(X)) → D
LOAD VIA X AND ADVANCE	2	LDXA	72	M(R(X)) → D; R(X)+1 → R(X)
REGISTER LOAD VIA X AND ADVANCE	5	RLXA	686N■	M(R(X)) → R(N).1; M(R(X)+1 → R(N).0; R(X)+2 → R(X)
STORE VIA N	2	STR	5N	D → M(RN)
STORE VIA X AND DECREMENT	2	STXD	73	D → M(R(X)); R(X)-1 → R(X)
REGISTER STORE VIA X AND DECREMENT	5	RSXD	68AN■	R(N).0 → M(R(X)); R(N).1 → M(R(X)-1); R(X)-2 → R(X)
REGISTER OPERATIONS				
INCREMENT REG N	2	INC	1N	R(N)+1 → R(N)
DECREMENT REG N	2	DEC	2N	R(N)-1 → R(N)
INCREMENT REG X	2	IRX	60	R(X)+1 → R(X)
GET LOW REG N	2	GLO	8N	R(N).0 → D
PUT LOW REG N	2	PLO	AN	D → R(N).0
GET HIGH REG N	2	GHI	9N	R(N).1 → D
PUT HIGH REG N	2	PHI	BN	D → R(N).1
REGISTER N TO REGISTER X COPY	4	RNX	68BN■	R(N) → R(X)
LOGIC OPERATIONS†				
OR	2	OR	F1	M(R(X)) OR D → D
OR IMMEDIATE	2	ORI	F9	M(R(P)) OR D → D; R(P)+1 → R(P)
EXCLUSIVE OR	2	XOR	F3	M(R(X)) XOR D → D
EXCLUSIVE OR IMMEDIATE	2	XRI	FB	M(R(P)) XOR D → D; R(P)+1 → R(P)
AND	2	AND	F2	M(R(X)) AND D → D
AND IMMEDIATE	2	ANI	FA	M(R(P)) AND D → D; R(P)+1 → R(P)
SHIFT RIGHT	2	SHR	F6	SHIFT D RIGHT, LSB(D) → DF, 0 → MSB(D)
SHIFT RIGHT WITH CARRY	2	SHRC	76▲	SHIFT D RIGHT, LSB(D) → DF, DF → MSB(D)
RING SHIFT RIGHT	2	RSHR		
SHIFT LEFT	2	SHL	FE	SHIFT D LEFT, MSB(D) → DF, 0 → LSB(D)
SHIFT LEFT WITH CARRY	2	SHLC	7E▲	SHIFT D LEFT, MSB(D) → DF, DF → LSB(D)
RING SHIFT LEFT	2	RSHL		

■ Previous contents of T register are destroyed during Instruction Execution.

† See page 12.

▲ This instruction is associated with more than one mnemonic. Each mnemonic is individually listed.

TABLE I — INSTRUCTION SUMMARY (Cont'd)

INSTRUCTION	NO. OF MACHINE CYCLES	MNEMONIC	OP CODE	OPERATION
ARITHMETIC OPERATIONS†				
ADD	2	ADD	F4	$M(R(X))+D-DF, D$
ADD IMMEDIATE	2	ADI	FC	$M(R(P))+D-DF, D; R(P)+1-R(P)$
ADD WITH CARRY	2	ADC	74	$M(R(X))+D+DF-DF, D$
ADD WITH CARRY, IMMEDIATE	2	ADCI	7C	$M(R(P))+D+DF-DF, D$ $R(P)+1-R(P)$
SUBTRACT D	2	SD	F5	$M(R(X))-D-DF, D$
SUBTRACT D IMMEDIATE	2	SDI	FD	$M(R(P))-D-DF, D;$ $R(P)+1-R(P)$
SUBTRACT D WITH BORROW	2	SDB	75	$M(R(X))-D-(NOT DF)-DF, D$
SUBTRACT D WITH BORROW, IMMEDIATE	2	SDBI	7D	$M(R(P))-D-(NOT DF)-DF, D;$ $R(P)+1-R(P)$
SUBTRACT MEMORY	2	SM	F7	$D-M(R(X))-DF, D$
SUBTRACT MEMORY IMMEDIATE	2	SMI	FF	$D-M(R(P))-DF, D;$ $R(P)+1-R(P)$
SUBTRACT MEMORY WITH BORROW	2	SMB	77	$D-M(R(X))-(NOT DF)-DF, D$
SUBTRACT MEMORY WITH BORROW, IMMEDIATE	2	SMBI	7F	$D-M(R(P))-(NOT DF)-DF, D$ $R(P)+1-R(P)$
BRANCH INSTRUCTIONS — SHORT BRANCH				
SHORT BRANCH	2	BR	30	$M(R(P))-R(P).0$
NO SHORT BRANCH (SEE SKP)	2	NBR	38▲	$R(P)+1-R(P)$
SHORT BRANCH IF D = 0	2	BZ	32	IF D = 0, $M(R(P))-R(P).0$ ELSE $R(P)+1-R(P)$
SHORT BRANCH IF D NOT 0	2	BNZ	3A	IF D NOT 0, $M(R(P))-R(P).0$ ELSE $R(P)+1-R(P)$
SHORT BRANCH IF DF = 1	2	BDF	33▲	IF DF = 1, $M(R(P))-R(P).0$ ELSE $R(P)+1-R(P)$
SHORT BRANCH IF POS OR ZERO	2	BPZ		
SHORT BRANCH IF EQUAL OR GREATER	2	BGE		
SHORT BRANCH IF DF = 0	2	BNF	3B▲	IF D = 0, $M(R(P))-R(P).0$ ELSE $R(P)+1-R(P)$
SHORT BRANCH IF MINUS	2	BM		
SHORT BRANCH IF LESS	2	BL		
SHORT BRANCH IF Q = 1	2	BQ	31	IF Q = 1, $M(R(P))-R(P).0$ ELSE $R(P)+1-R(P)$
SHORT BRANCH IF Q = 0	2	BNQ	39	IF Q = 0, $M(R(P))-R(P).0$ ELSE $R(P)+1-R(P)$
SHORT BRANCH IF EF1 = 1 (EF1 = VSS)	2	B1	34	IF EF1 = 1, $M(R(P))-R(P).0$ ELSE $R(P)+1-R(P)$
SHORT BRANCH IF EF1 = 0 (EF1 = VDD)	2	BN1	3C	IF EF1 = 0, $M(R(P))-R(P).0$ ELSE $R(P)+1-R(P)$
SHORT BRANCH IF EF2 = 1 (EF2 = VSS)	2	B2	35	IF EF2 = 1, $M(R(P))-R(P).0$ ELSE $R(P)+1-R(P)$

†The Arithmetic operations and the shift instructions are the only instructions that can alter the DF after an

ADD instruction:

DF = 1 denotes a carry has occurred

DF = 0 denotes a carry has not occurred

After a SUBTRACT instruction:

DF = 1 denotes no borrow. D is a true positive number

DF = 0 denotes a borrow, D is two's complement the syntax "-(NOT DF)" denotes the subtraction of the borrow

▲This instruction is associated with more than one mnemonic. Each mnemonic is individually listed.

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TABLE I — INSTRUCTION SUMMARY (Cont'd)

INSTRUCTION	NO. OF MACHINE CYCLES	MNEMONIC	OP CODE	OPERATION
BRANCH INSTRUCTIONS — SHORT BRANCH (Cont'd)				
SHORT BRANCH IF EF2 = 0 (EF2 = VDD)	2	BN2	3D	IF EF2 = 0, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH IF EF3 = 1 (EF3 = VSS)	2	B3	36	IF EF3 = 1, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH IF EF3 = 0 (EF3 = VDD)	2	BN3	3E	IF EF3 = 0, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH IF EF4 = 1 (EF4 = VSS)	2	B4	37	IF EF4 = 1, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH IF EF4 = 0 (EF4 = VDD)	2	BN4	3F	IF EF4 = 0, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH ON COUNTER INTERRUPT	3	BCI	683E•	IF CI = 1, M(R(P))→R(P).0; 0→CI ELSE R(P)+1→R(P)
SHORT BRANCH ON EXTERNAL INTERRUPT	3	BXI	683F	IF XI = 1, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
BRANCH INSTRUCTIONS — LONG BRANCH				
LONG BRANCH	3	LBR	C0	M(R(P))→R(P).1 M(R(P)+1)→R(P).0
NO LONG BRANCH (SEE LSKP)	3	NLBR	C8▲	R(P)+2→R(P)
LONG BRANCH IF D = 0	3	LBZ	C2	IF D = 0, M(R(P))→R(P).1 M(R(P)+1)→R(P).0 ELSE R(P)+2→R(P)
LONG BRANCH IF D NOT 0	3	LBNZ	CA	IF D NOT 0, M(R(P))→R(P).1 M(R(P)+1)→R(P).0 ELSE R(P)+2→R(P)
LONG BRANCH IF DF = 1	3	LBDF	C3	IF DF = 1, M(R(P))→R(P).1 M(R(P)+1)→R(P).0 ELSE R(P)+2→R(P)
LONG BRANCH IF DF = 0	3	LBNF	CB	IF DF = 0, M(R(P))→R(P).1 M(R(P)+1)→R(P).0 ELSE R(P)+2→R(P)
LONG BRANCH IF Q = 1	3	LBQ	C1	IF Q = 1, M(R(P))→R(P).1 M(R(P)+1)→R(P).0 ELSE R(P)+2→R(P)
LONG BRANCH IF Q = 0	3	LBNC	C9	IF Q = 0, M(R(P))→R(P).1 M(R(P)+1)→R(P).0 ELSE R(P)+2→R(P)
SKIP INSTRUCTIONS				
SHORT SKIP (SEE NBR)	2	SKP	38▲	R(P)+1→R(P)
LONG SKIP (SEE NLBR)	3	LSKP	C8▲	R(P)+2→R(P)
LONG SKIP IF D = 0	3	LSZ	CE	IF D = 0, R(P)+2→R(P) ELSE CONTINUE
LONG SKIP IF D NOT 0	3	LSNZ	C6	IF D NOT 0, R(P)+2→R(P) ELSE CONTINUE
LONG SKIP IF DF = 1	3	LSDF	CF	IF DF = 1, R(P)+2→R(P) ELSE CONTINUE
LONG SKIP IF DF = 0	3	LSNF	C7	IF DF = 0, R(P)+2→R(P) ELSE CONTINUE
LONG SKIP IF Q = 1	3	LSQ	CD	IF Q = 1, R(P)+2→R(P) ELSE CONTINUE
LONG SKIP IF Q = 0	3	LSNQ	C5	IF Q = 0, R(P)+2→R(P) ELSE CONTINUE
LONG SKIP IF IE = 1	3	LSIE	CC	IF IE = 1, R(P)+2→R(P) ELSE CONTINUE

▲This instruction is associated with more than one mnemonic, each mnemonic is individually listed.

CI = counter interrupt

XI = external interrupt

•ETQ cleared by LDC, reset of CPU, or BCI • (CI = 1)

TABLE I — INSTRUCTION SUMMARY (Cont'd)

INSTRUCTION	NO. OF MACHINE CYCLES	MNEMONIC	OP CODE	OPERATION
CONTROL INSTRUCTIONS				
IDLE	2	IDL	00#	WAIT FOR DMA OR INTERRUPT; M(R(0))→BUS
NO OPERATION	3	NOP	C4	CONTINUE
SET P	2	SEP	DN	N→P
SET X	2	SEX	EN	N→X
SET Q	2	SEQ	7B	1→Q
RESET Q	2	REQ	7A	0→Q
PUSH X, P TO STACK	2	MARK	79	(X, P)→T; (X, P)→M(R(2)) THEN P→X; R(2)→1→R(2)
COUNTER INSTRUCTIONS				
LOAD COUNTER	3	LDC	6806•	D→COUNTER; 0→CI; STOP COUNTER
GET COUNTER	3	GEC	6808	COUNTER→D
STOP COUNTER	3	STPC	6800	STOP COUNTER CLOCK; 0→÷32 PRESCALER
DECREMENT COUNTER	3	DTC	6801	COUNTER-1→COUNTER
SET TIMER MODE AND START	3	STM	6807	TPA÷32→COUNTER CLOCK
SET COUNTER MODE 1 AND START	3	SCM1	6805	EF1→COUNTER CLOCK
SET COUNTER MODE 2 AND START	3	SCM2	6803	EF2→COUNTER CLOCK
SET PULSE WIDTH MODE 1 AND START	3	SPM1	6804	TPA, EF1→COUNTER CLOCK; EF1 ≠ STOPS COUNT
SET PULSE WIDTH MODE 2 AND START	3	SPM2	6802	TPA, EF2→COUNTER CLOCK; EF2 ≠ STOPS COUNT
ENABLE TOGGLE Q	3	ETQ	6809•	IF COUNTER = 01•NEXT COUNTER CLOCK ≠ : Q→Q
INTERRUPT CONTROL				
EXTERNAL INTERRUPT ENABLE	3	XIE	680A	1→XIE
EXTERNAL INTERRUPT DISABLE	3	XID	680B	0→XIE
COUNTER INTERRUPT ENABLE	3	CIE	680C	1→CIE
COUNTER INTERRUPT DISABLE	3	CID	680D	0→CIE
RETURN	2	RET	70	M(R(X))→X, P; R(X)+1→R(X); 1→MIE
DISABLE	2	DIS	71	M(R(X))→X, P; R(X)+1→R(X); 0→MIE
SAVE	2	SAV	78	T→M(R(X))
INPUT-OUTPUT BYTE TRANSFER				
OUTPUT 1	2	OUT 1	61	M(R(X))→BUS; R(X)+1→R(X); N LINES=1
OUTPUT 2	2	OUT 2	62	M(R(X))→BUS; R(X)+1→R(X); N LINES=2
OUTPUT 3	2	OUT 3	63	M(R(X))→BUS; R(X)+1→R(X); N LINES=3
OUTPUT 4	2	OUT 4	64	M(R(X))→BUS; R(X)+1→R(X); N LINES=4
OUTPUT 5	2	OUT 5	65	M(R(X))→BUS; R(X)+1→R(X); N LINES=5
OUTPUT 6	2	OUT 6	66	M(R(X))→BUS; R(X)+1→R(X); N LINES=6
OUTPUT 7	2	OUT 7	67	M(R(X))→BUS; R(X)+1→R(X); N LINES=7
INPUT 1	2	INP 1	69	BUS→M(R(X)); BUS→D; N LINES=1
INPUT 2	2	INP 2	6A	BUS→M(R(X)); BUS→D; N LINES=2
INPUT 3	2	INP 3	6B	BUS→M(R(X)); BUS→D; N LINES=3
INPUT 4	2	INP 4	6C	BUS→M(R(X)); BUS→D; N LINES=4
INPUT 5	2	INP 5	6D	BUS→M(R(X)); BUS→D; N LINES=5
INPUT 6	2	INP 6	6E	BUS→M(R(X)); BUS→D; N LINES=6
INPUT 7	2	INP 7	6F	BUS→M(R(X)); BUS→D; N LINES=7

#An IDLE instruction initiates a repeating S1 cycle. The processor will continue to idle until an I/O request (INTERRUPT, DMA-IN, or DMA-OUT) is activated. When the request is acknowledged, the IDLE cycle is terminated and the I/O request is serviced, and then normal operation is resumed.

•ETQ cleared by LDC, reset of CPU, or BCI•(CI = 1).

RCA CMOS LSI Products
CDP1805C, CDP1806C

TABLE I — INSTRUCTION SUMMARY (Cont'd)

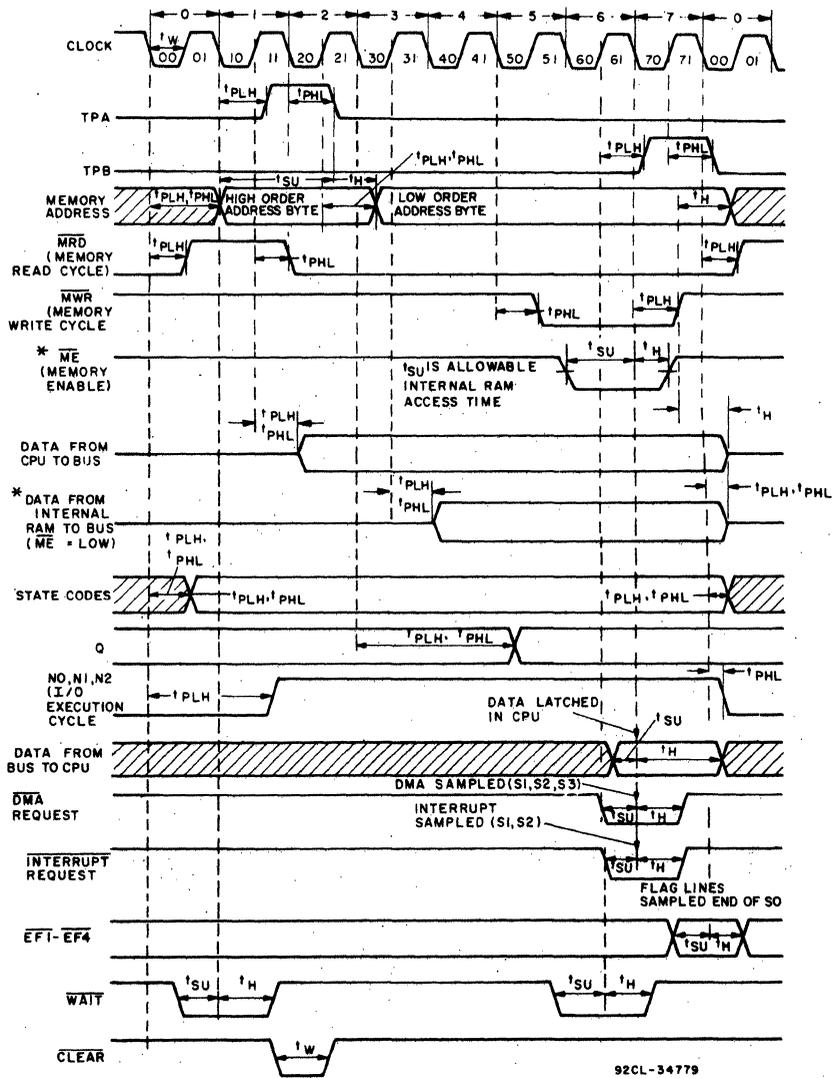
INSTRUCTION	NO. OF MACHINE CYCLES	MNEMONIC	OP CODE	OPERATION
CALL AND RETURN				
STANDARD CALL	10	SCAL	688N■	R(N).0→M(R(X); R(N).1→M(R(X)-1); R(X)-2→R(X); R(P)→ R(N); THEN M(R(N))→ R(P).1; M(R(N)+1)→R(P).0; R(N)+2→R(N)
STANDARD RETURN	8	SRET	689N■	R(N)→R(P); M(R(X)+1) →R(N).1; M(R(X)+2)→ R(N).0; R(X)+2→R(X)

■ Previous contents of T register are destroyed during Instruction Execution.

Notes for TABLE I

- Long-Branch, Long-Skip and No Op instructions require three cycles to complete (1 fetch + 2 execute).
 Long-Branch instructions are three bytes long. The first byte specifies the condition to be tested; and the second and third byte, the branching address.
 The long-branch instructions can:
 - Branch unconditionally
 - Test for D=0 or D≠0
 - Test for DF=0 or DF=1
 - Test for Q=0 or Q=1
 - Effect an unconditional no branch
 If the tested condition is met, then branching takes place; the branching address bytes are loaded in the high-and low-order bytes of the current program counter, respectively. This operation effects a branch to any memory location. If the tested condition is not met, the branching address bytes are skipped over, and the next instruction in sequence is fetched and executed. This operation is taken for the case of unconditional no branch (NLBR).
- The short-branch instructions are two or three bytes long. The first byte specifies the condition to be tested, and the second specifies the branching address, except for the branches on interrupt. For those, the first two bytes specify the condition to be tested and the third byte specifies the branching address.
 The short branch instruction can:
 - Branch unconditionally
 - Test for D=0 or D≠0
 - Test for DF=0 or DF=1
 - Test for Q=0 or Q=1
 - Test the status (1 or 0) of the four EF flags
 - Effect an unconditional no branch
 - Test for interrupts
 If the tested condition is met, then branching takes place; the branching address byte is loaded into the low-order byte position of the current program counter. This effects a branch within the current 256-byte page of the memory, i.e., the page which holds the branching address. If the tested condition is not met, the branching address byte is skipped over, and the next instruction in sequence is fetched and executed. This same action is taken in the case of unconditional no branch (NBR).
- The skip instructions are one byte long. There is one Unconditional Short-Skip (SKP) and eight Long-Skip instructions.
 The Unconditional Short-Skip instruction takes 2 cycles to complete (1 fetch + 1 execute). Its action is to skip over the byte following it. Then the next instruction in sequence is fetched and executed. This SKP instruction is identical to the unconditional no-branch instruction (NBR) except that the skipped-over byte is not considered part of the program.
 The Long-Skip instructions take three cycles to complete (1 fetch + 2 execute).
 They can:
 - Skip unconditionally
 - Test for D=0 or D≠0
 - Test for DF=0 or DF=1
 - Test for Q=0 or Q=1
 - Test for IE=1
 If the tested condition is met, then Long Skip takes place; the current program counter is incremented twice. Thus two bytes are skipped over and the next instruction in sequence is fetched and executed. If the tested condition is not met, then no action is taken. Execution is continued by fetching the next instruction in sequence.
- Instructions 6800 through 680D, 683E, and 683F take 3 machine cycles; 68BN takes 4 machine cycles; 686N, 68AN, and 68CN take 5 machine cycles; 688N takes 10 machine cycles; and 689N takes 8 machine cycles. In all cases, the first two cycles are fetches and subsequent cycles are executes. The first byte (68) of these two byte op codes is used to generate the second fetch, the second byte is then interpreted differently than the same code without the 68 prefix. DMA and INT requests are not serviced until the end of the last execute cycle. For the instructions noted in TABLE I with ■, previous contents of T register are destroyed during INSTRUCTION EXECUTION.

1800-Series Microprocessors and Microcomputers
CDP1805C, CDP1806C



92CL-34779

- NOTES:
1. THIS TIMING DIAGRAM IS USED TO SHOW SIGNAL RELATIONSHIPS ONLY AND DOES NOT REPRESENT ANY SPECIFIC MACHINE CYCLE.
 2. ALL MEASUREMENTS ARE REFERENCED TO 50% POINT OF THE WAVEFORMS.
 3. SHADED AREAS INDICATED "DON'T CARE" OR UNDEFINED STATE; MULTIPLE TRANSISTIONS MAY OCCUR DURING THIS PERIOD.

* FOR THE CDP1805C ONLY.

Fig. 13 - Objective dynamic timing waveforms for CDP1805C and CDP1806C.

RCA CMOS LSI Products
CDP1805C, CDP1806C

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $C_L = 50\text{ pF}$, $V_{DD} = 5\text{ V} \pm 5\%$.

CHARACTERISTIC	LIMITS		UNITS	
	CDP1805C and CDP1806C			
	Typ.*	Max.		
Propagation Delay Times:				
Clock to TPA, TPB	t_{PLH}, t_{PHL}	150	275	ns
Clock-to-Memory High-Address Byte	t_{PLH}, t_{PHL}	200	325	
Clock-to-Memory Low-Address Byte	t_{PLH}, t_{PHL}	150	250	
Clock to $\overline{\text{MRD}}$	t_{PLH}, t_{PHL}	200	325	
Clock to $\overline{\text{MWR}}$	t_{PLH}, t_{PHL}	150	275	
Clock to (CPU DATA to BUS)	t_{PLH}, t_{PHL}	275	475	
Clock to State Code	t_{PLH}, t_{PHL}	225	400	
Clock to Q	t_{PLH}, t_{PHL}	200	350	
Clock to N	t_{PLH}, t_{PHL}	250	425	
Clock to Internal RAM Data to BUS	t_{PLH}, t_{PHL}	420	650	
Minimum Set Up and Hold Times:■				
Data Bus Input Set Up	t_{SU}	-100	0	ns
Data Bus Input Hold	t_H	125	225	
DMA Set Up	t_{SU}	-75	0	
DMA Hold	t_H	125	200	
$\overline{\text{ME}}$ Set Up	t_{SU}	-25	0	
$\overline{\text{ME}}$ Hold	t_H	90	150	
Interrupt Set Up	t_{SU}	-100	0	
Interrupt Hold	t_H	125	200	
$\overline{\text{WAIT}}$ Set Up	t_{SU}	20	50	
$\overline{\text{EF1-4}}$ Set Up	t_{SU}	-125	0	
$\overline{\text{EF1-4}}$ Hold	t_H	125	225	
Minimum Pulse Width Times:■				
$\overline{\text{CLEAR}}$ Pulse Width	t_{WL}	75	225	ns
CLOCK Pulse Width	t_{WL}	75	125	

*Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .

■Maximum limits of minimum characteristics are the values above which all devices function.

TIMING SPECIFICATIONS as a function of T ($T = 1/f_{\text{Clock}}$) at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = 5\text{ V} \pm 5\%$.

CHARACTERISTIC	LIMITS		UNITS	
	CDP1805C and CDP1806C			
	Min.	Typ.*		
High-Order Memory-Address Byte Set Up to TPA \wedge Time	T_{SU}	2T-150	2T-75	ns
High-Order Memory-Address Byte Hold after TPA Time	t_H	T/2-50	T/2-15	
Low-Order Memory-Address Byte Hold after WR Time	t_H	T+0	T+100	
CPU Data to Bus Hold after WR Time	t_H	T-200	T-100	
Required Memory Access Time Address to Data	t_{ACC}	4.5T-250	4.5T-100	

*Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .

TABLE II. CONDITIONS ON DATA BUS AND MEMORY ADDRESS LINES DURING ALL MACHINE STATES

STATE	I	N	MNEMONIC	OPERATION	DATA BUS	MEMORY ADDRESS	MRD	MWR	N LINES
S1	RESET			0-Q, I, N; 1-CIE, XIE	00	XXXX	1	1	0
	INITIALIZE NOT PROGRAMMER ACCESSIBLE			X, P-T THEN 0-X, P; 1-MIE, 0000-R0	00▲	XXXX	1	1	0
S0	FETCH			MRP-1, N; RP+1-RP	MRP	RP	0	1	0
S1	0	0	IDL	MRO-BUS WAIT FOR DMA OR INT	MRO	R0	0	1	0
	0	1-F	LDN	MRN-D	MRN	RN	0	1	0
	1	0-F	INC	RN+1-RN	FLOAT	RN	1	1	0
	2	0-F	DEC	RN-1-RN	FLOAT	RN	1	1	0
	3	0-F	SHORT BRANCH	TAKEN: MRP-RP.0 NOT TAKEN: RP+1-RP	MRP	RP	0	1	0
	4	0-F	LDA	MRN-D; RN+1-RN	MRN	RN	0	1	0
	5	0-F	STR	D-MRN	D	RN	1	0	0
	6	0	IRX	RX+1-RX	MRX	RX	0	1	0
	6	1	OUT 1	MRX-BUS; RX+1-RX	MRX	RX	0	1	1
		2	OUT 2						2
		3	OUT 3						3
		4	OUT 4						4
		5	OUT 5						5
		6	OUT 6						6
		7	OUT 7						7
	7	9	INP 1	BUS-MRX, D	DATA FROM I/O DEVICE	RX	1	0	1
		A	INP 2						2
		B	INP 3						3
		C	INP 4						4
		D	INP 5						5
		E	INP 6						6
		F	INP 7						7
	7	0	RET	MRX-(X,P); RX+1-RX 1-MIE	MRX	RX	0	1	0
		1	DIS	MRX-(X,P); RX+1-RX 1-MIE	MRX	RX	0	1	0
		2	LDXA	MRX-D; RX+1-RX	MRX	RX	0	1	0
		3	STXD	D-MRX; RX-1-RX	D	RX	1	0	0
		4	ADC	MRX+D+DF-DF, D	MRX	RX	0	1	0
		5	SDB	MRX-D-DFN-DF, D	MRX	RX	0	1	0
		6	SHRC	LSB(D)-DF; DF-MSB(D)	FLOAT	RX	1	1	0
		7	SMB	D-MRX-DFN-DF, D	MRX	RX	0	1	0
8		SAV	T-MRX	T	RX	1	0	0	
9		MARK	(X,P)-T, MR2; P-X R2-1-R2	T	R2	1	0	0	
A		REQ	0-Q	FLOAT	RP	1	1	0	
B		SEQ	1-Q	FLOAT	RP	1	1	0	
C		ADC1	MRP+D+DF-DF, D; RP+1	MRP	RP	0	1	0	
D		SDB1	MRP-D-DFN-DF, D; RP+1	MRP	RP	0	1	0	
E		SHLC	MSB(D)-DF; DF-LSB(D)	FLOAT	RP	1	1	0	
F	SMB1	D-MRP-DFN-DF, D; RP+1	MRP	RP	0	1	0		
8	0-F	GLO	RN.0-D	RN.0	RN	1	1	0	
9	0-F	GHI	RN.1-D	RN.1	RN	1	1	0	
A	0-F	PLO	D-RN.0	D	RN	1	1	0	
B	0-F	PHI	D-RN.1	D	RN	1	1	0	

▲ = Data Bus Floats for first 2-1/2 clocks of the 9 clock initialization cycle; all zeros for remainder of cycle.

RCA CMOS LSI Products
CDP1805C, CDP1806C

TABLE II. CONDITIONS ON DATA BUS AND MEMORY ADDRESS LINES DURING ALL MACHINE STATES (Cont'd)

STATE	I	N	MNEMONIC	OPERATION	DATA BUS	MEMORY ADDRESS	MRD	MWR	N LINES
S1#1	C	0-3 8-B	LONG BRANCH	TAKEN: MRP-B; RP+1-RP	MRP	RP	0	1	0
#2				TAKEN: B-RP.1; MRP-RP.0	M(RP+1)	RP+1	0	1	0
S1#1				NOT TAKEN RP+1-RP	MRP	RP	0	1	0
#2				NOT TAKEN: RP+1-RP	M(RP+1)	RP+1	0	1	0
S1#1		5 6 7 C D E F	LONG SKIP	TAKEN: RP+1-RP	MRP	RP	0	1	0
#2				TAKEN: RP+1-RP	M(RP+1)	RP+1	0	1	0
S1#1				NOT TAKEN: NO OPERATION	MRP	RP	0	1	0
#2				NOT TAKEN: NO OPERATION	MRP	RP	0	1	0
S1#1	4	NOP	NO OPERATION	MRP	RP	0	1	0	
#2			NO OPERATION	MRP	RP	0	1	0	
S1#1			NO OPERATION	MRP	RP	0	1	0	
S1	D	0-F	SEP	N-P	NM	RN	1	1	0
	E	0-F	SEX	N-X	NN	RN	1	1	0
	F	0	LDX	MRX-D	MRX	RX	0	1	0
		1	OR	MRX OR D-D	MRX	RX	0	1	0
		2	AND	MRX AND D-D					
		3	XOR	MRX XOR D-D					
		4	ADD	MRX+D-DF, D					
		5	SD	MRX-D-DF, D					
		7	SM	D-MRX-DF, D					
		6	SHR	LSB(D)-DF; 0-MSB(D)	FLOAT	RX	1	1	0
		8	LDI	MRP-D; RP+1-RP	MRP	RP	0	1	0
		9	ORI	MRP OR D-D; RP+1-RP					
	A	ANI	MRP AND D-D; RP+1-RP						
	B	XRI	MRP XOR D-D; RP+1-RP						
C	ADI	MRP+D-DF, D; RP+1-RP							
D	SDI	MRP-D-DF, D; RP+1-RP							
F	SMI	D-MRP-DF, D; RP+1-RP							
E	SHL	MSB(D)-DF; 0-LSB(D)	FLOAT	RP	1	1	0		
S2	DMA IN		BUS-MR0; R0+1-R0		DATA FROM I/O DEVICE	R0	1	0	0
	DMA OUT		MR0-BUS; R0+1-R0		MR0	R0	0	1	0
S3	INTERRUPT		X,P-T; 0-MIE 1-P; 2-X		FLOAT	RN	1	1	0

TABLE II. CONDITIONS ON DATA BUS AND MEMORY ADDRESS LINES DURING ALL MACHINE STATES (Cont'd)

STATE	I	N	MNEMONIC	OPERATION	DATA BUS	MEMORY ADDRESS	$\overline{\text{MRD}}$	$\overline{\text{MWR}}$	N LINES
THE FOLLOWING ARE ALL LINKED INSTRUCTIONS "68" PRECEDES ALL THE OP CODES, SO THERE IS A DOUBLE FETCH									
S1	0	0	STPC	STOP COUNTER CLOCK; 0→+32 PRESCALER	FLOAT	R0	1	1	0
		1	DTC	CNTR-1-CNTR	FLOAT	R1	1	1	0
		2	SPM2	CNTR-1 ON EF2 AND TPA	FLOAT	R2	1	1	0
		3	SCM2	CNTR-1 ON EF2 0 TO 1	FLOAT	R3	1	1	0
		4	SPM1	CNTR-1 ON EF1 AND TPA	FLOAT	R4	1	1	0
		5	SCM1	CNTR-1 ON EF1 0 TO 1	FLOAT	R5	1	1	0
		6	LDC	D-CNTR;0-CI;STOP CNTR	D	R6	1	1	0
		7	STM	CNTR-1 ON TPA+32	FLOAT	R7	1	1	0
		8	GEC	CNTR-D	CNTR	R8	1	1	0
		9	ETQ	IF CNTR THRU 0: Q-Q	FLOAT	R9	1	1	0
		A	XIE	1-XIE	FLOAT	RA	1	1	0
		B	XID	0-XIE	FLOAT	RB	1	1	0
		C	CIE	1-CIE	FLOAT	RC	1	1	0
		D	CID	0-CIE	FLOAT	RD	1	1	0
	3	E	BCI	TAKEN: MRP-RP.0;0-CI NOT TAKEN: RP+1-RP	MRP	RP	0	1	0
F		BXI	TAKEN: MRP-RP.0 NOT TAKEN: RP+1-RP	MRP	RP	0	1	0	
S1#1	6	0-F	RLXA	MRX-B, RX+1-RX	MRX	RX	0	1	0
#2				B-T; MRX-B; RX+1-RX	M(RX+1)	RX+1	0	1	0
#3				B, T-RN.0, RN.1	FLOAT	RN	1	1	0
S1#1	8	0-F	SCAL	RN.0, RN.1-T, B	FLOAT	RN	1	1	0
#2				T-MRX; RX-1-RX	RN.0	RX	1	0	0
#3				B-MRX; RX-1-RX	RN.1	RX-1	1	0	0
#4				RP.0 RP.1-T, B	FLOAT	RP	1	1	0
#5				B, T-RN.1, RN.0	FLOAT	RN	1	1	0
#6				MRN-B; RN+1-RN	MRP	RP	0	1	0
#7				B-T; MRN-B; RN+1-RN	M(RP+1)	RP+1	0	1	0
#8				B, T-RP.0, RP.1	FLOAT	RP	1	1	0
S1#1	9	0-F	SRET	RN.0, RN.1-T, B	FLOAT	RN	1	1	0
#2				RX+1-RX	FLOAT	RX	1	1	0
#3				B, T-RP.1, RP.0	FLOAT	RP	1	1	0
#4				MRX-B; RX+1-RX	M(RX+1)	RX+1	0	1	0
#5				B-T; MRX-B	M(RX+1)	RX+2	0	1	0
#6				B, T-RN.0, RN.1	FLOAT	RN	1	1	0
S1#1	A	0-F	RSXD	RN.0, RN.1-T, B	FLOAT	RN	1	1	0
#2				T-MRX; RX-1-RX	RN.0	RX	1	0	0
#3				B-MRX; RX-1-RX	RN.1	RX-1	1	0	0
S1#1	B	0-F	RNx	RN.0, RN.1-T, B	FLOAT	RN	1	1	0
#2				B, T-RX.1, RX.0	FLOAT	RX	1	1	0
S1#1	C	0-F	RLDI	MRP-B; RP+1-RP	MRP	RP	0	1	0
#2				B-T; MRP-B; RP+1-RP	M(RP+1)	RP+1	0	1	0
#3				B, T-RN.0, RN.1; RP+1-RP	FLOAT	RN	1	1	0

RCA CMOS LSI Products
CDP1805C, CDP1806C

Instruction Summary
N

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0	IDL	LDN															
1	INC																
2	DEC																
3	BR	BQ	BZ	BDF	B1	B2	B3	B4	SKP	BNQ	BNZ	BNF	BN1	BN2	BN3	BN4	
4	LDA																
5	STR																
6	IRX	OUT							*	INP							
7	RET	DIS	LDXA	STXD	ADC	SDB	SHRC	SMB	SAV	MARK	REQ	SEQ	ADCI	SDBI	SHLC	SMBI	
8	GLO																
9	GHI																
A	PLO																
B	PHI																
C	LBR	LBQ	LBZ	LBDF	NOP	LSNQ	LSNZ	LSNF	LSKP	LBNQ	LBNZ	LBNF	LSIE	LSQ	LSZ	LSDF	
D	SEP																
E	SEX																
F	LDX	OR	AND	XOR	ADD	SD	SHR	SM	LDI	ORI	ANI	XRI	ADI	SDI	SHL	SMI	
'68' LINKED OPCODES (DOUBLE FETCH)																	
0	STPC	DTC	SPM2	SCM2	SPM1	SCM1	LDC	STM	GEC	ETQ	XIE	XID	CIE	CID	—	—	
3	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BCI	BXI	
6	RLXA																
8	SCAL																
9	SRET																
A	RSXD																
B	RNX																
C	RLDI																

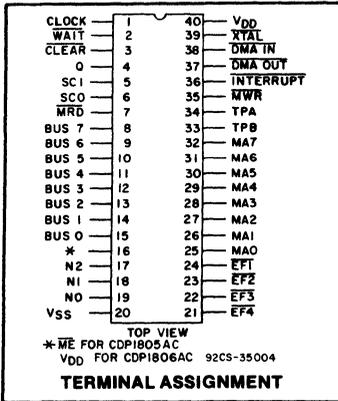
* '68' IS USED AS A LINKING OPCODE FOR THE DOUBLE FETCH INSTRUCTIONS.

CMOS 8-Bit Microprocessor With ON-CHIP RAM Δ and Timer/Counter

Performance Features:

- Instruction time of 3.2 μ s, -40 to +85°C
- 123 instructions - upwards software compatible with CDP1802, CDP1805, CDP1806
- BCD arithmetic instructions
- Low-power IDLE mode
- Pin compatible with CDP1802, CDP1805, CDP1806, except for V_{cc} terminal
- 64K-byte memory address capability
- 64 bytes of on-chip RAM Δ
- 16 x 16 matrix of on-board registers
- On-chip crystal or RC controlled oscillator
- 8-bit timer/counter

Δ CDP1805AC only



The RCA-CDP1805AC and CDP1806AC are functional and performance enhancements of the CDP1802, CDP1805C, and CDP1806C LSI CMOS 8-bit register-oriented microprocessor series and are designed for use in general-purpose applications.

The CDP1805AC hardware enhancements include a 64-byte RAM array and a 8-bit presettable down counter. The timer/counter which generates an internal interrupt request, can be programmed for use in time-base, event-counting, and pulse-duration measurement applications. The timer/counter underflow output can also be directed to the Q output terminal. The CDP1806AC hardware enhancements are identical to the CDP1805AC, except the CDP1806AC contains no on-chip RAM.

The CDP1805AC and CDP1806AC are identical to the CDP1804AC, except for the on-chip memory, and may be used for CDP1804AC development purposes.

The CDP1805AC and CDP1806AC software enhancements include 22 more instructions than the CDP1802 and 10 more instructions than the CDP1805C and CDP1806C. The 32 new software instructions add subroutine call and return capability, enhanced data transfer manipulation, timer/counter control, improved interrupt handling, single-instruction loop counting, and BCD arithmetic.

Upwards software and hardware compatibility is maintained when substituting a CDP1805AC or CDP1806AC for other CDP1800-series microprocessors. Pinout is identical except for the replacement of V_{cc} with \overline{ME} on the CDP1805AC and the replacement of V_{cc} with V_{DD} on the CDP1806AC.

The CDP1805AC and CDP1806AC have an operating voltage range of 4 V to 6.5 V and are supplied in a 40-lead hermetic dual-in-line ceramic package (D suffix) and in a 40-lead dual-in-line plastic package (E suffix).

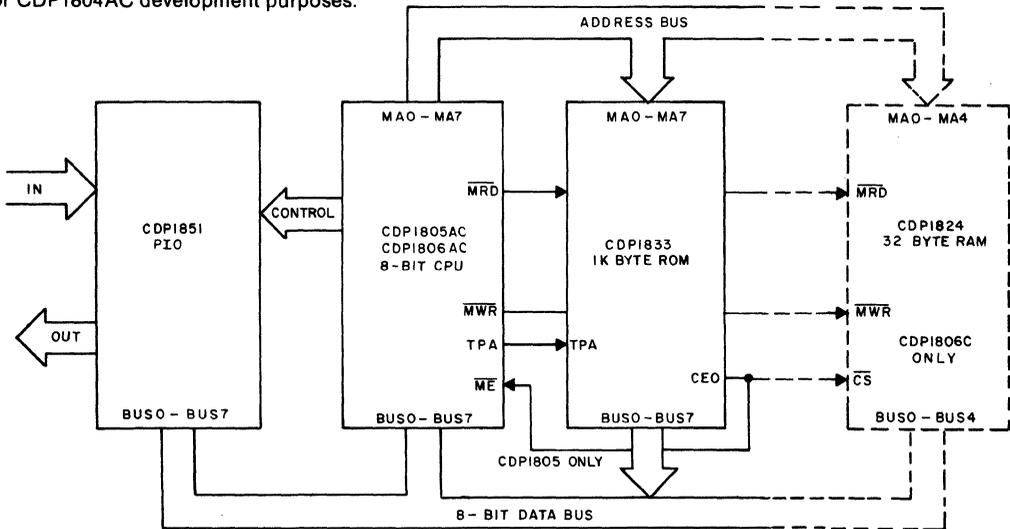


Fig. 1 - Typical CDP1805AC, CDP1806AC small microprocessor system.

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RCA CMOS LSI Products

CDP1805AC, CDP1806AC

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD}):	
(Voltage referenced to V_{SS} Terminal)	-0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to $V_{DD} + 0.5$ V
DC INPUT CURRENT, ANY ONE INPUT	± 10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For $T_A = -40$ to $+60^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +60$ to $+85^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 12 mW/ $^\circ\text{C}$ to 200 mW
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE D)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE D)	Derate Linearly at 12 mW/ $^\circ\text{C}$ to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
For $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE D	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E	-40 to $+85^\circ\text{C}$
STORAGE TEMPERATURE RANGE (T_{stg})	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ in. (1.59 ± 0.79 mm) from case for 10 s max.	$+265^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS at $T_A = -40$ to $+85^\circ\text{C}$

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	CONDITION V_{DD} (V)	LIMITS		UNITS
		CDP1805ACD, CDP1805ACE CDP1806ACD, CDP1806ACE		
		MIN.	MAX.	
DC Operating Voltage Range	—	4	6.5	V
Input Voltage Range	—	V_{SS}	V_{DD}	
Minimum Instruction Time* ($f_{CL} = 5$ MHz)	5	3.2	—	μs
Maximum DMA Transfer Rate	5	—	0.625	Mbytes/s
Maximum Clock Input Frequency, Load Capacitance (CL) = 50 pF	5	DC	5	MHz
Maximum External Counter/Timer Clock Input Frequency to $\overline{EF1}$, $\overline{EF2}$ t_{CLX}	5	DC	2	

*Equals 2 machine cycles - one Fetch and one Execute operation for all instructions except Long Branch, Long Skip, NOP, and "68" family instructions, which are more than two cycles.

1800-Series Microprocessors and Microcomputers
CDP1805AC, CDP1806AC

STATIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} \pm 5\%$, Except as noted

CHARACTERISTIC		CONDITIONS			LIMITS			UNITS
		V_O (V)	V_{IN} (V)	V_{DD} (V)	CDP1805ACD, CDP1805ACE CDP1806ACD, CDP1806ACE			
					Min.	Typ.*	Max.	
Quiescent Device Current	I_{DD}	—	0, 5	5	—	50	200	μA
Output Low Drive (Sink) Current (Except XTAL)	I_{OL}	0.4	0, 5	5	1.6	4	—	mA
XTAL Output	I_{OL}	0.4	5	5	0.2	0.4	—	
Output High Drive (Source) Current (Except XTAL)	I_{OH}	4.6	0, 5	5	-1.6	-4	—	
XTAL	I_{OH}	4.6	0	5	-0.1	-0.2	—	
Output Voltage Low-Level	V_{OL}	—	0, 5	5	—	0	0.1	V
Output Voltage High Level	V_{OH}	—	0, 5	5	4.9	5	—	
Input Low Voltage (BUS 0 — BUS 7, \overline{ME})	V_{IL}	0.5, 4.5	—	5	—	—	1.5	
Input High Voltage (BUS 0 — BUS 7, \overline{ME})	V_{IH}	0.5, 4.5	—	5	3.5	—	—	
Schmitt Trigger Input Voltage (Except BUS 0 — BUS 7, \overline{ME})								
Positive Trigger Threshold	V_P				2.2	2.9	3.6	
Negative Trigger Threshold	V_N	0.5, 4.5	—	5	0.9	1.9	2.8	
Hysteresis	V_H				0.3	0.9	1.6	
Input Leakage Current	I_{IN}	—	0.5	5	—	± 0.1	± 5	μA
3-State Output Leakage Current	I_{OUT}	0, 5	0, 5	5	—	± 0.2	± 5	
Input Capacitance	C_{IN}	—	—	—	—	5	7.5	pF
Output Capacitance	C_{OUT}	—	—	—	—	10	15	
Total Power Dissipation (f=5 MHz)								
Idle "00" at M(0000), $CL = 50$ pF		—	—	5	—	1.5	3	mW
Minimum Data Retention Voltage	V_{DR}	$V_{DD} = V_{DR}$			—	2	2.4	V
Data Retention Current	I_{DR}	$V_{DD} = 2.4$			—	25	100	μA

*Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .

OPERATING AND HANDLING CONSIDERATIONS

1. Handling

All inputs and outputs of RCA CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in ICAN-6525 "Guide to Better Handling and Operation of CMOS Integrated Circuits."

2. Operating

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause $V_{DD} - V_{SS}$ to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{CC} nor less than V_{SS} . Input currents must not exceed 10 mA even when the power supply is off.

Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{CC} or V_{SS} , whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} , V_{CC} , or V_{SS} may damage CMOS devices by exceeding the maximum device dissipation.

RCA CMOS LSI Products
CDP1805AC, CDP1806AC

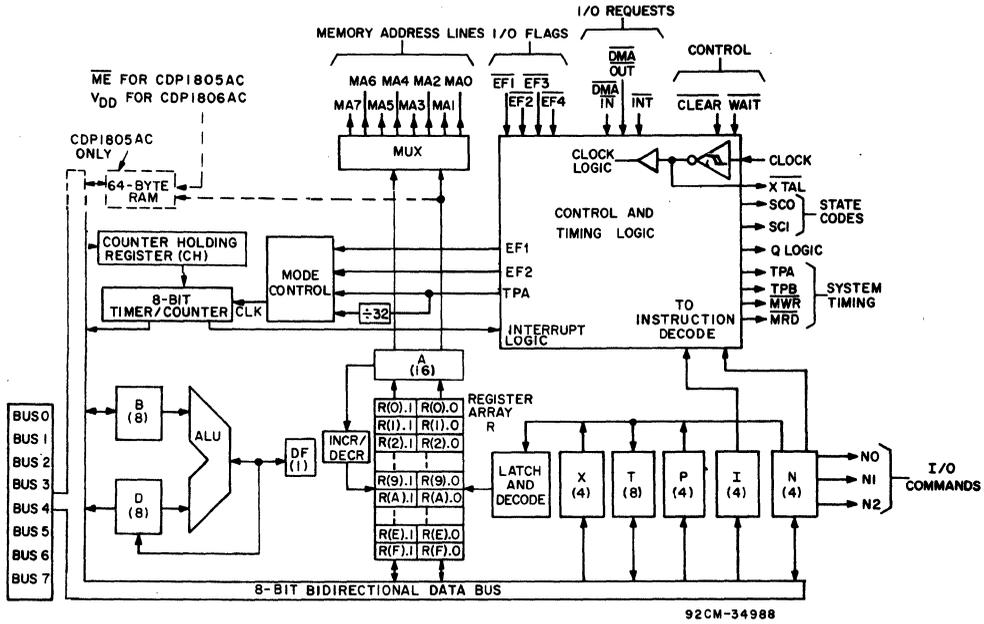
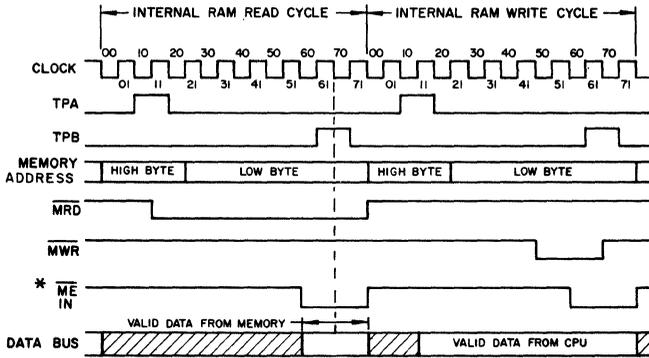


Fig. 2 - Block diagram for CDP1805AC and CDP1806AC.

TIMING WAVEFORMS FOR POSSIBLE OPERATING MODES



*NOTE
 ME HAS A MINIMUM SETUP AND HOLD TIME WITH RESPECT TO THE BEGINNING OF CLOCK 70 FOR A MEMORY READ OPERATION. RAM DATA WILL APPEAR ON THE DATA BUS DURING THE TIME ME IS ACTIVE. THE TIME SHOWN CAN BE LONGER, IF FOR INSTANCE, A DMA OUT OPERATION IS PERFORMED ON INTERNAL RAM DATA, TO ALLOW DATA ENOUGH TIME TO BE LATCHED INTO AN EXTERNAL DEVICE. THE INTERNAL RAM IS AUTOMATICALLY DESELECTED AT THE END OF CLOCK 71, INDEPENDENT OF ME.

* FOR CDP1805AC ONLY

Fig. 3 - Internal memory operation timing waveforms for CDP1805AC and CDP1806AC.

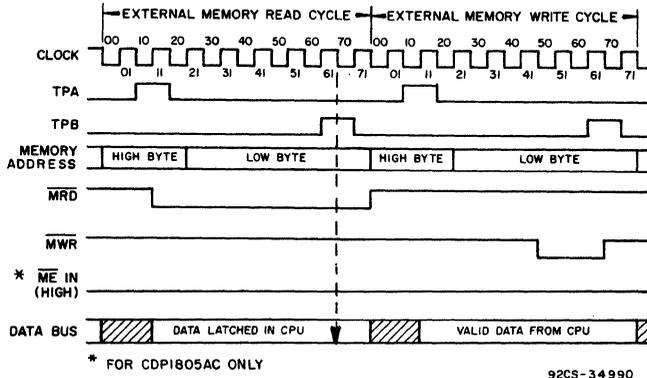


Fig. 4 - External memory operation timing waveforms for CDP1805AC and CDP1806AC.

ENHANCED CDP1805AC and CDP1806AC OPERATION

TIMING

Timing for the CDP1805AC and CDP1806AC is the same as the CDP1802 microprocessor series, with the following exceptions:

- 4.5 clock cycles are provided for memory access instead of 5.
- Q changes 1/2 clock cycle earlier during the SEQ and REQ instructions.
- Flag lines ($\overline{EF1}$ - $\overline{EF4}$) are sampled at the end of the S0 cycle instead of at the beginning of the S1 cycle.
- Pause can only occur on the low-to-high transition of either TPA or TPB, instead of any negative clock transition.

SPECIAL FEATURES

Schmitt triggers are provided on all control inputs, except

\overline{ME} , for maximum immunity from noise and slow signal transitions. A Schmitt trigger in the oscillator section allows operation with an RC or crystal.

The CDP1802-series LOAD mode is not retained. This mode (\overline{WAIT} , $CLEAR=0$) is not allowed on the CDP1805AC and CDP1806AC.

A low power mode is provided, which is initiated via the IDLE instruction. In this mode all external signals, except the oscillator, are stopped on the low-to-high transition of TPB. All outputs remain in their previous states, \overline{MRD} is set to a logic "1", and the data bus floats. The IDLE mode is exited by a DMA or INT condition. The INT includes both external interrupts and interrupts generated by the timer/counter. The only restrictions are that the Timer mode, which uses the $TPA \div 32$ clock source, and the underflow condition at the Pulse Width Measurement modes are not available to exit the IDLE mode.

SIGNAL DESCRIPTIONS

BUS 0 to BUS 7 (Data Bus):

8-bit bidirectional DATA BUS lines. These lines are used for transferring data between the memory, the microprocessor, and I/O devices.

N0 to N2 (I/O) Lines:

Activated by an I/O instruction to signal the I/O control logic of a data transfer between memory and I/O interface. These lines can be used to issue command codes or device

selection codes to the I/O devices. The N bits are low at all times except when an I/O instruction is being executed. During this time their state is the same as the corresponding bits in the N register. The direction of data flow is defined in the I/O instruction by bit N3 (internally) and is indicated by the level of the \overline{MRD} signal:

- $\overline{MRD} = V_{DD}$: Data from I/O to CPU and Memory
- $\overline{MRD} = V_{SS}$: Data from Memory to I/O

SIGNAL DESCRIPTIONS (Cont'd)

EF1 to EF4 (4 Flags):

These inputs enable the I/O controllers to transfer status information to the processor. The levels can be tested by the conditional branch instructions. They can be used in conjunction with the INTERRUPT request line to establish interrupt priorities. The flag(s) are sampled at the end of every S0 cycle. One additional use for EF1 and EF2 is event counting and pulse-width measurement in conjunction with the Timer/Counter.

INTERRUPT, DMA-IN, DMA-OUT (3 I/O Requests)

These inputs are sampled by the CDP1805AC and CDP1806AC during TPB.

Interrupt Action: X and P are stored in T after executing current instruction; designator X is set to 2; designator P is set to 1; interrupt enable is reset to 0 (inhibit); and instruction execution is resumed. The interrupt action requires one machine cycle (S3).

DMA Action: Finish executing current instruction; R(0) points to memory area for data transfer; data is loaded into or read out of memory; and increment R(0).

Note: In the event of concurrent DMA and INTERRUPT requests, DMA-IN has priority followed by DMA-OUT and then INTERRUPT.

SC0, SC1, (2 State Code Lines):

These outputs indicate that the CPU is: 1) fetching an instruction, or 2) executing an instruction, or 3) processing a DMA request, or 4) acknowledging an interrupt request. The levels of state code are tabulated below. All states are valid at TPA.

State Type	State Code Lines	
	SC1	SC0
S0 (Fetch)	L	L
S1 (Execute)	L	H
S2 (DMA)	H	L
S3 (Interrupt)	H	H

H = V_{DD}, L = V_{SS}.

TPA, TPB (2 Timing Pulses):

Positive pulses that occur once in each machine cycle (TPB follows TPA). They are used by I/O controllers to interpret codes and to time interaction with the data bus. The trailing edge of TPA is used by the memory system to latch the high-order byte of the 16-bit memory address.

MA0 to MA7 (8 Memory Address Lines):

In each cycle, the higher-order byte of a 16-bit memory address appears on the memory address lines MA0-7 first. Those bits required by the memory system can be strobed into external address latches by timing pulse TPA. The low-order byte of the 16-bit address appears on the address lines 1/2 clock after the termination of TPA.

MWR (Write Pulse):

A negative pulse appearing in a memory-write cycle, after the address lines have stabilized.

MRD (Read Level):

A low level on MRD indicates a memory read cycle. It can be used to control three-state outputs from the addressed memory and to indicate the direction of data transfer during an I/O instruction.

Q:

Single bit output from the CPU which can be set or reset, between the trailing edge of TPA and the leading edge of TPB, under program control. The Enable Toggle Q command connects the Q-line flip-flop to the output of the counter, such that each time the counter decrements from 01 to its next value, the Q line changes state. This command is cleared by a LOAD COUNTER (LDC) instruction, a CPU reset, or a BRANCH COUNTER INTERRUPT (BCI) instruction with the counter interrupt flip-flop set.

CLOCK:

Input for externally generated single-phase clock. The maximum clock frequency is 5 MHz at V_{DD} = 5 V. The clock is counted down internally to 8 clock pulses per machine cycle.

XTAL:

Connection to be used with clock input terminal, for an external crystal, if the on-chip oscillator is utilized.

WAIT, CLEAR (2 Control Lines):

Provide four control modes as listed in the following truth table:

CLEAR	WAIT	MODE
L	L	NOT ALLOWED
L	H	RESET
H	L	PAUSE
H	H	RUN

ME (Memory Enable CDP1805AC Only):

This active low signal line is used to select or deselect the internal RAM. It must be active prior to clock 70 for an internal RAM access to take place. Internal RAM data will appear on the data bus during the time that ME is active (after clock 31). Thus, if this data is to be latched into an external device (i.e., during an OUTPUT instruction or DMA OUT cycle), ME should be wide enough to provide enough time for valid data to be latched.

The internal RAM is not internally mask-decoded. Decoding of the starting address is performed externally, and may reside in any 64-byte block of memory.

V_{DD} (CDP1806AC Only):

This input replaces the ME signal of the CDP1805AC and must be connected to the positive power supply.

V_{DD}, V_{SS}, (Power Levels):

V_{SS} is the most negative supply voltage terminal and is normally connected to ground. V_{DD} is the positive supply voltage terminal. All outputs swing from V_{SS} to V_{DD}. The recommended input voltage swing is from V_{SS} to V_{DD}.

ARCHITECTURE

Fig. 2 shows a block diagram of the CDP1805AC and CDP1806AC. The principal feature of this system is a register array (R) consisting of sixteen 16-bit scratchpad registers. Individual registers in the array (R) are designated (selected) by a 4-bit binary code from one of the 4-bit registers labeled N, P, and X. The contents of any register can be directed to any one of the following three paths:

1. the external memory (multiplexed, higher-order byte first on to 8 memory address lines)
2. the D register (either of the two bytes can be gated to D)
3. the increment/decrement circuit where it is increased or decreased by one and stored back in the selected 16-bit register.

The three paths, depending on the nature of the instruction, may operate independently or in various combinations in the same machine cycle.

Most instructions consist of two 8-clock-pulse machine cycles. The first cycle is the fetch cycle, and the second —and more if necessary — are execute cycles. During the fetch cycle the four bits in the P designator select one of the 16 registers R(P) as the current program counter. The selected register R(P) contains the address of the memory location from which the instruction is to be fetched. When the instruction is read out from the memory, the higher-order 4 bits of the instruction byte are loaded into the I register and the lower-order 4 bits into the N register. The content of the program counter is automatically incremented by one so that R(P) is now "pointing" to the next byte in the memory.

The X designator selects one of the 16 registers R(X) to "point" to the memory for an operand (or data) in certain ALU or I/O operations.

The N designator can perform the following five functions depending on the type of instruction fetched:

1. designate one of the 16 registers in R to be acted upon during register operations
2. indicate to the I/O devices a command code or device-selection code for peripherals
3. indicate the specific operation to be executed during the ALU instructions, types of tests to be performed during the Branch instructions, or the specific operation required in a class of miscellaneous instructions
4. indicate the value to be loaded into P to designate a new register to be used as the program counter R(P)
5. indicate the value to be loaded into X to designate a new register to be used as data pointer R(X).

The registers in R can be assigned by a programmer in three different ways as program counters, as data pointers, or as scratchpad locations (data registers) to hold two bytes of data.

Program Counters

Any register can be the main program counter; the address of the selected register is held in the P designator. Other registers in R can be used as subroutine program counters. By a single instruction the contents of the P register can be changed to effect a "call" to subroutine. When interrupts are being serviced, register R(1) is used as the program

counter for the user's interrupt servicing routine. After reset, and during a DMA operation, R(0) is used as the program counter. At all other times the register designated as program counter is at the discretion of the user.

Data Pointers

The registers in R may be used as data pointers to indicate a location in memory. The register designated by X (i.e., R(X)) points to memory for the following instructions (see Table I):

1. ALU operations
2. output instructions
3. input instructions
4. register — memory transfer
5. interrupt and subroutine handling.

The register designated by N (i.e., R(N)) points to memory for the "load D from memory" instructions 0N and 4N and the "Store D" instruction 5N. The register designated by P (i.e., the program counter) is used as the data pointer for ALU instructions F8-FD, FF, 7C, 7D, 7F, and the RLDI instruction 68CN. During these instruction executions, the operation is referred to as "data immediate".

Another important use of R as a data pointer supports the built-in Direct-Memory-Access (DMA) function. When a DMA-In or DMA-Out request is received, one machine cycle is "stolen". This operation occurs at the end of the execute machine cycle in the current instruction. Register R(0) is always used as the data pointer during the DMA operation. The data is read from (DMA-Out) or written into (DMA-In) the memory location pointed to by the R(0) register. At the end of the transfer, R(0) is incremented by one so that the processor is ready to act upon the next DMA byte transfer request. This feature in the CDP1805AC and CDP1806AC architecture saves a substantial amount of logic when fast exchanges of blocks of data are required, such as with magnetic discs or during CRT-display-refresh cycles.

Data Registers

When registers in R are used to store bytes of data, instructions are provided which allow D to receive from or write into either the higher-order- or lower-order-byte portions of the register designated by N. By this mechanism (together with loading by data immediate) program pointer and data pointer designations are initialized. Also, this technique allows scratchpad registers in R to be used to hold general data. By employing increment or decrement instructions, such registers may be used as loop counters. The new RLDI, RLXA, RSXD, and RNX instructions also allow loading, storing, and exchanging the full 16-bit contents of the R registers. The new DBNZ instruction allows decrementing and branching-on-not-zero of any 16-bit R register without affecting the D register.

The Q Flip-Flop

An internal flip-flop, Q, can be set or reset by instruction and can be sensed by conditional branch instructions. It can also be driven by the output of the timer/counter. The output of Q is also available as a microprocessor output.

ARCHITECTURE (Cont'd)

Register Summary

D	8 Bits	Data Register (Accumulator)
DF	1 Bit	Data Flag (ALU Carry)
B	8 Bits	Auxiliary Holding Register
R	16 Bits	1 of 16 Scratchpad Registers
P	4 Bits	Designates which Register is Program Counter
X	4 Bits	Designates which Register is Data Pointer
N	4 Bits	Holds Low-Order Instr. Digit
I	4 Bits	Holds High-Order Instr. Digit
T	8 Bits	Holds old X, P after Interrupt (X is high nibble)
Q	1 Bit	Output Flip-Flop
CH	8 Bits	Holds Counter Jam Value
MIE	1 Bit	Master Interrupt Enable
CIE	1 Bit	Counter Interrupt Enable
XIE	1 Bit	External Interrupt Enable
CIL	1 Bit	Counter Interrupt Latch

Interrupt Servicing

Register R(1) is always used as the program counter whenever interrupt servicing is initialized. When an interrupt request occurs and the interrupt is allowed by the program (again, nothing takes place until the completion of the current instruction), the contents of the X and P registers are stored in the temporary register T, and X and P are set to new values; hex digit 2 in X and hex digit 1 in P. Master Interrupt Enable is automatically deactivated to inhibit further interrupts. The user's interrupt routine is now in control; the contents of T may be saved by means of a single SAV instruction (78) in the memory location pointed to by R(X) or the contents of T, D, and DF may be saved using a single DSAV instruction (6876). At the conclusion of the interrupt, the user's routine may restore the pre-interrupted value of X and P with either a RET instruction (70) which permits further interrupts, or a DIS instruction (71), which disables further interrupts.

Interrupt Generation and Arbitration (See Fig. 5)

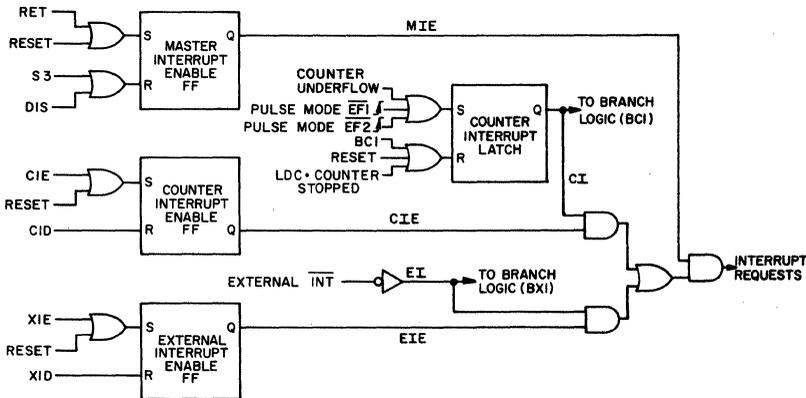
Interrupt requests can be generated from the following sources:

1. Externally through the interrupt input (Request not latched)
2. Internally due to timer/counter response (Request is latched)
 - a. On the transition from count (01)₁₆ to its next value (counter underflow)
 - b. On the transition of $\overline{EF1}$ in pulse measurement mode 1
 - c. On the transition of $\overline{EF2}$ in pulse measurement mode 2

For an interrupt to be serviced by the CPU, the appropriate Interrupt Enable flip-flops must be set. Thus, the External Interrupt Enable flip-flop must be set to service an external interrupt request, and the Counter Interrupt Enable flip-flop must be set to service an internal timer/counter interrupt request. In addition, the Master Interrupt Enable flip-flop (as used in the CDP1802) must be set to service either type of request. All 3 flip-flops are initially enabled with the application of a hardware reset, and, can be selectively enabled or disabled with software: CIE, CID instructions for the CIE flip-flop; XIE, XID instructions for the XIE flip-flop; RET, DIS instructions for the MIE flip-flop.

Short branch instructions on Counter Interrupt (BCI) and External Interrupt (BXI) can be placed in the user's interrupt service routine to provide a means of identifying and prioritizing the interrupt source. Note, however, that since the External Interrupt request is not latched, it must remain active until the short branch is executed if this priority arbitration scheme is used.

Interrupt requests can also be polled if automatic interrupt service is not desired (MIE=0). With the Counter Interrupt and External Interrupt short branch instructions, the branch will be taken if an interrupt request is pending, regardless of the state of any of the 3 Interrupt Enable flip-flops. The latched counter interrupt request signal will be reset when the branch is taken, when the CPU is reset, or with a LDC instruction with the Counter stopped.



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Fig. 5 - Interrupt logic-control diagram for CDP1805AC and CDP1806AC.

ARCHITECTURE (Cont'd)

Timer/Counter and Controls (see Fig. 6)

This logic consists of a presettable 8-bit down-counter (Modulo N type), and a conditional divide-by-32 prescaler. After counting down to (01)₁₆ the counter returns to its initial value at the next count and sets the Counter Interrupt Latch. It will continue decrementing on subsequent counts. If the counter is preset to (00)₁₆ a full 256 counts will occur.

During a Load Counter instruction (LDC) if the counter was stopped with a STPC instruction, the counter and its holding register (CH) are loaded with the value in the D register and any previous counter interrupt is cleared. If the LDC is executed when the counter is running, the contents of the D register are loaded into the holding register (CH) only and any previous counter interrupt is not cleared. After counting down to (01)₁₆ the next count will load the new initial value into the counter, set the Counter Interrupt Latch, and operation will continue.

The timer/counter has the following five programmable modes:

1. Event Counter 1: Input to counter is connected to the $\overline{EF1}$ terminal. The high-to-low transition decrements the counter.
2. Event Counter 2: Input to counter is connected to the $\overline{EF2}$ terminal. The high-to-low transition decrements the counter.
3. Timer: Input to counter is from the divide-by-32 prescaler clocked by TPA. The prescaler is decremented on the low-to-high transition of TPA. The divide-by-32 prescaler is reset when the counter is in a mode other than the Timer mode or stopped by a STPC.
4. Pulse Duration Measurement 1: Input to counter connected to TPA. Each low-to-high transition of TPA

decrements the counter if the input signal at $\overline{EF1}$ terminal (gate input) is low. On the transition of $\overline{EF1}$ to the positive state, the count is stopped, the mode is cleared, and the interrupt request latched. If the counter underflows while the input is low, interrupt will also be set, but counting will continue.

5. Pulse Duration Measurement 2: Operation is identical to Pulse Duration Measurement 1, except $\overline{EF2}$ is used as the gate input.

The modes can be changed without affecting the stored count.

Those modes which use $\overline{EF1}$ and $\overline{EF2}$ terminals as inputs do not exclude testing these flags for branch instructions.

The Stop Counter (STPC) instruction clears the counter mode and stops counting. The STPC instruction should be executed prior to a GEC instruction, if the counter is in the Event Counter Mode 1 or 2.

In addition to the five programmable modes, the Decrement Counter instruction (DTC) enables the user to count in software. In order to avoid conflict with counting done in the other modes, the instruction should be used only after the mode has been cleared by a Stop Counter instruction.

The Enable Toggle Q instruction (ETQ) connects the Q-line flip-flop to the output of the counter, such that each time the counter decrements from 01 to its next value, the Q output changes state. This action is independent of the counter mode and the Interrupt Enable flip-flops. The Enable Toggle Q condition is cleared by an LDC when the timer/counter stopped, system Reset, or a BCI with CI=1.

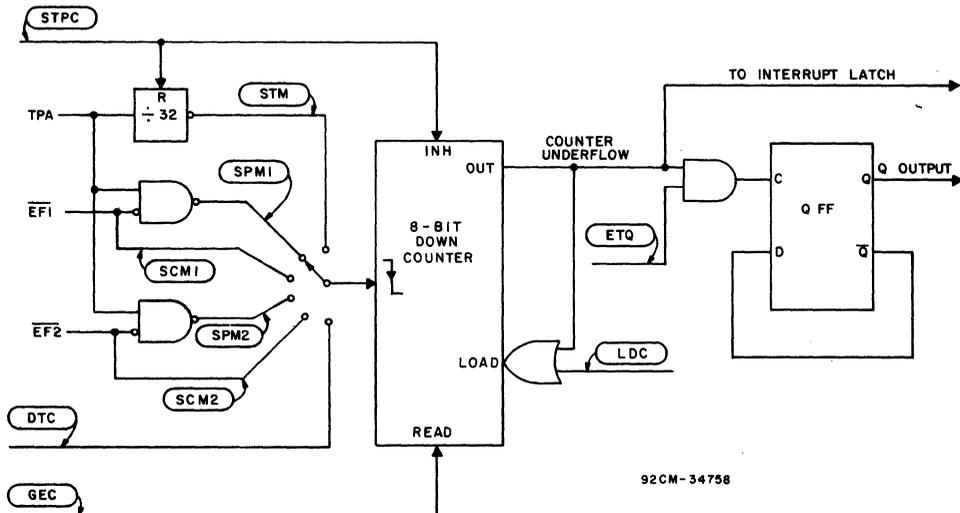


Fig. 6 - Timer/Counter diagram for CDP1805AC and CDP1806AC.

ARCHITECTURE (Cont'd)

On-Board Clock (see Fig. 7 and 8)

Clock circuits may use either an external crystal or an RC network.

The crystal is connected between terminals 1 and 39 (CLOCK and XTAL) in parallel with a resistance (1 megohm typ.).

Frequency trimming capacitors may be required at terminals 1 and 39. For additional information on crystal oscillators, see ICAN-6565. Because of the Schmitt Trigger input, an RC oscillator can be used as shown in Fig. 7. The frequency is approximately 1/RC (see Fig. 8).

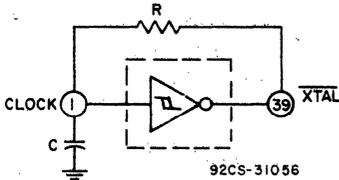


Fig. 7 - RC network for oscillator.

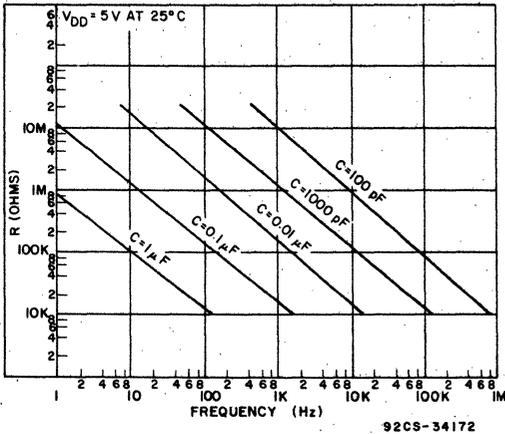


Fig. 8 - Nominal component values as a function of frequency for the RC oscillator.

CONTROL MODES

CLEAR	WAIT	MODE
L	L	NOT ALLOWED
L	H	RESET
H	L	PAUSE
H	H	RUN

The function of the modes are defined as follows:

RESET

Registers I, N, Q, counter prescaler, and Counter Interrupt Latch are reset. XIE and CIE are set and 0's (V_{SS}) are placed on the data bus. TPA and TPB are suppressed while reset is

held and the CPU is placed in S1. The state of the timer/counter is unaffected by the RESET operation.

The first machine cycle after termination of reset is an initialization cycle which requires 9 clock pulses. During this cycle the CPU remains in S1, X, P-T, and then registers X, P, and R(0) are reset and MIE is set. Interrupt and DMA servicing are suppressed during the initialization cycle. The next cycle is an S0 or an S2 but never an S1 or S3. The use of a 71 instruction, followed by 00 at memory locations 0000 and 0001, may be used to reset MIE, so as to preclude interrupts until ready for them. Power-up reset/run can be realized by connecting an RC network to CLEAR (see Fig. 9).

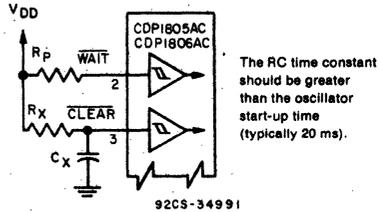


Fig. 9 - Reset/run diagram.

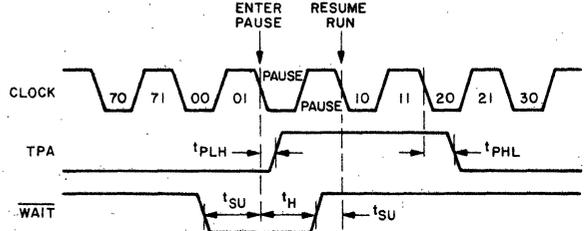
PAUSE

Stops the internal CPU timing generator, freezing the state of the processor. Pause can occur at two points in a machine cycle, on the low-to-high transition of either TPA or TPB.

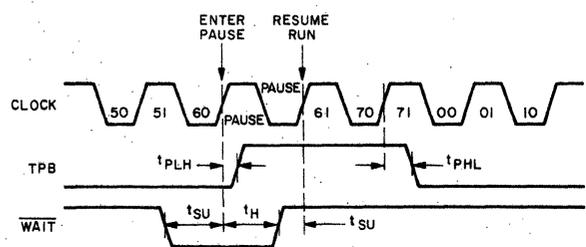
The oscillator continues to run but subsequent clock transitions are ignored. TPA and TPB remain at their previous state (see Fig. 10).

If Pause is entered while in the event counter mode, the appropriate Flag transitions will continue to decrement the counter.

TPA PAUSE TIMING



TPB PAUSE TIMING



NOTE: PAUSE (IN CLOCK WAVEFORM) WHILE REPRESENTED HERE AS ONE CLOCK CYCLE IN DURATION, COULD BE INFINITELY LONG.

Fig. 10 - Pause mode timing waveforms.

ARCHITECTURE (Cont'd)

CONTROL MODES (Cont'd)

RUN

May be initiated from the Pause or Reset mode functions. If initiated from Pause, the CPU resumes operation at the point it left off. If paused at TPA, it will resume on the next high-to-low clock transition, while if paused at TPB, it will resume on the next low-to-high clock transition (see Fig. 9). When initiated from the Reset operation, the first machine cycle following Reset is always the initialization cycle. The

initialization cycle is then followed by a DMA (S2) cycle or fetch (S0) from location 0000 in memory.

SCHMITT TRIGGER INPUTS

All inputs except BUS 0—BUS 7 and \overline{ME} contain a Schmitt Trigger circuit, which is especially useful on the **CLEAR** input as a power-up RESET (see Fig. 9) and the **CLOCK** input (see Fig. 7).

STATE TRANSITIONS

The CDP1805AC and CDP1806AC state transitions are shown in Fig. 11. Each machine cycle requires the same

period of time, 8 clock pulses, except the initialization cycle (INIT) which requires 9 clock pulses.

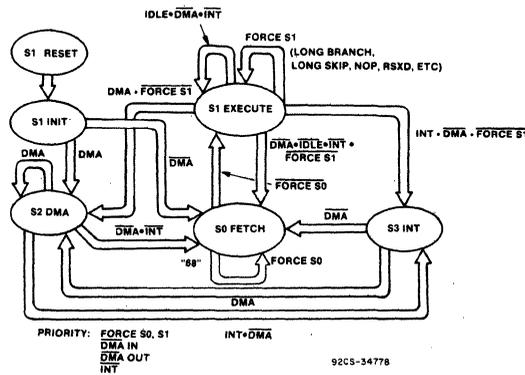


Fig. 11 - State transition diagram.

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INSTRUCTION SET

The CDP1805AC and CDP1806AC instruction summary is given in Table I. Hexadecimal notation is used to refer to the 4-bit binary codes.

In all registers bits are numbered from the least significant bit (LSB) to the most significant bit (MSB) starting with 0.

R(W): Register designated by W, where W=N or X, or P

R(W).0: Lower-order byte of R(W)
R(W).1: Higher-order byte of R(W)
Operation Notation

$M(R(N)) \rightarrow D; R(N) + 1 \rightarrow R(N)$

This notation means: The memory byte pointed to by R(N) is loaded into D, and R(N) is incremented by 1.

TABLE I — INSTRUCTION SUMMARY (For Notes, see also page 17)

INSTRUCTION	NO. OF MACHINE CYCLES	MNEMONIC	OP CODE	OPERATION
MEMORY REFERENCE				
LOAD IMMEDIATE	2	LDI	F8	$M(R(P)) \rightarrow D; R(P)+1 \rightarrow R(P)$
REGISTER LOAD IMMEDIATE	5	RLDI	68CN [■]	$M(R(P)) \rightarrow R(N).1; M(R(P))+1 \rightarrow R(N).0; R(P)+2 \rightarrow R(P)$
LOAD VIA N	2	LDN	0N	$M(R(N)) \rightarrow D; \text{FOR } N \text{ NOT } 0$
LOAD ADVANCE	2	LDA	4N	$M(R(N)) \rightarrow D; R(N)+1 \rightarrow R(N)$
LOAD VIA X	2	LDX	F0	$M(R(X)) \rightarrow D$
LOAD VIA X AND ADVANCE	2	LDXA	72	$M(R(X)) \rightarrow D; R(X)+1 \rightarrow R(X)$
REGISTER LOAD VIA X AND ADVANCE	5	RLXA	686N [■]	$M(R(X)) \rightarrow R(N).1; M(R(X))+1 \rightarrow R(N).0; R(X)+2 \rightarrow R(X)$
STORE VIA N	2	STR	5N	$D \rightarrow M(R(N))$
STORE VIA X AND DECREMENT	2	STXD	73	$D \rightarrow M(R(X)); R(X)-1 \rightarrow R(X)$
REGISTER STORE VIA X AND DECREMENT	5	RSXD	68AN [■]	$R(N).0 \rightarrow M(R(X)); R(N).1 \rightarrow M(R(X)-1); R(X)-2 \rightarrow R(X)$
REGISTER OPERATIONS				
INCREMENT REG N	2	INC	1N	$R(N)+1 \rightarrow R(N)$
DECREMENT REG N	2	DEC	2N	$R(N)-1 \rightarrow R(N)$
DECREMENT REG N AND LONG BRANCH IF NOT EQUAL 0	5	DBNZ	682N	$R(N)-1 \rightarrow R(N); \text{IF } R(N) \text{ NOT } 0, M(R(P)) \rightarrow R(P).1, M(R(P))+1 \rightarrow R(P).0, \text{ELSE } R(P)+2 \rightarrow R(P)$
INCREMENT REG X	2	IRX	60	$R(X)+1 \rightarrow R(X)$
GET LOW REG N	2	GLO	8N	$R(N).0 \rightarrow D$
PUT LOW REG N	2	PLO	AN	$D \rightarrow R(N).0$
GET HIGH REG N	2	GHI	9N	$R(N).1 \rightarrow D$
PUT HIGH REG N	2	PHI	BN	$D \rightarrow R(N).1$
REGISTER N TO REGISTER X COPY	4	RNX	68BN [■]	$R(N) \rightarrow R(X)$
LOGIC OPERATIONS (Note 5)				
OR	2	OR	F1	$M(R(X)) \text{ OR } D \rightarrow D$
OR IMMEDIATE	2	ORI	F9	$M(R(P)) \text{ OR } D \rightarrow D; R(P)+1 \rightarrow R(P)$
EXCLUSIVE OR	2	XOR	F3	$M(R(X)) \text{ XOR } D \rightarrow D$
EXCLUSIVE OR IMMEDIATE	2	XRI	FB	$M(R(P)) \text{ XOR } D \rightarrow D; R(P)+1 \rightarrow R(P)$
AND	2	AND	F2	$M(R(X)) \text{ AND } D \rightarrow D$
AND IMMEDIATE	2	ANI	FA	$M(R(P)) \text{ AND } D \rightarrow D; R(P)+1 \rightarrow R(P)$
SHIFT RIGHT	2	SHR	F6	SHIFT D RIGHT, $LSB(D) \rightarrow DF, 0 \rightarrow MSB(D)$
SHIFT RIGHT WITH CARRY	2	SHRC	76 [▲]	SHIFT D RIGHT, $LSB(D) \rightarrow DF, DF \rightarrow MSB(D)$
RING SHIFT RIGHT	2	RSHR		
SHIFT LEFT	2	SHL	FE	SHIFT D LEFT, $MSB(D) \rightarrow DF, 0 \rightarrow LSB(D)$

[■]Previous contents of T register are destroyed during instruction execution.

[▲]This instruction is associated with more than one mnemonic. Each mnemonic is individually listed.

Table 1 — INSTRUCTION SUMMARY (Cont'd)

INSTRUCTION	NO. OF MACHINE CYCLES	MNEMONIC	OP CODE	OPERATION
LOGIC OPERATIONS (Note 5) (Cont'd)				
SHIFT LEFT WITH CARRY	2	SHLC	7E [▲]	SHIFT D LEFT, MSB(D)→DF, DF→LSB(D)
RING SHIFT LEFT	2	RSHL		
ARITHMETIC OPERATIONS (Note 5)				
ADD	2	ADD	F4	M(R(X))+D→DF, D
DECIMAL ADD	4	DADD	68F4	M(R(X))+D→DF, D DECIMAL ADJUST→DF, D
ADD IMMEDIATE	2	ADI	FC	M(R(P))+D→DF, D; R(P)+1→R(P)
DECIMAL ADD IMMEDIATE	4	DADI	68FC	M(R(P))+D→DF, D R(P)+1→R(P) DECIMAL ADJUST→DF, D
ADD WITH CARRY	2	ADC	74	M(R(X))+D+DF→DF, D
DECIMAL ADD WITH CARRY	4	DADC	6874	M(R(X))+D+DF→DF, D DECIMAL ADJUST→DF, D
ADD WITH CARRY, IMMEDIATE	2	ADCI	7C	M(R(P))+D+DF→DF, D
DECIMAL ADD WITH CARRY, IMMEDIATE	4	DACI	687C	M(R(P))+D+DF→DF, D R(P)+1→R(P) DECIMAL ADJUST→DF, D
SUBTRACT D	2	SD	F5	M(R(X))-D→DF, D
SUBTRACT D IMMEDIATE	2	SDI	FD	M(R(P))-D→DF, D; R(P)+1→R(P)
SUBTRACT D WITH BORROW	2	SDB	75	M(R(X))-D-(NOT DF)→DF, D
SUBTRACT D WITH BORROW, IMMEDIATE	2	SDBI	7D	M(R(P))-D-(NOT DF)→DF, D; R(P)+1→R(P)
SUBTRACT MEMORY	2	SM	F7	D-M(R(X))→DF, D
DECIMAL SUBTRACT MEMORY	4	DSM	68F7	D-M(R(X))→DF, D DECIMAL ADJUST→DF, D
SUBTRACT MEMORY IMMEDIATE	2	SMI	FF	D-M(R(P))→DF, D; R(P)+1→R(P)
DECIMAL SUBTRACT MEMORY, IMMEDIATE	4	DSMI	68FF	D-M(R(P))→DF, D R(P)+1→R(P) DECIMAL ADJUST→DF, D
SUBTRACT MEMORY WITH BORROW	2	SMB	77	D-M(R(X))-(NOT DF)→DF, D
DECIMAL SUBTRACT MEMORY WITH BORROW	4	DSMB	6877	D-M(R(X))-(NOT DF)→DF, D DECIMAL ADJUST→DF, D
SUBTRACT MEMORY WITH BORROW, IMMEDIATE	2	SMBI	7F	D-M(R(P))-(NOT DF)→DF, D
DECIMAL SUBTRACT MEMORY WITH BORROW, IMMEDIATE	4	DSBI	687F	D-M(R(P))-(NOT DF)→DF, D R(P)+1→R(P) DECIMAL ADJUST→DF, D
BRANCH INSTRUCTIONS — SHORT BRANCH				
SHORT BRANCH	2	BR	30	M(R(P))→R(P).0
NO SHORT BRANCH (SEE SKP)	2	NBR	38 [▲]	R(P)+1→R(P)
SHORT BRANCH IF D = 0	2	BZ	32	IF D = 0, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH IF D NOT 0	2	BNZ	3A	IF D NOT 0, M(R(P))→R(P).0 ELSE R(P)+1→R(P)

[▲]This instruction is associated with more than one mnemonic. Each mnemonic is individually listed.

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Table I — INSTRUCTION SUMMARY (Cont'd)

INSTRUCTION	NO. OF MACHINE CYCLES	MNEMONIC	OP CODE	OPERATION
BRANCH INSTRUCTIONS — SHORT BRANCH (Cont'd)				
SHORT BRANCH IF DF = 1	2	BDF	33A	IF DF = 1, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH IF POS OR ZERO	2	BPZ		
SHORT BRANCH IF EQUAL OR GREATER	2	BGE		
SHORT BRANCH IF DF = 0	2	BNF	3BA	IF D = 0, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH IF MINUS	2	BM		
SHORT BRANCH IF LESS	2	BL		
SHORT BRANCH IF Q = 1	2	BQ	31	IF Q = 1, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH IF Q = 0	2	BNQ	39	IF Q = 0, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH IF EF1 = 1 (EF1 = V _{SS})	2	B1	34	IF EF1 = 1, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH IF EF1 = 0 (EF1 = V _{DD})	2	BN1	3C	IF EF1 = 0, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH IF EF2 = 1 (EF2 = V _{SS})	2	B2	35	IF EF2 = 1, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH IF EF2 = 0 (EF2 = V _{DD})	2	BN2	3D	IF EF2 = 0, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH IF EF3 = 1 (EF3 = V _{SS})	2	B3	36	IF EF3 = 1, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH IF EF3 = 0 (EF3 = V _{DD})	2	BN3	3E	IF EF3 = 0, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH IF EF4 = 1 (EF4 = V _{SS})	2	B4	37	IF EF4 = 1, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH IF EF4 = 0 (EF4 = V _{DD})	2	BN4	3F	IF EF4 = 0, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH ON COUNTER INTERRUPT	3	BCI	683E*	IF CI = 1, M(R(P))→R(P).0; 0→CI ELSE R(P)+1→R(P)
SHORT BRANCH ON EXTERNAL INTERRUPT	3	BXI	683F	IF XI = 1, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
BRANCH INSTRUCTIONS — LONG BRANCH				
LONG BRANCH	3	LBR	C0	M(R(P))→R(P).1, M(R(P)+1)→R(P).0
NO LONG BRANCH (SEE LSKP)	3	NLBR	C8A	R(P)+2→R(P)
LONG BRANCH IF D = 0	3	LBZ	C2	IF D = 0, M(R(P))→R(P).1 M(R(P)+1)→R(P).0 ELSE R(P)+2→R(P)
LONG BRANCH IF D NOT 0	3	LBNZ	CA	IF D NOT 0, M(R(P))→R(P).1 M(R(P)+1)→R(P).0 ELSE R(P)+2→R(P)
LONG BRANCH IF DF = 1	3	LBDF	C3	IF DF = 1, M(R(P))→R(P).1 M(R(P)+1)→R(P).0 ELSE R(P)+2→R(P)
LONG BRANCH IF DF = 0	3	LBNF	CB	IF DF = 0, M(R(P))→R(P).1 M(R(P)+1)→R(P).0 ELSE R(P)+2→R(P)
LONG BRANCH IF Q = 1	3	LBQ	C1	IF Q = 1, M(R(P))→R(P).1 M(R(P)+1)→R(P).0 ELSE R(P)+2→R(P)
LONG BRANCH IF Q = 0	3	LBNQ	C9	IF Q = 0, M(R(P))→R(P).1 M(R(P)+1)→R(P).0 ELSE R(P)+2→R(P)

▲This instruction is associated with more than one mnemonic. Each mnemonic is individually listed.

*ETQ cleared by LDC, reset of CPU, or BCI· (CI = 1).

CI = Counter Interrupt, XI = External Interrupt.

Table I — INSTRUCTION SUMMARY (Cont'd)

INSTRUCTION	NO. OF MACHINE CYCLES	MNEMONIC	OP CODE	OPERATION
SKIP INSTRUCTIONS				
SHORT SKIP (SEE NBR)	2	SKP	38 [▲]	R(P)+1→R(P)
LONG SKIP (SEE NLBR)	3	LSKP	C8 [▲]	R(P)→R(P)
LONG SKIP IF D = 0	3	LSZ	CE	IF D = 0, R(P)+2→R(P) ELSE CONTINUE
LONG SKIP IF D NOT 0	3	LSNZ	C6	IF D NOT 0, R(P)+2→R(P) ELSE CONTINUE
LONG SKIP IF DF = 1	3	LSDF	CF	IF DF = 1, R(P)+2→R(P) ELSE CONTINUE
LONG SKIP IF DF = 0	3	LSNF	C7	IF DF = 0, R(P)+2→R(P) ELSE CONTINUE
LONG SKIP IF Q = 1	3	LSQ	CD	IF Q = 1, R(P)+2→R(P) ELSE CONTINUE
LONG SKIP IF Q = 0	3	LSNQ	C5	IF Q = 0, R(P)+2→R(P) ELSE CONTINUE
LONG SKIP IF IE = 1	3	LSIE	CC	IF IE = 1, R(P)+2→R(P) ELSE CONTINUE
CONTROL INSTRUCTIONS				
IDLE	2	IDL	00 [#]	STOP ON TPB; WAIT FOR DMA OR INTERRUPT; BUS FLOATS
NO OPERATION	3	NOP	C4	CONTINUE
SET P	2	SEP	DN	N→P
SET X	2	SEX	EN	N→X
SET Q	2	SEQ	7B	1→Q
RESET Q	2	REQ	7A	0→Q
PUSH X, P TO STACK	2	MARK	79	(X, P)→T; (X, P)→M(R(2)) THEN P→X; R(2)→1→R(2)
TIMER/COUNTER INSTRUCTIONS				
LOAD COUNTER	3	LDC	6806 [*]	D→COUNTER; 0→CI; (IF COUNTER IS STOPPED)
GET COUNTER	3	GEC	6808	COUNTER→D
STOP COUNTER	3	STPC	6800	STOP COUNTER CLOCK; 0→÷32 PRESCALER
DECREMENT TIMER/COUNTER	3	DTC	6801	COUNTER-1→COUNTER
SET TIMER MODE AND START	3	STM	6807	TPA÷32→COUNTER CLOCK
SET COUNTER MODE 1 AND START	3	SCM1	6805	EF1→COUNTER CLOCK
SET COUNTER MODE 2 AND START	3	SCM2	6803	EF2→COUNTER CLOCK
SET PULSE WIDTH MODE 1 AND START	3	SPM1	6804	TPA.EF1→COUNTER CLOCK; EF1 ✗ STOPS COUNT
SET PULSE WIDTH MODE 2 AND START	3	SPM2	6802	TPA.EF2→COUNTER CLOCK; EF2 ✗ STOPS COUNT
ENABLE TOGGLE Q	3	ETQ	6809 [*]	IF COUNTER = 01 · NEXT COUNTER CLOCK ✗ : Q→Q

[▲]This instruction is associated with more than one mnemonic. Each mnemonic is individually listed.

[#]An IDLE instruction initiates an S1 cycle. All external signals, except the oscillator, are stopped on the low-to-high transition of TPB. All outputs remain in their previous states, MRD is set to a logic '1' and the data bus floats. The processor will continue to IDLE until an I/O request (INTERRUPT, DMA-IN, or DMA-OUT) is activated. When the request is acknowledged, the IDLE cycle is terminated and the I/O request is serviced, and then normal operation is resumed. (To respond to an INTERRUPT during an IDLE, MIE must be enabled.)

^{*}ETQ cleared by LDC, reset of CPU or BCI (CI = 1).

CI = Counter Interrupt, XI = External Interrupt.

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Table I — INSTRUCTION SUMMARY (Cont'd)

INSTRUCTION	NO. OF MACHINE CYCLES	MNEMONIC	OP CODE	OPERATION
INTERRUPT CONTROL				
EXTERNAL INTERRUPT ENABLE	3	XIE	680A	1→XIE
EXTERNAL INTERRUPT DISABLE	3	XID	680B	0→XIE
COUNTER INTERRUPT ENABLE	3	CIE	680C	1→CIE
COUNTER INTERRUPT DISABLE	3	CID	680D	0→CIE
RETURN	2	RET	70	M(R(X))→X, P; R(X)+1→R(X); 1→MIE
DISABLE	2	DIS	71	M(R(X))→X, P; R(X)+1→R(X); 0→MIE
SAVE	2	SAV	78	T→M(R(X))
SAVE T, D, DF	6	DSAV	6876 [■]	R(X)-1→R(X), T→M(R(X)), R(X)-1→R(X), D→M(R(X)), R(X)-1→R(X), SHIFT D RIGHT WITH CARRY, D→M(R(X))
INPUT-OUTPUT BYTE TRANSFER				
OUTPUT 1	2	OUT 1	61	M(R(X))→BUS; R(X)+1→R(X); N LINES = 1
OUTPUT 2	2	OUT 2	62	M(R(X))→BUS; R(X)+1→R(X); N LINES = 2
OUTPUT 3	2	OUT 3	63	M(R(X))→BUS; R(X)+1→R(X); N LINES = 3
OUTPUT 4	2	OUT 4	64	M(R(X))→BUS; R(X)+1→R(X); N LINES = 4
OUTPUT 5	2	OUT 5	65	M(R(X))→BUS; R(X)+1→R(X); N LINES = 5
OUTPUT 6	2	OUT 6	66	M(R(X))→BUS; R(X)+1→R(X); N LINES = 6
OUTPUT 7	2	OUT 7	67	M(R(X))→BUS; R(X)+1→R(X); N LINES = 7
INPUT 1	2	INP 1	69	BUS→M(R(X)); BUS→D; N LINES = 1
INPUT 2	2	INP 2	6A	BUS→M(R(X)); BUS→D; N LINES = 2
INPUT 3	2	INP 3	6B	BUS→M(R(X)); BUS→D; N LINES = 3
INPUT 4	2	INP 4	6C	BUS→M(R(X)); BUS→D; N LINES = 4
INPUT 5	2	INP 5	6D	BUS→M(R(X)); BUS→D; N LINES = 5
INPUT 6	2	INP 6	6E	BUS→M(R(X)); BUS→D; N LINES = 6
INPUT 7	2	INP 7	6F	BUS→M(R(X)); BUS→D; N LINES = 7
CALL AND RETURN				
STANDARD CALL	10	SCAL	688N [■]	R(N).0→M(R(X)); R(N).1→M(R(X)-1); R(X)-2→R(X); R(P)→R(N); THEN M(R(N))→R(P).1; M(R(N)+1)→R(P).0; R(N)+2→R(N)
STANDARD RETURN	8	SRET	689N [■]	R(N)→R(P); M(R(X)+1)→R(N).1; M(R(X)+2)→R(N).0; R(X)+2→R(X)

[■]Previous contents of T register are destroyed during instruction execution.

NOTES FOR TABLE I

1. Long-Branch, Long-Skip and No Op instructions require three cycles to complete (1 fetch + 2 execute).

Long-Branch instructions are three bytes long. The first byte specifies the condition to be tested; and the second and third byte, the branching address.

The long-branch instructions can:

- Branch unconditionally
- Test for $D=0$ or $D\neq 0$
- Test for $DF=0$ or $DF=1$
- Test for $Q=0$ or $Q=1$
- Effect an unconditional no branch

If the tested condition is met, then branching takes place; the branching address bytes are loaded in the high-and-low-order bytes of the current program counter, respectively. This operation effects a branch to any memory location.

If the tested condition is not met, the branching address bytes are skipped over, and the next instruction in sequence is fetched and executed. This operation is taken for the case of unconditional no branch (NLBR).

2. The short-branch instructions are two or three bytes long. The first byte specifies the condition to be tested, and the second specifies the branching address, except for the branches on interrupt. For those, the first two bytes specify the condition to be tested and the third byte specifies the branching address.

The short branch instruction can:

- Branch unconditionally
- Test for $D=0$ or $D\neq 0$
- Test for $DF=0$ or $DF=1$
- Test for $Q=0$ or $Q=1$
- Test the status (1 or 0) of the four EF flags
- Effect an unconditional no branch
- Test for counter or external interrupts (BCI, BXI)

If the tested condition is met, then branching takes place; the branching address byte is loaded into the low-order byte position of the current program counter. This effects a branch within the current 256-byte page of the memory, i.e., the page which holds the branching address. If the tested condition is not met, the branching address byte is skipped over, and the next instruction in sequence is fetched and executed. This same action is taken in the case of unconditional no branch (NBR).

3. The skip instructions are one byte long. There is one Unconditional Short-Skip (SKP) and eight Long-Skip instructions.

The Unconditional Short-Skip instruction takes 2 cycles to complete (1 fetch + 1 execute). Its action is to skip over the byte following it. Then the next instruction in sequence is fetched and executed. This SKP instruction is identical to the unconditional no-branch instruction (NBR) except that the skipped-over byte is not considered part of the program.

The Long-Skip instructions take three cycles to complete (1 fetch + 2 execute).

They can:

- Skip unconditionally
- Test for $D=0$ or $D\neq 0$
- Test for $DF=0$ or $DF=1$
- Test for $Q=0$ or $Q=1$
- Test for $MIE=1$

If the tested condition is met, then Long Skip takes place; the current program counter is incremented twice. Thus two bytes are skipped over and the next instruction in sequence is fetched and executed. If the tested condition is not met, then no action is taken. Execution is continued by fetching the next instruction in sequence.

4. Instruction 6800 through 68FF take a minimum of 3 machine cycles and up to a maximum of 10 machine cycles. In all cases, the first two cycles are fetches and subsequent cycles are executes. The first byte (68) of these two-byte op codes is used to generate the second fetch, the second byte is then interpreted differently than the same code without the 68 prefix. DMA and INT requests are not serviced until the end of the last execute cycle.

5. Arithmetic Operations:

The arithmetic and shift operations are the only instructions that can alter the content of DF. The syntax '(NOT DF)' denotes the subtraction of the borrow.

Binary Operations:

After an ADD instruction —

$DF=1$ denotes a carry has occurred. Result is greater than FF_{16} .

$DF=0$ denotes a carry has not occurred.

After a SUBTRACT instruction —

$DF=1$ denotes no borrow. D is a true positive number.

$DF=0$ denotes a borrow. D is in two's complement form.

Binary Coded Decimal Operations:

After a BCD ADD instruction —

$DF=1$ denotes a carry has occurred. Result is greater than 99_{10} .

$DF=0$ denotes a carry has not occurred.

After a BCD SUBTRACT instruction —

$DF=1$ denotes no borrow. D is a true positive decimal number.

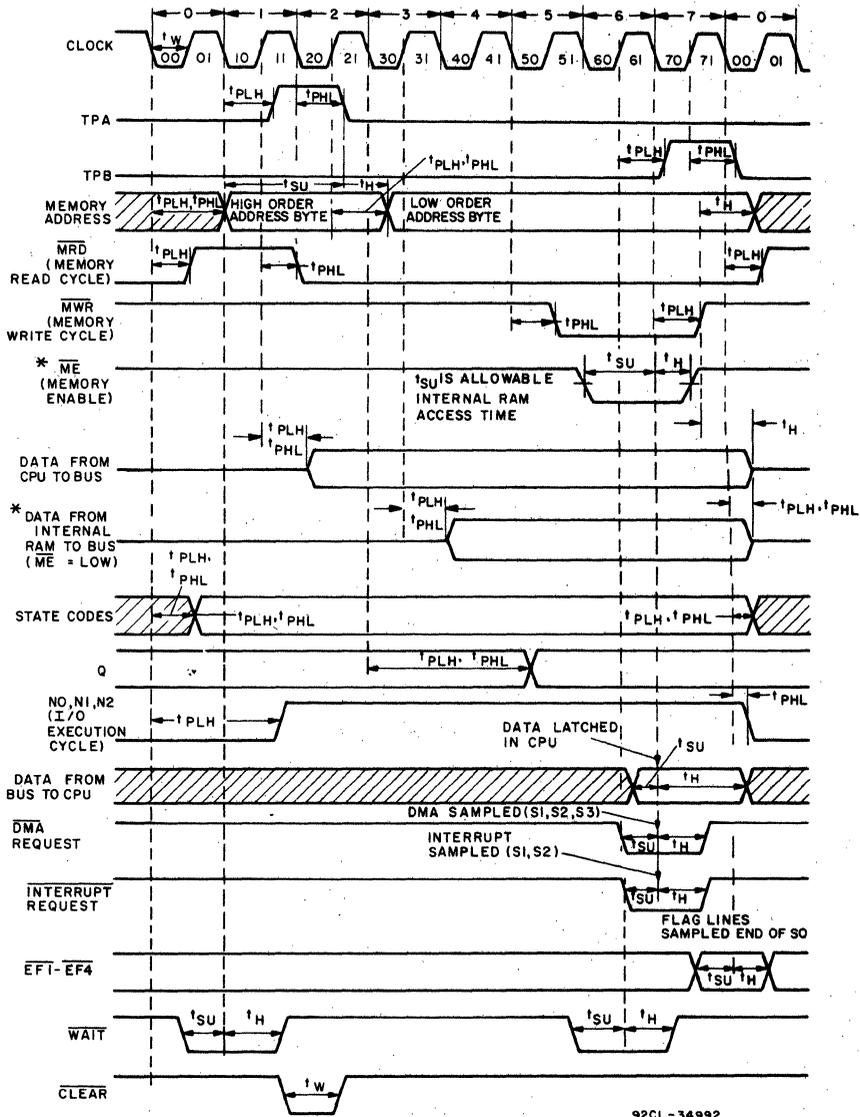
(Example)	99	D	
	-88	M(R(X))	
	11	D	DF=1

$DF=0$ denotes a borrow. D is in ten's complement form.

(Example)	88	D	
	-99	M(R(X))	
	89	D	DF=0

89 is the ten's complement of 11, which is the correct answer (with a minus value denoted by $DF=0$).

RCA CMOS LSI Products
CDP1805AC, CDP1806AC



- NOTES:**
1. THIS TIMING DIAGRAM IS USED TO SHOW SIGNAL RELATIONSHIPS ONLY AND DOES NOT REPRESENT ANY SPECIFIC MACHINE CYCLE.
 2. ALL MEASUREMENTS ARE REFERENCED TO 50% POINT OF THE WAVEFORMS.
 3. SHADED AREAS INDICATED "DON'T CARE" OR UNDEFINED STATE. MULTIPLE TRANSITIONS MAY OCCUR DURING THIS PERIOD.
- * FOR THE CDP1805AC ONLY

Fig. 12 - Objective dynamic timing waveforms for CDP1805AC and CDP1806AC.

1800-Series Microprocessors and Microcomputers

CDP1805AC, CDP1806AC

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $C_L = 50$ pF, $V_{DD} = 5$ V, $\pm 5\%$.

CHARACTERISTIC		LIMITS		UNITS
		CDP1805AC, CDP1806AC		
		Typ.*	Max.	
Propagation Delay Times:				
Clock to TPA, TPB	t_{PLH}, t_{PHL}	150	275	ns
Clock-to-Memory High-Address Byte	t_{PLH}, t_{PHL}	325	550	
Clock-to-Memory Low-Address Byte	t_{PLH}, t_{PHL}	275	450	
Clock to $\overline{\text{MRD}}$	t_{PLH}, t_{PHL}	200	325	
Clock to $\overline{\text{MWR}}$	t_{PLH}, t_{PHL}	150	275	
Clock to (CPU DATA to BUS)	t_{PLH}, t_{PHL}	375	625	
Clock to State Code	t_{PLH}, t_{PHL}	225	400	
Clock to Q	t_{PLH}, t_{PHL}	250	425	
Clock to N	t_{PLH}, t_{PHL}	250	425	
Clock to Internal RAM Data to BUS	t_{PLH}, t_{PHL}	420	650	
Minimum Set Up and Hold Times:■				
Data Bus Input Set-Up	t_{SU}	-100	0	ns
Data Bus Input Hold	t_H	125	225	
$\overline{\text{DMA}}$ Set-Up	t_{SU}	-75	0	
$\overline{\text{DMA}}$ Hold	t_H	100	175	
$\overline{\text{ME}}$ Set-Up	t_{SU}	-25	0	
$\overline{\text{ME}}$ Hold	t_H	90	150	
Interrupt Set-Up	t_{SU}	-100	0	
Interrupt Hold	t_H	100	175	
$\overline{\text{WAIT}}$ Set-Up	t_{SU}	20	50	
$\overline{\text{EF1-4}}$ Set-Up	t_{SU}	-125	0	
$\overline{\text{EF1-4}}$ Hold	t_H	175	300	
Minimum Pulse Width Times:■				
$\overline{\text{CLEAR}}$ Pulse Width	t_{WL}	100	175	ns
$\overline{\text{CLOCK}}$ Pulse Width	t_{WL}	75	125	

*Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .

■Maximum limits of minimum characteristics are the values above which all devices function.

TIMING SPECIFICATIONS as a function of T ($T = 1/f_{\text{clock}}$) at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = 5$ V, $\pm 5\%$.

CHARACTERISTIC		LIMITS		UNITS
		CDP1805AC, CDP1806AC		
		Min.	Typ.*	
High-Order Memory-Address Byte Set-Up to TPA Time	T_{SU}	2T-275	2T-175	ns
High-Order Memory-Address Byte Hold after TPA Time	t_H	T/2-50	T/2-15	
Low-Order Memory-Address Byte Hold after WR Time	t_H	T+0	T+100	
CPU Data to Bus Hold after WR Time	t_H	T-200	T-100	
Required Memory Access Time Address to Data	t_{ACC}	4.5T-400	4.5T-175	

*Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .

RCA CMOS LSI Products

CDP1805AC, CDP1806AC

TABLE II. CONDITIONS ON DATA BUS AND MEMORY ADDRESS LINES DURING ALL MACHINE STATES

STATE	I	N	MNEMONIC	OPERATION	DATA BUS	MEMORY ADDRESS	MRD	MWR	N LINES	
S1	RESET			0→Q,I,N, COUNTER PRESCALER, CIL; 1→CIE, XIE	00	UNDEFINED	1	1	0	
	INITIALIZE NOT PROGRAMMER ACCESSIBLE			X, P→T THEN 0→X, P; 1→MIE, 0000→R0	00 [▲]	UNDEFINED	1	1	0	
S0		FETCH		MRP→1, N; RP+1→RP	MRP	RP	0	1	0	
S1	0	0	IDL	STOP AT TPB WAIT FOR DMA OR INT	FLOAT	RO	1	1	0	
	0	1-F	LDN	MRN→D	MRN	RN	0	1	0	
	1	0-F	INC	RN+1→RN	FLOAT	RN	1	1	0	
	2	0-F	DEC	RN-1→RN	FLOAT	RN	1	1	0	
	3	0-F	SHORT BRANCH	TAKEN: MRP→RP.0 NOT TAKEN: RP+1→RP	MRP	RP	0	1	0	
	4	0-F	LDA	MRN→D; RN+1→RN	MRN	RN	0	1	0	
	5	0-F	STR	D→MRN	D	RN	1	0	0	
	6	0	IRX	RX+1→RX	MRX	RX	1	1	0	
	6	1		OUT 1	MRX→BUS; RX+1→RX	MRX	RX	0	1	1
		2		OUT 2						2
		3		OUT 3						3
		4		OUT 4						4
		5		OUT 5						5
		6		OUT 6						6
		7		OUT 7						7
	9	A		INP 1	BUS→MRX, D	DATA FROM I/O DEVICE	RX	1	0	1
		B		INP 2						2
		C		INP 3						3
		D		INP 4						4
		E		INP 5						5
		F		INP 6						6
			INP 7	7						
7	0		RET	MRX→X,P; RX+1→RX 1→MIE	MRX	RX	0	1	0	
	1		DIS	MRX→X,P; RX+1→RX 0→MIE	MRX	RX	0	1	0	
	2		LDXA	MRX→D; RX+1→RX	MRX	RX	0	1	0	
	3		STXD	D→MRX; RX-1→RX	D	RX	1	0	0	
	4		ADC	MRX+D+DF→DF, D	MRX	RX	0	1	0	
	5		SDB	MRX→D→DFN→DF, D	MRX	RX	0	1	0	
	6		SHRC	LSB(D)→DF; DF→MSB(D)	FLOAT	RX	1	1	0	
	7		SMB	D→MRX→DFN→DF, D	MRX	RX	0	1	0	
	8		SAV	T→MRX	T	RX	1	0	0	
	9		MARK	X,P→T, MR2; P→X R2-1→R2	T	R2	1	0	0	
	A		REQ	0→Q	FLOAT	RP	1	1	0	
	B		SEQ	1→Q	FLOAT	RP	1	1	0	
	C		ADC1	MRP+D+DF→DF, D; RP+1	MRP	RP	0	1	0	
	D		SDB1	MRP-D-DFN→DF, D; RP+1	MRP	RP	0	1	0	
	E		SHLC	MSB(D)→DF; DF→LSB(D)	FLOAT	RP	1	1	0	
	F		SMB1	D-MRP-DFN→DF, D; RP+1	MRP	RP	0	1	0	
	8	0-F	GLO	RN.0→D	RN.0	RN	1	1	0	
9	0-F	GHI	RN.1→D	RN.1	RN	1	1	0		
A	0-F	PLO	D→RN.0	D	RN	1	1	0		
B	0-F	PHI	D→RN.1	D	RN	1	1	0		

▲ = Data bus floats for first 2-1/2 clocks of the 9 clock initialization cycle; all zeros for remainder of cycle.

TABLE II. CONDITIONS ON DATA BUS AND MEMORY ADDRESS LINES DURING ALL MACHINE STATES (Cont'd)

STATE	I	N	MNEMONIC	OPERATION	DATA BUS	MEMORY ADDRESS	MRD	MWR	N LINES		
S1#1	C	0-3, 8-B	LONG BRANCH	TAKEN: MRP→B; RP+1→RP	MRP	RP	0	1	0		
#2				TAKEN: B→RP.1; MRP→RP.0	M(RP+1)	RP+1	0	1	0		
S1#1				NOT TAKEN RP+1→RP	MRP	RP	0	1	0		
#2				NOT TAKEN: RP+1→RP	M(RP+1)	RP+1	0	1	0		
S1#1		5 6 7 C D E F	LONG SKIP	TAKEN: RP+1→RP	MRP	RP	0	1	0		
#2				TAKEN: RP+1→RP	M(RP+1)	RP+1	0	1	0		
S1#1				NOT TAKEN: NO OPERATION	MRP	RP	0	1	0		
#2				NOT TAKEN: NO OPERATION	·M(RP+1)	RP+1	0	1	0		
S1#1				4	NOP	NO OPERATION	MRP	RP	0	1	0
#2						NO OPERATION	M(RP+1)	RP+1	0	1	0
S1		D	0-F	SEP	N→P	NN	RN	1	1	0	
		E	0-F	SEX	N→X	NN	RN	1	1	0	
	F	0	LDX	MRX→D	MRX	RX	0	1	0		
		1	OR	MRX OR D→D	MRX	RX	0	1	0		
		2	AND	MRX AND D→D							
		3	XOR	MRX XOR D→D							
		4	ADD	MRX+D→DF, D							
		5	SD	MRX-D→DF, D							
		7	SM	D-MRX→DF; D							
		6	SHR	LSB(D)→DF; 0→MSB(D)	FLOAT	RX	1	1	0		
		8	LDI	MRP→D; RP+1→RP	MRP	RP	0	1	0		
		9	ORI	MRP OR D→D; RP+1→RP							
	A	ANI	MRP AND D→D; RP+1→RP								
	B	XRI	MRP XOR D→D; RP+1→RP								
C	ADI	MRP+D→DF, D; RP+1→RP									
D	SDI	MRP-D→DF, D; RP+1→RP									
F	SMI	D-MRP→DF, D; RP+1→RP									
E	SHL	MSB(D)→DF; 0→LSB(D)	FLOAT	RP	1	1	0				
S2	DMA IN			BUS→MR0; R0+1→R0	DATA FROM I/O DEVICE	R0	1	0	0		
	DMA OUT			MR0→BUS; R0+1→R0	MR0	R0	0	1	0		
S3	INTERRUPT			X,P→T; 0→MIE 1→P; 2→X	FLOAT	RN	1	1	0		

CDP1805AC, CDP1806AC

TABLE II. CONDITIONS ON DATA BUS AND MEMORY ADDRESS LINES DURING ALL MACHINE STATES (Cont'd)

STATE	I	N	MNEMONIC	OPERATION	DATA BUS	MEMORY ADDRESS	MRD	MWR	N LINES
THE FOLLOWING ARE ALL LINKED INSTRUCTIONS									
"68" PRECEDES ALL THE OP CODES, SO THERE IS A DOUBLE FETCH									
S1	0	0	STPC	STOP COUNTER CLOCK; 0→÷32 PRESCALER	FLOAT	R0	1	1	0
		1	DTC	CNTR→1→CNTR	FLOAT	R1	1	1	0
		2	SPM2	CNTR-1 ON EF2 AND TPA	FLOAT	R2	1	1	0
		3	SCM2	CNTR-1 ON EF2 0 TO 1	FLOAT	R3	1	1	0
		4	SPM1	CNTR-1 ON EF1 AND TPA	FLOAT	R4	1	1	0
		5	SCM1	CNTR-1 ON EF1 0 TO 1	FLOAT	R5	1	1	0
		6	LDC	D→CNTR;0→CIL (IF CNTR IS STOPPED)	D	R6	1	1	0
		7	STM	CNTR-1 ON TPA÷32	FLOAT	R7	1	1	0
		8	GEC	CNTR→D	CNTR	R8	1	1	0
		9	ETQ	IF CNTR THRU 0: Q→Q	FLOAT	R9	1	1	0
		A	XIE	1→XIE	FLOAT	RA	1	1	0
		B	XID	0→XIE	FLOAT	RB	1	1	0
		C	CIE	1→CIE	FLOAT	RC	1	1	0
D	CID	0→CIE	FLOAT	RD	1	1	0		
S1#1	2	0-F	DBNZ	RN-1→RN	FLOAT	RN	1	1	0
#2				MRP→B; RP+1→RP	MRP	RP	0	1	0
#3				TAKEN: B→RP.1; MRP→RP.0 NOT TAKEN: RP+1→RP	M(RP+1)	RP+1	0	1	0
S1	3	E	BCI	TAKEN: MRP→RP.0; 0→CI NOT TAKEN: RP+1→RP	MRP	RP	0	1	0
		F	BXI	TAKEN: MRP→RP.0 NOT TAKEN: RP+1→RP	MRP	RP	0	1	0
S1#1	6	0-F	RLXA	MRX→B, RX+1→RX	MRX	RX	0	1	0
#2				B→T; MRX→B; RX+1→RX	M(RX+1)	RX+1	0	1	0
#3				B, T→RN.0, RN.1	FLOAT	RN	1	1	0
S1#1	7	4	DADC	MRX+D+DF→DF, D	MRX	RX	0	1	0
#2				DECIMAL ADJUST→DF, D	FLOAT	RP	1	1	1
S1#1	7	6	DSAV	RX-1→RX	FLOAT	RX	1	1	0
#2				T→MRX; RX-1→RX	T	RX-1	1	0	0
#3				D→MRX; RX-1→RX SHIFT D RIGHT WITH CARRY	D	RX-2	1	0	0
#4				D→MRX	D	RX-3	1	0	0
S1#1	7	7	DSMB	D→MRX-(NOT DF)→DF, D	MRX	RX	0	1	0
#2				DECIMAL ADJUST→DF, D	FLOAT	RP	1	1	0
S1#1	7	C	DACI	MRP+D+DF→DF, D; RP+1→RP	MRP	RP	0	1	0
#2				DECIMAL ADJUST→DF, D	FLOAT	RP+1	1	1	0
S1#1	7	F	DSBI	D→MRP-(NOT DF)→DF, D; RP+1→RP	MRP	RP	0	1	0
#2				DECIMAL ADJUST→DF, D	FLOAT	RP+1	1	1	0
S1#1	8	0-F	SCAL	RN.0, RN.1→T, B	FLOAT	RN	1	1	0
#2				T→MRX; RX-1→RX	RN.0	RX	1	0	0
#3				B→MRX, RX-1→RX	RN.1	RX-1	1	0	0
#4				RP.0, RP.1→T, B	FLOAT	RP	1	1	0
#5				B, T→RN.1, RN.0	FLOAT	RN	1	1	0
#6				MRN→B; RN+1→RN	MRP	RP	0	1	0
#7				B→T; MRN→B; RN+1→RN	M(RP+1)	RP+1	0	1	0
#8				B, T→RP.0, RP.1	FLOAT	RP	1	1	0

TABLE II. CONDITIONS ON DATA BUS AND MEMORY ADDRESS LINES DURING ALL MACHINE STATES (Cont'd)

STATE	I	N	MNEMONIC	OPERATION	DATA BUS	MEMORY ADDRESS	MRD	MWR	N LINES
THE FOLLOWING ARE ALL LINKED INSTRUCTIONS									
"68" PRECEDES ALL THE OP CODES, SO THERE IS A DOUBLE FETCH									
S1#1	9	0-F	SRET	RN.0, RN.1-T, B	FLOAT	RN	1	1	0
#2				RX+1-RX	FLOAT	RX	1	1	0
#3				B, T-RP.1, RP.0	FLOAT	RP	1	1	0
#4				MRX-B; RX+1-RX	M(RX+1)	RX+1	0	1	0
#5				B-T; MRX-B	M(RX+1)	RX+2	0	1	0
#6				B, T-RN.0, RN.1	FLOAT	RN	1	1	0
S1#1	A	0-F	RSXD	RN.0, RN.1-T, B	FLOAT	RN	1	1	0
#2				T-MRX; RX-1-RX	RN.0	RX	1	0	0
#3				B-MRX; RX-1-RX	RN.1	RX-1	1	0	0
S1#1	B	0-F	RNX	RN.0, RN.1-T, B	FLOAT	RN	1	1	0
#2				B, T-RX.1, RX.0	FLOAT	RX	1	1	0
S1#1	C	0-F	RLDI	MRP-B; RP+1-RP	MRP	RP	0	1	0
#2				B-T; MRP-B; RP+1-RP	M(RP+1)	RP+1	0	1	0
#3				B, T-RN.0, RN.1; RP+1-RP	FLOAT	RN	1	1	0
S1#1	F	4	DADD	MRX+D-DF, D	MRX	RX	0	1	0
#2				DECIMAL ADJUST-DF, D	FLOAT	RP	1	1	0
S1#1	F	7	DSM	D-MRX-DF, D	MRX	RX	0	1	0
#2				DECIMAL ADJUST-DF, D	FLOAT	RP	1	1	0
S1#1	F	C	DADI	MRP+D-DF, D; RP+1-RP	MRP	RP	0	1	0
#2				DECIMAL ADJUST-DF, D	FLOAT	RP+1	1	1	0
S1#1	F	F	DSMI	D-MRP-DF, D	MRP	RP	0	1	0
#2				RP+1-RP	FLOAT	RP+1	1	1	0

Instruction Summary

N

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F		
0	IDL																LDN	
1																	INC	
2																	DEC	
3	BR	BQ	BZ	BDF	B1	B2	B3	B4	SKP	BNQ	BNZ	BNF	BN1	BN2	BN3	BN4		
4																	LDA	
5																	STR	
6	IRX																OUT	
									*								INP	
7	RET	DIS	LDXA	STXD	ADC	SDB	SHRC	SMB	SAV	MARK	REQ	SEQ	ADCI	SDBI	SHLC	SMBI		
8																	GLO	
9																	GHI	
A																	PLO	
B																	PHI	
C	LBR	LBQ	LBZ	LBDF	NOP	LSNQ	LSNZ	LSNF	LSKP	LBNQ	LBNZ	LBNF	LSIE	LSQ	LSZ	LSDF		
D																	SEP	
E																	SEX	
F	LDX	OR	AND	XOR	ADD	SD	SHR	SM	LDI	ORI	ANI	XRI	ADI	SDI	SHL	SMI		
	'68' LINKED OPCODES (DOUBLE FETCH)																	
0	STPC	DTC	SPM2	SCM2	SPM1	SCM1	LDC	STM	GEC	ETQ	XIE	XID	CIE	CID	—	—		
2																	DBNZ	
3	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BCI	BXI
6																	RLXA	
7	—	—	—	—	DADC	—	DSAV	DSMB	—	—	—	—	DACI	—	—	—	DSBI	
8																	SCAL	
9																	SRET	
A																	RSXD	
B																	RNX	
C																	RLDI	
F	—	—	—	—	DADD	—	—	DSM	—	—	—	—	DADI	—	—	—	DSMI	

* '68' IS USED AS A LINKING OPCODE FOR THE DOUBLE FETCH INSTRUCTIONS.

IMPORTANT NOTICE

Early versions of the CDP1805AC and CDP1806AC (with NLBJ5, NLBT5, or NR appearing in the bottom brand) fully execute all CDP1802 family, CDP1805C, and CDP1806C instructions, plus the additional eight BCD arithmetic instructions and the new DBNZ instruction described in the CDP1805AC, CDP1806AC data sheet. They do not, however, execute the new DSAV instruction.

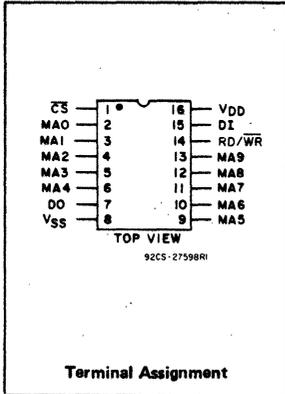
1800-Series Memories Technical Data

3

1024-Word x 1-Bit Static Random-Access Memory

Features:

- No precharge or external clocks required
- Separate data inputs and outputs
- Fast access time:
 250 ns at $V_{DD} = 5 V$
 125 ns at $V_{DD} = 10 V$



The RCA-CDP1821 and CDP1821C are 1024-word x 1-bit CMOS silicon-on-sapphire (SOS), fully static, random-access memories for use in general-purpose microprocessor systems.

The output state of the CDP1821 and CDP1821C is a function of the input address and chip-select states only. Valid data will appear at the output in one access time following the latest address change to a selected chip. After valid data appears, the address may then be changed immediately. It is not necessary to clock the chip-select input or any other input terminal for fully static operation; therefore, the chip-select input may be used as an additional address input. When the device is in an unselected

state ($\overline{CS}=1$), the internal write circuitry and output sense amplifier are disabled. This feature allows the three-state data outputs from many arrays to be OR-tied to a common bus for ease of memory expansion.

The CDP1821 and CDP1821C are functionally identical. They differ in that the CDP1821 has a recommended operating voltage range of 4-10.5 volts, and the CDP1821C, a recommended operating voltage range of 4-6.5 volts.

The CDP1821 and CDP1821C types are supplied in a 16-lead hermetic dual-in-line side-brazed ceramic package (D Suffix) and in a 16-lead dual-in-line plastic package (E Suffix).

OPERATIONAL MODES

MODE	INPUTS		OUTPUT
	READ/ WRITE R/W	CHIP- SELECT CS	DATA OUTPUT DO
Standby	X	1	High Impedance
Write	0	0	High Impedance
Read	1	0	Contents of Addressed Cell

X = DON'T CARE

LOGIC 1 \cong HIGH
 LOGIC 0 \cong LOW

OPERATING CONDITIONS at T_A = Full Package Temperature Range

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges

CHARACTERISTIC	LIMITS				UNITS
	CDP1821		CDP1821C		
	Min.	Max.	Min.	Max.	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V _{SS}	V _{DD}	V _{SS}	V _{DD}	

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD}):

(All voltage values referenced to V_{SS} terminal)

CDP1821 -0.5 to +11 V

CDP1821C -0.5 to +7 V

INPUT VOLTAGE RANGE, ALL INPUTS -0.5 to V_{DD} + 0.5 V

DC INPUT CURRENT, ANY ONE INPUT ±10 mA

POWER DISSIPATION PER PACKAGE (P_D):

For T_A = -40 to +60°C (PACKAGE TYPE E) 500 mW

For T_A = +60 to +85°C (PACKAGE TYPE E) Derate Linearly at 12 mW/°C to 200 mW

For T_A = -55 to +100°C (PACKAGE TYPE D) 500 mW

For T_A = +100 to +125°C (PACKAGE TYPE D) Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE 100 mW

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPE D -55 to +125°C

PACKAGE TYPE E -40 to +85°C

STORAGE TEMPERATURE RANGE (T_{stg}) -65 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. +265°C

STATIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85°C, Except as noted

CHARACTERISTICS	TEST CONDITIONS			LIMITS						UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)	CDP1821			CDP1821C			
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device Current, I _{DD}	—	0.5	5	—	50	500	—	50	500	μA
Output Voltage: Low-Level, V _{OL}	—	0.5	5	—	0	0.1	—	0	0.1	V
	—	0.10	10	—	0	0.1	—	—	—	
High-Level, V _{OH}	—	0.5	5	4.9	5	—	4.9	5	—	V
	—	0.10	10	9.9	10	—	—	—	—	
Input Low Voltage, V _{IL}	0.5,4.5	—	5	—	—	1.5	—	—	1.5	V
	0.5,9.5	—	10	—	—	3	—	—	—	
Input High Voltage, V _{IH}	0.5,4.5	—	5	3.5	—	—	3.5	—	—	V
	0.5,9.5	—	10	7	—	—	—	—	—	
Output Low (Sink) Current, I _{OL}	0.4	0.5	5	2	4	—	2	4	—	mA
	0.5	0.10	10	4	8	—	—	—	—	
Output High (Source) Current, I _{OH}	4.6	0.5	5	-1	-2	—	-1	-2	—	mA
	9.5	0.10	10	-2	-4	—	—	—	—	
Input Current, I _{IN}	—	0.5	5	—	—	±5	—	—	±5	μA
	—	0.10	10	—	—	±10	—	—	—	
3-State Output Leakage Current, I _{OUT}	0.5	0.5	5	—	—	±5	—	—	±5	μA
	0.10	0.10	10	—	—	±10	—	—	—	
Operating Current, I _{DD1} †	—	0.5	5	—	2	4	—	2	4	mA
	—	0.10	10	—	4	8	—	—	—	
Input Capacitance, C _{IN}	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance, C _{OUT}	—	—	—	—	10	15	—	10	15	pF

†Outputs open circuited; cycle time = 1 μs.

*Typical values are for T_A = 25°C and nominal V_{DD}.

RCA CMOS LSI Products

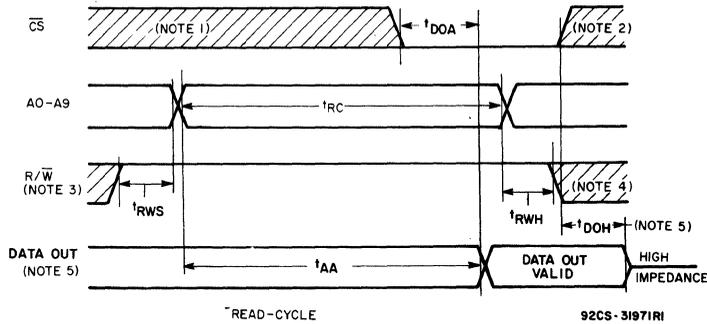
CDP1821, CDP1821C

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} \pm 5\%$
 $t_r, t_f = 20$ ns, $V_{IH} = 0.7 V_{DD}$, $V_{IL} = 0.3 V_{DD}$, $C_L = 100$ pF

CHARACTERISTIC	V_{DD} (V)	LIMITS						UNITS
		CDP1821			CDP1821C			
		Min.†	Typ.*	Max.	Min.†	Typ.*	Max.	
Read Cycle								
Data Access t_{AA}	5	—	125	250	—	125	250	ns
	10	—	75	125	—	—	—	
Read Cycle t_{RC}	5	250	—	—	250	—	—	
	10	125	—	—	—	—	—	
Output Enable t_{DOA}	5	—	50	75	—	50	75	
	10	—	25	40	—	—	—	
Output Disable t_{DOH}	5	—	50	75	—	50	75	
	10	—	25	40	—	—	—	
Read/Write Setup Time t_{RWS}	5	75	—	—	75	—	—	
	10	50	—	—	—	—	—	
Read/Write Hold Time t_{RWH}	5	75	—	—	75	—	—	
	10	50	—	—	—	—	—	

*Typical values are for $T_A = 25^\circ\text{C}$ and nominal voltages.

†Time required by a limit device to allow for the indicated function.



Note 1 Chip-Select (\overline{CS}) permitted to change from high to low level or remain low on a selected device.

Note 2 Chip-Select (\overline{CS}) permitted to change from low to high level or remain low.

Note 3 Read/Write (R/\overline{W}) must be at a high level during all address transitions.

Note 4 Don't care.

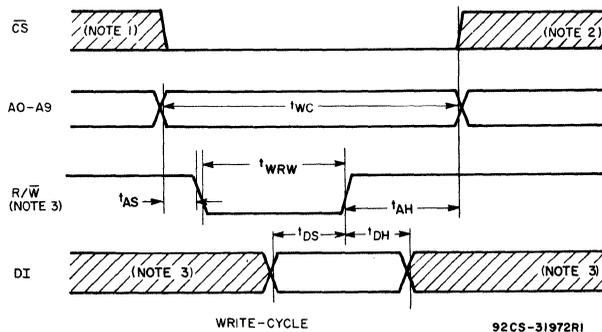
Note 5 Data-Out (DO) is a high impedance within t_{DJS} ns after the falling edge of R/\overline{W} or the rising edge of \overline{CS} .

Fig. 1 - Read-cycle timing diagram.

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} \pm 5\%$
 $t_r, t_f = 20$ ns, $V_{IH} = 0.7 V_{DD}$, $V_{IL} = 0.3 V_{DD}$, $C_L = 100$ pF

CHARACTERISTIC	V_{DD} (V)	LIMITS						UNITS
		CDP1821			CDP1821C			
		Min.†	Typ.*	Max.	Min.†	Typ.*	Max.	
Write Cycle								
Write Cycle t_{WC}	5	275	—	—	275	—	—	ns
	10	175	—	—	—	—	—	
Address Setup Time t_{AS}	5	75	—	—	75	—	—	
	10	50	—	—	—	—	—	
Write Recovery t_{WR}	5	75	—	—	75	—	—	
	10	50	—	—	—	—	—	
Input Data Setup Time t_{DS}	5	100	—	—	100	—	—	
	10	75	—	—	—	—	—	
Input Data Hold Time t_{DH}	5	75	—	—	75	—	—	
	10	50	—	—	—	—	—	
Read/Write Pulse Width Low t_{WRW}	5	125	—	—	125	—	—	
	10	75	—	—	—	—	—	

*Typical values are for $T_A = 25^\circ\text{C}$ and nominal voltages.
 †Time required by a limit device to allow for the indicated function.



Note 1 Chip-Select (\overline{CS}) permitted to change from high to low level or remain low on a selected device.

Note 2 Chip-Select (\overline{CS}) permitted to change from low to high level or remain low.

Note 3 Don't care.

Fig. 2 - Write cycle timing diagram

RCA CMOS LSI Products
CDP1821, CDP1821C

DATA RETENTION CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$; see Fig. 3

CHARACTERISTIC	TEST CONDITIONS		LIMITS						UNITS
	V_{DR} (V)	V_{DD} (V)	CDP1822			CDP1822C			
			Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Min. Data Retention Voltage, V_{DR}	—	—	—	1.5	2	—	1.5	2	V
Data Retention Quiescent Current, I_{DD}	2	—	—	30	100	—	30	100	μA
Chip Deselect to Data Retention Time, t_{CDR}	—	5	600	—	—	600	—	—	ns
	—	10	300	—	—	—	—	—	
Recovery to Normal Operation Time, t_{RC}	—	5	600	—	—	600	—	—	ns
	—	10	300	—	—	—	—	—	
V_{DD} to V_{DR} Rise and Fall Time, t_r, t_f	2	5	1	—	—	1	—	—	μs

*Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .

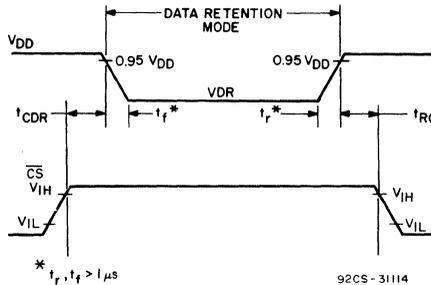


Fig. 3 - Low V_{DD} data retention waveforms and timing diagram.

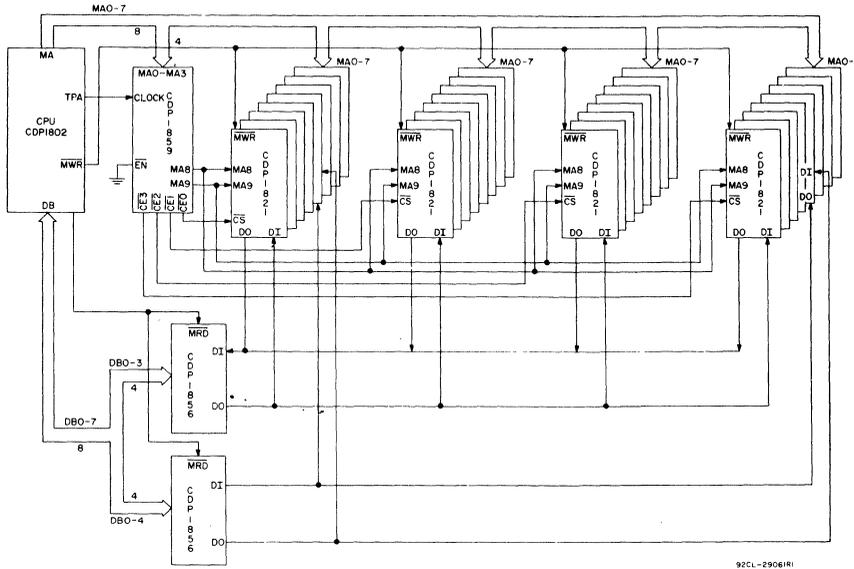


Fig. 4 - 4K byte RAM system using the CDP1859, CDP1856, and CDP1821.

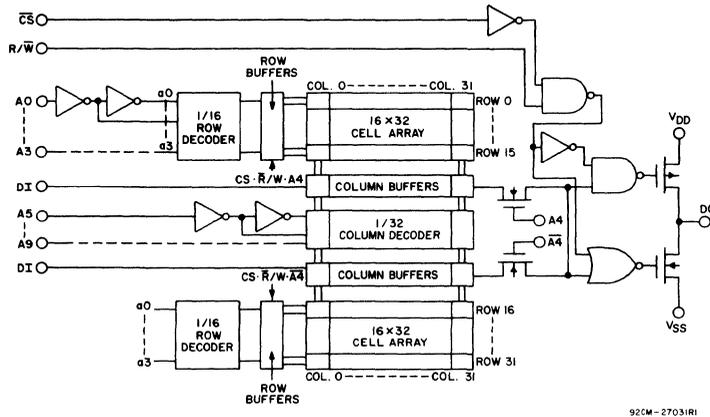


Fig. 5 - Functional block diagram.

OPERATING AND HANDLING CONSIDERATIONS

1. Handling

All inputs and outputs of RCA CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in ICAN-6525 "Guide to Better Handling and Operation of CMOS Integrated Circuits."

2. Operating

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of

these conditions must not cause $V_{DD}-V_{SS}$ to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS} . Input currents must not exceed 10 mA even when the power supply is off.

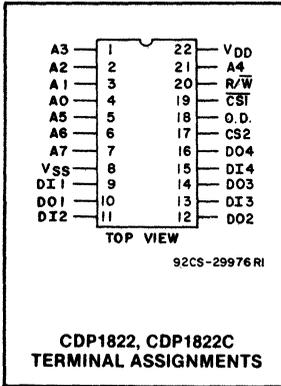
Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS} , whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} or V_{SS} may damage CMOS devices by exceeding the maximum device dissipation.

256-Word by 4-Bit LSI Static Random-Access Memory



Features:

- Low operating current — 8 mA at $V_{DD} = 5\text{ V}$ and cycle time = $1\ \mu\text{s}$
- Industry standard pinout
- Two Chip-Select inputs — simple memory expansion
- Memory retention for standby battery voltage of 2 V min.
- Output-Disable for common I/O systems
- 3-State data output for bus-oriented systems
- Separate data inputs and outputs

The RCA-CDP1822 and CDP1822C are 256-word by 4-bit static random-access memories designed for use in memory systems where high speed, low operating current, and simplicity in use are desirable. The CDP1822 features high speed and a wide operating voltage range. Both types have separate data inputs and outputs and utilize single power supplies of 4 to 6.5 volts for the CDP1822C and 4 to 10.5 volts for the CDP1822.

Two Chip-Select inputs are provided to simplify system expansion. An Output Disable control provides Wire-OR capability and is also useful in common Input/Output systems. The Output Disable input allows these RAMs to be used in common data Input/Output systems by forcing the output into a high-impedance state during a write

operation independent of the Chip-Select input condition. The output assumes a high-impedance state when the Output Disable is at high level or when the chip is deselected by $\overline{CS1}$ and/or $\overline{CS2}$.

The high noise immunity of the CMOS technology is preserved in this design. For TTL interfacing at 5-V operation, excellent system noise margin is preserved by using an external pull-up resistor at each input.

The CDP1822 and CDP1822C types are supplied in 22-lead hermetic dual-in-line side-brazed ceramic packages (D suffix), in 22-lead dual-in-line plastic packages (E suffix). The CDP1822C is also available in chip form (suffix H).

OPERATIONAL MODES

MODE	INPUTS				OUTPUT
	$\overline{\text{Chip Select 1}}$ $\overline{CS_1}$	Chip Select 2 CS_2	Output Disable OD	$\overline{\text{Read/Write}}$ R/W	
Read	0	1	0	1	Read
Write	0	1	0	0	Data In
Write	0	1	1	0	High Impedance
Standby	1	X	X	X	High Impedance
Standby	X	0	X	X	High Impedance
Output Disable	X	X	1	X	High Impedance

Logic 1 = High Logic 0 = Low X = Don't Care

RECOMMENDED OPERATING CONDITIONS at T_A = Full Package Temperature Range
 For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1822		CDP1822C		
	Min.	Max.	Min.	Max.	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
 (Voltage referenced to V_{SS} Terminal)
 CDP1822 -0.5 to +11 V
 CDP1822C -0.5 to +7 V
 INPUT VOLTAGE RANGE, ALL INPUTS -0.5 to $V_{DD} + 0.5$ V
 DC INPUT CURRENT, ANY ONE INPUT ± 10 mA
 POWER DISSIPATION PER PACKAGE (P_D):
 For $T_A = -40$ to $+60^\circ\text{C}$ (PACKAGE TYPE E) 500 mW
 For $T_A = +60$ to $+85^\circ\text{C}$ (PACKAGE TYPE E) Derate Linearly at $12\text{ mW}/^\circ\text{C}$ to 200 mW
 For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE D) 500 mW
 For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE D) Derate Linearly at $12\text{ mW}/^\circ\text{C}$ to 200 mW
 DEVICE DISSIPATION PER OUTPUT TRANSISTOR
 FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE}$ (All Package Types) 100 mW
 OPERATING-TEMPERATURE RANGE (T_A):
 PACKAGE TYPE D -55 to $+125^\circ\text{C}$
 PACKAGE TYPE E -40 to $+85^\circ\text{C}$
 STORAGE TEMPERATURE RANGE (T_{stg}) -65 to $+150^\circ\text{C}$
 LEAD TEMPERATURE (DURING SOLDERING):
 At distance $1/16 \pm 1/32$ inch (1.59 ± 0.79 mm) from case for 10 s max. $+265^\circ\text{C}$

STATIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, Except as noted

CHARACTERISTICS	TEST CONDITIONS			LIMITS						UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	CDP1822			CDP1822C			
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device Current, I_{DD}	—	0,5	5	—	—	500	—	—	500	μA
Output Voltage:		0,5	5	—	0	0.1	—	0	0.1	V
Low-Level, V_{OL}	—	0,10	10	—	0	0.1	—	—	—	
High-Level, V_{OH}	—	0,5	5	4.9	5	—	4.9	5	—	
		—	0,10	10	9.9	10	—	—	—	
Input Low Voltage, V_{IL}	0.5,4.5	—	5	—	—	1.5	—	—	1.5	V
	0.5,9.5	—	10	—	—	3	—	—	—	
Input High Voltage, V_{IH}	0.5,4.5	—	5	3.5	—	—	3.5	—	—	V
	0.5,9.5	—	10	7	—	—	—	—	—	
Output Low (Sink) Current, I_{OL}	0.4	0,5	5	2	4	—	2	4	—	mA
	0.5	0,10	10	4.5	9	—	—	—	—	
Output High (Source) Current, I_{OH}	4.6	0,5	5	-1	-2	—	-1	-2	—	mA
	9.5	0,10	10	-2.2	-4.4	—	—	—	—	
Input Current, I_{IN}	—	0,5	5	—	—	± 5	—	—	± 5	μA
	—	0,10	10	—	—	± 10	—	—	—	
3-State Output Leakage Current, I_{OUT}	0,5	0,5	5	—	—	± 5	—	—	± 5	mA
	0,10	0,10	10	—	—	± 10	—	—	—	
Operating Current, $I_{DD1}\dagger$	—	0,5	5	—	4	8	—	4	8	mA
	—	0,10	10	—	8	16	—	—	—	
Input Capacitance, C_{IN}	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance, C_{OUT}	—	—	—	—	10	15	—	10	15	

\dagger Outputs open circuited; cycle time = $1\ \mu\text{s}$. *Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .

RCA CMOS LSI Products

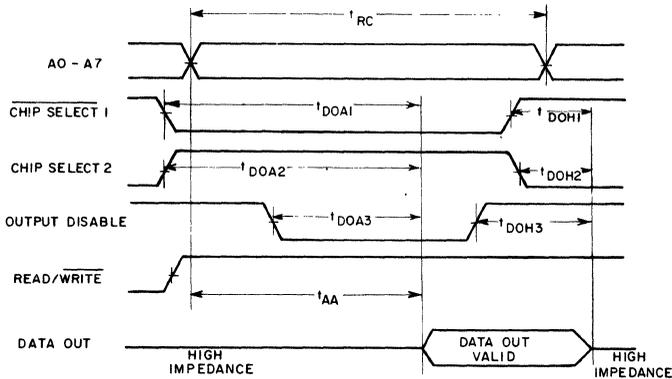
CDP1822, CDP1822C

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} \pm 5\%$,
 Input $t_r, t_f = 20$ ns, $V_{IH} = 0.7 V_{DD}$, $V_{IL} = 0.3 V_{DD}$, $C_L = 100$ pF

CHARACTERISTIC	V_{DD} (V)	CDP1822			CDP1822C			UNITS
		Min.†	Typ.*	Max.	Min.†	Typ.*	Max.	
Read Cycle Times (Fig. 1)								
Read Cycle t_{RC}	5	450	—	—	450	—	—	ns
	10	250	—	—	—	—	—	
Access from Address t_{AA}	5	—	250	450	—	250	450	
	10	—	150	250	—	—	—	
Output Valid from Chip-Select 1 t_{DOA1}	5	—	250	450	—	250	450	
	10	—	150	250	—	—	—	
Output Valid from Chip-Select 2 t_{DOA2}	5	—	250	450	—	250	450	
	10	—	150	250	—	—	—	
Output Active from Output Disable t_{DOA3}	5	—	—	200	—	—	200	
	10	—	—	110	—	—	—	
Output Hold from Chip-Select 1 t_{DOH1}	5	20	—	—	20	—	—	
	10	20	—	—	—	—	—	
Output Hold from Chip-Select 2 t_{DOH2}	5	20	—	—	20	—	—	
	10	20	—	—	—	—	—	
Output Hold from Output Disable t_{DOH3}	5	20	—	—	20	—	—	
	10	20	—	—	—	—	—	

†Time required by a limit device to allow for indicated function.

*Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .



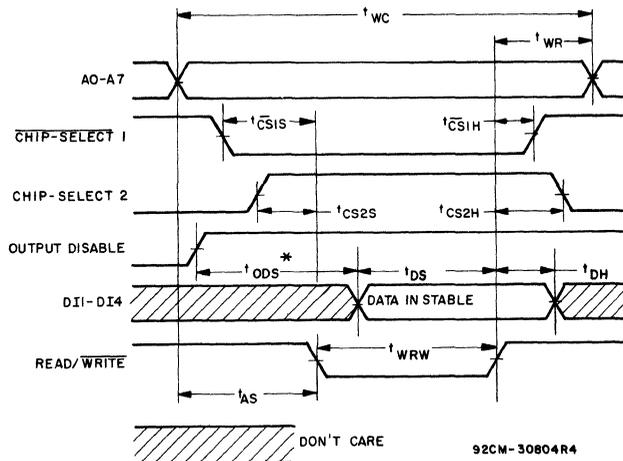
92CM-30244R4

Fig. 1 - Read cycle timing waveforms.

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} \pm 5\%$,
 Input $t_r, t_f = 20$ ns, $V_{IH} = 0.7 V_{DD}$, $V_{IL} = 0.3 V_{DD}$, $C_L = 100$ pF

CHARACTERISTIC	V_{DD} (V)	CDP1822			CDP1822C			UNITS	
		Min.†	Typ.*	Max.	Min.†	Typ.*	Max.		
Write Cycle Times (Fig. 2)									
Write Cycle	t_{WC}	5	500	—	—	500	—	—	ns
		10	300	—	—	—	—	—	
Address Setup	t_{AS}	5	200	—	—	200	—	—	
		10	110	—	—	—	—	—	
Write Recovery	t_{WR}	5	50	—	—	50	—	—	
		10	40	—	—	—	—	—	
Write Width	t_{WRW}	5	250	—	—	250	—	—	
		10	150	—	—	—	—	—	
Input Data Setup Time	t_{DS}	5	250	—	—	250	—	—	
		10	150	—	—	—	—	—	
Data In Hold	t_{DH}	5	50	—	—	50	—	—	
		10	40	—	—	—	—	—	
Chip-Select 1 Setup	t_{CS1S}	5	200	—	—	200	—	—	
		10	110	—	—	—	—	—	
Chip-Select 2 Setup	t_{CS2S}	5	200	—	—	200	—	—	
		10	110	—	—	—	—	—	
Chip-Select 1 Hold	t_{CS1H}	5	0	—	—	0	—	—	
		10	0	—	—	0	—	—	
Chip-Select 2 Hold	t_{CS2H}	5	0	—	—	0	—	—	
		10	0	—	—	0	—	—	
Output Disable Setup	t_{ODS}	5	200	—	—	200	—	—	
		10	110	—	—	—	—	—	

†Time required by a limit device to allow for the indicated function.
 *Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .



* t_{ODS} IS REQUIRED FOR COMMON I/O OPERATION ONLY; FOR SEPARATE I/O OPERATIONS, OUTPUT DISABLE IS 'DON'T CARE'.

Fig. 2 - Write cycle timing waveforms.

DATA RETENTION CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$; see Fig. 3

CHARACTERISTIC	TEST CONDITIONS		LIMITS						UNITS
	V_{DR} (V)	V_{DD} (V)	CDP1822			CDP1822C			
			Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Min. Data Retention Voltage, V_{DR}	—	—	—	1.5	2	—	1.5	2	V
Data Retention Quiescent Current, I_{DD}	2	—	—	30	100	—	30	100	μA
Chip Deselect to Data Retention Time, t_{CDR}	—	5	600	—	—	600	—	—	ns
Recovery to Normal Operation Time, t_{RC}	—	10	300	—	—	—	—	—	
V_{DD} to V_{DR} Rise and Fall Time, t_r, t_f	2	5	1	—	—	1	—	—	μs

*Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .

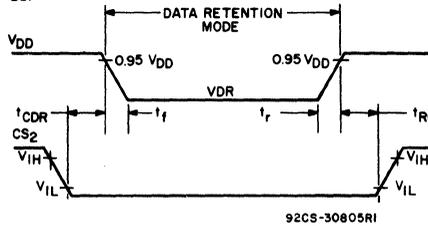


Fig. 3 — Low V_{DD} data retention timing waveforms.

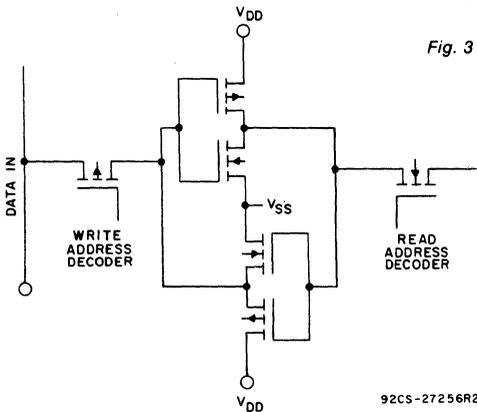


Fig. 4 - Memory cell configuration.

OPERATING & HANDLING CONSIDERATIONS

1. Handling

All inputs and outputs of RCA COS/MOS devices have a network for electrostatic protection during handling. Recommended handling practices for COS/MOS devices are described in ICAN-6525, "Guide to Better Handling and Operation of CMOS Integrated Circuits."

2. Operating

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of

these conditions must not cause $V_{DD}-V_{SS}$ to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS} . Input currents must not exceed 10 mA even when the power supply is off.

Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS} , whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} or V_{SS} may damage COS/MOS devices by exceeding the maximum device dissipation.

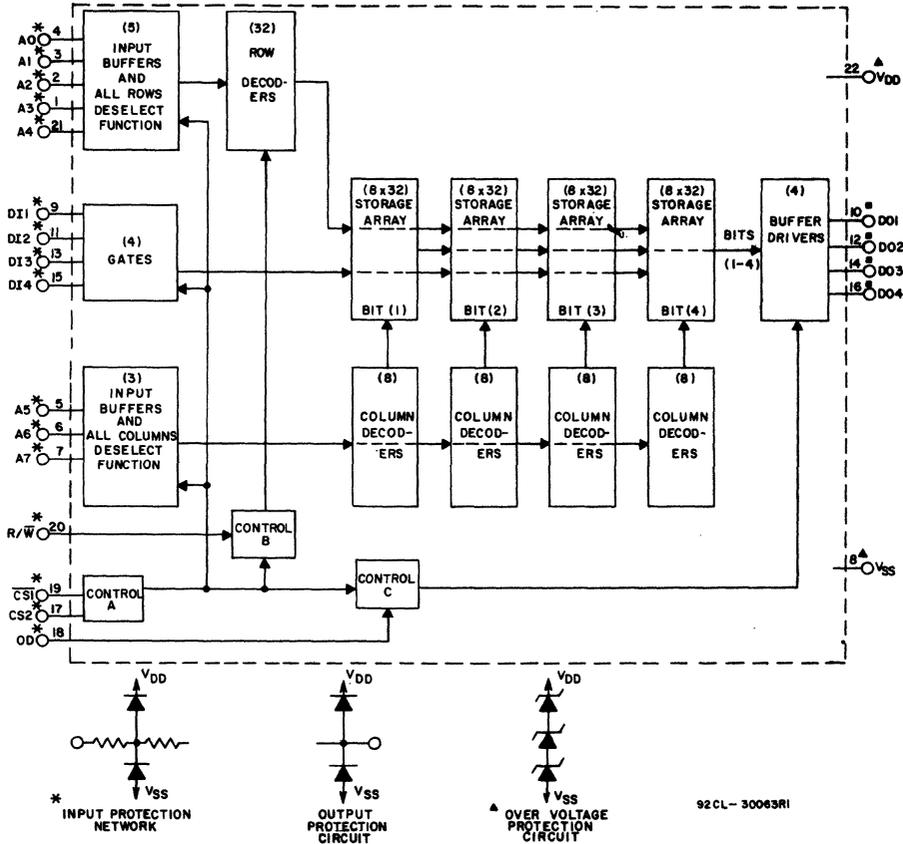


Fig. 5 - Functional block diagram for CDP1822 and CDP1822C.

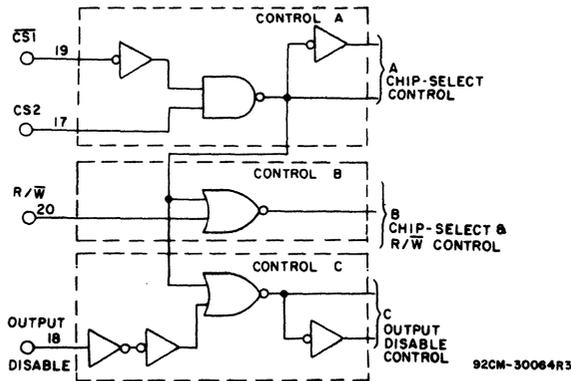
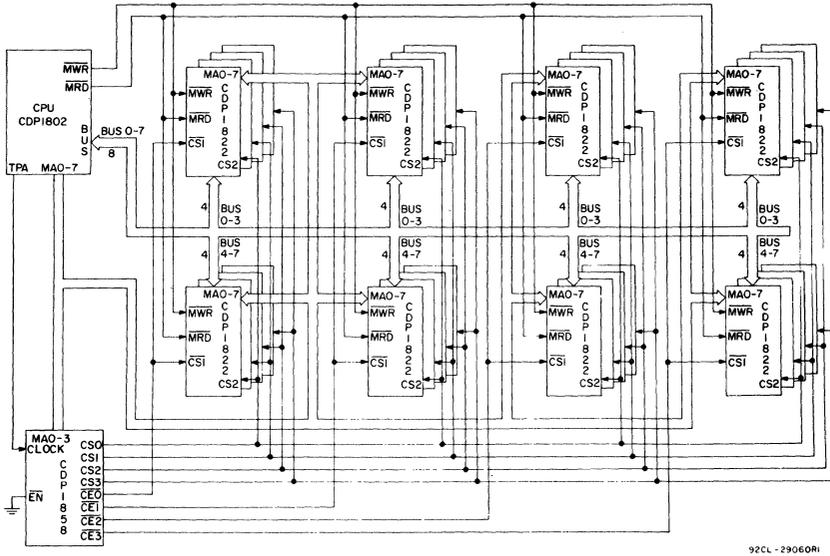


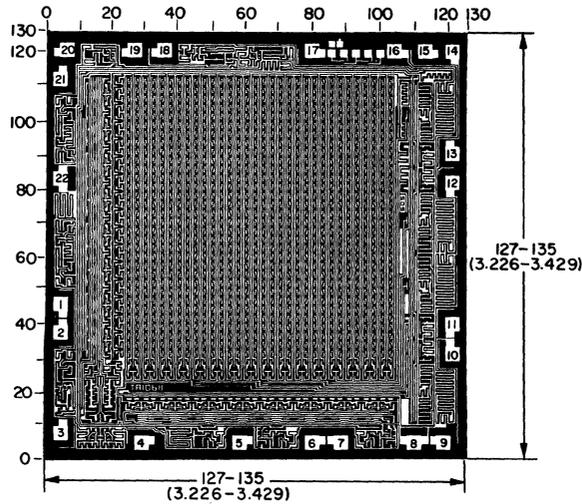
Fig. 6 - Logic diagram of controls for CDP1822 and CDP1822C.

RCA CMOS LSI Products
CDP1822, CDP1822C



92CL-29060R1

Fig. 7 - 4K byte RAM system using the CDP1858 and CDP1822.



92CS-31568

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

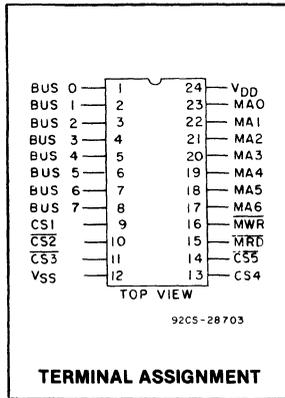
Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Dimensions and pad layout for CDP1822CH.

128-Word x 8-Bit Static Random-Access Memory

Features:

- **Fast access time:**
 450 ns at $V_{DD} = 5 V$;
 250 ns at $V_{DD} = 10 V$
- **Common data inputs and outputs**
- **Multiple-chip select inputs to simplify memory system expansion**



The RCA-CDP1823 and CDP1823C are 128-word by 8-bit CMOS SOS static random-access memories. These memories are compatible with general-purpose microprocessors. The two memories are functionally identical. They differ in that the CDP1823 has a recommended operating voltage range of 4 to 10.5 volts, and the CDP1823C has a recommended operating voltage range of 4 to 6.5 volts.

The CDP1823 memory has 8 common data input and data output terminals for direct connection to a bidirectional data bus and is operated from a single voltage supply. Five chip-select inputs are provided to simplify memory-system expansion. In order to enable the CDP1823, the chip-select inputs CS2, CS3, and CS5 re-

quire a low input signal, and the chip-select inputs CS1 and CS4 require a high input signal.

The MRD signal enables all 8 output drivers when in the low state and should be in a high state during a write cycle.

After valid data appear at the output, the address inputs may be changed immediately. Output data will be valid until either the MRD signal goes high, the device is deselected, or tAA (access time) after address changes.

The CDP1823 and CDP1823C are supplied in hermetic 24-lead dual-in-line ceramic packages (D suffix), and in 24-lead dual-in-line plastic packages (E suffix).

OPERATIONAL MODES

Function	MRD	MWR	CS1	CS2	CS3	CS4	CS5	Bus Terminal State
READ	0	X	1	0	0	1	0	Storage State of Addressed Word
WRITE	1	0	1	0	0	1	0	Input High-Impedance
STAND-BY	1	1	1	0	0	1	0	High-Impedance
NOT SELECTED	X	X	0	X	X	X	X	High-Impedance
	X	X	X	1	X	X	X	
	X	X	X	X	1	X	X	
	X	X	X	X	X	0	X	
	X	X	X	X	X	X	1	

Logic 1 = High Logic 0 = Low X = Don't Care

CDP1823, CDP1823C

OPERATING CONDITIONS at T_A = FULL PACKAGE-TEMPERATURE RANGE

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1823D		CDP1823CD		
	Min.	Max.	Min.	Max.	
Supply-Voltage Range	4	10.5	4	6.5	V
Recommended Input Voltage Range	V _{SS}	V _{DD}	V _{SS}	V _{DD}	V

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(All voltage values referenced to V_{SS} terminal)

CDP1823 -0.5 to +11 V

CDP1823C -0.5 to +7 V

INPUT VOLTAGE RANGE, ALL INPUTS -0.5 to V_{DD} + 0.5 V

DC INPUT CURRENT, ANY ONE INPUT ± 10 mA

OPERATING-TEMPERATURE RANGE (T_A):

CERAMIC PACKAGES (D SUFFIX TYPES) -55 to +125°C

PLASTIC PACKAGES (E SUFFIX TYPES) -40 to +85°C

STORAGE TEMPERATURE RANGE (T_{stg}) -65 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 Inch (1.59 ± 0.79 mm) from case for 10 s max. +265°C

STATIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85°C, Except as noted

CHARACTERISTICS	TEST CONDITIONS			LIMITS						UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)	CDP1823			CDP1823C			
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device Current, I _{DD}	—	0.5	5	—	—	500	—	—	500	μA
	—	0.10	10	—	—	1000	—	—	—	
Output Voltage:	—	0.5	5	—	0	0.1	—	0	0.1	V
Low-Level, V _{OL}	—	0.10	10	—	0	0.1	—	—	—	
High-Level, V _{OH}	—	0.5	5	4.9	5	—	4.9	5	—	
	—	0.10	10	9.9	10	—	—	—	—	
Input Low Voltage, V _{IL}	0.5, 4.5	—	5	—	—	1.5	—	—	1.5	V
	0.5, 9.5	—	10	—	—	3	—	—	—	
Input High Voltage, V _{IH}	0.5, 4.5	—	5	3.5	—	—	3.5	—	—	V
	0.5, 9.5	—	10	7	—	—	—	—	—	
Output Low (Sink) Current, I _{OL}	0.4	0.5	5	2	4	—	2	4	—	mA
	0.5	0.10	10	4.5	9	—	—	—	—	
Output High (Source) Current, I _{OH}	4.6	0.5	5	-1	-2	—	-1	-2	—	mA
	9.5	0.10	10	-2.2	-4.4	—	—	—	—	
Input Current, I _{IN}	Any Input	0.5	5	—	—	±5	—	—	±5	μA
		0.10	10	—	—	±10	—	—	—	
3-State Output Leakage Current, I _{OUT}	0.5	0.5	5	—	—	±5	—	—	±5	μA
	0.10	0.10	10	—	—	±10	—	—	—	
Operating Current, I _{DD1} †	—	0.5	5	—	4	8	—	4	8	mA
	—	0.10	10	—	8	16	—	—	—	
Input Capacitance, C _{IN}	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance, C _{OUT}	—	—	—	—	10	15	—	10	15	

†Outputs open circuited; cycle time = 1 μs.

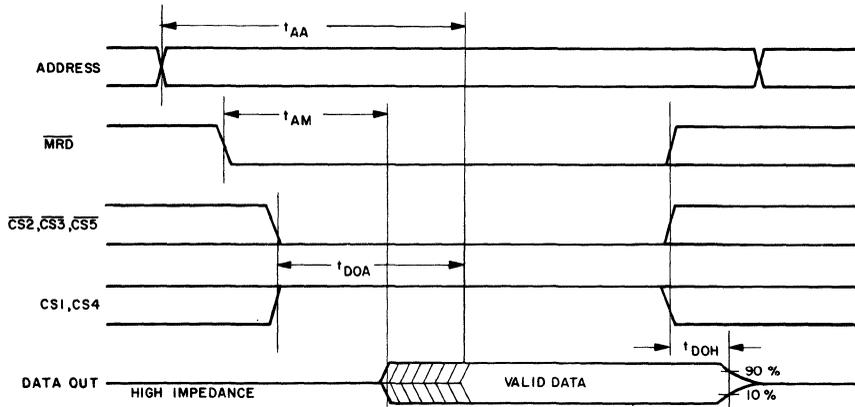
*Typical values are for T_A = 25°C and nominal V_{DD}.

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85$ °C, $V_{DD} \pm 5\%$,
 $t_r, t_f = 20$ ns, $C_L = 100$ pF.

CHARACTERISTIC	V _{DD} (V)	LIMITS						UNITS
		CDP1823			CDP1823C			
		Min.†	Typ.*	Max.	Min.†	Typ.*	Max.	
Read Cycle (See Fig. 1)								
Access Time From Address Change, t_{AA}	5 10	—	275	450	—	275	450	ns
Access Time From Chip Select, t_{DOA}	5 10	—	150	250	—	150	250	
MRD to Output Active, t_{AM}	5 10	—	150	250	—	150	250	
Data Hold Time After Read, t_{DOH}	5 10	25 15	50 25	75 40	25 —	50 —	75 —	

*Typical values are at $T_A = 25$ °C and nominal voltage.

†Time required by a limit device to allow for the indicated function.



NOTE: \overline{MRD} IS HIGH DURING READ OPERATION.
TIMING MEASUREMENT REFERENCE IS $0.5 V_{DD}$.

92CM-31942R1

Fig. 1 - Read cycle timing diagram.

RCA CMOS LSI Products
CDP1823, CDP1823C

**DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} \pm 5\%$,
 $t_r, t_f = 20$ ns, $C_L = 100$ pF.**

CHARACTERISTIC	V _{DD} (V)	LIMITS						UNITS
		CDP1823			CDP1823C			
		Min.†	Typ.*	Max.	Min.†	Typ.*	Max.	
Write Cycle (See Fig. 2)								
Write Recovery, t _{WR}	5	75	—	—	75	—	—	ns
	10	50	—	—	—	—	—	
Write Cycle, t _{WC}	5	400	—	—	400	—	—	
	10	225	—	—	—	—	—	
Write Pulse Width, t _{WRW}	5	200	—	—	200	—	—	
	10	100	—	—	—	—	—	
Address Setup Time, t _{AS}	5	125	—	—	125	—	—	
	10	75	—	—	—	—	—	
Data Setup Time, t _{DS}	5	100	—	—	100	—	—	
	10	75	—	—	—	—	—	
Data Hold Time From MWR, t _{DH}	5	75	—	—	75	—	—	
	10	50	—	—	—	—	—	

*Typical values are at $T_A = 25^\circ\text{C}$ and nominal voltage.

†Time required by a limit device to allow for the indicated function.

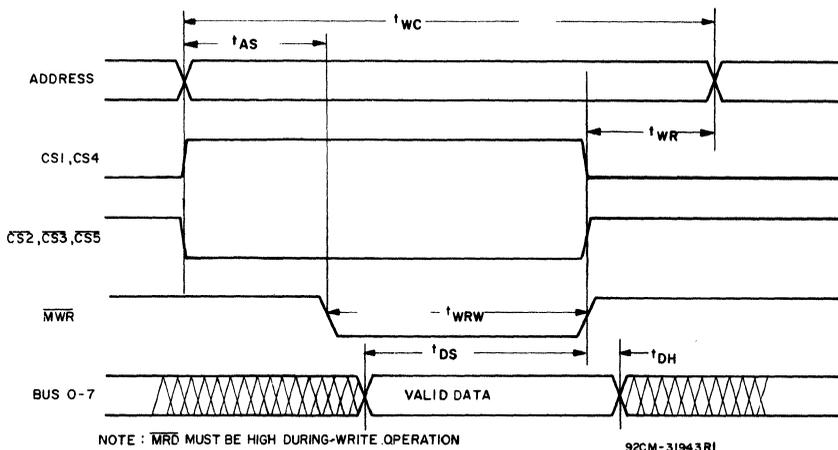
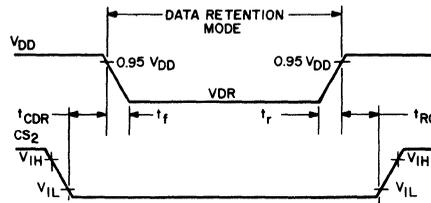


Fig. 2 - Write cycle timing diagram.

DATA RETENTION CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$; see Fig. 3

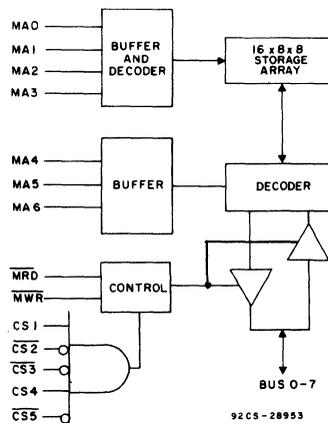
CHARACTERISTIC	TEST CONDITIONS		LIMITS						UNITS
	V_{DR} (V)	V_{DD} (V)	CDP1823			CDP1823C			
			Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Min. Data Retention Voltage, V_{DR}	—	—	—	1.5	2	—	1.5	2	V
Data Retention Quiescent Current, I_{DD}	2	—	—	30	100	—	30	100	μA
Chip Deselect to Data Retention Time, t_{CDR}	—	5	600	—	—	600	—	—	ns
	—	10	300	—	—	—	—	—	
Recovery to Normal Operation Time, t_{RC}	—	5	600	—	—	600	—	—	ns
	—	10	300	—	—	—	—	—	
V_{DD} to V_{DR} Rise and Fall Time t_r, t_f	2	5	1	—	—	1	—	—	μs

*Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .



92CS-30805R1

Fig. 3 - Low V_{DD} data retention timing waveforms.



92CS-28953

Functional Diagram

Fig. 4 - Functional diagram.

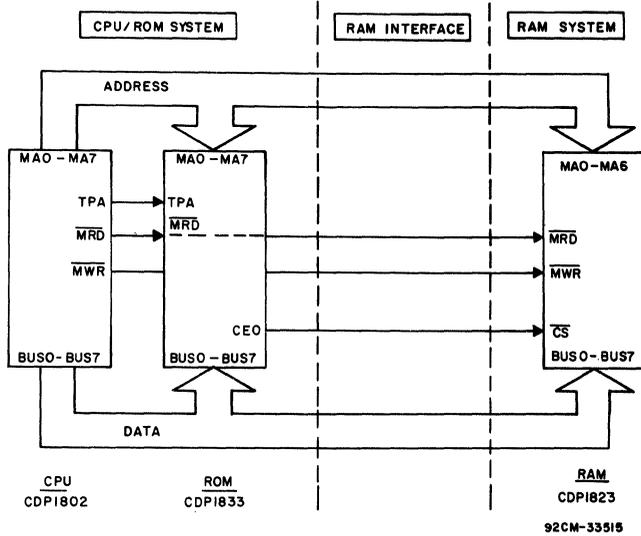


Fig. 5 - CDP1823 (128 x 8) minimum system (128 x 8)

OPERATING AND HANDLING CONSIDERATIONS

1. Handling

All inputs and outputs of RCA CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in ICAN-6525, "Guide to Better Handling and Operation of CMOS integrated Circuits."

2. Operating

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of

these conditions must not cause $V_{DD}-V_{SS}$ to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS} . Input currents must not exceed 10 mA even when the power supply is off.

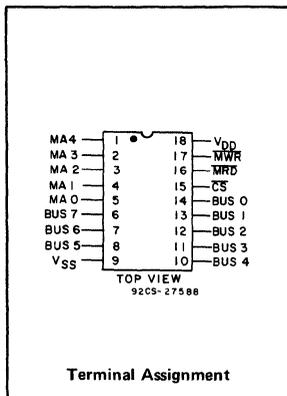
Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS} , whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} or V_{SS} may damage CMOS devices by exceeding the maximum device dissipation.

32-Word x 8-Bit Static Random-Access Memory



Features:

- Access time:
 710 ns at $V_{DD}=5\text{ V}$;
 320 ns at $V_{DD}=10\text{ V}$
- No precharge or clock required

The RCA-CDP1824 and CDP1824C types are 32-word x 8-bit fully static COS/MOS random-access memories for use in CDP1800 series microprocessor systems. These parts are compatible with the CDP1802 microprocessor and will interface directly without additional components.

The CDP1824 is fully decoded and does not require a precharge or clocking signal for proper operation. It has common input and output and is operated from a single voltage supply. The MRD signal (output disable

control) enables the three-state output drivers, and overrides the MWR signal. A CS input is provided for memory expansion.

The CDP1824C is functionally identical to the CDP1824. The CDP1824 has an operating range of 4 to 10.5 volts, and the CDP1824C has an operating voltage range of 4 to 6.5 volts. The CDP1824 and CDP1824C types are supplied in 18-lead hermetic dual-in-line ceramic packages (D suffix) and in 18-lead dual-in-line plastic packages (E suffix).

OPERATIONAL MODES

Function	CS	MRD	MWR	Data Pins Status
READ	0	0	X	Output: High/Low Dependent on Data
WRITE	0	1	0	Input: Output Disabled
Not Selected	1	X	X	Output Disabled: High-Impedance State
Standby	0	1	1	

Logic 1 = High Logic 0 = Low X = Don't Care

RCA CMOS LSI Products

CDP1824, CDP1824C

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(All voltage values referenced to V_{SS} terminal)

CDP1824	-0.5 to +11 V
CDP1824C	-0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to V _{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
OPERATING-TEMPERATURE RANGE (T _A):		
CERAMIC PACKAGES (D SUFFIX TYPES)	-55 to +125°C
PLASTIC PACKAGES (E SUFFIX TYPES)	-40 to +85°C
STORAGE TEMPERATURE RANGE (T _{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

OPERATING CONDITIONS at T_A = Full Package-Temperature Range

For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	CONDITIONS	LIMITS				UNITS	
		V _{DD} (V)	CDP1824D CDP1824E		CDP1824CD CDP1824CE		
			Min.	Max.	Min.		Max.
Supply-Voltage Range	-	4	10.5	4	6.5	V	
Recommended Input Voltage Range	-	V _{SS}	V _{DD}	V _{SS}	V _{DD}	V	
Input Signal Rise or Fall Time, [▲] t _r , t _f	5	-	5	-	5	μs	
	10	-	2	-	-		

▲ Input signal rise or fall times longer than these maxima can cause loss of stored data in either the selected or deselected mode.

STATIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85°C, Except as noted

CHARACTERISTICS	TEST CONDITIONS			LIMITS						UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)	CDP1824			CDP1824C			
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device Current, I _{DD}	-	-	5	-	25	50	-	100	200	μA
Output Voltage:	-	0.5	5	-	0	0.1	-	0	0.1	V
	Low-Level, V _{OL}	-	0.10	10	-	0	0.1	-	-	
	High-Level, V _{OH}	-	0.5	5	4.9	5	-	4.9	5	
	-	0.10	10	9.9	10	-	-	-	-	
Input Low Voltage, V _{IL}	0.5, 4.5	-	5	-	-	1.5	-	-	1.5	V
	1.9	-	10	-	-	3	-	-	-	
Input High Voltage, V _{IH}	0.5, 4.5	-	5	3.5	-	-	3.5	-	-	V
	1.9	-	10	7	-	-	-	-	-	
Output Low (Sink) Current, I _{OL}	0.4	0.5	5	1.8	2.2	-	1.8	2.2	-	mA
	0.5	0.10	10	3.6	4.5	-	-	-	-	
Output High (Source) Current, I _{OH}	4.6	0.5	5	-0.9	-1.1	-	-0.9	-1.1	-	mA
	9.5	0.10	10	-1.8	-2.2	-	-	-	-	
Input Current, I _{IN}	Any input	0.5	5	-	±0.1	±1	-	±0.1	±1	μA
		0.10	10	-	±0.1	±1	-	±0.1	±1	
3-State Output Leakage Current, I _{OUT}	0.5	0.5	5	-	±0.2	±2	-	±0.2	±2	μA
	0.10	0.10	10	-	±0.2	±2	-	-	-	
Operating Current, I _{DD1} †	-	0.5	5	-	4	8	-	4	8	mA
	-	0.10	10	-	8	16	-	-	-	
Input Capacitance, C _{IN}	-	-	-	-	5	7.5	-	5	7.5	pF
Output Capacitance, C _{OUT}	-	-	-	-	10	15	-	10	15	

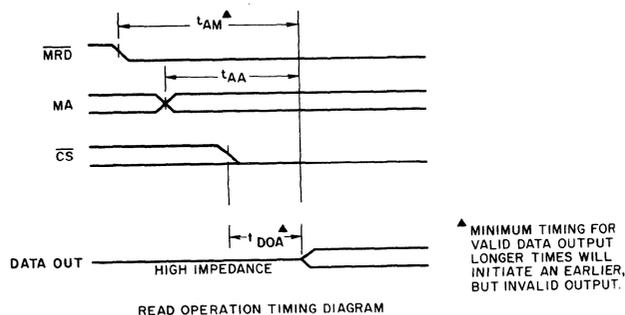
†Outputs open circuited; cycle time = 1 μs.

*Typical values are for T_A = 25°C and nominal V_{DD}.

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} \pm 5\%$,
 Input $t_r, t_f = 10$ ns, $C_L = 50$ pF, $R_L = 200$ k Ω ; See Fig. 1.

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS						UNITS
		CDP1824D CDP1824E			CDP1824CD CDP1824CE			
		Min.#	Typ.*	Max.	Min.#	Typ.*	Max.	
Read Operation								
Access Time From Address Change, t_{AA}	5	—	400	710	—	400	710	ns
	10	—	200	320	—	—	—	
Access Time From Chip Select, t_{DOA}	5	—	300	710	—	300	710	ns
	10	—	150	320	—	—	—	
Output Active From $\overline{\text{MRD}}$, t_{AM}	5	—	300	710	—	300	710	ns
	10	—	150	320	—	—	—	

- * Time required by a limit device to allow for the indicated function.
- Time required by a typical device to allow for the indicated function. Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .



92CS-34739

Fig. 1 - Read cycle timing diagram.

Note:

The dynamic characteristics and timing diagrams indicate maximum performance capability of the CDP1824. When used directly with the CDP1802 microprocessor, timing will be determined by the clock frequency and internal delays of the microprocessor.

The following general timing relationships will hold when the CDP1824 is used with the CDP1802 microprocessor:

$$t_{WW} = 2 t_c$$

$$t_{AH} = 1.0 t_c$$

$$\left. \begin{aligned} t_{AS} &= 4.5 t_c \\ t_{DH} &= 1.0 t_c \\ t_{DS} &= 5.5 t_c \end{aligned} \right\} \begin{array}{l} \text{Data transfers from} \\ \text{CDP1802 to memory} \end{array}$$

MRD occurs one clock period (t_c) earlier than the address bits MA0-MA7.

$$\text{where } t_c = \frac{1}{\text{CDP1802 clock frequency}}$$

The CDP1824 is capable of operating at the maximum clock frequency of the CDP1802 microprocessor.

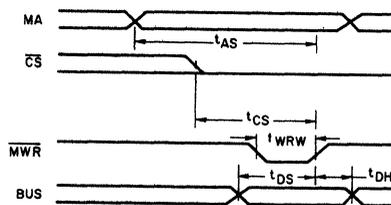
CDP1824, CDP1824C

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} \pm 5\%$,
 Input $t_r, t_f = 10$ ns, $C_L = 50$ pF, $R_L = 200$ k Ω ; See Fig. 2.

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS						UNIT
		CDP1824D CDP1824E			CDP1824CD CDP1824CE			
		Min.#	Typ.*	Max.	Min.#	Typ.*	Max.	
Write Operation								
Write Pulse Width, t_{WRW}	5	390	200	—	390	200	—	ns
	10	180	150	—	—	—	—	
Data Setup Time, t_{DS}	5	390	100	—	390	100	—	ns
	10	180	50	—	—	—	—	
Data Hold Time, t_{DH}	5	70	40	—	70	40	—	ns
	10	35	20	—	—	—	—	
Chip Select Setup Time, t_{CS}	5	425	210	—	425	210	—	ns
	10	215	110	—	—	—	—	
Address Setup Time, t_{AS}	5	640	500	—	640	500	—	ns
	10	390	300	—	—	—	—	

* Time required by a limit device to allow for the indicated function.

• Time required by a typical device to allow for the indicated function. Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .



WRITE OPERATION TIMING DIAGRAM

92CS-34740

Fig. 2 - Write cycle timing diagram.

DATA RETENTION CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$; See Fig. 3.

CHARACTERISTIC	TEST CONDITIONS	V_{DD} (V)	CDP1824		CDP1824C		UNITS
			Min.	Max.	Min.	Max.	
Data Retention Voltage, V_{DR}		—	2.5	—	2.5	—	V
Data Retention Quiescent Current, I_{DD}	$V_{DR} = 2.5\text{ V}$	—	—	10	—	40	μA
Chip Deselect to Data Retention Time, t_{CDR}	$V_{DR} = 2.5\text{ V}$	5	600	—	600	—	ns
		10	300	—	—	—	
Recovery to Normal Operation Time, t_{RC}	$V_{DR} = 2.5\text{ V}$	5	600	—	600	—	ns
		10	300	—	—	—	

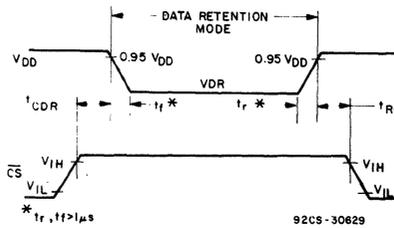


Fig. 3 - Low V_{DD} data retention waveforms and timing diagram.

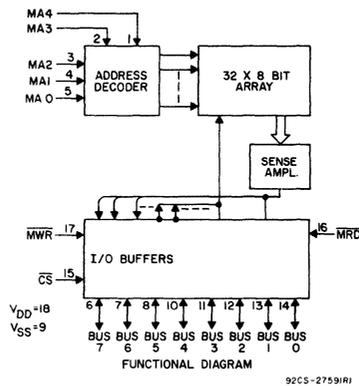


Fig. 4 - Functional diagram.

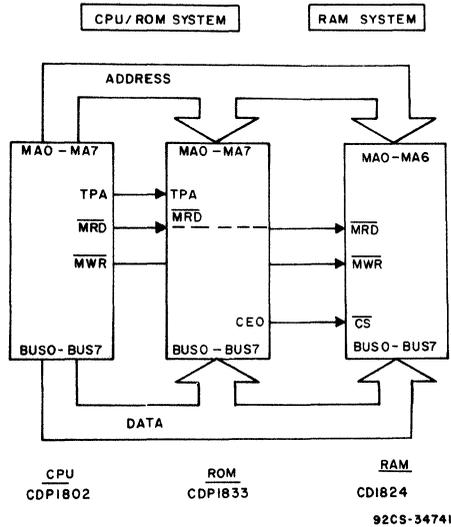


Fig. 5 - CDP1824 (128 x 8) minimum system (128 x 8)

OPERATING AND HANDLING CONSIDERATIONS

1. Handling

All inputs and outputs of RCA CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in ICAN-6525 "Guide to Better Handling and Operation of CMOS integrated Circuits."

2. Operating

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of

these conditions must not cause $V_{DD}-V_{SS}$ to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS} . Input currents must not exceed 10 mA even when the power supply is off.

Unused Inputs

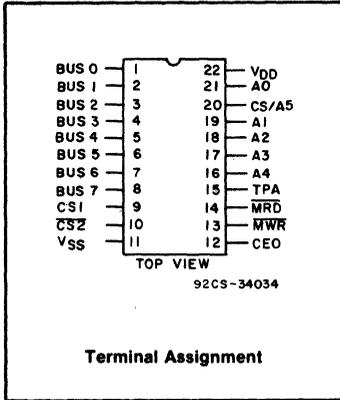
A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS} , whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} or V_{SS} may damage CMOS devices by exceeding the maximum device dissipation.

Preliminary Data

CMOS 64-Word x 8-Bit Static Random-Access Memory



Features:

- Compatible with CDP1800 and 4000-series devices
- Interfaces with CDP1800-series microprocessors without additional address decoding
- Daisy chain feature to further reduce external decoding needs
- Multiple chip-select inputs for versatility
- Single voltage supply
- No clock or precharge required

The RCA CDP1826C is a general-purpose, fully static, 64-word x 8-bit random-access memory, for use in CDP1800 series or other microprocessor systems where minimum component count and/or price performance and simplicity in use are desirable.

The CDP1826C has 8 common data input and data-output terminals with tristate capability for direct connection to a standard bi-directional data bus. Two chip-select inputs — CS1 and CS2 — are provided to simplify memory-system expansion. An additional select pin, CS/A5, is provided to enable the CDP1826C to be selected directly from the CDP1800 address bus without additional latching or decoding. In an 1800 system, the CS/A5 pin can be tied to any MA

address line from the CDP1800 processor. A TPA input is provided to latch the high-order bit of this address line as a chip-select for the CDP1826C. If this CS/A5 input is latched high, and if CS1=1 and CS2 = 0 at the appropriate time in the memory cycle, the CDP1826C will be enabled for writing or reading. In a non-1800 system, the TPA pin can be tied high, and the CS/A5 pin can be used as a normal address input.

The six input-address buffers are gated with the chip-select function to reduce standby current when the device is deselected, as well as to provide for a simplified power down mode by reducing address buffer sensitivity to long fall times from address drivers which are being powered down.

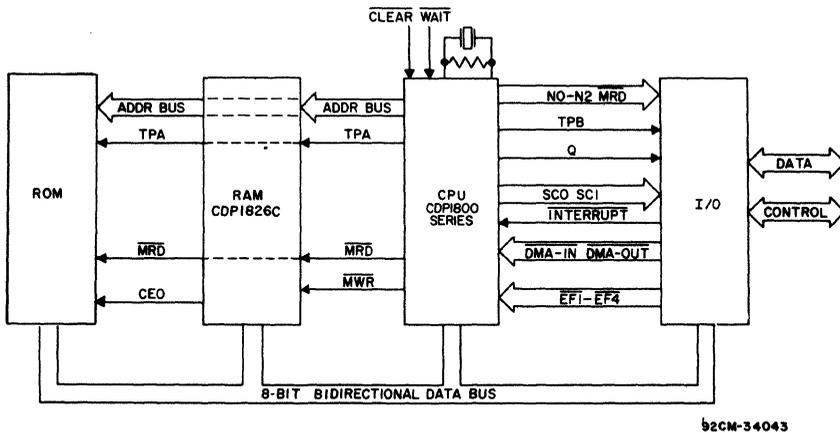


Fig. 1 - Typical CDP1802 microprocessor system.

RCA CMOS LSI Products

CDP1826C

Two memory control signals, $\overline{\text{MRD}}$ and $\overline{\text{MWR}}$, are provided for reading from and writing to the CDP1826C. The logic is designed so that $\overline{\text{MWR}}$ overrides $\overline{\text{MRD}}$, allowing the chip to be controlled from a single R/W line.

For such an interface, the $\overline{\text{MRD}}$ line can be tied to V_{SS} , with the $\overline{\text{MWR}}$ line connected to R/W.

A CHIP ENABLE OUTPUT is provided for daisy-chaining to additional memories. This output is high whenever the chip-select function selects the CDP1826C, which deselects any other chip which has its $\overline{\text{CS}}$ input connected to the CDP1826C CEO output. The connected chip is selected

when the CDP1826C is de-selected and the $\overline{\text{MRD}}$ input is low. Thus, the CEO is only active for a read cycle and can be set up so that a CEO of another device can feed the $\overline{\text{MRD}}$ of the CDP1826C, which in turn selects a third chip in the daisy chain.

The CDP1826C has a recommended operating voltage of 4.5 to 6.5 V and is supplied in 22-lead hermetic dual-in-line side-brazed ceramic packages (D suffix), in 22-lead dual-in-line plastic packages (E suffix). The CDP1826C is also available in chip form (H suffix).

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})	
(Voltages referenced to V_{SS} Terminal)	-0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to $V_{\text{DD}} + 0.5$ V
DC INPUT CURRENT, ANY ONE INPUT	± 10 mA
POWER DISSIPATION PER PACKAGE (P_{D}):	
For $T_{\text{A}} = -40$ to $+60^{\circ}\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_{\text{A}} = +60$ to $+85^{\circ}\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 12 mW/ $^{\circ}\text{C}$ to 200 mW
For $T_{\text{A}} = -55$ to $+100^{\circ}\text{C}$ (PACKAGE TYPE D)	500 mW
For $T_{\text{A}} = +100$ to $+125^{\circ}\text{C}$ (PACKAGE TYPE D)	Derate Linearly at 12 mW/ $^{\circ}\text{C}$ to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
For $T_{\text{A}} = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$	100 mW
OPERATING-TEMPERATURE RANGE (T_{A}):	
PACKAGE TYPE D	-55 to $+125^{\circ}\text{C}$
PACKAGE TYPE E	-40 to $+85^{\circ}\text{C}$
STORAGE TEMPERATURE RANGE (T_{stg})	-65 to $+150^{\circ}\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ inch (1.59 ± 0.79 mm) from case for 10 s max.	$+265^{\circ}\text{C}$

RECOMMENDED OPERATING CONDITIONS at $T_{\text{A}} = \text{Full Package Temperature Range}$.

For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

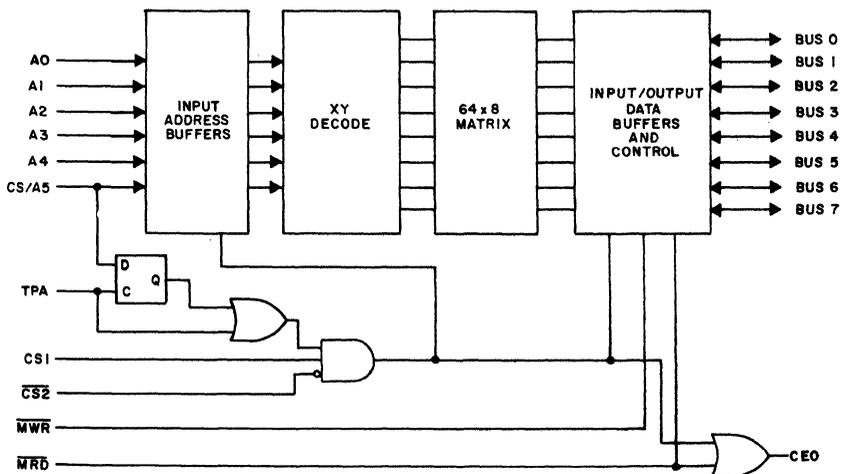
CHARACTERISTIC	LIMITS		UNITS
	CDP1826C		
	MIN.	MAX.	
DC Operating Voltage Range	4.5	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	
Input Signal Rise or Fall Time $V_{\text{DD}} = 5$ V	t_r, t_f	10	ms

STATIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} \pm 5\%$ except as noted

CHARACTERISTIC		CONDITIONS			LIMITS			UNITS
		V_o (V)	V_{IN} (V)	V_{DD} (V)	CDP1826C			
					MIN.	TYP.*	MAX.	
Quiescent Device Current	I_{DD}	—	0,5	5	—	5	50	μA
Output Low Drive (Sink) Current	I_{OL}	0.4	0,5	5	1	2	—	mA
Output High Drive (Source) Current	I_{OH}	4.6	0,5	5	-1	-1.5	—	
Output Voltage Low Level	V_{OL}	—	0,5	5	—	0	0.1	V
Output Voltage High Level	V_{OH}	—	0,5	5	4.9	5	—	
Input Low Voltage	V_{IL}	0.5,4.5	—	5	—	—	1.5	
Input High Voltage	V_{IH}	0.5,4.5	—	5	3.5	—	—	
Input Leakage Current	I_{IN}	Any Input	0,5	5	—	± 0.1	± 1	μA
3-State Output Leakage Current	I_{OUT}	0,5	0.5	5	—	± 0.1	± 1	
Operating Device Current	$I_{OPER}\dagger$	—	0,5	5	—	5	—	mA
Input Capacitance	C_{IN}	—	—	—	—	5	7.5	pF
Output Capacitance	C_{OUT}	—	0,5	5	—	10	15	

*Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .

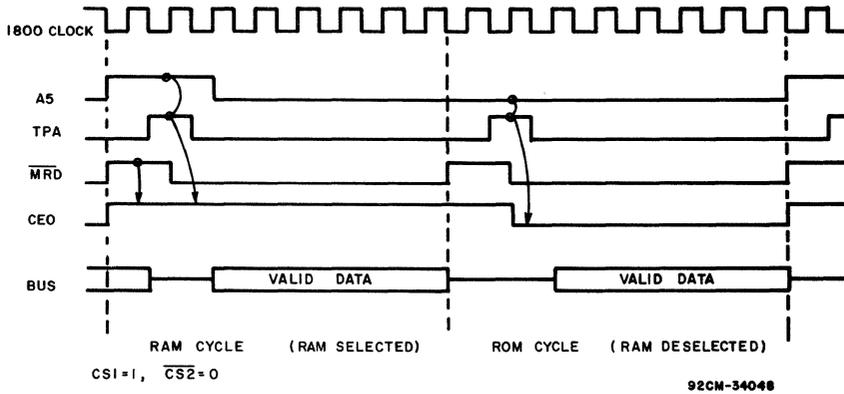
†Outputs open circuited; cycle times = 1 μs .



92CM-34044

Fig. 2 - Functional diagram.

RCA CMOS LSI Products
CDP1826C



		OPERATING MODES					
		MRD	MWR	CS1-CS2	TPA	CS/A5*	CEO
CDP1800 MODE	WRITE	X	0	1		1	1
	READ	0	1	1		1	1
	DESELECT	1	1	1		1	1
	DESELECT	1	X	0	X	X	1
	DESELECT	0	X	0	X	X	0
	DESELECT	1	X	X	X		0
DESELECT	0	X	X	X		0	0
NON-CDP1800 MODE	WRITE	X	0	1	1	X	1
	READ	0	1	1	1	X	1
	DESELECT	1	1	1	1	X	1
	DESELECT	1	X	0	1	X	1
	DESELECT	0	X	0	1	X	0

* FOR CDP1800 MODE, REFERS TO HIGH ORDER MEMORY ADDRESS BIT LEVEL AT TIME WHEN TPA TRANSITION TAKES PLACE

Fig. 3 - Chip Enable Output timing waveforms for CDP1800-based systems.

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = 5\text{ V} \pm 5\%$,

Input $t_r, t_f = 10\text{ ns}$; $C_L = 50\text{ pF}$ and 1 TTL Load

CHARACTERISTIC	LIMITS			UNITS	
	CDP1826C				
	MIN.†	TYP.●	MAX.		
Read — Cycle Times (Fig. 4)					
Address to TPA Setup	t_{ASH}	100	—	—	ns
Address to TPA Hold	t_{AH}	100	—	—	
Access from Address Change	t_{AA}	—	500	1000	
TPA Pulse Width	t_{PAW}	200	—	—	
Output Valid from MRD	t_{AM}	—	500	1000	
Access from Chip Select	t_{AC}	—	500	1000	
CEO Delay from TPA Edge	t_{CA}	—	150	300	
MRD to CEO Delay	t_{MC}	75	—	—	

†Time required by a limit device to allow for the indicated function.

●Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .

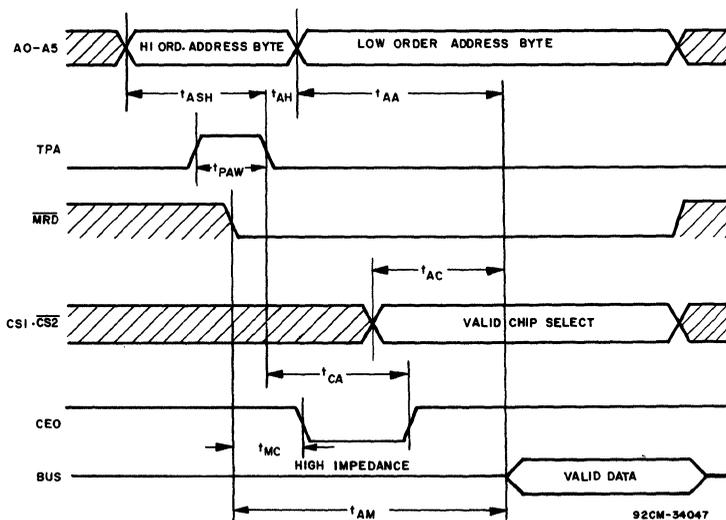


Fig. 4 - Read-cycle timing waveforms.

RCA CMOS LSI Products

CDP1826C

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = 5\text{ V} \pm 5\%$,

Input $t_r, t_f = 10\text{ ns}$; $C_L = 50\text{ pF}$ and 1 TTL Load

CHARACTERISTIC	LIMITS			UNITS	
	CDP1826C				
	MIN.†	TYP.●	MAX.		
Write-Cycle Times (Fig. 5)					
Address to TPA Setup, High Byte	t_{ASH}	100	—	—	ns
Address to TPA Hold	t_{AH}	100	—	—	
Address Setup Low Byte	t_{ASL}	500	250	—	
TPA Pulse Width	t_{PAW}	200	—	—	
Chip Select Setup	t_{CS}	700	350	—	
Write Pulse Width	t_{WW}	300	200	—	
Data Setup	t_{DS}	400*	200	—	
Data Hold	t_{DH}	100	50	—	

†Time required by a limit device to allow for the indicated function.

●Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .

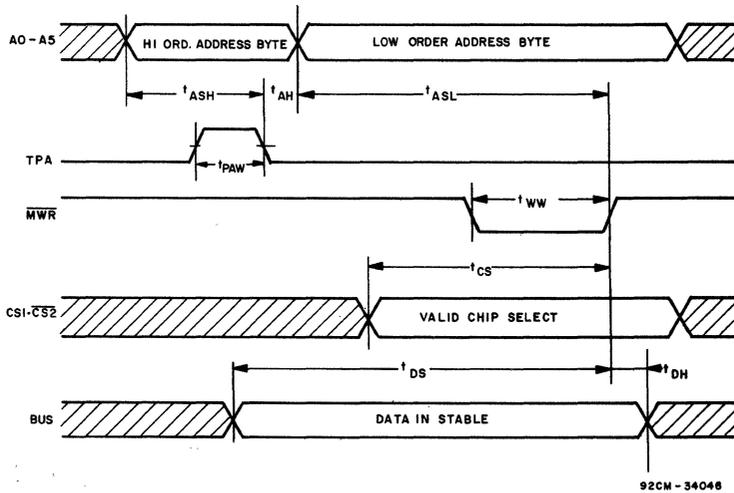


Fig. 5 - Write-cycle timing waveforms.

DATA RETENTION CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$; see Fig. 6

CHARACTERISTIC		TEST CONDI-TIONS		LIMITS			UNITS
		V_{DR} (V)	V_{DD} (V)	CDP1826C			
				MIN.	TYP.*	MAX.	
Min. Data Retention Voltage	V_{DR}	—	—	—	2	2.5	V
Data Retention Quiescent Current	I_{DD}	2.5	—	—	5	25	μA
Chip Deselect to Data Retention Time	t_{CDR}	—	5	600	—	—	ns
Recovery to Normal Operation Time	t_{RC}	—	5	600	—	—	
V_{DD} to V_{DR} Rise and Fall Time	t_r, t_f	2.5	5	1	—	—	μs

*Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .

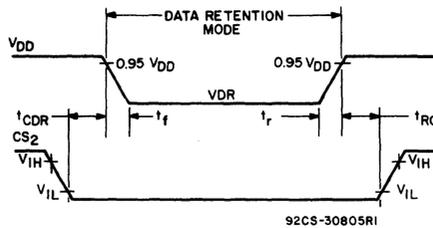
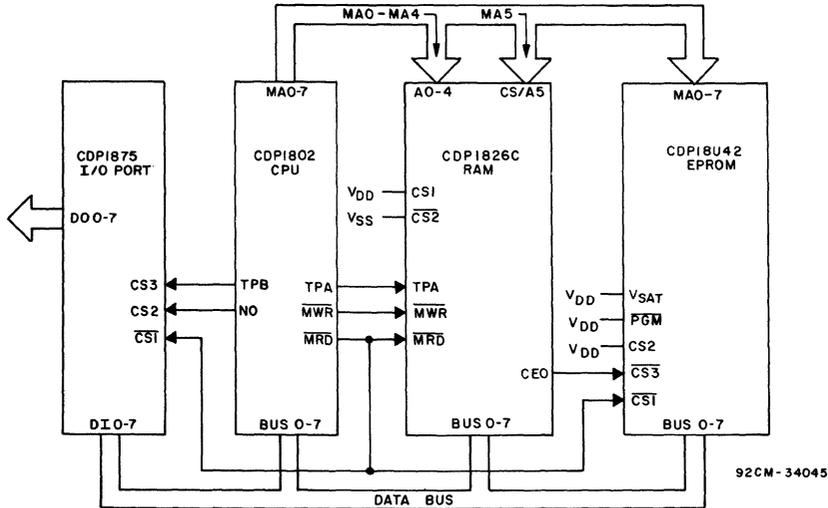


Fig. 6 - Low V_{DD} data retention timing waveforms.

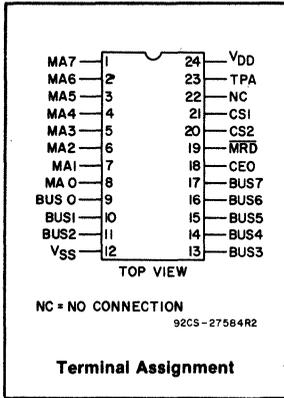


For the configuration shown, the RAM is mapped into locations 2000-3FFF with wrap-around at
6000-7FFF
A000-BFFF
E000-FFFF

The ROM is mapped into the first page of memory with wrap-around at all pages where $MA5.1 = 0$.

Note: Any address from MA0-MA5 can be connected to CS/A5 and still contiguously map 64 bytes of RAM — even though the address labels of the RAM do not match those of the CPU, the random access property of the RAM still results in proper operation.

Fig. 7 - A compact microcomputer system without external decoding.



512-Word x 8-Bit Static Read-Only Memory

Features:

- Compatible with CDP1800 and CD4000-series devices
- On-chip address latch
- Interfaces with CDP1802 microprocessor without additional components
- Optional programmable location within 64K memory space
- Three-state outputs

The RCA-CDP 1831 and CDP1831C types are 4096-bit mask-programmable CMOS read-only memories organized as 512 words x 8 bits and are completely static; no clocks required. They will directly interface with CDP1800-series micro-processors without additional components.

The CDP1831 and CDP1831C respond to 16-bit address multiplexed on 8 address lines. Address latches are provided on-chip to store the 8 most significant bits of the 16-bit address. By mask option, this ROM can be programmed to operate in any 512-word block within 64K memory space. The polarity of the high address strobe (TPA), and CS1 and CS2 are user mask-programmable. (See RPP-610, "ROM Sales Policy and Data Programming Instructions").

The Chip-Enable output signal (CEO) goes "high" when the device is selected, and is intended for use as an output disable control for RAM memory in a microprocessor system.

The CDP 1831C is functionally identical to the CDP1831. The CDP1831 has an operating voltage range of 4 to 10.5 volts, and the CDP1831C has an operating voltage range of 4 to 6.5 volts.

The CDP1831 and CDP1831C types are supplied in 24-lead hermetic dual-in-line, side-brazed ceramic packages (D suffix) and in 24-lead dual-in-line plastic packages (E suffix). The CDP1831C is also available in chip form (H suffix).

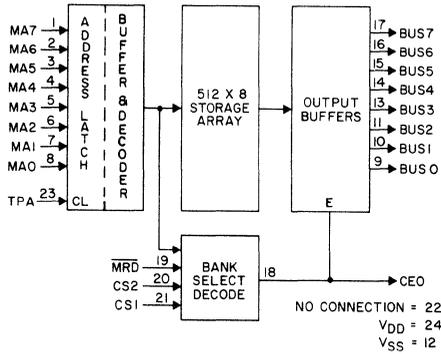


Fig. 1 - Functional diagram.

92CS-27587R3

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD}):

(All voltage values referenced to V_{SS} terminal)

CDP1831 -0.5 to +11 V
 CDP1831C -0.5 to +7 V

INPUT VOLTAGE RANGE, ALL INPUTS -0.5 to $V_{DD} + 0.5$ V

DC INPUT CURRENT, ANY ONE INPUT ± 10 mA

POWER DISSIPATION PER PACKAGE (P_D):

For $T_A = -40$ to $+60^\circ\text{C}$ (PACKAGE TYPE E) 500 mW

For $T_A = +60$ to $+85^\circ\text{C}$ (PACKAGE TYPE E) Derate Linearly at 12 mW/ $^\circ\text{C}$ to 200 mW

For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE D) 500 mW

For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE D) Derate Linearly at 12 mW/ $^\circ\text{C}$ to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE}$ 100 mW

OPERATING-TEMPERATURE RANGE (T_A)

PACKAGE TYPE D -55 to $+125^\circ\text{C}$

PACKAGE TYPE E -40 to $+85^\circ\text{C}$

STORAGE TEMPERATURE RANGE (T_{stg}) -65 to $+150^\circ\text{C}$

LEAD TEMPERATURE (DURING SOLDERING):

At distance $1/16 \pm 1/32$ inch (1.59 ± 0.79 mm) from case for 10 s max. $+265^\circ\text{C}$

OPERATING CONDITIONS at $T_A = \text{Full Package-Temperature Range}$. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1831		CDP1831C		
	Min.	Max.	Min.	Max.	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	

STATIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, Except as noted

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
	V_O	V_{IN}	V_{DD}	CDP1831			CDP1831C			
	(V)	(V)	(V)	Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device Current, I_{DD}	—	5	5	—	0.01	50	—	0.02	200	μA
	—	10	10	—	1	200	—	—	—	
Output Low Drive (Sink) Current, I_{OL}	0.4	0.5	5	0.55	—	—	0.55	—	—	mA
	0.5	0.10	10	1.30	—	—	—	—	—	
Output High Drive (Source) Current, I_{OH}	4.6	0.5	5	-0.35	—	—	-0.35	—	—	mA
	9.5	0.10	10	-0.65	—	—	—	—	—	
Output Voltage Low-Level, V_{OL}	—	0.5	5	—	0	0.1	—	0	0.1	V
	—	0.10	10	—	0	0.1	—	—	—	
Output Voltage High Level, V_{OH}	—	0.5	5	4.9	5	—	4.9	5	—	V
	—	0.10	10	9.9	10	—	—	—	—	
Input Low Voltage, V_{IL}	0.5, 4.5	—	5	—	—	1.5	—	—	1.5	V
	1.9	—	10	—	—	3	—	—	—	
Input High Voltage, V_{IH}	0.5, 4.5	—	5	3.5	—	—	3.5	—	—	V
	1.9	—	10	7	—	—	—	—	—	
Input Leakage Current, I_{IN}	Any	0.5	5	—	$\pm 10^{-4}$	± 1	—	—	± 1	mA
	Input	0.10	10	—	$\pm 10^{-4}$	± 2	—	—	—	
3-State Output Leakage Current, I_{OUT}	0.5	0.5	5	—	$\pm 10^{-4}$	± 1	—	—	± 1	mA
	0.10	0.10	10	—	$\pm 10^{-4}$	± 2	—	—	—	
Input Capacitance, C_{in}	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance, C_{out}	—	—	—	—	10	15	—	10	15	pF
Operating Current, $I_{DD1} \dagger$	—	0.5	5	—	5	10	—	5	10	mA
	—	0.10	10	—	10	20	—	—	—	

*Typical values are for "one" $T_A = 25^\circ\text{C}$ and nominal V_{DD}

†Outputs open-circuited; cycle time = 2.5 μs

RCA CMOS LSI Products
CDP1831, CDP1831C

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} \pm 5\%$,
 Input $t_r = 10$ ns, $C_L = 50$ pF, $R_L = 200\text{k}\Omega$

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS						UNITS
		CDP1831			CDP1831C			
		Min.†	Typ.*	Max.	Min.†	Typ.*	Max.	
Access Time from Address Change, t_{AA}	5	—	850	1000	—	850	1000	ns
	10	—	350	400	—	—	—	
Access Time from Chip Select, t_{ACS}	5	—	700	800	—	700	800	
	10	—	250	300	—	—	—	
Chip Select Delay, t_{CS}	5	—	600	—	—	600	—	
	10	—	200	300	—	—	—	
Address Setup Time, t_{AS}	5	50	—	—	50	—	—	
	10	25	—	—	—	—	—	
Address Hold Time, t_{AH}	5	150	—	—	150	—	—	
	10	75	—	—	—	—	—	
Read Delay, t_{MRD}	5	—	300	500	—	300	500	
	10	—	100	150	—	—	—	
Chip Enable Output Delay from Address, t_{CA}	5	—	500	600	—	500	600	
	10	—	200	250	—	—	—	
Bus Contention Delay, t_D	5	—	200	350	—	200	350	
	10	—	100	150	—	—	—	
TPA Pulse Width, t_{PAW}	5	200	—	—	200	—	—	
	10	70	—	—	—	—	—	

†Time required by a limit device to allow for the indicated function.

*Time required by a typical device to allow for the indicated function. Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .

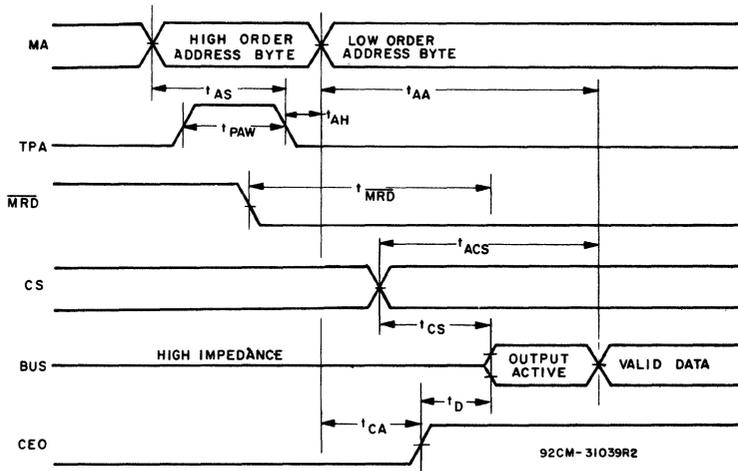
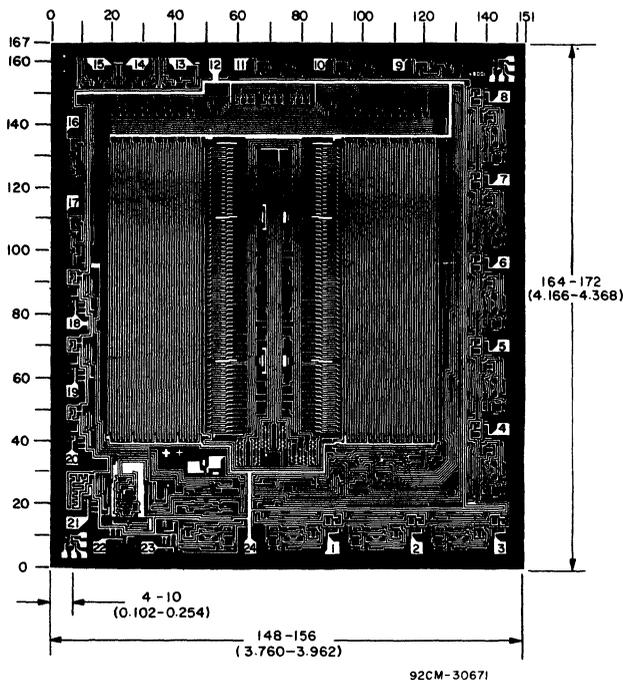


Fig. 2 - Timing waveforms.



Dimensions and pad layout for CDP1831CH chip.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Note:

The dynamic characteristics and timing diagrams indicate maximum performance capability of the CDP1831. When used directly with a CDP1800-series microprocessor, timing will be determined by the clock frequency and internal delays of the microprocessor.

The following general timing relationships will hold when the CDP1831 is used with a CDP1800-series microprocessor:

$$t_{AH} = 0.5 t_c$$

$$t_{PAW} = 1 t_c$$

\overline{MRD} occurs one clock period (t_c) earlier than the address bits MA0-MA7.

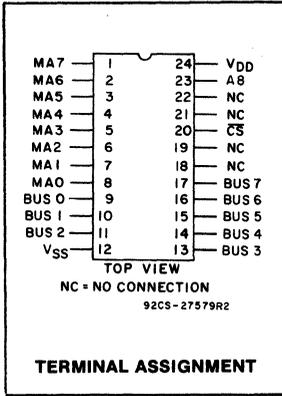
$$\text{where } t_c = \frac{1}{\text{CPU clock frequency}}$$

ORDERING INFORMATION

RCA Microprocessor device packages are identified by letters indicated in the following chart. When ordering a Microprocessor device, it is important that the appropriate suffix letter be affixed to the type number of the device.

Package	Suffix Letter
Dual-In-Line Side-Brazed	
Ceramic	D
Dual-In-Line Plastic	E
Chip	H

For example, a CDP1831 in a dual-in-line plastic package will be identified as the CDP1831E. A CDP1831C chip will be identified as the CDP1831CH.



512-Word x 8-Bit Static Read-Only Memory

- Features:**
- Compatible with CDP1800 and CD4000-series devices
 - Functional replacement for industry type 2704 512 x 8 EPROM
 - Three-state outputs

The RCA CDP1832 and CDP1832C types are 4096-bit mask-programmable CMOS read-only memories organized as 512 words x 8 bits and designed for use in CDP1800-series microprocessor systems. (See PD30, "ROM Purchase Policy and Data Programming Instructions.")

The CDP1832 ROM's are completely static; no clocks are required.

A Chip-Select input (\overline{CS}) is provided for memory expansion. Outputs are enabled when $\overline{CS}=0$.

The CDP1832 is a pin-for-pin compatible replacement for the industry types 2704 EPROM.

The CDP1832C is functionally identical to the CDP1832. The CDP1832 has a operating voltage range of 4 to 10.5 volts, and the CDP1832C has a operating voltage range of 4 to 6.5 volts.

The CDP1832 and CDP1832C are supplied in 24-lead, hermetic, dual-in-line, side-brazed, ceramic packages (D suffix) and in 24-lead dual-in-line plastic packages (E suffix). The CDP1832C is also available in chip form (H suffix).

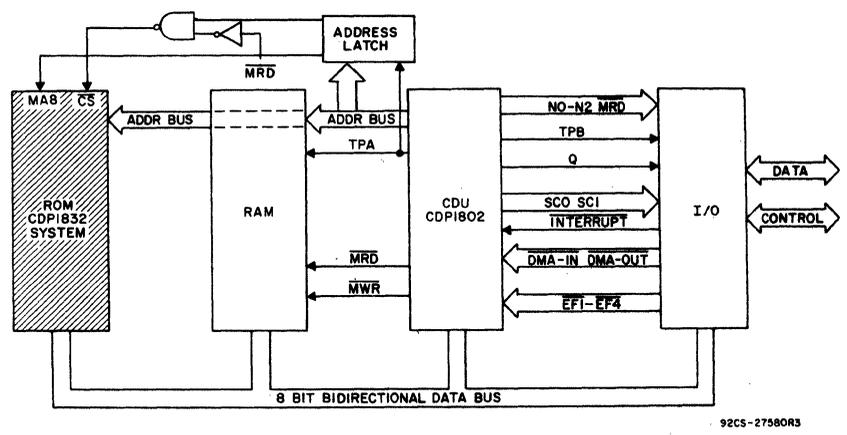


Fig. 1 - Typical CDP1802 microprocessor system.

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltage referenced to V_{SS} terminal)

CDP1832 -0.5 to +11 V
CDP1832C -0.5 to +7 V

INPUT VOLTAGE RANGE, ALL INPUTS -0.5 to V_{DD} +0.5 V

DC INPUT CURRENT, ANY ONE INPUT ±10 mA

POWER DISSIPATION PER PACKAGE (P_D):

For T_A=-40 to +60°C (PACKAGE TYPE E) 500 mW

For T_A=+60 to +85°C (PACKAGE TYPE E) Derate Linearly at 12 mW/°C to 200 mW

For T_A=-55 to +100°C (PACKAGE TYPE D) 500 mW

For T_A=+100 to 125°C (PACKAGE TYPE D) Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A=FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100 mW

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPE D -55 to +125°C

PACKAGE TYPE E -40 to +85°C

STORAGE TEMPERATURE RANGE (T_{stg}) -65 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. +265°C

OPERATING CONDITIONS at T_A=Full Package-Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1832		CDP1832C		
	Min.	Max.	Min.	Max.	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V _{SS}	V _{DD}	V _{SS}	V _{DD}	

STATIC ELECTRICAL CHARACTERISTICS at T_A=-40 to +85°C, V_{DD} ±5%, Except as noted

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)	CDP1832			CDP1832C			
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device Current, I _{DD}	—	5	5	—	0.01	50	—	0.02	200	μA
Current, I _{DD}	—	10	10	—	1	200	—	—	—	
Output Low Drive (Sink) Current, I _{OL}	0.4	0, 5	5	0.55	—	—	0.55	—	—	mA
	0.5	0, 10	10	1.30	—	—	—	—	—	
Output High Drive (Source) Current, I _{OH}	4.6	0, 5	5	-0.35	—	—	-0.35	—	—	mA
	9.5	0, 10	10	-0.65	—	—	—	—	—	
Output Voltage Low-Level, V _{OL}	—	0, 5	5	—	0	0.1	—	0	0.1	V
	—	0, 10	10	—	0	0.1	—	—	—	
Output Voltage High Level, V _{OH}	—	0, 5	5	4.9	5	—	4.9	5	—	V
	—	0, 10	10	9.9	10	—	—	—	—	
Input Low Voltage, V _{IL}	0.5, 4.5	—	5	—	—	1.5	—	—	1.5	V
	1, 9	—	10	—	—	3	—	—	—	
Input High Voltage, V _{IH}	0.5, 4.5	—	5	3.5	—	—	3.5	—	—	V
	1, 9	—	10	7	—	—	—	—	—	
Input Leakage Current, I _{IN}	Any Input	0, 5	5	—	±10 ⁻⁴	±1	—	±10 ⁻⁴	±1	μA
		0, 10	10	—	±10 ⁻⁴	±2	—	—	—	
3-State Output Leakage Current, I _{OUT}	0, 5	0, 5	5	—	±10 ⁻⁴	±1	—	±10 ⁻⁴	±1	μA
	0, 10	0, 10	10	—	±10 ⁻⁴	±2	—	—	—	
Input Capacitance, C _{IN}	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance, C _{OUT}	—	—	—	—	10	15	—	10	15	
Operating Device Current, I _{DD1} †	—	0, 5	5	—	5	10	—	5	10	mA
	—	0, 10	10	—	10	20	—	—	—	

*Typical values are for T_A=25°C and nominal V_{DD}.

†Outputs open-circuited; cycle time=2.5 μs.

RCA CMOS LSI Products
CDP1832, CDP1832C

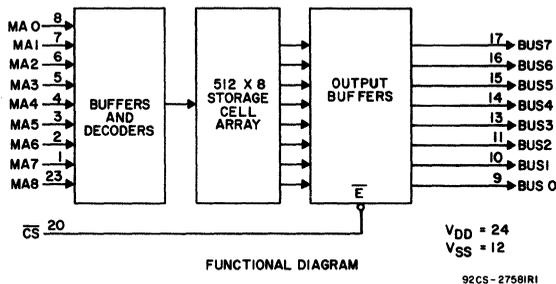


Fig. 2 - Functional diagram.

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} \pm 5\%$,
 Input $t_r, t_f = 10$ ns, $C_L = 50$ pF, $R_L = 200$ k Ω

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS						UNITS
		CDP1832			CDP1832C			
		Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Access Time From Address Change, t_{AA}	5	—	850	1000	—	850	1000	ns
Access Time From Chip Select, t_{ACS}	5	—	400	500	—	400	500	
Chip Select Delay, t_{CS}	5	—	200	250	—	200	250	
	10	—	100	130	—	—	—	

* Time required by a typical device to allow for the indicated function. Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .

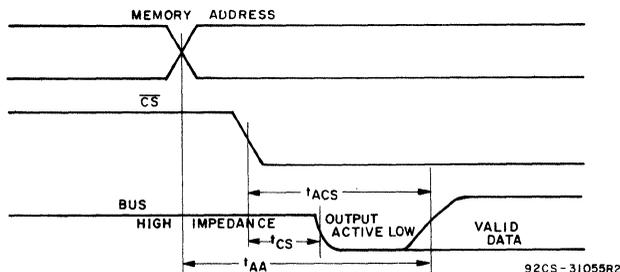


Fig. 3 - Timing waveforms.

OPERATING AND HANDLING CONSIDERATIONS

1. Handling

All inputs and outputs of RCA CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in ICAN-6525 "Guide to Better Handling and Operation of CMOS Integrated Circuits."

2. Operating

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause $V_{DD} - V_{SS}$

to exceed the absolute maximum rating.

Input Signals

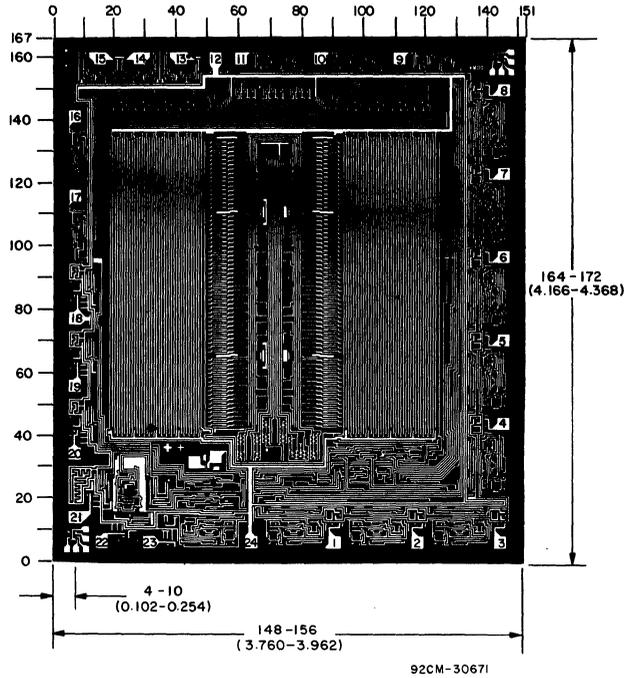
To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS} . Input currents must not exceed 10 mA even when the power supply is off.

Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS} , whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} or V_{SS} may damage CMOS devices by exceeding the maximum device dissipation.



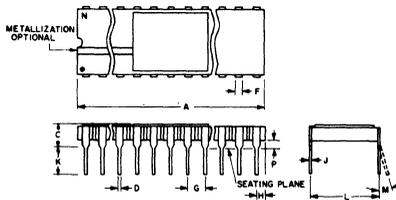
Dimensions and pad layout for CDP1832CH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

DIMENSIONAL OUTLINES

(D) SUFFIX
24-Lead Dual-In-Line Side-Braced Ceramic Package



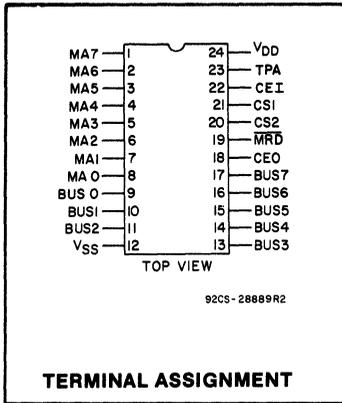
NOTES:

1. Leads within 0.005" (0.13 mm) radius of True Position at maximum material condition.
2. Center to center of leads when formed parallel.
3. When this device is supplied solder dipped, the maximum lead thickness (narrow portion) will not exceed 0.013" (0.33 mm).

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	1.180	1.220		29.98	30.98
C	0.085	0.145		2.16	3.68
D	0.015	0.023		0.39	0.58
F	0.040 REF.			1.02 REF.	
G	0.100 BSC		1	2.54 BSC	
H	0.030	0.070		0.77	1.77
J	0.008	0.012	3	0.21	0.30
K	0.125	0.175		3.18	4.44
L	0.580	0.620	2	14.74	15.74
M	— 7°			— 7°	
P	0.025	0.050		0.64	1.27
N	24			24	

92CS-30986R1

CDP1833, CDP1833C, CDP1833BC



CMOS 1024-Word x 8-Bit Static Read-Only Memory

Features:

- CDP1833BC is compatible with the CDP1802BC 5 MHz microprocessor
- On-chip address latch
- Interfaces with CDP1800-series microprocessors without additional components
- Optional programmable location within 64K memory space
- Three-state outputs

The RCA-CDP1833, CDP1833C, and CDP1833BC are static 8192-bit mask-programmable CMOS read-only memories organized as 1024-words x 8 bits and are completely static; no clocks are required. They will directly interface with the CDP1800-series microprocessors without additional components.

The CDP1833, CDP1833C, and CDP1833BC respond to a 16-bit address multiplexed on 8 address lines. Address latches are provided on-chip to store the 8 most significant bits of the 16-bit address. By mask option, this ROM can be programmed to operate in any 1024-word block within 64K memory space. The polarity of the high-address strobe (TPA), CEI, CS1, and CS2 are user mask-programmable. (See RPP-610, "Sales Policy and Data Programming Instructions", for RCA Custom ROMs).

The Chip-Enable output signal (CEO) is "high" when the device is selected. Terminals CEO and CEI can be connected in a daisy chain to control selection of RAM memory in a microprocessor system without additional components.

The CDP1833C and CDP1833BC are functionally identical to the CDP1833. The CDP1833 has a recommended operating voltage range of 4 to 10.5 volts, and the CDP1833C and CDP1833BC have a recommended operating voltage range of 4 to 6.5 volts. The CDP1833BC is designed to interface with the CDP1802BC microprocessor.

The CDP1833, CDP1833C, and CDP1833BC are supplied in 24-lead hermetic dual-in-line side-brazed ceramic package (D suffix) and 24-lead dual-in-line plastic package (E suffix). The CDP1833C is also available in chip form (H suffix).

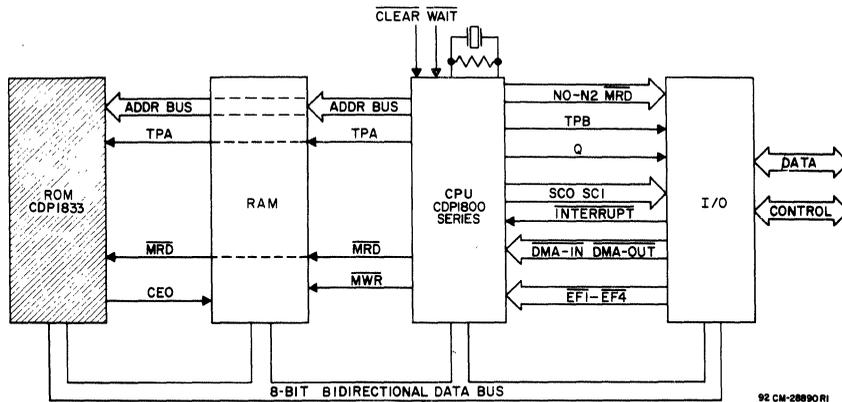


Fig. 1 - Typical CDP1800 Series microprocessor system.

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
 (Voltage referenced to V_{SS} terminal)

CDP1833 -0.5 to +11 V
 CDP1833C, CDP1833BC -0.5 to +7 V

INPUT VOLTAGE RANGE, ALL INPUTS -0.5 to V_{DD} + 0.5 V

DC INPUT CURRENT, ANY ONE INPUT ±10 mA

POWER DISSIPATION PER PACKAGE (P_D):

For T_A = -40 to +60° C (PACKAGE TYPE E) 500 mW
 For T_A = +60 to +85° C (PACKAGE TYPE E) Derate Linearly at 12 mW/°C to 200 mW
 For T_A = -55 to +100° C (PACKAGE TYPE D) 500 mW
 For T_A = +100 to 125° C (PACKAGE TYPE D) Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Packages) 10⁴

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPE D -55 to +125 °C
 PACKAGE TYPE E -40 to +85° C

STORAGE TEMPERATURE RANGE (T_{stg}) -65 to +150° C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. +265° C

OPERATING CONDITIONS at T_A = -40° to +85° C

For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1833		CDP1833C, CDP1833BC		
	Min.	Max.	Min.	Max.	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V _{SS}	V _{DD}	V _{SS}	V _{DD}	

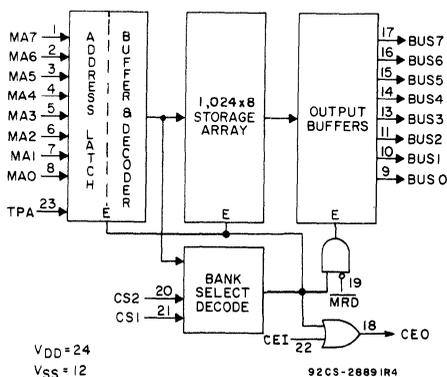


Fig. 2 - Functional diagram.

RCA CMOS LSI Products

CDP1833, CDP1833C, CDP1833BC

STATIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} \pm 5\%$, Except as noted

CHARACTERISTIC		CONDITIONS			LIMITS						UNITS
		V_o (V)	V_{IN} (V)	V_{DD} (V)	CDP1833			CDP1833C, CDP1833BC			
					Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device Current	I_{DD}	—	5	5	—	0.01	50	—	0.02	200	μA
		—	10	10	—	1	200	—	—	—	
Output Low Drive (Sink) Current	I_{OL}	0.4	0, 5	5	0.8	—	—	0.8	—	—	mA
		0.5	0, 10	10	1.8	—	—	—	—	—	
Output High Drive (Source) Current	I_{OH}	4.6	0, 5	5	-0.8	—	—	-0.8	—	—	mA
		9.5	0, 10	10	-1.8	—	—	—	—	—	
Output Voltage Low-Level	V_{OL}	—	0, 5	5	—	0	0.1	—	0	0.1	V
		—	0, 10	10	—	0	0.1	—	—	—	
Output Voltage High Level	V_{OH}	—	0, 5	5	4.9	5	—	4.9	5	—	V
		—	0, 10	10	9.9	10	—	—	—	—	
Input Low Voltage	V_{IL}	0.5, 4.5	—	5	—	—	1.5	—	—	1.5	V
		1, 9	—	10	—	—	3	—	—	—	
Input High Voltage	V_{IH}	0.5, 4.5	—	5	3.5	—	—	3.5	—	—	V
		1, 9	—	10	7	—	—	—	—	—	
Input Leakage Current	I_{IN}	Any	0, 5	5	—	$\pm 10^{-4}$	± 1	—	$\pm 10^{-4}$	± 1	μA
		Input	0, 10	10	—	$\pm 10^{-4}$	± 2	—	—	—	
3-State Output Current	I_{OUT}	0, 5	0, 5	5	—	$\pm 10^{-4}$	± 1	—	$\pm 10^{-4}$	± 1	μA
		0, 10	0, 10	10	—	$\pm 10^{-4}$	± 2	—	—	—	
Operating Device Current	I_{DD1}^\dagger	—	0, 5	5	—	7	10	—	7	10	mA
		—	0, 10	10	—	14	20	—	—	—	
Input Capacitance	C_{IN}	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance	C_{OUT}	—	—	—	—	10	15	—	10	15	pF

* Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .

† Outputs open-circuit; cycle time = 2.5 μs .

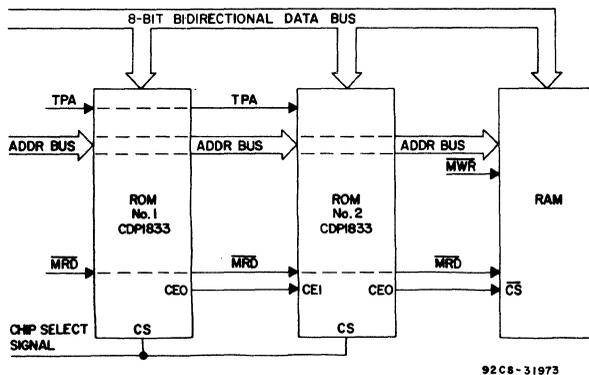


Fig. 3 - Daisy chaining CDP1833's.

"Daisy Chaining" with CEI inputs and CEO outputs is used to avoid memory conflicts between ROM and RAM in a user system. In the above configuration, if ROM #1 was masked-programmed for memory locations 0000-03FF₁₆ and ROM

#2 masked-programmed for memory locations 0400₁₆-07FF₁₆, for address from 0000-07FF₁₆ the RAM would be disabled and the ROM enabled. For locations above 07FF₁₆ the ROM's would be disabled and the RAM enabled.

CDP1833, CDP1833C, CDP1833BC

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} \pm 5\%$,
 Input $t_r = 10$ ns, $C_L = 50$ pF, $R_L = 200$ k Ω

CHARACTERISTIC	TEST CONDITIONS	LIMITS									UNITS
		CDP1833			CDP1833C			CDP1833BC			
		Min.#	Typ.*	Max.	Min.#	Typ.*	Max.	Min.#	Typ.*	Max.	
Access Time From Address Change t_{AA}	5	—	650	775	—	650	775	—	575	700	ns
	10	—	350	425	—	—	—	—	—	—	
Access Time From Chip Select t_{ACS}	5	—	500	625	—	500	625	—	475	600	
	10	—	275	310	—	—	—	—	—	—	
Chip Select Delay t_{CS}	5	—	250	320	—	250	320	—	250	320	
	10	—	125	180	—	—	—	—	—	—	
Address Setup Time t_{AS}	5	75	50	—	75	50	—	75	50	—	
	10	40	25	—	—	—	—	—	—	—	
Address Hold Time t_{AH}	5	100	75	—	100	75	—	75	50	—	
	10	50	30	—	—	—	—	—	—	—	
Read Delay t_{MRD}	5	—	400	500	—	400	500	—	400	500	
	10	—	200	275	—	—	—	—	—	—	
Chip Enable Output Delay from Address t_{CA}	5	—	120	170	—	120	170	—	120	170	
	10	—	70	100	—	—	—	—	—	—	
Bus Contention Delay t_D	5	—	220	270	—	220	270	—	220	270	
	10	—	130	150	—	—	—	—	—	—	
TPA Pulse Width t_{PAW}	5	200	—	—	200	—	—	175	—	—	
	10	70	—	—	—	—	—	—	—	—	
Chip Enable In to Chip Enable Out Delay t_{CEIO}	5	—	200	250	—	200	250	—	200	250	
	10	—	100	150	—	—	—	—	—	—	

Time required by a limit device to allow for the indicated function.

• Time required by a typical device to allow for the indicated function. Typical values are for $T_A = 25^\circ\text{C}$ and nominal voltages.

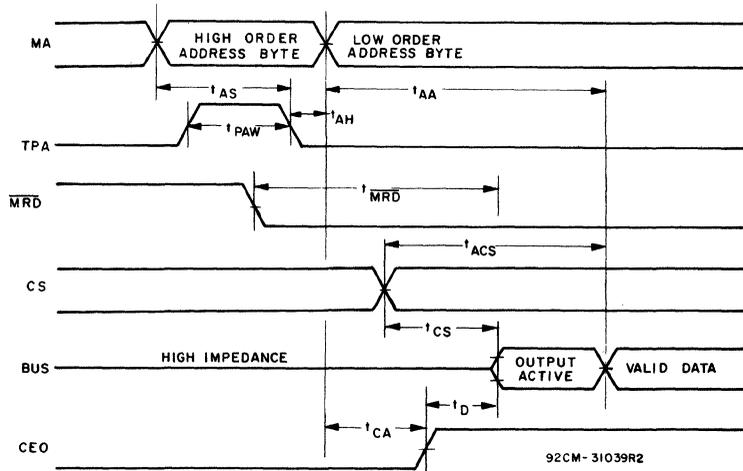
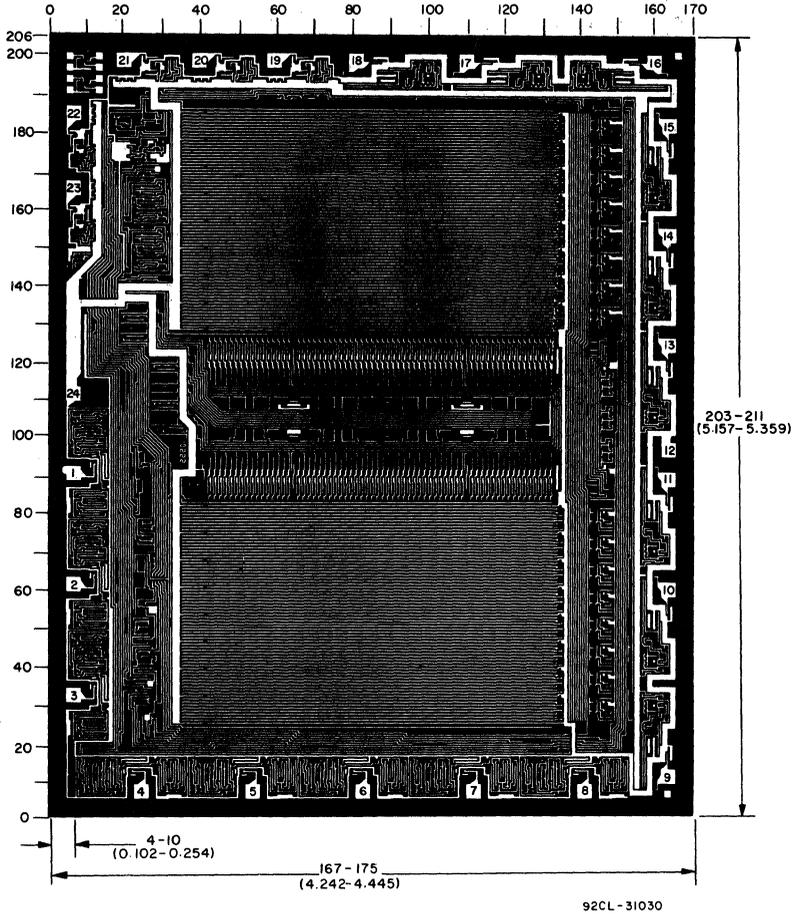


Fig. 4 - Timing waveforms.

RCA CMOS LSI Products
CDP1833, CDP1833C, CDP1833BC



Dimensions and pad layout for CDP1833CH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Note:

The dynamic characteristics and timing diagrams indicate maximum performance capability of the CDP1833. When used directly with a CDP1800-series microprocessor, timing will be determined by the clock frequency and internal delays of the microprocessor.

The following general timing relationships will hold when the CDP1833 is used with a CDP1800-series microprocessor.

$$t_{AH} = 0.5 t_c$$

$$t_{PAW} = 1 t_c$$

\overline{MRD} occurs one clock period (t_c) earlier than the address bits MA0-MA7.

$$\text{where } t_c = \frac{1}{\text{CPU clock frequency}}$$

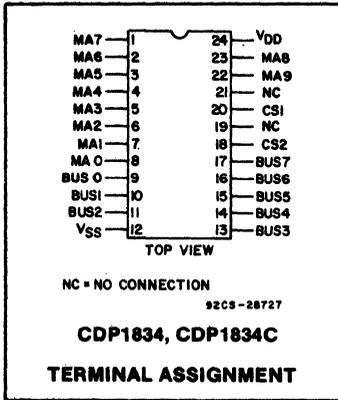
ORDERING INFORMATION

RCA Microprocessor device packages are identified by letters indicated in the following chart. When ordering a Microprocessor device, it is important that the appropriate suffix letter be affixed to the type number of the device.

Package	Suffix Letter
Dual-in-Line Side Brazed Ceramic	D
Dual-in-Line Plastic	E
Chip	H

For example, a CDP1833 in a dual-in-line plastic package will be identified as the CDP1833E. A CDP1833C chip will be identified as the CDP1833CH.

1028-Word x 8-Bit Static Read-Only Memory



Features

- Industry pin compatible
- Three-state outputs

The RCA-CDP1834 and CDP1834C are 8192-bit mask-programmable CMOS read-only memories organized as 1024-words x 8-bits and designed for use in CDP1800-series microprocessor systems. The CDP1834-series ROM's are completely static; no clocks are required.

Two Chip-Select inputs (CS1, CS2) are provided for memory expansion. The polarity of each Chip-Select is user mask-programmable. (See PD30, "ROM Purchase Policy and

Data Programming Instructions"). The CDP1834-series is pin-compatible with industry type 2708 EPROM. The CDP1834C is functionally identical to the CDP1834. The CDP1834 has a recommended operating voltage range of 4 to 10.5 volts and the CDP1834C has a recommended operating voltage range of 4 to 6.5 volts. The CDP1834 and the CDP1834C are supplied in 24-lead dual-in-line ceramic packages (D suffix) and in 24-lead dual-in-line plastic packages (E suffix). The CDP1834C is also available in chip form (H suffix).

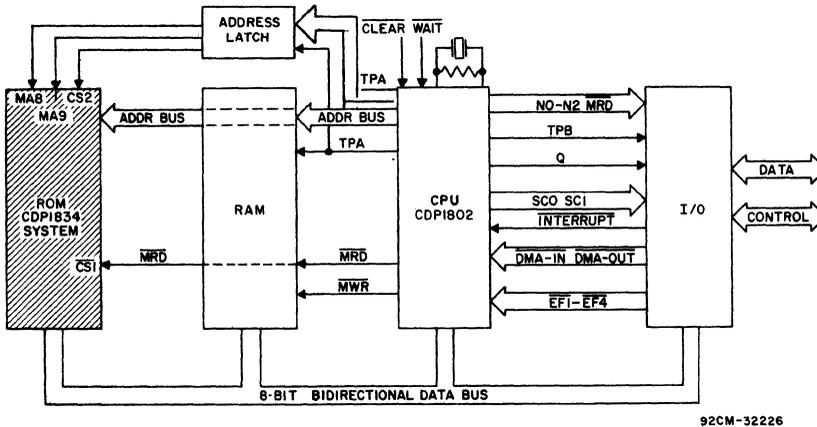


Fig. 1 - Typical CDP1802 microprocessor system.

RCA CMOS LSI Products

CDP1834, CDP1834C

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD}):

(All voltage values referenced to V_{SS} terminal)

CDP1834	0.5 to +11 V
CDP1834C	-0.5 to +7 V

INPUT VOLTAGE RANGE, ALL INPUTS -0.5 to V_{DD} +0.5 V

DC INPUT CURRENT, ANY ONE INPUT ±10 mA

POWER DISSIPATION PER PACKAGE (P_D):

For T_A = -40 to +60°C (PACKAGE TYPE E) 500 mW

For T_A = +60 to +85°C (PACKAGE TYPE E) Derate Linearly at 12 mW/°C to 200 mW

For T_A = -55 to +100°C (PACKAGE TYPE D) 500 mW

For T_A = 100 to +125°C (PACKAGE TYPE D) Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

For T_A = FULL PACKAGE-TEMPERATURE RANGE 100 mW

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPE D -55 to +125°C

PACKAGE TYPE E -40 to +85°C

STORAGE TEMPERATURE RANGE (T_{stg}) -65 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. +265°C

STATIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85°C, V_{DD} 5%, Except as noted

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)	CDP1834			CDP1834C			
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device Current I _{DD}	—	5	5	—	0.01	50	—	0.02	200	μA
	—	10	10	—	1	200	—	—	—	
Output Low Drive (Sink) Current I _{OL}	0.4	0, 5	5	0.8	—	—	0.8	—	—	mA
	0.5	0, 10	10	1.8	—	—	—	—	—	
Output High Drive (Source) Current I _{OH}	4.6	0, 5	5	-0.8	—	—	-0.8	—	—	mA
	9.5	0, 10	10	-1.8	—	—	—	—	—	
Output Voltage Low-Level V _{OL}	—	0, 5	5	—	0	0.1	—	0	0.1	V
	—	0, 10	10	—	0	0.1	—	—	—	
Output Voltage High Level V _{OH}	—	0, 5	5	4.9	5	—	4.9	5	—	V
	—	0, 10	10	9.9	10	—	—	—	—	
Input Low Voltage V _{IL}	0.5, 4.5	—	5	—	—	1.5	—	—	1.5	V
	1, 9	—	10	—	—	3	—	—	—	
Input High Voltage V _{IH}	0.5, 4.5	—	5	3.5	—	—	3.5	—	—	V
	1, 9	—	10	7	—	—	—	—	—	
Input Leakage Current I _{IN}	Any Input	0, 5	5	—	—	±1	—	—	±1	μA
		0, 10	10	—	—	±2	—	—	—	
3-State Output Leakage Current I _{OUT}	0, 5	5	5	—	—	±1	—	—	±1	μA
	0, 10	10	10	—	—	±2	—	—	—	
Input Capacitance C _{IN}	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance C _{OUT}	—	—	—	—	10	15	—	10	15	
Operating Device Current I _{DD1†}	—	0, 5	5	—	7	10	—	7	10	mA
	—	0, 10	10	—	14	20	—	—	—	

*Typical values are for T_A = 25°C and nominal V_{DD}.

†Outputs open-circuited; cycle time = 2.5 μs.

CDP1834, CDP1834C

OPERATING CONDITIONS at T_A = Full Package Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1834		CDP1834C		
	Min.	Max.	Min.	Max.	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	VSS	VDD	VSS	VDD	

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} \pm 5\%$, Input $t_r, t_f = 10$ ns, $C_L = 50$ pF, $R_L = 200$ k Ω

CHARACTERISTIC	TEST CONDITIONS VDD (V)	LIMITS						UNITS
		CDP1834			CDP1834C			
		Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Access Time from Address Change, t_{AA}	5	—	575	750	—	575	750	ns
	10	—	350	425	—	—	—	
Access Time from Chip Select, t_{ACS}	5	—	600	700	—	600	700	ns
	10	—	325	410	—	—	—	
Chip Select Delay, t_{CS}	5	—	480	580	—	480	580	ns
	10	—	250	340	—	—	—	

*Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .

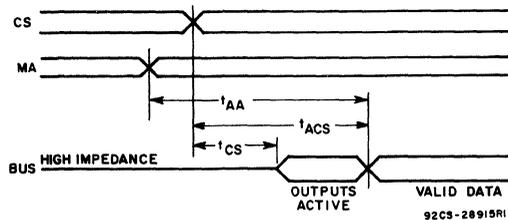


Fig. 2 - Timing waveforms.

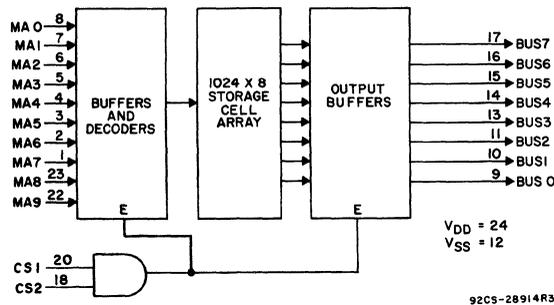
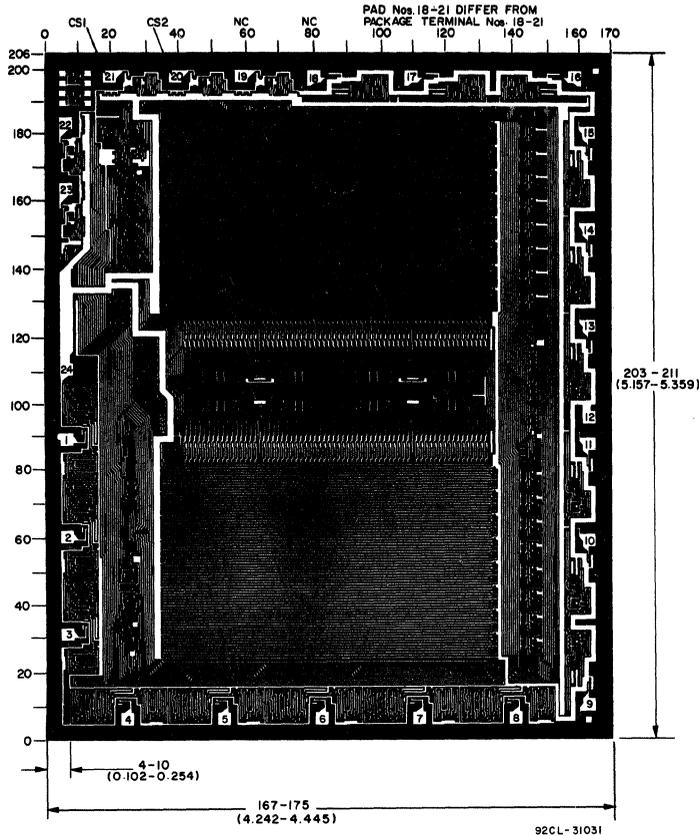


Fig. 3 - Functional diagram.

RCA CMOS LSI Products
CDP1834, CDP1834C



Dimensions and pad layout for CDP1834CH chip.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

OPERATING & HANDLING CONSIDERATIONS

1. Handling

All inputs and outputs of RCA CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in ICAN-6525 "Guide to Better Handling and Operation of CMOS Integrated Circuits".

2. Operating

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause $V_{DD} - V_{SS}$ to exceed the absolute maximum

rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS} . Input currents must not exceed 10 mA even when the power supply is off.

Unused Inputs

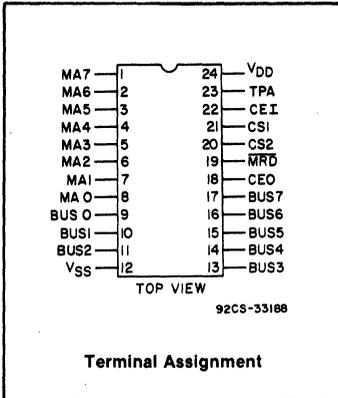
A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS} , whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} or V_{SS} may damage CMOS devices by exceeding the maximum device dissipation.

Objective Data

CMOS 2048-Word x 8-Bit Static Read-Only Memory



Features:

- Compatible with CDP1800- and CD4000-series devices
- On-chip address latch
- Interfaces with CDP1800-series microprocessors ($f_{CL} \leq 5$ MHz) without additional components
- Optional programmable location within 64K memory space
- 3-state outputs

The RCA CDP1835C is a 16384-bit mask-programmable CMOS read-only memory organized as 2048 words x 8 bits and is completely static; no clocks required. It will directly interface with CDP1800-series microprocessors that have clock frequencies up to 5 MHz without additional components.

The CDP1835C responds to 16-bit address multiplexed on 8 address lines. Address latches are provided on-chip to store the 8 most significant bits of the 16-bit address. By mask option, this ROM can be programmed to operate in any 2048-word block of 64K memory space. The polarity of the high address strobe (TPA), CEI, CS1 and CS2 are user mask-programmable.

(See Data Programming Instructions in this data sheet.)

The Chip-Enable output signal (CEO) is "high" when the device is selected. Terminals CEO and CEI can be connected in a daisy chain to control selection of RAM memory in a microprocessor system without additional components.

The CDP1835C has a recommended operating voltage range of 4 to 6.5 volts.

The CDP1835C is supplied in 24-lead hermetic dual-in-line side-brazed ceramic packages (D suffix) and 24-lead dual-in-line plastic packages (E suffix).

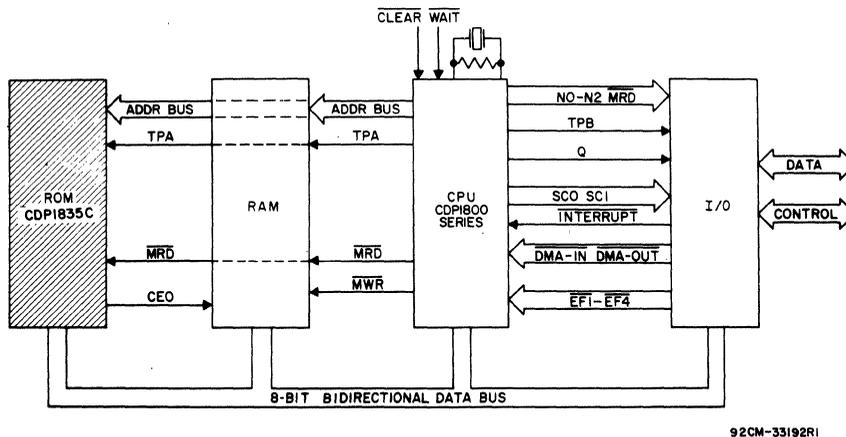


Fig. 1 — Typical CDP1800 Series microprocessor system.

RCA CMOS LSI Products

CDP1835C

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD}):

(All voltage values referenced to V_{SS} terminal)

CDP1835C	-0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to V_{DD} + 0.5 V
DC INPUT CURRENT, ANY ONE INPUT	± 10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For $T_A = -40$ to $+60^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +60$ to $+85^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 12 mW/ $^\circ\text{C}$ to 200 mW
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE D)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE D)	Derate Linearly at 12 mW/ $^\circ\text{C}$ to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE}$	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE D	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E	-40 to $+85^\circ\text{C}$
STORAGE TEMPERATURE RANGE (T_{stg})	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ inch (1.59 ± 0.79 mm) from case for 10 s max.	$+265^\circ\text{C}$

OPERATING CONDITIONS at $T_A = \text{Full Package Temperature}$

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	CDP1835C		
	MIN.	MAX.	
DC Operating Voltage Range	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	

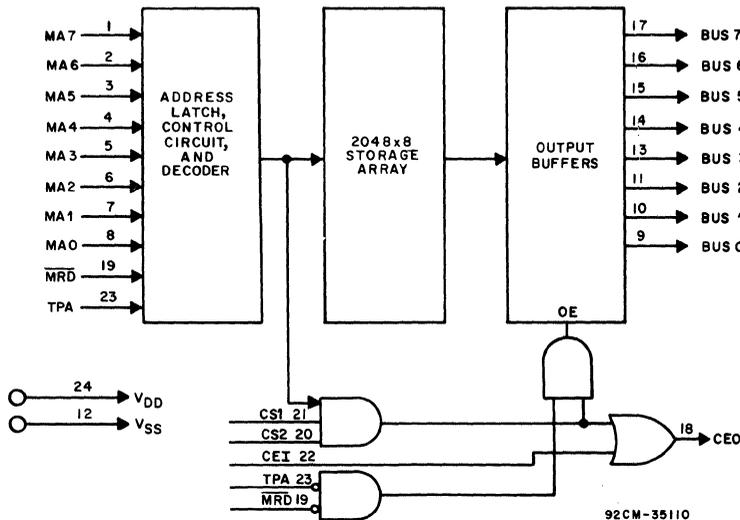


Fig. 2 — Functional diagram.

STATIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} \pm 5\%$, except as noted

CHARACTERISTIC	TEST CONDITIONS			LIMITS			UNITS
	V_o (V)	V_{in} (V)	V_{DD} (V)	CDP1835C			
				MIN.	TYP.*	MAX.	
Quiescent Device Current I_{DD}	—	5	5	—	5	50	μA
Output Low Drive (Sink) Current I_{OL}	0.4	0.5	5	0.8	1.6	—	mA
Output High Drive (Source Current) I_{OH}	4.6	0.5	5	-0.8	-1.6	—	
Output Voltage Low-Level V_{OL}	—	0.5	5	—	0	0.1	V
Output Voltage High-Level V_{OH}	—	0.5	5	4.9	5	—	
Input Low Voltage V_{IL}	0.5,4.5	—	5	—	—	1.5	V
Input High Voltage V_{IH}	0.5,4.5	—	5	3.5	—	—	
Input Leakage Current (Any Input) I_{IN}	—	0.5	5	—	—	± 1	μA
3-State Output Leakage Current I_{OUT}	0.5	0.5	5	—	—	± 2	
Input Capacitance C_{IN}	—	—	—	—	5	7.5	pF
Output Capacitance C_{OUT}	—	—	—	—	10	15	
Operating Device Current I_{OPER} ■	—	0.5	5	—	5	10	mA

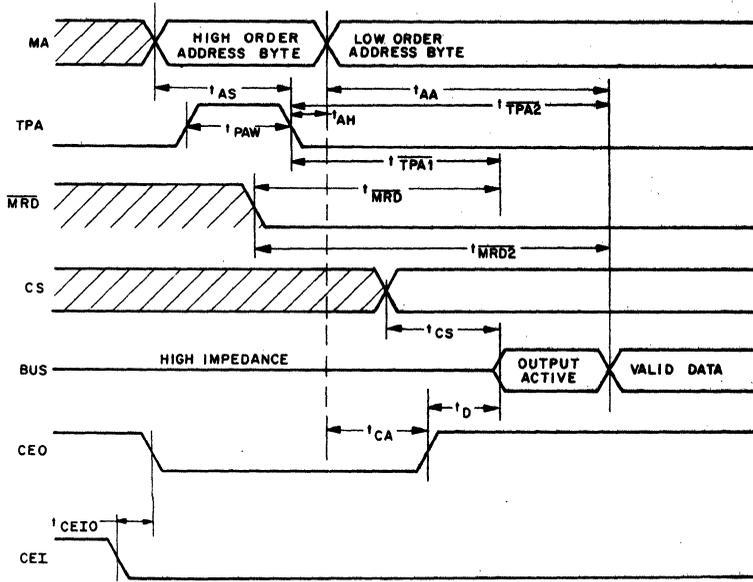
*Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .■Outputs open circuited; cycle time = 1 μs .**DYNAMIC ELECTRICAL CHARACTERISTICS** at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} \pm 5\%$,Input t_r , $t_f = 10$ ns, $C_L = 100$ pF, 1 TTL Load

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS			UNITS
		CDP1835C			
		MIN.†	TYP.*	MAX.	
Access Time from Address Change t_{AA}	5	—	—	550	ns
Chip Select Delay t_{CS}	5	—	—	200	
Address Setup Time t_{AS}	5	50	—	—	
Address Hold Time t_{AH}	5	70	—	—	
Output Active from MRD t_{MRD1}	5	—	—	100	
Output Valid from MRD t_{MRD2}	5	—	—	600	
Output Active from TPA t_{TPA1}	5	—	—	100	
Output Valid from TPA t_{TPA2}	5	—	—	60	
Chip Enable Output Delay from Address t_{CA}	5	—	—	100	
Bus Contention Delay t_D	5	—	—	200	
TPA Pulse Width t_{PAW}	5	125	—	—	
Chip Enable In to Chip Enable Out Delay t_{CEIO}	5	—	—	100	

*Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .

†Time required by a limit device to allow for the indicated function.

RCA CMOS LSI Products
CDP1835C



92CM-33191R2

Fig. 3 — Timing waveforms.

Note:

The dynamic characteristics and timing diagrams indicate maximum performance capability of the CDP1835C. When used directly with a CDP1800-series microprocessor, timing will be determined by the clock frequency and internal delays of the microprocessor.

The following general timing relationships will hold when

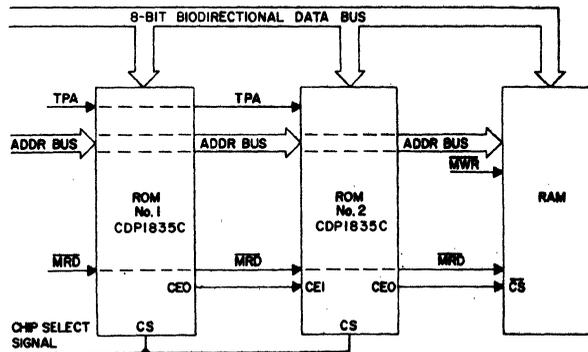
the CDP1835C is used with a CDP1800-series microprocessor.

$$t_{AH} = 0.5 t_c$$

$$t_{PAW} = 1.0 t_c$$

MRD occurs one clock period (t_c) earlier than the address bits MA0-MA7.

$$\text{where } t_c = \frac{1}{\text{CPU clock frequency}}$$



92CS-33190R1

Fig. 4 — Daisy chaining CDP1835C.

"Daisy Chaining" with CEI inputs and CEO outputs is used to avoid memory conflicts between ROM and RAM in a user system. In the above configuration, if ROM No. 1 was masked-programmed for memory locations 0000-07FF₁₆ and ROM No. 2 masked-programmed for memory locations

0800₁₆-0FFF₁₆, for addresses from 0000-0FFF₁₆, the RAM would be disabled and the ROM enabled. For locations above 0FFF₁₆, the ROMs would be disabled and the RAM enabled.

ROM ORDERING INFORMATION

All RCA mask-programmable ROMs are custom-ordered devices. ROM program patterns can be submitted to RCA by using master device (ROM, PROM or EPROM), a floppy diskette generated on an RCA development system, or computer punch cards.

For detailed instructions, refer to the ROM Information Sheet for the CDP1835C and publication "Sales Policy and Data Programming Instructions," RPP-610. (Note polarity options, columns 41 and 42, Part B, on the CDP1835C ROM Information Sheet must be blank).

ROM INFORMATION SHEET

How is ROM pattern being submitted to RCA?

- check one **Computer Cards** (Complete part B, C, and D)
Floppy Diskette (Complete parts A, B, C, D, and F)
Master Device (PROM) (Complete parts A, B, C, D, and E)

PART A	6-30	Customer Name (start at left)																			
	35-54																Address or Division				
	59-63	RCA Custom Number (Obtained from RCA Sales Office)																			
	65-71	ROM Type (without CDP prefix), e.g. 1835C																			

PART B	ROM TYPE	Circle one letter (P, N, or X) In each column (Single Letter Indicates No Choice) P = active when logic 1, N = active when logic 0, X = don't care												
	Pin Functions	CS1	CS2			CE1	TPA	A15	A14	A13	A12	A11	A10	A9
	CDP1835C Polarity Options	PNX	PNX	N	X	PX	PN	PNX	PNX	PNX	PNX	PNX		
Column #	28	29	30	31	32	34	36	37	38	39	40	41	42	

PART C	Positive or Negative Logic?
	POS or NEG <input type="checkbox"/> <input type="checkbox"/>

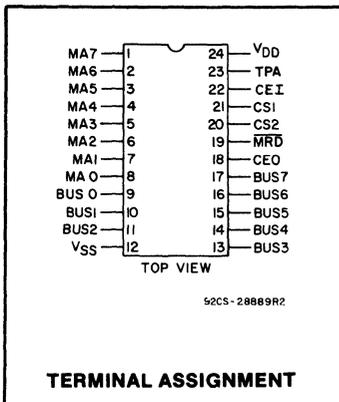
PART D	Starting address of ROM pattern in Hex.
	<input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/>

PART E	If a master device is submitted, state type of ROM/PROM:
	Starting and last address of data block in the Master Device (in Hex).
	<input type="checkbox"/>

PART F	If a diskette is submitted, check type of RCA Development System used:	
	<input type="checkbox"/> CDP18S005	<input type="checkbox"/> CDP18S007
	<input type="checkbox"/> CDP18S008	<input type="checkbox"/> CDP18S008
	Specify: Track # <input type="checkbox"/> <input type="checkbox"/>	Specify: File Name:
	Software program used: (check one)	(check one)
	<input type="checkbox"/> ROM SAVE	<input type="checkbox"/> MEM SAVE
<input type="checkbox"/> SAVE PROM	<input type="checkbox"/> SAVE PROM	

Objective Data

4096-Word x 8-Bit Static Read-Only Memory

**Features:**

- On-chip address latch
- Interfaces with CDP1800-series microprocessors ($f_{clock} \leq 5$ MHz) without additional components
- Optional programmable location within 64K memory space
- Three-state outputs

The RCA-CDP1837C is a 32768-bit mask-programmable CMOS read-only memory, organized as 4096 words x 8 bits and is completely static: no clocks required. It will directly interface with CDP1800-series microprocessors, having clock frequencies up to 5 MHz, without additional components.

The CDP1837C responds to a 16-bit address multiplexed on 8 address lines. Address latches are provided on chip for storing the high byte address data. By mask option, this ROM can be programmed to operate in any 4096-word block of 64-K memory space. The polarity of the high address strobe (TPA), MRD, CEI, CS1, and CS2 are user mask-programmable.

(See RPP-610, "Sales Policy and Data Programming Instructions", for RCA custom ROM's).

The Chip-Enable output signal (CEO) is "high" when the device is selected. Terminals CEO and CEI can be connected in a daisy chain to control selection of RAM memory in a microprocessor system without additional components.

The CDP1837C has a recommended operating voltage range of 4 to 6.5 volts.

The CDP1837C is supplied in 24-lead hermetic dual-in-line side-brazed ceramic packages (D suffix) and 24-lead dual-in-line plastic packages (E suffix).

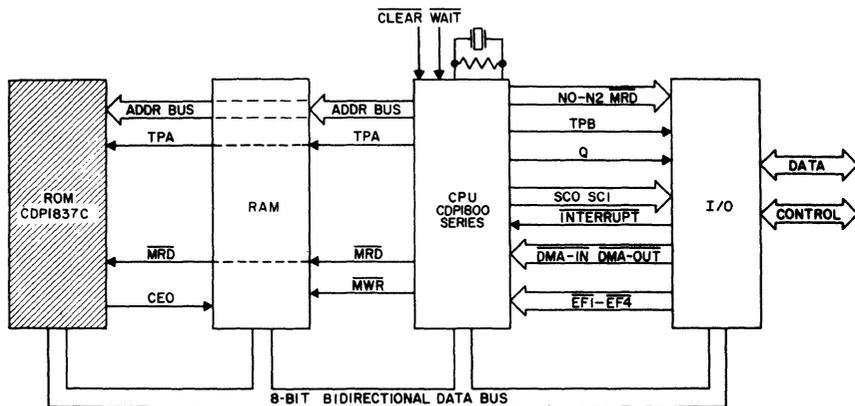


Fig. 1 - Typical CDP1800 Series microprocessor system.

92CM-35/20

CDP1837C

MAXIMUM RATING, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD}):
 (All voltages referenced to V_{SS} terminal)
 CDP1837C -0.5 to +7 V

INPUT VOLTAGE RANGE, ALL INPUTS -0.5 to V_{DD} +0.5 V

DC INPUT CURRENT, ANY ONE INPUT ±10 mA

POWER DISSIPATION PER PACKAGE (P_D):
 For T_A = -40 to +60°C (PACKAGE TYPE E) 500 mW
 For T_A = +60 to +85°C (PACKAGE TYPE E) Derate Linearly at 12 mW/°C to 200 mW
 For T_A = -55 to +100°C (PACKAGE TYPE D) 500 mW
 For T_A = +100 to +125°C (PACKAGE TYPE D) Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR
 For T_A = FULL PACKAGE-TEMPERATURE RANGE 100 mW

OPERATING-TEMPERATURE RANGE (T_A):
 PACKAGE TYPE D -55 to +125°C
 PACKAGE TYPE E -40 to +85°C

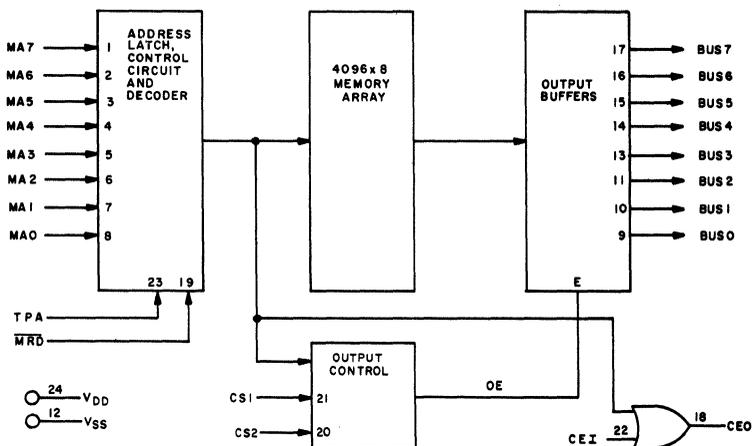
STORAGE TEMPERATURE RANGE (T_{stg}) -65 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):
 At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. +265°C

OPERATING CONDITIONS at T_A = FULL PACKAGE-TEMPERATURE RANGE

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	CDP1837C		
	MIN.	MAX.	
Supply-Voltage Range	4	6.5	V
Recommended Input Voltage Range	V _{SS}	V _{DD}	



92CM-35121

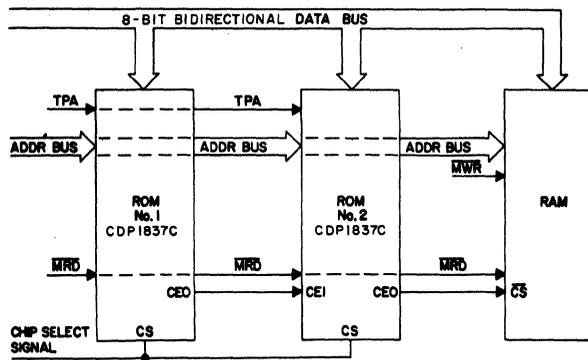
Fig. 2 - Functional block diagram.

STATIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} \pm 5\%$, except as noted

CHARACTERISTIC		CONDITIONS			LIMITS			UNITS
		V_O (V)	V_{IN} (V)	V_{DD} (V)	CDP1837C			
					Min.	Typ.*	Max.	
Quiescent Device Current	I_{DD}	—	0, 5	5	—	5	50	μA
Output Low Drive (Sink) Current	I_{OL}	0.4	0, 5	5	0.8	1.6	—	mA
Output High Drive (Source) Current	I_{OH}	4.6	0, 5	5	-0.8	-1.6	—	
Output Voltage Low-Level	V_{OL}	—	0, 5	5	—	0	0.1	V
Output Voltage High-Level	V_{OH}	—	0, 5	5	4.9	5	—	
Input Low Voltage	V_{IL}	0.5, 4.5	—	5	—	—	1.5	
Input High Voltage	V_{IH}	0.5, 4.5	—	5	3.5	—	—	
Input Current	I_{IN}	—	0, 5	5	—	—	± 1	μA
3-State Output Leakage Current	I_{OUT}	0, 5	0, 5	5	—	—	± 2	
Operating Current, 1 MHz	I_{DD1} •	—	0, 5	5	—	5	10	mA
Input Capacitance	C_{IN}	—	—	—	—	5	7.5	pF
Output Capacitance	C_{OUT}	—	—	—	—	10	15	

*Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .

•Outputs open circuited; cycle time 1 μs .



92CS-35122

Fig. 3 - Daisy chaining CDP1837C's.

"Daisy Chaining" with CEI inputs and CEO outputs is used to avoid memory conflicts between ROM and RAM in a user system. In the above configuration, if ROM No. 1 was masked-programmed for memory locations 0000-07FF₁₆

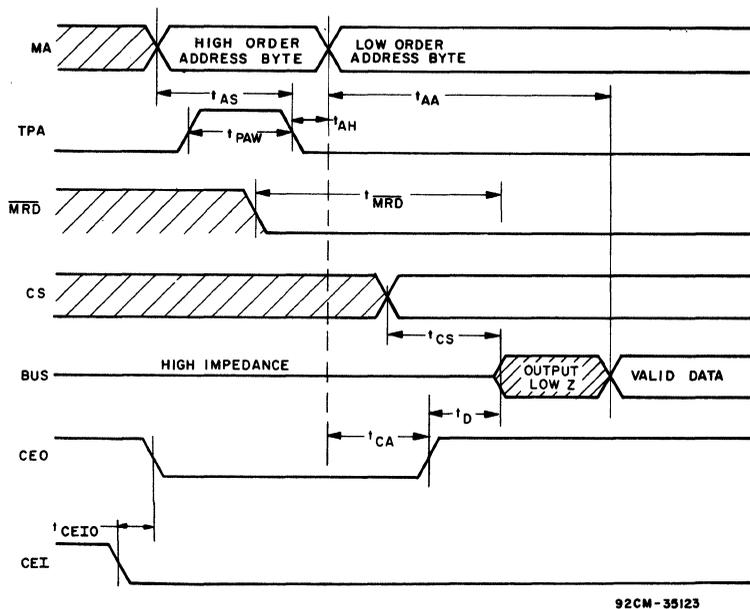
and ROM No. 2 masked-programmed for memory locations 0800₁₆-0FFF₁₆, for addresses from 0000-0FFF₁₆, the RAM would be disabled and the ROM, enabled. For locations above 0FFF₁₆, the ROM's would be disabled and the RAM enabled.

RCA CMOS LSI Products
CDP1837C

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} +5\%$,
 Input $t_r = 10$ ns, $C_L = 100$ pF, and 1 TTL Load

CHARACTERISTIC	CONDITIONS V_{DD} (V)	LIMITS		UNITS	
		CDP1837C			
		Min.#	Max.		
Access Time from Address Change	t_{AA}	5	—	550	ns
Chip Select Delay	t_{CS}	5	—	200	
Address Setup Time	t_{AS}	5	50	—	
Address Hold Time	t_{AH}	5	70	—	
Read Delay	t_{MRD}	5	—	200	
Chip Enable Output Delay from Address	t_{CA}	5	—	100	
Bus Contention Delay	t_D	5	—	200	
TPA Pulse Width	t_{PAW}	5	125	—	
Chip Enable In to Chip Enable Out Delay	t_{CEIO}	5	—	100	

Time required by a limit device to allow for the indicated function.



92CM-35123

Fig. 4 - Timing diagram.

Note:

The dynamic characteristics and timing diagrams indicate maximum performance capability of the CDP1837C. When used directly with a CDP1800-series microprocessor, timing will be determined by the clock frequency and internal delays of the microprocessor.

The following general timing relationships will hold when the CDP1837C is used with a CDP1800-series microprocessor.

$$t_{AH} = 0.5 t_c$$

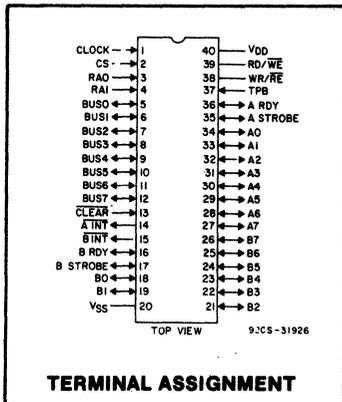
$$t_{PAW} = 1.0 t_c$$

\overline{MRD} occurs one clock period (t_c) earlier than the address bits MA0-MA7.

$$\text{where } t_c = \frac{1}{\text{CPU clock frequency}}$$

1800-Series Pheripherals Technical Data

4



CMOS Programmable I/O Interface

Features:

- 20 Programmable I/O Lines
- Programmable for Operation in Four Modes:
 - Input
 - Output
 - Bidirectional
 - Bit-programmable
- Operates in Either I/O or Memory Space

The RCA CDP1851 and CDP1851C are CMOS programmable two-port I/Os designed for use as general-purpose I/O devices. They are directly compatible with CDP1800 series microprocessors functioning at maximum clock frequency. Each port can be programmed in either byte-I/O or bit-programmable modes for interfacing with peripheral devices such as printers and keyboards.

Both ports A and B can be separately programmed to be 8 bit input or output ports with handshaking control lines, RDY and STROBE. Only port A can be programmed to be a bidirectional port. This configuration provides a means for communicating with a peripheral device or microprocessor system on a single 8 bit bus for both transmitting and receiving data. Handshaking signals are provided to maintain proper bus access control. Port A handshaking

lines are used for input control and port B handshaking lines are used for output; therefore port B must be in the bit-programmable mode where handshaking is not used.

Ports A and B can be separately bit programmed so that each individual line can be designated as an input or output line. The handshaking lines may also be individually programmed as input or output when port A is not in bidirectional mode.

The CDP1851 has a supply-voltage range of 4 to 10.5 V, and the CDP1851C has a range of 4 to 6.5 V. Both types are supplied in 40-lead dual-in-line plastic (E suffix) or hermetic ceramic (D suffix) packages. The CDP1851C is also available in chip form (H suffix).

CDP1851 Programming Modes

Mode	(8) Port A Data Pins	(2) Port A Handshaking Pins	(8) Port B Data Pins	(2) Port B Handshaking Pins
Input	Accept input data	READY, STROBE	Accept input data	READY, STROBE
Output	Output data	READY, STROBE	Output data	READY, STROBE
Bidirectional (Port A only)	Transfer input/ output data	Input handshaking for Port A	Must be previously set to bit-programmable mode	Output handshaking for Port A
Bit- Programmable	Programmed individually as inputs or outputs	Programmed individually as inputs or outputs	Programmed individually as inputs or outputs	Programmed individually as inputs or outputs

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
 (Voltage referenced to V_{SS} Terminal)
 CDP1851 -0.5 to +11 V
 CDP1851C -0.5 to +7 V

INPUT VOLTAGE RANGE, ALL INPUTS -0.5 to V_{DD} +0.5 V

DC INPUT CURRENT, ANY ONE INPUT ±10 mA

POWER DISSIPATION PER PACKAGE (P_D):
 For T_A = -40 to +60°C (PACKAGE TYPE E) 500 mW
 For T_A = +60 to +85°C (PACKAGE TYPE E) Derate Linearly at 12 mW/°C to 200 mW
 For T_A = -55 to 100°C (PACKAGE TYPE D) 500 mW
 For T_A = +100 to +125°C (PACKAGE TYPE D) Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR
 For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Type) 40 mW

OPERATING-TEMPERATURE RANGE (T_A):
 PACKAGE TYPE D, H -55 to +125°C
 PACKAGE TYPE E -40 to +85°C

STORAGE TEMPERATURE RANGE (T_{stg}) -85 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):
 At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. +265°C

OPERATING CONDITIONS at T_A = Full Package-Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1851		CDP1851C		
	MIN.	MAX.	MIN.	MAX.	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V _{SS}	V _{DD}	V _{SS}	V _{DD}	

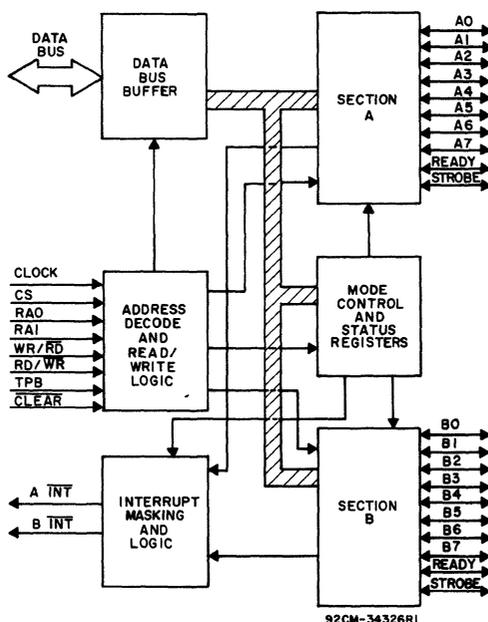


Fig. 1 - Functional diagram for CDP1851 and CDP1851C.

CDP1851, CDP1851C

STATIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} \pm 5\%$, Except as noted

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	CDP1851			CDP1851C			
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device Current I_{DD}	—	0, 5	5	—	0.01	50	—	0.02	200	μA
	—	0, 10	10	—	1	200	—	—	—	
Output Low Drive (Sink) Current I_{OL}	0.4	0, 5	5	1.6	3.2	—	1.6	3.2	—	mA
	0.5	0, 10	10	2.6	5.2	—	—	—	—	
Output High Drive (Source) Current I_{OH}	4.6	0, 5	5	-1.15	-2.3	—	-1.15	-2.3	—	mA
	9.5	0, 10	10	-2.6	-5.2	—	—	—	—	
Output Voltage Low-Level $V_{OL}\ddagger$	—	0, 5	5	—	0	0.1	—	0	0.1	V
	—	0, 10	10	—	0	0.1	—	—	—	
Output Voltage High Level $V_{OH}\ddagger$	—	0, 5	5	4.9	5	—	4.9	5	—	V
	—	0, 10	10	9.9	10	—	—	—	—	
Input Low Voltage V_{IL}	0.5, 4.5	—	5	—	—	1.5	—	—	1.5	V
	0.5, 9.5	—	10	—	—	3	—	—	—	
Input High Voltage V_{IH}	0.5, 4.5	—	5	3.5	—	—	3.5	—	—	V
	0.5, 9.5	—	10	7	—	—	—	—	—	
Input Leakage Current I_{IN}	Any Input	0, 5	5	—	—	± 1	—	—	± 1	μA
		0, 10	10	—	—	± 2	—	—	—	
3-State Output Leakage Current I_{OUT}	0, 5	0, 5	5	—	—	± 1	—	—	± 1	μA
	0, 10	0, 10	10	—	—	± 1	—	—	—	
Operating Current $I_{DD1}\Delta$	—	0, 5	5	—	1.5	3	—	1.5	3	mA
	—	0, 10	10	—	6	12	—	—	—	
Input Capacitance C_{IN}	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance C_{OUT}	—	—	—	—	10	15	—	10	15	

*Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .

$\ddagger I_{OL} = I_{OH} = 1 \mu\text{A}$.

Δ Operating current is measured at 200 kHz for $V_{DD} = 5\text{ V}$ and 400 kHz for $V_{DD} = 10\text{ V}$, with open outputs (worst-case frequencies for CDP1802A system operating at maximum speed of 3.2 MHz).

FUNCTIONAL DESCRIPTION

The CDP1851 has four modes of operation: input, output, bidirectional, and bit-programmable. Port A is programmable in all modes; port B is programmable in all but the bidirectional mode. A control byte must be loaded into the control register to program the ports. In the input and output modes, each port has two handshaking signals, STROBE and RDY. In the bidirectional mode, port A has four handshaking signals: A RDY and A STROBE for input, B RDY and B STROBE for output. If port A is programmed in the bidirectional mode, port B must be programmed in the bit-programmable mode. Each terminal of port A or B may be individually programmed for input or output in the bit-programmable mode. Since handshaking is not used in this mode, the RDY and STROBE lines may also be used for bit-programming if port A is not in the bidirectional mode.

Input Mode

When a peripheral device has data to input, it sends a

STROBE pulse to the PIO. The leading edge of this pulse clears the RDY line, inhibiting further transmission from the peripheral. The trailing edge of the STROBE pulse latches the data into the PIO buffer register and also activates the INT line to signal the CPU to read this data. The INT pin can be wired to the INT pin of the CPU or the EF lines for polling. The CPU then executes an input or a load instruction, depending on the mapping technique used. In either case the proper code must be asserted on the RAO, RA1, and CS lines to read the buffer register (see Table VI).

The INT line is deactivated on the leading edge of TPB. The trailing edge of TPB sets the RDY line to signal the peripheral that the port is ready to be loaded with new data. If RDY is low when the input mode is entered (i.e. after a reset), a "dummy" read must be done to set RDY high and signal the peripheral device that the port is ready to be loaded.

FUNCTIONAL DESCRIPTION (Cont'd)

Output Mode

A peripheral STROBE pulse sent to the PIO generates an interrupt to signal the CPU that the peripheral device is ready for data. The CPU executes the proper output or store instruction. Data are then read from memory and placed on the bus. The data are latched into the port buffer at the end of the window when $\overline{RE}/\overline{WE} = 0$ and $\overline{WR}/\overline{RE} = 1$. The RDY line is also set at this time, indicating to the peripheral that there is data in the port buffer. The \overline{INT} line is deactivated at the beginning of the window. After the peripheral reads valid port data, it can send another STROBE pulse, clearing the RDY line and activating the \overline{INT} line as in the input mode.

Bidirectional Mode

This mode programs port A to function as both an input and output port. The bidirectional feature allows the peripheral to control port direction by using both sets of handshake signals. The port A handshaking pins are used to control input data from peripheral to PIO, while the port B handshaking pins are used to control output data from PIO to peripheral. Data are transferred in the same manner as the input and output modes. Since \overline{AINT} is used for both

input and output, the status register must be read to determine what condition caused \overline{AINT} to be activated (see Table V).

Bit—Programmable Mode

This mode allows individual bits of port A or port B to be programmed as inputs or outputs. To output data to bits programmed as outputs, the CPU loads a data byte into the 8 bit port as in the output mode (no handshaking). Only bits programmed as outputs latch this data. Data must be stable when reading from bits programmed as inputs, since the input bits do not latch. When the CDP1851 inputs data to the CPU the CPU also reads the output bits latched during the last output cycle. The RDY and STROBE lines may be used for I/O by using the STROBE/RDY I/O control byte in table II. An additional feature available in the bit-programmable mode is the ability to generate interrupts based on input/output byte combinations. These interrupts can be programmed to occur on logic conditions (AND, OR, NAND, and NOR) generated by the eight I/O lines of each port (The STROBE and RDY lines cannot generate interrupts).

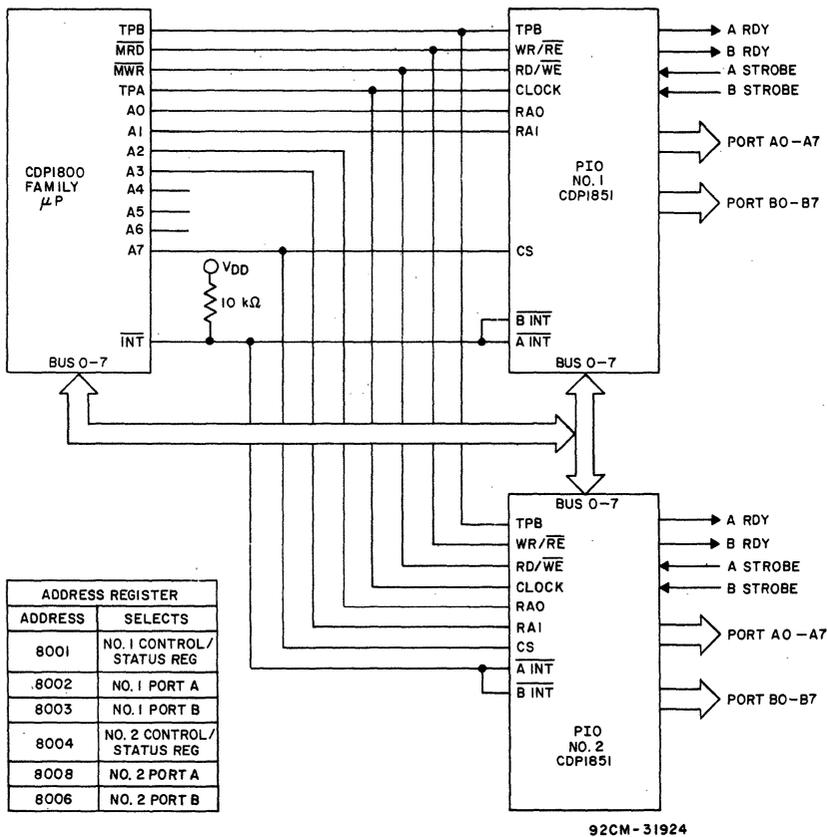


Fig. 2 - Memory space I/O. This configuration allows up to four CDP1851s to occupy memory space 8XXX with no additional hardware (A4 - A5 and A6 - A7 are used as RAO and RA1 on the third and fourth PIO's).

PROGRAMMING

1. Initialization and Controls

The CDP1851 PIO must be cleared by a low on the CLEAR input during power-on to set it for programming. Once programmed, modes can be changed without clearing except when exiting the bit-programmable mode. A low on the CLEAR input sets both ports to the input modes, disables interrupts, unmask all bit-programmed interrupt bits, and resets the status register, A RDY, and B RDY.

2. Mode Setting

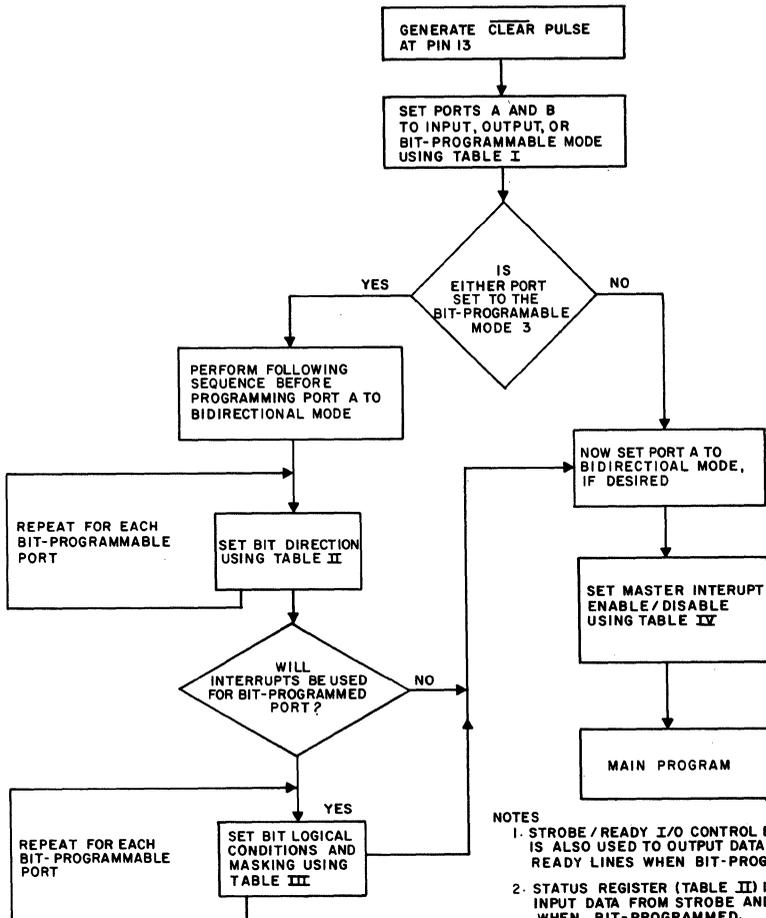
The control register must be sequentially loaded with the appropriate mode set control bytes in order as shown in table I (i.e. input mode then output mode, etc.). Port A is set with the SET A bit = 1 and port B is set with the SET B bit = 1. If a port is set to the bit-programmable mode, the bit-programming control byte from table II must be loaded. A bit is programmed for output with the I/O bit = 1 and for input with the I/O bit = 0. The STROBE and RDY lines may be programmed for input or output with the STROBE/RDY control byte of

table II. Input data on the STROBE and RDY lines is detected by reading the status register. When using the STROBE or RDY lines for output, the control byte must be loaded every time output data is to be changed. To program logical conditions that will generate an interrupt, the interrupt control byte of table III must be loaded. An interrupt mask of the eight I/O lines may be loaded next, if bit D4 (mask follows) of the interrupt control byte = 1. The I/O lines are masked if the corresponding bit of the interrupt mask register is 1, otherwise it is monitored. Any combination of masked bits are permissible, except all bits masked (mask = FF).

3. INT Enable/Disable

To enable or disable the INT line in all modes, the interrupt ENABLE/DISABLE byte must be loaded (see Table IV). Interrupts can also be detected by reading the status register see table V. All interrupts should be disabled when programming or false interrupts may occur. The INT outputs are open drain NMOS devices that allow wired ORing (use 10K pull-up registers).

A FLOW CHART GUIDE TO CDP1851 MODE PROGRAMMING



- NOTES
1. STROBE / READY I/O CONTROL BYTE (TABLE II) IS ALSO USED TO OUTPUT DATA TO STROBE AND READY LINES WHEN BIT-PROGRAMMED.
 2. STATUS REGISTER (TABLE III) IS USED TO INPUT DATA FROM STROBE AND READY LINES WHEN BIT-PROGRAMMED.
 3. INTERRUPT STATUS IS ALSO READ FROM STATUS REGISTER.

TABLE I [RA1=0, RA0=1]

MODE SET *	7	6	5	4	3	2	1	0
Input	0	0	X	Set B	Set A	X	1	1
Output	0	1	X	Set B	Set A	X	1	1
Bit-Programmable	1	1	X	Set B	Set A	X	1	1
Bidirectional	1	0	X	Set B	Set A	X	1	1

* Modes should be set in order as shown in Table I

If either port is set for bit-programmable mode, the two following control bytes should immediately follow:

TABLE II [RA1=0, RA0=1]

Bit-Programming	7	6	5	4	3	2	1	0
	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
STROBE/RDY I/O Control Δ	D7	D6	D5	D4	D3	D2	D1	D0

Δ Output = 1

Δ Input = 0

(D1) 0 = Port A, 1 = Port B

(D2) 0 = No change to RDY line function, 1 = Change per bit (D6)

(D3) 0 = No change to STROBE line function, 1 = Change per bit (D7)

(D4) RDY line output data

(D5) STROBE line output data

(D6) RDY line used as:

Output = 1

Input = 0

(D7) STROBE line used as:

Output = 1

Input = 0

If interrupts will be used for either bit-programmed port, the following control bytes should be loaded:

TABLE III [RA1=0, RA0=1]

INTERRUPT CONTROL	7	6	5	4	3	2	1	0
Logical Conditions and Mask	0	D6	D5	D4	D3	1	0	1

(D3) 0 = Port A, 1 = Port B

(D4) 0 = No change in mask, 1 = Mask follows (See TABLE IIIa)

(D5) (D6) 0, 0 = NAND; 1, 0 = OR; 0, 1 = NOR; 1, 1 = AND

TABLE IIIa [RA1=0, RA0=1]

INTERRUPT CONTROL	7	6	5	4	3	2	1	0
Mask Register (If D4 = 1)	B7 Mask	B6 Mask	B5 Mask	B4 Mask	B3 Mask	B2 Mask	B1 Mask	B0 Mask

If Bn Mask = 1 then mask Bit (for n = 0 to 7)

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CDP1851, CDP1851C

TABLE IV [RA1=0, RA0=1]

Interrupt Enable/Disable	7	6	5	4	3	2	1	0
	$\overline{\text{INT}}$ Enable	X	X	X	A/B	0	0	1

$\overline{\text{INT}}$ Enable = 1, $\overline{\text{INT}}$ Enabled
 = 0, $\overline{\text{INT}}$ Disabled

A/B = 0, Port A
 = 1, Port B

TABLE V [RA1=0, RA0=1]

Status Register	7	6	5	4	3	2	1	0
	D7	D6	D5	D4	D3	D2	D1	D0

(D0) $\overline{\text{B INT}}$ status (1 means set)	} All Modes	(D4) A RDY input data	} Bit-Programmable Mode
(D1) $\overline{\text{A INT}}$ status (1 means set)		(D5) A STROBE input data	
(D2) 1 = $\overline{\text{A INT}}$ was caused by B STROBE	} Bidirectional Mode Only	(D6) B RDY input data	
(D3) 1 = $\overline{\text{A INT}}$ was caused by A STROBE		(D7) B STROBE input data	

TABLE VI — CPU CONTROLS

CS *	RA1	RA0	RD/ $\overline{\text{WE}}$	WR/ $\overline{\text{RE}}$	Action
0	X	X	X	X	No-op bus 3-stated
X	0	0	X	X	No-op bus 3-stated
X	X	X	0	0	No-op bus 3-stated
X	X	X	1	1	No-op bus 3-stated
X	X	X	1	1	No-op bus 3-stated
1	0	1	1	0	Read * status register
1	0	1	0	1	Load control register
1	1	0	1	0	Read * port A
1	1	0	0	1	Load port A
1	1	1	1	0	Read * port B
1	1	1	0	1	Load port B

* Read = RD/ $\overline{\text{WE}}$ = 1 and WR/ $\overline{\text{RE}}$ = 0 is latched on trailing edge of CLOCK.

TABLE VII — MEMORY I/O USE

I/O Space	RD/ $\overline{\text{WE}}$ Input	WR/ $\overline{\text{RE}}$ Input	TPB Input	} PIO Terminals
	$\overline{\text{MRD}}$	TPB	TPB	
Memory Space	$\overline{\text{MWR}}$	MRD	TPB	} CPU Terminals

FUNCTION PIN DEFINITION

CLOCK (Input):

Positive input pulse that latches READ and CS on its trailing edge.

CS — CHIP SELECT (Input)

A high-level voltage at this input selects the CDP1851 PIO.

RA0 — REGISTER ADDRESS 0 (Input):

This input and RA1 are used to select either the ports or the control/status registers.

RA1 — REGISTER ADDRESS 1 (Input):

See RA0

BUS 0 — BUS 7:

Bidirectional CPU data bus.

CLEAR (Input)

A low-level voltage at this input resets both ports to the input mode, and also resets the status register. A RDY, B RDY, and interrupt enable (disabling interrupts).

A INT — A INTERRUPT (Output):

A low-level voltage at this output indicates the presence of one of the interrupt conditions listed in Table III. This output is an open-drain NMOS device (to allow wired ORing) and must be tied to a pullup resistor, normally 10 k Ω .

FUNCTION PIN DEFINITION (Cont'd)

B INT — B INTERRUPT (Output):

A low-level voltage at this output indicates the presence of one of the interrupt conditions listed in Table III. This output is also an open-drain NMOS device and must be tied to a pullup resistor.

B RDY — B READY (Output):

This output is a handshaking or data bit I/O line in the bit-programmable mode.

B STROBE (Input):

An input handshaking line for port B in the input and output modes, and for port A when it is in the bidirectional mode. It can be used as a data bit I/O line in the bit-programmable mode except when port A is not programmed as bidirectional.

B 0 — B 7:

Data input or output lines for port B.

V_{SS}:

Ground

A 0 — A 7:

Data input or output lines for port A.

A STROBE (Input):

An input handshaking line for port A in the input, output, and bidirectional modes. It can also be used as a data bit I/O line when port A is in the bit-programmable mode.

A RDY — A READY (Output):

A output handshaking line or data bit I/O line.

TPB (Input):

A positive input pulse used as a data load, set, or reset strobe.

WR/RE — WRITE/READ ENABLE (Input):

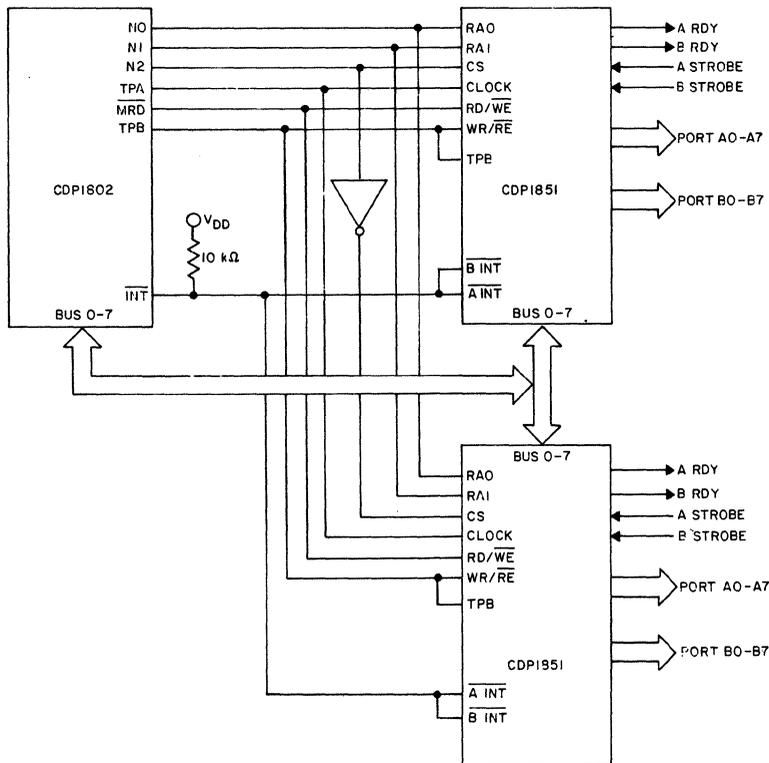
A positive input used to write data from the CDP1851 to the CPU bus.

RD/WE — READ/WRITE ENABLE (Input):

A positive input used to read data from the CDP1851 to the CPU bus.

V_{DD}:

Positive supply voltage.



92CM-31925

Fig. 3 - I/O space I/O.

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**DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} \pm 5\%$,
 $t_r, t_f = 20$ ns, $V_{IH} = 0.7 V_{DD}$, $V_{IL} = 0.3 V_{DD}$, $C_L = 100$ pF**

CHARACTERISTIC	VDD (V)	LIMITS						UNITS
		CDP1851			CDP1851C			
		Min.	Typ.*	Max.+	Min.	Typ.*	Max.+	
Input Mode see Figs. 4 and 5								
Minimum Setup Times:								
Chip Select to CLOCK	t_{CSCL}	5	—	50	75	—	50	75
		10	—	25	40	—	—	—
RD/ \overline{WE} to CLOCK	t_{RWCL}	5	—	75	120	—	75	120
		10	—	40	60	—	—	—
WR/ \overline{RE} to CLOCK	t_{WRCL}	5	—	75	120	—	75	120
		10	—	40	60	—	—	—
Data in to STROBE	t_{DIST}	5	—	75	120	—	75	120
		10	—	40	60	—	—	—
Minimum Hold Times:								
Chip Select After CLOCK	t_{HCSC}	5	—	75	120	—	75	120
		10	—	40	60	—	—	—
Address After TPB	T_{HATPB}	5	—	-50	0	—	-50	0
		10	—	-25	0	—	—	—
Data In After STROBE	t_{HSTDI}	5	—	50	75	—	50	75
		10	—	25	40	—	—	—
Data Bus Out After Address	t_{HADOH}	5	50	325	500	50	325	500
		10	25	165	250	—	—	—
Propagation Delay Times:								
TPB to \overline{INT}	t_{PINT}	5	—	200	300	—	200	300
		10	—	100	150	—	—	—
STROBE to \overline{INT}	t_{STINT}	5	—	200	300	—	200	300
		10	—	100	150	—	—	—
TPB to RDY	t_{TPRDY}	5	—	250	375	—	250	375
		10	—	125	200	—	—	—
STROBE to RDY	t_{STRDY}	5	—	260	400	—	260	400
		10	—	130	200	—	—	—
Minimum Pulse Widths:								
CLOCK	t_{WCL}	5	—	75	120	—	75	120
		10	—	40	60	—	—	—
TPB	t_{WTPB}	5	—	75	120	—	75	120
		10	—	40	60	—	—	—
STROBE	t_{WST}	5	—	100	150	—	100	150
		10	—	50	75	—	—	—
Access Time, Address to Data		5	—	325	500	—	325	500
Bus Out	t_{ADA}	10	—	165	250	—	—	—

ns

*Typical values are for $T_A = 25^\circ\text{C}$ and nominal voltages.

+Maximum limits of minimum characteristics are the values above which all devices function.

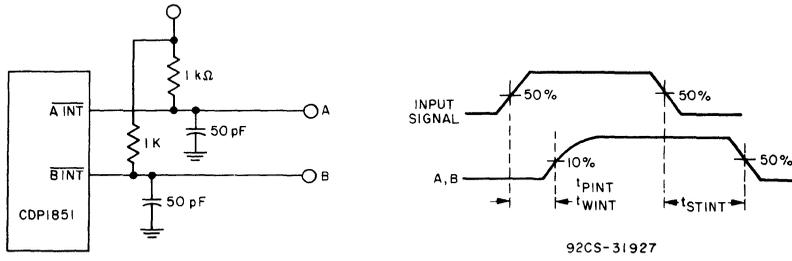


Fig. 4 - Interrupt signal propagation delay time test circuit and waveforms.

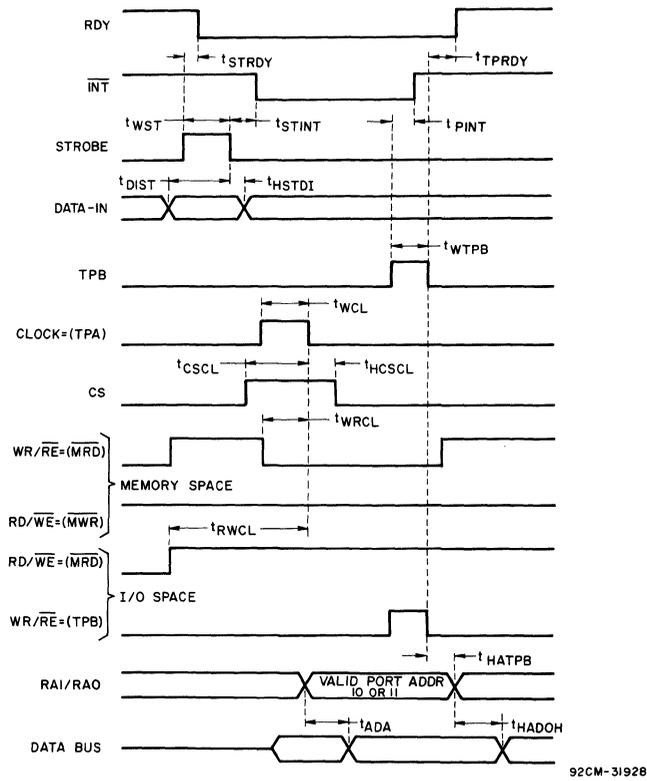


Fig. 5 - Input mode timing waveforms.

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CDP1851, CDP1851C

**DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} \pm 5\%$,
 $t_r, t_f = 20$ ns, $V_{IH} = 0.7 V_{DD}$, $V_{IL} = 0.3 V_{DD}$, $C_L = 100$ pF**

CHARACTERISTIC	VDD (V)	Min.	LIMITS						UNITS
			CDP1851			CDP1851C			
			Typ.*	Max.+	Min.	Typ.*	Max.+		
Output Mode see Figs. 4 and 6									
Minimum Setup Times:	5	—	50	75	—	50	75	ns	
Chip Select to CLOCK	t_{CSCL}	10	—	25	40	—	—		
$\overline{RD}/\overline{WE}$ to CLOCK	t_{RWCL}	5	—	75	120	—	75		
		10	—	40	60	—	—		
$\overline{WR}/\overline{RE}$ to CLOCK	t_{WRCL}	5	—	75	120	—	75		
		10	—	40	60	—	—		
Address to WRITE *	t_{AW}	5	—	50	75	—	50		
		10	—	25	40	—	—		
Data Bus to WRITE *	t_{DW}	5	—	80	120	—	80		
		10	—	40	60	—	—		
Minimum Hold Times:	5	—	75	120	—	75	120		
Chip Select After CLOCK	t_{HCSCl}	10	—	40	60	—	—		
Address After WRITE *	t_{HAW}	5	—	50	75	—	50		
		10	—	25	40	—	—		
Data Bus After WRITE *	t_{HDW}	5	—	50	75	—	50		
		10	—	25	40	—	—		
Propagation Delay Times:	5	—	225	350	—	225	350		
WRITE * to Data Out	t_{WDO}	10	—	125	200	—	—		
WRITE * to \overline{INT}	t_{WINT}	5	—	300	450	—	300		
		10	—	150	225	—	—		
WRITE * to RDY	t_{WRDY}	5	—	350	525	—	350		
		10	—	175	275	—	—		
STROBE to \overline{INT}	t_{STINT}	5	—	200	300	—	200		
		10	—	100	150	—	—		
STROBE to RDY	t_{STRDY}	5	—	260	400	—	260		
		10	—	130	200	—	—		
Minimum Pulse Widths:	5	—	75	120	—	75	120		
CLOCK	t_{WCL}	10	—	40	60	—	—		
STROBE	t_{WST}	5	—	100	150	—	100		
		10	—	50	75	—	—		
WRITE *	t_{WW}	5	—	175	275	—	175		
		10	—	90	150	—	—		

* WRITE is the overlap of $\overline{RD}/\overline{WE} = 0$ and $\overline{WR}/\overline{RE} = 1$.

*Typical values are for $T_A = 25^\circ\text{C}$ and nominal voltages.

*Maximum limits of minimum characteristics are the values above which all devices function.

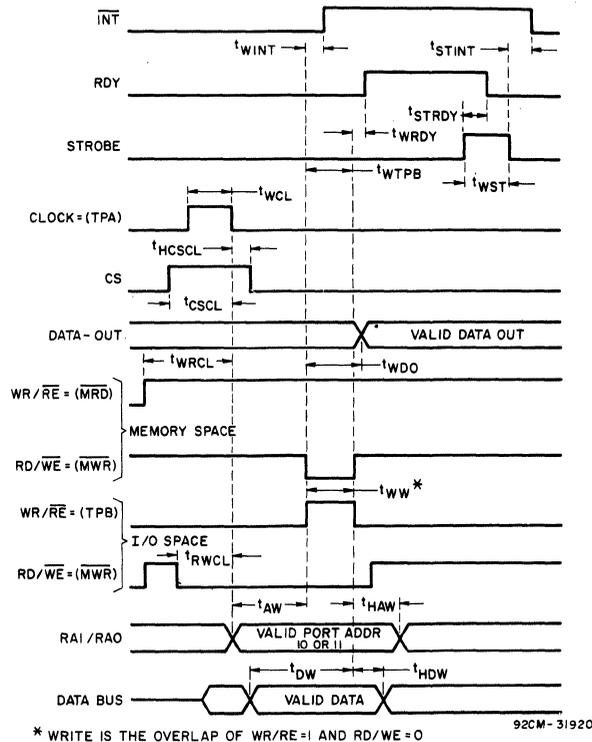


Fig. 6 - Output mode timing waveforms.

OPERATING AND HANDLING CONSIDERATIONS

1. Handling

All inputs and outputs of RCA CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in ICAN-6525 "Guide to Better Handling and Operation of CMOS Integrated Circuits."

2. Operating

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause $V_{DD} - V_{SS}$ to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS} . Input currents must not exceed 10 mA even when the power supply is off.

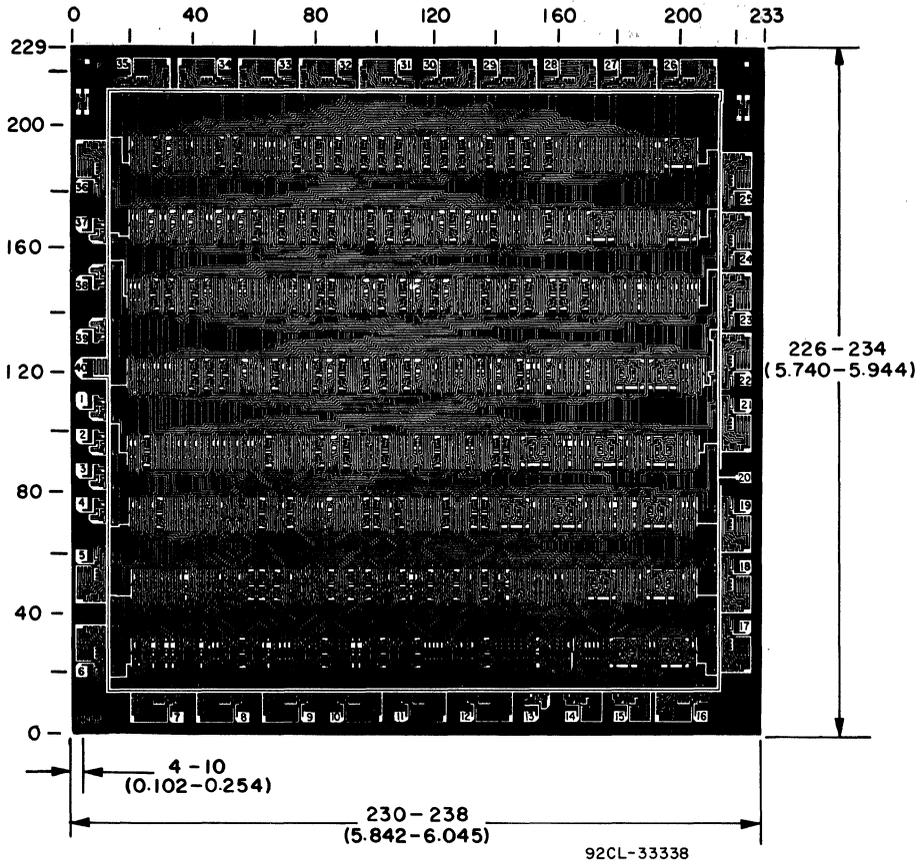
Unused Inputs

A connection must be provided at every input terminal. All unused STROBE and DATA terminals must be connected to either V_{DD} or V_{SS} , whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} or V_{SS} may damage CMOS devices by exceeding the maximum device dissipation.

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Dimensions and pad layout for CDP1851CH.

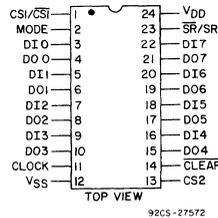
Dimensions in parentheses are in millimeters and are derived from the basic inch dimension as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

8-Bit Input/Output Port

Features:

- Static Silicon-Gate CMOS circuitry
- Compatible with CDP1800-series
- Interfaces with CDP1802 and CDP1804 microprocessors without additional components
- Single voltage supply
- Full military temperature range (-55°C to +125°C)
- Parallel 8-bit data register and buffer
- Flip-flop for service request
- Asynchronous register clear
- Low quiescent and operating power



Terminal Assignment

The RCA-CDP1852 and CDP1852C are parallel, 8-bit, mode-programmable COS/MOS input/output ports designed for use in CDP1800 series microprocessor systems. These input/output ports are compatible and will interface directly with the CDP1802 or CDP1804 without additional components. They are also useful as 8-bit address latches in 1800-series microprocessor systems and as I/O ports in general purpose applications.

The mode control is used to program the device as an input port (mode=0) or output port (mode=1). If the CDP1852 is used as an input port (mode=0), data is strobed into the port's 8-bit register by a high (1) level on the clock line. The negative, high-to-low transition of the clock sets the Service Request output (SR=0) and latches the data in the register. The SR output can be used to signal the microprocessor via a flag or interrupt line. When CS1·CS2=1 the three-state output drivers are enabled, the negative high-to-low transition of CS1·CS2 resets the Service Request output, \overline{SR} =1.

If the CDP1852 is used as an output port (mode=1), data is strobed into the port's 8-bit register when $\overline{CS1} \cdot \overline{CS2} \cdot \text{CLOCK}=1$. The three-state output drivers are enabled at all times when the CDP1852 is configured as an output port. The service request signal is generated at the termination of $\overline{CS1} \cdot \overline{CS2}=1$ and will be present, 1 level, until the following negative, high-to-low transition of the clock.

A CLEAR control is provided for resetting the port's register and service request flip-flop.

The CDP1852 is functionally identical to the CDP1852C. The CDP1852 has a recommended operating voltage range of 4 to 10.5 volts, and the CDP1852C has a recommended operating voltage range of 4 to 6.5 volts.

The CDP1852 and CDP1852C are supplied on 24-lead, hermetic, dual-in-line ceramic packages (D suffix), in 24-lead dual-in-line plastic packages (E suffix).

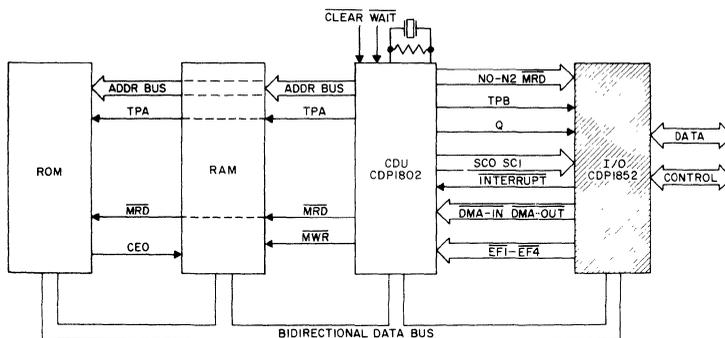


Fig. 1—Typical CDP1802 microprocessor system.

92CM-2757A

RCA CMOS LSI Products

CDP1852, CDP1852C

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})		
(Voltage referenced to V_{SS} Terminal)		
CDP1852		-0.5 to +11 V
CDP1852C		-0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS		-0.5 to $V_{DD} + 0.5$ V
DC INPUT CURRENT, ANY ONE INPUT		± 10 mA
POWER DISSIPATION PER PACKAGE (P_D):		
For $T_A = -40$ to $+60^\circ\text{C}$ (PACKAGE TYPE E)		500 mW
For $T_A = +60$ to $+85^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at $12\text{ mW}/^\circ\text{C}$	to 200 mW
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE D)		500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE D)	Derate Linearly at $12\text{ mW}/^\circ\text{C}$	to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR		
FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$		100 mW
OPERATING-TEMPERATURE RANGE (T_A):		
PACKAGE TYPES D, H		-55 to $+125^\circ\text{C}$
PACKAGE TYPE E		-40 to $+85^\circ\text{C}$
STORAGE TEMPERATURE RANGE (T_{stg})		
		-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):		
At distance $1/16 \pm 1/32$ inch (1.59 ± 0.79 mm) from case for 10 s max.		$+265^\circ\text{C}$

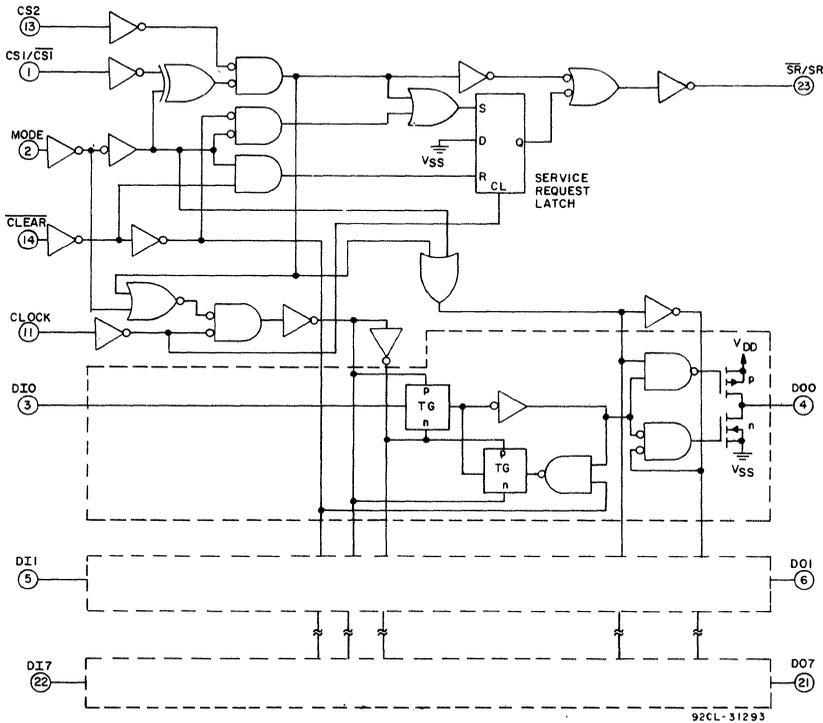


Fig. 2 - CDP1852 logic diagram.

RECOMMENDED OPERATING CONDITIONS at T_A = Full Package Temperature Range
 For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1852		CDP1852C		
	Min.	Max.	Min.	Max.	
DC Operating-Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	VSS	VDD	VSS	VDD	V

STATIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} \pm 5\%$

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	CDP1852			CDP1852C			
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device Current, I_{DD}	—	0,5	5	—	—	100	—	—	500	μA
	—	0,10	10	—	—	500	—	—	—	
Output Low Drive (Sink) Current, I_{OL}	0,4	0,5	5	1,6	3,2	—	1,6	3,2	—	mA
	—	0,10	10	3	6	—	—	—	—	
Output High Drive (Source) Current, I_{OH}	4,6	0,5	5	-1,15	-2,3	—	-1,15	-2,3	—	mA
	9,5	0,10	10	-3	-6	—	—	—	—	
Output Voltage Low-Level V_{OL}^Δ	—	0,5	5	—	0	0,1	—	0	0,1	V
	—	0,10	10	—	0	0,1	—	—	—	
Output Voltage HighLevel, V_{OH}	—	0,5	5	4,9	5	—	4,9	5	—	V
	—	0,10	10	9,9	10	—	—	—	—	
Input Low Voltage, V_{IL}	0,5,4,5	—	5	—	—	1,5	—	—	1,5	V
	0,5,9,5	—	10	—	—	3	—	—	—	
Input High Voltage, V_{IH}	0,5,4,5	—	5	3,5	—	—	3,5	—	—	V
	0,5,9,5	—	10	7	—	—	—	—	—	
Input Current, I_{IN}	—	0,5	5	—	—	± 1	—	—	± 1	μA
	—	0,10	10	—	—	± 2	—	—	—	
3-State Output Leakage Current I_{OUT}	0,5	0,5	5	—	—	± 1	—	—	± 1	μA
	0,10	0,10	10	—	—	± 2	—	—	—	
Operating Current, $I_{DD1}^\#$	—	0,5	5	—	130	200	—	150	200	μA
	—	0,10	10	—	400	600	—	—	—	
Input Capacitance C_{IN}	—	—	—	—	5	7,5	—	5	7,5	pF
Output Capacitance, C_{OUT}	—	—	—	—	5	7,5	—	—	—	

* Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .

$^\Delta I_{OL} = I_{OH} = 1 \mu\text{A}$

$^\#$ Operating current is measured at 2 MHz in an 1800 system with open outputs and a program of 6N55, 6NAA, 6N55, 6NAA,

RCA CMOS LSI Products
CDP1852, CDP1852C

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = \pm 5\%$,
 $t_r, t_f = 20$ ns, $V_{IH} = 0.7 V_{DD}$, $V_{IL} = 0.3 V_{DD}$, $C_L = 100$ pF, and 1 TTL Load
 LIMITS AT $V_{DD} = 10$ V APPLY TO THE CDP1852 ONLY

CHARACTERISTIC	V_{DD} (V)	LIMITS			UNITS
		Min.	Typ.*	Max.	
MODE 0 – Input Port					
Required Select Pulse Width, t_{SW}	5	–	180	360	ns
	10	–	90	180	
Required Write Pulse Width, t_{WW}	5	–	90	180	
	10	–	45	90	
Required Clear Pulse Width, t_{CLR}	5	–	80	160	
	10	–	40	80	
Required Data Setup Time, t_{SD}	5	–	–10	0	
	10	–	–5	0	
Required Data Hold Time, t_{DH}	5	–	75	150	
	10	–	35	75	
Data Out Hold Time, t_{DOH}^Δ	5	30	185	370	
	10	15	100	200	
SR Output Transition Time	5	–	30	60	
	10	–	15	30	
Data Output Transition Time	5	–	30	60	
	10	–	15	30	
Propagation Delay Times, t_{PLH} , t_{PHL} : Select to Data Out $^\Delta$	5	30	185	370	
	10	15	100	200	
Clear to SR	5	–	170	340	
	10	–	85	170	
Clock to SR	5	–	110	220	
	10	–	55	110	
Select to SF	5	–	120	240	
	10	–	60	120	
MODE 1 – Input Port					
Required Clock Pulse Width, t_{CL}	5	–	130	260	ns
	10	–	65	130	
Required Write Pulse Width, t_{WW}	5	–	130	260	
	10	–	65	130	
Required Clear Pulse Width, t_{CLR}	5	–	60	120	
	10	–	30	60	
Required Data Setup Time, t_{DS}	5	–	–10	0	
	10	–	–5	0	
Required Data Hold Time, t_{DH}	5	–	75	150	
	10	–	35	75	
Required Clock-after-Select Hold Time	5	–	–10	0	
	10	–	–5	0	
SR Output Transition Time	5	–	30	60	
	10	–	15	30	
Data Output Transition Time	5	–	30	60	
	10	–	15	30	

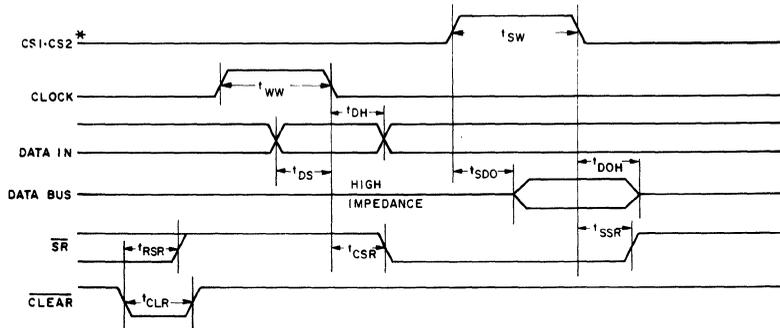
$^\Delta$ Minimum value is measured from CS2; maximum value is measured from CS1.

* Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .

DYNAMIC ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	V _{DD} (V)	LIMITS			UNITS
		Min.	Typ.*	Max.	
Propagation Delay Times, t _{PLH} , t _{PHL} : Clear to Data Out	5	—	140	280	ns
	10	—	70	140	
Write to Data Out	5	—	220	440	
	10	—	110	220	
Data In to Data Out	5	—	100	200	
	10	—	50	100	
Clear to SR	5	—	120	240	
	10	—	60	120	
Clock to SR	5	—	120	240	
	10	—	60	120	
Select to SR	5	—	120	240	
	10	—	60	120	

* Typical values are for T_A = 25°C and nominal V_{DD}.



* CS1-CS2 IS THE OVERLAP OF CS1=1 AND CS2=1

INPUTS			OUTPUTS	
CLOCK	CS1-CS2 [†]	CLEAR	DATA OUT	SR OUT
X	0	0	HIGH Z	1
X	0	1	HIGH Z	SR LATCH*
0	1	0	0	0
0	1	1	DATA LATCH	0
1	1	X	DATA IN	0

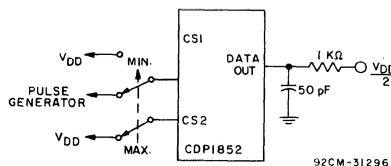
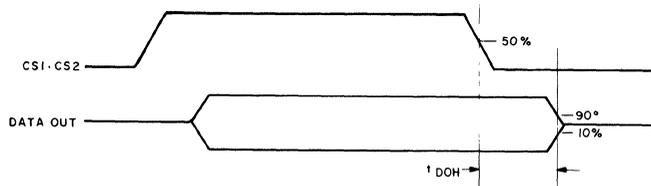
INPUTS		OUTPUTS	
CLOCK	CS1-CS2 [†]	CLEAR	SR LATCH*
X	X	0	1
X	1	X	1
0	0	1	0
0	0	1	NO CHANGE

[†] CS1-CS2 = 1 → CS1 = 1 and CS2 = 1.

* SR Latch is internal to the device (See Fig. 2).

Fig. 3 — MODE 0 input port timing diagram and truth tables.

92CM-31292



92CM-31296

Fig. 4 — Data out hold time waveforms and test circuit.

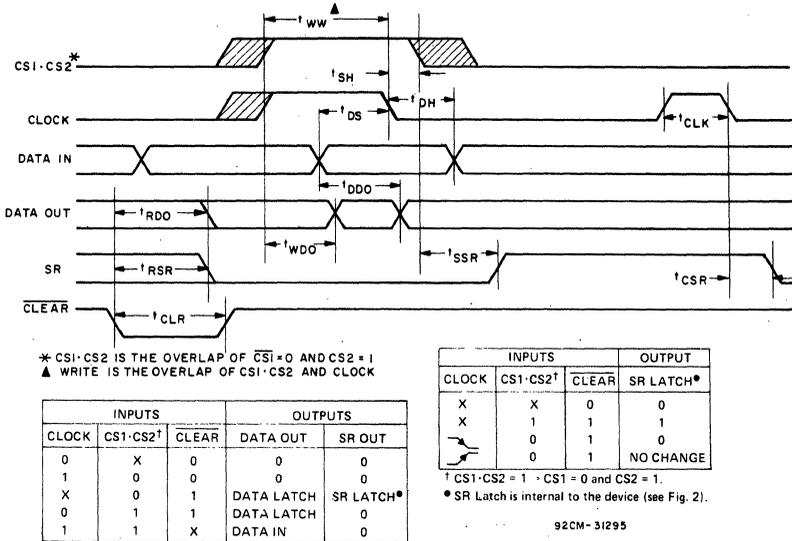


Fig. 5 - MODE 1 input port timing diagram and truth tables.

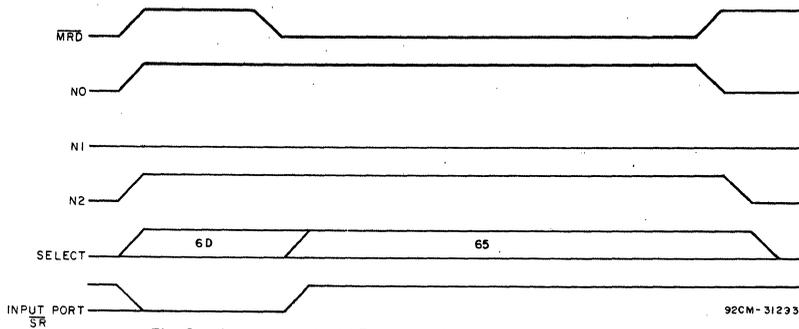


Fig. 6 - Execution of a "65" output instruction showing momentary selection of input port "D".

Application Information

In a CDP1802- or CDP1804-based system where MRD is used to distinguish between INP and OUT instructions, and INP instruction is assumed to occur at the beginning of every I/O cycle because MRD starts high. Therefore, at the start of an OUT instruction, which uses the same 3-bit N code as that used for selection of an input port, the input device will be selected for a short time (see Fig. 6). This condition forces SR low and resets the SR latch (see Fig. 2).

In a small system with unique N codes for inputs and outputs, this situation does not arise. Using the CDP1853 N-bit decoder or equivalent logic to decode the N lines after TPA prevents dual selection in larger systems.

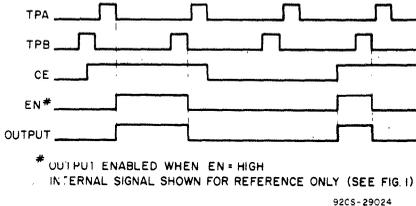


Fig. 7 CDP1853 timing diagram.

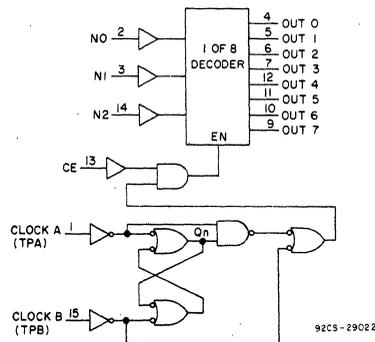
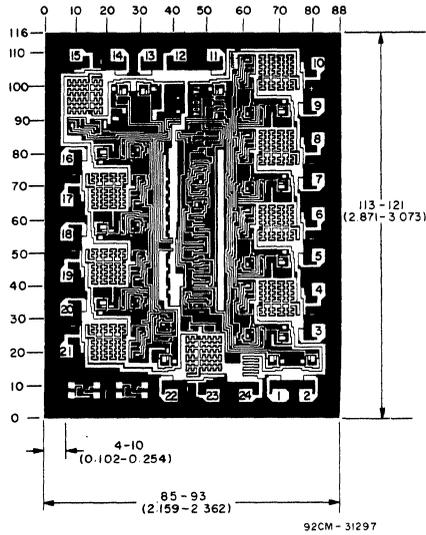


Fig. 8 - CDP1853 functional diagram.

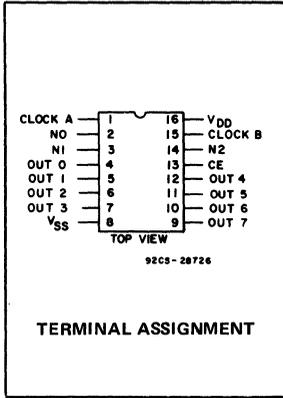


Dimensions and pad layout for CDP1852H.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

N-Bit 1 of 8 Decoder



Features:

- Provides direct control of up to 7 input and 7 output devices
- CHIP ENABLE (CE) allows easy expansion for multi-level I/O systems

The RCA-CDP1853 and CDP1853C are 1 of 8 decoders designed for use in general purpose microprocessor systems. These devices, which are functionally identical, are specifically designed for use as gated N-bit decoders and interface directly with the 1800-series microprocessors without additional components. The CDP1853 has a recommended operating voltage range of 4 to 10.5 volts, and the CDP1853C has a recommended operating voltage range of 4 to 6.5 volts.

When CHIP ENABLE (CE) is high, the selected output will be true (high) from the trailing edge of CLOCK A (high-to-low transition) to the trailing edge of CLOCK B (high-to-low transition). All outputs will be low when the device is not selected (CE = 0) and during conditions of CLOCK A and CLOCK B as shown in Fig. 2. The CDP1853 inputs N0, N1, N2, CLOCK A, and CLOCK B are connected to an 1800 series microprocessor outputs N0, N1, N2, TPA, and TPB respectively, when used to decode I/O

commands as shown in Fig. 5. The CHIP ENABLE (CE) input provides the capability for multiple levels of decoding as shown in Fig. 6.

The CDP1853 can also be used as a general 1 of 8 decoder for I/O and memory system applications as shown in Fig. 4.

The CDP1853 and CDP1853C are supplied in hermetic 16-lead dual-in-line ceramic (D suffix) and plastic (E suffix) packages.

TRUTH TABLE

CE	CL A	CL B	EN
1	0	0	Q _{n-1} *
1	0	1	1
1	1	0	0
1	1	1	1
0	X	X	0

N2	N1	N0	EN	0	1	2	3	4	5	6	7
0	0	0	1	1	0	0	0	0	0	0	0
0	0	1	1	0	1	0	0	0	0	0	0
0	1	0	1	0	0	1	0	0	0	0	0
0	1	1	1	0	0	0	1	0	0	0	0
1	0	0	1	0	0	0	0	1	0	0	0
1	0	1	1	0	0	0	0	0	1	0	0
1	1	0	1	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	0	1
X	X	X	0	0	0	0	0	0	0	0	0

1 = High level 0 = Low level X = Don't care

*Q_{n-1} = Enable remains in previous state.

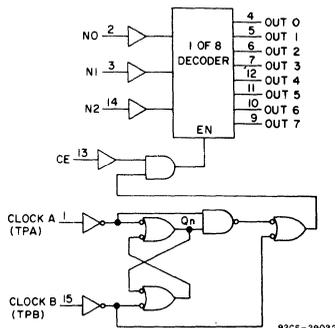


Fig. 1 - CDP1853 functional diagram.

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
 (All voltage values referenced to V_{SS} terminal)

CDP1853 -0.5 to +11 V
 CDP1853C -0.5 to +7 V

INPUT VOLTAGE RANGE, ALL INPUTS -0.5 to $V_{DD} + 0.5$ V
 DC INPUT CURRENT, ANY ONE INPUT ± 10 mA²

OPERATING-TEMPERATURE RANGE (T_A):
 CERAMIC PACKAGES (D SUFFIX TYPES) -55 to +125°C
 PLASTIC PACKAGES (E SUFFIX TYPES) -40 to +85°C

STORAGE TEMPERATURE RANGE (T_{sto}) -65 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):
 At distance 1/16 \pm 1/32 inch (1.59 \pm 0.79 mm) from case for 10 s max. +265°C

STATIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to +85°C. Except as noted

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	CDP1853			CDP1853C			
				Min.	Typ. †	Max.	Min.	Typ. †	Max.	
Quiescent Device Current, I_L	-	-	5	-	1	10	-	5	50	μ A
	-	-	10	-	10	100	-	-	-	
Output Low Drive (Sink) Current, I_{OL}	0.4	0.5	5	1.6	3.2	-	1.6	3.2	-	mA
	0.5	0.10	10	2.6	5.2	-	-	-	-	
Output High Drive (Source Current) I_{OH}	4.6	0.5	5	-1.15	-2.3	-	-1.15	-2.3	-	mA
	9.5	0.10	10	-2.6	-5.2	-	-	-	-	
Output Voltage Low-Level Δ V_{OL}	-	0.5	5	-	0	0.1	-	0	0.1	V
	-	0.10	10	-	0	0.1	-	-	-	
Output Voltage High Level V_{OH}	-	0.5	5	4.9	5	-	4.9	5	-	V
	-	0.10	10	9.9	10	-	-	-	-	
Input Low Voltage V_{IL}	0.5,4.5	-	5	-	-	1.5	-	-	1.5	V
	1.9	-	10	-	-	3	-	-	-	
Input High Voltage V_{IH}	0.5,4.5	-	5	3.5	-	-	3.5	-	-	V
	1.9	-	10	7	-	-	-	-	-	
Input Leakage Current I_{IN}	Any Input	0.5	5	-	-	± 1	-	-	± 1	μ A
		0.10	10	-	-	± 1	-	-	-	
Operating Current I_{DD1} *	0.5	0.5	5	-	50	100	-	50	100	μ A
	0.10	0.10	10	-	150	300	-	-	-	
Input Capacitance C_{IN}	-	-	-	-	5	7.5	-	5	7.5	ρ F
Output Capacitance C_{OUT}	-	-	-	-	10	15	-	10	15	ρ F

† Typical values are for $T_A = 25^\circ\text{C}$ and nominal voltage.

* Operating current measured in a CDP1802 system at 2MHz with outputs floating.

$\Delta I_{OL} = I_{OH} = 1\mu\text{A}$

RCA CMOS LSI Products

CDP1853, CDP1853C

OPERATING CONDITIONS at T_A = Full Package-Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1853		CDP1853C		
	Min.	Max.	Min.	Max.	
Supply-Voltage Range	4	10.5	4	6.5	V
Recommended Input Voltage Range	VSS	VDD	VSS	VDD	V

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} \pm 5\%$,

$V_{IH} = 0.7 V_{DD}$, $V_{IL} = 0.3 V_{DD}$, $t_r, t_f = 20$ ns, $C_L = 100$ pF

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS	
		CDP1853		CDP1853C			
		Typ.	Max.	Typ.	Max.		
Propagation Delay Time: CE to Output, t_{EOH} , t_{EOL}	5	175	275	175	275	ns	
	10	90	150	—	—		
N to Outputs, t_{NOH} , t_{NOL}	5	225	350	225	350	ns	
	10	120	200	—	—		
Clock A to Output, t_{AO}	5	200	300	200	300	ns	
	10	100	150	—	—		
Clock B to Output, t_{BO}	5	175	275	175	275	ns	
	10	90	150	—	—		
Minimum Pulse Widths: Clock A, t_{CACA}	5	50	75	50	75	ns	
	10	25	50	—	—		
	Clock B, t_{CBCB}	5	50	75	50		75
		10	25	50	—		—

Note 1: Maximum limits of minimum characteristics are the values above which all devices function.

Note 2: Typical values are for $T_A = 25^\circ\text{C}$ and nominal voltages.

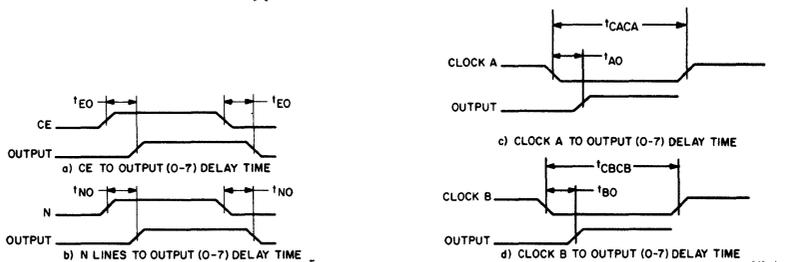
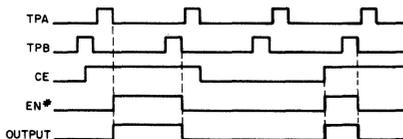


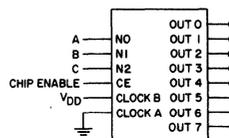
Fig. 2 — Propagation delay time diagrams.



* OUTPUT ENABLED WHEN EN = HIGH
INTERNAL SIGNAL SHOWN FOR REFERENCE ONLY (SEE FIG. 1)

92CS-29024

Fig. 3 — Timing diagram.



92CS-29027

Fig. 4 — N-bit decoder used as a 1 of 8 decoder.

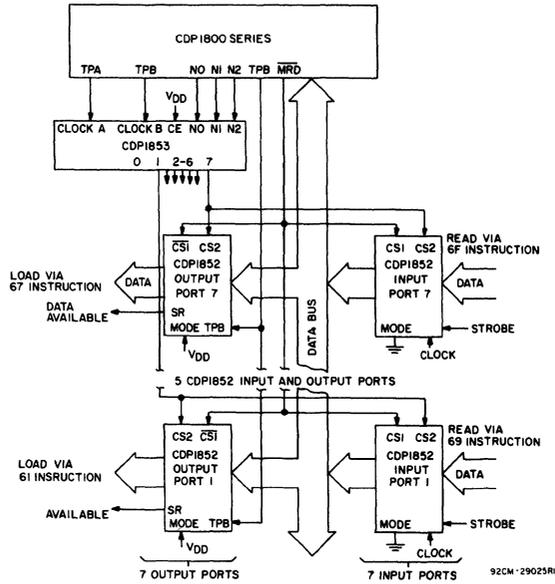


Fig. 5 - N-bit decoder in a one-level I/O system.

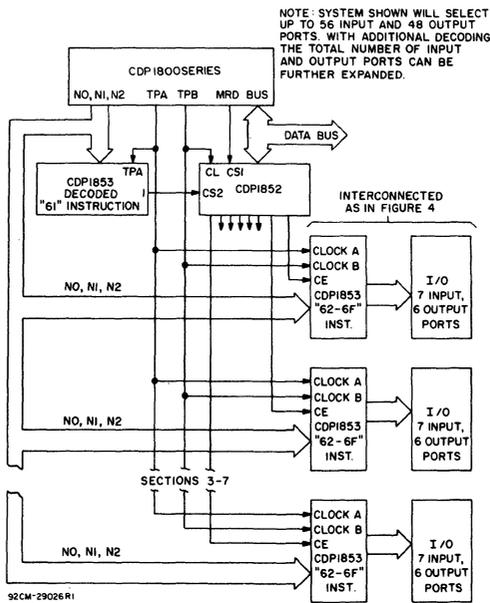
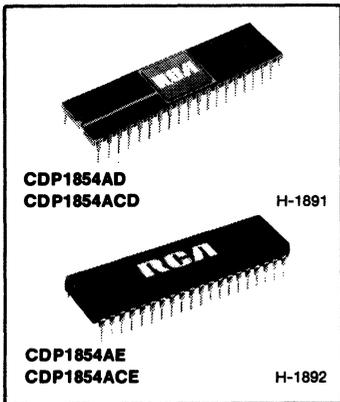


Fig. 6 - Two-level I/O using CDP1853 and CDP1852.



Programmable Universal Asynchronous Receiver/Transmitter (UART)

Features:

- **Two operating modes:**
Mode 0—functionally compatible with industry types such as the TR1602A
Mode 1—interfaces directly with CDP1800-series microprocessors without additional components
- **Full- or half-duplex operation**
- **Parity, framing, and overrun error detection**
- **Baud rate—DC to 200 K bits/sec @ $V_{DD}=5 V$**
DC to 400 K bits/sec @ $V_{DD}=10 V$
- **Fully programmable with externally selectable word length (5-8 bits), parity inhibit, even/odd parity, and 1, 1½, or 2 stop bits**
- **False start bit detection**

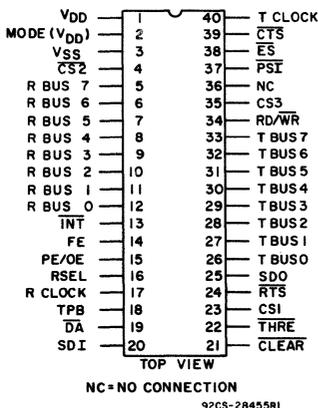
The RCA CDP1854A and CDP1854AC are silicon-gate CMOS Universal Asynchronous Receiver/Transmitter (UART) circuits. They are designed to provide the necessary formatting and control for interfacing between serial and parallel data. For example, these UARTs can be used to interface between a peripheral or terminal with serial I/O ports and the 8-bit CDP1800-series microprocessor parallel data bus system. The CDP1854A is capable of full duplex operation, i.e., simultaneous conversion of serial input data to parallel output data and parallel input data to serial output data.

The CDP1854A UART can be programmed to operate in one of two modes by using the mode control input. When the mode input is high (MODE=1), the CDP1854A is

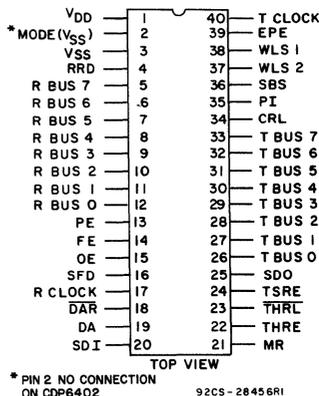
directly compatible with the CDP1800-series microprocessor system without additional interface circuitry. When the mode input is low (MODE=0), the device is functionally compatible with industry standard UART's such as the TR1602A. It is also pin compatible with these types, except that pin 2 is used for the mode control input instead of a $V_{GG}=-12 V$ supply connection.

The CDP1854A and the CDP1854AC are functionally identical. The CDP1854A has a recommended operating-voltage range of 4-10.5 volts, and the CDP1854AC has a recommended operating-voltage range of 4-6.5 volts.

The CDP1854A and CDP1854AC are supplied in hermetic 40-lead dual-in-line ceramic packages (D suffix) and in 40-lead dual-in-line plastic packages (E suffix). The CDP1854AC is also available in chip form (H suffix).



Mode 1
Terminal Assignment



Mode 0
Terminal Assignment

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltage referenced to V_{SS} Terminal)

CDP1854A	-0.5 to +11 V
CDP1854AC	-0.5 to +7 V

INPUT VOLTAGE RANGE, ALL INPUTS

.....	-0.5 to V _{DD} +0.5 V
-------	--------------------------------

DC INPUT CURRENT, ANY ONE INPUT

.....	±10 mA
-------	--------

POWER DISSIPATION PER PACKAGE (P_D):

For T _A =-40 to +60°C (PACKAGE TYPE E)	500 mW
For T _A =+60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T _A =-55 to 100°C (PACKAGE TYPE D)	500 mW
For T _A =+100 to +125°C (PACKAGE TYPE D)	Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T _A =FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
--	--------

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPE D	-55 to +125°C
PACKAGE TYPE E	-40 to +85°C

STORAGE TEMPERATURE RANGE (T_{stg})

.....	-65 to +150°C
-------	---------------

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
---	--------

Mode Input High (Mode = 1)

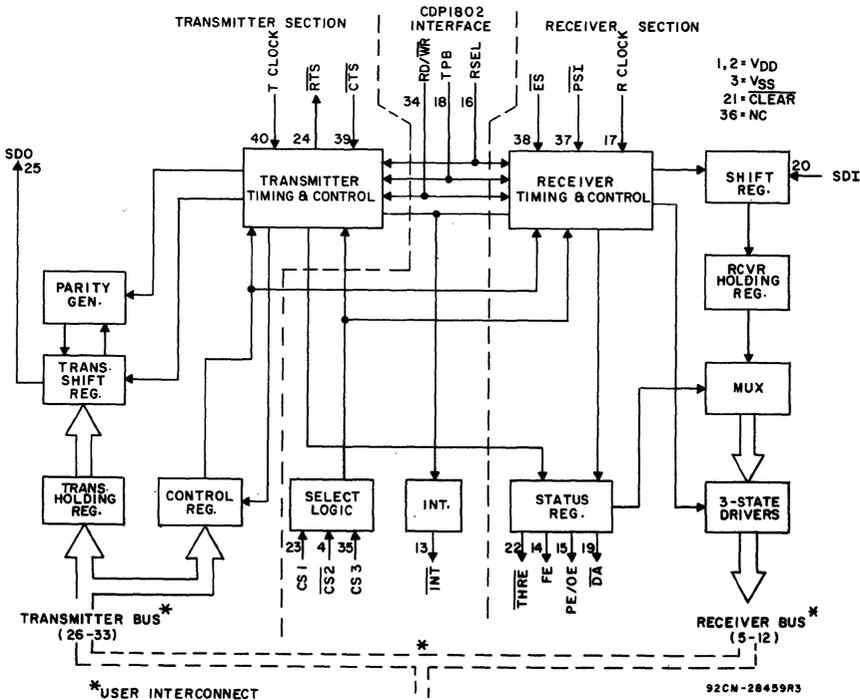


Fig. 1 - Mode 1 block diagram (CDP1800-series microprocessor compatible).

RCA CMOS LSI Products

CDP1854, CDP1854C

STATIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, unless otherwise noted.

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	CDP1854A			CDP1854AC			
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device Current, I_{DD}	—	0, 5	5	—	0.01	50	—	0.02	200	μA
	—	0, 10	10	—	1	200	—	—	—	
Output Low Drive (Sink) Current, I_{OL}	0.4	0, 5	5	0.55	1.1	—	0.55	1.1	—	mA
	0.5	0, 10	10	1.3	2.6	—	—	—	—	
Output High Drive (Source) Current, I_{OH} (Except pins 24 and 25)	4.6	0, 5	5	-0.55	-1.1	—	-0.55	-1.1	—	mA
	9.5	0, 10	10	-1.3	-2.6	—	—	—	—	
Output High Drive (Source) Current, I_{OH} Pins 24 and 25	4.6	0, 5	5	-1.6	-3.5	—	-1.6	-3.5	—	mA
	9.5	0, 10	10	-2.8	-6.0	—	—	—	—	
Output Voltage Low-Level, V_{OL}^*	—	0, 5	5	—	0	0.1	—	0	0.1	V
	—	0, 10	10	—	0	0.1	—	—	—	
Output Voltage High-Level, V_{OH}	—	0, 5	5	4.9	5	—	4.9	5	—	V
	—	0, 10	10	9.9	10	—	—	—	—	
Input Low Voltage, V_{IL}	0.5, 4.5	—	5	—	—	1.5	—	—	1.5	V
	0.5, 9.5	—	10	—	—	3	—	—	—	
Input High Voltage, V_{IH}	0.5, 4.5	—	5	3.5	—	—	3.5	—	—	V
	0.5, 9.5	—	10	7	—	—	—	—	—	
Input Current, I_{IN}	—	0, 5	5	—	—	± 1	—	—	± 1	μA
	—	0, 10	10	—	—	± 2	—	—	—	
3-State Output Leakage Current, I_{OUT}	0, 5	0, 5	5	—	—	± 1	—	—	± 1	μA
	0, 10	0, 10	10	—	—	± 10	—	—	—	
Operating Current, $I_{DD1}^\#$	—	0, 5	5	—	1.5	3.0	—	1.5	3.0	mA
	—	0, 10	10	—	6.0	12	—	—	—	
Input Capacitance, C_{IN}	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance, C_{OUT}	—	—	—	—	10	15	—	10	15	

*Typical values are for $T_A=25^\circ\text{C}$.

* $I_{OL}=I_{OH}=1\ \mu\text{A}$.

$^\#$ Operating current is measured at 200 kHz for $V_{DD}=5\ \text{V}$ and 400 kHz for $V_{DD}=10\ \text{V}$ in a CDP1800-series microprocessor system, with open outputs.

RECOMMENDED OPERATING CONDITIONS at T_A =Full Package Temperature Range

For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	CONDITIONS	LIMITS				UNITS
	V_{DD} V	CDP1854A		CDP1854AC		
		Min.	Max.	Min.	Max.	
DC Operating-Voltage Range	—	4	10.5	4	6.5	V
Input Voltage Range	—	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V
Baud Rate (Receive or Transmit)	5	—	200	—	200	K bits /sec
	10	—	400	—	—	

Functional Definitions for CDP1854A Terminals

Mode 1

CDP1800-Series Microprocessor Compatible

SIGNAL: FUNCTION

VDD:

Positive supply voltage

MODE SELECT (MODE):

A high-level voltage at this input selects CDP1800-series microprocessor Mode operation.

VSS:

Ground

CHIP SELECT 2 (CS2):

A low-level voltage at this input together with CS1 and CS3 selects the CDP1854A UART.

RECEIVER BUS (R BUS 7 - R BUS 0):

Receiver parallel data outputs (may be externally connected to corresponding transmitter bus terminals).

INTERRUPT (INT):

A low-level voltage at this output indicates the presence of one or more of the interrupt conditions listed in Table I.

FRAMING ERROR (FE):

A high-level voltage at this output indicates that the received character has no valid stop bit, i.e., the bit following the parity bit (if programmed) is not a high-level voltage. This output is updated each time a character is transferred to the Receiver Holding Register.

PARITY ERROR or OVERRUN ERROR (PE/OE):

A high-level voltage at this output indicates that either the PE or OE bit in the Status Register has been set (see Status Register Bit Assignment, Table II).

REGISTER SELECT (RSEL):

This input is used to choose either the Control/Status Registers (high input) or the transmitter/receiver data registers (low input) according to the truth table in Table III.

RECEIVER CLOCK (RCLOCK):

Clock input with a frequency 16 times the desired receiver shift rate.

TPB:

A positive input pulse used as a data load or reset strobe.

DATA AVAILABLE (DA):

A low-level voltage at this output indicates that an entire character has been received and transferred to the Receiver Holding Register.

SERIAL DATA IN (SDI):

Serial data received on this input line enters the Receiver Shift Register at a point determined by the character length. A high-level input voltage must be present when data is not being received.

CLEAR (CLEAR):

A low-level voltage at this input resets the Interrupt Flip-Flop, Receiver Holding Register, Control Register, and Status Register, and sets SERIAL DATA OUT (SDO) high.

TRANSMITTER HOLDING REGISTER EMPTY (THRE):

A low-level voltage at this output indicates that the Transmitter Holding Register has transferred its contents to the Transmitter Shift Register and may be reloaded with a new character.

CHIP SELECT 1 (CS1):

A high-level voltage at this input together with CS2 and CS3 selects the UART.

REQUEST TO SEND (RTS):

This output signal tells the peripheral to get ready to receive data. CLEAR TO SEND (CTS) is the response from the peripheral. RTS is set to a low-level voltage when data is latched in the Transmitter Holding Register or TR is set high, and is reset high when both the Transmitter Holding Register and Transmitter Shift Register are empty and TR is low.

SERIAL DATA OUTPUT (SDO):

The contents of the Transmitter Shift Register (start bit, data bits, parity bit, and stop bit(s)) are serially shifted out on this output. When no character is being transmitted, a high level is maintained. Start of transmission is defined as the transition of the start bit from a high-level to a low-level output voltage.

TRANSMITTER BUS (T BUS 0 - T BUS 7):

Transmitter parallel data input. These may be externally connected to corresponding Receiver bus terminals.

RD/WR:

A low-level voltage at this input gates data from the transmitter bus to the Transmitter Holding Register or the Control Register as chosen by register select. A high-level voltage gates data from the Receiver Holding Register or the Status Register, as chosen by register select, to the receiver bus.

CHIP SELECT 3 (CS3):

With high-level voltage at this input together with CS1 and CS2 selects the UART.

PERIPHERAL STATUS INTERRUPT (PSI):

A high-to-low transition on this input line sets a bit in the Status Register and causes an INTERRUPT (INT=low).

EXTERNAL STATUS (ES):

A low-level voltage at this input sets a bit in the Status Register.

CLEAR TO SEND (CTS):

When this input from peripheral is high, transfer of a character to the Transmitter Shift Register and shifting of serial data out is inhibited.

TRANSMITTER CLOCK (TCLOCK):

Clock input with a frequency 16 times the desired transmitter shift rate.

Table I — Interrupt Set and Reset Conditions

SET* (INT = LOW)	RESET (INT = HIGH)	
CAUSE	CONDITION	TIME
DA (Receipt of data)	Read of data	TPB leading edge
THRE* (Ability to reload)	Read of status or write of character	TPB leading edge
THRE · TSRE (Transmitter done)	Read of status or write of character	TPB leading edge
$\overline{\text{PSI}}$ (Negative edge)	Read of status	TPB trailing edge
$\overline{\text{CTS}}$ (Positive edge when $\overline{\text{THRE}} \cdot \overline{\text{TSRE}}$)	Read of status	TPB leading edge

*Interrupts will occur only after the IE bit in the Control Register (see Table IV) has been set.

*THRE will cause an interrupt only after the TR bit in the Control Register (see Table IV) has been set.

Table II — Status Register Bit Assignment

Bit	7	6	5	4	3	2	1	0
Signal	THRE	TSRE	PSI	ES	FE	PE	OE	DA
Also Available at Terminal	22*	—	—	—	14	15	15	19*

*Polarity reversed at output terminal.

Bit Signal: Function

0—DATA AVAILABLE (DA):

When set high, this bit indicates that an entire character has been received and transferred to the Receiver Holding Register. This signal is also available at Term. 19 but with its polarity reversed.

1—OVERRUN ERROR (OE):

When set high, this bit indicates that the Data Available bit was not reset before the next character was transferred to the Receiver Holding Register. This signal OR'ed with PE is output at Term. 15.

2—PARITY ERROR (PE):

When set high, this bit indicates that the received parity bit does not compare to that programmed by the EVEN PARITY ENABLE (EPE) control. This bit is updated each time a character is transferred to the Receiver Holding Register. This signal OR'ed with OE is output at Term. 15.

3—FRAMING ERROR (FE):

When set high, this bit indicates that the received character has no valid stop bit, i.e., the bit following the parity bit (if programmed) is not a high-level voltage. This bit is updated each time a character is transferred to the Receiver Holding Register. This signal is also available at Term. 14.

4—EXTERNAL STATUS (ES):

This bit is set high by a low-level input at Term. 38 ($\overline{\text{ES}}$).

5—PERIPHERAL STATUS INTERRUPT (PSI):

This bit is set high by a high-to-low voltage transition of Term. 37 ($\overline{\text{PSI}}$). The INTERRUPT output (Term. 13) is also asserted (INT=low) when this bit is set.

6—TRANSMITTER SHIFT REGISTER EMPTY (TSRE):

When set high, this bit indicates that the Transmitter Shift Register has completed serial transmission of a full character including stop bit(s). It remains set until the start of transmission of the next character.

7—TRANSMITTER HOLDING REGISTER EMPTY (THRE):

When set high, this bit indicates that the Transmitter Holding Register has transferred its contents to the Transmitter Shift Register and may be reloaded with a new character. Setting this bit also sets the $\overline{\text{THRE}}$ output (Term. 22) low and causes an INTERRUPT (INT=low), if TR is high.

Description of Mode 1 Operation CDP1800-Series Microprocessor Compatible (Mode Input=V_{DD})

1. Initialization and Controls

In the CDP1800-series microprocessor compatible mode, the CDP1854A is configured to receive commands and send status via the microprocessor data bus. The register connected to the transmitter bus or the receiver bus is determined by the RD/W_R and RSEL inputs as follows:

Table III — Register Selection Summary

RSEL	RD/W _R	Function
Low	Low	Load Transmitter Holding Register from Transmitter Bus
Low	High	Read Receiver Holding Register from Receiver Bus
High	Low	Load Control Register from Transmitter Bus
High	High	Read Status Register from Receiver Bus

In this mode the CDP1854A is compatible with a bidirectional bus system. The receiver and transmitter buses are connected to the bus. CDP1800-series microprocessor I/O control output signals can be connected directly to the CDP1854A inputs as shown in Fig. 2. The CLEAR input is pulsed, resetting the Control, Status, and Receiver Holding Registers and setting SERIAL DATA OUT (SDO) high. The Control Register is loaded from the Transmitter Bus in order to determine the operating configuration for the UART. Data is transferred from the Transmitter Bus inputs to the Control Register during TPB when the UART is selected CS1 · CS2 · CS3=1 and the Control Register is designated (RSEL=H, RD/W_R=L). The CDP1854A also has a Status Register which can be read onto the Receiver Bus (R BUS 0 - R BUS 7) in order to determine the status of the UART. Some of these status bits are also available at separate terminals as indicated in Table II.

2. Transmitter Operation

Before beginning to transmit, the TRANSMIT REQUEST (TR) bit in the Control Register (see bit assignment, Table IV) is set. Loading the Control Register with TR=1 (bit 7=high) inhibits changing the other control bits. Therefore two loads are required: one to format the UART, the second to set TR. When TR has been set, a TRANSMITTER HOLDING REGISTER EMPTY (THRE) interrupt will occur, signalling the microprocessor that the Transmitter Holding Register is empty and may be loaded. Setting TR also causes assertion of a low-level on the REQUEST TO SEND (RTS) output to the peripheral. It is not necessary to set TR for proper operation for the UART. If desired, it can be used to enable THRE interrupts and to generate the RTS signal. The Transmitter Holding Register is loaded from the bus by TPB during execution of an output instruction. The CDP1854A is selected by CS1 · CS2 · CS3=1, and the Holding Register is selected by RSEL=L and RD/W_R=L. When the CLEAR TO SEND (CTS) input, which can be connected to a peripheral device output, goes low, the Transmitter Shift Register will be loaded from the Transmitter Holding Register and data transmission will begin. If CTS is always low, the Transmitter Shift Register will be loaded on the first high-to-low edge of the clock which occurs at least 1/2 clock period after the trailing edge of TPB and transmission of a start bit will occur 1/2 clock period later (see Fig. 3). Parity (if programmed) and stop bit(s) will be transmitted following the last data bit. If the word length selected is less than 8 bits, the most significant unused bits in the transmitter shift register will not be transmitted.

One transmitter clock period after the Transmitter Shift Register is loaded from the Transmitter Holding Register, the THRE signal will go low and an interrupt will occur (INT goes low). The next character to be transmitted can then be loaded into the Transmitter Holding Register for transmission with its start bit immediately following the last stop bit of the previous character. This cycle can be repeated until the last character is transmitted, at which time a final THRE · TSRE interrupt will occur. This interrupt signals the microprocessor that TR can be turned off. This is done by reloading the original control byte in the Control Register with the TR bit = 0, thus terminating the REQUEST TO SEND (RTS) signal.

SERIAL DATA OUT (SDO) can be held low by setting the BREAK bit in the Control Register (see Table IV). SDO is held low until the BREAK bit is reset.

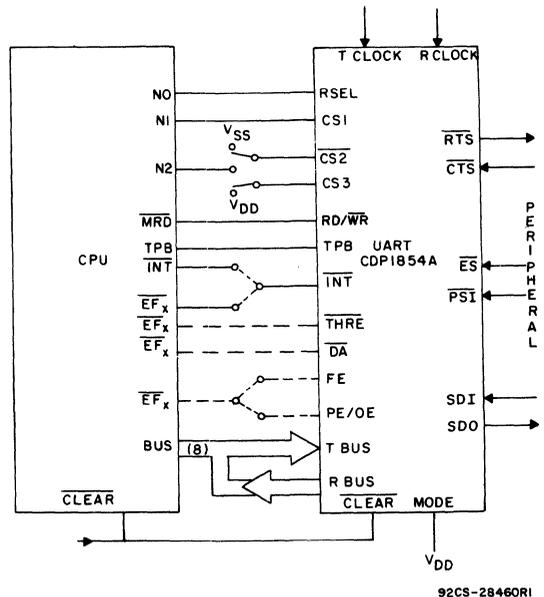


Fig. 2 - Recommended CDP1800-series connection, Mode 1 (non-interrupt driven system).

3. Receiver Operation

The receive operation begins when a start bit is detected at the SERIAL DATA IN (SDI) input. After detection of the first high-to-low transition on the SDI line, a valid start bit is verified by checking for a low-level input 7-1/2 receiver clock periods later. When a valid start bit has been verified, the following data bits, parity bit (if programmed) and stop bit(s) are shifted into the Receiver Shift Register by clock pulse 7-1/2 in each bit time. The parity bit (if programmed) is checked and receipt of a valid stop bit is verified. On count 7-1/2 of the first stop bit, the received data is loaded into the Receiver Holding Register. If the word length is less than 8 bits, zeros (low output level) are loaded into the unused most significant bits. If DATA AVAILABLE (DA) has not been reset by the time the Receiver Holding Register is loaded, the OVERRUN ERROR (OE) status bit is set. One half clock period later, the PARITY ERROR (PE) and FRAMING ERROR (FE) status bits become valid for the character in the Receiver Holding Register. At this time, the Data Available status bit is also set and the DATA AVAILABLE (DA) and INTERRUPT (INT) outputs go low, signalling the microprocessor that a received character is

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ready. The microprocessor responds by executing an input instruction. The UART's 3-state bus drivers are enabled when the UART is selected ($CS1 \cdot CS2 \cdot CS3=1$) and $RD/WR=high$. Status can be read when $RSEL=high$. Data is read when $RSEL=low$. When reading data, TPB latches data in the microprocessor and resets DATA AVAILABLE (DA) in the UART. The preceding sequence is repeated for each serial character which is received from the peripheral.

4. Peripheral Interface

In addition to serial data in and out, four signals are

provided for communication with a peripheral. The REQUEST TO SEND (RTS) output signal alerts the peripheral to get ready to receive data. The CLEAR TO SEND (CTS) input signal is the response, signalling that the peripheral is ready. The EXTERNAL STATUS (ES) input latches a peripheral status level, and the PERIPHERAL STATUS INTERRUPT (PSI) input senses a status edge (high-to-low) and also generates an interrupt. For example, the modem DATA CARRIER DETECT line could be connected to the PSI input on the UART in order to signal the microprocessor that transmission failed because of loss of the carrier on the communications line. The PSI and ES bits are stored in the Status Register (see Table II).

Table IV — Control Register Bit Assignment

Bit	7	6	5	4	3	2	1	0
Signal	TR	BREAK	IE	WLS2	WLS1	SBS	EPE	PI

Bit Signal: Function

0—PARITY INHIBIT (PI):

When set high parity generation and verification are inhibited and the PE Status bit is held low. If parity is inhibited the stop bit(s) will immediately follow the last data bit on transmission, and EPE is ignored.

1—EVEN PARITY ENABLE (EPE):

When set high, even parity is generated by the transmitter and checked by the receiver. When low, odd parity is selected.

2—STOP BIT SELECT (SBS):

See table below.

3—WORD LENGTH SELECT 1 (WLS1):

See table below.

4—WORD LENGTH SELECT 2 (WLS2):

See table below.

5—INTERRUPT ENABLE (IE):

When set high THRE, DA, THRE · TSRE, CTS, and PSI interrupts are enabled (see Interrupt Conditions, Table I).

6—TRANSMIT BREAK (BREAK):

Holds SDO low when set. Once the break bit in the control register has been set high, SDO will stay low until the break bit is reset low and one of the following occurs: CLEAR goes low; CTS goes high; or a word is transmitted. (The transmitted word will not be valid since there can be no start bit if SDO is already low. SDO can be set high without intermediate transitions by transmitting a word consisting of all zeros).

7—TRANSMIT REQUEST (TR):

When set high, RTS is set low and data transfer through the transmitter is initiated by the initial THRE interrupt. (When loading the Control Register from the bus, this (TR) bit inhibits changing of other control flip-flops).

Bit 4	Bit 3	Bit 2	Function
WLS2	WLS1	SBS	
0	0	0	5 data bits, 1 stop bit
0	0	1	5 data bits, 1.5 stop bits
0	1	0	6 data bits, 1 stop bit
0	1	1	6 data bits, 2 stop bits
1	0	0	7 data bits, 1 stop bit
1	0	1	7 data bits, 2 stop bits
1	1	0	8 data bits, 1 stop bit
1	1	1	8 data bits, 2 stop bits

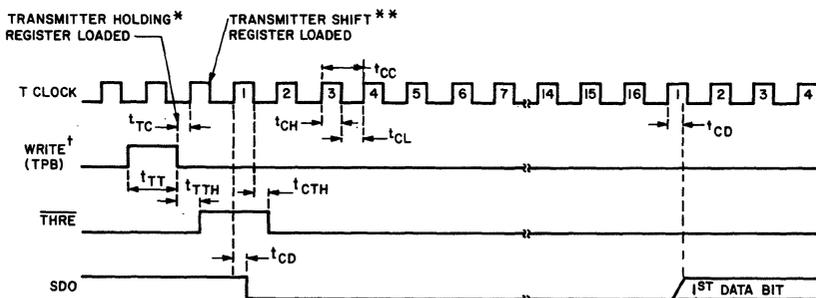
1800-Series Peripherals
CDP1854, CDP1854C

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} \pm 5\%$, $t_r, t_f = 20$ ns, $V_{IH} = 0.7 V_{DD}$, $V_{IL} = 0.3 V_{DD}$, $C_L = 100$ pF, see Fig. 3.

CHARACTERISTIC	V _{DD} (V)	LIMITS				UNITS	
		CDP1854A		CDP1854AC			
		Typ. [†]	Max.*	Typ. [†]	Max.*		
Transmitter Timing — Mode 1							
Minimum Clock Period	t_{CC}	5	250	310	250	310	ns
		10	125	155	—	—	
Minimum Pulse Width: Clock Low Level	t_{CL}	5	100	125	100	125	ns
		10	75	100	—	—	
Clock High Level	t_{CH}	5	100	125	100	125	ns
		10	75	100	—	—	
TPB	t_{TT}	5	100	150	100	150	ns
		10	50	75	—	—	
Minimum Setup Time: TPB to Clock	t_{TC}	5	175	225	175	225	ns
		10	90	150	—	—	
Propagation Delay Time: Clock to Data Start Bit	t_{CD}	5	300	450	300	450	ns
		10	150	225	—	—	
TPB to <u>THRE</u>	t_{TTH}	5	200	300	200	300	ns
		10	100	150	—	—	
Clock to <u>THRE</u>	t_{CTH}	5	200	300	200	300	ns
		10	100	150	—	—	

[†]Typical values are for $T_A = 25^\circ\text{C}$ and nominal voltages.

*Maximum limits of minimum characteristics are the values above which all devices function.



- * THE HOLDING REGISTER IS LOADED ON THE TRAILING EDGE OF TPB.
- ** THE TRANSMITTER SHIFT REGISTER IS LOADED ON THE FIRST HIGH-TO-LOW TRANSITION OF THE CLOCK WHICH OCCURS AT LEAST 1/2 CLOCK PERIOD + t_{TC} AFTER THE TRAILING EDGE OF TPB, AND TRANSMISSION OF A START BIT OCCURS 1/2 CLOCK PERIOD + t_{CD} LATER.
- † WRITE IS THE OVERLAP OF TPB, CSI, AND CS3 = 1 AND CS3, RD / WR = 0.

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Fig. 3 - Transmitter timing diagram - Mode 1.

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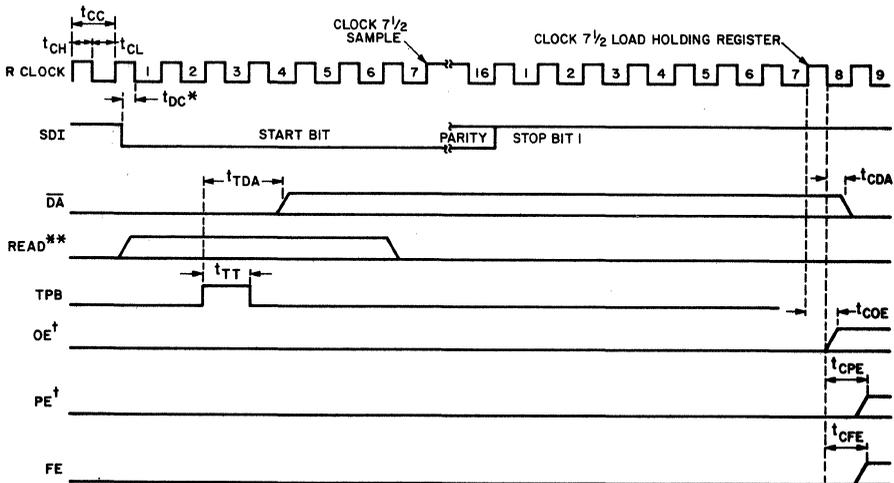
CDP1854, CDP1854C

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} \pm 5\%$, $t_r, t_f = 20$ ns, $V_{IH} = 0.7 V_{DD}$, $V_{IL} = 0.3 V_{DD}$, $C_L = 100$ pF, see Fig. 4.

CHARACTERISTIC	V _{DD} (V)	LIMITS				UNITS	
		CDP1854A		CDP1854AC			
		Typ. [†]	Max.*	Typ. [†]	Max.*		
Receiver Timing — Mode 1							
Minimum Clock Period	t_{CC}	5 10	250 125	310 155	250 —	310 —	ns
Minimum Pulse Width:		5	100	125	100	125	ns
Clock Low Level	t_{CL}	10	75	100	—	—	ns
Clock High Level	t_{CH}	5 10	100 75	125 100	100 —	125 —	ns
TPB	t_{TT}	5 10	100 50	150 75	100 —	150 —	ns
Minimum Setup Time:		5	100	150	100	150	ns
Data Start Bit to Clock	t_{DC}	10	50	75	—	—	ns
Propagation Delay Time:		5	220	325	220	325	ns
TPB to DATA AVAILABLE	t_{TDA}	10	110	175	—	—	ns
Clock to DATA AVAILABLE	t_{CDA}	5 10	220 110	325 175	220 —	325 —	ns
Clock to Overrun Error	t_{COE}	5 10	210 105	300 150	210 —	300 —	ns
Clock to Parity Error	t_{CPE}	5 10	240 120	375 175	240 —	375 —	ns
Clock to Framing Error	t_{CFE}	5 10	200 100	300 150	200 —	300 —	ns

[†]Typical values are for $T_A = 25^\circ\text{C}$ and nominal voltages.

*Maximum limits of minimum characteristics are the values above which all devices function.



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* IF A START BIT OCCURS AT A TIME LESS THAN t_{DC} BEFORE A HIGH-TO-LOW TRANSITION OF THE CLOCK, THE START BIT MAY NOT BE RECOGNIZED UNTIL THE NEXT HIGH-TO-LOW TRANSITION OF THE CLOCK. THE START BIT MAY BE COMPLETELY ASYNCHRONOUS WITH THE CLOCK.

** READ IS THE OVERLAP OF $CS1$, $CS3$, $RD/\overline{WR} = 1$ AND $CS2 = 0$. IF A PENDING DA HAS NOT BEEN CLEARED BY A READ OF THE RECEIVER HOLDING REGISTER, THE OE SIGNAL WILL COME TRUE. TIME A NEW WORD IS LOADED INTO THE RECEIVER HOLDING REGISTER.

† OE AND PE SHARE TERMINAL 15 AND ARE ALSO AVAILABLE AS TWO SEPARATE BITS IN THE STATUS REGISTER

Fig. 4 - Mode 1 receiver timing diagram.

1800-Series Peripherals
CDP1854, CDP1854C

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} \pm 5\%$, $t_r, t_f = 20$ ns, $V_{IH} = 0.7 V_{DD}$, $V_{IL} = 0.3 V_{DD}$, $C_L = 100$ pF, see Fig. 5.

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS	
		CDP1854A		CDP1854AC			
		Typ.†	Max.*	Typ.†	Max.*		
CPU Interface — WRITE Timing — Mode 1							
Minimum Pulse Width: TPB	t_{TT}	5	100	150	100	150	ns
		10	50	75	—	—	
Minimum Setup Time: RSEL to Write	t_{RSW}	5	50	75	50	75	ns
		10	25	40	—	—	
Data to Write	t_{DW}	5	-100	-75	-100	-75	ns
		10	-50	-35	—	—	
Minimum Hold Time: RSEL after Write	t_{WRS}	5	50	75	50	75	ns
		10	25	40	—	—	
Data after Write	t_{WD}	5	75	125	75	125	ns
		10	40	60	—	—	

†Typical values are for $T_A = 25^\circ\text{C}$ and nominal voltages.

*Maximum limits of minimum characteristics are the values above which all devices function.

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} \pm 5\%$, $t_r, t_f = 20$ ns, $V_{IH} = 0.7 V_{DD}$, $V_{IL} = 0.3 V_{DD}$, $C_L = 100$ pF, see Fig. 6.

CHARACTERISTIC	V_{DD} (V)	LIMITS						UNITS	
		CDP1854A			CDP1854AC				
		Min.	Typ.†	Max.*	Min.	Typ.†	Max.*		
CPU Interface — READ Timing — Mode 1									
Minimum Pulse Width: TPB	t_{TT}	5	—	100	150	—	100	150	ns
		10	—	50	75	—	—	—	
Minimum Setup Time: RSEL to TPB	t_{RST}	5	—	50	75	—	50	75	ns
		10	—	25	40	—	—	—	
Minimum Hold Time: RSEL after TPB	t_{TRS}	5	—	50	75	—	50	75	ns
		10	—	25	40	—	—	—	
Read to Data Access Time	t_{RDDA}	5	—	200	300	—	200	300	ns
		10	—	100	150	—	—	—	
Read to Data Valid Time	t_{RDV}	5	—	200	300	—	200	300	ns
		10	—	100	150	—	—	—	
RSEL to Data Valid Time	t_{RSDV}	5	—	150	225	—	150	225	ns
		10	—	75	125	—	—	—	
Hold Time: Data after Read	t_{RDH}	5	50	150	—	50	150	—	ns
		10	25	75	—	—	—	—	

†Typical values are for $T_A = 25^\circ\text{C}$ and nominal voltages.

*Maximum limits of minimum characteristics are the values above which all devices function.

RCA CMOS LSI Products
CDP1854, CDP1854C

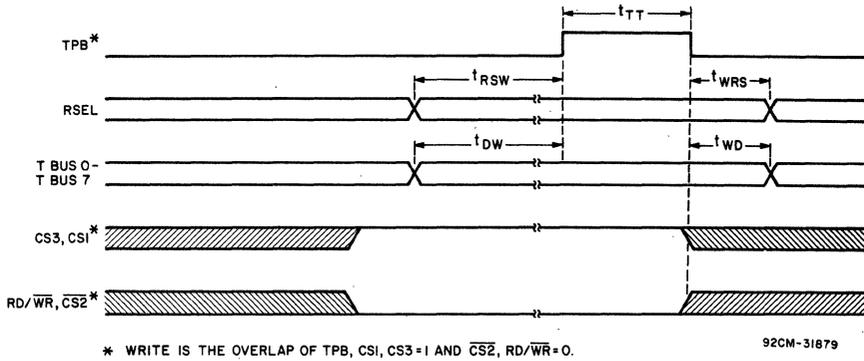


Fig. 5 - Mode 1 CPU interface (WRITE) timing diagram.

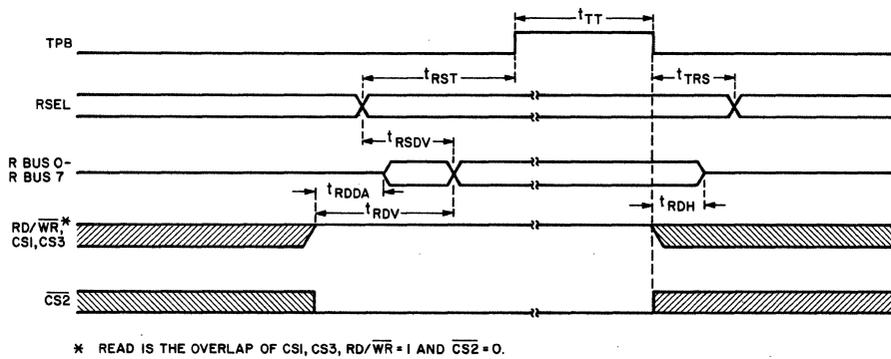


Fig. 6 - Mode 1 CPU interface (READ) timing diagram.

Mode Input Low (Mode = 0)

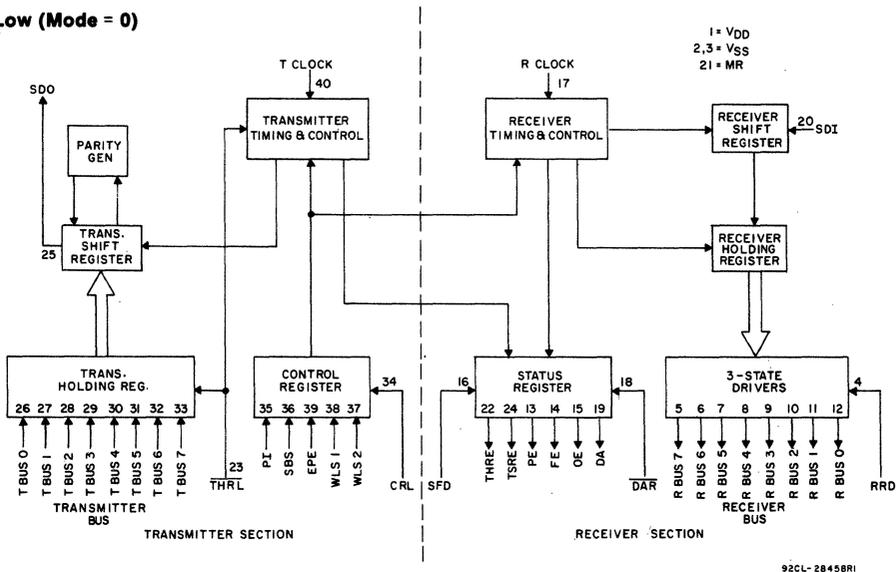


Fig. 7 - Mode 0 block diagram (industry standard compatible).

**Functional Definitions for CDP1854A Terminals
 Standard Mode 0**

SIGNAL: FUNCTION

VDD:

Positive supply voltage.

MODE SELECT (MODE):

A low-level voltage at this input selects Standard Mode 0 Operation.

VSS:

Ground.

RECEIVER REGISTER DISCONNECT (RRD):

A high-level voltage applied to this input disconnects the Receiver Holding Register from the Receiver Bus.

RECEIVER BUS (R BUS 7 - R BUS 0):

Receiver parallel data outputs.

PARITY ERROR (PE):

A high-level voltage at this output indicates that the received parity does not compare to that programmed by the EVEN PARITY ENABLE (EPE) control. This output is updated each time a character is transferred to the Receiver Holding Register. PE lines from a number of arrays can be bused together since an output disconnect capability is provided by the STATUS FLAG DISCONNECT (SFD) line.

FRAMING ERROR (FE):

A high-level voltage at this output indicates that the received character has no valid stop bit, i.e., the bit following the parity bit (if programmed) is not a high-level voltage. This output is updated each time a character is transferred to the Receiver Holding Register. FE lines from a number of arrays can be bused together since an output disconnect capability is provided by the STATUS FLAG DISCONNECT (SFD) line.

OVERRUN ERROR (OE):

A high-level voltage at this output indicates that the DATA AVAILABLE (DA) flag was not reset before the next character was transferred to the Receiver Holding Register. OE lines from a number of arrays can be bused together since an output disconnect capability is provided by the STATUS FLAG DISCONNECT (SFD) line.

STATUS FLAG DISCONNECT (SFD):

A high-level voltage applied to this input disables the 3-state output drivers for PE, FE, OE, DA, and THRE, allowing these status outputs to be bus connected.

RECEIVER CLOCK (RCLOCK):

Clock input with a frequency 16 times the desired receiver shift rate.

DATA AVAILABLE RESET (DAR):

A low-level voltage applied to this input resets the DA flip-flop.

DATA AVAILABLE (DA):

A high-level voltage at this output indicates that an entire character has been received and transferred to the Receiver Holding Register.

SERIAL DATA IN (SDI):

Serial data received at this input enters the receiver shift register at a point determined by the character length. A high-level voltage must be present when data is not being received.

MASTER RESET (MR):

A high-level voltage at this input resets the Receiver Holding Register, Control Register, and Status Register, and sets the serial data output high.

TRANSMITTER HOLDING REGISTER EMPTY (THRE):

A high-level voltage at this output indicates that the Transmitter Holding Register has transferred its contents to the Transmitter Shift Register and may be reloaded with a new character.

TRANSMITTER HOLDING REGISTER LOAD (THRL):

A low-level voltage applied to this input enters the character on the bus into the Transmitter Holding Register. Data is latched on the trailing edge of this signal.

TRANSMITTER SHIFT REGISTER EMPTY (TSRE):

A high-level voltage at this output indicates that the Transmitter Shift Register has completed serial transmission of a full character including stop bit(s). It remains at this level until the start of transmission of the next character.

SERIAL DATA OUTPUT (SDO):

Contents of the Transmitter Shift Register (start bit, data bits, parity bit, and stop (bit(s)) are serially shifted out on this output. When no character is being transmitted, a high-level is maintained. Start of transmission is defined as the transition of the start bit from a high-level to a low-level output voltage.

TRANSMITTER BUS (T BUS 0 - T BUS 7):

Transmitter parallel data inputs.

CONTROL REGISTER LOAD (CRL):

A high-level voltage at this input loads the Control Register with the control bits (PI, EPE, SBS, WLS1, WLS2). This line may be strobed or hardwired to a high-level input voltage.

PARITY INHIBIT (PI):

A high-level voltage at this input inhibits the parity generation and verification circuits and will clamp the PE output low. If parity is inhibited the stop bit(s) will immediately follow the last data bit on transmission.

STOP BIT SELECT (SBS):

This input selects the number of stop bits to be transmitted after the parity bit. A high-level selects two stop bits, a low-level selects one stop bit. Selection of two stop bits with five data bits programmed selects 1.5 stop bits.

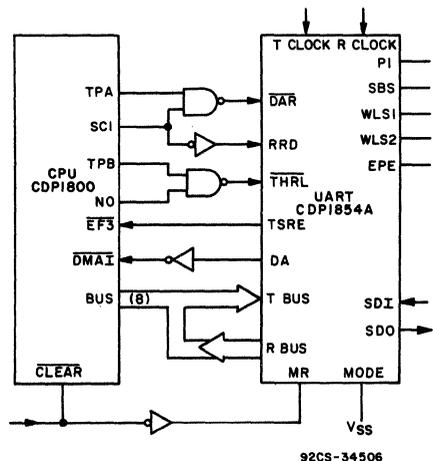


Fig. 8 - Mode 0 connection diagram.

WORD LENGTH SELECT 2 (WLS2):

WORD LENGTH SELECT 1 (WLS1):

These two inputs select the character length (exclusive of parity) as follows:

WLS2	WLS1	Word Length
Low	Low	5 Bits
Low	High	6 Bits
High	Low	7 Bits
High	High	8 Bits

EVEN PARITY ENABLE (EPE):

A high-level voltage at this input selects even parity to be generated by the transmitter and checked by the receiver. A low-level input selects odd parity.

TRANSMITTER CLOCK (TCLOCK):

Clock input with a frequency 16 times the desired transmitter shift rate.

Description of Standard Mode 0 Operation (Mode Input=V_{SS})

1. Initialization and Controls

The MASTER RESET (MR) input is pulsed, resetting the Control, Status, and Receiver Holding Registers and setting the SERIAL DATA OUTPUT (SDO) signal high. Timing is generated from the clock inputs, Transmitter Clock (TCLOCK) and Receiver Clock (RCLOCK), at a frequency equal to 16 times the serial data bit rate. When the receiver data input rate and the transmitter data output rate are the same, the TCLOCK and RCLOCK inputs may be connected together. The CONTROL REGISTER LOAD (CRL) input is pulsed to store the control inputs PARITY INHIBIT (PI), EVEN PARITY ENABLE (EPE), STOP BIT SELECT (SBS), and WORD LENGTH SELECTs (WLS1 and WLS2). These inputs may be hardwired to the proper voltage levels (V_{SS} or V_{DD}) instead of being dynamically set and CRL may be hardwired to V_{DD}. The CDP1854A is then ready for transmitter and/or receiver operation.

2. Transmitter Operation

For the transmitter timing diagram refer to Fig. 10. At the beginning of a typical transmitting sequence the Transmitter Holding Register is empty (THRE is HIGH). A character is transferred from the transmitter bus to the Transmitter

holding Register by applying a low pulse to the TRANSMITTER HOLDING REGISTER LOAD (THRL) input causing THRE to go low. If the Transmitter Shift Register is empty (TSRE is HIGH) and the clock is low, on the next high-to-low transition of the clock the character is loaded into the Transmitter Shift Register preceded by a start bit. Serial data transmission begins 1/2 clock period later with a start bit and 5-8 data bits followed by the parity bit (if programmed) and stop bit(s). The THRE output signal goes high 1/2 clock period later on the high-to-low transition of the clock. When THRE goes high, another character can be loaded into the Transmitter Holding Register for transmission beginning with a start bit immediately following the last stop bit of the previous character. This process is repeated until all characters have been transmitted. When transmission is complete, THRE and Transmitter Shift Register Empty (TSRE) will both be high. The format of serial data is shown in Fig. 12. Duration of each serial output data bit is determined by the transmitter clock frequency (f_{CLOCK}) and will be 16/f_{CLOCK}.

3. Receiver Operation

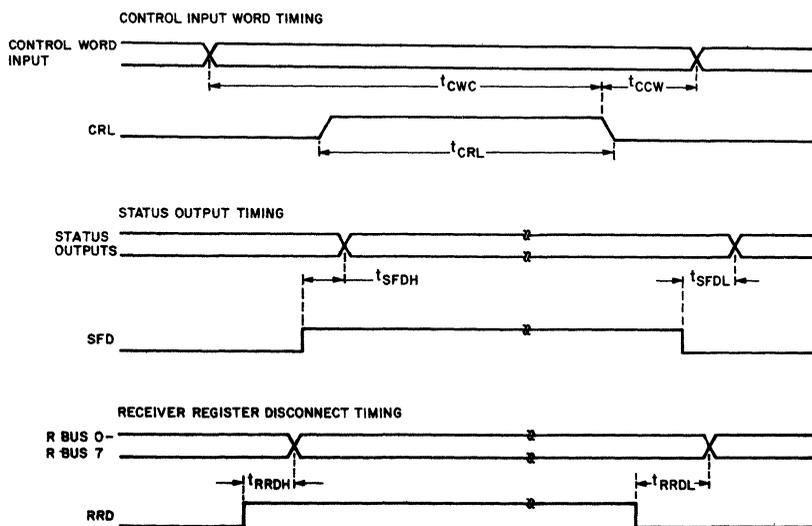
The receive operation begins when a start bit is detected at the SERIAL DATA IN (SDI) input. After the detection of a high-to-low transition on the SDI line, a divide-by-16 counter is enabled and a valid start bit is verified by checking for a low-level input 7-1/2 receiver clock periods later. When a valid start bit has been verified, the following data bits, parity bit (if programmed), and stop bit(s) are shifted into the Receiver Shift Register at clock pulse 7-1/2 in each bit time. If programmed, the parity bit is checked, and receipt of a valid stop bit is verified. On count 7-1/2 of the first stop bit, the received data is loaded into the Receiver Holding Register. If the word length is less than 8 bits, zeros (low output voltage level) are loaded into the unused most significant bits. If DATA AVAILABLE (DA) has not been reset by the time the Receiver Holding Register is loaded, the OVERRUN ERROR (OE) signal is raised. One-half clock period later, the PARITY ERROR (PE) and FRAMING ERROR (FE) signals become valid for the character in the Receiver Holding Register. The DA signal is also raised at this time. The 3-state output drivers for DA, OE, PE and FE are enabled when STATUS FLAG DISCONNECT (SFD) is low. When RECEIVER REGISTER DISCONNECT (RRD) goes low, the receiver bus 3-state output drivers are enabled and data is available at the RECEIVER BUS (R BUS 0 - R BUS 7) outputs. Applying a negative pulse to the DATA AVAILABLE RESET (DAR) resets DA. The preceding sequence of operation is repeated for each serial character received. A receiver timing diagram is shown in Fig. 11.

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} \pm 5\%$, $t_r, t_f = 20$ ns, $V_{IH} = 0.7 V_{DD}$, $V_{IL} = 0.3 V_{DD}$, $C_L = 100$ pF, see Fig. 9.

CHARACTERISTIC	V _{DD} (V)	LIMITS				UNITS
		CDP1854A		CDP1854C		
		Typ. [†]	Max.*	Typ. [†]	Max.*	
Interface Timing — Mode 0						
Minimum Pulse Width: CRL	5 10	50 40	150 100	50 —	150 —	ns
Minimum Pulse Width: MR	5 10	300 150	400 200	300 —	400 —	ns
Minimum Setup Time: Control Word to CRL	5 10	20 0	50 40	20 —	50 —	ns
Minimum Hold Time: Control Word after CRL	5 10	40 20	60 30	40 —	60 —	ns
Propagation Delay Time: SFD High to SOD	5 10	200 100	300 150	200 —	300 —	ns
SFD Low to SOD	5 10	75 40	120 60	75 —	120 —	ns
RRD High to Receiver Register High Impedance	5 10	200 100	300 150	200 —	300 —	ns
RRD Low to Receiver Register Active	5 10	80 40	150 70	80 —	150 —	ns

[†]Typical values are for $T_A = 25^\circ\text{C}$ and nominal voltages.

*Maximum limits of minimum characteristics are the values above which all devices function.



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Fig. 9 - Mode 0 interface timing diagram.

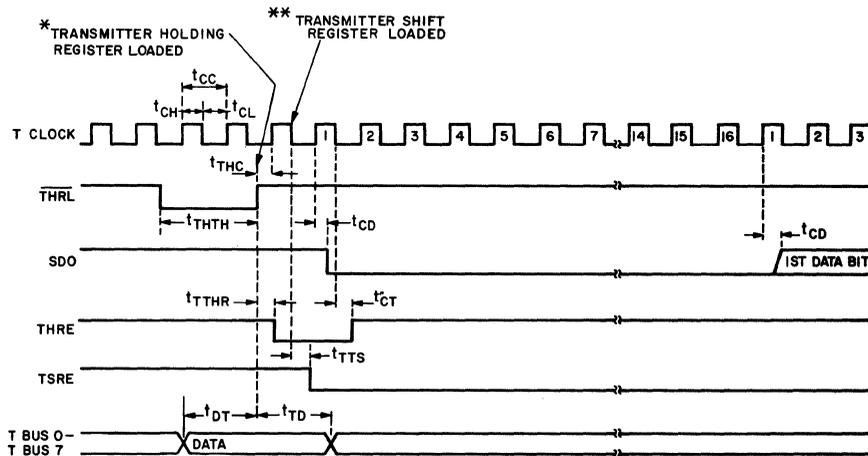
CDP1854, CDP1854C

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} \pm 5\%$, $t_r, t_f = 20$ ns, $V_{IH} = 0.7 V_{DD}$, $V_{IL} = 0.3 V_{DD}$, $C_L = 100$ pF, see Fig. 10.

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS	
		CDP1854A		CDP1854AC			
		Typ. [†]	Max.*	Typ. [†]	Max.*		
Transmitter Timing — Mode 0							
Minimum Clock Period	t_{CC}	5	250	310	250	310	ns
Minimum Pulse Width: Clock Low Level	t_{CL}	5	100	125	100	125	ns
		10	75	100	—	—	
Clock High Level	t_{CH}	5	100	125	100	125	ns
		10	75	100	—	—	
$\overline{\text{THRL}}$	t_{THTH}	5	60	150	60	150	ns
		10	40	100	—	—	
Minimum Setup Time: $\overline{\text{THRL}}$ to Clock	t_{THC}	5	175	275	175	275	ns
		10	90	150	—	—	
Data to $\overline{\text{THRL}}$	t_{DT}	5	20	50	20	50	ns
		10	0	40	—	—	
Minimum Hold Time: Data after $\overline{\text{THRL}}$	t_{TD}	5	40	60	40	60	ns
		10	20	30	—	—	
Propagation Delay Time: Clock to Data Start Bit	t_{CD}	5	300	450	300	450	ns
		10	150	225	—	—	
Clock to THRE	t_{CT}	5	200	300	200	300	ns
		10	100	150	—	—	
$\overline{\text{THRL}}$ to THRE	t_{TTHR}	5	200	300	200	300	ns
		10	100	150	—	—	
Clock to TSRE	t_{TTS}	5	200	300	200	300	ns
		10	100	150	—	—	

[†]Typical values are for $T_A = 25^\circ\text{C}$ and nominal voltages.

*Maximum limits of minimum characteristics are the values above which all devices function.



- * THE HOLDING REGISTER IS LOADED ON THE TRAILING EDGE OF $\overline{\text{THRL}}$.
- ** THE TRANSMITTER SHIFT REGISTER, IF EMPTY, IS LOADED ON THE FIRST HIGH-TO-LOW TRANSITION OF THE CLOCK WHICH OCCURS AT LEAST $1/2$ CLOCK PERIOD + t_{THC} AFTER THE TRAILING EDGE OF $\overline{\text{THRL}}$, AND TRANSMISSION OF A START BIT OCCURS $1/2$ CLOCK PERIOD + t_{CD} LATER.

92CM-31876R1

Fig. 10 - Mode 0 transmitter timing diagram.

1800-Series Peripherals
CDP1854, CDP1854C

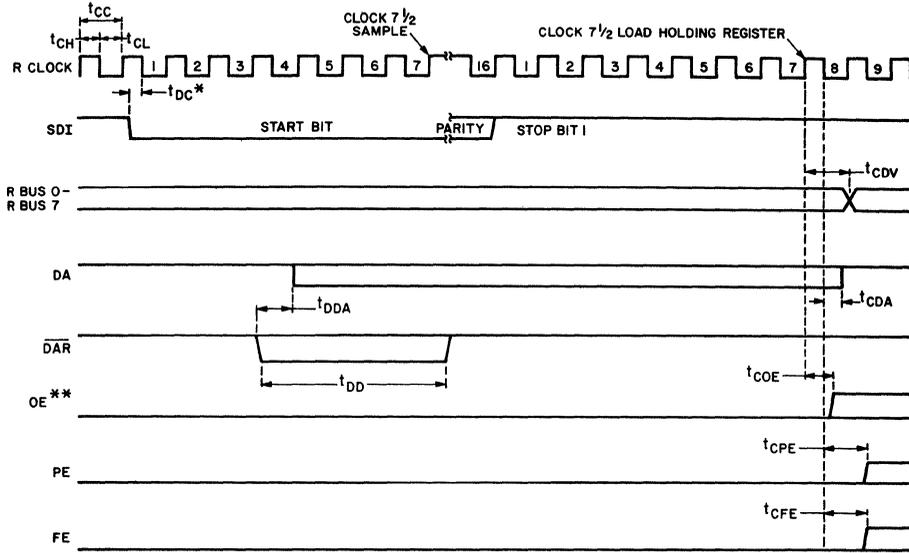
DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} \pm 5\%$, $t_r, t_f = 20$ ns, $V_{IH} = 0.7 V_{DD}$, $V_{IL} = 0.3 V_{DD}$, $C_L = 100$ pF, see Fig. 11.

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS	
		CDP1854A		CDP1854AC			
		Typ. [†]	Max.*	Typ. [†]	Max.*		
Receiver Timing — Mode 0							
Minimum Clock Period	t_{CC}	5	250	310	250	310	ns
		10	125	155	—	—	
Minimum Pulse Width: Clock Low Level	t_{CL}	5	100	125	100	125	ns
		10	75	100	—	—	
Clock High Level	t_{CH}	5	100	125	100	125	ns
		10	75	100	—	—	
DATA AVAILABLE RESET	t_{DD}	5	50	75	50	75	ns
		10	25	40	—	—	
Minimum Setup Time: Data Start Bit to Clock	t_{DC}	5	100	150	100	150	ns
		10	50	75	—	—	
Propagation Delay Time: DATA AVAILABLE RESET to Data Available	t_{DDA}	5	150	225	150	225	ns
		10	75	125	—	—	
Clock to Data Valid	t_{CDV}	5	225	325	225	325	ns
		10	110	175	—	—	
Clock to Data Available	t_{CDA}	5	225	325	225	325	ns
		10	110	175	—	—	
Clock to Overrun Error	t_{COE}	5	210	300	210	300	ns
		10	100	150	—	—	
Clock to Parity Error	t_{CPE}	5	240	375	240	375	ns
		10	120	175	—	—	
Clock to Framing Error	t_{CFE}	5	200	300	200	300	ns
		10	100	150	—	—	

[†]Typical values are for $T_A = 25^\circ\text{C}$ and nominal voltages.

*Maximum limits of minimum characteristics are the values above which all devices function.

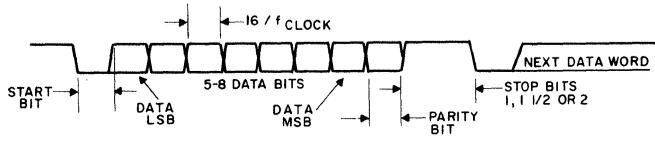
RCA CMOS LSI Products
CDP1854, CDP1854C



- * IF A START BIT OCCURS AT A TIME LESS THAN t_{DC} BEFORE A HIGH-TO-LOW TRANSITION OF THE CLOCK, THE START BIT MAY NOT BE RECOGNIZED UNTIL THE NEXT HIGH-TO-LOW TRANSITION OF THE CLOCK. THE START BIT MAY BE COMPLETELY ASYNCHRONOUS WITH THE CLOCK.
- ** IF A PENDING DA HAS NOT BEEN CLEARED BY A READ OF THE RECEIVER HOLDING REGISTER BY THE TIME A NEW WORD IS LOADED INTO THE RECEIVER HOLDING REGISTER, THE OE SIGNAL WILL COME TRUE.

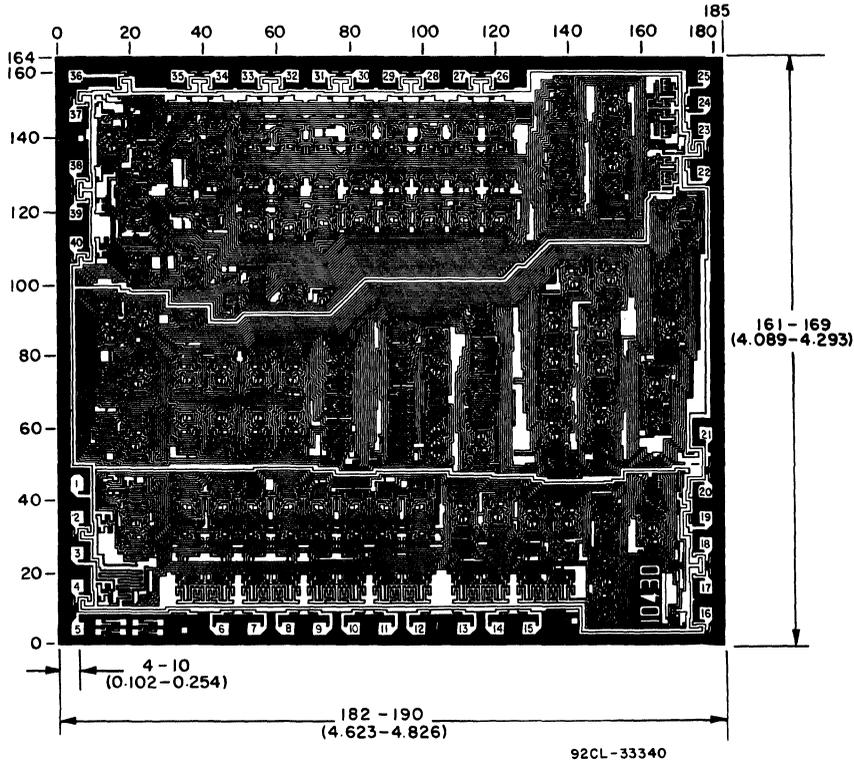
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Fig. 11 - Mode 0 receiver timing diagram.



92CS - 28463

Fig. 12 - Serial data word format.



Dimensions and pad layout for CDP1854ACH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

OPERATING AND HANDLING CONSIDERATIONS

1. Handling

All inputs and outputs of RCA CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in ICAN-6525 "Guide to Better Handling and Operation of CMOS Integrated Circuits."

2. Operating

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause $V_{DD}-V_{SS}$ to exceed the absolute maximum rating.

Input Signals

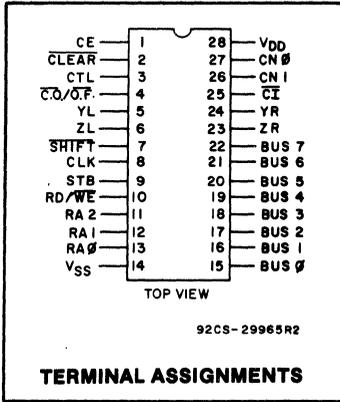
To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS} . Input currents must not exceed 10 mA even when the power supply is off.

Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS} , whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} or V_{SS} may damage CMOS devices by exceeding the maximum device dissipation.



8-Bit Programmable Multiply/Divide Unit

Features:

- Cascadable up to 4 units for 32-bit by 32-bit multiply or 64 ÷ 32 bit divide
- 8-bit by 8-bit multiply or 16 ÷ 8 bit divide in 5.6 μs at 5 V or 2.8 μs at 10 V
- Direct interface to CDP1800 Series microprocessors
- Easy interface to other 8-bit microprocessors
- Significantly increases throughput of microprocessor used for arithmetic calculations

The RCA-CDP1855 and CDP1855C are CMOS 8-bit multiply/divide units which can be used to greatly increase the capabilities of 8-bit microprocessors. They perform multiply and divide operations on unsigned, binary operators. In general, microprocessors do not contain multiple or divide instructions and even efficiently coded multiply or divide subroutines require considerable memory and execution time. These multiply/divide units directly interface to the CDP1800 series microprocessors via the N-lines and can easily be configured to fit in either the memory or I/O space of other 8-bit microprocessors.

The multiple/divide unit is based on a method of multiplying

by add and shift right operations and dividing by subtract and shift left operations. The device is structured to permit cascading identical units to handle operands up to 32 bits.

The CDP1855 and CDP1855C are functionally identical. They differ in that the CDP1855 has a recommended operating voltage range of 4 — 10.5 volts, and the CDP1855C, a recommended operating voltage range of 4 — 6.5 volts.

The CDP1855 and CDP1855C types are supplied in a 28-lead hermetic dual-in-line ceramic package (D suffix) and in a 28-lead dual-in-line plastic package (E suffix). The CDP1855C is also available in chip form (H suffix).

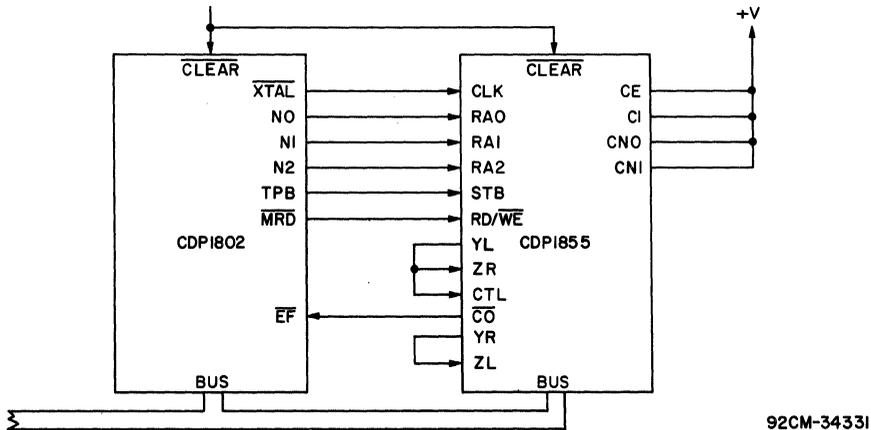


Fig. 1 - Circuit configuration for MDU addressed as an I/O device.

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltage referenced to V_{SS} Terminal)
CDP1855 -0.5 to +11 V
CDP1855C -0.5 to +7 V

INPUT VOLTAGE RANGE, ALL INPUTS -0.5 to V_{DD} +0.5 V

DC INPUT CURRENT, ANY ONE INPUT ±10 mA

POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) Derate Linearly at 12 mW/°C to 200 mW
For T_A = -55 to 100°C (PACKAGE TYPE D) 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE D) Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100 mW

OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE D -55 to +125°C
PACKAGE TYPE E -40 to +85°C

STORAGE TEMPERATURE RANGE (T_{stg}) -65 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. +265°C

STATIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85°C, V_{DD} ± 10%, Except as noted

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS	
	V _O (V)	V _{IN} (V)	V _{DD} (V)	CDP1855			CDP1855C				
				Min.	Typ.*	Max.	Min.	Typ.*	Max.		
Quiescent Device Current	I _{DD}	—	0, 5	5	—	0.01	50	—	0.02	200	μA
Output Low Drive (Sink) Current	I _{OL}	0.4	0, 5	5	1.6	3.2	—	1.6	3.2	—	mA
		0.5	0, 10	10	2.6	5.2	—	—	—	—	
Output High Drive (Source) Current	I _{OH}	4.6	0, 5	5	1.15	2.3	—	1.15	2.3	—	mA
		9.5	0, 10	10	2.6	5.2	—	—	—	—	
Output Voltage Low-Level	V _{OL‡}	—	0, 5	5	—	0	0.1	—	0	0.1	V
		—	0, 10	10	—	0	0.1	—	—	—	
Output Voltage High Level	V _{OH‡}	—	0, 5	5	4.9	5	—	4.9	5	—	V
		—	0, 10	10	9.9	10	—	—	—	—	
Input Low Voltage	V _{IL}	0.5, 4.5	—	5	—	—	1.5	—	—	1.5	V
		0.5, 9.5	—	10	—	—	3	—	—	—	
Input High Voltage	V _{IH}	0.5, 4.5	—	5	3.5	—	—	3.5	—	—	V
		0.5, 9.5	—	10	7	—	—	—	—	—	
Input Leakage Current	I _{IN}	—	0, 5	5	—	—	±1	—	—	±1	μA
		—	0, 10	10	—	—	±1	—	—	—	
3-State Output Leakage Current	I _{OUT}	0, 5	0, 5	5	—	—	±1	—	—	±1	μA
		0, 10	0, 10	10	—	—	±10	—	—	—	
Operating Current	I _{DD1#}	—	0, 5	5	—	1.5	—	—	1.5	3	mA
		—	0, 10	10	—	6	12	—	—	—	
Input Capacitance	C _{IN}	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance	C _{OUT}	—	—	—	—	10	15	—	10	15	pF

*Typical values are for T_A = 25°C and nominal V_{DD}.

#Operating current is measured at 3.2 MHz with open outputs.

‡I_{OL} = I_{OH} = 1 μA.

RCA CMOS LSI Products

CDP1855, CDP1855C

OPERATING CONDITIONS at T_A = Full Package-Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	CONDITIONS VDD (V)	LIMITS				UNITS
		CDP1855		CDP1855C		
		Min.	Max.	Min.	Max.	
DC Operating Voltage Range	—	4	10.5	4	6.5	V
Input Voltage Range	—	VSS	VDD	VSS	VDD	
Maximum Input Clock Frequency	5	3.2	—	3.2	—	MHz
	10	6.4	—	—	—	
Minimum 8 x 8 Multiply (16 ÷ 8 Divide) Time	5	—	5.6	—	5.6	μs
	10	—	2.8	—	—	

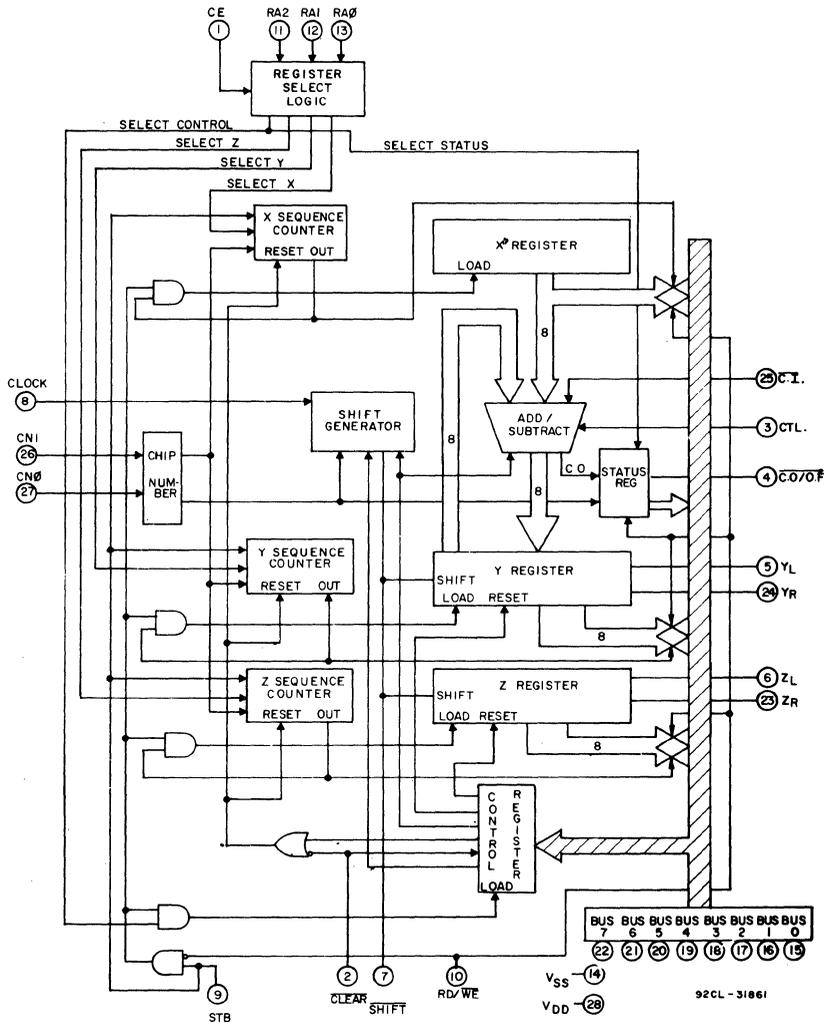


Fig. 2 - Block diagram of CDP1855 and CDP1855C.

FUNCTIONAL DESCRIPTION

The CDP1855 is a multiply-divide unit (MDU) designed to be compatible with CDP1800 series microprocessor systems. It can, in fact, be interfaced to most 8-bit microprocessors (see Fig. 5). The CDP1855 performs binary multiply or divide operations as directed by the microprocessor. It can do a 16N-bit by 8N-bit divide yielding an 8N-bit result plus and 8N-bit remainder. The multiply is an 8N-bit by 8N-bit operation with a 16N-bit result. The "N" represent the number of cascaded CDP1855's and can be 1, 2, 3 or 4. All operations require $8N + 1$ shift pulses (See "DELAY NEEDED WITH AND WITHOUT PRESCALER" Pg. 7).

The CDP1855 contains three registers, X, Y, and Z, which are loaded with the operands prior to an operation and contain the results at the completion. In addition, the control register must be loaded to initiate a multiply or divide. There is also a status register which contains an overflow flag as shown in the "CONTROL REGISTER BIT ASSIGNMENT TABLE". The register address lines (RA0-RA1) are used to select the appropriate register for loading or reading. The RD/ \overline{WE} and STB lines are used in conjunction with the RA lines to determine the exact MDU response (See "CONTROL TRUTH TABLE").

When multiple MDU's are cascaded, the loading of each register is done sequentially. For example, the first selection of register X for loading loads the most significant CDP1855, the second loads the next significant, and so on. Registers are also read out sequentially. This is accomplished by internal counters on each MDU which are decremented by STB during each register selection. When the counter matches the chip number (CN1, CN0 lines), the device is selected. These counters must be cleared with a clear on pin 2 or with bit 6 in the control word (See "CONTROL REGISTER BIT ASSIGNMENT TABLE") in order to start each sequence of accesses with the most significant device.

The CDP1855 has a built in clock prescaler which can be selected via bit 7 in the control register. The prescaler may be necessary in cascaded systems operating at high frequencies or in systems where a suitable clock frequency is not readily available. Without the prescaler select, the shift frequency is equal to the clock input frequency. With the prescaler selected, the rate depends on the number of MDU's as defined by bits 4 and 5 of the control word (See "CONTROL REGISTER BIT ASSIGNMENT TABLE").

1. For one MDU, the clock frequency is divided by 2.
2. For two MDU's the clock frequency is divided by 4.
3. For 3 or 4 MDU's, the clock frequency is divided by 8.

OPERATION

1. Initialization and Controls

The CDP1855 must be cleared by a low on pin 2 during power-on which prevents bus contention problems at the Y_L , Y_R and Z_L , Z_R terminals and also resets the sequence counters and the shift pulse generator.

Prior to loading any other registers the control register must be loaded to specify the number of MDU's being used (See "CONTROL REGISTER BIT ASSIGNMENT TABLE").

Once the number of devices has been specified and the sequence counters cleared with a clear pulse or bit 6 of the control word, the X, Y, and Z registers can be loaded as defined in the "CONTROL TRUTH TABLE". All bytes of the X register can be loaded, then all bytes of the Y, and then all bytes of the Z, or they can be loaded randomly. Successive loads to a given register will always proceed sequentially from the most significant byte to the least significant byte, as previously described. Resetting the sequence counters select the most significant MDU. In a four MDU system, loading all MDU's results in the sequence counter pointing to the first MDU again. In all other configurations (1, 2, or 3 MDU's), the sequence counter must be reset prior to each series of register reads or writes.

2. Divide Operation

For the divide operation, the divisor is loaded in the X register. The dividend is loaded in the Y and Z registers with the more significant half in the Y register and the less significant half in the Z register. These registers may be

loaded in any order, and after loading is completed, a control word is loaded to specify a divide operation and the number of MDU's and also to reset the sequence counters and Y or Z register and select the clock option if desired. Clearing the sequence counters with bit 6 will set the MDU's up for reading the results.

The X register will be unaltered by the operation. The quotient will be in the Z register while the remainder will be in the Y register. An overflow will be indicated by the C.O./O.F. of the most significant MDU and can also be determined by reading the status byte.

The overflow indicator will be set at the start of a divide operation if the resultant will exceed the size of the Z register (8N bits).

The Z register can simply be reset using bit 2 of the control word and another divide can be done in order to further divide the remainder.

3. Multiply Operation

For a multiply operation the two numbers to be multiplied are loaded in the X and Z registers. The result is in the Y and Z register with Y being the more significant half and Z the less significant half. The X register will be unchanged after the operation is completed.

The original contents of the Y register are added to the product of X and Z. Bit 3 of the control word will reset register Y to 0 if desired.

FUNCTIONAL DESCRIPTION OF CDP1855 TERMINALS

CE - CHIP ENABLE (Input):

A high on this pin enables the CDP1855 MDU to respond to the select lines. All cascaded MDU's must be enabled together. CE also controls the tristate $\overline{C.O./O.F.}$, output of the most significant MDU.

CLEAR (Input):

The CDP1855 MDU(s) must be cleared upon power-on with a low-on this pin. The clear signal resets the sequence counters, the shift pulse generator, and bits 0 and 1 of the control register.

CTL — CONTROL (Input):

This is an input pin. All CTL pins must be wired together and to the Y_L of the most significant CDP1855 MDU and to the Z_R of the least significant CDP1855 MDU. This signal is used to indicate whether the registers are to be operated on or only shifted.

C.O./O.F. — CARRY OUT/OVER FLOW (Output):

This is a tristate output pin. It is the CDP1855 $\overline{Carry Out}$ signal and is connected to CI (CARRY-IN) of the next more significant CDP1855 MDU, except for on the most significant MDU. On that MDU it is an overflow indicator and is enabled when chip enables is true. A low on this pin indicates that an overflow has occurred. The overflow signal is latched each time the control register is loaded, but is only meaningful after a divide command.

 Y_L, Y_R — Y-LEFT, Y-RIGHT:

These are tristate bi-directional pins for data transfer between the Y registers of cascaded CDP1855 MDU's. The Y_R pin is an output and Y_L is an input during a multiply and the reverse is true at all other times. The Y_L pin must be connected to the Y_R pin of the next more significant MDU. An exception is that the Y_L pin of the most significant CDP1855 MDU must be connected to the Z_R pin of the least significant MDU and to the CTL pins of all MDU's. Also the Y_R pin of the least significant MDU is tied to the Z_L pin of the most significant MDU.

 Z_L, Z_R — Z-LEFT, Z-RIGHT:

These are tristate bi-directional pins for data transfers between the "Z" registers of cascaded MDU's. The Z_R pin is an output and Z_L is an input during a multiply and the reverse is true at all other times. The Z_L pin must be tied to the Y_R pin of the next more significant MDU. An exception is that the Z_L pin of the most significant MDU must be connected to the Y_R pin of the least significant MDU. Also, the Z_R pin of the least significant MDU is tied to the Y_L of the most significant MDU.

SHIFT — SHIFT CLOCK:

This is a tristate bi-directional pin. It is an output on the most significant MDU. And an input on all other MDU's. It provides the MDU system timing pulses. All SHIFT pins must be connected together for cascaded operation. A maximum of the $8N + 1$ shifts are required for an operation where "N" equals the number of MDU devices that are cascaded.

CLK — CLOCK (Input):

This pin should be grounded on all but the most significant MDU. There is an optional reduction of clock frequency available on this pin if so desired, controlled by bit 7 of the control byte.

STB — STROBE (Input):

When RD/WE is low data is latched from bus lines on the falling edge of this signal. It may be asynchronous to the clock. Strobe also increments the selected register's sequence counter during reads and writes. TPB would be used in CDP1800 systems.

RD/WE — READ/WRITE ENABLE (Input):

This signal defines whether the selected register is to be read from or written to. In 1800 systems use \overline{MRD} if MDU's are addressed as I/O devices, \overline{MWR} is used if MDU's are addressed as memory devices.

RA2, RA1, RA0 — REGISTER ADDRESS (Input):

These input signals define which register is to be read from or written to. It can be seen in the "CONTROL TRUTH TABLE" that RA2 can be used as a chip enable. It is identical to the CE pin, except only CE controls the tristate $\overline{C.O./O.F.}$ on the most significant MDU. In 1800 systems use N lines if MDU's are used as I/O devices, use address lines or function of address lines if MDU's are used as memory devices.

BUS 0 — BUS 7 - BUS LINES:

Tristate bi-directional bus for direct interface with CDP1800 series and other 8-bit microprocessors.

 Z_R — Z-RIGHT:

See Pin 6.

 Y_R — Y-RIGHT:

See Pin 5.

CI — CARRY IN (Input):

This is an input for the carry from the next less significant MDU. On the least significant MDU it must be high (V_{DD}) on all others it must be connected to the \overline{CO} pin of the next less significant MDU.

CN1, CN0 — CHIP NUMBER (Input):

These two input pins are wired high or low to indicate the MDU position in the cascaded chain. Both are high for the most significant MDU regardless of how many CDP1855 MDU's are used. Then CN1 = high and CN0 = low for the next MDU and so forth.

 V_{SS} — GROUND:

Power supply line.

 V_{DD} — V+:

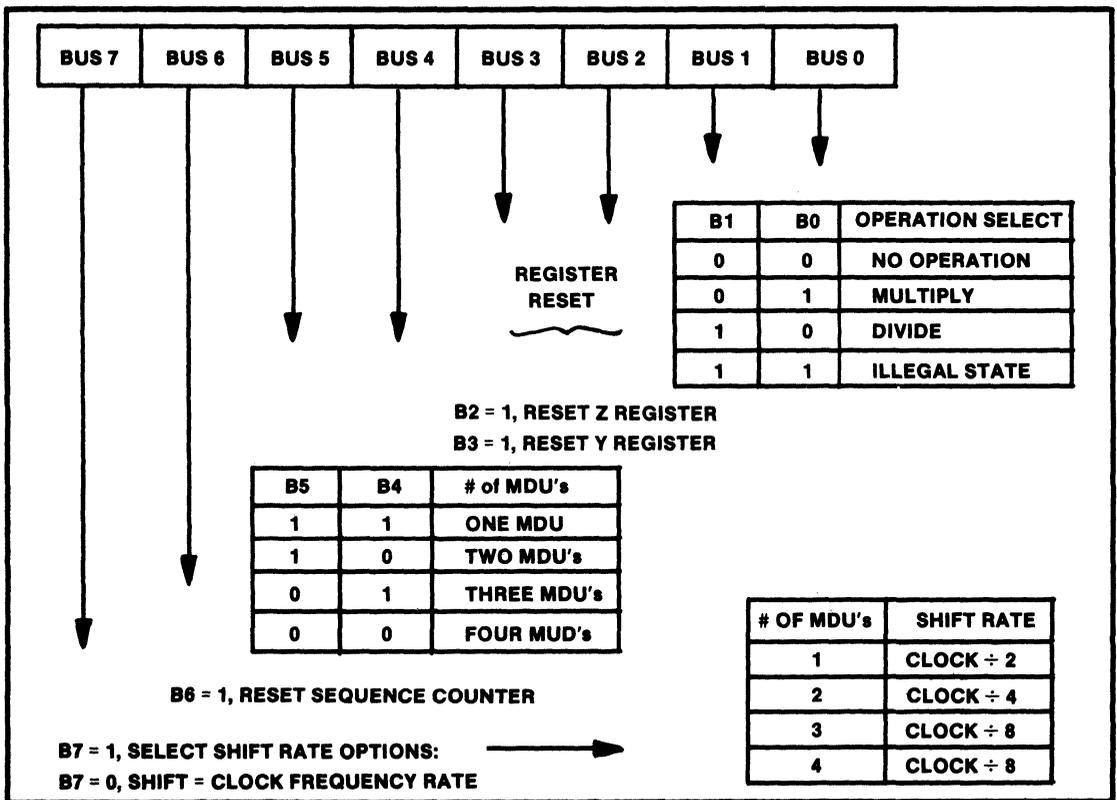
Power supply line.

CONTROL TRUTH TABLE

INPUTS*						RESPONSE
CE	RA2 (N2)	RA1 (N1)	RA0 (N0)	RD/ \overline{WE} (MRD)	STB (TPB)	
0	X	X	X	X	X	NO ACTION (BUS FLOATS)
X	0	X	X	X	X	NO ACTION (BUS FLOATS)
1	1	0	0	1	X	X TO BUS } INCREMENT SEQUENCE
1	1	0	1	1	X	Z TO BUS } COUNTER WHEN
1	1	1	0	1	X	Y TO BUS } STB AND RD = 1
1	1	1	1	1	X	STATUS TO BUS
1	1	0	0	0	1	LOAD X FROM BUS } INCREMENT
1	1	0	1	0	1	LOAD Z FROM BUS } SEQUENCE
1	1	1	0	0	1	LOAD Y FROM BUS } COUNTER
1	1	1	1	0	1	LOAD CONTROL REGISTER
1	1	X	X	0	0	NO ACTION (BUS FLOATS)

* () = 1800 system signals. 1 = High Level, 0 = Low Level, X = High or Low Level.

CONTROL REGISTER BIT ASSIGNMENT TABLE



STATUS REGISTER

Status Byte	
Bit	7 6 5 4 3 2 1 0
Output	0 0 0 0 0 0 0 O.F.
	O.F. = 1 if overflow (only valid after a divide has been done)

NOTE: Bits 1 — 7 are read as 0 always

DELAY NEEDED WITH AND WITHOUT PRESCALER

8N+1 Shifts/Operation at 1 Clock Cycle/Shift
N = Number of MDU's S = Shift Rate

Number of MDU's	No Prescaler		With Prescaler		
	Shifts = 8N+1 Needed	Machine Cycles Needed*	Shifts = S (8N+1) Needed	Machine Cycles Needed*	Shift Rate
1	9	2 (1 NOP)	18	3 (1 NOP)	2
2	17	2 (1 NOP)	68	9 (3 NOPs)	4
3	25	3 (1 NOP)	200	25 (9 NOPs)	8
4	33	4 (2 NOPs)	264	33 (11 NOPs)	8

*NOP instruction is shown for machine cycles needed (3/NOP). Other instructions may be used.

CDP1855 INTERFACING SCHEMES

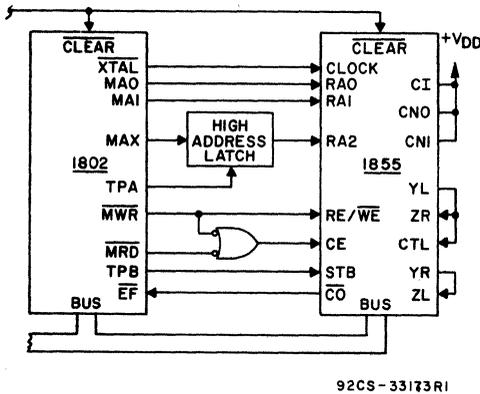


Fig. 3 - Required connection for memory mapped addressing of the MDU.

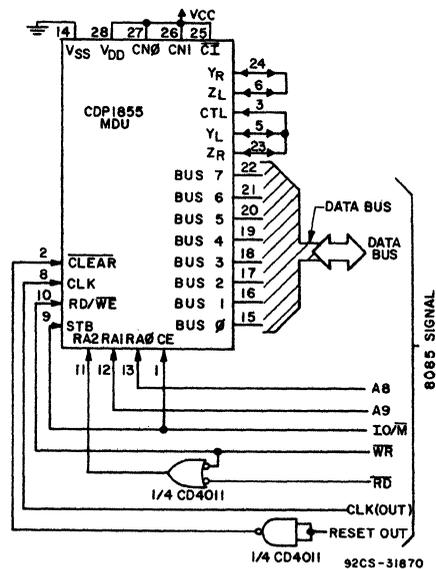


Fig. 4 - Interfacing the CDP1855 to an 8085 microprocessor as an I/O device.

PROGRAMMING EXAMPLE

For a 24-bit x 24-bit multiply using the system shown in Figure 5, the following is an assembly listing of a program to multiply 201F7C₁₆ by 723C09₁₆:

MEMORY LOCATION	OP CODE	LINE NO.	ASSEMBLY LANGUAGE
0000	F830;	0001	LDI 030H
0002	A2;	0002	PLD R2 ..LOAD 30 INTO R2.0
0003	F800;	0003	LDI 00H
0005	B2;	0004	PHI R2 ..LOAD 00 INTO R2.1 (R2=0030)
0006	6758;	0005	OUT 7; DC 058H ..LOAD CONTROL REGISTERS
0008	;	0006	..SPECIFYING THREE MDU'S,
0008	;	0007	..RESET THE Y REGISTER AND
0008	;	0008	..SEQUENCE COUNTER
0008	6420;	0009	OUT 4; DC 020H ..LOAD MSB OF X REGISTER
000A	;	0010	..WITH 20
000A	641F;	0011	OUT 4; DC 01FH ..LOAD NEXT MSB OF X REG
000C	;	0012	..WITH 1F
000C	647C;	0013	OUT 4; DC 07CH ..LOAD LSB OF X REGISTER
000E	;	0014	..WITH 7C
000E	6572;	0015	OUT 5; DC 072H ..LOAD MSB OF Z REGISTER
0010	;	0016	..WITH 72
0010	653C;	0017	OUT 5; DC 03CH ..LOAD NEXT MSB OF Z REG
0012	;	0018	..WITH 3C
0012	6509;	0019	OUT 5; DC 09H ..LOAD LSB OF Z REGISTER
0014	;	0020	..WITH 09
0014	6759;	0021	OUT 7; DC 059H ..LOAD CONTROL REGISTERS
0016	;	0022	..RESETTING Y REGISTERS
0016	;	0023	..AND SEQUENCE COUNTERS
0016	;	0024	..AND STARTING MULTIPLY
0016	;	0025	..OPERATION
0016	E2;	0026	SEX R2
0017	6E60;	0027	INP 6; IRX ..MSB OF RESULTS IS STORED
0019	;	0028	..AT LOCATION 0030
0019	6E60;	0029	INP 6; IRX
001B	6E60;	0030	INP 6; IRX
001D	6D60;	0031	INP 5; IRX
001F	6D60;	0032	INP 5; IRX
0021	6D;	0033	INP 5 ..COMPLETE LOADING RESULT
0022	;	0034	..INTO MEMORY LOCATIONS
0022	;	0035	..0030 TO 0035
0022	;	0036	..RESULTS=0E558DBA2B5C
0022	3022;	0037	STDP BR STOP
0024	;	0038	END
0000	;		

The result of 201F7C₁₆ x 723C09₁₆ is 0E558DBA2B5C = 15760612797276₁₀. It will be stored in memory as follows:

LOC	BYTE
0030	0E
31	55
32	8D
33	BA
34	2B
35	5C

BEFORE MULTIPLY

	MDU1	MDU2	MDU3
Register X	20	1F	7C
Register Y	00	00	00
Register Z	72	3C	09

AFTER MULTIPLY

	MDU1	MDU2	MDU3
Register X	20	1F	7C
Register Y	0E	55	8D
Register Z	BA	2B	5C

1800-Series Peripherals
CDP1855, CDP1855C

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} \pm 5\%$, $t_r, t_f = 20\text{ ns}$, $V_{IH} = 0.7 V_{DD}$, $V_{IL} = 0.3 V_{DD}$, $C_L = 100\text{ pF}$ (See Fig. 7)

CHARACTERISTIC*	VDD (V)	LIMITS						UNITS
		CDP1855			CDP1855C			
		Min.	Typ.*	Max.	Min.	Typ.*	Max.	

Operation Timing

Maximum Clock Frequency+		5	3.2	4	—	3.2	4	—	MHz
		10	6.4	8	—	—	—	—	
Maximum Shift Frequency (1 Device) Δ		5	1.6	2	—	1.6	2	—	MHz
		10	3.2	4	—	—	—	—	
Minimum Clock Width	tCLK0	5	—	100	150	—	100	150	ns
	tCLK1	10	—	50	75	—	—	—	
Minimum Clock Period	tCLK	5	—	250	312	—	250	312	ns
		10	—	125	156	—	—	—	
Clock to Shift Prop. Delay	tCSH	5	—	200	300	—	200	300	ns
		10	—	100	150	—	—	—	
Minimum C.I. to Shift Setup	tSU	5	—	50	67	—	50	67	ns
		10	—	25	33	—	—	—	
C.O. from Shift Prop. Delay	tPLH	5	—	450	600	—	450	600	ns
	tPHL	10	—	225	300	—	—	—	
Minimum C.I. from Shift Hold	tH	5	—	50	75	—	50	75	ns
		10	—	25	40	—	—	—	
Minimum Register Input Setup	tSU	5	—	-20	10	—	-20	10	ns
		10	—	-10	10	—	—	—	
Register after Shift Delay	tPLH	5	—	400	600	—	400	600	ns
	tPHL	10	—	200	300	—	—	—	
Minimum Register after Shift Hold	tH	5	—	50	100	—	50	100	ns
		10	—	25	50	—	—	—	
C.O. from C.I. Prop. Delay	tPLH	5	—	100	150	—	100	150	ns
	tPHL	10	—	50	75	—	—	—	
Register from C.I. Prop. Delay	tPLH	5	—	80	120	—	80	120	ns
	tPHL	10	—	40	60	—	—	—	

*Maximum limits of minimum characteristics are the values above which all devices function.

*Typical values are for $T_A = 25^\circ\text{C}$ and nominal voltages.

+Clock frequency and pulse width are given for systems using the internal clock option of the CDP1855. Clock frequency equals shift frequency for systems not using the internal clock option.

Δ Shift period for cascading of devices is increased by an amount equal to the $\overline{\text{C.I.}}$ to $\overline{\text{C.O.}}$ Prop. Delay for each device added.

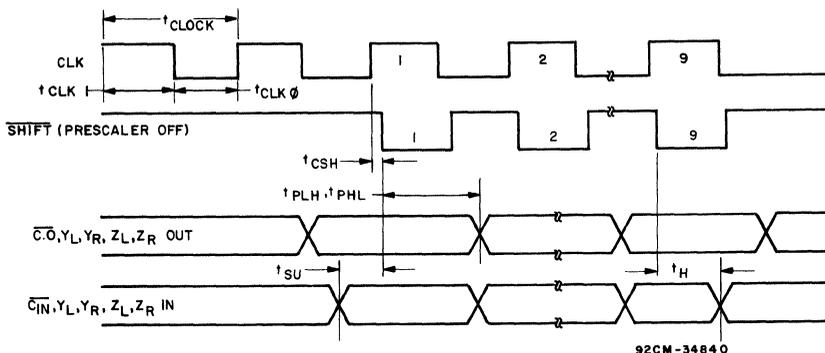


Fig. 7 - Operation timing diagram.

92CM-34840

RCA CMOS LSI Products
CDP1855, CDP1855C

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} \pm 5\%$, $t_r, t_f = 20\text{ ns}$, $V_{IH} = 0.7 V_{DD}$, $V_{IL} = 0.3 V_{DD}$, $C_L = 100\text{ pF}$ (See Fig. 8)

CHARACTERISTIC*	V _{DD} (V)	LIMITS						UNITS
		CDP1855			CDP1855C			
		Min.	Typ.*	Max.	Min.	Typ.*	Max.	

Write Cycle

Characteristic	Symbol	5	—	50	75	—	50	75	ns
Minimum Clear Pulse Width	t _{CLR}	10	—	25	40	—	—	—	
Minimum Write Pulse Width	t _{WW}	5	—	150	225	—	150	225	
		10	—	75	115	—	—	—	
Minimum Data-In Setup	t _{DSU}	5	—	-75	0	—	-75	0	
		10	—	-40	0	—	—	—	
Minimum Data-In-Hold	t _{DH}	5	—	50	75	—	50	75	
		10	—	25	40	—	—	—	
Minimum Address to Write Setup	t _{ASU}	5	—	50	75	—	50	75	
		10	—	25	40	—	—	—	
Minimum Address after Write Hold	t _{AH}	5	—	50	75	—	50	75	
		10	—	25	40	—	—	—	

•Maximum limits of minimum characteristics are the values above which all devices function.

*Typical values are for $T_A = 25^\circ\text{C}$ and nominal voltages.

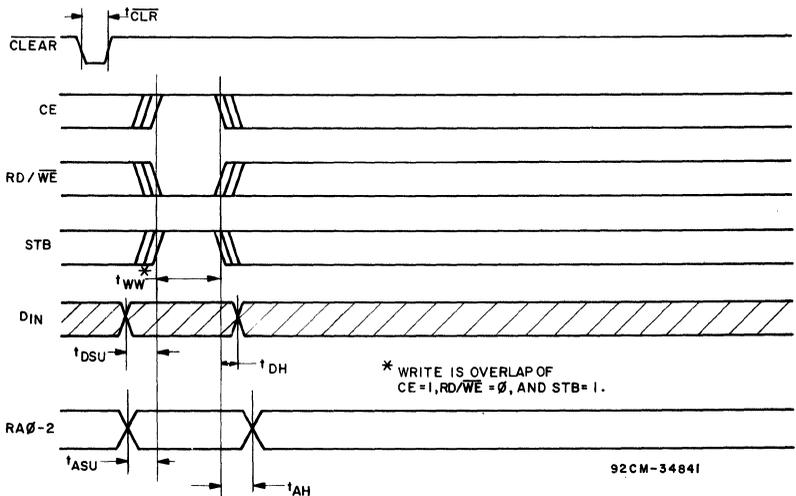


Fig. 8 - Write timing diagram.

1800-Series Peripherals
CDP1855, CDP1855C

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} \pm 5\%$, $t_r, t_f = 20$ ns, $V_{IH} = 0.7 V_{DD}$, $V_{IL} = 0.3 V_{DD}$, $C_L = 100$ pF (See Fig. 9)

CHARACTERISTIC*	V _{DD} (V)	LIMITS						UNITS
		CDP1855			CDP1855C			
		Min.	Typ.*	Max.	Min.	Typ.*	Max.	

Read Cycle

CHARACTERISTIC	Symbol	5	10	200	300	200	300	UNITS
CE to Data Out Active	t _{CDO}	—	—	200	300	—	200	ns
		—	100	150	—	—	—	
CE to Data Access	t _{CA}	—	—	300	450	—	300	ns
		—	150	225	—	—	—	
Address to Data Access	t _{AA}	—	—	300	450	—	300	ns
		—	150	225	—	—	—	
Data Out Hold after CE	t _{DOH}	50	25	150	225	50	150	ns
		75	115	—	—	—	—	
Data Out Hold after Read	t _{DOH}	50	25	150	225	50	150	ns
		75	115	—	—	—	—	
Read to Data Out Active	t _{RDO}	—	—	200	300	—	200	ns
		—	100	150	—	—	—	
Read to Data Access	t _{RA}	—	—	200	300	—	200	ns
		—	100	150	—	—	—	
Strobe to Data Access	t _{SA}	50	25	200	300	50	200	ns
		100	150	—	—	—	—	
Minimum Strobe Width	t _{SW}	—	—	150	225	—	150	ns
		—	75	115	—	—	—	

•Maximum limits of minimum characteristics are the values above which all devices function.

*Typical values are for $T_A = 25^\circ\text{C}$ and nominal voltages.

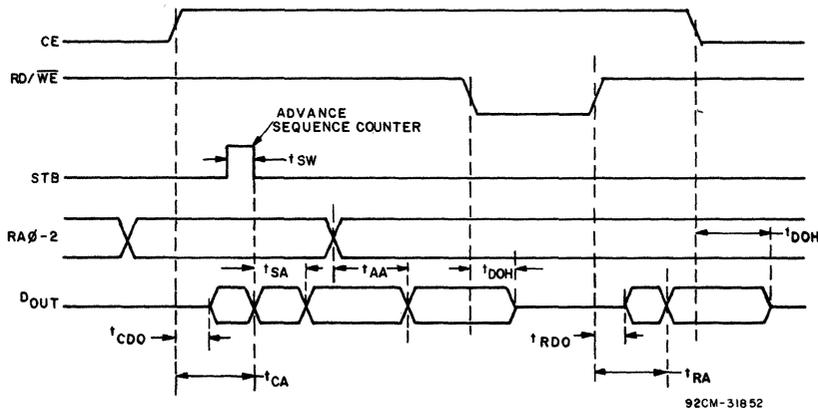
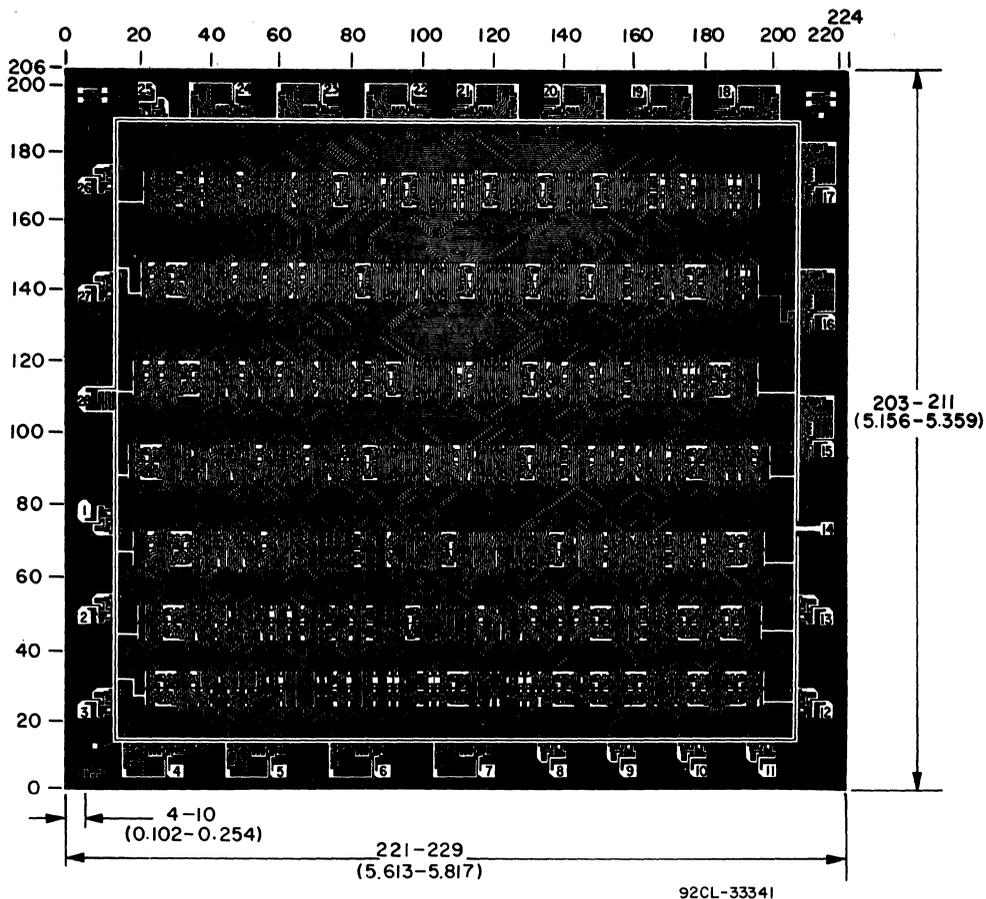


Fig. 9 - Read timing diagram.

RCA CMOS LSI Products
CDP1855, CDP1855C



Dimensions and pad layout for CDP1855CH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mil (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

OPERATING AND HANDLING CONSIDERATIONS

1. Handling

All inputs and outputs of RCA CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in ICAN-6525, "Guide to Better Handling and Operation of CMOS Integrated Circuits".

2. Operating

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause $V_{DD} - V_{SS}$ to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{CC} nor less than V_{SS} . Input currents must not exceed 10 mA even when the power supply is off.

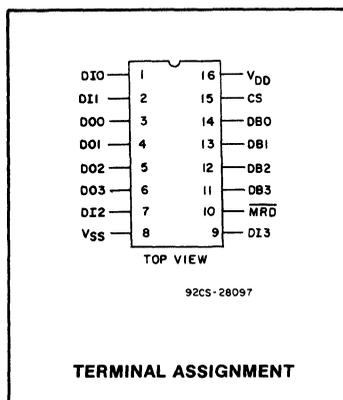
Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{CC} or V_{SS} , whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} , V_{CC} , or V_{SS} may damage CMOS devices by exceeding the maximum device dissipation.

4-Bit Bus Buffers/Separators



Features:

- Provides easy connection of memory and I/O devices to CDP1800-series microprocessor data bus.
- Non-inverting fully buffered data transfer

The RCA-CDP1856, CDP1856C, CDP1857, and CDP1857C are 4-bit CMOS non-inverting bus separators designed for use in CDP1800-series microprocessor systems. They can be controlled directly by a 1800-series microprocessor without the use of additional components.

The CDP 1856 is designed for use as a bus buffer or separator between the 1800-series microprocessor data bus and memories. The CDP1857 is designed for use as a bus buffer or separator between the 1800-series microprocessor data bus and I/O devices. Both types provide a chip-select (CS) input signal which, when high (1), enables the bus-separator three-state output drivers. The direction of data flow, when enabled, is controlled by the MRD input signal.

In the CDP1856, when the $\overline{\text{MRD}}$ signal = 0 (low), it enables the three-state bus drivers (DB0 — DB3) and outputs data from the DATA-IN terminals to the data bus. When $\overline{\text{MRD}}$ = 1 (high), it disables the three-state bus drivers and enables the three-state data output drivers (DO0-DO3), thus transferring data from the data bus to the DATA-OUT terminals.

In the CDP1857, when $\overline{\text{MRD}}$ = 1, it enables the three state bus drivers (DB0-DB3) and transfers data from the DATA-IN lines onto the data bus. When $\overline{\text{MRD}}$ = 0, it disables the

three-state bus drivers (DB0-DB3) and enables the three-state data output drivers (DO0-DO3), thus transferring data from the data bus to the DATA-OUT terminals.

The CDP1856 or CDP1857 can be used as a bi-directional bus buffer by connecting the corresponding DI and DO terminals (Fig. 2). The $\overline{\text{MRD}}$ output signal from the 1800 series microprocessor has the correct polarity to control the CDP1856 when this device is used as a memory data bus buffer/ separator, or the CDP1857 when it is used as I/O bus buffer/separator. Therefore, the 1800 series microprocessor $\overline{\text{MRD}}$ signal can be connected directly to the $\overline{\text{MRD}}$ input of either device. See Function Tables I and II for use of the CDP1856 as a memory data bus buffer/separator and CDP1857 as an I/O bus buffer/separator.

The CDP1856 and CDP1857 are functionally identical to the CDP1856C and CDP1857C, respectively. The CDP1856 and CDP1857 have a recommended operating-voltage range of 4 to 10.5 volts, and the CDP1856C and CDP1857C have a recommended operating-voltage range of 4 to 6.5 volts. The CDP1856, CDP1856C, CDP1857 and CDP1857C are supplied in 16-lead hermetic, dual-in-line ceramic packages (D suffix), and in 16-lead plastic packages (E suffix).

CDP1857 FUNCTION TABLE I
For I/O Bus Separator Operation

CS	$\overline{\text{MRD}}$	DATA BUS OUT DB0 — DB3	DATA OUT DO0 — DO3
0	X	HIGH IMPEDANCE	HIGH IMPEDANCE
1	0	HIGH IMPEDANCE	DATA BUS HIGH IMPEDANCE
1	1	DATA IN	HIGH IMPEDANCE

CDP1856 FUNCTION TABLE II
For Memory Data Bus Separator Operation

CS	$\overline{\text{MRD}}$	DATA BUS OUT DB0 — DB3	DATA OUT DO0 — DO3
0	X	HIGH IMPEDANCE	HIGH IMPEDANCE
1	0	DATA IN HIGH IMPEDANCE	HIGH IMPEDANCE
1	1	HIGH IMPEDANCE	DATA BUS

CDP1856, CDP1856C, CDP1857, CDP1857C

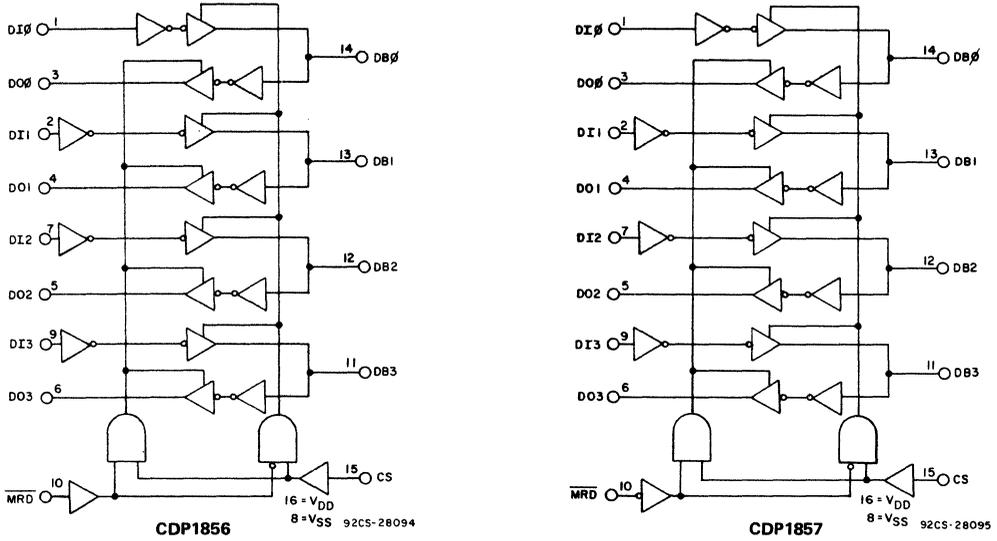


Fig. 1 — Functional diagrams for CDP1856 and CDP1857.

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(All voltage values referenced to V_{SS} terminal)

CDP1856, CDP1857	-0.5 to +11 V
CDP1856C, CDP1857C	-0.5 to +7 V

INPUT VOLTAGE RANGE, ALL INPUTS

DC INPUT CURRENT, ANY ONE INPUT

POWER DISSIPATION PER PACKAGE (P_D):

For $T_A = -40$ to $+60^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +60$ to $+85^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 12 mW/ $^\circ\text{C}$ to 200 mW
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE D)	500 mW
For $T_A +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE D)	Derate Linearly at 12 mW/ $^\circ\text{C}$ to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE}$ (All Package Types)

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPE D	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E	-40 to $+85^\circ\text{C}$

STORAGE TEMPERATURE RANGE (T_{stg})

LEAD TEMPERATURE (DURING SOLDERING):

At distance $1/16 \pm 1/32$ inch (1.59 ± 0.79 mm) from case for 10 s max.

CDP1856, CDP1856C, CDP1857, CDP1857C

OPERATING CONDITIONS at T_A = Full Package-Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1856 CDP1857		CDP1856C CDP1857C		
	Min.	Max.	Min.	Max.	
Supply-Voltage Range	4	10.5	4	6.5	V
Recommended Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85°C, Except as noted

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	CDP1856 CDP1857			CDP1856C CDP1857C			
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device Current, I_{DD}	—	0,5	5	—	1	10	—	5	50	μA
	—	0,10	10	—	10	100	—	—	—	
Output Low Drive (Sink) Current, I_{OL}	0,4	0,5	5	1,6	3,2	—	1,6	3,2	—	mA
	0,5	0,10	10	2,6	5,2	—	—	—	—	
Output High Drive (Source Current), I_{OH}	4,6	0,5	5	-1,15	-2,3	—	-1,15	-2,3	—	mA
	9,5	0,10	10	-2,6	-5,2	—	—	—	—	
Output Voltage Low-Level [•] , V_{OL}	—	0,5	5	—	0	0,1	—	0	0,1	V
	—	0,10	10	—	0	0,1	—	—	—	
Output Voltage High-Level [•] , V_{OH}	—	0,5	5	4,9	5	—	4,9	5	—	V
	—	0,10	10	9,9	10	—	—	—	—	
Input Low Voltage, V_{IL}	0,5,4,5	—	5	—	—	1,5	—	—	1,5	V
	0,5,9,5	—	10	—	—	3	—	—	—	
Input High Voltage, V_{IH}	0,5,9,5	—	5	3,5	—	—	3,5	—	—	V
	0,5,9,5	—	10	7	—	—	—	—	—	
Input Leakage Current, I_{IN}	Any Input	0,5	5	—	—	± 1	—	—	± 1	μA
		0,10	10	—	—	± 1	—	—	—	
Operating Current, I_{DD1} ■	0,5	0,5	5	—	50	100	—	50	100	μA
	0,10	0,10	10	—	150	300	—	—	—	
Input Capacitance, C_{IN}	—	—	—	—	5	7,5	—	5	7,5	pF
Output Capacitance, C_{OUT}	—	—	—	—	10	15	—	10	15	pF

*Typical values are for T_A = 25°C and nominal voltage.

■ Operating current measured in a CDP1802 system at 3.2 MHz with outputs floating.

• $I_{OL} = I_{OH} = 1 \mu A$.

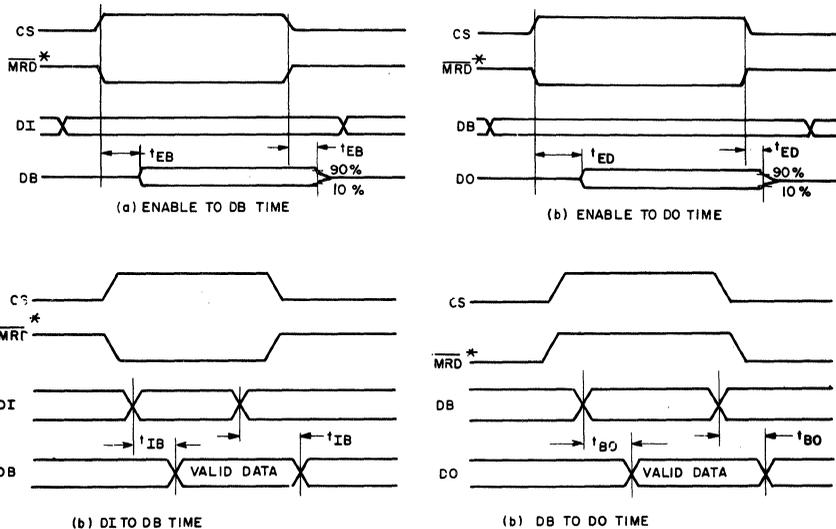
CDP1856, CDP1856C, CDP1857, CDP1857C

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = \pm 5\%$,

$V_{IH} = 0.7 V_{DD}$, $V_{IL} = 0.3 V_{DD}$, $t_r, t_f = 20\text{ ns}$, $C_L = 100\text{ pF}$

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		CDP1856 CDP1857		CDP1856C CDP1857C		
		Typ.*	Max.	Typ.*	Max.	
Propagation Delay Time: MRD or CS to DO,	5	150	225	150	225	ns
	10	75	125	—	—	
MRD or CS to DB,	5	150	225	150	225	ns
	10	75	125	—	—	
DI to DB,	5	100	150	100	150	ns
	10	50	75	—	—	
DB to DO	5	100	150	100	150	ns
	10	50	75	—	—	

*Typical values are for $T_A = 25^\circ\text{C}$ and nominal voltages.



* POLARITIES ARE REVERSED FOR CDP1857

92CM-28093R2

Fig. 2 — Timing diagrams for CDP1856 or CDP1857 (see footnote).

CDP1856, CDP1856C, CDP1857, CDP1857C

TYPICAL APPLICATIONS

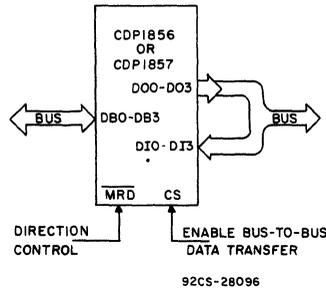


Fig. 3 — CDP1856, CDP1857 bidirectional bus buffer operation.

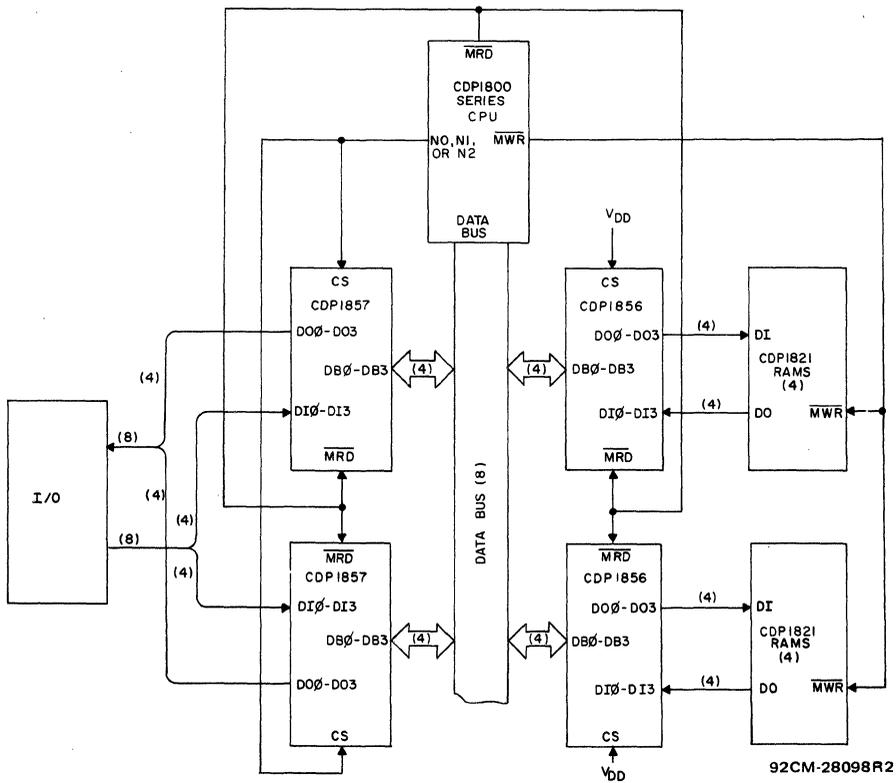
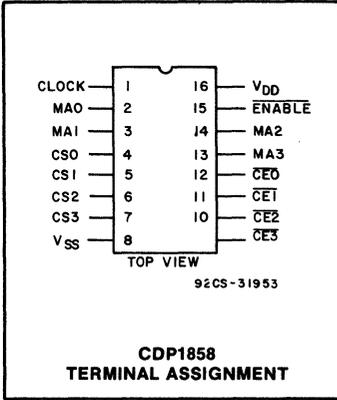


Fig. 4 — CDP1856 and CDP1857 bus separator operation.

4-Bit Latch and Decoder Memory Interfaces



Features:

- Provides easy connection of memory devices to CDP1802 microprocessor
- Non-inverting fully buffered data transfer

RCA-CDP1858, CDP1858C, CDP1859, and CDP1859C are CMOS 4-bit latch decode circuits designed for use in CDP1800 series microprocessor systems. These devices have been specifically designed for use as memory-system decoders and interface directly with the 1800-series microprocessor multiplexed address bus at maximum clock frequency.

The CDP1858 and CDP1859 are functionally identical to the CDP1858C and CDP1859C, respectively. The CDP1858 and CDP1859 have a recommended operating-voltage range of 4 to 10.5 volts, and the CDP1858C and CDP1859C have a recommended operating-voltage range of 4 to 6.5 volts.

The CDP1858 interfaces the 1800-series microprocessor address bus and up to 32 CDP1822 256 x 4 RAM's to provide a 4K byte RAM system. No additional components are required. The CDP1858 generates the chip selects required by the CDP1822 RAM. The chip select outputs are a function of the address bits connected to inputs MA0 through MA3.

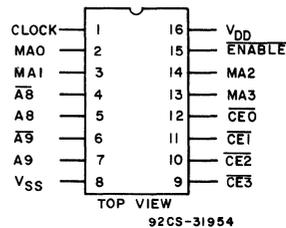
The MA0-MA3 address bits are latched at the trailing edge of TPA (generated by the CDP1802). When $\overline{ENABLE}=1$ (V_{DD}), the CS outputs=0 (V_{SS}), and the CE outputs=1. When $\overline{ENABLE}=0$, the outputs are enabled and correspond to the binary decode of the inputs. The \overline{ENABLE} input can be used for memory system expansion.

The CDP1858 is also compatible with non-multiplexed address bus microprocessors. By connecting the CLOCK input to 1 (V_{DD}), the latches are in the data following mode and the decoded outputs can be used in general-purpose memory-system applications.

The CDP1859 interfaces the 1800-series microprocessor address bus and up to 32 CDP1821 1024 x 1 RAM's to

provide a 4K byte RAM system. The CDP1859 generates the chip selects required by the CDP1821 RAM. The chip select outputs are a function of the address bits connected to inputs MA2 and MA3. The address bits connected to inputs MA0 and MA1 are latched by the trailing edge of TPA (generated by the 1800-series microprocessor) to provide the two additional address lines required by the CDP1821 when used in a CDP1800 series microprocessor-based system. When $\overline{ENABLE}=1$, the CE outputs are 1's; when $\overline{ENABLE}=0$, and CE outputs are enabled and correspond to the binary decode of the MA2 and MA3 inputs. \overline{ENABLE} does not affect the latching or state of outputs A8, $\overline{A8}$, A9, or $\overline{A9}$.

The CDP1858, CDP1858C, CDP1859, and CDP1859C are supplied in 16-lead, hermetic, dual-in-line side-brazed ceramic packages (D suffix) and in 16-lead dual-in-line plastic packages (E suffix).



CDP1858, CDP1858C, CDP1859, CDP1859C

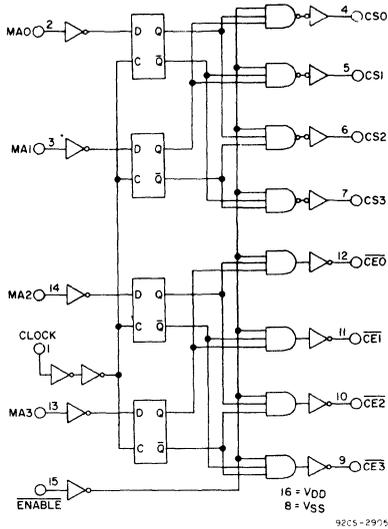


Fig. 1 — CDP1858 — Functional diagram.

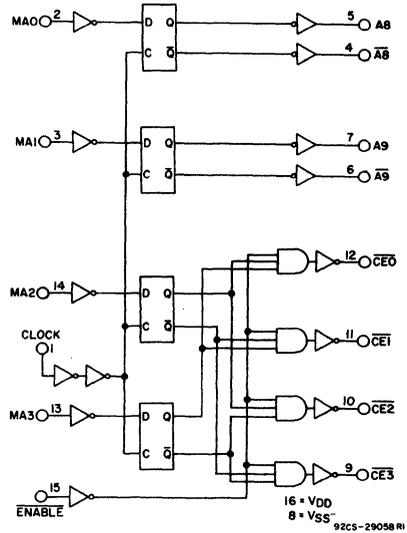


Fig. 2 — CDP1859 — Functional diagram.

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltage referenced to V_{SS} Terminal)

CDP1858, CDP1859	-0.5 to +11 V
CDP1858C, CDP1859C	-0.5 to +7 V

INPUT VOLTAGE RANGE, ALL INPUTS

DC INPUT CURRENT, ANY ONE INPUT

POWER DISSIPATION PER PACKAGE (P_D):

For $T_A = -40$ to $+60^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +60$ to $+85^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 12 mW/ $^\circ\text{C}$ to 200 mW
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE D)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE D)	Derate Linearly at 12 mW/ $^\circ\text{C}$ to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, H	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E	-40 to $+85^\circ\text{C}$

STORAGE TEMPERATURE RANGE (T_{stg})

LEAD TEMPERATURE (DURING SOLDERING):

At distance $1/16 \pm 1/32$ inch (1.59 ± 0.79 mm) from case for 10 s max.

RCA CMOS LSI Products

CDP1858, CDP1858C, CDP1859, CDP1859C

OPERATING CONDITIONS at T_A = Full Package-Temperature Range.

For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1858 CDP1859		CDP1858C CDP1859C		
	Min.	Max.	Min.	Max.	
Supply-Voltage Range	4	10.5	4	6.5	V
Recommended Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, Except as noted

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
	V_O	V_{IN}	V_{DD}	CDP1858 CDP1859			CDP1858C CDP1859C			
	(V)	(V)	(V)	Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device Current, I_{DD}	—	0,5	5	—	0.1	10	—	5	50	μA
	—	0,10	10	—	1	100	—	—	—	
Output Low Drive (Sink) Current, I_{OL}	0.4	0,5	5	1.6	3.2	—	1.6	3.2	—	mA
	0.5	0,10	10	2.6	5.2	—	—	—	—	
Output High Drive (Source Current), I_{OH}	4.6	0,5	5	-1.15	-2.3	—	-1.15	-2.3	—	mA
	9.5	0,10	10	-2.6	-5.2	—	—	—	—	
Output Voltage• Low-Level, V_{OL}	—	0,5	5	—	0	0.1	—	0	0.1	V
	—	0,10	10	—	0	0.1	—	—	—	
Output Voltage• High-Level, V_{OH}	—	0,5	5	4.9	5	—	4.9	5	—	V
	—	0,10	10	9.9	10	—	—	—	—	
Input Low Voltage, V_{IL}	0.5,4.5	—	5	—	—	1.5	—	—	1.5	V
	0.5,9.5	—	10	—	—	3	—	—	—	
Input High Voltage, V_{IH}	0.5,4.5	—	5	3.5	—	—	3.5	—	—	V
	0.5,9.5	—	10	7	—	—	—	—	—	
Input Leakage Current, I_{IN}	Any Input	0,5	5	—	10^{-4}	± 1	—	10^{-4}	± 1	μA
		0,10	10	—	10^{-4}	± 2	—	—	—	
Operating Current, I_{DD} ■	—	0,5	5	—	50	100	—	50	100	μA
	—	0,10	10	—	150	300	—	—	—	
Input Capacitance, C_{IN}	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance, C_{OUT}	—	—	—	—	10	15	—	—	—	pF

*Typical values are for $T_A = 25^\circ\text{C}$ and nominal voltage.

• $I_{OL} = I_{OH} = 1 \mu\text{A}$.

■ Measured in a CDP1802 or CDP1804 system at 3.2 MHz with open outputs.

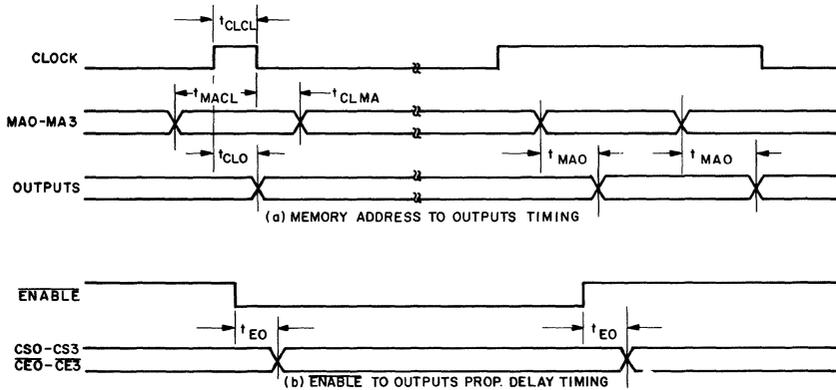
CDP1858, CDP1858C, CDP1859, CDP1859C

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} \pm 5\%$, $t_r, t_f = 20$ ns,
 $V_{IH} = 0.7 V_{DD}$, $V_{IL} = 0.3 V_{DD}$, $C_L = 100$ pF, See Fig. 3.

CHARACTERISTIC	V_{DD} (V)	LIMITS						UNITS
		CDP1858			CDP1858C			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Minimum Setup Time, Memory Address to Clock, t_{MACL}	5	—	25	40	—	25	40	ns
Minimum Hold Time, Memory Address After Clock, t_{CLMA}	10	—	0	25	—	0	25	
Minimum Clock Pulse Width, t_{CLCL}	5	—	50	75	—	50	75	ns
Propagation Delay Times:	10	—	25	40	—	—	—	
Clock to Outputs, t_{CLO}	5	—	150	225	—	150	225	ns
Memory Address to Outputs, t_{MAO}	10	—	75	125	—	—	—	
ENABLE to Outputs, t_{EO}	5	—	125	200	—	125	200	
Outputs, t_{EO}	10	—	65	100	—	—	—	

Typical values are for $T_A = 25^\circ\text{C}$ and nominal voltages.

Maximum limits of minimum characteristics are the values above which all devices function.



92CM-31956

Fig. 3 — CDP1858 timing diagram.

RCA CMOS LSI Products

CDP1858, CDP1858C, CDP1859, CDP1859C

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} \pm 5\%$, $t_r, t_f = 20$ ns,
 $V_{IH} = 0.7 V_{DD}$, $V_{IL} = 0.3 V_{DD}$, $C_L = 100$ pF, See Fig. 4.

CHARACTERISTIC	V_{DD} (V)	LIMITS						UNITS
		CDP1859			CDP1859C			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Minimum Setup Time, Memory Address to Clock, t_{MACL}	5	—	25	40	—	25	40	ns
	10	—	10	25	—	—	—	
Minimum Hold Time, Memory Address After Clock, t_{CLMA}	5	—	0	25	—	0	25	ns
	10	—	0	10	—	—	—	
Minimum Clock Pulse Width, t_{CLCL}	5	—	50	75	—	50	75	ns
	10	—	25	40	—	—	—	
Propagation Delay Times:								
Clock to Address, t_{CLA}	5	—	125	200	—	125	200	ns
	10	—	65	100	—	—	—	
Clock to <u>CHIP ENABLE</u> , t_{CLCE}	5	—	175	275	—	175	275	
	10	—	90	140	—	—	—	
Memory Address to Address, t_{MAA}	5	—	100	150	—	100	150	
	10	—	50	75	—	—	—	
Memory Address to <u>CHIP ENABLE</u> , t_{MACE}	5	—	150	225	—	150	225	
	10	—	75	125	—	—	—	
<u>ENABLE</u> to <u>CHIP ENABLE</u> , t_{ECE}	5	—	125	200	—	125	200	
	10	—	65	100	—	—	—	

Typical values are for $T_A = 25^\circ\text{C}$ and nominal voltages.

Maximum limits of minimum characteristics are the values above which all devices function.

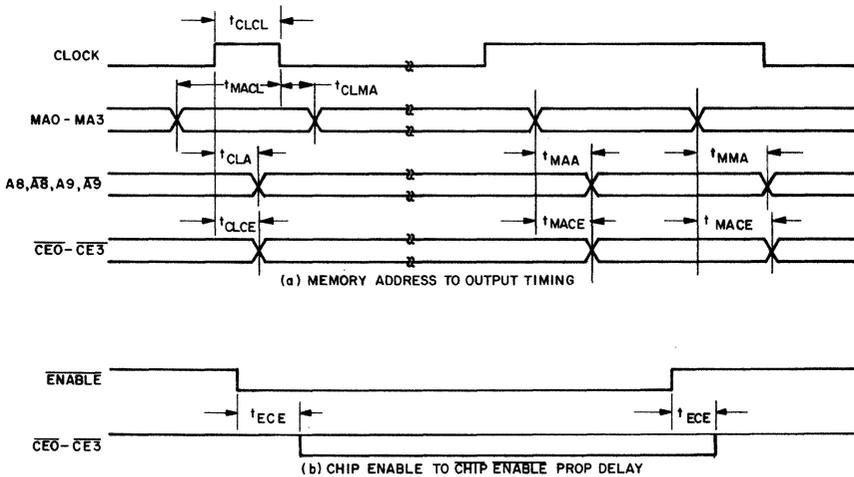


Fig. 4 — CDP1859 timing diagram.

CDP1858, CDP1858C, CDP1859, CDP1859C

CDP1858 DECODE TRUTH TABLE

ENABLE	DATA INPUTS		CS0	CS1	CS2	CS3	CE0	CE1	CE2	CE3
	MA1	MA0								
0	0	0	1	0	0	0	NOT AFFECTED BY MA1, MA0			
0	0	1	0	1	0	0				
0	1	0	0	0	1	0				
0	1	1	0	0	0	1				
	MA3	MA2								
0	0	0	NOT AFFECTED BY MA3, MA2				0	1	1	1
0	0	1					1	0	1	1
0	1	0					1	1	0	1
0	1	1					1	1	1	0
1	X	X	0	0	0	0	1	1	1	1

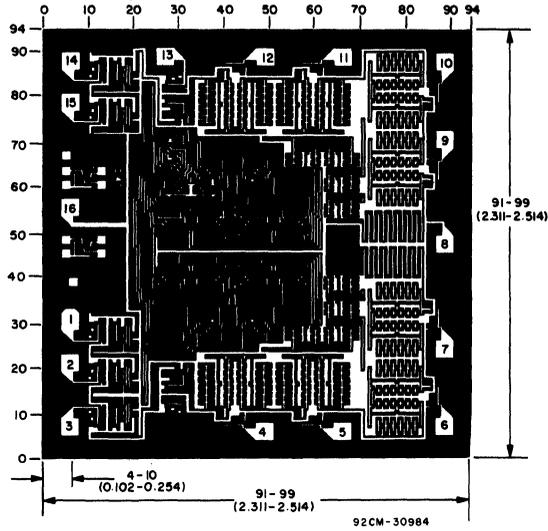
X = MA3, MA2, MA1, MA0 DON'T CARE

CDP1859 DECODE TRUTH TABLE

ENABLE	DATA INPUTS		A8	A9	A8	A9	CE0	CE1	CE2	CE3
	MA0	MA1								
0	0	0	0	0	1	1	NOT AFFECTED BY MA1, MA0			
0	0	1	0	1	1	0				
0	1	0	1	0	0	1				
0	1	1	1	1	0	0				
	MA3	MA2								
0	0	0	NOT AFFECTED BY MA3, MA2				0	1	1	1
0	0	1					1	0	1	1
0	1	0					1	1	0	1
0	1	1					1	1	1	0
1	X	X	NOT AFFECTED BY ENABLE				1	1	1	1

X = MA3, MA2, MA1, MA0 DON'T CARE

CDP1858, CDP1858C, CDP1859, CDP1859C

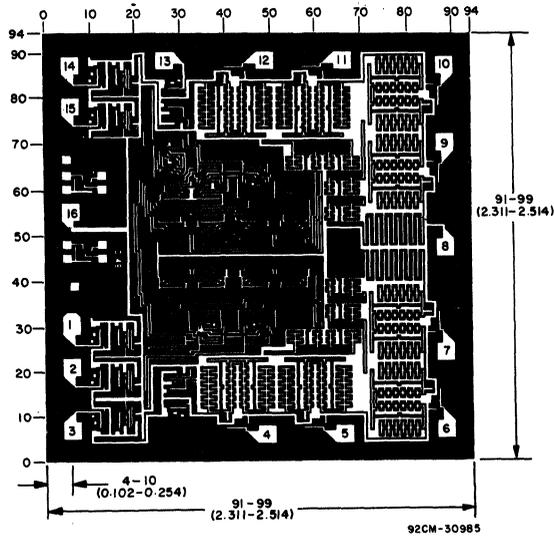


DIMENSIONS AND PAD LAYOUT FOR CDP1858

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each CMOS

chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.



DIMENSIONS AND PAD LAYOUT FOR CDP1859

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

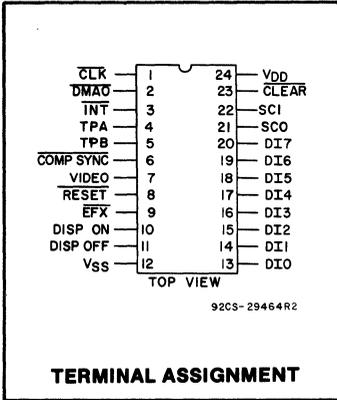
The photographs and dimensions of each CMOS

chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

CDP1861C

Preliminary Data

Video Display Controller

**Features:**

- Supports bit-mapped video display for graphic flexibility
- Generates composite horizontal and vertical sync
- Programmable vertical resolution for matrix display of up to 64 x 128 segments
- Real-time interrupt generator
- Clear input
- External display control

The RCA-CDP1861C is a video display controller designed for use in CDP1800-series microprocessor systems.

The CDP1861C utilizes many of the features of the CDP1800-series microprocessor to simplify control and minimize the need for external components. The DMA feature of the CDP1800-series microprocessor may be used for direct data transfers from memory to the CDP1861C. The INTERRUPT input and the I/O command lines may be used to perform the necessary handshaking between the CDP1800-series microprocessor and the CDP1861C. Timing may be simplified by operating the microprocessor at a clock frequency of 1.76064-MHz (the standard color frequency of 3.58 MHz, divided by 2, may also be used in some applications). The clock and the CDP1800-series microprocessor timing signals (TPA and TPB) may then be used to set the interface timing (as shown in the system diagram). In general, the clock frequency equals the number of fields per second (60), times the number of lines per field (262), times the number of machine cycles per line (14), times the number of bits per byte (8). In DMA operation, each machine cycle is a memory access.

Flexibility in vertical resolution may be obtained by synchronizing the CDP1861C with the CDP1800-series microprocessor and employing direct program control over the DMA process in real time. The actual video display takes place during a "window" of 4.6 milliseconds out of each 16.7-millisecond TV field. Throughout each such display window, a CDP1800-series microprocessor interrupt program may be used to manipulate the DMA pointer, re-issuing a given line of the display several times to save memory storage at the expense of reduced vertical resolution.

The CDP1861C generates composite vertical and horizontal sync plus luminance signals which can be combined externally to create an NTSC compatible composite video signal. This composite vertical and horizontal sync output signal (COMP SYNC) is generated from the sync reference (TPA) and TBP inputs. Vertical sync is derived from

horizontal sync by dividing the horizontal sync frequency by 262. The composite sync signal generates timing for a non-interlace video display of 262 lines per field.

The CDP1861C generates an interrupt request ($\overline{\text{INT}}$) once per field, 62 lines after the trailing edge of vertical sync and two lines before the raster has reached a "display window" (see Fig. 5). This request alerts the CDP1800-series microprocessor (or other control system) to prepare for DMA (direct memory access) activity. The CDP1861C DISP STATUS (EFX) output goes low during the 4 lines before the display window, and again during the last 4 lines of the window. This signal may be used to give early warning of the display window and to release the control system from monitoring the DMA activity.

Beginning in the third machine cycle of each line of the display window, and lasting for 8 cycles, the CDP1861C asserts the $\overline{\text{DMAO}}$ output to request a sequence of eight 8-bit bytes, which are then used to generate the VIDEO signal. Then, when control signals SCI and SCO are low and high respectively, each assertion of the TPB input causes the CDP1861C to read a byte from the BUS lines, and immediately to shift it out on the VIDEO output, high-order bit first. A DMA pointer defines an area of memory which is accessed by the CDP1861C to provide a bit-mapped display.

The display on (DISP ON) and display off (DISP OFF) inputs set and reset an internal control flip-flop in the CDP1861C. When this flip-flop is set, $\overline{\text{DMAO}}$ and INT are enabled; when reset, they are disabled.

The reset input (RESET) is a Schmitt trigger input that resets the CDP1861C. The CLEAR output is a conditioned output pulse which can be used to reset the external system.

The CDP1861C is supplied in 24-lead hermetic dual-in-line ceramic packages (D suffix), in 24-lead dual-in-line plastic packages (E suffix).

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) -0.5 to +7 V
 (Voltage referenced to V_{SS} Terminal)

INPUT VOLTAGE RANGE, ALL INPUTS -0.5 to V_{DD} +0.5 V

DC INPUT CURRENT, ANY ONE INPUT ±10 mA

POWER DISSIPATION PER PACKAGE (P_D):

For T_A = -40 to +60°C (PACKAGE TYPE E) 500 mW

For T_A = +60 to +85°C (PACKAGE TYPE E)..... Derate Linearly at 12 mW/°C to 200 mW

For T_A = -55 to +100°C (PACKAGE TYPE D)..... 500 mW

For T_A = +100 to +125°C (PACKAGE TYPE D) Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100 mW

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPE D -55 to +125°C

PACKAGE TYPE E -40 to +85°C

STORAGE TEMPERATURE RANGE (T_{stg}) -65 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. +265°C

STATIC ELECTRICAL CHARACTERISTICS, at T_A = -40 to +85°C, Except as Noted

CHARACTERISTIC		CONDITIONS			LIMITS			UNITS
		V _O (V)	V _{IN} (V)	V _{DD} (V)	CDP1861CD CDP1861CE			
					MIN.	TYP.*	MAX.	
Quiescent Device Current	I _{DD}	—	0, 5	5	—	50	250	μA
Input Leakage Current,	I _{IN}	Any Input	0, 5	5	—	±0.1	±1	μA
Input Low Voltage	V _{IL}	0.5, 4.5	—	5	—	—	1.5	V
Input High Voltage	V _{IH}	0.5, 4.5	—	5	3.5	—	—	
Output Voltage Low-Level	V _{OL}	—	0, 5	5	—	0	0.05	V
Output Voltage High-Level (Except DMAO, INT)	V _{OH}	—	0, 5	5	4.95	5	—	
Output Low Drive (Sink) Current INT, DMAO: CLEAR, EF: VIDEO, COMP SYNC:	I _{OL}	0.4	0, 5	5	0.2	0.5	—	mA
0.4		0, 5	5	0.4	0.8	—		
0.4		0, 5	5	0.8	1.6	—		
Output High Drive (Source) Current CLEAR EF: VIDEO, COMP SYNC:	I _{OH}	4.6	0, 5	5	-0.4	-0.8	—	mA
4.6		0, 5	5	-0.5	-1	—		
RESET (Schmitt Trig.) Pos. Trig. Threshold Neg. Trig. Threshold Hysteresis Voltage	V _P V _N V _H	— — —	— — —	5 5 5	— — —	2.5 1.7 0.8	— — —	V

* Typical values are for T_A = 25°C.

RECOMMENDED OPERATING CONDITIONS at T_A = Full Package Temperature Range

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC		CONDITIONS	LIMITS		UNITS
			CDP1861C		
		V _{DD} (V)	MIN.	MAX.	
DC Operating Voltage Range		—	4	6.5	V
Input Voltage Range		—	V _{SS}	V _{DD}	
Maximum Input Rise or Fall Time	t _r , t _f	5	—	5	μs
Maximum Clock Input Frequency	f _{CL}	5	DC	2.5	MHz

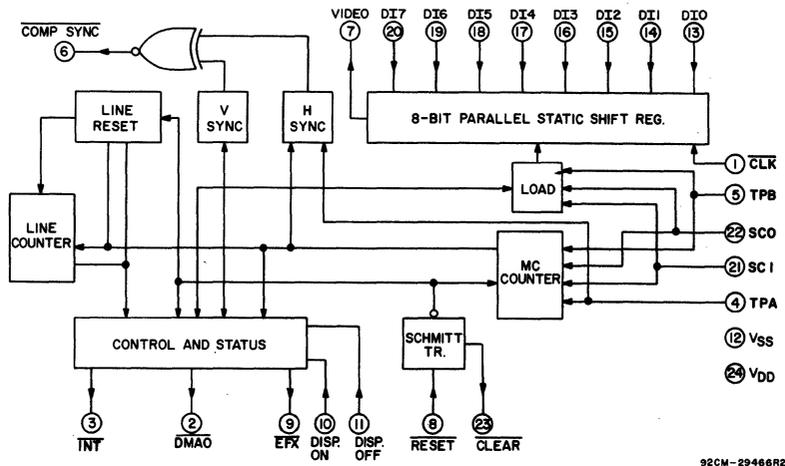


Fig. 1 - CDP1861C block diagram.

FUNCTIONAL DESCRIPTION OF CDP1861C TERMINALS

CLK:

The active low input for an externally generated single-phase clock which determines the clock rate for the 8-bit data shift register. Data are shifted on the high-to-low transition of the $\overline{\text{CLK}}$ input signal, most significant bit first. A low level (V_{SS}) is shifted into the least significant bit.

The $\overline{\text{CLK}}$ signal may be derived directly from the CDP1800-series microprocessor by connecting the $\overline{\text{CLK}}$ terminal of the CDP1861C to the XTAL terminal of the CDP1800-series microprocessor.

DMAO:

An active low output (V_{SS}) that requests an 8-bit data transfer. The output signal is from the "open drain" of an n-channel transistor and requires an external pull-up resistor to V_{DD} . Depending on the status of the SC0 and SC1 input signals at horizontal sync time, DMA requests are initiated on the leading edge of the second TPA input signal following the horizontal sync output. This feature is necessary in order to reference the data requests to the program's ability to respond to them, insuring that data will always be initiated at the same point on the display. The system should respond to a DMAO by setting SC0 high (V_{DD}), and SC1 low (V_{SS}), permitting data transfer. Data will be loaded on the subsequent 8 TPB input signals.

DMAO will be terminated on the ninth sync pulse, at which time SC0 should be set low (V_{SS}) prior to the next TPB command. Timing is illustrated in Figs. 3 and 5. The DMAO output signal may be connected to the DMA OUT Terminal of the CDP1800-series microprocessor, which responds as discussed above.

INT:

An active low (V_{SS}) output signal two horizontal cycles prior to the display, as shown in Figs. 3 and 5. This signal is the output of the "open drain" of an n-channel transistor and requires an external pull-up resistor to V_{DD} . The INT output signal is normally connected to the INTERRUPT input terminal of the CDP1800-series microprocessor. In a CDP1800-series microprocessor based system, 29 machine cycles occur from initiation of an INT until the DMAO.

TPA:

An active high timing pulse occurring once for every 8 clock pulses. The TPA signal is used as the clock for the horizontal line counter. It is normally tied to the TPA terminal of the CDP1800-series microprocessor. The TPA signal precedes the TPB signal.

TPB:

An active high timing pulse occurring once for every 8 clock pulses. The TPB signal is used as a strobe for gating the output of the counter and for loading data into the data register. It is normally connected to the TPB terminal of the CDP1800-series microprocessor.

COMP SYNC:

An active low output signal resulting from the exclusive "OR" of the output of the horizontal and vertical counters. COMP SYNC can be combined with the VIDEO output to form a composite video signal.

The COMP SYNC output frequency and pulse duration are determined by the TPA and TPB input signals. A horizontal sync pulse is initiated by the trailing edge of the TPB input signal following the 13th or 14th TPA input, as determined by the status of the SC0 and SC1 input signals, and is terminated on the leading edge of the subsequent second count of the TPA input.

Vertical timing is generated coincident with the 262nd horizontal timing pulse and is present for six horizontal clock cycles. Idealized timing is illustrated in Figs. 2 and 4.

VIDEO:

An active high output from the most significant bit of the 8-bit P/S data register. It is used to determine the luminance level and may be combined externally with the COMP SYNC output signal to form a composite video signal.

RESET:

An active low input signal which initializes the counters, inhibits the display, and places all control outputs in the high (V_{DD}) state. Refer to Fig. 3.

FUNCTIONAL DESCRIPTION OF CDP1861C TERMINALS (Cont'd)

RESET (Cont'd)

The **RESET** terminal is a Schmitt-trigger-type input which permits the use of an external RC network to provide a power-on reset.

EFX:

An active low output signal which occurs for a period of four horizontal cycles prior to the beginning and end of the 128-line display window, as illustrated in Figs. 2 and 4. The signal can be used by the program software routines to indicate the boundaries of the display area. It is normally connected to a CDP1800-series microprocessor EF1-EF4 FLAG input terminal.

DISP ON, DISP OFF:

Active high input signals that control the display. When enabled by pulsing **DISP ON** high (V_{DD}), data transfers, DMA, and interrupt requests are permitted. These operations are inhibited by the low-to-high transition of the **DISP OFF** input signal if **DISP ON** is low (V_{SS}). The **RESET** signal also inhibits the display. When inhibited, the internal counters remain operational. Sync and display status signals are generated. Video output becomes low when the register is emptied. Table I indicates the enable/disable conditions.

The **DISP ON** and **DISP OFF** signals may be provided by the I/O commands (N bits) of the CDP1800-series microprocessor.

TABLE I

STATE	SIGNAL		
	RESET	DISP ON	DISP OFF
RESET	L	L	X
INVALID	L	H	X
DISPLAY ENABLE	H		X
DISPLAY DISABLE	H	L	

D10 — D17:

Input signals to the data register. Data are loaded during the high-to-low transition of the **CLK** only when **TPB**, **DISP ON**, and **SC0** are high (V_{DD}), **SC1** is low (V_{SS}), and the CDP1861C is enabled.

The data input signals are normally connected to the 8-bit microprocessor data bus.

SC0, SC1:

Input signals used to synchronize the operation of the CDP1861C with its controller. They should be initiated prior to the **TPA** input and terminate after the **TPB** input pulse.

These control signals are sampled at two different times: **1)** During the horizontal sync output when the **TPA** input is present, the CDP1861C expects to see **SC1** = 1 (V_{DD}) and **SC0** = 0 (V_{SS}). Any other combination will result in the skipping of one of the normal 14 cycles per line. This feature allows the CDP1800-series microprocessor to force initial instruction fetch/execute sync with the CDP1861C, and assures sync in case it is later lost for any reason. **2)** In the 6 cycles following the CDP1861C **DMAO** assertion, the CDP1861C expects to see **SC1** = 0 and **SC0** = 1. Any other combination will prevent the CDP1861C from loading data from the bus.

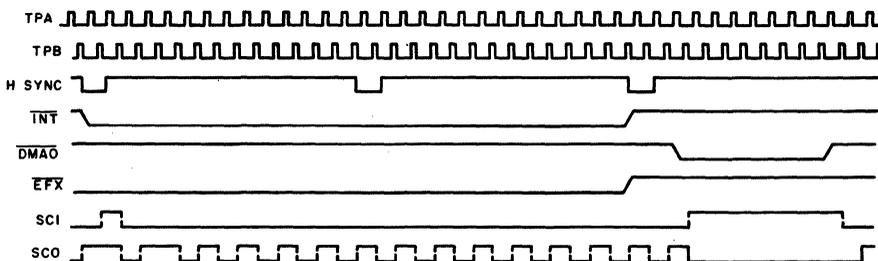
These signals may be connected to the STATE CODE (**SC0, SC1**) outputs of the CDP1800-series microprocessor.

CLEAR:

The output of the Schmitt trigger (reset input circuitry) provides high speed transitions that may be used to reset other devices. It may be connected to the **CLEAR** terminal of the CDP1800-series microprocessor.

VDD, VSS:

V_{DD} is the positive supply voltage terminal, V_{SS} is the negative supply voltage terminal and is normally connected to ground.



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Fig. 2 - Horizontal sync timing diagram.

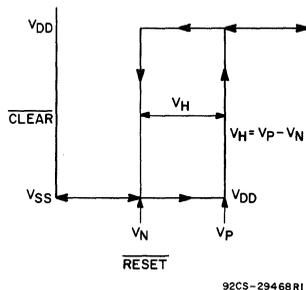


Fig. 3 - Reset transfer characteristics.

APPLICATION INFORMATION (CDP1861C DIRECTLY CONTROLLED BY THE CDP1800-SERIES MICROPROCESSOR)

Figure 5 shows a simple graphic display system using the CDP1800-series microprocessor and the CDP1861C. The CDP1861C uses both the INTERRUPT and direct memory access (DMA) output channel of the microprocessor for display refresh. The microprocessor specifies the area of memory displayed via the interrupt routines, and the DMA output channel is the mechanism which transfers the data from memory to the CDP1861C via the 8-bit data bus. The data are then shifted out one bit at a time at the clock frequency to generate the video (VIDEO) signal.

The composite sync ($\overline{\text{COMP SYNC}}$) signal creates a 262-line-per-field, 60-field-per-second non-interlace video picture. The non-interlaced picture frame for this display consists of two even fields of 262 horizontal lines each. This format differs slightly from the National Television Standard (NTSC) which has a 525-line interlaced picture frame of one odd field and one even field. The vertical sync pulse generated at $\overline{\text{COMP SYNC}}$ of the CDP1861C has no equalizing pulses but is serrated to maintain horizontal synchronization during the vertical blanking time. The VIDEO and $\overline{\text{COMP SYNC}}$ pulses are resistively coupled to create the composite video, which can be supplied directly to a video monitor, a modified TV receiver, or a FCC approved rf modulator.

A clock source of 3.58 MHz, the NTSC color frequency, if divided by 2, may be used for some applications in place of the 1.76-MHz crystal shown in Fig. 5. Deviations from the NTSC frequencies are as follows:

The user should determine which choice of frequencies provides an optimal cost/performance trade-off for his application. Generally, video CRT's are more sensitive to line frequency accuracy than to field frequency accuracy.

The display is a bit map of memory. Each bit in the display memory corresponds to one spot on the video screen. Logical 1 (V_{DD}) bits in memory correspond to white or lighted spots in the display. The highest resolution that may be produced is 128 vertical by 64-horizontal segments. This resolution requires 1024 bytes of memory for the display. The upper left-most spot that can be displayed on the video screen is the most significant bit of the first byte in the display refresh memory buffer. The starting location of the display buffer is initialized in the INTERRUPT routine and may be anywhere in addressable memory (ROM, RAM, or both). The lower right-most spot that can be displayed is the least significant bit of the last byte of the display bit map. For each of the 128 horizontal display lines, 8 bytes of memory are sequentially accessed and displayed from left to right on the video screen. Adjacent illuminated spots

appear contiguous both in the horizontal and in the vertical directions. All display manipulations are accomplished by changing the data within the display buffer or by changing display buffers.

To control the CDP1861C as shown in Fig. 5, the CDP1800-series microprocessor must be in synchronization with the CDP1861C during the display window. Exactly six machine cycles must be executed beyond the eight DMA cycles during each line, and an even number of cycles (262 x 14) must be executed from the start of one display window to the start of the next. These requirements insure that the DMA burst will not be delayed one cycle waiting for an instruction to finish — this delay would cause jitter on the screen. These requirements can be accomplished in two steps: 1) the main program must not execute any 3-cycle instructions (i.e., SKIP, LONG BRANCHES, and NOP), and 2) the interrupt routine, including the interrupt cycle itself, must employ an even number of cycles, and must be synchronized with the DMA bursts. There must be 29 cycles between the INTERRUPT cycle (S3) and the first burst of eight DMA cycles. This timing is accomplished by executing an early 3-cycle instruction to compensate for the INTERRUPT cycle. Furthermore, exactly three 2-cycle instructions must be executed between each successive burst. Occasionally these restrictions may be ignored at the expense of jitter on the screen.

For the 128 x 64 display, the CDP1800-series microprocessor software requirement is straightforward. The DISP STATUS/EF1 line is not required, and EF1 may be used for other purposes. A simple interrupt routine merely resets the DMA pointer, RO, to the beginning of the display buffer area (see Fig. 8) — note the 3-cycle NOP instruction at the beginning which compensates for the 1-cycle interrupt. The first burst of eight DMA cycles occurs just as this routine finishes, as indicated by the bracket following the RETURN instruction (70). Exactly 29 cycles separate the interrupt request cycle and the first DMA burst. The interrupt routine must last at least 28 cycles, because the interrupt request line is held up that long by the CDP1861C.

When less RAM is to be used (less resolution), a more complicated interrupt routine is used. The interrupt routine is protracted for the full duration of the display window, and the six free cycles in each line are used to execute three instructions, which maintain control over the DMA pointer, RO.1. In the simplest cases, each line of 8 bytes is repeated n times to give 128/n vertical resolution. With n = 4, for example, 64 x 32 resolution is obtained. Such an interrupt routine is shown in Fig. 7. The use of three instructions per

APPLICATION INFORMATION (CDP1861C DIRECTLY CONTROLLED BY THE CDP1800-SERIES MICROPROCESSOR)
(Cont'd)

line does not leave time to control a loop, so each of four copies of the line corresponds to three instructions in the main loop, starting at \overline{EFX} . The \overline{EFX} signal, applied to \overline{EFT} , is used to signal the last pass through the loop.

For other values of n , similar routines can be devised. For $n = 2$, the 64×64 format, the last 4 lines need special treatment (see Fig. 6). Other schemes are possible, resulting in other resolutions which vary on command from the main program,

or even resolutions which vary through the display window.

In general, additional functions may be implemented in the routine before returning to the main program. For example, a real-time clock can be maintained by incrementing a counter once on each interrupt, i.e., once per 1/60 second. Another example is vertical "scrolling" of the display, wherein the starting address in a display file is incremented or reincremented at regular intervals.

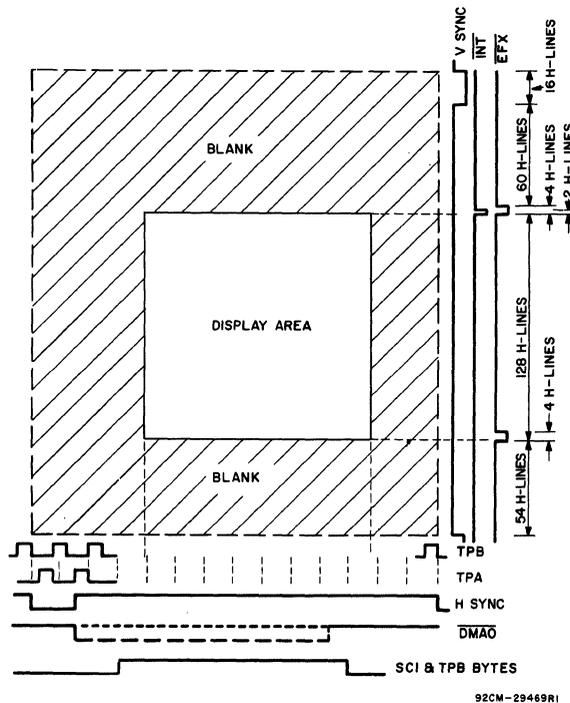


Fig. 4 - Spatial diagram of one video display field (not to scale).

NTSC		CLOCK FREQUENCIES (MHz)		
Line Freq.	Field Freq.	1.76064	1.764000	3.579545/2
15750	60	15720	15750	15980
		60	60.11	60.99

RCA CMOS LSI Products
CDP1861C

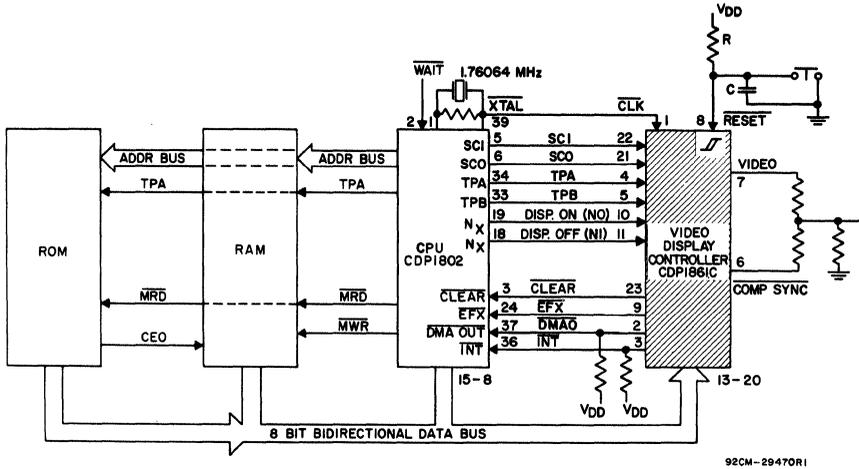


Fig. 5 - Typical CDP1802/CDP1861C video display system.

Machine Code		Assembly Language	Comments
72		INTRET : LDXA	.. RESTORE D
70		RET	.. RETURN
C4		INT : NOP	.. 3 CYC. INSTR. FOR PGM. SYNC
22		DEC R2	.. R2 IS STACK PTR
78		SAV	.. T-STACK
22		DEC R2	
52		STR R2	.. D-STACK
F8-B0		A.1 (DISMEM)--RO.1	.. DISMEM IS START ADDR
F8-A0		A.0 (DISMEM)--RO.0	.. OF DISPLAY MEMORY
C4, C4		NOP; NOP	.. NOPS FOR PGM SYNC
E2		SEX2	
80]	DISP	: GLO RO	.. NEW LINE
E2		SEX2	.. NOP
20		DEC RO	.. RESTORES RO.1 IF PASS PG
A0]		PLO RO	.. REPEATS SAME LINE
E2		SEX2	.. NOP
3C—		BN1 DISP	.. LOOP 60 TIMES
80]	DISEF	: GLO RO	.. LAST 4 VIDEO LINES
E2		SEX2	.. NOP
20 A0]		DEC RO; PLO RO	
E2		SEX2	.. NOP
34—		B1 DISEF	
30—		BR INTRET	.. END OF DISPLAY

Fig. 6 - Interrupt routine for 64 x 64 format (2 pgs mem).

Machine Code		Assembly Language	Comments
72	INTRET	: LDXA	.. RESTORE D
70		RET	.. RETURN
C4	INT	: NOP	.. 3 CYC. INSTRU. USED
			.. FOR PGM. SYNC
22		DEC R2	.. R2 IS STACK PTR
78		SAV	.. T-STACK
22		DEC R2	
52		STR R2	.. D-STACK
F8-B0		A.1 (DISMEM)--R0.1	.. LOAD RO WITH
F8-A0		A.0 (DISMEM)--R0.0	.. START ADDR. OF DISP. MEM
C4, C4		NOP; NOP	.. NOPS USED FOR SYNC
E2	DISP	: SEX2	
80]		GLO RO	.. LINE START ADDR.--D
E2		SEX2	.. NOP
20		DEC RO	.. RESET RO.1 IF PASS PG
A0]		PLO RO	.. LINE START ADDR.--RO.0
E2		SEX2	.. NOP
20		DEC RO	.. RESET RO.1 IF PASS PG
A0]		PLO RO	.. LINE START ADDR.--RO.0
E2		SEX2	.. NOP
20		DEC RO	.. RESET RO.1 IF PASS PG
A0]		PLO RO	.. REPEATS SAME LINE
3C—		BN1 DISP	.. LOOPS 32 TIMES
30—		BR INTRET	.. END OF DIPLAY

Fig. 7 - Interrupt routine for 64 x 32 format (1 pg mem).

Machine Code		Assembly Language	Comments
72	INTRET	: LDXA	.. RESTORE D
70]		RET	.. RETURN
C4	INT	: NOP	.. ENTRY POINT
22		DEC R2	.. R2 = STACK PTR
78		SAV	.. T-STACK
22		DEC R2	
52		STR R2	.. D-STACK
E2, E2		SEX R2; SEX R2	.. NOP
F8-B0		A.1 (DISMEM)--R0.1	.. LOAD RO WITH
F8-A0		A.0 (DISMEM)--R0.0	.. START ADDR OF DISP. MEM.
30—		BR INTRET	.. BRANCH TO INTERRUPT RETURN

Fig. 8 - Interrupt routine for 64 x 128 (4 pgs mem).

OPERATING AND HANDLING CONSIDERATIONS**1. Handling**

All inputs and outputs of RCA CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in ICAN-6525, "Guide to Better Handling and Operation of CMOS Integrated Circuits."

2. Operating**Operating Voltage**

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must

not cause $V_{DD} - V_{SS}$ to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS} . Input currents must not exceed 10 mA even when the power supply is off.

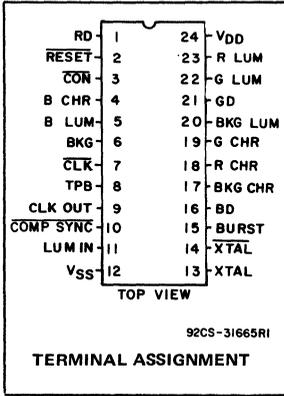
Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS} , whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} or V_{SS} may damage CMOS devices by exceeding the maximum device dissipation.

CMOS Color Generator Controller



Features:

- Interfaces directly with CDP1861C Video Display Controller
- Programmable background color
- Programmable video (dot) color
- On-chip crystal controlled oscillator
- NTSC and RGB compatible

The RCA-CDP1862C is a color generator controller designed for use in CDP1800-series microprocessor systems. It is intended for use with the RCA-CDP1861C video display controller and will interface directly with the CDP1802/CDP1861C as shown in the system diagram below.

The CDP1862C utilizes many features of the CDP1802 and CDP1861C to simplify control and minimize the need for external components. The CDP1862C is NTSC color compatible. Red, green and blue luminance signals are also available for directly controlling the red, green and

blue amplifiers of a video monitor. A 7.15909-MHz on-chip crystal-controlled oscillator or an external 7.15909-MHz clock is used to generate multiple phases of the 3.579545-MHz color burst frequency for NTSC-compatible color. The color burst is further divided by 2 to provide system timing for the CDP1802 and the CDP1861C. This frequency [1.789773 MHz] is available at CLK OUT. Two inputs TPB and COMP SYNC, are used to maintain system synchronization. The RESET input resets the CDP1862C and sets the background color to blue and the dot color to white.

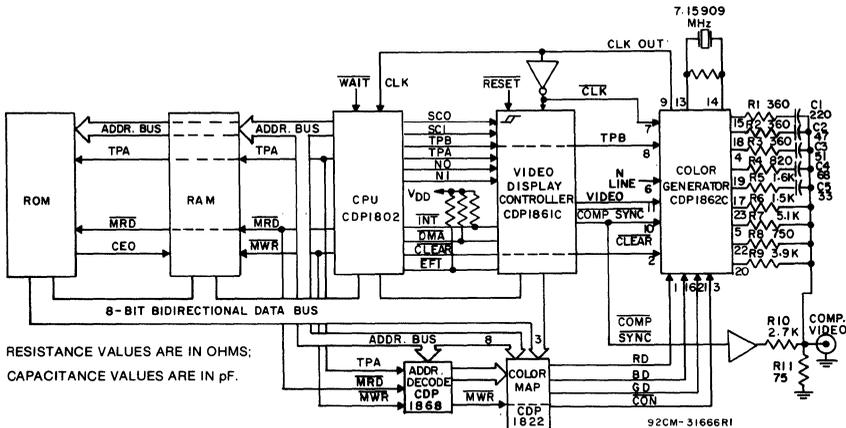
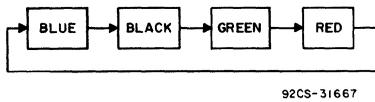


Fig. 1-Typical CDP1802 microprocessor system using the CDP1862C.

Background color: Four background colors are available. The colors are changed each time TPB is pulsed when BKG = high. The sequence is from blue to black to green to red and return to blue [see Fig. 2].



92CS-31667

Fig. 2-Background Color Sequencing.

Dot color: Color data [RD, BD, GD] is latched internally on the high-to-low transition of CLK when TPB = high. Eight colors are available as shown in Table I. The color is overlaid onto the LUM IN data [video output from CDP1861C]. Each color

TABLE I - Color Table

RD	BD	GD	COLOR
0	0	0	Black
0	0	1	Green
0	1	0	Blue
0	1	1	Cyan
1	0	0	Red
1	0	1	Yellow
1	1	0	Purple
1	1	1	White

corresponds to eight horizontal bits of video information. Only the selected background color appears at the output if LUM IN = low. When used with the CDP1861C and set for the maximum

resolution of 64 x 128, 1024 color blocks [8 x 128] are possible, and would require a 1K x 3 random-access memory storage area. This area would appear to be write-only memory to the microprocessor because, in the programmed state, this area occupies an unique, unused 1K block of memory space. However, when it is read, this area responds to the same address space occupied by the CDP1861C refresh RAM. This is accomplished with proper decoding and requires the memory to have separate I/O lines.

The CON input enables the RD, BD and GD input latches. After a RESET condition, the dot color is set to white and any color change is inhibited until the CON input is pulsed low, which normally occurs when data is written into the color map. The CON input provides a means of inhibiting erroneous color data until the color map is properly loaded.

The color luminance [R LUM, B LUM, G LUM], color chrominance [R CHR, B CHR, G, CHR], background luminance [BKG LUM], background chrominance [BKG CHR], color burst [BURST], and COMP SYNC are combined by an external RC network to generate the composite video [see Fig. 1].

The BURST signal is normally high and oscillates at 1/2 the XTAL frequency from the low-to-high transition of COMP SYNC until TPB = high.

The CDP1862C types are supplied in 24-lead hermetic dual-in-line side-braced ceramic packages [D suffix], and in 24-lead dual-in-line plastic packages [E suffix].

RECOMMENDED OPERATING CONDITIONS at $T_A = 25^\circ\text{C}$, Except as Noted.

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V _{DD} (V)	LIMITS		UNITS
		Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	—	4	6.5	V
Input Voltage Range	—	V _{SS}	V _{DD}	
Input Signal Rise or Fall Time, t_r , t_f	5	—	5	μs
Clock Input Frequency, f_{CL}	5	7.15909		MHz

CDP1862C

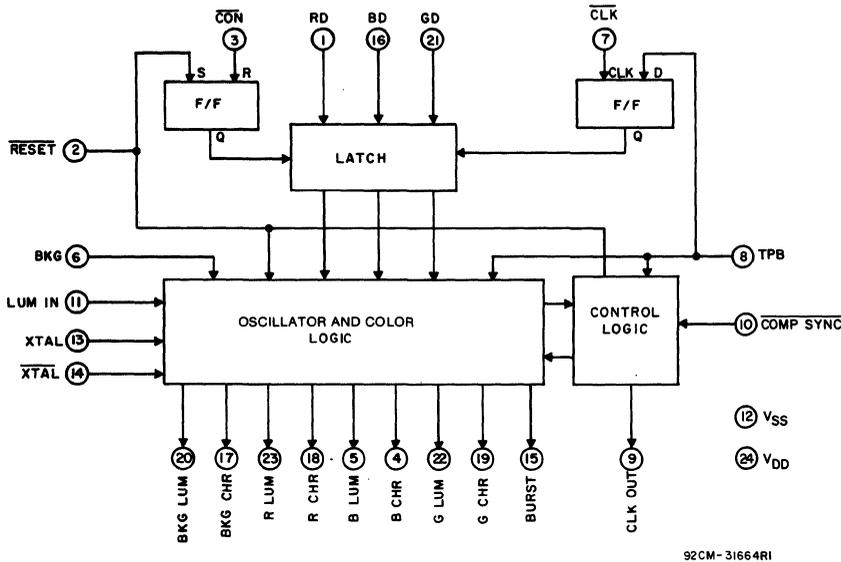
MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	-0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	± 10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For $T_A = -40$ to $+60^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +60$ to $+85^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 12 mW/ $^\circ\text{C}$ to 200 mW
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE D)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE D)	Derate Linearly at 12 mW/ $^\circ\text{C}$ to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR $T_A =$ FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE D	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E	-40 to $+85^\circ\text{C}$
STORAGE TEMPERATURE RANGE (T_{stg})	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ inch (1.59 ± 0.79 mm) from case for 10 s max.	$+265^\circ\text{C}$

STATIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, except as noted.

CHARACTERISTIC	CONDITIONS			LIMITS			UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	CDP1862CD CDP1862CE			
				Min.	Typ.*	Max.	
Quiescent Device Current, I_L	-	0, 5	5	-	50	250	μA
Output Low Drive (Sink) Current, I_{OL} (Except XTAL)	0.4	0, 5	5	2	2.4	-	mA
XTAL Output, I_{OL}	0.4	0, 5	5	150	200	-	μA
Output High Drive (Source) Current, I_{OH} (Except XTAL)	4.6	0, 5	5	-1.6	-1.8	-	mA
XTAL Output, I_{OH}	4.6	0, 5	5	-150	-200	-	μA
Output Voltage Low-Level, V_{OL}	-	0, 5	5	-	0	0.1	V
Output Voltage High Level, V_{OH}	-	0, 5	5	4.9	5	-	
Input Low Voltage, V_{IL}	0.5, 4.5	-	5	-	-	1.5	
Input High Voltage, V_{IH}	0.5, 4.5	-	5	3.5	-	-	
Input Leakage Current, I_{IN}	Any Input	0, 5	5	-	± 0.1	± 1	μA

* Typical values are for $T_A = 25^\circ\text{C}$ and nominal voltage.



92CM-31664RI

Fig. 3-Functional block diagram.

SIGNAL DESCRIPTIONS

RESET

A low level on this input initializes the internal counters, sets the background color to blue, and sets the dot color to white.

BKG

A high level on this input enables the background color to be changed when TPB is pulsed high. This signal is normally connected to an I/O line of the 1800-Series microprocessor.

CLK

An input signal used to latch the color data information. Color data [RD, BD, GD] is latched on the high-to-low transition of CLK when TPB = high. This signal is normally connected to CLK OUT through an inverter.

TPB

A high level on this input enables color data latching and sequences background color when BKG = high. This signal is normally connected to the TPB terminal of the 1800-Series microprocessor.

CLK OUT

An output signal, equal to the XTAL frequency divided by four, that provides the overall system synchronization. This signal is normally connected to the CLOCK terminal of the 1800-Series microprocessor.

The inverse of this signal is normally connected to the CLOCK terminal of the CDP1861C and the CLK terminal of the CDP1862C.

COMP SYNC

An input signal used to provide horizontal line synchronization between the CDP1861C and the CDP1862C color signals. This signal is normally connected to the COMP SYNC terminal of the CDP1861C.

LUM IN

The luminance video input, to which the color information is added. One color block corresponds to eight serial bits of data from this input. This input is normally connected to the VIDEO terminal of the CDP1861C.

VSS

Negative supply voltage; ground.

XTAL, XTAL

Terminal connections for an external crystal, in parallel with a resistance [10 megohms typ.] if the on-chip oscillator is utilized. Frequency trimming capacitors may be required at terminals 13 and 14. XTAL is the input for an externally generated single-phase clock.

BURST

The color reference output, which oscillates at the XTAL frequency divided by 2.

CDP1862C

This signal provides approximately 11 cycles of 3.579545 MHz from the low-to-high transition of COMP SYNC until TPB = high. This signal is coupled through an external series RC circuit to the COMP SYNC output of the CDP1861C.

RD, BD, GD

The red, blue, and green color data inputs. One of eight colors is latched on the high-to-low transition of CLK when TPB = high, forming a color block of eight horizontal LUM IN data bits. Only the selected background color appears at the output if LUM IN = low. These inputs are normally connected to the DATA OUT terminals of the color map memory.

BKG LUM, R LUM, B LUM, G LUM

These output signals provide background and color luminance information. They are resistively added externally to the COMP SYNC output of the CDP1861C.

BKG CHR, R CHR, B CHR, G CHR

These output signals provide background and color chrominance information. They are coupled through an external series RC circuit to the COMP SYNC output of the CDP1861C. Each signal is phase-shifted from the BURST reference signal by the amount necessary for proper color operation.

CON

The color data input latch enable signal. After a RESET condition, the internal RD, BD, and GD input latches are held in a reset state, providing a white color output. When CON is pulsed low, the reset state is removed and the latches are enabled, providing color output. This input is normally connected to the gated MWR signal from the 1800-Series Microprocessor.

VDD

Positive supply voltage.

OPERATING AND HANDLING CONSIDERATIONS

1. Handling

All inputs and outputs of RCA CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in ICAN-6525, "Guide to Better Handling and Operation of CMOS Integrated Circuits."

2. Operating

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of

these conditions must not cause $V_{DD}-V_{SS}$ to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS} . Input currents must not exceed 10 mA even when the power supply is off.

Unused Inputs

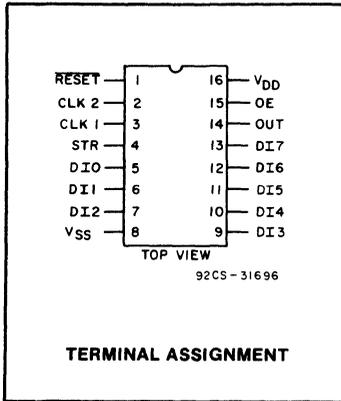
A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS} , whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} or V_{SS} may damage CMOS devices by exceeding the maximum device dissipation.

Preliminary Data

CMOS 8-Bit Programmable Frequency Generator



Features:

- Directly interfaces with CDP1800-series microprocessors
- 256 possible programmable frequencies
- Two clock input predividers ($\div 4$ and $\div 8$)
- Gated square-wave output
- Single 4 to 10.5 V supply

The RCA-CDP1863 and CDP1863C CMOS integrated circuits are programmable frequency generators designed to produce 256 possible frequencies from a single-frequency input clock. They will interface directly with the CDP1800-series microprocessor as shown in the system diagram (see Fig. 1).

The CDP1863 and CDP1863C consist of a programmable up-counter and an 8-bit latch (see Fig. 2). An input clock is predivided by a fixed internal counter chain in addition to the programmable counter. The final stage of the device divides the output of the up-counter by two to provide a square-wave output. The input clock may be applied to either of two inputs; CLK1 provides a divide-by-four predivide, and CLK2 a divide-by-eight. The unused input must be tied to V_{DD} to avoid interference with the true clock. After the programmable up-counter has reached its maximum count, the next predivided clock pulse will cause it to go to zero. At this time, the output flip-flop toggles and the load flip-flop is turned on. The output of the load flip-flop is fed into the NOR gates which allow the divide rate stored in the 8-bit latch to preset the up-counter. Before the next predivided clock pulse clocks this up-counter, the load flip-flop is reset and the NOR gates are turned off. The counter then re-

sumes its up-count. The data at the eight data inputs is latched into the device by the high-to-low transition of CLK1, when STR(STROBE) is high, or by the high-to-low transition of STR, when CLK1 is high.

When using CLK2, CLK1 must be tied to V_{DD} to permit the STR input to generate the internal latch clock. The 8-bit data in the latch determines the divide rate of the programmable up-counter in the device. This rate may range from divide-by-one to divide-by-256.

A low level on the RESET input resets the up-counter, predividers, and flip-flops, and forces an initial state into the 8-bit data latch. This initial state provides a fixed divide rate for the device prior to running the system. A high level on the RESET input enables the up-counter, predividers, and flip-flops and allows programming a new divide rate into the device.

The CDP1863 and CDP1863C are functionally identical. They differ in that the CDP1863 has an operating voltage range of 4 to 10.5 volts and the CDP1863C has an operating voltage range of 4 to 6.5 volts. Both are supplied in 16-lead hermetic dual-in-line ceramic packages (D suffix) and in 16-lead dual-in-line plastic packages (E suffix).

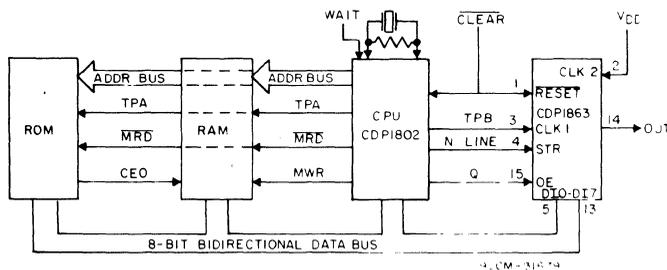


Fig. 1 — Typical CDP1800-series microprocessor system using the CDP1863 and CDP1863C.

RCA CMOS LSI Products

CDP1863, CDP1863C

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD}):

(Voltage referenced to V_{SS} Terminal)

CDP1863	-0.5 to +11 V
CDP1863C	-0.5 to +7 V

INPUT VOLTAGE RANGE, ALL INPUTS -0.5 to $V_{DD} + 0.5$ V

DC INPUT CURRENT, ANY ONE INPUT ± 10 mA

POWER DISSIPATION PER PACKAGE (P_D):

For $T_A = -40$ to $+60^\circ\text{C}$ (PACKAGE TYPE E) 500 mW

For $T_A = +60$ to $+85^\circ\text{C}$ (PACKAGE TYPE E) Derate Linearly at 12 mW/ $^\circ\text{C}$ to 200 mW

For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE D) 500 mW

For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE D) Derate Linearly at 12 mW/ $^\circ\text{C}$ to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

For $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE}$ (All Package Types) 100 mW

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPE D -55 to $+125^\circ\text{C}$

PACKAGE TYPE E -40 to $+85^\circ\text{C}$

STORAGE TEMPERATURE RANGE (T_{stg}) -65 to $+150^\circ\text{C}$

LEAD TEMPERATURE (DURING SOLDERING):

At distance $1/16 \pm 1/32$ inch (1.59 ± 0.79 mm) from case for 10 s max. $+265^\circ\text{C}$

STATIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, except as noted

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	CDP1863			CDP1863C			
				MIN.	TYP.*	MAX.	MIN.	TYP.*	MAX.	
Quiescent Device Current, I_L	—	—	5	—	50	250	—	50	250	μA
	—	—	10	—	250	500	—	—	—	
Output Low Drive (Sink) Current, I_{OL}	0.4	0.5	5	1.6	2.2	—	1.6	2.2	—	mA
	0.4	0.10	10	3	3.6	—	—	—	—	
Output High Drive (Source) Current, I_{OH}	4.5	0.5	5	-1	-1.6	—	-1	-1.6	—	mA
	9.5	0.10	10	-3	-3.6	—	—	—	—	
Output Voltage Low-Level, V_{OL}	—	0.5	5	—	0	0.05	—	0	0.05	V
	—	0.10	10	—	0	0.05	—	—	—	
Output Voltage High-Level, V_{OH}	—	0.5	5	4.95	5	—	4.95	5	—	V
	—	0.10	10	9.95	10	—	—	—	—	
Input Low Voltage, V_{IL}	0.5,4.5	—	5	—	—	1.5	—	—	1.5	V
	0.5,9.5	—	10	—	—	3	—	—	—	
Input High Voltage, V_{IH}	0.5,4.5	—	5	3.5	—	—	3.5	—	—	V
	0.5,9.5	—	10	7	—	—	—	—	—	
Input Leakage Current, I_{IN}	Any	0.5	5	—	± 0.1	± 1	—	± 0.1	± 1	μA
	Input	0.10	10	—	± 0.1	± 1	—	—	—	
Operating Current, $I_{DD1}\ddagger$	—	0.5	5	—	0.67	1	—	0.67	1	mA
	—	0.10	10	—	3.5	4.5	—	—	—	

*Typical values are for $T_A = 25^\circ\text{C}$

†Measured with CLK1=2 MHz, total divide rate of 8, $C_L = 50$ pF.

‡Measured with CLK1=4 MHz, total divide rate of 8, $C_L = 50$ pF.

OPERATING CONDITIONS at $T_A = 25^\circ\text{C}$ Unless Otherwise Specified
 For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges

CHARACTERISTIC	LIMITS				UNITS
	CDP1863		CDP1863C		
	MIN.	MAX.	MIN.	MAX.	
Supply-Voltage Range (At $T_A = \text{Full Package-Temperature Range}$)	4	10.5	4	6.5	V
Recommended Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V
Input Signal Rise and Fall Time, t_r, t_f	—	.5	—	5	μs

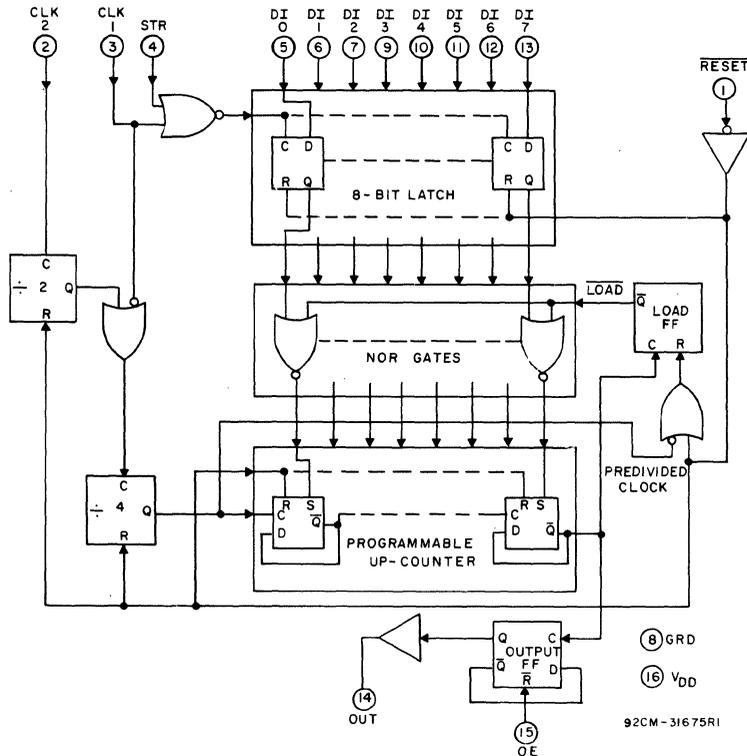


Fig. 2 — Block diagram for the CDP1863 and CDP1863C.

SIGNAL DESCRIPTIONS

CLK1, CLK2

Input clock which is divided-down by the device to provide an output frequency. The divide rate of the device is composed of a fixed predivide, the programmable divider, and a divide-by-two output flip-flop which provides a square-wave output. CLK1 is pre-divided by four and CLK2 is pre-divided by eight. The unused CLOCK input must be tied to V_{DD} to avoid interference with the true CLOCK signal. CLK1 may also be used to latch the eight data inputs.

OUT

Square-wave output which is the result of the divided-down input CLOCK. The OUTPUT toggles after the programmable up-counter reaches its maximum value and goes to zero. OUT is held low when OE is low.

OE

A high on this input allows OUT to toggle freely. A low on OE holds OUT low.

SIGNAL DESCRIPTIONS (Cont'd.)

D10-D17

Data inputs for programming the divide rate of the device. The divide rates programmed into the device are inversely proportional to the output frequencies generated. For example, programming the device with 00_{16} causes the programmable up-counter to divide by one, providing the maximum output frequency for any given input clock. Programming an FF_{16} results in the maximum divide rate and the minimum output frequency. To determine the frequency generated by a given programmed divide rate, divide the input clock frequency by the decimal equivalent of the programmed divide rate plus one, times the fixed predivide which is 8 for CLK1 or 16 or CLK2:

$Input\ Clock\ Frequency / [(Programmed\ Divide\ Rate + 1)_{10} (Fixed\ Predivide)]$

STR

Positive pulse used to latch data at the eight inputs into the device. This pulse is gated with CLK1 to form the internal latch clock. When CLK1 is the input clock, the STR input

must be positive during the high-to-low transition of CLK1. When CLK2 is the input clock, CLK1 must be tied to V_{DD} so that the STR input produces the latch clock.

RESET

A low on the **RESET** input resets all the stages of the predictors and the programmable up-counter and sets an initial divide rate into the latch. This is to provide a standard initial divide rate at the moment the system begins running. A high on **RESET** enables the counter to run freely and allows programming a new divide rate. The initial state of the up-counter is a divide-by-54 resulting in a total divide rate of 432, after 1024 clock pulses when using CLK1, and 864, after 2048 clock pulses when using CLK2.

V_{DD}

Positive supply voltage.

V_{SS}

Negative supply voltage; ground.

APPLICATION

The programmable frequency generator is directly compatible with the CDP1802 CMOS microprocessor. In Fig. 1 a simple CDP1802 system using this device is shown. TPB may be used as the input clock. At typical CDP1802 system clock frequencies, using TPB as an input to CLK1 results in nearly every possible output of the device being in the audio range. The Q output of the CDP1802 may be used as the OUTPUT ENABLE (OE) of the device. The eight data inputs are connected to the bidirectional data bus which allows the system memory to provide divide rate data to the device. A single N bit or some decoded output of all the N bits may be used as the STR input to latch data into the device. This involves designating some output instruction of the CDP1802 for providing the STR. The output instruction places the data pointed to by the X register on the bus, while simultaneously pulsing the appropriate N bits. By the internal gating of TPB and STR, when TPB is fed into CLK1, the resulting latch clock terminates while the data is still valid on the 8-bit bus. If TPB is fed into CLK2, it is necessary to provide an external AND gate for the appropriate N bits and TPB, to preserve this timing feature. The same signal that feeds the CLEAR input of the CDP1802 may be used as the RESET signal to this device.

As an example of programming the frequency generator, assume a 64 instruction is selected as the output code used to program the device. Let machine register E point to the data to be latched. N2 is the only N bit pulsed by a 64 instruction and may be fed directly to the STR input if TPB is fed to CLK1. An EE instruction makes RE the X register. Following this with a 64 instruction puts the data pointed to by RE onto the data bus and raises the N2 bit. TPB, which is within the duration of the N2 pulse, causes the internal latch clock to terminate before the data bus loses validity. The latch in the device continually passes the data inputs through to the outputs of the latch as long as CLK1 and STR are high. Once CLK1 goes low, data is locked in. A 7B instruction then sets the Q line high which, if connected to OE, allows the OUT to toggle at the desired rate.

Code:

- EE RE is the X register
- 64 M(E)-BUS N2 pulsed high
- 7B Q turned on

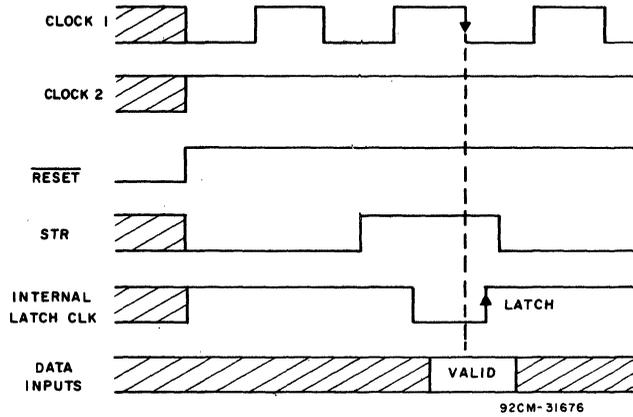


Fig. 3 — General CLOCK 1 timing diagram.

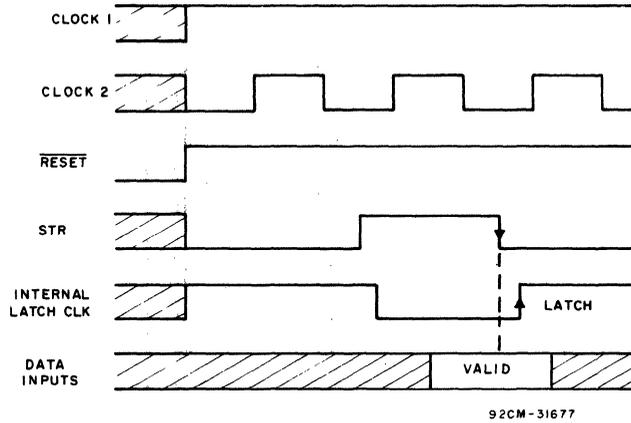


Fig. 4 — General CLOCK 2 timing diagram.

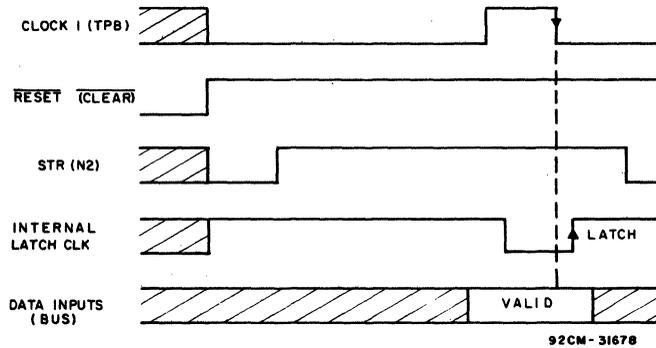


Fig. 5 — General CDP1800-series microprocessor system timing diagram.

CDP1863, CDP1863C

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} \pm 5\%$, $C_L = 50\text{ pF}$

CHARACTERISTIC	V_{DD} (V)	LIMITS						UNITS
		CDP1863			CDP1863C			
		MIN.	TYP.*	MAX.	MIN.	TYP.*	MAX.	
Clock 1 Frequency	t_{CLK1}	5	—	2	—	—	2	MHz
	10	—	—	5	—	—	—	
Clock 2 Frequency	t_{CLK2}	5	—	4	—	—	4	MHz
	10	—	—	8	—	—	—	
Clock 1 Width	t_1	5	250	—	—	250	—	ns
	10	—	100	—	—	—	—	
Clock 2 Width	t_2	5	125	—	—	125	—	ns
	10	—	70	—	—	—	—	
Clock 1 to Clockout	t_{CL1}	5	—	1	1.7	—	1	μs
	10	—	0.3	0.5	—	—	—	
Clock 2 to Clockout	t_{CL2}	5	—	0.9	1.2	—	0.9	μs
	10	—	0.3	0.5	—	—	—	
$\overline{\text{Reset}}$ to Clockout	t_{CLR}	5	—	260	375	—	260	ns
	10	—	130	170	—	—	—	
OE Delay to Clockout	t_{OED}	5	—	110	150	—	110	ns
	10	—	40	70	—	—	—	
$\overline{\text{Reset}}$ Pulse Width	t_{RS}	5	—	120	160	—	120	ns
	10	—	60	90	—	—	—	
Data Setup to Clock 1	t_{DS}	5	—	0	20	—	0	ns
	10	—	0	10	—	—	—	
Data Hold to Clock 1	t_{DH}	5	—	75	100	—	75	ns
	10	—	50	80	—	—	—	
Data Setup to Strobe	t_{DSS}	5	—	0	30	—	0	ns
	10	—	0	30	—	—	—	
Data Hold to Strobe	t_{DHS}	5	—	50	100	—	50	ns
	10	—	40	60	—	—	—	

*Typical values are for $T_A = 25^\circ\text{C}$ and nominal voltages.

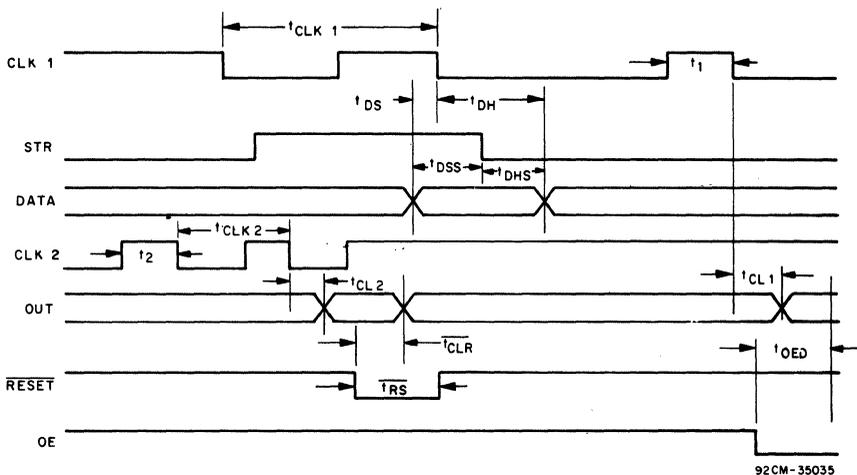
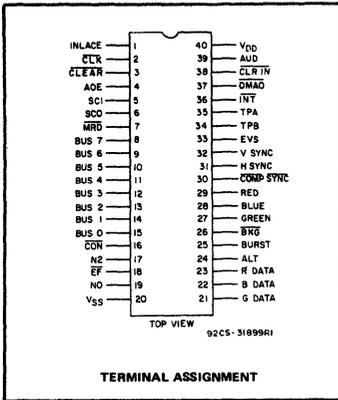


Fig. 6 — Timing diagram for the CDP1863 and CDP1863C.

Preliminary Data

CMOS PAL Compatible Color TV Interface



Features:

- Single chip contains circuitry for video, sync, RGB color, and programmable frequency for tone generation
- Programmable 1-of-8 dot colors plus 1-of-4 background colors
- Bit-mapped display with maximum resolution of 192 vertical x 64 horizontal
- Interlaced or non-interlaced displays
- Schmitt trigger clear input and output for power-on reset of CDP1800 system
- 1.75-MHz crystal operation

The RCA-CDP1864C is an LSI CMOS color or black and white PAL-compatible video controller designed for use in CDP1800 microprocessor systems. It interfaces directly with the 1800-series microprocessor as shown in Figs. 1 and 2. The DMA feature of these processors is used for direct data transfers of luminance information for display refresh. The INTERRUPT input and a flag line (EF1, EF2, EF3, or EF4) are used for handshaking.

The CDP1864C generates vertical sync, horizontal sync, and composite sync. These signals, combined with the

RED, BLUE, GREEN, BURST, and $\overline{\text{BKG}}$ signals, can be used to generate a composite video signal, or they can be used directly inside a TV set.

In addition to generating a bit-mapped video display the CDP1864C contains a programmable frequency generator designed to produce 256 tones that range from 107 Hz to 13672 Hz.

The CDP1864C is supplied in the 40-lead dual-in-line ceramic (D suffix) and plastic (E suffix) packages.

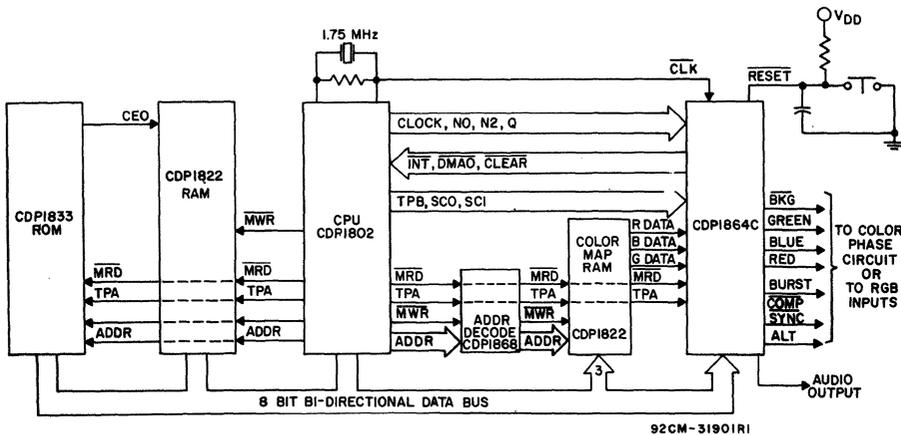


Fig. 1 — Typical color system.

RCA CMOS LSI Products

CDP1864C

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltage reference to V_{SS} Terminal)	-0.5 to +7 V
CDP1864C	-0.5 to $V_{DD} + 0.5$ V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to $V_{DD} + 0.5$ V
DC INPUT CURRENT, ANY ONE INPUT	± 10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For $T_A = -40$ to $+60^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +60$ to $+85^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at $12\text{ mW}/^\circ\text{C}$ to 200 mW
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE D)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE D)	Derate Linearly at $12\text{ mW}/^\circ\text{C}$ to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE}$ (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES, D, H	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E	-40 to $+85^\circ\text{C}$
STORAGE TEMPERATURE RANGE (T_{stg})	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ inch (1.59 ± 0.79 mm) from case for 10 s max.	$+265^\circ\text{C}$

OPERATING CONDITIONS at $T_A = \text{Full Package Temperature Range}$

For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	TYPICAL VALUES	UNITS
DC Operating-Voltage Range	—	4. to 6.5	V
Input Voltage Range	—	V_{SS} to V_{DD}	V
Maximum Input Pulse Rise or Fall Time, t_r, t_f	5	5	μs
Maximum Input Clock Frequency, f_{CL}	5	1.75	MHZ

STATIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$, $V_{DD} = 5\text{ V} \pm 5\%$

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS	
		CDP1864C				
		Min.	Typ.	Max.		
Quiescent Device Current, I_{DD}	V_O (V)	V_{IN} (V)	—	100	500	μA
Output Voltage:*						V
Low-Level, V_{OL}	—	0.5	—	0	0.1	
High-Level, V_{OH}	—	0.5	4.9	5	—	
Input Low Voltage, V_{IL}	0.5, 4.5	Any Input	—	—	1.5	mV
Input High Voltage, V_{IH}	0.5, 4.5		3.5	—	—	
Output Low (Sink) Current, I_{OL}	0.4	0.5	2	2.4	—	mA
Output High (Source) Current, I_{OH}	4.5	0.5	-1.6	-1.8	—	
Input Leakage Current, I_{IL}, I_{IH}	—	Any Input	—	± 0.1	± 1	μA
3-State Output Leakage Current, I_{OUT}	0.5	0.5	—	± 0.2	± 2	

* $I_O \leq 1\ \mu\text{A}$.

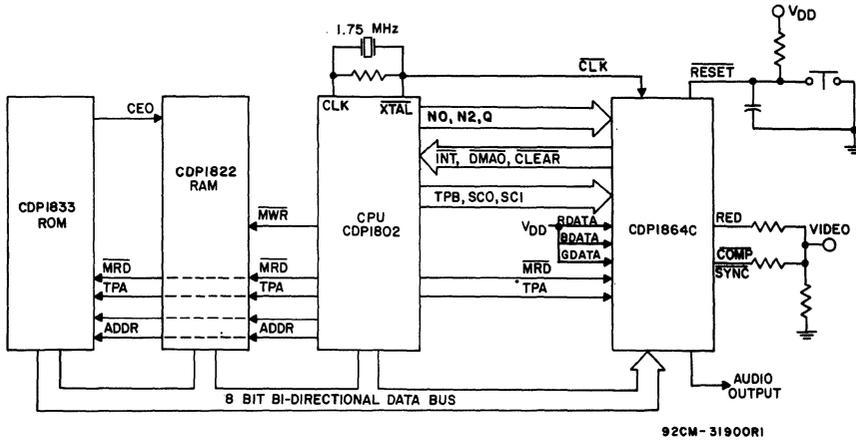


Fig. 2 — Typical black and white system.

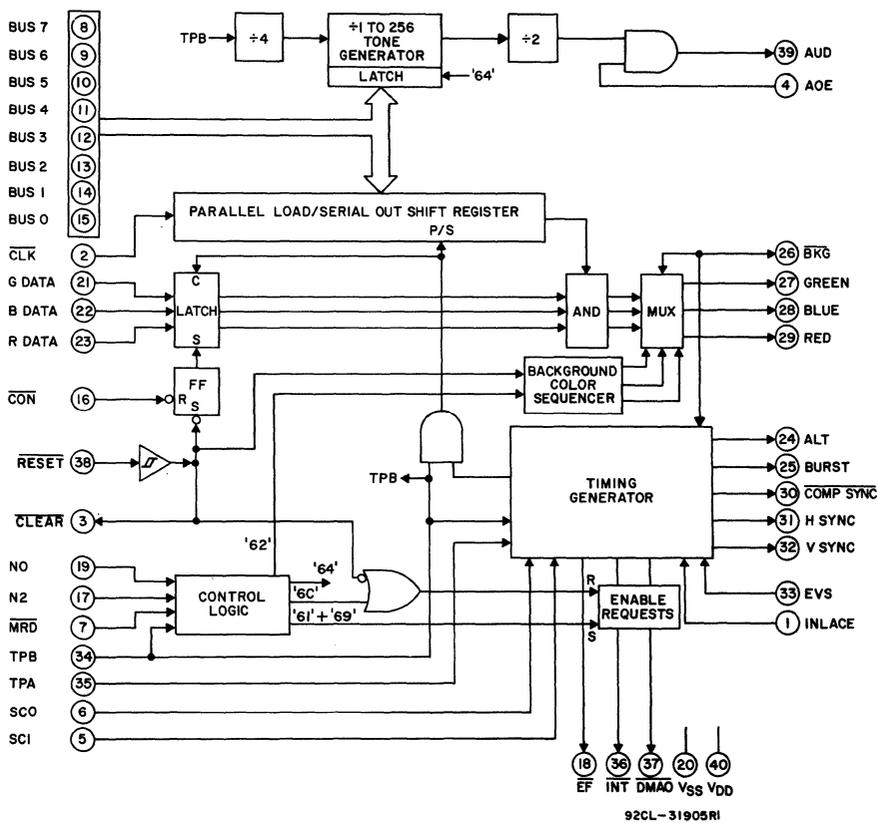


Fig. 3 — CDP1864C block diagram.

BUS 0 — BUS 7 (Inputs):

These inputs load the luminance information during the display interval, and the frequency generator divide byte when selected. They are connected to the DATA BUS.

CON — COLOR ON (Input):

A low level at this input enables the CDP1864 to begin loading color information from the RDATA, GDATA, and BDATA inputs. CON is connected to the gated MWR signal of the color memory.

N2 (Input):

This input is used in conjunction with MRD and TPB to load data into the tone generator latch (MRD•N2•TPB) and disable the generation of INTERRUPT and DMA requests by the CDP1864 (MRD•N2•TPB). For example, a 64 instruction would result in data being loaded into the tone-divider latch, while a 6C instruction would disable the INTERRUPT and DMA requests. N2 is connected to the N2 output of the 1800-series microprocessor.

EF — EXTERNAL FLAG OUT (Output):

This output is connected to a 1800-series microprocessor EF1 - EF4 inputs. It maintains software synchronization with the display. Two pulses per field are generated on this line, each of which is four horizontal lines wide. The first pulse begins four horizontal lines before the display, and the second pulse begins four horizontal lines prior to the end of the display. The second pulse is used to indicate to the microprocessor that the display is ending.

NO (Input):

This input is used in conjunction with MRD and TPB to step the background color (MRD•NO•TPB) and to enable the INTERRUPT and DMA requests (NO•TPB). For example, a 61 instruction would step the background color, and a 61 or 69 instruction would enable the INTERRUPT and DMA requests. NO is connected to the NO output of the 1800-series microprocessor.

V_{SS}:

Negative supply voltage.

GDATA, BDATA, RDATA — RED, GREEN, and BLUE DATA (Inputs):

These inputs carry color information from the color RAM. The data on these lines are latched concurrent with the latching of the luminance information from the data bus during the display interval if the CON input has gone low since reset.

ALT — ALTERNATE (Output):

This output toggles at each horizontal sync time and is used to perform the phase alternation.

BURST (Output):

This output applies a 4.57 us pulse to each horizontal sync back-porch (except for 24 lines during vertical sync when it is blanked) which gates in the color burst signal.

BKG — BACKGROUND (Output):

This CMOS logic level output indicates that the color selected by the RGB outputs is due to background color select rather than a one bit in a display luminance byte. BKG may be used to lower the luminance of the background color so that the same color may be used for display of data. This output is blanked (held high) during horizontal and vertical blanking.

GREEN, BLUE, RED (Outputs):

These CMOS logic level outputs are used either directly in the TV to generate the selected colors, or indirectly to generate a composite video signal. These outputs are used to indicate the selected color for an "on" spot or the background color for an "off" spot.

COMP SYNC — COMPOSITE SYNC (Output):

This output is the composite horizontal and serrated vertical sync signal.

HSYNC — HORIZONTAL SYNC (Output):

This output is a separate horizontal sync signal.

EVS — EXTERNAL VERTICAL SYNC (Input):

A high level at this input sets the line counters to the vertical sync state.

TPB — TIMING PULSE B (Input):

This input is connected to the TPB output of the 1800-series microprocessor. It is used for strobing the MRD and N lines, for horizontal line timing, and as the input to the tone generator.

TPA — TIMING PULSE A (Input):

This input is connected to the TPA output of the 1800-series microprocessor. It is used for horizontal line timing.

INT — INTERRUPT (Output):

This output is connected to the INT input of the 1800-series microprocessor. One interrupt request is issued per field. The request is issued two horizontal lines before the display interval, and the signal remains active for two horizontal lines.

DMAO — DMA OUT REQUEST (Output):

This output is connected to the DMAOUT input of the 1800-series microprocessor. During the display interval the CDP1864 issues this request for 6 machine cycles during the center of each horizontal line (each line time is 14 machine cycles).

RESET — RESET IN

A low level at this input resets the CDP1864 and generates a low on the CLR_{OUT} output. The requests and the loading of color information are inhibited by reset. These remain inhibited until enabled by the appropriate signals. The line counters and horizontal counters are also held reset while RESET is low. The Schmitt trigger circuit at this input allows the use of an RC circuit for power-on reset and reset debounce.

AUD — AUDIO OUT:

This is the output of the programmable frequency generator.

V_{DD}:

Positive supply voltage.

CDP1864C

CIRCUIT OPERATION

The CDP1864C consists of four major sections: a timing generator that produces the necessary signals for video interface, a parallel-in/serial out shift register for dot generation, a tone generator for one of 256 frequencies, and control logic for software control of the first three sections (see Fig. 3). In a typical CDP1800 system, control of the CDP1864C is accomplished with I/O commands as shown in Fig. 5.

The CDP1864C display is a bit-mapped, color or black and white display with a maximum resolution of 192 lines vertically and 64 dots (eight 8-bit bytes) horizontally. This resolution, which requires 1.5 Kbytes of refresh RAM, is seldom used because of the poor aspect ratio of the resultant picture element. An approximately square picture element is obtained by repeating each horizontal line 6 times (this is done in software by the CPU) for a 32-row by 64-dot display. This lower resolution display requires 256 bytes of refresh RAM.

The CDP1864C generates both composite and separate horizontal and vertical sync, RED, BLUE, GREEN, BURST, and BKG signals. These signals may be used directly (inside the TV), or they may be used to generate the composite video signal. The sync signals generate either a 625 line-per-frame interlaced display or a 312 line-per-frame non-interlaced display. This is selectable by connecting the INTERLACE input to either V_{DD} or GND.

The video refresh is accomplished via the DMA channel of the microprocessor, and synchronization is provided by INT, EF, SC0, and SC1. The EF signal goes low 4 horizontal lines prior to the start of display and again 4 lines prior to the end of the display. This signal alone can be used by the CPU to initialize R(O) for DMA refresh. Alternatively, the INT, which goes low 2 lines prior to the start of the display, may be used to enter an interrupt routine that initializes R(O), and the EF signal can be used to indicate the end of the display. The combination of INT and EF allows for an interrupt routine to oversee DMA refresh and repeat horizontal lines for configurations with less than the maximum 192-line resolution. EF can be sampled to detect the end of the display and cause a return to the main program from the interrupt routine.

SC1 and SC0 are used to provide CDP1864C-to-CPU synchronization for a jitter-free display. During every horizontal sync the CDP1864C samples SC0 and SC1 for SC0 = 1 and SC1 = 0 (CDP1800 execute state). Detection of a fetch cycle causes the CDP1864C to skip cycles to attain synchronization. Once in lock the system will remain locked if: (1) no 3-cycle instructions (e.g. NOP) are executed during

the display (three 2-cycle instructions are executed each horizontal line); (2) an even number of cycles is performed between frames (easiest to do by avoiding 3-cycle instructions); or (3) exactly 29 cycles, beginning with a fetch and ending with an execute, are completed between the S3 interrupt response of the cpu and the first DMA in systems using INT. The 29 cycles of interrupt should consist of an early 3-cycle instruction and thirteen 2-cycle instructions (or equivalent). Fig. 5 is an example of an interrupt routine for a 64 by 32 picture element display (each horizontal line is repeated 6 times).

Reset disables the color, control, INT, and DMA requests. A 61 or 69 instruction enables the requests, and a 6C instruction disables them (see Fig. 5). Color is enabled by CON, which is normally connected to the gated MWR signal of the color RAM.

The background color is program-selected to be either blue, black, green or red. The initial default is blue. The color selected is changed by a 61 instruction (see Fig. 5). This condition causes the color to step to the next color in the order shown above. From red it steps to blue. The BKG output may be used to lower the luminance of the color when it is background. This would, for instance, enable a blue spot to be used on a blue background and still be visible. The BKG signal and RGB outputs are internally blanked during the horizontal and vertical retrace.

The CDP1864C also contains a programmable tone generator designed to produce 256 frequencies. The frequency input to this generator is the TPB input (TPB frequency = 1.75 MHz ÷ 8 = 218.75 kHz). This frequency is further reduced by a divide-by-4 predivider, an 8-bit programmable up-counter, and a divide-by-2 output stage. The programmable up-counter is reloaded automatically from the 8-bit tone generator latch each time it reaches the terminal count. The tone generator latch is loaded by the CPU from the data bus during a 64 output instruction (see Fig. 5).

An AUDIO OUTPUT ENABLE (AOE) terminal is also provided. When this terminal is high the output of the generator (AUDIO OUT) is allowed to toggle freely. When this terminal is low the output is held low. AUDIO OUT may be connected to the Q line of the 1800-series microprocessor. A low on the reset sets the 8-bit latch to a default state of 35 hex and resets the programmable counter. When reset is released a frequency output of 506 Hz will be generated until a new value is loaded into the latch. The frequencies generated from the input to the 8-bit tone generator latch can be computed by:

$$f = \frac{27343.75}{(\text{Hex Code} + 1)_{10}} \text{ Hz.}$$

CONTROL LINE TRUTH TABLE

MRD	N2	N0	TPB	OP CODE*	OPERATION
X	0	0	X	—	NO ACTION
X	0	1	1	61 or 69	ENABLE REQUESTS
0	0	1	1	61	STEP BACKGROUND COLOR
0	1	0	1	64	LOAD TONE GENERATOR LATCH
1	1	0	1	6C	DISABLE REQUESTS
X	1	1	X	—	ILLEGAL COMMAND
X	X	X	0	—	NO ACTION

*The OP CODE column is given assuming that N1 = 0. It is actually a DON'T CARE because N1 from the microprocessor is not connected to the CDP1864C.

Machine Code	Assembly Language	Comments
72	INTRET: LDXA	.. RESTORE D
70	RET	.. RETURN
C4	INT : NOP	.. 3 CYC. INSTR. USED
		.. FOR PGM. SYNC
22	DEC R2	.. R2 IS STACK PTR
78	SAV	.. T → STACK
22	DEC R2	
52	STR R2	.. D → STACK
F8-B0	A.1 (DISMEM) → RO.1	.. LOAD RO WITH
F8-A0	A.0 (DISMEM) → RO.0	.. START.ADDR.OF DISP. MEM
C4, C4	NOP; NOP	.. NOPS USED FOR SYNC
E2	DISP : SEX2	
80]	GLO RO	.. LINE START ADDR. → D
E2	SEX2	.. NOP
20	DEC RO	.. RESET RO.1 IF PASS PG
A0]	PLO RO	.. LINE START ADDR. → RO.0
E2	SEX2	.. NOP
20	DEC RO	.. RESET RO.1 IF PASS PG
A0]	PLO RO	.. LINE START ADDR. → RO.0
E2	SEX2	.. NOP
20	DEC RO	.. RESET RO.1 IF PASS PG
A0]	PLO RO	.. LINE START ADDR. → RO.0
E2	SEX2	.. NOP
20	DEC RO	.. RESET RO.1 IF PASS PG
A0]	PLO RO	.. LINE START ADDR. → RO.0
E2	SEX2	.. NOP
20	DEC RO	.. RESET RO.1 IF PASS PG
A0]	PLO RO	.. REPEATS SAME LINE
3C	BN1 DISP	.. LOOPS 32 TIMES
30	BR INTRET	.. END OF DISPLAY

Fig. 5 — Interrupt routine for a 64 x 32 display.

OPERATING AND HANDLING CONSIDERATIONS

1. Handling

All inputs and outputs of RCA CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in ICAN-6525 "Guide to Better Handling and Operation of CMOS integrated Circuits."

2. Operating

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause $V_{DD}-V_{SS}$ to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS} . Input currents must not exceed 10 mA even when the power supply is off.

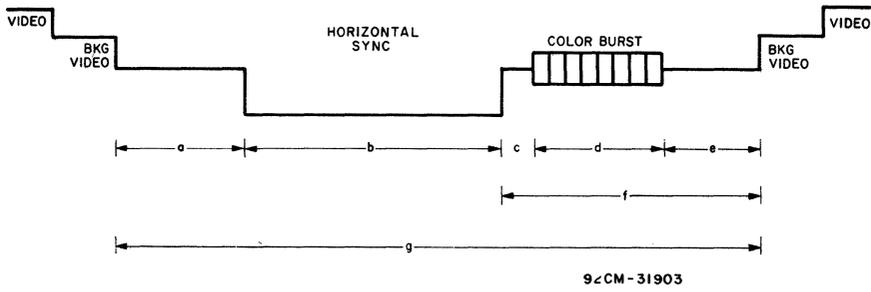
Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS} , whichever is appropriate.

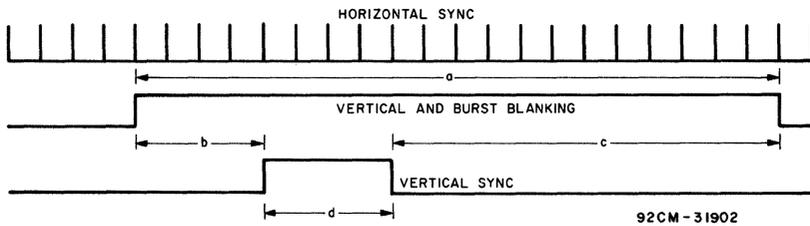
Output Short Circuits

Shorting of outputs to V_{DD} or V_{SS} may damage CMOS devices by exceeding the maximum device dissipation.

RCA CMOS LSI Products
CDP1864C



	PAL STANDARD	CDP1864
a	1.55 μ s	3.14 μ s
b	4.7 \pm 0.1 μ s	4.57 μ s
c	900 ns \pm 100 ns	857 ns
d	2.25 ns \pm 0.25 μ s	2.57 μ s
e	2.6 μ s	2.0 μ s
f	5.8 μ s	5.43 μ s
g	12.05 μ s	13.14 μ s
HORZ. FREQ.	15625 Hz	15625 Hz



	PAL STANDARD	CDP1864
a	25 H	24 H
b	2.5 H	4 H
c	20 H	12 H
d	2.5 H	4 H
Burst Blanking	9 H	24 H
Vertical freq. (interlaced)	50 Hz	50
Vertical freq. (non-interlaced)	50 Hz	50.08 Hz

Fig. 6 — Timing diagrams.

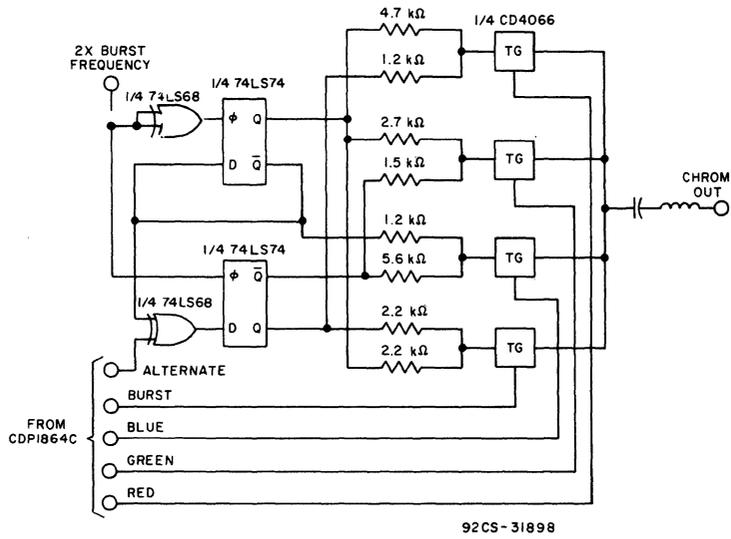


Fig. 7 — Typical color signal generator.

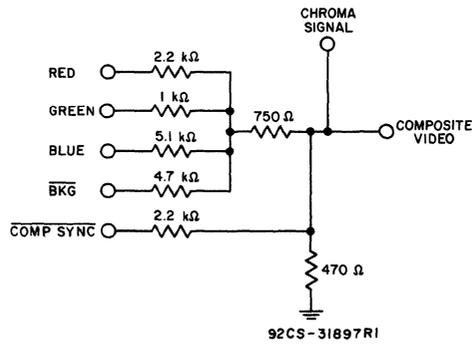
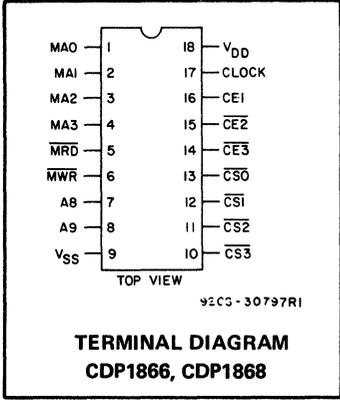


Fig. 8 — Typical composite video network.

CDP1866, CDP1866C, CDP1867, CDP1867C, CDP1868, CDP1868C

CMOS 4-Bit Latch and Decoder Memory Interfaces



Features:

- Performs memory address latch and decoder functions multiplexed or non-multiplexed
- Interfaces directly with all CDP1800 family CPUs

The RCA-CDP1866, CDP1867, and CDP1868 are CMOS 4-bit memory latch and decoder circuits intended for use in CDP1800 series microprocessor systems. They can interface directly with the multiplexed address bus of this system at maximum clock frequency, and up to eight 4096-bit random-access memories to provide a 4096-byte RAM system. All the necessary chip selects are provided as outputs along with additional enable inputs so that in larger memory systems, the 9-chip 4096-byte blocks can be readily accessed.

These devices are also compatible with non-multiplexed address bus microprocessors.

By connecting the clock input to V_{DD} , the latches are in the

data-following mode and the decoded outputs can be used in general-purpose memory-system applications.

The CDP1866 and CDP1868 are intended for use with 1024-word RAMs and are identical except that in the CDP1868, CE1 and CE2 are latched and CS2 is valid on MWR only. This allows the CDP1868 to be used in a color display system with the CDP1861 and CDP1862 (see Fig. 9). The CDP1867 is intended for use with 4096-word RAMs.

The CDP1866, CDP1867, and CDP1868 are supplied in an 18-lead hermetic dual-in-line ceramic package (D suffix) and an 18-lead plastic package (E suffix). The CDP1866C, CDP1867C, and the CDP1868C are available in chip form (H suffix).

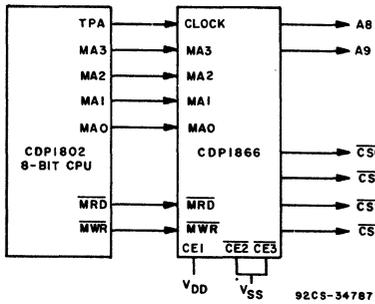
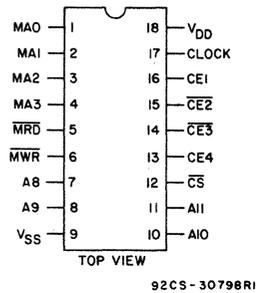


Fig. 1 - CDP1866 used as a high-order address latch decoder.



TERMINAL DIAGRAM CDP1867

CDP1866, CDP1866C, CDP1867, CDP1867C, CDP1868, CDP1868C

OPERATING CONDITIONS at T_A = Full Package-Temperature Range.

For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1866, CDP1867, CDP1868		CDP1866C, CDP1867C, CDP1868C		
	Min.	Max.	Min.	Max.	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	

STATIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} \pm 5\%$, Except as noted

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	CDP1866, CDP1867, CDP1868			CDP1866C, CDP1867C, CDP1868C			
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device Current I_{DD}	— —	0,5 0,10	5 10	— —	1 10	10 100	— —	5 —	50 —	μA
Output Low Drive (Sink) Current I_{OL}	0.4 0.5	0,5 0,10	5 10	1.6 2.6	3.2 5.2	— —	1.6 —	3.2 —	— —	mA
Output High Drive (Source) Current I_{OH}	4.6 9.5	0,5 0,10	5 10	-1.15 -2.6	-2.3 -5.2	— —	-1.15 —	-2.3 —	— —	
Output Voltage Low-Level $V_{OL}\ddagger$	— —	0,5 0,10	5 10	— —	0 0	0.1 0.1	— —	0 —	0.1 —	V
Output Voltage High-Level $V_{OH}\ddagger$	— —	0,5 0,10	5 10	4.9 9.9	5 10	— —	4.9 —	5 —	— —	
Input Low Voltage V_{IL}	0.5,4.5 0.5,9.5	— —	5 10	— —	— —	1.5 3	— —	— —	1.5 —	
Input High Voltage V_{IH}	0.5,4.5 0.5,9.5	— —	5 10	3.5 7	— —	— —	3.5 —	— —	— —	
Input Leakage Current I_{IN}	Any Input	0,5 0,10	5 10	— —	— —	± 1 ± 2	— —	— —	± 1 —	μA
Input Capacitance C_{IN}	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance C_{OUT}	—	—	—	—	10	15	—	10	15	
Operating Device Current $I_{DD1\Delta}$	0,5 0,10	0,5 0,10	5 10	— —	50 150	100 300	— —	50 —	100 —	μA
Minimum Data Retention Voltage V_{DR}	$V_{DD} = V_{DR}$			—	2	2.4	—	2	2.4	V
Data Retention Current I_{DR}	$V_{DD} = 2.4\text{ V}$			—	0.01	1	—	0.5	5	μA

*Typical values are for $T_A = 25^\circ\text{C}$. $\ddagger I_{OL} = I_{OH} = 1\ \mu\text{A}$.

Δ Operating current is measured at 200 kHz for $V_{DD} = 5\text{ V}$ and 400 kHz for $V_{DD} = 10\text{ V}$, with open outputs (worst-case frequencies for CDP1802A system operating at maximum speed of 3.2 MHz).

RCA CMOS LSI Products

CDP1866, CDP1866C, CDP1867, CDP1867C, CDP1868, CDP1868C

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltage referenced to V_{SS} Terminal)

CDP1866, CDP1867, CDP1868	-0.5 to 11 V
CDP1866C, CDP1867C, CDP1868C	-0.5 to 7 V

INPUT VOLTAGE RANGE, ALL INPUTS -0.5 to $V_{DD} + 0.5$ V

DC INPUT CURRENT, ANY ONE INPUT ± 10 mA

POWER DISSIPATION PER PACKAGE (P_D):

For $T_A = -40$ to $+60^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +60$ to $+85^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 12 mW/ $^\circ\text{C}$ to 200 mW
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE D)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE D)	Derate Linearly at 12 mW/ $^\circ\text{C}$ to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$ 40 mW

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPE D	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E	-65 to $+150^\circ\text{C}$

STORAGE TEMPERATURE RANGE (T_{stg}) -65 to $+150^\circ\text{C}$

LEAD TEMPERATURE (DURING SOLDERING):

At distance $1/16 \pm 1/32$ inch (1.59 ± 0.79 mm) from case for 10 s max. $+265^\circ\text{C}$

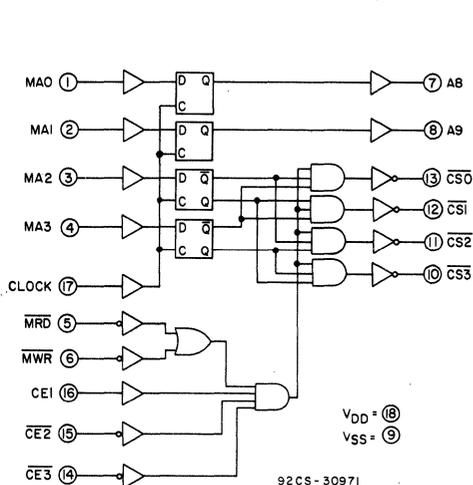


Fig. 2 - Functional diagram for the CDP1866.

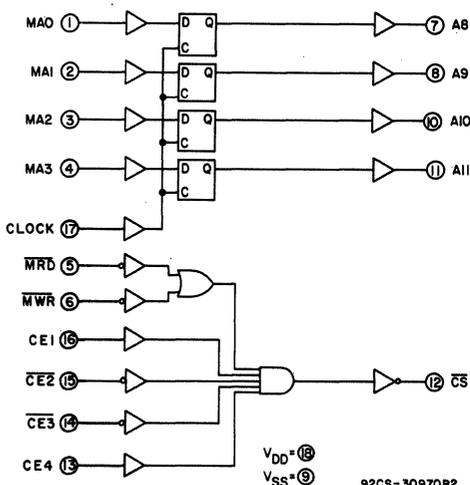


Fig. 3 - Functional diagram for the CDP1867.

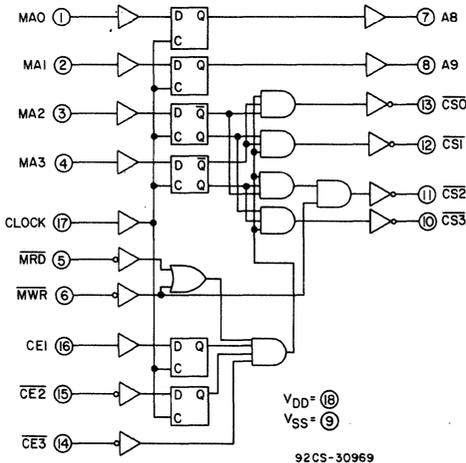
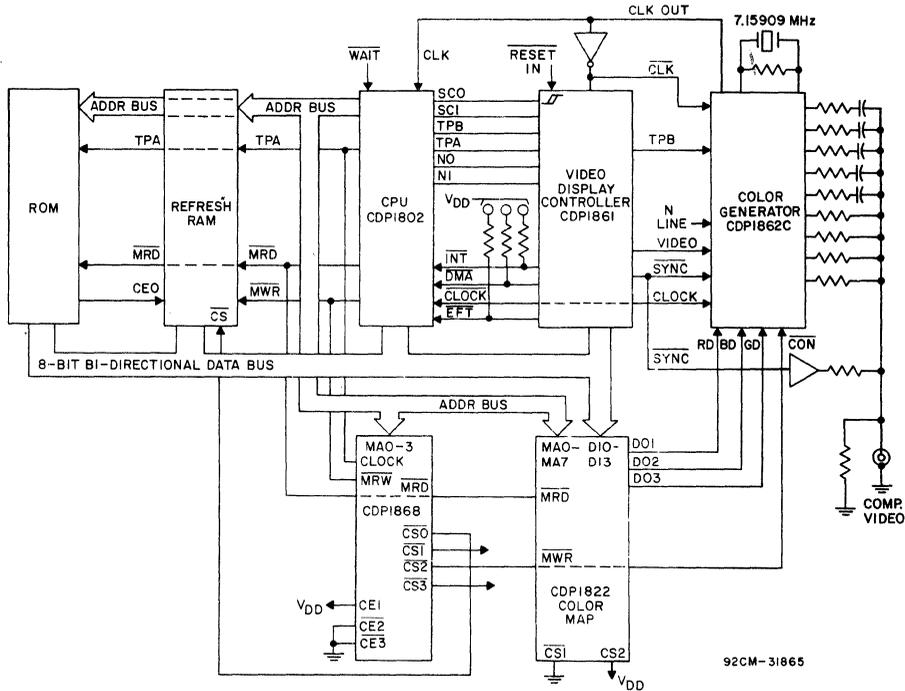


Fig. 4 - Functional diagram for the CDP1868.



CHIP SELECT	ADDRESS
CS0	0000 - 03FF
CS1	0400 - 07FF
CS2	0800 - 0BFF
CS3	0C00 - 0FFF

Fig. 6 - Typical color display system using the CDP1868.

The CDP1868 can be used in a color display system to write to the refresh RAM and the color map RAM at different address locations, as shown in Fig. 9. Both the refresh RAM and the color map RAM are read from the same address. The purpose of reading from the same address is that when a byte of data from the refresh RAM is sent to the video display controller (CDP1861), an additional 3 bits of color information are needed from the color map RAM for the color generator (CDP1862). In Fig. 9, the bit display data are written into the refresh RAM at 0000-00FF. The color display data are written into the color map RAM at locations 0800-08FF. Both are read at locations 0000-00FF.

CDP1866, CDP1866C, CDP1867, CDP1867C, CDP1868, CDP1868C

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} \pm 5\%$, $t_r = 20$ ns,
 $V_{IH} = 0.7 V_{DD}$, $V_{IL} = 0.3 V_{DD}$, $C_L = 100$ pF. See Fig. 8

CHARACTERISTIC	V_{DD} (V)	LIMITS						UNITS
		CDP1866			CDP1866C			
		Min.	Typ.*	Max.Δ	Min.	Typ.*	Max.Δ	
Minimum Setup Time, Memory Address to CLOCK, t_{MACL}	5 10	—	50 25	75 40	—	50 —	75 —	ns
Minimum Hold Time, Memory Address After CLOCK, t_{CLMA}	5 10	—	50 25	75 40	—	50 —	75 —	
Minimum CLOCK Pulse Width t_{CLCL}	5 10	—	50 25	75 40	—	50 —	75 —	
Propagation Delay Times:								
Chip Enable to Chip Select, t_{CECS}	5 10	—	150 75	225 125	—	150 —	225 —	
MRD or MRW to Chip Select, t_{MCS}	5 10	—	125 65	200 125	—	125 —	200 —	
CLOCK to Chip Select, t_{CLCS}	5 10	—	175 90	275 150	—	175 —	275 —	
CLOCK to Address, t_{CLA}	5 10	—	125 65	200 125	—	125 —	200 —	
Memory Address to Chip Select, t_{MACS}	5 10	—	150 75	225 125	—	150 —	225 —	
Memory Address to Address, t_{MAA}	5 10	—	80 40	125 60	—	80 —	125 —	

*Typical values are for $T_A = 25^\circ\text{C}$.
 ΔMaximum limits of minimum characteristics are the values above which all devices function.

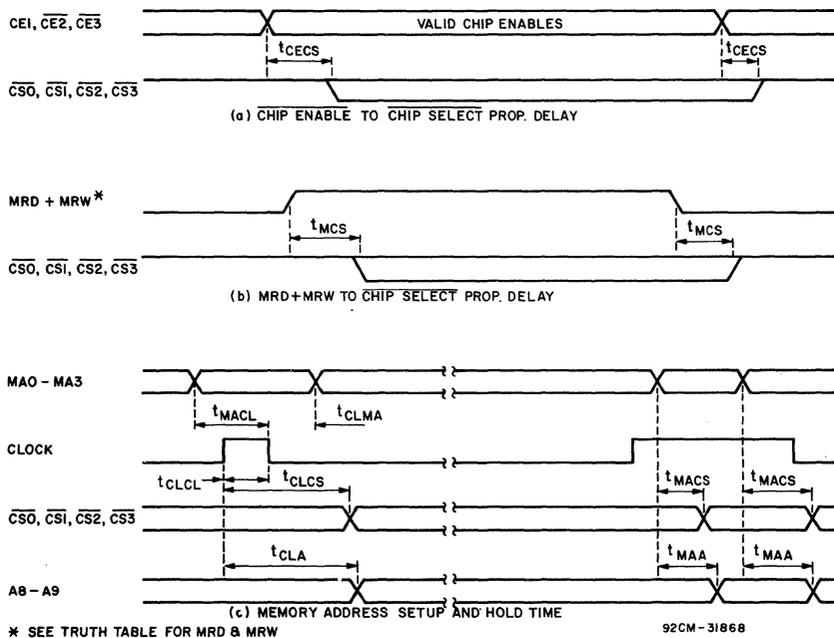


Fig. 8 - CDP1866 timing waveforms.

CDP1866, CDP1866C, CDP1867, CDP1867C, CDP1868, CDP1868C

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} \pm 5\%$, $t_r, t_f = 20$ ns,
 $V_{IH} = 0.7 V_{DD}$, $V_{IL} = 0.3 V_{DD}$, $C_L = 100$ pF. See Fig. 9

CHARACTERISTIC	V_{DD} (V)	LIMITS						UNITS	
		CDP1867			CDP1867C				
		Min.	Typ.*	Max.Δ	Min.	Typ.*	Max.Δ		
Minimum Setup Time, Memory Address to CLOCK,	t_{MACL}	5	—	50	75	—	50	75	ns
Minimum Hold Time, Memory Address After CLOCK,	t_{CLMA}	10	—	25	40	—	—	—	
Minimum CLOCK Pulse Width	t_{CLCL}	5	—	50	75	—	50	75	
		10	—	25	40	—	—	—	
Propagation Delay Times:									
Chip Enable to Chip Select,	t_{CECS}	5	—	100	150	—	100	150	
MRD or MRW to Chip Select,	t_{MCS}	10	—	80	125	—	80	125	
CLOCK to Address,	t_{CLA}	5	—	125	200	—	125	200	
		10	—	65	100	—	—	—	
Memory Address to Address,	t_{MAA}	5	—	75	125	—	75	125	
		10	—	40	60	—	—	—	

*Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .
 ΔMaximum limits of minimum characteristics are the values above which all devices function.

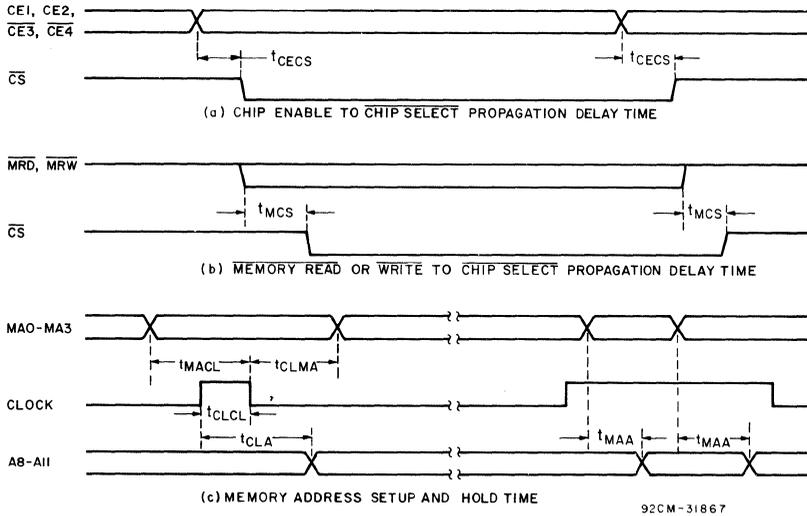


Fig. 9 - CDP1867 timing waveforms.

CDP1866, CDP1866C, CDP1867, CDP1867C, CDP1868, CDP1868C

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} \pm 5\%$, $t_r = 20$ ns,
 $V_{IH} = 0.7 V_{DD}$, $V_{IL} = 0.3 V_{DD}$, $C_L = 100$ pF. See Fig. 10

CHARACTERISTIC	V _{DD} (V)	LIMITS						UNITS
		CDP1868			CDP1868C			
		Min.	Typ.*	Max.Δ	Min.	Typ.*	Max.Δ	
Minimum Setup Times:								
Chip Enable to CLOCK,	5	—	50	75	—	50	75	ns
t_{CECL}	10	—	25	40	—	—	—	
Memory Address to CLOCK,	5	—	50	75	—	50	75	
t_{MACL}	10	—	25	40	—	—	—	
Minimum Hold Times:								
Chip Enable After CLOCK,	5	—	50	75	—	50	75	
t_{CLCE}	10	—	25	40	—	—	—	
Memory Address After CLOCK,	5	—	50	75	—	50	75	
t_{CLMA}	10	—	25	40	—	—	—	
Minimum CLOCK Pulse Width,	5	—	50	75	—	50	75	
t_{CLCL}	10	—	25	40	—	—	—	
Propagation Delay Times:								
CLOCK to Chip Select,	5	—	175	275	—	175	275	
t_{CLCS}	10	—	90	150	—	—	—	
Chip Enable to Chip Select,	5	—	150	225	—	150	225	
t_{CECS}	10	—	75	125	—	—	—	
Chip Enable 3 to Chip Select,	5	—	150	225	—	150	225	
t_{C3CS}	10	—	75	125	—	—	—	
MRD or MRW to Chip Select,	5	—	125	200	—	125	200	
t_{MCS}	10	—	65	100	—	—	—	
CLOCK to Address,	5	—	125	200	—	125	200	
t_{CLA}	10	—	65	100	—	—	—	
Memory Address to Chip Select,	5	—	125	200	—	125	200	
t_{MACS}	10	—	65	100	—	—	—	
Memory Address to Address,	5	—	80	120	—	80	120	
t_{MAA}	10	—	40	60	—	—	—	

•Typical values are for $T_A = 25^\circ\text{C}$ and nominal.
 ΔMaximum limits of minimum characteristics are the values above which all devices function.

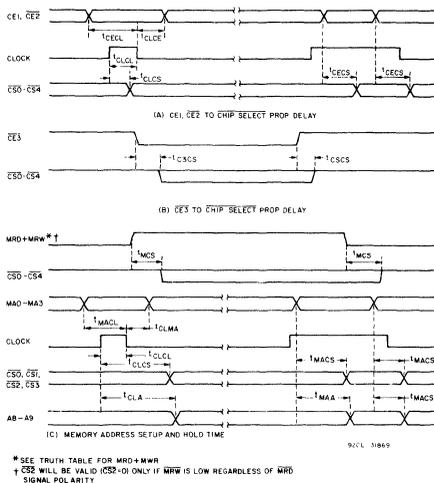
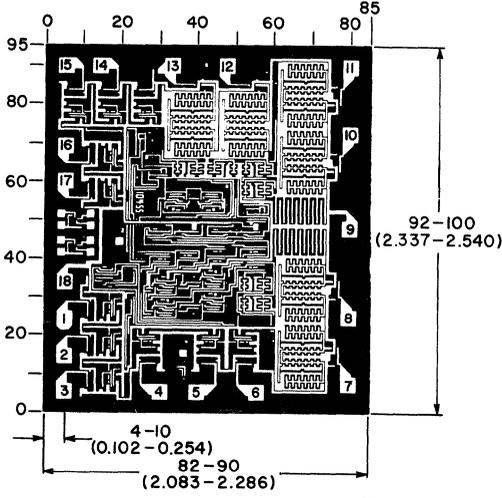


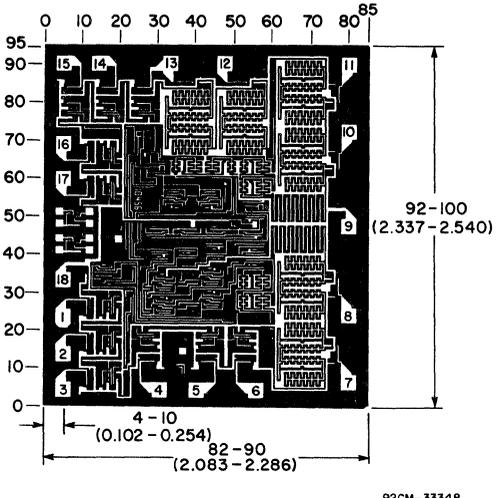
Fig. 10 - CDP1868 timing waveforms.

RCA CMOS LSI Products

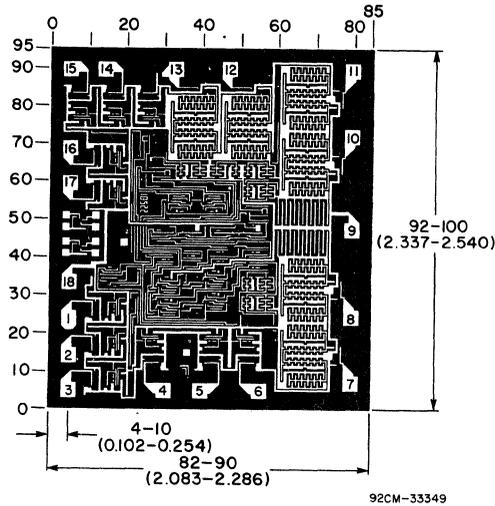
CDP1866, CDP1866C, CDP1867, CDP1867C, CDP1868, CDP1868C



Dimensions and pad layout for CDP1866CH.



Dimensions and pad layout for CDP1867CH.



Dimensions and pad layout for CDP1868CH.

Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

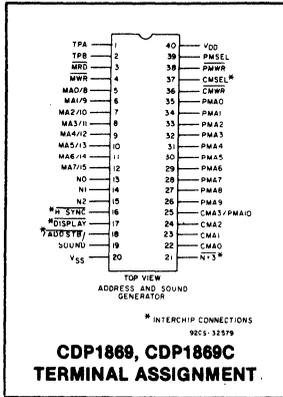
The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

CDP1869, CDP1869C, CDP1870, CDP1870C, CDP1876, CDP1876C

COS/MOS Video Interface System

Features:

- CMOS technology (C²L)
 - Directly interfaces with CDP1800 series microprocessors
 - DOT frequency = 5.67 MHz (PAL = 5.626 MHz). Produces maximum feasible resolution for RF (antenna) input
 - CPU clock independent (1/2 DOT rate provided)
 - CPU not involved in screen refresh
- Produces extremely low chip-count systems for games and/or "intelligent" terminals
 - Graphics and motion through character selection or bit map in character memory
 - Up to 256 different characters
 - Character memory may be any combination of ROM or RAM, allowing modification of characters and graphics
 - Programmable for 24 rows x 40 char/row or 12 rows x 20 char/row
 - 6 x 8 or 6 x 16 char. matrix (6 x 9 for PAL)
 - Character generation approach minimizes memory
 - PAL and NTSC compatible
 - Page memory is accessed as extension of CPU memory during non-display time

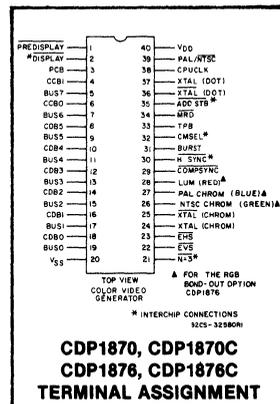


The RCA-CDP1869 and CDP1870 video interface system is designed for use in CDP1800-Series Microprocessor systems. It consists of the CDP1869C address and sound generator and the CDP1870C color video generator. These two LSI COS/MOS circuits interface directly with the CDP1802 or CDP1804 to simplify control and minimize external components. (See Fig. 1.)

The VIS offers a variety of formats for the display and modification of data under software control, with either NTSC or PAL compatible output signals. The display device can be a video monitor or a standard TV receiver with an RF modulator. Composite sync, luminance, and chrominance are combined externally to form a single system-output. (With the RGB Bond-Out option (CDP1876), Red, Green, and Blue outputs are provided to drive the CRT color amplifiers directly.) External sync inputs are also provided to allow picture overlays in existing TV chassis.

A sound output provides white noise and eight octaves of programmable tones. The output amplitude is variable in 16 steps from 0 V to 0.78 V_{DD}. This output is particularly useful in video game applications.

The CPU is clock independent of the VIS and is not involved in screen refresh, although a CPU clock output (1/2 DOT rate) is provided. At this clock rate 787 instructions (1080 for PAL) can be executed during non-display time. PREDISPLAY provides synchronization between the CPU



CDP1869, CDP1869C, CDP1870, CDP1870C, CDP1876, CDP1876C

Features: (cont'd)

- Composite sync, composite luminance, and composite chrominance outputs
- Programmable background color
- Programmable color format control allowing several modes for high resolution color
- Hardware scroll capability
- Audio generator (576 selectable tones covering 8 octaves) and white noise generator.
- Both tones and white noise can be enveloped from 0 to 0.78 V_{DD} in 16 steps
- External horizontal and vertical sync inputs allow for integration into existing chassis for character-on-picture overlays
- Teletext compatible format
- RGB bond-out option available (CDP1876)

and the VIS. The system configurations for the CDP1869/CDP1870 VIS are almost unlimited due to:

PAGE MEMORY

- 20 Characters x 12 Lines—Requires 240 Bytes of RAM
- 40 Characters x 24 Lines—Requires 960 Bytes of RAM

Character Memory—Can be RAM or ROM

- 32 Different (or any Combination of) Characters—Requires 256 Bytes (NTSC)
- 64 Different Characters—Requires 512 Bytes (NTSC)
- 128 Different Characters—Requires 1024 Bytes (NTSC)
- 256 Different Characters—Requires 2048 Bytes (NTSC)

Character memory requirements for PAL are the same as NTSC in most alphanumeric applications, but are 12.5% higher for graphics applications due to the larger character matrix (6x9) used for PAL.

The CDP1869 and CDP1869C are functionally identical. They differ in that the CDP1869 has an operating voltage range of 4 to 10.5 volts and the CDP1869C has an operating voltage range of 4 to 6.5 volts. The CDP1870 differs from the

CDP1870C in the same manner. All are supplied in 40-lead hermetic dual-in-line ceramic packages (D suffix) and in 40-lead dual-in-line plastic packages (E suffix).

Color

Color information may be stored in the two extra bits in each character byte (characters are only six dots wide), providing a choice of one of four colors for each character. With 128 different characters, only seven bits are required in the page memory and the eighth bit expands color to eight colors.

Graphics and Motion

Graphics and motion may be accomplished with two basic techniques. The first is by character selection. In this approach the desired graphics and motion symbols are stored in ROM or RAM. In a system where the character memory is all ROM, all the possible required positions within a character space are stored in the ROM. Graphics and motion are accomplished by selecting the appropriate one for each screen position. If the character memory is RAM then not all combinations need be stored in the character memory since they can be modified as required during operation.

The second technique is used for more sophisticated motion. In this technique a block of characters in the RAM character memory is treated as a continuous sur-

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})	
(Voltage referenced to V_{SS} Terminal)	
CDP1869, CDP1870, CDP1876	—0.5 to +11 V
CDP1869C, CDP1870C, CDP1876C	—0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS	
	—0.5 to V_{DD} + 0.5 V
DC INPUT CURRENT, ANY ONE INPUT	
	± 10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = —40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = —55 to +100°C (PACKAGE TYPE D)	500 mW
For T_A = +100 to 125°C (PACKAGE TYPE D)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE D	—55 to +125°C
PACKAGE TYPE E	—40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	
	—65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+ 265°C

CDP1869, CDP1869C, CDP1870, CDP1870C, CDP1876, CDP1876C

face. These characters are placed in adjacent locations on the screen to provide a background. The object is moved through this background using a bit map approach. As the object approaches the "edge" of the characters as selected on the screen, the background is moved. For example, if the object approaches the

edge of the last background character on the left, then the background characters on the right are moved to the left side via the page memory. Thus as the object moves through these background characters (as a continuous surface) it moves across the screen.

RECOMMENDED CONDITIONS at $T_A = 25^\circ\text{C}$ Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		CDP1869 CDP1870		CDP1869C CDP1870C		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (At $T_A =$ Full Package-Temperature Range)	—	4	10.5	4	6.5	V
Input Voltage Range	—	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V
Input Signal Rise or Fall Time, t_r, t_f	5	—	5	—	5	μs
	10	—	5	—	—	
Clock Input Frequency, f_{CL}	5,10	7.15909(8.867236-PAL)				MHz

STATIC CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, Except as noted

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	CDP1869 CDP1870			CDP1869C CDP1870C			
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device Current, I_L	—	0,5	5	—	100	500	—	100	500	μA
	—	0,10	10	—	200	1000	—	—	—	
Output Low Drive (Sink) Current, I_{OL} (Except XTAL)	0,4	0,5	5	2	2,4	—	2	2,4	—	mA
	0,5	0,10	10	4	4,8	—	—	—	—	
XTAL Output, I_{OL}	0,4	5	5	75	150	—	75	150	—	μA
	0,5	10	10	150	300	—	—	—	—	
Output High Drive (Source) Current, I_{OH} (Except XTAL)	4,6	0,5	5	—1,6	—1,8	—	—1,6	—1,8	—	mA
	9,5	0,10	10	—3,2	—3,6	—	—	—	—	
XTAL Output, I_{OH}	4,6	0	5	—38	—75	—	—38	—75	—	μA
	9,5	0	10	—75	—150	—	—	—	—	
Output Voltage Low-Level, V_{OL}	—	0,5	5	—	0	0,05	—	0	0,05	V
	—	0,10	10	—	0	0,05	—	—	—	
Output Voltage High Level, V_{OH}	—	0,5	5	4,95	5	—	4,95	5	—	V
	—	0,10	10	9,95	10	—	—	—	—	
Input Low Voltage, V_{IL}	0,5, 4,5	—	5	—	—	1,5	—	—	1,5	V
	1,9	—	10	—	—	3	—	—	—	
Input High Voltage, V_{IH}	0,5, 4,5	—	5	3,5	—	—	3,5	—	—	V
	1,9	—	10	7	—	—	—	—	—	
Input Leakage Current, I_{IN}	Any	0,5	5	—	$\pm 0,1$	± 1	—	$\pm 0,1$	± 1	μA
	Input	0,10	10	—	$\pm 0,1$	± 1	—	—	—	
3-State Output Leakage Current, I_{OUT}	0,5	0,5	5	—	$\pm 0,2$	± 2	—	$\pm 0,2$	± 2	μA
	0,10	0,10	10	—	$\pm 0,2$	$\pm 0,2$	—	—	—	

* Typical values are for $T_A = 25^\circ\text{C}$.

CDP1869, CDP1869C, CDP1870, CDP1870C, CDP1876, CDP1876C

Bit Map Operation

The VIS may be used to display data in a bit map format, offering a high resolution display (up to 46,080 pixels) with up to 7,680 color blocks (8 colors). In this mode, the character memory addresses and the page memory addresses are used to address the bit map memory. X-Y coordinates are located by implementing the appropriate software.

RGB Bond-Out Option (CDP1876) — The CDP1870 and CDP1870C may be ordered with an alternate pin-out to provide direct drive to the internal TV chassis red, blue, and green amplifiers. For the CDP1876, the LUM, PAL CHROM, and NTSC CHROM outputs become the RED, BLUE, and GREEN outputs, respectively.

In the RGB mode of operation, the RF and IF color demodulator circuits of the TV chassis are bypassed and the composite sync, video, and color information are supplied directly to the appropriate chassis sections. Since no color sub-carrier is used, the CHROM crystal is not needed, although the XTAL CHROM input must be terminated (Fig. 1B). The CDP1876, RGB Bond-Out option, offers higher color resolution and simpler interfacing than the CDP1870, CDP1870C composite interface systems when used with direct internal TV chassis systems.

OPERATION

CDP1869—Address and Sound Generator
This circuit formats and controls sound, page-memory addressing, and character-memory addressing. This is accomplished by software instructions, data from the CPU, and hardware interaction with the CDP1870 timing signals. Control and multiplexing is determined by inter-

nal registers, which are loaded by four CPU I/O instructions. Data to the command registers are loaded from the 8 multiplexed address inputs (MA0/8-MA7/15). The high-order byte (MA8-MA15) is latched by the high-to-low transition of TPA, to provide up to 16 internal data bits. The I/O instruction data are latched by the high-to-low transition of TPB (Fig. 2).

OUT 4 Instruction — This instruction uses 15 data bits(MA0-MA14) to control the tone output function. (Bit 15 is unused, but must be latched as a low). Bits MA0-MA3 control the tone output amplitude using an on-chip binary R/2R ladder network to produce a varying output amplitude in 16 steps. Bits MA4-MA6 control the tone output frequency range. Eight octaves are available (TABLE 1). Within each range the input frequency is divided by the N + 1 value on bits MA8-MA14, producing up to 128 different frequencies. The divided output is a square-wave signal gated on or off by bit MA7. A high on MA7 turns the tone output off. If both the tone and white noise are turned off, the sound output impedance is equal to 2.5R.

OUT 5 instruction—This instruction uses 13 data bits. (Bits MA1, MA2, and MA4 are unused and need not be programmed). The higher-order byte (MA8-MA15) is used to control the white noise output function. Bits MA8-MA11 control the white noise output amplitude using an on-chip binary R/2R ladder network to provide a varying output amplitude in 16 steps. Bits MA12-MA14 control the white noise output frequency range. Eight ranges are available (TABLE 2). The white noise output is gated on or off by bit MA15. The result is

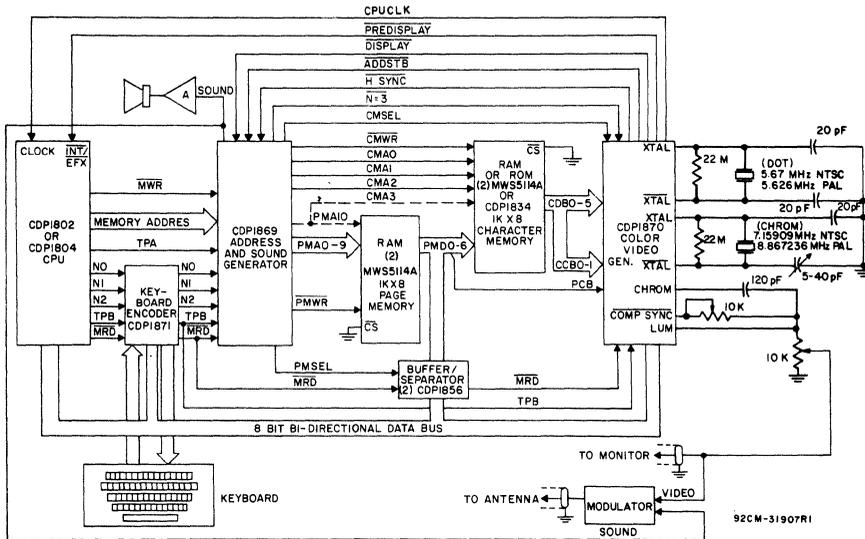


Fig. 1A—System diagram using CDP1869 and CDP1870 (Composite Outputs).
See Fig. 1B using CDP1876 (RGB Bond-Out Option Outputs).

CDP1869, CDP1869C, CDP1870, CDP1870C, CDP1876, CDP1876C

an explosion-type sound effect useful in TV game systems. A high on MA15 turns the white noise output off. If both the tone and white noise are on, a combined amplitude and frequency output results.

The lower-order byte (MA0-MA7) provides screen format control. The CMEM ACCESS MODE Bit (MA0) is used in conjunction with the OUT 6 Instruction to control the character memory READ/WRITE functions. A high on MA0 enables the character access mode.

The 9-LINE bit (MA3) is used to select either 8-line or 9-line character matrix operation. A low on MA3 selects 9-line operation, which is normally used with PAL compatible signal timing (TABLE 7). The 16-LINE HI-RES bit (MA5) is used to define the vertical resolution of each character by selective control of the CMA3/PMA10 output. A low on MA5 defines each character as a 6x8 dot matrix and PMA10 is available to extend the page memory addressing. A high on MA5 defines each character as a 6x16 dot matrix by using CMA3 to extend the character memory line addressing. Each of the 16 character matrix lines may contain different data. The 16-LINE HI-RES bit (MA5) must be low if the DOUBLE-PAGE bit (MA6) is high. (During PAL operation, where each character is normally a 6x9 dot matrix, the 16-LINE HI-RES mode is not available and MA5 should be programmed low).

The DOUBLE-PAGE bit (MA6) is used to select the function of the CMA3/PMA10 output. A low on MA6 selects the single-page mode, in which the maximum page memory size is limited to 960 bytes. The VIS will normally do a roll screen operation when the end of the display page is reached. In the single-page mode, the CMA3/PMA10 output is available as CMA3 to expand the character-memory if the 16-line HI-RES bit is high. A high on MA6 selects the double-page mode. In this mode, the CMA3/PMA10 output functions as PMA10 to expand the page-memory addressing to 1920 bytes. At the end of the first page a scroll automatically occurs. The next row entered is displayed at the bottom of the screen, with the previous page shifted up one row. The old top row is no longer displayed, but is still in memory.

In PAL systems, the double-page function is normally useful only for alphanumeric applications, since the CMA3 bit is not available for addressing the character-memory.

The FRES VERT bit (MA7) controls the full screen vertical resolution of the display. A low on MA7 sets the maximum resolution to 12 rows of characters. A high on MA7 sets the maximum resolution of 24 rows of characters.

All valid display format combinations are shown in TABLE 8, along with the page and character-memory requirements. Fig. 7 shows the relative character matrix sizes.

OUT 6 Instruction—This instruction uses 11 data bits (MA0-MA10) to load the page-memory address-register bits (PMA0-PMA10). If the CMEM ACCESS MODE is set (high), the page-memory address data are latched to provide character selection during a character-memory READ/WRITE operation. If the DOUBLE-PAGE bit is not set (low), PMA10 is not used and does not have to be programmed.

If the CMEM ACCESS MODE is not set (low), the 8 multiplexed inputs (MA0/8-MA7/15) are multiplexed to the page-memory address outputs (PMA0-PMA10) and the page-memory functions as an extension of the CPU memory. When the page-memory is selected (F800-FFFF), the PMWR output and the PMSEL output are enabled. The PMWR output is connected to the WRITE input of the page-memory. When using memories with a common READ/WRITE input (RCA MWS5114), the PMSEL output is connected to the select input of the data-bus buffer/separator (Fig. 1).

When the character-memory is selected (F400-F7FF), the 8 multiplexed inputs (MA0/8-MA7/15) are multiplexed to the

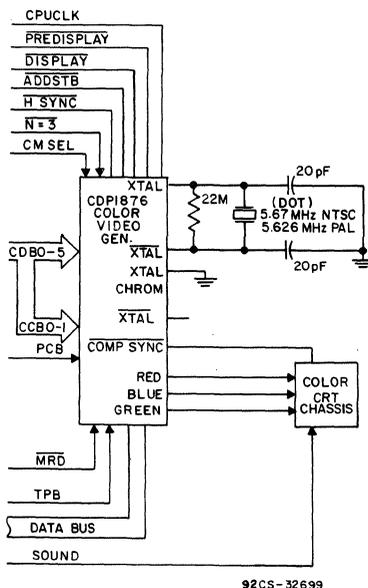


Fig. 1B—System diagram (same as that shown in Fig. 1A) using CDP1876 (RGB Bond-Out Option).

CDP1869, CDP1869C, CDP1870, CDP1870C, CDP1876, CDP1876C

OUT 6 Instruction (cont'd)

character-memory address outputs (CMA0-CMA3), and the CMWR and CMSEL outputs are enabled. The CMWR output is connected to the WRITE input of the character-memory. The CMSEL output is connected to the CMSEL input of the CDP1870C to provide data bus multiplexing. If the DOUBLE-PAGE bit is set (high), CMA3 is not used and bit MA3 does not have to be programmed.

Out 7 Instruction—This instruction uses 9 data bits (MA2-MA10) to load the home address register bits (HMA2-HMA10). The home address determines which row of characters, from the page-memory, is displayed starting at the top left-hand corner of the screen. In the FULL RES HORZ MODE (CDP1870), the home address must be an even multiple of 40. In the HALF RES HORZ MODE (CDP1870), the home address must be an even multiple of 20. Therefore, the HMA0 and HMA1 bits are not used and do not have to be programmed.

After the last row of characters has been displayed, the home address is reloaded into the page-memory address counter to begin the next display frame. When final page memory address count (maximum page-memory size in TABLE 8) is reached prior to the end of the display, zero is loaded into the address counter. Changing the home address can be used to scroll through the page-memory. In the double-page mode, row zero will scroll on to the screen after the final row, as described above.

CDP1870—Color Video Generator

This circuit formats and controls the TV sync, video, and color information. It also provides synchronization timing to the CDP1869 and the CPU. The character-memory data I/O lines are multiplexed through the CDP1870 to the CPU 8-bit bidirectional data bus. This is accomplished by software instructions, data from the CPU, and hardware interaction with the CDP1869 timing signals. Control and multiplexing is determined by a single internal command register, which is loaded by a CPU I/O instruction. Data to the command register are loaded from the 8-bit bidirectional data bus, which is latched by the high-to-low transition of TPB when the MRD and the $\overline{N=3}$ inputs are at a logic 0 (Fig. 3).

OUT 3 Instruction—This instruction uses 8 data bits to control the internal format and timing functions. The BKG GREEN, BKG BLUE, BKG RED bits (BUS0-BUS2) provide a binary selection of eight screen background colors, as shown in TABLE 5. The CFC bit (BUS 3) selects the color format control function (TABLE 4). When the CFC bit is low, the background luminance

and chrominance are selected by the BKG GREEN, BKG BLUE, and BKG RED control bits. The dot chrominance and luminance are selected by the CCBO, CCBI, and PCB inputs. Operation is the same when the CFC bit is high, except that the dot chrominance is now selected by the BKG GREEN, BKG BLUE, and BKG RED control bits to provide a tone-on-tone color display. The DISP OFF bit (BUS 4) is used to turn the screen display off. When the DISP-OFF bit is high, the PAL CHROM, NTSC CHROM, and LUM outputs are held at the background color and the ADDSTB, PREDISPLAY, and DISPLAY outputs are held at a high level. However, the COMPSYNC, HSYNC, and CPUCLK outputs continue to supply synchronization timing. This display-off condition allows the CPU to access the VIS, page memory, and character memory asynchronously. Any change in this bit is only recognized at the end of the frame. The COLB0 and COLB1 bits (BUS 5, BUS 6) provide a binary selection of 3 character-color control modes, as shown in TABLE 3. These 3 modes control which color bit inputs (CCB0, CCB1, PCB) select a particular character color (TABLE 5). The FRES HORZ bit (BUS 7) controls the full screen horizontal resolution of the display. A low of BUS 7 sets the maximum resolution to 20 characters per row. A high on BUS 7 sets the maximum resolution to 40 characters per row. All valid display format combinations are shown in TABLE 8.

The CDP1870 uses two separate input frequencies. On-chip oscillators are provided, requiring only external crystal circuits. One oscillator circuit provides the dot clock frequency, from which SYNC and ADDSTB timing is derived. The DOT frequency, divided by two, provides a CPU CLK output. The other oscillator circuit provides the color reference and chrominance frequencies. The NTSC CHROM, PALCHROM, and LUM outputs include on-chip summing resistors to reduce the external components required. The outputs are connected to the COMPSYNC output to provide a single video signal, which may be used to drive a video monitor directly or a standard TV receiver through an RF modulator circuit.

(With the RGB Bond-Out option, CDP1876, the color crystal is not used and the LUM, NTSC CHROM, and PAL CHROM become the RED, BLUE, and GREEN outputs, respectively.)

The EVS and EHS inputs may be used to sync the VIS from an existing TV chassis to provide picture overlay and teletext operations. The PAL/NTSC input is used to select either European or U.S. Operation (TABLE 6 and 7).

The VIS does not provide for an external system reset. All command and format instructions must be executed before proper operation is initiated.

CDP1869, CDP1869C, CDP1870, CDP1870C, CDP1876, CDP1876C

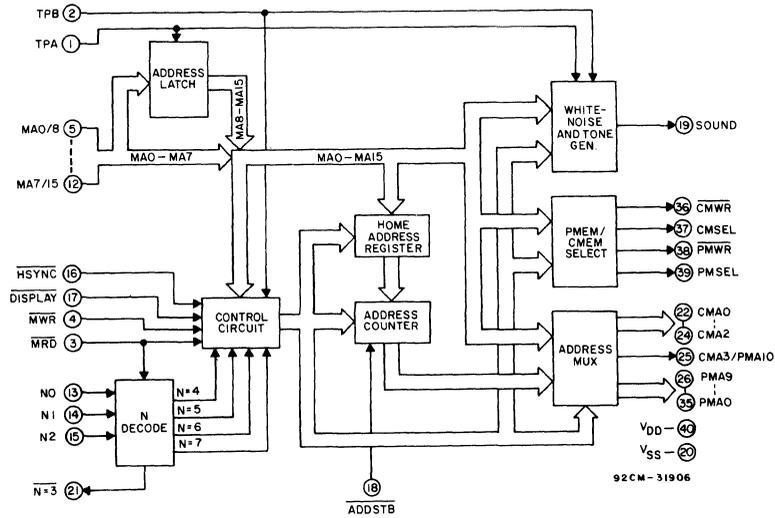


Fig. 2—CDP1869 and CDP1869C block diagram.

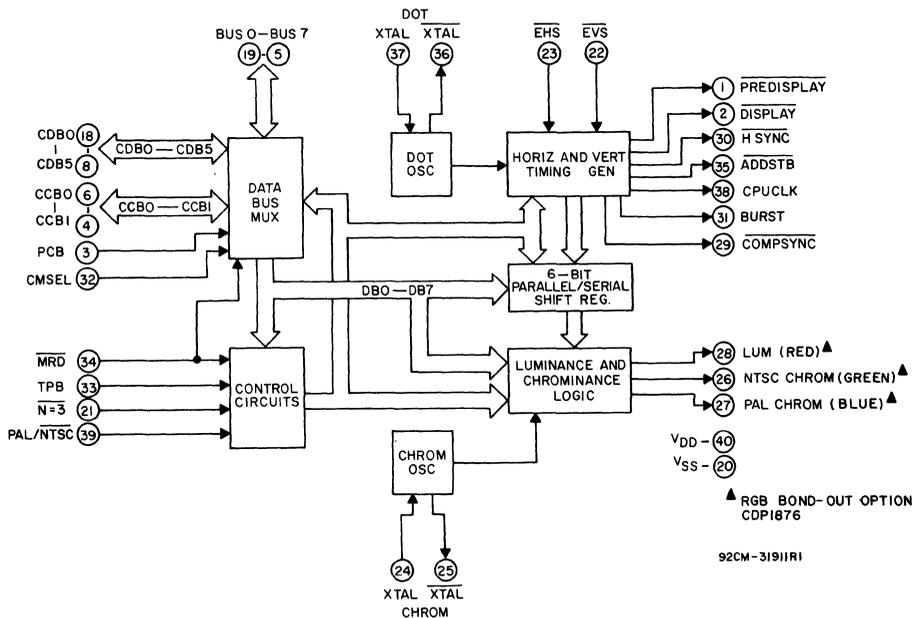


Fig. 3—CDP1870, CDP1870C, CDP1876, and CDP1876C block diagram.

FUNCTIONAL DESCRIPTION OF CDP1869 TERMINALS

TPA (Input):

An active high pulse from the CPU that occurs once in each machine cycle. The trailing edge of TPA is used to latch the higher-order byte of the 16-bit memory address. TPA is also one of the frequency generator input clocks.

TPB (Input):

An active high pulse from the CPU that occurs once in each machine cycle, following TPA. It is used to latch the various internal command registers. TPB is also one of the frequency generator input clocks.

MRD (Input):

An active low pulse from the CPU, indicating a memory read cycle. It is used to provide various latch and control functions.

MWR (Input):

An active low pulse from the CPU, appearing in a memory write cycle after the address lines have stabilized. It is used to gate various latch and control functions.

MA0/8-MA7/15 (Inputs):

The 8 memory address lines. The higher-order byte of a 16-bit CDP1802 or CDP1804 memory address appears on the memory address lines MA0-MA7 first, and is latched by the high-to-low transition of TPA. These 8-lines serve a dual purpose. They can be used to provide direct address information to the page or character memories or they can be used to provide data to the command registers.

N0 to N2 (Inputs):

These lines are used to issue command codes during an I/O instruction from the CPU. Their state is the same as the corresponding bits in the CPU N register. The three N bits are internally decoded with MRD to provide various latch and control functions.

HSYNC (Input):

Active low horizontal sync signal from the CDP1870. This signal provides synchronization between the CDP1869 and the CDP1870 timing signals.

DISPLAY (Input):

Active low signal from the CDP1870 that indicates that a screen refresh is in progress. This signal provides synchronization between the CDP1869 and the CDP1870 timing signals.

ADDSTB (Input):

Active low pulses from a CDP1870 that provide page and character-memory address clock timing. $ADDSTB = DOT\ clock \div 6$ (40 character display). $ADDSTB = DOT\ clock \div 12$ (20 character display). Only 40 or 20 pulses are generated per horizontal line, and no pulses occur during non-display time.

SOUND (Output):

This output provides two types of frequency signals that can be selected either individually or in combination. The first type provides single frequency tones in 8 selectable ranges, with 128 different tones in each range (TABLE 1). The second type provides a white-noise output in 8 selectable ranges, with the white noise consisting of all 128 tones of each range (TABLE 2). Both tone and white-noise outputs are programmable from 0 volts to $0.78 V_{DD}$ in 16 steps.

VSS:

Ground

$\overline{N=3}$ (Output):

Active low output from the internally decoded N bits that is normally connected to the CDP1870. It is used to select the CDP1870 command register.

CMA0-CMA2—CHARACTER-MEMORY ADDRESS (Outputs):

The character memory address outputs. These three outputs function as character-line selects. During a screen refresh the address data are provided by an internal counter, which is controlled by HSYNC, to provide character information in one of eight formats (Fig. 7). During non-refresh periods the address data are provided by the MA0-MA2 inputs as an extension of the CPU memory.

CMA3/PMA10 (Output):

This output signal serves a dual purpose. In the 16-LINE HI-RES character mode (command bit 5=1) this output represents CMA3 and its function is identical to the CMA0-CMA2 outputs. In the 9-LINE mode (command bit 3=0), this signal represents CMA3 in both the low-and high-resolution modes (command bit 5=0 or 1), and is used to select the ninth line of the character matrix. In the double-page mode (command bit 6=1) this output represents PMA10 and its function is identical to the PMA0-PMA9 outputs.

PMA0-PMA9—PAGE-MEMORY ADDRESS (Outputs):

These ten page-memory address outputs access the page-memory data (PMDO-6), 7 bits of which are used to address the character memory. The spare bit (PCB) may be used to expand the color information. During a screen refresh the address data are provided by an internal counter, which is controlled by ADDSTB to provide page-memory information in one of four formats (TABLE 8). During non-refresh periods the address data are provided by the MA0/8-MA9/15 inputs as an extension of the CPU memory.

CMWR—CHARACTER-MEMORY WRITE (Output):

CMWR is an active low output signal that is connected to the WRITE input of the

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character memory. This output provides a delayed MWR pulse during non-display periods, when the character memory is selected by the MA10-MA15 inputs (F400-F7FF).

CMSEL—CHARACTER-MEMORY**SELECT (Output):**

CMSEL is an active high output signal that is connected to the CDP1870 CMSEL input. This output provides a delayed positive pulse during non-display periods, when the character memory is selected by the MA10-MA15 inputs (F400-F7FF) and MRD or MWR is low.

PMWR—PAGE-MEMORY**WRITE (Output):**

PMWR is an active low output signal that is connected to the WRITE input of the page memory. This output provides a delayed MWR pulse during non-display periods, when the page memory is selected by the MA11-MA15 inputs (F800-FFFF).

PMSEL—PAGE-MEMORY**SELECT (Output):**

PMSEL is an active high output signal that is connected to an external bus separator. This output provides a delayed positive chip-enable pulse during non-display periods, when the page memory is selected by the MA11-MA15 inputs (F800-FFFF) and MRD or MWR is low.

VDD

Positive supply voltage.

FUNCTIONAL DESCRIPTION OF CDP1870 TERMINALS**PREDISPLAY (Output):**

An output signal that goes low one horizontal line before the start of the display field. This output may be connected to the CPU to provide advance warning of a refresh operation.

DISPLAY (Output):

An output signal that is low during the display field. This signal is connected to the CDP1869 to provide synchronization timing during a screen refresh.

PCB—PAGE-MEMORY**COLOR BIT (Input):**

The page-memory color bit expands the character color information to 3 bits (8 colors). (Table 3)

CCB0, CCB1—CHARACTER-MEMORY**COLOR BITS (I/O):**

The character memory color bit inputs provide character color data. These two inputs select one of four colors (Table 3) during screen refresh periods. When the CMSEL input is high during non-display periods, CCB0 and CCB1 are multiplexed to the CPU data bus (BUS 6, BUS 7) to provide character memory READ/WRITE data.

CDB0-CDB5—CHARACTER-MEMORY DATA BITS (I/O):

The character-memory data bit inputs provide character data during screen refresh periods. When the CMSEL input is high during non-display periods, CDB0-CDB5 are multiplexed to the CPU data bus (BUS 0-BUS 5) to provide character memory READ/WRITE data.

BUS 0-BUS 7 (I/O):

The 8-bit bidirectional data bus that is normally connected directly to the CPU. During non-display periods, these I/O lines serve a dual function. If the CMSEL input is high, BUS 0-BUS 7 provide character-memory READ/WRITE data. If the $N=3$ input (OUT 3 instruction) is low, BUS 0-BUS 7 provide input data to the CDP1870 command register. These data are latched on the high-to-low transition of TPB when MRD is low.

Vss:

Ground.

 $N=3$ (Input):

An input signal from the CDP1869 that is low during an OUT 3 instruction from the CPU. This input is used to select the CDP1870 command register.

EVS, EHS—EXTERNAL VERTICAL SIGNAL, EXTERNAL HORIZONTAL SIGNAL (Inputs):

The active low external vertical and horizontal sync signals synchronize the VIS to an external system. When not used, these inputs must be connected high.

XTAL (Input), \overline{XTAL} (Output)—CHROM COLOR CHROMINANCE CRYSTAL

The color chrominance crystal inputs are normally connected to a 7.15909-MHz crystal (NTSC) or an 8.867236-MHz crystal (PAL) to provide a burst and color data input clock. The XTAL input may be connected to an external generator. (With the RGB Bond-Out option, CDP1876, the chrominance crystal is not required although the XTAL input must be terminated.)

NTSC CHROM (Output):

The United States Standard Color Video Signal (NTSC). This output provides a composite signal containing chrominance information and 11 cycles of the color reference signal. (With the RGB Bond-Out option, CDP1876, this output provides the GREEN drive.)

PAL CHROM (Output):

The European standard color video signal (PAL). This output provides a composite signal containing chrominance information and 14 cycles of the color reference signal. (With the RGB Bond-Out option, CDP1876, this output provides the BLUE drive.)

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LUM—LUMINANCE (Output):

The luminance output signal provides video dot brightness information. (With the RGB Bond-Out option, CDP1876, this output provides the RED drive.)

COMPSYNC (Output):

The composite TV synchronization signal provides negative pulses at the TV line rate (horizontal) and frame (vertical) rates.

HSYNC (Output):

The horizontal synchronization signal provides an active low pulse at the TV line rate. It is connected to the CDP1869 to control timing synchronization.

BURST (Output):

This output provides a positive pulse following the horizontal sync pulse. It indicates when the color reference signal is being output, however it is not required for normal operation.

CMSEL—CHARACTER-MEMORY

SELECT (Input):

The character-memory select input, from the CDP1869, indicates a character-memory READ/WRITE operation. When CMSEL is high, the 8-bit bidirectional data bus from the CPU is multiplexed to the CCB0, CCB1, and CDB0-CDB5 I/O lines to provide character-memory data. This input is active only during non-display periods.

TPB (Input):

An active high pulse from the CPU that occurs once in each machine cycle, following the TPA pulse. This input pulse is used to latch the CDP1870 command register data on the high-to-low transition, when the N=3 and MRD inputs are low.

TABLE 1 TONE RANGE SELECT

TONE FREQ SEL2	TONE FREQ SEL1	TONE FREQ SEL0	INPUT FREQUENCY (kHz)	CPU CLK *
0	0	0	5.5371093	+ 512
0	0	1	11.074218	+ 256
0	1	0	22.148437	+ 128
0	1	1	44.296875	+ 64
1	0	0	88.593750	+ 32
1	0	1	177.18750	+ 16
1	1	0	354.37500	+ 8
1	1	1	708.75000	+ 4

* CPUCLK = 2.835 MHz

TABLE 2 WHITE NOISE RANGE SELECT

WN FREQ SEL2	WN FREQ SEL1	WN FREQ SEL0	TOP-OF-RANGE FREQUENCY (kHz)	CPU CLK *
0	0	0	0.69213867	+ 4096
0	0	1	1.3842773	+ 2048
0	1	0	2.7685546	+ 1024
0	1	1	5.5371093	+ 512
1	0	0	11.074218	+ 256
1	0	1	22.148437	+ 128
1	1	0	44.296875	+ 64
1	1	1	88.593750	+ 32

* CPUCLK = 2.835 MHz

CDP1869, CDP1869C, CDP1870, CDP1870C, CDP1876, CDP1876C

MRD—MEMORY READ (Input):

An active low pulse from the CPU indicating a memory READ cycle. This signal enables the command register clock and selects the direction of data flow in the data bus multiplexer. When this signal is low, a CPU READ operation is in progress.

ADDSTB—MEMORY ADDRESS STROBE (Output):

The ADDSTB output signal is connected to the CDP1869 to provide the page and character-memory address counter clock.

XTAL (Input), XTAL (Output)—DOT CRYSTAL:

The dot crystal inputs are normally connected to a 5.67-MHz crystal (NTSC) or a 5.626-MHz crystal (PAL) that is used to provide horizontal, vertical, and control

timing. The XTAL input may be connected to an external generator.

CPUCLK—CLOCK (Output):

A clock output equal to 1/2 the DOT frequency. It may be connected to the CPU CLOCK input terminal. At this frequency, 2947 instructions per frame are available, with 787 instructions occurring during the non-display period.

PAL/NTSC (Input):

This input selects either PAL or NTSC operation. When the PAL/NTSC input is high, the VIS provides PAL compatible output signals. When the PAL/NTSC input is low, the VIS provides NTSC compatible output signals.

VDD:

Positive supply voltage.

**TABLE 3
CHARACTER COLOR CONTROL**

COLB1	COLB0	RED	BLUE	GREEN
0	0	CCB0	CCB1	PCB
0	1	CCB0	PCB	CCB1
1	0	PCB	CCB0	CCB1
1	1	PCB	CCB0	CCB1

**TABLE 4
COLOR FORMAT CONTROL**

CFC	BKG CHR	BKG LUM	DOT CHR	DOT LUM
0	BKG R,B,G	BKG R,B,G	CCB0/CCB1 PCB	CCB0/CCB1 PCB
1	BKG R,B,G	BKG R,B,G	BKG R,B,G	CCB0/CCB1 PCB

**TABLE 5
COLOR SELECT**

CHAR OR BKG COLOR DATA BITS			OUTPUT COLOR	% OF MAX LUMINANCE
RED	BLUE	GREEN		
0	0	0	BLACK	0
0	0	1	GREEN	59
0	1	0	BLUE	11
0	1	1	CYAN	70
1	0	0	RED	30
1	0	1	YELLOW	89
1	1	0	MAGENTA	41
1	1	1	WHITE	100

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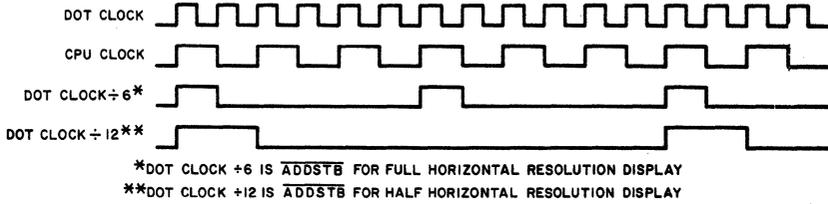


Fig. 4A—ADDSTB timing diagram.

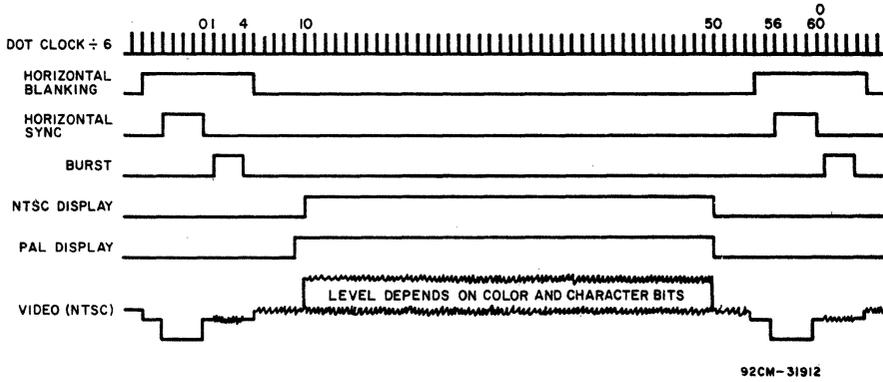


Fig. 4B—Horizontal timing diagram.

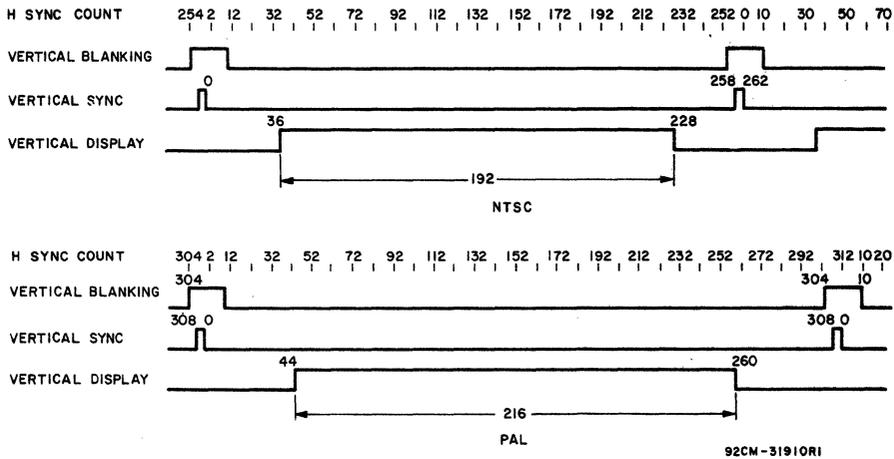


Fig. 4C—Vertical timing diagram.

CDP1869, CDP1869C, CDP1870, CDP1870C, CDP1876, CDP1876C

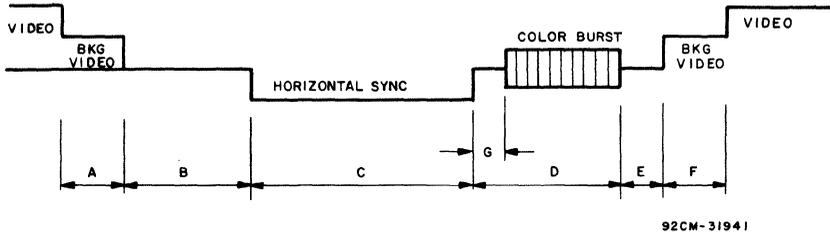


Fig. 5—Horizontal sync timing (see Table 6).

TABLE 6
HORIZONTAL TIMING STANDARDS

DIAGRAM	NTSC STANDARD	NTSC VIS 5.87 MHz XTAL	PAL STANDARD	PAL VIS 5.626 MHz XTAL
A	NA	3.7 μ s	NA	4.8 μ s
B	0.02H MIN 1.27 μ s MIN	2.12 μ s	1.55 μ s	2.12 μ s
C	0.07H-08H 4.45-5.08 μ s	4.23 μ s	4.7 μ s	4.27 μ s
D	0.045H-0.55H 8-11 CYCLES 3.58 MHz	3.174 μ s 11 CYCLES 3.58 MHz	11 CYCLES 4.433 MHz	3.199 μ s 14 CYCLES 4.433 MHz
E	0.02H MIN 1.27 μ s MIN	1.41 μ s	2.07 μ s	1.07 μ s
F	NA	6 μ s	NA	4.98 μ s
G	0.006H 0.381 μ s	0.352 μ s	0.70 μ s	0.355 μ s
HORIZONTAL FREQUENCY	15,734.264 Hz (COLOR) 15,750 Hz (B&W)	15,750 Hz	15,625 Hz	15,628 Hz

H = 63.5 μ s

NA = NOT APPLICABLE

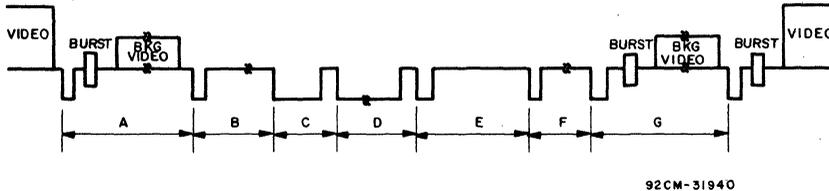


Fig. 6—Vertical sync timing (see Table 7).

TABLE 7
VERTICAL TIMING STANDARDS

DIAGRAM	NTSC STANDARD	NTSC VIS 5.87 MHz XTAL	PAL STANDARD	PAL VIS 5.626 MHz XTAL
A	NA	26H	NA	44H
B*	3H	4H	2.5H	4H
C	1H	1H	1H	1H
D	2H	3H	1.5H	3H
E	1H	1H	1H	1H
F	2H	9H	19H	9H
G	9H-12H	26H	NA	34H
HORIZONTAL PERIOD (H)	63.5 μ s	63.5 μ s	64 μ s	64 μ s
VERTICAL FREQUENCY	59.94 Hz (COLOR) 60 Hz (B&W)	60.115 Hz	50 Hz	50.09 Hz

* = NO BKG VIDEO, NO BURST

NA = NOT APPLICABLE

CDP1869, CDP1869C, CDP1870, CDP1870C, CDP1876, CDP1876C

**TABLE 8
DISPLAY FORMAT**

COMMAND DATA					DISPLAY/		
CDP1870 FRES HORZ	CDP1869 FRES VERT	CDP1869 DOUBLE PAGE	CDP1869 16-LINE HI-RES	CDP1869 9-LINE	CHAR DISPLAY MATRIX	CHAR/ ROW	CHAR ROWS/ FRAME
0	0	0	0	1	6x8	20	12
0	0	0	1	1	6x16	20	6
0	0	1	0	1	6x8	20	12
0	1	0	0	1	6x8	20	24
0	1	0	1	1	6x16	20	12
0	1	1	0	1	6x8	20	24
1	0	0	1	1	6x16	40	6
1	0	1	0	1	6x8	40	12
1	1	0	0	1	6x8	40	24
1	1	0	1	1	6x16	40	24
1	1	1	0	1	6x8	40	24
0	0	0	0	0	6x9	20	12
0	1	0	0	0	6x9	20	24
1	1	0	0	0	6x9	40	24

NOTE: ALL OTHER COMMAND COMBINATIONS ARE INVALID AND WILL RESULT IN IMPROPER DISPLAY OPERATION.

**TABLE 9
CDP1869 COMMAND**

CPU I/O INSTRUCTION	MA15	MA14	MA13	MA12	MA11	MA10	MA9	MA8
OUT 4	0*	TONE + 26	TONE + 25	TONE + 24	TONE + 23	TONE + 22	TONE + 21	TONE + 20
OUT 5	WN OFF	WN FREQ SEL2	WN FREQ SEL1	WN FREQ SEL0	WN AMP 23	WN AMP 22	WN AMP 21	WN AMP 20
OUT 6	X	X	X	X	X	PMA10 REG	PMA9 REG	PMA8 REG
OUT 7	X	X	X	X	X	HMA10 REG	HMA9 REG	HMA8 REG

X = DON'T CARE
* = MUST BE LATCHED LOW

CDP1869, CDP1869C, CDP1870, CDP1870C, CDP1876, CDP1876C

COMBINATIONS (FULL COLOR SYSTEM)

MEMORY COMBINATIONS

MAX. DISPLAY PAGE MEM. SIZE*	MAX. DISPLAY CHAR. MEM. SIZE**	CHAR SIZE ●	COMMENTS
240x8	128x8x8	4	REPEATS EACH LINE AND COL TWICE (NTSC)
240x8	128x16x8	8	REPEATS EACH LINE AND COL TWICE, 16 DIFFERENT LINES (NTSC)
1200x8	128x8x8	4	REPEATS EACH LINE AND COL TWICE, HARDWARE SCROLL (NTSC)
960x8	128x8x8	2	REPEATS EACH COL TWICE (NTSC)
960x8	128x16x8	6	REPEATS EACH COL TWICE 16 DIFFERENT LINES (NTSC)
1920x8	128x8x8	2	REPEATS EACH COL TWICE, HARDWARE SCROLL (NTSC)
240x8	128x16x8	7	REPEATS EACH LINE TWICE, 16 DIFFERENT LINES (NTSC)
1200x8	128x8x8	3	REPEATS EACH LINE TWICE, HARDWARE SCROLL (NTSC)
960x8	128x8x8	1	HIGHEST RESOLUTION (NTSC)
960x8	128x16x8	5	HIGHEST RESOLUTION, 16 DIFFERENT LINES (NTSC)
1920x8	128x8x8	1	HIGHEST RESOLUTION, HARDWARE SCROLL (NTSC)
240x8	128x9x8	4	REPEATS EACH LINE AND COL TWICE (PAL)
960x8	128x9x8	2	REPEATS EACH COL TWICE (PAL)
960x8	128x9x8	1	HIGHEST RESOLUTION (PAL)

* = 7 BITS FOR ADDRESS DATA, 1 BIT FOR COLOR DATA

● See Fig. 7.

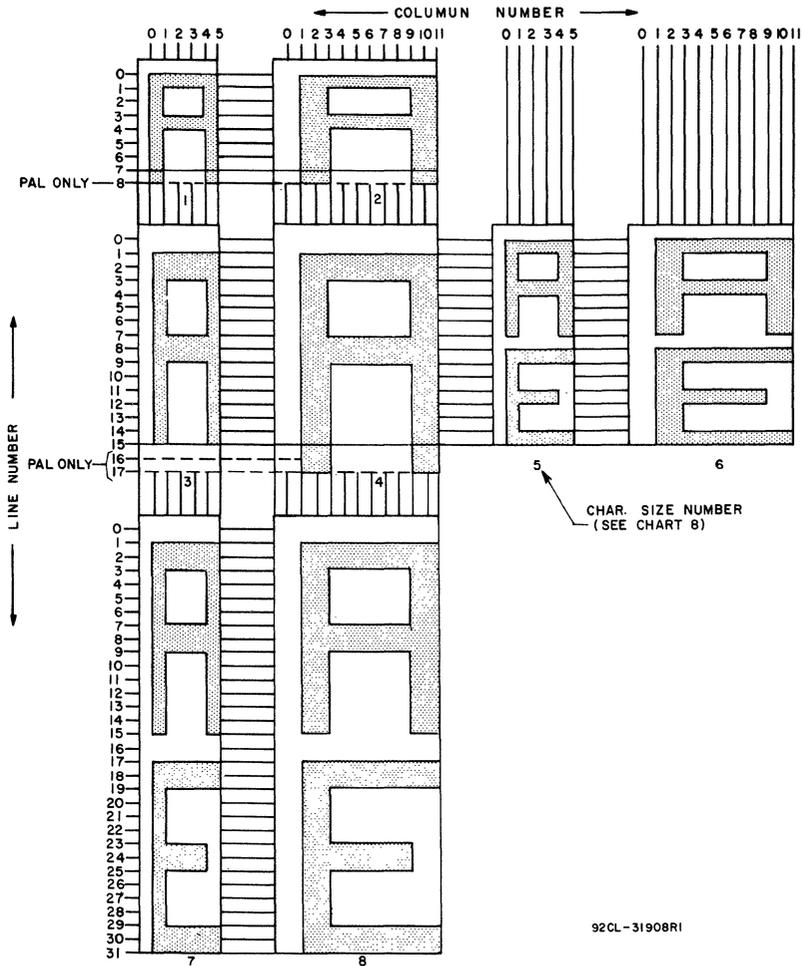
** = 6 BITS FOR CHARACTER DATA, 2 BITS FOR COLOR DATA

REGISTER CODES

MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
TONE OFF	TONE FREQ SEL2	TONE FREQ SEL1	TONE FREQ SEL0	TONE AMP 23	TONE AMP 22	TONE AMP 21	TONE AMP 20
FRES VERT	DOUBLE PAGE ***	16 LINE HI-RES ***	X	9-LINE	X	X	CMEM ACCESS MODE
PMA7 REG	PMA6 REG	PMA5 REG	PMA4 REG	PMA3 REG	PMA2 REG	PMA1 REG	PMA0 REG
HMA7 REG	HMA6 REG	HMA5 REG	HMA4 REG	HMA3 REG	HMA2 REG	X**	X**

** = ALWAYS LATCHED LOW INTERNALLY

*** MUST BE LATCHED LOW DURING 9-LINE OPERATION



92CL-31908R1

Fig. 7—Character display matrix size.

TABLE 10
CDP1870 COMMAND REGISTER CODE

CPU I/O INSTRUCTION	BUS 7	BUS 6	BUS 5	BUS 4	BUS 3	BUS 2	BUS 1	BUS 0
OUT 3	FRES HORZ	COLB1	COLB0	DISP OFF	CFC	BKG RED	BKG BLUE	BKG GREEN

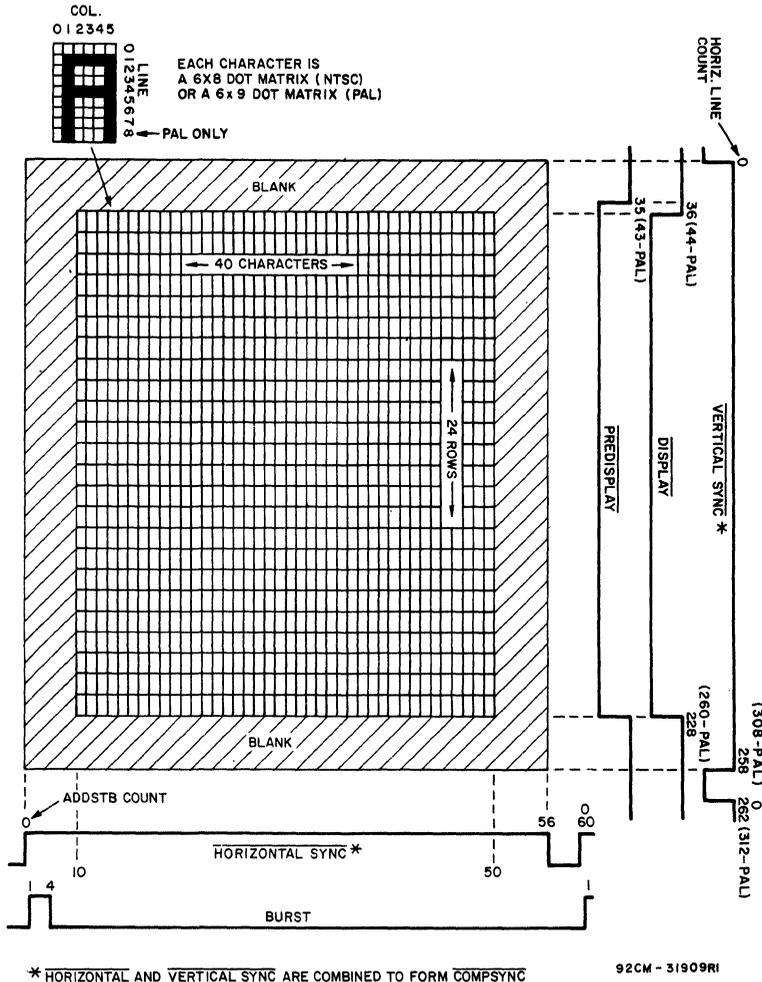


Fig. 8—40 x 24 character display.

OPERATING AND HANDLING CONSIDERATIONS

1. Handling

All inputs and outputs of RCA COS/MOS devices have a network for electrostatic protection during handling. Recommended handling practices for COS/MOS devices are described in ICAN-6525, "Guide to Better Handling and Operation of CMOS Integrated Circuits."

2. Operating

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause V_{DD} —

V_{SS} to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS} . Input currents must not exceed 10 mA even when the power supply is off.

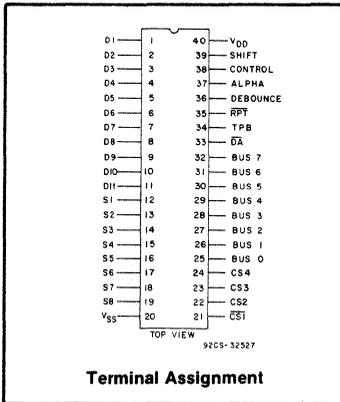
Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS} , whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} or V_{SS} may damage COS/MOS devices by exceeding the maximum device dissipation.

CMOS Keyboard Encoder



Features:

- Directly interfaces with CDP1800-series microprocessors
- Low power dissipation
- 3-State outputs
- Scans and generates code for 53 key ASCII keyboard plus 32 HEX keys (SPST mechanical contact switches)
- Shift, control, and alpha lock inputs
- RC-controlled debounce circuitry
- Single 4 to 10.5 V supply (CDP1871A); 4 to 6.5 V (CDP1871AC)
- N-key lockout

The RCA-CDP1871A is a keyboard encoder designed to directly interface between a CDP1800-series microprocessor and a mechanical keyboard array, providing up to 53 ASCII coded keys and 32 HEX coded keys, as shown in the system diagram (Fig. 1).

The keyboard may consist of simple single-pole single-throw (SPST) mechanical switches. Inputs are provided for alpha-lock, control, and shift functions, allowing 160 unique codes. An external R-C input is available for user-selectable debounce times. The N-key lock-out feature pre-

vents unwanted key codes if two or more keys are pressed simultaneously.

The CDP1871A and CDP1871AC are functionally identical. They differ in that the CDP1871A has a recommended operating voltage range of 4 to 10.5 volts, and the CDP1871AC has a recommended operating voltage range of 4 to 6.5 volts. These types are supplied in 40-lead dual-in-line ceramic packages (D suffix), and 40-lead dual-in-line plastic packages (E suffix).

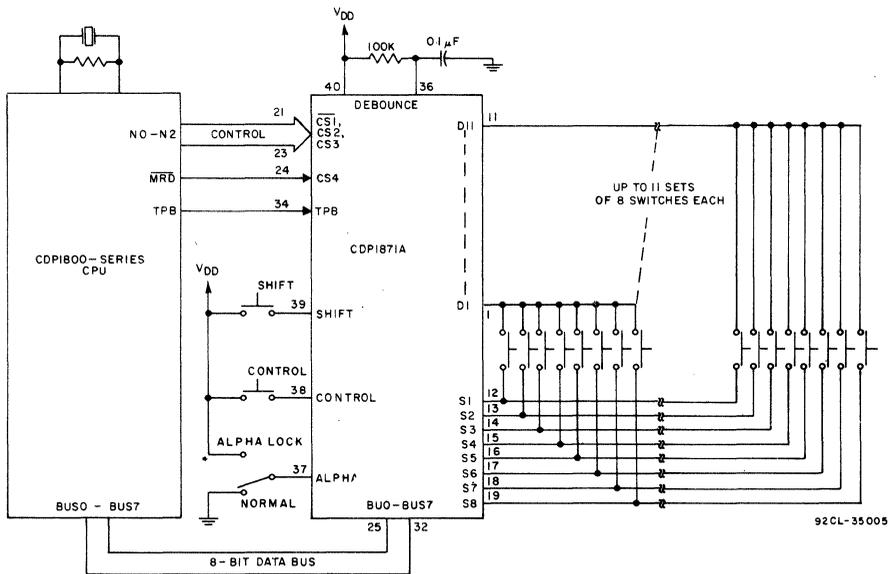


Fig. 1 — Typical CDP1800-series microprocessor system using the CDP1871A.

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD}):

(All voltage values referenced to V_{SS} terminal)

CDP1871A	-0.5 to +11 V
CDP1871AC	-0.5 to +7 V

INPUT VOLTAGE RANGE, ALL INPUTS

DC INPUT CURRENT, ANY ONE INPUT

POWER DISSIPATION PER PACKAGE (P_D):

For $T_A = -40$ to $+60^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +60$ to $+85^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 12 mW/ $^\circ\text{C}$ to 200 mW
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE D)	500 mW
For $T_A = 100$ to $+125^\circ\text{C}$ (PACKAGE TYPE D)	Derate Linearly at 12 mW/ $^\circ\text{C}$ to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE}$

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPE D	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E	-40 to $+85^\circ\text{C}$

STORAGE TEMPERATURE RANGE (T_{stg})

LEAD TEMPERATURE (DURING SOLDERING):

At distance $1/16 \pm 1/32$ inch (1.59 ± 0.79 mm) from case for 10 s max.

RECOMMENDED OPERATING CONDITIONS at $T_A = -40$ to $+85^\circ\text{C}$

For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		CDP1871AD CDP1871AE		CDP1871ACD CDP1871ACE		
		MIN.	MAX.	MIN.	MAX.	
Supply-Voltage Range		4	10.5	4	6.5	V
Recommended Input Voltage Range		V_{SS}	V_{DD}	V_{SS}	V_{DD}	V
Clock Input Frequency, TPB (Keyboard Capacitance = 200 pF)	f_{cl}	5	DC	DC	0.4	MHz
		10	DC	—	—	

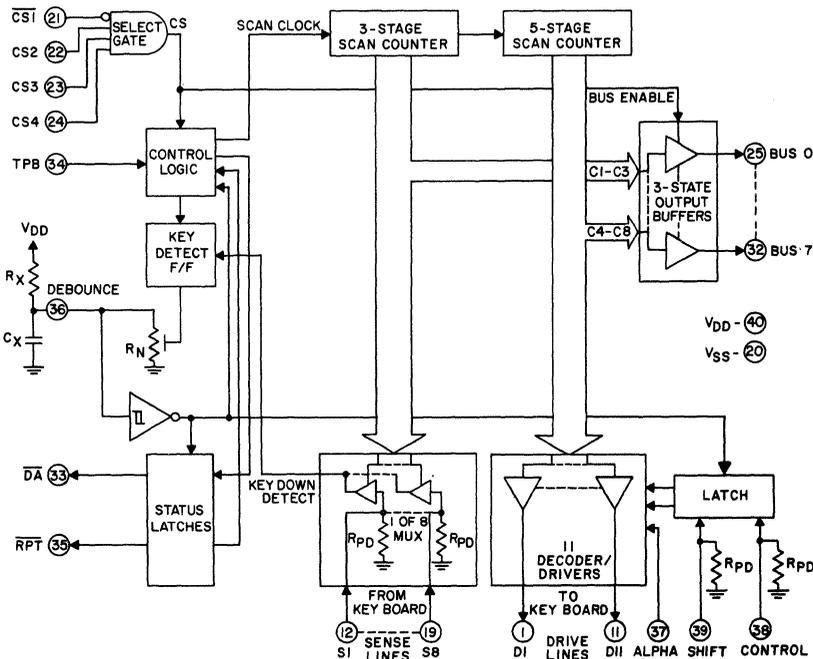


Fig. 2 — CDP1871A block diagram.

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CDP1871A, CDP1871AC

STATIC ELECTRICAL CHARACTERISTIC at $T_A = -40$ to $+85^\circ\text{C}$, except as noted

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS	
	V_O (V)	V_{IN} (V)	V_{DD} (V)	CDP1871AD CDP1871AE			CDP1871ACD CDP1871ACE				
				MIN.	TYP.*	MAX.	MIN.	TYP.*	MAX.		
Quiescent Device Current	I_{DD}	—	0,5	5	—	0.1	50	—	1	200	μA
Output Low Drive (sink) Current (except debounce and D1-D11)	I_{OL}	0.4	0,5	5	0.5	1	—	0.5	1	—	mA
Debounce	I_{OL}	0.5	0,10	10	1	2	—	—	—	—	
		0.4	0,5	5	0.75	1.5	—	0.75	1.5	—	
D1-D11	I_{OL}	0.5	0,10	10	1	2	—	—	—	—	
		0.4	0,5	5	.05	0.1	—	.05	0.1	—	
Output High Drive (Source) Current	I_{OH}	4.6	0,5	5	0.3	0.6	—	0.3	0.6	—	
Input Low Voltage (except Debounce)	V_{IL}	0.5,4.5	—	5	—	—	1.5	—	—	1.5	V
		1.9	—	10	—	—	3	—	—	—	
Input High Voltage (except Debounce)	V_{IH}	0.5,4.5	—	5	3.5	—	—	3.5	—	—	
		1.9	—	10	7	—	—	—	—	—	
Debounce Schmitt Trigger Input Voltage Positive Trigger Voltage	V_D	0.4	—	5	2.0	3.3	4.0	2.0	3.3	4.0	
		0.5	—	10	4.0	6.3	8.0	—	—	—	
Negative Trigger Voltage	V_N	0.4	—	5	0.8	1.8	3.0	0.8	1.8	3.0	
		0.5	—	10	1.9	4.0	6.0	—	—	—	
Hysteresis	V_H	0.4	0,5	5	0.3	1.6	2.6	0.3	1.6	2.6	
Output Voltage Low Level	V_{OL}	—	0,5	5	—	0	.05	—	0	.05	
		—	0,10	10	—	0	.05	—	—	—	
Output Voltage High Level	V_{OH}	—	0,5	5	4.95	5	—	4.95	5	—	
		—	0,10	10	9.95	10	—	—	—	—	
Input Leakage Current (except S1-S8, Shift, Control)	I_{IN}	—	0,5	5	—	.01	1	—	.01	1	μA
		—	0,10	10	—	.01	1	—	—	—	
3-State Output Leakage Current	I_{OUT}	0.5	0,5	5	—	.01	1	—	.02	2	
		0,10	0,10	10	—	.02	2	—	—	—	
Pull-Down Resistor Value (S1-S8, Shift, Control)	R_{PD}	—	—	—	7	14	24	7	14	24	k Ω
Operating Current (All-outputs unloaded) $f_{CL} = 0.4$ MHz $f_{CL} = 0.8$ MHz	I_{oper}	0.5,4.5	0,5	5	—	0.6	—	—	0.6	—	mA
		1,9	0,10	10	—	2.7	—	—	—	—	

*Typical values are for $T_A = +25^\circ\text{C}$. and nominal V_{DD} .

FUNCTIONAL DESCRIPTION OF CDP1871A TERMINALS

D1 — D11 (Outputs):

Drive lines for the 11 x 8 keyboard switch matrix. These outputs are connected through the external switch matrix to the sense lines (S1 — S8).

S1 — S8 (Inputs):

Sense lines for the 11 x 8 keyboard maxtrix. These inputs have internal pull-down resistors and are driven high by appropriate drive line when a keyboard switch is closed.

$\overline{CS1}$, CS2, CS3, CS4 (Inputs):

Chip select inputs, which are used to enable the tri-state data bus outputs (BUS 0 — BUS 7) and to enable the resetting of the status flag (\overline{DA}), which occurs on the low-to-high transition of TPB. These four inputs are normally connected to the N-lines (N0-N2) and \overline{MRD} output of the CDP1800-series microprocessor. (Table 2)

BUS 0 — BUS 7 (Outputs):

Tri-state data bus outputs which provide the ASII and HEX codes of the detected keys. The outputs are normally connected to the BUS 0 — BUS 7 terminals of the CDP1800-series microprocessor.

\overline{DA} (Output):

The data available output flag which is set low when a valid key closure is detected. It is reset high by the low-to-high transition of TPB when data is read from the CDP1871A. This output is normally connected to a flag input (EF1-EF4) of the CDP1800-series microprocessor.

TPB (Input):

The input clock used to drive the scan generator and reset

the status flag (\overline{DA}). This input is normally connected to the TPB output of the CDP1800-series microprocessor.

\overline{RPT} (Output):

The repeat output flag which is used to indicate that a key is still closed after data has been read from the CDP1871A (\overline{DA} = high). It remains low as long as the key is closed and is used for an autorepeat function, under CPU control. This output is normally connected to a flag input (EF1-EF4) of the CDP1800-series microprocessor.

DEBOUNCE (Input):

This input is connected to the junction of an external resistor to V_{DD} and capacitor to V_{SS} . It provides a debounce time delay ($t \cong RC$) after the release of a key. If a debounce is not desired, the external pull-up resistor is still required.

ALPHA, SHIFT, CONTROL (Inputs):

A high on the SHIFT or CONTROL inputs will be internally latched (after the debounce time) and the drive and sense line decoding will be modified as shown in Table 3. They are normally connected to the keyboard, but produce no code by themselves. The SHIFT and CONTROL inputs have internal pull-down resistors to simplify use with momentary contact switches. The ALPHA input is not latched and is designed for a standard SPDT switch to provide an alpha-lock function. When ALPHA = 1 the drive and sense line decoding will be modified as shown in Table 3.

V_{DD} , V_{SS} :

V_{DD} is the positive supply voltage input. V_{SS} is the most negative supply voltage terminal and is normal connected to ground. All outputs swing from V_{SS} to V_{DD} . The recommended input voltage swing is from V_{SS} to V_{DD} .

TABLE 1 — SWITCH INPUT FUNCTIONS

CONTROL	SHIFT	ALPHA	KEY FUNCTION
0	0	0	NORMAL
1	X	X	CONTROL
0	1	X	SHIFT
0	0	1	ALPHA

X = DON'T CARE

TABLE 2 — VALID N-LINE CONNECTIONS

CPU	CDP1871A SIGNAL				CPU INPUT INSTRUCTION
	CS4	CS3	CS2	CS1	
CDP1800-SERIES SIGNAL	\overline{MRD}	N2	N0	N1	INP5
	\overline{MRD}	N0	N1	N2	INP3
	\overline{MRD}	N2	N1	N0	INP6

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CDP1871A, CDP1871AC

TABLE 3 — DRIVE AND SENSE LINE KEYBOARD CONNECTIONS‡

SENSE LINES	DRIVE LINES																
	D ₁		D ₂		D ₃		D ₄		D ₅		D ₆		D ₇	D ₈ †	D ₉ †	D ₁₀ †	D ₁₁ †
S ₁	SP	0	(8	'	@	H	H	P	P	X	X	SPACE	80 ₁₆	88 ₁₆	90 ₁₆	98 ₁₆
	0	8	@	NUL	h	BS	p	DLE	x	CAN							
S ₂	!	1)	9	A	A	l	l	Q	Q	Y	Y		81 ₁₆	89 ₁₆	91 ₁₆	99 ₁₆
	1	9	a	SOH	i	HT	q	DC1	y	EM							
S ₃	"	2	*	:	B	B	J	J	R	R	Z	Z	LINE FEED	82 ₁₆	8A ₁₆	92 ₁₆	9A ₁₆
	2	:	b	STX	j	LF	r	DC2	z	SUB							
S ₄	#	3	+	;	C	C	K	K	S	S	{	[ESCAPE	83 ₁₆	8B ₁₆	93 ₁₆	9B ₁₆
	3	;	c	ETX	k	VT	s	DC3	[ESC							
S ₅	\$	4	<	,	D	D	L	L	T	T	\	\		84 ₁₆	8C ₁₆	94 ₁₆	9C ₁₆
	4	,	d	EOT	l	FF	t	DC4	\	FS							
S ₆	%	5	=	-	E	E	M	M	U	U	}]	CARRIAGE RETURN	85 ₁₆	8D ₁₆	95 ₁₆	9D ₁₆
	5	-	e	ENQ	m	CR	u	NAK]	GS							
S ₇	&	6	>	.	F	F	N	N	V	V	~	†		86 ₁₆	8E ₁₆	96 ₁₆	9E ₁₆
	6	.	f	ACK	n	SO	v	SYN	†	RS							
S ₈	'	7	?	/	G	G	O	O	W	W	DEL	—	DELETE	87 ₁₆	8F ₁₆	97 ₁₆	9F ₁₆
	7	/	g	BEL	o	SI	w	ETB	—	US							

KEY:

SHIFT*	ALPHA*
NORMAL	CONTROL*

*CONTROL overrides SHIFT and ALPHA  = NO RESPONSE

‡Showing ASCII outputs for all combinations with and without SHIFT, ALPHA LOCK and CONTROL.
 †Drive lines 8, 9, 10, and 11 generate non-ASCII hex values which can be used for special codes.

TABLE 4 — HEXIDECIMAL VALUES OF ASCII CHARACTERS

	BITS					MSD							
	b4	b3	b2	b1	HEX	0	0	0	0	1	1	1	1
						0	0	1	1	0	0	1	1
LSD	0	0	0	0	0	NUL	DLE	SP	0	@	P	\	p
	0	0	0	1	1	SOH	DC1	!	1	A	Q	a	q
	0	0	1	0	2	STX	DC2	"	2	B	R	b	r
	0	0	1	1	3	ETX	DC3	#	3	C	S	c	s
	0	1	0	0	4	EOT	DC4	\$	4	D	T	d	t
	0	1	0	1	5	ENQ	NAK	%	5	E	U	e	u
	0	1	1	0	6	ACK	SYN	&	6	F	V	f	v
	0	1	1	1	7	BEL	ETB	/	7	G	W	g	w
	1	0	0	0	8	BS	CAN	(8	H	X	h	x
	1	0	0	1	9	HT	EM)	9	I	Y	i	y
	1	0	1	0	A	LF	SUB	*	:	J	Z	j	z
	1	0	1	1	B	VT	ESC	+	;	K	[k	{
	1	1	0	0	C	FF	FS	,	<	L	\	l	
	1	1	0	1	D	CR	GS	-	=	M]	m	};
	1	1	1	0	E	SO	RS	.	>	N	~	n	~
	1	1	1	1	F	SI	US	/	?	O	—	o	DEL

OPERATION

The CDP1871A is made up of two major sections: the counter/scan-selection logic and the control logic (Fig. 2). The counter and scan-selection logic scans the keyboard array using the drive lines (D1-D11) and the sense lines (S1-S8). The outputs of the internal 5-stage scancounter are conditionally encoded by the ALPHA, SHIFT, and CONTROL inputs (Table 1, Table 3) and are used to drive the D1-D11 output lines high one at a time. Each D1-D11 output may drive up to eight keys, which are sampled by the sense line inputs (S1-S8). The S1-S8 inputs are enabled by the internal 3-stage scancounter.

The control logic interfaces with the CDP1800-series I/O and timing signals to establish timing and status conditions for the CDP1871A.

The TPB input clocks the scancounters and is also used to reset the Data Available output (DA). When a valid keydown condition is detected on a sense line, the control logic inhibits the clock to the scancounters on the next low-to-high transition of TPB and the DA output is set low. The scancounter outputs (C1-C8) represent the ASCII and HEX key codes and are used to drive the BUS 0 — BUS 7 outputs, which interface directly to the CDP1800-Series data bus. The BUS 0 — BUS 7 outputs, which are normally tri-stated, are enabled by decoding the CS inputs during a CPU input instruction (Table 2). The low-to-high transition of TPB during the input instruction resets the DA output high. Once the DA output has been reset, it cannot go low again until the present key is released and a new keydown condition is detected. (This prevents unwanted repeated keycode outputs which may be caused by fast software routines).

After the depressed key is released and the debounce delay (determined by RX, CX) has occurred, the scan clock inhibit

is removed, allowing the scancounters to advance on the following high-to-low transitions of TPB. This provides an N-key lockout feature, which prevents the entry of erroneous codes when two or more keys are pressed simultaneously. The first key pressed in the scanning order is recognized, while all other keys pressed are ignored until the first key is released and read by the CPU, at which time the next key pressed in the scanning order is detected. If the first key remains closed after the CPU reads the data and resets the DA output, on the low-to-high transition of TPB, an auxiliary signal (RPT) is generated and is available to the CPU to indicate an auto-repeat condition. The RPT output is reset high at the end of the debounce delay after the depressed key is released.

The DEBOUNCE input provides a terminal connection for an external user-selected RC circuit to eliminate false detection of a keydown condition caused by keyboard noise. The operation of the DEBOUNCE circuit is shown in Fig. 2 (Pin 36). When a valid keydown is detected, the on-chip active-resistor device (R_N) is enabled and the external capacitor (C_X) is discharged, providing a key closure debounce time $\cong R_N C_X$. This discharge is sensed by the Schmitt-tigger inverter, which clocks the DA flip-flop (latching the DA output low and inhibiting the scan clock). (The DA F/F is reset by the low-to-high transition of TPB when the CS inputs are enabled). When a valid key-release is detected R_N is disabled and C_X begins to charge through the external resistor (R_X), providing a key-release debounce time $\cong R_X C_X$. This charge time is again sensed by the Schmitt-trigger inverter, enabling the scan clock to continue on the next high-to-low transitions of TPB, after the current keycode data is read by the CPU.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A -40 to +85° C, V_{DD} ±5%

CHARACTERISTIC	V _{DD} (V)	LIMITS						UNITS
		CDP1871AD CDP1871AE			CDP1871ACD CDP1871ACE			
		MIN.	TYP.*	MAX.	MIN.	TYP.*	MAX.	
Clock Cycle Time	t _{CC}	5	—	—	—	—	—	NOTE 1
		10	—	—	—	—	—	
Clock Pulse Width High	t _{CWH}	5	100	40	—	100	40	ns
		10	50	20	—	—	—	
Data Available Valid Delay	t _{DAL}	5	—	260	500	—	260	ns
		10	—	130	250	—	—	
Data Available Invalid Delay	t _{DAH}	5	—	70	150	—	70	ns
		10	—	35	75	—	—	
Scan Count Delay (Non-Repeat)	t _{CD1}	5	—	850	1900	—	850	ns
		10	—	425	950	—	—	
Data Out Valid Delay	t _{CDV}	5	—	120	250	—	120	ns
		10	—	60	125	—	—	
Data Out Hold Time	t _{CDH}	5	—	100	200	—	100	ns
		10	—	50	100	—	—	
Repeat Valid Delay	t _{RPL}	5	—	150	400	—	150	ns
		10	—	75	200	—	—	
Repeat Invalid Delay	t _{RPM}	5	—	350	700	—	350	ns
		10	—	170	350	—	—	

*Typical Values are for T_A = +25° C and nominal V_{DD}

Note 1: t_{CC} = t_{CWH} + t_{CWL}
t_{CWL} = t_{CD1} + KC
k = 0.9 × 10⁻⁹ Ω
c = keyboard capacitance (pF)

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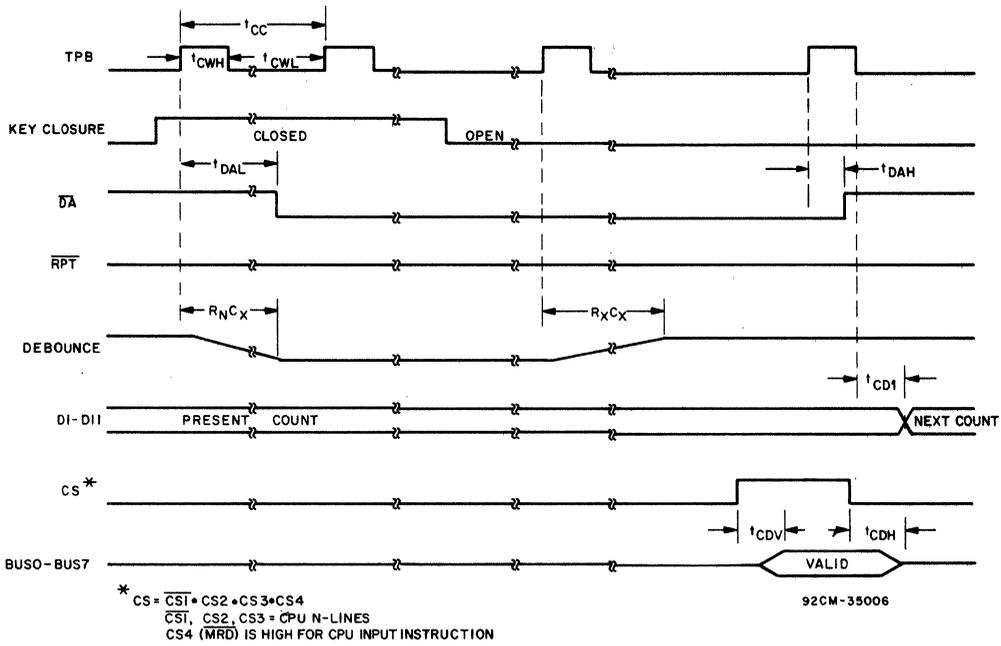


Fig. 3 — CDP1871A dynamic timing diagram (non-repeat).

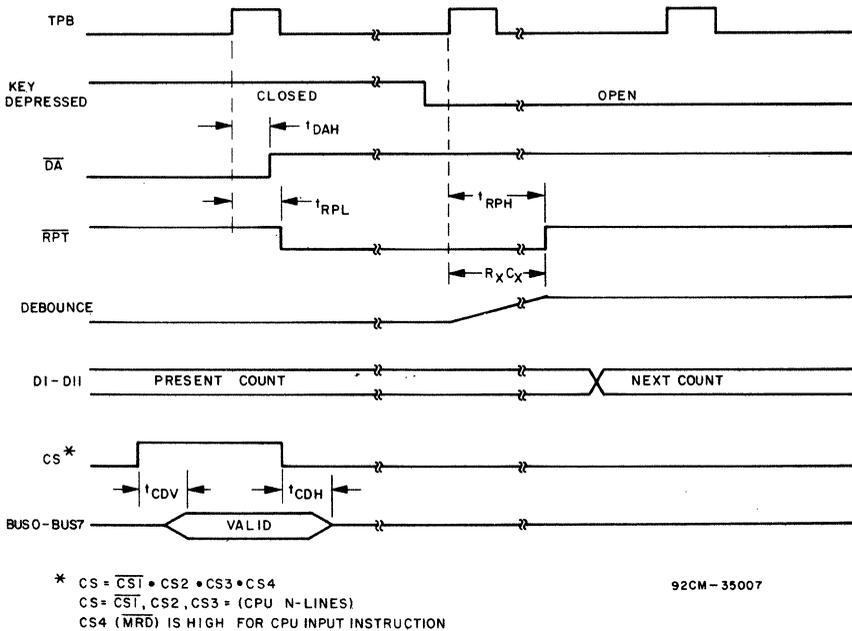
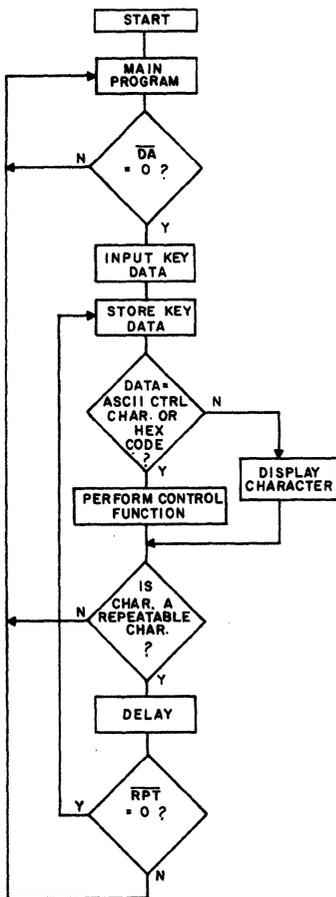


Fig. 4 — CDP1871A dynamic timing diagram (repeat).



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Fig. 5 — Typical system software flowchart for CDP1871A, CDP1871AC.

ORDERING INFORMATION

RCA Microprocessor device packages are identified by letter indicated in the following chart. When ordering a Microprocessor device, it is important that the appropriate suffix letter be affixed to the type number of the device.

Package	Suffix Letter
Dual-In-Line Side-Brazed Ceramic	D
Dual-In-Line Plastic	E

For example, a CDP1871AC in a dual-in-line plastic package will be identified as the CDP1871ACE.

OPERATING AND HANDLING CONSIDERATIONS

1. Handling

All inputs and outputs of RCA Microprocessor devices have a network for electrostatic protection during handling. Recommended handling practices for Microprocessor devices are described in ICAN-6525, "Guide to Better Handling and Operation of CMOS Integrated Circuits."

2. Operating

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause $V_{DD}-V_{SS}$ to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS} . Input currents must not exceed 10 mA even when the power supply is off.

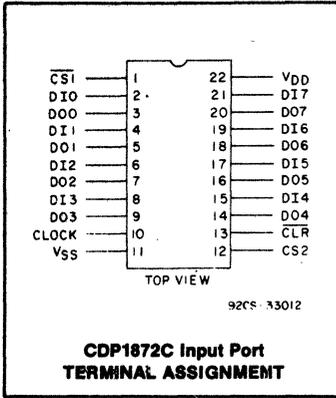
Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS} , whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} or V_{SS} may damage Microprocessor devices by exceeding the maximum device dissipation.

High-Speed 8-Bit Input and Output Ports



Features:

- Parallel 8-bit input/output register with buffered outputs
- High-speed data-in to data-out:
85 ns (max.) at $V_{DD}=5 V$
- Flexible applications in microprocessor systems as buffers and latches
- High order address-latch capability in CDP1800 series microprocessor systems
- Output sink current=5 mA (min.) at $V_{DD}=5 V$
- 3-state output-CDP1872C and CDP1874C

The RCA-CDP1872C, CDP1874C and CDP1875C devices are high-speed 8-bit parallel input and output ports designed for use in the CDP1800 microprocessor system and for general use in other microprocessor systems. The CDP1872C and CDP1874C are 8-bit input ports; the CDP1875C is an 8-bit output port.

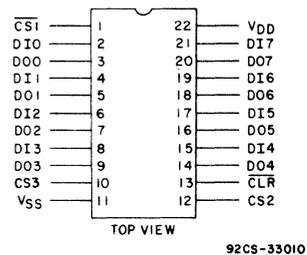
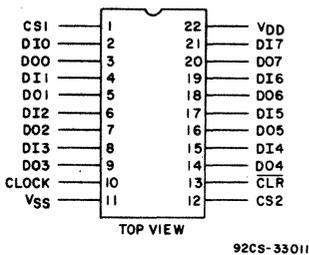
These devices have flexible capabilities as buffers and data latches and are reset by CLR input when the data strobe is not active.

The CDP1872C and CDP1874C are functionally identical except for device selects. The CDP1872C has one active low and one active high select; the CDP1874C has two

active high device selects. These devices also feature 3-state outputs when deselected. Data is strobed into the register on the leading edge of the CLOCK and latched on the trailing edge of the CLOCK.

The CDP1875C is an output port with data latched into the registers when the device selects are active. There are two active high and one active low selects. The output buffers are enabled at all times.

These devices are supplied in 22-lead hermetic, dual-in-line side-brazed ceramic packages (D suffix) and in 22-lead dual-in-line plastic packages (E suffix).



CDP1872C, CDP1874C, CDP1875C

RECOMMENDED OPERATING CONDITIONS at $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS ALL TYPES	UNITS
DC Operating-Voltage Range	4 to 6.5	V
Input Voltage Range	V_{SS} to V_{DD}	

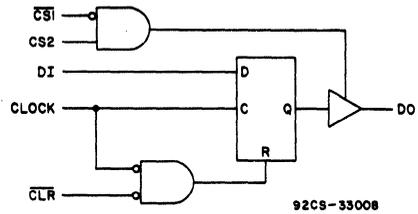


Fig. 1—Equivalent logic diagram (1 of 8 latches shown) for CDP1872C.

MAXIMUM RATINGS, Absolute-Maximum Values:

- DC SUPPLY-VOLTAGE RANGE, (V_{DD}) -0.5 to $+7$ V
(Voltage referenced to V_{SS} Terminal)
- INPUT VOLTAGE RANGE, ALL INPUTS -0.5 to $V_{DD} + 0.5$ V
- DC INPUT CURRENT, ANY ONE INPUT ± 10 mA
- POWER DISSIPATION PER PACKAGE (P_D):
 - For $T_A = -40$ to $+60^\circ\text{C}$ (PACKAGE TYPE E) 500 mW
 - For $T_A = +60$ to $+85^\circ\text{C}$ (PACKAGE TYPE E) Derate Linearly at $12\text{ mW}/^\circ\text{C}$ to 200 mW
 - For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE D) 500 mW
 - For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE D) Derate Linearly at $12\text{ mW}/^\circ\text{C}$ to 200 mW
- DEVICE DISSIPATION PER OUTPUT TRANSISTOR
 - FOR T_A —FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100 mW
- OPERATING-TEMPERATURE RANGE (T_A):
 - PACKAGE TYPE D -55 to $+125^\circ\text{C}$
 - PACKAGE TYPE E -40 to $+85^\circ\text{C}$
- STORAGE TEMPERATURE RANGE (T_{stg}) -65 to $+150^\circ\text{C}$
- LEAD TEMPERATURE (DURING SOLDERING):
 - At distance $1/16 \pm 1/32$ in. (1.59 ± 0.79 mm) from case for 10 s max. $+265^\circ\text{C}$

STATIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} \pm 5\%$, except as noted

CHARACTERISTIC		TEST CONDITIONS			LIMITS ALL TYPES			UNITS
		V_O	V_{IN}	V_{DD}	Min.	Typ.*	Max.	
		(V)	(V)	(V)				
Quiescent Device Current	I_{DD}	—	0, 5	5	—	25	50	μA
Output Low Drive (Sink) Current	I_{OL}	0.4	0, 5	5	5	10	—	mA
Output High Drive (Source) Current	I_{OH}	4.6	0, 5	5	-4	-7	—	
Output Voltage Low-Level *	V_{OL}	—	0, 5	5	—	0	0.1	V
Output Voltage High-Level *	V_{OH}	—	0, 5	5	4.9	5	—	
Input Low Voltage	V_{IL}	0.5, 4.5	—	5	—	—	1.5	
Input High Voltage	V_{IH}	0.5, 4.5	—	5	3.5	—	—	
Input Leakage Current	I_{IN}	—	0, 5	5	—	—	± 1	μA
3-State Output Leakage Current #	I_{OUT}	0, 5	0, 5	5	—	—	± 5	
Input Capacitance	C_{IN}	—	—	—	—	15	—	pF
Output Capacitance #	C_{OUT}	—	—	—	—	15	—	

* Typical values are for $T_A = 25^\circ\text{C}$ and $V_{DD} \pm 5\%$.
 * $I_{OL} = I_{OH} = 1\ \mu\text{A}$.
 # For CDP1872C and CDP1874C only.

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CDP1872C, CDP1874C, CDP1875C

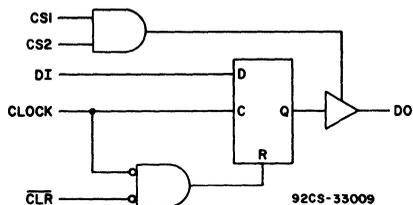


Fig. 2—Equivalent logic diagram (1 of 8 latches shown) for CDP1874C.

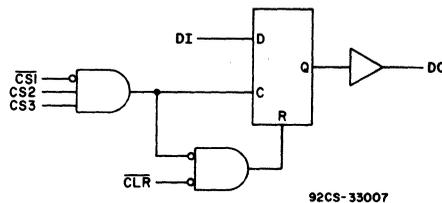


Fig. 3—Equivalent logic diagram (1 of 8 latches shown) for CDP1875C.

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A=25^\circ\text{C}$, $V_{DD}=5\text{ V}$, $t_r, t_f=10\text{ ns}$, $V_{IH}=0.7 V_{DD}$, $V_{IL}=0.3 V_{DD}$, $C_L=150\text{ pF}$

CHARACTERISTIC	LIMITS		UNITS	
	CDP1872C CDP1874C			
	Typ.*	Max.†		
Input Port (Fig. 4)				
Output Enable	t_{EN}	45	90	ns
Output Disable	t_{DIS}	45	90	
Clock to Data Out	t_{CLO}	45	90	
Clear to Output	t_{CRO}	80	160	
Data In to Data Out	t_{DIO}	50	85	
Minimum Data Setup Time	t_{DSU}	10	30	
Data Hold Time	t_{DH}	10	30	
Minimum Clock Pulse Width	t_{CL}	30	60	
Minimum Clear Pulse Width	t_{CR}	30	60	

* Typical values are for $T_A=25^\circ\text{C}$ and $V_{DD} \pm 5\%$.

† Maximum values are for $T_A=85^\circ\text{C}$ and $V_{DD} \pm 5\%$.

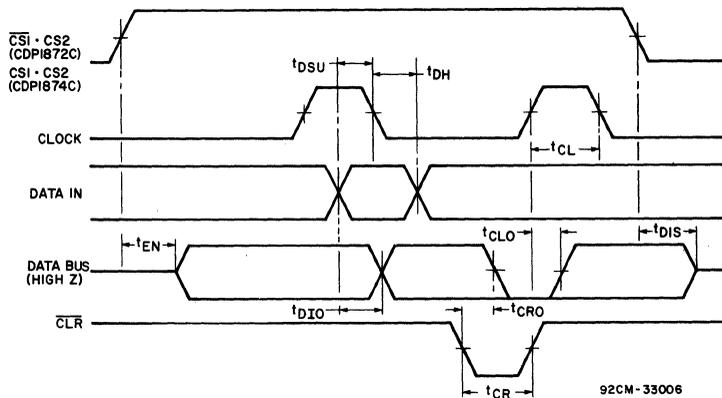


Fig. 4—Timing waveforms for CDP1872C and CDP1874C (input-port types).

CDP1872C, CDP1874C, CDP1875C

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A=25^\circ\text{C}$, $V_{DD}=5\text{V}$, $t_r, t_f=10\text{ns}$, $V_{IH}=0.7V_{DD}$,
 $V_{IL}=0.3V_{DD}$, $C_L=150\text{pF}$

CHARACTERISTIC	LIMITS		UNITS	
	CDP1875C			
	Typ.*	Max.†		
Output Port (Fig. 5)				
Clock to Data Out	t_{CLO}	50	100	ns
Clear to Output	t_{CRO}	80	160	
Data In to Data Out	t_{DIO}	50	85	
Minimum Data Setup Time	t_{DS}	10	30	
Data Hold Time	t_{DH}	10	30	
Minimum Clear Pulse Width	t_{CR}	30	60	

* Typical values are for $T_A=25^\circ\text{C}$ and $V_{DD} \pm 5\%$.

† Maximum values are for $T_A=85^\circ\text{C}$ and $V_{DD} \pm 5\%$.

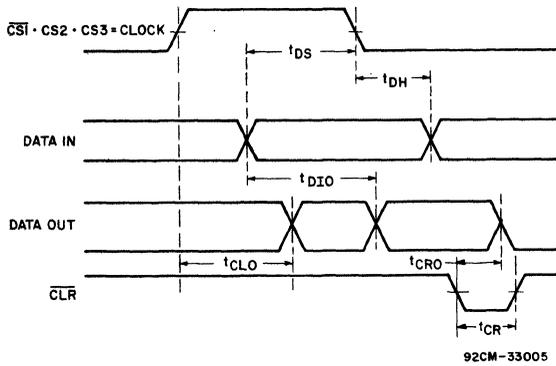


Fig. 5-Timing waveforms for CDP1875C (output port).

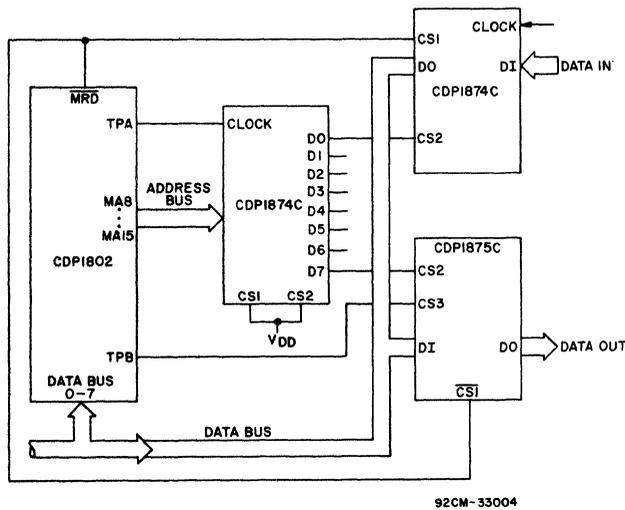
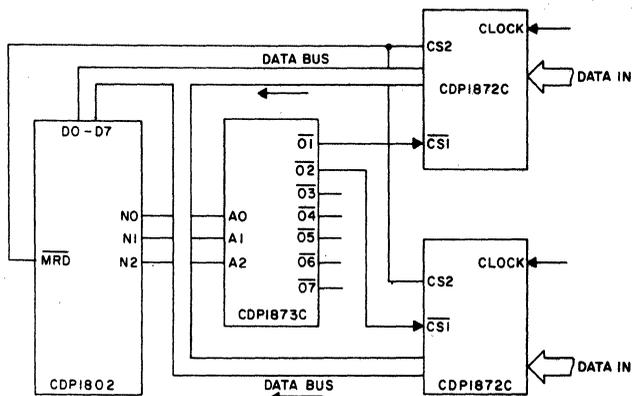


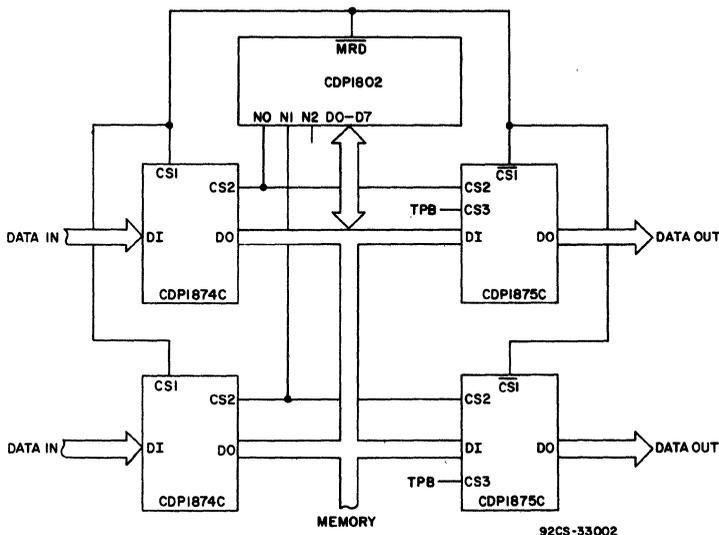
Fig. 6-CDP1874C used as an input port and address latch with CDP1875C used as an output port.

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CDP1872C, CDP1874C, CDP1875C



92CS-33003

Fig. 7—CDP1872C used as an input port and selected by CDP1873C.



92CS-33002

Fig. 8—CDP1874C and CDP1875C used as input/output buffers.

OPERATING AND HANDLING CONSIDERATIONS

1. Handling

All inputs and outputs of RCA CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in ICAN-6525 "Guide to Better Handling and Operation of CMOS Integrated Circuits."

2. Operating

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must

not cause $V_{DD}-V_{SS}$ to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS} . Input currents must not exceed 10 mA even when the power supply is off.

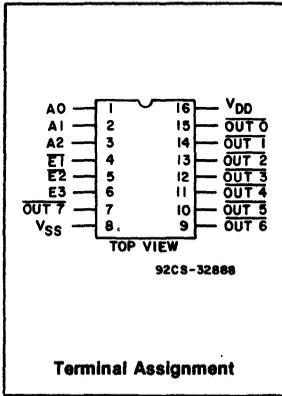
Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS} , whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} or V_{SS} may damage CMOS devices by exceeding the maximum device dissipation.

CMOS 1 of 8 Binary Decoder



Features:

- High-speed address to output enable delay 100 ns (max.) at $V_{DD}=5\text{ V}$
- Output sink 6 mA (min.) at $V_{DD}=5\text{ V}$
- I/O port or memory selector
- 3 chip-select input allows simple expansion

The RCA-CDP1873C is a high-speed 1 of 8 decoder designed for use with microprocessor systems that require expansion capabilities utilizing memory or input/output ports with active low chip-select inputs. The CDP1873C has a recommended operating voltage range of 4 to 6.5 volts.

When the decoder is enabled and addressed, one of its 8 outputs goes low.

Enabling is controlled by 3 chip-select inputs, allowing for easy system expansion. All outputs will be high when the decoder is not selected. The CDP1873C can be cascaded for very large systems and offers a low propagation delay that reduces memory-access time requirements in those designs where delays are critical.

The CDP1873C is supplied in hermetic 16-lead dual-in-line ceramic (D suffix) and plastic (E suffix) packages.

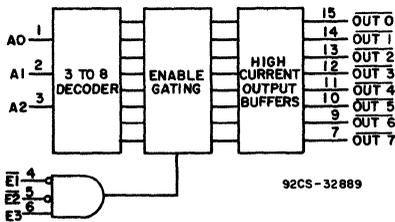


Fig. 1 - CDP1873C functional diagram.

TRUTH TABLE

ADDRESS			ENABLE			OUTPUTS							
A0	A1	A2	$\bar{E}1$	$\bar{E}2$	$\bar{E}3$	0	1	2	3	4	5	6	7
L	L	L	L	L	H	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	L	H	H	H	L	H	H	H	H	H
H	H	L	L	L	H	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
H	L	H	L	L	H	H	H	H	H	L	H	H	H
L	H	H	L	L	H	H	H	H	H	H	L	H	H
H	H	H	L	L	H	H	H	H	H	H	H	L	H
X	X	X	X	X	L	H	H	H	H	H	H	H	H
X	X	X	H	X	X	H	H	H	H	H	H	H	H
X	X	X	X	H	X	H	H	H	H	H	H	H	H

H = High level
L = Low level
X = Don't care

CDP1873C

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltage referenced to V_{SS} terminal) -0.5 to +7 V

INPUT VOLTAGE RANGE, ALL INPUTS -0.5 to V_{DD} +0.5 V

DC INPUT CURRENT, ANY ONE INPUT ±10 mA

POWER DISSIPATION PER PACKAGE (P_D):

For T_A=-40 to +60°C (PACKAGE TYPE E) 500 mW

For T_A=+60 to +85°C (PACKAGE TYPE E) Derate Linearly at 12 mW/°C to 200 mW

For T_A=-55 to +100°C (PACKAGE TYPE D) 500 mW

For T_A=+100 to +125°C (PACKAGE TYPE D) Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

For T_A=FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100 mW

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPE D -55 to +125°C

PACKAGE TYPE E -40 to +85°C

STORAGE-TEMPERATURE RANGE (T_{stg}) -65 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. +265°C

STATIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85°C, except as noted

CHARACTERISTIC	CONDITIONS			LIMITS			UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)	CDP1873C			
				Min.	Typ.*	Max.	
Quiescent Device Current, I _{DD}	—	0, 5	5	—	5	50	μA
Output Low Drive (Sink) Current, I _{OL}	0.4	0, 5	5	6	12	—	mA
Output High Drive (Source) Current, I _{OH}	4.6	0, 5	5	-4	-7	—	mA
Output Voltage Low-Level, V _{OL} ^Δ	—	0, 5	5	—	0	0.1	V
Output Voltage High Level, V _{OH} ^Δ	—	0, 5	5	4.9	5	—	
Input Low Voltage, V _{IL}	0.5, 4.5	—	5	—	—	1.5	V
Input High Voltage, V _{IH}	0.5, 4.5	—	5	3.5	—	—	
Input Leakage Current, I _{IN}	Any Input	0, 5	5	—	—	±1	μA
Operating Current, I _{DD1} [●]	—	0, 5	5	—	2	3	mA
Input Capacitance, C _{IN}	—	—	—	—	20	—	pF

*Typical values are for T_A = 25°C and nominal voltage, V_{DD}.

^ΔI_{OL} = I_{OH} = 1 μA.

[●] Operating current is measured at 200 kHz for V_{DD}=5 V and 400 kHz for V_{DD}=10 V, with open outputs (worst-case frequencies for CDP1802A system operating at maximum speed of 3.2 MHz).

OPERATING CONDITIONS at T_A = Full Package Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

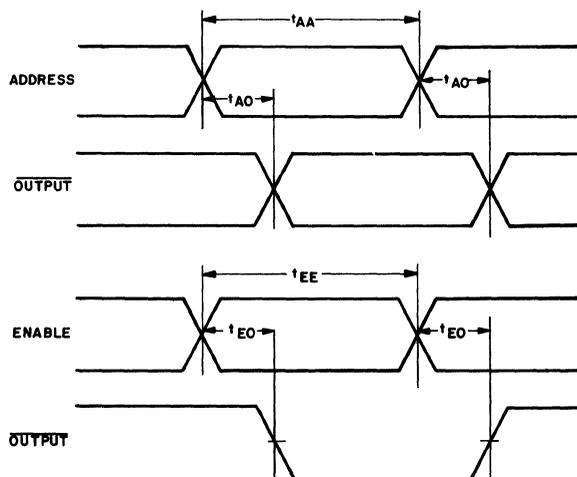
CHARACTERISTIC	LIMITS		UNITS
	CDP1873C		
	Min.	Max.	
DC Operating Voltage Range	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85$ °C, $V_{DD} = \pm 5\%$, $V_{IH} = 0.7 V_{DD}$, $V_{IL} = 0.3 V_{DD}$, $t_r, t_f = 10$ ns, $C_L = 100$ pF

CHARACTERISTIC	V_{DD} (V)	LIMITS		UNITS
		CDP1873C		
		Typ.	Max.	
Propagation Delay Time:				
Address to Output t_{AO}	5	65	100	ns
Enable to Output t_{EO}	5	65	90	
Minimum Pulse Widths:				
Address t_{AA}	5	30	50	
Enable t_{EE}	5	40	70	

Note 1: Maximum limits of minimum characteristics are the values above which all devices function.

Note 2: Typical values are for $T_A = 25$ °C and nominal voltage, V_{DD} .



92CM-32890

Fig. 2 - Timing waveforms.

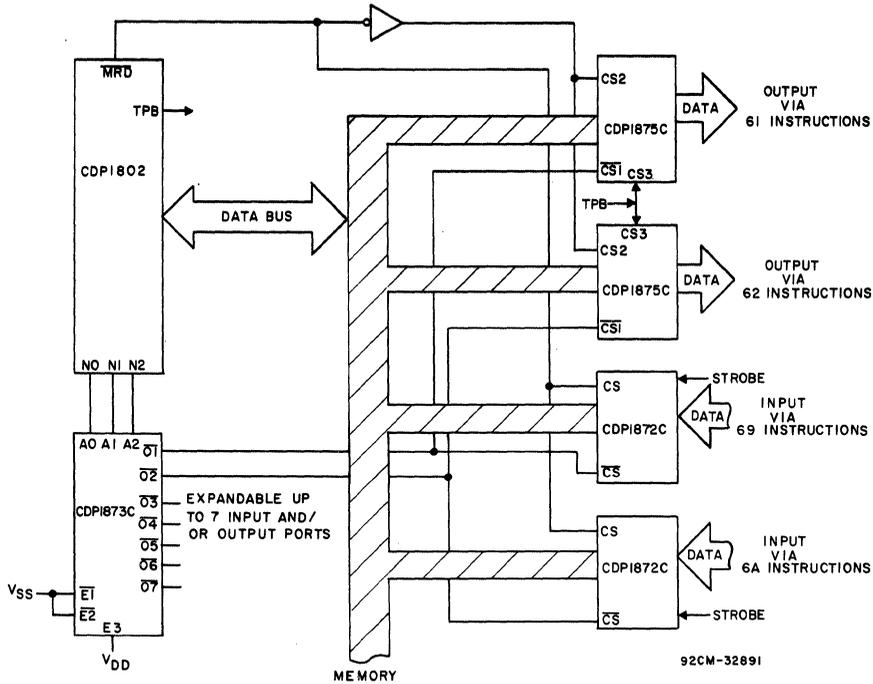


Fig. 3 - N-line decoded in a one-level I/O system.

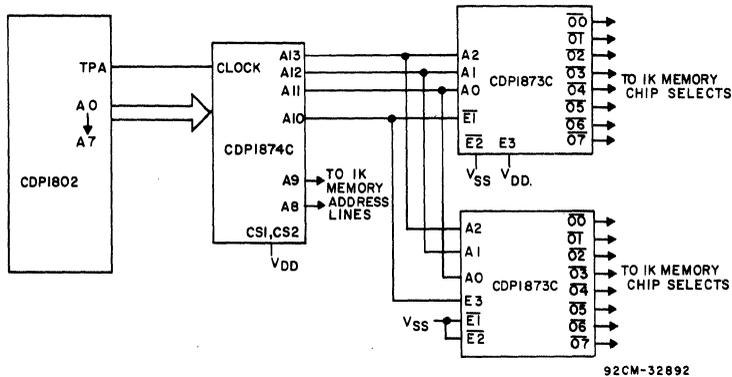


Fig. 4 - 16-k memory-select using the CDP1873C with the CDP1874C as an address latch.

OPERATING AND HANDLING CONSIDERATIONS

1. Handling

All inputs and outputs of RCA CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in ICAN-6525, "Guide to Better Handling and Operation of CMOS Integrated Circuits."

2. Operating

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these

conditions must not cause $V_{DD}-V_{SS}$ to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{CC} nor less than V_{SS} . Input currents must not exceed 10 mA even when the power supply is off.

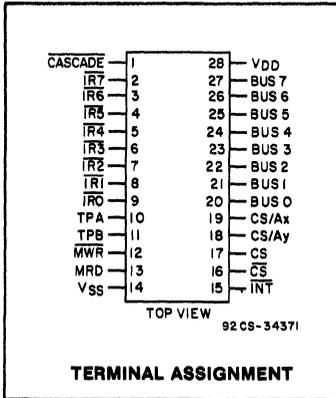
Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{CC} or V_{SS} , whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} , V_{CC} or V_{SS} may damage CMOS devices by exceeding the maximum device dissipation.

Programmable Interrupt Controller (PIC)



Features:

- Compatible with CDP1800 series
- Programmable long branch vector address and vector interval
- 8 levels of interrupt per chip
- Easily expandable
- Latched interrupt requests
- Hard wired interrupt priorities
- Memory mapped
- Multiple chip select inputs to minimize address space requirements

The RCA-CDP1877 and CDP1877C* are programmable 8-level interrupt controllers designed for use in CDP1800-series microprocessor systems. They provide added versatility by extending the number of permissible interrupts from 1 to N in increments of 8.

When a high to low transition occurs on any of the PIC interrupt lines (IRO to IR7), it will be latched and, unless the request is masked, it will cause the INTERRUPT line on the PIC and consequently the INTERRUPT input on the CPU to go low.

The CPU accesses the PIC by having interrupt vector register R(1) loaded with the memory address of the PIC. After the interrupt S3 cycle, this register value will appear at the CPU address bus, causing the CPU to fetch an instruction from the PIC. This fetch cycle clears the interrupt request latch bit to accept a new high-to-low transition, and also causes the PIC to issue a long branch instruction (CO) followed by the preprogrammed vector address written into the PIC's address registers, causing the CPU to branch to the address corresponding to the highest priority active interrupt request.

*Formerly RCA-Dev. Type No. TA10911 and TA10911C, respectively.

If no other unmasked interrupts are pending, the INTERRUPT output of the PIC will return high. When an interrupt is requested on a masked interrupt line, it will be latched but it will not cause the PIC INTERRUPT output to go low. All pending interrupts, masked and unmasked, will be indicated by a "1" in the corresponding bit of the status register. Reading of the status register will clear all pending interrupt request latches.

Several PICs can be cascaded together by connecting the INTERRUPT output of one chip to the CASCADE input of another. Each cascaded PIC provides 8 additional interrupt levels to the system. The number of units cascaded depends on the amount of memory space and the extent of the address decoding in the system.

Interrupts are prioritized in descending order; IR7 has the highest and IRO has the lowest priority.

The CDP1877 and CDP1877C are functionally identical. They differ in that the CDP1877 has a recommended operating voltage range of 4 to 10.5 volts, and the CDP1877C has a recommended operating voltage range of 4 to 6.5 volts. These types are supplied in 28-lead dual-in-line ceramic packages (D suffix), and 28-lead dual-in-line plastic packages (E suffix).

Programmable Interrupt Controller (PIC) Programming Model

BUS 7				BUS 0				
A15	A14	A13	PAGE REGISTER		A10	A9	A8	WRITE ONLY
BUS 7				BUS 0				
B7	B6	B5	CONTROL REGISTER		B2	B1	B0	WRITE ONLY
BUS 7				BUS 0				
M7	M6	M5	MASK REGISTER		M2	M1	M0	WRITE ONLY
BUS 7				BUS 0				
S7	S6	S5	STATUS REGISTER		S2	S1	S0	READ ONLY
BUS 7				BUS 0				
P7	P6	P5	POLLING REGISTER		P2	P1	P0	READ ONLY

RCA CMOS LSI Products

CDP1877, CDP1877C

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltage referenced to V_{SS} terminal)

CDP1877	-0.5 to +11 V
CDP1877C	-0.5 to +7 V

INPUT VOLTAGE RANGE, ALL INPUTS -0.5 to V_{DD} +0.5 V

DC INPUT CURRENT, ANY ONE INPUT ±10 mA

POWER DISSIPATION PER PACKAGE (P_D):

For T _A =-40 to +60°C (PACKAGE TYPE E)	500 mW
For T _A =+60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T _A =-55 to +100°C (PACKAGE TYPE D)	500 mW
For T _A =+100 to 125°C (PACKAGE TYPE D)	Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A=FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100 mW

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPE D	-55 to +125°C
PACKAGE TYPE E	-40 to +85°C

STORAGE-TEMPERATURE RANGE (T_{stg}) -65 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. +265°C

STATIC ELECTRICAL CHARACTERISTICS at T_A=-40 to +85°C, V_{DD} ±5%, Except as noted

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)	CDP1877			CDP1877C			
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device Current I _{DD}	—	0, 5	5	—	0.01	50	—	0.02	200	μA
	—	0, 10	10	—	1	200	—	—	—	
Output Low Drive (Sink) Current I _{OL}	0.4	0, 5	5	1.6	3.2	—	1.6	3.2	—	mA
	0.5	0, 10	10	2.6	5.2	—	—	—	—	
Output High Drive (Source) Current I _{OH}	4.6	0, 5	5	-1.15	-2.3	—	-1.15	-2.3	—	mA
	9.5	0, 10	10	-2.6	-5.2	—	—	—	—	
Output Voltage Low-Level V _{OL} †	—	0, 5	5	—	0	0.1	—	0	0.1	V
	—	0, 10	10	—	0	0.1	—	—	—	
Output Voltage High Level V _{OH} †	—	0, 5	5	4.9	5	—	4.9	5	—	
	—	0, 10	10	9.9	10	—	—	—	—	
Input Low Voltage V _{IL}	0.5,4,5	—	5	—	—	1.5	—	—	1.5	V
	0.5,9,5	—	10	—	—	3	—	—	—	
Input High Voltage V _{IH}	0.5,4,5	—	5	3.5	—	—	3.5	—	—	V
	0.5,9,5	—	10	7	—	—	—	—	—	
Input Leakage Current I _{IN}	Any Input	0, 5	5	—	—	±1	—	—	±1	μA
		0, 10	10	—	—	±2	—	—	—	
3-State Output Leakage Current I _{OUT}	0, 5	0, 5	5	—	±10 ⁻⁴	±1	—	±10 ⁻⁴	±1	μA
	0, 10	0, 10	10	—	±10 ⁻⁴	±10	—	—	—	
Input Capacitance C _{IN}	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance C _{OUT}	—	—	—	—	10	15	—	10	15	
Operating Device Current I _{OPER} #			5	—	0.5	1.0	—	0.5	1.0	mA
			10	—	1.9	3.0	—	—	—	

* Typical values are for T_A=25°C and nominal V_{DD}. † I_{OL}=I_{OH}=1 μA.

Operating current measured under worst-case conditions in a 3.2-MHz CDP1802A system: one PIC access per instruction cycle.

OPERATING CONDITIONS at T_A =Full Package-Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1877		CDP1877C		
	Min.	Max.	Min.	Max.	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	VSS	VDD	VSS	VDD	

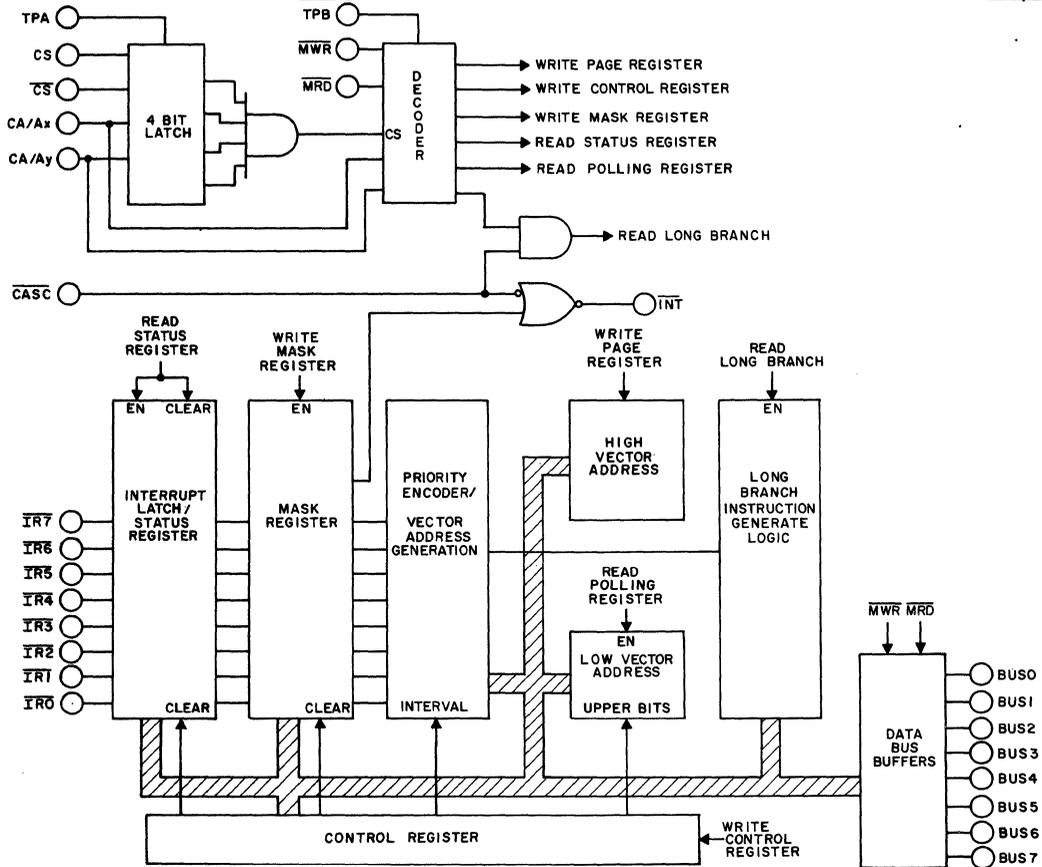


Fig. 1 - Functional diagram for CDP1877.

92CL-34372

Functional Definitions for CDP1877 and CDP1877C Terminals

TERMINAL	USAGE	TYPE
VDD-VSS	Power	
BUS0-BUS7	Data bus—Communicates information to and from CPU	Bidirectional
IR0-IR7	Interrupt Request Lines	Input
INTERRUPT	Interrupt to CPU	Output
MRD, MWR	Read/Write controls from CPU	Input
TPA, TPB	Timing pulses from CPU	Input
CS, CS-bar	Chip selects, Enable Chip if valid during TPA	Input
CS/Ax, CS/Ay	Used as a Chip Select during TPA and as a Register address during Read/Write Operations	Input
CASCADE	Used for cascading several PIC units. The INTERRUPT output from a higher priority PIC can be tied to this input, or the input can be tied to VDD if cascading is not used.	Input

RCA CMOS LSI Products

CDP1877, CDP1877C

PIC Programming Model

INTERNAL REGISTERS

The PIC has three write-only programmable registers and two read-only registers.

Page Register

This write only register contains the high order vector address the device will issue in response to an interrupt request. This high-order address will be the same for any of

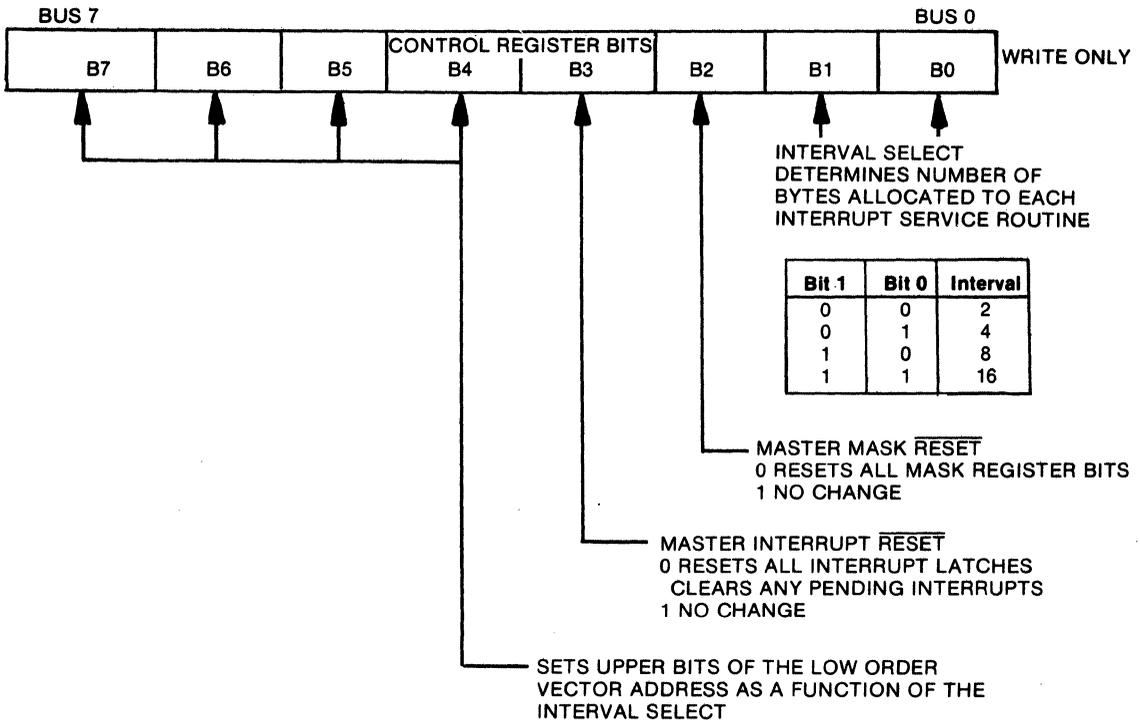
the 8 possible interrupt requests; thus, interrupt vectoring differs only in location within a specified page.



Control Register

The upper nibble of this write-only register contains the low order vector address the device will issue in response to an

interrupt request. The lower nibble is used for a master interrupt reset, master mask reset and for interval select.



THE LOW ORDER VECTOR ADDRESS WILL BE SET ACCORDING TO THE TABLE BELOW:

INTERVAL SELECTED- NO. OF BYTES	LOW ADDRESS BITS			
	BIT B7	BIT B6	BIT B5	BIT B4
2	SETS A7	SETS A6	SETS A5	SET A4
4	SETS A7	SETS A6	SETS A5	X
8	SETS A7	SETS A6	X	X
16	SETS A7	X	X	X

X=DON'T CARE

NOTE: All DON'T CARE Addresses and Addresses A0-A3 are determined by interrupt request.

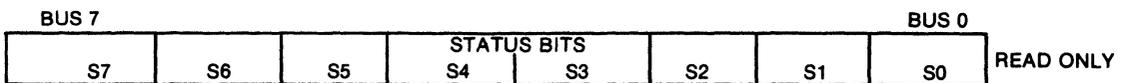
Mask Register

A "1" written into any location in this write only register will mask the corresponding interrupt request line. All interrupt inputs (except CASCADE) are maskable.



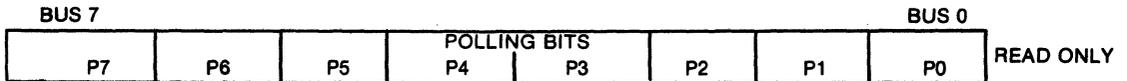
Status Register

In this read only register a "1" will be present in the corresponding bit location for every masked or unmasked pending interrupt.



Polling Register

This read only register provides the low order vector address and is used to identify the source of interrupt if a polling technique, rather than interrupt servicing, is used.

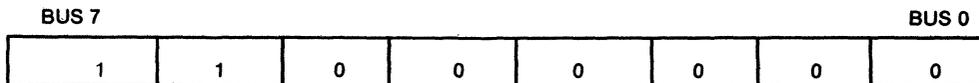


RESPONSE TO INTERRUPT (AFTER S3 CYCLE)

The PIC's response to interrogation by the CPU is always 3 bytes long, placed on the data bus in consecutive bytes in the following format:

First (Instruction) Byte:

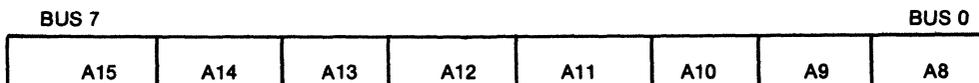
LONG BRANCH INSTRUCTION - CO (Hex)



Second (High-Order Address) Byte

This byte is the High-Order vector Address that was written into the PIC's Page Register by the user. The PIC does not alter this value in any way.

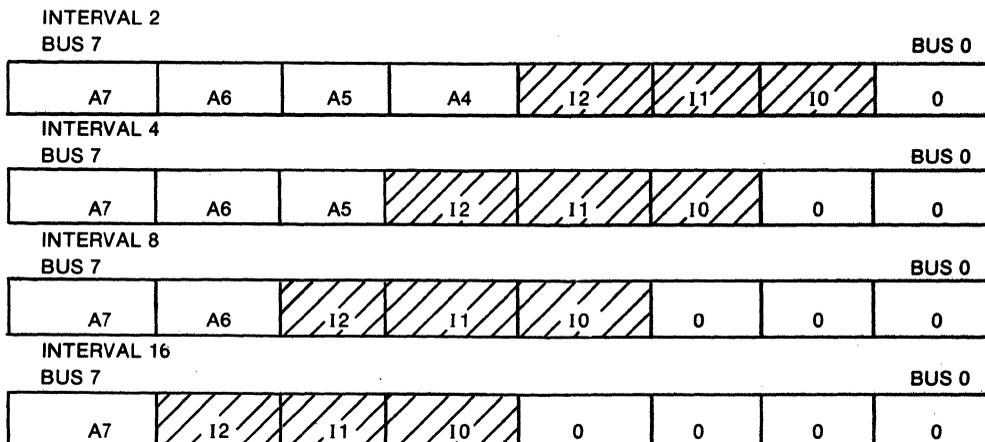
High-Order Vector Address



RCA CMOS LSI Products

CDP1877, CDP1877C

Third (Low-Order Address) Bytes



Indicates active interrupt input number (binary 0 to 7).

Bits indicated by Ax (x=4 to 7) are the same as programmed into the Control Register. All other bits are generated by the PIC.

REGISTER ADDRESSES

In order to read/write or obtain an interrupt vector from any PIC in the system, all chip selects (CS/Ax, CS/Ay, CS, \overline{CS}) must be valid during TPA.

CS/Ax and CS/Ay are multiplexed addresses; both must be high during TPA, and set according to this table during TPB to access the proper register.

CS/Ax	CS/Ay	\overline{RD}	\overline{WR}	ACTION TAKEN
1	0	0	1	READ Long Branch instruction and vector for highest priority unmasked interrupt pending.
1	0	1	0	WRITE to Page Register
0	1	1	0	WRITE to Control Register
0	0	0	1	READ Status Register
0	0	1	0	WRITE to Mask Register
0	1	0	1	READ Polling Register (Used to identify INTERRUPT source if Polling technique rather than INTERRUPT service is used.)
1	1	X	X	Unused condition

PIC Application Examples

Example I—Single PIC Application

Fig. 2 shows all the connections required between CPU and PIC to handle eight levels of interrupt control.

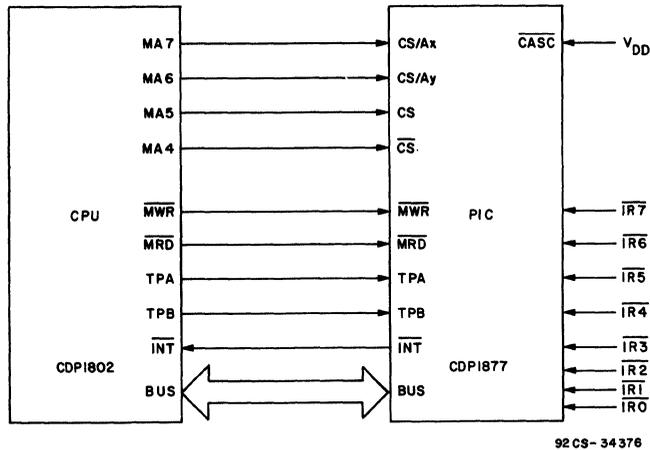


Fig. 2 - PIC and CPU connection diagram.

Programming

Programming the PIC consists of the following steps:

1. Disable interrupt at CPU.
2. Reset Master Interrupt Bit, B3, of Control Register.
3. Write a "1" into the Interrupt Input bit location of the Mask Register, if masking is desired.
4. Write the High-Order Address byte into the Page Register.
5. Write the Low-Order Address and the vector interval into the Control Register.
6. Program R(1) of the CPU to point to the PIC so that the Long Branch instruction can be read from the PIC during the Interrupt Service routine.

Values for Example I with LOCATION 8400 arbitrarily chosen as the Vector Address with interval of eight bytes, IR4 pending, is shown in Table I.

In deriving the above addresses, all DON'T CARE bits are assumed to be 0.

When an INTERRUPT (IR4) is received by the CPU, it will address the PIC and will branch to the interrupt service routine.

The three bytes generated by the PIC will be:

- 1st Byte=CO_H
- 2nd Byte=84_H
- 3rd Byte=EO_H

Table I — Register Address Values

REGISTER	REGISTER ADDRESS	OPERATION	DATA BYTE
MASK	E000H	WRITE	00 _H
CONTROL	E040H	WRITE	CE _H
PAGE	E080H	WRITE	84 _H
STATUS	E000H	READ	10 _H
POLLING	E040H	READ	20 _H
R(1) (IN CPU)	E080H	—	—

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Example II—Multi-PIC Application

Fig. 3 shows all the connections required between CPU and PICs to handle sixteen levels of interrupt control.

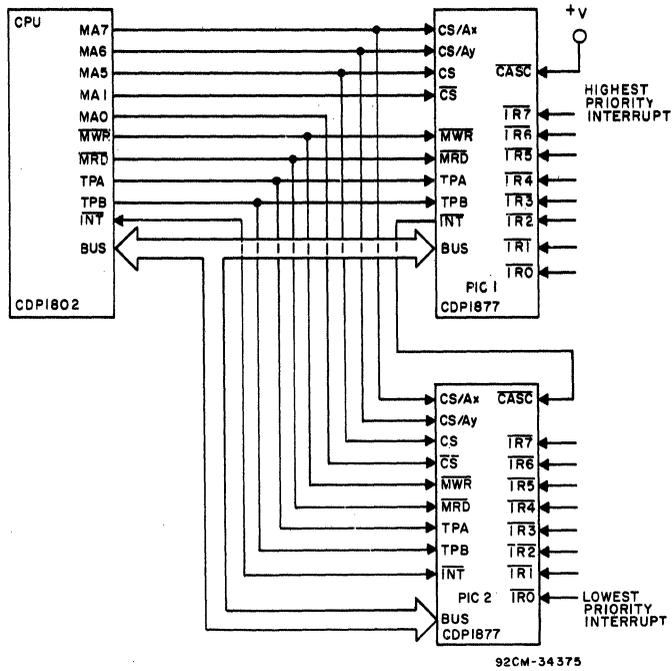


Fig. 3 - PICs and CPU connection diagram.

Register Address Assignments

The low-byte register address for any WRITE or READ operation is the same as shown in Table I.

The high-byte register differs for each PIC because of the linear addressing technique shown in the example:

- PIC 1=111XXX01 (E1H FOR X=0)
- PIC 2=111XXX10 (E2H FOR X=0)

The R(1) vector address is unchanged. This address will select both PICs simultaneously (R(1).1=111XXX00=E0H). Internal CDP1877 logic controls which PIC will respond when an interrupt request is serviced.

Additional PIC Application Comments

The interval select options provide significant flexibility for interrupt routine memory allocations:

- The 2-byte interval allows one to dedicate a full page to interrupt servicing, with variable space between routines, by specifying indirect vectoring with 2 byte short branch instructions on the current page.
- The 4-byte interval allows for a 3 byte long branch to any location in memory where the interrupt service

routine is located. The branch can be preceded by a Save Instruction to save previous contents of X and P on the stack.

- The 8-byte and 16-byte intervals allow enough space to perform a service routine without indirect vectoring. The amount of interval memory can be increased even further if all 8 INTERRUPTS are not required. Thus a 4-level interrupt system could use alternate TR Inputs, and expand the interval to 16 and 32 bytes, respectively.

The 4 Chip Selects allow one to conserve total allotted memory space to the PIC. For one chip, a total of 4 address lines could be used to select the device, mapping it into as little as 4-K of memory space. Note that this selection technique is the only one that allows the PIC to work properly in the system: I/O mapping cannot be used because the PIC must work within the CDP1800 interrupt structure to define the vector address. Decoded signals also will not work because the chip selects must be valid on the trailing edge of TPA.

1800-Series Peripherals
CDP1877, CDP1877C

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} \pm 5\%$, $t_r, t_f = 20$ ns,
 $V_{IH} = 0.7 V_{DD}$, $V_{IL} = 0.3 V_{DD}$, $C_L = 50$ pF

CHARACTERISTIC	V _{DD} (V)	LIMITS						UNITS
		CDP1877			CDP1877C			
		Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Address to TPA Setup Time	5	60	—	—	60	—	—	ns
	10	40	—	—	—	—	—	
Address to TPA Hold Time	5	60	—	—	60	—	—	
	10	40	—	—	—	—	—	
Data Valid after TPB	5	370	—	—	370	—	—	
	10	210	310	—	—	—	—	
Data Hold Time from Write	5	30	—	—	30	—	—	
	10	40	—	—	—	—	—	
Address to Valid Data Access Time	5	—	340	490	—	340	490	
	10	—	125	230	—	—	—	
Data Setup Time to Write	5	0	—	—	0	—	—	
	10	0	—	—	—	—	—	
Address Hold from TPB	5	80	—	—	80	—	—	
	10	40	—	—	—	—	—	
Minimum $\overline{\text{MWR}}$ Pulse Width	5	130	—	—	130	—	—	
	10	60	—	—	—	—	—	
Minimum $\overline{\text{IRX}}$ Pulse Width	5	130	—	—	130	—	—	
	10	60	—	—	—	—	—	

* Typical values are for $T_A = 25^\circ\text{C}$ and $V_{DD} \pm 5\%$.

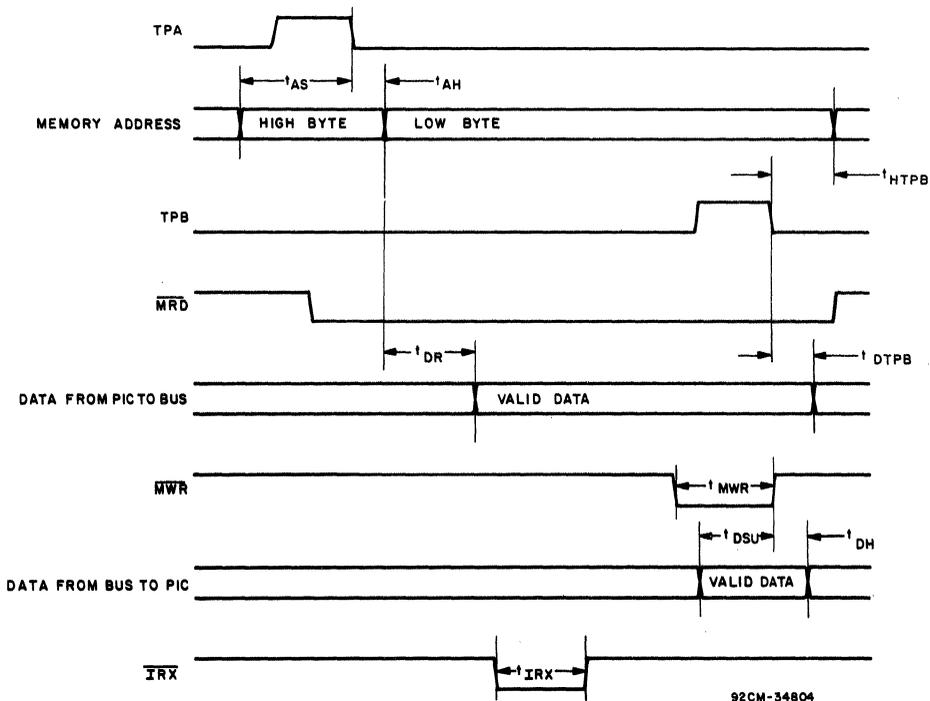
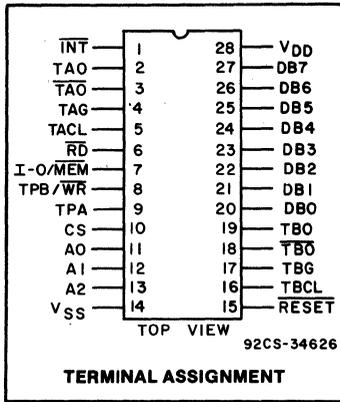


Fig. 4 - Timing waveforms for CDP1877.

CMOS Dual Counter-Timer



Features:

- Compatible with general-purpose and CDP1800-series microprocessor systems
- Two 16-bit down-counters and two 8-bit control registers
- 5 modes including a versatile variable-duty cycle mode
- Programmable gate-level select
- Two-complemented output pins for each counter-timer
- Software-controlled interrupt output
- Addressable in memory space or CDP1800-series I/O space

The RCA-CDP1878 and CDP1878CA are dual counter-timers consisting of two 16-bit programmable down counters that are independently controlled by separate control registers. The value in the registers determine the mode of operation and control functions. Counters and registers are directly addressable in memory space by any general-industry-type microprocessors, in addition to input/output mapping with the CDP1800-series microprocessors.

Each counter-timer can be configured in five modes with the additional flexibility of gate-level control. The control registers in addition to mode formatting, allow software start and stop, interrupt enable, and an optional read control that allows a stable readout from the counters. Each

counter-timer has software control of a common interrupt output with an interrupt status register indicating which counter-timer has timed out.

In addition to the interrupt output, true and complemented outputs are provided for each counter-timer for control of peripheral devices.

The CDP1878 and CDP1878C are functionally identical. They differ in that the CDP1878 has a recommended operating voltage range of 4 to 10.5 volts, and the CDP1878C has a recommended operating voltage range of 4 to 6.5 volts. These types are supplied in 28-lead dual-in-line ceramic packages (D suffix), and 28-lead dual-in-line plastic packages (E suffix).

▲Formerly RCA Dev. Type No. TA10981 and TA10981C, respectively.

Table I - Mode Description

Mode	Function	Application
1 Timeout	Outputs change when clock decrements counter to "0"	Event counter
2 Timeout Strobe	One clockwide output pulse when clock decrements counter to "0"	Trigger pulse
3 Gate-Controlled One Shot	Outputs change when clock decrements counter to "0". Retriggerable	Time-delay generation
4 Rate Generator	Repetitive clockwide output pulse	Time-base generator
5 Variable-Duty Cycle	Repetitive output with programmed duty cycle	Motor control

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltage referenced to V_{SS} terminal)

CDP1878	-0.5 to +11 V
CDP1878C	-0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to V _{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P _D):	
For T _A =-40 to +60° C (PACKAGE TYPE E)	500 mW
For T _A =+80 to +85° C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T _A =-55 to +100° C (PACKAGE TYPE D)	500 mW
For T _A =+100 to 125° C (PACKAGE TYPE D)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
For T _A =FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T _A):	
PACKAGE TYPE D	-55 to +125° C
PACKAGE TYPE E	-40 to +85° C
STORAGE-TEMPERATURE RANGE (T _{stg})	
-65 to +150° C	
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265° C

STATIC ELECTRICAL CHARACTERISTICS at T_A=-40 to +85° C, V_{DD} ±5%, Except as noted

CHARACTERISTIC		CONDITIONS			LIMITS						UNITS
		V _O (V)	V _{IN} (V)	V _{DD} (V)	CDP1878			CDP1878C			
					Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device Current	I _{DD}	—	0, 5	5	—	0.01	50	—	0.02	200	μA
		—	0, 10	10	—	1	200	—	—	—	
Output Low Drive (Sink) Current	I _{OL}	0.4	0, 5	5	1.6	3.2	—	1.6	3.2	—	mA
		0.5	0, 10	10	2.6	5.2	—	—	—	—	
Output High Drive (Source) Current	I _{OH}	4.6	0, 5	5	-1.15	-2.3	—	-1.15	-2.3	—	mA
		9.5	0, 10	10	-2.6	-5.2	—	—	—	—	
Output Voltage Low-Level	V _{OL} ‡	—	0, 5	5	—	0	0.1	—	0	0.1	V
		—	0, 10	10	—	0	0.1	—	—	—	
Output Voltage High Level	V _{OH} ‡	—	0, 5	5	4.9	5	—	4.9	5	—	V
		—	0, 10	10	9.9	10	—	—	—	—	
Input Low Voltage	V _{IL}	0.5, 4.5	—	5	—	—	1.5	—	—	1.5	V
		0.5, 9.5	—	10	—	—	3	—	—	—	
Input High Voltage	V _{IH}	0.5, 4.5	—	5	3.5	—	—	3.5	—	—	V
		0.5, 9.5	—	10	7	—	—	—	—	—	
Input Leakage Current	I _{IN}	Any	0, 5	5	—	—	±1	—	—	±1	μA
		Input	0, 10	10	—	—	±2	—	—	—	
Operating Current	I _{DD1} ^Δ	—	0, 5	5	—	1.5	3	—	1.5	3	mA
		—	0, 10	10	—	6	12	—	—	—	
Input Capacitance	C _{IN}	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance	C _{OUT}	—	—	—	—	10	15	—	10	15	

*Typical values are for T_A=25° C and nominal V_{DD}. ‡I_{OL}=I_{OH}=1 μA.

ΔOperating current is measured at 200 kHz for V_{DD}=5 V and 400 kHz for V_{DD}=10 V, with open outputs (worst-case frequencies for CDP1802A system operating at maximum speed of 3.2 MHz).

CDP1878, CDP1878C

OPERATING CONDITIONS at T_A =Full Package-Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1878		CDP1878C		
	Min.	Max.	Min.	Max.	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	
Maximum Clock Input Rise or Fall Time t_{r,t_f}	—	5	—	5	μs
Minimum Clock Pulse Width t_{WL}, t_{WH}	200	—	200	—	ns
Maximum Clock Input Frequency, f_{CL}	DC	2	DC	2	MHz

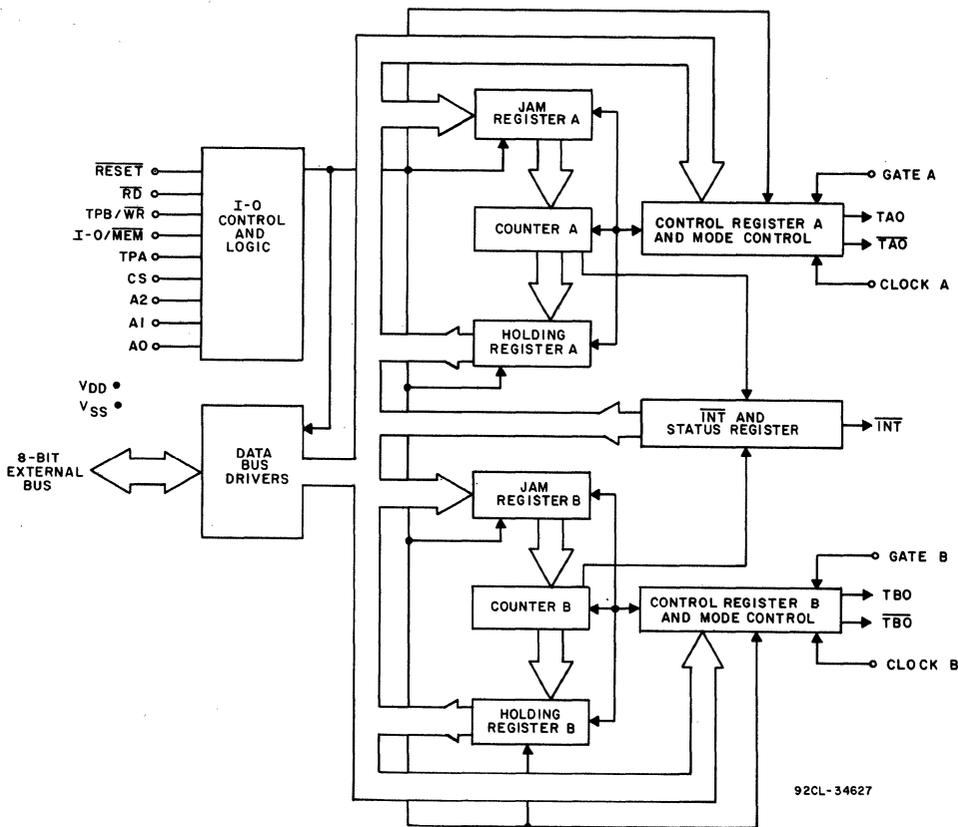


Fig. 1 - Functional diagram CDP1878 and CDP1878C.

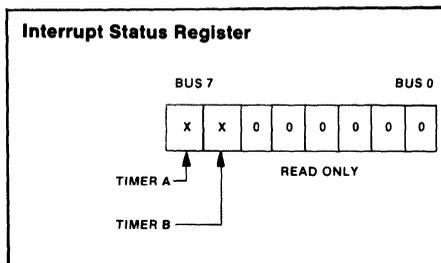
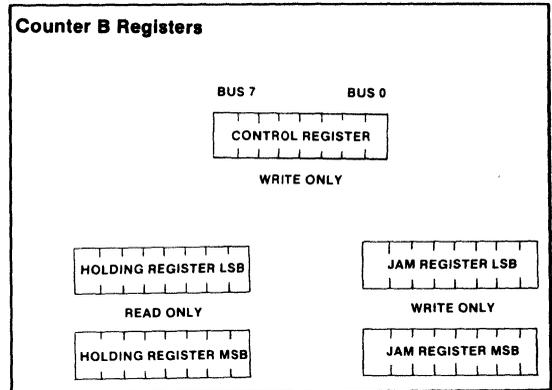
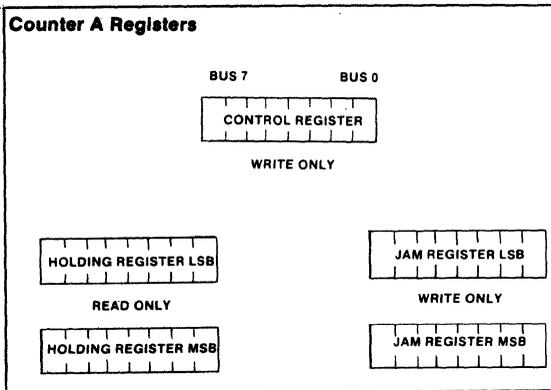
Functional Definitions for CDP1878 and CDP1878C Terminals

TERMINAL	USAGE	TERMINAL	USAGE
VDD-VSS	Power	CS	Active high input that enables device
DB0-DB7	Data to and from device	\overline{INT}	Low when counter is "0"
TPB/ \overline{WR} , RD	Directional control signals	RESET	When active, TAO, TBO are low, \overline{TAO} , \overline{TBO} are high. Interrupt status register is cleared
A0, A1, A2	Addresses that select counters or registers	I-O/ \overline{MEM}	Tied high in CDP1800 input/output mode, otherwise tied low
TACL, TBCL	Clocks used to decrement counters		
TAG, TBG	Gate inputs that control counters		
TAO, \overline{TAO}	Complemented outputs of Timer A		
TBO, \overline{TBO}	Complemented outputs of Timer B		
TPA	Used with CDP1800-series processors, tied high otherwise		

REGISTER TRUTH TABLE

ADDRESS			ACTIVE		REGISTER OPERATION
A2	A1	A0	TPB/ $\overline{\text{WR}}$	$\overline{\text{RD}}$	
1	1	0	X		Write Counter A MSB
1	1	0		X	Read Counter A MSB
0	1	0	X		Write Counter A LSB
0	1	0		X	Read Counter A LSB
1	0	0	X		Control Register A
1	1	1	X		Write Counter B MSB
1	1	1		X	Read Counter B MSB
0	1	1	X		Write Counter B LSB
0	1	1		X	Read Counter B LSB
1	0	1	X		Control Register B
1	0	0		X	Interrupt Status Register
1	0	1		X	
0	0	0			Not Used
0	0	1			Not Used

PROGRAMMING MODEL



CDP1878, CDP1878C

Functional Description—See Fig. 1

The dual counter-timer consists of two programmable 16-bit down counters, separately addressable and controlled by two independent 8-bit control registers. The word in the control register determines the mode and type of operation that the counter-timer performs. Writing to or reading from a counter or register is enabled by selective addressing during a write or read cycle. The data is placed on the data bus by the microprocessor during the write cycle or read from the counter during the read cycle. Data to and from the counters and to the control registers is in binary format.

Each counter-timer consists of three parts. The first is the counter itself, a 16-bit down counter that is decremented on the trailing edge of the clock input. The second is the jam register that receives the data when the counter is written to. The word in the control register determines when the jam register value is placed into the counter. The third part is the holding register that places the counter value on the data bus when the counter is read.

When the counter has decremented to zero, three events occur. The first involves the common interrupt output pin that, if enabled, becomes active low. The second is the setting of a bit in the interrupt status register. This register can be read to determine which counter-timer has timed out. The third event is the logic change of the complemented output pins.

In addition to the clock input used to decrement the counter, a gate input is available to enable or initiate operation. The counter-timers are independent and can have different mode operations.

Write Operation

The counters and registers are separately addressable and are programmed via the data bus when the chip is selected with the TPB/ \overline{WR} pin active. Normal sequencing requires that the counter jam register be loaded first with the

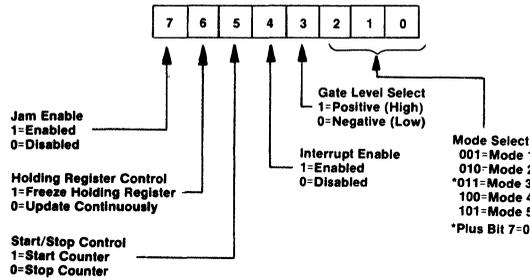
required value (most significant and least significant byte in any order), and then the control register be accessed and loaded with the control word. The trailing edge of the TPB/ \overline{WR} pulse will latch the control word into the control register and cause the counter to be jammed with its initial value. The counter will decrement on the trailing edge of succeeding clocks until it reaches zero. The output levels will then change, and if enabled, the interrupt output will become active and the appropriate timer bit will be set in the interrupt status register. The interrupt output and the interrupt status register can be cleared (to their inactive state) by addressing the control register with the TPB/ \overline{WR} line active. For example, if counter A times out, control register A must be accessed to reset the interrupt output high and reset the timer A bit in the status register low. Timer B bit in the status register will be unaffected.

Read Operation

Each counter has a holding register that is continuously being updated by the counter and is accessed when the counter is addressed during read cycles. Counter reads are accomplished by halting the holding register and then reading it, or by reading the holding register directly. If the holding register is read directly, data will appear on the bus if the counters are addressed with the \overline{RD} line active. However, if the clock decrements the counter between the two read operations (most and least significant byte), an inaccurate value will be read. To preclude this from happening, writing a "1" into bit 6 of the control register and then addressing and reading the counter will result in a stable reading. This operation prevents the holding register from being updated by the counter and does not affect the counter's operation.

The interrupt status register is read by addressing either control register with the \overline{RD} line active. A "1" in bit 7 indicates Timer A has timed out and a "1" in bit 6 indicates Timer B has timed out. Bits 0-5 are zeros.

Control Register



Bits 0, 1 and 2 — Mode Selects—See Mode Timing Diagrams (Figs. 2, 3, 4, 5 and 6).

	Bit 7	Bit 2	Bit 1	Bit 0
Mode 1 — Timeout	—	0	0	1
Mode 2 — Timeout Strobe	—	0	1	0
Mode 3 — Gate Controlled One Shot	0	0	1	1
Mode 4 — Rate Generator	—	1	0	0
Mode 5 — Variable-Duty Cycle	—	1	0	1
No Mode selected. Counter outputs unaffected.	—	0	0	0

Note: When selecting a mode, the timer outputs TAO and TBO are set low, and TAO and TBO are set high. If bits 0, 1 and 2 are all zero's when the control register is loaded, no

mode is selected, and the counter-timer outputs are unaffected.

Bit 3—Gate level select—All modes require an enabling signal on the gate to allow counter operation. This enabling signal is either a level or a pulse (edge). Positive gate level or edge enabling is selected by writing a “1” into this bit and negative (low) enabling is selected when bit 3 is “0”.

Bit 4—Interrupt enable—Setting this bit to “1” enables the $\overline{\text{INT}}$ output, and setting it to “0” disables it. When reset, the $\overline{\text{INT}}$ output is at a high level. If the interrupt enable bit in the control register is enabled and the counter decrements to zero, the $\overline{\text{INT}}$ output will go low and will not return high until the counter-timer is reset or the selected control register is written to. Example: If timer B times out, control register B must be accessed to reset the $\overline{\text{INT}}$ output high. If the interrupt enable bit is set to “0”, the counter’s timeout will have no effect on the $\overline{\text{INT}}$ output.

In mode 5, the variable-duty cycle mode, the $\overline{\text{INT}}$ pin will become active low when the MSB in the counter has decremented to zero.

Bit 5—Start/stop control—This bit controls the clock input to the counter and must be set to “1” to enable it. Writing a “0” into this location will halt operation of the counter. Operation will not resume until the bit is set to “1”.

Bit 6—Holding register control—Since the counter may be decrementing during a read cycle, writing a “1” into this location will hold a stable value in the hold register for subsequent read operations. Rewriting a “1” into bit 6 will cause an update in the holding register on the next trailing clock edge. If this location contains a “0”, the holding register will be updated continuously by the value in the counter.

Bit 7—Jam enable—When this bit is set to “1” during a write to the control register, the value in the jam register will be placed into the counter. The counter outputs TAO and TBO will be set high and $\overline{\text{TAO}}$ and $\overline{\text{TBO}}$ will be set low on the next trailing clock edge. Setting this bit to “0” will leave the counter value unaffected. This location should be set to “0” any time a write to the control register must be performed without changing the present counter value. Writing a “1” into bit 7 and zeros into bits 0, 1 and 2 (mode selects) will load the counter with the value in the jam register and start the counter in the mode previously selected.

In mode 3, the hardware start is enabled by writing a “0” into bit 7. If a “1” is written to bit 7, the timeout will start immediately and mode 3 will resemble mode 1.

MODE DESCRIPTIONS

Mode		Control Register	Gate Control								
1	Timeout	<table border="1" style="margin: auto;"> <tr> <td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>1</td> </tr> </table>	X	X	X	X	X	0	0	1	Selectable High or Low Level Enables Operation
		X	X	X	X	X	0	0	1		
BUS 7 BUS 0											

Mode 1:

After the count is loaded into the jam register and the control register is written to with the jam-enable bit high, TXO goes high and $\overline{\text{TXO}}$ goes low. The input clock decrements the counter. When it reaches zero, TXO goes low and $\overline{\text{TXO}}$ goes high, and if enabled, the interrupt output

is set low. Writing to the counter while it is decrementing has no effect on the counter value unless the control register is subsequently written to with the jam-enable bit high.

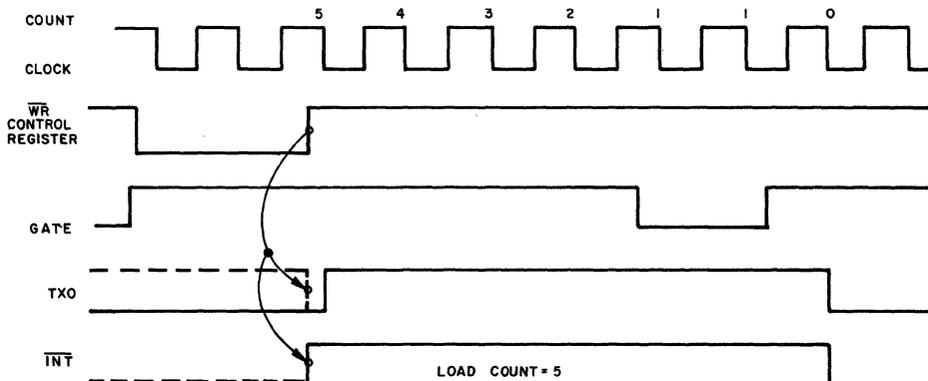


Fig. 2 - Timeout (mode 1) timing waveforms.

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Mode		Control Register	Gate Control								
2	Timeout Strobe	<table border="1" style="display: inline-table;"> <tr> <td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>1</td><td>0</td> </tr> </table>	X	X	X	X	X	0	1	0	Selectable High or Low Level Enables Operation
		X	X	X	X	X	0	1	0		
BUS 7	BUS 0										

Mode 2:

Operation of this mode is the same as mode 1, except the outputs will change for one clock period only and then

return to the condition of TXO high and $\overline{\text{TXO}}$ low.

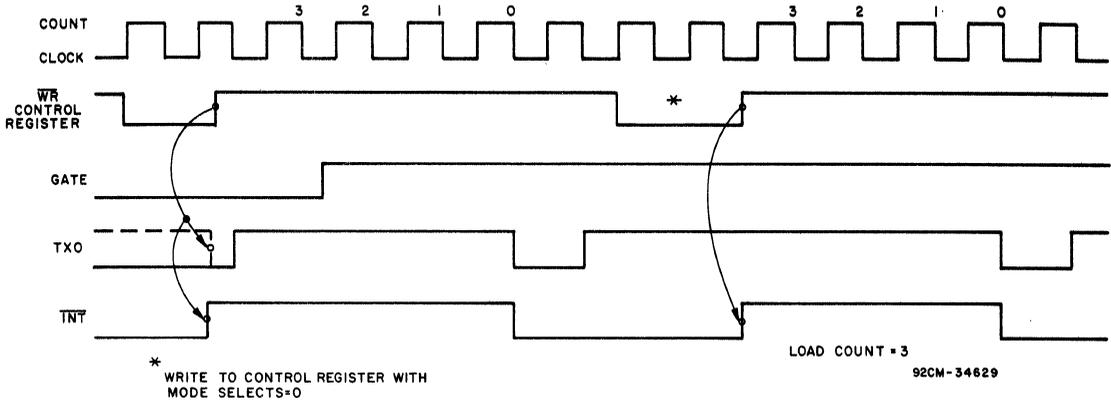


Fig. 3 - Timeout strobe (mode 2) timing waveforms.

Mode		Control Register	Gate Control								
3	Gate Controlled One Shot	<table border="1" style="display: inline-table;"> <tr> <td>0</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>1</td><td>1</td> </tr> </table>	0	X	X	X	X	0	1	1	Selectable Positive or Negative Going Edge Initiates Operation
		0	X	X	X	X	0	1	1		
BUS 7	BUS 0										

Mode 3:

After the jam register is loaded with the required value, the gate edge will initiate this mode. TXO will be set high, and $\overline{\text{TXO}}$ will be set low. The clock will decrement the counter. When zero is reached, TXO will go low and $\overline{\text{TXO}}$ will be high, and the interrupt output will be set low. The counter is

retriggerable: While the counter is decrementing, a gate edge or write to the control register with the jam-enable bit high, will load the counter with the jam register value and restart the one-shot operation.

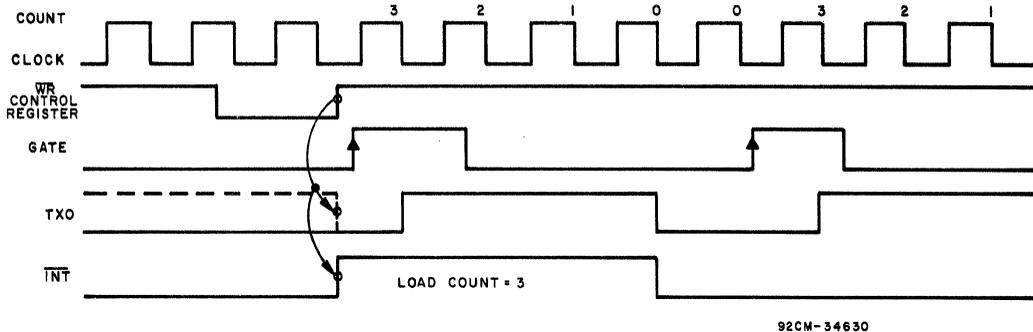


Fig. 4 - Gate controlled one-shot (mode 3) timing waveforms.

Mode	Control Register	Gate Control																
4	<table border="1"> <tr> <td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>1</td><td>0</td><td>0</td> </tr> <tr> <td colspan="5">BUS 7</td> <td colspan="3">BUS 0</td> </tr> </table>	X	X	X	X	X	1	0	0	BUS 7					BUS 0			Selectable High or Low Level Enables Operation
X	X	X	X	X	1	0	0											
BUS 7					BUS 0													

Mode 4:

A repetitive clock-wide output pulse will be output, with the time between pulses equal to the counter's value, (trailing edge to leading edge). This mode is software started with a write to the control register if the gate level is valid. If the counter is written to while decrementing, the new value will

not affect the counter's operation until the present timeout has concluded, unless the control register is written to with the jam-enable bit high. If the gate input (TAG or TBG) is used to start this mode. The first cycle following the gate going true is indeterminate.

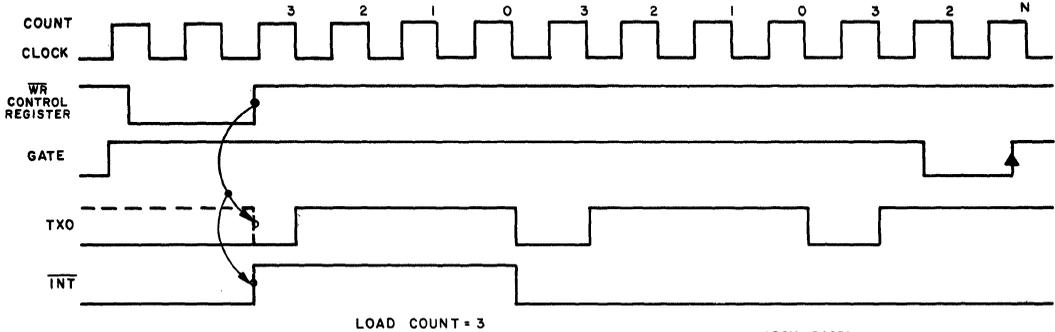


Fig. 5 - Rate generators (mode 4) timing waveforms.

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Mode	Control Register	Gate Control																
5	<table border="1"> <tr> <td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>1</td><td>0</td><td>1</td> </tr> <tr> <td colspan="5">BUS 7</td> <td colspan="3">BUS 0</td> </tr> </table>	X	X	X	X	X	1	0	1	BUS 7					BUS 0			Selectable High or Low Level Enables Operation
X	X	X	X	X	1	0	1											
BUS 7					BUS 0													

Mode 5:

After the mode is initiated, the outputs will remain at one level until the clock decrements the least significant byte of the counter to N+1. The outputs will then change level and the counter decrements the most significant byte to N+1. The process will then repeat, resulting in a repetitive output

with a duty cycle directly controlled by the value in the counter. The output period will be equal to $LSB+MSB+2$.

The interrupt output will become active after the MSB is loaded into the counter and decrements to zero.

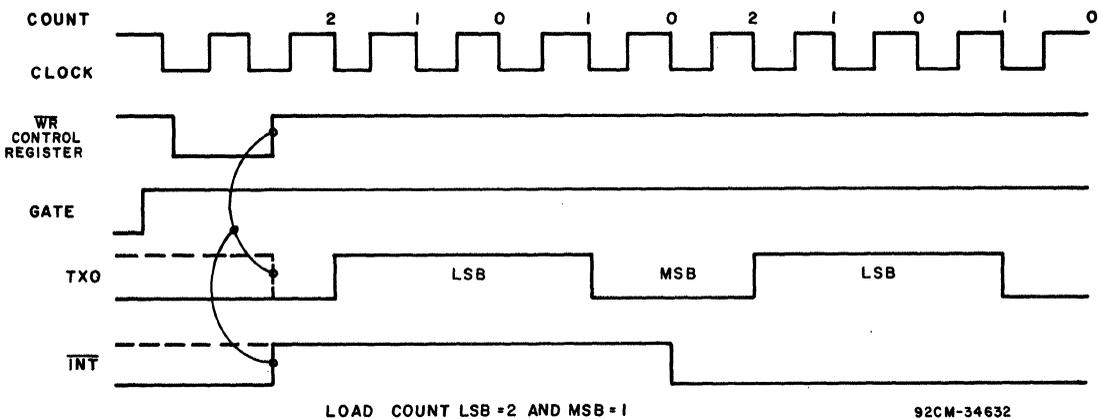


Fig. 6 - Variable-duty cycle (mode 5) timing waveforms.

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Note:

In order to avoid unwanted starts when selecting mode 3 or 4, the gate signal must be set to the opposite level that will be programmed.

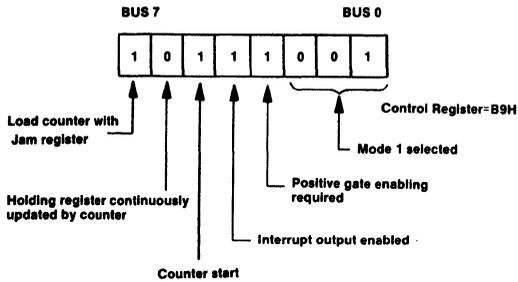
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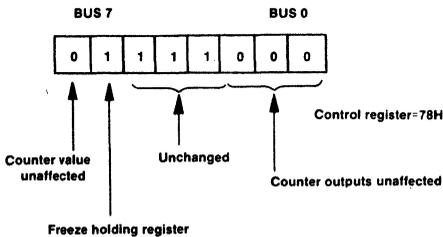
Setting the Control Register

The following will illustrate a counter write and subsequent reads that places stable, accurate values on the data bus from the counter-timer.

The counter is addressed and the required values are loaded with a write operation. The control register is addressed next and loaded with B9H.



The counter will now decrement with each input clock pulse. Assuming the counter has not decremented to zero and its value is to be read without affecting the counter's operation, a write to the control register is performed. 78H is loaded into the control register.



The counter is addressed and read operations are performed.

Function Pin Definition

DB7-DB0—8-bit bidirectional bus used to transfer binary information between the microprocessor and the dual counter-timer.

VDD, VSS—Power and ground for device.

A0, A1, and A2—Addresses used to select counters or registers.

TPB/ \overline{WR} , \overline{RD} —Directional signals that determine whether data will be placed on the bus from a counter or the interrupt status register (\overline{RD} active) (memory mapped), or data on the bus will be placed into a counter or control register (TPB/ \overline{WR} active). The following connections are required between the microprocessor and the counter-timer in the CDP1800-series input/output mapping mode.

Microprocessor	Counter-Timer
\overline{MRD}	\overline{RD}
TPB	TPB/ \overline{WR}
TPA	TPA
N Lines	Address Lines

and I-O/ \overline{MEM} to VDD.

During an output instruction, data from the memory is strobed into the counter-timer during TPB when \overline{RD} is active, and latched on TPB's trailing edge. Data is read from the counter-timer when \overline{RD} is not active between the trailing edges of TPA and TPB. (See Figs. 10, 11, and 12.)

TACL, TBCL—Clocks used to decrement the counter.

TAG, TBG—Gate inputs used to control counter.

TAO, \overline{TAO} —Complemented outputs of Timer A.

TBO, \overline{TBO} —Complemented outputs of Timer B.

\overline{INT} —Common interrupt output. Active when counter decrements to zero.

RESET—Active low signal that resets counter outputs (TAO, TBO low, \overline{TAO} , \overline{TBO} high). The interrupt output is set high and the status register is cleared.

I-O/ \overline{MEM} —Tied high in CDP1800-series input/output mode, otherwise tied low.

TPA—Tied to TPA of the CDP1800-series microprocessors. During memory mapping, it is used to latch the high order address bit for the chip select. In the CDP1800 input/output mode, it is used to gate the N lines. When the counter-timer is used with other microprocessors, or when the high order address of the CDP1800-series microprocessors is externally latched, it is connected to VDD.

CS—An active high signal that enables the device.

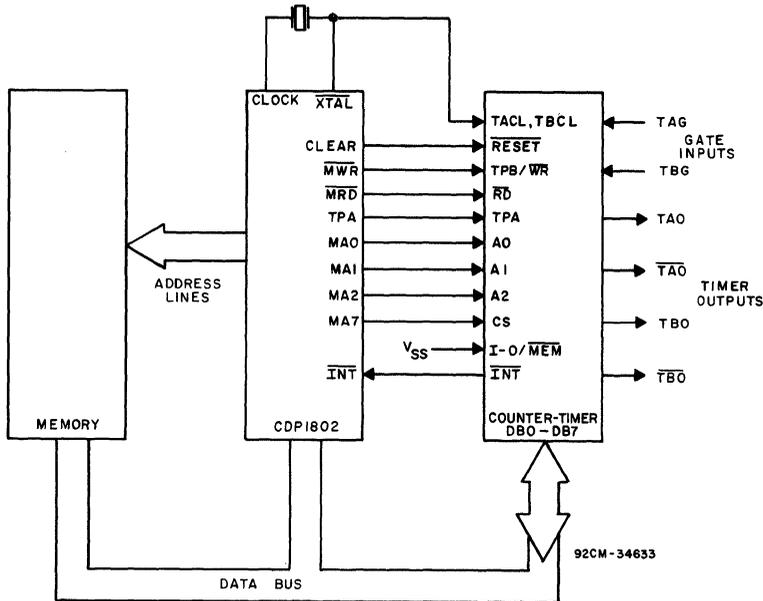


Fig. 7 - Typical CDP1802 memory-mapped system.

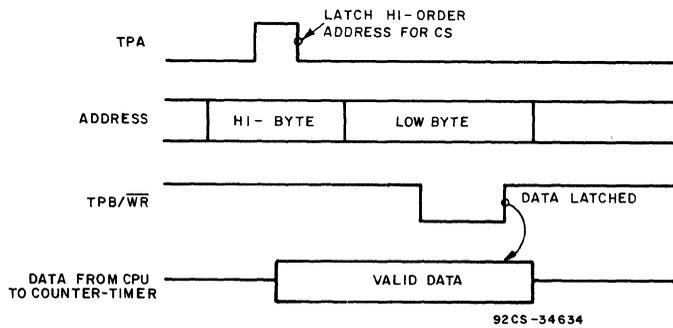


Fig. 8 - CDP1800-series memory-mapping write cycle timing waveforms.

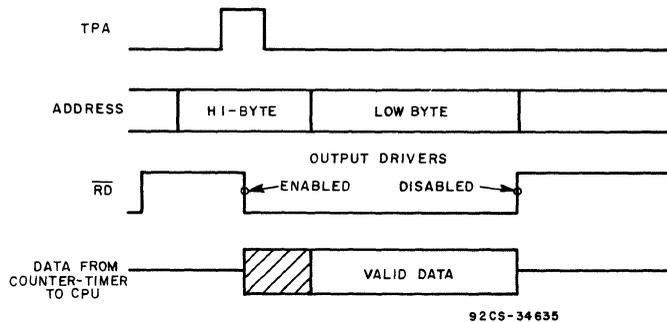


Fig. 9 - CDP1800-series memory-mapping read cycle timing waveforms.

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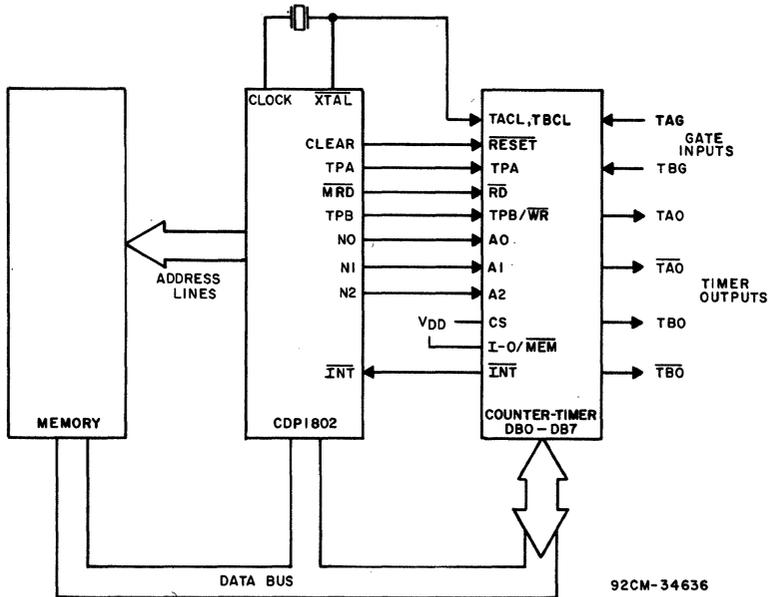


Fig. 10 - Typical CDP1802 input/output-mapped system.

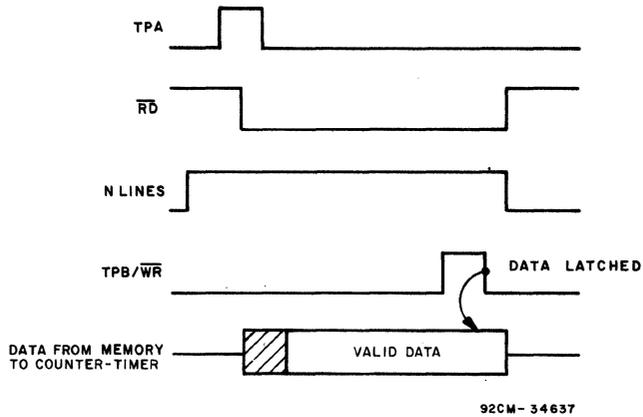


Fig. 11 - CDP1800-series input/output-mapping timing waveforms with output instruction.

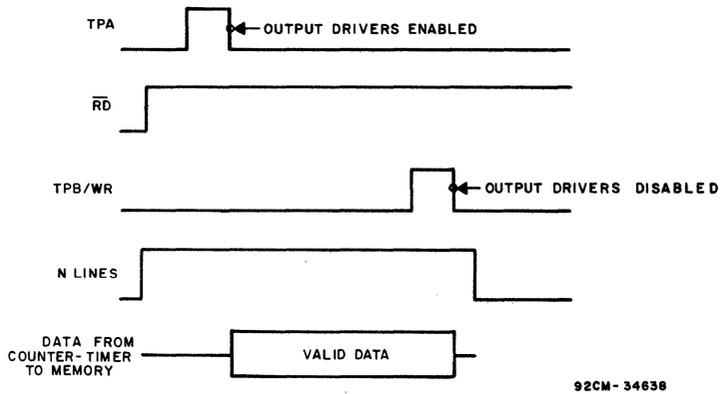


Fig. 12 - CDP1800-series input/output-mapping timing waveforms with input instruction.

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = 5\text{V} \pm 5\%$,
Input $t_r, t_f = 10\text{ ns}$; $C_L = 50\text{ pF}$ and 1 TTL Load

CHARACTERISTIC	LIMITS			UNITS	
	Min. [†]	Typ.*	Max.		
Read Cycle Times (see Fig. 13)					
Data Access from Address	t_{DA}	—	350	—	ns
Read Pulse Width	t_{RD}	400	—	—	
Data Access from $\overline{\text{Read}}$	t_{DR}	—	250	—	
Address Hold after $\overline{\text{Read}}$	t_{RH}	0	—	—	
Output Hold after $\overline{\text{Read}}$	t_{DH}	50	—	—	
Chip Select Setup to TPA	t_{CS}	50	—	—	

[†]Time required by a limit device to allow for the indicated function.

*Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .

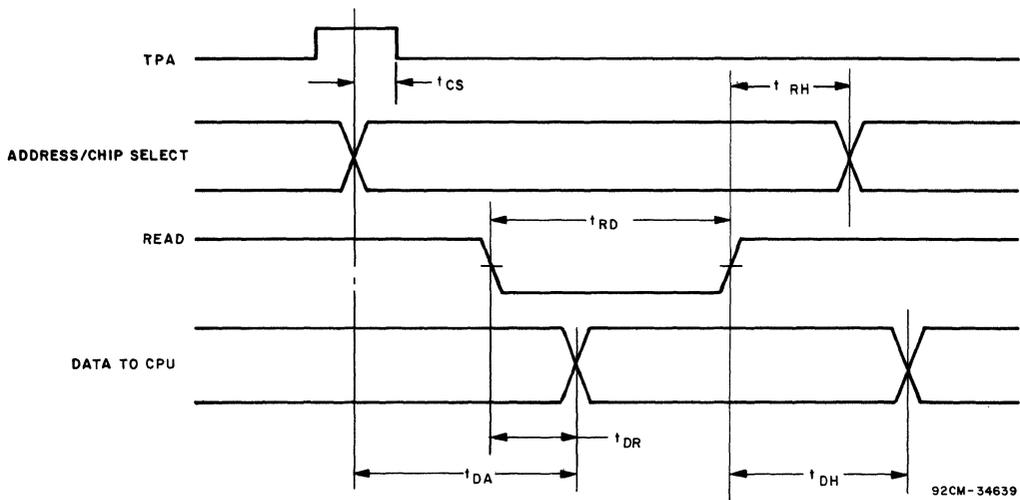


Fig. 13 - Read cycle timing waveforms.

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = 5\text{ V} \pm 5\%$,

Input $t_r, t_f = 10\text{ ns}$; $C_L = 50\text{ pF}$ and 1 TTL Load

CHARACTERISTIC	LIMITS			UNITS	
	Min.†	Typ.*	Max.		
Write Cycle Times (see Fig. 14)					
Address Setup to Write	t_{AS}	150	—	—	ns
Write Pulse Width	t_{WR}	150	—	—	
Data Setup to Write	t_{DS}	200	—	—	
Address Hold after Write	t_{AH}	50	—	—	
Data Hold after Write	t_{WH}	50	—	—	
Chip Select Setup to TPA	t_{CS}	50	—	—	

†Time required by a limit device to allow for the indicated function.

*Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .

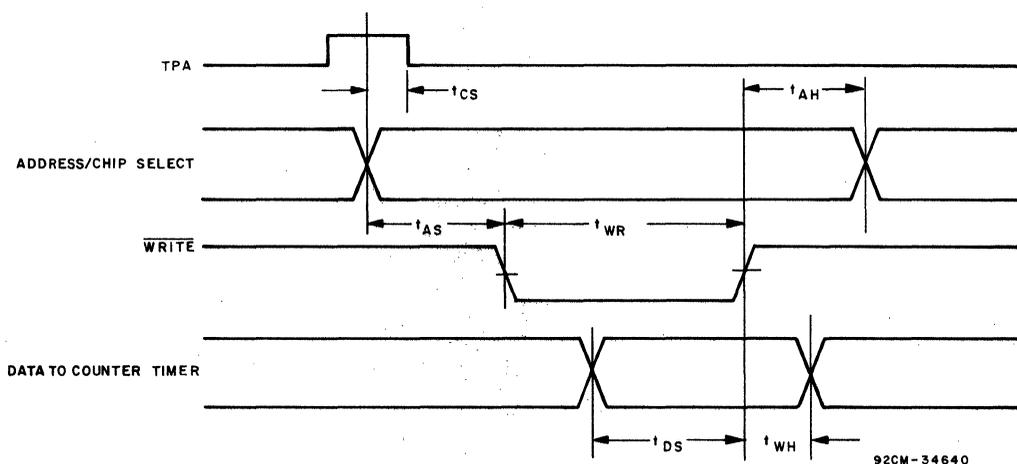


Fig. 14 - Write cycle timing waveforms.

OPERATING AND HANDLING CONSIDERATIONS

1. Handling

All inputs and outputs of RCA CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in ICAN-6525, "Guide to Better Handling and Operation of CMOS Integrated Circuits."

2. Operating

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not

cause $V_{DD} - V_{SS}$ to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{CC} nor less than V_{SS} . Input currents must not exceed 10 mA even when the power supply is off.

Unused Inputs

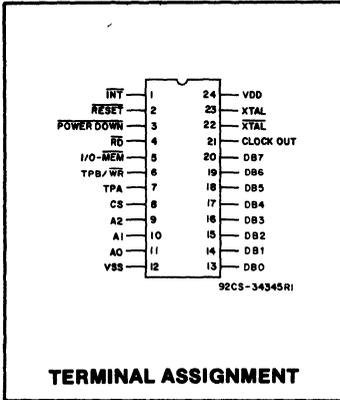
A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{CC} or V_{SS} , whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} , V_{CC} , or V_{SS} may damage CMOS devices by exceeding the maximum device dissipation.

Objective Data

CMOS Real-Time Clock



Features

- Time of day/calendar
- Reads seconds, minutes, hours
- Reads day of month and month
- Alarm circuit with seconds, minutes or hours operation
- Power down mode
- Separate clock output selects 1 of 15 square wave signals
- Interrupt output activated by clock output and/or alarm circuit
- Data integrity sampling for clock rollover eliminated
- On board oscillator
- One of four crystal frequency operation
- Addressable in memory space or CDP1800 series I/O mode

The CDP1879 real-time clock supplies time and calendar information in BCD format from seconds to months. It consists of 5 separately addressable and programmable counters that divide down an oscillator input. The frequency of the oscillator is determined by one of four possible external crystals.

The device is memory-mapped by any general-purpose microprocessor with the additional capability of operating in the CDP1800-series input/output mode.

The real-time clock functions as a time-of-day/calendar with an alarm capability that can be set for combinations of seconds, minutes or hours. Alarm time is configured by loading alarm latches that activate an interrupt output through a comparator when the counter and alarm latch values are equal.

Fifteen selectable square-wave signals are available as a separate clock output signal and also activate the interrupt output. A status register is available to indicate the interrupt source. The value in an 8-bit control register determines the operational characteristics of the device, by selecting the prescaler divisor and the clock output, and controls the load and alarm functions.

A transparent "freeze" circuit precludes clock rollover during counter and latch access times to assure stable and accurate values in the counters and alarm latches.

The CDP1879 is functionally identical to the CDP1879C. The CDP1879 has a recommended operating voltage range of 4 to 10.5 volts, and the CDP1879C has a recommended operating voltage range of 4 to 6.5 volts. The CDP1879 and the CDP1879C are supplied in 24 lead hermetic dual-in-line side-brazed ceramic packages (D suffix) and 24 lead dual-in-line plastic packages (E suffix).

CDP1879 MODES OF OPERATION

OPERATION	FUNCTION
Read	<ol style="list-style-type: none"> 1. Seconds, minutes, hours, date and month counters 2. Status register to identify interrupt source
Write	<ol style="list-style-type: none"> 1. Control register to set device operation 2. Seconds, minutes, hours, date and month counters 3. Alarm latches for alarm time
Power Down	Tri-state bus with active alarm or clock out circuitry for wake up control
Interrupt	<ol style="list-style-type: none"> 1. Clock out as source 2. Alarm time as source 3. Either interrupt can occur during normal or power down mode

CDP1879, CDP1879C

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltage referenced to V_{SS} Terminal)

CDP1879 -0.5 to +11 V
CDP1879C -0.5 to +7 V

INPUT VOLTAGE RANGE, ALL INPUTS -0.5 to V_{DD} +0.5 V

DC INPUT CURRENT, ANY ONE INPUT ±10 mA

POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) Derate Linearly at 12 mW/°C to 200 mW
For T_A = -55 to 100°C (PACKAGE TYPE D) 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE D) Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 40 mW

OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE D, H -55 to +125°C
PACKAGE TYPE E -40 to +85°C

STORAGE TEMPERATURE RANGE (T_{stg}) -65 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. +265°C

TABLE I

Control Register Bit Assignment		
BIT		
0.	Frequency 00	32768 Hz
1.	Select 01	1.048576 MHz
	10	2.097152 MHz
	11	4.194304 MHz
2.	Start/Stop	1 = Start 0 = Stop
3.	Counter/Latch Control	"0" = Write to counter & disable alarm "1" = Write to and enable alarm
4.	Clock Select	
5.	0000 — disable μs	1000 — 62.5 ms
6.	0001 — 488.2 μs	1001 — 125 ms
7.	0010 — 976.5 μs	1010 — 250 ms
	0011 — 1953.1 μs	1011 — 500 ms
	0100 — 3906.2 μs	1100 — sec.
	0101 — 7812.5 μs	1101 — min.
	0110 — 15.625 ms	1110 — hour
	0111 — 31.25 ms	1111 — day

TABLE II

	Pins
V _{DD} , V _{SS}	2
DB0-DB7	8
A0-A2	3
TPA	1
I-O/MEM	1
RD, TPB/WR	2
CS	1
INT	1
CLOCK	1
XTAL	1
XTAL	1
POWER DOWN	1
RESET	1
	24

TABLE III

Addresses	A2	A1	A0
Latch, Counter Seconds	0	1	0
Latch, Counter Minutes	0	1	1
Latch, Counter Hours	1	0	0
Counter, Day	1	0	1
Counter, Month	1	1	0
Control, Register	1	1	1
Status Register	1	1	1

MSB of hours counters (Bit 7) is an AM-PM bit. 0 = AM; 1 = PM.

Bit 6 of hours counter controls 12/24 hr. 1 = 12 hr; 0 = 24 hr.

Status Register: Bit 7 MSB = alarm

Interrupt Source: Bit 6 = clock

MSB of Month Counter (Bit 7) is a Leap Year Bit 0 = No, 1 = Yes.

OPERATING CONDITIONS at T_A = Full Package-Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1879		CDP1879C		
	Min.	Max.	Min.	Max.	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	VSS	VDD	VSS	VDD	

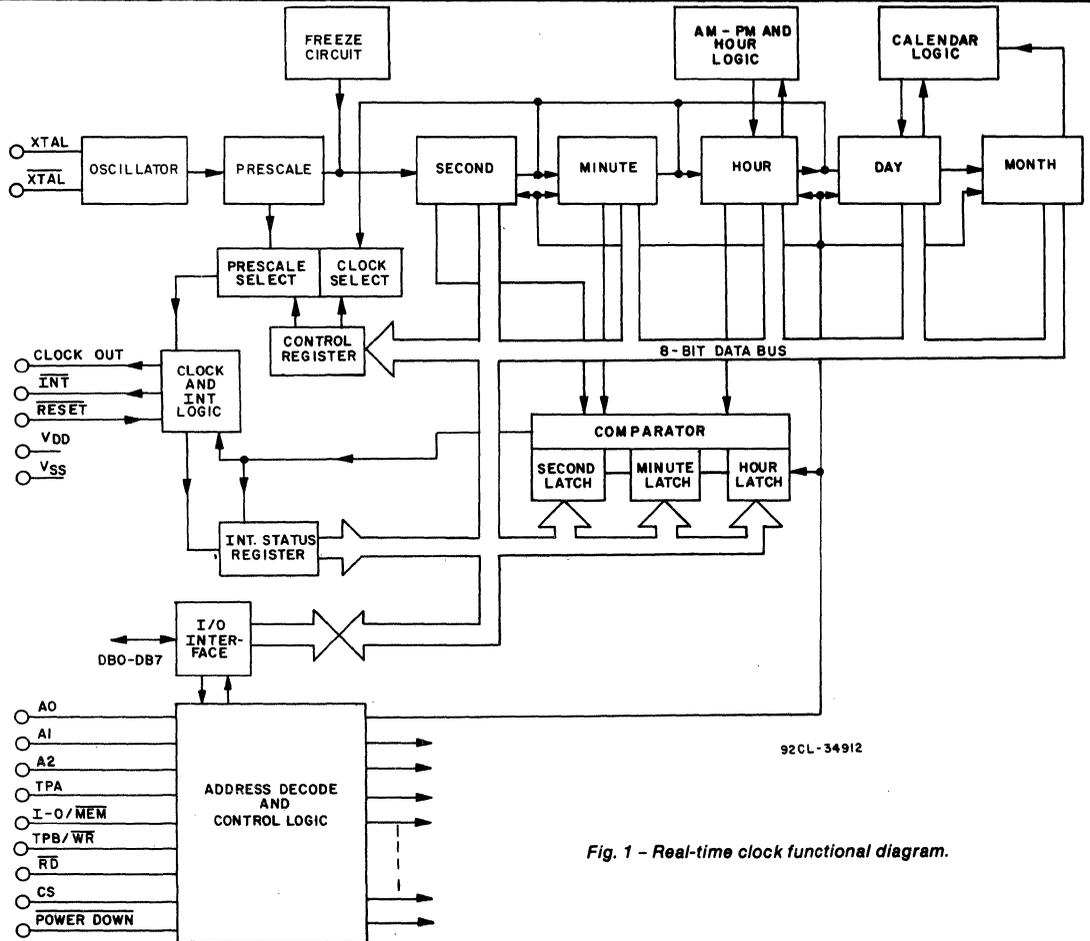


Fig. 1 - Real-time clock functional diagram.

RCA CMOS LSI Products

CDP1879, CDP1879C

STATIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$ $V_{DD} \pm 5\%$, Except as noted

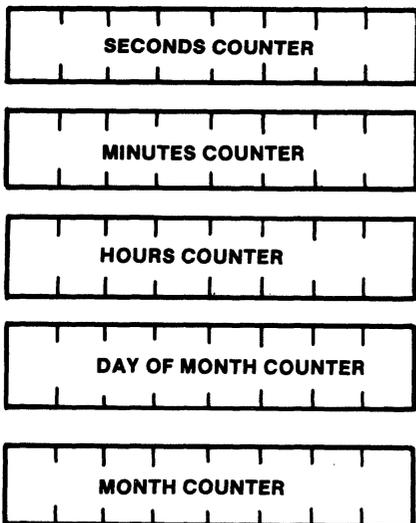
CHARACTERISTIC	CONDITIONS			LIMITS						UNITS		
	V_O (V)	V_{IN} (V)	V_{DD} (V)	CDP1879			CDP1879C					
				Min.	Typ.*	Max.	Min.	Typ.*	Max.			
Quiescent Device Current	I_{DD}	—	0, 5	5	—	0.01	50	—	0.02	200	μA	
		—	0, 10	10	—	1	200	—	—	—		
Output Low Drive (Sink) Current, Data Bus	I_{OL}	0.4	0, 5	5	1.6	3.2	—	1.6	3.2	—	mA	
		0.5	0, 10	10	2.6	5.2	—	—	—	—		
Output High Drive (Source) Current, Data Bus	I_{OH}	4.6	0, 5	5	-1.15	-2.3	—	-1.15	-2.3	—	mA	
		9.5	0, 10	10	-2.6	-5.2	—	—	—	—		
Output Low Drive (Sink) Current, Clock Out	I_{OL}	0.4	0, 5	5	600	—	—	600	—	—	μA	
		0.5	0, 10	10	1.2	—	—	—	—	—	mA	
Output High Drive (Source) Current, Clock Out	I_{OH}	4.6	0, 5	5	600	—	—	600	—	—	μA	
		9.5	0, 10	10	1.2	—	—	—	—	—	mA	
Output Low Drive (Sink) Current, XTAL Out	I_{OL}	0.4	0, 5	5	200	—	—	200	—	—	μA	
		0.5	0, 10	10	400	—	—	—	—	—		
Output High Drive (Source) Current, XTAL Out	I_{OH}	4.6	0, 5	5	200	—	—	200	—	—	μA	
		9.5	0, 10	10	400	—	—	—	—	—		
Output Voltage Low-Level	$V_{OL}\ddagger$	—	0, 5	5	—	0	0.1	—	0	0.1	V	
		—	0, 10	10	—	0	0.1	—	—	—		
Output Voltage High Level	$V_{OH}\ddagger$	—	0, 5	5	4.9	5	—	4.9	5	—	V	
		—	0, 10	10	9.9	10	—	—	—	—		
Input Low Voltage	V_{IL}	0.5, 4.5	—	5	—	—	1.5	—	—	1.5	V	
		0.5, 9.5	—	10	—	—	3	—	—	—		
Input High Voltage	V_{IH}	0.5, 4.5	—	5	3.5	—	—	3.5	—	—	V	
		0.5, 9.5	—	10	7	—	—	—	—	—		
Input Leakage Current	I_{IN}	Any	0, 5	5	—	—	± 1	—	—	± 1	μA	
		Input	0, 10	10	—	—	± 2	—	—	—		
3-State Output Leakage Current	I_{OUT}	0, 5	0, 5	5	—	—	± 1	—	—	± 1	μA	
		0, 10	0, 10	10	—	—	± 1	—	—	—		
Operating Current	I_{DD1}	External Clock	32 kHz	5	—	20	—	—	20	—	μA	
					2 MHz	—	750	—	—	750	—	—
					4 MHz	—	1.4	—	—	1.4	—	—
		32 kHz	10	—	40	—	—	—	—	—	μA	
				2 MHz	—	2	—	—	—	—	—	
				4 MHz	—	4.5	—	—	—	—	—	
XTAL Oscillator	32 kHz	0, 5	5	—	200	—	—	200	—	μA		
				2 MHz	—	550	—	—	550	—	—	
				4 MHz	—	900	—	—	900	—	—	
	32 kHz	0, 10	10	—	2.3	—	—	—	—	—		
				2 MHz	—	3	—	—	—	—	mA	
				4 MHz	—	3.8	—	—	—	—	—	
Input Capacitance	C_{IN}	—	—	—	—	5	7.5	—	5	7.5	pF	
Output Capacitance	C_{OUT}	—	—	—	—	10	15	—	10	15		

*Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .

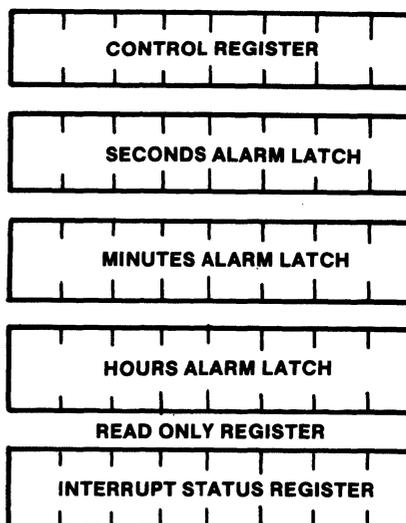
‡ $I_{OL} = I_{OH} = 1 \mu\text{A}$.

PROGRAMMING MODEL

WRITE AND READ REGISTERS



WRITE ONLY REGISTERS



READ ONLY REGISTER



REGISTER TRUTH TABLE

ADDRESS			ACTIVE SIGNAL		BIT 3 CONTROL REGISTER	REGISTER OPERATION
A2	A1	A0	TPB/ $\overline{\text{WR}}$	$\overline{\text{RD}}$		
0	1	0	X		0	Write Seconds Counter
0	1	0		X	0	Read Seconds Counter
0	1	1	X		0	Write Minutes Counter
0	1	1		X	0	Read Minutes Counter
1	0	0	X		0	Write Hours Counter
1	0	0		X	0	Read Hours Counter
1	0	1	X		0	Write Date Counter
1	0	1		X	0	Read Date Counter
1	1	0	X		0	Write Month Counter
1	1	0		X	0	Read Month Counter
0	1	0	X		1	Write Seconds Alarm Latch
0	1	1	X		1	Write Minutes Alarm Latch
1	0	0	X		1	Write Hours Alarm Latch
1	1	1	X			Write Control Register
1	1	1		X		Read Int. Status Register

GENERAL OPERATION

The real-time clock contains seconds, minutes, and hours, date and month counters that hold time of day/calendar information (See Fig. 2). The frequency of an intrinsic oscillator is divided down to supply a once-a-second signal to the counter series string. The counters are separately addressable and can be written to or read from.

The real-time clock contains seconds, minutes and hour write only alarm latches that store the alarm time (See Fig. 3). When the value of the alarm latches and counters are equal, the interrupt output is activated. The interrupt output can also be activated by a clock output transition. The clock output is derived from the prescaler and counters and can be one of 15 square-wave signals. The value in the read only interrupt status register identifies the interrupt source.

Operational control of the real time clock is determined by the byte in a write only control register. The 8 bit value in this register determines the correct divisor for the prescaler, a data direction and alarm enable bit, clock output select, and start/stop control (See Fig. 4).

Data transfer and addressing are accomplished in two modes of operation, memory mapping and I/O mapping using the CDP1800-series microprocessors. The mode is selected by the level on an input pin (I-O/MEM). Memory mapping implies use of the address lines as chip selects and address inputs using linear selection or partial or full decoding methods. I/O mapping with the CDP1800-series microprocessors involves use of the N line outputs in conjunction with input and output instructions to transfer data to and from memory.

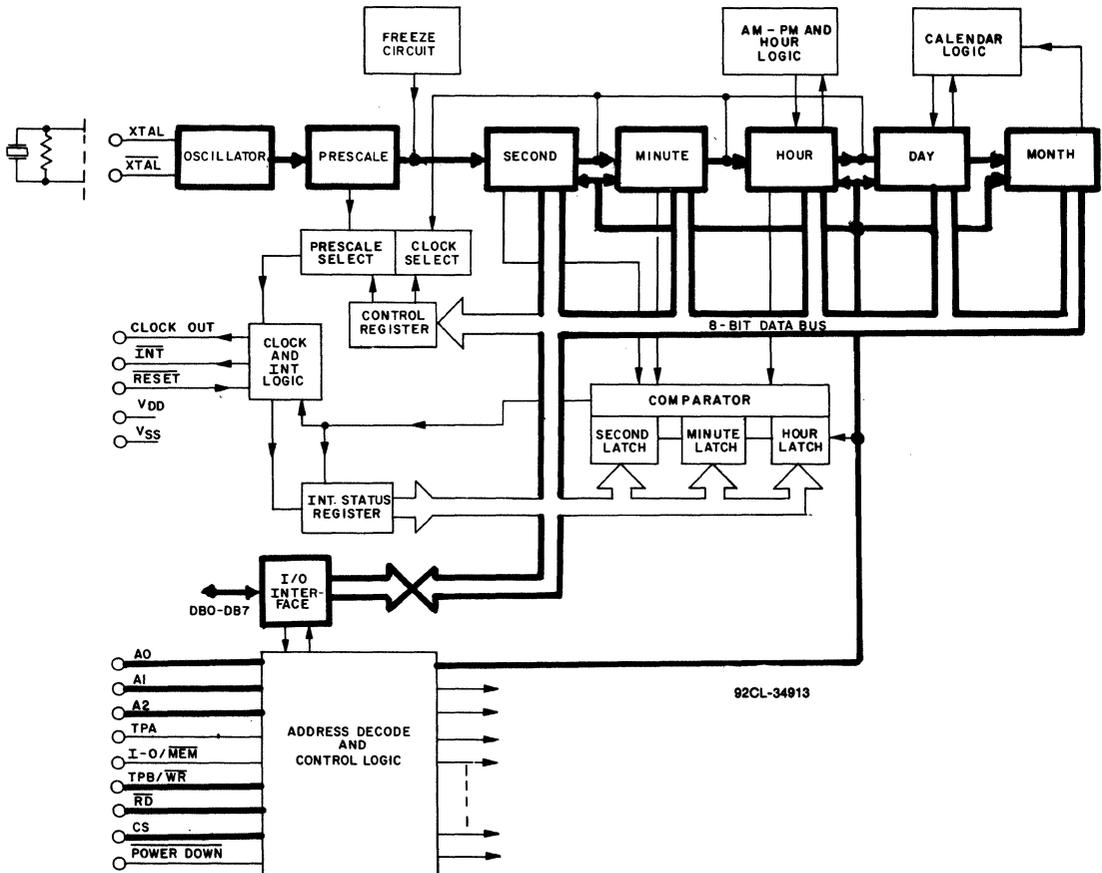


Fig. 2 - Functional diagram - time counters highlighted.

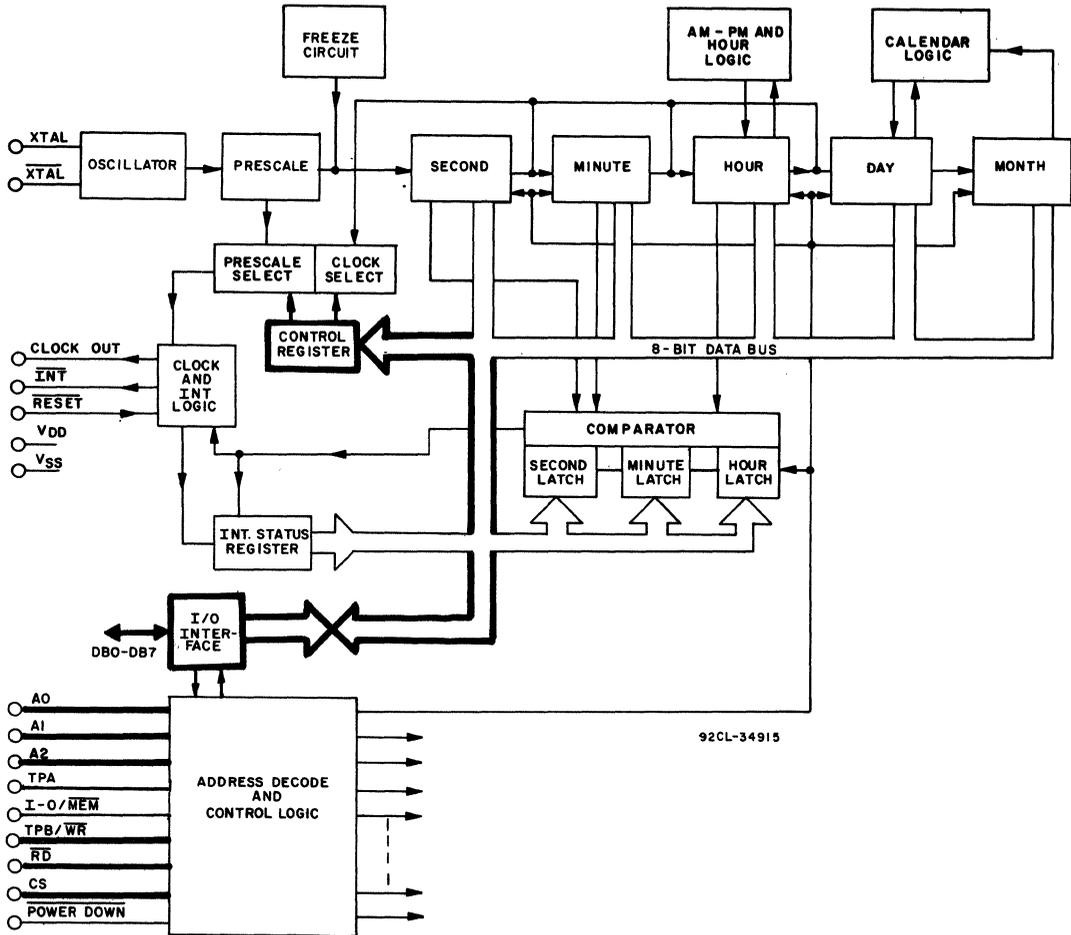


Fig. 4 - Functional diagram - control register highlighted.

COUNTERS (See Fig. 2) (Cont'd)

counters are addressed separately and BCD data is transferred to and from the via the data bus. The most significant bit of the hours counter (Bit 7) is user programmed to indicate AM or PM and will be inverted every 12th hour. (0 = AM, 1 = PM). Bit 6 of the hours counter is user programmed to enable the hours counter for 12 or 24 hour operation. (0 = 24, 1 = 12). If 24-hour operation is selected, the AM-PM bit is "don't care", but still toggles every 12th hour. Writing to the seconds counter resets the last 7 stages of the prescaler, allowing time accuracy to approximately 1/100 of a second.

The most significant bit of the month counter is a Leap Year bit. If it is set to "1", the counter will count to February 29, then roll to March 1. If set to "0" it will go to March 1st after February 28th.

ALARM AND INTERRUPT STATUS REGISTER (See Fig. 3)

The alarm circuit consists of 1) seconds, minutes and hour alarm latches that hold the alarm time, 2) the outputs of the seconds, minutes and hour counters, and 3) a comparator

that drives an interrupt output. The comparator senses the counter and alarm latch values and activates the interrupt output (active low) when they are equal.

The write only alarm latches have the same addresses as their comparable counters. Bit 3 in the control register determines data direction to the latches or counters and alarm enabling. For example, during a write cycle, if bit 3 in the control register is a "1", addressing the seconds counter or alarm latch will load the seconds alarm latch from the data bus and will enable the alarm function. Conversely, if bit 3 in the control register is a "0", addressing the seconds counter or alarm latch during a write cycle will place the value on the data bus into the seconds counter and will disable the alarm function. The interrupt output can be activated by the alarm circuit or the clock output. When an interrupt occurs, the upper two bits of the interrupt status register identify the interrupt source. The interrupt status register has the same address as the control register. Addressing the interrupt status register with the RD line active will place these register bits on the data bus. Bits 0-5 are held low. A "1" in bit 6 represents a clock output transition as the interrupt source. A "1" in bit 7 will identify the alarm circuit as the interrupt source.

ALARM AND INTERRUPT STATUS REGISTER (See Fig. 3) (Cont'd)

Activating the reset pin (active low) resets the hour latch to "30" which prevents a match between alarm and time registers during an initialization procedure. Activating the reset pin or writing to the control register resets the interrupt output(high) and clears the interrupt status register.

CLOCK OUTPUT (See Fig. 3)

One of 15 counter and prescaler overflows can be selected as a 50% duty cycle output signal that is available at the "clock out" pin. The frequency is selected by the upper nibble in the control register. For example, selecting a one-second clock output will result in a repetitive signal that will be high for 500 ms and low for the same period. The high-to-low transition of the output signal will set the clock bit in the status register and activate the interrupt output. The level of the "clock out" signal is derived from the value in the counter. Example: if hours clock is selected and the minutes counter holds 4 minutes, the clock out will be low for 26 minutes and high for 30 minutes. Thereafter, the clock out will toggle at a 50% duty cycle rate.

CONTROL REGISTER (See Table 1 and Fig. 4)

BIT								BIT			
7	6	5	4	3	2	1	0	7	6	5	4

CONTROL REGISTER BYTE

The 8-bit value in the control register determines the following:

- Bit 0 and 1 — Frequency Select** — Since there are one of 4 possible crystals the oscillator in the real time clock can operate with, these bit levels determine the prescaler divisor so that an accurate one second pulse is supplied to the counter series string.

BIT 1	BIT 0	FREQUENCY
0	0	32,768 Hz
0	1	1.048576 MHz
1	0	2.097152 MHz
1	1	4.194304 MHz

- Bit 2 — Start-Stop Control** — Counter enabling is controlled by the value at this location. A "1" will allow the counters to function and a "0" in this location will disable the counters.
- Bit 3 — Counter/Latch Control** — The level at this location controls two functions. It is required since the counters and alarm latches have the same addresses.
 - A "0" in bit 3 will direct subsequent data to or from the counter selected and the alarm function will be disabled.
 - A "1" in bit 3 will direct subsequent data to or from the alarm latch and will enable the alarm.
- Bits 4 to 7 — Clock Select** — These bits select one of 15 square wave signals that will be present at the "clock-out" pin. If bits 4 to 7 are zero's, the clock output pin will be high. If a clock is selected, the first high to low clock out transition will activate the interrupt pin (active low) and place a "1" in bit 6 of the status register. Writing to the control register or activating the reset pin will set the interrupt pin high and reset the interrupt status register.

Normal operation requires the control register to be written to and loaded first with a control word. However, subsequent writing to a counter if a "clock out" is selected may cause an interrupt out signal. Therefore, "clock-out" should be deselected by writing zero's into bits 4 through 7 if the interrupt is used. When the counters are loaded, the control register is again written to with the value in the upper nibble selecting the "clock out" signal.

READ AND WRITE SIGNALS

When the I-O/MEM pin is low, the real time clock is enabled for memory mapped operation. Data on the bus is placed in, or read from a counter, alarm latch or register by 1) placing the CS pin high 2) selective addressing 3) placing the TPB/W \overline{R} pin low during a write cycle with the RD pin high or 4) setting the RD pin low during a read cycle with the TPB/W \overline{R} pin high.

The I/O mapping mode used with the CDP1800 Series microprocessor is selected by setting the I-O/MEM pin high. The TPB/W \overline{R} pin on the real time clock is connected to the TPB output pin of the microprocessor. Data on the bus is written to or read from the counters, latches and registers by 1) placing the CS pin high 2) selective addressing utilizing the microprocessor N lines and I/O instructions 3) placing the TPB/W \overline{R} pin high with the RD pin low during an output or write operation (data is latched on TPB's trailing edge) 4) setting the RD line high during an input or read operation. Data is placed on the bus by the real time clock between the trailing edges of TPA and TPB.

FREEZE CIRCUIT

Since writing to or reading from the counters or alarm latches is performed asynchronously, the once-a-second signal from the prescaler may pulse the counter series string during these operations. This can result in erroneous data. To avoid this occurring, a transparent "freeze" circuit is incorporated into the real time clock. This circuit is designed to trap and hold the one second input clock transition if it occurs during access times. When the operations are completed, it is inserted into the counter series string. To utilize the "freeze" circuit, address "1" (A0 = 1, A1 = 0, A2 = 0) is selected first while performing a write operation. Read or write accesses may now be performed with assurance the data is stable. All operations must be concluded within 250 ms of the address "1" access. If memory mapping any dummy write operation after selecting address "1" will set the "freeze" circuit. If using the I/O mode, a 61 output instruction will perform the same function. There is no time restriction on subsequent accesses as long as the read or write operations are preceded by selecting address "1".

POWER DOWN

Power down operation is initiated with a low signal on the "POWER DOWN" input pin. Any inputs on the address or data bus are ignored. The clock output pin is set low. The interrupt output is tri-stated. If enabled previously, the alarm circuitry is active and will set the interrupt output pin low when alarm time occurs. The interrupt output will also go low if a clock was selected and an internal high-to-low transition occurs during power down. The clock output pin will remain low. If power down is initiated in the middle of a read or write sequence, it will not become activated until the read or write operation is completed.

APPLICATIONS (Cont'd)

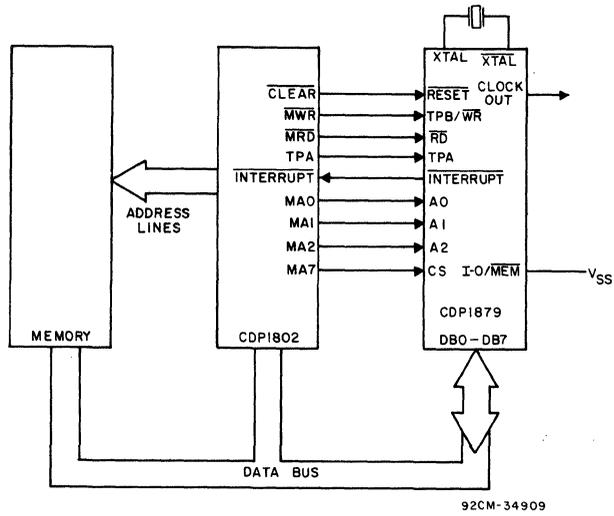


Fig. 6 - Typical CDP1802 memory-mapped system.

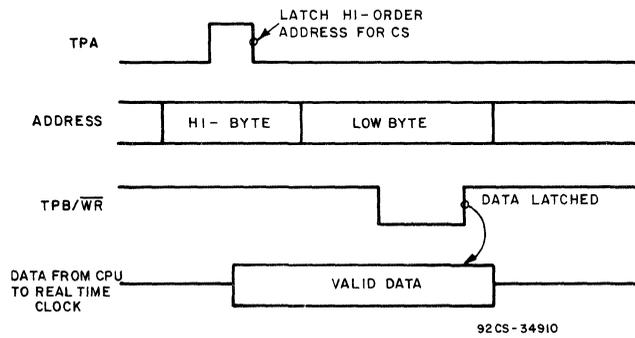


Fig. 7 - CDP1800-series memory-mapped write cycle timing waveforms.

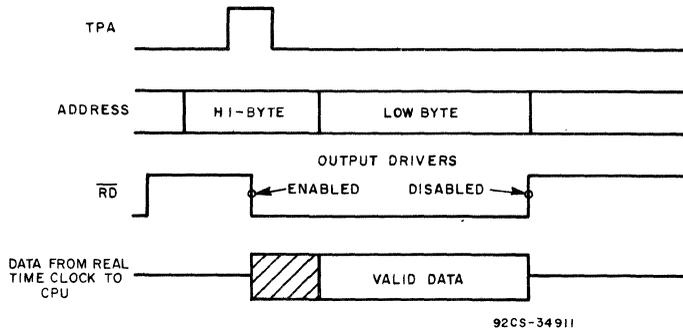


Fig. 8 - CDP1800-series memory-mapped read cycle timing waveforms.

APPLICATIONS (Cont'd)

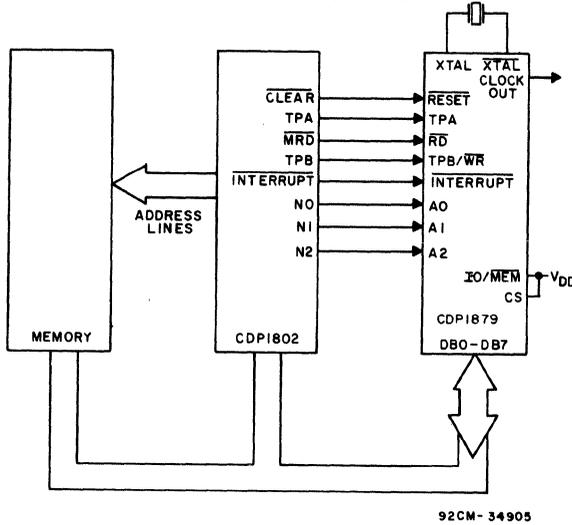


Fig. 9 - Typical CDP1802 input/output-mapped system.

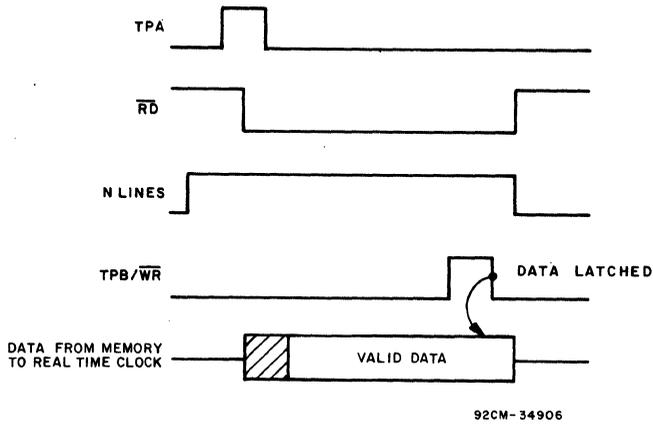


Fig. 10 - CDP1800-series input/output-mapping timing waveforms with output instruction.

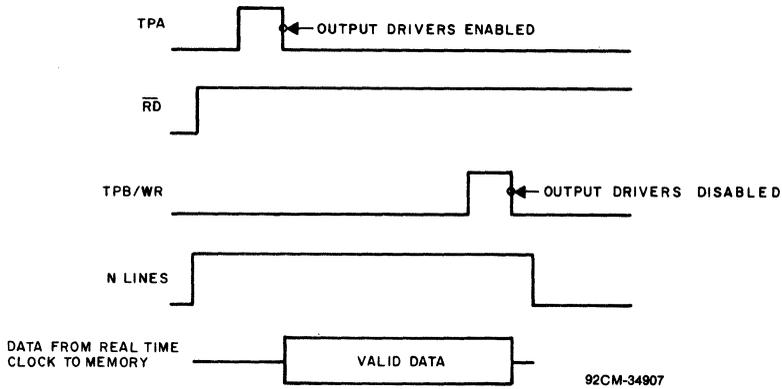


Fig. 11 - CDP1800-series input/output-mapping timing waveforms with input instruction.

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = 5\text{V} \pm 5\%$,
 Input $t_r, t_f = 10\text{ ns}$; $C_L = 50\text{ pF}$ and 1 TTL Load

CHARACTERISTIC	LIMITS			UNITS
	Min.†	Typ.*	Max.	

Read Cycle Times (see Fig. 12)

Data Access from Address	t_{DA}	—	350	—	ns
Read Pulse Width	t_{RD}	350	—	—	
Data Access from $\overline{\text{Read}}$	t_{DR}	—	250	—	
Address Hold after $\overline{\text{Read}}$	t_{RH}	0	—	—	
Output Hold after $\overline{\text{Read}}$	t_{DH}	50	—	250	
Chip Select Setup to TPA	t_{CS}	50	—	—	

†Time required by a limit device to allow for the indicated function.

*Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .

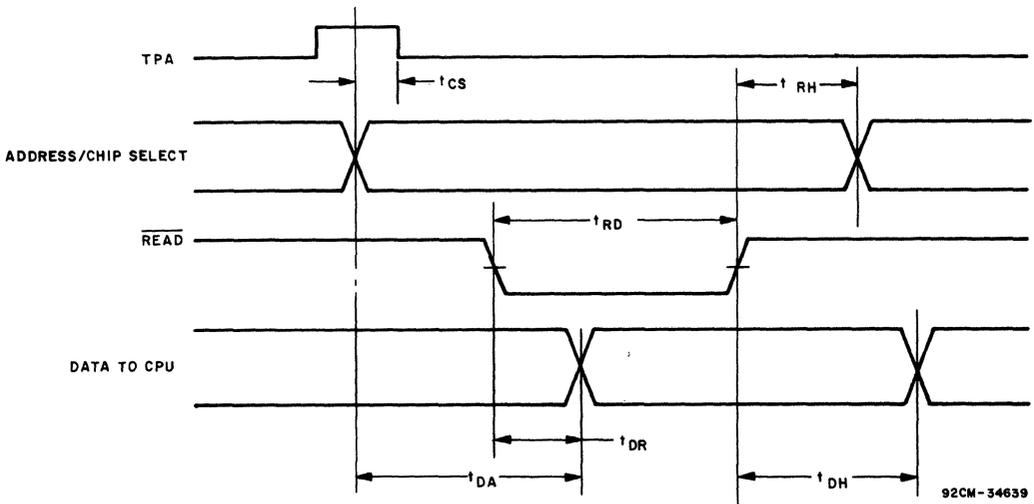


Fig. 12 - Read cycle timing waveforms.

CDP1879, CDP1879C

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = 5\text{V} \pm 5\%$,
 Input $t_r, t_f = 10\text{ ns}$; $C_L = 50\text{ pF}$ and 1 TTL Load

CHARACTERISTIC	LIMITS			UNITS
	Min.†	Typ.*	Max.	

Write Cycle Times (see Fig. 13)

Address Setup to Write	t_{AS}	450	—	—	ns
Write Pulse Width	t_{WR}	150	—	—	
Data Setup to Write	t_{DS}	200	—	—	
Address Hold after Write	t_{AH}	50	—	—	
Data Hold after Write	t_{WH}	100	—	—	
Chip Select Setup to TPA	t_{CS}	50	—	—	

†Time required by a limit device to allow for the indicated function.

*Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .

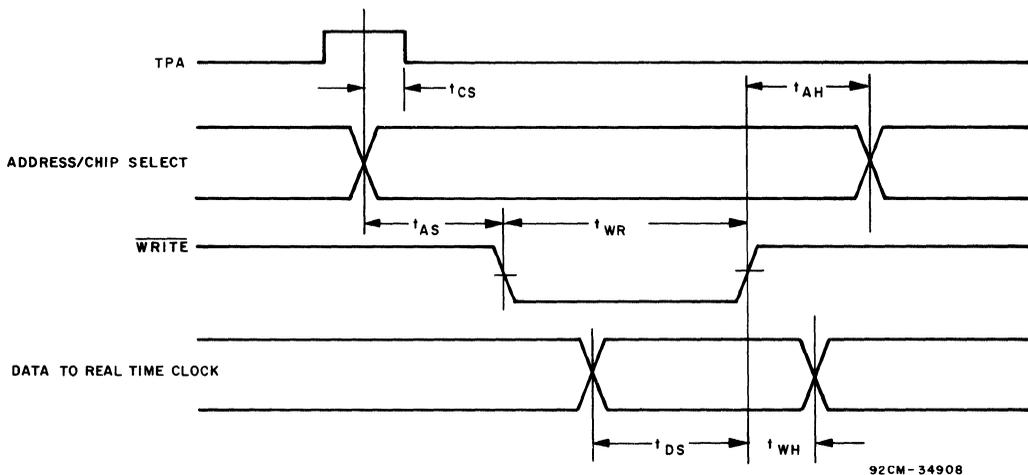


Fig. 13 - Write cycle timing waveforms.

OPERATING AND HANDLING CONSIDERATIONS

1. Handling

All inputs and outputs of RCA CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in ICAN-6525. "Guide to Better Handling and Operation of CMOS Integrated Circuits."

2. Operating

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause $V_{DD} - V_{SS}$ to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{CC} nor less than V_{SS} . Input currents must not exceed 10 mA even when the power supply is off.

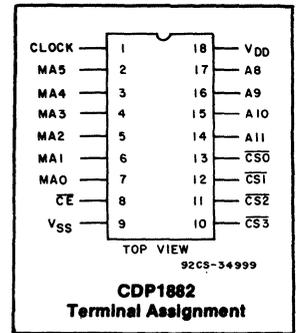
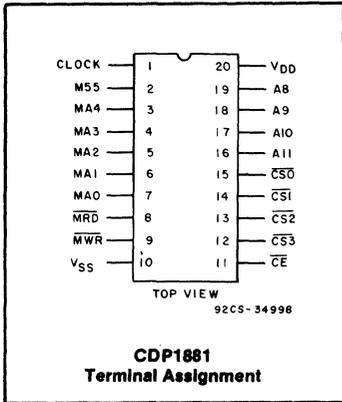
Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{CC} or V_{SS} , whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} , V_{CC} , or V_{SS} may damage CMOS devices by exceeding the maximum device dissipation.

CMOS 6-Bit Latch and Decoder Memory Interfaces



Features

- Performs memory address latch and decoder functions multiplexed or non-multiplexed
- Interfaces directly with the CDP1800-series microprocessors
- Can replace existing CDP1866 and CDP1867 (upward speed and function capability)
- Allows decoding for systems larger than 16K

The RCA-CDP1881 and CDP1882 are CMOS 6-bit memory latch and decoder circuits intended for use in CDP1800 series microprocessor systems. They can interface directly with the multiplexed address bus of this system at maximum clock frequency, and up to four 4K x 8-bit random-access memories to provide a 16K-byte RAM system. With four 2K x 8-bit RAMs, an 8K-byte RAM system can be decoded.

The devices are also compatible with non-multiplexed address bus microprocessors. By connecting the clock input to V_{DD}, the latches are in the data-following mode and the decoded outputs can be used in general-purpose memory-system applications.

The CDP1881 and CDP1882 are intended for use with 2K or 4K-byte RAMs and are identical except that in the CDP1882 MWR and MRD are excluded.

The CDP1881 and CDP1882 are functionally identical to the CDP1881C and the CDP1882C. They differ in that the CDP1881 and CDP1882 have a recommended operating voltage range of 4 to 10.5 volts and their C versions have a recommended operating voltage range of 4 to 6.5 volts.

The CDP1881 and CDP1882 are supplied in 20-lead and 18-lead packages, respectively. Both the CDP1881 and CDP1882 are available in hermetic, dual-in-line side-brazed ceramic (D suffix) and plastic (E suffix) packages.

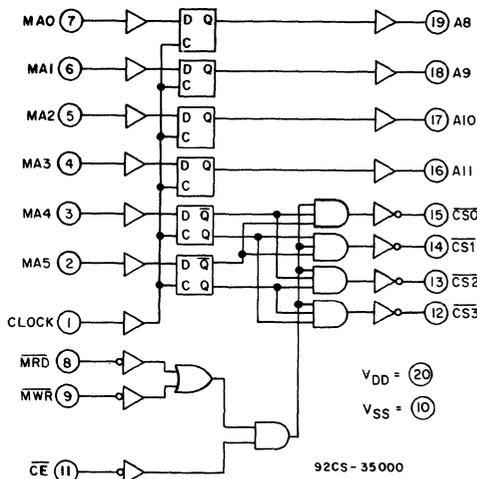


Fig. 1 - Functional diagram for the CDP1881.

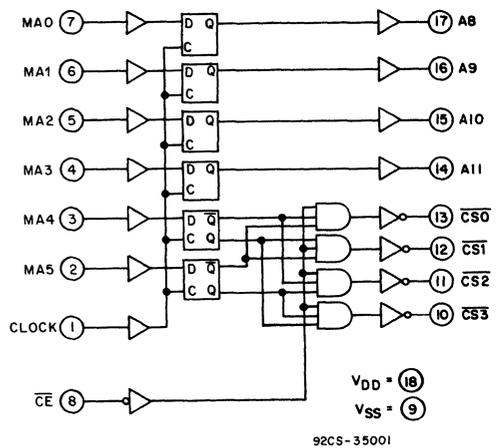


Fig. 2 - Functional diagram for the CDP1882.

RCA CMOS LSI Products

CDP1881, CDP1881C, CDP1882, CDP1882C

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltage referenced to V_{SS} terminal)

CDP1881 and CDP1882 -0.5 to +11 V

CDP1881C and CDP1882C -0.5 to +7 V

INPUT VOLTAGE RANGE, ALL INPUTS -0.5 to V_{DD} +0.5 V

DC INPUT CURRENT, ANY ONE INPUT ± 10 mA

POWER DISSIPATION PER PACKAGE (P_D):

For $T_A = -40$ to $+60^\circ\text{C}$ (PACKAGE TYPE E) 500 mW

For $T_A = +60$ to $+85^\circ\text{C}$ (PACKAGE TYPE E) Derate Linearly at 12 mW/ $^\circ\text{C}$ to 200 mW

For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE D) 500 mW

For $T_A = +100$ to 125°C (PACKAGE TYPE D) Derate Linearly at 12 mW/ $^\circ\text{C}$ to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

For $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE}$ (All Package Types) 100 mW

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPE D -55 to $+125^\circ\text{C}$

PACKAGE TYPE E -40 to $+85^\circ\text{C}$

STORAGE-TEMPERATURE RANGE (T_{stg}) -65 to $+150^\circ\text{C}$

LEAD TEMPERATURE (DURING SOLDERING):

At distance $1/16 \pm 1/32$ in. (1.59 ± 0.79 mm) from case for 10 s max. $+265^\circ\text{C}$

OPERATING CONDITIONS at $T_A = \text{Full Package-Temperature Range}$. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1881, CDP1882		CDP1881C, CDP1882C		
	Min.	Max.	Min.	Max.	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	

OPERATING AND HANDLING CONSIDERATIONS

1. Handling

All inputs and outputs of RCA CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in ICAN-6525, "Guide to Better Handling and Operation of CMOS Integrated Circuits."

2. Operating

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must

not cause $V_{DD} - V_{SS}$ to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{CC} nor less than V_{SS} . Input currents must not exceed 10 mA even when the power supply is off.

Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{CC} or V_{SS} , whichever is appropriate.

Output Short Circuits

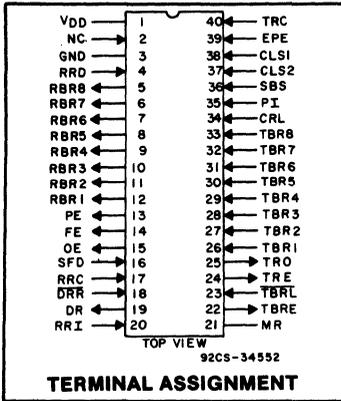
Shorting of outputs to V_{DD} , V_{CC} , or V_{SS} may damage CMOS devices by exceeding the maximum device dissipation.

Preliminary Data

CMOS Universal Asynchronous Receiver/Transmitter (UART)

Features:

- Low-power CMOS circuitry — 7.5 mW typ. at 3.2 MHz (max. freq.) at $V_{DD} = 5 V$
- Baud rate — DC to 200K bits/sec (max.) at $V_{DD} = 5 V$
 DC to 400K bits/sec (max.) at $V_{DD} = 10 V$
- 4 V to 10.5 operation
- Automatic data formatting and status generation
- Fully programmable with externally selectable word length (5-8 bits), parity inhibit, even/odd parity, and 1, 1.5, or 2 stop bits
- Operating-temperature range: (CDP6402D, CD) -55 to +125° (CDP6402E, CE) -40 to +85° C
- Replaces industry types IM6402 and HD6402



The RCA CDP6402 and CDP6402C are silicon-gate CMOS Universal Asynchronous Receiver/Transmitter (UART) circuits for interfacing computers or microprocessors to asynchronous serial data channels. They are designed to provide the necessary formatting and control for interfacing between serial and parallel data channels. The receiver

converts serial start, data, parity, and stop bits to parallel data verifying proper code transmission, parity and stop bits. The transmitter converts parallel data into serial form and automatically adds start parity and stop bits.

The data word can be 5, 6, 7 or 8 bits in length. Parity may be odd, even or inhibited. Stop bits can be 1, 1.5, or 2 (when transmitting 5-bit code).

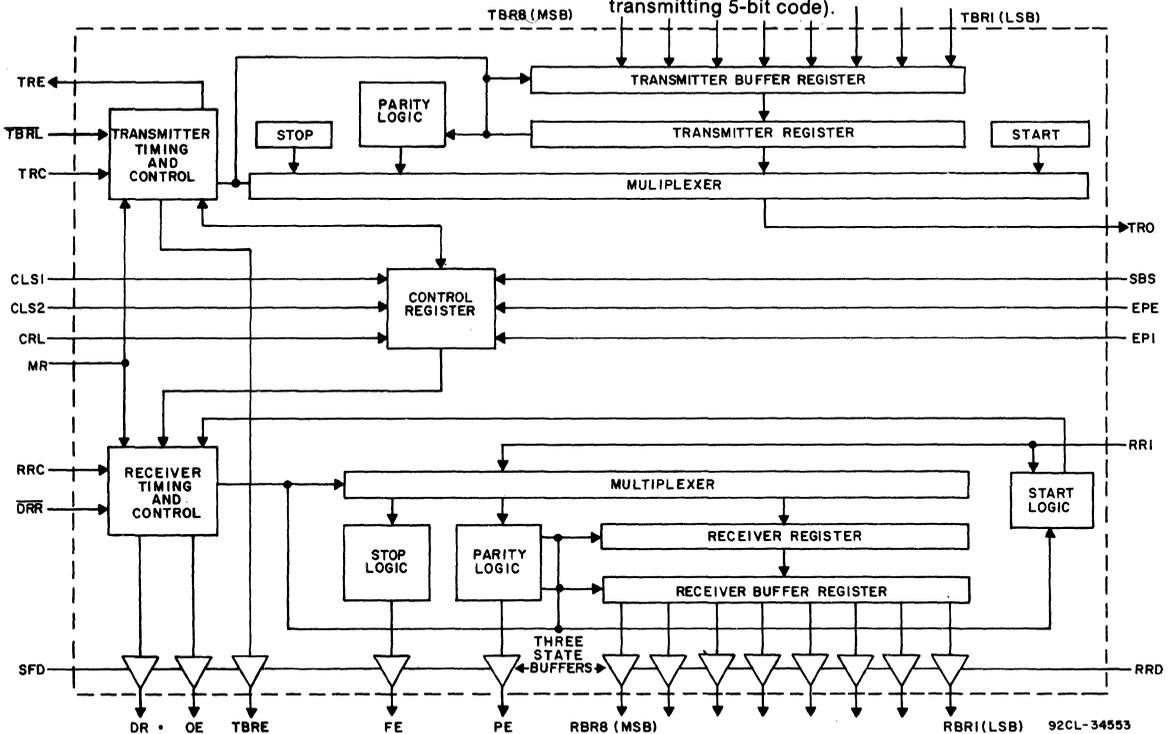


Fig. 1 - Functional block diagram.

RCA CMOS LSI Products

CDP6402, CDP6402C

The CDP6402 and CDP6402C can be used in a wide range of applications including modems, printers, peripherals, video terminals, remote data acquisition systems, and serial data links for distributed processing systems.

The CDP6402 and CDP6402C are functionally identical. They differ in that the CDP6402 has a recommended

operating voltage range of 4 to 10.5 volts, and the CDP6402C has a recommended operating voltage range of 4 to 6.5 volts. Both types are supplied in 40-lead dual-in-line ceramic packages (D suffix), and 40-lead dual-in-line plastic packages (E suffix).

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltage referenced to V_{SS} Terminal)

CDP6402 -0.5 to +11 V

CDP6402C -0.5 to +7 V

INPUT VOLTAGE RANGE, ALL INPUTS -0.5 to V_{DD} +0.5 V

DC INPUT CURRENT, ANY ONE INPUT ± 100 μA

POWER DISSIPATION PER PACKAGE (P_D):

For T_A = -40 to +60°C (PACKAGE TYPE E) 500 mW

For T_A = +60 to +85°C (PACKAGE TYPE E) Derate Linearly at 12 mW/°C to 200 mW

For T_A = -55 to 100°C (PACKAGE TYPE D) 500 mW

For T_A = +100 to +125°C (PACKAGE TYPE D) Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100 mW

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPE D -55 to +125°C

PACKAGE TYPE E -40 to +85°C

STORAGE TEMPERATURE RANGE (T_{stg}) -85 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. +265°C

OPERATING CONDITIONS at T_A = Full Package-Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP6402		CDP6402C		
	Min.	Max.	Min.	Max.	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V _{SS}	V _{DD}	V _{SS}	V _{DD}	

STATIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85°C, V_{DD} ± 10%, Except as noted

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)	CDP6402			CDP6402C			
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device Current	I _{DD}	0, 5 0, 10	5 10	— —	0.01 1	50 200	— —	0.02 —	200 —	μA
Output Low Drive (Sink) Current	I _{OL}	0.4, 0.5 0.5, 0, 10	5 10	1.2, 2.5 2.5, 5	2.4 5	— —	1.2 —	2.4 —	— —	mA
Output High Drive (Source) Current	I _{OH}	4.6, 0.5 9.5, 0, 10	5 10	-0.55, -1.3 -1.1, -2.6	-1.1 -2.6	— —	-0.55 —	-1.1 —	— —	mA
Output Voltage Low-Level	V _{OL} ‡	—, 0.5 —, 0, 10	5 10	—, 0 —, 0	0 0	0.1 0.1	— —	0 —	0.1 —	V
Output Voltage High Level	V _{OH} ‡	—, 0.5 —, 0, 10	5 10	4.9, 9.9 9.9, 10	5 10	— —	4.9 —	5 —	— —	V
Input Low Voltage	V _{IL}	0.5, 4.5 0.5, 9.5	— 10	5 10	— —	0.8 0.2V _{DD}	— —	— —	0.8 —	V
Input High Voltage	V _{IH}	0.5, 4.5 0.5, 9.5	— 10	5 10	V _{DD} -2.0 7	— —	V _{DD} -2.0 —	— —	— —	V
Input Leakage Current	I _{IN}	Any Input	0, 5 0, 10	5 10	— —	±10 ⁻⁴ ±10 ⁻⁴	±1 ±2	— —	±1 —	μA
3-State Output Leakage Current	I _{OUT}	0, 5 0, 10	0, 5 0, 10	5 10	— —	±10 ⁻⁴ ±10 ⁻⁴	±1 ±10	±10 ⁻⁴ —	±1 —	μA
Operating Current, I _{DD1} ‡	I _{DD1} ‡	—, 0.5 —, 0, 10	5 10	— —	1.5 10	— —	— —	1.5 —	— —	mA
Input Capacitance	C _{IN}	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance	C _{OUT}	—	—	—	10	15	—	10	15	pF

*Typical values are for T_A = 25°C and nominal V_{DD}. ‡I_{OL} = I_{OH} = 1 μA.

#Operating current is measured at 200 kHz or V_{DD} = 5 V and 400 kHz for V_{DD} = 10 V, with open outputs (worst-case frequencies for CDP1802A system operating at maximum speed of 3.2 MHz).

DESCRIPTION OF OPERATION

Initialization and Controls

A positive pulse on the MASTER RESET (MR) input resets the control, status, and receiver buffer registers, and sets the serial output (TRO) High. Timing is generated from the clock inputs RRC and TRC at a frequency equal to 16 times the serial data bit rate. The RRC and TRC inputs may be driven by a common clock, or may be driven independently by two different clocks. The CONTROL REGISTER LOAD (CRL) input is strobed to load control bits for PARITY INHIBIT (PI), EVEN PARITY ENABLE (EPE), STOP BIT SELECTS (SBS), and CHARACTER LENGTH SELECTS (CLS1 and CLS2). These inputs may be hand wired to V_{SS} or V_{DD} with CRL to V_{DD}. When the initialization is completed, the UART is ready for receiver and/or transmitter operations.

Transmitter Operation

The transmitter section accepts parallel data, formats it, and transmits it in serial form (Fig. 2) on the TRO terminal.

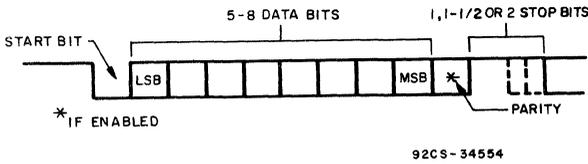


Fig. 2 - Serial data format.

Transmitter timing is shown in Fig. 3. (A) Data is loaded into the transmitter buffer register from the inputs TBR1 through TBR8 by a logic low on the TBRL input. Valid data must be present at least t_{DT} prior to, and t_{DD} following, the rising edge of TBRL. If words less than 8 bits are used, only the least significant bits are used. The character is right justified into the least significant bit, TBR1. (B) The rising edge of TBRL clears TBRE. Zero to 1 clock cycles later data is transferred to the transmitter register and TRE is cleared and transmission starts. TBREmpty is reset to a logic high. Output data is clocked by TRC. The clock rate is 16 times the data rate. (C) A second pulse on TBRL loads data into the transmitter buffer register. Data transfer to the transmitter register is delayed until transmission of the current character is complete. (D) Data is automatically transferred to the transmitter register and transmission of that character begins.

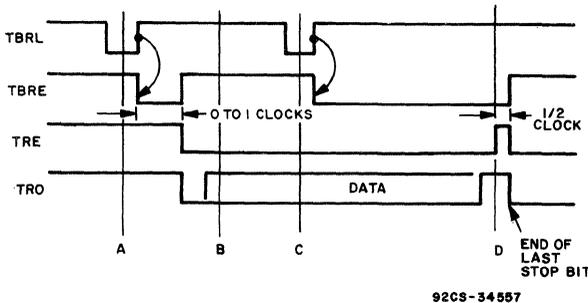


Fig. 3 - Transmitter timing waveforms.

Receiver Operation

Data is received in serial form at the RRI input. When no data is being received, RRI input must remain high. The data is clocked through the RRC. The clock rate is 16 times the data rate. Receiver timing is shown in Fig. 4.

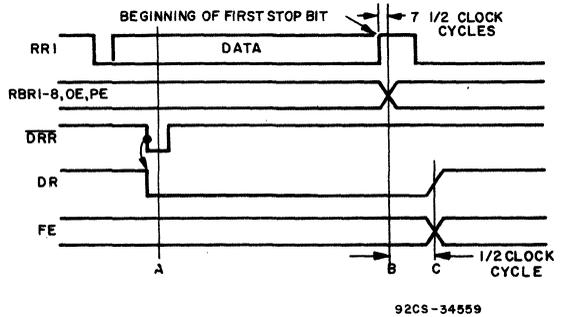


Fig. 4 - Receiver timing waveforms.

(A) A low level on \overline{DRR} clears the DR line. (B) During the first stop bit data is transferred from the receiver register to the RBR register. If the word is less than 8 bits, the unused most significant bits will be a logic low. The output character is right justified to the least significant bit RBR1. A logic high on OE indicates overruns. An overrun occurs when DR has not been cleared before the present character was transferred to the RBR. A logic high on PE indicates a parity error. (C) 1/2 clock cycle later DR is set to a logic high and FE is evaluated. A logic high on FE indicates an invalid stop bit was received.

Start Bit Detection

The receiver uses a 16X clock for timing (Fig. 5). The start bit could have occurred as much as one clock cycle before it was detected, as indicated by the shaded portion. The center of the start bit is defined as clock count 7 1/2. If the receiver clock is a symmetrical square wave, the center of the start bit will be located within $\pm 1/2$ clock cycle, $\pm 1/32$ bit or $\pm 3.125\%$. The receiver begins searching for the next start bit at 9 clocks into the first stop bit.

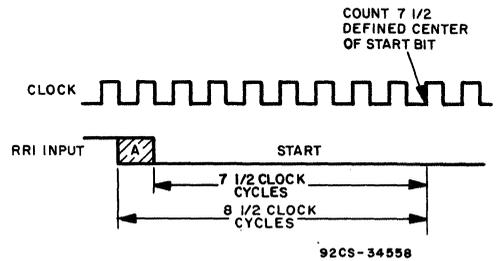


Fig. 5 - Start bit timing waveforms.

RCA CMOS LSI Products

CDP6402, CDP6402C

Table I - Control Word Function

CONTROL WORD					DATA BITS	PARITY BIT	STOP BIT(S)
CLS2	CLS1	PI	EPE	SBS			
L	L	L	L	L	5	ODD	1
L	L	L	L	H	5	ODD	1.5
L	L	L	H	L	5	EVEN	1
L	L	L	H	H	5	EVEN	1.5
L	L	H	X	L	5	DISABLED	1
L	L	H	X	H	5	DISABLED	1.5
L	H	L	L	L	6	ODD	1
L	H	L	L	H	6	ODD	2
L	H	L	L	L	6	EVEN	1
L	H	L	L	H	6	EVEN	2
L	H	H	X	L	6	DISABLED	1
L	H	H	X	H	6	DISABLED	2
L	L	L	L	L	7	ODD	1
L	L	L	L	H	7	ODD	2
L	L	L	H	L	7	EVEN	1
L	L	L	H	H	7	EVEN	2
L	L	H	X	L	7	DISABLED	1
L	L	H	X	H	7	DISABLED	2
L	H	L	L	L	8	ODD	1
L	H	L	L	H	8	ODD	2
L	H	L	L	L	8	EVEN	1
L	H	L	L	H	8	EVEN	2
L	H	H	X	L	8	DISABLED	1
L	H	H	X	H	8	DISABLED	2

X = Don't Care

Table II - Function Pin Definition

PIN	SYMBOL	DESCRIPTION	PIN	SYMBOL	DESCRIPTION
1	VDD	Positive Power Supply	15	OE	A high level on OVERRUN ERROR indicates the data received flag was not cleared before the last character was transferred to the receiver buffer register. The Error is reset at the next character's stop bit if DRR has been performed (i.e., DRR; active low).
2	N/C	No Connection	16	SFD	A high level on STATUS FLAGS DISABLE forces the outputs PE, FE, OE, DR, TBRE to a high impedance state.
3	GND	Ground (VSS)	17	RRC	The RECEIVER REGISTER CLOCK is 16X the receiver data rate.
4	RRD	A high level on RECEIVER REGISTER DISABLE forces the receiver holding register outputs RBR1-RBR8 to a high impedance state.	18	DDR	A low level on DATA RECEIVED RESET clears the data received output (DR), to a low level.
5	RBR8	The contents of the RECEIVER BUFFER REGISTER appear on these three-state outputs. Word formats less than 8 characters are right justified to RBR1.	19	DR	A high level on DATA RECEIVED indicates a character has been received and transferred to the receiver buffer register.
6	RBR7	See Pin 5 - RBR8	20	RRI	Serial data on RECEIVER REGISTER INPUT is clocked into the receiver register.
7	RBR6		21	MR	A high level on MASTER RESET (MR) clears PE, FE, OE, DR, TRE and sets TBRE, TRO high. Less than 18 clocks after MR goes low, TRE returns high. MR does not clear the receiver buffer register, and is required after power-up.
8	RBR5		22	TBRE	A high level on TRANSMITTER BUFFER REGISTER EMPTY indicates the transmitter buffer register has transferred its data to the transmitter register and is ready for new data.
9	RBR4				
10	RBR3				
11	RBR2				
12	RBR1				
13	PE	A high level on PARITY ERROR indicates that the received parity does not match parity programmed by control bits. The output is active until parity matches on a succeeding character. When parity is inhibited, this output is low.			
14	FE	A high level on FRAMING ERROR indicates the first stop bit was invalid. FE will stay active until the next valid character's stop bit is received.			

Table II - Function Pin Definition (Cont'd)

PIN	SYMBOL	DESCRIPTION
23	TBRL	A low level on TRANSMITTER BUFFER REGISTER LOAD transfers data from inputs TBR1-TBR8 into the transmitter buffer register. A low to high transition on TBRL requests data transfer to the transmitter register. If the transmitter register is busy, transfer is automatically delayed so that the two characters are transmitted end to end.
24	TRE	A high level on TRANSMITTER REGISTER EMPTY indicates completed transmission of a character including stop bits.
25	TRO	Character data, start data and stop bits appear serially at the TRANSMITTER REGISTER OUTPUT.
26	TBR1	Character data is loaded into the TRANSMITTER BUFFER REGISTER via inputs TBR1-TBR8. For character formats less than 8-bits, the TBR8, 7, and 6 inputs are ignored corresponding to the programmed word length.
27	TBR2	} See Pin 26 - TBR1
28	TBR3	
29	TBR4	
30	TBR5	
31	TBR6	
32	TBR7	
33	TBR8	

PIN	SYMBOL	DESCRIPTION
34	CRL	A high level on CONTROL REGISTER LOAD loads the control register.
35	PI*	A high level on PARITY INHIBIT inhibits parity generation, parity checking and forces PE output low.
36	SBS*	A high level on STOP BIT SELECT selects 1.5 stop bits for a 5 character format and 2 stop bits for other lengths.
37	CLS2*	These inputs program the CHARACTER LENGTH SELECTED. (CLS1 low CLS2 low 5-bits) (CLS1 high CLS2 low 6-bits) (CLS1 low CLS2 high 7-bits) (CLS1 high CLS2 high 8-bits).
38	CLS1*	See Pin 37 - CLS2
39	EPE*	When PI is low, a high level on EVEN PARITY ENABLE generates and checks even parity. A low level selects odd parity.
40	TRC	The TRANSMITTER REGISTER CLOCK is 16X the transmit data rate.

*See Table I (Control Word Function)

OPERATING AND HANDLING CONSIDERATIONS

1. Handling

All inputs and outputs of RCA CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in ICAN-6525, "Guide to Better Handling and Operation of CMOS Integrated Circuits."

2. Operating

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause $V_{DD} - V_{SS}$ to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{CC} nor less than V_{SS} . Input currents must not exceed $100\mu A$ even when the power supply is off.

Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{CC} or V_{SS} , whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} , V_{CC} or V_{SS} may damage CMOS devices by exceeding the maximum device dissipation.

RCA CMOS LSI Products

CDP6402, CDP6402C

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} \pm 5\%$, $t_r, t_f = 20$ ns,

$V_{IH} = 0.7 V_{DD}$, $V_{IL} = 0.3 V_{DD}$, $C_L = 100$ pF

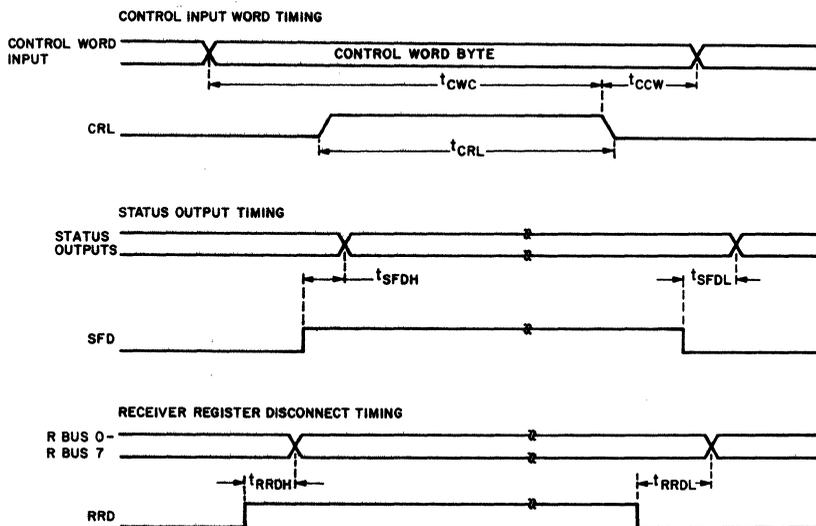
CHARACTERISTIC	VDD (V)	LIMITS				UNITS
		CDP6402		CDP6402C		
		Typ.*	Max.Δ	Typ.*	Max.Δ	

System Timing (See Fig. 6)

Minimum Pulse Width: CRL	t_{CRL}	5 10	50 40	150 100	50 —	150 —	ns
Minimum Setup Time Control Word to CRL	t_{CWC}	5 10	20 0	50 40	20 —	50 —	
Minimum Hold Time Control Word after CRL	t_{CCW}	5 10	40 20	60 30	40 —	60 —	
Propagation Delay Time SFD High to SOD	t_{SFDH}	5 10	200 100	300 150	200 —	300 —	
SFD Low to SOD	t_{SFDL}	5 10	75 40	120 60	75 —	120 —	
RRD High to Receiver Register High Impedance	t_{RRDH}	5 10	80 40	150 70	80 —	150 —	
RRD Low to Receiver Register Active	t_{RRDL}	5 10	80 40	150 70	80 —	150 —	

*Typical values for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .

ΔMaximum limits of minimum characteristics are the values above which all devices function.



92CM-31875R1

Fig. 6 - System timing waveforms.

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} \pm 5\%$, $t_r, t_f = 20\text{ ns}$,
 $V_{IH} = 0.7 V_{DD}$, $V_{IL} = 0.3 V_{DD}$, $C_L = 100\text{ pF}$

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		CDP6402		CDP6402C		
		Typ.*	Max.Δ	Typ.*	Max.Δ	
Transmitter Timing (See Fig. 7)						
Minimum Clock Period (TRC)	t_{CC} 5 10	250 125	310 155	250 —	310 —	ns
Minimum Pulse Width: Clock Low Level	t_{CL} 5 10	100 75	125 100	100 —	125 —	
Clock High Level	t_{CH} 5 10	100 75	125 100	100 —	125 —	
$\overline{\text{TBRL}}$	t_{THTH} 5 10	60 40	150 100	60 —	150 —	
Minimum Setup Time: $\overline{\text{TBRL}}$ to Clock	t_{THC} 5 10	175 90	275 150	175 —	275 —	
Data to $\overline{\text{TBRL}}$	t_{DT} 5 10	20 0	50 40	20 —	50 —	
Minimum Hold Time: Data after $\overline{\text{TBRL}}$	t_{TD} 5 10	40 20	60 30	40 —	60 —	
Propagation Delay Time: Clock to Data Start Bit	t_{CD} 5 10	300 150	450 225	300 —	450 —	
Clock to TBRE	t_{CT} 5 10	200 100	300 150	200 —	300 —	
$\overline{\text{TBRL}}$ to TBRE	t_{TTHR} 5 10	200 100	300 150	200 —	300 —	
Clock to TRE	t_{TTS} 5 10	200 100	300 150	200 —	300 —	

*Typical values for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .

ΔMaximum limits of minimum characteristics are the values above which all devices function.

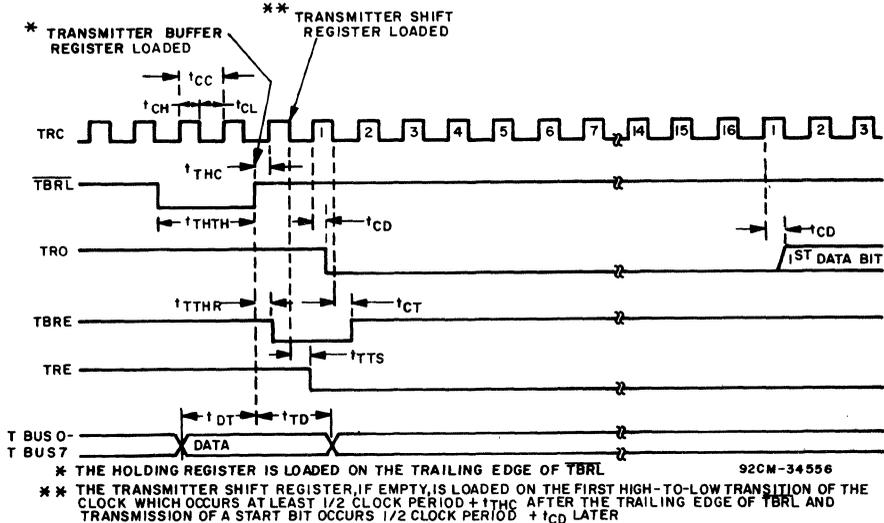


Fig. 7 - Transmitter timing waveforms.

CDP6402, CDP6402C

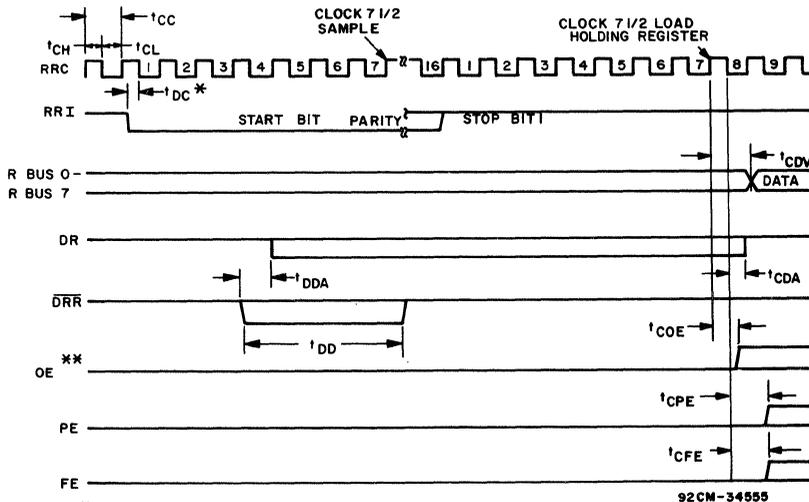
DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} \pm 5\%$, $t_r, t_f = 20$ ns,

$V_{IH} = 0.7 V_{DD}$, $V_{IL} = 0.3 V_{DD}$, $C_L = 100$ pF

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS	
		CDP6402		CDP6402C			
		Typ.*	Max.Δ	Typ.*	Max.Δ		
Receiver Timing (See Fig. 8)							
Minimum Clock Period (RRC)	t_{CC}	5	250	310	250	310	ns
Minimum Pulse Width:	t_{CL}	5	100	125	100	125	
		10	75	100	—	—	
Clock Low Level	t_{CH}	5	100	125	100	125	
		10	75	100	—	—	
DATA RECEIVED RESET	t_{DD}	5	50	75	50	75	
		10	25	40	—	—	
Minimum Setup Time:	t_{DC}	5	100	150	100	150	
		10	50	75	—	—	
Propagation Delay Time:	t_{DDA}	5	150	225	150	225	
		10	75	125	—	—	
Clock to Data Valid	t_{CDV}	5	225	325	225	325	
		10	110	175	—	—	
Clock to DR	t_{CDA}	5	225	325	225	325	
		10	110	175	—	—	
Clock to Overrun Error	t_{COE}	5	210	300	210	300	
		10	100	150	—	—	
Clock to Parity Error	t_{CPE}	5	240	375	240	375	
		10	120	175	—	—	
Clock to Framing Error	t_{CFE}	5	200	300	200	300	
		10	100	150	—	—	

*Typical values for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .

ΔMaximum limits of minimum characteristics are the values above which all devices function.



* IF A START BIT OCCURS AT A TIME LESS THAN t_{DC} BEFORE A HIGH-TO-LOW TRANSITION OF THE CLOCK, THE START BIT MAY NOT BE RECOGNIZED UNTIL THE NEXT HIGH-TO-LOW TRANSITION OF THE CLOCK. THE START BIT MAY BE COMPLETELY ASYNCHRONOUS WITH THE CLOCK.

** IF A PENDING DA HAS NOT BEEN CLEARED BY A READ OF THE RECEIVER HOLDING REGISTER BY THE TIME A NEW WORD IS LOADED INTO THE RECEIVER HOLDING REGISTER, THE OE SIGNAL WILL COME TRUE.

Fig. 8 - Receiver timing waveforms.

General-Purpose Memories Technical Data

COS/MOS 4-Word by 8-Bit Random-Access NDRO Memory

Binary Addressing CD4036AD, CD4036AK
Direct Word-Line Addressing CD4039AD, CD4039AK

Special Features:

- COS/MOS logic compatibility at all input and output terminals
- Memory bit expansion
- Memory word expansion via Wire-OR capability at the 8 INPUT-BIT and 8 OUTPUT-BIT lines

RCA type CD4036A is a single monolithic integrated circuit containing a 4-word x 8-bit Random Access NDRO Memory. Inputs include 8 INPUT-BIT lines, CHIP INHIBIT, WRITE, READ INHIBIT, MEMORY BYPASS, and 2 ADDRESS inputs. 8 OUTPUT-BIT lines are provided.

All input and output lines utilize standard COS/MOS inverter configurations and hence can be directly interfaced with COS/MOS logic devices.

CHIP INHIBIT allows memory word expansion by WIRE-ORing of multiple CD4036A packages at either the 8-bit input and/or output lines (see Fig. 19). With CHIP INHIBIT "high", both READ and WRITE operations are inhibited on the CD4036A. With CHIP INHIBIT "low", information can be written into and/or read continuously from one of the four words selected by the binary code on the two address lines. With CHIP INHIBIT "low", a "high" WRITE signal and a "low" READ INHIBIT signal activate WRITE and READ operations, respectively, at the addressed word location (see Fig. 4).

The MEMORY BYPASS signal, when "high", allows shunting of information from the 8 INPUT-BIT lines directly to the 8 OUTPUT-BIT lines without disturbing the state of the 4 words. During the bypass operation input information may also be written into a selected word location, provided the CHIP INHIBIT is "low" and the WRITE is "high". The READ operation is deactivated during the BYPASS operation because information is fed directly from the 8 INPUT-BIT lines to the 8 OUTPUT-BIT lines.

- Memory bypass capability for all bits
- Buffering on all outputs
- CD4036A—on-chip binary address decoding, separate READ INHIBIT and WRITE controls
- CD4039A—Direct word-line addressing
- Access Time—200 ns (typ.) at $V_{DD} = 10\text{ V}$

Applications:

Digital equipment where low power dissipation and/or high noise immunity are primary design requirements.

- Channel Preset Memory in digital frequency-synthesizer circuits
- General-purpose and scratchpad memory in COS/MOS and other low-power systems.

RCA type CD4039A is identical to the CD4036A with the exception that individual address-line inputs have been provided for each memory word in place of the binary ADDRESS, CHIP INHIBIT, and READ INHIBIT inputs. When Wire-ORing multiple CD4039A packages for memory word expansion, an individual CD4039A is selected by addressing one of its word locations. The READ operation is activated whenever a word location is addressed (via a "high" signal—see Fig. 5).

These devices will be supplied in two different 24-lead ceramic packages; the CD4036AK and CD4039AK in the flat-pack, and the CD4036AD and CD4039AD in the dual-in-line package.

MAXIMUM RATINGS,

Absolute-Maximum Values:

STORAGE-TEMPERATURE RANGE	-65 to +150 °C
OPERATING-TEMPERATURE RANGE	-55 to +125 °C
DC SUPPLY VOLTAGE RANGE (V _{DD} - V _{SS})	-0.5 to +15 V
DEVICE DISSIPATION (Per Package)	200 mW
ALL INPUTS	V _{SS} ≤ V _I ≤ V _{DD}
RECOMMENDED DC SUPPLY VOLTAGE (V _{DD} - V _{SS})	3 to 15 V
LEAD TEMPERATURE (During Soldering)	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	265 °C

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS		LIMITS						UNITS	
			CD4036AD, CD4036AK CD4039AD, CD4039AK							
			-55 °C		25 °C		125 °C			
V _O Volts	V _{DD} Volts	Min.	Max.	Min.	Max.	Min.	Max.			
Quiescent Device Current, I _L		5	—	5	—	5	—	300	μA	
		10	—	10	—	10	—	600		
Quiescent Device Dissipation/Pack- age, P _D		5	—	25	—	25	—	1500	μW	
		10	—	100	—	100	—	6000		
Output Voltage: Low-Level, V _{OL}		5	—	0.01	—	0.01	—	0.05	V	
		10	—	0.01	—	0.01	—	0.05		
High-Level, V _{OH}		5	4.99	—	4.99	—	4.95	—	V	
		10	9.99	—	9.99	—	9.95	—		
Threshold Voltage: N-Channel, V _{THN} P-Channel, V _{THP}	I _D = 20 μA		1.7 typ.		1.5 typ.		1.3 typ.		V	
	I _D = -20 μA		-1.7 typ.		-1.5 typ.		-1.3 typ.		V	
Noise Immunity, V _{NL} (All inputs except bit inputs when in memory by-pass mode.) V _{NH}		5	1.5	—	1.5	—	1.4	—	V	
		10	3	—	3	—	2.9	—		
		5	1.4	—	1.5	—	1.5	—		
		10	2.9	—	3	—	3	—		
Output Drive Current: N-Channel, I _{DN} P-Channel, I _{DP}	Normal Modes	0.5	5	0.12	—	0.10	—	0.07	—	mA
		0.5	10	0.30	—	0.25	—	0.17	—	
	Read Modes	4.5	5	-0.12	—	-0.10	—	-0.07	—	mA
		9.5	10	-0.30	—	-0.25	—	-0.17	—	
Output Drive Current: N-Channel, I _{DN} P-Channel, I _{DP}	Memory By-pass Mode +	0.5	5	0.04	—	0.03	—	0.02	—	mA
		0.5	10	0.09	—	0.075	—	0.05	—	
	Memory By-pass Mode +	4.5	5	-0.04	—	-0.03	—	-0.02	—	mA
		9.5	10	-0.09	—	-0.075	—	-0.05	—	
Input Current, I _I		—	—	—	—	10 typ.	—	—	pA	

+ Bit inputs driven from low-impedance driver.

RCA CMOS LSI Products
CD4036A, CD4039A

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$ and $C_L = 15\text{ pF}$
Typical Temperature Coefficient for all values of $V_{DD} = 0.3\%/^\circ\text{C}$

CHARACTERISTIC	TEST CONDITIONS	CD4036AD, CD4036AK CD4039AD, CD4039AK			UNITS	
		VDD Volts	Min.	Typ.		Max.
Read Delay Time, t_{rd} : (Access time) Read Inhibit (RI) Chip Inhibit (CI) Memory Bypass (MB) Address ¹ (ADD)	Output tied through 100 k Ω to V_{SS} for data output "high" and to V_{DD} for data output "low"	5	—	375	750	ns
		10	—	150	300	Note 4
		5	—	500	1000	ns
		10	—	200	400	Note 4
		5	—	375	750	ns
		10	—	150	300	ns
Write Set-up Time ² , t_{WS}		5	250	125	—	μs
		10	100	50	—	
Write Removal Time ³ , t_{WR}		5	0	0	—	ns
		10	0	0	—	
Write Pulse Duration, t_W		5	150	75	—	ns
		10	60	30	—	
Data Set-up Time ⁵ , t_{DS}		5	—	0	0*	ns
		10	—	0	0*	
Data Overlap Time ⁶ , t_{DO}		5	100*	50	—	ns
		10	40*	20	—	
Output Transition Time, t_{THL} t_{TLH}		5	—	200	400	ns
		10	—	100	200	
Input Capacitance, C_I	Any Input		—	5	—	pF

1. For CD4036A only, remove 100-k Ω test condition and write all 1's in word one, and all 0's in word two, or vice versa.
2. Delay from change of ADDRESS or CHIP-INHIBIT signals to application of WRITE pulse.
3. Delay from removal of WRITE pulse to change of ADDRESS or CHIP-INHIBIT signals.
4. Values for CD4036AD and CD4036AK only.
5. The time that DATA signal must be present before the WRITE pulse removal.
* Max. indicates satisfactory operation if t_{DS} equals or exceeds this value.
6. The time that DATA signal must remain present after the WRITE pulse removal.
* Min. indicates satisfactory operation if t_{DO} equals or exceeds this value.

HANDLING CONSIDERATIONS

Although protection against electrostatic effects is provided by built-in circuitry, the following handling precautions should be taken:

1. Soldering iron tips and test equipment should be grounded.
2. Devices should not be inserted in non-conductive containers such as conventional plastic snow or trays.

OPERATING CONSIDERATIONS

1. Low impedance pulse generators or power supplies connected to the inputs of these devices must be disconnected before the dc power supply is turned off.
2. All unused input leads should be connected to either V_{SS} or V_{DD} , whichever is appropriate for the logic circuit involved.

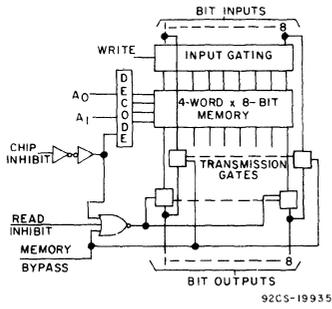


Fig. 1—CD4036A—logic block diagram.

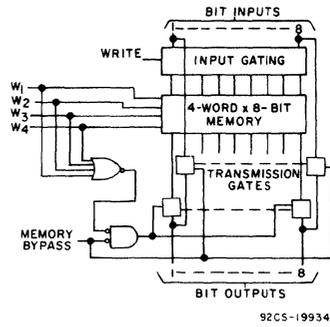


Fig. 2—CD4039A—logic block diagram.

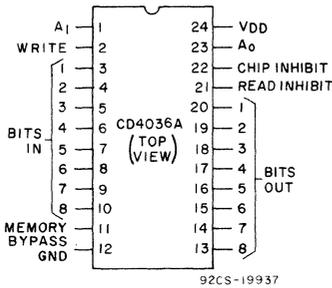
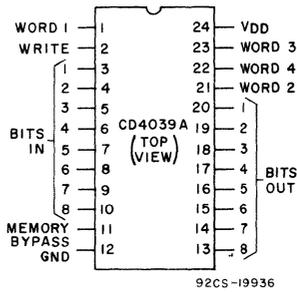


Fig. 3a)—CD4036AD and CD4036AK terminal assignments.



b)—CD4039AD and CD4039AK terminal assignments.

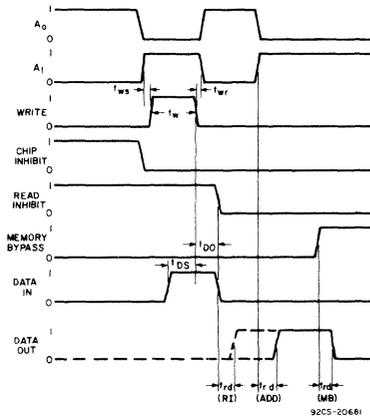


Fig. 4—CD4036A timing diagram.

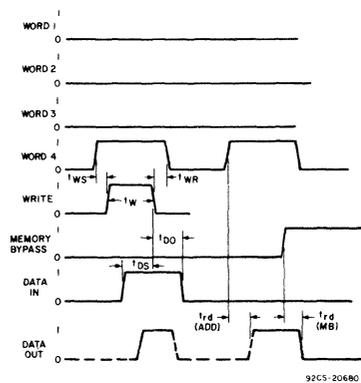


Fig. 5—CD4039A timing diagram.

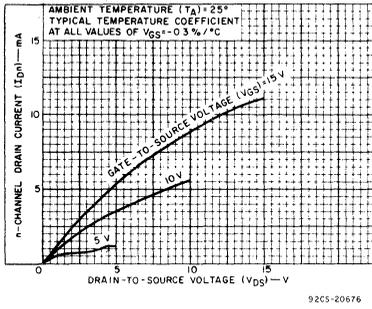


Fig. 6—Typical n-channel drain characteristics.

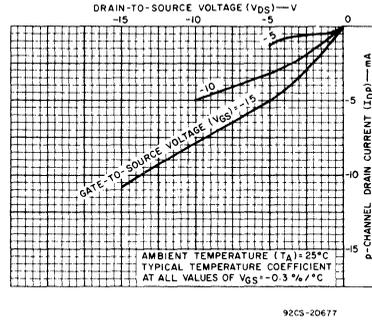


Fig. 7—Typical p-channel drain characteristics.

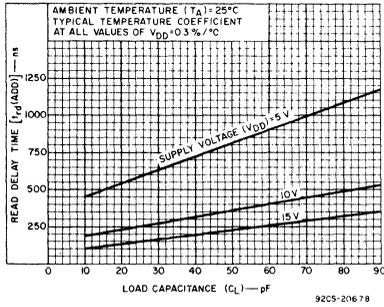


Fig. 8—Typical read delay time vs. C_L .

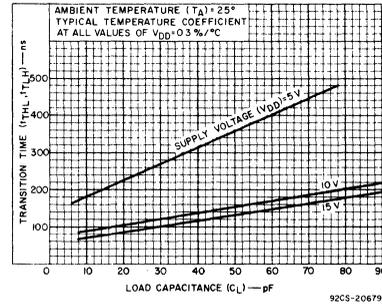


Fig. 9—Typical transition time vs. C_L .

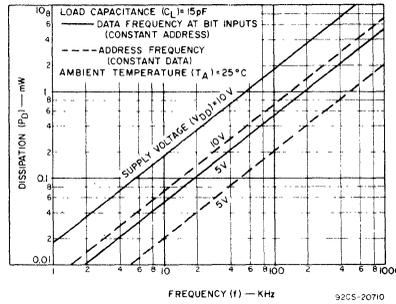
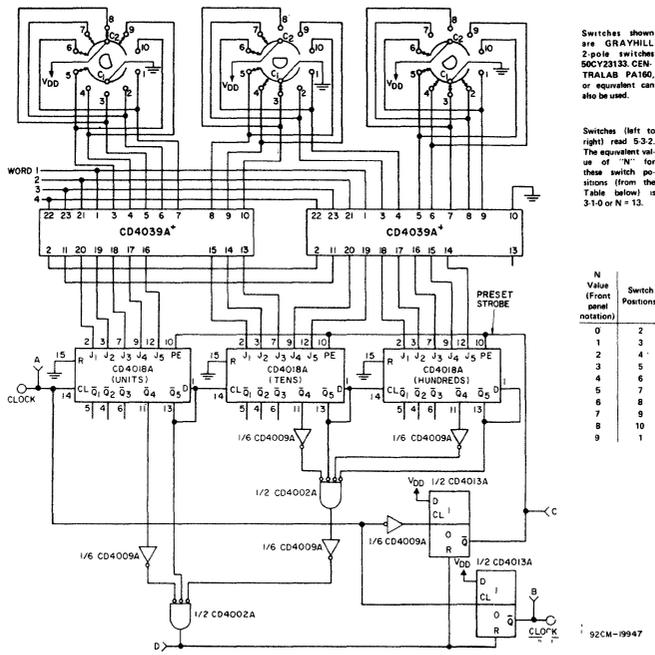


Fig. 10—Typical power dissipation vs. frequency.

RCA CMOS LSI Products
CD4036A, CD4039A



* The CD4036A CAN BE UTILIZED IN A SIMILAR FASHION. SEE APP. NOTE ICAN-6498 - "DESIGN OF FIXED AND PROGRAMMABLE COUNTERS USING THE RCA CD4018A COS/MOS PRESETTABLE DIVIDE-BY-'N' COUNTER" AND ICAN-6716, "LOW POWER DIGITAL FREQUENCY SYNTHESIZERS UTILIZING COS/MOS IC'S".

Fig. 18—Three-decade programmable ÷ N counter with 4-channel preset memory settings for frequency synthesizers.

The divide-by-N counter system shown in Fig. 18 is programmable from 2 to 999. Four counter-preset words, selected by means of the rotary switches, can be stored in the CD4039A devices and can be

read into each CD4018A by simply addressing the proper word. Note that the CD4029A (see Bulletin File No. 503) Presettable Up/Down Counter with BCD decade counting can also be used to perform the basic counting function.

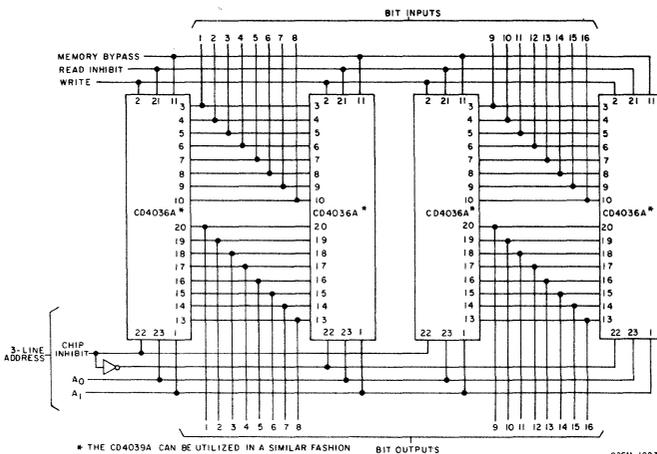
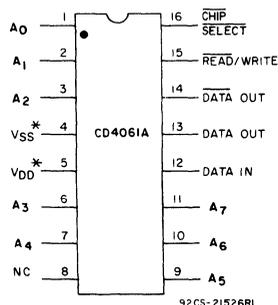


Fig. 19—General-purpose memory storage—8 words x 16 bits (RAM or ROM).

COS/MOS 256-Word by 1-Bit Static Random-Access Memory

Features:

- Low standby power: 10 nW/bit (typ.) @ $V_{DD} = 10\text{ V}$
- Access time: 380 ns (max.) @ $V_{DD} = 10\text{ V}$
- Single 3-to-15 V power supply
- COS/MOS input/output logic compatibility
- TTL output drive capability
- Three-state data outputs for bus-oriented systems
- 1101-type pin designations*
- Separate data output and data input lines
- Noise immunity: 45% of V_{DD} (typ.)
- Fully decoded addressing
- Single write/read control line



The RCA-CD4061A is a single monolithic integrated circuit containing a 256-word by 1-bit fully static, random-access, NDRO memory. The memory is fully decoded and requires 8 address input lines (A_0 - A_7) to select one of 256 storage locations. Additional connections are provided for a READ/WRITE command $\overline{\text{CHIP SELECT}}$ DATA IN, and DATA OUT and $\overline{\text{DATA OUT}}$ lines.

To perform READ and WRITE operations the $\overline{\text{CHIP-SELECT}}$ signal must be low. When the $\overline{\text{CHIP-SELECT}}$ signal is high, read and write operations are inhibited and the output is a high impedance. To change addresses, the $\overline{\text{CHIP-SELECT}}$ signal must be returned to a high level, regardless of the logic level of the $\overline{\text{READ/WRITE}}$ input. In a multiple package application, the $\overline{\text{CHIP-SELECT}}$

signal may be used to permit the selection of individual packages.

Output-voltage levels appear on the outputs only when the $\overline{\text{CHIP SELECT}}$ and $\overline{\text{READ/WRITE}}$ signals are both low. Separate data inputs and outputs are provided; they may be tied together, or, to eliminate interaction between READ and WRITE functions, may be used separately. The circuit arrangement permits the outputs from many arrays to be tied to a common bus.

All input and output lines are buffered. The CD4061A output buffers are capable of direct interfacing with TTL devices.

The CD4061A is available in a hermetically sealed 16-lead dual-in-line ceramic package (CD4061AD) or in chip form (CD4061AH).

MAXIMUM RATINGS,

Absolute-Maximum Values:

STORAGE-TEMPERATURE RANGE	-65 to +150°C
OPERATING-TEMPERATURE RANGE	-55 to +125°C
DC SUPPLY-VOLTAGE RANGE:	
V_{DD}^{Δ}	-0.5 to +15 V

DEVICE DISSIPATION (PER PACKAGE)

ALL INPUTS	$V_{SS} \leq V_i \leq V_{DD}$	200 mW
RECOMMENDED DC SUPPLY VOLTAGE	$(V_{DD} - V_{SS})$	3 to 15 V
LEAD TEMPERATURE (DURING SOLDERING):		
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm)		+265°C
from case for 10 s max.		

*The pin designations are compatible with other static 256-bit memories and are, therefore, not compatible with standard COS/MOS CD4000A-series devices; i.e., V_{DD} is pin 5 and V_{SS} is pin 4.

CD4061A

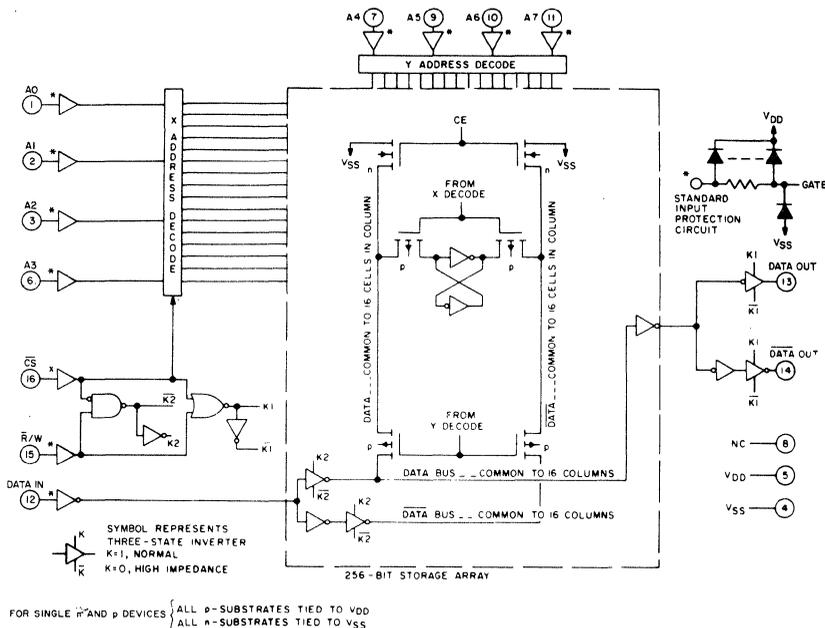


Fig. 1 - CD4061A logic diagram.

CD4061A OPERATIONAL MODES

OPERATION	ADDRESS LINES	CHIP-SELECT	READ/ WRITE	DATA IN	DATA OUTPUTS
Write "0"	Stable	0	1	0	High-Impedance
Write "1"	Stable	0	1	1	High-Impedance
Read	Stable	0	0	X	Valid 1 or 0
*Read Modify Write	Stable	0	0/1	X	Valid 1 or 0/High-Impedance
Address Change	Changing	1	X	X	High-Impedance

X = Don't Care

*For a READ MODIFY WRITE operation, CHIP SELECT may be held to logic 0 for the whole operation.

STATIC ELECTRICAL CHARACTERISTICS

(All inputs . . . $V_{SS} < V_i < V_{DD}$)

(Recommended DC Supply Voltage ($V_{DD} - V_{SS}$) . . . 3 to 15 V)

CHARACTERISTIC	TEST CONDITIONS		LIMITS							UNIT
	V _O (V)	V _{DD} (V)	-55°C		25°C			125°C		
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
Quiescent Device Current, I _L <i>See Fig. 14</i>	5	5	—	5	—	0.12	5	—	150	μA
	10	10	—	10	—	0.25	10	—	300	
Quiescent Device Dissipation/Package, P _D	5	5	—	—	—	0.6	25	—	750	μW
	10	10	—	—	—	2.5	100	—	3000	
Output Voltage Low-Level, V _{OL}	5	5	—	0.01	—	0	0.01	—	0.05	V
	10	10	—	0.01	—	0	0.01	—	0.05	
High-Level, V _{OH}	5	5	4.99	—	4.99	5	—	4.95	—	
	10	10	9.99	—	9.99	10	—	9.95	—	
Noise Immunity, (All Inputs) <i>See Fig. 17</i> V _{NL}	0.8	5	1.5	—	1.5	2.25	—	1.4	—	V
	1	10	3	—	3	4.5	—	2.9	—	
V _{NH}	4.2	5	1.4	—	1.5	2.25	—	1.5	—	
	9	10	2.9	—	3	4.5	—	3	—	
Output Drive Current: (Data Out, Data Out) N-Channel (Sink), I _{DN} <i>See Figs. 3, 4, 12</i>	0.4	4.5	2	—	1.6	2.5	—	1.1	—	mA
	0.5	10	4.3	—	3.5	5	—	2.4	—	
P-Channel (Source), I _{DP} <i>See Figs. 5, 6, 13</i>	2.5	5	-1.1	—	-0.9	-1.8	—	-0.65	—	
	4.6	5	-0.5	—	-0.4	-0.8	—	-0.3	—	
	9.5	10	-1.1	—	-0.9	-1.8	—	-0.65	—	
Output Off Resistance (High-Impedance State), R _O (Off)	5	5	10	—	10	—	—	10	—	
	10	10	10	—	10	—	—	10	—	

DYNAMIC ELECTRICAL CHARACTERISTICS

at $T_A = 25^\circ\text{C}$, $V_{SS} = 0\text{ V}$, $C_L = 50\text{ pF}$, and $t_r, t_f = 20\text{ ns}$

CHARACTERISTIC	TEST CONDITIONS	LIMITS				UNITS
		V _{DD} (V)	MIN.*	TYP.	MAX.*	
READ CYCLE TIME						
Read Cycle	t_{RC}	5	1200	1000	—	ns
		10	550	450	—	
Address Setup	t_{ADS}	5	40	0	—	ns
		10	0	—	—	
Chip Select	$t_{\overline{CS}}$	5	700	500	—	ns
		10	350	250	—	
Address Hold	t_{ADH}	5	460	—	—	ns
		10	200	—	—	
Read Access	t_{RA}	5	—	450	750	ns
		10	—	250	380	
Data Out Hold	t_{DOH}	5	110	170	230	ns
		10	130	160	190	
Data Out Active	t_{DOA}	5	80	120	160	ns
		10	40	70	100	
Output Transition	t_{TLH}	5	—	60	100	ns
		10	—	50	75	
	t_{THL}	5	—	35	60	
		10	—	25	40	
Chip-Select Input Rise and Fall Time,	t_{rCE} t_{fCE}	5	—	—	15	μs
		10	—	—	5	
		15	—	—	1	
WRITE CYCLE TIME						
Write Cycle	t_{WC}	5	1200	1000	—	ns
		10	550	450	—	
Address Setup	t_{ADS}	5	40	0	—	
		10	0	—	—	
Chip Select	$t_{\overline{CS}}$	5	700	500	—	
		10	350	250	—	
Address Hold	t_{ADH}	5	460	—	—	
		10	200	—	—	
Write Hold	t_{WRH}	5	150	100	—	
		10	100	70	—	
Write	t_{WRW}	5	150	100	—	
		10	100	70	—	
Data-In Setup	t_{DIS}	5	140	80	—	
		10	80	35	—	
Data-In Hold	t_{DIH}	5	25	10	—	
		10	20	10	—	

* See Symbols Definitions.

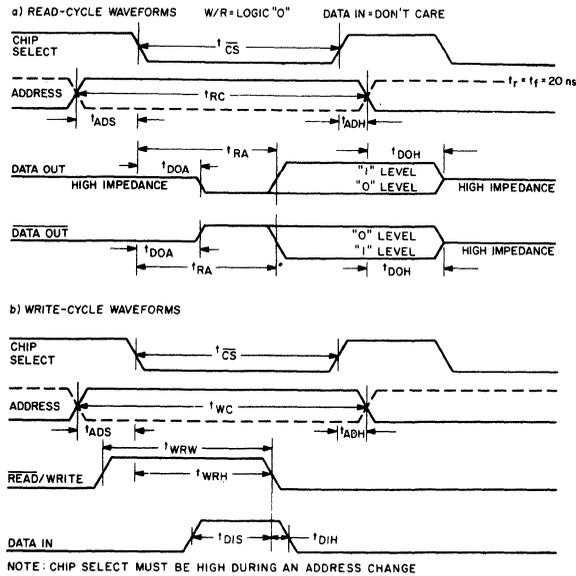


Fig. 2 - Typical write-read waveforms.

SYMBOL DEFINITIONS

- t_{RC}** - Read Cycle Time - Time required between address changes during a read cycle. Minimum read cycle time is equal to $t_{ADS(min)} + t_{CS}$ (min) + $t_{ADH(min)}$.
- t_{ADS}** - Address Setup Time - Time required before the $\overline{\text{Chip-Select}}$ voltage level can be lowered after the slowest address transition.
- t_{ADH}** - Address Hold Time - Time required before the earliest address transition can take place after $\overline{\text{Chip-Select}}$ voltage level has been increased. $t_{ADH(min)} + t_{ADS(min)}$ is the minimum time required to discharge internal nodes and allow setting of address decoders during an address transition. $\overline{\text{Chip-Select}}$ level must be high during each address change, even if only read or write cycles are successively performed. However, if address is not changed, the $\overline{\text{Chip-Select}}$ may remain in its active (low) state during successive read and write cycles.
- t_{CS}** - $\overline{\text{Chip Select}}$ Time - Time required for the $\overline{\text{Chip Select}}$ to be active for a valid memory cycle.
- t_{RA}** - Read Access Time - Measured from $\overline{\text{Chip Select}}$ negative going transition to the valid output data.
- t_{DOA}** - Data-Out Active - Time required before the high-impedance state of Data Output is changed to a low-voltage state and $\overline{\text{Data Output}}$ is changed to a high-voltage state. (If the read out data from a selected storage location is logic "1", then $\overline{\text{Data Output}}$ will rise and $\overline{\text{Data Output}}$ will fall. If the read out data is logic "0", both $\overline{\text{Data Output}}$ and $\overline{\text{Data Output}}$ will maintain their original states.
- t_{DOH}** - Data-Out Hold - Time required for the $\overline{\text{Data Output}}$ and $\overline{\text{Data Output}}$ to change from an active to a high-impedance state.
- t_{WC}** - Write Cycle Time - Time required between address changes during a write cycle. This time sets the maximum operating speed for the memory, with a minimum cycle time equal to $t_{ADS(min)} + t_{CS}$ (min) + $t_{ADH(min)}$.
- t_{WRH}** - Write Hold Time - Time required before the negative transition of $\overline{\text{R/W}}$ pulse with respect to the negative transition of the $\overline{\text{Chip-Select}}$ signal.
- t_{DIS}** - Data-In Setup Time - Time required for the data input to be valid before the negative transition of the $\overline{\text{R/W}}$ pulse.

t_{DIH} — Data-In Hold Time — Time required for the data input to be valid after R/W pulse is returned to a low level. The minimum data-in width is equal to $t_{DIS(min)} + t_{DIH(min)}$.

t_{WRW} — Write Width — Time required for the R/W pulse to be high. Note that the positive transition of this signal can be made after the Chip-Select signal is high. In addition, the high state of the R/W signal shall be within the Chip-Select active state by at least a t_{WRH} period.

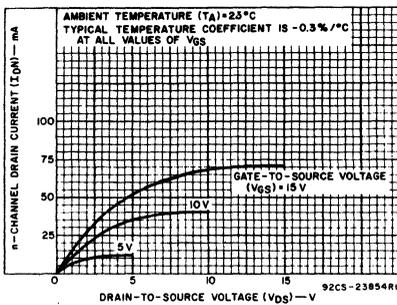


Fig. 3 — Typical n-channel drain characteristics.

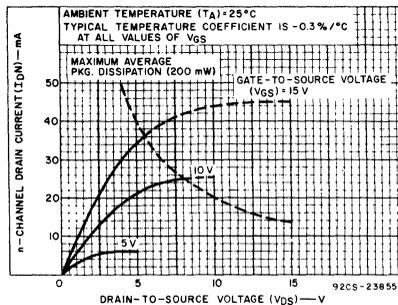


Fig. 4 — Minimum n-channel drain characteristics.

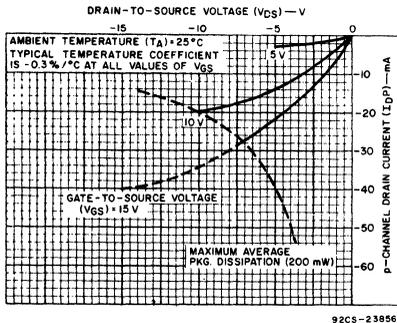


Fig. 5 — Typical p-channel drain characteristics.

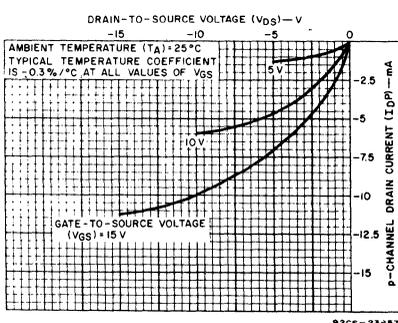


Fig. 6 — Minimum p-channel drain characteristics.

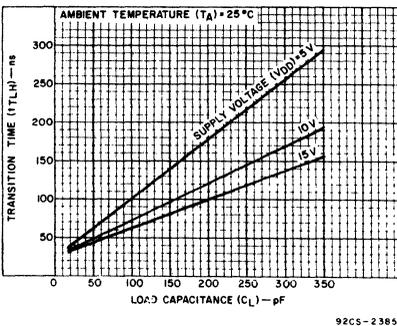


Fig. 7 — Typical low-to-high transition time (t_{TLH}) vs. C_L .

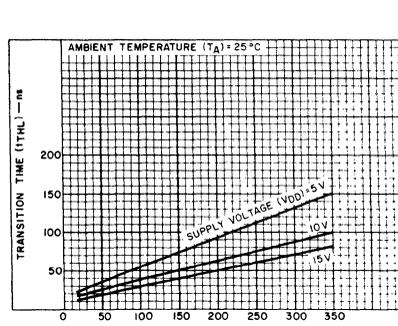


Fig. 8 — Typical high-to-low transition time (t_{THL}) vs. C_L .

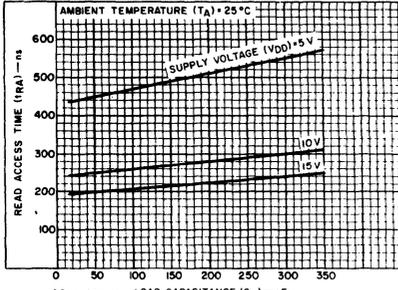


Fig. 9 – Typical read access time (t_{RA}) vs. C_L .

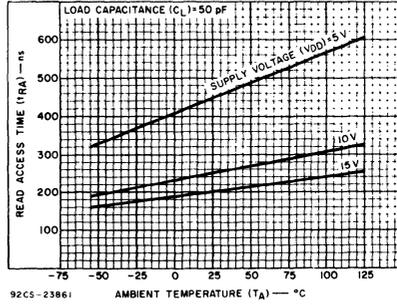


Fig. 10 – Typical read access time (t_{RA}) vs. temperature.

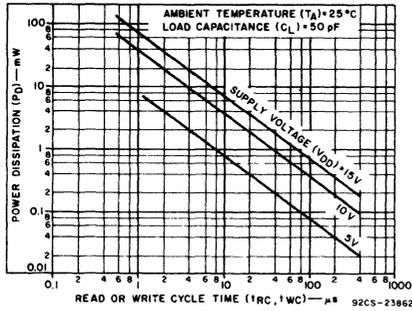
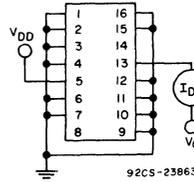


Fig. 11 – Typical power dissipation vs. cycle time.



Note: At address "0", "0" stored in memory.

Fig. 12 – N-channel drive current.

Note for Fig. 12 and Fig. 13:
Power dissipation measured using random data pattern. Input pulse delays and widths set to minimum values specified on data sheet with the exception of cycle time, 15 V setups identical to 10 V data sheet values, with the exception of $t_{CE} = 400$ ns.

Note: At address 0, "1" stored in memory.

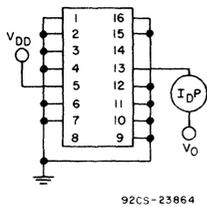


Fig. 13 – P-channel drive current.

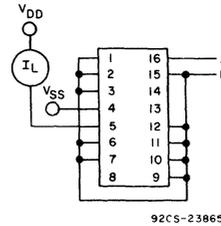


Fig. 14 – Quiescent device current.

Quiescent Device Current Test Conditions

Test	A	B	Memory Cells
1	0	0	All 0
2	1	1	All 0
3	0	1	All 0
4	0	0	All 1
5	1	1	All 1
6	0	1	All 1

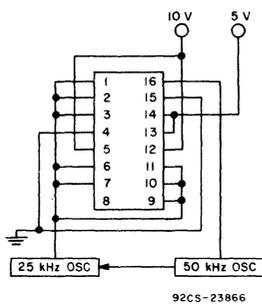
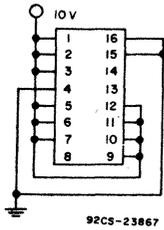


Fig. 15 – Operating life.

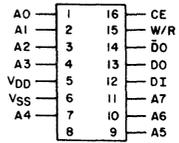
Note: Connection to all terminals in Figs. 15 & 16 (except 4 and 5) are made through 47 kΩ resistors.

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CD4061A



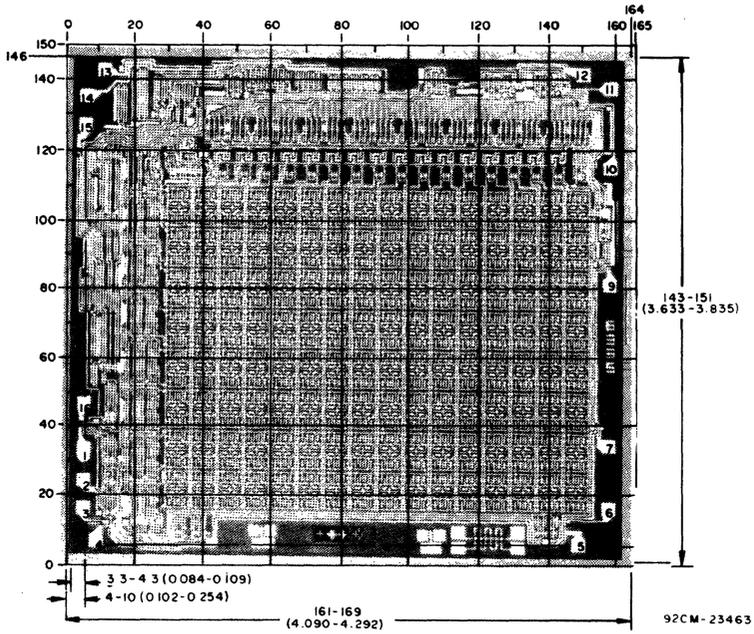
Description of Test:
 Functional test run with random data input. All inputs toggle between 30% and 70% of V_{DD} .

Fig. 16 - Bias life.



92CS-23868

Fig. 17 - Noise immunity.



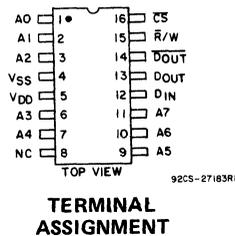
Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid Graduations are in Mils (10^{-3} inch).

Dimensions and pad layout for CD4061A.

COS/MOS 256-Word by 1-Bit Static Random-Access Memory

Features:

- Organization — 256-words by 1-bit
- COS/MOS compatible inputs and outputs
- Low power dissipation (typ.) @ 700 nS cycle time:
 - 10 nW/Bit standby @ $V_{DD} = 5\text{ V}$
 - 0.1 mW/Bit operating @ $V_{DD} = 5\text{ V}$
 - 40 nW/Bit standby @ $V_{DD} = 10\text{ V}$
 - 0.4 mW/Bit operating @ $V_{DD} = 10\text{ V}$
- Access time (typ.):
 - 265 nS @ $V_{DD} = 10\text{ V}$; 700 nS @ $V_{DD} = 5\text{ V}$
- Noise immunity (typ.): 30% of V_{DD}
- TTL output drive capability
- 3-State complementary data outputs
- Separate data-in and data-out lines



The RCA-CD40061 and CD40061A are 256-word by 1-bit COS/MOS fully static random access memories. They are similar in terminal arrangement and function to the CD4061A, except that the requirement for the Chip-Select input to return to a high level between address changes is eliminated.

The CD40061AD and CD40061AE have maximum supply voltage ratings of 12 V; the CD40061E maximum rating is 7 V. These devices are fully decoded and utilize eight Address inputs (A_0 - A_7) to select one of the 256 storage locations. Additional connections are provided for an active Low Chip-Select (\overline{CS}), a Read/Write command ($\overline{R/W}$), a Data input (DATA IN), an active High 3-State Output (DATA OUT), and an active Low 3-

State Output ($\overline{DATA\ OUT}$). DATA OUT is the same voltage state as DATA IN.

The Chip-Select input must be low to enable the Read or Write operations. A high level both inhibits these functions and causes the outputs to exhibit a high impedance. Output voltage levels appear at the output only when both \overline{CS} and $\overline{R/W}$ inputs are at low levels. These outputs interface directly with TTL devices.

Both the CD40061E and CD40061AE are supplied in 16-lead dual-in-line plastic packages. The CD40061A is supplied in a hermetically sealed 16-lead dual-in-line ceramic side-brazed package. The CD40061 is also supplied in chip form (H suffix).

CD40061 and CD40061A OPERATIONAL MODES

MODE	$\overline{CHIP-SELECT}$	$\overline{READ/WRITE}$	DATA OUT	$\overline{DATA\ OUT}$
Write	0	1	High Impedance	High Impedance
Read	0	0	Storage State	Complement of Storage State
Unselected	1	X	High Impedance	High Impedance

1 = High Level

0 = Low Level

X = Don't Care

RCA CMOS LSI Products

CD40061, CD40061A

MAXIMUM RATINGS, Absolute-Maximum Values:

SUPPLY-VOLTAGE RANGE ($V_{DD} - V_{SS}$):	
CD40061E	-0.5 to 7 V
CD40061AD, CD40061AE	-0.5 to 12 V
RECOMMENDED DC SUPPLY VOLTAGE RANGE ($V_{DD} - V_{SS}$):	
CD40061E	3 to 6 V
CD40061AD, CD40061AE	3 to 11 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to $V_{DD} + 0.5$ V
DC INPUT CURRENT ANY ONE INPUT	± 10 mA
RECOMMENDED INPUT VOLTAGE SWING	V_{DD} to V_{SS}
DEVICE DISSIPATION (per package)	200 mW
OPERATING-TEMPERATURE RANGE:	
CERAMIC-PACKAGE TYPE (CD40061AD)	-55 to +125°C
PLASTIC-PACKAGE TYPES (CD40061E, CD40061AE)	-40 to +85°C
STORAGE-TEMPERATURE RANGE	-65 to +150°C
LEAD TEMPERATURE (During soldering):	
At distance $1/16 \pm 1/32$ inch (1.59 ± 0.79 mm) from case for 10 seconds max.	265°C

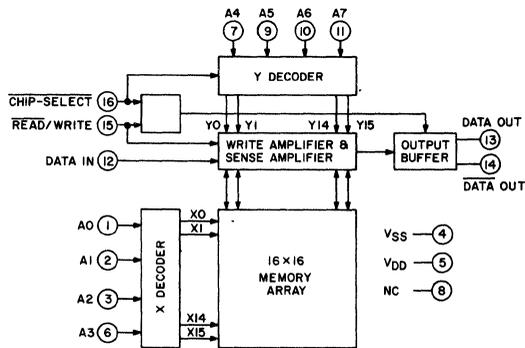


Fig. 1 — Functional block diagram for CD40061 and CD40061A.

STATIC ELECTRICAL CHARACTERISTICS

Values shown for $V_{DD} = 5$ V apply to all types, values shown for $V_{DD} = 10$ V apply to the CD40061AD and CD40061AE only.

CHARACTERISTIC	TEST CONDITIONS		LIMITS Full Temp. Range		TYPICAL VALUES	UNITS
	V_O (V)	V_{DD} (V)	Min.	Max.	at 25°C	
Quiescent Device Current, I_{DD}		5	—	10	0.5	μ A
		10	—	20	1	
Output Voltage, Low Level, V_{OL}		5	—	0.05	0	V
		10	—	0.05	0	
Output Voltage, High Level, V_{OH}		5	4.95	—	5	V
		10	9.95	—	10	
Output Current, Low Level, I_{OL}	0.4	5	0.85	—	1.1	mA
	0.5	10	2.1	—	2.8	
Output Current, High Level, I_{OH}	4.5	5	-0.3	—	-0.4	mA
	9	10	-0.6	—	-0.9	
Noise Immunity, All Inputs Low, V_{NL}	0.8	5	1	—	1.5	V
	1	10	2	—	3	
Noise Immunity, All Inputs High, V_{NH}	4.2	5	1	—	1.5	V
	9	10	2	—	3	
Output Resistance, Off State, R_O (off)		5	5	—	10	M Ω
		10	5	—	10	

DYNAMIC ELECTRICAL CHARACTERISTICS at $V_{DD} \pm 5\%$, Input t_r ,
 $t_f = 20$ ns, and $C_I = 50$ pF, see Note 2.

Values shown for $V_{DD} = 5$ V apply to all types; values shown for $V_{DD} = 10$ V apply to the CD40061AD and CD40061AE only.

READ CYCLE TIMES (For waveforms, see Figs. 2, 3, and 4)

CHARACTERISTIC	TEST CONDITIONS $V_{DD}(V)$	LIMITS* Full Temp. Range		TYPICAL VALUES at 25°C	UNITS
		Min.	Max.		
Chip-Select, (Note 1) $t_{\overline{CS}}$	5	880	—	720	ns
	10	380	—	290	
Address Setup, (Note 2) t_{ADS}	5	40	—	20	ns
	10	20	—	10	
Address Hold, t_{ADH}	5	0	—	—5	ns
	10	0	—	—5	
Read Setup, t_{RDS}	5	0	—	—5	ns
	10	0	—	—5	
Read Hold, t_{RDH}	5	0	—	—5	ns
	10	0	—	—5	
Data Out Hold, t_{DOH}	5	—	65	40	ns
	10	—	40	20	
Data Out Active, t_{DOA}	5	—	50	35	ns
	10	—	35	25	
Read Cycle, (Note 3) t_{RC}	5	880	—	720	ns
	10	380	—	290	
Access, t_{ACC}	5	—	850	700	ns
	10	—	345	265	

WRITE CYCLE TIMES (For waveforms, see Figs. 2,3, and 4)

CHARACTERISTIC	TEST CONDITIONS $V_{DD}(V)$	LIMITS* Full Temp. Range		TYPICAL VALUES at 25°C	UNITS
		Min.	Max.		
Chip-Select, $t_{\overline{CS}}$	5	420	—	350	ns
	10	200	—	150	
Address Setup, (Note 2) t_{ADS}	5	40	—	20	ns
	10	20	—	10	
Address Hold, t_{ADH}	5	0	—	—5	ns
	10	0	—	—5	
Write Setup, t_{WRS}	5	330	—	270	ns
	10	190	—	140	
Write Width, t_{WRW}	5	330	—	270	ns
	10	190	—	140	
Data In Setup, t_{DIS}	5	0	—	—5	ns
	10	0	—	—5	
Data In Hold, t_{DIH}	5	40	—	20	ns
	10	20	—	10	
Write Cycle, (Note 3) t_{WC}	5	480	—	400	ns
	10	240	—	180	

For footnotes, see page 4.

RCA CMOS LSI Products
CD40061, CD40061A

DYNAMIC ELECTRICAL CHARACTERISTICS (Cont'd)
READ/MODIFY/WRITE TIMES (For waveforms, see Figs. 2, 3, and 4)

CHARACTERISTIC	TEST CONDITIONS V _{DD} (V)	LIMITS* Full Temp. Range		TYPICAL VALUES at 25°C	UNITS
		Min.	Max.		
Chip-Select, (Note 1) $\overline{t_{CS}}$	5	1190	—	980	ns
	10	545	—	410	
Address Setup, (Note 2) t_{ADS}	5	40	—	20	ns
	10	20	—	10	
Address Hold, t_{ADH}	5	0	—	—5	ns
	10	0	—	—5	
Read Setup, t_{RDS}	5	0	—	—5	ns
	10	0	—	—5	
Data Out Active, t_{DOA}	5	—	50	35	ns
	10	—	35	25	
Previous Data Hold, t_{PDH}	5	—	65	50	ns
	10	—	40	25	
Access, t_{ACC}	5	—	850	700	ns
	10	—	345	265	
Read Width Effective, t_{RDW}	5	860	—	710	ns
	10	355	—	270	
Write Setup, t_{WRS}	5	330	—	270	ns
	10	190	—	140	
Write Width, t_{WRW}	5	330	—	270	ns
	10	190	—	140	
Data In Setup, t_{DIS}	5	0	—	—5	ns
	10	0	—	—5	
Data In Hold, t_{DIH}	5	40	—	20	ns
	10	20	—	10	
Read/Modify/Write Cycle, (Note 3) t_{RWC}	5	1230	—	1000	ns
	10	570	—	430	

● The maximum and minimum limit values of the dynamic characteristics under worst operating conditions are based on the time durations expressed in Figs. 2, 3, and 4. The minimum limit indicates the shortest time generated at the output or required at the input. The maximum limit indicates the longest time generated at the output or required at the input. The typical values are for 25°C and nominal voltage. Timing measurements for the transition period are taken at either the 0.8 V_{DD} or 0.2 V_{DD} point.

Note 1 — The chip-select times specified provide an active output data time of 50 ns minimum.

Note 2 — Address rise and fall times must be equal to or less than 1 μs under all conditions and for all modes.

Note 3 — Cycle time defines the shortest time in which this memory will correctly perform its desired function.

CAPACITANCES (V_I = 0, f = 1 MHz)

CHARACTERISTICS	Min.	Typ.	Max.	UNITS
Address Input, C _A	—	9	—	pF
Chip-Select, C _{CS}	—	9	—	pF
Read/Write Input, C _{WE}	—	5	—	pF
Data Input, C _{DI}	—	5	—	pF
Data Output, C _{DO}	—	10	—	pF

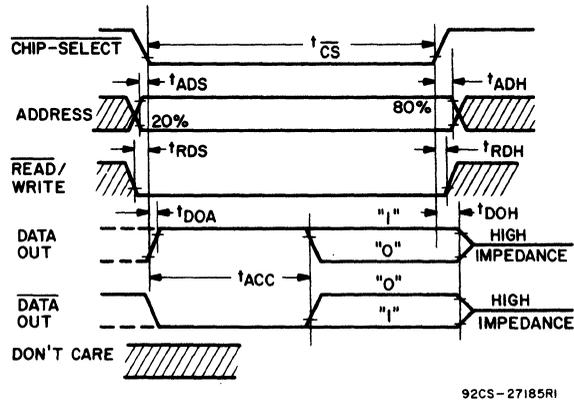


Fig.2 - Read cycle waveforms for CD40061, CD40061A.

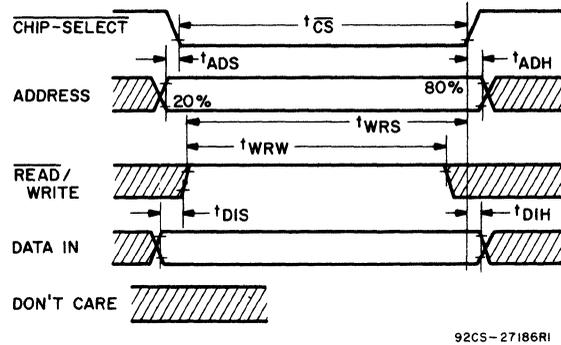


Fig.3 - Write cycle waveforms for CD40061, CD40061A.

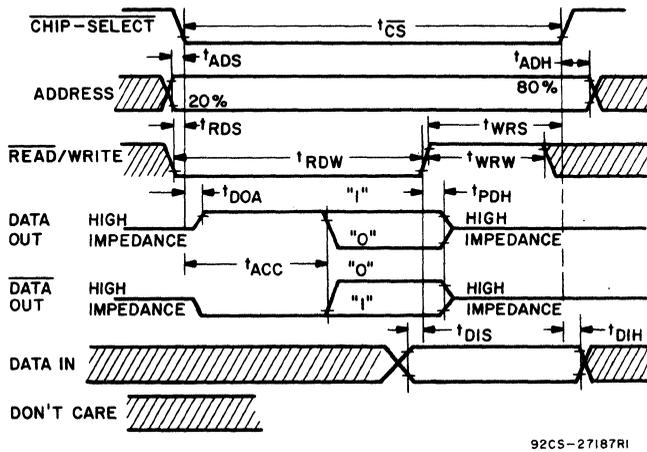


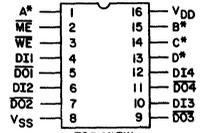
Fig.4 - Read/modify/write cycle waveforms for CD40061, CD40061A.

COS/MOS 64-Bit Random Access Memory

High-Voltage Types (20-Volt Rating)

Features:

- Input address latch
- 3-state outputs
- Low-power TTL compatible
- Equivalent to and pin-compatible with National 74C89
- Pin-compatible with 74S189
- Buffered inputs and outputs
- 100% tested for quiescent current at 20 V
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for description of "B" Series CMOS Devices"



TOP VIEW
 92CS-30960
 *ADDRESS INPUTS

Terminal Assignment

The RCA-CD40114B is a 16-word x 4-bit random access memory (RAM) with four address inputs, four data inputs, a WRITE ENABLE (WE) input, a MEMORY ENABLE (ME) input, and four 3-state data outputs. The four address inputs are decoded internally to select one of the 16 possible word locations. The address information is latched on the negative edge of the ME input by an internal address register. The selected output assumes a high-impedance condition when the device is writing or disabled. The ME input and the 3-state outputs allow memory expansion.

Applications:

- Main frame memories
- Scratch-pad memories
- Memory storage
- Games

\overline{ME}	\overline{WE}	OPERATION	CONDITION OF OUTPUTS
L	L	Write	3-STATE
L	H	Read	Complement of Selected Word
H	L	Inhibit, Storage	3-STATE
H	H	Inhibit, Storage	3-STATE

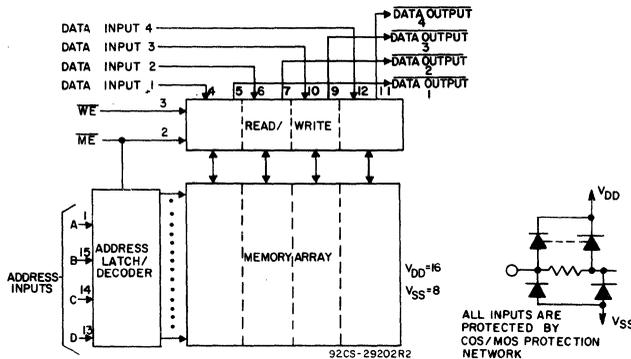


Fig. 1 — Functional Block Diagram

Address Operation

The high-to-low transition of \overline{ME} enables the memory. Address inputs must be stable (either high or low) prior to and during this transition, but it is not necessary to hold them stable beyond it.

Write Operation

When \overline{WE} and \overline{ME} are low, information present at the data inputs is written into the memory at the selected address.

Read Operation

When \overline{ME} is low and \overline{WE} is high the complement of the memory contents at the selected address location are non-destructively read out at the four data outputs.

The CD40114B is supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead plastic packages (E suffix), and in chip form (H suffix).

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	-0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to $V_{DD} + 0.5$ V
DC INPUT CURRENT, ANY ONE INPUT	± 10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For $T_A = -40$ to $+60^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +60$ to $+85^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at $12 \text{ mW}/^\circ\text{C}$ to 200 mW
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPES D, F)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPES D, F)	Derate Linearly at $12 \text{ mW}/^\circ\text{C}$ to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, H	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E	-40 to $+85^\circ\text{C}$
STORAGE TEMPERATURE RANGE (T_{stg})	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ inch (1.59 ± 0.79 mm) from case for 10 s max.	$+265^\circ\text{C}$

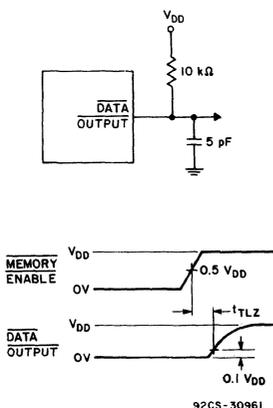


Fig. 2 — Output low to high-impedance transition time test circuit and waveforms.

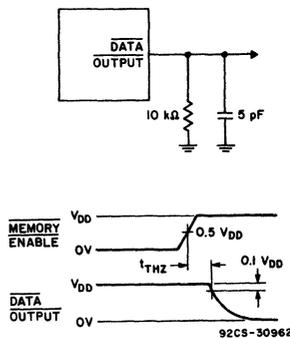


Fig. 3 — Output high to high-impedance transition time test circuit and waveforms.

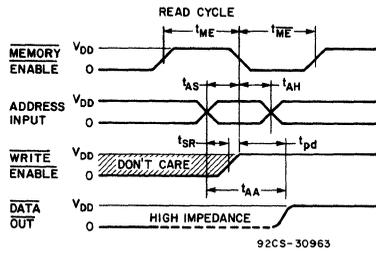


Fig. 4 – Read cycle waveforms.

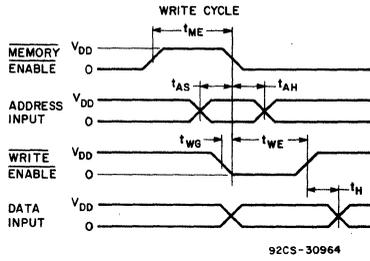


Fig. 5 – Write cycle waveforms

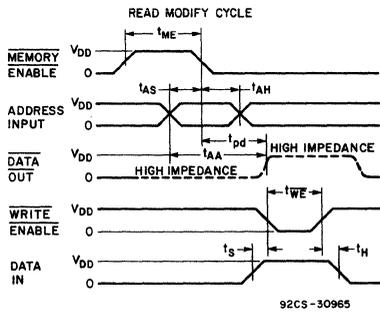


Fig. 6 – Read-modify-write cycle waveforms.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTER- ISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)	Values at -55, +25, +125 Apply to D,F,H Packages				Values at -40, +25, +85 Apply to E Package			
				-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current, I _{DD} Max.	-	0,5	5	5	5	150	150	-	0,04	5	μA
	-	0,10	10	10	10	300	300	-	0,04	10	
	-	0,15	15	20	20	600	600	-	0,04	20	
	-	0,20	20	100	100	3000	3000	-	0,08	100	
Output Low (Sink) Current I _{OL} Min.	0,4	0,5	5	0,64	0,61	0,42	0,36	0,51	1	-	mA
	0,5	0,10	10	1,6	1,5	1,1	0,9	1,3	2,6	-	
	1,5	0,15	15	4,2	4	2,8	2,4	3,4	6,8	-	
Output High (Source) Current, I _{OH} Min.	-4,6	0,5	5	-0,64	-0,61	-0,42	-0,36	-0,51	-1	-	mA
	2,5	0,5	5	-2	-1,8	-1,3	-1,15	-1,6	-3,2	-	
	9,5	0,10	10	-1,6	-1,5	-1,1	-0,9	-1,3	-2,6	-	
	13,5	0,15	15	-4,2	-4	-2,8	-2,4	-3,4	-6,8	-	
Output Voltage: Low-Level, V _{OL} Max.	-	0,5	5	0,05				-	0	0,05	V
	-	0,10	10	0,05				-	0	0,05	
	-	0,15	15	0,05				-	0	0,05	
Output Voltage: High-Level, V _{OH} Min.	-	0,5	5	4,95				4,95	5	-	V
	-	0,10	10	9,95				9,95	10	-	
	-	0,15	15	14,95				14,95	15	-	
Input Low Voltage, V _{IL} Max.	0,5, 4,5	-	5	1,5				-	-	1,5	V
	1,9	-	10	3				-	-	3	
	1,5, 13,5	-	15	4				-	-	4	
Input High Voltage, V _{IH} Min.	0,5, 4,5	-	5	3,5				3,5	-	-	V
	1,9	-	10	7				7	-	-	
	1,5, 13,5	-	15	11				11	-	-	
Input Current I _{IN} Max.	-	0,18	18	±0,1	±0,1	±1	±1	-	±10 ⁻⁵	±0,1	μA
3-State Output Leakage Current I _{OUT} Max.	0,18	0,18	18	±0,4	±0,4	±12	±12	-	±10 ⁻⁴	±0,4	μA

ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$, $C_L = 50 \text{ pF}$, $R_L = 200 \text{ k}\Omega$, $t_r, t_f = 20 \text{ ns}$

Unless Otherwise Specified

CHARACTERISTIC	TEST CONDITIONS	V _{DD} (V)	LIMITS		UNITS
			Typ.	Max.	
Access Time From Address Change, t_{AA}		5	325	650	ns
		10	140	280	
		15	120	240	
Min. Address Setup Time, t_{AS}		5	75	150	ns
		10	30	60	
		15	25	50	
Min. Address Hold Time, t_{AH}		5	30	60	ns
		10	20	40	
		15	15	30	
Min. Memory Enable Pulse Width, t_{ME} , $\overline{t_{ME}}$		5	200	400	ns
		10	75	150	
		15	60	120	
Min. $\overline{\text{Write Enable}}$ Setup Time For a Read, t_{SR}		5	—	0	ns
		10	—	0	
		15	—	0	
Min. $\overline{\text{Write Enable}}$ Setup Time for a Write, t_{WS}		5	—	t_{ME}	ns
		10	—	t_{ME}	
		15	—	t_{ME}	
Min. $\overline{\text{Write Enable}}$ Pulse Width, $\overline{t_{WE}}$		5	150	300	ns
		10	50	100	
		15	40	80	
Min. Data Input Hold Time, t_H		5	25	50	ns
		10	12	25	
		15	10	20	
Min. Data Input Setup Time, t_S		5	25	50	ns
		10	12	25	
		15	10	20	
Propagation Delay Time from Output-high or Output-low to High-Impedance State from Memory Enable	$R_L = 10 \text{ k}\Omega$ $C_L = 5 \text{ pF}$	5	150	300	ns
		10	60	120	
		15	50	100	
Propagation Delay Time from Output-high or Output-low to High-Impedance State from Write Enable	$R_L = 10 \text{ k}\Omega$ $C_L = 5 \text{ pF}$	5	150	300	ns
		10	60	120	
		15	50	100	
Propagation Delay Time From Memory Enable, t_{pd}		5	250	500	ns
		10	100	200	
		15	80	160	
Input Capacitance, C_{IN}	Any Input		5	7.5	pF
Output Capacitance, C_{OUT}	Any Output		6.5	13	pF

RCA CMOS LSI Products

CDM5332, CDM5333

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V _{DD}) (Voltage referenced to V _{SS} terminal)	-0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to V _{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P _D):	
For T _A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T _A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T _A = -55 to +100°C (PACKAGE TYPE D)	500 mW
For T _A = +100 to 125°C (PACKAGE TYPE D)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
For T _A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T _A):	
PACKAGE TYPE D	-55 to +125°C
PACKAGE TYPE E	-40 to +85°C
STORAGE-TEMPERATURE RANGE (T _{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

RECOMMENDED OPERATING CONDITIONS at T_A = -40 to +85°C

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
DC Operating Voltage Range	4	6.5	V
Input Voltage Range	V _{SS}	V _{DD}	

STATIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85°C, V_{DD} = 5 V ± 10%, Except as noted

CHARACTERISTIC		CONDITIONS		LIMITS ALL TYPES			UNITS
		V _O (V)	V _{IN} (V)	Min.	Typ.*	Max.	
Quiescent Device Current	I _{DD} Δ	—	0, V _{DD}	—	2	50	μA
Output Low Drive (Sink) Current	I _{OL}	0.4	0, V _{DD}	1.8	3.6	—	mA
Output High Drive (Source) Current	I _{OH}	V _{DD} -0.4	0, V _{DD}	-0.4	-0.8	—	
Output Voltage Low-Level	V _{OL}	—	0, V _{DD}	—	0	0.1	V
Output Voltage High-Level	V _{OH}	—	0, V _{DD}	V _{DD} -0.1	V _{DD}	—	
Input Low Voltage	V _{IL}	0.5, V _{DD} -0.5	—	—	—	0.8	
Input High Voltage	V _{IH}	0.5, V _{DD} -0.5	—	2.4	—	—	
Input Leakage Current (Any Input)	I _{IN}	—	0, V _{DD}	—	—	±1	μA
3-State Output Leakage Current	I _{OUT}	0, V _{DD}	0, V _{DD}	—	—	±1	
Input Capacitance	C _{IN}	—	—	—	5	7.5	pF _r
Output Capacitance	C _{OUT}	—	—	—	10	15	
Standby Device Current	I _{SBY} Δ	—	0.8V, 2.4V	—	0.25	0.5	mA
Operating Device Current	I _{OPER} Δ	—	0.8V, 2.4V	—	7.5	15	

*Typical values are for T_A = 25°C and nominal V_{DD}.

STATIC CHARACTERISTIC Device Current Test Conditions:

CHARACTERISTIC	CHIP SELECT STATUS	ADDRESS INPUT TO TOGGLE FREQUENCY	OUTPUT LOADING
I _{DD} Quiescent Device Current	Any Chip Select Disabled	0	Open Circuit
I _{SBY} — Standby Device Current	CS2 Disabled at TTL Level	1 MHz	Open Circuit
I _{OPER} — Operating Device Current	CS2 Active CS1 Don't Care	1 MHz	Open Circuit

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85° C, V_{DD} = 5 V ± 10%, Input tr, tr = 10 ns, Cl = 100 pf, 1 TTL Load

CHARACTERISTIC		LIMITS			UNITS
		Min. ⁺	Typ. [•]	Max.	
Address Access Time	t _{AA}	—	—	450	ns
Data Hold from Address or CS2	t _{DH}	50	—	—	
CS1/OE Enable to Bus Active	t _{CX}	0	—	150	
Data Float from CS1/OE Disabled	t _{DF}	—	—	120	
Output Hold from CS1/OE Disabled	t _{OH}	0	—	—	

⁺Time required by a limit device to allow for the indicated function.

[•]Typical values are for T_A = 25° C and nominal V_{DD}.

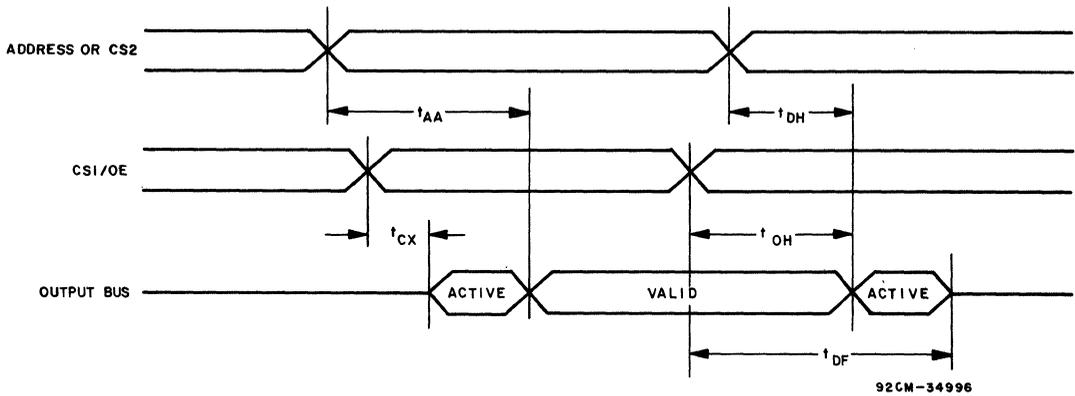


Fig. 2 - Timing waveforms.

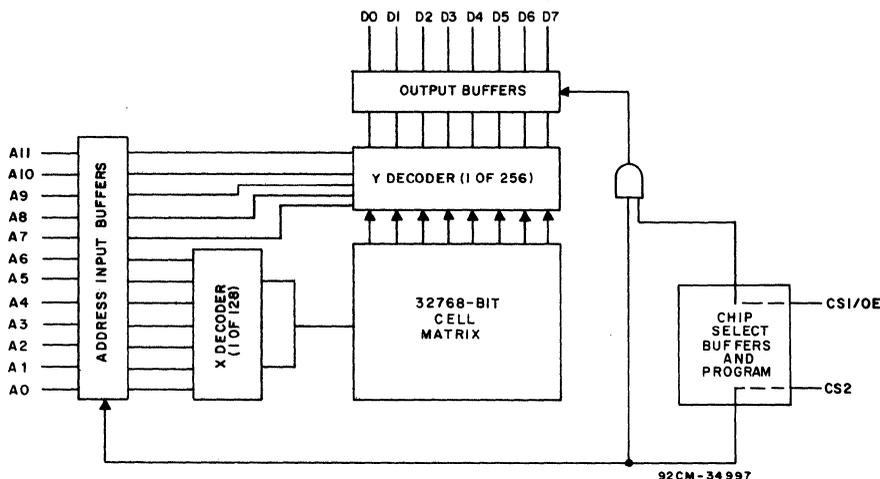


Fig. 3 - Functional block diagram.

ROM ORDERING INFORMATION

All RCA mask-programmable ROM's are custom-ordered devices. ROM program patterns can be submitted to RCA by using a master device (ROM, PROM or EPROM), a floppy

diskette generated on an RCA development system, or computer punch cards.

DATA PROGRAMMING INSTRUCTIONS

When a customer submits instructions for programming RCA custom ROM's, the customer must also complete the relevant parts of the ROM information sheet and submit this sheet together with the programming instructions. Programming instructions may be submitted in any one of three ways, as follows:

1. **Computer-Card Deck** — use standard 80-column computer punch cards.
2. **Floppy Diskette** — diskette information must be generated on an RCA CDP1800-series microprocessor development system.

3. **Master Device** — a ROM, PROM, or EPROM that contains the required programming information.

The requirements for each method are explained in detail in the following paragraphs:

Computer-Card Method

Use standard 80-column computer cards. Each card deck must contain, in order, a title card, an option card, a data-format card, and data cards. Punch the cards as specified in the following charts:

TITLE CARD

Column No.	Data
1	Punch T
2-5	leave blank
6-30	Customer Name (start at 6)
31-34	leave blank
35-54	Customer Address or Division (start at 35)
55-58	leave blank
59-63	RCA custom selection number (5 digits) (Obtained from RCA Sales Office)
64	leave blank
65-71	RCA device type, without CDM prefix, e.g. 5332E
72	Punch an opening parenthesis (
73	Punch 8
74	Punch an closing parenthesis)
75-78	leave blank
79-80	Punch a 2-digit decimal number to indicate the deck number; the first deck should be numbered 01

DATA PROGRAMMING INSTRUCTIONS (Cont'd)
OPTION CARD

Use the ROM Information Sheet to select the polarity options, P, N, or X, for the desired ROM type.

Column No.	Data
1-6	Punch the word OPTION
7	leave blank
8-17	RCA device type, including CDM prefix, e.g. CDM5332E
18-27	leave blank
28-29	Punch P or N per ROM Information Sheet
30-39	Punch X or leave blank per ROM Information Sheet
40-78	leave blank
79-80	Punch the deck number (the 2-digit number in columns 79-80 of the title card)

DATA-FORMAT CARD

The data-format card specifies the form in which the data is to be entered into ROM.

Column No.	Data
1-11	Punch the words DATA FORMAT
12	leave blank
13-15	Punch the letters HEX
16	leave blank
17-19	Punch POS
20-78	leave blank
79-80	Punch the deck number (the 2-digit number in columns 79-80 of the title card)

DATA CARDS

The data cards contain the hexadecimal data to be programmed into the ROM device.
Each card must contain the starting address plus sixteen words of data in clusters of four Hex Bytes.

Column No.	Data	Column No.	Data
1-4	Punch the starting address in hexadecimal for the following data.*	26-27	2 hex digits of 9th WORD
5	Blank	28-29	2 hex digits of 10th WORD
6-7	2 hex digits of 1st WORD	30	Blank
8-9	2 hex digits of 2nd WORD	31-32	2 hex digits of 11th WORD
10	Blank	33-34	2 hex digits of 12th WORD
11-12	2 hex digits of 3rd WORD	35	Blank
13-14	2 hex digits of 4th WORD	36-37	2 hex digits of 13th WORD
15	Blank	38-39	2 hex digits of 14th WORD
16-17	2 hex digits of 5th WORD	40	Blank
18-19	2 hex digits of 6th WORD	41-42	2 hex digits of 15th WORD
20	Blank	43-44	2 hex digits of 16th WORD
21-22	2 hex digits of 7th WORD	45	Blank if last card, semicolon follow
23-24	2 hex digits of 8th WORD	46-78	Blank
25	Blank	79-80	Punch 2 decimal digits as in title card

*The address block must be contiguous starting at an even-numbered address.
Column 4 must be zero.

RCA CMOS LSI Products

CDM5332, CDM5333

To minimize power consumption, all unused ROM locations should contain zeros.

Floppy-Diskette Method

The diskette contains the ROM address and data information. Title, option, and data-format information, which would otherwise be punched on computer cards, must be submitted on the ROM Information Sheet. In addition, specify the RCA Development System used to generate the diskette (CDP18S005, CDP18S007, or CDP18S008) and supply a track number or file name. If possible, include a printout of the program for verification purposes. The format of the address and data information is essentially the same as that described for Computer-Card method with the addition of a carriage-return character at the end of each line and an end-of-file character (DC3) at the end of the file.

Master-Device Method

Data may be submitted on a master ROM, PROM, or EPROM device. Title, option, and data-format information,

which would otherwise be punched on computer cards, must be submitted on the ROM Information Sheet. In addition, specify the master device type; RCA will accept Intel types 1702, 2704, 2708, 2716, 2732, 2332A, 2758, Supertex CM3200, T.I. TMS4732, Motorola type: MCM68732 and MCM68A332 or their equivalents as well as RCA type CDP18U42. If the ROM to be manufactured is smaller in memory size than the master device, or if more than one ROM pattern is stored in the master device, the starting address and size of each pattern must be stated on separate ROM Information Sheets.

If the Master-Device is smaller than 4 kilobytes, the starting address of each Master-Device must be clearly identified.

For additional information refer to the following RCA publications:

"Sales Policy and Programming Instructions for RCA Custom ROMs", RPP-610.

"Programming 2732 PROMs with the CDP18S480 PROM Programmer", RCA Application Note ICAN-6847.

ROM INFORMATION SHEET

How is ROM pattern being submitted to RCA?

- check one
- Computer Cards** (Complete part B)
 - Floppy Diskette** (Complete parts A, B, and D)
 - Master Device (PROM)** (Complete parts A, B, and C)

PART A	6-30	Customer Name (start at left)									
	35-54	Address or Division									
	59-63	RCA Custom Number (Obtained from RCA Sales Office)									
	65-71	ROM Type (without CDM prefix), e.g. 5332E									

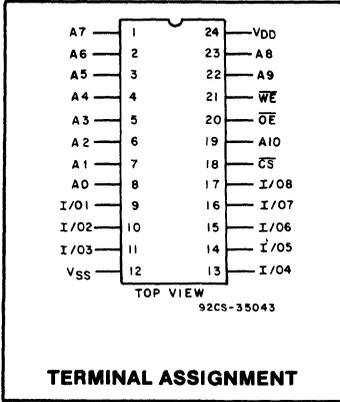
PART B	ROM TYPE Circle one	Circle the ROM type desired, then circle one letter (P, N, or X) In each column for that ROM.									
	Pin Functions	P = active when logic 1, N = active when logic 0, X = don't care									
		CS1	CS2								
CDM5332		PN	PN	X	X	X	X	X	X	X	X
Polarity Options											
CDM5333		PN	PN	X	X	X	X	X	X	X	X
Polarity Options											
Column #		28	29	30	31	32	34	36	37	38	39

PART C	If a master device is submitted, state type of ROM/PROM:
	Starting and last address of data block in the Master Device (in Hex).
	<div style="display: flex; justify-content: space-around;"> <div style="border: 1px solid black; width: 40px; height: 20px;"></div> <div style="border: 1px solid black; width: 40px; height: 20px;"></div> </div>

PART D	If a diskette is submitted, check type of RCA Development System used:
	<input type="checkbox"/> CDP18S005 <input type="checkbox"/> CDP18S007
	Specify: Track # <input style="width: 20px; height: 20px;" type="text"/> <input type="checkbox"/> CDP18S008
	Software program used: (check one) Specify: File Name: (check one)
	<input type="checkbox"/> ROM SAVE <input type="checkbox"/> MEM SAVE <input type="checkbox"/> SAVE PROM <input type="checkbox"/> SAVE PROM

Preliminary Data

CMOS 2048-Word by 8-Bit LSI Static RAM



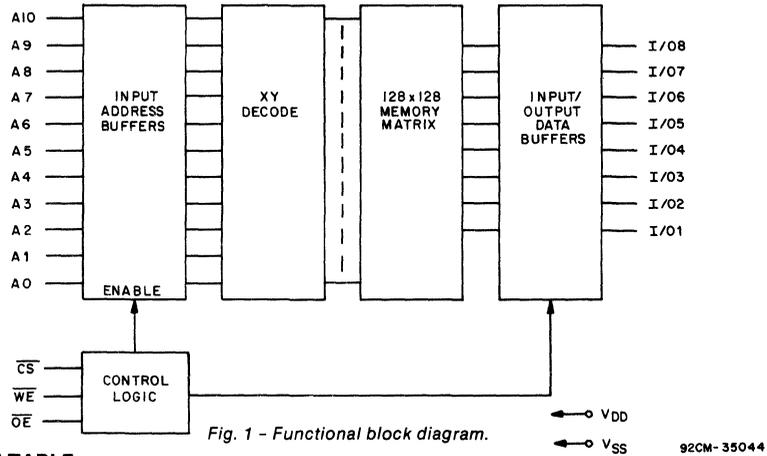
Features:

- Fully static operation
- Single power supply - 4.5 V to 5.5 V
- All inputs and outputs directly TTL compatible
- 3-state outputs
- Industry standard 24 pin configuration
- Input address buffers gated off with chip deselect
- Fast access time
- Low standby and operating power - $I_{DDS1} = 1 \mu A$ typical, $I_{OPER} = 35 mA$ maximum
- Data retention voltage - 2 V min.
- Operating temperature range (Max. Rating) - 0° to 70°C

The RCA-CDM6116 is a 2048-word by 8-bit static random-access memory. It is designed for use in memory systems where high-speed, low power and simplicity in use are desirable. This type has common data input and data output and utilizes a single power supply of 4.5 V to 5.5 V.

The input address buffers are gated off with chip deselect for minimum standby power with inputs toggling.

The CDM6116 is supplied in 24-lead, hermetic, dual-in-line side-brazed ceramic (D suffix) and in 24-lead dual-in-line plastic packages (E suffix).



TRUTH TABLE

\overline{CS}	\overline{OE}	\overline{WE}	A0 TO A10	MODE	DATA I/O
H	X	X	X	STANDBY	HIGH Z
L	L	H	STABLE	READ	DATA OUT
L	H	L	STABLE	WRITE	DATA IN
L	L	L	STABLE	WRITE	DATA IN

L = LOW H = HIGH X = DON'T CARE

RCA CMOS LSI Products

CDM6116-1, CDM6116-2

MAXIMUM RATING, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V _{DD}):	
(All voltage values referenced to V _{SS} terminal)	-0.3 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.3 to +7 V
POWER DISSIPATION PER PACKAGE (P _D):	
For T _A = 0° to +60° C (PACKAGE TYPE E)	500 mW
For T _A = +60 to +70° C (PACKAGE TYPE E)	Derate Linearly at 12 mW/° C to 380 mW
For T _A = 0° to +70° C (PACKAGE TYPE D)	500 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
For T _A = FULL PACKAGE-TEMPERATURE RANGE	100 mW
OPERATING-TEMPERATURE RANGE (T _A):	
PACKAGE TYPE D	0 to +70° C
PACKAGE TYPE E	0 to +70° C
STORAGE TEMPERATURE RANGE (T _{stg})	-55 to +125° C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265° C

OPERATING CONDITIONS at T_A = 0° to +70° C

For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	ALL TYPES		
	MIN.	MAX.	
DC Operating Voltage Range	4.5	5.5	V
Input Voltage Range	V _{IH}	V _{DD} + 0.3	
	V _{IL}	-0.3	

STATIC ELECTRICAL CHARACTERISTICS at T_A = 0 to +70° C, V_{DD} = 5 V ± 10%, Except as noted

CHARACTERISTIC	CONDITIONS	LIMITS						UNITS	
		CDM6116-1			CDM6116-2				
		MIN.	TYP.*	MAX.	MIN.	TYP.*	MAX.		
Standby Device Current	I _{DDS}	$\overline{CS} = V_{IH}$	—	0.6	2	—	0.6	2	mA
Current	I _{DDS1}	$\overline{CS} = V_{DD} - 0.2 V$	—	1	100	—	1	30	μA
Output Voltage	V _{OL} Max.	I _{OL} = 2.1 mA	—	—	0.4	—	—	0.4	V
Low-Level		I _{OL} = 1 μA	—	0.1	—	—	0.1	—	
Output Voltage	V _{OH} Min.	I _{OH} = -1 mA	2.4	—	—	2.4	—	—	V
High Level		I _{OH} = -1 μA	—	V _{DD} -0.1	—	—	V _{DD} -0.1	—	
Input Leakage Current	I _{IN} Max.	V _{DD} = 5.5 V V _{IN} = 0 V to V _{DD}	—	±0.1	±2	—	±0.1	±2	μA
3-State Output Leakage Current	I _{OUT}	\overline{CS} or $\overline{OE} = V_{IH}$ V _{I/O} = 0 V to V _{DD}	—	±0.5	±2	—	±0.5	±2	
Operating Device Current	I _{OPER#}	V _{IN} = V _{IL} , V _{IH}	—	20	35	—	20	35	mA
Input Capacitance	C _{IN}	V _{IN} = 0 V, f = 1 MHz, T _A = 25° C	—	4	6	—	4	6	pF
Output Capacitance	C _{I/O}	V _{I/O} = 0 V, f = 1 MHz, T _A = 25° C	—	6	8	—	6	8	

*Typical values are for T_A = 25° C and nominal V_{DD}.

#Outputs open circuited; cycle time = Min. t_{cycle}, duty = 100%

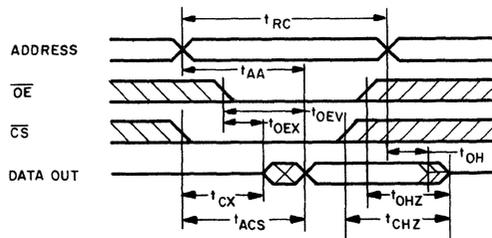
General-Purposes Memories
CDM6116-1, CDM6116-2

**DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 0$ to $+70^\circ\text{C}$, $V_{DD} = 5\text{ V} \pm 10\%$,
Input $t_r, t_f = 10\text{ ns}$; $C_L = 100\text{ pF}$ and 1 TTL Load, Input Pulse Levels: 0.8 V to 2.4 V**

Read Cycle Times See Fig. 2

CHARACTERISTIC		LIMITS				UNITS
		CDM6116-1		CDM6116-2		
		MIN.†	MAX.	MIN.†	MAX.	
Read Cycle Time	t_{RC}	250	—	200	—	ns
Address Access Time	t_{AA}	—	250	—	200	
Chip Select Access Time	t_{ACS}	—	250	—	200	
Chip Select to Output Active	t_{CX}	15	—	15	—	
Output Enable to Output Valid	t_{OEV}	—	150	—	120	
Output Enable to Output Active	t_{OEX}	15	—	15	—	
Chip Deselect to Output High Z	t_{CHZ}	0	80	0	60	
Output Disable to Output High Z	t_{OHZ}	0	80	0	60	
Output Hold from Address Change	t_{OH}	15	—	15	—	

†Time required by a limit device to allow for the indicated function.



NOTE:

WE IS HIGH DURING READ CYCLE.
TIMING MEASUREMENT REFERENCE
LEVEL IS 1.5 V

92CS-35042

Fig. 2 - Read-cycle timing waveforms.

General-Purposes Memories

CDM6116-1, CDM6116-2

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 0$ to $+70^\circ\text{C}$, $V_{DD} = 5\text{V} \pm 10\%$,

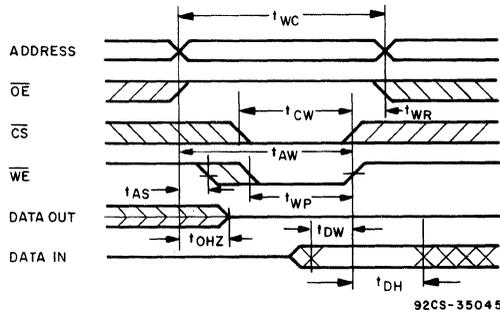
Input $t_r, t_f = 10\text{ ns}$; $C_L = 100\text{ pF}$ and 1 TTL Load, Input Pulse Levels: 0.8 V to 2.4 V

Write Cycle Times See Fig. 3

CHARACTERISTIC		LIMITS				UNITS
		CDM6116-1		CDM6116-2		
		MIN.†	MAX.	MIN.†	MAX.	
Write Cycle Time	t_{WC}	250	—	200	—	ns
Chip Select to End of Write	t_{CW}	200	—	160	—	
Address Valid to End of Write	t_{AW}	200	—	160	—	
Address Setup Time	t_{AS}	0	—	0	—	
Write Pulse Width	t_{WP}	200	—	160	—	
Write Recovery Time	t_{WR}	10	—	10	—	
Output Disable to Output High Z	t_{OHZ}	0	80	0	60	
Write to Output High Z	t_{WHZ}	0	80	0	60	
Input Data Setup Time	t_{DW}	100	—	80	—	
Input Data Hold Time	t_{DH}	10	—	10	—	
Output Active from End of Write	t_{OW}	10	—	10	—	

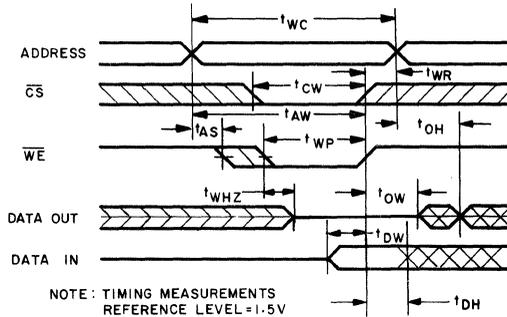
†Time required by a limit device to allow for the indicated function.

WRITE CYCLE (1):



92CS-35045

WRITE CYCLE (2): $\overline{OE} = \text{LOW}$



NOTE: TIMING MEASUREMENTS
REFERENCE LEVEL = 1.5V

92CS-35046

Fig. 3 - Write cycle timing waveforms.

DATA RETENTION CHARACTERISTICS at $T_A = 0$ to 70°C ; See Fig. 4.

CHARACTERISTIC	TEST CONDITIONS	LIMITS		UNITS	
		ALL TYPES			
		MIN.	MAX.		
Minimum Data Retention Voltage	V_{DR}	$\overline{CS} \geq V_{DD} - 0.2\text{ V}$	2	—	V
Data Retention Quiescent Current	I_{DDDR}	$V_{DD} = 3\text{ V}, \overline{CS} \geq 2.8\text{ V}$	—	50	μA
	CDM6116-1				
		CDM6116-2	—	15	
Chip Deselect to Data Retention Time	t_{CDR}	See Fig. 4	0	—	ns
Recovery to Normal Operation Time	t_R	See Fig. 4	* t_{RC}	—	

* t_{RC} = Read Cycle Time

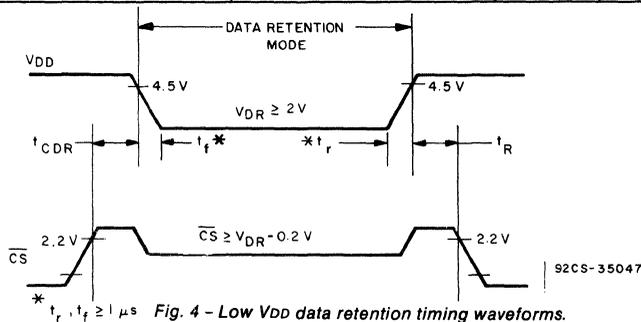


Fig. 4 - Low V_{DD} data retention timing waveforms.

OPERATING AND HANDLING CONSIDERATIONS

1. Handling

All inputs and outputs of RCA CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in ICAN-6525, "Guide to Better Handling and Operation of CMOS Integrated Circuits."

2. Operating

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must

not cause $V_{DD} - V_{SS}$ to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS} .

Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS} , whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} , or V_{SS} may damage CMOS devices by exceeding the maximum device dissipation.

ORDERING INFORMATION

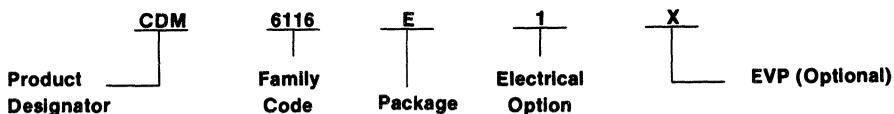
The RCA-CDM6116 family packages, and electrical options are identified by suffix letters indicated in the following chart. When ordering a Memory/Microprocessor device, it is important that the appropriate suffix letter be affixed to the type number of the device.

Package/Option	Suffix Letter *
Dual-in-Line Side Brazed Ceramic	D
Dual-in-Line Plastic	E
Chip (When applicable)	H

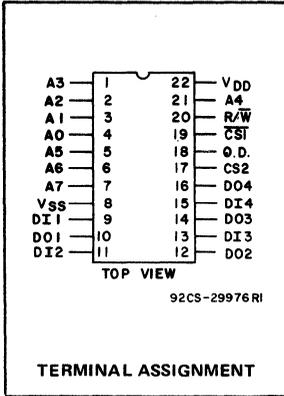
Package/Option	Suffix Letter *
----------------	-----------------

EVP Screening (Extra Value Program)
 i.e. Burn-In — optional for D, E package types X
 Electrical Option (0° to 70°C Temperature Range) 1 or 2
 For example, a CDM6116 with electrical option 1, and in a dual-in-line plastic package will be identified as the CDM6116E1. A CDM6116E1 with EVP screening option will be identified as the CDM6116E1X.

*** Nomenclature Guide**



MWS5101DL2, MWS5101DL3, MWS5101EL2, MWS5101EL3



256-Word by 4-Bit LSI Static Random-Access Memory

Features:

- Industry standard pinout
- Very low operating current — 8 mA at $V_{DD} = 5\text{ V}$ and cycle time = $1\ \mu\text{s}$
- Two Chip-Select inputs — simple memory expansion
- Memory retention for standby battery voltage of 2 V min.
- Output-Disable for common I/O systems
- 3-State data output for bus-oriented systems
- Separate data inputs and outputs

The RCA-MWS5101 is a 256-word by 4-bit static random-access memory designed for use in memory systems where high speed, very low operating current, and simplicity in use are desirable. It has separate data inputs and outputs and utilizes a single power supply of 4 to 6.5 volts.

Two Chip-Select inputs are provided to simplify system expansion. An Output Disable control provides Wire-OR capability and is also useful in common Input/Output systems. The Output Disable input allows these RAMs to be used in common data Input/Output systems by forcing the output into a high-impedance state during a write operation independent of the Chip-Select input condition. The output assumes a high-impedance

state when the Output Disable is at high level or when the chip is deselected by $\overline{CS1}$ and/or $\overline{CS2}$.

The high noise immunity of the CMOS technology is preserved in this design. For TTL interfacing at 5-V operation, excellent system noise margin is preserved by using an external pull-up resistor at each input.

For applications requiring wider temperature and operating voltage ranges, the mechanically and functionally equivalent static RAM, RCA-CDP1822, may be used.

The MWS5101 types are supplied in 22-lead hermetic dual-in-line side-brazed ceramic packages (D suffix), in 22-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

OPERATIONAL MODES

MODE	INPUTS				OUTPUT
	Chip Select 1 $\overline{CS1}$	Chip Select 2 $CS2$	Output Disable OD	Read/Write $\overline{R/W}$	
READ	0	1	0	1	Read
WRITE	0	1	0	0	Data In
WRITE	0	1	1	0	High Impedance
STANDBY	1	X	X	X	High Impedance
STANDBY	X	0	X	X	High Impedance
OUTPUT DISABLE	X	X	1	X	High Impedance

Logic 1 = High

Logic 0 = Low

X = Don't Care

MWS5101DL2, MWS5101DL3, MWS5101EL2, MWS5101EL3

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE (V_{DD}) -0.5 to -7 V
 (All voltage referenced to V_{SS} terminal)

INPUT VOLTAGE RANGE, ALL INPUTS -0.5 to $V_{DD} + 0.5$ V

DC INPUT CURRENT, ANY ONE INPUT ± 10 mA

POWER DISSIPATION PER PACKAGE (P_D):

For $T_A = -40$ to $+60^\circ\text{C}$ (PACKAGE TYPE E) 500 mW

For $T_A = +60$ to $+85^\circ\text{C}$ (PACKAGE TYPE E) Derate Linearly at 12 mW/ $^\circ\text{C}$ to 200 mW

For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE D) 500 mW

For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE D) Derate Linearly at 12 mW/ $^\circ\text{C}$ to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR $T_A =$ FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100 mW

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPE D -55 to $+125^\circ\text{C}$

PACKAGE TYPE E -40 to $+85^\circ\text{C}$

STORAGE TEMPERATURE RANGE (T_{stg}) -65 to $+150^\circ\text{C}$

LEAD TEMPERATURE (DURING SOLDERING):

At distance $1/16 \pm 1/32$ inch (1.59 ± 0.79 mm) from case for 10 s max. $+265^\circ\text{C}$

OPERATING CONDITIONS at $T_A =$ Full Package-Temperature Range
 For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	ALL TYPES		
	Min.	Max.	
DC Operating-Voltage Range	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	

STATIC ELECTRICAL CHARACTERISTICS at $T_A = 0$ to 70°C , $V_{DD} = 5 \text{ V} \pm 5\%$.

CHARACTERISTIC	TEST CONDITIONS		LIMITS			UNITS	
	V_O (V)	V_{IN} (V)	MWS5101D MWS5101E				
			Min.	Typ.*	Max.		
Quiescent Device Current, I_{DD}	L2 Types	—	0.5	—	25	50	μA
	L3 Types	—	0.5	—	100	200	
Output Voltage:	Low-Level, V_{OL}	—	0.5	—	0	0.1	V
	High-Level, V_{OH}	—	0.5	4.9	5	—	
Input Low Voltage, V_{IL}	—	—	—	—	—	1.5	
Input High Voltage, V_{IH}	—	—	3.5	—	—	—	
Output Low (Sink) Current, I_{OL}	0.4	0.5	2	4	—	—	mA
Output High (Source) Current, I_{OH}	4.6	0.5	-1	-2	—	—	
Input Current, I_{IN}	—	0.5	—	—	—	± 5	
3-State Output Leakage Current,* I_{OUT}	L2 Types	0.5	0.5	—	—	± 5	μA
	L3 Types	0.5	0.5	—	—	± 5	
Operating Current, I_{DD1} #	—	0.5	—	4	8	—	mA
Input Capacitance, C_{IN}	—	—	—	5	7.5	—	pF
Output Capacitance, C_{OUT}	—	—	—	10	15	—	

* Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .

▲ All inputs in parallel.

* All outputs in parallel.

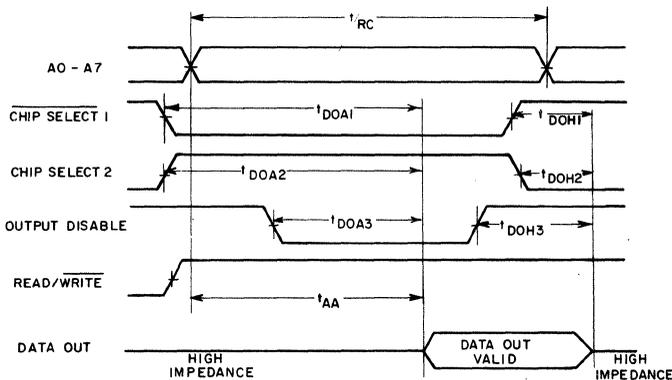
Outputs open-circuited; cycle time=1 μs .

MWS5101DL2, MWS5101DL3, MWS5101EL2, MWS5101EL3

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 0$ to 70°C , $V_{DD} = 5\text{ V} \pm 5\%$,
 $t_r, t_f = 20\text{ ns}$, $V_{IH} = 0.7 V_{DD}$, $V_{IL} = 0.3 V_{DD}$, $C_L = 100\text{ pF}$

CHARACTERISTIC	LIMITS						U N I T S
	MWS5101D, MWS5101E						
	L2 Types			L3 Types			
	Min.†	Typ.*	Max.	Min.†	Typ.*	Max.	
Read Cycle Times (Fig. 1)							
Read Cycle	t_{RC}	250	—	—	350	—	—
Access from Address	t_{AA}	—	150	250	—	200	350
Output Valid from Chip-Select 1	t_{DOA1}	—	150	250	—	200	350
Output Valid from Chip-Select 2	t_{DOA2}	—	150	250	—	200	350
Output Active from Output Disable	t_{DOA3}	—	—	110	—	—	150
Output Hold from Chip-Select 1	t_{DOH1}	20	—	—	20	—	—
Output Hold from Chip-Select 2	t_{DOH2}	20	—	—	20	—	—
Output Hold from Output Disable	t_{DOH3}	20	—	—	20	—	—

- † Time required by a limit device to allow for the indicated function.
- * Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .



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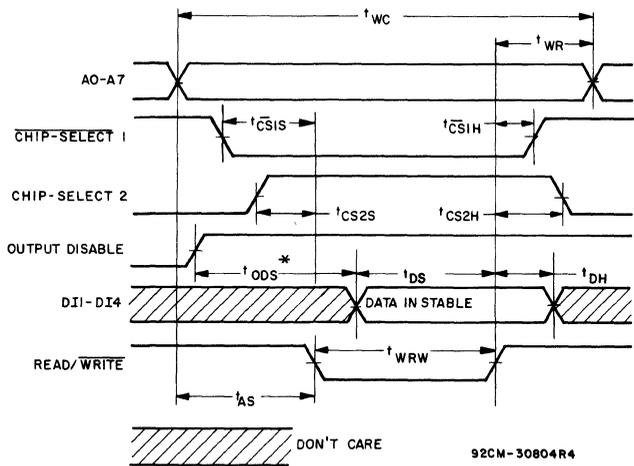
Fig. 1 - Read cycle timing waveforms.

MWS5101DL2, MWS5101DL3, MWS5101EL2, MWS5101EL3

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 0$ to 70°C , $V_{DD} = 5\text{ V} \pm 5\%$,
 $t_r, t_f = 20\text{ ns}$, $V_{IH} = 0.7 V_{DD}$, $V_{IL} = 0.3 V_{DD}$, $C_L = 100\text{ pF}$

CHARACTERISTIC	LIMITS						UNITS	
	MWS5101D, MWS5101E							
	L2 Types			L3 Types				
	Min. [†]	Typ. [●]	Max.	Min. [†]	Typ. [●]	Max.		
Write Cycle Times (Fig. 2)								
Write Cycle	t_{WC}	300	—	—	400	—	—	ns
Address Setup	t_{AS}	110	—	—	150	—	—	
Write Recovery	t_{WR}	40	—	—	50	—	—	
Write Width	t_{WRW}	150	—	—	200	—	—	
Input Data Setup Time	t_{DS}	150	—	—	200	—	—	
Data In Hold	t_{DH}	40	—	—	50	—	—	
Chip-Select 1 Setup	t_{CS1S}	110	—	—	150	—	—	
Chip-Select 2 Setup	t_{CS2S}	110	—	—	150	—	—	
Chip-Select 1 Hold	t_{CS1H}	0	—	—	0	—	—	
Chip-Select 2 Hold	t_{CS2H}	0	—	—	0	—	—	
Output Disable Setup	t_{ODS}	110	—	—	150	—	—	

[†] Time required by a limit device to allow for the indicated function.
[●] Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .



* t_{ODS} IS REQUIRED FOR COMMON I/O OPERATION ONLY; FOR SEPARATE I/O OPERATIONS, OUTPUT DISABLE IS 'DON'T CARE'.

Fig. 2 - Write cycle timing waveforms.

MWS5101DL2, MWS5101DL3, MWS5101EL2, MWS5101EL3

DATA RETENTION CHARACTERISTICS at $T_A = 0$ to 70°C ; See Fig. 3

CHARACTERISTIC	TEST CONDITIONS		LIMITS			UNITS
	VDR (V)	VDD (V)	All Types			
			Min.	Typ.*	Max.	
Minimum Data Retention Voltage, VDR	—	—	—	1.5	2	V
Data Retention Quiescent Current, IDD	L2 Types	—	—	2	10	μA
	L3 Types		—	5	50	
Chip Deselect to Data Retention Time, tCDR	—	5	600	—	—	ns
Recovery to Normal Operation Time, tRC	—	5	600	—	—	
VDD to VDR Rise and Fall Time, tr,tf	2	5	1	—	—	μs

* Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .

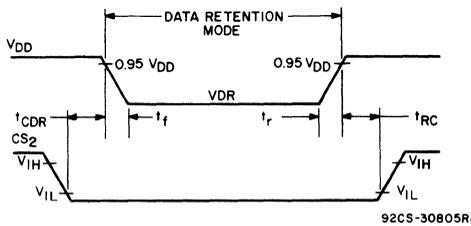


Fig. 3 - Low V_{DD} data retention timing waveforms.

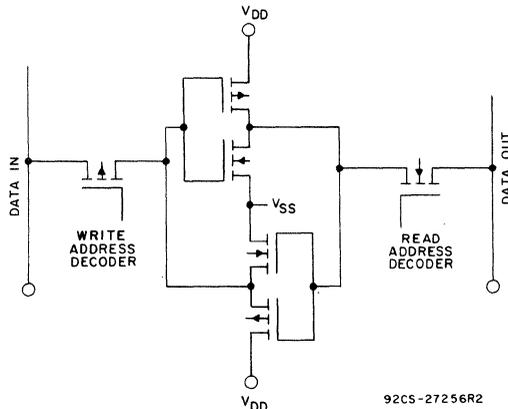


Fig. 4 - Memory cell configuration.

OPERATING AND HANDLING CONSIDERATIONS

1. Handling

All inputs and outputs of RCA COS/MOS devices have a network for electrostatic protection during handling. Recommended handling practices for COS/MOS devices are described in ICAN-6525, "Guide to Better Handling and Operation of CMOS Integrated Circuits."

2. Operating

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause V_{DD} —

V_{SS} to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS} . Input currents must not exceed 10 mA even when the power supply is off.

Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS} , whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} or V_{SS} may damage COS/MOS devices by exceeding the maximum device dissipation.

MWS5101DL2, MWS5101DL3, MWS5101EL2, MWS5101EL3

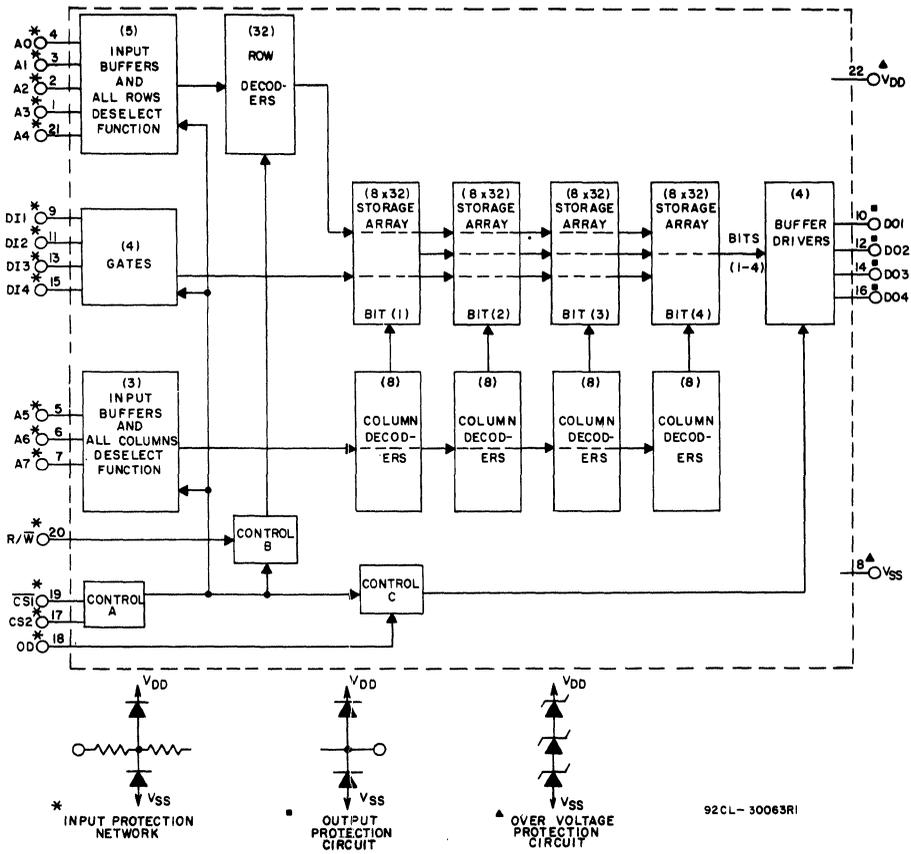


Fig. 5 - Functional block diagram for MWS5101.

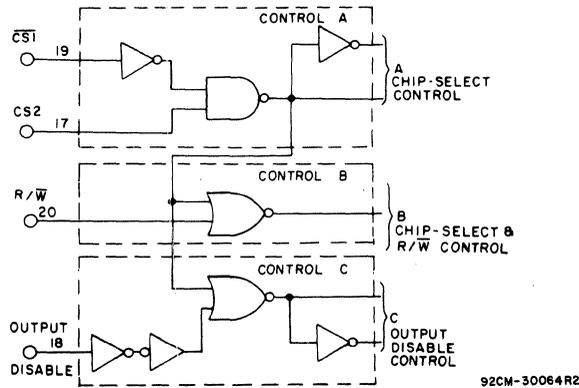


Fig. 6 - Logic diagram of controls for MWS5101.

MWS5101DL2, MWS5101DL3, MWS5101EL2, MWS5101EL3

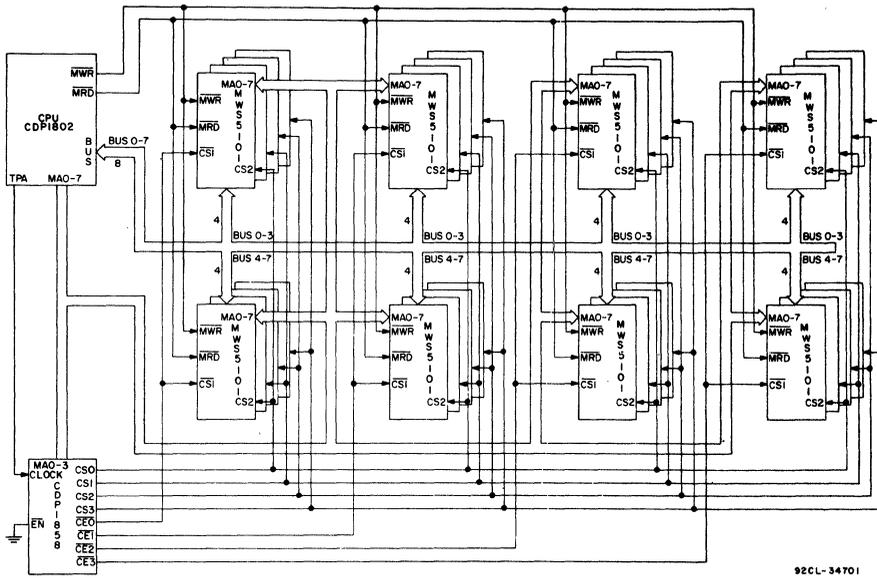
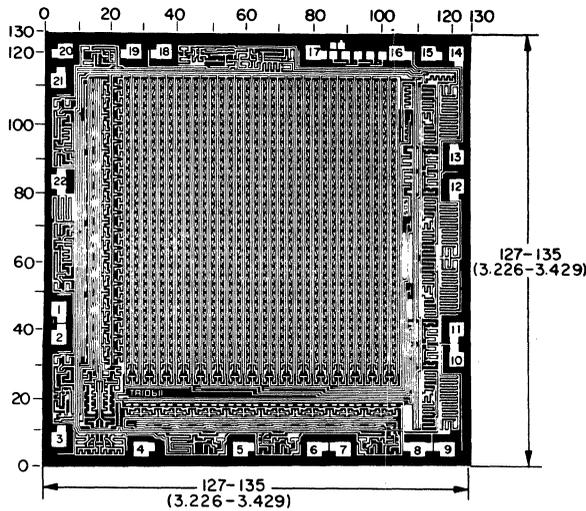


Fig. 7 - 4K byte Ram system using the CDP1858 and MWS5101.



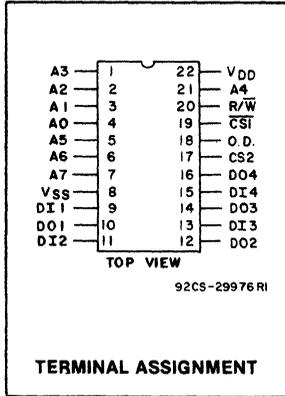
Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Dimensions and pad layout for MSW5101.

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

MWS5101ADL2, MWS5101ADL3, MWS5101AEL2, MWS5101AEL3

256-Word by 4-Bit LSI Static Random-Access Memory



Features:

- Industry standard pinout
- Low operating current - 8 mA at $V_{DD} = 5\text{ V}$ and cycle time = $1\ \mu\text{s}$
- Two Chip-Select inputs - simple memory expansion
- Memory retention for standby battery voltage of 2 V min.
- TTL compatible
- Output-Disable for common I/O systems
- 3-state data output for bus-oriented systems
- Separate data inputs and outputs

The RCA-MWS5101A is a 256-word by 4-bit static random-access memory designed for use in memory systems where high speed, very low operating current, and simplicity in use are desirable. It has separate data inputs and outputs and utilizes a single power supply of 4 to 6.5 volts.

Two Chip-Select inputs are provided to simplify system expansion. An Output Disable control provides Wire-OR capability and is also useful in common Input/Output systems. The Output Disable input allows these RAM's to be used in common data Input/Output systems by forcing the output into a high-

impedance state during a write operation independent of the Chip-Select input condition. The output assumes a high-impedance state when the Output Disable is at high level or when the chip is deselected by CS1 and/or CS2.

For applications requiring CMOS compatibility over wider operating voltage and temperature ranges, the mechanical and functional equivalent RCA-CDP1822 static RAM may be used.

The MWS5101A types are supplied in 22-lead hermetic dual-in-line side-brazed ceramic packages (D suffix), in 22-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

OPERATIONAL MODES

MODE	INPUTS				OUTPUT
	Chip Select 1 CS1	Chip Select 2 CS2	Output Disable OD	Read/Write R/W	
READ	0	1	0	1	Read
WRITE	0	1	0	0	Data In
WRITE	0	1	1	0	High Impedance
STANDBY	1	X	X	X	High Impedance
STANDBY	X	0	X	X	High Impedance
OUTPUT DISABLE	X	X	1	X	High Impedance

Logic 1 = High

Logic 0 = Low

X = Don't Care

MWS5101ADL2, MWS5101ADL3, MWS5101AEL2, MWS5101AEL3

OPERATING CONDITIONS at T_A = Full Package-Temperature Range
 For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	ALL TYPES		
	Min.	Max.	
DC Operating-Voltage Range	4	6.5	V
Input Voltage Range	V _{SS}	V _{DD}	

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE (V_{DD})

(All voltage referenced to V_{SS} terminal) -0.5 to -7 V
 INPUT VOLTAGE RANGE, ALL INPUTS -0.5 to V_{DD} + 0.5 V
 DC INPUT CURRENT, ANY ONE INPUT ± 10 mA

POWER DISSIPATION PER PACKAGE (P_D):

For T_A = -40 to +60°C (PACKAGE TYPE E) 500 mW
 For T_A = +60 to +85°C (PACKAGE TYPE E) Derate Linearly at 12 mW/°C to 200 mW
 For T_A = -55 to +100°C (PACKAGE TYPE D) 500 mW
 For T_A = +100 to +125°C (PACKAGE TYPE D) Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100 mW
 OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPE D -55 to +125°C
 PACKAGE TYPE E -40 to +85°C

STORAGE TEMPERATURE RANGE (T_{stg}) -65 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. +265°C

STATIC ELECTRICAL CHARACTERISTICS at T_A = 0 to 70°C, V_{DD} = 5 V

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS		
		MWS5101AD					
		MWS5101AE					
	V _O (V)	V _{IN} (V)	Min.	Typ.*	Max.		
Quiescent Device Current, I _{DD}	L2 Types	—	0, 5	—	25	50	μA
	L3 Types	—	0, 5	—	100	200	
Output Voltage:	Low-Level, V _{OL}	—	0, 5	—	0	0.1	V
	High-Level, V _{OH}	—	0, 5	4.9	5	—	
Input Low Voltage, V _{IL}	—	—	—	—	—	0.65	mV
Input High Voltage, V _{IH}	—	—	—	2.2	—	—	
Output Low (Sink) Current, I _{OL}	0.4	0, 5	2	4	—	mA	
Output High (Source) Current, I _{OH}	4.6	0, 5	-1	-2	—		
Input Current, I _{IN} ▲	—	0, 5	—	—	±5	μA	
3-State Output Leakage Current,* I _{OUT}	L2 Types	0, 5	0, 5	—	—		±5
	L3 Types	0, 5	0, 5	—	—	±5	
Operating Current, I _{DD1} #	—	0, 5	—	4	8	mA	
Input Capacitance, C _{IN}	—	—	—	5	7.5		
Output Capacitance, C _{OUT}	—	—	—	10	15	pF	

*Typical values are for T_A = 25°C and nominal V_{DD}.

▲All inputs in parallel.

*All outputs in parallel.

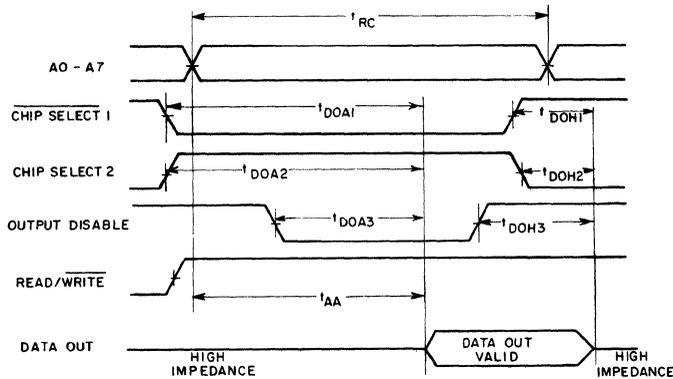
#Outputs open-circuited; cycle time = 1 μs.

MWS5101ADL2, MWS5101ADL3, MWS5101AEL2, MWS5101AEL3

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 0$ to 70°C , $V_{DD} = 5\text{ V} \pm 5\%$,
 $t_r, t_f = 20\text{ ns}$, $C_L = 50\text{ pF}$ and 1 TTL Load

CHARACTERISTIC	LIMITS						UNITS
	MWS5101AD, MWS5101AE						
	L2 Types			L3 Types			
	Min.†	Typ.*	Max.	Min.†	Typ.*	Max.	
Read Cycle Times (Fig. 1)							
Read Cycle	t_{RC}	250	—	—	350	—	—
Access from Address	t_{AA}	—	150	250	—	200	350
Output Valid from Chip-Select 1	t_{DOA1}	—	150	250	—	200	350
Output Valid from Chip-Select 2	t_{DOA2}	—	150	250	—	200	350
Output Active from Output Disable	t_{DOA3}	—	—	110	—	—	150
Output Hold from Chip-Select 1	t_{DOH1}	20	—	—	20	—	—
Output Hold from Chip-Select 2	t_{DOH2}	20	—	—	20	—	—
Output Hold from Output Disable	t_{DOH3}	20	—	—	20	—	—

†Time required by a limit device to allow for the indicated function.
 *Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .



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Fig. 1 - Read cycle timing waveforms.

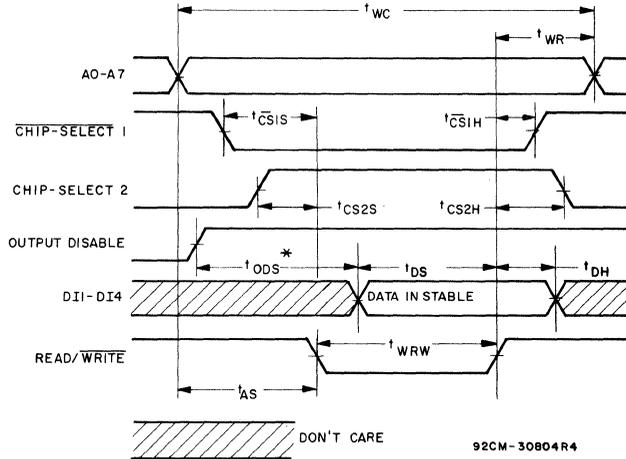
MWS5101ADL2, MWS5101ADL3, MWS5101AEL2, MWS5101AEL3

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 0$ to 70°C , $V_{DD} = 5\text{V} \pm 5\%$,
 $t_r, t_f = 20\text{ ns}$, $C_L = 50\text{ pF}$ and 1 TTL Load

CHARACTERISTIC	LIMITS						UNITS	
	MWS5101AD, MWS5101AE							
	L2 Types			L3 Types				
	Min.†	Typ.*	Max.	Min.†	Typ.*	Max.		
Write Cycle Times (Fig. 2)								
Write Cycle	t _{WC}	300	—	—	400	—	—	ns
Address Setup	t _{AS}	110	—	—	150	—	—	
Write Recovery	t _{WR}	40	—	—	50	—	—	
Write Width	t _{WRW}	150	—	—	200	—	—	
Input Data Setup Time	t _{DS}	150	—	—	200	—	—	
Data In Hold	t _{DH}	40	—	—	50	—	—	
Chip-Select 1 Setup	t _{CS1S}	110	—	—	150	—	—	
Chip-Select 2 Setup	t _{CS2S}	110	—	—	150	—	—	
Chip-Select 1 Hold	t _{CS1H}	0	—	—	0	—	—	
Chip-Select 2 Hold	t _{CS2H}	0	—	—	0	—	—	
Output Disable Setup	t _{ODS}	110	—	—	150	—	—	

†Time required by a limit device to allow for the indicated function.

*Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .



* t_{ODS} IS REQUIRED FOR COMMON I/O OPERATION ONLY. FOR SEPARATE I/O OPERATIONS, OUTPUT DISABLE IS DON'T CARE.

Fig. 2 - Write cycle timing waveforms.

MWS5101ADL2, MWS5101ADL3, MWS5101AEL2, MWS5101AEL3

DATA RETENTION CHARACTERISTICS at $T_A = 0$ to 70°C ; See Fig. 3.

CHARACTERISTIC	TEST CONDITIONS		LIMITS			UNITS
	VDR (V)	VDD (V)	All Types			
			Min.	Typ.*	Max.	
Minimum Data Retention Voltage, VDR	—	—	—	1.5	2	V
Data Retention Quiescent Current, IDD	L2 Types	—	—	2	10	μA
	L3 Types	—	—	5	50	
Chip Deselect to Data Retention Time, tCDR	—	5	600	—	—	ns
Recovery to Normal Operation Time, tRC	—	5	600	—	—	
VDD to VDR Rise and Fall Time, tr,tf	2	5	1	—	—	μs

*Typical values are for $T_A = 25^\circ\text{C}$.

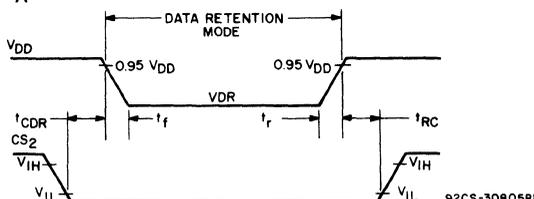


Fig. 3 - Low V_{DD} data retention timing waveforms.

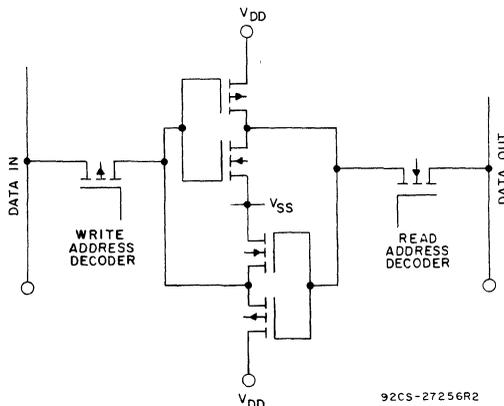


Fig. 4 - Memory cell configuration.

OPERATING AND HANDLING CONSIDERATIONS

1. Handling

All inputs and outputs of RCA COS/MOS devices have a network for electrostatic protection during handling. Recommended handling practices for COS/MOS devices are described in ICAN-6525, "Guide to Better Handling and Operation of CMOS Integrated Circuits."

2. Operating

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause $V_{DD} - V_{SS}$ to

exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS} . Input currents must not exceed 10 mA even when the power supply is off.

Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS} , whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} or V_{SS} may damage COS/MOS devices by exceeding the maximum device dissipation.

MWS5101ADL2, MWS5101ADL3, MWS5101AEL2, MWS5101AEL3

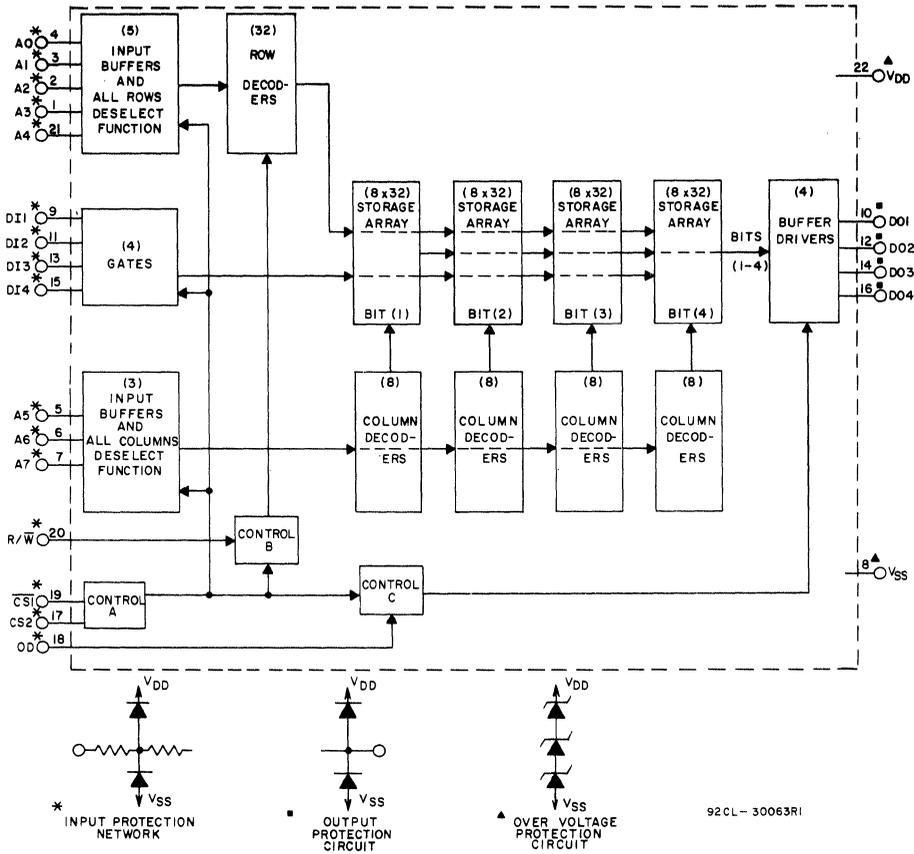


Fig. 5 - Functional block diagram for MWS5101A.

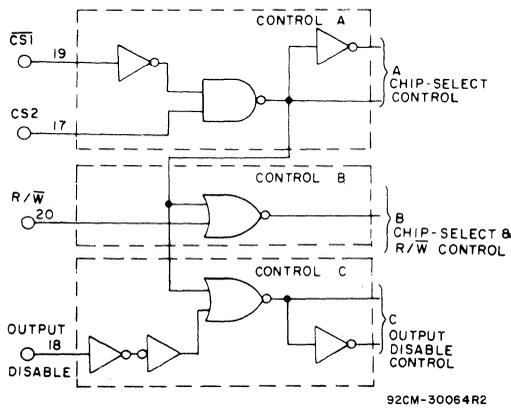
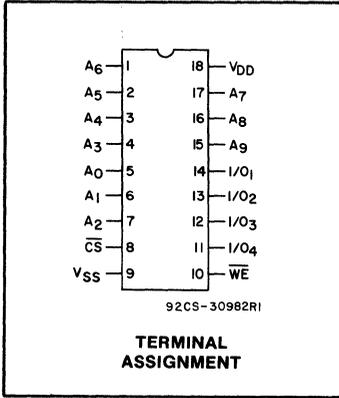


Fig. 6 - Logic diagram of controls for MWS5101A.

CMOS 1024-Word by 4-Bit LSI Static RAM

Features:

- Fully static operation
- Industry standard 1024 x 4 pinout (same as pinouts for 6514, 2114, 9114, and 4045 types)
- Common data input and output
- Memory retention for stand-by battery voltage as low as 2 V min.
- All inputs and outputs directly TTL compatible
- 3-state outputs
- Low standby and operating power



The RCA-MWS5114 is a 1024-word by 4-bit static random-access memory that uses the RCA ion-implanted silicon gate complementary MOS (CMOS) technology. It is designed for use in memory systems where low power and simplicity in use are desirable. This type has common data

input and data output and utilizes a single power supply of 4.5 V to 6.5 V.

The MWS5114 is supplied in 18-lead, hermetic, dual-in-line side-brazed ceramic packages (D suffix) and in 18-lead dual-in-line plastic packages (E suffix).

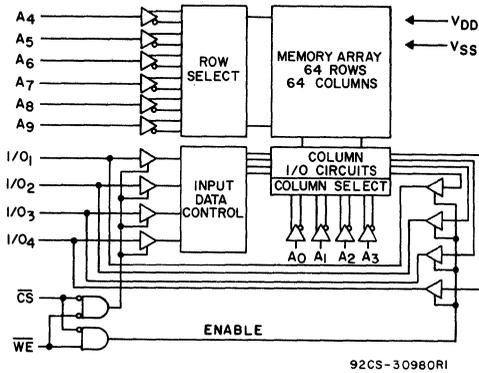


Fig. 1 — Functional block diagram for MWS5114

OPERATIONAL MODES			
FUNCTION	\overline{CS}	\overline{WE}	DATA PINS
Read	0	1	Output: Dependent on data
Write	0	0	Input
Not Selected	1	X	High-Impedance

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY VOLTAGE RANGE, (V _{DD})	-0.5 to +7 V
(Voltages referenced to V _{SS} Terminal)	
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to V _{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P _D):	
For T _A = -40 to +60° C (PACKAGE TYPE E)	500 mW
For T _A = +60 to +85° C (PACKAGE TYPE E)	Derate Linearly at 12 mW/° C to 200mW
For T _A = -55 to +100° C (PACKAGE TYPE D)	500 mW
For T _A = +100 to +125° C (PACKAGE TYPE D)	Derate Linearly at 12 mW/° C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T _A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T _A):	
PACKAGE TYPE D	-55 to +125° C
PACKAGE TYPE E	-40 to +85° C
STORAGE TEMPERATURE RANGE (T _{stg})	-65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265° C

OPERATING CONDITIONS at T_A = -40° C to +85° C

For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
DC Operating-Voltage Range	4.5	6.5	V
Input Voltage Range	V _{SS}	V _{DD}	

STATIC ELECTRICAL CHARACTERISTICS at T_A = 0 to +70° C, V_{DD} ±5%, Except as noted

CHARACTERISTIC	CONDITIONS			LIMITS									UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)	MWS 5114-3			MWS 5114-2			MWS 5114-1			
				MIN.	TYP.*	MAX.	MIN.	TYP.*	MAX.	MIN.	TYP.*	MAX.	
Quiescent Device Current I _{DD} Max.	—	0.5	5	—	75	100	—	75	100	—	75	250	μA
Output Voltage Low Level V _{OL} Max. High Level V _{OH} Min.	—	0.5	5	—	0	0.1	—	0	0.1	—	0	0.1	V
Input Voltage Low Level V _{IL} Max. High Level V _{IH} Min.	0.5,4.5	—	5	—	1.2	0.8	—	1.2	0.8	—	1.2	0.8	
Output Current (Sink) I _{OL} Min. (Source) I _{OH} Max.	0.4	0.5	5	2	4	—	2	4	—	2	4	—	mA
Input Current I _{IN} Max. ^Δ	—	0.5	5	—	±0.1	±5	—	±0.1	±5	—	±0.1	±5	μA
3-State Output Leakage Current I _{OUT} *	0.5	0.5	5	—	±0.5	±5	—	±0.5	±5	—	±0.5	±5	
Operating Device Current I _{DD1} #	—	0.5	5	—	4	8	—	4	8	—	4	8	mA
Input Capacitance C _{IN}	—	—	—	—	5	7.5	—	5	7.5	—	5	7.5	pF
Output Capacitance C _{OUT}	—	—	—	—	10	15	—	10	15	—	10	15	

*Typical values are for T_A = 25° C and nominal V_{DD}.
 ΔAll inputs in parallel.

#Outputs open circuited; cycle time = 1 μs.
 * All outputs in parallel.

RCA CMOS LSI Products

MWS5114-1, MWS5114-2, MWS5114-3

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 0$ to $+70^\circ\text{C}$, $V_{DD} = 5\text{V} \pm 5\%$,
 Input $t_r, t_f = 10\text{ ns}$; $C_L = 50\text{ pF}$ and 1 TTL Load

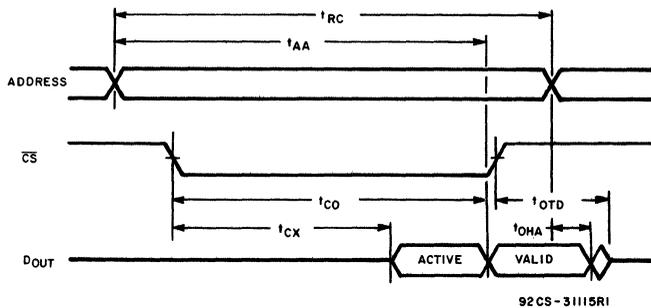
CHARACTERISTIC	LIMITS									UNITS
	MWS 5114-3			MWS 5114-2			MWS 5114-1			
	MIN.†	TYP.*	MAX.	MIN.†	TYP.*	MAX.	MIN.†	TYP.*	MAX.	

Read Cycle Times See Fig. 2

Read Cycle	t_{RC}	200	160	—	250	200	—	300	250	—	ns
Access	t_{AA}	—	160	200	—	200	250	—	250	300	
Chip Selection to Output Valid	t_{CO}	—	110	150	—	150	200	—	200	250	
Chip Selection to Output Active	t_{CX}	20	100	—	20	100	—	20	100	—	
Output 3-state from Deselection	t_{OTD}	—	75	125	—	75	125	—	75	125	
Output Hold from Address Change	t_{OHA}	50	100	—	50	100	—	50	100	—	

† Time required by a limit device to allow for the indicated function.

* Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .



NOTE:
 \overline{WE} IS HIGH DURING THE READ CYCLE.
 TIMING MEASUREMENT REF. LEVEL IS 1.5V

Fig. 2 — Read cycle waveforms.

MWS5114-1, MWS5114-2, MWS5114-3

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 0$ to $+70^\circ\text{C}$, $V_{DD} = 5V \pm 5\%$,
 Input $t_r, t_f = 10\text{ ns}$; $C_L = 50\text{ pF}$ and 1 TTL Load

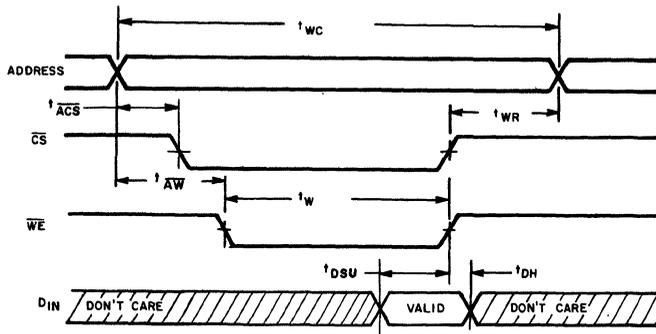
CHARACTERISTIC	LIMITS									UNITS
	MWS 5114-3			MWS 5114-2			MWS 5114-1			
	MIN.†	TYP.*	MAX.	MIN.†	TYP.*	MAX.	MIN.†	TYP.*	MAX.	

Write Cycle Times See Fig. 3

Write Cycle	t_{WC}	200	160	—	250	200	—	300	220	—	ns
Write	t_W	125	100	—	150	120	—	200	140	—	
Write Release	t_{WR}	50	40	—	50	40	—	50	40	—	
Address To Chip Select Set-up Time	t_{ACS}	0	0	—	0	0	—	0	0	—	
Address To Write Set-up Time	t_{AW}	25	20	—	50	40	—	50	40	—	
Data to Write Set-up Time	t_{DSU}	75	50	—	75	50	—	75	50	—	
Data Hold From Write	t_{DH}	30	10	—	30	10	—	30	10	—	

† Time required by a limit device to allow for the indicated function.

*Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .



NOTE: \overline{WE} IS LOW DURING THE WRITE CYCLE
 TIMING MEASUREMENT REF. LEVEL IS 1.5 V

Fig. 3 — Write cycle waveforms.

RCA CMOS LSI Products

MWS5114-1, MWS5114-2, MWS5114-3

DATA RETENTION CHARACTERISTICS at $T_A = 0$ to 70°C ; See Fig. 4.

CHARACTERISTIC		TEST CONDITIONS		LIMITS			UNITS
		V_{DR} (V)	V_{DD} (V)	ALL TYPES			
				MIN.	TYP.*	MAX.	
Minimum Data Retention Voltage	V_{DR}	—	—	2	—	—	V
Data Retention Quiescent Current, I_{DD}	MWS 5114-3	2	—	—	25	50	μA
	MWS 5114-2		—	—	25	50	
	MWS 5114-1		—	—	60	125	
Chip Deselect to Data Retention Time,	t_{CDR}	—	5	300	—	—	ns
Recovery to Normal Operation Time,	t_{RC}	—	5	300	—	—	
V_{DD} to V_{DR} Rise and Fall Time	t_r, t_f	2	5	1	—	—	μs

*Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .

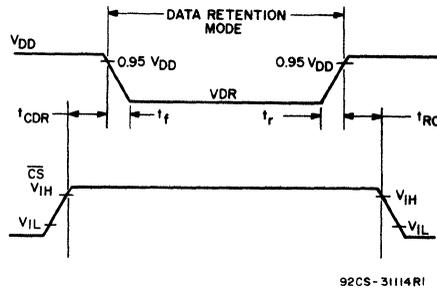


Fig. 4 — Low V_{DD} data retention timing waveforms.

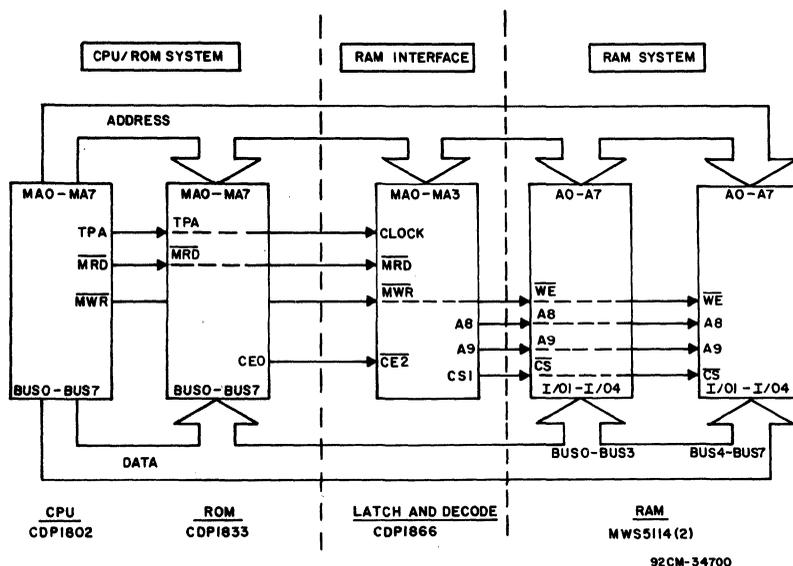


Fig. 5 - MWS5114 (1K x 4) minimum system (1K x 8).

OPERATING AND HANDLING CONSIDERATIONS

1. Handling

All inputs and outputs of RCA CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in ICAN-6525, "Guide to Better Handling and Operation of CMOS Integrated Circuits."

2. Operating

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause $V_{DD} - V_{SS}$ to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS} . Input currents must not exceed 10 mA even when the power supply is off.

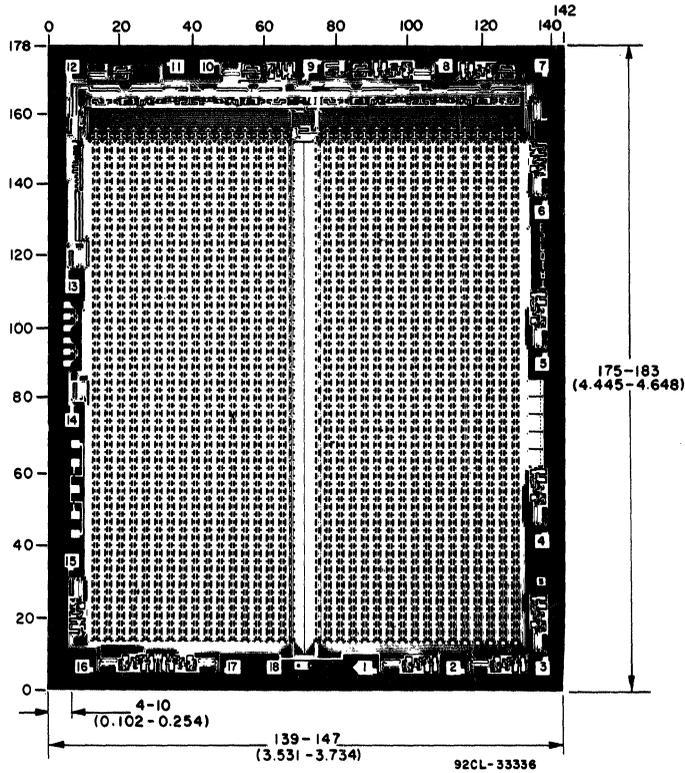
Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS} , whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} or V_{SS} may damage CMOS devices by exceeding the maximum device dissipation.

MWS5114-1, MWS5114-2, MWS5114-3



Dimensions and pad layout for MWS5114H

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

ORDERING INFORMATION

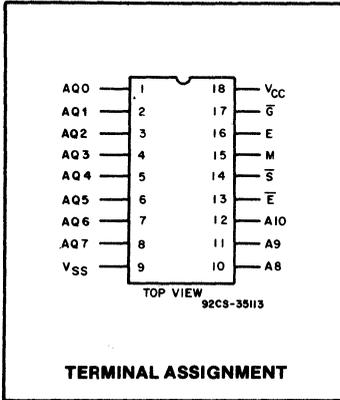
RCA Memory device packages are identified by letters indicated in the following chart. When ordering a Memory device, it is important that the appropriate suffix letter be affixed to the type number of the device.

Package	Suffix Letter
Dual-in-Line Side-Brazed Ceramic	D
Dual-in-Line Plastic	E
Chip	H

For example, a MWS5114-3 in a dual-in-line plastic package will be identified as the MWS5114E-3.

6805-Series LSI Products Technical Data

CMOS 2048-Word x 8-Bit Static Read-Only Memory



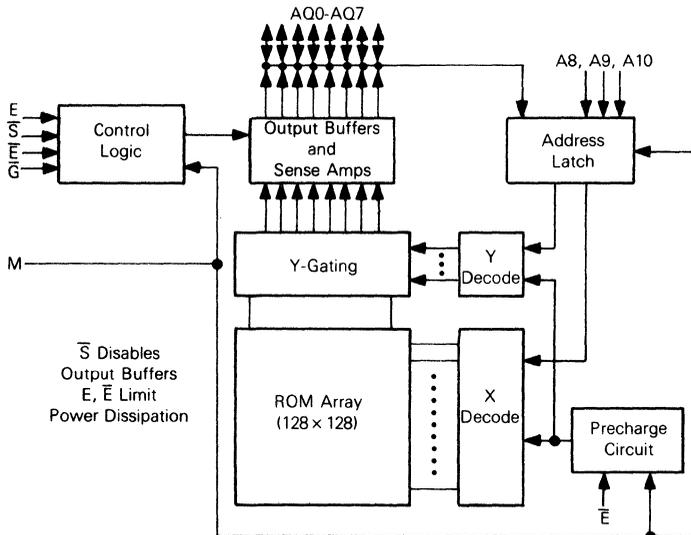
Features

- 2K x 8 CMOS ROM
- 3 to 6 volt supply
- Access time
430 ns (5 V) CDP65516-43
550 ns (5 V) CDP65516-55
- Low power dissipation
15 mA maximum (active)
30 µA maximum (standby)
- Directly compatible with muxed bus CMOS microprocessors
- Pins 13, 14, 16, and 17 are mask programmable
- MOTEL mask option also insures direct compatibility with many NMOS microprocessors
- Standard 18-pin package

The CDP65516 is a complementary MOS mask programmable byte organized read-only memory (ROM). The CDP65516 is organized as 2048 bytes of 8 bits, designed for use in multiplex bus systems. It is fabricated using silicon gate CMOS technology, which offers low-power operation from a single 5-volt supply.

The memory is compatible with CMOS microprocessors that share address and data lines. Compatibility is enhanced by pins 13, 14, 16, and 17 which give the user the versatility

of selecting the active levels of each. Pin 17 allows the user to choose active high, active low or a third option of programming which is termed the "MOTEL" mode. If this mode is selected by the user, it provides direct compatibility with the CDP6805E2 type microprocessor series. In the MOTEL operation the ROM can accept either polarity signal on the data strobe input as long as the signal toggles during the cycle. This unique operational feature makes the ROM an extremely versatile part.



PIN NAMES	
A00-A07	Address/Data Output
A8-A10	Address
M	Multiplex Address Strobe
E	Chip Enable
S	Chip Select
G	Data Strobe (Output Enable)

Fig. 1 - Block diagram.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7	V
Input Voltage	V_{in}	-0.3 to +7	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage (V_{CC} must be applied at least 100 μ s before proper device operation is achieved)	V_{CC}	4.5	5	5.5	V
Input High Voltage	V_{IH}	$V_{CC} - 2$	-	5.5	V
Input Low Voltage	V_{IL}	-0.3	-	0.8	V

RECOMMENDED OPERATING CHARACTERISTICS

Characteristic	Symbol	CDP65516-43		CDP65516-55		Unit	Test Condition
		Min	Max	Min	Max		
Output High Voltage Source Current - 1.6 mA	V_{OH}	$V_{CC} - 0.4$ V	-	$V_{CC} - 0.4$ V	-	V	
Output Low Voltage Sink Current + 1.6 mA	V_{OL}	-	0.4	-	0.4	V	
Supply Current (Operating)	I_{CC1}	-	15	-	15	mA	$C_L = 130$ pF, $V_{in} = V_{IH}$ to V_{IL} $t_{cyc} = 1$ μ s
Supply Current (DC Active)	I_{CC2}	-	100	-	100	μ A	$V_{in} = V_{CC}$ to GND
Standby Current	I_{ISB}	-	30	-	50	μ A	$V_{in} = V_{CC}$ to GND
Input Leakage	I_{in}	-10	+10	-10	+10	μ A	
Output Leakage	I_{OL}	-10	+10	-10	+10	μ A	

CAPACITANCE ($f = 1$ MHz, $T_A = 25^\circ\text{C}$, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Max	Unit
Input Capacitance	C_{in}	5	pF
Output Capacitance	C_{out}	12.5	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

READ CYCLE

$C_L = 130$ pF

Parameter	Symbol	CDP65516-43		CDP65516-55		Unit
		Min	Max	Min	Max	
Address Strobe Access Time	t_{MLDV}	-	430	-	550	ns
Read Cycle Time	t_{MHMH}	-	750	-	1000	ns
Multiplex Address Strobe High to Multiplex Address Strobe Low (Pulse Width)	t_{MHML}	150	-	175	-	ns
Data Strobe Low to Multiplex Address Strobe Low	t_{GLML}	50	-	50	-	ns
Multiplex Address Strobe Low to Data Strobe High	t_{MLGH}	100	-	160	-	ns
Address Valid to Multiplex Address Strobe Low	t_{AVML}	50	-	50	-	ns
Chip Select Low to Multiplex Address Strobe Low	t_{SLML}	50	-	50	-	ns
Multiplex Address Strobe Low to Chip Select High	t_{MLSH}	50	-	80	-	ns
Chip Enable Low/High to Multiplex Address Strobe Low	t_{ELML} t_{EHML}	50	-	50	-	ns
Multiplex Address Strobe Low to Address Don't Care	t_{MLAX}	50	-	80	-	ns
Data Strobe High to Data Valid	t_{GHDV}	175	-	200	-	ns
Data Strobe Low to High-Z	t_{GLDZ}	-	160	-	160	ns

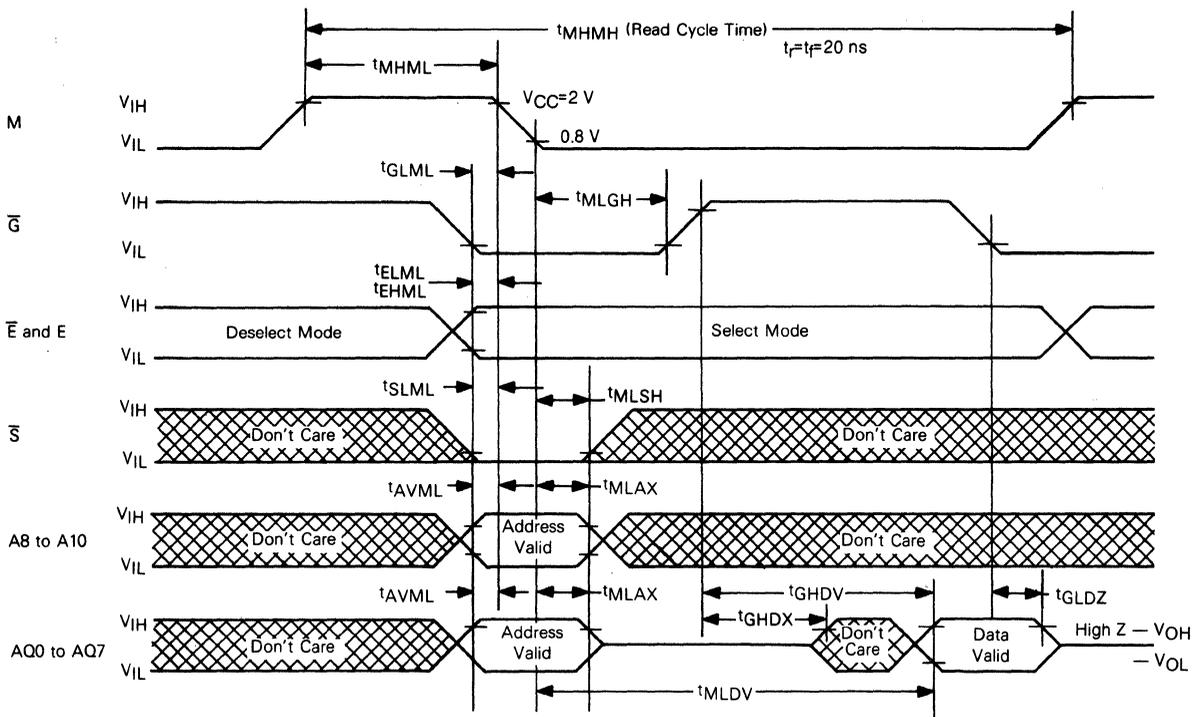


Fig. 2 - Read cycle timing waveforms.

Functional Description

The 2K x 8 bit CMOS ROM (CDP65516) shares address and data lines and, therefore, is compatible with the majority of CMOS microprocessors in the industry. The package size is reduced from 24 pins for standard NMOS ROMs to 18 pins because of the multiplexed bus approach. The savings in package size and external bus lines adds up to tighter board packing density which is handy for battery-powered hand-carried CMOS Systems. This ROM is designed with the intention of having very low active as well as standby currents. The active power dissipation of 75 mW (at $V_{CC}=5 V$, freq.=1 MHz) and standby power of 150 μW (at $V_{CC}=5 V$) add up to low power for battery operation. The typical access time of the ROM is 280 ns making it acceptable for operation with today's existing CMOS microprocessors.

An example of this operation is shown in Fig. 3. Shown is a typical connection with the CDP6805E2 CMOS microprocessor. The main difference between this system and competitive process is that the data strobe (DS) on the CDP6805E2 and the read bar (\overline{RD}) on the competitive process both control the output of data from the ROM but are of opposite polarity. The 2K x 8 ROM can accept either polarity signal on the data strobe input as long as the signal toggles during the cycle. This is termed the MOTEL mode of operation. This unique operational feature makes the ROM an extremely versatile part. Further operational features are explained in the following section.

Operational Features

In order to operate in a multiplexed bus system the ROM latches, for one cycle, the address and chip-select input information on the trailing edge of address strobe (M) so the address signals can be taken off the bus.

Since they are latched, the address and chip-select signals have a setup and hold time referenced to the negative edge of address strobe. Address strobe has a minimum pulse

width requirement since the circuit is internally precharged during this time and is set up for the next cycle on the trailing edge of address strobe. Access time is measured from the negative edge of address strobe.

The part is equipped with a data strobe input (G) which controls the output of data onto the bus lines after the addresses are off the bus. The data strobe has three potential modes of operation which are programmable with the ROM array. The first mode is termed the MOTEL mode of operation. In this mode, the circuit can work with either the 6805 or 8085 type microprocessor series. The difference between the two series for a ROM peripheral is only the polarity of the data-strobe signal. Therefore, in the MOTEL mode the ROM recognizes the state of the data-strobe signal at the trailing edge of address strobe (requires a setup and hold time), latches the state into the circuit after address strobe, and turns on the data outputs when an opposite polarity signal appears on the data-strobe input. In this manner the data-strobe input can work with either polarity signal but that signal must toggle during a cycle to output data on the bus lines. If the data strobe remains at a dc level the outputs will remain off. The data-strobe input has two other programmable modes of operation and those are the standard static select modes (high or low) where a dc input not synchronous with the address strobe will turn the output on or off.

The chip-enable and chip-select inputs are all programmable with the ROM array to either a high or low select. The chip select acts as an additional address and is latched on the address-strobe trailing edge. On deselect the chip select merely turns off the output drivers acting as an output disable. It does not power down the chip. The chip-enable inputs, however, do put the chip in a power down standby mode but they are not latched with address strobe and must be maintained in a dc state for a full cycle.

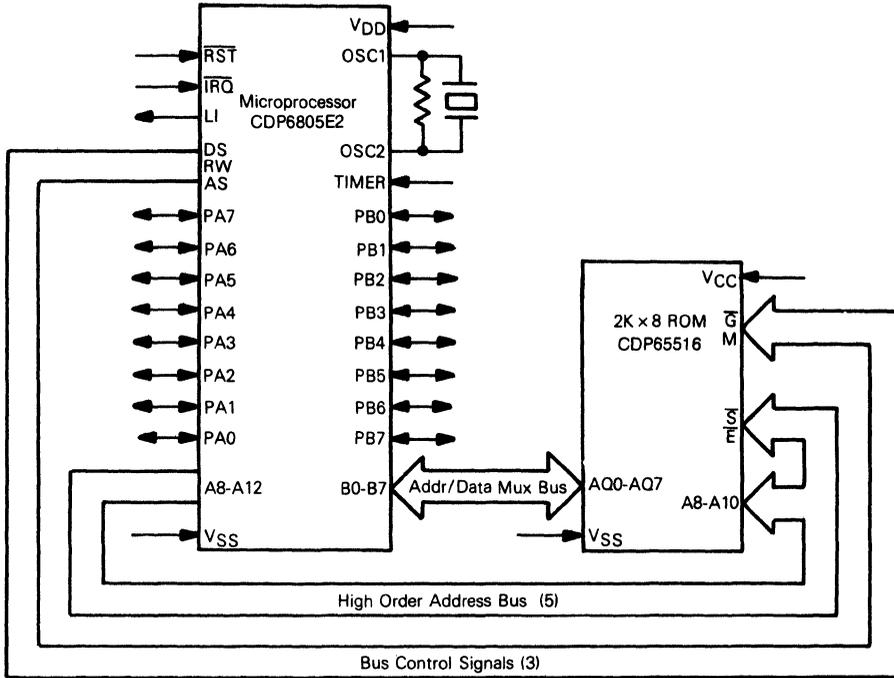
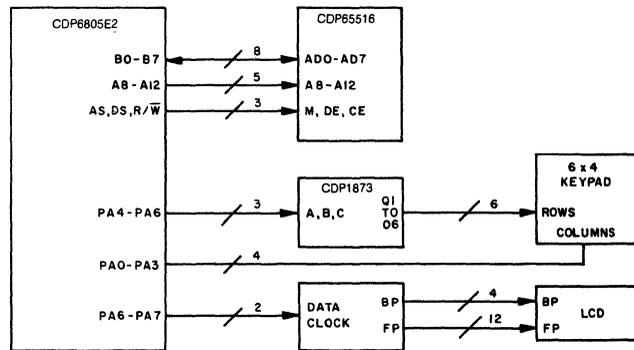


Fig. 3 - Typical minimum system.

Introduction

CBUG05 is a debug monitor program written for the CDP6805E2 Microprocessor Unit and contained in the CDP65516 2K x 8 CMOS ROM. CBUG05 allows for rapid development and evaluation of hardware and 6805 Family type software, using memory and register examine/change commands as well as breakpoint and single instruction trace commands. CBUG05 also includes software to set

and display time, using an optional CDP6818 Real-Time Clock (RTC), and routines to punch and load an optional cassette interface. Fig. 2 shows a minimum system which only requires the MPU, ROM, keypad inputs and display output interfaces. Port A of the CDP6805E2 MPU is required for the I/O; however, Port B and all other CDP6805E2 MPU features remain available to the user. A possible expanded system is shown in Fig. 3.



92CM-35118

Fig. 4 - Minimum CBUG05 system.

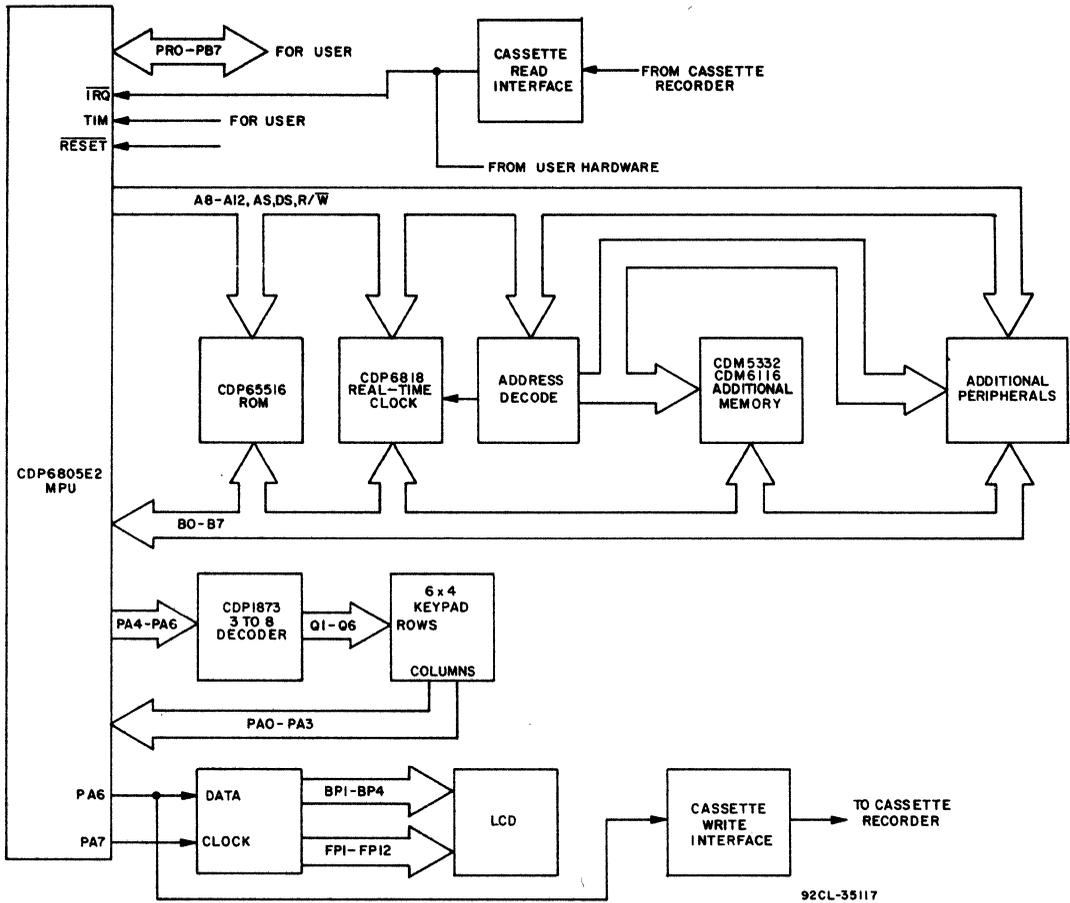


Fig. 5 - Expanded CBUG05 system.

DATA PROGRAMMING INSTRUCTIONS

When a customer submits instructions for programming RCA custom ROMs, the customer must also complete the relevant parts of the ROM information sheet and submit this sheet together with the programming instructions. Programming instructions may be submitted in any one of three ways, as follows:

1. **Computer-Card Deck**—use standard 80-column computer punch cards.
2. **Floppy Diskette**—diskette information must be generated on an RCA CDP1800-series microprocessor development system.

3. **Master Device** — a ROM, PROM, or EPROM that contains the required programming information.

The requirements for each method are explained in detail in the following paragraphs:

COMPUTER-CARD METHOD

Use standard 80-column computer cards. Each card deck must contain, in order, a title card, an option card, a data-format card, and data cards. Punch the cards as specified in the following charts:

TITLE CARD

Column No.	Data
1	Punch T
2-5	leave blank
6-30	Customer Name (start at 6)
31-34	leave blank
35-54	Customer Address or Division (start at 35)
55-58	leave blank
59-63	RCA custom selection number (5 digits) (Obtained from RCA Sales Office)
64	leave blank
65-71	RCA device type, without CDP6 prefix, e.g., 5516
72	Punch an opening parenthesis (
73	Punch 8
74	Punch a closing parenthesis)
75-78	leave blank
79-80	Punch a 2-digit decimal number to indicate the deck number; the first deck should be numbered 01

OPTION CARD

Use the ROM Information Sheet to select the polarity options, P, N, or X, for the desired ROM type.

Column No.	Data
1-6	Punch the word OPTION
7	leave blank
8-17	RCA device type, including CDP6 prefix, e.g., CDP65516
18-27	leave blank
28-31	Punch P or N per ROM Information Sheet
32-78	leave blank
79-80	Punch the deck number (the 2-digit number in columns 79-80 of the title card)

DATA-FORMAT CARD

The data-format card specifies the form in which the data is to be entered into ROM.

Column No.	Data
1-11	Punch the words DATA FORMAT
12	leave blank
13-15	Punch the letters HEX
16	leave blank
17-19	Punch POS
20-78	leave blank
79-80	Punch the deck number (the 2-digit number in columns 79-80 of the title card)

ROM INFORMATION SHEET

OPTION LIST

Select the options for your ROM from the following list. A manufacturing mask will be generated from this information. Select one in each section..

PROGRAMMABLE PIN OPTIONS

	Pin Number			
	13 (\bar{S})	14 (M)	16 (E)	17 (\bar{G})
Active High (1 or P)	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Active Low (1 or P)	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
MOTEL (X)	—	—	—	<input type="checkbox"/>
	28	29	30	31

Column Number
(On Option Card)

CUSTOMER INFORMATION

Customer Name _____

Address _____

City _____ State _____ Zip _____

Phone () _____ Extension _____

Contact Ms./Mr. _____

Customer Part No. _____

PATTERN MEDIA

 EPROM Card Deck Other*

*Other media require factory approval.

Signature _____

Title _____

OPERATING AND HANDLING CONSIDERATIONS

1. Handling

All inputs and outputs of RCA CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in ICAN-6525 "Guide to Better Handling and Operation of CMOS Integrated Circuits."

2. Operating

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause $V_{DD} - V_{SS}$ to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{CC} nor less than V_{SS} . Input currents must not exceed 10 mA even when the power supply is off.

Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{CC} or V_{SS} , whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} , V_{CC} , or V_{SS} may damage CMOS devices by exceeding the maximum device dissipation.

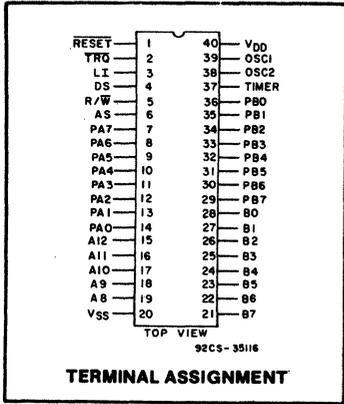
CMOS 8-Bit Microprocessor

Hardware Features

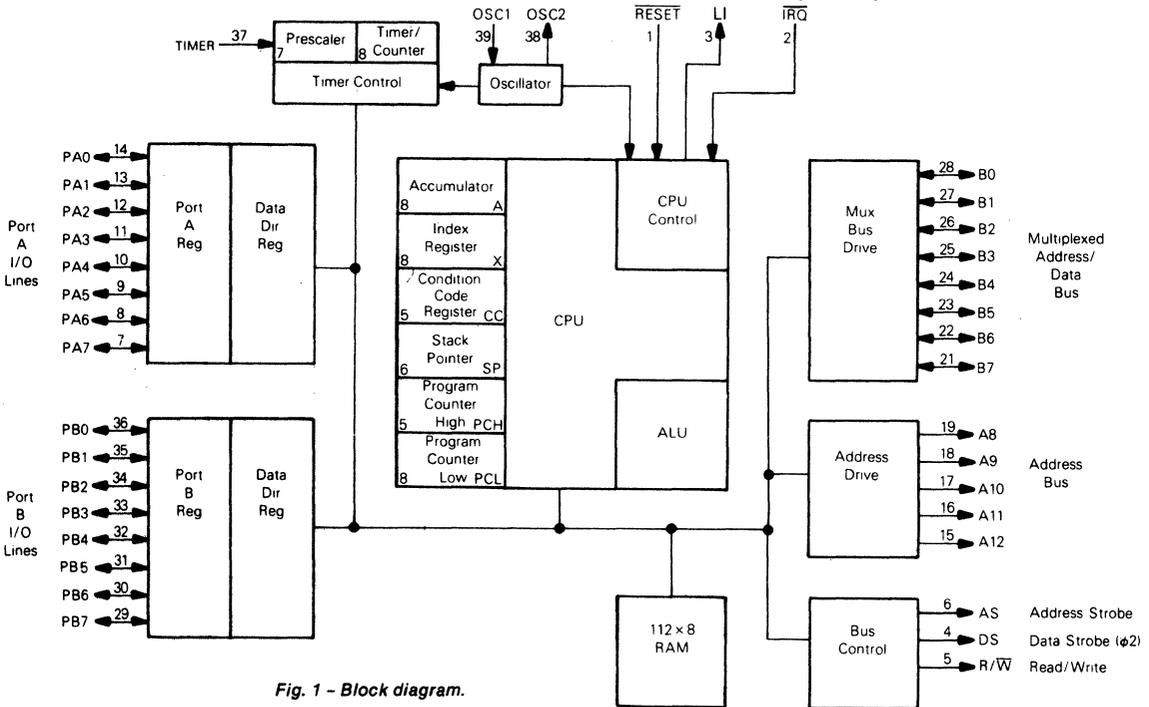
- Typical full speed operating power of 35 mW @ 5 V
- Typical WAIT mode power of 5 mW
- Typical STOP mode power of 25 μW
- 112 bytes of on-chip RAM
- 16 bidirectional I/O lines
- Internal 8-bit timer with software programmable 7-bit prescaler
- External timer input
- Full external and timer interrupts
- Multiplexed address/data bus
- Master reset and power-on reset
- Capable of addressing up to 8K bytes of external memory
- Single 3- to 6-volt supply
- On-chip oscillator
- 40-pin dual-in-line package

Software Features

- Similar to the MC6800
- Efficient use of program space
- Versatile interrupt handling
- True bit manipulation
- Addressing modes with indexed addressing for tables
- Efficient instruction set
- Memory mapped I/O
- Two power saving standby modes



The CDP6805E2 Microprocessor Unit (MPU) belongs to the CDP6805 Family of Microcomputers. This 8-bit fully static and expandable microprocessor contains a CPU, on-chip RAM, I/O, and TIMER. It is a low-power, low-cost processor designed for low-end to mid-range applications in the consumer, automotive, industrial, and communications markets where very low power consumption constitutes an important factor. The following are the major features of the CDP6805E2 MPU.



MAXIMUM RATINGS (voltages referenced to V_{SS})

Ratings	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.3 to +8.0	V
All Input Voltages Except OSC1	V_{in}	$V_{SS} - 0.5$ to $V_{DD} + 0.5$	V
Current Drain Per Pin Excluding V_{DD} and V_{SS}	I	10	mA
Operating Temperature Range CDP6805E2 CDP6805E2C	T_A	T_L to T_H 0 to 70 -40 to 85	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

DC ELECTRICAL CHARACTERISTICS 3.0 V ($V_{DD} = 3.0$ Vdc, $V_{SS} = 0$, $T_A = 0^\circ$ to 70° C, unless otherwise noted)

Characteristics	Symbol	Min	Max	Unit
Output Voltage $I_{LOAD} \leq 10.0 \mu A$	V_{OL} V_{OH}	- $V_{DD} - 0.1$	0.1 -	V
Total Supply Current ($C_L = 50$ pF — no DC loads) $t_{cyc} = 5 \mu s$				
Run ($V_{IL} = 0.2$ V, $V_{IH} = V_{DD} - 0.2$ V)	I_{DD}	-	1.3	mA
Wait (Test Conditions — See Note Below)	I_{DD}	-	200	μA
Stop (Test Conditions — See Note Below)	I_{DD}	-	100	μA
Output High Voltage				
($I_{LOAD} = 0.25$ mA) A8-A12, B0-B7	V_{OH}	2.7	-	V
($I_{LOAD} = 0.1$ mA) PA0-PA7, PB0-PB7	V_{OH}	2.7	-	V
($I_{LOAD} = 0.25$ mA) DS, AS, R/ \bar{W}	V_{OH}	2.7	-	V
Output Low Voltage				
($I_{LOAD} = 0.25$ mA) A8-A12, B0-B7	V_{OL}	-	0.3	V
($I_{LOAD} = 0.25$ mA) PA0-PA7, PB0-PB7	V_{OL}	-	0.3	V
($I_{LOAD} = 0.25$ mA) DS, AS, R/ \bar{W}	V_{OL}	-	0.3	V
Input High Voltage				
PA0-PA7, PB0-PB7, B0-B7	V_{IH}	2.1	-	V
TIMER, \bar{IRQ} , \bar{RESET}	V_{IH}	2.5	-	V
OSC1	V_{IH}	2.1	-	V
Input Low Voltage (All inputs)	V_{IL}	-	0.5	V
Frequency of Operation				
Crystal	f_{OSC}	0.032	1.0	MHz
External Clock	f_{OSC}	DC	1.0	MHz
Input Current				
\bar{RESET} , \bar{IRQ} , Timer, OSC1	I_{in}	-	± 1	μA
Three-State Output Leakage				
PA0-OA7, PB0-PB7, B0-B7	I_{TSL}	-	± 10	μA
Capacitance				
\bar{RESET} , \bar{IRQ} , Timer	C_{in}	-	8.0	pF
Capacitance				
DS, AS, R/ \bar{W} , A8-A12, PA0-PA7, PB0-PB7, B0-B7	C_{out}	-	12.0	pF

NOTE: Test conditions for Quiescent Current Values are:

Port A and B programmed as inputs.

 $V_{IL} = 0.2$ V for PA0-PA7, PB0-PB7, and B0-B7. $V_{IH} = V_{DD} - 0.2$ V for \bar{RESET} , \bar{IRQ} , and Timer.OSC1 input is a squarewave from $V_{SS} + 0.2$ V to $V_{DD} - 0.2$ V.

OSC2 output load (including tester) is 35 pF maximum.

Wait mode I_{DD} is affected linearly by this capacitance.

RCA CMOS LSI Products

CDP6805E2

DC ELECTRICAL CHARACTERISTICS 5.0 V ($V_{DD}=5.0\text{ Vdc} \pm 10\%$, $V_{SS}=0$, $T_A=0^\circ$ to 70° , unless otherwise noted)

Characteristics	Symbol	Min	Max	Unit
Output Voltage $I_{LOAD} \leq 10.0\ \mu\text{A}$	V_{OL}	–	0.1	V
	V_{OH}	$V_{DD}-0.1$	–	V
Total Supply Current ($C_L = 130\ \text{pF}$ – On Bus, $C_L = 50\ \text{pF}$ – On Ports, No DC Loads, $t_{cyc} = 1.0\ \mu\text{s}$ Run ($V_{IL} = 0.2\ \text{V}$, $V_{IH} = V_{DD} - 0.2\ \text{V}$)	I_{DD}	–	10	mA
Wait (Test Conditions – See Note Below)	I_{DD}	–	1.5	mA
Stop (Test Conditions – See Note Below)	I_{DD}	–	200	μA
Output High Voltage ($I_{LOAD} = 1.6\ \text{mA}$) A8-A12, B0-B7	V_{OH}	4.1	–	V
($I_{LOAD} = 0.36\ \text{mA}$) PA0-PA7, PB0-PB7	V_{OH}	4.1	–	V
($I_{LOAD} = 1.6\ \text{mA}$) DS, AS, R/ \overline{W}	V_{OH}	4.1	–	V
Output Low Voltage ($I_{LOAD} = 1.6\ \text{mA}$) A8-A12, B0-B7	V_{OL}	–	0.4	V
($I_{LOAD} = 1.6\ \text{mA}$) PA0-PA7, PB0-PB7	V_{OL}	–	0.4	V
($I_{LOAD} = 1.6\ \text{mA}$) DS, AS, R/ \overline{W}	V_{OL}	–	0.4	V
Input High Voltage PA0-PA7, PB0-PB7	V_{IH}	$V_{DD}-2.0$	–	V
TIMER, \overline{IRQ} , RESET	V_{IH}	$V_{DD}-0.8$	–	V
OSC1	V_{IH}	$V_{DD}-1.5$	–	V
Input Low Voltage (All Inputs)	V_{IL}	–	0.8	V
Frequency of Operation Crystal	f_{OSC}	0.032	5.0	MHz
External Clock	f_{OSC}	DC	5.0	MHz
Input Current \overline{RESET} , \overline{IRQ} , Timer, OSC1	I_{in}	–	± 1	μA
Three-State Output Leakage PA0-PA7, PB0-PB7, B0-B7	I_{TSI}	–	± 10	μA
Capacitance \overline{RESET} , \overline{IRQ} , Timer	C_{in}	–	8.0	pF
Capacitance DS, AS, R/ \overline{W} , A8-A12, PA0-PA7, PB0-PB7, B0-B7	C_{out}	–	12.0	pF

NOTE: Test conditions for Quiescent Current Values are:

Port A and B programmed as inputs.

$V_{IL} = 0.2\ \text{V}$ for PA0-PA7, PB0-PB7, and B0-B7.

$V_{IH} = V_{DD} - 0.2\ \text{V}$ for \overline{RESET} , \overline{IRQ} , and Timer.

OSC1 input is a squarewave from $V_{SS} + 0.2\ \text{V}$ to $V_{DD} - 0.2\ \text{V}$.

OSC2 output load (including tester) is 35 pF maximum.

Wait mode (I_{DD}) is affected linearly by this capacitance.

DC ELECTRICAL CHARACTERISTICS 5.0 V ($V_{DD}=5.0\text{ Vdc} \pm 10\%$, $V_{SS}=0$, $T_A=0^\circ$ to 70° , unless otherwise noted)

Characteristics	Symbol	Min	Max	Unit
Output Voltage $I_{LOAD} \leq 10.0\ \mu\text{A}$	V_{OL}	–	0.1	V
	V_{OH}	$V_{DD}-0.1$	–	V
Total Supply Current ($C_L = 130\ \text{pF}$ – On Bus, $C_L = 50\ \text{pF}$ – On Ports, No DC Loads, $t_{cyc} = 1.0\ \mu\text{s}$ Run ($V_{IL} = 0.2\ \text{V}$, $V_{IH} = V_{DD} - 0.2\ \text{V}$) Wait (Test Conditions – See Note Below) Stop (Test Conditions – See Note Below)	I_{DD}	–	10	mA
	I_{DD}	–	1.5	mA
	I_{DD}	–	200	μA
Output High Voltage ($I_{LOAD} = 1.6\ \text{mA}$) A8-A12, B0-B7	V_{OH}	4.1	–	V
($I_{LOAD} = 0.36\ \text{mA}$) PA0-PA7, PB0-PB7	V_{OH}	4.1	–	V
($I_{LOAD} = 1.6\ \text{mA}$) DS, AS, R/ \bar{W}	V_{OH}	4.1	–	V
Output Low Voltage ($I_{LOAD} = 1.6\ \text{mA}$) A8-A12, B0-B7	V_{OL}	–	0.4	V
($I_{LOAD} = 1.6\ \text{mA}$) PA0-PA7, PB0-PB7	V_{OL}	–	0.4	V
($I_{LOAD} = 1.6\ \text{mA}$) DS, AS, R/ \bar{W}	V_{OL}	–	0.4	V
Input High Voltage PA0-PA7, PB0-PB7	V_{IH}	$V_{DD}-2.0$	–	V
TIMER, \bar{IRQ} , RESET	V_{IH}	$V_{DD}-0.8$	–	V
OSC1	V_{IH}	$V_{DD}-1.5$	–	V
Input Low Voltage (All Inputs)	V_{IL}	–	0.8	V
Frequency of Operation Crystal	f_{OSC}	0.032	5.0	MHz
External Clock	f_{OSC}	DC	5.0	MHz
Input Current RESET, \bar{IRQ} , Timer, OSC1	I_{in}	–	± 1	μA
Three-State Output Leakage PA0-PA7, PB0-PB7, B0-B7	I_{TSI}	–	± 10	μA
Capacitance RESET, \bar{IRQ} , Timer	C_{in}	–	8.0	pF
Capacitance DS, AS, R/ \bar{W} , A8-A12, PA0-PA7, PB0-PB7, B0-B7	C_{out}	–	12.0	pF

NOTE: Test conditions for Quiescent Current Values are:

Port A and B programmed as inputs.

$V_{IL} = 0.2\ \text{V}$ for PA0-PA7, PB0-PB7, and B0-B7.

$V_{IH} = V_{DD} - 0.2\ \text{V}$ for RESET, \bar{IRQ} , and Timer.

OSC1 input is a squarewave from $V_{SS} + 0.2\ \text{V}$ to $V_{DD} - 0.2\ \text{V}$.

OSC2 output load (including tester) is 35 pF maximum.

Wait mode (I_{DD}) is affected linearly by this capacitance.

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TABLE 1 — CONTROL TIMING ($V_{SS}=0$, $T_A=0^\circ$ to 70°C)

Characteristics	Symbol	$V_{DD}=3\text{ V}$ $f_{OSC}=1\text{ MHz}$			$V_{DD}=5\text{ V} \pm 10\%$ $f_{OSC}=5\text{ MHz}$			Unit
		Min	Typ	Max	Min	Typ	Max	
I/O Port Timing — Input Setup Time (Figure 3)	t_{PVASL}	500	—	—	250	—	—	ns
Input Hold Time (Figure 3)	t_{ASLPX}	100	—	—	100	—	—	ns
Output Delay Time (Figure 3)	t_{ASLPV}	—	—	0	—	—	0	ns
Interrupt Setup Time (Figure 6)	t_{ILASL}	2	—	—	0.4	—	—	μs
Crystal Oscillator Startup Time (Figure 5)	t_{OXOV}	—	30	300	—	15	100	ms
Wait Recovery Startup Time (Figure 7)	t_{VASH}	—	—	10	—	—	2	μs
Stop Recovery Startup Time (Crystal Oscillator) (Figure 8)	t_{LASH}	—	30	300	—	15	100	ms
Required Interrupt Release (Figure 6)	t_{DSLH}	—	—	5	—	—	1.0	μs
Timer Pulse Width (Figure 7)	t_{TH}, t_{TL}	0.5	—	—	0.5	—	—	t_{cyc}
Reset Pulse Width (Figure 5)	t_{RL}	5.2	—	—	1.05	—	—	μs
Timer Period (Figure 7)	t_{LTL}	1.0	—	—	1.0	—	—	t_{cyc}
Interrupt Pulse Width Low (Figure 16)	t_{LIH}	1.0	—	—	1.0	—	—	t_{cyc}
Interrupt Pulse Period (Figure 16)	t_{LIL}	*	—	—	*	—	—	t_{cyc}
Oscillator Cycle Period (1/5 of t_{cyc})	t_{LOL}	1000	—	—	200	—	—	ms
OSC1 Pulse Width High	t_{OH}	350	—	—	75	—	—	ns
OSC1 Pulse Width Low	t_{OL}	350	—	—	75	—	—	ns

* The minimum period t_{LIL} should not be less than the number of t_{cyc} cycles it takes to execute the interrupt service routine plus 20 t_{cyc} cycles.

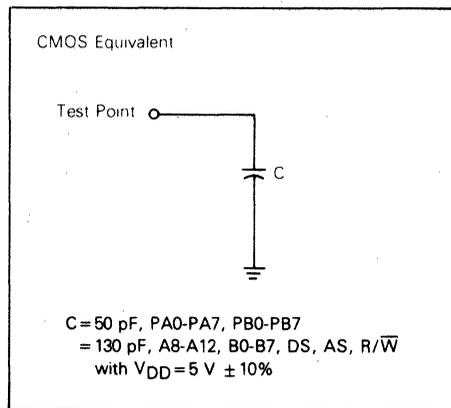
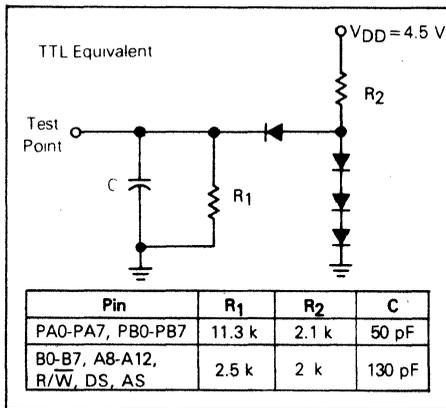
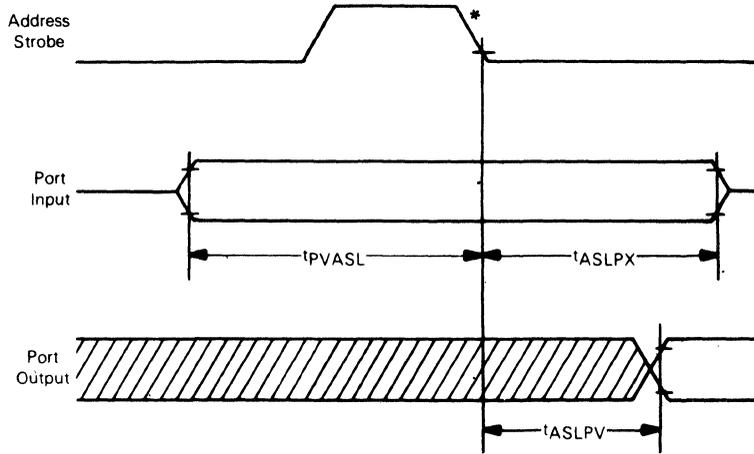


Fig. 2 — Equivalent test-load circuits.

($V_{LOW} = 0.8\text{ V}$, $V_{HIGH} = V_{DD} - 2\text{ V}$, $V_{DD} = 5 \pm 10\%$
 Temp = 0° to 70°C , C_L on Port = 50 pF , $f_{OSC} = 5\text{ MHz}$)

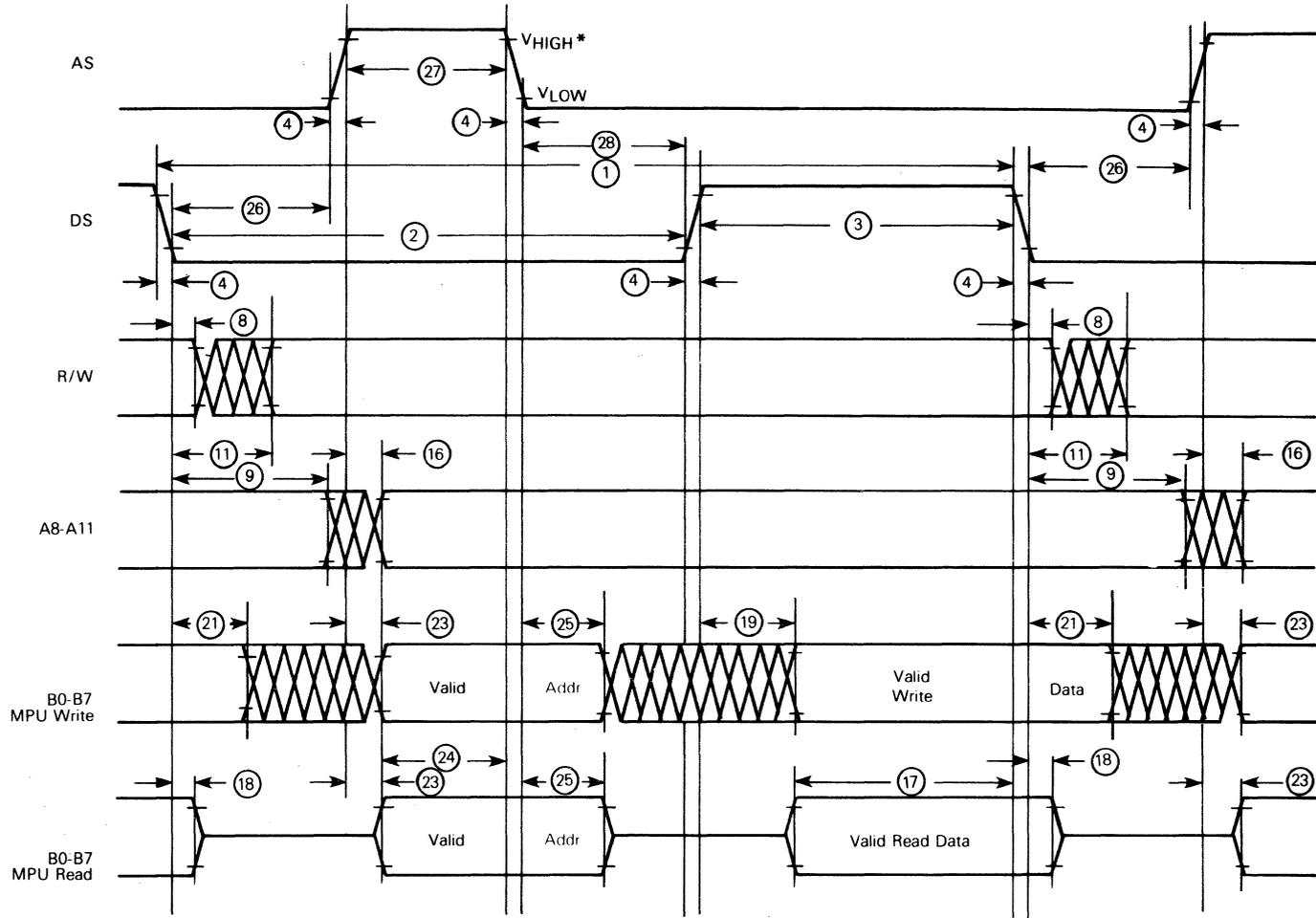


*The address strobe of the first cycle of the next instruction as shown in Table 11.

Fig. 3 - I/O port timing waveforms.

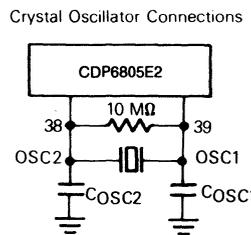
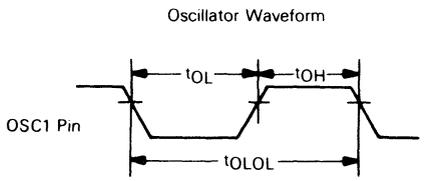
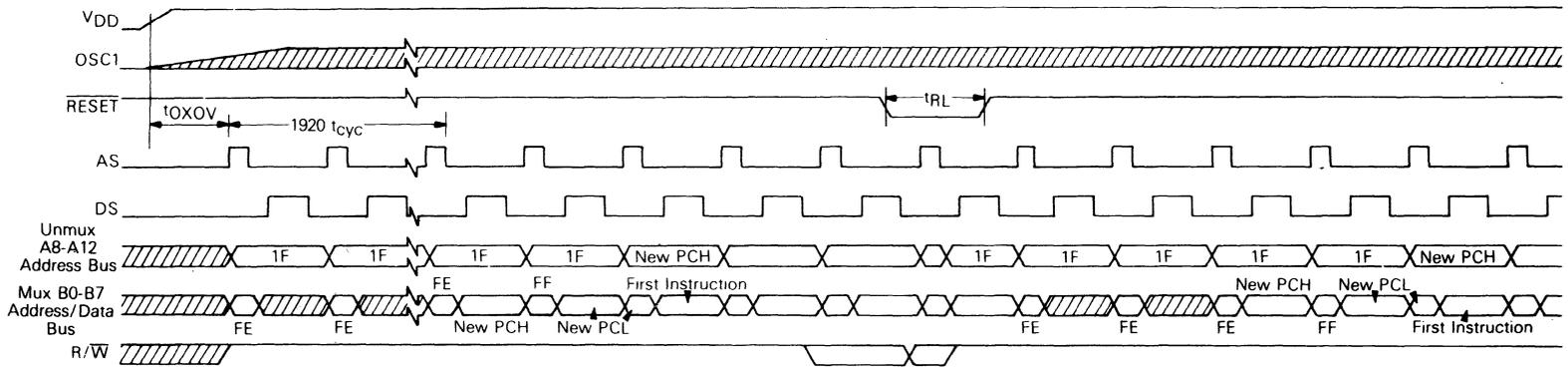
TABLE 2 - BUS TIMING ($T_A = 0^\circ$ to 70°C , $V_{SS} = 0\text{ V}$) See Figure 4

Num	Characteristics	Symbol	$f_{OSC} = 1\text{ MHz}$, $V_{DD} = 3\text{ V}$ 50 pF Load		$f_{OSC} = 5\text{ MHz}$, $V_{DD} = 5\text{ V} \pm 10\%$, 1 TTL and 130 pF Load		Unit
			Min	Max	Min	Max	
1	Cycle Time	t_{cyc}	5000	DC	1000	DC	ns
2	Pulse Width, DS Low	PW_{EL}	2800	—	560	—	ns
3	Pulse Width, DS High or RD, WR, Low	PW_{EH}	1800	—	375	—	ns
4	Clock Transition	t_r, t_f	—	100	—	30	ns
8	R/W Hold	t_{RWH}	10	—	10	—	ns
9	Non-Muxed Address Hold	t_{AH}	800	—	100	—	ns
11	R/W Delay from DS Fall	t_{AD}	—	500	—	300	ns
16	Non-Muxed Address Delay from AS Rise	t_{ADH}	0	200	0	100	ns
17	MPU Read Data Setup	t_{DSR}	200	—	115	—	ns
18	Read Data Hold	t_{DHR}	0	1000	0	160	ns
19	MPU Data Delay, Write	t_{DDW}	—	0	—	120	ns
21	Write Data Hold	t_{DHW}	800	—	55	—	ns
23	Muxed Address Delay from AS Rise	t_{BHD}	0	250	0	120	ns
24	Muxed Address Valid to AS Fall	t_{ASL}	600	—	55	—	ns
25	Muxed Address Hold	t_{AHL}	250	750	60	180	ns
26	Delay DS Fall to AS Rise	t_{ASD}	800	—	160	—	ns
27	Pulse Width, AS High	PW_{ASH}	850	—	175	—	ns
28	Delay, AS Fall to DS Rise	t_{ASED}	800	—	160	—	ns



* V_{HIGH}=2 V, V_{LOW}=0.5 V for V_{DD}=3 V
 V_{HIGH}=V_{DD} - 2 V, V_{LOW}=0.8 V for V_{DD}=5 V ± 10%

Fig. 4 - Bus timing waveforms.



Crystal Parameters Representative Frequencies

	5 MHz	4 MHz	1 MHz
RS max	50Ω	75Ω	400Ω
C0	8 pF	7 pF	5 pF
C1	0.02 pF	0.012 pF	0.008 pF
Q	50 k	40 k	30 k
C _{OSC1}	15-30 pF	15-30 pF	15-40 pF
C _{OSC2}	15-25 pF	15-25 pF	15-30 pF

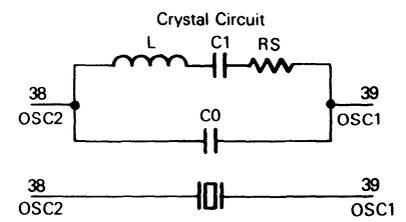
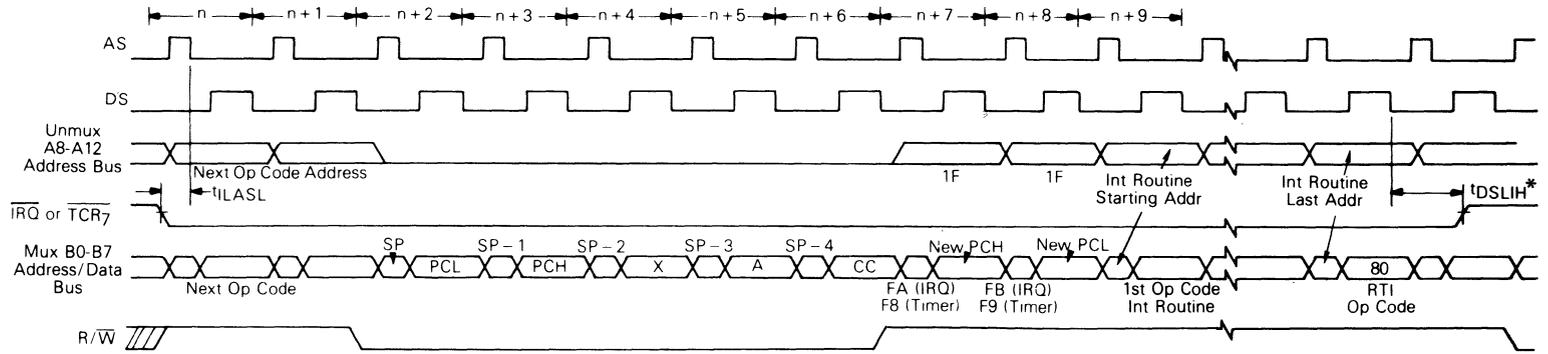


Fig. 5 - Power-on reset and reset timing waveforms.



* t_{DSLIIH} - The interrupting device must release the IRQ line within this time to prevent subsequent recognition of the same interrupt.

Fig. 6 - $\overline{\text{IRQ}}$ and $\overline{\text{TCR}}_7$ interrupt timing waveforms.

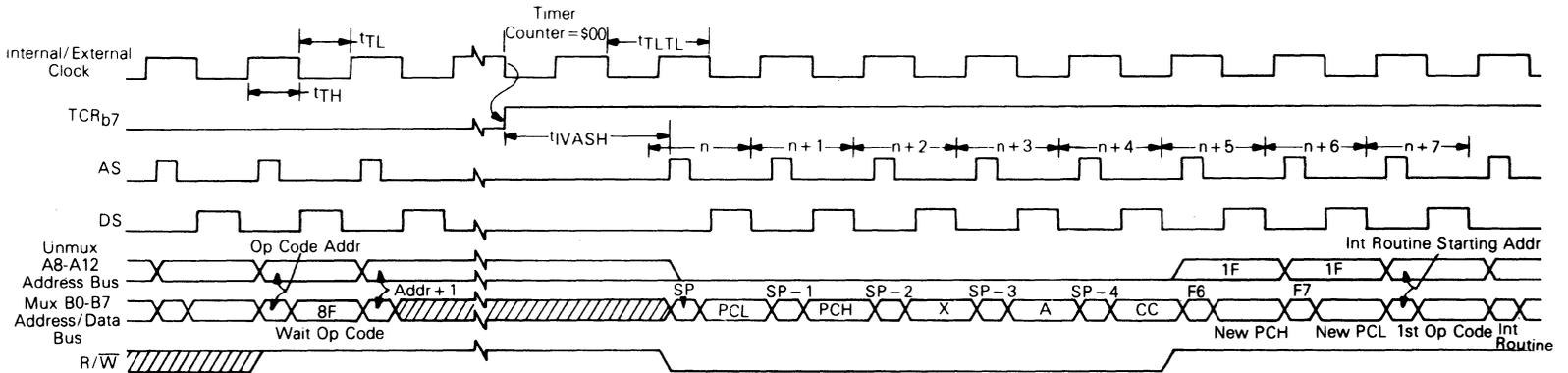
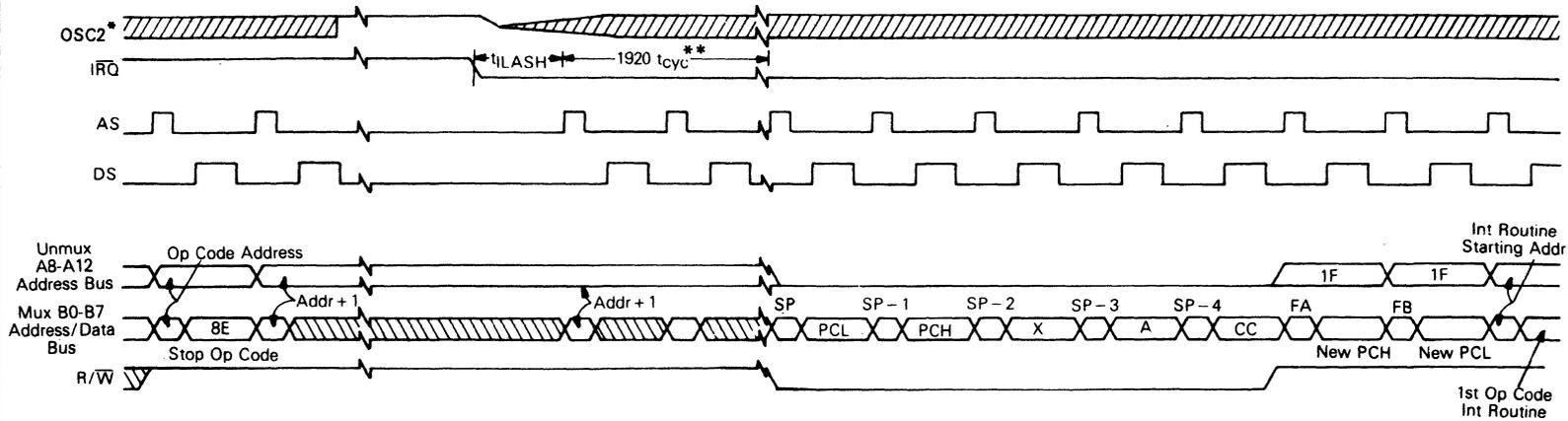


Fig. 7 - Timer interrupt after WAIT instruction timing waveforms.



* Represents the internal gating of the OSC1 input pin.
 ** t_{cyc} is one instruction cycle (for $f_{OSC} = 5 \text{ MHz}$, $t_{cyc} = 1 \mu\text{s}$)

Fig. 8 - Interrupt recovery from STOP instruction timing waveforms.

FUNCTIONAL PIN DESCRIPTION

VDD and VSS — VDD and VSS provide power to the chip. VDD provides power and VSS is ground.

IRQ (Maskable Interrupt Request) — IRQ is a level-sensitive and edge sensitive input which can be used to request an interrupt sequence. The MPU completes the current instruction before it responds to the request. If IRQ is low and the interrupt mask bit (I-bit) in the Condition Code Register is clear, the MPU begins an interrupt sequence at the end of the current instruction. The interrupt circuit recognizes both a "Wire ORed" level as well as pulses on the IRQ line (see Interrupt Section for more details). IRQ requires an external resistor to VDD for "Wire OR" operation.

RESET — The RESET input is not required for start-up but can be used to reset the MPU's internal state and provide an orderly software start-up procedure. Refer to the RESET section for a detailed description.

TIMER — The TIMER input is used for clocking the on-chip timer. Refer to TIMER section for a detailed description.

AS (Address Strobe) — Address Strobe (AS) is an output strobe used to indicate the presence of an address on the 8-bit multiplexed bus. The AS line is used to demultiplex the eight least significant address bits from the data bus. A latch controlled by Address Strobe should capture addresses on the negative edge. This output is capable of driving one standard TTL load and 130 pF and is available at fOSC + 5 when the MPU is not in the WAIT or STOP states.

DS (Data Strobe) — This output is used to transfer data to or from a peripheral or memory. DS occurs anytime the MPU does a data read or write. DS also occurs when the MPU does a data transfer to or from the MPU's internal memory. Refer to Table 2 and Figure 4 for timing characteristics. This output is capable of driving one standard TTL load and

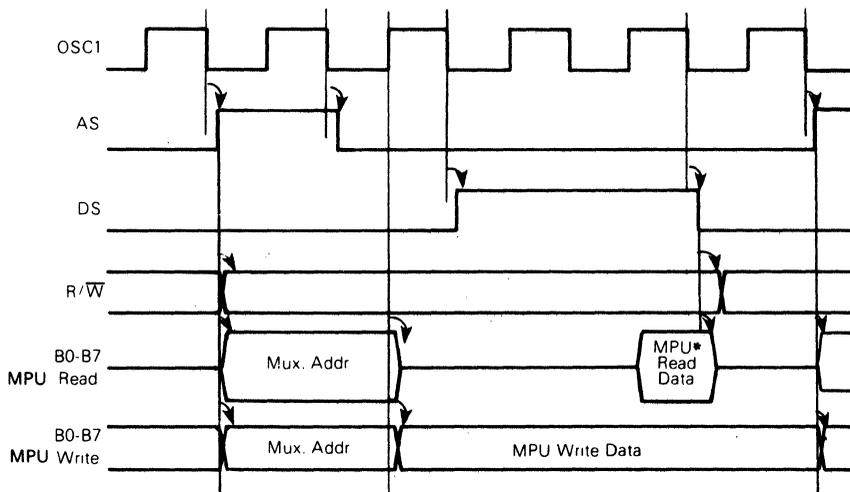
130 pF. DS is a continuous signal at fOSC + 5 when the MPU is not in WAIT or STOP state. Some bus cycles are redundant reads of op code bytes.

R/W (Read/Write) — The R/W output is used to indicate the direction of data transfer for both internal memory and I/O registers, and external peripheral devices and memories. This output is used to indicate to a selected peripheral whether the MPU is going to read or write data on the next Data Strobe (R/W low = processor write; R/W high = processor read). The R/W output is capable of driving one standard TTL load and 130 pF. The normal standby state is Read (high).

A8-A12 (High Order Address Lines) — The A8-A12 output lines constitute the higher order non-multiplexed addresses. Each output line is capable of driving one standard TTL load and 130 pF.

B0-B7 (Address/Data Bus) — The B0-B7 bidirectional lines constitute the lower order addresses and data. These lines are multiplexed, with address present at Address Strobe time and data present at Data Strobe time. When in the data mode, these lines are bidirectional, transferring data to and from memory and peripheral devices as indicated by the R/W pin. As outputs in either the data or address modes, these lines are capable of driving one standard TTL load and 130 pF.

OSC1, OSC2 — The CDP6805E2 provides for two types of oscillator inputs — crystal circuit or external clock. The two oscillator pins are used to interface to a crystal circuit, as shown in Figure 5. If an external clock is used, it must be connected to OSC1. The input at these pins is divided by five to form the cycle rate seen on the AS and DS pins. The frequency range is specified by fOSC. The OSC1 to bus transitions relationships are provided in Figure 9 for system designs using oscillators slower than 5 MHz.



* Read data "latched" on DS fall.

Fig. 9 - OSC1 to bus transitions timing waveforms.

Crystal — The circuit shown in Figure 5 is recommended when using a crystal. The internal oscillator is designed to interface with an AT-cut parallel resonant quartz crystal resonator in the frequency range specified for f_{OSC} in the electrical characteristics table. An external CMOS oscillator is recommended when crystals outside the specified ranges are to be used. The crystal and components should be mounted as close as possible to the input pins to minimize output distortion and start-up stabilization time.

External Clock — An external clock should be applied to the OSC1 input with the OSC2 input not connected, as shown in Figure 10.

FIGURE 10 — EXTERNAL CLOCK CONNECTION

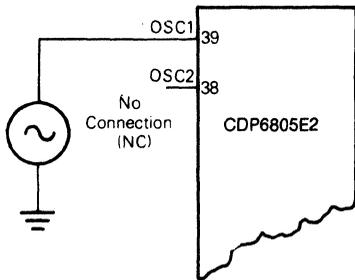
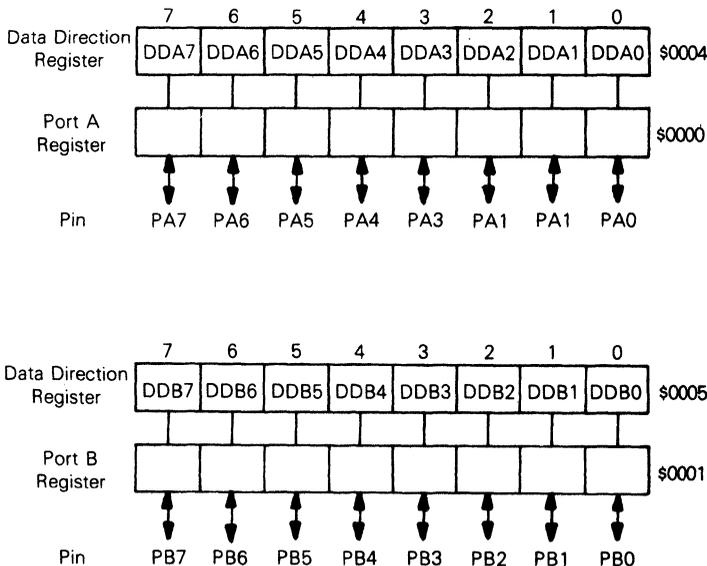


Fig. 10 — External clock connection.

LI (Load Instruction) — This output is used to indicate that a fetch of the next opcode is in progress. LI remains low during an External or Timer interrupt. The LI output is only used for certain debugging and test systems. For normal operations this pin is not connected. The LI output is capable of driving one standard TTL load and 50 pF. This signal overlaps Data Strobe.

PA0-PA7 — These eight pins constitute Input/Output Port A. Each line is individually programmed to be either an input or output under software control via its Data Direction Register as shown below. An I/O pin is programmed as an output when the corresponding DDR bit is set to a "1," and as an input when it is set to a "0". In the output mode the bits are latched and appear on the corresponding output pins. An MPU read of the port bits programmed as outputs reflect the last value written to that location. When programmed as an input, the input data bit(s) are not latched. An MPU read of the port bits programmed as inputs reflects the current status of the corresponding input pins. The Read/Write port timing is shown in Figure 3. See typical I/O Port Circuitry in Figure 11. During a Power-On Reset or external RESET all lines are configured as inputs (zero in Data Direction Register). The output port register is not initialized by reset. The TTL compatible three-state output buffers are capable of driving one standard TTL load and 50 pF. The DDR is a read/write register.

PB0-PB7 — These eight pins interface to Input/Output Port B. Refer to PA0-PA7 description for details of operation.



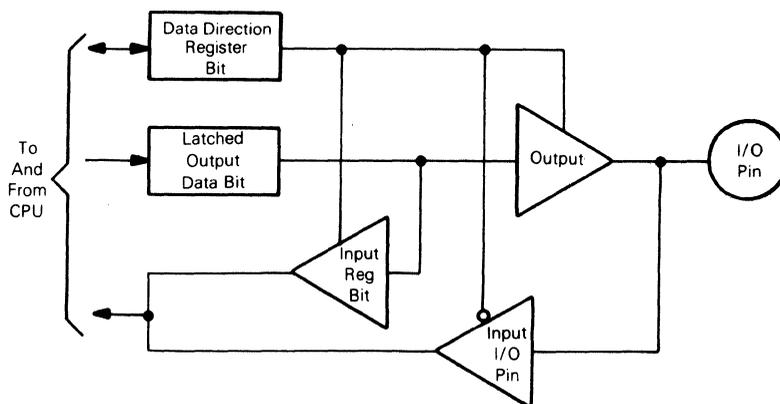


Fig. 11 - Typical I/O port circuitry.

TABLE 3 - I/O PIN FUNCTIONS

R/ \bar{W}	DDR	I/O Pin Functions
0	0	The I/O pin is in input mode. Data is written into the output data latch.
0	1	Data is written into the output data latch and output to the I/O pin.
1	0	The state of the I/O pin is read.
1	1	The I/O pin is in an output mode. The output data latch is read.

MEMORY ADDRESSING

The CDP6805E2 is capable of addressing 8192 bytes of memory and I/O registers. The address space is divided into internal memory space and external memory space, as shown in Figure 12.

The internal memory space is located within the first 128 bytes of memory (first half of page zero) and is comprised of the I/O port locations, timer locations, and 112 bytes of RAM. The MPU can read from or write to any of these locations. A program write to on-chip locations is repeated on the external bus to permit off-chip memory to duplicate the content of on-chip memory. Program reads to on-chip locations also appear on the external bus, but the MPU accepts data only from the addressed on-chip location. Any read data appearing on the input bus is ignored.

The stack pointer is used to address data stored on the stack. Data is stored on the stack during interrupts and subroutine calls. At power up, the stack pointer is set to \$7F and it is decremented as data is pushed onto the stack. When data is removed from the stack, the stack pointer is incremented. A maximum of 64 bytes of RAM is available for stack usage. Since most programs use only a small part of the allotted stack locations for interrupts and/or subroutine stacking purposes, the unused bytes are usable for program data storage.

All memory locations above location \$007F are part of the external memory map. In addition, ten locations in the I/O portion of the lower 128 bytes of memory space, as shown

in Figure 12, are part of the external memory map. All of the external memory space is user definable except the highest 10 locations. Locations \$1FF6 to \$1FFF of the external address space are reserved for interrupt and reset vectors (see Figure 12).

REGISTERS

The CDP6805E2 contains five registers as shown in the programming model in Figure 13. The interrupt stacking order is shown in Figure 14.

ACCUMULATOR (A) - This Accumulator is an 8-bit general purpose register used for arithmetic calculations and data manipulations.

INDEX REGISTER (X) - The X register is an 8-bit register which is used during the indexed modes of addressing. It provides an 8-bit operand which is used to create an effective address. The index register is also used for data manipulations with the Read/Modify/Write type of instructions and as a temporary storage register when not performing addressing operations.

PROGRAM COUNTER (PC) - The program counter is a 13-bit register that contains the address of the next instruction to be executed by the processor.

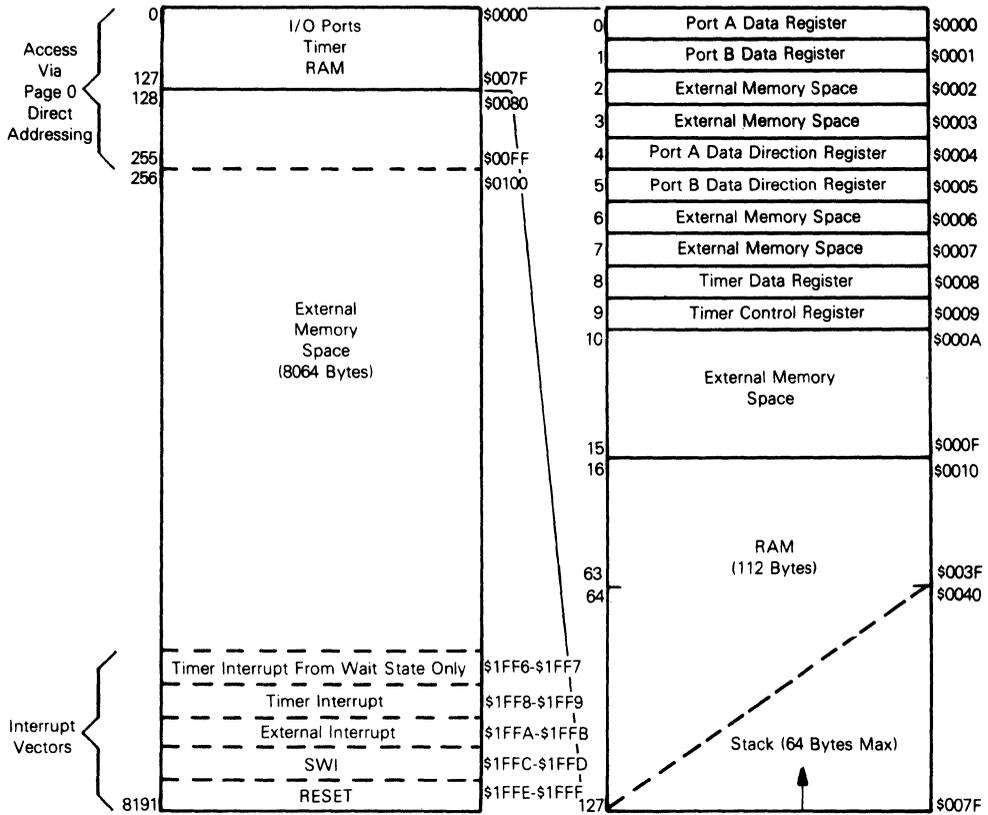


Fig. 12 - Address map.

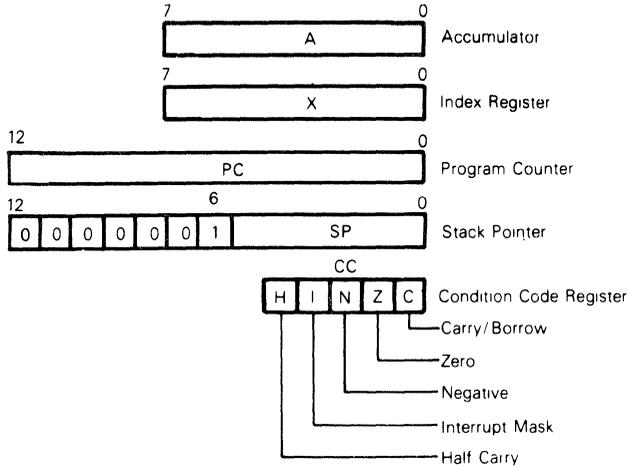
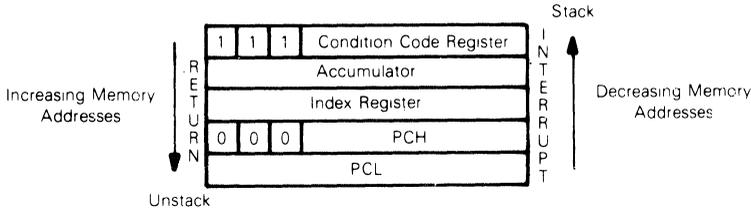


Fig. 13 - Programming model.



NOTE: Since the Stack Pointer decrements during pushes, the PCL is stacked first, followed by PCH, etc. Pulling from the stack is in the reverse order.

Fig. 14 - Stacking order.

STACK POINTER (SP) — The stack pointer is a 13-bit register containing the address of the next free location on the stack. When accessing memory, the seven most-significant bits are permanently set to 0000001. They are appended to the six least-significant register bits to produce an address within the range of \$007F to \$0040. The stack area of RAM is used to store the return address on subroutine calls and the machine state during interrupts. During external or power-on reset, and during a “reset stack pointer” instruction, the stack pointer is set to its upper limit (\$007F). Nested interrupts and/or subroutines may use up to 64 (decimal) locations, beyond which the stack pointer “wraps around” and points to its upper limit thereby losing the previously stored information. A subroutine call occupies two RAM bytes on the stack, while an interrupt uses five bytes.

CONDITION CODE REGISTER (CC) — The condition code register is a 5-bit register in which each bit is used to indicate the results of the instruction just executed. These bits can be individually tested by a program and specific action

taken as a result of their state. Each of the five bits is explained below.

Half Carry Bit (H) — The H-bit is set to a one when a carry occurs between bits 3 and 4 of the ALU during an ADD or ADC instruction. The H-bit is useful in Binary Coded Decimal addition subroutines.

Interrupt Mask Bit (I) — When the I-bit is set, both the external interrupt and the timer interrupt are disabled. Clearing this bit enables the above interrupts. If an interrupt occurs while the I-bit is set, the interrupt is latched and will be processed when the I-bit is next cleared.

Negative Bit (N) — When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation was negative (bit 7 in the result is a logical one).

Zero Bit (Z) — When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation was zero.

Carry Bit (C) — The C-bit is set when a carry or a borrow out of the ALU occurs during an arithmetic instruction. The C-bit is also modified during bit test, shift, rotate, and branch types of instruction.

RESETS

The CDP6805E2 has two reset modes: an active low external reset pin ($\overline{\text{RESET}}$) and a Power-On Reset function; refer to Figure 5.

$\overline{\text{RESET}}$ (Pin #1) — The $\overline{\text{RESET}}$ input pin is used to reset the MPU and provide an orderly software start-up procedure. When using the external reset mode, the $\overline{\text{RESET}}$ pin must stay low for a minimum of one t_{cyc} . The $\overline{\text{RESET}}$ pin is provided with a Schmitt Trigger to improve its noise immunity capability.

Power-On Reset — The Power-on Reset occurs when a positive transition is detected on V_{DD} . The Power-on Reset is used strictly for power turn-on conditions and should not be used to detect any drops in the power supply voltage. There is no provision for a power-down reset. The power-on circuitry provides for a $1920 t_{\text{cyc}}$ delay from the time of the first oscillator operation. If the external reset pin is low at the end of the $1920 t_{\text{cyc}}$ time out, the processor remains in the reset condition.

Either of the two types of reset conditions causes the following to occur:

- Timer control register interrupt request bit (bit 7) is cleared to a "0".
- Timer control register interrupt mask bit (bit 6) is set to a "1".
- All data direction register bits are cleared to a "0" (inputs).
- Stack pointer is set to \$007F.
- The address bus is forced to the reset vector (\$1FFE, \$1FFF).
- Condition code register interrupt mask bit (I) is set to a "1".
- STOP and WAIT latches are reset.
- External interrupt latch is reset.

All other functions, such as other registers (including output ports) the timer, etc., are not cleared by the reset conditions.

INTERRUPTS

The CDP6805E2 is capable of operation with three different interrupts, two hardware (timer interrupt and external interrupt) and one software (SWI). When any of these interrupts occur, normal processing is suspended at the end of the current instruction execution. All of the program registers (the machine state) are pushed onto the stack; refer to Figure 14 for stacking order. The appropriate vector pointing to the starting address of the interrupt service routine is then fetched; refer to Figure 15 for the interrupt sequence.

The priority of the various interrupts from highest to lowest is as follows:

RESET → * → External Interrupt → Timer Interrupt

TIMER INTERRUPT — If the timer mask bit (TCR6) is cleared, then each time the timer decrements to zero (transitions from \$01 to \$00) an interrupt request is generated. The actual processor interrupt is generated only if the interrupt

mask bit of the condition code register is also cleared. When the interrupt is recognized, the current state of the machine is pushed onto the stack and the I-bit in the condition code register is set. This masks further interrupts until the present one is serviced. The processor now vectors to the timer interrupt service routine. The address for this service routine is specified by the contents of \$1FF8 and \$1FF9. The contents of \$1FF6 and \$1FF7 specify the service routine. Also, software must be used to clear the timer interrupt request bit (TCR7). At the end of the timer interrupt service routine, the software normally executes an RTI instruction which restores the machine state and starts executing the interrupted program.

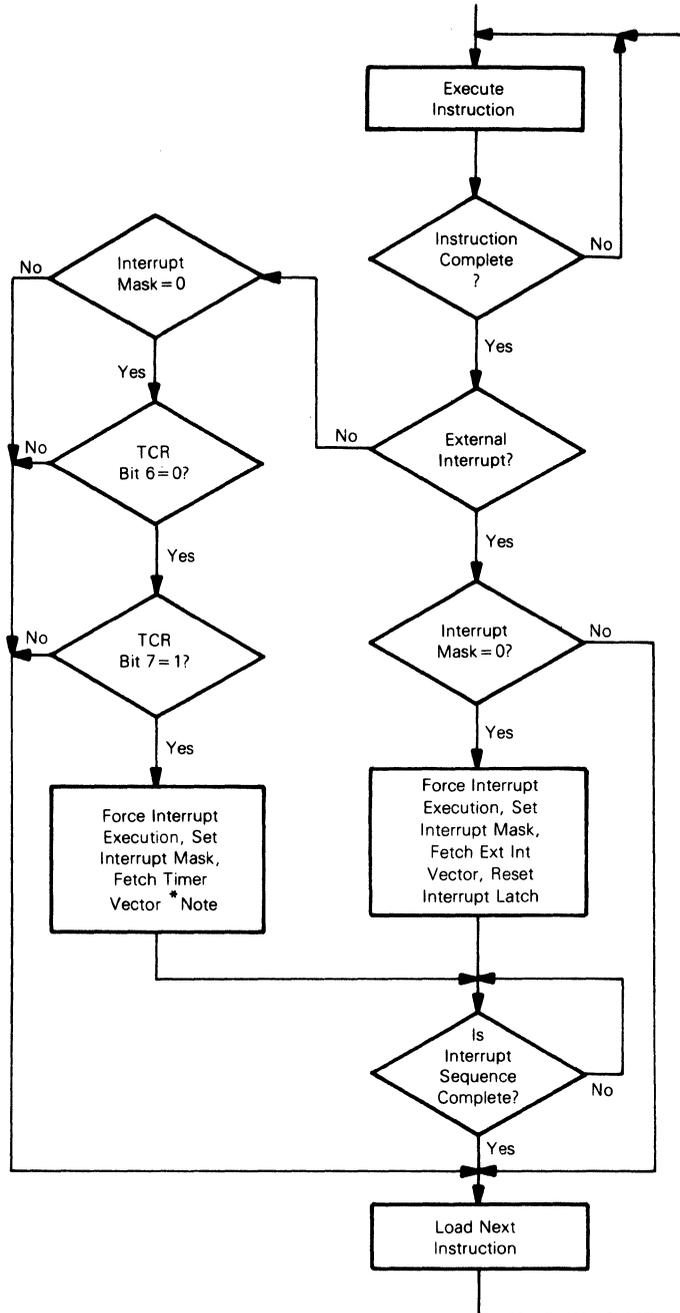
EXTERNAL INTERRUPT — If the interrupt mask bit of the condition code register is cleared and the external interrupt pin $\overline{\text{IRQ}}$ is "low," then the external interrupt occurs. The action of the external interrupt is identical to the timer interrupt with the exception that the service routine address is specified by the contents of \$1FFA and \$1FFB. The interrupt logic recognizes both a "wire ORed" level and pulses on the external interrupt line. Figure 16 shows both a functional diagram and timing for the interrupt line. The timing diagram shows two different treatments of the interrupt line ($\overline{\text{IRQ}}$) to the processor. The first configuration shows many interrupt lines "wire ORed" to form the interrupts at the processor. Thus, if after servicing an interrupt the $\overline{\text{IRQ}}$ remains low, then the next interrupt is recognized. The second method is single pulses on the interrupt line spaced far enough apart to be service. The minimum time between pulses is a function of the length of the interrupt service routine. Once a pulse occurs, the next pulse should not occur until the MPU software has exited the routine (an RTI occurs). This time (t_{LIL}) is obtained by adding 20 instruction cycles (one cycle $t_{\text{cyc}} = 5/f_{\text{OSC}}$) to the total number of cycles it takes to complete the service routine including the RTI instruction; refer to Figure 6.

SOFTWARE INTERRUPT (SWI) — The software interrupt is an executable instruction. The action of the SWI instruction is similar to the hardware interrupts. The SWI is executed regardless of the state of the interrupt mask in the condition code register. The service routine address is specified by the contents of memory locations \$1FFC and \$1FFD. See Figure 15 for Interrupt and Instruction Processing Flowchart.

The following three functions are not strictly interrupts; however, they are tied very closely to the interrupts. These functions are $\overline{\text{RESET}}$, STOP, WAIT.

$\overline{\text{RESET}}$ — The $\overline{\text{RESET}}$ input pin and the internal Power-on Reset function each cause the program to vector to an initialization program. This vector is specified by the contents of memory locations \$1FFE and \$1FFF. The interrupt mask of the condition code register is also set. Refer to RESET section for details.

*Any current instruction including SWI.



* NOTE: The clear of TCR bit 7 must be accomplished with software.

Fig. 15 - Interrupt and instruction processing flowchart.

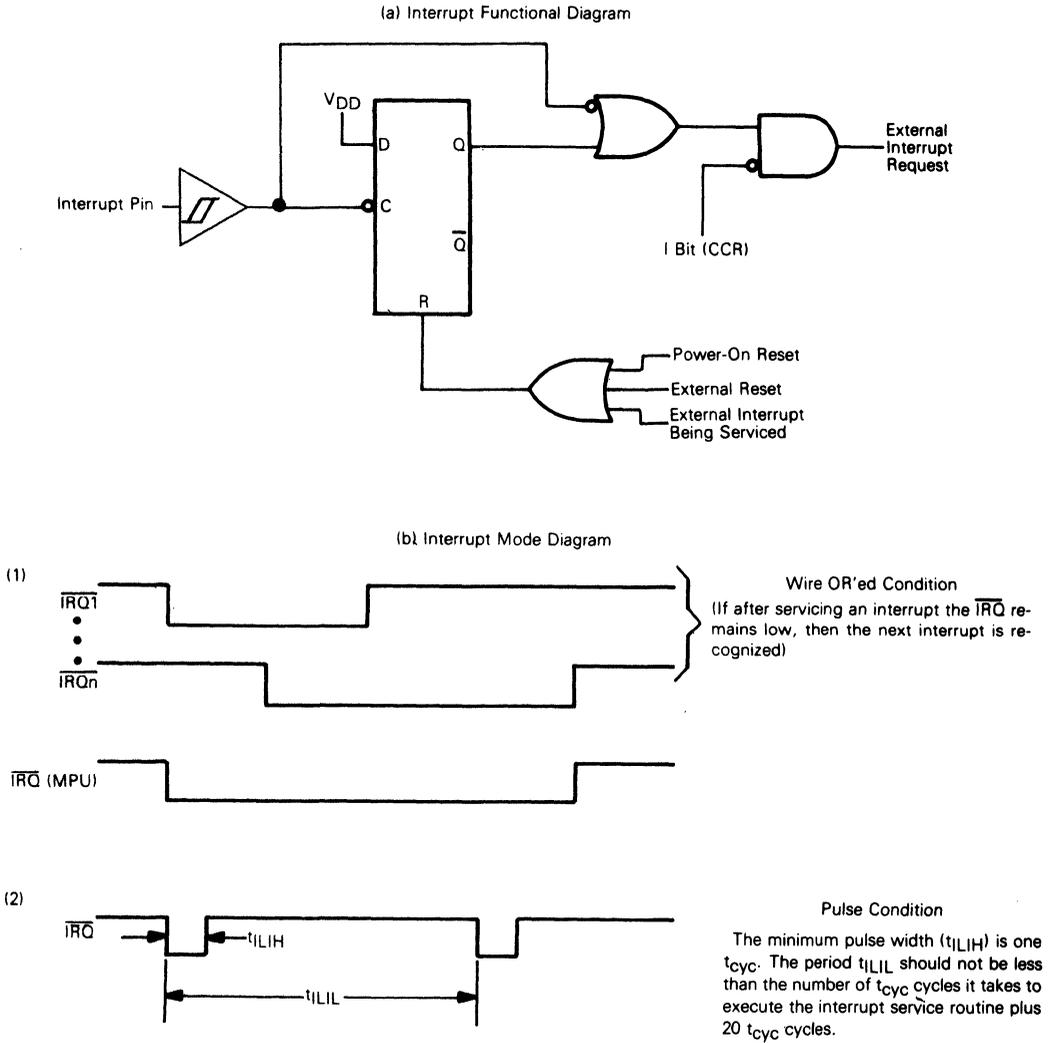


Fig. 16 - External interrupt.

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STOP — The STOP instruction places the CDP6805E2 in a low power consumption mode. In the STOP function the internal oscillator is turned off, causing all internal processing and the timer to be halted; refer to Figure 17. The DS and AS lines go to a low state and the R/W line goes to a high state. The multiplexed address/data bus goes to the data input state. The high order address lines remain at the address of the next instruction. The MPU remains in the STOP mode until an external interrupt or reset occurs; refer to Figure 8 and 17.

During the STOP mode, timer control register (TCR) bits 6 and 7 are altered to remove any pending timer interrupt requests and to disable any further timer interrupts. External interrupts are enabled in the condition code register. All other registers and memory remain unaltered. All I/O lines remain unchanged.

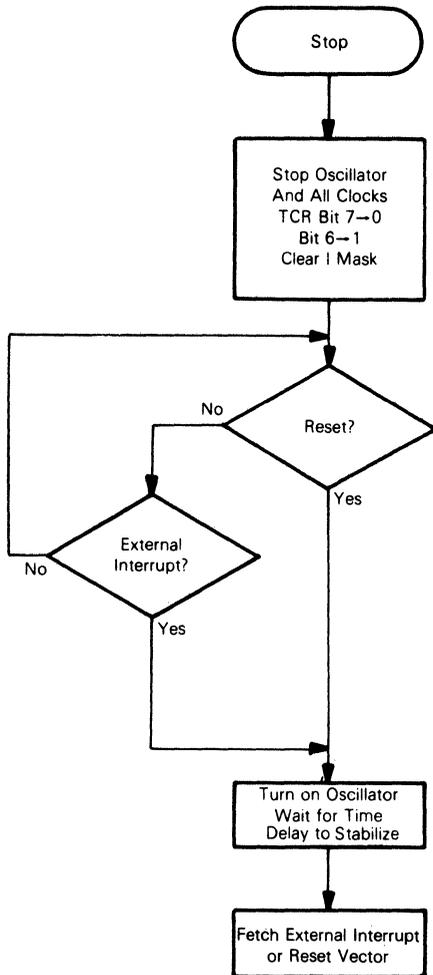


Fig. 17 — Stop function flowchart.

WAIT — The WAIT instruction places the MC146805E2 in a low power consumption mode, but the WAIT mode con-

sumes somewhat more power than the STOP mode; refer to Table 1. In the WAIT function, the internal clock is disabled from all internal circuitry except the Timer circuit; refer to Figure 18. Thus, all internal processing is halted except the Timer which is allowed to count in a normal sequence. The R/W line goes to a high state, the multiplexed address/data bus goes to the data input state, and the DS and AS lines go to the low state. The high order address lines remain at the address of the next instruction. The MPU remains in this state until an external interrupt, timer interrupt, or a reset occurs; refer to Figures 7 and 18.

During the WAIT mode, the I-bit in the condition code register is cleared to enable interrupts. All other registers, memory, and I/O lines remain in their last state. The timer may be enabled to allow a periodic exit from the WAIT mode. If an external and a timer interrupt occur at the same time, the external interrupt is serviced first; then, if the timer interrupt request is not cleared in the external interrupt routine, the normal timer interrupt (not the timer WAIT interrupt) is serviced since the MCU is no longer in the WAIT mode.

TIMER

The MPU timer contains a single 8-bit software programmable counter with 7-bit software selectable prescaler. The counter may be preset under program control and decrements towards zero. When the counter decrements to zero, the timer interrupt request bit, i.e., bit 7 of the Timer Control Register (TCR) is set. Then if the timer interrupt is not masked, i.e., bit 6 of the TCR and the I-bit in the Condition Code Register are both cleared, the processor receives an interrupt. After completion of the current instruction, the processor proceeds to store the appropriate registers on the stack, and then fetches the timer vector address from locations \$1FF8 and \$1FF9 in order to begin servicing the interrupt, unless it was in locations \$1FF6 and \$1FF7 the WAIT mode.

The counter continues to count after it reaches zero, allowing the software to determine the number of internal or external input clocks since the timer interrupt request bit was set. The counter may be read at any time by the processor without disturbing the count. The contents of the counter becomes stable prior to the read portion of a cycle and does not change during the read. The timer interrupt request bit remains set until cleared by the software. If this happens before the timer interrupt is serviced, the interrupt is lost. TCR7 may also be used as a scanned status bit in a non-interrupt mode of operation (TCR6=1).

The prescaler is a 7-bit divider which is used to extend the maximum length of the timer. Bit 0, bit 1, and bit 2 of the TCR are programmed to choose the appropriate prescaler output which is used as the counter input. The processor cannot write into or read from the prescaler; however, its contents are cleared to all "0's" by the write operation into TCR when bit 3 of the written data equals 1, which allows for truncation-free counting.

The Timer input can be configured for three different operating modes, plus a disable mode depending on the value written to the TCR4, TCR5 control bits. Refer to the TIMER CONTROL REGISTER section.

Timer Input Mode 1 — If TCR4 and TCR5 are both programmed to a "0", the input to the Timer is from an internal clock and the Timer input is disabled. The internal clock mode can be used for periodic interrupt generation, as well

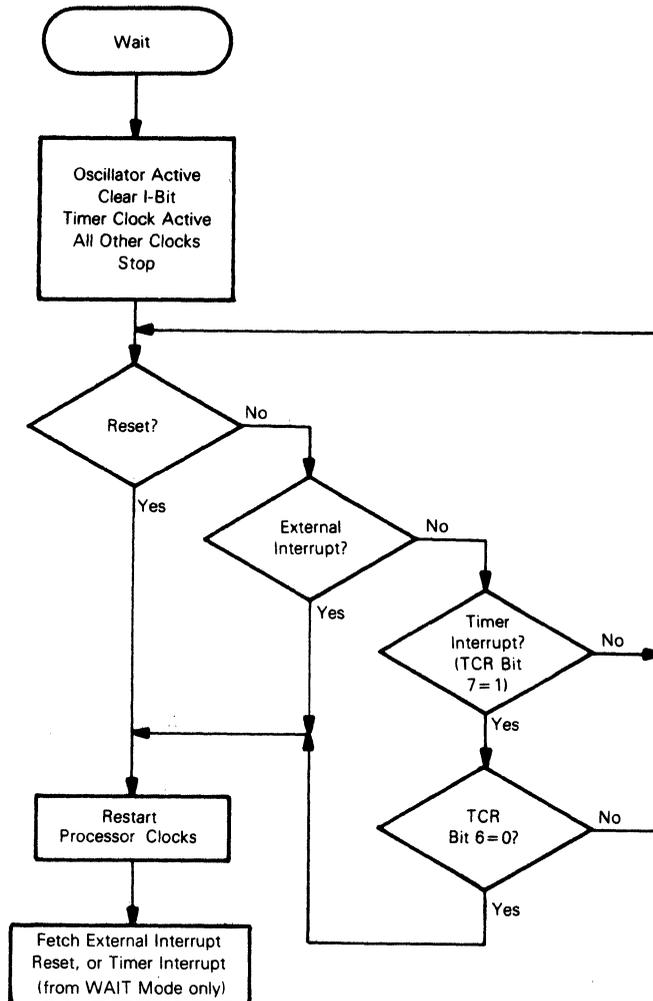


Fig. 18 - Wait function flowchart.

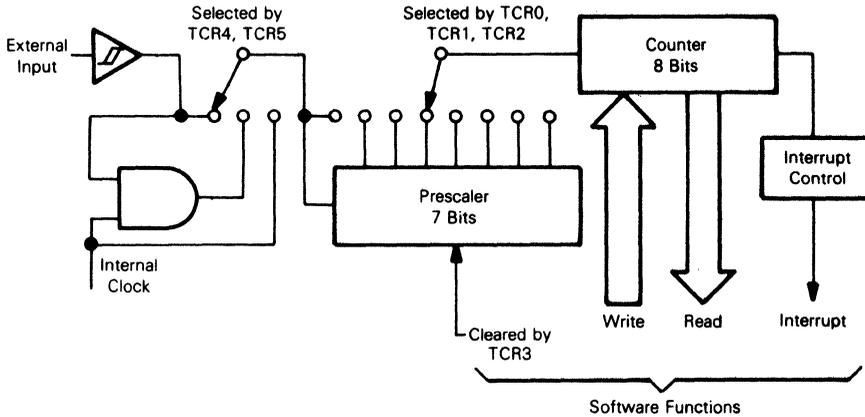
as a reference in frequency and event measurement. The internal clock is the instruction cycle clock and is coincident with Address Strobe (AS) except during a WAIT instruction. During a WAIT instruction the AS pin goes to a low state but the internal clock to the Timer continues to run at its normal rate.

Timer Input Mode 2 - With TCR4=1 and TCR5=0, the internal clock and the TIMER input pin are ANDed together to form the Timer input signal. This mode can be used to measure external pulse widths. The external pulse simply turns on the internal clock for the duration of the pulse. The resolution of the count in this mode is ± 1 clock and therefore accuracy improves with longer input pulse widths.

Timer Input Mode 3 - If TCR4=0 and TCR5=1, then all inputs to the Timer are disabled.

Timer Input Mode 4 - If TCR4=1 and TCR5=1, the internal clock input to the Timer is disabled and the TIMER input pin becomes the input to the Timer. The external Timer pin can, in this mode, be used to count external events as well as external frequencies for generating periodic interrupts.

Figure 19 shows a block diagram of the Timer subsystem. Power-on Reset and the STOP instruction cause the counter to be set to \$F0.



- NOTES:**
1. Prescaler and 8-bit counter are clocked falling edge of the internal clock (AS) or external input.
 2. Counter is written to during Data Strobe (DS) and counts down continuously.

Fig. 19 - Timer block diagram.

Timer Control Register (TCR)

7	6	5	4	3	2	1	0
TCR7	TCR6	TCR5	TCR4	TCR3	TCR2	TCR1	TCR0

All bits in this register except bit 3 are Read/Write bits.

TCR7 - Timer interrupt request bit: bit used to indicate the timer interrupt when it is logic "1".

- 1 - Set whenever the counter decrements to zero, or under program control.
- 0 - Cleared on external reset, power-on reset, STOP instruction, or program control.

TCR6 - Timer interrupt mask bit: when this bit is a logic "1" it inhibits the timer interrupt to the processor.

- 1 - Set on external reset, power-on reset, STOP instruction, or program control.
- 0 - Cleared under program control.

TCR5 - External or internal bit: selects the input clock source to be either the external timer pin or the internal clock. (Unaffected by $\overline{\text{RESET}}$.)

- 1 - Select external clock source.
- 0 - Select internal clock source (AS).

TCR4 - External enable bit: control bit used to enable the external timer pin. (Unaffected by $\overline{\text{RESET}}$.)

- 1 - Enable external timer pin.
- 0 - Disable external timer pin.

TCR5 TCR4

0	0	Internal clock (AS) to Timer
0	1	AND of internal clock (AS) and TIMER pin to Timer
1	0	Inputs to Timer disabled
1	1	TIMER pin to Timer

Refer to Figure 19 for Logic Representation.

TCR3 - Timer Prescaler Reset bit: writing a "1" to this bit resets the prescaler to zero. A read of this location always indicates a "0." (Unaffected by $\overline{\text{RESET}}$.)

TCR2, TCR1, TCR0 - Prescaler address bits: decoded to select one of eight taps on the prescaler. (Unaffected by $\overline{\text{RESET}}$.)

Prescaler

TCR2	TCR1	TCR0	Result
0	0	0	+1
0	0	1	+2
0	1	0	+4
0	1	1	+8
1	0	0	+16
1	0	1	+32
1	1	0	+64
1	1	1	+128

INSTRUCTION SET

The MPU has a set of 61 basic instructions. They can be divided into five different types: register/memory, read/modify/write, branch, bit manipulation, and control. The following paragraphs briefly explain each type. All the instructions within a given type are presented in individual tables.

REGISTER/MEMORY INSTRUCTIONS — Most of these instructions use two operands. One operand is either the accumulator or the index register. The other operand is obtained from memory using one of the addressing modes. The jump unconditional (JMP) and jump to subroutine (JSR) instructions have no register operand. Refer to Table 4.

READ/MODIFY/WRITE INSTRUCTIONS — These instructions read a memory location or a register, modify or test its contents, and write the modified value back to memory or to the register. The test for negative or zero (TST) instruction is an exception to the read/modify/write sequence since it does not modify the value. Refer to Table 5.

BRANCH INSTRUCTIONS — This set of instructions branches if a particular condition is met, otherwise no operation is performed. Branch instructions are two byte instructions. Refer to Table 6.

BIT MANIPULATION INSTRUCTIONS — The MPU is capable of setting or clearing any bit which resides in the first 256 bytes of the memory space, where all port registers, port DDRs, timer, timer control, and on-chip RAM reside. An additional feature allows the software to test and branch on the state of any bit within these 256 locations. The bit set, bit clear and bit test and branch functions are all implemented with a single instruction. For the test and branch instructions the value of the bit tested is also placed in the carry bit of the Condition Code Register. Refer to Table 7 for instruction cycle timing.

CONTROL INSTRUCTIONS — These instructions are register reference instructions and are used to control processor operation during program execution. Refer to Table 8 for instruction cycle timing.

ALPHABETICAL LISTING — The complete instruction set is given in alphabetical order in Table 9.

OPCODE MAP SUMMARY — Table 10 is an opcode map for the instructions used on the MCU.

ADDRESSING MODES

The MPU uses ten different addressing modes to give the programmer an opportunity to optimize the code to all situations. The various indexed addressing modes make it possible to locate data tables, code conversion tables and scaling tables anywhere in the memory space. Short indexed accesses are single byte instructions, while the longest instructions (three bytes) permit tables throughout memory. Short and long absolute addressing is also included. Two byte

direct addressing instructions access all data bytes in most applications. Extended addressing permits jump instructions to reach all memory. Table 9 shows the addressing modes for each instruction, with the effects each instruction has on the Condition Code Register. An opcode map is shown in Table 10.

The term "Effective Address" or EA is used in describing the various addressing modes, which is defined as the address to or from which the argument for an instruction is fetched or stored. The ten addressing modes of the processor are described below. Parentheses are used to indicate "contents of," an arrow indicates "is replaced by" and a colon indicates concatenation of two bytes.

Inherent — In inherent instructions all the information necessary to execute the instruction is contained in the opcode. Operations specifying only the index register or accumulator, and no other arguments, are included in this mode.

Immediate — In immediate addressing, the operand is contained in the byte immediately following the opcode. Immediate addressing is used to access constants which do not change during program execution (e.g., a constant used to initialize a loop counter).

$$EA = PC + 1; PC = PC + 2$$

Direct — In the direct addressing mode, the effective address of the argument is contained in a single byte following the opcode byte. Direct addressing allows the user to directly address the lowest 256 bytes in memory with a single two byte instruction. This includes all on-chip RAM and I/O registers and up to 128 bytes of off-chip ROM. Direct addressing is efficient in both memory and speed.

$$EA = (PC + 1); PC = PC + 2$$

$$\text{Address Bus High} = 0; \text{Address Bus Low} = (PC + 1)$$

Extended — In the extended addressing mode, the effective address of the argument is contained in the two bytes following the opcode. Instructions with extended addressing modes are capable of referencing arguments anywhere in memory with a single three byte instruction. When using the CDP6805 assembler, the user need not specify whether an instruction uses direct or extended addressing. The assembler automatically selects the most efficient addressing mode.

$$EA = (PC + 1):(PC + 2); PC = PC + 3$$

$$\text{Address Bus High} = (PC + 1); \text{Address Bus Low} = (PC + 2)$$

Indexed, No-Offset — In the indexed, no offset addressing mode, the effective address of the argument is contained in the 8-bit index register. Thus, this addressing mode can access the first 256 memory locations. These instructions are only one byte long. This mode is used to move a pointer through a table or to address a frequently referenced RAM or I/O location.

$$EA = X; PC = PC + 1$$

$$\text{Address Bus High} = 0; \text{Address Bus Low} = X$$

TABLE 4 — REGISTER/MEMORY INSTRUCTIONS

Function	Mnemonic	Addressing Modes																	
		Immediate			Direct			Extended			Indexed (No Offset)			Indexed (8-Bit Offset)			Indexed (16-Bit Offset)		
		Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles
Load A from Memory	LDA	A6	2	2	B6	2	3	C6	3	4	F6	1	3	E6	2	4	D6	3	5
Load X from Memory	LDX	AE	2	2	BE	2	3	CE	3	4	FE	1	3	EE	2	4	DE	3	5
Store A in Memory	STA	—	—	—	B7	2	4	C7	3	5	F7	1	4	E7	2	5	D7	3	6
Store X in Memory	STX	—	—	—	BF	2	4	CF	3	5	FF	1	4	EF	2	5	DF	3	6
Add Memory to A	ADD	AB	2	2	BB	2	3	CB	3	4	FB	1	3	EB	2	4	DB	3	5
Add Memory and Carry to A	ADC	A9	2	2	B9	2	3	C9	3	4	F9	1	3	E9	2	4	D9	3	5
Subtract Memory	SUB	A0	2	2	B0	2	3	C0	3	4	F0	1	3	E0	2	4	D0	3	5
Subtract Memory from A with Borrow	SBC	A2	2	2	B2	2	3	C2	3	4	F2	1	3	E2	2	4	D2	3	5
AND Memory to A	AND	A4	2	2	B4	2	3	C4	3	4	F4	1	3	E4	2	4	D4	3	5
OR Memory with A	ORA	AA	2	2	BA	2	3	CA	3	4	FA	1	3	EA	2	4	DA	3	5
Exclusive OR Memory with A	EOR	A8	2	2	B8	2	3	C8	3	4	F8	1	3	E8	2	4	D8	3	5
Arithmetic Compare A with Memory	CMP	A1	2	2	B1	2	3	C1	3	4	F1	1	3	E1	2	4	D1	3	5
Arithmetic Compare X with Memory	CPX	A3	2	2	B3	2	3	C3	3	4	F3	1	3	E3	2	4	D3	3	5
Bit Test Memory with A (Logical Compare)	BIT	A5	2	2	B5	2	3	C5	3	4	F5	1	3	E5	2	4	D5	3	5
Jump Unconditional	JMP	—	—	—	BC	2	2	CC	3	3	FC	1	2	EC	2	3	DC	3	4
Jump to Subroutine	JSR	—	—	—	BD	2	5	CD	3	6	FD	1	5	ED	2	6	DD	3	7

TABLE 5 — READ/MODIFY/WRITE INSTRUCTIONS

Function	Mnemonic	Addressing Modes														
		Inherent (A)			Inherent (X)			Direct			Indexed (No Offset)			Indexed (8-Bit Offset)		
		Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles
Increment	INC	4C	1	3	5C	1	3	3C	2	5	7C	1	5	6C	2	6
Decrement	DEC	4A	1	3	5A	1	3	3A	2	5	7A	1	5	6A	2	6
Clear	CLR	4F	1	3	5F	1	3	3F	2	5	7F	1	5	6F	2	6
Complement	COM	43	1	3	53	1	3	33	2	5	73	1	5	63	2	6
Negate (2's Complement)	NEG	40	1	3	50	1	3	30	2	5	70	1	5	60	2	6
Rotate Left Thru Carry	ROL	49	1	3	59	1	3	39	2	5	79	1	5	69	2	6
Rotate Right Thru Carry	ROR	46	1	3	56	1	3	36	2	5	76	1	5	66	2	6
Logical Shift Left	LSL	48	1	3	58	1	3	38	2	5	78	1	5	68	2	6
Logical Shift Right	LSR	44	1	3	54	1	3	34	2	5	74	1	5	64	2	6
Arithmetic Shift Right	ASR	47	1	3	57	1	3	37	2	5	77	1	5	67	2	6
Test for Negative or Zero	TST	4D	1	3	5D	1	3	3D	2	4	7D	1	4	6D	2	5

TABLE 6 — BRANCH INSTRUCTIONS

Function	Mnemonic	Relative Addressing Mode		
		Op Code	# Bytes	# Cycles
Branch Always	BRA	20	2	3
Branch Never	BRN	21	2	3
Branch IFF Higher	BHI	22	2	3
Branch IFF Lower or Same	BLS	23	2	3
Branch IFF Carry Clear	BCC	24	2	3
(Branch IFF Higher or Same)	(BHS)	24	2	3
Branch IFF Carry Set	B \overline{C} S	25	2	3
(Branch IFF Lower)	(BLO)	25	2	3
Branch IFF Not Equal	BNE	26	2	3
Branch IFF Equal	BEQ	27	2	3
Branch IFF Half Carry Clear	BHCC	28	2	3
Branch IFF Half Carry Set	BHCS	29	2	3
Branch IFF Plus	BPL	2A	2	3
Branch IFF Minus	BMI	2B	2	3
Branch IFF Interrupt Mask Bit is Clear	BMC	2C	2	3
Branch IFF Interrupt Mask Bit is Set	BMS	2D	2	3
Branch IFF Interrupt Line is Low	BIL	2E	2	3
Branch IFF Interrupt Line is High	BIH	2F	2	3
Branch to Subroutine	BSR	AD	2	6

TABLE 7 — BIT MANIPULATION INSTRUCTIONS

Function	Mnemonic	Addressing Modes					
		Bit Set/Clear			Bit Test and Branch		
		Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles
Branch IFF Bit n is Set	BRSET n (n=0...7)	—	—	—	2*n	3	5
Branch IFF Bit n is Clear	BRCLR n (n=0...7)	—	—	—	01+2*n	3	5
Set Bit n	BSET n (n=0...7)	10+2*n	2	5	—	—	—
Clear Bit n	BCLR n (n=0...7)	11+2*n	2	5	—	—	—

TABLE 8 — CONTROL INSTRUCTIONS

Function	Mnemonic	Inherent		
		Op Code	# Bytes	# Cycles
Transfer A to X	TAX	97	1	2
Transfer X to A	TXA	9F	1	2
Set Carry Bit	SEC	99	1	2
Clear Carry Bit	CLC	98	1	2
Set Interrupt Mask Bit	SEI	9B	1	2
Clear Interrupt Mask Bit	CLI	9A	1	2
Software Interrupt	SWI	83	1	10
Return from Subroutine	RTS	81	1	6
Return from Interrupt	RTI	80	1	9
Reset Stack Pointer	RSP	9C	1	2
No-Operation	NOP	9D	1	2
Stop	STOP	8E	1	2
Wait	WAIT	8F	1	2

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TABLE 9 – INSTRUCTION SET

Mnemonic	Addressing Modes									Condition Codes					
	Inherent	Immediate	Direct	Extended	Relative	Indexed (No Offset)	Indexed (8 Bits)	Indexed (16 Bits)	Bit Set/Clear	Bit Test & Branch	H	I	N	Z	C
ADC		X	X	X		X	X	X			Λ	●	Λ	Λ	Λ
ADD		X	X	X		X	X	X			Λ	●	Λ	Λ	Λ
AND		X	X	X		X	X	X			●	●	Λ	Λ	●
ASL	X		X			X	X				●	●	Λ	Λ	Λ
ASR	X		X			X	X				●	●	Λ	Λ	Λ
BCC					X						●	●	●	●	●
BCLR									X		●	●	●	●	●
BCS					X						●	●	●	●	●
BEQ					X						●	●	●	●	●
BHCC					X						●	●	●	●	●
BHCS					X						●	●	●	●	●
BHI					X						●	●	●	●	●
BHS					X						●	●	●	●	●
BIH					X						●	●	●	●	●
BIL					X						●	●	●	●	●
BIT		X	X	X		X	X	X			●	●	Λ	Λ	●
BLO					X						●	●	●	●	●
BLS					X						●	●	●	●	●
BMC					X						●	●	●	●	●
BMI					X						●	●	●	●	●
BMS					X						●	●	●	●	●
BNE					X						●	●	●	●	●
BPL					X						●	●	●	●	●
BRA					X						●	●	●	●	●
BRN					X						●	●	●	●	●
BRCLR										X	●	●	●	●	Λ
BRSET										X	●	●	●	●	Λ
BSET											●	●	●	●	●
BSR					X				X		●	●	●	●	●
CLC	X										●	●	●	●	0
CLI	X										●	0	●	●	●
CLR	X		X			X	X				●	●	0	1	●
CMP		X	X	X		X	X	X			●	●	Λ	Λ	Λ
COM	X		X			X	X				●	●	Λ	Λ	1
CPX		X	X	X		X	X	X			●	●	Λ	Λ	Λ
DEC	X		X			X	X				●	●	Λ	Λ	●
EOR		X	X	X		X	X	X			●	●	Λ	Λ	●
INC	X		X			X	X				●	●	Λ	Λ	●
JMP			X	X		X	X	X			●	●	●	●	●
JSR			X	X		X	X	X			●	●	●	●	●
LDA		X	X	X		X	X	X			●	●	Λ	Λ	●
LDX		X	X	X		X	X	X			●	●	Λ	Λ	●
LSL	X		X			X	X				●	●	Λ	Λ	Λ
LSR	X		X			X	X				●	●	0	Λ	Λ
NEG	X		X			X	X				●	●	Λ	Λ	Λ
NOP	X										●	●	●	●	●
ORA		X	X	X		X	X	X			●	●	Λ	Λ	●
ROL	X		X			X	X				●	●	Λ	Λ	Λ
ROR	X		X			X	X				●	●	Λ	Λ	Λ
RSP	X										●	●	●	●	●
RTI	X										?	?	?	?	?
RTS	X										●	●	●	●	●
SBC		X	X	X		X	X	X			●	●	Λ	Λ	Λ
SEC	X										●	●	●	●	1
SEI	X										●	1	●	●	●
STA			X	X		X	X	X			●	●	Λ	Λ	●
STOP	X										●	0	●	●	●
STX			X	X		X	X	X			●	●	Λ	Λ	●
SUB		X	X	X		X	X	X			●	●	Λ	Λ	Λ
SWI	X										●	1	●	●	●
TAX	X										●	●	●	●	●
TST	X		X			X	X				●	●	Λ	Λ	Λ
TXA	X										●	●	●	●	●
WAIT	X										●	0	●	●	●

Condition Code Symbols

- | | |
|---------------------------|--|
| H Half Carry (From Bit 3) | Λ Test and Set if True. Cleared Otherwise. |
| I Interrupt Mask | ● Not Affected |
| N Negative (Sign Bit) | ? Load CC Register From Stack |
| Z Zero | 0 Cleared |
| C Carry/Borrow | 1 Set |

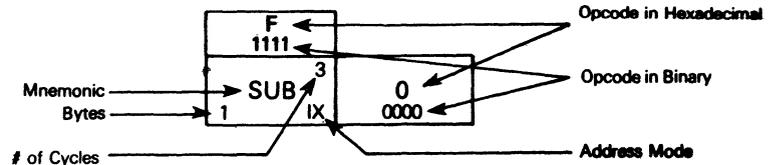
TABLE 10 — CDP6805E2 INSTRUCTION SET OPCODE MAP

HI	Bit Manipulation		Branch	Read/Modify/Write						Control		Register/Memory						Low
	BTB 0	BSC 1	REL 2	DIR 3	INH(A) 4	INH(X) 5	IX1 6	IX 7	INH 8	INH 9	IMM A	DIR B	EXT C	IX2 D	IX1 E	IX F		
Low	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111		
0	BRSET0 BTB	BSET0 BSC	BRA REL	NEG DIR	NEGA INH	NEGX INH	NEG IX1	NEG IX	RTI INH		SUB IMM	SUB DIR	SUB EXT	SUB IX2	SUB IX1	SUB IX	0 0000	
1	BRCLR0 BTB	BCLR0 BSC	BRN REL						RTS INH		CMP IMM	CMP DIR	CMP EXT	CMP IX2	CMP IX1	CMP IX	1 0001	
2	BRSET1 BTB	BSET1 BSC	BHI REL								SBC IMM	SBC DIR	SBC EXT	SBC IX2	SBC IX1	SBC IX	2 0010	
3	BRCLR1 BTB	BCLR1 BSC	BLS REL	COM DIR	COMA INH	COMX INH	COM IX1	COM IX	SWI INH		CPX IMM	CPX DIR	CPX EXT	CPX IX2	CPX IX1	CPX IX	3 0011	
4	BRSET2 BTB	BSET2 BSC	BCC REL	LSR DIR	LSRA INH	LSRX INH	LSR IX1	LSR IX			AND IMM	AND DIR	AND EXT	AND IX2	AND IX1	AND IX	4 0100	
5	BRCLR2 BTB	BCLR2 BSC	BCS REL								BIT IMM	BIT DIR	BIT EXT	BIT IX2	BIT IX1	BIT IX	5 0101	
6	BRSET3 BTB	BSET3 BSC	BNE REL	ROR DIR	RORA INH	RORX INH	ROR IX1	ROR IX			LDA IMM	LDA DIR	LDA EXT	LDA IX2	LDA IX1	LDA IX	6 0110	
7	BRCLR3 BTB	BCLR3 BSC	BEQ REL	ASR DIR	ASRA INH	ASRX INH	ASR IX1	ASR IX	TAX INH		STA DIR	STA EXT	STA IX2	STA IX1	STA IX	7 0111		
8	BRSET4 BTB	BSET4 BSC	BHCC REL	LSL DIR	LSLA INH	LSLX INH	LSL IX1	LSL IX	CLC INH		EOR IMM	EOR DIR	EOR EXT	EOR IX2	EOR IX1	EOR IX	8 1000	
9	BRCLR4 BTB	BCLR4 BSC	BHCS REL	ROL DIR	ROLA INH	ROLX INH	ROL IX1	ROL IX	SEC INH		ADC IMM	ADC DIR	ADC EXT	ADC IX2	ADC IX1	ADC IX	9 1001	
A	BRSET5 BTB	BSET5 BSC	BPL REL	DEC DIR	DECA INH	DECX INH	DEC IX1	DEC IX	CLI INH		ORA IMM	ORA DIR	ORA EXT	ORA IX2	ORA IX1	ORA IX	A 1010	
B	BRCLR5 BTB	BCLR5 BSC	BMI REL						SEI INH		ADD IMM	ADD DIR	ADD EXT	ADD IX2	ADD IX1	ADD IX	B 1011	
C	BRSET6 BTB	BSET6 BSC	BMC REL	INC DIR	INCA INH	INCX INH	INC IX1	INC IX	RSP INH		JMP DIR	JMP EXT	JMP IX2	JMP IX1	JMP IX	C 1100		
D	BRCLR6 BTB	BCLR6 BSC	BMS REL	TST DIR	TSTA INH	TSTX INH	TST IX1	TST IX	NOP INH		BSR REL	JSR DIR	JSR EXT	JSR IX2	JSR IX1	JSR IX	D 1101	
E	BRSET7 BTB	BSET7 BSC	BIL REL						STOP INH		LDX IMM	LDX DIR	LDX EXT	LDX IX2	LDX IX1	LDX IX	E 1110	
F	BRCLR7 BTB	BCLR7 BSC	BIH REL	CLR DIR	CLRA INH	CLRX INH	CLR IX1	CLR IX	WAIT INH	TXA INH	STX DIR	STX EXT	STX IX2	STX IX1	STX IX	F 1111		

Abbreviations for Address Modes

- INH Inherent
- IMM Immediate
- DIR Direct
- EXT Extended
- REL Relative
- BSC Bit Set/Clear
- BTB Bit Test and Branch
- IX Indexed (No Offset)
- IX1 Indexed, 1 Byte (8-Bit) Offset
- IX2 Indexed, 2 Byte (16-Bit) Offset
- CMOS Versions Only

LEGEND



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Indexed, 8-bit Offset — Here the EA is obtained by adding the contents of the byte following the opcode to that of the index register. The operand is therefore located anywhere within the lowest 511 memory locations. For example, this mode of addressing is useful for selecting the m-th element in an n element table. All instructions are two bytes. The contents of the index register (X) is not changed. The contents of (PC + 1) is an unsigned 8-bit integer. One byte offset indexing permits look-up tables to be easily accessed in either RAM or ROM.

$$EA = X + (PC + 1); PC - PC + 2$$

Address Bus High—K; Address Bus Low—X + (PC + 1)
Where: K = The carry from the addition of X + (PC + 1)

Indexed, 16-Bit Offset — In the indexed, 16-bit offset addressing mode the effective address is the sum of the contents of the unsigned 8-bit index register and the two unsigned bytes following the opcode. This addressing mode can be used in a manner similar to indexed 8-bit offset, except that this three byte instruction allows tables to be anywhere in memory (e.g., jump tables in ROM). As with direct and extended, the assembler determines the most efficient form of indexed offset — 8 or 16 bit. The content of the index register is not changed.

$$EA = X + [(PC + 1); (PC + 2)]; PC - PC + 3$$

Address Bus High—(PC + 1) + K;
Address Bus Low—X + (PC + 2)

Where: K = The carry from the addition of X + (PC + 2)

Relative — Relative addressing is only used in branch instructions. In relative addressing the contents of the 8-bit signed byte following the opcode (the offset) is added to the PC if and only if the branch condition is true. Otherwise, control proceeds to the next instruction. The span of relative addressing is limited to the range of - 126 to + 129 bytes from the branch instruction opcode location. The Motorola assembler calculates the proper offset and checks to see if it

is within the span of the branch.

$$EA = PC + 2 + (PC + 1); PC - EA \text{ if branch taken;}$$

$$\text{otherwise } PC - PC + 2$$

Bit Set/Clear — Direct addressing and bit addressing are combined in instructions which set and clear individual memory and I/O bits. In the bit set and clear instructions, the byte is specified as a direct address in the location following the opcode. The first 256 addressable locations are thus accessed. The bit to be modified within that byte is specified with three bits of the opcode. The bit set and clear instructions occupy two bytes, one for the opcode (including the bit number) and the second to address the byte which contains the bit of interest.

$$EA = (PC + 1); PC - PC + 2$$

Address Bus High—0; Address Bus Low—(PC + 1)

Bit Test and Branch — Bit test and branch is a combination of direct addressing, bit addressing and relative addressing. The bit address and condition (set or clear) to be tested is part of the opcode. The address of the byte to be tested is in the single byte immediately following the opcode byte (EA1). The signed relative 8-bit offset is in the third byte (EA2) and is added to the PC if the specified bit is set or clear in the specified memory location. This single three byte instruction allows the program to branch based on the condition of any bit in the first 256 locations of memory.

$$EA1 = (PC + 1)$$

Address Bus High—0; Address Bus Low—(PC + 1)

$$EA2 = PC + 3 + (PC + 2); PC - EA2 \text{ if branch taken;}$$

$$\text{otherwise } PC - PC + 3$$

SYSTEM CONFIGURATION

Figures 20 through 25 show in general terms how the CDP6805E2 bus structure may be utilized. Specified interface details vary with the various peripheral and memory devices employed.

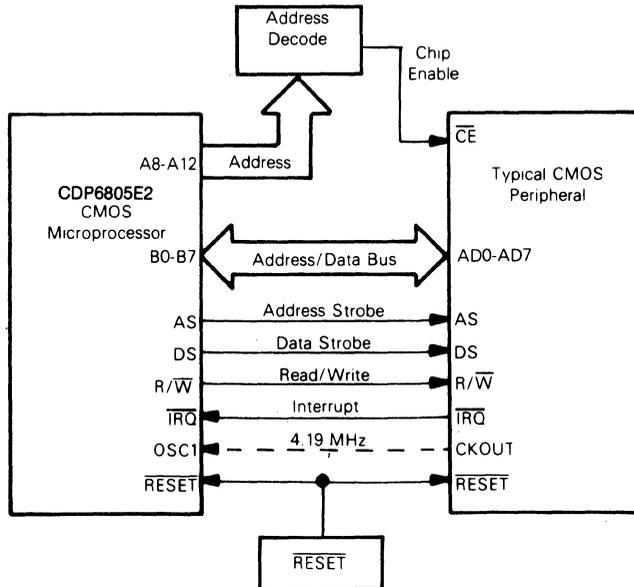


Fig. 20 - Connection to CMOS peripherals.

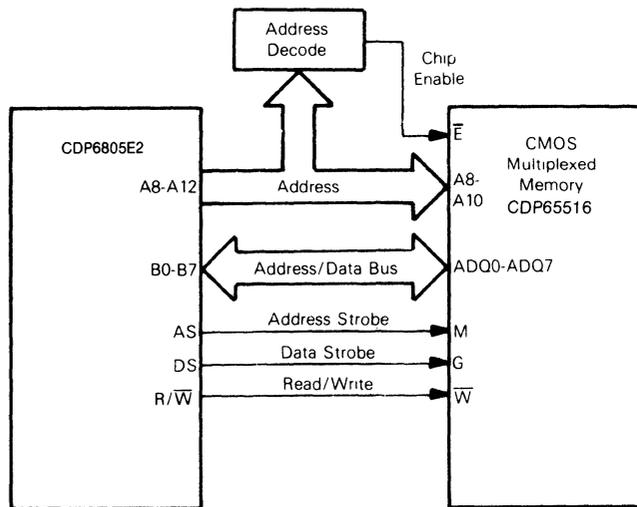
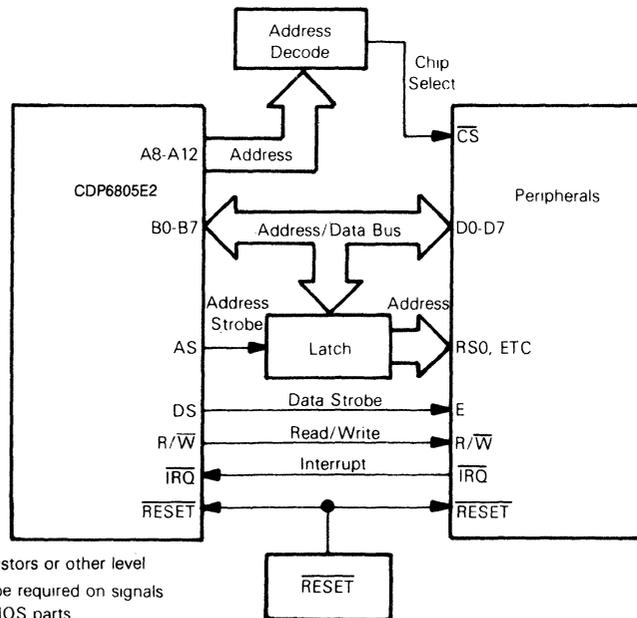


Fig. 21 - Connection to CMOS multiplexed memories.



NOTE: In some cases, pullup resistors or other level shifting techniques may be required on signals going from NMOS to CMOS parts.

Fig. 22 - Connection to peripherals.

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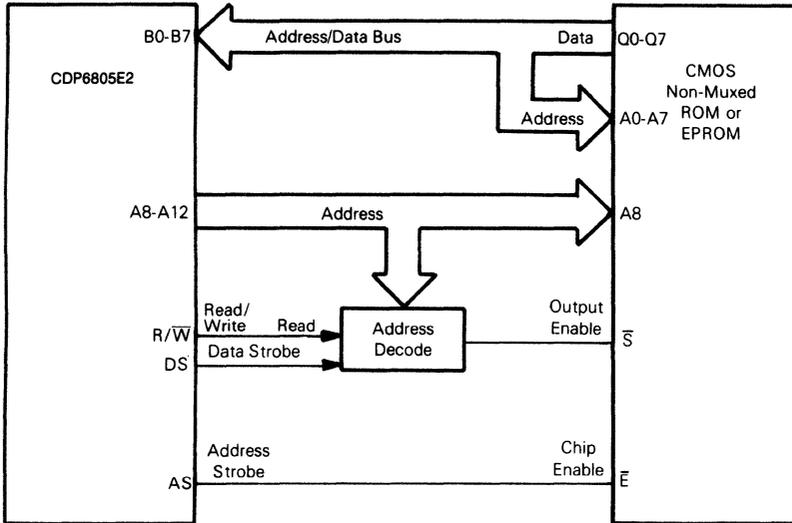


Fig. 23 - Connection to latch non-multiplexed CMOS ROM or EPROM.

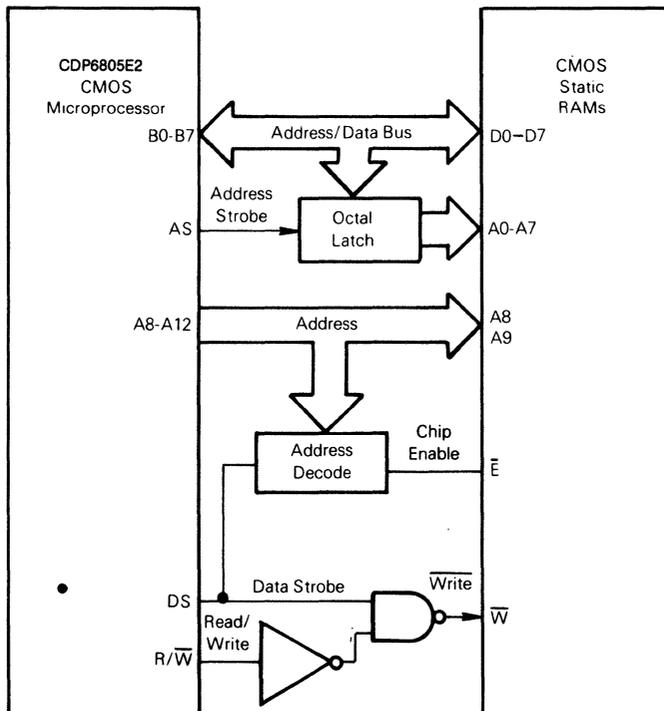


Fig. 24 - Connection to static CMOS RAMs.

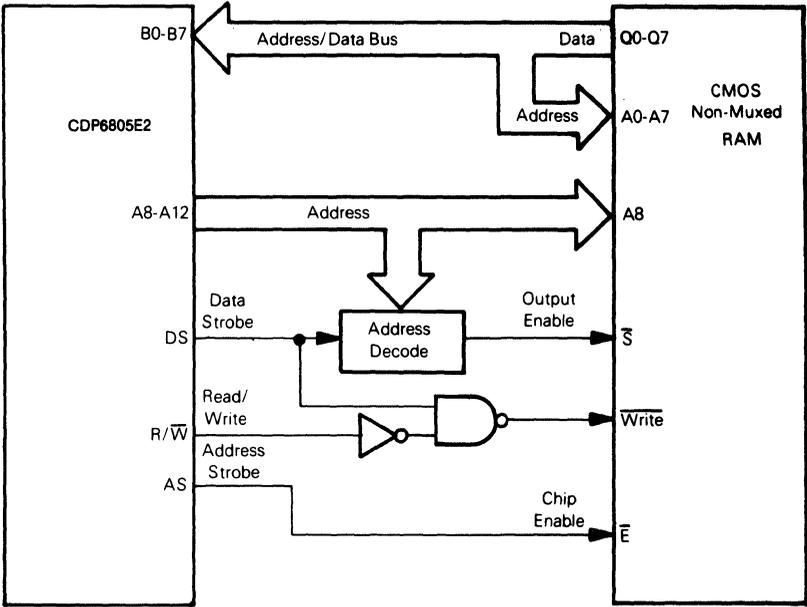


Fig. 25 - Connection to latched non-multiplexed CMOS RAM.

RCA CMOS LSI Products

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Table 11 provides a detailed description of the information present on the Bus, the Read/Write (R/W) pin and the Load Instruction (LI) pin during each cycle for each instruction.

This information is useful in comparing actual with ex-

pected results during debug of both software and hardware as the control program is executed. The information is categorized in groups according to addressing mode and number of cycles per instruction.

TABLE 11 — SUMMARY OF CYCLE BY CYCLE OPERATION

Address Mode Instructions	Cycles	Cycle #	Address Bus	R/W Pin	LI Pin	Data Bus
Inherent						
LSR LSL ASR NEG CLR ROL COM ROR DEC INC TST	3	1 2 3	Op Code Address Op Code Address + 1 Op Code Address + 1	1 1 1	1 0 0	Op Code Op Code Next Instruction Op Code Next Instruction
TAX CLC SEC STOP CLI SEI RSP WAIT NOP TXA	2	1 2	Op Code Address Op Code Address + 1	1 1	1 0	Op Code Op Code Next Instruction
RTS	6	1 2 3 4 5 6	Op Code Address Op Code Address + 1 Stack Pointer Stack Pointer + 1 Stack Pointer + 2 New Op Code Address	1 1 1 1 1 1	1 0 0 0 0 0	Op Code Op Code Next Instruction Irrelevant Data Irrelevant Data Irrelevant Data New Op Code
SWI	10	1 2 3 4 5 6 7 8 9 10	Op Code Address Op Code Address + 1 Stack Pointer Stack Pointer - 1 Stack Pointer - 2 Stack Pointer - 3 Stack Pointer - 4 Vector Address 1FFC (Hex) Vector Address 1FFD (Hex) Interrupt Routine Starting Address	1 1 0 0 0 0 0 1 1 1	1 0 0 0 0 0 0 0 0 0	Op Code Op Code Next Instruction Return Address (LO Byte) Return Address (HI Byte) Contents of Index Register Contents of Accumulator Contents of CC Register Address of Int. Routine (HI Byte) Address of Int. Routine (LO Byte) Interrupt Routine First Opcode
RTI	9	1 2 3 4 5 6 7 8 9	Op Code Address Op Code Address + 1 Stack Pointer Stack Pointer + 1 Stack Pointer + 2 Stack Pointer + 3 Stack Pointer + 4 Stack Pointer + 5 New Op Code Address	1 1 1 1 1 1 1 1 1	1 0 0 0 0 0 0 0 0	Op Code Op Code Next Instruction Irrelevant Data Irrelevant Data Irrelevant Data Irrelevant Data Irrelevant Data Irrelevant Data New Op Code
Immediate						
ADC EOR CPX ADD LDA LDX AND ORA BIT SBC CMB SUB	2	1 2	Op Code Address Op Code Address + 1	1 1	1 0	Op Code Operand Data
Bit Set/Clear						
BSET n BCLR n	5	1 2 3 4 5	Op Code Address Op Code Address + 1 Address of Operand Address of Operand Address of Operand	1 1 1 1 0	1 0 0 0 0	Op Code Address of Operand Operand Data Operand Data Manipulated Data
Bit Test and Branch						
BRSET n BRCLR n	5	1 2 3 4 5	Op Code Address Op Code Address + 1 Address of Operand Op Code Address + 2 Op Code Address + 2	1 1 1 1 1	1 0 0 0 0	Op Code Address of Operand Operand Data Branch Offset Branch Offset
Relative						
BCC BHI BNE BEQ BCS BPL BHCC BLS BIL BMC BRN BHCS BIH BMI BMS BRA	3	1 2 3	Op Code Address Op Code Address + 1 Op Code Address + 1	1 1 1	1 0 0	Op Code Branch Offset Branch Offset
BSR	6	1 2 3 4 5 6	Op Code Address Op Code Address + 1 Op Code Address + 1 Subroutine Starting Address Stack Pointer Stack Pointer - 1	1 1 1 1 0 0	1 0 0 0 0 0	Op Code Branch Offset Branch Offset First Subroutine Op Code Return Address (LO Byte) Return Address (HI Byte)

TABLE 11 — SUMMARY OF CYCLE BY CYCLE OPERATION (CONTINUED)

Address Mode Instructions	Cycles	Cycles #	Address Bus	R/W Pin	LI Pin	Data Bus
Direct						
JMP	2	1 2	Op Code Address Op Code Address + 1	1 1	1 0	Op Code Jump Address
ADC EOR CPX ADD LDA LDX AND ORA BIT SBC CMP SUB	3	1 2 3	Op Code Address Op Code Address + 1 Address of Operand	1 1 1	1 0 0	Op Code Address of Operand Operand Data
TST	4	1 2 3 4	Op Code Address Op Code Address + 1 Address of Operand Op Code Address + 2	1 1 1 1	1 0 0 0	Op Code Address of Operand Operand Data Op Code Next Instruction
STA STX	4	1 2 3 4	Op Code Address Op Code Address + 1 Op Code Address + 1 Address of Operand	1 1 1 0	1 0 0 0	Op Code Address of Operand Address of Operand Operand Data
LSL LSR DEC ASR NEG INC CLR ROL COM ROR	5	1 2 3 4 5	Op Code Address Op Code Address + 1 Operand Address Operand Address Operand Address	1 1 1 1 0	1 0 0 0 0	Op Code Address of Operand Current Operand Data Current Operand Data New Operand Data
JSR	5	1 2 3 4 5	Op Code Address Op Code Address + 1 Subroutine Starting Address Stack Pointer Stack Pointer - 1	1 1 1 0 0	1 0 0 0 0	Op Code Subroutine Address (LO Byte) 1st Subroutine Op Code Return Address (LO Byte) Return Address (HI Byte)
Extended						
JMP	3	1 2 3	Op Code Address Op Code Address + 1 Op Code Address + 2	1 1 1	1 0 0	Op Code Jump Address (HI Byte) Jump Address (LO Byte)
ADC BIT ORA ADD CMP LDX AND EOR SBC CPX LDA SUB	4	1 2 3 4	Op Code Address Op Code Address + 1 Op Code Address + 2 Address of Operand	1 1 1 1	1 0 0 0	Op Code Address Operand (HI Byte) Address Operand (LO Byte) Operand Data
STA STX	5	1 2 3 4 5	Op Code Address Op Code Address + 1 Op Code Address + 2 Op Code Address + 2 Address of Operand	1 1 1 1 0	1 0 0 0 0	Op Code Address of Operand (HI Byte) Address of Operand (LO Byte) Address of Operand (LO Byte) Operand Data
JSR	6	1 2 3 4 5 6	Op Code Address Op Code Address + 1 Op Code Address + 2 Subroutine Starting Address Stack Pointer Stack Pointer - 1	1 1 1 1 0 0	1 0 0 0 0 0	Op Code Address of Subroutine (HI Byte) Address of Subroutine (LO Byte) 1st Subroutine Op Code Return Address (LO Byte) Return Address (HI Byte)
Indexed, No-Offset						
JMP	2	1 2	Op Code Address Op Code Address + 1	1 1	1 0	Op Code Op Code Next Instruction
ADC EOR CPX ADD LDA LDX AND ORA BIT SBC CMP SUB	3	1 2 3	Op Code Address Op Code Address + 1 Index Register	1 1 1	1 0 0	Op Code Op Code Next Instruction Operand Data
TST	4	1 2 3 4	Op Code Address Op Code Address + 1 Index Register Op Code Address + 1	1 1 1 1	1 0 0 0	Op Code Op Code Next Instruction Operand Data Op Code Next Instruction
STA STX	4	1 2 3 4	Op Code Address Op Code Address + 1 Op Code Address + 1 Index Register	1 1 1 0	1 0 0 0	Op Code Op Code Next Instruction Op Code Next Instruction Operand Data
LSL LSR DEC ASR NEG INC CLR ROL COM ROR	5	1 2 3 4 5	Op Code Address Op Code Address + 1 Index Register Index Register Index Register	1 1 1 1 0	1 0 0 0 0	Op Code Op Code Next Instruction Current Operand Data Current Operand Data New Operand Data
JSR	5	1 2 3 4 5	Op Code Address Op Code Address + 1 Index Register Stack Pointer Stack Pointer - 1	1 1 1 0 0	1 0 0 0 0	Op Code Op Code Next Instruction 1st Subroutine Op Code Return Address (LO Byte) Return Address (HI Byte)

TABLE 11 — SUMMARY OF CYCLE BY CYCLE OPERATION (CONTINUED)

Address Mode Instructions	Cycles	Cycles #	Address Bus	R/W Pin	LI Pin	Data Bus
Indexed 8-Bit Offset						
JMP	3	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Offset
		3	Op Code Address + 1	1	0	Offset
ADC EOR CPX ADD LDA LDX AND ORA CMP SUB BIT SBC	4	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Offset
		3	Op Code Address + 1	1	0	Offset
		4	Index Register + Offset	1	0	Operand Data
STA STX	5	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Offset
		3	Op Code Address + 1	1	0	Offset
		4	Op Code Address + 1	1	0	Offset
		5	Index Register + Offset	0	0	Operand Data
TST	5	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Offset
		3	Op Code Address + 1	1	0	Offset
		4	Index Register + Offset	1	0	Operand Data
		5	Op Code Address + 2	1	0	Op Code Next Instruction
LSL LSR ASR NEG CLR ROL COM ROR DEC INC	6	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Offset
		3	Op Code Address + 1	1	0	Offset
		4	Index Register + Offset	1	0	Current Operand Data
		5	Index Register + Offset	1	0	Current Operand Data
		6	Index Register + Offset	0	0	New Operand Data
JSR	6	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Offset
		3	Op Code Address + 1	1	0	Offset
		4	Index Register + Offset	1	0	1st Subroutine Op Code
		5	Stack Pointer	0	0	Return Address LO Byte
		6	Stack Pointer - 1	0	0	Return Address HI Byte
Indexed, 16-Bit Offset						
JMP	4	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Offset (HI Byte)
		3	Op Code Address + 2	1	0	Offset (LO Byte)
		4	Op Code Address + 2	1	0	Offset (LO Byte)
ADC CMP SUB ADD EOR SBC AND ORA CPX LDA BIT LDX	5	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Offset (HI Byte)
		3	Op Code Address + 2	1	0	Offset (LO Byte)
		4	Op Code Address + 2	1	0	Offset (LO Byte)
		5	Index Register + Offset	1	0	Operand Data
STA STX	6	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Offset (HI Byte)
		3	Op Code Address + 2	1	0	Offset (LO Byte)
		4	Op Code Address + 2	1	0	Offset (LO Byte)
		5	Op Code Address + 2	1	0	Offset (LO Byte)
		6	Index Register + Offset	0	0	Operand Data
JSR	7	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Offset (HI Byte)
		3	Op Code Address + 2	1	0	Offset (LO Byte)
		4	Op Code Address + 2	1	0	Offset (LO Byte)
		5	Index Register + Offset	1	0	1st Subroutine Op Code
		6	Stack Pointer	0	0	Return Address (LO Byte)
		7	Stack Pointer - 1	0	0	Return Address (HO Byte)

TABLE 11 — SUMMARY OF CYCLE BY CYCLE OPERATION (CONTINUED)

Instructions	Cycles	Cycles #	Address Bus	RESET Pin	R/W Pin	LI Pin	Data Bus
Other Functions							
Hardware RESET	5		\$1FFE	0	1	0	Irrelevant Data
		1	\$1FFE	0	1	0	Irrelevant Data
		2	\$1FFE	1	1	0	Irrelevant Data
		3	\$1FFE	1	1	0	Vector High
		4	\$1FFE	1	1	0	Vector Low
		5	Reset Vector	1	1	0	Op Code
Power on Reset	1922	1	\$1FFE	1	1	0	Irrelevant Data
		•	•	•	•	•	•
		•	•	•	•	•	•
		•	•	•	•	•	•
		•	•	•	•	•	•
		1919	\$1FFE	1	1	0	Irrelevant Data
		1920	\$1FFE	1	1	0	Vector High
		1921	\$1FFF	1	1	0	Vector Low
		1922	Reset Vector	1	1	0	Op Code
Instruction	Cycles	Cycles #	Address Bus	IRQ Pin	R/W Pin	LI Pin	Data Bus
IRQ Interrupt (Timer Vector \$1FF8, \$1FF9)	10		Last Cycle of Previous Instruction	0	X	0	X
		1	Next Op Code Address	0	1	0	Irrelevant Data
		2	Next Op Code Address	X	1	0	Irrelevant Data
		3	SP	X	0	0	Return Address (LO Byte)
		4	SP - 1	X	0	0	Return Address (HI Byte)
		5	SP - 2	X	0	0	Contents Index Reg
		6	SP - 3	X	0	0	Contents Accumulator
		7	SP - 4	X	0	0	Contents CC Register
		8	\$1FFA	X	1	0	Vector High
		9	\$1FFB	X	1	0	Vector Low
		10	IRQ Vector	X	1	0	Int Routine First

APPENDIX

CDP6805E2 INTERRUPT CLARIFICATION

Under certain circumstances, the CDP6805E2 (BP4xxx & AW9xxx) 8-bit Microprocessor Unit $\overline{\text{IRQ}}$ interrupt does not conform to the operation described in this Advanced Information Sheet (ADI-850R1).

- The level sensitive $\overline{\text{IRQ}}$ mode, which is by far the most frequently used, is **FULLY OPERATIONAL**; thus, most CDP6805E2 applications are unaffected. However, the edge-triggered $\overline{\text{IRQ}}$ interrupt mode **MIGHT NOT BE SERVICED** under certain programming circumstances; therefore, it is recommended that the edge-triggered mode not be used.
- An interrupt-vector address **CAN BE** improperly generated in some circumstances. There is a possibility that when an external interrupt ($\overline{\text{IRQ}}$) and timer interrupt occur during the Wait mode (following a Wait instruction), address locations \$1FF2 and \$1FF3 are selected instead of vector locations \$1FF6 and \$1FF7. There are three specific examples listed below; two of

these require no action and the third has a recommended solution.

- Those not using the Wait mode need not take any action.
- If the Wait mode is used without external interrupt ($\overline{\text{IRQ}}$ pin held high), no precautions are required.
- When $\overline{\text{IRQ}}$ can be active (low) during the Wait mode, the vector in locations \$1FF6 and \$1FF7 (the Wait mode Timer Interrupt Vector) should be duplicated in \$1FF2 and \$1FF3. In this way the circumstances that caused selection of the second vector do not disturb normal program execution.

On future CDP6805E2 parts, no special actions will be necessary. If you have questions, contact your Motorola distributor or Motorola sales office, or contact Motorola Microprocessor Applications Engineering in Austin, Texas.

CDP6805 FAMILY

	CDP6805E2	CDP6805F2	CDP6805G2
Technology	CMOS	CMOS	CMOS
Number of Pins	40	28	40
On-Chip RAM (Bytes)	112	64	112
On-Chip User ROM (Bytes)	None	1K	2K
External Bus	Yes	None	None
Bidirectional I/O Lines	16	16	32
Unidirectional I/O Lines	None	4 Inputs	None
Other I/O Features	Timer	Timer	Timer
External Interrupt Inputs	1	1	1
EPROM Version	None	None	None
STOP and WAIT	Yes	Yes	Yes

OPERATING AND HANDLING CONSIDERATIONS

1. Handling

All inputs and outputs of RCA CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in ICAN-6525, "Guide to Better Handling and Operation of CMOS Integrated Circuits."

2. Operating

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause $V_{DD}-V_{SS}$ to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS} . Input currents must not exceed 10 mA even when the power supply is off.

Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS} , whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} or V_{SS} may damage CMOS devices by exceeding the maximum device dissipation.

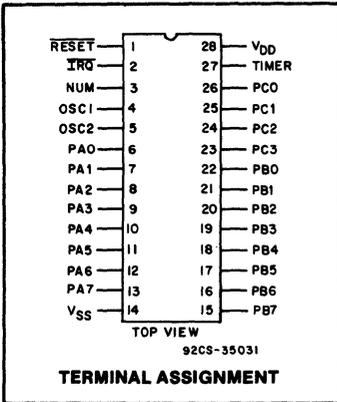
Ordering Information

RCA Microprocessor device packages are identified by letters indicated in the following chart. When ordering a Microprocessor device, it is important that the appropriate suffix letter be affixed to the type number of the device.

Package	Suffix Letter
Dual-In-Line Side-Brazed Ceramic	D
Dual-In-Line Plastic	E

For example, a CDP6805E2 in a dual-in-line plastic package will be identified as the CDP6805E2E.

CMOS High-Performance Silicon-Gate 8-Bit Microcomputer



Features:

- Typical full speed operating power of 10 mW at 5 V
- Typical WAIT mode power of 3 mW
- Typical STOP mode power of 25 μ W
- Fully static operation
- 64 bytes of on-chip RAM
- 1089 bytes of on-chip ROM
- 16 bidirectional I/O lines
- 4 input-only lines
- Internal 8-bit timer with software programmable 7-bit prescaler
- External timer input
- External and timer interrupts
- Self-check mode
- Master reset and power-on reset

- Single 3 to 6 volt supply
- On-chip oscillator
- 1 μ s cycle time
- 28-pin dual-in-line package

Software Features:

- Similar to the MC6800
- Efficient use of program space
- Versatile interrupt handling
- True bit manipulation
- Addressing modes with indexed addressing for tables
- Efficient instruction set
- Memory-mapped I/O
- User-callable self-check routines
- Two power-saving standby modes

The CDP6805F2 Microcomputer Unit (MCU) belongs to the CDP6805 Family of Microcomputers. This 8-bit MCU contains on-chip oscillator CPU, RAM, ROM, I/O, and Timer. The fully static design allows operation at frequencies down to DC, further reducing its already low-power

consumption. It is a low-power processor designed for low-end to mid-range applications in the consumer, automotive, industrial, and communications markets where very low power consumption constitutes an important factor.

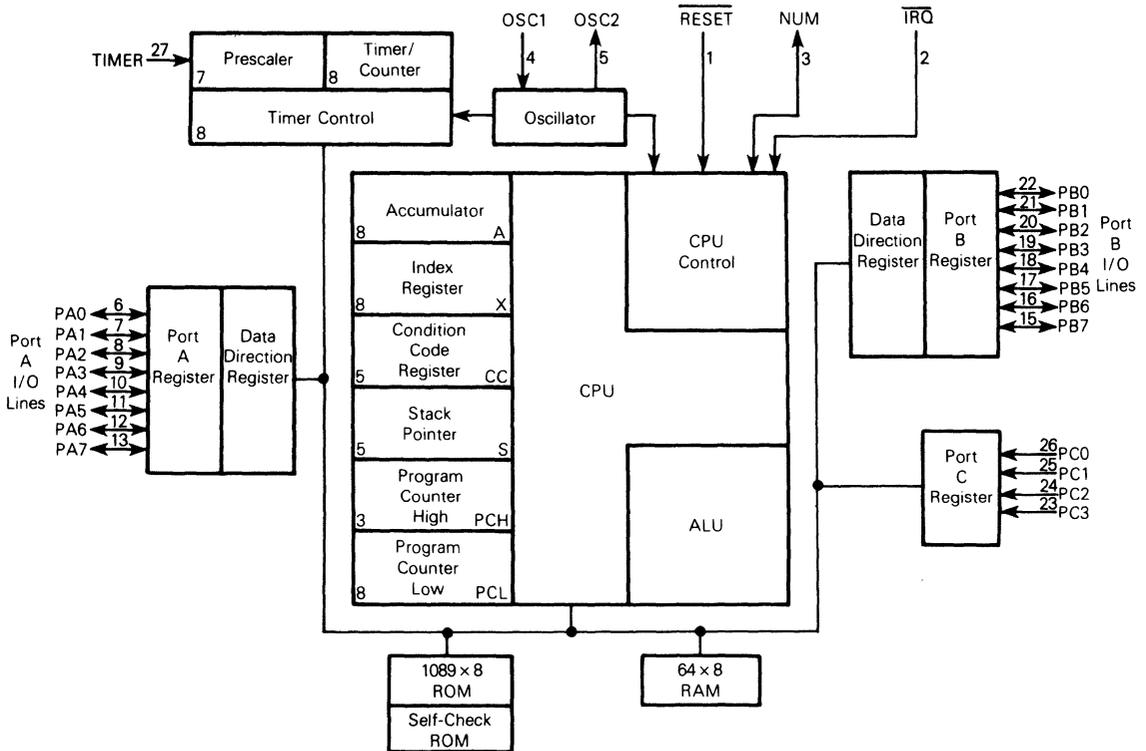


Fig. 1 - CDP6805F2 CMOS microcomputer block diagram.

RCA CMOS LSI Products
CDP6805F2

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Ratings	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.3 to +8	V
All Input Voltages Except OSC1	V_{in}	$V_{SS} - 0.5$ to $V_{DD} + 0.5$	V
Current Drain per Pin Excluding V_{DD} and V_{SS}	I	10	mA
Operating Temperature Range CDP6805F2 CDP6805F2C	T_A	T_L to T_H 0 to 70 -40 to +85	$^{\circ}C$
Storage Temperature Range	T_{stg}	-55 to +150	$^{\circ}C$

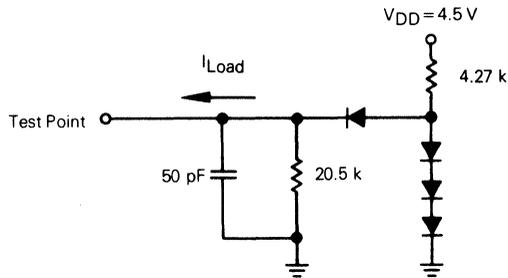


Fig. 2 - Equivalent test load.

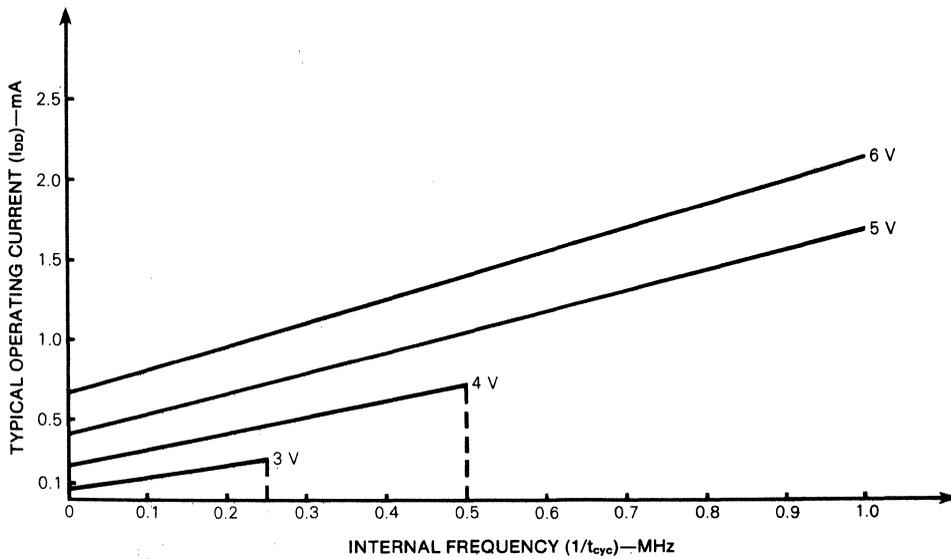


Fig. 3 - Typical operating current vs. internal frequency.

DC ELECTRICAL CHARACTERISTICS ($V_{DD}=5$ Vdc $\pm 10\%$, $V_{SS}=0$ Vdc, $T_A=T_L$ to T_H , unless otherwise noted) (See Note 1)

Characteristics	Symbol	Min	Max	Unit
Output Voltage, $I_{Load} \leq 10.0 \mu A$	V_{OL} V_{OH}	— $V_{DD}-0.1$	0.1 —	V
Output High Voltage ($I_{Load} = -200 \mu A$) PA0-PA7, PB0-PB7	V_{OH}	4.1	—	V
Output Low Voltage, ($I_{Load} = 800 \mu A$) PA0-PA7, PB0-PB7	V_{OL}	—	0.4	V
Input High Voltage Ports PA0-PA7, PB0-PB7, PC0-PC3 TIMER, \overline{IRQ} , RESET OSC1	V_{IH}	$V_{DD}-2$ $V_{DD}-0.8$ $V_{DD}-1.5$	V_{DD} V_{DD} V_{DD}	V
Input Low Voltage, All Inputs	V_{IL}	V_{SS}	0.8	V
Total Supply Current ($C_L = 50$ pF on Ports, No dc Loads, $t_{cyc} = 1 \mu s$) RUN (Measured During Self-Check, $V_{IL} = 0.2$ V, $V_{IH} = V_{DD} - 0.2$ V) WAIT (See Note 2) STOP (See Note 2)	I_{DD}	— — —	5 2 200	mA mA μA
I/O Ports Input Leakage — PA0-PA7, PB0-PB7	I_{IL}	—	± 10	μA
Input Current — RESET, \overline{IRQ} , TIMER, OSC1, PC0-PC3	I_{in}	—	± 1	μA
Output Capacitance — Ports A and B	C_{out}	—	12	pF
Input Capacitance — RESET, \overline{IRQ} , TIMER, OSC1, PC0-PC3	C_{in}	—	8	pF

NOTES:

- Electrical Characteristics for $V_{DD} = 3$ V available soon.
- Test Conditions for I_{DD} are as follows:
All ports programmed as inputs
 $V_{IL} = 0.2$ V (PA0-PA7, PB0-PB7, PC0-PC3)
 $V_{IH} = V_{DD} - 0.2$ V for RESET, \overline{IRQ} , TIMER
OSC1 input is a square wave from 0.2 V to $V_{DD} - 0.2$ V
OSC2 output load = 20 pF (WAIT I_{DD} is affected linearly by the OSC2 capacitance)

TABLE 1 — CONTROL TIMING CHARACTERISTICS ($V_{DD}=5$ Vdc $\pm 10\%$, $V_{SS}=0$, $T_A=T_L$ to T_H , $f_{osc}=4$ MHz, $t_{cyc}=1 \mu s$)

Characteristics	Symbol	Min	Max	Unit
Crystal Oscillator Startup Time (See Figure 5)	t_{OXOV}	—	100	ms
Stop Recovery Startup Time — Crystal Oscillator (See Figure 6)	t_{ILCH}	—	100	ms
Timer Pulse Width (See Figure 4)	t_{TH}, t_{TL}	0.5	—	t_{cyc}
Reset Pulse Width (See Figure 5)	t_{RL}	1.5	—	t_{cyc}
Timer Period (See Figure 4)	t_{TLTL}	1	—	t_{cyc}
Interrupt Pulse Width (See Figure 15)	t_{ILIH}	1	—	t_{cyc}
Interrupt Pulse Period (See Figure 15)	t_{LIL}	*	—	t_{cyc}
OSC1 Pulse Width (See Figure 7)	t_{OH}, t_{OL}	100	—	ns
Cycle Time	t_{cyc}	1000	—	ns
Frequency of Operation Crystal External Clock	f_{osc}	— dc	4 4	MHz

*The minimum period, t_{LIL} , should not be less than the number of t_{cyc} cycles it takes to execute the interrupt service routines plus 20 t_{cyc} cycles.

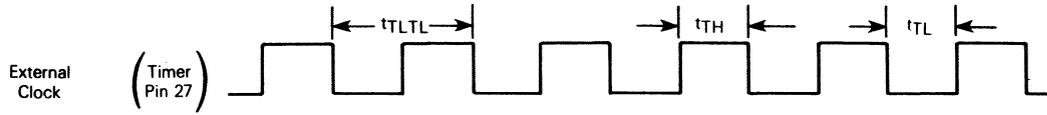
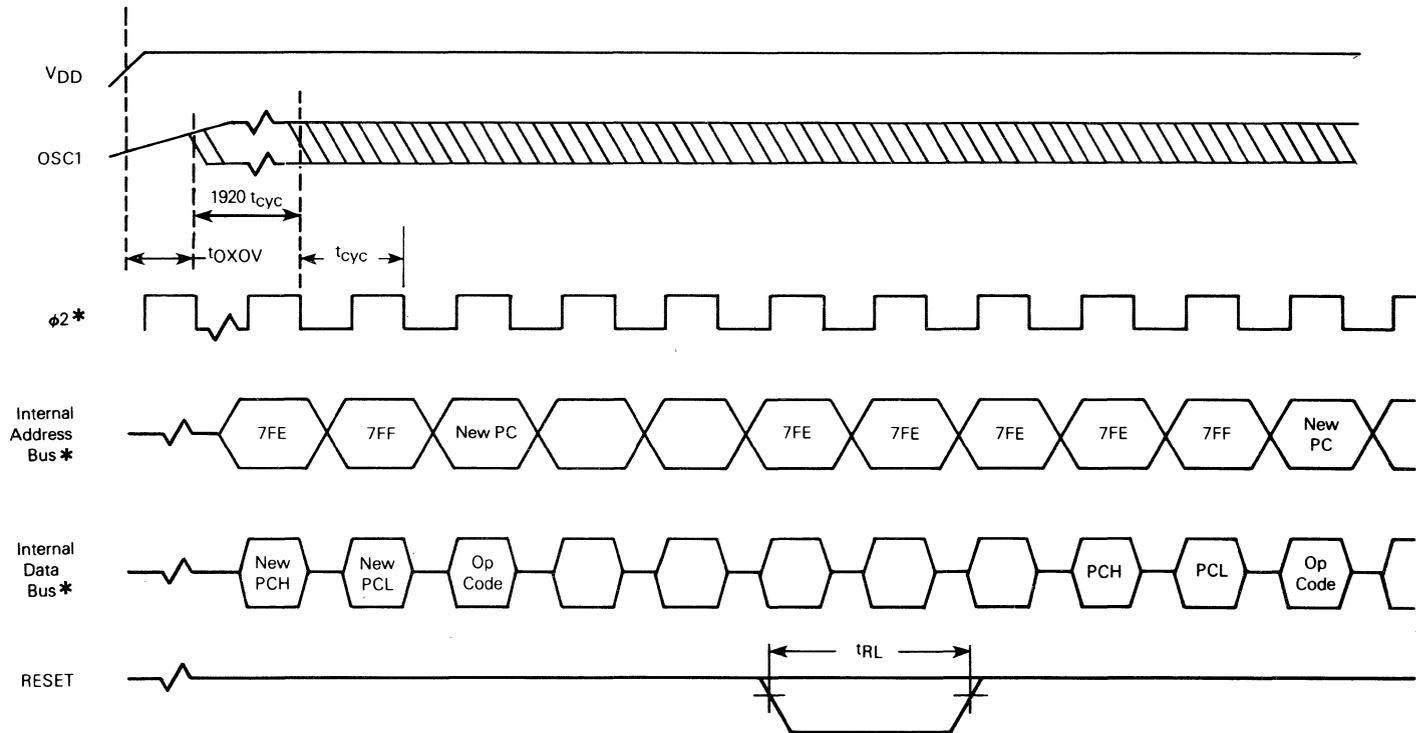
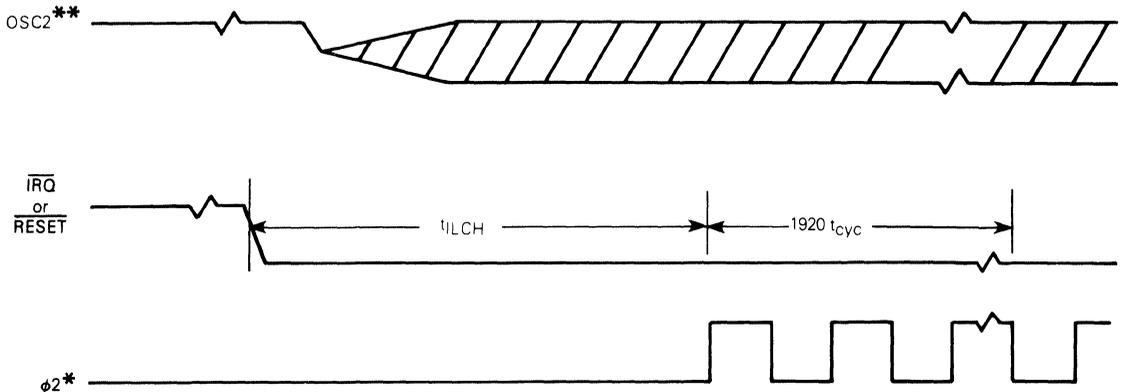


Fig. 4 - Timer relationships.



* Internal timing signal not available externally.

Fig. 5 - Power-on RESET and \overline{RESET} .



* Internal timing signals not available externally.

** Represents the internal gating of the OSC1 input pin.

Fig. 6 – Stop recovery.

FUNCTIONAL PIN DESCRIPTION

VDD and VSS

Power is supplied to the MCU using these two pins. VDD is power and VSS is ground.

IRQ (MASKABLE INTERRUPT REQUEST)

IRQ is photomask option selectable with the choice of interrupt sensitivity being both level and negative edge or negative edge only. The MCU completes the current instruction before it responds to the request. If IRQ is low and the interrupt mask bit (I bit) in the condition code register is clear, the MCU begins an interrupt sequence at the end of the current instruction.

If the photomask option is selected to include level sensitivity, then the IRQ input requires an external resistor to VDD for "wire-OR" operation. See the Interrupt section for more detail.

RESET

The RESET input is not required for start-up but can be used to reset the MCU's internal state and provide an orderly software start-up procedure. Refer to the Resets section for a detailed description.

TIMER

The TIMER input may be used as an external clock for the on-chip timer. Refer to the Timer section for a detailed description.

NUM (NON-USER MODE)

This pin is intended for use in self-check only. User applications should leave this pin connected to ground through a 10 kilohm resistor.

OSC1, OSC2

The CDP6805F2 can be configured to accept either a crystal input or an RC network. Additionally, the internal clocks can be derived from either a divide-by-two or divide-by-four of the external frequency (f_{OSC}). Both of these options are photomask selectable.

RC — If the RC oscillator option is selected, then a resistor is connected to the oscillator pins as shown in Figure 7(b). The relationship between R and f_{OSC} is shown in Figure 8.

CRYSTAL — The circuit shown in Figure 7(a) is recommended when using a crystal. The internal oscillator is designed to interface with an AT-cut parallel resonant quartz crystal resonator in the frequency range specified for f_{OSC} in the electrical characteristics table. Using an external CMOS oscillator is suggested when crystals outside the specified ranges are to be used. The crystal and components should be mounted as close as possible to the input pins to minimize output distortion and start-up stabilization time. Crystal frequency limits are also affected by VDD. Refer to Table 1, Control Timing Characteristics, for limits.

EXTERNAL CLOCK — An external clock should be applied to the OSC1 input with the OSC2 input not connected, as shown in Figure 7(c). An external clock may be used with either the RC or crystal oscillator mask option. tOXOV or tLCH do not apply when using an external clock input.

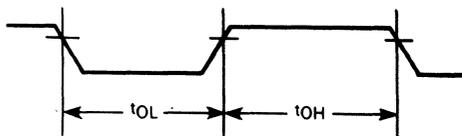
PA0-PA7

These eight I/O lines comprise Port A. The state of any pin is software programmable. Refer to the Input/Output Programming section for a detailed description.

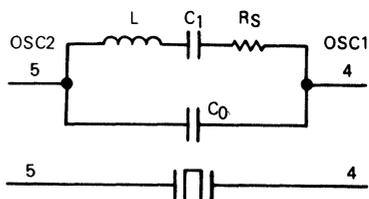
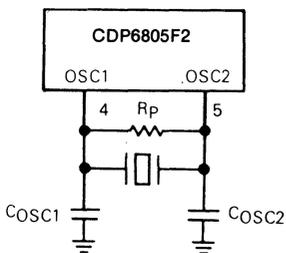
Crystal Parameters

	1 MHz	4 MHz	Units
R _S MAX	400	75	Ω
C ₀	5	7	pF
C ₁	0.008	0.012	μF
C _{OSC1}	15-40	15-30	pF
C _{OSC2}	15-30	15-25	pF
R _p	10	10	MΩ
Q	30 k	40 k	—

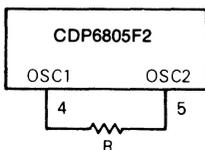
Oscillator Waveform



(a) Crystal Oscillator Connections and Equivalent Crystal Circuit



(b) RC Oscillator Connection



(c) External Clock Source Connections

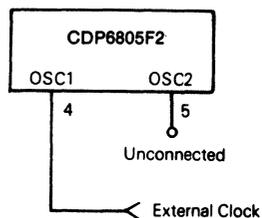


Fig. 7 - Oscillator connections.

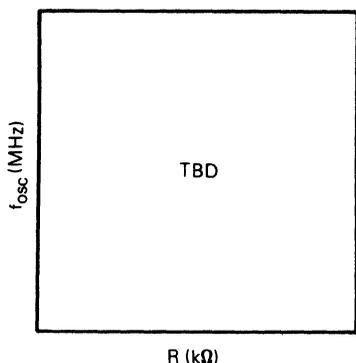


Fig. 8 - Frequency vs. resistance for RC oscillator option only.

PB0-PB7

These eight lines comprise Port B. The state of any pin is software programmable. Refer to the Input/Output Programming section for a detailed description.

PC0-PC3

These four lines comprise Port C, a fixed input port. When Port C is read, the four most-significant bits on the data bus are "1s". There is no data direction register associated with Port C.

INPUT/OUTPUT PROGRAMMING

Any Port A or B pin may be software programmed as an input or output by the state of the corresponding bit in the port data direction register (DDR). A pin is configured as an output if its corresponding DDR bit is set to a logic "1". A pin is configured as an input if its corresponding DDR bit is cleared to a logic "0". At reset, all DDRs are cleared, which configures all port pins as inputs. A port pin configured as an output will output the data in the corresponding bit of its port data latch. Refer to Figure 9 and Table 2.

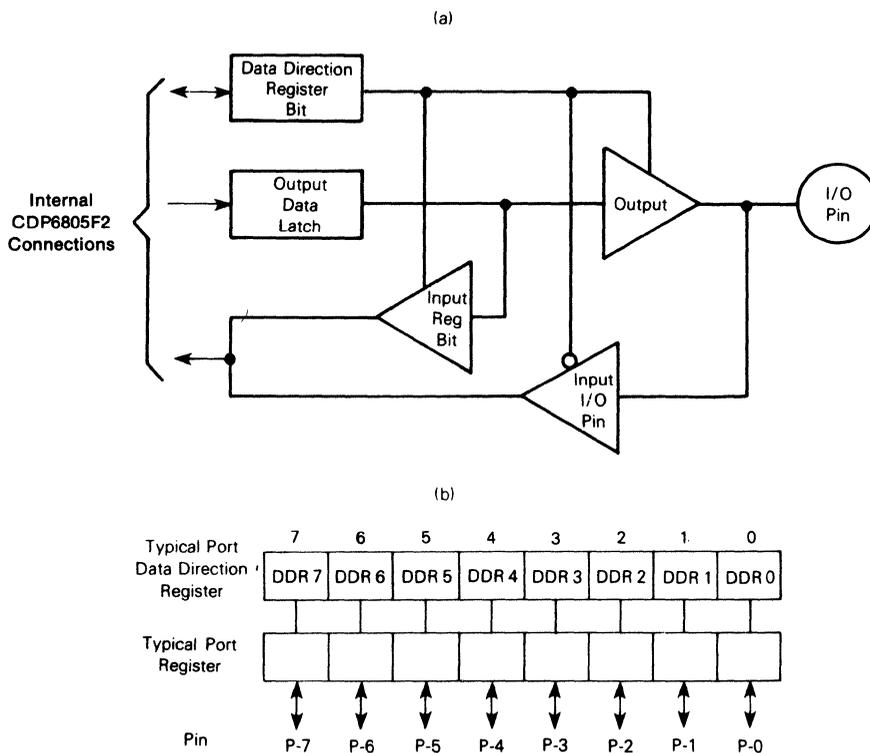


Fig. 9 - Typical I/O port circuitry.

TABLE 2 - I/O PIN FUNCTIONS

R/ \bar{W}	DDR	I/O Pin Function
0	0	The I/O pin is in input mode. Data is written into the output data latch.
0	1	Data is written into the output data latch and output to the I/O pin.
1	0	The state of the I/O pin is read.
1	1	The I/O pin is in an output mode. The output data latch is read.

SELF-CHECK

The CDP6805F2 self-check is performed using the circuit in Figure 10. Self-check is initiated by tying NUM and TIMER pins to a logic "1" then executing a reset. After reset, the following five tests are executed automatically:

- I/O – Functionally Exercise Ports A, B, C
- RAM – Walking Bit Test
- ROM – Exclusive OR with ODD "1s" Parity Result
- Timer – Functionally Exercise Timer
- Interrupts – Functionally Exercise External and Timer Interrupts

Self-check results are shown in Table 3. The following subroutines are available to user programs and do not require any external hardware.

TABLE 3 – SELF-CHECK RESULTS

PB3	PB2	PB1	PB0	Remarks
1	0	1	1	Bad Timer
1	1	0	0	Bad RAM
1	1	0	1	Bad ROM
1	1	1	0	Bad Interrupt or Request Flag
All Cycling				Good Part
All Others				Bad Part

RAM SELF-CHECK SUBROUTINE

Returns with the Z bit clear if any error is detected; otherwise, the Z bit is set.

The RAM test must be called with the stack pointer at \$7F and the accumulator zeroed. When run, the test checks every RAM cell except for \$7F and \$7E which are assumed to contain the return address.

A and X are modified. All RAM locations except the top 2 are modified. (Enter at location \$78B.)

ROM CHECKSUM SUBROUTINE

Returns with Z bit cleared if any error was found; otherwise Z = 1, X = 0 on return, and A is zero if the test passed. RAM locations \$40-\$43 are overwritten. (Enter at location \$7A4.)

TIMER TEST SUBROUTINE

Return with Z bit cleared if any error was found; otherwise Z = 1.

This routine runs a simple test on the timer. In order to work correctly as a user subroutine, the internal clock must be the clocking source and interrupts must be disabled. Also, on exit, the clock will be running and the interrupt mask will not be set, so the caller must protect himself from interrupts if necessary.

A and X register contents are lost; this routine counts how many times the clock counts in 128 cycles. The number of counts should be a power of two since the prescaler is a power of two. If not, the timer probably is not counting correctly. The routine also detects if the timer is running at all. (Enter at location \$7BE.)

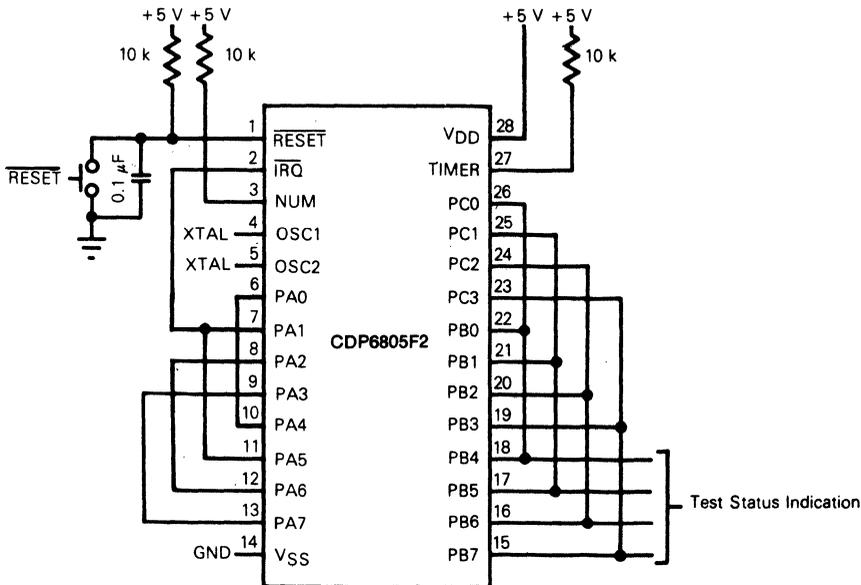


Fig. 10 – Self-check pinout configuration.

MEMORY

The CDP6805F2 has a total address space of 2048 bytes of memory and I/O registers. The address space is shown in Figure 11.

The first 128 bytes of memory (first half of page zero) is comprised of the I/O port locations, timer locations, and 64 bytes of RAM. The next 1079 bytes comprise the user ROM. The 10 highest address bytes contain the reset and interrupt vectors.

The stack pointer is used to address data stored on the stack. Data is stored on the stack during interrupts and subroutine calls. At power-up, the stack pointer is set to \$7F and it is decremented as data is pushed on the stack. When data is removed from the stack, the stack pointer is incremented. A maximum of 32 bytes of RAM are available for stack usage. Since most programs use only a small part of the allocated stack locations for interrupts and/or subroutine stacking purposes, the unused bytes are available for program data storage.

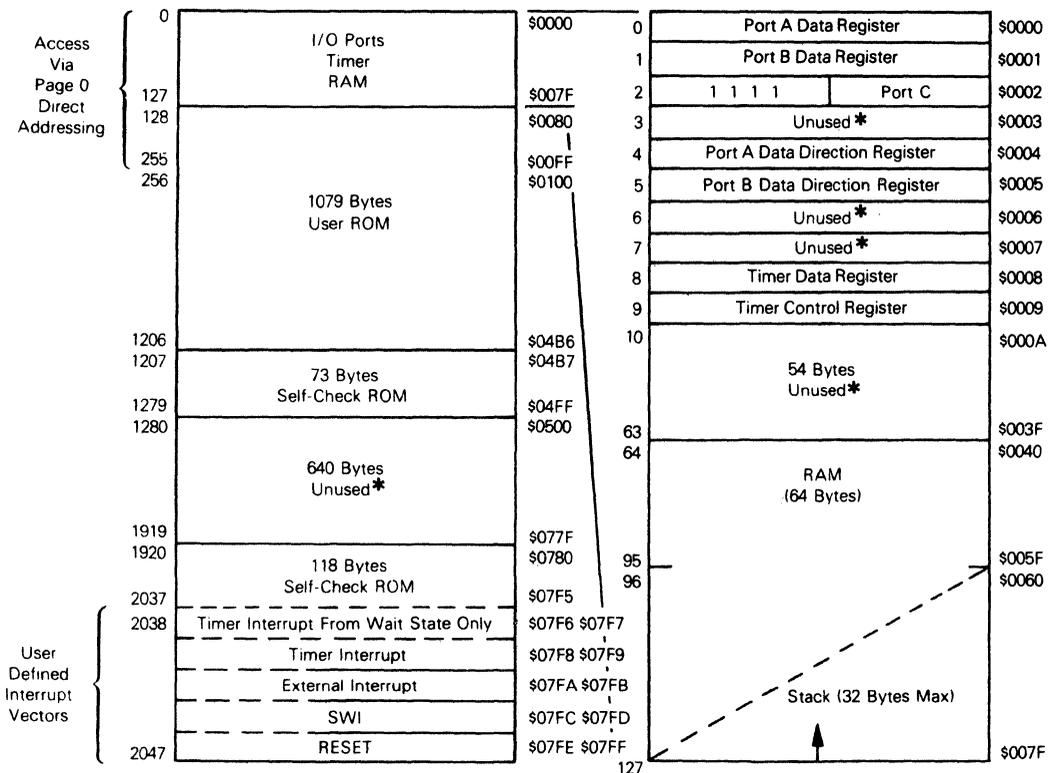


Fig. 11 - Address map.

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CDP6805F2

REGISTERS

The CDP6805F2 contains five registers as shown in the programming model (Figure 12). The interrupt stacking order is shown in Figure 13.

ACCUMULATOR (A)

This accumulator is an 8-bit general purpose register used to hold operands and results of the arithmetic calculations and data manipulations.

INDEX REGISTER (X)

The X register is an 8-bit register which is used during the indexed modes of addressing. It provides the 8-bit operand which is used to create an effective address. The index register is also used for data manipulations with the read-modify-write type of instructions and as a temporary storage register when not performing addressing operations.

PROGRAM COUNTER (PC)

The program counter is an 11-bit register that contains the address of the next instruction to be executed by the processor.

STACK POINTER (SP)

The stack pointer is an 11-bit register containing the address of the next free location on the stack. When accessing memory, the six most-significant bits are appended to the five least-significant register bits to produce an address within the range of \$7F to \$60. The stack area of RAM is used to store the return address on subroutine calls and the machine state during interrupts. During external or power-on reset, and during a "reset stack pointer" instruction, the stack pointer is set to its upper limit (\$7F). Nested interrupts and/or subroutines may use up to 32 (decimal) locations beyond which the stack pointer "wraps around" and points to its upper limit thereby losing the previously stored information. A subroutine call occupies two RAM bytes on the stack, while an interrupt uses five bytes.

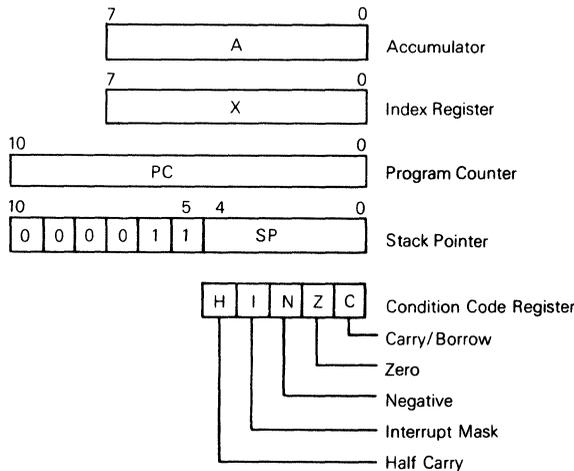
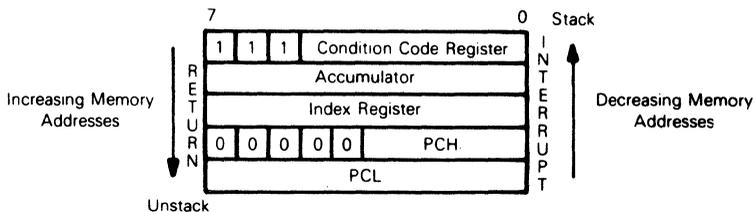


Fig. 12 - Programming model.



NOTE: Since the Stack Pointer decrements during pushes, the PCL is stacked first, followed by PCH, etc. Pulling from the stack is in the reverse order.

Fig. 13 - Stacking order.

CONDITION CODE REGISTER (CC)

The condition code register is a 5-bit register which indicates the results of the instruction just executed. These bits can be individually tested by a program and specific action taken as a result of their state. Each bit is explained in the following paragraphs.

HALF CARRY BIT (H) — The H bit is set to a "1" when a carry occurs between bits 3 and 4 of the ALU during an ADD or ADC instruction. The H bit is useful in binary coded decimal subroutines.

INTERRUPT MASK BIT (I) — When the I bit is set, both the external interrupt and the timer interrupt are disabled. Clearing this bit enables the above interrupts. If an interrupt occurs while the I bit is set, the interrupt is latched and is processed when the I bit is next cleared.

NEGATIVE (N) — Indicates that the result of the last arithmetic, logical, or data manipulation is negative (bit 7 in the result is a logical "1").

ZERO (Z) — Indicates that the result of the last arithmetic, logical, or data manipulation is zero.

CARRY/BORROW (C) — Indicates that a carry or borrow out of the arithmetic logic unit (ALU) occurred during the last arithmetic operation. This bit is also affected during bit test and branch instructions, shifts, and rotates.

RESETS

The CDP6805F2 has two reset modes: an active low external reset pin ($\overline{\text{RESET}}$) and a power-on reset function; refer to Figure 5.

RESET

The $\overline{\text{RESET}}$ input pin is used to reset the MCU to provide an orderly software start-up procedure. When using the external reset mode, the $\overline{\text{RESET}}$ pin must stay low for a minimum of one t_{PL} . The $\overline{\text{RESET}}$ pin is provided with a Schmitt Trigger input to improve its noise immunity.

POWER-ON RESET

The power-on reset occurs when a positive transition is detected on V_{DD} . The power-on reset is used strictly for power turn-on conditions and should not be used to detect any drops in the power supply voltage. There is no provision

for a power-down reset. The power-on circuitry provides for a 1920 t_{CYC} delay from the time of the first oscillator operation. If the external $\overline{\text{RESET}}$ pin is low at the end of the 1920 time out, the processor remains in the reset condition.

Either of the two types of reset conditions causes the following to occur:

- Timer control register interrupt request bit (TCR7) is cleared to a "0".
- Timer control register interrupt mask bit (TCR6) is set to a "1".
- All data direction register bits are cleared to a "0". All ports are defined as inputs.
- Stack pointer is set to \$7F.
- The internal address bus is forced to the reset vector (\$7FE, \$7FF).
- Condition code register interrupt mask bit (I) is set to a "1".
- STOP and WAIT latches are reset.
- External interrupt latch is reset.

All other functions, such as other registers (including output ports), the timer, etc., are not cleared by the reset conditions.

INTERRUPTS

Systems often require that normal processing be interrupted so that some external event may be serviced. The CDP6805F2 may be interrupted by one of three different methods, either one of two maskable interrupts (external input or timer) or a non-maskable software interrupt (SWI).

Interrupts cause the processor registers to be saved on the stack and the interrupt mask set to prevent additional interrupts. The RTI instruction causes the register contents to be recovered from the stack and return to normal processing. The stacking order is shown in Figure 13.

Unlike $\overline{\text{RESET}}$, hardware interrupts do not cause the current instruction execution to be halted, but are considered pending until the current instruction execution is complete.

When the current instruction is complete, the processor checks all pending hardware interrupts and if unmasked, proceeds with interrupt processing; otherwise, the next instruction is fetched and executed. Note that masked interrupts are latched for later interrupt service.

If both an external interrupt and a timer interrupt are pending at the end of an instruction execution, the external interrupt is serviced first. The SWI is executed as any other instruction. Refer to Figure 14 for the interrupt and instruction processing sequence.

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CDP6805F2

TIMER INTERRUPT

Each time the timer decrements to zero (transitions from \$01 to \$00), the timer interrupt request bit (TCR7) is set. The processor is interrupted only if the timer mask bit (TCR6) and interrupt mask bit (I bit) are both cleared. When the interrupt is recognized, the current state of the machine is pushed on to the stack and the interrupt mask bit in the condition code register is set. This mask prevents further interrupts until the present one is serviced. The processor now vectors to the

timer interrupt service routine. The address for this service routine is specified by the contents of \$7F8 and \$7F9 unless the processor is in a WAIT mode, in which case the contents of \$7F6 and \$7F7 specify the timer service routine address. Software must be used to clear the timer interrupt request bit (TCR7). At the end of the timer interrupt service routine, the software normally executes an RTI instruction which restores the machine state and starts executing the interrupted program.

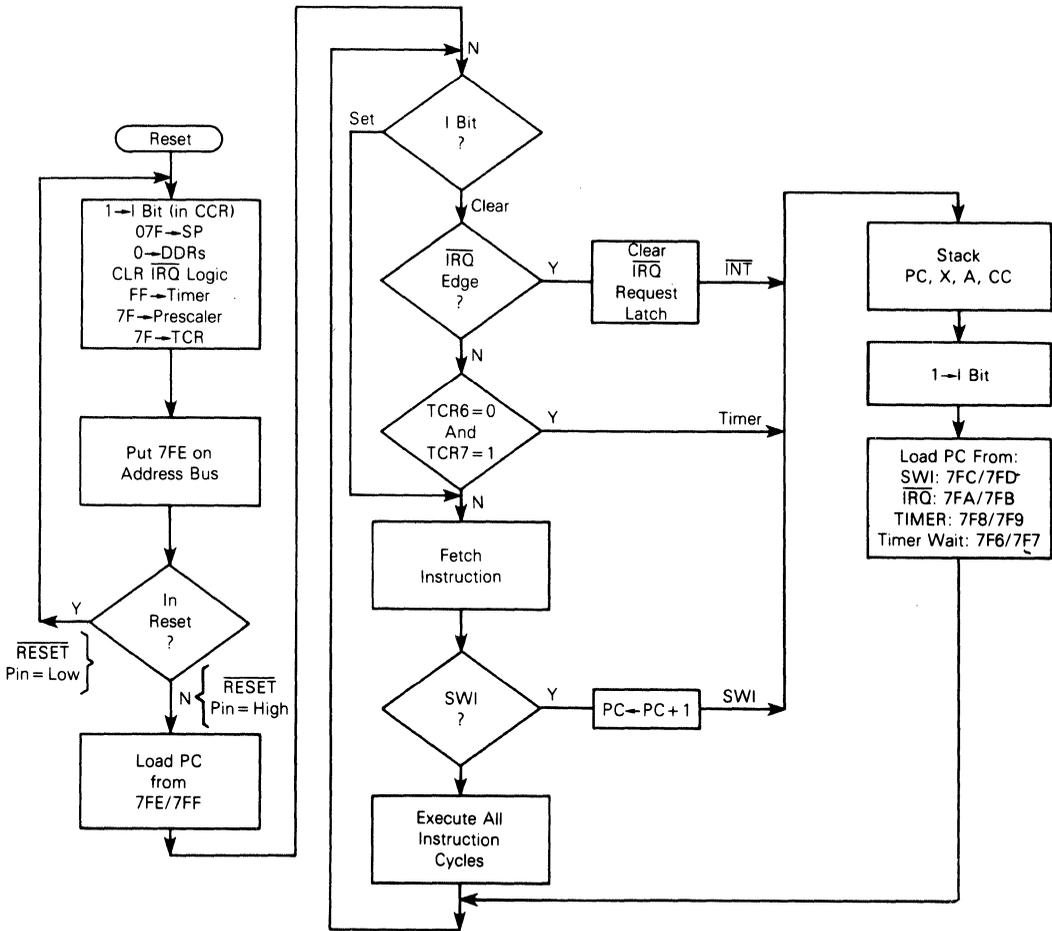


Fig. 14 - RESET and INTERRUPT processing flowchart.

EXTERNAL INTERRUPT

Either level- and edge-sensitive or edge-sensitive only inputs are available as mask options. If the interrupt mask bit of the condition code register is cleared and the external interrupt pin (\overline{IRQ}) is "low" or a negative edge has set the internal interrupt flip-flop, then the external interrupt occurs. The action of the external interrupt is identical to the timer except that the service routine address is specified by the contents of \$7FA and \$7FB. Figure 15 shows both a functional diagram and timing for the interrupt line. The timing diagram shows two different treatments of the interrupt line (\overline{IRQ}) to the processor. The first method is single pulses on the interrupt line spaced far enough apart to be serviced. The minimum time between pulses is a function of the length of the interrupt service routine. Once a pulse occurs, the next pulse should not occur until the MPU software has exited the routine (an RTI occurs). This time (t_{LIL}) is obtained by adding 20 instruction cycles (t_{CYC}) to the total number of cycles it takes to complete the service routine including the RTI in-

struction; refer to Figure 15. The second configuration shows many interrupt lines "wire ORed" to form the interrupts at the processor. Thus, if after servicing an interrupt the \overline{IRQ} remains low, then the next interrupt is recognized.

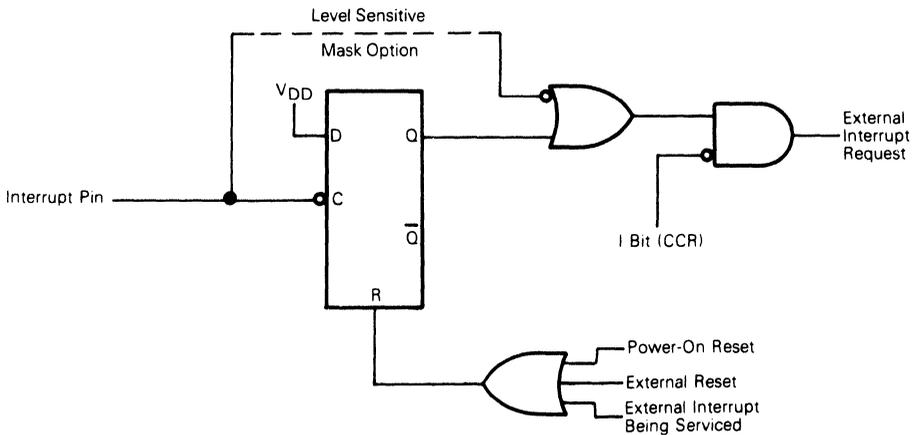
SOFTWARE INTERRUPT (SWI)

The software interrupt is an executable instruction. The action of the SWI instruction is similar to the hardware interrupts. The SWI is executed regardless of the state of the interrupt mask in the condition code register. The service routine address is specified by the contents of memory locations \$7FC and \$7FD.

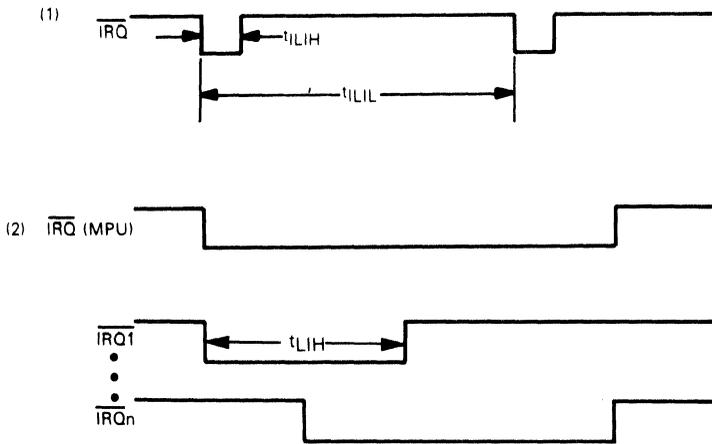
The following three functions are not strictly interrupts, however, they are tied very closely to the interrupts. These functions are RESET, STOP, and WAIT.

RESET — The RESET input pin and the internal power-on reset function each cause the program to vector to an initialization program. This vector is specified by the contents

(a) Interrupt Functional Diagram



(b) Interrupt Mode Diagram



Edge Condition
The minimum pulse width (t_{LIH}) is one t_{CYC} . The period t_{LIL} should not be less than the number of t_{CYC} cycles it takes to execute the interrupt service routine plus 20 t_{CYC} cycles.

Mask Optional Level Sensitive
If after servicing an interrupt the \overline{IRQ} remains low, then the next interrupt is recognized.

Fig. 15 - External interrupt.

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CDP6805F2

of memory locations \$7FE and \$7FF. The interrupt mask of the condition code register is also set. See preceding section on Reset for details.

STOP — The STOP instruction places the CDP6805F2 in its lowest power consumption mode. In the STOP function, the internal oscillator is turned off causing all internal processing and the timer to be halted; refer to Figure 16.

During the STOP mode, timer control register (TCR) bits 6 and 7 are altered to remove any pending timer interrupt requests and to disable any further timing interrupts. External interrupts are enabled in the condition code register. All other registers and memory remain unaltered. All I/O lines remain unchanged. The processor can only be brought out of the STOP mode by an external IRQ or RESET.

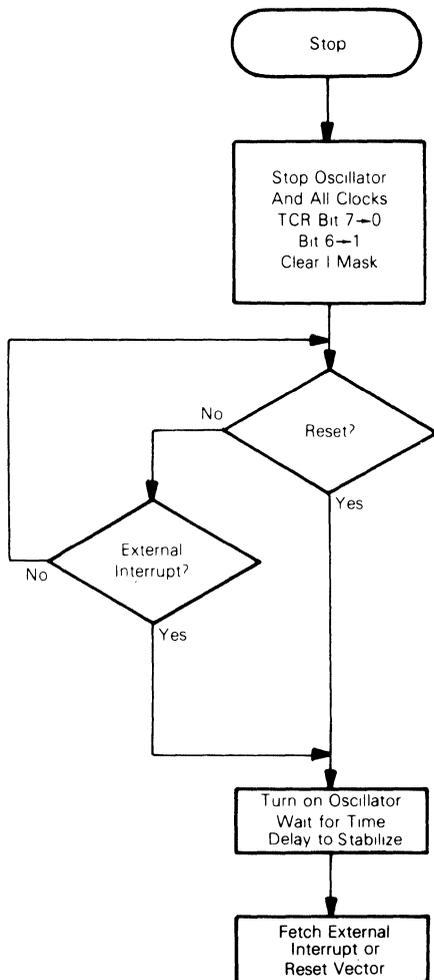


Fig. 16 — Stop function flowchart.

WAIT — The WAIT instruction places the CDP6805F2 in a low-power consumption mode, but the WAIT mode consumes somewhat more power than the STOP mode. In the WAIT mode, the internal clock is disabled from all internal circuitry except the timer circuit; refer to Figure 17. Thus, all internal processing is halted, however, the timer continues to count normally.

During the WAIT mode, the I bit in the condition code register is cleared to enable interrupts. All other registers, memory, and I/O lines remain in their last state. The timer may be enabled by software prior to entering the WAIT mode to allow a periodic exit from the WAIT mode. If an external and a timer interrupt occur at the same time, the external interrupt is serviced first; then, if the timer interrupt request is not cleared in the external interrupt routine, the normal timer interrupt (not the timer WAIT interrupt) is serviced since the MCU is no longer in the WAIT mode.

TIMER

The MCU timer contains an 8-bit software programmable counter with a 7-bit software selectable prescaler. Figure 18 contains a block diagram of the timer. The counter may be preset under program control and decrements towards zero. When the counter decrements to zero, the timer interrupt request bit (i.e., bit 7 of the timer control register (TCR)) is set. Then, if the timer interrupt is not masked (i.e., bit 6 of the TCR and the I bit in the condition code register are both cleared) the processor receives an interrupt. After completion of the current instruction, the processor proceeds to store the appropriate registers on the stack and then fetches the timer vector address from locations \$7F8 and \$7F9 (or \$7F6 and \$7F7 if in the WAIT mode) in order to begin servicing.

The counter continues to count after it reaches zero allowing the software to determine the number of internal or external input clocks since the timer interrupt request bit was set. The counter may be read at any time by the processor without disturbing the count. The contents of the counter become stable, prior to the read portion of a cycle, and do not change during the read. The timer interrupt request bit remains set until cleared by the software. TCR7 may also be used as a scanned status bit in a non-interrupt mode of operation (TCR6=1).

The prescaler is a 7-bit divider which is used to extend the maximum length of the timer. Bit 0, bit 1, and bit 2 of the TCR are programmed to choose the appropriate prescaler output within the range of +1 to +128 which is used as the counter input. The processor cannot write into or read from the prescaler, however, its contents are cleared to all "0s" by the write operation into TCR when bit 3 of the written data equals one. This allows for truncation-free counting.

The timer input can be configured for three different operating modes plus a disable mode depending on the value written to the TCR4 and TCR5 control bits. Refer to the Timer Control Register section.

TIMER INPUT MODE 1

If TCR5 and TCR4 are both programmed to a "0", the input to the timer is from an internal clock and the TIMER input pin is disabled. The internal clock mode can be used for

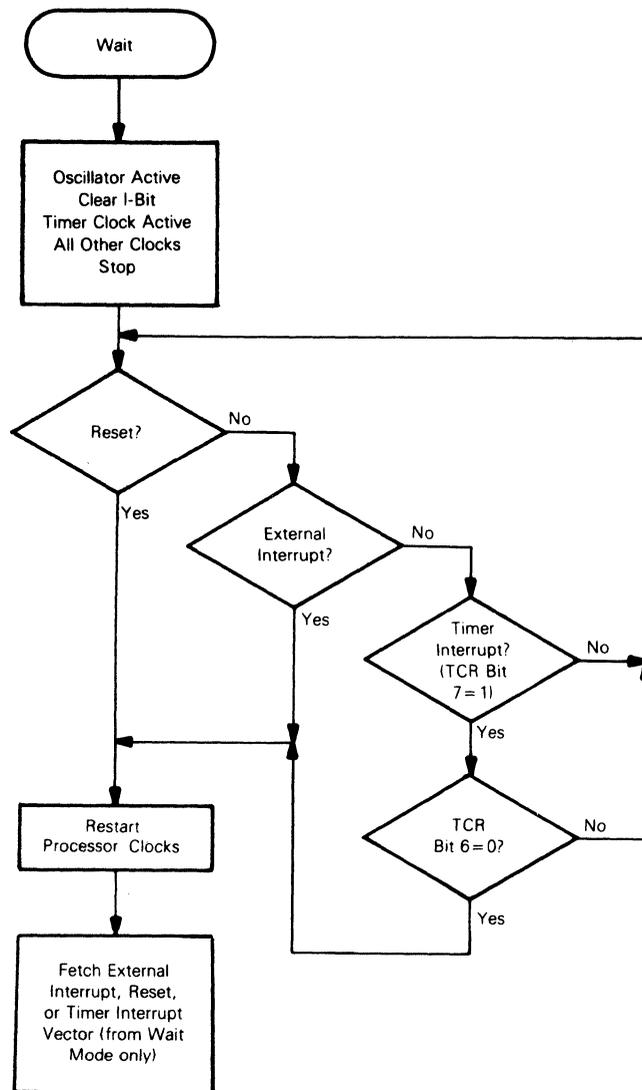


Fig. 17 - WAIT function flowchart.

periodic interrupt generation as well as a reference in frequency and event measurement. The internal clock is the instruction cycle clock. During a WAIT instruction, the internal clock to the timer continues to run at its normal rate.

TIMER INPUT MODE 2

With $TCR5=0$ and $TCR4=1$, the internal clock and the TIMER input pin are ANDed to form the timer input signal. This mode can be used to measure external pulse widths. The external timer input pulse simply turns on the internal clock for the duration of the pulse. The resolution of the count in this mode is \pm one internal clock and therefore, accuracy improves with longer input pulse widths.

TIMER INPUT MODE 3

If $TCR5=1$ and $TCR4=0$, all inputs to the timer are disabled.

TIMER INPUT MODE 4

If $TCR5=1$ and $TCR4=1$, the internal clock input to the timer is disabled and the TIMER input pin becomes the input to the timer. The timer can, in this mode, be used to count external events as well as external frequencies for generating periodic interrupts. The counter is clocked on the falling edge of the external signal.

Figure 18 shows a block diagram of the timer subsystem. Power-on reset and the STOP instruction invalidate the contents of the counter.

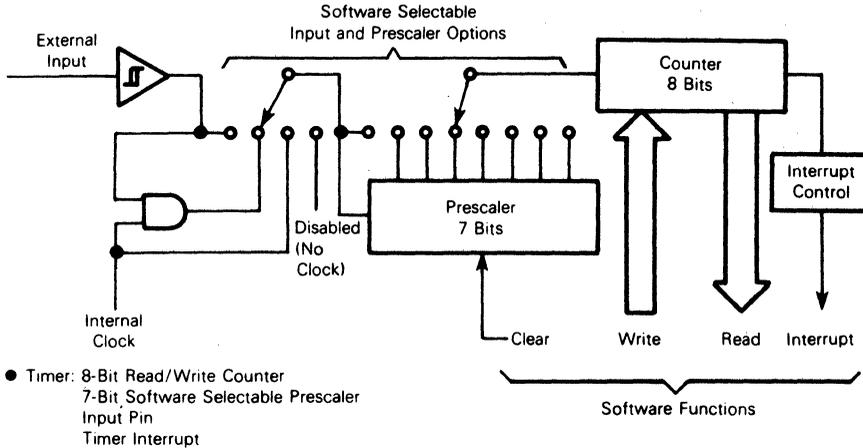


Fig. 18 - Programmable timer/counter block diagram.

TIMER CONTROL REGISTER (TCR)

7	6	5	4	3	2	1	0
TCR7	TCR6	TCR5	TCR4	TCR3	TCR2	TCR1	TCR0

All bits in this register except bit 3 are read/write bits.

TCR7 - Timer interrupt request bit: bit used to indicate the timer interrupt when it is logic "1".

- 1 - Set whenever the counter decrements to zero or under program control.
- 0 - Cleared on external **RESET**, power-on reset, STOP instruction, or program control.

TCR6 - Timer interrupt mask bit: when this bit is a logic "1", it inhibits the timer interrupt to the processor.

- 1 - Set on external **RESET**, power-on reset, STOP instruction, or program control.
- 0 - Cleared under program control.

TCR5 - External or internal bit: selects the input clock source to be either the external timer pin or the internal clock. (Unaffected by **RESET**.)

- 1 - Select external clock source.
- 0 - Select internal clock source.

TCR4 - External enable bit: control bit used to enable the external **TIMER** pin. (Unaffected by **RESET**.)

- 1 - Enable external **TIMER** pin.
- 0 - Disable external **TIMER** pin.

TCR5	TCR4	
0	0	Internal Clock to Timer
0	1	AND of Internal Clock and TIMER Pin to Timer
1	0	Inputs to Timer Disabled
1	1	TIMER Pin to Timer

TCR3 - Timer Prescaler Reset bit: writing a "1" to this bit resets the prescaler to zero. A read of this location always indicates "0". (Unaffected by **RESET**.)

TCR2, TCR1, TCR0 - Prescaler select bits: decoded to select one of eight outputs on the prescaler. (Unaffected by **RESET**.)

Prescaler

TCR2	TCR1	TCR0	Result
0	0	0	+1
0	0	1	+2
0	1	0	+4
0	1	1	+8
1	0	0	+16
1	0	1	+32
1	1	0	+64
1	1	1	+128

INSTRUCTION SET

The MCU has a set of 61 basic instructions. They can be divided into five different types: register/memory, read-modify-write, branch, bit manipulation, and control. The following paragraphs briefly explain each type. All the instructions within a given type are presented in individual tables.

REGISTER/MEMORY INSTRUCTIONS

Most of these instructions use two operands. One operand is either the accumulator or the index register. The other operand is obtained from memory using one of the addressing modes. The operand for the jump unconditional (**JMP**) and jump to subroutine (**JSR**) instructions is the program counter. Refer to Table 4.

READ-MODIFY-WRITE INSTRUCTIONS

These instructions read a memory location or a register, modify or test its contents, and write the modified value back to memory or to the register. The test for negative or zero (TST) instruction is an exception to the read-modify-write sequence since it does not modify the value. Refer to Table 5.

BRANCH INSTRUCTIONS

Most branch instructions test the state of the condition code register and, if certain criteria are met, a branch is executed. This adds an offset between -127 and $+128$ to the current program counter. Refer to Table 6.

BIT MANIPULATION INSTRUCTIONS

The MCU is capable of setting or clearing any bit which resides in the first 128 bytes of the memory space where all port registers, port DDRs, timer, timer control, and on-chip RAM reside. An additional feature allows the software to test and branch on the state of any bit within the first 256 locations. The bit set, bit clear, and bit test and branch functions are implemented with a single instruction. For the test and branch instructions, the value of the bit tested is also placed in the carry bit of the condition code register. Refer to Table 7.

CONTROL INSTRUCTIONS

These instructions are register reference instructions and are used to control processor operation during program execution. Refer to Table 8.

OPCODE MAP

Table 9 is an opcode map for the instructions used on the MCU.

ALPHABETICAL LISTING

The complete instruction set is given in alphabetical order in Table 10.

ADDRESSING MODES

The MCU uses ten different addressing modes to provide the programmer with an opportunity to optimize the code to all situations. The various indexed addressing modes make it possible to locate data tables, code conversion tables, and scaling tables anywhere in the memory space. Short indexed accesses are single-byte instructions while the longest instructions (three bytes) permit tables throughout memory. Short and long absolute addressing is also included. Two-byte direct addressing instructions access all data bytes in most applications. Extended addressing permits jump instructions to reach all memory. Table 10 shows the addressing modes for each instruction with the effects each instruction has on the condition code register. An opcode map is shown in Table 9.

The term "Effective Address" (EA) is defined as the byte address to or from which the argument for an instruction is fetched or stored. The ten addressing modes of the processor are described below. Parentheses are used to indicate

"contents of," an arrow indicates "is replaced by," and a colon indicates "concatenation of two bytes."

INHERENT

In inherent instructions, all the information necessary to execute the instruction is contained in the opcode. Operations specifying only the index registers or accumulator and no other arguments are included in this mode.

IMMEDIATE

In immediate addressing, the operand is contained in the byte immediately following the opcode. Immediate addressing is used to access constants which do not change during program execution (e.g., a constant used to initialize a loop counter).

$$EA = PC + 1; PC \leftarrow PC + 2$$

DIRECT

In the direct addressing mode, the effective address of the argument is contained in a single byte following the opcode byte. Direct addressing allows the user to directly address the lowest 256 bytes in memory with a single two-byte instruction. This includes all on-chip RAM and I/O registers and 128 bytes of on-chip ROM. Direct addressing is efficient in both memory and time.

$$EA = (PC + 1); PC \leftarrow PC + 2$$

$$\text{Address Bus High} \leftarrow 0; \text{Address Bus Low} \leftarrow (PC + 1)$$

EXTENDED

In the extended addressing mode, the effective address of the argument is contained in the two bytes following the opcode. Instructions with extended addressing modes are capable of referencing arguments anywhere in memory with a single three-byte instruction. When using the CDP6805 assembler, the user need not specify whether an instruction uses direct or extended addressing. The assembler automatically selects the most efficient addressing mode.

$$EA = (PC + 1):(PC + 2); PC \leftarrow PC + 3$$

$$\text{Address Bus High} \leftarrow (PC + 1); \text{Address Bus Low} \leftarrow (PC + 2)$$

INDEXED, NO-OFFSET

In the indexed, no-offset addressing mode, the effective address of the argument is contained in the 8-bit index register. Thus, this addressing mode can access the first 256 memory locations. These instructions are only one byte long. This mode is used to move a pointer through a table or to address a frequently referenced RAM or I/O location.

$$EA = X; PC \leftarrow PC + 1$$

$$\text{Address Bus High} \leftarrow 0; \text{Address Bus Low} \leftarrow X$$

INDEXED, 8-BIT OFFSET

Here the EA is obtained by adding the contents of the byte following the opcode to that of the index register, therefore, the operand is located anywhere within the lowest 511 memory locations. For example, this mode of addressing is useful for selecting the m th element in an n element table. All instructions are two bytes. The content of the index register

(X) is not changed. The content of (PC + 1) is an unsigned 8-bit integer. One-byte offset indexing permits look-up tables to be easily accessed in either RAM or ROM.

$$EA = X + (PC + 1); PC \leftarrow PC + 2$$

Address Bus High \leftarrow K; Address Bus Low \leftarrow X + (PC + 1)
where K = The carry from the addition of X + (PC + 1)

INDEXED, 16-BIT OFFSET

In the indexed, 16-bit offset addressing mode, the effective address is the sum of the contents of the unsigned 8-bit index register and the two unsigned bytes following the opcode. This addressing mode can be used in a manner similar to indexed 8-bit offset, except that this three-byte instruction allows tables to be anywhere in memory (e.g., jump tables in ROM). **As with direct and extended, the assembler determines the most efficient form of indexed offset — 8 or 16 bit. The content of the index register is not changed.**

$$EA = X + [(PC + 1):(PC + 2)]; PC \leftarrow PC + 3$$

$$\text{Address Bus High} \leftarrow (PC + 1) + K;$$

$$\text{Address Bus Low} \leftarrow X + (PC + 2)$$

where K = The carry from the addition of X + (PC + 2)

RELATIVE

Relative addressing is only used in branch instructions. In relative addressing, the contents of the 8-bit signed byte following the opcode (the offset) is added to the PC if and only if the branch condition is true. Otherwise, control proceeds to the next instruction. The span of relative addressing is limited to the range of -126 to +129 bytes from the branch instruction opcode location. The Motorola assembler calculates the proper offset and checks to see if it is within the span of the branch.

$$EA = PC + 2 + (PC + 1); PC \leftarrow EA \text{ if branch taken;} \\ \text{otherwise, } PC \leftarrow PC + 2$$

BIT SET/CLEAR

Direct addressing and bit addressing are combined in instructions which set and clear individual memory and I/O bits. In the bit set and clear instructions, the byte is specified as a direct address in the location following the opcode. The first 128 addressable locations are thus accessed. The bit to be modified within that byte is specified with three bits of the opcode. The bit set and clear instructions occupy two bytes: one for the opcode (including the bit number) and the second for addressing the byte which contains the bit of interest.

$$EA = (PC + 1); PC \leftarrow PC + 2$$

$$\text{Address Bus High} \leftarrow 0; \text{Address Bus Low} \leftarrow (PC + 1)$$

BIT TEST AND BRANCH

Bit test and branch is a combination of direct addressing, bit addressing, and relative addressing. The bit address and condition (set or clear) to be tested is part of the opcode. The address of the byte to be tested is in the single byte immediately following the opcode byte (EA1). The signed relative 8-bit offset is in the third byte (EA2) and is added to the PC if the specified bit is set or cleared in the specified memory location. This single three-byte instruction allows the program to branch based on the condition of any bit in the first 256 locations of memory.

$$EA1 = (PC + 1)$$

$$\text{Address Bus High} \leftarrow 0; \text{Address Bus Low} \leftarrow (PC + 1)$$

$$EA2 = PC + 3 + (PC + 2); PC \leftarrow EA2 \text{ if branch taken;} \\ \text{otherwise, } PC \leftarrow PC + 3$$

TABLE 4 — REGISTER/MEMORY INSTRUCTIONS

		Addressing Modes																	
		Immediate			Direct			Extended			Indexed (No Offset)			Indexed (8-Bit Offset)			Indexed (16-Bit Offset)		
Function	Mnemonic	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles
Load A from Memory	LDA	A6	2	2	B6	2	3	C6	3	4	F6	1	3	E6	2	4	D6	3	5
Load X from Memory	LDX	AE	2	2	BE	2	3	CE	3	4	FE	1	3	EE	2	4	DE	3	5
Store A in Memory	STA	—	—	—	B7	2	4	C7	3	5	F7	1	4	E7	2	5	D7	3	6
Store X in Memory	STX	—	—	—	BF	2	4	CF	3	5	FF	1	4	EF	2	5	DF	3	6
Add Memory to A	ADD	AB	2	2	BB	2	3	CB	3	4	FB	1	3	EB	2	4	DB	3	5
Add Memory and Carry to A	ADC	A9	2	2	B9	2	3	C9	3	4	F9	1	3	E9	2	4	D9	3	5
Subtract Memory	SUB	A0	2	2	B0	2	3	C0	3	4	F0	1	3	E0	2	4	D0	3	5
Subtract Memory from A with Borrow	SBC	A2	2	2	B2	2	3	C2	3	4	F2	1	3	E2	2	4	D2	3	5
AND Memory to A	AND	A4	2	2	B4	2	3	C4	3	4	F4	1	3	E4	2	4	D4	3	5
OR Memory with A	ORA	AA	2	2	BA	2	3	CA	3	4	FA	1	3	EA	2	4	DA	3	5
Exclusive OR Memory with A	EOR	A8	2	2	B8	2	3	C8	3	4	F8	1	3	E8	2	4	D8	3	5
Arithmetic Compare A with Memory	CMP	A1	2	2	B1	2	3	C1	3	4	F1	1	3	E1	2	4	D1	3	5
Arithmetic Compare X with Memory	CPX	A3	2	2	B3	2	3	C3	3	4	F3	1	3	E3	2	4	D3	3	5
Bit Test Memory with A (Logical Compare)	BIT	A5	2	2	B5	2	3	C5	3	4	F5	1	3	E5	2	4	D5	3	5
Jump Unconditional	JMP	—	—	—	BC	2	2	CC	3	3	FC	1	2	EC	2	3	DC	3	4
Jump to Subroutine	JSR	—	—	—	BD	2	5	CD	3	6	FD	1	5	ED	2	6	DD	3	7

TABLE 5 — READ-MODIFY-WRITE INSTRUCTIONS

		Addressing Modes														
		Inherent (A)			Inherent (X)			Direct			Indexed (No Offset)			Indexed (8-Bit Offset)		
Function	Mnemonic	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles
Increment	INC	4C	1	3	5C	1	3	3C	2	5	7C	1	5	6C	2	6
Decrement	DEC	4A	1	3	5A	1	3	3A	2	5	7A	1	5	6A	2	6
Clear	CLR	4F	1	3	5F	1	3	3F	2	5	7F	1	5	6F	2	6
Complement	COM	43	1	3	53	1	3	33	2	5	73	1	5	63	2	6
Negate (2's Complement)	NEG	40	1	3	50	1	3	30	2	5	70	1	5	60	2	6
Rotate Left Thru Carry	ROL	49	1	3	59	1	3	39	2	5	79	1	5	69	2	6
Rotate Right Thru Carry	ROR	46	1	3	56	1	3	36	2	5	76	1	5	66	2	6
Logical Shift Left	LSL	48	1	3	58	1	3	38	2	5	78	1	5	68	2	6
Logical Shift Right	LSR	44	1	3	54	1	3	34	2	5	74	1	5	64	2	6
Arithmetic Shift Right	ASR	47	1	3	57	1	3	37	2	5	77	1	5	67	2	6
Test for Negative or Zero	TST	4D	1	3	5D	1	3	3D	2	4	7D	1	4	6D	2	5

TABLE 6 — BRANCH INSTRUCTIONS

Function	Mnemonic	Relative Addressing Mode		
		Op Code	# Bytes	# Cycles
Branch Always	BRA	20	2	3
Branch Never	BRN	21	2	3
Branch IFF Higher	BHI	22	2	3
Branch IFF Lower or Same	BLS	23	2	3
Branch IFF Carry Clear	BCC	24	2	3
(Branch IFF Higher or Same)	(BHS)	24	2	3
Branch IFF Carry Set	BCS	25	2	3
(Branch IFF Lower)	(BLO)	25	2	3
Branch IFF Not Equal	BNE	26	2	3
Branch IFF Equal	BEQ	27	2	3
Branch IFF Half Carry Clear	BHCC	28	2	3
Branch IFF Half Carry Set	BHCS	29	2	3
Branch IFF Plus	BPL	2A	2	3
Branch IFF Minus	BMI	2B	2	3
Branch IFF Interrupt Mask Bit is Clear	BMC	2C	2	3
Branch IFF Interrupt Mask Bit is Set	BMS	2D	2	3
Branch IFF Interrupt Line is Low	BIL	2E	2	3
Branch IFF Interrupt Line is High	BIH	2F	2	3
Branch to Subroutine	BSR	AD	2	6

TABLE 7 — BIT MANIPULATION INSTRUCTIONS

Function	Mnemonic	Addressing Modes					
		Bit Set/Clear			Bit Test and Branch		
		Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles
Branch IFF Bit n is Set	BRSET n (n=0...7)	—	—	—	2*n	3	5
Branch IFF Bit n is Clear	BRCLR n (n=0...7)	—	—	—	01+2*n	3	5
Set Bit n	BSET n (n=0...7)	10+2*n	2	5	—	—	—
Clear Bit n	BCLR n (n=0...7)	11+2*n	2	5	—	—	—

TABLE 8 — CONTROL INSTRUCTIONS

Function	Mnemonic	Inherent		
		Op Code	# Bytes	# Cycles
Transfer A to X	TAX	97	1	2
Transfer X to A	TXA	9F	1	2
Set Carry Bit	SEC	99	1	2
Clear Carry Bit	CLC	98	1	2
Set Interrupt Mask Bit	SEI	9B	1	2
Clear Interrupt Mask Bit	CLI	9A	1	2
Software Interrupt	SWI	83	1	10
Return from Subroutine	RTS	81	1	6
Return from Interrupt	RTI	80	1	9
Reset Stack Pointer	RSP	9C	1	2
No-Operation	NOP	9D	1	2
Stop	STOP	8E	1	2
Wait	WAIT	8F	1	2

TABLE 9— INSTRUCTION SET OPCODE MAP

		Bit Manipulation		Branch		Read-Modify-Write				Control		Register/Memory							
		BTB	BSC	REL	DIR	INH	INH	IX1	IX	INH	INH	IMM	DIR	EXT	IX2	IX1	IX	Hi	Low
		0	0001	0010	0011	0100	0101	0110	0111	1000	1001	A	B	C	D	E	F		
Low	Hi	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111		
0	0000	BRSET0 BTB 5	BSET0 BSC 5	BRA REL 3	NEG DIR 1	NEG INH 1	NEG INH 2	NEG IX1 1	NEG IX 1	RTI INH 6		SUB IMM 2	SUB DIR 3	SUB EXT 3	SUB IX2 2	SUB IX1 1	SUB IX 3	0	0000
1	0001	BRCLR0 BTB 5	BCLR0 BSC 5	BRN REL 3						RTS INH 6		CMP IMM 2	CMP DIR 3	CMP EXT 3	CMP IX2 2	CMP IX1 1	CMP IX 3	1	0001
2	0010	BRSET1 BTB 5	BSET1 BSC 5	BHI REL 3								SBC IMM 2	SBC DIR 3	SBC EXT 3	SBC IX2 2	SBC IX1 1	SBC IX 3	2	0010
3	0011	BRCLR1 BTB 5	BCLR1 BSC 5	BLS REL 3	COM DIR 1	COMA INH 1	COMX INH 2	COM IX1 1	COM IX 1	SWI INH 10		CPX IMM 2	CPX DIR 3	CPX EXT 3	CPX IX2 2	CPX IX1 1	CPX IX 3	3	0011
4	0100	BRSET2 BTB 5	BSET2 BSC 5	BCC REL 2	LSR DTR 1	LSRA INH 1	LSRX INH 2	LSR IX1 1	LSR IX 1			AND IMM 2	AND DIR 3	AND EXT 3	AND IX2 2	AND IX1 1	AND IX 3	4	0100
5	0101	BRCLR2 BTB 5	BCLR2 BSC 5	BCS REL 3								BIT IMM 2	BIT DIR 3	BIT EXT 3	BIT IX2 2	BIT IX1 1	BIT IX 3	5	0101
6	0110	BRSET3 BTB 5	BSET3 BSC 5	BNE REL 2	ROR DIR 1	RORA INH 1	RORX INH 2	ROR IX1 1	ROR IX 1			LDA IMM 2	LDA DIR 3	LDA EXT 3	LDA IX2 2	LDA IX1 1	LDA IX 3	6	0110
7	0111	BRCLR3 BTB 5	BCLR3 BSC 5	BEQ REL 3	ASR DIR 1	ASRA INH 1	ASRX INH 2	ASR IX1 1	ASR IX 1	TAX INH 2			STA DIR 3	STA EXT 3	STA IX2 2	STA IX1 1	STA IX 3	7	0111
8	1000	BRSET4 BTB 5	BSET4 BSC 5	BHCC REL 2	LSL DIR 1	LSLA INH 1	LSLX INH 2	LSL IX1 1	LSL IX 1	CLC INH 1		EOR IMM 2	EOR DIR 3	EOR EXT 3	EOR IX2 2	EOR IX1 1	EOR IX 3	8	1000
9	1001	BRCLR4 BTB 5	BCLR4 BSC 5	BHCS REL 2	ROL DIR 1	ROLA INH 1	ROLX INH 2	ROL IX1 1	ROL IX 1	SEC INH 1		ADC IMM 2	ADC DIR 3	ADC EXT 3	ADC IX2 2	ADC IX1 1	ADC IX 3	9	1001
A	1010	BRSET5 BTB 5	BSET5 BSC 5	BPL REL 2	DEC DIR 1	DECA INH 1	DECX INH 2	DEC IX1 1	DEC IX 1	CLI INH 1		ORA IMM 2	ORA DIR 3	ORA EXT 3	ORA IX2 2	ORA IX1 1	ORA IX 3	A	1010
B	1011	BRCLR5 BTB 5	BCLR5 BSC 5	BMI REL 3						SEI INH 1		ADD IMM 2	ADD DIR 3	ADD EXT 3	ADD IX2 2	ADD IX1 1	ADD IX 3	B	1011
C	1100	BRSET6 BTB 5	BSET6 BSC 5	BMC REL 2	INC DIR 1	INCA INH 1	INCX INH 2	INC IX1 1	INC IX 1	RSP INH 1			JMP DIR 3	JMP EXT 3	JMP IX2 2	JMP IX1 1	JMP IX 3	C	1100
D	1101	BRCLR6 BTB 5	BCLR6 BSC 5	BMS REL 2	TST DIR 1	TSTA INH 1	TSTX INH 2	TST IX1 1	TST IX 1	NOP INH 2		BSR REL 2	JSR DIR 3	JSR EXT 3	JSR IX2 2	JSR IX1 1	JSR IX 3	D	1101
E	1110	BRSET7 BTB 5	BSET7 BSC 5	BIL REL 3						STOP INH 2		LDX IMM 2	LDX DIR 3	LDX EXT 3	LDX IX2 2	LDX IX1 1	LDX IX 3	E	1110
F	1111	BRCLR7 BTB 5	BCLR7 BSC 5	BIH REL 2	CLR DIR 1	CLRA INH 1	CLRX INH 2	CLR IX1 1	CLR IX 1	WAIT INH 2	TXA INH 1		STX DIR 3	STX EXT 3	STX IX2 2	STX IX1 1	STX IX 3	F	1111

Abbreviations for Address Modes

- INH Inherent
- IMM Immediate
- DIR Direct
- EXT Extended
- REL Relative
- BSC Bit Set/Clear
- BTB Bit Test and Branch
- IX Indexed (No Offset)
- IX1 Indexed, 1 Byte (8-Bit) Offset
- IX2 Indexed, 2 Byte (16-Bit) Offset

LEGEND

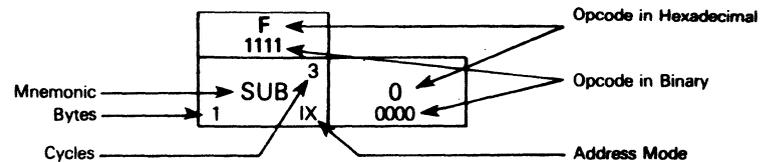


TABLE 10 — INSTRUCTION SET

Mnemonic	Addressing Modes										Condition Codes				
	Inherent	Immediate	Direct	Extended	Relative	Indexed (No Offset)	Indexed (8 Bits)	Indexed (16 Bits)	Bit Set/Clear	Bit Test & Branch	H	I	N	Z	C
ADC		X	X	X		X	X	X			●	●	●	●	●
ADD		X	X	X		X	X	X			●	●	●	●	●
AND		X	X	X		X	X	X			●	●	●	●	●
ASL	X		X			X	X				●	●	●	●	●
ASR	X		X			X	X				●	●	●	●	●
BCC					X						●	●	●	●	●
BCLR									X		●	●	●	●	●
BCS					X						●	●	●	●	●
BEO					X						●	●	●	●	●
BHCC					X						●	●	●	●	●
BHCS					X						●	●	●	●	●
BHI					X						●	●	●	●	●
BHS					X						●	●	●	●	●
BIH					X						●	●	●	●	●
BIL					X						●	●	●	●	●
BIT		X	X	X		X	X	X			●	●	●	●	●
BLO					X						●	●	●	●	●
BLS					X						●	●	●	●	●
BMC					X						●	●	●	●	●
BMI					X						●	●	●	●	●
BMS					X						●	●	●	●	●
BNE					X						●	●	●	●	●
BPL					X						●	●	●	●	●
BRA					X						●	●	●	●	●
BRN					X						●	●	●	●	●
BRCLR										X	●	●	●	●	●
BRSET										X	●	●	●	●	●
BSET									X		●	●	●	●	●
BSR					X						●	●	●	●	●
CLC	X										●	●	●	●	●
CLI	X										●	0	●	●	●
CLR	X		X			X	X				●	0	1	●	●
CMP		X	X	X		X	X	X			●	●	●	●	●
COM	X		X			X	X				●	●	●	1	●
CPX		X	X	X		X	X	X			●	●	●	●	●
DEC	X		X			X	X				●	●	●	●	●
EOR		X	X	X		X	X	X			●	●	●	●	●
INC	X		X			X	X				●	●	●	●	●
JMP			X	X		X	X	X			●	●	●	●	●
JSR			X	X		X	X	X			●	●	●	●	●
LDA		X	X	X		X	X	X			●	●	●	●	●
LDX		X	X	X		X	X	X			●	●	●	●	●
LSL	X		X			X	X				●	●	●	●	●
LSR	X		X			X	X				●	0	●	●	●
NEG	X		X			X	X				●	●	●	●	●
NOP	X										●	●	●	●	●
ORA		X	X	X		X	X	X			●	●	●	●	●
ROL	X		X			X	X				●	●	●	●	●
ROR	X		X			X	X				●	●	●	●	●
RSP	X										●	●	●	●	●
RTI	X										?	?	?	?	?
RTS	X										●	●	●	●	●
SBC		X	X	X		X	X	X			●	●	●	●	●
SEC	X										●	●	●	1	●
SEI	X										●	1	●	●	●
STA			X	X		X	X	X			●	●	●	●	●
STOP	X										●	0	●	●	●
STX			X	X		X	X	X			●	●	●	●	●
SUB		X	X	X		X	X	X			●	●	●	●	●
SWI	X										●	1	●	●	●
TAX	X										●	●	●	●	●
TST	X		X			X	X				●	●	●	●	●
TXA	X										●	●	●	●	●
WAIT	X										●	0	●	●	●

Condition Code Symbols

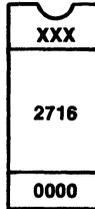
- H Half Carry (From Bit 3)
- I Interrupt Mask
- N Negative (Sign Bit)
- Z Zero
- C Carry/Borrow
- A Test and Set if True. Cleared Otherwise.
- Not Affected
- ? Load CC Register From Stack
- 0 Cleared
- 1 Set

To minimize power consumption, all unused ROM locations should contain zeros.

MASTER-DEVICE METHOD

EPROM—A 2716 EPROM, programmed with the customer program (positive logic sense for address and data), may be submitted for pattern generation. Fill out Customer Information of ROM Information Sheet. Note that the first 128

(0000-007F) bytes of the EPROM correspond to the CDP6805F2 internal RAM and I/O ports and will be ignored when generating ROM masks. The 831 unused and self-check bytes (04B7-07F5) will also be ignored when generating ROM masks. The EPROM should be placed in a conductive IC carrier and securely packed. Do not use styrofoam.



XXX=Customer ID

Fig. 1a - EPROM marking.

ROM INFORMATION SHEET

OPTION LIST

Select the options for your MCU from the following list. A manufacturing mask will be generated from this information. Select one in each section.

Internal Oscillator Input Column 28 of Option Card
 Crystal 0 or N
 Resistor 1 or P

Internal Divide Column 29 of Option Card
 ÷ 4 0 or N
 ÷ 2 1 or P

Interrupt Column 30 of Option Card
 Edge-Sensitive 0 or N
 Level- and Edge-Sensitive 1 or P

VECTOR LIST

Timer Interrupt from Wait State Only _____
 Timer Interrupt _____
 External Interrupt _____
 SWI _____
 RESET _____

CUSTOMER INFORMATION

Customer Name _____
 Address _____
 City _____ State _____ Zip _____
 Phone () _____ Extension _____
 Contact Ms./Mr. _____
 Customer Part No. _____

PATTERN MEDIA

- 6805F2
- EPROM
- Card Deck
- Other*

*Other media require factory approval.

Signature _____
 Title _____

CDP6805F2

DATA PROGRAMMING INSTRUCTIONS

When a customer submits instructions for programming RCA custom ROMs, the customer must also complete the relevant parts of the ROM information sheet and submit this sheet together with the programming instructions. Programming instructions may be submitted in any one of three ways, as follows:

1. **Computer-Card Deck**—use standard 80-column computer punch cards.
2. **Floppy Diskette**—diskette information must be generated on an RCA CDP1800-series microprocessor development system.

3. **Master Device**—a ROM, PROM, EPROM, or CDP6805F2 that contains the required programming information.

The requirements for each method are explained in detail in the following paragraphs:

COMPUTER-CARD METHOD

Use standard 80-column computer cards. Each card deck must contain, in order, a title card, an option card, a data-format card, and data cards. Punch the cards as specified in the following charts:

TITLE CARD

Column No.	Data
1	Punch T
2-5	leave blank
6-30	Customer Name (start at 6)
31-34	leave blank
35-54	Customer Address or Division (start at 35)
55-58	leave blank
59-63	RCA custom selection number (5 digits) (Obtained from RCA Sales Office)
64	leave blank
65-71	RCA device type, without CDP68 prefix, e.g. 05F2
72	Punch an opening parenthesis (
73	Punch 8
74	Punch a closing parenthesis)
75-78	leave blank
79-80	Punch a 2-digit decimal number to indicate the deck number; the first deck should be numbered 01

OPTION CARD

Use the ROM Information Sheet to select the polarity options, P, N, or X, for the desired ROM type.	
Column No.	Data
1-6	Punch the word OPTION
7	leave blank
8-17	RCA device type, including CDP68 prefix, e.g. CDP6805F2
18-27	leave blank
28-30	Punch P or N per ROM Information Sheet
31-78	leave blank
79-80	Punch the deck number (the 2-digit number in columns 79-80 of the title card)

DATA-FORMAT CARD

The data-format card specifies the form in which the data is to be entered into ROM.	
Column No.	Data
1-11	Punch the words DATA FORMAT
12	leave blank
13-15	Punch the letters HEX
16	leave blank
17-19	Punch POS
20-78	leave blank
79-80	Punch the deck number (the 2-digit number in columns 79-80 of the title card)

CDP6805 FAMILY

	Available Now	
	CDP6805E2	CDP6805G2
Technology	CMOS	CMOS
Number of Pins	40	40
On-Chip RAM (Bytes)	112	112
On-Chip User ROM (Bytes)	None	2K
External Bus	Yes	None
Bidirectional I/O Lines	16	32
Unidirectional I/O Lines	None	None
Other I/O Features	Timer	Timer
EPROM Version	None	None
STOP and WAIT	Yes	Yes

	CDP6805F2
Technology	CMOS
Number of Pins	28
On-Chip RAM (Bytes)	64
On-Chip User ROM (Bytes)	1K
External Bus	None
Bidirectional I/O Lines	20
Unidirectional I/O Lines	None
Other I/O Lines	Timer
EPROM Version	None
STOP and WAIT	Yes

OPERATING AND HANDLING CONSIDERATIONS

1. Handling

All inputs and outputs of RCA CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in ICAN-6525, "Guide to Better Handling and Operation of CMOS Integrated Circuits."

2. Operating

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause $V_{DD} - V_{SS}$ to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{CC} nor less than V_{SS} . Input currents must not exceed 10 mA even when the power supply is off.

Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{CC} or V_{SS} , whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} , V_{CC} , or V_{SS} may damage CMOS devices by exceeding the maximum device dissipation.

ORDERING INFORMATION

RCA Microprocessor device packages are identified by letters indicated in the following chart. When ordering a Microprocessor device, it is important that the appropriate suffix letter be affixed to the type number of the device.

Package	Suffix Letter
Dual-in-Line Side Brazed Ceramic	D
Dual-in-Line Plastic	E

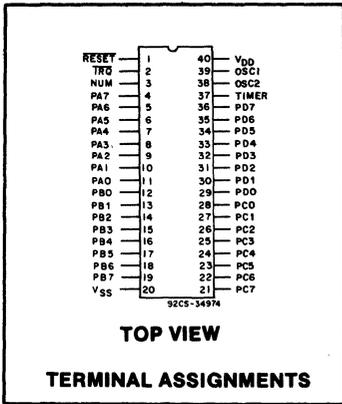
For example, a CDP6805F2 in a dual-in-line plastic package will be identified as the CDP6805F2E.

Objective Data

CMOS High-Performance Silicon-Gate 8-Bit Microcomputer

Features:

- Typical full speed operating power of 15 mW at 5 V
- Typical WAIT mode power of 4 mW
- Typical STOP mode power of 25 μ A
- Fully static operation
- 112 bytes of on-chip RAM
- 2106 bytes of on-chip ROM
- 32 bidirectional I/O lines
- High current drive
- Internal 8-bit timer with software programmable 7-bit prescaler
- External timer input
- External and timer interrupts
- Self-check mode
- Master reset and power-on reset
- Single 3 to 6 volt supply
- On-chip oscillator with RC or crystal mask options
- 40-pin dual-in-line package
- Similar to the MC6800
- Efficient use of program space
- Versatile interrupt handling
- True bit manipulation
- Addressing modes with indexed addressing for tables
- Efficient instruction set
- Memory mapped I/O
- Most self-check routines user callable
- Two power saving standby modes



The CDP6805G2 Microcomputer Unit (MCU) belongs to the CDP6805 Family of Microcomputers. This 8-bit MCU contains on-chip oscillator CPU, RAM, ROM, I/O, and Timer. The fully static design allows operation at frequencies down to DC, further reducing its already low-

power consumption. It is a low-power processor designed for low-end to mid-range applications in the consumer, automotive, industrial, and communications markets where very low power consumption constitutes an important factor.

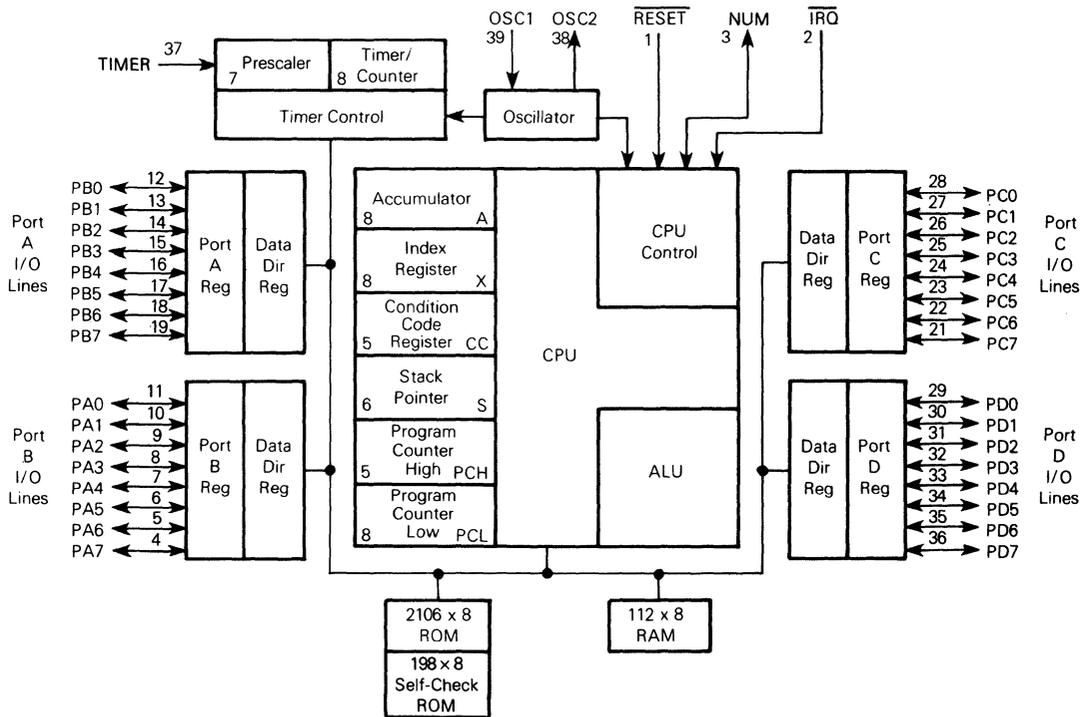


Fig. 1 - CDP6805G2 CMOS microcomputer block diagram.

RCA CMOS LSI Products

CDP6805G2

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Ratings	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.3 to +8.0	V
All Input Voltages Except OSC1	V_{in}	$V_{SS} - 0.5$ to $V_{DD} + 0.5$	V
Current Drain Per Pin Excluding V_{DD} and V_{SS}	I	10	mA
Operating Temperature Range	T_A	0 to +70	$^{\circ}C$
Storage Temperature Range	T_{stg}	-55 to +150	$^{\circ}C$
Current Drain Total (PD4-PD7 only)	I_{OH}	40	mA

THERMAL CHARACTERISTICS

Characteristics	Symbol	Value	Unit
Thermal Resistance Plastic	—	100	—
Ceramic	θ_{JA}	50	$^{\circ}C/W$

This device contains circuitry to protect the inputs against damage due to high static voltages of electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$. Reliability of operation is enhanced if unused inputs except OSC2 and NUM are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

Port	R_1	R_2
B and C	24.3 k Ω	4.32 k Ω
A, PD0-PD3	1.21 k Ω	3.1 k Ω
PD4-PD7	300 Ω	1.64 k Ω

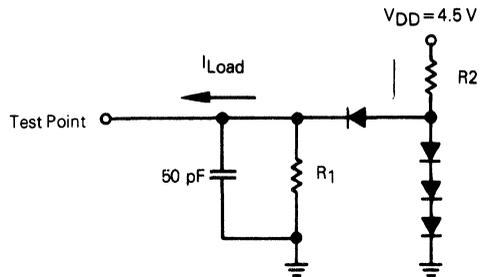


Fig. 2 - Equivalent test load.

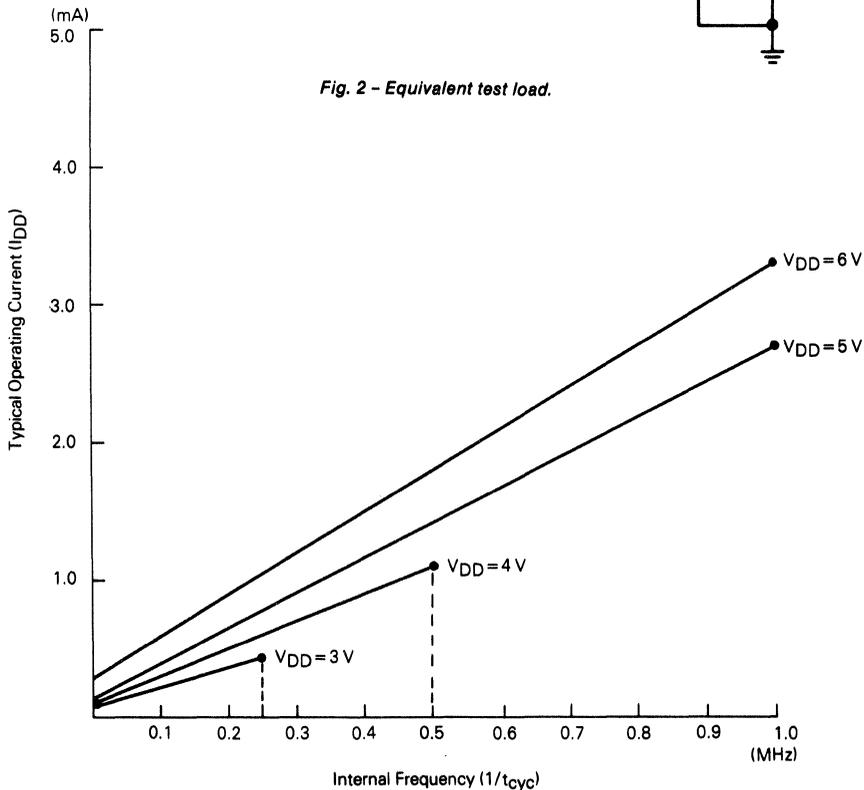


Fig. 3 - Typical operating current vs. internal frequency.

DC ELECTRICAL CHARACTERISTICS (See Note 2) ($V_{DD} = 5.0 \text{ Vdc} \pm 10\%$, $V_{SS} = 0 \text{ Vdc}$, $T_A = 0^\circ$ to 70°C unless otherwise noted)

Characteristics	Symbol	Min	Max	Unit
Output Voltage $I_{Load} \leq 10.0 \mu\text{A}$	V_{OL} V_{OH}	— $V_{DD} - 0.1$	0.1 —	V V
Output High Voltage ($I_{Load} = -100 \mu\text{A}$) PB0-PB7, PC0-PC7	V_{OH}	2.4	—	V
($I_{Load} = -2 \text{ mA}$) PA0-PA7, PD0-PD3	V_{OH}	2.4	—	V
($I_{Load} = -8 \text{ mA}$) PD4-PD7	V_{OH}	2.4	—	V
Output Low Voltage ($I_{Load} = 800 \mu\text{A}$) All Ports PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD7	V_{OL}	—	0.4	V
Input High Voltage Ports PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD7	V_{IH}	$V_{DD} - 2.0$	V_{DD}	V
TIMER, $\overline{\text{IRQ}}$, RESET	V_{IH}	$V_{DD} - 0.8$	V_{DD}	V
OSC1	V_{IH}	$V_{DD} - 0.8$	V_{DD}	V
Input Low Voltage All Inputs	V_{IL}	V_{SS}	0.8	V
Total Supply Current ($C_L = 50 \text{ pF}$ on Ports, no dc Loads, $t_{cyc} = 1 \mu\text{s}$) RUN (measured during self-check, $V_{IL} = 0.2 \text{ V}$, $V_{IH} = V_{DD} - 0.2 \text{ V}$)	I_{DD}	—	6	mA
WAIT (See Note 1)	I_{DD}	—	3	mA
STOP (See Note 1)	I_{DD}	—	250	μA
I/O Ports Input Leakage PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD7	I_{IL}	—	± 10	μA
Input Current RESET, $\overline{\text{IRQ}}$, TIMER, OSC1	I_{in}	—	± 1	μA
Capacitance Ports	C_{out}	—	12	pF
RESET, $\overline{\text{IRQ}}$, TIMER, OSC1	C_{in}	—	8	pF

NOTES: 1. Test conditions for I_{DD} are as follows:

All ports programmed as inputs

$V_{IL} = 0.2 \text{ V}$ (PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD7)

$V_{IH} = V_{DD} - 0.2 \text{ V}$ for RESET, $\overline{\text{IRQ}}$, TIMER

OSC1 input is a squarewave from 0.2 V to $V_{DD} - 0.2 \text{ V}$

OSC2 output load = 20 pF (wait I_{DD} is affected linearly by the OSC2 capacitance).

2. Electrical Characteristics for $V_{DD} = 3 \text{ V}$ available soon.

TABLE 1 — CONTROL TIMING

($V_{DD} = 5 \text{ Vdc} \pm 10\%$, $V_{SS} = 0$, $T_A = 0^\circ$ to 70°C , $f_{osc} = 4 \text{ MHz}$)

Characteristics	Symbol	Min	Max	Unit
Crystal Oscillator Startup Time (Figure 5)	t_{OXOV}	—	100	ms
Stop Recovery Startup Time (Crystal Oscillator) (Figure 6)	t_{ILCH}	—	100	ms
Timer Pulse Width (Figure 4)	t_{TH} , t_{TL}	0.5	—	t_{cyc}
Reset Pulse Width (Figure 5)	t_{RL}	1.5	—	t_{cyc}
Timer Period (Figure 4)	t_{TLTL}	1	—	t_{cyc}
Interrupt Pulse Width Low (Figure 15)	t_{LILH}	1	—	t_{cyc}
Interrupt Pulse Period (Figure 15)	t_{LILL}	*	—	t_{cyc}
OSC1 Pulse Width	t_{OH} , t_{OL}	100	—	ns
Cycle Time	t_{cyc}	1000	—	ns
Frequency of Operation				
Crystal	f_{osc}	—	4	MHz
External Clock	f_{osc}	DC	4	MHz

*The minimum period t_{LILL} should not be less than the number of t_{cyc} cycles it takes to execute the interrupt service routines plus 20 t_{cyc} cycles.

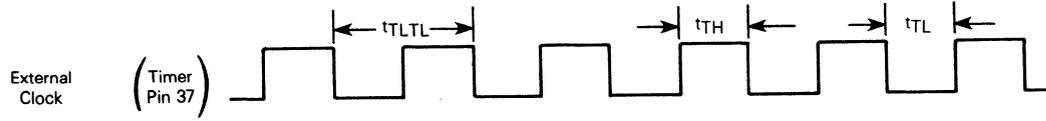
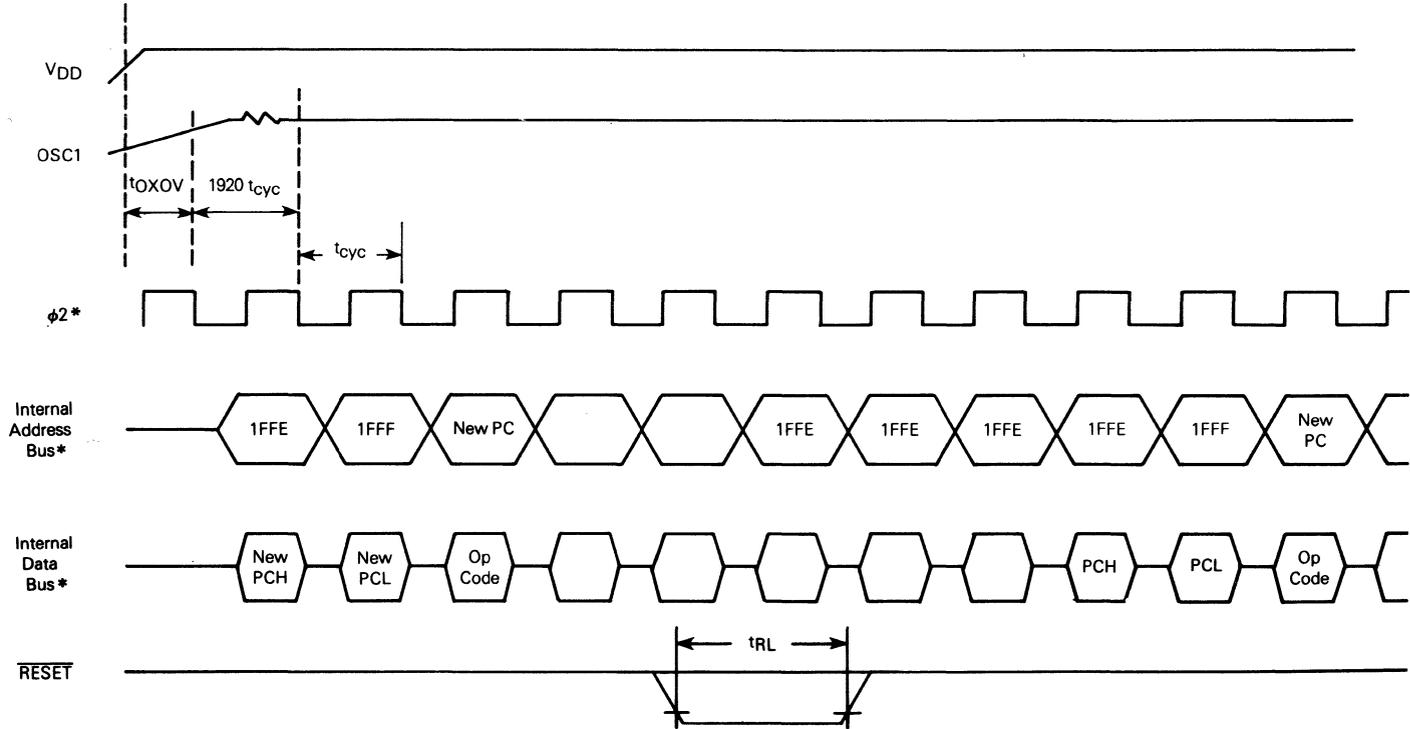
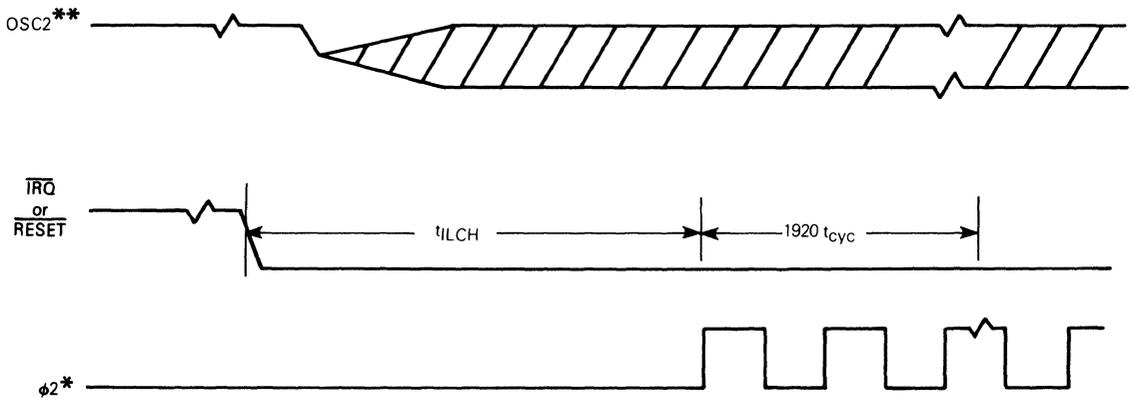


Fig. 4 - Timer relationships.



* Internal timing signal not available externally.

Fig. 5 - Power-on RESET and $\overline{\text{RESET}}$.



* Internal timing signals not available externally.

** Represents the internal gating of the OSC1 input pin.

Fig. 6 - Stop recovery and power-on RESET.

FUNCTIONAL PIN DESCRIPTION

V_{DD} and V_{SS}

Power is supplied to the MCU using these two pins. V_{DD} is power and V_{SS} is ground.

IRQ (MASKABLE INTERRUPT REQUEST)

IRQ is mask option selectable with the choice of interrupt sensitivity being both level- and negative-edge or negative-edge only. The MCU completes the current instruction before it responds to the request. If IRQ is low and the interrupt mask bit (I bit) in the condition code register is clear, the MCU begins an interrupt sequence at the end of the current instruction.

If the mask option is selected to include level sensitivity, then the IRQ input requires an external resistor to V_{DD} for "wire-OR" operation. See the Interrupt section for more detail.

RESET

The RESET input is not required for start-up but can be used to reset the MCU's internal state and provide an orderly software start-up procedure. Refer to the Reset section for a detailed description.

TIMER

The TIMER input may be used as an external clock for the on-chip timer. Refer to Timer section for a detailed description.

NUM - NON-USER MODE

This pin is intended for use in self-check only. User applications should connect this pin to ground through a 10 kΩ resistor.

OSC1, OSC2

The CDP6805G2 can be configured to accept either a crystal input or an RC network. Additionally, the internal clocks can be derived by either a divide-by-two or divide-by-four of the external frequency (f_{OSC}). Both of these options are mask selectable.

RC - If the RC oscillator option is selected, then a resistor is connected to the oscillator pins as shown in Figure 7(b). The relationship between R and f_{OSC} is shown in Figure 8.

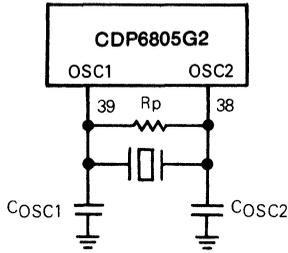
CRYSTAL - The circuit shown in Figure 7(a) is recommended when using a crystal. The internal oscillator is designed to interface with an AT-cut parallel resonant quartz crystal resonator in the frequency range specified for f_{OSC} in the electrical characteristics table. Using an external CMOS oscillator is suggested when crystals outside the specified ranges are to be used. The crystal and components should be mounted as close as possible to the input pins to minimize output distortion and start-up stabilization time. Crystal frequency limits are also affected by V_{DD}. Refer to Control Timing Characteristics for limits. See Table 1.

EXTERNAL CLOCK - An external clock should be applied to the OSC1 input with the OSC2 input not connected, as shown in Figure 7(c). An external clock may be used with either the RC or crystal oscillator mask option. t_{OXOY} or t_{ILCH} do not apply when using an external clock input.

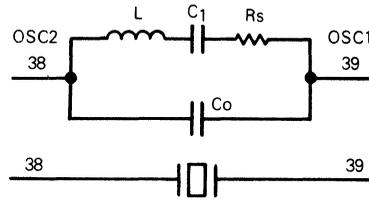
RCA CMOS LSI Products
CDP6805G2

	1 MHz	4 MHz	Units
R _S MAX	400	75	Ω
C ₀	5	7	pF
C ₁	0.008	0.012	μ F
C _{OSC1}	15-40	15-30	pF
C _{OSC2}	15-30	15-25	pF
R _P	10	10	M Ω
Q	30	40	—

Crystal Parameters

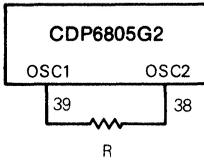


Crystal Oscillator Connections

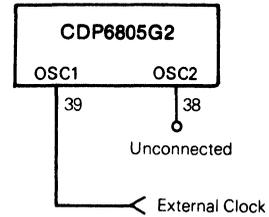


Equivalent Crystal Circuit

(a)



(b) RC Oscillator Connection



(c) External Clock Source Connections

Fig. 7 - Oscillator connections.

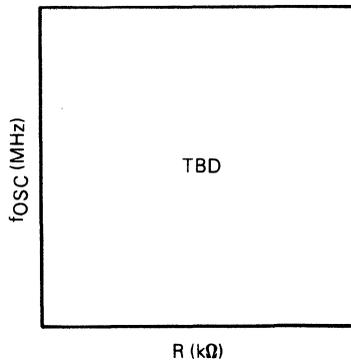


Fig. 8 - Frequency vs. resistance for RC oscillator option only.

PA0-PA7

These eight I/O lines comprise Port A. The state of any pin is software programmable. Refer to Input/Output Programming section for a detailed description.

PB0-PB7

These eight lines comprise Port B. The state of any pin is software programmable. Refer to Input/Output Programming section for a detailed description.

PC0-PC7

These eight lines comprise Port C. The state of any pin is software programmable. Refer to the Input/Output Programming section for a detailed description.

PD0-PD7

These eight lines comprise Port D. PD4-PD7 also are capable of driving LED's directly. The state of any pin is software programmable. Refer to the Input/Output Programming section for a detailed description.

INPUT/OUTPUT PROGRAMMING

Any port pin may be software programmed as an input or output by the state of the corresponding bit in the port Data Direction Register (DDR). A pin is configured as an output if its corresponding DDR bit is set to a logic '1.' A pin is configured as an input if its corresponding DDR bit is cleared to a logic '0.' At reset, all DDRs are cleared, which configures all port pins as inputs. A port pin configured as an output will output the data in the corresponding bit of its port data latch. Refer to Figure 9 and Table 2.

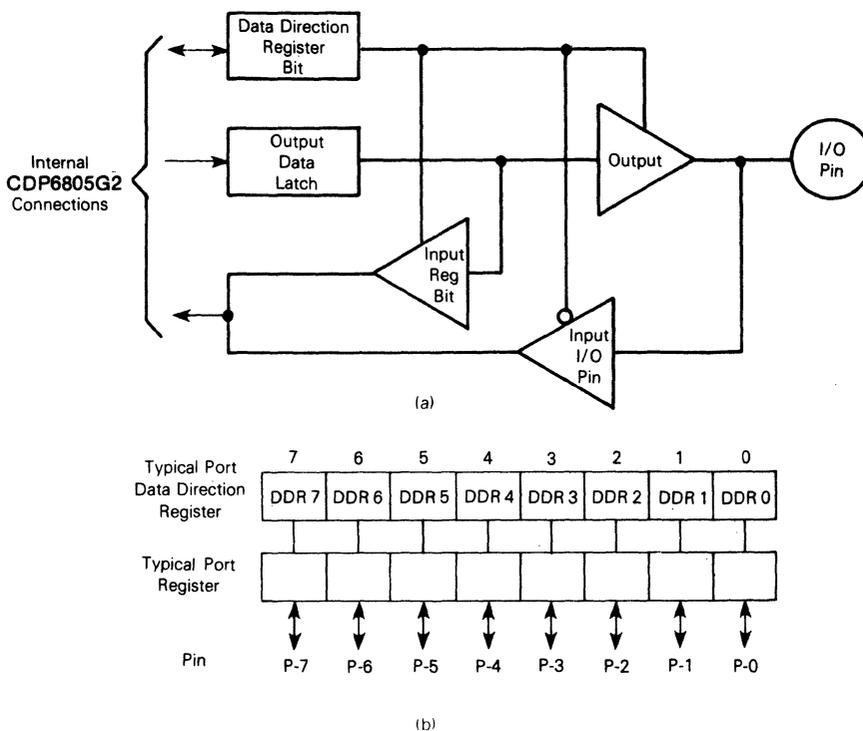


TABLE 2 - I/O PIN FUNCTIONS

R/W	DDR	I/O Pin Function
0	0	The I/O pin is in input mode. Data is written into the output data latch.
0	1	Data is written into the output data latch and output to the I/O pin.
1	0	The state of the I/O pin is read.
1	1	The I/O pin is in an output mode. The output data latch is read.

Fig. 9 - Typical port I/O circuitry.

CDP6805G2

SELF-CHECK

The CDP6805G2 self-check is performed using the circuit in Figure 10. Self-check is initiated by tying NUM and TIMER pins to a logic 1 then executing a reset. After reset, five subroutines are called that execute the following tests:

- I/O—Functionally exercise port A, B, C, D
- RAM—Walking bit test
- ROM—Exclusive OR with odd 1's parity result
- Timer—Functionally exercise timer
- Interrupts—Functionally exercise external and timer interrupts

Self-check results are shown in Table 3. The following subroutines are available to user programs and do not require any external hardware.

RAM SELF-CHECK SUBROUTINE

Returns with the Z-bit clear if any error is detected; otherwise the Z-bit is set.

The RAM test must be called with the stack pointer at \$07F. When run, the test checks every RAM cell except for \$07F and \$07E which are assumed to contain the return address.

A and X are modified. All RAM locations except the top 2 are modified. (Enter at location \$1FB7.)

ROM CHECKSUM SUBROUTINE

Returns with Z-bit cleared if any was found, otherwise Z = 1. X = 0 on return, and A is zero if the test passed. RAM locations \$040-\$043 are overwritten. (Enter at location 1FA1.)

TIMER TEST SUBROUTINE

Return with Z-bit cleared if any error was found; otherwise Z = 1.

This routine runs a simple test on the timer. In order to work correctly as a user subroutine, the internal clock must be the clocking source and interrupts must be disabled. Also, on exit, the clock will be running and the interrupt mask not set so the caller must protect himself from interrupts if necessary.

A and X register contents are lost; this routine counts how many times the clock counts in 128 cycles. The number of counts should be a power of two since the prescaler is a power of two. If not, the timer probably is not counting correctly. The routine also detects if the timer is running at all. (Enter at location \$1FBB.)

MEMORY

The CDP6805G2 has a total address space of 8192 bytes of memory and I/O registers. The address space is shown in Figure 11.

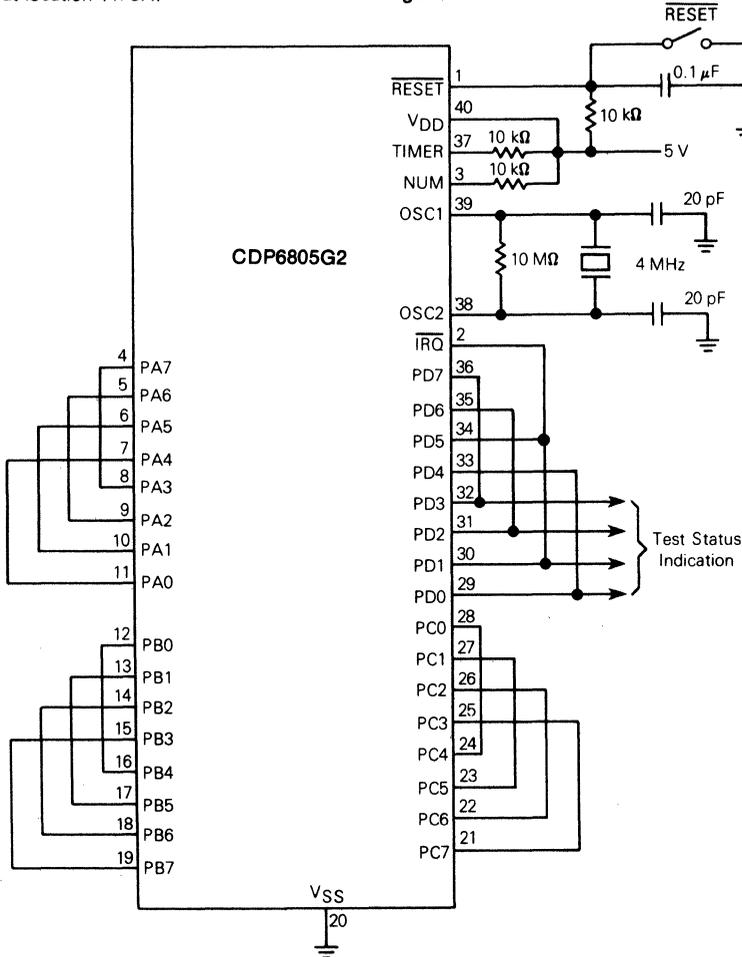
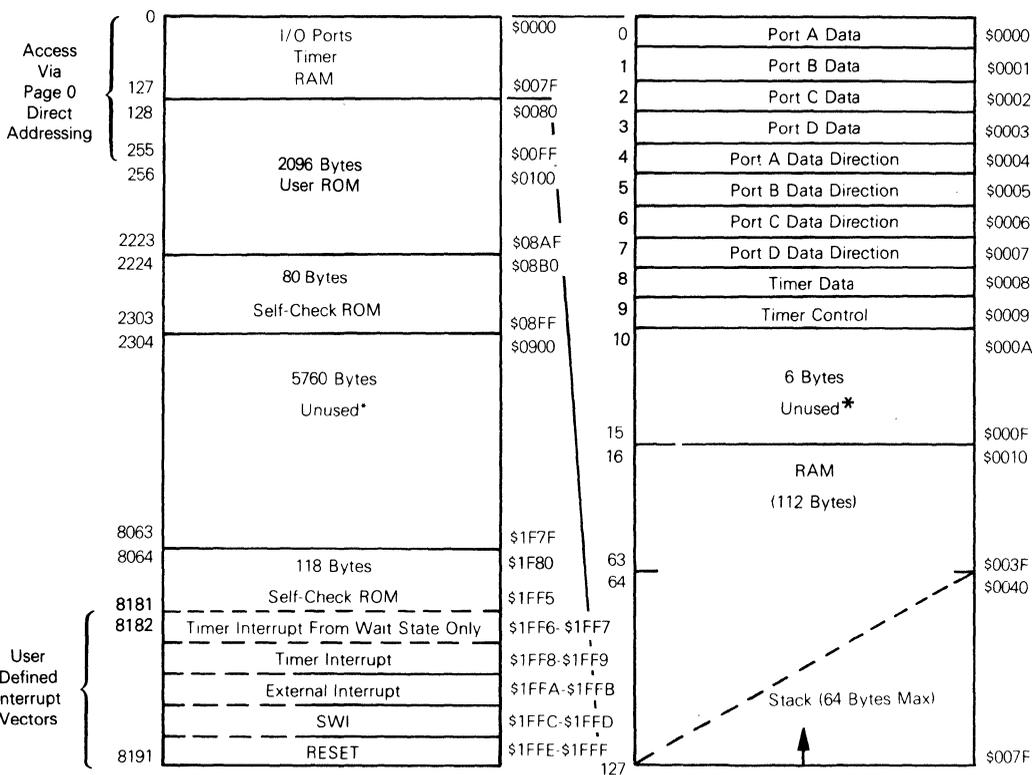


Fig. 10 - Self-check circuit.

TABLE 3 – SELF-CHECK RESULTS

PD3	PD2	PD1	PD0	Remarks
1	0	1	0	Bad I/O
1	0	1	1	Bad Timer
1	1	0	0	Bad RAM
1	1	0	1	Bad ROM
1	1	1	0	Bad Interrupt or Request Flag
All Cycling				Good Part
All Others				Bad Part



*Reads of unused locations undefined.

Fig. 11 – Address map.

CDP6805G2

The first 128 bytes of memory (first half of page zero) is comprised of the I/O port locations, timer locations, and 112 bytes of RAM. The next 2096 bytes comprise the user ROM. The 10 highest address bytes contain the reset and interrupt vectors.

The stack pointer is used to address data stored on the stack. Data is stored on the stack during interrupts and subroutine calls. At power-up, the stack pointer is set to \$007F and it is decremented as data is pushed on the stack. When data is removed from the stack, the stack pointer is incremented. A maximum of 64 bytes of RAM is available for stack usage. Since most programs use only a small part of the allocated stack locations for interrupts and/or subroutine stacking purposes, the unused bytes are usable for program data storage.

REGISTERS

The CDP6805G2 contains five registers as shown in the programming model in Figure 12. The interrupt stacking order is shown in Figure 13.

ACCUMULATOR (A)

This accumulator is an 8-bit general purpose register used for arithmetic calculations and data manipulations.

INDEX REGISTER (X)

The X register is an 8-bit register which is used during the indexed modes of addressing. It provides an 8-bit operand which is used to create an effective address. The index register is also used for data manipulations with the read/modify/write type of instructions and as a temporary storage register when not performing addressing operations.

PROGRAM COUNTER (PC)

The program counter is a 13-bit register that contains the address of the next instruction to be executed by the processor.

STACK POINTER (SP)

The stack pointer is a 13-bit register containing the address of the next free location on the stack. When accessing memory, the seven most-significant bits are permanently set to 0000001. These seven bits are appended to the six least-significant register bits to produce an address within the range of \$007F to \$0040. The stack area of RAM is used to store the return address on subroutine calls and the

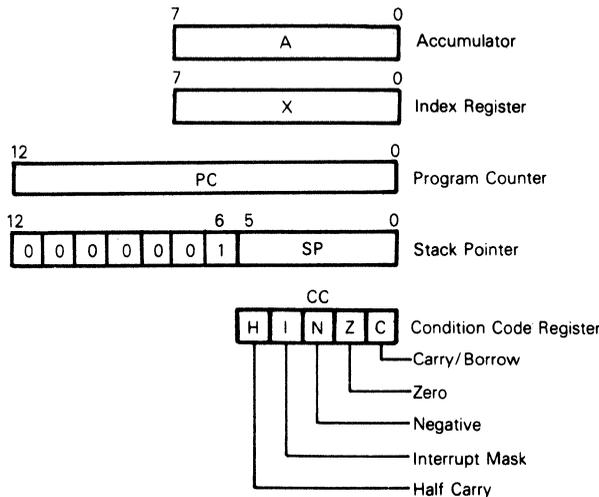
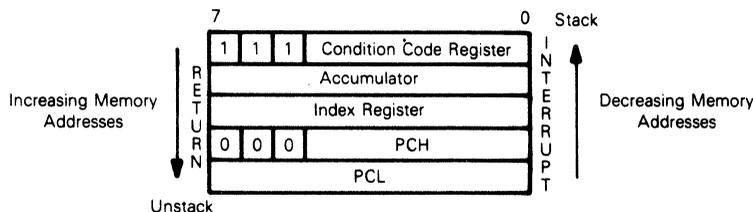


Fig. 12 - Programming Model.



NOTE: Since the Stack Pointer decrements during pushes, the PCL is stacked first, followed by PCH, etc. Pulling from the stack is in the reverse order.

Fig. 13 - Stacking order.

machine state during interrupts. During external or power-on reset, and during a "reset stack pointer" instruction, the stack pointer is set to its upper limit (\$007F). Nested interrupts and/or subroutines may use up to 64 (decimal) locations, beyond which the stack pointer "wraps around" and points to its upper limit thereby losing the previously stored information. A subroutine call occupies two RAM bytes on the stack, while an interrupt uses five bytes.

CONDITION CODE REGISTER (CC)

The condition code register is a 5-bit register which indicates the results of the instruction just executed. These bits can be individually tested by a program and specific action taken as a result of their state. Each bit is explained in the following paragraphs.

HALF CARRY BITS (H) — The H-bit is set to a one when a carry occurs between bits 3 and 4 of the ALU during an ADD or ADC instruction. The H-bit is useful in binary coded decimal subroutines.

INTERRUPT MASK BIT (I) — When the I-bit is set, both the external interrupt and the timer interrupt are disabled. Clearing this bit enables the above interrupts. If an interrupt occurs while the I-bit is set, the interrupt is latched and is processed when the I-bit is next cleared.

NEGATIVE (N) — Indicates that the result of the last arithmetic, logical, or data manipulation is negative (bit 7 in the result is a logical one).

ZERO (Z) — Indicates that the result of the last arithmetic, logical, or data manipulation is zero.

CARRY/BORROW (C) — Indicates that a carry or borrow out of the arithmetic logic unit (ALU) occurred during the last arithmetic operation. This bit is also affected during bit test and branch instructions, shifts, and rotates.

RESETS

The CDP6805G2 has two reset modes: an active low external reset pin (RESET) and a power-on reset function; refer to Figure 5.

RESET

The RESET input pin is used to reset the MCU to provide an orderly software start-up procedure. When using the external reset mode, the RESET pin must stay low for a minimum of one t_{CYC} . The RESET pin is provided with a Schmitt Trigger input to improve its noise immunity.

POWER-ON RESET

The power-on reset occurs when a positive transition is detected on VDD. The power-on reset is used strictly for power turn-on conditions and should not be used to detect any drops in the power supply voltage. There is no provision for a power-down reset. The power-on circuitry provides for a 1920 t_{CYC} delay from the time of the first oscillator operation. If the external RESET pin is low at the end of the 1920 t_{CYC} time out, the processor remains in the reset condition.

Either of the two types of reset conditions causes the following to occur:

- Timer control register interrupt request bit TCR7 is cleared to a "0."
- Timer control register interrupt mask bit TCR6 is set to a "1."
- All data direction register bits are cleared to a "0." All ports are defined as inputs.
- Stack pointer is set to \$007F.
- The internal address bus is forced to the reset vector (\$1FFE, \$1FFF).
- Condition code register interrupt mask bit (I) is set to a "1."
- STOP and WAIT latches are reset.
- External interrupt latch is reset.

All other functions, such as other registers (including output ports), the timer, etc., are not cleared by the reset conditions.

INTERRUPTS

The CDP6805G2 is capable of operation with three different interrupts, two hardware (timer interrupt and external interrupt), and one software (SWI). When any of these interrupts occur, normal processing is suspended at the end of the current instruction execution. All of the program registers (the machine state) are pushed onto the stack; refer to Figure 13 for stacking order. The appropriate vector pointing to the starting address of the interrupt service routine is then fetched; refer to Figure 14 for the interrupt sequence.

The priority of the various interrupts from highest to lowest is as follows:

RESET—*—External Interrupt—Timer Interrupt

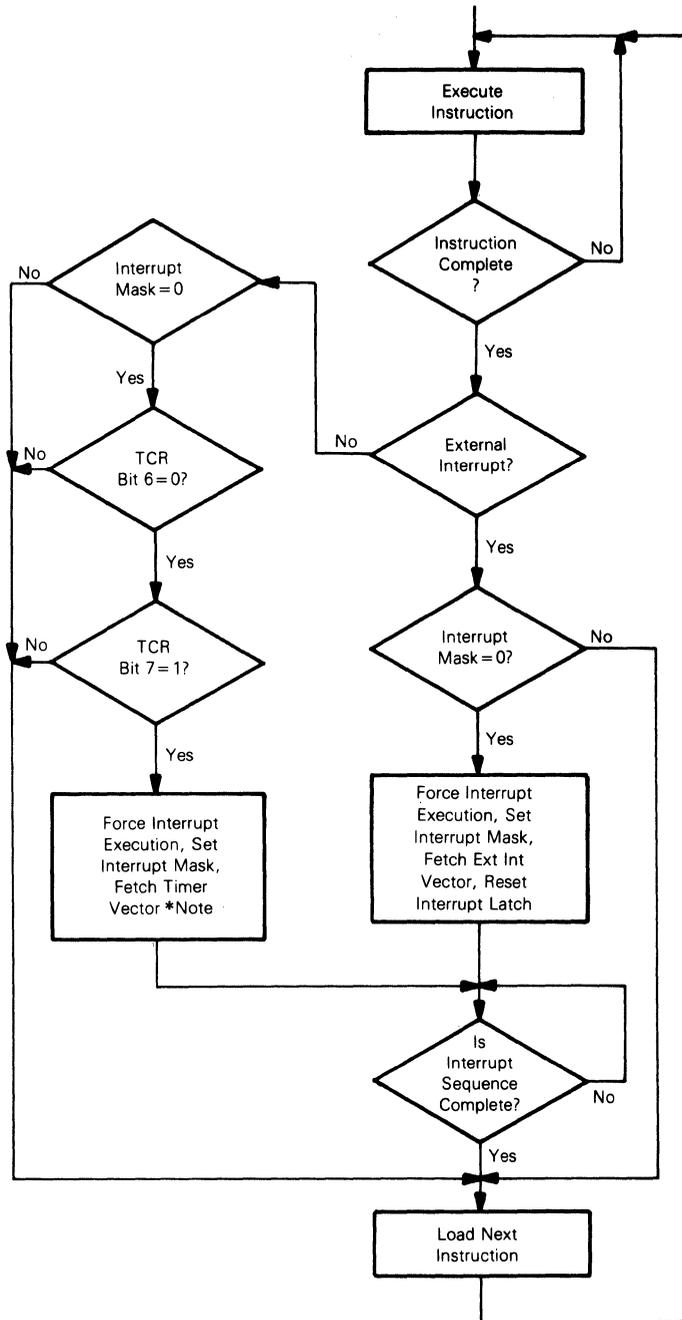
TIMER INTERRUPT

If the timer mask bit (TCR6) is cleared, then each time the timer decrements to zero (transitions from \$01 to \$00) an interrupt request is generated. The actual processor interrupt is generated only if the interrupt mask bit of the condition code register is also cleared. When the interrupt is recognized, the current state of the machine is pushed onto the stack and the interrupt mask bit in the condition code register is set. This masks further interrupts until the present one is serviced. The processor now vectors to the timer interrupt service routine. The address for this service routine is specified by the contents of \$1FF8 and \$1FF9 unless the processor is in a WAIT mode in which case the contents of \$1FF6 and \$1FF7 specify the timer service routine address. Software must be used to clear the timer interrupt request bit (TCR7). At the end of the timer interrupt service routine, the software normally executes an RTI instruction which restores the machine state and starts executing the interrupted program.

EXTERNAL INTERRUPT

If the interrupt mask bit of the condition code register is cleared and the external interrupt pin is "low," then the external interrupt occurs. The action of the external interrupt is

*Any current instruction including SWI.



*NOTE: The clear of TCR bit 7 must be accomplished with software.

Fig. 14 - Interrupt and instruction processing flowchart.

identical to the timer interrupt with the exception that the service routine address is specified by the contents of \$1FFA and \$1FFB. Either a level- and edge-sensitive (or edge-sensitive only) are available as mask options. Figure 15 shows both a functional diagram and timing for the interrupt line. The timing diagram shows two different treatments of the interrupt line (\overline{IRQ}) to the processor. The first method is single pulses on the interrupt line spaced far enough apart to be serviced. The minimum time between pulses is a function of the length of the interrupt service routine. Once a pulse occurs, the next pulse should not occur until the MPU software has exited the routine (an RTI occurs). This time (t_{LIL}) is obtained by adding 20 instruction cycles (t_{cyc}) to the total number of cycles it takes to complete the service routine including the RTI instruction; refer to Figure 15. The second configuration shows many interrupt lines "wire ORed" to form the interrupts at the processor. Thus, if after servicing an interrupt the \overline{IRQ} remains low, then the next interrupt is recognized.

SOFTWARE INTERRUPT (SWI)

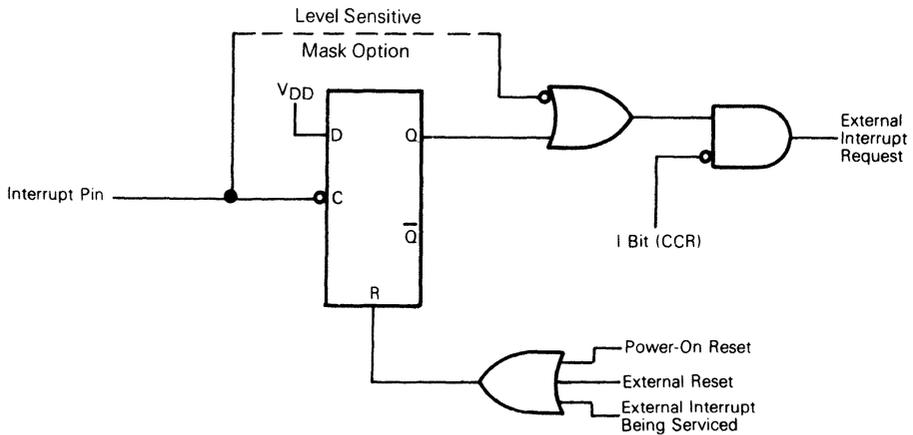
The software interrupt is an executable instruction. The action of the SWI instruction is similar to the hardware interrupts. The SWI is executed regardless of the state of the interrupt mask in the condition code register. The service routine address is specified by the contents of memory locations \$1FFC and \$1FFD. See Figure 14 for interrupt and instruction processing flowchart.

The following three functions are not strictly interrupts; however, they are tied very closely to the interrupts. These functions are **RESET**, **STOP**, **WAIT**.

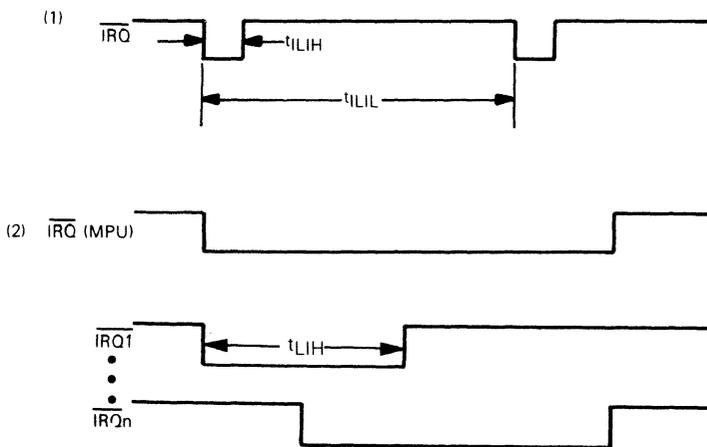
RESET

The **RESET** input pin and the internal power-on reset function each cause the program to vector to an initialization program. This vector is specified by the contents of memory locations \$1FFE and \$1FFF. The interrupt mask of the condition code register is also set. Refer to Resets section for details.

(a) Interrupt Functional Diagram



(b) Interrupt Mode Diagram



Edge Condition
(The minimum pulse width (t_{LIH}) is one t_{cyc} . The period t_{LIL} should not be less than the number of t_{cyc} cycles it takes to execute the interrupt service routine plus 20 t_{cyc} cycles.)

Mask Optional Level Sensitive
(If after servicing an interrupt the \overline{IRQ} remains low, then the next interrupt is recognized)

Fig. 15 - External interrupt.

CDP6805G2

STOP

The STOP instruction places the CDP6805G2 in its lowest power consumption mode. In the STOP function the internal oscillator is turned off, causing all internal processing and the timer to be halted; refer to Figure 16.

During the STOP mode, timer control register (TCR) bits 6 and 7 are altered to remove any pending timer interrupt requests and to disable any further timer interrupts. The timer prescaler is cleared. External interrupts are enabled in the condition code register. All other registers and memory remain unaltered. All I/O lines remain unchanged.

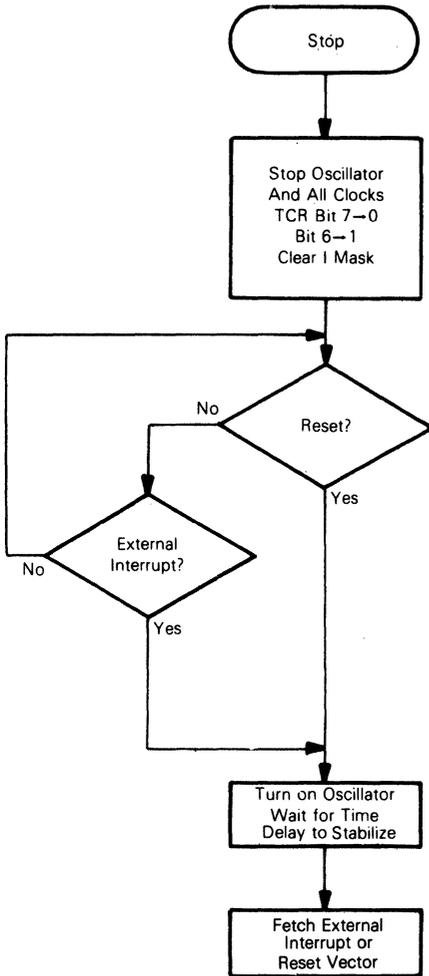


Fig. 16 - Stop function flowchart.

WAIT

The WAIT instruction places the CDP6805G2 in a low power consumption mode, but the WAIT mode consumes somewhat more power than the STOP mode. In the WAIT mode, the internal clock is disabled from all internal circuitry

except the timer circuit; refer to Figure 17. Thus, all internal processing is halted; however, the timer continues to count normally.

During the Wait mode, the I-bit in the condition code register is cleared to enable interrupts. All other registers, memory, and I/O lines remain in their last state. The timer may be enabled to allow a periodic exit from the Wait mode. If an external and a timer interrupt occur at the same time, the external interrupt is serviced first; then, if the timer interrupt request is not cleared in the external interrupt routine, the normal timer interrupt (not the timer Wait interrupt) is serviced since the MCU is no longer in the WAIT mode.

TIMER

The MCU timer contains a 8-bit software programmable counter with 7-bit software selectable prescaler. The counter may be present under program control and decrements towards zero. When the counter decrements to zero, the timer interrupt request bit, i.e., bit 7 of the timer control register (TRC), is set. Then, if the timer interrupt is not masked, i.e., bit 6 of the TCR and the I-bit in the condition code register are both cleared, the processor receives an interrupt. After completion of the current instruction, the processor proceeds to store the appropriate registers on the stack, and then fetches the timer vector address from locations \$1FF8 and \$1FF9 (or \$1FF6 and \$1FF7 if in the WAIT mode) in order to begin servicing.

The counter continues to count after it reaches zero, allowing the software to determine the number of internal or external input clocks since the timer interrupt request bit was set. The counter may be read at any time by the processor without disturbing the count. The contents of the counter becomes stable prior to the read portion of a cycle and does not change during the read. The timer interrupt request bit remains set until cleared by the software. If a read occurs before the timer interrupt is serviced, the interrupt is lost. TCR7 may also be used as a scanned status bit in a non-interrupt mode of operation (TCR6 = 1).

The prescaler is a 7-bit divider which is used to extend the maximum length of the timer. Bit 0, bit 1, and bit 2 of the TCR are programmed to choose the appropriate prescaler output which is used as the counter input. The processor cannot write into or read from the prescaler; however, its contents are cleared to all "0's" by the write operation into TCR when bit 3 of the written data equals 1. This allows for truncation-free counting.

The timer input can be configured for three different operating modes, plus a disable mode depending on the value written to the TCR4, TCR5 control bits. Refer to the Timer Control Register section.

TIMER INPUT MODE 1

If TCR4 and TCR5 are both programmed to a "0," the input to the timer is from an internal clock and the TIMER input pin is disabled. The internal clock mode can be used for periodic interrupt generation, as well as a reference in frequency and event measurement. The internal clock is the instruction cycle clock. During a WAIT instruction, the internal clock to the timer continues to run at its normal rate.

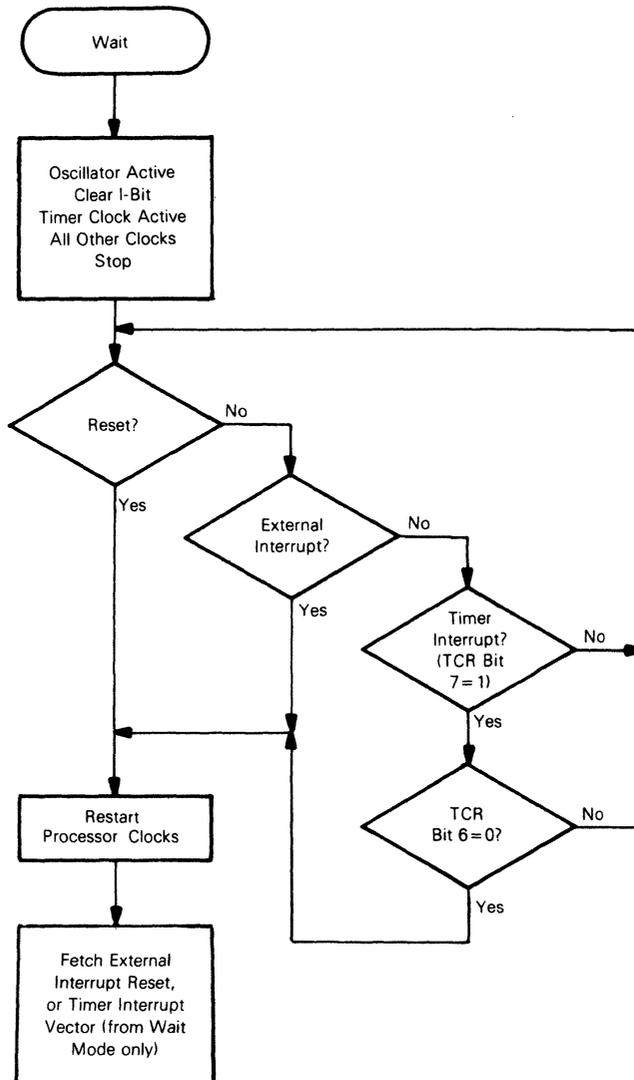


Fig. 17 - Wait function flowchart.

TIMER INPUT MODE 2

With TCR4=1 and TCR5=0, the internal clock and the TIMER input pin are ANDed together to form the timer input signal. This mode can be used to measure external pulse widths. The external pulse simply turns on the internal clock for the duration of the pulse. The resolution of the count in this mode is ± 1 clock and, therefore, accuracy improves with longer input pulse widths.

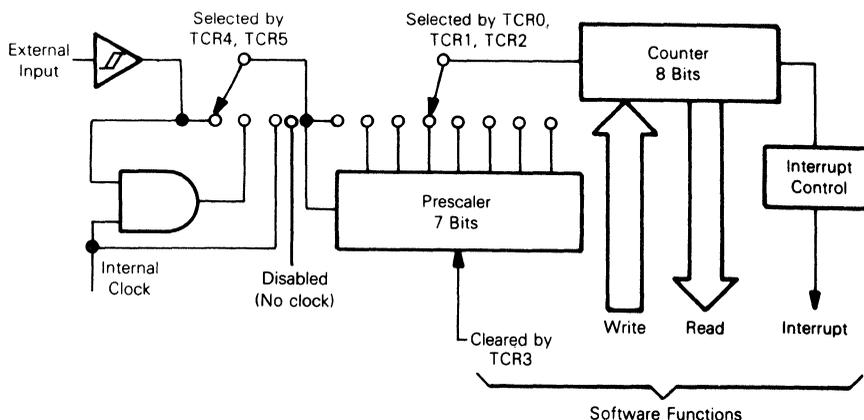
TIMER INPUT MODE 3

If TCR4=0 and TCR5=1, then all inputs to the Timer are disabled.

TIMER INPUT MODE 4

If TCR4=1 and TCR5=1, the internal clock input to the Timer is disabled and the TIMER input pin becomes the input to the Timer. The timer can, in this mode, be used to count external events as well as external frequencies for generating periodic interrupts. The counter is clocked on the falling edge of the external signal.

Figure 18 shows a block diagram of the Timer subsystem. Power-on Reset and the STOP instruction cause the counter to be set to \$F0.



NOTES:

1. Prescaler and 8-bit counter are clocked on the falling edge of the internal clock or external input.
2. Counter counts down continuously.

Fig. 18 - Timer block diagram.

Timer Control Register (TCR)

7	6	5	4	3	2	1	0
TCR7	TCR6	TCR5	TCR4	TCR3	TCR2	TCR1	TCR0

All bits in this register except bit 3 are Read/Write bits.

TCR7 — Timer interrupt request bit: bit used to indicate the timer interrupt when it is logic "1".

- 1 — Set whenever the counter decrements to zero, or under program control.
- 0 — Cleared on external reset, power-on reset, STOP instruction, or program control.

TCR6 — Timer interrupt mask bit: when this bit is a logic "1" it inhibits the timer interrupt to the processor.

- 1 — Set on external reset, power-on reset, STOP instruction, or program control.
- 0 — Cleared under program control.

TCR5 — External or internal bit: selects the input clock source to be either the external timer pin or the internal clock. (Unaffected by RESET.)

- 1 — Select external clock source.
- 0 — Select internal clock source (AS).

TCR4 — External enable bit: control bit used to enable the external timer pin. (Unaffected by RESET.)

- 1 — Enable external timer pin.
- 0 — Disable external timer pin.

TCR5 TCR4

0	0	Internal clock to Timer
0	1	AND of internal clock and TIMER pin to Timer
1	0	Inputs to Timer disabled
1	1	TIMER pin to Timer

Refer to Figure 18 for Logic Representation.

TCR3 — Timer Prescaler Reset bit: writing a "1" to this bit resets the prescaler to zero. A read of this location always indicates a "0". (Unaffected by RESET.)

TCR2, TCR1, TCR0 — Prescaler select bits: decoded to select one of eight taps on the prescaler. (Unaffected by RESET.)

Prescaler

TCR2	TCR1	TCR0	Result
0	0	0	+1
0	0	1	+2
0	1	0	+4
0	1	1	+8
1	0	0	+16
1	0	1	+32
1	1	0	+64
1	1	1	+128

INSTRUCTION SET

The MCU has a set of 61 basic instructions. They can be divided into five different types: register/memory, read/modify/write, branch, bit manipulation, and control. The following paragraphs briefly explain each type. All the instructions within a given type are presented in individual tables.

REGISTER/MEMORY INSTRUCTIONS

Most of these instructions use two operands. One operand is either the accumulator or the index register. The other operand is obtained from memory using one of the addressing modes. The operand for the jump unconditional (JMP) and jump to subroutine (JSR) instructions are the program counter. Refer to Table 4.

READ/MODIFY/WRITE INSTRUCTIONS

These instructions read a memory location or a register, modify or test its contents, and write the modified value back to memory or to the register. The test for negative or zero (TST) instruction is an exception to the read/modify/write sequence since it does not modify the value. Refer to Table 5.

BRANCH INSTRUCTIONS

Most branch instructions test the state of the Condition Code Register and if certain criteria are met, a branch is executed. This adds an offset between +128 and -127 to the current program counter. Refer to Table 6.

BIT MANIPULATION INSTRUCTIONS

The MPU is capable of setting or clearing any bit which resides in the first 256 bytes of the memory space, where all port registers, port DDR's, timer, timer control, and on-chip RAM reside. An additional feature allows the software to test and branch on the state of any bit within these 256 locations. The bit set, bit clear and bit test and branch functions are all implemented with a single instruction. For the test and branch instructions the value of the bit tested is also placed in the carry bit of the Condition Code Register. Refer to Table 7 for instruction cycle timing.

CONTROL INSTRUCTIONS

These instructions are register reference instructions and are used to control processor operation during program execution. Refer to Table 8 for instruction cycle timing.

ALPHABETICAL LISTING

The complete instruction set is given in alphabetical order in Table 10.

OPCODE MAP

Table 9 is an opcode map for the instructions used on the MCU.

ADDRESSING MODES

The MCU uses ten different addressing modes to give the programmer an opportunity to optimize the code to all situations. The various indexed addressing modes make it possible to locate data tables, code conversion tables and scaling tables anywhere in the memory space. Short indexed accesses are single byte instructions, while the longest instructions (three bytes) permit tables throughout memory. Short

and long absolute addressing is also included. One and two byte direct addressing instructions access all data bytes in most applications. Extended addressing permits jump instructions to reach all memory. Table 10 shows the addressing modes for each instruction, with the effects each instruction has on the Condition Code Register. An opcode map is shown in Table 9.

The term "Effective Address" (EA) is used in describing the various addressing modes, which is defined as the byte address to or from which the argument for an instruction is fetched or stored. The ten addressing modes of the processor are described below. Parentheses are used to indicate "contents of," an arrow indicates "is replaced by" and a colon indicates concatenation of two bytes. For additional details and graphical illustrations, refer to the M6805 Family User Manual.

INHERENT

In inherent instructions all the information necessary to execute the instruction is contained in the opcode. Operations specifying only the index register or accumulator, and no other arguments, are included in this mode.

IMMEDIATE

In immediate addressing, the operand is contained in the byte immediately following the opcode. Immediate addressing is used to access constants which do not change during program execution (e.g., a constant used to initialize a loop counter).

$$EA = PC + 1; PC - PC + 2$$

DIRECT

In the direct addressing mode, the effective address of the argument is contained in a single byte following the opcode byte. Direct addressing allows the user to directly address the lowest 256 bytes in memory with a single two byte instruction. This includes all on-chip RAM and I/O registers and 128 bytes of on-chip ROM. Direct addressing is efficient in both memory and time.

$$EA = (PC + 1); PC - PC + 2$$

$$\text{Address Bus High} - 0; \text{Address Bus Low} - (PC + 1)$$

EXTENDED

In the extended addressing mode, the effective address of the argument is contained in the two bytes following the opcode. Instructions with extended addressing modes are capable of referencing arguments anywhere in memory with a single three byte instruction. When using the CDP6805 assembler, the user need not specify whether an instruction uses direct or extended addressing. The assembler automatically selects the most efficient addressing mode.

$$EA = (PC + 1); (PC + 2); PC - PC + 3$$

$$\text{Address Bus High} - (PC + 1); \text{Address Bus Low} - (PC + 2)$$

INDEXED, NO-OFFSET

In the indexed, no offset addressing mode, the effective address of the argument is contained in the 8-bit index register. Thus, this addressing mode can access the first 256 memory locations. These instructions are only one byte long and therefore are more efficient. This mode is used to move a pointer through a table or to address a frequency referenced RAM or I/O location.

$$EA = X; PC - PC + 1$$

$$\text{Address Bus High} - 0; \text{Address Bus Low} - X$$

CDP6805G2**INDEXED, 8-BIT OFFSET**

Here the EA is obtained by adding the contents of the byte following the opcode to that of the index register. The operand is therefore located anywhere within the lowest 511 memory locations. For example, this mode of addressing is useful for selecting the m-th element in an n element table. All instructions are two bytes. The contents of the index register (X) is not changed. The contents of (PC+1) is an unsigned 8-bit integer. One byte offset indexing permits look-up tables to be easily accessed in either RAM or ROM.

$$EA = X + (PC + 1); PC - PC + 2$$

Address Bus High—K; Address Bus Low—X + (PC + 1)

Where: K = The carry from the addition of X + (PC + 1)

INDEXED, 16-BIT OFFSET

In the indexed, 16-bit offset addressing mode the effective address is the sum of the contents of the unsigned 8-bit index register and the two unsigned bytes following the opcode. This addressing mode can be used in a manner similar to indexed 8-bit offset, except that this three byte instruction allows tables to be anywhere in memory (e.g., jump tables in ROM). As with direct and extended, the M6805 assembler determines the most efficient form of indexed offset — 8 or 16 bit. The content of the index register is not changed.

$$EA = X + [(PC + 1):(PC + 2)]; PC - PC + 3$$

Address Bus High—(PC + 1) + K;

Address Bus Low—X + (PC + 2)

Where: K = The carry from the addition of X + (PC + 2)

RELATIVE

Relative addressing is only used in branch instructions. In relative addressing the contents of the 8-bit signed byte following the opcode (the offset) is added to the PC if and only if the branch condition is true. Otherwise, control proceeds to the next instruction. The span of relative addressing

is limited to the range of -126 to +129 bytes from the branch instruction opcode location. The Motorola assembler calculates the proper offset and checks to see if it is within the span of the branch.

$$EA = PC + 2 + (PC + 1); PC - EA \text{ if branch taken;}$$

otherwise PC - PC + 2

BIT SET/CLEAR

Direct addressing and bit addressing are combined in instructions which set and clear individual memory and I/O bits. In the bit set and clear instructions, the byte is specified as a direct address in the location following the opcode. The first 256 addressable locations are thus accessed. The bit to be modified within that byte is specified with three bits of the opcode. The bit set and clear instructions occupy two bytes, one for the opcode (including the bit number) and the second to address the byte which contains the bit of interest.

$$EA = (PC + 1); PC - PC + 2$$

Address Bus High—0; Address Bus Low—(PC + 1)

BIT TEST AND BRANCH

Bit test and branch is a combination of direct addressing, bit addressing and relative addressing. The bit address and condition (set or clear) to be tested is part of the opcode. The address of the byte to be tested is in the single byte immediately following the opcode byte (EA1). The signed relative 8-bit offset is in the third byte (EA2) and is added to the PC if the specified bit is set or clear in the specified memory location. This single three byte instruction allows the program to branch based on the condition of any bit in the first 256 locations of memory.

$$EA1 = (PC + 1)$$

Address Bus High—0; Address Bus Low—(PC + 1)

$$EA2 = PC + 3 + (PC + 2); PC - EA2 \text{ if branch taken;}$$

otherwise PC - PC + 3

TABLE 4 – REGISTER/MEMORY INSTRUCTIONS

		Addressing Modes																	
		Immediate			Direct			Extended			Indexed (No Offset)			Indexed (8-Bit Offset)			Indexed (16-Bit Offset)		
Function	Mnemonic	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles
Load A from Memory	LDA	A6	2	2	B6	2	3	C6	3	4	F6	1	3	E6	2	4	D6	3	5
Load X from Memory	LDX	AE	2	2	BE	2	3	CE	3	4	FE	1	3	EE	2	4	DE	3	5
Store A in Memory	STA	—	—	—	B7	2	4	C7	3	5	F7	1	4	E7	2	5	D7	3	6
Store X in Memory	STX	—	—	—	BF	2	4	CF	3	5	FF	1	4	EF	2	5	DF	3	6
Add Memory to A	ADD	AB	2	2	BB	2	3	CB	3	4	FB	1	3	EB	2	4	DB	3	5
Add Memory and Carry to A	ADC	A9	2	2	B9	2	3	C9	3	4	F9	1	3	E9	2	4	D9	3	5
Subtract Memory	SUB	A0	2	2	B0	2	3	C0	3	4	F0	1	3	E0	2	4	D0	3	5
Subtract Memory from A with Borrow	SBC	A2	2	2	B2	2	3	C2	3	4	F2	1	3	E2	2	4	D2	3	5
AND Memory to A	AND	A4	2	2	B4	2	3	C4	3	4	F4	1	3	E4	2	4	D4	3	5
OR Memory with A	ORA	AA	2	2	BA	2	3	CA	3	4	FA	1	3	EA	2	4	DA	3	5
Exclusive OR Memory with A	EOR	A8	2	2	B8	2	3	C8	3	4	F8	1	3	E8	2	4	D8	3	5
Arithmetic Compare A with Memory	CMP	A1	2	2	B1	2	3	C1	3	4	F1	1	3	E1	2	4	D1	3	5
Arithmetic Compare X with Memory	CPX	A3	2	2	B3	2	3	C3	3	4	F3	1	3	E3	2	4	D3	3	5
Bit Test Memory with A (Logical Compare)	BIT	A5	2	2	B5	2	3	C5	3	4	F5	1	3	E5	2	4	D5	3	5
Jump Unconditional	JMP	—	—	—	BC	2	2	CC	3	3	FC	1	2	EC	2	3	DC	3	4
Jump to Subroutine	JSR	—	—	—	BD	2	5	CD	3	6	FD	1	5	ED	2	6	DD	3	7

TABLE 5 – READ/MODIFY/WRITE INSTRUCTIONS

		Addressing Modes														
		Inherent (A)			Inherent (X)			Direct			Indexed (No Offset)			Indexed (8-Bit Offset)		
Function	Mnemonic	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles
Increment	INC	4C	1	3	5C	1	3	3C	2	5	7C	1	5	6C	2	6
Decrement	DEC	4A	1	3	5A	1	3	3A	2	5	7A	1	5	6A	2	6
Clear	CLR	4F	1	3	5F	1	3	3F	2	5	7F	1	5	6F	2	6
Complement	COM	43	1	3	53	1	3	33	2	5	73	1	5	63	2	6
Negate (2's Complement)	NEG	40	1	3	50	1	3	30	2	5	70	1	5	60	2	6
Rotate Left Thru Carry	ROL	49	1	3	59	1	3	39	2	5	79	1	5	69	2	6
Rotate Right Thru Carry	ROR	46	1	3	56	1	3	36	2	5	76	1	5	66	2	6
Logical Shift Left	LSL	48	1	3	58	1	3	38	2	5	78	1	5	68	2	6
Logical Shift Right	LSR	44	1	3	54	1	3	34	2	5	74	1	5	64	2	6
Arithmetic Shift Right	ASR	47	1	3	57	1	3	37	2	5	77	1	5	67	2	6
Test for Negative or Zero	TST	4D	1	3	5D	1	3	3D	2	4	7D	1	4	6D	2	5

TABLE 6 – BRANCH INSTRUCTIONS

Function	Mnemonic	Relative Addressing Mode		
		Op Code	# Bytes	# Cycles
Branch Always	BRA	20	2	3
Branch Never	BRN	21	2	3
Branch IFF Higher	BHI	22	2	3
Branch IFF Lower or Same	BLS	23	2	3
Branch IFF Carry Clear	BCC	24	2	3
(Branch IFF Higher or Same)	(BHS)	24	2	3
Branch IFF Carry Set	BCS	25	2	3
(Branch IFF Lower)	(BLO)	25	2	3
Branch IFF Not Equal	BNE	26	2	3
Branch IFF Equal	BEQ	27	2	3
Branch IFF Half Carry Clear	BHCC	28	2	3
Branch IFF Half Carry Set	BHCS	29	2	3
Branch IFF Plus	BPL	2A	2	3
Branch IFF Minus	BMI	2B	2	3
Branch IFF Interrupt Mask Bit is Clear	BMC	2C	2	3
Branch IFF Interrupt Mask Bit is Set	BMS	2D	2	3
Branch IFF Interrupt Line is Low	BIL	2E	2	3
Branch IFF Interrupt Line is High	BIH	2F	2	3
Branch to Subroutine	BSR	AD	2	6

TABLE 7 – BIT MANIPULATION INSTRUCTIONS

Function	Mnemonic	Addressing Modes					
		Bit Set/Clear			Bit Test and Branch		
		Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles
Branch IFF Bit n is Set	BRSET n (n=0...7)	—	—	—	2*n	3	5
Branch IFF Bit n is Clear	BRCLR n (n=0...7)	—	—	—	01+2*n	3	5
Set Bit n	BSET n (n=0...7)	10+2*n	2	5	—	—	—
Clear Bit n	BCLR n (n=0...7)	11+2*n	2	5	—	—	—

TABLE 8 – CONTROL INSTRUCTIONS

Function	Mnemonic	Inherent		
		Op Code	# Bytes	# Cycles
Transfer A to X	TAX	97	1	2
Transfer X to A	TXA	9F	1	2
Set Carry Bit	SEC	99	1	2
Clear Carry Bit	CLC	98	1	2
Set Interrupt Mask Bit	SEI	9B	1	2
Clear Interrupt Mask Bit	CLI	9A	1	2
Software Interrupt	SWI	83	1	10
Return from Subroutine	RTS	81	1	6
Return from Interrupt	RTI	80	1	9
Reset Stack Pointer	RSP	9C	1	2
No-Operation	NOP	9D	1	2
Stop	STOP	8E	1	2
Wait	WAIT	8F	1	2

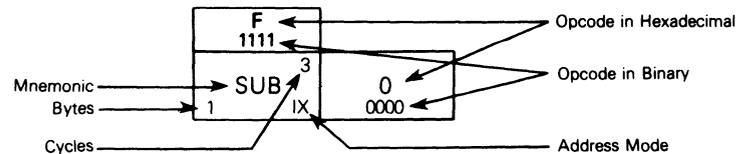
TABLE 9 — INSTRUCTION SET OPCODE MAP

Low	Hi	Bit Manipulation		Branch	Read/Modify/Write						Control		Register/Memory						Hi	Low
		BTB	BSC	REL	DIR	INH	INH	IX1	IX	INH	INH	IMM	DIR	EXT	IX2	IX1	IX			
		0 0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111			
0	0000	BRSET0 BTB	BSET0 BSC	BRA REL	NEG DIR	NEG INH	NEG IX1	NEG IX	RTI INH		SUB IMM	SUB DIR	SUB EXT	SUB IX2	SUB IX1	SUB IX	0 0000			
1	0001	BRCLR0 BTB	BCLR0 BSC	BRN REL					RTS INH		CMP IMM	CMP DIR	CMP EXT	CMP IX2	CMP IX1	CMP IX	1 0001			
2	0010	BRSET1 BTB	BSET1 BSC	BHI REL							SBC IMM	SBC DIR	SBC EXT	SBC IX2	SBC IX1	SBC IX	2 0010			
3	0011	BRCLR1 BTB	BCLR1 BSC	BLS REL	COM DIR	COMA INH	COMX INH	COM IX1	COM IX	SWI INH	CPX IMM	CPX DIR	CPX EXT	CPX IX2	CPX IX1	CPX IX	3 0011			
4	0100	BRSET2 BTB	BSET2 BSC	BCC REL	LSR DTR	LSRA INH	LSRX INH	LSR IX1	LSR IX		AND IMM	AND DIR	AND EXT	AND IX2	AND IX1	AND IX	4 0100			
5	0101	BRCLR2 BTB	BCLR2 BSC	BCS REL							BIT IMM	BIT DIR	BIT EXT	BIT IX2	BIT IX1	BIT IX	5 0101			
6	0110	BRSET3 BTB	BSET3 BSC	BNE REL	ROR DIR	RORA INH	RORX INH	ROR IX1	ROR IX		LDA IMM	LDA DIR	LDA EXT	LDA IX2	LDA IX1	LDA IX	6 0110			
7	0111	BRCLR3 BTB	BCLR3 BSC	BEQ REL	ASR DIR	ASRA INH	ASRX INH	ASR IX1	ASR IX	TAX INH		STA DIR	STA EXT	STA IX2	STA IX1	STA IX	7 0111			
8	1000	BRSET4 BTB	BSET4 BSC	BHCC REL	LSL DIR	LSLA INH	LSLX INH	LSL IX1	LSL IX	CLC INH	EOR IMM	EOR DIR	EOR EXT	EOR IX2	EOR IX1	EOR IX	8 1000			
9	1001	BRCLR4 BTB	BCLR4 BSC	BHCS REL	ROL DIR	ROLA INH	ROLX INH	ROL IX1	ROL IX	SEC INH	ADC IMM	ADC DIR	ADC EXT	ADC IX2	ADC IX1	ADC IX	9 1001			
A	1010	BRSET5 BTB	BSET5 BSC	BPL REL	DEC DIR	DECA INH	DECX INH	DEC IX1	DEC IX	CLI INH	ORA IMM	ORA DIR	ORA EXT	ORA IX2	ORA IX1	ORA IX	A 1010			
B	1011	BRCLR5 BTB	BCLR5 BSC	BMI REL						SEI INH	ADD IMM	ADD DIR	ADD EXT	ADD IX2	ADD IX1	ADD IX	B 1011			
C	1100	BRSET6 BTB	BSET6 BSC	BMC REL	INC DIR	INCA INH	INCX INH	INC IX1	INC IX	RSP INH		JMP DIR	JMP EXT	JMP IX2	JMP IX1	JMP IX	C 1100			
D	1101	BRCLR6 BTB	BCLR6 BSC	BMS REL	TST DIR	TSTA INH	TSTX INH	TST IX1	TST IX	NOP INH	BSR REL	JSR DIR	JSR EXT	JSR IX2	JSR IX1	JSR IX	D 1101			
E	1110	BRSET7 BTB	BSET7 BSC	BIL REL					STOP INH		LDX IMM	LDX DIR	LDX EXT	LDX IX2	LDX IX1	LDX IX	E 1110			
F	1111	BRCLR7 BTB	BCLR7 BSC	BIH REL	CLR DIR	CLRA INH	CLR INH	CLR IX1	CLR IX	WAIT INH	TXA INH	STX DIR	STX EXT	STX IX2	STX IX1	STX IX	F 1111			

Abbreviations for Address Modes

- INH Inherent
- A Accumulator
- X Index Register
- IMM Immediate
- DIR Direct
- EXT Extended
- REL Relative
- BSC Bit Set/Clear
- BTB Bit Test and Branch
- IX Indexed (No Offset)
- IX1 Indexed, 1 Byte (8-Bit) Offset
- IX2 Indexed, 2 Byte (16-Bit) Offset

LEGEND



RCA CMOS LSI Products
CDP6805G2

TABLE 10 – INSTRUCTION SET

Mnemonic	Addressing Modes										Condition Codes				
	Inherent	Immediate	Direct	Extended	Relative	Indexed (No Offset)	Indexed (8 Bits)	Indexed (16 Bits)	Bit Set/Clear	Bit Test & Branch	H	I	N	Z	C
ADC		X	X	X		X	X	X			Λ	●	Λ	Λ	Λ
ADD		X	X	X		X	X	X			Λ	●	Λ	Λ	Λ
AND		X	X	X		X	X	X			●	●	Λ	Λ	●
ASL	X		X			X	X				●	●	Λ	Λ	Λ
ASR	X		X			X	X				●	●	Λ	Λ	Λ
BCC					X						●	●	●	●	●
BCLR									X		●	●	●	●	●
BCS					X						●	●	●	●	●
BEQ					X						●	●	●	●	●
BHCC					X						●	●	●	●	●
BHCS					X						●	●	●	●	●
BHI					X						●	●	●	●	●
BHS					X						●	●	●	●	●
BIH					X						●	●	●	●	●
BIL					X						●	●	●	●	●
BIT		X	X	X		X	X	X			●	●	Λ	Λ	●
BLO					X						●	●	●	●	●
BLS					X						●	●	●	●	●
BMC					X						●	●	●	●	●
BMI					X						●	●	●	●	●
BMS					X						●	●	●	●	●
BNE					X						●	●	●	●	●
BPL					X						●	●	●	●	●
BRA					X						●	●	●	●	●
BRN					X						●	●	●	●	●
BRCLR										X	●	●	●	●	Λ
BRSET										X	●	●	●	●	Λ
BSET									X		●	●	●	●	●
BSR					X						●	●	●	●	●
CLC	X										●	●	●	●	0
CLI	X										●	0	●	●	●
CLR	X		X								●	●	0	1	●
CMP		X	X	X		X	X	X			●	●	Λ	Λ	Λ
COM	X		X			X	X				●	●	Λ	Λ	1
CPX		X	X	X		X	X	X			●	●	Λ	Λ	Λ
DEC	X		X			X	X				●	●	Λ	Λ	●
EOR		X	X	X		X	X	X			●	●	Λ	Λ	●
INC	X		X			X	X				●	●	Λ	Λ	●
JMP			X	X		X	X	X			●	●	●	●	●
JSR			X	X		X	X	X			●	●	●	●	●
LDA		X	X	X		X	X	X			●	●	Λ	Λ	●
LDX		X	X	X		X	X	X			●	●	Λ	Λ	●
LSL	X		X			X	X				●	●	Λ	Λ	Λ
LSR	X		X			X	X				●	●	0	Λ	Λ
NEG	X		X			X	X				●	●	Λ	Λ	Λ
NOP	X										●	●	●	●	●
ORA		X	X	X		X	X	X			●	●	Λ	Λ	●
ROL	X		X			X	X				●	●	Λ	Λ	Λ
ROR	X		X			X	X				●	●	Λ	Λ	Λ
RSP	X										●	●	●	●	●
RTI	X										7	7	7	7	7
RTS	X										●	●	●	●	●
SBC		X	X	X		X	X	X			●	●	Λ	Λ	Λ
SEC	X										●	●	●	●	1
SEI	X										●	1	●	●	●
STA			X	X		X	X	X			●	●	Λ	Λ	●
STOP	X										●	0	●	●	●
STX			X	X		X	X	X			●	●	Λ	Λ	Λ
SUB		X	X	X		X	X	X			●	●	Λ	Λ	Λ
SWI	X										●	1	●	●	●
TAX	X										●	●	●	●	●
TST	X		X			X	X				●	●	Λ	Λ	Λ
TXA	X										●	●	●	●	●
WAIT	X										●	0	●	●	●

Condition Code Symbols

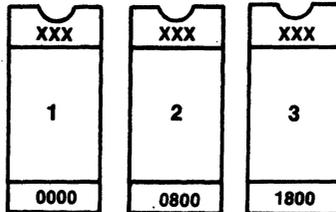
- | | | | |
|---|-------------------------|---|--|
| H | Half Carry (From Bit 3) | Λ | Test and Set if True. Cleared Otherwise. |
| I | Interrupt Mask | ● | Not Affected |
| N | Negative (Sign Bit) | ? | Load CC Register From Stack |
| Z | Zero | 0 | Cleared |
| C | Carry/Borrow | 1 | Set |

To minimize power consumption, all unused ROM locations should contain zeros.

Master-Device Method

EPROMs — 2716 EPROMs, programmed with the customer program (positive logic sense for address and data), may be submitted for pattern generation. Fill out Customer Information of ROM Information Sheet. The EPROMs must be clearly marked to indicate which EPROM corresponds to which

address mapping. Note that the first 128 (0000-007F) bytes of EPROM 1 correspond to the CDP6805G2 internal RAM and I/O ports and will be ignored when generating ROM masks. Only the first 176 (0000-00AF) bytes of EPROM 2 represent user ROM in the CDP6805G2 and all other locations are ignored. EPROM 3 may be replaced by filling out vector list on ROM Information Sheet since there are only 10 bytes. After the EPROMs are marked they should be placed in conductive IC carriers and securely packed. Do not use styrofoam.



XXX = Customer ID

Fig. A-1 - EPROM marking.

ROM INFORMATION SHEET

OPTION LIST

Select the options for your MCU from the following list. A manufacturing mask will be generated from this information. Select one in each section.

Internal Oscillator Input

- Crystal
- Resistor

Column 28 of Option Card

- 0 or N
- 1 or P

Internal Divide

- ÷ 4
- ÷ 2

Column 29 of Option Card

- 0 or N
- 1 or P

Interrupt

- Edge-Sensitive
- Level- and Edge-Sensitive

Column 30 of Option Card

- 0 or N
- 1 or P

VECTOR LIST

Timer Interrupt from Wait State Only _____

Timer Interrupt _____

External Interrupt _____

SWI _____

RESET _____

CUSTOMER INFORMATION

Customer Name _____

Address _____

City _____ State _____ Zip _____

Phone () _____ Extension _____

Contact Ms./Mr. _____

Customer Part No. _____

PATTERN MEDIA

- 6805G2
- EPROM
- Card Deck
- Other*

*Other media require factory approval.

Signature _____

Title _____

DATA PROGRAMMING INSTRUCTIONS

When a customer submits instructions for programming RCA custom ROM's, the customer must also complete the relevant parts of the ROM information sheet and submit this sheet together with the programming instructions. Programming instructions may be submitted in any one of three ways, as follows:

1. **Computer-Card Deck**—use standard 80-column computer punch cards.
2. **Floppy Diskette**—diskette information must be generated on an RCA CDP1800-series microprocessor development system.

3. **Master Device**—a ROM, PROM, EPROM or CDP6805G2 that contains the required programming information.

The requirements for each method are explained in detail in the following paragraphs:

Computer-Card Method

Use standard 80-column computer cards. Each card deck must contain, in order, a title card, an option card, a data-format card, and data cards. Punch the cards as specified in the following charts:

TITLE CARD

Column No.	Data
1	Punch T
2-5	leave blank
6-30	Customer Name (start at 6)
31-34	leave blank
35-54	Customer Address or Division (start at 35)
55-58	leave blank
59-63	RCA custom selection number (5 digits) (Obtained from RCA Sales Office)
64	leave blank
65-71	RCA device type, without CDP68 prefix, e.g. 05G2
72	Punch an opening parenthesis (
73	Punch 8
74	Punch a closing parenthesis)
75-78	leave blank
79-80	Punch a 2-digit decimal number to indicate the deck number; the first deck should be numbered 01

OPTION CARD

Use the ROM Information Sheet to select the polarity options, P, N, or X, for the desired ROM type.	
Column No.	Data
1-6	Punch the word OPTION
7	leave blank
8-17	RCA device type, including CDP68 prefix, e.g. CDP6805G2
18-27	leave blank
28-30	Punch P or N per ROM Information Sheet
31-78	leave blank
79-80	Punch the deck number (the 2-digit number in columns 79-80 of the title card)

DATA-FORMAT CARD

The data-format card specifies the form in which the data is to be entered into ROM.	
Column No.	Data
1-11	Punch the words DATA FORMAT
12	leave blank
13-15	Punch the letters HEX
16	leave blank
17-19	Punch POS
20-78	leave blank
79-80	Punch the deck number (the 2-digit number in columns 79-80 of the title card)

CDP6805 FAMILY

	Available Now	
	CDP6805E2	CDP6805G2
Technology	CMOS	CMOS
Number of Pins	40	40
On-Chip RAM (Bytes)	112	112
On-Chip User ROM (Bytes)	None	2K
External Bus	Yes	None
Bidirectional I/O Lines	16	32
Unidirectional I/O Lines	None	None
Other I/O Features	Timer	Timer
EPROM Version	None	None
STOP and WAIT	Yes	Yes

	CDP6805F2
Technology	CMOS
Number of Pins	28
On-Chip RAM (Bytes)	64
On-Chip User ROM (Bytes)	1K
External Bus	None
Bidirectional I/O Lines	20
Unidirectional I/O Lines	None
Other I/O Lines	Timer
EPROM Version	None
STOP and WAIT	Yes

OPERATING AND HANDLING CONSIDERATIONS

1. Handling

All inputs and outputs of RCA CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in ICAN-6525. "Guide to Better Handling and Operation of CMOS Integrated Circuits."

2. Operating

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause $V_{DD} - V_{SS}$ to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{CC} nor less than V_{SS} . Input currents must not exceed 10 mA even when the power supply is off.

Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{CC} or V_{SS} , whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} , V_{CC} , or V_{SS} may damage CMOS devices by exceeding the maximum device dissipation.

ORDERING INFORMATION

RCA Microprocessor device packages are identified by letters indicated in the following chart. When ordering a Microprocessor device, it is important that the appropriate suffix letter be affixed to the type number of the device.

Package	Suffix Letter
Dual-in-Line Side Brazed Ceramic	D
Dual-in-Line Plastic	E

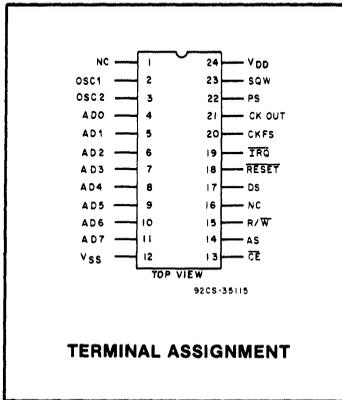
For example, a CDP6805G2 in a dual-in-line plastic package will be identified as the CDP6805G2E.

Objective Data

CMOS Real-Time Clock with RAM

Features:

- Low-Power, High-Speed, High-Density CMOS
- Internal Time Base and Oscillator
- Counts Seconds, Minutes, and Hours of the Day
- Counts Days of the Week, Date, Month, and Year
- 3 V to 6 V Operation
- Time Base Input Options: 4.194304 MHz, 1.048576 MHz, or 32.768 kHz
- Time Base Oscillator for Parallel Resonant Crystals
- 40 to 200 μ W Typical Operating Power at Low Frequency Time Base
- 4.0 to 20 mW Typical Operating Power at High Frequency Time Base
- Binary or BCD Representation of Time, Calendar, and Alarm
- 12- or 24-Hour Clock with AM and PM in 12-Hour Mode
- Daylight Savings Time Option
- Automatic End of Month Recognition
- Automatic Leap Year Compensation
- Microprocessor Bus Compatible
- MOTEL Circuit for Bus Universality
- Multiplexed Bus for Pin Efficiency
- Interfaced with Software as 64 RAM Locations
- 14 Bytes of Clock and Control Registers
- 50 Bytes of General Purpose RAM
- Status Bit Indicates Data Integrity
- Bus Compatible Interrupt Signals (\overline{IRQ})
- Three Interrupts are Separately Software Maskable and Testable
 - Time-of-Day Alarm, Once-per-Second to Once-per-Day
 - Periodic Rates from 30.5 μ s to 500 ms
 - End-of-Clock Update Cycle
- Programmable Square-Wave Output Signal
- Clock Output May Be Used as Microprocessor Clock Input
 - At Time Base Frequency +1 or +4
- 24-Pin Dual-In-Line Package
- Chip Carrier Also Available



The CDP6818 Real-Time Clock plus RAM is a peripheral device which includes the unique MOTEL concept for use with various microprocessor, microcomputers, and larger computers. This part combines three unique features: a complete time-of-day clock with alarm and one hundred year calendar, a programmable periodic interrupt and square-wave generator, and 50 bytes of low-power static RAM. The CDP6818 uses high-speed CMOS technology to interface with 1 MHz processor buses, while consuming very little power.

The Real-Time Clock plus RAM has two distinct uses. First, it is designed as a battery powered CMOS part (in an otherwise NMOS/TTL system) including all the common battery backed-up functions such as RAM, time, and calendar. Secondly, the CDP6818 may be used with a CMOS microprocessor to relieve the software of the timekeeping workload and to extend the available RAM of an MPU such as the CDP6805E2.

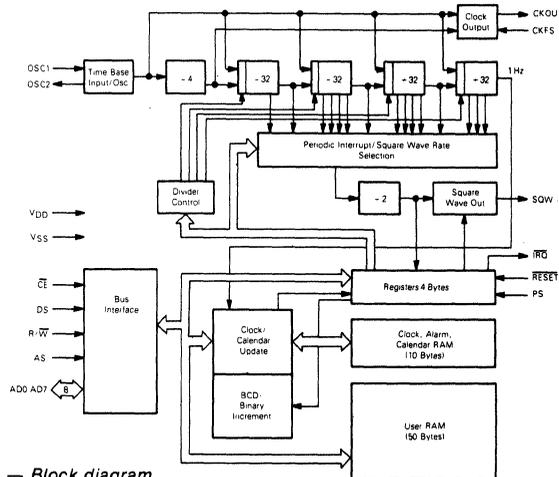


Fig. 1 — Block diagram.

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CDP6818

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Ratings	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.3 to +8	V
All Input Voltages Except OSC1	V_{in}	$V_{SS} - 0.5$ to $V_{DD} + 0.5$	V
Current Drain per Pin Excluding V_{DD} and V_{SS}	I	10	mA
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

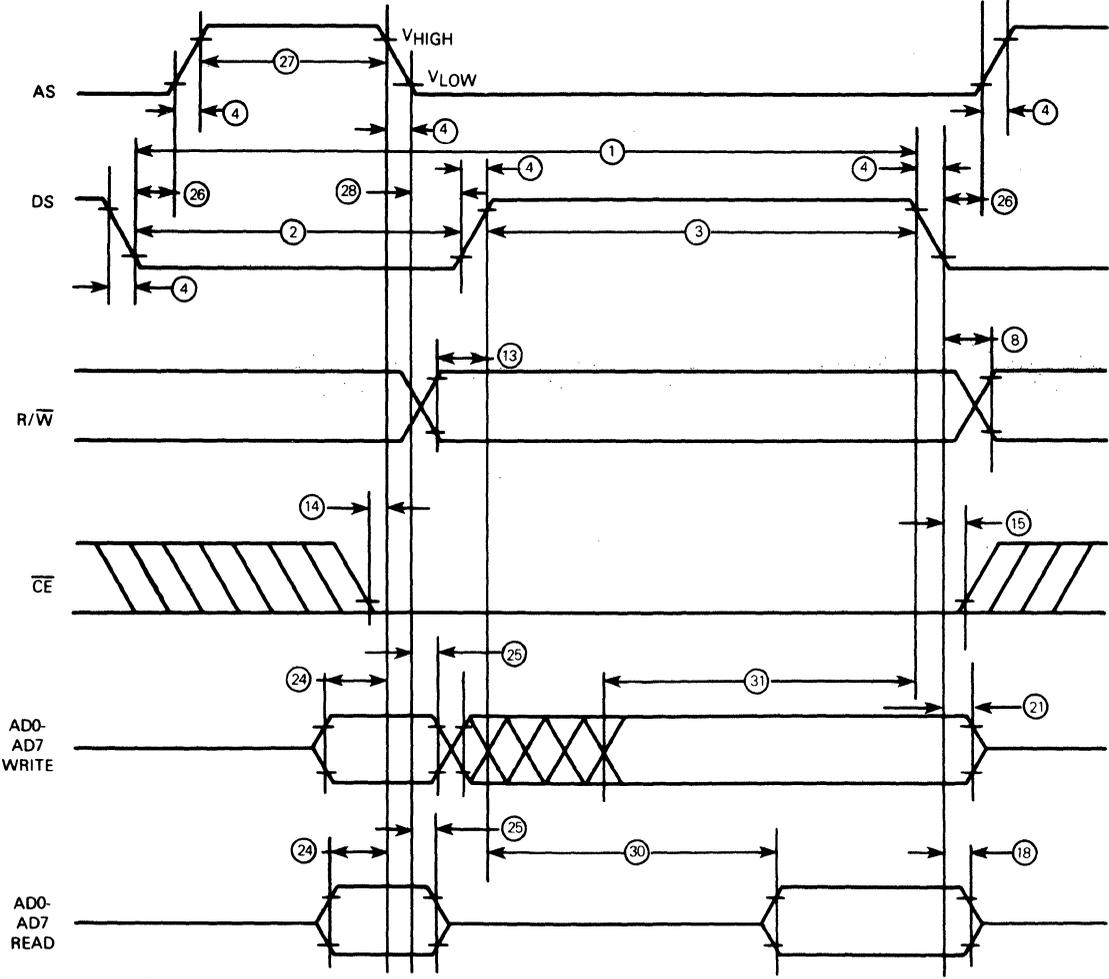
DC ELECTRICAL CHARACTERISTICS ($V_{DD} = 5 \text{ Vdc} \pm 10\%$, $V_{SS} = 0 \text{ Vdc}$, $T_A = 0^\circ$ to 70°C unless otherwise noted)

Characteristics	Symbol	Min	Max	Unit
Frequency of Operation	f_{osc}	32.768	4194.304	kHz
Output Voltage $I_{Load} < 10 \mu\text{A}$	V_{OL}	-	0.1	V
	V_{OH}	$V_{DD} - 0.1$	-	
$I_{DD} - \text{Bus Idle}$ CKOUT = f_{osc} , $C_L = 15 \text{ pF}$; SQW Disabled, $\overline{CE} = V_{DD} - 0.2$; $C_L (\text{OSC2}) = 10 \text{ pF}$ $f_{osc} = 4.194304 \text{ MHz}$ $f_{osc} = 1.048516 \text{ MHz}$ $f_{osc} = 32.768 \text{ kHz}$	I_{DD1} I_{DD2} I_{DD3}	- - -	5 2 200	mA mA μA
$I_{DD} - \text{Quiescent}$ $f_{osc} = \text{DC}$; OSC1 = DC; All Other Inputs = $V_{DD} - 0.2 \text{ V}$; No Clock	I_{DD4}	-	100	μA
Output High Voltage ($I_{Load} = -1.6 \text{ mA}$, All Outputs Except \overline{IRQ} , OSC2, and SQW, $I_{Load} = -1.0 \text{ mA}$)	V_{OH}	4.1	-	V
Output Low Voltage ($I_{Load} = 1.6 \text{ mA}$, All Outputs Except OSC2, \overline{IRQ} , and SQW, $I_{Load} = 1.0 \text{ mA}$)	V_{OL}	-	0.4	V
Input High Voltage CKFS, AD0-AD7, DS, AS, R/W, \overline{CE} , PS RESET OSC1	V_{IH}	$V_{DD} - 2$ $V_{DD} - 0.8$ $V_{DD} - 1$	V_{DD} V_{DD} V_{DD}	V
Input Low Voltage AD0-AD7, DS, AS, R/W, \overline{CE} CKFS, PS, RESET OSC1	V_{IL}	V_{SS} V_{SS} V_{SS}	0.8 0.8 0.8	V
Input Current All Inputs	I_{in}	-	± 1	μA
Three-State Leakage AD0-AD7	I_{TSL}	-	± 10	μA

BUS TIMING ($V_{DD} = 5 \text{ Vdc} \pm 10\%$, $V_{SS} = 0 \text{ Vdc}$, $T_A = 0^\circ$ to 70°C unless otherwise noted)

Ident. Number	Characteristics	Symbol	Min	Max	Unit
1	Cycle Time	t_{cyc}	953	DC	ns
2	Pulse Width, DS/E Low or $\overline{RD}/\overline{WR}$ High	PW_{EL}	300	-	ns
3	Pulse Width, DS/E High or $\overline{RD}/\overline{WR}$ Low	PW_{EH}	325	-	ns
4	Clock Rise and Fall Time	t_r, t_f	-	30	ns
8	R/W Hold Time	t_{RWH}	10	-	ns
13	R/W Setup Time Before DS/E	t_{RWS}	15	-	ns
14	Chip Enable Setup Time Before AS/ALE Fall	t_{CS}	55	-	ns
15	Chip Enable Hold Time	t_{CH}	0	-	ns
18	Read Data Hold Time	t_{DHR}	10	100	ns
21	Write Data Hold Time	t_{DHW}	0	-	ns
24	Muxed Address Valid Time to AS/ALE Fall	t_{ASL}	50	-	ns
25	Muxed Address Hold Time	t_{AHL}	50	-	ns
26	Delay Time DS/E to AS/ALE Rise	t_{ASD}	50	-	ns
27	Pulse Width, AS/ALE High	PW_{ASH}	100	-	ns
28	Delay Time, AS/ALE to DS/E Rise	t_{ASED}	90	-	ns
30	Peripheral Output Data Delay Time From DS/E or \overline{RD}	t_{DDR}	20	240	ns
31	Peripheral Data Setup Time	t_{DSW}	220	-	ns

Note: Designations E, ALE, \overline{RD} and \overline{WR} refer to signals from non-6805 type microprocessors.



NOTE: V_{HIGH} = V_{DD} - 2.0 V, V_{LOW} = 0.8 V, for V_{DD} = 5.0 V ± 10%

Fig. 2 — CDP6818 bus timing waveforms.

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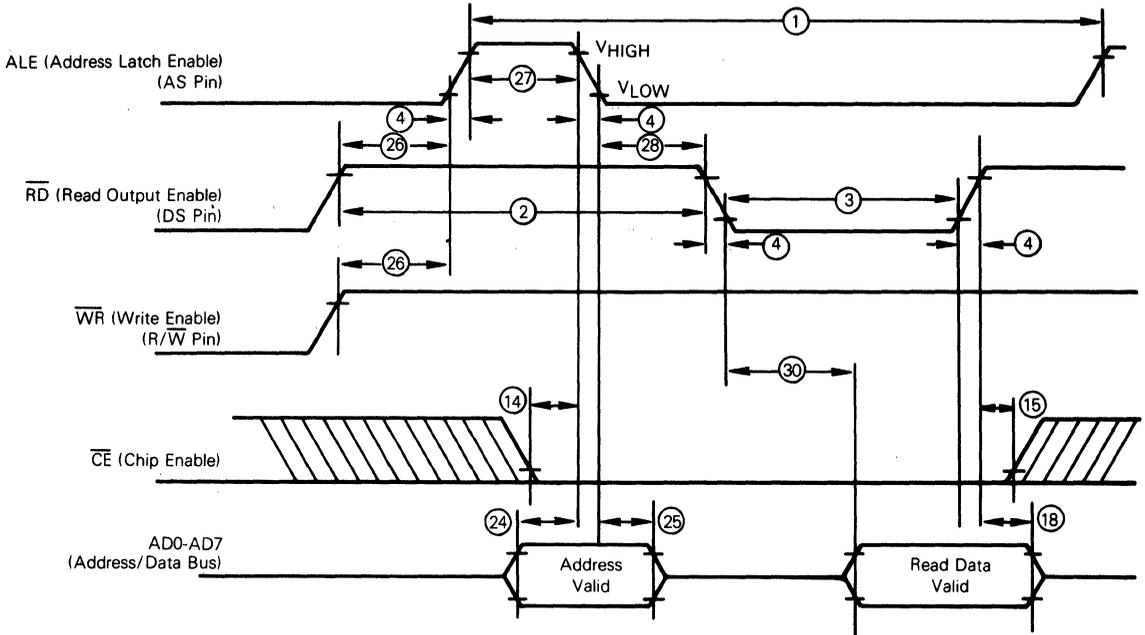
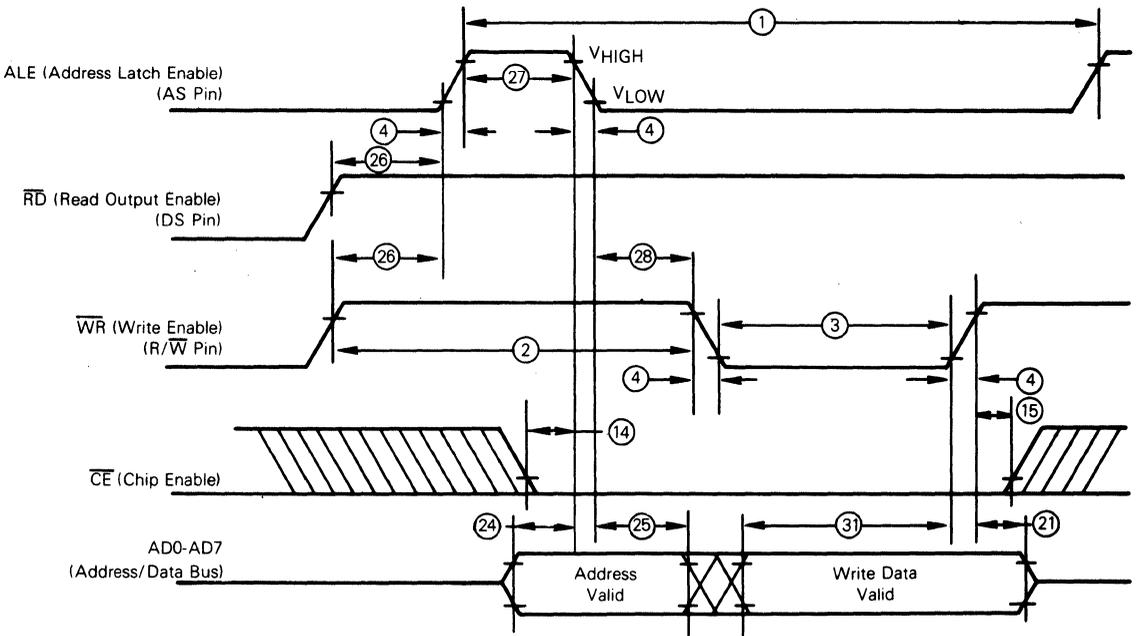


Fig. 3 — Bus-read timing competitor multiplexed bus.

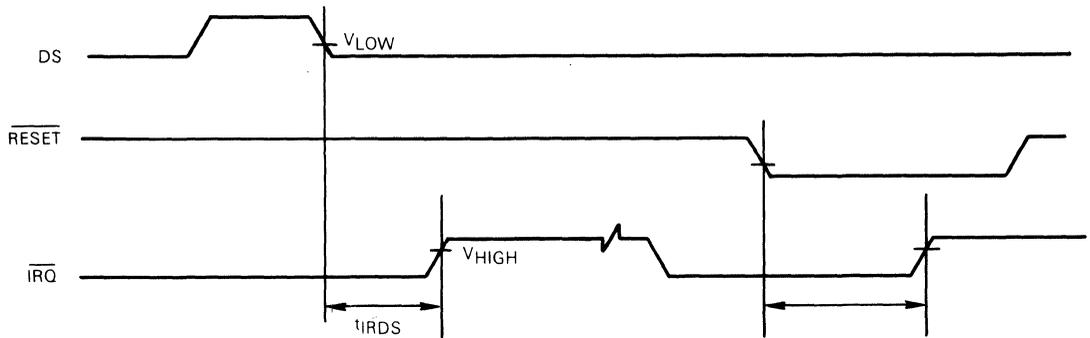


NOTE: $V_{HIGH} = V_{DD} - 2.0 \text{ V}$, $V_{LOW} = 0.8 \text{ V}$, for $V_{DD} = 5.0 \text{ V} \pm 10\%$

Fig. 4 — Bus-write timing competitor multiplexed bus.

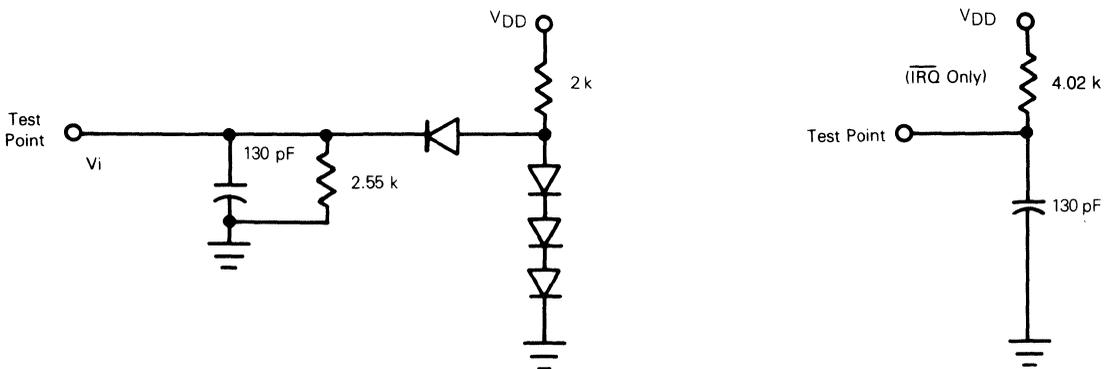
TABLE 1 — SWITCHING CHARACTERISTICS ($V_{DD}=5\text{ Vdc} \pm 10\%$, $V_{SS}=0\text{ Vdc}$, $T_A=0^\circ\text{ to }70^\circ\text{C}$)

Description	Symbol	Min	Max	Unit
Oscillator Startup	t_{RC}	—	100	ms
Reset Pulse Width	t_{RWL}	5	—	μs
Reset Delay Time	t_{RLH}	5	—	μs
Power Sense Pulse Width	t_{PWL}	5	—	μs
Power Sense Delay Time	t_{PLH}	5	—	μs
$\overline{\text{IRQ}}$ Release from DS	t_{IRDS}	2	—	μs
$\overline{\text{IRQ}}$ Release from $\overline{\text{RESET}}$	t_{IRR}	2	—	μs
VRT Bit Delay	t_{VRTD}	2	—	μs



NOTE: $V_{HIGH} = V_{DD} - 2.0\text{ V}$, $V_{LOW} = 0.8\text{ V}$, for $V_{DD} = 5.0\text{ V} \pm 10\%$

Fig. 5 — $\overline{\text{IRQ}}$ release delay timing waveforms.



All Outputs Except OSC2 (See Figure 10)

Fig. 6 — TTL equivalent test load.

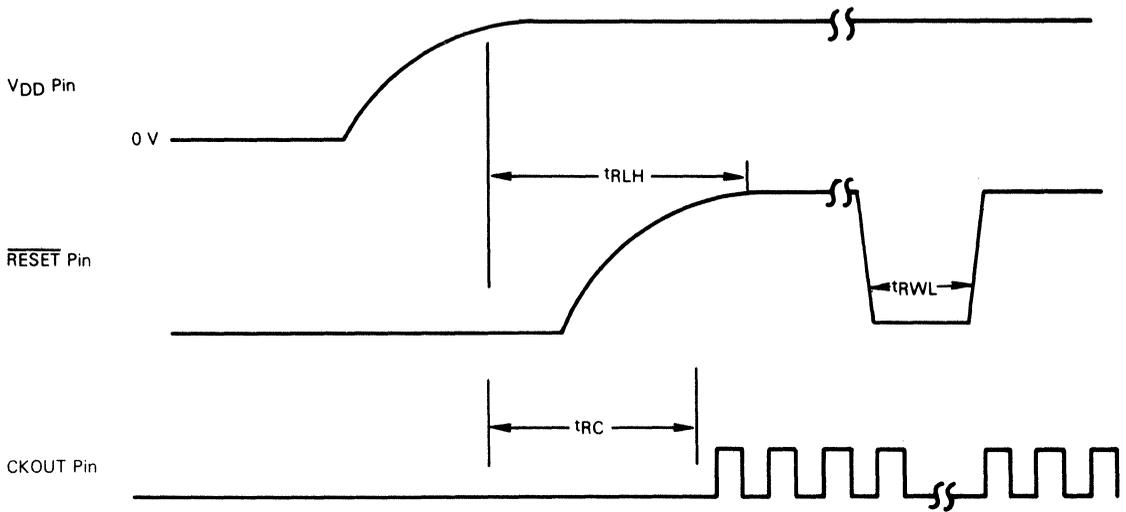
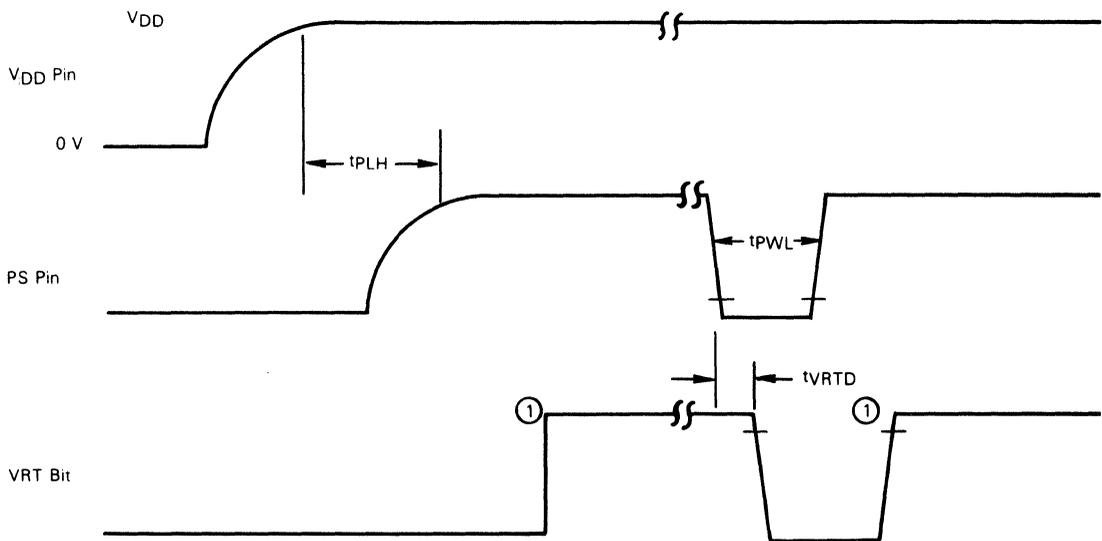


Fig. 7 — Power-up timing waveforms.



① The VRT bit is set to a "1" by reading Control Register #D. There is no additional way to clear the VRT Bit (see section on VRT).

Fig. 8 — Conditions that clear VRT bit timing waveforms.

MOTEL

The MOTEL circuit is a new concept that permits the CDP6818 to be directly interfaced with many types of microprocessors. No external logic is needed to adapt to the differences in bus control signals from common multiplexed bus microprocessors.

Practically all microprocessors interface with one of two synchronous bus structures.

The MOTEL circuit is built into peripheral and memory ICs to permit direct connection to either type of bus. An industry standard bus structure is now available. The MOTEL concept is shown logically in Figure 9.

MOTEL selects one of two interpretations of two pins. In the 6805 case, DS and R/\overline{W} are gated together to produce the internal read enable. The internal write enable is a similar gating of the inverse of R/\overline{W} . With competitor buses, the inversion of \overline{RD} and \overline{WR} create functionally identical internal read and write enable signals.

The CDP6818 automatically selects the processor type by using AS/ALE to latch the state of the DS/ \overline{RD} pin. Since DS is always low and \overline{RD} is always high during AS and ALE, the latch automatically indicates which processor type is connected.

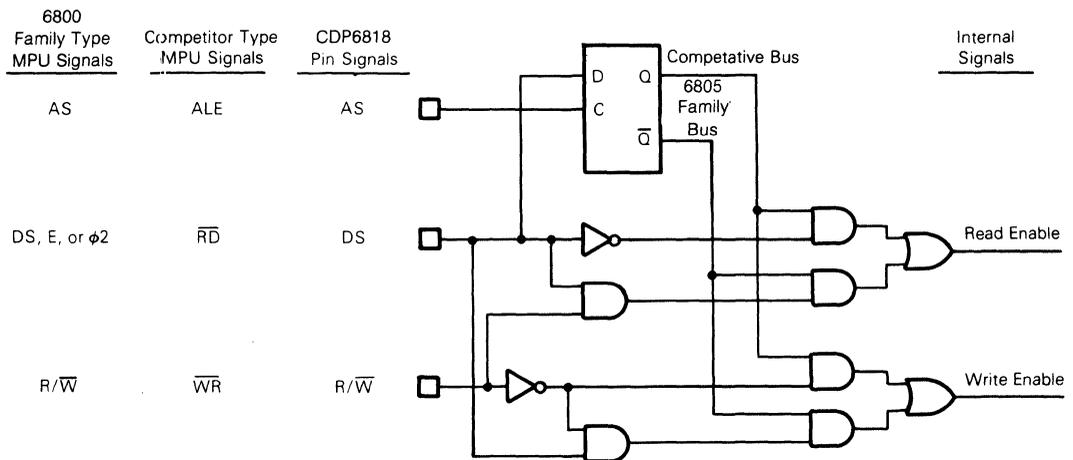


Fig. 9 — Functional diagram of MOTEL circuit.

SIGNAL DESCRIPTIONS

The block diagram in Figure 1, shows the pin connection with the major internal functions of the CDP6818 Real-Time Clock plus RAM. The following paragraphs describe the function of each pin.

VDD, VSS

DC power is provided to the part on these two pins, V_{DD} being the most positive voltage. The minimum and maximum voltages are listed in the Electrical Characteristics tables.

OSC1, OSC2 — TIME BASE, INPUTS

The time base for the time functions may be an external signal or the crystal oscillator. External square waves at 4.194304 MHz, 1.048576 MHz, or 32.768 kHz may be connected to OSC1 as shown in Figure 10. The time-base frequency to be used is chosen in Register A.

The on-chip oscillator is designed for a parallel resonant

AT cut crystal at 4.194304 MHz or 1.048576 MHz frequencies. The crystal connections are shown in Figure 11 and the crystal characteristics in Figure 12.

CKOUT — CLOCK OUT, OUTPUT

The CKOUT pin is an output at the time-base frequency divided by 1 or 4. A major use for CKOUT is as the input clock to the microprocessor; thereby saving the cost of a second crystal. The frequency of CKOUT depends upon the time-base frequency and the state of the CKFS pin as shown in Table 2.

CKFS — CLOCK OUT FREQUENCY SELECT, INPUT

The CKOUT pin is an output at the time-base frequency divided by 1 or 4. CKFS tied to V_{DD} causes CKOUT to be the same frequency as the time base at the OSC1 pin. When CKFS is at V_{SS} , CKOUT is the OSC1 time-base frequency divided by four. Table 2 summarizes the effect of CKFS.

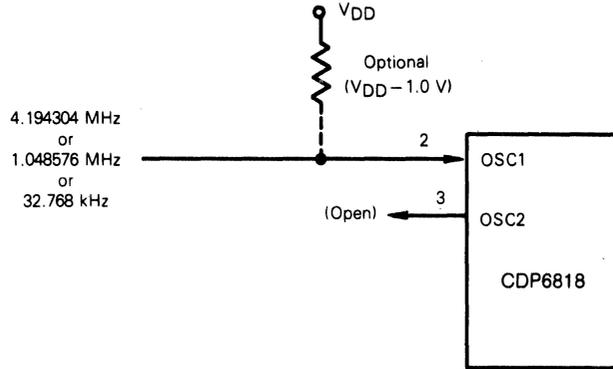


Fig. 10 — External Time-base connection.

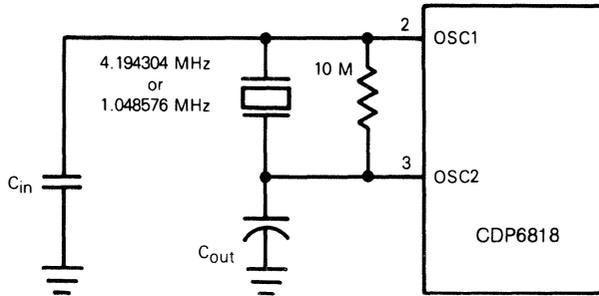
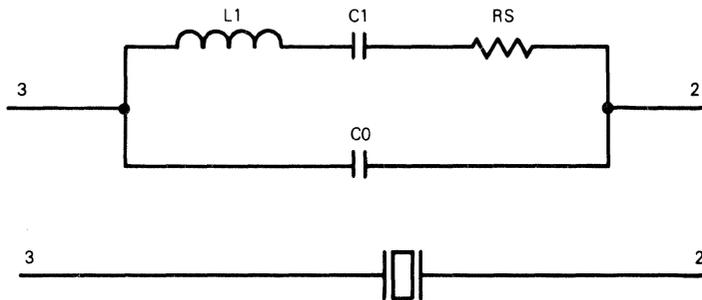


Fig. 11 — Crystal oscillator connection.

Crystal Equivalent Circuit



f_{osc}	4.194304 MHz	1.048576 MHz
R_s max	75 Ω	400 Ω
C_0 max	7 pF	5 pF
C_1	0.012 pF	0.008 pF
C_{in}/C_{out}	15-30 pF	15-40 pF
Q	50 k	35 k

Fig. 12 — Crystal parameters.

TABLE 2 — CLOCK OUTPUT FREQUENCIES

Time Base (OSC1) Frequency	Clock Frequency Select Pin (CKFS)	Clock Frequency Output Pin (CKOUT)
4.194304 MHz	High	4.194304 MHz
4.194304 MHz	Low	1.048576 MHz
1.048576 MHz	High	1.048576 MHz
1.048576 MHz	Low	262.144 kHz
32.768 kHz	High	32.768 kHz
32.768 kHz	Low	8.192 kHz

SQW — SQUARE WAVE, OUTPUT

The SQW pin can output a signal one of 15 of the 22 internal-divider stages. The frequency and output enable of the SQW may be altered by programming Register A, as shown in Table 5. The SQW signal may be turned on and off using a bit in Register B.

AD0-AD7 — MULTIPLEXED BIDIRECTIONAL ADDRESS/DATA BUS

Multiplexed bus processors save pins by presenting the address during the first portion of the bus cycle and using the same pins during the second portion for data. Address-then-data multiplexing does not slow the access time of the CDP6818 since the bus reversal from address to data is occurring during the internal RAM access time.

The address must be valid just prior to the fall of AS/ALE at which time the CDP6818 latches the address from AD0 to AD5. Valid write data must be presented and held stable during the latter portion of the DS or WR pulses. In a read cycle, the CDP6818 outputs 8 bits of data during the latter portion of the DS or RD pulses, then ceases driving the bus (returns the output drivers to three-state) when DS falls in this case of MOTEL or RD rises in the other case.

AS — MULTIPLEXED ADDRESS STROBE, INPUT

A positive going multiplexed address strobe pulse serves to demultiplex the bus. The falling edge of AS or ALE causes the address to be latched within the CDP6818. The automatic MOTEL circuitry in the CDP6818 also latches the state of the DS pin with the falling edge of AS or ALE.

DS — DATA STROBE OR READ, INPUT

The DS pin has two interpretations via the MOTEL circuit. When emanating from a 6800 type processor, DS is a positive pulse during the latter portion of the bus cycle, and is variously called DS (data strobe), E (enable), and $\phi 2$ ($\phi 2$ clock). During read cycles, DS signifies the time that the RTC is to drive the bidirectional bus. In write cycles, the trailing edge of DS causes the Real-Time Clock plus RAM to latch the written data.

The second MOTEL interpretation of DS is that of RD, MEMR, or I/OW emanating from a competitor type processor. In this case, DS identifies the time period when the real-time clock plus RAM drives the bus with read data. This interpretation of DS is also the same as an output-enable signal on a typical memory.

The MOTEL circuit, within the CDP6818, latches the state of the DS pin on the falling edge of AS/ALE. When the 6800 mode of MOTEL is desired DS must be low during AS/ALE, which is

the case with the CDP6805 family of multiplexed bus processors. To insure the competitor mode of MOTEL, the DS pin must remain high during the time AS/ALE is high.

R/W — READ/WRITE, INPUT

The MOTEL circuit treats the R/W pin in one of two ways. When a 6805 type processor is connected, R/W is a level which indicates whether the current cycle is a read or write. A read cycle is indicated with a high level on R/W while DS is high, whereas a write cycle is a low on R/W during DS.

The second interpretation of R/W is as a negative write pulse, WR, MEMW, and I/OW from competitor type processors. The MOTEL circuit in this mode gives R/W pin the same meaning as the write (W) pulse on many generic RAMs.

CE — CHIP ENABLE, INPUT

The chip-enable (CE) signal must be asserted (low) for a bus cycle in which the CDP6818 is to be accessed. CE is not latched and must be stable during DS and AS (in the 6805 mode of MOTEL) and during RD and WR (in the competitor mode). Bus cycles which take place without asserting CE cause no actions to take place within the CDP6818. When CE is high, the multiplexed bus output is in a high-impedance state.

When CE is high, all address, data, DS, and R/W inputs from the processor are disconnected within the CDP6818. This permits the CDP6818 to be isolated from a powered-down processor. When CE is held high, an unpowered device cannot receive power through the input pins from the real-time clock power source. Battery power consumption can thus be reduced by using a pullup resistor or active clamp on CE when the main power is off.

IRQ — INTERRUPT REQUEST, OUTPUT

The IRQ pin is an active low output of the CDP6818 that may be used as an interrupt input to a processor. The IRQ output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt-enable bit is set. To clear the IRQ pin, the processor program normally reads Register C. The RESET pin also clears pending interrupts.

When no interrupt conditions are present, the IRQ level is in the high-impedance state. Multiple interrupting devices may thus be connected to an IRQ bus with one pullup at the processor.

RESET — RESET, INPUT

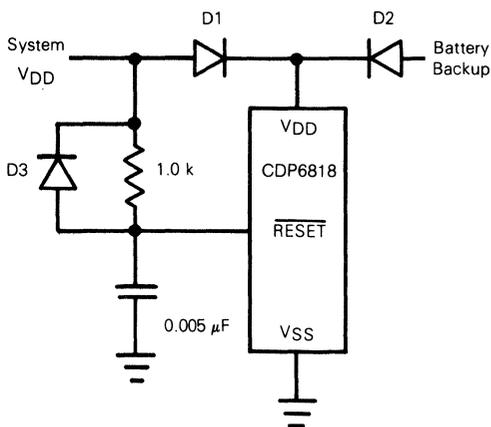
The RESET pin does not affect the clock, calendar, or RAM functions. On the powerup, the RESET pin must be held low for the specified time, t_{RLH} , in order to allow the power supply to stabilize. Figure 13 shows a typical representation of the RESET pin circuit.

When RESET is low the following occurs:

- Periodic Interrupt Enable (PIE) bit is cleared to zero,
- Alarm Interrupt Enable (AIE) bit is cleared to zero,
- Update ended Interrupt Enable (UIE) bit is cleared to zero,
- Update ended Interrupt Flag (UF) bit is cleared to zero,
- Interrupt Request status Flag (IRQF) bit is cleared to zero,
- Periodic Interrupt Flag (PF) bit is cleared to zero,

CDP6818

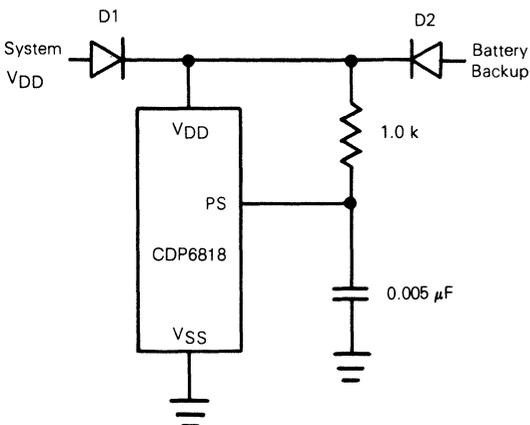
- g) Alarm Interrupt Flag (AF) bit is cleared to zero,
- h) \overline{IRQ} pin is in high-impedance state, and
- i) Square Wave output Enable (SQWE) bit is cleared to zero.



D1 = D2 = D3 = 1N4148 or Equivalent

Note: If the RTC is isolated from the MPU or MCU power by a diode drop, care must be taken to meet V_{IN} requirements.

Fig. 13 — Typical power-up delay circuit for \overline{RESET} .



D1 = D2 = 1N4148 or Equivalent

Fig. 14 — Typical power-up delay circuit for POWER SENSE.

PS — POWER SENSE, INPUT

The power-sense pin is used in the control of the valid RAM and time (VRT) bit in Register C. When the PS pin is low the VRT bit is cleared to zero.

During powerup, the PS pin must be externally held low for the specified time, t_{PL} . As power is applied the VTR bit remains low indicating that the contents of the RAM, time registers, and calendar are not guaranteed. When normal operation commences PS should be permitted to go high. Figure 14 shows a typical circuit connection for the power-sense pin.

POWER-DOWN CONSIDERATIONS

In most systems, the CDP6818 must continue to keep time when system power is removed. In such systems, a conversion from system power to an alternate power supply, usually a battery, must be made. During the transition from system to battery power, the designer of a battery backed-up RTC system must protect data integrity, minimize power consumption, and ensure hardware reliability.

The chip enable (\overline{CE}) pin controls all bus inputs (R/ \overline{W} , DS, AS, AD0-AD7). \overline{CE} , when negated, disallows any unintended modification of the RTC data by the bus. \overline{CE} also reduces power consumption by reducing the number of transitions seen internally.

Power consumption may be further reduced by removing resistive and capacitive loads from the clock out (CKOUT) pin and the squarewave (SQW) pin.

During and after the power source conversion, the V_{IN} maximum specification must never be exceeded. Failure to meet the V_{IN} maximum specification can cause a virtual SCR to appear which may result in excessive current drain and destruction of the part.

ADDRESS MAP

Figure 15 shows the address map of the CDP6818. The memory consists of 50 general purpose RAM bytes, 10 RAM bytes which normally contain the time, calendar, and alarm data, and four control and status bytes. All 64 bytes are directly readable and writable by the processor program except Registers C and D which are read only. Bit 7 of Register A and the seconds byte are also read only. Bit 7, of the second byte, always reads "0". The contents of the four control and status registers are described in the Register section.

TIME, CALENDAR, AND ALARM LOCATIONS

The processor program obtains time and calendar information by reading the appropriate locations. The program may initialize the time, calendar, and alarm by writing to these RAM locations. The contents of the 10 time, calendar, and alarm byte may be either binary or binary-coded decimal (BCD).

Before initializing the internal registers, the SET bit in Register B should be set to a "1" to prevent time/calendar updates from occurring. The program initializes the 10 locations in the selected format (binary or BCD), then indicates the format in the data mode (DM) bit of Register B. All 10 time, calendar, and alarm bytes must use the same data mode, either binary or BCD. The SET bit may now be cleared to allow updates. Once initialized the real-time clock makes all updates in the selected data mode. The data mode cannot be changed without reinitializing the 10 data bytes.

Table 3 shows the binary and BCD formats of the 10 time, calendar, and alarm locations. The 24/12 bit in Register B establishes whether the hour locations represent 1-to-12 or

0-to-23. The 24/12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected the high-order bit of the hours byte represents PM when it is a "1".

The time, calendar, and alarm bytes are not always accessible by the processor program. Once-per-second the 10 bytes are switched to the update logic to be advanced by one second and to check for an alarm condition. If any of the 10 bytes are read at this time, the data outputs are undefined. The update lockout time is 248 μ s at the 4.194304 MHz and 1.048567 MHz time bases and 1948 μ s for the 32.768 kHz time base. The Update Cycle section shows how to accommodate the update cycle in the processor program.

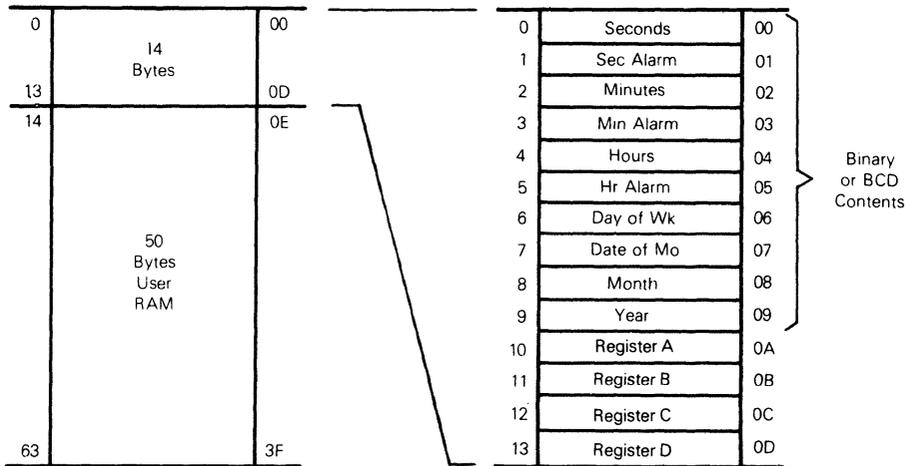


Fig. 15 — Address map.

TABLE 3 — TIME, CALENDAR, AND ALARM DATA MODES

Address Location	Function	Decimal Range	Range		Example*	
			Binary Data Mode	BCD Data Mode	Binary Data Mode	BCD Data Mode
0	Seconds	0-59	\$00-\$3B	\$00-\$59	15	21
1	Seconds Alarm	0-59	\$00-\$3B	\$00-\$59	15	21
2	Minutes	0-59	\$00-\$3B	\$00-\$59	3A	58
3	Minutes Alarm	0-59	\$00-\$3B	\$00-\$59	3A	58
4	Hours (12 Hour Mode)	1-12	\$01-\$0C (AM) and \$81-\$8C (PM)	\$01-\$12 (AM) and \$81-\$92 (PM)	05	05
	Hours (24 Hour Mode)	0-23	\$00-\$17	\$00-\$23	05	05
5	Hours Alarm (12 Hour Mode)	1-12	\$01-\$0C (AM) and \$81-\$8C (PM)	\$01-\$12 (AM) and \$81-\$92 (PM)	05	05
	Hours Alarm (24 Hour Mode)	0-23	\$00-\$17	\$00-\$23	05	05
6	Day of the Week Sunday = 1	1-7	\$01-\$07	\$01-\$07	05	05
7	Day of the Month	1-31	\$01-\$1F	\$01-\$31	0F	15
8	Month	1-12	\$01-\$0C	\$01-\$12	02	02
9	Year	0-99	\$00-\$63	\$00-\$99	4F	79

*Example: 5:58:21 Thursday February 1979

The three alarm bytes may be used in two ways. When the program inserts an alarm time in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high. The alternate usage is to insert a "don't care" state in one or more of three alarm bytes. The "don't care" code is any hexadecimal byte from C0 to FF. That is, the two most-significant bits of each byte, when set to "1", create a "don't care" situation. An alarm interrupt each hour is created with a "don't care" code in the hours alarm location. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minutes alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second.

STATIC CMOS RAM

The 50 general purpose RAM bytes are not dedicated within the CDP6818. They can be used by the processor program, and are fully available during the update cycle.

When time and calendar information must use battery back-up, very frequently there is other non-volatile data that must be retained when main power is removed. The 50 user RAM bytes serve the need for low-power CMOS battery-backed storage, and extend the RAM available to the program.

When further CMOS RAM is needed, additional CDP6818s may be included in the system. The time/calendar functions may be disabled by holding the dividers, in Register A, in the reset state by setting the SET bit in CR2 or by removing the oscillator. Holding the dividers in reset prevents interrupts or SQW output from operating while setting the SET bit allows these functions to occur. With the dividers clear, the available user RAM is extended to 59 bytes. Bit 7 of Register A, Registers C and D, and the high-order Bit of the seconds byte cannot effectively be used as general purpose RAM.

INTERRUPTS

The RTC plus RAM includes three separate fully automatic sources of interrupts to the processor. The alarm interrupt may be programmed to occur at rates from once-per-second to one-a-day. The periodic interrupt may be selected for rates from half-a-second to 30.517 μ s. The update-ended interrupt may be used to indicate to the program that an update cycle is completed. Each of these independent interrupt conditions are described in greater detail in other sections.

The processor program selects which interrupts, if any, it wishes to receive. Three bits in Register B enable the three interrupts. Writing a "1" to an interrupt-enable bit permits that interrupt to be initiated when the event occurs. A "0" in the interrupt-enable bit prohibits the IRQ pin from being asserted due to the interrupt cause.

If an interrupt flag is already set when the interrupt becomes enabled, the $\overline{\text{IRQ}}$ pin is immediately activated, though the interrupt initiating the event may have occurred much earlier. Thus, there are cases where the program should clear such earlier initiated interrupts before first enabling new interrupts.

When an interrupt event occurs a flag bit is set to a "1" in Register C. Each of the three interrupt sources have separate flag bits in Register C, which are set independent of the state of the corresponding enable bits in Register B. The flag bit may be used with or without enabling the corresponding enable bits.

In the software scanned case, the program does not enable the interrupt. The "interrupt" flag bit becomes a status bit, which the software interrogates, when it wishes. When the software detects that the flag is set, it is an indication to software that the "interrupt" event occurred since the bit was last read.

However, there is one precaution. The flag bits in Register C are cleared (record of the interrupt event is erased) when Register C is read. Double latching is included with Register C so the bits which are set are stable throughout the read cycle. All bits which are high when read by the program are cleared, and new interrupts (on any bits) are held until after the read cycle. One, two, or three flag bits may be found to be set when Register C is read. The program should inspect all utilized flag bits every time Register C is read to insure that no interrupts are lost.

The second flag bit usage method is with fully enabled interrupts. When an interrupt-flag bit is set and the corresponding interrupt-enable bit is also set, the $\overline{\text{IRQ}}$ pin is asserted low. $\overline{\text{IRQ}}$ is asserted as long as at least one of the three interrupt sources has its flag and enable bits both set. The IRQF bit in Register C is a "1" whenever the $\overline{\text{IRQ}}$ pin is being driven low.

The processor program can determine that the RTC initiated the interrupt by reading Register C. A "1" in bit 7 (IRQF bit) indicates that one or more interrupts have been initiated by the part. The act of reading Register C clears all the then-active flag bits, plus the IRQF bit. When the program finds IRQF set, it should look at each of the individual flag bits in the same byte which have the corresponding interrupt-mask bits set and service each interrupt which is set. Again, more than one interrupt-flag bit may be set.

DIVIDER STAGES

The CDP6818 has 22 binary-divider stages following the time base as shown in Figure 1. The output of the dividers is a 1 Hz signal to the update-cycle logic. The dividers are controlled by three divider bits (DV2, DV1, and DV0) in Register A.

DIVIDER CONTROL

The divider-control bits have three uses, as shown in Table 4. Three usable operating time bases may be selected (4.194304 MHz, 1.048576 MHz, or 32.768 kHz). The divider chain may be held reset, which allows precision setting of the time. When the divider is changed from reset to an operating time base, the first update cycle is one second later. The divider-control bits are also used to facilitate testing the CDP6818.

TABLE 4 — DIVIDER CONFIGURATIONS

Time-Base Frequency	Divider Bits Register A			Operation Mode	Divider Reset	Bypass First N-Divider Bits
	DV2	DV1	DV0			
4.194304 MHz	0	0	0	Yes	—	N = 0
1.048576 MHz	0	0	1	Yes	—	N = 2
32.768 kHz	0	1	0	Yes	—	N = 7
Any	1	1	0	No	Yes	—
Any	1	1	1	No	Yes	—

Note: Other combinations of divider bits are used for test purposes only.

SQUARE-WAVE OUTPUT SELECTION

Fifteen of the 22 divider taps are made available to a 1-of-15 selector as shown in Figure 1. The first purpose of selecting a divider tap is to generate a square-wave output signal on the SQW pin. Four bits in Register A establish the square-wave frequency as listed in Table 5. The SQW frequency selection shares the 1-of-15 selector with periodic interrupts.

Once the frequency is selected, the output of the SQW pin may be turned on and off under program control with the square-wave enable (SQWE) bit in Register B. Altering the divider, square-wave output selection bits, or the SQW output-enable bit may generate an asymmetrical waveform at the time of execution. The square-wave output pin has a number of potential uses. For example, it can serve as a frequency standard for external use, a frequency synthesizer, or could be used to generate one or more audio tones under program control.

PERIODIC INTERRUPT SELECTION

The periodic interrupt allows the $\overline{\text{IRQ}}$ pin to be triggered from once every 500 ms to once every 30.517 μs . The periodic interrupt is separate from the alarm interrupt which may be output from once-per-second to once-per-day.

Table 5 shows that the periodic interrupt rate is selected with the same Register A bits which select the square-wave frequency. Changing one also changes the other. But each function may be separately enabled so that a program could switch between the two features or use both. The SQW pin is enabled by the SQWE bit. Similarly the periodic interrupt is enabled by the PIE bit in Register B.

Periodic interrupt is usable by practically all real-time systems. It can be used to scan for all forms of inputs from contact closures to serial receive bits on bytes. It can be used in multiplexing displays or with software counters to measure inputs, create output intervals, or await the next needed software function.

TABLE 5 — PERIODIC INTERRUPT RATE AND SQUARE WAVE OUTPUT FREQUENCY

Rate Select Control Register 1				4.194304 or 1.048576 MHz Time Base		32.768 kHz Time Base	
				Periodic Interrupt Rate tPI	SQW Output Frequency	Periodic Interrupt Rate tPI	SQW Output Frequency
RS3	RS2	RS1	RS0				
0	0	0	0	None	None	None	None
0	0	0	1	30.517 μs	32.768 kHz	3.90625 ms	256 Hz
0	0	1	0	61.035 μs	16.384 kHz	7.8125 ms	128 Hz
0	0	1	1	122.070 μs	8.192 kHz	122.070 μs	8.192 kHz
0	1	0	0	244.141 μs	4.096 kHz	244.141 μs	4.096 kHz
0	1	0	1	488.281 μs	2.048 kHz	488.281 μs	2.048 kHz
0	1	1	0	976.562 μs	1.024 kHz	976.562 μs	1.024 kHz
0	1	1	1	1.953125 ms	512 Hz	1.953125 ms	512 Hz
1	0	0	0	3.90625 ms	256 Hz	3.90625 ms	256 Hz
1	0	0	1	7.8125 ms	128 Hz	7.8125 ms	128 Hz
1	0	1	0	15.625 ms	64 Hz	15.625 ms	64 Hz
1	0	1	1	31.25 ms	32 Hz	31.25 ms	32 Hz
1	1	0	0	62.5 ms	16 Hz	62.5 ms	16 Hz
1	1	0	1	125 ms	8 Hz	125 ms	8 Hz
1	1	1	0	250 ms	4 Hz	250 ms	4 Hz
1	1	1	1	500 ms	2 Hz	500 ms	2 Hz

UPDATE CYCLE

The CDP6818 executes an update cycle once-per-second, assuming one of the proper time bases is in place, the divider is not clear, and the SET bit in Register B is clear. The SET bit in the "1" state permits the program to initialize the time and calendar bytes by stopping an existing update and preventing a new one from occurring.

The primary function of the update cycle is to increment the seconds byte, check for overflow, increment the minutes byte when appropriate and so forth through to the year of the century byte. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a "don't care" code (11XXXXXX) is present in all three positions.

With a 4.194304 MHz or 1.048576 MHz time base the update cycle takes 248 μ s while a 32.768 kHz time base update cycle takes 1984 μ s. During the update cycle, the time, calendar, and alarm bytes are not accessible by the processor program. The CDP6818 protects the program from reading transitional data. This protection is provided by switching the time, calendar, and alarm portion of the RAM off the microprocessor bus during the entire update cycle. If the processor reads these RAM locations before the update is complete the output will be undefined. The update in progress (UIP) status bit is set during the interval.

A program which randomly accesses the time and date information finds data unavailable statistically once every 4032 attempts. Three methods of accommodating nonavailability during update are usable by the program. In discussing the three methods it is assumed that at random points user programs are able to call a subroutine to obtain the time of day.

The first method of avoiding the update cycle uses the update-ended interrupt. If enabled, an interrupt occurs after every update cycle which indicates that over 999 ms are available to read valid time and date information. During this time a display could be updated or the information could be transferred to continuously available RAM. Before leaving the interrupt service routine, the IRQF bit in Register C should be cleared.

The second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress or not. The UIP bit will pulse once-per-second. Statistically, the UIP bit will indicate that time and date information is unavailable once every 2032 attempts. After the UIP bit goes high, the update cycle begins 244 μ s later. Therefore, if a low is read on the UIP bit, the user has at least 244 μ s before the time/calendar data will be changed. If a "1" is read in the

UIP bit, the time/calendar data may not be valid. The user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 μ s.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit on Register C (see Figure 16). Periodic interrupts that occur at intervals greater than $t_{BUC} + t_{UC}$ allow valid time and date information to be read at each occurrence of the periodic interrupt. The reads should be completed within $(T_{PI} + 2) + t_{BUC}$ to insure that data is not read during the update cycle.

REGISTERS

The CDP6818 has four registers which are accessible to the processor program. The four registers are also fully accessible during the update cycle.

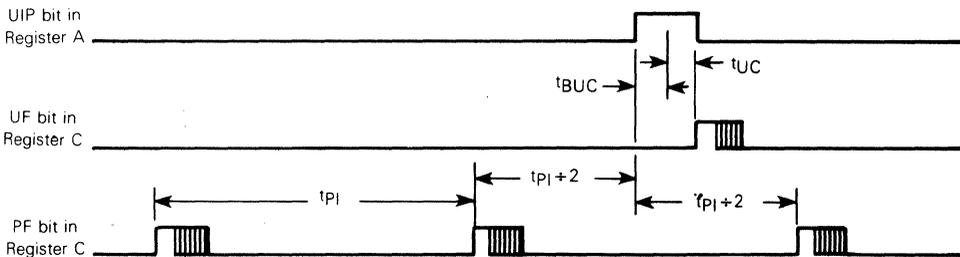
REGISTER A (\$0A)

MSB							LSB		Read/Write Register except UIP
b7	b6	b5	b4	b3	b2	b1	b0		
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0		

UIP — The update in progress (UIP) bit is a status flag that may be monitored by the program. When UIP is a "1" the update cycle is in progress or will soon begin. When UIP is a "0" the update cycle is not in progress and will not be for at least 244 μ s (for all time bases). This is detailed in Table 6. The time, calendar, and alarm information in RAM is fully available to the program when the UIP bit is zero — it is not in transition. The UIP bit is a read-only bit, and is not affected by Reset. Writing the SET bit in Register B to a "1" inhibit any update cycle and then clear the UIP status bit.

TABLE 6 — UPDATE CYCLE TIMES

UIP Bit	Time Base (OSC1)	Update Cycle Time (t_{UC})	Minimum Time Before Update Cycle (t_{BUC})
1	4.194304 MHz	248 μ s	—
1	1.048576 MHz	248 μ s	—
1	32.768 kHz	1984 μ s	—
0	4.194304 MHz	—	244 μ s
0	1.048576 MHz	—	244 μ s
0	32.768 kHz	—	244 μ s



t_{PI} = Periodic Interrupt Time Interval (500 ms, 250 ms, 125 ms, 62.5 ms, etc.)
 t_{UC} = Update Cycle Time (248 μ s or 1984 μ s)
 t_{BUC} = Delay Time Before Update Cycle (244 μ s)

Fig. 16 — Update-ended and periodic interrupt relationships.

DV2, DV1, DV0 — Three bits are used to permit the program to select various conditions of the 22-stage divider chain. The divider selection bits identify which of the three time-base frequencies is in use. Table 4 shows that time bases of 4.194304 MHz, 1.048576 MHz, and 32.768 kHz may be used. The divider selection bits are also used to reset the divider chain. When the time/calendar is first initialized, the program may start the divider at the precise time stored in the RAM. When the divider reset is removed the first update cycle begins one second later. These three read/write bits are never modified by the RTC and are not affected by RESET.

RS3, RS2, RS1, RS0 — The four rate selection bits select one of 15 taps on the 22-stage divider, or disable the divider output. The tape selected may be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The program may do one of the following: 1) enable the interrupt with the PIE bit, 2) enable the SQW output pin with the SQWE bit, 3) enable both at the same time at the same rate, or 4) enable neither. Table 5 lists the periodic interrupt rates and the square-wave frequencies that may be chosen with the RS bits. These four bits are read/write bits which are not affected by RESET and are never changed by the RTC.

REGISTER B (\$0B)

MSB							LSB		Read/Write Register
b7	b6	b5	b4	b3	b2	b1	b0		
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE		

SET — When the SET bit is a "0", the update cycle functions normally by advancing the counts once-per-second. When the SET bit is written to a "1", any update cycle in progress is aborted and the program may initialize the time and calendar bytes without an update occurring in the midst of initializing. SET is read/write bit which is not modified but RESET or internal functions of the CDP6818.

PIE — The periodic interrupt enable (PIE) bit is a read/write bit which allows the periodic-interrupt flag (PF) bit to cause the $\overline{\text{IRQ}}$ pin to be driven low. A program writes a "1" to the PIE bit in order to receive periodic interrupts at the rate specified by the RS3, RS2, RS1, and RS0 bits in Control Register A. A zero in PIE blocks $\overline{\text{IRQ}}$ from being initiated by a periodic interrupt, but the periodic flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal CDP6818 functions, but is cleared to "0" by a RESET.

AIE — The alarm interrupt enable (AIE) bit is a read/write bit which when set to a "1" permits the alarm flag (AF) to assert $\overline{\text{IRQ}}$. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes (including a "don't care" alarm code of binary 11XXXXXX). When the AIE bit is a "0", the AF bit does not initiate an $\overline{\text{IRQ}}$ signal. The RESET pin clears AIE to "0". The internal functions do not affect the AIE bit.

UIE — The UIE (update-ended interrupt enable) bit is a read/write bit which enables the update-end flage (UF) bit to assert $\overline{\text{IRQ}}$. The RESET pin going low or the SET bit going high clears the UIE bit.

SQWE — When the square-wave enable (SQWE) bit is set to a "1" by the program, a square-wave signal at the fre-

quency specified in the rate selection bits (RS3 to RS0) appears on the SQW pin. When the SQWE bit is set to a zero the SQW pin is held low. The state of SQWE is cleared by the RESET pin. SQWE is a read/write bit.

DM — The data mode (DM) bit indicates whether time and calendar updates are to use binary or BCD formats. The DM bit is written by the processor program and may be read by the program, but is not modified by any internal functions or RESET. A "1" in DM signifies binary data, while a "0" in DM specifies binary-coded-decimal (BCD) data.

24/12 — The 24/12 control bit establishes the format of the hours bytes as either the 24-hour mode (a "1") or the 12-hour mode (a "0"). This is a read/write bit, which is affected only by the software.

DSE — The daylight savings enable (DSE) bit is a read/write bit which allows the program to enable two special updates (when DSE is a "1"). On the last Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a "0". DSE is not changed by any internal operations or RESET.

REGISTER C (\$0C)

MSB							LSB		Read-Only Register
b7	b6	b5	b4	b3	b2	b1	b0		
IRQF	PF	AF	UF	0	0	0	0		

IRQF — The interrupt request flag (IRQF) is set to a "1" when one or more of the following are true:

PF = PIE = "1"

AF = AIE = "1"

UF = UIE = "1"

i.e., $\text{IRQF} = \text{PF} \cdot \text{PIE} + \text{AF} \cdot \text{AIE} + \text{UF} \cdot \text{UIE}$

Any time the IRQF bit is a "1", the $\overline{\text{IRQ}}$ pin is driven low. All flag bits are cleared after Register C is read by the program or when the RESET pin is low. A program write to Status Register 2 does not modify any of the flag bits.

PF — The periodic interrupt flag (PF) is a read-only bit which is set to a "1" when a particular edge is detected on the selected tap of the divider chain. The RS3 to RS0 bits establish the periodic rate. PF is set to a "1" independent of the state of the PIE bit. PF being a "1" initiates an $\overline{\text{IRQ}}$ signal and the IRQF bit when PIE is also a "1". The PF bit is cleared by a RESET or a software read of Register C.

AF — A "1" in the AF (alarm interrupt flag) bit indicates that the current time has matched the alarm time. A "1" in the AF causes the $\overline{\text{IRQ}}$ pin to go low, and a "1" to appear in the IRQF bit, when the AIE bit also is a "1". A RESET or a read of Register C clears AF.

UF — The update-ended interrupt flag (UF) bit is set after each update cycle. When the UIE bit is a "1", the "1" in UF causes the IRQF bit to be a "1", asserting $\overline{\text{IRQ}}$. UF is cleared by a Register C read or a RESET.

b3 TO b0 — The unused bits of Status Register 1 are read as "0's". They can not be written.

RCA CMOS LSI Products

CDP6818

REGISTER D (\$0D)

MSB							LSB	
b7	b6	b5	b4	b3	b2	b1	b0	
VRT	0	0	0	0	0	0	0	Read Only Register

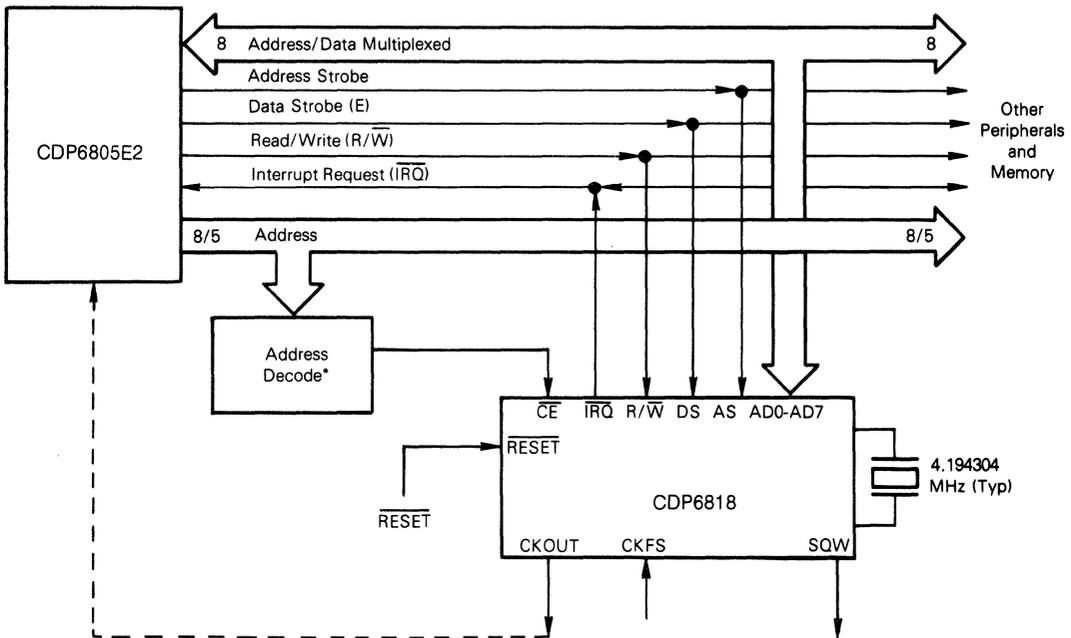
VRT — The valid RAM and time (VRT) bit indicates the condition of the contents of the RAM, provided the power sense (PS) pin is satisfactorily connected. A "0" appears in the VRT bit when the power-sense pin is low. The processor program can set the VRT bit when the time and calendar are initialized to indicate that the RAM and time are valid. The VRT is a read-only bit which is not modified by the **RESET** pin. The VRT bit can only be set by reading the Register D.

b6 TO b0 — The remaining bits of Register D are unused. They cannot be written, but are always read as "0's."

TYPICAL INTERFACING

The CDP6818 is best suited for use with microprocessors which generate an address-then-data multiplexed bus. Figures 17 and 18 show typical interfaces to bus-compatible processors. These interfaces assume that the address decoding can be done quickly. However, if standard metal-gate CMOS gates are used the **CE** setup time may be violated. Figure 19 illustrates an alternative method of chip selection which will accommodate such slower decoding.

The CDP6818 can be interfaced to single-chip microcomputers (MCU) by using eleven port lines as shown in Figure 20. Non-multiplexed bus microprocessors can be interfaced with additional support.



*High-Speed Silicon-Gate CMOS or TTL Address Decoding

Fig. 17 — CDP6818 interfaced to CDP6805E2 compatible multiplexed bus microprocessors.

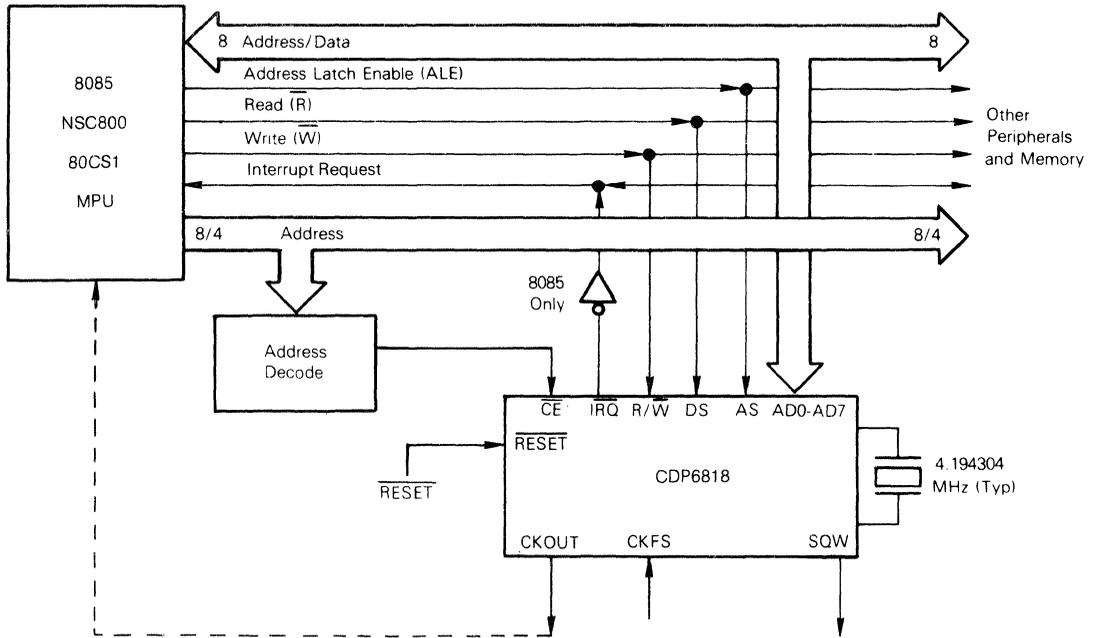
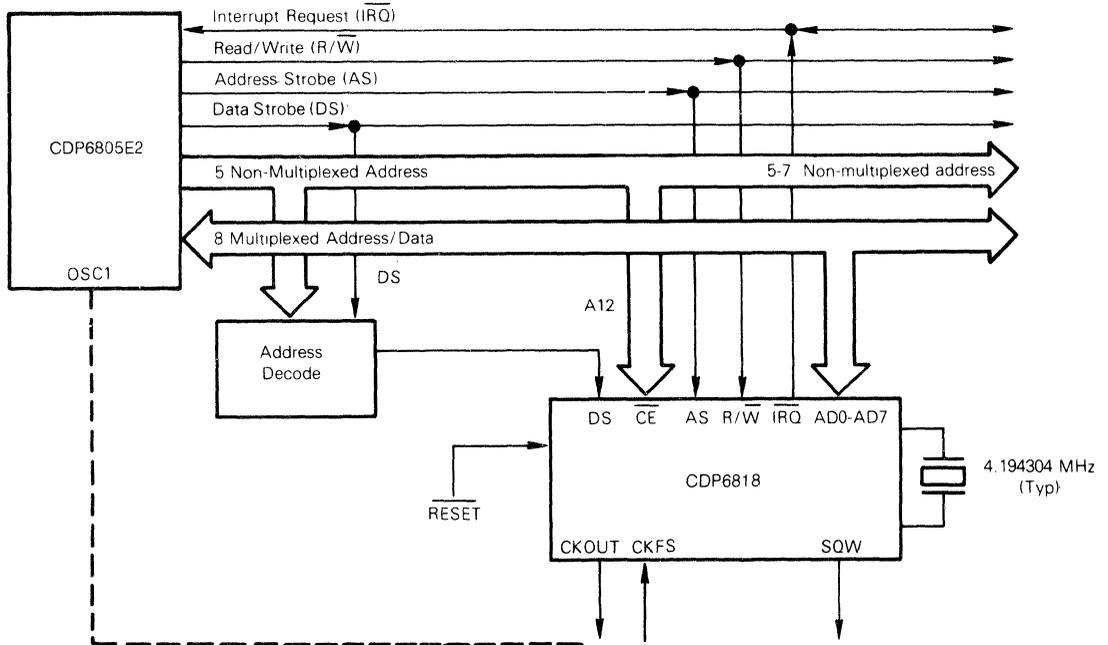


Fig. 18 — CDP6818 interfaced to competitor compatible multiplexed bus microprocessors.



This illustrates the use of CMOS gating for address decoding.

Fig. 19 — CDP6818 interface to CDP6805E2 CMOS multiplexed microprocessor with slow address decoding.

CDP6818

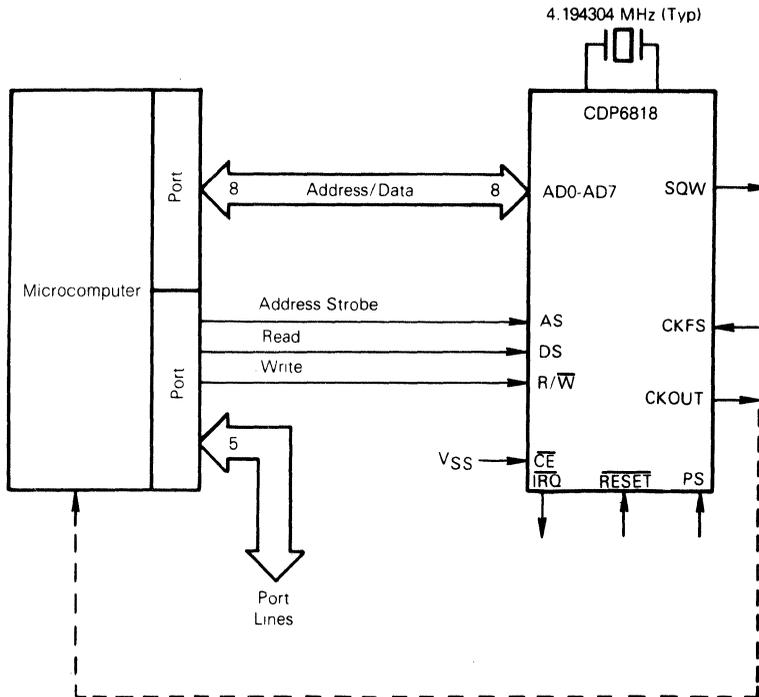


Fig. 20 — CDP6818 interfaced with the ports of a typical single-chip microcomputer.

ORDERING INFORMATION

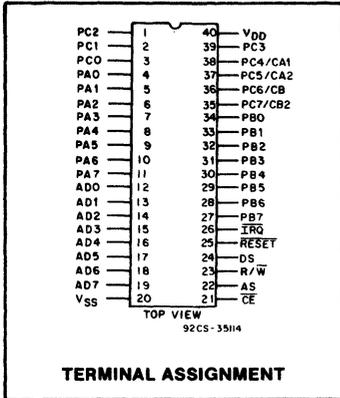
RCA Microprocessor device packages are identified by letters indicated in the following chart. When ordering a Microprocessor device, it is important that the appropriate suffix letter be affixed to the type number of the device.

Package	Suffix Letter
Dual-In-Line Side-Brazed Ceramic	D
Dual-In-Line Plastic	E

For example, a CDP6818 in a dual-in-line plastic package will be identified as the CDP6818E.

Objective Data

CMOS Parallel Interface



Features:

- 24 Individual Programmed I/O Pins
- MOTEL Circuit for Bus Compatibility with Many Microprocessors
- Multiplexed Bus Compatible with: CDP6805E2 and Competitive Microprocessors
- Data Direction Registers for Ports A, B, and C
- Port C may also be Control Lines for:
 - Four Interrupt Inputs
 - Input Byte Latch
 - Output Pulse
- 16 Registers Addressed as Memory Locations
- Handshake Control Logic for Input and Output Peripheral Operation
- Interrupt Output Pin
- Reset Input to Clear Interrupts and Initialize Internal Registers
- 40-Pin Package

The CMOS CDP6823 Parallel Interface (PI) provides a universal means of interfacing external signals with the CDP6805E2 CMOS microprocessor, and other multiplexed bus microprocessors. The unique MOTEL circuit on-chip allows direct interfacing to most industry CMOS microprocessors, as well as many NMOS MPUs.

The CDP6823 PI includes three bidirectional 8-bit ports, or 24

I/O pins. Each I/O line may be separately established as an input or an output under program control via data direction registers associated with each port. Using the bit change and test instructions of the CDP6805E2, each individual I/O pin can be separately accessed. All port registers are read/write bytes to accommodate read/modify/write instructions.

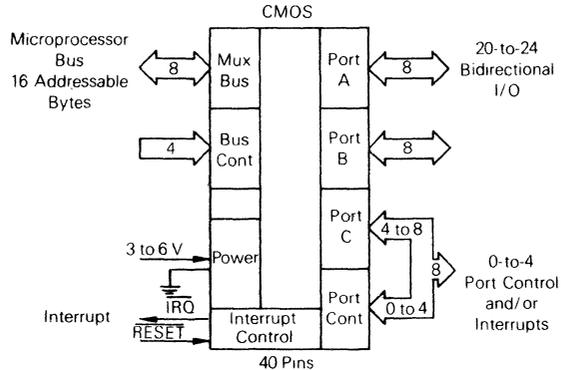
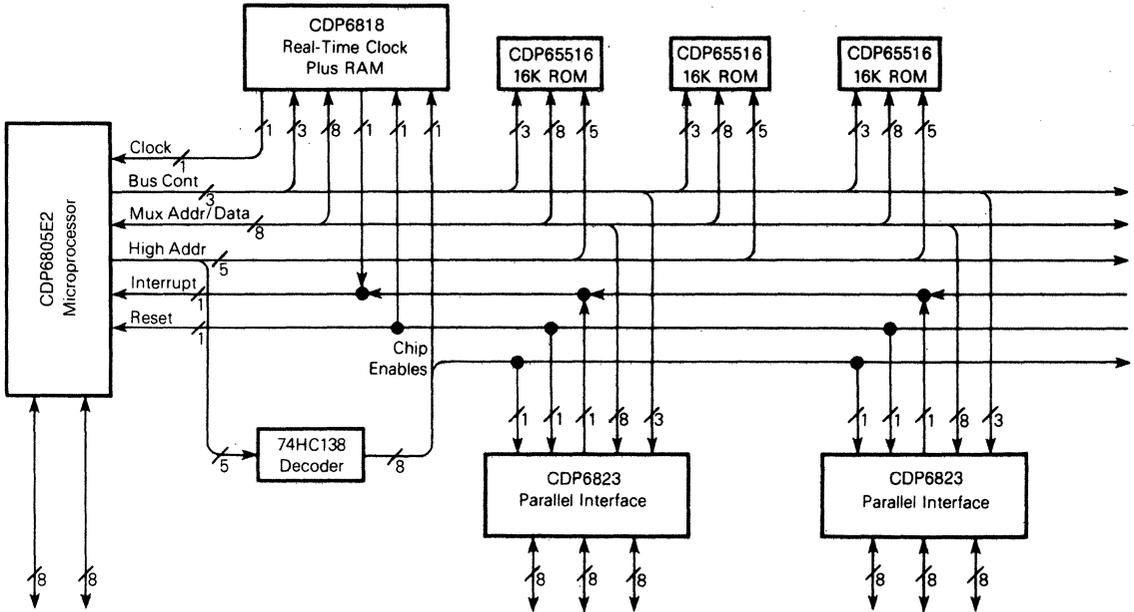


Fig. 1 — Functional diagram.

CDP6823



An 8-Chip CMOS Microprocessor System Includes:
 Powerful 8-Bit Processor
 6K Bytes of ROM
 162 Bytes of RAM
 64 Parallel I/O Pins

Up to 12 System Interrupts:
 Timer Interrupt
 Periodic Interrupt
 Alarm Time Interrupt
 Update Cycle (1 Second) Interrupt
 Up to 8 External Event Interrupts
 Time-Of-Day and Calendar
 8-Bit Programmable Counter with 7-Bit Prescaler

Fig. 2 — A typical CMOS microprocessor system.

Four of the 24 I/O pins have multiple functions. The mode of these four lines is selected by programming the Port C Pin Function Select Register. Any of the four control pins may be configured to initiate interrupts to the microprocessor via the \overline{IRQ} pin. All four interrupts have separate programmable enables, status bits, methods of clearing the interrupt, and over-run detection.

The interrupts are enabled and the port handshaking controls are established via the content of Control Registers associated with Ports A and B. The interrupt conditions are indicated in a Status Register and the \overline{IRQ} pin is asserted. The interrupts are normally cleared by reading or writing the associated port data. Ports A and B each have three addresses for reading/writing data. Two addresses access the data and clear an interrupt while the third accesses the data without modifying the interrupt status.

CDP6823 Registers

0	Port A Data, Clear CA1 Interrupt
1	Port A Data, Clear CA2 Interrupt
2	Port A Data
3	Port B Data
4	Port C Data
5	Not Used
6	Data Direction Register for Port A
7	Data Direction Register for Port B
8	Data Direction Register for Port C
9	Control Register for Port A
A	Control Register for Port B
B	Pin Function Select Register for Port C
C	Port B Data, Clear CB1 Interrupt
D	Port B Data, Clear CB2 Interrupt
E	Interrupt Status Register
F	Interrupt Over-Run Warning Register

Supplementary Information

RCA High-Reliability IC Capability

RCA Solid State is a leading supplier of high-reliability integrated circuits to the military and aerospace community. Years of commitment, dedication, experience, and know-how make possible shipment of hundreds of thousands of quality high-reliability microcircuits annually.

RCA specialists fully understand the needs of component and systems engineers in the design of high-reliability equipment, are thoroughly familiar with the objective and requirements of MIL-STD-883 and MIL-M-38510, and work closely with governmental agencies in the establishment of detailed specifications for high-reliability microcircuits. Moreover, RCA provides complete facilities for processing and testing integrated circuits to these specifications. RCA is justly proud of its many significant accomplishments with respect to the development, production and shipment of high-reliability integrated circuits, including:

- First supplier of MIL-M-38510 to attain QPL Class S Part One Radiation-Hardness Listing
- First supplier of MIL-M-38510 CMOS integrated circuits
- Leader in the production of radiation-resistant CMOS microcircuits [to 1×10^6 rad (Si)]
- Initiator of scanning-electron-microscope (SEM) inspections in the production of high-reliability microcircuits — in use at RCA since 1972
- Initiator of MIL-STD-883, Condition A inspections — in use at RCA since 1972
- A leading supplier of dielectrically isolated circuits

Standard-Product High-Reliability IC's

RCA offers high-reliability versions of virtually its entire line of standard-product integrated circuits from the CD4000 series of CMOS digital logic types, the CDP1800 series of microprocessor and associated memory and input/output (I/O) types, and the CA3000 series of bipolar linear types. These integrated circuits are processed and screened to MIL-STD-883 Class B requirements. Extensive inventories are maintained for rapid, off-the-shelf delivery.

RCA also offers high-reliability versions of standard-product types that are processed and screened to special customized specifications, especially for the aerospace user and others who procure types to Class S specifications.

RCA maintains an extensive computer file of customer specifications and has the methodology required to translate these customized specifications into internal RCA standards and factory operating procedures. In addition to the detailed device specifications, the computer file lists the customer specification number, any revision number, and the RCA custom number assigned to a specific device type.

Radiation-Hardened High-Reliability IC's

RCA also offers radiation-hardened versions of high-reliability (Class S and Class S format) CD4000-series CMOS integrated circuits. Radiation-hardened types, which are identified by addition of a "Z" or "J" suffix to the device type number, are electrically and mechanically identical to their prototype with the exception that they are processed and screened to withstand a total gamma-

radiation dosage of 10^5 rads(Si) for Z-suffix types or 10^6 rads(Si) for J-suffix types. Selected CDP1800-series CMOS integrated circuits are available to various levels of radiation hardness. In addition, RCA offers a spectrum of radiation-hardened bipolar integrated circuits that employ dielectric isolation and diode-photocurrent compensation.

High-Reliability Custom IC's

RCA has complete custom-circuit capabilities for various CMOS and bipolar integrated-circuit technologies. Custom circuits are offered whenever this approach to integrated-circuit design is determined to be economically feasible. RCA high-reliability custom integrated circuits can be processed and screened to MIL-STD-883 Class S and Class B specifications. These custom circuits, which are described in detail in later sections of this DATABOOK, include:

- Gate universal arrays
- EPIC 8-bit slice microcomputer family and associated memory (RAM) complement
- Radiation-hardened linear IC's
- Radiation-hardened high-speed bipolar IC's.

The image shows three overlapping pages of a computer file. The top page is titled 'CUSTOM NUMBER, NORTH-DATASITE DATE ACTIVITY AS OF 11.27.69 ON 12/29/69'. It lists columns for CUSTOM-NUM, CUSTOMER, SPEC-NUM, REV, TYPE, LEVEL, MISC, and COMPLY. The middle page is titled 'SPECIFICATION, NORTH-DATASITE DATE ACTIVITY AS OF 11.27.69 ON 12/29/69' and lists columns for SPEC-NUM, REV, CUSTOMER, COMPLY, TYPE, LEVEL, MISC, and RECD. The bottom page is titled 'CUSTOMER, NORTH-DATASITE DATE ACTIVITY AS OF 11.27.69 ON 12/29/69' and lists columns for CUSTOMER, SPEC-NUM, REV, TYPE, LEVEL, MISC, CUSTOM-NUM, COMPLY, and ENDORSE.

Sample pages of RCA's computer file on standard-product high-reliability IC's processed to special custom specifications. The file can be accessed by device specification number, by customer or by the RCA custom number assigned to the device.

RCA also provides a broad line of high-reliability discrete solid-state power devices (power transistors, triacs, and silicon controlled rectifiers). These devices include types qualified as JAN or JANTX devices in accordance with MIL-STD-19500 General Specifications and MIL-STD-750 Test Methods, types that are not yet covered by military specifications but that are processed and screened to specifications patterned after the military standards, and types that are specially designed and processed to withstand high radiation environments.

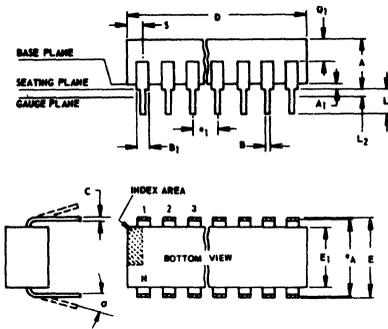
Dimensional Outlines

Dual-In-Line Plastic Packages

E SUFFIX

16-Lead (E & F) (JEDEC MO-001-AC)

18-Lead

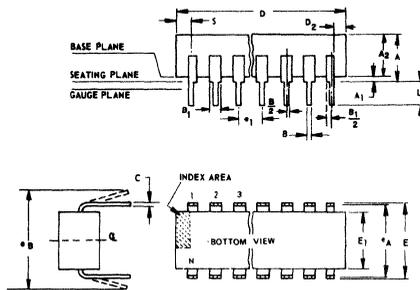


SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A ₁	0.020	0.050		0.51	1.27
B	0.014	0.020		0.356	0.508
B ₁	0.035	0.065		0.89	1.65
C	0.008	0.012	1	0.204	0.304
D	0.745	0.785		18.93	19.93
E	0.300	0.325		7.62	8.25
E ₁	0.240	0.260		6.10	6.60
e ₁	0.100 TP		2	2.54 TP	
e _A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L ₂	0.000	0.030		0.000	0.76
a	0°	15°	4	0°	15°
N	16		5	16	
N ₁	0		6	0	
Q ₁	0.040	0.075		1.02	1.90
S	0.015	0.060		0.39	1.52

92CM-15967R4

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A ₁	0.020	0.050		0.508	1.27
B	0.014	0.020		0.356	0.508
B ₁	0.035	0.065		0.89	1.65
C	0.008	0.012	1	0.204	0.304
D	0.845	0.885		21.47	22.47
E ₁	0.240	0.260		6.10	6.60
e ₁	0.100 TP		2	2.54 TP	
e _A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
a	0°	15°	4	0°	15°
N	18		5	18	
N ₁	0		6	0	
S	0.015	0.060		0.39	1.52

92CS-30630



20-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	—	0.210	10	—	5.33
A ₁	0.010	—	10	0.254	—
A ₂	0.115	0.195		2.93	4.95
B	0.014	0.022		0.356	0.558
B ₁	0.045	0.070	3	1.15	1.77
C	0.008	0.015		0.204	0.381
D	0.925	1.040	4	23.49	26.42
D ₂	0.005	—	5	0.13	—
E	0.300	0.325	6	7.62	8.25
E ₁	0.240	0.280	7, 8	6.10	7.11
e ₁	0.090	0.110	9	2.29	2.79
e _A	0.300 TP		10	7.62 TP	
e _B	—	0.410	11	—	10.41
L	0.115	0.150	10	2.93	3.81
N	20		12	20	
S	—	—	13	—	—

92CM-35136

NOTES:

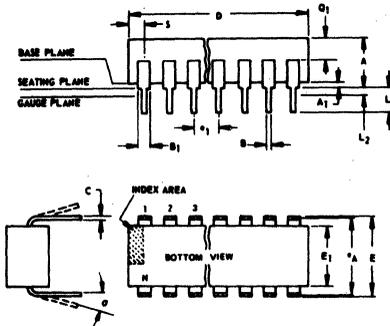
1. Refer to JEDEC Publication No. 95 JEDEC Registered and Standard Outlines for Solid State Products, for rules and general information concerning registered and standard outlines.
2. Protrusions (flash) on the base plane surface shall not exceed .25 mm (.010 in.).
3. The dimension shown is for full leads. "Half" leads are optional at lead positions 1, N, $\frac{N}{2}$, $\frac{N}{2} + 1$.
4. Dimension D does not include mold flash or protrusions. Mold flash or protrusions shall not exceed .25 mm (.010 in.).
5. This dimension is controlling when a particular combination of body length, lead width and lead spacing dimensions would allow lead material to overhang the ends of the package.
6. E is the dimension to the outside of the leads and is measured with the leads perpendicular to the base plane (zero lead spread).
7. Dimension E₁ does not include mold flash or protrusions.

8. Package body and leads shall be symmetrical around center line shown in end view within .25 mm (.010 in.).
9. Lead spacing e₁ shall be non-cumulative and shall be measured at the lead tip. This measurement shall be made before insertion into gauges, boards or sockets.
10. This is a basic installed dimension. Measurement shall be made with the device installed in the seating plane gauge (JEDEC Outline No. GS-3, seating plane gauge). Leads shall be in true position within .25 mm (.010 in.) diameter for dimension e_A.
11. e_B is the dimension to the outside of the leads and is measured at the lead tips before the device is installed. Negative lead spread is not permitted.
12. N is the maximum number of lead positions.
13. Dimension S at the left end of the package must equal dimension S at the right end of the package within .76 mm (.030 in.).

Dimensional Outlines (Cont'd)

Dual-In-Line Plastic Packages

E SUFFIX



22-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A ₁	0.020	0.050		0.508	1.27
B	0.015	0.020		0.381	0.508
B ₁	0.035	0.065		0.89	1.65
C	0.008	0.012	1	0.204	0.304
D		1.120			28.44
E	0.390	0.420		9.91	10.66
E ₁	0.345	0.355		8.77	9.01
e ₁	0.100 TP		2	2.54 TP	
e _A	0.400 TP		2, 3	10.16 TP	
L	0.125	0.150		3.18	3.81
L ₂	0	0.030		0	0.762
α	2°	15°	4	2°	15°
N	22		5	22	
N ₁	0		6	0	
Q ₁	0.055	0.085		1.40	2.15
S	0.015	0.060		0.381	1.27

92CS-30830

24-Lead (JEDEC MO-015-AA)

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.120	0.250		3.10	6.30
A ₁	0.020	0.070		0.51	1.77
B	0.016	0.020		0.407	0.508
B ₁	0.028	0.070		0.72	1.77
C	0.008	0.012	1	0.204	0.304
D	1.20	1.29		30.48	32.76
E	0.600	0.625		15.24	15.87
E ₁	0.515	0.580		13.09	14.73
e ₁	0.100 TP		2	2.54 TP	
e _A	0.600 TP		2, 3	15.24 TP	
L	0.100	0.200		2.54	5.00
L ₂	0.000	0.030		0.00	0.76
α	0°	15°	4	0°	15°
N	24		5	24	
N ₁	0		6	0	
Q ₁	0.040	0.075		1.02	1.90
S	0.040	0.100		1.02	2.54

92CS26938R3

28-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.120	0.250		3.10	6.30
A ₁	0.020	0.070		0.51	1.77
B	0.016	0.020		0.407	0.508
B ₁	0.028	0.070		0.72	1.77
C	0.008	0.012	1	0.204	0.304
D	1.400	1.490		35.56	37.85
E ₁	0.515	0.580		13.09	14.73
e ₁	0.100 TP		2	2.54 TP	
e _A	0.600 TP		2, 3	15.24 TP	
L	0.100	0.200		2.54	5.00
L ₂	0.000	0.030		0.00	0.76
α	0°	15°	4	0°	15°
N	28		5	28	
N ₁	0		6	0	
Q ₁	0.045	0.080		1.14	2.03
S	0.040	0.100		1.02	2.54

92CS-31862

NOTES:

Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.

1. When this device is supplied solder dipped, the maximum lead thickness (narrow portion) will not exceed 0.013" (0.33 mm).

40-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.120	0.250		3.10	6.30
A ₁	0.020	0.070		0.51	1.77
B	0.016	0.020		0.407	0.508
B ₁	0.028	0.070		0.72	1.77
C	0.008	0.012	1	0.204	0.304
D	2.000	2.090		50.80	53.09
E ₁	0.515	0.580		13.09	14.73
e ₁	0.100 TP		2	2.54 TP	
e _A	0.600 TP		2, 3	15.24 TP	
L	0.100	0.200		2.54	5.00
L ₂	0.000	0.030		0.00	0.76
α	0°	15°	4	0°	15°
N	40		5	40	
N ₁	0		6	0	
Q ₁	0.065	0.095		1.66	2.41
S	0.040	0.100		1.02	2.54

92CS-30959

2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at gauge plane with maximum material condition and unit installed.

3. e_A applies in zone L₂ when unit installed.

4. α applies to spread leads prior to installation.

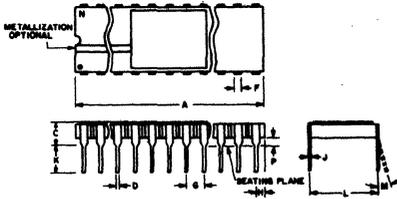
5. N is the maximum quantity of lead positions.

6. N₁ is the quantity of allowable missing leads.

Dimensional Outlines (Cont'd)

Dual-In-Line Side-Braced Ceramic Packages

D SUFFIX



16-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	—	0.830		—	21.08
C	—	0.200		—	5.08
D	0.015	0.021		0.381	0.533
F	0.045	0.070	1	1.143	1.778
G	0.100	BSC	1	2.54	BSC
H	0.015	0.090		0.381	2.286
J	0.008	0.012	3	0.203	0.304
K	0.125	0.150		3.175	3.810
L	0.290	0.310	2	7.366	7.874
M	0°	15°		0°	15°
P	0.020	—		0.508	—
N	16			16	

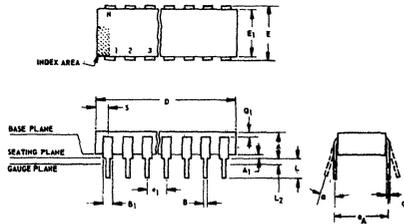
92CS-31130

18-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.890	0.915		22.606	23.241
C	—	0.200		—	5.080
D	0.015	0.021		0.381	0.533
F	0.054	REF.	1	1.371	REF.
G	0.100	BSC	1	2.54	BSC
H	0.035	0.065		0.889	1.651
J	0.008	0.012	3	0.203	0.304
K	0.125	0.150		3.175	3.810
L	0.290	0.310	2	7.366	7.874
M	0°	15°		0°	15°
P	0.025	0.045		0.635	1.143
N	18			18	

92CS-27231R1

20-Lead



SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.105	0.175	6	2.667	4.445
A ₁	0.025	0.055	6	0.635	1.397
B	0.015	0.021	—	0.381	0.533
B ₁	0.038	0.060	—	0.965	1.524
C	0.008	0.015	—	0.203	0.381
D	0.970	1.020	—	24.638	25.908
E	0.290	0.325	—	7.366	8.255
E ₁	0.280	0.310	5	7.112	7.874
e ₁	0.090	0.110	1	2.286	2.794
e _A	0.300 TP		1, 2	7.620 TP	
L	0.125	0.175	6	3.175	4.445
L ₂	0.000	0.030	—	0.000	0.762
α	0°	15°	3	0°	15°
N	20		4	20	
Q ₁	0.005	—	—	0.127	—
S	0.030	0.065	—	0.762	1.651

92CM-35139

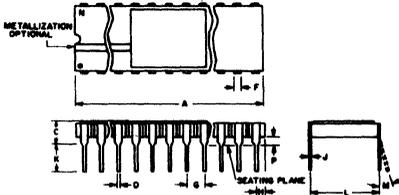
NOTES:

- Leads within 0.005" (0.13 mm) radius of True Position (T.P.) at gauge plane with maximum material condition and unit installed. Lead spacing e₁ shall be non-cumulative and shall be measured at the lead tip. This measurement shall be made before insertion into gauges, boards, or sockets.
- e_A applies in zone L₂ when unit is installed.
- α applies to spread leads prior to installation.
- N is the number of terminal positions.
- E₁ does not include particles of package materials.
- This dimension shall be measured with the device seated in the seating plane gauge JEDEC Outline No. GS-3.

Dimensional Outlines (Cont'd)

Dual-In-Line Side-Brazed Ceramic Packages

D SUFFIX



22-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	1.085	1.085		27.06	27.55
C	0.090	0.150		2.29	3.81
D	0.017	0.023		0.44	0.58
F	0.040 REF.			1.02 REF.	
G	0.100 BSC		1	2.54 BSC	
H	0.030	0.045		0.77	1.14
J	0.008	0.012	3	0.21	0.30
K	0.125	0.145		3.18	3.68
L	0.390	0.420	2	9.91	10.66
M	—	7°		—	7°
P	0.025	0.050		0.64	1.27
N	22			22	

92CS-25186R3

24-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	1.180	1.220		29.98	30.98
C	0.085	0.145		2.16	3.68
D	0.015	0.023		0.39	0.58
F	0.040 REF.			1.02 REF.	
G	0.100 BSC		1	2.54 BSC	
H	0.030	0.070		0.77	1.77
J	0.008	0.012	3	0.21	0.30
K	0.125	0.175		3.18	4.44
L	0.580	0.620	2	14.74	15.74
M	—	7°		—	7°
P	0.025	0.050		0.64	1.27
N	24			24	

92CS-30886R1

28-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	1.380	1.420		35.06	36.06
C	0.085	0.145		2.16	3.68
D	0.017	0.023		0.43	0.56
F	0.050 REF.		1	1.27 REF.	
G	0.100 BSC		1	2.54 BSC	
H	0.030	0.070		0.76	1.78
J	0.008	0.012	3	0.20	0.30
K	0.125	0.175		3.18	4.45
L	0.580	0.620	2	14.74	15.74
M	—	7°		—	7°
P	0.025	0.050		0.64	1.27
N	28			28	

92CM-26419R1

40-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	1.980	2.020		50.30	51.30
C	0.095	0.155		2.43	3.93
D	0.017	0.023		0.43	0.56
F	0.050 REF.			1.27 REF.	
G	0.100 BSC		1	2.54 BSC	
H	0.030	0.070		0.76	1.78
J	0.008	0.012	3	0.20	0.30
K	0.125	0.175		3.18	4.45
L	0.580	0.620	2	14.74	15.74
M	—	7°		—	7°
P	0.025	0.050		0.64	1.27
N	40			40	

92CM-27029R2

NOTES:

1. Leads within 0.005" (0.13 mm) radius of True Position at maximum material condition.
2. Center to center of leads when formed parallel.
3. When this device is supplied solder dipped, the maximum lead thickness (narrow portion) will not exceed 0.013" (0.33 mm).

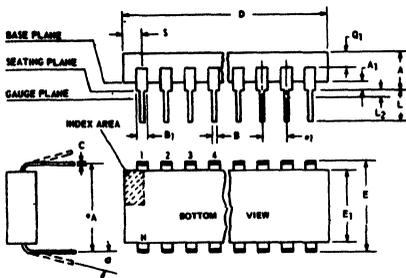
Dimensional Outlines (Cont'd)

Dual-In-Line Ceramic Package

D SUFFIX

16-Lead

24-Lead (JEDEC MO-015-AG)



NOTES:

- Refer to JEDEC Publication No. 95 for Rules for Dimensioning Axial Lead Product Outlines.
- 1. When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013" (0.33 mm).
- 2. Leads within 0.006" (0.127 mm) radius of True Position (TP) at gauge plane with maximum material condition.
- 3. e₁ and e_A apply in zone L₂ when unit is installed.
- 4. Applies to spread leads prior to installation.
- 5. N is the maximum quantity of lead positions.
- 6. N₁ is the quantity of allowable missing leads.

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.120	0.160		3.05	4.06
A ₁	0.020	0.065		0.51	1.65
B	0.014	0.020		0.356	0.508
B ₁	0.035	0.065		0.89	1.65
C	0.008	0.012	1	0.204	0.304
D	0.745	0.785		18.93	19.93
E	0.300	0.325		7.62	8.25
E ₁	0.240	0.260		6.10	6.60
e ₁	0.100 TP		2	2.54 TP	
e _A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L ₂	0.000	0.030		0.000	0.76
α	0°	15°	4	0°	15°
N	16		5	16	
N ₁	0		6	0	
Q ₁	0.050	0.085		1.27	2.15
S	0.015	0.060		0.39	1.52

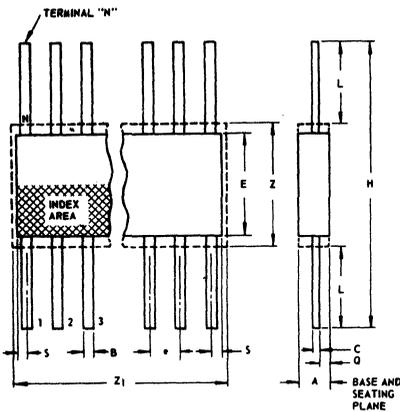
92SS-4286R5

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.090	0.200		2.29	5.08
A ₁	0.020	0.070		0.51	1.78
B	0.015	0.020		0.381	0.508
B ₁	0.045	0.055		1.143	1.397
C	0.008	0.012	1	0.204	0.304
D	1.15	1.22		29.21	30.98
E	0.600	0.625		15.24	15.87
E ₁	0.480	0.520		12.20	13.20
e ₁	0.100 TP		2	2.54 TP	
e _A	0.600 TP		2, 3	15.24 TP	
L	0.100	0.180		2.54	4.57
L ₂	0.000	0.030		0.00	0.76
α	0°	15°	4	0°	15°
N	24		5	24	
N ₁	0		6	0	
Q ₁	0.020	0.080		0.51	2.03
S	0.020	0.060		0.51	1.52

92CS-19948R4

Ceramic Flat Pack

K SUFFIX*



92CS-19949R2

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.075	0.120		1.91	3.04
B	0.018	0.022	1	0.458	0.558
C	0.004	0.007	1	0.102	0.177
e	0.050 TP		2	1.27 TP	
E	0.600	0.700		15.24	17.78
H	1.150	1.350		29.21	34.29
L	0.225	0.325		5.72	8.25
N	24		3	24	
Q	0.035	0.070		0.89	1.77
S	0.060	0.110	1	1.53	2.79
Z	0.700		4	17.78	
Z ₁	0.750		4	19.05	

NOTES:

- 1. Refer to JEDEC Publication No. 95 for Rules for Dimensioning Peripheral Lead Outlines.
- 2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at maximum material condition.
- 3. N is the maximum quantity of lead positions.
- 4. Z and Z₁ determine a zone within which all body and lead irregularities lie.

*This package is used for CD4036K and CD4039AK types only.

Application Notes - Abstracts

ICAN-6315 COS/MOS Interfacing Simplified	8
Example of practical circuits for a wide variety of interfacing situations are given in this Note; design constraints are included in each case.	
ICAN-6416 An Introduction to Microprocessors and the RCA COSMAC COS/MOS Microprocessor	8
This Note is an introduction to the fundamentals of microprocessors and to the specific capabilities of the RCA COSMAC microprocessor.	
ICAN-6525 Guide to Better Understanding and Operation of COS/MOS Integrated Circuits	6
This Note recommends specific handling and operating practices that minimize the probability of damage to CMOS integrated circuits in the manufacturing operation and the field environment.	
ICAN-6536 Use of CMOS ROMs CDP1831 and CDP1832 with the RCA Microprocessor Evaluation Kit CDP18S020*	4
This application note describes the operation and design of CDP1831- and CDP1832-based read-only memory systems in the CDP18S020 Evaluation Kit.	
ICAN-6537 Use of CMOS RAM CDP1824 with the RCA Microprocessor Evaluation Kit CDP18S020*	4
This Note describes the CDP1824, its application in the CDP18S020 Evaluation Kit, and presents examples of how the CDP1824 can be combined with the CDP1831 ROM to form efficient ROM-RAM systems.	
ICAN-6538 Use of the CDP1852 8-Bit I/O Port with the RCA Microprocessor Evaluation Kit CDP18S020*	4
This Note describes several applications of the CDP1852 I/O port and especially explains its use in the CDP18S020 Evaluation Kit.	
ICAN-6539 Use of CMOS-SOS RAM CDP1822 with the RCA Microprocessor Evaluation Kit CDP18S020*	4
This application note describes the CDP1822, its operation, and its application in the CDP18S020 Evaluation Kit.	
ICAN-6562 Register-Based Output Function for RCA COSMAC Microprocessors	2
This Note describes a circuit for use with RCA COSMAC Microprocessors; the circuit provides the capability to output information from any of the 16 general-purpose scratchpad registers contained within the CPU.	
ICAN-6565 Design of Clock Generators for use with the RCA COSMAC Microprocessor CDP1802	4
This Note describes clock generator designs suitable for various applications.	
ICAN-6581 Power-On Reset/Run Circuits for the RCA CDP1802 COSMAC Microprocessor	2
This Note describes several circuits which enable a power-on reset/run capability for COSMAC microprocessor systems.	
ICAN-6595 Interfacing Analog and Digital Displays with CMOS Integrated Circuits	12
This Note describes some of the COS/MOS integrated circuits most suitable for interfacing the electronic circuit display.	
ICAN-6602 Interfacing COS/MOS with Other Logic Families	12
This Note describes the conditions governing the interface of COS/MOS logic circuits with other logic families.	
ICAN-6611 Keyboard Scan Routine for Use with the RCA COSMAC Microterminal CDP18S021	4
This Note contains the code for such a keyboard reading routine which can be added as a subroutine to the user program, thereby making the Microterminal useful as a general-purpose input as well as output device.	
ICAN-6632 Use of the CDP1854 UART with RCA Microprocessor Evaluation Kit CDP18S020 or EK/Assembler-Editor Design Kit CDP18S024*	6
This application note describes several methods of interfacing the CDP1854 with the CDP1802 microprocessor and specifically explains the use of the CDP1854 in the CDP18S020 and CDP18S024 kits.	
ICAN-6635 Use of CMOS ROMs CDP1833 and CDP1834 with the RCA Microprocessor Evaluation Kit CDP18S020 and the EK/Assembler-Editor Design Kit CDP18S024*	4
The CDP18S020 Evaluation Kit and the CDP18S024 EK/Assembler-Editor Design Kit are designed to accept the CDP1833 and CDP1834 as described in this application note.	
ICAN-6657 Use of the CDP1856 and CDP1857 Buffer/Separator in CDP1802 Microprocessor Systems	4
This Note describes the uses of the CDP1856 and CDP1857 and, more specifically, how they may be utilized in the RCA Evaluation Kit, CDP18S020, and the EK/Assembler-Editor Design Kit, CDP18S024.	
ICAN-6693 CDP1802-Based Designs Using the 8253 Programmable Counter/Timer	4
The 8253 programmable interval timer, manufactured by Intel Corp., is an integrated circuit containing three independent 16-bit counters, each programmable in any of six modes. This Note describes methods by which it can be incorporated in RCA COSMAC-based microprocessor systems.	
ICAN-6704 Optimizing Hardware/Software Trade-offs in RCA CDP1802 Microprocessor Applications	12
This Note will develop some examples of processor interfaces that not only minimize external hardware but, through judicious programming techniques, also minimize speed requirements on the CPU.	
ICAN-6834 Microprocessor Control for Color-TV Receivers	12
This Note describes a microprocessor control for a color-TV receiver, a control that supports a large number of features and options.	
ICAN-6842 16-Bit Operations in the CDP1802 Microprocessor	6
This paper describes various software routines and a few interface circuits that can be used to manipulate full 16-bit values in the CDP1802.	
ICAN-6847 Programming 2732 PROMs with the CDP18S480 PROM Programmer	4
This Note describes the techniques utilizing the PROM Programmer to program Intel 2732 PROMs.	
ICAN-6883 Simplified Design of Astable RC Oscillators Using the CD4060B or Two CMOS Inverters	2
Application notes are available that deal with theoretical approaches to oscillator design; this Note stresses practical aspects of design and provides easy-to-use algebraic equations that permit values of R and C for a given oscillator frequency to be quickly determined.	

*Note: The information in this Application Note is useful here; the Evaluation Kit, however, is no longer available.

Application Notes - Abstracts (Cont'd)

- ICAN-6889**
Using Slower Memories with the VIS Display System 4
 The scheme described in this Note, while requiring a few more parts, very nearly doubles the memory access-time requirement of the system and permits the use of memories approximately half as fast as those normally required with the VIS system.
- ICAN-6901**
CDP1802 Microprocessor-Based Setback Thermostat 8
 This Note describes an inexpensive, programmable, setback thermostat circuit, based on the RCA CDP1802 microprocessor that can be used to control both heating and air-conditioning systems.
- ICAN-6918**
A Methodology for Programming COSMAC 1802 Applications Using Higher-Level Languages 4
 This Note defines a method of optimizing the time-critical portions of programs written in higher-level languages for COSMAC 1802 applications by recording those portions in assembly language.
- ICAN-6925**
Understanding and Using the CDP18U42 EPROM 8
 This Note describes the design and programming characteristics of the RCA CDP18U42 nonvolatile ultraviolet-erasable /programmable read-only memory.
- ICAN-6928**
Interfacing PLM Code to CDOS System Functions 6
 This application note defines a method for interfacing PLM programs to CDOS system functions without the need for assembly language; the interface is an array of PLM procedures (which can be included in a PLM library) and supportive macro definitions, all of which are described in detail and used in a sample program.
- ICAN-6934**
Cassette Tape I/O for COSMAC Microprocessor Systems... 12
 This Note describes a circuit and the software needed to add a low-cost cassette-tape input and output to the COSMAC Evaluation Kit (CDP18S020, CDP18S024, and CDP18S025), the COSMAC Developmental System (CDP18S005 and CDP-18S007), or the Microboard Prototyping Kit (CDP18S691).
- ICAN-6943**
Designing Minimum/Nonvolatile Memory Systems with CMOS Static RAMs 28
 This Note details the system considerations and circuit requirements for CDP1800-series RAM operation and data retention in CDP1802-based systems.
- ICAN-6948**
Parallel Clocking of Sequential CMOS Devices 2
 This Note shows the equations for modeling the maximum permitted clock input rise time, t_{ACL} for sequential devices.
- ICAN-6953**
An Introduction to the Video Interface System (VIS) Devices—CDP1869 and CDP1870 12
 This Note describes a circuit and the software required to mate the RCA-CDP1869 and CDP1870 VIS (Video Interface System) chip set to the Evaluation Kit, CDP18S020.
- ICAN-6955**
Using the COSMAC Microboard Battery-Backup RAM, CDP18S622 6
 This Note discusses the application of the board as a standard power backup medium, a nonvolatile transport medium, and as an efficient means of aiding the testing of new or prototype boards.
- ICAN-6957**
CDP1804 and CDP1805 Processors Improve System Performance and Lower Chip Count 6
 This Note describes the CDP1804 and CDP1805 enhancement to the capability of the CDP1802 microprocessor, both in higher performance and additional system functions, while maintaining upward software and hardware capability.
- ICAN-6968**
New CMOS CDP1800-Series Processors Reduce Chip Count 4
 This Note describes the CDP1804 and CDP1805 devices having combined CPU, memory, and peripheral functions on a single chip, and provide a compact system design with the additional portability offered by battery-operation.
- ICAN-6970**
Understanding and Using the CDP1855 Multiply/Divide Unit 12
 This Note describes the CDP1855 MDU as an efficient hardware replacement for the software-only implementation of arithmetic and signal-processing algorithms.
- ICAN-6971**
New CMOS CDP1800-Series Processors Enhance System Performance 6
 This Note is devoted to a discussion of the attributes of the CDP1804 and CDP1805, both of which are hardware and software upward-compatible with the CDP1802.
- ICAN-6991**
A Slave CDP1802 Serial Printer Buffer System 8
 This Note describes a CDP1802-based stand-alone line printer buffer that links a master processor system to a serial printer through an RS232C interface.
- ICAN-7009**
New CDP1805 Microprocessor Upgrades CDP1800-Based Systems 6
 This Note describes specific CDP1805 features and explains how they are optimally applied in microcomputer systems.
- ICAN-7020**
Multimicroprocessor-based Transistor Test Equipment 8
 This Note discusses a modern test system that meets these demands through its ability to perform multiple-temperature testing of traditional and custom parameters in one insertion.
- ICAN-7023**
CDP1800-Series Peripherals - Building Blocks of a Complete Processor Family 8
 This Note discusses the host of peripheral chips available from RCA that make available to the system designer the functions, flexibility, and performance levels that once were only achieved with NMOS.
- ICAN-7026**
Microboard Equipment Control 6
 This Note discusses the project to build a piece of equipment to demonstrate the use of RCA Microboards in specialized manufacturing-test equipment. The specific example selected was the testing of some active parameters of power transistors.
- ICAN-7029**
Low-Power Techniques for Use with CMOS CDP1800-Based Systems 6
 This Note describes various techniques for reducing the power requirements of microcomputer systems since battery life is so important in most portable applications and in systems having RAM battery-back-up provision.
- ICAN-7032**
CDP1800-Based Video Terminal Using the RCA Video Interface System, VIS 36
 This Note discusses the RCA Video Interface System, VIS, chip set CDP1869, CDP1870, and CDP1876 for use in video terminals, industrial displays, and broadcast-TV text overlays.
- ICAN-7038**
A CDP1800-Based CRT Controller 8
 This Note discusses the addition of the Video Interface System, VIS, to the peripheral support line for the CDP1800-series microprocessors.
- ICAN-7063**
Understanding the CDP1851 Programmable I/O 6
 This Note discusses the general-purpose programmable I/O port, CDP1851, having 20 I/O pins which may be used in several different modes of operation.
- ICAN-7067**
VIS - A Commercially Competitive CRT Controller Chip Set 4
 This Note discusses the VIS as an economical solution to a variety of CRT display applications.

Related Technical Publications

Microsystem and Microboard Product Descriptions

MB-601	Microboard Computer, CDP18S601
MB-602	Microboard Computer, CDP18S602
MB-603	Microboard Computer, CDP18S603
MB-604B	Microboard Computer, CDP18S604B
MB-620	Microboard 4-Kilobyte RAM, CDP18S620
MB-621	Microboard 16-Kilobyte RAM, CDP18S621
MB-622	Microboard 8-Kilobyte Battery-Backup RAM, CDP18S622
MB-623	Microboard 8-Kilobyte RAM, CDP18S623
MB-623A	Microboard 8-Kilobyte RAM CDP18S623A
MB-624	Microboard 4-Kilobyte Battery-Backup RAM, CDP18S624
MB-625	Microboard 8/16/32-Kilobyte ROM/PROM, CDP18S625
MB-626	Microboard 32/64-Kilobyte EPROM/ROM/RAM
MB-627	Microboard 4-Kilobyte CMOS EPROM CDP18S627
MB-629	Microboard 32-Kilobyte RAM
MB-640	Microboard Control and Display Module, CDP18S640
MB-640V1	Microboard Control and Display Module, CDP18S640V1
MB-641	Microboard UART Interface, CDP18S641
MB-642	Microboard D/A Converter, CDP18S642
MB-643	Microboard A/D Converter, CDP18S643
MB-644	Microboard A/D and D/A Converters, CDP18S644 and CDP18S654
MB-647	Microboard D/A Converters, CDP18S647 and CDP18S657
MB-648	Microboard A/D Converters, CDP18S648 and CDP18S658
MB-659	Microboard Breadboard, CDP18S659
MB-660	Microboard Combination Memory and I/O Module, CDP18S660
MB-661	Microboard Video-Audio-Keyboard Interface, CDP18S661V1 and CDP18S661V3
MB-661B	Microboard Video/Audio/Keyboard Interface CDP18S661B
MB-670	Microboard 22-Card Chassis with Integral Power Supply CDP18S670
MB-675	Microboard 5-Card Chassis, CDP18S675 and CDP18S676 (with case)
MB-691	Microboard Prototyping System, CDP18S691 and CDP18S691V3
MB-692	Microboard Prototyping System, CDP18S692
MPM-920B	CDP1802 Microprocessor Instruction Summary
PD6	Fixed-Point Arithmetic Subroutine
PD7	Floating-Point Arithmetic Subroutine
PD8	COSMAC Development System IV CDP18S008
PD10	COSMAC Dictionary
PD12	COSMAC Microterminal
PD13	Microboard Computer Development Systems (MCDS) CDP18S683 and CDP18S694
PD14	Color Microboard Computer Development System CDP18S695
PD16C	COSMAC Development Systems
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PD24	EK/Assembler-Editor
PD30	ROM Purchase Policy and Programming Instructions
PD31	Micromonitor Operating System (MOPS)
PD34	BASIC1 Compiler/Interpreter (CDP18S834)
PD37A	Disk Operating System Upgrade Package (CDP18S837)
PD39	PLM 1800 High-Level-Language Compiler (CDP18S839)
PD40	BASIC2 High-Level-Language Interpreter CDP18S840
PD44	Micro Concurrent PASCAL Cross-Compiler CDP18S844 and Interpreter/Kernel CDP18S852 and CDP18S853

Product Guides

CMB-250B	COSMAC Microboard Computer Systems
MPG-180D	COSMAC Microprocessor Product Guide
MPL-200	Microsystems Product Guide and Price List

DATABOOKS

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SSD-280	LSI Products - Applications
SSD-230A	High-Reliability IC Products

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