INTEGRATED CIRCUITS

DATA HANDBOOK

Programmable Logic Devices (PLD)

BOOK IC 1 3 1 9 9 2

Signetics

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Programmable Logic Devices

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Preface

The 1992 Philips Semiconductors–Signetics PLD Data Handbook is loaded with information on new parts. Using the fastest technologies in the most innovative architectures, today's system designer can pick from the largest selection of PLDs in the industry. Featured in 1992 are the ultra high-speed BiCMOS devices designed to be pin, function, and fusemap identical to existing industry standard parts. Some highlights of this handbook include the fastest silicon PLDs available (PHD16N8 and PHD48N22)—at 5 nanoseconds! These devices make ideal decoders to squeeze maximum performance from powerful microprocessors. If that's not fast enough, check out the 10H20EV8 at 4.5 nanoseconds!

Designers using DRAM, VRAM and graphics will appreciate the speed and power of the new line of sequencers which include the PLC415, PLC42VA12, PLUS405 and PLUS105. These sequencers also make innovative bus and LAN controllers for emerging standard protocols.

At last, the logical power of dual programmable arrays comes forth in the PLUS153 and PLUS173 devices—at 10 nanosecond propagation delays.

The PLC18V8Z is the only zero power 20-pin device which can replace 16V8's!

For maximum density in a truly compact system, the Programmable Macro Logic family now boasts three members—the PML2552, the PML2852, and the original PLHS501. The PML2552 is the PLD industry's first dense device to implement SCAN test.

To complement the devices, SLICE design software is offered through our Sales Offices (see Section 11) and SNAP software is available for high level support. Read about them under Product Support.

Expanding customer service has been an ongoing effort. Our Applications staff continues to answer your technical questions on PLD designs and our free computer Bulletin Board, with 24-hour service, is at (800)451-6644.

Product Status

DEFINITIONS		
Data Sheet Identification	**Product Status**	**Definition**
Objective Specification	**Formative or In Design**	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	**Preproduction Product**	This data sheet contains preliminary data and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	**Full Production**	This data sheet contains Final Specifications. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

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PAL is a registered trademark of AMD.

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PAL DEVICES									
10H20EV8–4/ 10020EV8–4	20 × 90 × 8	24-Pin	20 (12)	8 to 12	0	8 varied	4.5ns	208MHz	–250mA
PHD16N8–5	16 × 16 × 8	20-Pin	16 (10)	1♦	0	2 C, 6 I/O	5ns		180mA
PHD48N22–7	48 × 73 × 22	68-Pin	48 (36)	7 to 12	0	10 C, 12 I/O	7.5ns		420mA
PLUS16L8–7	16 × 64 × 8	20-Pin	16 (10)	7	0	2 C, 6 I/O	7.5ns		180mA
PLUS16R4–7	16 × 64 × 8	20-Pin	16 (8)	7 to 8	4 (0)	4 I/O, 4 R	7.5ns	74MHz	180mA
PLUS16R6–7	16 × 64 × 8	20-Pin	16 (8)	7 to 8	6 (0)	2 I/O, 6 R	7.5ns	74MHz	180mA
PLUS16R8–7	16 × 64 × 8	20-Pin	16 (8)	8	8 (0)	8 R		74MHz	180mA
PLUS16L8D	16 × 64 × 8	20-Pin	16 (10)	7	0	2 C, 6 I/O	10ns		180mA
PLUS16R4D	16 × 64 × 8	20-Pin	16 (8)	7 to 8	4 (0)	4 I/O, 4 R	10ns	60MHz	180mA
PLUS16R6D	16 × 64 × 8	20-Pin	16 (8)	7 to 8	6 (0)	2 I/O, 6R	10ns	60MHz	180mA
PLUS16R8D	16 × 64 × 8	20-Pin	16 (8)	8	8 (0)	8 R		60MHz	180mA
PLUS20L8–7	20 × 64 × 8	24-Pin	20 (14)	7	0	2 C, 6 I/O	7.5ns		210mA
PLUS20R4–7	20 × 64 × 8	24-Pin	20 (12)	7 to 8	4 (0)	4 I/O, 4 R	7.5ns	74MHz	210mA
PLUS20R6–7	20 × 64 × 8	24-Pin	20 (12)	7 to 8	6 (0)	2 I/O, 6 R	7.5ns	74MHz	210mA
PLUS20R8–7	20 × 64 × 8	24-Pin	20 (12)	8	8 (0)	8 R		74MHz	210mA
PLUS20L8D	20 × 64 × 8	24-Pin	20 (14)	7	0	2 C, 6 I/O	10ns		210mA
PLUS20R4D	20 × 64 × 8	24-Pin	20 (12)	7 to 8	4 (0)	4 I/O, 4R	10ns	60MHz	210mA
PLUS20R6D	20 × 64 × 8	24-Pin	20 (12)	7 to 8	6 (0)	2 I/O, 6 R	10ns	60MHz	210mA
PLUS20R8D	20 × 64 × 8	24-Pin	20 (12)	8	8 (0)	8 R		60MHz	210mA
PLQ16L8–5	16 × 64 × 8	20-Pin	16 (10)	7	0	2 C, 6 I/O	5ns		180mA
PLQ16R4–5	16 × 64 × 8	20-Pin	16 (8)	7 to 8	4 (0)	4 I/O, 4 R	5ns	118MHz	180mA
PLQ16R6–5	16 × 64 × 8	20-Pin	16 (8)	7 to 8	6 (0)	2 I/O, 6R	5ns	118MHz	180mA
PLQ16R8–5	16 × 64 × 8	20-Pin	16 (8)	8	8 (0)	8 R		118MHz	180mA
PLQ20L8D	20 × 64 × 8	24-Pin	20 (14)	7	0	2 C, 6 I/O	5ns		210mA
PLQ20R4D	20 × 64 × 8	24-Pin	20 (12)	7 to 8	4 (0)	4 I/O, 4R	5ns	118MHz	210mA
PLQ20R6D	20 × 64 × 8	24-Pin	20 (12)	7 to 8	6 (0)	2 I/O, 6 R	5ns	118MHz	210mA
PLQ20R8D	20 × 64 × 8	24-Pin	20 (12)	8	8 (0)	8 R		118MHz	210mA
PLQ22V10-7	22 × 130 × 10	24-Pin	22 (12)	8 to 16	10 (0)	10 varied	7.5ns	87MHz	180mA
PL22V10-15/I15	22 × 130 × 10	24-Pin	22 (12)	8 to 16	10 (0)	10 varied	15ns	53MHz	110mA, 0.5mA/MHz
PL22V10–12	22 × 130 × 10	24-Pin	22 (12)	8 to 16	10 (0)	10 varied	12ns	67MHz	110mA, 0.5mA/MHz
PL22V10–10	22 × 130 × 10	24-Pin	22 (12)	8 to 16	10 (0)	10 varied	10ns	77MHz	110mA, 0.5mA/MHz
PLC18V8Z35 PLC18V8ZI	18 × 74 × 8	20-Pin	18 (8)	8	8 (0)	8 varied	35, 40ns	21MHz	100µA, 1.5mA/MHz
PLC18V8Z25 PLC18V8ZAI	18 × 74 × 8	20-Pin	18 (8)	8	8 (0)	8 varied	25ns	30MHz	100µA, 1.5mA/MHz
PLA									
PLS100/101	16 × 48 × 8	28-Pin	16 (16)	Up to 48	0	8 C	50ns		170mA
PLS153	18 × 42 × 10	20-Pin	18 (8)	Up to 32	0	10 I/O	40ns		155mA
PLS153A	18 × 42 × 10	20-Pin	18 (8)	Up to 32	0	10 I/O	30ns		155mA
PLUS153B	18 × 42 × 10	20-Pin	18 (8)	Up to 32	0	10 I/O	15ns		200mA
PLUS153D	18 × 42 × 10	20-Pin	18 (8)	Up to 32	0	10 I/O	12ns		200mA
PLUS153–10	18 × 42 × 10	20-Pin	18 (8)	Up to 32	0	10 I/O	10ns		200mA
PLS173	22 × 42 × 10	24-Pin	22 (12)	Up to 32	0	10 I/O	30ns		170mA
PLUS173B	22 × 42 × 10	24-Pin	22 (12)	Up to 32	0	10 I/O	15ns		200mA
PLUS173D	22 × 42 × 10	24-Pin	22 (12)	Up to 32	0	10 I/O	12ns		200mA
PLUS173–10	22 × 42 × 10	24-Pin	22 (12)	Up to 32	0	10 I/O	10ns		210mA

Selection guide

SIGNETICS PART NUMBER	ARCHITECTURE (Inputs × Terms* × Outputs)	PACKAGE	TOTAL INPUTS (# Dedicated)	PRODUCT TERMS PER OR GATE	INTERNAL STATE REGISTERS (# Dedicated)	OUTPUTS C, I/O, R, R I/O	t_{PD} (Max)	f_{MAX}	I_{CC} (Max)
PLS									
PLS105	22 × 48 × 8	28-Pin	22 (16)	Up to 48	6 (6)	8 R		14MHz	180mA
PLS105A	22 × 48 × 8	28-Pin	22 (16)	Up to 48	6 (6)	8 R		20MHz	180mA
PLUS105–45	22 × 48 × 8	28-Pin	22 (16)	Up to 48	6 (6)	8 R		45MHz	200mA
PLUS105–55	22 × 48 × 8	28-Pin	22 (16)	Up to 48	6 (6)	8 R		55MHz	200mA
PLUS405–37	24 × 64 × 8	28-Pin	24 (16)	Up to 64	8 (8)	8 R		37MHz	225mA
PLUS405–45	24 × 64 × 8	28-Pin	24 (16)	Up to 64	8 (8)	8 R		45MHz	225mA
PLUS405–55	24 × 64 × 8	28-Pin	24 (16)	Up to 64	8 (8)	8 R		55MHz	225mA
PLS155	16 × 45 × 12	20-Pin	16 (4)	Up to 32	4 (0)	8 I/O, 4 R I/O	50ns	14MHz	190mA
PLS157	16 × 45 × 12	20-Pin	16 (4)	Up to 32	6 (0)	6 I/O, 6 R I/O	50ns	14MHz	190mA
PLS159A	16 × 45 × 12	20-Pin	16 (4)	Up to 32	8 (0)	4 I/O, 8 R I/O	35ns	18MHz	190mA
PLS167	22 × 48 × 6	24-Pin	22 (14)	Up to 48	8 (6)	6 R		14MHz	180mA
PLS167A	22 × 48 × 6	24-Pin	22 (14)	Up to 48	8 (6)	6 R		20MHz	180mA
PLS168	22 × 48 × 8	24-Pin	22 (12)	Up to 48	10 (6)	8 R		14MHz	180mA
PLS168A	22 × 48 × 8	24-Pin	22 (12)	Up to 48	10 (6)	8 R		20MHz	180mA
PLS179	20 × 45 × 12	24-Pin	20 (8)	Up to 32	8 (0)	4 I/O, 8 R I/O	35ns	18MHz	210mA
PLC42VA12/I	42 × 105 × 12	24-Pin	42 (10)	Up to 64	10 (0)	10 I/O or R I/O, 2 I/O	35ns	25MHz	135mA
PLC415–16	25 × 68 × 8	28-Pin	25 (17)	Up to 64	8 (8)	8 R		16MHz	100µA/ 80mA
PML									
PLHS501	104 × 116 × 24	52-Pin	32 (24)	Up to 136♦	0	16 C, 8 I/O	22ns		295mA
PML2552–35	205 × 210 × 24	68-Pin	53 (29)	Up to 258♦	36 (20)	8 I/O, 16 R I/O	35ns	50MHz	10mA/ 100mA
PML2552–50	205 × 210 × 24	68-Pin	53 (29)	Up to 258♦	36 (20)	8 I/O, 16 R I/O	50ns	35MHz	10mA/ 100mA
PML2852–35	205 × 210 × 40	84-Pin	53 (29)	Up to 258♦	36 (20)	16 C, 8 I/O, 16 R I/O	35ns	50MHz	10mA/ 100mA
PML2852–50	205 × 210 × 40	84-Pin	53 (29)	Up to 258♦	36 (20)	16 C, 8 I/O, 16 R I/O	50ns	35MHz	10mA/ 100mA

PAL Device = Programmable Array Logic (Fixed OR Array)-Type
PHD = Programmable High-Speed Decoder
PLA = Programmable Logic Array
PLS = Programmable Logic Sequencer
PML = Programmable Macro Logic

OUTPUTS:
C = Combinatorial output
R = Registered output
I/O = Combinatorial I/O
R I/O = Registered I/O

NOTES:
$f_{MAX} = 1/(t_{IS} + t_{CKO})$ worst case
* Includes control product terms
♦ Product terms per NAND gate
PAL is a registered trademark of AMD.
PML is a trademark of Signetics.

All packages refer to DIP configurations except PHD48N22, PML2552 and PML2852, which are offered in PLCC only.

Ordering information

PLD PRODUCTS

Example: P(L) XX YYYY Q P

Package Code
- F = 20-, 24-, 28-Pin Ceramic Dual In-Line
- N = 20-, 24-, 28-Pin Plastic Dual In-Line
- A = 20-, 28-, 52-, 68-lead Plastic Leaded Chip Carrier (PLCC)
- FA = 20-, 24-Pin Ceramic Dual In-Line with Quartz Window
- KA = CerQuad (window)

Performance indicator
- Z = Zero standby power devices
- blank, A, B, D, -35, -7, etc. = propagation delay (ns)
- -37, -45, -55, etc. = operating frequency (MHz)

Basic Part Number
- (3 to 8 characters)
- (e.g., 100, 105, 153, 168, 173, 18P8, 42VA12)

Process/Architecture Indicator
- S = Bipolar Junction Isolated Schottky – Nichrome fuses
- C = CMOS – EPROM cells
- HS = High Speed Bipolar Oxide Isolated – Vertical Fuse
- US = High Speed Bipolar Oxide Isolated – Lateral Fuse
- HD = High Speed Decoder
- ML = Macro Logic
- (Blank for ECL devices)

Indicator for Signetics Programmable Logic
- (Can be either P, PL, or blank)
- (P for PHD and PML and blank for ECL devices)

Operating temperature range = 0 to +70°C
EXCEPT: PLC18V8ZI= -40 to +85°C

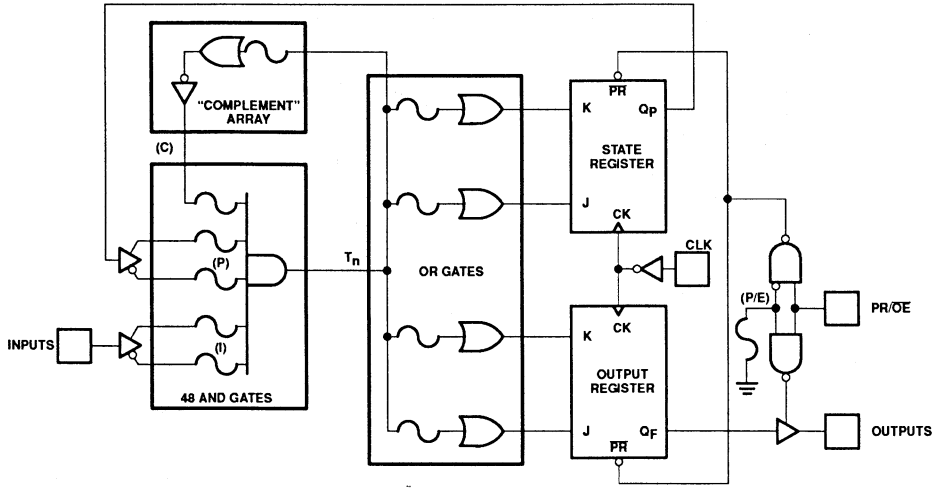
Section 2
Introduction

INDEX

WHAT IS PROGRAMMABLE LOGIC?

In 1975, Signetics Corporation developed a new product family by combining its expertise in semi-custom gate array products and fuse-link Programmable Read Only Memories (PROMs). Out of this marriage came Signetics Programmable Logic Family. The PLS100 Field-Programmable Logic Array (FPLA) was the first member of this family. The FPLA was an important industry first in two ways. First, the AND/OR/INVERT architecture allowed the custom implementations of Sum of Product logic equations. Second, the three-level fusing allows complete flexibility in the use of this device family. All logic interconnections from input to output are programmable.

Figure 1 shows the architecture of a high performance sequencer combining a PLA architecture with JK flip-flops. The Selection Guide shown on pages 4 and 5 of this data handbook shows the current spectrum of Philips Semiconductors–Signetics PLDs. Parts for every need are available in nearly every architecture and across at least three technologies. The PLUS and PLHS prefixes describe bipolar parts, the PLC prefix describes EPLD (CMOS) parts and the PLQ prefix refers to the new Signetics QUBiC BiCMOS process. Figure 2 shows a shorthand image of the PLUS153 programmable logic array (PLA), which was derived from the original PLS100.



NOTES:
I, P, C, N, F and P/E are user-programmable connections.

Figure 1. High Speed Sequencer

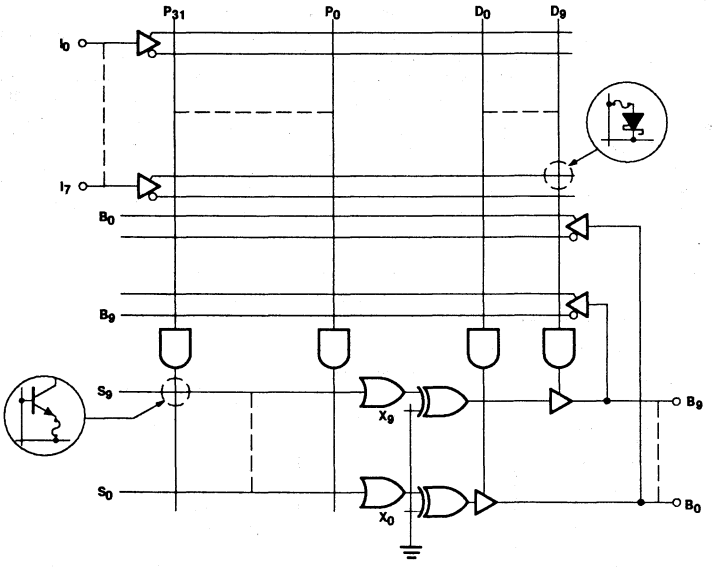


Figure 2. PLUS153 20-Pin Functional Diagram

PLD LOGIC SYNTHESIS

No intermediate step is required to implement Boolean Logic Equations with PLDs. Each term in each equation simply becomes a direct entry into the Logic Program Table. The following example illustrates this straightforward concept:

$X_0 = AB + \overline{C}D + B\overline{D}$

$\overline{X}_1 = \overline{A}B + \overline{C}D + EFG$

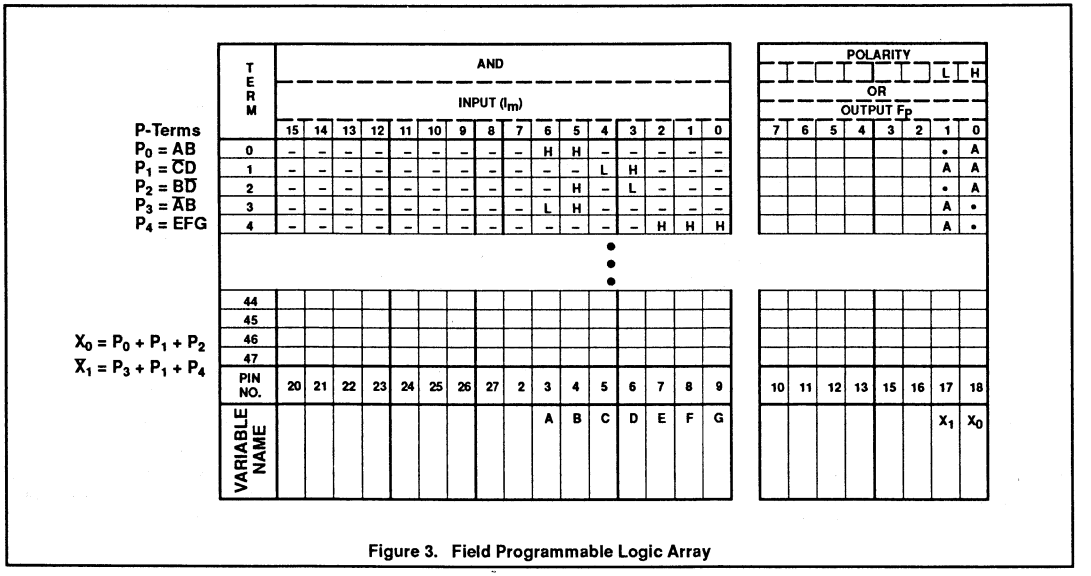


Figure 3. Field Programmable Logic Array

Figure 4. Equivalent Fixed Logic Diagram

In the previous example, the two Boolean Logic equations were broken into Product terms. Each P-term was then programmed into the P-term section of the PLA Program Table. This was accomplished in the following manner:

Step 1

Select which input pins $I_0 - I_{15}$ will correspond to the input variables. In this case A – G are the input variable names. I_6 through I_0 were selected to accept inputs A – G respectively.

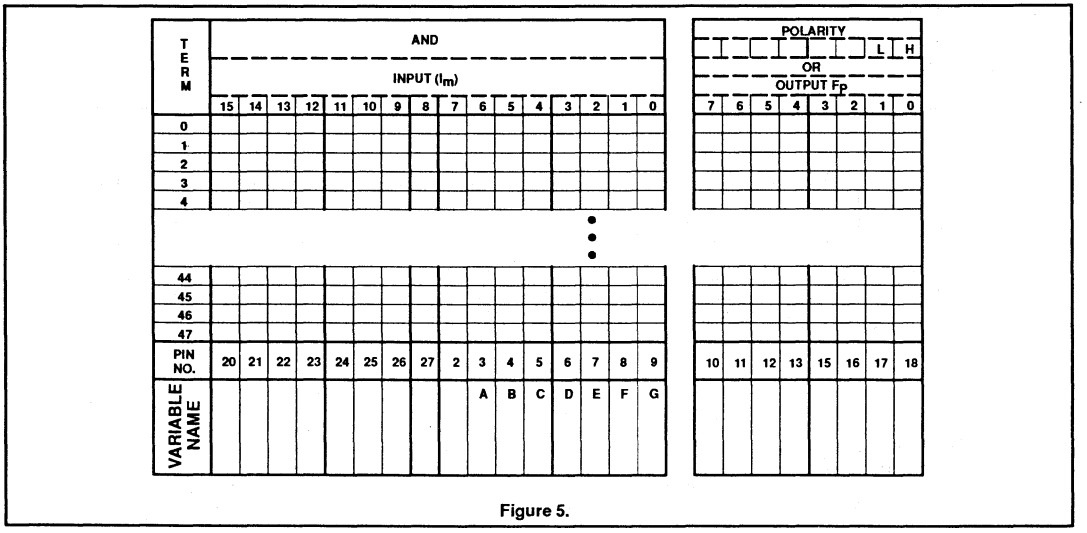


Figure 5.

Step 2

Transfer the Boolean Terms to the PLA Program Table. This is done simply by defining each term and entering it on the Program Table.

e.g., $P_0 = AB$

This P-term translates to the Program Table by selecting $A = I_6 = H$ and $B = I_5 = H$ and entering the information in the appropriate column.

$P_1 = \overline{C}D$

This term is defined by selecting $C = I_4 = L$ and $D = I_3 = H$, and entering the data into the Program Table. Continue this operation until all P-terms are entered into the Program Table.

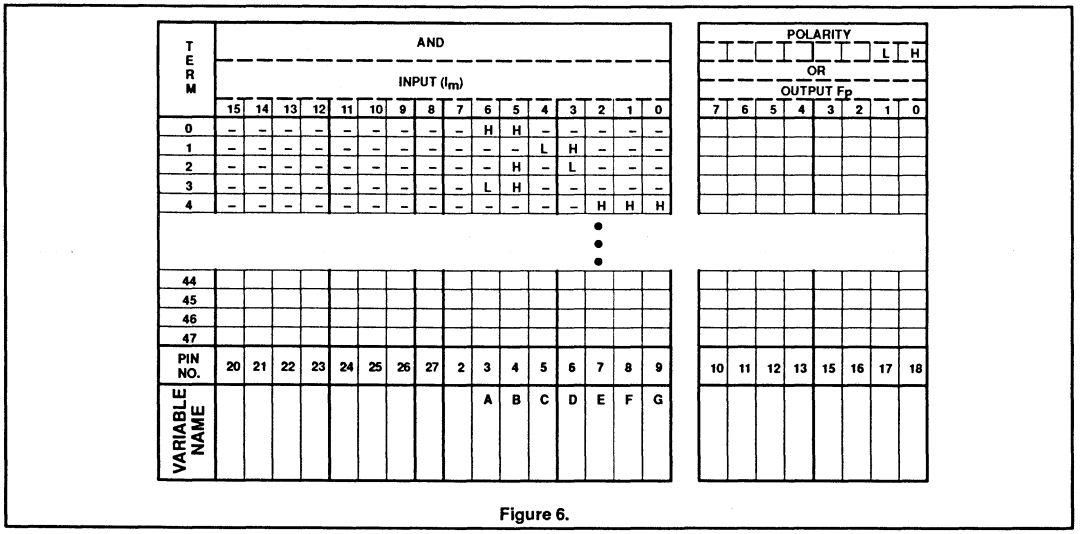


Figure 6.

Step 3

Select which output pins correspond to each output function. In this case F_0 = Pin 18 = X_0, and F_1 = Pin 17 = X_1.

TERM	AND INPUT (I_m) 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POLARITY / OR / OUTPUT Fp 7	6	5	4	3	2	1	0
0	–	–	–	–	–	–	–	–	–	H	H	–	–	–	–	–								
1	–	–	–	–	–	–	–	–	–	–	–	L	H	–	–	–								
2	–	–	–	–	–	–	–	–	–	–	H	–	L	–	–	–								
3	–	–	–	–	–	–	–	–	–	L	H	–	–	–	–	–								
4	–	–	–	–	–	–	–	–	–	–	–	–	–	H	H	H								
• • •																								
44																								
45																								
46																								
47																								
PIN NO.	20	21	22	23	24	25	26	27	2	3	4	5	6	7	8	9	10	11	12	13	15	16	17	18
VARIABLE NAME										A	B	C	D	E	F	G							X_1	X_0

Figure 7.

Step 4

Select the Output Active Level desired for each Output Function. For X_0 the active level is high for a positive logic expression of this equation. Therefore, it is only necessary to place an (H) in the Active Level box above Output Function 0, (F_0). Conversely, X_1 can be expressed as $\overline{X}_1$ by placing an (L) in the Active Level box above Output Function 1, (F_1).

TERM	AND INPUT (I_m) 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POLARITY L H / OR / OUTPUT Fp 7	6	5	4	3	2	1	0
0	–	–	–	–	–	–	–	–	–	H	H	–	–	–	–	–								
1	–	–	–	–	–	–	–	–	–	–	–	L	H	–	–	–								
2	–	–	–	–	–	–	–	–	–	–	H	–	L	–	–	–								
3	–	–	–	–	–	–	–	–	–	L	H	–	–	–	–	–								
4	–	–	–	–	–	–	–	–	–	–	–	–	–	H	H	H								
• • •																								
44																								
45																								
46																								
47																								
PIN NO.	20	21	22	23	24	25	26	27	2	3	4	5	6	7	8	9	10	11	12	13	15	16	17	18
VARIABLE NAME										A	B	C	D	E	F	G							X_1	X_0

Figure 8.

Step 5

Select the P-Terms you wish to make active for each Output Function. In this case $X_0 = P_0 + P_1 + P_2$, so an A has been placed in the intersection box for P_0 and X_0, P_1 and X_0 and P_2 and X_0.

Terms which are not active for a given output are made inactive by placing a (•) in the box under that P-term. Leave all unused P-terms unprogrammed.

Continue this operation until all outputs have been defined in the Program Table.

Step 6

Enter the data into a Signetics approved programmer. The input format is identical to the Signetics Program Table. You specify the P-terms, Output Active Level, and which P-terms are active for each output exactly the way it appears on the Program Table.

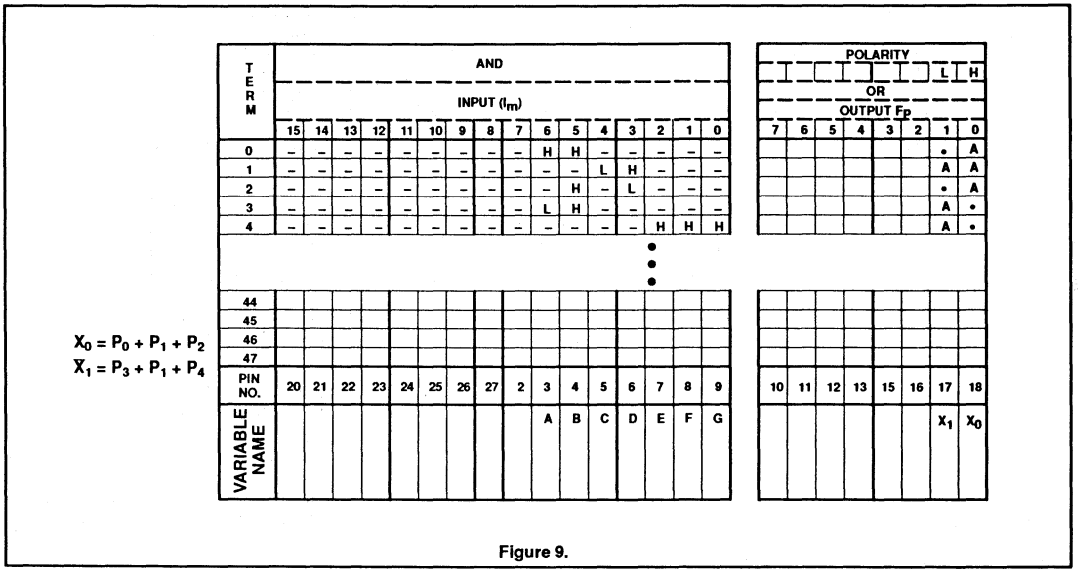


Figure 9.

PLD LOGIC SYNTHESIS (Continued)

When fewer inputs and outputs are required in a logic design and low cost is most important, the Signetics 20-pin PLD should be considered first choice. The PLUS153 is a PLA with 8 inputs, 10 I/O pins, and 42 product terms. The user can configure the device by defining the direction of the I/O pins. This is easily accomplished by using the direction control terms $D_0 - D_9$ to establish the direction of pins $B_0 - B_9$. The D-terms control the 3-State buffers found on the outputs of the Ex-OR gates. Figures 10 and 11 show how the D-term configures each B_X pin.

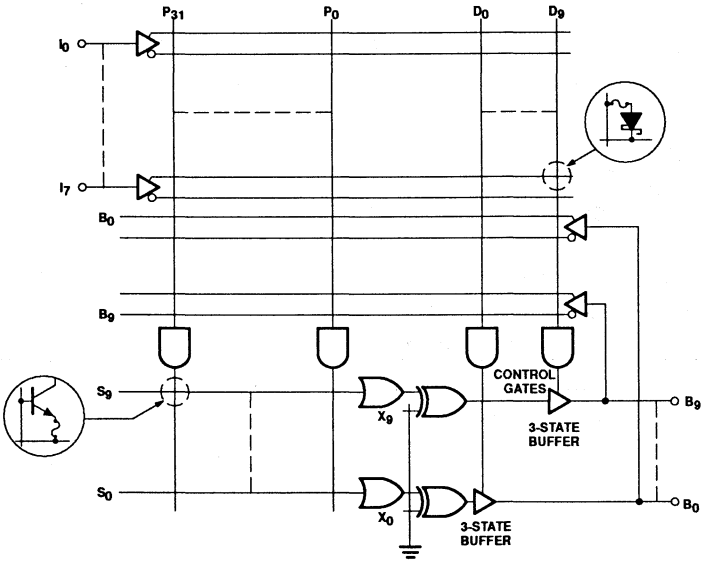
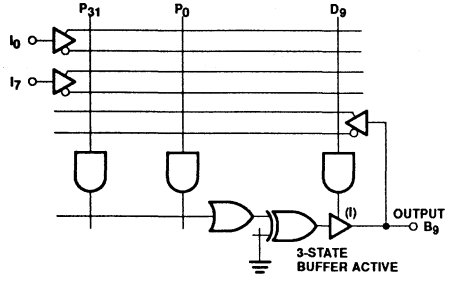
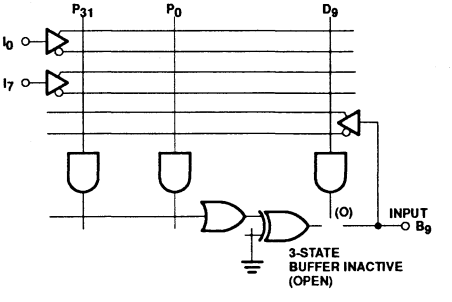


Figure 10. PLUS153 Functional Diagram



a. D_9 Active Makes B_9 Appear as an Output with Feedback



b. D_9 Inactive Makes B_9 Appear as an Input

Figure 11.

To control each D-term, it is necessary to understand that each control gate is a 36-input AND gate. To make the 3-State buffer active (B_x pin an output), the output of the control gate must be at logic HIGH (1). This can be accomplished in one of two ways. A HIGH can be forced on all control gate input nodes, or fuses can be programmed. When a fuse is programmed, that control gate input node is internally pulled up to HIGH (1). See Figure 12 and Figure 13.

Programming the fuse permanently places a HIGH (1) on the input to the control gate. The input pin no longer has any effect on that state.

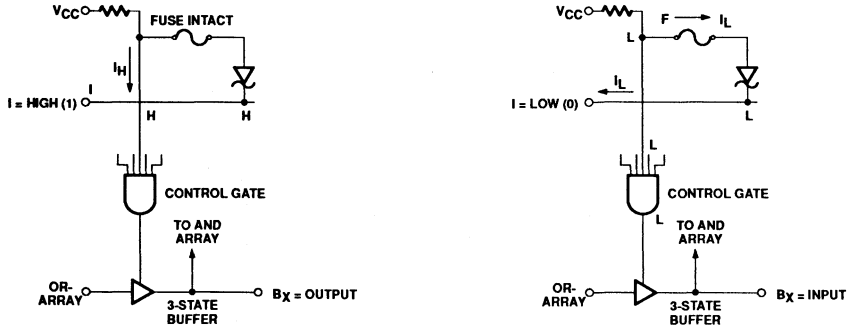


Figure 12. Input Effect on Control Gates (Fuse Intact)

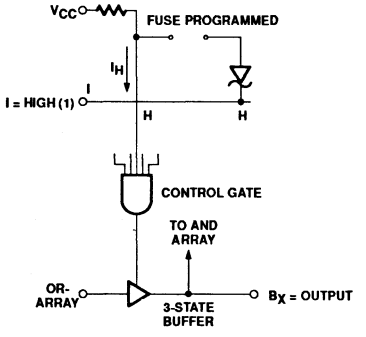


Figure 13. Effect on Control Gate if Fuse is Programmed

DEDICATING B_X PIN DIRECTION

Since each input to the D-terms is true and complement buffered (see Figure 11), when the device is shipped with all fuses intact, all control gates have half of the 36 input lines at logic low (0). The result of this is all Control Gate outputs are low (0) and the 3-State buffers are inactive. This results in all B_X pins being in the input condition. the resultant device is, therefore, an 18-input, 0-output FPLA. While useful as a bit bucket or Write-Only-Memory (WOM), most applications require at least one output. Clearly, the first task is to determine which of the B_X pins are to be outputs. The next step is to condition the control gate to make the 3-State buffer for those gates active. To dedicate B_0 and B_1 as outputs, it is necessary to program all fuses to the inputs to Control Gates D_0 and D_1. This internally pulls all inputs to those gates to HIGH (1) permanently. since all inputs to the Control Gates are HIGH (1), the output is HIGH (1) and the 3-State buffers for B_0 and B_1 are active. This permanently enables B_0 and B_1 as outputs. Note that even though B_0 and B_1 are outputs, the output data is available to the AND array via the internal feedback (see Figure 11a).

To program this data, the PLUS153 Program Table is used as shown in Figure 14.

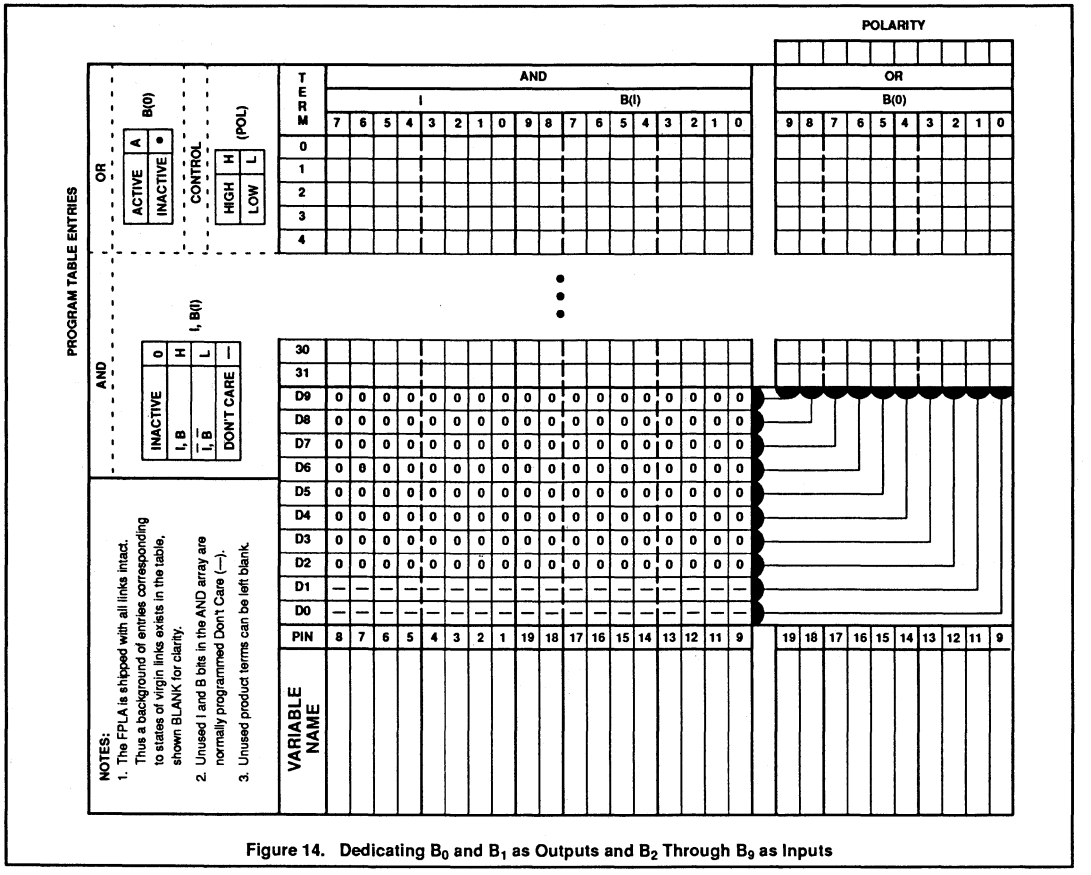


Figure 14. Dedicating B_0 and B_1 as Outputs and B_2 Through B_9 as Inputs

By placing a (—) Don't Care in each input box you are specifying that the True and Complement fuses are programmed on each Control Gate, thus permanently dedicating the B_0 and B_1 pins as outputs. By placing a (0) in all input boxes for B_2 - B_9, you are specifying that both True and Complement fuses are intact. This causes a low (0) to be forced on half of the Control Gate inputs, guaranteeing the output of the Control Gate will be low (0). When the Control Gate outputs are low (0), the 3-State buffer is inactive and the B_2 - B_9 pins are enabled as inputs. All B_X pin directions can be controlled in this manner.

ACTIVE DIRECTION CONTROL

Sometimes it is necessary to be able to actively change the direction of the B_X pins without permanently dedicating them. Some applications which require this include 3-State bus enable, multi-function decoding, etc. This can easily be done by programming the Control Gate to respond to one or more input pins. It is only necessary to select which I_X and B_X pins will control the pin directions and the active level HIGH (H) or LOW (L) that will be used. The PLUS153 Program Table in Figure 15 shows the method of controlling $B_0 - B_9$ with I_7. When I_7 is LOW (L), pins $B_0 - B_9$ are outputs; when I_7 is HIGH (H), pins $B_0 - B_9$ are inputs. Note that by programming all other I_X and B_X pins as DON'T CARE (—), they are permanently disconnected from control of B_X pin direction.

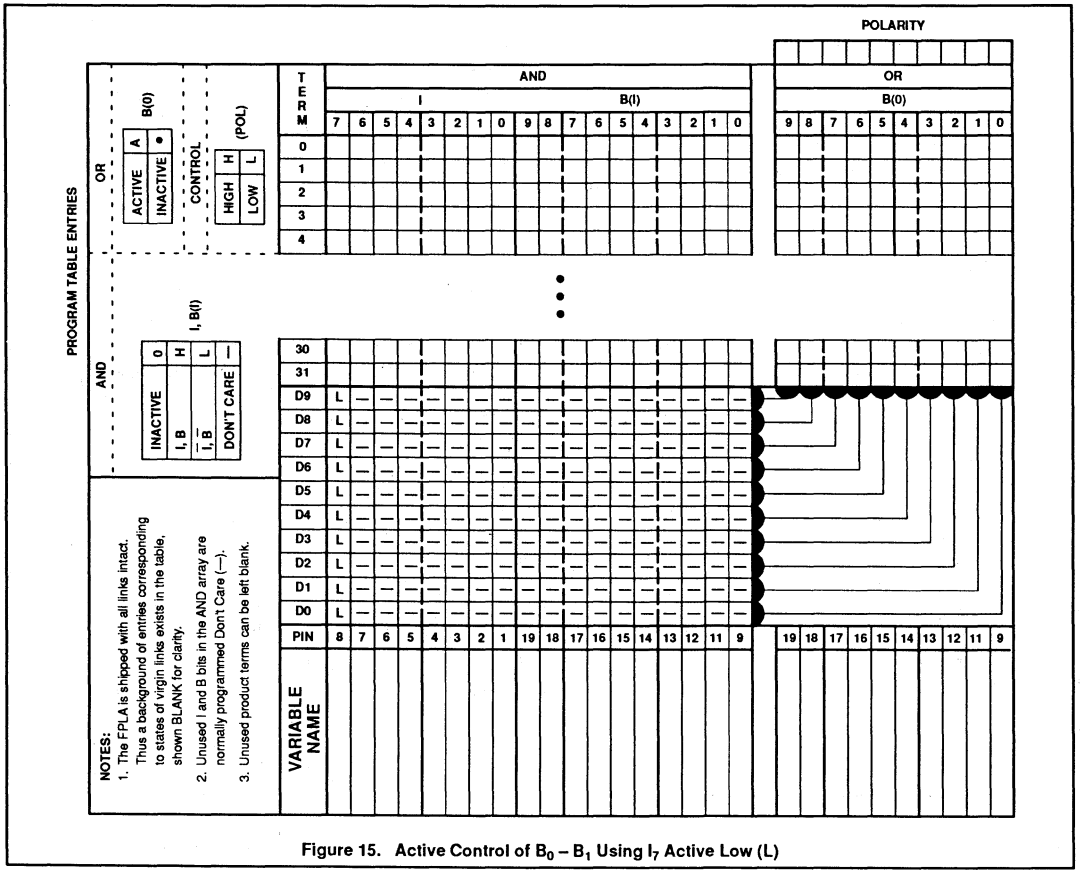


Figure 15. Active Control of $B_0 - B_1$ Using I_7 Active Low (L)

The previous 28-pin logic synthesis example could be done on the PLUS153 as follows:

$X_0 = AB + \overline{C}D + B\overline{D}$

$X_1 = \overline{A}B + \overline{C}D + EFG$

Note that B_0 was used as a CHANGE input. When B_0 is HIGH (H) the outputs appear on B_8 and B_9. When B_0 is LOW (L), the outputs appear on B_6 and B_7. B_1 through B_5 are not used and therefore left unprogrammed.

Signetics offers two packages for user-friendly design assistance. The first package, AMAZE, has evolved over 10 years to support Signetics programmable products with logic equation, state equation, and schematic entry. AMAZE can compile designs quite well for Signetics lower density parts. However, to satisfy the needs of Programmable Macro Logic users, Signetics developed an additional software package called SNAP. SNAP expands upon the capabilities of AMAZE in its approach to design implementation, more closely resembling a gate array methodology. Both of these products are described in more depth at a later point in this handbook.

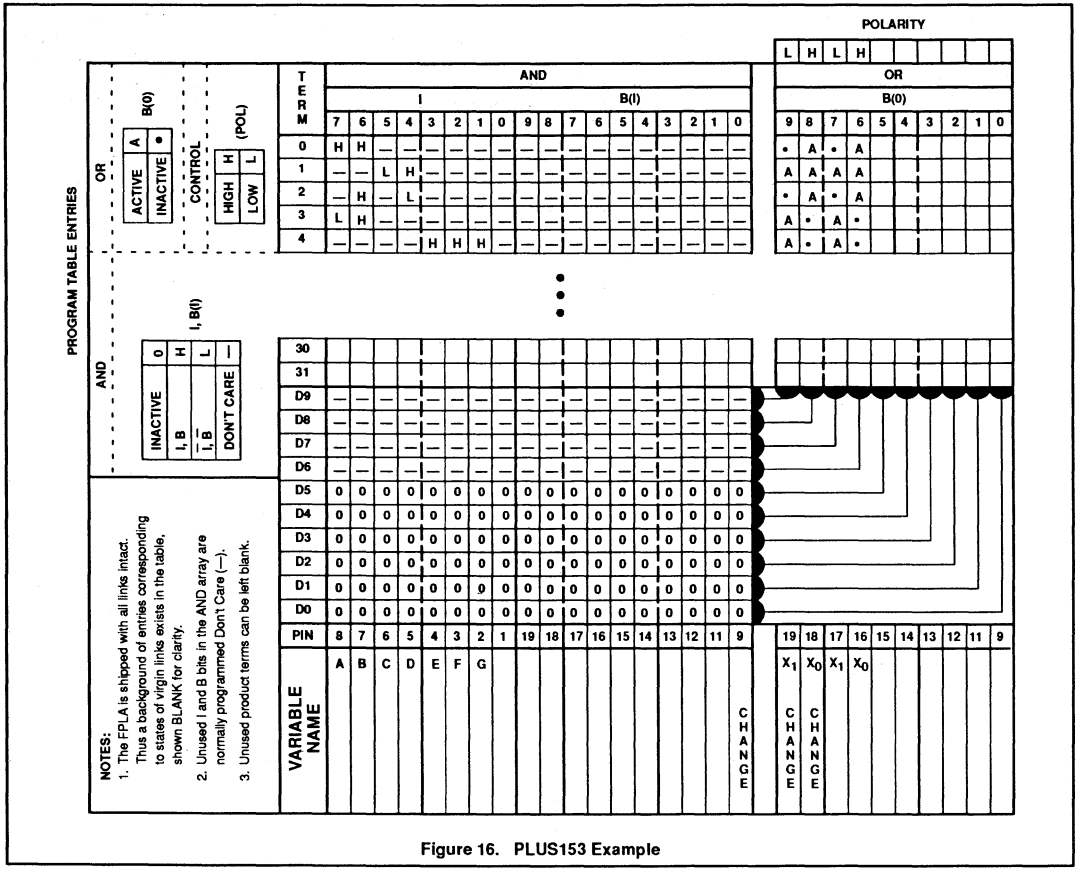


Figure 16. PLUS153 Example

SEQUENTIAL LOGIC CONSIDERATIONS

The PLUS405, PLUS105 and PLC42VA12 represent significant increases in complexity when compared to the combinatorial logic devices previously discussed. By combining the AND/OR combinatorial logic with clock output flip-flops and appropriate feedback, Signetics has created the first family of totally flexible sequential logic machines.

The PLUS405 (Programmable Logic Sequencer) is an example of a high-order machine whose applications are many. Application areas for this device include VRAM, DRAM, Bus and LAN control. The PLUS405 is fully capable of performing fast sequential operations in relatively high-speed processor systems. By placing repetitive sequential operations on the PLUS405, processor overhead is reduced.

The following pages summarize the PLUS405 architecture and features.

Sequencer Architecture

The PLUS405 Logic Sequencer is a programmable state machine, in which the output is a function of the present state and the present input.

With the PLUS405, a user can program any logic sequence expressed as a series of jumps between stable states, triggered by a valid input condition (I) at clock time (t). All stable states are stored in the State Register. The logic output of the machine is also programmable, and is stored in the Output Register. The PLUS105 is a subset of the PLUS405.

Clocked Sequence

A synchronous logic sequence can be represented as a group of circles interconnected with arrows. The circles represent stable states, labeled with an arbitrary numerical code (binary, hex, etc.) corresponding to discrete states of a suitable register. The arrows represent state transitions, labeled with symbols denoting the jump condition and the required **change** in output. The number of states in the sequence depends on the length and complexity of the desired algorithm.

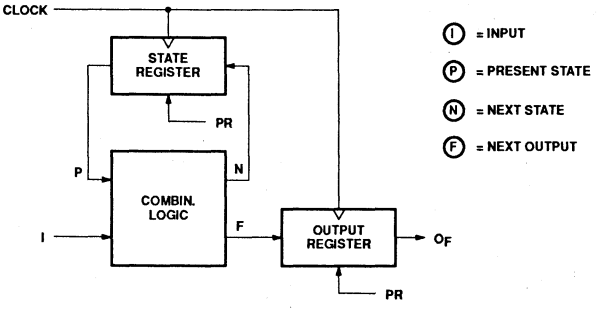
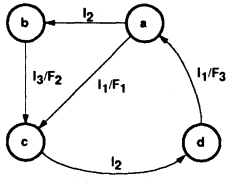
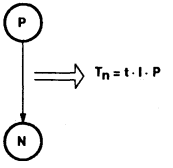


Figure 17. Basic Architecture of PLS105 FPLS. I, P, N, and F are Multi-line Paths Denoting Groups of Binary Variables Programmed by the User.



I_{1-3} are jump conditions which must be satisfied before any transitions take place.
F_r are changes in output triggered by I_m, and stored in the output register.
State transitions a → b and c → d involve no output change.

Figure 18. Typical State Diagram.



The arrow connecting the two states gives rise to a transition term T_n. I is the jump condition.

Figure 19. Typical State Transition Between Any Two States of Figure 18.

State Jumps

The state from which a jump originates is referred to as the Present state (P), and the state to which a jump terminates is defined as the Next state (N). A state jump always causes a change in state, but may or may not cause a change in machine output (F).

State jumps can occur only via "transition terms" T_n. These are logical AND functions of the clock (t), the Present state (P), and a valid input (I). Since the clock is actually applied to the State Register, $T_n = I \bullet P$. When T_n is "true", a control signal is generated and used at clock time (t) to force the contents of the State Register from (P) to (N), and to change the contents of the Output Register (if necessary). The simple state jump in Figure 20, involving 2 inputs, 1 state bit, and 1 output bit, illustrates the equivalence of discrete and programmable logic implementations.

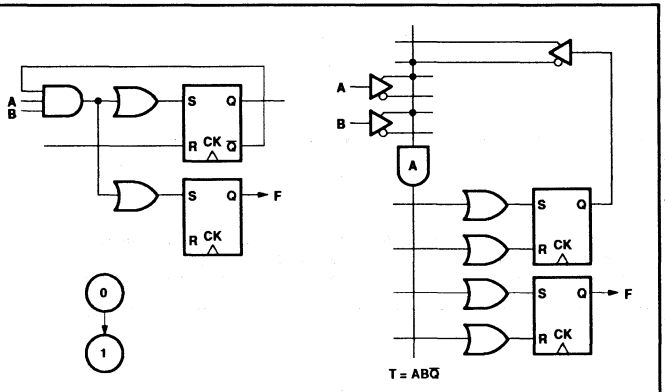


Figure 20. Typical State Jump From State (0) to State (1), if Inputs A = B = "1". The Jump Also Forces F = "1", as Required.

Sequencer Logic Structure

The Sequencer consists of programmable AND and OR gate arrays which control the Set and Reset inputs of a State Register, as well as monitor its output via an internal feedback path. The arrays also control an independent Output Register, added to store output commands generated during state transitions, and to hold the output constant during state sequences involving no output changes. If desired, any number of bits of the Output Register can be used to extend the width of the State Register, via external feedback.

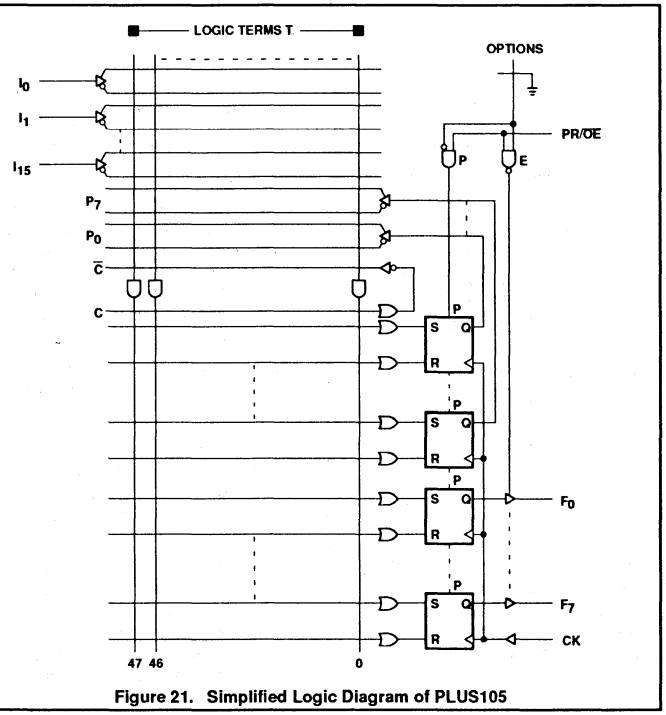


Figure 21. Simplified Logic Diagram of PLUS105

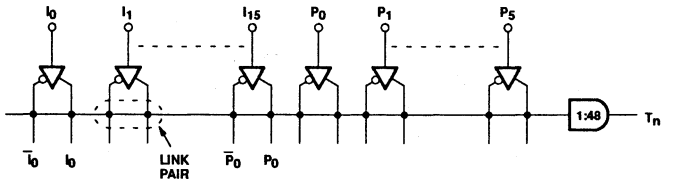


Figure 22. Typical AND Gate Coupled to (I) and (P) Inputs. If at Least One Link Pair Remains Intact, T_n is Unconditionally Forced Low.

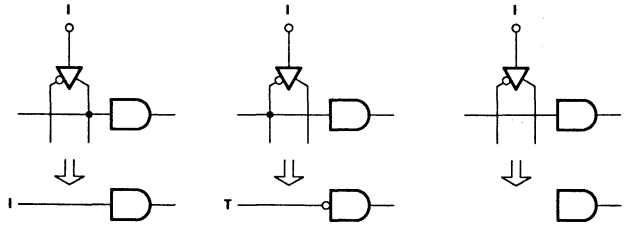


Figure 23. Choice of Input Polarity Coupling to a Typical AND Gate. With Both Links Open, (I) is Logically Don't Care.

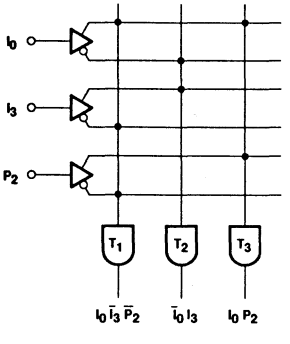


Figure 24. Typical Transition Terms Involving Arbitrary Inputs and State Variables. All Remaining Gate Inputs Are Programmed Don't Care. Note That T_2 Output is State Independent.

Input Buffers

16 external inputs (I_m) and 6 internal inputs (P_s), fed back from the State Register, are combined in the AND array through two sets of True/Complement (T/C) buffers. There are a total of 22 T/C buffers, all connected to multi-input AND gates via fusible links which are initially intact.

Selective fusing of these links allows coupling either True, Complement, or Don't Care values of (I_m) and (P_s).

"AND" Array

State jumps and output changes are triggered at clock time by valid transition terms T_n. These are logical AND functions of the present state (P) and the present input (I).

The PLUS105 AND Array contains a total of 48 AND gates. Each gate has 45 inputs – 44 connected to 22 T/C input buffers, and 1 dedicated to the Complement Array. The outputs of all AND gates are propagated through the OR Array, and used at clock time (t) to force the contents of the State Register from (P) to (N). they are also used to control the Output Register, so that the FPLS 8-bit output F_r is a function of the inputs and the present state. The PLUS405 contains 64 AND gates in its' AND array.

"OR" Array

In general, a clocked sequence will consist of several stable states and transitions, as determined by the complexity of the desired algorithm. All state and output changes in the state diagram imply changes in the contents of State and Output Registers.

Thus, each flip-flop in both registers may need to be conditionally set or reset several times with T_n commands. This is accomplished by selectively ORing through a programmable OR Array all AND gate outputs T_n necessary to activate the proper flip-flop control inputs.

The PLUS105 OR Array consists of 14 pairs of OR gates, controlling the S/R inputs of 14 State and Output Register stages, and a single NOR gate for the Complement Array. All gates have 48 inputs for connecting to all 48 AND gates. The PLUS405 uses 64 input gates.

The PLUS405 contains 16 pairs of OR gates controlling state transitions and output stages and two additional NOR gates for dual complement arrays.

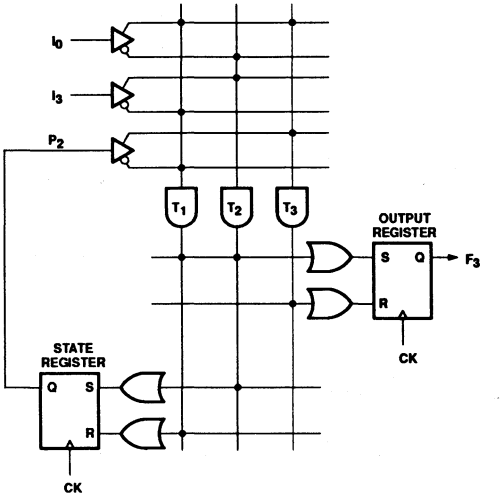


Figure 25. Typical OR Array Gating of Transition Terms $T_{1,2,3}$ Controlling Arbitrary State and Output Register Stages.

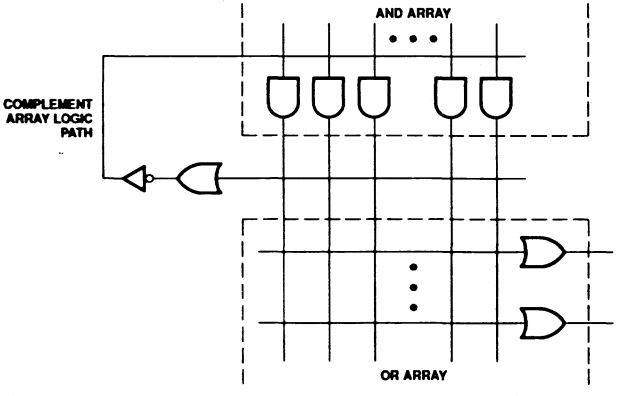
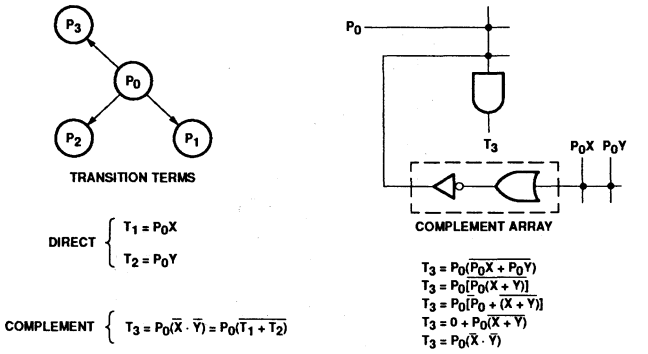


Figure 26. The COMPLEMENT Array is Logically Constructed from a Multiple Input Programmable NOR Gate. All AND Terms Coupled to the OR Gate are Complemented at the Inverter Output, and Can be Fed Back as Inputs to the AND Array.



a. Typical State Sequence b. Complement Jump

Figure 27.

a. X and Y Specify the Conditional Logic for Direct Jump Transition Terms T_1 and T_2. The Complement Jump Term T_3 is True Only When Both T_1 and T_2 are False.

b. Note that the Complementary Logic Expression for T_3, $\overline{T_1 + T_2}$, Corresponds Exactly to the Logic Structure of the Complement Array.

Complement Array

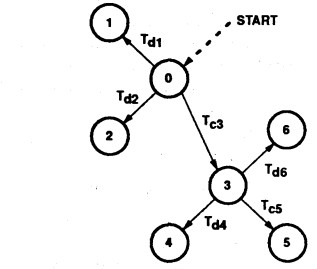
The COMPLEMENT Array provides an asynchronous feedback path from the OR Array back to the AND Array.

This structure enables the sequencer to perform both direct and complement sequential state jumps with a minimum of transition (AND) terms.

Typically direct jumps, such as T_1 and T_2 in Figure 27 require only a single AND gate each.

But a complement jump such as T_3 generally requires many AND gates if implemented as a direct jump. However, by using the Complement Array, the logic requirements for this type of jump can be handled with just one more gate from the AND Array. Because it can be split into separate machines (2 clocks), the PLUS405 incorporates two COMPLEMENT Arrays.

As indicated in Figure 28, the single Complement Array gate may be used for many states of the state diagram. This happens because all transition terms linked to the OR gate include the present state as a part of their conditional logic. In any particular state, only those transition terms which are a function of that state are enabled; all other terms coupled to different states are disabled and do not influence the output of the Complement Array. As a general rule of thumb, the Complement Array can be used as many times as there are states.



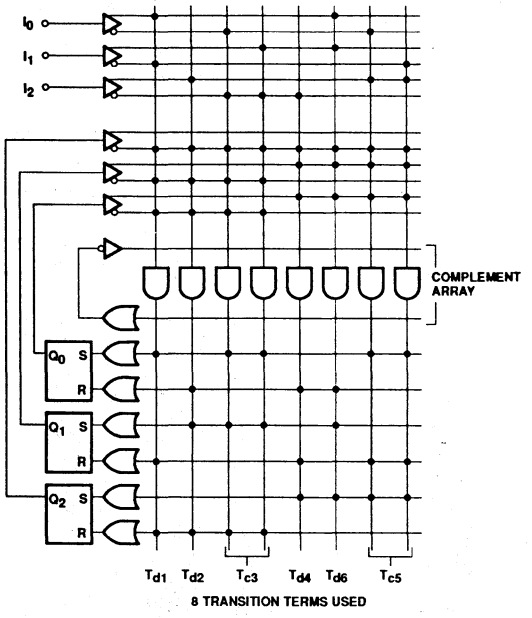
a. State Diagram

$T_{d1} = I_0 I_1 P_0$
$T_{d2} = I_2 P_0$
$T_{c3} = (\overline{T_{d1} + T_{d2}}) P_0 = (\overline{I_0 I_1 + I_2}) P_0$

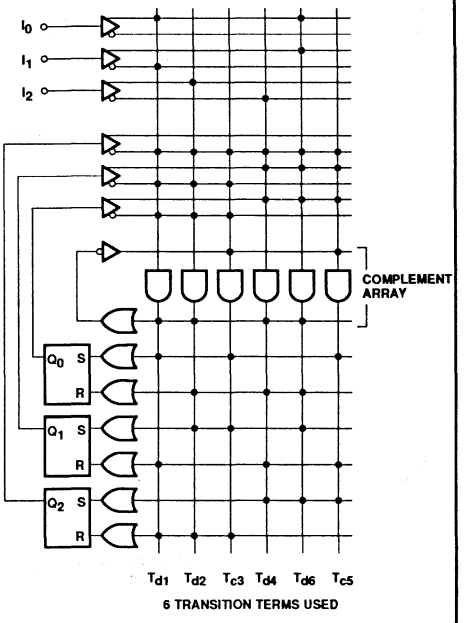
$T_{d4} = I_2 P_3$
$T_{d6} = I_0 I_1 P_0$
$T_{c5} = (\overline{T_{d4} + T_{d6}}) P_3 = (\overline{I_0 I_1 + I_2}) P_3$

T_{cn} = COMPLEMENT STATE TRANSITION TERM
T_{dn} = DIRECT STATE TRANSITION TERM
P_s = PRESENT STATE

b. Logic Definition



c. State Logic without Using the Complement Array



d. State Logic Using the Complement Array

Figure 28. Logic Reduction with the Complement Array. The Logic State Diagram in (a) Includes Complement Jumps T_{C3} and T_{C5} Defined in (b). When Using the Complement Array, a Savings of 2 Transition Terms Results, as Shown in (c) and (d).

Additional features are available depending on a specific part. In particular, the PLC42VA12 has everything mentioned here, and more. More details on PLAs, PAL devices and Sequencers can be found in the application section later in the manual.

Programmable Macro Logic, Signetics very high density logic is fully described in detail in its own section.

Quality and reliability

SUMMARY

The Signetics Company was founded in September, 1961 by a group of scientists and engineers who were among the pioneers in the development of integrated circuits. Signetics, acquired by Philips in 1975, was the first company in the world to be established for the sole purpose of designing, developing, manufacturing, and marketing ICs. Philips celebrated its 100th anniversary in 1991. On 1st January 1991, the Integrated Circuits and Discrete Semiconductor Business Units, formerly part of Philips Components, were merged into an autonomous product division (PD)—Philips Semiconductors as part of a major reorganization to focus Philips' semiconductor activities and to strengthen its standing in selected strategic markets. At the heart of this reorganization comes quality.

The Signetics approach to Quality Management has evolved with each evolution building upon the foundation laid. The emphasis in the 1960s and 1970s was quality by policy, documentation, and inspection. The emphasis in the 1980s was quality by employee involvement and process control. In the 1990s quality is achieved by emphasizing process and product Design For Manufacturability (DFM) and to customer requirements. (See Figure 1.) To ensure transformation, a formal Design Development Process (DDP) exists which requires the utilization of Cross-Functional Teams (CFTs) to assure that the customer Dimensions of Performance are met.

The modern Signetics Quality Journey (see Table 1) began in 1980. During the ensuing decade it achieved a 90-fold improvement in product electrical quality, 30-fold improvement in product visual and mechanical quality and a 20-fold improvement in product reliability. The great reduction in defect levels and a continued commitment to our customers made possible the following industry firsts:

- Ship-To-Stock Program
- Self-Qualification Program
- Zero Defects Warranty Policy

The Journey never ends—Signetics continues to strive for **EXCELLENCE** in all aspects of our business through company focus and initiatives aimed at achieving three performance level goals in 1994:

- Industry Leader in Customer Satisfaction
- With Products of Six Sigma Quality and Reliability
- And World Class Responsiveness to Customer Needs and Wants.

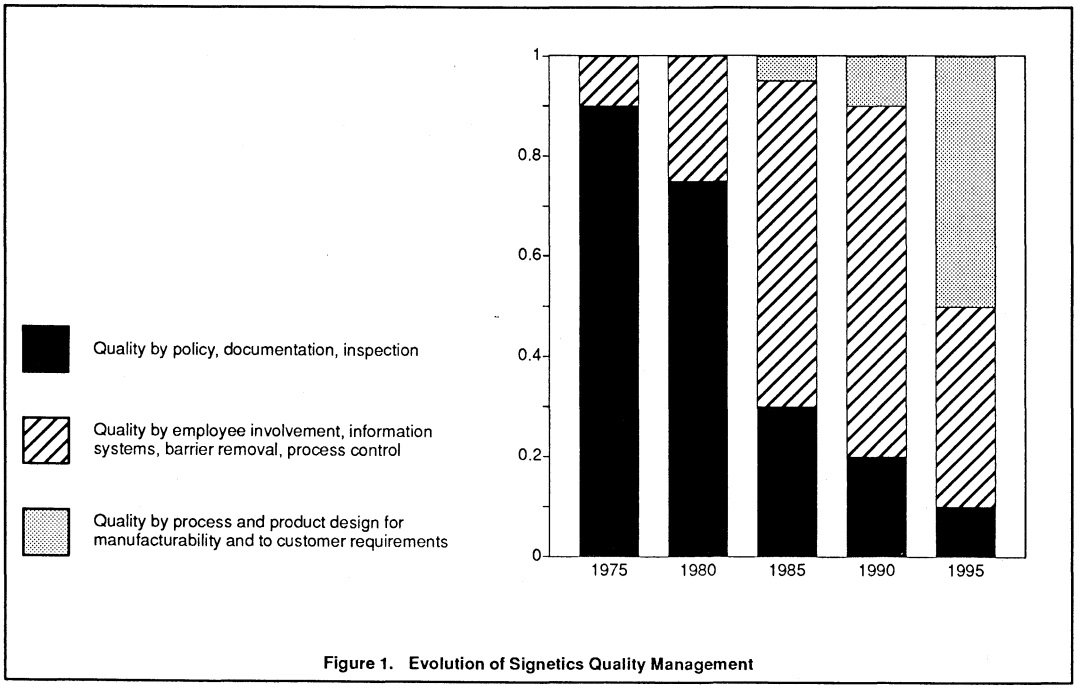


Figure 1. Evolution of Signetics Quality Management

Quality and reliability

SIGNETICS' QUALITY IMPROVEMENT PROCESS

In 1979, Signetics recognized that quality was becoming a major competitive issue, not only in the semiconductor business but also in other industries. Increases in the volume of products imported from the Far East (steel, automobiles, and consumer products) sent strong signals that new competitive forces were at work.

An investigation into a variety of quality programs was started. The company realized that quality improvement would require a contribution from all employees. Management commitment and participation, however, was recognized as the primary prerequisite for this program to work successfully. Resources required for the resolution of defects were under management control.

The "Signetics Quality Journey" from 1980 into the decade of the '90s is summarized in Table 1. In 1980 a program was developed which focused on quality management. Rearranging previous quality control philosophies, we developed a decentralized, distributed quality organization and simultaneously installed a Quality Improvement Process (QIP) based on the 14-Step improvement program advocated by Phil Crosby. The process was formally begun company-wide in 1981. Since then substantial progress has been made in every aspect of our operations. From incoming raw material conformance to improvements in clerical errors — every department and individual is involved and striving for Zero Defects. Zero Accept sampling plans and Zero Defects warranties are evidence of our ongoing commitment to and progress in quality. The Crosby 14 steps evolved into 9 elements as the foundation of the QIP. The QIP continued to expand, including more processes and disciplines as Signetics' vision cleared.

Today the Total Quality Management (TQM) model is applied to the QIP, as illustrated in Figure 2, having a far-reaching impact on all aspects of our business. The customer is at the start (driver) and end (goal) of the TQM model which requires a driver, system, measures and goal. The customer is the primary driver. Leadership is provided by Quality Improvement Teams (QITs) which ensure that customer interaction occurs and that the organization supports the mission, QI policy and customer direction. TQM requires a clear set of management principles which mandate systems and measurements consistent with stated objectives. TQM endorses and utilizes the seven major examination categories of the U.S.A. Malcolm Baldrige National Quality Award. Together, the examination categories address all major components of an integrated, prevention based system built around continuous improvement and customer satisfaction.

ZERO DEFECTS WARRANTY

In the '80s, American industry demanded increased product quality of its IC suppliers in order to meet growing international competitive pressure. As a result of this quality focus, it became clear that what once was thought to be unattainable— Zero Defects— is, in fact, achievable.

Signetics offers a Zero Defects Warranty which states that we will take back an entire lot if a single defective part is found. This precedent setting warranty implemented in 1985 effectively ended the IC industry's "war of the AQLs" (Acceptable Quality Levels). The ongoing efforts of IC suppliers to reduce PPM (Parts Per Million) defect levels is now a competitive customer service measure. This intense commitment to quality provides an advantage to today's electronics OEM. That advantage can be summed up in four words: ***Reduced Cost of Ownership.***

As IC customers look beyond purchase price to the total cost of doing business with a supplier, it is apparent that a quality-conscious supplier represents a viable cost reduction resource. Consistent high-quality circuits reduce requirements for expensive test equipment and personnel, and allow for smaller inventories, less rework, and fewer field failures. Programs such as Self Qualification and Ship-To-Stock implemented in 1984 and Cycle Time Management (CTM) implemented in 1989 help reduce cost of ownership.

STATISTICAL PROCESS CONTROL (SPC)

Although application of statistics in our process development and manufacturing activities goes back to the early 1970's, the corporate-wide emphasis on Statistical Process Control (SPC) did not come until mid-1984.

A natural evolution of our quality improvement process made introduction of SPC and other related programs an inevitable event. SPC was, therefore, introduced under the QIP umbrella. The Crosby definition of Quality, "Conformance To Requirements (Specification)" was expanded to include "Conformance To Specified Targets". The measurement definition of "continuous improvement" was expanded to include "Continuous Reduction of Variability Around the Specified Target".

The objective of SPC is to institutionalize a systematic and scientific approach to business and manufacturing activities. This approach utilizes sound statistical theory. Managers are expected to be able to turn data into information and to make decisions solely on data (not perception).

The most critical and challenging aspect of implementing SPC is the establishment of a discipline within the operating areas so that decision making is fundamentally based on verifiable data and so that actions are documented. The other is the realization that statistical tools merely point out the problems but are not themselves solutions. The burden of action on the process is still on the shoulders of the person that implemented it. In order to implement SPC effectively, three steps are continually followed:

1. Documenting and understanding the process and using process flow charts and component diagrams.
2. Establishing data collection systems and using SPC tools to identify process problems and opportunities for improvement.
3. Acting on the process and establishing guidelines to monitor and maintain process control.

Repeating steps 1-3 again.

These fundamentals are the basis of establishing specifications and operating philosophy with respect to SPC. The management of SPC, be it policy, function deployment or ongoing continuous improvement is accomplished in a systematic way by following the four step Plan, Do, Check, Act – PDCA/Shewart/Deming Cycles of Learning.

Quality and reliability

Table 1. Signetics Quality Journey

FOCUS		• Raw Material Quality • Product Quality • Individual Responsibility for Quality	• Supplier Partnerships • Manufacturing Excellence	• Customer Partnerships • In-process Quality Control • Product Reliability	• Cross Functional Operation • Better Management Practices • Cycle Time Management	• Customer Driven • Design Quality • Involve Everyone • Competitive & Functional Benchmarks
INITIATIVES	SUPPLIER	• No Waiver Policy • Audits • Certification Program	• Recognition • Ship-to-Stock (STS)	• SPC Implementation	• Measurement-TQRDC • Supplier Teams	• Cycle Time Management • Broaden to Equipment & Service
	INTERNAL	• Decentralized Q & R Function • Crosby 14 Steps & Absolutes • 33 QITs Formed • All Employees Sign ZD Pledge	• JIT Manufacturing • Zero Accept Sampling Plans • Repeat 14 Steps	• SPC Introduction • Early Failure C/A Program • 14 Steps to 9 Elements • Customer Workshop	• Design Development Cycle Time Reduction • Make Market Cycle Time Reduction • Inventory Reduction • Baldrige Assessment & Planning	• 6 Sigma Strategy • Responsiveness Strategy • Benchmarking – Design Methodology – Mfg. Excellence – Quality & Service • QIP Audits • ISO 9001 Certification • TQE Award
	CUSTOMER	• PPM Program	• ZD Warranty Policy • STS Program • Customer Process Change Notification • Self Qual Program	• Listening Post-TQRDC • Advocate Program • Lot Traceability	• SPC Communications • Customer Certifications • Electronic Data Interchange	• Customer Relationship Management Plan • Customer Survey • Quality Strategy Communications
GOAL		• Conformance to Requirements • Zero Defects	• Zero Defects to Customers	• Conformance to Customer Requirements • Continuous Improvement	• Total Customer Satisfaction • Cycle Time Entitlement	• Industry Leader in Customer Satisfaction • 6 Sigma Quality • World Class Responsiveness
		1980 – 1983	**1984 – 1985**	**1986 – 1988**	**1989 – 1990**	**1991 – 1994**

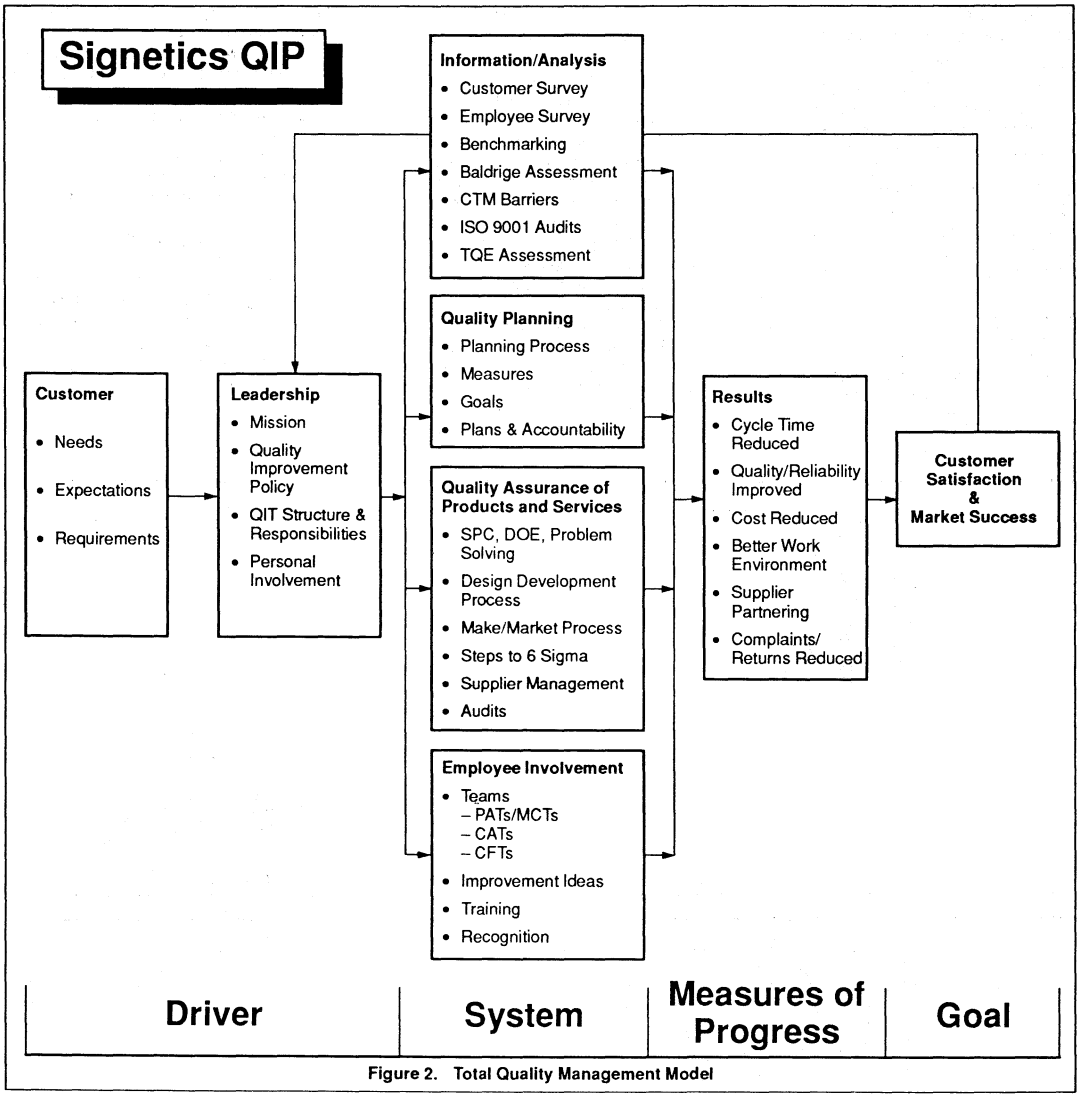


Figure 2. Total Quality Management Model

CYCLE TIME MANAGEMENT (CTM)

Cycle Time Management efforts are focused on Design-Development Process and Make-Market Process Responsiveness. Both are aimed at reducing the cycle time of tasks from current performance (Baseline) to entitlement (Using Existing Resources) then to improved entitlement and theoretical limit. Design-Development focuses on getting the right products and processes to production within the market window interval. Make-Market concentrates on getting product into the customers hands within Customer Lead Time Requirements. Cycle time management directly links to quality improvement in its requirement for task barrier identification at the root cause level and removal of those barriers (e.g. eliminating causes of rejects thereby eliminating rework or product sort). Also, the acceleration of results from reducing cycle time increases the frequency of events thereby increasing the cycles of learning required for quality improvement.

Quality and reliability

DESIGN FOR MANUFACTURABILITY (DFM) AND SIX SIGMA

A by-product of CTM application to the Design-Development Process (DDP) is the Signetics proprietary DDP manual introduced in January 1991 followed by Cross Functional Team (CFT) training. The DDP applies to all product, package and technology groups in Signetics. CFT's are used to drive the project from planning phase until all objectives of the new product contract are met. The requirements for SPC, DFM and meeting Six Sigma objectives are contained in the DDP manual. The CFTs are responsible for assuring that DFM occurs with an objective of Six Sigma. A Six Sigma design means that any desired characteristic of a part has a yield of 99.9997% or a defect rate of 3.4PPM (C_p of 2 or C_{pk} of 1.5)

QUALITY PERFORMANCE

Our Quality Improvement Process has influenced our entire production cycle - from the purchases of raw materials to the shipment of finished product. The involvement of all areas of the company has resulted in impressive quality improvements. A traditional quality gauge is final electrical and visual/mechanical product defect levels as measured upon first submittal results at outgoing Quality Assurance gates; Estimated Process Quality (EPQ). This is the PPM Level at our outgoing inspection for all accepted and rejected lots. (See Figures 3 and 4.) Current product shipments routinely record below 20PPM (Parts Per Million) electrical defect levels and 150PPM visual/mechanical defect levels. Since we utilize zero accept sampling on all finished product inspection, any lot with one or more rejects is rejected and 100 percent inspected.

The most meaningful measure of our quality is how we measure up to our customer's expectations. Many customers routinely send us incoming inspection data or ratings on our products and services. In 1991, Signetics also implemented a formal annual customer survey to solicit inputs on Signetics performance to the Dimension of Performance deemed relevant by the customer. Signetics is very appreciative of the recognition given by customers. Since 1986, Signetics has received over 70 formal commendation plaques from customers in recognition of Quality, Delivery and Service. Due to this type of performance, a number of our customers have eliminated expensive incoming inspection testing and have subscribed to the Ship-to-Stock Program. (See Figure 5.)

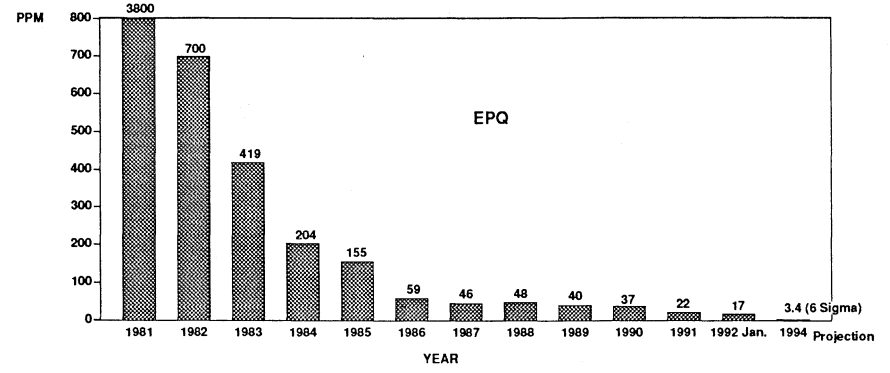


Figure 3. Electrical Product Quality Based on First Time Q.A. Submission Results

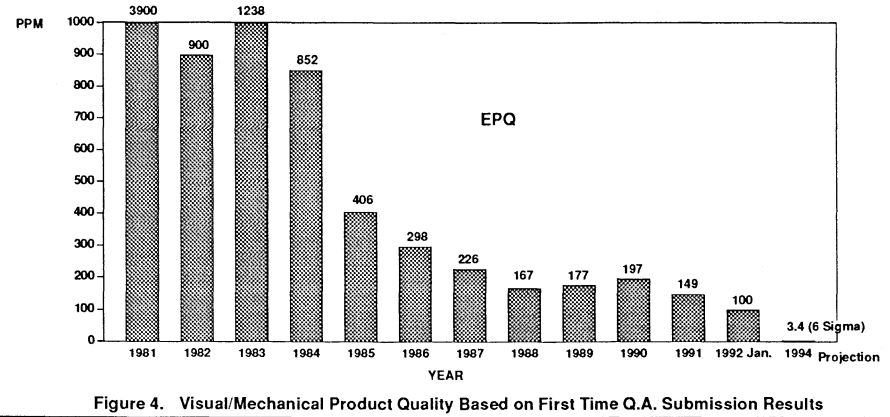
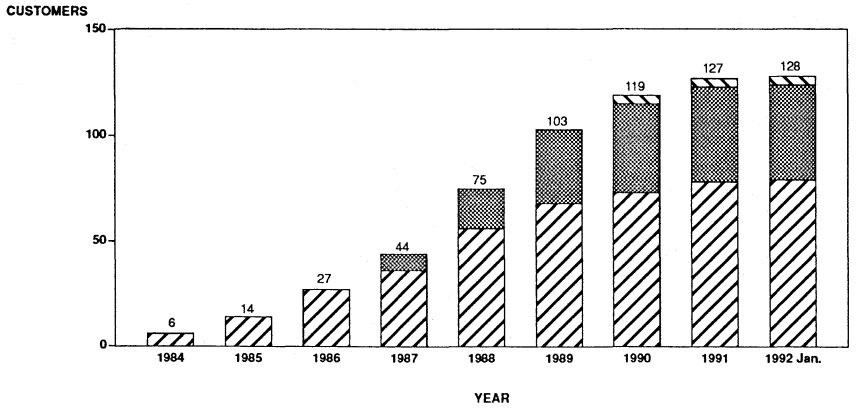


Figure 4. Visual/Mechanical Product Quality Based on First Time Q.A. Submission Results

Quality and reliability



	1984	1985	1986	1987	1988	1989	1990	1991	Jan. 1992
Asia Customers							4	4	4
Euro Customers				8	19	35	42	45	45
U.S. Customers	6	14	27	36	56	68	73	78	79

Figure 5. Signetics Ship-To-Stock Customer Growth

SHIP-TO-STOCK PROGRAM

Ship-to-Stock is a formal program developed at the request of our customers to help them reduce their costs by eliminating incoming test and inspection. Through close work with these customers in our quality improvement program, they became confident that our defect rates were so low that the redundancy of incoming inspections and testing was not only expensive, but unnecessary. They also saw that added component handling increased the potential of causing defects.

Ship-to-Stock is a joint program between Signetics and a customer which formally certifies specific parts to go directly into the customer's assembly line or inventory. This program was developed at the request of several major manufacturers after they had worked with us and had a chance to experience the data exchange and joint corrective action occurring as part of our quality improvement program.

Manufacturers using large volumes of ICs, those who are evaluating Just-in-Time delivery programs, or those who want to reduce or avoid high-cost incoming inspection are strongly encouraged to participate in this worthwhile program. Contact your local sales representative for further assistance and information on how to participate in this program.

RELIABILITY ASSURANCE PROGRAMS

Focus on Product Reliability

From 1981 to 1984, continuing improvements in process and material quality had a significant impact on product reliability.

Since 1984, the company has intensified its effort to markedly improve product reliability. Corporate Reliability Engineering, Group and Plant Reliability Units and Manufacturing Engineering work jointly on numerous improvement activities. These focused activities enhance the reliability of future products by providing improved methods for reliability assessment, increased understanding of failure physics, advanced analytical techniques, and aid in the development of material and processes.

Quality and reliability

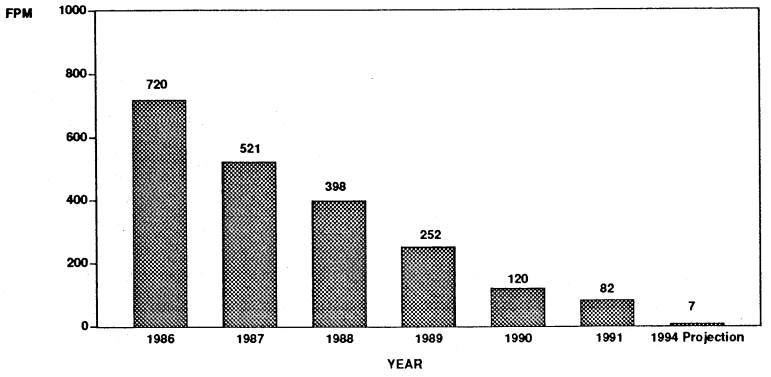


Figure 6. Signetics Early Failure Rate (EFR) Levels

EARLY FAILURE RATE (EFR) FOCUS

In 1986 Signetics intensified the focus on Early Life Reliability because of the significant impact EFR failures have on end system reliability performance. This program, which has now become a standard element in our reliability monitoring activities, provides quality engineering with statistically significant definition of low level process related defects. From these data, focused failure mechanism corrective actions can be developed. Average EFR levels on a broad cross section of processes, have been reduced from 720FPM to less than 100FPM since the corrective action effort was initiated in 1986 (reference Figure 6). Details of that activity are available upon request.

RELIABILITY MEASUREMENT PROGRAMS

Comprehensive product and process qualification programs have been developed to assure that our customers are receiving highly reliable products for their critical applications. Additionally, ongoing reliability monitoring programs, SURE III and Product Monitor, sample standard production on a regularly established basis (see Table 2).

Table 2. Reliability Assurance Programs

RELIABILITY FUNCTION	TYPICAL STRESS	FREQUENCY
New Process Qualification	High Temperature Operating Life Temperature-Humidity, Biased, Static High Temperature Storage Life Pressure Pot Temperature Cycle	Each new wafer fab process (and facility) Each new assembly process (and facility)
New Product Qualification	High Temperature Operating Life Temperature-Humidity, Biased, Static High Temperature Storage Life Pressure Pot Temperature Cycle Electrostatic Discharge Characterization	Each new product family
SURE III	High Temperature Operating Life Temperature-Humidity, Biased, Static Pressure Pot Temperature Cycle	Each fab process family, every four weeks
Product Monitor	Pressure Pot	Each plastic package type and technology family at each assembly plant, every week

Quality and reliability

DESCRIPTION OF STRESSES

High Temperature Operating Life

Static High Temperature Life (SHTL) stressing applies static DC bias to the device. This has specific merit in detecting ionic contamination problems which require continuous uninterrupted bias to drive contaminants to the silicon surface. The voltage bias must be maintained until the devices are cooled down to room temperature from the elevated life test temperature. Dynamic High Temperature Life (DHTL) stressing is not as effective in detecting such problems because the bias continuously changes, intermittently generating and healing the problem. For this reason, SHTL has typically been used as the accelerated life stress for Logic products. DHTL is useful for products such as memory and micro-processor/controller where a large portion of the area can only be accessed by dynamic means.

HTSL-High Temperature Storage Life

This stress exposes the parts to elevated temperatures (150°C-175°C) with no applied bias. For plastic packages, 175°C is the high end of its safe temperature region without accelerating untypical failure mechanisms. This test is intended to accelerate potential mechanical package-related failure mechanisms such as Gold-Aluminum bond integrity and other process instabilities.

THBS-Temperature-Humidity, Biased, Static

The accelerated temperature and humidity bias is performed at 85°C and 85% relative humidity (85°C/ 85% RH). In general, the worst case bias condition is the one which minimizes the device power dissipations and maximizes the applied voltages. Higher power dissipations tend to lower the humidity level at the chip surface and lessen the corrosion susceptibility.

TMCL-Temperature-Cycling, Air to Air

The device is cycled between the specified upper and lower temperature without power in an air or Nitrogen environment. Normal temperature extremes are -65°C and +150°C with a minimum 10 minute dwell and 5 minute transition per MIL-STD-883C, Method 1010.5, Condition C. This is a good test to measure the overall package to die mechanical compatibility, because the thermal expansion coefficients of the plastic are normally very much higher than those of the die and leadframe. However, for large die the stress may be too severe and induce failures that would not be expected in a real application.

PPOT-Pressure Pot

This stress exposes the devices to saturated steam at elevated temperature and pressure. The standard condition is 20 PSIG which occurs at a temperature of 127°C and 100% RH. The stress is used to test the moisture resistance of plastic encapsulated devices. The plastic encapsulant is not a moisture barrier and will saturate with moisture within 72 hours. Since the chip is not powered up the chip temperature and relative humidity will be the same as the autoclave once equilibrium is reached. Because the steam environment has an unlimited supply of moisture and ample temperature to catalyze thermally activated events, it is effective at detecting corrosion problems, contamination induced leakage problems, and general glassivation stability and integrity. It is also a good test for both package integrity (cracks in the package), and for die cracks (the moisture swells the plastic enough to stress the die; also the moisture causes leakage paths in the crack itself).

PRODUCT AND PROCESS QUALIFICATION PROGRAMS

Qualification activity is centered around new products and processes and changes in products and processes. The goal is to assure that the products can meet the qualification requirements prior to general release, and on an ongoing basis to demonstrate conformance to those requirements. The nature and extent of reliability stressing required depends on the type of change and the amount of applicable reliability data available.

A full qualification may include Early Failure Rate (EFR), Intrinsic Failure Rate (IFR), and Environmental Endurance Stressing. Such stress plans are reserved for introductions or changes that involve new or untested material or processes and, as such should be subjected to the maximum reliability interrogation. This normally entails a full range of biased and unbiased temperature and humidity stresses along with thermo-mechanical stresses.

For changes that are of limited scope, the full range of qualification stressing may not be warranted. In these instances, the nature and extent of the change is examined and only those stresses which provide a valuable measure of the change, or those which will detect potential weakness, are performed.

SELF-QUAL PROGRAM (SQP)

Self-Qual, initiated in 1984, is a joint program between Signetics and a customer that formally communicates the qualification activities for a new or changed product, process, or material. The Self Qual process provides our customer's engineering groups an opportunity to participate in the development of the qualification plan. During the qualification process, customers may audit the project, and can receive interim updates of qualification progress. Upon completion, formal detailed engineering reports are provided.

The major impact to the customer comes from the reduced workload on the component engineering and qualification groups. These engineering resources generally divide their time between routine qualification activity and problem resolution on critical components. By eliminating the need to perform qualification for one of the basic supplier changes the customer component engineer can spend more of his time resolving the critical product issues. In addition, the total amount of stress hardware needed to perform qualification life tests and other environmental evaluations can be reduced, saving the customer facility costs and reducing operating expense.

Self-Qual is a no-risk proposition for the customer. Each Self-Qual proposal provides a detailed description of what we are changing and why. It includes a detailed plan of what we intend to do to establish the reliability of the products affected. If the customer wishes to have product added to the plan or select some additional stresses, or prefers alternative stress conditions, Signetics will do everything possible to accommodate those requests. After that, if the customer is still uncomfortable with the recommended change, they are under no obligation to accept our data, and they may also perform their own qualification program. Customers who are interested in participating in this program should contact their local sales representative or the Corporate Reliability Engineering department directly.

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SURE III RELIABILITY MONITORING PROGRAM

In order to implement an improvement program, a standard measure of performance was needed. The results from the SURE III Reliability Monitoring Program are used as basic ongoing measures of product reliability performance. This program samples all generic families of products manufactured and utilizes standardized stress methods and test procedures. A measurement philosophy was adopted based on the premise of continual improvement toward our performance standard of zero defects. We also increased our standard Pressure Pot stress conditions from 15 PSIG/121°C to 20 PSIG/127°C. This reduced stress duration from 168 hours to 72 hours, and increased high volume sampling, which increased sensitivity to low defect levels. Our standard monitoring program, SURE III, includes the stress conditions as described in Table 3. The continuous improvement results are shown in Figure 7 Signetics Reliability Index as Failure Per Million (FPM). The FPM value includes all rejects from all accelerated stresses divided by total units submitted to all stresses. This is a relative number used to manage continuous reliability improvement. It should not be interpreted as an expected failure rate. Figure 8 shows the continuous improvement in the SURE III 1000 Hour High-Temperature (T_J > 150°C) Operating Life Test FPM (includes early and intrinsic failure rates) for all technologies combined. The 428 FPM for 1991 derates to 1 FIT at 45°C ambient temperature when assumptions of 0.7eV, 60% UCL and an 8°C junction rise above ambient are used. Admittedly the 1 FIT calculation for 1991 includes all technologies and unsubstantiated assumptions, but is a plausible number. Detailed FIT calculations by family do exist. Failure rate information is provided in the Signetics Product Reliability Summary Report available to all customers. In addition, the Signetics Reliability Handbook and the Signetics Process Technology and Manufacturing Facility Roadmap publications further define the rationale for methods used and the formation of process, product and package families.

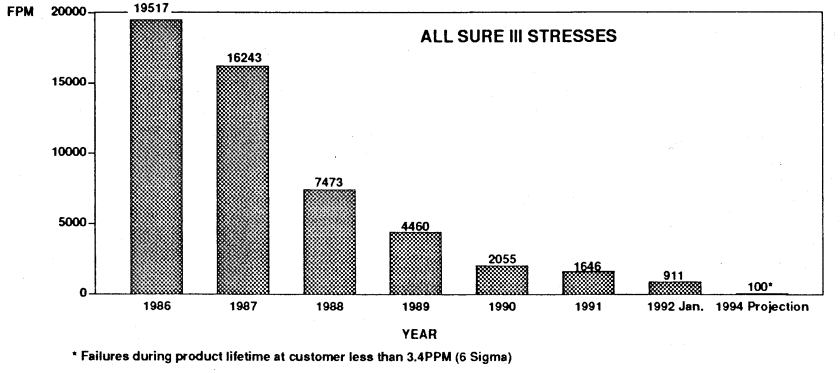


Figure 7. Signetics Reliability Index

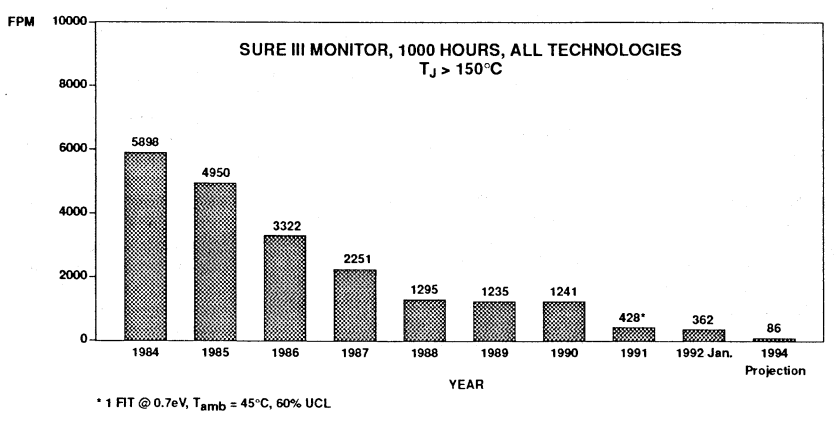


Figure 8. High-Temperature Operating Life Test FPM

Quality and reliability

Table 3. SURE III Reliability Monitoring Program

RELIABILITY FUNCTION	STRESS CONDITIONS	# UNITS
Static High Temperature Operating Life (SHTL)	$T_j \geq 150°C$, $T_{amb} = 125°C$ to 150°C, Biased condition = Static, V_{CC} = MAX, Duration = 1000 hours	135/150 Monthly
Temperature-Humidity, Biased, Static (THBS)	$T_{amb} = 85°C \pm 3°C$, Humidity = 85% RH ± 5%, Biased condition = Static, V_{CC} = MAX, Duration = 1000 hours	100 Monthly
Temperature Cycling (TMCL)	T_{amb} = -65°C (+0°C -10°C) to +150°C (+10°C -0°C), Air-to-Air, Dwell time = 10 minutes minimum each extreme, Biased condition = None, Duration = 1000 cycles for plastic package, 300 cycles for ceramic package	100 Monthly
Pressure Pot	$T_{amb} = 127°C \pm 2°C$, 20 PSIG ±0.5 PSIG (PPOT). 100% saturated steam, Biased condition = None, Duration = 72 hours	100 Weekly
		435/450 per Family

NOTE: V_{CC} = MAX is generally equal to V_{CC} = MAX as specified in data handbook

PRODUCT MONITOR

In addition to the SURE III program, each assembly plant performs Pressure Pot (20PSIG, 127°C, 72hours) reliability monitors on a weekly basis for each molded package type by pin count. The purpose of this program is to monitor the consistency of the assembly operations for such attributes as molding quality and die attach and wire bond integrity. This data is reported back to manufacturing operations and corporate and group reliability and quality assurance departments by electronic mail each week.

RELIABILITY EVALUATION

In addition to the product performance monitors encompassed in the SURE III program, Corporate and Group Reliability Engineering departments sustain a broad range of evaluation and qualification activities. Included in the engineering process are:

- Evaluation and qualification of new or changed materials, assembly/wafer-fab processes and equipment, product designs, facilities, and subcontractors.
- Devices or generic group failure rate studies.
- Advanced environmental stress development.
- Failure mechanism characterization and corrective action/prevention reporting.

The environmental stresses utilized in the engineering programs are similar to those utilized for the SURE III program; however, more highly accelerated conditions and extended durations typify these engineering projects. Additional stress systems such as biased pressure pot, power-temperature cycling, and cycle-biased temperature-humidity, are included in some evaluation programs.

STRESS FACILITY QUALITY

Quality improvement has reached all functional areas of the company, and the reliability stress laboratories are no exception. Corporate Reliability Laboratory (CRL) is one of the many areas where the benefits of the quality improvement process pays repeated dividends.

CRL utilizes stress which accelerate failure rates hundreds to thousands of times, requiring precision and control to make reliability data meaningful. Stress loading schedules are maintained with absolute regularity and chambers are never off-line beyond scheduled loading plans. Board currents are recorded prior to and at each interval on biased stresses, and monitoring of in-oven currents is conducted daily.

Thermal modeling of the Temperature Cycling systems has been accomplished and all loads are carefully weighed to ensure that thermal ramps are consistent.

Pressure Pot and Biased Pressure Pot systems utilize microprocessor controllers, and are accurate to within 0.1 degree centigrade. Saturation is guaranteed via automatic timing circuits, and a host of fail-safe controls ensure that test groups are never damaged.

Electrostatic discharge (ESD) handling precautions are standard procedures in the laboratories, and the occurrences of devices lost, zapped, or overstressed have become almost non-existent.

MANUFACTURING FACILITIES

Signetics, as part of a multinational corporation, utilize manufacturing facilities for wafer fabrication, package assembly, and test in three states and six overseas countries as shown in Table 4. Wafer fabrication is performed in fabs which report to the Product Groups. Assembly operations in Korea and Thailand report to Assembly Manufacturing Operations (AMO). Assembly subcontractors are scheduled and controlled through the AMO organization. Assembly subcontractors process all product to Signetics' specifications and materials. We have on-site quality assurance personnel at each subcontractor site to audit assembly processes and procedures.

TYPICAL IC MANUFACTURING FLOW

The manufacturing process for integrated circuits begins with wafer fabrication. The wafers are then electrically sorted, assembled, and tested prior to customer shipment. Quality assurance inspections are utilized throughout the manufacturing process, with manufacturing being responsible for the process/product quality.

Quality and reliability

Table 4. Product Manufacturing

FACILITIES	DESIGNATION	LOCATION	PROCESS OR PACKAGE FAMILIES
Wafer Fabrication	Fab 01	Sunnyvale, California, USA	Bipolar, Linear, Junction Isolated and Quality Assurance
	Fab 21	Orem, Utah, USA	Bipolar Gold Doped, Schottky, Oxide Isolated, ECL, PLD and Quality Assurance
	Fab 22	Albuquerque, New Mexico, USA	NMOS, CMOS, ACMOS, BiCMOS, EPROM and Quality Assurance
	Fab 23	Albuquerque, New Mexico, USA	CMOS EPROM, Flash EPROM, BiCMOS, and Quality Assurance
	MOS #2	Nijmegen, The Netherlands	HC(T) CMOS Logic and Quality Assurance
Assembly	Alphatec (R)	Bangkok, Thailand	Ceramic DIP and Quality Assurance
	Anam (L)	Seoul, Korea	Plastic DIP, SO, PLCC, Metal Can and Quality Assurance
	ASAT (C)	Hong Kong	Plastic QFP, SO, and Quality Assurance
	HANA (M)	Bangkok, Thailand	Plastic DIP and Quality Assurance
	Hyundai (W)	Ichon, Kyungki, Korea	Plastic DIP, SO, PLCC, Ceramic DIP and Quality Assurance
	MEC (T)	Osaka, Japan	Plastic SO EIAJ, QFP and Quality Assurance
	Orem (P)	Orem, Utah, USA	Ceramic DIP, Flat Pack, QFP, PGA and Quality Assurance
	Pebei (B)	Kaosiung, Taiwan	Plastic DIP, SO, SSOP, PLCC, and Quality Assurance
	SigKor (K)	Seoul, Korea	Plastic DIP, SO, PLCC, and Quality Assurance
	Sig Thai (V)	Bangkok, Thailand	Plastic DIP, SO, and Quality Assurance
	Rohm (G)	Kyoto, Japan	Plastic QFP and Quality Assurance
Test	TA05	Sunnyvale, California, USA	Wafer Sort, Final Test and Quality Assurance
	SigKor	Seoul, Korea	Final Test and Quality Assurance
	SigThai	Bangkok, Thailand	Final Test and Quality Assurance
	Albuquerque	Albuquerque, New Mexico, USA	Wafer Test and Quality Assurance
	Orem	Orem, Utah, USA	Wafer Test, Military Final Test and Quality Assurance

Table 5. Package Construction

ITEMS	PLASTIC DIP	SO AND PLCC	CERAMIC DIP(CERDIP)	CERAMIC FLAT PACK
Lead Frame	Copper, 194 Alloy	Copper, 194 or PMC102	Alloy-42	Alloy-42
Lead Finish	Tin/Lead Solder Dip (60/40)	Tin/Lead Solder Dip (60/40) or Solder Plate (80/20)	Tin/Lead Solder Dip (60/40)	Tin/Lead Solder Dip (60/40)
Bond Area Finish	Silver Spot	Silver Spot	Silver Spot	Silver Spot
Die Attach	Silver Filled Polymide or Thermoplastic	Silver Filled Polymide or Thermoplastic	Silver Filled Glass	Silver Filled Glass
Bond Wire	Gold, 1.0-1.3 mils in Diameter	Gold, 1.0-1.3 mils in Diameter	Aluminum, 1.0-1.3 mils in Diameter	Aluminum, 1.0-1.3 mils in Diameter
Wire Bonding Die Lead Frame	Thermosonic Ball Stitch	Thermosonic Ball Stitch	Ultrasonic Stitch Stitch	Ultrasonic Stitch Stitch
Package Material	Novolac Epoxy	Novolac Epoxy	Ceramic	Ceramic

SPECIAL PROCESSING

SUPR II LEVEL B –

For our customers who require an infant mortality rate level less than that normally provided for our standard products (typically less than 1000PPM), we offer our Signetics Upgraded Product Reliability (SUPR) program.

Devices are burned-in per Signetics specification 850-227 schematics for a minimum of 21 hours at junction temperature between 155°C to 175°C. For a 1.0eV activation energy, 21 hours at 155°C is equivalent to 168 hours at 125°C.

Following burn-in, all devices are cooled down under bias and tested within 96 hours. All devices are tested before and after burn-in, yield calculated and compared to Percent Defective Allowed (PDA). If a lot fails PDA, it is investigated and good units submitted to a second burn-in. All "SUPR II B" devices carry a "B" marking.

The SUPR program was introduced in 1972 to improve quality and reliability and was expanded in 1975 to SUPR II A which included the burn-in option, SUPR II B. With the implementation of the Signetics Quality Improvement Process in 1980, standard product quality levels and guarantees caught up and passed SUPR II. All processing,

Quality and reliability

except for burn-in, is now standard. The Signetics standard warranty is Zero Defects.

"Evaluation of Early Failure Levels and The Effectiveness of Burn-In" is available upon request through your local sales office. This brochure is an aid for those users and purchasers of integrated circuits who need to make a decision regarding burn-in.

PUBLICATIONS

Signetics routinely publishes documents supporting the Quality and Reliability Improvement Process. The following significant documents are currently available.

IC Quality Series

Quality and Reliability Policy Manual (850-8000)

This manual is the starting point for understanding the policies of Signetics pursuant to constantly improving the high standards of quality and reliability in the manufacture of monolithic integrated circuits. Responsibilities and authority of organizations are defined along with governing specifications and operator instruction documents.

Signetics QIP Total Quality Management

This booklet describes the TQM model, patterned after the U.S.A. Malcom Baldrige National Quality Award criteria and how the model is applied to the Signetics Quality Improvement Process.

Supplier Partnership Guide

This booklet defines Signetics philosophy, policy and requirements for establishing strategic partnerships with raw material suppliers.

Product Symbol Formats

This publication provides a guide for determining standard product symbol format and content for decoding inventory and product in field usage since 1980. Since date code 8717, Signetics has symbolized the assembly start computer Lot ID on commercial products providing full traceability back to start of wafer fabrication.

Quality Attributes EDI System

This manual defines system requirements for Electronic Data Interchange (EDI) of Quality Attributes (pass/fail) Data.

Monthly Product Outgoing Quality Summary Reports

Estimated Process Quality (EPQ) in PPM for electrical, visual/ mechanical and hermeticity by part number or by family.

Statistical Process Control

This booklet introduces the Signetics SPC system including terminologies, philosophy, organization, training and implementation strategy and status.

Ship-To-Stock Program

This booklet defines the "joint program" requirements of Signetics and the customer to formally certify specific products to go directly into the assembly line or inventory with reduced or no incoming inspection thereby reducing cost of ownership.

Customer Return Immediate Service Program (CRISP)

This booklet defines the joint responsibilities of Signetics and the customer to assure that correlation samples are investigated and results reported per the Signetics 1-4-5 cycle time commitments.

IC Reliability Series

Signetics Reliability Handbook

This handbook is a detailed guide to Signetics Reliability Qualification and Monitoring activities. It includes reference sections that deal with the application and statistics of integrated circuit reliability issues.

Product Reliability Summary

Yearly, SURE III monitoring data is summarized and published for all product families in a Product Reliability Summary. Summaries like this one provide a detailed overview of product family performance and estimates the reliability of those products in use conditions.

Quarterly Reliability Update

Detailed results, by part number, package type, date code, assembly location, and by stress and test interval are routinely published in the Signetics Quarterly Reliability Update. The "Update" is available at the end of each quarter, and contains the results of reliability monitors which completed during the previous quarter, plus approximately 3 years of history for each product family.

SMD Reliability (The Reliability and Durability of Surface Mount Packages)

In support of Signetics' leadership in Surface Mount Device (SMD) technology, we have published in-depth studies and evaluations on the reliability and durability of SMD packages. The Surface Mount Reliability report covers evaluation of products after exposure to the unique environments created by various SMD soldering and cleaning processes.

Process Technology and Manufacturing Facility Roadmap

This document defines the various process technologies in production in Signetics manufacturing facilities, and defines in detail, the fab and assembly processes and locations qualified to produce all released products.

Thermal Characteristics of Integrated Circuit Packages

This is a comprehensive collection of thermal characterization data for all packages manufactured by Signetics. Thermal resistance data to *Case*, and to *Ambient* are provided. Details on airflow effects and die size are included.

SSQP – Signetics Self-Qual Program-Reports

In addition to the regular publications of reliability monitor results, a special program for the publication of qualification proposals and final engineering reports has been in place since January of 1984. Self-Qual Reports are available on all major process changes and introductions, thereby reducing customer cost of ownership.

Evaluation of Early Failure Levels and the Effectiveness of Burn-In

This report provides results of the Signetics Early Failure Rate (EFR) program implemented in 1986 to identify and eliminate root causes of infant mortality and to aid users of IC components faced with a decision regarding Burn-In of purchased integrated circuits.

DATA AVAILABILITY

The previously referenced documents are available to all our customers. Many are available in your local sales office, or from:

Corporate Quality System Group
Mail Stop #35
811 East Arques Avenue
P. O. Box 3409
Sunnyvale, CA 94088-3409, USA

where you can be placed on a standard mailing list for all documentation which meet your requirement(s).

Quality and reliability

PLD PRODUCT QUALITY AND RELIABILITY

Bipolar Programmable Products

Programmable Logic Devices (PLDs) have also undergone the "Signetics Quality Journey" described earlier. More monitoring in addition to those previously described is done on bipolar PLDs because they cannot be fully tested by Signetics. These products are not complete until the selected fusible elements (metallic fuse links of NiCr or TiW, or vertical diodes) are programmed by our customers.

Our goal is 100% programming yields. To meed this goal, we begin with correct product and process design to ensure sufficient current is delivered to the selected fuses without programming any de-selected fuses. Confirmation of proper design is done through the performance of fusibility testing and post-fuse functional testing hot (PFTH) during the qualification of new products and processes. PFTH includes functional, DC and AC testing.

Monitoring of fusibility continues on all PLDs in production with electrical testing of fuse resistance on Process Control Monitor die present on the same wafers as the product die. Product is also screened for fusibility at wafer electrical probing (Esort) where a test row and test column are programmed on each die. Die that cannot successfully program the test row and column are rejected. Samples of selected representative products continue to routinely undergo fusibility and PFTH monitors to ensure maintenance of high programming yields.

On occasion, our internal monitors or customer feedback may indicate certain products do not meet our customers' expectations in regard to programming. In that event, management commits the necessary resources to identify and implement corrective actions. This is usually accomplished in a Cross Functional Team as it may not be clear is improved design, process, testing, or some combination, is required. The success of such team efforts is exemplified in the release of new revisions of the PLUS153/173, PLUS16XX, and 10H20EV8/10020EV8 products. These products were converted to the new RD2 process that was developed to improve fusibility. Some of these products underwent design improvements as well.

CMOS Programmable Products

Our goal for CMOS EPLD programming yields is also 100%. In addition, data retention is to be better than 10 years at 45°C. Our efforts towards these goals also begin with proper product and process design and continue with SPC in manufacturing.

In contrast to bipolar PLDs, EPLDs are completely tested by programming all cells at Esort. Defective die that cannot be fully programmed are rejected. Product is also screened for data retention (charge loss) by voltage and thermally accelerated testing. The former is accomplished by an elevated voltage drain stress test at Esort. The latter is done by means of a 250°C bake between programming at Esort1 and verification at Esort2.

As for all products, ongoing verification of product quality and reliability is accomplished with PA sampling after final electrical test, SURE III reliability testing, and EFR monitoring.

Section 3
PAL Device Data Sheets

INDEX

Programmable high-speed decoder logic (16 × 16 × 8)

PHD16N8-5

DESCRIPTION

The PHD16N8-5 is an ultra fast Programmable High-speed Decoder featuring a 5ns maximum propagation delay. The architecture has been optimized using Philips Semiconductors–Signetics state-of-the-art bipolar oxide isolation process coupled with titanium-tungsten fuses to achieve superior speed in any design.

The PHD16N8-5 is a single level logic element comprised of 10 fixed inputs, 8 AND gates, and 8 outputs of which 6 are bidirectional. This gives the device the ability to have as many as 16 inputs. Individual 3-State control of all outputs is also provided.

The device is field-programmable, enabling the user to quickly generate custom patterns using standard programming equipment. Proprietary designs can be protected by programming the security fuse.

The SLICE software package from Philips Semiconductors–Signetics supports easy design entry for the PHD16N8-5 as well as other PLD devices.

Order codes are listed below.

FEATURES

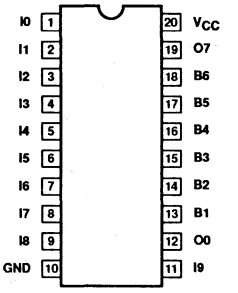
- Ideal for high speed system decoding
- Super high speed at 5ns t_{PD}
- 10 dedicated inputs
- 8 outputs
  - 6 bidirectional I/O
  - 2 dedicated outputs
- Security fuse to prevent duplication of proprietary designs.
- Individual 3-State control of all outputs
- Field-programmable on industry standard programmers
- Available in 20-pin Plastic Dual In-Line and 20-Pin PLCC

APPLICATIONS

- High speed memory decoders
- High speed code detectors
- Random logic
- Peripheral selectors
- Machine state decoders
- Footprint compatible to 16L8
- Fuse/Footprint compatible to TIBPAD

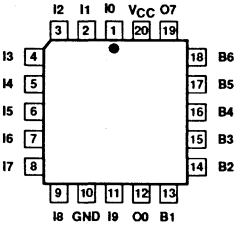
PIN CONFIGURATIONS

N Package



N = Plastic Dual In-Line Package (300mil-wide)

A Package



A = Plastic Leaded Chip Carrier

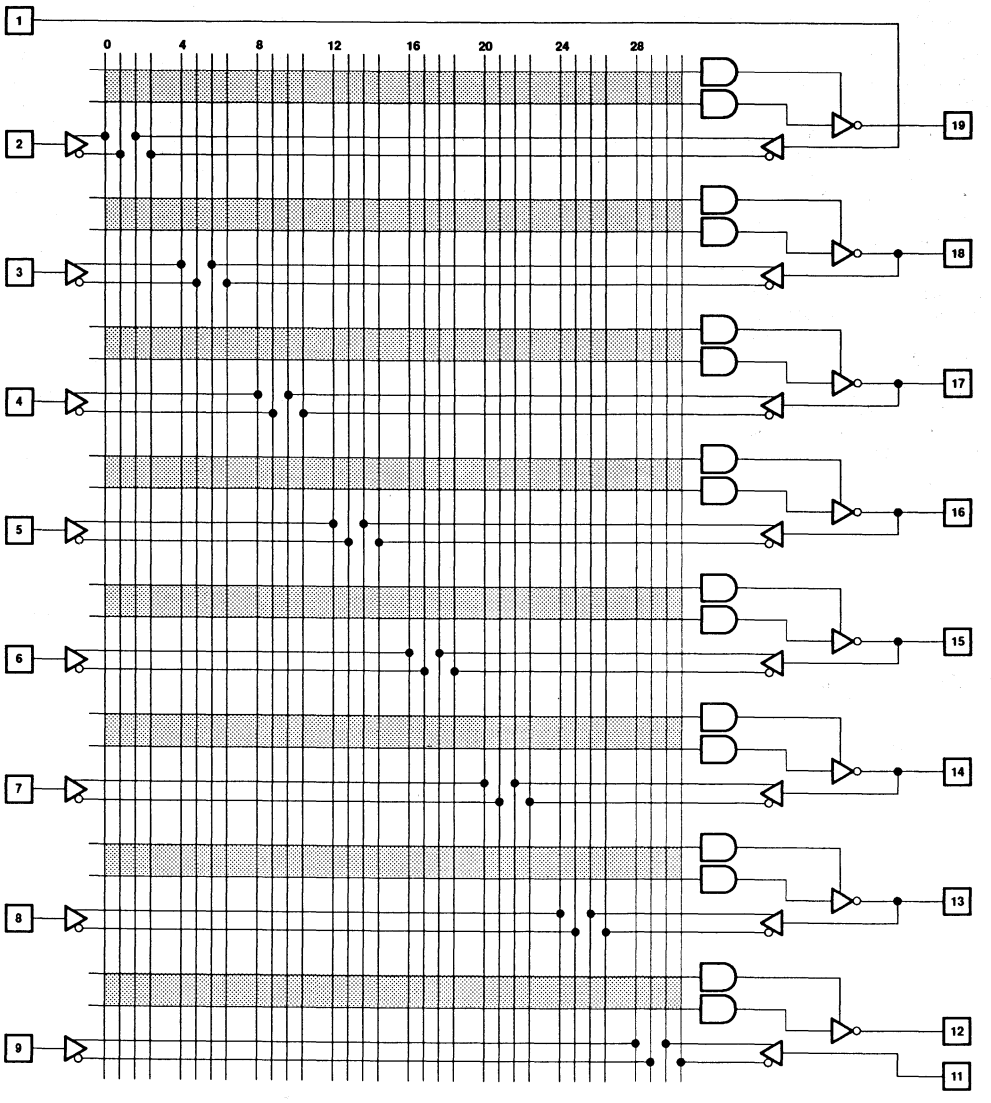
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
20-Pin Plastic Dual In Line Package; (300mil-wide)	PHD16N8-5N
20-Pin Plastic Leaded Chip Carrier; (350mil square)	PHD16N8-5A

Programmable high-speed decoder logic (16 × 16 × 8)

PHD16N8-5

LOGIC DIAGRAM



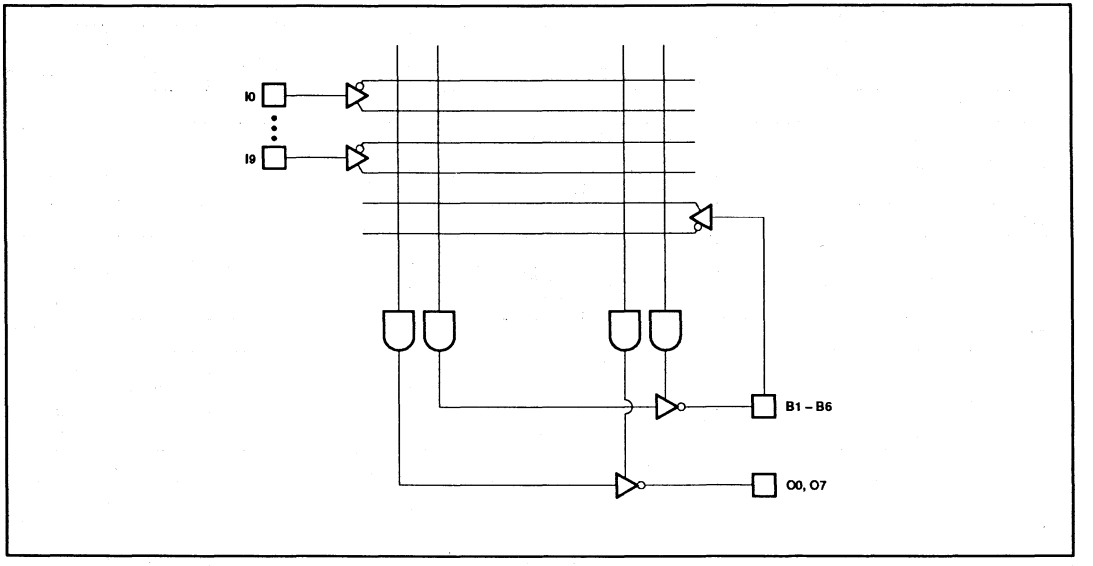
NOTES:

1. All unprogrammed or virgin "AND" gate locations are pulled to logic "0"
2. ▒ Programmable connections

Programmable high-speed decoder logic (16 × 16 × 8)

PHD16N8-5

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS Min	RATINGS Max	UNIT
V_{CC}	Supply voltage	–0.5	+7	V_{DC}
V_{IN}	Input voltage	–0.5	+5.5	V_{DC}
V_{OUT}	Output voltage		+5.5	V_{DC}
I_{IN}	Input currents	–30	+30	mA
I_{OUT}	Output currents		+100	mA
T_{amb}	Operating temperature range	0	+75	°C
T_{stg}	Storage temperature range	–65	+150	°C

NOTES:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

OPERATING RANGES

SYMBOL	PARAMETER	RATINGS Min	RATINGS Max	UNIT
V_{CC}	Supply voltage	+4.75	+5.25	V_{DC}
T_{amb}	Operating free-air temperature	0	+75	°C

DC ELECTRICAL CHARACTERISTICS

$0°C \leq T_{amb} \leq +75°C$, $4.75 \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[1]	MAX	
Input voltage[2]						
V_{IL}	Low	V_{CC} = MIN			0.8	V
V_{IH}	High	V_{CC} = MAX	2.0			V
V_{IC}	Clamp	V_{CC} = MIN, I_{IN} = –18mA		–0.8	–1.5	V
Output voltage						
		V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}				
V_{OL}	Low	I_{OL} = +24mA			0.5	V
V_{OH}	High	I_{OH} = –3.2mA	2.4			V
Input current						
		V_{CC} = MAX				
I_{IL}	Low	V_{IN} = +0.40V		–20	–250	μA
I_{IH}	High	V_{IN} = +2.7V			25	μA
I_I	High	V_{IN} = V_{CC} = V_{CC} MAX			100	μA
Output current						
		V_{CC} = MAX				
I_{OZH}	Output leakage[3]	V_{OUT} = +2.7V			100	μA
I_{OZL}	Output leakage[3]	V_{OUT} = +0.40V			–100	μA
I_{OS}	Short circuit[4]	V_{OUT} = 0V	–30		–90	mA
I_{CC}	V_{CC} supply current	V_{CC} = MAX		115	180	mA
Capacitance[5]						
		V_{CC} = +5V				
C_{IN}	Input	V_{IN} = 2.0V @ f = 1MHz		8		pF
C_{OUT}	I/O (B)	V_{OUT} = 2.0V @ f = 1MHz		8		pF

NOTES:
1. Typical limits are at V_{CC} = 5.0V and T_{amb} = +25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. Leakage current for bidirectional pins is the worst case of I_{IL} and I_{OZL} or I_{IH} and I_{OZH}.
4. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second.
5. These parameters are not 100% tested, but are periodically sampled.

Programmable high-speed decoder logic (16 × 16 × 8)

PHD16N8-5

AC ELECTRICAL CHARACTERISTICS

$0°C \le T_{amb} \le +75°C$, $4.75 \le V_{CC} \le 5.25V$, $R_1 = 200\Omega$, $R_2 = 390\Omega$

SYMBOL	PARAMETER	FROM	TO	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNIT
t_{PD}[1]	Propagation delay	(I, B) ±	Output ±	C_L = 50pF		5	ns
t_{OE}[2]	Output Enable	(I, B) ±	Output enable	C_L = 50pF		10	ns
t_{OD}[2]	Output Disable	(I, B) ±	Input disable	C_L = 5pF		10	ns

NOTES:

1. t_{PD} is tested with switch S_1 closed and C_L = 50pF.
2. For 3-State output; output enable times are tested with C_L = 50pF to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with C_L = 5pF. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} - 0.5V)$ with S_1 open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with S_1 closed.

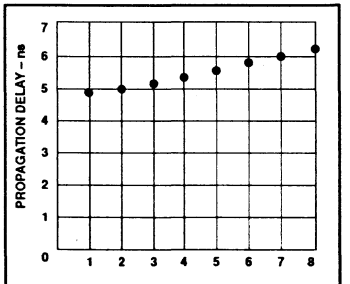
VIRGIN STATE

A factory shipped virgin device contains all fusible links open, such that:

1. All outputs are disabled.
2. All p-terms are disabled in the AND array.

TIMING DEFINITIONS

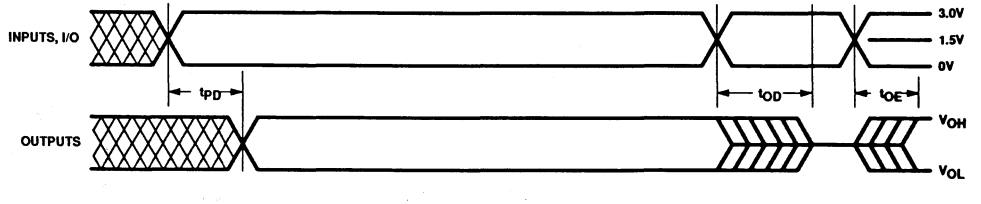
SYMBOL	PARAMETER
t_{PD}	Input to output propagation delay.
t_{OD}	Input to Output Disable (3-State) delay (Output Disable).
t_{OE}	Input to Output Enable delay (Output Enable).



TEST CONDITIONS: T_{amb} = 75°C; V_{CC} = 4.75V; C_L = 50pF; R_1 = 200Ω; R_2 = 390Ω

Worst-Case Propagation Delay vs. Number of Outputs Switching

TIMING DIAGRAM

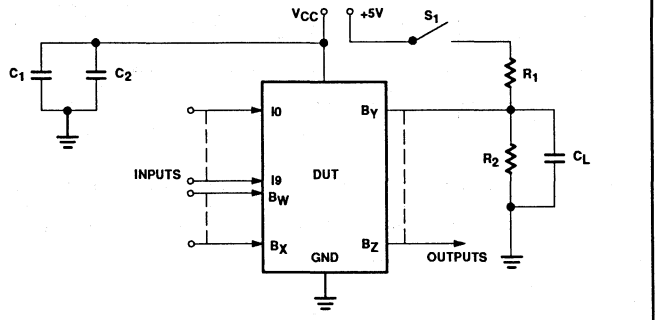


WAVEFORM	INPUTS	OUTPUTS	WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY		DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
				DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

Programmable high-speed decoder logic (16 × 16 × 8)

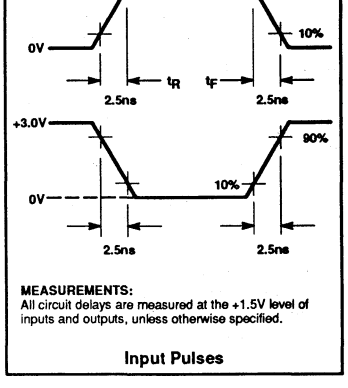
PHD16N8-5

AC TEST LOAD CIRCUIT



NOTE:
C_1 and C_2 are to bypass V_{CC} to GND.

VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

LOGIC PROGRAMMING

The PHD16N8-5 is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Signetics' SLICE and SNAP design software packages. ABEL™ CUPL™ and PALASM® 90 design software packages also support the PHD16N8–5 architecture.

All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

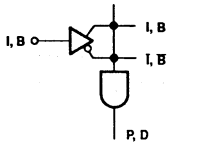
PHD16N8-5 logic designs can also be generated using the program table entry format, which is detailed on the following page. This program table entry format is supported by SLICE only. The SLICE design package is available, free of charge, to qualified users.

To implement the desired logic functions, each logic variable (I, B, P and D) from the logic equations is assigned a symbol. TRUE (High), COMPLEMENT (Low), DON'T CARE and INACTIVE symbols are defined below.

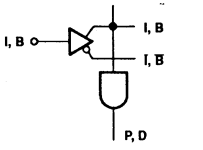
PROGRAMMING/SOFTWARE SUPPORT

Refer to Section 8 *(Development Software)* and Section 9 *(Third-Party Programmer/ Software Support)* of this data handbook for additional information.

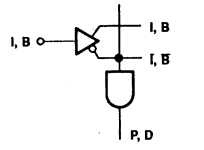
"AND" ARRAY – (I, B)



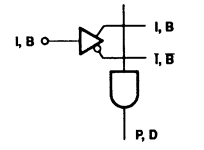
STATE	CODE
INACTIVE[1]	O



STATE	CODE
TRUE	H



STATE	CODE
COMPLEMENT	L



STATE	CODE
DON'T CARE	–

NOTE:
1. This is the initial state.

ABEL is a trademark of Data I/O Corp.
CUPL is a trademark of Logical Devices, Inc.
PALASM is a registered trademark of AMD Corp.

Programmable high-speed decoder logic (16 × 16 × 8)

PHD16N8-5

PROGRAM TABLE

OR (FIXED): D = DIRECTION, A = ACTIVE OUTPUT, NOT USED

AND: I, B(I): 0 = INACTIVE; H = I, B; L = $\overline{I, B}$; — = DON'T CARE

CUSTOMER NAME _____

PURCHASE ORDER # _____

SIGNETICS DEVICE # _____ CF(XXXX)

CUSTOMER SYMBOLIZED PART # _____

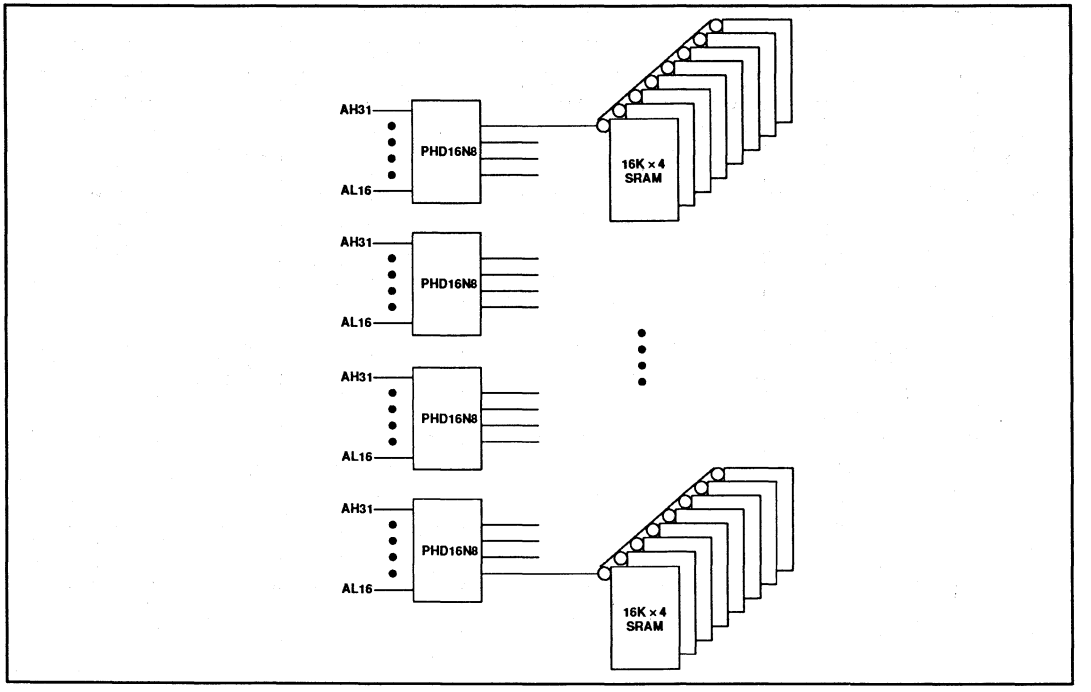
TOTAL NUMBER OF PARTS _____

PROGRAM TABLE # _____ REV ____ DATE _____

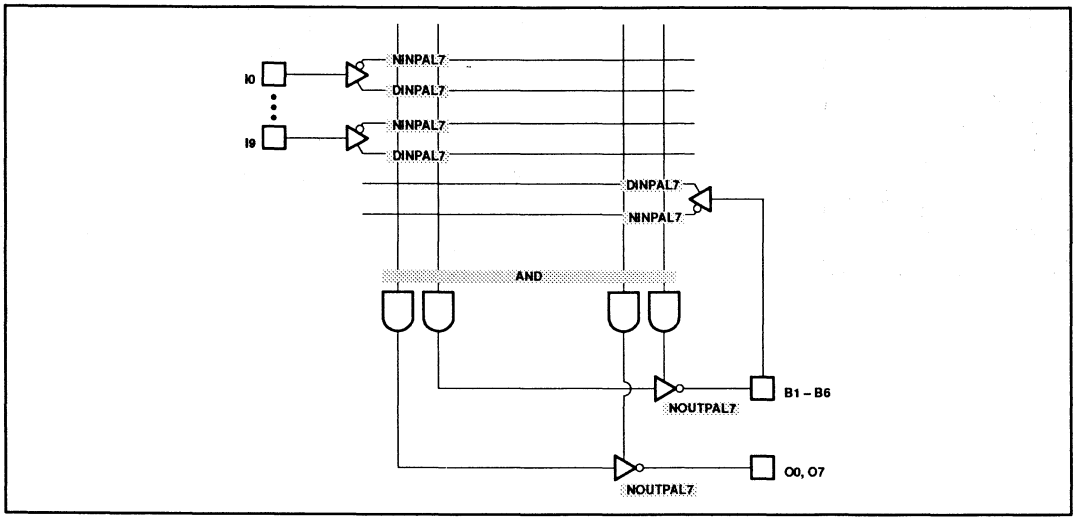
TERM	AND: INPUT (I) 9	8	7	6	5	4	3	2	1	0	AND: INPUTS (B) 6	5	4	3	2	1	OR (FIXED): OUTPUTS (B, O) 7	6	5	4	3	2	1	0
0																	D							
1																	A							
2																		D						
3																		A						
4																			D					
5																			A					
6																				D				
7																				A				
8																					D			
9																					A			
10																						D		
11																						A		
12																							D	
13																							A	
14																								D
15																								A
PIN	11	9	8	7	6	5	4	3	2	1	18	17	16	15	14	13	19	18	17	16	15	14	13	12
VARIABLE NAME																								

NOTES:
1. The PHD16N8-5 is shipped with all links intact.
2. Unused I and B bits in the AND array exist as INACTIVE in the virgin state.
3. All p-terms are inactive until programmed otherwise.
4. Data cannot be entered into the OR array field due to the fixed nature of the device architecture.

DECODING 1/2 MEG STATIC MEMORY



SNAP RESOURCE SUMMARY DESIGNATIONS



Zero standby power CMOS versatile PAL devices

PLC18V8Z35 / PLC18V8ZI

DESCRIPTION

The PLC18V8Z35 and PLC18V8ZI are universal PAL® devices featuring high performance and virtually zero-standby power for power sensitive applications. They are reliable, user-configurable substitutes for discrete TTL/CMOS logic. While compatible with TTL and HCT logic, the PLC18V8ZI can also replace HC logic over the V_{CC} range of 4.5 to 5.5V.

The PLC18V8Z is a two-level logic element comprised of 10 inputs, 74 AND gates (product terms) and 8 output Macro cells.

Each output features an "Output Macro Cell" which can be individually configured as a dedicated input, a combinatorial output, or a registered output with internal feedback. As a result, the PLC18V8Z is capable of emulating all common 20-pin PAL devices to reduce documentation, inventory, and manufacturing costs.

A power-up reset function and a Register Preload function have been incorporated in the PLC18V8Z architecture to facilitate state machine design and testing.

With a standby current of less than 100µA and active power consumption of 1.5mA/MHz, the PLC18V8Z is ideally suited for power sensitive applications in battery operated/backed portable instruments and computers.

The PLC18V8Z is also processed to industrial requirements for operation over an extended temperature range of -40°C to +85°C and supply voltage of 4.5V to 5.5V.

Ordering information can be found below.

FEATURES

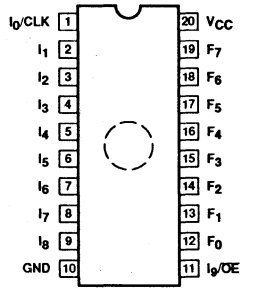
- 20-pin Universal Programmable Array Logic
- Virtually Zero-Standby-power
- Functional replacement for Series 20 PAL devices
  - I_{OL} = 24mA
- High-performance CMOS EPROM cell technology
  - Erasable
  - Reconfigurable
  - 100% testable
- 35ns Max propagation delay (comm)
- 40ns Max propagation delay (Industrial)
- Up to 18 inputs and 8 input/output macro cells
- Programmable output polarity
- Power-up reset on all registers
- Register Preload capability
- Synchronous Preset/Asynchronous Reset
- Security fuse to prevent duplication of proprietary designs
- Design support provided using SLICE software development package and other CAD tools for PLDs
- Available in 300mil-wide DIP with quartz window, plastic DIP (OTP) or PLCC (OTP)

APPLICATIONS

- Battery powered instruments
- Laptop and pocket computers
- Industrial control
- Medical Instruments
- Portable communications equipment

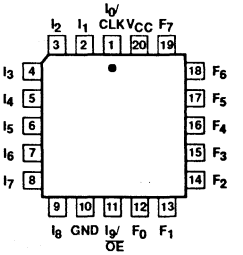
PIN CONFIGURATIONS

N and FA Packages



N = Plastic DIP (300mil-wide)
FA = Ceramic DIP with Quartz Window (300mil-wide)

A Package



A = Plastic Leaded Chip Carrier

PIN LABEL DESCRIPTIONS

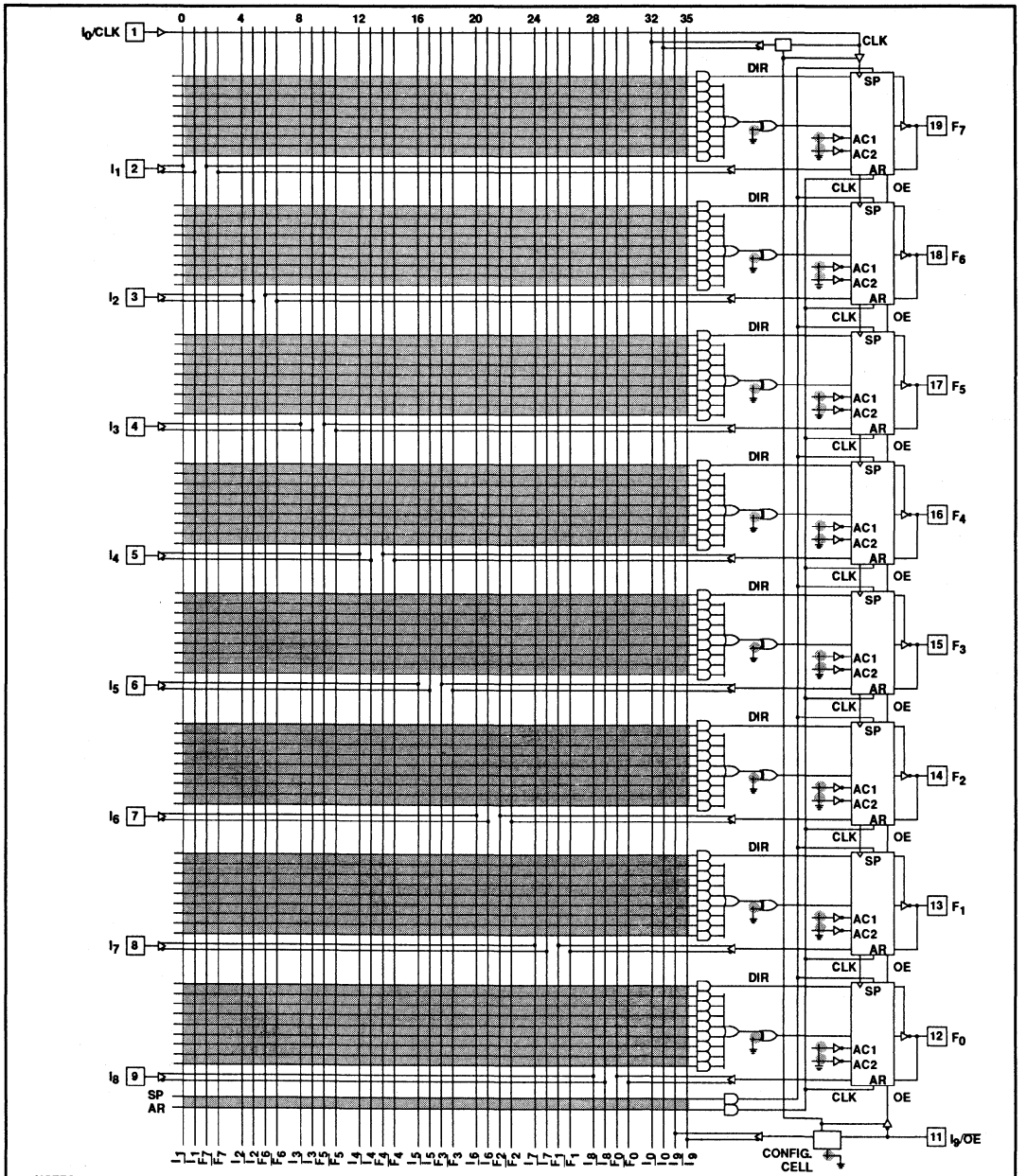
I	Dedicated input
B	Bidirectional input/output
O	Dedicated output
D	Registered output (D-type flip-flop)
F	Macrocell Input/Output
CLK	Clock input
$\overline{OE}$	Output Enable
V_{CC}	Supply voltage
GND	Ground

ORDERING INFORMATION

DESCRIPTION	OPERATING CONDITIONS	ORDER CODE
20-Pin Plastic Dual In-Line Package 300mil-wide (t_{PD} = 35ns)	Commercial Temperature Range ± 5% Power Supplies	PLC18V8Z35N
20-Pin Ceramic Dual In-Line Package 300mil-wide with quartz window (t_{PD} = 35ns)		PLC18V8Z35FA
20-Pin Plastic Leaded Chip Carrier 350mil square (t_{PD} = 35ns)		PLC18V8Z35A
20-Pin Plastic Dual In-Line Package 300mil-wide (t_{PD} = 40ns)	Industrial Temperature Range ± 10% Power Supplies	PLC18V8ZIN
20-Pin Ceramic Dual In-Line Package 300mil-wide with quartz window (t_{PD} = 40ns)		PLC18V8ZIFA
20-Pin Plastic Leaded Chip Carrier 350mil square (t_{PD} = 40ns)		PLC18V8ZIA

®PAL is a registered trademark of Advanced Micro Devices, Inc.

LOGIC DIAGRAM



NOTES:
In the unprogrammed or virgin state:

All cells are in a conductive state.
All AND gate locations are pulled to a logic "0" (Low).
Output polarity is inverting.

Pins 1 and 11 are configured as Inputs 0 and 9, respectively, via the configuration cell. The clock and OE functions are disabled.
All output macro cells (OMC) are configured as bidirectional I/O, with the outputs disabled via the direction term.
Denotes a programmable cell location.

Zero standby power CMOS versatile PAL devices

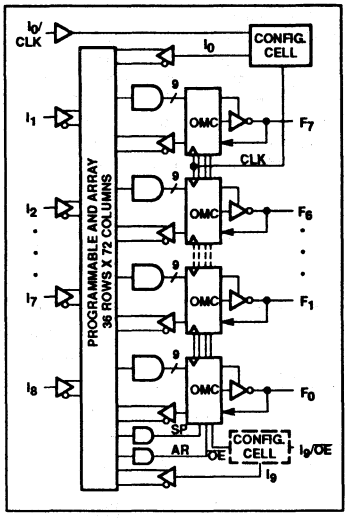
PLC18V8Z35 / PLC18V8ZI

PAL DEVICE TO PLC18V8Z OUTPUT PIN CONFIGURATION CROSS REFERENCE

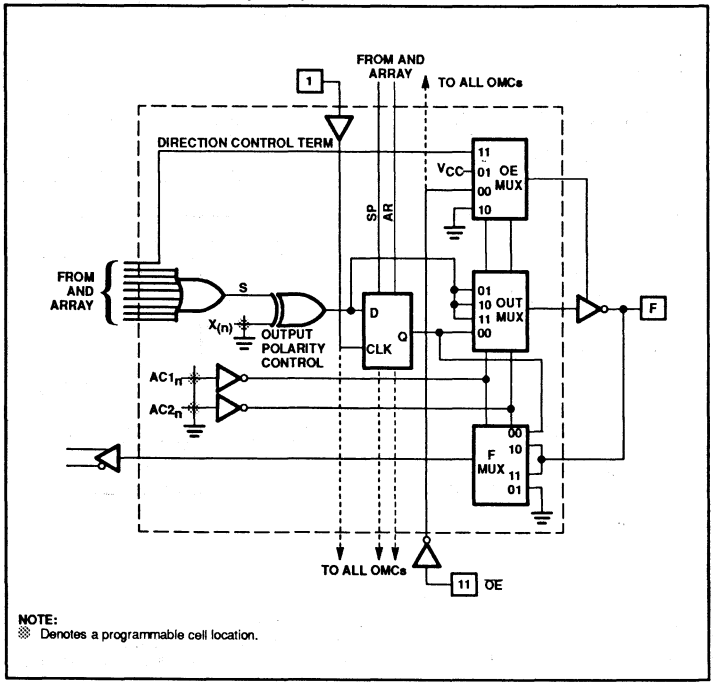
PIN NO.	PLC 18V8Z	16L8 16H8 16P8 16P8	16R4 16RP4	16R6 16RP6	16R8 16RP8	16L2 16H2 16P2	14L4 14H4 14P4	12L6 12H6 12P6	10L8 10H8 10P8
1	I_0/CLK	I	CLK	CLK	CLK	I	I	I	I
19	F7	B	B	B	D	I	I	I	O
18	F6	B	B	D	D	I	I	O	O
17	F5	B	D	D	D	I	O	O	O
16	F4	B	D	D	D	O	O	O	O
15	F3	B	D	D	D	O	O	O	O
14	F2	B	D	D	D	I	O	O	O
13	F1	B	B	D	D	I	I	O	O
12	F0	B	B	B	D	I	I	I	O
11	I_9/$\overline{OE}$	I	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	I	I	I	I

The Signetics state-of-the-art Floating-Gate CMOS EPROM process yields bipolar equivalent performance at less than one-quarter the power consumption. The erasable nature of the EPROM process enables Signetics to functionally test the devices prior to shipment to the customer. Additionally, this allows Signetics to extensively stress test, as well as ensure the threshold voltage of each individual EPROM cell. 100% programming yield is subsequently guaranteed.

FUNCTIONAL DIAGRAM



OUTPUT MACRO CELL (OMC)



NOTE:
※ Denotes a programmable cell location.

THE OUTPUT MACRO CELL (OMC)

The PLC18V8Z series devices have 8 individually programmable Output Macro Cells. The 72 AND inputs (or product terms) from the programmable AND array are connected to the 8 OMCs in groups of 9. Eight of the AND terms are dedicated to logic functions; the ninth is for asynchronous direction control, which enables/disables the respective bidirectional I/O pin. Two product terms are dedicated for the Synchronous Preset and Asynchronous Reset functions.

Each OMC can be independently programmed via 16 architecture control bits, $AC1_n$ and $AC2_n$ (one pair per macro cell). Similarly, each OMC has a programmable output polarity control bit (Xn). By configuring the pair of architecture control bits according to the configuration cell table, 4 different configurations may be implemented. Note that the configuration cell is automatically programmed based on the OMC configuration.

DESIGN SECURITY

The PLC18V8Z series devices have a programmable security fuse that controls the access to the data programmed in the device. By using this programmable feature, proprietary designs implemented in the device cannot be copied or retrieved.

CONFIGURATION CELL

A single configuration cell controls the functions of Pins 1 and 11. Refer to Functional Diagram. When the configuration cell is programmed, Pin 1 is a dedicated clock and Pin 11 is dedicated for output enable. When the configuration cell is unprogrammed, Pins 1 and 11 are both dedicated inputs. Note that the output enable for all registered OMCs is common—from Pin 11 only. Output enable control of the bidirectional I/O OMCs is provided from the AND array via the direction product term.

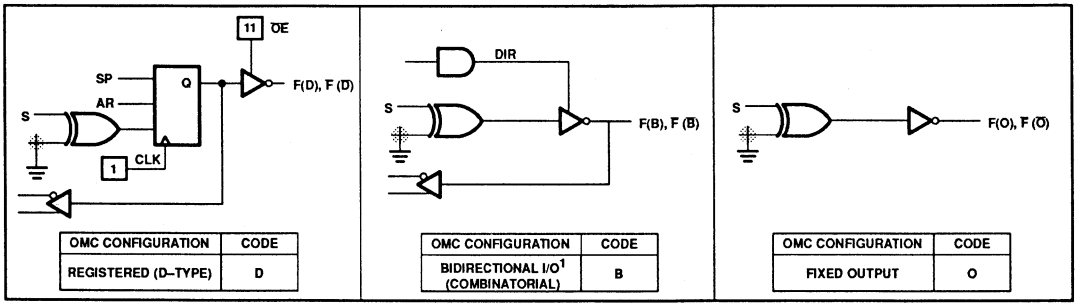
If any one OMC is configured as registered, the configuration cell will be automatically configured (via the design software) to ensure that the clock and output enable functions are enabled on Pins 1 and 11, respectively. If none of the OMCs are registered, the configuration cell will be programmed such that Pins 1 and 11 are dedicated inputs. The programming codes are as follows:

Pin 1 = CLK, Pin 11 = $\overline{OE}$	L
Pin 1 and Pin 11 = Input	H

FUNCTION	CONTROL CELL CONFIGURATIONS			COMMENTS
	$AC1_1$	$AC2_N$	CONFIG. CELL	
Registered mode	Programmed	Programmed	Programmed	Dedicated clock from Pin 1. $\overline{OE}$ Control for all registerd OMCs from Pin 11 only.
Bidirectional I/O mode[1]	Unprogrammed	Unprogrammed	Unprogrammed	Pins 1 and 11 are dedicated inputs. 3-State control from AND array only.
Fixed input mode	Unprogrammed	Programmed	Unprogrammed	Pins 1 and 11 are dedicated inputs.
Fixed output mode	Programmed	Unprogrammed	Unprogrammed	Pins 1 and 11 are dedicated inputs. The feedback path (via F_{MUX}) is disabled.

NOTE:
1. This is the virgin state as shipped from the factory.

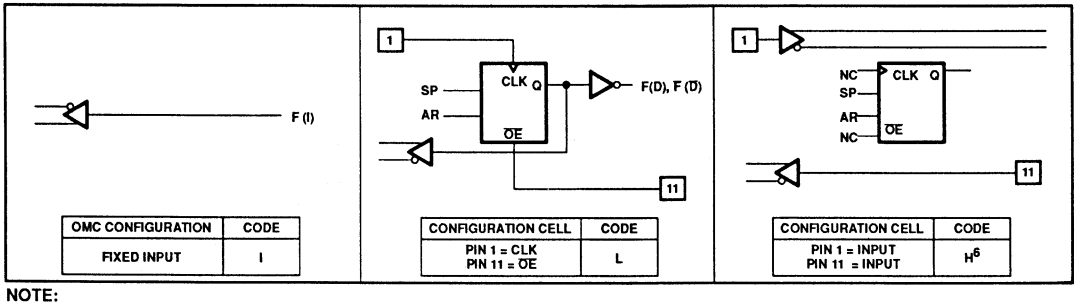
ARCHITECTURE CONTROL—AC1 and AC2



OMC CONFIGURATION	CODE
REGISTERED (D–TYPE)	D

OMC CONFIGURATION	CODE
BIDIRECTIONAL I/O[1] (COMBINATORIAL)	B

OMC CONFIGURATION	CODE
FIXED OUTPUT	O



OMC CONFIGURATION	CODE
FIXED INPUT	I

CONFIGURATION CELL	CODE
PIN 1 = CLK PIN 11 = $\overline{OE}$	L

CONFIGURATION CELL	CODE
PIN 1 = INPUT PIN 11 = INPUT	H[6]

NOTE:
A factory shipped unprogrammed device is configured such that:
1. This is the initial unprogrammed state. All cells are in a conductive state.
2. All AND gates are pulled to a logic "0" (Low).
3. Output polarity is inverting.
4. Pins 1 and 11 are configured as inputs 0 and 9. The clock and $\overline{OE}$ functions are disabled.
5. All Output Macro Cells (OMCs) are configured as bidirectional I/O, with the outputs disabled via the direction term.
6. This configuration cannot be used if any OMCs are configured as registered (Code = D). The configuration cell will be automatically configured to ensure that the clock and output enable functions are enabled on Pins 1 and 11, respectively, if any one OMC is programmed as registered.

Zero standby power CMOS versatile PAL devices

PLC18V8Z35 / PLC18V8ZI

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS	UNIT
V_{CC}	Supply voltage	–0.5 to +7	V_{DC}
V_{CC}	Operating supply voltage	4.5 to 5.5 (Industrial) 4.75 to 5.25 (Commercial)	V_{DC}
V_{IN}	Input voltage	–0.5 to V_{CC} + 0.5	V_{DC}
V_{OUT}	Output voltage	–0.5 to V_{CC} + 0.5	V_{DC}
I_{IN}	Input currents	–10 to +10	mA
I_{OUT}	Output currents	+24	mA
T_{amb}	Operating temperature range	–40 to +85 (Industrial) 0 to +75 (Commercial)	°C
T_{stg}	Storage temperature range	–65 to +150	°C

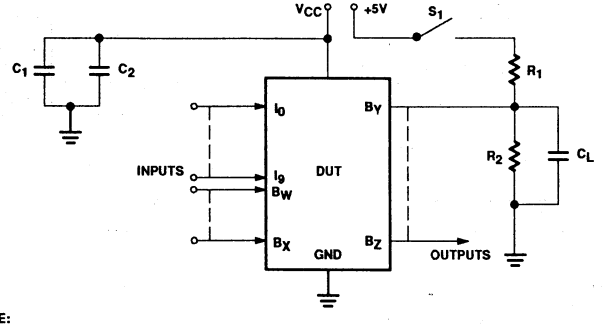
NOTE:

1. Stresses above those listed may cause malfuncion or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

THERMAL RATINGS

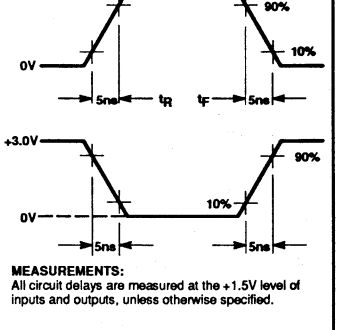
TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

AC TEST CONDITIONS



NOTE:
C_1 and C_2 are to bypass V_{CC} to GND.

VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

DC ELECTRICAL CHARACTERISTICS

Commercial = 0°C ≤ T_{amb} ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V;
Industrial = –40°C ≤ T_{amb} ≤ +85°C, 4.5V ≤ V_{CC} ≤ 5.5V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			MIN	TYP[1]	MAX	
Input voltage						
V_{IL}	Low	V_{CC} = MIN	–0.3		0.8	V
V_{IH}	High	V_{CC} = MAX	2.0		V_{CC} + 0.3	V
Output voltage[2]						
V_{OL}	Low	V_{CC} = MIN, I_{OL} = 20µA V_{CC} = MIN, I_{OL} = 24mA			0.100 0.500	V V
V_{OH}	High	V_{CC} = MIN, I_{OH} = –3.2mA V_{CC} = MIN, I_{OH} = –20µA	2.4 V_{CC} – 0.1V			V V
Input current						
I_{IL}	Low[7]	V_{IN} = GND			–10	µA
I_{IH}	High	V_{IN} = V_{CC}			10	µA
Output current						
$I_{O(OFF)}$	Hi–Z state	V_{OUT} = V_{CC} V_{OUT} = GND			10 –10	µA µA
I_{OS}	Short-circuit[3]	V_{OUT} = GND			–130	mA
I_{CC}	V_{CC} supply current (Standby)	V_{CC} = MAX, V_{IN} = 0 or V_{CC}[8]			100	µA
I_{CC}/f	V_{CC} supply current (Active)[4]	V_{CC} = MAX (CMOS inputs)[5, 6]			1.5	mA/MHz
Capacitance						
C_I	Input	V_{CC} = 5V V_{IN} = 2.0V		12		pF
C_B	I/O	V_B = 2.0V		15		pF

NOTES:
1. All typical values are at V_{CC} = 5V, T_{amb} = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Duration of short-circuit should not exceed one second. Test one at a time.
4. Tested with TTL input levels: V_{IL} = 0.45V, V_{IH} = 2.4V. Measured with all outputs switching.
5. ΔI_{CC}/TTL input = 2mA.
6. ΔI_{CC} vs frequency (registered configuration) = 2mA/MHz.
7. I_{IL} for Pin 1 (I_0/CLK) is ± 10µA with V_{IN} = 0.4V.
8. V_{IN} includes CLK and $\overline{OE}$ if applicable.

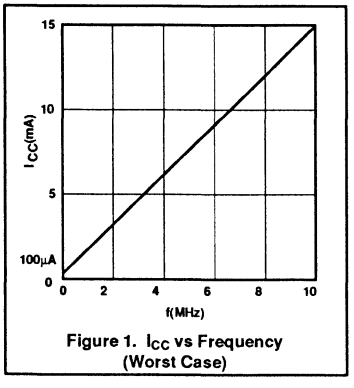


Figure 1. I_{CC} vs Frequency (Worst Case)

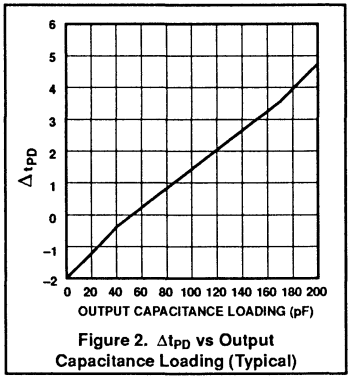


Figure 2. Δt_{PD} vs Output Capacitance Loading (Typical)

AC ELECTRICAL CHARACTERISTICS

Commercial = 0°C ≤ T_{amb} ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V;
Industrial = –40°C ≤ T_{amb} ≤ +85°C, 4.5V ≤ V_{CC} ≤ 5.5V; R_2 = 390Ω

SYMBOL	PARAMETER	FROM	TO	TEST CONDITION[1]		PLC18V8Z35 (Commercial)		PLC18V8ZI (Industrial)		UNIT
				R_1 (Ω)	C_L (pF)	MIN	MAX	MIN	MAX	
Pulse width										
t_{CKP}	Clock period (Minimum $t_{IS} + t_{CKO}$)	CLK +	CLK +	200	50	47		57		ns
t_{CKH}	Clock width High	CLK +	CLK –	200	50	20		25		ns
t_{CKL}	Clock width Low	CLK –	CLK +	200	50	20		25		ns
t_{ARW}	Async reset pulse width	I ±, F±	$I\overline{+}$, $F\overline{+}$			35		40		ns
Hold time										
t_{IH}	Input or feedback data hold time	CLK +	Input ±	200	50	0		0		ns
Setup time										
t_{IS}	Input or feedback data setup time	I ±, F±	CLK +	200	50	25		30		ns
Propagation delay										
t_{PD}	Delay from input to active output	I ±, F±	F±	200	50		35		40	ns
t_{CKO}	Clock High to output valid access Time	CLK +	F±	200	50		22		27	ns
t_{OE1}[3]	Product term enable to outputs off	I ±, F±	F±	Active-High R = 1.5k Active-Low R = 550	50		35		40	ns
t_{OD1}[2]	Product term disable to outputs off	I ±, F±	F±	From V_{OH} R = ∞ From V_{OL} R = 200	5		35		40	ns
t_{OD2}[2]	Pin 11 output disable High to outputs off	OE –	F±	From V_{OH} R = ∞ From V_{OL} R = 200	5		25		30	ns
t_{OE2}[3]	Pin 11 output enable to active output	OE +	F±	Active-High R = 1.5k Active-Low R = 550	50		25		30	ns
t_{ARD}	Async reset delay	I ±, F±	F +				35		40	ns
t_{ARR}	Async reset recovery time	I ±, F±	CLK +			25		30		ns
t_{SPR}	Sync preset recovery time	I ±, F±	CLK +			25		30		ns
t_{PPR}	Power-up reset	V_{CC} +	F +				35		40	ns
Frequency of operation										
f_{MAX}	Maximum frequency	$1/(t_{IS} + t_{CKO})$		200	50		21		18	MHz

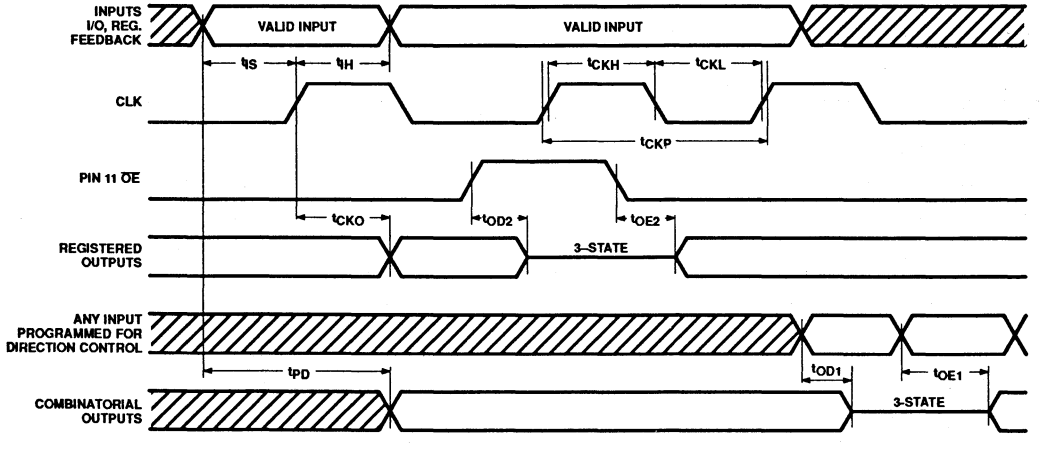
NOTES:
1. Refer also to AC Test Conditions. (Test Load Circuit)
2. For 3-State output; output enable times are tested with C_L = 50pF to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with C_L = 5pF. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} - 0.5V)$ with S_1 open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with S_1 closed.
3. Resistor values of 1.5k and 550Ω provide 3-State levels of 1.0V and 2.0V, respectively. Output timing measurements are to 1.5V level.

POWER-UP RESET

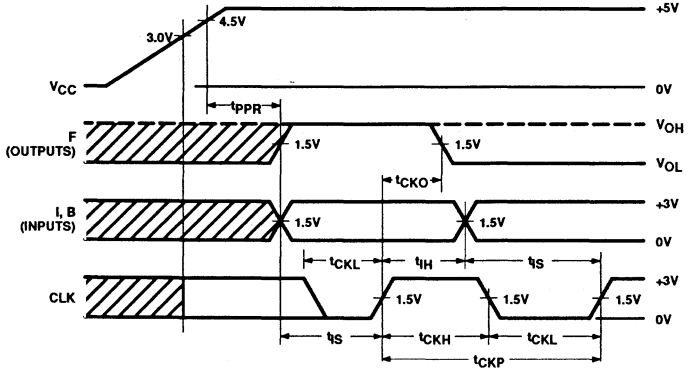
In order to facilitate state machine design and testing, a power-up reset function has been incorporated in the PLC18V8Z. All internal registers will reset to Active-Low (logical "0") after a specified period of time (t_{PPR}).

Therefore, any OMC that has been configured as a registered output will always produce an Active-High on the associated output pin because of the inverted output buffer. The internal feedback (Q) of a registered OMC will also be set Low. The programmed polarity of OMC will not affect the Active-High output condition during a system power-up condition.

TIMING DIAGRAMS



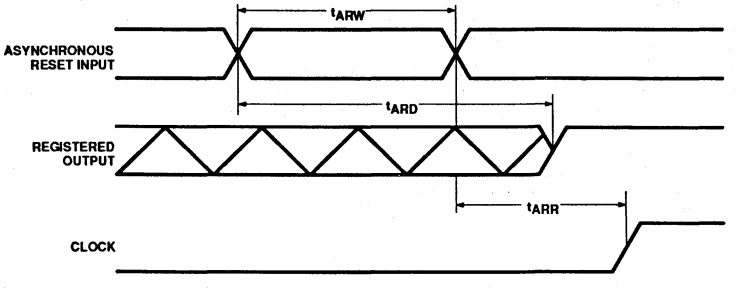
Switching Waveforms



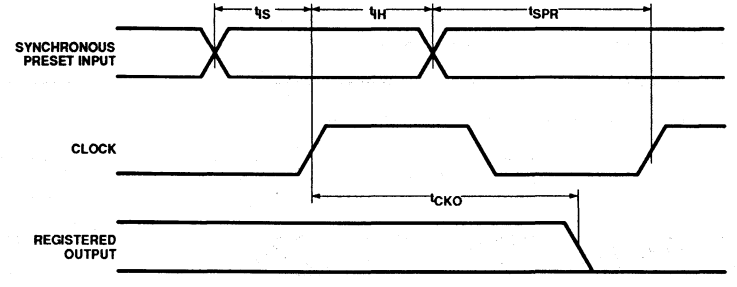
NOTE:
Diagram presupposes that the outputs (F) are enabled. The reset occurs regardless of the output condition (enabled or disabled).

Power-Up Reset

TIMING DIAGRAMS (Continued)



Asynchronous Reset



Synchronous Preset

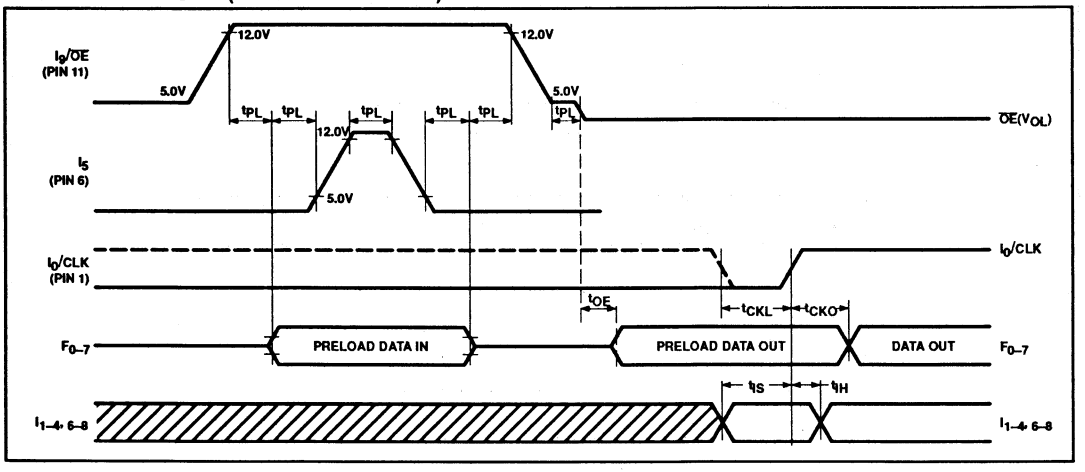
REGISTER PRELOAD FUNCTION (DIAGNOSTIC MODE ONLY)

In order to facilitate the testing of state machine/controller designs, a diagnostic mode register preload feature has been incorporated into the PLC18V8Z series device. This feature enables the user to load the registers with predetermined states while a super voltage is applied to Pins 11 and 6 ($I_9/\overline{OE}$ and I_5). (See diagram for timing and sequence.)

To read the data out, Pins 11 and 6 must be returned to normal TTL levels. The outputs, F_{0-7}, must be enabled in order to read data out. The Q outputs of the registers will reflect data in as input via F_{0-7} during preload. Subsequently, the register Q output via the feedback path will reflect the data in as input via F_{0-7}.

Refer to the voltage waveform for timing and voltage references. t_{PL} = 10µsec.

REGISTER PRELOAD (DIAGNOSTIC MODE)



LOGIC PROGRAMMING

The PLC18V8Z series is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Signetics SLICE and SNAP design software packages. ABEL™ CUPL™ and PALASM® 90 design software packages also support the PLC18V8Z architecture.

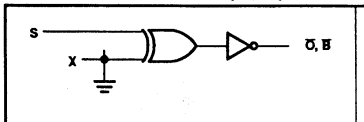
All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

PLC18V8Z logic designs can also be generated using the program table entry format, which is detailed on the following pages. This program table entry format is supported by SLICE only. The SLICE design package is available, free of charge, to qualified users.

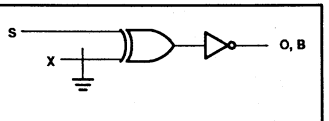
With Logic programming, the AND/OR/Ex-OR gate input connections necessary to implement the desired logic function are coded directly from logic equations using the Program Table. Similarly, various OMC configurations are implemented by programming the Architecture Control bits AC1 and AC2. Note that the configuration cell is automatically programmed based on the OMC configuration.

In this table, the logic state of variables I, P and B associated with each Sum Term S is assigned a symbol which results in the proper fusing pattern of corresponding link pairs, defined as follows:

OUTPUT POLARITY – (O, B)

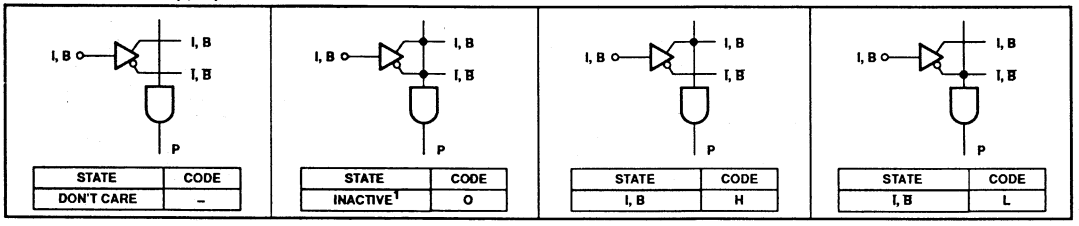


ACTIVE LEVEL	CODE
INVERTING[1]	L



ACTIVE LEVEL	CODE
NON-INVERTING	H

"AND" ARRAY – (I, B)



STATE	CODE
DON'T CARE	–

STATE	CODE
INACTIVE[1]	O

STATE	CODE
I, B	H

STATE	CODE
I, B	L

NOTE:
1. A factory shipped unprogrammed device is configured such that all cells are in a conductive state.

ERASURE CHARACTERISTICS (For Quartz Window Packages Only)

The erasure characteristics of the PLC18V8Z Series devices are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lighting could erase a typical PLC18V8Z in approximately three years, while it would take approximately one week to cause erasure when exposed to direct sunlight. If the PLC18V8Z is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure for the PLC18V8Z is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15Wsec/cm^2. The erasure time with this dosage is approximately 30 to 35 minutes using an ultraviolet lamp with a 12,000µW/cm^2 power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose a CMOS EPLD can be exposed to without damage is 7258Wsec/cm^2). Exposure of these CMOS EPLDs to high intensity UV light for longer periods may cause permanent damage.

The maximum number of guaranteed erase/write cycles is 50. Data retention exceeds 20 years.

PROGRAMMING/SOFTWARE SUPPORT

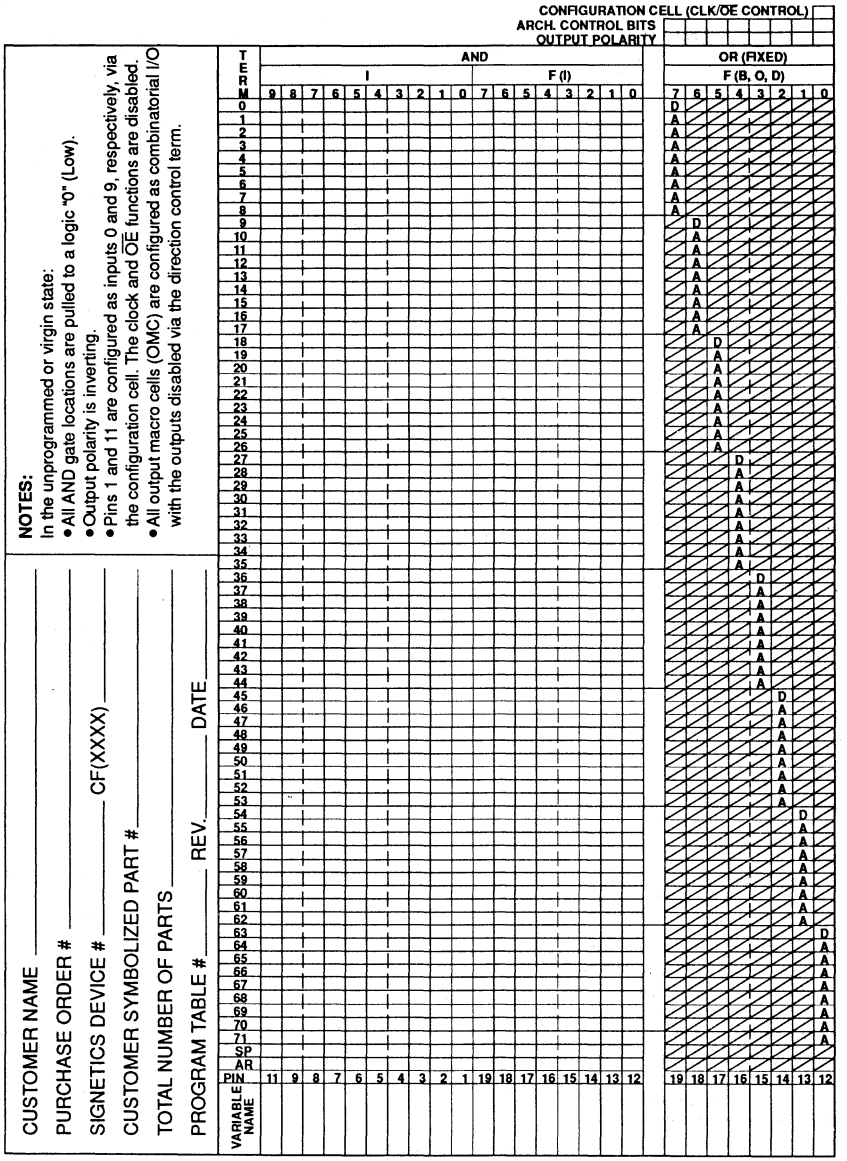
Refer to Section 8 *(Development Software)* and Section 9 *(Third-Party Programmer/ Software Support)* of this data handbook for additional information.

ABEL is a trademark of Data I/O Corp.
CUPL is a trademark of Logical Devices, Inc.
PALASM is a registered trademark of AMD Corp.

Zero standby power CMOS versatile PAL devices

PLC18V8Z35 / PLC18V8ZI

PROGRAM TABLE



AND ARRAY	
INACTIVE	O
I, F (I, B)	H
I, F (I, B)	L
**DON'T CARE	–

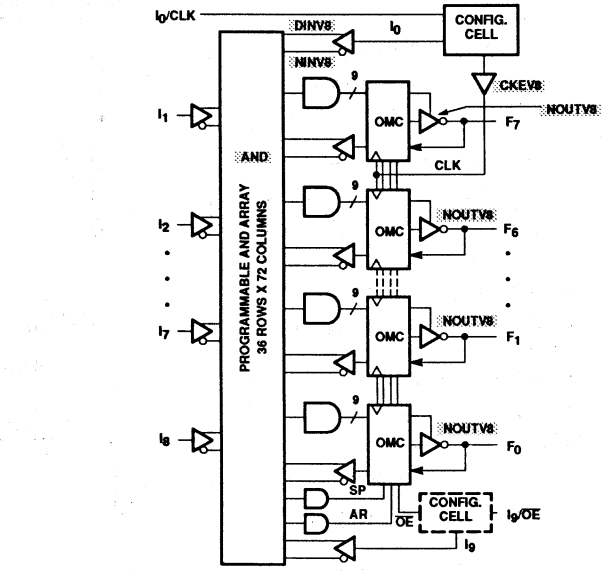
CONTROL			
OMC ARCH.		OUTPUT POLARITY	
REGISTERED (D-TYPE)	D	NON-INVERTING	H
FIXED INPUT	I	INVERTING	L
FIXED OUTPUT	O	CONFIG. CELL*	
BIDIRECTIONAL I/O	B	PIN 1 = CLK; PIN 11 = OE	L
		PIN 1, PIN 11 = INPUT	H

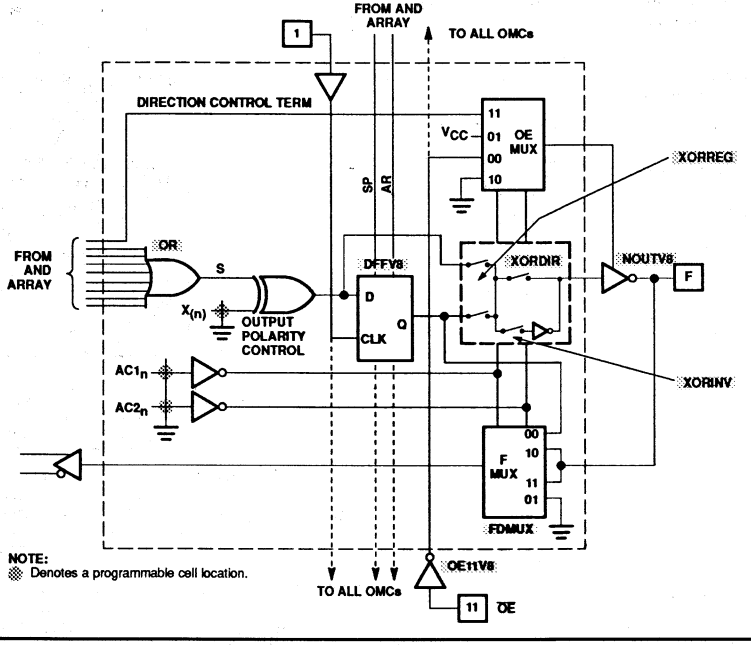
OR ARRAY (FIXED)	
DIRECTION CONTROL	D
ACTIVE OUTPUT	A
NOT USED	

DATA CANNOT BE ENTERED INTO THE OR ARRAY FIELD DUE TO THE FIXED NATURE OF THE DEVICE ARCHITECTURE.

* THE CONFIGURATION CELL IS AUTOMATICALLY PROGRAMMED BASED ON THE OMC ARCHITECTURE.
** FOR SP, AR: "–" IS NOT ALLOWED.

SNAP RESOURCE SUMMARY DESIGNATIONS





Zero standby power CMOS versatile PAL devices

PLC18V8Z25/PLC18V8ZIA

DESCRIPTION

The PLC18V8Z is a universal PAL® device featuring high performance and virtually zero-standby power for power sensitive applications. They are reliable, user-configurable substitutes for discrete TTL/CMOS logic. While compatible with TTL and HCT logic, the PLC18V8Z can also replace HC logic over the V_{CC} range of 4.5 to 5.5V.

The PLC18V8Z is a two-level logic element comprised of 10 inputs, 74 AND gates (product terms) and 8 output Macro cells.

Each output features an "Output Macro Cell" which can be individually configured as a dedicated input, a combinatorial output, or a registered output with internal feedback. As a result, the PLC18V8Z is capable of emulating all common 20-pin PAL devices to reduce documentation, inventory, and manufacturing costs.

A power-up reset function and a Register Preload function have been incorporated in the PLC18V8Z architecture to facilitate state machine design and testing.

With a standby current of less than 100µA and active power consumption of 1.5mA/MHz, the PLC18V8Z is ideally suited for power sensitive applications in battery operated/backed portable instruments and computers.

The PLC18V8Z is also processed to industrial requirements for operation over an extended temperature range of -40°C to +85°C and supply voltage of 4.5V to 5.5V.

Ordering information can be found below.

FEATURES

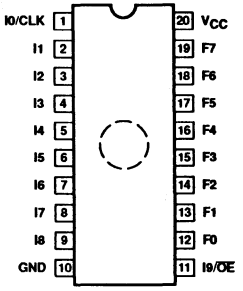
- 20-pin Universal Programmable Array Logic
- Virtually Zero-Standby-power
- Functional replacement for Series 20 PAL devices
  - I_{OL} = 24mA
- High-performance CMOS EPROM cell technology
  - Erasable
  - Reconfigurable
  - 100% testable
- 25ns Max propagation delay (comm)
- Up to 18 inputs and 8 input/output macro cells
- Programmable output polarity
- Power-up reset on all registers
- Register Preload capability
- Synchronous Preset/Asynchronous Reset
- Security fuse to prevent duplication of proprietary designs
- Design support provided using SLICE software development package and other CAD tools for PLDs
- Available in 300mil-wide DIP with quartz window, plastic DIP (OTP) or PLCC (OTP)

APPLICATIONS

- Battery powered instruments
- Laptop and pocket computers
- Industrial control
- Medical Instruments
- Portable communications equipment

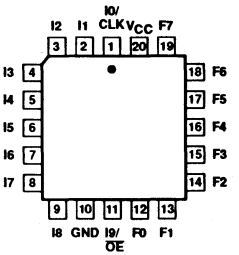
PIN CONFIGURATIONS

N and FA Packages



N = Plastic DIP (300mil-wide)
FA = Ceramic DIP with Quartz Window (300mil-wide)

A Package



A = Plastic Leaded Chip Carrier

PIN LABEL DESCRIPTIONS

I	Dedicated input
B	Bidirectional input/output
O	Dedicated output
D	Registered output (D-type flip-flop)
F	Macrocell Input/Output
CLK	Clock Input
$\overline{OE}$	Output Enable
V_{CC}	Supply Voltage
GND	Ground

ORDERING INFORMATION

DESCRIPTION	OPERATING CONDITIONS	ORDER CODE
20-Pin Plastic Dual In-Line Package 300mil-wide (t_{PD} = 25ns)	Commercial	PLC18V8Z25N
20-Pin Ceramic Dual In-Line Package 300mil-wide with quartz window (t_{PD} = 25ns)	Temperature Range	PLC18V8Z25FA
20-Pin Plastic Leaded Chip Carrier 350mil square (t_{PD} = 25ns)	± 5% Power Supplies	PLC18V8Z25A
20-Pin Plastic Dual In-Line Package 300mil-wide (t_{PD} = 25ns)	Industrial	PLC18V8ZIAN
20-Pin Ceramic Dual In-Line Package 300mil-wide with quartz window (t_{PD} = 25ns)	Temperature Range	PLC18V8ZIAFA
20-Pin Plastic Leaded Chip Carrier 350mil square (t_{PD} = 25ns)	± 10% Power Supplies	PLC18V8ZIAA

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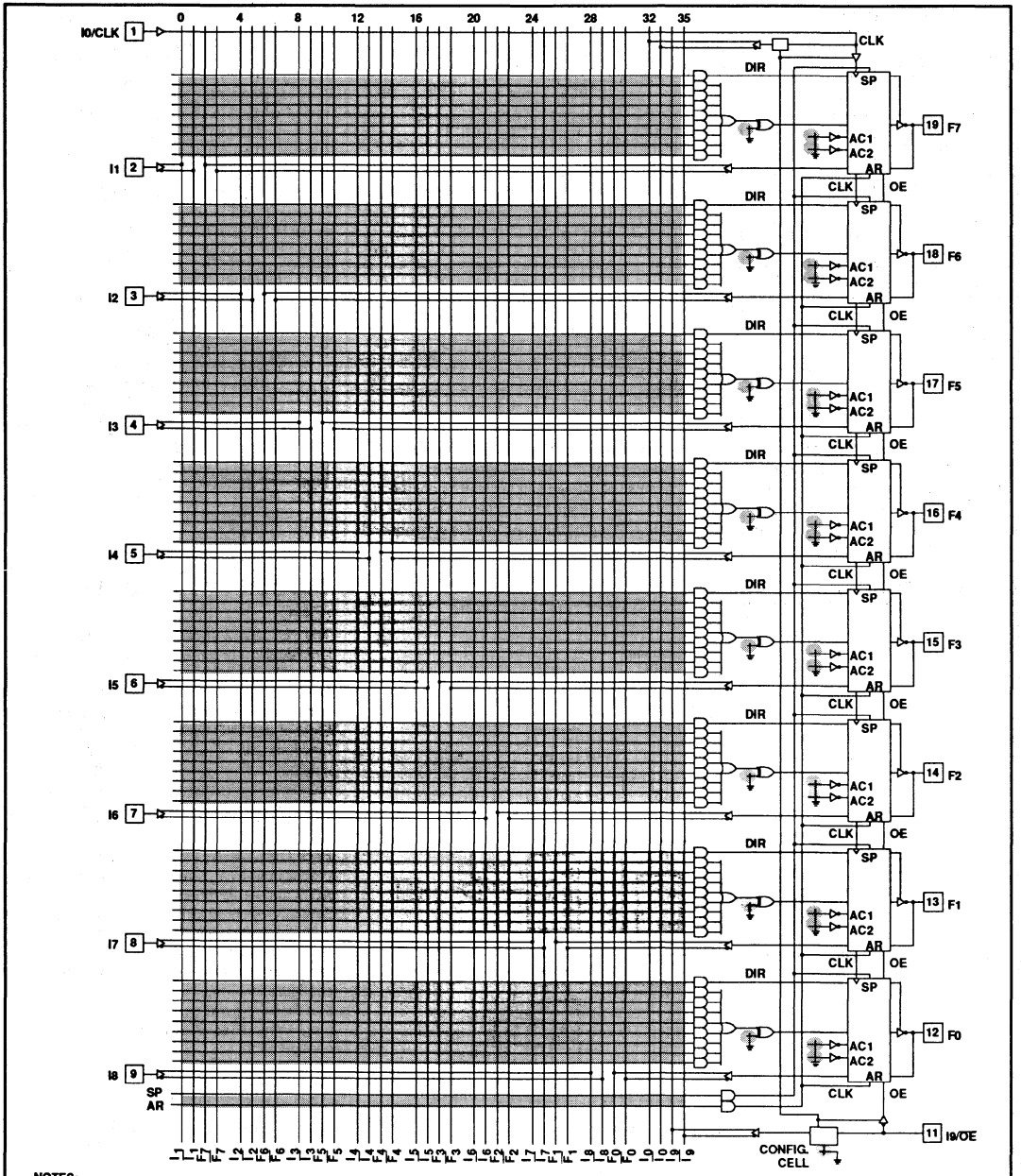
LOGIC DIAGRAM



NOTES:
In the unprogrammed or virgin state:

All cells are in a conductive state.
All AND gate locations are pulled to a logic "0" (Low).
Output polarity is inverting.

Pins 1 and 11 are configured as Inputs 0 and 9, respectively, via the configuration cell. The clock and OE functions are disabled.
All output macro cells (OMC) are configured as bidirectional I/O, with the outputs disabled via the direction term.
Denotes a programmable cell location.

Zero standby power CMOS versatile PAL devices

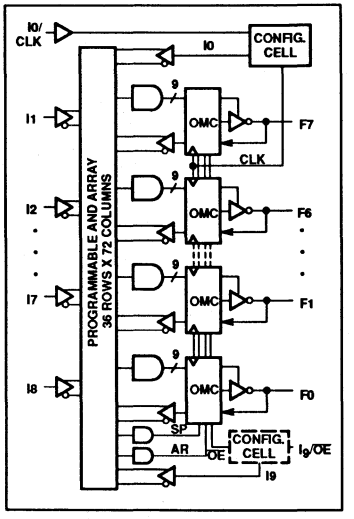
PLC18V8Z25/PLC18V8ZIA

PAL DEVICE TO PLC18V8Z OUTPUT PIN CONFIGURATION CROSS REFERENCE

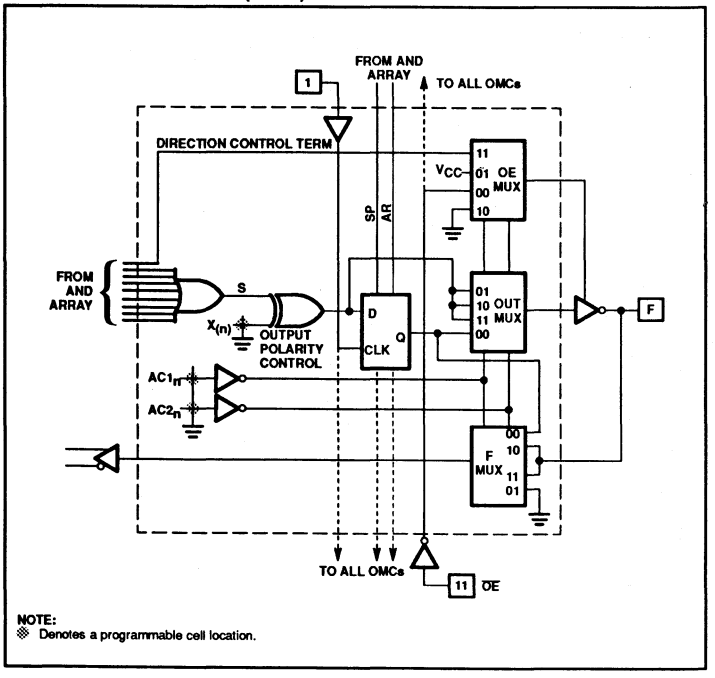
PIN NO.	PLC 18V8Z	16L8 16H8 16P8 16P8	16R4 16RP4	16R6 16RP6	16R8 16RP8	16L2 16H2 16P2	14L4 14H4 14P4	12L6 12H6 12P6	10L8 10H8 10P8
1	I_0/CLK	I	CLK	CLK	CLK	I	I	I	I
19	F7	B	B	B	D	I	I	I	O
18	F6	B	B	D	D	I	I	O	O
17	F5	B	D	D	D	I	O	O	O
16	F4	B	D	D	D	O	O	O	O
15	F3	B	D	D	D	O	O	O	O
14	F2	B	D	D	D	I	O	O	O
13	F1	B	B	D	D	I	I	O	O
12	F0	B	B	B	D	I	I	I	O
11	I_9/$\overline{OE}$	I	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	I	I	I	I

The Signetics state-of-the-art Floating-Gate CMOS EPROM process yields bipolar equivalent performance at less than one-quarter the power consumption. The erasable nature of the EPROM process enables Signetics to functionally test the devices prior to shipment to the customer. Additionally, this allows Signetics to extensively stress test, as well as ensure the threshold voltage of each individual EPROM cell. 100% programming yield is subsequently guaranteed.

FUNCTIONAL DIAGRAM



OUTPUT MACRO CELL (OMC)



NOTE:
▒ Denotes a programmable cell location.

THE OUTPUT MACRO CELL (OMC)

The PLC18V8Z series devices have 8 individually programmable Output Macro Cells. The 72 AND inputs (or product terms) from the programmable AND array are connected to the 8 OMCs in groups of 9. Eight of the AND terms are dedicated to logic functions; the ninth is for asynchronous direction control, which enables/disables the respective bidirectional I/O pin. Two product terms are dedicated for the Synchronous Preset and Asynchronous Reset functions.

Each OMC can be independently programmed via 16 architecture control bits, $AC1_n$ and $AC2_n$ (one pair per macro cell). Similarly, each OMC has a programmable output polarity control bit (Xn). By configuring the pair of architecture control bits according to the configuration cell table, 4 different configurations may be implemented. Note that the configuration cell is automatically programmed based on the OMC configuration.

DESIGN SECURITY

The PLC18V8Z series devices have a programmable security fuse that controls the access to the data programmed in the device. By using this programmable feature, proprietary designs implemented in the device cannot be copied or retrieved.

CONFIGURATION CELL

A single configuration cell controls the functions of Pins 1 and 11. Refer to Functional Diagram. When the configuration cell is programmed, Pin 1 is a dedicated clock and Pin 11 is dedicated for output enable. When the configuration cell is unprogrammed, Pins 1 and 11 are both dedicated inputs. Note that the output enable for all registered OMCs is common—from Pin 11 only. Output enable control of the bidirectional I/O OMCs is provided from the AND array via the direction product term.

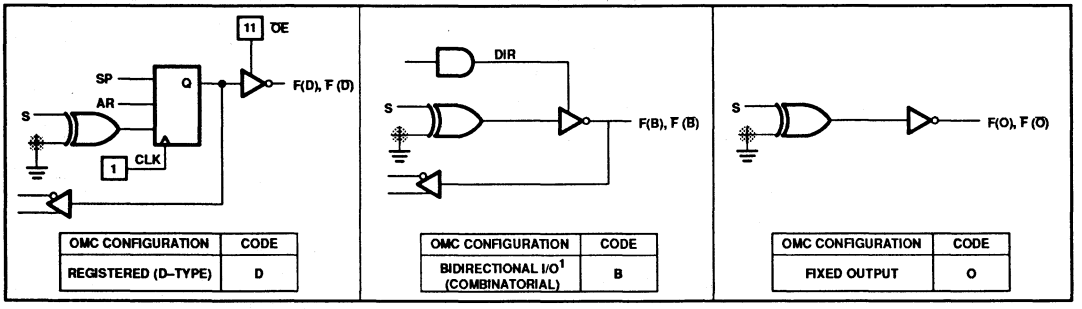
If any one OMC is configured as registered, the configuration cell will be automatically configured (via the design software) to ensure that the clock and output enable functions are enabled on Pins 1 and 11, respectively. If none of the OMCs are registered, the configuration cell will be programmed such that Pins 1 and 11 are dedicated inputs. The programming codes are as follows:

Pin 1 = CLK, Pin 11 = $\overline{OE}$	L
Pin 1 and Pin 11 = Input	H

FUNCTION	CONTROL CELL CONFIGURATIONS			COMMENTS
	$AC1_1$	$AC2_N$	CONFIG. CELL	
Registered mode	Programmed	Programmed	Programmed	Dedicated clock from Pin 1. $\overline{OE}$ Control for all registerd OMCs from Pin 11 only.
Bidirectional I/O mode[1]	Unprogrammed	Unprogrammed	Unprogrammed	Pins 1 and 11 are dedicated inputs. 3-State control from AND array only.
Fixed input mode	Unprogrammed	Programmed	Unprogrammed	Pins 1 and 11 are dedicated inputs.
Fixed output mode	Programmed	Unprogrammed	Unprogrammed	Pins 1 and 11 are dedicated inputs. The feedback path (via F_{MUX}) is disabled.

NOTE:
1. This is the virgin state as shipped from the factory.

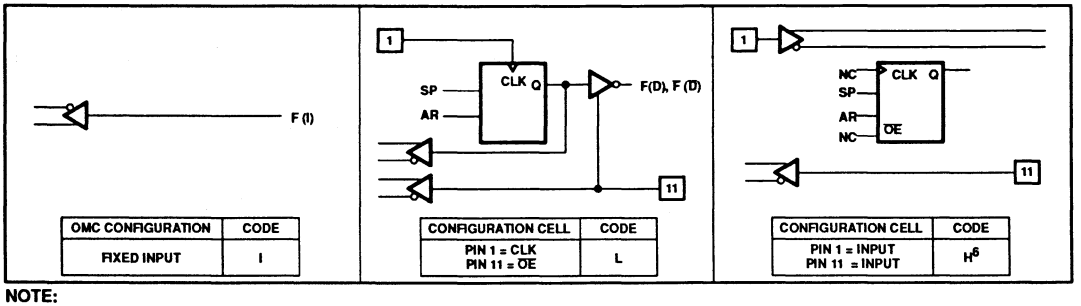
ARCHITECTURE CONTROL—AC1 and AC2



OMC CONFIGURATION	CODE
REGISTERED (D-TYPE)	D

OMC CONFIGURATION	CODE
BIDIRECTIONAL I/O[1] (COMBINATORIAL)	B

OMC CONFIGURATION	CODE
FIXED OUTPUT	O



OMC CONFIGURATION	CODE
FIXED INPUT	I

CONFIGURATION CELL	CODE
PIN 1 = CLK PIN 11 = $\overline{OE}$	L

CONFIGURATION CELL	CODE
PIN 1 = INPUT PIN 11 = INPUT	H[6]

NOTE:
A factory shipped unprogrammed device is configured such that:
1. This is the initial unprogrammed state. All cells are in a conductive state.
2. All AND gates are pulled to a logic "0" (Low).
3. Output polarity is inverting.
4. Pins 1 and 11 are configured as inputs 0 and 9. The clock and $\overline{OE}$ functions are disabled.
5. All Output Macro Cells (OMCs) are configured as bidirectional I/O, with the outputs disabled via the direction term.
6. This configuration cannot be used if any OMCs are configured as registered (Code = D).

ABSOLUTE MAXIMUM RATINGS[1]

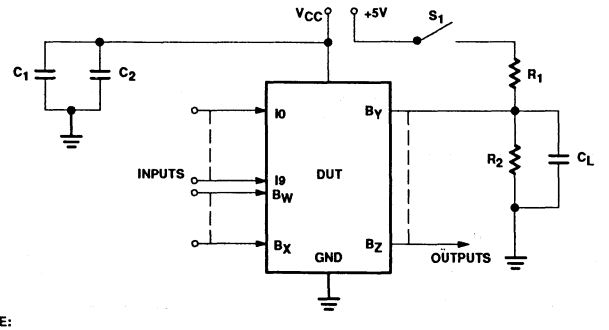
SYMBOL	PARAMETER	RATINGS	UNIT
V_{CC}	Supply voltage	–0.5 to +7	V_{DC}
V_{CC}	Operating supply voltage	4.5 to 5.5 (Industrial) 4.75 to 5.25 (Commercial)	V_{DC}
V_{IN}	Input voltage	–0.5 to V_{CC} + 0.5	V_{DC}
V_{OUT}	Output voltage	–0.5 to V_{CC} + 0.5	V_{DC}
I_{IN}	Input currents	–10 to +10	mA
I_{OUT}	Output currents	+24	mA
T_{amb}	Operating temperature range	–40 to +85 (Industrial) 0 to +75 (Commercial)	°C
T_{stg}	Storage temperature range	–65 to +150	°C

NOTE:
1. Stresses above those listed may cause malfuncion or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

THERMAL RATINGS

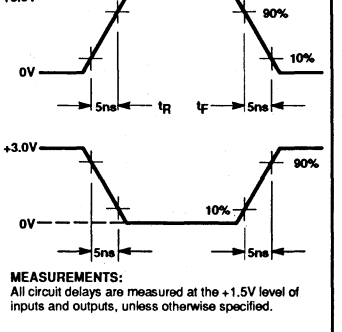
TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

AC TEST CONDITIONS



NOTE:
C_1 and C_2 are to bypass V_{CC} to GND.

VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

DC ELECTRICAL CHARACTERISTICS

Commercial = $0°C \le T_{amb} \le +75°C$, $4.75V \le V_{CC} \le 5.25V$;
Industrial = $-40°C \le T_{amb} \le +85°C$, $4.5V \le V_{CC} \le 5.5V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			MIN	TYP[1]	MAX	
Input voltage						
V_{IL}	Low	V_{CC} = MIN	–0.3		0.8	V
V_{IH}	High	V_{CC} = MAX	2.0		V_{CC} + 0.3	V
Output voltage[2]						
V_{OL}	Low	V_{CC} = MIN, I_{OL} = 20µA V_{CC} = MIN, I_{OL} = 24mA			0.100 0.500	V V
V_{OH}	High	V_{CC} = MIN, I_{OH} = –3.2mA V_{CC} = MIN, I_{OH} = –20µA	2.4 V_{CC} – 0.1V			V V
Input current						
I_{IL}	Low[7]	V_{IN} = GND			–10	µA
I_{IH}	High	V_{IN} = V_{CC}			10	µA
Output current						
$I_{O(OFF)}$	Hi-Z state	V_{OUT} = V_{CC} V_{OUT} = GND			10 –10	µA µA
I_{OS}	Short-circuit[3]	V_{OUT} = GND			–130	mA
I_{CC}	V_{CC} supply current (Standby)	V_{CC} = MAX, V_{IN} = 0 or V_{CC}[8]			100	µA
I_{CC}/f	V_{CC} supply current (Active)[4]	V_{CC} = MAX (CMOS inputs)[5, 6]			1.5	mA/MHz
Capacitance						
C_I	Input	V_{CC} = 5V V_{IN} = 2.0V		12		pF
C_B	I/O	V_B = 2.0V		15		pF

NOTES:
1. All typical values are at V_{CC} = 5V, T_{amb} = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Duration of short-circuit should not exceed one second. Test one at a time.
4. Tested with TTL input levels: V_{IL} = 0.45V, V_{IH} = 2.4V. Measured with all outputs switching.
5. ΔI_{CC}/TTL input = 2mA.
6. ΔI_{CC} vs frequency (registered configuration) = 2mA/MHz.
7. I_{IL} for Pin 1 (I_O/CLK) is ± 10µA with V_{IN} = 0.4V.
8. V_{IN} includes CLK and $\overline{OE}$ if applicable.

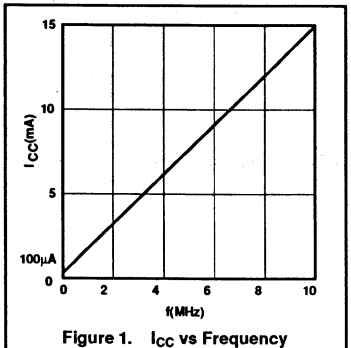


Figure 1. I_{CC} vs Frequency (Worst Case)

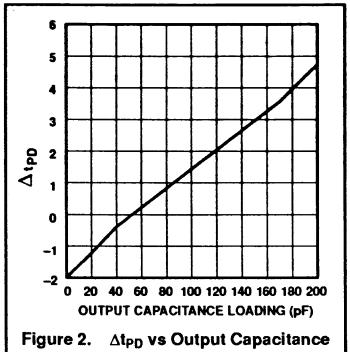


Figure 2. Δt_{PD} vs Output Capacitance Loading (Typical)

AC ELECTRICAL CHARACTERISTICS

Commercial = 0°C ≤ T_{amb} ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V;
Industrial = –40°C ≤ T_{amb} ≤ +85°C, 4.5V ≤ V_{CC} ≤ 5.5V; R_2 = 390Ω

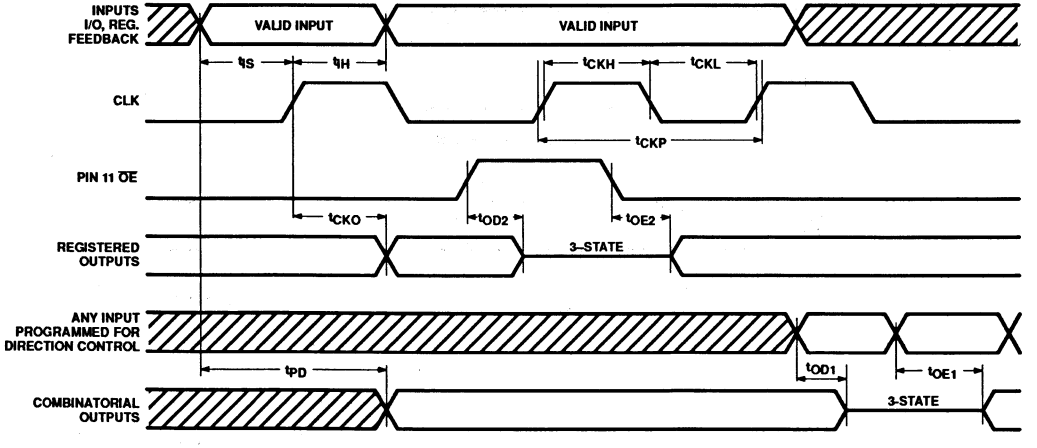
SYMBOL	PARAMETER	FROM	TO	TEST CONDITION[1]		PLC18V8Z25 (Commercial)		PLC18V8ZIA (Industrial)		UNIT
				R_1 (Ω)	C_L (pF)	MIN	MAX	MIN	MAX	
Pulse width										
t_{CKP}	Clock period (Minimum $t_{IS} + t_{CKO}$)	CLK +	CLK +	200	50	33		33		ns
t_{CKH}	Clock width High	CLK +	CLK –	200	50	15		15		ns
t_{CKL}	Clock width Low	CLK –	CLK +	200	50	15		15		ns
t_{ARW}	Async reset pulse width	I ±, F±	I ∓, F ∓			25		25		ns
Hold time										
t_{IH}	Input or feedback data hold time	CLK +	Input ±	200	50	0		0		ns
Setup time										
t_{IS}	Input or feedback data setup time	I ±, F±	CLK +	200	50	18		18		ns
Propagation delay										
t_{PD}	Delay from input to active output	I ±, F±	F±	200	50		25		25	ns
t_{CKO}	Clock High to output valid access Time	CLK +	F±	200	50		15		15	ns
t_{OE1}[3]	Product term enable to outputs off	I ±, F±	F±	Active-High R = 1.5k Active-Low R = 550	50		25		25	ns
t_{OD1}[2]	Product term disable to outputs off	I ±, F±	F±	From V_{OH} R = ∞ From V_{OL} R = 200	5		25		25	ns
t_{OD2}[2]	Pin 11 output disable High to outputs off	OE –	F±	From V_{OH} R = ∞ From V_{OL} R = 200	5		20		20	ns
t_{OE2}[3]	Pin 11 output enable to active output	OE +	F±	Active-High R = 1.5k Active-Low R = 550	50		20		20	ns
t_{ARD}	Async reset delay	I ±, F±	F +				30		30	ns
t_{ARR}	Async reset recovery time	I ±, F±	CLK +			20		20		ns
t_{SPR}	Sync preset recovery time	I ±, F±	CLK +			20		20		ns
t_{PPR}	Power-up reset	V_{CC} +	F +				25		25	ns
Frequency of operation										
f_{MAX}	Maximum frequency	$1/(t_{IS} + t_{CKO})$		200	50		30		30	MHz

NOTES:
1. Refer also to AC Test Conditions. (Test Load Circuit)
2. For 3-State output; output enable times are tested with C_L = 50pF to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with C_L = 5pF. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} - 0.5V)$ with S_1 open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with S_1 closed.
3. Resistor values of 1.5k and 550Ω provide 3-State levels of 1.0V and 2.0V, respectively. Output timing measurements are to 1.5V level.
4. Leave all the cells on unused product terms intact (unprogrammed) for all patterns.

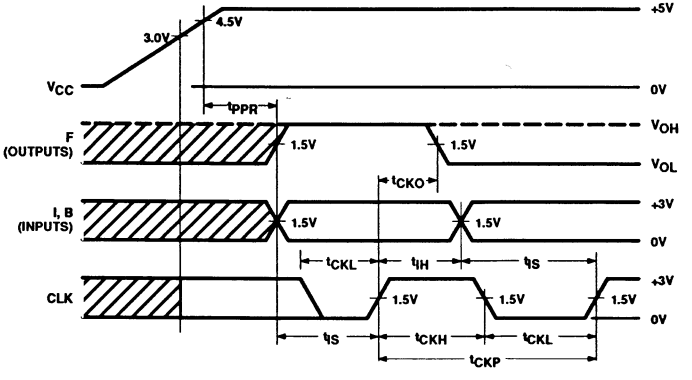
POWER-UP RESET

In order to facilitate state machine design and testing, a power-up reset function has been incorporated in the PLC18V8Z. All internal registers will reset to Active-Low (logical "0") after a specified period of time (t_{PPR}). Therefore, any OMC that has been configured as a registered output will always produce an Active-High on the associated output pin because of the inverted output buffer. The internal feedback (Q) of a registered OMC will also be set Low. The programmed polarity of OMC will not affect the Active-High output condition during a system power-up condition.

TIMING DIAGRAMS



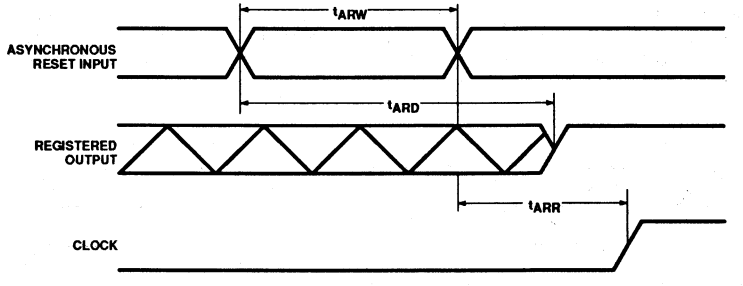
Switching Waveforms



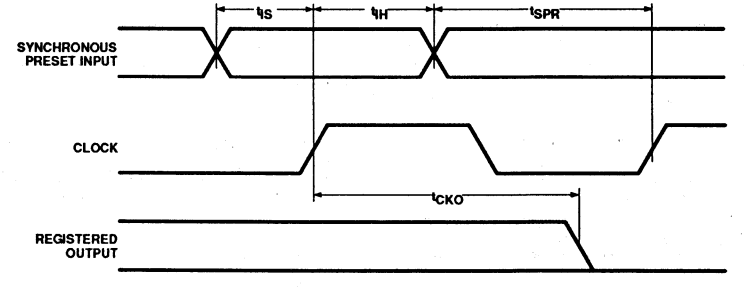
NOTE:
Diagram presupposes that the outputs (F) are enabled. The reset occurs regardless of the output condition (enabled or disabled).

Power-Up Reset

TIMING DIAGRAMS (Continued)



Asynchronous Reset



Synchronous Preset

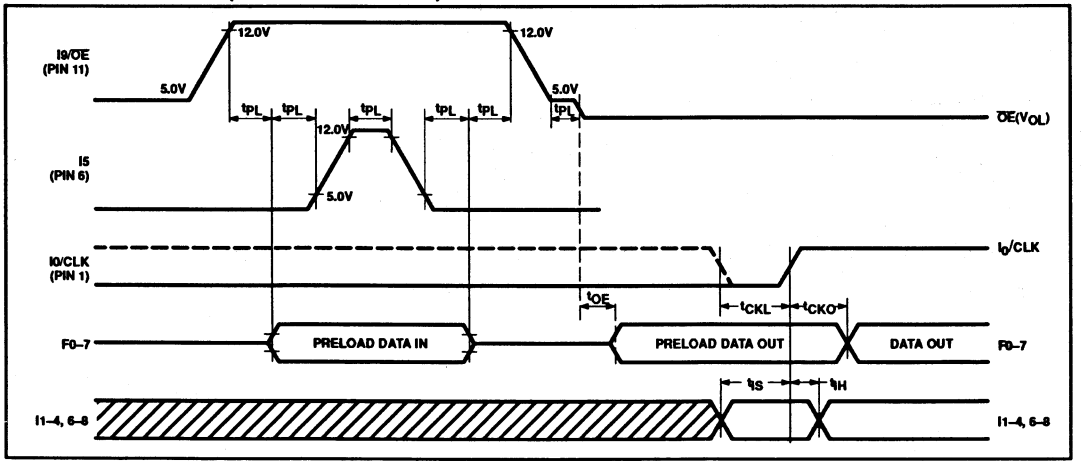
REGISTER PRELOAD FUNCTION (DIAGNOSTIC MODE ONLY)

In order to facilitate the testing of state machine/controller designs, a diagnostic mode register preload feature has been incorporated into the PLC18V8Z series device. This feature enables the user to load the registers with predetermined states while a super voltage is applied to Pins 11 and 6 (I9/$\overline{OE}$ and I5). (See diagram for timing and sequence.)

To read the data out, Pins 11 and 6 must be returned to normal TTL levels. The outputs, F0 – F7, must be enabled in order to read data out. The Q outputs of the registers will reflect data in as input via F0 – F7 during preload. Subsequently, the register Q output via the feedback path will reflect the data in as input via F0 – F7.

Refer to the voltage waveform for timing and voltage references. t_{PL} = 10μsec.

REGISTER PRELOAD (DIAGNOSTIC MODE)



LOGIC PROGRAMMING

The PLC18V8Z series is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Signetics SLICE and SNAP design software packages. ABEL™ CUPL™ and PALASM® 90 design software packages also support the PLC18V8Z architecture.

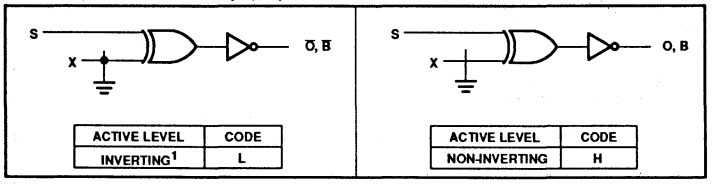
All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

PLC18V8Z logic designs can also be generated using the program table entry format, which is detailed on the following pages. This program table entry format is supported by SLICE only. The SLICE design package is available, free of charge, to qualified users.

With Logic programming, the AND/OR/Ex-OR gate input connections necessary to implement the desired logic function are coded directly from logic equations using the Program Table. Similarly, various OMC configurations are implemented by programming the Architecture Control bits AC1 and AC2. Note that the configuration cell is automatically programmed based on the OMC configuration.

In this table, the logic state of variables I, P and B associated with each Sum Term S is assigned a symbol which results in the proper fusing pattern of corresponding link pairs, defined as follows:

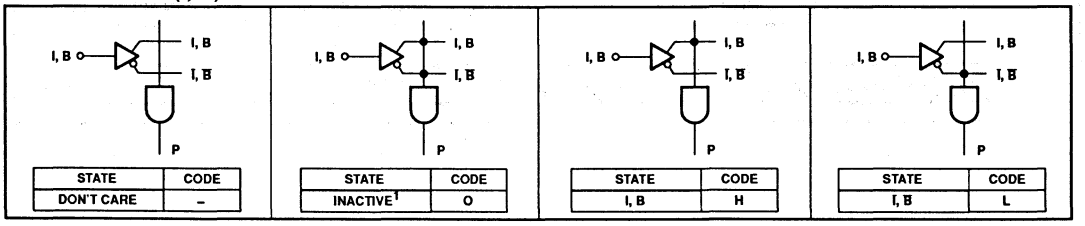
OUTPUT POLARITY – (O, B)



ACTIVE LEVEL	CODE
INVERTING[1]	L

ACTIVE LEVEL	CODE
NON-INVERTING	H

"AND" ARRAY – (I, B)



STATE	CODE
DON'T CARE	–

STATE	CODE
INACTIVE[1]	O

STATE	CODE
I, B	H

STATE	CODE
I, B̄	L

NOTE:
1. A factory shipped unprogrammed device is configured such that all cells are in a conductive state.

ERASURE CHARACTERISTICS (For Quartz Window Packages Only)

The erasure characteristics of the PLC18V8Z Series devices are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lighting could erase a typical PLC18V8Z in approximately three years, while it would take approximately one week to cause erasure when exposed to direct sunlight. If the PLC18V8Z is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure for the PLC18V8Z is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15Wsec/cm^2. The erasure time with this dosage is approximately 30 to 35 minutes using an ultraviolet lamp with a 12,000µW/cm^2 power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose a CMOS EPLD can be exposed to without damage is 7258Wsec/cm^2). Exposure of these CMOS EPLDs to high intensity UV light for longer periods may cause permanent damage.

The maximum number of guaranteed erase/write cycles is 50. Data retention exceeds 20 years.

PROGRAMMING/SOFTWARE SUPPORT

Refer to Section 8 *(Development Software)* and Section 9 *(Third-Party Programmer/ Software Support)* of this data handbook for additional information.

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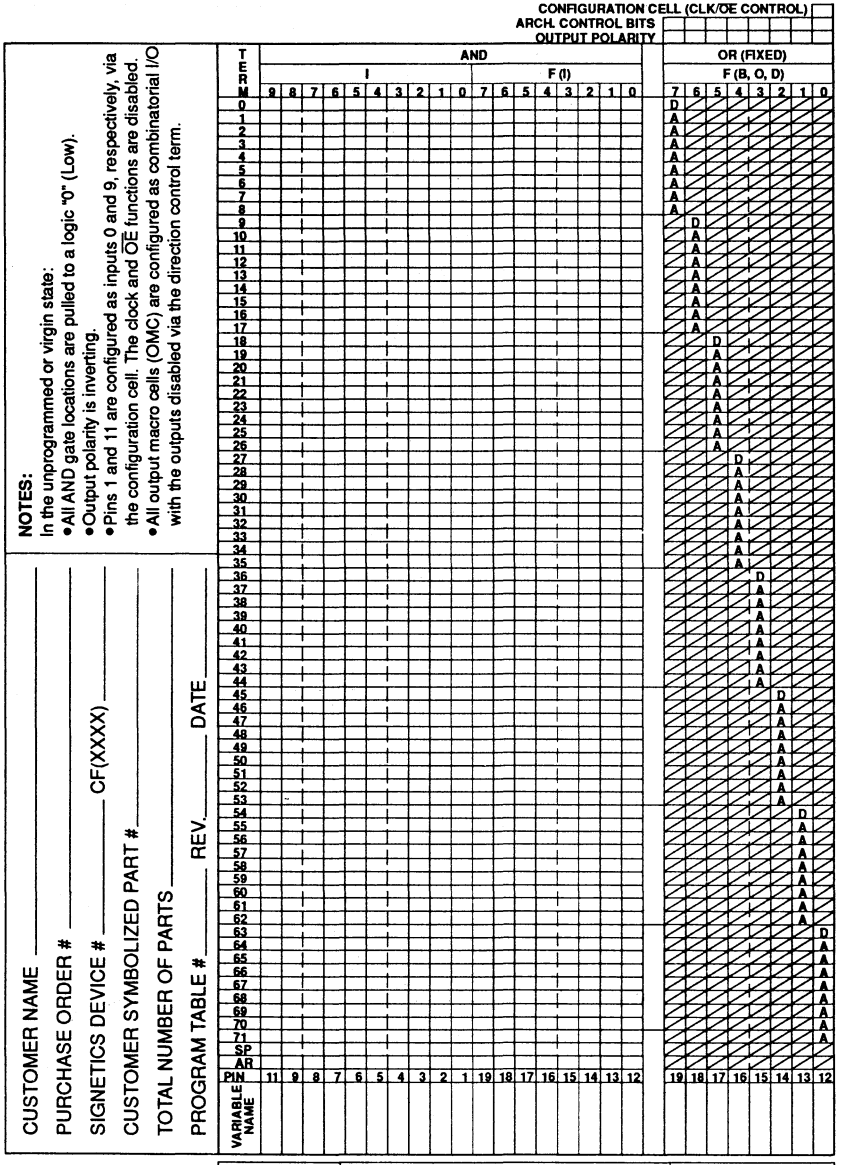
CUPL is a trademark of Logical Devices, Inc.
PALASM is a registered trademark of AMD Corp.

Zero standby power CMOS versatile PAL devices

PLC18V8Z25/PLC18V8ZIA

PROGRAM TABLE



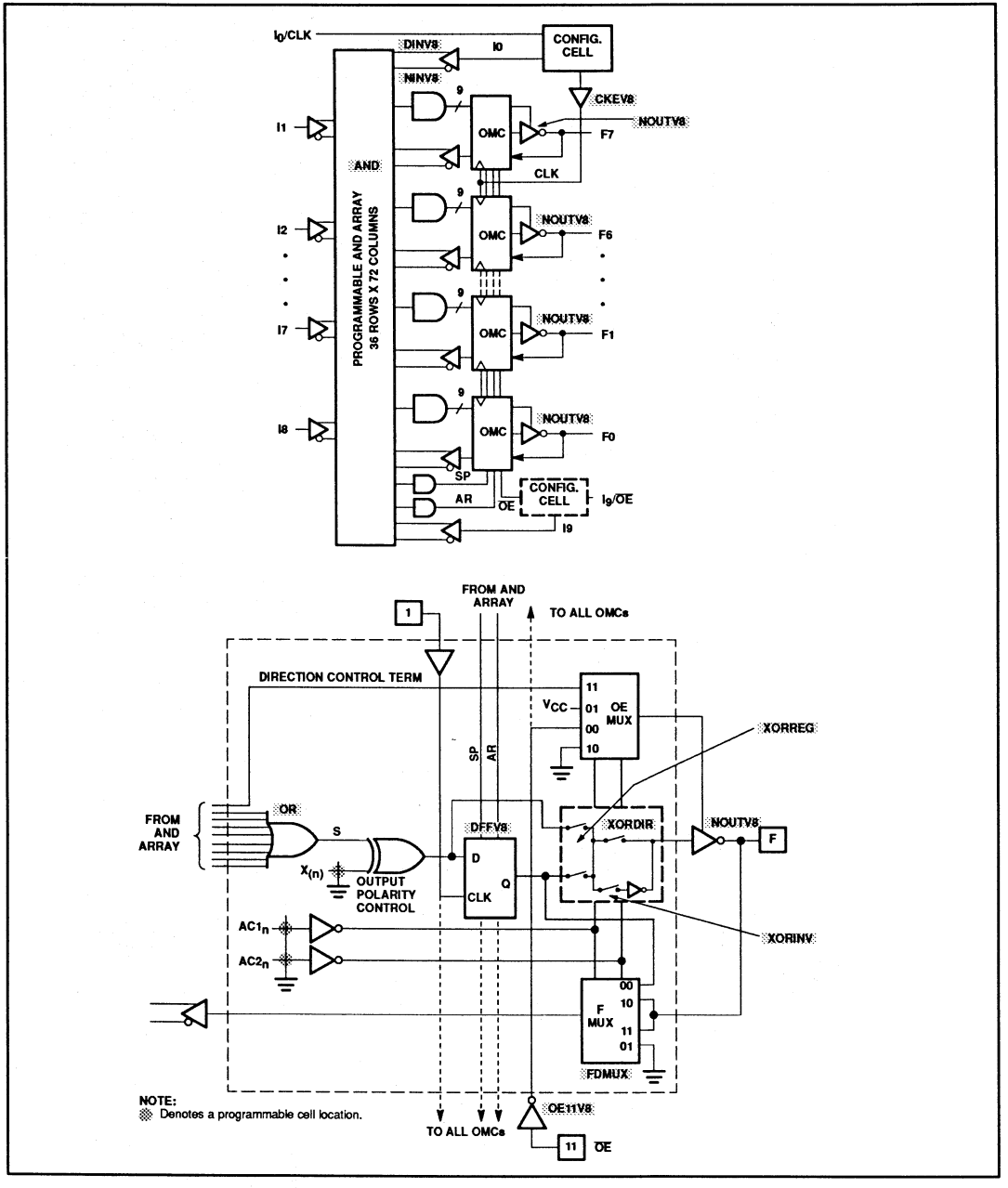
AND ARRAY	
INACTIVE	0
I, F (I, B)	H
I, F (I, B)	L
**DON'T CARE	–

CONTROL			
OMC ARCH.		OUTPUT POLARITY	
REGISTERED (D-TYPE)	D	NON-INVERTING	H
FIXED INPUT	I	INVERTING	L
FIXED OUTPUT	O	CONFIG. CELL*	
BIDIRECTIONAL I/O	B	PIN 1 = CLK; PIN 11 = $\overline{OE}$	L
		PIN 1, PIN 11 = INPUT	H

OR ARRAY (FIXED)	
DATA CANNOT BE ENTERED INTO THE OR ARRAY FIELD DUE TO THE FIXED NATURE OF THE DEVICE ARCHITECTURE.	
DIRECTION CONTROL	D
ACTIVE OUTPUT	A
NOT USED	

* THE CONFIGURATION CELL IS AUTOMATICALLY PROGRAMMED BASED ON THE OMC ARCHITECTURE.
** FOR SP, AR: "–" IS NOT ALLOWED.

SNAP RESOURCE SUMMARY DESIGNATIONS



PAL devices 16L8, 16R8, 16R6, 16R4

PLUS16R8D/-7 SERIES

FEATURES

- Ultra high-speed
  - t_{PD} = 7.5ns and f_{MAX} = 74MHz for the PLUS16R8-7 Series
  - t_{PD} = 10ns and f_{MAX} = 60 MHz for the PLUS16R8D Series
- 100% functionally and pin-for-pin compatible with industry standard 20-pin PAL® ICs
- Power-up reset function to enhance state machine design and testability
- Design support provided via SLICE and other CAD tools for Series 20 PAL devices
- Field-programmable on industry standard programmers
- Security fuse
- Individual 3-State control of all outputs

DESCRIPTION

The Signetics PLUS16XX family consists of ultra high-speed 7.5ns and 10ns versions of Series 20 PAL devices.

The PLUS16XX family is 100% functional and pin-compatible with the 16L8, 16R8, 16R6, and 16R4 Series devices.

The sum of products (AND-OR) architecture is comprised of 64 programmable AND gates and 8 fixed OR gates. Multiple bidirectional pins provide variable input/output pin ratios. Individual 3-State control of all outputs and registers with feedback (R8, R6, R4) is also provided. Proprietary designs can be protected by programming the security fuse.

The PLUS16R8, R6, and R4 have D-type flip-flops which are loaded on the Low-to-High transition of the clock input.

In order to facilitate state machine design and testing, a power-up reset function has been incorporated into these devices to reset all internal registers to Active-Low after a specific period of time.

The Signetics State-of-the-Art oxide isolation Bipolar fabrication process is employed to achieve high-performance operation.

The PLUS16XX family of devices are field programmable, enabling the user to quickly generate custom patterns using standard programming equipment. See the programmer chart for qualified programmers.

The SLICE software package from Signetics supports easy design entry for the PLUS16XX series as well as other PLD devices from Signetics. The PLUS16XX series are also supported by other standard CAD tools for PAL-type devices.

Order codes are listed in the Ordering Information table.

DEVICE NUMBER	DEDICATED INPUTS	COMBINATORIAL OUTPUTS	REGISTERED OUTPUTS
PLUS16L8	10	8 (6 I/O)	0
PLUS16R8	8	0	8
PLUS16R6	8	2 I/O	6
PLUS16R4	8	4 I/O	4

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
20-Pin Plastic Dual-In-Line 300mil-wide	PLUS16R8DN PLUS16R6DN PLUS16R4DN PLUS16L8DN PLUS16R8–7N PLUS16R6–7N PLUS16R4–7N PLUS16L8–7N
20-Pin Plastic Leaded Chip Carrier (PLCC)	PLUS16R8DA PLUS16R6DA PLUS16R4DA PLUS16L8DA PLUS16R8–7A PLUS16R6–7A PLUS16R4–7A PLUS16L8–7A

NOTE:
The PLUS16XX series of devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information, consult the Signetics Military Data Book.

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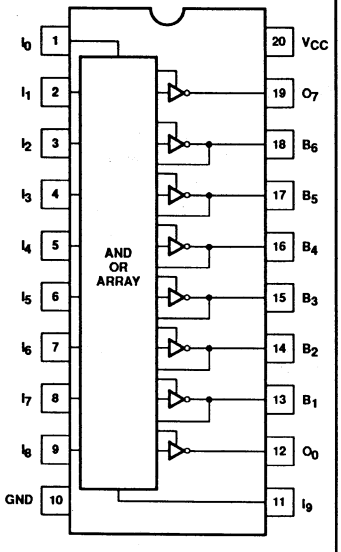
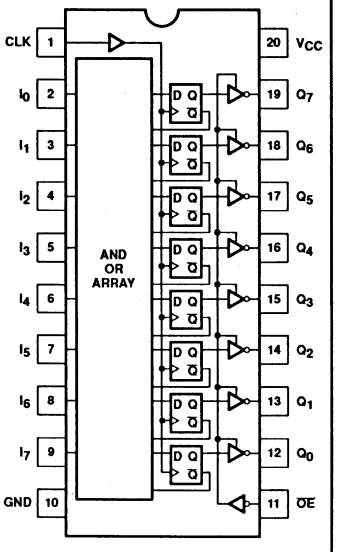
PIN CONFIGURATIONS

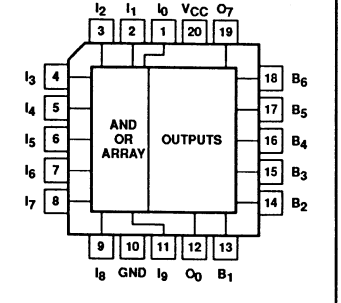
PLUS16L8



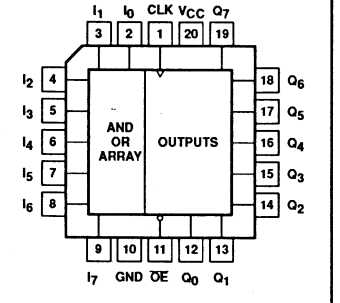
PLUS16R8



PLUS16L8



PLUS16R8

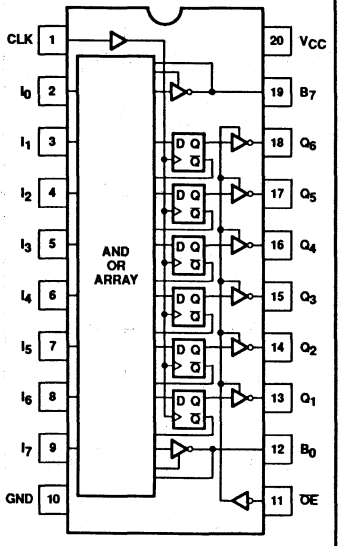


SYMBOL	DESCRIPTION
I	Dedicated Input
O	Dedicated combinatorial Output
Q	Registered output
B	Bidirectional (input/output)
CLK	Clock input
$\overline{OE}$	Output Enable
V_{CC}	Supply Voltage
GND	Ground

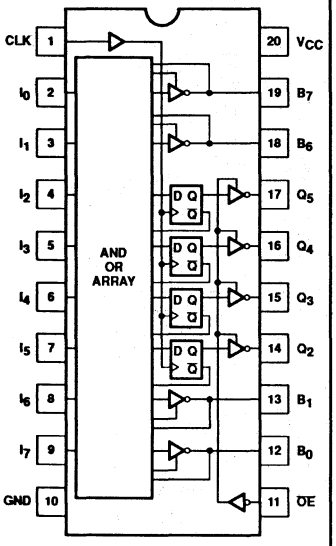
SYMBOL	DESCRIPTION
I	Dedicated Input
O	Dedicated combinatorial Output
Q	Registered output
B	Bidirectional (input/output)
CLK	Clock input
$\overline{OE}$	Output Enable
V_{CC}	Supply Voltage
GND	Ground

PIN CONFIGURATIONS

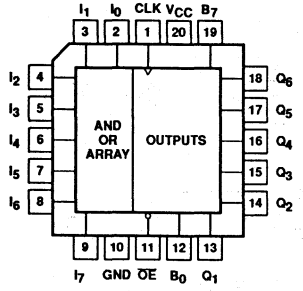
PLUS16R6



PLUS16R4

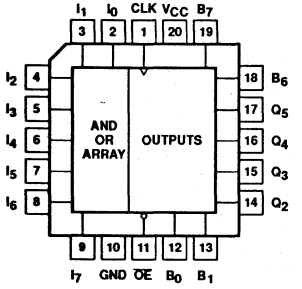


PLUS16R6



SYMBOL	DESCRIPTION
I	Dedicated Input
O	Dedicated combinatorial Output
Q	Registered output
B	Bidirectional (input/output)
CLK	Clock input
$\overline{OE}$	Output Enable
V_{CC}	Supply Voltage
GND	Ground

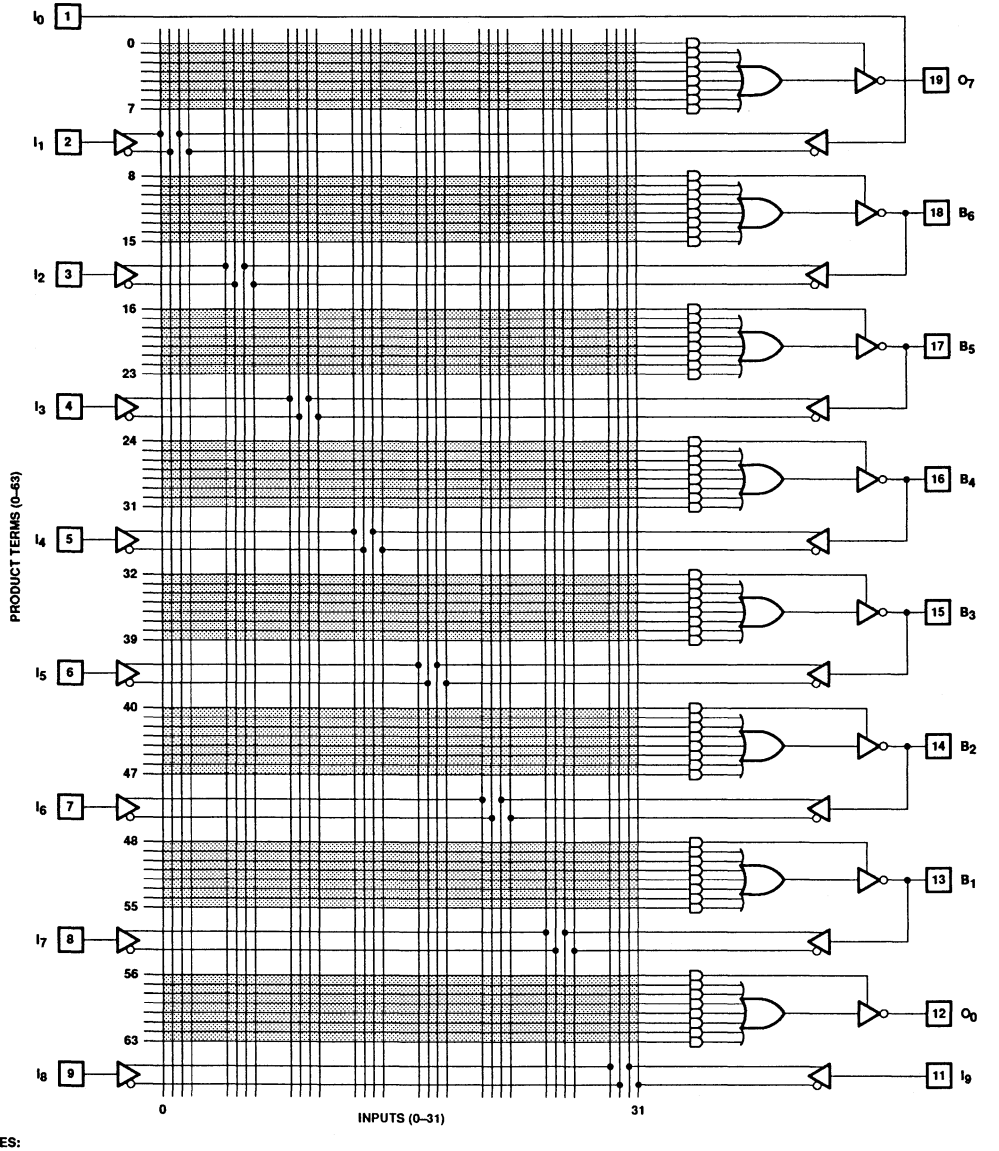
PLUS16R4



SYMBOL	DESCRIPTION
I	Dedicated Input
O	Dedicated combinatorial Output
Q	Registered output
B	Bidirectional (input/output)
CLK	Clock input
$\overline{OE}$	Output Enable
V_{CC}	Supply Voltage
GND	Ground

LOGIC DIAGRAM

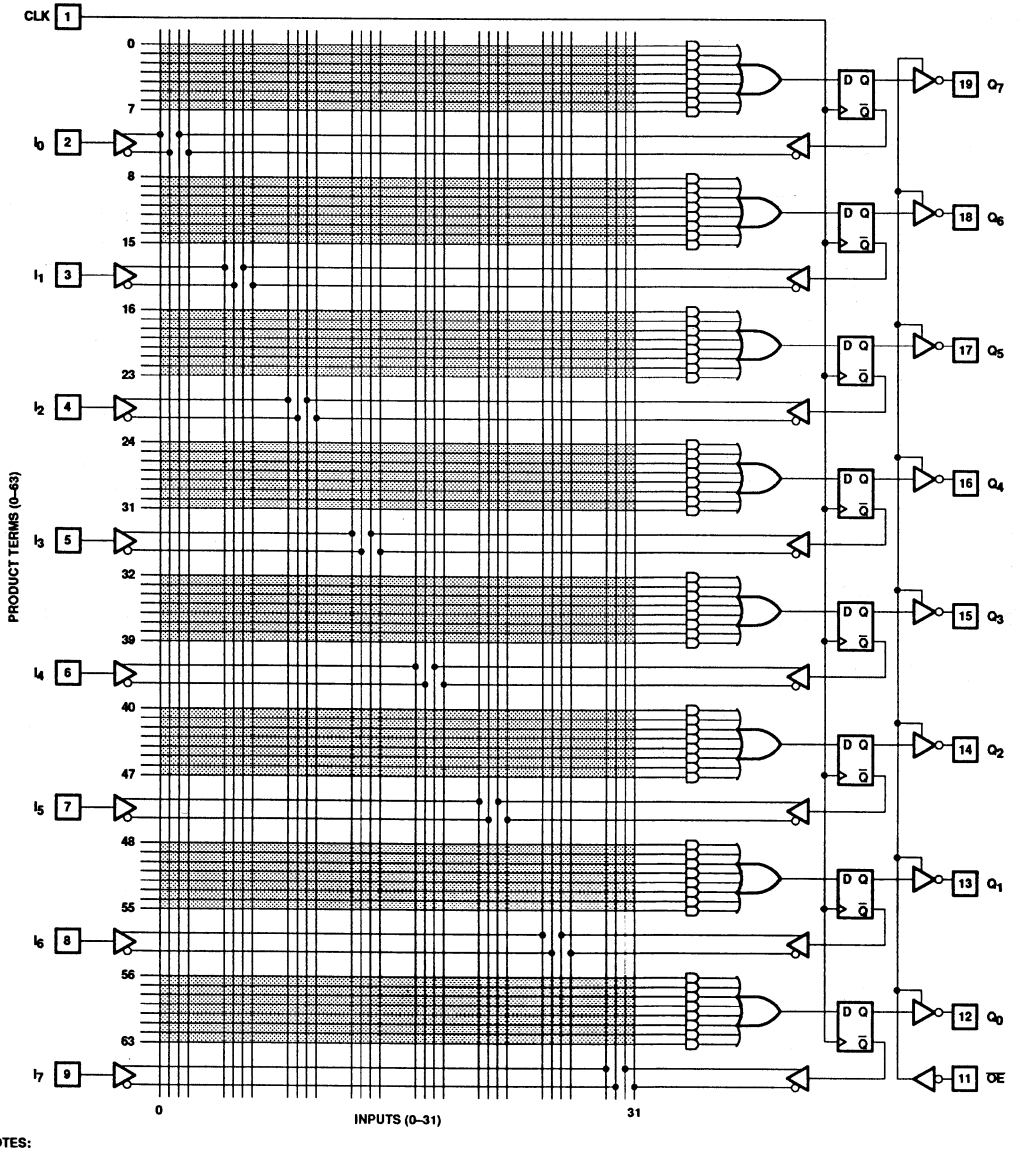
PLUS16L8



NOTES:
1. All unprogrammed or virgin "AND" gate locations are pulled to logic "0".
2. ▒ Programmable connections.

LOGIC DIAGRAM

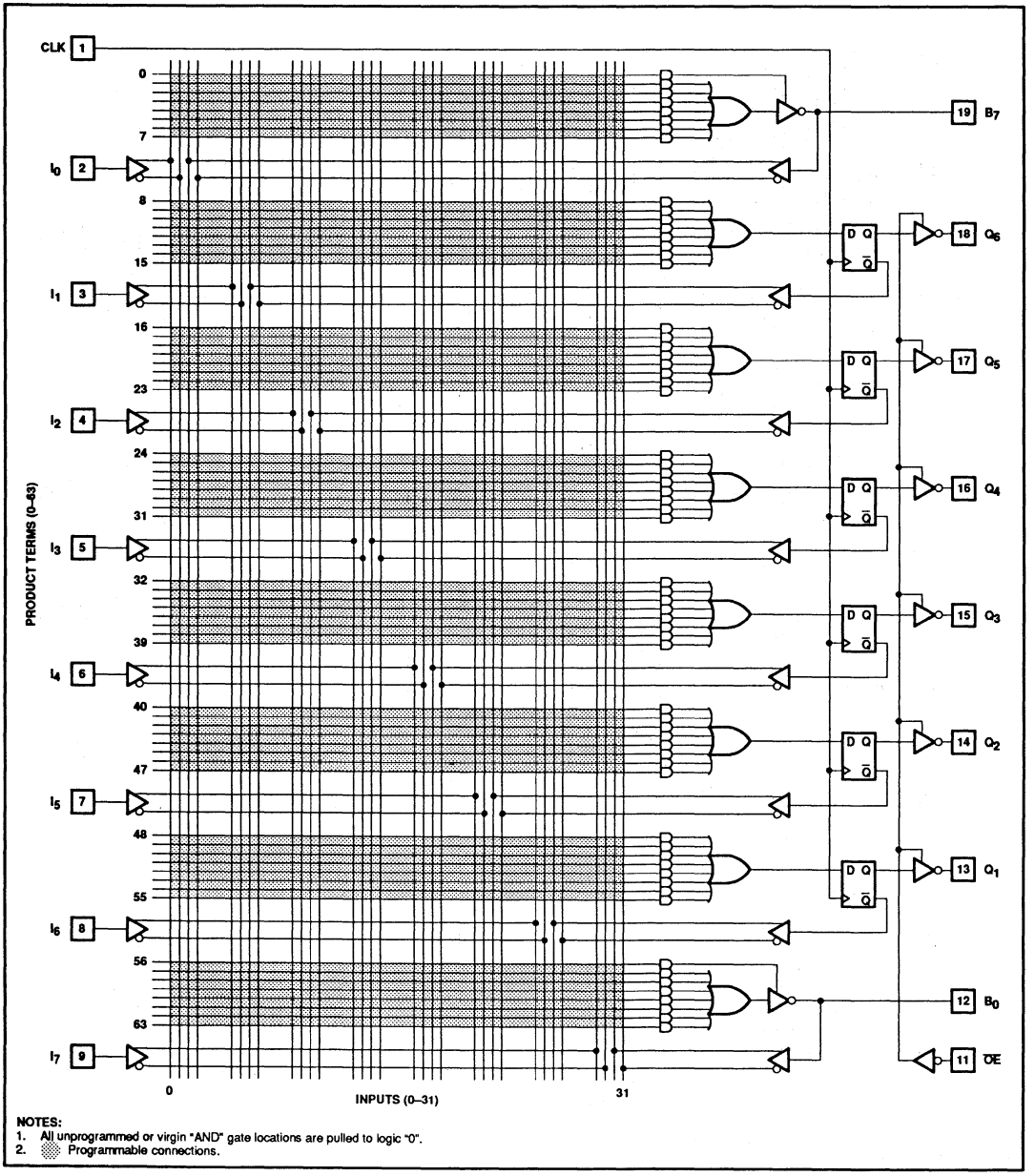
PLUS16R8



NOTES:
1. All unprogrammed or virgin "AND" gate locations are pulled to logic "0".
2. ▒ Programmable connections.

LOGIC DIAGRAM

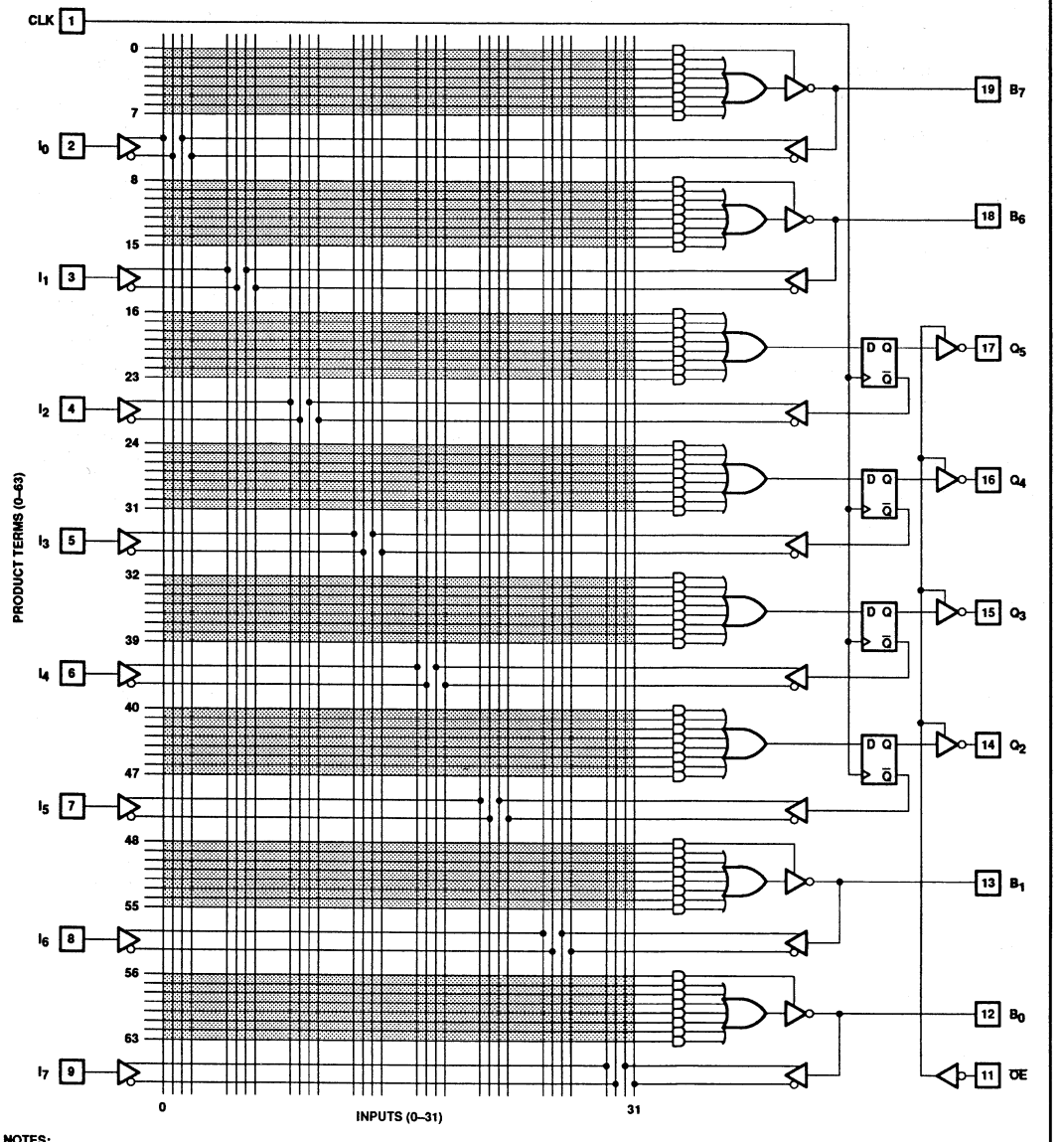
PLUS16R6



NOTES:
1. All unprogrammed or virgin "AND" gate locations are pulled to logic "0".
2. ▒ Programmable connections.

LOGIC DIAGRAM

PLUS16R4



NOTES:
1. All unprogrammed or virgin "AND" gate locations are pulled to logic "0".
2. ▒ Programmable connections.

FUNCTIONAL DESCRIPTIONS

The PLUS16XX series utilizes the familiar sum-of-products implementation consisting of a programmable AND array and a fixed OR array. These devices are capable of replacing an equivalent of four or more SSI/MSI integrated circuits to reduce package count and board area occupancy, consequently improving reliability and design cycle over Standard Cell or gate array options. By programming the security fuse, proprietary designs can be protected from duplication.

The PLUS16XX series consists of four PAL-type devices. Depending on the particular device type, there are a variable number of combinatorial and registered outputs available to the designer. The PLUS16L8 is a combinatorial part with 8 user configurable outputs (6 bidirectional), while the other three devices, PLUS16R8, PLUS16R6, PLUS16R4, have respectively 8, 6, and 4 output registers.

3-State Outputs

The PLUS16XX series devices also feature 3-State output buffers on each output pin which can be programmed for individual control of all outputs. The registered outputs (Qn) are controlled by an external input (/OE), and the combinatorial outputs (On, Bn) use a product term to control the enable function.

Programmable Bidirectional Pins

The PLUS16XX products feature variable Input/Output ratios. In addition to 8 dedicated inputs, each combinatorial output pin of the registered devices can be individually programmed as an input or output. The PLUS16L8 provides 10 dedicated inputs and 6 Bidirectional I/O lines that can be individually configured as inputs or outputs.

Output Registers

The PLUS16R8 has 8 output registers, the 16R6 has 6, and the 16R4 has 4. Each output register is a D-type flip-flop which is loaded on the Low-to-High transition of the clock input. These output registers are capable of feeding the outputs of the registers back into the array to facilitate design of synchronous state machines.

Power-up Reset

By resetting all flip-flops to a logic Low, as the power is turned on, the PLUS16R8, R6, R4 enhance state machine design and initialization capability.

Software Support

Like other Programmable Logic Devices from Signetics, the PLUS16XX series are supported by SLICE, the PC-based software development tool from Signetics. The PLUS16XX family of devices are also supported by standard CAD tools for PAL devices, including ABEL and CUPL.

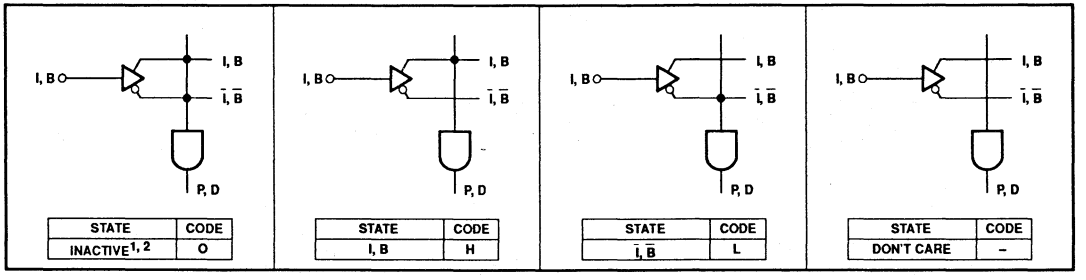
SLICE is available free of charge to qualified users.

Logic Programming

The PLUS16XX series is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Signetics SLICE and SNAP design software packages. ABEL™ CUPL™ and PALASM® 90 design software packages also support the PLUS16XX architecture.

All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

AND ARRAY – (I, B)



STATE	CODE
INACTIVE[1, 2]	O

STATE	CODE
I, B	H

STATE	CODE
$\overline{I}$, $\overline{B}$	L

STATE	CODE
DON'T CARE	–

VIRGIN STATE

A factory shipped virgin device contains all fusible links intact, such that:

1. All outputs are at "H" polarity.
2. All P_n terms are disabled.
3. All P_n terms are active on all outputs.

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CUPL is a trademark of Logical Devices, Inc.
PALASM is a registered trademark of AMD Corp.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS		UNIT
		MIN	MAX	
V_{CC}	Supply voltage	–0.5	+7	V_{DC}
V_{IN}	Input voltage	–1.2	+8.0	V_{DC}
V_{OUT}	Output voltage	–0.5	V_{CC} + 0.5V	V_{DC}
I_{IN}	Input currents	–30	+30	mA
I_{OUT}	Output currents		+100	mA
T_{stg}	Storage temperature range	–65	+150	°C

NOTE:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

OPERATING RANGES

SYMBOL	PARAMETER	RATINGS		UNIT
		MIN	MAX	
V_{CC}	Supply voltage	+4.75	+5.25	V_{DC}
T_{amb}	Operating free–air temperature	0	+75	°C

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

DC ELECTRICAL CHARACTERISTICS

$0°C \leq T_{amb} \leq +75°C$, $4.75 \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[1]	MAX	
Input voltage[2]						
V_{IL}	Low	V_{CC} = MIN			0.8	V
V_{IH}	High	V_{CC} = MAX	2.0			V
V_{IC}	Clamp	V_{CC} = MIN, I_{IN} = –18mA		–0.8	–1.5	V
Output voltage						
		V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}				
V_{OL}	Low	I_{OL} = 24mA			0.5	V
V_{OH}	High	I_{OH} = –3.2 mA	2.4			V
Input current						
		V_{CC} = MAX				
I_{IL}	Low[3]	V_{IN} = 0.40V			–250	µA
I_{IH}	High[3]	V_{IN} = 2.7V			25	µA
I_I	Maximum input current	V_{IN} = V_{CC} = V_{CCMAX}			100	µA
Output current						
		V_{CC} = MAX				
I_{OZH}	Output leakage	V_{OUT} = 2.7V			100	µA
I_{OZL}	Output leakage	V_{OUT} = 0.4V			–100	µA
I_{OS}	Short circuit[4, 5]	V_{OUT} = 0V	–30		–90	mA
I_{CC}	V_{CC} supply current	V_{CC} = MAX		160	180	mA
Capacitance[6]						
C_{IN}	Input	V_{CC} = 5V				
		V_{OUT} = 2.0V		8		pF
C_B	I/O (B)	V_{OUT} = 2V, f = 1MHz		8		pF

NOTES:
1. All typical values are at V_{CC} = 5V, T_{amb} = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Leakage current for bidirectional pins is the worst case of I_{IL} and I_{OZL} or I_{IH} and I_{OZH}.
4. Test one at a time.
5. Duration of short circuit should not exceed 1 second.
6. These parameters are not 100% tested but periodically sampled.

AC ELECTRICAL CHARACTERISTICS

$R_1 = 200\Omega$, $R_2 = 390\Omega$, $0°C \le T_{amb} \le +75°C$, $4.75 \le V_{CC} \le 5.25V$

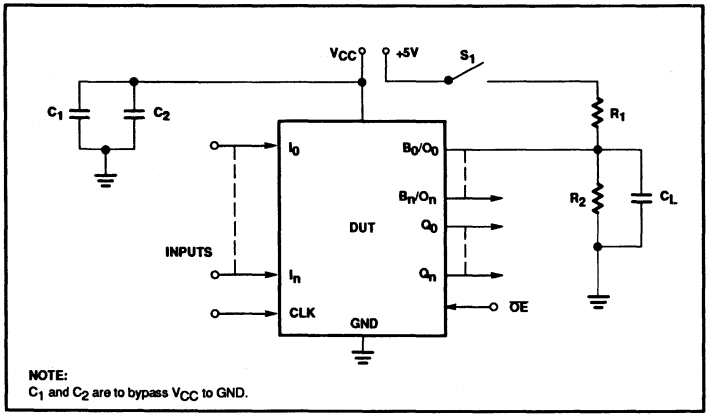
SYMBOL	PARAMETER	FROM	TO	LIMITS					UNIT
				-7			D		
				MIN[1]	TYP	MAX	MIN[1]	MAX	
Pulse Width									
t_{CKH}	Clock High	CK+	CK–	5			7		ns
t_{CKL}	Clock Low	CK–	CK+	5			7		ns
t_{CKP}	Period	CK+	CK+	10			14		ns
Setup & Hold time									
t_{IS}	Input	Input or feedback	CK+	7			9		ns
t_{IH}	Input	CK+	Input or feedback	0			0		ns
Propagation delay									
t_{CKO}	Clock	CK±	Q±	3		6.5	3	7.5	ns
t_{CKF}	Clock[3]	CK±	$\overline{Q}$			3		6.5	ns
t_{PD}	Output (16L8, R6, R4)[2]	I, B	Output	3		7.5	3	10	ns
t_{OE1}	Output enable[4]	$\overline{OE}$	Output enable	3		8	3	10	ns
t_{OE2}	Output enable[4,5]	I	Output enable	3		10	3	10	ns
t_{OD1}	Output disable[4]	$\overline{OE}$	Output disable	3		8	3	10	ns
t_{OD2}	Output disable[4,5]	I	Output disable	3		10	3	10	ns
t_{SKW}	Output	Q	Q			1		1	ns
t_{PPR}	Power-Up Reset	V_{CC}+	Q+			10		10	ns
Frequency (16R8, R6, R4)									
f_{MAX}	No feedback 1/ $(t_{CKL} + t_{CKH})$[6]				100		71.4		MHz
	Internal feedback 1/ $(t_{IS} + t_{CKF})$[6]				90		64.5		MHz
	External feedback 1/ $(t_{IS} + t_{CKO})$[6]				74		60.6		MHz

* For definitions of the terms, please refer to the Timing/Frequency Definitions tables.

NOTES:

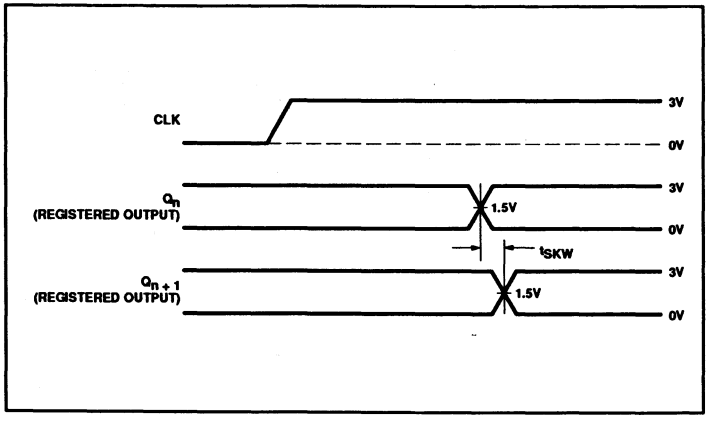
1. CL = 0pF while measuring minimum output delays.
2. t_{PD} test conditions: CL = 50pF (with jig and scope capacitance), $V_{IH} = 3V$, $V_{IL} = 0V$, $V_{OH} = V_{OL} = 1.5V$.
3. t_{CKF} was calculated from measured Internal f_{MAX}.
4. For 3-State output; output enable times are tested with $C_L = 50pF$ to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with $C_L = 5pF$. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} - 0.5V)$ with S_1 open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with S_1 closed.
5. Same function as t_{OE1} and t_{OD1}, with the difference of using product term control.
6. Not 100% tested, but calculated at initial characterization and at any time a modification in design takes place which may affect the frequency.

TEST LOAD CIRCUIT

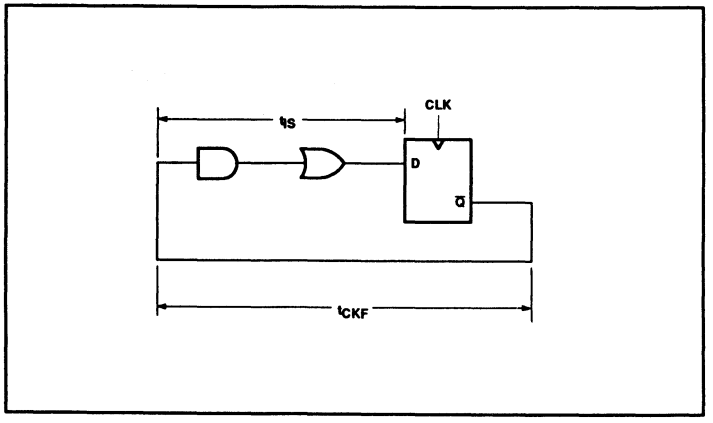


NOTE:
C_1 and C_2 are to bypass V_{CC} to GND.

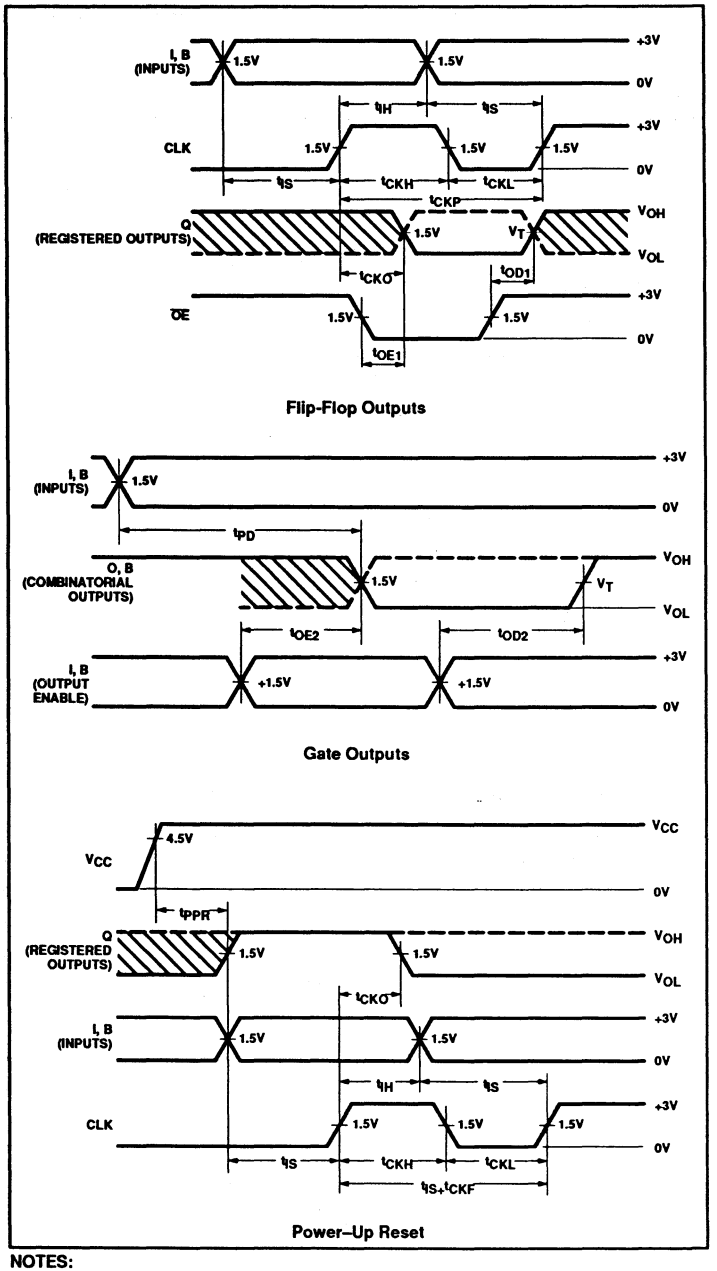
OUTPUT REGISTER SKEW



CLOCK TO FEEDBACK PATH



TIMING DIAGRAMS[1, 2]



TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{CKH}	Width of input clock pulse.
t_{CKL}	Interval between clock pulses.
t_{CKP}	Clock period.
t_{IS}	Required delay between beginning of valid input and positive transition of clock.
t_{IH}	Required delay between positive transition of clock and end of valid input data.
t_{CKF}	Delay between positive transition of clock and when internal $\overline{Q}$ output of flip-flop becomes valid.
t_{CKO}	Delay between positive transition of clock and when outputs become valid (with $\overline{OE}$ Low).
t_{OE1}	Delay between beginning of Output Enable Low and when outputs become valid.
t_{OD1}	Delay between beginning of Output Enable High and when outputs are in the Off-State.
t_{OE2}	Delay between predefined Output Enable High, and when combinational outputs become valid.
t_{OD2}	Delay between predefined Output Enable Low and when combinational outputs are in the Off-State.
t_{PPR}	Delay between V_{CC} (after power-on) and when flip-flop outputs become preset at "1" (internal Q outputs at "0").
t_{PD}	Propagation delay between combinational inputs and outputs.

FREQUENCY DEFINITIONS

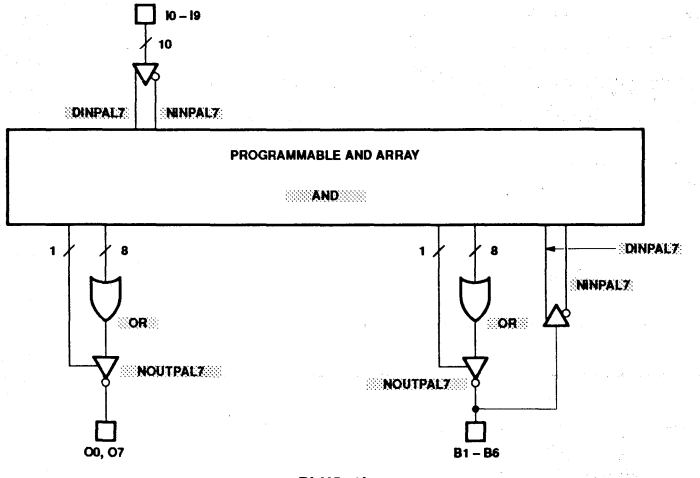
f_{MAX}	**No feedback:** Determined by the minimum clock period, $1/(t_{CKL} + t_{CKH})$. **Internal feedback:** Determined by the internal delay from flip-flop outputs through the internal feedback and array to the flip-flop inputs, $1/(t_{IS} + t_{CKF})$. **External feedback:** Determined by clock-to-output delay and input setup time, $1/(t_{IS} + t_{CKO})$.

NOTES:
1. Input pulse amplitude is 0V to 3V.
2. Input rise and fall times are 2.5ns.

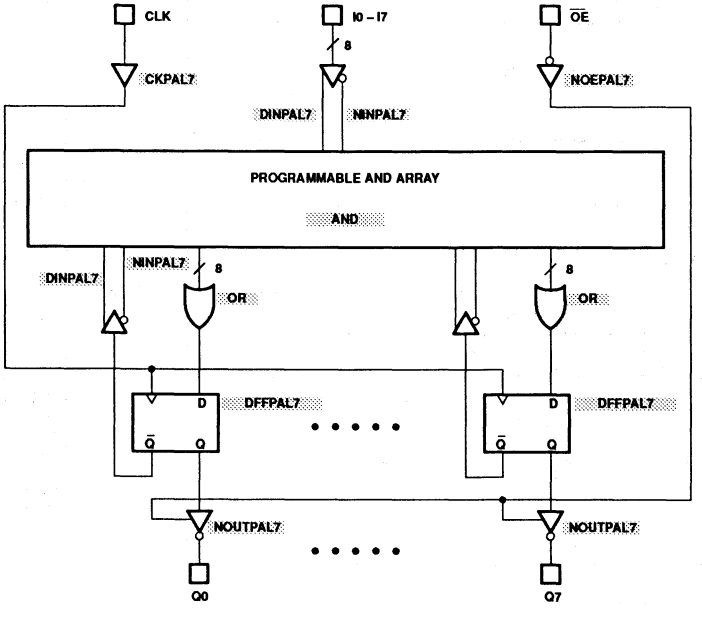
PROGRAMMING/SOFTWARE

Refer to Section 8 (*Development Software*) and Section 9 (*Third-Party Programmer/Software Support*) of this data handbook for additional information.

SNAP RESOURCE SUMMARY DESIGNATIONS

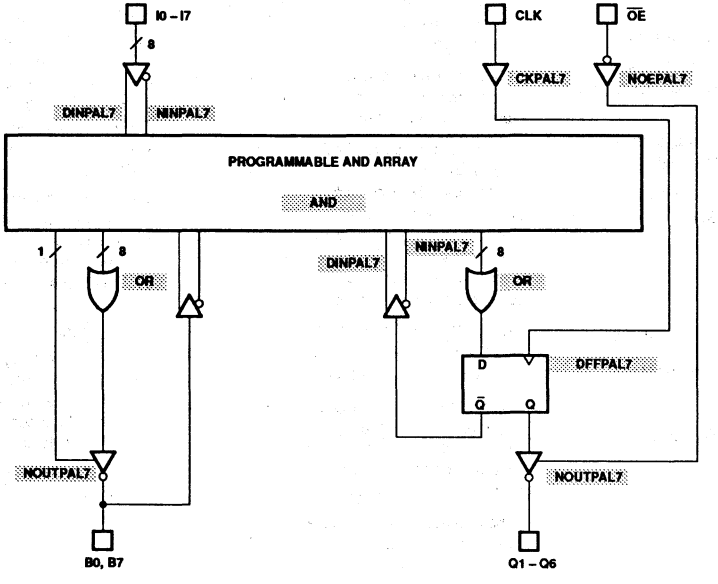


PLUS16L8

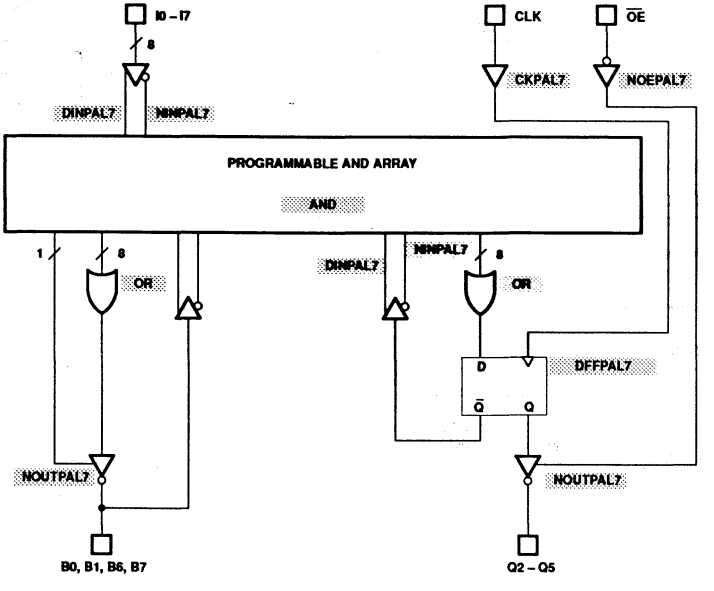


PLUS16R8

SNAP RESOURCE SUMMARY DESIGNATIONS (Continued)



PLUS16R6



PLUS16R4

PAL devices
16L8, 16R8, 16R6, 16R4

PLQ16R8-5 SERIES

FEATURES

- Ultra high-speed
  - t_{PD} = 5ns and f_{MAX} = 118MHz
- 100% functionally and pin-for-pin compatible with industry standard 20-pin PAL® ICs
- Power-up reset function to enhance state machine design and testability
- Design support provided via SLICE and other CAD tools for Series 20 PAL devices
- Field-programmable on industry standard programmers
- Security fuse
- Individual 3-State control of all outputs
- Register Preload for testability
- Power-up 3-State
- 20-Pin DIP and 20-Pin PLCC

DESCRIPTION

The Signetics PLQ16XX family consists of ultra high-speed 5ns versions of Series 20 PAL devices.

The PLQ16XX family is 100% functional and pin-compatible with the 16L8, 16R8, 16R6, and 16R4 Series devices.

The sum of products (AND-OR) architecture is comprised of 64 programmable AND gates and 8 fixed OR gates. Multiple bidirectional pins provide variable input/output pin ratios. Individual 3-State control of all outputs and registers with feedback (R8, R6, R4) is also provided. Proprietary designs can be protected by programming the security fuse.

The PLQ16R8, R6, and R4 have D-type flip-flops which are loaded on the Low-to-High transition of the clock input.

In order to facilitate state machine design and testing, a power-up reset function has been incorporated into these devices to reset all internal registers to active-Low after a specific period of time.

The Signetics State-of-the-Art BiCMOS process, known as QUBiC, has been employed to achieve higher levels of operating performance for the PLQ16XX family of PLDs. The QUBiC transistors have been optimized to provide two-thirds more speed at less than half the power consumed from products using our last generation of bipolar technology. QUBiC reduces on-chip delays and provides high output drive currents while consuming power at very low levels.

The PLQ16XX family of devices are field programmable, enabling the user to quickly generate custom patterns using standard programming equipment. See the programmer section for qualified programmers.

The SLICE software package from Signetics supports easy design entry for the PLQ16XX series as well as other PLD devices from Signetics. The PLQ16XX series are also supported by other standard CAD tools for PAL-type devices.

Order codes are listed in the Ordering Information table.

DEVICE NUMBER	DEDICATED INPUTS	COMBINATORIAL OUTPUTS	REGISTERED OUTPUTS
PLQ16L8	10	8 (6 I/O)	0
PLQ16R8	8	0	8
PLQ16R6	8	2 I/O	6
PLQ16R4	8	4 I/O	4

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
20-Pin Plastic Dual-In-Line 300mil-wide	PLQ16R8–5N PLQ16R6–5N PLQ16R4–5N PLQ16L8–5N
20-Pin Plastic Leaded Chip Carrier (PLCC)	PLQ16R8–5A PLQ16R6–5A PLQ16R4–5A PLQ16L8–5A

NOTE:
The PLQ16XX series of devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information, consult the Signetics Military Data Handbook.

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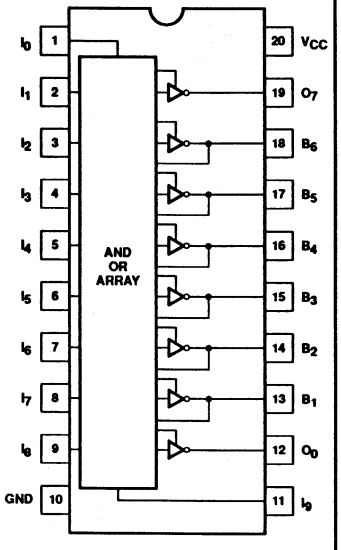
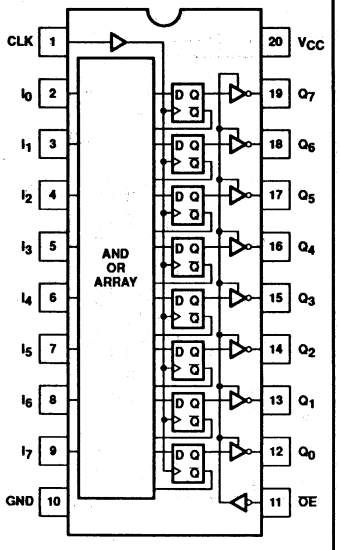
PIN CONFIGURATIONS

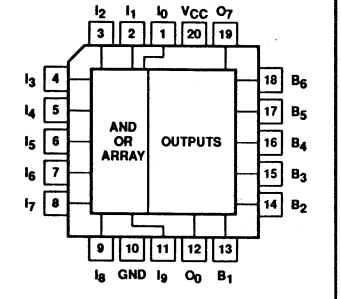
PLQ16L8



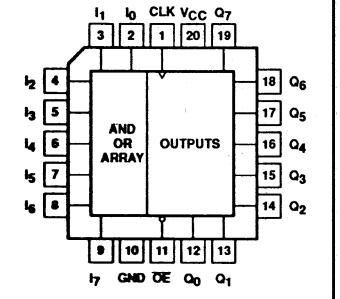
PLQ16R8



PLQ16L8



PLQ16R8

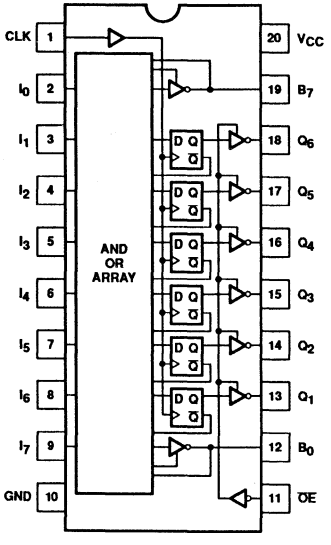


SYMBOL	DESCRIPTION
I	Dedicated Input
O	Dedicated combinatorial Output
Q	Registered output
B	Bidirectional (input/output)
CLK	Clock input
$\overline{OE}$	Output Enable
V_{CC}	Supply Voltage
GND	Ground

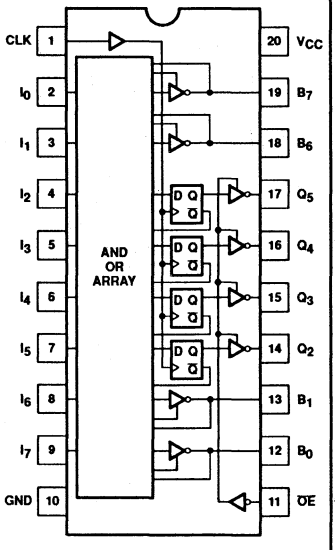
SYMBOL	DESCRIPTION
I	Dedicated Input
O	Dedicated combinatorial Output
Q	Registered output
B	Bidirectional (input/output)
CLK	Clock input
$\overline{OE}$	Output Enable
V_{CC}	Supply Voltage
GND	Ground

PIN CONFIGURATIONS

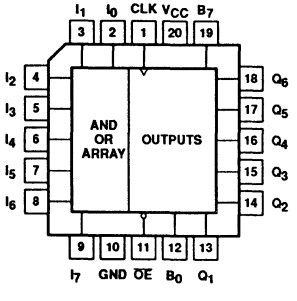
PLQ16R6



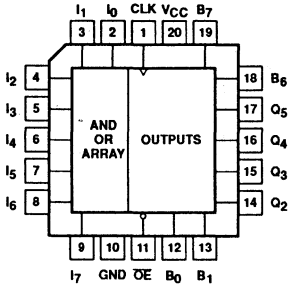
PLQ16R4



PLQ16R6



PLQ16R4



SYMBOL	DESCRIPTION
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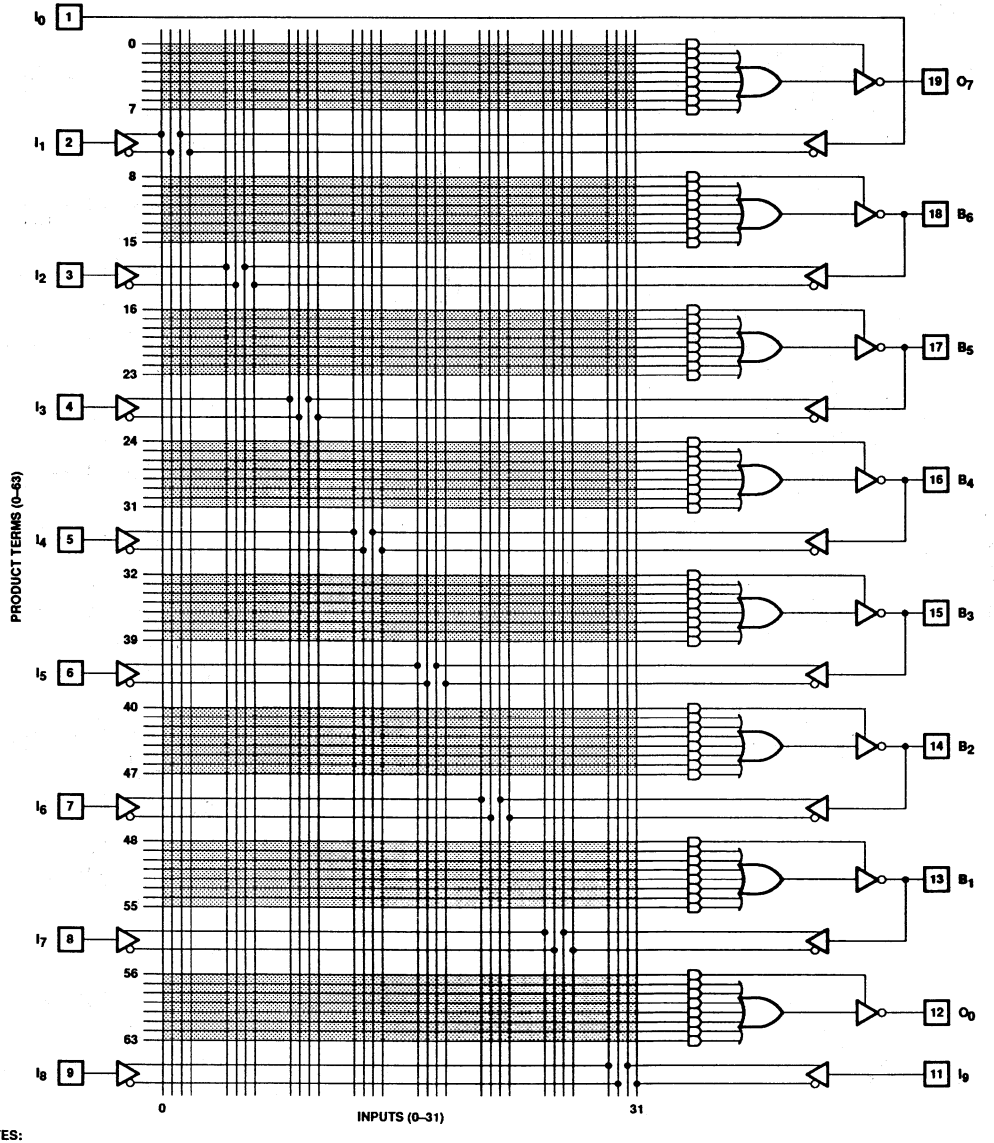
O	Dedicated combinatorial Output
Q	Registered output
B	Bidirectional (input/output)
CLK	Clock input
$\overline{OE}$	Output Enable
V_{CC}	Supply Voltage
GND	Ground

SYMBOL	DESCRIPTION
I	Dedicated Input
O	Dedicated combinatorial Output
Q	Registered output
B	Bidirectional (input/output)
CLK	Clock input
$\overline{OE}$	Output Enable
V_{CC}	Supply Voltage
GND	Ground

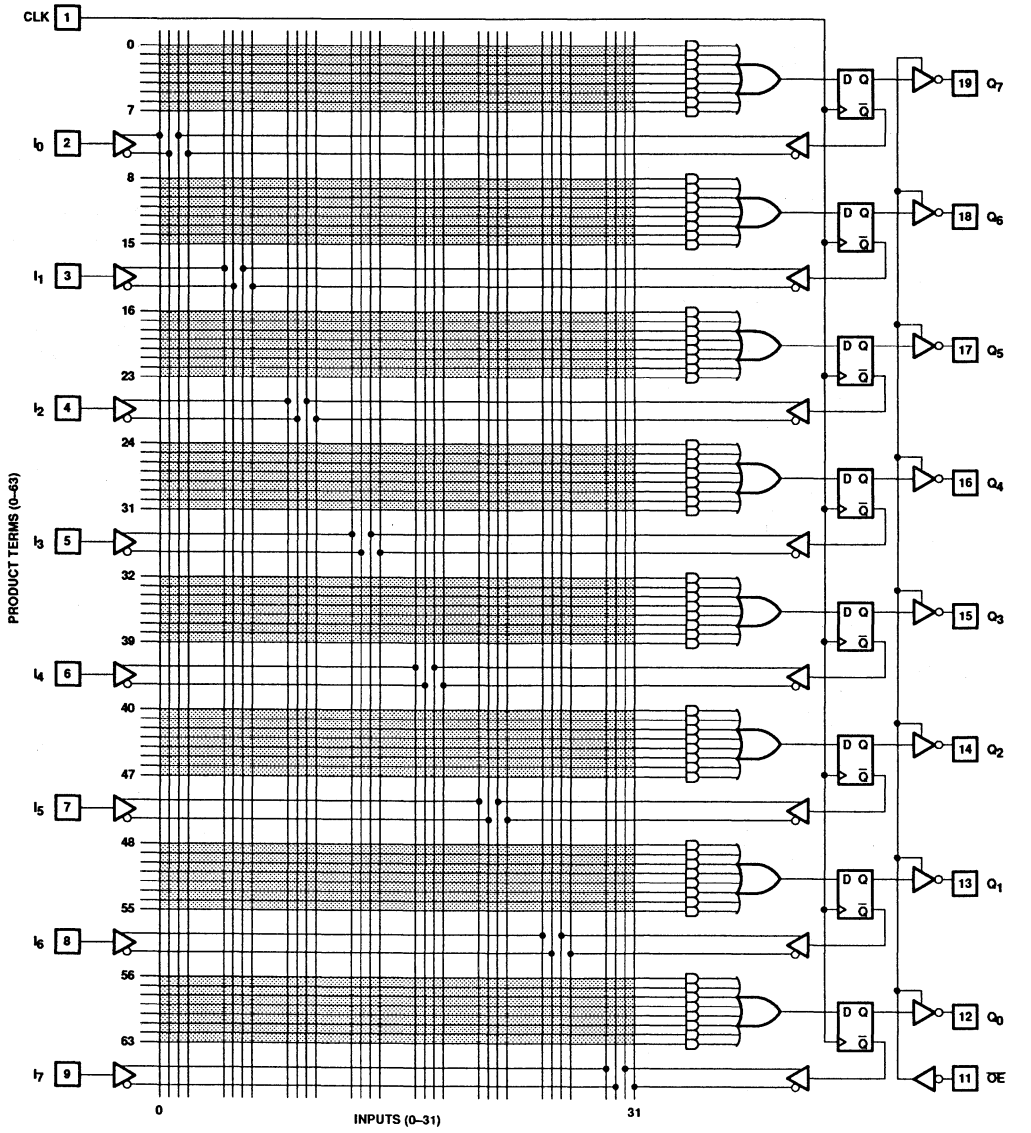
LOGIC DIAGRAM — PLQ16L8



NOTES:
1. All unprogrammed or virgin "AND" gate locations are pulled to logic "0".
2. ▒ Programmable connections.

LOGIC DIAGRAM

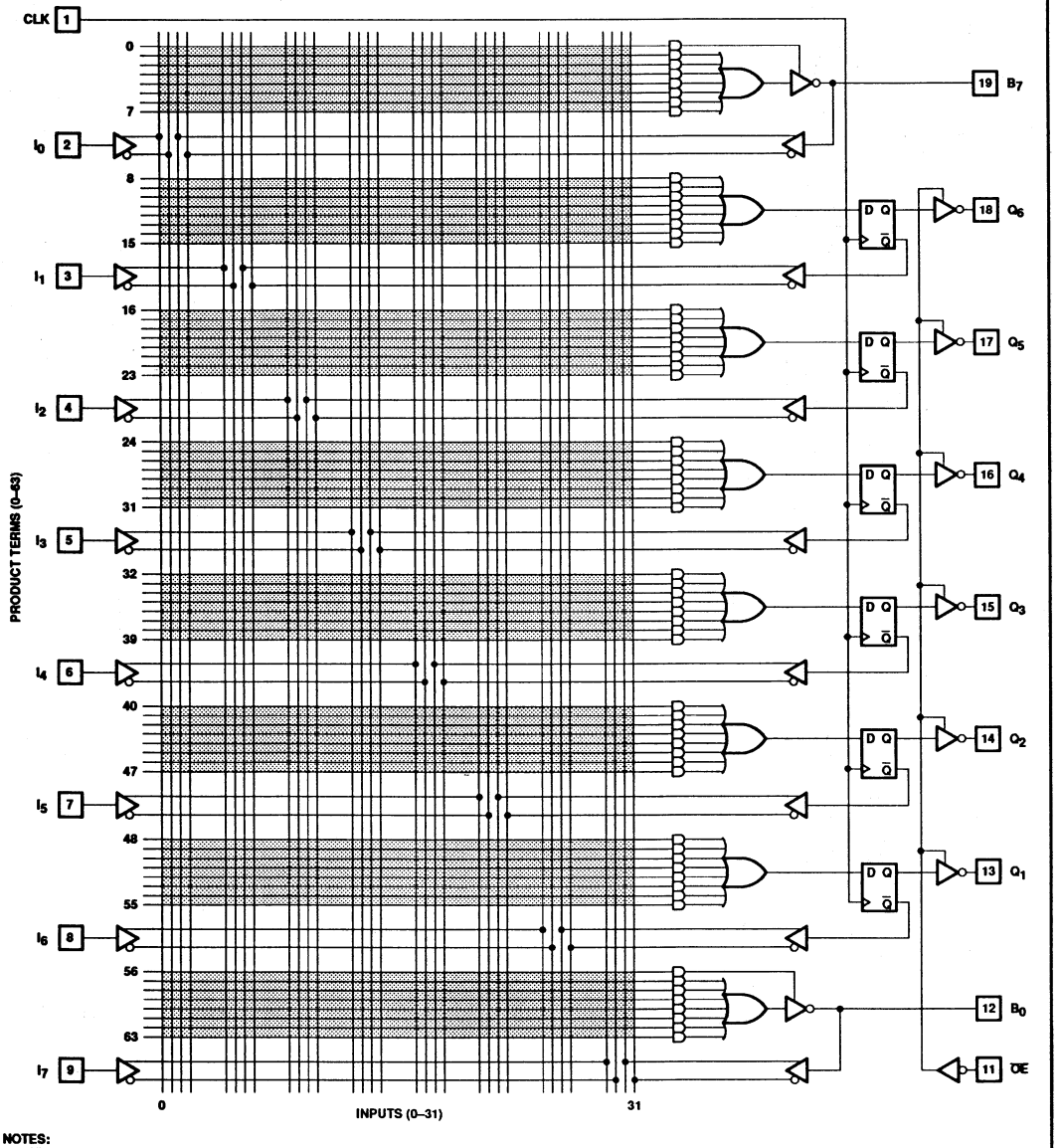
PLQ16R8



NOTES:
1. All unprogrammed or virgin "AND" gate locations are pulled to logic "0".
2. ▒ Programmable connections.

LOGIC DIAGRAM

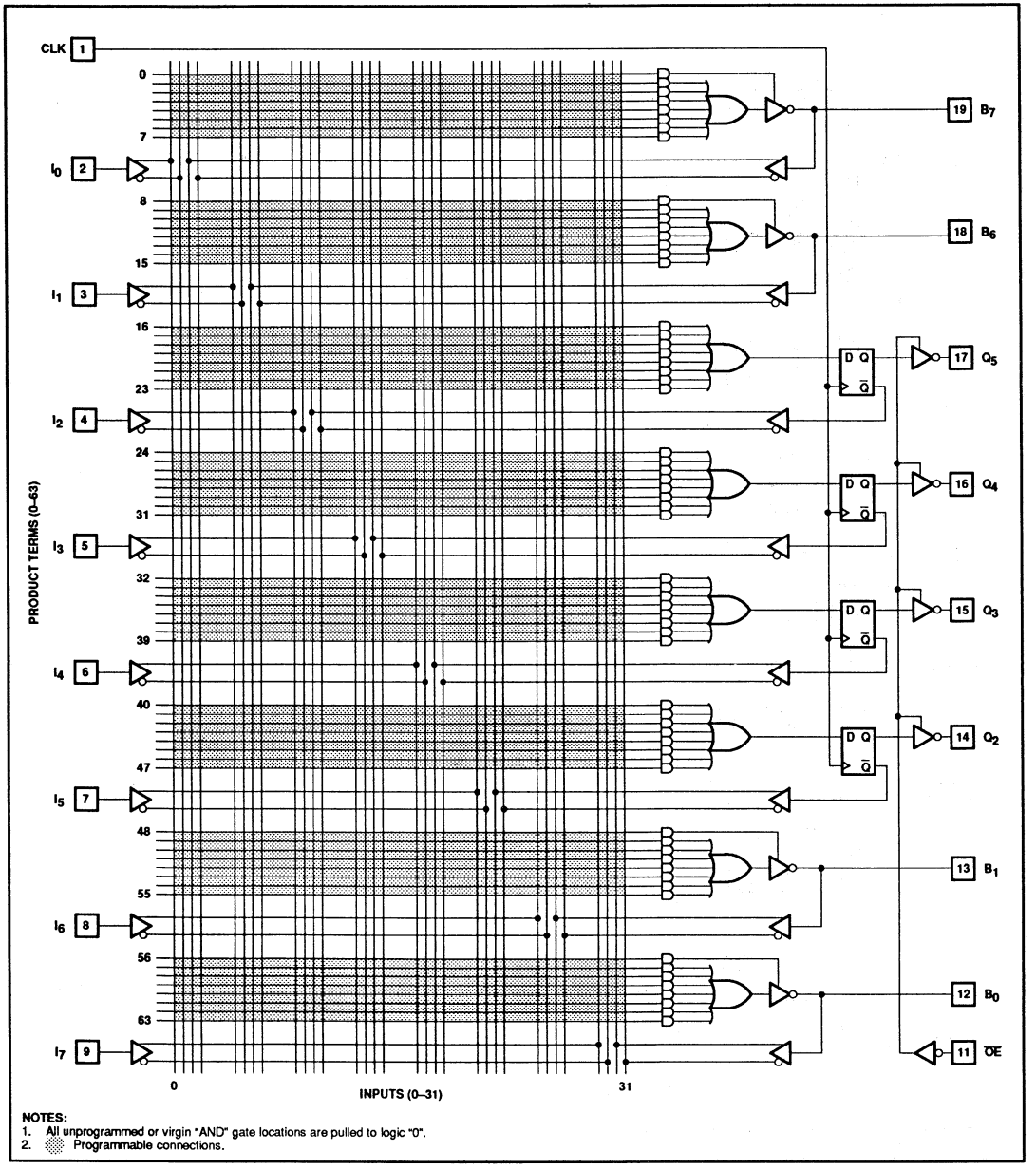
PLQ16R6



NOTES:
1. All unprogrammed or virgin "AND" gate locations are pulled to logic "0".
2. ▒ Programmable connections.

LOGIC DIAGRAM

PLQ16R4



NOTES:
1. All unprogrammed or virgin "AND" gate locations are pulled to logic "0".
2. ▒ Programmable connections.

FUNCTIONAL DESCRIPTIONS

The PLQ16XX series utilizes the familiar sum-of-products implementation consisting of a programmable AND array and a fixed OR array. These devices are capable of replacing an equivalent of four or more SSI/MSI integrated circuits to reduce package count and board area occupancy, consequently improving reliability and design cycle over Standard Cell or gate array options. By programming the security fuse, proprietary designs can be protected from duplication.

The PLQ16XX series consists of four PAL-type devices. Depending on the particular device type, there are a variable number of combinatorial and registered outputs available to the designer. The PLQ16L8 is a combinatorial part with 8 user configurable outputs (6 bidirectional), while the other three devices, PLQ16R8, PLQ16R6, PLQ16R4, have respectively 8, 6, and 4 output registers.

3-State Outputs

The PLQ16XX series devices also feature 3-State output buffers on each output pin which can be programmed for individual control of all outputs. The registered outputs (Qn) are controlled by an external input (/OE), and the combinatorial outputs (On, Bn) use a product term to control the enable function.

Programmable Bidirectional Pins

The PLQ16XX products feature variable Input/Output ratios. In addition to 8 dedicated inputs, each combinatorial output pin of the registered devices can be individually programmed as an input or output. The PLQ16L8 provides 10 dedicated inputs and 6 Bidirectional I/O lines that can be individually configured as inputs or outputs.

Output Registers

The PLQ16R8 has 8 output registers, the 16R6 has 6, and the 16R4 has 4. Each output register is a D-type flip-flop which is loaded on the Low-to-High transition of the clock input. These output registers are capable of feeding the outputs of the registers back into the array to facilitate design of synchronous state machines.

Power-up Reset

By resetting all flip-flops to a logic Low, as the power is turned on, the PLQ16R8, R6, R4 enhance state machine design and initialization capability.

Register Preload

Preload function allows the register to be loaded from the output pins. This feature allows functional testing of sequential patterns by loading output states.

Power-up 3-State

All outputs will be disabled when V_{CC} is 3.0V ± 20% (25°C). This special feature keeps outputs 3-Stated during power-up. Only when V_{CC} reaches its normal operating range will device function normally.

Software Support

Like other Programmable Logic Devices from Signetics, the PLQ16XX series are supported by SLICE, the PC-based software development tool from Signetics. The PLQ16XX family of devices are also supported by standard CAD tools for PAL devices, including ABEL and CUPL.

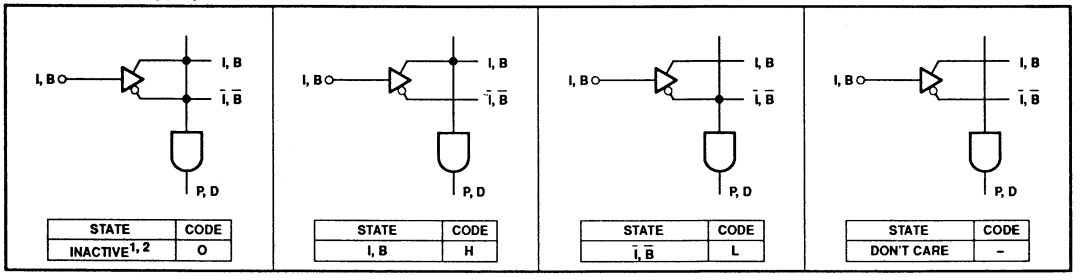
SLICE is available free of charge to qualified users.

Logic Programming

The PLQ16XX series is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Signetics SLICE and SNAP design software packages. ABEL™ CUPL™ and PALASM® 90 design software packages also support the PLQ16XX architecture.

All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

AND ARRAY – (I, B)



STATE	CODE
INACTIVE[1, 2]	O

STATE	CODE
I, B	H

STATE	CODE
$\overline{I, B}$	L

STATE	CODE
DON'T CARE	–

VIRGIN STATE

A factory shipped virgin device contains all fusible links intact, such that:

1. All P_n terms are disabled.
2. All P_n terms are active on all outputs.

ABEL is a trademark of Data I/O Corp.
CUPL is a trademark of Logical Devices, Inc.
PALASM is a registered trademark of AMD Corp.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS MIN	RATINGS MAX	UNIT
V_{CC}	Supply voltage	–0.5	+7.0	V_{DC}
V_{IN}	Input voltage	–1.2	+7.0	V_{DC}
V_{OUT}	Output voltage		+5.5	V_{DC}
I_{IN}	Input currents	–30	+30	mA
I_{OUT}	Output currents		+100	mA
T_{stg}	Storage temperature range	–65	+150	°C

NOTE:
1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

OPERATING RANGES

SYMBOL	PARAMETER	RATINGS MIN	RATINGS MAX	UNIT
V_{CC}	Supply voltage	+4.75	+5.25	V_{DC}
T_{amb}	Operating free-air temperature	0	+75	°C

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

DC ELECTRICAL CHARACTERISTICS

$0°C \leq T_{amb} \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[1]	MAX	
Input voltage[2]						
V_{IL}	Low	V_{CC} = MIN			0.8	V
V_{IH}	High	V_{CC} = MAX	2.0			V
V_{IC}	Clamp	V_{CC} = MIN, I_{IN} = –18mA		–0.8	–1.5	V
Output voltage						
		V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}				
V_{OL}	Low	I_{OL} = 24mA			0.5	V
V_{OH}	High	I_{OH} = –3.2 mA	2.4			V
Input current						
		V_{CC} = MAX				
I_{IL}	Low[3]	V_{IN} = 0.40V			–250	µA
I_{IH}	High[3]	V_{IN} = 2.7V			25	µA
I_I	Maximum input current	V_{IN} = 5.5V, V_{CC} = MAX			100	µA
Output current						
		V_{CC} = MAX				
I_{OZH}	Output leakage	V_{OUT} = 2.7V			100	µA
I_{OZL}	Output leakage	V_{OUT} = 0.4V			–100	µA
I_{OS}	Short circuit[4, 5]	V_{OUT} = 0.5V	–30		–130	mA
I_{CC}	V_{CC} supply current	V_{CC} = MAX		160	180	mA
Capacitance[6]						
C_{IN}	Input	V_{CC} = 5V				
		V_{OUT} = 2.0V		8		pF
C_B	I/O (B)	V_{OUT} = 2V, f = 1MHz		8		pF

NOTES:
1. All typical values are at V_{CC} = 5V, T_{amb} = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Leakage current for bidirectional pins is the worst case of I_{IL} and I_{OZL} or I_{IH} and I_{OZH}.
4. Test one at a time.
5. Duration of short circuit should not exceed 1 second.
6. These parameters are not 100% tested but periodically sampled.

AC ELECTRICAL CHARACTERISTICS

$R_1 = 200\Omega$, $R_2 = 390\Omega$, $0°C \le T_{amb} \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

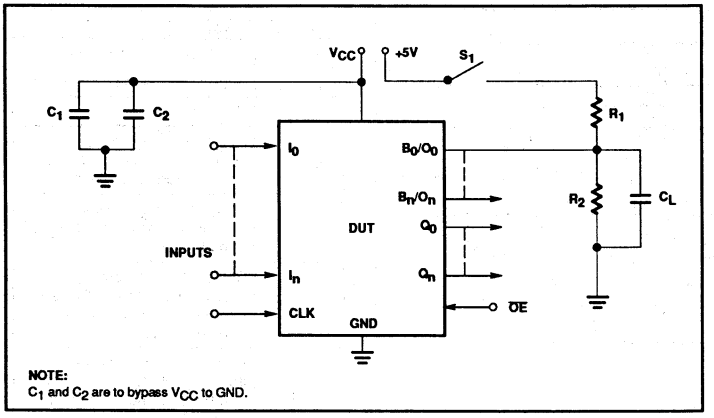
SYMBOL	PARAMETER	FROM	TO	LIMITS MIN[1]	LIMITS MAX	UNIT
Pulse Width						
t_{CKH}	Clock High	CLK+	CLK–	3.0		ns
t_{CKL}	Clock Low	CLK–	CLK+	3.0		ns
t_{CKP}	Period	CLK+	CLK+	6.0		ns
Setup & Hold time						
t_{IS}	Input	Input or feedback	CLK+	4.0		ns
t_{IH}	Input	CLK+	Input or feedback	0		ns
Propagation delay						
t_{CKO}	Clock	CLK±	Q±		4.5	ns
t_{CKF}	Clock[3]	CLK±	$\overline{Q}$		2.5	ns
t_{PD}	Output (16L8, R6, R4)[2]	I, B	Output		5.0	ns
t_{OE1}	Output enable[4]	$\overline{OE}$	Output enable		6.0	ns
t_{OE2}	Output enable[4,5]	I	Output enable		8.0	ns
t_{OD1}	Output disable[4]	$\overline{OE}$	Output disable		6.0	ns
t_{OD2}	Output disable[4,5]	I	Output disable		8.0	ns
t_{SKW}	Output	Q	Q		1.0	ns
t_{PPR}	Power-Up Reset	V_{CC}+	Q+		8.0	ns
Frequency (16R8, R6, R4)						
f_{MAX}	No feedback $1/(t_{CKL} + t_{CKH})$[6]				167	MHz
	Internal feedback $1/(t_{IS} + t_{CKF})$[6]				154	MHz
	External feedback $1/(t_{IS} + t_{CKO})$[6]				118	MHz

* For definitions of the terms, please refer to the Timing/Frequency Definitions tables.

NOTES:

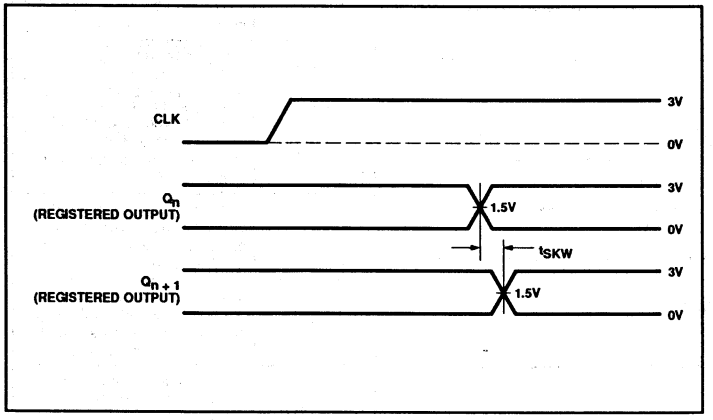
1. CL = 0pF while measuring minimum output delays.
2. t_{PD} test conditions: C_L = 50pF (with jig and scope capacitance), V_{IH} = 3V, V_{IL} = 0V, $V_{OH} = V_{OL}$ = 1.5V.
3. t_{CKF} was calculated from measured Internal f_{MAX}.
4. For 3-State output; output enable times are tested with C_L = 50pF to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with C_L = 5pF. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} - 0.5V)$ with S_1 open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with S_1 closed.
5. Same function as t_{OE1} and t_{OD1}, with the difference of using product term control.
6. Not 100% tested, but calculated at initial characterization and at any time a modification in design takes place which may affect the frequency.

TEST LOAD CIRCUIT

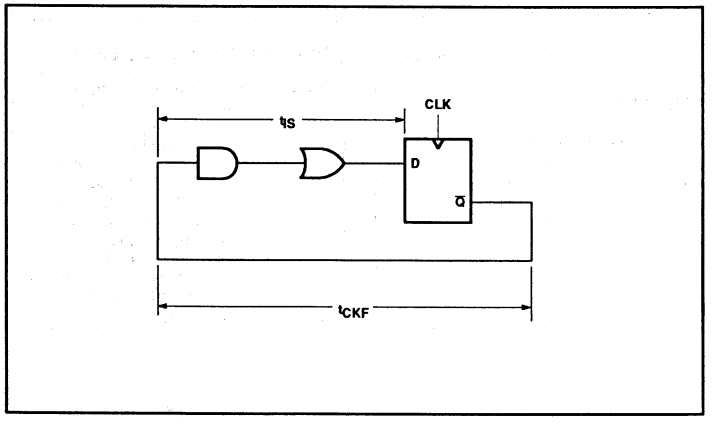


NOTE:
C_1 and C_2 are to bypass V_{CC} to GND.

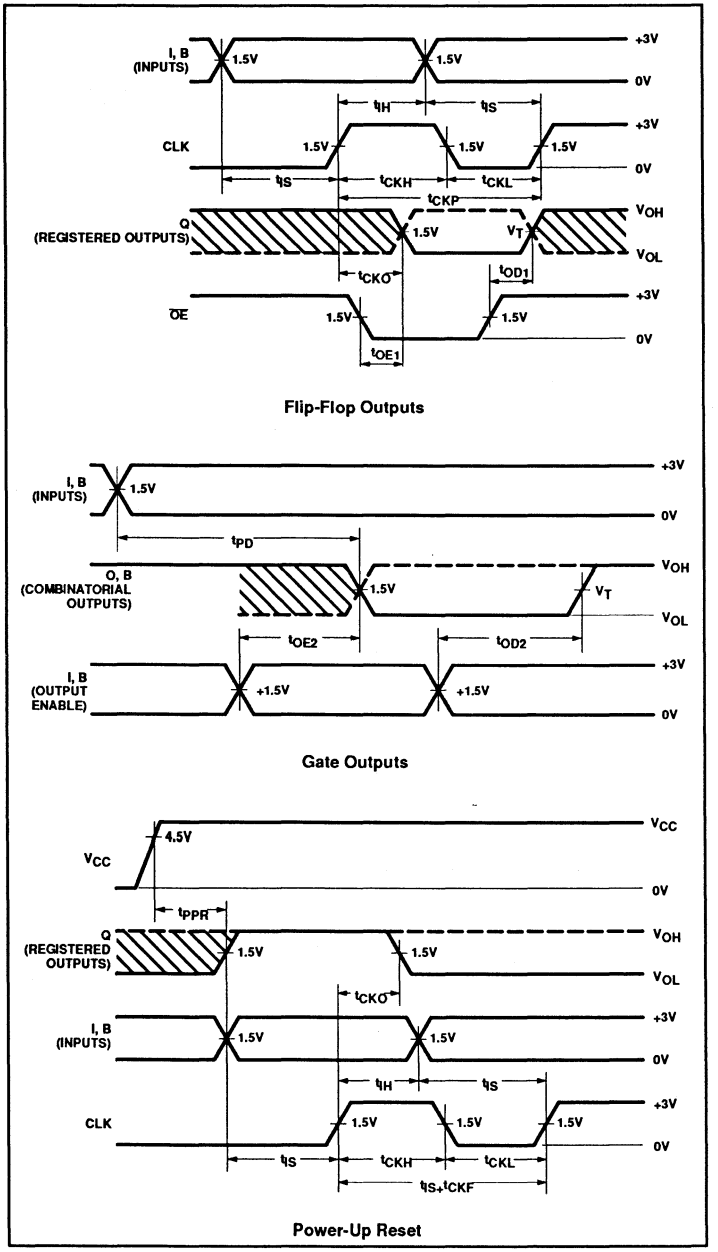
OUTPUT REGISTER SKEW



CLOCK TO FEEDBACK PATH



TIMING DIAGRAMS[1, 2]



NOTES:
1. Input pulse amplitude is 0V to 3V.
2. Input rise and fall times are 2.0ns typical.

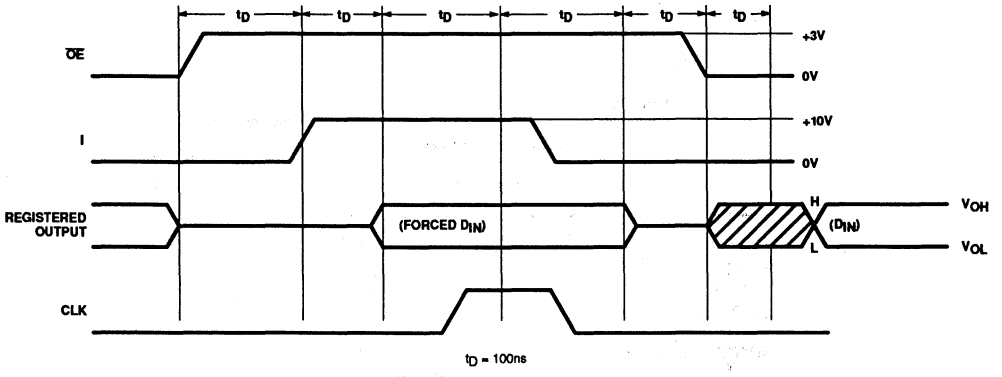
TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{CKH}	Width of input clock pulse.
t_{CKL}	Interval between clock pulses.
t_{CKP}	Clock period.
t_{IS}	Required delay between beginning of valid input and positive transition of clock.
t_{IH}	Required delay between positive transition of clock and end of valid input data.
t_{CKF}	Delay between positive transition of clock and when internal $\overline{Q}$ output of flip-flop becomes valid.
t_{CKO}	Delay between positive transition of clock and when outputs become valid (with $\overline{OE}$ Low).
t_{OE1}	Delay between beginning of Output Enable Low and when outputs become valid.
t_{OD1}	Delay between beginning of Output Enable High and when outputs are in the Off-State.
t_{OE2}	Delay between predefined Output Enable High, and when combinational outputs become valid.
t_{OD2}	Delay between predefined Output Enable Low and when combinational outputs are in the Off-State.
t_{PPR}	Delay between V_{CC} (after power-on) and when flip-flop outputs become preset at "1" (internal Q outputs at "0").
t_{PD}	Propagation delay between combinational inputs and outputs.
t_D	Delay between each input change.

FREQUENCY DEFINITIONS

f_{MAX}	**No feedback:** Determined by the minimum clock period, $1/(t_{CKL} + t_{CKH})$. **Internal feedback:** Determined by the internal delay from flip-flop outputs through the internal feedback and array to the flip-flop inputs, $1/(t_{IS} + t_{CKF})$. **External feedback:** Determined by clock-to-output delay and input setup time, $1/(t_{IS} + t_{CKO})$.

TIMING DIAGRAMS (Continued)

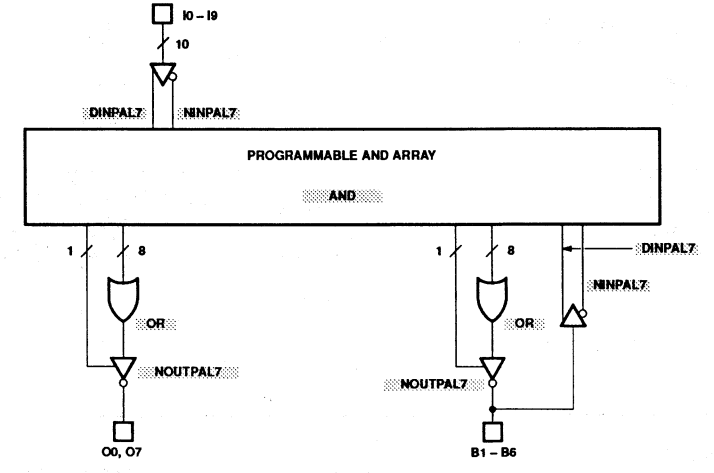


Output Register Preload

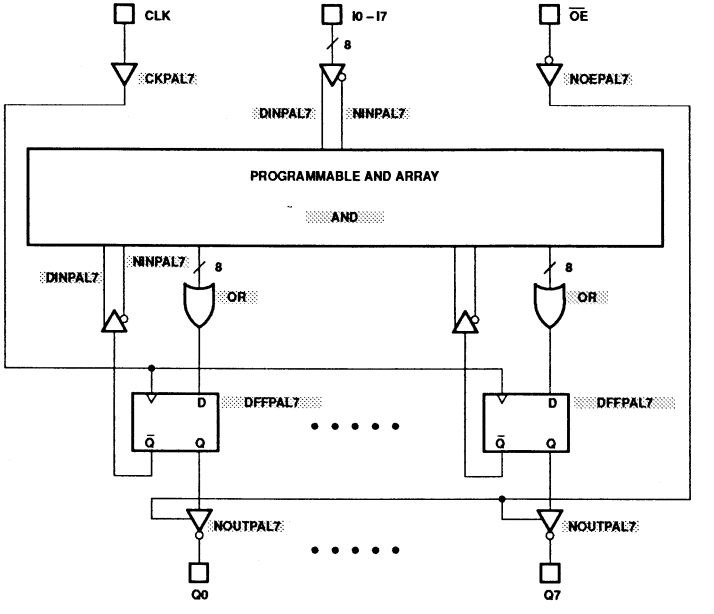
PROGRAMMING/SOFTWARE

Refer to Section 8 *(Development Software)* and Section 9 *(Third-Party Programmer/ Software Support)* of this data handbook for additional information.

SNAP RESOURCE SUMMARY DESIGNATIONS

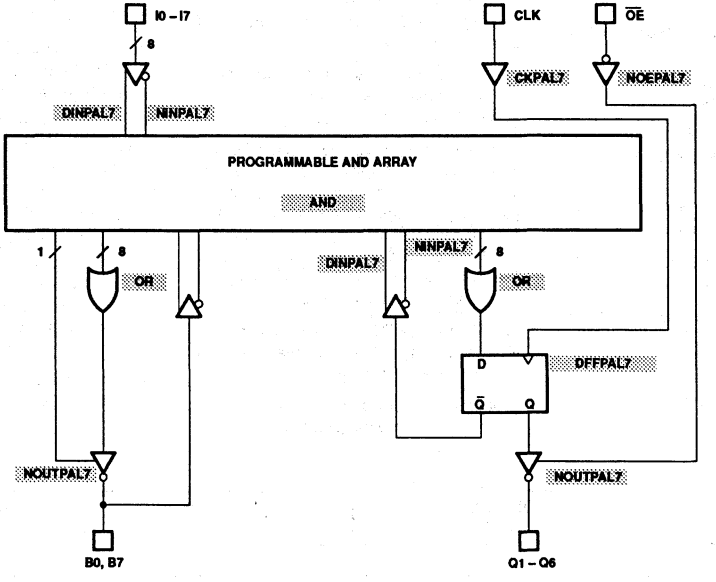


PLQ16L8

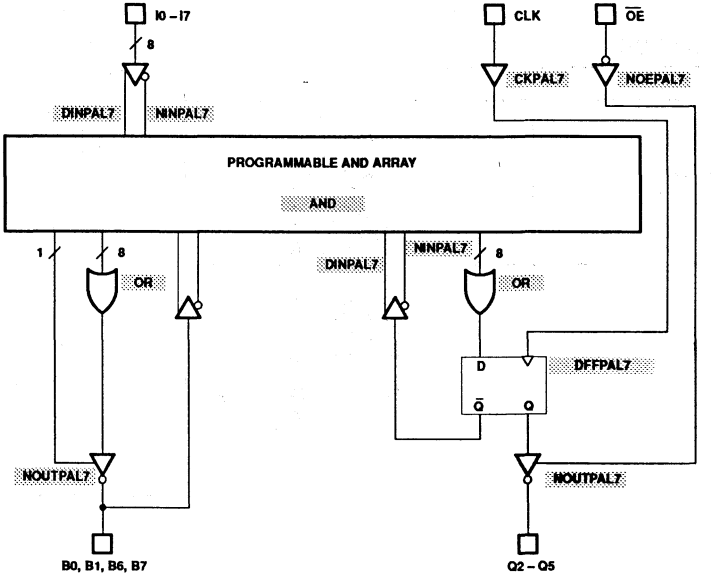


PLQ16R8

SNAP RESOURCE SUMMARY DESIGNATIONS (Continued)



PLQ16R6



PLQ16R4

PAL devices
20L8, 20R8, 20R6, 20R4

PLUS20R8D/-7 SERIES

FEATURES

- Ultra high-speed
  - t_{PD} = 7.5ns and f_{MAX} = 74MHz for the PLUS20R8-7 Series
  - t_{PD} = 10ns and f_{MAX} = 60 MHz for the PLUS20R8D Series
- 100% functionally and pin-for-pin compatible with industry standard 24-pin PAL® ICs
- Power-up reset function to enhance state machine design and testability
- Design support provided via SLICE and other CAD tools for Series 24 PAL devices
- Field-programmable on industry standard programmers
- Security fuse
- Individual 3-State control of all outputs

DESCRIPTION

The Signetics PLUS20XX family consists of ultra high-speed 7.5ns and 10ns versions of Series 24 PAL devices.

The PLUS20XX family is 100% functional and pin-compatible with the 20L8, 20R8, 20R6, and 20R4 Series devices.

The sum of products (AND-OR) architecture is comprised of 64 AND gates and 8 fixed OR gates. Multiple bidirectional pins provide variable input/output pin ratios. Individual 3-State control of all outputs and registers with feedback (R8, R6, R4) is also provided. Proprietary designs can be protected by programming the security fuse.

The PLUS20R8, R6, and R4 have D-type flip-flops which are loaded on the Low-to-High transition of the clock input.

In order to facilitate state machine design and testing, a power-up reset function has been incorporated into these devices to reset all internal registers to active-Low after a specific period of time.

The Signetics State-of-the-Art oxide isolation Bipolar fabrication process is employed to achieve high-performance operation.

The PLUS20XX family of devices are field programmable, enabling the user to quickly generate custom patterns using standard programming equipment. See the programmer chart for qualified programmers.

The SLICE software package from Signetics supports easy design entry for the PLUS20XX series as well as other PLD devices from Signetics. The PLUS20XX series are also supported by other standard CAD tools for PAL-type devices.

Order codes are listed in the Ordering Information table.

DEVICE NUMBER	DEDICATED INPUTS	COMBINATORIAL OUTPUTS	REGISTERED OUTPUTS
PLUS20L8	14	8 (6 I/O)	0
PLUS20R8	12	0	8
PLUS20R6	12	2 I/O	6
PLUS20R4	12	4 I/O	4

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-Pin Plastic Dual-In-Line 300mil-wide	PLUS20R8DN PLUS20R6DN PLUS20R4DN PLUS20L8DN PLUS20R8–7N PLUS20R6–7N PLUS20R4–7N PLUS20L8–7N
28-Pin Plastic Leaded Chip Carrier (PLCC)	PLUS20R8DA PLUS20R6DA PLUS20R4DA PLUS20L8DA PLUS20R8–7A PLUS20R6–7A PLUS20R4–7A PLUS20L8–7A

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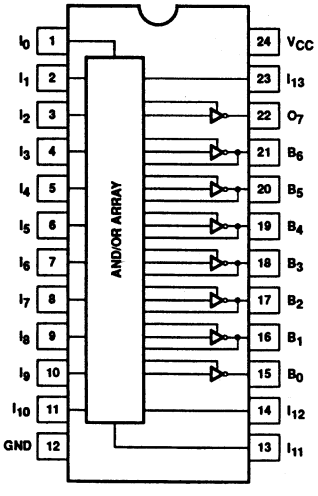
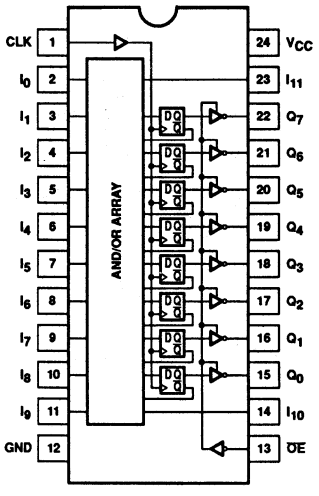
PIN CONFIGURATIONS

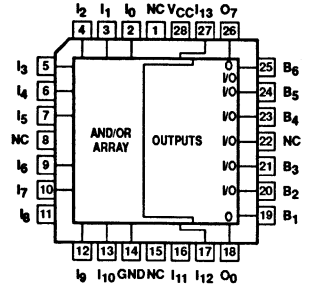
PLUS20L8



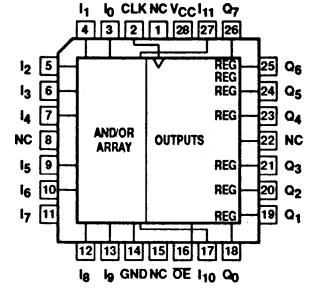
PLUS20R8



PLUS20L8



PLUS20R8

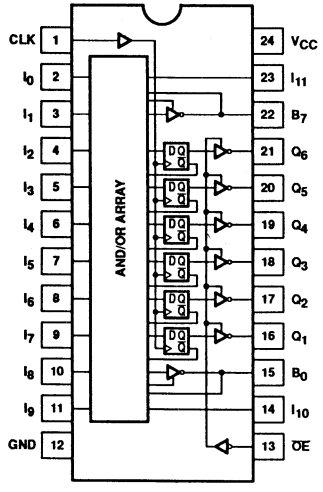


SYMBOL	DESCRIPTION
I	Dedicated Input
O	Dedicated combinatorial Output
Q	Registered output
B	Bidirectional (input/output)
CLK	Clock input
OE	Output Enable
V_{CC}	Supply Voltage
GND	Ground
NC	No Connection

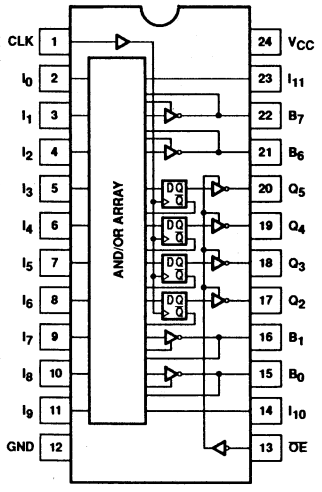
SYMBOL	DESCRIPTION
I	Dedicated Input
O	Dedicated combinatorial Output
Q	Registered output
B	Bidirectional (input/output)
CLK	Clock input
OE	Output Enable
V_{CC}	Supply Voltage
GND	Ground
NC	No Connection

PIN CONFIGURATIONS

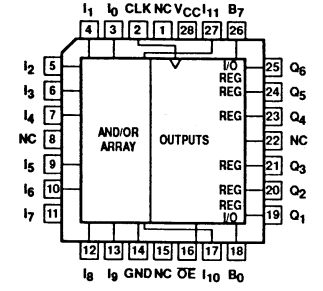
PLUS20R6



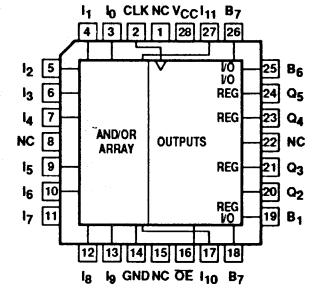
PLUS20R4



PLUS20R6



PLUS20R4

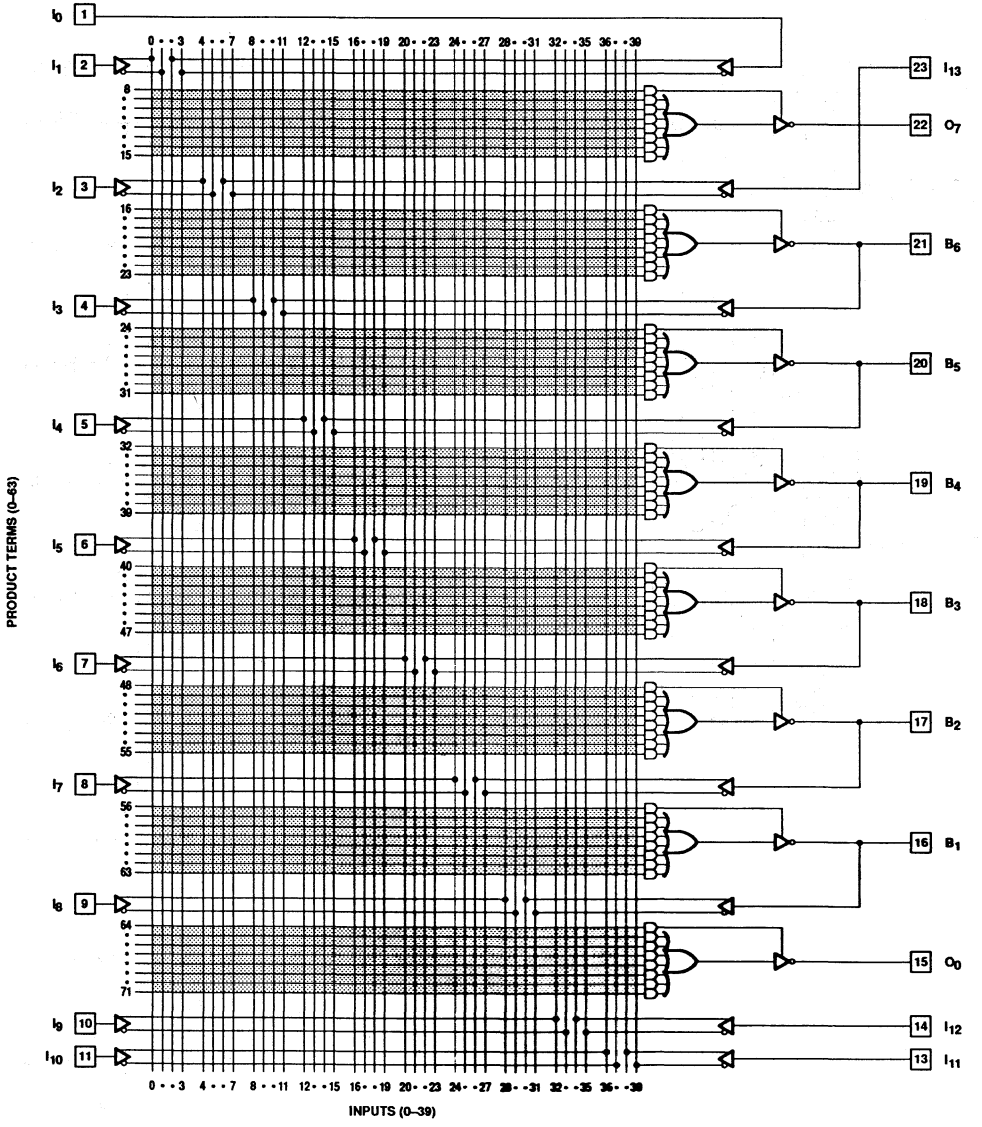


SYMBOL	DESCRIPTION
I	Dedicated Input
O	Dedicated combinatorial Output
Q	Registered output
B	Bidirectional (input/output)
CLK	Clock input
OE	Output Enable
V_{CC}	Supply Voltage
GND	Ground
NC	No Connection

SYMBOL	DESCRIPTION
I	Dedicated Input
O	Dedicated combinatorial Output
Q	Registered output
B	Bidirectional (input/output)
CLK	Clock input
OE	Output Enable
V_{CC}	Supply Voltage
GND	Ground
NC	No Connection

LOGIC DIAGRAM

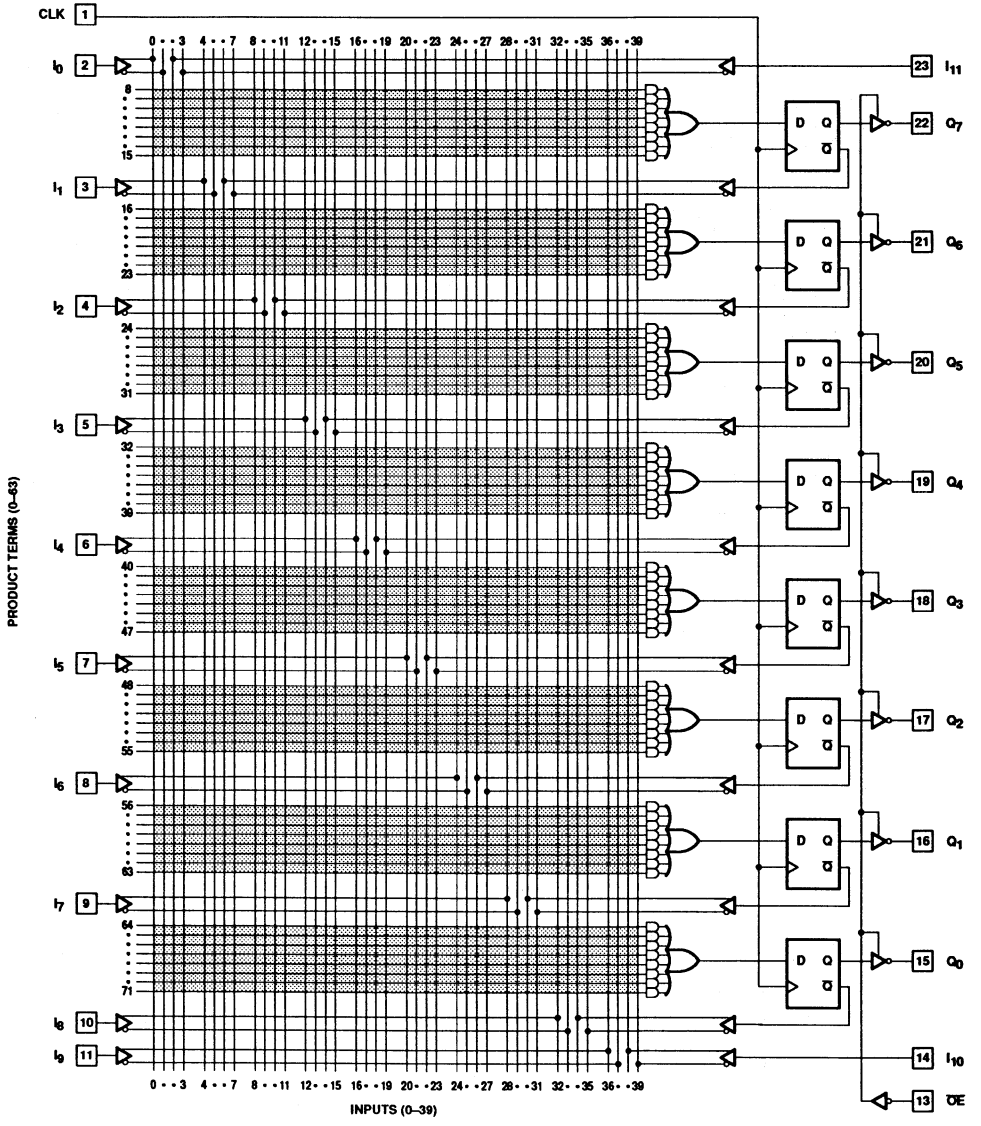
PLUS20L8



NOTES:
1. All unprogrammed or virgin "AND" gate locations are pulled to logic "0".
2. ▒ Programmable connections.

LOGIC DIAGRAM

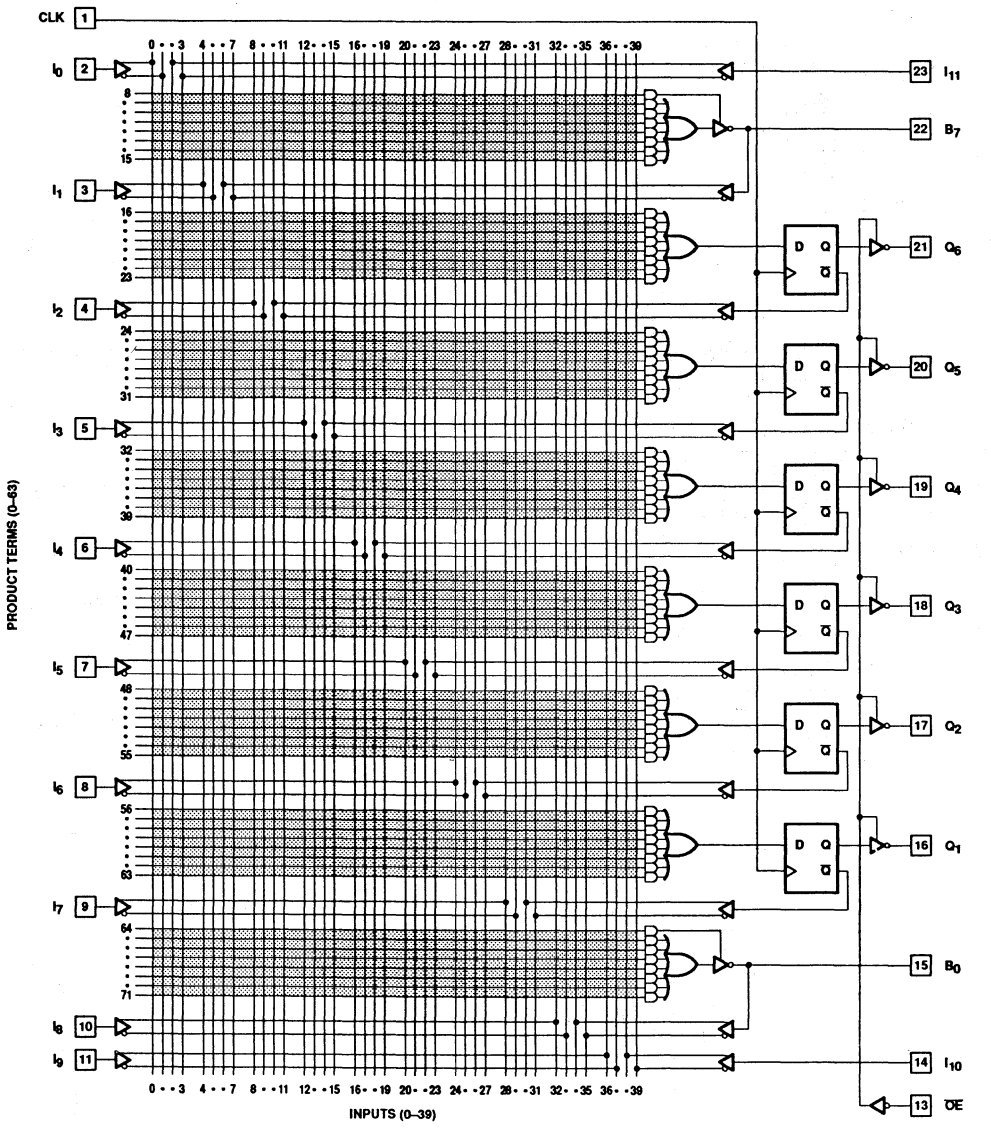
PLUS20R8



NOTES:
1. All unprogrammed or virgin "AND" gate locations are pulled to logic "0".
2. ▒ Programmable connections.

LOGIC DIAGRAM

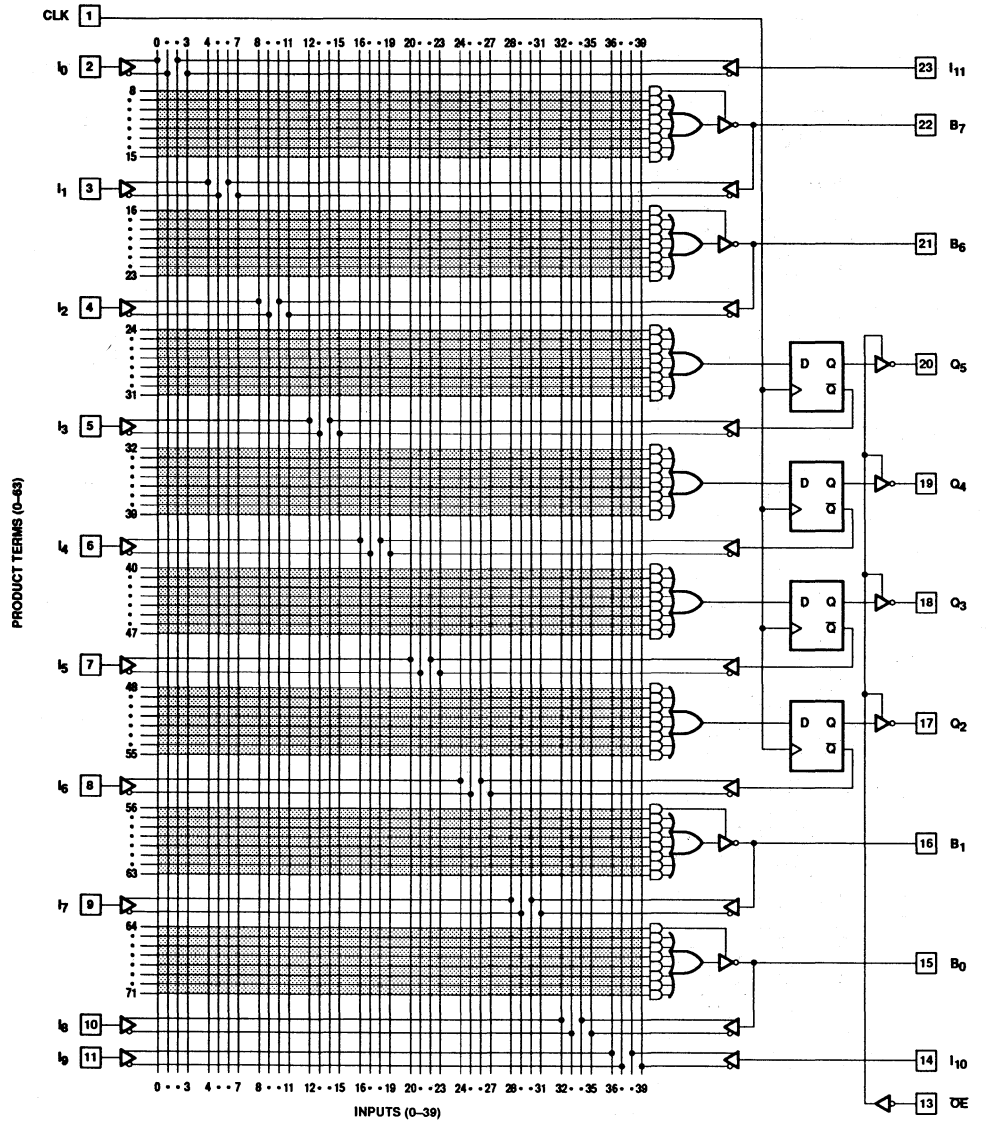
PLUS20R6



NOTES:
1. All unprogrammed or virgin "AND" gate locations are pulled to logic "0".
2. ▒ Programmable connections.

LOGIC DIAGRAM

PLUS20R4



NOTES:
1. All unprogrammed or virgin "AND" gate locations are pulled to logic "0".
2. ▒ Programmable connections.

FUNCTIONAL DESCRIPTIONS

The PLUS20XX series utilizes the familiar sum-of-products implementation consisting of a programmable AND array and a fixed OR array. These devices are capable of replacing an equivalent of four or more SSI/MSI integrated circuits to reduce package count and board area occupancy, consequently improving reliability and design cycle over Standard Cell or gate array options. By programming the security fuse, proprietary designs can be protected from duplication.

The PLUS20XX series consists of four PAL-type devices. Depending on the particular device type, there are a variable number of combinatorial and registered outputs available to the designer. The PLUS20L8 is a combinatorial part with 8 user configurable outputs (6 bidirectional), while the other three devices, PLUS20R8, PLUS20R6, PLUS20R4, have respectively 8, 6, and 4 output registers.

3-State Outputs

The PLUS20XX series devices also feature 3-State output buffers on each output pin which can be programmed for individual control of all outputs. The registered outputs (Qn) are controlled by an external input (/OE), and the combinatorial outputs (On, Bn) use a product term to control the enable function.

Programmable Bidirectional Pins

The PLUS20XX products feature variable Input/Output ratios. In addition to 12 dedicated inputs, each combinatorial output pin of the registered devices can be individually programmed as an input or output. The PLUS20L8 provides 14 dedicated inputs and 6 Bidirectional I/O lines that can be individually configured as inputs or outputs.

Output Registers

The PLUS20R8 has 8 output registers, the 20R6 has 6, and the 20R4 has 4. Each output register is a D-type flip-flop which is loaded on the Low-to-High transition of the clock input. These output registers are capable of feeding the outputs of the registers back into the array to facilitate design of synchronous state machines.

Power-up Reset

By resetting all flip-flops to a logic Low, as the power is turned on, the PLUS20R8, R6, R4 enhance state machine design and initialization capability.

Software Support

Like other Programmable Logic Devices from Signetics, the PLUS20XX series are supported by SLICE, the PC-based software development tool from Signetics. The PLUS20XX family of devices are also supported by standard CAD tools for PAL devices, including ABEL and CUPL.

SLICE is available free of charge to qualified users.

Logic Programming

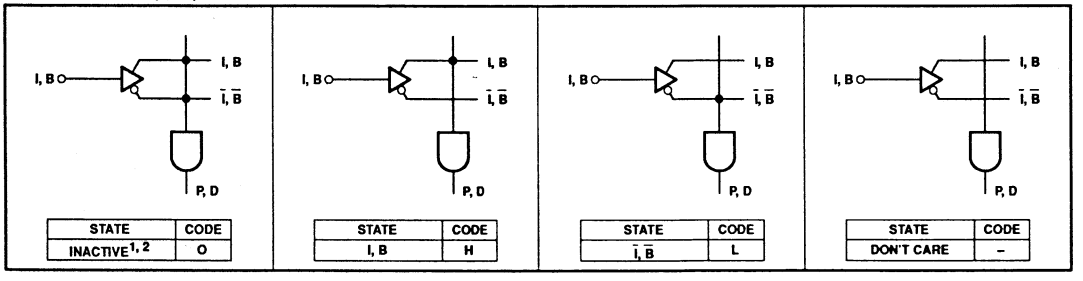
The PLUS20XX series is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Signetics SLICE and SNAP design software packages. ABEL™ CUPL™ and PALASM® 90 design software packages also support the PLUS20XX architecture.

All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

PROGRAMMING/SOFTWARE SUPPORT

Refer to Section 8 *(Development Software)* and Section 9 *(Third-Party Programmer/ Software Support)* of the PLD data handbook for additional information.

AND ARRAY – (I, B)



STATE	CODE
INACTIVE[1, 2]	O

STATE	CODE
I, B	H

STATE	CODE
$\overline{I}$, $\overline{B}$	L

STATE	CODE
DON'T CARE	–

VIRGIN STATE

A factory shipped virgin device contains all fusible links intact, such that:

1. All outputs are at "H" polarity.
2. All P_n terms are disabled.
3. All P_n terms are active on all outputs.

ABEL is a trademark of Data I/O Corp.
CUPL is a trademark of Logical Devices, Inc.
PALASM is a registered trademark of AMD Corp.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS		UNIT
		MIN	MAX	
V_{CC}	Supply voltage	–0.5	+7	V_{DC}
V_{IN}	Input voltage	–1.2	+8.0	V_{DC}
V_{OUT}	Output voltage	–0.5	V_{CC} + 0.5V	V_{DC}
I_{IN}	Input currents	–30	+30	mA
I_{OUT}	Output currents		+100	mA
T_{stg}	Storage temperature range	–65	+150	°C

NOTE:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

OPERATING RANGES

SYMBOL	PARAMETER	RATINGS		UNIT
		MIN	MAX	
V_{CC}	Supply voltage	+4.75	+5.25	V_{DC}
T_{amb}	Operating free–air temperature	0	+75	°C

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

DC ELECTRICAL CHARACTERISTICS

$0°C \leq T_{amb} \leq +75°C$, $4.75 \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[1]	MAX	
Input voltage[2]						
V_{IL}	Low	V_{CC} = MIN			0.8	V
V_{IH}	High	V_{CC} = MAX	2.0			V
V_{IC}	Clamp	V_{CC} = MIN, I_{IN} = –18mA		–0.8	–1.5	V
Output voltage						
		V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}				
V_{OL}	Low	I_{OL} = 24mA			0.5	V
V_{OH}	High	I_{OH} = –3.2mA	2.4			V
Input current						
		V_{CC} = MAX				
I_{IL}	Low[3]	V_{IN} = 0.40V			–250	µA
I_{IH}	High[3]	V_{IN} = 2.7V			25	µA
I_I	Maximum input current	V_{IN} = V_{CC} = V_{CCMAX}			100	µA
Output current						
		V_{CC} = MAX				
I_{OZH}	Output leakage	V_{OUT} = 2.7V			100	µA
I_{OZL}	Output leakage	V_{OUT} = 0.4V			–100	µA
I_{OS}	Short circuit[4, 5]	V_{OUT} = 0V	–30		–90	mA
I_{CC}	V_{CC} supply current	V_{CC} = MAX		150	210	mA
Capacitance[6]						
C_{IN}	Input	V_{CC} = 5V				
		V_{OUT} = 2.0V		8		pF
C_B	I/O (B)	V_{OUT} = 2V, f = 1MHz		8		pF

NOTES:
1. All typical values are at V_{CC} = 5V, T_{amb} = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Leakage current for bidirectional pins is the worst case of I_{IL} and I_{OZL} or I_{IH} and I_{OZH}.
4. Test one at a time.
5. Duration of short circuit should not exceed 1 second.
6. These parameters are not 100% tested but periodically sampled.

AC ELECTRICAL CHARACTERISTICS

$R_1 = 200\Omega$, $R_2 = 390\Omega$, $0°C \le T_{amb} \le +75°C$, $4.75 \le V_{CC} \le 5.25V$

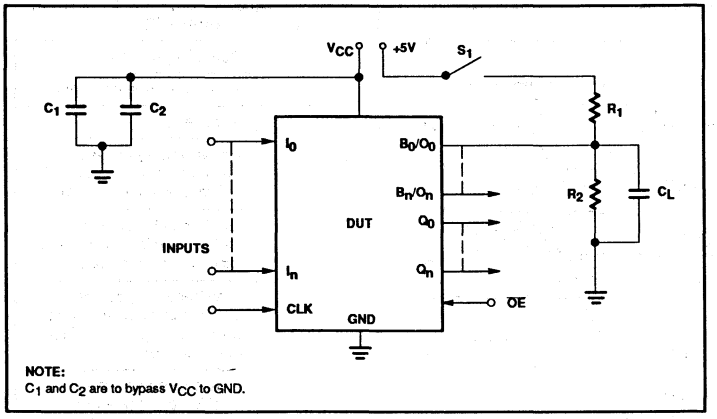
SYMBOL	PARAMETER	FROM	TO	LIMITS					UNIT
				-7			D		
				MIN[1]	TYP	MAX	MIN[1]	MAX	
Pulse Width									
t_{CKH}	Clock High	CK+	CK–	5			7		ns
t_{CKL}	Clock Low	CK–	CK+	5			7		ns
t_{CKP}	Period	CK+	CK+	10			14		ns
Setup & Hold time									
t_{IS}	Input	Input or feedback	CK+	7			9		ns
t_{IH}	Input	CK+	Input or feedback	0			0		ns
Propagation delay									
t_{CKO}	Clock	CK±	Q±	3		6.5	3	7.5	ns
t_{CKF}	Clock[3]	CK±	$\overline{Q}$			3		6.5	ns
t_{PD}	Output (20L8, R6, R4)[2]	I, B	Output	3		7.5	3	10	ns
t_{OE1}	Output enable[4]	$\overline{OE}$	Output enable	3		8	3	10	ns
t_{OE2}	Output enable[4,5]	I	Output enable	3		10	3	10	ns
t_{OD1}	Output disable[4]	$\overline{OE}$	Output disable	3		8	3	10	ns
t_{OD2}	Output disable[4,5]	I	Output disable	3		10	3	10	ns
t_{SKW}	Output	Q	Q			1		1	ns
t_{PPR}	Power-Up Reset	V_{CC}+	Q+			10		10	ns
Frequency (20R8, R6, R4)									
f_{MAX}	No feedback $1/(t_{CKL} + t_{CKH})$[6]				100		71.4		MHz
	Internal feedback $1/(t_{IS} + t_{CKF})$[6]				90		64.5		MHz
	External feedback $1/(t_{IS} + t_{CKO})$[6]				74		60.6		MHz

* For definitions of the terms, please refer to the Timing/Frequency Definitions tables.

NOTES:

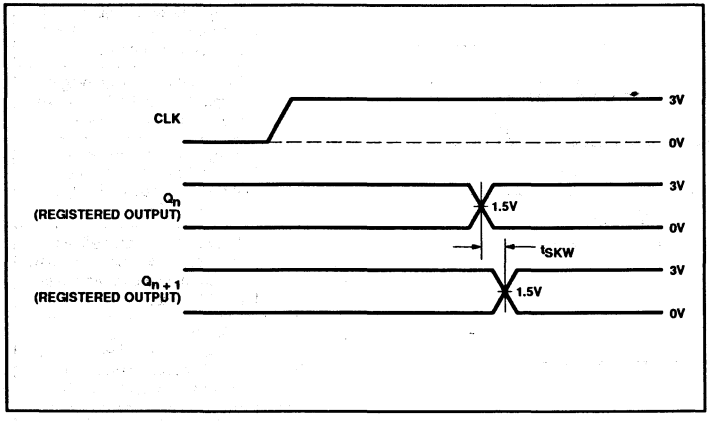
1. CL = 0pF while measuring minimum output delays.
2. t_{PD} test conditions: CL = 50pF (with jig and scope capacitance), $V_{IH} = 3V$, $V_{IL} = 0V$, $V_{OH} = V_{OL} = 1.5V$.
3. t_{CKF} was calculated from measured Internal f_{MAX}.
4. For 3-State output; output enable times are tested with $C_L = 50pF$ to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with $C_L = 5pF$. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} - 0.5V)$ with S_1 open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with S_1 closed.
5. Same function as t_{OE1} and t_{OD1}, with the difference of using product term control.
6. Not 100% tested, but calculated at initial characterization and at any time a modification in design takes place which may affect the frequency.

TEST LOAD CIRCUIT

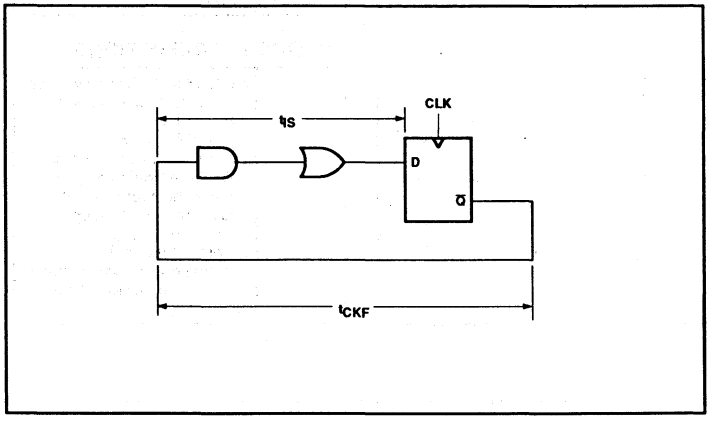


NOTE:
C_1 and C_2 are to bypass V_{CC} to GND.

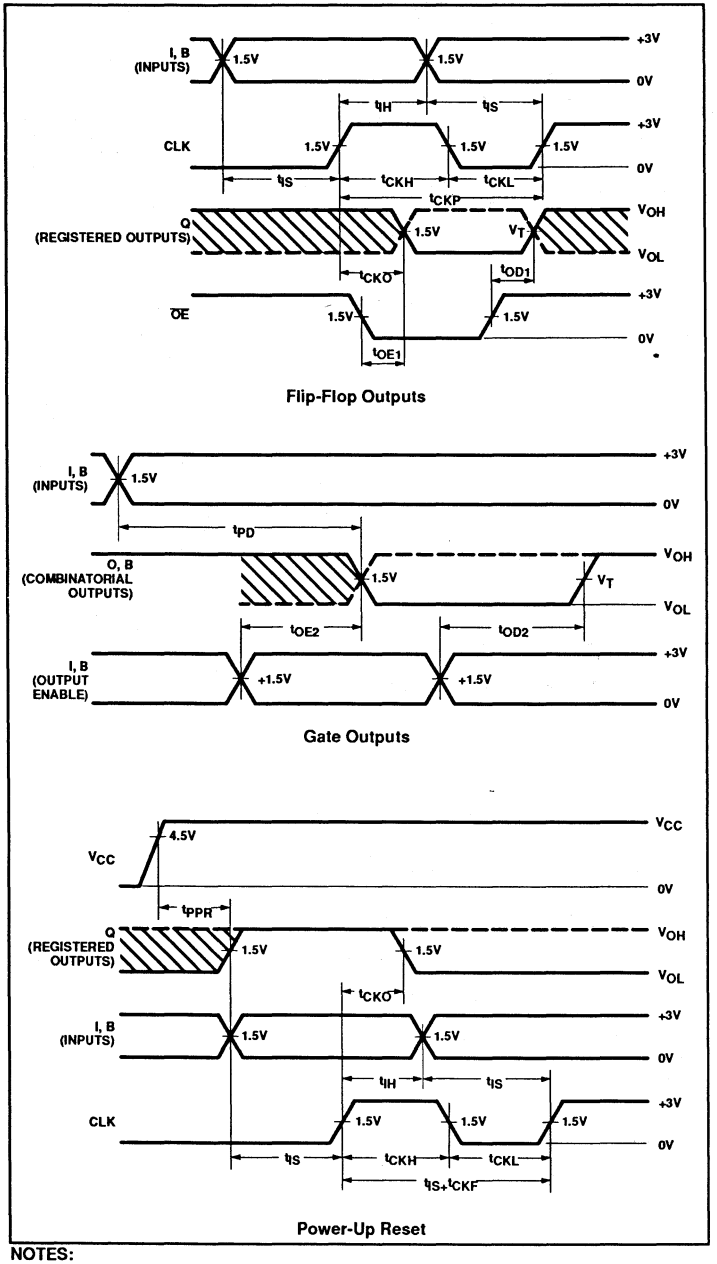
OUTPUT REGISTER SKEW



CLOCK TO FEEDBACK PATH



TIMING DIAGRAMS[1, 2]



NOTES:
1. Input pulse amplitude is 0V to 3V.
2. Input rise and fall times are 2.5ns.

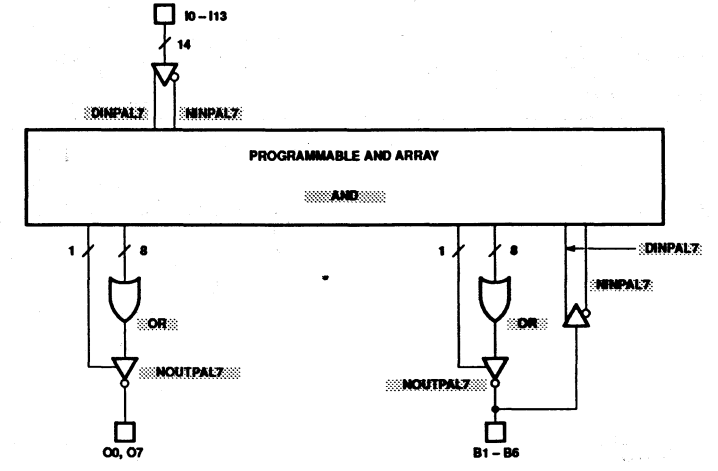
TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{CKH}	Width of input clock pulse.
t_{CKL}	Interval between clock pulses.
t_{CKP}	Clock period.
t_{IS}	Required delay between beginning of valid input and positive transition of clock.
t_{IH}	Required delay between positive transition of clock and end of valid input data.
t_{CKF}	Delay between positive transition of clock and when internal $\overline{Q}$ output of flip-flop becomes valid.
t_{CKO}	Delay between positive transition of clock and when outputs become valid (with $\overline{OE}$ Low).
t_{OE1}	Delay between beginning of Output Enable Low and when outputs become valid.
t_{OD1}	Delay between beginning of Output Enable High and when outputs are in the Off-State.
t_{OE2}	Delay between predefined Output Enable High, and when combinational outputs become valid.
t_{OD2}	Delay between predefined Output Enable Low and when combinational outputs are in the Off-State.
t_{PPR}	Delay between V_{CC} (after power-on) and when flip-flop outputs become preset at "1" (internal Q outputs at "0").
t_{PD}	Propagation delay between combinational inputs and outputs.

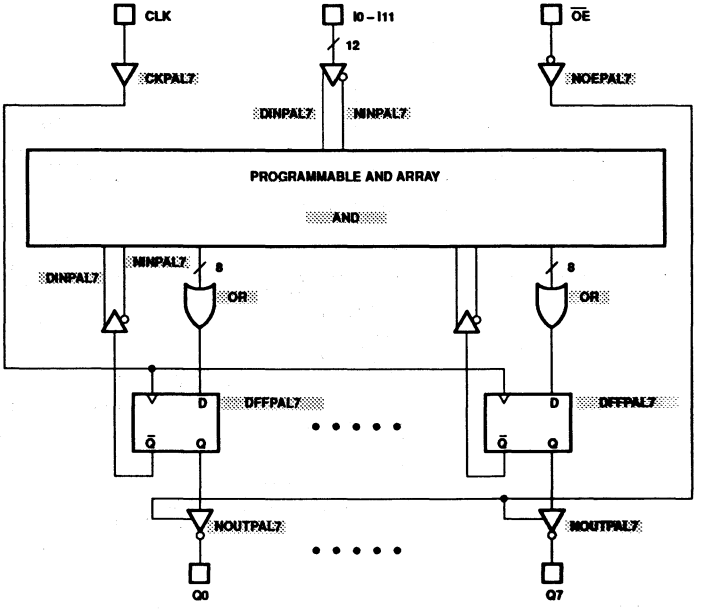
FREQUENCY DEFINITIONS

f_{MAX}	**No feedback:** Determined by the minimum clock period, $1/(t_{CKL} + t_{CKH})$. **Internal feedback:** Determined by the internal delay from flip-flop outputs through the internal feedback and array to the flip-flop inputs, $1/(t_{IS} + t_{CKF})$. **External feedback:** Determined by clock-to-output delay and input setup time, $1/(t_{IS} + t_{CKO})$.

SNAP RESOURCE SUMMARY DESIGNATIONS

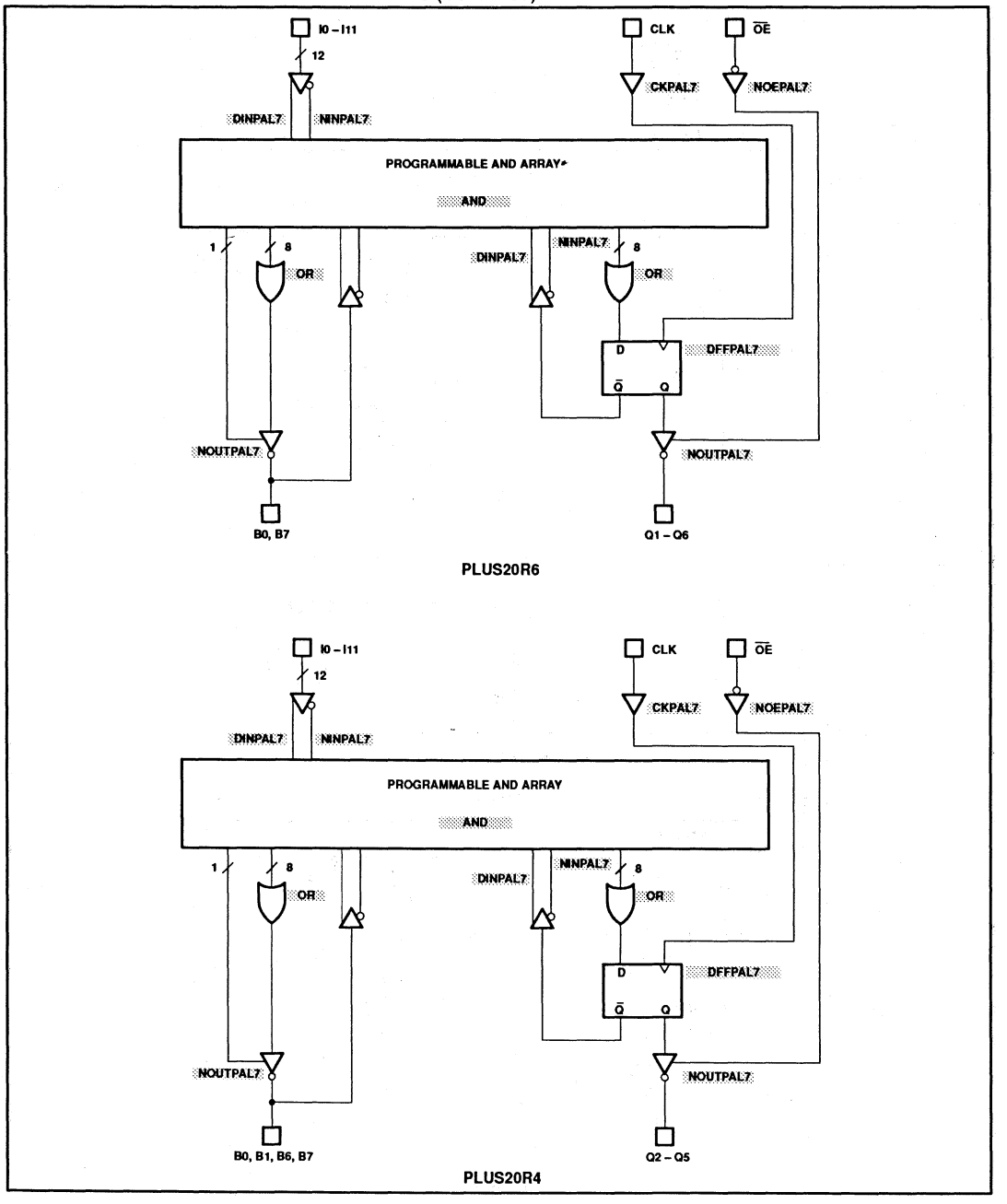


PLUS20L8



PLUS20R8

SNAP RESOURCE SUMMARY DESIGNATIONS (Continued)



PAL devices
20L8, 20R8, 20R6, 20R4

PLQ20R8-5 SERIES

FEATURES

- Ultra high-speed
  - t_{PD} = 5ns and f_{MAX} = 118MHz
- 100% functionally and pin-for-pin compatible with industry standard 24-pin PAL ICs
- Power-up reset function to enhance state machine design and testability
- Design support provided via SLICE and other CAD tools for Series 24 PAL devices
- Field-programmable on industry standard programmers
- Security fuse
- Individual 3-State control of all outputs
- Register preload for testability
- Power-up 3-State
- 24-Pin DIP and 28-Pin PLCC

DESCRIPTION

The Signetics PLQ20XX family consists of ultra high-speed 5ns versions of Series 24 PAL devices.

The PLQ20XX family is 100% functional and pin-compatible with the 20L8, 20R8, 20R6, and 20R4 Series devices.

The sum of products (AND-OR) architecture is comprised of 64 AND gates and 8 fixed OR gates. Multiple bidirectional pins provide variable input/output pin ratios. Individual 3-State control of all outputs and registers with feedback (R8, R6, R4) is also provided. Proprietary designs can be protected by programming the security fuse.

The PLQ20R8, R6, and R4 have D-type flip-flops which are loaded on the Low-to-High transition of the clock input.

In order to facilitate state machine design and testing, a power-up reset function has been incorporated into these devices to reset all internal registers to active-Low after a specific period of time.

The Signetics State-of-the-Art BiCMOS process, known as QUBiC, has been employed to achieve higher levels of operating performance for the PLQ20XX family of PLDs. The QUBiC transistors have been optimized to provide two-thirds more speed at less than half the power consumed from products using our last generation of bipolar technology. QUBiC reduces on-chip delays and provides high output drive currents while consuming power at very low levels.

The PLQ20XX family of devices are field programmable, enabling the user to quickly generate custom patterns using standard programming equipment. See the programmer chart for qualified programmers.

The SLICE software package from Signetics supports easy design entry for the PLQ20XX series as well as other PLD devices from Signetics. The PLQ20XX series are also supported by other standard CAD tools for PAL-type devices.

Order codes are listed in the Ordering Information table.

DEVICE NUMBER	DEDICATED INPUTS	COMBINATORIAL OUTPUTS	REGISTERED OUTPUTS
PLQ20L8	14	8 (6 I/O)	0
PLQ20R8	12	0	8
PLQ20R6	12	2 I/O	6
PLQ20R4	12	4 I/O	4

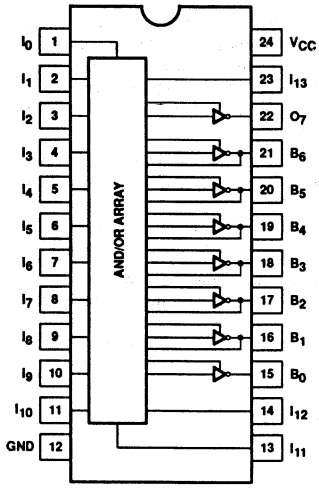
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-Pin Plastic Dual-In-Line 300mil-wide	PLQ20R8–5N PLQ20R6–5N PLQ20R4–5N PLQ20L8–5N
28-Pin Plastic Leaded Chip Carrier (PLCC)	PLQ20R8–5A PLQ20R6–5A PLQ20R4–5A PLQ20L8–5A

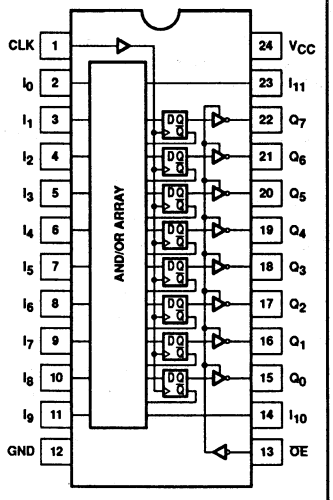
NOTE:
The PLQ20XX series of devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information, consult the Signetics Military Data Handbook.

PIN CONFIGURATIONS

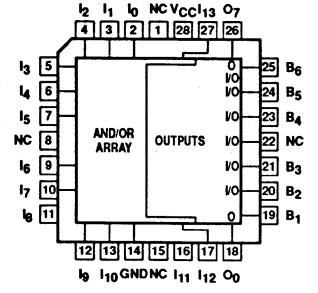
PLQ20L8



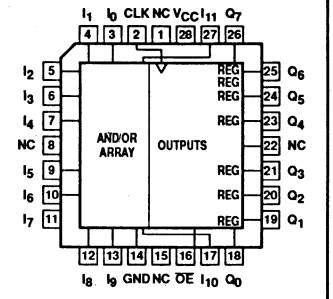
PLQ20R8



PLQ20L8



PLQ20R8

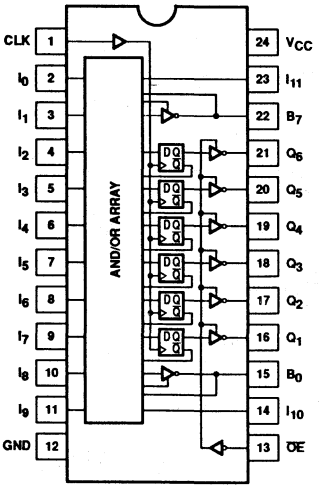


SYMBOL	DESCRIPTION
I	Dedicated Input
O	Dedicated combinatorial Output
Q	Registered output
B	Bidirectional (input/output)
CLK	Clock input
OE	Output Enable
V_{CC}	Supply Voltage
GND	Ground
NC	No Connection

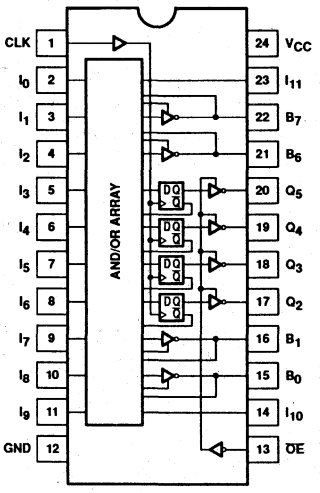
SYMBOL	DESCRIPTION
I	Dedicated Input
O	Dedicated combinatorial Output
Q	Registered output
B	Bidirectional (input/output)
CLK	Clock input
OE	Output Enable
V_{CC}	Supply Voltage
GND	Ground
NC	No Connection

PIN CONFIGURATIONS

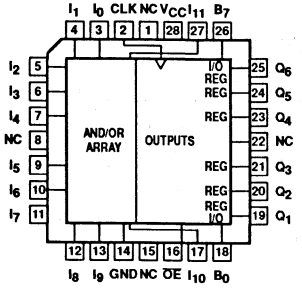
PLQ20R6



PLQ20R4

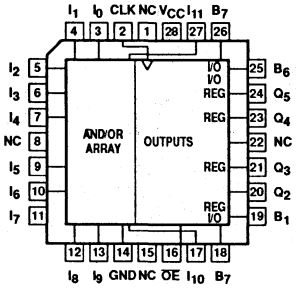


PLQ20R6



SYMBOL	DESCRIPTION
I	Dedicated Input
O	Dedicated combinatorial Output
Q	Registered output
B	Bidirectional (input/output)
CLK	Clock input
OE	Output Enable
V_{CC}	Supply Voltage
GND	Ground
NC	No Connection

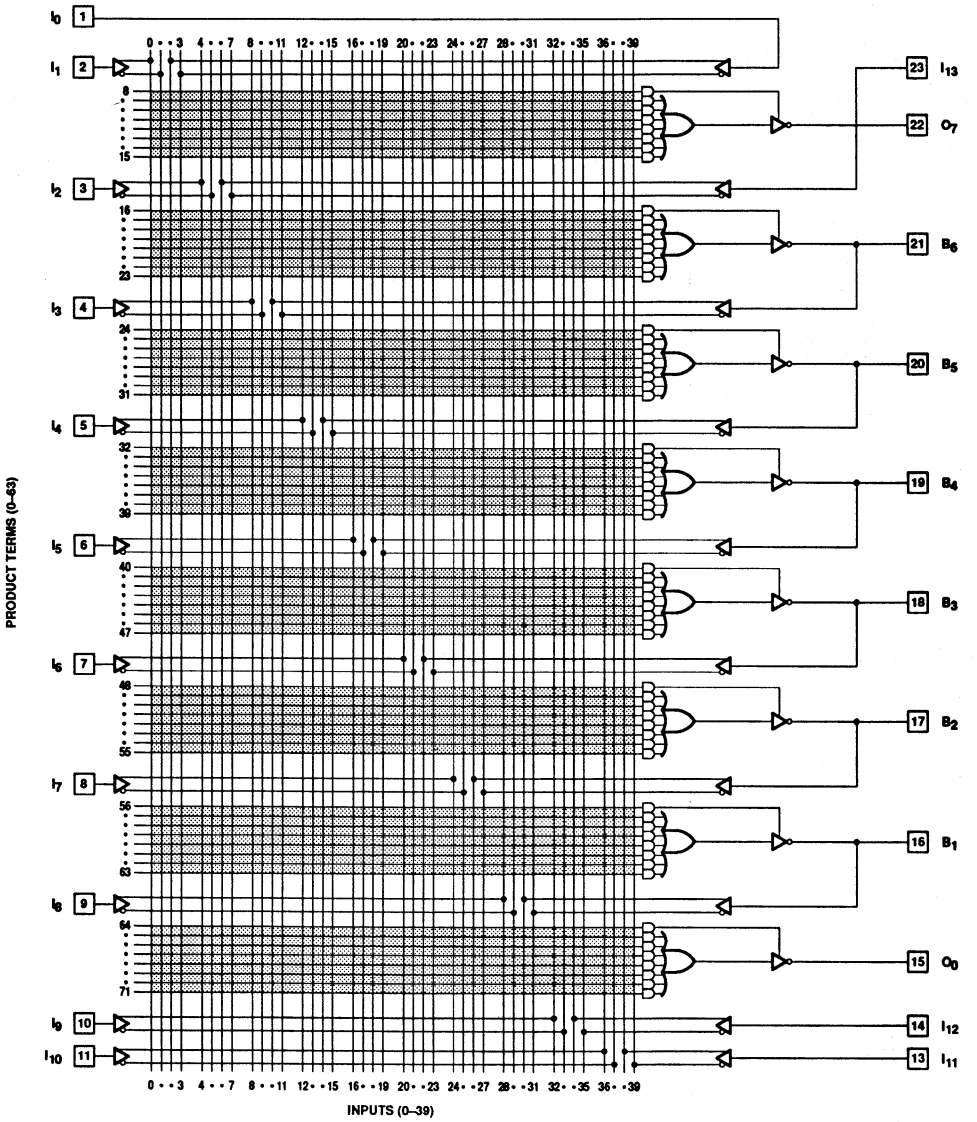
PLQ20R4



SYMBOL	DESCRIPTION
I	Dedicated Input
O	Dedicated combinatorial Output
Q	Registered output
B	Bidirectional (input/output)
CLK	Clock input
OE	Output Enable
V_{CC}	Supply Voltage
GND	Ground
NC	No Connection

LOGIC DIAGRAM

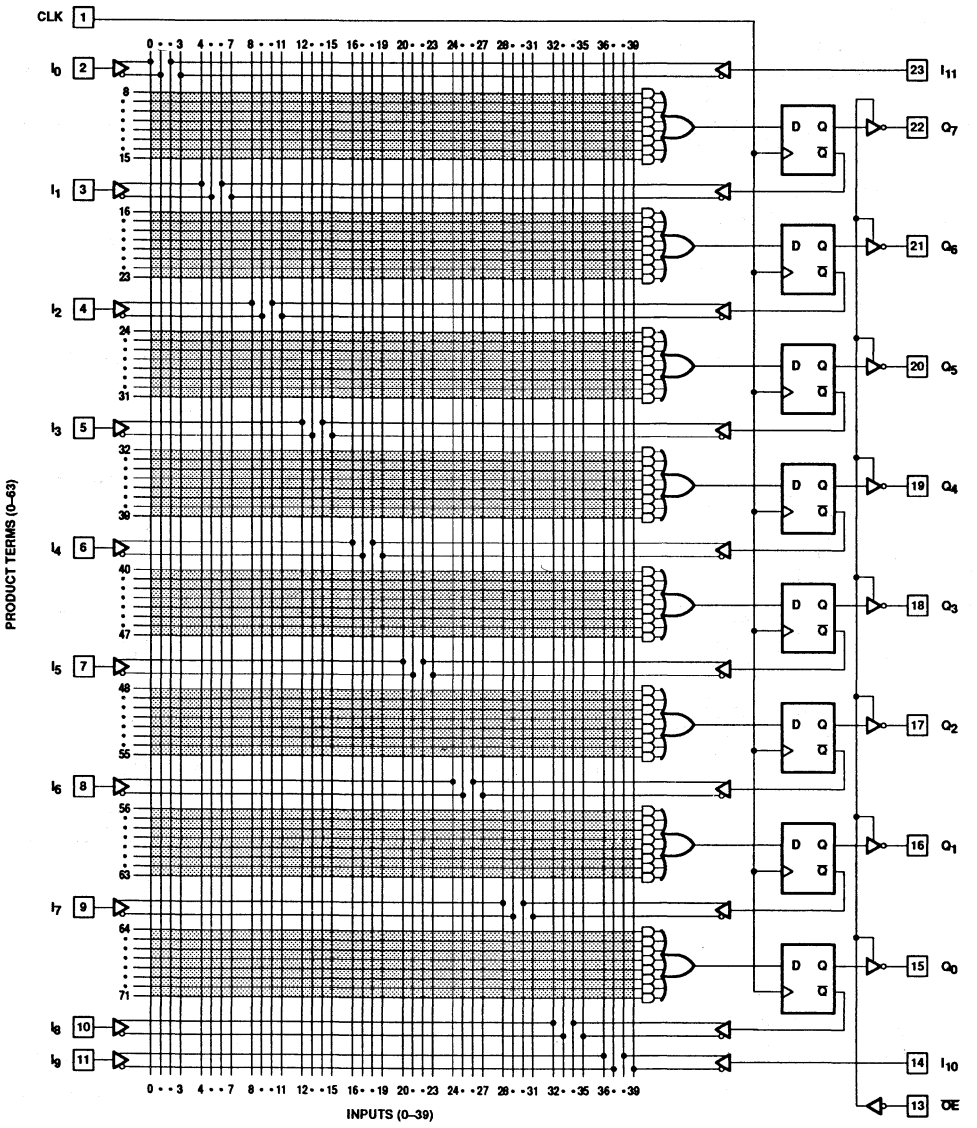
PLQ20L8



NOTES:
1. All unprogrammed or virgin "AND" gate locations are pulled to logic "0".
2. ▒ Programmable connections.

LOGIC DIAGRAM

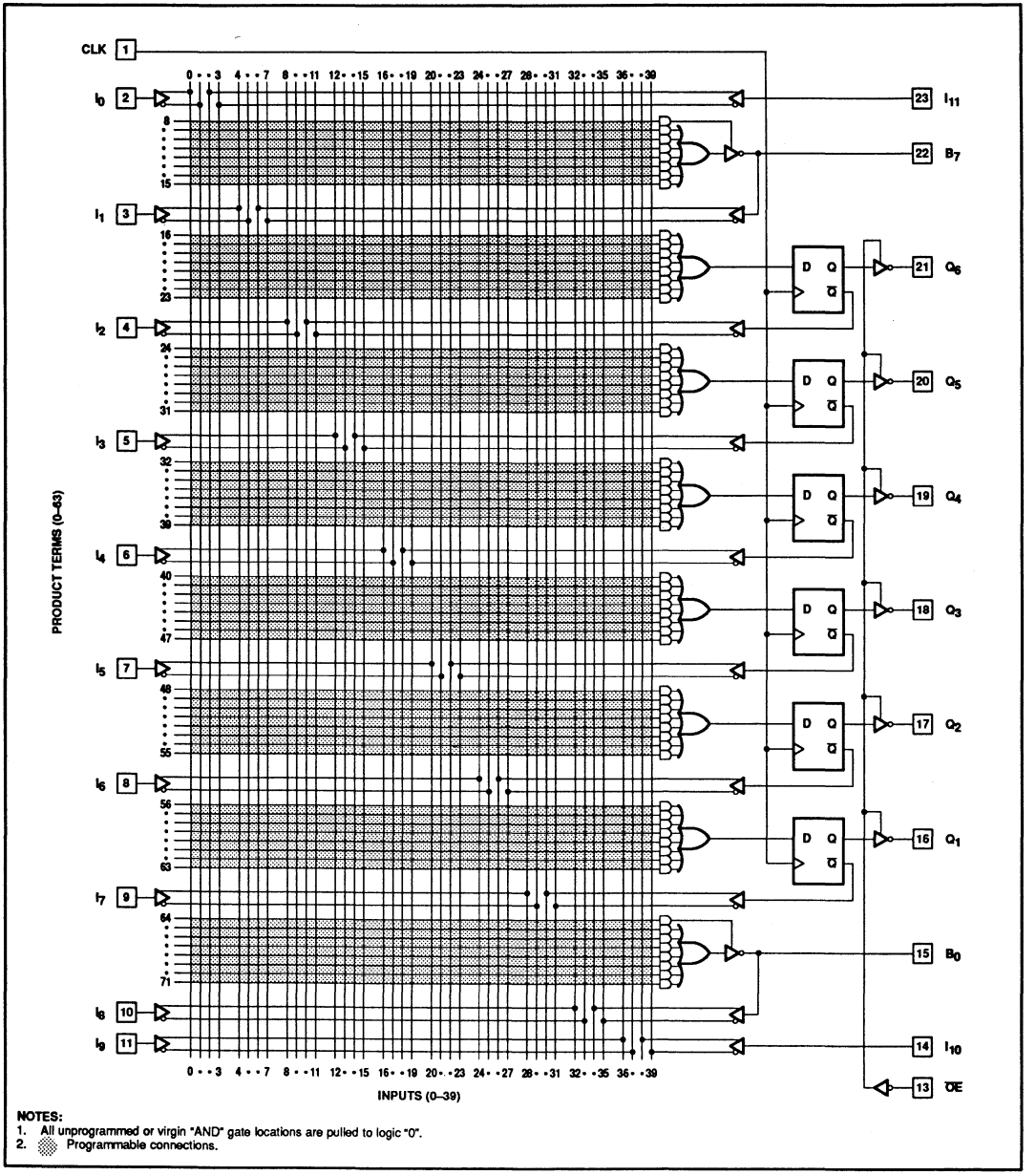
PLQ20R8



NOTES:
1. All unprogrammed or virgin "AND" gate locations are pulled to logic "0".
2. ▒ Programmable connections.

LOGIC DIAGRAM

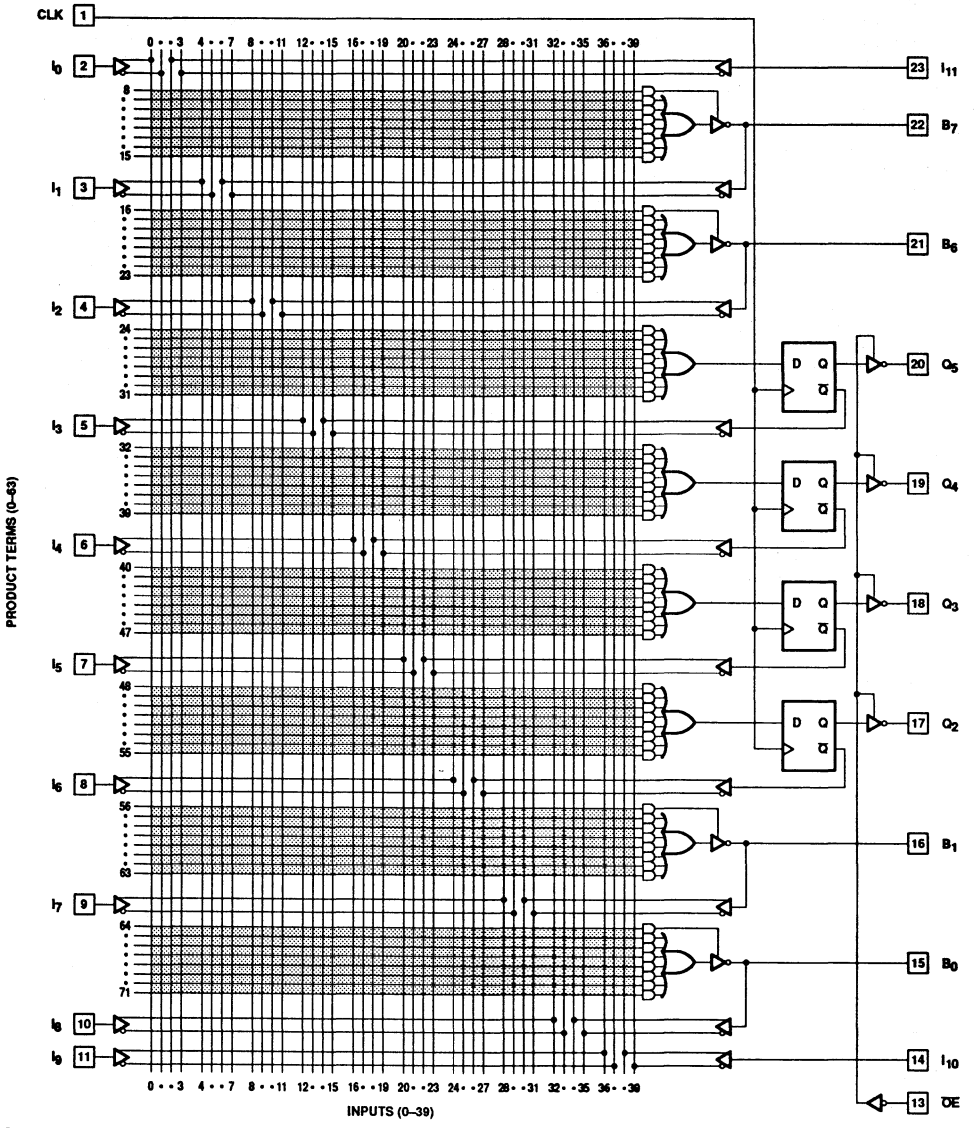
PLQ20R6



NOTES:
1. All unprogrammed or virgin "AND" gate locations are pulled to logic "0".
2. ▒ Programmable connections.

LOGIC DIAGRAM

PLQ20R4



NOTES:
1. All unprogrammed or virgin "AND" gate locations are pulled to logic "0".
2. ▒ Programmable connections.

FUNCTIONAL DESCRIPTIONS

The PLQ20XX series utilizes the familiar sum-of-products implementation consisting of a programmable AND array and a fixed OR array. These devices are capable of replacing an equivalent of four or more SSI/MSI integrated circuits to reduce package count and board area occupancy, consequently improving reliability and design cycle over Standard Cell or gate array options. By programming the security fuse, proprietary designs can be protected from duplication.

The PLQ20XX series consists of four PAL-type devices. Depending on the particular device type, there are a variable number of combinatorial and registered outputs available to the designer. The PLQ20L8 is a combinatorial part with 8 user configurable outputs (6 bidirectional), while the other three devices, PLQ20R8, PLQ20R6, PLQ20R4, have respectively 8, 6, and 4 output registers.

3-State Outputs

The PLQ20XX series devices also feature 3-State output buffers on each output pin which can be programmed for individual control of all outputs. The registered outputs (Qn) are controlled by an external input (/OE), and the combinatorial outputs (On, Bn) use a product term to control the enable function.

Programmable Bidirectional Pins

The PLQ20XX products feature variable Input/Output ratios. In addition to 12 dedicated inputs, each combinatorial output pin of the registered devices can be individually programmed as an input or output. The PLQ20L8 provides 14 dedicated inputs and 6 Bidirectional I/O lines that can be individually configured as inputs or outputs.

Output Registers

The PLQ20R8 has 8 output registers, the 20R6 has 6, and the 20R4 has 4. Each output register is a D-type flip-flop which is loaded on the Low-to-High transition of the clock input. These output registers are capable of feeding the outputs of the registers back into the array to facilitate design of synchronous state machines.

Power-up Reset

By resetting all flip-flops to a logic Low, as the power is turned on, the PLQ20R8, R6, R4 enhance state machine design and initialization capability.

Register Preload

Preload function allows the register to be loaded from the output pins. This feature allows functional testing of sequential patterns by loading output states.

Power-up 3-State

All outputs will be disabled when V_{CC} is 3.0V ± 20% (25°C). This special feature keeps outputs 3-Stated during power-up. Only when V_{CC} reaches its normal operating range will device function normally.

Software Support

Like other Programmable Logic Devices from Signetics, the PLQ20XX series are supported by SLICE, the PC-based software development tool from Signetics. The PLQ20XX family of devices are also supported by standard CAD tools for PAL devices, including ABEL and CUPL.

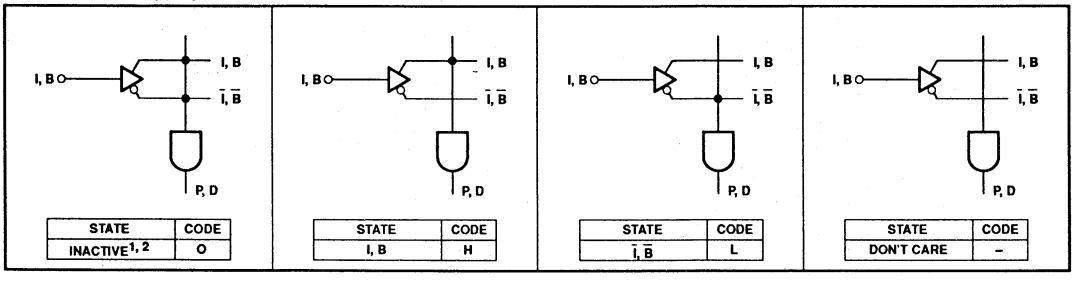
SLICE is available free of charge to qualified users.

Logic Programming

The PLQ20XX series is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Signetics SLICE and SNAP design software packages. ABEL™ CUPL™ and PALASM® 90 design software packages also support the PLQ20XX architecture.

All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

AND ARRAY – (I, B)



STATE	CODE
INACTIVE[1, 2]	O

STATE	CODE
I, B	H

STATE	CODE
$\overline{I}, \overline{B}$	L

STATE	CODE
DON'T CARE	–

VIRGIN STATE

A factory shipped virgin device contains all fusible links intact, such that:

1. All P_n terms are disabled.
2. All P_n terms are active on all outputs.

ABEL is a trademark of Data I/O Corp.
CUPL is a trademark of Logical Devices, Inc.
PALASM is a registered trademark of AMD Corp.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS MIN	RATINGS MAX	UNIT
V_{CC}	Supply voltage	–0.5	+7.0	V_{DC}
V_{IN}	Input voltage	–1.2	+7.0	V_{DC}
V_{OUT}	Output voltage		+5.5	V_{DC}
I_{IN}	Input currents	–30	+30	mA
I_{OUT}	Output currents		+100	mA
T_{stg}	Storage temperature range	–65	+150	°C

NOTE:
1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

OPERATING RANGES

SYMBOL	PARAMETER	RATINGS MIN	RATINGS MAX	UNIT
V_{CC}	Supply voltage	+4.75	+5.25	V_{DC}
T_{amb}	Operating free-air temperature	0	+75	°C

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

DC ELECTRICAL CHARACTERISTICS

$0°C \le T_{amb} \le +75°C$, $4.75 \le V_{CC} \le 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[1]	MAX	
Input voltage[2]						
V_{IL}	Low	V_{CC} = MIN			0.8	V
V_{IH}	High	V_{CC} = MAX	2.0			V
V_{IC}	Clamp	V_{CC} = MIN, I_{IN} = –18mA		–0.8	–1.5	V
Output voltage						
		V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}				
V_{OL}	Low	I_{OL} = 24mA			0.5	V
V_{OH}	High	I_{OH} = –3.2 mA	2.4			V
Input current						
		V_{CC} = MAX				
I_{IL}	Low[3]	V_{IN} = 0.40V			–250	µA
I_{IH}	High[3]	V_{IN} = 2.7V			25	µA
I_I	Maximum input current	V_{IN} = 5.5V, V_{CC} = MAX			100	µA
Output current						
		V_{CC} = MAX				
I_{OZH}	Output leakage	V_{OUT} = 2.7V			100	µA
I_{OZL}	Output leakage	V_{OUT} = 0.4V			–100	µA
I_{OS}	Short circuit[4, 5]	V_{OUT} = 0.5V	–30		–130	mA
I_{CC}	V_{CC} supply current	V_{CC} = MAX		150	210	mA
Capacitance[6]						
C_{IN}	Input	V_{CC} = 5V				
		V_{OUT} = 2.0V		8		pF
C_B	I/O (B)	V_{OUT} = 2V, f = 1MHz		8		pF

NOTES:
1. All typical values are at V_{CC} = 5V, T_{amb} = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Leakage current for bidirectional pins is the worst case of I_{IL} and I_{OZL} or I_{IH} and I_{OZH}.
4. Test one at a time.
5. Duration of short circuit should not exceed 1 second.
6. These parameters are not 100% tested but periodically sampled.

AC ELECTRICAL CHARACTERISTICS

$R_1 = 200\Omega$, $R_2 = 390\Omega$, $0°C \leq T_{amb} \leq +75°C$, $4.75 \leq V_{CC} \leq 5.25V$

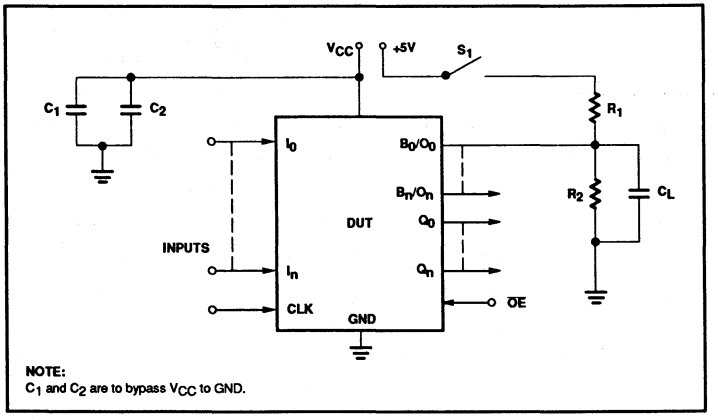
SYMBOL	PARAMETER	FROM	TO	LIMITS MIN[1]	LIMITS MAX	UNIT
Pulse Width						
t_{CKH}	Clock High	CLK+	CLK–	3.0		ns
t_{CKL}	Clock Low	CK–	CLK+	3.0		ns
t_{CKP}	Period	CLK+	CLK+	6.0		ns
Setup & Hold time						
t_{IS}	Input	Input or feedback	CLK+	4.0		ns
t_{IH}	Input	CLK+	Input or feedback	0		ns
Propagation delay						
t_{CKO}	Clock	CLK±	Q±		4.5	ns
t_{CKF}	Clock[3]	CLK±	$\overline{Q}$		2.5	ns
t_{PD}	Output (20L8, R6, R4)[2]	I, B	Output		5.0	ns
t_{OE1}	Output enable[4]	$\overline{OE}$	Output enable		6.0	ns
t_{OE2}	Output enable[4,5]	I	Output enable		8.0	ns
t_{OD1}	Output disable[4]	$\overline{OE}$	Output disable		6.0	ns
t_{OD2}	Output disable[4,5]	I	Output disable		8.0	ns
t_{SKW}	Output	Q	Q		1.0	ns
t_{PPR}	Power-Up Reset	V_{CC}+	Q+		8.0	ns
Frequency (20R8, R6, R4)						
f_{MAX}	No feedback $1/(t_{CKL} + t_{CKH})$[6]				167	MHz
	Internal feedback $1/(t_{IS} + t_{CKF})$[6]				154	MHz
	External feedback $1/(t_{IS} + t_{CKO})$[6]				118	MHz

* For definitions of the terms, please refer to the Timing/Frequency Definitions tables.

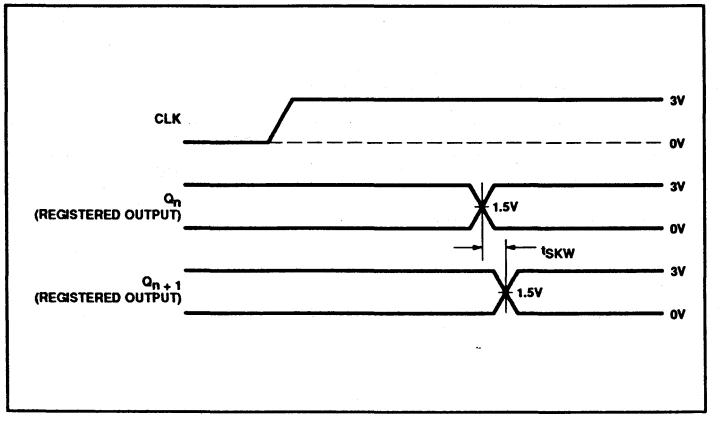
NOTES:

1. C_L = 0pF while measuring minimum output delays.
2. t_{PD} test conditions: C_L = 50pF (with jig and scope capacitance), V_{IH} = 3V, V_{IL} = 0V, $V_{OH} = V_{OL}$ = 1.5V.
3. t_{CKF} was calculated from measured Internal f_{MAX}.
4. For 3-State output; output enable times are tested with C_L = 50pF to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with C_L = 5pF. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} - 0.5V)$ with S_1 open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with S_1 closed.
5. Same function as t_{OE1} and t_{OD1}, with the difference of using product term control.
6. Not 100% tested, but calculated at initial characterization and at any time a modification in design takes place which may affect the frequency.

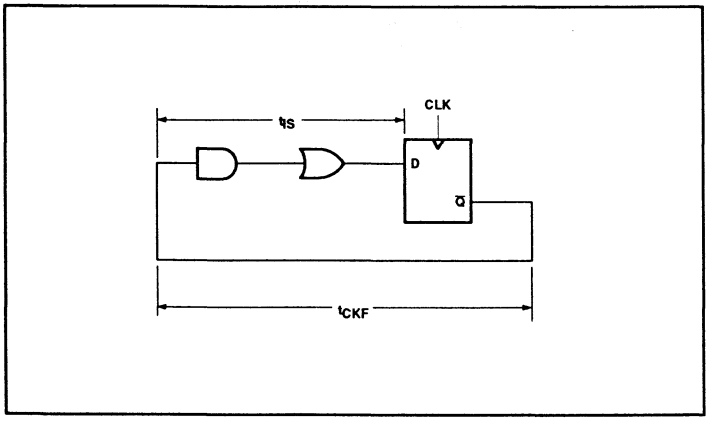
TEST LOAD CIRCUIT



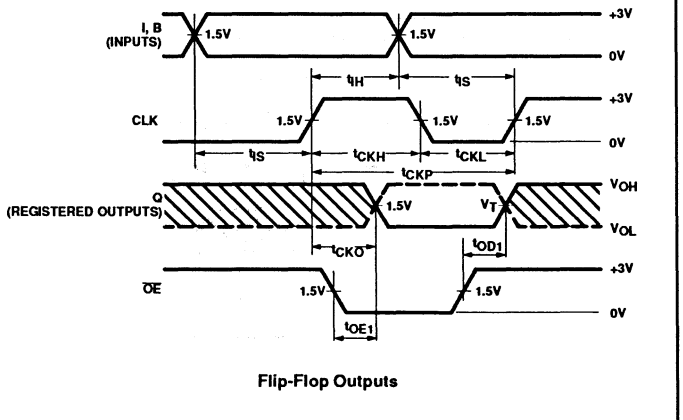
OUTPUT REGISTER SKEW



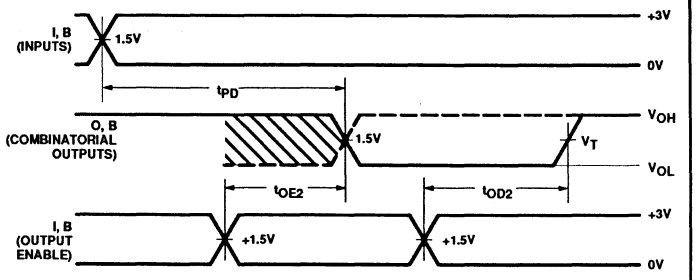
CLOCK TO FEEDBACK PATH



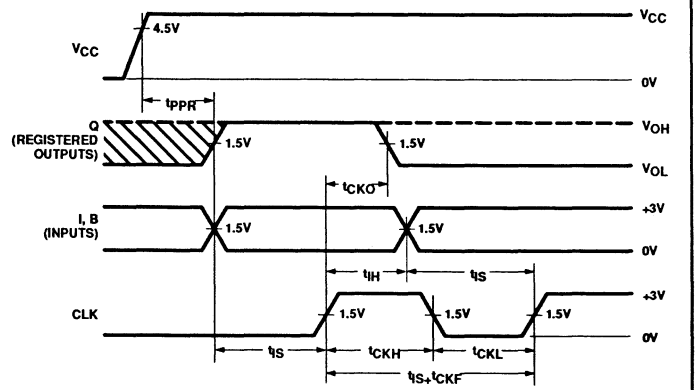
TIMING DIAGRAMS[1, 2]



Flip-Flop Outputs



Gate Outputs



Power-Up Reset

TIMING DEFINITIONS

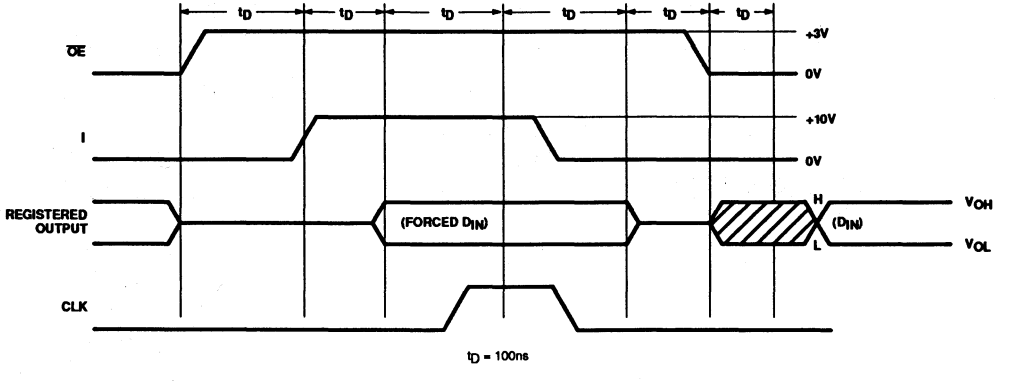
SYMBOL	PARAMETER
t_{CKH}	Width of input clock pulse.
t_{CKL}	Interval between clock pulses.
t_{CKP}	Clock period.
t_{IS}	Required delay between beginning of valid input and positive transition of clock.
t_{IH}	Required delay between positive transition of clock and end of valid input data.
t_{CKF}	Delay between positive transition of clock and when internal $\overline{Q}$ output of flip-flop becomes valid.
t_{CKO}	Delay between positive transition of clock and when outputs become valid (with $\overline{OE}$ Low).
t_{OE1}	Delay between beginning of Output Enable Low and when outputs become valid.
t_{OD1}	Delay between beginning of Output Enable High and when outputs are in the Off-State.
t_{OE2}	Delay between predefined Output Enable High, and when combinational outputs become valid.
t_{OD2}	Delay between predefined Output Enable Low and when combinational outputs are in the Off-State.
t_{PPR}	Delay between V_{CC} (after power-on) and when flip-flop outputs become preset at "1" (internal Q outputs at "0").
t_{PD}	Propagation delay between combinational inputs and outputs.
t_D	Delay between each input change

FREQUENCY DEFINITIONS

f_{MAX}	**No feedback:** Determined by the minimum clock period, $1/(t_{CKL} + t_{CKH})$. **Internal feedback:** Determined by the internal delay from flip-flop outputs through the internal feedback and array to the flip-flop inputs, $1/(t_{IS} + t_{CKF})$. **External feedback:** Determined by clock-to-output delay and input setup time, $1/(t_{IS} + t_{CKO})$.

NOTES:
1. Input pulse amplitude is 0V to 3V.
2. Input rise and fall times are 2.0ns typical.

TIMING DIAGRAMS (Continued)

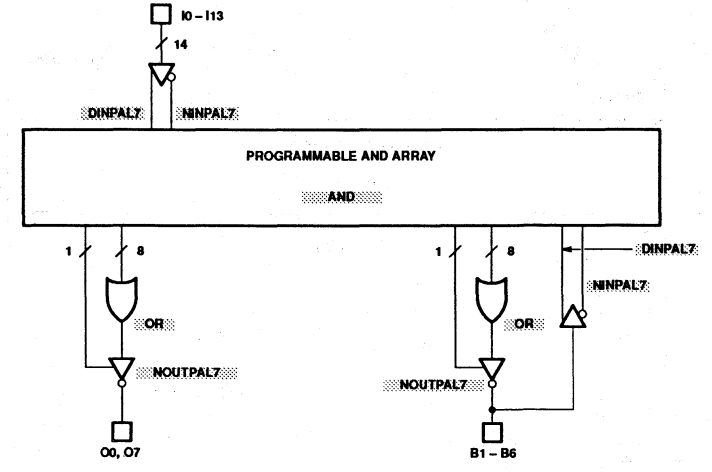


Output Register Preload

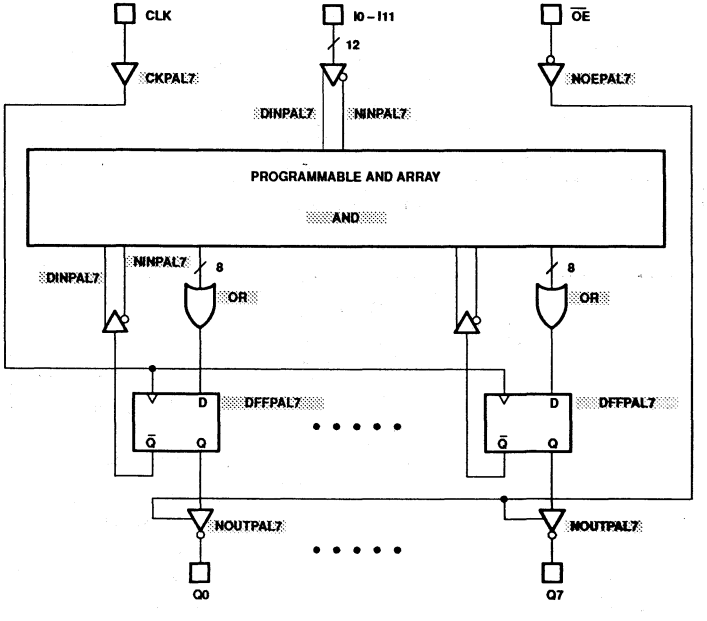
PROGRAMMING/SOFTWARE SUPPORT

Refer to Section 8 *(Development Software)* and Section 9 *(Third-Party Programmer/ Software Support)* for additional information.

SNAP RESOURCE SUMMARY DESIGNATIONS

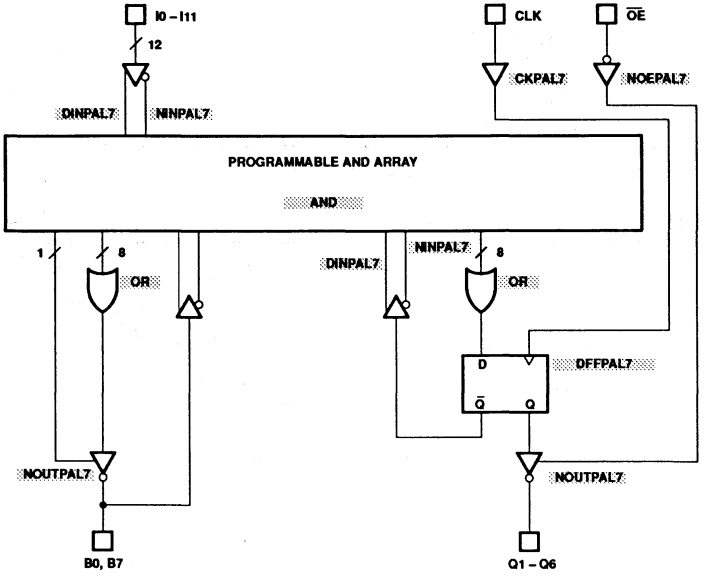


PLQ20L8

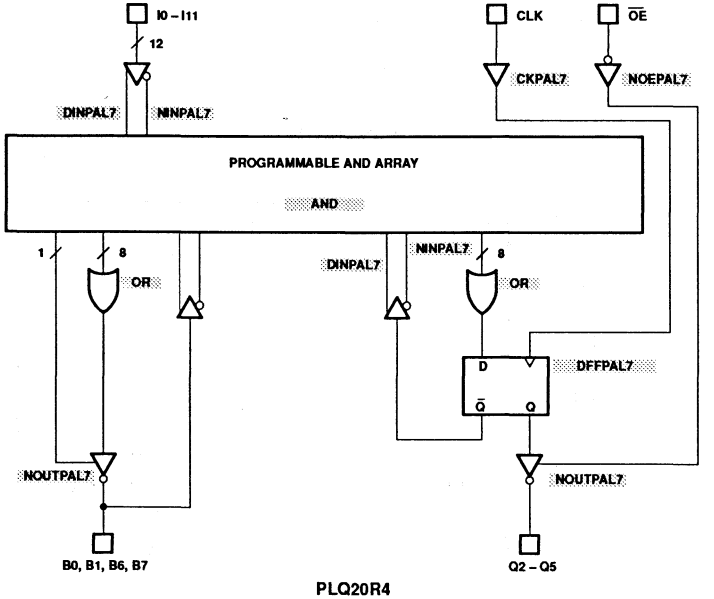


PLQ20R8

SNAP RESOURCE SUMMARY DESIGNATIONS (Continued)



PLQ20R6



PLQ20R4

CMOS programmable electrically erasable logic device

PL22V10-10/-12/-15, PL22V10I15

FEATURES

- Advanced CMOS EEPROM technology
- Ultra high performance
  - 10ns, 12ns, 15ns (t_{PD}) commercial versions
  - 15ns (t_{PD}) industrial version
  - f_{MAX} as fast as 83.3MHz
- Low power consumption
  - 110mA + 0.5mA/MHz max
- EE reprogrammability
  - Low-risk reprogrammable inventory
  - Superior programming and functional yield
  - 100% testable
  - Erases and programs in seconds
  - 100 guaranteed erase cycles
- Development and programming support
  - Third-party software and programmers
  - SLICE development software
- Architectural flexibility
  - 132 product term × 44 input AND array
  - Up to 22 inputs and 10 outputs
  - Variable product term distribution (8 to 16 per output) for greater logic flexibility
  - Independently programmable 4-configuration I/O macrocells
  - Synchronous preset, asynchronous clear
  - Independently programmable output enables
- Application versatility
  - Pin-for-pin and JEDEC-file compatible with the bipolar AmPAL22V10, CMOS PALC22V10 and PEEL22CV10A

DESCRIPTION

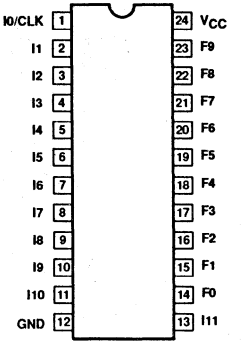
The Signetics PL22V10-10, PL22V10-12 and PL22V10-15 are CMOS programmable electrically erasable logic devices that provide a high-performance, low-power, reprogrammable, and architecturally enhanced alternative to early generation programmable logic devices (PLDs). Designed in advanced CMOS EEPROM technology, the PL22V10 rivals speed parameters of comparable bipolar PLDs while providing a dramatic improvement in active power consumption. The EE reprogrammability of the PL22V10 allows cost effective plastic packaging, low risk inventory, reduced development and retrofit costs, and enhanced testability to ensure 100% field programmability and function. The PL22V10's flexible architecture offers complete function and JEDEC-file compatibility with the bipolar AmPAL22V10 and the CMOS PALC22V10. Applications for the PL22V10 include: replacement of random SSI/MSI logic circuitry and user customized sequential and combinatorial functions such as counters, shift registers, state machines, address decoders, multiplexers, etc. Development and programming support for the PL22V10 is provided by Signetics and third-party manufacturers.

PIN LABEL DESCRIPTIONS

I1 – I11	Dedicated Input
NC	Not Connected
F0 – F9	Macro Cell Input/Output
CLK/I0	Clock Input/Dedicated Input
V_{CC}	Supply Voltage
GND	Ground

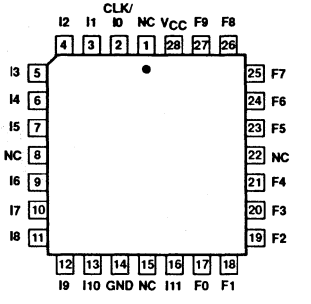
PIN CONFIGURATIONS

N Package



N = Plastic Dual In-Line Package (300mil-wide)

A Package

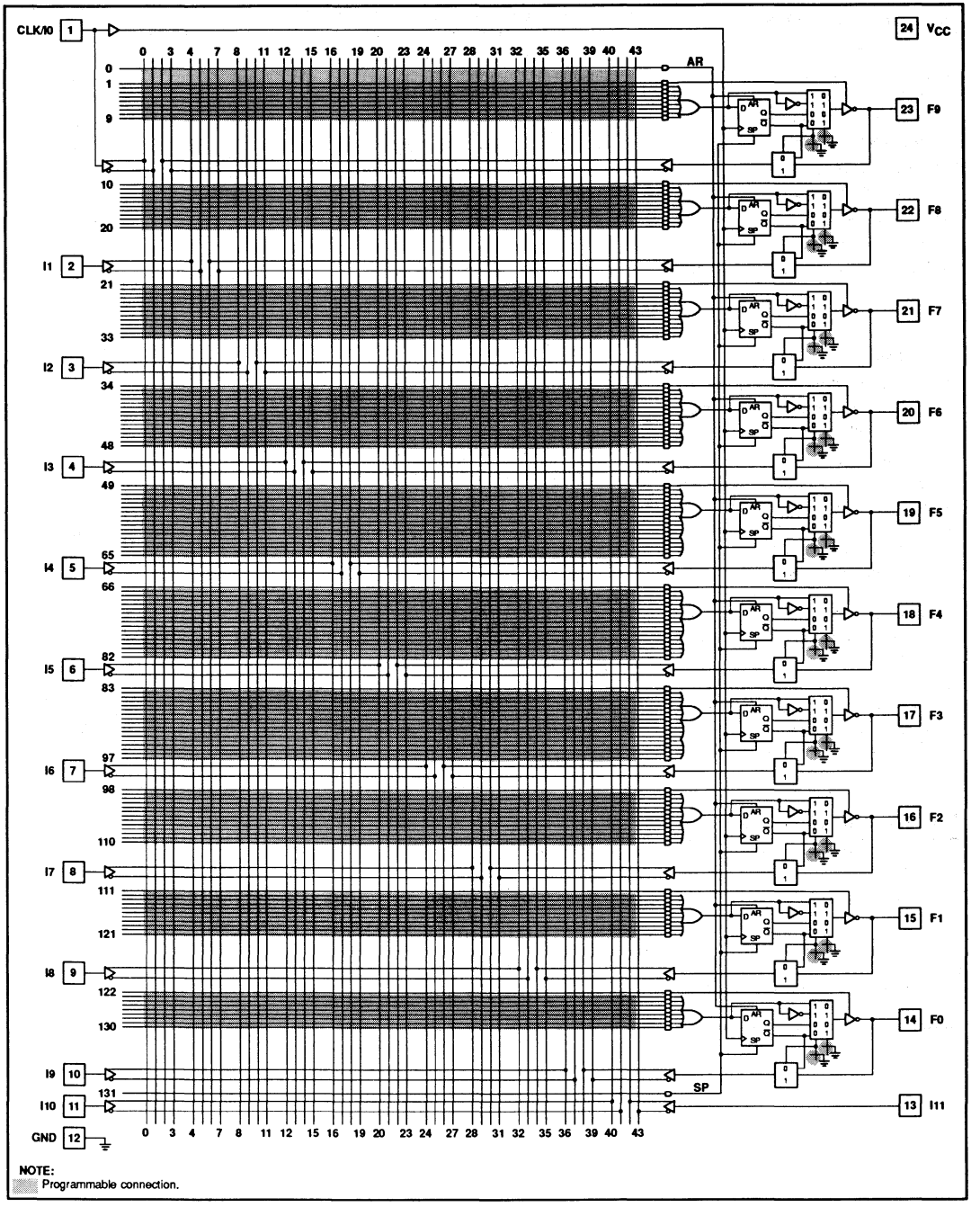


A = Plastic Leaded Chip Carrier

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-Pin Plastic Dual-In-Line 300mil-wide	PL22V10–10N PL22V10–12N PL22V10–15N PL22V10I15N
28-Pin Plastic Leaded Chip Carrier (PLCC)	PL22V10–10A PL22V10–12A PL22V10–15A PL22V10I15A

LOGIC DIAGRAM



NOTE:
Programmable connection.

CMOS programmable electrically erasable logic device

PL22V10-10/-12/-15, PL22V10I15

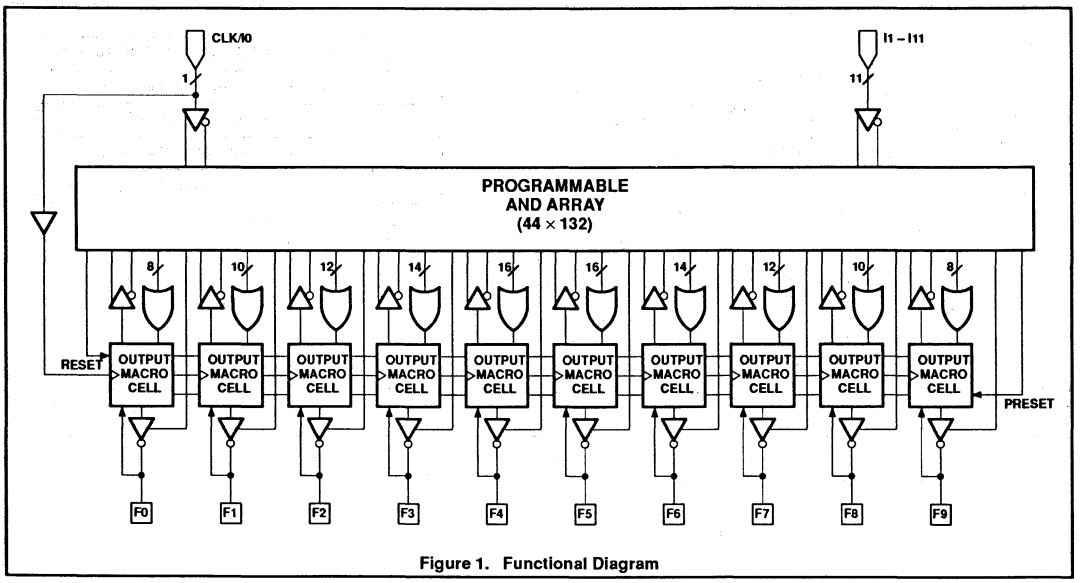


Figure 1. Functional Diagram

FUNCTION DESCRIPTION

The PL22V10 implements logic functions as sum-of-products expressions in a programmable-AND/fixed-OR logic array. User-defined functions are created by programming the connections of input signals into the array. User-configurable output structures in the form of I/O macrocells further increase logic flexibility.

ARCHITECTURE OVERVIEW

The PL22V10 architecture is illustrated in the Figure 1. Twelve dedicated inputs and 10 I/Os provide up to 22 inputs and 10 outputs for creation of logic functions. At the core of the device is a programmable electrically-erasable AND array which drives a fixed OR array. With this structure, the PL22V10 can implement up to 10 sum-of-products logic expressions.

Associated with each of the 10 OR functions is an I/O macro cell which can be independently programmed to one of 4 different configurations. The programmable macro cells allow each I/O to create sequential or combinatorial logic functions with either Active-High or Active-Low polarity.

AND/OR LOGIC ARRAY

The programmable AND array of the PL22V10 (shown in the Logic Diagram) is formed by input lines intersecting product terms. The input lines and product terms are used as follows:

44 input lines:

- 24 input lines carry the True and Complement of the signals applied to the 12 input pins
- 20 additional lines carry the True and Complement values of feedback or input signals from the 10 I/Os

132 product terms:

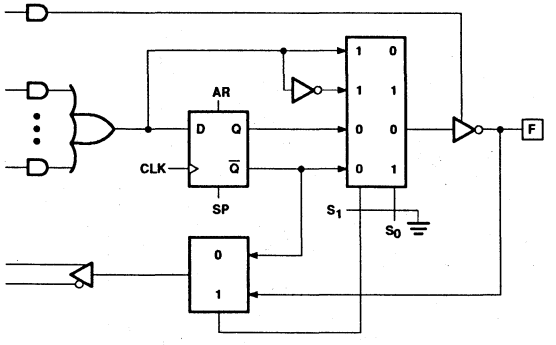
- 120 product terms (arranged in 2 groups of 8, 10, 12, 14, and 16) used to form logical sums
- 10 output enable terms (one for each I/O)
- 1 global synchronous preset term
- 1 global asynchronous clear term

At each input-line/product-term intersection there is an EEPROM memory cell which determines whether or not there is a logical connection at that intersection. Each product term is essentially a 44-input AND gate. A product term which is connected to both the True and Complement of an input signal will always be FALSE, and thus will not effect the OR function that it drives. When all the connections on a product term are opened, a Don't Care state exists and that term will always be TRUE.

When programming the PL22V10, the device programmer first performs a bulk erase to instantly remove the previous pattern. The erase cycle opens every logical connection in the array. The device is then configured to perform the user-defined function by programming selected connections in the AND array. (Note that EEPROM device programmers automatically program the connections on unused product terms so that they will have no effect on the output function.)

VARIABLE PRODUCT TERM DISTRIBUTION

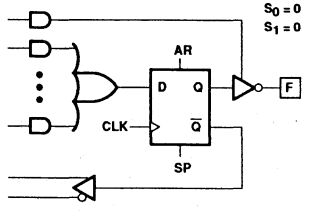
The PL22V10 provides 120 product terms to drive the 10 OR functions. These product terms are distributed among the outputs in groups of 8, 10, 12, 14, and 16 to form logical sums (see Logic Diagram). This distribution allows optimum use of device resources.



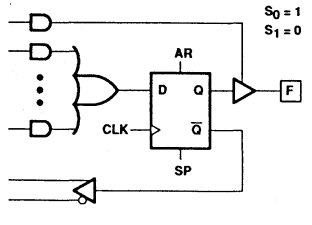
S_1	S_0	OUTPUT CONFIGURATION
0	0	Registered/Active-LOW
0	1	Registered/Active-HIGH
1	0	Combinatorial/Active-LOW
1	1	Combinatorial/Active-HIGH

0 = Unprogrammed fuse
1 = Programmed fuse

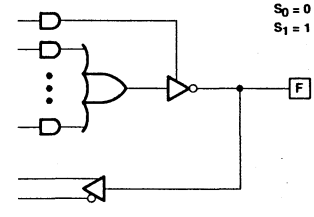
Figure 2. Output Macro Cell Logic Diagram



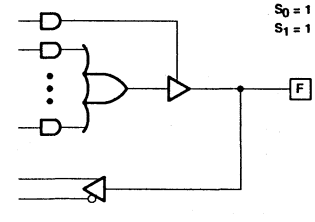
a. Registered/Active-LOW



b. Registered/Active-HIGH



c. Combinatorial/Active-LOW



d. Combinatorial/Active-HIGH

Figure 3.

PROGRAMMABLE I/O MACROCELL

The output macrocell provides complete control over the architecture of each output. The ability to configure each output independently permits users to tailor the configuration of the PL22V10 to the precise requirements of their designs.

MACROCELL ARCHITECTURE

Each I/O macrocell, as shown in Figure 2, consists of a D-type flip-flop and two signal-select multiplexers. The configuration of each macrocell of the PL22V10 is determined by the two EEPROM bits controlling these multiplexers. These bits determine output polarity, and output type (registered or non-registered). Equivalent circuits for the macrocell configurations are illustrated in Figure 3.

OUTPUT TYPE

The signal from the OR array can be fed directly to the output pin (combinatorial function) or latched in the D-type flip-flop (registered function). The D-type flip-flop latches data on the rising edge of the clock and is controlled by the global preset and clear terms. When the synchronous preset term is satisfied, the Q output of the register will be set HIGH at the next rising edge of the clock input. Satisfying the asynchronous clear term will set Q LOW, regardless of the clock state. If both terms are satisfied simultaneously, the clear will override the preset.

PROGRAM/ERASE CYCLES

The PL22V10 is 100% testable, erases/programs in seconds, and has 100 guaranteed erase cycles.

OUTPUT POLARITY

Each macrocell can be configured to implement Active-High or Active-Low logic. Programmable polarity eliminates the need for external inverters.

OUTPUT ENABLE

The output of each I/O macrocell can be enabled or disabled under the control of its associated programmable output enable product term. When the logical conditions programmed on the output enable term are satisfied, the output signal is propagated to the I/O pin. Otherwise, the output buffer is driven into the high-impedance state.

Under the control of the output enable term, the I/O pin can function as a dedicated input, a dedicated output, or a bi-directional I/O. Opening every connection on the output enable term will permanently enable the output buffer and yield a dedicated output. Conversely, if every connection is intact, the enable term will always be logically FALSE and the I/O will function as a dedicated input.

REGISTER FEEDBACK SELECT

When the I/O macrocell is configured to implement a registered function (S1=0) (Figures 3.a or 3.b), the feedback signal to the AND array is taken from the $\overline{Q}$ output.

BI-DIRECTIONAL I/O SELECT

When configuring an I/O macrocell to implement a combinatorial function (S1=1) (Figures 3.c or 3.d), the feedback signal is taken from the I/O pin. In this case, the pin can be used as a dedicated input, a dedicated output, or a bi-directional I/O.

POWER-ON RESET

To ease system initialization, all flip-flops will power-up to a reset condition and the Q output will be low. The actual output of the PL22V10 will depend on the programmed output polarity. The V_{CC} rise must be monotonic and the reset delay time is 5µs maximum.

DESIGN SECURITY

The PL22V10 provides a special EEPROM security bit that prevents unauthorized reading or copying of designs programmed into the device. The security bit is set by the PLD programmer, either at the conclusion of the programming cycle or as a separate step, after the device has been programmed. Once the security bit is set it is impossible to verify (read) or program the PL22V10 until the entire device has first been erased with the bulk-erase function.

PROGRAM AND ERASE

The PL22V10 can be programmed on standard logic programmers. If a device needs to be reprogrammed, simply place back into the programmer, at which point it will be automatically erased, then repatterened.

Approved programmers are listed in the Signetics Programmer Reference Guide.

SOFTWARE SUPPORT

The PL22V10 is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Signetics' SLICE and SNAP design software packages. ABEL™, CUPL™, and PALASM® 90 design software packages also support the PL22V10 architecture.

All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

PL22V10 logic designs can also be generated using the program table entry format, which is detailed on the following pages. This program table entry format is supported by SLICE only. The SLICE design package is available, free of charge, to qualified users.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	CONDITIONS	RATINGS		UNIT
			MIN	MAX	
V_{CC}	Supply voltage	Relative to GND	–0.5	+7.0	V
V_{IN}, V_{OUT}	Voltage applied to any pin[3]	Relative to GND[2]	–1.2	V_{CC} + 0.5	V_{DC}
I_{OUT}	Output current	Per pin (I_{OL}, I_{OH})	±25		mA
T_{stg}	Storage temperature range		–65	+125	°C
T_{LT}	Lead temperature	Soldering 10 seconds	+300		°C

NOTES:
1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.
2. Minimum DC input is –0.5V, however inputs may undershoot to –2.0V for periods less than 20ns.
3. V_{IN} and V_{OUT} are not specified for program/verify operation.

OPERATING RANGES

SYMBOL	PARAMETER	CONDITIONS	RATINGS		UNIT
			MIN	MAX	
V_{CC}	Supply voltage	Commercial[1]	+4.75	+5.25	V_{DC}
		Industrial	+4.5	+5.5	V_{DC}
T_{amb}	Ambient temperature	Commercial[1]	0	+70	°C
		Industrial	–40	+85	°C
t_R	Clock Rise Time	See note 2		250	ns
t_F	Clock Fall Time	See note 2		250	ns
t_{RVCC}	V_{CC} Rise Time	See note 2		250	ms

NOTES:
1. Voltage applied to input or output must not exceed V_{CC} +0.3V.
2. Test points for Clock and V_{CC} in t_R, t_F, t_{CL}, t_{CH}, and t_{RESET} are referenced at 10% and 90% levels.

DC ELECTRICAL CHARACTERISTICS

Commercial = 0°C ≤ T_{amb} ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V;
Industrial = –40°C ≤ T_{amb} ≤ +85°C, 4.5V ≤ V_{CC} ≤ 5.5V

SYMBOL	PARAMETER	CONDITIONS	LIMITS			UNIT
			MIN	TYP[4]	MAX	
Input voltage						
V_{IL}	Low		–0.3		0.8	V
V_{IH}	High		2.0		V_{CC} + 0.3	V
Output voltage						
V_{OL}	Low – TTL	V_{CC} = MIN, I_{OL} = 16mA			0.5	V
V_{OLC}	Low – CMOS	V_{CC} = MIN, I_{OL} = 10μA			0.1	V
V_{OH}	High – TTL	V_{CC} = MIN, I_{OH} = –4.0mA	2.4			V
V_{OHC}	High – CMOS	V_{CC} = MIN, I_{OH} = –10μA	V_{CC} – 0.1			V
Input current						
I_{IL}/I_{IH}	Input leakage current	V_{CC} = MAX, GND ≤ V_{IN} ≤ V_{CC}		1	±10	μA
Output current						
I_{OZ}	Output leakage	I/O = Hi-Z, GND ≤ V_O ≤ V_{CC}		2	±10	μA
I_{SC}[5]	Short circuit	V_{CC} = 5V, V_{OUT} = 0.5V[1]	–30		–130	mA
I_{CC}	V_{CC} active current, CMOS (commercial)	V_{IN} = V_{CC} or GND[2, 3]		80 + 0.5mA/MHz	110 + 0.5mA/MHz	mA
	V_{CC} active current, CMOS (industrial)	V_{IN} = V_{CC} or GND[2, 3]		90 + 0.5mA/MHz	120 + 0.5mA/MHz	mA
	V_{CC} active current, TTL (commercial)	V_{IN} = V_{IL} or V_{IH}[2, 3]		90 + 0.5mA/MHz	120 + 0.5mA/MHz	mA
	V_{CC} active current, TTL (industrial)	V_{IN} = V_{IL} or V_{IH}[2, 3]		100 + 0.5mA/MHz	130 + 0.5mA/MHz	mA

NOTES:
1. No more than one output should be tested at a time. Duration of the short-circuit test should not exceed one second.
2. I/O pins open (no load).
3. I_{CC} for a typical application: This parameter is tested with the device programmed as a 10-bit Counter.
4. Typical values are at V_{CC} = 5V. Typical values are guaranteed by design.
5. Room temperature only.

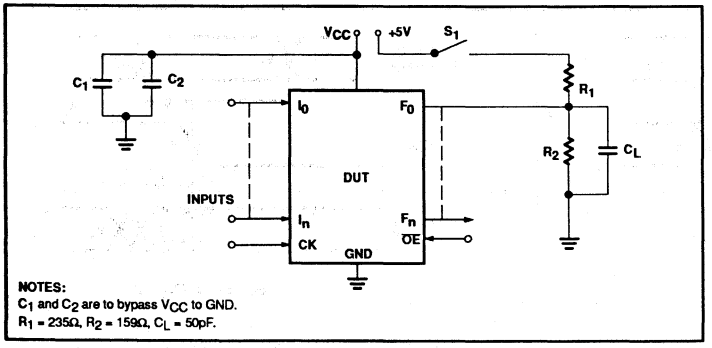
AC ELECTRICAL CHARACTERISTICS

Commercial = $0°C \le T_{amb} \le +75°C$, $4.75V \le V_{CC} \le 5.25V$[1,2];
Industrial = $-40°C \le T_{amb} \le +85°C$, $4.5V \le V_{CC} \le 5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS	PL22V10-10		PL22V10-12		PL22V10-15 PL22V10I15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PD}	Input[3] to non-registered output	50pF		10		12		15	ns
t_{EA}	Input[3] to Output Enable[4]	50pF		10		12		15	ns
t_{ER}	Input[3] to Output Disable[4]	5pF		10		12		15	ns
t_{CO}	Clock to output	50pF		8		9		10	ns
t_{CO2}	Clock to combinatorial output delay via internal registered feedback	50pF		14		16		19	ns
t_S	Input[3] or feedback setup to clock	50pF	7		8		10		ns
t_{SF}	Internal feedback[6]	50pF	5		6		9		ns
t_H	Input[3] hold after clock	50pF	0		0		0		ns
t_{WL}, t_{WH}	Clock width – clock low time, clock high time[5]	50pF	6		7		8		ns
t_{CP}	MIN clock period External ($t_S + t_{CO}$)	50pF	15		17		20		ns
f_{MAX1}	MAX operating frequency; Internal feedback[6] $\left(\frac{1}{t_{SF} + t_{CO}}\right)$	50pF	76.9		66.7		52.6		MHz
f_{MAX2}	MAX operating frequency; External ($1/t_{CP}$)	50pF	66.6		58.8		50.0		MHz
f_{MAX3}	MAX clock frequency; No feedback[6] $\left(\frac{1}{t_{WL} + t_{WH}}\right)$	50pF	83.3		71.4		62.5		MHz
t_{ARW}	Asynchronous Reset pulse width	50pF	10		12		15		ns
t_{AR}	Input[3] to Asynchronous Reset	50pF		12		15		18	ns
t_{ARR}	Asynchronous Reset recovery time	50pF	12		15		18		ns
t_{SPR}	Synchronous Preset recovery time	50pF	12		15		18		ns
t_{RESET}	Power-on reset time for registers in clear state[5]	50pF		5		5		5	µs
Capacitance[6]									
C_{IN}	Input Capacitance[7]	$T_{amb} = 25°C$, $V_{CC} = 5.0V$		6		6		6	pF
C_{OUT}	Output Capacitance[7]	@ f = 1MHz		12		12		12	pF

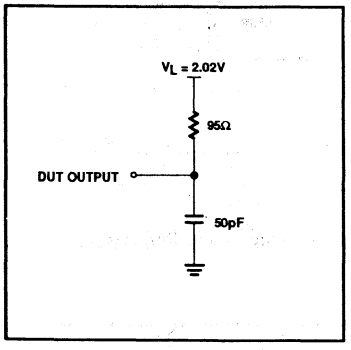
NOTES:
1. Test conditions assume: signal transition times of 2.5ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
2. Device test loads are specified at the end of this section.
3. "Input" refers to an Input pin signal.
4. t_{OE} is measured from input transition to $V_{REF} \pm 0.1V$, t_{OD} is measured from input transition to $V_{OH} - 0.1V$ or $V_{OL} + 0.1V$.
5. Test points for Clock and V_{CC} in t_R, t_F, t_{CL}, t_{CH}, and t_{RESET} are referenced at 10% and 90% levels.
6. Parameters are not 100% tested. Specifications are based on initial characterization and are tested after any design or process modification which may affect operational frequency.
7. Capacitances are tested on a sample basis.

TEST LOAD CIRCUIT

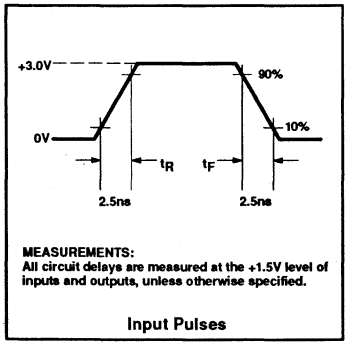


NOTES:
C_1 and C_2 are to bypass V_{CC} to GND.
R_1 = 235Ω, R_2 = 159Ω, C_L = 50pF.

THEVENIN EQUIVALENT



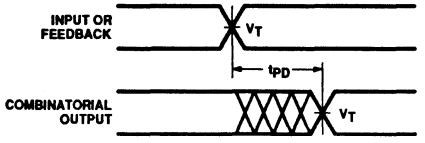
VOLTAGE WAVEFORM



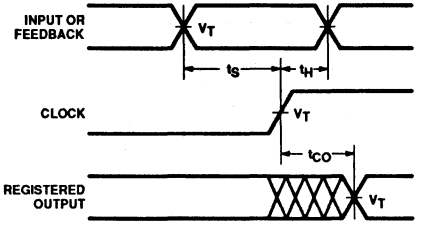
MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

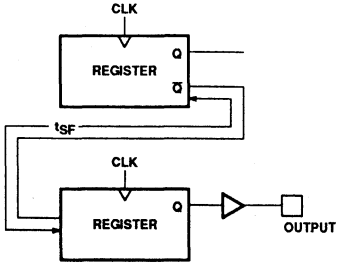
SWITCHING WAVEFORMS



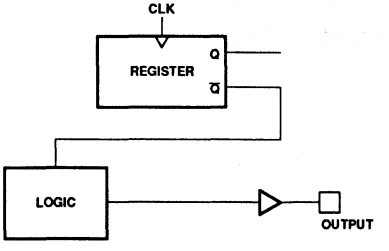
Combinatorial Output



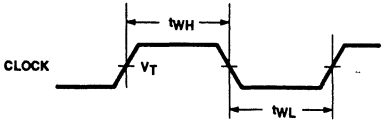
Registered Output



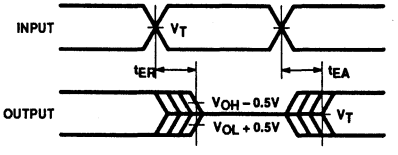
f_{MAX1}; Internal Feedback $\left(\frac{1}{t_{SF} + t_{CO}}\right)$



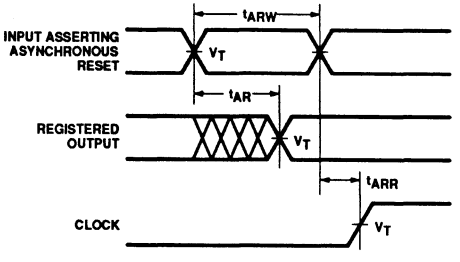
Clock to Combinatorial Output (t_{CO2})



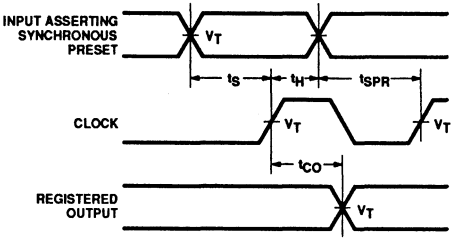
Clock Width



Input to Output Disable/Enable



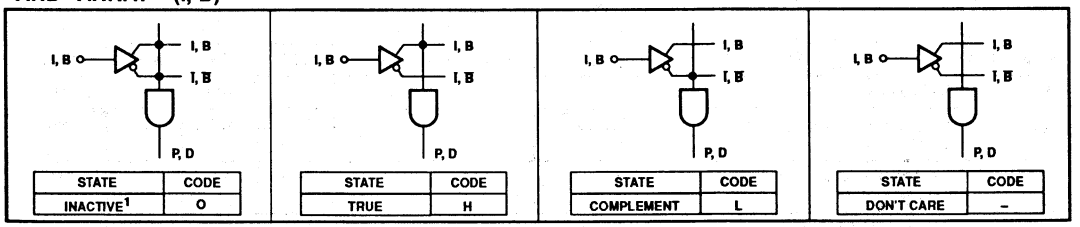
Asynchronous Reset



Synchronous Preset

NOTES:
1. V_T = 1.5V.
2. Input pulse amplitude 0V to 3.0V.
3. Input rise and fall times 2.5ns max.

"AND" ARRAY – (I, B)



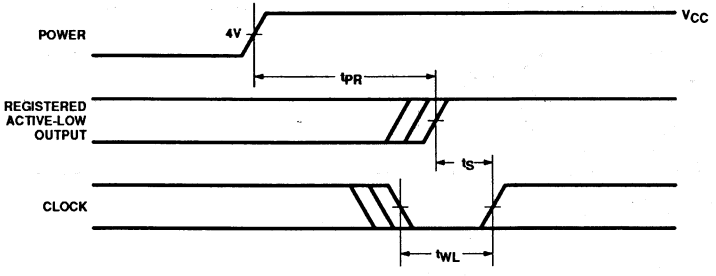
NOTE:
1. This is the initial state.

POWER-UP RESET

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will depend on the programmed pattern. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
t_{PR}	Power-up Reset Time		1	µs
t_S, t_{SF}	Input or Feedback Setup Time	See AC Electrical Characteristics		
t_{WL}	Clock Width LOW			

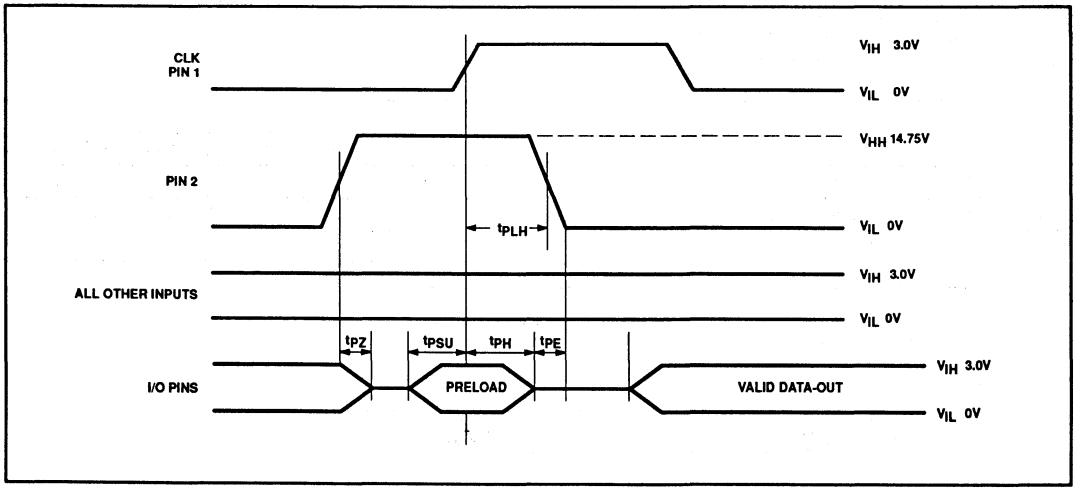


Power-Up Reset Waveform

PRELOAD TEST CONDITION

SYMBOL	PARAMETER	CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
t_{PE}	Valid data out			100		ns
t_{PZ}	Output 3-State delay time after assertion of Preload (Pin 2 = V_{HH})			100		ns
t_{PH}	Hold time of all preload inputs with respect to Clock rising edge			15		ns
t_{PSU}	Setup time of all preload inputs with respect to Clock rising edge			100		ns
t_{PLH}	Hold time for Preconditioning input			50		ns
V_{HH}	Preload enable voltage		14.50	14.75	15.0	V

PRELOAD WAVEFORM



CMOS programmable electrically erasable logic device

PL22V10-10/-12/-15, PL22V10I15

PROGRAM TABLE

B – COMBINATORIAL
D – REGISTERED
CONTROL WORD

POLARITY: H → ACTIVE HIGH; L → ACTIVE LOW

TERM	AND I 11	10	9	8	7	6	5	4	3	2	1	0	F(I) 9	8	7	6	5	4	3	2	1	0	POLARITY F(O) 9	8	7	6	5	4	3	2	1	0
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1																							A								
2																							A								
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PIN	13	11	10	9	8	7	6	5	4	3	2	1	23	22	21	20	19	18	17	16	15	14										
VARIABLE NAME																																

PROGRAM TABLE (Continued)

TERM	AND I 11	10	9	8	7	6	5	4	3	2	1	0	AND F(I) 9	8	7	6	5	4	3	2	1	0	F(O) 9	8	7	6	5	4	3	2	1	0
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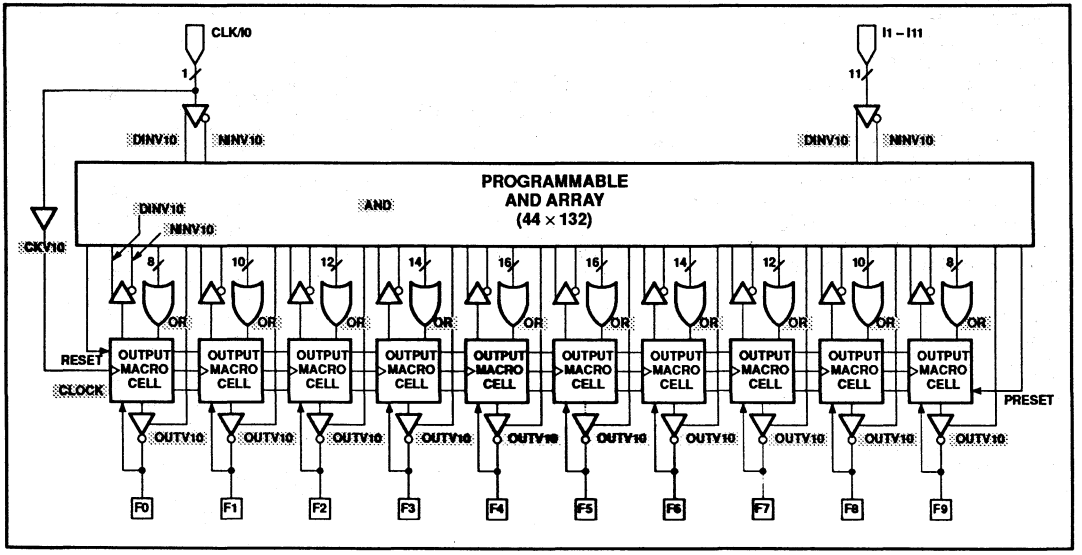
128																																A
129																																A
AR																																
SP																																
PIN	13	11	10	9	8	7	6	5	4	3	2	1	23	22	21	20	19	18	17	16	15	14										
VARIABLE NAME																																

SNAP RESOURCE SUMMARY DESIGNATIONS



BiCMOS versatile PLD device

PLQ22V10-7

DESCRIPTION

The PLQ22V10 is a versatile PAL device fabricated through the use of our BiCMOS process known as QUBiC. This is an excellent device where fast propagation delays are required.

The PLQ22V10 uses the familiar AND/OR logic array structure, which allows direct implementation of sum-of-product equations. This device has a programmable AND array driving a fixed OR array. This AND array is programmed to create custom product terms while the fixed OR array sums selected terms at the output.

The OR sum of the products feeds the "Output Macro Cell" (OMC) which can be individually configured as a dedicated input, a combinatorial output, or a registered output with internal feedback. In other words, the architecture provides maximum design flexibility by allowing the Output Macro Cell to be configured by the user.

This device is pin and JEDEC file compatible with industry standard 22V10 and can be used in all standard applications where speed is to be maximized.

Order codes can be found in the Ordering Information table.

FEATURES

- Ultra fast 7.5ns t_{PD} and 6ns t_{CKO}
- Pin and JEDEC file compatible to industry standard 22V10
- 24-Pin Versatile Programmable Array Logic
- 10 input/output macro cells for architectural flexibility
- Varied product term distribution with up to 16 product terms per output for complex functions
- Programmable output polarity
- Power-up reset on all registers
- Synchronous Preset/Asynchronous Reset
- Programmable on standard PAL-type device programmers
- Design support provided using SNAP or SLICE software development packages and other CAD tools for PLDs
- Available in 300mil-wide 24-Pin Plastic DIP and 28-Pin PLCC

APPLICATIONS

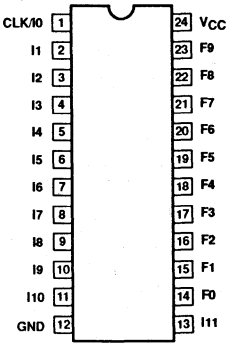
- DMA control
- State machine implementation
- High speed graphics processing
- Counters/shift registers
- SSI/MSI random logic replacement
- High speed memory decoder

PIN LABEL DESCRIPTIONS

I1 – I11	Dedicated Input
NC	Not Connected
F0 – F9	Macro Cell Input/Output
CLK/I0	Clock Input/Dedicated Input
V_{CC}	Supply Voltage
GND	Ground

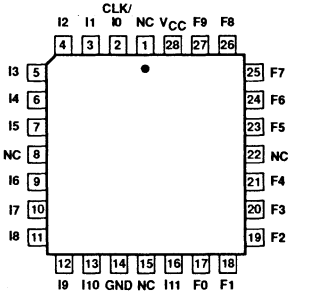
PIN CONFIGURATIONS

F and N Packages



N = Plastic DIP (300mil-wide)
F = Ceramic DIP (300mil-wide)

A Package



A = Plastic Leaded Chip Carrier

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-Pin Plastic Dual-In-Line 300mil-wide	PLQ22V10–7N
24-Pin Ceramic Dual-In-Line 300mil-wide	PLQ22V10–7F
28-Pin Plastic Leaded Chip Carrier (PLCC)	PLQ22V10–7A

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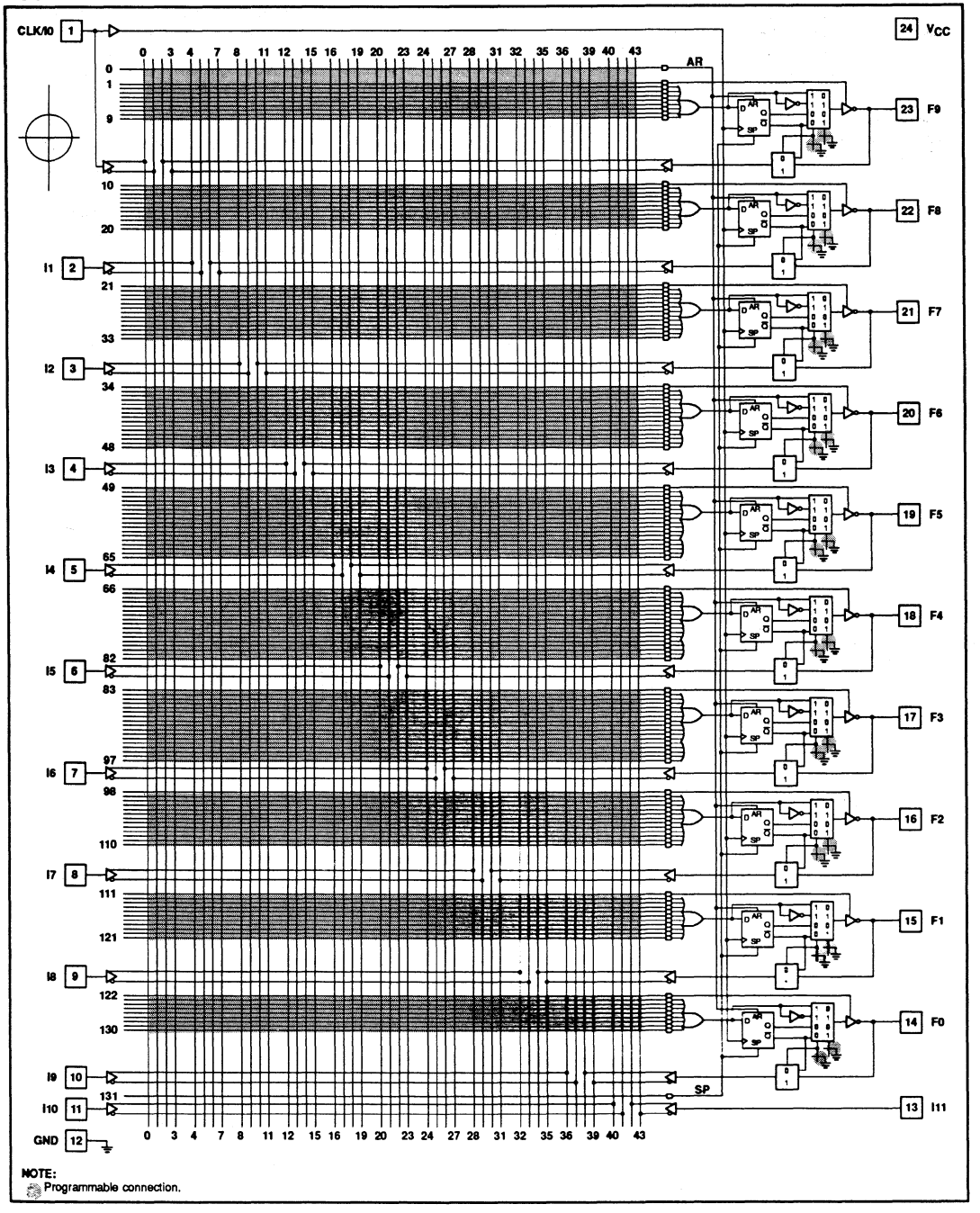
LOGIC DIAGRAM



NOTE:
Programmable connection.

FUNCTIONAL DESCRIPTION

The PLQ22V10 allows the systems engineer to implement the design on-chip, by opening fuse links to configure AND and OR gates within the device, according to the desired logic function.

Product terms with all fuses opened assume the logical HIGH state; product terms connected to both True and Complement of any single input assume the logical LOW state.

The PLQ22V10 has 12 inputs and 10 I/O Macro Cells (Figure 1). The Macro Cell allows one of four potential output configurations, registered output or combinatorial I/O, Active-HIGH or Active-LOW (see Figure 2). The configuration choice is made according to the user's design specification and corresponding programming of the configuration bits $S_0 - S_1$. Multiplexer controls are connected to ground (0) through a programmable fuse link, selecting the "0" path through the multiplexer. Programming the fuse disconnects the control line from GND and it floats to V_{CC} (1), selecting the "1" path.

The device is produced with a fuse link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit. Utilizing an easily-implemented programming algorithm, these products can be rapidly programmed to any customized pattern. Information on approved programmers can be found in the Programmer Reference Guide. Extra test fuses are pre-programmed during manufacturing to ensure extremely high field programming yields, and provide extra test paths to achieve excellent parametric correlation.

Variable Input/Output Pin Ratio

The PLQ22V10 has twelve dedicated input lines, and each Macro Cell output can be an I/O pin. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied to V_{CC} or GND.

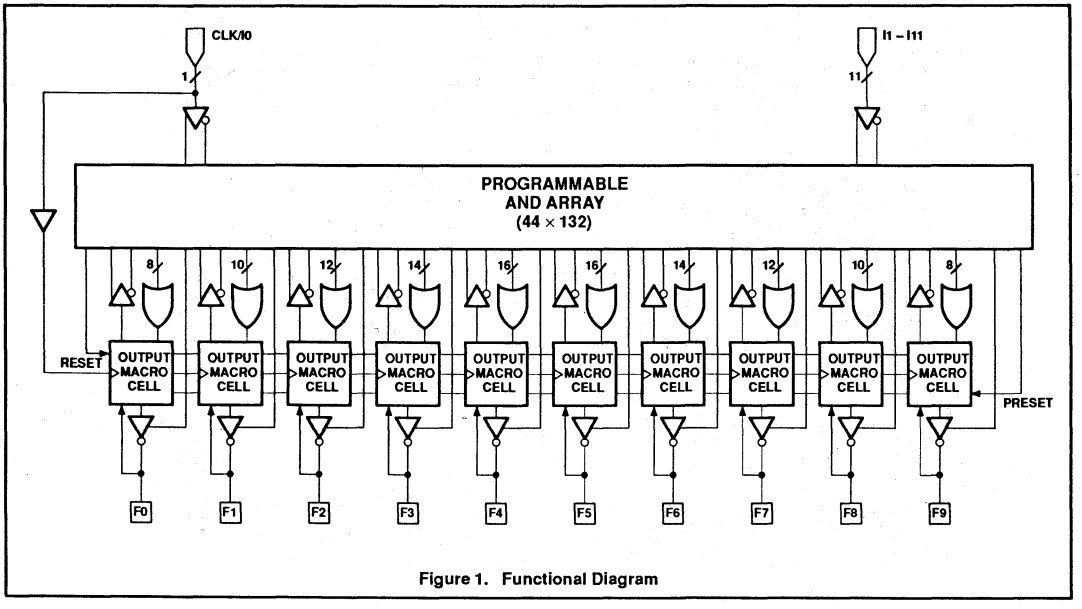
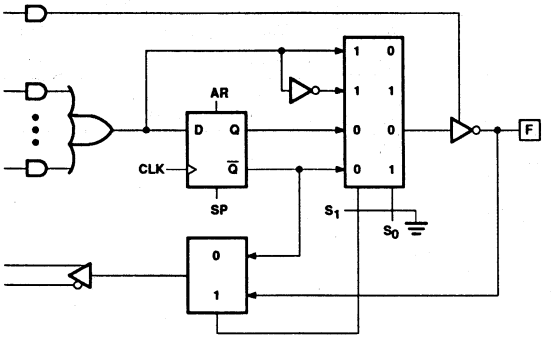


Figure 1. Functional Diagram

OUTPUT MACRO CELL



S_1	S_0	OUTPUT CONFIGURATION
0	0	Registered/Active-LOW
0	1	Registered/Active-HIGH
1	0	Combinatorial/Active-LOW
1	1	Combinatorial/Active-HIGH

0 = Unprogrammed fuse
1 = Programmed fuse

Figure 2. Output Macro Cell Logic Diagram

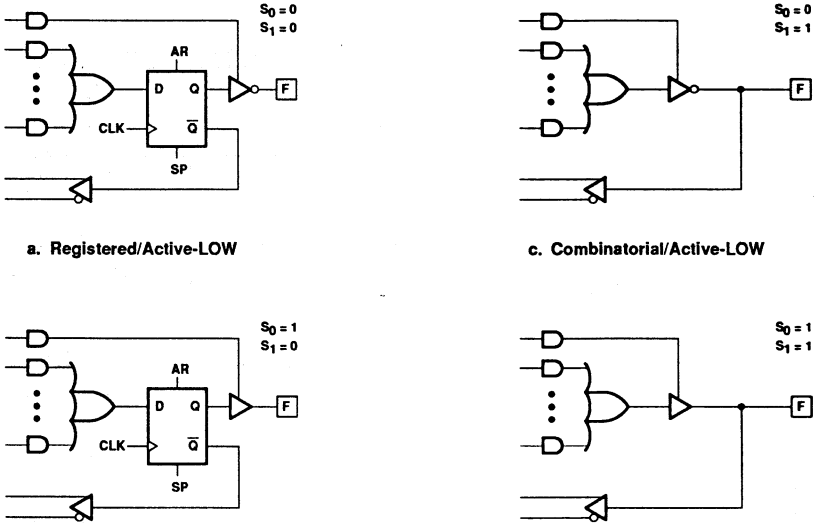


Figure 3.

Registered Output Configuration

Each Macro Cell of the PLQ22V10 includes a D-type flip-flop for data storage and synchronization. The flip-flop is loaded on the LOW-to-HIGH transition of the clock input. In the registered configuration (S_1 = 0), the array feedback is from $\overline{Q}$ of the flip-flop.

Combinatorial I/O Configuration

Any Macro Cell can be configured as combinatorial by selecting the multiplexer path that bypasses the flip-flop (S_1 = 1). In the combinatorial configuration, the feedback is from the pin.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS MIN	RATINGS MAX	UNIT
V_{CC}	Supply voltage	–0.5	+7.0	V_{DC}
V_{IN}	Input voltage	–1.2	V_{CC} + 0.5	V_{DC}
V_{OUT}	Output voltage	–0.5	V_{CC} + 0.5	V_{DC}
I_{IN}	Input currents	–30	+30	mA
I_{OUT}	Output currents		+100	mA
T_{stg}	Storage temperature range	–65	+150	°C

NOTE:
1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

OPERATING RANGES

SYMBOL	PARAMETER	RATINGS MIN	RATINGS MAX	UNIT
V_{CC}	Supply voltage	+4.75	+5.25	V_{DC}
T_{amb}	Operating free-air temperature	0	+75	°C

DC ELECTRICAL CHARACTERISTICS Over commercial operating range unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS[1]	LIMITS MIN	LIMITS MAX	UNIT
Input voltage					
V_{IL}	Low	V_{CC} = MIN		0.8	V
V_{IH}	High	V_{CC} = MAX	2.0		V
V_I	Clamp	V_{CC} = MIN, I_{IN} = –18mA		–1.2	V
Output voltage					
		V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}			
V_{OL}	Low	I_{OL} = 16mA		0.5	V
V_{OH}	High	I_{OH} = –3.2 mA	2.4		V
Input current					
		V_{CC} = MAX			
I_{IL} (except Pin 1)	Low	V_{IN} = 0.40V		–100	µA
I_{IL} (Pin 1)	Low	V_{IN} = 0.40V		–150	µA
I_{IH}	High	V_{IN} = 2.7V		25	µA
I_I	Maximum input current	V_{IN} = 5.5V		1.0	mA
Output current					
		V_{CC} = MAX			
I_{OZH}	Output leakage[3]	V_{IN} = V_{IL} or V_{IH}, V_{OUT} = 2.7V		100	µA
I_{OZL}	Output leakage[3]	V_{IN} = V_{IL} or V_{IH}, V_{OUT} = 0.4V		–100	µA
I_{SC}	Short circuit[2]	V_{OUT} = 0.5V	–30	–130	mA
I_{CC}	V_{CC} supply current	V_{CC} = MAX		210	mA

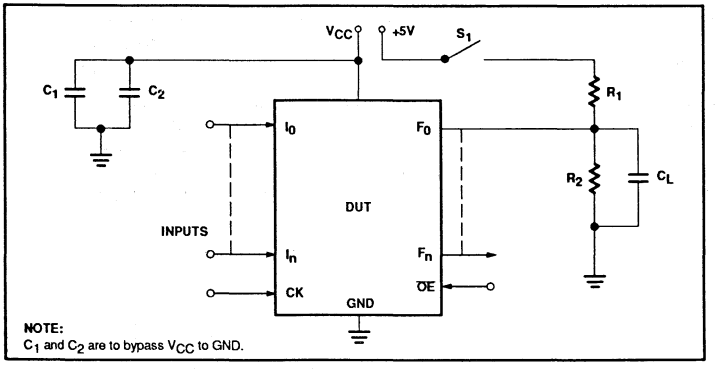
NOTES:
1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. No more than one output should be tested at a time. Duration of the short-circuit test should not exceed one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
3. I/O pin leakage is the worst case of I_{OZX} or I_{IX} (where X = H or L).

AC ELECTRICAL CHARACTERISTICS Over commercial operating range unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS[1] MIN	TYP	MAX	UNIT
t_{PD}	Input or feedback to non-registered output[2]	Active-LOW				7.5	
		Active-HIGH				7.5	ns
t_S	Setup time from input, feedback or SP to Clock			5.5			ns
t_H	Hold time			0			ns
t_{CO}	Clock to output					6.0	ns
t_{CF}	Clock to feedback[3]					2.5	ns
t_{AR}	Asynchronous Reset to registered output					10.0	ns
t_{ARW}	Asynchronous Reset width			7.5			ns
t_{ARR}	Asynchronous Reset recovery time			5.5			ns
t_{SPR}	Synchronous Preset recovery time			5.5			ns
t_{WL}	Width of Clock LOW			4.0			ns
t_{WH}	Width of Clock HIGH			4.0			ns
f_{MAX}	Maximum frequency; External feedback $1/(t_S + t_{CO})$[4]			87			MHz
	Maximum frequency; Internal feedback $1/(t_S + t_{CF})$[4]			125			MHz
t_{EA}	Input to Output Enable[5]					9.0	ns
t_{ER}	Input to Output Disable[5]					9.0	ns
Capacitance[6]							
C_{IN}	Input Capacitance (Pin 1)	V_{IN} = 2.0V	V_{CC} = 5.0V		6		pF
	Input Capacitance (Others)	V_{IN} = 2.0V	T_{amb} = 25°C		6		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V	f = 1MHz		8		pF

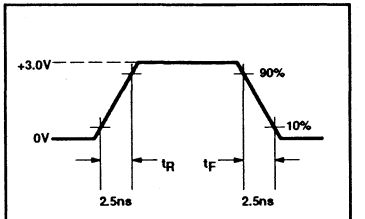
NOTES:
1. Commercial Test Conditions: R_1 = 300Ω, R_2 = 390Ω (see Test Load Circuit).
2. t_{PD} is tested with switch S_1 closed and C_L = 50pF (including jig capacitance). V_{IH} = 3V, V_{IL} = 0V, V_T = 1.5V.
3. Calculated from measured f_{MAX} internal.
4. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
5. For 3-State output; output enable times are tested with C_L = 50pF to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with C_L = 5pF. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} - 0.5V)$ with S_1 open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with S_1 closed.
6. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modifed where capacitance may be affected.

TEST LOAD CIRCUIT



NOTE:
C_1 and C_2 are to bypass V_{CC} to GND.

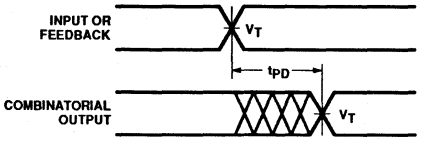
VOLTAGE WAVEFORM



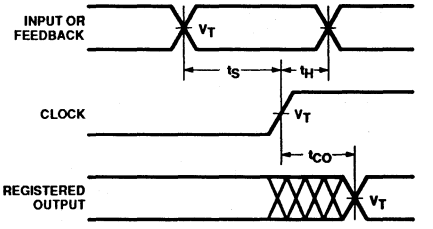
MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

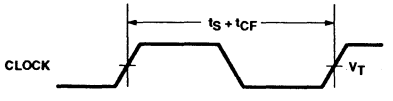
SWITCHING WAVEFORMS



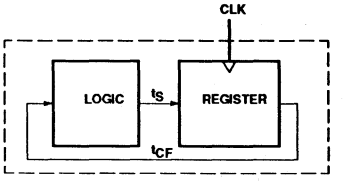
Combinatorial Output

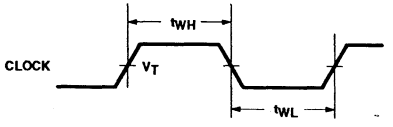


Registered Output

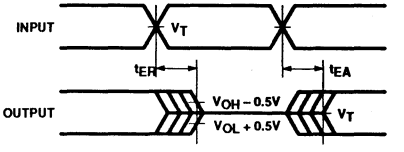


Clock to Feedback (f_{MAX} Internal)
(See Path at Right)

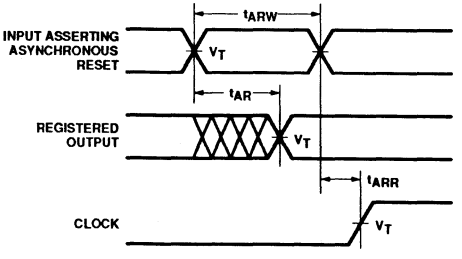




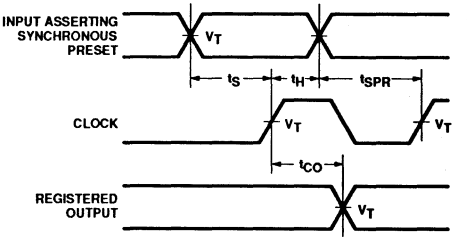
Clock Width



Input to Output Disable/Enable



Asynchronous Reset



Synchronous Preset

NOTES:
1. V_T = 1.5V.
2. Input pulse amplitude 0V to 3.0V.
3. Input rise and fall times 2.5ns max.

Programmable 3-State Outputs

Each output has a 3-State output buffer with 3-State control. A product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin, and may be configured as a dedicated input if the buffer is always disabled.

Programmable Output Polarity

The polarity of each macro cell output can be Active-HIGH or Active-LOW, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

Selection is controlled by programmable bit S_0 in the Output Macro Cell, and affects both registered and combinatorial outputs. Selection is automatic, based on the design specification and pin definitions. If the pin definition and output equation have the same polarity, the output is programmed to be Active-HIGH ($S_0 = 1$).

Preset/Reset

For initialization, the PLQ22V10 has additional Preset and Reset product terms. These terms are connected to all registered outputs. When the Synchronous Preset (SP) product term is asserted high, the output registers will be loaded with a HIGH on the next LOW-to-HIGH clock transition. When the Asynchronous Reset (AR) product term is asserted high, the output registers will be immediately loaded with a LOW independent of the clock.

Note that Preset and Reset control the flip-flop, not the output pin. The output level is determined by the output polarity selected.

Power-Up Reset

All flip-flops power-up to a logic LOW for predictable system initialization. Outputs of the PLQ22V10 will depend on the programmed output polarity. The V_{CC} rise must be monotonic and the reset delay time is 1–10μs maximum.

Register Preload

The register on the PLQ22V10 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Fuse

After programming and verification, a PLQ22V10 design can be secured by programming the security fuse link. Once programmed, this fuse defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security fuse is programmed, the array will read as if every fuse is programmed.

Quality and Testability

The PLQ22V10 offers a very high level of built-in quality. Extra programmable fuses provide a means of verifying performance of all AC and DC parameters. In addition, this verifies programmability and functionality of the device to provide the highest programming and post-programming functional yields.

Technology

The BiCMOS PLQ22V10 is fabricated with the Philips Semiconductors–Signetics process known as QUBiC. QUBiC combines an advanced, state-of-the-art 1.0μm (drawn feature size) CMOS process with an ultra fast bipolar process to achieve superior speed and drive capabilities. QUBiC incorporates three layers of Al/Cu interconnects for reduced chip size, and our proven Ti-W fuse technology ensures highest programming yields.

Programming

The PLQ22V10–7 is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Signetics' SLICE and SNAP design software packages. ABEL™ CUPL™ and PALASM® 90 design software packages also support the PLQ22V10–7 architecture.

All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

PLQ22V10–7 logic designs can also be generated using the program table entry format, which is detailed on the following pages. This program table entry format is supported by SLICE only. The SLICE design package is available, free of charge, to qualified users.

PROGRAMMING/SOFTWARE SUPPORT

Refer to Section 8 *(Development Software)* and Section 9 *(Third-Party Programming Support)* of this data handbook for additional information.

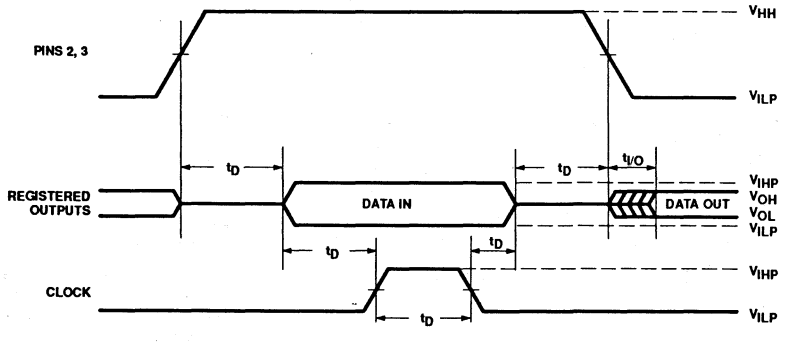
ABEL is a trademark of Data I/O Corp.
CUPL is a trademark of Logical Devices, Inc.
PALASM is a registered trademark of AMD Corp.

OUTPUT REGISTER PRELOAD

The preload function allows the registers to be loaded from the output pins. This feature aids functional testing of sequential designs by allowing direct setting of output states. The procedure for preloading follows:

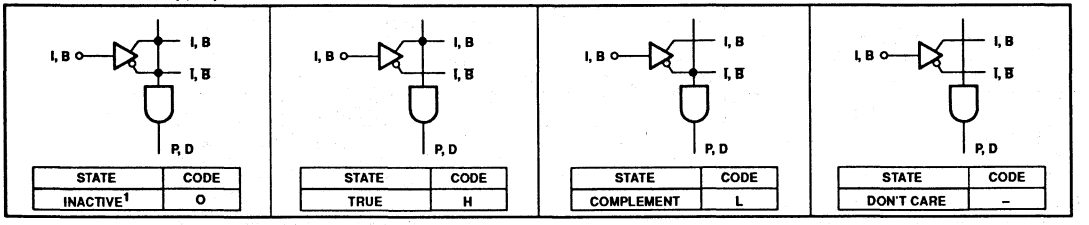
1. Raise V_{CC} to 5.0V ± 0.25V.
2. Set Pin 2 or 3 to V_{HH} to disable outputs and enable preload.
3. Apply the desired value (V_{ILP}/V_{IHP}) to all registered output pins. Leave combinatorial output pins floating.
4. Clock Pin 1 from V_{ILP} to V_{IHP}.
5. Remove V_{ILP}/V_{IHP} from all registered output pins.
6. Lower Pin 2 or 3 to V_{ILP}.
7. Enable the output registers according to the programmed pattern.
8. Verify V_{OL}/V_{OH} at all registered output pins. Note that the output pin signal will depend on the output polarity.

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	REC	MAX	
V_{HH}	Super-level input voltage	9.5	10	10.5	V
V_{ILP}	Low-level input voltage	0	0	0.5	V
V_{IHP}	High-level input voltage	2.4	5.0	5.5	V
t_D	Delay time	100	200	1000	ns
$t_{I/O}$	I/O valid after Pin 2 or 3 drops from V_{HH} to V_{ILP}	100			ns



Output Register Preload Waveform

"AND" ARRAY – (I, B)



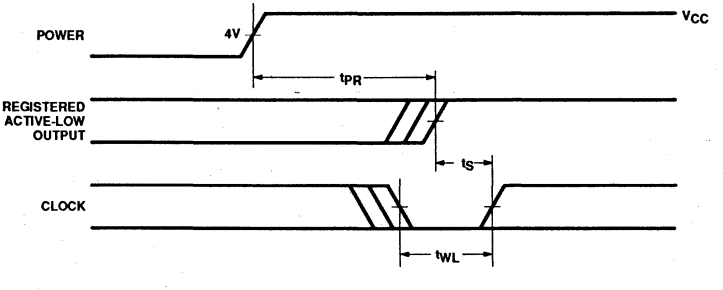
NOTE:
1. This is the initial state.

POWER-UP RESET

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will depend on the programmed pattern. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

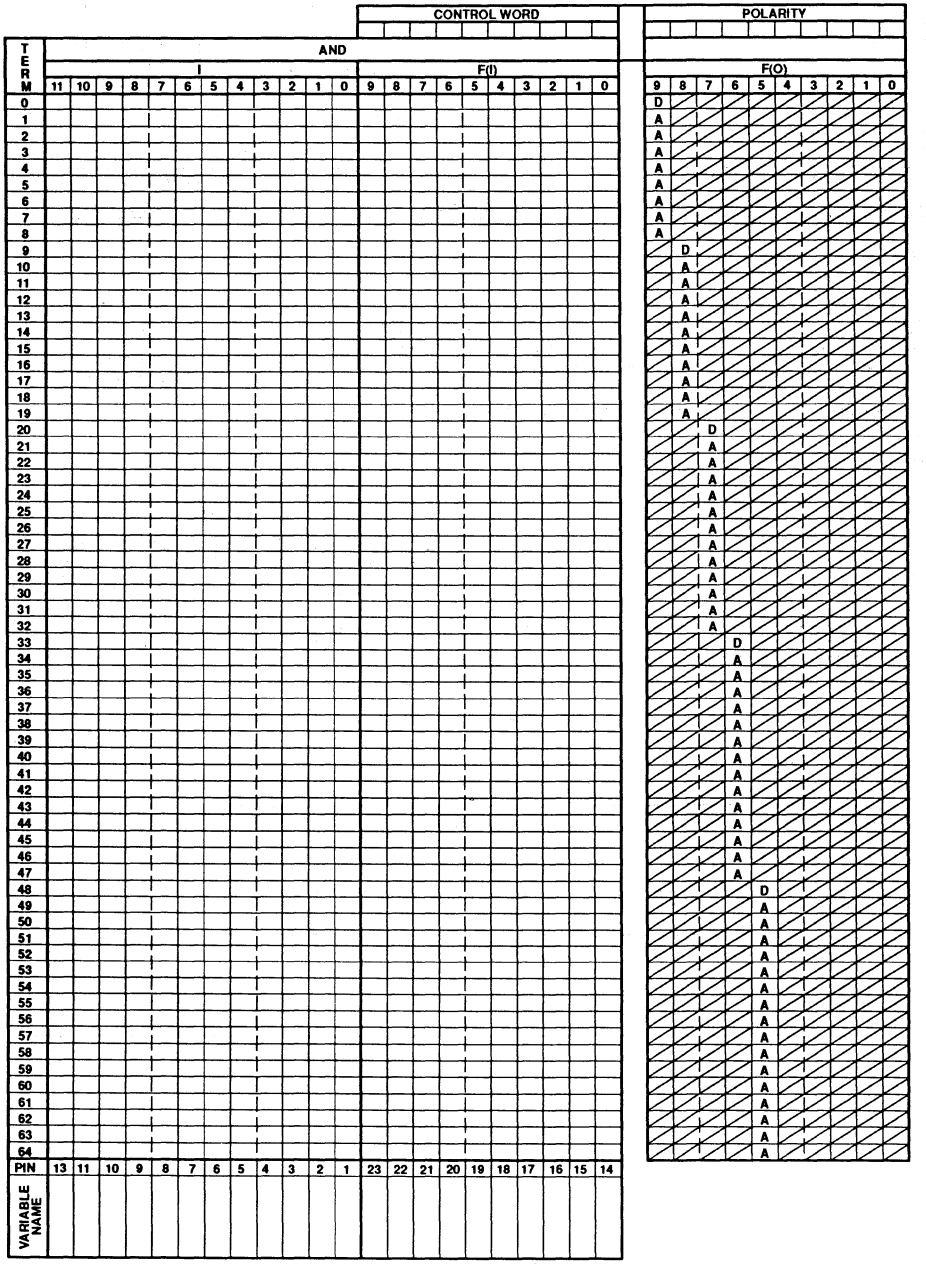
1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
t_{PR}	Power-up Reset Time		1	µs
t_S	Input or Feedback Setup Time	See AC Electrical Characteristics		
t_{WL}	Clock Width LOW			



Power-Up Reset Waveform

PROGRAM TABLE



PROGRAM TABLE (Continued)

TERM	AND I 11	10	9	8	7	6	5	4	3	2	1	0	AND F(I) 9	8	7	6	5	4	3	2	1	0	F(O) 9	8	7	6	5	4	3	2	1	0
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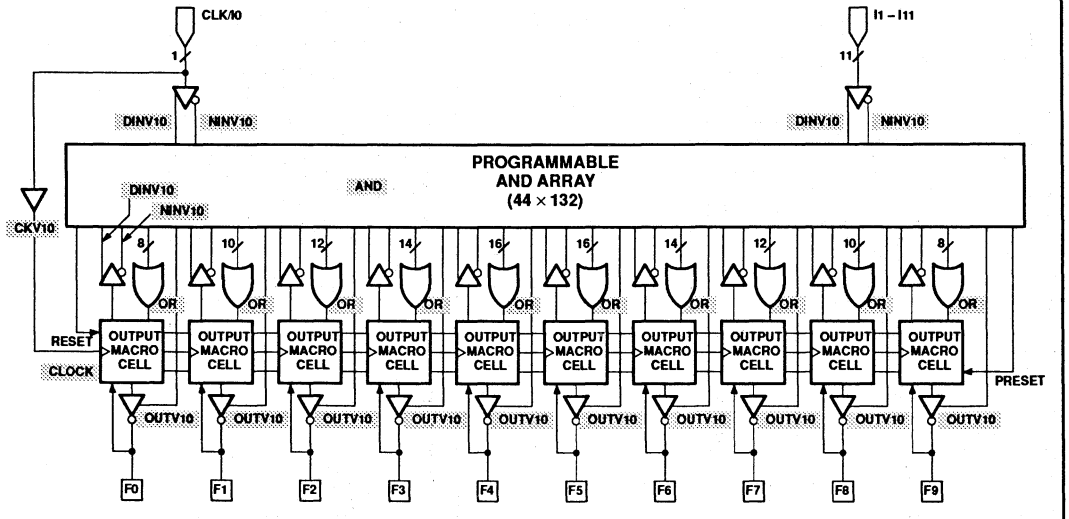
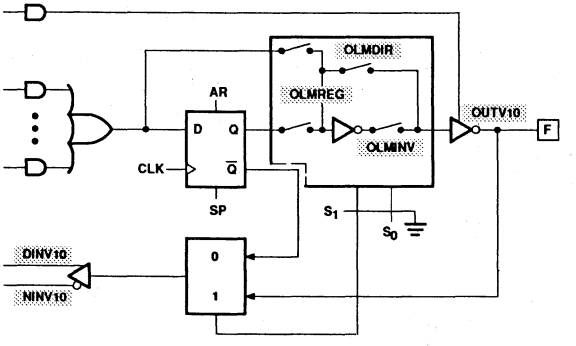
129																																A
AR																																
SP																																
PIN	13	11	10	9	8	7	6	5	4	3	2	1	23	22	21	20	19	18	17	16	15	14										
VARIABLE NAME																																

SNAP RESOURCE SUMMARY DESIGNATIONS





Output Macro Cell

ECL programmable array logic — 10H20EV8/10020EV8

DESCRIPTION

The 10H20EV8/10020EV8 is an ultra high-speed universal ECL PAL® device. Combining versatile output macrocells with a standard AND/OR single programmable array, this device is ideal in implementing a user's custom logic. The use of Signetics state-of-the-art bipolar oxide isolation process enables the 10H20EV8/10020EV8 to achieve optimum speed in any design. The SNAP design software package from Signetics simplifies design entry based upon Boolean or state equations.

The 10H20EV8/10020EV8 is a two-level logic element comprised of 11 fixed inputs, an input pin that can either be used as a clock or 12th input, 90 AND gates, and 8 Output Logic Macrocells. Each Output Macrocell can be individually configured as a dedicated input, dedicated output with polarity control, a bidirectional I/O, or as a registered output that has both output polarity control and feedback to the AND array. This gives the part the capability of having up to 20 inputs and eight outputs.

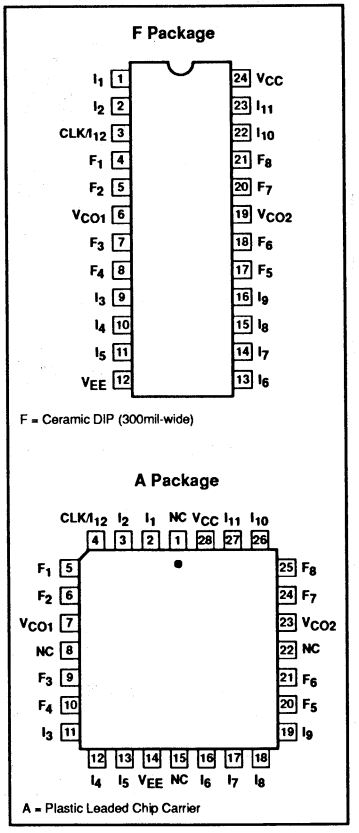
The 10H20EV8/10020EV8 has a variable number of product terms that can be OR'd per output. Four of the outputs have 12 AND terms available and the other four have 8 terms per output. This allows the designer the extra flexibility to implement those functions that he couldn't in a standard PAL device. Asynchronous Preset and Reset product terms are also included for system design ease. Each output has a separate output enable product term. Another feature added for the system designer is a power-up Reset on all registered outputs.

The 10H20EV8/10020EV8 also features the ability to Preload the registers to any desired state during testing. The Preload is not affected by the pattern within the device, so can be performed at any step in the testing sequence. This permits full logical verification even after the device has been patterned.

FEATURES

- Ultra high speed ECL device
  - t_{PD} = 4.5ns (max)
  - t_{IS} = 2.6ns (max)
  - t_{CKO} = 2.3ns (max)
  - f_{MAX} = 208MHz
- Universal ECL Programmable Array Logic
  - 8 user programmable output macrocells
  - Up to 20 inputs and 8 outputs
  - Individual user programmable output polarity
- Variable product term distribution allows increased design capability
- Asynchronous Preset and Reset capability
- 10KH and 100K options
- Power-up Reset and Preload function to enhance state machine design and testing
- Design support provided via SNAP and other CAD tools
- Security fuse for preventing design duplication
- Available in 24-Pin 300mil-wide DIP and 28-Pin PLCC.

PIN CONFIGURATIONS



ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-Pin Ceramic Dual In-Line (300mil-wide)	10H20EV8–4F 10020EV8–4F
28-Pin Plastic Leaded Chip Carrier	10H20EV8–4A 10020EV8–4A

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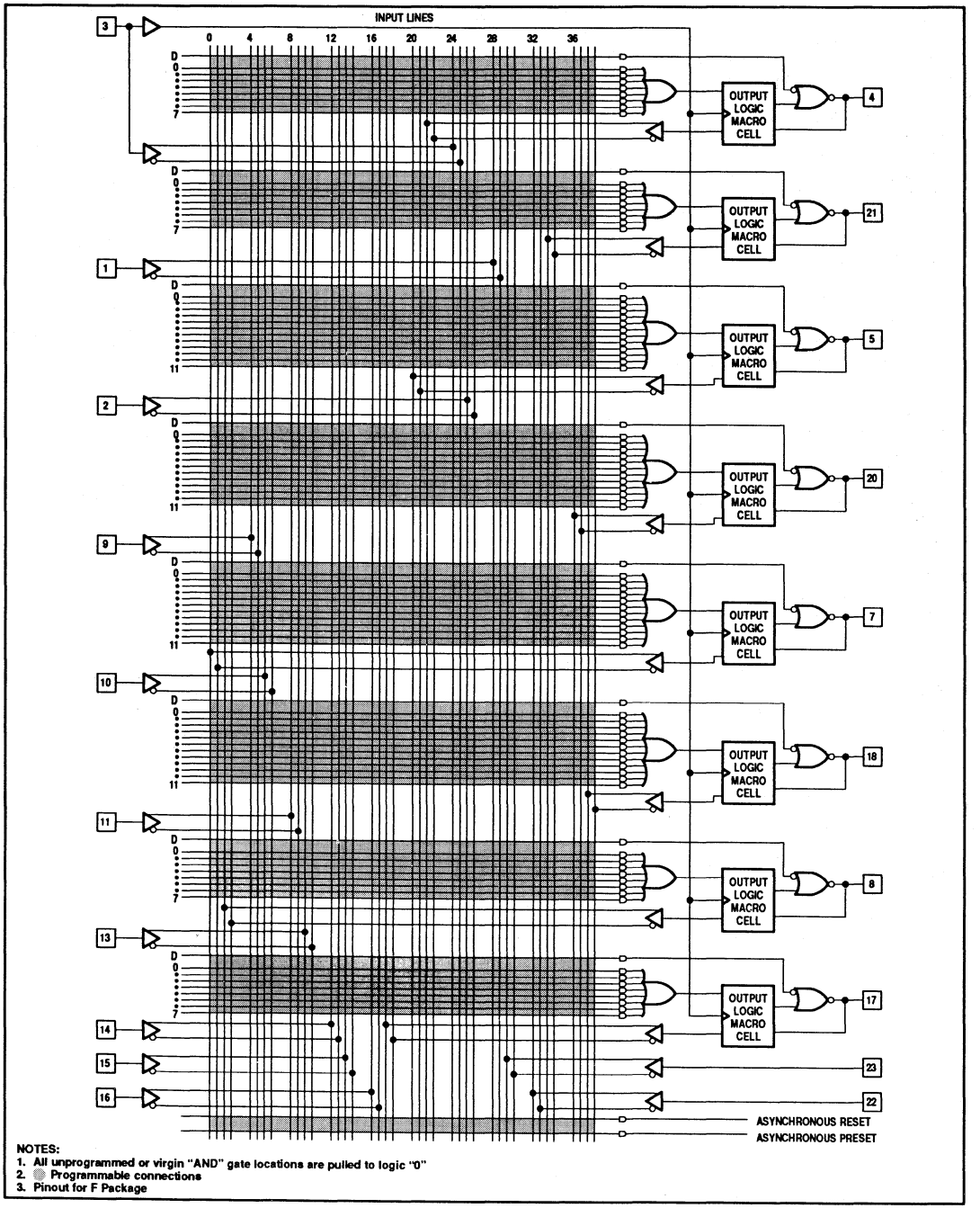
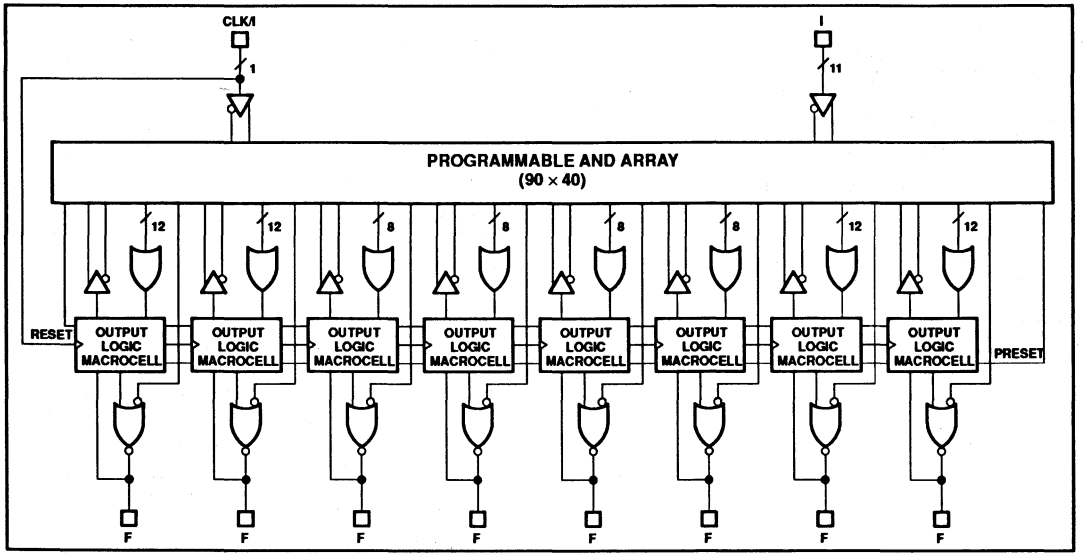
LOGIC DIAGRAM



NOTES:
1. All unprogrammed or virgin "AND" gate locations are pulled to logic "0"
2. ● Programmable connections
3. Pinout for F Package

FUNCTIONAL DIAGRAM



FUNCTIONAL DESCRIPTION

The 10H20EV8/10020EV8 is an ultra high-speed universal ECL PAL-type device. Combining versatile Output Macrocells with a standard AND/OR single programmable array, this device is ideal in implementing a user's custom logic.

As can be seen in the Logic Diagram, the device is a two-level logic element with a programmable AND array. The 20EV8 can have up to 20 inputs and 8 outputs. Each output has a versatile Macrocell whereby the output can either be configured as a dedicated input, a dedicated combinatorial output with polarity control, a bidirectional I/O, or as a registered output that has both output polarity control and feedback into the AND array.

The device also features 90 product terms. Two of the product terms can be used for a global asynchronous preset and/or reset. Eight of the product terms can be used for individual output enable control of each Macrocell. The other 80 product terms are distributed among the outputs. Four of the outputs have eight product terms, while the other four have 12. This arrangement allows the utmost in flexibility when implementing user patterns.

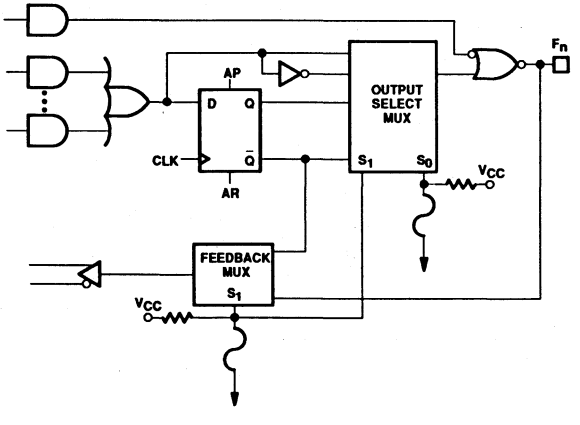


Figure 1. Output Logic Macrocell

Output Logic Macrocell

The 10H20EV8/10020EV8 incorporates an extremely versatile Output Logic Macrocell that allows the user complete flexibility when configuring outputs.

As seen in Figure 1, the 10H20EV8/10020EV8 Output Logic Macrocell consists of an edge-triggered D-type flip-flop, an output select MUX, and a feedback select MUX. Fuses S_0 and S_1 allow the user to select between the various cells. S_1 controls whether the output will be either registered with internal feedback or combinatorial I/O. S_0 controls the polarity of the output (Active-HIGH or Active-LOW). This allows the user to achieve the following configurations: Registered Active-HIGH output, Registered Active-LOW output, Combinatorial Active-HIGH output, and Combinatorial Active-LOW output. With the output enable product term, this list can be extended by adding the configurations of a Combinatorial I/O with Polarity or another input.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER		RATING	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current		–50	mA
T_S	Operating Temperature range		–55 to +150	°C
T_J	Storage Temperature range	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

DC OPERATING CONDITIONS 10H20EV8

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS NOM	LIMITS MAX	UNIT
V_{CC}, V_{CO1}, V_{CO2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_{amb} = 0°C	–1170		–840	mV
		T_{amb} = +25°C	–1130		–810	mV
		T_{amb} = +75°C	–1070		–735	mV
V_{IL}	Low level input voltage	T_{amb} = 0°C	–1950		–1480	mV
		T_{amb} = +25°C	–1950		–1480	mV
		T_{amb} = +75°C	–1980		–1450	mV
T_{amb}	Operating ambient temperature range		0	+25	+75	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC OPERATING CONDITIONS 10020EV8

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS NOM	LIMITS MAX	UNIT
V_{CC}, V_{CO1}, V_{CO2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage		–4.8	–4.5	–4.2	V
V_{EE}	Supply voltage when opetating with the 10K or 10KH ECL family		–5.7			V
V_{IH}	High level input voltage	V_{EE} = –4.2V	–1150		–880	mV
		V_{EE} = –4.5V	–1165			
		V_{EE} = –4.8V	–1165			
V_{IL}	Low level input voltage	V_{EE} = –4.2V	–1810		–1475	mV
		V_{EE} = –4.5V			–1475	mV
		V_{EE} = –4.8V			–1490	mV
T_{amb}	Operating ambient temperature range		0	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltages (–4.2V, –4.5V, –4.8V), the DC and AC Electrical Characteristics will vary slightly from their specified values.

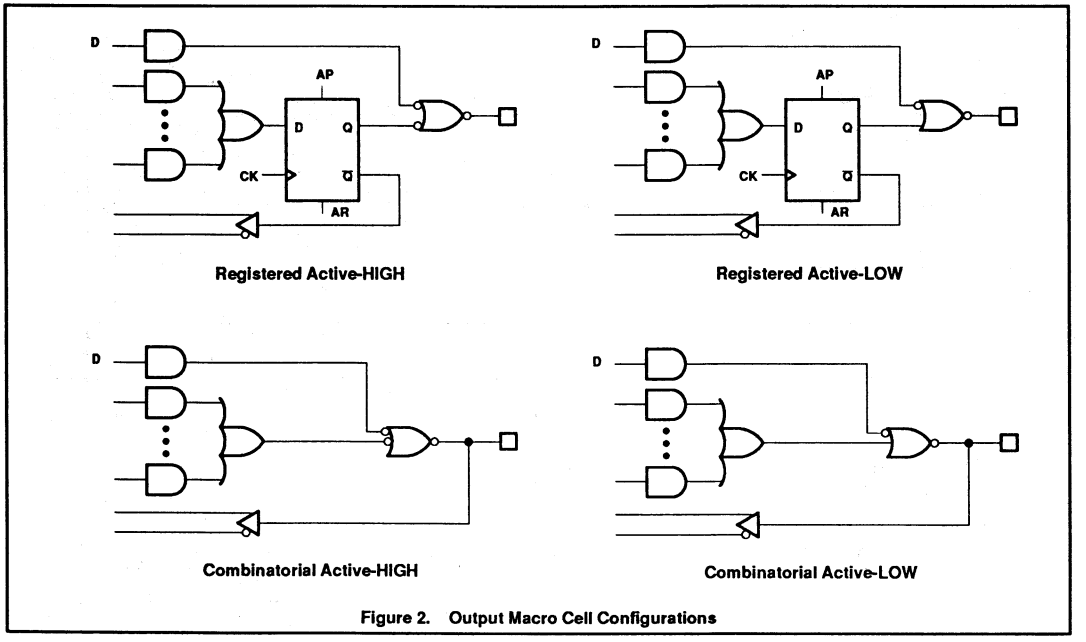


Figure 2. Output Macro Cell Configurations

OUTPUT MACRO CELL CONFIGURATION

Shown in Figure 2 are the four possible configurations of the output macrocell using fuses S_0 and S_1. As seen, the output can either be registered Active-HIGH/LOW with feedback or combinatorial Active-HIGH/LOW with feedback. If the registered mode is chosen, the feedback from the $\overline{Q}$ output to the AND array enables one to make state machines or shift registers without having to tie the output to one of the inputs. If a combinatorial output is chosen, the feedback gate is enabled from the pin and allows one to create permanent outputs, permanent inputs, or I/O pins through the use of the output enable (D) product term.

OUTPUT ENABLE

Each output on the 10H20EV8/10020EV8 has its own individual product term for output enable. The use of the D product term (direction control) allows the user three possible configurations of the outputs. They are: always enabled, always disabled, and controlled by a programmed pattern. A HIGH on the D term enables the output, while a LOW performs the disable function. Output enable control can be achieved by programming a pattern on the D term.

The output enable control can also be used to expand a designer's possibilities once a combinatorial output has been chosen. If the D term is always HIGH, the pin becomes a permanent Active-HIGH/LOW output. If the D term is always LOW (all fuses left intact), the pin now becomes an extra input.

PRESET AND RESET

The 10H20EV8/10020EV8 also includes a separate product term for asynchronous Preset and asynchronous Reset. These lines are common for all registers and are asserted when the specific product term goes HIGH. Being asynchronous, they are independent of the clock. It should be noted that the actual state of the output is dependent on how the polarity of the particular output has been chosen. If the outputs are a mix of Active-HIGH and Active-LOW, a Preset signal will force the Active-HIGH outputs HIGH while the Active-LOW outputs would go LOW, even though the Q output of all flip-flops would go HIGH. A Reset signal would force the opposite conditions.

PRELOAD

To simplify testing, the 10H20EV8/10020EV8 has also included PRELOAD circuitry. This allows a user to load any particular data desired into the registers regardless of the programmed pattern. This means that the PRELOAD can be done on a blank part and after that same part has been programmed to facilitate any post-fuse testing desired.

It can also be used by a designer to help debug a circuit. This could be important if a state machine was implemented in the 10H20EV8/ 10020EV8. The PRELOAD would allow the entry of any state in the sequence desired and start clocking from that particular point. Any or all transitions could be verified.

DC ELECTRICAL CHARACTERISTICS 10H20EV8

$0°C \leq T_{amb} \leq +75°C$, $V_{EE} = -5.2V \pm 5\%$, $V_{CC} = V_{CO1} = V_{CO2} = GND$

SYMBOL	PARAMETER[1]	TEST CONDITIONS[2]	T_{amb}	LIMITS[4] MIN	LIMITS[4] MAX	UNITS
V_{OH}	High level output voltage	$V_{IN} = V_{IH}$ MIN or V_{IL} MAX	0°C +25°C +75°C	–1020 –980 –920	–840 –810 –735	mV
V_{OL}	Low level output voltage	$V_{IN} = V_{IH}$ MIN or V_{IL} MAX	0°C +25°C +75°C	–1950 –1950 –1950	–1630 –1630 –1600	mV
I_{IH}	High level input current	$V_{IN} = V_{IH}$ MAX	0°C +75°C		220	µA
I_{IL}	Low level input current	$V_{IN} = V_{IL}$ MIN Except I/O Pins	0°C +75°C	0.3		µA
$-I_{EE}$	Supply current	V_{EE} = MAX All inputs = V_{IH} MAX	0°C to +75°C		250	mA

DC ELECTRICAL CHARACTERISTICS 10020EV8

$0°C \leq T_{amb} \leq +85°C$, $-4.8V \leq V_{EE} \leq -4.2V$, $V_{CC} = V_{CO1} = V_{CO2} = GND$

SYMBOL	PARAMETER[1]	TEST CONDITIONS[2]			LIMITS[4] MIN	LIMITS[4] TYP	LIMITS[4] MAX	UNITS
V_{OH}	High level output voltage	Outputs Loaded with 50Ω to –2.0V ± 0.010V	$V_{IN} = V_{IH}$ MAX or V_{IL} MIN	$V_{EE} = -4.2V$	–1020		–870	mV
				$V_{EE} = -4.5V$	–1025	–955	–880	mV
				$V_{EE} = -4.8V$	–1035		–880	mV
V_{OHT}	High level output threshold voltage		Apply V_{IHMIN} or V_{ILMAX} to one input at a time, other inuts at V_{IHMAX} or V_{ILMIN}.	$V_{EE} = -4.2V$	–1030			mV
				$V_{EE} = -4.5V$	–1035			mV
				$V_{EE} = -4.8V$	–1045			mV
V_{OLT}	Low level output threshold voltage		Apply V_{IHMIN} or V_{ILMAX} to one input at a time, other inuts at V_{IHMAX} or V_{ILMIN}.	$V_{EE} = -4.2V$			–1595	mV
				$V_{EE} = -4.5V$			–1610	mV
				$V_{EE} = -4.8V$			–1610	mV
V_{OL}	Low level output voltage		Inuts at V_{IHMAX} or V_{ILMIN}.	$V_{EE} = -4.2V$	–1810		–1605	mV
				$V_{EE} = -4.5V$	–1810	–1705	–1620	mV
				$V_{EE} = -4.8V$	–1830		–1620	mV
I_{IH}	High level input current	One input under test at V_{IHMAX}. Other inputs at V_{ILMIN}.					220	µA
I_{IL}	Low level input current	One input under test at V_{ILMIN}. Other inputs at V_{IHMAX}.			0.5			µA
$-I_{EE}$	V_{EE} supply current	All inputs at V_{IHMAX}.					230	mA

NOTES:

1. All voltage measurements are referenced to the ground terminal.
2. Each ECL 10KH/100K series device has been designed to meet the DC specification after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min.) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3, of the *Signetics 10/100K ECL Data Handbook*.
3. Terminals not specifically referenced can be left electrically open. Open inputs assume a logic LOW state. Any unused pins can be terminated to –2V. If tied to V_{EE}, it must be through a resistor > 10K. It is recommended that pins that have been programmed as RESET, PRESET, or CLOCK inputs not be left open due to the possibility of false triggering from internally and externally generated switching transients.
4. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.

AC ELECTRICAL CHARACTERISTICS (for Ceramic Dual In-Line Package)

10H20EV8: $0°C \leq T_{amb} \leq +75°C$, $V_{EE} = -5.2V \pm 5\%$, $V_{CC} = V_{CO1} = V_{CO2} = GND$
10020EV8: $0°C \leq T_{amb} \leq +85°C$, $-4.8V \leq V_{EE} \leq -4.2V$, $V_{CC} = V_{CO1} = V_{CO2} = GND$

SYMBOL	PARAMETER	FROM	TO	LIMITS[1]									UNIT
				0°C			+25°C			+75°C/+85°C			
				MIN[2]	TYP[3]	MAX[2]	MIN[2]	TYP[3]	MAX[2]	MIN[2]	TYP[3]	MAX[2]	
Pulse Width													
t_{CKH}	Clock High	CLK +	CLK –	2.0	0.6		2.0	0.6		2.0	0.6		ns
t_{CKL}	Clock Low	CLK –	CLK +	2.0	0.9		2.0	0.9		2.0	0.9		ns
t_{CKP}	Clock Period	CLK +	CLK +	4.0			4.0			4.0			ns
t_{PRH}	Preset/Reset Pulse	(I, I/O) ±	(I, I/O) ±	4.5	—		4.5	—		4.5	—		ns
Setup and Hold Time													
t_{IS}	Input	(I, I/O) ±	CLK +	2.6	1.0		2.6	1.1		2.7	1.4		ns
t_{IH}	Input	CLK +	(I, I/O) ±	0.1	< 0		0.1	< 0		0.1	< 0		ns
t_{PRS}	Clock Resume after Preset/Reset	(I, I/O) ±	CLK +	4.6	1.0		4.6	0.9		4.6	0.8		ns
Propagation Delay													
t_{PD}	Input	(I, I/O) ±	I/O ±		2.85	4.7		2.95	4.7		3.35	4.7	ns
t_{CKO}	Clock	CLK +	I/O ±		1.65	2.4		1.7	2.4		2.0	2.5	ns
t_{OE}	Output Enable	(I, I/O) ±	I/O		2.0	4.2		2.1	4.2		2.2	4.2	ns
t_{OD}	Output Disable	(I, I/O) ±	I/O		2.0	4.2		2.1	4.2		2.2	4.2	ns
t_{PRO}	Preset/Reset	(I, I/O) ±	I/O ±		2.8	4.7		3.0	4.7		3.5	4.7	ns
t_{PPR}	Power-on Reset	V_{EE}	I/O		—	10		—	10		—	10	ns
f_{MAX}				208	300		208	300		208	300		MHz

NOTES:
1. Refer to AC Test Circuit and Voltage Wafeforms diagrams.
2. Maximum loading conditions: 89 fuses intact per row.
3. Typical loading conditions: 15 fuses intact per row. (All "inactive" fuses, except those necessary for correct functionality, are removed.)

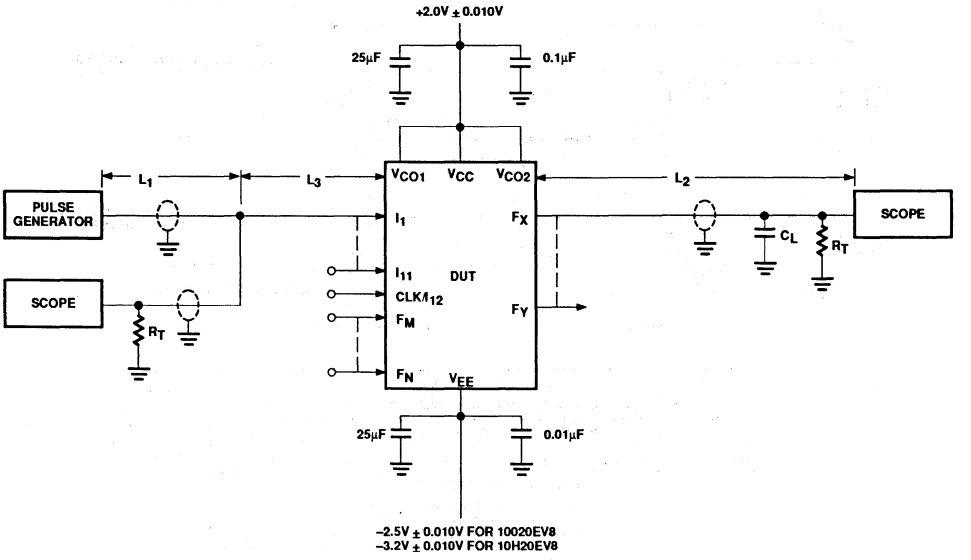
AC ELECTRICAL CHARACTERISTICS (for Plastic Leaded Chip Carrier)

10H20EV8: $0°C \le T_{amb} \le +75°C$, $V_{EE} = -5.2V \pm 5\%$, $V_{CC} = V_{CO1} = V_{CO2} = GND$
10020EV8: $0°C \le T_{amb} \le +85°C$, $-4.8V \le V_{EE} \le -4.2V$, $V_{CC} = V_{CO1} = V_{CO2} = GND$

SYMBOL	PARAMETER	FROM	TO	LIMITS[1]									UNIT
				0°C			+25°C			+75°C/+85°C			
				MIN	TYP[3]	MAX[2]	MIN	TYP[3]	MAX[2]	MIN	TYP[3]	MAX[2]	
Pulse Width													
t_{CKH}	Clock High	CLK +	CLK –	2.0	0.6		2.0	0.6		2.0	0.6		ns
t_{CKL}	Clock Low	CLK –	CLK +	2.0	0.9		2.0	0.9		2.0	0.9		ns
t_{CKP}	Clock Period	CLK +	CLK +	4.0			4.0			4.0			ns
t_{PRH}	Preset/Reset Pulse	(I, I/O) ±	(I, I/O) ±	4.5	—		4.5	—		4.5	—		ns
Setup and Hold Time													
t_{IS}	Input	(I, I/O) ±	CLK +	2.5	1.0		2.5	1.1		2.6	1.4		ns
t_{IH}	Input	CLK +	(I, I/O) ±	0	< 0		0	< 0		0	< 0		ns
t_{PRS}	Clock Resume after Preset/Reset	(I, I/O) ±	CLK +	4.5	1.0		4.5	0.9		4.5	0.8		ns
Propagation Delay													
t_{PD}	Input	(I, I/O) ±	I/O ±		2.85	4.5		2.95	4.5		3.35	4.5	ns
t_{CKO}	Clock	CLK +	I/O ±		1.65	2.2		1.7	2.2		2.0	2.3	ns
t_{OE}	Output Enable	(I, I/O) ±	I/O		2.0	4.0		2.1	4.0		2.2	4.0	ns
t_{OD}	Output Disable	(I, I/O) ±	I/O		2.0	4.0		2.1	4.0		2.2	4.0	ns
t_{PRO}	Preset/Reset	(I, I/O) ±	I/O ±		2.8	4.5		3.0	4.5		3.5	4.5	ns
t_{PPR}	Power-on Reset	V_{EE}	I/O		—	10		—	10		—	10	ns
f_{MAX}				208	300		208	300		208	300		MHz

NOTES:
1. Refer to AC Test Circuit and Voltage Wafeforms diagrams.
2. Maximum loading conditions: 89 fuses intact per row.
3. Typical loading conditions: 15 fuses intact per row. (All "inactive" fuses, except those necessary for correct functionality, are removed.)

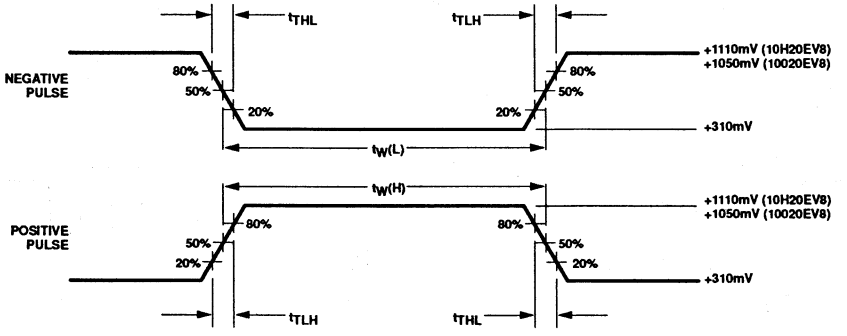
AC TEST CIRCUIT



NOTES:

1. Use decoupling capacitors of 0.1µF and 25µF from GND to V_{CC}, and 0.01µF and 25µF from GND to V_{EE} (0.01 and 0.1µF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than $^1/_4$ inch (6mm).
2. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
3. All unused outputs are loaded with 50Ω to GND.
4. L_1 and L_2 are equal length 50Ω impedance lines. L_3, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed $^1/_4$ inch (6mm).
5. R_T = 50Ω terminator internal to Scope.
6. The unmatched wire stub between coaxial cable and pins under test must be less than $^1/_4$ inch (6mm) long for proper test.
7. C_L = Fixture and stray capacitance ≤ 3pF.
8. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed $^1/_4$ inch (6mm) in length (refer to section on AC setup procedure).
9. All 50Ω resistors should have tolerance of ± 1% or better.
10. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.

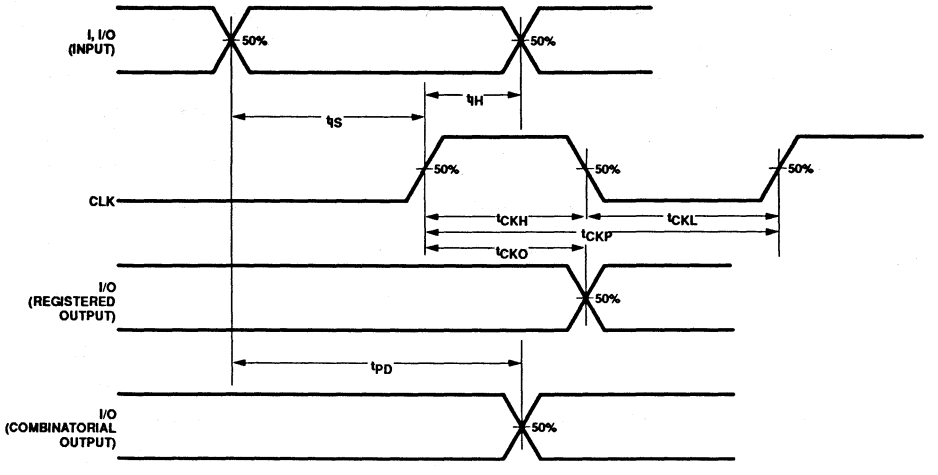
VOLTAGE WAVEFORMS



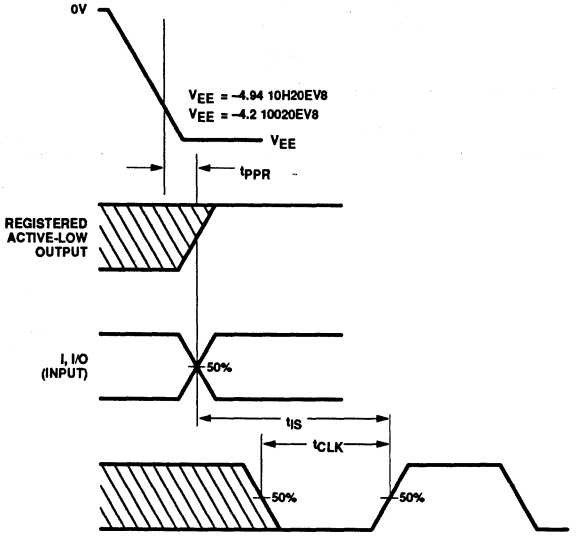
INPUT PULSE REQUIREMENTS $V_{CC} = V_{CO1} = V_{CO2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, V_T = GND (0V)					
FAMILY	AMPLITUDE	REP RATE	PULSE WIDTH	t_{TLH}	t_{THL}
10KH ECL	$800mV_{P-P}$	1MHz	500ns	$1.3 \pm 0.2ns$	$1.3 \pm 0.2ns$
INPUT PULSE REQUIREMENTS $V_{CC} = V_{CO1} = V_{CO2} = +2.0V \pm 0.010V$, $V_{EE} = -2.5V \pm 0.010V$, V_T = GND (0V)					
FAMILY	AMPLITUDE	REP RATE	PULSE WIDTH	t_{TLH}	t_{THL}
100K ECL	$740mV_{P-P}$	1MHz	500ns	$0.7 \pm 0.1ns$	$0.7 \pm 0.1ns$

Input Pulse Definition

TIMING DIAGRAMS

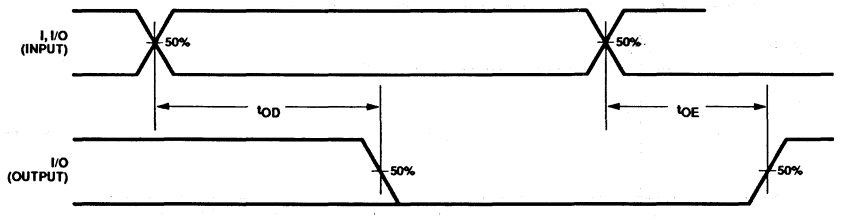


Flip-Flop and Gate Outputs

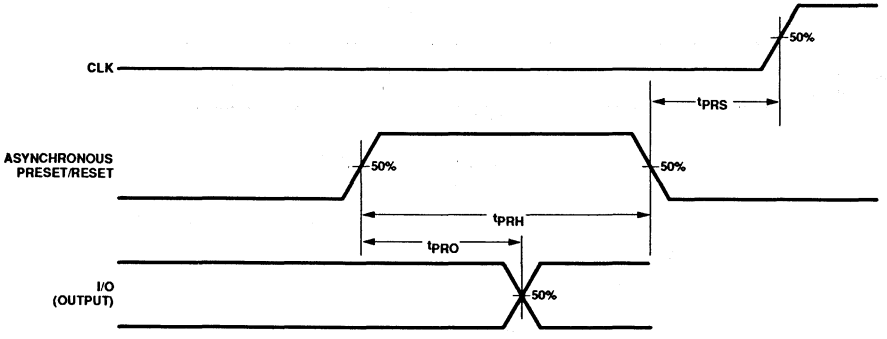


Power-On Reset

TIMING DIAGRAMS (Continued)



Output Enable/Disable

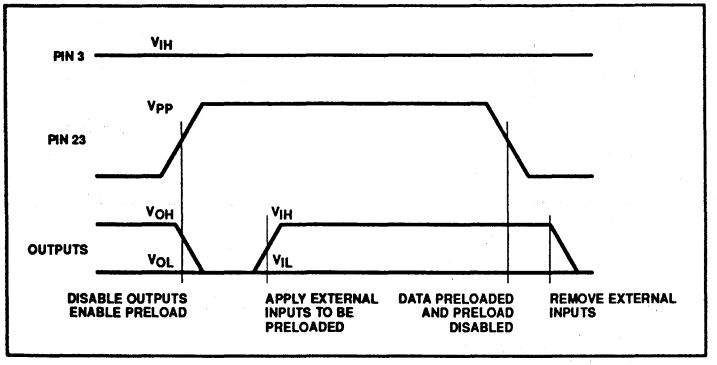


Asynchronous Preset/Reset

REGISTER PRELOAD

The 10H20EV8/10020EV8 has included circuitry that allows a user to load data into the output registers. Register PRELOAD can be done at any time and is not dependent on any particular pattern programmed into the device. This simplifies the ability to fully verify logic states and sequences even after the device has been patterned.

The pin levels and sequence necessary to perform the register PRELOAD are shown below.



SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	TYP	MAX	
V_{IH}	Input HIGH level during PRELOAD and Verify	–1.1	–0.9	–0.7	V
V_{IL}	Input LOW level during PRELOAD and Verify	–1.85	–1.65	–1.45	V
V_{PP}	PRELOAD enable voltage applied to I_{11}	1.45	1.6	1.75	V

NOTE:

1. Unused inputs should be handled as follows:
   - Set at V_{IH} or V_{IL}
   - Terminated to –2V
   - Tied to V_{EE} through a resistor > 10K
   - Open

LOGIC PROGRAMMING

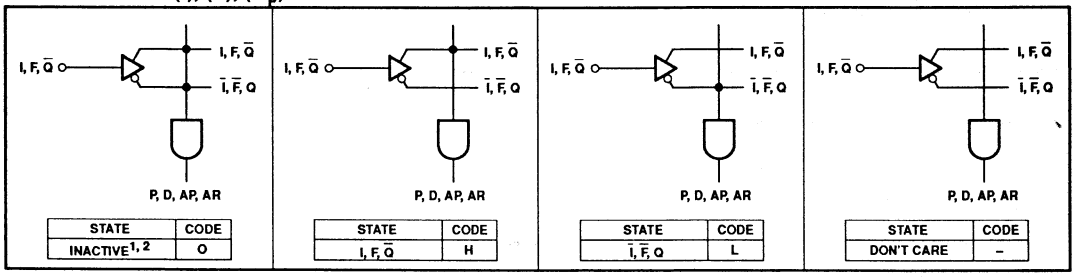
The 10H20EV8/10020EV8 is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Signetics SLICE and SNAP design software packages. ABEL™ and CUPL™ design software packages also support the 10H20EV8/10020EV8.

All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

10H20EV8/10020EV8 logic designs can also be generated using the program table entry format detailed on the following page. This program table entry format is supported by SLICE only. SLICE is available, free of charge, to qualified users.

To implement the desired logic functions, the state of each logic variable from logic equations (I, F, Q, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

"AND" ARRAY – (I), (F), ($\overline{Q}_p$)



NOTES:
1. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates.
2. Any gate (P, D, AP, AR) will be unconditionally inhibited if any one of the I, F or Q link pairs is left intact.

OUTPUT MACROCELL CONFIGURATIONS

OUTPUT MACROCELL CONFIGURATION	CONTROL WORD FUSE	POLARITY FUSE
Registered Output, Active-HIGH	D	H
Registered Output, Active-LOW	D[1]	L[1]
Combinatorial I/O, Active-HIGH	B	H
Combinatorial I/O, Acitve-LOW	B	L

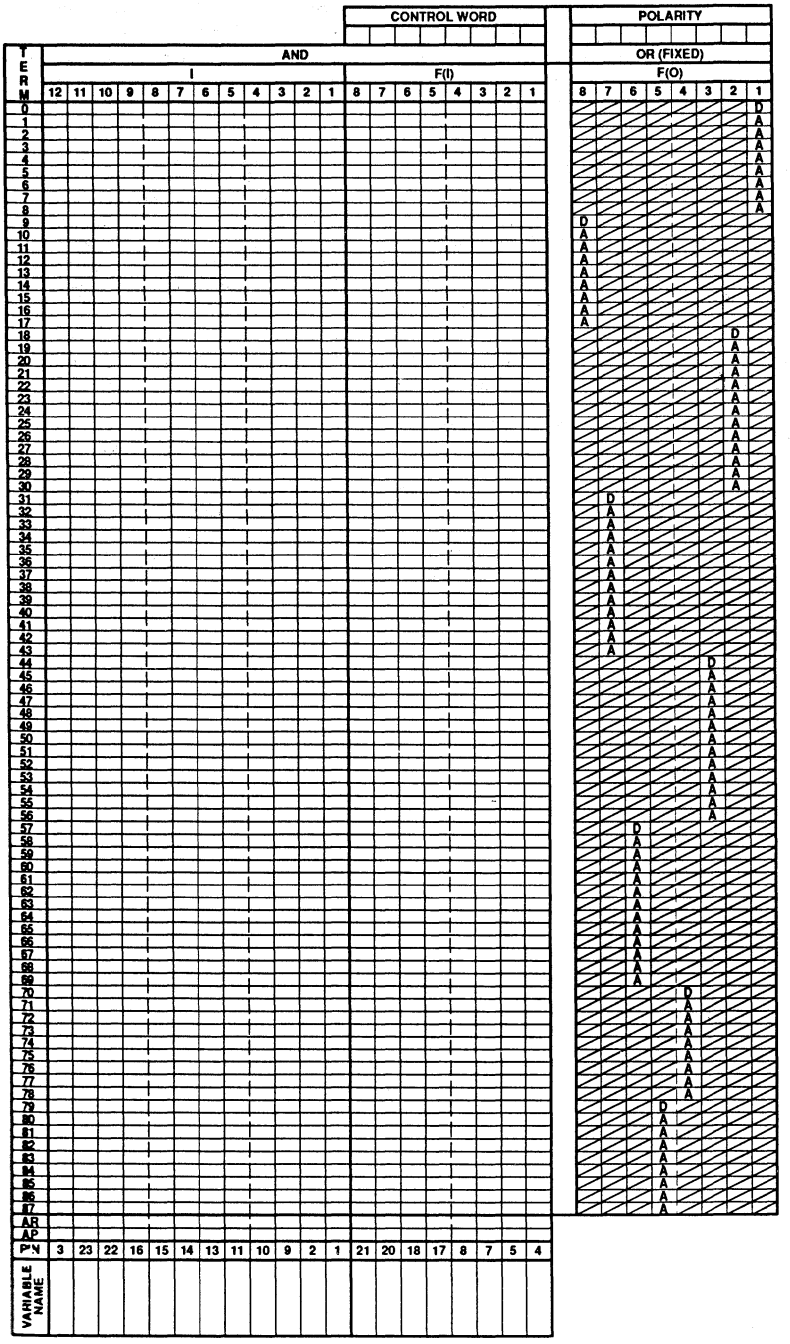
NOTE:
1. This is the initial (unprogrammed) state of the device.

PROGRAMMING AND SOFTWARE SUPPORT

Refer to Section 8 *(Development Software)* and Section 9 *(Third-party Programmer/ Software Support)* of this data handbook for additional information.

ABEL is a trademark of Data I/O Corp.
CUPL is a trademark of Logical Devices, Inc.

PROGRAM TABLE



SNAP

Features

- Schematic entry using DASH™ 4.0 or above or OrCAD™ SDT III
- State Equation Entry
- Boolean Equation Entry
- Allows design entry in any combination of above formats
- Simulator
  - Logic and fault simulation
  - Timing model generation for device timing simulation
  - Synthetic logic analyzer format
- Macro library for standard TTL and user defined functions
- Device independent netlist generation
- JEDEC fuse map generated from netlist

SNAP (Synthesis, Netlist, Analysis and Program) is a versatile development tool that speeds the design and testing of PML. SNAP combines a user-friendly environment and powerful modules that make designing with PML simple. The SNAP environment gives the user the freedom to design independent of the device architecture.

The flexibility in the variations of design entry methodologies allows design entry in the most appropriate terms. SNAP merges the inputs, regardless of the type, into a high-level netlist for simulation or compilation into a JEDEC fuse map. The JEDEC fuse map can then be transferred from the host computer to the device programer.

SNAP's simulator uses a synthetic logic analyzer format to display and set the nodes of the design. The SNAP simulator provides complete timing information, setup and hold-time checking, plus toggle and fault grading analysis.

SNAP operates on an IBM® PC/XT, PC/AT, PS/2, or any compatible system with DOS 2.1 or higher. A minimum of 640K bytes of RAM is required together with a hard disk.

SLICE

SLICE, which supports Signetics PLD line, is easy to understand and simple to use. Select a PLD, assign input and output pins and enter the desired equations in either Boolean or state form. SLICE then checks the equations for errors. It automatically generates a JEDEC-format fuse map for downloading to a PLD programmer.

Fully menu driven, SLICE incorporates a fuse table editor for making quick modifications to the design and a test vector editor for input of test vectors.

A built-in Boolean equation extractor allows existing PLDs to be used as the basis for a new design. the extractor reads JEDEC information from a PLD and creates a file containing the corresponding Boolean equations. The result can then be used to consolidate several PLD designs into a single, denser part.

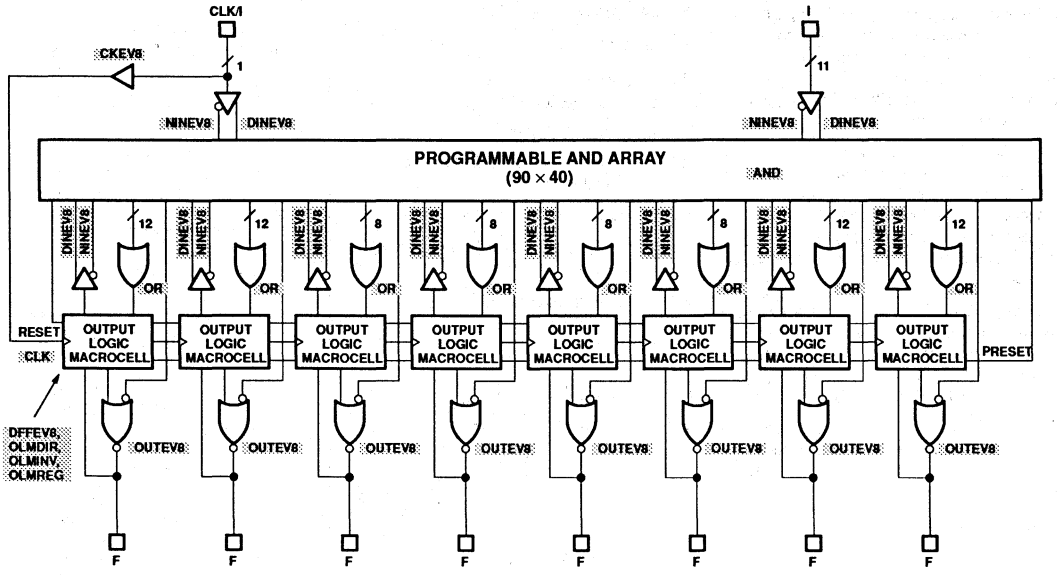
And SLICE is upward compatible with Signetics extensive design suite, SNAP.

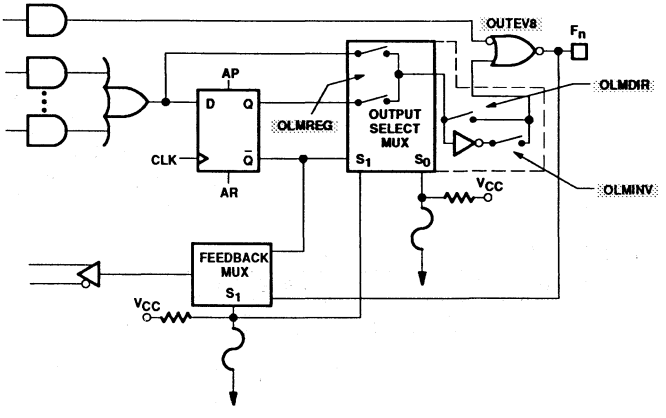
DESIGN SECURITY

The 10H20EV8/10020EV8 has a programmable security fuse that controls the access to the data programmed in the device. By using this programmable feature, proprietary designs implemented in the device cannot be copied or retrieved.

DASH is a trademark of Data I/O Corporation.
OrCAD is a trademark of OrCAD, Inc.
IBM is a registered trademark of International Business Machines Corporation.

SNAP RESOURCE SUMMARY DESIGNATIONS





Output Logic Macrocell

Programmable high-speed decoder logic (48 × 73 × 22)

PHD48N22–7

DESCRIPTION

The PHD48N22–7 is an ultra fast Programmable High-speed Decoder featuring a 7.5ns maximum propagation delay. The architecture has been optimized using Signetics state-of-the-art bipolar oxide isolation process coupled with titanium-tungsten fuses to achieve superior speed in any design.

The PHD48N22–7 is a two level logic element comprised of 36 fixed inputs, 73 AND gates, 10 outputs, and 12 bidirectional I/Os. This gives the device the ability to have as many as 48 inputs. Individual 3-State control of all outputs is also provided.

The device is field-programmable, enabling the user to quickly generate custom patterns using standard programming equipment. Proprietary designs can be protected by programming the security fuse.

The SLICE and SNAP software packages from Philips Components–Signetics support easy design entry for the PHD48N22–7 as well as other PLD devices.

Order codes are listed below.

FEATURES

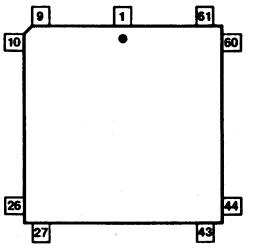
- Ideal for high speed system decoding
- Super high speed at 7.5ns t_{PD}
- 36 dedicated inputs
- 22 outputs
  - 12 bidirectional I/O
  - 10 dedicated outputs
- Security fuse to prevent duplication of proprietary designs.
- Individual 3-State control of all outputs
- Field-programmable on industry standard programmers
- Available in 68-Pin Plastic Leaded Chip Carrier (PLCC)

APPLICATIONS

- High speed memory decoders
- High speed code detectors
- Random logic
- Peripheral selectors
- Machine state decoders

PIN CONFIGURATION

A Package



A = Plastic Leaded Chip Carrier

Pin	Function	Pin	Function
1	I0	35	I29
2	I1	36	I30
3	I2	37	I31
4	V_{CC3}	38	V_{CC4}
5	I3	39	I32
6	I4	40	I33
7	I5	41	I34
8	I6	42	I35
9	I7	43	B0
10	I8	44	B1
11	I9	45	B2
12	I10	46	B3
13	I11	47	B4
14	GND5	48	GND6
15	GND1	49	GND2
16	I12	50	B5
17	I13	51	B6
18	I14	52	B7
19	I15	53	O0
20	I16	54	O1
21	V_{CC2}	55	V_{CC1}
22	I17	56	O2
23	I18	57	O3
24	I19	58	O4
25	I20	59	O5
26	I21	60	O6
27	I22	61	O7
28	I23	62	O8
29	I24	63	O9
30	I25	64	OR0
31	I26	65	OR1
32	GND3	66	GND4
33	I27	67	OR2
34	I28	68	OR3

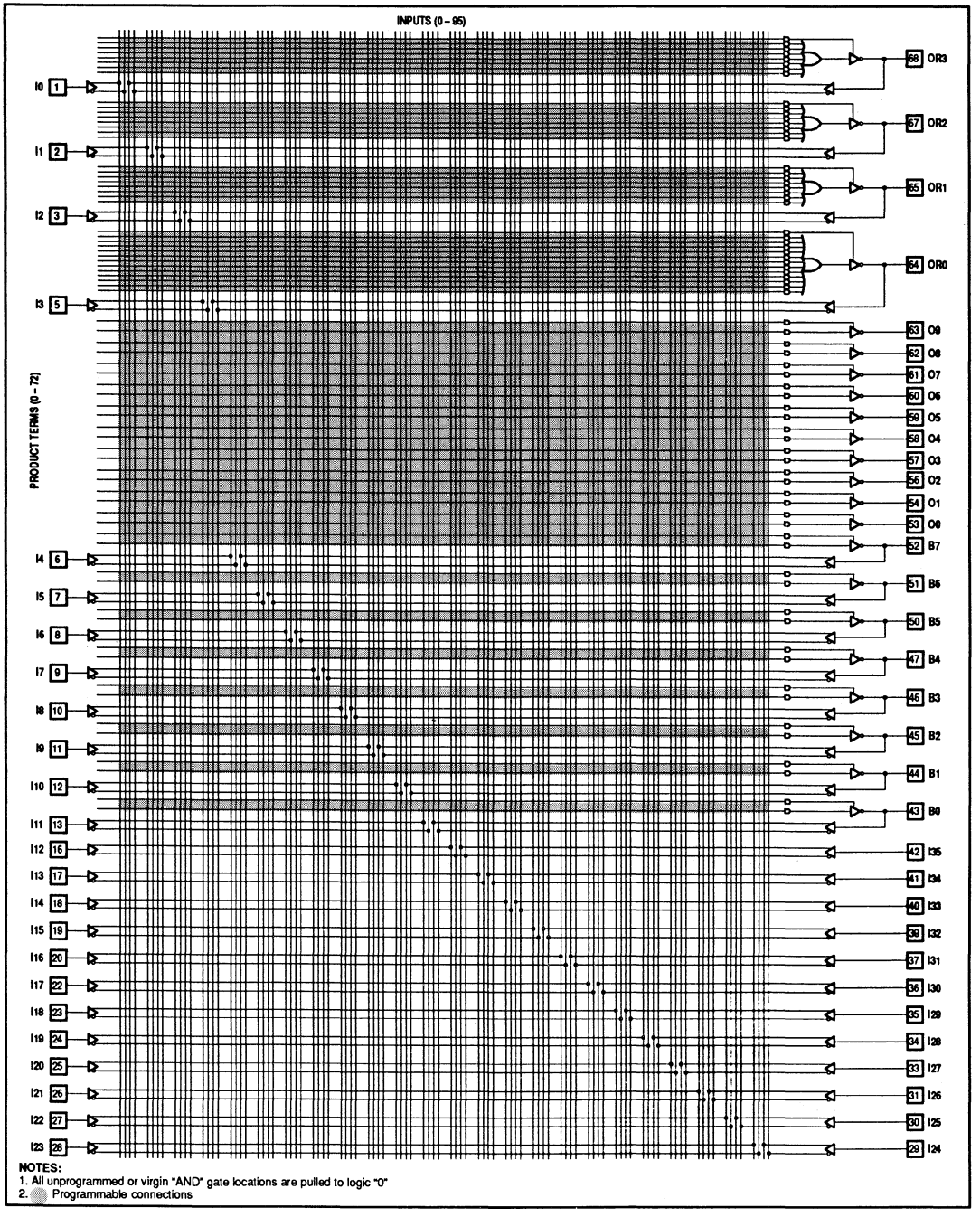
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
68-Pin Plastic Leaded Chip Carrier	PHD48N22–7A

Programmable high-speed decoder logic (48 × 73 × 22)

PHD48N22–7

LOGIC DIAGRAM

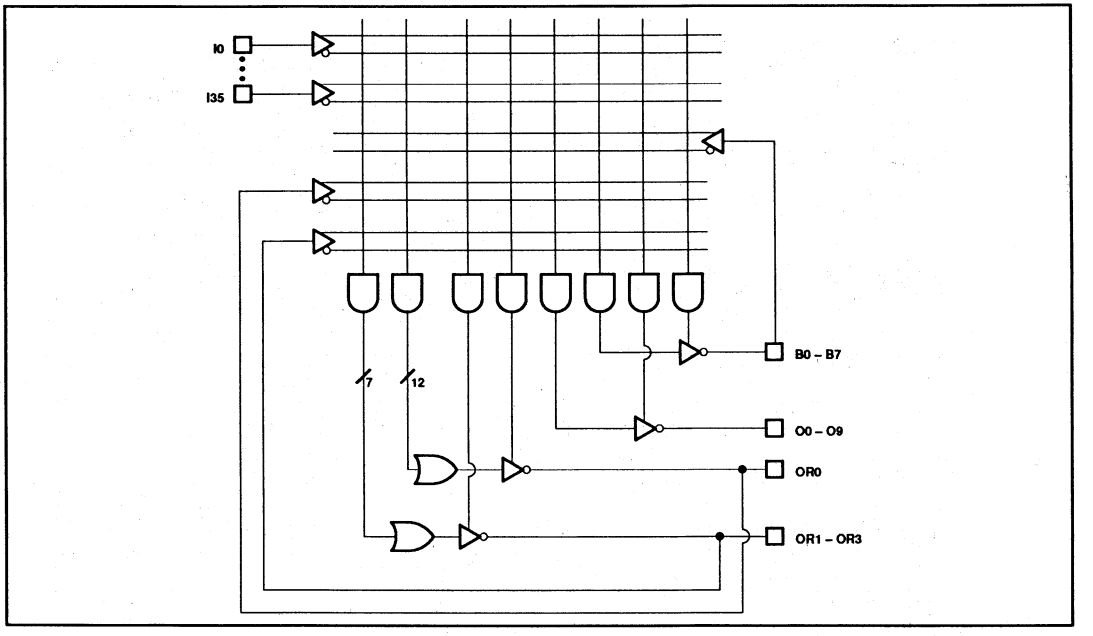


NOTES:
1. All unprogrammed or virgin "AND" gate locations are pulled to logic "0"
2. ▒ Programmable connections

Programmable high-speed decoder logic (48 × 73 × 22)

PHD48N22–7

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS MIN	RATINGS MAX	UNIT
V_{CC}	Supply voltage	–0.5	+7	V_{DC}
V_{IN}	Input voltage	–0.5	+5.5	V_{DC}
V_{OUT}	Output voltage		+5.5	V_{DC}
I_{IN}	Input currents	–30	+30	mA
I_{OUT}	Output currents		+100	mA
T_{amb}	Operating temperature range	0	+75	°C
T_{stg}	Storage temperature range	–65	+150	°C

NOTES:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

OPERATING RANGES

SYMBOL	PARAMETER	RATINGS MIN	RATINGS MAX	UNIT
V_{CC}	Supply voltage	+4.75	+5.25	V_{DC}
T_{amb}	Operating free-air temperature	0	+75	°C

DC ELECTRICAL CHARACTERISTICS

$0°C \leq T_{amb} \leq +75°C$, $4.75 \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[1]	MAX	
Input voltage[2]						
V_{IL}	Low	V_{CC} = MIN			0.8	V
V_{IH}	High	V_{CC} = MAX	2.0			V
V_{IC}	Clamp	V_{CC} = MIN, I_{IN} = –18mA		-0.8	–1.5	V
Output voltage						
		V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}				
V_{OL}	Low	I_{OL} = +24mA			0.5	V
V_{OH}	High	I_{OH} = –3.2mA	2.4			V
Input current						
		V_{CC} = MAX				
I_{IL}	Low	V_{IN} = +0.40V		–20	–250	µA
I_{IH}	High	V_{IN} = +2.7V			25	µA
I_I	High	V_{IN} = V_{CC} = $V_{CC\ MAX}$			100	µA
Output current						
		V_{CC} = MAX				
I_{OZH}	Output leakage [3]	V_{OUT} = +2.7V			100	µA
I_{OZL}	Output leakage [3]	V_{OUT} = +0.40V			–100	µA
I_{OS}	Short circuit [4]	V_{OUT} = +0V	–30	–60	–90	mA
I_{CC}	V_{CC} current	V_{CC} = MAX			420	mA
Capacitance[5]						
		V_{CC} = +5V				
C_{IN}	Input	V_{IN} = 2.0V @ f = 1MHz		8		pF
C_{OUT}	I/O	V_{OUT} = 2.0V @ f = 1MHz		8		pF

NOTES:
1. Typical limits are at V_{CC} = 5.0V and T_{amb} = +25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. Leakage current for bidirectional pins is the worst case of I_{IL} and I_{OZL} or I_{IH} and I_{OZL}.
4. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second.
5. These parameters are not 100% tested, but are periodically sampled.

Programmable high-speed decoder logic (48 × 73 × 22)

PHD48N22–7

AC ELECTRICAL CHARACTERISTICS

$0°C \leq T_{amb} \leq +75°C$, $4.75 \leq V_{CC} \leq 5.25V$, $R_1 = 200\Omega$, $R_2 = 390\Omega$
Operating temerature at 200 CFM Minimum air flow.

SYMBOL	PARAMETER	FROM	TO	TEST CONDITIONS	LIMITS MIN	LIMITS MIN	UNIT
t_{PD1}[1]	Propagation delay through B/O outputs	(I, B, OR) ±	Output ±	$C_L = 50pF$		7.5	ns
t_{PD2}[1]	Propagation delay through OR outputs	(I, B, OR) ±	Output ±	$C_L = 50pF$		8.0	ns
t_{OE}[2]	Output Enable	(I, B, OR) ±	Output enable	$C_L = 50pF$		10	ns
t_{OD}[2]	Output Disable	(I, B, OR) ±	Output disable	$C_L = 5pF$		10	ns

NOTES:
1. $t_{PD1,2}$ are tested with switch S_1 closed and $C_L = 50pF$.
2. For 3-State output; output enable times are tested with $C_L = 50pF$ to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with $C_L = 5pF$. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} - 0.5V)$ with S_1 open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with S_1 closed.

VIRGIN STATE

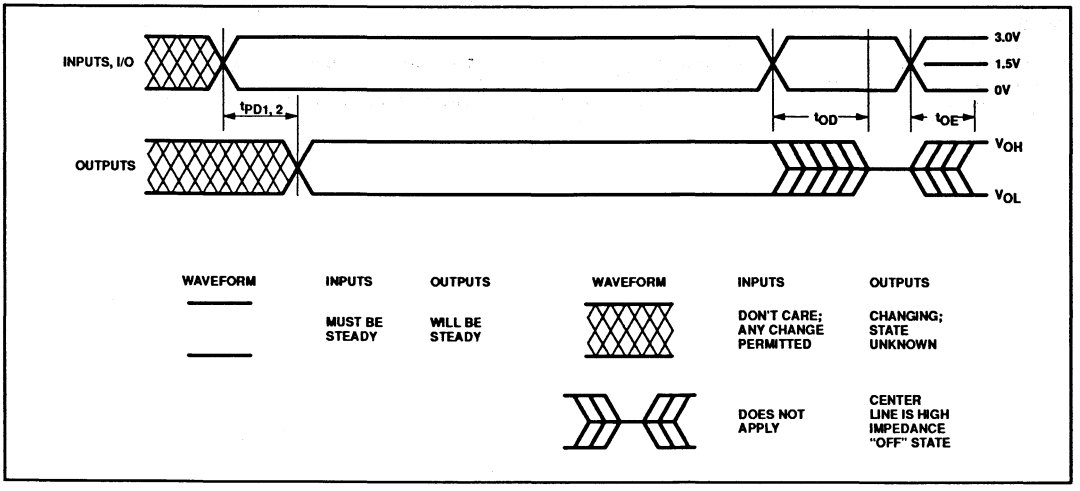
A factory shipped virgin device contains all fusible links intact, such that:

1. All outputs are disabled.
2. All p-terms are disabled in the AND array.

TIMING DEFINITIONS

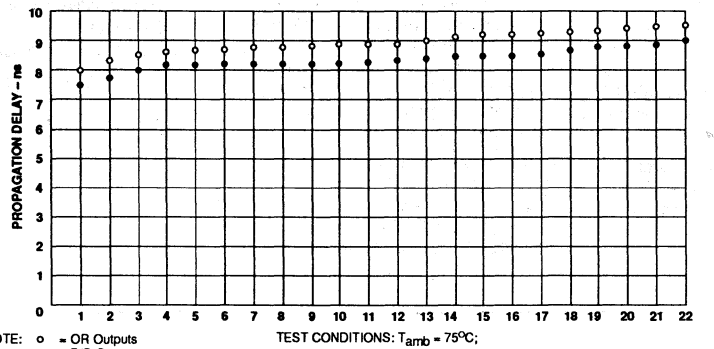
SYMBOL	PARAMETER
t_{PD1}	Input to output propagation delay (through B/O outputs).
t_{PD2}	Input to output propagation delay (through OR outputs).
t_{OD}	Input to Output Disable (3-State) delay (Output Disable).
t_{OE}	Input to Output Enable delay (Output Enable).

TIMING DIAGRAM



Programmable high-speed decoder logic (48 x 73 x 22)

PHD48N22–7

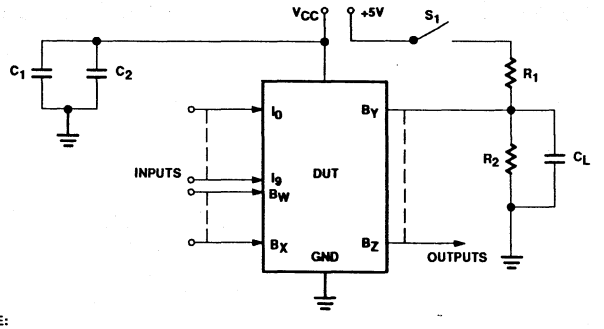


NOTE: o = OR Outputs
● = B/O Outputs

TEST CONDITIONS: T_{amb} = 75°C;
V_{CC} = 4.75V; C_L = 50pF;
R_1 = 200Ω; R_2 = 390Ω

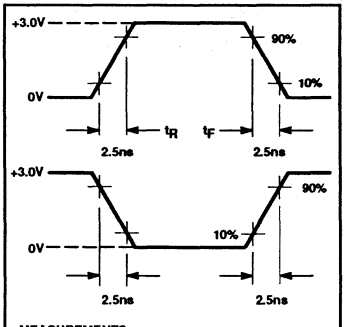
Worst-Case Propagation Delay vs. Number of Outputs Switching

AC TEST LOAD CIRCUIT



NOTE:
C_1 and C_2 are to bypass V_{CC} to GND.

VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

Programmable high-speed decoder logic (48 × 73 × 22)

PHD48N22–7

LOGIC PROGRAMMING

The PHD48N22–7 is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Signetics SLICE and SNAP design software packages. ABEL™ CUPL™ and PALASM® 90 design software packages also support the architecture.

All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

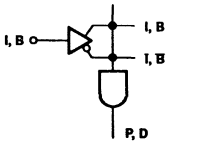
PHD48N22–7 logic designs can also be generated using the program table entry format, which is detailed on the following pages. This program table entry format is supported by SLICE. The SLICE design package is available, free of charge, to qualified users.

To implement the desired logic functions, each logic variable (I, B, P and D) from the logic equations is assigned a symbol. TRUE (High), COMPLEMENT (Low), DON'T CARE and INACTIVE symbols are defined below.

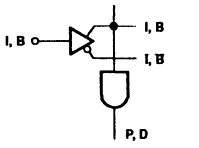
PROGRAMMING/SOFTWARE SUPPORT

Refer to Section 8 *(Development Software)* and Section 9 *(Third-Party Programmer/ Software Support)* of this data handbook for additional information.

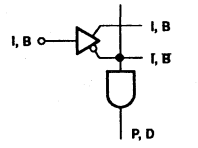
"AND" ARRAY – (I, B)



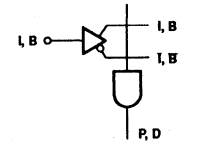
STATE	CODE
INACTIVE[1]	O



STATE	CODE
TRUE	H



STATE	CODE
COMPLEMENT	L



STATE	CODE
DON'T CARE	–

NOTE:
1. This is the initial state.

ABEL is a trademark of Data I/O Corp.
CUPL is a trademark of Logical Devices, Inc.
PALASM is a registered trademark of AMD Corp.

Programmable high-speed decoder logic (48 × 73 × 22)

PHD48N22–7

PROGRAM TABLE

TERM	INPUTS																																															
	I																																			B								OR			
	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	3	2	1	0
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PIN	42	41	40	39	37	36	35	34	33	31	30	29	28	27	26	25	24	23	22	20	19	18	17	16	13	12	11	10	9	8	7	6	5	3	2	1	52	51	50	47	46	45	44	43	68	67	65	64
VARIABLE NAME																																																

Programmable high-speed decoder logic (48 × 73 × 22)

PHD48N22–7

PROGRAM TABLE (Continued)

TERM	OUTPUTS																			
	O									B							OR			
	9	8	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	3	2	1	0
0																			D			
1																			A			
2																			A			
3																			A			
4																			A			
5																			A			
6																			A			
7																			A			
8																				D		
9																				A		
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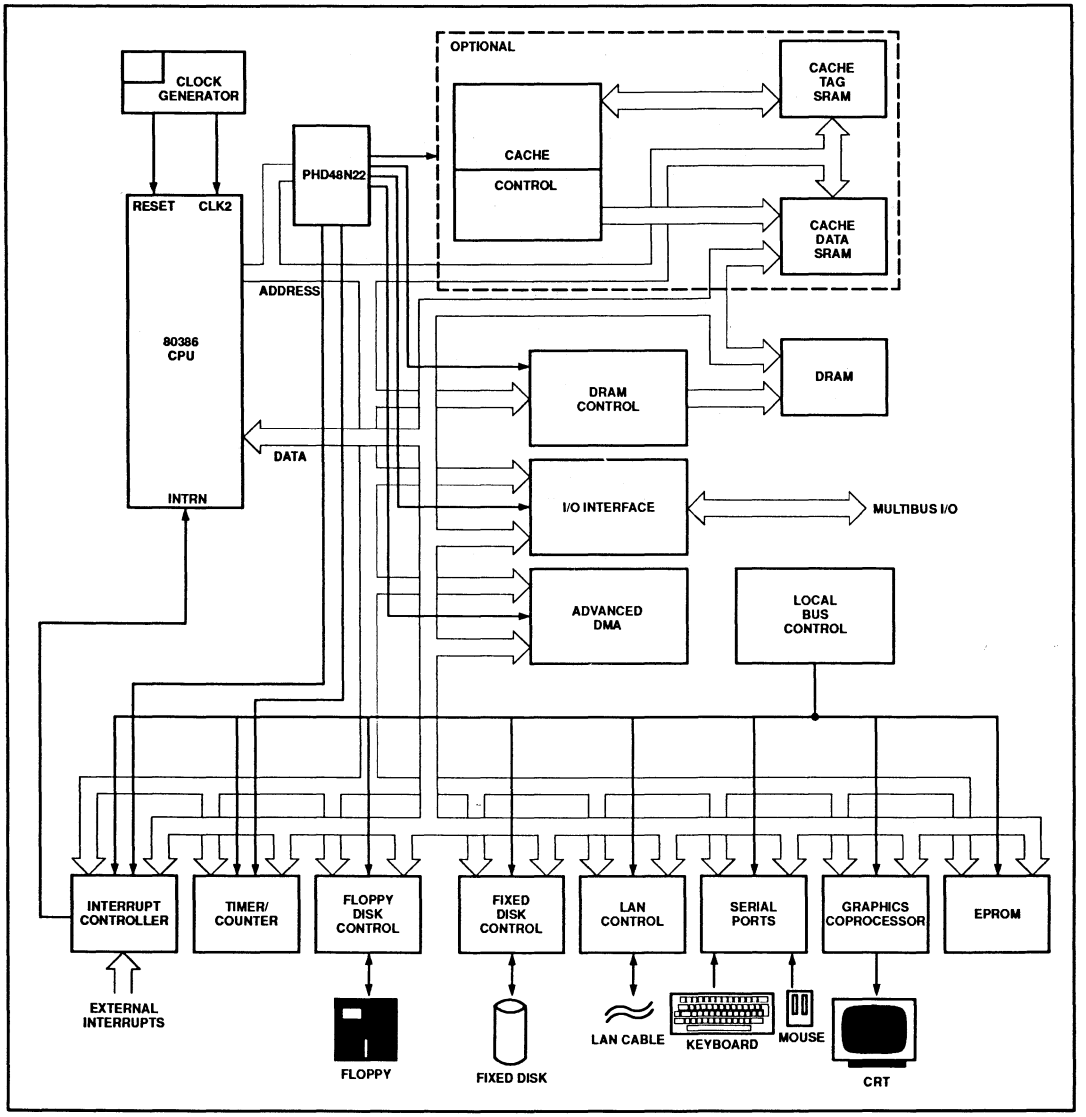
68																A						
69																	D					
70																	A					
71																		D				
72																		A				
PIN	63	62	61	60	59	58	57	56	54	53	52	51	50	47	46	45	44	43	68	67	65	64
VARIABLE NAME																						

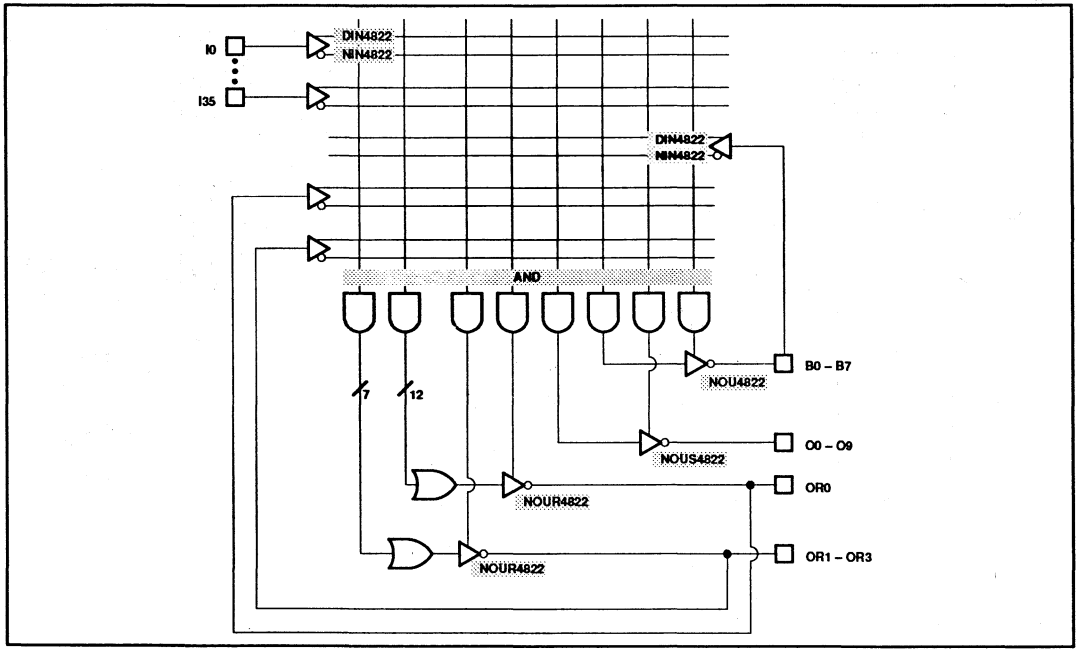
Programmable high-speed decoder logic (48 x 73 x 22) PHD48N22–7

TYPICAL SYSTEM APPLICATION



Programmable high-speed decoder logic (48 × 73 × 22) — PHD48N22–7

SNAP RESOURCE SUMMARY DESIGNATIONS



Section 4
Programmable Logic Array Device Data Sheets

INDEX

Programmable logic arrays (18 × 42 × 10)

PLS153/A

DESCRIPTION

The PLS153 and PLS153A are two-level logic elements, consisting of 42 AND gates and 10 OR gates with fusible link connections for programming I/O polarity and direction.

All AND gates are linked to 8 inputs (I) and 10 bidirectional I/O lines (B). These yield variable I/O gate configurations via 10 direction control gates (D), ranging from 18 inputs to 10 outputs.

On-chip T/C buffers couple either True (I, B) or Complement ($\overline{I}$, $\overline{B}$) input polarities to all AND gates, whose outputs can be optionally linked to all OR gates. Their output polarity, in turn, is individually programmable through a set of EX-OR gates for implementing AND/OR or AND/NOR logic functions.

The PLS153 and PLS153A are field-programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

FEATURES

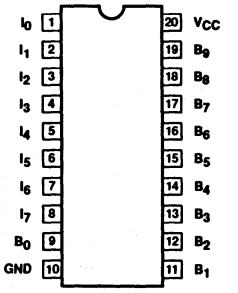
- Field-Programmable (Ni-Cr links)
- 8 inputs
- 42 AND gates
- 10 OR gates
- 10 bidirectional I/O lines
- Active-High or -Low outputs
- 42 product terms:
  - 32 logic terms
  - 10 control terms
- I/O propagation delay:
  - PLS153: 40ns (max)
  - PLS153A: 30ns (max)
- Input loading: −100μA (max)
- Power dissipation: 650mA (typ)
- 3-State outputs
- TTL compatible

APPLICATIONS

- Random logic
- Code converters
- Fault detectors
- Function generators
- Address mapping
- Multiplexing

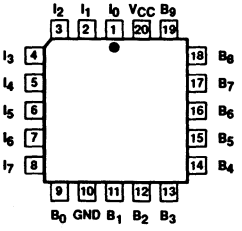
PIN CONFIGURATIONS

N Package



N = Plastic DIP (300mil-wide)

A Package



A = Plastic Leaded Chip Carrier

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
20-Pin Plastic Dual In-Line, 300mil-wide	PLS153N, PLS153AN
20-Pin Plastic Leaded Chip Carrier	PLS153A, PLS153AA

LOGIC FUNCTION

TYPICAL PRODUCT TERM:

$Pn = A \cdot B \cdot C \cdot D \cdot \ldots$

TYPICAL LOGIC FUNCTION:

AT OUTPUT POLARITY = H

$Z = P0 + P1 + P2 \ldots$

AT OUTPUT POLARITY = L

$Z = \overline{P0 + P1 + P2 + \ldots}$

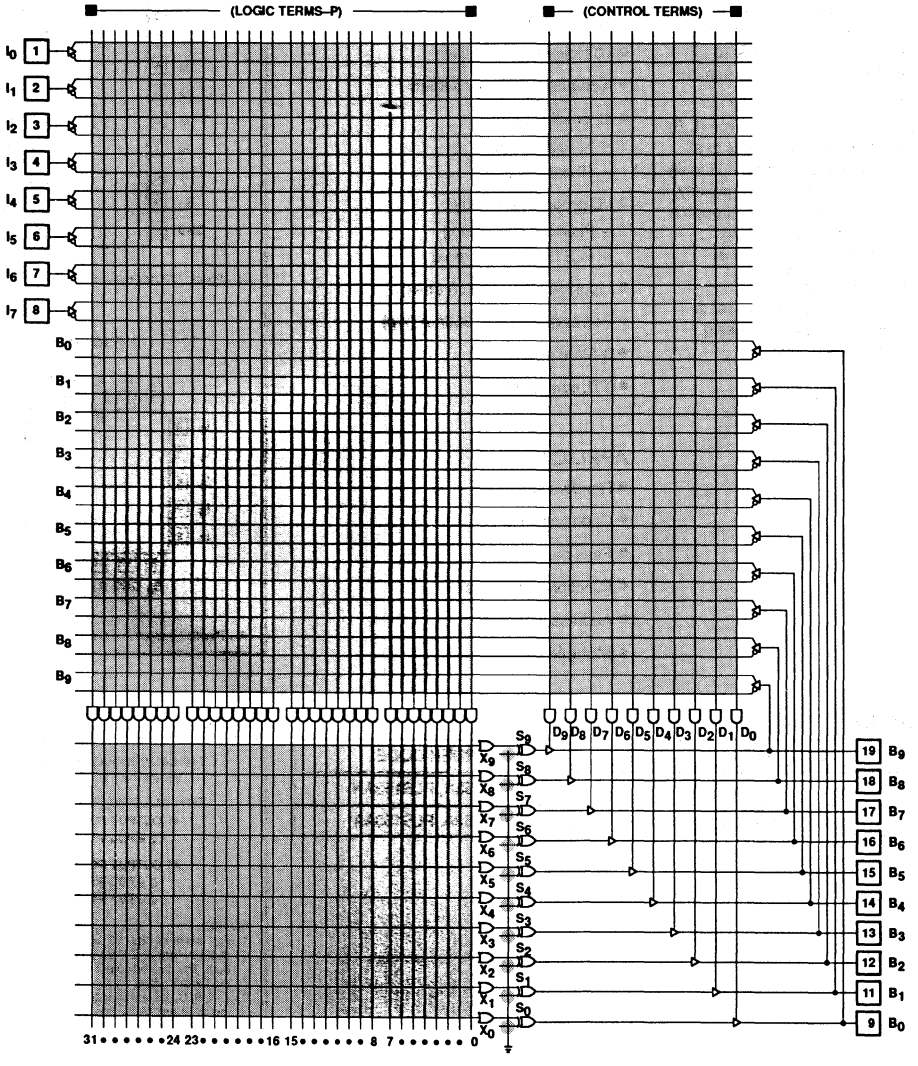
$Z = \overline{P0} \cdot \overline{P1} \cdot \overline{P2} \cdot \ldots$

NOTES:
1. For each of the 10 outputs, either function Z (Active-High) or Z (Active-Low) is available, but not both. The desired output polarity is programmed via the Ex-OR gates.
2. Z, A, B, C, etc. are user defined connections to fixed inputs (I) and bidirectional pins (B).

Programmable logic arrays (18 × 42 × 10)

PLS153/A

LOGIC DIAGRAM

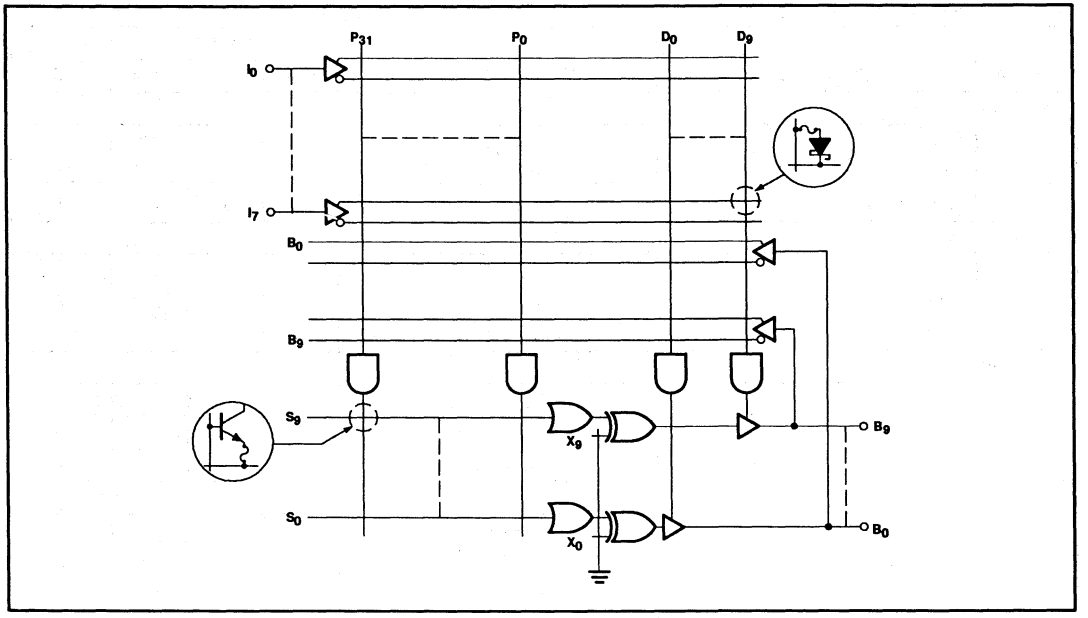


NOTES:
1. All programmed 'AND' gate locations are pulled to logic "1".
2. All programmed 'OR' gate locations are pulled to logic "0".
3. ⊗ Programmable connection.

Programmable logic arrays (18 × 42 × 10)

PLS153/A

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS MIN	RATINGS MAX	UNIT
V_{CC}	Supply voltage		+7	V_{DC}
V_{IN}	Input voltage		+5.5	V_{DC}
V_{OUT}	Output voltage		+5.5	V_{DC}
I_{IN}	Input currents	–30	+30	mA
I_{OUT}	Output currents		+100	mA
T_{amb}	Operating temperature range	0	+75	°C
T_{stg}	Storage temperature range	–65	+150	°C

NOTES:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

The PLS153/A devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Handbook.

DC ELECTRICAL CHARACTERISTICS

$0°C \leq T_{amb} \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[1]	MAX	
Input voltage[2]						
V_{IL}	Low	V_{CC} = MIN			0.8	V
V_{IH}	High	V_{CC} = MAX	2.0			V
V_{IC}	Clamp[3]	V_{CC} = MIN, I_{IN} = –12mA		–0.8	–1.2	V
Output voltage[2]						
		V_{CC} = MIN				
V_{OL}	Low[4]	I_{OL} = 15mA			0.5	V
V_{OH}	High[5]	I_{OH} = –2mA	2.4			V
Input current[9]						
		V_{CC} = MAX				
I_{IL}	Low	V_{IN} = 0.45V			–100	μA
I_{IH}	High	V_{IN} = 5.5V			40	μA
Output current						
		V_{CC} = MAX				
$I_{O(OFF)}$	Hi-Z state[8]	V_{OUT} = 5.5V			80	μA
		V_{OUT} = 0.45V			–140	
I_{OS}	Short circuit[3, 5, 6]	V_{OUT} = 0V	–15		–70	mA
I_{CC}	V_{CC} supply current[7]	V_{CC} = MAX		130	155	mA
Capacitance						
		V_{CC} = 5V				
C_{IN}	Input	V_{IN} = 2.0V		8		pF
C_B	I/O	V_B = 2.0V		15		pF

NOTES:
1. All typical values are at V_{CC} = 5V, T_{amb} = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Test one at a time.
4. Measured with +10V applied to I_7.
5. Measured with +10V applied to I_{0-7}. Output sink current is supplied through a resistor to V_{CC}.
6. Duration of short circuit should not exceed 1 second.
7. I_{CC} is measured with I_0, I_1 at 0V, $I_2 - I_7$ and B_{0-9} at 4.5V.
8. Leakage values are a combination of input and output leakage.
9. I_{IL} and I_{IH} limits are for dedicated inputs only ($I_0 - I_7$).

Programmable logic arrays (18 × 42 × 10)

PLS153/A

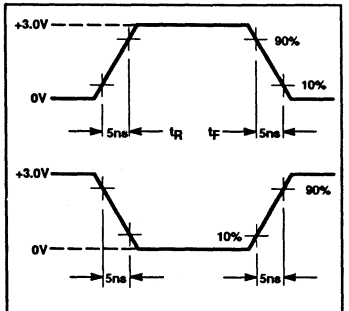
AC ELECTRICAL CHARACTERISTICS

$0°C \le T_{amb} \le +75°C$, $4.75V \le V_{CC} \le 5.25V$, $R_1 = 300\Omega$, $R_2 = 390\Omega$

SYMBOL	PARAMETER	FROM	TO	TEST CONDITION	LIMITS						UNIT
					PLS153			PLS153A			
					MIN	TYP[1]	MAX	MIN	TYP[1]	MAX	
t_{PD}	Propagation delay	Input ±	Output ±	C_L = 30pF		30	40		20	30	ns
t_{OE}	Output enable[2]	Input ±	Output –	C_L = 30pF		25	35		20	30	ns
t_{OD}	Output disable[2]	Input ±	Output +	C_L = 5pF		25	35		20	30	ns

NOTES:
1. All typical values are at V_{CC} = 5V, T_{amb} = +25°C.
2. For 3-State output; output enable times are tested with C_L = 30pF to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with C_L = 5pF. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} - 0.5V)$ with S_1 open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with S_1 closed.
3. All propagation delays are measured and specified under worst case conditions.

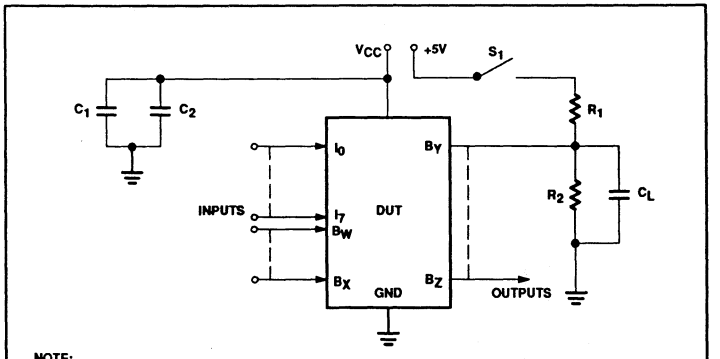
VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

TEST LOAD CIRCUIT

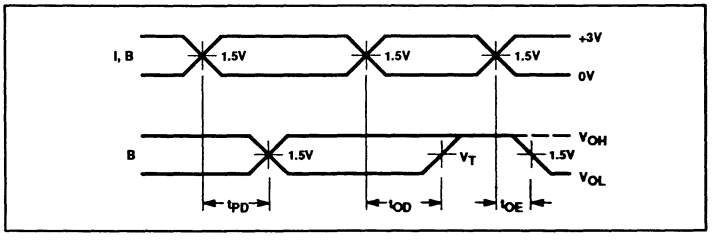


NOTE:
C_1 and C_2 are to bypass V_{CC} to GND.

TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{PD}	Propagation delay between input and output.
t_{OD}	Delay between input change and when output is off (Hi-Z or High).
t_{OE}	Delay between input change and when output reflects specified output level.

TIMING DIAGRAM



Programmable logic arrays (18 × 42 × 10)

PLS153/A

LOGIC PROGRAMMING

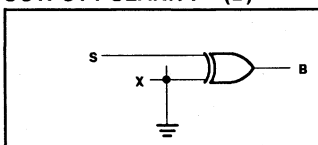
The PLS153/A is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Signetics SLICE and SNAP, Data I/O's ABEL™ and Logical Devices, Inc. CUPL™ design software packages.

All packages allow Boolean and state equation entry formats. SNAP ABEL and CUPL also accept, as input, schematic capture format.

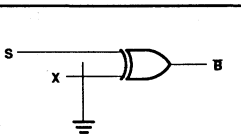
PLS153/A logic designs can also be generated using the program table entry format detailed on the following page. This program table entry format is supported by the Signetics SLICE and SNAP PLD design software packages (PTP module). SLICE is available free of charge to qualified users. b

To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

OUTPUT POLARITY – (B)

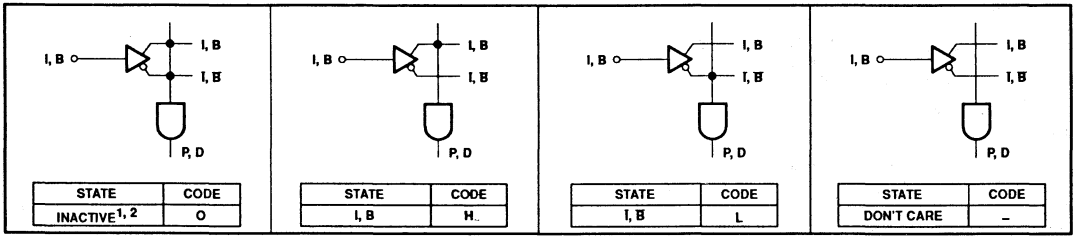


ACTIVE LEVEL	CODE
HIGH[1] (NON-INVERTING)	H



ACTIVE LEVEL	CODE
LOW (INVERTING)	L

AND ARRAY – (I, B)



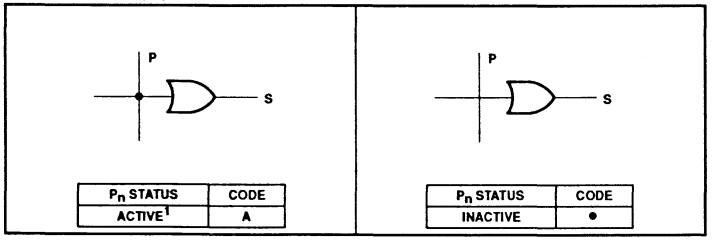
STATE	CODE
INACTIVE[1, 2]	O

STATE	CODE
I, B	H

STATE	CODE
I, B̄	L

STATE	CODE
DON'T CARE	–

OR ARRAY – (B)



P_n STATUS	CODE
ACTIVE[1]	A

P_n STATUS	CODE
INACTIVE	•

NOTES:
1. This is the initial unprogrammed state of all links.
2. Any gate P_n will be unconditioanlly inhibited if both the True and Complement of an input (either I or B) are left intact.

VIRGIN STATE

A factory shipped virgin device contains all fusible links intact, such that:

1. All outputs are at "H" polarity.
2. All P_n terms are disabled.
3. All P_n terms are active on all outputs.

CAUTION: PLS153A TEST COLUMNS

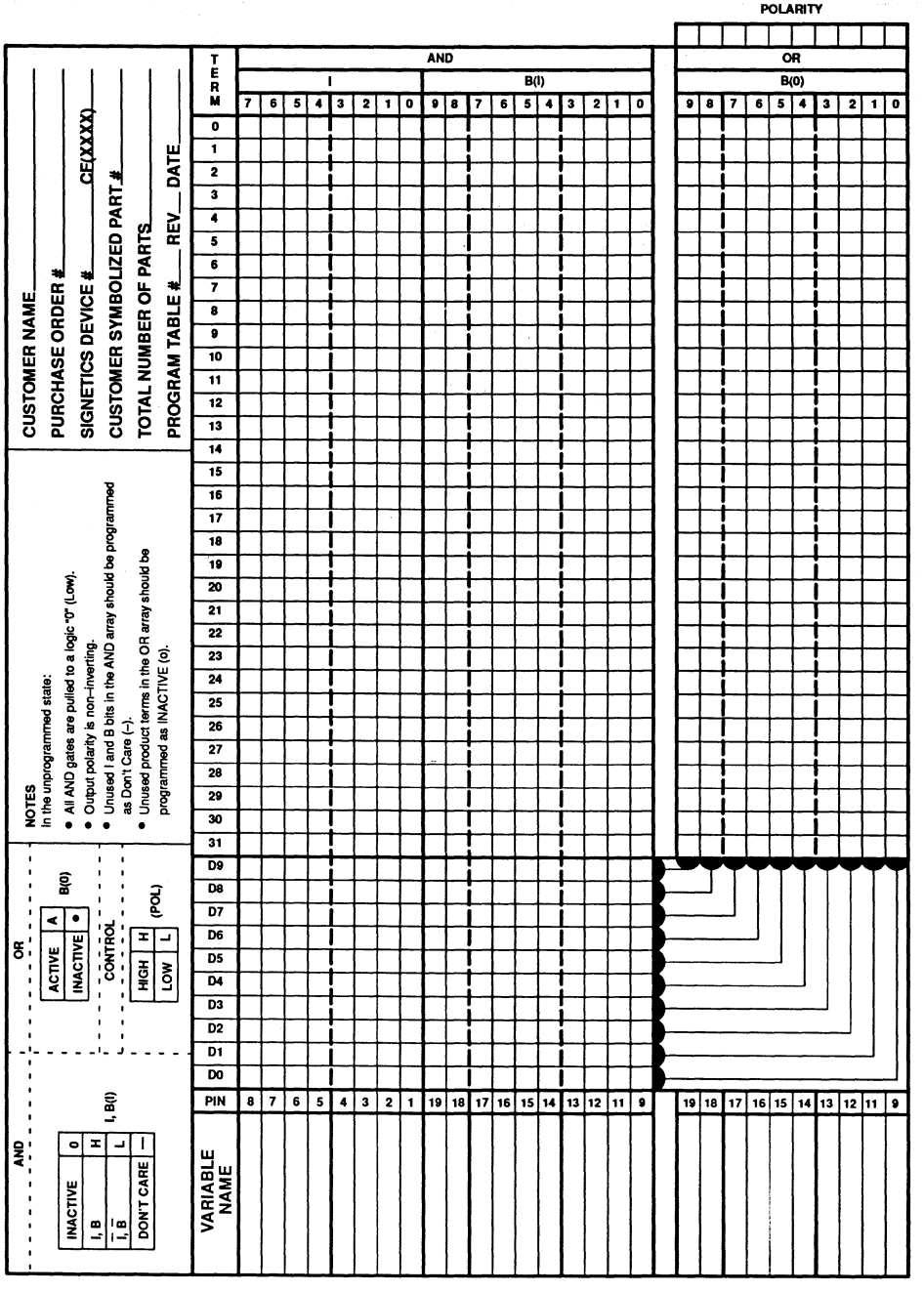
The PLS153A incorporates two columns not shown in the logic block diagram. These columns are used for in-house testing of the device in the unprogrammed state. These columns must be disabled prior to using the PLS153A in your application. If you are using a Signetics-approved programmer, the disabling is accomplished during the device programming sequence. If these columns are not disabled, abnormal operation is possible.

Furthermore, because of these test columns, the PLS153A cannot be programmed using the programmer algorithm for the PLS153.

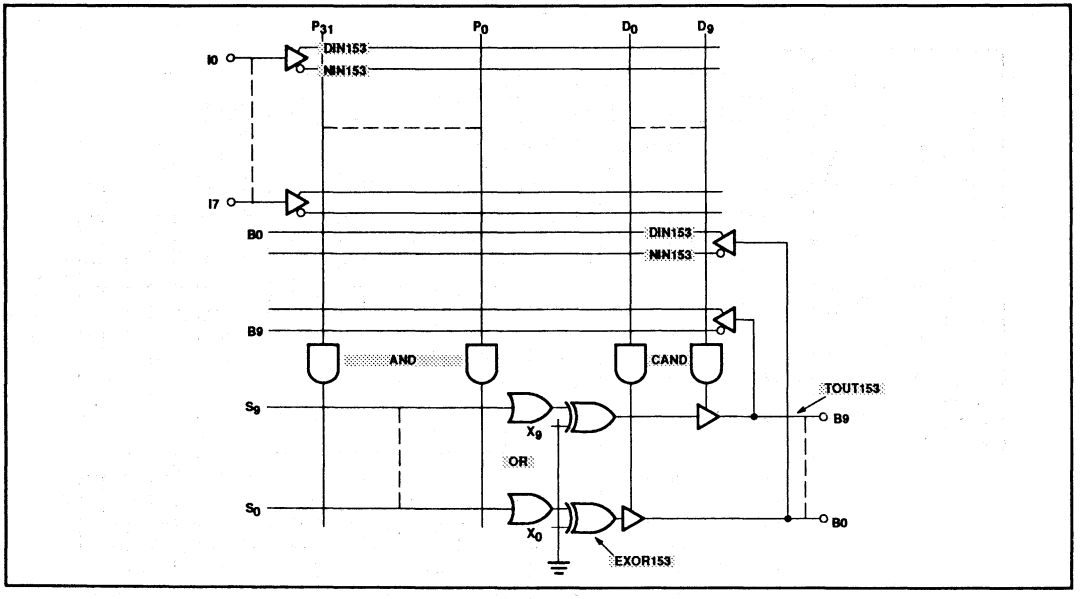
Programmable logic arrays (18 × 42 × 10)

PLS153/A

PROGRAM TABLE



SNAP RESOURCE SUMMARY DESIGNATIONS



Programmable logic arrays (18 × 42 × 10)

PLUS153B/D

DESCRIPTION

The PLUS153 PLDs are high speed, combinatorial Programmable Logic Arrays. The Signetics state-of-the-art Oxide Isolated Bipolar fabrication process is employed to produce propagation delays as short as 12ns.

The 20-pin PLUS153 devices have a programmable AND array and a programmable OR array. Unlike PAL® devices, 100% product term sharing is supported. Any of the 32 logic product terms can be connected to any or all of the 10 output OR gates. Most PAL ICs are limited to 7 AND terms per OR function; the PLUS153 devices can support up to 32 input wide OR functions.

The polarity of each output is user-programmable as either active-High or active-Low, thus allowing AND-OR or AND-NOR logic implementation. This feature adds an element of design flexibility, particularly when implementing complex decoding functions.

The PLUS153 devices are user-programmable using one of several commercially available, industry standard PLD programmers.

FEATURES

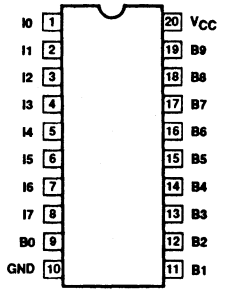
- I/O propagation delays (worst case)
  - PLUS153B – 15ns max.
  - PLUS153D – 12ns max.
- Functional superset of 16L8 and most other 20-pin combinatorial PAL devices
- Two programmable arrays
  - Supports 32 input wide OR functions
- 8 inputs
- 10 bi-directional I/O
- 42 AND gates
  - 32 logic product terms
  - 10 direction control terms
- Programmable output polarity
  - Active-High or Active-Low
- Security fuse
- 3-State outputs
- Power dissipation: 750mW (typ.)
- TTL Compatible

APPLICATIONS

- Random logic
- Code converters
- Fault detectors
- Function generators
- Address mapping
- Multiplexing

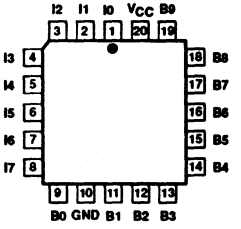
PIN CONFIGURATIONS

N Package



N = Plastic Dual In-Line Package (300mil-wide)

A Package



A = Plastic Leaded Chip Carrier

ORDERING INFORMATION

DESCRIPTION	t_{PD} (MAX)	ORDER CODE
20-Pin Plastic Dual-In-Line 300mil-wide	15ns	PLUS153BN
20-Pin Plastic Dual-In-Line 300mil-wide	12ns	PLUS153DN
20-Pin Plastic Leaded Chip Carrier	15ns	PLUS153BA
20-Pin Plastic Leaded Chip Carrier	12ns	PLUS153DA

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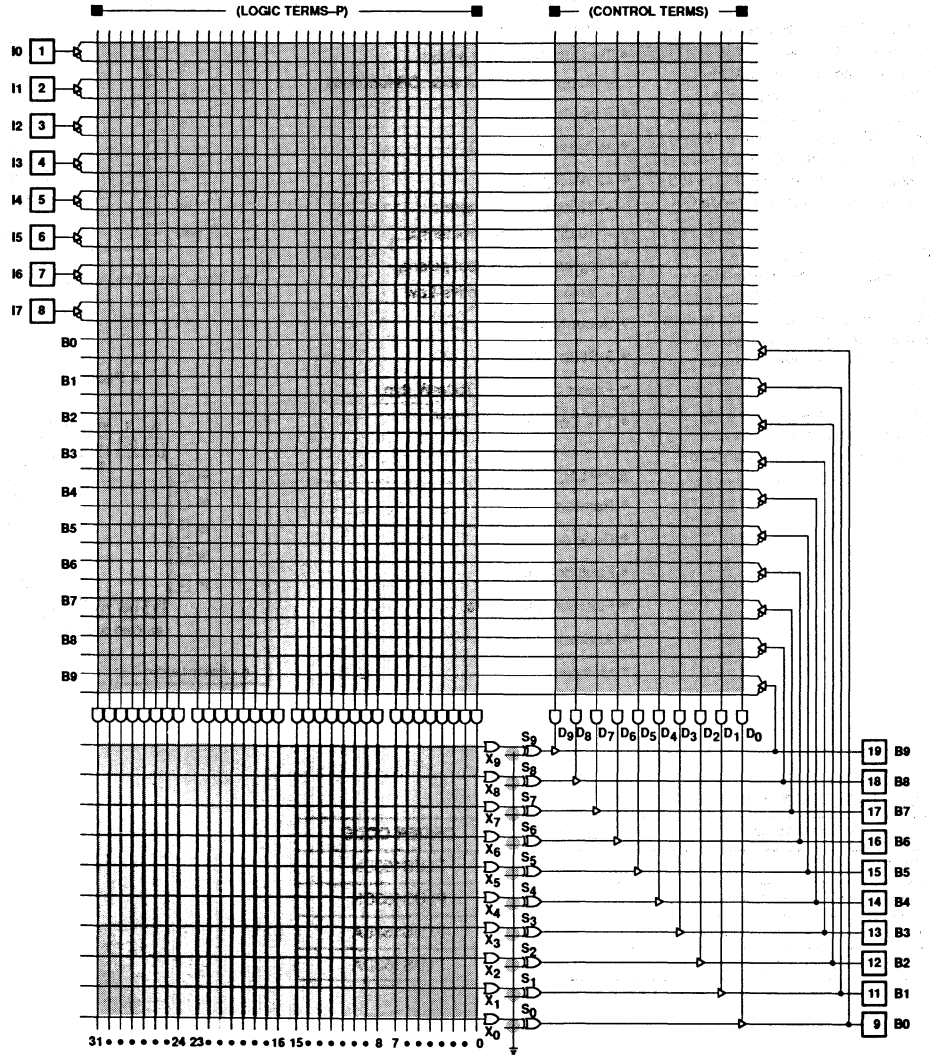
Programmable logic arrays (18 × 42 × 10)

PLUS153B/D

LOGIC DIAGRAM

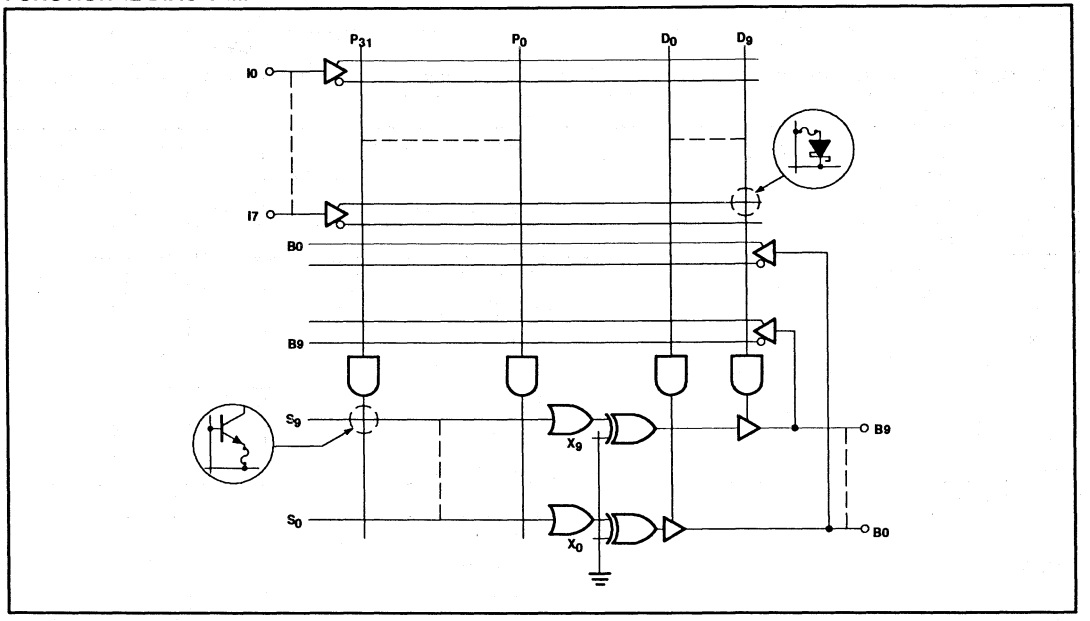


NOTES:
1. All programmed 'AND' gate locations are pulled to logic "1".
2. All programmed 'OR' gate locations are pulled to logic "0".
3. ▒ Programmable connection.

Programmable logic arrays (18 × 42 × 10)

PLUS153B/D

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING MIN	RATING MAX	UNIT
V_{CC}	Supply voltage		+7	V_{DC}
V_{IN}	Input voltage		+5.5	V_{DC}
V_{OUT}	Output voltage		+5.5	V_{DC}
I_{IN}	Input currents	–30	+30	mA
I_{OUT}	Output currents		+100	mA
T_{amb}	Operating free-air temperature range	0	+75	°C
T_{stg}	Storage temperature range	–65	+150	°C

NOTES:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

DC ELECTRICAL CHARACTERISTICS

$0°C \leq T_{amb} \leq +75°C$, $4.75 \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[1]	MAX	
Input voltage[2]						
V_{IL}	Low	V_{CC} = MIN			0.8	V
V_{IH}	High	V_{CC} = MAX	2.0			V
V_{IC}	Clamp	V_{CC} = MIN, I_{IN} = –12mA		–0.8	–1.2	V
Output voltage[2]						
		V_{CC} = MIN				
V_{OL}	Low[4]	I_{OL} = 15mA			0.5	V
V_{OH}	High[5]	I_{OH} = –2mA	2.4			V
Input current[9]						
		V_{CC} = MAX				
I_{IL}	Low	V_{IN} = 0.45V			–100	µA
I_{IH}	High	V_{IN} = V_{CC}			40	µA
Output current						
		V_{CC} = MAX				
$I_{O(OFF)}$	Hi-Z state[8]	V_{OUT} = 2.7V			80	µA
		V_{OUT} = 0.45V			–140	
I_{OS}	Short circuit[3, 5, 6]	V_{OUT} = 0V	–15		–70	mA
I_{CC}	V_{CC} supply current[7]	V_{CC} = MAX		150	200	mA
Capacitance						
		V_{CC} = 5V				
C_{IN}	Input	V_{IN} = 2.0V		8		pF
C_B	I/O	V_B = 2.0V		15		pF

NOTES:

1. All typical values are at V_{CC} = 5V, T_{amb} = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Test one at a time.
4. Measured with inputs I0 – I2 = 0V, inputs I3 – I5 = 4.5V, inputs I7 = 4.5V and I6 = 10V. For outputs B0 – B4 and for outputs B5 – B9 apply the same conditions except I7 = 0V.
5. Same conditions as Note 4 except I7 = +10V.
6. Duration of short circuit should not exceed 1 second.
7. I_{CC} is measured with inputs I0 – I7 and B0 – B9 = 0V.
8. Leakage values are a combination of input and output leakage.
9. I_{IL} and I_{IH} limits are for dedicated inputs only (I0 – I7).

Programmable logic arrays (18 x 42 x 10)

PLUS153B/D

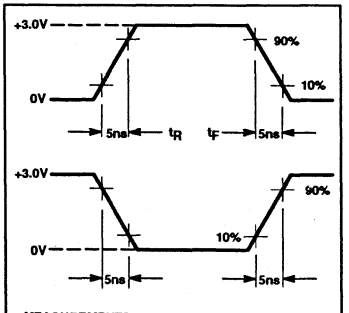
AC ELECTRICAL CHARACTERISTICS

$0°C \le T_{amb} \le +75°C$, $4.75V \le V_{CC} \le 5.25V$, $R_1 = 300\Omega$, $R_2 = 390\Omega$

SYMBOL	PARAMETER	FROM	TO	TEST CONDITION	LIMITS						UNIT
					PLUS153B			PLUS153D			
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{PD}	Propagation Delay[2]	Input +/–	Output +/–	C_L = 30pF		11	15		10	12	ns
t_{OE}	Output Enable[1]	Input +/–	Output –	C_L = 30pF		11	15		10	12	ns
t_{OD}	Output Disable[1]	Input +/–	Output +	C_L = 5pF		11	15		10	12	ns

NOTES:
1. For 3-State output; output enable times are tested with C_L = 30pF to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with C_L = 5pF. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} - 0.5V)$ with S_1 open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with S_1 closed.
2. All propagation delays are measured and specified under worst case conditions.

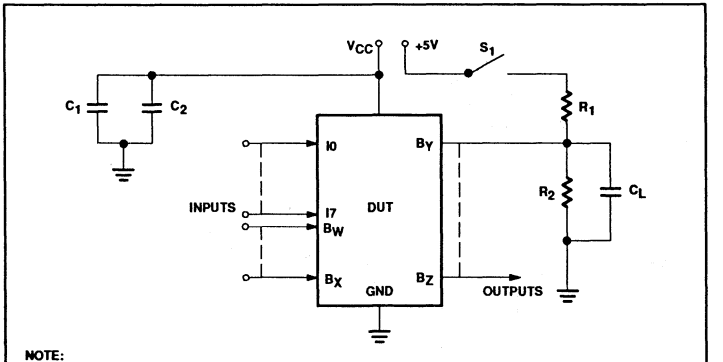
VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

TEST LOAD CIRCUIT

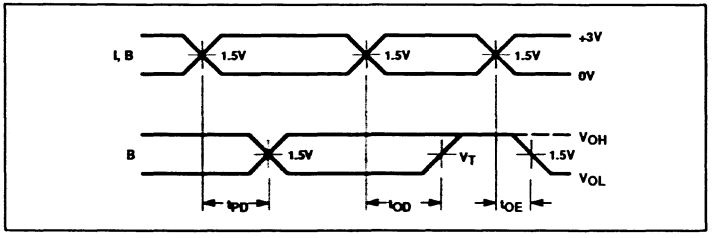


NOTE:
C_1 and C_2 are to bypass V_{CC} to GND.

TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{PD}	Propagation delay between input and output.
t_{OD}	Delay between input change and when output is off (Hi-Z or High).
t_{OE}	Delay between input change and when output reflects specified output level.

TIMING DIAGRAM



Programmable logic arrays (18 × 42 × 10)

PLUS153B/D

LOGIC PROGRAMMING

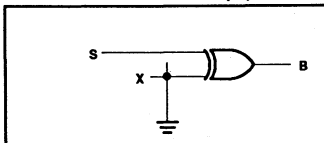
The PLUS153B/D is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Signetics SLICE and SNAP design software packages. ABEL™ and CUPL™ design software packages also support the PLUS153B/D architecture.

All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

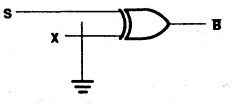
PLUS153B/D logic designs can also be generated using the program table entry format, which is detailed on the following page. This program table entry format is supported by SNAP and SLICE only. The SLICE design package is available, free of charge, to qualified users.

To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

OUTPUT POLARITY – (B)

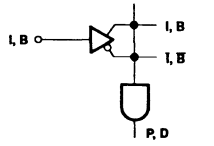


ACTIVE LEVEL	CODE
HIGH[1] (NON-INVERTING)	H

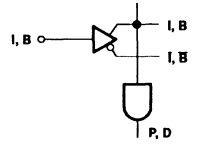


ACTIVE LEVEL	CODE
LOW (INVERTING)	L

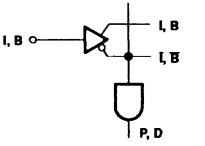
AND ARRAY – (I, B)



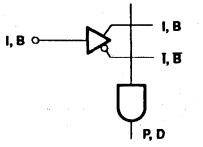
STATE	CODE
INACTIVE[1, 2]	O



STATE	CODE
I, B	H

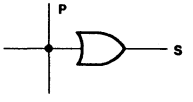


STATE	CODE
I, B̄	L

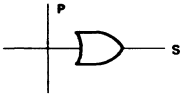


STATE	CODE
DON'T CARE	–

OR ARRAY – (B)



P_n STATUS	CODE
ACTIVE[1]	A



P_n STATUS	CODE
INACTIVE	•

NOTES:
1. This is the initial unprogrammed state of all links.
2. Any gate P_n will be unconditionally inhibited if both the true and complement of an input (either I or B) are left intact.

VIRGIN STATE

A factory shipped virgin device contains all fusible links intact, such that:

1. All outputs are at "H" polarity.
2. All P_n terms are disabled.
3. All P_n terms are active on all outputs.

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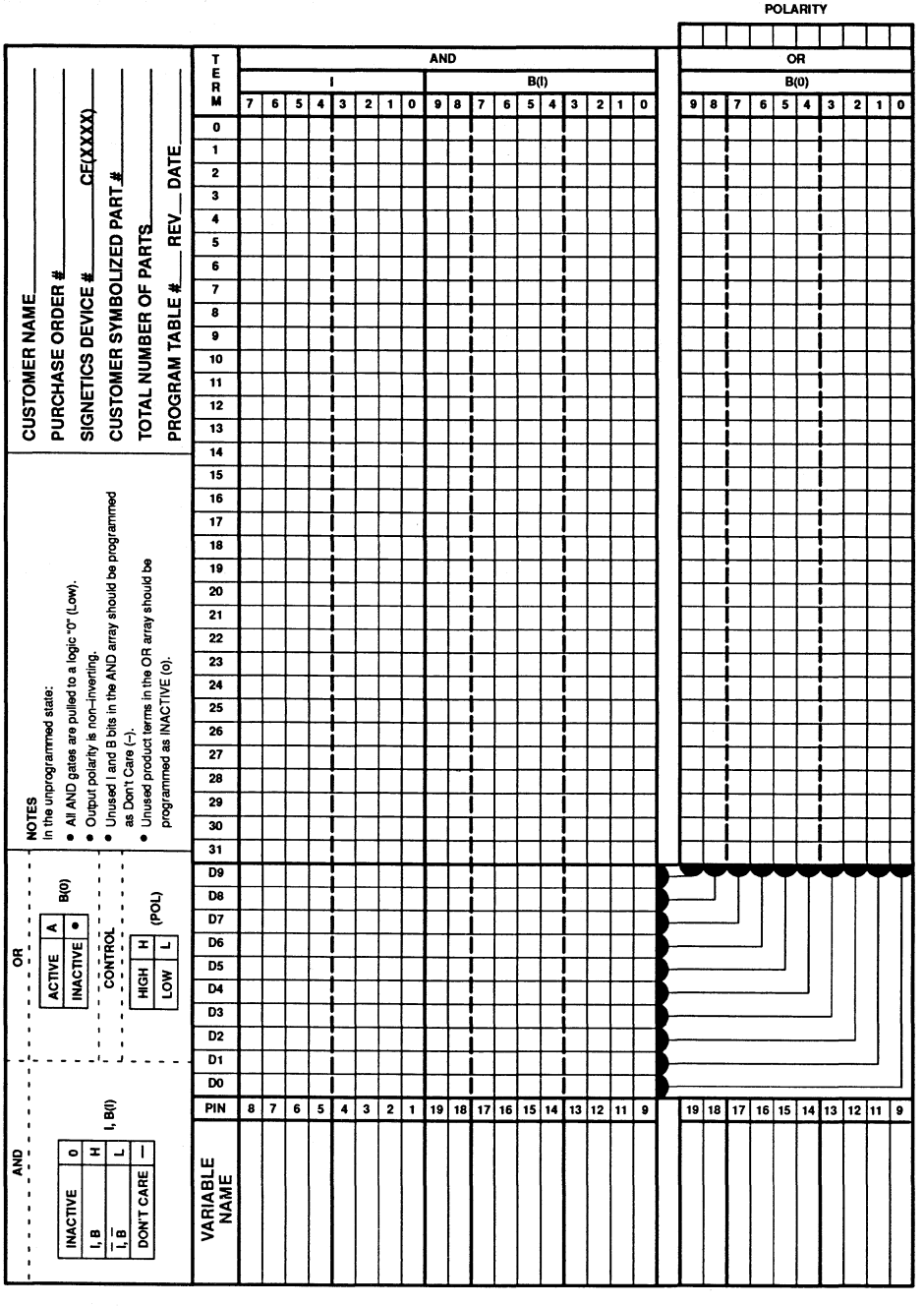
CUPL is a trademark of Logical Devices, Inc.

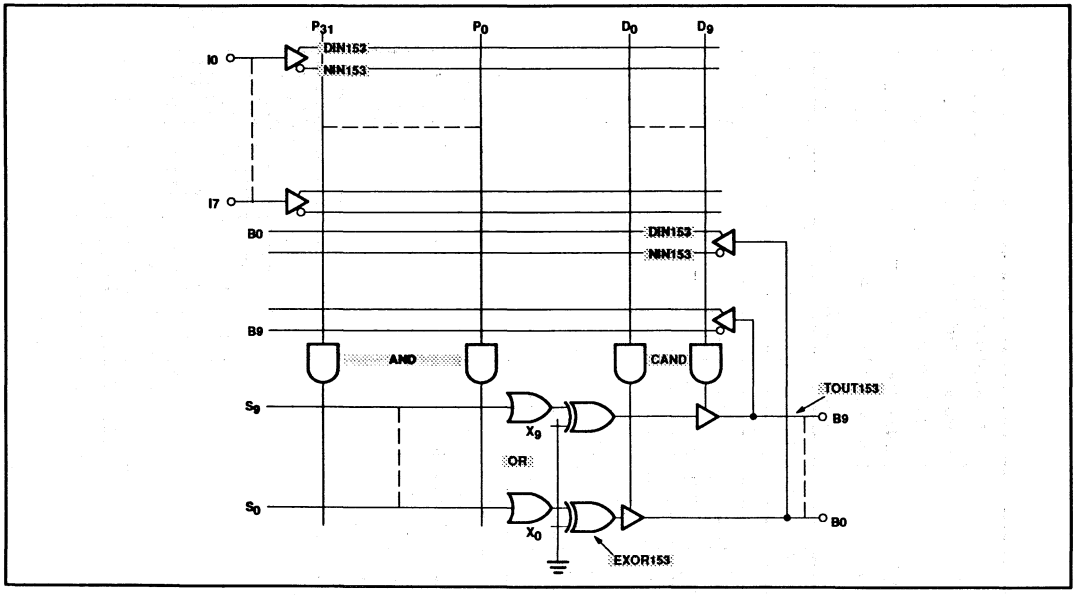
Programmable logic arrays (18 × 42 × 10)

PLUS153B/D

ROGRAM TABLE



SNAP RESOURCE SUMMARY DESIGNATIONS



Programmable logic array (18 × 42 × 10)

PLUS153–10

DESCRIPTION

The PLUS153–10 PLD is a high speed, combinatorial Programmable Logic Array. The Signetics state-of-the-art Oxide Isolated Bipolar fabrication process is employed to produce maximum propagation delays of 10ns or less.

The 20-pin PLUS153 device has a programmable AND array and a programmable OR array. Unlike PAL® devices, 100% product term sharing is supported. Any of the 32 logic product terms can be connected to any or all of the 10 output OR gates. Most PAL ICs are limited to 7 AND terms per OR function; the PLUS153–10 can support up to 32 input wide OR functions.

The polarity of each output is user-programmable as either Active-High or Active-Low, thus allowing AND-OR or AND-NOR logic implementation. This feature adds an element of design flexibility, particularly when implementing complex decoding functions.

The PLUS153–10 device is user-programmable using one of several commercially available, industry standard PLD programmers.

FEATURES

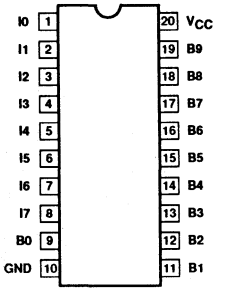
- I/O propagation delays (worst case)
  - PLUS153–10 – 10ns max.
- Functional superset of 16L8 and most other 20-pin combinatorial PAL devices
- Two programmable arrays
  - Supports 32 input wide OR functions
- 8 inputs
- 10 bi-directional I/O
- 42 AND gates
  - 32 logic product terms
  - 10 direction control terms
- Programmable output polarity
  - Active-High or Active-Low
- Security fuse
- 3-State outputs
- Power dissipation: 825mW (typ.)
- TTL Compatible

APPLICATIONS

- Random logic
- Code converters
- Fault detectors
- Function generators
- Address mapping
- Multiplexing

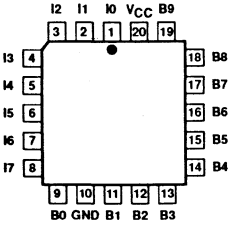
PIN CONFIGURATIONS

N Package



N = Plastic DIP (300mil-wide)

A Package



A = Plastic Leaded Chip Carrier

ORDERING INFORMATION

DESCRIPTION	t_{PD} (MAX)	ORDER CODE
20-Pin Plastic Dual-In-Line 300mil-wide	10ns	PLUS153–10N
20-Pin Plastic Leaded Chip Carrier	10ns	PLUS153–10A

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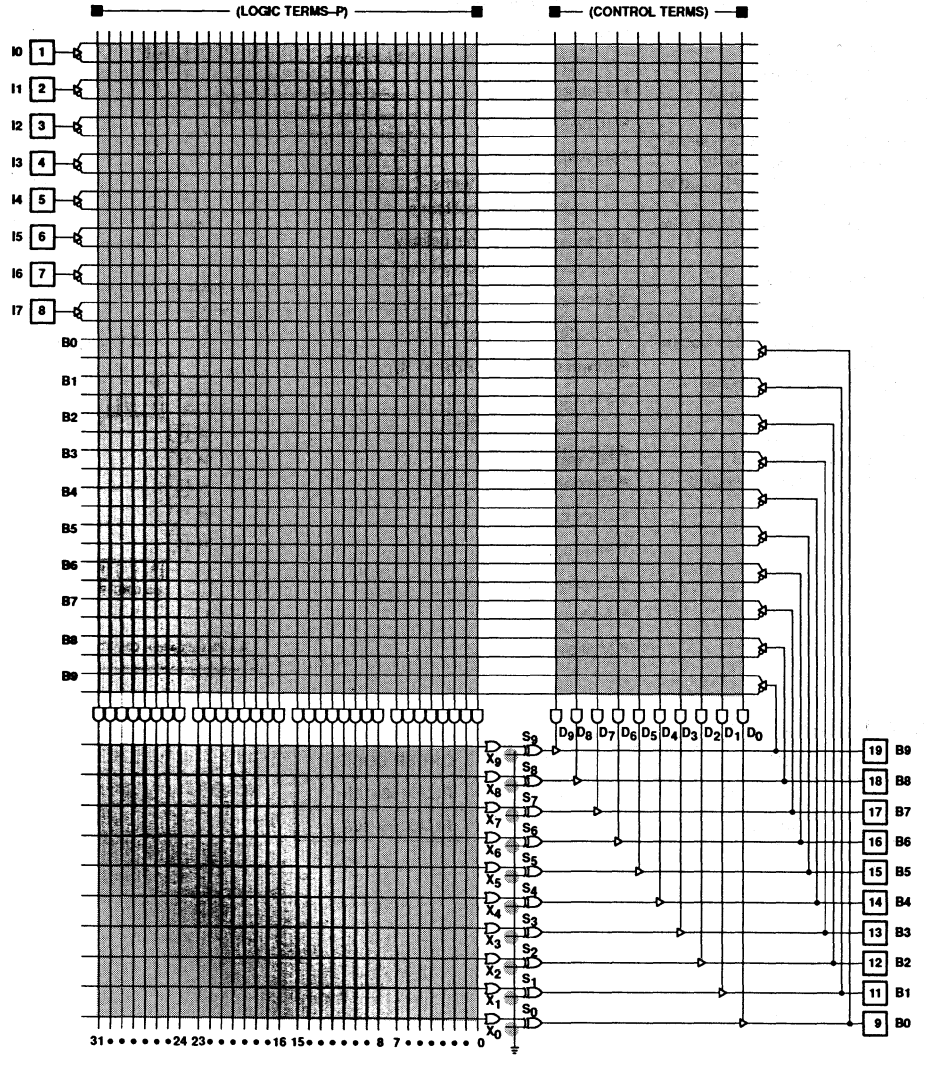
Programmable logic array (18 × 42 × 10)

PLUS153–10

LOGIC DIAGRAM

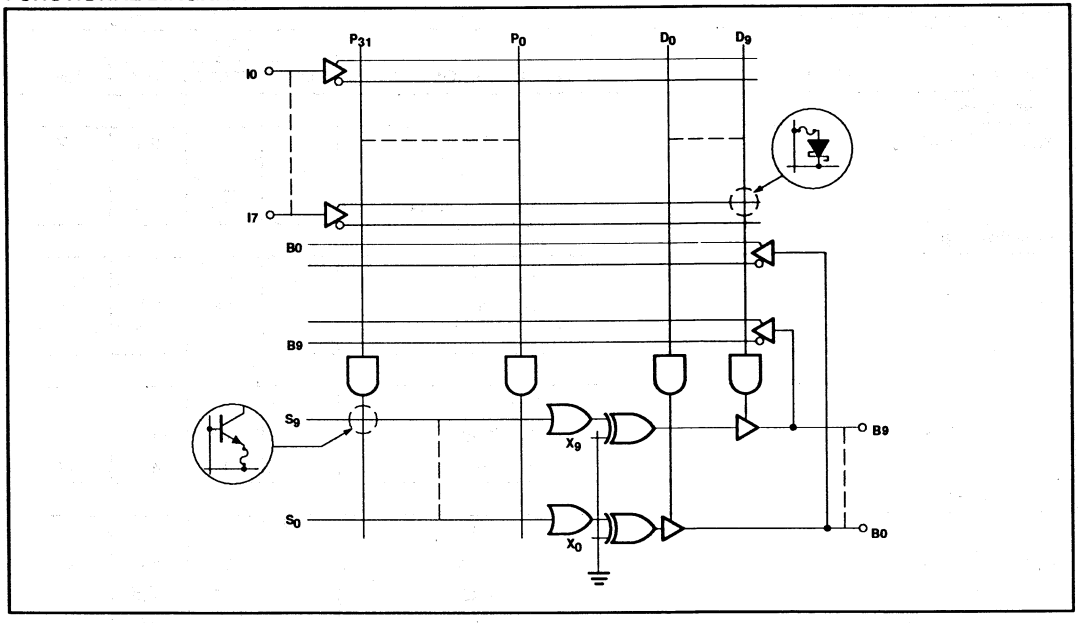


NOTES:
1. All programmed 'AND' gate locations are pulled to logic "1".
2. All programmed 'OR' gate locations are pulled to logic "0".
3. Programmable connection.

Programmable logic array (18 × 42 × 10)

PLUS153–10

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING MIN	RATING MAX	UNIT
V_{CC}	Supply voltage		+7	V_{DC}
V_{In}	Input voltage		+5.5	V_{DC}
V_{OUT}	Output voltage		+5.5	V_{DC}
I_{IN}	Input currents	–30	+30	mA
I_{OUT}	Output currents		+100	mA
T_{amb}	Operating free-air temperature range	0	+75	°C
T_{stg}	Storage temperature range	–65	+150	°C

NOTES:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

Programmable logic array (18 × 42 × 10)

PLUS153–10

DC ELECTRICAL CHARACTERISTICS

$0°C \leq T_{amb} \leq +75°C$, $4.75 \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[1]	MAX	
Input voltage[2]						
V_{IL}	Low	V_{CC} = MIN			0.8	V
V_{IH}	High	V_{CC} = MAX	2.0			V
V_{IC}	Clamp	V_{CC} = MIN, I_{IN} = –12mA		–0.8	–1.2	V
Output voltage[2]						
		V_{CC} = MIN				
V_{OL}	Low[4]	I_{OL} = 15mA		0.4	0.5	V
V_{OH}	High[5]	I_{OH} = –2mA	2.4	2.9		V
Input current[9]						
		V_{CC} = MAX				
I_{IL}	Low	V_{IN} = 0.45V		–20	–100	µA
I_{IH}	High	V_{IN} = V_{CC}		1	40	µA
Output current						
		V_{CC} = MAX				
$I_{O(OFF)}$	Hi-Z state[8]	V_{OUT} = 2.7V		0	80	µA
		V_{OUT} = 0.45V		–15	–140	
I_{OS}	Short circuit[3, 5, 6]	V_{OUT} = 0V	–15	–30	–70	mA
I_{CC}	V_{CC} supply current[7]	V_{CC} = MAX		165	200	mA
Capacitance						
		V_{CC} = 5V				
C_{IN}	Input	V_{IN} = 2.0V		8		pF
C_B	I/O	V_B = 2.0V		15		pF

NOTES:

1. All typical values are at V_{CC} = 5V, T_{amb} = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Test one at a time.
4. Measured with inputs I0 – I2 = 0V, inputs I3 – I5 = 4.5V, inputs I7 = 4.5V and I6 = 10V. For outputs B0 – B4 and for outputs B5 – B9 apply the same conditions except I7 = 0V.
5. Same conditions as Note 4 except I7 = +10V.
6. Duration of short circuit should not exceed 1 second.
7. I_{CC} is measured with inputs I0 – I7 and B0 – B9 = 0V.
8. Leakage values are a combination of input and output leakage.
9. I_{IL} and I_{IH} limits are for dedicated inputs only (I0 – I7).

Programmable logic array (18 × 42 × 10)

PLUS153–10

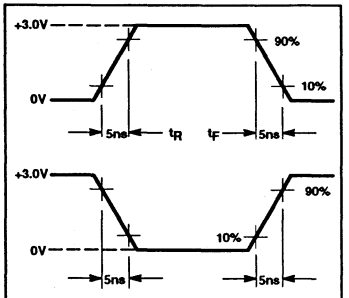
AC ELECTRICAL CHARACTERISTICS

$0°C \le T_{amb} \le +75°C$, $4.75V \le V_{CC} \le 5.25V$, $R_1 = 300\Omega$, $R_2 = 390\Omega$

SYMBOL	PARAMETER	FROM	TO	TEST CONDITION	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
t_{PD}	Propagation Delay[2]	Input +/–	Output +/–	C_L = 30pF		8	10	ns
t_{OE}	Output Enable[1]	Input +/–	Output –	C_L = 30pF		8	10	ns
t_{OD}	Output Disable[1]	Input +/–	Output +	C_L = 5pF		8	10	ns

NOTES:
1. For 3-State output; output enable times are tested with C_L = 30pF to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with C_L = 5pF. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} - 0.5V)$ with S_1 open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with S_1 closed.
2. All propagation delays are measured and specified under worst case conditions.

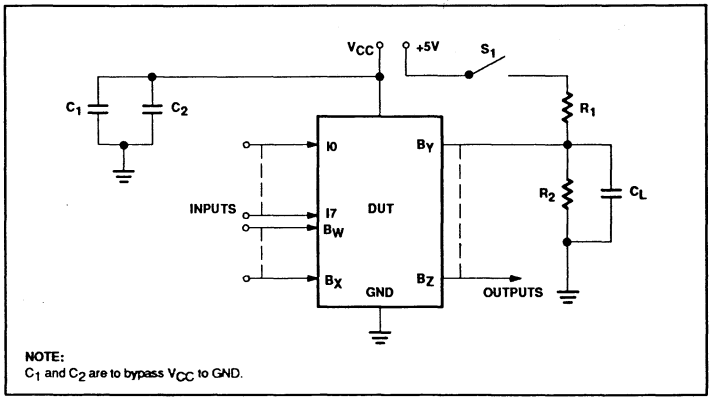
VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

TEST LOAD CIRCUIT

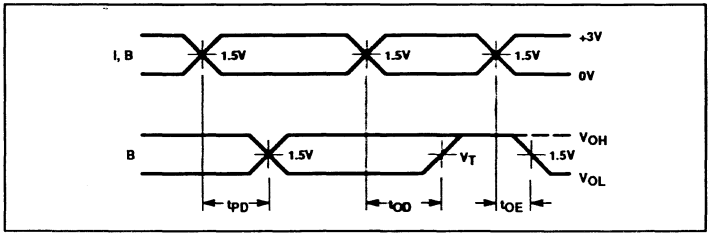


NOTE:
C_1 and C_2 are to bypass V_{CC} to GND.

TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{PD}	Propagation delay between input and output.
t_{OD}	Delay between input change and when output is off (Hi-Z or High).
t_{OE}	Delay between input change and when output reflects specified output level.

TIMING DIAGRAM



Programmable logic array (18 × 42 × 10)

PLUS153–10

LOGIC PROGRAMMING

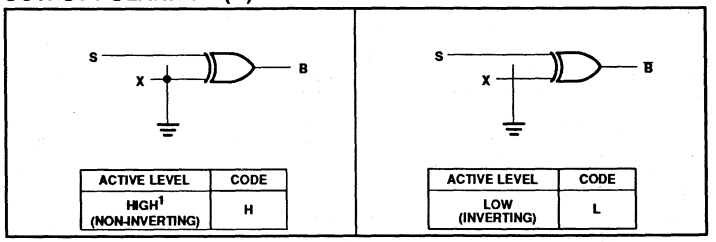
The PLUS153–10 is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Signetics SLICE and SNAP design software packages. ABEL™ and CUPL™ design software packages also support the PLUS153–10 architecture.

All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

PLUS153–10 logic designs can also be generated using the program table entry format, which is detailed on the following page. This program table entry format is supported by SNAP and SLICE only. The SLICE design package is available, free of charge, to qualified users.

To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

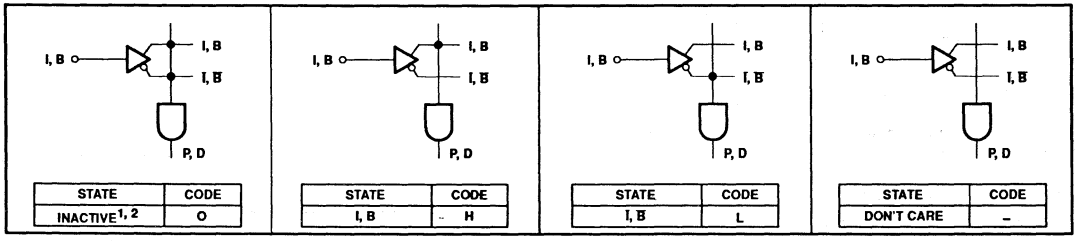
OUTPUT POLARITY – (B)



ACTIVE LEVEL	CODE
HIGH[1] (NON-INVERTING)	H

ACTIVE LEVEL	CODE
LOW (INVERTING)	L

AND ARRAY – (I, B)



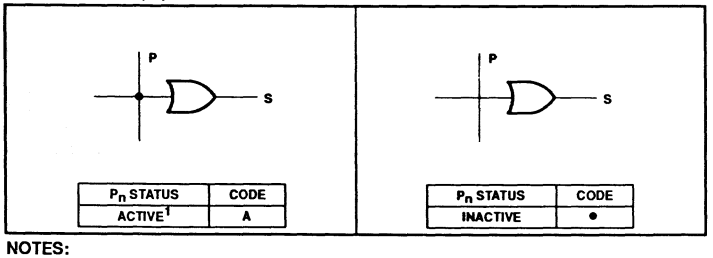
STATE	CODE
INACTIVE[1, 2]	O

STATE	CODE
I, B	H

STATE	CODE
I, B̄	L

STATE	CODE
DON'T CARE	–

OR ARRAY – (B)



P_n STATUS	CODE
ACTIVE[1]	A

P_n STATUS	CODE
INACTIVE	•

VIRGIN STATE

A factory shipped virgin device contains all fusible links intact, such that:

1. All outputs are at "H" polarity.
2. All P_n terms are disabled.
3. All P_n terms are active on all outputs.

NOTES:

1. This is the initial unprogrammed state of all links.
2. Any gate P_n will be unconditionally inhibited if both the true and complement of an input (either I or B) are left intact.

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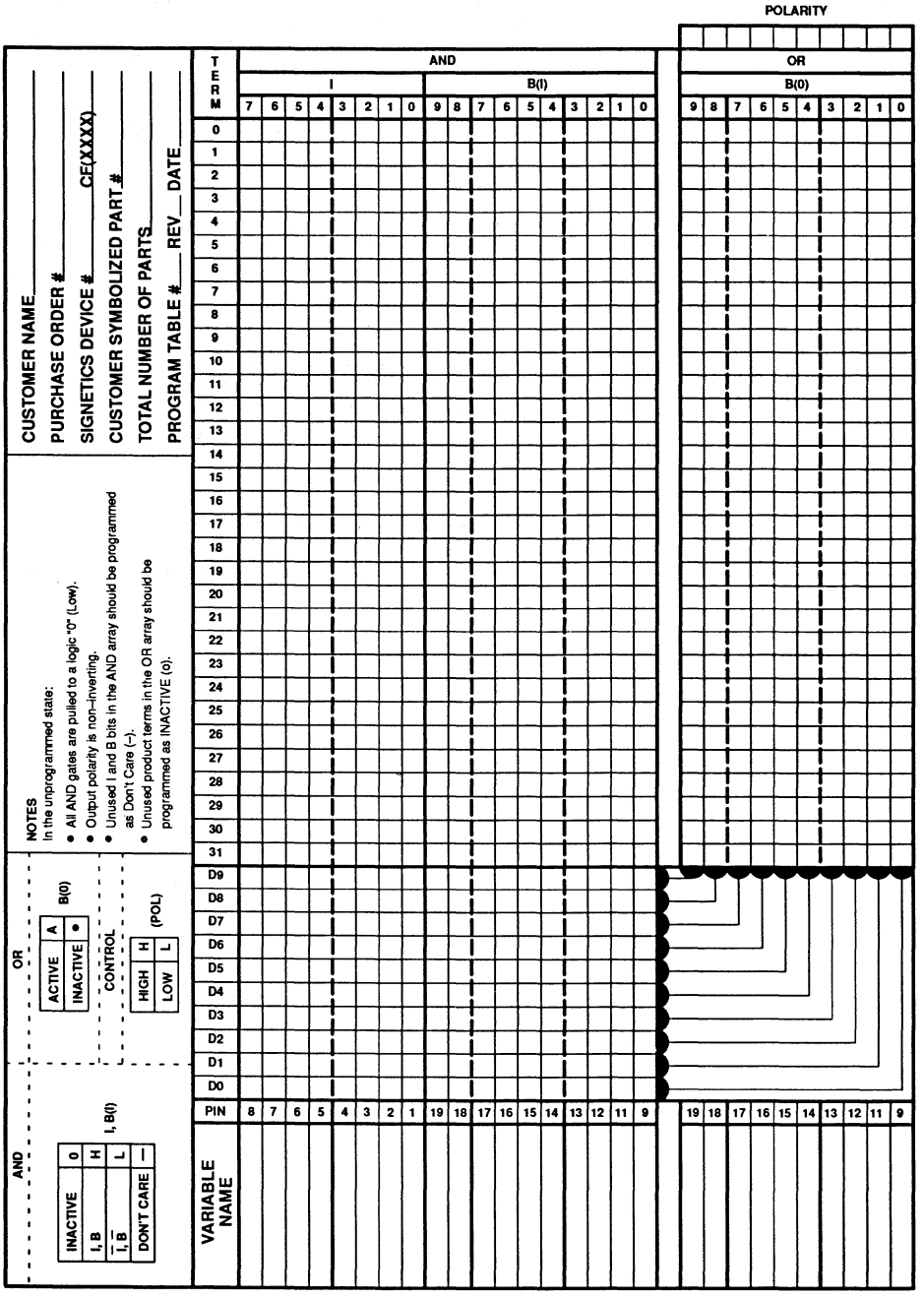
Programmable logic array (18 × 42 × 10)

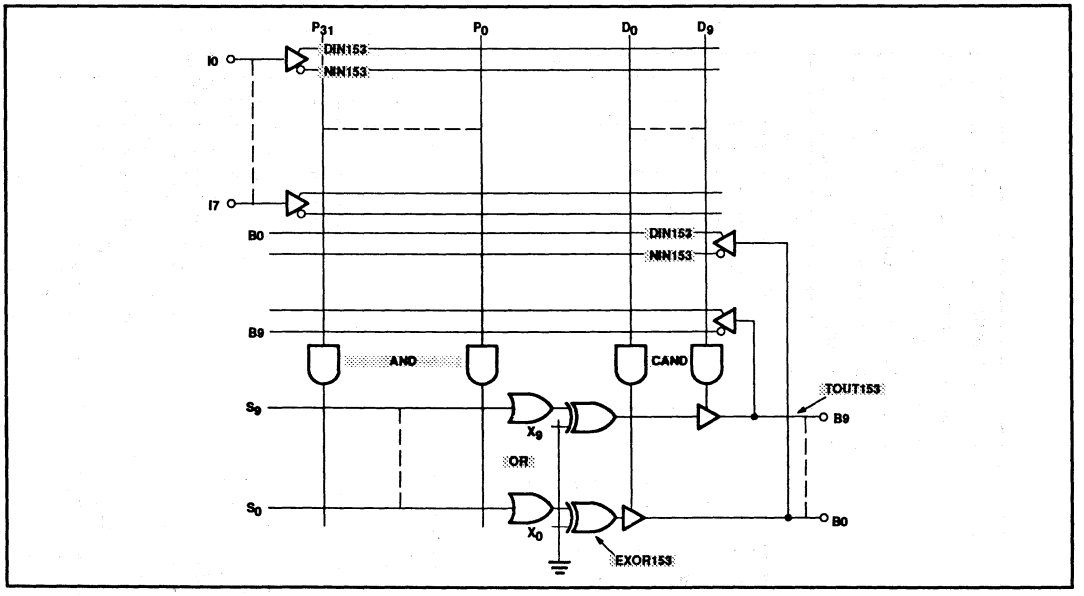
PLUS153–10

PROGRAM TABLE



Programmable logic array (18 × 42 × 10) PLUS153–10

SNAP RESOURCE SUMMARY DESIGNATIONS



Programmable logic array (22 × 42 × 10)

PLS173

DESCRIPTION

The PLS173 is a two-level logic element consisting of 42 AND gates and 10 OR gates with fusible link connections for programming I/O polarity and direction.

All AND gates are linked to 12 inputs (I) and 10 bidirectional I/O lines (B). These yield variable I/O gate configurations via 10 direction control gates (D), ranging from 22 inputs to 10 outputs.

On-chip T/C buffers couple either True (I, B) or Complement ($\overline{I}$, $\overline{B}$) input polarities to all AND gates, whose outputs can be optionally linked to all OR gates. Their output polarity, in turn, is individually programmable through a set of EX-OR gates for implementing AND/OR or AND/NOR logic functions.

The PLS173 is field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

Order codes for this device are listed below.

FEATURES

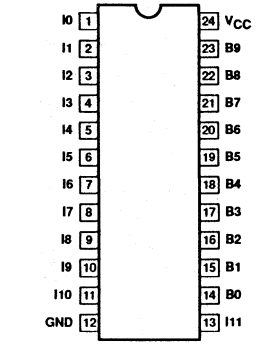
- I/O propagation delay: 30ns (max.)
- 12 inputs
- 42 AND gates
- 10 OR gates
- 10 bidirectional I/O lines
- Active-High or -Low outputs
- 42 product terms:
  - 32 logic terms
  - 10 control terms
- Ni-Cr programmable links
- Input loading: −100μA (max.)
- Power dissipation: 750mW (typ.)
- 3-State outputs
- TTL compatible

APPLICATIONS

- Random logic
- Code converters
- Fault detectors
- Function generators
- Address mapping
- Multiplexing

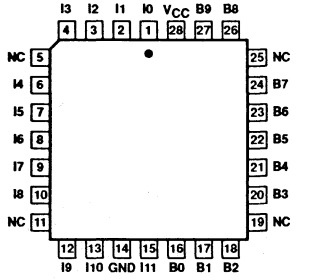
PIN CONFIGURATIONS

N Package



N = Plastic DIP (300mil-wide)

A Package



A = Plastic Leaded Chip Carrier

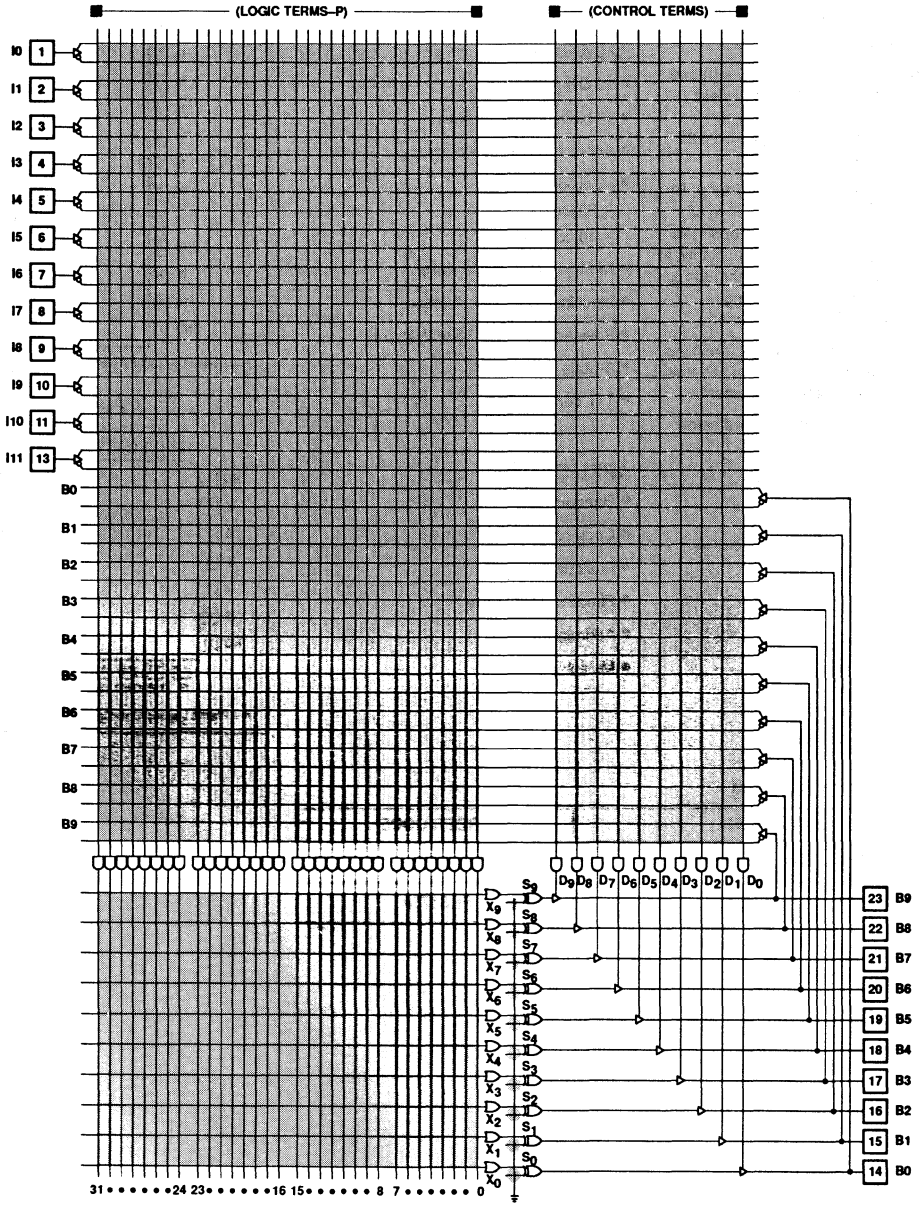
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-Pin Plastic Dual-In-Line 300mil-wide	PLS173N
28-Pin Plastic Leaded Chip Carrier	PLS173A

Programmable logic array (22 × 42 × 10)

PLS173

LOGIC DIAGRAM

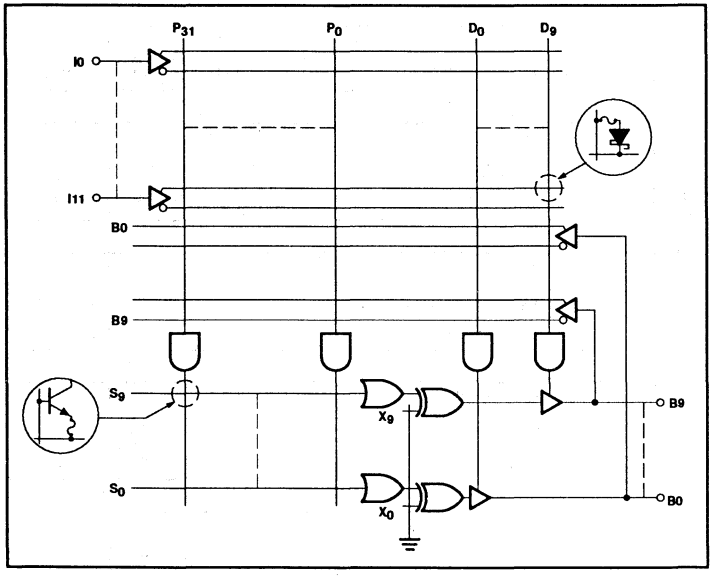


NOTES:
1. All programmed 'AND' gate locations are pulled to logic "1".
2. All programmed 'OR' gate locations are pulled to logic "0".
3. Programmable connection.

Programmable logic array (22 × 42 × 10)

PLS173

FUNCTIONAL DIAGRAM



LOGIC FUNCTION

TYPICAL PRODUCT TERM:

$Pn = A \cdot \overline{B} \cdot C \cdot D \cdot \ldots$

TYPICAL LOGIC FUNCTION:

AT OUTPUT POLARITY = H

$Z = P0 + P1 + P2 \ldots$

AT OUTPUT POLARITY + L

$Z = \overline{P0 + P1 + P2 + \ldots}$

$Z = \overline{P0} \cdot \overline{P1} \cdot \overline{P2} \cdot \ldots$

NOTES:

1. For each of the 10 outputs, either function Z (Active-High) or $\overline{Z}$ (Active-Low) is available, but not both. The desired output polarity is programmed via the EX-OR gates.
2. ZX, A, B, C, etc. are user defined connections to fixed inputs (I), and bidirectional pins (B).

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING Min	RATING Max	UNIT
V_{CC}	Supply voltage		+7	V_{DC}
V_{IN}	Input voltage		+5.5	V_{DC}
V_{OUT}	Output voltage		+5.5	V_{DC}
I_{IN}	Input currents	–30	+30	mA
I_{OUT}	Output currents		+100	mA
T_{amb}	Operating free-air temperature range	0	+75	°C
T_{stg}	Storage temperature range	–65	+150	°C

NOTES:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

The PLS173 is also processed to military requirements for operation over the military temperature range. For specifications and ordering information, consult the Signetics Military Data Handbook.

Programmable logic array (22 × 42 × 10)

PLS173

DC ELECTRICAL CHARACTERISTICS

$0°C \leq T_{amb} \leq +75°C$, $4.75 \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[1]	MAX	
Input voltage[2]						
V_{IL}	Low	V_{CC} = MIN			0.8	V
V_{IH}	High	V_{CC} = MAX	2.0			V
V_{IC}	Clamp[3]	V_{CC} = MIN, I_{IN} = −12mA		−0.8	−1.2	V
Output voltage[2]						
		V_{CC} = MIN				
V_{OL}	Low[4]	I_{OL} = 15mA			0.5	V
V_{OH}	High[5]	I_{OH} = −2mA	2.4			V
Input current[9]						
		V_{CC} = MAX				
I_{IL}	Low	V_{IN} = 0.45V			−100	µA
I_{IH}	High	V_{IN} = V_{CC}			40	µA
Output current						
		V_{CC} = MAX				
$I_{O(OFF)}$	Hi-Z state[8]	V_{OUT} = 5.5V			80	µA
		V_{OUT} = 0.45V			−140	
I_{OS}	Short circuit[3, 5, 6]	V_{OUT} = 0V	−15		−70	mA
I_{CC}	V_{CC} supply current[7]	V_{CC} = MAX		150	170	mA
Capacitance						
		V_{CC} = 5V				
I_{IN}	Input	V_{IN} = 2.0V		8		pF
C_B	I/O	V_B = 2.0V		15		pF

NOTES:

1. All typical values are at V_{CC} = 5V, T_{amb} = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Test one at a time.
4. Measured with inputs V_{IL} applied to I_{11}. Pins 1–5 = 0V. Pins 6–10 = 4.5V, Pin 11 = 0V and Pin 13 = 10V.
5. Same conditions as Note 4 except Pin 11 = +10V.
6. Duration of short circuit should not exceed 1 second.
7. I_{CC} is measured with I_0 and I_1 = 0V, and $I_2 - I_{11}$ and $B_0 - B_9$ = 4.5V. Part in Virgin State.
8. Leakage values are a combination of input and output leakage.
9. I_{IL} and I_{IH} limits are for dedicated inputs only ($I_0 - I_{11}$).

Programmable logic array (22 × 42 × 10)

PLS173

AC ELECTRICAL CHARACTERISTICS

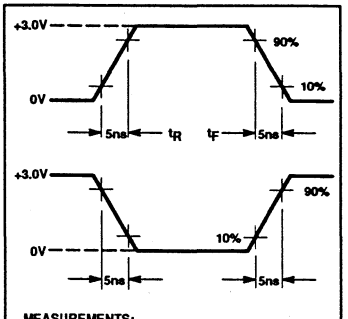
$0°C \le T_{amb} \le +75°C$, $4.75 \le V_{CC} \le 5.25V$, $R_1 = 470\Omega$, $R_2 = 1k\Omega$

SYMBOL	PARAMETER	FROM	TO	TEST CONDITION	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
t_{PD}	Propagation delay[2]	Input ±	Output ±	C_L = 30pF		20	30	ns
t_{OE}	Output enable[1]	Input ±	Output –	C_L = 30pF		20	30	ns
t_{OD}	Output disable[1]	Input ±	Output +	C_L = 5pF		20	30	ns

NOTES:

1. For 3-State output; output enable times are tested with C_L = 30pF to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with C_L = 5pF. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} - 0.5V)$ with S_1 open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with S_1 closed.
2. All propagation delays are measured and specified under worst case conditions.

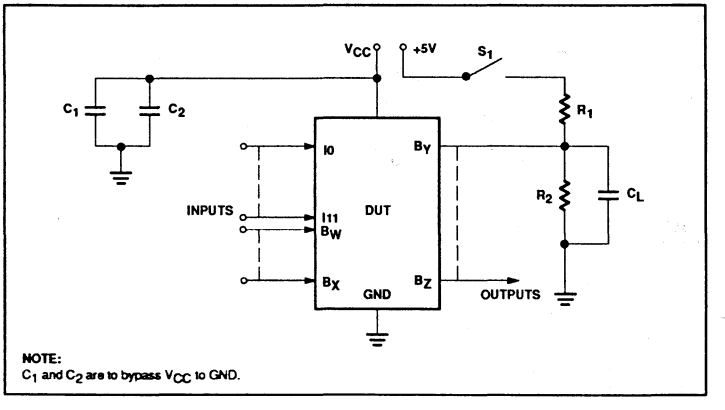
VOLTAGE WAVEFORM



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

TEST LOAD CIRCUIT

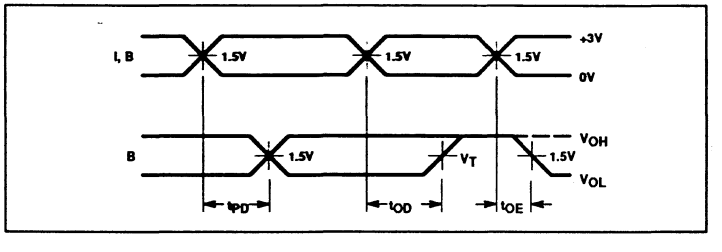


NOTE:
C_1 and C_2 are to bypass V_{CC} to GND.

TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{PD}	Propagation delay between input and output.
t_{OD}	Delay between input change and when output is off (Hi-Z or High).
t_{OE}	Delay between input change and when output reflects specified output level.

TIMING DIAGRAM



Programmable logic array (22 × 42 × 10)

PLS173

LOGIC PROGRAMMING

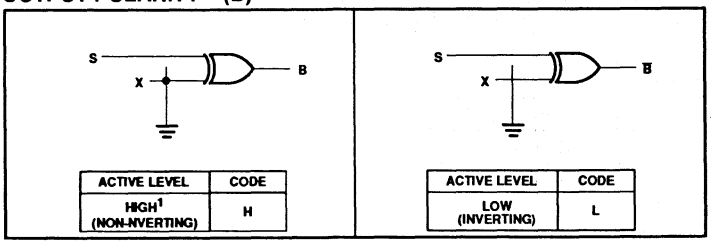
The PLS173 is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Signetics SNAP and SLICE, Data I/O Corporation's ABEL™, and Logical Devices Incorporated's CUPL™ design software packages.

All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

PLS173 logic designs can also be generated using the program table entry format detailed on the following pages. This program table entry format is supported by the Signetics SLICE and SNAP PLD design software (PTP module) packages. SLICE is available free of charge to qualified users.

To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

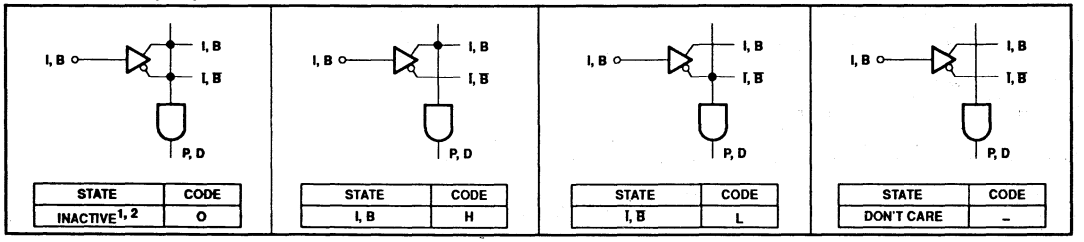
OUTPUT POLARITY – (B)



ACTIVE LEVEL	CODE
HIGH[1] (NON-INVERTING)	H

ACTIVE LEVEL	CODE
LOW (INVERTING)	L

AND ARRAY – (I, B)



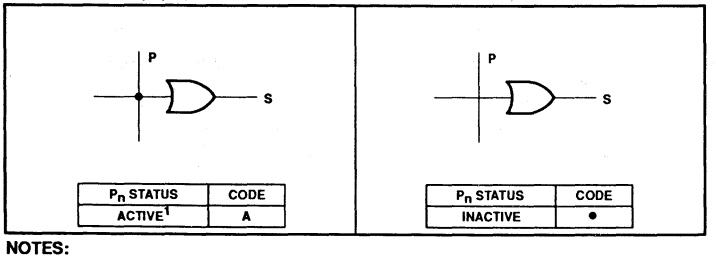
STATE	CODE
INACTIVE[1,2]	O

STATE	CODE
I, B	H

STATE	CODE
I, $\overline{B}$	L

STATE	CODE
DON'T CARE	–

OR ARRAY – (B)



P_n STATUS	CODE
ACTIVE[1]	A

P_n STATUS	CODE
INACTIVE	•

NOTES:

1. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates P_n, D_n.
2. Any gate P_n, D_n will be unconditionally inhibited if both the True and Complement of any input (I, B) are left intact.

VIRGIN STATE

A factory shipped virgin device contains all fusible links intact, such that:

1. All outputs are at "H" polarity.
2. All P_n terms are disabled.
3. All P_n terms are active on all outputs.

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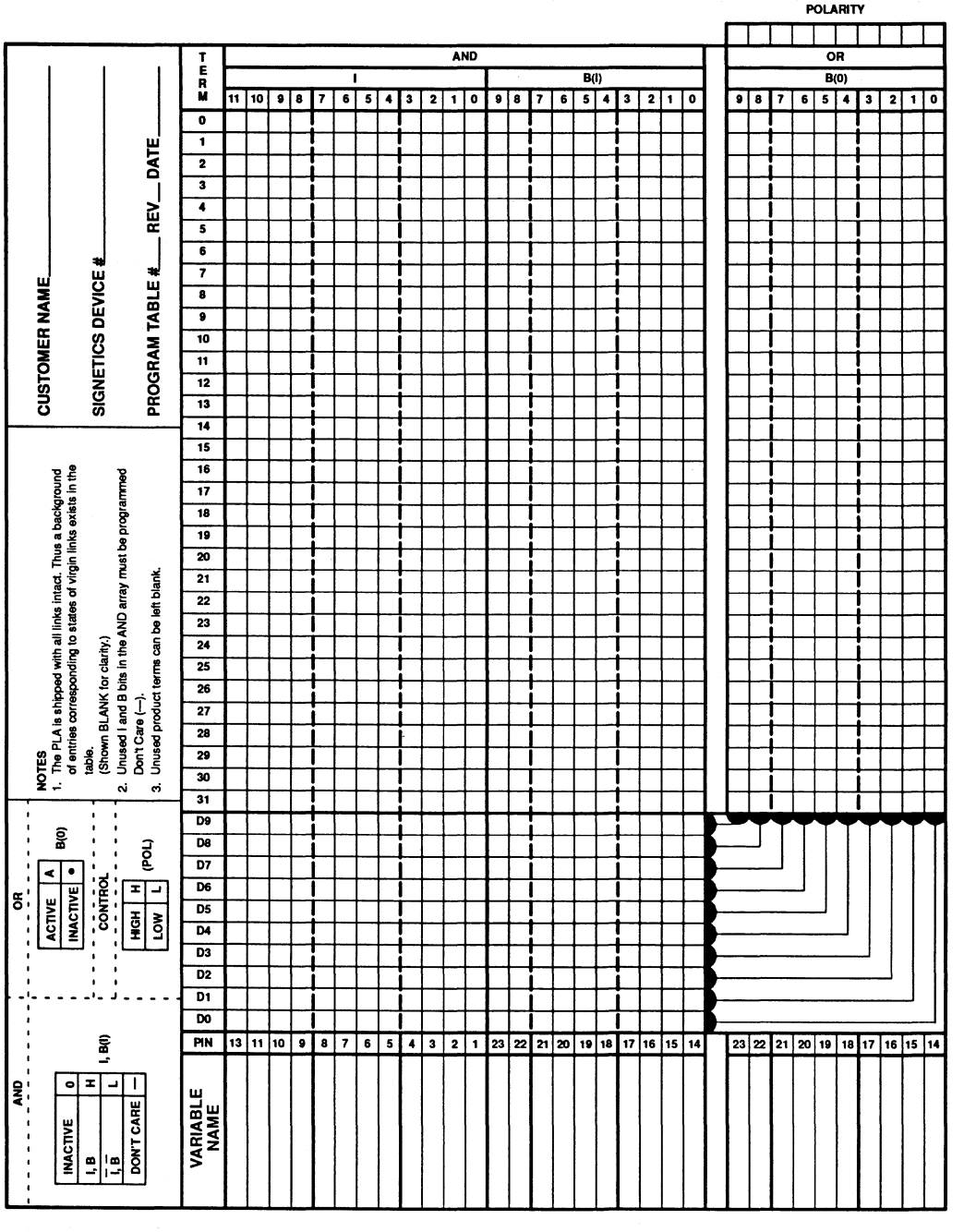
Programmable logic array (22 × 42 × 10)

PLS173

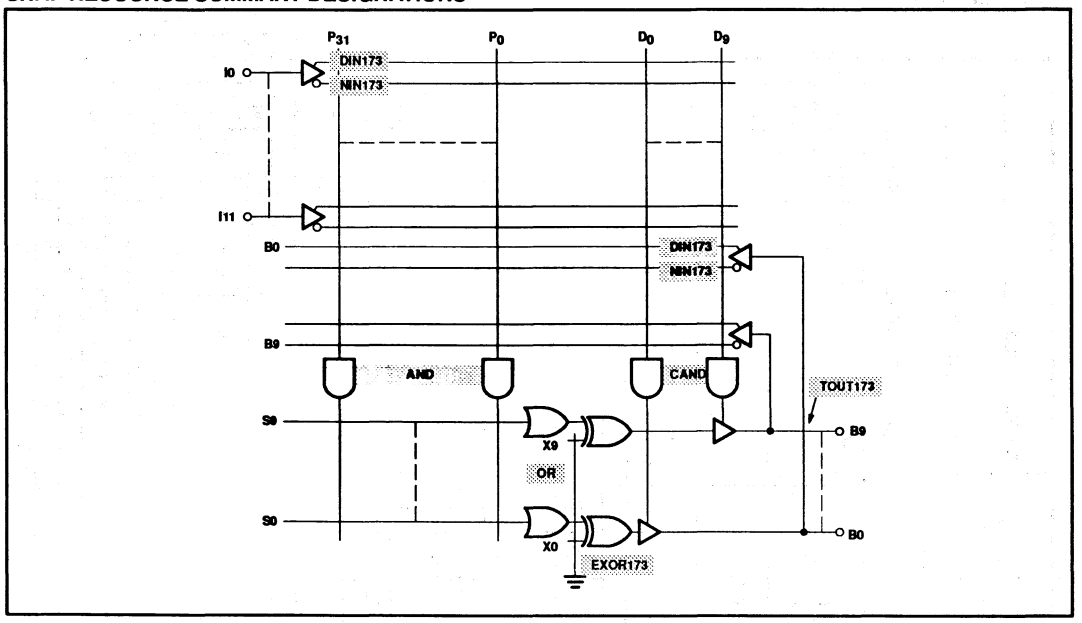
PROGRAM TABLE



Programmable logic array (22 × 42 × 10)

PLS173

SNAP RESOURCE SUMMARY DESIGNATIONS



Programmable logic arrays (22 × 42 × 10)

PLUS173B/D

DESCRIPTION

The PLUS173 PLDs are high speed, combinatorial Programmable Logic Arrays. The Signetics state-of-the-art Oxide Isolated Bipolar fabrication process is employed to produce propagation delays as short as 12ns.

The 24-pin PLUS173 devices have a programmable AND array and a programmable OR array. Unlike PAL ® devices, 100% product term sharing is supported. Any of the 32 logic product terms can be connected to any or all of the 10 output OR gates. Most PAL ICs are limited to 7 AND terms per OR function; the PLUS173 devices can support up to 32 input wide OR functions.

The polarity of each output is user-programmable as either Active-High or Active-Low, thus allowing AND-OR or AND-NOR logic implementation. This feature adds an element of design flexibility, particularly when implementing complex decoding functions.

The PLUS173 devices are user-programmable using one of several commercially available, industry standard PLD programmers.

FEATURES

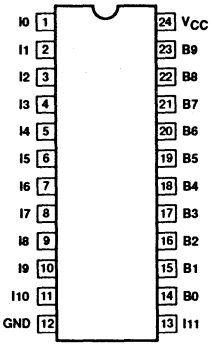
- I/O propagation delays (worst case)
  - PLUS173B – 15ns max.
  - PLUS173D – 12ns max.
- Functional superset of 20L10 and most other 24-pin combinatorial PAL devices
- Two programmable arrays
  - Supports 32 input wide OR functions
- 12 inputs
- 10 bi-directional I/O
- 42 AND gates
  - 32 logic product terms
  - 10 direction control terms
- Programmable output polarity
  - Active-High or Active-Low
- Security fuse
- 3-State outputs
- Power dissipation: 750mW (typ.)
- TTL Compatible

APPLICATIONS

- Random logic
- Code converters
- Fault detectors
- Function generators
- Address mapping
- Multiplexing

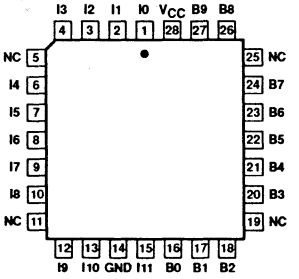
PIN CONFIGURATIONS

N Package



N = Plastic Dual In-Line (300mil-wide)

A Package



A = Plastic Leaded Chip Carrier

ORDERING INFORMATION

DESCRIPTION	t_{PD} (MAX)	ORDER CODE
24-Pin Plastic Dual In-Line 300mil-wide	15ns	PLUS173BN
24-Pin Plastic Dual In-Line 300mil-wide	12ns	PLUS173DN
28-Pin Plastic Leaded Chip Carrier	15ns	PLUS173BA
28-Pin Plastic Leaded Chip Carrier	12ns	PLUS173DA

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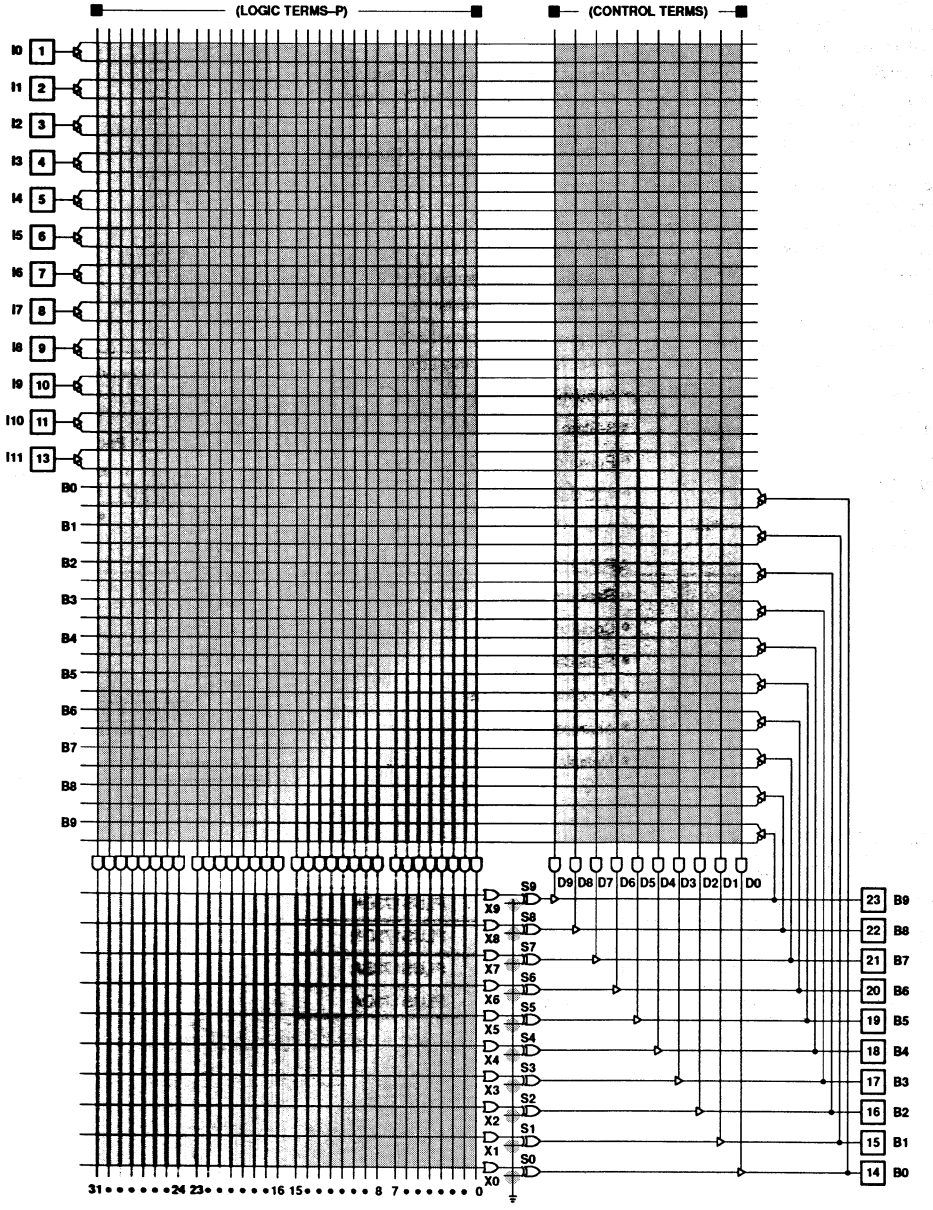
Programmable logic arrays (22 × 42 × 10)

PLUS173B/D

LOGIC DIAGRAM

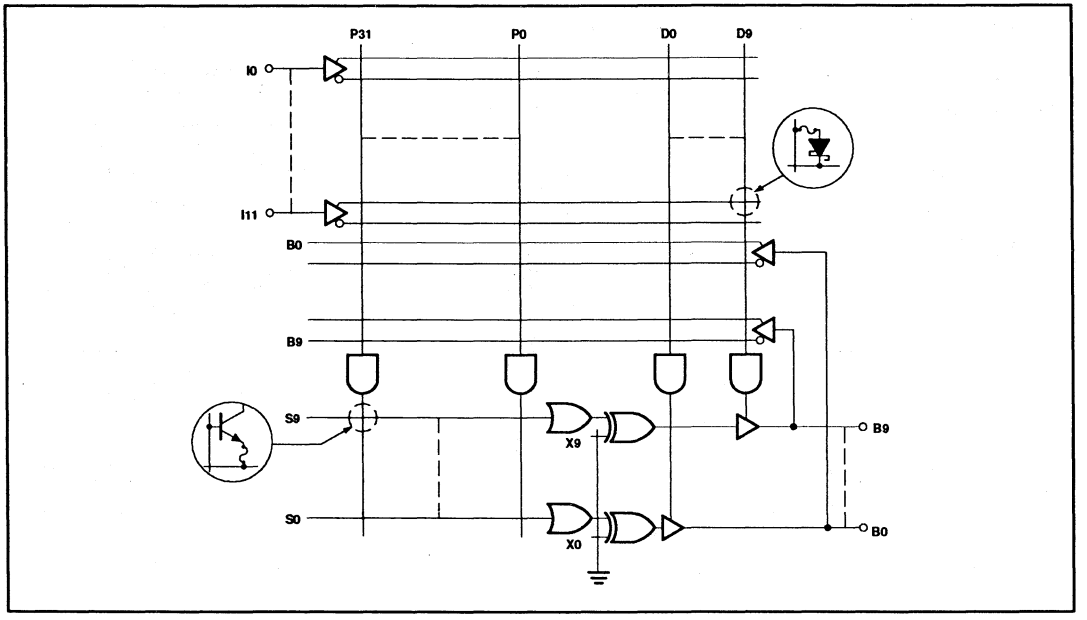


NOTES:
1. All programmed 'AND' gate locations are pulled to logic "1".
2. All programmed 'OR' gate locations are pulled to logic "0".
3. ● Programmable connection.

Programmable logic arrays (22 × 42 × 10)

PLUS173B/D

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING MIN	RATING MAX	UNIT
V_{CC}	Supply voltage		+7	V_{DC}
V_{IN}	Input voltage		+5.5	V_{DC}
V_{OUT}	Output voltage		+5.5	V_{DC}
I_{IN}	Input currents	–30	+30	mA
I_{OUT}	Output currents		+100	mA
T_{amb}	Operating free-air temperature range	0	+75	°C
T_{stg}	Storage temperature range	–65	+150	°C

NOTES:
1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

DC ELECTRICAL CHARACTERISTICS

$0°C \leq T_{amb} \leq +75°C$, $4.75 \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[1]	MAX	
Input voltage[2]						
V_{IL}	Low	V_{CC} = MIN			0.8	V
V_{IH}	High	V_{CC} = MAX	2.0			V
V_{IC}	Clamp	V_{CC} = MIN, I_{IN} = −12mA		−0.8	−1.2	V
Output voltage[2]						
		V_{CC} = MIN				
V_{OL}	Low[4]	I_{OL} = 15mA			0.5	V
V_{OH}	High[5]	I_{OH} = −2mA	2.4			V
Input current[9]						
		V_{CC} = MAX				
I_{IL}	Low	V_{IN} = 0.45V			−100	μA
I_{IH}	High	V_{IN} = V_{CC}			40	μA
Output current						
		V_{CC} = MAX				
$I_{O(OFF)}$	Hi-Z state[8]	V_{OUT} = 2.7V			80	μA
		V_{OUT} = 0.45V			−140	
I_{OS}	Short circuit[3, 5, 6]	V_{OUT} = 0V	−15		−70	mA
I_{CC}	V_{CC} supply current[7]	V_{CC} = MAX		150	200	mA
Capacitance						
		V_{CC} = 5V				
I_{IN}	Input	V_{IN} = 2.0V		8		pF
C_B	I/O	V_B = 2.0V		15		pF

NOTES:

1. All typical values are at V_{CC} = 5V, T_{amb} = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Test one at a time.
4. Measured with inputs I0 – I4 = 0V, inputs I5 – I9 = 4.5V, I11 = 4.5V and I19 = 10V. For outputs B0 – B4 and for outputs B5 – B9 apply the same conditions except I11 = 0V.
5. Same conditions as Note 4 except input I11 = +10V.
6. Duration of short circuit should not exceed 1 second.
7. I_{CC} is measured with inputs I0 – I11 and B0 – B9 = 0V. Part in Virgin State.
8. Leakage values are a combination of input and output leakage.
9. I_{IL} and I_{IH} limits are for dedicated inputs only (I0 – I11).

AC ELECTRICAL CHARACTERISTICS

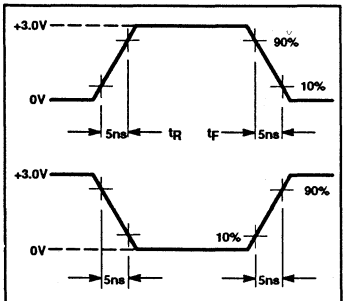
$0°C \le T_{amb} \le +75°C$, $4.75 \le V_{CC} \le 5.25V$, $R_1 = 300\Omega$, $R_2 = 390\Omega$

SYMBOL	PARAMETER	FROM	TO	TEST CONDITION	LIMITS						UNIT
					PLUS173B			PLUS173D			
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{PD}	Propagation Delay[2]	Input +/–	Output +/–	C_L = 30pF		11	15		10	12	ns
t_{OE}	Output Enable[1]	Input +/–	Output –	C_L = 30pF		11	15		10	12	ns
t_{OD}	Output Disable[1]	Input +/–	Output +	C_L = 5pF		11	15		10	12	ns

NOTES:

1. For 3-State outputs; output enable times are tested with C_L = 30pF to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with C_L = 5pF. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} - 0.5V)$ with S_1 open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with S_1 closed.
2. All propagation delays are measured and specified under worst case conditions.

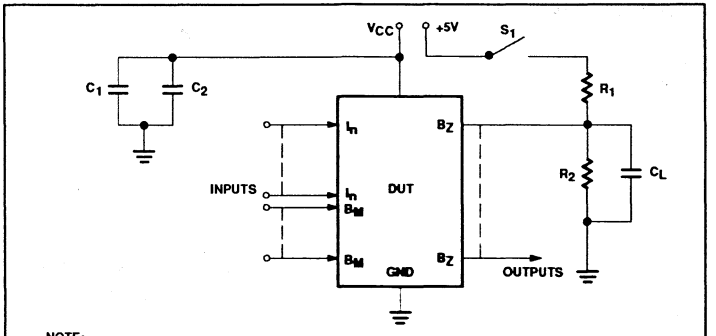
VOLTAGE WAVEFORM



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

TEST LOAD CIRCUIT



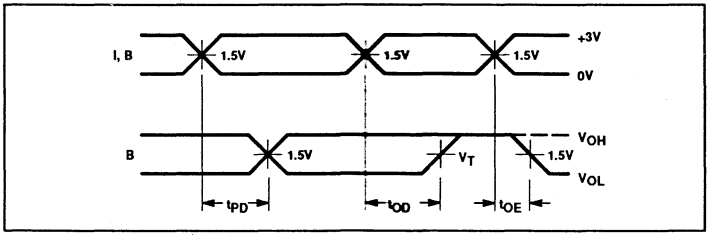
NOTE:
C_1 and C_2 are to bypass V_{CC} to GND.

Test Load Circuit

TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{PD}	Propagation delay between input and output.
t_{OD}	Delay between input change and when output is off (Hi-Z or High).
t_{OE}	Delay between input change and when output reflects specified output level.

TIMING DIAGRAM



Programmable logic arrays (22 × 42 × 10)

PLUS173B/D

LOGIC PROGRAMMING

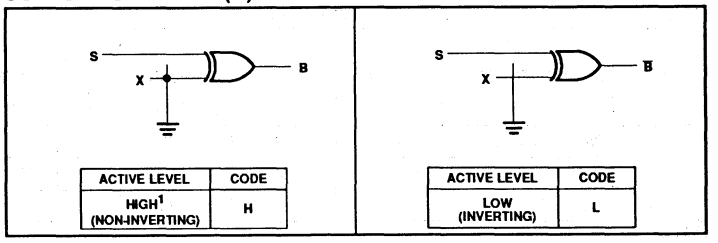
The PLUS173 series is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Signetics SLICE and SNAP design software packages. ABEL™ and CUPL™ design software packages also support the PLUS173 architecture.

All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

PLUS173 logic designs can also be generated using the program table entry format, which is detailed on the following page. This program table entry format is supported by SNAP and SLICE only. The SLICE design package is available, free of charge, to qualified users.

To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

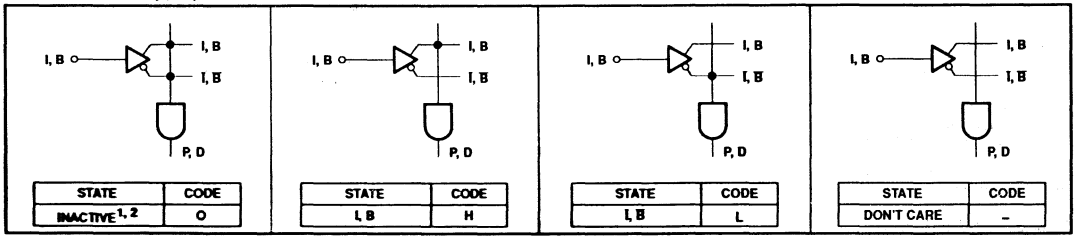
OUTPUT POLARITY – (B)



ACTIVE LEVEL	CODE
HIGH[1] (NON-INVERTING)	H

ACTIVE LEVEL	CODE
LOW (INVERTING)	L

AND ARRAY – (I, B)



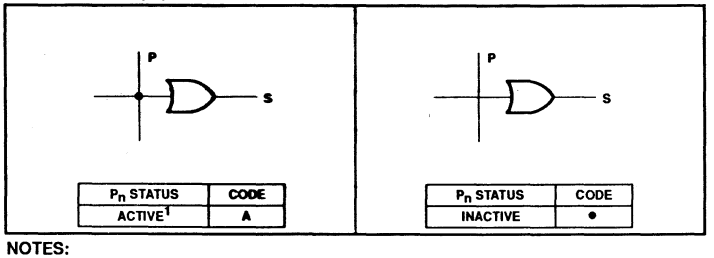
STATE	CODE
INACTIVE[1, 2]	O

STATE	CODE
I, B	H

STATE	CODE
I, B	L

STATE	CODE
DON'T CARE	–

OR ARRAY – (B)



P_n STATUS	CODE
ACTIVE[1]	A

P_n STATUS	CODE
INACTIVE	•

VIRGIN STATE

A factory shipped virgin device contains all fusible links intact, such that:

1. All outputs are at "H" polarity.
2. All P_n terms are disabled.
3. All P_n terms are active on all outputs.

NOTES:

1. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates P_n, D_n.
2. Any gate P_n, D_n will be unconditionally inhibited if both the true and complement of any input (I, B) are left intact.

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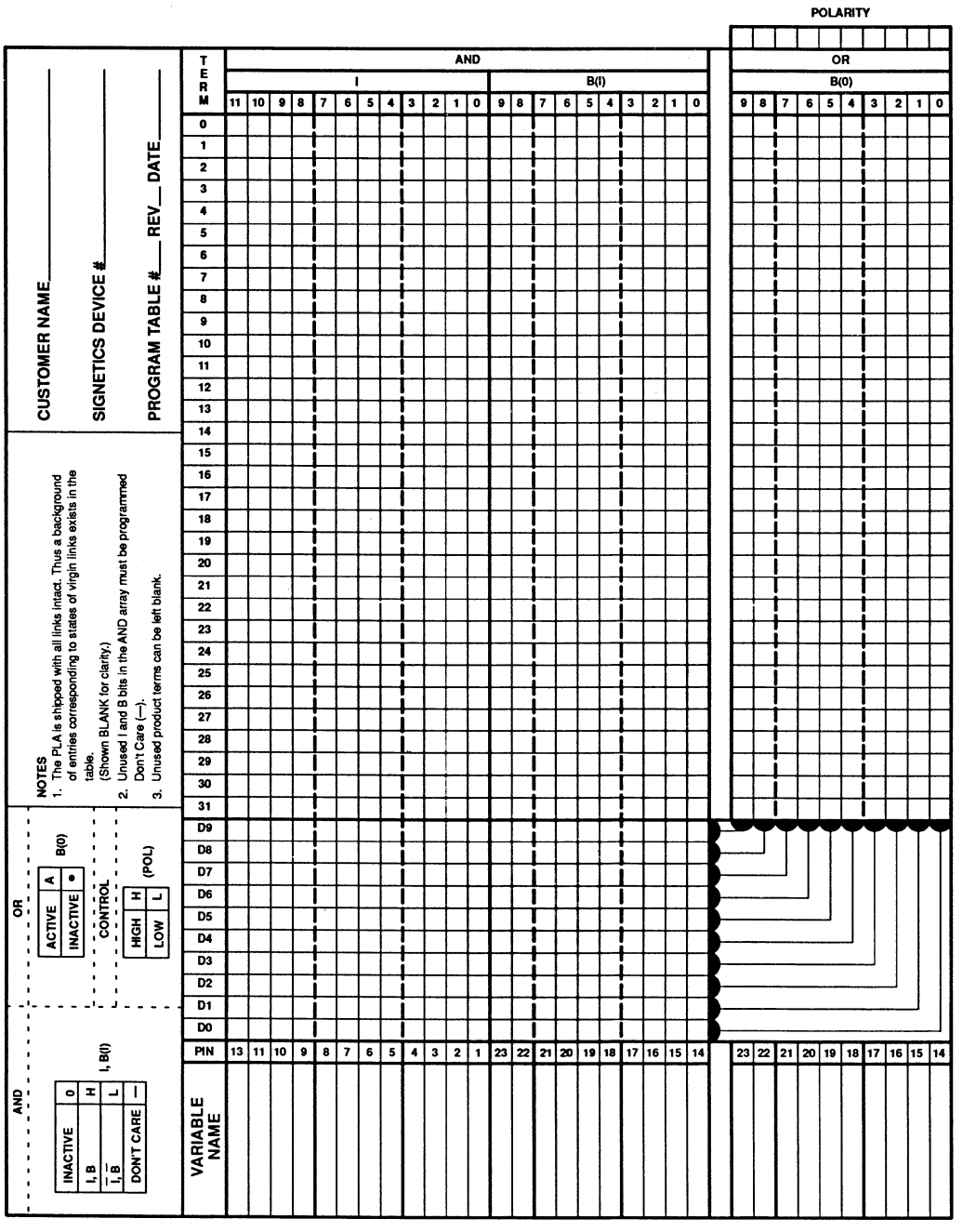
Programmable logic arrays (22 × 42 × 10)

PLUS173B/D

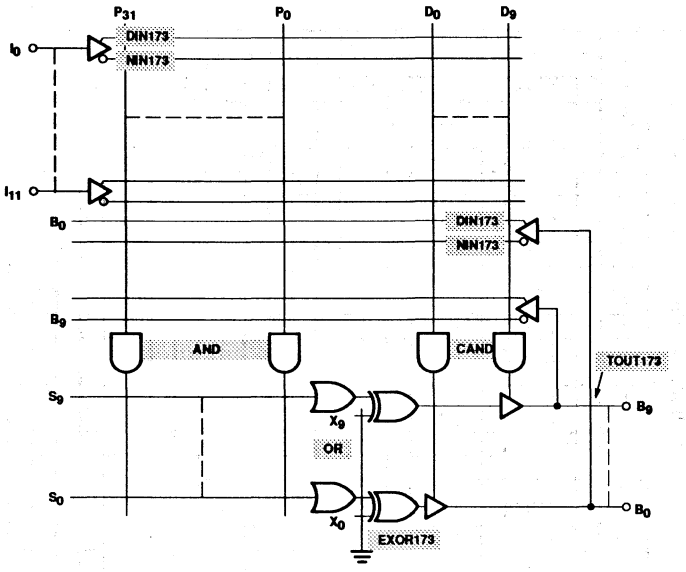
PROGRAM TABLE



Programmable logic arrays (22 × 42 × 10)

PLUS173B/D

SNAP RESOURCE SUMMARY DESIGNATIONS



Programmable logic array (22 × 42 × 10)

PLUS173–10

DESCRIPTION

The PLUS173–10 PLD is a high speed, combinatorial Programmable Logic Array. The Signetics state-of-the-art Oxide Isolated Bipolar fabrication process is employed to produce maximum propagation delays of 10ns or less.

The 24-pin PLUS173–10 device has a programmable AND array and a programmable OR array. Unlike PAL® devices, 100% product term sharing is supported. Any of the 32 logic product terms can be connected to any or all of the 10 output OR gates. Most PAL ICs are limited to 7 AND terms per OR function; the PLUS173–10 device can support up to 32 input wide OR functions.

The polarity of each output is user-programmable as either Active-High or Active-Low, thus allowing AND-OR or AND-NOR logic implementation. This feature adds an element of design flexibility, particularly when implementing complex decoding functions.

The PLUS173–10 device is user-programmable using one of several commercially available, industry standard PLD programmers.

FEATURES

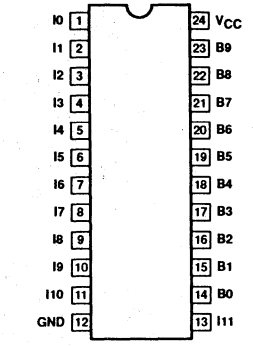
- I/O propagation delays
  - 10ns (worst case)
- Functional superset of 20L10 and most other 24-pin combinatorial PAL devices
- Two programmable arrays
  - Supports 32 input wide OR functions
- 12 inputs
- 10 bi-directional I/O
- 42 AND gates
  - 32 logic product terms
  - 10 direction control terms
- Programmable output polarity
  - Active-High or Active-Low
- Security fuse
- 3-State outputs
- Power dissipation: 850mW (typ.)
- TTL Compatible

APPLICATIONS

- Random logic
- Code converters
- Fault detectors
- Function generators
- Address mapping
- Multiplexing

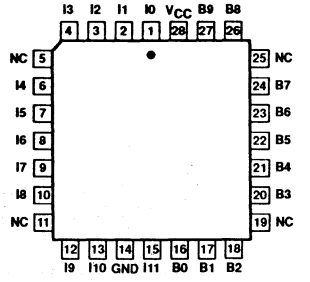
PIN CONFIGURATIONS

N Package



N = Plastic Dual In-Line (300mil-wide)

A Package



A = Plastic Leaded Chip Carrier

ORDERING INFORMATION

DESCRIPTION	t_{PD} (MAX)	ORDER CODE
24-Pin Plastic Dual In-Line 300mil-wide	10ns	PLUS173–10N
28-Pin Plastic Leaded Chip Carrier	10ns	PLUS173–10A

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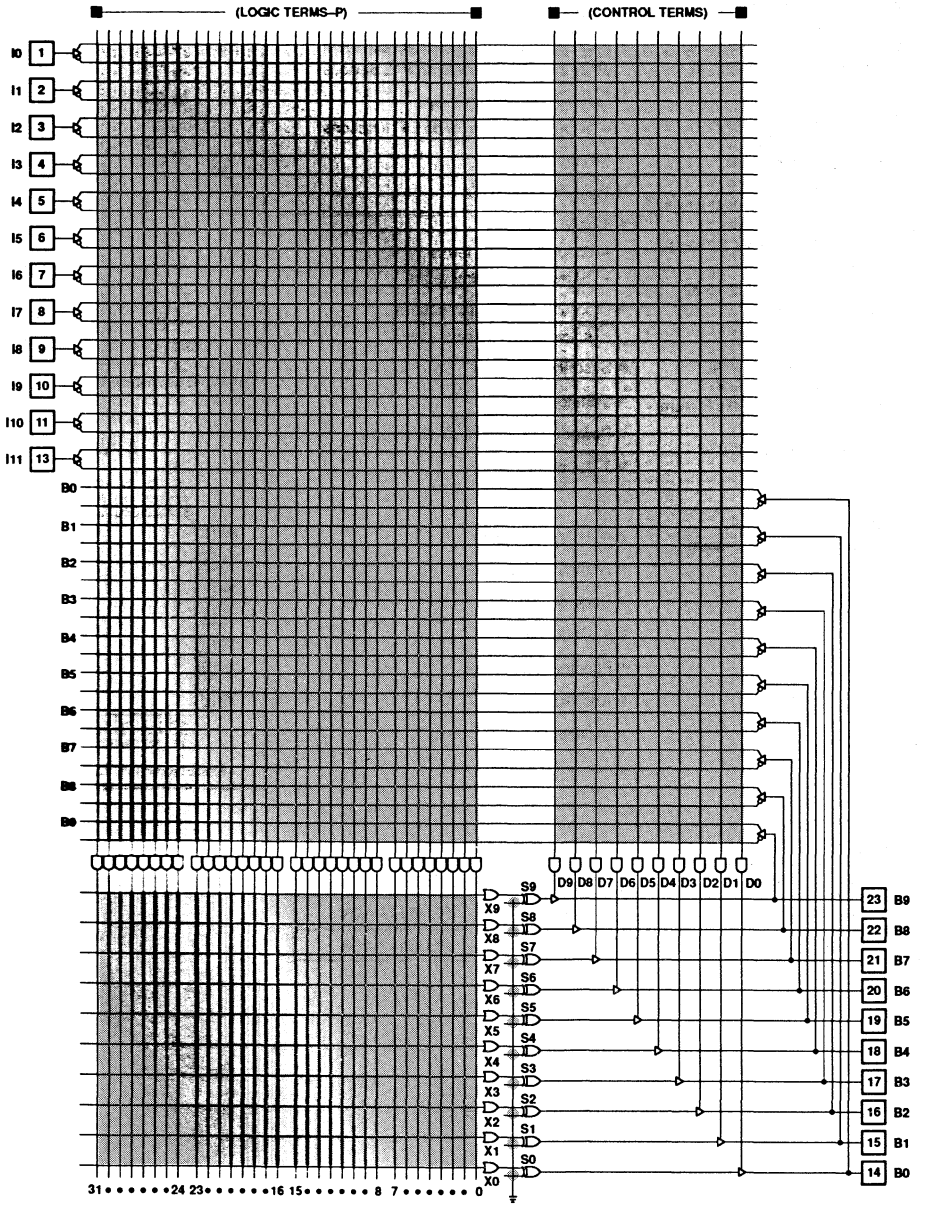
Programmable logic array (22 × 42 × 10)

PLUS173–10

LOGIC DIAGRAM

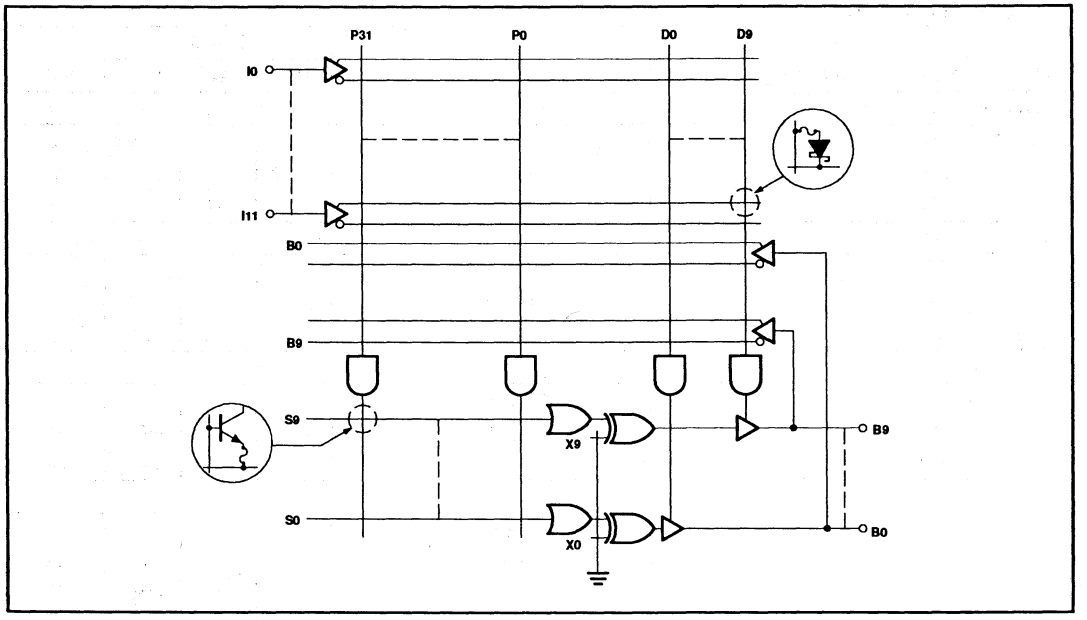


NOTES:
1. All programmed 'AND' gate locations are pulled to logic "1".
2. All programmed 'OR' gate locations are pulled to logic "0".
3. Programmable connection.

Programmable logic array (22 × 42 × 10)

PLUS173–10

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING		UNIT
		Min	Max	
V_{CC}	Supply voltage		+7	V_{DC}
V_{IN}	Input voltage		+5.5	V_{DC}
V_{OUT}	Output voltage		+5.5	V_{DC}
I_{IN}	Input currents	–30	+30	mA
I_{OUT}	Output currents		+100.0	mA
T_{amb}	Operating free-air temperature range	0	+75	°C
T_{stg}	Storage temperature range	–65	+150	°C

NOTES:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

DC ELECTRICAL CHARACTERISTICS

$0°C \leq T_{amb} \leq +75°C$, $4.75 \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[1]	MAX	
Input voltage[2]						
V_{IL}	Low	V_{CC} = MIN			0.8	V
V_{IH}	High	V_{CC} = MAX	2.0			V
V_{IC}	Clamp	V_{CC} = MIN, I_{IN} = –12mA		–0.8	–1.2	V
Output voltage[2]						
		V_{CC} = MIN				
V_{OL}	Low[4]	I_{OL} = 15mA		0.4	0.5	V
V_{OH}	High[5]	I_{OH} = –2mA	2.4	2.9		V
Input current[9]						
		V_{CC} = MAX				
I_{IL}	Low	V_{IN} = 0.45V		–20	–100	µA
I_{IH}	High	V_{IN} = V_{CC}		1	40	µA
Output current						
		V_{CC} = MAX				
$I_{O(OFF)}$	Hi-Z state[8]	V_{OUT} = 2.7V		0	80	µA
		V_{OUT} = 0.45V		–15	–140	
I_{OS}	Short circuit[3, 5, 6]	V_{OUT} = 0V	–15	–30	–70	mA
I_{CC}	V_{CC} supply current[7]	V_{CC} = MAX		170	210	mA
Capacitance						
		V_{CC} = 5V				
I_{IN}	Input	V_{IN} = 2.0V		8		pF
C_B	I/O	V_B = 2.0V		15		pF

NOTES:

1. All typical values are at V_{CC} = 5V, T_{amb} = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Test one at a time.
4. Measured with inputs I0 – I4 = 0V, inputs I5 – I9 = 4.5V, I11 = 4.5V and I10 = 10V. For outputs B0 – B4 and for outputs B5 – B9 apply the same conditions except I11 = 0V.
5. Same conditions as Note 4 except input I11 = +10V.
6. Duration of short circuit should not exceed 1 second.
7. I_{CC} is measured with inputs I0 – I11 and B0 – B9 = 0V. Part in Virgin State.
8. Leakage values are a combination of input and output leakage.
9. I_{IL} and I_{IH} limits are for dedicated inputs only (I0 – I11).

Programmable logic array (22 × 42 × 10)

PLUS173–10

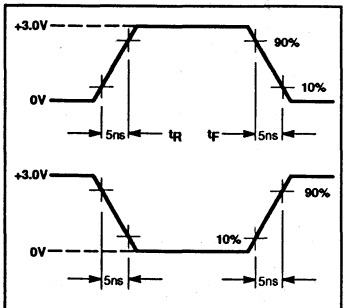
AC ELECTRICAL CHARACTERISTICS

$0°C \le T_{amb} \le +75°C$, $4.75 \le V_{CC} \le 5.25V$, $R_1 = 300\Omega$, $R_2 = 390\Omega$

SYMBOL	PARAMETER	FROM	TO	TEST CONDITION	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
t_{PD}	Propagation Delay[2]	Input +/–	Output +/–	C_L = 30pF		8	10	ns
t_{OE}	Output Enable[1]	Input +/–	Output –	C_L = 30pF		8	10	ns
t_{OD}	Output Disable[1]	Input +/–	Output +	C_L = 5pF		8	10	ns

NOTES:
1. For 3-State outputs; output enable times are tested with C_L = 30pF to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with C_L = 5pF. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} - 0.5V)$ with S_1 open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with S_1 closed.
2. All propagation delays are measured and specified under worst case conditions.

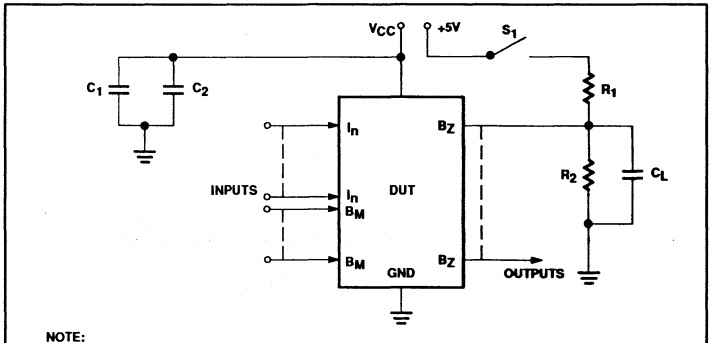
VOLTAGE WAVEFORM



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

TEST LOAD CIRCUIT



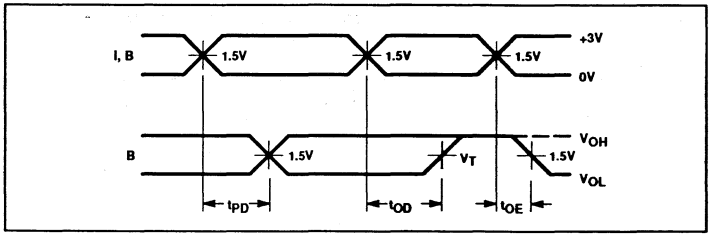
NOTE:
C_1 and C_2 are to bypass V_{CC} to GND.

Test Load Circuit

TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{PD}	Propagation delay between input and output.
t_{OD}	Delay between input change and when output is off (Hi-Z or High).
t_{OE}	Delay between input change and when output reflects specified output level.

TIMING DIAGRAM



Programmable logic array (22 x 42 x 10)

PLUS173–10

LOGIC PROGRAMMING

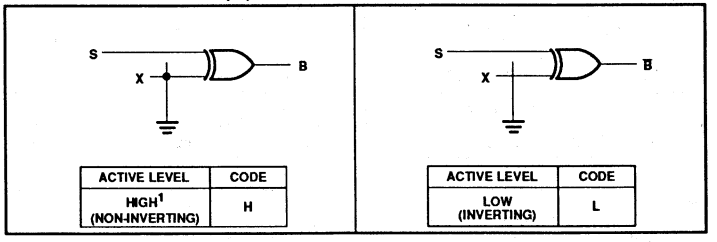
The PLUS173–10 is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Signetics SLICE and SNAP design software packages. ABEL™ and CUPL™ design software packages also support the PLUS173–10 architecture.

All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

PLUS173–10 logic designs can also be generated using the program table entry format, which is detailed on the following page. This program table entry format is supported by SNAP and SLICE only. The SLICE design package is available, free of charge, to qualified users.

To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

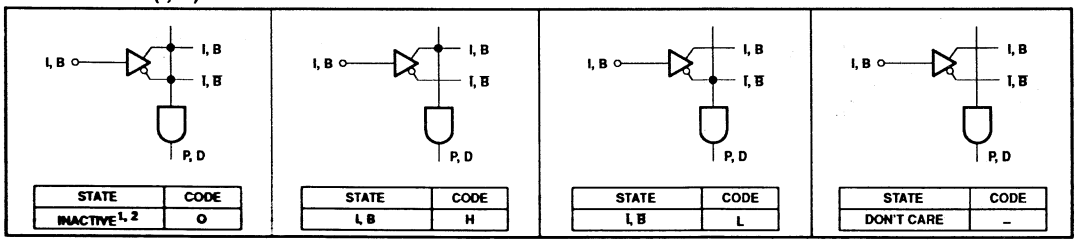
OUTPUT POLARITY – (B)



ACTIVE LEVEL	CODE
HIGH[1] (NON-INVERTING)	H

ACTIVE LEVEL	CODE
LOW (INVERTING)	L

AND ARRAY – (I, B)



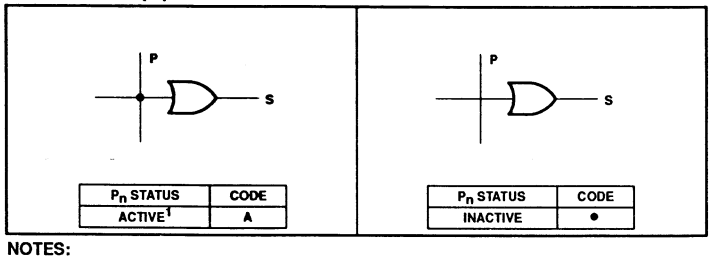
STATE	CODE
INACTIVE[1, 2]	O

STATE	CODE
I, B	H

STATE	CODE
I, B	L

STATE	CODE
DON'T CARE	–

OR ARRAY – (B)



P_n STATUS	CODE
ACTIVE[1]	A

P_n STATUS	CODE
INACTIVE	•

VIRGIN STATE

A factory shipped virgin device contains all fusible links intact, such that:

1. All outputs are at "H" polarity.
2. All P_n terms are disabled.
3. All P_n terms are active on all outputs.

NOTES:

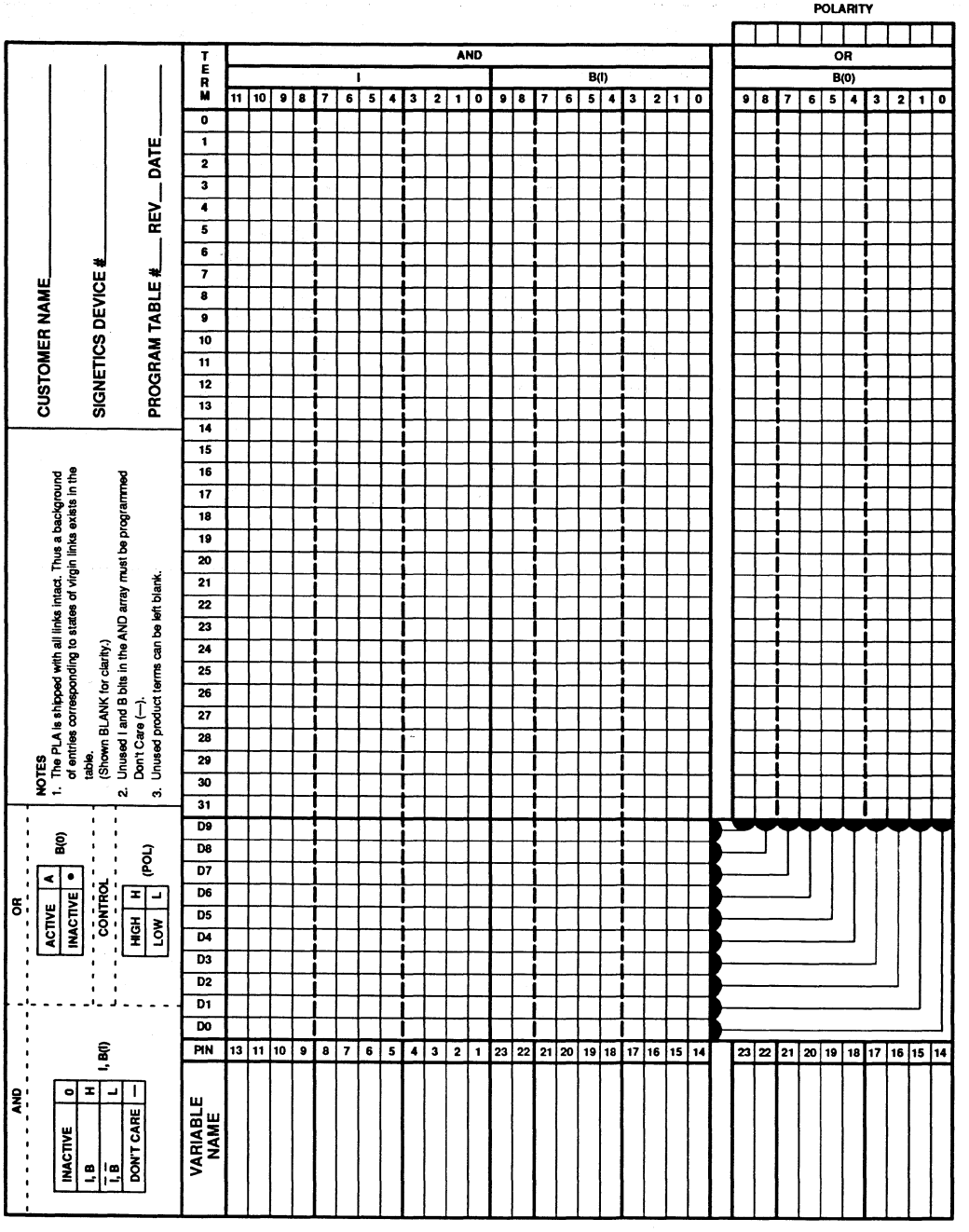
1. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates P_n, D_n.
2. Any gate P_n, D_n will be unconditionally inhibited if both the true and complement of any input (I, B) are left intact.

ABEL is a trademark of Data I/O Corp.
CUPL is a trademark of Logical Devices, Inc.

Programmable logic array (22 × 42 × 10)

PLUS173–10

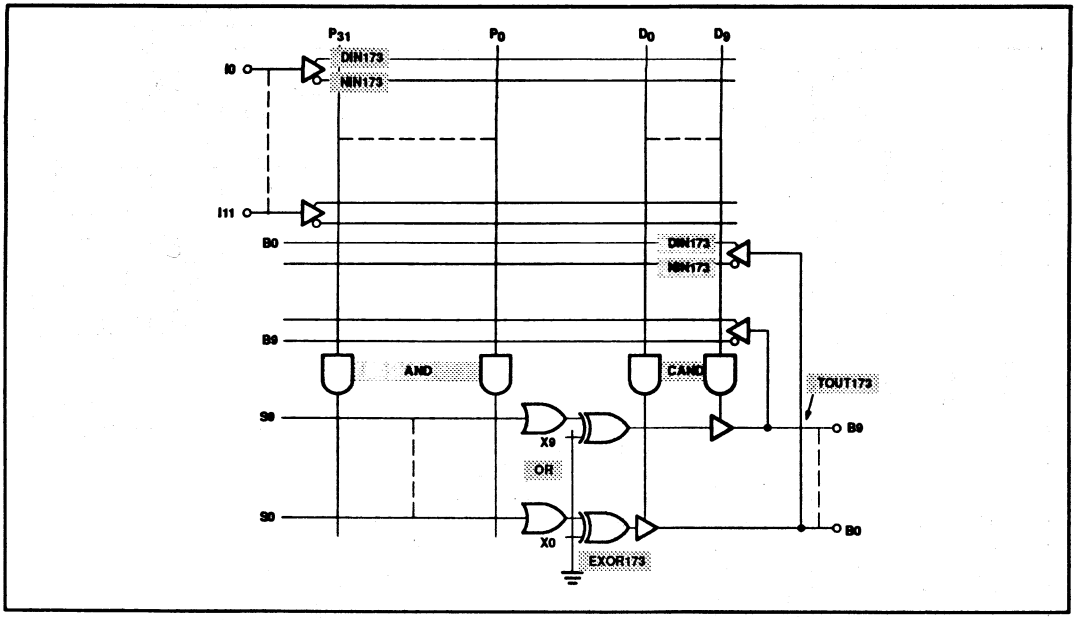
PLA PROGRAM TABLE



Programmable logic array (22 × 42 × 10)

PLUS173–10

SNAP RESOURCE SUMMARY DESIGNATIONS



Programmable logic arrays (16 × 48 × 8)

PLS100/PLS101

DESCRIPTION

The PLS100 (3-State) and PLS101 (Open Collector) are bipolar, fuse Programmable Logic Arrays (PLAs). Each device utilizes the standard AND/OR/Invert architecture to directly implement custom sum of product equations.

Each device consists of 16 dedicated inputs and 8 dedicated outputs. Each output is capable of being actively controlled by any or all of the 48 product terms. The True, Complement, or Don't Care condition of each of the 16 inputs and be ANDed together to comprise one P-term. All 48 P-terms can be selectively ORed to each output.

The PLS100 and PLS101 are fully TTL compatible, and chip enable control for expansion of input variables and output inhibit. They feature either Open Collector or 3-State outputs for ease of expansion of product terms and application in bus-organized systems.

Order codes are listed in the Ordering Information Table.

FEATURES

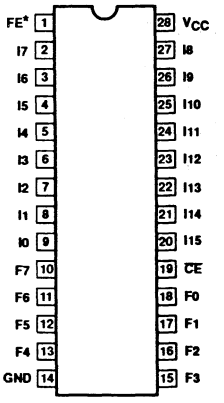
- Field-programmable (Ni-Cr link)
- Input variables: 16
- Output functions: 8
- Product terms: 48
- I/O propagation delay: 50ns (max.)
- Power dissipation: 600mW (typ.)
- Input loading: –100μA (max.)
- Chip Enable input
- Output option:
  - PLS100: 3-State
  - PLS101: Open-Collector
- Output disable function:
  - 3-State: Hi-Z
  - Open-Collector: High

APPLICATIONS

- CRT display systems
- Code conversion
- Peripheral controllers
- Function generators
- Look-up and decision tables
- Microprogramming
- Address mapping
- Character generators
- Data security encoders
- Fault detectors
- Frequency synthesizers
- 16-bit to 8-bit bus interface
- Random logic replacement

PIN CONFIGURATIONS

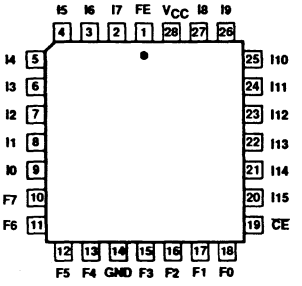
N Package



* Fuse Enable Pin: It is recommended that this pin be left open or connected to ground during normal operation.

N = Plastic DIP (600mil-wide)

A Package



A = Plastic Leaded Chip Carrier

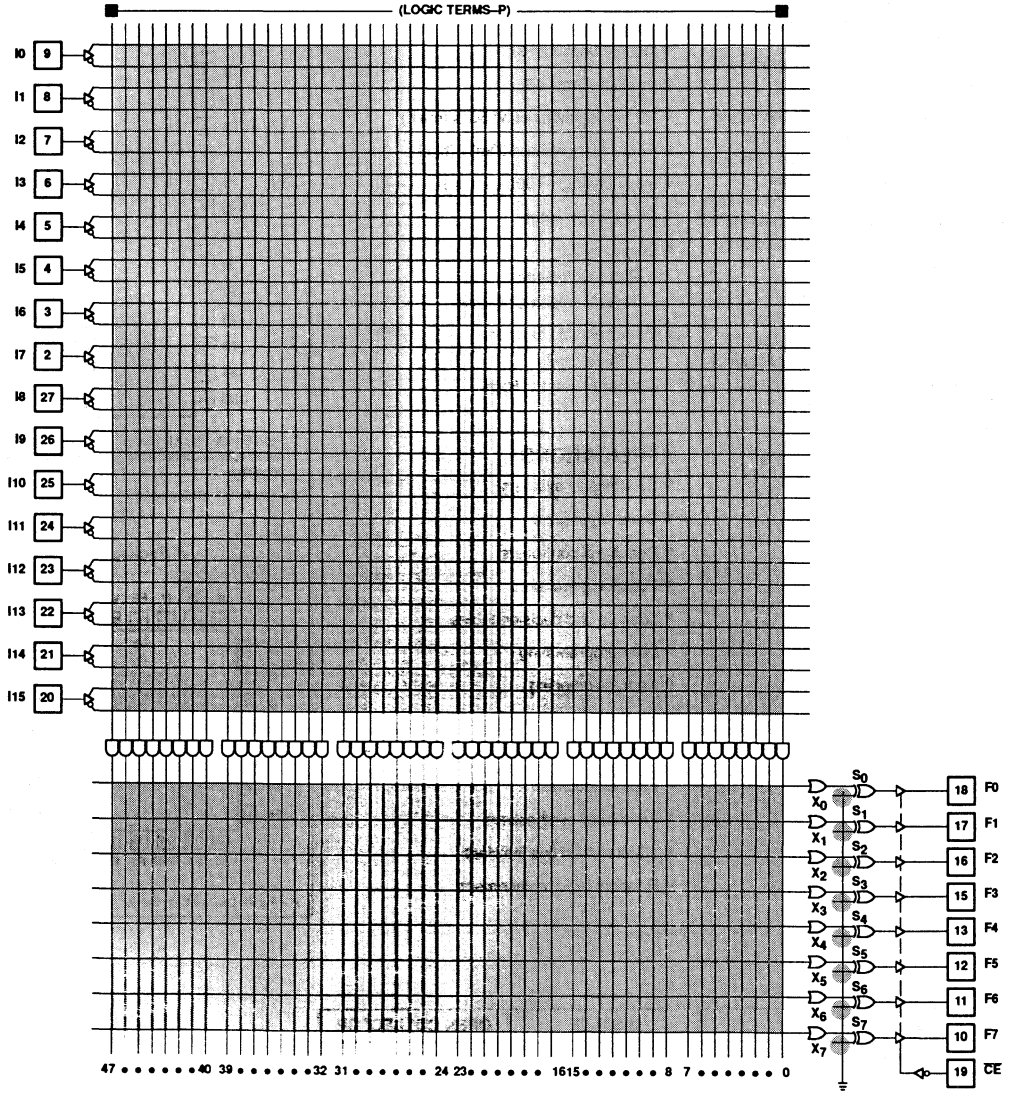
ORDERING INFORMATION

DESCRIPTION	3-STATE	OPEN COLLECTOR
28-Pin Plastic Dual In-Line 600mil-wide	PLS100N	PLS101N
28-Pin Plastic Leaded Chip Carrier	PLS100A	PLS101A

Programmable logic arrays (16 × 48 × 8)

PLS100/PLS101

LOGIC DIAGRAM

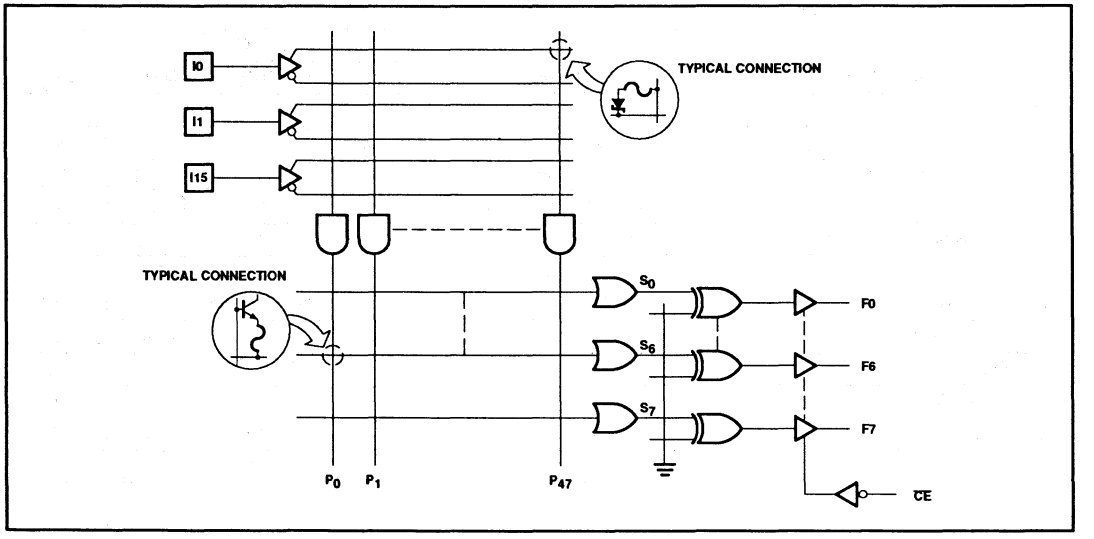


NOTES:
1. All AND gate inputs with a blown link float to a logic "1".
2. All OR gate inputs with a blown fuse float to logic "0".
3. ▒ Programmable connection.

Programmable logic arrays (16 × 48 × 8)

PLS100/PLS101

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS	UNIT
V_{CC}	Supply voltage	+7.0	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage	+5.5	V_{DC}
I_{IN}	Input current	±30	mA
I_{OUT}	Output current	+100	mA
T_{amb}	Operating temperature range	0 to +75	°C
T_{stg}	Storage temperature range	–65 to +150	°C

NOTE:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other conditions above those indicated in the operational and programming specification of the device is not implied.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

The PLS100 device is also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Handbook.

DC ELECTRICAL CHARACTERISTICS

$0°C \le T_{amb} \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[1]	MAX	
Input voltage[2]						
V_{IH}	High	V_{CC} = MAX	2.0			V
V_{IL}	Low	V_{CC} = MIN			0.8	V
V_{IC}	Clamp[3]	V_{CC} = MIN, I_{IN} = −12mA		−0.8	−1.2	V
Output voltage[2]						
		V_{CC} = MIN				
V_{OH}	High (PLS100)[4]	I_{OH} = −2mA	2.4			V
V_{OL}	Low[5]	I_{OL} = 9.6mA		0.35	0.45	V
Input current						
I_{IH}	High	V_{IN} = 5.5V		< 1	25	µA
I_{IL}	Low	V_{IN} = 0.45V		−10	−100	µA
Output current						
$I_{O(OFF)}$	Hi-Z state (PLS100)	$\overline{CE}$ = High, V_{CC} = MAX				
		V_{OUT} = 5.5V		1	40	µA
		V_{OUT} = 0.45V		−1	−40	µA
I_{OS}	Short circuit (PLS100) [3, 6]	$\overline{CE}$ = Low, V_{OUT} = 0V	−15		−70	mA
I_{CC}	V_{CC} supply current[7]	V_{CC} = MAX		120	170	mA
Capacitance						
		$\overline{CE}$ = High, V_{CC} = 5.0V				
C_{IN}	Input	V_{IN} = 2.0V		8		pF
C_{OUT}	Output	V_{OUT} = 2.0V		17		pF

NOTES:
1. All typical values are at V_{CC} = 5V, T_{amb} = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Test one pin at a time.
4. Measured with V_{IL} applied to $\overline{CE}$ and a logic high stored.
5. Measured with a programmed logic condition for which the output test is at a low logic level. Output sink current is applied through a resistor to V_{CC}.
6. Duration of short circuit should not exceed 1 second.
7. I_{CC} is measured with the Chip Enable input grounded, all other inputs at 4.5V and the outputs open.

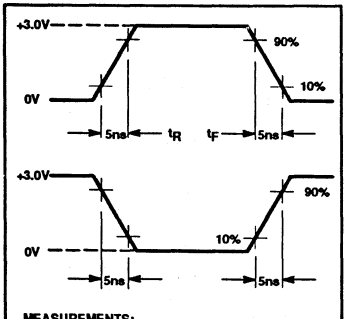
AC ELECTRICAL CHARACTERISTICS

$0°C \leq T_{amb} \leq +75°C$, $4.75 \leq V_{CC} \leq 5.25V$, $R_1 = 470\Omega$, $R_2 = 1k\Omega$

SYMBOL	PARAMETER	TO	FROM	LIMITS MIN	LIMITS TYP[1]	LIMITS MAX	UNIT
Propagation delay[2]							
t_{PD}	Input	Output	Input		35	50	ns
t_{CE}	Chip Enable[3]	Output	Chip Enable		15	30	ns
Disable time							
t_{CD}	Chip Disable[3]	Output	Chip Enable		15	30	ns

NOTES:
1. All typical values are at $V_{CC} = 5V$. $T_{amb} = +25°C$.
2. All propagation delays are measured and specified under worst case conditions.
3. For 3-State output; output enable times are tested with $C_L = 30pF$ to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with $C_L = 5pF$. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} - 0.5V)$ with S_1 open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with S_1 closed.

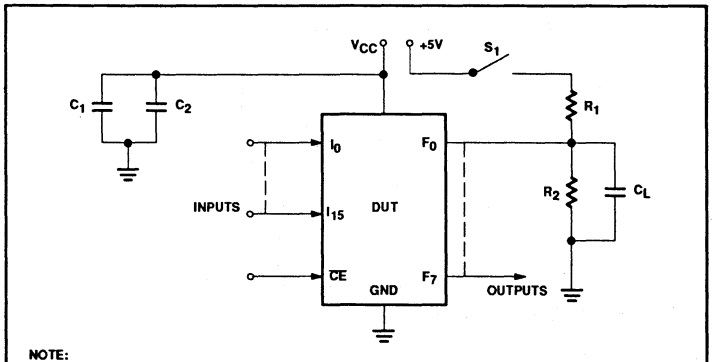
VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

TEST LOAD CIRCUIT

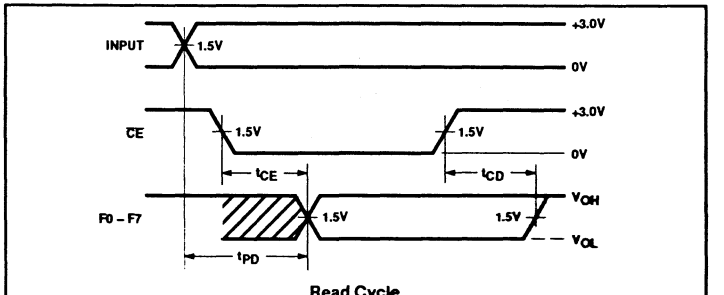


NOTE:
C_1 and C_2 are to bypass V_{CC} to GND.

TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{CE}	Delay between beginning of Chip Enable Low (with Input valid) and when Data Output becomes valid.
t_{CD}	Delay between when Chip Enable becomes High and Data Output is in off state (Hi-Z or High).
t_{PD}	Delay between beginning of valid Input (with Chip Enable Low) and when Data Output becomes valid.

TIMING DIAGRAM



Read Cycle

Programmable logic arrays (16 × 48 × 8)

PLS100/PLS101

LOGIC PROGRAMMING

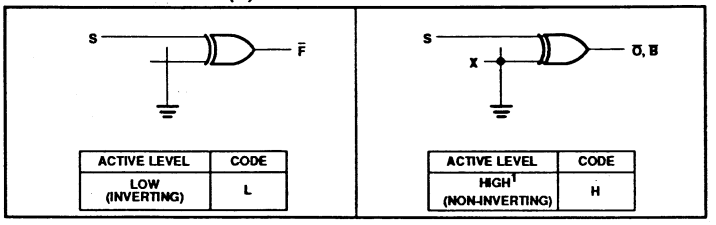
PLS100/PLS101 is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Signetics' SNAP and SLICE, Data I/O Corporation's ABEL and Logical Devices Inc.'s CUPL design software packages.

All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

PLS100/PLS101 logic designs can also be generated using the program table entry format detailed on the following pages. This program table entry format is supported by the Signetics' SNAP and SLICE PLD design software (PTP module) packages. SLICE is available free of charge to qualified users.

To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The sumbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

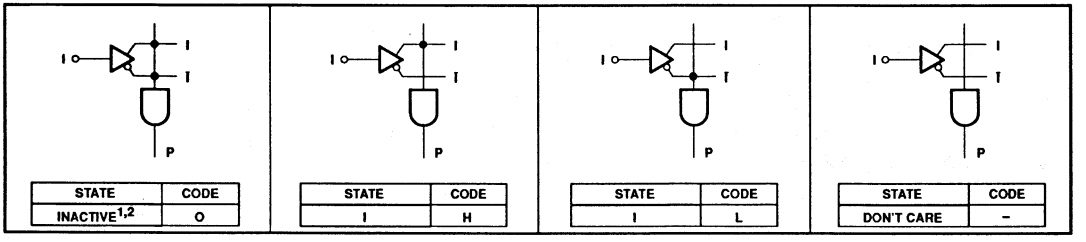
OUTPUT POLARITY – (F)



ACTIVE LEVEL	CODE
LOW (INVERTING)	L

ACTIVE LEVEL	CODE
HIGH[1] (NON-INVERTING)	H

"AND" ARRAY – (I)



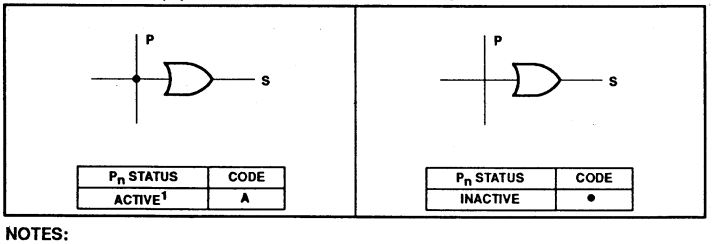
STATE	CODE
INACTIVE[1,2]	O

STATE	CODE
I	H

STATE	CODE
I	L

STATE	CODE
DON'T CARE	–

"OR" ARRAY – (F)



P_n STATUS	CODE
ACTIVE[1]	A

P_n STATUS	CODE
INACTIVE	•

NOTES:

1. This is the initial unprogrammed state of all links. It is normally associated with all unused (inactive) AND gates P_n.
2. Any gate P_n will be unconditionally inhibited if any one of its (I) link pairs is left intact.

VIRGIN STATE

The PLS100/101 virgin devices are factory shipped in an unprogrammed state, with all fuses intact, such that:

1. All P_n terms are disabled (inactive) in the AND array.
2. All P_n terms are active in the OR array.
3. All outputs are Active-High.

Programmable logic arrays (16 × 48 × 8)

PLS100/PLS101

PROGRAM TABLE

CUSTOMER NAME _____

PURCHASE ORDER # _____

SIGNETICS DEVICE # _____ CF (XXXX) _____

CUSTOMER SYMBOLIZED PART # _____

TOTAL NUMBER OF PARTS _____

PROGRAM TABLE # _____ REV ____ DATE ____

PROGRAM TABLE ENTRIES

INPUT VARIABLE			OUTPUT FUNCTION		OUTPUT ACTIVE LEVEL	
Im	Im	Don't Care	Prod. Term Present in Fp	Prod. Term Not Present in Fp	Active High	Active Low
H	L	– (dash)	A	• (period)	H	L

NOTE
Enter (–) for unused inputs of used P-terms.

NOTES
1. Entries independent of output polarity.
2. Enter (A) for unused outputs of used P-terms.

NOTES
1. Polarity programmed once only.
2. Enter (H) for all unused outputs.

	AND															
TERM	INPUT (I_m)															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0																
1																
2																
3																
4																
5																
6																
7																
8																
9																
10																
11																
12																
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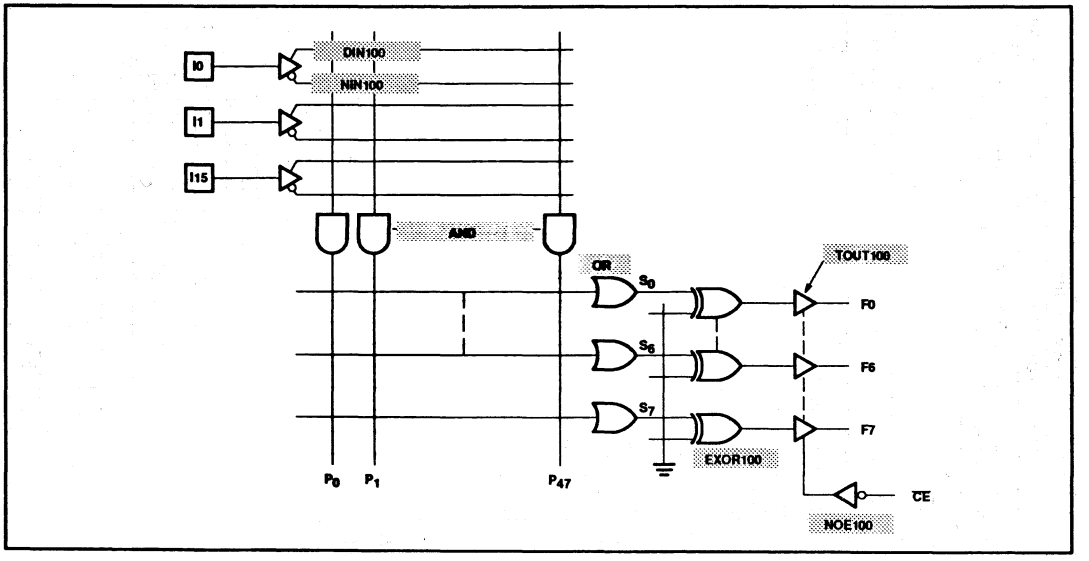
36																
37																
38																
39																
40																
41																
42																
43																
44																
45																
46																
47																
PIN NO.	20	21	22	23	24	25	26	27	2	3	4	5	6	7	8	9
VARIABLE NAME																

POLARITY										
OR OUTPUT (F_p)										
7	6	5	4	3	2	1	0			
10	11	12	13	15	16	17	18			

SNAP RESOURCE SUMMARY DESIGNATIONS



Section 5
Programmable Logic Sequencer Device Data Sheets

INDEX

Programmable logic sequencer (16 × 45 × 12)

PLS155

DESCRIPTION

The PLS155 is a 3-State output, registered logic element combining AND/OR gate arrays with clocked J-K flip-flops. These J-K flip-flops are dynamically convertible to D-type via a "fold-back" inverting buffer and control gate F_C. It features 4 registered I/O outputs (F) in conjunction with 8 bidirectional I/O lines (B). These yield variable I/O gate and register configurations via control gates (D, L) ranging from 16 inputs to 12 outputs.

The AND/OR arrays consist of 32 logic AND gates, 13 control AND gates, and 21 OR gates with fusible link connections for programming I/O polarity and direction. All AND gates are linked to 4 inputs (I), bidirectional I/O lines (B), internal flip-flop outputs (Q), and Complement Array output ($\overline{C}$). The Complement Array consists of a NOR gate optionally linked to all AND gates for generating and propagating complementary AND terms.

On-chip T/C buffers couple either True (I, B, Q) or Complement ($\overline{I}$, $\overline{B}$, $\overline{Q}$, $\overline{C}$) input polarities to all AND gates, whose outputs can be optionally linked to all OR gates. Any of the 32 AND gates can drive bidirectional I/O lines (B), whose output polarity is individually programmable through a set of Ex-OR gates for implementing AND-OR or AND-NOR logic functions. Similarly, any of the AND gates can drive the J-K inputs of all flip-flops. The Asynchronous Preset and Reset lines (P, R), are driven from the OR matrix.

All flip-flops are positive edge-triggered and can be used as input, output or I/O (for interfacing with a bidirectional data bus) in conjunction with load control gates (L), steering inputs (I), (B), (Q) and programmable output select lines (E).

The PLS155 is field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

Order codes are listed below.

FEATURES

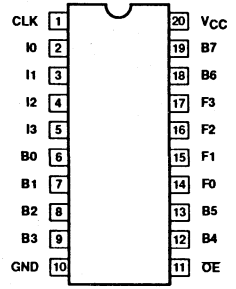
- f_{MAX} = 14MHz
  - 18.2MHz clock rate
- Field-Programmable (Ni-Cr link)
- 4 dedicated inputs
- 13 control gates
- 32 AND gates
- 21 OR gates
- 45 product terms:
  - 32 logic terms
  - 13 control terms
- 8 bidirectional I/O lines
- 4 bidirectional registers
- J-K, T, or D-type flip-flops
- Asynchronous Preset/Reset
- Complement Array
- Active-High or -Low outputs
- Programmable $\overline{OE}$ control
- Positive edge-triggered clock
- Input loading: –100μA (max.)
- Power dissipation: 750mW (typ.)
- TTL compatible
- 3-State outputs

APPLICATIONS

- Random sequential logic
- Synchronous up/down counters
- Shift registers
- Bidirectional data buffers
- Timing function generators
- System controllers/synchronizers
- Priority encoder/registers

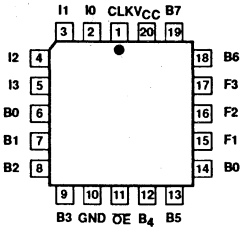
PIN CONFIGURATIONS

N Package



N = Plastic Dual In-Line Package (300mil-wide)

A Package



A = Plastic Leaded Chip Carrier

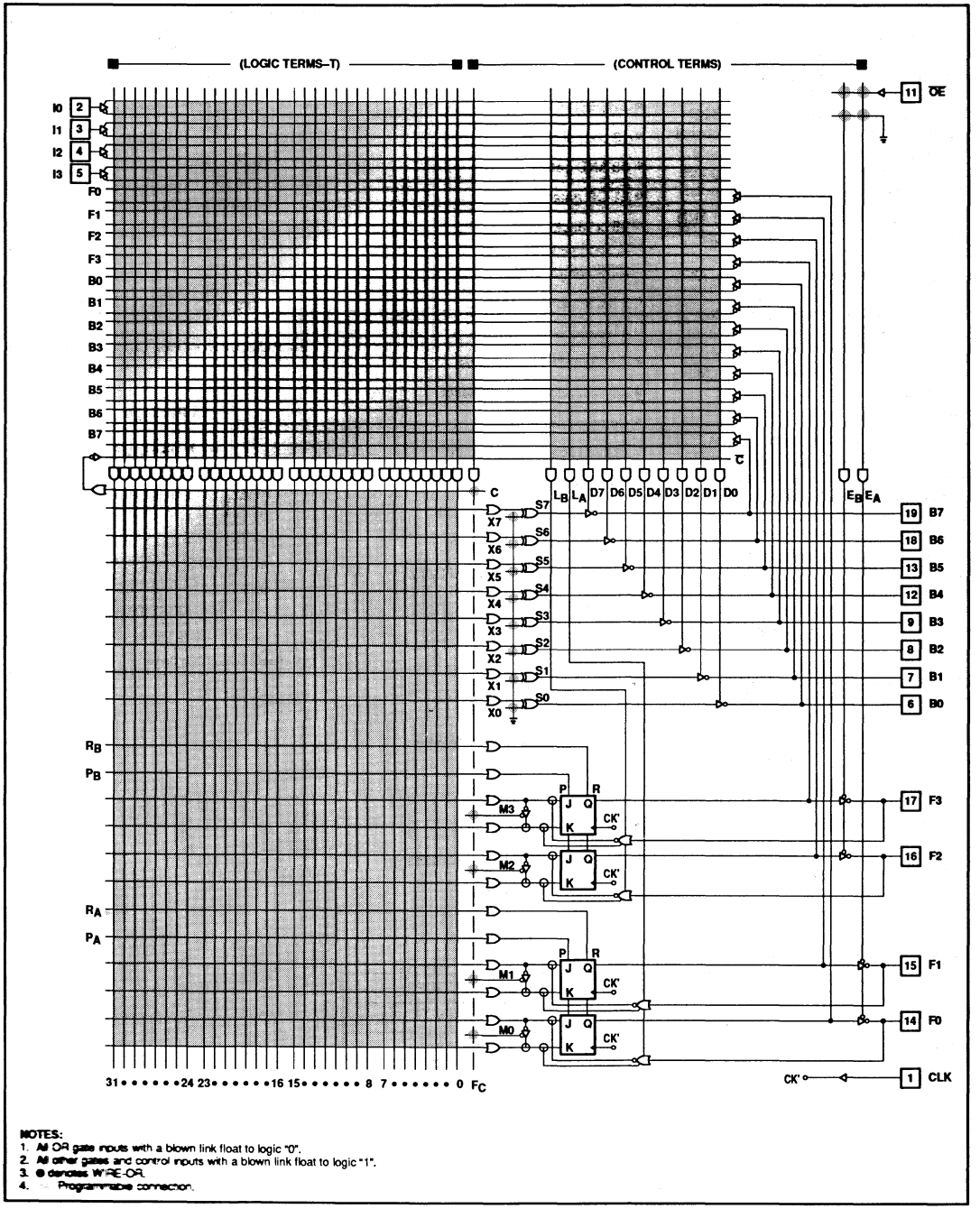
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
20-Pin Plastic Dual In-Line Package (300mil-wide)	PLS155N
20-Pin Plastic Leaded Chip Carrier	PLS155A

Programmable logic sequencer (16 × 45 × 12)

PLS155

LOGIC DIAGRAM

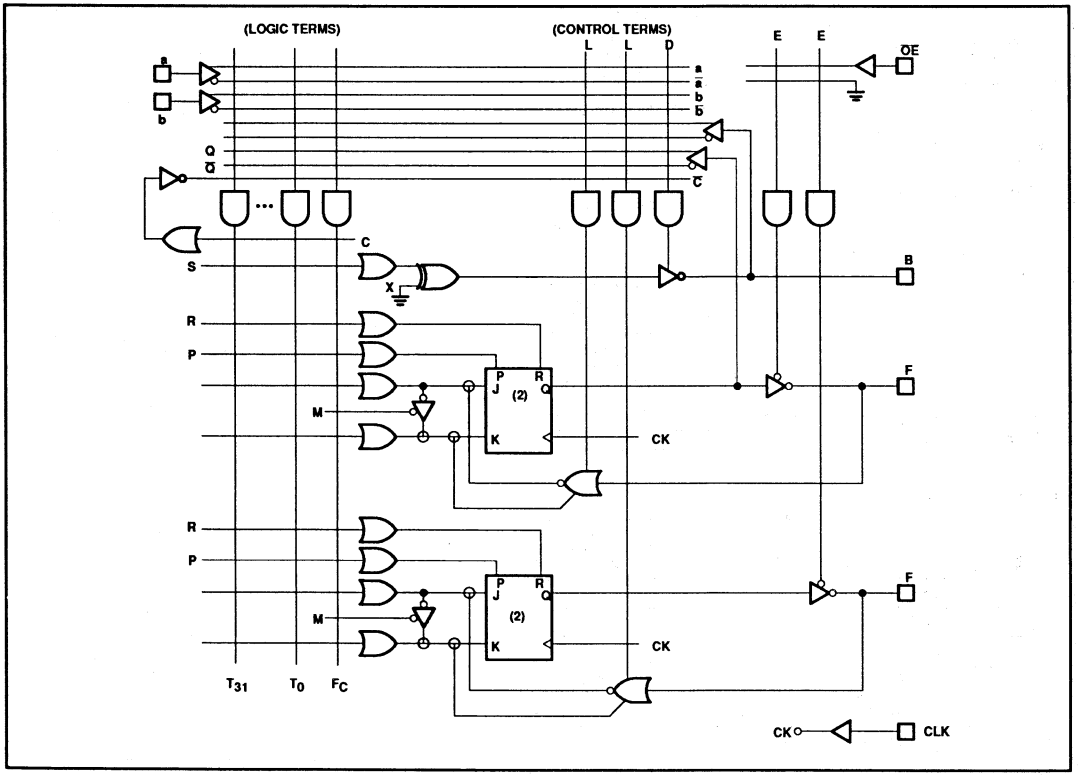


NOTES:
1. All OR gate inputs with a blown link float to logic "0".
2. All other gates and control inputs with a blown link float to logic "1".
3. ● denotes WIRE-OR.
4. Programmable connection.

Programmable logic sequencer (16 × 45 × 12)

PLS155

FUNCTIONAL DIAGRAM



FLIP-FLOP TRUTH TABLE

OE	L	CK	P	R	J	K	Q	F
H								Hi-Z
L	X	X	H	L	X	X	H	L
L	X	X	L	H	X	X	L	H
L	L	↑	L	L	L	L	Q	$\overline{Q}$
L	L	↑	L	L	L	H	L	H
L	L	↑	L	L	H	L	H	L
L	L	↑	L	L	H	H	$\overline{Q}$	Q
H	H	↑	L	L	L	H	L	H*
H	H	↑	L	L	H	L	H	L*
+10V	X	↑	X	X	L	H	L	H**
	X	↑	X	X	H	L	H	L**

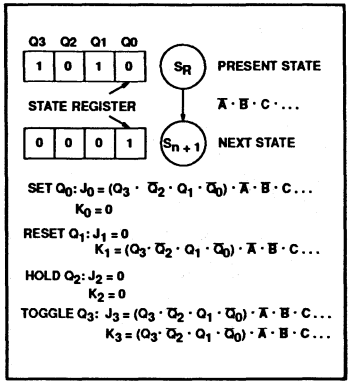
NOTES:

1. Positive Logic:
   $J\text{-}K = T_0 + T_1 + T_2 \ldots\ldots\ldots\ldots T_{31}$
   $T_n = \overline{C} \cdot (I_0 \cdot I_1 \cdot I_2 \ldots) \cdot (Q_0 \cdot Q_1 \ldots) \cdot (B_0 \cdot B_1 \cdot \ldots)$
2. ↑ denotes transition from Low to High level.
3. X = Don't care
4. * = Forced at F_n pin for loading the J-K flip-flop in the Input mode. The load control term, L_n must be enabled (HIGH) and the p-terms that are connected to the associated flip-flop must be forced LOW (disabled) during Preload.
5. At P = R = H, Q = H. The final state of Q depends on which is released first.
6. ** = Forced at F_n pin to load J-K flip-flop independent of program code (Diagnostic mode), 3-State B outputs.

Programmable logic sequencer (16 × 45 × 12)

PLS155

LOGIC FUNCTION



NOTE:
Similar logic functions are applicable for D and T mode flip-flops.

VIRGIN STATE

The factory shipped virgin device contains all fusible links intact, such that:

1. $\overline{OE}$ is always enabled.
2. Preset and Reset are always disabled.
3. All transition terms are disabled.
4. All flip-flops are in D-mode unless otherwise programmed to J-K only or J-K or D (controlled).
5. All B pins are inputs and all F pins are outputs unless otherwise programmed.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS Min	RATINGS Max	UNIT
V_{CC}	Supply voltage		+7	V_{DC}
V_{IN}	Input voltage		+5.5	V_{DC}
V_{OUT}	Output voltage		+5.5	V_{DC}
I_{IN}	Input currents	–30	+30	mA
I_{OUT}	Output currents		+100	mA
T_{amb}	Operating temperature range	0	+75	°C
T_{stg}	Storage temperature range	–65	+150	°C

NOTES:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

DC ELECTRICAL CHARACTERISTICS

$0°C \leq T_{amb} \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			MIN	TYP[1]	MAX	
Input voltage[2]						
V_{IH}	High	V_{CC} = MAX	2.0			V
V_{IL}	Low	V_{CC} = MIN			0.8	V
V_{IC}	Clamp	V_{CC} = MIN, I_{IN} = –12mA		–0.8	–1.2	V
Output voltage[2]						
		V_{CC} = MIN				
V_{OH}	High	I_{OH} = –2mA	2.4			V
V_{OL}	Low	I_{OL} = 10mA		0.35	0.5	V
Input current[5]						
		V_{CC} = MAX				
I_{IH}	High	V_{IN} = 5.5V		<1	80	µA
I_{IL}	Low	V_{IN} = 0.45V		–10	–100	µA
Output current						
		V_{CC} = MAX				
$I_{O(OFF)}$	Hi-Z state[5, 6]	V_{OUT} = 5.5V		1	80	µA
		V_{OUT} = 0.45V		–1	–140	µA
I_{OS}	Short circuit[3, 7]	V_{OUT} = 0V	–15		–70	mA
I_{CC}	V_{CC} supply current[4]	V_{CC} = MAX		150	190	mA
Capacitance						
		V_{CC} = 5.0V				
C_{IN}	Input	V_{IN} = 2.0V		8		pF
C_{OUT}	Output	V_{OUT} = 2.0V		15		pF

NOTES:
1. All typical values are at V_{CC} = 5V, T_{amb} = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Test one at a time.
4. I_{CC} is measured with the $\overline{OE}$ input grounded, all other inputs at 4.5V and the outputs open.
5. Leakage values are a combination of input and output leakage.
6. Measured with V_{IH} applied to $\overline{OE}$.
7. Duration of short circuit should not exceed 1 second.

Programmable logic sequencer (16 × 45 × 12)

PLS155

AC ELECTRICAL CHARACTERISTICS

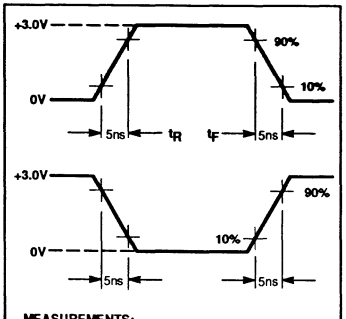
$0°C \le T_{amb} \le +75°C$, $4.75V \le V_{CC} \le 5.25V$, $R_1 = 470\Omega$, $R_2 = 1k\Omega$

SYMBOL	PARAMETER	FROM	TO	TEST CONDITION	LIMITS MIN	LIMITS TYP[1]	LIMITS MAX	UNIT
Pulse width								
t_{CKH}	Clock[2] High	CK +	CK –	C_L = 30pF	25	20		ns
t_{CKL}	Clock Low	CK –	CK +	C_L = 30pF	30	20		ns
t_{CKP}	Period	CK +	CK +	C_L = 30pF	70	50		ns
t_{PRH}	Preset/Reset pulse	(I,B) –	(I,B) +	C_L = 30pF	40	30		ns
Setup time[5]								
t_{IS1}	Input	(I,B) ±	CK +	C_L = 30pF	40	30		ns
t_{IS2}	Input (through F_n)	F ±	CK +	C_L = 30pF	20	10		ns
t_{IS3}	Input (through Complement Array)[4]	(I,B) ±	CK +	C_L = 30pF	65	40		ns
Hold time								
t_{IH1}	Input	(I,B) ±	CK +	C_L = 30pF	0	–10		ns
t_{IH2}	Input	F ±	CK +	C_L = 30pF	15	10		ns
Propagation delays								
t_{CKO}	Clock	CK +	F ±	C_L = 30pF		25	30	ns
t_{OE1}	Output enable[3]	$\overline{OE}$ –	F –	C_L = 30pF		20	30	ns
t_{OD1}	Output disable[3]	$\overline{OE}$ +	F +	C_L = 5pF		20	30	ns
t_{PD}	Output	(I,B) ±	B ±	C_L = 30pF		40	50	ns
t_{OE2}	Output enable[3]	(I,B) +	B ±	C_L = 30pF		35	55	ns
t_{OD2}	Output disable[3]	(I,B) –	B +	C_L = 5pF		30	35	ns
t_{PRO}	Preset/Reset	(I,B) +	F ±	C_L = 30pF		50	55	ns

NOTES:

1. All typical values are at V_{CC} = 5V, T_{amb} = +25°C.
2. To prevent spurious clocking, clock rise time (10% – 90%) ≤ 10ns.
3. For 3-State output; output enable times are tested with C_L = 30pF to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with C_L = 5pF. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} - 0.5V)$ with S_1 open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with S_1 closed.
4. When using the Complement Array t_{CKP} = 95ns (min).
5. Limits are guaranteed with 12 product terms maximum connected to each sum term line.
6. For test circuits, waveforms and timing diagrams see the following pages.

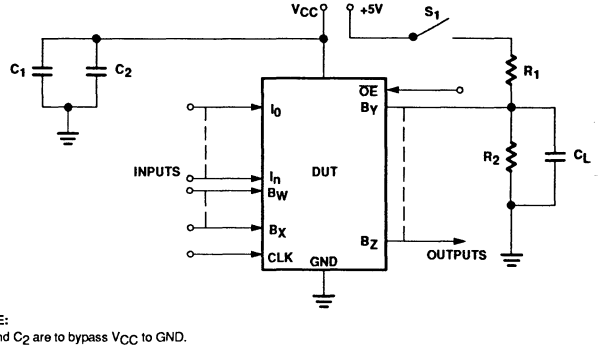
VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

TEST LOAD CIRCUIT

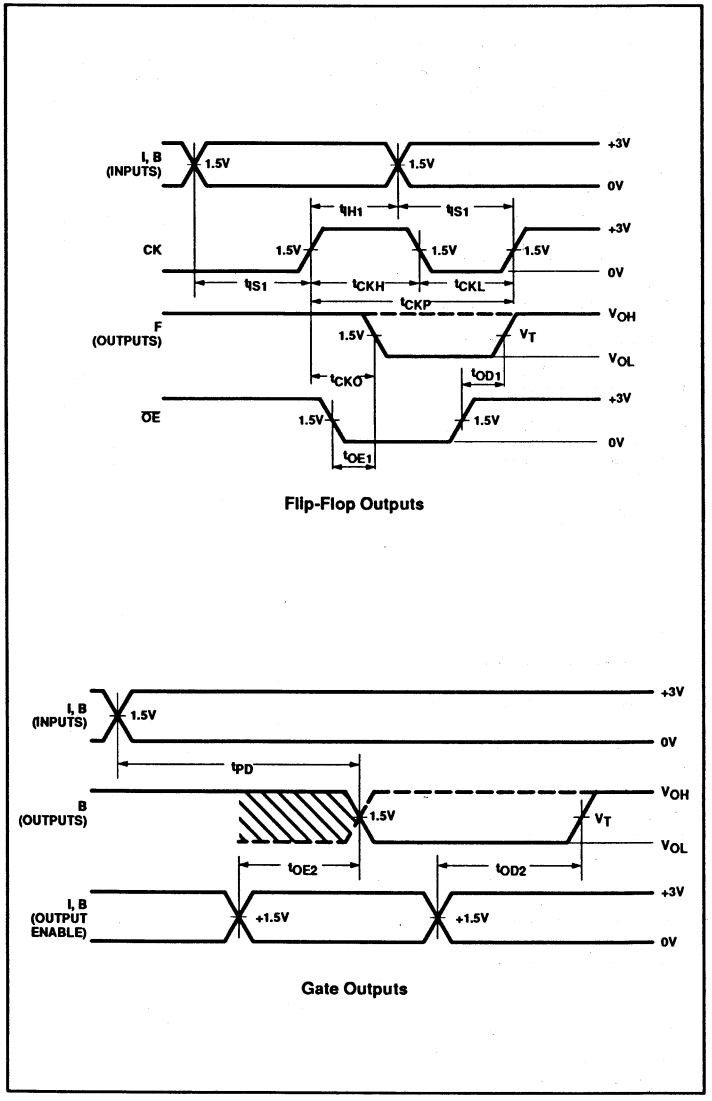


NOTE:
C_1 and C_2 are to bypass V_{CC} to GND.

Programmable logic sequencer (16 × 45 × 12)

PLS155

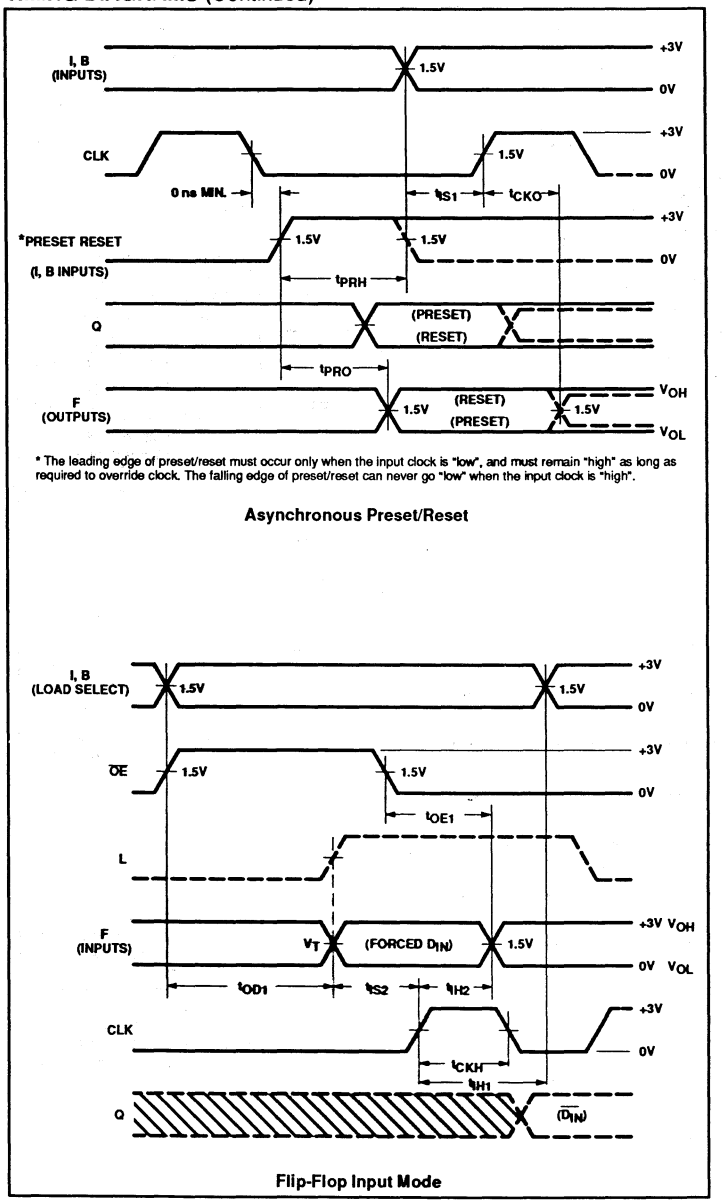
TIMING DIAGRAMS



TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{CKH}	Width of input clock pulse.
t_{CKL}	Interval between clock pulses.
t_{CKP}	Clock period.
t_{PRH}	Width of preset input pulse.
t_{S1}	Required delay between beginning of valid input and positive transition of clock.
t_{S2}	Required delay between beginning of valid input forced at flip-flop output pins, and positive transition of clock.
t_{H1}	Required delay between positive transition of clock and end of valid input data.
t_{H2}	Required delay between positive transition of clock and end of valid input data forced at flip-flop output pins.
t_{CKO}	Delay between positive transition of clock and when outputs become valid (with $\overline{OE}$ Low).
t_{OE1}	Delay between beginning of Output Enable Low and when outputs become valid.
t_{OD1}	Delay between beginning of Output Enable High and when outputs are in the OFF-State.
t_{PD}	Propagation delay between combinational inputs and outputs.
t_{OE2}	Delay between predefined Output Enable High, and when combinational outputs become valid.
t_{OD2}	Delay between predefined Output Enable Low and when combinational outputs are in the OFF-State.
t_{PRO}	Delay between positive transition of predefined Preset/Reset input, and when flip-flop outputs become valid.

TIMING DIAGRAMS (Continued)



* The leading edge of preset/reset must occur only when the input clock is "low", and must remain "high" as long as required to override clock. The falling edge of preset/reset can never go "low" when the input clock is "high".

Asynchronous Preset/Reset

Flip-Flop Input Mode

Programmable logic sequencer (16 × 45 × 12)

PLS155

LOGIC PROGRAMMING

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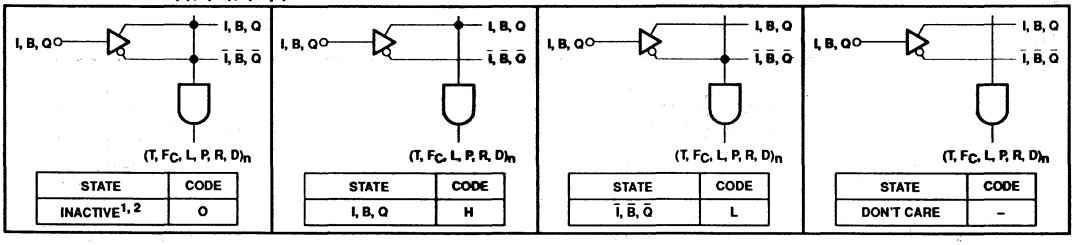
To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

"AND" ARRAY – (I), (B), (Qp)



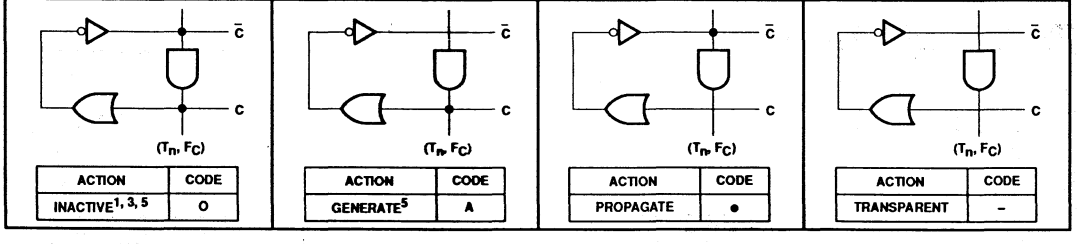
STATE	CODE
INACTIVE[1, 2]	O

STATE	CODE
I, B, Q	H

STATE	CODE
Ī, B̄, Q̄	L

STATE	CODE
DON'T CARE	–

"COMPLEMENT" ARRAY – (C)



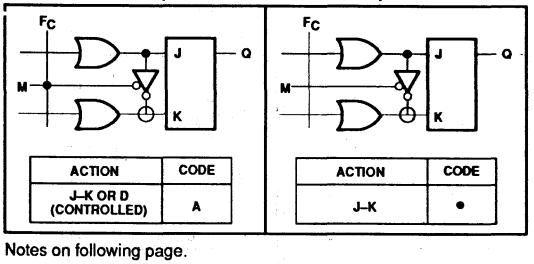
ACTION	CODE
INACTIVE[1, 3, 5]	O

ACTION	CODE
GENERATE[5]	A

ACTION	CODE
PROPAGATE	•

ACTION	CODE
TRANSPARENT	–

"OR" ARRAY – (F-F CONTROL MODE)



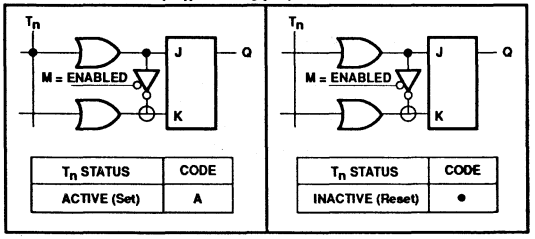
ACTION	CODE
J–K OR D (CONTROLLED)	A

ACTION	CODE
J–K	•

Notes on following page.

ABEL is a trademark of Data I/O Corp.
CUPL is a trademark of Logical Devices, Inc.

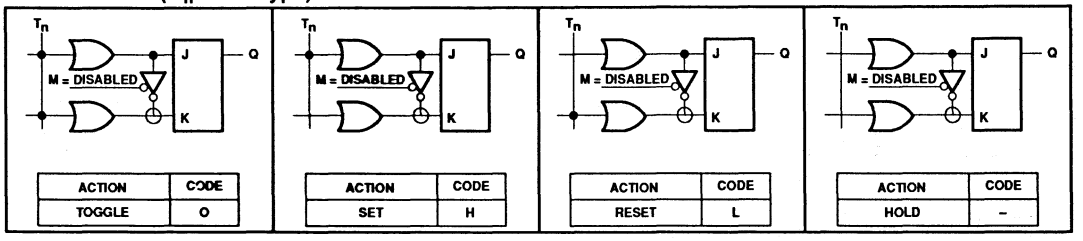
"OR" ARRAY – (Q_n = D-Type)



T_n STATUS	CODE
ACTIVE (Set)	A

T_n STATUS	CODE
INACTIVE (Reset)	•

"OR" ARRAY – (Q_n = J-K Type)



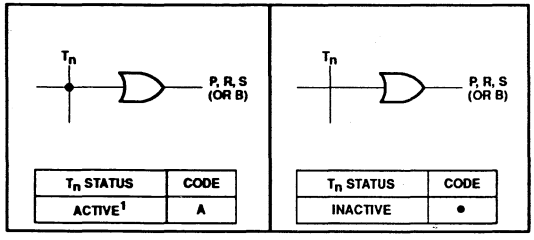
ACTION	CODE
TOGGLE	O

ACTION	CODE
SET	H

ACTION	CODE
RESET	L

ACTION	CODE
HOLD	–

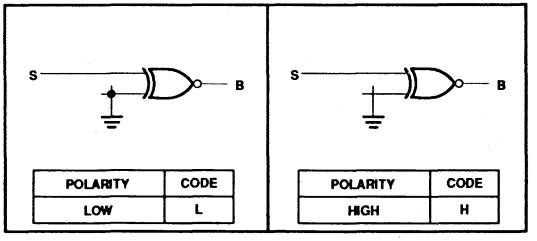
"OR" ARRAY – (S or B), (P), (R)



T_n STATUS	CODE
ACTIVE[1]	A

T_n STATUS	CODE
INACTIVE	•

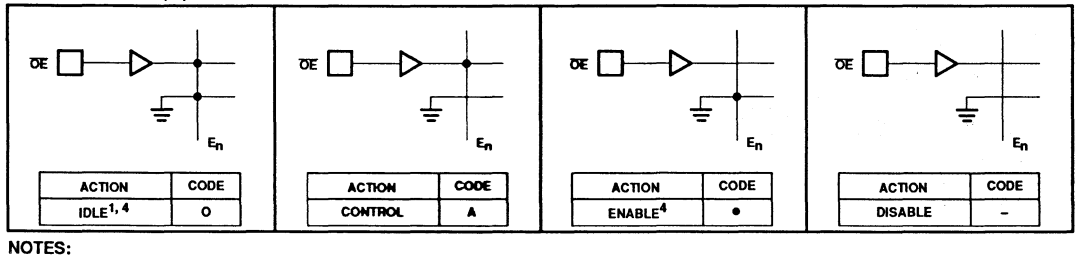
"EX-OR" ARRAY – (B)



POLARITY	CODE
LOW	L

POLARITY	CODE
HIGH	H

"$\overline{OE}$" ARRAY – (E)



ACTION	CODE
IDLE[1, 4]	O

ACTION	CODE
CONTROL	A

ACTION	CODE
ENABLE[4]	•

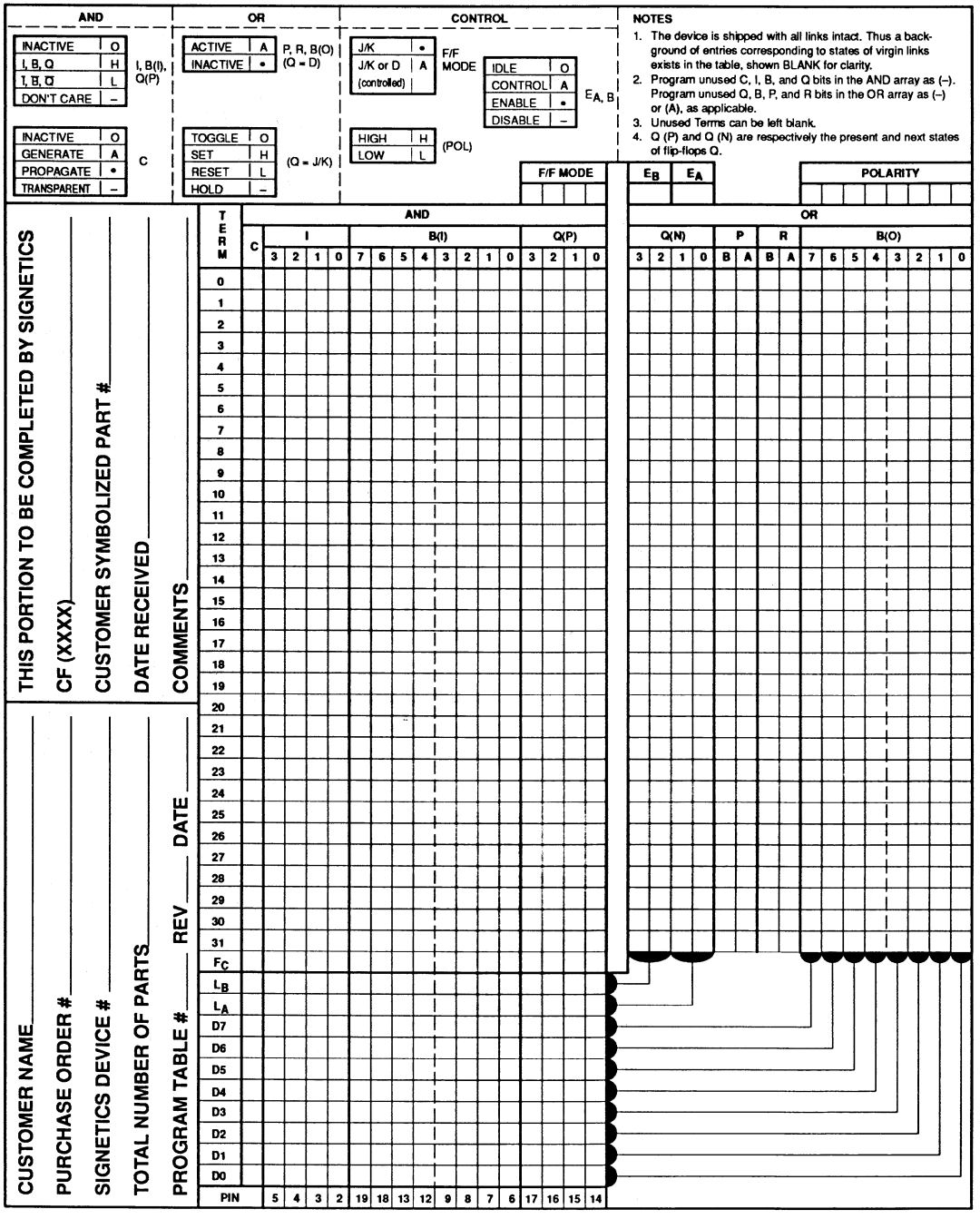
ACTION	CODE
DISABLE	–

NOTES:
1. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates.
2. Any gate (T, F_C, L, P, R, D)$_n$ will be unconditionally inhibited if both of the I, B, or Q links are left intact.
3. To prevent oscillations, this state is not allowed for C link pairs coupled to active gates T_n, F_C.
4. E_n = O and E_n = • are logically equivalent states, since both cause F_n outputs to be unconditionally enabled.
5. These states are not allowed for control gates (L, P, R, D)$_n$ due to their lack of "OR" array links.

Programmable logic sequencer (16 × 45 × 12)

PLS155

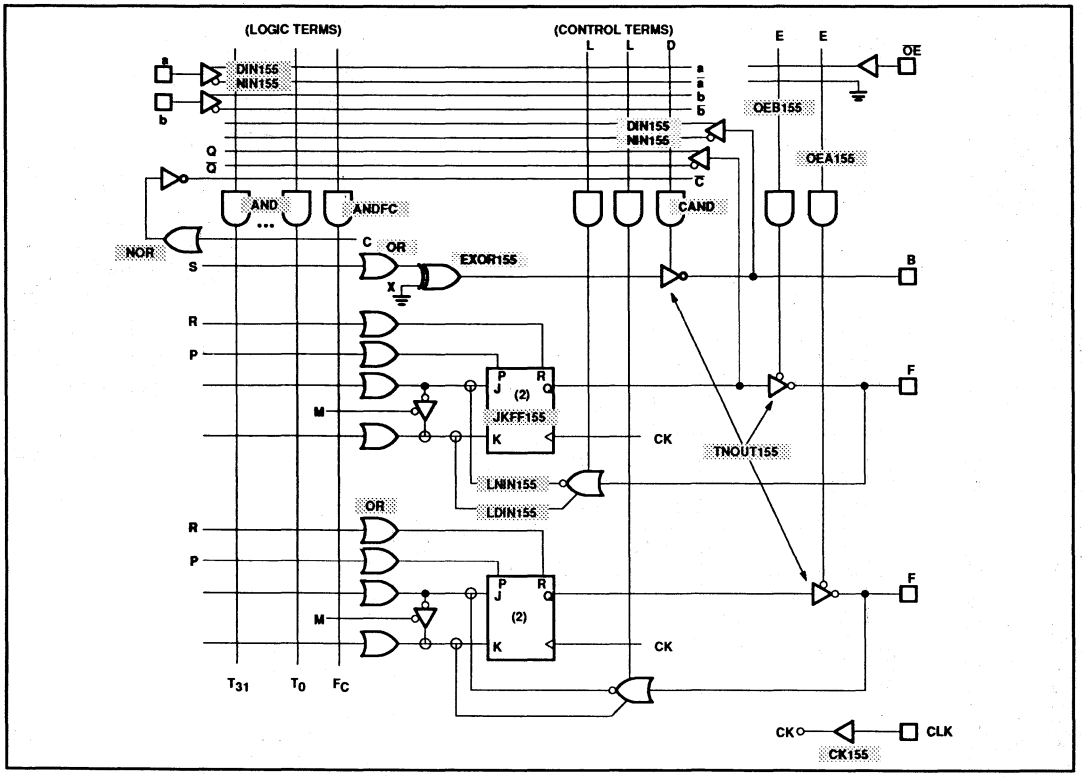
PROGRAM TABLE



Programmable logic sequencer (16 × 45 × 12)

PLS155

SNAP RESOURCE SUMMARY DESIGNATIONS



Programmable logic sequencer (16 × 45 × 12)

PLS157

DESCRIPTION

The PLS157 is a 3-State output, registered logic element combining AND/OR gate arrays with clocked J-K flip-flops. These J-K flip-flops are dynamically convertible to D-type via a "fold-back" inverting buffer and control gate F_C. It features 6 registered I/O outputs (F) in conjunction with 6 bidirectional I/O lines (B). These yield variable I/O gate and register configurations via control gates (D, L) ranging from 16 inputs to 12 outputs.

The AND/OR arrays consist of 32 logic AND gates, 13 control AND gates, and 21 OR gates with fusible link connections for programming I/O polarity and direction. All AND gates are linked to 4 inputs (I), bidirectional I/O lines (B), internal flip-flop outputs (Q), and Complement Array output ($\overline{C}$). The Complement Array consists of a NOR gate optionally linked to all AND gates for generating and propagating complementary AND terms.

On-chip T/C buffers couple either True (I, B, Q) or Complement ($\overline{I}$, $\overline{B}$, $\overline{Q}$, $\overline{C}$) input polarities to all AND gates, whose outputs can be optionally linked to all OR gates. Any of the 32 AND gates drives bidirectional I/O lines (B), whose output polarity is individually programmable through a set of Ex-OR gates for implementing AND-OR or AND-NOR logic functions. Similarly, any of the 32 AND gates can drive the J-K inputs of all flip-flops. The Asynchronous Preset and Reset lines (P, R), are driven from the AND array for 4 of the 8 registers. The Preset and Reset lines (P, R) controlling the lower four registers are driven from the OR matrix.

All flip-flops are positive edge-triggered and can be used as input, output or I/O (for interfacing with a bidirectional data bus) in conjunction with load control gates (L), steering inputs (I), (B), (Q) and programmable output select lines (E).

The PLS157 is field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

Order codes are listed below.

FEATURES

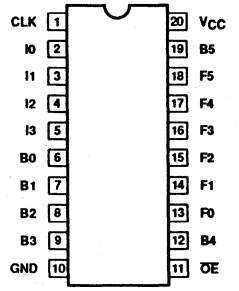
- f_{MAX} = 14MHz
  - 18.2MHz clock rate
- Field-Programmable (Ni-Cr link)
- 4 dedicated inputs
- 13 control gates
- 32 AND gates
- 21 OR gates
- 45 product terms:
  - 32 logic terms
  - 13 control terms
- 6 bidirectional I/O lines
- 6 bidirectional registers
- J-K, T, or D-type flip-flops
- 3-State outputs
- Asynchronous Preset/Reset
- Complement Array
- Active-High or -Low outputs
- Programmable $\overline{OE}$ control
- Positive edge-triggered clock
- Input loading: −100μA (max.)
- Power dissipation: 750mW (typ.)
- TTL compatible

APPLICATIONS

- Random sequential logic
- Synchronous up/down counters
- Shift registers
- Bidirectional data buffers
- Timing function generators
- System controllers/synchronizers
- Priority encoder/registers

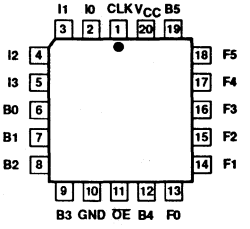
PIN CONFIGURATIONS

N Package



N = Plastic Dual In-Line Package (300mil-wide)

A Package



A = Plastic Leaded Chip Carrier

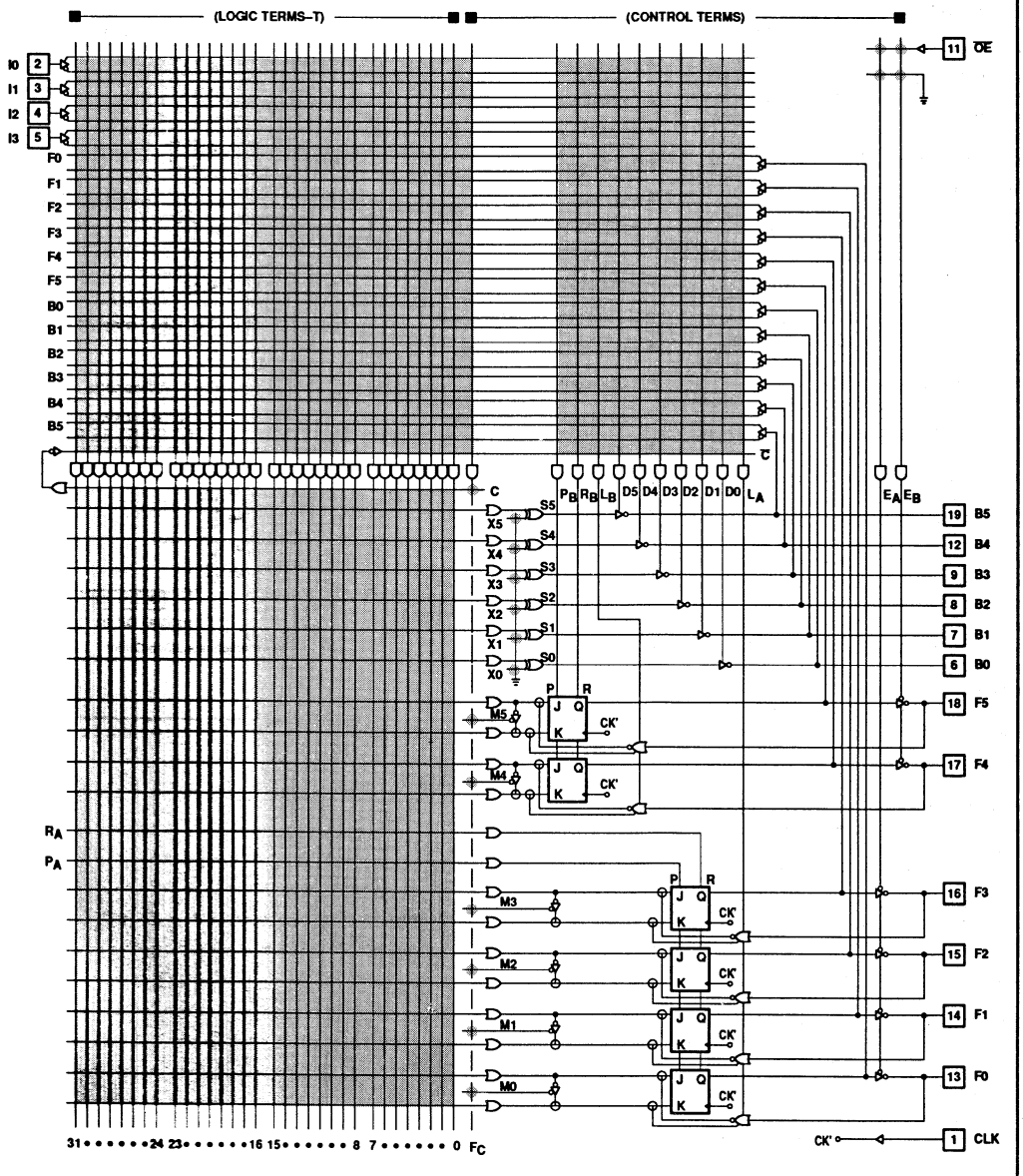
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
20-Pin Plastic Dual In-Line Package (300mil-wide)	PLS157N
20-Pin Plastic Leaded Chip Carrier	PLS157A

Programmable logic sequencer (16 × 45 × 12)

PLS157

LOGIC DIAGRAM

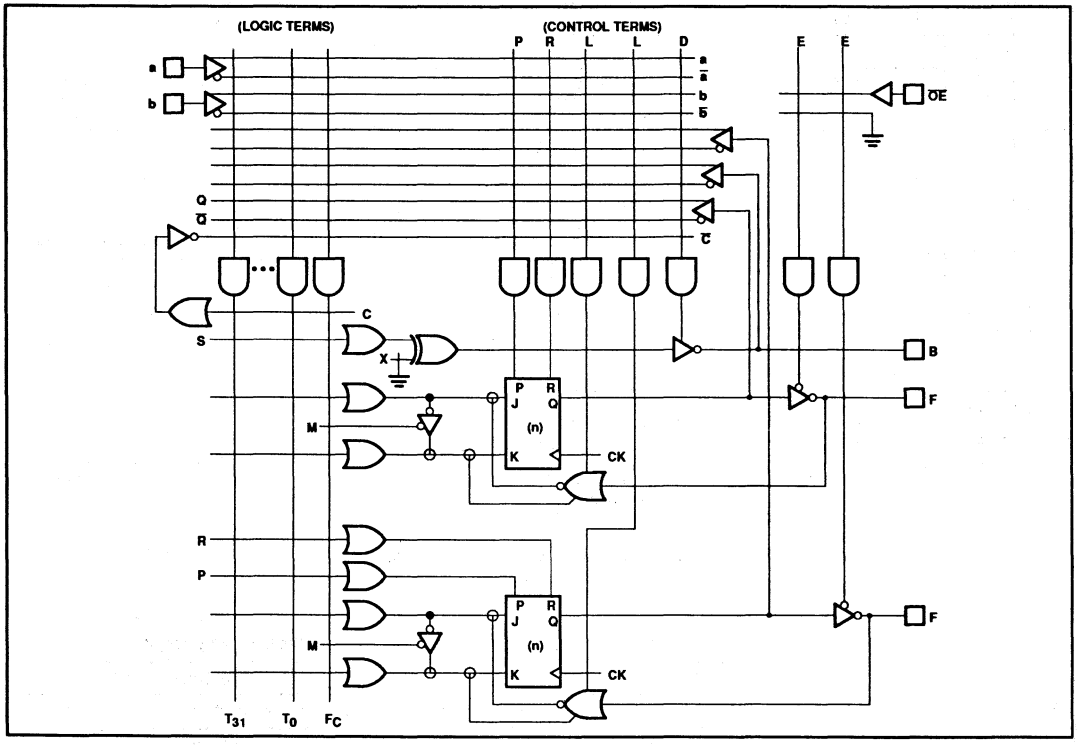


NOTES:
1. All OR gate inputs with a blown link float to logic "0".
2. All other gates and control inputs with a blown link float to logic "1".
3. ⊕ denotes WIRE-OR.
4. ▒ Programmable connection.

Programmable logic sequencer (16 × 45 × 12)

PLS157

FUNCTIONAL DIAGRAM

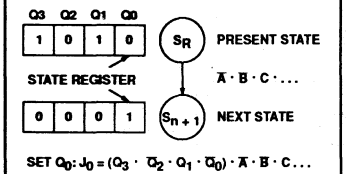


VIRGIN STATE

The factory shipped virgin device contains all fusible links intact, such that:

1. $\overline{OE}$ is always enabled.
2. Preset and Reset are always disabled.
3. All transition terms are disabled.
4. All flip-flops are in D-mode unless otherwise programmed to J-K only or J-K or D (controlled).
5. All B pins are inputs and all F pins are outputs unless otherwise programmed.

LOGIC FUNCTION



SET Q_0: $J_0 = (Q_3 \cdot \overline{Q}_2 \cdot Q_1 \cdot \overline{Q}_0) \cdot \overline{A} \cdot \overline{B} \cdot C \ldots$
$K_0 = 0$

RESET Q_1: $J_1 = 0$
$K_1 = (Q_3 \cdot \overline{Q}_2 \cdot Q_1 \cdot \overline{Q}_0) \cdot \overline{A} \cdot \overline{B} \cdot C \ldots$

HOLD Q_2: $J_2 = 0$
$K_2 = 0$

TOGGLE Q_3: $J_3 = (Q_3 \cdot \overline{Q}_2 \cdot Q_1 \cdot \overline{Q}_0) \cdot \overline{A} \cdot \overline{B} \cdot C \ldots$
$K_3 = (Q_3 \cdot \overline{Q}_2 \cdot Q_1 \cdot \overline{Q}_0) \cdot \overline{A} \cdot \overline{B} \cdot C \ldots$

NOTE:
Similar logic functions are applicable for D and T mode flip-flops.

FLIP-FLOP TRUTH TABLE

$\overline{OE}$	L	CK	P	R	J	K	Q	F
H								Hi-Z
L	X	X	H	L	X	X	H	L
L	X	X	L	H	X	X	L	H
L	L	↑	L	L	L	L	Q	$\overline{Q}$
L	L	↑	L	L	L	H	L	H
L	L	↑	L	L	H	L	H	L
L	L	↑	L	L	H	H	$\overline{Q}$	Q
H	H	↑	L	L	L	H	L	H*
H	H	↑	L	L	H	L	H	L*
+10V	X	↑	X	X	L	H	L	H* *
	X	↑	X	X	H	L	H	L* *

NOTES:

1. Positive Logic: $\overline{J\text{-}K} = T_0 + T_1 + T_2 \ldots\ldots\ldots\ldots T_{31}$
   $T_n = \overline{C} \cdot (I_0 \cdot I_1 \cdot I_2 \ldots) \cdot (Q_0 \cdot Q_1 \ldots) \cdot (B_0 \cdot B_1 \cdot \ldots)$
2. ↑ denotes transition from Low to High level.
3. X = Don't care
4. * = Forced at F_n pin for loading the J-K flip-flop in the Input mode. The load control term, L_n must be enabled (HIGH) and the p-terms that are connected to the associated flip-flop must be forced LOW (disabled) during Preload.
5. At P = R = H, Q = H. The final state of Q depends on which is released first.
6. * * = Forced at F_n pin to load J-K flip-flop independent of program code (Diagnostic mode), 3-State B outputs.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS MIN	RATINGS MAX	UNIT
V_{CC}	Supply voltage		+7	V_{DC}
V_{IN}	Input voltage		+5.5	V_{DC}
V_{OUT}	Output voltage		+5.5	V_{DC}
I_{IN}	Input currents	–30	+30	mA
I_{OUT}	Output currents		+100	mA
T_{amb}	Operating temperature range	0	+75	°C
T_{stg}	Storage temperature range	–65	+150	°C

NOTES:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

DC ELECTRICAL CHARACTERISTICS

$0°C \leq T_{amb} \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			MIN	TYP[1]	MAX	
Input voltage[2]						
V_{IH}	High	V_{CC} = MAX	2.0			V
V_{IL}	Low	V_{CC} = MIN			0.8	V
V_{IC}	Clamp	V_{CC} = MIN, I_{IN} = –12mA		–0.8	–1.2	V
Output voltage[2]						
		V_{CC} = MIN				
V_{OH}	High	I_{OH} = –2mA	2.4			V
V_{OL}	Low	I_{OL} = 10mA		0.35	0.5	V
Input current						
I_{IH}	High	V_{IN} = 5.5V		<1	80	µA
I_{IL}	Low	V_{IN} = 0.45V		–10	–100	µA
Output current						
		V_{CC} = MAX				
$I_{O(OFF)}$	Hi-Z state[5, 6]	V_{OUT} = 5.5V		1	80	µA
		V_{OUT} = 0.45V		–1	–140	µA
I_{OS}	Short circuit[3, 7]	V_{OUT} = 0V	–15		–70	mA
I_{CC}	V_{CC} supply current[4]	V_{CC} = MAX		150	190	mA
Capacitance						
		V_{CC} = 5.0V				
C_{IN}	Input	V_{IN} = 2.0V		8		pF
C_{OUT}	Output	V_{OUT} = 2.0V		15		pF

NOTES:
1. All typical values are at V_{CC} = 5V, T_{amb} = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Test one at a time.
4. I_{CC} is measured with the $\overline{OE}$ input grounded, all other inputs at 4.5V and the outputs open.
5. Leakage values are a combination of input and output leakage.
6. Measured with V_{IH} applied to $\overline{OE}$.
7. Duration of short circuit should not exceed 1 second.

Programmable logic sequencer (16 × 45 × 12)

PLS157

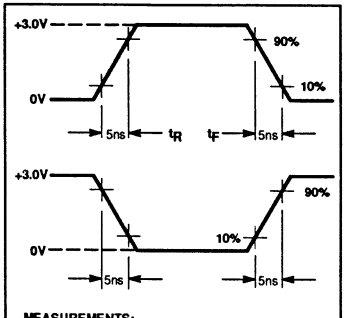
AC ELECTRICAL CHARACTERISTICS

$0°C \le T_{amb} \le +75°C$, $4.75V \le V_{CC} \le 5.25V$, $R_1 = 470\Omega$, $R_2 = 1k\Omega$

SYMBOL	PARAMETER	FROM	TO	TEST CONDITION	LIMITS MIN	LIMITS TYP[1]	LIMITS MAX	UNIT
Pulse width								
t_{CKH}	Clock[2] High	CK +	CK –	C_L = 30pF	25	20		ns
t_{CKL}	Clock Low	CK –	CK +	C_L = 30pF	30	20		ns
t_{CKP}	Period	CK +	CK +	C_L = 30pF	70	50		ns
t_{PRH}	Preset/Reset pulse	(I,B) –	(I,B) +	C_L = 30pF	40	30		ns
Setup time[5]								
t_{IS1}	Input	(I,B) ±	CK +	C_L = 30pF	40	30		ns
t_{IS2}	Input (through F_n)	F ±	CK +	C_L = 30pF	20	10		ns
t_{IS3}	Input (through Complement Array)[4]	(I,B) ±	CK +	C_L = 30pF	65	40		ns
Hold time								
t_{IH1}	Input	(I,B) ±	CK +	C_L = 30pF	0	–10		ns
t_{IH2}	Input	F ±	CK +	C_L = 30pF	15	10		ns
Propagation delays								
t_{CKO}	Clock	CK +	F ±	C_L = 30pF		25	30	ns
t_{OE1}	Output enable[3]	$\overline{OE}$ –	F –	C_L = 30pF		20	30	ns
t_{OD1}	Output disable[3]	$\overline{OE}$ +	F +	C_L = 5pF		20	30	ns
t_{PD}	Output	(I,B) ±	B ±	C_L = 30pF		40	50	ns
t_{OE2}	Output enable[3]	(I,B) +	B ±	C_L = 30pF		35	55	ns
t_{OD2}	Output disable[3]	(I,B) –	B +	C_L = 5pF		30	35	ns
t_{PRO}	Preset/Reset	(I,B) +	F ±	C_L = 30pF		50	55	ns

NOTES:
1. All typical values are at V_{CC} = 5V, T_{amb} = +25°C.
2. To prevent spurious clocking, clock rise time (10% – 90%) ≤ 10ns.
3. For 3-State output; output enable times are tested with C_L = 30pF to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with C_L = 5pF. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} - 0.5V)$ with S_1 open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with S_1 closed.
4. When using the Complement Array t_{CKP} = 95ns (min).
5. Limits are guaranteed with 12 product terms maximum connected to each sum term line.
6. For test circuits, waveforms and timing diagrams see the following pages.

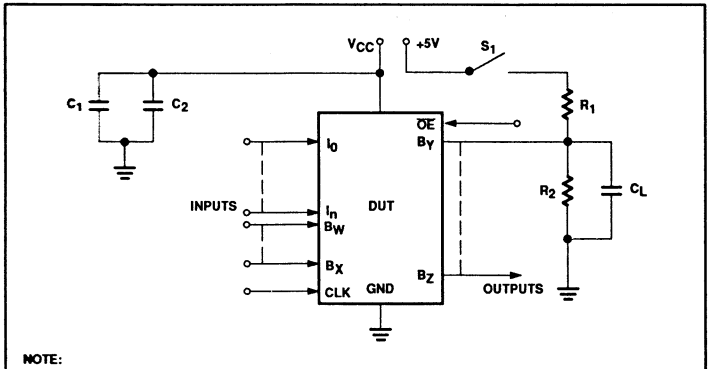
VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

TEST LOAD CIRCUIT

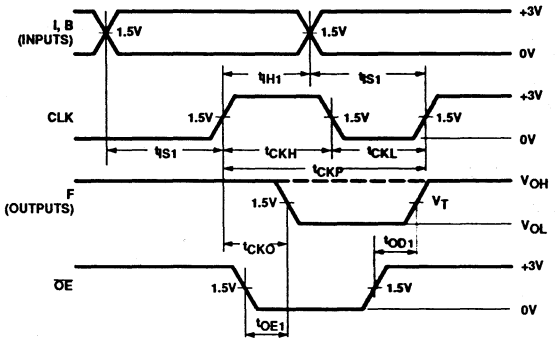


NOTE:
C_1 and C_2 are to bypass V_{CC} to GND.

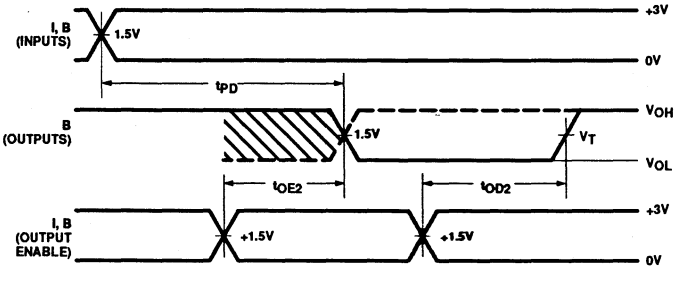
Programmable logic sequencer (16 × 45 × 12)

PLS157

TIMING DIAGRAMS



Flip-Flop Outputs

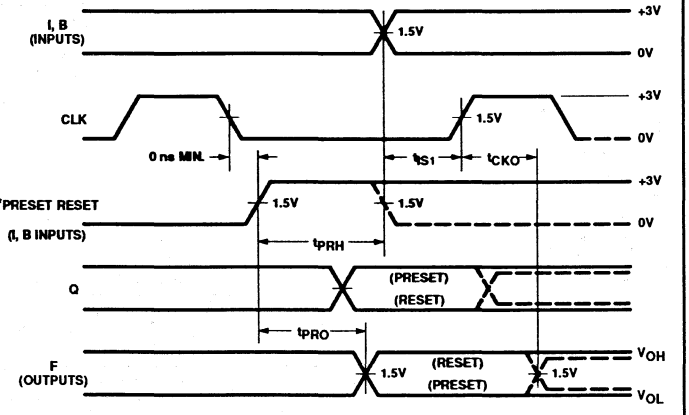


Gate Outputs

TIMING DEFINITIONS

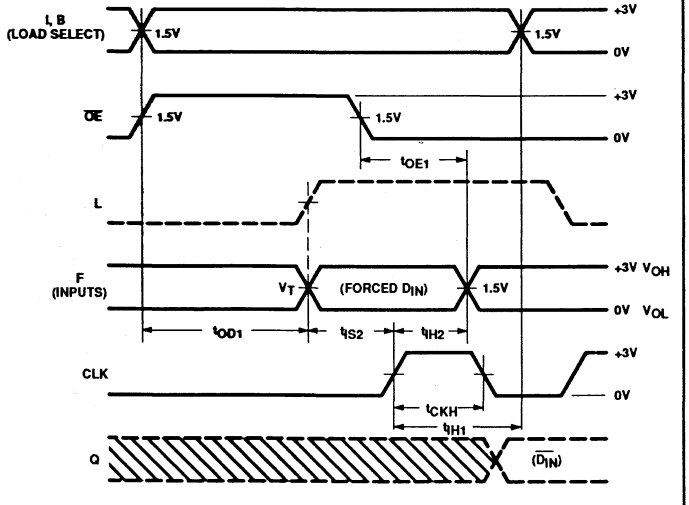
SYMBOL	PARAMETER
t_{CKH}	Width of input clock pulse.
t_{CKL}	Interval between clock pulses.
t_{CKP}	Clock period.
t_{PRH}	Width of preset input pulse.
t_{IS1}	Required delay between beginning of valid input and positive transition of clock.
t_{IS2}	Required delay between beginning of valid input forced at flip-flop output pins, and positive transition of clock.
t_{IH1}	Required delay between positive transition of clock and end of valid input data.
t_{IH2}	Required delay between positive transition of clock and end of valid input data forced at flip-flop output pins.
t_{CKO}	Delay between positive transition of clock and when outputs become valid (with $\overline{OE}$ Low).
t_{OE1}	Delay between beginning of Output Enable Low and when outputs become valid.
t_{OD1}	Delay between beginning of Output Enable High and when outputs are in the OFF-State.
t_{PD}	Propagation delay between combinational inputs and outputs.
t_{OE2}	Delay between predefined Output Enable High, and when combinational outputs become valid.
t_{OD2}	Delay between predefined Output Enable Low and when combinational outputs are in the OFF-State.
t_{PRO}	Delay between positive transition of predefined Preset/Reset input, and when flip-flop outputs become valid.

TIMING DIAGRAMS (Continued)



* The leading edge of preset/reset must occur only when the input clock is "low", and must remain "high" as long as required to override clock. The falling edge of preset/reset can never go "low" when the input clock is "high".

Asynchronous Preset/Reset



Flip-Flop Input Mode

Programmable logic sequencer (16 × 45 × 12)

PLS157

LOGIC PROGRAMMING

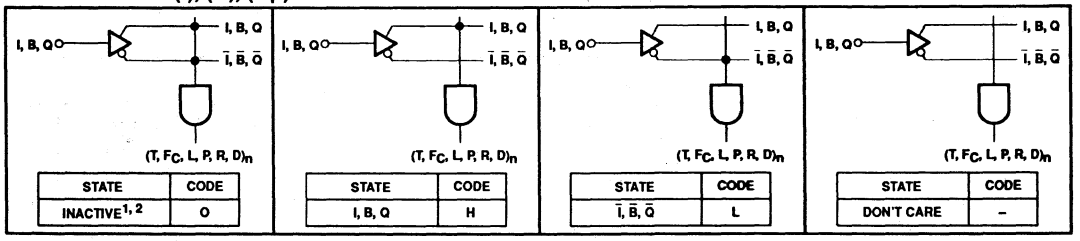
The PLS157 is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Signetics' SNAP and SLICE, Data I/O Corporation's ABEL™ and Logical Devices Inc.'s CUPL™ design software packages.

All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

PLS157 logic designs can also be generated using the program table entry format detailed on the following pages. This program table entry format is supported by the Signetics SNAP and SLICE PLD design software packages (PTP module). SLICE is available free of charge to qualified users.

To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

"AND" ARRAY – (I), (B), (Qp)



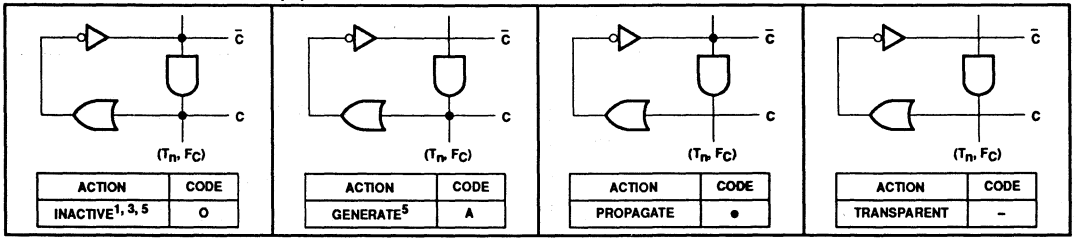
STATE	CODE
INACTIVE[1, 2]	O

STATE	CODE
I, B, Q	H

STATE	CODE
Ī, B̄, Q̄	L

STATE	CODE
DON'T CARE	–

"COMPLEMENT" ARRAY – (C)



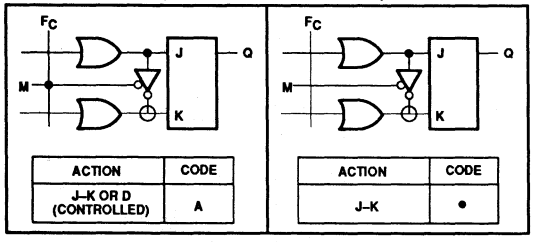
ACTION	CODE
INACTIVE[1, 3, 5]	O

ACTION	CODE
GENERATE[5]	A

ACTION	CODE
PROPAGATE	•

ACTION	CODE
TRANSPARENT	–

"OR" ARRAY – (F-F CONTROL MODE)



ACTION	CODE
J–K OR D (CONTROLLED)	A

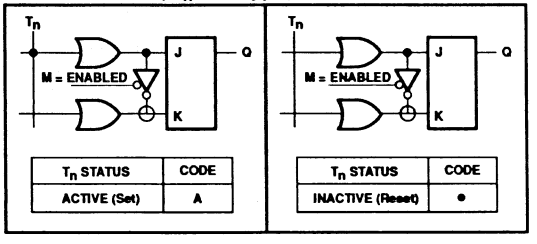
ACTION	CODE
J–K	•

Notes on following page.

ABEL is a trademark of Data I/O Corp.
CUPL is a trademark of Logical Devices, Inc.

Programmable logic sequencer (16 × 45 × 12) — PLS157

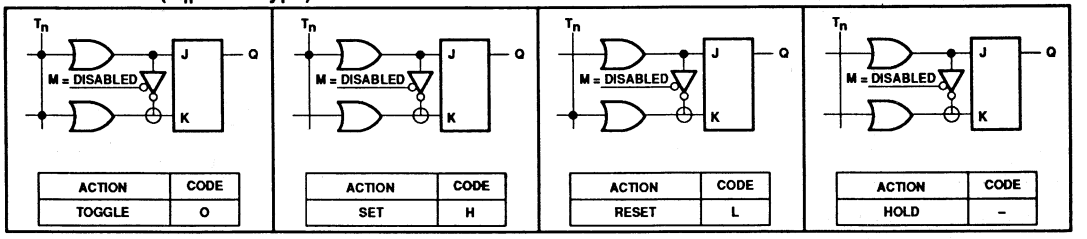
"OR" ARRAY – (Q_n = D-Type)



T_n STATUS	CODE
ACTIVE (Set)	A

T_n STATUS	CODE
INACTIVE (Reset)	•

"OR" ARRAY – (Q_n = J-K Type)



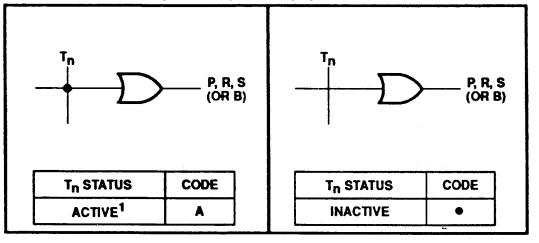
ACTION	CODE
TOGGLE	O

ACTION	CODE
SET	H

ACTION	CODE
RESET	L

ACTION	CODE
HOLD	–

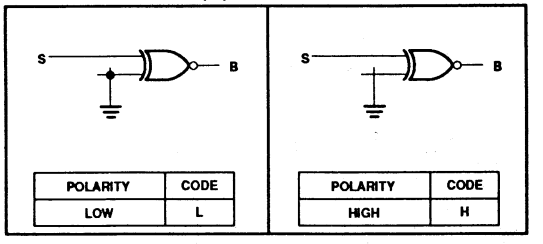
"OR" ARRAY – (S or B), (P), (R)



T_n STATUS	CODE
ACTIVE[1]	A

T_n STATUS	CODE
INACTIVE	•

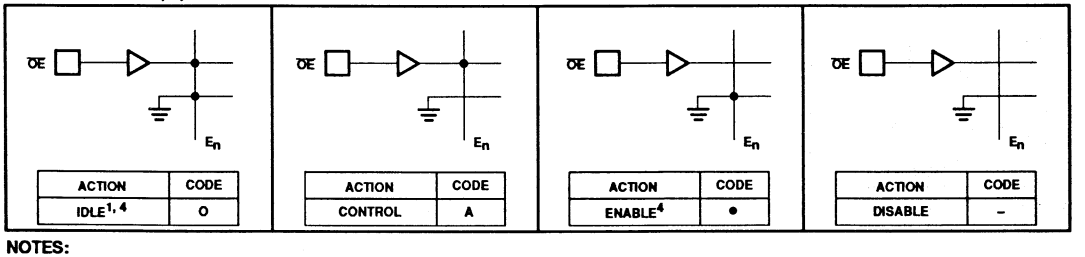
"EX-OR" ARRAY – (B)



POLARITY	CODE
LOW	L

POLARITY	CODE
HIGH	H

"$\overline{OE}$" ARRAY – (E)



ACTION	CODE
IDLE[1, 4]	O

ACTION	CODE
CONTROL	A

ACTION	CODE
ENABLE[4]	•

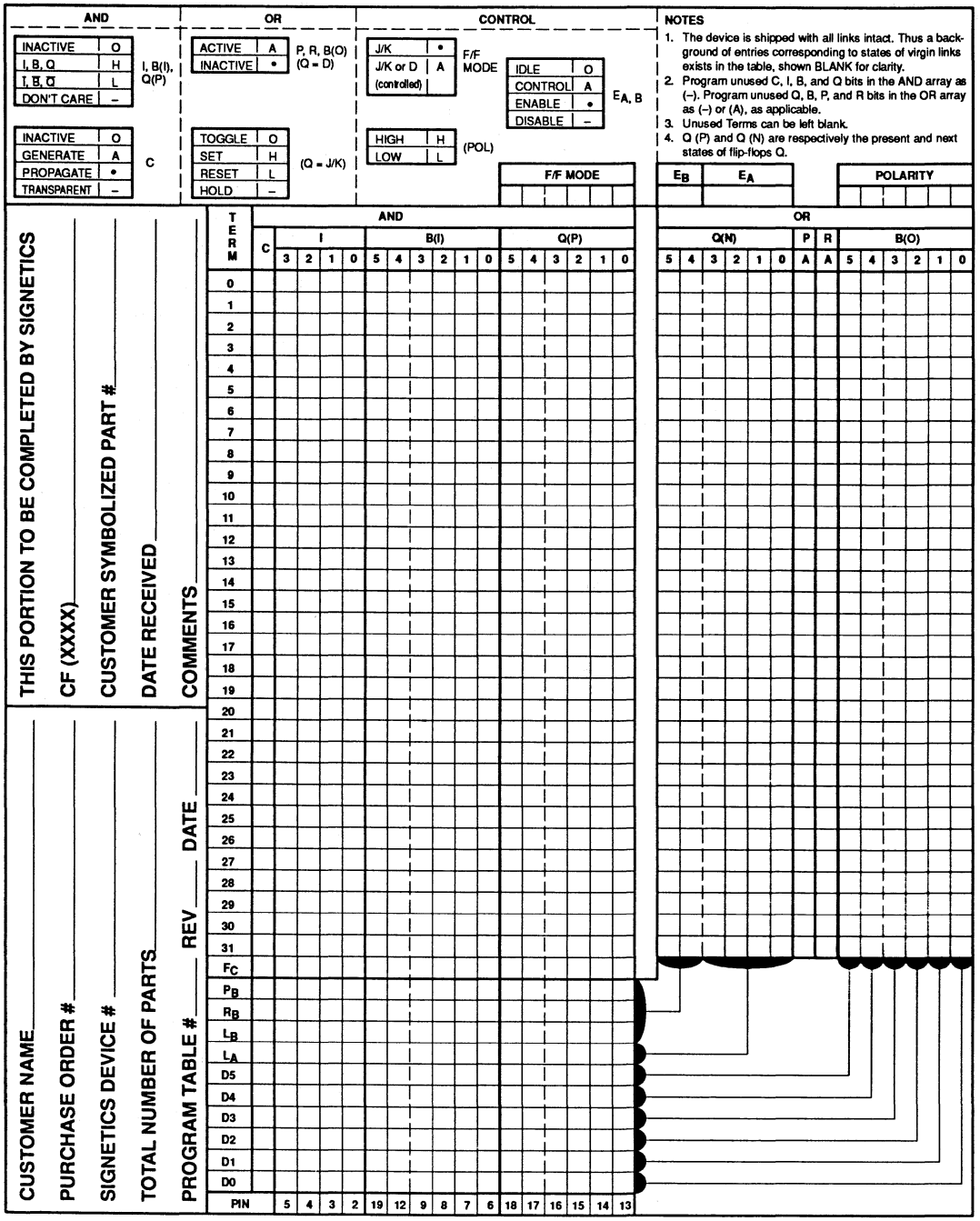
ACTION	CODE
DISABLE	–

NOTES:
1. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates.
2. Any gate $(T, F_C, L, P, R, D)_n$ will be unconditionally inhibited if both of the I, B, or Q links are left intact.
3. To prevent oscillations, this state is not allowed for C link pairs coupled to active gates T_n, F_C.
4. E_n = O and E_n = • are logically equivalent states, since both cause F_n outputs to be unconditionally enabled.
5. These states are not allowed for control gates $(L, P, R, D)_n$ due to their lack of "OR" array links.

Programmable logic sequencer (16 × 45 × 12)

PLS157

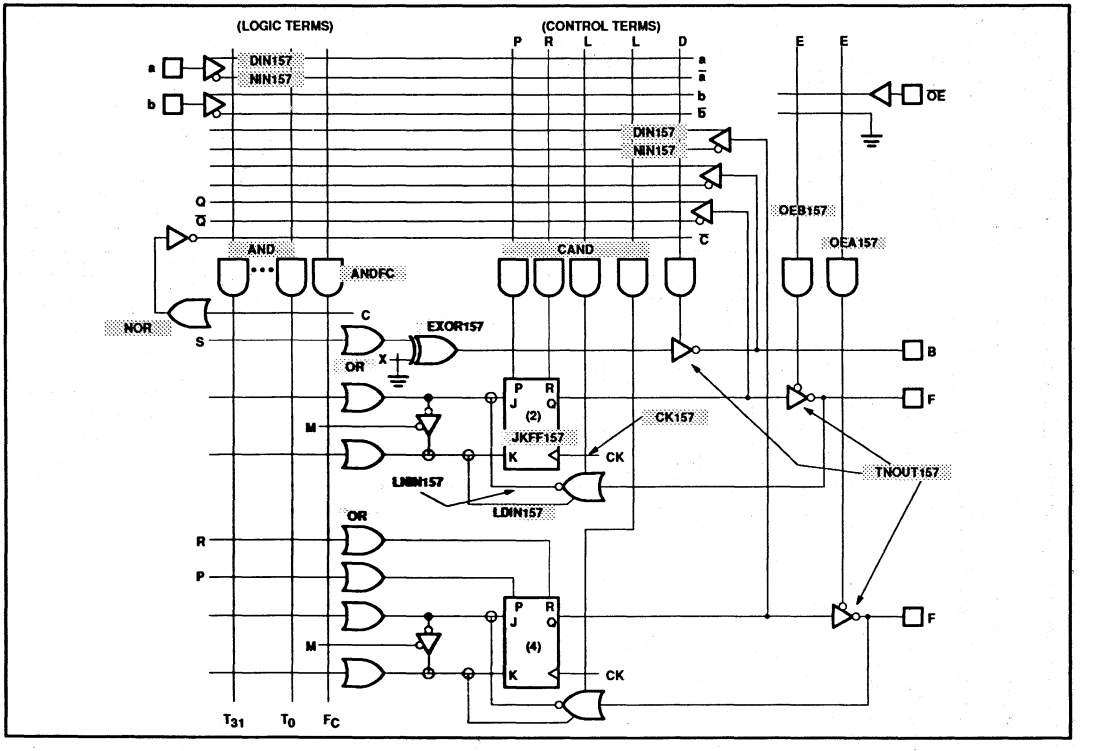
PROGRAM TABLE



Programmable logic sequencer (16 × 45 × 12)

PLS157

SNAP RESOURCE SUMMARY DESIGNATIONS



Programmable logic sequencer (16 × 45 × 12)

PLS159A

DESCRIPTION

The PLS159A is a 3-State output, registered logic element combining AND/OR gate arrays with clocked J-K flip-flops. These J-K flip-flops are dynamically convertible to D-type via a "fold-back" inverting buffer and control gate F_C. It features 8 registered I/O outputs (F) in conjunction with 4 bidirectional I/O lines (B). These yield variable I/O gate and register configurations via control gates (D, L) ranging from 16 inputs to 12 outputs.

The AND/OR arrays consist of 32 logic AND gates, 13 control AND gates, and 21 OR gates with fusible link connections for programming I/O polarity and direction. All AND gates are linked to 4 inputs (I), bidirectional I/O lines (B), internal flip-flop outputs (Q), and Complement Array output ($\overline{C}$). The Complement Array consists of a NOR gate optionally linked to all AND gates for generating and propagating complementary AND terms.

On-chip T/C buffers couple either True (I, B, Q) or Complement ($\overline{I}$, $\overline{B}$, $\overline{Q}$, $\overline{C}$) input polarities to all AND gates, whose outputs can be optionally linked to all OR gates. Any of the 32 AND gates can drive bidirectional I/O lines (B), whose output polarity is individually programmable through a set of Ex-OR gates for implementing AND-OR or AND-NOR logic functions. Similarly, any of the 32 AND gates can drive the J-K inputs of all flip-flops. There are 4 AND gates for the Asynchronous Preset/Reset functions.

All flip-flops are positive edge-triggered and can be used as input, output or I/O (for interfacing with a bidirectional data bus) in conjunction with load control gates (L), steering inputs (I), (B), (Q) and programmable output select lines (E).

The PLS159A is field-programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

FEATURES

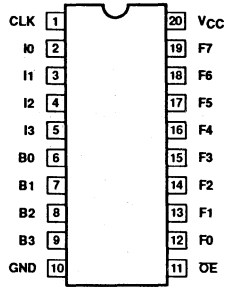
- High-speed version of PLS159
- f_{MAX} = 18MHz
  - 25MHz clock rate
- Field-Programmable (Ni-Cr link)
- 4 dedicated inputs
- 13 control gates
- 32 AND gates
- 21 OR gates
- 45 product terms:
  - 32 logic terms
  - 13 control terms
- 4 bidirectional I/O lines
- 8 bidirectional registers
- J-K, T, or D-type flip-flops
- Power-on reset feature on all flip-flops (F_n = 1)
- Asynchronous Preset/Reset
- Complement Array
- Active-High or -Low outputs
- Programmable $\overline{OE}$ control
- Positive edge-triggered clock
- Input loading: −100µA (max.)
- Power dissipation: 750mW (typ.)
- TTL compatible
- 3-State outputs

APPLICATIONS

- Random sequential logic
- Synchronous up/down counters
- Shift registers
- Bidirectional data buffers
- Timing function generators
- System controllers/synchronizers
- Priority encoder/registers

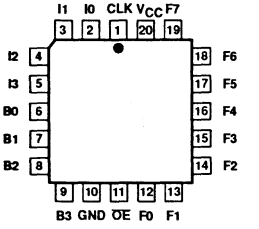
PIN CONFIGURATIONS

N Package



N = Plastic Dual In-Line Package (300mil-wide)

A Package



A = Plastic Leaded Chip Carrier

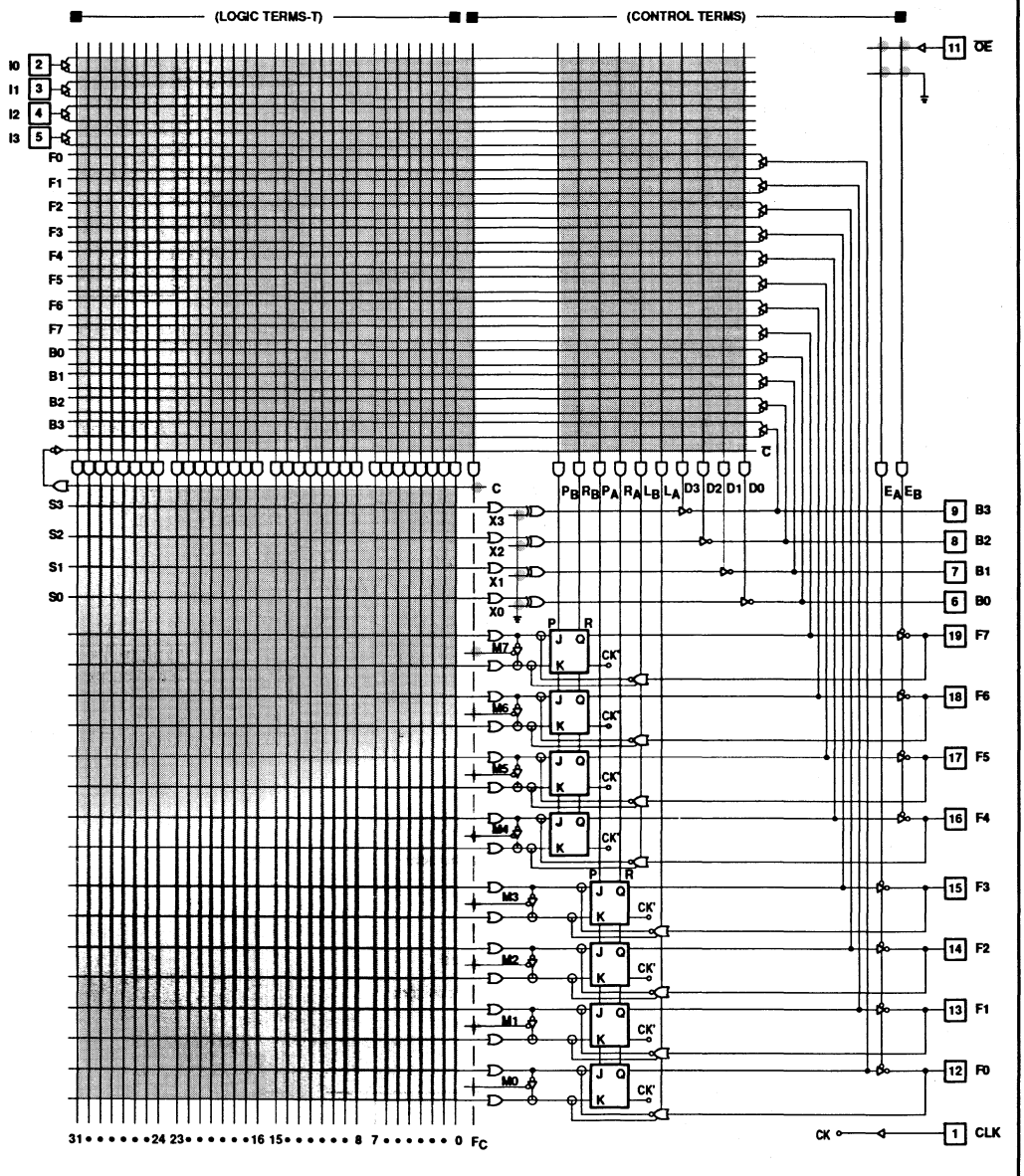
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
20-Pin Plastic Dual In-Line Package (300mil-wide)	PLS159AN
20-Pin Plastic Leaded Chip Carrier	PLS159AA

Programmable logic sequencer (16 × 45 × 12)

PLS159A

LOGIC DIAGRAM

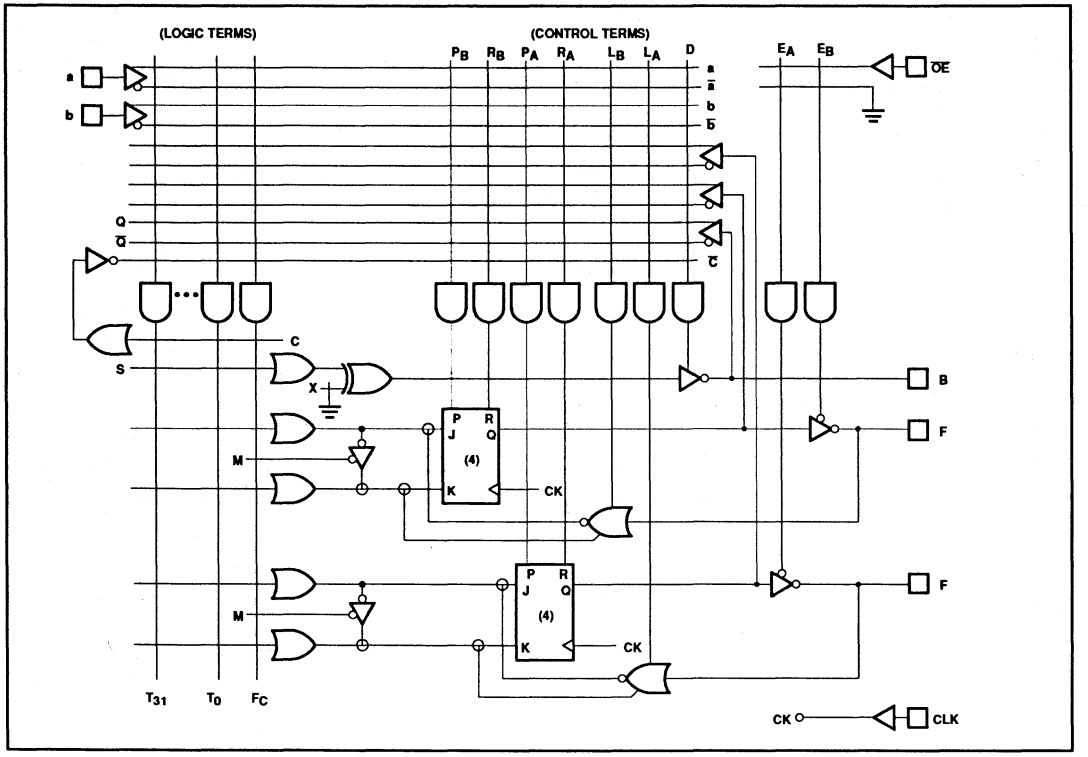


NOTES:
1. All OR gate inputs with a blown link float to logic "0".
2. All other gates and control inputs with a blown link float to logic "1".
3. ⊕ denotes WIRE-OR.
4. Programmable connection.

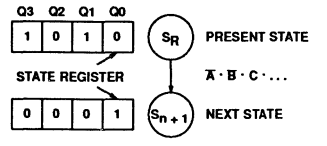
Programmable logic sequencer (16 × 45 × 12)

PLS159A

FUNCTIONAL DIAGRAM



LOGIC FUNCTION



SET Q_0: $J_0 = (Q_3 \cdot \overline{Q}_2 \cdot Q_1 \cdot \overline{Q}_0) \cdot \overline{A} \cdot \overline{B} \cdot C \ldots$
$K_0 = 0$

RESET Q_1: $J_1 = 0$
$K_1 = (Q_3 \cdot \overline{Q}_2 \cdot Q_1 \cdot \overline{Q}_0) \cdot \overline{A} \cdot \overline{B} \cdot C \ldots$

HOLD Q_2: $J_2 = 0$
$K_2 = 0$

TOGGLE Q_3: $J_3 = (Q_3 \cdot \overline{Q}_2 \cdot Q_1 \cdot \overline{Q}_0) \cdot \overline{A} \cdot \overline{B} \cdot C \ldots$
$K_3 = (Q_3 \cdot \overline{Q}_2 \cdot Q_1 \cdot \overline{Q}_0) \cdot \overline{A} \cdot \overline{B} \cdot C \ldots$

NOTE:
Similar logic functions are applicable for D and T mode flip-flops.

FLIP-FLOP TRUTH TABLE

$\overline{OE}$	L	CK	P	R	J	K	Q	F
H								Hi-Z
L	X	X	L	X	X	X	L	H
L	X	X	H	L	X	X	H	L
L	X	X	L	H	X	X	L	H
L	L	↑	L	L	L	L	Q	$\overline{Q}$
L	L	↑	L	L	L	H	L	H
L	L	↑	L	L	H	L	H	L
L	L	↑	L	L	H	H	$\overline{Q}$	Q
H	H	↑	L	L	L	H	L	H*
H	H	↑	L	L	H	L	H	L*
+10V	X	↑	X	X	L	H	L	H* *
	X	↑	X	X	H	L	H	L* *

NOTES:
1. Positive Logic:
   $J\text{-}K = T_0 + T_1 + T_2 \ldots\ldots\ldots\ldots T_{31}$
   $T_n = C \cdot (I0 \cdot I1 \cdot I2 \ldots) \cdot (Q_0 \cdot Q_1 \ldots) \cdot (B0 \cdot B1 \cdot \ldots)$
2. ↑ denotes transition from Low to High level.
3. X = Don't care
4. * = Forced at F_n pin for loading the J-K flip-flop in the Input mode. The load control term, L_n must be enabled (HIGH) and the p-terms that are connected to the associated flip-flop must be forced LOW (disabled) during Preload.
5. At P = R = H, Q = H. The final state of Q depends on which is released first.
6. * * = Forced at F_n pin to load J-K flip-flop independent of program code (Diagnostic mode), 3-State B outputs.

Programmable logic sequencer (16 × 45 × 12)

PLS159A

VIRGIN STATE

The factory shipped virgin device contains all fusible links intact, such that:

1. $\overline{OE}$ is always enabled.
2. Preset and Reset are always disabled.
3. All transition terms are disabled.
4. All flip-flops are in D-mode unless otherwise programmed to J-K only or J-K or D (controlled).
5. All B pins are inputs and all F pins are outputs unless otherwise programmed.

CAUTION: PLS159A PROGRAMMING ALGORITHM

The programming voltage required to program the PLS159A is higher (17.5V) than that required to program the PLS159 (14.5V). Consequently, the PLS159 programming algorithm will not program the PLS159A. Please exercise caution when accessing programmer device codes to insure that the correct algorithm is used.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS MIN	RATINGS MAX	UNIT
V_{CC}	Supply voltage		+7	V_{DC}
V_{IN}	Input voltage		+5.5	V_{DC}
V_{OUT}	Output voltage		+5.5	V_{DC}
I_{IN}	Input currents	–30	+30	mA
I_{OUT}	Output currents		+100	mA
T_{amb}	Operating temperature range	0	+75	°C
T_{stg}	Storage temperature range	–65	+150	°C

NOTES:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

Programmable logic sequencer (16 × 45 × 12)

PLS159A

DC ELECTRICAL CHARACTERISTICS

$0°C \le T_{amb} \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			MIN	TYP[1]	MAX	
Input voltage[2]						
V_{IH}	High	V_{CC} = MAX	2.0			V
V_{IL}	Low	V_{CC} = MIN			0.8	V
V_{IC}	Clamp	V_{CC} = MIN, I_{IN} = −12mA		−0.8	−1.2	V
Output voltage[2]						
V_{OH}	High	V_{CC} = MIN, I_{OH} = −2mA	2.4			V
V_{OL}	Low	I_{OL} = 10mA		0.35	0.5	V
Input current						
I_{IH}	High	V_{CC} = MAX, V_{IN} = 5.5V		<1	80	µA
I_{IL}	Low	V_{IN} = 0.45V		−10	−100	µA
Output current						
$I_{O(OFF)}$	Hi-Z state[4, 7]	V_{CC} = MAX, V_{OUT} = 5.5V		1	80	µA
		V_{OUT} = 0.45V		−1	−140	µA
I_{OS}	Short circuit[3, 5]	V_{OUT} = 0V	−15		−70	mA
I_{CC}	V_{CC} supply current[6]	V_{CC} = MAX		150	190	mA
Capacitance						
C_{IN}	Input	V_{CC} = 5.0V, V_{IN} = 2.0V		8		pF
C_{OUT}	Output	V_{OUT} = 2.0V		15		pF

NOTES:
1. All typical values are at V_{CC} = 5V, T_{amb} = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Test one at a time.
4. Measured with V_{IH} applied to $\overline{OE}$.
5. Duration of short circuit should not exceed 1 second.
6. I_{CC} is measured with the $\overline{OE}$ input grounded, all other inputs at 4.5V and the outputs open.
7. Leakage values are a combination of input and output leakage.

Programmable logic sequencer (16 × 45 × 12)

PLS159A

AC ELECTRICAL CHARACTERISTICS

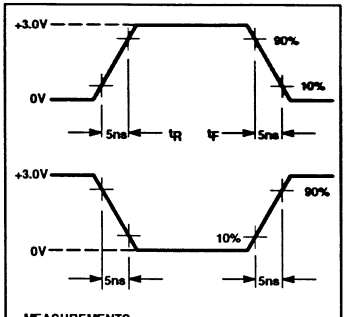
$0°C \le T_{amb} \le +75°C$, $4.75V \le V_{CC} \le 5.25V$, $R_1 = 470\Omega$, $R_2 = 1k\Omega$

SYMBOL	PARAMETER	FROM	TO	TEST CONDITION	LIMITS MIN	LIMITS TYP[1]	LIMITS MAX	UNIT
Pulse width								
t_{CKH}	Clock[2] High	CK +	CK –	C_L = 30pF	20	15		ns
t_{CKL}	Clock Low	CK –	CK +	C_L = 30pF	20	15		ns
t_{CKP}	Period	CK +	CK +	C_L = 30pF	55	45		ns
t_{PRH}	Preset/Reset pulse	(I,B) –	(I,B) +	C_L = 30pF	35	30		ns
Setup time[5]								
t_{IS1}	Input	(I,B) ±	CK +	C_L = 30pF	35	30		ns
t_{IS2}	Input (through F_n)	F ±	CK +	C_L = 30pF	15	10		ns
t_{IS3}	Input (through Complement Array)[4]	(I,B) ±	CK +	C_L = 30pF	55	45		ns
Hold time								
t_{IH1}	Input	(I,B) ±	CK +	C_L = 30pF	0	–5		ns
t_{IH2}	Input (through F_n)	F ±	CK +	C_L = 30pF	15	10		ns
Propagation delay								
t_{CKO}	Clock	CK +	F ±	C_L = 30pF		15	20	ns
t_{OE1}	Output enable[3]	$\overline{OE}$ –	F –	C_L = 30pF		20	30	ns
t_{OD1}	Output disable[3]	$\overline{OE}$ +	F +	C_L = 5pF		20	30	ns
t_{PD}	Output	(I,B) ±	B ±	C_L = 30pF		25	35	ns
t_{OE2}	Output enable[3]	(I,B) +	B ±	C_L = 30pF		20	30	ns
t_{OD2}	Output disable[3]	(I,B) –	B +	C_L = 5pF		20	30	ns
t_{PRO}	Preset/Reset	(I,B) +	F ±	C_L = 30pF		35	45	ns
t_{PPR}	Power-on/preset	V_{CC} +	F –	C_L = 30pF		0	10	ns

NOTES:

1. All typical values are at V_{CC} = 5V, T_{amb} = +25°C.
2. To prevent spurious clocking, clock rise time (10% – 90%) ≤ 10ns.
3. For 3-State output; output enable times are tested with C_L = 30pF to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with C_L = 5pF. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} - 0.5V)$ with S_1 open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with S_1 closed.
4. When using the Complement Array t_{CKP} = 75ns (min).
5. Limits are guaranteed with 12 product terms maximum connected to each sum term line.

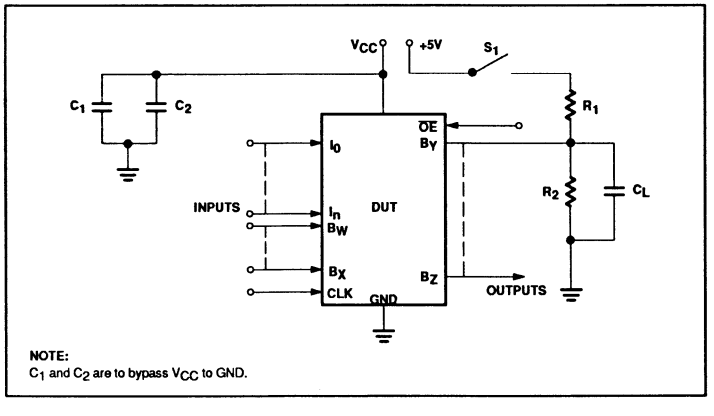
VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

TEST LOAD CIRCUIT

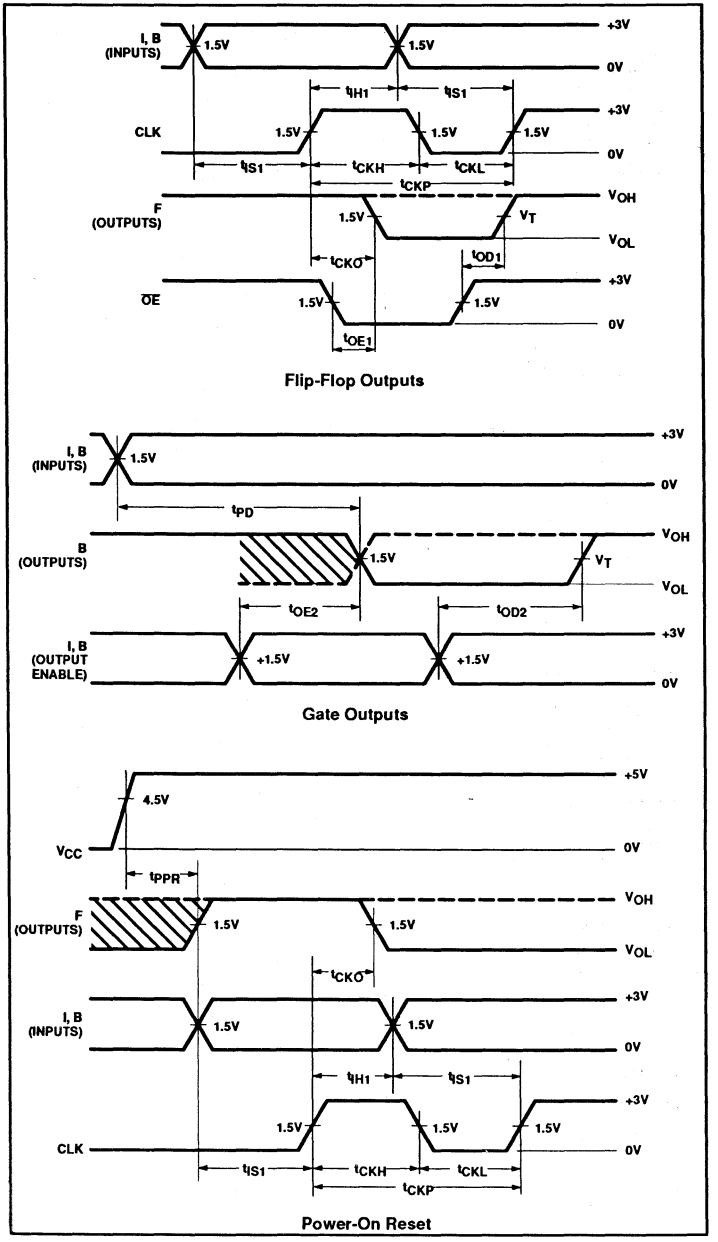


NOTE:
C_1 and C_2 are to bypass V_{CC} to GND.

Programmable logic sequencer (16 × 45 × 12)

PLS159A

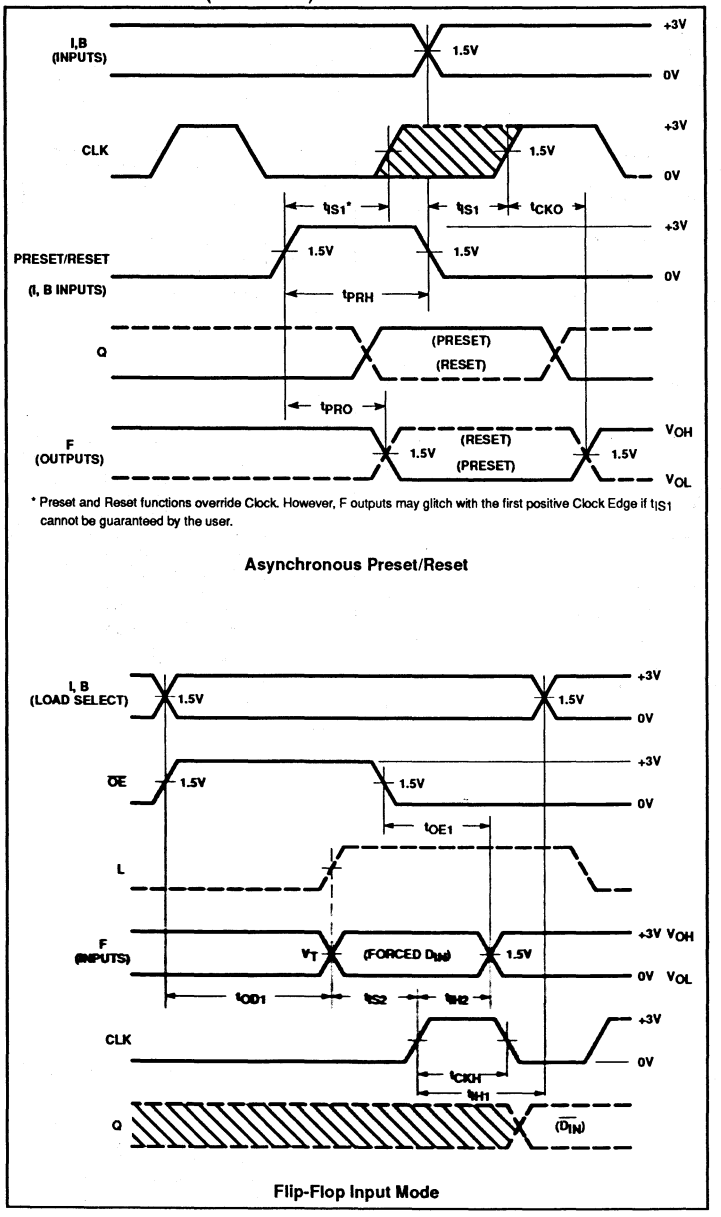
TIMING DIAGRAMS



TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{CKH}	Width of input clock pulse.
t_{CKL}	Interval between clock pulses.
t_{CKP}	Clock period.
t_{PRH}	Width of preset input pulse.
t_{IS1}	Required delay between beginning of valid input and positive transition of clock.
t_{IS2}	Required delay between beginning of valid input forced at flip-flop output pins, and positive transition of clock.
t_{IH1}	Required delay between positive transition of clock and end of valid input data.
t_{IH2}	Required delay between positive transition of clock and end of valid input data forced at flip-flop output pins.
t_{CKO}	Delay between positive transition of clock and when outputs become valid (with $\overline{OE}$ Low).
t_{OE1}	Delay between beginning of Output Enable Low and when outputs become valid.
t_{OD1}	Delay between beginning of Output Enable High and when outputs are in the OFF-State.
t_{PPR}	Delay between V_{CC} (after power-on) and when flip-flop outputs become preset at "1" (internal Q outputs at "0").
t_{PD}	Propagation delay between combinational inputs and outputs.
t_{OE2}	Delay between predefined Output Enable High, and when combinational outputs become valid.
t_{OD2}	Delay between predefined Output Enable Low and when combinational outputs are in the OFF-State.
t_{PRO}	Delay between positive transition of predefined Preset/Reset input, and when flip-flop outputs become valid.

TIMING DIAGRAMS (Continued)



Programmable logic sequencer (16 × 45 × 12)

PLS159A

LOGIC PROGRAMMING

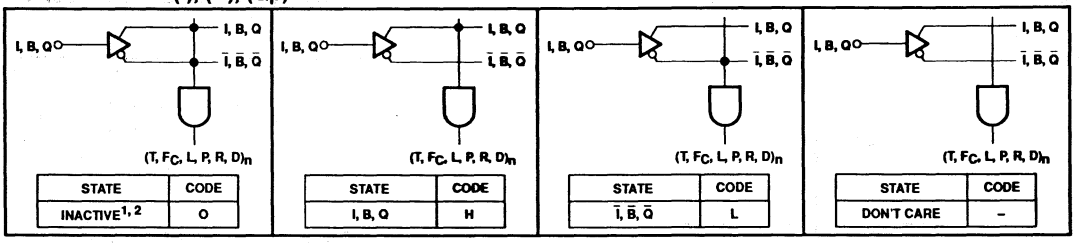
The PLS159A is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Signetics' SNAP and SLICE, Data I/O Corporation's ABEL™, and Logical Devices Inc.'s CUPL™ design software packages.

All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

PLS159A logic designs can also be generated using the program table entry format detailed on the following pages. This program table entry format is supported by the Signetics SNAP and SLICE PLD design software packages (PTP module). SLICE is available free of charge to qualified users.

To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

"AND" ARRAY – (I), (B), (Qp)



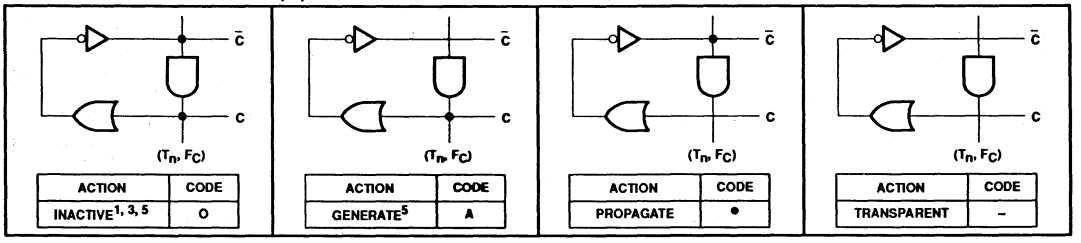
STATE	CODE
INACTIVE[1, 2]	O

STATE	CODE
I, B, Q	H

STATE	CODE
Ī, B̄, Q̄	L

STATE	CODE
DON'T CARE	–

"COMPLEMENT" ARRAY – (C)



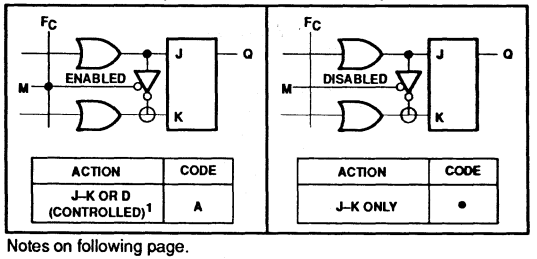
ACTION	CODE
INACTIVE[1, 3, 5]	O

ACTION	CODE
GENERATE[5]	A

ACTION	CODE
PROPAGATE	•

ACTION	CODE
TRANSPARENT	–

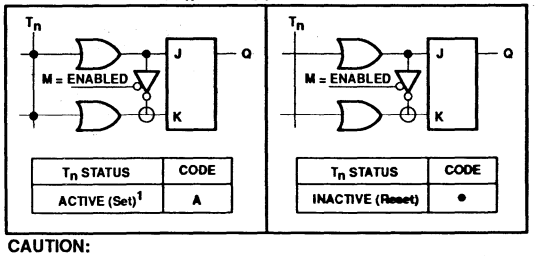
"OR" ARRAY – (F-F CONTROL MODE)



ACTION	CODE
J-K OR D (CONTROLLED)[1]	A

ACTION	CODE
J-K ONLY	•

"OR" ARRAY – (Q_n = D-Type)



Tn STATUS	CODE
ACTIVE (Set)[1]	A

Tn STATUS	CODE
INACTIVE (Reset)	•

Notes on following page.

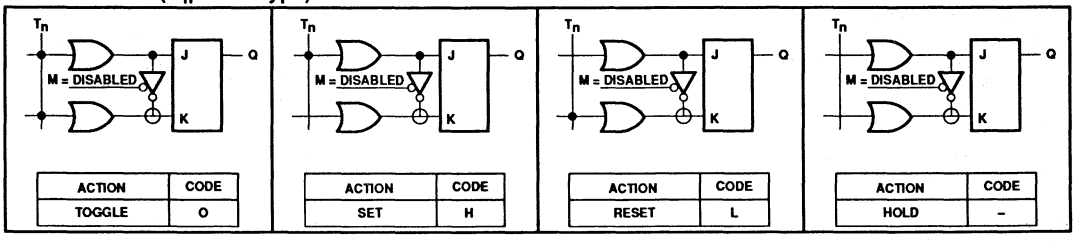
CAUTION:
THE PLS159A Programming Algorithm is different from the PLS159.

ABEL is a trademark of Data I/O Corp.
CUPL is a trademark of Logical Devices, Inc.

Programmable logic sequencer (16 × 45 × 12)

PLS159A

"OR" ARRAY – (Q_n = J-K Type)



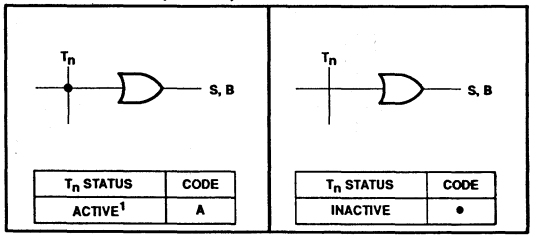
ACTION	CODE
TOGGLE	O

ACTION	CODE
SET	H

ACTION	CODE
RESET	L

ACTION	CODE
HOLD	-

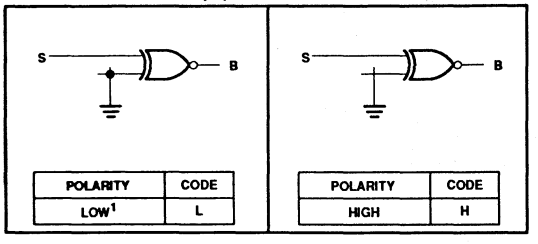
"OR" ARRAY – (S or B)



T_n STATUS	CODE
ACTIVE[1]	A

T_n STATUS	CODE
INACTIVE	•

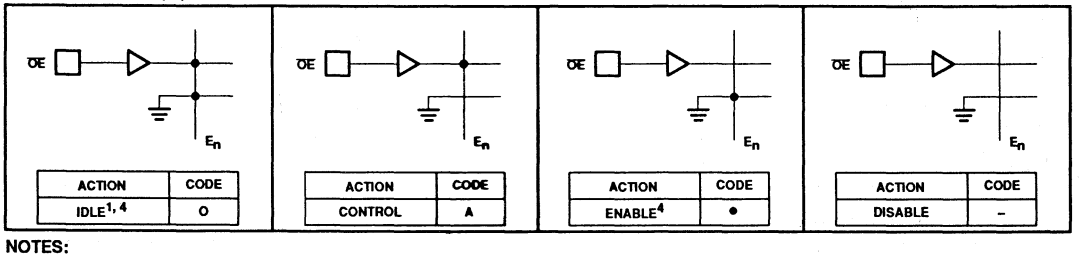
"EX-OR" ARRAY – (B)



POLARITY	CODE
LOW[1]	L

POLARITY	CODE
HIGH	H

"$\overline{OE}$" ARRAY – (E)



ACTION	CODE
IDLE[1,4]	O

ACTION	CODE
CONTROL	A

ACTION	CODE
ENABLE[4]	•

ACTION	CODE
DISABLE	-

NOTES:
1. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates.
2. Any gate (T, F_C, L, P, R, D)$_n$ will be unconditionally inhibited if both of the I, B, or Q links are left intact.
3. To prevent oscillations, this state is not allowed for C link pairs coupled to active gates T_n, F_C.
4. E_n = O and E_n = • are logically equivalent states, since both cause F_n outputs to be unconditionally enabled.
5. These states are not allowed for control gates (L, P, R, D)$_n$ due to their lack of "OR" array links.

Programmable logic sequencer (16 × 45 × 12)

PLS159A

FPLS PROGRAM TABLE

AND

INACTIVE	O
I, B, Q	H
$\overline{I}$, $\overline{B}$, $\overline{Q}$	L
DON'T CARE	–

I, B(I), Q(P)

INACTIVE	O
GENERATE	A
PROPAGATE	•
TRANSPARENT	–

C

OR

ACTIVE	A
INACTIVE	•

P, R, B(O) (Q = D)

TOGGLE	O
SET	H
RESET	L
HOLD	–

(Q = J/K)

CONTROL

J/K	•
J/K or D (controlled)	A

F/F MODE

IDLE	O
CONTROL	A
ENABLE	•
DISABLE	–

$E_{A, B}$

HIGH	H
LOW	L

(POL)

NOTES

1. The device is shipped with all links intact. Thus a background of entries corresponding to states of virgin links exists in the table, shown BLANK for clarity.
2. Program unused C, I, B, and Q bits in the AND array as (–). Program unused Q, B, P, and R bits in the OR array as (–) or (A), as applicable.
3. Unused Terms can be left blank.
4. Q (P) and Q (N) are respectively the present and next states of flip-flops Q.

THIS PORTION TO BE COMPLETED BY SIGNETICS

CF (XXXX)_____

CUSTOMER SYMBOLIZED PART #_____

DATE RECEIVED_____

COMMENTS_____

CUSTOMER NAME_____

PURCHASE ORDER #_____

SIGNETICS DEVICE #_____

TOTAL NUMBER OF PARTS_____

PROGRAM TABLE #_____ REV____ DATE_____

TERM	F/F MODE	E_B	E_A	POLARITY	C	AND: I 3 2 1 0	AND: B(I) 3 2 1 0	AND: Q(P) 7 6 5 4 3 2 1 0	(OR): Q(N) 7 6 5 4 3 2 1 0	(OR): B(O) 3 2 1 0
0										
1										
2										
3										
4										
5										
6										
7										
8										
9										
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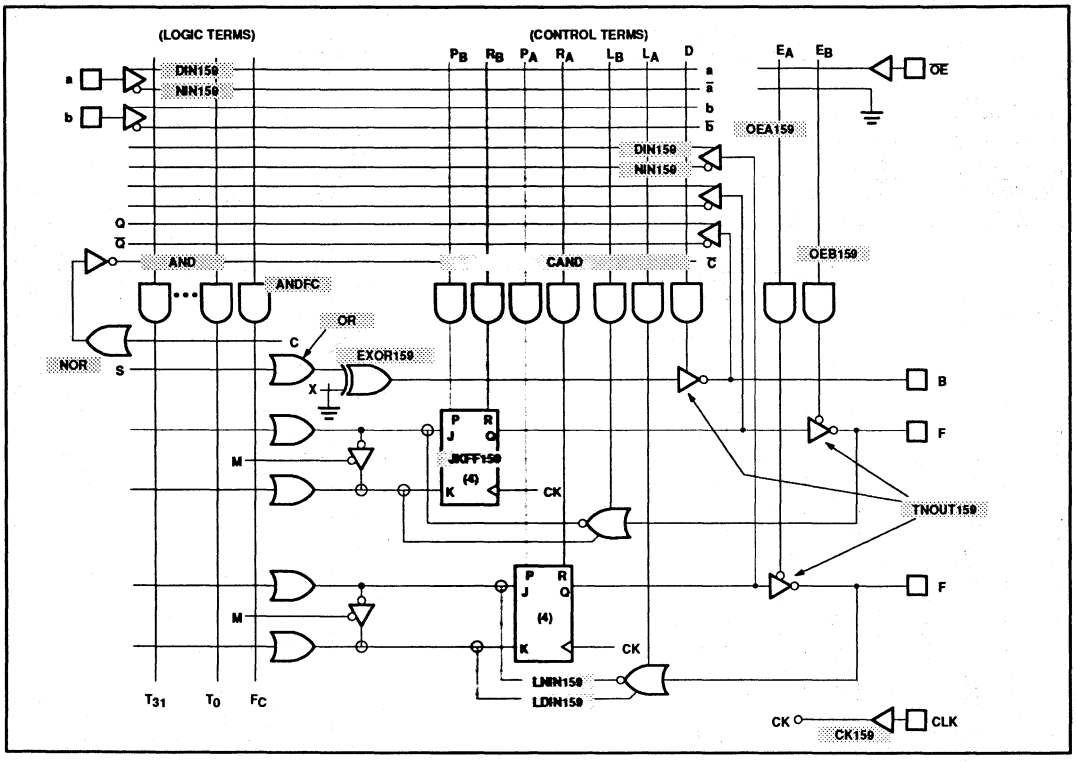
29										
30										
31										
F_C										
P_B										
R_B										
L_B										
P_A										
R_A										
L_A										
D3										
D2										
D1										
D0										
PIN						5 4 3 2	9 8 7 6	19 18 17 16 15 14 13 12		

Programmable logic sequencer (16 × 45 × 12)

PLS159A

SNAP RESOURCE SUMMARY DESIGNATIONS



Programmable logic sequencers (14 × 48 × 6)

PLS167/A

DESCRIPTION

The PLS167 and PLS167A are bipolar, Programmable Logic State machines of the Mealy type. The Programmable Logic Sequencers (PLS) contain logic AND/OR gate arrays with user programmable connections which control the inputs of on-chip State and Output Registers. These consist respectively of 8 Q_P, and 4 Q_F edge-triggered, clocked S/R flip-flops, with an asynchronous Preset Option.

All flip-flops are unconditionally preset to "1" during power turn-on.

The AND array combines 14 external inputs, I0-13, with 8 internal inputs, P0-7, fed back from the State Register to form up to 48 transition terms (AND terms). In addition, P0 and P1 of the internal State Register are brought off-chip to allow extending the Output Register to 6 bits, if so desired.

All transition terms can include True, False, or Don't Care states of the controlling variables, and are merged in the OR array to issue next-state and next-output commands to their respective registers on the Low-to-High transition of the Clock pulse.

Both True and Complement transition terms can be generated by optional use of the internal variable (C) from the Complement Array. Also, if desired, the Preset input can be converted to output-enable function, as an additional user programmable option.

Order codes are listed in the Ordering Information Table.

FEATURES

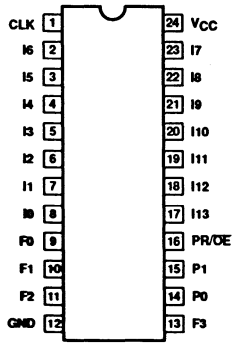
- PLS167
  - f_{MAX} = 13.9MHz
  - 20MHz clock rate
- PLS167A
  - f_{MAX} = 20MHz
  - 25MHz clock rate
- Field-Programmable (Ni-Cr link)
- 14 True/Complement buffered inputs
- 48 programmable AND gates
- 25 programmable OR gates
- 8-bit State Register
- 2-bit shared State/Output Register
- 4-bit Output Register
- Transition Complement Array
- Programmable Asynchronous Preset/Output Enable
- Positive edge-triggered clock
- Power-on preset to logic "1" of all registers
- Automatic logic "HOLD" state via S/R flip-flops
- On-chip Test Array
- Power: 600mW (typ.)
- TTL compatible
- 3-State outputs
- Single +5V supply

APPLICATIONS

- Interface protocols
- Sequence detectors
- Peripheral controllers
- Timing generators
- Sequential circuits
- Security locking systems

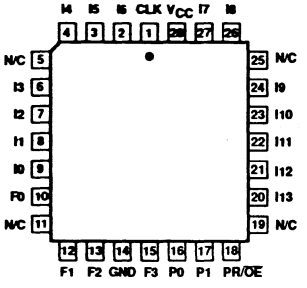
PIN CONFIGURATIONS

N Package



N = Plastic Dual In-Line Package (300mil-wide)

A Package



A = Plastic Leaded Chip Carrier

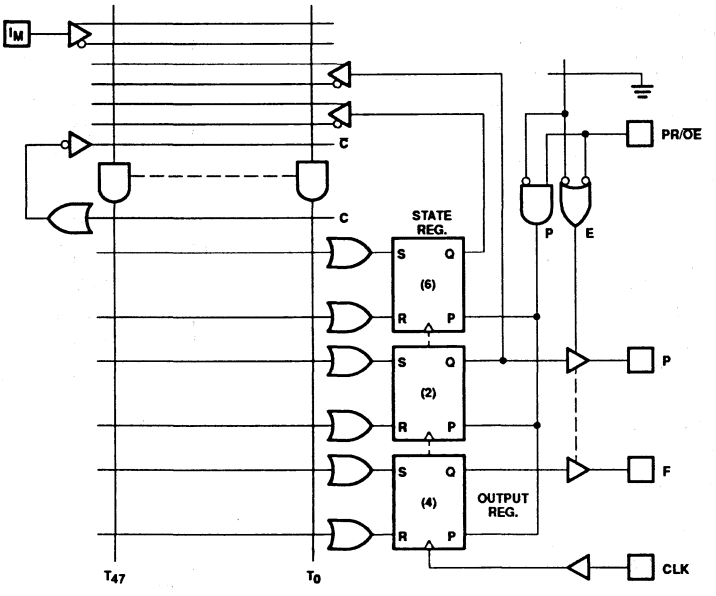
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-Pin Plastic Dual In-Line Package (300mil-wide)	PLS167N, PLS167AN
28-Pin Plastic Leaded Chip Carrier	PLS167A, PLS167AA

Programmable logic sequencers (14 × 48 × 6)

PLS167/A

FUNCTIONAL DIAGRAM



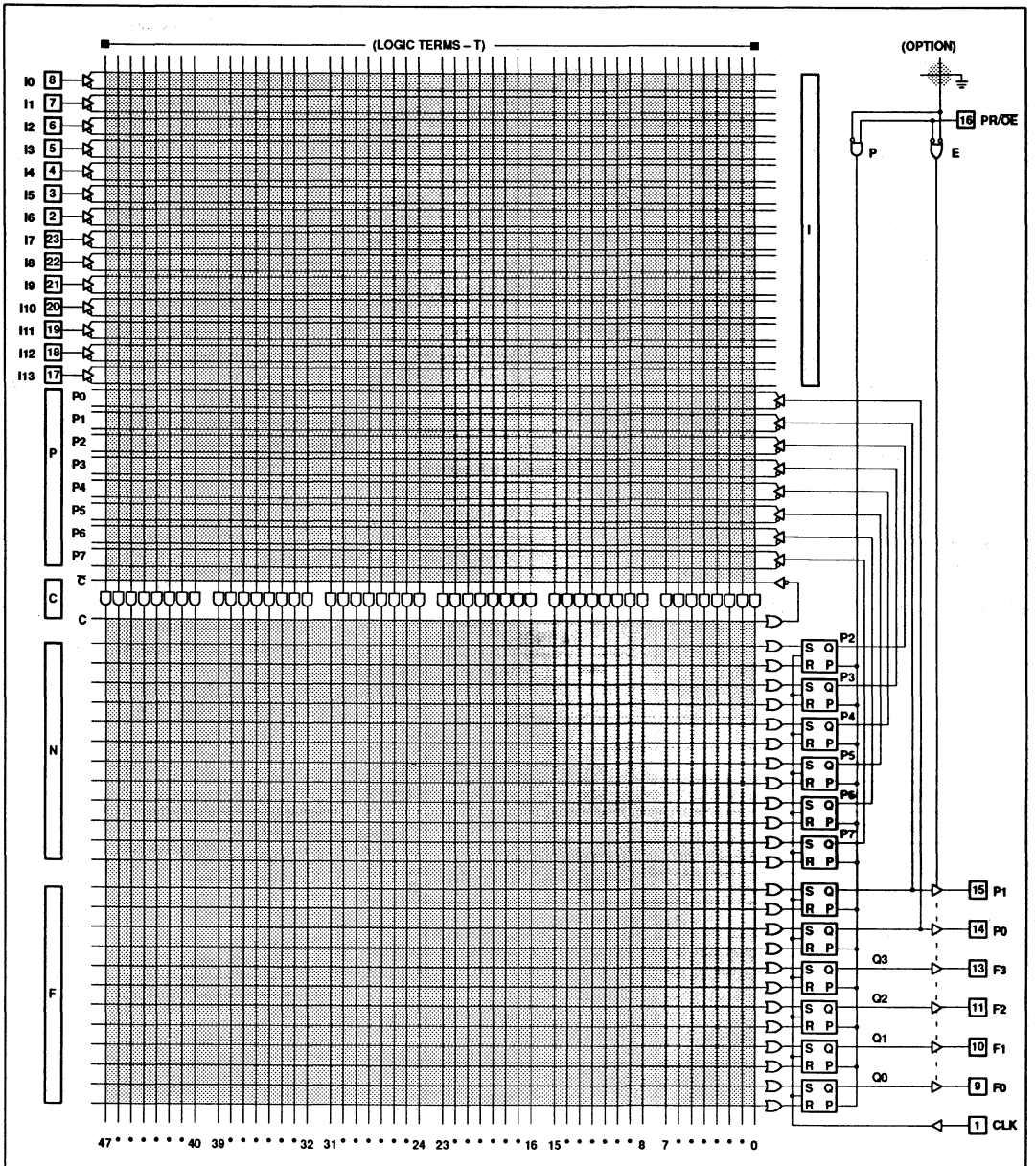
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION	POLARITY
1	CLK	**Clock:** The Clock input to the State and Output Registers. A Low-to-High transition on this line is necessary to update the contents of both registers.	Active-High
2 – 7 17 – 23	I1 – I13	**Logic Inputs:** The 13 external inputs to the AND array used to program jump conditions between machine states, as determined by a given logic sequence.	Active-High/Low
8	I0	**Logic/Diagnostic Input:** A 14th external logic input to the AND array, as above, when exercised with standard TTL levels. When I0 is held at +10V, device outputs F0 – 3 and P0 – 1 reflect the contents of State Register bits P2 – 7 (see Diagnostic Output Mode diagram). The contents of flip-flops P0 – 1 and F0 – 3 remain unaltered.	Active-High/Low
9 – 11 13	F0 – 3	**Logic/Diagnostic Outputs:** Four device outputs which normally reflect the contents of Output Register bits Q_{0-3}, when enabled. When I0 is held at +10V, F0 – 3 = (P2 – 5).	Active-High
14 – 15	P0 – 1	**Logic/Diagnostic Outputs:** Two register bits with shared function as least Significant State Register bits, or most significant Output Register bits. When I_0 is held at +10V, P0 – 1 = (P6 – 7).	Active-High
16	PR/$\overline{OE}$	**Preset or $\overline{\text{Output Enable}}$ Input:** A user programmable function:	
		• **Preset:** Provides an Asynchronous Preset to logic "1" of all State and Output Register bits. Preset overrides Clock, and when held High, clocking is inhibited and P0 – 7 and F0 – 3 are High. Normal clocking resumes with the first full clock pulse following a High-to-Low clock transition, after Preset goes Low.	Active-High (H)
		• **$\overline{\text{Output Enable}}$:** Provides an Output Enable function to all output buffers.	Active-Low (L)

Programmable logic sequencers (14 × 48 × 6)

PLS167/A

LOGIC DIAGRAM



NOTES:
1. All AND gate inputs with a blown link float to a logic "1".
2. All OR gate inputs with a blown fuse float to logic "0".
3. ▒ Programmable connection.

Programmable logic sequencers (14 × 48 × 6)

PLS167/A

TRUTH TABLE [1, 2, 3, 4, 5, 6]

V_{CC}	OPTION PR	OPTION $\overline{OE}$	I_0	CK	S	R	$Q_{P/F}$	F
	H		*	X	X	X	H	H
	L		+10V	X	X	X	Q_n	$(Q_P)_n$
	L		X	X	X	X	Q_n	$(Q_F)_n$
		H	*	X	X	X	Q_n	Hi-Z
+5V		L	+10V	X	X	X	Q_n	$(Q_P)_n$
		L	X	X	X	X	Q_n	$(Q_F)_n$
		L	X	↑	L	L	Q_n	$(Q_F)_n$
		L	X	↑	L	H	L	L
		L	X	↑	H	L	H	H
		L	X	↑	H	H	IND.	IND.
↑	X	X	X	X	X	X	H	

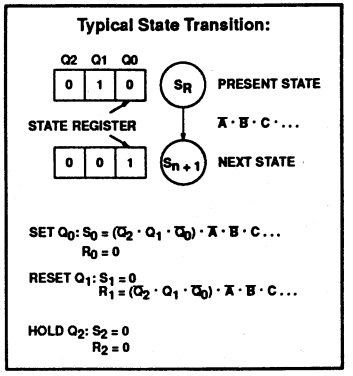
NOTES:
1. Positive Logic:
   $S/R = T_0 + T_1 + T_2 + \ldots T_{47}$
   $T_n = C(I0\ I1\ I2 \ldots)\ (P0\ P1 \ldots P7)$
2. Either Preset (Active-High) or $\overline{\text{Output Enable}}$ (Active-Low) are available, but not both. The desired function is a user-programmable option.
3. ↑ denotes transition from Low-to-High level.
4. R = S = High is an illegal input condition.
5. * = H or L or +10V.
6. X = Don't Care (≤5.5V)

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS MIN	RATINGS MAX	UNIT
V_{CC}	Supply voltage		+7	V_{DC}
V_{IN}	Input voltage		+5.5	V_{DC}
V_{OUT}	Output voltage		+5.5	V_{DC}
I_{IN}	Input currents	–30	+30	mA
I_{OUT}	Output currents		+100	mA
T_{amb}	Operating temperature range	0	+75	°C
T_{stg}	Storage temperature range	–65	+150	°C

NOTES:
1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

LOGIC FUNCTION



VIRGIN STATE

The factory shipped virgin device contains all fusible links intact, such that:
1. PR/$\overline{OE}$ option is set to PR. Thus, all outputs will be at "1", as preset by initial power-up procedure.
2. All transition terms are disabled (0).
3. All S/R flip-flop inputs are disabled (0).
4. The device can be clocked via a Test Array pre-programmed with a standard test pattern.
   NOTE: The Test Array pattern MUST be deleted before incorporating a user program. This is accomplished automatically by any Signetics qualified programming equipment.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

DC ELECTRICAL CHARACTERISTICS

$0°C \le T_{amb} \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			MIN	TYP[1]	MAX	
Input voltage[2]						
V_{IH}	High	V_{CC} = MAX	2.0			V
V_{IL}	Low	V_{CC} = MIN			0.8	V
V_{IC}	Clamp[3]	V_{CC} = MIN, I_{IN} = –12mA		–0.8	–1.2	V
Output voltage[2]						
V_{OH}	High[4]	V_{CC} = MIN I_{OH} = –2mA	2.4			V
V_{OL}	Low[5]	I_{OL} = 9.6mA		0.35	0.45	V
Input current						
I_{IH}	High	V_{IN} = 5.5V		<1	80	µA
I_{IL}	Low	V_{IN} = 0.45V		–10	–100	µA
I_{IL}	Low (CK input)	V_{IN} = 0.45V		–50	–250	µA
Output current						
$I_{O(OFF)}$	Hi-Z state[5, 6]	V_{CC} = MAX V_{OUT} = 5.5V		1	40	µA
		V_{OUT} = 0.45V		–1	–40	µA
I_{OS}	Short circuit[3, 7]	V_{OUT} = 0V	–15		–70	mA
I_{CC}	V_{CC} supply current[8]	V_{CC} = MAX		120	180	mA
Capacitance[6]						
C_{IN}	Input	V_{CC} = 5.0V V_{IN} = 2.0V		8		pF
C_{OUT}	Output	V_{OUT} = 2.0V		10		pF

NOTES:
1. All typical values are at V_{CC} = 5V, T_{amb} = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Test one at a time.
4. Measured with V_{IL} applied to $\overline{OE}$ and a logic high stored, or with V_{IH} applied to PR.
5. Measured with a programmed logic condition for which the output is at a low logic level, and V_{IL} applied to PR/$\overline{OE}$ Output sink current is supplied through a resistor to V_{CC}.
6. Measured with V_{IH} applied to PR/$\overline{OE}$.
7. Duration of short circuit should not exceed 1 second.
8. I_{CC} is measured with the PR/$\overline{OE}$ input grounded, all other inputs at 4.5V and the outputs open.

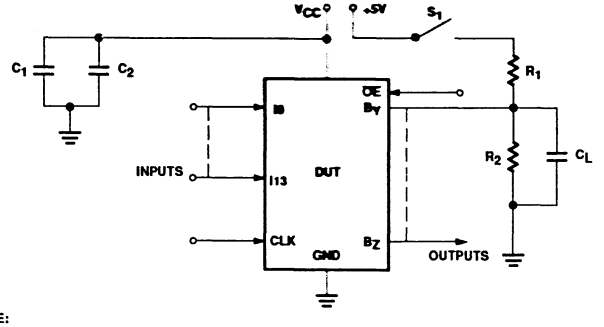
AC ELECTRICAL CHARACTERISTICS

$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0°C \le T_{amb} \le +75°C$, $4.75°CV \le V_{CC} \le 5.25V$

SYMBOL	PARAMETER	FROM	TO	LIMITS						UNIT
				PLS167			PLS167A			
				MIN	TYP[1]	MAX	MIN	TYP[1]	MAX	
Pulse width[3]										
t_{CKH}	Clock[2] High	CK +	CK –	25	15		20	15		ns
t_{CKL}	Clock Low	CK –	CK +	25	15		20	15		ns
t_{CKP}	Clock Period	CK +	CK +	50	30		40	30		ns
t_{PRH}	Preset pulse	PR +	PR –	25	15		25	15		ns
Setup time[3]										
$t_{IS1}A$	Input	Input ±	CK +	60			40			ns
$t_{IS1}B$	Input	Input ±	CK +	50			30			ns
$t_{IS1}C$	Input	Input ±	CK +	42			N/A			ns
$t_{IS2}A$	Input (through Complement Array)	Input ±	CK +	90			70			ns
$t_{IS2}B$	Input (through Complement Array)	Input	CK +	80			60			ns
$t_{IS2}C$	Input (through Complement Array)	Input	CK +	72			N/A			ns
t_{VS}	Power-on preset	V_{CC} +	CK –	0	–10		0	–10		ns
t_{PRS}	Preset	PR –	CK –	0	–10		0	–10		ns
Hold time										
t_{IH}	Input	CK +	Input ±	5	–10		5	–5		ns
Propagation delay										
t_{CKO}	Clock	CK +	Output ±		15	30		15	20	ns
t_{OE}	Output enable[4]	OE –	Output –		20	30		20	30	ns
t_{OD}	Output disable[4]	OE +	Output +		20	30		20	30	ns
t_{PR}	Preset	PR +	Output +		18	30		18	30	ns
t_{PPR}	Power-on preset	V_{CC} +	Output +		0	10		0	10	ns
Frequency of operation[3]										
$f_{MAX}C$	Without Complement Array			13.9			20.0			MHz
$f_{MAX}C$	With Complement Array			9.8			12.5			MHz

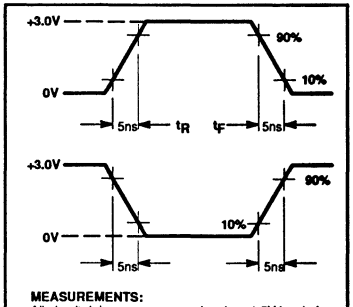
NOTES:
1. All typical values are at $V_{CC} = 5V$, $T_{amb} = +25°C$.
2. To prevent spurious clocking, clock rise time (10% – 90%) ≤ 30ns.
3. See "Speed vs. OR Loading" diagrams.
4. For 3-State output; output enable times are tested with $C_L = 30pF$ to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with $C_L = 5pF$. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} - 0.5V)$ with S_1 open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with S_1 closed.

TEST LOAD CIRCUIT



NOTE:
C_1 and C_2 are to bypass V_{CC} to GND.

VOLTAGE WAVEFORMS



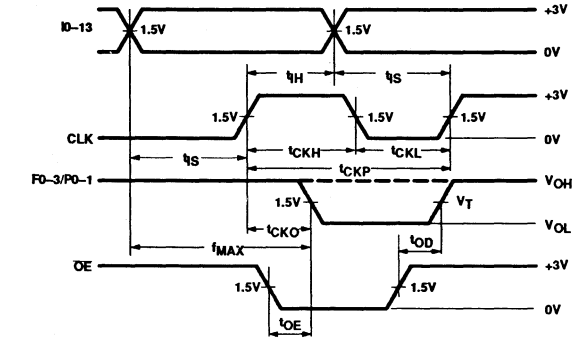
MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

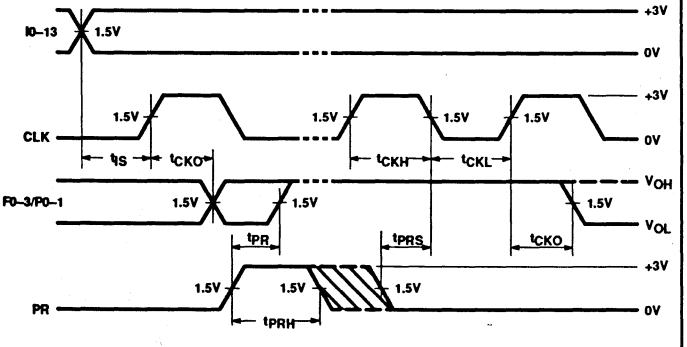
Programmable logic sequencers (14 × 48 × 6)

PLS167/A

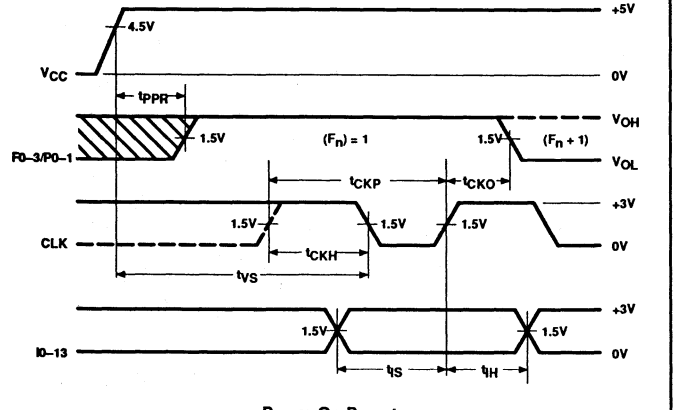
TIMING DIAGRAMS



Flip-Flop Outputs



Asynchronous Preset

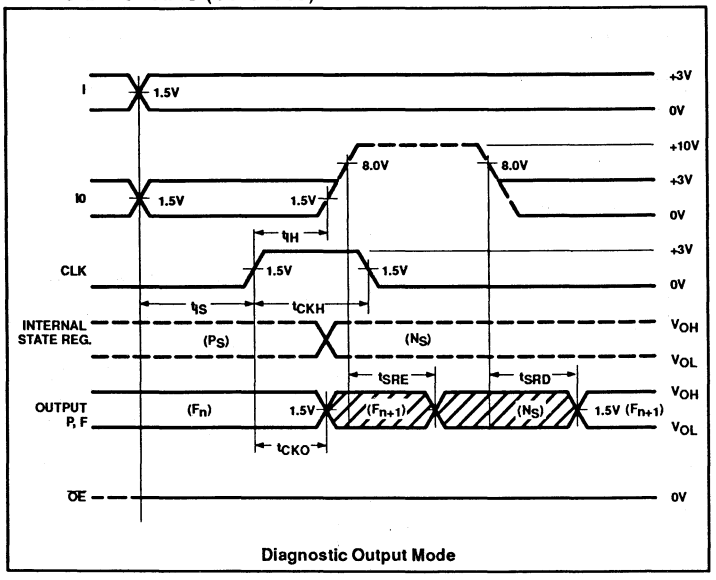


Power-On Preset

TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{CKH}	Width of input clock pulse.
t_{CKL}	Interval between clock pulses.
t_{CKP}	Minimum guaranteed clock period.
t_{IS1}	Required delay between beginning of valid input and positive transition of clock.
t_{IS2}	Required delay between beginning of valid input and positive transition of clock, when using optional Complement Array (two passes necessary through the AND array).
t_{VS}	Required delay between V_{CC} (after power-on) and negative transition of clock preceding first reliable clock pulse.
t_{PRS}	Required delay between negative transition of asynchronous Preset and negative transition of clock preceding first reliable clock pulse.
t_{IH}	Required delay between positive transition of clock and end of valid input data.
t_{CKO}	Delay between positive transition of clock and when outputs become valid (with PR/$\overline{OE}$ Low).
t_{OE}	Delay between beginning of Output Enable Low and when outputs become valid.
t_{OD}	Delay between beginning of Output Enable High and when outputs are in the OFF-State.
t_{SRE}	Delay between input I_0 transition to Diagnostic mode and when the outputs reflect the contents of the State Register.
t_{SRD}	Delay between input I_0 transition to Logic mode and when the outputs reflect the contents of the Output Register.
t_{PR}	Delay between positive transition of Preset and when outputs become valid at "1".
t_{PPR}	Delay between V_{CC} (after power-on) and when outputs become preset at "1".
t_{PRH}	Width of preset input pulse.
f_{MAX}	Minimum guaranteed operating frequency.

TIMING DIAGRAMS (Continued)



Diagnostic Output Mode

SPEED VS. "OR" LOADING

The maximum frequency at which the PLS can be clocked while operating in *sequential mode* is given by:

$$(1/f_{MAX}) = t_{CY} = t_{IS} + t_{CKO}$$

This frequency depends on the number of transition terms T_n used. Having all 48 terms connected in the AND array does not appreciably impact performance; but the number of terms connected to each OR line affects t_{IS}, due to capacitive loading. The effect of this loading can be seen in Figure 1, showing the variation of t_{IS1} with the number of terms connected per OR.

The PLS167 AC electrical characteristics contain three limits for the parameters t_{IS1} and t_{IS2} (refer to Figure 1). The first, t_{IS1A} is guaranteed for a device with 48 terms connected to any OR line. t_{IS1B} is guaranteed for a device with 32 terms connected to any OR line. And t_{IS1C} is guranteed for a device with 24 terms connected to any OR line.

The three other entries in the AC table, t_{IS2} A, B, and C are corresponding 48, 32, and 24 term limits when using the on-chip Complement Array.

The PLS167A AC electrical characteristics contain two limits for the parameters t_{IS1} and t_{IS2} (refer to Figure 2). The first, t_{IS1A} is guaranteed for a device with 24 terms connected to any OR line. t_{IS1B} is guaranteed for a device with 16 terms connected to any OR line.

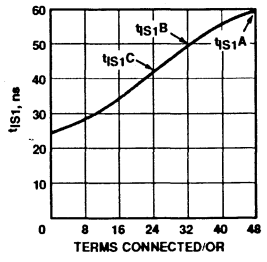


Figure 1. PLS167 t_{IS1} vs. Terms/OR Connected

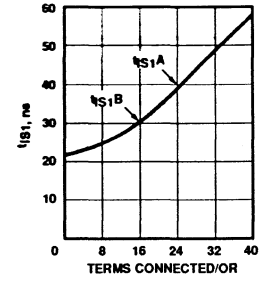


Figure 2. PLS167A t_{IS1} vs. Terms/OR Connected

The two other entries in the AC table, t_{IS2} A and B are corresponding 24 and 16 term limits when using the on-chip Complement Array.

The worst case of t_{IS} for a given application can be determined by identifying the OR line with the maximum number of T_n connections. This can be done by referring to the interconnect pattern in the PLS logic diagram, typically illustrated in Figure 3, or by counting the maximum number of "H" *or* "L" entries in one of the columns of the device Program Table.

This number plotted on the curve in Figure 1 or Figure 2 will yield the worst case t_{IS} and, by implication, the maximum clocking frequency for reliable operation.

Note that for maximum speed all UNUSED transition terms should be disconnected from the OR array.

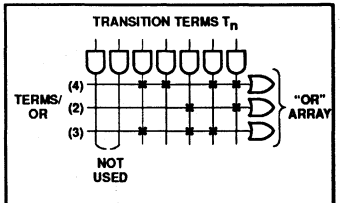


Figure 3. Typical OR Array Interconnect Pattern

Programmable logic sequencers (14 × 48 × 6)

PLS167/A

LOGIC PROGRAMMING

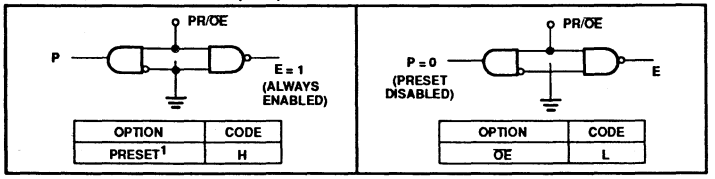
The PLS167/A devices are fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Signetics' SNAP and SLICE design software packages. ABEL™, CUPL™ and PALASM® 90 design software packages also support the PLS167/A architecture.

All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

PLS167/A logic designs can also be generated using the program table entry format detailed on the following pages. This program table entry format is supported by the Signetics SNAP and SLICE PLD design software packages (PTP module). SLICE is available free of charge to qualified users.

To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

PRESET/$\overline{OE}$ OPTION – (P/E)



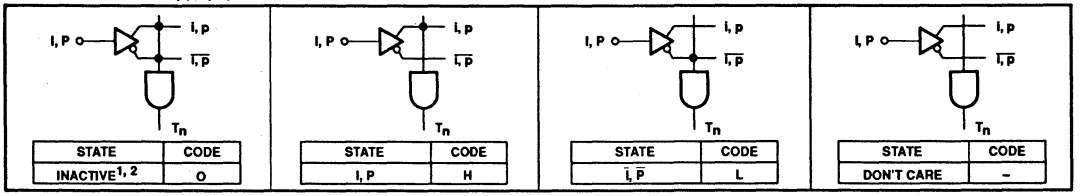
OPTION	CODE
PRESET[1]	H

OPTION	CODE
$\overline{OE}$	L

PROGRAMMING:

The PS167/A has a power-up preset feature. This feature insures that the device will power-up in a known state with all register elements (State and Output Register) at logic High (H). When programming the device it is important to realize this is the initial state of the device. You *must* provide a next state jump if you do not wish to use all Highs (H) as the present state.

"AND" ARRAY – (I), (P)



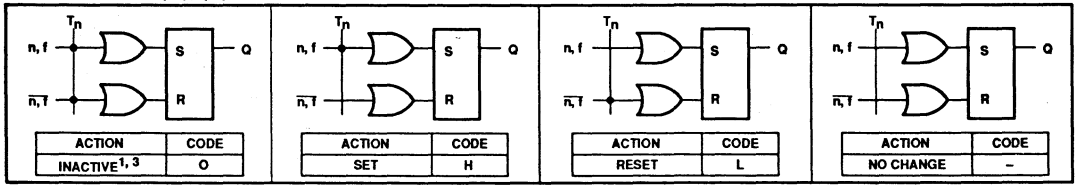
STATE	CODE
INACTIVE[1, 2]	O

STATE	CODE
I, P	H

STATE	CODE
$\overline{I, P}$	L

STATE	CODE
DON'T CARE	–

"OR" ARRAY – (N), (F)



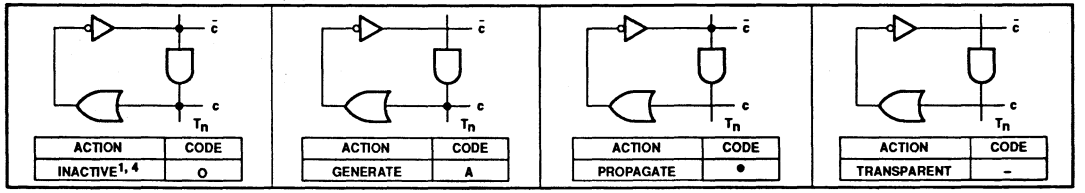
ACTION	CODE
INACTIVE[1, 3]	O

ACTION	CODE
SET	H

ACTION	CODE
RESET	L

ACTION	CODE
NO CHANGE	–

"COMPLEMENT" ARRAY – (C)



ACTION	CODE
INACTIVE[1, 4]	O

ACTION	CODE
GENERATE	A

ACTION	CODE
PROPAGATE	•

ACTION	CODE
TRANSPARENT	–

NOTES:

1. This is the initial unprogrammed state of all links.
2. Any gate T_n will be unconditionally inhibited if both the true and complement of any input (I, P) are left intact.
3. To prevent simultaneous Set and Reset flip-flop commands, this state is not allowed for N and F link pairs coupled to active gates T_n (see flip-flop truth tables).
4. To prevent oscillations, this state is not allowed for C link pairs coupled to active gates T_n.

ABEL is a trademark of Data I/O Corp.
CUPL is a trademark of Logical Devices, Inc.
PALASM is a registered trademark of AMD Corp.

Programmable logic sequencers (14 × 48 × 6)

PLS167/A

PROGRAM TABLE

CUSTOMER NAME_____
PURCHASE ORDER #_____
SIGNETICS DEVICE # CF (XXXX)
CUSTOMER SYMBOLIZED PART #_____
TOTAL NUMBER OF PARTS_____
PROGRAM TABLE_____
REV_____
DATE_____

PROGRAM TABLE ENTRIES

AND		C_n	OR		Ns, Fr
INACTIVE	0		INACTIVE	0	
GENERATE	A		SET	H	
PROPAGATE	•		RESET	L	
TRANSPARENT	—		NO CHANGE	—	

		I_m, P_s	OPTION		P/E
INACTIVE	0		PRESET	H	
I, P	H		$\overline{OE}$	L	
$\overline{I}$, $\overline{P}$	L				
DON'T CARE	—				

TERM	C_n	AND: INPUT (I_m) 13 12 11 10 9 8 7 6 5 4 3 2 1 0	AND: PRESENT STATE (P_s) 7 6 5 4 3 2 1 0	REMARKS	OPTION (P/E) OR: NEXT STATE (Ns) 7 6 5 4 3 2 1 0	OUTPUT (Fr) 3 2 1 0
0						
1						
2						
3						
4						
5						
6						
7						
8						
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43						
44						
45						
46						
47						
PIN NO.		17 18 19 20 21 22 23 2 3 4 5 6 7 8				15 14 13 11 10 9
VARIABLE NAME						

NOTES:

1. The device is shipped with all links initially intact. Thus, a background of "0" for all Terms, and an "H" for the P/E option, exists in the table, shown BLANK instead for clarity.
2. Unused C_n, I_m, and P_s bits are normally programmed Don't Care (–).
3. Unused Transition Terms can be left blank for future code modification, or programmed as (–) for maximum speed.
4. Letters in variable fields are used as identifiers by logic type programmers.

Programmable logic sequencers (14 × 48 × 6)

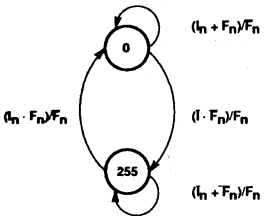
PLS167/A

TEST ARRAY

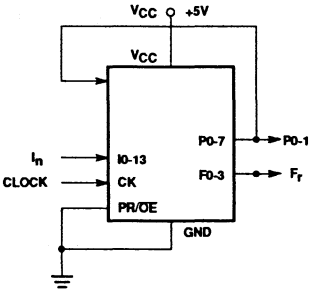
The PLS may be subjected to AC and DC parametric tests prior to programming via an on-chip test array.

The array consists of test transition terms 48 and 49, factory programmed as shown below.

Testing is accomplished by clocking the PLS and applying the proper input sequence to $I_{0\text{-}13}$ as shown in the test circuit timing diagram.



State Diagram

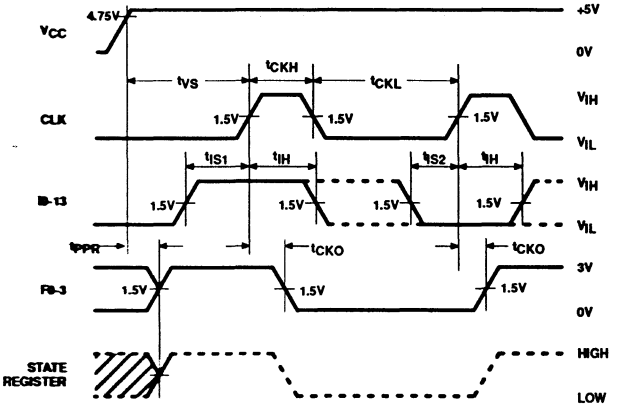


PLS Under Test

TERM	C	AND INPUT (Im) 13	12	11	10	9	8	7	6	5	4	3	2	1	0	PRESENT STATE (Ps) 7	6	5	4	3	2	1	0	OPTION (P/E) H; OR; NEXT STATE (Ns) 7	6	5	4	3	2	1	0	OUTPUT (Fr) 3	2	1	0
48	A	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L
49	•	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H

Test Array Program

Both terms 48 and 49 must be deleted during user programming to avoid interfering with the desired logic function. This is accomplished automatically by any Signetic's qualified programming equipment.

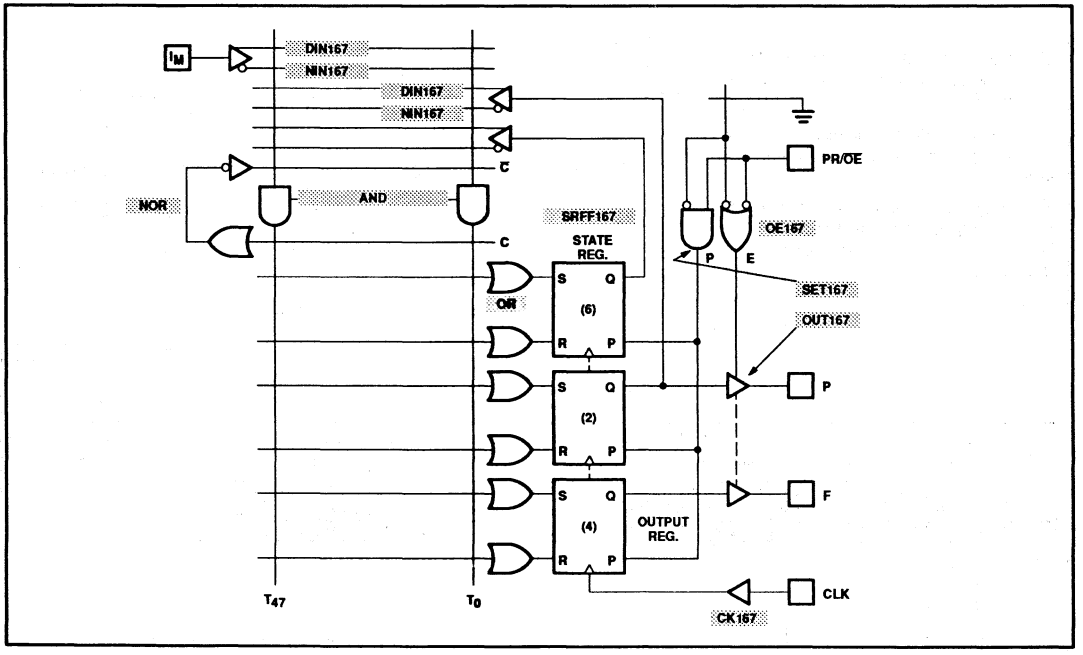


Test Circuit Timing Diagram

TERM	C	AND INPUT (Im) 13	12	11	10	9	8	7	6	5	4	3	2	1	0	PRESENT STATE (Ps) 7	6	5	4	3	2	1	0	OPTION (P/E) H; OR; NEXT STATE (Ns) 7	6	5	4	3	2	1	0	OUTPUT (Fr) 5	4	3	2	1	0
48	–	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	–	–	–	–	–	–	–	–	–	–	–	–	–	–
49	•	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	–	–	–	–	–	–	–	–	–	–	–	–	–	–

Test Array Deleted

SNAP RESOURCE SUMMARY DESIGNATIONS



Programmable logic sequencers (12 × 48 × 8)

PLS168/A

DESCRIPTION

The PLS168 and the PLS168A are bipolar, Programmable Logic State machines of the Mealy type. They contain logic AND/OR gate arrays with user programmable connections which control the inputs of on-chip State and Output Registers. These consist respectively of 10 Q_P, and 4 Q_F edge-triggered, clocked S/R flip-flops, with an Asynchronous Preset Option.

All flip-flops are unconditionally preset to "1" during power turn-on.

The AND array combines 12 external inputs, I0-11, with 10 internal inputs, P0-9, fed back from the State Register to form up to 48 transition terms (AND terms). In addition, P0–P3 of the internal State Register are brought off-chip to allow extending the Output Register to 8 bits, if so desired.

All transition terms can include True, False, or Don't Care states of the controlling variables, and are merged in the OR array to issue next-state and next-output commands to their respective registers on the Low-to-High transition of the Clock pulse.

Both True and Complement transition terms can be generated by optional use of the internal variable (C) from the Complement Array. Also, if desired, the Preset input can be converted to output-enable function, as an additional user programmable option.

Order codes are listed in the Ordering Information table below.

FEATURES

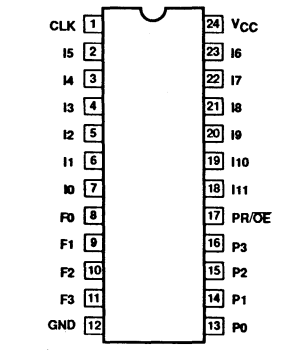
- PLS168
  - f_{MAX} = 13.9MHz
  - 20MHz clock rate
- PLS168A
  - f_{MAX} = 20MHz
  - 25MHz clock rate
- Field-Programmable (Ni-Cr link)
- 12 True/Complement buffered inputs
- 48 programmable AND gates
- 29 programmable OR gates
- 10-bit State Register
- 4-bit shared State/Output Register
- 4-bit Output Register
- Transition Complement Array
- Programmable Asynchronous Preset/Output Enable
- Positive edge-triggered clock
- Power-on preset to logic "1" of all registers
- Automatic logic "HOLD" state via S/R flip-flops
- On-chip Test Array
- Power: 600mW (typ.)
- TTL compatible
- 3-State outputs
- Single +5V supply

APPLICATIONS

- Interface protocols
- Sequence detectors
- Peripheral controllers
- Timing generators
- Sequential circuits
- Security locking systems
- Counters
- Shift registers

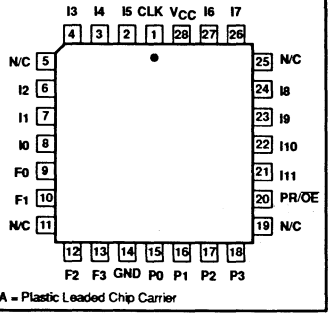
PIN CONFIGURATIONS

N Package



N = Plastic DIP (300mil-wide)

A Package



A = Plastic Leaded Chip Carrier

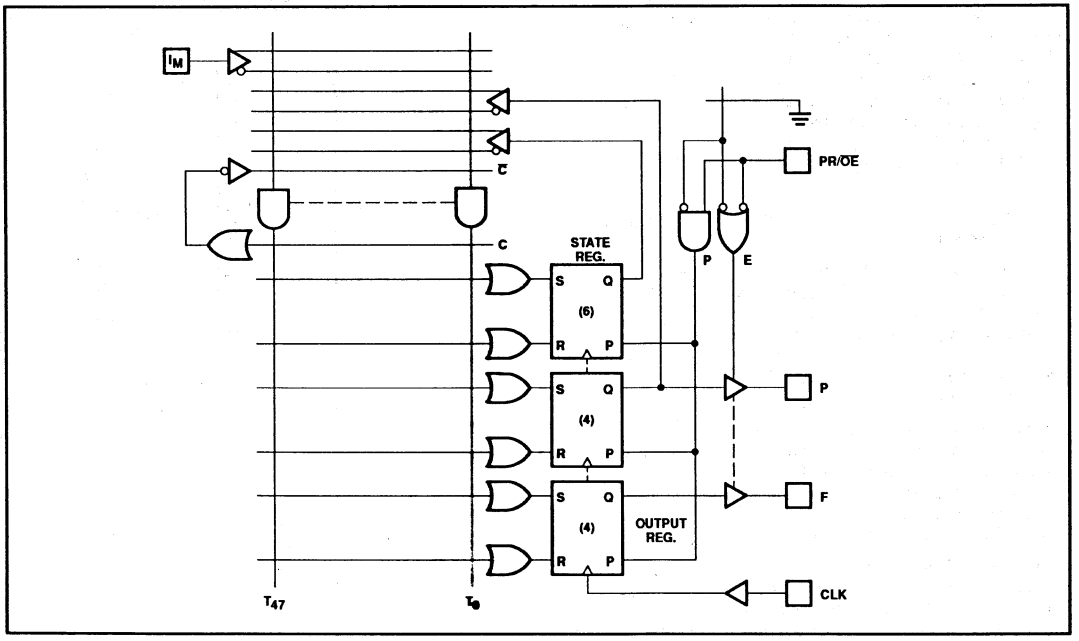
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-Pin Plastic DIP (300mil-wide)	PLS168N, PLS168AN
28-Pin Plastic Leaded Chip Carrier	PLS168A, PLS168AA

Programmable logic sequencers (12 × 48 × 8)

PLS168/A

FUNCTIONAL DIAGRAM



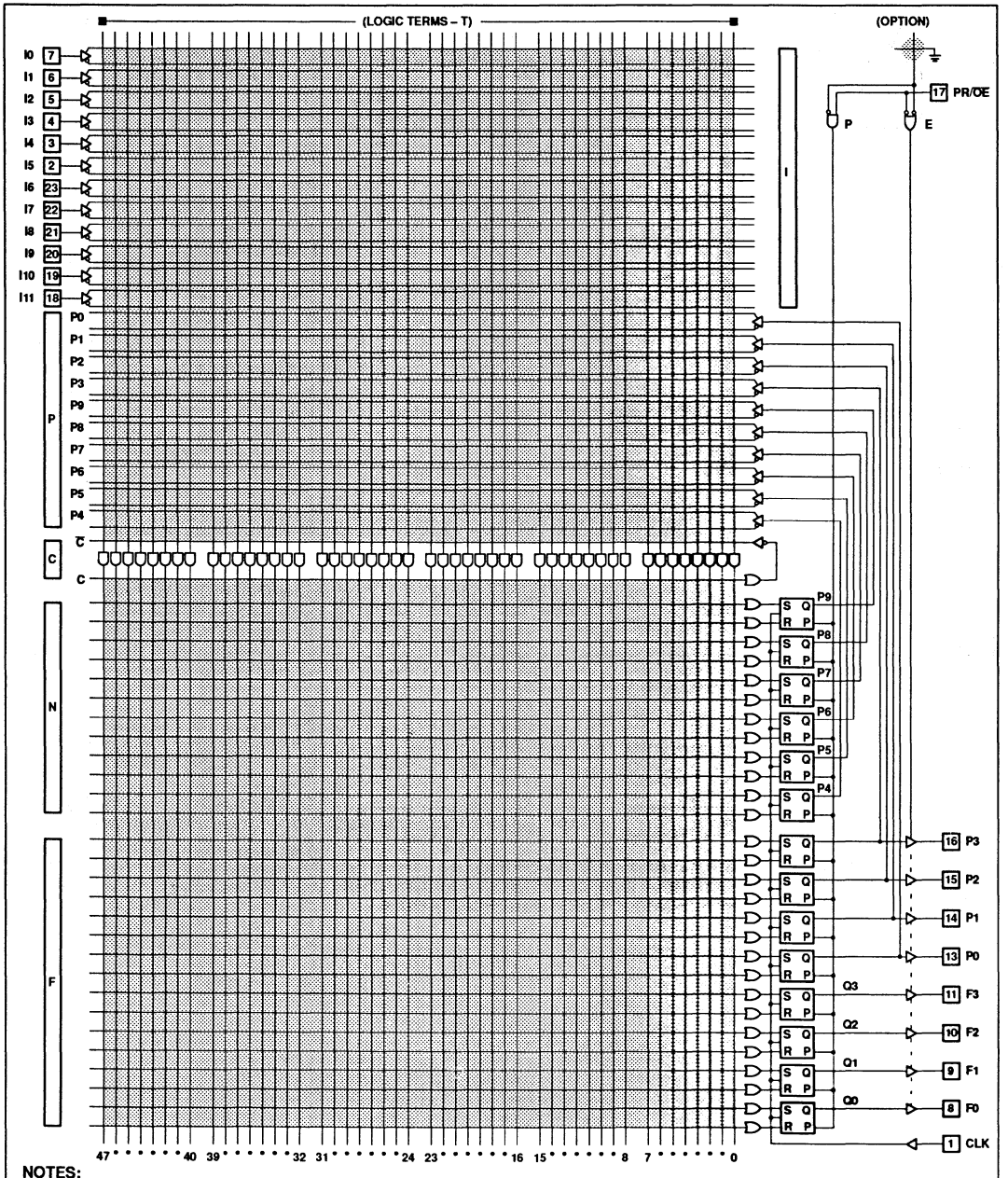
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION	POLARITY
1	CLK	**Clock:** The Clock input to the State and Output Registers. A Low-to-High transition on this line is necessary to update the contents of both registers.	Active-High
2 – 6 18 – 23	I1 – I11	**Logic Inputs:** The 11 external inputs to the AND array used to program jump conditions between machine states, as determined by a given logic sequence.	Active-High/Low
7	I0	**Logic/Diagnostic Input:** A 12th external logic input to the AND array, as above, when exercised with standard TTL levels. When I0 is held at +10V, device outputs F2 – F3 and P0 – P3 reflect the contents of State Register bits P4 – 9 (see Diagnostic Output Mode diagram). The contents of flip-flops P0 – 1 and F0 – 3 remain unaltered.	Active-High/Low
13 – 16	P0 – 3	**Logic/Diagnostic Outputs:** Four device outputs which normally reflect the contents of State Register bits P0 – 3. When I0 is held at +10V these pins reflect (P6 – P9).	Active-High
10 – 11	F2 – F3	**Logic/Diagnostic Outputs:** Two register bits (F2 – F3) which reflect Output register bits (Q2 – Q3). When I0 is held at +10V, these pins reflect (P4 – P5).	Active-High
17	PR/$\overline{OE}$	**Preset or $\overline{\text{Output Enable}}$ Input:** A user programmable function:	
		• **Preset:** Provides an Asynchronous Preset to logic "1" of all State and Output Register bits. Preset overrides Clock, and when held High, clocking is inhibited and P0 – 9 and F0 – 3 are High. Normal clocking resumes with the first full clock pulse following a High-to-Low clock transition, after Preset goes Low.	Active-High (H)
		• $\overline{\text{Output Enable}}$**:** Provides an Output Enable function to all output buffers.	Active-Low (L)
8, 9	F0 – F1	**Logic Output:** Two device outputs which reflect Output Registers Q0 – Q1. When I0 is held at +10V, F0 – F1 = Logic "1".	

Programmable logic sequencers (12 × 48 × 8)

PLS168/A

LOGIC DIAGRAM



NOTES:
1. All programmed "AND" gate locations are pulled to logic "1".
2. All programmed "OR" gate locations are pulled to logic "0".
3. ▒ Programmable connection.

Programmable logic sequencers (12 × 48 × 8)

PLS168/A

TRUTH TABLE [1, 2, 3, 4, 5, 6]

V_{CC}	OPTION PR	OPTION $\overline{OE}$	I_0	CLK	S	R	$Q_{P/F}$	F
+5V	H		*	X	X	X	H	H
	L		+10V	X	X	X	Q_n	$(Q_P)_n$
	L		X	X	X	X	Q_n	$(Q_F)_n$
		H	*	X	X	X	Q_n	Hi-Z
		L	+10V	X	X	X	Q_n	$(Q_P)_n$
		L	X	X	X	X	Q_n	$(Q_F)_n$
		L	X	↑	L	L	Q_n	$(Q_F)_n$
		L	X	↑	L	H	L	L
		L	X	↑	H	L	H	H
		L	X	↑	H	H	IND.	IND.
↑	X	X	X	X	X	X	H	

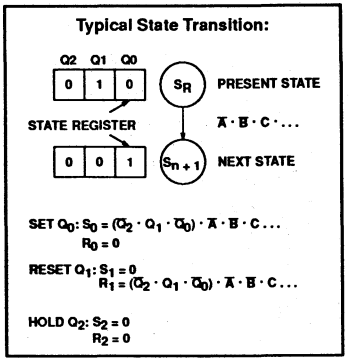
NOTES:
1. Positive Logic:
   $S/R = T_0 + T_1 + T_2 + \ldots + T_{47}$
   $T_n = C(I0\ I1\ I2 \ldots)\ (P0\ P1 \ldots P9)$
2. Either Preset (Active-High) or $\overline{\text{Output Enable}}$ (Active-Low) are available, but not both. The desired function is a user-programmable option.
3. ↑ denotes transition from Low-to-High level.
4. R = S = High is an illegal input condition.
5. * = H or L or +10V.
6. X = Don't Care (≤5.5V)

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS MIN	RATINGS MAX	UNIT
V_{CC}	Supply voltage		+7	V_{DC}
V_{IN}	Input voltage		+5.5	V_{DC}
V_{OUT}	Output voltage		+5.5	V_{DC}
I_{IN}	Input currents	–30	+30	mA
I_{OUT}	Output currents		+100	mA
T_{amb}	Operating temperature range	0	+75	°C
T_{stg}	Storage temperature range	–65	+150	°C

NOTES:
1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

LOGIC FUNCTION



VIRGIN STATE

The factory shipped virgin device contains all fusible links intact, such that:
1. PR/$\overline{OE}$ option is set to PR. Thus, all outputs will be at "1", as preset by initial power-up procedure.
2. All transition terms are disabled (0).
3. All S/R flip-flop inputs are disabled (0).
4. The device can be clocked via a Test Array pre-programmed with a standard test pattern.
   NOTE: The Test Array pattern MUST be deleted before incorporating a user program. This is accomplished automatically by any Signetics qualified programming equipment.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

DC ELECTRICAL CHARACTERISTICS

$0°C \leq T_{amb} \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			MIN	TYP[1]	MAX	
Input voltage[2]						
V_{IH}	High	V_{CC} = MAX	2.0			V
V_{IL}	Low	V_{CC} = MIN			0.8	V
V_{IC}	Clamp[3]	V_{CC} = MIN, I_{IN} = –12mA		–0.8	–1.2	V
Output voltage[2]						
		V_{CC} = MIN				
V_{OH}	High[4]	I_{OH} = –2mA	2.4			V
V_{OL}	Low[5]	I_{OL} = 9.6mA		0.35	0.45	V
Input current						
I_{IH}	High	V_{IN} = 5.5V		<1	25	µA
I_{IL}	Low	V_{IN} = 0.45V		–10	–100	µA
I_{IL}	Low (CLK input)	V_{IN} = 0.45V		–50	–250	µA
Output current						
		V_{CC} = MAX				
$I_{O(OFF)}$	Hi-Z state[6]	V_{OUT} = 5.5V		1	40	µA
		V_{OUT} = 0.45V		–1	–40	µA
I_{OS}	Short circuit[3, 7]	V_{OUT} = 0V	–15		–70	mA
I_{CC}	V_{CC} supply current[8]	V_{CC} = MAX		120	180	mA
Capacitance[6]						
		V_{CC} = 5.0V				
C_{IN}	Input	V_{IN} = 2.0V		8		pF
C_{OUT}	Output	V_{OUT} = 2.0V		10		pF

NOTES:

1. All typical values are at V_{CC} = 5V, T_{amb} = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Test one at a time.
4. Measured with V_{IL} applied to $\overline{OE}$ and a logic high stored, or with V_{IH} applied to PR.
5. Measured with a programmed logic condition for which the output is at a low logic level, and V_{IL} applied to PR/$\overline{OE}$. Output sink current is supplied through a resistor to V_{CC}.
6. Measured with V_{IH} applied to PR/$\overline{OE}$.
7. Duration of short circuit should not exceed 1 second.
8. I_{CC} is measured with the PR/$\overline{OE}$ input grounded, all other inputs at 4.5V and the outputs open.

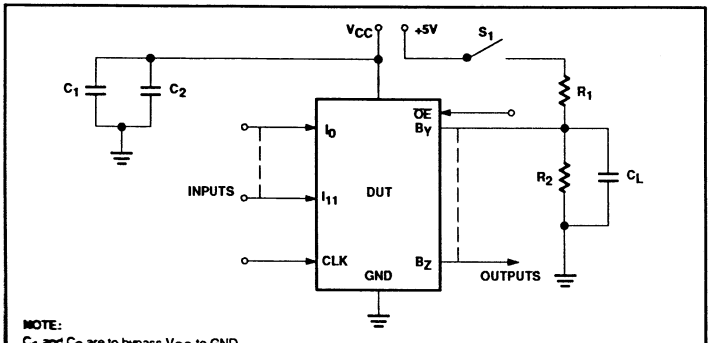
AC ELECTRICAL CHARACTERISTICS

$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0°C \le T_{amb} \le +75°C$, $4.75°CV \le V_{CC} \le 5.25V$

SYMBOL	PARAMETER	FROM	TO	LIMITS						UNIT
				PLS168			PLS168A			
				MIN	TYP[1]	MAX	MIN	TYP[1]	MAX	
Pulse width[3]										
t_{CKH}	Clock[2] High	CK +	CK –	25	15		20	15		ns
t_{CKL}	Clock Low	CK –	CK +	25	15		20	15		ns
t_{CKP}	Clock Period	CK +	CK +	50	30		40	30		ns
t_{PRH}	Preset pulse	PR +	PR –	25	15		25	15		ns
Setup time[3]										
$t_{IS1}A$	Input	Input ±	CK +	60			40			ns
$t_{IS1}B$	Input	Input ±	CK +	50			30			ns
$t_{IS1}C$	Input	Input ±	CK +	42			N/A			ns
$t_{IS2}A$	Input (through Complement Array)	Input ±	CK +	90			70			ns
$t_{IS2}B$	Input (through Complement Array)	Input	CK +	80			60			ns
$t_{IS2}C$	Input (through Complement Array)	Input	CK +	72			N/A			ns
t_{VS}	Power-on preset	V_{CC} +	CK –	0	–10		0	–10		ns
t_{PRS}	Preset	PR –	CK –	0	–10		0	–10		ns
Hold time										
t_{IH}	Input	CK +	Input ±	5	–10		5	–10		ns
Propagation delay										
t_{CKO}	Clock	CK +	Output ±		15	30		15	20	ns
t_{OE}	Output enable[4]	OE –	Output –		20	30		20	30	ns
t_{OD}	Output disable[4]	OE +	Output +		20	30		20	30	ns
t_{PR}	Preset	PR +	Output +		18	30		18	30	ns
t_{PPR}	Power-on preset	V_{CC} +	Output +		0	10		0	10	ns
Frequency of operation[3]										
$f_{MAX}C$	Without Complement Array			13.9			20.0			MHz
$f_{MAX}C$	With Complement Array			9.8			12.5			MHz

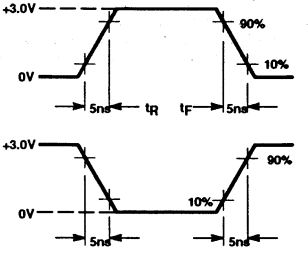
NOTES:
1. All typical values are at $V_{CC} = 5V$, $T_{amb} = +25°C$.
2. To prevent spurious clocking, clock rise time (10% – 90%) ≤ 30ns.
3. See "Speed vs. OR Loading" diagrams.
4. For 3-State output; output enable times are tested with $C_L = 30pF$ to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with $C_L = 5pF$. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} - 0.5V)$ with S_1 open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with S_1 closed.

TEST LOAD CIRCUIT



NOTE:
C_1 and C_2 are to bypass V_{CC} to GND.

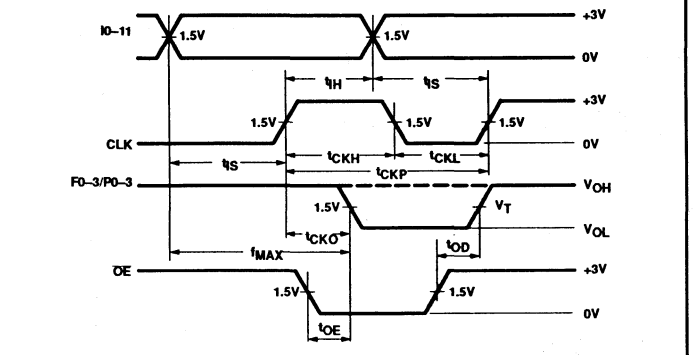
VOLTAGE WAVEFORMS



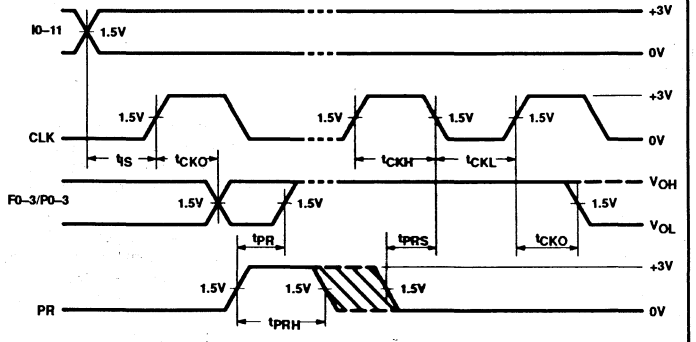
MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

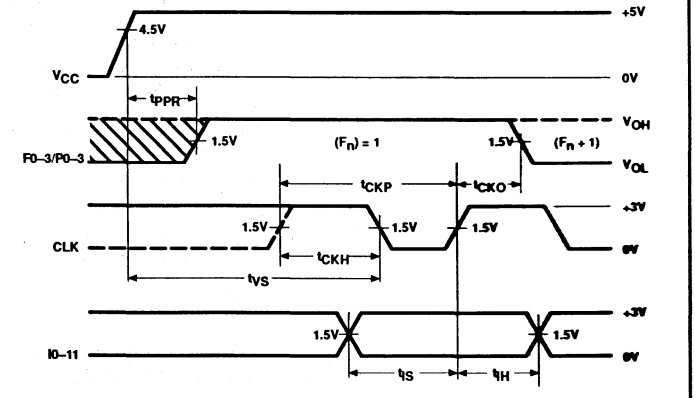
TIMING DIAGRAMS



Flip-Flop Outputs



Asynchronous Preset

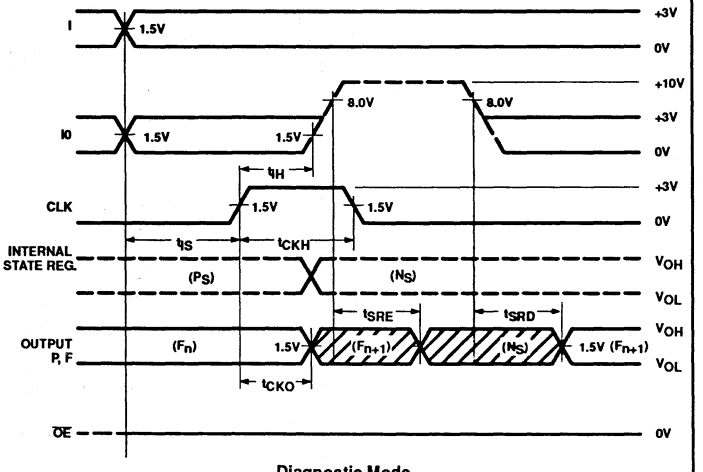


Power-On Preset

TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{CKH}	Width of input clock pulse.
t_{CKL}	Interval between clock pulses.
t_{CKP}	Minimum guaranteed clock period.
t_{IS1}	Required delay between beginning of valid input and positive transition of clock.
t_{IS2}	Required delay between beginning of valid input and positive transition of clock, when using optional Complement Array (two passes necessary through the AND array).
t_{VS}	Required delay between V_{CC} (after power-on) and negative transition of clock preceding first reliable clock pulse.
t_{PRS}	Required delay between negative transition of asynchronous Preset and negative transition of clock preceding first reliable clock pulse.
t_{IH}	Required delay between positive transition of clock and end of valid input data.
t_{CKO}	Delay between positive transition of clock and when outputs become valid (with PR/$\overline{OE}$ Low).
t_{OE}	Delay between beginning of Output Enable Low and when outputs become valid.
t_{OD}	Delay between beginning of Output Enable High and when outputs are in the OFF-State.
t_{SRE}	Delay between input I_0 transition to Diagnostic mode and when the outputs reflect the contents of the State Register.
t_{SRD}	Delay between input I_0 transition to Logic mode and when the outputs reflect the contents of the Output Register.
t_{PR}	Delay between positive transition of Preset and when outputs become valid at "1".
t_{PPR}	Delay between V_{CC} (after power-on) and when outputs become preset at "1".
t_{PRH}	Width of preset input pulse.
f_{MAX}	Minimum guaranteed operating frequency.

TIMING DIAGRAMS (Continued)



Diagnostic Mode

SPEED VS. "OR" LOADING

The maximum frequency at which the PLS can be clocked while operating in *sequential mode* is given by:

$$(1/f_{MAX}) = t_{CY} = t_{IS} + t_{CKO}$$

This frequency depends on the number of transition terms T_n used. Having all 48 terms connected in the AND array does not appreciably impact performance; but the number of terms connected to each OR line affects t_{IS}, due to capacitive loading. The effect of this loading can be seen in Figure 1, showing the variation of t_{IS1} with the number of terms connected per OR.

The PLS168 AC electrical characteristics contain three limits for the parameters t_{IS1} and t_{IS2} (refer to Figure 1). The first, t_{IS1A} is guaranteed for a device with 48 terms connected to any OR line. t_{IS1B} is guaranteed for a device with 32 terms connected to any OR line. And t_{IS1C} is guranteed for a device with 24 terms conntected to any OR line.

The three other entries in the AC table, t_{IS2} A, B, and C are corresponding 48, 32, and 24 term limits when using the on-chip Complement Array.

The PLS168A AC electrical characteristics contain two limits for the parameters t_{IS1} and t_{IS2} (refer to Figure 2). The first, t_{IS1A} is guaranteed for a device with 24 terms connected to any OR line. t_{IS1B} is guaranteed for a device with 16 terms connected to any OR line.

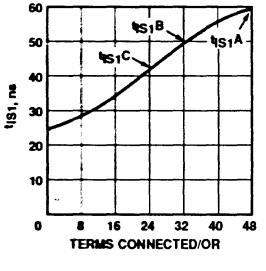


Figure 1. PLS168 t_{IS1} vs. Terms/OR Connected

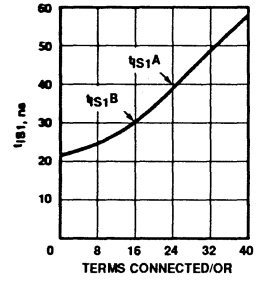


Figure 2. PLS168A t_{IS1} vs. Terms/OR Connected

The two other entries in the AC table, t_{IS2} A and B are corresponding 24 and 16 term limits when using the on-chip Complement Array.

The worst case of t_{IS} for a given application can be determined by identifying the OR line with the maximum number of T_n connections. This can be done by referring to the interconnect pattern in the PLS logic diagram, typically illustrated in Figure 3, or by counting the maximum number of "H" *or* "L" entries in one of the columns of the device Program Table.

This number plotted on the curve in Figure 1 or 2 will yield the worst case t_{IS} and, by implication, the maximum clocking frequency for reliable operation.

Note that for maximum speed all UNUSED transition terms should be disconnected from the OR array.

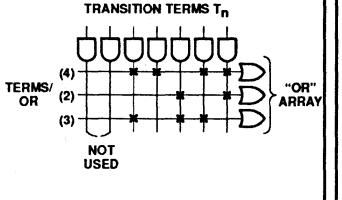


Figure 3. Typical OR Array Interconnect Pattern

Programmable logic sequencers (12 × 48 × 8)

PLS168/A

LOGIC PROGRAMMING

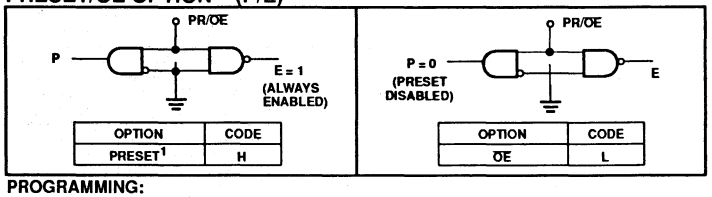
The PLS168/A devices are fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Signetics' SNAP and SLICE design software packages. ABEL™, CUPL™ and PALASM® 90 design software packages also support the PLS168/A architecture.

All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

PLS168/A logic designs can also be generated using the program table entry format detailed on the following pages. This program table entry format is supported by the Signetics SNAP and SLICE PLD design software packages (PTP module). SLICE is available free of charge to qualified users.

To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

PRESET/$\overline{OE}$ OPTION – (P/E)



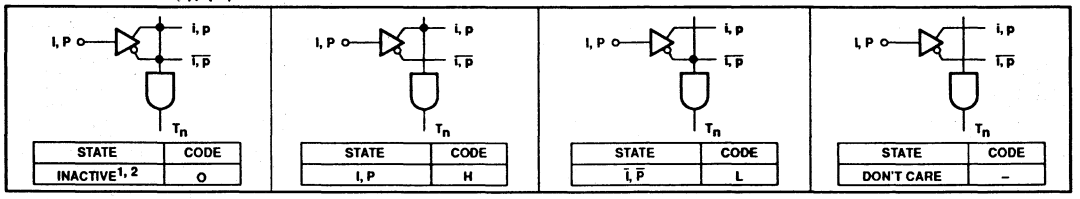
OPTION	CODE
PRESET[1]	H

OPTION	CODE
$\overline{OE}$	L

PROGRAMMING:

The PLS168/A has a power-up preset feature. This feature insures that the device will power-up in a known state with all register elements (State and Output Register) at logic High (H). When programming the device it is important to realize this is the initial state of the device. You *must* provide a next state jump if you do not wish to use all Highs (H) as the present state.

"AND" ARRAY – (I), (P)



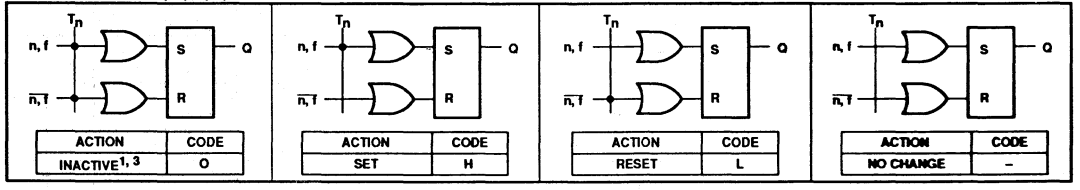
STATE	CODE
INACTIVE[1, 2]	O

STATE	CODE
I, P	H

STATE	CODE
$\overline{I, P}$	L

STATE	CODE
DON'T CARE	–

"OR" ARRAY – (N), (F)



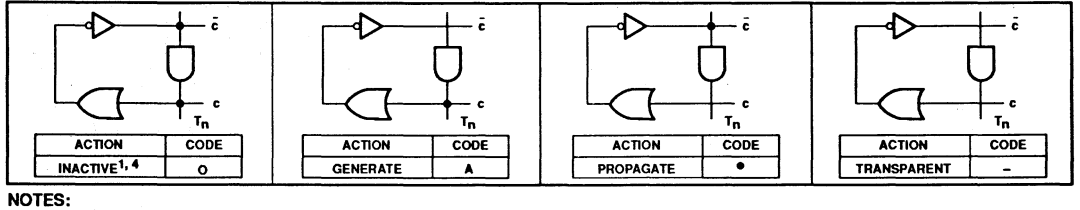
ACTION	CODE
INACTIVE[1, 3]	O

ACTION	CODE
SET	H

ACTION	CODE
RESET	L

ACTION	CODE
NO CHANGE	–

"COMPLEMENT" ARRAY – (C)



ACTION	CODE
INACTIVE[1, 4]	O

ACTION	CODE
GENERATE	A

ACTION	CODE
PROPAGATE	•

ACTION	CODE
TRANSPARENT	–

NOTES:

1. This is the initial unprogrammed state of all links.
2. Any gate T_n will be unconditionally inhibited if both the true and complement of any input (I, P) are left intact.
3. To prevent simultaneous Set and Reset flip-flop commands, this state is not allowed for N and F link pairs coupled to active gates T_n (see flip-flop truth tables).
4. To prevent oscillations, this state is not allowed for C link pairs coupled to active gates T_n.

ABEL is a trademark of Data I/O Corp.
CUPL is a trademark of Logical Devices, Inc.
PALASM is a registered trademark of AMD Corp.

Programmable logic sequencers (12 × 48 × 8)

PLS168/A

PROGRAM TABLE

CUSTOMER NAME_____
PURCHASE ORDER #_____
SIGNETICS DEVICE # CF (XXXX)
CUSTOMER SYMBOLIZED PART #_____
TOTAL NUMBER OF PARTS_____
PROGRAM TABLE_____
REV_____
DATE_____

PROGRAM TABLE ENTRIES

AND			OR		
INACTIVE	0	C_n	INACTIVE	0	Ns, Fr
GENERATE	A		SET	H	
PROPAGATE	•		RESET	L	
TRANSPARENT	—		NO CHANGE	—	
INACTIVE	0	I_m, P_s	**OPTION**		
I, P	H		PRESET	H	P/E
$\overline{I}$, $\overline{P}$	L		$\overline{OE}$	L	
DON'T CARE	—				

TERM	C_n	AND: INPUT (I_m) 11 10 9 8 7 6 5 4 3 2 1 0	AND: PRESENT STATE (P_s) 9 8 7 6 5 4 3 2 1 0	REMARKS	OPTION (P/E) OR: NEXT STATE (Ns) 9 8 7 6 5 4 3 2 1 0	OUTPUT (Fr) 3 2 1 0
0						
1						
2						
3						
4						
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47						

PIN NO.	18	19	20	21	22	23	2	3	4	5	6	7	16	15	14	13	11	10	9	8
VARIABLE NAME																				

NOTES:

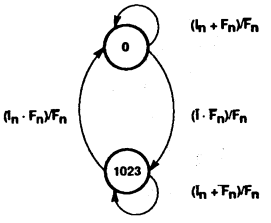
1. The device is shipped with all links initially intact. Thus, a background of "0" for all Terms, and an "H" for the P/E option, exists in the table, shown BLANK instead for clarity.
2. Unused C_n, I_m, and P_s bits are normally programmed Don't Care (–).
3. Unused Transition Terms can be left blank for future code modification, or programmed as (–) for maximum speed.
4. Letters in variable fields are used as identifiers by logic type programmers.

TEST ARRAY

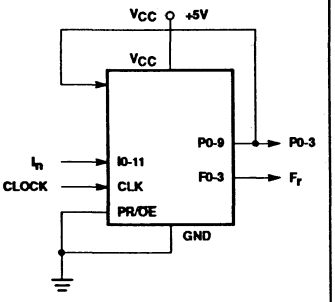
The PLS may be subjected to AC and DC parametric tests prior to programming via an on-chip test array.

The array consists of test transition terms 48 and 49, factory programmed as shown below.

Testing is accomplished by clocking the FPLS and applying the proper input sequence to I0-13 as shown in the test circuit timing diagram.



State Diagram

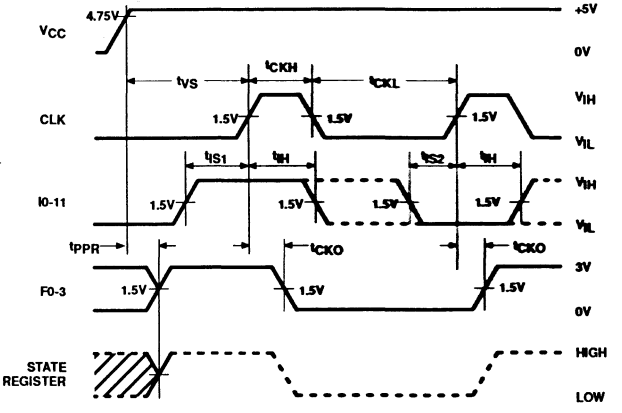


FPLS Under Test

TERM	C_n	AND: INPUT (Im) 11 10 9 8 7 6 5 4 3 2 1 0	AND: PRESENT STATE (Ps) 9 8 7 6 5 4 3 2 1 0	OPTION (P/E) H — OR: NEXT STATE (Ns) 9 8 7 6 5 4 3 2 1 0	OR: OUTPUT (Fr) 3 2 1 0
48	A	H H H H H H H H H H H H	H H H H H H H H H H	L L L L L L L L L L	L L L L
49	•	L L L L L L L L L L L L	L L L L L L L L L L	H H H H H H H H H H	H H H H

Test Array Program

Both terms 48 and 49 must be deleted during user programming to avoid interfering with the desired logic function. This is accomplished automatically by any Signetic's qualified programming equipment.

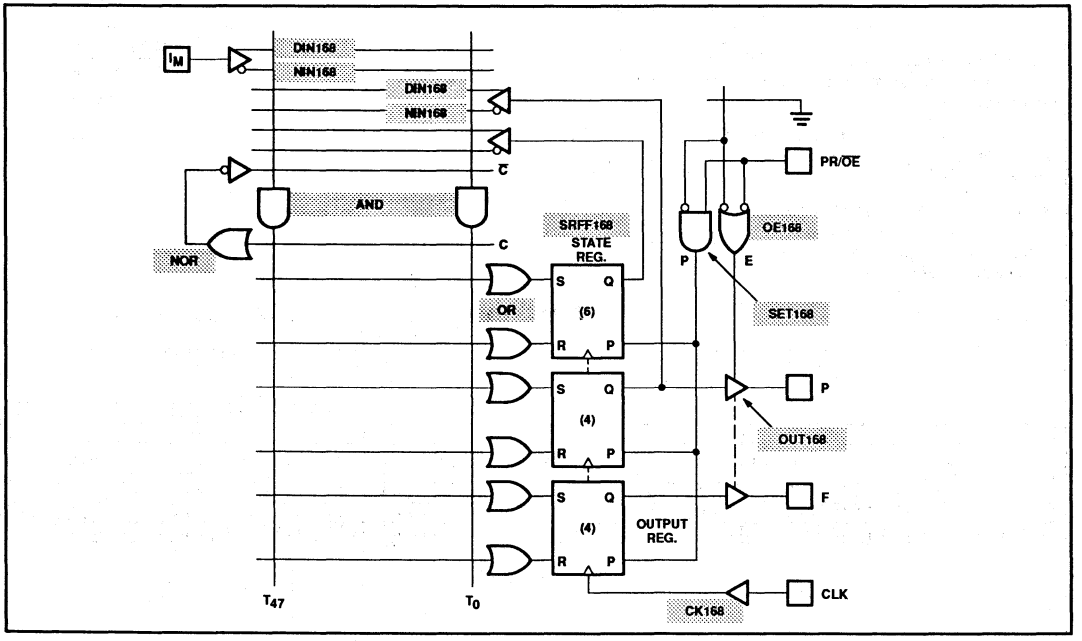


Test Circuit Timing Diagram

TERM	C_n	AND: INPUT (Im) 11 10 9 8 7 6 5 4 3 2 1 0	AND: PRESENT STATE (Ps) 9 8 7 6 5 4 3 2 1 0	OPTION (P/E) H — OR: NEXT STATE (Ns) 9 8 7 6 5 4 3 2 1 0	OR: OUTPUT (Fr) 3 2 1 0
48	–	H H H H H H H H H H H H	H H H H H H H H H H	– – – – – – – – – –	– – – –
49	•	L L L L L L L L L L L L	L L L L L L L L L L	– – – – – – – – – –	– – – –

Test Array Deleted

SNAP RESOURCE SUMMARY DESIGNATIONS



Programmable logic sequencer (20 × 45 × 12)

PLS179

DESCRIPTION

The PLS179 is a 3-State output, registered logic element combining AND/OR gate arrays with clocked J-K flip-flops. These J-K flip-flops are dynamically convertible to D-type via a "foldback" inverting buffer and control gate, F_C. It features 8 registered I/O outputs (F) in conjunction with 4 bidirectional I/O lines (B). There are 8 dedicated inputs. These yield variable I/O gate and register configurations via control gates (D, L) ranging from 20 inputs to 12 outputs.

The AND/OR arrays consist of 32 logic AND gates, 13 control AND gates, and 21 OR gates with fusible link connections for programming I/O polarity and direction. All AND gates are linked to 8 inputs (I), bidirectional I/O lines (B), internal flip-flop outputs (Q), and the Complement Array output ($\overline{C}$). The Complement Array consists of a NOR gate optionally linked to all AND gates for generating and propagating complementary AND terms.

On-chip T/C buffers couple either True (I, B, Q) or Complement ($\overline{I}$, $\overline{B}$, $\overline{Q}$, $\overline{C}$) input polarities to all AND gates, whose outputs can be optionally linked to all OR gates. Any of the 32 AND gates can drive bidirectional I/O lines (B), whose output polarity is individually programmable through a set of EX-OR gates for implementing AND-OR or AND-NOR logic functions. Similarly, any of the 32 AND gates can drive the J-K inputs of all flip-flops. Four AND gates have been dedicated for the Asynchronous Preset/Reset functions.

All flip-flops are positive edge-triggered and can be used as input, output or I/O (for interfacing with a bidirectional data bus) in conjunction with load control gates (L), steering inputs (I), (B), (Q) and programmable output select lines (E).

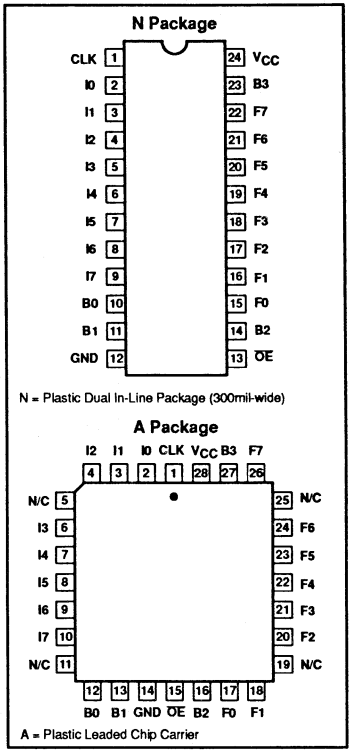
The PLS179 is field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

Order codes are listed below.

FEATURES

- f_{MAX} = 18.2MHz
  - 25MHz clock rate
- Field-Programmable (Ni-Cr link)
- 8 dedicated inputs
- 13 control gates
- 32 AND gates
- 21 OR gates
- 45 product terms:
  - 32 logic terms
  - 13 control terms
- 4 bidirectional I/O lines
- 8 bidirectional registers
- J/K, T, or D-type flip-flops
- Asynchronous Preset/Reset
- Complement Array
- Active-High or -Low outputs
- Programmable $\overline{OE}$ control
- Positive edge-triggered clock
- Power-on reset on flip-flop (F_n = "1")
- Input loading: – 100μA (max.)
- Power dissipation: 750mW (typ.)
- TTL compatible
- 3-State outputs

PIN CONFIGURATIONS



APPLICATIONS

- Random sequential logic
- Synchronous up/down counters
- Shift registers
- Bidirectional data buffers
- Timing function generators
- System controllers/synchronizers
- Priority encoder/registers

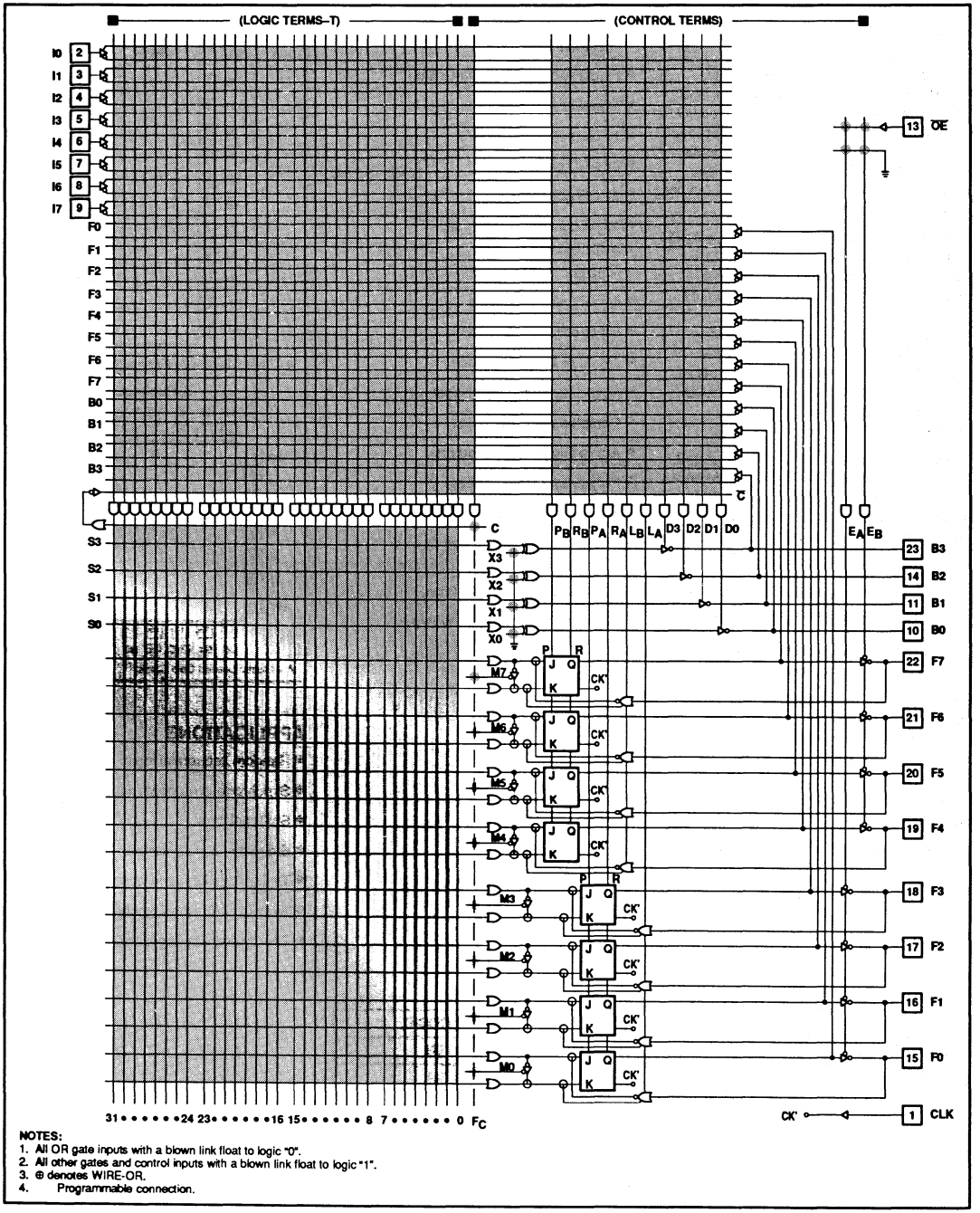
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-Pin Plastic Dual In-Line Package (300mil-wide)	PLS179N
28-Pin Plastic Leaded Chip Carrier	PLS179A

Programmable logic sequencer (20 × 45 × 12)

PLS179

LOGIC DIAGRAM

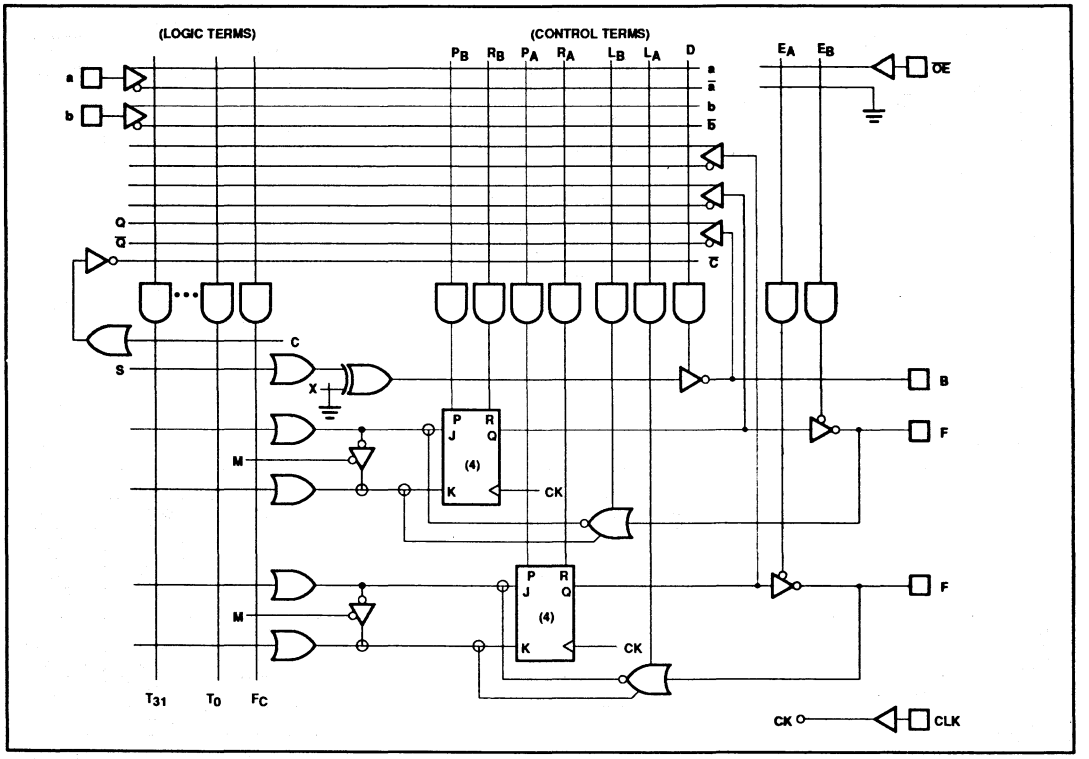


NOTES:
1. All OR gate inputs with a blown link float to logic "0".
2. All other gates and control inputs with a blown link float to logic "1".
3. ⊕ denotes WIRE-OR.
4. ▪ Programmable connection.

Programmable logic sequencer (20 × 45 × 12)

PLS179

FUNCTIONAL DIAGRAM



FLIP-FLOP TRUTH TABLE

$\overline{OE}$	L	CK	P	R	J	K	Q	F
H								H/Hi-Z
L	X	X	X	X	X	X	L	H
L	X	X	H	L	X	X	H	L
L	X	X	L	H	X	X	L	H
L	L	↑	L	L	L	L	Q	$\overline{Q}$
L	L	↑	L	L	L	H	L	H
L	L	↑	L	L	H	L	H	L
L	L	↑	L	L	H	H	$\overline{Q}$	Q
H	H	↑	L	L	L	H	L	H*
H	H	↑	L	L	H	L	H	L*
+10V	X	↑	X	X	L	H	L	H* *
	X	↑	X	X	H	L	H	L* *

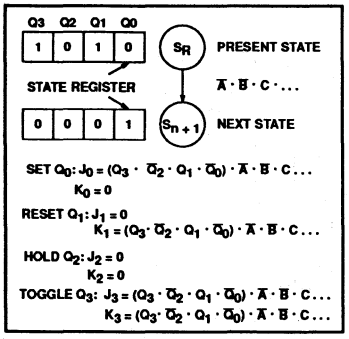
NOTES:

1. Positive Logic:
   $J\text{-}K = T_0 + T_1 + T_2 \ldots\ldots\ldots\ldots T_{31}$
   $T_n = \overline{C} \cdot (I0 \cdot I1 \cdot I2 \ldots) \cdot (Q_0 \cdot Q_1 \ldots) \cdot (B0 \cdot B1 \cdot \ldots)$
2. ↑ denotes transition from Low to High level.
3. X = Don't care
4. * = Forced at F_n pin for loading the J-K flip-flop in the Input mode. The load control term, L_n must be enabled (HIGH) and the p-terms that are connected to the associated flip-flop must be forced LOW (disabled) during Preload.
5. At P = R = H, Q = H. The final state of Q depends on which is released first.
6. * * = Forced at F_n pin to load J-K flip-flop independent of program code (Diagnostic mode), 3-State B outputs.

Programmable logic sequencer (20 × 45 × 12)

PLS179

LOGIC FUNCTION



NOTE:
Similar logic functions are applicable for D and T mode flip-flops.

VIRGIN STATE

The factory shipped virgin device contains all fusible links intact, such that:

1. $\overline{OE}$ is always enabled.
2. Preset and Reset are always disabled.
3. All transition terms are disabled.
4. All flip-flops are in D-mode unless otherwise programmed to J-K only or J-K or D (controlled).
5. All B pins are inputs and all F pins are outputs unless otherwise programmed.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS MIN	RATINGS MAX	UNIT
V_{CC}	Supply voltage		+7	V_{DC}
V_{IN}	Input voltage		+5.5	V_{DC}
V_{OUT}	Output voltage		+5.5	V_{DC}
I_{IN}	Input currents	–30	+30	mA
I_{OUT}	Output currents		+100	mA
T_{amb}	Operating temperature range	0	+75	°C
T_{stg}	Storage temperature range	–65	+150	°C

NOTES:
1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

DC ELECTRICAL CHARACTERISTICS

$0°C \leq T_{amb} \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			MIN	TYP[1]	MAX	
Input voltage[2]						
V_{IH}	High	V_{CC} = MAX	2.0			V
V_{IL}	Low	V_{CC} = Min			0.8	V
V_{IC}	Clamp	V_{CC} = MIN, I_{IN} = −12mA		−0.8	−1.2	V
Output voltage[2]						
V_{OH}	High	V_{CC} = MIN, I_{OH} = −2mA	2.4			V
V_{OL}	Low[5]	I_{OL} = 10mA		0.35	0.5	V
Input current						
I_{IH}	High	V_{CC} = MAX, V_{IN} = 5.5V		<1	40	µA
I_{IL}	Low	V_{IN} = 0.45V		−10	−100	µA
Output current						
$I_{O(OFF)}$	Hi-Z state[4, 7]	V_{CC} = MAX, V_{OUT} = 5.5V		1	80	µA
		V_{OUT} = 0.45V			−140	µA
I_{OS}	Short circuit[3, 5]	V_{OUT} = 0V	−15		−70	mA
I_{CC}	V_{CC} supply current[6]	V_{CC} = MAX		150	210	mA
Capacitance						
C_{IN}	Input	V_{CC} = 5.0V, V_{IN} = 2.0V		8		pF
C_{OUT}	Output	V_{OUT} = 2.0V		15		pF

NOTES:
1. All typical values are at V_{CC} = 5V, T_{amb} = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Test one at a time.
4. Measured with V_{IH} applied to $\overline{OE}$.
5. Duration of short circuit should not exceed 1 second.
6. I_{CC} is measured with the $\overline{OE}$ input grounded, all other inputs at 4.5V and the outputs open.
7. Leakage values are a combination of input and output leakage.

Programmable logic sequencer (20 × 45 × 12)

PLS179

AC ELECTRICAL CHARACTERISTICS

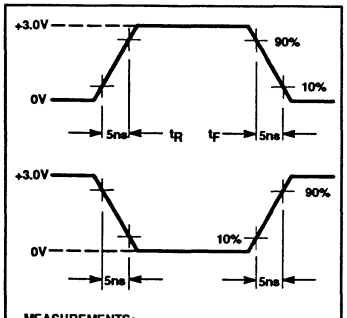
$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0°C \leq T_{amb} \leq +75°C$, $4.75°CV \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	FROM	TO	TEST CONDITION	LIMITS MIN[5]	LIMITS TYP[1]	LIMITS MAX	UNIT
Pulse width[3]								
t_{CKH}	Clock[2] High	CK +	CK –	$C_L = 30pF$	20	15		ns
t_{CKL}	Clock Low	CK –	CK +	$C_L = 30pF$	20	15		ns
t_{CKP}	Clock period	CK +	CK +	$C_L = 30pF$	40	30		ns
t_{PRH}	Preset/Reset pulse	(I, B) –	(I, B) +	$C_L = 30pF$	35	30		ns
Setup time								
t_{IS1}	Input	(I, B) ±	CK +	$C_L = 30pF$	35	30		ns
t_{IS2}	Input (through F_n)	F ±	CK +	$C_L = 30pF$	15	10		ns
t_{IS3}	Input (through Complement Array)[4]	(I, B) ±	CK +	$C_L = 30pF$	55	45		ns
Hold time								
t_{IH1}	Input	(I, B) ±	CK +	$C_L = 30pF$	0	–5		ns
t_{IH2}	Input (through F_n)	F ±	CK +	$C_L = 30pF$	15	10		ns
Propagation delay								
t_{CKO}	Clock	CK ±	F ±	$C_L = 30pF$		15	20	ns
t_{OE1}	Output enable[3]	$\overline{OE}$ –	F –	$C_L = 30pF$		20	30	ns
t_{OD1}	Output disable[3]	$\overline{OE}$ +	F +	$C_L = 5pF$		20	30	ns
t_{PD}	Output	(I, B) ±	B ±	$C_L = 30pF$		25	35	ns
t_{OE2}	Output enable[3]	(I, B) +	B ±	$C_L = 30pF$		20	30	ns
t_{OD2}	Output disable[3]	(I, B) –	B +	$C_L = 5pF$		20	30	ns
t_{PRO}	Preset/Reset	(I, B) +	F ±	$C_L = 30pF$		35	45	ns
t_{PPR}	Power-on preset	V_{CC} +	F –	$C_L = 30pF$		0	10	ns

NOTES:

1. All typical values are at $V_{CC} = 5V$, $T_{amb} = +25°C$.
2. To prevent spurious clocking, clock rise time (10% – 90%) ≤ 10ns.
3. For 3-State output; output enable times are tested with $C_L = 30pF$ to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with $C_L = 5pF$. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} – 0.5V)$ with S_1 open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with S_1 closed.
4. When using the Complement Array $t_{CKP} = 75ns$ (min).
5. Limits are guaranteed with 12 product terms maximum connected to each sum term line.

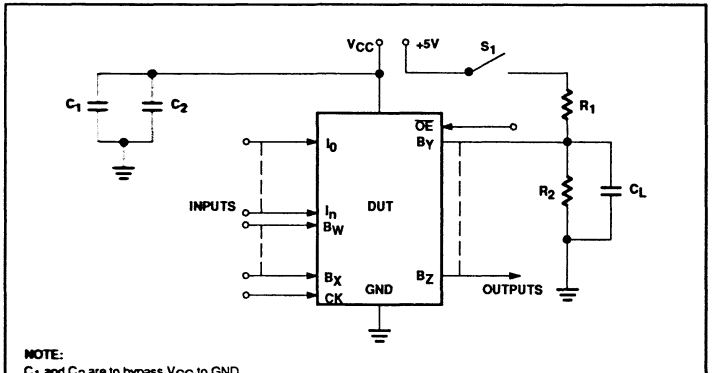
VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

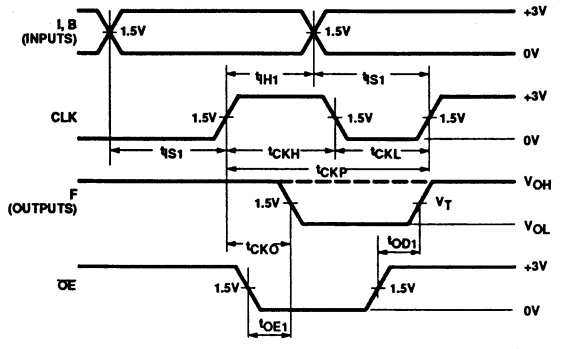
Input Pulses

TEST LOAD CIRCUIT

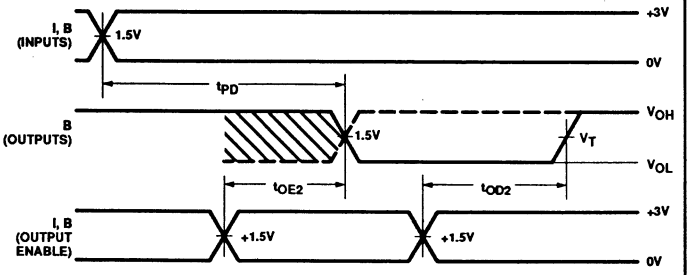


NOTE:
C_1 and C_2 are to bypass V_{CC} to GND.

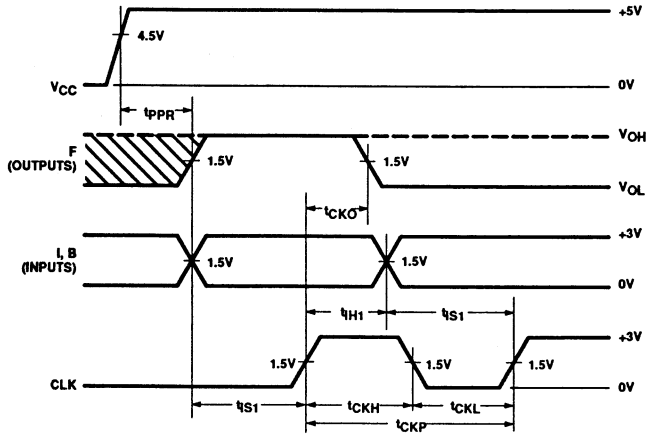
TIMING DIAGRAMS



Flip-Flop Outputs



Gate Outputs

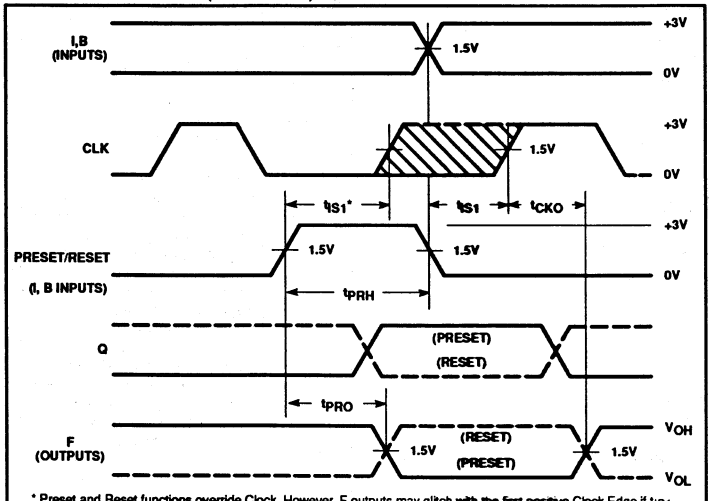


Power-On Reset

TIMING DEFINITIONS

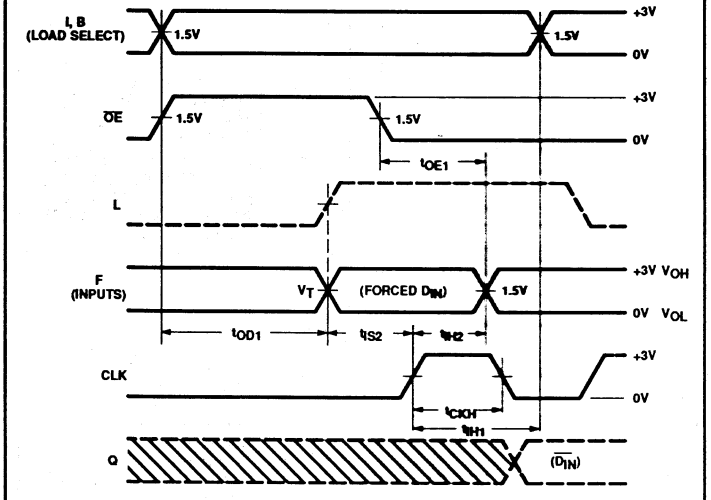
SYMBOL	PARAMETER
t_{CKH}	Width of input clock pulse.
t_{CKL}	Interval between clock pulses.
t_{CKP}	Minimum guaranteed Clock period.
t_{PRH}	Width of preset input pulse.
t_{IS1}	Required delay between beginning of valid input and positive transition of clock.
t_{IS2}	Required delay between beginning of valid input forced at flip-flop output pins, and positive transition of clock.
t_{IH1}	Required delay between positive transition of clock and end of valid input data.
t_{IH2}	Required delay between positive transition of clock and end of valid input data forced at flip-flop output pins.
t_{CKO}	Delay between positive transition of clock and when outputs become valid (with $\overline{OE}$ Low).
t_{OE1}	Delay between beginning of Output Enable Low and when outputs become valid.
t_{OD1}	Delay between beginning of Output Enable High and when outputs are in the OFF-State.
t_{PPR}	Delay between V_{CC} (after power-on) and when flip-flop outputs become preset at "1" (internal Q outputs at "0").
t_{PD}	Propagation delay between combinational inputs and outputs.
t_{OE2}	Delay between predefined Output Enable High, and when combinational Outputs become valid.
t_{OD2}	Delay between predefined Output Enable Low and when combinational Outputs are in the OFF-State.
t_{PRO}	Delay between positive transition of predefined Preset/Reset input, and when flip-flop outputs become valid.

TIMING DIAGRAMS (Continued)



* Preset and Reset functions override Clock. However, F outputs may glitch with the first positive Clock Edge if t_{IS1} cannot be guaranteed by the user.

Asynchronous Preset/Reset



Flip-Flop Input Mode

Programmable logic sequencer (20 x 45 x 12)

PLS179

LOGIC PROGRAMMING

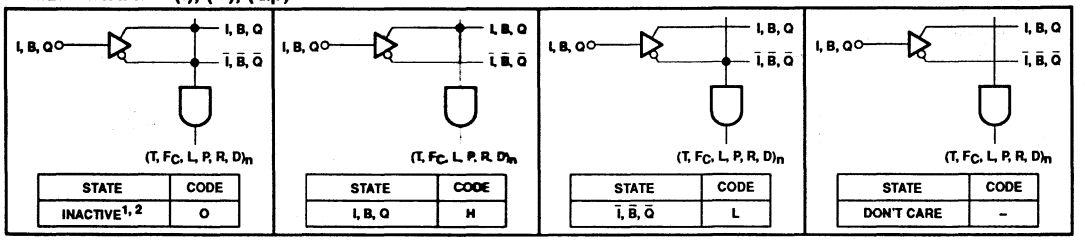
The PLS179 is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Signetics' SNAP and SLICE, Data I/O Corporation's ABEL™; and Logical Devices Inc.'s CUPL™ design software packages.

All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

PLS179 logic designs can also be generated using the program table entry format detailed on the following pages. This program table entry format is supported by the Signetics SNAP and SLICE PLD design software packages (PTP module). SLICE is available free of charge to qualified users.

To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

"AND" ARRAY – (I), (B), (Qp)



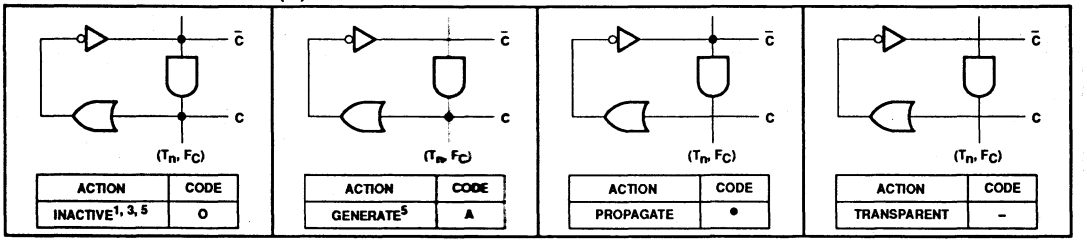
STATE	CODE
INACTIVE[1, 2]	O

STATE	CODE
I, B, Q	H

STATE	CODE
Ī, B̄, Q̄	L

STATE	CODE
DON'T CARE	–

"COMPLEMENT" ARRAY – (C)



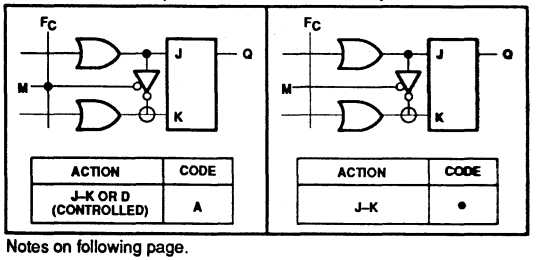
ACTION	CODE
INACTIVE[1, 3, 5]	O

ACTION	CODE
GENERATE[5]	A

ACTION	CODE
PROPAGATE	•

ACTION	CODE
TRANSPARENT	–

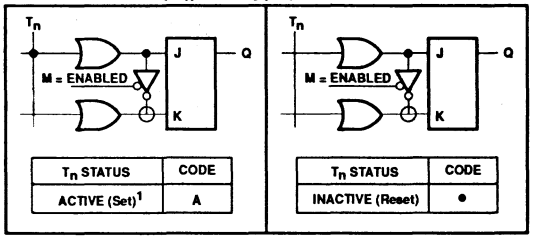
"OR" ARRAY – (F-F CONTROL MODE)



ACTION	CODE
J–K OR D (CONTROLLED)	A

ACTION	CODE
J–K	•

"OR" ARRAY – (Q_n = D-Type)



T_n STATUS	CODE
ACTIVE (Set)[1]	A

T_n STATUS	CODE
INACTIVE (Reset)	•

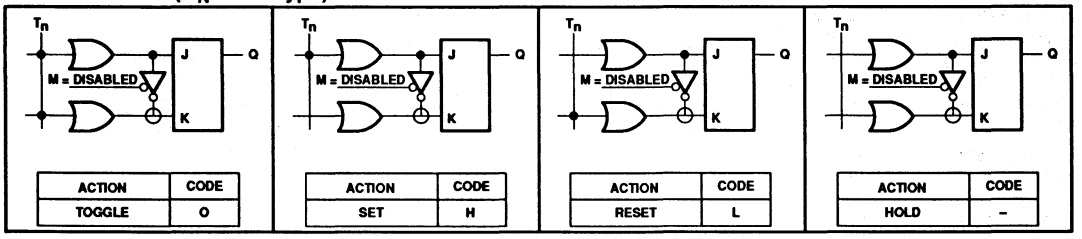
Notes on following page.

ABEL is a trademark of Data I/O Corp.
CUPL is a trademark of Logical Devices, Inc.

Programmable logic sequencer (20 × 45 × 12)

PLS179

"AND" ARRAY – (Q_N = J-K Type)



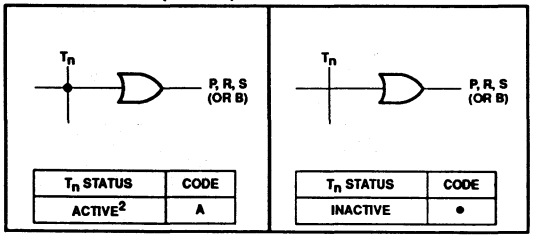
ACTION	CODE
TOGGLE	O

ACTION	CODE
SET	H

ACTION	CODE
RESET	L

ACTION	CODE
HOLD	–

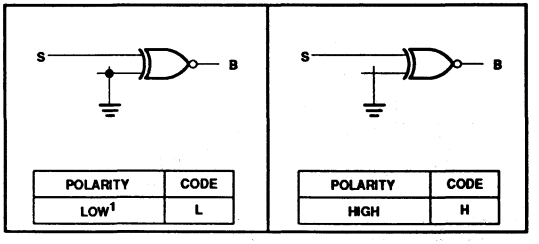
"OR" ARRAY – (S or B)



T_n STATUS	CODE
ACTIVE[2]	A

T_n STATUS	CODE
INACTIVE	•

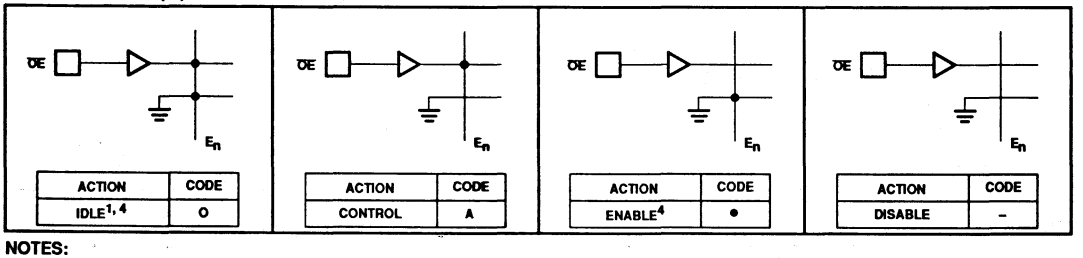
"EX-OR" ARRAY – (B)



POLARITY	CODE
LOW[1]	L

POLARITY	CODE
HIGH	H

"$\overline{OE}$" ARRAY – (E)



ACTION	CODE
IDLE[1, 4]	O

ACTION	CODE
CONTROL	A

ACTION	CODE
ENABLE[4]	•

ACTION	CODE
DISABLE	–

NOTES:
1. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates.
2. Any gate $(T, F_C, L, P, R, D)_n$ will be unconditionally inhibited if any one of the I, B, or Q link pairs are left intact.
3. To prevent oscillations, this state is not allowed for C link pairs coupled to active gates T_n, F_C.
4. E_n = O and E_n = • are logically equivalent states, since both cause F_n outputs to be unconditionally enabled.
5. These states are not allowed for control gates $(L, P, R, D)_n$ due to their lack of "OR" array links.

Programmable logic sequencer (20 × 45 × 12)

PLS179

PROGRAM TABLE

AND

INACTIVE	O
I, B, Q	H
$\overline{I}$, $\overline{B}$, $\overline{Q}$	L
DON'T CARE	–

I, B(I), Q(P)

INACTIVE	O
GENERATE	A
PROPAGATE	•
TRANSPARENT	–

C

OR

ACTIVE	A
INACTIVE	•

P, R, B(O) (Q = D)

TOGGLE	O
SET	H
RESET	L
HOLD	–

(Q = J/K)

CONTROL

J/K	•
J/K or D (controlled)	A

F/F MODE

IDLE	0
CONTROL	A
ENABLE	•
DISABLE	–

$E_{A, B}$

HIGH	H
LOW	L

(POL)

NOTES

1. The device is shipped with all links intact. Thus a background of entries corresponding to states of virgin links exists in the table, shown BLANK for clarity.
2. Program unused C, I, B, and Q bits in the AND array as (–). Program unused Q, B, P, and R bits in the OR array as (–) or (A), as applicable.
3. Unused Terms can be left blank.
4. Q (P) and Q (N) are respectively the present and next states of flip-flops Q.

THIS PORTION TO BE COMPLETED BY SIGNETICS

CF (XXXX) _____ CUSTOMER SYMBOLIZED PART # _____ DATE RECEIVED _____ COMMENTS _____

CUSTOMER NAME _____ PURCHASE ORDER # _____ SIGNETICS DEVICE # _____ TOTAL NUMBER OF PARTS _____ PROGRAM TABLE # _____ REV ____ DATE ____

TERM	C	AND I 7	6	5	4	3	2	1	0	AND B(I) 3	2	1	0	AND Q(P) 7	6	5	4	3	2	1	0	F/F MODE	E_B	E_A	(OR) Q(N) 7	6	5	4	3	2	1	0	POLARITY (OR) B(O) 3	2	1	0
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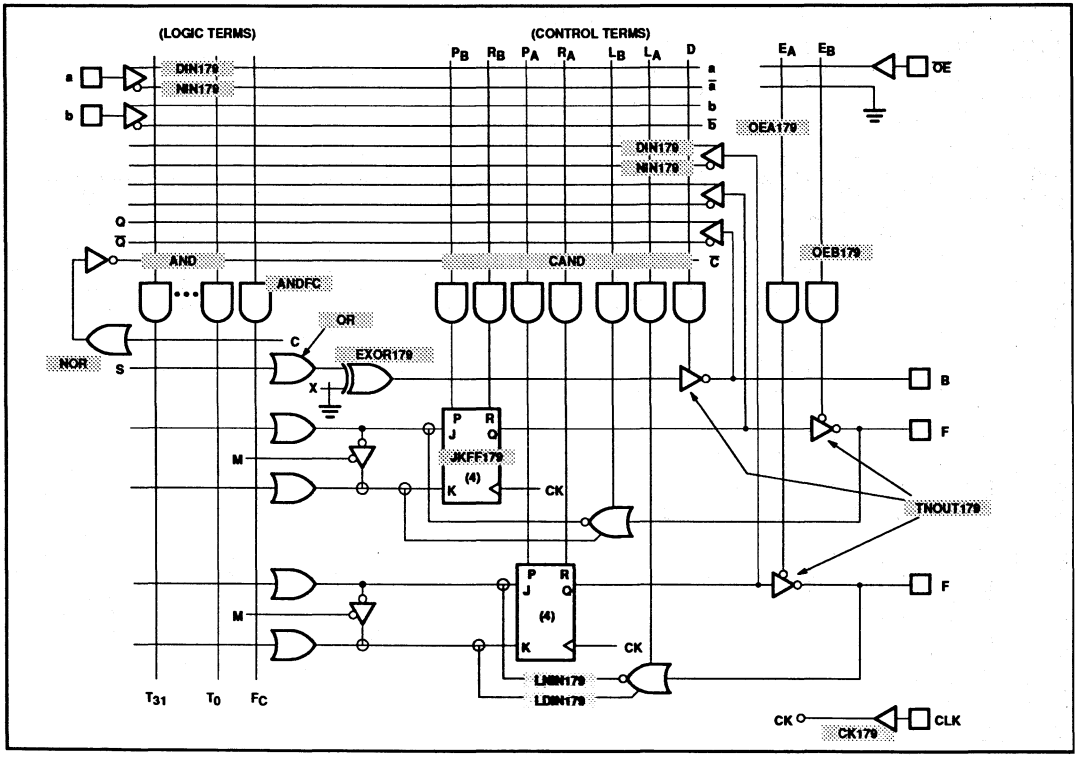
R_A																																			
L_A																																			
D3																																			
D2																																			
D1																																			
D0																																			
PIN		9	8	7	6	5	4	3	2	23	14	11	10	22	21	20	19	18	17	16	15														

Programmable logic sequencer (20 × 45 × 12) PLS179

SNAP RESOURCE SUMMARY DESIGNATIONS



CMOS programmable multi-function PLD (42 × 105 × 12)

PLC42VA12

DESCRIPTION

The new PLC42VA12 CMOS PLD from Signetics exhibits a unique combination of the two architectural concepts that revolutionized the PLD marketplace.

The Signetics unique Output Macro Cell (OMC) embodies all the advantages and none of the disadvantages associated with the "V" type Output Macro Cell devices. This new design, combined with added functionality of two programmable arrays, represents a significant advancement in the configurability and efficiency of multi-function PLDs.

The most significant improvement in the Output Macro Cell structure is the implementation of the register bypass function. Any of the 10 J-K/D registers can be individually bypassed, thus creating a combinatorial I/O path from the AND array to the output pin. Unlike other "V" type devices, the register in the PLC42VA12 Macro Cell remains fully functional as a buried register. Both the combinatorial I/O and buried register have separate input paths (from the AND array). In most V-type architectures, the register is lost as a resource when the cell is configured as a combinatorial I/O. This feature provides the capability to operate the buried register independently from the combinatorial I/O.

The PLC42VA12 is an EPROM-based CMOS device. Designs can be generated using Signetics SNAP and SLICE PLD design software packages or one of several other commercially available JEDEC standard PLD design software packages.

FEATURES

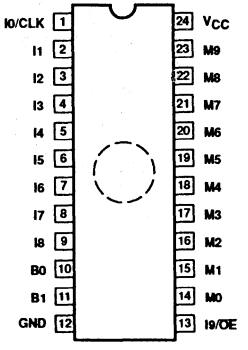
- High-speed EPROM-based CMOS Multi-Function PLD
  - Super set of 22V10, 32VX10 and 20RA10 PAL® ICs
- Two fully programmable arrays eliminate "P-term Depletion"
  - Up to 64 P-terms per OR function
- Improved Output Macro Cell Structure
  - Individually programmable as:
    - Registered Output with feedback
    - Registered Input
    - Combinatorial I/O with Buried Register
    - Dedicated I/O with feedback
    - Dedicated Input (combinatorial)
  - Bypassed Registers are 100% functional with separate input and feedback paths
  - Individual Output Enable control functions
    - From pin or AND array
- Reprogrammable – 100% tested for programmability
- Eleven clock sources
- Register Preload and Diagnostic Test Mode Features
- Security fuse

APPLICATIONS

- Mealy or Moore State Machines
  - Synchronous
  - Asynchronous
- Multiple, independent State Machines
- 10-bit ripple cascade
- Sequence recognition
- Bus Protocol generation
- Industrial control
- A/D Scanning

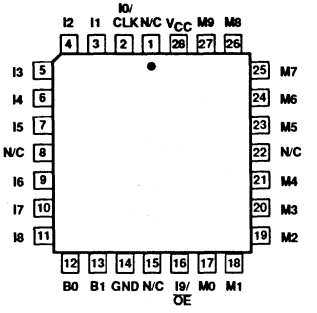
PIN CONFIGURATIONS

FA and N Packages



N = Plastic DIP (300mil-wide)
FA = Ceramic DIP with Quartz Window (300mil-wide)

A Package



A = Plastic Leaded Chip Carrier (450mil-square)

ORDERING INFORMATION

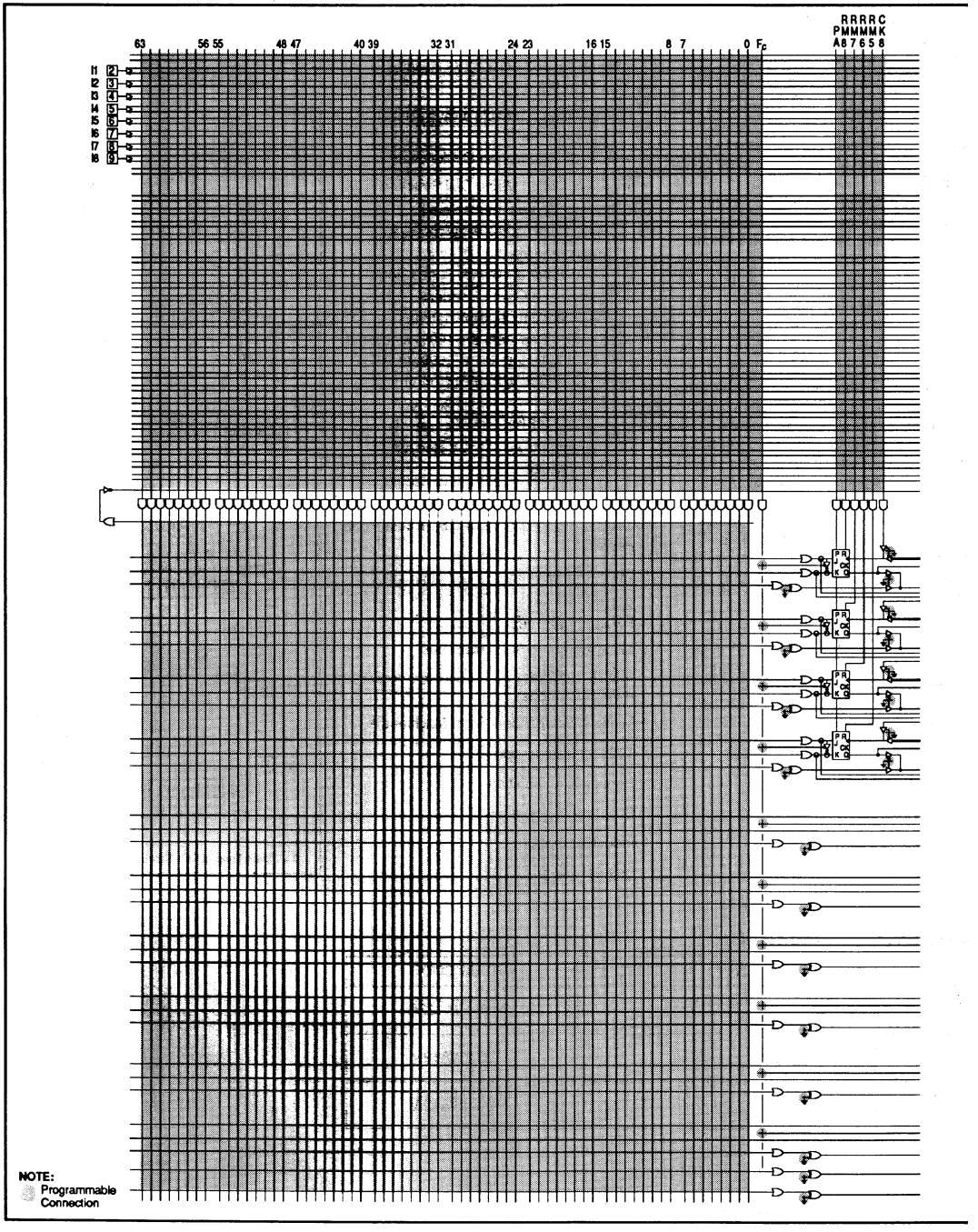
DESCRIPTION	ORDER CODE
24-Pin Ceramic Dual In-Line with window, Reprogrammable (300mil-wide)	PLC42VA12FA
24-Pin Plastic Dual In-Line, One Time Programmable (300mil-wide)	PLC42VA12N
28-Pin Plastic Leaded Chip Carrier, One Time Programmable (450mil-wide)	PLC42VA12A

PAL is a registered trademark of Advanced Micro Devices, Inc.

CMOS programmable multi-function PLD (42 × 105 × 12)

PLC42VA12

LOGIC DIAGRAM

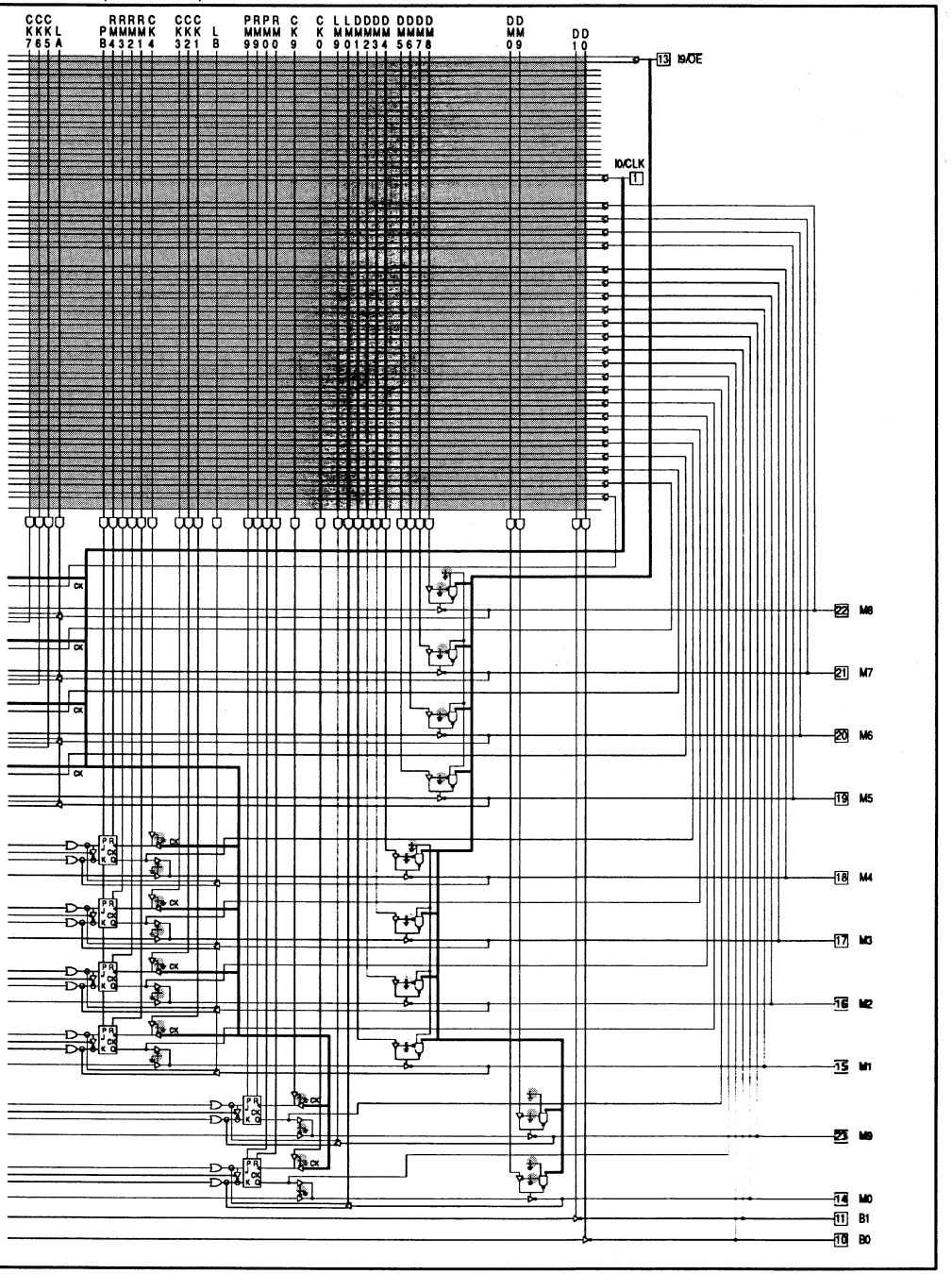


NOTE:
Programmable Connection

CMOS programmable multi-function PLD (42 x 105 x 12)

PLC42VA12

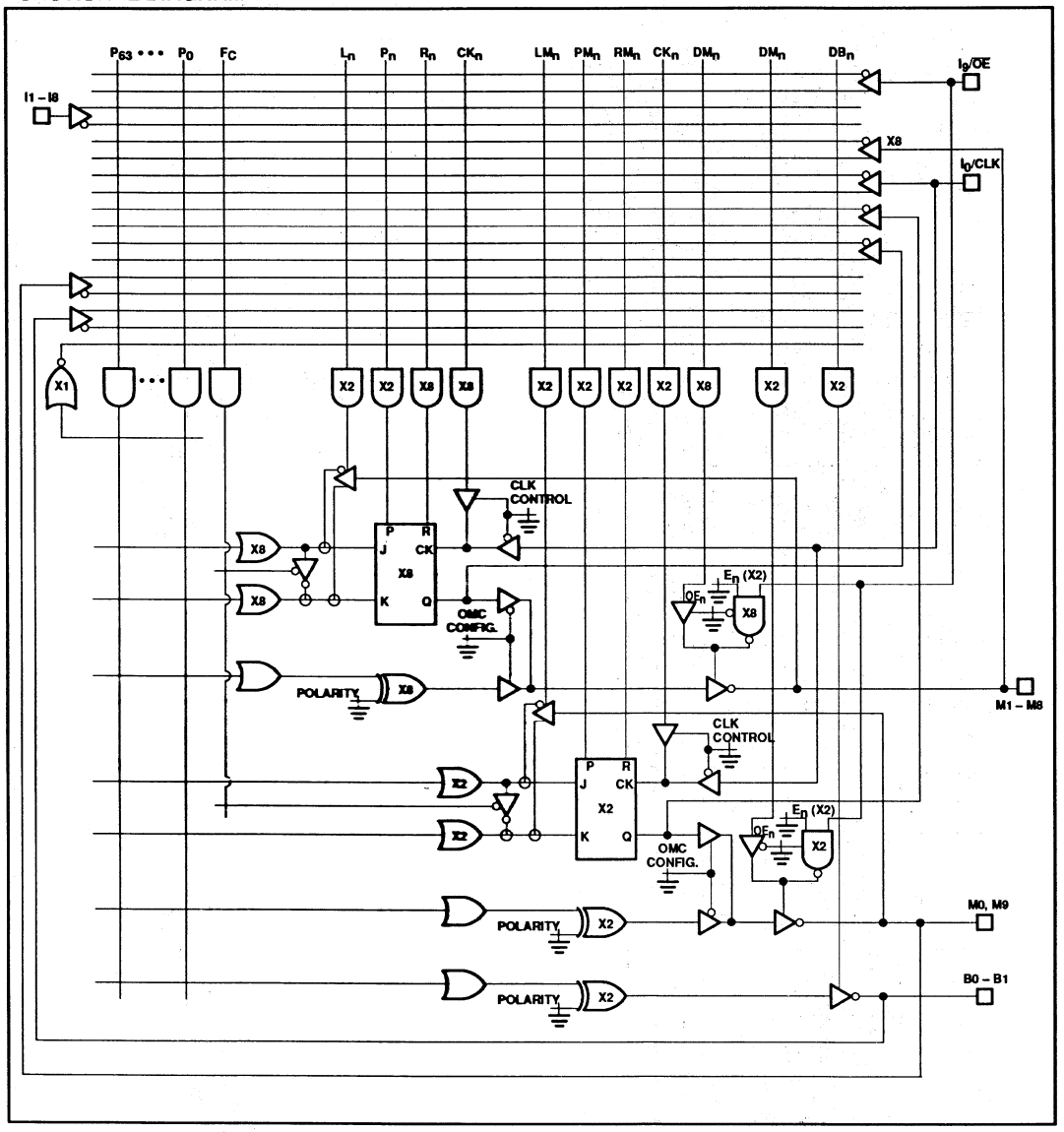
LOGIC DIAGRAM (Continued)



CMOS programmable multi-function PLD (42 × 105 × 12)

PLC42VA12

FUNCTIONAL DIAGRAM



CMOS programmable multi-function PLD (42 × 105 × 12)

PLC42VA12

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS	UNIT
V_{CC}	Supply voltage	–0.5 to +7	V_{DC}
V_{IN}	Input voltage	–0.5 to V_{CC} +0.5	V_{DC}
V_{OUT}	Output voltage	–0.5 to V_{CC} +0.5	V_{DC}
I_{IN}	Input currents	–10 to +10	mA
I_{OUT}	Output currents	+24	mA
T_{amb}	Operating temperature range	0 to +75	°C
T_{stg}	Storage temperature range	–65 to +150	°C

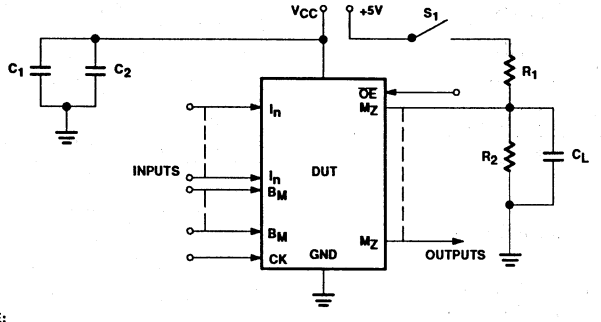
NOTE:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

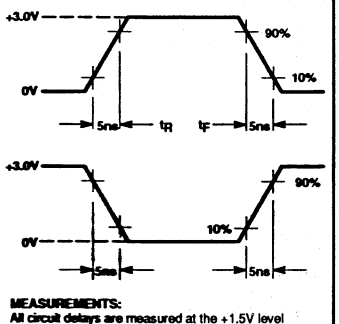
AC TEST CONDITIONS



NOTE:
C_1 and C_2 are to bypass V_{CC} to GND.

Test Load Circuit

VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

DC ELECTRICAL CHARACTERISTICS

$0°C \le T_{amb} \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			MIN	TYP[1]	MAX	
Input voltage[2]						
V_{IL}	Low	V_{CC} = MIN	–0.3		0.8	V
V_{IH}	High	V_{CC} = MAX	2.0		V_{CC} + 0.3	V
Output voltage[2]						
V_{OL}	Low	V_{CC} = MIN; I_{OL} = 16mA		0.3	0.5	V
V_{OH}	High	V_{CC} = MIN; I_{OH} = –3.2mA	2.4	4.3		V
Input current						
I_{IL}	Low	V_{IN} = GND		–1	–10	µA
I_{IH}	High	V_{IN} = V_{CC}		+1	10	µA
Output current						
$I_{O(OFF)}$	Hi-Z state	V_{OUT} = V_{CC} V_{OUT} = GND		1 –1	10 –10	µA µA
I_{OS}	Short-circuit[3,7]	V_{OUT} = GND			–130	mA
I_{CC1}	V_{CC} supply current (Active)[4]	I_{OUT} = 0mA, f = 15MHz[6], V_{CC} = MAX		90	120	mA
I_{CC2}	V_{CC} supply current (Active)[5]	I_{OUT} = 0mA, f = 15MHz[6], V_{CC} = MAX		70	100	mA
Capacitance						
C_I	Input	V_{CC} = 5V; V_{IN} = 2.0V		12		pF
C_B	I/O	V_B = 2.0V		15		pF

NOTES:

1. All typical values are at V_{CC} = 5V. T_{amb} = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Duration of short–circuit should not exceed one second. Test one at a time.
4. Tested with V_{IL} = 0.45V, V_{IH} = 2.4V.
5. Tested with V_{IL} = 0V, V_{IH} = V_{CC}.
6. Refer to Figure 1, ΔI_{CC} vs Frequency (worst case). (Referenced from 15MHz)
   The I_{CC} increases by 1.5mA per MHz for the frequency range of 16MHz up to 25MHz.
   The I_{CC} remains at a worst case for the frequency range of 26MHz up to 37MHz.
   The I_{CC} decreases by 1.0mA per MHz for the frequency range of 14MHz down to 1MHz.
   The worst case I_{CC} is calculated as follows:
   - All dedicated inputs are switching.
   - All OMCs are configured as JK flip-flops in the toggle mode. . .all are toggling.
   - All 12 outputs are disabled.
   - The number of product terms connected does not impact the I_{CC}.
7. Refer to Figure 2 for Δt_{PD} vs output capacitance loading.

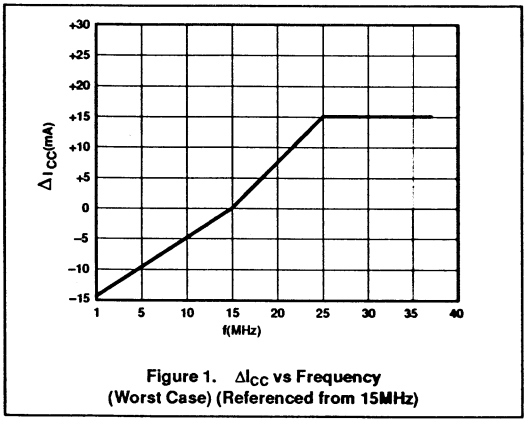


Figure 1. ΔI_{CC} vs Frequency (Worst Case) (Referenced from 15MHz)

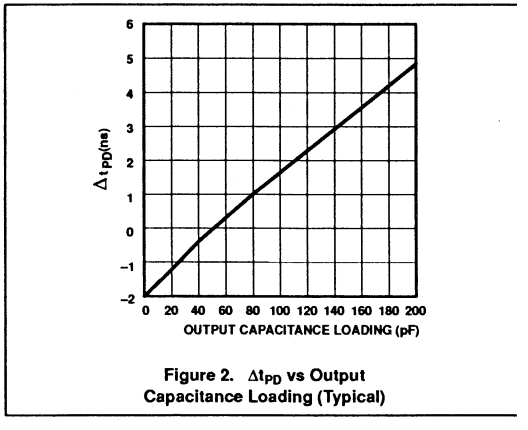


Figure 2. Δt_{PD} vs Output Capacitance Loading (Typical)

AC ELECTRICAL CHARACTERISTICS

$0°C \le T_{amb} \le +75°C$, $4.75V \le V_{CC} \le 5.25V$; $R_1 = 238\Omega$, $R_2 = 170\Omega$

SYMBOL	PARAMETER	FROM	TO	TEST[2] CONDITION (C_L (pF))	PLC42VA12 MIN	PLC42VA12 TYP[1]	PLC42VA12 MAX	UNIT
Set-up Time								
t_{IS1}	Input; dedicated clock	(I, B, M) +/–	CK+	50	23	16		ns
t_{IS2}	Input; P-term clock	(I, B, M) +/–	(I, B, M) +/–	50	20	13		ns
t_{IS3}[3]	Preload; dedicated clock	(M) +/–	CK+	50	10	3.5		ns
t_{IS4}[3]	Preload; P-term clock	(M) +/–	(I, B, M) +/–	50	2	–1.0		ns
t_{IS5}[3]	Input through complement array; dedicated clock	(I, B, M) +/–	CK+	50	50	34		ns
t_{IS6}[3]	Input through complement array; P-term clock	(I, B, M) +/–	(I, B, M) +/–	50	40	30		ns
Propagation Delay								
t_{PD1}	Propagation Delay	(I, B, M) +/–	(I, B, M) +/–	50		20	35	ns
t_{PD2}	Propagation Delay with complement array (2 passes)	(I, B,) +/–	(I, B, M) +/–	50		36	55	ns
t_{CKO1}	Clock to Output; Dedicated clock	CK+	(M) +/–	50		13	17	ns
t_{CKO2}	Clock to output; P-term clock	(I, B, M) +/–	(M) +/–	50		18	27	ns
t_{RP1}	Registered operating period; Dedicated clock ($t_{IS1} + t_{CKO1}$)	(I, B, M) +/–	(M) +/–	50		29	40	ns
t_{RP2}	Registered operating period; P-term clock ($t_{IS2} + t_{CKO2}$)	(I, B, M) +/–	(M) +/–	50		31	47	ns
t_{RP3}[3]	Register preload operating period; Dedicated clock ($t_{IS3} + t_{CKO1}$)	(M) +/–	(M) +/–	50		16.5	27	ns
t_{RP4}[3]	Register preload operating period; P-term clock ($t_{IS4} + t_{CKO2}$)	(M) +/–	(M) +/–	50		17	29	ns
t_{RP5}[3]	Registered operating period with complement array; dedicated clock ($t_{IS5} + t_{CKO1}$)	(I, B, M) +/–	(M) +/–	50		47	67	ns
t_{RP6}[3]	Registered operating period with complement array; P-term clock ($t_{IS6} + t_{CKO2}$)	(I, B, M) +/–	(M) +/–	50		48	67	ns
t_{OE1}	Output Enable; from /OE pin[4]	/OE –	(M) +/–	50		10	20	ns
t_{OE2}	Output Enable; from P-term[4]	(I, B, M) +/–	(B, M) +/–	50		12.5	25	ns
t_{OD1}	Output Disable; from /OE pin[4]	/OE +	Outputs disabled	5		10	20	ns
t_{OD2}	Output Disable; from P-term[4]	(I, B, M) +/–	Outputs disabled	5		14.5	25	ns
t_{PRO}[3]	Preset to Output	(I, B, M) +/–	(M) +/–	50		25	35	ns
t_{PPR}[3]	Power-on Reset (Mn = 1)	V_{CC} +	(M) +/–	50			15	ns
Hold Time								
t_{IH1}	Input (Dedicated clock)	CK+	(I, B, M) +/–	50	0	–13		ns
t_{IH2}	Input (P-term clock)	(I, B, M) +/–	(I, B, M) +/–	50	5	–7.5		ns
t_{IH3}[3]	Input; from Mn (Dedicated clock)	CK+	(M) +/–	50	5	–1.5		ns
t_{IH4}[3]	Input; from Mn (P-term clock)	(I, B, M) +/–	(M) +/–	50	10	3.5		ns
Pulse Width								
t_{CKH1}	Clock High; Dedicated clock	CK+	CK–	50	10	5		ns
t_{CKL1}	Clock Low; Dedicated clock	CK–	CK+	50	10	5		ns
t_{CKH2}	Clock High; P-term clock	CK+	CK–	50	15	7		ns
t_{CKL2}	Clock Low; P-term clock	CK–	CK+	50	15	7		ns
t_{PRH}[3]	Width of preset/reset input pulse	(I, B, M) +/–	(I, B, M) +/–	50	30	7		ns

Notes on page 332.

AC ELECTRICAL CHARACTERISTICS (Continued)

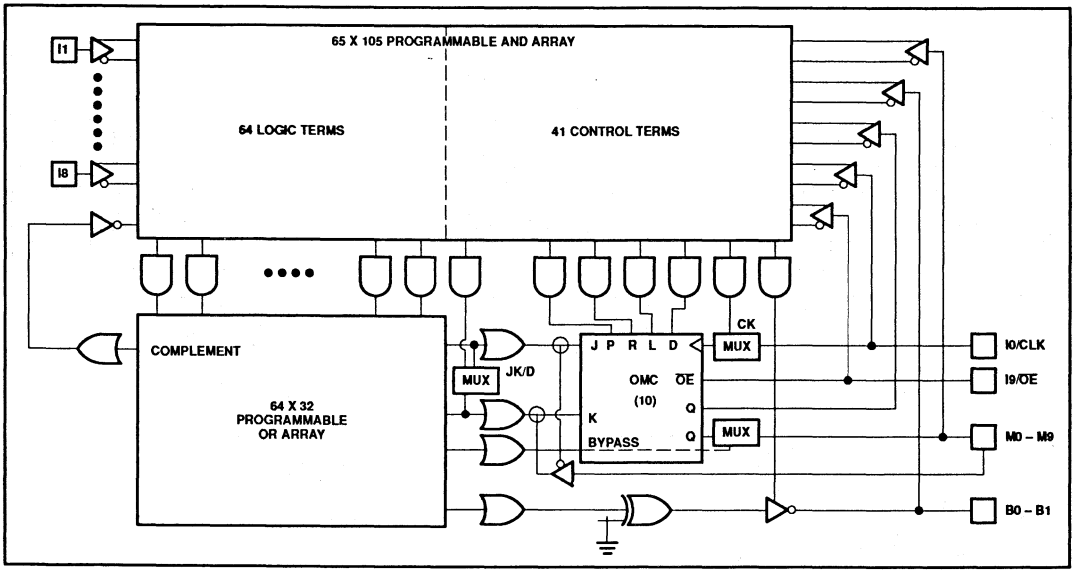
$0°C \le T_{amb} \le +75°C$, $4.75V \le V_{CC} \le 5.25V$; $R_1 = 238\Omega$, $R_2 = 170\Omega$

SYMBOL	PARAMETER	FROM	TO	TEST[2] CONDITION (C_L (pF))	PLC42VA12 MIN	PLC42VA12 TYP[1]	PLC42VA12 MAX	UNIT
Frequency of Operation								
f_{CK1}	Dedicated clock frequency	C+	C+	50	50	100		MHz
f_{CK2}	P-term clock frequency	C+	C+	50	33	71.4		MHz
f_{MAX1}	Registered operating frequency; Dedicated clock ($t_{IS1} + t_{CKO1}$)	(I, B, M) +/–	(M) +/–	50	25	34.5		MHz
f_{MAX2}	Registered operating frequency; P-term clock ($t_{IS2} + t_{CKO2}$)	(I, B, M) +/–	(M) +/–	50	21.3	32.3		MHz
f_{MAX3}[3]	Register preload operating frequency; Dedicated clock ($t_{IS3} + t_{CKO1}$)	(M) +/–	(M) +/–	50	37	60.6		MHz
f_{MAX4}[3]	Register preload operating frequency; P-term clock ($t_{IS4} + t_{CKO2}$)	(M) +/–	(M) +/–	50	34.5	58.8		MHz
f_{MAX5}[3]	Registered operating frequency with complement array; Dedicated clock ($t_{IS5} + t_{CKO1}$)	(I, B, M) +/–	(M) +/–	50	14.9	21.3		MHz
f_{MAX6}[3]	Registered operating frequency with complement array; P-term clock ($t_{IS6} + t_{CKO2}$)	(I, B, M) +/–	(M) +/–	50	14.9	20.8		MHz

NOTES:

1. All typical values are at $V_{CC} = 5V$, $T_{amb} = +25°C$. These limits are not tested/guaranteed.
2. Refer also to AC Test Conditions (Test Load Circuit).
3. These limits are not tested, but are characterized periodically and are guaranteed by design.
4. For 3-State output; output enable times are tested with $C_L = 50pF$ to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with $C_L = 5pF$. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} - 0.5V)$ with S_1 open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with S_1 closed.

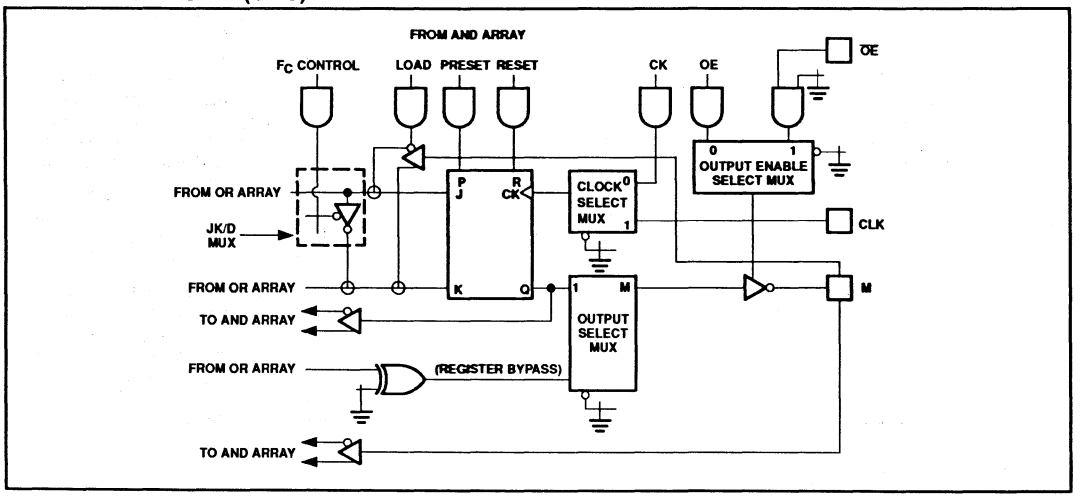
BLOCK DIAGRAM



CMOS programmable multi-function PLD (42 × 105 × 12)

PLC42VA12

OUTPUT MACRO CELL (OMC)



Output Macro Cell Configuration

Signetics unique Output Macro Cell design represents a significant advancement in the configurability of multi-function Programmable Logic Devices.

The PLC42VA12 has 10 programmable Output Macro Cells. Each can be individually programmed in any of 5 basic configurations:

- Dedicated I/O (combinatorial) with feedback to AND array
- Dedicated Input
- Combinatorial I/O with feedback and Buried Register with feedback (register bypass)
- Registered Input
- Registered Output with feedback

Each of the registered options can be further customized as J-K type or D-type, with either an internally derived clock (from the AND array) or clocked from an external source. With these additional programmable options, it is possible to program each Output Macro Cell in any one of 14 different configurations.

These 14 configurations, combined with the fully programmable OR array, make the PLC42VA12 the most versatile and silicon efficient of all the Output Macro Cell-type PLDs.

The most significant Output Macro Cell (OMC) feature is the implementation of the register bypass function. Any of the 10 J-K/D registers can be individually bypassed, thus creating a combinatorial I/O path from the AND array to the output pin. Unlike other Output Macro Cell-type devices, the register in the OMC is fully functional as a buried register. Furthermore, both the combinatorial I/O and the buried register have separate input paths (from the AND array) and separate feedback paths (to the AND array). This feature provides the capability to operate the buried register independently from the combinatorial I/O.

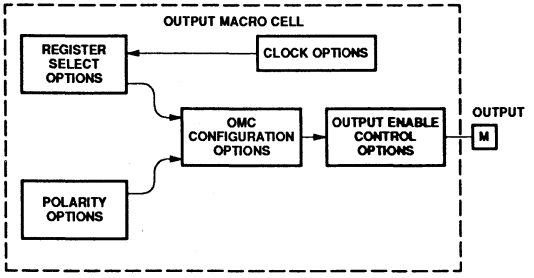
The PLC42VA12 is ideally suited for both synchronous and asynchronous logic functions. Eleven clock sources – 10 driven from the AND array and one from an external source – make it possible to design synchronous state machine functions, event-driven state machine functions and combinatorial (asynchronous) functions all on the same chip.

Sophisticated control functions support individual OE control and Reset functions from the AND array. OE control is also available from the I9/$\overline{OE}$ pin. Register Preset and Load functions are controlled from the AND array, in 2 banks of 4 for OMCs M1 – M8. Output Macro Cells M0 and M9 have individual Preset and Load Control terms.

Output Polarity for the combinatorial I/O paths is configurable via 12 programmable EX-OR gates. The output of each register can be configured as inverting (active Low) or non-inverting (active High) via manipulation of the logic equations.

The output of each buried register can also be configured as inverting or non-inverting via the input buffer which feeds back to the AND array.

OUTPUT MACRO CELL PROGRAMMABLE OPTIONS



OMC Programmable Options

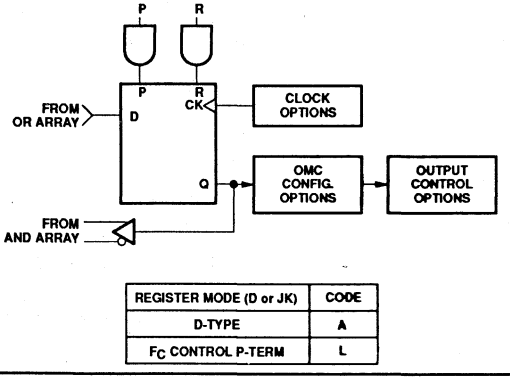
For purposes of programming, the Output Macro Cell should be considered to be partitioned into five separate blocks. As shown in the drawing titled "Output Macro Cell Programmable Options", the programmable blocks are: Register Select Options, Polarity Options, Clock Options, OMC Configuration Options and Output Enable Control Options.

There is one programmable location associated with each block except the Output Enable Control block which has two programmable fuse locations per OMC.

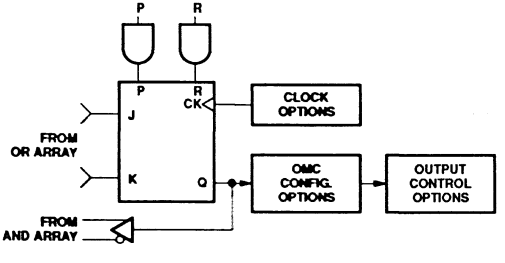
The following drawings detail the options associated with each programmable block. The associated programming codes are also included. The table titled "Output Macro Cell Configurations" (page 339) lists all the possible combinations of the five programmable options.

ARCHITECTURAL OPTIONS

REGISTER SELECT OPTIONS



REGISTER MODE (D or JK)	CODE
D-TYPE	A
F_C CONTROL P-TERM	L



REGISTER MODE (D or JK)	CODE
JK-TYPE	•
F_C CONTROL P-TERM	–

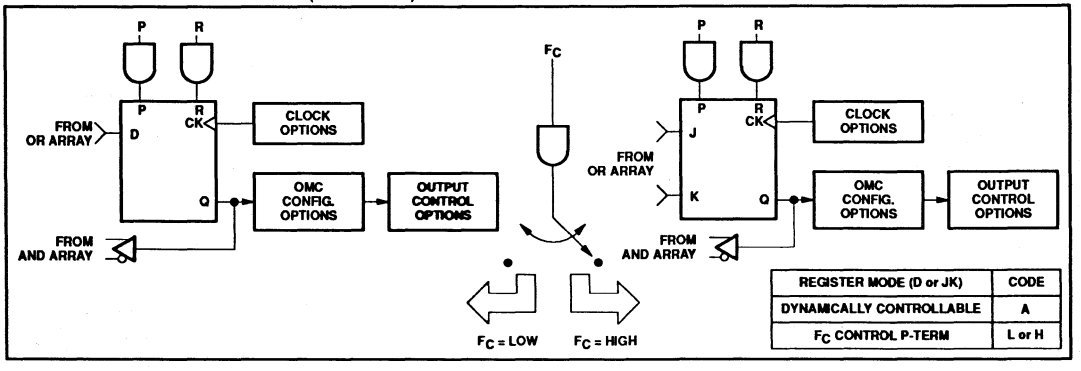
Register Select Options

Each OMC Register can be configured either as a dedicated D-type or a J-K flip-flop. The Flip-Flop Control term, Fc, provides the option to control each Register dynamically—switching from D-type to J-K type, based on the Fc control signal.

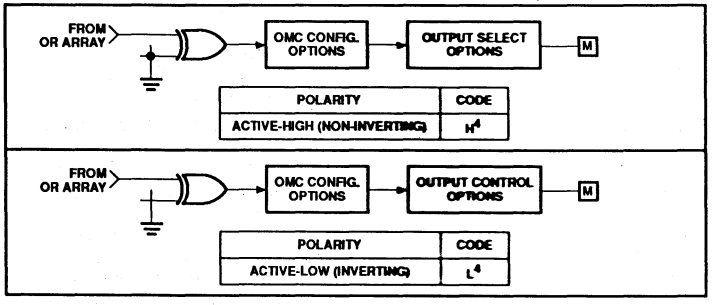
Register Preset and Reset are controlled from the AND array. Each OMC has an individual Reset Control term (RMn). The Register Preset function is controlled in two banks of 4 for OMCs M1 – M3 and M4 – M8 (via the control terms PA and PB). OMCs M0 and M9 have individual control terms (PM0 and PM9 respectively).

Notes on page 339.

REGISTER SELECT OPTIONS (Continued)



POLARITY OPTIONS (for Combinatorial I/O Configurations Only[1])

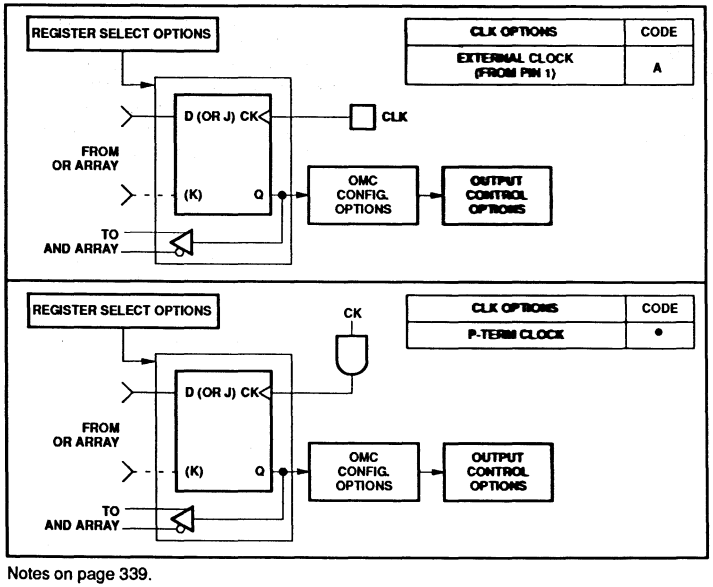


Polarity Options

When an OMC is configured as a Combinatorial I/O with Buried Register, the polarity of the combinatorial path can be programmed as Active-High or Active-Low. A configurable EX-OR gate provides polarity control.

If an OMC is configured as a Registered Output, /Q is propagated to the output pin. Note that either Q or /Q can be fedback to the AND array by manipulating the feedback logic equations. (TRUE or COMPLEMENT).

CLOCK OPTIONS



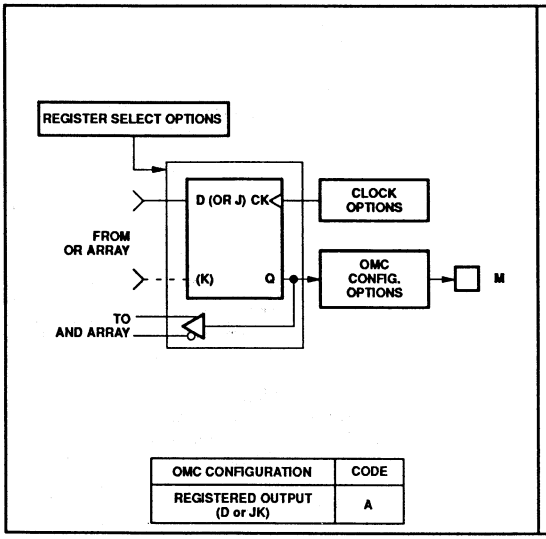
Clock Options

In the unprogrammed state, all Output Macro Cell clock sources are connected to the External Clock pin (I_0/CLK pin 1). Each OMC can be individually programmed such that its P-term Clock (CK_n) is enabled, thus disabling it from the External Clock and providing event-driven clocking capability.

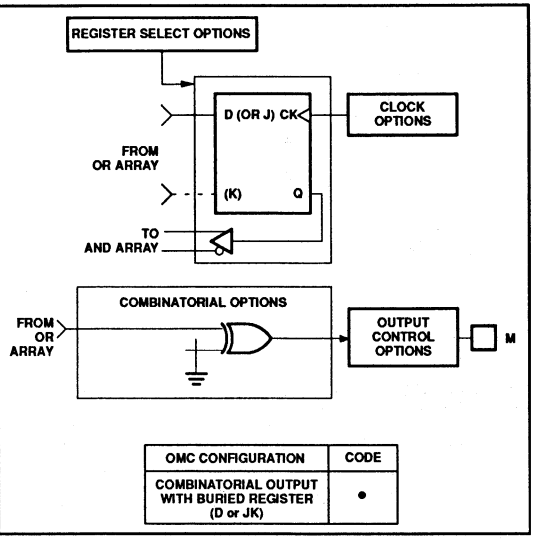
This feature supports multiple state machines, clocked at several different rates, all on one chip, or the ability to collect large amounts of random logic, including 10 separately clocked flip-flops.

Notes on page 339.

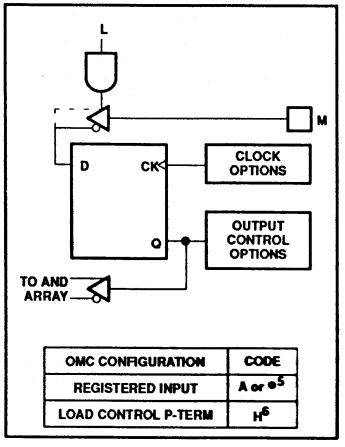
OUTPUT MACRO CELL CONFIGURATION OPTIONS



OMC CONFIGURATION	CODE
REGISTERED OUTPUT (D or JK)	A



OMC CONFIGURATION	CODE
COMBINATORIAL OUTPUT WITH BURIED REGISTER (D or JK)	•



OMC CONFIGURATION	CODE
REGISTERED INPUT	A or •[5]
LOAD CONTROL P-TERM	H[6]

Notes on page 339.

OMC Configuration Options

Each OMC can be configured as a Registered Output with feedback, a Registered Input or a Combinatorial I/O with Buried Register. Dedicated Input and dedicated I/O configurations are also possible.

When the Combinatorial I/O option is selected, (the Register Bypass option), the Buried Register remains 100% functional, with its own inputs from the AND array and a separate feedback path. This unique feature is ideal for designing any type of state machine; synchronous Mealy-types that require both Buried and Output Registers, or asynchronous Mealy-types that require buried registers and combinatorial output functions. Both synchronous and asynchronous Moore-type state machines can also be easily accommodated with the flexible OMC structure.

Note that an OMC can be configured as either a Combinatorial I/O (with Buried Register) or a Registered Output with feedback and it can still be used as a Registered Input. By disabling the outputs via any OE control function, the M pin can be used as an input. When the Load Control P-term is asserted HIGH, the register is preloaded from the M pin(s). When the L_C P-term is Active-Low and the output is enabled, the OMC will again function as configured (either a combinatorial I/O or a registered output with feedback). This feature is suited for synchronizing input signals prior to commencing a state sequence.

CMOS programmable multi-function PLD (42 × 105 × 12)

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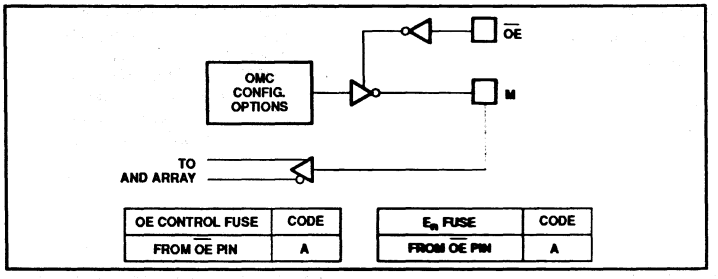
OUTPUT CONTROL OPTIONS



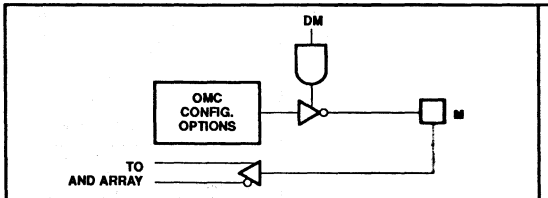
OE CONTROL FUSE	CODE
FROM $\overline{OE}$ PIN	A

E_n FUSE	CODE
FROM $\overline{OE}$ PIN	A

Output Enable Control Options

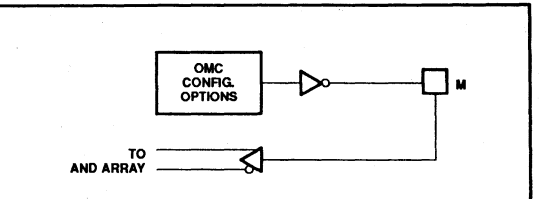
Similar to the Clock Options, the Output Enable Control for each OMC can be connected either to an external source (I9/$\overline{OE}$, pin 13) or controlled from the AND array (P-terms DM_n). Each Output can also be permanently enabled.

Output Enable control for the two bi-directional I/O (B pins 10 and 11) is from the AND array only (P-terms DB0 and DB1 respectively).



OE FUSE	CODE
FROM P-TERM CONTROL	•

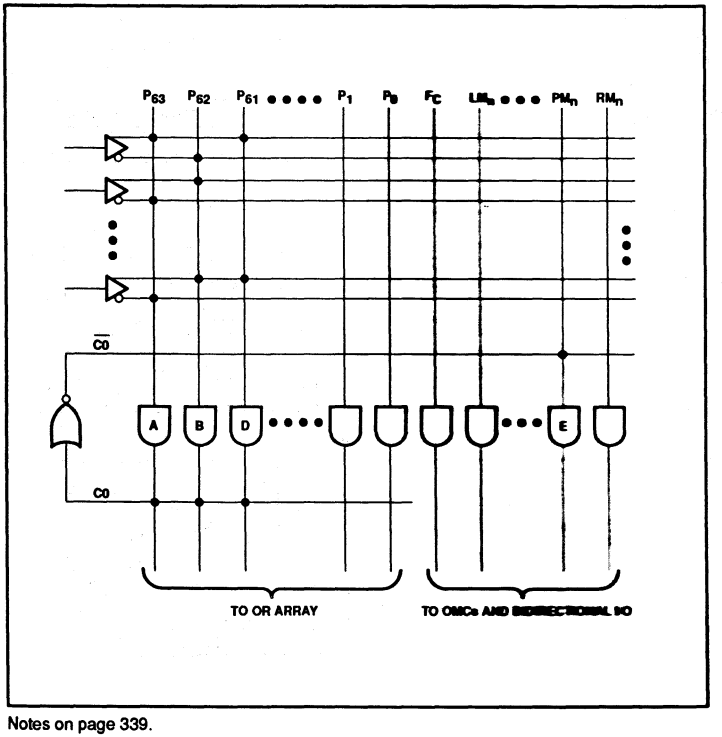
E_n FUSE	CODE
FROM P-TERM CONTROL	A or 0



OE CONTROL FUSE	CODE
ALWAYS ENABLED	A

E_n FUSE	CODE
ALWAYS ENABLED	0

COMPLEMENT ARRAY DETAIL



Complement Array Detail

The complement array is a special sequencer feature that is often used for detecting illegal states. It is also ideal for generating IF-THEN-ELSE logic statements with a minimum number of product terms.

The concept is deceptively simple. If you subscribe to the theory that the expressions (/A * /B * /C) and ($\overline{A + B + C}$) are equivalent, you will begin to see the value of this single term NOR array.

The complement array is a single OR gate with inputs from the AND array. The output of the complement array is inverted and fedback to the AND array (NOR function). The output of the array will be LOW if any one or more of the AND terms connected to it are active (HIGH). If, however, all the connected terms are inactive (LOW), which is a classic unknown state, the output of the complement array will be HIGH.

Consider the product terms A, B and D that represent defined states. They are also connected to the input of the complement array. When the condition (not A and not B and not D) exists, the Complement Array will detect this and propagate an Active-High signal to the AND array. This signal can be connected to product term E, which could be used in turn to preset the state machine to known state. Without the complement array, one would have to generate product terms for all unknown or illegal states. With very complex state machines, such an approach can be prohibitive, both in terms of time and wasted resources.

Notes on page 339.

CMOS programmable multi-function PLD (42 × 105 × 12)

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LOGIC PROGRAMMING

The PLC42VA12 is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Signetics SLICE and SNAP design software packages. ABEL™ and CUPL™ design software packages also support the PLC42VA12 architecture.

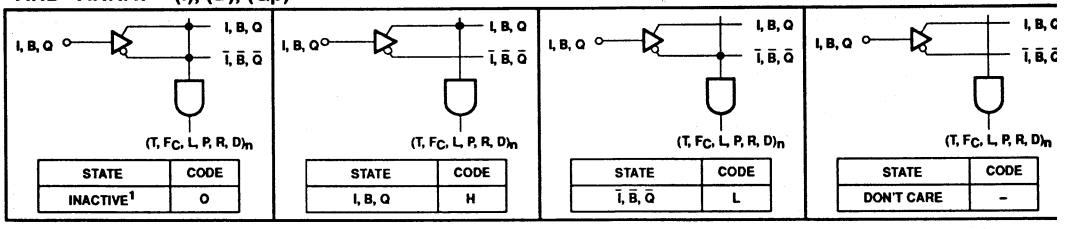
All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

PLC42VA12 logic designs can also be generated using the program table entry format, which is detailed on the following pages. This program table entry format is supported by SNAP and SLICE only. The SLICE design package is available, free of charge, to qualified users.

To implement the desired logic functions, th state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below. Symbols for OMC configuration have been previously defined the Architectural Options section.

LOGIC IMPLEMENTATION

"AND" ARRAY – (I), (B), (Qp)



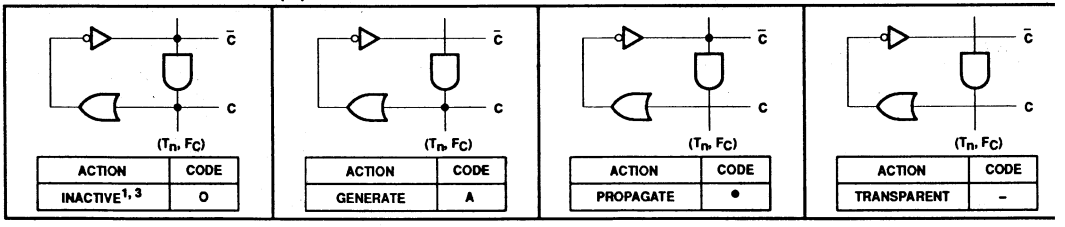
STATE	CODE
INACTIVE[1]	0

STATE	CODE
I, B, Q	H

STATE	CODE
Ī, B̄, Q̄	L

STATE	CODE
DON'T CARE	–

"COMPLEMENT" ARRAY – (C)



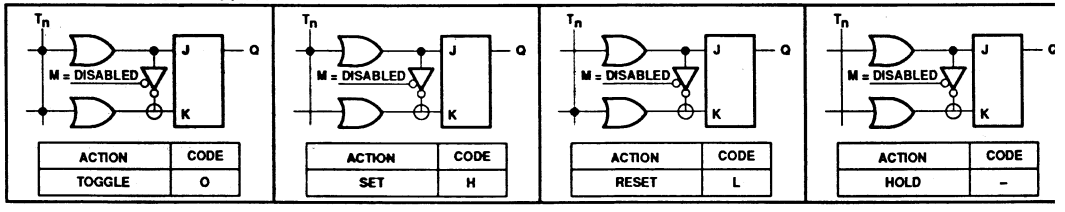
ACTION	CODE
INACTIVE[1, 3]	0

ACTION	CODE
GENERATE	A

ACTION	CODE
PROPAGATE	•

ACTION	CODE
TRANSPARENT	–

"OR" ARRAY – (J-K Type)



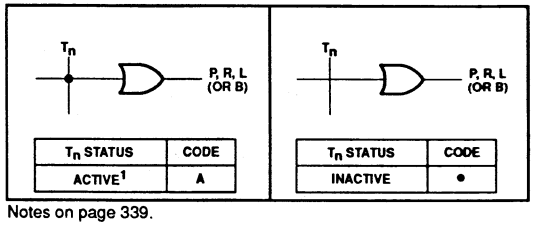
ACTION	CODE
TOGGLE	0

ACTION	CODE
SET	H

ACTION	CODE
RESET	L

ACTION	CODE
HOLD	–

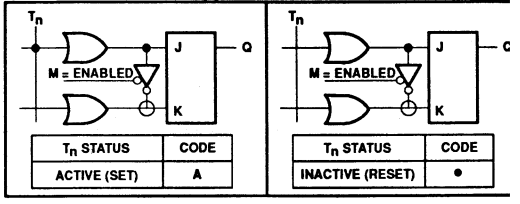
"OR" ARRAY



Tn STATUS	CODE
ACTIVE[1]	A

Tn STATUS	CODE
INACTIVE	•

"OR" ARRAY – (D-Type)



Tn STATUS	CODE
ACTIVE (SET)	A

Tn STATUS	CODE
INACTIVE (RESET)	•

Notes on page 339.

ABEL is a trademark of Data I/O Corp.
CUPL is a trademark of Logical Devices, Inc.

LOGIC IMPLEMENTATION (Continued)

OUTPUT MACRO CELL CONFIGURATIONS

OUTPUT MACRO CELL CONFIGURATION	PROGRAMMING CODES			
	REGISTER SELECT FUSE	OMC CONFIGURATION FUSE	POLARITY FUSE	CLOCK FUSE
Combinatorial I/O with Buried D-type register				
External clock source	A	•	H or L	A
P-term clock source	A	•	H or L	•
Combinatorial I/O with Buried J-K type register				
External clock source	•	•	H or L	A
P-term clock source	•	•	H or L	•
Registered Output (D-type) with feedback				
External clock source	A	A	N/A	A
P-term clock source	A	A	N/A	•
Registered Output (J-K type) with feedback				
External clock source	•	A	N/A	A
P-term clock source	•	A	N/A	•
Registered Input (Clocked Preload) with feedback				
External clock source	A	A or •[5]	Optional[5]	A
P-term clock source	A	A or •[5]	Optional[5]	•

OUTPUT ENABLE CONTROL[8] CONFIGURATION	OUTPUT CONTROL FUSES		CONTROL SIGNAL
	OE CONTROL FUSE	En FUSES	
OMC controlled by /OE pin	A	A	
Output Enabled			Low
Output Disabled			High
OMC controlled by P-term	•	A or 0	
Output Enabled			High
Output Disabled			Low
Output always Enabled	A	0	Not Applicable

NOTES:
1. This is the initial (unprogrammed) state of the device.
2. Any gate will be unconditionally inhibited if both the TRUE and COMPLEMENT fuses are left intact.
3. To prevent oscillations, this state is not allowed for Complement Array fuse pairs that are coupled to active product terms.
4. The OMC Configuration fuse must be programmed as Combinatorial I/O in order to make use of the Polarity Option.
5. Regardless of the programmed state of the OMC Configuration fuse, an OMC can be used as a Registered Input. Note that the Load Control P-term must be asserted Active-High.
6. Output must be disabled.
7. Program code definitions:
   - A = Active (unprogrammed fuse)
   - 0, • = Inactive (programmed fuse)
   - – = Don't Care (both TRUE and COMPLEMENT fuses unprogrammed)
   - H = Active-High connection
   - L = Active-Low connection
8. OE control for B0 and B1 (Pins 10 and 11) is from the AND array only.

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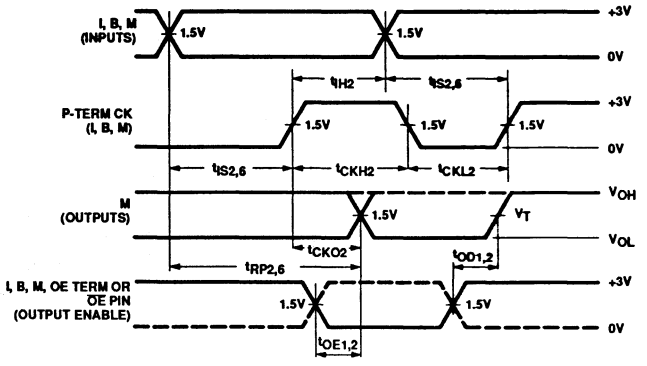
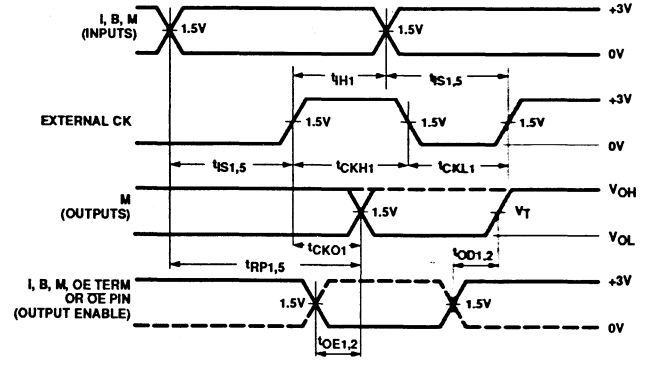
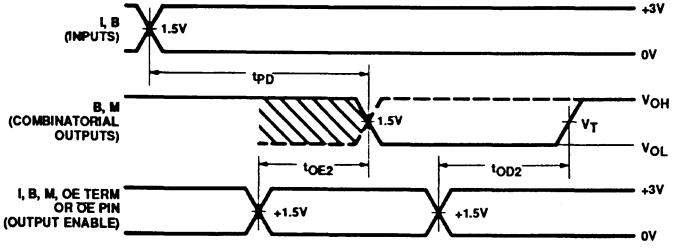
TIMING DIAGRAMS



Flip-Flop Outputs with P-term Clock



Flip-Flop Outputs with External Clock

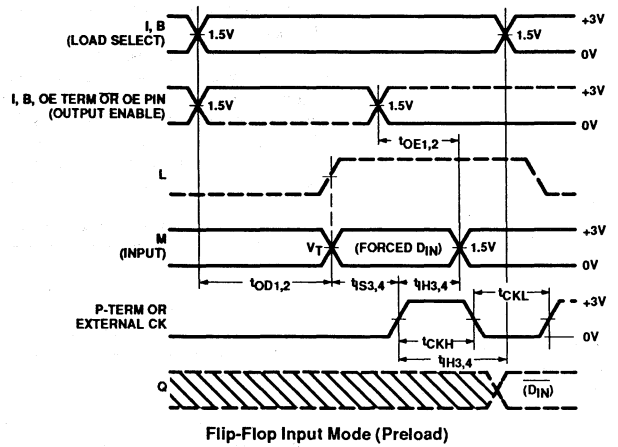


Gated Outputs

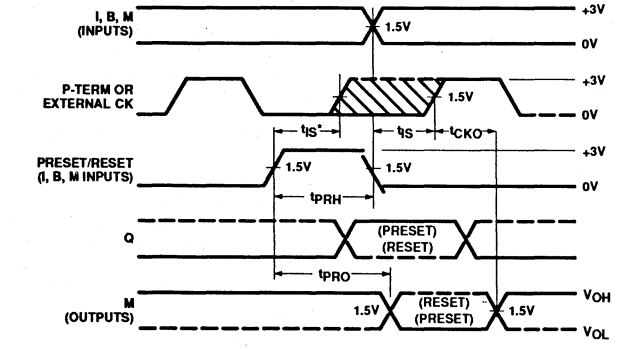
TIMING DEFINITIONS

SYMBOL	PARAMETER
f_{CK1}	Clock Frequency; External Clock
f_{CK2}	Clock Frequency; P-term Clock
t_{CKH1}	Width of Input Clock Pulse; External Clock
t_{CKH2}	Width of Input Clock Pulse; P-term Clock
t_{CKL1}	Interval between Clock pulses; External Clock
t_{CKL2}	Interval between Clock Pulses; P-term Clock
t_{CKO1}	Delay between the Positive Transition of External Clock and when M Outputs become valid.
t_{CKO2}	Delay between the Positive Transition of P-term Clock and when M Outputs become valid.
t_{RP1}	Delay between beginning of Valid Input and when the M outputs become Valid when using External Clock.
t_{RP2}	Delay between beginning of Valid Input and when the M outputs become Valid when using P-term Clock.
t_{RP3}	Delay between beginning of Valid Input and when the M outputs become Valid when using Preload Inputs (from M pins) and External Clock.
t_{RP4}	Delay between beginning of Valid Input and when the M outputs become valid when using Preload inputs (from M pins) and P-term Clock.
t_{RP5}	Delay between beginning of Valid Input and when the M outputs become Valid when using Complement Array and External clock.
t_{RP6}	Delay between beginning of Valid Input and when the M outputs become Valid when using Complement Array and P-term Clock.
f_{MAX1}	Minimum guaranteed Operating Frequency; Dedicated Clock
f_{MAX2}	Minimum guaranteed Operating Frequency; P-term Clock
f_{MAX3}	Minimum guaranteed Operating Frequency using Preload; Dedicated Clock (M pin to M pin)
f_{MAX4}	Minimum guaranteed Operating Frequency using Preload; P-term Clock (M pin to M pin)
f_{MAX5}	Minimum guaranteed Operating Frequency using Complement Array; Dedicated Clock
f_{MAX6}	Minimum Operating Frequency using Complement Array; P-term Clock
t_{IH1}	Required delay between positive transition of External Clock and end of valid input data.

TIMING DIAGRAMS (Continued)

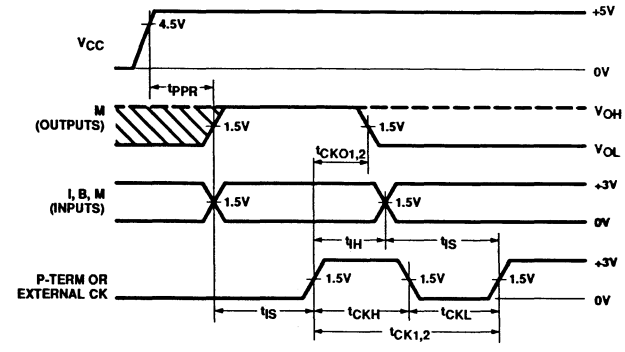


Flip-Flop Input Mode (Preload)



*Preset and Reset functions override Clock. However, M outputs may glitch with the first positive Clock Edge if t_{IS} cannot be guaranteed by the user.

Asynchronous Preset/Reset



Power-On Reset

TIMING DEFINITIONS (Continued)

SYMBOL	PARAMETER
t_{IH2}	Required delay between positive transition of P-term Clock and end of valid input data.
t_{IH3}	Required delay between positive transition of External Clock and end of valid input data when using Preload Inputs (from M pins).
t_{IH4}	Required delay between positive transition of P-term Clock and end of valid input data when using Preload Inputs (from M pins).
t_{IS1}	Required delay between beginning of valid input and positive transition of External Clock.
t_{IS2}	Required delay between beginning of valid input and positive transition of P-term Clock input.
t_{IS3}	Required delay between beginning of valid Preload input (from M pins) and positive transition of External Clock.
t_{IS4}	Required delay between beginning of valid Preload input (from M pins) and positive transition of P-term Clock input.
t_{IS5}	Required delay between beginning of valid input through Complement Array and positive transition of External Clock.
t_{IS6}	Required delay between beginning of valid input through Complement Array and positive transition of P-term Clock input.
t_{OE1}	Delay between beginning of Output Enable signal (Low) from /OE pin and when Outputs become valid.
t_{OE2}	Delay between beginning of Output Enable signal (High or Low) from OE P-term and when Outputs become valid.
t_{OD1}	Delay between beginning of Output Enable signal (HIGH) from /OE pin and when Outputs become disabled.
t_{OD2}	Delay between beginning of Output Enable signal (High or Low) from OE P-term and when Outputs become disabled.
t_{PD}	Delay between beginning of valid input and when the Outputs become valid (Combinatorial Path).
t_{SR}	Width of Preset/Reset Pulse.
t_{SRO}	Delay between beginning of valid Preset/Reset Input and when the registered Outputs become Preset ("1") or Reset ("0").
t_{PPR}	Delay between V_{CC} (after power-up) and when flip-flops become Reset to "0". Note: Signal at Output (M pin) will be inverted.

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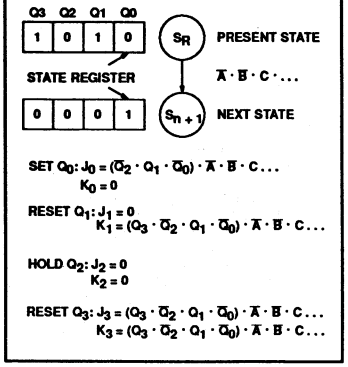
LOGIC FUNCTION



NOTE:
Similar logic functions are applicable for D mode flip-flops.

FLIP-FLOP TRUTH TABLE

$\overline{OE}$	L_n	CK_n	P_n	R_n	J	K	Q	M
H								Hi-Z
L	X	X	X	X	X	X	L	H
L	X	X	H	L	X	X	H	L
L	X	X	L	H	X	X	L	H
L	L	↑	L	L	L	L	Q	$\overline{Q}$
L	L	↑	L	L	L	H	L	H
L	L	↑	L	L	H	L	H	L
L	L	↑	L	L	H	H	$\overline{Q}$	Q
H	H	↑	L	L	L	H	L	H*
H	H	↑	L	L	H	L	H	L*
+10V	X	↑	X	X	L	H	L	H**
	X	↑	X	X	H	L	H	L**

NOTES:
1. Positive Logic:
   $J\text{-}K = \overline{T}_0 + T_1 + T_2 + ... + T_{31}$
   $T_n = \overline{C} \cdot (I0 \cdot I1 \cdot I2...) \cdot (\overline{Q0} \cdot Q1...) \cdot (B0 \cdot B1...)$
2. ↑ denotes transition for Low to High level.
3. X = Don't care
4. * = Forced at M_n pin for loading the J-K flip-flop in the Input mode. The load control term, L_n must be enabled (HIGH) and the p-terms that are connected to the associated flip-flop must be forced LOW (disabled) during Preload.
5. At P = R = H, Q = H. The final state of Q depends on which is released first.
6. ** = Forced at F_n pin to load J/K flip-flop (Diagnostic mode).

PLC42VA12 UNPROGRAMMED STATE

A factory shipped unprogrammed device is configured such that all cells are in a conductive state.

The following are:

ACTIVE:
- OR array logic terms
- Output Macro Cells M1 – M8;
  - D-type registered outputs (D = 0)
- External clock path
- Inputs: B0, B1, M0, M9

INACTIVE:
- AND array logic and control terms (except flip-flop mode control term, F_C)
- Bidirectional I/O (B0, B1);
  - Inputs are active. Outputs are 3-Stated via the OE P-terms, D0 and D1.
  - D-type registers (D = 0).
- Output Macro Cells M0 and M9;
  - Bidirectional I/O, 3-Stated via the OE P-terms, DM0 and DM9. The inputs are active.
- P-term clocks
- Complement Array
- J-K Flip-Flop mode

ERASURE CHARACTERISTICS (For Quartz Window Packages Only)

The erasure characteristics of the PLC42VA12 devices are such that erasure begins to occur upon exposure to light with wavelength shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000 – 4000Å range. Data shows that constant exposure to room level fluorescent lighting could erase a typical PLC42VA12 in approximately three years, while it would take approximately one week to cause erasure when exposed to direct sunlight. If the PLC42VA12 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

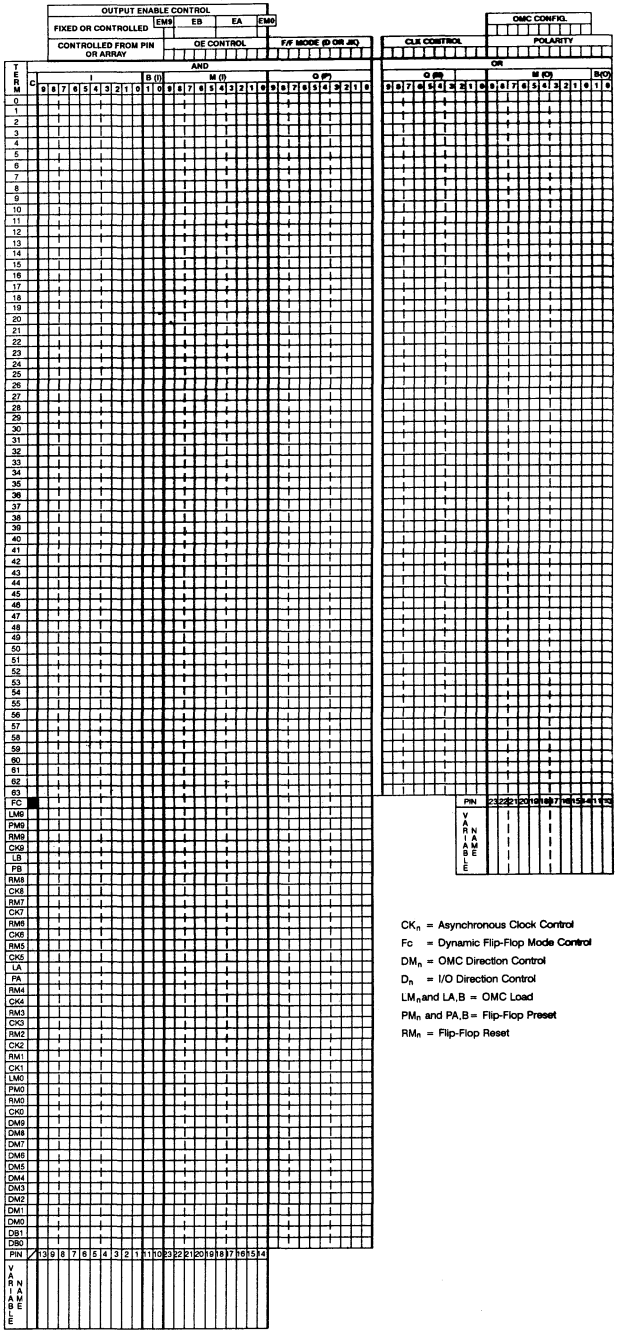
The recommended erasure procedure for the PLC42VA12 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15Wsec/cm^2. The erasure time with this dosage is approximately 30 to 35 minutes using an ultraviolet lamp with a 12,000µW/cm^2 power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose a CMOS EPLD can be exposed to without damage is 7258Wsec/cm^2 (1 week @ 12000µW/cm^2). Exposure of these CMOS EPLDs to high intensity UV light for longer periods may cause permanent damage.

The maximum number of guaranteed erase/write cycles is 50. Data retentions exceeds 20 years.

CMOS programmable multi-function PLD (42 × 105 × 12)

PLC42VA12

PROGRAM TABLE

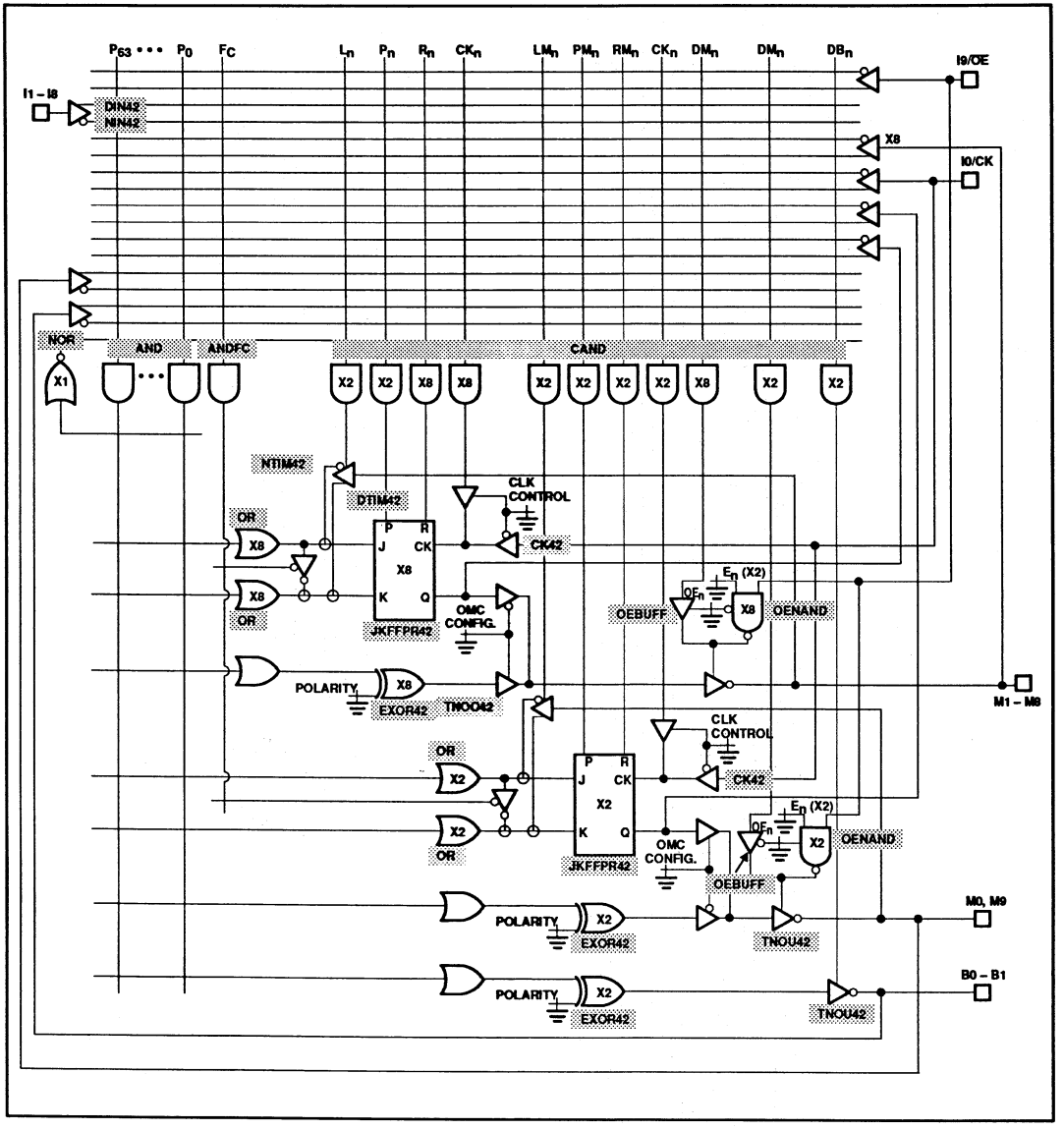


CK_n = Asynchronous Clock Control
Fc = Dynamic Flip-Flop Mode Control
DM_n = OMC Direction Control
D_n = I/O Direction Control
LM_n and LA,B = OMC Load
PM_n and PA,B = Flip-Flop Preset
RM_n = Flip-Flop Reset

CMOS programmable multi-function PLD (42 × 105 × 12)

PLC42VA12

SNAP RESOURCE SUMMARY DESIGNATIONS



CMOS programmable multi-function PLD (42 × 105 × 12)

PLC42VA12I (Industrial)

DESCRIPTION

The new PLC42VA12I CMOS PLD from Signetics exhibits a unique combination of the two architectural concepts that revolutionized the PLD marketplace.

The Signetics unique Output Macro Cell (OMC) embodies all the advantages and none of the disadvantages associated with the "V" type Output Macro Cell devices. This new design, combined with added functionality of two programmable arrays, represents a significant advancement in the configurability and efficiency of multi-function PLDs.

The most significant improvement in the Output Macro Cell structure is the implementation of the register bypass function. Any of the 10 J-K/D registers can be individually bypassed, thus creating a combinatorial I/O path from the AND array to the output pin. Unlike other "V" type devices, the register in the PLC42VA12I Macro Cell remains fully functional as a buried register. Both the combinatorial I/O and buried register *have separate input paths (from the AND* array). In most V-type architectures, the register is lost as a resource when the cell is configured as a combinatorial I/O. This feature provides the capability to operate the buried register independently from the combinatorial I/O.

The PLC42VA12I is an EPROM-based CMOS device. Designs can be generated using Signetics SNAP and SLICE PLD design software packages or one of several other commercially available JEDEC standard PLD design software packages.

FEATURES

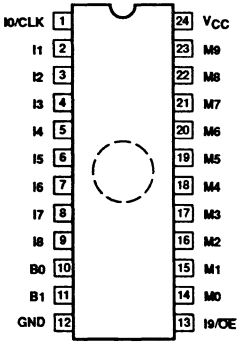
- Industrial temperature range EPROM-based CMOS multi-function PLD
  - –40°C to +85°C (10% power supplies)
- Super set of 22V10, 32VX10 and 20RA10 PAL® ICs
- Two fully programmable arrays eliminate "P-term Depletion"
  - Up to 64 P-terms per OR function
- Improved Output Macro Cell Structure
  - Individually programmable as:
    - Registered Output with feedback
    - Registered Input
    - Combinatorial I/O with Buried Register
    - Dedicated I/O with feedback
    - Dedicated Input (combinatorial)
  - Bypassed Registers are 100% functional with separate input and feedback paths
  - Individual Output Enable control functions
    - From pin or AND array
- Reprogrammable—tested 100% for programmability
- Eleven clock sources
- Register Preload and Diagnostic Test Mode Features
- Security fuse

APPLICATIONS

- Mealy or Moore State Machines
  - Synchronous
  - Asynchronous
- Multiple, independent State Machines
- 10-bit ripple cascade
- Sequence recognition
- Bus Protocol generation
- Industrial control
- A/D Scanning

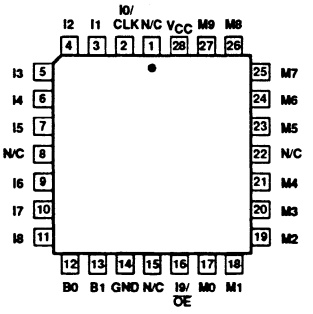
PIN CONFIGURATIONS

FA and N Packages



N = Plastic DIP (300mil-wide)
FA = Ceramic DIP with Quartz Window (300mil-wide)

A Package



A = Plastic Leaded Chip Carrier (450mil-square)

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-Pin Ceramic Dual In-Line with window, Industrial Temperature Range, Reprogrammable (300mil-wide)	PLC42VA12IFA
24-Pin Plastic Dual In-Line, Industrial Temperature Range, One Time Programmable (300mil-wide)	PLC42VA12IN
28-Pin Plastic Leaded Chip Carrier, Industrial Temperature Range, One Time Programmable (450mil-wide)	PLC42VA12IA

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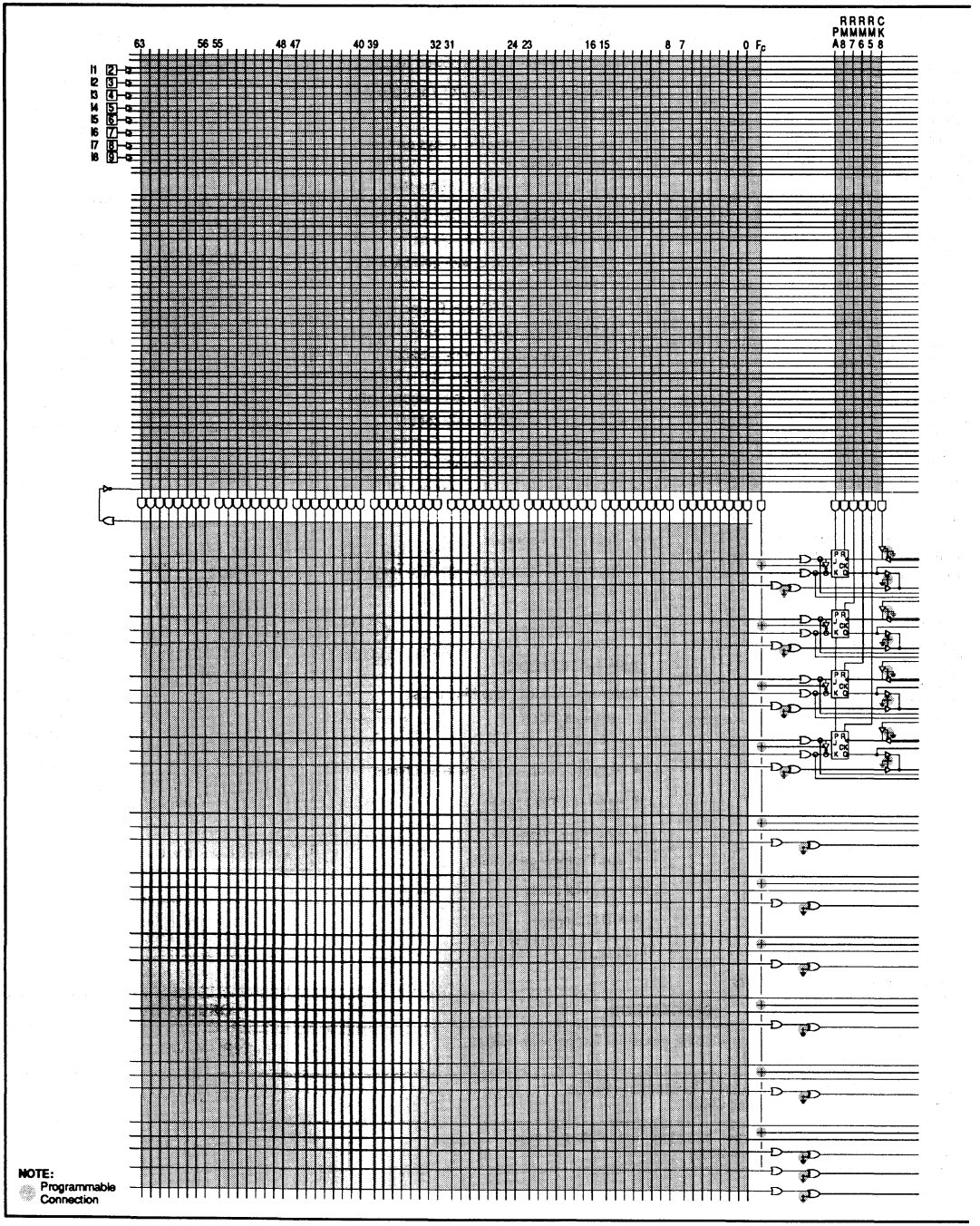
CMOS programmable multi-function PLD (42 × 105 × 12)

PLC42VA12I

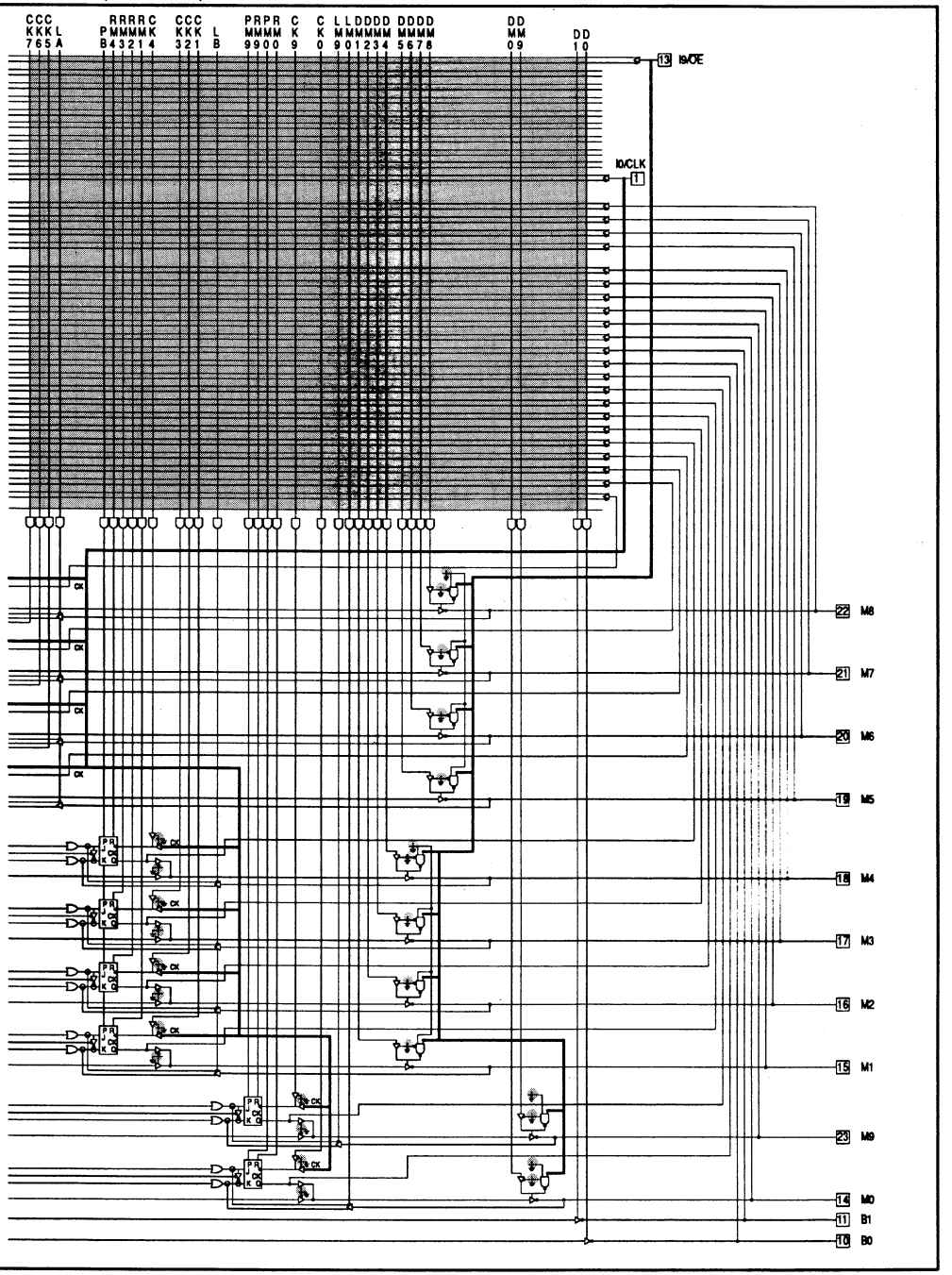
LOGIC DIAGRAM



CMOS programmable multi-function PLD (42 × 105 × 12)

PLC42VA12I

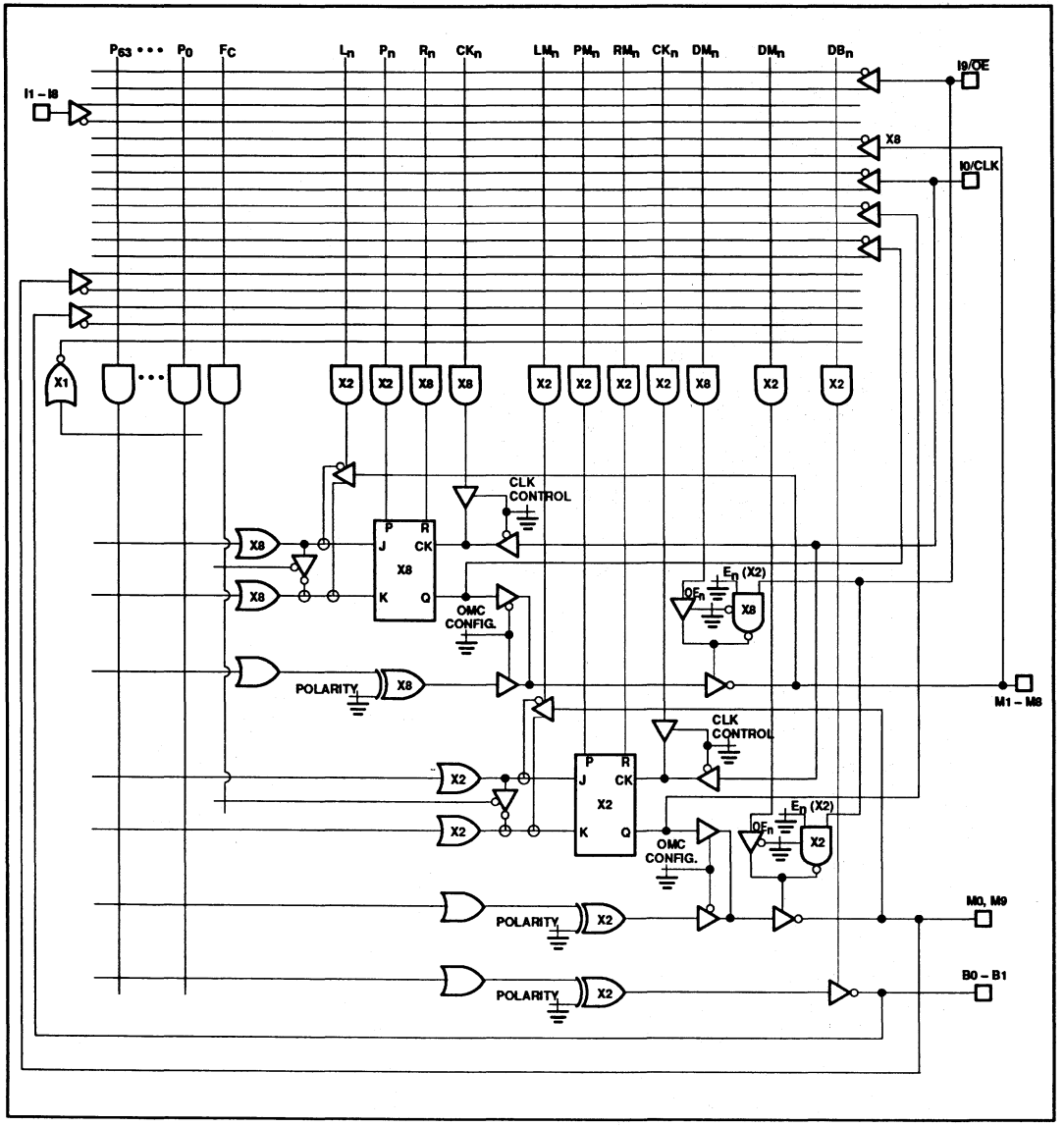
LOGIC DIAGRAM (Continued)



CMOS programmable multi-function PLD (42 × 105 × 12)

PLC42VA12I

FUNCTIONAL DIAGRAM



CMOS programmable multi-function PLD (42 × 105 × 12)

PLC42VA12I

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS	UNIT
V_{CC}	Supply voltage	–0.5 to +7	V_{DC}
V_{IN}	Input voltage	–0.5 to V_{CC} +0.5	V_{DC}
V_{OUT}	Output voltage	–0.5 to V_{CC} +0.5	V_{DC}
I_{IN}	Input currents	–10 to +10	mA
I_{OUT}	Output currents	+24	mA
T_{amb}	Operating temperature range	–40 to +85	°C
T_{stg}	Storage temperature range	–65 to +150	°C

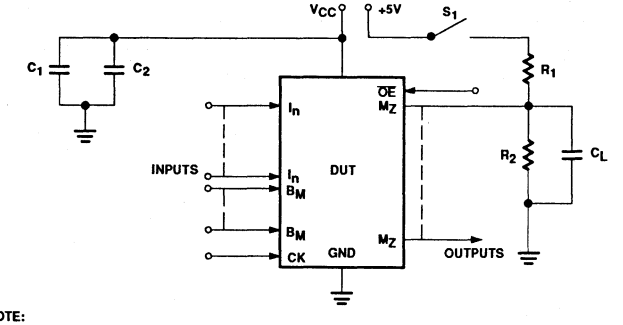
NOTE:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	160°C
Maximum ambient	85°C
Allowable thermal rise ambient to junction	75°C

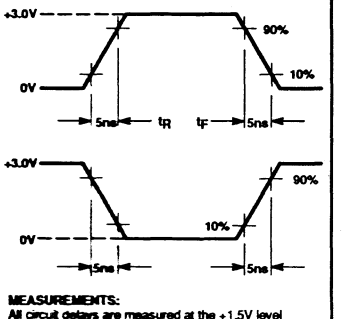
AC TEST CONDITIONS



NOTE:
C_1 and C_2 are to bypass V_{CC} to GND.

Test Load Circuit

VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

DC ELECTRICAL CHARACTERISTICS

$-40°C \le T_{amb} \le +85°C$, $4.5V \le V_{CC} \le 5.5V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS MIN	LIMITS TYP[1]	LIMITS MAX	UNIT
Input voltage[2]						
V_{IL}	Low	V_{CC} = MIN	–0.3		0.8	V
V_{IH}	High	V_{CC} = MAX	2.0		V_{CC} + 0.3	V
Output voltage[2]						
V_{OL}	Low	V_{CC} = MIN; I_{OL} = 16mA		0.3	0.5	V
V_{OH}	High	V_{CC} = MIN; I_{OH} = –3.2mA	2.4	4.3		V
Input current						
I_{IL}	Low	V_{IN} = GND		–1	–10	µA
I_{IH}	High	V_{IN} = V_{CC}		+1	10	µA
Output current						
$I_{O(OFF)}$	Hi-Z state	V_{OUT} = V_{CC} V_{OUT} = GND		1 –1	10 –10	µA µA
I_{OS}	Short-circuit[3,7]	V_{OUT} = GND			–130	mA
I_{CC1}	V_{CC} supply current (Active)[4]	I_{OUT} = 0mA, f = 15MHz[6], V_{CC} = MAX			150	mA
I_{CC2}	V_{CC} supply current (Active)[5]	I_{OUT} = 0mA, f = 15MHz[5], V_{CC} = MAX			120	mA
Capacitance						
C_I	Input	V_{CC} = 5V; V_{IN} = 2.0V		12		pF
C_B	I/O	V_B = 2.0V		15		pF

NOTES:

1. All typical values are at V_{CC} = 5V. T_{amb} = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Duration of short–circuit should not exceed one second. Test one at a time.
4. Tested with V_{IL} = 0.45V, V_{IH} = 2.4V.
5. Tested with V_{IL} = 0V, V_{IH} = V_{CC}.
6. Refer to Figure 1, ΔI_{CC} vs Frequency (worst case). (Referenced from 15MHz)
   The I_{CC} increases by 1.5mA per MHz for the frequency range of 16MHz up to 25MHz.
   The I_{CC} remains at a worst case for the frequency range of 26MHz up to 37MHz.
   The I_{CC} decreases by 1.0mA per MHz for the frequency range of 14MHz down to 1MHz.
   The worst case I_{CC} is calculated as follows:
   - All dedicated inputs are switching.
   - All OMCs are configured as JK flip-flops in the toggle mode. . .all are toggling.
   - All 12 outputs are disabled.
   - The number of product terms connected does not impact the I_{CC}.
7. Refer to Figure 2 for Δt_{PD} vs output capacitance loading.

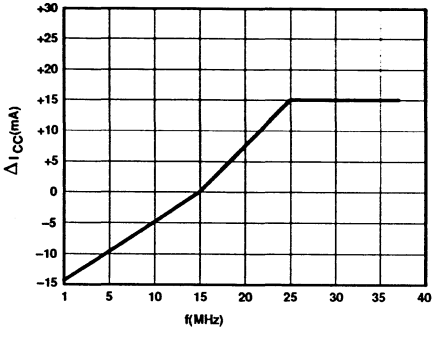


Figure 1. ΔI_{CC} vs Frequency (Worst Case) (Referenced from 15MHz)

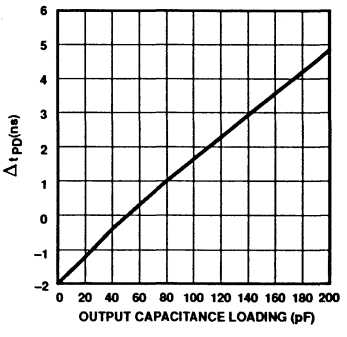


Figure 2. Δt_{PD} vs Output Capacitance Loading (Typical)

AC ELECTRICAL CHARACTERISTICS

$-40°C \le T_{amb} \le +85°C$, $4.5V \le V_{CC} \le 5.5V$; $R_1 = 238\Omega$, $R_2 = 170\Omega$

SYMBOL	PARAMETER	FROM	TO	TEST[2] CONDITION (C_L (pF))	PLC42VA12I MIN	PLC42VA12I TYP[1]	PLC42VA12I MAX	UNIT
Set-up Time								
t_{IS1}	Input; dedicated clock	(I, B, M) +/–	CK+	50	23	16		ns
t_{IS2}	Input; P-term clock	(I, B, M) +/–	(I, B, M) +/–	50	20	13		ns
t_{IS3}[3]	Preload; dedicated clock	(M) +/–	CK+	50	10	3.5		ns
t_{IS4}[3]	Preload; P-term clock	(M) +/–	(I, B, M) +/–	50	2	–1.0		ns
t_{IS5}[3]	Input through complement array; dedicated clock	(I, B, M) +/–	CK+	50	50	34		ns
t_{IS6}[3]	Input through complement array; P-term clock	(I, B, M) +/–	(I, B, M) +/–	50	40	30		ns
Propagation Delay								
t_{PD1}	Propagation Delay	(I, B, M) +/–	(I, B, M) +/–	50		20	35	ns
t_{PD2}	Propagation Delay with complement array (2 passes)	(I, B,) +/–	(I, B, M) +/–	50		36	55	ns
t_{CKO1}	Clock to Output; Dedicated clock	CK+	(M) +/–	50		13	17	ns
t_{CKO2}	Clock to output; P-term clock	(I, B, M) +/–	(M) +/–	50		18	27	ns
t_{RP1}	Registered operating period; Dedicated clock ($t_{IS1} + t_{CKO1}$)	(I, B, M) +/–	(M) +/–	50		29	40	ns
t_{RP2}	Registered operating period; P-term clock ($t_{IS2} + t_{CKO2}$)	(I, B, M) +/–	(M) +/–	50		31	47	ns
t_{RP3}[3]	Register preload operating period; Dedicated clock ($t_{IS3} + t_{CKO1}$)	(M) +/–	(M) +/–	50		16.5	27	ns
t_{RP4}[3]	Register preload operating period; P-term clock ($t_{IS4} + t_{CKO2}$)	(M) +/–	(M) +/–	50		17	29	ns
t_{RP5}[3]	Registered operating period with complement array; dedicated clock ($t_{IS5} + t_{CKO1}$)	(I, B, M) +/–	(M) +/–	50		47	67	ns
t_{RP6}[3]	Registered operating period with complement array; P-term clock ($t_{IS6} + t_{CKO2}$)	(I, B, M) +/–	(M) +/–	50		48	67	ns
t_{OE1}	Output Enable; from /OE pin[4]	/OE –	(M) +/–	50		10	20	ns
t_{OE2}	Output Enable; from P-term[4]	(I, B, M) +/–	(B, M) +/–	50		12.5	25	ns
t_{OD1}	Output Disable; from /OE pin[4]	/OE +	Outputs disabled	5		10	20	ns
t_{OD2}	Output Disable; from P-term[4]	(I, B, M) +/–	Outputs disabled	5		14.5	25	ns
t_{PRO}[3]	Preset to Output	(I, B, M) +/–	(M) +/–	50		25	35	ns
t_{PPR}[3]	Power-on Reset (Mn = 1)	V_{CC} +	(M) +/–	50			15	ns
Hold Time								
t_{IH1}	Input (Dedicated clock)	CK+	(I, B, M) +/–	50	0	–13		ns
t_{IH2}	Input (P-term clock)	(I, B, M) +/–	(I, B, M) +/–	50	5	–7.5		ns
t_{IH3}[3]	Input; from Mn (Dedicated clock)	CK+	(M) +/–	50	5	–1.5		ns
t_{IH4}[3]	Input; from Mn (P-term clock)	(I, B, M) +/–	(M) +/–	50	10	3.5		ns
Pulse Width								
t_{CKH1}	Clock High; Dedicated clock	CK+	CK–	50	10	5		ns
t_{CKL1}	Clock Low; Dedicated clock	CK–	CK+	50	10	5		ns
t_{CKH2}	Clock High; P-term clock	CK+	CK–	50	15	7		ns
t_{CKL2}	Clock Low; P-term clock	CK–	CK+	50	15	7		ns
t_{PRH}[3]	Width of preset/reset input pulse	(I, B, M) +/–	(I, B, M) +/–	50	30	7		ns

Notes on page 352.

AC ELECTRICAL CHARACTERISTICS (Continued)

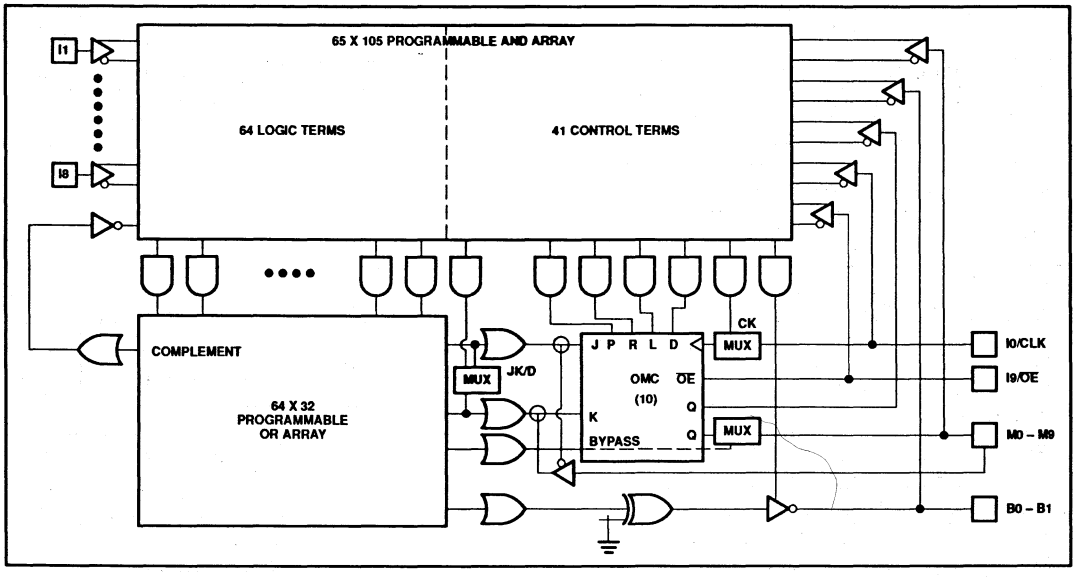
$-40°C \le T_{amb} \le +85°C$, $4.5V \le V_{CC} \le 5.5V$; $R_1 = 238\Omega$, $R_2 = 170\Omega$

SYMBOL	PARAMETER	FROM	TO	TEST[2] CONDITION (C_L (pF))	PLC42VA12I MIN	PLC42VA12I TYP[1]	PLC42VA12I MAX	UNIT
Frequency of Operation								
f_{CK1}	Dedicated clock frequency	C+	C+	50	50	100		MHz
f_{CK2}	P-term clock frequency	C+	C+	50	33	71.4		MHz
f_{MAX1}	Registered operating frequency; Dedicated clock ($t_{IS1} + t_{CKO1}$)	(I, B, M) +/–	(M) +/–	50	25	34.5		MHz
f_{MAX2}	Registered operating frequency; P-term clock ($t_{IS2} + t_{CKO2}$)	(I, B, M) +/–	(M) +/–	50	21.3	32.3		MHz
f_{MAX3}[3]	Register preload operating frequency; Dedicated clock ($t_{IS3} + t_{CKO1}$)	(M) +/–	(M) +/–	50	37	60.6		MHz
f_{MAX4}[3]	Register preload operating frequency; P-term clock ($t_{IS4} + t_{CKO2}$)	(M) +/–	(M) +/–	50	34.5	58.8		MHz
f_{MAX5}[3]	Registered operating frequency with complement array; Dedicated clock ($t_{IS5} + t_{CKO1}$)	(I, B, M) +/–	(M) +/–	50	14.9	21.3		MHz
f_{MAX6}[3]	Registered operating frequency with complement array; P-term clock ($t_{IS6} + t_{CKO2}$)	(I, B, M) +/–	(M) +/–	50	14.9	20.8		MHz

NOTES:

1. All typical values are at $V_{CC} = 5V$, $T_{amb} = +25°C$. These limits are not tested/guaranteed.
2. Refer also to AC Test Conditions (Test Load Circuit).
3. These limits are not tested, but are characterized periodically and are guaranteed by design.
4. For 3-State output; output enable times are tested with $C_L = 50pF$ to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with $C_L = 5pF$. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} - 0.5V)$ with S_1 open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with S_1 closed.

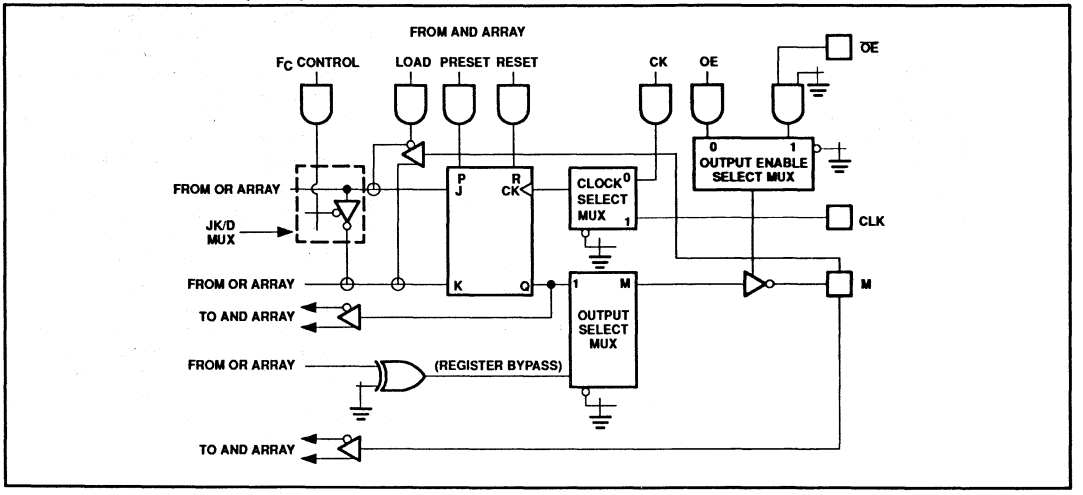
BLOCK DIAGRAM



CMOS programmable multi-function PLD (42 × 105 × 12)

PLC42VA12I

OUTPUT MACRO CELL (OMC)



Output Macro Cell Configuration

Signetics unique Output Macro Cell design represents a significant advancement in the configurability of multi-function Programmable Logic Devices.

The PLC42VA12I has 10 programmable Output Macro Cells. Each can be individually programmed in any of 5 basic configurations:

- Dedicated I/O (combinatorial) with feedback to AND array
- Dedicated Input
- Combinatorial I/O with feedback and Buried Register with feedback (register bypass)
- Registered Input
- Registered Output with feedback

Each of the registered options can be further customized as J-K type or D-type, with either an internally derived clock (from the AND array) or clocked from an external source. With these additional programmable options, it is possible to program each Output Macro Cell in any one of 14 different configurations.

These 14 configurations, combined with the fully programmable OR array, make the PLC42VA12I the most versatile and silicon efficient of all the Output Macro Cell-type PLDs.

The most significant Output Macro Cell (OMC) feature is the implementation of the register bypass function. Any of the 10 J-K/D registers can be individually bypassed, thus creating a combinatorial I/O path from the AND array to the output pin. Unlike other Output Macro Cell-type devices, the register in the OMC is fully functional as a buried register. Furthermore, both the combinatorial I/O and the buried register have separate input paths (from the AND array) and separate feedback paths (to the AND array). This feature provides the capability to operate the buried register independently from the combinatorial I/O.

The PLC42VA12I is ideally suited for both synchronous and asynchronous logic functions. Eleven clock sources – 10 driven from the AND array and one from an external source – make it possible to design synchronous state machine functions, event-driven state machine functions and combinatorial (asynchronous) functions all on the same chip.

Sophisticated control functions support individual OE control and Reset functions from the AND array. OE control is also available from the I9/$\overline{OE}$ pin. Register Preset and Load functions are controlled from the AND array, in 2 banks of 4 for OMCs M1 – M8. Output Macro Cells M0 and M9 have individual Preset and Load Control terms.

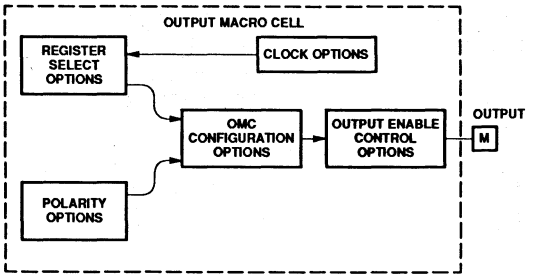
Output Polarity for the combinatorial I/O paths is configurable via 12 programmable EX-OR gates. The output of each register can be configured as inverting (active Low) or non-inverting (active High) via manipulation of the logic equations.

The output of each buried register can also be configured as inverting or non-inverting via the input buffer which feeds back to the AND array.

CMOS programmable multi-function PLD (42 × 105 × 12)

PLC42VA12I

OUTPUT MACRO CELL PROGRAMMABLE OPTIONS



OMC Programmable Options

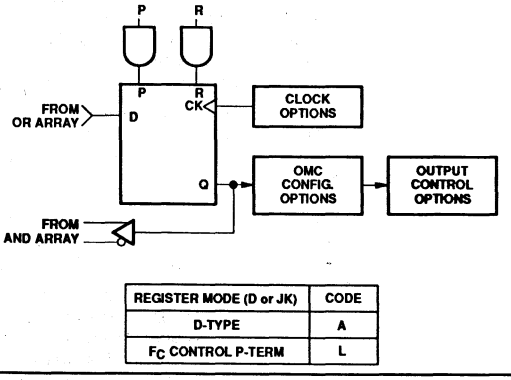
For purposes of programming, the Output Macro Cell should be considered to be partitioned into five separate blocks. As shown in the drawing titled "Output Macro Cell Programmable Options", the programmable blocks are: Register Select Options, Polarity Options, Clock Options, OMC Configuration Options and Output Enable Control Options.

There is one programmable location associated with each block except the Output Enable Control block which has two programmable fuse locations per OMC.

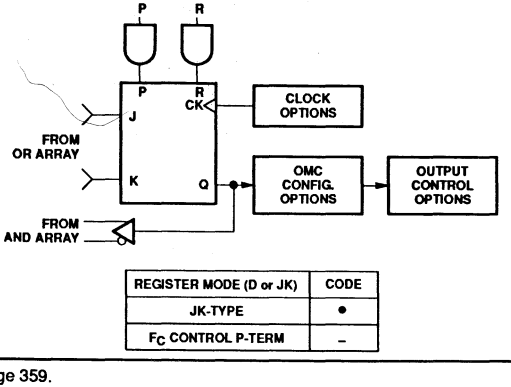
The following drawings detail the options associated with each programmable block. The associated programming codes are also included. The table titled "Output Macro Cell Configurations" (page 359) lists all the possible combinations of the five programmable options.

ARCHITECTURAL OPTIONS

REGISTER SELECT OPTIONS



REGISTER MODE (D or JK)	CODE
D-TYPE	A
F_C CONTROL P-TERM	L



REGISTER MODE (D or JK)	CODE
JK-TYPE	•
F_C CONTROL P-TERM	–

Register Select Options

Each OMC Register can be configured either as a dedicated D-type or a J-K flip-flop. The Flip-Flop Control term, Fc, provides the option to control each Register dynamically—switching from D-type to J-K type, based on the Fc control signal.

Register Preset and Reset are controlled from the AND array. Each OMC has an individual Reset Control term (RMn). The Register Preset function is controlled in two banks of 4 for OMCs M1 – M3 and M4 – M8 (via the control terms PA and PB). OMCs M0 and M9 have individual control terms (PM0 and PM9 respectively).

Notes on page 359.

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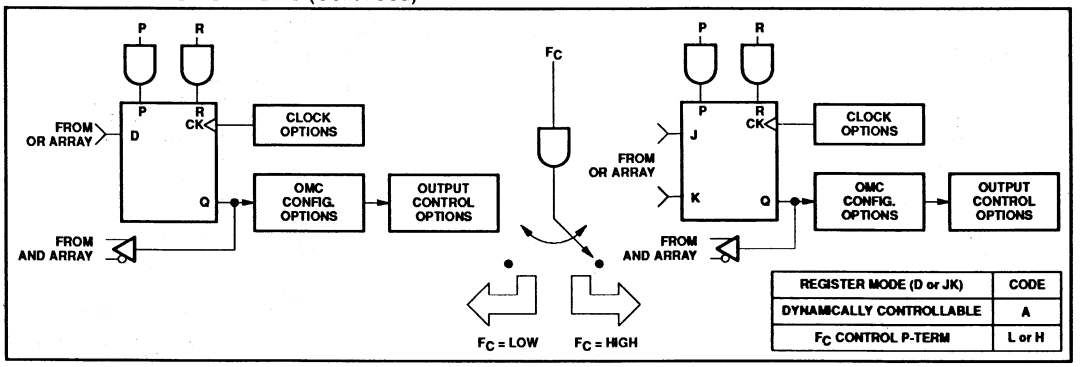
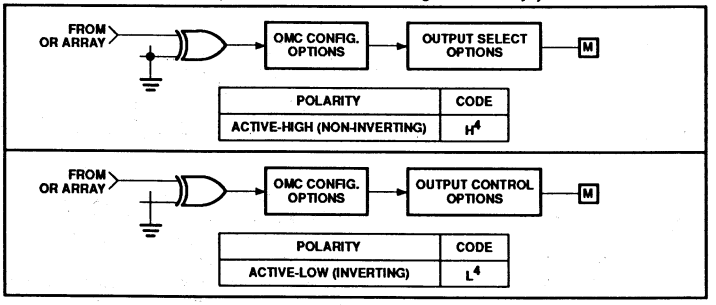
REGISTER SELECT OPTIONS (Continued)



POLARITY OPTIONS (for Combinatorial I/O Configurations Only[1])

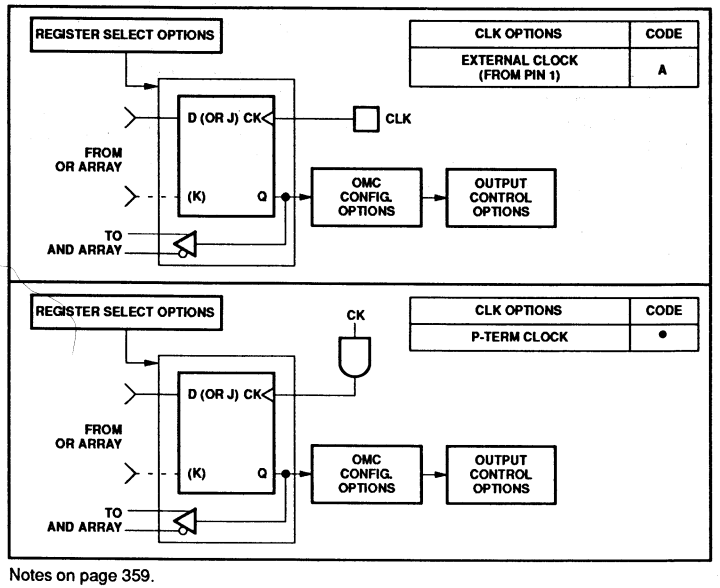


Polarity Options

When an OMC is configured as a Combinatorial I/O with Buried Register, the polarity of the combinatorial path can be programmed as Active-High or Active-Low. A configurable EX-OR gate provides polarity control.

If an OMC is configured as a Registered Output, /Q is propagated to the output pin. Note that either Q or /Q can be fedback to the AND array by manipulating the feedback logic equations. (TRUE or COMPLEMENT).

CLOCK OPTIONS



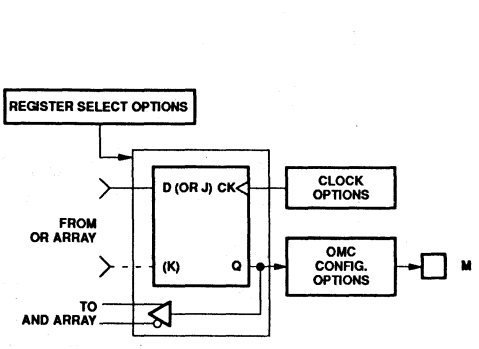
Clock Options

In the unprogrammed state, all Output Macro Cell clock sources are connected to the External Clock pin (I0/CLK pin 1). Each OMC can be individually programmed such that its P-term Clock (CK_n) is enabled, thus disabling it from the External Clock and providing event-driven clocking capability.

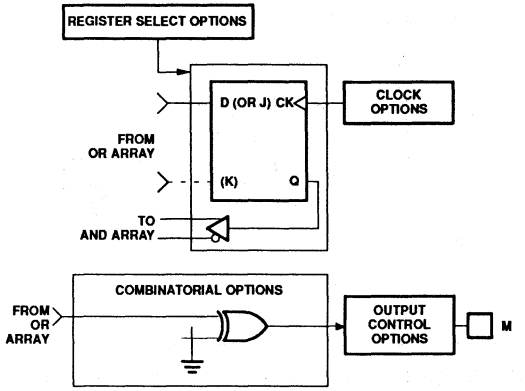
This feature supports multiple state machines, clocked at several different rates, all on one chip, or the ability to collect large amounts of random logic, including 10 separately clocked flip-flops.

Notes on page 359.

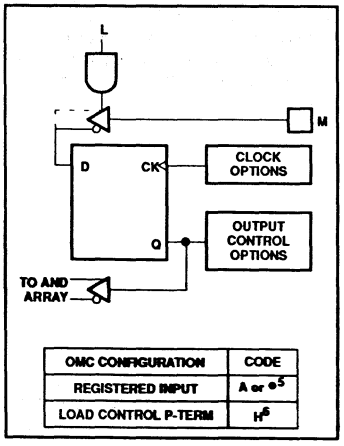
OUTPUT MACRO CELL CONFIGURATION OPTIONS



OMC CONFIGURATION	CODE
REGISTERED OUTPUT (D or JK)	A



OMC CONFIGURATION	CODE
COMBINATORIAL OUTPUT WITH BURIED REGISTER (D or JK)	•



OMC CONFIGURATION	CODE
REGISTERED INPUT	A or •[5]
LOAD CONTROL P-TERM	H[6]

Notes on page 359.

OMC Configuration Options

Each OMC can be configured as a Registered Output with feedback, a Registered Input or a Combinatorial I/O with Buried Register. Dedicated Input and dedicated I/O configurations are also possible.

When the Combinatorial I/O option is selected, (the Register Bypass option), the Buried Register remains 100% functional, with its own inputs from the AND array and a separate feedback path. This unique feature is ideal for designing any type of state machine; synchronous Mealy-types that require both Buried and Output Registers, or asynchronous Mealy-types that require buried registers and combinatorial output functions. Both synchronous and asynchronous Moore-type state machines can also be easily accommodated with the flexible OMC structure.

Note that an OMC can be configured as either a Combinatorial I/O (with Buried Register) or a Registered Output with feedback and it can still be used as a Registered Input. By disabling the outputs via any OE control function, the M pin can be used as an input. When the Load Control P-term is asserted HIGH, the register is preloaded from the M pin(s). When the L_C P-term is Active-Low and the output is enabled, the OMC will again function as configured (either a combinatorial I/O or a registered output with feedback). This feature is suited for synchronizing input signals prior to commencing a state sequence.

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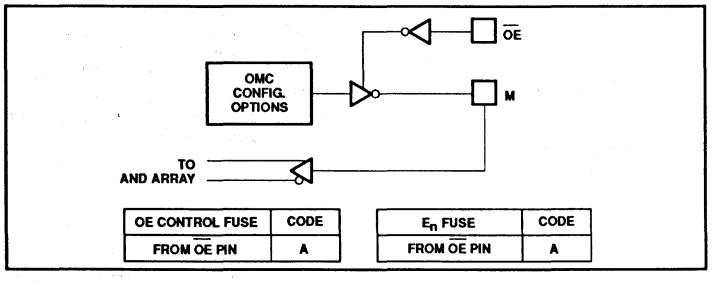
OUTPUT CONTROL OPTIONS



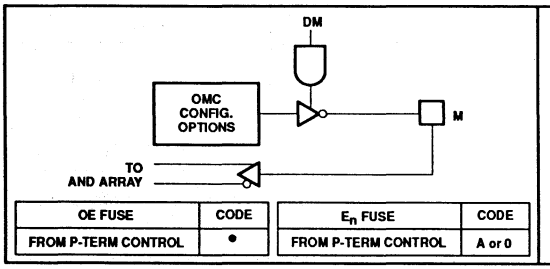
OE CONTROL FUSE	CODE
FROM $\overline{OE}$ PIN	A

E_n FUSE	CODE
FROM $\overline{OE}$ PIN	A

Output Enable Control Options

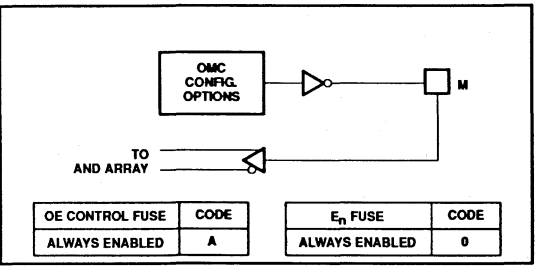
Similar to the Clock Options, the Output Enable Control for each OMC can be connected either to an external source (I9/$\overline{OE}$, pin 13) or controlled from the AND array (P-terms DM_n). Each Output can also be permanently enabled.

Output Enable control for the two bi-directional I/O (B pins 10 and 11) is from the AND array only (P-terms DB0 and DB1 respectively).



OE FUSE	CODE
FROM P-TERM CONTROL	•

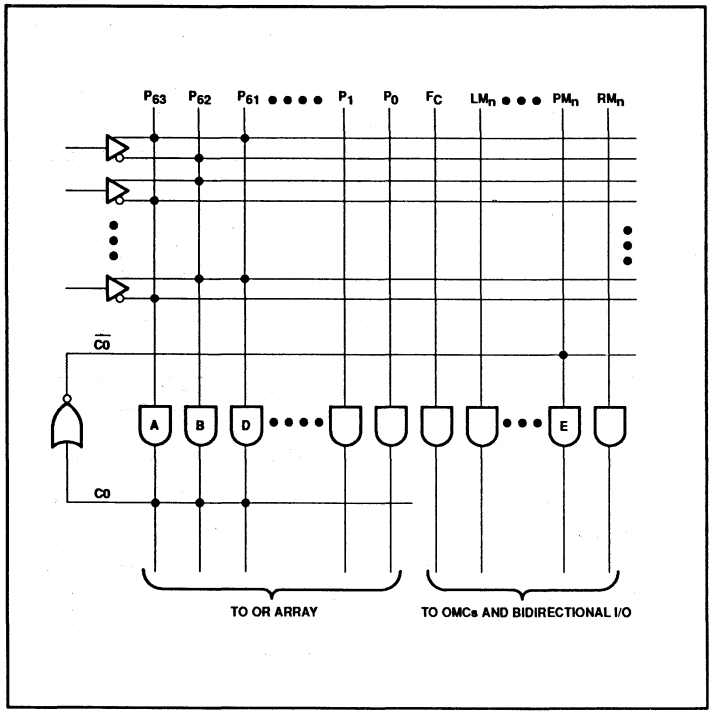
E_n FUSE	CODE
FROM P-TERM CONTROL	A or 0



OE CONTROL FUSE	CODE
ALWAYS ENABLED	A

E_n FUSE	CODE
ALWAYS ENABLED	0

COMPLEMENT ARRAY DETAIL



Complement Array Detail

The complement array is a special sequencer feature that is often used for detecting illegal states. It is also ideal for generating IF-THEN-ELSE logic statements with a minimum number of product terms.

The concept is deceptively simple. If you subscribe to the theory that the expressions (/A * /B * /C) and ($\overline{A + B + C}$) are equivalent, you will begin to see the value of this single term NOR array.

The complement array is a single OR gate with inputs from the AND array. The output of the complement array is inverted and fedback to the AND array (NOR function). The output of the array will be LOW if any one or more of the AND terms connected to it are active (HIGH). If, however, all the connected terms are inactive (LOW), which is a classic unknown state, the output of the complement array will be HIGH.

Consider the product terms A, B and D that represent defined states. They are also connected to the input of the complement array. When the condition (not A and not B and not D) exists, the Complement Array will detect this and propagate an Active-High signal to the AND array. This signal can be connected to product term E, which could be used in turn to preset the state machine to known state. Without the complement array, one would have to generate product terms for all unknown or illegal states. With very complex state machines, such an approach can be prohibitive, both in terms of time and wasted resources.

Notes on page 359.

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LOGIC PROGRAMMING

The PLC42VA12I is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Signetics SLICE and SNAP design software packages. ABEL™ and CUPL™ design software packages also support the PLC42VA12I architecture.

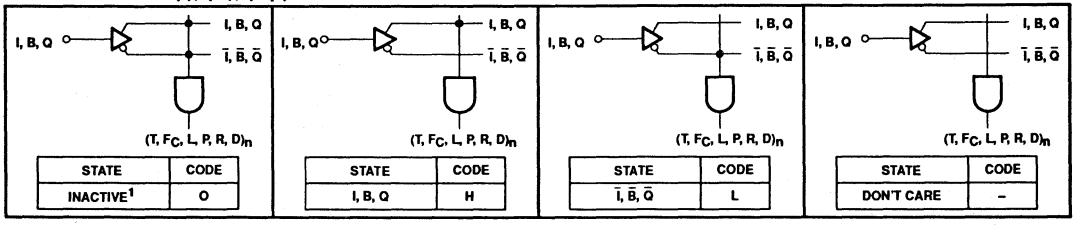
All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

PLC42VA12I logic designs can also be generated using the program table entry format, which is detailed on the following pages. This program table entry format is supported by SNAP and SLICE only. The SLICE design package is available, free of charge, to qualified users.

To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below. Symbols for OMC configuration have been previously defined in the Architectural Options section.

LOGIC IMPLEMENTATION

"AND" ARRAY – (I), (B), (Qp)



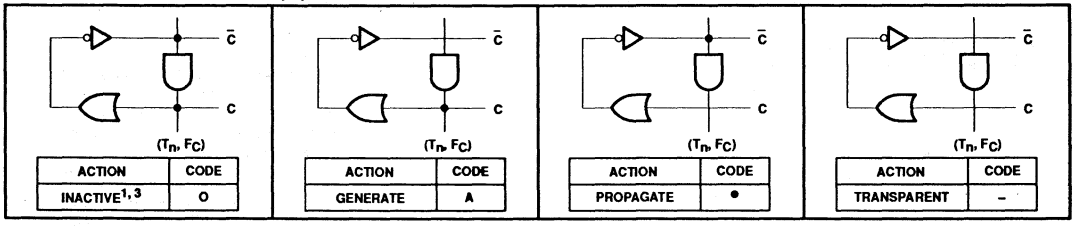
STATE	CODE
INACTIVE[1]	O

STATE	CODE
I, B, Q	H

STATE	CODE
Ī, B̄, Q̄	L

STATE	CODE
DON'T CARE	–

"COMPLEMENT" ARRAY – (C)



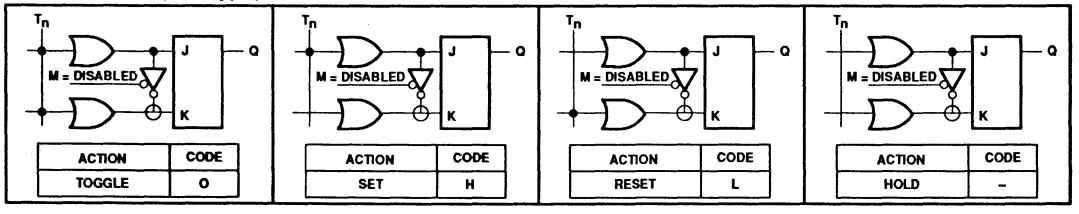
ACTION	CODE
INACTIVE[1, 3]	O

ACTION	CODE
GENERATE	A

ACTION	CODE
PROPAGATE	•

ACTION	CODE
TRANSPARENT	–

"OR" ARRAY – (J-K Type)



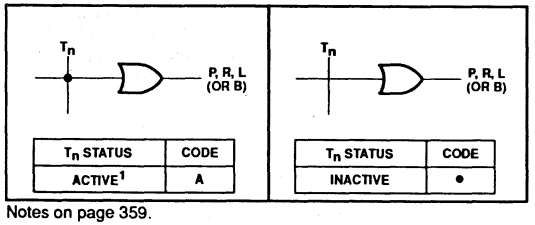
ACTION	CODE
TOGGLE	O

ACTION	CODE
SET	H

ACTION	CODE
RESET	L

ACTION	CODE
HOLD	–

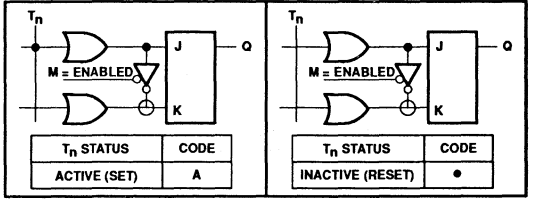
"OR" ARRAY



Tn STATUS	CODE
ACTIVE[1]	A

Tn STATUS	CODE
INACTIVE	•

"OR" ARRAY – (D-Type)



Tn STATUS	CODE
ACTIVE (SET)	A

Tn STATUS	CODE
INACTIVE (RESET)	•

Notes on page 359.

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CUPL is a trademark of Logical Devices, Inc.

LOGIC IMPLEMENTATION (Continued)

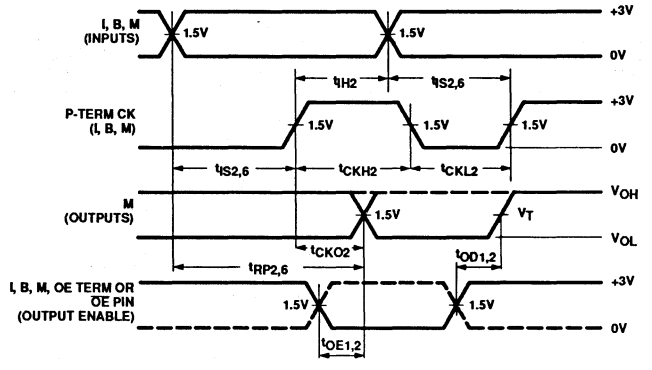
OUTPUT MACRO CELL CONFIGURATIONS

OUTPUT MACRO CELL CONFIGURATION	PROGRAMMING CODES			
	REGISTER SELECT FUSE	OMC CONFIGURATION FUSE	POLARITY FUSE	CLOCK FUSE
Combinatorial I/O with Buried D-type register				
External clock source	A	•	H or L	A
P-term clock source	A	•	H or L	•
Combinatorial I/O with Buried J-K type register				
External clock source	•	•	H or L	A
P-term clock source	•	•	H or L	•
Registered Output (D-type) with feedback				
External clock source	A	A	N/A	A
P-term clock source	A	A	N/A	•
Registered Output (J-K type) with feedback				
External clock source	•	A	N/A	A
P-term clock source	•	A	N/A	•
Registered Input (Clocked Preload) with feedback				
External clock source	A	A or •[5]	Optional[5]	A
P-term clock source	A	A or •[5]	Optional[5]	•

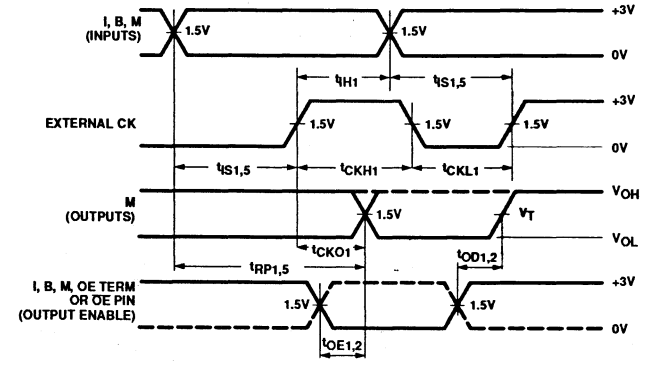
OUTPUT ENABLE CONTROL[8] CONFIGURATION	OUTPUT CONTROL FUSES		CONTROL SIGNAL
	OE CONTROL FUSE	En FUSES	
OMC controlled by /OE pin	A	A	
Output Enabled			Low
Output Disabled			High
OMC controlled by P-term	•	A or 0	
Output Enabled			High
Output Disabled			Low
Output always Enabled	A	0	Not Applicable

NOTES:
1. This is the initial (unprogrammed) state of the device.
2. Any gate will be unconditionally inhibited if both the TRUE and COMPLEMENT fuses are left intact.
3. To prevent oscillations, this state is not allowed for Complement Array fuse pairs that are coupled to active product terms.
4. The OMC Configuration fuse must be programmed as Combinatorial I/O in order to make use of the Polarity Option.
5. Regardless of the programmed state of the OMC Configuration fuse, an OMC can be used as a Registered Input. Note that the Load Control P-term must be asserted Active-High.
6. Output must be disabled.
7. Program code definitions:
   - A = Active (unprogrammed fuse)
   - 0, • = Inactive (programmed fuse)
   - – = Don't Care (both TRUE and COMPLEMENT fuses unprogrammed)
   - H = Active-High connection
   - L = Active-Low connection
8. OE control for B0 and B1 (Pins 10 and 11) is from the AND array only.

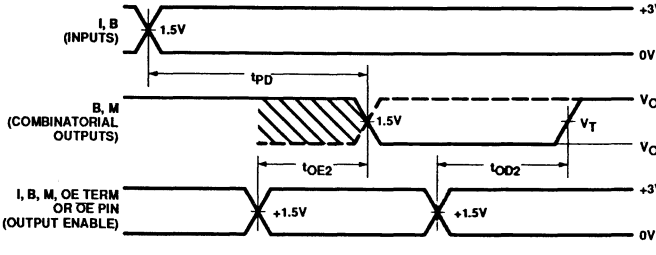
TIMING DIAGRAMS



Flip-Flop Outputs with P-term Clock



Flip-Flop Outputs with External Clock



Gated Outputs

TIMING DEFINITIONS

SYMBOL	PARAMETER
f_{CK1}	Clock Frequency; External Clock
f_{CK2}	Clock Frequency; P-term Clock
t_{CKH1}	Width of Input Clock Pulse; External Clock
t_{CKH2}	Width of Input Clock Pulse; P-term Clock
t_{CKL1}	Interval between Clock pulses; External Clock
t_{CKL2}	Interval between Clock Pulses; P-term Clock
t_{CKO1}	Delay between the Positive Transition of External Clock and when M Outputs become valid.
t_{CKO2}	Delay between the Positive Transition of P-term Clock and when M Outputs become valid.
t_{RP1}	Delay between beginning of Valid Input and when the M outputs become Valid when using External Clock.
t_{RP2}	Delay between beginning of Valid Input and when the M outputs become Valid when using P-term Clock.
t_{RP3}	Delay between beginning of Valid Input and when the M outputs become Valid when using Preload Inputs (from M pins) and External Clock.
t_{RP4}	Delay between beginning of Valid Input and when the M outputs become valid when using Preload inputs (from M pins) and P-term Clock.
t_{RP5}	Delay between beginning of Valid Input and when the M outputs become Valid when using Complement Array and External clock.
t_{RP6}	Delay between beginning of Valid Input and when the M outputs become Valid when using Complement Array and P-term Clock.
f_{MAX1}	Minimum guaranteed Operating Frequency; Dedicated Clock
f_{MAX2}	Minimum guaranteed Operating Frequency; P-term Clock
f_{MAX3}	Minimum guaranteed Operating Frequency using Preload; Dedicated Clock (M pin to M pin)
f_{MAX4}	Minimum guaranteed Operating Frequency using Preload; P-term Clock (M pin to M pin)
f_{MAX5}	Minimum guaranteed Operating Frequency using Complement Array; Dedicated Clock
f_{MAX6}	Minimum Operating Frequency using Complement Array; P-term Clock
t_{IH1}	Required delay between positive transition of External Clock and end of valid input data.

CMOS programmable multi-function PLD (42 × 105 × 12)

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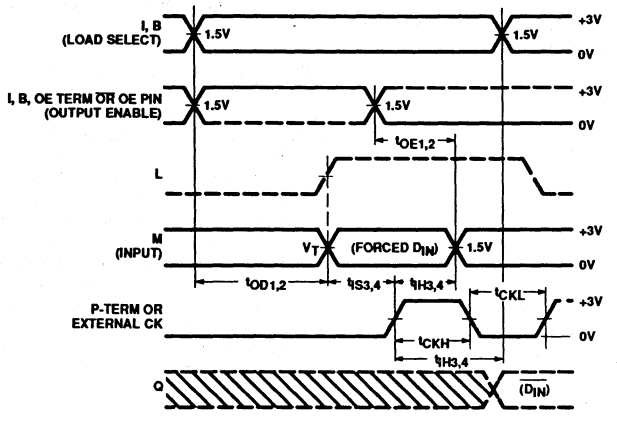
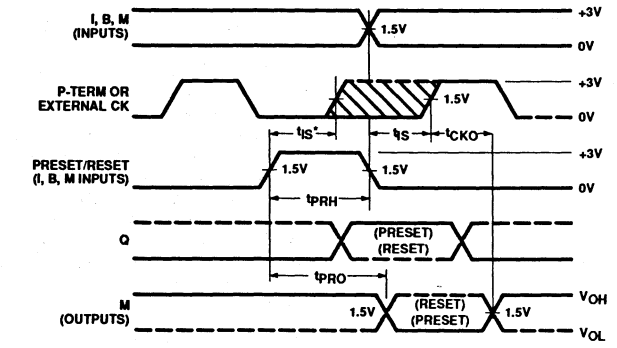
TIMING DIAGRAMS (Continued)

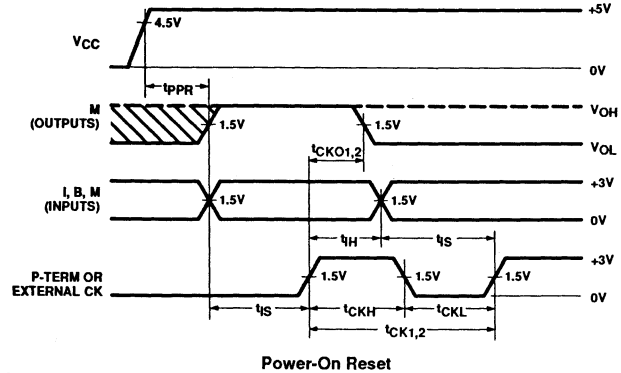


Flip-Flop Input Mode (Preload)



*Preset and Reset functions override Clock. However, M outputs may glitch with the first positive Clock Edge if t_{IS} cannot be guaranteed by the user.

Asynchronous Preset/Reset



Power-On Reset

TIMING DEFINITIONS (Continued)

SYMBOL	PARAMETER
t_{IH2}	Required delay between positive transition of P-term Clock and end of valid input data.
t_{IH3}	Required delay between positive transition of External Clock and end of valid input data when using Preload Inputs (from M pins).
t_{IH4}	Required delay between positive transition of P-term Clock and end of valid input data when using Preload Inputs (from M pins).
t_{IS1}	Required delay between beginning of valid input and positive transition of External Clock.
t_{IS2}	Required delay between beginning of valid input and positive transition of P-term Clock input.
t_{IS3}	Required delay between beginning of valid Preload input (from M pins) and positive transition of External Clock.
t_{IS4}	Required delay between beginning of valid Preload input (from M pins) and positive transition of P-term Clock input.
t_{IS5}	Required delay between beginning of valid input through Complement Array and positive transition of External Clock.
t_{IS6}	Required delay between beginning of valid input through Complement Array and positive transition of P-term Clock input.
t_{OE1}	Delay between beginning of Output Enable signal (Low) from /OE pin and when Outputs become valid.
t_{OE2}	Delay between beginning of Output Enable signal (High or Low) from OE P-term and when Outputs become valid.
t_{OD1}	Delay between beginning of Output Enable signal (HIGH) from /OE pin and when Outputs become disabled.
t_{OD2}	Delay between beginning of Output Enable signal (High or Low) from OE P-term and when Outputs become disabled.
t_{PD}	Delay between beginning of valid input and when the Outputs become valid (Combinatorial Path).
t_{PRH}	Width of Preset/Reset Pulse.
t_{PRO}	Delay between beginning of valid Preset/Reset Input and when the registered Outputs become Preset ("1") or Reset ("0").
t_{PPR}	Delay between V_{CC} (after power-up) and when flip-flops become Reset to "0". Note: Signal at Output (M pin) will be inverted.

CMOS programmable multi-function PLD (42 × 105 × 12)

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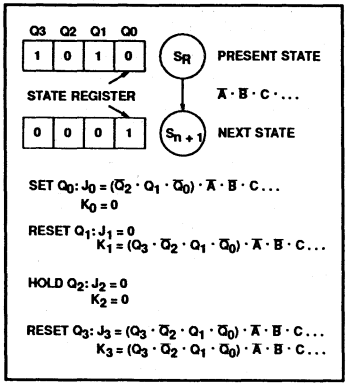
LOGIC FUNCTION



NOTE:
Similar logic functions are applicable for D mode flip-flops.

FLIP-FLOP TRUTH TABLE

$\overline{OE}$	L_n	CK_n	P_n	R_n	J	K	Q	M
H								Hi-Z
L	X	X	X	X	X	X	L	H
L	X	X	H	L	X	X	H	L
L	X	X	L	H	X	X	L	H
L	L	↑	L	L	L	L	Q	$\overline{Q}$
L	L	↑	L	L	L	H	L	H
L	L	↑	L	L	H	L	H	L
L	L	↑	L	L	H	H	$\overline{Q}$	Q
H	H	↑	L	L	L	H	L	H*
H	H	↑	L	L	H	L	H	L*
+10V	X	↑	X	X	L	H	L	H**
	X	↑	X	X	H	L	H	L**

NOTES:
1. Positive Logic:
   $J\text{-}K = \overline{T}_0 + \overline{T}_1 + T_2 + \ldots + T_{31}$
   $T_n = \overline{C} \cdot (I0 \cdot \overline{I1} \cdot I2\ldots) \cdot (Q0 \cdot \overline{Q1}\ldots) \cdot (B0 \cdot \overline{B1}\ldots)$
2. ↑ denotes transition for Low to High level.
3. X = Don't care
4. * = Forced at M_n pin for loading the J-K flip-flop in the Input mode. The load control term, L_n must be enabled (HIGH) and the p-terms that are connected to the associated flip-flop must be forced LOW (disabled) during Preload.
5. At P = R = H, Q = H. The final state of Q depends on which is released first.
6. ** = Forced at F_n pin to load J/K flip-flop (Diagnostic mode).

PLC42VA12I UNPROGRAMMED STATE

A factory shipped unprogrammed device is configured such that all cells are in a conductive state.

The following are:

ACTIVE:
- OR array logic terms
- Output Macro Cells M1 – M8;
  - D-type registered outputs (D = 0)
- External clock path
- Inputs: B0, B1, M0, M9.

INACTIVE:
- AND array logic and control terms (except flip-flop mode control term, F_C)
- Bidirectional I/O (B0, B1);
  - Inputs are active. Outputs are 3-Stated via the OE P-terms, D0 and D1
  - D-type registers (D = 0).
- Output Macro Cells M0 and M9;
  - Bidirectional I/O, 3-Stated via the OE P-terms, DM0 and DM9. The inputs are active
- P-term clocks
- Complement Array
- J-K Flip-Flop mode.

ERASURE CHARACTERISTICS (For Quartz Window Packages Only)

The erasure characteristics of the PLC42VA12I devices are such that erasure begins to occur upon exposure to light with wavelength shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000 – 4000Å range. Data shows that constant exposure to room level fluorescent lighting could erase a typical PLC42VA12I in approximately three years, while it would take approximately one week to cause erasure when exposed to direct sunlight. If the PLC42VA12I is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

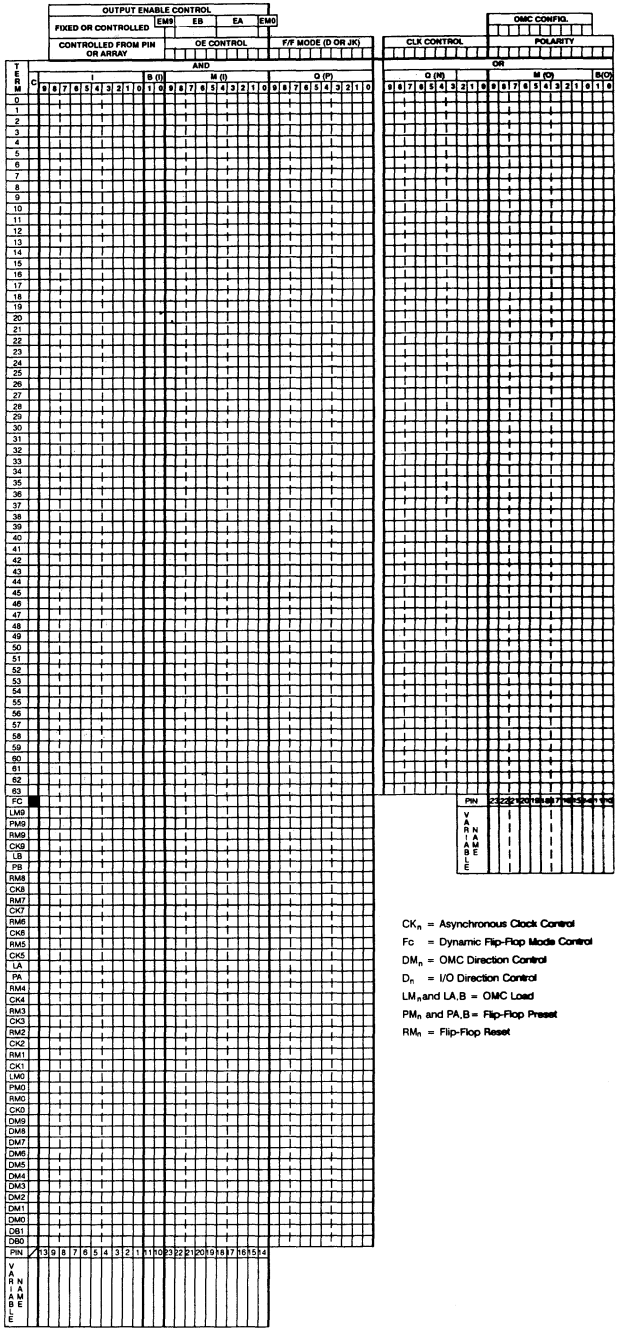
The recommended erasure procedure for the PLC42VA12I is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15Wsec/cm^2. The erasure time with this dosage is approximately 30 to 35 minutes using an ultraviolet lamp with a 12,000µW/cm^2 power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose a CMOS EPLD can be exposed to without damage is 7258Wsec/cm^2 (1 week @ 12000µW/cm^2). Exposure of these CMOS EPLDs to high intensity UV light for longer periods may cause permanent damage.

The maximum number of guaranteed erase/write cycles is 50. Data retentions exceeds 20 years.

CMOS programmable multi-function PLD (42 × 105 × 12)

PLC42VA12I

PROGRAM TABLE

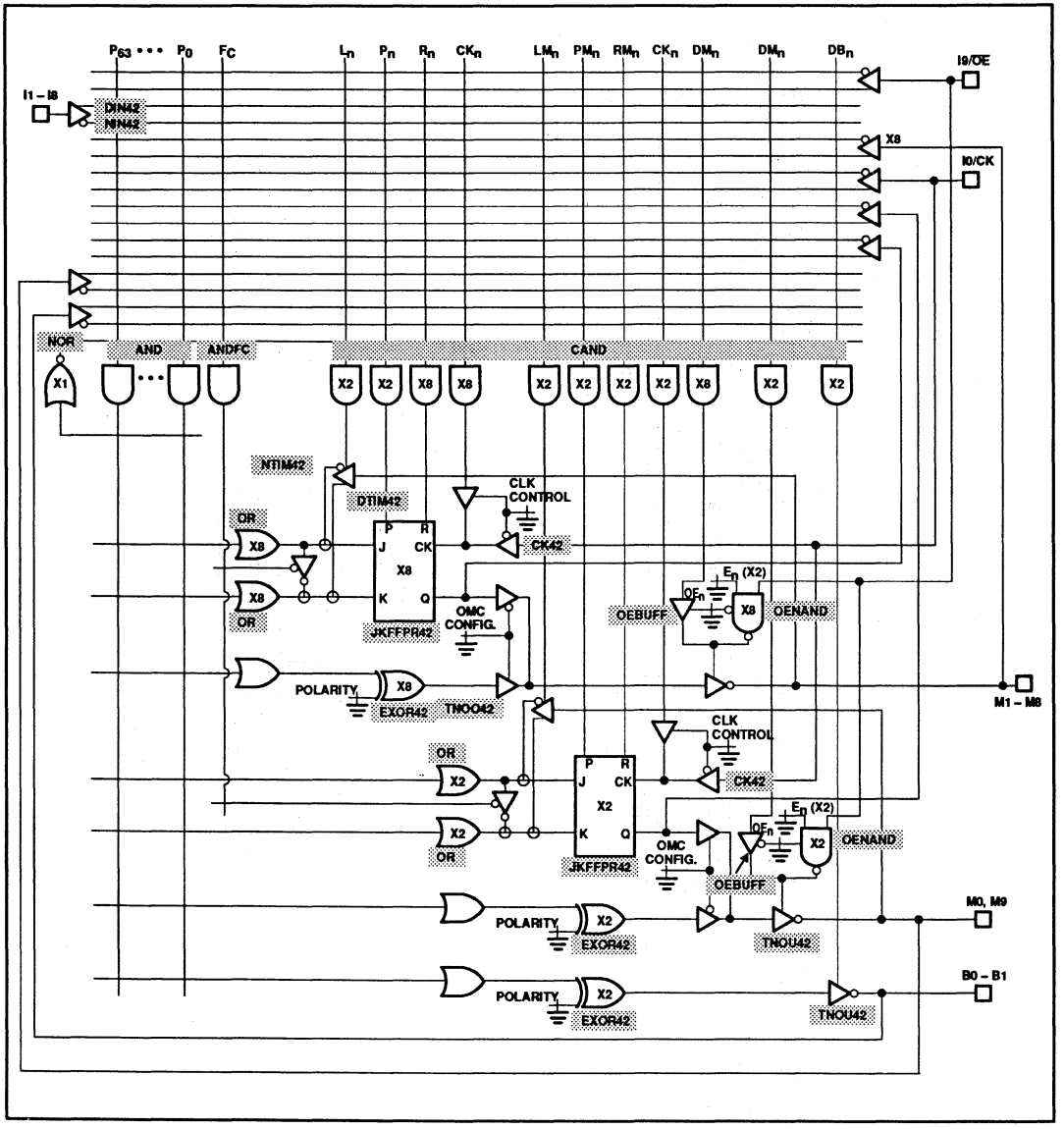


CK_n = Asynchronous Clock Control
Fc = Dynamic Flip-Flop Mode Control
DM_n = OMC Direction Control
D_n = I/O Direction Control
LM_n and LA,B = OMC Load
PM_n and PA,B = Flip-Flop Preset
RM_n = Flip-Flop Reset

CMOS programmable multi-function PLD (42 × 105 × 12)

PLC42VA12I

SNAP RESOURCE SUMMARY DESIGNATIONS



CMOS programmable logic sequencer (17 × 68 × 8)

PLC415-16

DESCRIPTION

The PLC415-16 PLD is a CMOS Programmable Logic Sequencer of the Mealy type. The PLC415-16 is a pin-for-pin compatible, functional superset of the PLS105 and PLUS405 Bipolar Programmable Logic Sequencer devices.

The PLC415 is ideally suited for high density, power sensitive controller functions. The Power Down feature provides true CMOS standby power levels of less than 100µA. The EPROM-based process technology supports operating frequencies of 16 to 20MHz. The PLC415-16 has been designed to accept both CMOS and TTL input levels to facilitate logic integration in almost any system environment.

The PLC415 architecture has been tailored for state machine functions. Both arrays are programmable, thus providing full interconnectability. Any one or all of the 64 AND transition terms can be connected to any (or all) of the 8 buried state and 8 output registers.

Two clock sources enable the design of 2 state machines on one chip. Separate INIT functions and Output Enable functions for each are controllable either from the array or from an external pin. The J-K flip-flops provide the added flexibility of the toggle function which is indeterminate on S-R flip-flops. The programmable Initialization feature supports asynchronous initialization of the state machine to any user defined pattern.

The unique Complement Array feature supports complex ELSE transition statements with a single product term. The PLC415-16 has 2 Complement Arrays which allows the user to design two independent complement functions. This is particularly useful if two state machines have been implemented on one chip.

FEATURES

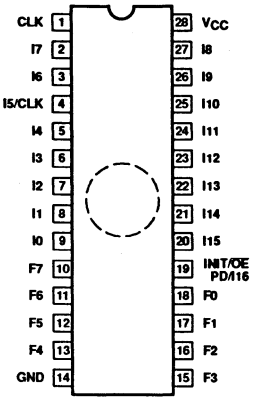
- Pin-for-Pin compatible, functional superset of PLS105/A and PLUS405 Logic Sequencers
- Zero standby power of less than 100µA (worst case)
  - Power dissipation at f_{MAX} = 80mA (worst case)
- CMOS and TTL compatible
- Programmable asynchronous Initialization and OE functions
  - Controllable from AND Array or external source
- 17 input variables
- 8 output functions
- 68 Product Terms
  - 64 transition terms
  - 4 control terms
- 8-bit State Register
- 8-bit Output Register
- 2 Transition Complement Arrays
- Multiple clocks
- Diagnostic test modes features for access to state and output registers
- Power-on preset of all registers to "1"
- J-K flip-flops
  - Automatic Hold states
- Security Fuse
- 3-State outputs

APPLICATIONS

- Interface protocols
- Sequence detectors
- Peripheral controllers
- Timing generators
- Arbitration functions
- Sequential circuits
- Security locking systems
- Counters
- Shift Registers

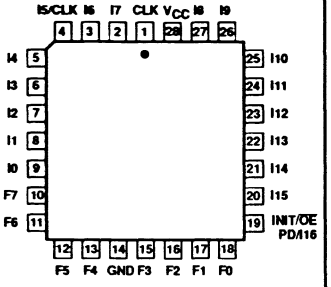
PIN CONFIGURATIONS

N, FA Packages



NOTE:
N = Plastic DIP (600mil-wide)
FA = Ceramic DIP with Quartz window (600mil-wide)

A Package



NOTE:
A = Plastic Leaded Chip Carrier

ORDERING INFORMATION

DESCRIPTION	OPERATING FREQUENCY	ORDER CODE
28-Pin Ceramic DIP with window; Reprogrammable (600mil-wide)	f_{MAX} = 16MHz	PLC415–16FA
28-Pin Plastic DIP; One-Time Programmable (600mil-wide)	f_{MAX} = 16MHz	PLC415–16N
28-Pin Plastic Leaded Chip Carrier; One-Time Programmable (450mil-wide)	f_{MAX} = 16MHz	PLC415–16A

CMOS programmable logic sequencer (17 × 68 × 8) — PLC415-16

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION	POLARITY
1	CLK1	**Clock:** The Clock input to the State and Output Registers. A Low-to-High transition on this line is necessary to update the contents of both registers. Pin 1 only clocks P0–3 and F0–3 if Pin 4 is also being used as a clock.	Active-High (H)
2, 3, 5–9, 26–27 20–22	I0–I4, I7, I6 I8–I9 I13–I15	**Logic Inputs:** The 12 external inputs to the AND array used to program jump conditions between machine states, as determined by a given logic sequence. True and complement signals are generated via use of "H" and "L".	Active-High/Low (H/L)
4	I5/CLK2	**Logic Input/Clock:** A user programmable function:	
		• **Logic Input:** A 13th external logic input to the AND array, as above.	Active-High/Low (H/L)
		• **Clock:** A 2nd clock for the State Registers P4–7 and Output Registers F4–7, as above. Note that input buffer I_5 must be deleted from the AND array (i.e., all fuse locations "Don't Care") when using Pin 4 as a Clock.	Active-High (H)
23	I12	**Logic/Diagnostic Input:** A 14th external logic input to the AND array, as above, when exercising standard TTL or CMOS levels. When I12 is held at +11V, device outputs F0–F7 reflect the contents of State Register bits P0–P7. The contents of each Output Register remains unaltered.	Active-High/Low (H/L)
24	I11	**Logic/Diagnostic Input:** A 15th external logic input to the AND array, as above, when exercising standard TTL or CMOS levels. When I11 is held at +11V, device outputs F0–F7 become direct inputs for State Register bits P0–P7; a Low-to-High transition on the appropriate clock line loads the values on pins F0–F7 into the State Register bits P0–P7. The contents of each Output Register remains unaltered.	Active-High/Low (H/L)
25	I10	**Logic/Diagnostic Input:** A 16th external logic input to the AND array, as above, when exercising standard TTL or CMOS levels. When I10 is held at +11V, device outputs F0–F7 become direct inputs for Output Register bits Q0–Q7; a Low-to-High transition on the appropriate clock line loads the values on pins F0–F7 into the Output Register bits Q0–Q7. The contents of each State Register remains unaltered.	Active-High/Low (H/L)
10–13 15–18	F0–F7	**Logic Outputs/Diagnostic Outputs/Diagnostic Inputs:** Eight device outputs which normally reflect the contents of Output Register Bits Q0–Q7, when enabled. When I12 is held at +11V, F0–F7 = (P0–P7). When I11 is held at +11V, F0–F7 become inputs to State Register bits P0–P7. When I10 is held at +11V, F0–F7 become inputs to Output Register bits Q0–Q7.	Active-High (H)
19	INIT/$\overline{OE}$ I16/PD	**External Initialization, External /OE, PD or I16:** A user programmable function: Only one of the four options below may be selected. Note that both Initialization and /OE options are alternately available via the AND array. (P-terms INA, INB, OEA, and OEB.)	
		• **External Initialization:** Provides an asynchronous Preset to logic "1" or Reset to logic "0" of any or all State and Output Registers, determined individually on a register-by-register basis. INIT overrides the clock, and when held High, clocking is inhibited. Normal clocking resumes with the first full clock pulse following a High-to-Low clock transition, after the INIT pulse goes Low. See timing diagrams for t_{NVCK} and t_{VCK}. Note that if the External Initialization option is selected, I16 is disabled automatically via the design software and the Power Down and External OE options are not available. Internal OE is available via P-Terms OEA and/or OEB. This option can be selected for one or both banks of registers.	Active-High (H)
		• **External Output Enable:** Provides an Output Enable/Disable function for Output Registers. Note that if the External OE option is selected, I16 is disabled automatically via the design software and the Power Down and External INIT options are not available. Internal INIT is available via P-terms INA and/or INB. This option can be selected for one or both banks of registers.	Active-Low (L)
		• **Power Down:** When invoked, provides a Power Down (zero power) mode. The contents of all Registers is retained, despite the toggling of the Inputs or the clocks. To obtain the lowest possible power level, all Inputs should be static and at CMOS input levels. Note that if the PD options is selected, I_{16} is disabled automatically via the design software and the External INIT and External OE options are not available. Internal INIT is available via P-terms INA and/or INB and Internal OE is available via P-terms OEA and/or OEB.	Active-High (H)
		• **Logic Input:** The 17th external logic input to the AND array as above. Note that when the I16 option is selected, the Power Down, External /OE and External INIT are not available. Internal OE and Internal INIT are available from P-Terms OEA/OEB and INA/INB, respectively.	Active-High/Low (H/L)

CMOS programmable logic sequencer (17 × 68 × 8)

PLC415-16

TRUTH TABLE [1, 2, 3, 4, 5]

V_{CC}	OPTION										
	INIT	$\overline{OE}$	I_{10}	I_{11}	I_{12}	CK	J	K	Q_P	Q_F	F
+5V	H		X	X	X	X	X	X	H/L	H/L	Q_F
	X		+11V	X	X	↑	X	X	Q_P	L	L
	X		+11V	X	X	↑	X	X	Q_P	H	H
	X		X	+11V	X	↑	X	X	L	Q_F	L
	X		X	+11V	X	↑	X	X	H	Q_F	H
	X		X	X	+11V	X	X	X	Q_P	Q_F	Q_P
	L		X	X	X	X	X	X	Q_P	Q_F	Q_F
		H	X	X	X	X	X	X	Q_P	Q_F	Hi-Z
		X	+11V	X	X	↑	X	X	Q_P	L	L
		X	+11V	X	X	↑	X	X	Q_P	H	H
		X	X	+11V	X	↑	X	X	L	Q_F	L
		X	X	+11V	X	↑	X	X	H	Q_F	H
		L	X	X	+11V	X	X	X	Q_P	Q_F	Q_P
		L	X	X	X	X	X	X	Q_P	Q_F	Q_F
		L	X	X	X	↑	L	L	Q_P	Q_F	Q_F
		L	X	X	X	↑	L	H	L	L	L
		L	X	X	X	↑	H	L	H	H	H
		L	X	X	X	↑	H	H	$\overline{Q_P}$	$\overline{Q_F}$	$\overline{Q_F}$
↑	L	L	X	X	X	X	X	X	H	H	

NOTES:

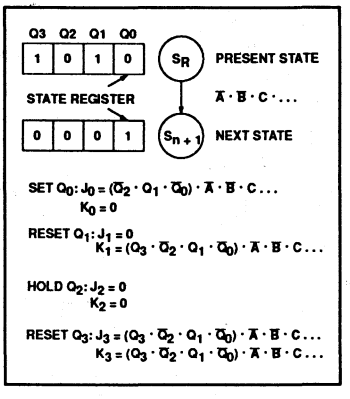
1. Positive Logic:
   S/R (or J/K) = $T_0 + T_1 + T_2 + \ldots T_{63}$
   $T_n = (C_0, C_1)(I0, I1, I2, \ldots)$ (P0, P1 . . . P7)
2. ↑ denotes transition from Low-to-High level.
3. X = Don't Care (≤5.5V)
4. H/L implies that either a High or a Low can occur, depending upon user-programmed Initialization selection (each State and Output Register individually programmable).
5. When using the F_n pins as inputs to the State and Output Registers in diagnostic mode, the F buffers are 3-Stated and the indicated levels on the output pins are forced by the user.

VIRGIN STATE

A factory-shipped virgin device contains all fusible links intact, such that:

1. INIT/$\overline{OE}$/PD/I16 is set to INIT. In order to use the INIT function, the user must select either the PRESET or the RESET option for each flip-flop. Note that regardless of the user-programmed initialization, or even if the INIT function is not used, all registers are preset to "1" by the power-up procedure.
2. All transition terms are inactive (0).
3. All J/K flip-flop inputs are disabled (0).
4. The Complement Arrays are inactive.
5. Clock 1 is connected to all State and Output Registers.

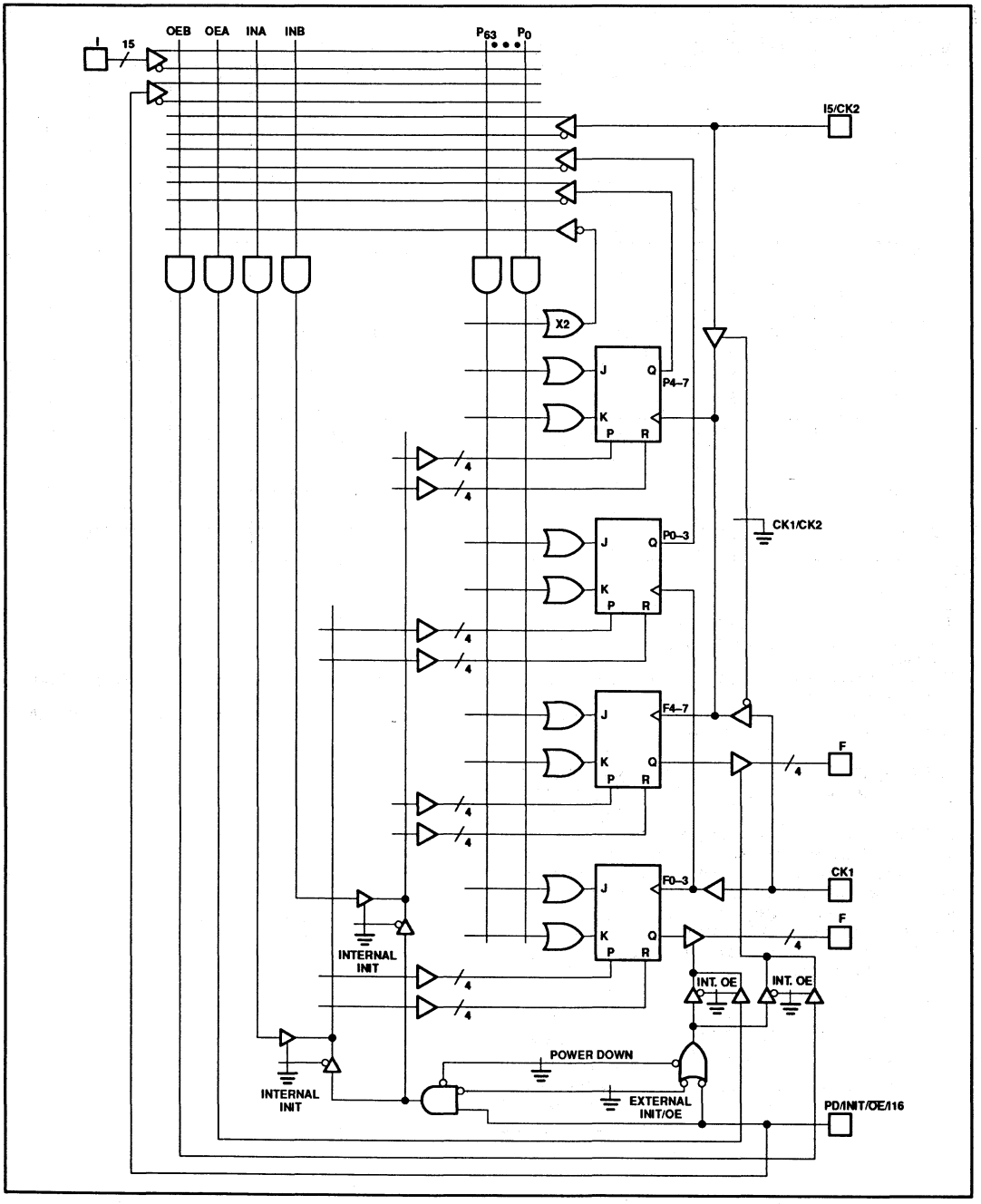
LOGIC FUNCTION



CMOS programmable logic sequencer (17 × 68 × 8)

PLC415-16

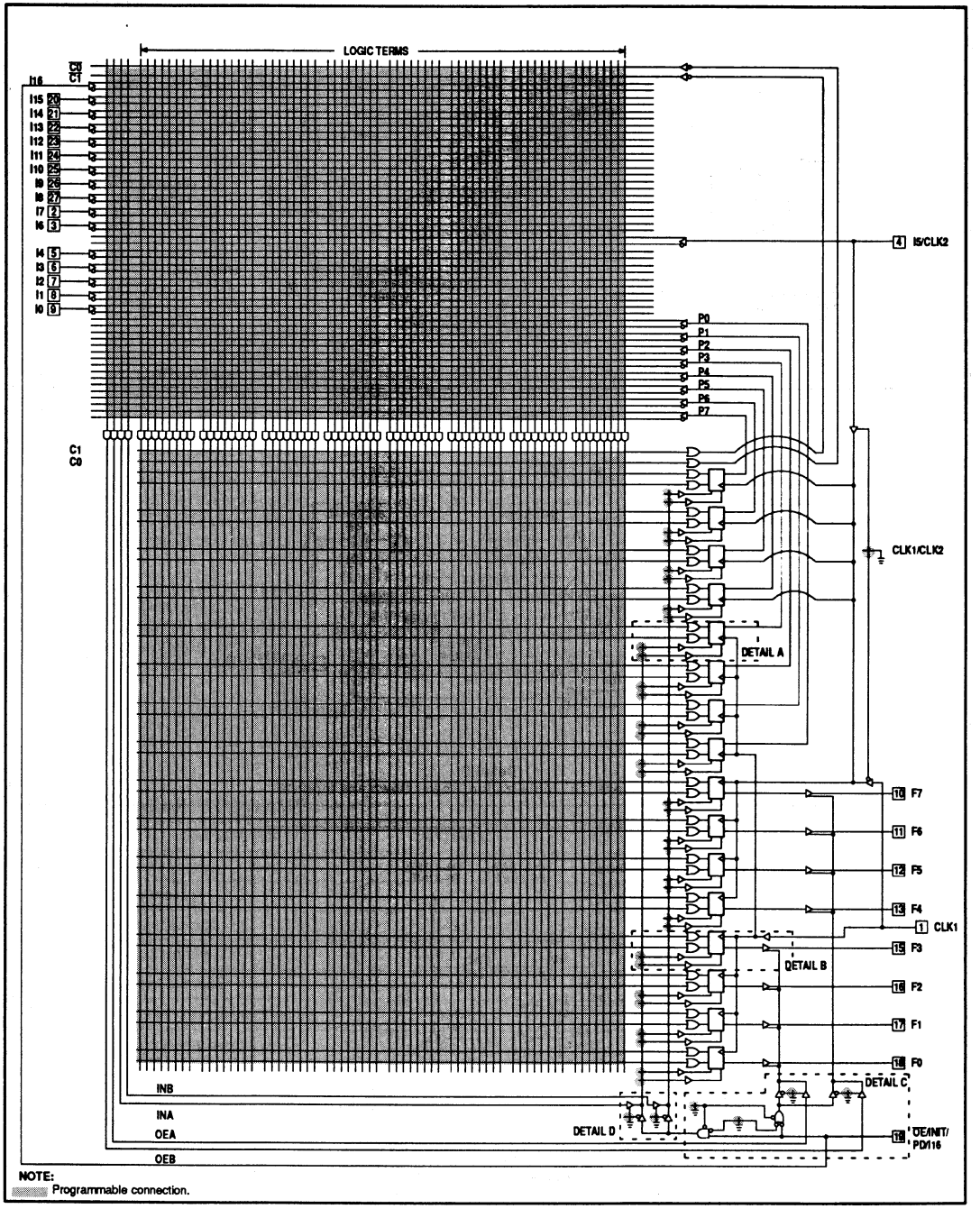
FUNCTIONAL DIAGRAM



CMOS programmable logic sequencer (17 × 68 × 8)

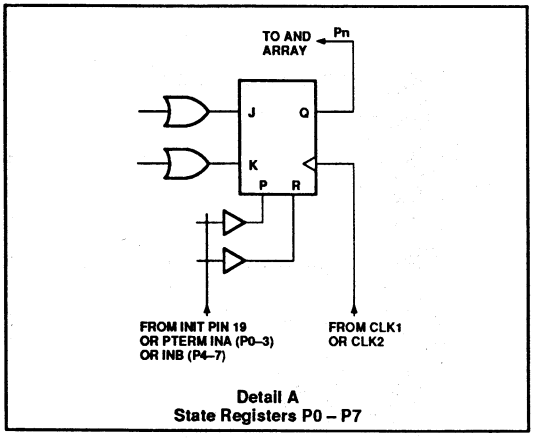
PLC415-16

LOGIC DIAGRAM

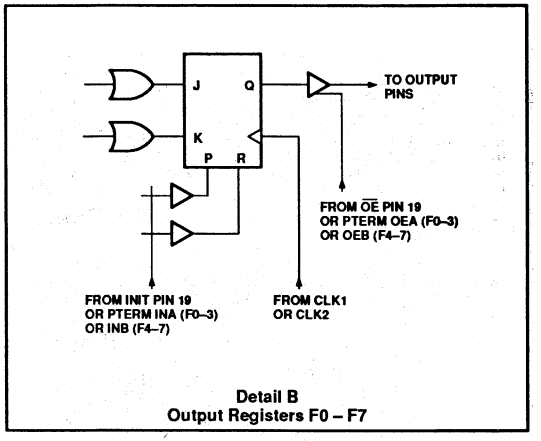


NOTE:
Programmable connection.

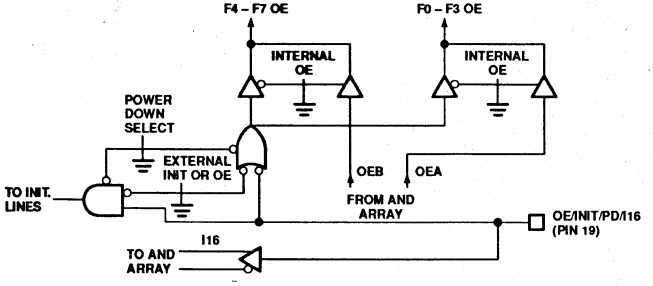
DETAILS FOR PLC415-16 LOGIC DIAGRAM



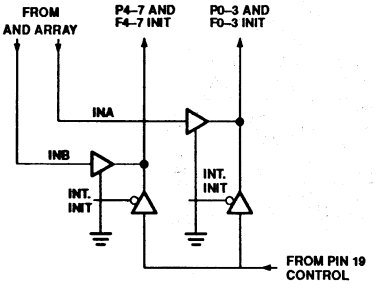
Detail A
State Registers P0 – P7



Detail B
Output Registers F0 – F7



Detail C
Pin 19 Options: $\overline{OE}$, Initialization, Power Down and Input 16

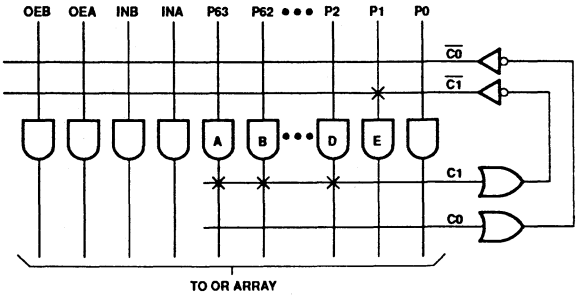


Detail D
Internal and External Initialization

CMOS programmable logic sequencer (17 × 68 × 8)

PLC415-16

DETAILS FOR PLC415-16 LOGIC DIAGRAM (Continued)



Complement Array Detail

The Complement Array is a special sequencer feature that is often used for detecting illegal states. It is also ideal for generating IF-THEN-ELSE logic statements with a minimum number of product terms.

The concept is deceptively simple. If you subscribe to the theory that the expressions (/A • /B • /C) and ($\overline{A + B + C}$) are equivalent, you will begin to see the value of this single term NOR array.

The Complement Array is a single OR gate with inputs from the AND array. The output of the Complement Array is inverted and fed back to the AND array (NOR). The output of the array will be Low if any one or more of the AND terms connected to it are active (High). If, however, all the connected terms are inactive (Low), which is a classic unknown state, the output of the Complement Array will be High.

Consider the Product Terms A, B and D that represent defined states. They are also connected to the input of the Complement Array. When the condition (not A and not B and not D) exists, the Complement Array will detect this and propagate an Active-High signal to the AND array. This signal can be connected to Product Term E, which could be used in turn to reset the state machine to a known state. Without the Complement Array, one would have to generate product terms for all unknown or illegal states. With very complex state machines, such an approach can be prohibitive, both in terms of time and wasted resources.

Note that the PLC416-16 has 2 Complement Arrays which allow the user to design 2 independent Complement functions. This is particularly useful if 2 independent state machines have been implemented on one device.

Note that use of the Complement Array adds an additional delay path through the device. Please refer to the AC Electrical Characteristics for details.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_{OUT}	Output voltage	+5.5	V_{DC}
I_{IN}	Input currents	–30 to +30	mA
I_{OUT}	Output currents	+100	mA
T_{amb}	Operating temperature range	0 to +75	°C
T_{stg}	Storage temperature range	–65 to +150	°C

NOTES:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

CMOS programmable logic sequencer (17 × 68 × 8)

PLC415-16

DC ELECTRICAL CHARACTERISTICS

$0°C \le T_{amb} \le +75°C$, $4.75 \le V_{CC} \le 5.25V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS MIN	LIMITS TYP[1]	LIMITS MAX	UNIT
Input voltage[2]						
V_{IL}	Low	V_{CC} = MIN	–0.3		0.8	V
V_{IH}	High	V_{CC} = MAX	2.0		V_{CC} + 0.3	V
Output voltage[2]						
V_{OL}	Low	V_{CC} = MIN I_{OL} = 16mA			0.5	V
V_{OH}	High	I_{OH} = –3.2mA	2.4			V
Input current						
I_{IL}	Low	V_{IN} = GND			–10	µA
I_{IH}	High	V_{IN} = V_{CC}			10	µA
Output current						
$I_{O(OFF)}$	Hi-Z state	V_{OUT} = V_{CC} V_{OUT} = GND			10 –10	µA µA
I_{OS}	Short-circuit[3, 6]	V_{OUT} = GND			–130	mA
I_{CCSB}	V_{CC} supply current with PD asserted[7]	V_{CC} = MAX V_{IN} = 0 or V_{CC}		50	100	µA
I_{CC}	V_{CC} supply current Active[4, 5]	I_{OUT} = 0mA, at f = 1MHz			55	mA
	(TTL or CMOS Inputs)	V_{CC} = MAX, at f = MAX			80	mA
Capacitance						
C_I	Input	V_{CC} = 5V V_{IN} = 2.0V		12		pF
C_B	I/O	V_B = 2.0V		15		pF

NOTES:
1. All typical values are at V_{CC} = 5V. T_{amb} = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Duration of short-circuit should not exceed one second. Test one at a time.
4. Tested with TTL input levels: V_{IL} = 0.45V, V_{IH} = 2.4V. Measured with all inputs and outputs switching.
5. Refer to Figure 1, I_{CC} vs Frequency (worst case).
6. Refer to Figure 2 for Δt_{PD} vs output capacitance loading.
7. The outputs are automatically 3-Stated when the device is in the Power Down mode. To achieve the lowest possible current, the inputs and clocks should be at CMOS static levels.

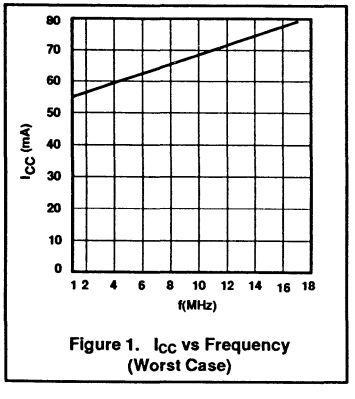


Figure 1. I_{CC} vs Frequency (Worst Case)

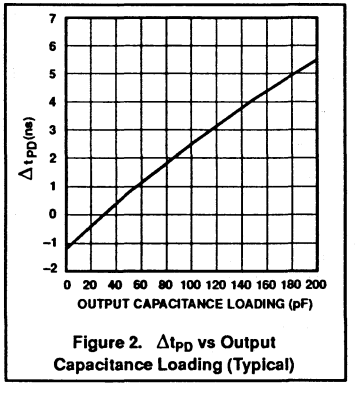


Figure 2. Δt_{PD} vs Output Capacitance Loading (Typical)

AC ELECTRICAL CHARACTERISTICS

$R_1 = 252\Omega$, $R_2 = 178\Omega$, $0°C \le T_{amb} \le +75°C$, $4.75 \le V_{CC} \le 5.25V$

SYMBOL	PARAMETER	FROM	TO	TEST CONDITION	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Pulse width								
t_{CKH}	Clock High	CK+	CK–	30pF	25	10		ns
t_{CKL}	Clock Low	CK–	CK+	30pF	25	10		ns
t_{INITH}	Initialization Input pulse	INIT+	INIT–	30pF	20			ns
Set–up time								
t_{IS1}	Input	(I) +/–	CK+	30pF	38	25		ns
t_{IS2}[1]	Input through Complement array	(I) +/–	CK+	30pF	60	40		ns
t_{ISPD}	Power Down Setup (from PD pin)	PD+	CK+	30pF	38	15		ns
t_{ISPU}	Power Up Setup (from PD pin)	PD–	First Valid CK+	30pF	38	30		ns
t_{VS}[1]	Power on Preset Setup	V_{CC}+	CK–	30pF	0			ns
t_{VCK1}	Clock resume (after INIT) when using INIT pin (pin 19)	INIT–	CK–	30pF	10	–5		ns
t_{VCK2}[1]	Clock resume (after INIT) when using P-term INIT (from AND array)	(I) +/–	CK–	30pF	20	8		ns
t_{NVCK1}	Clock lockout (before INIT) when using INIT pin (pin 19)	CK–	INIT–	30pF	10	–3		ns
t_{NVCK2}[1]	Clock lockout (before INIT) when using P-term INIT (from AND array)	CK–	INIT–	30pF	0	–5		ns
Propagation delays								
t_{CKO}	Clock to Output	CK+	(F) +/–	30pF		15	22	ns
t_{PDZ}	Power Down to outputs off	PD+	Outputs Off	5pF		25	30	ns
t_{PUA1}	Power Up to outputs Active with dedicated Output Enable	PD–	Outputs Active	30pF		20	35	ns
t_{PUA2}[1]	Power Up to outputs Active with P-term Output Enable[1]	PD–	Outputs Active	30pF		37	55	ns
t_{IHPU}	Last valid clock to Power Down delay (Hold)	Last Valid Clock	PD+	30pF	25	15		ns
t_{IHPD}	First valid clock cycle before Power Up	Beginning of First Valid Clock Cycle	PD–	30pF	0	–25		ns
t_{OE1}[3]	Output Enable: from /OE pin	OE–	Output Enabled	30pF		15	30	ns
t_{OE2}[1]	Output Enable; from P–term	(I) +/–	Output Enabled	30pF		25	40	ns
t_{OD1}[3]	Output Disable; from /OE pin	OE+	Output Disabled	5pF		20	30	ns
t_{OD2}[3]	Output Disable; from P-term	(I) +/–	Output Disabled	5pF		30	40	ns
t_{INIT1}	INIT to output when using INIT pin	INIT+	(F) +/–	30pF		22	35	ns
t_{INIT2}	INIT to output when using P-term INIT	(I) +/–	(F) +/–	30pF		35	45	ns
t_{PPR}[1]	Power-on Preset (F_n = 1)	V_{CC} +	(F) +	30pF			15	ns
t_{RP1}	Registered operating period; (t_{IS1} + t_{CKO1})	(I) +/–	(F) +/–	30pF		40	60	ns
t_{RP2}[1]	Registered operating period with Complement Array (t_{IS2} + t_{CKO1})	(I) +/–	(F) +/–	30pF		55	75	ns

Notes on following page

AC ELECTRICAL CHARACTERISTICS (Continued)

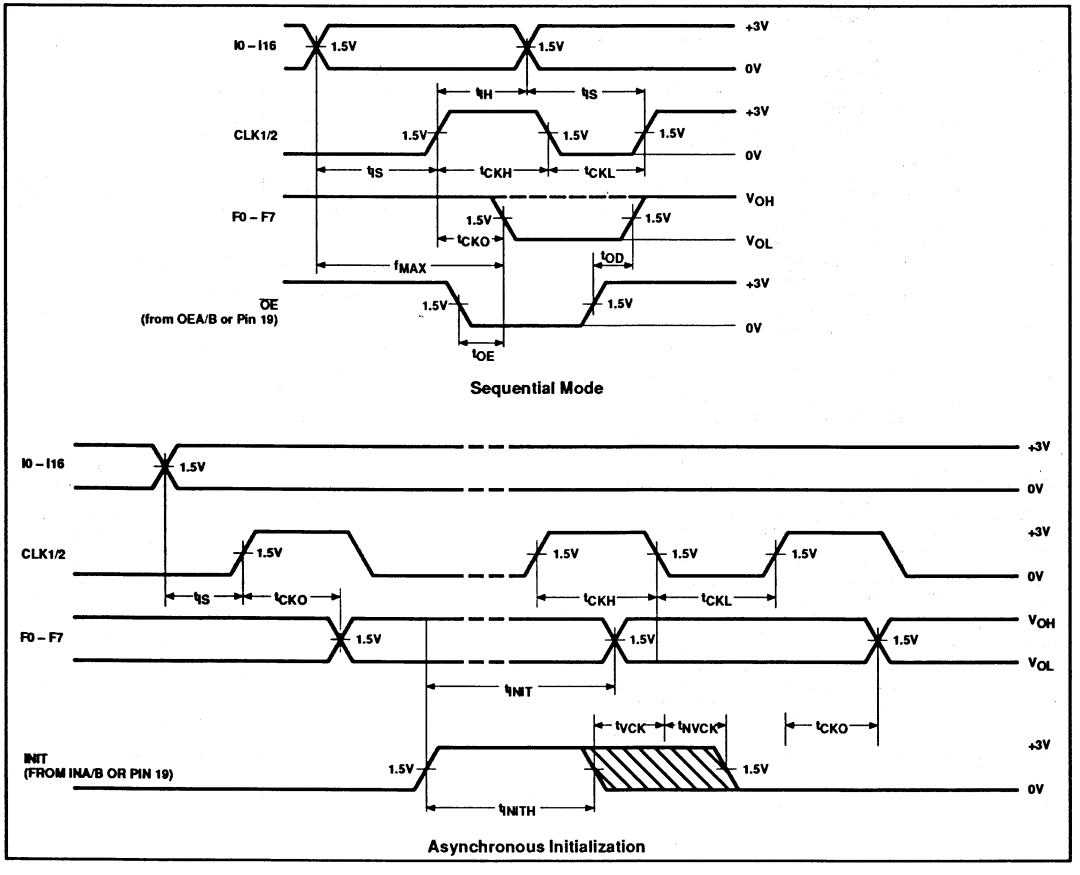
$R_1 = 252\Omega$, $R_2 = 178\Omega$, $0°C \le T_{amb} \le +75°C$, $4.75 \le V_{CC} \le 5.25V$

SYMBOL	PARAMETER	FROM	TO	TEST CONDITION	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Hold time								
t_{IH}	Input Hold	CK+	(F) +/–	30pF		–10	0	ns
Frequency of operation								
f_{CLK}[1]	Clock (toggle) frequency	C+	C+	30pF	20	50		MHz
f_{MAX1}	Registered operating frequency ($t_{IS1} + t_{CKO1}$)	(I) +/–	(F) +/–	30pF	16.7	25		MHz
f_{MAX2}	Registered operating frequency with Complement Array ($t_{IS2} + t_{CKO1}$)[1]	(I) +/–	(F) +/–	30pF	13.3	18.2		MHz

NOTE:

1. Not 100% tested, but guaranteed by design/characterization.
2. All propagation delays and setup times are measured and specified under worst case conditions.
3. For 3-State output; output enable times are tested with $C_L = 30pF$ to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with $C_L = 5pF$. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} - 0.5V)$ with S_1 open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with S_1 closed.

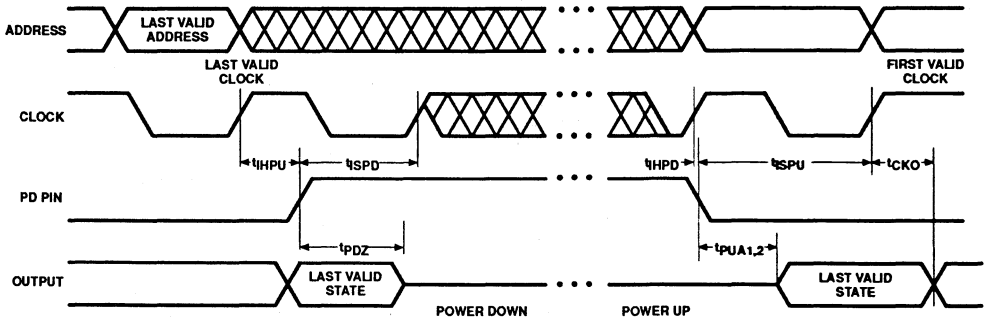
TIMING DIAGRAMS



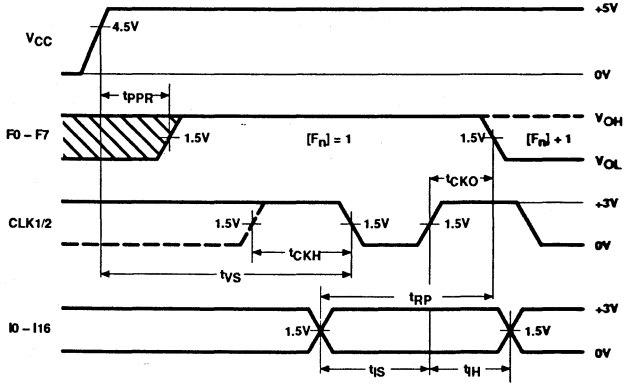
The PLC416-16 has a unique power down feature that is ideal for power sensitive controller and state machine applications. During idle periods, the PLC415 can be powered down to a near zero power consumption level of less than 100 micro Amps. Externally controlled from Pin 19, the power down sequence first saves the data in all the State and Output registers. In order to insure that the last valid states are saved, there are certain hold times associated with the first and last valid clock edges and the Power Down input pulse. The Outputs are then automatically 3-Stated and power consumption is reduced to a minimum.

Once in the power down mode, any or all of the inputs, including the clocks, may be toggled without the loss of data. To obtain the lowest possible power level, the inputs should be at static CMOS input levels during the power down period.

TIMING DIAGRAMS (Continued)

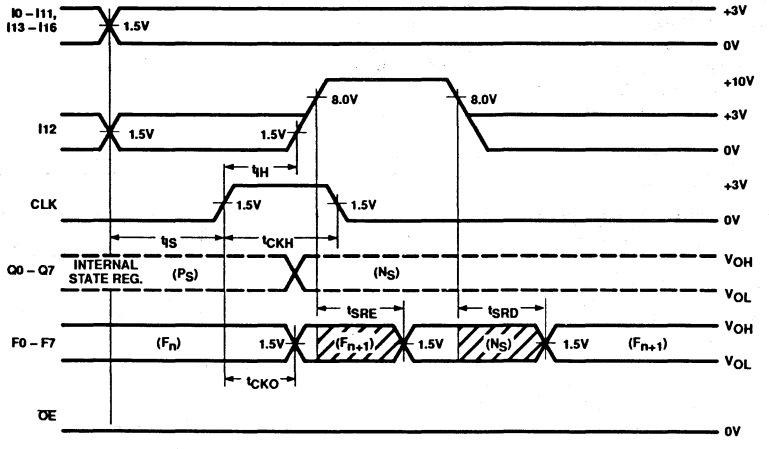


Power Down Enable and Disable

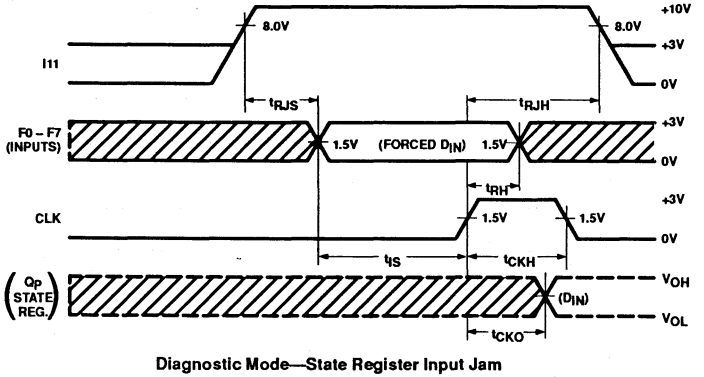


Power-On Preset

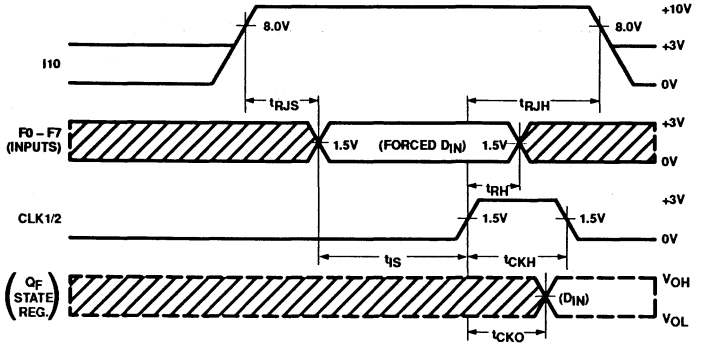
TIMING DIAGRAMS (Continued)



Diagnostic Mode—State Register Outputs



Diagnostic Mode—State Register Input Jam



Diagnostic Mode—Output Register Input Jam

TIMING DEFINITIONS

SYMBOL	PARAMETER
f_{CLK}	Minimum guaranteed toggle frequency of the clock (from Clock HIGH to Clock HIGH).
$f_{MAX1,2}$	Minimum guaranteed operating frequency.
t_{CKH}	Width of input clock pulse.
t_{CKL}	Interval between clock pulses.
t_{RP1}	Minimum guaranteed operating period – when not using Complement Array.
t_{RP2}	Minimum guaranteed operating period – when using Complement Array.
t_{CKO}	Delay between positive transition of Clock and when Outputs become valid (with outputs enabled).
t_{IH}	Required delay between positive transition of Clock and end of valid Input data.
t_{IHPD}	Required delay between the positive transition of the beginning of the first valid clock cycle to the beginning of Power Down LOW to insure that the last valid states are intact and that the next positive transition of the clock is valid.
t_{IHPU}	Required delay between the positive transition of the last valid clock and the beginning of Power Down HIGH to insure that last valid states are saved.
t_{INITH}	Width of initialization input pulse.
t_{INIT1}	Delay between positive transition of Initialization and when Outputs become valid when using external INIT control (from pin 19).
t_{INIT2}	Delay between positive transition of Initialization and when outputs become valid when using internal INIT control (from P-terms INA and INB).
t_{ISPD}	Required delay between the beginning of Power Down HIGH (from pin 19) and the positive transition of the next clock to insure that the clock edge is not detected as a valid Clock and that the last valid states are saved.

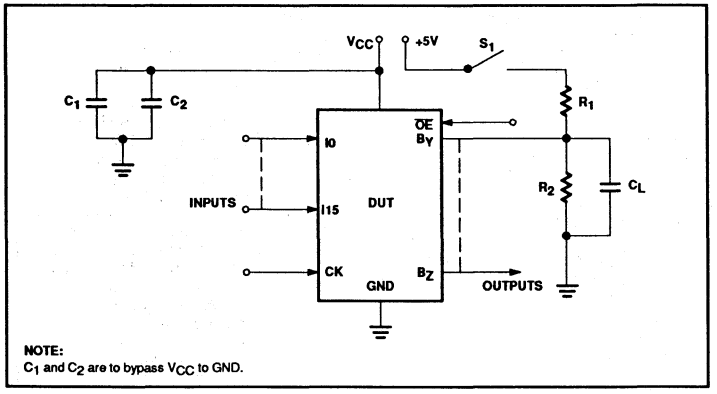
SYMBOL	PARAMETER
t_{ISPU}	Required delay between the beginning of Power Down LOW and the positive transition of the first valid clock.
t_{IS1}	Required delay between beginning of valid input and positive transition of Clock.
t_{IS2}	Required delay between beginning of valid input and positive transition of Clock, when using optional Complement Array (two passes necessary through the AND Array).
t_{NVCK1}	Required delay between the negative transition of the clock and the negative transition of the Asynchronous Initialization when using external INIT control (from pin 19) to guarantee that the clock edge is not detected as a valid negative transition.
t_{NVCK2}	Required delay between the negative transition of the clock and the negative transition of the Asynchronous Initialization, when using the internal INIT control (from P-terms INA and INB), to guarantee that the clock edge is not detected as a valid negative transition.
t_{OD1}	Delay between beginning of Output Enable High and when Outputs are in the OFF-State, when using external OE control (from pin 19).
t_{OD2}	Delay between beginning of Output Enable High and when outputs are in the OFF-State when using internal OE control (from P-terms OEA and OEB).
t_{OE1}	Delay between beginning of Output Enable Low and when Outputs become valid when using external OE control from pin 19.
t_{OE2}	Delay between beginning of Output Enable Low and when outputs become valid when using internal OE control (from P-terms OEA and OEB).
t_{PDZ}	Delay between beginning of Power Down HIGH and when outputs are in OFF–State and the circuit is "powered down".

SYMBOL	PARAMETER
t_{PPR}	Delay between V_{CC} (after power-on) and when Outputs become preset at "1".
$t_{PUA1,2}$	Delay between beginning of Power Down LOW and when outputs become Active (valid) and the circuit is "powered up". See AC Specifications.
t_{RH}	Required delay between positive transition of Clock and end of valid Input data when jamming data into State or Output Registers in diagnostic mode.
t_{RJH}	Required delay between positive transition of Clock and end of inputs I11 or I10 transition to State and Output Register Input Jam Diagnostic Modes, respectively.
t_{RJS}	Required delay between when inputs I11 or I10 transition to State and Output Register Input Jam Diagnostic Modes, respectively, and when the output pins become available as inputs.
t_{SRD}	Delay between input I12 transition to Logic mode and when the Outputs reflect the contents of the Output Register.
t_{SRE}	Delay between input I12 transition to Diagnostic Mode and when the Outputs reflect the contents of the State Register.
t_{VCK1}	Required delay between negative transition of Asynchronous Initialization and negative transition of Clock preceding the first valid clock pulse when using external INIT control (pin 19).
t_{VCK2}	Required delay between the negative transition of the Asynchronous Initialization and the negative transition of the clock preceding the first valid clock pulse when using internal INIT control (from P–terms INA and INB).
t_{VS}	Required delay between V_{CC} (after power-on) and negative transition of Clock preceding first reliable clock pulse.

CMOS programmable logic sequencer (17 × 68 × 8)

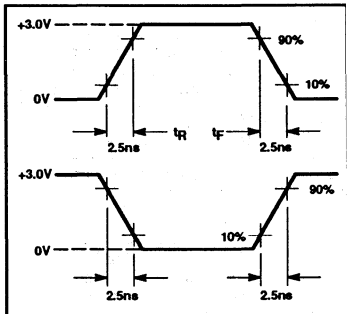
PLC415-16

TEST LOAD CIRCUIT



NOTE:
C_1 and C_2 are to bypass V_{CC} to GND.

VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

LOGIC PROGRAMMING

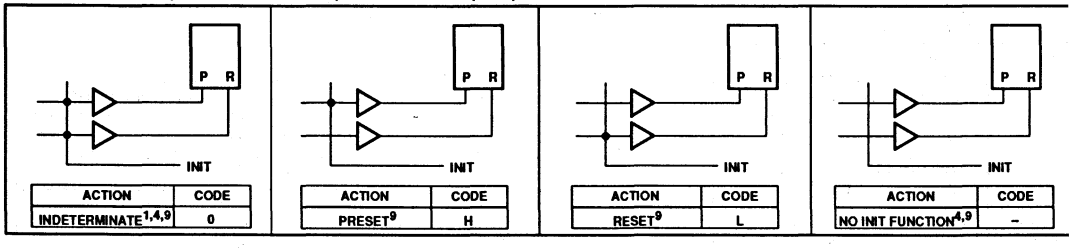
The PLC416-16 is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Signetics SLICE and SNAP design software packages. ABEL™ and CUPL™ design software packages also support the PLC416-16 architecture.

All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

PLC416-16 logic designs can also be generated using the program table entry format, which is detailed on the following pages. This program table entry format is supported by SNAP and SLICE only. The SLICE design package is available, free of charge, to qualified users.

To implement the desired logic functions, each logic variable (I, B, P, S, T, etc.) from the logic equations if assigned a symbol. TRUE, COMPLEMENT, PRESET, RESET, OUTPUT ENABLE, INACTIVE, etc., symbols are defined below.

INITIALIZATION (PRESET/RESET)[11] OPTION – (P/R)



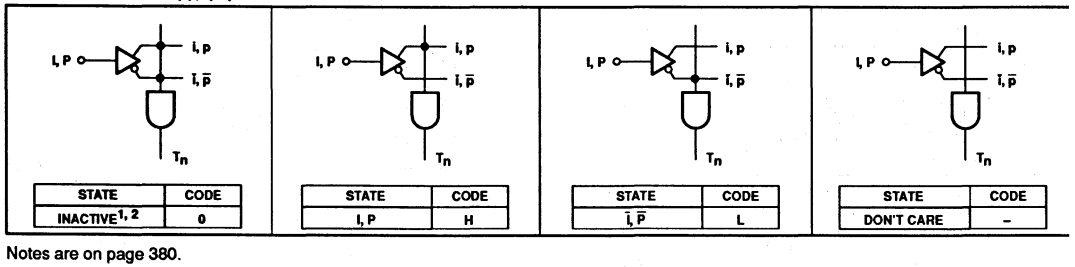
ACTION	CODE
INDETERMINATE[1,4,9]	0

ACTION	CODE
PRESET[9]	H

ACTION	CODE
RESET[9]	L

ACTION	CODE
NO INIT FUNCTION[4,9]	–

"AND" ARRAY – (I), (P)



STATE	CODE
INACTIVE[1,2]	0

STATE	CODE
I, P	H

STATE	CODE
$\bar{I}, \bar{P}$	L

STATE	CODE
DON'T CARE	–

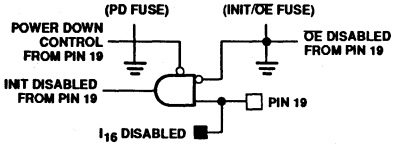
Notes are on page 380.

ABEL is a trademark of Data I/O Corp.
CUPL is a trademark of Logical Devices, Inc.

LOGIC PROGRAMMING (Continued)

PIN 19 FUNCTION: POWER DOWN, INIITALIZATION, $\overline{OE}$, OR INPUT

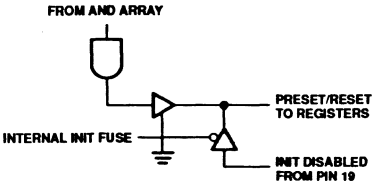
Power Down Mode



POWER DOWN FUSE	CODE
PIN 19 AS POWER DOWN	H^6

EXTERNAL INIT/$\overline{OE}$ FUSE	CODE
EXTERNAL INIT/$\overline{OE}$ DISABLED	L

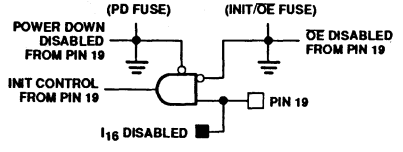
P-Term Initialization Control



INTERNAL INIT FUSES	CODE
P-TERM INIT CONTROL	$H^{7,8}$

POWER DOWN FUSE	CODE
POWER DOWN ENABLED OR DISABLED	H OR L

External Initialization Control

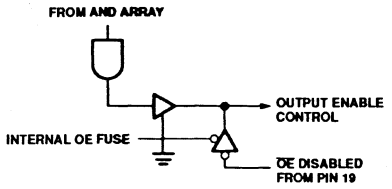


PD FUSE	CODE
POWER DOWN DISABLED	L^1

EXTERNAL INIT/$\overline{OE}$ FUSE	CODE
PIN 19 AS EXTERNAL INIT	L^1

INTERNAL INIT FUSES	CODE
P-TERM INIT ACTIVE OR INACTIVE	H OR $L^{7,8}$

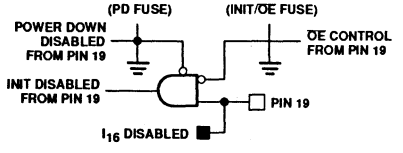
P-Term OE Control



INTERNAL OE FUSES	CODE
P-TERM OE CONTROL	$H^{7,8}$

POWER DOWN FUSE	CODE
POWER DOWN ENABLED OR DISABLED	H OR L

External Output Enable Control



PD FUSE	CODE
POWER DOWN DISABLED	L

EXTERNAL INIT/$\overline{OE}$ FUSE	CODE
PIN 19 AS EXTERNAL $\overline{OE}$	H

INTERNAL INIT FUSES	CODE
P-TERM $\overline{OE}$ ACTIVE OR INACTIVE	H OR $L^{7,8}$

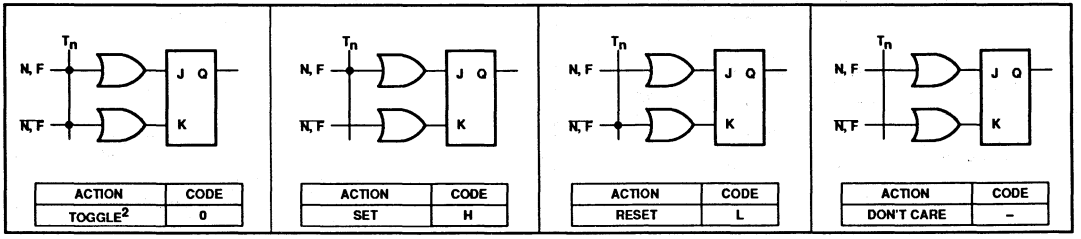
Notes are on page 380.

CMOS programmable logic sequencer (17 × 68 × 8)

PLC415-16

LOGIC PROGRAMMING (Continued)

"OR" ARRAY – J-K FUNCTION – (N), (F)



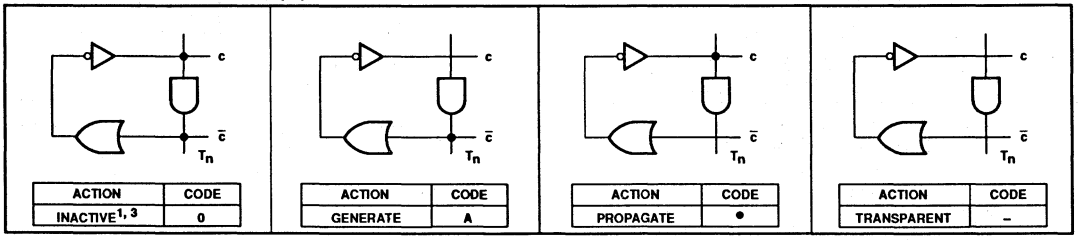
ACTION	CODE
TOGGLE[2]	0

ACTION	CODE
SET	H

ACTION	CODE
RESET	L

ACTION	CODE
DON'T CARE	–

"COMPLEMENT" ARRAY – (C)



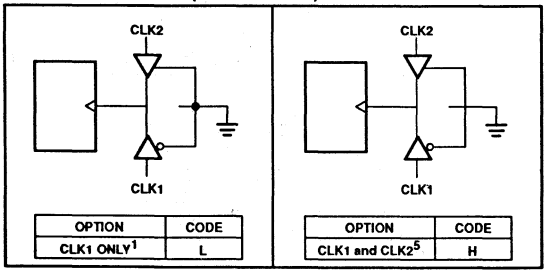
ACTION	CODE
INACTIVE[1, 3]	0

ACTION	CODE
GENERATE	A

ACTION	CODE
PROPAGATE	•

ACTION	CODE
TRANSPARENT	–

CLOCK OPTION – (CLK1/CLK2)



OPTION	CODE
CLK1 ONLY[1]	L

OPTION	CODE
CLK1 and CLK2[5]	H

NOTES:

1 This is the initial unprogrammed state of all links.
2 Any gate T_n will be unconditionally inhibited if any one of its I or P link pairs is left intact.
3 To prevent oscillations, this state is not allowed for C link pairs coupled to active gates T_n.
4 These states are not allowed when using PRESET/RESET option.
5 Input buffer I_5 must be deleted from the AND array (i.e., all fuse locations "Don't Care") when using second clock option.
6 When using Power Down feature, INPUT 16 is automatically disabled via the design software.
7 If the internal (P-term) control fuse for INIT and/or OE is programmed as Active High, the associated External Control function will be permanently disabled, regardless of the state of the External INIT/OE fuse.
8 One internal control fuse exists for each group of 8 registers. P0 – 3 and F0 – 3 are banked together in one group, as are P4 – 7 and F4 – 7. Control can be split between the INIT/OE pin (Pin 19) and P–terms INA, INB, OEA and OEB.
9 The PLC416-16 also has a power-up preset feature. This feature insures that the device will power-up in a known state with all register elements (State and Output Register) at a logic High (H). When programming the device it is important to realize this is the initial state of the device. You *must* provide a next state jump if you do not wish to use all Highs (H) as the present state.
10 L = cell unprogrammed.
H = cell programmed.
11 Inputs 10, 11 and 12 (pins 25, 24, & 23) can be used for supervoltage diagnostic mode tests. It is recommended that these inputs not be connected to product terms INA, INB, OEA or OEB if you intend to make use of the diagnostic modes due to the fact that the patterns associated with the internal INIT and OE control product terms may interfere with the diagnostic mode data loading and reading.

CMOS programmable logic sequencer (17 × 68 × 8)

PLC415-16

PROGRAM TABLE

AND

(Im, Ps)	
INACTIVE	O
I, P	H
$\bar{I}$, $\bar{P}$	L
DON'T CARE	–

(Cn)	
INACTIVE	O
GENERATE	A
PROPAGATE	•
TRANSPARENT	–

OR (Ns, Fn)

TOGGLE	O
SET	H
RESET	L
NO CHANGE	–

OPTIONS

ENTERNAL INIT	L
EXTERNAL OE	H
INTERNAL INIT/OE ENABLED	H
INTERNAL INIT/OE DISABLED	L
POWER DOWN ENABLED	H
POWER DOWN DISABLED	L
CLOCK 1 ONLY	L
CLOCK 1 AND 2	H

INITIALIZATION	
PRESET	H
RESET	L
NO INIT	–
INDETERMINATE	O

PROJECT NAME _____ DATE _____ REVISION _____

CUSTOMER NAME _____ SIGNETICS PART # _____ CUSTOMER PART # _____

TERMS	COMP. ARRAY	INTERNAL INIT INB	INTERNAL INIT INA	INTERNAL OE OEB	INTERNAL OE OEA	EXTERNAL INIT/OE	CLK 1/1&2	PD	INITIALIZATION
	NOR	AND							OR
	Cn	INPUT (Im)					PRESENT STATE (Ps)		NEXT STATE (Ns) / OUTPUT (Fn)
	C1 C0	I16 I15 I14 I13 I12 I11 I10 I9 I8 I7 I6 I5 I4 I3 I2 I1 I0					P7 P6 P5 P4 P3 P2 P1 P0		N7 N6 N5 N4 N3 N2 N1 N0 / F7 F6 F5 F4 F3 F2 F1 F0
0									
1									
2									
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63									
INB									
OEB									
INA									
OEA									
PIN NO.		19 20 21 22 23 24 25 26 27 2 3 4 5 6 7 8 9							10 11 12 13 15 16 17 18
PIN LABELS									

NOTES:

1. In the unprogrammed state all cells are conducting. Thus, the program table for an unprogrammed device would contain "0"s for all product terms (inactive) and initialization states (indeterminate). The default or unprogrammed state of all other options is "L".
2. Unused Cn, Im and Ps cells are normally programmed as Don't Care (–).
3. Unused product terms can be left blank (inactive) for future code modification.

ERASURE CHARACTERISTICS (For Quartz Window Packages Only)

The erasure characteristics of the PLC415 Series devices are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps has wavelengths in the 3000 – 4000Å range. Data shows that constant exposure to room level fluorescent lighting could erase a typical PLC415 in approximately three years, while it would take approximately one week to cause erasure when exposed to direct sunlight. If the PLC415 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

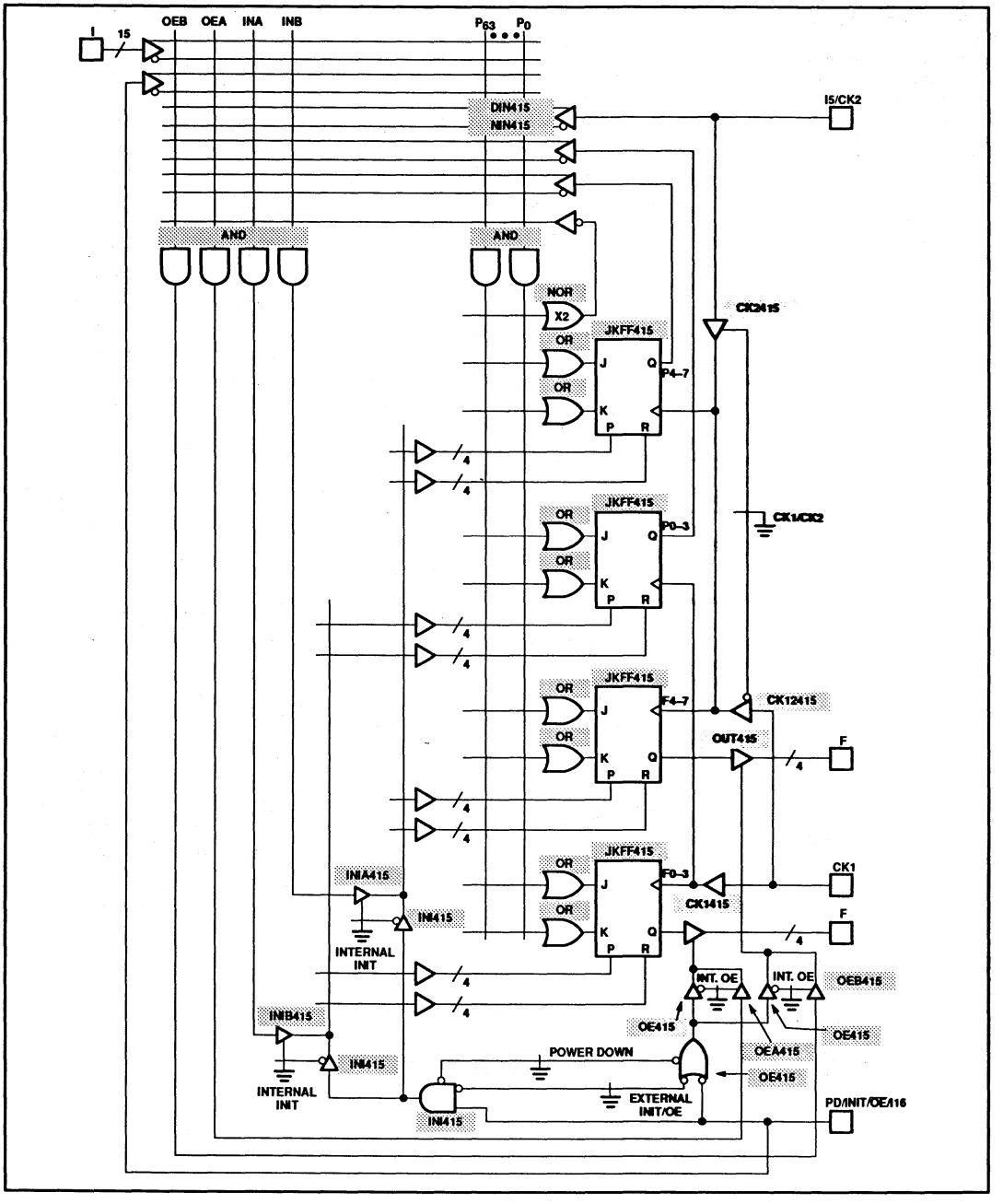
The recommended erasure procedure for the PLC415 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15Wsec/cm^2. The erasure time with this dosage is approximately 30 to 35 minutes using an ultraviolet lamp with a 12,000µW/cm^2 power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose a CMOS EPLD can be exposed to without damage is 7258Wsec/cm^2 (1 week @ 12000µW/cm^2). Exposure of these CMOS EPLDs to high intensity UV light for longer periods may cause permanent damage.

The maximum number of guaranteed erase/write cycles is 50. Data retention exceeds 20 years.

CMOS programmable logic sequencer (17 × 68 × 8)

PLC415-16

SNAP RESOURCE SUMMARY DESIGNATIONS



Programmable logic sequencers (16 × 48 × 8)

PLS105/A

DESCRIPTION

The PLS105and the PLS105A are bipolar Programmable Logic State machines of the Mealy type. They contain logic AND-OR gate arrays with user programmable connections which control the inputs of on-chip State and Output Registers. These consist respectively of 6 Q_P, and 8 Q_F edge-triggered, clocked S/R flip-flops, with an Asynchronous Preset option. all flip-flops are unconditionally preset to "1" during power turn on.

The AND array combines 16 external inputs $I_0 - I_{15}$ with six internal inputs P_{0-5}, which are fed back from the State Registers to form up to 48 transition terms (AND terms). All transition terms can include True, False, or Don't Care states of the controlling variables, and are merged in the OR array to issue next-state and next-output commands to their respective registers on the Low-to-High transition of the Clock pulse. Both True and Complement transition terms can be generated by optional use of the internal input variable (C) from the Complement Array. Also, if desired, the Preset input can be converted to $\overline{\text{Output Enable}}$ function, as an additional user-programmable option.

Order codes are listed below in the Ordering Information Table.

FEATURES

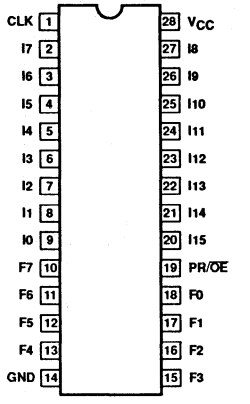
- PLS105
  - f_{MAX} = 13.9MHz
  - 20MHz clock rate
- PLS105A
  - f_{MAX} = 20MHz
  - 25MHz clock rate
- Field-Programmable (Ni-Cr link)
- 16 input variables
- 8 output functions
- 48 transition terms
- 6-bit State Register
- 8-bit Output Register
- Transition complement array
- Positive edge-triggered clocked flip-flops
- Programmable Asynchronous Preset or Output Enable
- Power-on preset to all "1" of internal registers
- Power dissipation: 600mW (typ.)
- TTL compatible
- Single +5V supply
- 3-State outputs

APPLICATIONS

- Interface protocols
- Sequence detectors
- Peripheral controllers
- Timing generators
- Sequential circuits
- Elevator controllers
- Security locking systems
- Counters
- Shift registers

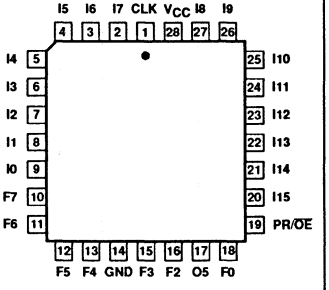
PIN CONFIGURATIONS

N Package



N = Plastic DIP (600mil-wide)

A Package



A = Plastic Leaded Chip Carrier

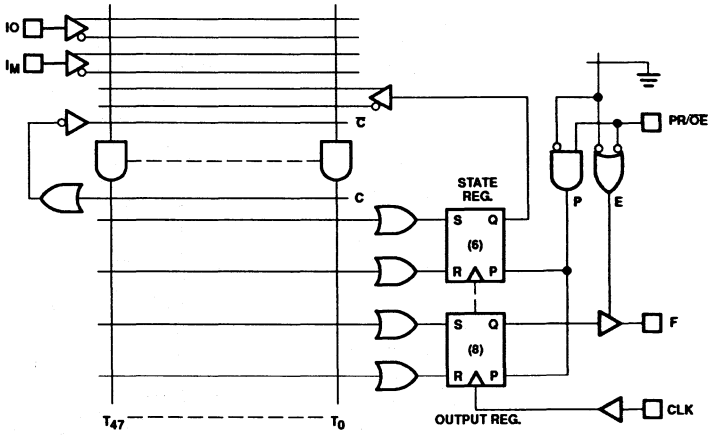
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
28-Pin Plastic DIP (600mil-wide)	PLS105N, PLS105AN
28-Pin Plastic Leaded Chip Carrier	PLS105A, PLS105AA

Programmable logic sequencers (16 × 48 × 8)

PLS105/A

FUNCTIONAL DIAGRAM



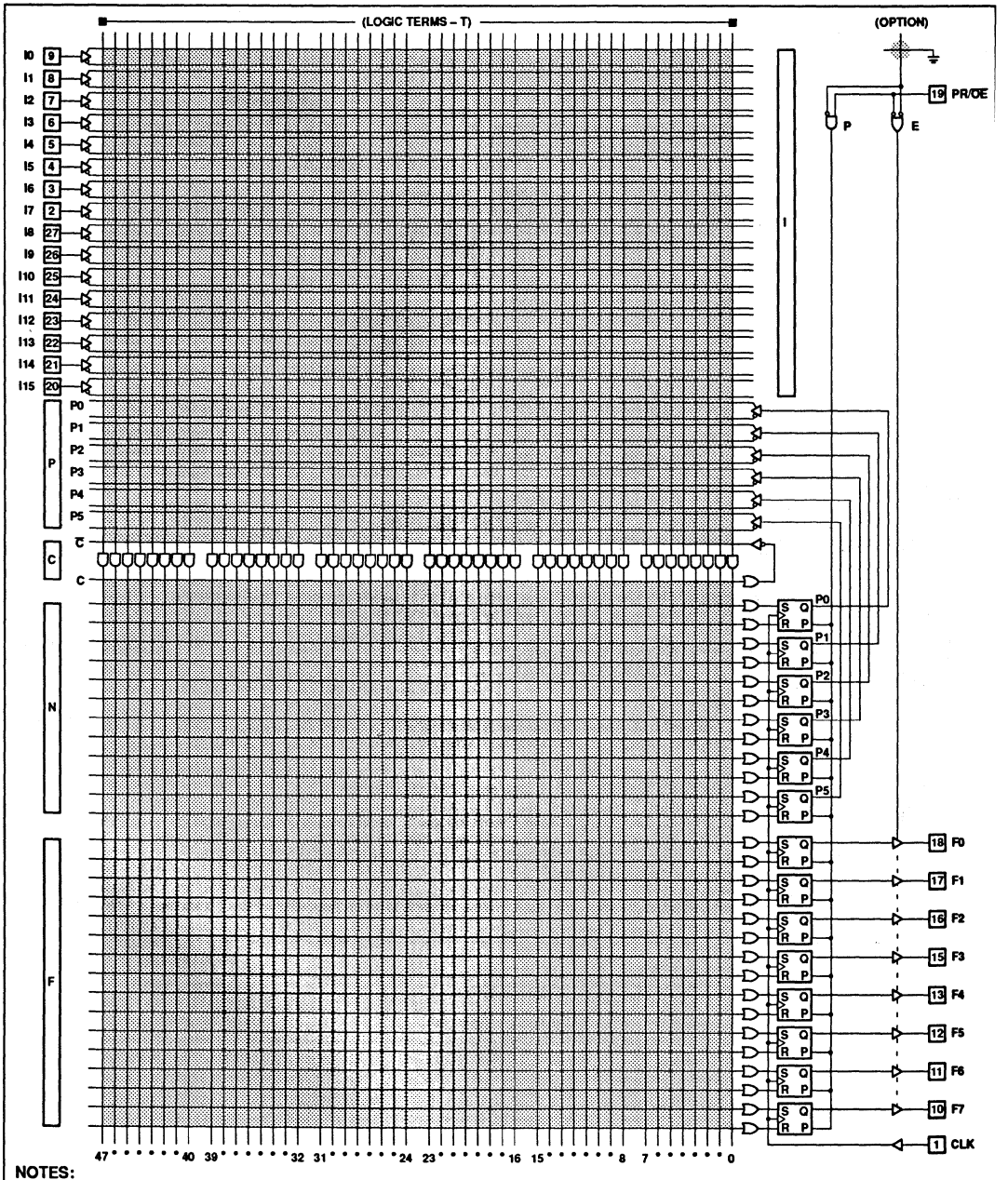
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION	POLARITY
1	CLK	**Clock:** The Clock input to the State and Output Registers. A Low-to-High transition on this line is necessary to update the contents of both registers.	Active-High
2 – 8 20 – 27	I1 – I15	**Logic Inputs:** The 15 external inputs to the AND array used to program jump conditions between machine states, as determined by a given logic sequence.	Active-High/Low
9	I0	**Logic/Diagnostic Input:** A 16th external logic input to the AND array, as above, when exercised with standard TTL levels. When I0 is held at +10V, device outputs F0 – 5 reflect the contents of State Register bits P0 – 5. The contents each Output Register remains unaltered.	Active-High/Low
10 – 13 15 – 18	F0 – 7	**Logic/Diagnostic Outputs:** Eight device outputs which normally reflect the contents of Output Register bits Q0 – 7, when enabled. When I0 is held at +10V, F0 – 5 = (P0 – 5), and F6, 7 = Logic "1".	Active-High
19	PR/$\overline{OE}$	**Preset or $\overline{\text{Output Enable}}$ Input:** A user programmable function:	
		• **Preset:** Provides an Asynchronous Preset to logic "1" of all State and Output Register bits. Preset overrides Clock, and when held High, clocking is inhibited and F0 – 7 are High. Normal clocking resumes with the first full clock pulse following a High-to-Low clock transition, after Preset goes Low.	Active-High (H)
		• **$\overline{\text{Output Enable}}$:** Provides an Output Enable function to all output buffers F0 – 7 from the Output Register.	Active-Low (L)

Programmable logic sequencers (16 × 48 × 8)

PLS105/A

LOGIC DIAGRAM



NOTES:
1. All AND gate inputs with a blown link float to a logic "1".
2. All OR gate inputs with a blown fuse float to logic "0".
3. ▒ Programmable connection.

Programmable logic sequencers (16 × 48 × 8)

PLS105/A

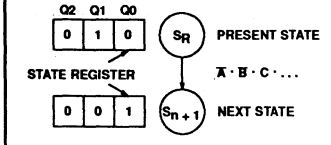
TRUTH TABLE [1, 2, 3, 4, 5, 6]

V_{CC}	OPTION PR	OPTION $\overline{OE}$	I_0	CK	S	R	$Q_{P/F}$	F
+5V	H		*	X	X	X	H	H
	L		+10V	X	X	X	Q_n	$(Q_P)_n$
	L		X	X	X	X	Q_n	$(Q_F)_n$
		H	*	X	X	X	Q_n	Hi–Z
		L	+10V	X	X	X	Q_n	$(Q_P)_n$
		L	X	X	X	X	Q_n	$(Q_F)_n$
		L	X	↑	L	L	Q_n	$(Q_F)_n$
		L	X	↑	L	H	L	L
		L	X	↑	H	L	H	H
		L	X	↑	H	H	IND.	IND.
↑	X	X	X	X	X	X	H	

NOTES:
1. Positive Logic:
   $S/R = T_0 + T_1 + T_2 + \ldots + T_{47}$
   $T_n = C(I0\ I1\ I2 \ldots)\ (P0\ P1 \ldots P5)$
2. Either Preset (Active–High) or $\overline{\text{Output Enable}}$ (Active–Low) are available, but not both. The desired function is a user-programmable option.
3. ↑ denotes transition from Low-to-High level.
4. R = S = High is an illegal input condition.
5. * = H or L or +10V.
6. X = Don't Care (≤5.5V).

LOGIC FUNCTION

Typical State Transition:



SET Q_0: $S_0 = (\overline{Q}_2 \cdot Q_1 \cdot \overline{Q}_0) \cdot \overline{A} \cdot \overline{B} \cdot C \ldots$
$R_0 = 0$

RESET Q_1: $S_1 = 0$
$R_1 = (\overline{Q}_2 \cdot Q_1 \cdot \overline{Q}_0) \cdot \overline{A} \cdot \overline{B} \cdot C \ldots$

HOLD Q_2: $S_2 = 0$
$R_2 = 0$

VIRGIN STATE

The factory shipped virgin device contains all fusible links intact, such that:

1. PR/$\overline{OE}$ option is set to PR. Thus, all outputs will be at "1", as preset by initial power-up procedure.
2. All transition terms are disabled (0).
3. All S/R flip-flop inputs are disabled (0).
4. The device can be clocked via a Test Array pre-programmed with a standard test pattern.
   NOTE: The Test Array pattern MUST be deleted before incorporating a user program. This is accomplished automatically by any Signetics qualified programming equipment.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS MIN	RATINGS MAX	UNIT
V_{CC}	Supply voltage		+7	V_{DC}
V_{IN}	Input voltage		+5.5	V_{DC}
V_{OUT}	Output voltage		+5.5	V_{DC}
I_{IN}	Input currents	–30	+30	mA
I_{OUT}	Output currents		+100	mA
T_{amb}	Operating temperature range	0	+75	°C
T_{stg}	Storage temperature range	–65	+150	°C

NOTES:
1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

DC ELECTRICAL CHARACTERISTICS

$0°C \le T_{amb} \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS MIN	LIMITS TYP[1]	LIMITS MAX	UNIT
Input voltage[2]						
V_{IH}	High	V_{CC} = MAX	2.0			V
V_{IL}	Low	V_{CC} = MIN			0.8	V
V_{IC}	Clamp[3]	V_{CC} = MIN, I_{IN} = –12mA		–0.8	–1.2	V
Output voltage[2]						
		V_{CC} = MIN				
V_{OH}	High[4]	I_{OH} = –2mA	2.4			V
V_{OL}	Low[5]	I_{OL} = 9.6mA		0.35	0.45	V
Input current						
I_{IH}	High	V_{IN} = 5.5V		<1	25	µA
I_{IL}	Low	V_{IN} = 0.45V		–10	–100	µA
I_{IL}	Low (CK input)	V_{IN} = 0.45V		–50	–250	µA
Output current						
		V_{CC} = MAX				
$I_{O(OFF)}$	Hi-Z state[6]	V_{OUT} = 5.5V		1	40	µA
		V_{OUT} = 0.45V		–1	–40	µA
I_{OS}	Short circuit [3, 7]	V_{OUT} = 0V	–15		–70	mA
I_{CC}	V_{CC} supply current[8]	V_{CC} = MAX		120	180	mA
Capacitance[6]						
		V_{CC} = 5.0V				
C_{IN}	Input	V_{IN} = 2.0V		8		pF
C_{OUT}	Output	V_{OUT} = 2.0V		10		pF

NOTES:
1. All typical values are at V_{CC} = 5V, T_{amb} = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Test one at a time.
4. Measured with V_{IL} applied to $\overline{OE}$ and a logic high stored, or with V_{IH} applied to PR.
5. Measured with a programmed logic condition for which the output is at a low logic level, and V_{IL} applied to PR/$\overline{OE}$ Output sink current is supplied through a resistor to V_{CC}.
6. Measured with V_{IH} applied to PR/$\overline{OE}$.
7. Duration of short circuit should not exceed 1 second.
8. I_{CC} is measured with the PR/$\overline{OE}$ input grounded, all other inputs at 4.5V and the outputs open.

Programmable logic sequencers (16 × 48 × 8)

PLS105/A

AC ELECTRICAL CHARACTERISTICS

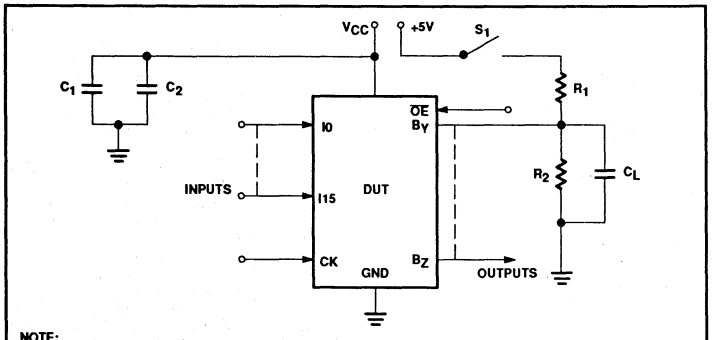
$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0°C \le T_{amb} \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

SYMBOL	PARAMETER	FROM	TO	LIMITS						UNIT
				PLS105			PLS105A			
				MIN	TYP[1]	MAX	MIN	TYP[1]	MAX	
Pulse width										
t_{CKH}	Clock[2] High	CK +	CK –	25	15		20	15		ns
t_{CKL}	Clock Low	CK –	CK +	25	15		20	15		ns
t_{CKP}	Clock period	CK +	CK +	50	30		40	30		ns
t_{PRH}	Preset pulse	PR +	PR –	25	15		25	15		ns
Setup time[3]										
$t_{IS1}A$	Input	Input ±	CK +	60			40			ns
$t_{IS1}B$	Input	Input ±	CK +	50			30			ns
$t_{IS1}C$	Input	Input ±	CK +	42			N/A			ns
$t_{IS2}A$	Input (through Complement Array)	Input ±	CK +	90			70			ns
$t_{IS2}B$	Input (through Complement Array)	Input	CK +	80			60			ns
$t_{IS2}C$	Input (through Complement Array)	Input	CK +	72			N/A			ns
t_{VS}	Power-on preset	V_{CC} +	CK –	0	–10		0	–10		ns
t_{PRS}	Preset	PR –	CK –	0	–10		0	–10		ns
Hold time										
t_{IH}	Input	CK +	Input ±	5	–10		5	–10		ns
Propagation delay										
t_{CKO}	Clock	CK +	Output ±		15	30		15	20	ns
t_{OE}	Output enable[4]	OE –	Output –		20	30		20	30	ns
t_{OD}	Output disable[4]	OE +	Output +		20	30		20	30	ns
t_{PR}	Preset	PR +	Output +		18	30		18	30	ns
t_{PPR}	Power-on preset	V_{CC} +	Output +		0	10		0	10	ns
Frequency of operation[3]										
$f_{MAX}C$	Without Complement Array			13.9			20.0			MHz
$f_{MAX}C$	With Complement Array			9.8			12.5			MHz

NOTES:

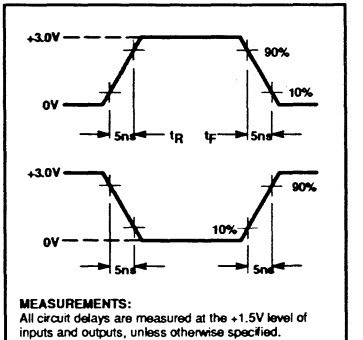
1. All typical values are at $V_{CC} = 5V$, $T_{amb} = +25°C$.
2. To prevent spurious clocking, clock rise time (10% – 90%) ≤ 30ns.
3. See "Speed vs. OR Loading" diagrams.
4. For 3-State output; output enable times are tested with $C_L = 30pF$ to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with $C_L = 5pF$. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} - 0.5V)$ with S_1 open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with S_1 closed.

TEST LOAD CIRCUIT



NOTE:
C_1 and C_2 are to bypass V_{CC} to GND.

VOLTAGE WAVEFORMS



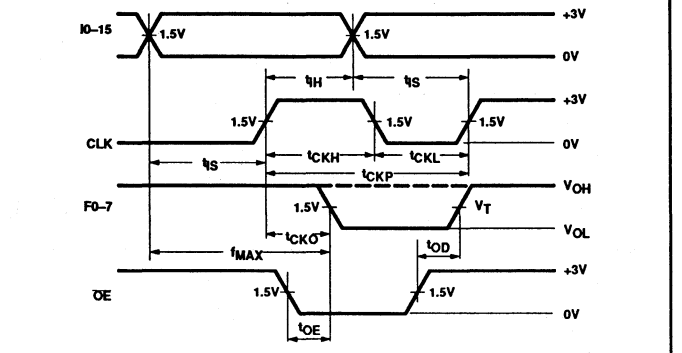
MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

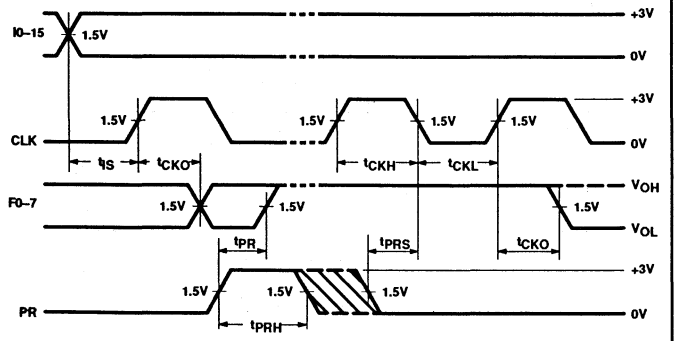
Programmable logic sequencers (16 × 48 × 8)

PLS105/A

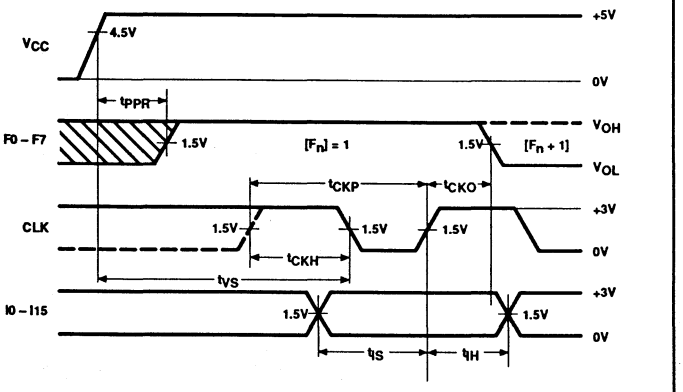
TIMING DIAGRAMS



Sequential Mode



Asynchronous Preset

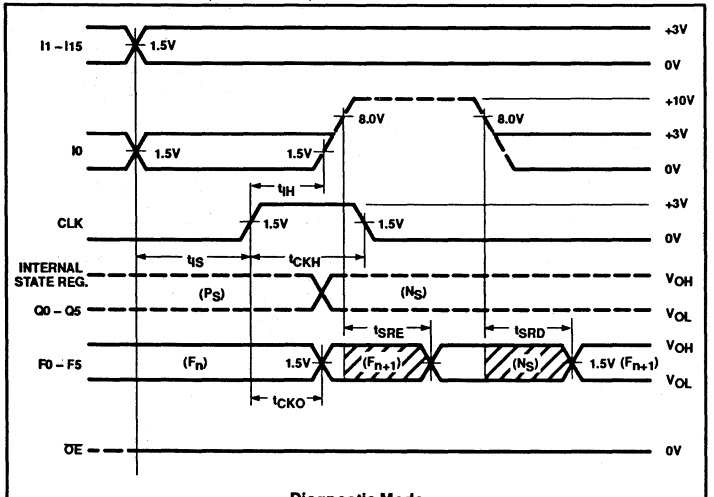


Power-On Preset

TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{CKH}	Width of input clock pulse.
t_{CKL}	Interval between clock pulses.
t_{CKP}	Minimum guaranteed Clock period.
t_{IS1}	Required delay between beginning of valid input and positive transition of clock.
t_{IS2}	Required delay between beginning of valid input and positive transition of Clock, when using optional Complement Array (two passes necessary through the AND array).
t_{VS}	Required delay between V_{CC} (after power-on) and negative transition of Clock preceding first reliable clock pulse.
t_{PRS}	Required delay between negative transition of Asynchronous Preset and negative transition of Clock preceding first reliable clock pulse.
t_{IH}	Required delay between positive transition of Clock and end of valid input data.
t_{CKO}	Delay between positive transition of clock and when outputs become valid (with PR/$\overline{OE}$ Low).
t_{OE}	Delay between beginning of Output Enable Low and when outputs become valid.
t_{OD}	Delay between beginning of Output Enable High and when outputs are in the OFF-State.
t_{SRE}	Delay between input I_0 transition to Diagnostic mode and when the outputs reflect the contents of the State Register.
t_{SRD}	Delay between input I_0 transition to Logic mode and when the outputs reflect the contents of the Output Register.
t_{PR}	Delay between positive transition of Preset and when outputs become valid at "1".
t_{PPR}	Delay between V_{CC} (after power-on) and when outputs become preset at "1".
t_{PRH}	Width of preset input pulse.
f_{MAX}	Minimum guaranteed operating frequency.

TIMING DIAGRAMS (Continued)



Diagnostic Mode

SPEED VS. "OR" LOADING

The maximum frequency at which the PLS can be clocked while operating in *sequential mode* is given by:

$$(1/f_{MAX}) = t_{CY} = t_{IS} + t_{CKO}$$

This frequency depends on the number of transition terms T_n used. Having all 48 terms connected in the AND array does not appreciably impact performance; but the number of terms connected to each OR line affects t_{IS}, due to capacitive loading. The effect of this loading can be seen in Figure 1, showing the variation of t_{IS1} with the number of terms connected per OR.

The PLS105 AC electrical characteristics contain three limits for the parameters t_{IS1} and t_{IS2} (refer to Figure 1). The first, t_{IS1A} is guaranteed for a device with 48 terms connected to any OR line. t_{IS1B} is guaranteed for a device with 32 terms connected to any OR line. And t_{IS1C} is guranteed for a device with 24 terms conntected to any OR line.

The three other entries in the AC table, t_{IS2} A, B, and C are corresponding 48, 32, and 24 term limits when using the on–chip Complement Array.

The PLS105A AC electrical characteristics contain two limits for the parameters t_{IS1} and t_{IS2} (refer to Figure 2). The first, t_{IS1A} is guaranteed for a device with 24 terms connected to any OR line. t_{IS1B} is guaranteed for a device with 16 terms connected to any OR line.

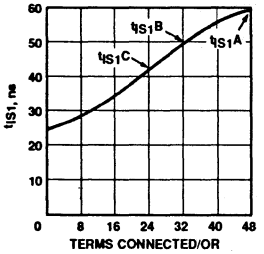


Figure 1. PLS105 t_{IS1} vs. Terms/OR Connected

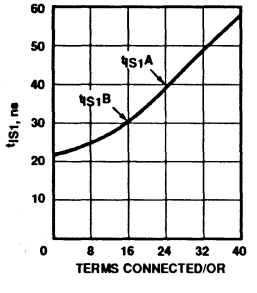


Figure 2. PLS105A t_{IS1} vs. Terms/OR Connected

The two other entries in the AC table, t_{IS2} A and B are corresponding 24 and 16 term limits when using the on-chip Complement Array.

The worst case of t_{IS} for a given application can be determined by identifying the OR line with the maximum number of T_n connections. This can be done by referring to the interconnect pattern in the PLS logic diagram, typically illustrated in Figure 3, or by counting the maximum number of "H" *or* "L" entries in one of the columns of the device Program Table.

This number plotted on the curve in Figure 1 or 2 will yield the worst case t_{IS} and, by implication, the maximum clocking frequency for reliable operation.

Note that for maximum speed all UNUSED transition terms should be disconnected from the OR array.

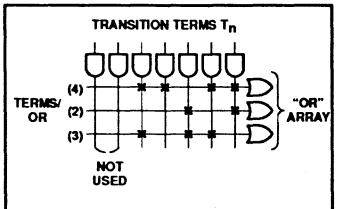


Figure 3. Typical OR Array Interconnect Pattern

Programmable logic sequencers (16 × 48 × 8)

PLS105/A

LOGIC PROGRAMMING

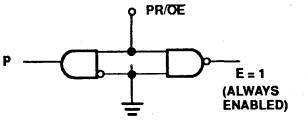
The PLS105/A devices are fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Signetics' SNAP and SLICE, Data I/O Corporation's ABEL and Logical Devices Inc.'s CUPL design software packages.

All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

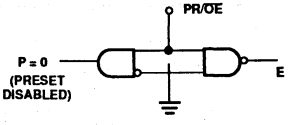
PLS105/A logic designs can also be generated using the program table entry format detailed on the following pages. This program table entry format is supported by the Signetics SNAP and SLICE PLD design software packages (PTP module). SLICE is available free of charge to qualified users.

To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

PRESET/$\overline{OE}$ OPTION – (P/E)



OPTION	CODE
PRESET[1]	H

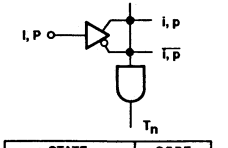


OPTION	CODE
$\overline{OE}$	L

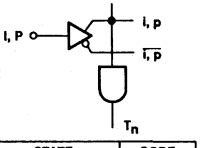
PROGRAMMING:

The PLS105/A has a power-up preset feature. This feature insures that the device will power-up in a known state with all register elements (State and Output Register) at logic High (H). When programming the device it is important to realize this is the initial state of the device. You *must* provide a next state jump if you do not wish to use all Highs (H) as the present state.

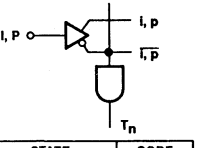
"AND" ARRAY – (I), (P)



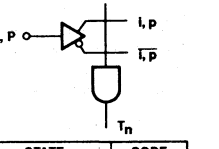
STATE	CODE
INACTIVE[1, 2]	O



STATE	CODE
I, P	H

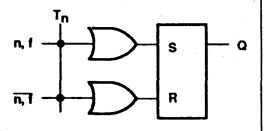


STATE	CODE
$\overline{I, P}$	L

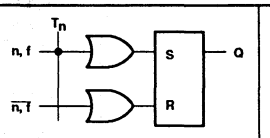


STATE	CODE
DON'T CARE	–

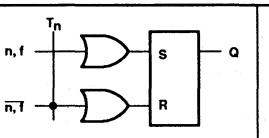
"OR" ARRAY – (N), (F)



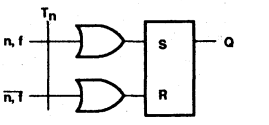
ACTION	CODE
INACTIVE[1, 3]	O



ACTION	CODE
SET	H

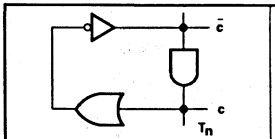


ACTION	CODE
RESET	L

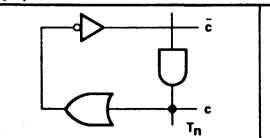


ACTION	CODE
NO CHANGE	–

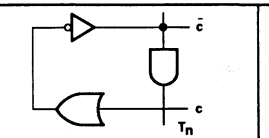
"COMPLEMENT" ARRAY – (C)



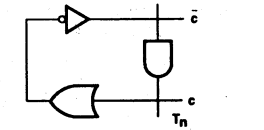
ACTION	CODE
INACTIVE[1, 4]	O



ACTION	CODE
GENERATE	A



ACTION	CODE
PROPAGATE	•



ACTION	CODE
TRANSPARENT	–

NOTES:

1. This is the initial unprogrammed state of all links.
2. Any gate T_n will be unconditionally inhibited if both the true and complement of any input (I or P) are left intact.
3. To prevent simultaneous Set and Reset flip-flop commands, this state is not allowed for N and F link pairs coupled to active gates T_n (see flip-flop truth tables).
4. To prevent oscillations, this state is not allowed for C link pairs coupled to active gates T_n.

Programmable logic sequencers (16 × 48 × 8)

PLS105/A

PROGRAM TABLE

PROGRAM TABLE ENTRIES

AND			OR	
INACTIVE	0	C_n	INACTIVE 0	Ns, Fr
GENERATE	A		SET H	
PROPAGATE	•		RESET L	
TRANSPARENT	—		NO CHANGE —	
INACTIVE	0	I_m, P_s	OPTION	
I, P	H		PRESET H	P/E
$\overline{I}$, $\overline{P}$	L		$\overline{OE}$ L	
DON'T CARE	—			

CUSTOMER NAME _____

PURCHASE ORDER # _____

SIGNETICS DEVICE # CF (XXXX)

CUSTOMER SYMBOLIZED PART # _____

TOTAL NUMBER OF PARTS _____

PROGRAM TABLE _____

REV _____

DATE _____

	AND																		OPTION (P/E) OR																	
TERM	C_n	INPUT (I_m)																PRESENT STATE (P_s)						REMARKS	NEXT STATE (Ns)						OUTPUT (Fr)							
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	5	4	3	2	1	0		5	4	3	2	1	0	7	6	5	4	3	2	1	0
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PIN NO.		20	21	22	23	24	25	26	27	2	3	4	5	6	7	8	9														10	11	12	13	15	16	17	18
VARIABLE NAME																																					

NOTES:

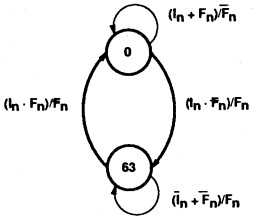
1. The FPLS is shipped with all links initially intact. Thus, a background of "0" for all Terms, and an "H" for the P/E option, exists in the table, shown BLANK instead for clarity.
2. Unused C_n, I_m, and P_s bits are normally programmed Don't Care (–).
3. Unused Transition Terms can be left blank for future code modification, or programmed as (–) for maximum speed.
4. Letters in variable fields are used as identifiers by logic type programmers.

TEST ARRAY

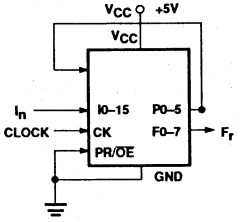
The PLS105/A may be subjected to AC and DC parametric tests prior to programming via an on-chip test array.

The array consists of test transition terms 48 and 49, factory programmed as shown below.

Testing is accomplished by clocking the PLS105/A and applying the proper input sequence to I0 – I15 as shown in the test circuit timing diagram.



State Diagram

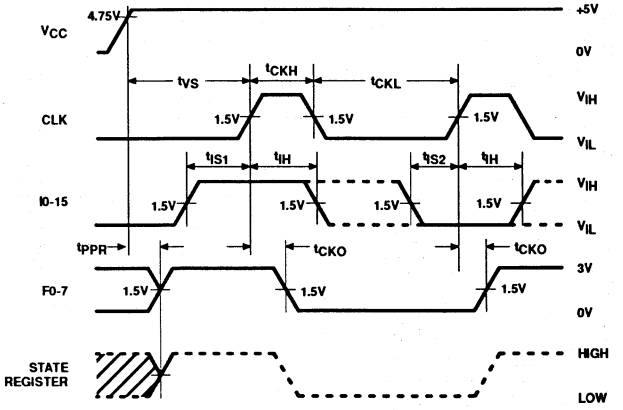


PLS Under Test

TERM	C	AND: INPUT (Im) I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0	PRESENT STATE (Ps) P5	P4	P3	P2	P1	P0	OPTION (P/E): H — OR: NEXT STATE (Ns) N5	N4	N3	N2	N1	N0	OUTPUT (Fr) F7	F6	F5	F4	F3	F2	F1	F0
48	A	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L
49	•	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H

Test Array Program

Both terms 48 and 49 must be deleted during user programming to avoid interfering with the desired logic function. This is accomplished automatically by any Signetics' qualified programming equipment.



Test Circuit Timing Diagram

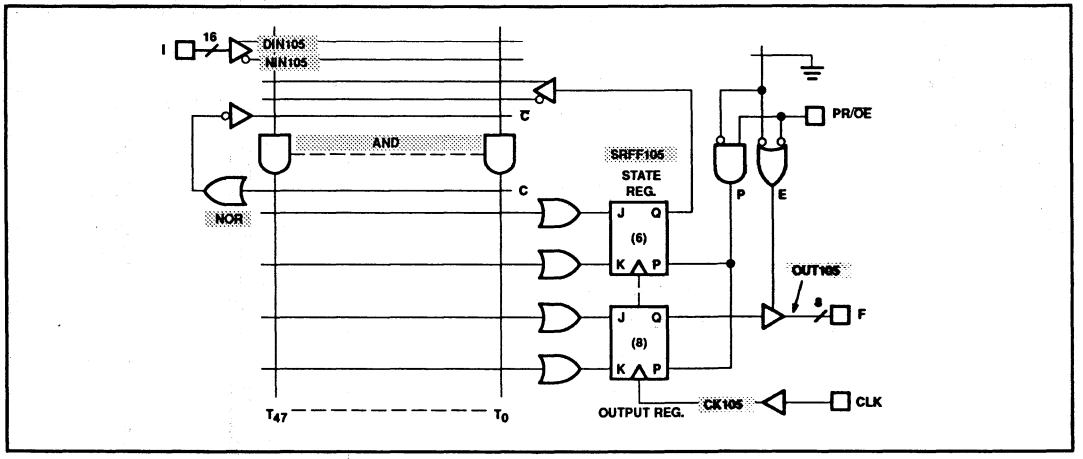
TERM	C	AND: INPUT (Im) I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0	PRESENT STATE (Ps) P5	P4	P3	P2	P1	P0	OPTION (P/E): H — OR: NEXT STATE (Ns) N5	N4	N3	N2	N1	N0	OUTPUT (Fr) F7	F6	F5	F4	F3	F2	F1	F0
48	–	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	–	–	–	–	–	–	–	–	–	–	–	–	–	–
49	•	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	–	–	–	–	–	–	–	–	–	–	–	–	–	–

Test Array Deleted

Programmable logic sequencers (16 × 48 × 8)

PLS105/A

SNAP RESOURCE SUMMARY DESIGNATIONS



Programmable logic sequencer (16 × 48 × 8)

PLUS105-45

DESCRIPTION

The PLUS105-45 is a bipolar programmable state machine of the Mealy type. Both the AND and the OR array are user-programmable. All 48 AND gates are connected to the 16 external dedicated inputs (I0-I15) and to the feedback paths of the 6 buried State Registers (Q_{P0}-Q_{P5}). Because the OR array is programmable, any one or all of the 48 transition terms can be connected to any or all of the State and Output Registers.

All state transition terms can include True, False and Don't Care states of the controlling state variables. A Complement Transition Array supports complex IF-THEN-ELSE state transitions with a single product term.

The PLUS105-45 device features edge-triggered, J-K flip-flops, which provide the added flexibility of the toggle function which is indeterminate on S-R flip-flops. Because the J-K function is a superset of the S-R flip-flop function, the PLUS105-45 is backward compatible with all 105-type devices that have S-R flip-flops. Asynchronous Preset/Output Enable functions are available.

The PLUS105-45 is pin-for-pin and software compatible with the Signetics PLS105 and PLS105A Logic Sequencers, as well as other commercially available 105-type programmable logic devices.

To facilitate testing of state machine designs, diagnostic mode features for register preset and buried state register observability have been incorporated into the PLUS105-45 device architecture.

Ordering codes are listed in the Ordering Information Table.

FEATURES

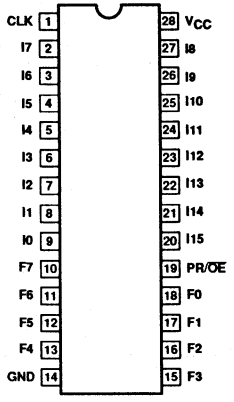
- 45MHz operating frequency
  - 55.6MHz clock rate
  - No OR term loading restrictions
- Available in 300mil skinny DIP, 600mil-wide Plastic DIP and PLCC packages
- Pin and software compatible with other commerically available 105 logic sequencers
- 16 input variables
- 8 output functions
- 48 transition terms
- 6-bit State Register
- 8-bit Output Register
- Transition complement array
- Positive edge-triggered clocked J-K (or S-R) flip-flops
- Security fuse
- Programmable Asynchronous Preset or Output Enable
- Power-on preset (to all "1"s) of internal registers
- Power dissipation: 800mW (typ.)
- TTL compatible
- Single +5V supply
- 3-State outputs

APPLICATIONS

- Interface protocols
- Sequence detectors
- Peripheral controllers
- Timing generators
- Sequential circuits
- Elevator controllers
- Security Locking systems
- Counters
- Shift registers

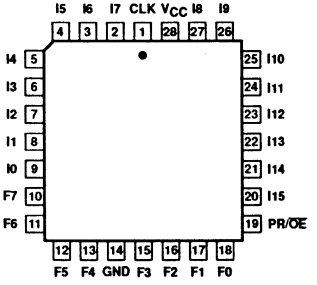
PIN CONFIGURATIONS

N Packages



N = Plastic DIP (600mil-wide)
N3 = Plastic DIP (300mil-wide)

A Package



A = Plastic Leaded Chip Carrier

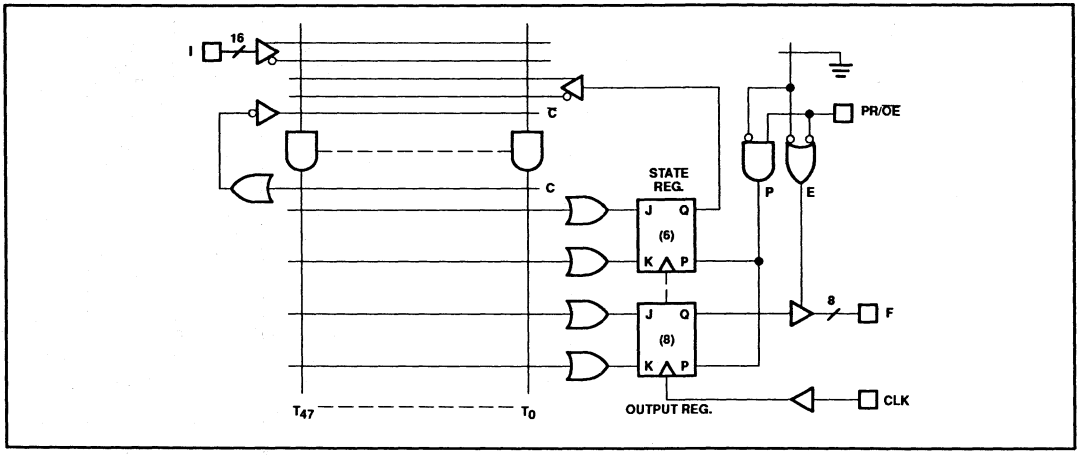
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
28-pin Plastic Dual-In-Line, 600mil-wide	PLUS105–45N
28-pin Plastic Dual-In-Line, 300mil-wide	PLUS105–45N3
28-pin Plastic Leaded Chip Carrier, 450mil-square	PLUS105–45A

Programmable logic sequencer (16 × 48 × 8)

PLUS105-45

FUNCTIONAL DIAGRAM



PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION	POLARITY
1	CLK	**Clock:** The Clock input to the State and Output Registers. A Low-to-High transition on this line is necessary to update the contents of both state and output registers.	Active-High (H)
2-9, 26, 27 20-22	I0 - I9, I13 - I15	**Logic Inputs:** The 13 external inputs to the AND array used to program jump conditions between machine states, as determined by a given logic sequence. True and complement signals are generated via use of "H" and "L".	Active-High/ Low (H/L)
23	I12	**Logic/Diagnostic Input:** A 14th external logic input to the AND array, as above, when exercising standard TTL levels. When I12 is held at +10V, device outputs F0 - F5 reflect the contents of State Register bits P_0 - P_5. The contents of each Output Register remains unaltered.	Active-High/ Low (H/L)
24	I11	**Logic/Diagnostic Input:** A 15th external logic input to the AND array, as above, when exercising standard TTL levels. When I11 is held at +10V, device outputs F0 - F5 become direct inputs for State Register bits P_0 - P_5; a Low-to-High transition on the clock line loads the values on pins F0 - F5 into the State Register bits P_0 - P_5. The contents of each Output Register remains unaltered.	Active-High/ Low (H/L)
25	I10	**Logic/Diagnostic Input:** A 16th external logic input to the AND array, as above, when exercising standard TTL levels. When I10 is held at +10V, device outputs F0 - F7 become direct inputs for Output Register bits Q0 - Q7; a Low-to-High transition on the clock line loads the values on pins F0 - F7 into the Output Register bits Q0 - Q7. The contents of each State Register remains unaltered.	Active-High/ Low (H/L)
10-13 15-18	F0 - F7	**Logic Outputs/Diagnostic Outputs/Diagnostic Inputs:** Eight device outputs which normally reflect the contents of Output Register bits Q0 - Q7, when enabled. When I12 is held at +10V, F0 - F5 = (P_0 - P_5). When I11 is held at +10V, F0 - F5 become inputs to State Register bits P_0 - P_5. When I10 is held at +10V, F0 - F7 become inputs to Output Register bits Q0 - Q7.	Active-High (H)
19	PR/$\overline{OE}$	**Preset or Output Enable Input:** **A user programmable function:** • **Preset:** Provides an asynchronous preset to logic "1" of all State and Output Register bits. PR overrides Clock, and when held High, clocking is inhibited and F0 - F7 are High. Normal clocking resumes with the first full clock pulse following a High-to-Low clock transition, after the Preset signal goes low. See timing definitions.	Active-High (H)
		• **Output Enable:** Provides an output enable function to buffers F0 - F7 from the Output Registers.	Active-Low (L)

Programmable logic sequencer (16 × 48 × 8)

PLUS105-45

TRUTH TABLE [1, 2, 3, 4, 5, 6]

V_{CC}	OPTION										
	PR	$\overline{OE}$	I10	I11	I12	CK	J	K	Q_P	Q_F	F
	H		*	*	*	X	X	X	H	H	Q_F
	L		+10V	X	X	↑	X	X	Q_P	L	L
	L		+10V	X	X	↑	X	X	Q_P	H	H
	L		X	+10V	X	↑	X	X	L	Q_F	L
	L		X	+10V	X	↑	X	X	H	Q_F	H
	L		X	X	+10V	X	X	X	Q_P	Q_F	Q_P
	L		X	X	X	X	X	X	Q_P	Q_F	Q_F
		H	X	X	*	X	X	X	Q_P	Q_F	Hi-Z
+5V		X	+10V	X	X	↑	X	X	Q_P	L	L
		X	+10V	X	X	↑	X	X	Q_P	H	H
		X	X	+10V	X	↑	X	X	L	Q_F	L
		X	X	+10V	X	↑	X	X	H	Q_F	H
		L	X	X	+10V	X	X	X	Q_P	Q_F	Q_P
		L	X	X	X	X	X	X	Q_P	Q_F	Q_F
		L	X	X	X	↑	L	L	Q_P	Q_F	Q_F
		L	X	X	X	↑	L	H	L	L	L
		L	X	X	X	↑	H	L	H	H	H
		L	X	X	X	↑	H	H	$\overline{Q_P}$	$\overline{Q_F}$	$\overline{Q_F}$
↑	X	X	X	X	X	X	X	X	H	H	

NOTES:

1. Positive Logic:
   J-K (or S/R) = $T_0 + T_1 + T_2 + \ldots T_{47}$
   $T_n = (C_0)\ (I0, I1, I2, \ldots)\ (P_0, P_1, \ldots P_5)$
2. Either Preset (Active-High) or Output Enable (Active-Low) are available, but not both. The desired function is a user-programmable option.
3. ↑ denotes transition from Low-to-High level.
4. * = H or L or +10V
5. X = Don't Care (≤ 5.5V)
6. When using the F_n pins as inputs to the State and Output Registers in diagnostic mode, the F buffers are 3-Stated and the indicated levels on the output pins are forced by the user.

VIRGIN STATE

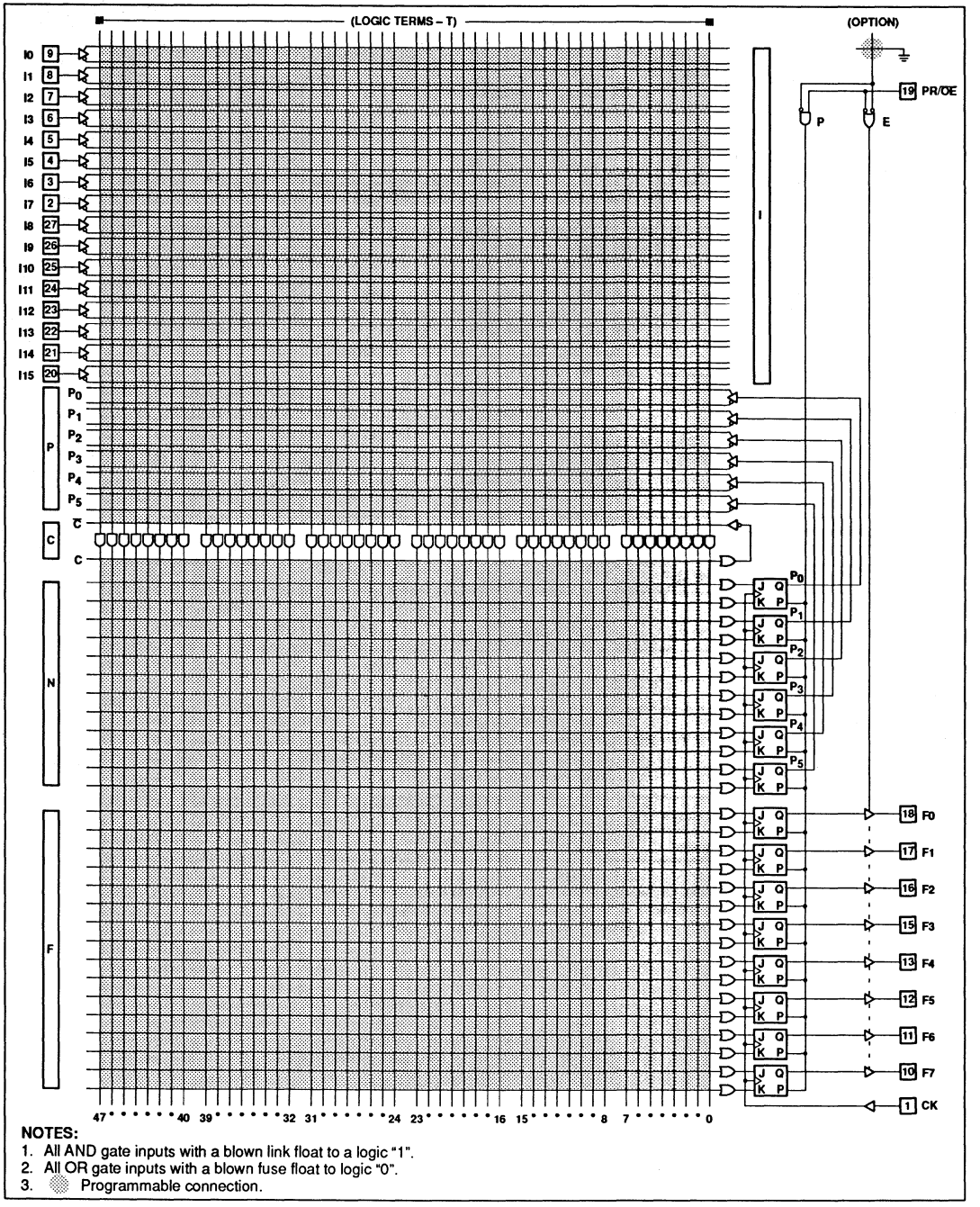
A factory-shipped virgin device contains all fusible links intact, such that:

1. PR/$\overline{OE}$ option is set to PR. Note that even if the PR function is not used, all registers are preset to "1" by the power-up procedure.
2. All transition terms are disabled (0).
3. All J-K flip-flop inputs are disabled (0).

Programmable logic sequencer (16 × 48 × 8)

PLUS105-45

LOGIC DIAGRAM

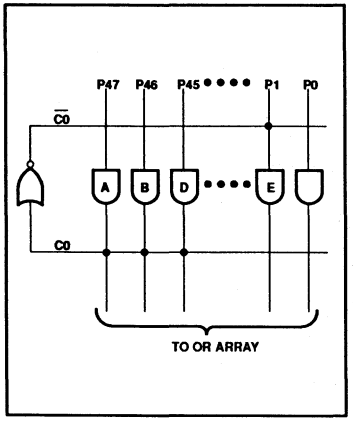


NOTES:
1. All AND gate inputs with a blown link float to a logic "1".
2. All OR gate inputs with a blown fuse float to logic "0".
3. ▒ Programmable connection.

Programmable logic sequencer (16 × 48 × 8)

PLUS105-45

COMPLEMENT ARRAY DETAIL



The complement array is a special sequencer feature that is often used for detecting illegal states. It is also ideal for generating IF-THEN-ELSE logic statements with a minimum number of product terms.

The concept is deceptively simple. If you subscribe to the theory that the expressions (/A * /B * /C) and $(\overline{A + B + C})$ are equivalent, you will begin to see the value of this single term NOR array.

The complement array is a single OR gate with inputs from the AND array. The output of the complement array is inverted and fedback to the AND array (NOR function). The output of the array will be LOW if any one or more of the AND terms connected to it are active (HIGH). If, however, all the connected terms are inactive (LOW), which is a classic unknown state, the output of the complement array will be HIGH.

Consider the product terms A, B and D that represent defined states. They are also connected to the input of the complement array. When the condition (not A and not B and not D) exists, the Complement Array will detect this and propagate an Active-High signal to the AND array. This signal can be connected to product term E, which could be used in turn to preset the state machine to a known state. Without the complement array, one would have to generate product terms for all unknown or illegal states. With very complex state machines, this approach can be prohibitive, both in terms of time and wasted resources.

Note that use of the Complement Array adds an additional delay path through the device. Refer to the AC Electrical Characteristics for details.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

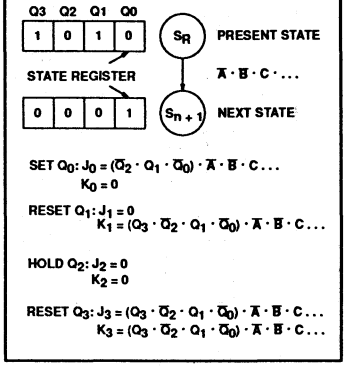
ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS MIN	RATINGS MAX	UNIT
V_{CC}	Supply voltage		+7.0	V_{DC}
V_{IN}	Input voltage		+5.5	V_{DC}
V_{OUT}	Output voltage		+5.5	V_{DC}
I_{IN}	Input currents	–30	+30	mA
I_{OUT}	Output currents		+100	mA
T_{amb}	Operating temperature range	0	+75	°C
T_{stg}	Storage temperature range	–65	+150	°C

NOTE:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

LOGIC FUNCTION



Programmable logic sequencer (16 × 48 × 8)

PLUS105-45

DC ELECTRICAL CHARACTERISTICS

$0°C \leq T_{amb} \leq 75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			MIN	TYP[1]	MAX	
Input voltage[2]						
V_{IH}	High	V_{CC} = MAX	2.0			V
V_{IL}	Low	V_{CC} = MIN			0.8	V
V_{IC}	Clamp[3]	V_{CC} = MIN, I_{IN} = –12mA		–0.8	–1.2	V
Output voltage[2]						
		V_{CC} = MIN				
V_{OH}	High	I_{OH} = –2mA	2.4			V
V_{OL}	Low	I_{OL} = 9.6mA		0.35	0.45	V
Input current						
		V_{CC} = MAX				
I_{IH}	High	V_{IN} = V_{CC}		<1	30	µA
I_{IL}	Low	V_{IN} = 0.45V		–20	–250	µA
Output current						
		V_{CC} = MAX				
$I_{O(OFF)}$	Hi-Z state	V_{OUT} = 2.7V		1	40	µA
		V_{OUT} = 0.45V		–1	–40	µA
I_{OS}	Short circuit[3, 4]	V_{OUT} = 0V	–15		–70	mA
I_{CC}	V_{CC} supply current[5]	V_{CC} = MAX		160	200	mA
Capacitance						
		V_{CC} = 5.0V				
C_{IN}	Input	V_{IN} = 2.0V		8		pF
C_{OUT}	Output	V_{OUT} = 2.0V		10		pF

NOTES:
1. All typical values are at V_{CC} = 5V, T_{amb} = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Test one at a time.
4. Duration of short circuit should not exceed 1 second.
5. I_{CC} is measured with the PR/$\overline{OE}$ input grounded, all other inputs at 4.5V and the outputs open.

AC ELECTRICAL CHARACTERISTICS

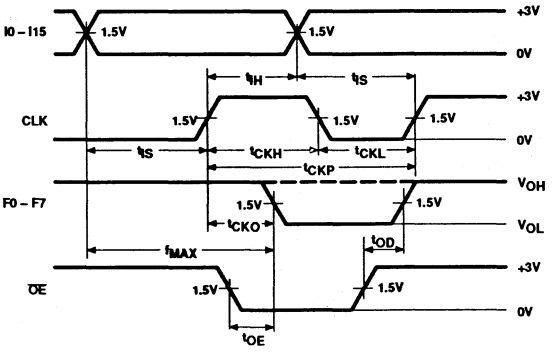
$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30PF$, $0°C \leq T_{amb} \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	FROM	TO	LIMITS MIN	LIMITS TYP[1]	LIMITS MAX	UNIT
Pulse Width							
t_{CKH}	Clock High	CK +	CK –	9	8		ns
t_{CKL}	Clock Low	CK –	CK +	9	8		ns
t_{CKP}	Clock Period	CK +	CK +	18	16		ns
t_{PRH}	Preset pulse	PR +	PR -	10	8		ns
Setup Time							
t_{IS1}	Input	Input ±	CK+	13	12		ns
t_{IS2}	Input (through Complement Array)	Input ±	CK +	23	20		ns
t_{VS}	Power-on preset	V_{CC} +	CK –	0	–10		ns
t_{PRS}	Clock resume (after preset)	PR –	CK –	0	–5		ns
t_{NVCK}	Clock lockout (before preset)	CK –	PR –	10	5		ns
Hold Time							
t_{IH}	Input	CK +	Input ±	0	–5		ns
Diagnostic Mode							
t_{RJS}	Initialization of diagnostic mode	I10, I11 or I12+ (to 10V)	F_n as inputs	50	25		ns
t_{RJH}	Clock for diagnostic mode	CK +	Register input jam	50	25		ns
Propagation Delay[3]							
t_{CKO}	Clock	CK +	Output ±		8	9	ns
t_{OE}	Output enable[2]	OE –	Output –		8	9	ns
t_{OD}	Output disable[2]	OE +	Output +		8	9	ns
t_{PR}	Preset	PR +	Output +		12	15	ns
t_{PPR}	Power-on preset	V_{CC} +	Output +		0	10	ns
Frequency of Operation							
f_{MAX1}	Without Complement Array $\left(\frac{1}{t_{IS1} + t_{CKO}}\right)$	Input ±	Output ±	45.5	50.0		MHz
f_{MAX2}	With Complement Array $\left(\frac{1}{t_{IS2} + t_{CKO}}\right)$	Input thru Complement Array ±	Output ±	31.3	35.7		MHz
f_{MAX3}	Internal feedback without Complement Array $\left(\frac{1}{t_{CKL} + t_{CKH}}\right)$	Register Output ±	Register Input ±	55.6	62.5		MHz
f_{MAX4}	Internal feedback with Complement Array $\left(\frac{1}{t_{IS2}}\right)$	Register Output thru Complement Array ±	Register Input ±	43.5	50.0		MHz
f_{CLK}	Clock frequency	CK +	CK +	55.6	62.5		MHz

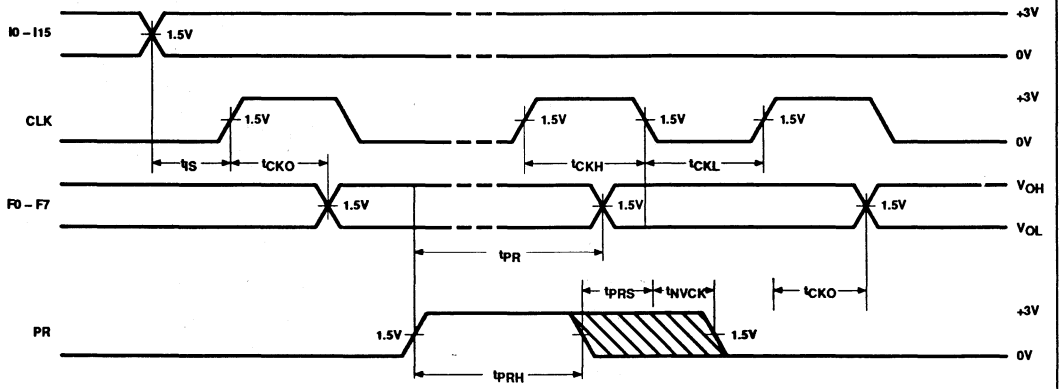
NOTES:

1. All typical values are at $V_{CC} = 5V$, $T_{amb} = +25°C$.
2. For 3-State output; output enable times are tested with $C_L = 30pF$ to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with $C_L = 5pF$. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} - 0.5V)$ with S_1 open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with S_1 closed.
3. All propagation delays and setup times are meausred and specified under worst case conditions.

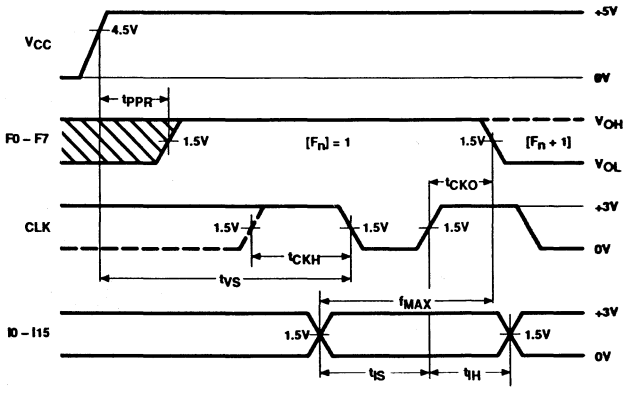
TIMING DIAGRAMS



Sequential Mode

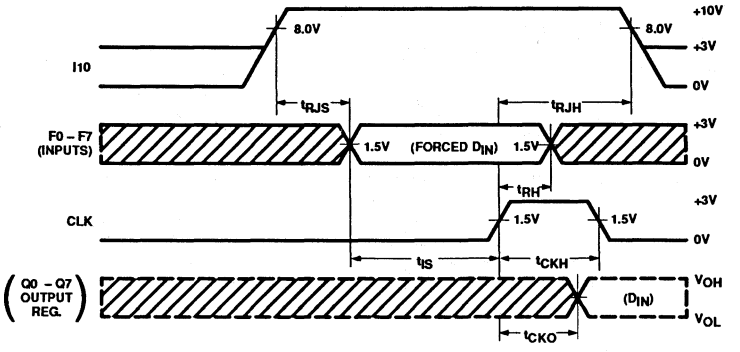


Asynchronous Preset

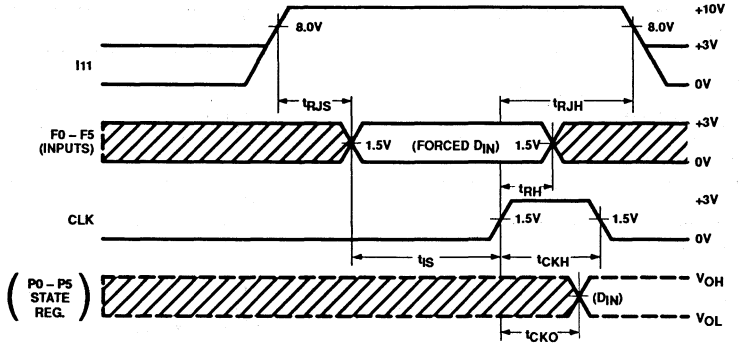


Power-On Preset

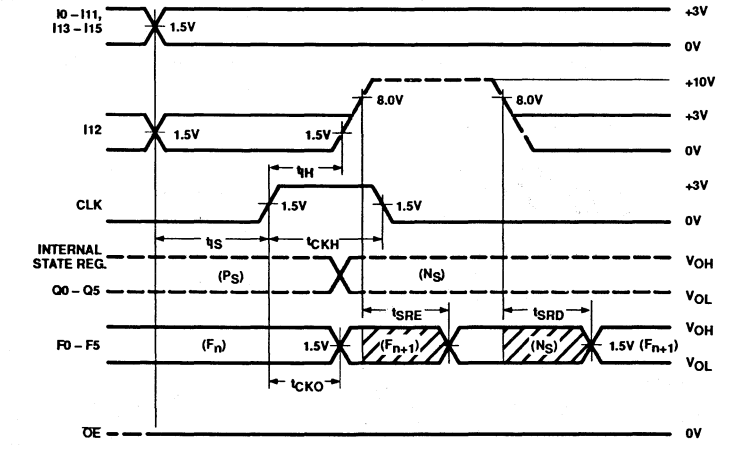
TIMING DIAGRAMS (Continued)



Diagnostic Mode—Output Register Input Jam



Diagnostic Mode—State Register Input Jam



Diagnostic Mode—State Register Outputs

Programmable logic sequencer (16 × 48 × 8)

PLUS105-45

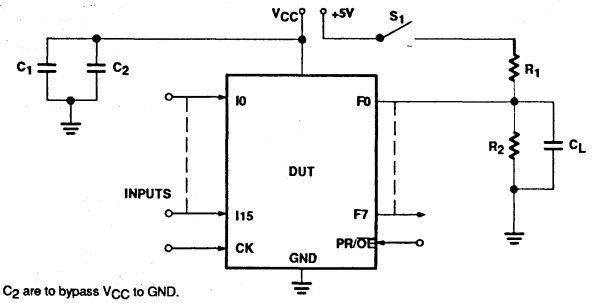
TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{IH}	Required delay between positive transition of Clock and end of valid Input data.
t_{IS1}	Required delay between beginning of valid input and positive transition of Clock.
t_{IS2}	Required delay between beginning of valid Input and positive transition of Clock, when using optional Complement Array (two passes necessary through the AND Array).
t_{CKH}	Width of input clock pulse
t_{CKL}	Interval between clock pulses.
t_{CKO}	Delay between positive transition of Clock and when Outputs become valid (with PR/$\overline{OE}$ Low).
t_{CKP}	Minimum guaranteed clock period.
t_{NVCK}	Required delay between the negative transition of the clock and the negative transition of the Asynchronous PRESET to guarantee that the clock edge is not detected as a valid negative transition.

SYMBOL	PARAMETER
t_{OD}	Delay between beginning of Output Enable High and when Outputs are in the OFF-state.
t_{OE}	Delay between beginning of Output Enable Low and when Outputs become valid.
t_{PPR}	Delay between V_{CC} (after power-on) and when Outputs become preset at "1".
t_{PR}	Delay between positive transition of Preset and when Outputs become valid at "1".
t_{PRH}	Width of preset input pulse.
t_{PRS}	Required delay between negative transition of Asynchronous Preset and the first positive transition of Clock.
t_{RH}	Required delay between positive transition of clock and the end of valid input data (F0–F7 as inputs), when jamming data into the State or Output registers in the Diagnostic Mode.

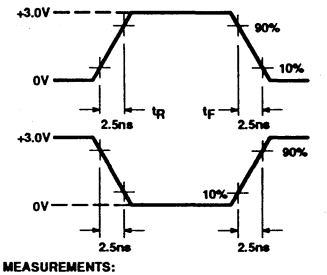
SYMBOL	PARAMETER
t_{RJH}	Required delay between positive transition of clock and return of input I10, I11 OR I12 from Diagnostic Mode (10V).
t_{RJS}	Required delay between inputs I10, I11 or I12 transition to Diagnostic Mode (10V), and when the output pins become available as inputs.
t_{SRD}	Delay between input (I12) transition to Logic mode and when the Outputs reflect the contents of the Output Register.
t_{SRE}	Delay between input I12 transition to Diagnostic Mode and when the Outputs reflect the contents of the State Register.
t_{VS}	Required delay between V_{CC} (after power-on) and negative transition of Clock preceding first reliable clock pulse.
f_{CLK}	Minimum guaranteed clock frequency (register toggle frequency)
f_{MAX}	Minimum guaranteed operating frequency.

TEST LOAD CIRCUITS



NOTE:
C_1 and C_2 are to bypass V_{CC} to GND.

VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

LOGIC PROGRAMMING

PLUS105-45 is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Signetics' SLICE and SNAP design software packages. ABEL™, CUPL™ and PALASM® 90 design software packages also support the PLUS105-45 architecture.

All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

PLUS105-45 logic designs can also be generated using the program table entry format, which is detailed on the following pages. This program table entry format is supported by SLICE only. The SLICE design package is available, free of charge, to qualified users.

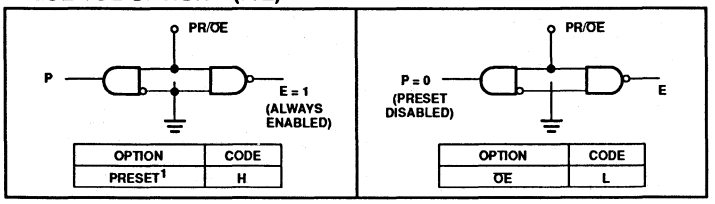
To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

ABEL is a trademark of Data I/O Corp.
CUPL is a trademark of Logical Devices, Inc.
PALASM is a registered trademark of AMD Corp.

Programmable logic sequencer (16 × 48 × 8)

PLUS105-45

PRESET/OE OPTION – (P/E)

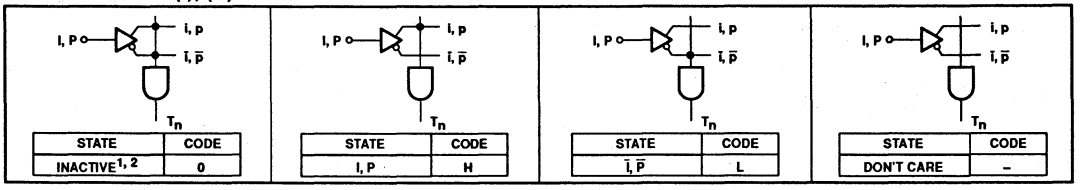


OPTION	CODE
PRESET[1]	H

OPTION	CODE
$\overline{OE}$	L

PROGRAMMING THE PLUS105–45:
The PLUS105–45 has a power-up preset feature. This feature insures that the device will power-up in a known state with all register elements (State and Output Register) at logic High (H). When programming the device it is important to realize this is the initial state of the device. You *must* provide a next state jump if you do not wish to use all Highs (H) as the present state.

"AND" ARRAY – (I), (P)



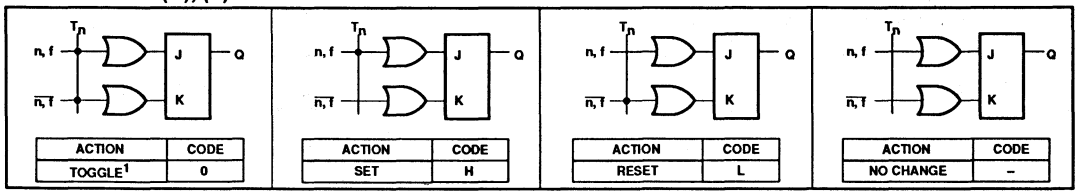
STATE	CODE
INACTIVE[1, 2]	0

STATE	CODE
I, P	H

STATE	CODE
$\overline{I}$, $\overline{P}$	L

STATE	CODE
DON'T CARE	–

"OR" ARRAY – (N), (F)



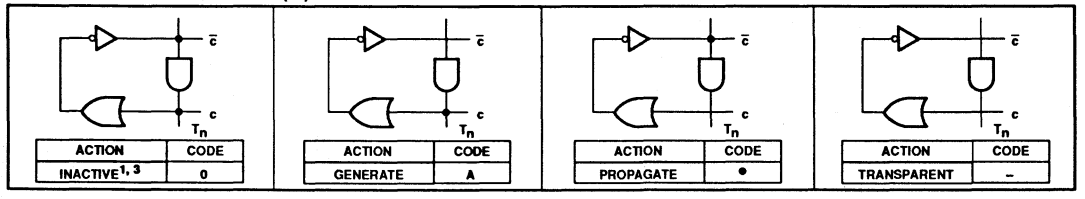
ACTION	CODE
TOGGLE[1]	0

ACTION	CODE
SET	H

ACTION	CODE
RESET	L

ACTION	CODE
NO CHANGE	–

"COMPLEMENT" ARRAY – (C)



ACTION	CODE
INACTIVE[1, 3]	0

ACTION	CODE
GENERATE	A

ACTION	CODE
PROPAGATE	•

ACTION	CODE
TRANSPARENT	–

NOTES:
1. This is the initial unprogrammed state of all link pairs.
2. Any gate T_n will be unconditionally inhibited if both the true and complement fuses of any input (I,P) are left intact.
3. To prevent oscillations, this state is not allowed for C link pairs coupled to active gates T_n.

Programmable logic sequencer (16 × 48 × 8)

PLUS105-45

PLUS105 PROGRAM TABLE

CUSTOMER NAME_____
PURCHASE ORDER #_____
SIGNETICS DEVICE # CF (XXXX)
CUSTOMER SYMBOLIZED PART #_____
TOTAL NUMBER OF PARTS_____
PROGRAM TABLE_____
REV_____
DATE_____

PROGRAM TABLE ENTRIES

AND

C_n	
INACTIVE	0
GENERATE	A
PROPAGATE	•
TRANSPARENT	—

I_m, P_s	
INACTIVE	0
I, P	H
$\overline{I}$, $\overline{P}$	L
DON'T CARE	—

OR

Ns, Fr	
INACTIVE or TOGGLE	0
SET	H
RESET	L
NO CHANGE	—

OPTION

P/E	
PRESET	H
$\overline{OE}$	L

TERM	C_n	AND: INPUT (I_m) 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	AND: PRESENT STATE (P_s) 5 4 3 2 1 0	REMARKS	OPTION (P/E) OR: NEXT STATE (Ns) 5 4 3 2 1 0	OUTPUT (Fr) 7 6 5 4 3 2 1 0
0						
1						
2						
3						
4						
5						
6						
7						
8						
9						
10						
11						
12						
13						
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41						
42						
43						
44						
45						
46						
47						
PIN NO.		20 21 22 23 24 25 26 27 2 3 4 5 6 7 8 9				10 11 12 13 15 16 17 18
VARIABLE NAME						

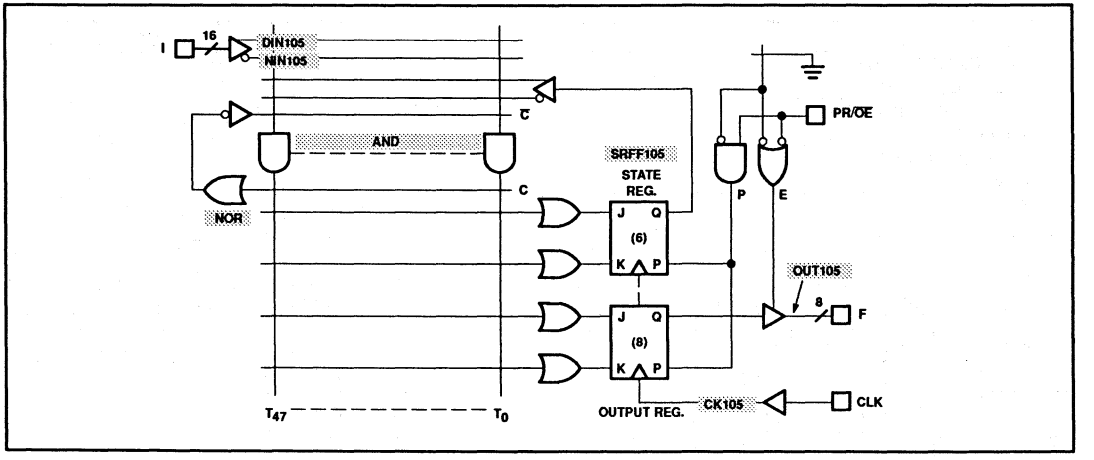
NOTES:

1. The device is shipped with all links initially intact. Thus, a background of "0" for all Terms, and an "H" for the P/E option, exists in the table, shown BLANK instead for clarity.
2. Unused C_n, I_m, and P_s bits are normally programmed Don't Care (–).
3. Unused Transition Terms can be left blank for future code modification, or programmed as (–) for maximum speed.
4. Letters in variable fields are used as identifiers by logic type programmers.

Programmable logic sequencer (16 × 48 × 8)

PLUS105-45

SNAP RESOURCE SUMMARY DESIGNATIONS



Programmable logic sequencer (16 × 48 × 8)

PLUS105-55

DESCRIPTION

The PLUS105-55 is a bipolar programmable state machine of the Mealy type. Both the AND and the OR array are user-programmable. All 48 AND gates are connected to the 16 external dedicated inputs (I0 - I15) and to the feedback paths of the 6 buried State Registers (Q_{P0}-Q_{P5}). Because the OR array is programmable, any one or all of the 48 transition terms can be connected to any or all of the State and Output Registers.

All state transition terms can include True, False and Don't Care states of the controlling state variables. A Complement Transition Array supports complex IF-THEN-ELSE state transitions with a single product term.

The PLUS105-55 device features edge-triggered, J-K flip-flops, which provide the added flexibility of the toggle function which is indeterminate on S-R flip-flops. Because the J-K function is a superset of the S-R flip-flop function, the PLUS105-55 is backward compatible with all 105-type devices that have S-R flip-flops. Asynchronous Preset/Output Enable functions are available.

The PLUS105-55 is pin-for-pin and software compatible with Signetics PLS105 and PLS105A Logic Sequencers, as well as other commercially available 105-type programmable logic devices.

To facilitate testing of state machine designs, diagnostic mode features for register preset and buried state register observability have been incorporated into the PLUS105-55 device architecture.

Ordering codes are listed in the Ordering Information Table.

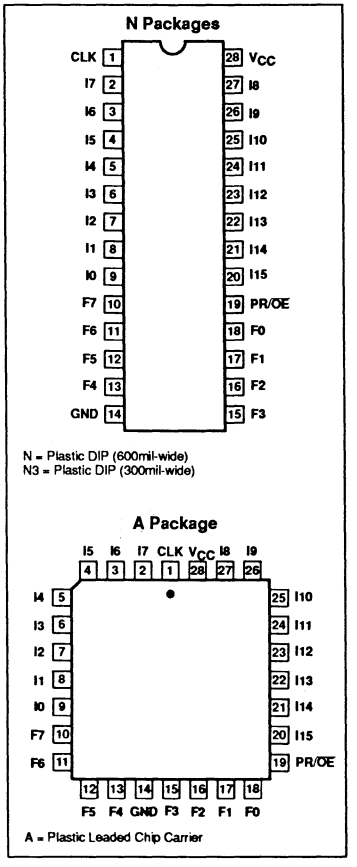
FEATURES

- 55MHz operating frequency
  - 71.4MHz clock rate
  - No OR term loading restrictions
- Available in 300mil skinny DIP, 600mil-wide DIP, and PLCC packages
- Pin and software compatible with other commerically available 105 sequencers
- 16 input variables
- 8 output functions
- 48 transition terms
- 6-bit State Register
- 8-bit Output Register
- Transition complement array
- Positive edge-triggered clocked J-K (or S-R) flip-flops
- Security fuse
- Programmable Asynchronous Preset or Output Enable
- Power-on preset to (all "1"s) of internal registers
- Power dissipation: 800mW (typ.)
- TTL compatible
- Single +5V supply
- 3-State outputs

APPLICATIONS

- Interface protocols
- Sequence detectors
- Peripheral controllers
- Timing generators
- Sequential circuits
- Elevator controllers
- Security Locking systems
- Counters
- Shift registers

PIN CONFIGURATIONS



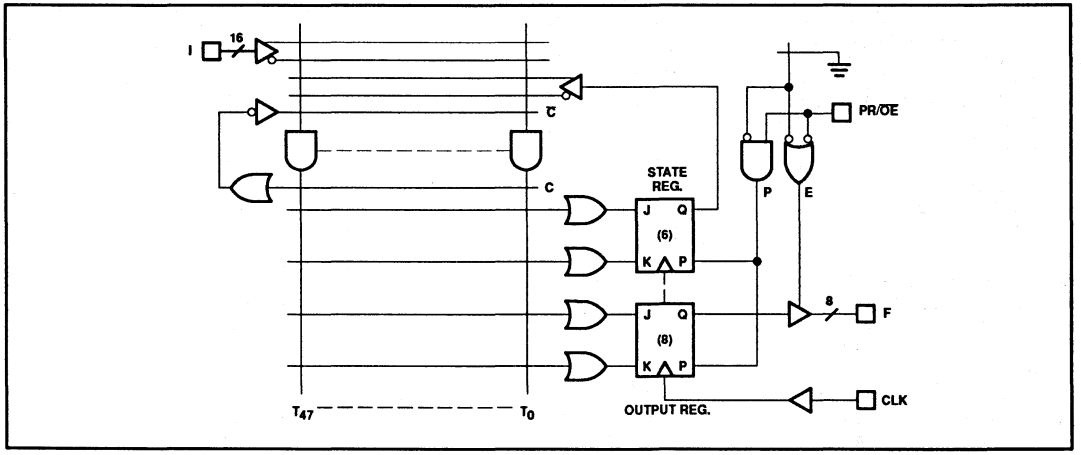
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
28-pin Plastic Dual-In-Line, 600mil-wide	PLUS105-55N
28-pin Plastic Dual-In-Line, 300mil-wide	PLUS105-55N3
28-pin Plastic Leaded Chip Carrier, 450mil-square	PLUS105-55A

Programmable logic sequencer (16 × 48 × 8)

PLUS105-55

FUNCTIONAL DIAGRAM



PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION	POLARITY
1	CLK	**Clock:** The Clock input to the State and Output Registers. A Low-to-High transition on this line is necessary to update the contents of both state and output registers.	Active-High (H)
2-9, 26, 27 20-22	I0 - I9, I13 - I15	**Logic Inputs:** The 13 external inputs to the AND array used to program jump conditions between machine states, as determined by a given logic sequence. True and complement signals are generated via use of "H" and "L".	Active-High/ Low (H/L)
23	I12	**Logic/Diagnostic Input:** A 14th external logic input to the AND array, as above, when exercising standard TTL levels. When I12 is held at +10V, device outputs F0 - F5 reflect the contents of State Register bits P0 - P5. The contents of each Output Register remains unaltered.	Active-High/ Low (H/L)
24	I11	**Logic/Diagnostic Input:** A 15th external logic input to the AND array, as above, when exercising standard TTL levels. When I11 is held at +10V, device outputs F0 - F5 become direct inputs for State Register bits P0 - P5; a Low-to-High transition on the clock line loads the values on pins F0 - F5 into the State Register bits P0 - P5. The contents of each Output Register remains unaltered.	Active-High/ Low (H/L)
25	I10	**Logic/Diagnostic Input:** A 16th external logic input to the AND array, as above, when exercising standard TTL levels. When I10 is held at +10V, device outputs F0 - F7 become direct inputs for Output Register bits Q0 - Q7; a Low-to-High transition on the clock line loads the values on pins F0 - F7 into the Output Register bits Q0 - Q7. The contents of each State Register remains unaltered.	Active-High/ Low (H/L)
10-13 15-18	F0 - F7	**Logic Outputs/Diagnostic Outputs/Diagnostic Inputs:** Eight device outputs which normally reflect the contents of Output Register bits Q0 - Q7, when enabled. When I12 is held at +10V, F0 - F5 = (P0 - P5). When I11 is held at +10V, F0 - F5 become inputs to State Register bits P0 - P5. When I10 is held at +10V, F0 - F7 become inputs to Output Register bits Q0 - Q7.	Active-High (H)
19	PR/$\overline{OE}$	**Preset or Output Enable Input:** **A user programmable function:**	
		• **Preset:** Provides an asynchronous preset to logic "1" of all State and Output Register bits. PR overrides Clock, and when held High, clocking is inhibited and F0 - F7 are High. Normal clocking resumes with the first full clock pulse following a High-to-Low clock transition, after the Preset signal goes Low. See timing definitions.	Active-High (H)
		• **Output Enable:** Provides an output enable function to buffers F0 - F7 from the Output Registers.	Active-Low (L)

Programmable logic sequencer (16 × 48 × 8)

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TRUTH TABLE[1, 2, 3, 4, 5, 6]

V_{CC}	OPTION PR	OPTION $\overline{OE}$	I10	I11	I12	CK	J	K	Q_P	Q_F	F
	H		*	*	*	X	X	X	H	H	Q_F
	L		+10V	X	X	↑	X	X	Q_P	L	L
	L		+10V	X	X	↑	X	X	Q_P	H	H
	L		X	+10V	X	↑	X	X	L	Q_F	L
	L		X	+10V	X	↑	X	X	H	Q_F	H
	L		X	X	+10V	X	X	X	Q_P	Q_F	Q_P
	L		X	X	X	X	X	X	Q_P	Q_F	Q_F
		H	X	X	*	X	X	X	Q_P	Q_F	Hi-Z
+5V		X	+10V	X	X	↑	X	X	Q_P	L	L
		X	+10V	X	X	↑	X	X	Q_P	H	H
		X	X	+10V	X	↑	X	X	L	Q_F	L
		X	X	+10V	X	↑	X	X	H	Q_F	H
		L	X	X	+10V	X	X	X	Q_P	Q_F	Q_P
		L	X	X	X	X	X	X	Q_P	Q_F	Q_F
		L	X	X	X	↑	L	L	Q_P	Q_F	Q_F
		L	X	X	X	↑	L	H	L	L	L
		L	X	X	X	↑	H	L	H	H	H
		L	X	X	X	↑	H	H	$\overline{Q_P}$	$\overline{Q_F}$	$\overline{Q_F}$
↑	X	X	X	X	X	X	X	X	H	H	

NOTES:

1. Positive Logic:
   J-K (or S/R) = $T_0 + T_1 + T_2 + \ldots T_{48}$
   $T_n = (C_0)\ (I0, I1, I2, \ldots)\ (P_0, P_1, \ldots P_5)$
2. Either Preset (Active-High) or Output Enable (Active-Low) are available, but not both. The desired function is a user-programmable option.
3. ↑ denotes transition from Low-to-High level.
4. * = H or L or +10V
5. X = Don't Care (≤ 5.5V)
6. When using the F_n pins as inputs to the State and Output Registers in diagnostic mode, the F buffers are 3-Stated and the indicated levels on the output pins are forced by the user.

VIRGIN STATE

A factory-shipped virgin device contains all fusible links intact, such that:

1. PR/$\overline{OE}$ option is set to PR. Note that even if the PR function is not used, all registers are preset to "1" by the power-up procedure.
2. All transition terms are disabled (0).
3. All J-K flip-flop inputs are disabled (0).

Programmable logic sequencer (16 × 48 × 8)

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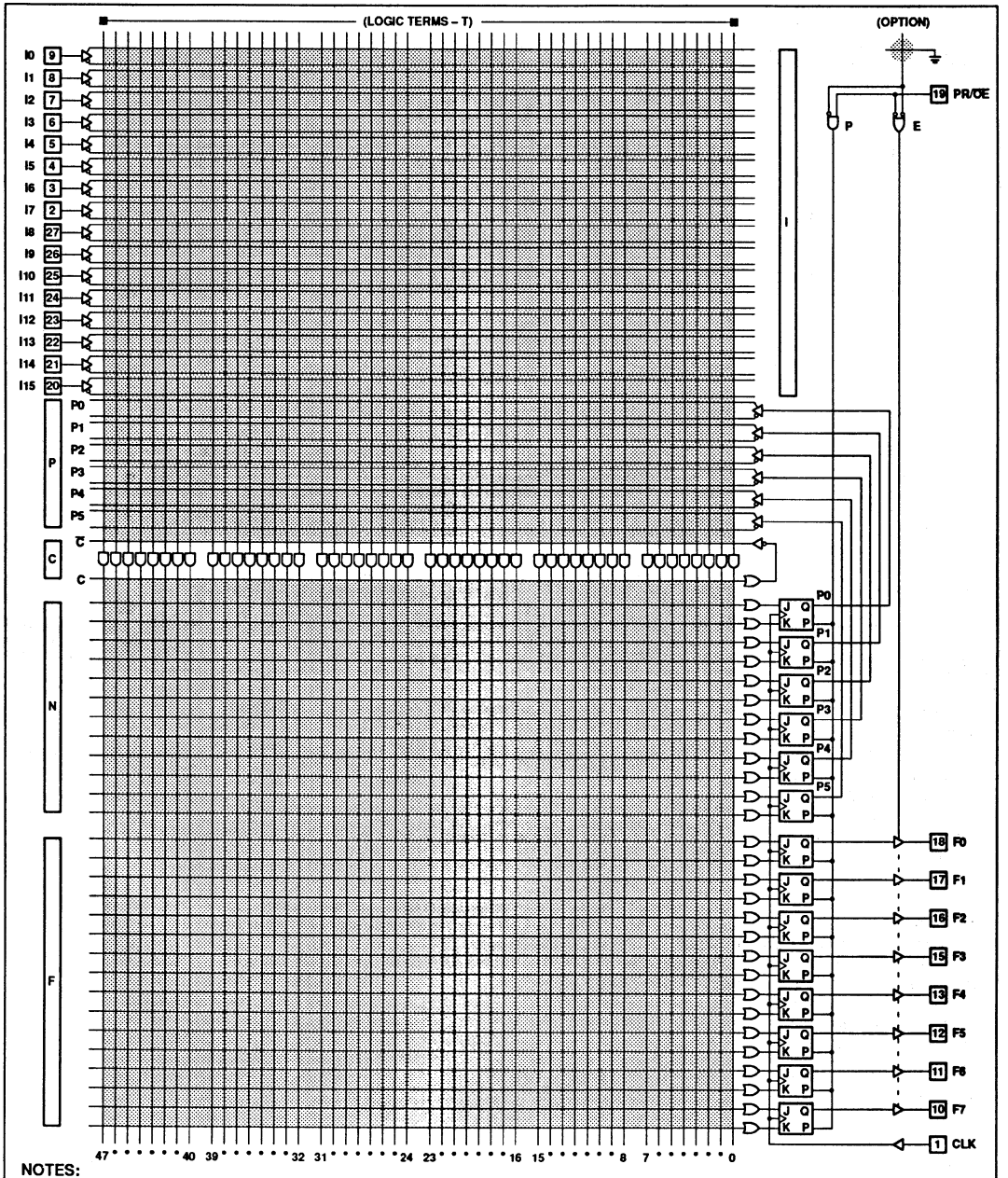
LOGIC DIAGRAM



NOTES:

1. All AND gate inputs with a blown link float to a logic "1".
2. All OR gate inputs with a blown fuse float to logic "0".
3. ⁘ Programmable connection.

Programmable logic sequencer (16 × 48 × 8)

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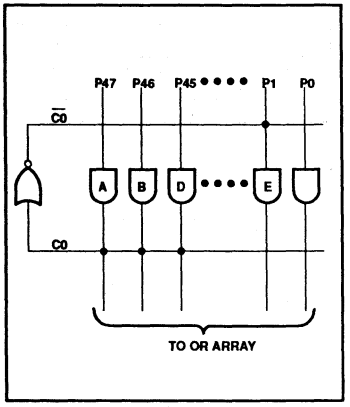
COMPLEMENT ARRAY DETAIL



The complement array is a special sequencer feature that is often used for detecting illegal states. It is also ideal for generating IF-THEN-ELSE logic statements with a minimum number of product terms.

The concept is deceptively simple. If you subscribe to the theory that the expressions (/A * /B * /C) and $(\overline{A + B + C})$ are equivalent, you will begin to see the value of this single term NOR array.

The complement array is a single OR gate with inputs from the AND array. The output of the complement array is inverted and fedback to the AND array (NOR function). The output of the array will be LOW if any one or more of the AND terms connected to it are active (HIGH). If, however, all the connected terms are inactive (LOW), which is a classic unknown state, the output of the complement array will be HIGH.

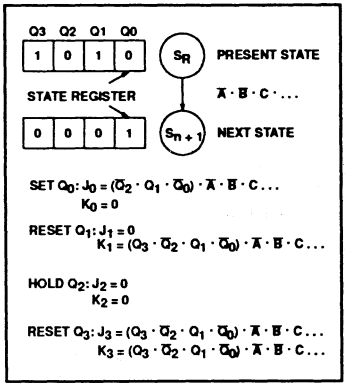
Consider the product terms A, B and D that represent defined states. They are also connected to the input of the complement array. When the condition (not A and not B and not D) exists, the Complement Array will detect this and propagate an Active-High signal to the AND array. This signal can be connected to product term E, which could be used in turn to preset the state machine to a known state. Without the complement array, one would have to generate product terms for all unknown or illegal states. With very complex state machines, this approach can be prohibitive, both in terms of time and wasted resources.

Note that use of the Complement Array adds an additional delay path through the device. Refer to the AC Electrical Characteristics for details.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

LOGIC FUNCTION



ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS		UNIT
		MIN	MAX	
V_{CC}	Supply voltage		+7.0	V_{DC}
V_{IN}	Input voltage		+5.5	V_{DC}
V_{OUT}	Output voltage		+5.5	V_{DC}
I_{IN}	Input currents	-30	+30	mA
I_{OUT}	Output currents		+100	mA
T_{amb}	Operating temperature range	0	+75	°C
T_{stg}	Storage temperature range	-65	+150	°C

NOTE:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

Programmable logic sequencer (16 × 48 × 8)

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DC ELECTRICAL CHARACTERISTICS

$0°C \le T_{amb} \le 75°C$, $4.75V \le V_{CC} \le 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[1]	MAX	
Input voltage[2]						
V_{IH}	High	V_{CC} = MAX	2.0			V
V_{IL}	Low	V_{CC} = MIN			0.8	V
V_{IC}	Clamp[3]	V_{CC} = MIN, I_{IN} = –12mA		–0.8	–1.2	V
Output voltage[2]						
		V_{CC} = MIN				
V_{OH}	High	I_{OH} = –2mA	2.4			V
V_{OL}	Low	I_{OL} = 9.6mA		0.35	0.45	V
Input current						
		V_{CC} = MAX				
I_{IH}	High	V_{IN} = V_{CC}		<1	30	µA
I_{IL}	Low	V_{IN} = 0.45V		–20	–250	µA
Output current						
		V_{CC} = MAX				
$I_{O(OFF)}$	Hi-Z state	V_{OUT} = 2.7V		1	40	µA
		V_{OUT} = 0.45V		–1	–40	µA
I_{OS}	Short circuit[3, 4]	V_{OUT} = 0V	–15		–70	mA
I_{CC}	V_{CC} supply current[5]	V_{CC} = MAX		160	200	mA
Capacitance						
		V_{CC} = 5.0V				
C_{IN}	Input	V_{IN} = 2.0V		8		pF
C_{OUT}	Output	V_{OUT} = 2.0V		10		pF

NOTES:
1. All typical values are at V_{CC} = 5V, T_{amb} = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Test one at a time.
4. Duration of short circuit should not exceed 1 second.
5. I_{CC} is measured with the PR/$\overline{OE}$ input grounded, all other inputs at 4.5V and the outputs open.

AC ELECTRICAL CHARACTERISTICS

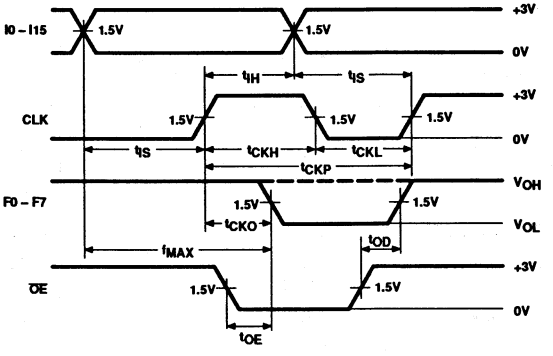
$R_1 = 470\Omega$, $R_2 = 1K\Omega$, $C_L = 30pF$, $0°C \le T_{amb} \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

SYMBOL	PARAMETER	FROM	TO	LIMITS MIN	LIMITS TYP[1]	LIMITS MAX	UNIT
Pulse Width							
t_{CKH}	Clock High	CK +	CK –	7	6.5		ns
t_{CKL}	Clock Low	CK –	CK +	7	6.5		ns
t_{CKP}	Clock Period	CK +	CK +	14	13		ns
t_{PRH}	Preset pulse	PR +	PR –	10	8.0		ns
Setup Time							
t_{IS1}	Input	Input ±	CK +	10	9.5		ns
t_{IS2}	Input (through Complement Array)	Input ±	CK +	20	18.0		ns
t_{VS}	Power-on preset	V_{CC} +	CK –	0	0		ns
t_{PRS}	Clock resume (after preset)	PR –	CK –	0	0		ns
t_{NVCK}	Clock lockout (before preset)	CK –	PR –	12	10.0		ns
Hold Time							
t_{IH}	Input	CK +	Input ±	0	–5		ns
Diagnostic Mode							
t_{RJS}	Initialization of diagnostic mode	I10, I11 or I12 + (to 10V)	F_n as inputs	50	25		ns
t_{RJH}	Clock for diagnostic mode	CK +	Register input jam	50	25		ns
Propagation Delay[2]							
t_{CKO}	Clock	CK +	Output ±		7	8	ns
t_{OE}	Output enable[3]	OE –	Output –		6	8	ns
t_{OD}	Output disable[3]	OE +	Output +		6	8	ns
t_{PR}	Preset	PR +	Output +		12	15	ns
t_{PPR}	Power-on preset	V_{CC} +	Output +		5	10	ns
Frequency of Operation							
f_{MAX1}	Without Complement Array $\left(\frac{1}{t_{IS1} + t_{CKO}}\right)$	Input ±	Output ±	55.6	60.6		MHz
f_{MAX2}	With Complement Array $\left(\frac{1}{t_{IS2} + t_{CKO}}\right)$	Input thru Complement Array ±	Output ±	35.7	40.0		MHz
f_{MAX3}	Internal feedback without Complement Array $\left(\frac{1}{t_{CKL} + t_{CKH}}\right)$	Register Output ±	Register Input ±	71.4	76.9		MHz
f_{MAX4}	Internal feedback with Complement Array $\left(\frac{1}{t_{IS2}}\right)$	Register Output thru Complement Array ±	Register Input ±	50.0	55.6		MHz
f_{CLK}	Clock period	CK +	CK +	71.4	76.9		MHz

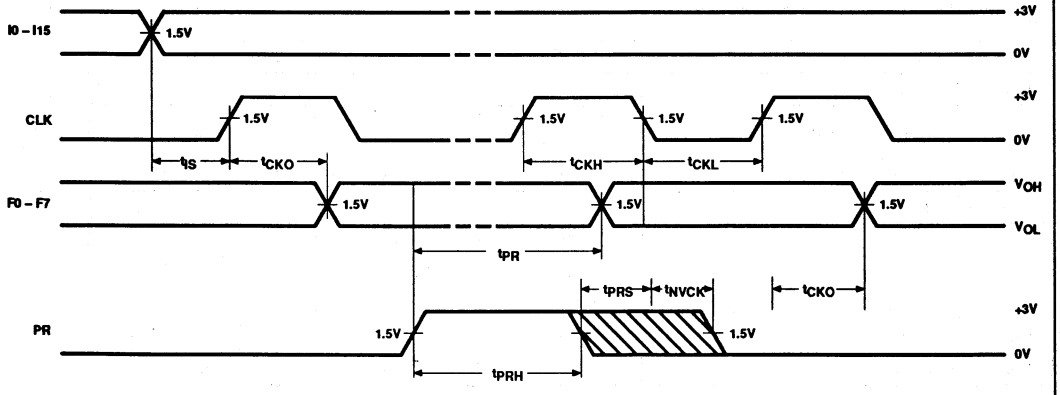
NOTES:

1. All typical values are at $V_{CC} = 5V$, $T_{amb} = +25°C$.
2. All propagation delays and setup times are meausred and specified under worst case conditions.
3. For 3-State output; output enable times are tested with $C_L = 30pF$ to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with $C_L = 5pF$. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} - 0.5V)$ with S_1 open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with S_1 closed.

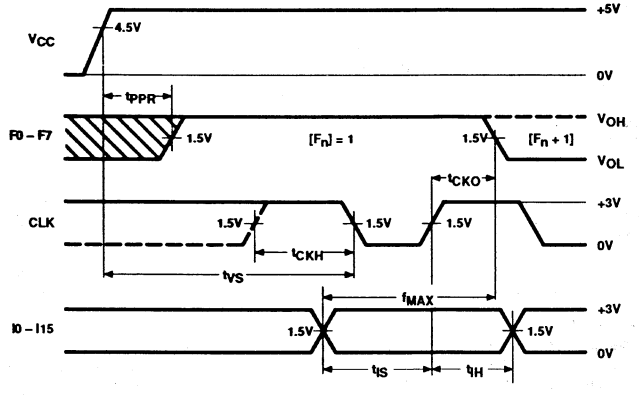
TIMING DIAGRAMS



Sequential Mode

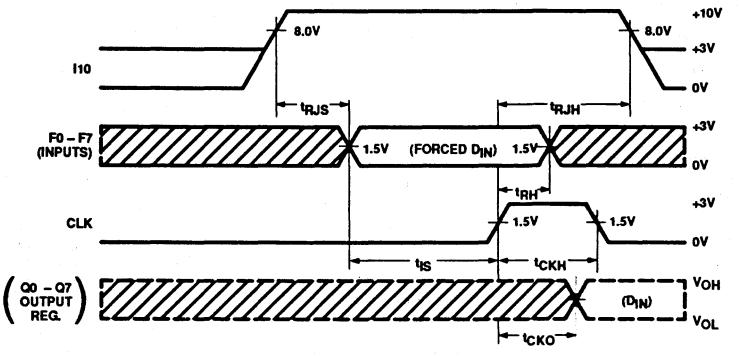


Asynchronous Preset

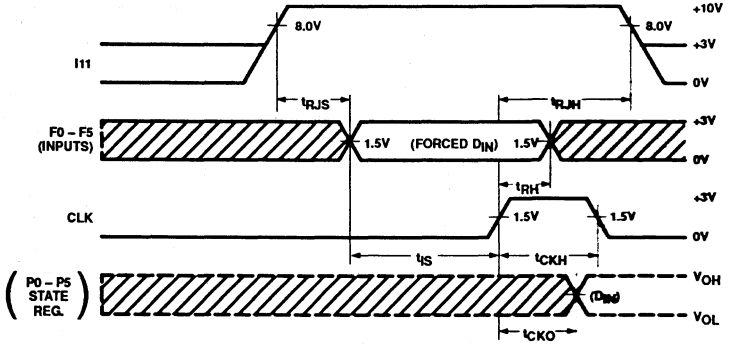


Power-On Preset

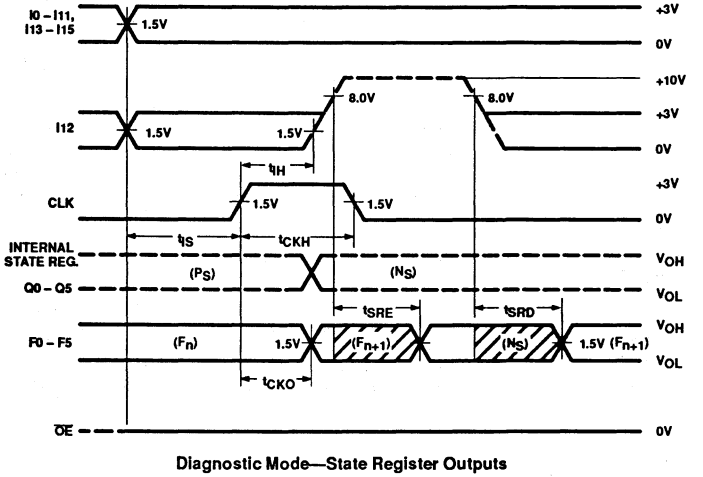
TIMING DIAGRAMS (Continued)



Diagnostic Mode—Output Register Input Jam



Diagnostic Mode—State Register Input Jam



Diagnostic Mode—State Register Outputs

Programmable logic sequencer (16 × 48 × 8)

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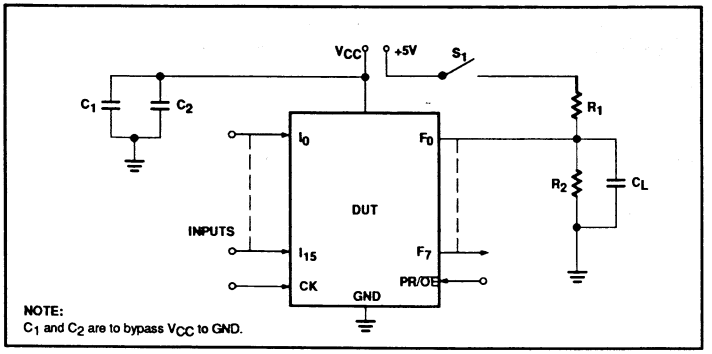
TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{IH}	Required delay between positive transition of Clock and end of valid Input data.
t_{IS1}	Required delay between beginning of valid input and positive transition of Clock.
t_{IS2}	Required delay between beginning of valid Input and positive transition of Clock, when using optional Complement Array (two passes necessary through the AND Array).
t_{CKH}	Width of input clock pulse
t_{CKL}	Interval between clock pulses.
t_{CKO}	Delay between positive transition of Clock and when Outputs become valid (with PR/$\overline{OE}$ Low).
t_{CKP}	Minimum guaranteed clock period.
t_{NVCK}	Required delay between the negative transition of the clock and the negative transition of the Asynchronous PRESET to guarantee that the clock edge is not detected as a valid negative transition.

SYMBOL	PARAMETER
t_{OD}	Delay between beginning of Output Enable High and when Outputs are in the OFF-state.
t_{OE}	Delay between beginning of Output Enable Low and when Outputs become valid.
t_{PPR}	Delay between V_{CC} (after power-on) and when Outputs become preset at "1".
t_{PR}	Delay between positive transition of Preset and when Outputs become valid at "1".
t_{PRH}	Width of preset input pulse.
t_{PRS}	Required delay between negative transition of Asynchronous Preset and the first positive transition of Clock.
t_{RH}	Required delay between positive transition of clock and the end of valid input data (F0 – F7 as inputs), when jamming data into the State or Output registers in the Diagnostic Mode.

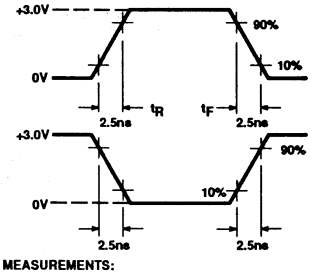
SYMBOL	PARAMETER
t_{RJH}	Required delay between positive transition of clock and return of input I10, I11 or I12 from Diagnostic Mode (10V).
t_{RJS}	Required delay between inputs I10, I11 or I12 transition to Diagnostic Mode (10V), and when the output pins become available as inputs.
t_{SRD}	Delay between input (I12) transition to Logic mode and when the Outputs reflect the contents of the Output Register.
t_{SRE}	Delay between input I12 transition to Diagnostic Mode and when the Outputs reflect the contents of the State Register.
t_{VS}	Required delay between V_{CC} (after power-on) and negative transition of Clock preceding first reliable clock pulse.
f_{CLK}	Minimum guaranteed clock frequency (register toggle frequency)
f_{MAX}	Minimum guaranteed operating frequency.

TEST LOAD CIRCUITS



NOTE:
C_1 and C_2 are to bypass V_{CC} to GND.

VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

LOGIC PROGRAMMING

PLUS105-55 is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Signetics' SLICE and SNAP design software packages. ABEL™, CUPL™ and PALASM® 90 design software packages also support the PLUS105-55 architecture.

All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

PLUS105-55 logic designs can also be generated using the program table entry format, which is detailed on the following pages. This program table entry format is supported by SNAP and SLICE only. The SLICE design package is available, free of charge, to qualified users.

To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

ABEL is a trademark of Data I/O Corp.
CUPL is a trademark of Logical Devices, Inc.
PALASM is a registered trademark of AMD Corp.

Programmable logic sequencer (16 × 48 × 8)

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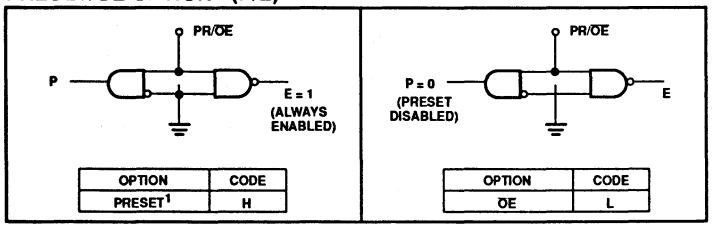
PRESET/OE OPTION - (P/E)

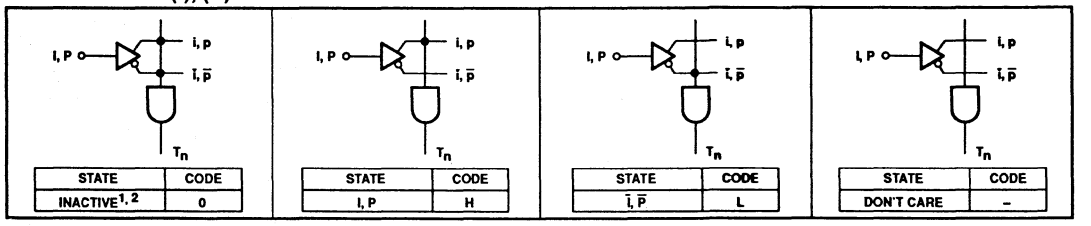


OPTION	CODE
PRESET[1]	H

OPTION	CODE
$\overline{OE}$	L

PROGRAMMING THE PLUS105-55:
The PLUS105-55 has a power-up preset feature. This feature insures that the device will power-up in a known state with all register elements (State and Output Register) at logic High (H). When programming the device it is important to realize this is the initial state of the device. You *must* provide a next state jump if you do not wish to use all Highs (H) as the present state.

"AND" ARRAY - (I), (P)



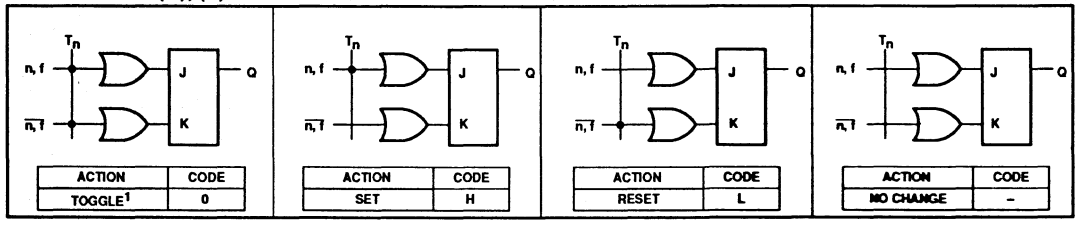
STATE	CODE
INACTIVE[1, 2]	0

STATE	CODE
I, P	H

STATE	CODE
$\overline{i}$, $\overline{p}$	L

STATE	CODE
DON'T CARE	–

"OR" ARRAY - (N), (F)



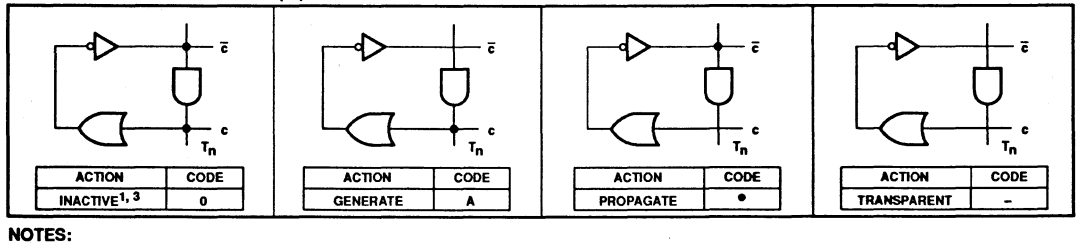
ACTION	CODE
TOGGLE[1]	0

ACTION	CODE
SET	H

ACTION	CODE
RESET	L

ACTION	CODE
NO CHANGE	–

"COMPLEMENT" ARRAY - (C)



ACTION	CODE
INACTIVE[1, 3]	0

ACTION	CODE
GENERATE	A

ACTION	CODE
PROPAGATE	•

ACTION	CODE
TRANSPARENT	–

NOTES:
1. This is the initial unprogrammed state of all link pairs
2. Any gate T_n will be unconditionally inhibited if both the true and complement fuses of any input (I,P) are left intact.
3. To prevent oscillations, this state is not allowed for C link pairs coupled to active gates T_n.

Programmable logic sequencer (16 × 48 × 8)

PLUS105-55

PLUS105 PROGRAM TABLE

CUSTOMER NAME _____

PURCHASE ORDER # _____

SIGNETICS DEVICE # CF (XXXX)

CUSTOMER SYMBOLIZED PART # _____

TOTAL NUMBER OF PARTS _____

PROGRAM TABLE _____

REV _____

DATE _____

PROGRAM TABLE ENTRIES

AND

INACTIVE	0	C_n
GENERATE	A	
PROPAGATE	•	
TRANSPARENT	—	

INACTIVE	0	I_m, P_s
I, P	H	
$\overline{I}$, $\overline{P}$	L	
DON'T CARE	—	

OR

INACTIVE or TOGGLE	0	N_s, F_r
SET	H	
RESET	L	
NO CHANGE	—	

OPTION

PRESET	H	P/E
$\overline{OE}$	L	

	AND																OPTION (P/E) OR																	
TERM	C_n	INPUT (I_m)															PRESENT STATE (P_s)						REMARKS	NEXT STATE (N_s)						OUTPUT (F_r)							
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	5	4	3	2	1	0		5	4	3	2	1	0	7	6	5	4	3	2	1	0
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PIN NO.		20	21	22	23	24	25	26	27	2	3	4	5	6	7	8	9														10	11	12	13	15	16	17	18
VARIABLE NAME																																					

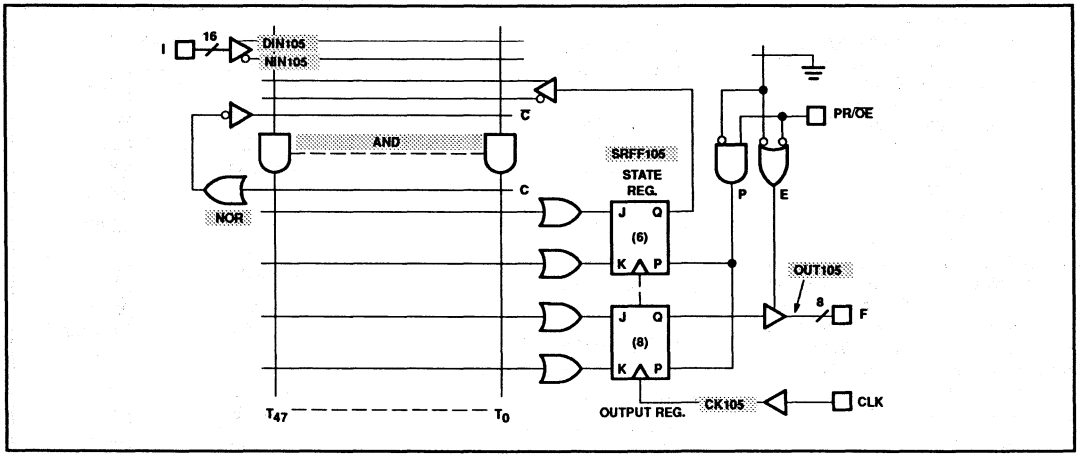
NOTES:

1. The device is shipped with all links initially intact. Thus, a background of "0" for all Terms, and an "H" for the P/E option, exists in the table, shown BLANK instead for clarity.
2. Unused C_n, I_m, and P_s bits are normally programmed Don't Care (–).
3. Unused Transition Terms can be left blank for future code modification, or programmed as (–) for maximum speed.
4. Letters in variable fields are used as identifiers by logic type programmers.

Programmable logic sequencer (16 × 48 × 8)

PLUS105-55

SNAP RESOURCE SUMMARY DESIGNATIONS



Programmable logic sequencers (16 × 64 × 8)

PLUS405-37/-45

DESCRIPTION

The PLUS405 devices are bipolar, programmable state machines of the Mealy type. Both the AND and the OR array are user-programmable. All 64 AND gates are connected to the 16 external dedicated inputs (I0 - I15) and to the feedback paths of the 8 on-chip State Registers (Q_{P0} - Q_{P7}). Two complement arrays support complex IF-THEN-ELSE state transitions with a single product term (input variables C0, C1).

All state transition terms can include True, False and Don't Care states of the controlling state variables. All AND gates are merged into the programmable OR array to issue the next-state and next-output commands to their respective registers. Because the OR array is programmable, any one or all of the 64 transition terms can be connected to any or all of the State and Output Registers.

All state (Q_{P0} - Q_{P7}) and output (Q_{F0} - Q_{F7}) registers are edge-triggered, clocked J-K flip-flops, with Asynchronous Preset and Reset options. The PLUS405 architecture provides the added flexibility of the J-K toggle function which is indeterminate on S-R flip-flops. Each register may be individually programmed such that a specific Preset-Reset pattern is initialized when the initialization pin is raised to a logic level "1". This feature allows the state machine to be asynchronously initialized to known internal state and output conditions, prior to proceeding through a sequence of state transitions. Upon power-up, all registers are unconditionally preset to "1". If desired, the initialization input pin (INIT) can be converted to an $\overline{\text{Output Enable}}$ ($\overline{\text{OE}}$) function as an additional user-programmable feature.

Availability of two user-programmable clocks allows the user to design two independently clocked state machine functions consisting of four state and four output bits each.

Order codes are listed in the Ordering Information Table.

FEATURES

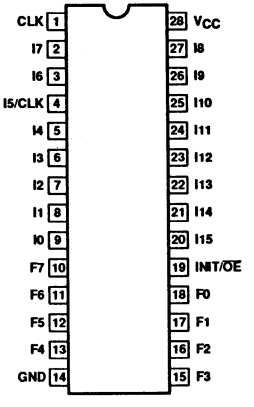
- PLUS405-37
  - f_{MAX} = 37MHz
  - 50MHz clock rate
- PLUS405-45
  - f_{MAX} = 45MHz
  - 58.8MHz clock rate
- Functional superset of PLS105/105A
- Field-programmable (Ti-W fusible link)
- 16 input variables
- 8 output functions
- 64 transition terms
- 8-bit State Register
- 8-bit Output Register
- 2 transition Complement Arrays
- Multiple clocks*
- Programmable Asynchronous Initialization or $\overline{\text{Output Enable}}$
- Power-on preset of all registers to "1"
- "On-chip" diagnostic test mode features for access to state and output registers
- 950mW power dissipation (typ.)
- TTL compatible
- J-K or S-R flip-flop functions
- Automatic "Hold" states
- 3-State outputs

APPLICATIONS

- Interface protocols
- Sequence detectors
- Peripheral controllers
- Timing generators
- Sequential circuits
- Elevator contollers
- Security locking systems
- Counters
- Shift registers

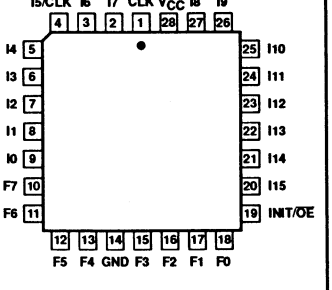
PIN CONFIGURATIONS

N Package



N = Plastic DIP (600mil-wide)

A Package



A = Plastic Leaded Chip Carrier

ORDERING INFORMATION

DESCRIPTION	OPERATING FREQUENCY	ORDER CODE
28-Pin Plastic DIP (600mil-wide)	45MHz (t_{IS1} + t_{CKO1})	PLUS405–45N
28-Pin Plastic DIP (600mil-wide)	37MHz (t_{IS1} + t_{CKO1})	PLUS405–37N
28-Pin Plastic Leaded Chip Carrier	45MHz (t_{IS1} + t_{CKO1})	PLUS405–45A
28-Pin Plastic Leaded Chip Carrier	37MHz (t_{IS1} + t_{CKO1})	PLUS405–37A

*Refer to AC Specifications for clock and operating frequencies when using multiple clocks.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION	POLARITY
1	CLK1	**Clock:** The Clock input to the State and Output Registers. A Low-to-High transition on this line is necessary to update the contents of both state and output registers. Pin 1 only clocks P0–3 and F0–3 if Pin 4 is also being used as a clock.	Active-High (H)
2, 3, 5–9, 26–27 20–22	I0–I4, I7, I6 I8–I9 I13–I15	**Logic Inputs:** The 12 external inputs to the AND array used to program jump conditions between machine states, as determined by a given logic sequence. True and complement signals are generated via use of "H" and "L".	Active-High/Low (H/L)
4	CLK2	**Logic Input/Clock:** A user programmable function:	
		• **Logic Input:** A 13th external logic input to the AND array, as above.	Active-High/Low (H/L)
		• **Clock:** A 2nd clock for the State Registers P4–7 and Output Registers F4–7, as above. Note that input buffer I_5 must be deleted from the AND array (i.e., all fuse locations "Don't Care") when using Pin 4 as a Clock.	Active-High (H)
23	I12	**Logic/Diagnostic Input:** A 14th external logic input to the AND array, as above, when exercising standard TTL or CMOS levels. When I12 is held at +10V, device outputs F0–F7 reflect the contents of State Register bits P0–P7. The contents of each Output Register remains unaltered.	Active-High/Low (H/L)
24	I11	**Logic/Diagnostic Input:** A 15th external logic input to the AND array, as above, when exercising standard TTL levels. When I11 is held at +10V, device outputs F0–F7 become direct inputs for State Register bits P0–P7; a Low-to-High transition on the appropriate clock line loads the values on pins F0–F7 into the State Register bits P0–P7. The contents of each Output Register remains unaltered.	Active-High/Low (H/L)
25	I10	**Logic/Diagnostic Input:** A 16th external logic input to the AND array, as above, when exercising standard TTL levels. When I_{10} is held at +10V, device outputs F0–F7 become direct inputs for Output Register bits Q0–Q7; a Low-to-High transition on the appropriate clock line loads the values on pins F0–F7 into the Output Register bits Q0–Q7. The contents of each State Register remains unaltered.	Active-High/Low (H/L)
10–13 15–18	F0 – F7	**Logic Outputs/Diagnostic Outputs/Diagnostic Inputs:** Eight device outputs which normally reflect the contents of Output Register Bits Q0–Q7, when enabled. When I12 is held at +10V, F0–F7 = (P0–P7). When I11 is held at +10V, F0–F7 become inputs to State Register bits P0–P7. When I10 is held at +10V, F0–F7 become inputs to Output Register bits Q0–Q7.	Active-High (H)
19	INIT/$\overline{OE}$	**Initialization or $\overline{\text{Output Enable}}$ Input:** A user programmable function:	
		• **Initialization:** Provides an asynchronous preset to logic "1" or reset to logic "0" of all State and Output Register bits, determined individually for each register bit through user programming. INIT overrides Clock, and when held High, clocking is inhibited and F0–F7 and P0–P7 are in their initialization state. Normal clocking resumes with the first full clock pulse following a High-to-Low clock transition, after INIT goes Low. See timing definition for t_{NVCK} and t_{VCK}.	Active-High (H)
		• **$\overline{\text{Output Enable}}$:** Provides an output enable function to buffers F0–F7 from the Output Registers.	Active-Low (L)

Programmable logic sequencers (16 × 64 × 8)

PLUS405-37/-45

TRUTH TABLE [1, 2, 3, 4, 5, 6, 7]

V_{CC}	OPTION										
	INIT	$\overline{OE}$	I10	I11	I12	CK	J	K	Q_P	Q_F	F
	H		*	*	*	X	X	X	H/L	H/L	Q_F
	L		+10V	X	X	↑	X	X	Q_P	L	L
	L		+10V	X	X	↑	X	X	Q_P	H	H
	L		X	+10V	X	↑	X	X	L	Q_F	L
	L		X	+10V	X	↑	X	X	H	Q_F	H
	L		X	X	+10V	X	X	X	Q_P	Q_F	Q_P
	L		X	X	X	X	X	X	Q_P	Q_F	Q_F
		H	X	X	*	X	X	X	Q_P	Q_F	Hi-Z
+5V		X	+10V	X	X	↑	X	X	Q_P	L	L
		X	+10V	X	X	↑	X	X	Q_P	H	H
		X	X	+10V	X	↑	X	X	L	Q_F	L
		X	X	+10V	X	↑	X	X	H	Q_F	H
		L	X	X	+10V	X	X	X	Q_P	Q_F	Q_P
		L	X	X	X	X	X	X	Q_P	Q_F	Q_F
		L	X	X	X	↑	L	L	Q_P	Q_F	Q_F
		L	X	X	X	↑	L	H	L	L	L
		L	X	X	X	↑	H	L	H	H	H
		L	X	X	X	↑	H	H	$\overline{Q_P}$	$\overline{Q_F}$	$\overline{Q_F}$
↑	X	X	X	X	X	X	X	X	H	H	

NOTES:

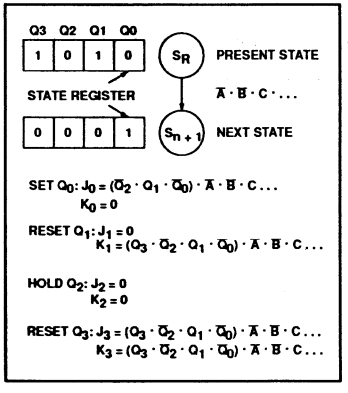
1. Positive Logic:
   S/R (or J/K) = $T_0 + T_1 + T_2 + \ldots T_{63}$
   T_n = (C0, C1) (I0, I1, I2, . . .) (P0, P1, ... P7)
2. Either Initialization (Active-High) or Output Enable (Active-Low) are available, but not both. The desired function is a user-programmable option.
3. ↑ denotes transition from Low-to-High level.
4. * = H or L or +10V
5. X = Don't Care (≤5.5V)
6. H/L implies that either a High or a Low can occur, depending upon user-programmed selection (each State and Output Register individually programmable).
7. When using the F_n pins as inputs to the State and Output Registers in diagnostic mode, the F buffers are 3-Stated and the indicated levels on the output pins are forced by the user.

VIRGIN STATE

A factory-shipped virgin device contains all fusible links intact, such that:

1. INIT/$\overline{OE}$ is set to INIT. In order to use the INIT function, the user must select either the PRESET or the RESET option for each flip-flop. Note that regardless of the user-programmed initialization, or even if the INIT function is not used, all registers are preset to "1" by the power-up procedure.
2. All transition terms are inactive (0).
3. All S/R (or J/K) flip-flop inputs are disabled (0).
4. The device can be clocked via a Test Array preprogrammed with a standard test pattern.
5. Clock 2 is inactive.

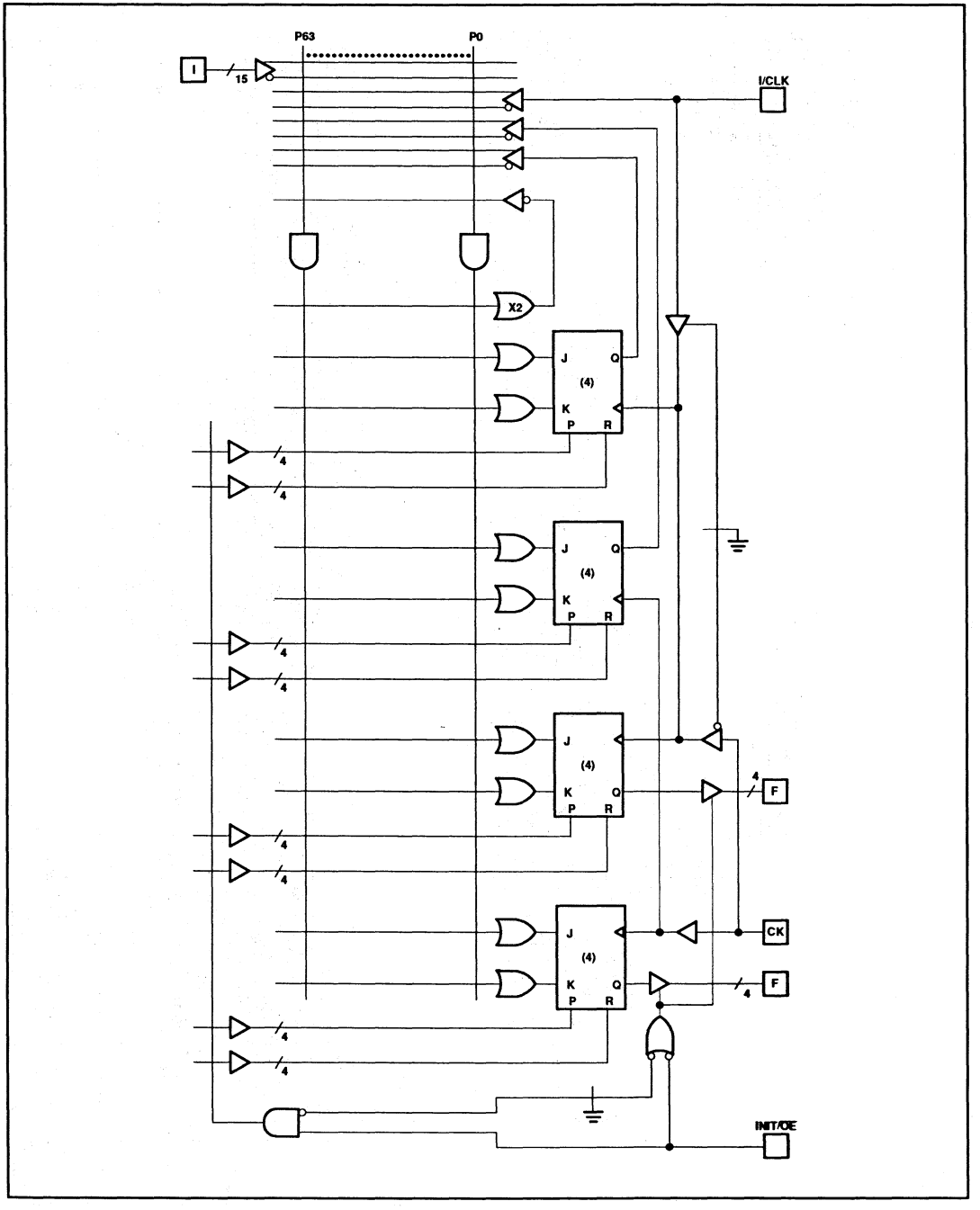
LOGIC FUNCTION



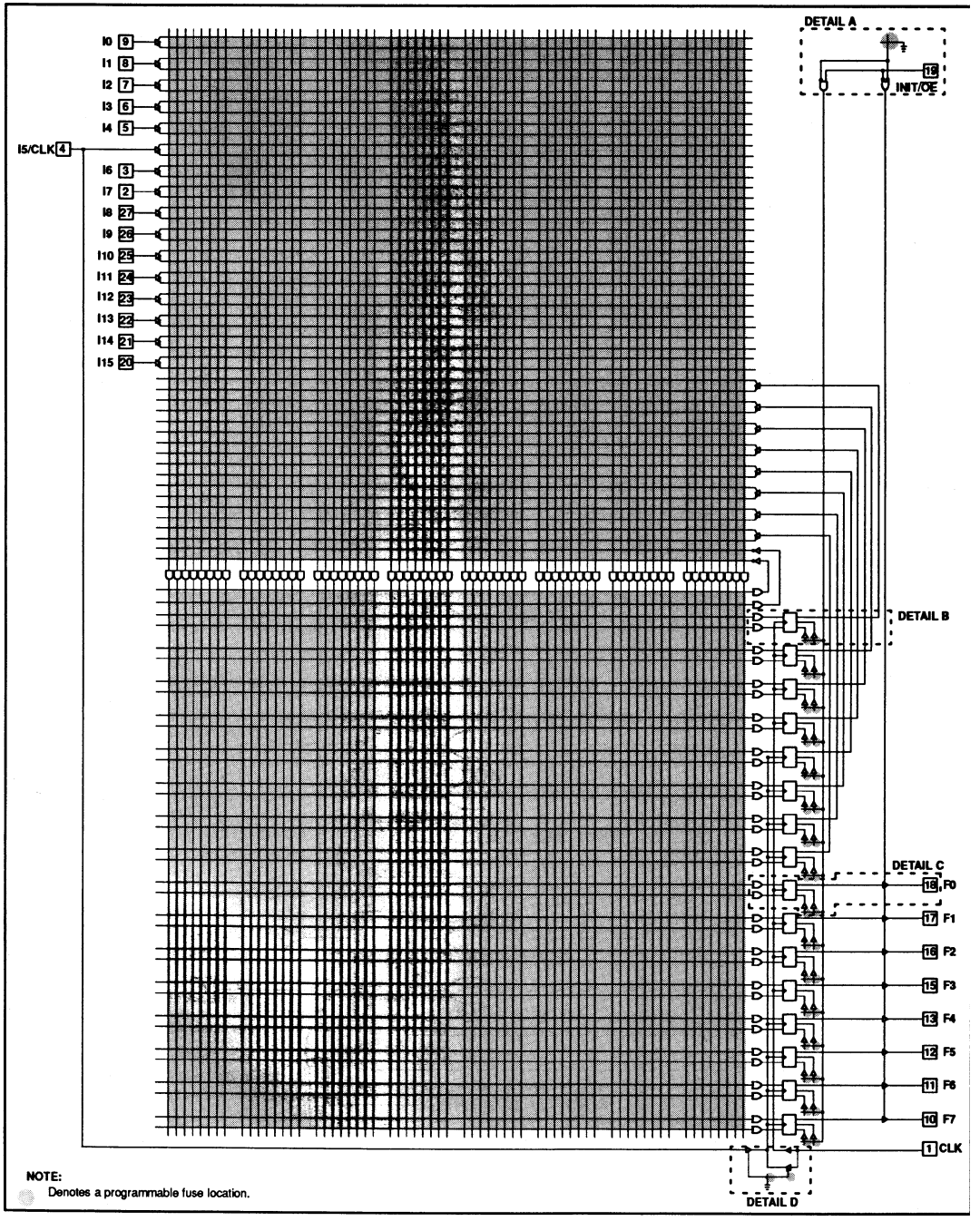
Programmable logic sequencers (16 × 64 × 8)

PLUS405-37/-45

FUNCTIONAL DIAGRAM



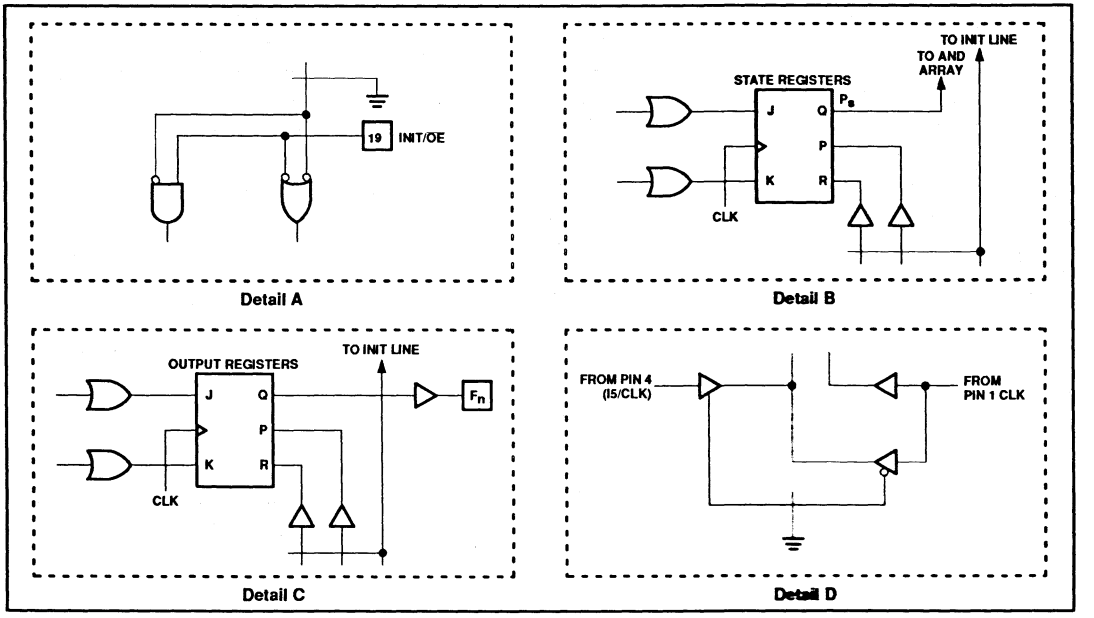
LOGIC DIAGRAM



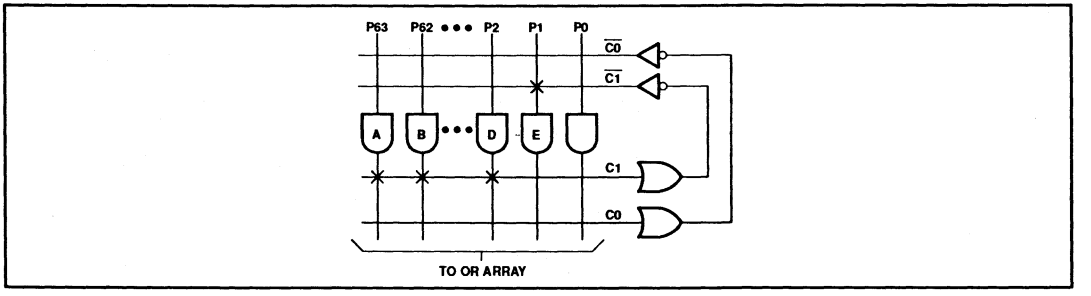
Programmable logic sequencers (16 × 64 × 8)

PLUS405-37/-45

DETAILS FOR REGISTERS FOR PLUS405



COMPLEMENT ARRAY DETAIL



The Complement Array is a special sequencer feature that is often used for detecting illegal states. It is also ideal for generating IF-THEN-ELSE logic statements with a minimum number of product terms.

The concept is deceptively simple. If you subscribe to the theory that the expressions (/A • /B • /C) and $(\overline{A + B + C})$ are equivalent, you will begin to see the value of this single term NOR array.

The Complement Array is a single OR gate with inputs from the AND array. The output of the Complement Array is inverted and fed back to the AND array (NOR). The output of the array will be Low if any one or more of the AND terms connected to it are active (High). If, however, all the connected terms are inactive (Low), which is a classic unknown state, the output of the Complement Array will be High.

Consider the Product Terms A, B and D that represent defined states. They are also connected to the input of the Complement Array. When the condition (not A and not B and not D) exists, the Complement Array will detect this and propagate an Active-High signal to the AND array. This signal can be connected to Product Term E, which could be used in turn to reset the state machine to a known state. Without the Complement Array, one would have to generate product terms for all unknown or illegal states. With very complex state machines, this approach can be prohibitive, both in terms of time and wasted resources.

Note that the PLUS405 has 2 Complement Arrays which allow the user to design 2 independent Complement functions. This is particularly useful if 2 independent state machines have been implemented on one device.

Note that use of the Complement Array adds an additional delay path through the device. Please refer to the AC Electrical Characteristics for details.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_{OUT}	Output voltage	+5.5	V_{DC}
I_{IN}	Input currents	–30 to +30	mA
I_{OUT}	Output currents	+100	mA
T_{amb}	Operating temperature range	0 to +75	°C
T_{Sstg}	Storage temperature range	–65 to +150	°C

NOTES:
1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

DC ELECTRICAL CHARACTERISTICS

$0°C \le T_{amb} \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[1]	MAX	
Input voltage[2]						
V_{IH}	High	V_{CC} = MAX	2.0			V
V_{IL}	Low	V_{CC} = MIN			0.8	V
V_{IC}	Clamp[3]	V_{CC} = MIN, I_{IN} = –12mA		–0.8	–1.2	V
Output voltage[2]						
V_{OH}	High	V_{CC} = MIN, I_{OH} = –2mA	2.4			V
V_{OL}	Low	V_{CC} = MIN, I_{OL} = 9.6mA		0.35	0.45	V
Input current						
I_{IH}	High	V_{CC} = MAX, V_{IN} = V_{CC}		<1	30	µA
I_{IL}	Low	V_{CC} = MAX, V_{IN} = 0.45V		–20	–250	µA
Output current						
$I_{O(OFF)}$	Hi-Z state	V_{CC} = MAX, V_{OUT} = 2.7V		1	40	µA
		V_{CC} = MAX, V_{OUT} = 0.45V		–1	–40	µA
I_{OS}	Short circuit[3, 4]	V_{OUT} = 0V	–15		–70	mA
I_{CC}	V_{CC} supply current[5]	V_{CC} = MAX		190	225	mA
Capacitance						
C_{IN}	Input	V_{CC} = 5.0V, V_{IN} = 2.0V		8		pF
C_{OUT}	Output	V_{CC} = 5.0V, V_{OUT} = 2.0V		10		pF

NOTES:
1. All typical values are at V_{CC} = 5V. T_{amb} = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Test one at a time.
4. Duration of short-circuit should not exceed one second.
5. I_{CC} is measured with the INIT/$\overline{OE}$ input grounded, all other inputs at 4.5V and the outputs open.

AC ELECTRICAL CHARACTERISTICS

$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0°C \leq T_{amb} \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	FROM	TO	LIMITS						UNIT
				PLUS405-37			PLUS405-45			
				MIN	TYP[1]	MAX	MIN	TYP[1]	MAX	
Pulse width										
t_{CKH1}	Clock High; CLK1 (Pin 1)	CK+	CK–	10	8		8.5	7		ns
t_{CKL1}	Clock Low; CLK1 (Pin 1)	CK–	CK+	10	8		8.5	7		ns
t_{CKP1}	CLK1 Period	CK+	CK+	20	16		17	14		ns
t_{CKH2}	Clock High; CLK2 (Pin 4)	CK+	CK–	10	8		10	8		ns
t_{CKL2}	Clock Low; CLK2 (Pin 4)	CK–	CK+	10	8		10	8		ns
t_{CKP2}	CLK2 Period	CK+	CK+	20	16		20	16		ns
t_{INITH}	Initialization pulse	INIT–	INIT+	15	10		15	8		ns
Setup time										
t_{IS1}	Input	Input ±	CK+	15	12		12	10		ns
t_{IS2}	Input (through Complement Array)	Input ±	CK+	25	20		22	18		ns
t_{VS}	Power-on preset	V_{CC}+	CK–	0	–10		0	–10		ns
t_{VCK}	Clock resume (after Initialization)	INIT–	CK–	0	–5		0	–5		ns
t_{NVCK}	Clock lockout (before Initialization)	CK–	INIT–	15	5		15	5		ns
Hold time										
t_{IH}	Input	CK+	Input ±	0	–5		0	–5		ns
Propagation delay										
t_{CKO1}	Clock1 (Pin 1)	CK1+	Output ±		10	12		8	10	ns
t_{CKO2}	Clock2 (Pin 4)	CK2+	Output ±		12	15		10	12	ns
t_{OE}[2]	Output Enable	OE–	Output –		12	15		12	15	ns
t_{OD}[2]	Output Disable	OE+	Output +		12	15		12	15	ns
t_{INIT}	Initialization	INIT+	Output +		15	20		15	20	ns
t_{PPR}	Power-on Preset	V_{CC} +	Output +		0	10		0	10	ns

Notes on following page

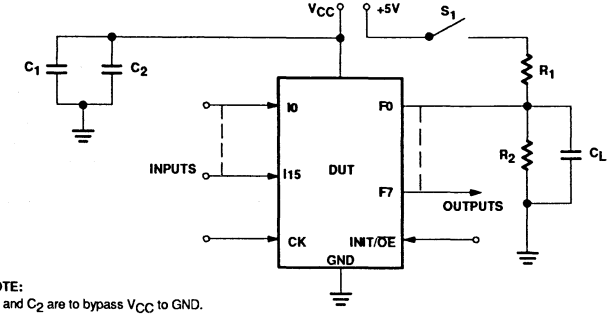
AC ELECTRICAL CHARACTERISTICS (Continued)

$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0°C \le T_{amb} \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

SYMBOL	PARAMETER	FROM	TO	LIMITS						UNIT
				PLUS405-37			PLUS405-45			
				MIN	TYP[1]	MAX	MIN	TYP[1]	MAX	
Frequency of operation										
f_{MAX1}	CLK1; without Complement Array $\left(\frac{1}{t_{IS1} + t_{CKO1}}\right)$	Input ±	Output ±	37.0	45.5		45.5	55.6		MHz
f_{MAX2}	CLK2; without Complement Array $\left(\frac{1}{t_{IS1} + t_{CKO2}}\right)$	Input ±	Output ±	33.0	41.7		41.7	50.0		MHz
f_{MAX3}	CLK1; with Complement Array $\left(\frac{1}{t_{IS2} + t_{CKO1}}\right)$	Input thru Complement Array ±	Output ±	27.0	33.3		31.3	38.5		MHz
f_{MAX4}	CLK2; with Complement Array $\left(\frac{1}{t_{IS2} + t_{CKO2}}\right)$	Input thru Complement Array ±	Output ±	25.0	31.3		29.4	35.7		MHz
f_{MAX5}	Internal feedback without Complement Array (CLK1 or CLK2) $\left(\frac{1}{t_{CKL} + t_{CKH}}\right)$	Register Output ±	Register Intput ±	50.0	62.5		58.8	72.4		MHz
f_{MAX6}	Internal feedback with Complement Array (CLK1 or CLK2) $\left(\frac{1}{t_{IS2}}\right)$	Register Output thru Complement Array ±	Register Intput ±	40.0	50.0		45.5	55.6		MHz
f_{CLK}	Minimum guaranteed clock frequency	CK +	CK +	50.0	62.5		58.8	72.4		MHZ

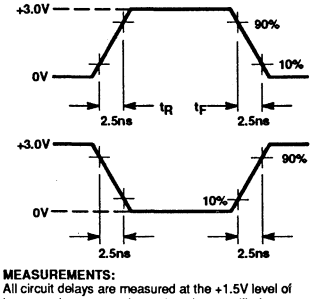
NOTES:
1. All typical values are at $V_{CC} = 5V$, $T_{amb} = +25°C$.
2. For 3-State output; output enable times are tested with $C_L = 30pF$ to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with $C_L = 5pF$. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} - 0.5V)$ with S_1 open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with S_1 closed.
3. All propagation delays and setup times are measured and specified under worst case conditions.

TEST LOAD CIRCUIT



NOTE:
C_1 and C_2 are to bypass V_{CC} to GND.

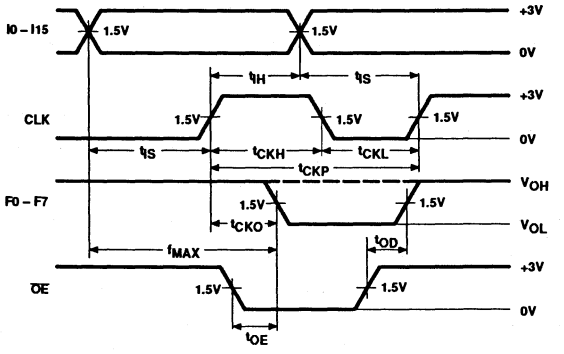
VOLTAGE WAVEFORMS



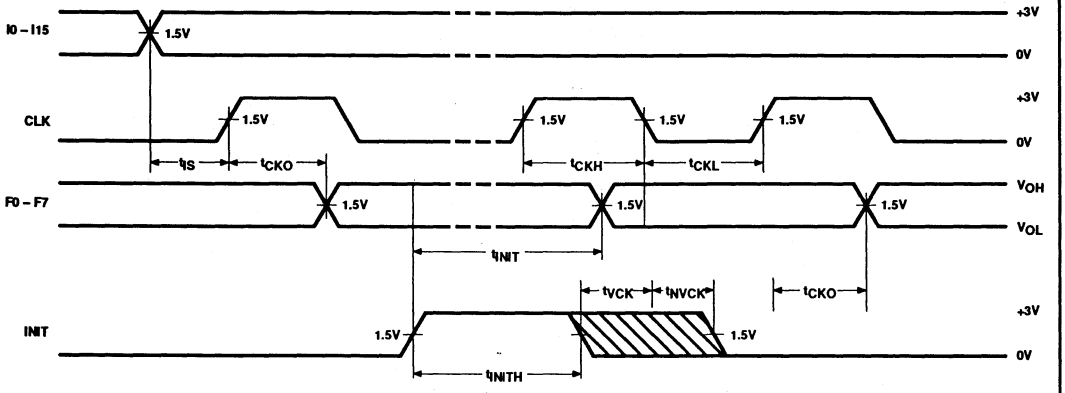
MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

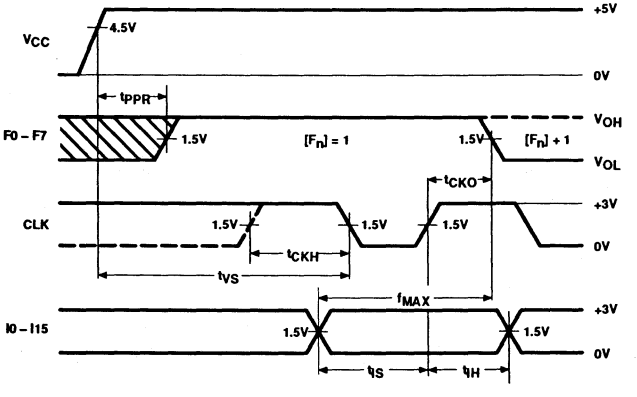
TIMING DIAGRAMS



Sequential Mode

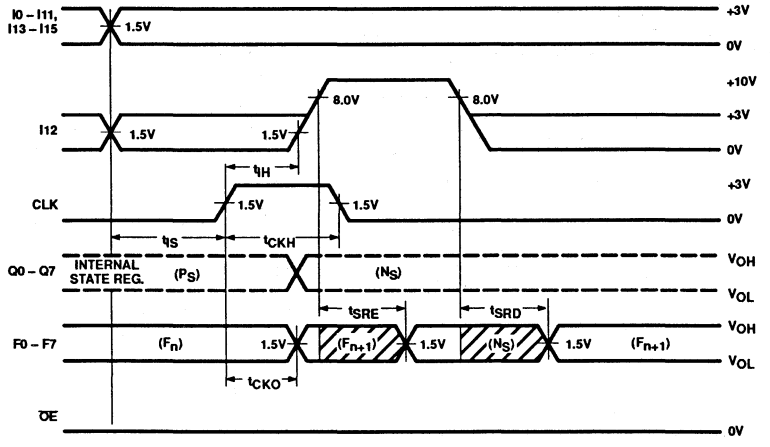


Asynchronous Initialization

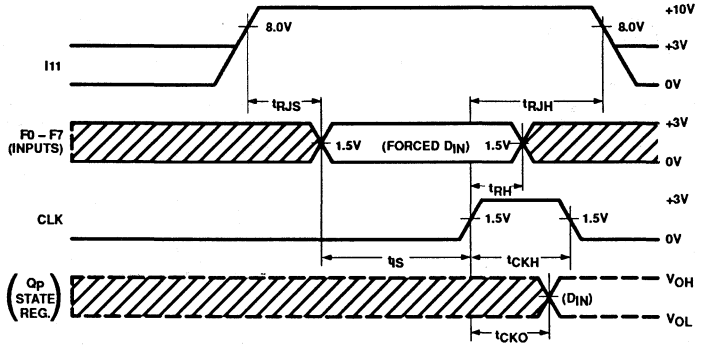


Power-On Preset

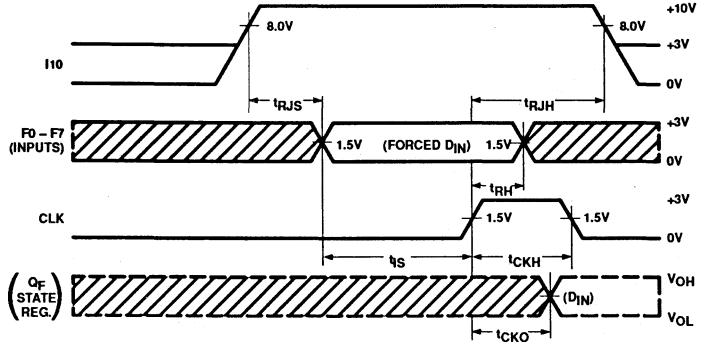
TIMING DIAGRAMS (Continued)



Diagnostic Mode – State Register Outputs



Diagnostic Mode – State Register Input Jam



Diagnostic Mode – Output Register Input Jam

TIMING DEFINITIONS

SYMBOL	PARAMETER
$t_{CKH1,2}$	Width of input clock pulse.
$t_{CKP1,2}$	Minimum guaranteed clock period.
t_{IS1}	Required delay between beginning of valid input and positive transition of Clock.
$t_{CKO1,2}$	Delay between positive transition of Clock and when Outputs become valid (with INIT/$\overline{OE}$ Low).
t_{PPR}	Delay between V_{CC} (after power–on) and when Outputs become preset at "1".
t_{IS2}	Required delay between beginning of valid Input and positive transition of Clock, when using optional Complement Array (two passes necessary through the AND Array).
t_{RJH}	Required delay between positive transition of clock, and return of input I10, I11 or I12 from Diagnostic Mode (10V).
$f_{MAX1,2}$	Minimum guaranteed operating frequency; input to output (CLK1 and CLK2).
$f_{MAX3,4}$	Minimum guaranteed operating frequency; input through Complement Array, to output (CLK1 and CLK2).
f_{MAX5}	Minimum guaranteed internal operating frequency; with internal feedback from state register to state register.

SYMBOL	PARAMETER
f_{MAX6}	Minimum guaranteed internal operating frequency with Complement Array, with internal feedback from state register through Complement Array, to state register.
f_{CLK}	Minimum guaranteed clock frequency (register toggle frequency).
$t_{CKL1,2}$	Interval between clock pulses.
t_{IH}	Required delay between positive transition of Clock and end of valid Input data.
t_{OE}	Delay between beginning of Output Enable Low and when Outputs become valid.
t_{SRE}	Delay between input I12 transition to Diagnostic Mode and when the Outputs reflect the contents of the State Register.
t_{RJS}	Required delay between inputs I11, I10 or I12 transition to Diagnostic Mode (10V), and when the output pins become available as inputs.
t_{NVCK}	Required delay between the negative transition of the clock and the negative transition of the Asynchronous Initialization to guarantee that the clock edge is not detected as a valid negative transition.

SYMBOL	PARAMETER
t_{INITH}	Width of initialization input pulse.
t_{VS}	Required delay between V_{CC} (after power–on) and negative transition of Clock preceding first reliable clock pulse.
t_{OD}	Delay between beginning of Output Enable High and when Outputs are in the OFF–state.
t_{INIT}	Delay between positive transition of Initialization and when Outputs become valid.
t_{SRD}	Delay between input I12 transition to Logic mode and when the Outputs reflect the contents of the Output Register.
t_{RH}	Required delay between positive transition of Clock and end of valid Input data when jamming data into State or Output Registers in diagnostic mode.
t_{VCK}	Required delay between negative transition of Asynchronous Initialization and negative transition of Clock preceding first reliable clock pulse.

Programmable logic sequencers (16 × 64 × 8)

PLUS405-37/-45

LOGIC PROGRAMMING

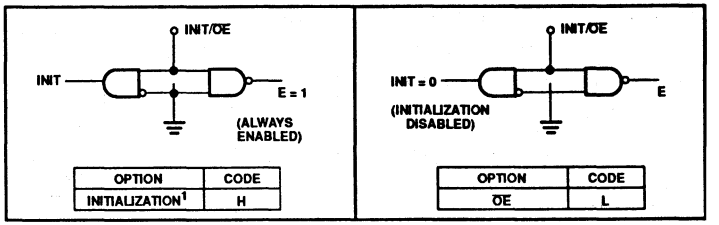
The PLUS405-37/-45 is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Signetics SLICE and SNAP design software packages. ABEL™ and CUPL™ design software packages also support the PLUS405-37/-45 architecture.

All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

PLUS405-37-45 logic designs can also be generated using the program table entry format, which is detailed on the following pages. This program table entry format is supported by SNAP and SLICE only. The SLICE design package is available, free of charge, to qualified users.

To implement the desired logic functions, each logic variable (I, B, P, S, T, etc.) from the logic equations is assigned a symbol. TRUE, COMPLEMENT, PRESET, RESET, OUTPUT ENABLE, INACTIVE, etc., symbols are defined below.

INITIALIZATION/$\overline{OE}$ OPTION – (INIT/$\overline{OE}$)

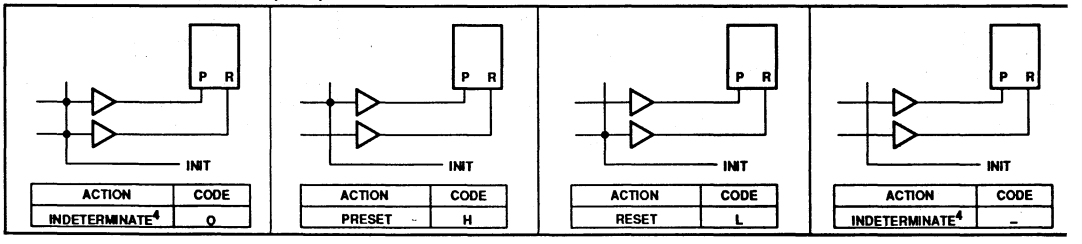


OPTION	CODE
INITIALIZATION[1]	H

OPTION	CODE
$\overline{OE}$	L

PROGRAMMING THE PLUS405:
The PLUS405 has a power-up preset feature. This feature insures that the device will power-up in a known state with all register elements (State and Output Register) at logic High (H). When programming the device it is important to realize this is the initial state of the device. You *must* provide a next state jump if you do not wish to use all Highs (H) as the present state.

INITIALIZATION OPTION – (INIT)



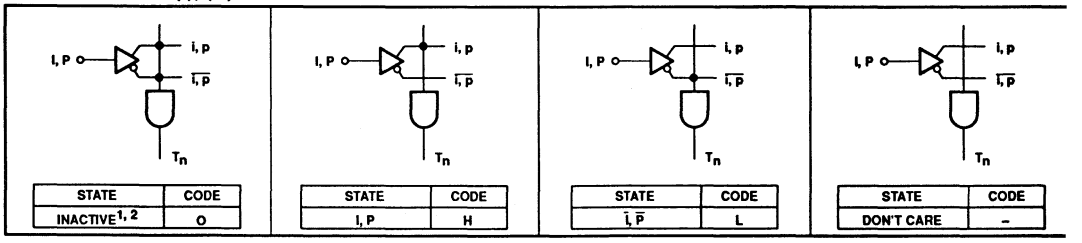
ACTION	CODE
INDETERMINATE[4]	Q

ACTION	CODE
PRESET	H

ACTION	CODE
RESET	L

ACTION	CODE
INDETERMINATE[4]	–

"AND" ARRAY – (I), (P)



STATE	CODE
INACTIVE[1, 2]	Q

STATE	CODE
I, P	H

STATE	CODE
$\overline{i, p}$	L

STATE	CODE
DON'T CARE	–

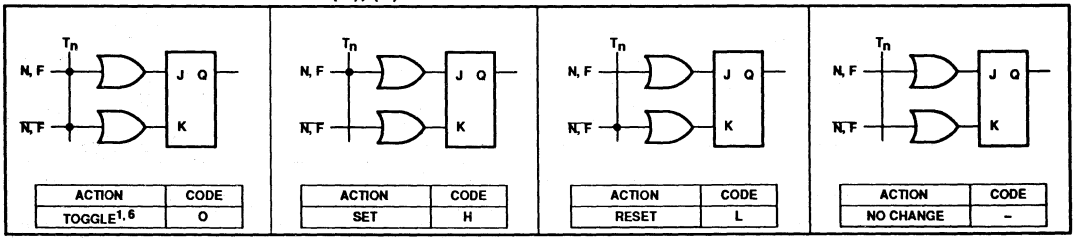
Notes are on next page.

ABEL is a trademark of Data I/O Corp.
CUPL is a trademark of Logical Devices, Inc.

Programmable logic sequencers (16 × 64 × 8)

PLUS405-37/-45

"OR" ARRAY – J-K FUNCTION – (N), (F)



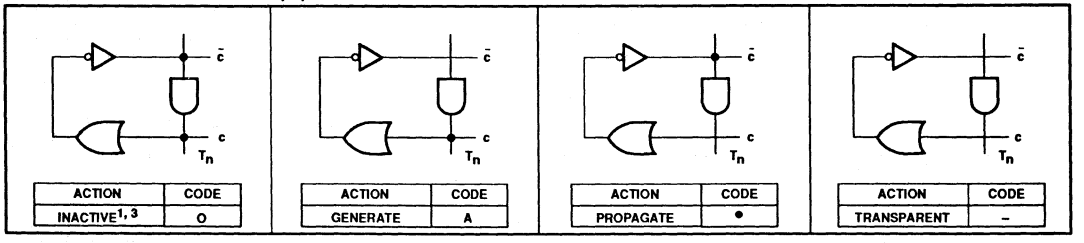
ACTION	CODE
TOGGLE[1, 6]	O

ACTION	CODE
SET	H

ACTION	CODE
RESET	L

ACTION	CODE
NO CHANGE	–

"COMPLEMENT" ARRAY – (C)



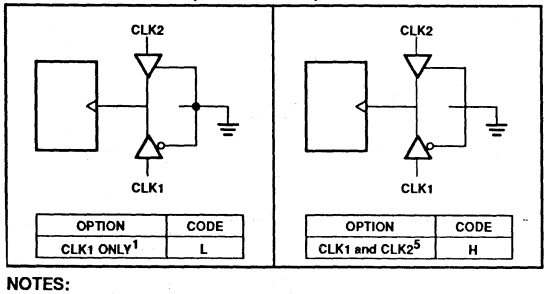
ACTION	CODE
INACTIVE[1, 3]	O

ACTION	CODE
GENERATE	A

ACTION	CODE
PROPAGATE	•

ACTION	CODE
TRANSPARENT	–

CLOCK OPTION – (CLK1/CLK2)



OPTION	CODE
CLK1 ONLY[1]	L

OPTION	CODE
CLK1 and CLK2[5]	H

NOTES:

1. This is the initial unprogrammed state of all links.
2. Any gate T_n will be unconditionally inhibited if any one of its I or P link pairs is left intact.
3. To prevent oscillations, this state is not allowed for C link pairs coupled to active gates T_n.
4. These states are not allowed when using INITIALIZATION option.
5. Input buffer I5 must be deleted from the AND array (i.e., all fuse locations "Don't Care") when using second clock option.
6. A single product term cannot drive more than 8 registers by itself when used in TOGGLE mode.

Programmable logic sequencers (16 × 64 × 8)

PLUS405-37/-45

PLUS405 PROGRAM TABLE

AND						OR			OPTIONS		
INACTIVE	0	Im, Ps	INACTIVE	0	Cn	INACTIVE OR TOGGLE	0	Ns, Fr	INIT	H	INIT/OE
I, P	H		GENERATE	A		SET	H		$\overline{OE}$	L	
$\overline{I}$, $\overline{P}$	L		PROPAGATE	•		RESET	L		CLK1 ONLY	L	CLK1/ CLK2
DON'T CARE	–		TRANSPARENT	–		NO CHANGE	–		CLK1 AND 2	H	

CUSTOMER NAME _____ REV _____ DATE _____

SIGNETICS DEVICE # _____ CF (XXXX) _____ PROGRAM TABLE _____

CUSTOMER SYMBOLIZED PART # _____

	CLOCK 1/2																				INITIALIZATION/OUTPUT ENABLE									
	AND																				OR									
	COMP. ARRAY		INPUT (Im)														PRESENT STATE (Ps)								NEXT STATE (Ns)								OUTPUT (Fr)							
	C1	C0	I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0	P7	P6	P5	P4	P3	P2	P1	P0	N7	N6	N5	N4	N3	N2	N1	N0	F7	F6	F5	F4	F3	F2	F1	F0
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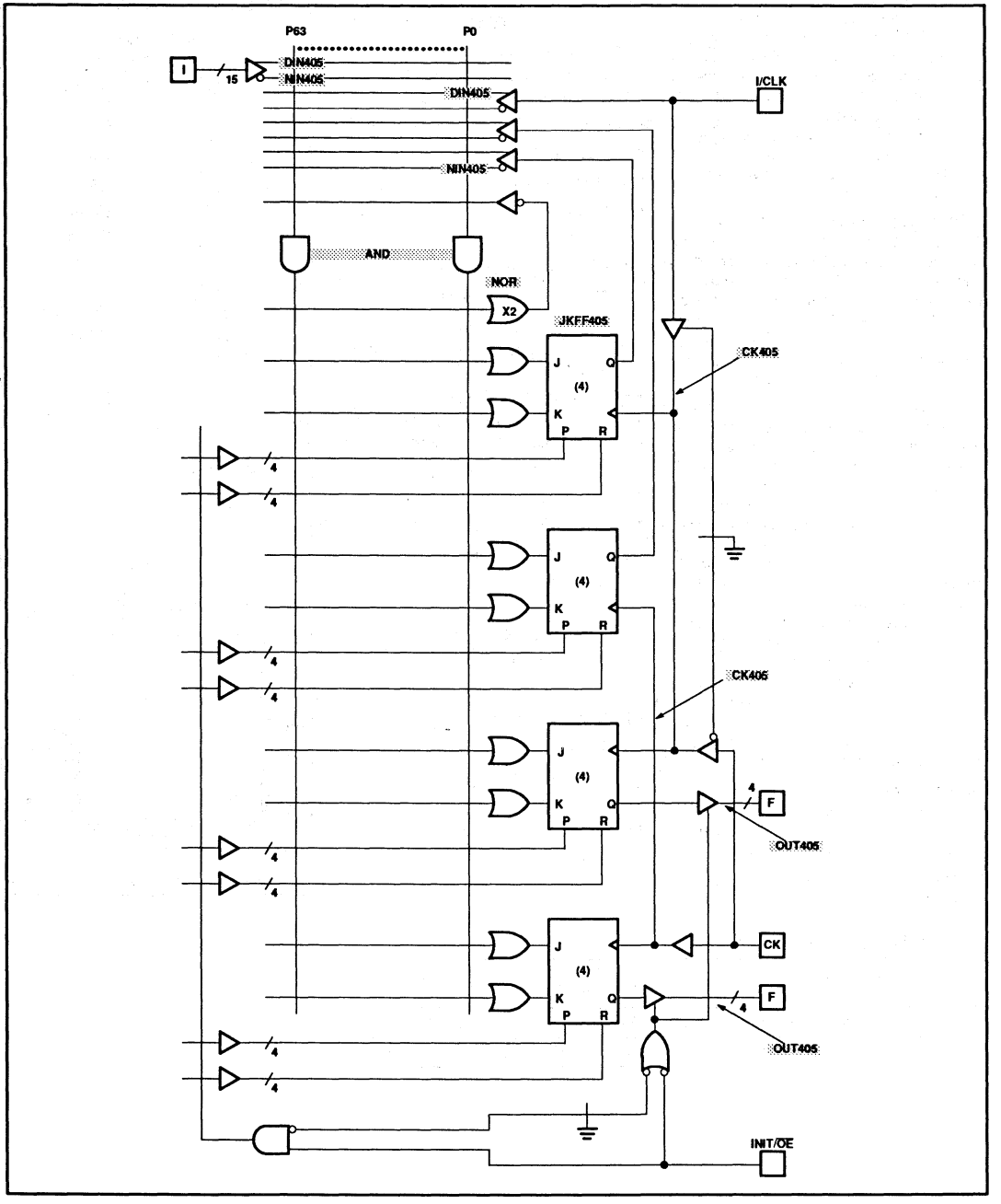
PIN NO.			20	21	22	23	24	25	26	27	2	3	4	5	6	7	8	9																	10	11	12	13	15	16	17	18
PIN LABELS																																									

NOTES:
1. The device is shipped with all links initially intact. Thus, a background of "0" for all Terms, and an "H" for the IN/E and H for the clock option, exists in the table, shown BLANK instead for clarity.
2. Unused Cn Im, and Ps bits are normally programmed Don't Care (—).
3. Unused Transition Terms can be left blank for future code modification, or programmed as (—) for maximum speed.

SNAP RESOURCE SUMMARY DESIGNATIONS



Programmable logic sequencer (16 × 64 × 8)

PLUS405-55

DESCRIPTION

The PLUS405-55 device is a bipolar, programmable state machine of the Mealy type. Both the AND and the OR array are user-programmable. All 64 AND gates are connected to the 16 external dedicated inputs (I0 - I15) and to the feedback paths of the 8 on-chip State Registers (Q_{P0} - Q_{P7}). Two complement arrays support complex IF-THEN-ELSE state transitions with a single product term (input variables C_0, C_1).

All state transition terms can include True, False and Don't Care states of the controlling state variables. All AND gates are merged into the programmable OR array to issue the next-state and next-output commands to their respective registers. Because the OR array is programmable, any one or all of the 64 transition terms can be connected to any or all of the State and Output Registers.

All state (Q_{P0} - Q_{P7}) and output (Q_{F0} - Q_{F7}) registers are edge-triggered, clocked J-K flip-flops, with Asynchronous Preset and Reset options. The PLUS405 architecture provides the added flexibility of the J-K toggle function which is indeterminate on S-R flip-flops. Each register may be individually programmed such that a specific Preset-Reset pattern is initialized when the initialization pin is raised to a logic level "1". This feature allows the state machine to be asynchronously initialized to known internal state and output conditions prior to proceeding through a sequence of state transitions. Upon power-up, all registers are unconditionally preset to "1". If desired, the initialization input pin (INIT) can be converted to an Output Enable ($\overline{OE}$) function as an additional user-programmable feature.

Availability of two user-programmable clocks allows the user to design two independently clocked state machine functions consisting of four state and four output bits each.

Order codes are listed in the Ordering Information Table below.

FEATURES

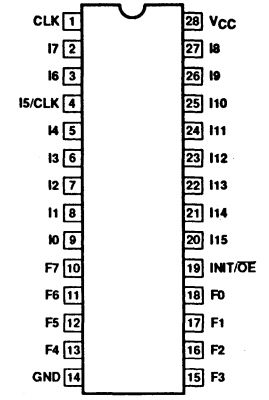
- 66.7MHz minimum guaranteed clock rate
- 55MHz minimum guaranteed operating frequency ($1/(t_{IS1} + t_{CKO1})$)
- Functional superset of PLS105/105A
- Field-programmable (Ti-W fusible link)
- 16 input variables
- 8 output functions
- 64 transition terms
- 8-bit State Register
- 8-bit Output Register
- 2 transition Complement Arrays
- Multiple clocks
- Programmable Asynchronous Initialization or Output Enable
- Power-on preset of all registers to "1"
- "On-chip" diagnostic test mode features for access to state and output registers
- 950mW power dissipation (typ.)
- TTL compatible
- J-K or S-R flip-flop functions
- Automatic "Hold" states
- 3-State outputs

APPLICATIONS

- Interface protocols
- Sequence detectors
- Peripheral controllers
- Timing generators
- Sequential circuits
- Elevator contollers
- Security locking systems
- Counters
- Shift registers

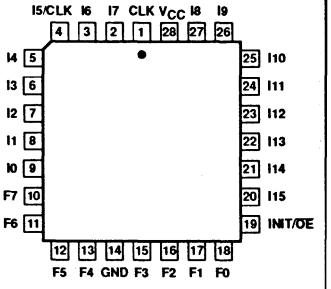
PIN CONFIGURATIONS

N Package



N = Plastic DIP (600mil-wide)

A Package



A = Plastic Leaded Chip Carrier

ORDERING INFORMATION

DESCRIPTION	OPERATING FREQUENCY	ORDER CODE
28-Pin Plastic Dual In-Line (600mil-wide)	55MHz ($t_{IS} + t_{CKO}$)	PLUS405–55N
28-Pin Plastic Leaded Chip Carrier	55MHz ($t_{IS} + t_{CKO}$)	PLUS405–55A

Programmable logic sequencer (16 × 64 × 8)

PLUS405-55

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION	POLARITY
1	CLK1	**Clock:** The Clock input to the State and Output Registers. A Low-to-High transition on this line is necessary to update the contents of both state and output registers. Pin 1 only clocks P0–3 and F0–3 if Pin 4 is also being used as a clock.	Active-High (H)
2, 3, 5–9, 26–27 20–22	I0 – I4, I7, I6 I8 – I9 I13 – I15	**Logic Inputs:** The 12 external inputs to the AND array used to program jump conditions between machine states, as determined by a given logic sequence. True and complement signals are generated via use of "H" and "L".	Active-High/Low (H/L)
4	CLK2	**Logic Input/Clock:** A user programmable function:	
		• **Logic Input:** A 13th external logic input to the AND array, as above.	Active-High/Low (H/L)
		• **Clock:** A 2nd clock for the State Registers P4–7 and Output Registers F4–7, as above. Note that input buffer I5 must be deleted from the AND array (i.e., all fuse locations "Don't Care") when using Pin 4 as a Clock.	Active-High (H)
23	I12	**Logic/Diagnostic Input:** A 14th external logic input to the AND array, as above, when exercising standard TTL or CMOS levels. When I12 is held at +10V, device outputs F0–F7 reflect the contents of State Register bits P0–P7. The contents of each Output Register remains unaltered.	Active-High/Low (H/L)
24	I11	**Logic/Diagnostic Input:** A 15th external logic input to the AND array, as above, when exercising standard TTL levels. When I11 is held at +10V, device outputs F0–F7 become direct inputs for State Register bits P0–P7; a Low-to-High transition on the appropriate clock line loads the values on pins F0–F7 into the State Register bits P0–P7. The contents of each Output Register remains unaltered.	Active-High/Low (H/L)
25	I10	**Logic/Diagnostic Input:** A 16th external logic input to the AND array, as above, when exercising standard TTL levels. When I10 is held at +10V, device outputs F0–F7 become direct inputs for Output Register bits Q0–Q7; a Low-to-High transition on the appropriate clock line loads the values on pins F0–F7 into the Output Register bits Q0–Q7. The contents of each State Register remains unaltered.	Active-High/Low (H/L)
10–13 15–18	F0 – F7	**Logic Outputs/Diagnostic Outputs/Diagnostic Inputs:** Eight device outputs which normally reflect the contents of Output Register Bits Q0–Q7, when enabled. When I12 is held at +10V, F0–F7 = (P0–P7). When I11 is held at +10V, F0–F7 become inputs to State Register bits P0–P7. When I10 is held at +10V, F0–F7 become inputs to Output Register bits Q0–Q7.	Active-High (H)
19	INIT/$\overline{OE}$	**Initialization or Output Enable Input:** A user programmable function:	
		• **Initialization:** Provides an asynchronous preset to logic "1" or reset to logic "0" of all State and Output Register bits, determined individually for each register bit through user programming. INIT overrides Clock, and when held High, clocking is inhibited and F0–F7 and P0–P7 are in their initialization state. Normal clocking resumes with the first full clock pulse following a High-to-Low clock transition, after INIT goes Low. See timing definition for t_{NVCK} and t_{VCK}.	Active-High (H)
		• **Output Enable:** Provides an output enable function to buffers F0–F7 from the Output Registers.	Active-Low (L)

Programmable logic sequencer (16 × 64 × 8)

PLUS405-55

TRUTH TABLE [1, 2, 3, 4, 5, 6, 7]

V_{CC}	OPTION										
	INIT	$\overline{OE}$	I10	I11	I12	CK	J	K	Q_P	Q_F	F
+5V	H		*	*	*	X	X	X	H/L	H/L	Q_F
	L		+10V	X	X	↑	X	X	Q_P	L	L
	L		+10V	X	X	↑	X	X	Q_P	H	H
	L		X	+10V	X	↑	X	X	L	Q_F	L
	L		X	+10V	X	↑	X	X	H	Q_F	H
	L		X	X	+10V	X	X	X	Q_P	Q_F	Q_P
	L		X	X	X	X	X	X	Q_P	Q_F	Q_F
		H	X	X	*	X	X	X	Q_P	Q_F	Hi-Z
		X	+10V	X	X	↑	X	X	Q_P	L	L
		X	+10V	X	X	↑	X	X	Q_P	H	H
		X	X	+10V	X	↑	X	X	L	Q_F	L
		X	X	+10V	X	↑	X	X	H	Q_F	H
		L	X	X	+10V	X	X	X	Q_P	Q_F	Q_P
		L	X	X	X	X	X	X	Q_P	Q_F	Q_F
		L	X	X	X	↑	L	L	Q_P	Q_F	Q_F
		L	X	X	X	↑	L	H	L	L	L
		L	X	X	X	↑	H	L	H	H	H
		L	X	X	X	↑	H	H	$\overline{Q_P}$	$\overline{Q_F}$	$\overline{Q_F}$
↑	X	X	X	X	X	X	X	X	H	H	

NOTES:

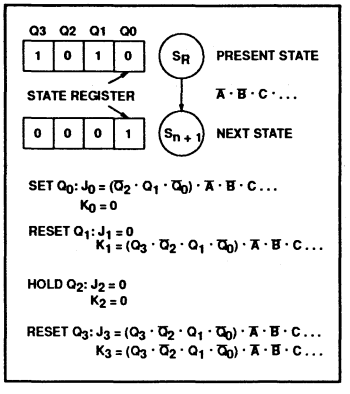
1. Positive Logic:
   S/R (or J/K) = $T_0 + T_1 + T_2 + \ldots T_{63}$
   T_n = (C0, C1) (I0, I1, I2, . . .) (P0, P1, . . . P7)
2. Either Initialization (Active-High) or $\overline{\text{Output Enable}}$ (Active-Low) are available, but not both. The desired function is a user-programmable option.
3. ↑ denotes transition from Low-to-High level.
4. * = H or L or +10V
5. X = Don't Care (≤5.5V)
6. H/L implies that either a High or a Low can occur, depending upon user-programmed selection (each State and Output Register individually programmable).
7. When using the F_n pins as inputs to the State and Output Registers in diagnostic mode, the F buffers are 3-Stated and the indicated levels on the output pins are forced by the user.

VIRGIN STATE

A factory-shipped virgin device contains all fusible links intact, such that:

1. INIT/$\overline{OE}$ is set to INIT. In order to use the INIT function, the user must select either the PRESET or the RESET option for each flip-flop. Note that regardless of the user-programmed initialization, or even if the INIT function is not used, all registers are preset to "1" by the power-up procedure.
2. All transition terms are inactive (0).
3. All S/R (or J/K) flip-flop inputs are disabled (0).
4. The device can be clocked via a Test Array preprogrammed with a standard test pattern.
5. Clock 2 is inactive.

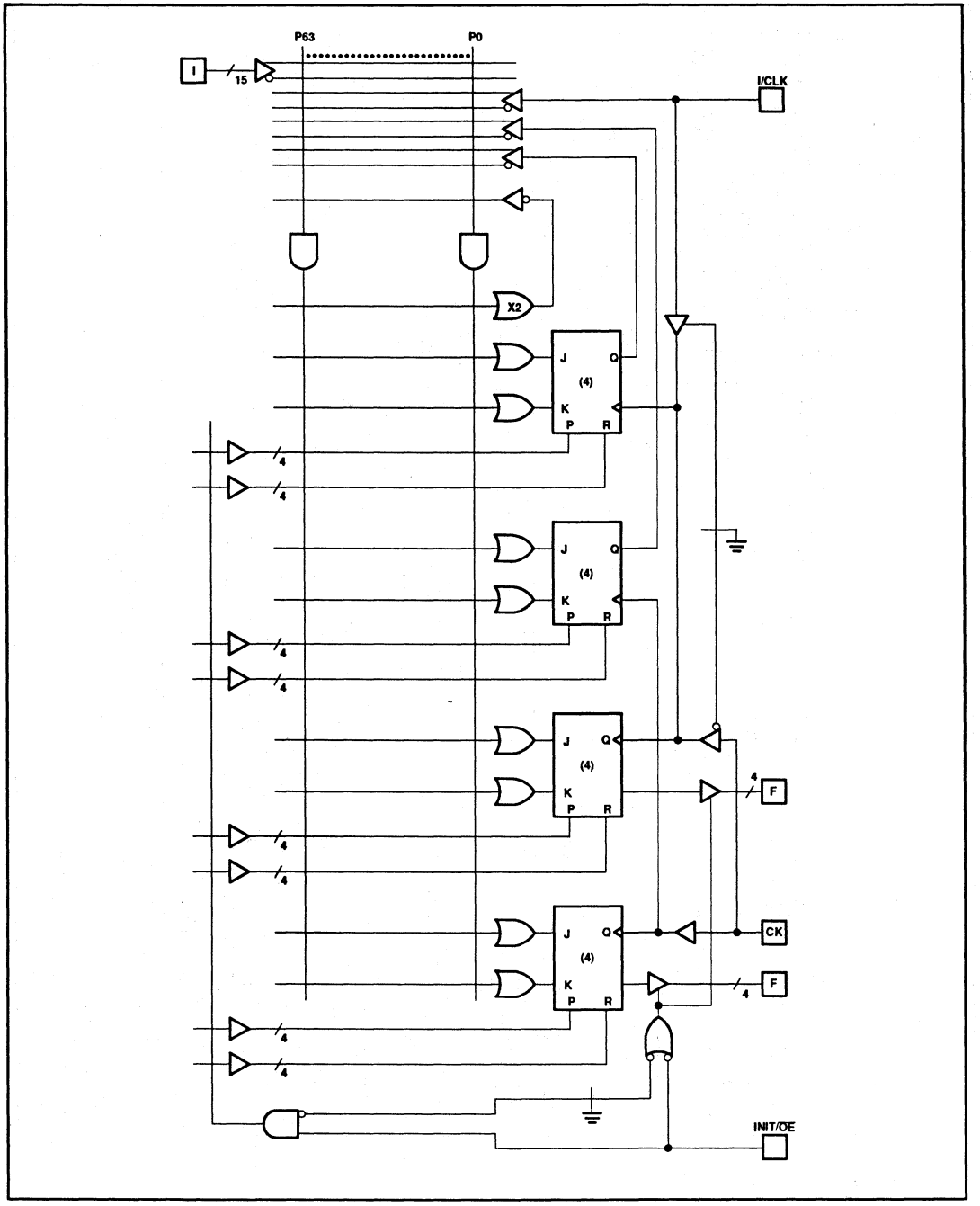
LOGIC FUNCTION



Programmable logic sequencer (16 x 64 x 8)

PLUS405-55

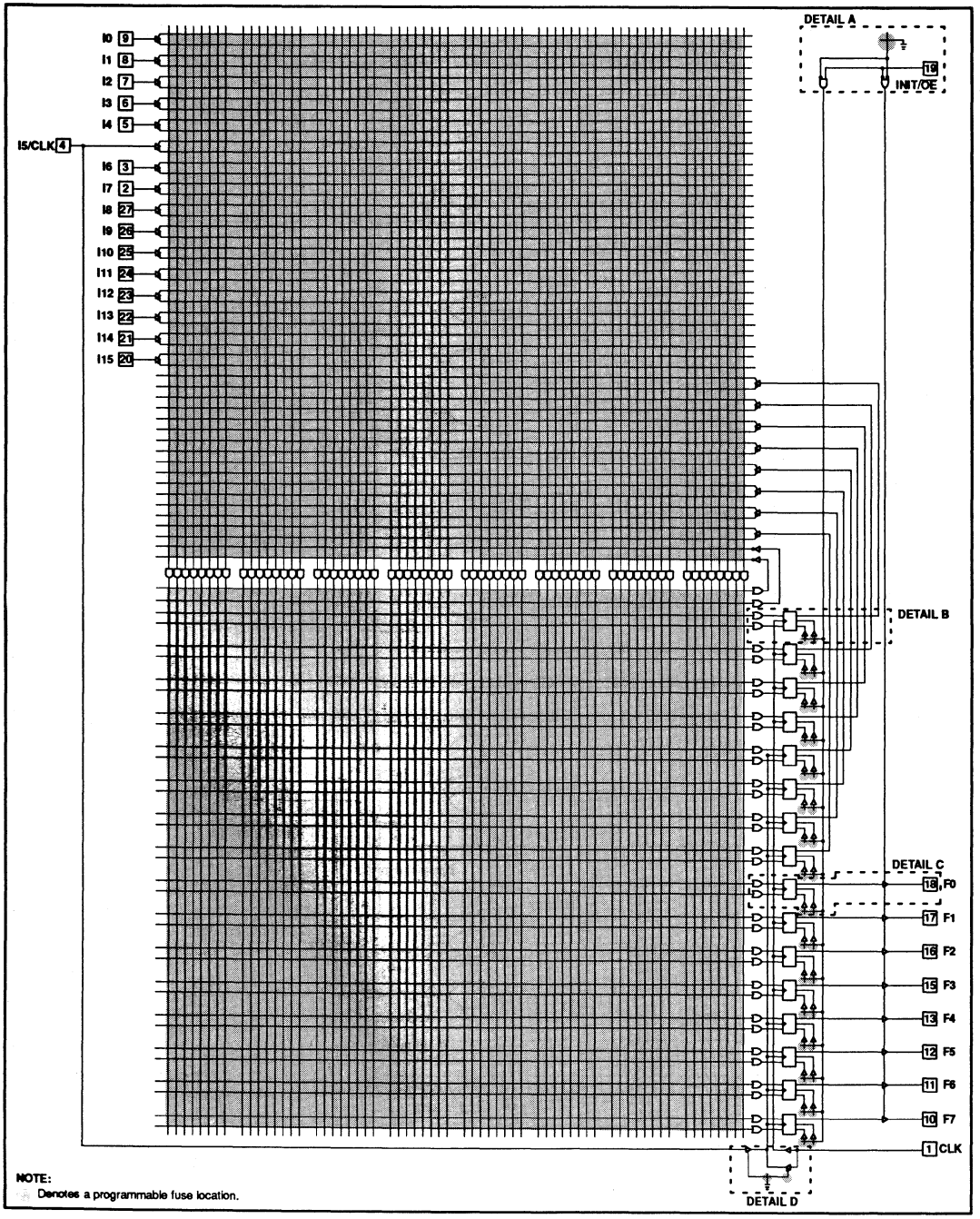
FUNCTIONAL DIAGRAM



Programmable logic sequencer (16 × 64 × 8)

PLUS405-55

LOGIC DIAGRAM



Programmable logic sequencer (16 × 64 × 8)

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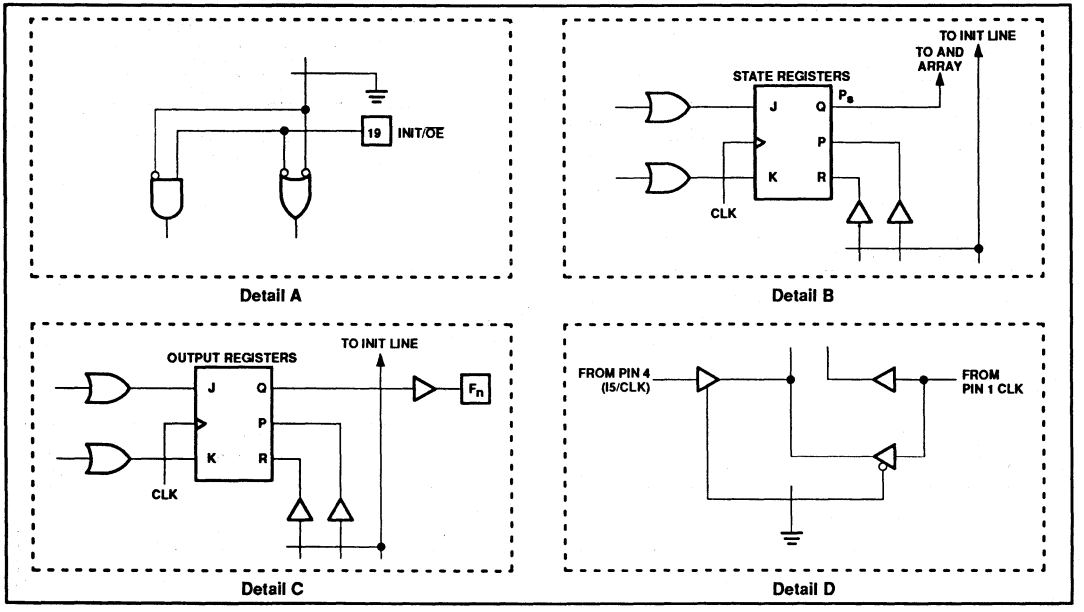
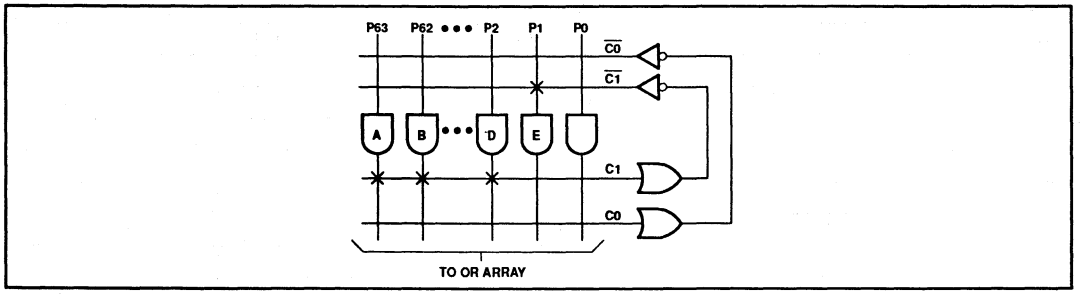
DETAILS FOR REGISTERS FOR PLUS405



COMPLEMENT ARRAY DETAIL



The Complement Array is a special sequencer feature that is often used for detecting illegal states. It is also ideal for generating IF-THEN-ELSE logic statements with a minimum number of product terms.

The concept is deceptively simple. If you subscribe to the theory that the expressions (/A • /B • /C) and ($\overline{A + B + C}$) are equivalent, you will begin to see the value of this single term NOR array.

The Complement Array is a single OR gate with inputs from the AND array. The output of the Complement Array is inverted and fed back to the AND array (NOR). The output of the array will be Low if any one or more of the AND terms connected to it are active (High). If, however, all the connected terms are inactive (Low), which is a classic unknown state, the output of the Complement Array will be High.

Consider the Product Terms A, B and D that represent defined states. They are also connected to the input of the Complement Array. When the condition (not A and not B and not D) exists, the Complement Array will detect this and propagate an Active-High signal to the AND array. This signal can be connected to Product Term E, which could be used in turn to reset the state machine to a known state. Without the Complement Array, one would have to generate product terms for all unknown or illegal states. With very complex state machines, this approach can be prohibitive, both in terms of time and wasted resources.

Note that the PLUS405 sequencers have 2 Complement Arrays which allow the user to design 2 independent Complement functions. This is particularly useful if 2 independent state machines have been implemented on one device.

Note that use of the Complement Array adds an additional delay path through the device. Please refer to the AC Electrical Characteristics for details.

Programmable logic sequencer (16 × 64 × 8)

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ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_{OUT}	Output voltage	+5.5	V_{DC}
I_{IN}	Input currents	–30 to +30	mA
I_{OUT}	Output currents	+100	mA
T_{amb}	Operating temperature range	0 to +75	°C
T_{stg}	Storage temperature range	–65 to +150	°C

NOTES:
1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

DC ELECTRICAL CHARACTERISTICS

$0°C \le T_{amb} \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[1]	MAX	
Input voltage[2]						
V_{IH}	High	V_{CC} = MAX	2.0			V
V_{IL}	Low	V_{CC} = MIN			0.8	V
V_{IC}	Clamp[3]	V_{CC} = MIN, I_{IN} = –12mA		–0.8	–1.2	V
Output voltage[2]						
V_{OH}	High	V_{CC} = MIN, I_{OH} = –2mA	2.4			V
V_{OL}	Low	V_{CC} = MIN, I_{OL} = 9.6mA		0.35	0.45	V
Input current						
I_{IH}	High	V_{CC} = MAX, V_{IN} = V_{CC}		<1	30	µA
I_{IL}	Low	V_{CC} = MAX, V_{IN} = 0.45V		–20	–250	µA
Output current						
$I_{O(OFF)}$	Hi-Z state	V_{CC} = MAX, V_{OUT} = 2.7V		1	40	µA
		V_{CC} = MAX, V_{OUT} = 0.45V		–1	–40	µA
I_{OS}	Short circuit[3, 4]	V_{OUT} = 0V	–15		–70	mA
I_{CC}	V_{CC} supply current[5]	V_{CC} = MAX		190	225	mA
Capacitance						
C_{IN}	Input	V_{CC} = 5.0V, V_{IN} = 2.0V		8		pF
C_{OUT}	Output	V_{CC} = 5.0V, V_{OUT} = 2.0V		10		pF

NOTES:
1. All typical values are at V_{CC} = 5V. T_{amb} = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Test one at a time.
4. Duration of short-circuit should not exceed one second.
5. I_{CC} is measured with the INIT/$\overline{OE}$ input grounded, all other inputs at 4.5V and the outputs open.

AC ELECTRICAL CHARACTERISTICS

$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0°C \leq T_{amb} \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	FROM	TO	LIMITS			UNIT
				MIN	TYP[1]	MAX	
Pulse width							
t_{CKH1}	Clock High; CLK1 (Pin 1)	CK+	CK–	7.5	6		ns
t_{CKL1}	Clock Low; CLK1 (Pin 1)	CK–	CK+	7.5	6		ns
t_{CKP1}	CLK1 Period	CK+	CK+	15	12		ns
t_{CKH2}	Clock High; CLK2 (Pin 4)	CK+	CK–	7.5	6		ns
t_{CKL2}	Clock Low; CLK2 (Pin 4)	CK–	CK+	7.5	6		ns
t_{CKP2}	CLK2 Period	CK +	CK +	15	12		ns
t_{INITH}	Initialization pulse	INIT–	INIT+	14	12		ns
Setup time							
t_{IS1}	Input	Input ±	CK+	10	9		ns
t_{IS2}	Input (through Complement Array)	Input ±	CK+	18	15		ns
t_{VS}	Power-on preset	V_{CC}+	CK–	0	–10		ns
t_{VCK}	Clock resume (after Initialization)	INIT–	CK–	0	–5		ns
t_{NVCK}	Clock lockout (before Initialization)	CK–	INIT–	12	5		ns
Hold time							
t_{IH}	Input	CK+	Input ±	0	–5		ns
Propagation delay							
t_{CKO1}	Clock1 (Pin 1)	CK1+	Output ±		6.5	8	ns
t_{CKO2}	Clock2 (Pin 4)	CK2+	Output ±		7.0	8	ns
t_{OE}[2]	Output Enable	OE–	Output –		6.5	8	ns
t_{OD}[2]	Output Disable	OE+	Output +		6.5	8	ns
t_{INIT}	Initialization	INIT+	Output +		12	18	ns
t_{PPR}	Power-on Preset	V_{CC} +	Output +		0	10	ns

Notes on following page

AC ELECTRICAL CHARACTERISTICS (Continued)

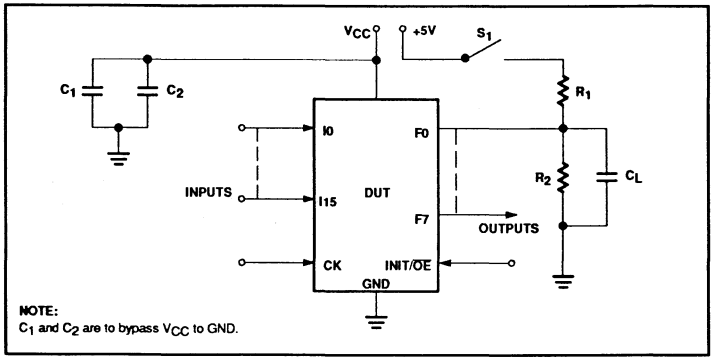
$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0°C \le T_{amb} \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

SYMBOL	PARAMETER	FROM	TO	LIMITS MIN	LIMITS TYP[1]	LIMITS MAX	UNIT
Frequency of operation							
f_{MAX1}	CLK1; (without Complement Array) $\left(\frac{1}{t_{IS1} + t_{CKO1}}\right)$	Input ±	Output ±	55.6	64.5		MHz
f_{MAX2}	CLK2; (without Complement Array) $\left(\frac{1}{t_{IS1} + t_{CKO2}}\right)$	Input ±	Output ±	55.6	62.5		MHz
f_{MAX3}	CLK1; (with Complement Array) $\left(\frac{1}{t_{IS2} + t_{CKO1}}\right)$	Input through Complement Array ±	Output ±	38.5	46.5		MHz
f_{MAX4}	CLK2; (with Complement Array) $\left(\frac{1}{t_{IS2} + t_{CKO2}}\right)$	Input through Complement Array ±	Output ±	38.5	45.5		MHz
f_{MAX5}	Internal feedback without Complement Array (CLK1 or CLK2) $\left(\frac{1}{t_{CKL} + t_{CKH}}\right)$	Register Output ±	Register Input ±	66.7	83.3		MHz
f_{MAX6}	Internal feedback with Complement Array (CLK1 or CLK2) $\left(\frac{1}{t_{IS2}}\right)$	Register Output through Complement Array ±	Register Input ±	55.6	66.7		MHz
f_{CLK}	Minimum guaranteed Clock frequency	CK +	CK +	66.7	83.3		MHz

NOTES:

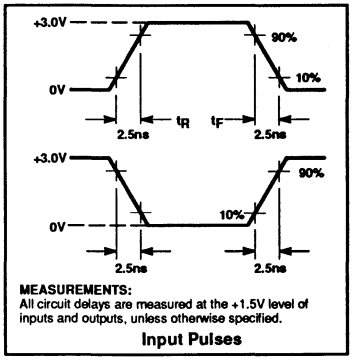
1. All typical values are at $V_{CC} = 5V$, $T_{amb} = +25°C$.
2. For 3-State output; output enable times are tested with $C_L = 30pF$ to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with $C_L = 5pF$. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} - 0.5V)$ with S_1 open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with S_1 closed.
3. All propagation delays and setup times are measured and specified under worst case conditions.

TEST LOAD CIRCUIT



NOTE:
C_1 and C_2 are to bypass V_{CC} to GND.

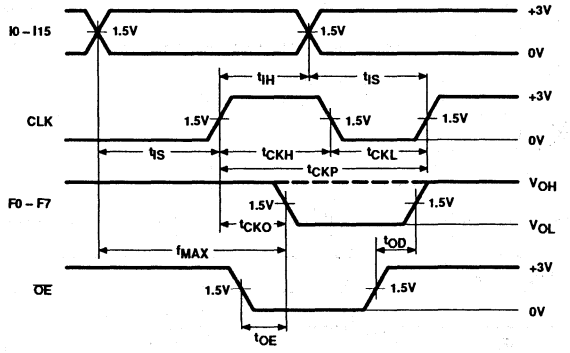
VOLTAGE WAVEFORMS



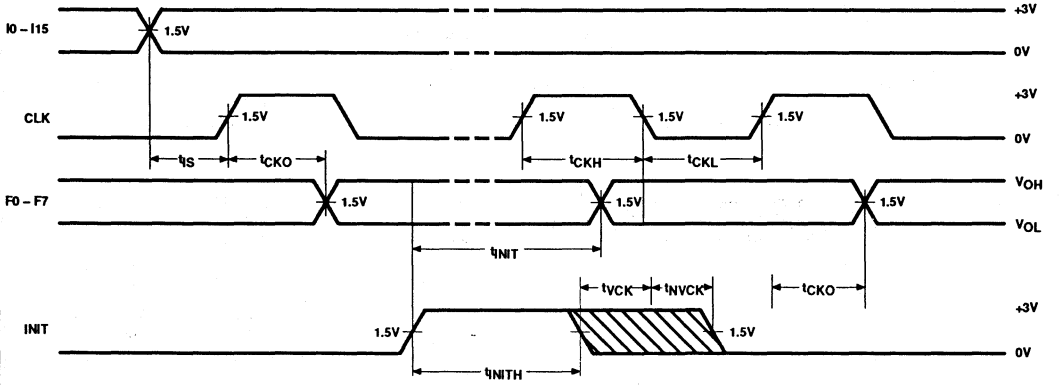
MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

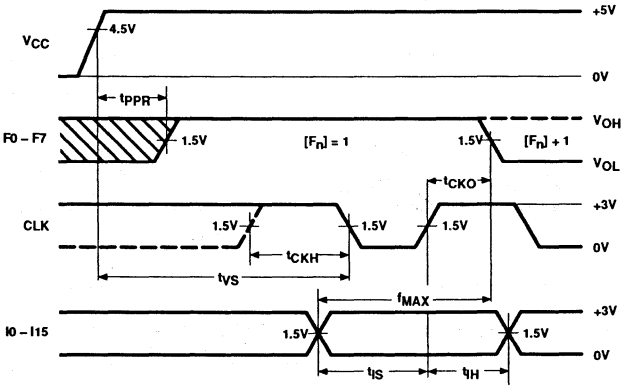
TIMING DIAGRAMS



Sequential Mode

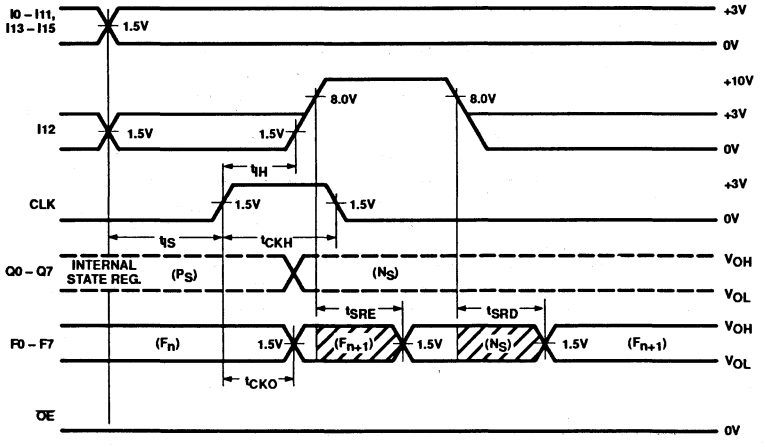


Asynchronous Initialization

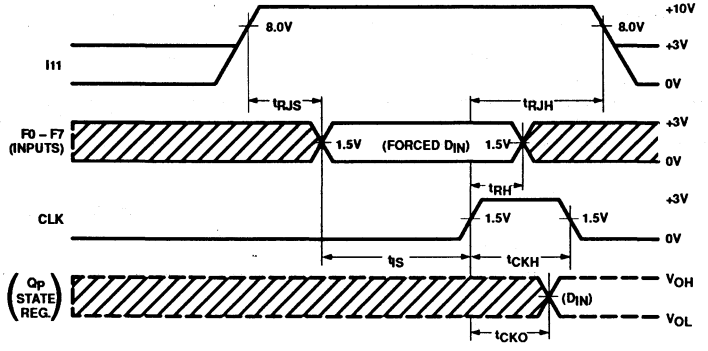


Power-On Preset

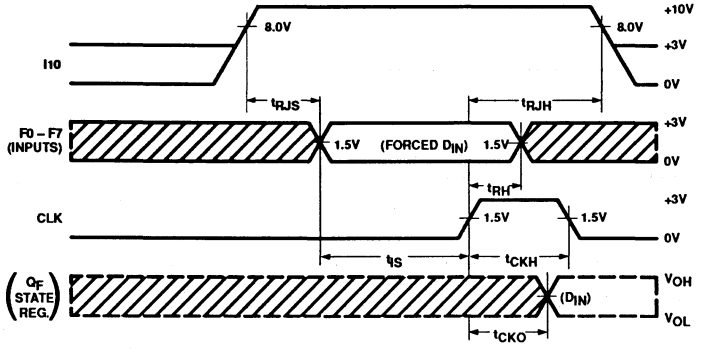
TIMING DIAGRAMS (Continued)



Diagnostic Mode – State Register Outputs



Diagnostic Mode – State Register Input Jam



Diagnostic Mode – Output Register Input Jam

TIMING DEFINITIONS

SYMBOL	PARAMETER
$t_{CKH1,2}$	Width of input clock pulse.
$t_{CKP1,2}$	Minimum guaranteed clock period.
t_{IS1}	Required delay between beginning of valid input and positive transition of Clock.
$t_{CKO1,2}$	Delay between positive transition of Clock and when Outputs become valid (with INIT/$\overline{OE}$ Low).
t_{PPR}	Delay between V_{CC} (after power-on) and when Outputs become preset at "1".
t_{IS2}	Required delay between beginning of valid Input and positive transition of Clock, when using optional Complement Array (two passes necessary through the AND Array).
t_{RJH}	Required delay between positive transition of clock, and return of input I10, I11 or I12 from Diagnostic Mode (10V).
$f_{MAX1,2}$	Minimum guaranteed operating frequency; input to output (CLK1 and CLK2).
$f_{MAX3,4}$	Minimum guaranteed operating frequency; input through Complement Array, to output (CLK1 and CLK2).
f_{MAX5}	Minimum guaranteed internal operating frequency; with internal feedback from state register to state register.

SYMBOL	PARAMETER
f_{MAX6}	Minimum guaranteed internal operating frequency with Complement Array, with internal feedback from state register through Complement Array, to state register.
f_{CLK}	Minimum guaranteed clock frequency (register toggle frequency).
$t_{CKL1,2}$	Interval between clock pulses.
t_{IH}	Required delay between positive transition of Clock and end of valid Input data.
t_{OE}	Delay between beginning of Output Enable Low and when Outputs become valid.
t_{SRE}	Delay between input I12 transition to Diagnostic Mode and when the Outputs reflect the contents of the State Register.
t_{RJS}	Required delay between inputs I11, I10 or I12 transition to Diagnostic Mode (10V), and when the output pins become available as inputs.
t_{NVCK}	Required delay between the negative transition of the clock and the negative transition of the Asynchronous Initialization to guarantee that the clock edge is not detected as a valid negative transition.

SYMBOL	PARAMETER
t_{INITH}	Width of initialization input pulse.
t_{VS}	Required delay between V_{CC} (after power-on) and negative transition of Clock preceding first reliable clock pulse.
t_{OD}	Delay between beginning of Output Enable High and when Outputs are in the OFF-state.
t_{INIT}	Delay between positive transition of Initialization and when Outputs become valid.
t_{SRD}	Delay between input I12 transition to Logic mode and when the Outputs reflect the contents of the Output Register.
t_{RH}	Required delay between positive transition of Clock and end of valid Input data when jamming data into State or Output Registers in diagnostic mode.
t_{VCK}	Required delay between negative transition of Asynchronous Initialization and negative transition of Clock preceding first reliable clock pulse.

Programmable logic sequencer (16 × 64 × 8)

PLUS405-55

LOGIC PROGRAMMING

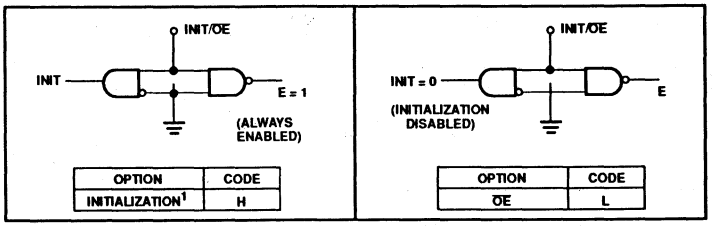
The PLUS405-55 is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Signetics SLICE and SNAP design software packages. ABEL™ and CUPL™ design software packages also support the PLUS405-55 architecture.

All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

PLUS405-55 logic designs can also be generated using the program table entry format, which is detailed on the following pages. This program table entry format is supported by SNAP and SLICE only. The SLICE design package is available, free of charge, to qualified users.

To implement the desired logic functions, each logic variable (I, B, P, S, T, etc.) from the logic equations is assigned a symbol. TRUE, COMPLEMENT, PRESET, RESET, OUTPUT ENABLE, INACTIVE, etc., symbols are defined below.

INITIALIZATION/$\overline{OE}$ OPTION – (INIT/$\overline{OE}$)



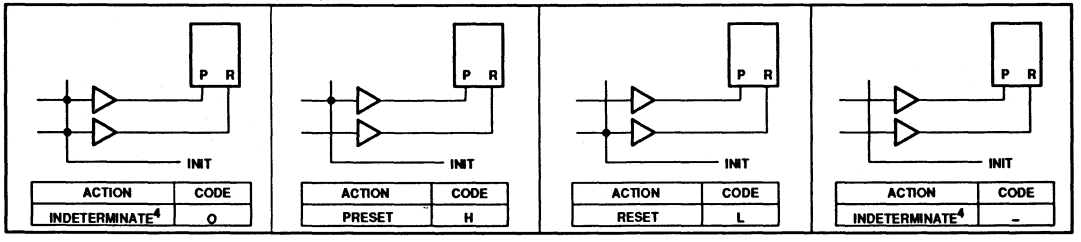
OPTION	CODE
INITIALIZATION[1]	H

OPTION	CODE
$\overline{OE}$	L

PROGRAMMING THE PLUS405:

The PLUS405 has a power-up preset feature. This feature insures that the device will power-up in a known state with all register elements (State and Output Register) at logic High (H). When programming the device it is important to realize this is the initial state of the device. You *must* provide a next state jump if you do not wish to use all Highs (H) as the present state.

INITIALIZATION OPTION – (INIT)



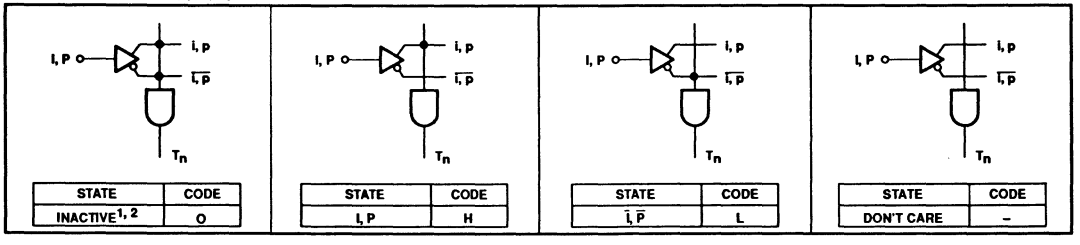
ACTION	CODE
INDETERMINATE[4]	0

ACTION	CODE
PRESET	H

ACTION	CODE
RESET	L

ACTION	CODE
INDETERMINATE[4]	–

"AND" ARRAY – (I), (P)



STATE	CODE
INACTIVE[1, 2]	0

STATE	CODE
I, P	H

STATE	CODE
$\overline{I, P}$	L

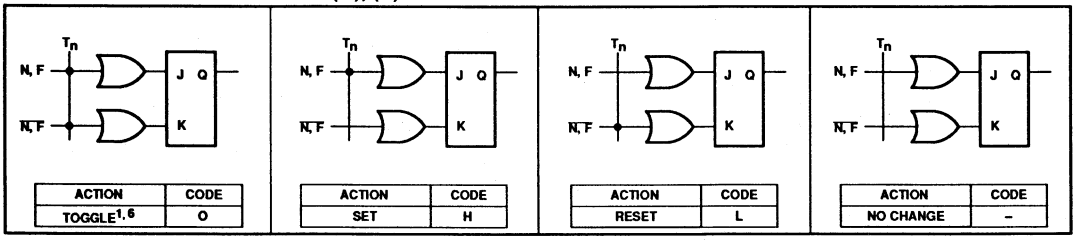
STATE	CODE
DON'T CARE	–

Notes are on next page.

ABEL is a trademark of Data I/O Corp.
CUPL is a trademark of Logical Devices, Inc.

Programmable logic sequencer (16 × 64 × 8) — PLUS405-55

"OR" ARRAY – J-K FUNCTION – (N), (F)



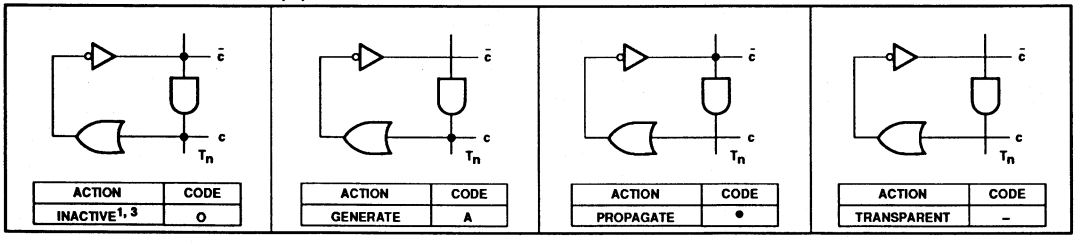
ACTION	CODE
TOGGLE[1,6]	O

ACTION	CODE
SET	H

ACTION	CODE
RESET	L

ACTION	CODE
NO CHANGE	–

"COMPLEMENT" ARRAY – (C)



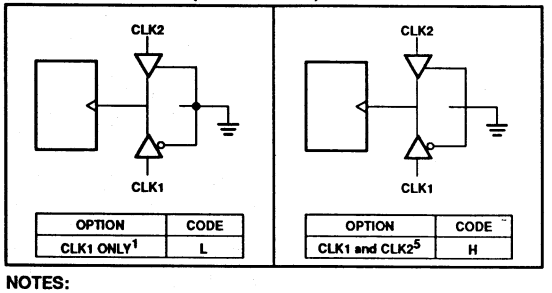
ACTION	CODE
INACTIVE[1,3]	O

ACTION	CODE
GENERATE	A

ACTION	CODE
PROPAGATE	•

ACTION	CODE
TRANSPARENT	–

CLOCK OPTION – (CLK1/CLK2)



OPTION	CODE
CLK1 ONLY[1]	L

OPTION	CODE
CLK1 and CLK2[5]	H

NOTES:
1. This is the initial unprogrammed state of all links.
2. Any gate T_n will be unconditionally inhibited if any one of its I or P link pairs is left intact.
3. To prevent oscillations, this state is not allowed for C link pairs coupled to active gates T_n.
4. These states are not allowed when using INITIALIZATION option.
5. Input buffer I5 must be deleted from the AND array (i.e., all fuse locations "Don't Care") when using second clock option.
6. A single product term cannot drive more than 8 registers by itself when used in TOGGLE mode.

Programmable logic sequencer (16 × 64 × 8)

PLUS405-55

PLUS405 PROGRAM TABLE

AND

INACTIVE	0	Im, Ps
I, P	H	
$\bar{I}, \bar{P}$	L	
DON'T CARE	–	

INACTIVE	0	Cn
GENERATE	A	
PROPAGATE	•	
TRANSPARENT	–	

OR

INACTIVE OR TOGGLE	0	Ns, Fr
SET	H	
RESET	L	
NO CHANGE	–	

OPTIONS

INIT	H	INIT/$\overline{OE}$
$\overline{OE}$	L	
CLK1 ONLY	L	CLK1/ CLK2
CLK1 AND 2	H	

REV________ DATE________

PROGRAM TABLE________

CUSTOMER NAME________

SIGNETICS DEVICE # CF (XXXX)________

CUSTOMER SYMBOLIZED PART #________

CLOCK 1/2

INITIALIZATION/OUTPUT ENABLE

	AND																										OR															
	COMP. ARRAY		INPUT (Im)																PRESENT STATE (Ps)								NEXT STATE (Ns)								OUTPUT (Fr)							
	C1	C0	I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0	P7	P6	P5	P4	P3	P2	P1	P0	N7	N6	N5	N4	N3	N2	N1	N0	F7	F6	F5	F4	F3	F2	F1	F0
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PIN NO.			20	21	22	23	24	25	26	27	2	3	4	5	6	7	8	9																	10	11	12	13	15	16	17	18
PIN LABELS																																										

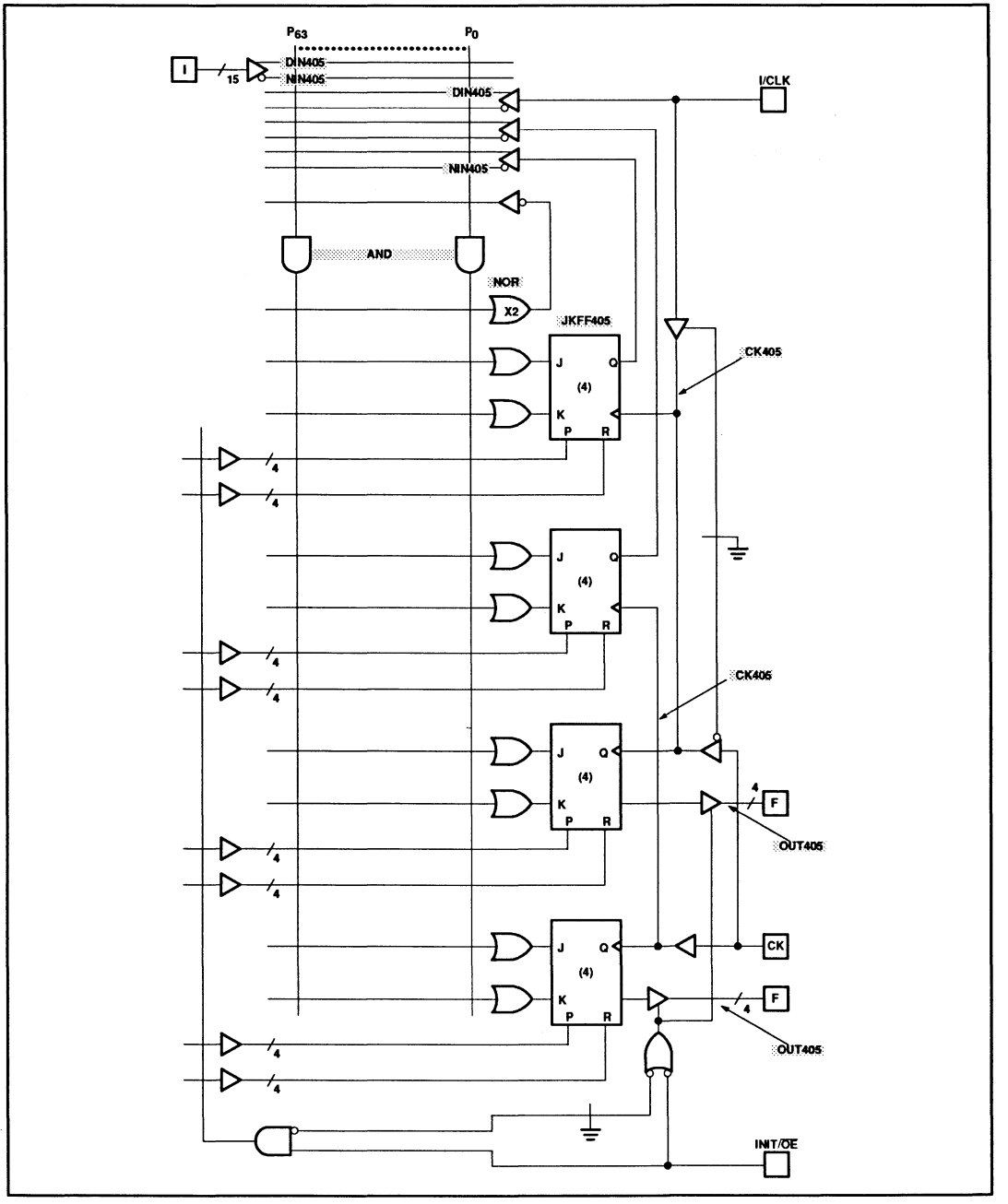
NOTES:

1. The device is shipped with all links initially intact. Thus, a background of "0" for all Terms, and an "H" for the IN/E and H for the clock option, exists in the table, shown BLANK instead for clarity.
2. Unused Cn Im, and Ps bits are normally programmed Don't Care (—).
3. Unused Transition Terms can be left blank for future code modification, or programmed as (—) for maximum speed.

Programmable logic sequencer (16 × 64 × 8)

PLUS405-55

SNAP RESOURCE SUMMARY DESIGNATIONS



Section 6
Programmable Macro Logic Data Sheets

INDEX

Programmable macro logic PML™

PLHS501/PLHS501I

FEATURES

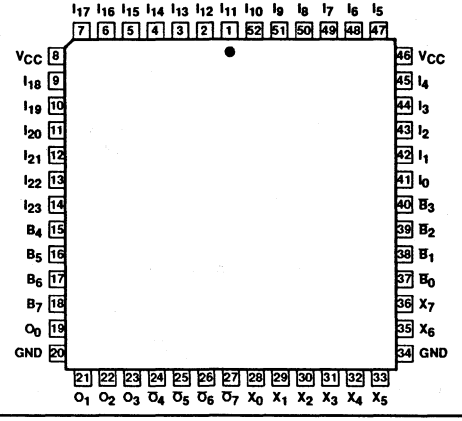
- Programmable Macro Logic device
- Full connectivity
- TTL compatible
- SNAP development system:
  - Supports third-party schematic entry formats
  - Macro library
  - Versatile netlist format for design portability
  - Logic, timing, and fault simulation
- SLICE development system:
  - Easy to learn and use
  - State or Boolean equation entry
  - Fuse table editor
  - Test vector editor
  - Boolean equation extractor
  - JEDEC fusemap compiler
  - Upgradeable to SNAP
- Delay per internal NAND function = 6.5ns (typ)
- Testable in unprogrammed state
- Security fuse allows protection of proprietary designs

STRUCTURE

- NAND gate based architecture
  - 72 foldback NAND terms
- 136 input-wide logic terms
- 44 additional logic terms
- 24 dedicated inputs ($I_0 - I_{23}$)
- 8 bidirectional I/Os with individual 3-State enable:
  - 4 Active-High ($B_4 - B_7$)
  - 4 Active-Low ($\overline{B}_0 - \overline{B}_3$)
- 16 dedicated outputs:
  - 4 Active-High outputs
    O_0, O_1 with common 3-State enable
    O_2, O_3 with common 3-State enable
  - 4 Active-Low outputs:
    $\overline{O}_4$, $\overline{O}_5$ with common 3-State enable
    $\overline{O}_6$, $\overline{O}_7$ with common 3-State enable
  - 8 Exclusive-OR outputs:
    X_0, X_1 with common 3-State enable
    X_2, X_3 with common 3-State enable
    X_4, X_5 with common 3-State enable
    X_6, X_7 with common 3-State enable

PIN CONFIGURATION

A Package
(52-pin PLCC)



DESCRIPTION

The PLHS501 is a high-density Bipolar Programmable Macro Logic device. PML incorporates a programmable NAND structure. The NAND architecture is an efficient method for implementing any logic function. The SNAP software development system provides a user friendly environment for design entry. SNAP eliminates the need for a detailed understanding of the PLHS501 architecture and makes it transparent to the user. PLHS501 is also supported on the Signetics SNAP and SLICE software development systems.

The PLHS501 is ideal for a wide range of microprocessor support functions, including bus interface and control applications.

The PLHS501 is also processed to industrial requirements for operation over an extended temperature range of –40°C to +85°C and supply voltage of 4.5V to 5.5V.

ARCHITECTURE

The core of the PLHS501 is a programmable fuse array of 72 NAND gates. The output of each gate folds back upon itself and all other NAND gates. In this manner, full connectivity of all logic functions is achieved in the PLHS501. Any logic function can be created within the core of the device without wasting valuable I/O pins. Furthermore, a speed advantage is acquired by implementing multi-level logic within a fast internal core without incurring any delays from the I/O buffers.

PML is a trademark of Philips Semiconductors–Signetics.

Programmable macro logic PML™

PLHS501/PLHS501I

ORDERING INFORMATION

DESCRIPTION	OPERATING CONDITIONS	ORDER CODE
52-Pin Plastic Leaded Chip Carrier	Commercial Temperature Range ±5% Power Supply	PLHS501A
52-Pin Plastic Leaded Chip Carrier	Industrial Temperature Range ±10% Power Supply	PLHS501IA

DESIGN DEVELOPMENT TOOLS

SNAP

The SNAP Software Development System provides the necessary tools for designing with PML. SNAP provides the following:

- Schematic entry netlist generation from third-party schematic design packages such as OrCAD/SDT III™ and FutureNet™.
- Macro library for standard TTL functions and user defined functions
- Boolean equation entry
- State equation entry
- Syntax and design entry checking
- Simulator includes logic simulation, fault simulation and timing simulation.

SNAP operates on an IBM® PC/XT, PC/AT, PS/2, or any compatible system with DOS 2.1 or higher. The minimum system configuration for SNAP is 640K bytes of RAM and a hard disk.

SNAP provides primitive PML function libraries for third-party schematic design packages. Custom macro function libraries can be defined in schematic or equation form.

After the completion of a design, the software compiles the design for syntax and completeness. Complete simulation can be carried out using the different simulation tools available.

The programming data is generated in JEDEC format. Using the Device Programmer Interface (DPI) module of SNAP, the JEDEC fusemap is sent from the host computer to the device programmer.

SLICE

SLICE, which supports Signetics PLD line, is easy to understand and simple to use. Select a PLD, assign input and output pins and enter the desired equations in either Boolean or state form. SLICE then checks the equations for errors. It automatically generates a JEDEC-format fuse map for downloading to a PLD programmer.

Fully menu driven, SLICE incorporates a fuse table editor for making quick modifications to the design and a test vector editor for input of test vectors.

A built-in Boolean equation extractor allows existing PLDs to be used as the basis for a new design. the extractor reads JEDEC information from a PLD and creates a file containing the corresponding Boolean equations. The result can then be used to consolidate several PLD designs into a single, denser part.

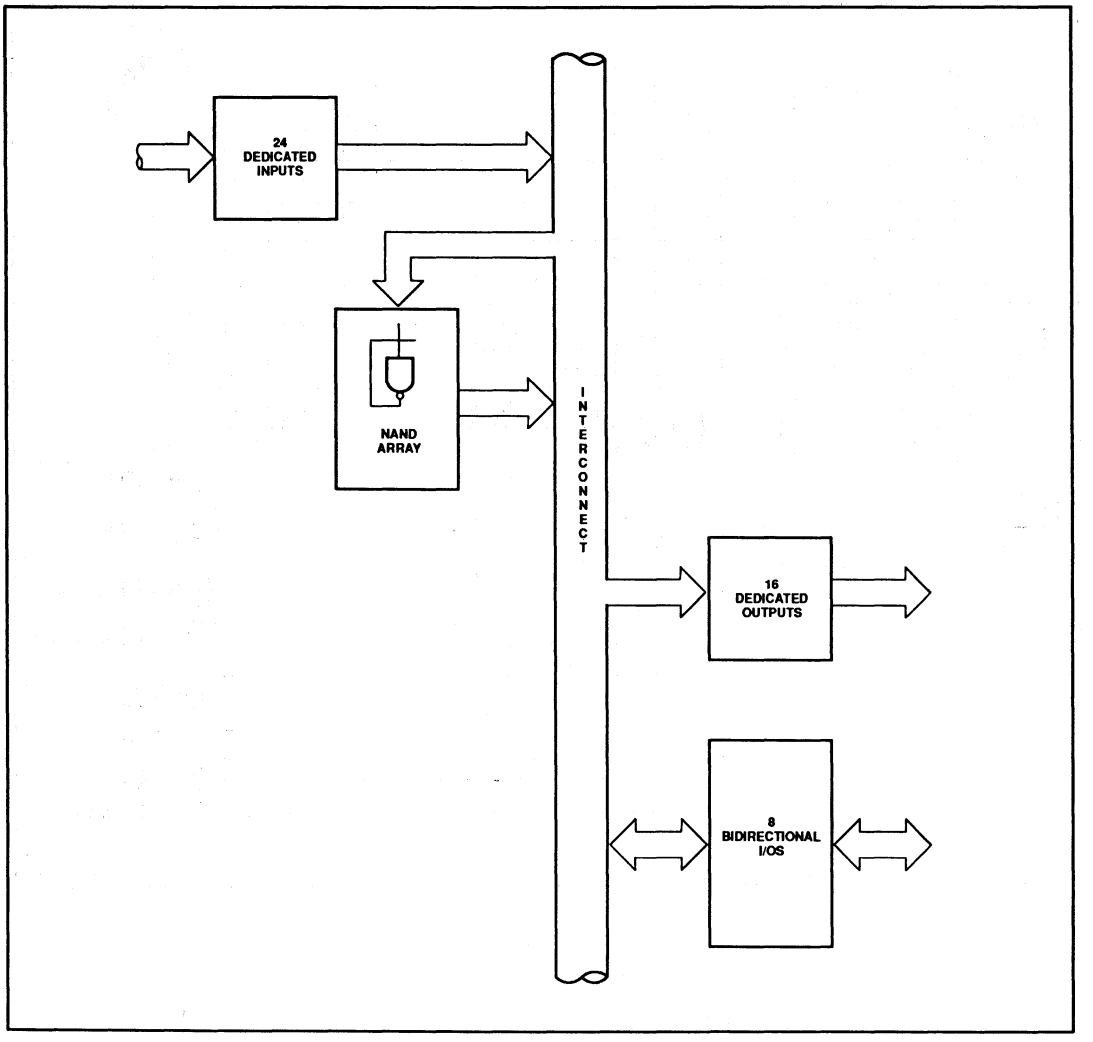
And SLICE is upward compatible with Signetics extensive design suite, SNAP.

DESIGN SECURITY

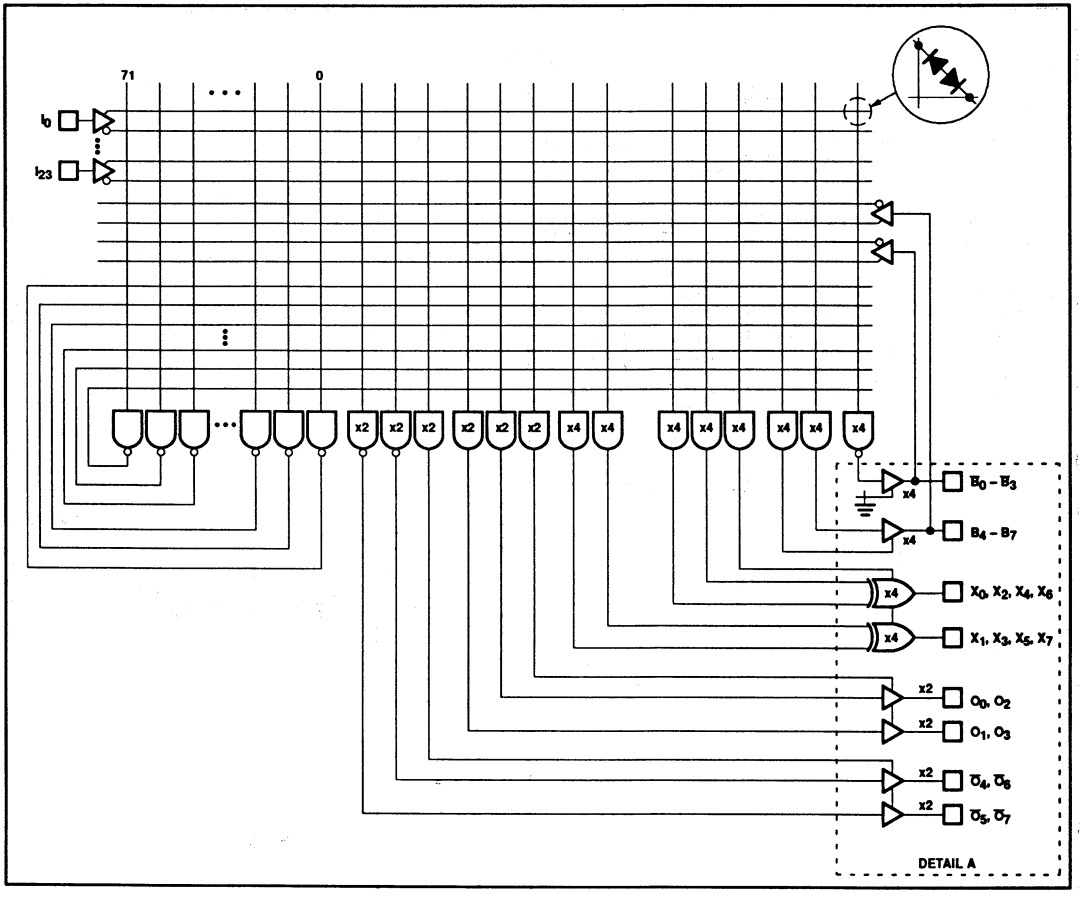
The PLHS501 has a programmable security fuse that controls the access to the data programmed in the device. By using this programmable feature, proprietary designs implemented in the device cannot be copied or retrieved.

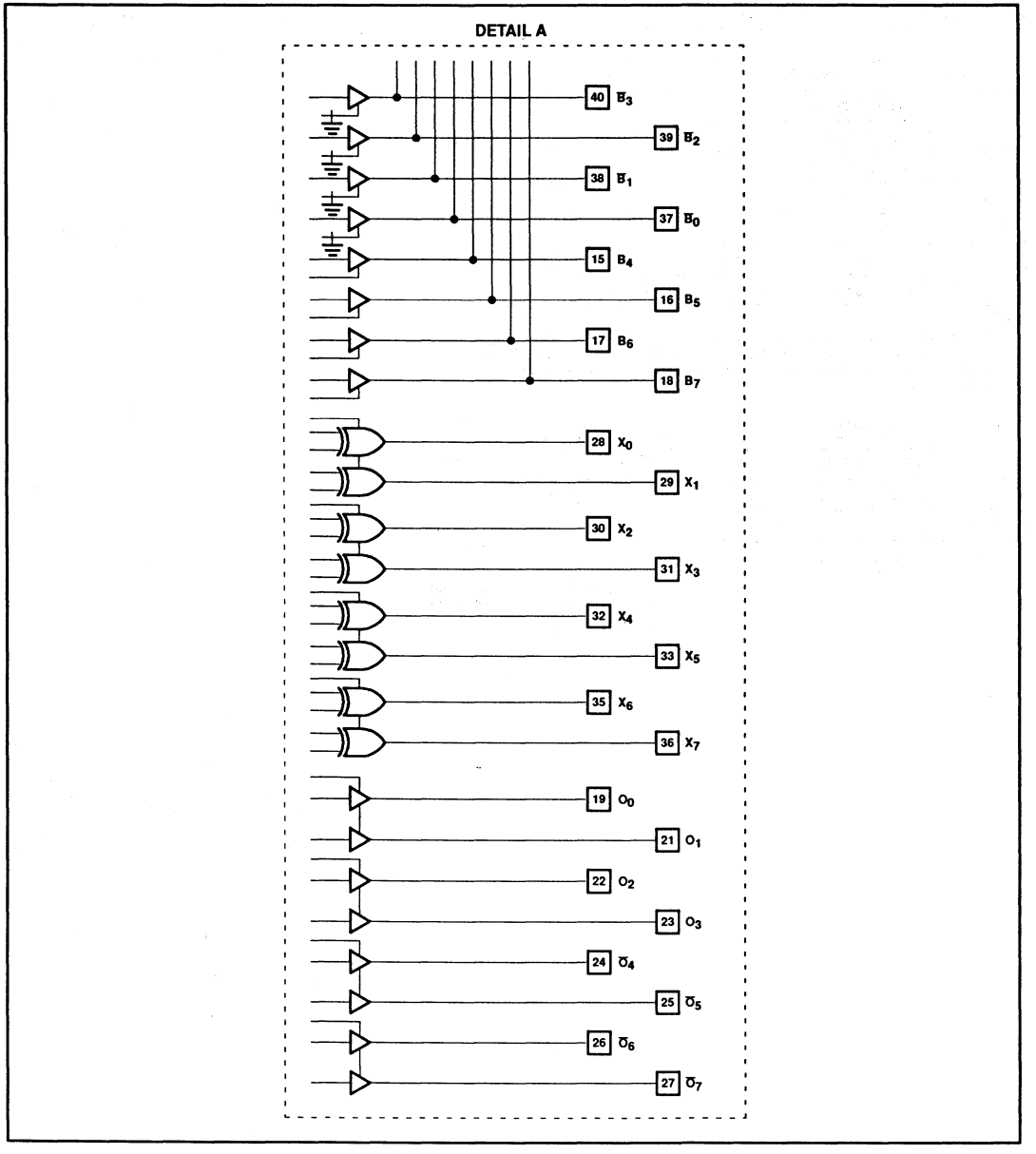
FutureNet is a trademark of FutureNet Corporation.
OrCAD/SDT is a trademark of OrCAD, Inc.
IBM is a registered trademark of International Business Machines Corporation.

PLHS501 FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DIAGRAM




DETAIL A
40 $\overline{B}_3$
39 $\overline{B}_2$
38 $\overline{B}_1$
37 $\overline{B}_0$
15 B_4
16 B_5
17 B_6
18 B_7
28 X_0
29 X_1
30 X_2
31 X_3
32 X_4
33 X_5
35 X_6
36 X_7
19 O_0
21 O_1
22 O_2
23 O_3
24 $\overline{O}_4$
25 $\overline{O}_5$
26 $\overline{O}_6$
27 $\overline{O}_7$

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS MIN	RATINGS MAX	UNIT
V_{CC}	Supply voltage		+7	V_{DC}
V_{IN}	Input voltage		+5.5	V_{DC}
V_{OUT}	Output voltage		+5.5	V_{DC}
I_{IN}	Input currents	–30	+30	mA
I_{OUT}	Output currents		+100	mA
T_{amb}	Operating temperature range	0	+75	°C
T_{stg}	Storage temperature range	–65	+150	°C

NOTE:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

VIRGIN STATE

A factory shipped virgin device contains all fusible links open, such that:

1. All product terms are enabled.
2. All bidirectional (B) pins are outputs.
3. All outputs are enabled.
4. All outputs are Active-High **except** $\overline{B}_0 - \overline{B}_3$ (fusible I/O) and $\overline{O}_4 - \overline{O}_7$ which are Active-Low.

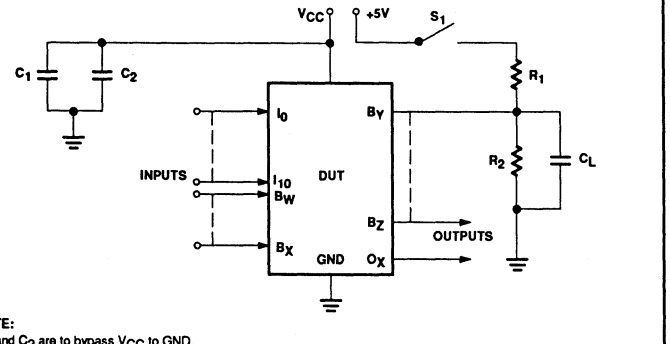
DC ELECTRICAL CHARACTERISTICS

Commercial= 0°C ≤ T_{amb} ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
Industrial = –40°C ≤ T_{amb} ≤ +85°C, 4.5V ≤ V_{CC} ≤ 5.5V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS MIN	LIMITS TYP[1]	LIMITS MAX	UNIT
Input voltage[2]						
V_{IL}	Low	V_{CC} = MIN			0.8	V
V_{IH}	High	V_{CC} = MAX	2.0			V
V_{IC}	Clamp[2, 3]	V_{CC} = MIN, I_{IN} = –12mA		–0.8	–1.2	V
Output voltage						
V_{OL}	Low[2, 4]	V_{CC} = MIN I_{OL} = 10mA			0.45	V
V_{OH}	High[2, 5]	I_{OH} = –2mA	2.4			V
Input current						
I_{IL}	Low	V_{CC} = MAX V_{IN} = 0.45V			–100	µA
I_{IH}	High	V_{IN} = 5.5V			40	µA
Output current						
$I_{O(OFF)}$	Hi-Z state[9]	V_{CC} = MAX V_{OUT} = 5.5V			80	µA
		V_{OUT} = 0.45V			–140	
I_{OS}	Short circuit[3, 5, 6]	V_{OUT} = 0V	–15		–70	mA
I_{CC}	V_{CC} supply current[8]	V_{CC} = MAX		225	295	mA
Capacitance						
C_{IN}	Input	V_{CC} = 5V V_{IN} = 2.0V		8		pF
C_B	I/O	V_{OUT} = 2.0V		15		pF

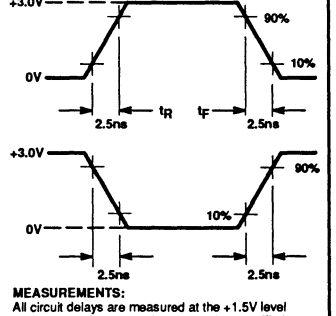
NOTES:
1. All typical values are at V_{CC} = 5V, T_{amb} = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Test one at a time.
4. For Pins 15 – 19, 21 – 27 and 37 – 40, V_{OL} is measured with Pins 5 and 41 = 8,75V, Pin 43 = 0V and Pins 42 and 44 = 4.5V. For Pins 28 – 33 and 35 – 36, V_{OL} is measured under same conditions EXCEPT Pin 44 = 0V.
5. V_{OH} is measured with Pins 5 and 41 = 8.75V, Pins 42 and 43 = 4.5V and Pin 44 = 0V.
6. Duration of short circuit should not exceed 1 second.
7. I_{CC} is measured with all dedicated inputs at 0V and bidirectional and output pins open.
8. Measured at V_T = V_{OL} + 0.5V.
9. Leakage values are a combination of input and output leakage.

TEST LOAD CIRCUITS



NOTE:
C_1 and C_2 are to bypass V_{CC} to GND.

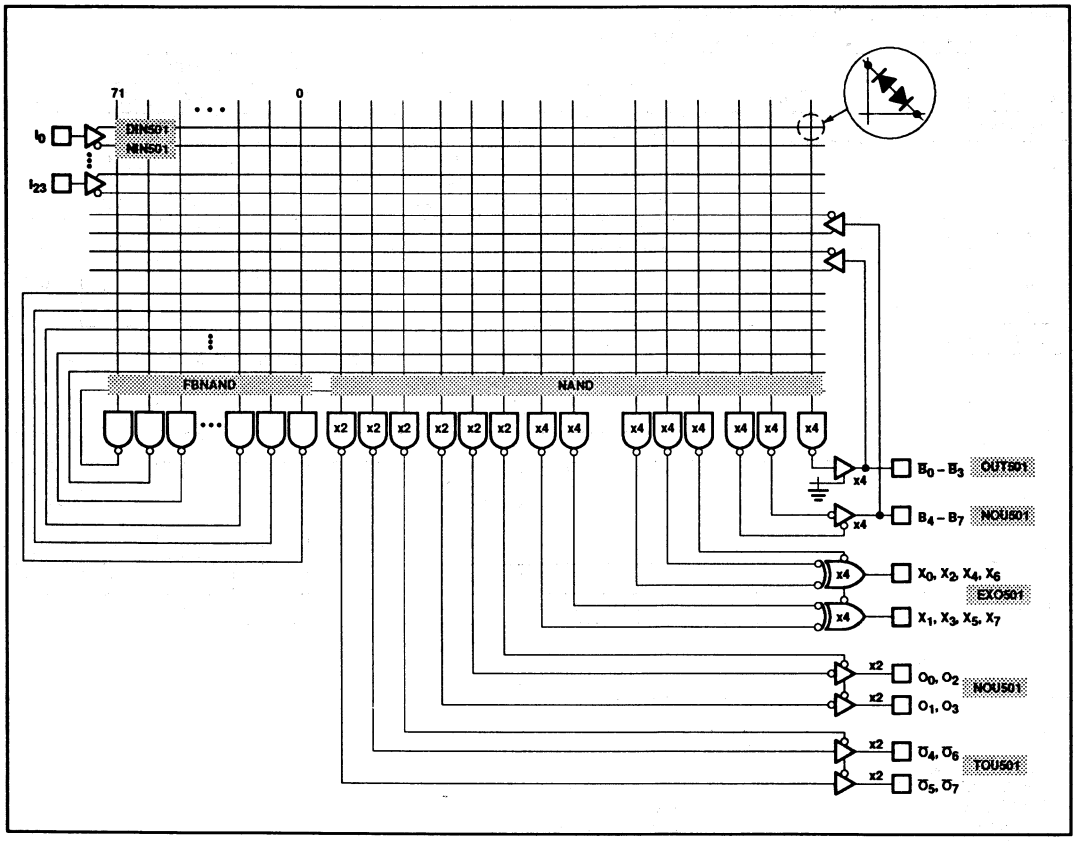
VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

SNAP RESOURCE SUMMARY DESIGNATIONS



MACRO CELL SPECIFICATIONS[1] (SNAP Resource Summary Designations in Parantheses)

Commercial: T_{amb} = 0°C to +75°C, 4.75V ≤ V_{CC} ≤ 5.25V, C_L = 30pF, R_2 = 1000Ω, R_1 = 470Ω
Industrial: T_{amb} = –40°C to +85°C, 4.5V ≤ V_{CC} ≤ 5.5V, C_L = 30pF, R_2 = 1000Ω, R_1 = 470Ω

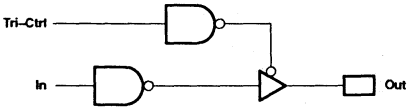
Input Buffer
(DIN501 [Non-Inverting], NIN501 [Inverting])

SYMBOL	LIMITS MIN	TYP	MAX	UNIT
Δt_{HL}	0.05	0.1	0.15	ns/p-term
Δt_{LH}	–0.02	–0.05	–0.08	ns/p-term

SYMBOL	PARAMETER To (Output)	From (Input)	LIMITS MIN	TYP	MAX	UNIT	NOTES
t_{PHL}	X	I	4.5	5.5	6.5	ns	With 0 p-terms load
t_{PLH}	X	I	5	6	7.5	ns	
t_{PHL}	Y	I	2.5	3	3.5	ns	With 0 p-terms load
t_{PLH}	Y	I	4	4	4.5	ns	

Input Pins: 1 – 7, 9 – 14, 41 – 45, 48 – 52.
Bidirectional Pins: 15 – 18, 37 – 40.
Maximum internal fan-out: 16 p-terms on X or Y.

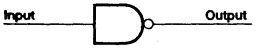
NAND Output Buffer with 3-State Control
(TOU501)



SYMBOL	PARAMETER To (Output)	From (Input)	LIMITS MIN	TYP	MAX	UNIT
t_{PHL}	Out	In	8.5	14.0	17.5	ns
t_{PLH}	Out	In	8.5	14.0	16	ns
t_{OE}[2]	Out	Tri-Ctrl	8.5	15	18.5	ns
t_{OD}[2]	Out	Tri-Ctrl	8.5	12.5	17.0	ns

Output Pins: 24 – 27.

Internal Foldback NAND
(FBNAND)



SYMBOL	LIMITS MIN	TYP	MAX	UNIT
Δt_{PHL}	0.05	0.1	0.15	ns/p-term
Δt_{PLH}	–0.0	–0.05	–0.1	ns/p-term

SYMBOL	PARAMETER To (Output)	From (Input)	LIMITS MIN	TYP	MAX	UNIT	NOTES
t_{PHL}	Out	Any	4.0	4.5	6.8	ns	With 0 p-terms load
t_{PLH}			5.5	6.5	8	ns	

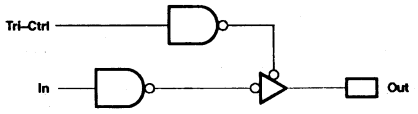
Maximum internal loading of 16 terms.

Notes are on following page.

MACRO CELL SPECIFICATIONS[1] (Continued) (SNAP Resource Summary Designations in Parantheses)

Commercial: T_{amb} = 0°C to +75°C, 4.75V ≤ V_{CC} ≤ 5.25V, C_L = 30pF, R_2 = 1000Ω, R_1 = 470Ω
Industrial: T_{amb} = –40°C to +85°C, 4.5V ≤ V_{CC} ≤ 5.5V, C_L = 30pF, R_2 = 1000Ω, R_1 = 470Ω

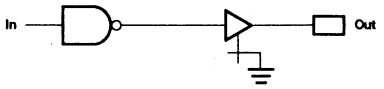
AND Output Buffer with 3-State Control (NOU501)



SYMBOL	PARAMETER		LIMITS			UNIT
	To (Output)	From (Input)	MIN	TYP	MAX	
t_{PHL}	Output	In	8.0	11	13	ns
t_{PLH}	Output	In	8.0	11	13	ns
t_{OE}[2]	Out	Tri-Ctrl	8.5	15	18.5	ns
t_{OD}[2]	Out	Tri-Ctrl	8.5	12.5	17.0	ns

Bidirectional and Output Pins: 19, 21, 22, 23, 15 – 18.

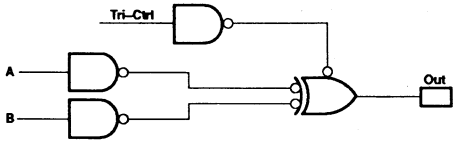
NAND Output Buffer (OUT501)



SYMBOL	PARAMETER		LIMITS			UNIT
	To (Output)	From (Input)	MIN	TYP	MAX	
t_{PHL}	Out	In	8.5	14	17.5	ns
t_{PLH}	Out	In	8.5	14	16.0	ns

Bidirectional Pins: 37 – 40.

Ex–OR Output Buffer (EXO501)



SYMBOL	PARAMETER		LIMITS			UNIT
	To (Output)	From (Input)	MIN	TYP	MAX	
t_{PHL}	Out	A or B	8.5	14	17.5	ns
t_{PLH}	Out	A or B	8.5	14	16.0	ns
t_{OE}[2]	Out	Tri-Ctrl	8.5	15	18.5	ns
t_{OD}[2]	Out	Tri-Ctrl	8.5	12.5	17.0	ns

Ex-OR Output Pins: 28 – 33.

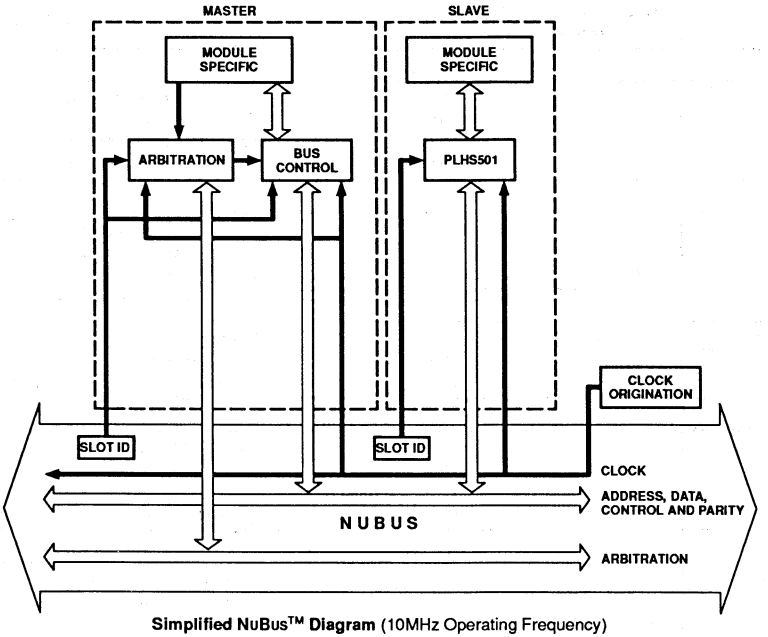
NOTES:

1. Limits are guaranteed with internal feedback buffers simultaneously switching cumulative maximum of eight outputs.
2. For 3-State output; output enable times are tested with C_L = 30pF to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with C_L = 5pF. High-to-High impedance tests are made to an output voltage of V_T = (V_{OH} – 0.5V) with S_1 open, and Low-to-High impedance tests are made to the V_T = (V_{OL} + 0.5V) level with S_1 closed.

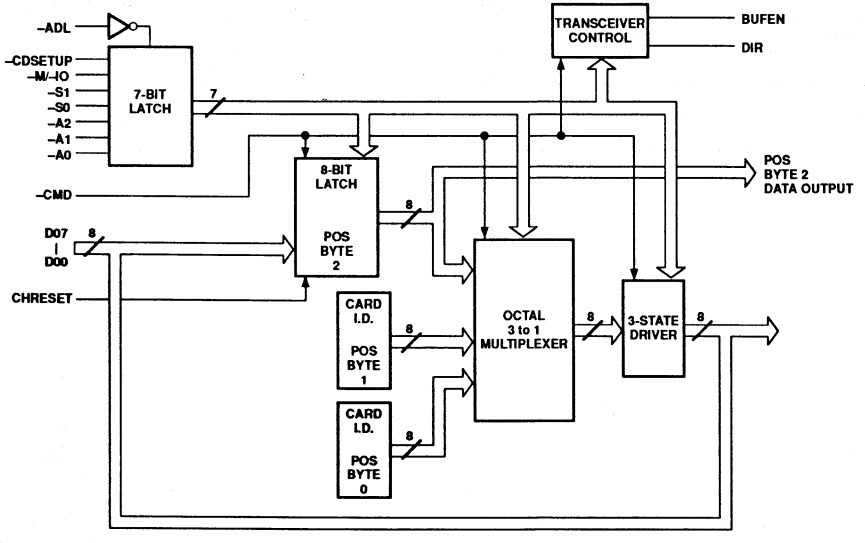
PLHS501 GATE AND SPEED ESTIMATE TABLE

FUNCTION	INTERNAL NAND EQUVALENT	TYPICAL t_{PD}	f_{MAX}	COMMENTS
Gates				
NANDs	1	6.5ns		For 1 to 32 input variables
ANDs	1	6.5ns		For 1 to 32 input variables
NORs	1	6.5ns		For 1 to 32 input variables
ORs	1	6.5ns		For 1 to 32 input variables
Decoders				
3-to-8	8	11ns		Inverted inputs available
4-to-16	16	11ns		Inverted inputs available
5-to-32	32	11ns		Inverted inputs available (24 chip outputs only)
Encoders				
8-to-3	15	11ns		Inverted inputs, 2 logic levels
16-to-4	32	11ns		Inverted inputs, 2 logic levels
32-to-5	41	11ns		Inverted inputs, 2 logic levels, factored solution.
Multiplexers				
4-to-1	5	11ns		Inverted inputs available
8-to-1	9	11ns		
16-to-1	17	11ns		
27-to-1	28	11ns		Can address only 27 external inputs - more if internal
Flip-Flops				
D-type Flip-Flop	6		30MHz	With asynchronous S-R
T-type Flip-Flop	6		30MHz	With asynchronous S-R
J-K-type Flip-Flop	10		30MHz	With asynchronous S-R
Adders				
8-bit	45	15.5ns		Full carry-lookahead (four levels of logic)
Barrel Shifters				
8-bit	72	11ns		2 levels of logic
Latches				
D-latch	3			2 levels of logic with one shared gate

APPLICATIONS



Simplified NuBus™ Diagram (10MHz Operating Frequency)



Block Diagram of Basic POS Implementation in PLHS501

NuBus is a trademark of Texas Instruments, Inc.

CMOS high density programmable macro logic — PML2552

FEATURES

- Full connectivity
- Erasable version and one time programmable version available
- Scan test
- Power down mode
- Power on reset
- 100% testable
- SNAP development system
  - Supports third-party schematic entry formats
  - TTL Macro library
  - Versatile netlist format for design portability
  - Logic, timing, and fault simulation
- SLICE development system:
  - Easy to learn and use
  - State or Boolean equation entry
  - Fuse table editor
  - Test vector editor
  - Boolean equation extractor
  - JEDEC fusemap compiler
  - Upgradeable to SNAP
- Power dissipation (TTL) = 630mW
- Power dissipation (CMOS) = 525mW
- Power dissipation (Power-Down mode) = 52mW
- Security fuse for copy protection
- Reprogrammable

PROPAGATION DELAYS

- Delay per internal NAND gate = 15ns (typ)
- 50MHz flip-flop toggle rate

APPLICATIONS

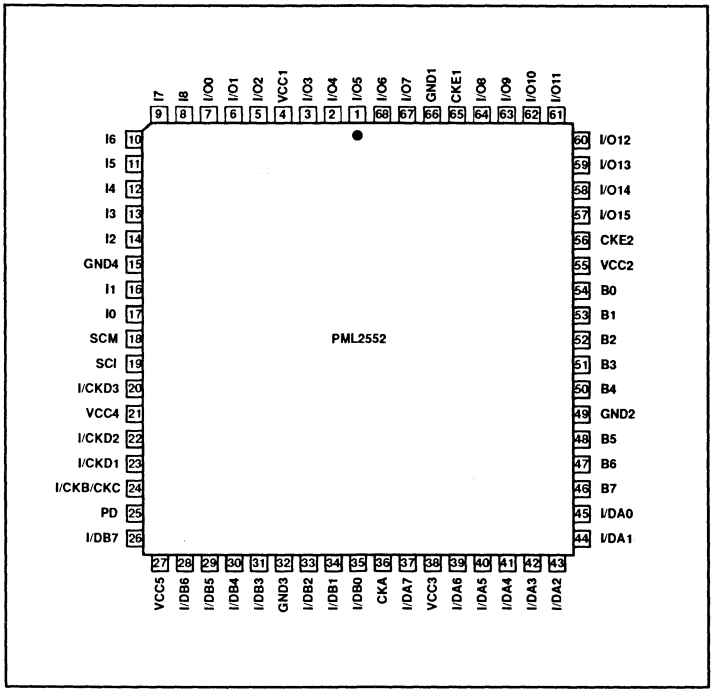
- Low-end gate array replacement
- Instrumentation
- Bus arbitration functions
- Wide multiplexers and decoders
- Multiple independent state machines
- General purpose logic integration and microprocessor support logic
- PAL® and glue logic replacement

DESCRIPTION

The Signetics PML family of PLDs provides "instant gate array" capabilities for general purpose logic integration applications. The PML2552 is the first high density CMOS-PML product. Fabricated with the Signetics high-performance EPROM process, it is an ideal way to reduce NRE costs, inventory problems and quality concerns. The PML2552 incorporates the PML folded NAND array architecture which provides 100% connectivity to eliminate routing restrictions. What distinguishes the PML2552 from the "classic" PLD architectures is its flexibility and the potent flip-flop building blocks. The device utilizes a folded NAND architecture, which enables the designer to implement multiple levels of logic on a single chip. The PML2552 eliminates the NRE costs, risks, and hard to use design tools associated with semicustom and full custom approaches. It allows the system designer to manage reliable functionality, in less time and space plus a faster time to market. The PML2552 is ideal in todays instrumentation, industrial control, EISA, NuBus™, bus interface and dense state machine applications in conjunction with the state-of-the-art CMOS processors. It is capable of replacing large amounts of TTL, SSI and MSI logic and literally allows the designer to build a system on the chip.

The SNAP development software gives easy access to the density and flexibility of the PML2552 through a variety of design entry formats, including schematic, logic equations, and state equations in any combination.

PIN CONFIGURATION



PAL is a registered trademark of Advanced Micro Devices, Inc.
NuBus is a trademark of Texas Instruments, Inc.

ORDERING INFORMATION

DESCRIPTION	t_{PD} (MAX)	ORDER CODE
68-pin Plastic Leaded Chip Carrier	35ns	PML2552-35A
68-pin "J" Leaded Ceramic Cerquad Package	35ns	PML2552-35KA
68-pin Plastic Leaded Chip Carrier	50ns	PML2552-50A
68-pin "J" Leaded Ceramic Cerquad Package	50ns	PML2552-50KA

FUNCTIONAL BLOCK DIAGRAM

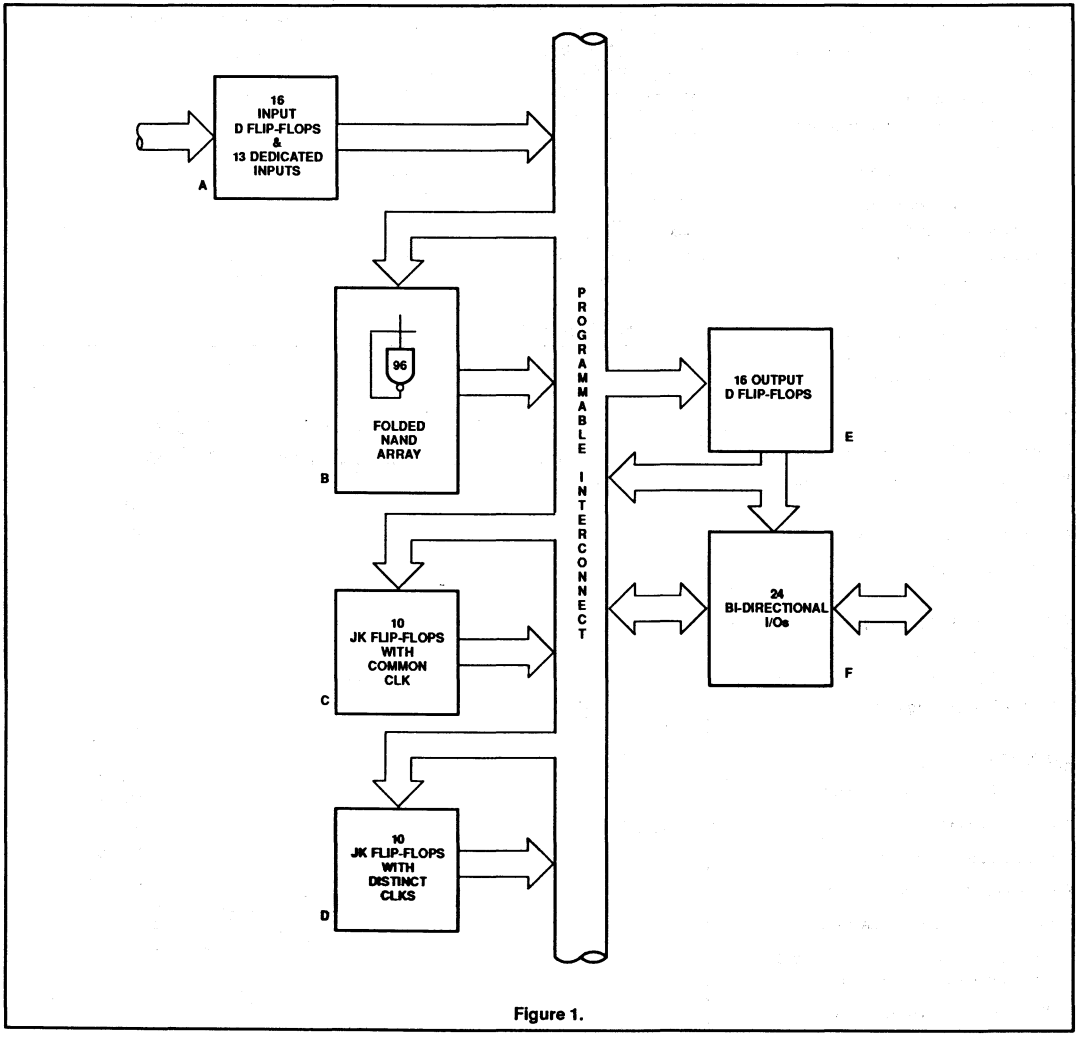
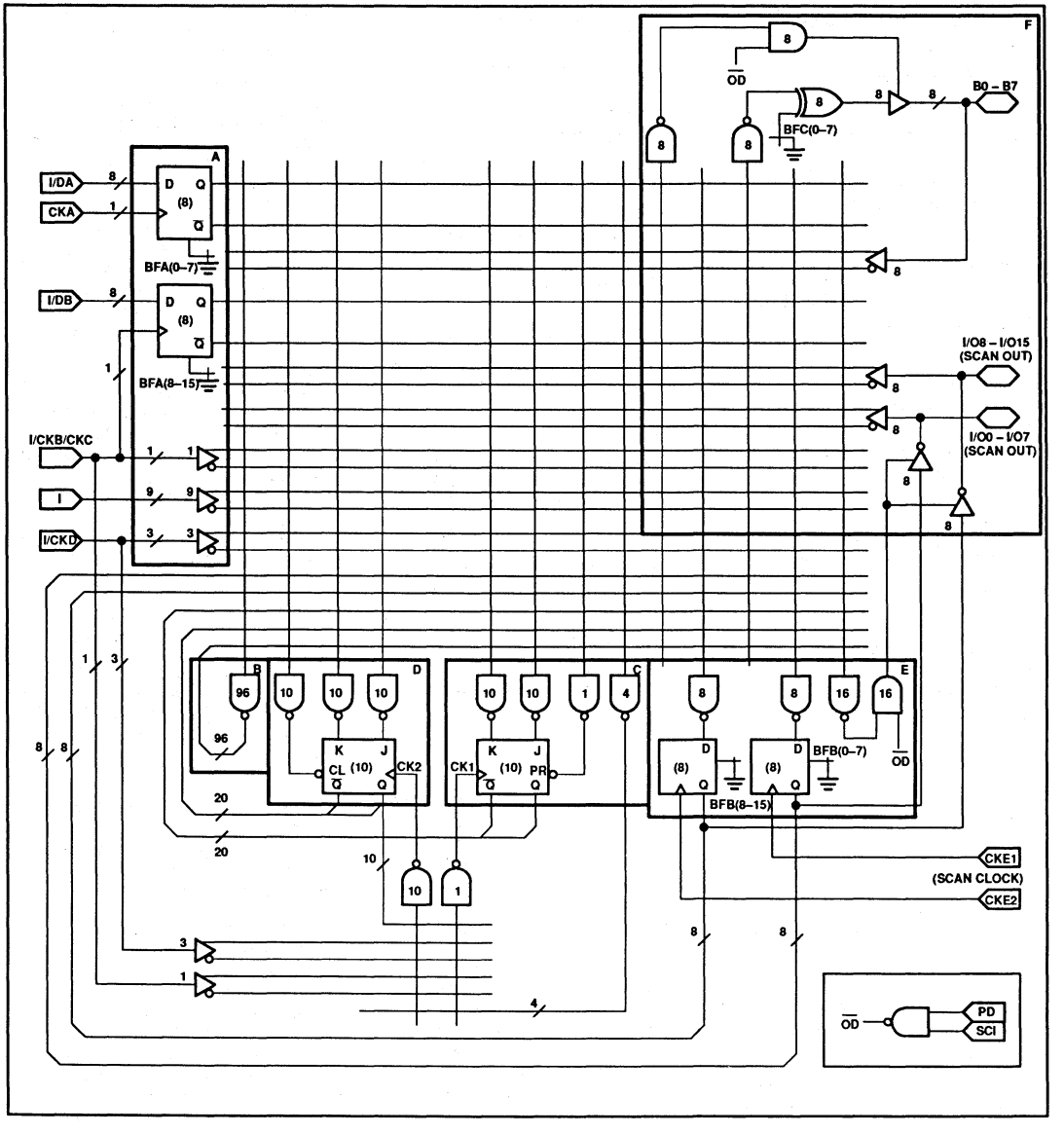


Figure 1.

LOGIC DIAGRAM



CMOS high density programmable macro logic — PML2552

STRUCTURE

- 112 possible foldback NAND gates:
  - 96 internal NAND
  - 16 from the I/O macros
- 114 additional logic terms
- 53 possible inputs (with programmable polarity)
  - 29 dedicated inputs
  - 24 bidirectional I/Os
- 24 bidirectional pins
- 52 flip-flops
- 24 possible outputs with individual Output Enable control (8 with programmable polarity)
- Multiple independent clocks
- 20 Buried JK-type flip-flops with foldback (JKFFs):
  - 10 JKFFs with one shared preset signal and one shared clocked signal originating from the clock array.
  - 10 JKFFs with 10 independent clock signals originating from the clock array and 10 independent clear signals
- 258 inputs per NAND gate
- Bypassable Input D-type flip-flop (DFFs)/Combinatorial Inputs:
  - 16 DFFs/combinatorial inputs
  - DFFs clocked in two groups of eight
  - DFFs not bypassed in unprogrammed state
  - Independent bypass fuse on each DFF
- Inputs/bypassable D-type flip-flop outputs/foldback NAND gates:
  - 16 output DFFs/combinatorial inputs/outputs with individual Output Enable control
  - DFFs clocked in two groups of eight
  - DFFs not bypassed in unprogrammed state
  - Independent bypass fuse on each DFF
  - The DFF can be used as an internal DFF or an internal foldback NAND gate.
- Combinatorial inputs:
  - 9 dedicated inputs to the NAND array
  - 3 inputs optional to NAND array and/or clock array
  - 1 input optional to NAND array and/or clock array, and/or clock of Input D Flip-Flops (Group B)
- Separate clock array:
  - Separate clock array for JKFFs clock inputs
  - 4 inputs to clock array originated from NAND array
  - 4 inputs (with programmable polarity) directly from input pins
  - 10 inputs from Q outputs of JKFFs with clear
- Dedicated clocks:
  - One dedicated clock for input DFFs (Group A)
  - Two dedicated clocks for output DFFs
- Scan test feature:
  - Scan chain is implemented through the 20 buried JKFFs and 16 output DFFs
  - Pins SCI, SCM, and CKE1 are used to operate the scan test
- Power down mode
  - Dedicated pin (PD) freezes the circuit when brought to logic "1". The circuit remains in the same state prior to the logic "0" to logic "1" transition of the "PD" pin.
  - When in the power down mode, the SCI pin acts as the 3-State pin for the 24 outputs.
- Power on reset:
  - All flip-flops (16 input DFFs, 20 buried JKFFs, and 16 output DFFs) are reset to logic "0" after V_{CC} power on.

ARCHITECTURE

The core of the PML2552 is a programmable NAND array of 96 NAND gates and 20 buried JKFFs. The output of each NAND gate folds back upon itself and all other NAND gates and flip-flops. The 'Q' and '$\overline{Q}$' output of each flip-flop also folds back in the same manner. Thus, total connectivity of all logic functions is achieved in the PML2552. Any logic function can be created within the core without wasting valuable I/O pins. Furthermore, a speed advantage is acquired by implementing multi-level logic within a fast internal core without incurring any delays from the I/O buffers. Figure 1 shows the functional block diagram of the PML2552.

Macro Cells

There are 16 bypassable DFFs on the input to the NAND array. These flip-flops are split in two banks of 8 (Bank A and Bank B). Each bank of flip-flops has a common clock. In the unprogrammed state of the device the flip-flops are active. In order to bypass any DFF, its respective bypass fuse (BFA_X) must be programmed.

The 16 I/O pins (IO_0 - IO_{15}) and their respective D flip-flop macros can be used in any one of the following configurations:

1. As combinatorial input(s).
   Each of the 16 3-State outputs can be individually disabled by the associated NAND term and the pin is used as an inverting or non-inverting input.
2. As registered DFF outputs.
   These DFFs are split into two banks of 8, and each bank is clocked separately. The bypass fuse BFB_X (see PML2552 Logic Diagram) is used to bypass any one of these DFFs. The flip-flops are all active in an unprogrammed device.
3. As combinatorial outputs.
   By programming the bypass (BFB_X) fuse of any one of the DFFs, the flip-flop(s) is bypassed. The I/O pin can then be used as a combinatorial output.
4. As Internal foldback DFFs or foldback NAND gates.
   When the I/O pin is used as an input, the output macro can be used as an internal DFF or a foldback NAND term. If the bypass fuse is programmed, the macro will act as a foldback NAND term. Otherwise it will act as an internal DFF.

The 8 bidirectional pins (B0-B7) can be used as either combinatorial inputs or outputs with programmable polarity. The Exclusive-OR polarity gates are non-inverting in the unprogrammed state.

The NAND signal labeled '$\overline{OD}$' (Output Disable) shown on the PML2552 logic diagram is used for the Power Down mode operation. This signal disables the outputs when the device enters the Power Down mode and SCI is high.

Clock Array

The 20 buried JKFFs can be clocked through the 'Clock Array'. The Clock Array consists of 11 NAND terms. Ten of these terms are connected to the clock inputs of the Bank A flip-flops that can be clocked individually. One NAND gate is connected to Bank B flip-flops that have a common clock. There are 18 inputs to the clock array. Four come directly from the input pins (with programmable polarity), 4 inputs are from 4 NAND gates connected directly to the folded NAND array. 10 inputs are from the Q outputs of the JKFFs with clear.

SCAN TEST FEATURE

With the rise in the ratio of devices on a chip to the number of I/O pins, Design For Testability is becoming an essential factor in logic design methodology. The PML2552 incorporates a variable length scan test feature which permits access to the internal flip-flop nodes without requiring a separate external I/O pin for each node accessed. Figure 2 (Scan Mode Operation) shows how a scan chain is implemented through the 20 buried JKFFs and 16 output DFFs. Two dedicated pins, SCI (Scan In) and SCM (Scan Mode), are used to operate the scan test. The SCM pin is used to put the circuit in scan mode. When this pin is brought to a logic "1", the circuit enters the scan mode.

In this mode it is possible to shift an arbitrary test pattern into the flip-flops. The SCI pin is used to input the pattern. The inverted outputs of flip-flops D0 - D15 are observable on pins I/O0 - I/O15.

The following are features and characteristics of the device when in Scan Mode:

1. CKE1 is the common scan-clock for all the flip-flops when in scan mode. CKE1 overrides all clock resources of normal operational mode.
2. The Preset (PR) and Clear (CL) functions of the flip-flops are disabled.
3. Scan overrides the bypass fuse of the flip-flops. This means that all the bypassable DFFs remain intact during scan operation even though they may have been bypassed during normal operation.
4. To observe the SCAN data, the output buffers must be enabled by the Output Enable (tri-ctrl) terms.
5. The outputs of the flip-flops are complemented on pins I/O0 - I/O15.
6. All external inputs to flip-flops in the scan chain are disabled when the device enters the scan mode.
7. Blowing the security fuse does not disable the Scan Test feature.

SCAN MODE OPERATION

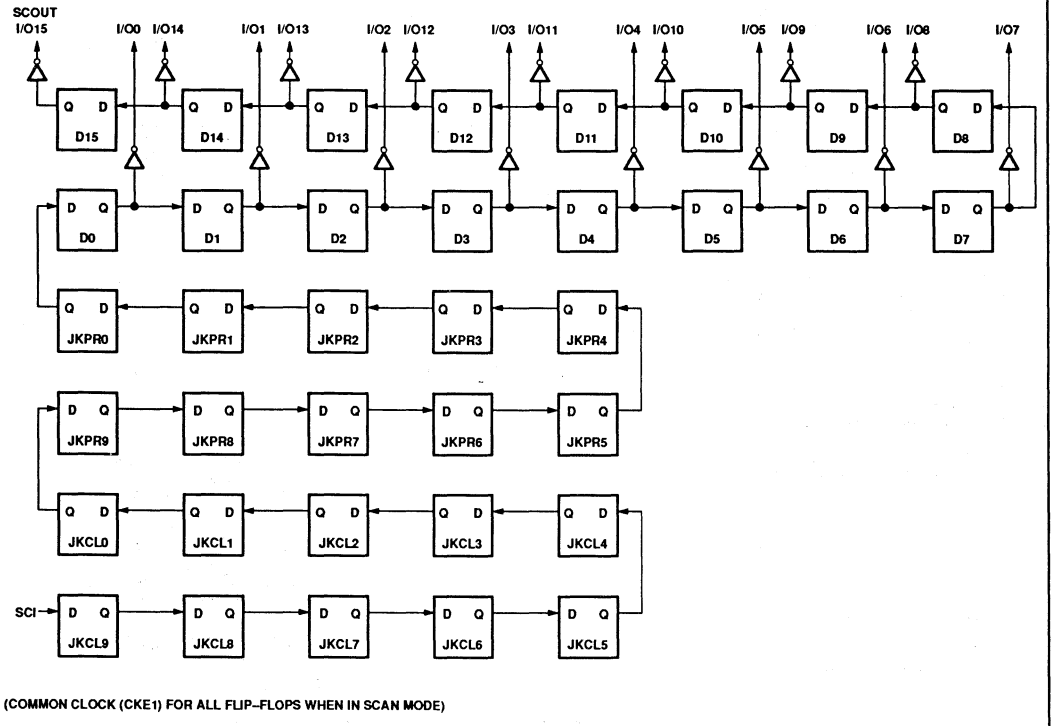


Figure 2.

SCAN TEST STRATEGY

The scan test pattern is design dependent and the user must make considerations for Design For Testability (DFT) during the initial stages of the design. A typical test sequence is to pre-load (i.e., enter a state); revert to normal operation (i.e., activate the next state transition); go back to scan mode to check the result. Note that the scan test feature available in the PML2552 is a variable length scan chain. The DATA entered at SCI (JKCL9) can be accessed anywhere between 21 clock cycles (at I/O0) to 36 clock cycles (at I/O15). For the strategy discussed here, DATA is read out after 36 clocks at I/O15 (i.e., D15). The following operation sequence suggests a possible scan test method.

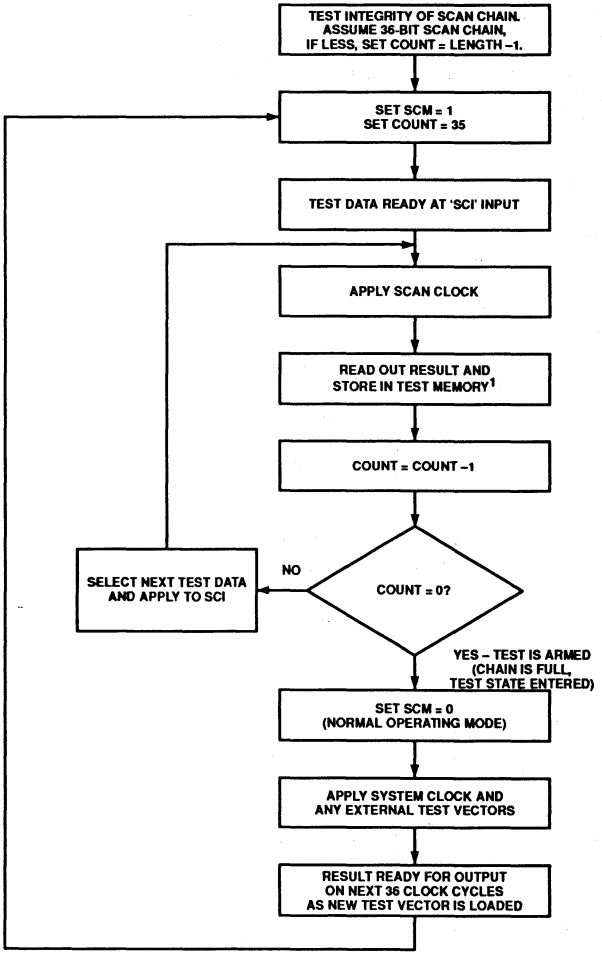
A conservative test policy demands proof that the test facility is working. Thus, to prove Scan Chain holds and maintains correct data:

a. Fill chain with several patterns (for example, all ones and all zeros).

b. Retrieve same patterns.

The user is responsible for managing an external test memory buffer for applied vectors and results, as part of the test equipment.

1. Parallel readout of I/O0 - I/O15 is possible, but assume only I/O15 is used for this strategy.
2. The first DATA entered at SCI (or JKCL9) will be the content of D15 after 36 clocks. This DATA will be inverted at the output pin I/O15 (i.e., SCOUT). The last DATA entering the scan chain will be the content of JKCL9. Thus, the scan chain resembles a first-in-first-out shift register with inverted outputs (I/O0 - I/O15).
3. 'Test Data' is read in at the SCI input and read out of the SCOUT output pin (I/O15). To enter 'Test Data':
   a. Put device in Scan Mode by applying the scan control signals (SCM=1).
   b. Clock device with scan clock (CKE1).
   c. Apply consecutive serial test vectors.
   d. Read back results as new 'Test Data' (States) are applied. The first 36 outputs read at SCOUT (I/O15) are random ('old') data (e.g., remnant of Step 1).
   e. Apply 36 'Test Data' until the chain is full.
4. To apply 'Test Data' (States), exit Scan Mode and apply on system clock together with any other possible test vectors.
5. To read result of the state transition, re-enter scan and apply the scan clock (CKE1). The result of the state transition in JKCL9 will be available at SCOUT (I/O15) after 36 clocks. The results can be stored in a user defined test memory buffer in inverted logic representation.
6. As the results are being read and stored, new 'Test Data' can be entered via SCI.
7. Repeat for all test patterns of interest.
8. Figure 3 (FLOW_CHART) depicts a flow chart version of the test sequence.



NOTE:
1. The first 36 outputs are random ('OLD') data.

Figure 3. FLOW_CHART

A Simple Example

Assume the last three cells of the scan chain (JKCL9, JKCL8, JKCL7 in Figure 4 contain a 3-bit up counter. Our test vector will be a single clock applied to the counter. Suppose we wish to first check the *State 5* (i.e., 101) to *State 6* (i.e., 110) transition, then the *State 3* (i.e., 011) to *State 4* (i.e., 100) transition. Assume the scan chain has been pre-verified and we may begin.

Enter scan mode (set SCM=1)l apply 36 bits in sequence so that the value *101* (i.e., State 5) resides in the last three cells. Exit scan mode (set SCM=0) and apply a single clock to the counter. Now the value *110* (i.e., State 6) resides in the last three cells. Re-enter scan mode (set SCM=1) and read back 36 bits from position I/O15. Note that the outputs are complemented and are also read back in the reverse order. Therefore the value for *STATE 6* read at I/O15 will be 100 which is the complement of *STATE 6* (110) read in the reverse order.

As this is being read back, apply a new state, serially equal to the value *011* (i.e., State 3). This state should be loaded on the last three clock cycles during which *STATE 6* is being read back at I/O15. After *STATE 3* has been loaded (and *STATE 6* read back), exit scan mode and apply a single clock which will invoke the *STATE 3* (i.e., 011) to *STATE 4* (i.e., 100) transition. Re-enter scan mode and read back 36 bits at I/O15. The last three bits should contain *110* which is the complement of *State 4* read in the reverse order. Figure 4 (SCAN_EXAMPLE) shows a flow diagram of this example. Note that the States will always be complemented and read back in the reverse at I/O15. Other sequences may be applied in the same manner.

A possible alternative to this example is to read back the output states at I/O0 (D0) instead of I/O15 (JKCL9). This will allow the outputs to be read back after 21 clock cycles rather than the 36 used in the above example.

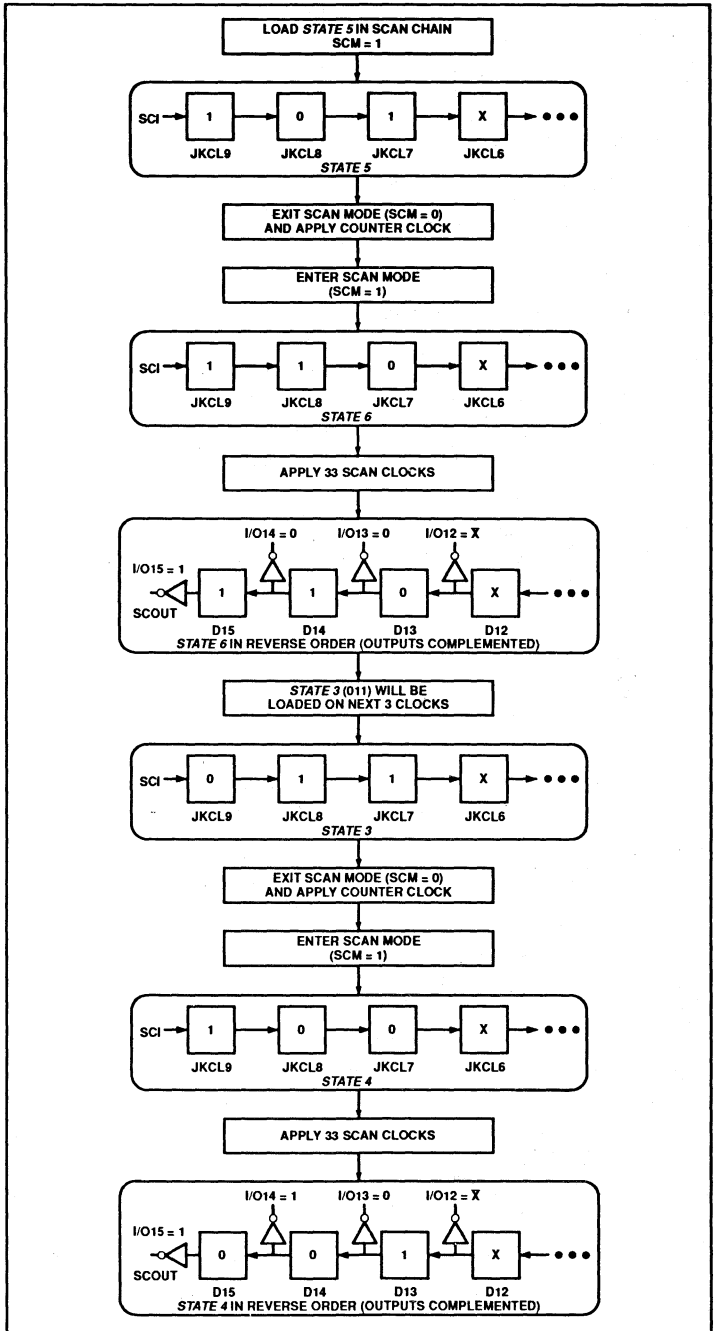


Figure 4. SCAN_EXAMPLE

POWER DOWN

The PML2552 offers the user controlled capability of putting the device to "sleep" where power dissipation is reduced to very low levels. When brought to a logic "1", the PD pin freezes the circuit while reducing the power. All data is retained. This not only includes that of the registers, but also the state of each foldback gate. For those cases where it is desirable to 3-State the outputs, that can be accomplished by raising the SCI pin to a logic "1".

There is one point that should be noted while the circuit is in its power-down mode. The switching of any external clock pin will cause a disruption of the data. All clocks must be frozen before the circuit goes into power-down and stay that way until it powered back up. Clocks that are internally generated and feed the clock array are automatically stopped by the power-down circuitry. Any other input can toggle without any loss of data.

NOTE:
1. During power down, external clocks (CKA, CKB/CKC, CKE1, CKE2) should not change.
2. SCM must be "0" as in normal operation mode.
3. External clock recovery time (low-to-high) is 60ns (high-speed) and 70ns (standard) after the device is powered up.
4. Power Down Timing Diagrams on pages 17 and 18 are for combinatorial operation only.

DEVELOPMENT TOOLS

The PM2552 is supported by the Signetics SNAP software development package and a multitude of hardware and software development tools. These include industry standard PLD programmers and CAD software.

SNAP

Features

- Schematic entry using DASH™ 4.0 or above or OrCAD™ SDT III
- State Equation Entry
- Boolean Equation Entry
- Allows design entry in any combination of above formats
- Simulator
  - Logic and fault simulation
  - Timing model generation for device timing simulation
  - Synthetic logic analyzer format
- Macro library for standard TTL and user defined functions
- Device independent netlist generation
- JEDEC fuse map generated from netlist

SNAP (Synthesis, Netlist, Analysis and Program) is a versatile development tool that speeds the design and testing of PML. SNAP combines a user-friendly environment and powerful modules that make designing with PML simple. The SNAP environment gives the user the freedom to design independent of the device architecture.

The flexibility in the variations of design entry methodologies allows design entry in the most appropriate terms. SNAP merges the inputs, regardless of the type, into a high-level netlist for simulation or compilation into a JEDEC fuse map. The JEDEC fuse map can then be transferred from the host computer to the device programer.

SNAP's simulator uses a synthetic logic analyzer format to display and set the nodes of the design. The SNAP simulator provides complete timing information, setup and hold-time checking, plus toggle and fault grading analysis.

SNAP operates on an IBM® PC/XT, PC/AT, PS/2, or any compatible system with DOS 2.1 or higher. A minimum of 640K bytes of RAM is required together with a hard disk.

SLICE

SLICE, which supports Signetics PLD line, is easy to understand and simple to use. Select a PLD, assign input and output pins and enter the desired equations in either Boolean or state form. SLICE then checks the equations for errors. It automatically generates a JEDEC-format fuse map for downloading to a PLD programmer.

Fully menu driven, SLICE incorporates a fuse table editor for making quick modifications to the design and a test vector editor for input of test vectors.

A built-in Boolean equation extractor allows existing PLDs to be used as the basis for a new design. the extractor reads JEDEC information from a PLD and creates a file containing the corresponding Boolean equations. The result can then be used to consolidate several PLD designs into a single, denser part.

And SLICE is upward compatible with Signetics extensive design suite, SNAP.

DESIGN SECURITY

The PML2552 has a programmable security fuse that controls the access to the data programmed in the device. By using this programmable feature, proprietary design implemented in the device cannot be copied or retrieved.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_{OUT}	Output voltage	+5.5	V_{DC}
I_{IN}	Input currents	–30 to +30	mA
I_{OUT}	Output currents	+100	mA
T_{amb}	Operating temperature range	0 to +75	°C
T_{stg}	Storage temperature range	–65 to +150	°C

NOTE:
1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

DASH is a trademark of Data I/O Corporation.
OrCAD is a trademark of OrCAD, Inc.
IBM is a registered trademark of International Business Machines Corporation.

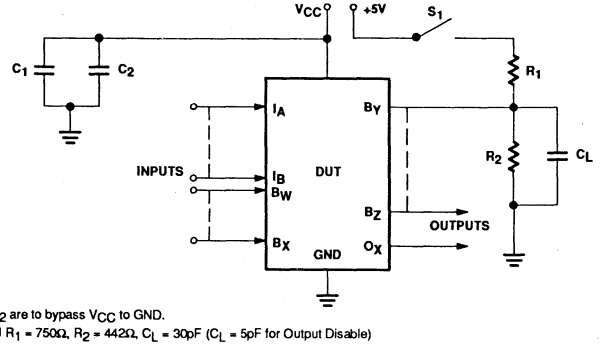
DC ELECTRICAL CHARACTERISTICS

$0°C \le T_{amb} \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS MIN	LIMITS TYP[1]	LIMITS MAX	UNIT
Input voltage							
V_{IL}	Low	V_{CC} = MIN		–0.3		0.8	V
V_{IH}	High	V_{CC} = MAX		2.0		V_{CC} + 0.3	V
Output voltage							
V_{OL}	Low	V_{CC} = MIN, I_{OL} = 5mA				0.45	V
V_{OH}	High	V_{CC} = MIN, I_{OH} = –2mA		2.4			V
Input current							
I_{IL}	Low	V_{IN} = GND				–10	µA
I_{IH}	High	V_{IN} = V_{CC}				10	µA
Output current							
$I_{O(OFF)}$	Hi-Z state	V_{OUT} = V_{CC}				10	µA
		V_{OUT} = GND				–10	µA
I_{OH}	Output High	V_{CC} = MIN, V_{OUT} = 2.4V				–2	mA
I_{OL}	Output Low	V_{CC} = MIN, V_{OUT} = 0.45V				5	mA
I_{OS}	Short-circuit[5]	V_{OUT} = GND				–100	mA
I_{CC}	V_{CC} supply current	V_{CC} = MAX, No load	CMOS input[2]		60	100[6]	mA
		f = 1MHz	TTL input[3]		65	120[6]	mA
I_{SB}	Standby V_{CC} supply current	V_{CC} = MAX, No load	CMOS input		1.0	10	mA
		PD = V_{IH}	TTL input		1.5	10	mA
Capacitance							
C_{IN}	Input	V_{CC} = 5V, T_{amb} = +25°C, V_{IN} = 2.0V			8		pF
C_B	I/O	V_{CC} = 5V, T_{amb} = +25°C, V_{IO} = 2.0V			16		pF

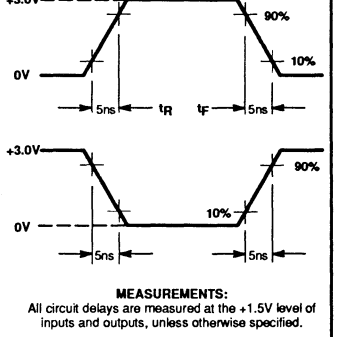
NOTES:
1. All typical values are at V_{CC} = 5V, T_{amb} = +25°C.
2. CMOS inputs: V_{IL} = GND, V_{IH} = V_{CC}.
3. TTL inputs: V_{IL} = 0.45V, V_{IH} = 2.4V.
4. All voltage values are with respect to network ground terminal.
5. Duration of short-circuit should not exceed one second. Test one at a time.
6. ΔI_{CC} vs. Frequency = 4mA/MHz max.

TEST LOAD CIRCUITS



NOTES:
C_1 and C_2 are to bypass V_{CC} to GND.
Test Load R_1 = 750Ω, R_2 = 442Ω, C_L = 30pF (C_L = 5pF for Output Disable)
$0°C \le T_{amb} \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

VOLTAGE WAVEFORMS



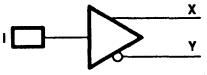
MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

MACRO CELL AC SPECIFICATIONS

Min: 0°C, 5.25V; Typ: 25°C, 5.0V; Max: 75°C, 4.75V (SNAP Resource Summary Designations in Parentheses)

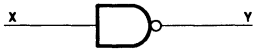
Input Buffer
(DIN552, NIN552, BDIN55, BNIN552
CDIN552, CNIN552, CKDIN552, CKNIN552, IDFF552*)



SYMBOL	PARAMETER		LIMITS						UNIT
	To	From	PML2552-35			PML2552-50			
	(Output)	(Input)	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	X	I	5	7	10	7	10	15	ns
t_{PLH}	X	I	5	7	10	7	10	15	ns
t_{PHL}	Y	I	5	7	10	7	10	15	ns
t_{PLH}	Y	I	5	7	10	7	10	15	ns

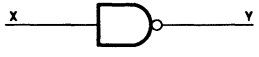
* When D flip-flop is bypassed.
Input Pins: 8–14, 16, 17, 20, 22–24.
Bidirectional Pins: 1–3, 5–7, 46–48, 50–54, 57–64, 67, 68.
Bypassed D flip-flop at pins 26, 28–31, 33–35, 37, 39–45.

Internal NAND of Main Array
(FBNAND, NAND)



SYMBOL	PARAMETER		LIMITS			LIMITS			UNIT
	To	From	PML2552-35			PML2552-50			
	(Output)	(Input)	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Y	X	10	15	20	12	18	25	ns
t_{PLH}	Y	X	10	15	20	12	18	25	ns

Internal NAND of Clock Array
(NAND)

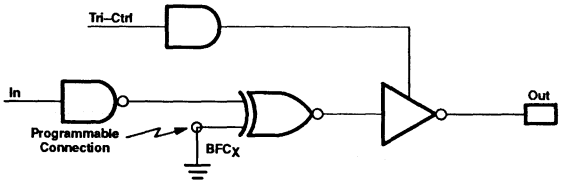


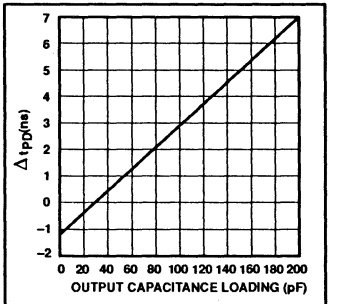
SYMBOL	PARAMETER		LIMITS			LIMITS			UNIT
	To	From	PML2552-35			PML2552-50			
	(Output)	(Input)	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Y	X	5	7	10	7	10	15	ns
t_{PLH}	Y	X	5	7	10	7	10	15	ns

MACRO CELL AC SPECIFICATIONS (Continued)

Min: 0°C, 5.25V; Typ: 25°C, 5.0V; Max: 75°C, 4.75V (SNAP Resource Summary Designations in Parentheses)

3-State Output with Programmable Polarity (TOUT552 + EXOR552)



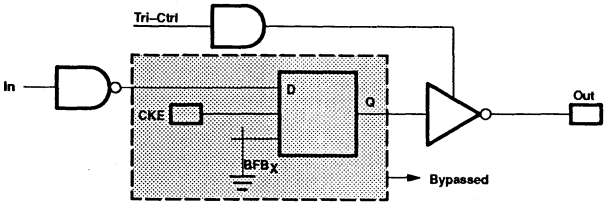


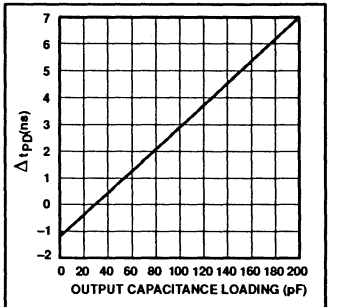
ΔtPD vs Output Capacitance Loading (Typical)

SYMBOL	PARAMETER		LIMITS						UNIT
	To (Output)	From (Input)	PML2552-35			PML2552-50			
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Out	In	12	18	25	17	25	35	ns
t_{PLH}	Out	In	12	18	25	17	25	35	ns
t_{OE}[4]	Out	Tri-Ctrl	5	7	10	7	10	15	ns
t_{OD}[4]	Out	Tri-Ctrl	5	7	10	7	10	15	ns

Bidirectional Pins: 46–48, 50–54.

I/O Output Buffer with 3-State Control, DFF Bypassed (TOUT552 + NAND)





ΔtPD vs Output Capacitance Loading (Typical)

SYMBOL	PARAMETER		LIMITS						UNIT
	To (Output)	From (Input)	PML2552-35			PML2552-50			
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Out	In	12	18	25	17	25	35	ns
t_{PLH}	Out	In	12	18	25	17	25	35	ns
t_{OE}[4]	Out	Tri-Ctrl	5	7	10	7	10	15	ns
t_{OD}[4]	Out	Tri-Ctrl	5	7	10	7	10	15	ns

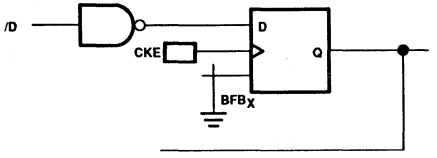
I/O Pins: 1–3, 5–7, 57–64, 67, 68.

lotes on page 483.

MACRO CELL AC SPECIFICATIONS (Continued) (SNAP Resource Summary Designations in Parentheses)

D FLIP-FLOP

Output DFF Used Internally (ODFF552)



SYMBOL	PARAMETER	LIMITS						UNIT
		PML2552-35			PML2552-50			
		MIN	TYP	MAX	MIN	TYP	MAX	
f_{CKE}	Flip-flop toggle rate			50			35	MHz
$t_{W\,CKE}$ High	Clock HIGH	10			14			ns
$t_{W\,CKE}$ Low	Clock LOW	10			14			ns
t_{SETUP} /D	/D setup time to CKE	15			20			ns
t_{HOLD} /D	/D hold time to CKE	4			6			ns

SYMBOL	PARAMETER		LIMITS						UNIT
	From (Input)	To (Output)	PML2552-35			PML2552-50			
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	CKE ↑	Q	10	15	20	14	20	25	ns
t_{PHL}	CKE ↑	Q	10	15	20	14	20	25	ns

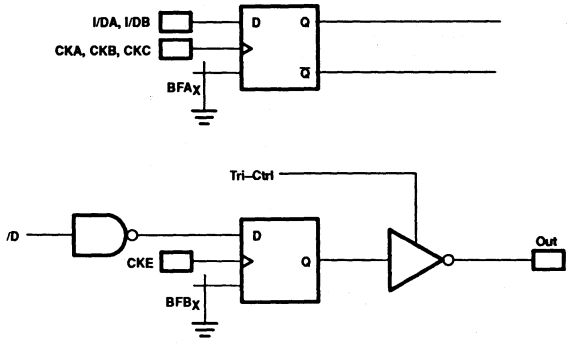
MACRO CELL AC SPECIFICATIONS (Continued) (SNAP Resource Summary Designations in Parentheses)

D FLIP-FLOP (Continued)

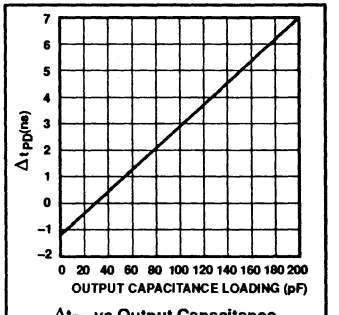
Input and Output
(IDFF552 & ODFF552)

INPUTS		OUTPUTS	
CK	D	Q	$\overline{Q}$
L	X	Q_0	$\overline{Q}_0$
↑	H	H	L
↑	L	L	H

NOTE:
Q_0, $\overline{Q}_0$ represent previous stable condition of Q, $\overline{Q}$.



SYMBOL	LIMITS						UNIT
	PML2552-35			PML2552-50			
	MIN	TYP	MAX	MIN	TYP	MAX	
$f_{CKA, CKB, CKC}$			50			35	MHz
$t_{W\ CKA, CKB, CKC}$ High	10			14			ns
$t_{W\ CKA, CKB, CKC}$ Low	10			14			ns
t_{SETUP} I/DA, I/DB	5			7			ns
t_{HOLD} I/DA, I/DB	5			7			ns
f_{CKE}			50			35	MHz
$t_{W\ CKE}$ High	10			14			ns
$t_{W\ CKE}$ Low	10			14			ns
t_{SETUP} /D	15			20			ns
t_{HOLD} /D	4			6			ns



Δt_{PD} vs Output Capacitance Loading (Typical)

SYMBOL	PARAMETER		LIMITS						UNIT
	From (Input)	To (Output)	PML2552-35			PML2552-50			
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	CKA, CKB/CKC ↑	Q, $\overline{Q}$	5	7	10	7	10	15	ns
t_{PHL}	CKA, CKB/CKC ↑	Q, $\overline{Q}$	5	7	10	7	10	15	ns
t_{PLH}	CKE ↑	Out	12	18	25	17	25	35	ns
t_{PHL}	CKE ↑	Out	12	18	25	17	25	35	ns

MACRO CELL AC SPECIFICATIONS (Continued) (SNAP Resource Summary Designations in Parentheses)

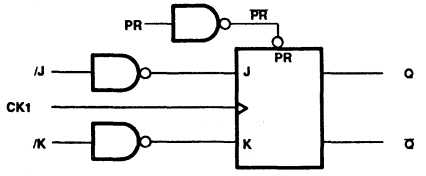
JK FLIP-FLOPS

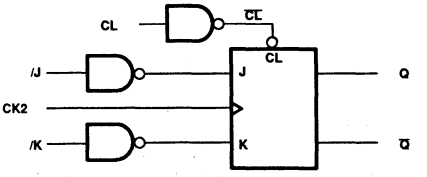
(JKPR552)

INPUTS				OUTPUTS	
$\overline{PR}$	CK	J	K	Q	$\overline{Q}$
L	X	X	X	H	L
H	↑	L	L	Q_0	$\overline{Q}_0$
H	↑	H	L	H	L
H	↑	L	H	L	H
H	↑	H	H	TOGGLE	
H	L	X	X	Q_0	$\overline{Q}_0$

(JKCL552)

INPUTS				OUTPUTS	
$\overline{CL}$	CK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↑	L	L	Q_0	$\overline{Q}_0$
H	↑	H	L	H	L
H	↑	L	H	L	H
H	↑	H	H	TOGGLE	
H	L	X	X	Q_0	$\overline{Q}_0$





SYMBOL	PARAMETER	LIMITS						UNIT
		PML2552-35			PML2552-50			
		MIN	TYP	MAX	MIN	TYP	MAX	
f_{CK1}	CK1 toggle frequency			50			35	MHz
f_{CK2}	CK2 toggle frequency			50			35	MHz
$t_{W\,CK1}$ High	CK1 clock HIGH	10			14			ns
$t_{W\,CK1}$ Low	CK1 clock LOW	10			14			ns
$t_{W\,CK2}$ High	CK2 clock HIGH	10			14			ns
$t_{W\,CK2}$ Low	CK2 clock LOW	10			14			ns
t_{SETUP} /J, /K	/J, /K setup time to CK1, CK2	27			35			ns
t_{HOLD} /J, /K	/J, /K hold time to CK1, CK2	0			0			ns
t_W PR Low	Preset Low period	10			14			ns
t_W CL Low	Clear Low period	10			14			ns

SYMBOL	PARAMETER		LIMITS						UNIT
	From (Input)	To (Output)	PML2552-35			PML2552-50			
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	CK1,2	Q, $\overline{Q}$	2	3.5	5	3	5	7	ns
t_{PHL}	CK1,2	Q, $\overline{Q}$	2	3.5	5	3	5	7	ns
t_{PLH}	PR	Q, $\overline{Q}$	12	18	25	17	24	30	ns
t_{PHL}	PR	Q, $\overline{Q}$	12	18	25	17	24	30	ns
t_{PLH}	CL	Q, $\overline{Q}$	12	18	25	17	24	30	ns
t_{PHL}	CL	Q, $\overline{Q}$	12	18	25	17	24	30	ns

AC ELECTRICAL CHARACTERISTICS

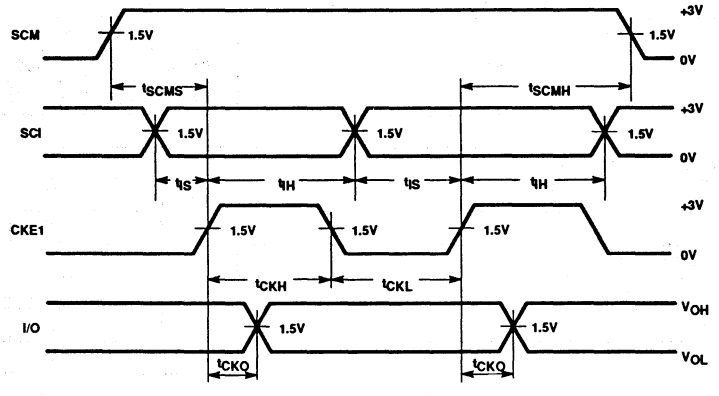
)°C ≤ T_{amb} ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V, V_{PP} = V_{CC},
R_1 = 750Ω, R_2 = 442Ω, C_L = 5pF for Output Disable) (See Test Load Circuit Diagram)

SYMBOL	PARAMETER	LIMITS				UNIT
		PML2552-35		PML2552-50		
		MIN	MAX	MIN	MAX	
Scan mode operation[1]						
t_{SCMS}	Scan Mode (SCM) Setup time	15		15		ns
t_{SCMH}	Scan Mode (SCM) Hold time	25		30		ns
t_{IS}	Data Input (SCI) Setup time	5		5		ns
t_{IH}	Data Input (SCI) Hold time	5		5		ns
t_{CKO}	Clock to Output (I/O) delay		30		40	ns
t_{CKH}	Clock High	10		15		ns
t_{CKL}	Clock Low	10		15		ns
Power down, power up[2]						
t_1	Input (I, bypassed I/DA, I/DB, I/O, B) setup time before power down	40		50		ns
t_2	Input hold time	30		35		ns
t_3	Power Up recovery time		60		70	ns
t_4	Output hold time	0		0		ns
t_5	Input setup time before Power Up	20		25		ns
t_{OE}	SCI to Output Enable time[3]		40		50	ns
t_{OD}	SCI to Output Disable time[3]		40		50	ns
t_6	Power Down setup time	10		15		ns
t_7	Power Up to Output valid		70		80	ns
Power-on reset						
t_{PPR1}	Power-on reset output register (Q = 0) to output (I/O) delay		10		15	ns
t_{PPR2}	Power-on reset input register (Q = 0), buried JK Flip-Flop (Q = 0) to output (B, bypassed I/O) delay		40		50	ns

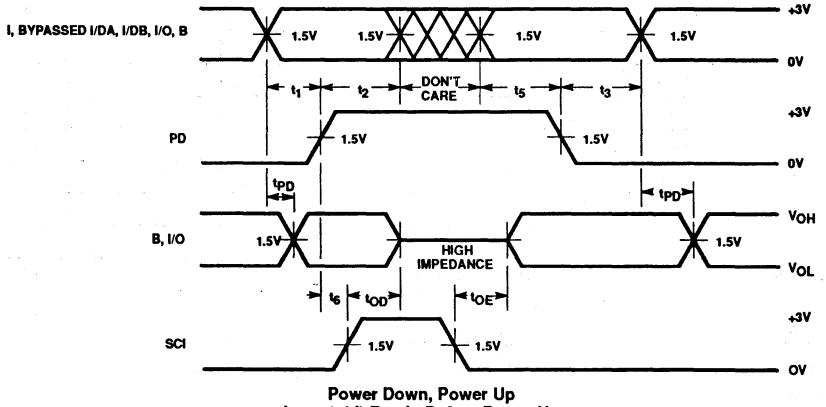
IOTES:

. SCM recovery time is 50ns after SCM operation. 50ns after SCM operation, normal operations can be resumed.
. Timings are measured without foldbacks.
. Transition is measured at steady state High level (–500mV) or steady state Low level (+500mV) on the output from 1.5V level on the input with specified test load (R_1 = 750Ω, R_2 = 442Ω, C_L = 5pF). This parameter is sampled and not 100% tested.
. For 3-State output; output enable times are tested with C_L = 30pF to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with C_L = 5pF. High-to-High impedance tests are made to an output voltage of V_T = (V_{OH} – 0.5V) with S_1 open, and Low-to-High impedance tests are made to the V_T = (V_{OL} + 0.5V) level with S_1 closed.

TIMING DIAGRAMS

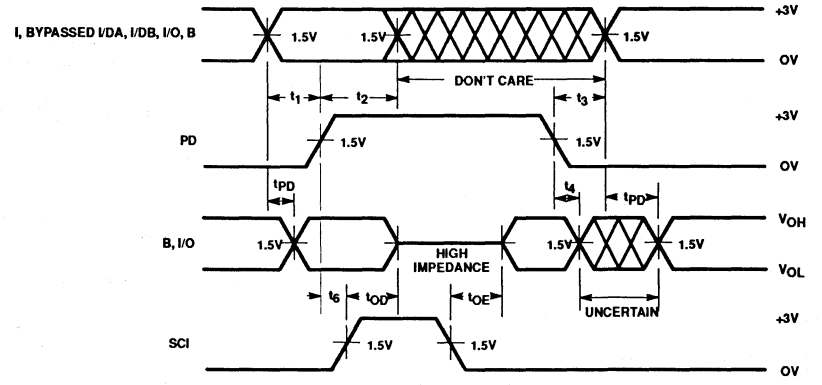


Scan Mode Operation

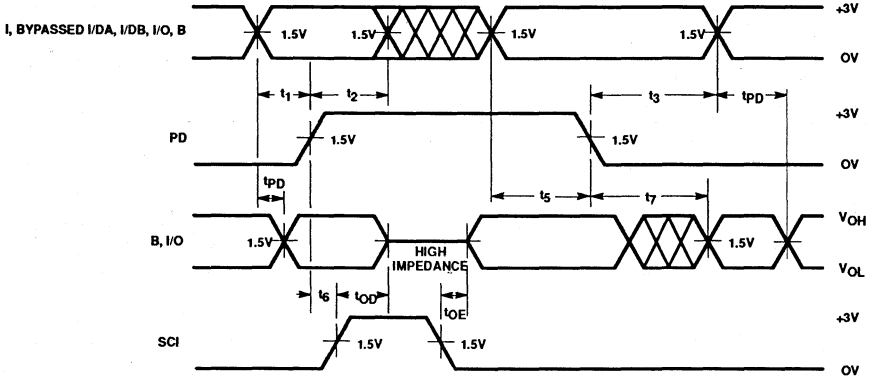


Power Down, Power Up
Input (old) Ready Before Power Up

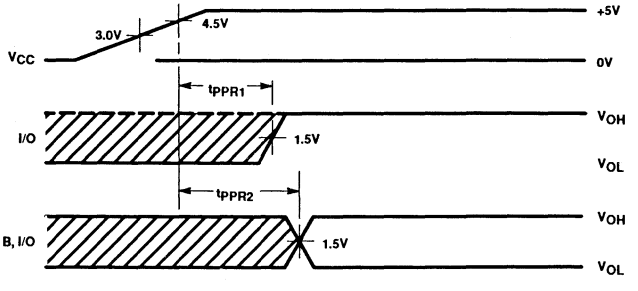
TIMING DIAGRAMS (Continued)



Power Down, Power Up
Input (new) Ready After Power Up

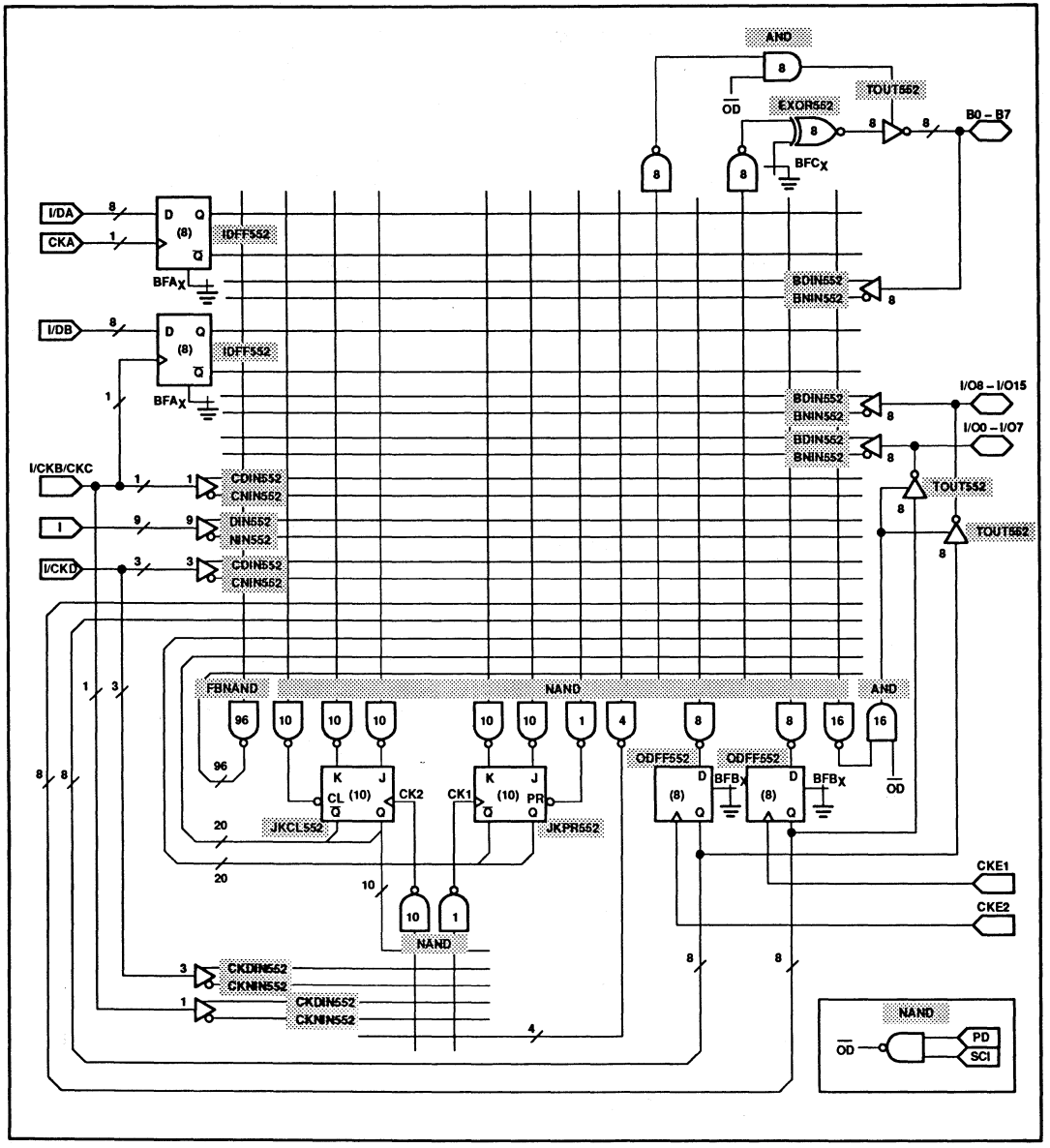


Power Down, Power Up
Input (new) Ready Before Power Up



Power-On Reset

SNAP RESOURCE SUMMARY DESIGNATIONS



ERASURE CHARACTERISTICS (For Quartz Window Packages Only)

The erasure characteristics of the PML2552 device is such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000 – 4000Å range. Data shows that constant exposure to room level fluorescent lighting could erase a typical PML2552 in approximately three years, while it would take approximately one week to cause erasure when exposed to direct sunlight. If the PML2552 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure for the PML2552 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15Wsec/cm^2. The erasure time with this dosage is approximately 30 to 35 minutes using an ultraviolet lamp with a 12,000µW/cm^2 power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose a CMOS EPLD can be exposed to without damage is 7258Wsec/cm^2 (1 week @ 12,000µW/cm^2). Exposure of these CMOS EPLDs to high intensity UV light for longer periods may cause permanent damage.

The maximum number of guaranteed erase/write cycles is 50. Data retention exceeds 20 years.

PROGRAMMING

Refer to the following charts for qualified manufacturers of programmers and software tools:

PROGRAMMER MANUFACTURER	PROGRAMMER MODEL	FAMILY/PINOUT CODES
DATA I/O CORPORATION 10525 WILLOWS ROAD, N.E. P.O. BOX 97046 REDMOND, WASHINGTON 98073–9746 (800)247–5700	UNISITE 40/48 V2.8 Pinsite – V2.0	15908C* (with adaptor) 15908D (with pinsite)
STREBOR DATA COMMUNICATIONS 1008 N. NOB HILL AMERICAN FORK, UTAH 84003	PLP–S1A Programmer MP68CC Adaptor	
BASIC COMPUTER SYSTEMS AG WOLFGANG-PAULI-GASSE A-1140 WIEN-AUHOF, AUSTRIA	UP2000 Rev. 2.25	
SMS – W. STEUDEL IM MORGENTAL 13 D-8994 HERGATZ, GERMANY	SPRINT PLUS/EXPERT Rev. 4/91	
SYSTEM GENERAL 244 SOUTH PARK VICTORIA DRIVE MILPITAS, CALIFORNIA 95035	TURPRO-1 Rev. 1.42	

* Needs a 40-pin DIP to 68-pin PLCC adaptor that is available from Emulation Technology.
Part Number: AS–68–40–04P–6

EMULATION TECHNOLOGY, INC.
2368B Walsh Avenue, Building D
Santa Clara, California 95051
Telephone No. (408) 982–0660
Fax. No. (408) 982–0664

SOFTWARE MANUFACTURER	DEVELOPMENT SYSTEM
SIGNETICS COMPANY 811 EAST ARQUES AVENUE P.O. BOX 3409 SUNNYVALE, CALIFORNIA 94088–3409 (408)991–2000	SNAP SOFTWARE REV. 1.4 AND LATER

CMOS high density programmable macro logic — PML2852

FEATURES

- Wide gates for efficient product term use
- Multiple I/O pins for 16–32 bit buses or up to 32-bit data flow
- Multiple I/O pins for multiple-port data handling
- Multiple clocks for independent state machines and storage banks
- 100% connectible, no place and route restrictions
- Erasable and one time programmable versions available
- Scan test
- Low CMOS power dissipation = 525mW max.
- Power down mode (52mW max.)
- Power on reset
- Security fuse for copy protection
- Supported by advanced SNAP and SLICE development systems

PERFORMANCE

- 35ns max. pin-to-pin for 32-bit decoders
- 40ns max. internal, 55ns max. pin-to-pin for 16-bit multiplexers
- 33MHz max. throughput for 16-bit latches
- 18–50MHz max. for 10-bit counters
- 31MHz max. for 10-bit shift registers
- 15ns (typ.) delay for internal NANDs
- 50MHz max. flip-flop toggle rate

APPLICATIONS

- Bus interface and control (microchannel, VME, NuBus, etc.)
- Microcomputer peripheral interface and control (printers, SCSI, hard disk drives, etc.)
- Multiport memory control and arbitration (cache, DRAM, VRAM, etc.)
- Intelligent instrumentation (data acquisition, testers, medical equipment, etc.)
- Industrial control (process control, motor control, engine control, etc.)
- Communication network control (LAN, Ethernet, T1, TDMA, etc.)
- General purpose logic integration
- Laptops, pocket computers, and handheld instruments
- Low-end gate array replacement for quick prototyping

SNAP DEVELOPMENT SYSTEM

- Supports third-party schematic entry formats
- Versatile EDIF-compatible netlist format for design portability
- TTL macro library for automatic mapping
- Logic, timing, and fault simulation
- Automatic test vector generator
- Espresso logic minimizer
- Boolean equation extractor from JEDEC fusemap

SLICE DEVELOPMENT SYSTEM

- Easy to learn and use
- State or Boolean equation entry
- Fusetable editor
- Test vector editor
- Boolean equation extractor
- JEDEC fusemap compiler
- Upward compatible with SNAP

DESCRIPTION

The Signetics family of Programmable Macro Logic is optimized for handling wide buses, wide datapaths, and multiple-port applications with the highest throughputs among high density PLDs and FPGAs. The PML2852 now expands Signetics CMOS PML product offering into the 32-bit arena. Fabricated with a high-performance EPROM process, the PML2852 is ideal in today's bus interface control, microprocessor peripheral control, memory interface, communications, instrumentation, and industrial control. It is capable of replacing large amounts of TTL SSI and MSI logic, and literally integrates a complete custom microcontroller.

The PML2852 incorporates the folded NAND array architecture, which provides 100% connectivity to eliminate the routing restrictions associated with other high density PLD/FPGA architectures. The array of wide-input NAND gates enables the designer to implement any wide-gate logic function, from decoders to multiplexers, with no more than two gate-level delays. It also allows implementation of multiple levels of logic within the chip, without wasting I/O pins. Its flexible and potent flip-flop building blocks provide for high throughput data storage, high speed state machines, and fast counters.

The PML2852 also incorporates two unique features: scan test and power down. With user-controlled scan test, the PML2852 significantly reduces system functional test time by providing access to all of its internal registers. In the user-controlled power down mode, the PML2852 power dissipation is reduced to a mere 52mW, making it ideal for laptop or pocket computers and handheld instruments.

Thanks to its high density and its flexible architecture, the PML2852 provides **instant gate array** capabilities for all general purpose logic integration. As such, the PML2852 eliminates the NRE costs, risks, inventory problems, and hard to use design tools associated with semicustom and full custom approaches. It allows the designer to quickly bring concepts to silicon for faster learning cycles and a much shorter time to market. Functional prototypes are available within minutes.

The SNAP development software is designed to fully exploit the flexibility and density of the PML2852. It accepts a variety of design entry formats, including schematic, logic equations, and state equations in any combination for maximum flexibility. Its powerful features, but ease of use, allows literally push-button operation.

Together, the PML2852 and SNAP constitute the designer's personal **desktop silicon foundry**.

NuBus is a trademark of Texas Instruments, Inc.

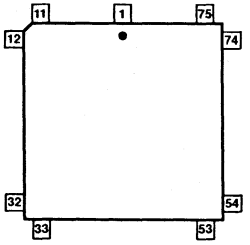
CMOS high density programmable macro logic — PML2852

)RDERING INFORMATION

DESCRIPTION	t_{PD} (MAX)	ORDER CODE
84-pin Plastic Leaded Chip Carrier	35ns	PML2852-35A
84-pin "J" Leaded Ceramic Cerquad Package	35ns	PML2852-35KA
84-pin Plastic Leaded Chip Carrier	50ns	PML2852-50A
84-pin "J" Leaded Ceramic Cerquad Package	50ns	PML2852-50KA

'IN CONFIGURATION

A and KA Packages



'in	Function	Pin	Function	Pin	Function
1	I/O5	29	PD	57	O8
2	I/O4	30	I/DB7	58	B7
3	I/O3	31	I/DB6	59	B6
4	VCC1	32	I/DB5	60	B5
5	I/O2	33	VCC5	61	VSS3
6	I/O1	34	I/DB4	62	B4
7	I/O0	35	I/DB3	63	B3
8	O3	36	I/DB2	64	B2
9	O2	37	I/DB1	65	B1
10	O1	38	I/DB0	66	B0
11	O0	39	I/DA7	67	VCC4
12	I8	40	VSS2	68	CKE2
13	I7	41	I/DA6	69	I/O15
14	I6	42	I/DA5	70	I/O14
15	I5	43	I/DA4	71	O7
16	I4	44	CKA	72	O6
17	I3	45	I/DA3	73	O5
18	I2	46	VCC3	74	O4
19	VSS1	47	I/DA2	75	I/O13
20	I1	48	I/DA1	76	I/O12
21	I0	49	I/DA0	77	I/O11
22	SCM	50	O15	78	I/O10
23	SCI	51	O14	79	I/O9
24	I/CKD3	52	O13	80	I/O8
25	VCC2	53	O12	81	CKE1
26	I/CKD2	54	O11	82	VSS4
27	I/CKD1	55	O10	83	I/O7
28	I/CKB/CKC	56	O9	84	I/O6

FUNCTIONAL BLOCK DIAGRAM

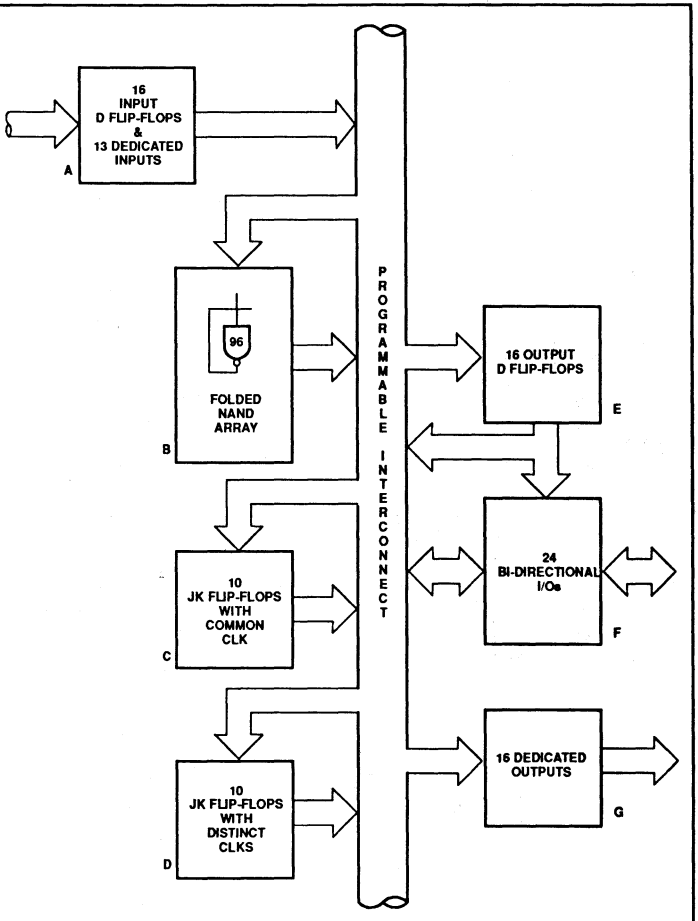
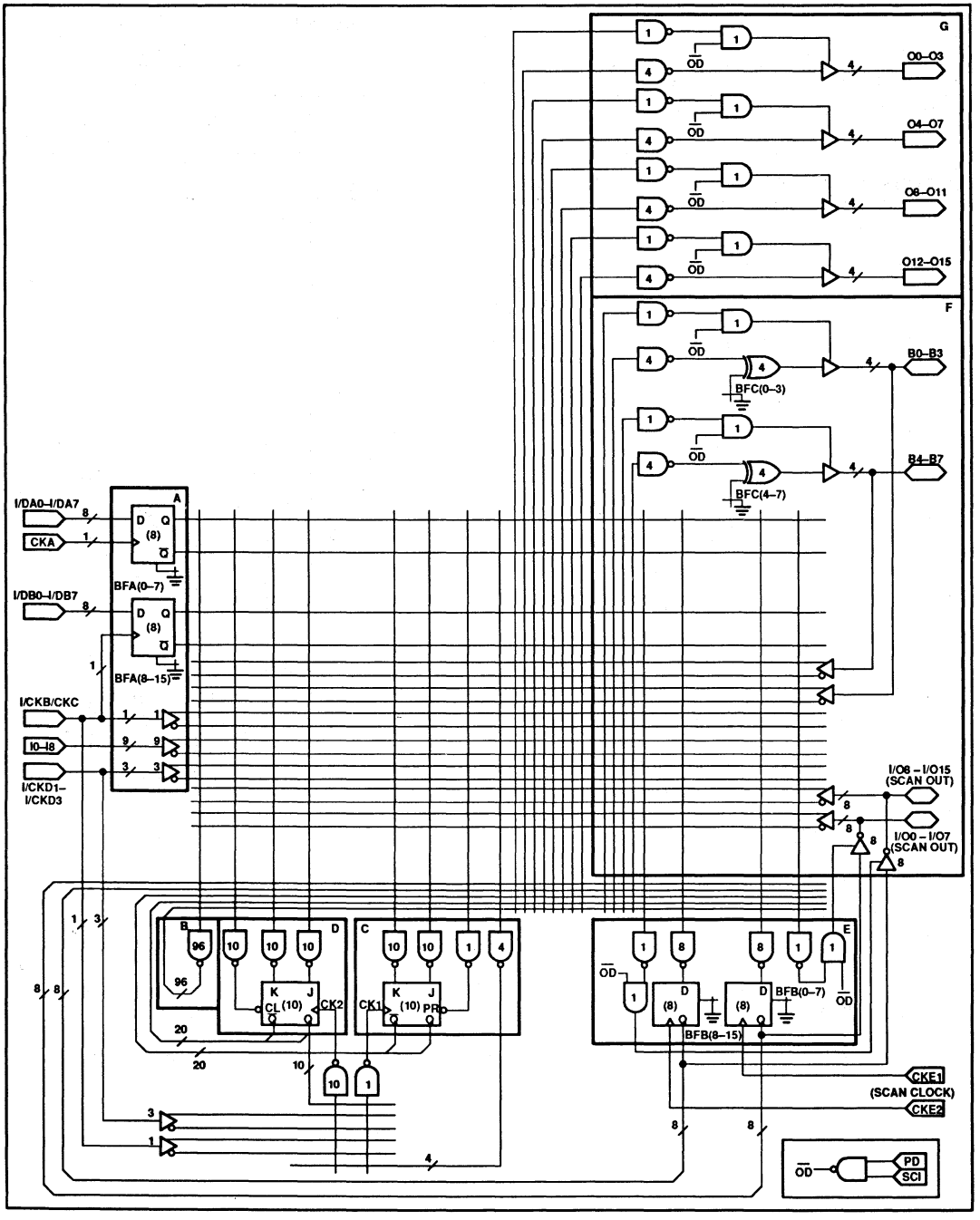


Figure 1.

LOGIC DIAGRAM



CMOS high density programmable macro logic | PML2852

STRUCTURE

- 112 possible foldback NAND gates:
  - 96 internal NAND
  - 16 from the I/O macros
- 114 additional logic terms
- 53 possible inputs (with programmable polarity)
  - 29 dedicated inputs
  - 24 bidirectional I/Os
- 24 bidirectional pins
- 16 dedicated output pins
- 52 flip-flops
- 40 possible outputs with Output Enable control (8 with programmable polarity)
- Multiple independent clocks
- 20 Buried JK-type flip-flops with foldback (JKFFs):
  - 10 JKFFs with one shared preset signal and one shared clocked signal originating from the clock array.
  - 10 JKFFs with 10 independent clock signals originating from the clock array and 10 independent clear signals
- 258 inputs per NAND gate
- Bypassable Input D-type flip-flop (DFFs)/Combinatorial Inputs:
  - 16 DFFs/combinatorial inputs
  - DFFs clocked in two groups of eight
  - DFFs not bypassed in unprogrammed state
  - Independent bypass fuse on each DFF
- Inputs/bypassable D-type flip-flop outputs/foldback NAND gates:
  - 16 output DFFs/combinatorial inputs/outputs with individual Output Enable control
  - DFFs clocked in two groups of eight
  - DFFs not bypassed in unprogrammed state
  - Independent bypass fuse on each DFF
  - The DFF can be used as an internal DFF or an internal foldback NAND gate.
- Combinatorial inputs:
  - 9 dedicated inputs to the NAND array
  - 3 inputs optional to NAND array and/or clock array
  - 1 input optional to NAND array and/or clock array, and/or clock of Input D Flip-Flops (Group B)
- Separate clock array:
  - Separate clock array for JKFFs clock inputs
  - 4 inputs to clock array originated from NAND array
  - 4 inputs (with programmable polarity) directly from input pins
  - 10 inputs from Q outputs of JKFFs with clear
- Dedicated clocks:
  - One dedicated clock for input DFFs (Group A)
  - Two dedicated clocks for output DFFs (Group E)
- Scan test feature:
  - Scan chain is implemented through the 20 buried JKFFs and 16 output DFFs
  - Pins SCI, SCM, and CKE1 are used to operate the scan test
- Power down mode
  - Dedicated pin (PD) freezes the circuit when brought to logic "1". The circuit remains in the same state prior to the logic "0" to logic "1" transition of the "PD" pin.
  - When in the power down mode, the SCI pin acts as the 3-State pin for the 40 outputs.
- Power on reset:
  - All flip-flops (16 input DFFs, 20 buried JKFFs, and 16 output DFFs) are reset to logic "0" after V_{CC} power on.

ARCHITECTURE

The core of the PML2852 is a programmable NAND array of 96 NAND gates and 20 buried JKFFs. The output of each NAND gate folds back upon itself and all other NAND gates and flip-flops. The 'Q' and '$\overline{Q}$' output of each flip-flop also folds back in the same manner. Thus, total connectivity of all logic functions is achieved in the PML2852. Any logic function can be created within the core without wasting valuable I/O pins. Furthermore, a speed advantage is acquired by implementing multi-level logic within a fast internal core without incurring any delays from the I/O buffers. Figure 1 shows the functional block diagram of the PML2852.

Macro Cells

There are 16 bypassable DFFs on the input to the NAND array. These flip-flops are split in two banks of 8 (Bank A and Bank B). Each bank of flip-flops has a common clock. In the unprogrammed state of the device the flip-flops are active. In order to bypass any DFF, its respective bypass fuse (BFA_X) must be programmed.

The 16 I/O pins (IO_0 - IO_{15}) and their respective D flip-flop macros can be used in any one of the following configurations:

1. As combinatorial input(s):
   Each of the 16 3-State outputs can be individually disabled by the associated NAND term and the pin is used as an inverting or non-inverting input.
2. As registered DFF outputs:
   These DFFs are split into two banks of 8, and each bank is clocked separately. The bypass fuse BFB_X (see PML2552 Logic Diagram) is used to bypass any one of these DFFs. The flip-flops are all active in an unprogrammed device.
3. As combinatorial outputs:
   By programming the bypass (BFB_X) fuse of any one of the DFFs, the flip-flop(s) is bypassed. The I/O pin can then be used as a combinatorial output.
4. As Internal foldback DFFs or foldback NAND gates:
   When the I/O pin is used as an input, the output macro can be used as a buried DFF or a foldback NAND term. If the bypass fuse is programmed, the macro will act as a foldback NAND term. Otherwise it will act as a buried DFF.

The 8 bidirectional pins (B0-B7) can be used as either combinatorial inputs or outputs with programmable polarity. The Exclusive-OR polarity gates are non-inverting in the unprogrammed state.

The NAND signal labeled '$\overline{OD}$' (Output Disable) shown on the PML2852 logic diagram is used for the Power Down mode operation. This signal disables the outputs when the device enters the Power Down mode and SCI is high.

Clock Array

The 20 buried JKFFs are clocked through the 'Clock Array'. The Clock Array consists of 11 NAND terms. Ten of these terms are connected to the clock inputs of the Bank A flip-flops that can be clocked individually. One NAND gate is connected to Bank B flip-flops that have a common clock. There are 18 inputs to the clock array. Four come directly from the input pins (with programmable polarity), 4 inputs are from 4 NAND gates connected directly to the folded NAND array. 10 inputs are from the Q outputs of the JKFFs with clear.

SCAN TEST FEATURE

With the rise in the ratio of devices on a chip to the number of I/O pins, Design For Testability is becoming an essential factor in logic design methodology. The PML2852 incorporates a variable length scan test feature which permits access to the internal flip-flop nodes without requiring a separate external I/O pin for each node accessed. Figure 2 (Scan Mode Operation) shows how a scan chain is implemented through the 20 buried JKFFs and 16 output DFFs. Two dedicated pins, SCI (Scan In) and SCM (Scan Mode), are used to operate the scan test. The SCM pin is used to put the circuit in scan mode. When this pin is brought to a logic "1", the circuit enters the scan mode.

In this mode it is possible to shift an arbitrary test pattern into the flip-flops. The SCI pin is used to input the pattern. The inverted outputs of flip-flops D0 - D15 are observable on pins I/O0 - I/O15.

The following are features and characteristics of the device when in Scan Mode:

1. CKE1 is the common scan-clock for all the flip-flops when in scan mode. CKE1 overrides all clock resources of normal operational mode.
2. The Preset (PR) and Clear (CL) functions of the flip-flops are disabled.
3. Scan overrides the bypass fuse of the flip-flops. This means that all the bypassable DFFs remain intact during scan operation even though they may have been bypassed during normal operation.
4. To observe the SCAN data, the output buffers must be enabled by the Output Enable (tri-ctrl) terms.
5. The outputs of the flip-flops are complemented on pins I/O0 - I/O15.
6. All external inputs to flip-flops in the scan chain are disabled when the device enters the scan mode.
7. Blowing the security fuse does not disable the Scan Test feature.

SCAN MODE OPERATION

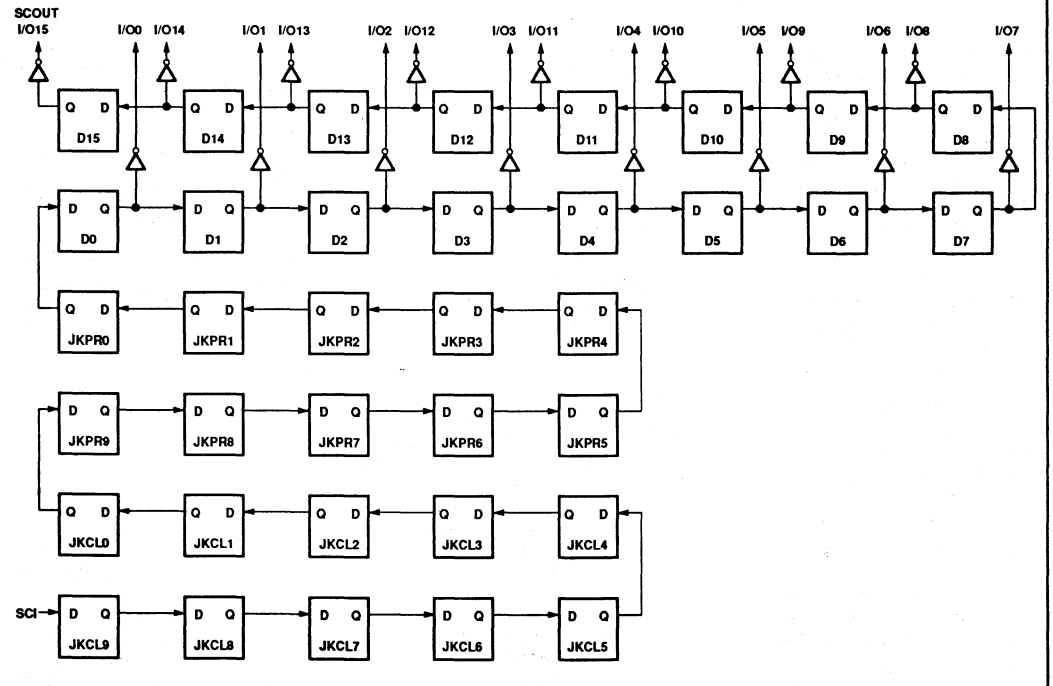


Figure 2.

SCAN TEST STRATEGY

The scan test pattern is design dependent and the user must make considerations for Design For Testability (DFT) during the initial stages of the design. A typical test sequence is to pre-load (i.e., enter a state); revert to normal operation (i.e., activate the next state transition); go back to scan mode to check the result. Note that the scan test feature available in the PML2852 is a variable length scan chain. The DATA entered at SCI (JKCL9) can be accessed anywhere between 21 clock cycles (at I/O0) to 36 clock cycles (at I/O15). For the strategy discussed here, DATA is read out after 36 clocks at I/O15 (i.e., D15). The following operation sequence suggests a possible scan test method.

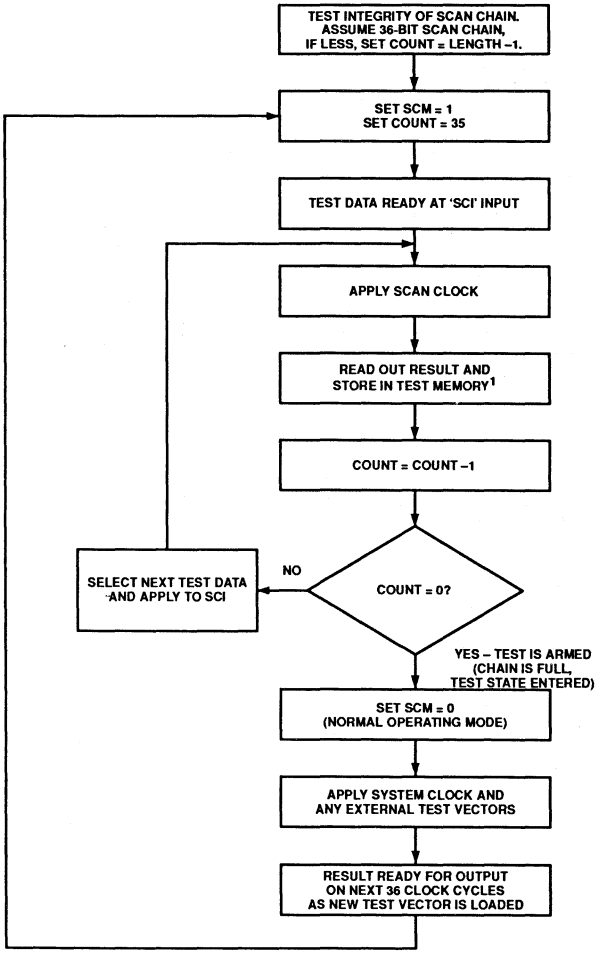
A conservative test policy demands proof that the test facility is working. Thus, to prove Scan Chain holds and maintains correct data:

a. Fill chain with several patterns (for example, all ones and all zeros).

b. Retrieve same patterns.

The user is responsible for managing an external test memory buffer for applied vectors and results, as part of the test equipment.

1. Parallel readout of I/O0 - I/O15 is possible, but assume only I/O15 is used for this strategy.
2. The first DATA entered at SCI (or JKCL9) will be the content of D15 after 36 clocks. This DATA will be inverted at the output pin I/O15 (i.e., SCOUT). The last DATA entering the scan chain will be the content of JKCL9. Thus, the scan chain resembles a first-in-first-out shift register with inverted outputs (I/O0 - I/O15).
3. 'Test Data' is read in at the SCI input and read out of the SCOUT output pin (I/O15). To enter 'Test Data':
   a. Put device in Scan Mode by applying the scan control signals (SCM=1).
   b. Clock device with scan clock (CKE1).
   c. Apply consecutive serial test vectors.
   d. Read back results as new 'Test Data' (States) are applied. The first 36 outputs read at SCOUT (I/O15) are random ('old') data (e.g., remnant of Step 1).
   e. Apply 36 'Test Data' until the chain is full.
4. To apply 'Test Data' (States), exit Scan Mode and apply on system clock together with any other possible test vectors.
5. To read result of the state transition, re-enter scan and apply the scan clock (CKE1). The result of the state transition in JKCL9 will be available at SCOUT (I/O15) after 36 clocks. The results can be stored in a user defined test memory buffer in inverted logic representation.
6. As the results are being read and stored, new 'Test Data' can be entered via SCI.
7. Repeat for all test patterns of interest.
8. Figure 3 (FLOW_CHART) depicts a flow chart version of the test sequence.



NOTE:
1. The first 36 outputs are random ('OLD') data.

Figure 3. FLOW_CHART

A Simple Example

Assume the last three cells of the scan chain (JKCL9, JKCL8, JKCL7 in Figure 4 contain a 3-bit up counter. Our test vector will be a single clock applied to the counter. Suppose we wish to first check the *State 5* (i.e., 101) to *State 6* (i.e., 110) transition, then the *State 3* (i.e., 011) to *State 4* (i.e., 100) transition. Assume the scan chain has been pre-verified and we may begin.

Enter scan mode (set SCM=1)I apply 36 bits in sequence so that the value *101* (i.e., State 5) resides in the last three cells. Exit scan mode (set SCM=0) and apply a single clock to the counter. Now the value *110* (i.e., State 6) resides in the last three cells. Re-enter scan mode (set SCM=1) and read back 36 bits from position I/O15. Note that the outputs are complemented and are also read back in the reverse order. Therefore the value for *STATE 6* read at I/O15 will be 100 which is the complement of *STATE 6* (110) read in the reverse order.

As this is being read back, apply a new state, serially equal to the value *011* (i.e., State 3). This state should be loaded on the last three clock cycles during which *STATE 6* is being read back at I/O15. After *STATE 3* has been loaded (and *STATE 6* read back), exit scan mode and apply a single clock which will invoke the *STATE 3* (i.e., 011) to *STATE 4* (i.e., 100) transition. Re-enter scan mode and read back 36 bits at I/O15. The last three bits should contain *110* which is the complement of *State 4* read in the reverse order. 4 (SCAN_EXAMPLE) shows a flow diagram of this example. Note that the States will always be complemented and read back in the reverse at I/O15. Other sequences may be applied in the same manner.

A possible alternative to this example is to read back the output states at I/O0 (D0) instead of I/O15 (JKCL9). This will allow the outputs to be read back after 21 clock cycles rather than the 36 used in the above example.

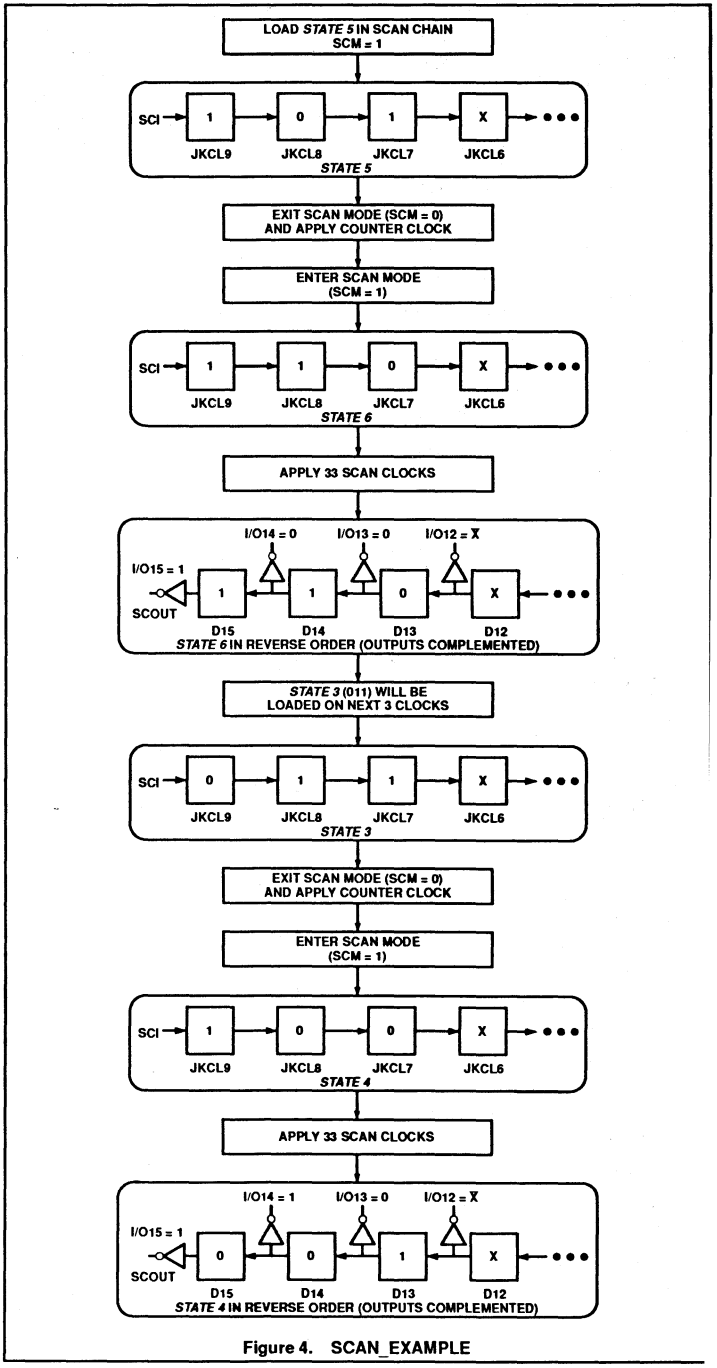


Figure 4. SCAN_EXAMPLE

POWER DOWN

The PML2852 offers the user controlled capability of putting the device to "sleep" where power dissipation is reduced to very low levels. When brought to a logic "1", the PD pin freezes the circuit while reducing the power. All data is retained. This not only includes that of the registers, but also the state of each foldback gate. For those cases where it is desirable to 3-State the outputs, that can be accomplished by raising the SCI pin to a logic "1".

There is one point that should be noted while the circuit is in its power-down mode. The switching of any external clock pin will cause a disruption of the data. All clocks must be frozen before the circuit goes into power-down and stay that way until it powered back up. Clocks that are internally generated and feed the clock array are automatically stopped by the power-down circuitry. Any other input can toggle without any loss of data.

NOTE:
1. During power down, external clocks (CKA, CKB/CKC, CKE1, CKE2) should not change.
2. SCM must be "0" as in normal operation mode.
3. External clock recovery time (low-to-high) is 60ns (high-speed) and 70ns (standard) after the device is powered up.
4. Power Down Timing Diagrams on pages 504 and 505 are for combinatorial operation only.

DEVELOPMENT TOOLS

The PM2852 is supported by the Signetics SNAP software development package and a multitude of hardware and software development tools. These include industry standard PLD programmers and CAD software.

SNAP

Features

- Schematic entry using DASH™ 4.0 or above or OrCAD™ SDT III
- State Equation Entry
- Boolean Equation Entry
- Allows design entry in any combination of above formats
- Simulator
  - Logic and fault simulation
  - Timing model generation for device timing simulation
  - Synthetic logic analyzer format
- Macro library for standard TTL and user defined functions
- Device independent netlist generation
- JEDEC fuse map generated from netlist

SNAP (Synthesis, Netlist, Analysis and Program) is a versatile development tool that speeds the design and testing of PML. SNAP combines a user-friendly environment and powerful modules that make designing with PML simple. The SNAP environment gives the user the freedom to design independent of the device architecture.

The flexibility in the variations of design entry methodologies allows design entry in the most appropriate terms. SNAP merges the inputs, regardless of the type, into a high-level netlist for simulation or compilation into a JEDEC fuse map. The JEDEC fuse map can then be transferred from the host computer to the device programer.

SNAP's simulator uses a synthetic logic analyzer format to display and set the nodes of the design. The SNAP simulator provides complete timing information, setup and hold-time checking, plus toggle and fault grading analysis.

SNAP operates on an IBM® PC/XT, PC/AT, PS/2, or any compatible system with DOS 2.1 or higher. A minimum of 640K bytes of RAM is required together with a hard disk.

SLICE

SLICE, which supports Signetics PLD line, is easy to understand and simple to use. Select a PLD, assign input and output pins and enter the desired equations in either Boolean or state form. SLICE then checks the equations for errors. It automatically generates a JEDEC-format fuse map for downloading to a PLD programmer.

Fully menu driven, SLICE incorporates a fuse table editor for making quick modifications to the design and a test vector editor for input of test vectors.

A built-in Boolean equation extractor allows existing PLDs to be used as the basis for a new design. the extractor reads JEDEC information from a PLD and creates a file containing the corresponding Boolean equations. The result can then be used to consolidate several PLD designs into a single, denser part.

And SLICE is upward compatible with Signetics advanced design suite, SNAP.

DESIGN SECURITY

The PML2852 has a programmable security fuse that controls the access to the data programmed in the device. By using this programmable feature, proprietary design implemented in the device cannot be copied or retrieved.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_{OUT}	Output voltage	+5.5	V_{DC}
I_{IN}	Input currents	–30 to +30	mA
I_{OUT}	Output currents	+100	mA
T_{amb}	Operating temperature range	0 to +75	°C
T_{stg}	Storage temperature range	–65 to +150	°C

NOTE:
1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

DASH is a trademark of Data I/O Corporation.
OrCAD is a trademark of OrCAD, Inc.
IBM is a registered trademark of International Business Machines Corporation.

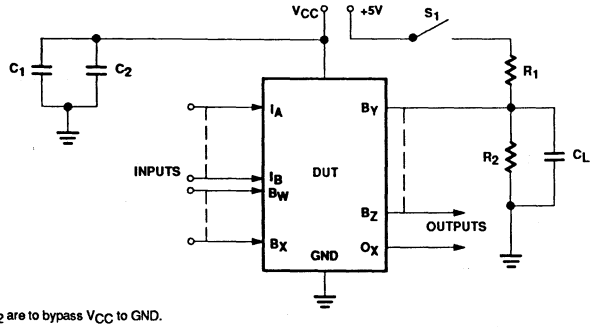
DC ELECTRICAL CHARACTERISTICS

$0°C \le T_{amb} \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS MIN	LIMITS TYP[1]	LIMITS MAX	UNIT
Input voltage							
V_{IL}	Low	V_{CC} = MIN		–0.3		0.8	V
V_{IH}	High	V_{CC} = MAX		2.0		V_{CC} + 0.3	V
Output voltage							
V_{OL}	Low	V_{CC} = MIN, I_{OL} = 5mA				0.45	V
V_{OH}	High	V_{CC} = MIN, I_{OH} = –2mA		2.4			V
Input current							
I_{IL}	Low	V_{IN} = GND				–10	µA
I_{IH}	High	V_{IN} = V_{CC}				10	µA
Output current							
$I_{O(OFF)}$	Hi-Z state	V_{OUT} = V_{CC}				10	µA
		V_{OUT} = GND				–10	µA
I_{OH}	Output High	V_{CC} = MIN, V_{OUT} = 2.4V				–2	mA
I_{OL}	Output Low	V_{CC} = MIN, V_{OUT} = 0.45V				5	mA
I_{OS}	Short-circuit[5]	V_{OUT} = GND				–100	mA
I_{CC}	V_{CC} supply current	V_{CC} = MAX, No load	CMOS input[2]		60	100[6]	mA
		f = 1MHz	TTL input[3]		65	120[6]	mA
I_{SB}	Standby V_{CC} supply current	V_{CC} = MAX, No load	CMOS input		1.0	10	mA
		PD = V_{IH}	TTL input		1.5	10	mA
Capacitance							
C_{IN}	Input	V_{CC} = 5V, T_{amb} = +25°C, V_{IN} = 2.0V			8		pF
C_B	I/O	V_{CC} = 5V, T_{amb} = +25°C, V_{IO} = 2.0V			16		pF

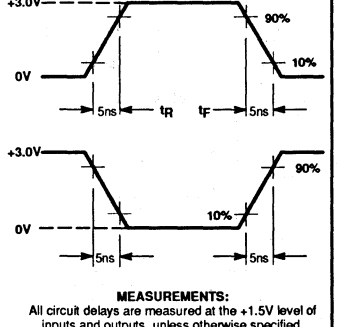
NOTES:
1. All typical values are at V_{CC} = 5V, T_{amb} = +25°C.
2. CMOS inputs: V_{IL} = GND, V_{IH} = V_{CC}.
3. TTL inputs: V_{IL} = 0.45V, V_{IH} = 2.4V.
4. All voltage values are with respect to network ground terminal.
5. Duration of short-circuit should not exceed one second. Test one at a time.
6. ΔI_{CC} vs. Frequency = 4mA/MHz max.

TEST LOAD CIRCUITS



NOTES:
C_1 and C_2 are to bypass V_{CC} to GND.
Test Load R_1 = 750Ω, R_2 = 442Ω, C_L = 30pF (C_L = 5pF for Output Disable)
$0°C \le T_{amb} \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

VOLTAGE WAVEFORMS



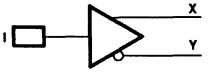
MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

MACRO CELL AC SPECIFICATIONS

Min: 0°C, 5.25V; Typ: 25°C, 5.0V; Max: 75°C, 4.75V (SNAP Resource Summary Designations in Parentheses)

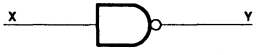
Input Buffer
(DIN552, NIN552, BDIN552, BNIN552 CDIN552, CNIN552, CKDIN552, CKNIN552, IDFF552*)



SYMBOL	PARAMETER		LIMITS						UNIT
	To	From	PML2852-35			PML2852-50			
	(Output)	(Input)	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	X	I	5	7	10	7	10	15	ns
t_{PLH}	X	I	5	7	10	7	10	15	ns
t_{PHL}	Y	I	5	7	10	7	10	15	ns
t_{PLH}	Y	I	5	7	10	7	10	15	ns

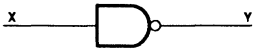
* When input D flip-flop is bypassed.
Input Pins: 12–18, 20, 21, 24, 26–28.
I/O and Bidirectional Pins: 1–3, 5–7, 58–60, 62–66, 69, 70, 75–80, 83, 84.
Bypassed DFF at Pins: 30–32, 34–39, 41–43, 45, 47–49.

Internal NAND of Main Array
(FBNAND, NAND)



SYMBOL	PARAMETER		LIMITS			LIMITS			UNIT
	To	From	PML2852-35			PML2852-50			
	(Output)	(Input)	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Y	X	10	15	20	12	18	25	ns
t_{PLH}	Y	X	10	15	20	12	18	25	ns

Internal NAND of Clock Array
(NAND)

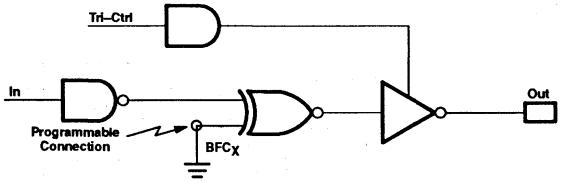


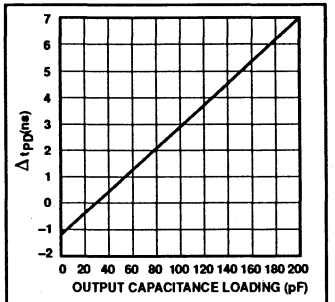
SYMBOL	PARAMETER		LIMITS			LIMITS			UNIT
	To	From	PML2852-35			PML2852-50			
	(Output)	(Input)	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Y	X	5	7	10	7	10	15	ns
t_{PLH}	Y	X	5	7	10	7	10	15	ns

MACRO CELL AC SPECIFICATIONS (Continued)

Min: 0°C, 5.25V; Typ: 25°C, 5.0V; Max: 75°C, 4.75V (SNAP Resource Summary Designations in Parentheses)

3-State Output with Programmable Polarity (TOUT552 + EXOR552 + NAND)



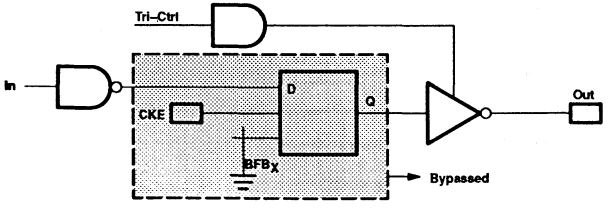


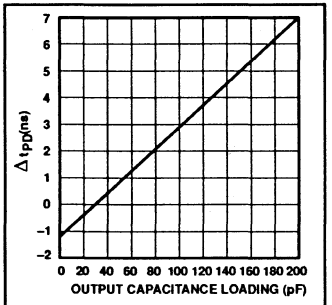
Δt$_{PD}$ vs Output Capacitance Loading (Typical)

SYMBOL	PARAMETER		LIMITS						UNIT
	To (Output)	From (Input)	PML2852-35			PML2852-50			
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Out	In	12	18	25	17	25	35	ns
t_{PLH}	Out	In	12	18	25	17	25	35	ns
t_{OE}[4]	Out	Tri-Ctrl	5	7	10	7	10	15	ns
t_{OD}[4]	Out	Tri-Ctrl	5	7	10	7	10	15	ns

Bidirectional Pins: 58–60, 62–66.

I/O Output Buffer with 3-State Control, DFF Bypassed (TOUT552 + NAND)





Δt$_{PD}$ vs Output Capacitance Loading (Typical)

SYMBOL	PARAMETER		LIMITS						UNIT
	To (Output)	From (Input)	PML2852-35			PML2852-50			
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Out	In	12	18	25	17	25	35	ns
t_{PLH}	Out	In	12	18	25	17	25	35	ns
t_{OE}[4]	Out	Tri-Ctrl	5	7	10	7	10	15	ns
t_{OD}[4]	Out	Tri-Ctrl	5	7	10	7	10	15	ns

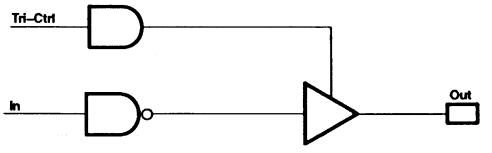
I/O Pins: 1–3, 5–7, 69, 70, 75–80, 83, 84.

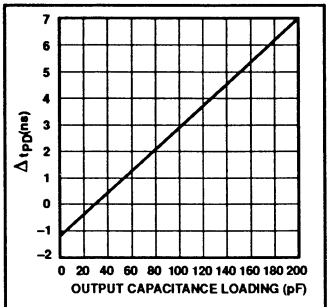
Notes on page 503.

MACRO CELL AC SPECIFICATIONS (Continued)

Min: 0°C, 5.25V; Typ: 25°C, 5.0V; Max: 75°C, 4.75V (SNAP Resource Summary Designations in Parentheses)

Active-Low 3-State Output (TOUT852 + NAND)





Δt_{PD} vs Output Capacitance Loading (Typical)

SYMBOL	PARAMETER		LIMITS						UNIT
	To (Output)	From (Input)	PML2852-35			PML2852-50			
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Out	In	12	18	25	17	25	35	ns
t_{PLH}	Out	In	12	18	25	17	25	35	ns

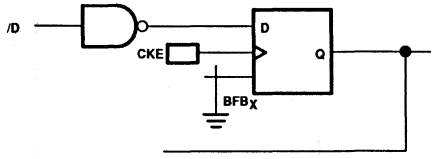
Output Pins: 8–11, 50–57, 71–74.

MACRO CELL AC SPECIFICATIONS (Continued) (SNAP Resource Summary Designations in Parentheses)

D FLIP-FLOP

Min: 0°C, 5.25V; Typ: 25°C, 5.0V; Max: 75°C, 4.75V

Output DFF Used Internally
(ODFF552)



SYMBOL	PARAMETER	LIMITS						UNIT
		PML2852-35			PML2852-50			
		MIN	TYP	MAX	MIN	TYP	MAX	
f_{CKE}	Flip-flop toggle rate			50			35	MHz
$t_{W\,CKE}$ High	Clock HIGH	10			14			ns
$t_{W\,CKE}$ Low	Clock LOW	10			14			ns
t_{SETUP} /D	/D setup time to CKE	15			20			ns
t_{HOLD} /D	/D hold time to CKE	4			6			ns

SYMBOL	PARAMETER		LIMITS						UNIT
	From	To	PML2852-35			PML2852-50			
	(Input)	(Output)	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	CKE ↑	Q	10	15	20	14	20	25	ns
t_{PHL}	CKE ↑	Q	10	15	20	14	20	25	ns

MACRO CELL AC SPECIFICATIONS (Continued) (SNAP Resource Summary Designations in Parentheses)

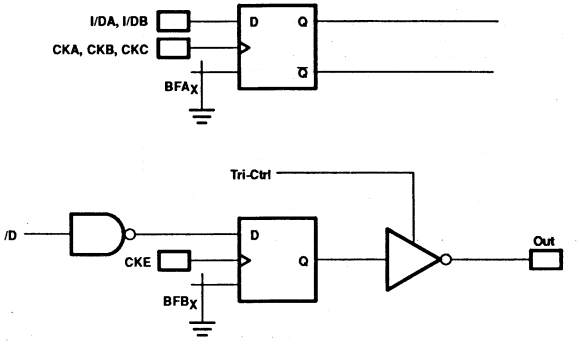
D FLIP-FLOP (Continued)

Min: 0°C, 5.25V; Typ: 25°C, 5.0V; Max: 75°C, 4.75V

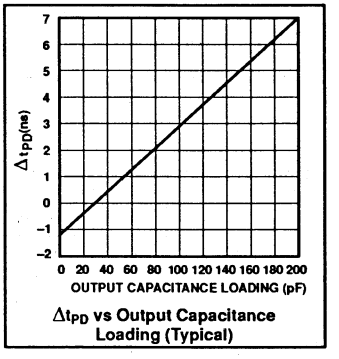
INPUTS		OUTPUTS	
CK	D	Q	$\overline{Q}$
L	X	Q_0	$\overline{Q}_0$
↑	H	H	L
↑	L	L	H

NOTE:
Q_0, $\overline{Q}_0$ represent previous stable condition of Q, $\overline{Q}$.

Input and Output (IDFF552 & ODFF552)



SYMBOL	LIMITS						UNIT
	PML2852-35			PML2852-50			
	MIN	TYP	MAX	MIN	TYP	MAX	
$f_{CKA, CKB, CKC}$			50			35	MHz
$t_{W\ CKA, CKB, CKC}$ High	10			14			ns
$t_{W\ CKA, CKB, CKC}$ Low	10			14			ns
t_{SETUP} I/DA, I/DB	5			7			ns
t_{HOLD} I/DA, I/DB	5			7			ns
f_{CKE}			50			35	MHz
$t_{W\ CKE}$ High	10			14			ns
$t_{W\ CKE}$ Low	10			14			ns
t_{SETUP} /D	15			20			ns
t_{HOLD} /D	4			6			ns



Δt_{PD} vs Output Capacitance Loading (Typical)

SYMBOL	PARAMETER		LIMITS						UNIT
	From (Input)	To (Output)	PML2852-35			PML2852-50			
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	CKA, CKB/CKC ↑	Q, $\overline{Q}$	5	7	10	7	10	15	ns
t_{PHL}	CKA, CKB/CKC ↑	Q, $\overline{Q}$	5	7	10	7	10	15	ns
t_{PLH}	CKE ↑	Out	12	18	25	17	25	35	ns
t_{PHL}	CKE ↑	Out	12	18	25	17	25	35	ns

MACRO CELL AC SPECIFICATIONS (Continued) (SNAP Resource Summary Designations in Parentheses)

JK FLIP-FLOPS

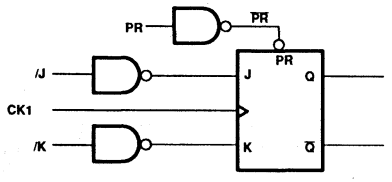
Min: 0°C, 5.25V; Typ: 25°C, 5.0V; Max: 75°C, 4.75V

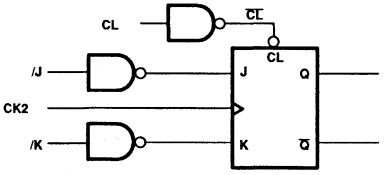
(JKPR552)

INPUTS				OUTPUTS	
$\overline{PR}$	CK	J	K	Q	$\overline{Q}$
L	X	X	X	H	L
H	↑	L	L	Q_0	$\overline{Q}_0$
H	↑	H	L	H	L
H	↑	L	H	L	H
H	↑	H	H	TOGGLE	
H	L	X	X	Q_0	$\overline{Q}_0$

(JKCL552)

INPUTS				OUTPUTS	
$\overline{CL}$	CK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↑	L	L	Q_0	$\overline{Q}_0$
H	↑	H	L	H	L
H	↑	L	H	L	H
H	↑	H	H	TOGGLE	
H	L	X	X	Q_0	$\overline{Q}_0$





SYMBOL	PARAMETER	LIMITS						UNIT
		PML2852-35			PML2852-50			
		MIN	TYP	MAX	MIN	TYP	MAX	
f_{CK1}	CK1 toggle frequency			50			35	MHz
f_{CK2}	CK2 toggle frequency			50			35	MHz
$t_{W\,CK1}$ High	CK1 clock HIGH	10			14			ns
$t_{W\,CK1}$ Low	CK1 clock LOW	10			14			ns
$t_{W\,CK2}$ High	CK2 clock HIGH	10			14			ns
$t_{W\,CK2}$ Low	CK2 clock LOW	10			14			ns
t_{SETUP} /J, /K	/J, /K setup time to CK1, CK2	27			35			ns
t_{HOLD} /J, /K	/J, /K hold time to CK1, CK2	0			0			ns
t_W PR Low	Preset Low period	10			14			ns
t_W CL Low	Clear Low period	10			14			ns

SYMBOL	PARAMETER		LIMITS						UNIT
	From (Input)	To (Output)	PML2852-35			PML2852-50			
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	CK1,2	Q, $\overline{Q}$	2	3.5	5	3	5	7	ns
t_{PHL}	CK1,2	Q, $\overline{Q}$	2	3.5	5	3	5	7	ns
t_{PLH}	PR	Q, $\overline{Q}$	12	18	25	17	24	30	ns
t_{PHL}	PR	Q, $\overline{Q}$	12	18	25	17	24	30	ns
t_{PLH}	CL	Q, $\overline{Q}$	12	18	25	17	24	30	ns
t_{PHL}	CL	Q, $\overline{Q}$	12	18	25	17	24	30	ns

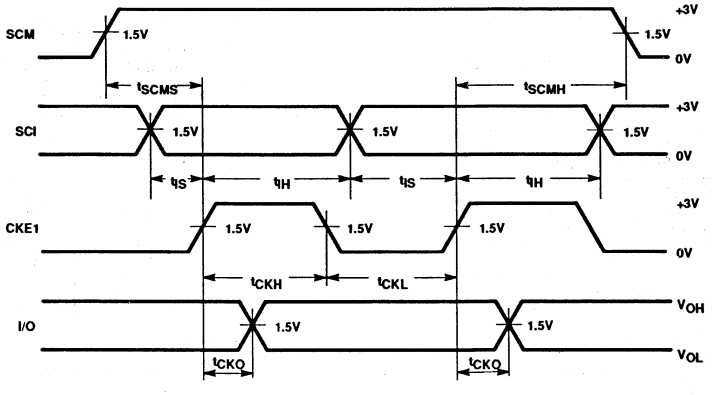
AC ELECTRICAL CHARACTERISTICS

$0°C \leq T_{amb} \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$, $V_{PP} = V_{CC}$,
$R_1 = 750\Omega$, $R_2 = 442\Omega$, $C_L = 5pF$ for Output Disable) (See Test Load Circuit Diagram)

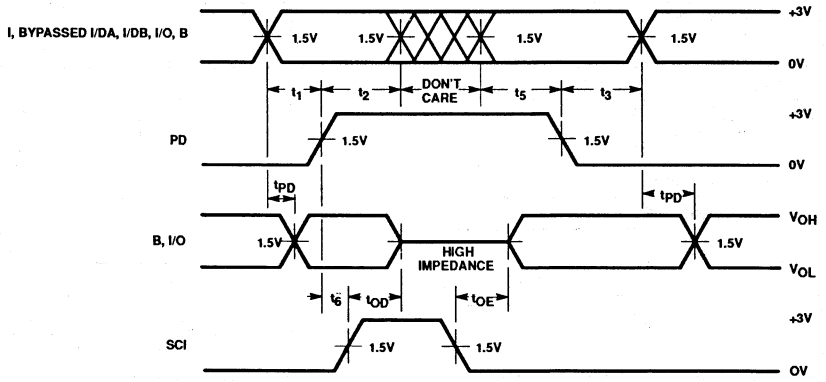
SYMBOL	PARAMETER	LIMITS				UNIT
		PML2852-35		PML2852-50		
		MIN	MAX	MIN	MAX	
Scan mode operation[1]						
t_{SCMS}	Scan Mode (SCM) Setup time	15		15		ns
t_{SCMH}	Scan Mode (SCM) Hold time	25		30		ns
t_{IS}	Data Input (SCI) Setup time	5		5		ns
t_{IH}	Data Input (SCI) Hold time	5		5		ns
t_{CKO}	Clock to Output (I/O) delay		30		40	ns
t_{CKH}	Clock High	10		15		ns
t_{CKL}	Clock Low	10		15		ns
Power down, power up[2]						
t_1	Input (I, bypassed I/DA, I/DB, I/O, B) setup time before power down	40		50		ns
t_2	Input hold time	30		35		ns
t_3	Power Up recovery time		60		70	ns
t_4	Output hold time	0		0		ns
t_5	Input setup time before Power Up	20		25		ns
t_{OE}	SCI to Output Enable time[3]		40		50	ns
t_{OD}	SCI to Output Disable time[3]		40		50	ns
t_6	Power Down setup time	10		15		ns
t_7	Power Up to Output valid		70		80	ns
Power-on reset						
t_{PPR1}	Power-on reset output register (Q = 0) to output (I/O) delay		10		15	ns
t_{PPR2}	Power-on reset input register (Q = 0), buried JK Flip-Flop (Q = 0) to output (B, bypassed I/O) delay		40		50	ns

NOTES:
1. SCM recovery time is 50ns after SCM operation. 50ns after SCM operation, normal operations can be resumed.
2. Timings are measured without foldbacks.
3. Transition is measured at steady state High level (–500mV) or steady state Low level (+500mV) on the output from 1.5V level on the input with specified test load ($R_1 = 750\Omega$, $R_2 = 442\Omega$, $C_L = 5pF$). This parameter is sampled and not 100% tested.
4. For 3-State output; output enable times are tested with $C_L = 30pF$ to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with $C_L = 5pF$. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} - 0.5V)$ with S_1 open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with S_1 closed.

TIMING DIAGRAMS

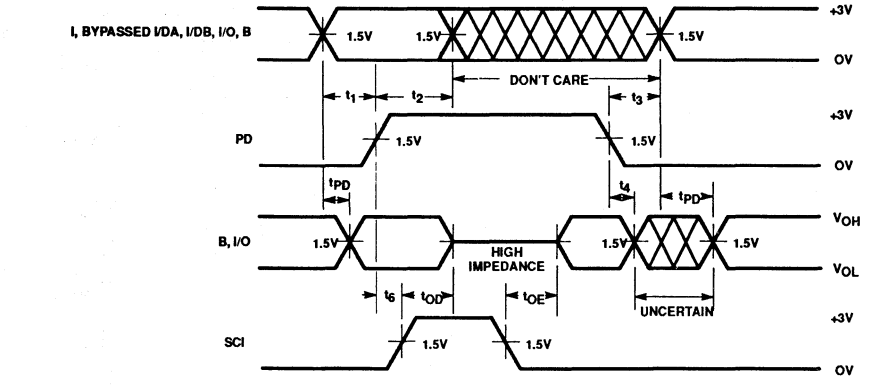


Scan Mode Operation

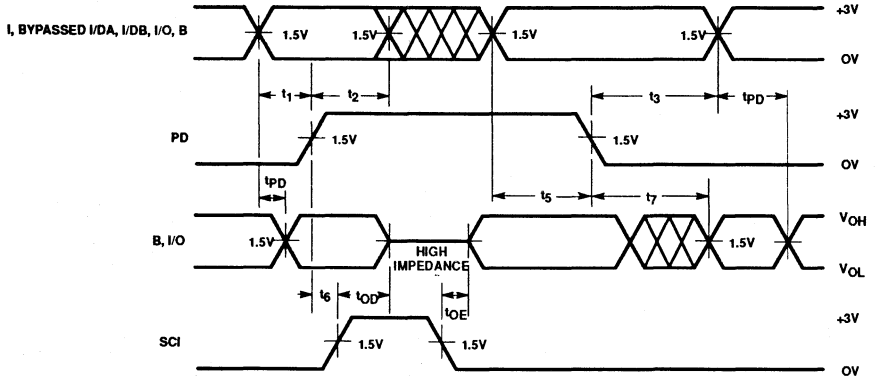


Power Down, Power Up
Input (old) Ready Before Power Up

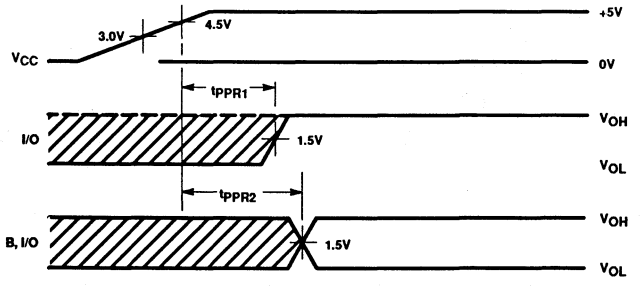
TIMING DIAGRAMS (Continued)



Power Down, Power Up
Input (new) Ready After Power Up

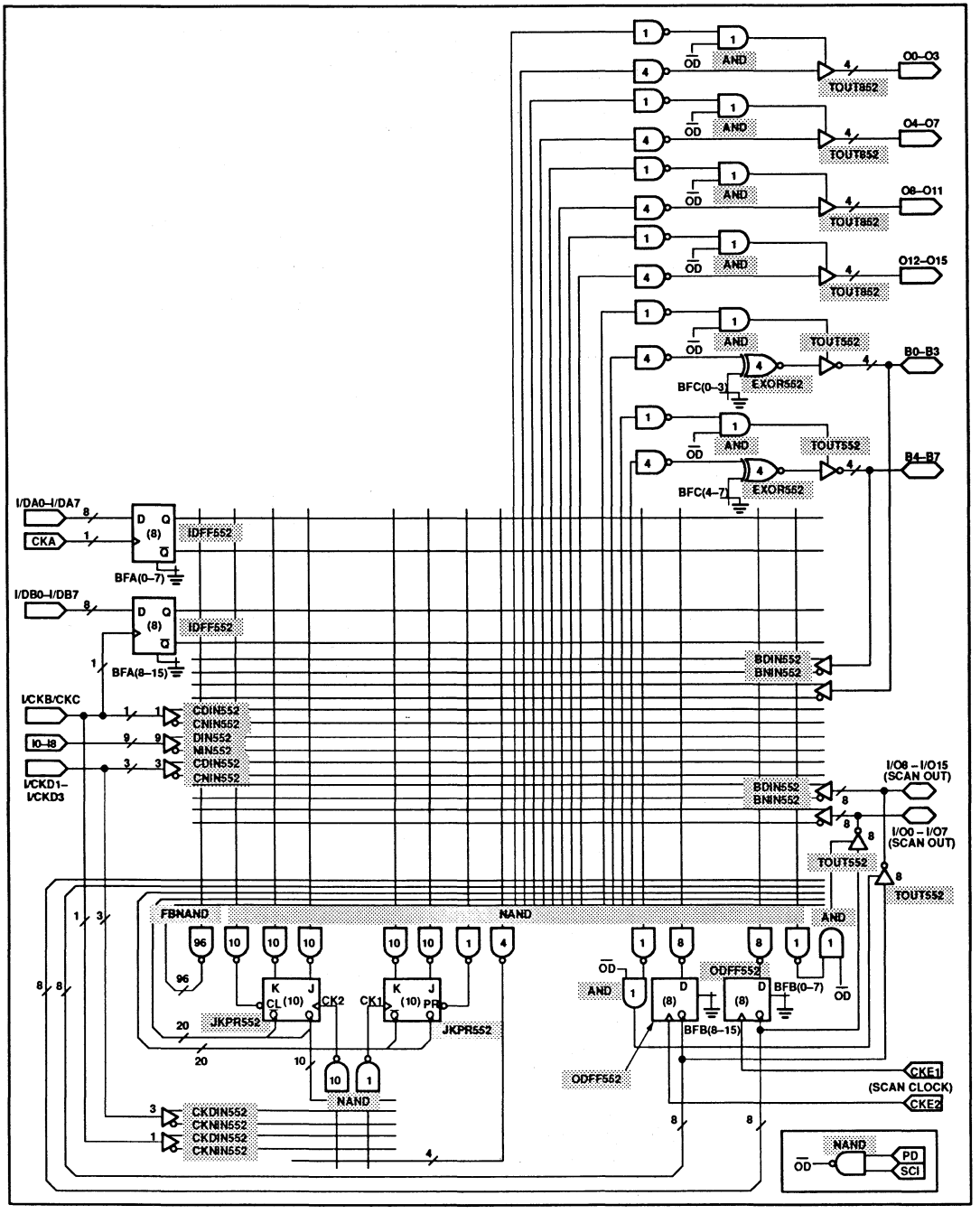


Power Down, Power Up
Input (new) Ready Before Power Up



Power-On Reset

SNAP RESOURCE SUMMARY DESIGNATIONS



ERASURE CHARACTERISTICS (For Quartz Window Packages Only)

The erasure characteristics of the PML2852 device is such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000 – 4000Å range. Data shows that constant exposure to room level fluorescent lighting could erase a typical PML2852 in approximately three years, while it would take approximately one week to cause erasure when exposed to direct sunlight. If the PML2852 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure for the PML2852 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15Wsec/cm^2. The erasure time with this dosage is approximately 30 to 35 minutes using an ultraviolet lamp with a 12,000µW/cm^2 power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose a CMOS EPLD can be exposed to without damage is 7258Wsec/cm^2 (1 week @ 12,000µW/cm^2). Exposure of these CMOS EPLDs to high intensity UV light for longer periods may cause permanent damage.

The maximum number of guaranteed erase/write cycles is 50. Data retention exceeds 20 years.

PROGRAMMING

Refer to the following charts for qualified manufacturers of programmers and software tools:

PROGRAMMER MANUFACTURER	PROGRAMMER MODEL	FAMILY/PINOUT CODES
DATA I/O CORPORATION 10525 WILLOWS ROAD, N.E. P.O. BOX 97046 REDMOND, WASHINGTON 98073–9746 (800)247–5700	UNISITE 40/48 Ver. 3.5 PINSITE Ver. 3.5	15918C* (with adaptor) 15918D
STREBOR DATA COMMUNICATIONS 1008 N. NOB HILL AMERICAN FORK, UT 84003	PLP–S1A Programmer MP68CC adapter	
BASIC COMPUTER SYSTEMS AG WOLFGANG–PAULI–GASSE A–1140 WIEN–AUHOF, AUSTRIA	UP2000 Rev. 2.28	
SMS – W. STEUDEL IM MORGENTAL 13 D–8994 HERGATZ, GERMANY	SPRINT PLUS/EXPERT Rev. TBD	
SYSTEM GENERAL 244 SOUTH PARK VICTORIA DRIVE MILPITAS, CALIFORNIA 95035	TURPRO-1 Rev. 1.42	

* Needs a 40-pin DIP to 84-pin PLCC adaptor that is available from Emulation Technology.
Part Number: AS–84–40–01P–6YAM

EMULATION TECHNOLOGY, INC.
2368B Walsh Avenue, Building D
Santa Clara, California 95051
Telephone No. (408) 982–0660
Fax. No. (408) 982–0664

SOFTWARE MANUFACTURER	DEVELOPMENT SYSTEM
SIGNETICS COMPANY 811 EAST ARQUES AVENUE P.O. BOX 3409 SUNNYVALE, CALIFORNIA 94088–3409 (408)991–2000	SLICE SOFTWARE SNAP SOFTWARE

Section 7
Military Selection Guide

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Military selection guide

Part Number	Device Description	Package Description	Standard MIL–Drawing	MIL–Drawing Status**
PLS159A	PLS	20DIP3	PLANNED	NA
PLS173/BLA	PLA	24DIP3	5962–8850402LA	A
PLS179/BLA	PLS	24DIP3	5962–8850701LA	A
82S100/BXA	PLA	28DIP6		
82S100/BYA	PLA	28FLAT		
82S100/B3A	PLA	28LLCC		
82S101/BXA	PLA	28DIP6		
82S101/BYA	PLA	28FLAT		
82S101/B3A	PLA	28LLCC		
82S105/BXA	PLS	28DIP6	5962–8670901XA	A
82S105/BYA	PLS	28FLAT	5962–8670901YA	A
82S105/B3A	PLS	28LLCC	5962–86709013A	A
82S153A/BRA	PLA	20DIP3	5962–8768201RA	A
82S153A/B2A	PLA	20LLCC	5962–87682012A	A
PLC42VA12/BLA	PLS	24DIP	PLANNED	NA
PLC42VA12/BYA	PLS	24FLAT	PLANNED	NA
PLC42VA12/B3A	PLS	28LLCC	PLANNED	NA
PML2552/BUA	PML	68LLCC	PLANNED	NA
PLC18V8Z/BRA	PAL	20DIP	PLANNED	NA
PLC18V8Z/BSA	PAL	20FLAT	PLANNED	NA
PLC18V8Z/B2A	PAL	20LLCC	PLANNED	NA
22V10/BLA	PAL	24DIP3	5962–8984103LA	NA

* Not available as a Class B standard product. See M38510 and/or Military Drawing columns for availability
** A = available, NA = not available, IP = in process, call for availability.

Section 8
Development Software

INDEX

Synthesis Netlist Analysis Program — SNAP 1.8

FEATURES

- Schematic entry available using Data I/O DASH™ OrCAD SDT IV™
- State equation entry
- Boolean equation entry
- Netlist entry
- Edif 2.xx entry
- Simulation waveform entry
- Capability to design in one or any combination of formats
- Device independent, netlist based design platform
- Boolean equation extractor
- Fuse table editor
- Philips LESIM 5-State gate array simulator as well as Signetics SIGSIM:
  - Logic and fault simulation
  - Model extraction and timing simulation
  - Synthetic logic analyzer format
  - Stimuli entry in waveform format
- Freezing of selected Critical paths
- Capability to create user defined macros or to use TTL elements
- Full documentation of design and simulation results in waveform format
- JEDEC fusemap compiler and device programmer interface

GENERAL DESCRIPTION

SNAP PLD development software.
Simple-to-use tools for demanding designs.

Get ready for greater design productivity. SNAP, the complete logic synthesis, simulation and layout package for Signetics full line of PLDs, saves one commodity in preciously short supply: design time. **Fully equipped with every tool you need to turn out PLD designs quickly,** SNAP eliminates the "learning curve" that can keep you from being immediately productive. Regardless of whether you're a PLD novice or seasoned pro, SNAP allows you to produce optimized designs within a matter of hours.

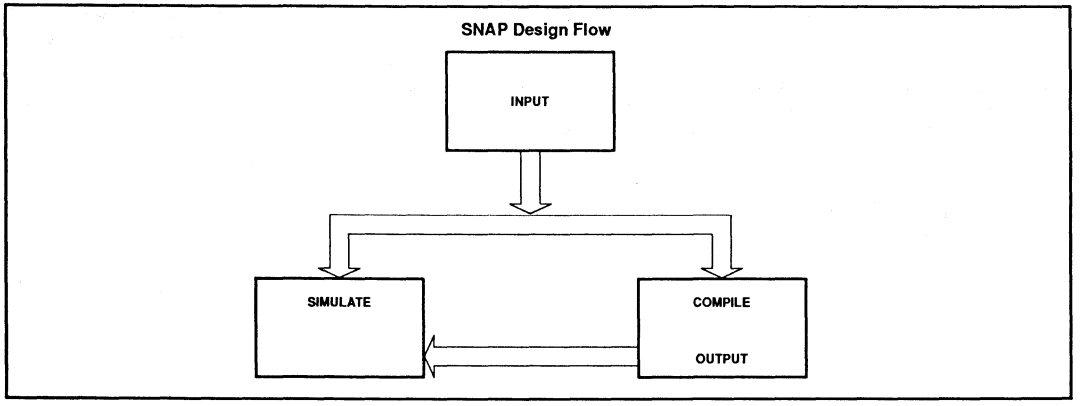
For rapid design you need flexibility and SNAP provides lots of it. Enter your design in the most convenient way possible — using **any combination of schematics, waveforms, Boolean equations, state equations or netlists.** SNAP merges the inputs and generates a dense, high-speed design that can be simulated in SNAP's powerful simulator and then downloaded to a PLD programmer.

With SNAP, you produce your design in a netlist-based, device-independent environment. No need to commit to a particular part from the start of the design process: With SNAP, you can change the target PLD at will. If you find that your design needs a larger device or can fit into a smaller, less expensive one, simply select a new part and resimulate. SNAP allows you to take advantage of the most appropriate PLD for the job without wasting time.

SNAP'S UNRIVALED SIMULATION FACILITY

Simulation is a key part of the SNAP design process. **SNAP incorporates Philips 5-State ASIC simulator,** a simulator so unsurpassed in its accuracy and diagnostic ability that it is a standard tool used by the company's own chip designers. You can examine any of your design's internal nodes and apply SNAP's virtual logic analyzer to display the precise timing at that node. Then change the stimulus and put the design through its paces with SNAP's built-in waveform editor. Compile into a specific PLD and resimulate. When you finally program a PLD, chances are that it will run perfectly the first time.

Since testability represents an ever-important measure of the success of a PLD design, **SNAP includes a powerful fault simulator** that simplifies the task of analyzing fault coverage. The tool rapidly generates a report detailing undetected and potentially undetectable faults, coverage efficiency, and other useful data. With it, you get the most thorough fault coverage possible in a limited test period.



DASH is a trademark of Data I/O Corp.
OrCAD STD IV is a trademark of OrCAD, Inc.

Synthesis Netlist Analysis Program SNAP 1.8

Would you like to know how many potential faults your test vectors can detect?
Just look at the output of the SNAP FAULT SIMULATOR...

```
FAULT LIST:
   TOTAL NUMBER OF SIGNALS                =     6
   NUMBER OF NAMED SIGNALS                =     6
   NUMBER OF CIRCUIT FAULTS               =    12
   NUMBER OF INSERTED FAULTS              =    10
   NUMBER OF COLLAPSED FAULTS             =     2

FAULT DETECTION:
   NUMBER OF HARD DETECTED FAULTS         =    12
   NUMBER OF POTENTIALLY DETECTED FAULTS  =     0
   NUMBER OF UNDETECTED FAULTS            =     0

FAULT COVERAGE:
   HARD DETECTION FAULT COVERAGE          =  100.0%
   POTENTIAL DETECTION FAULT COVERAGE     =  0.0  %
   TOTAL DETECTION FAULT COVERAGE         =  100.0%

HARD DETECTION FAULT COVERAGE VERSUS PATTERN# :
PATTERN#   %      0         20        40        60        80        100
-----------------+---------+---------+---------+---------+---------+
       1  58.3    .****************************
       2  75.0    .************************************
       3  83.3    .*******************************************
       4  100.0   .**************************************************
       5  100.0   .**************************************************
-----------------+---------+---------+---------+---------+---------+
```

Designers who need to consolidate the designs of existing logic devices will draw considerable benefit from SNAP's unique **Boolean equation extractor.** It take the design data from existing PLDs and converts it to the actual, corresponding Boolean equations, which can then be used as an input to SNAP. It eliminates the need to find and re-enter design data, often a time-consuming process.

And for added convenience, **SNAP features the powerful logic optimizer, Espresso Minimizer.** Espresso automatically removes all unnecessary gates from your design, assuring that it will be the fastest and densest possible. Espresso allows you to pack more in — or fit it into a smaller PLD. The result can be substantial cost and power savings.

FULL SUPPORT NOW — AND INTO THE FUTURE

SNAP supports Signetics broad line of PLDs, which includes high-speed PAL®-type devices, programmable logic arrays, programmable logic sequencers, and sophisticated programmable macro logic. It is fully compatible with SLICE, Signetics entry-level design package. And as Signetics introduces new PLDs in the future, SNAP will support those too, in a timely manner. You can standardize on SNAP for your future development, with confidence.

Menu-driven and supported by clear, concise documentation, SNAP is a pleasure to use. But if problems do arise, Signetics network of field applications engineers stand ready to help. Specially trained and backed by a comps of factory experts, Signetics FAEs are stationed in all major cities in the U.S. and overseas. Wherever you are, chances are that support is nearby.

PAL is a registered trademark of AMD/MMI, Inc.

Synthesis Netlist Analysis Program SNAP 1.8

SNAP Boolean Equation Extractor

FROM THIS:

```
L0000
11111111111111011101111011111111111111111
00000000000000000000000000000000000000000
00000000000000000000000000000000000000000
00000000000000000000000000000000000000000
00000000000000000000000000000000000000000
00000000000000000000000000000000000000000
00000000000000000000000000000000000000000
00000000000000000000000000000000000000000
11111111111111011111111111111111111011111
```

TO THIS:

```
@LOGIC EQUATION
S.D     =/(ASN*RWN*/DREQN1+S*/DREQN1);
```

AUTOMATICALLY • IMMEDIATELY • EFFORTLESSLY

PRODUCT SUPPORT

SLICE supports the Signetics line of PLDs, which ranges from high-speed PAL devices to complex Programmable Macro Logic circuits. It will also support new Signetics PLDs as they are introduced. The devices currently supported are:

Programmable Logic Arrays:

PLUS153 PLS100
PLUS173

Programmable Macro Logic:

PLHS501 PML2852
PML2552

Programmable Logic Sequencers:

PLS155 PLC42VA12
PLS157 PLC415
PLS159 PLS105
PLS167 PLUS105
PLS168 PLUS405
PLS179

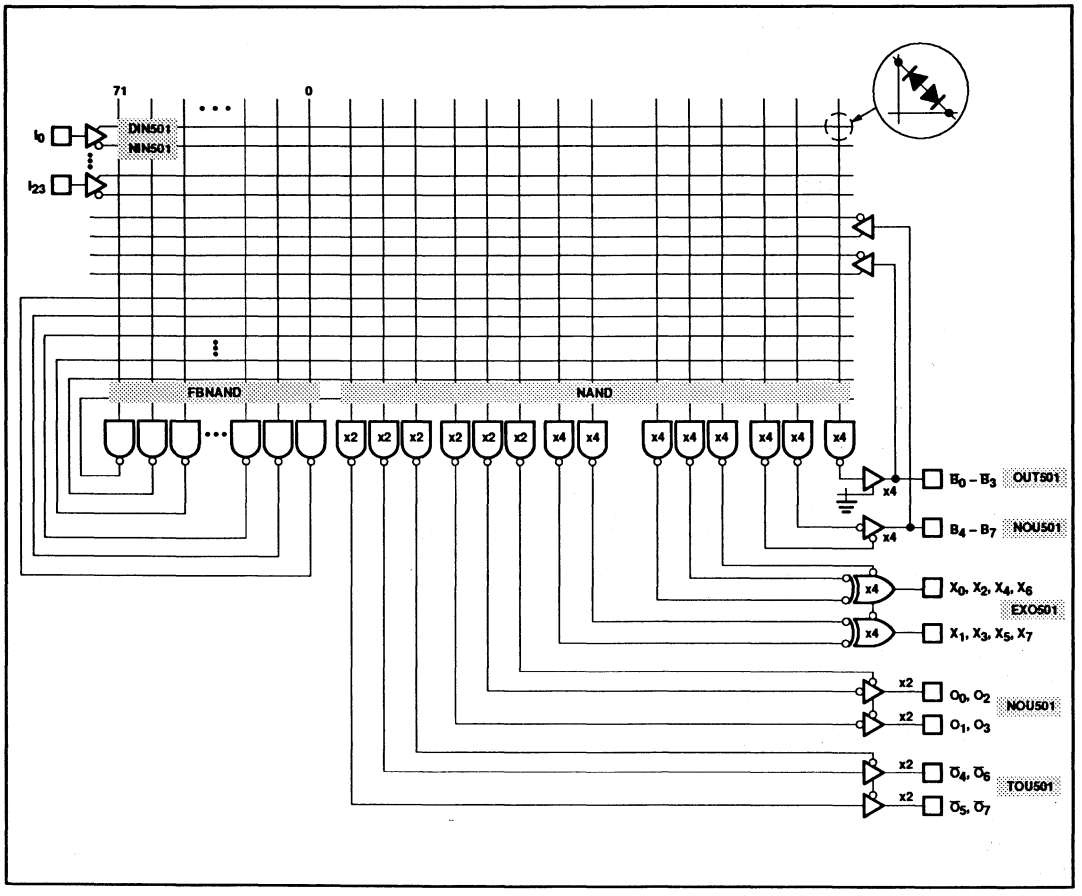
Programmable Array Logic

PLUS20L8 PLUS16L8
PLUS20R8 PLUS16R8
PLUS20R6 PLUS16R6
PLUS20R4 PLUS16R4
10H20EV8 PLQ22V10
10020EV8 PLC18V8Z
PHD48N22 PL22V10
PHD16N8

TRY IT — YOU'LL LIKE IT

Pop the enclosed SNAP demo disk into your computer and see how easy PLD design can be. The demo, like SNAP itself, runs on almost any IBM® PC or compatible having DOS 2.1 or higher, 640K RAM and a hard disk.

IBM is a registered trademark of International Business Machines Corp.



SNAP Resources Summary

Cell name	used/total	%
DIN501	18 / 32	56%
NIN501	7 / 32	21%
FBNAND	72 / 72	100%
NAND	34 / 44	77%
OUT501	2 / 4	50%
NOU501	4 / 8	50%
EXO501	8 / 8	100%
TOU501	4 / 4	100%

Please hit any key to continue...

PLHS501 Resources

Synthesis Netlist Analysis Program — SNAP 1.8

SNAP OVERVIEW

Signetics SNAP (Synthesis Netlist Analysis and Program) is a software program used in implementing logic designs with Signetics Programmable Logic Devices. The software runs on any IBM PS/2, AT, XT, or compatible computer. SNAP accepts the logic design specified in the form of schematics, EDIF netlists, Boolean logic equations, and/or state equations; combines the different forms and different parts of the design into a single netlist; prompts the user to select a target PLD; and generates the JEDEC fuse map used for programming the target PLD device.

Schematics can be created with either OrCAD SDT III, OrCAD SDT IV or DASH, three schematic capture packages offered as options to SNAP. Logic and state equations can be created using any ASCII text editor such as PC-Write. After you specify the design, SNAP converts the schematic, logic equations, and state equations into a single netlist. You can then use SNAP to perform the following functions:

- Create, display, and edit the stimulus waveforms for simulation
- Simulate the logic functions and timing
- Display and print the simulation results
- Determine the fault coverage for a given set of inputs
- Generate the test vectors
- Generate the fuse map for the target PLD device
- Generate a netlist of the PLD implementation for simulation
- Download the fuse map and test vectors to the PLD programmer

Specification of the logic design is independent of the type of PLD device. You can specify the design first and choose the PLD device later, after simulating and debugging the logic design. If the chosen device is unable to accommodate the design, it is a simple matter to select another device and generate the fuse map for that device. After this has been done, SNAP can generate a netlist and a set of logic equations directly from the final fuse map, allowing analysis and simulation of the final design as implemented in the target device. Also, a design using several PLD devices can be accurately simulated with the use of real delays.

Supported PLD Devices

The PLD devices supported by SNAP 1.8 are listed below, showing the part number, architecture (Inputs x Terms x Outputs), and number of pins for each device type.

Programmable Macro Logic (PML) Devices

PLHS501	104 x 116 x 24	52 pins
PML2552	185 x 226 x 24	68 pins
PML2852	185 x 226 x 40	84 pins

Programmable Logic Sequencer (PLS) Devices

PLS155	16 x 45 x 12	20 pins
PLS157	16 x 45 x 12	20 pins
PLS159	16 x 45 x 12	20 pins
PLS167	14 x 48 x 6	24 pins
PLS168	16 x 45 x 12	20 pins
PLS179	12 x 48 x 8	24 pins
PLC42VA12	42 x 105 x 12	24 pins
PLC415	17 x 68 x 8	28 pins
PLS105	16 x 48 x 8	28 pins
PLUS105	22 x 48 x 8	28 pins
PLUS405	24 x 64 x 8	28 pins

Programmable Logic Array (PLA) Devices

PLS100	16 x 48 x 8	28 pins
PLUS153	18 x 42 x 10	20 pins
PLUS173	22 x 42 x 10	24 pins

PAL Devices

PLUS16L8	16 x 64 x 8	20 pins
PLUS16R8	16 x 64 x 8	20 pins
PLUS16R6	16 x 64 x 8	20 pins
PLUS16R4	16 x 64 x 8	20 pins
PHD16N8	16 x 16 x 8	20 pins
PLC18V8Z	18 x 74 x 8	20 pins
PLUS20L8	20 x 64 x 8	24 pins
PLUS20R8	20 x 64 x 8	24 pins
PLUS20R6	20 x 64 x 8	24 pins
PLUS20R4	20 x 64 x 8	24 pins
10X20EV8	20 x 90 x 8	24 pins
PHD48N22	48 x 73 x 22	68 pins
PL22V10	22 x 132 x 10	24 pins
PLQ22V10	22 x 132 x 10	24 pins

Before you can begin using SNAP, you must first install the software and learn the function keys and top-level menu. As part of the setup procedure, you specify the text editor and schematic capture software you are using with SNAP so that SNAP can invoke these programs as needed.

Overview of SNAP Process

The OrCAD SDT IV and DASH schematic capture systems are available as options to the SNAP software package.

OrCAD SDT IV is a complete schematic capture package, one of several design tools offered by OrCad Systems Corporation. OrCAD SDT IV lets you create, edit, save, and print logic schematics. Schematic data files are accepted directly by the SNAP software. Instructions on installing and using OrCAD SDT IV are provided with the OrCAD SDT IV software package. Supplemental information is provided in Appendix A of the User's Manual on configuring OrCAD SDT IV for compatibilty with SNAP.

DASH is Data I/O schematic capture package. Schematic data files are accepted directly by the SNAP software. Instructions on installing and using DASH are provided in Appendix B of the User's Manual, serving as an addendum to the DASH User's Manual.

Any of these schematic capture systems may be used for logic design purposes with SNAP.

SNAP is an interactive, menu-driven software package. At the top level of the program is a graphical menu that allows selection of the desired SNAP operation. See Figure 5.

The boxes show the SNAP program operations that you can select. Operations may be performed at any time and in any order, provided that the input files for that operation are available.

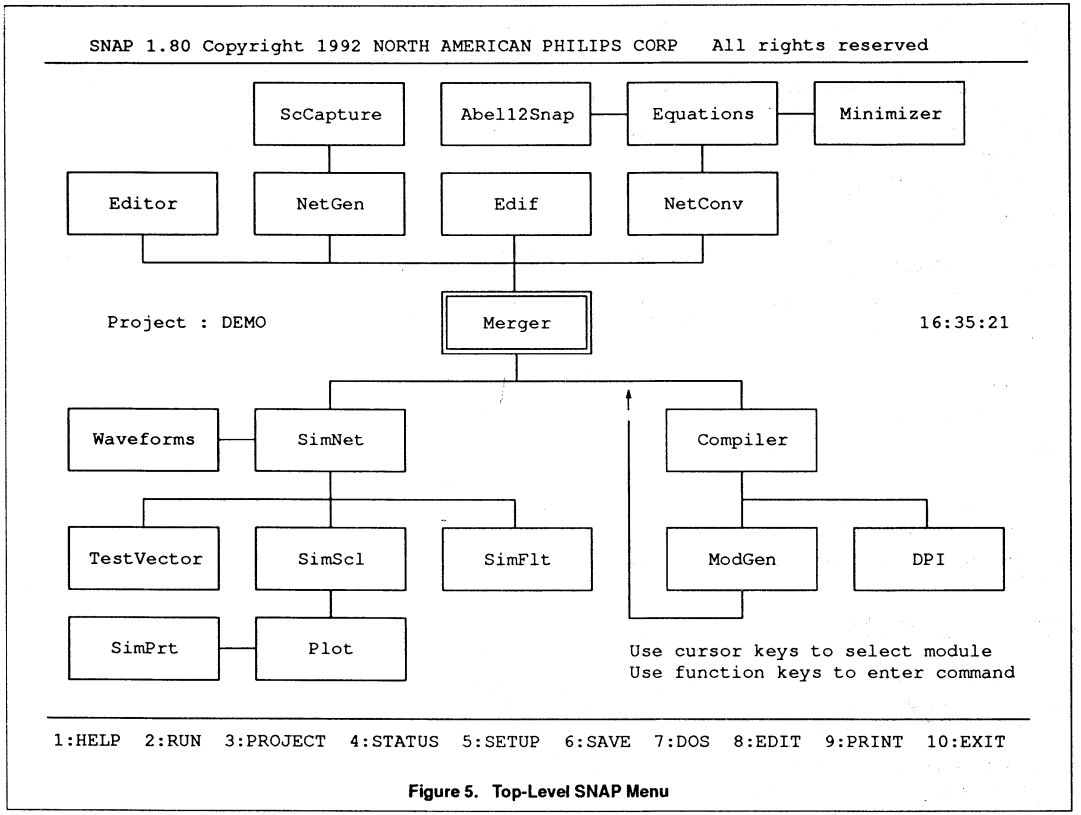


Figure 5. Top-Level SNAP Menu

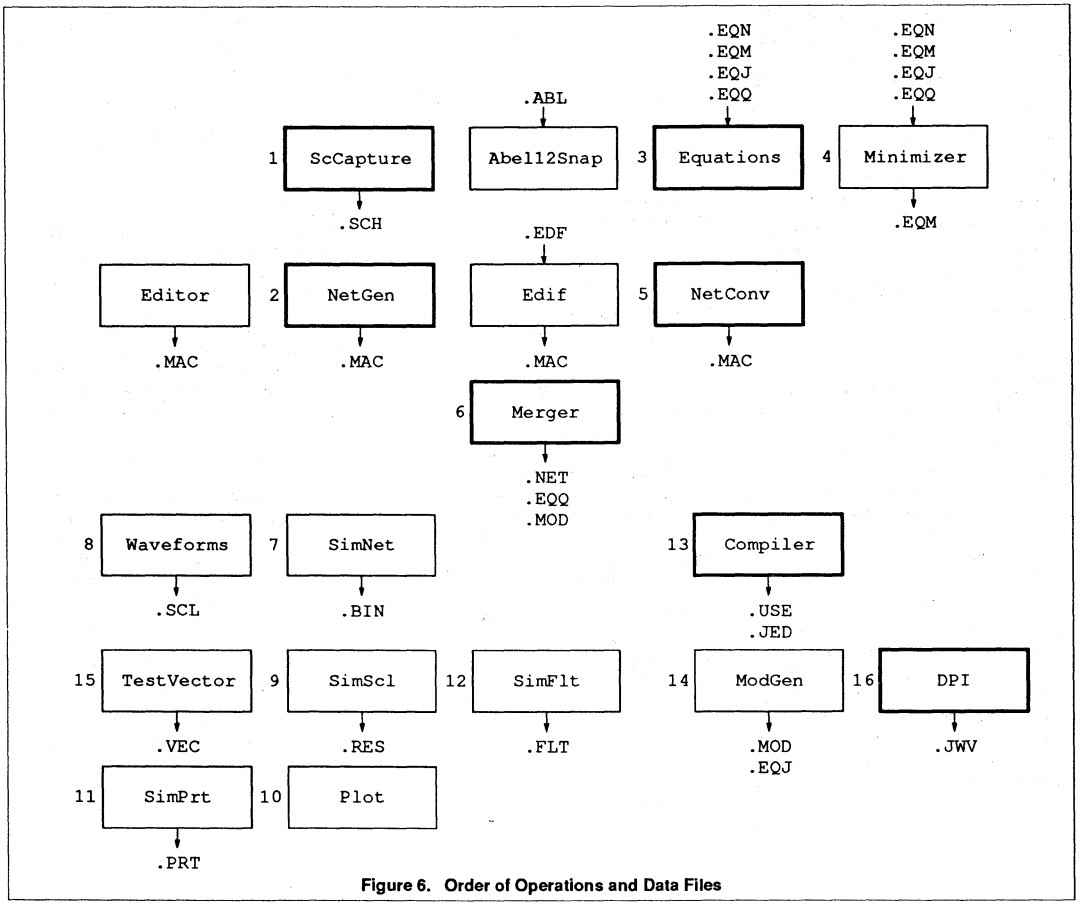


Figure 6. Order of Operations and Data Files

Figure 6 shows the typical order in which the SNAP program operations are executed. The figure also shows the file name extensions for the files produced by (and used by) the individual program operations. The menu options shown in bold boxes are the minimum required to specify a design and generate the fuse map. The remaining menu options may be used as needed for simulation and testing purposes.

In Step 1 (ScCapture), you specify part or all of the logic design with the schematic capture package (OrCAD SDT IV or DASH), using a library of logic elements recognized by SNAP. The design may be drawn hierarchically. In Step 2 (NetGen), SNAP converts the schematic into an intermediate netlist (.MAC file).

In Step 3 (Equations), you specify part or all of the logic design with Boolean logic equations and/or state equations. In Step 4 (Minimizer), an optional step, SNAP changes the form of the equations to minimize the number of gates necessary to implement the design. In Step 5 (NetConv), SNAP converts the logic and state equations into an intermediate netlist (.MAC file).

The complete design may be specified with any combination of schematic capture, logic equations, and state equations. Different parts of the design may be specified separately. Each lower-level part of the design is a "macro" that can be used multiple times at a higher level of the hierarchy.

In Step 6 (Merger), SNAP combines the separate netlists (.MAC files) into a single master netlist (.NET file).

In Step 7 (SimNet), SNAP converts the master netlist into a binary-format file (.BIN file) that is accepted by the simulator.

In Step 8 (Waveforms), you use a graphical waveform editor to create the input signals for the simulation. SNAP converts the waveforms into the "Simulation Control Language" format (.SCL file).

In Step 9 (SimScl), SNAP simulates the logic operation and timing of the design using the input signals created previously. The resulting output signals are stored in a "results" file (.RES file).

Synthesis Netlist Analysis Program SNAP 1.8

In Step 10 (Plot), SNAP displays the results graphically on the screen. You can analyze the simulation results in detail by adjusting the time range and time scale of the display.

In Step 11 (SimPrt), SNAP prints out the simulation results on the printer, monitor screen, or a disk file. You select the type of display (alphanumeric or graphic), the time range, and the time scale for the printout.

In Step 12 (SimFlt), SNAP simulates the design with circuit faults, and reports the percentage of potential faults that can be detected with the given set of input test signals. Test signals may be specified as waveforms or by an ASCII file. A detailed fault coverage report is generated (.FLT file).

In Step 13 (Compiler), SNAP generates the fuse map for implementing the logic design. You select the PLD device type and then specify the input/output signal name associated with each device pin. SNAP optimizes the design for the selected device, generates the fuse map, and writes out the results in JEDEC format (.JED file). The percentage utilization of the on-chip PLD resources is reported on the screen and stored in a separate file (.USE).

In Step 14 (ModGen), SNAP takes the PLD device structure and fuse map, and generates a new netlist (.MOD file) based on the actual implementation of the logic design in the PLD device. This new netlist can be simulated in the same manner as the original design, allowing verification of the PLD implementation.

In Step 15 (TestVector), the test vectors (input signals and expected output signals) are converted to JEDEC format. This information can be downloaded to the device programmer machine along with the fuse map (.VEC file).

In Step 16 (DPI), the Device Programmer Interface, SNAP downloads the fuse map and test vectors to the PLD programmer machine through a serial port. The programmer machine uses the fuse map to program the PLD device, and the test vectors to test the device after programming.

The programmed device operates as specified by the schematics, logic equations, and state equations created in Steps 1 and 3.

Many of the steps described above are optional. The minimum steps necessary for a project are either ScCapture and NetGen, or Equations and NetConv, to specify the logic design; Merger to make the netlist; Compiler to generate the fuse map; and DPI to download the fuse map to the device programmer. The other steps allow you to analyze and simulate the design, and to generate the test vectors.

Hardware and Software Requirements

SNAP requires the following computer resources:

- IBM PS/2, AT, XT or compatible computer
- MS-DOS operating system, version 2.0 or higher
- 640 Kbytes RAM
- Hard disk drive: 10 Mbytes (20 Mbytes or more preferred)
- Floppy disk drive
- Monitor: Hercules, EGA, or VGA recommended for schematic capture
- Text editor software

Installation

The SNAP software is provided on a set of floppy diskettes. Two functionally identical sets are provided: a $5^1/_4$ inch set and a $3^1/_2$ inch set.

The files are stored on the diskettes in compressed-data format, so you cannot simply copy the files to the hard disk. Instead, use the installation program provided on the diskettes. Running the installation program is straightforward. The program takes care of creating a SNAP subdirectory (if it doesn't already exist), and automatically "decompresses" the SNAP files and transfers them to the hard disk.If you have an earlier version of SNAP installed on your system, first make a backup of all data files (if any) in your SNAP subdirectory. To ensure that you don't lose any valuable files, make a separate, complete backup of the SNAP subdirectory using the BACKUP command or a backup utility program. Then delete all the files from the SNAP subdirectory.

If you are upgrading from SLICE, you can install SNAP without removing SLICE. Once you are familiar with SNAP, you can delete SLICE from the hard disk.

Signetics Logic Integration Computer Environment — SLICE 1.08

FEATURES

- Easy to learn and use
- Supports Signetics PLD line
- State or Boolean equation entry
- Fuse table editor
- Test vector editor
- Boolean equation extractor
- JEDEC fusemap compiler
- Interfaces to standard PLD programmers
- Upgradeable to SNAP

PRODUCT SUPPORT

SLICE supports the Signetics line of PLDs, which ranges from high-speed PAL®-type devices to complex Programmable Macro Logic circuits. It will also support new Signetics PLDs as they are introduced. The devices currently supported are:

Programmable Logic Arrays:

PLUS153 PLS100
PLUS173

Programmable Macro Logic:

PLHS501 PML2852
PML2552

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PLS155 PLC42VA12
PLS157 PLC415
PLS159 PLS105
PLS167 PLUS105
PLS168 PLUS405
PLS179

Programmable Array Logic

PLUS20L8 PLUS16L8
PLUS20R8 PLUS16R8
PLUS20R6 PLUS16R6
PLUS20R4 PLUS16R4
10H20EV8 PLQ22V10
10020EV8 PLC18V8Z
PHD48N22 PL22V10
PHD16N8

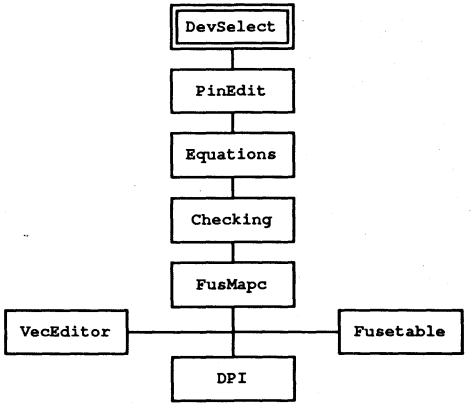
GENERAL DESCRIPTION

Sit down at your PC, install the SLICE software, and **you'll be programming PLDs within the hour**. SLICE (Signetics Logic Integration Computer Environment) provides all the functions you need for speedy PLD development without the tedious learning curve that accompanies other PLD design tools. **It allows first–time users to immediately produce a working PLD design—in the very first session.**

SLICE, which supports Signetics PLD line, is **easy to understand and simple to use.** Select a PLD, assign input and output pins and enter the desired equations in either Boolean or state form. SLICE then checks the equations for errors. It automatically generates a JEDEC-format fuse map for downloading to a PLD programmer.

As easy as 1, 2, 3:

1. **Select device and enter pins.**
2. **Enter equation.**
3. **Generate fuse map and download to device.**



PAL is a trademark of AMD.

Signetics Logic Integration Computer Environment — SLICE 1.08

Boolean Equation Extractor

FROM THIS:

```
L0000
11111111111111011101111011111111111111111
00000000000000000000000000000000000000000
00000000000000000000000000000000000000000
00000000000000000000000000000000000000000
00000000000000000000000000000000000000000
00000000000000000000000000000000000000000
00000000000000000000000000000000000000000
00000000000000000000000000000000000000000
11111111111111011111111111111111111011111
```

TO THIS:

```
@LOGIC EQUATION
S.D     =/(ASN*RWN*/DREQN1+S*/DREQN1);
```

AUTOMATICALLY • IMMEDIATELY • EFFORTLESSLY

Fully menu driven, SLICE incorporates a **fuse table editor** for making quick modifications to the design and a test vector editor for input of test vectors.

A built-in Boolean equation extractor allows existing PLDs to be used as the basis for a new design. The extractor reads JEDEC information from a PLD and creates a file containing the corresponding Boolean equations. The result can then be used to consolidate several PLD designs into a single, denser part.

And SLICE is **upward compatible with Signetics extensive design suite, SNAP.** SNAP, in fact, is a superset of SLICE. Among other enhancements, it provides full logic and fault simulation capabilities and design entry using the popular Data I/O DASH and OrCAD STD IV schematic capture tools. Compatibility means users can move up to SNAP for more complex design, while making full use of files created under SLICE.

ORDERING INFORMATION

To order your **FREE** SLICE 1.08 package, contact your local Signetics sales or representative office.

INTERPRETING THE SLICE FUSETABLE

A PLD fusetable or program table is a representation of how the device is actually programmed. It may be used to hand code the device, or more importantly, check that the design software implemented the design efficiently. Sometimes the way equations are written affects their implementation. It is recommended if a change in the program table is desired, that it NOT be modified directly. The original equations should be edited, compiled and a new JEDEC fuse table generated.

SLICE contains a module called 'Fusetable' which is a program table editor. It reads in the JEDEC fuse table (.JED file) and displays the program table on the screen. The program tables displayed are similar in appearance to the program tables printed on device data sheets and in the Signetics PLD Data Manual. SLICE fusetable representations differ slightly from those in data sheets. Data sheet program tables contain boxes, headers and labeling surrounding each section while SLICE contains a box in the upper right of the screen describing the cursor location. The characters describing the different fusing configurations are the same.

We will start out first by looking at a simple PHD16N8 program table. Next, different device program tables will be presented from devices of varying levels of complexity up to the PLHS501. The concepts used in all program tables are similar and once the user is familiar with the character representations used, any program table should be easy to interpret. Three areas of connections to especially note are the input/feedback buffers to product terms, OR gate inputs, and JK type flip-flop inputs. Each of these areas either use different or have unique definitions of the fusing representation characters.

The PHD16N8 is a very simple and useful high-speed device. It contains only 16 product terms (AND gates), 8 of which are connected through 3-State inverters to pins. The remaining 8 product terms control the 3-State function of the output buffers. It contains no OR gates. Each product term may receive inputs from up to 16 sources. There are 10 direct input pins and 6 feedbacks from bidirectional pins. Each possible input source goes through a buffer which has an inverting and a non-inverting output. Four characters are therefore required to show how each input source is connected. A SLICE representation of the program table is shown below with four product terms programmed.

```
----------------
--------HH------
----------------
---------L------
0000000000000000
0000000000000000
0000000000000000
0000000000000000
0000000000000000
0000000000000000
0000000000000000
0000000000000000
0000000000000000
0000000000000000
0000000000000000
```

There are 16 lines of 16 characters. Each line represents a product term. Each character represents the way an input source is connected to the product term. By moving the cursor around the program table, a box in the upper right of the screen will display the product term number and input designator. In the PHD16N8 program table, product terms controlling the output buffer 3-State function are arranged in the program table immediately above the product term for the output function. The four characters used to denote connections between an input or feedback buffer and a product term are H, L, –, and 0.

A zero (0) is the default or virgin state designator for the connection between an input buffer and product term. It indicates that both the non-inverting and inverting outputs from the buffer are connected to a product term's input. This has the effect of holding the product term's input and thus it's output LOW. A zero is usually not found on a row alone. To hold a product term low, it is better to connect all inputs of a product term to all buffer outputs. This is because the two paths through a buffer do not have equal delays. If only one buffer was used to hold a product term LOW, any signal on the input of the buffer may cause a glitch on the output of the product term.

A dash (–) is the opposite of a zero. It denotes neither the non-inverting or inverting output of a buffer is connected to the product term. If all of the inputs to a product term are dashed, then an internal pull-up guarantees that the output of the product term will be HIGH. This is used frequently for product terms controlling 3-State output buffers. In the PHD16N8 example above, the first and third product terms control the 3-State output buffers of the second and fourth product terms. They are all dashed so the two outputs are constantly enabled. The other 3-State control product terms are all zeroed so the unused outputs are in a high-impedance mode.

The H and L characters denote respectively a connection between only the non-inverting and inverting buffer outputs and the product term's input. Reading the H and L characters on a specific product term's row almost makes the device appear to be a collection of many comparators. For example, the second product term of the PHD16N8 program table above is:

```
--------HH------
```

The output of the product term will only be HIGH when the inputs match that pattern. In other words, the output will only be HIGH when I0 is HIGH AND I2 is HIGH. The fourth product term is:

```
---------L------
```

The output of this product term will be HIGH only when I0 is LOW. Note that the PHD16N8 has a 3-State inverting buffer following the product term. Therefore, the device pin will be LOW when the product term is HIGH.

A FIXED-OR architecture PLD such as the PLQ22V10 is represented by the following program table segment.

```
HHHHHHHHHH
DDDBBBBBBB
----------------------
------------------L--
00000000000000000000
00000000000000000000
00000000000000000000
00000000000000000000
00000000000000000000
00000000000000000000
00000000000000000000
----------------------
-------------------LHH
-------------------HLH
-------------------HLL
-------------------LLL
```

At the top of the program table are two lines which are shorter than the regular product term lines. These lines indicate the functions of each output macrocell (OMC). When the cursor is moved over the top row, the upper right box of SLICE will show POLARITY. Each character indicates how a particular output's polarity is programmed, either H or L indicating Active-High or Active-Low. Output F9 is on the left and F0 is on the right. The next line will show CONTROL indicating whether an OMC is set for D-type flip-flop or combinatorial output. Valid characters in this line are D for flip-flop and B for bidirectional combinatorial output.

The OR terms are not shown by SLICE because they are fixed. If the cursor is moved over a product term the indicator in the upper

right of the editor will show with which output pin the product term is associated. The 3-State control product term for a specific output occurs before the associated group of ORed product terms. For example, if the cursor is moved over the first product term, the indicator will show OE9-P23 which means that this product term is the output enable control for output F9. Moving the cursor down to the second product term shows P0-F9 which indicates this term is one which feeds into the OR gate of output F9.

The next program table segment is from a PLUS153. This segment is from the top portion of the program table.

```
------LH----------A.AAAAAAAA
------HL----------A.AAAAAAAA
------HH----------.AAAAAAAAA
00000000000000000..AAAAAAAA
00000000000000000..AAAAAAAA
00000000000000000..AAAAAAAA
```

A new section has been added to what we've seen previously. The new section indicates the programming of the OR array and is represented on the right portion by "A" and dot (.) characters. In any PLA architecture device the OR array is connectable to any product term. This enables product terms to be 'shared' between outputs. For example, if an output called OUT1 had an equation of "OUT1 = IN1 * IN2 + IN3" and OUT2 had an equation of "OUT2 = IN1 * IN2" only two product terms would be needed for a PLA while three would be needed for a FIXED-OR architecture device. One product term (IN1 * IN2) is common to both outputs and in a PLA may be connected to both OUT1 and OUT2. The FIXED-OR device would have to duplicate this product term – one for each output. In addition, a bipolar PLA device may even be reprogrammed if the changes are small. This can be achieved by disconnecting the unwanted product term from the OR array, adding the desired product term to the end of the program table and connecting it to the desired output.

The OR section of the PLUS153 program table consists of 10 columns, one for each output and 24 rows, one for each possible product term connection (the other 10 product terms control the 3-State output buffers). We noted in the preceding paragraphs for product terms that each input buffer had both inverting and non-inverting outputs and thus four characters were required to describe possible connections. The AND gates only have only one output and therefore only 2 characters are needed to represent a connection and lack thereof. This is denoted by an A and a dot (.) respectively. Also, this section is read vertically, NOT horizontally as the product term inputs. If a PLUS153 logic diagram is rotated 90 degrees, the relationship to the program table should be obvious.

A section of an adder example is shown below.

```
------LH----------A.AAAAAAAA
------HL----------A.AAAAAAAA
------HH----------.AAAAAAAAA
00000000000000000..AAAAAAAA
00000000000000000..AAAAAAAA
00000000000000000..AAAAAAAA
```

In this example outputs B(9) and B(8) are used. The remaining outputs are not used. The first and second product terms are connected to output B(9) and the third is connected to B(8). Notice that these product terms are also connected to all unused outputs. This does not cause any problems because of the 3-State control fusing as shown by the following segment from the end of the same PLUS153 program table.

```
00000000000000000..AAAAAAAA
00000000000000000..AAAAAAAA
00000000000000000
00000000000000000
00000000000000000
00000000000000000
00000000000000000
00000000000000000
00000000000000000
------------------
------------------
HHLLLLLLLL
```

FIXED-OR architecture devices have their 3-State output control product term distributed between sections of OR groupings. PLA devices have control product terms displayed at the end of their program table. The outputs B(9) and B(8) have their 3-State output buffer constantly enabled as shown by the dashed product terms. The other enabling product terms are all zeroed, forcing the unused B pins into their high-impedance 3-State mode.

Leaving product terms connected to unused B pins gives an advantage if additional output pins are added at a later time. If another output is added that requires a product term which is already used by an output, then it may be possible to reprogram the old device with the new pattern.

A minor section of the PLUS153 fusemap occurs as the last line as shown above. It consists of 10 characters which may be either H or L. These characters show the polarity of the outputs. An 'H' denotes no inversion or the output is 'Active-High'. An 'L' denotes an inversion or the output is 'Active-Low'. In the adder example, B(9) and B(8) are both 'Active-High'.

So, just to quickly review the PLUS153 adder example program table, three product terms were programmed. Two for the B(9) output which when read from the fusemap translates to B(9) = I0 * /I1 + /I0 * I1. This is an AND-OR implementation of the XOR function. Output B(8) used one product term of B(8) = I0 * I1. Both outputs are 'Active-High' and constantly enabled.

The following is a PLUS405 program table segment. However, the different sections have been separated by spaces for clarity.

```
LH
LLLLLLLLLLLLLLL
AA ---------------- -----LLL -----HLL HLL-----
AA ---------------- -----HLL -----HHH HHH-----
AA ---------------- -----LHL -----HHL HHL-----
AA ---------------- -----HHL -----HLH HLH-----
AA ---------------- -----LLH -----LLL LLL-----
AA ---------------- -----HLH -----LLH LLH-----
AA ---------------- -----LHH -----LHL LHL-----
AA ---------------- -----HHH -----LHH LHH-----
00 0000000000000000 00000000 00000000 00000000
00 0000000000000000 00000000 00000000 00000000
|| |               | |      | |      | |      |
01 2              17 18    25 26    33 34    41
```

The first row indicates the fusing configuration for the CLK1/CLK2 and INIT/OE options. The second row displays the flip-flop PRESET/RESET option for each flip-flop. In this example, all flip-flops will be reset upon an INIT signal on pin 19.

The next row is a representation of a product term within the PLUS405 and it's connections to the OR arrays. Like the PLUS153 it consists of two main sections. The product term array (columns 0 - 25) and the OR array (26 - 41). Ignoring columns 0 and 1 for the moment, columns 2 through 25 display the fusing of input buffers connected to the product term. It is exactly like the combinatorial devices we have seen so far. Columns 2 through 17 show the dedicated input buffer connection fusing and 18 through 25 display the feedback from the internal buried (not connected to pins) flip-flops. In this example, the output of the first product term will be HIGH when the outputs of flip-flops P2, P1 and P0 are all LOW.

The OR array differs in it's representation as compared to a device without JK or SR flip-flops because of the two inputs required for JK flip-flops. As the input buffer to product term connections consists of two buffer output lines being fused to a single product term input, the PLUS405 OR array section consists of one product term output being fused to two OR gate inputs - one or the J and one for the K flip-flop input. Four characters are required to represent the two fuses. The same characters are used as in the product term section. The PLUS405's OR array section is still read vertically for a single output but it can also be read horizontally to determine the next state. In the above program table, columns 26 - 33 are inputs to P7 - P0 (the internal flip-flops). Columns 34 - 41 are inputs to F7 - F0 which are the output flip-flops.

A zero (0) is also the default virgin state condition of the OR array section. It represents a connection of the product term output to both the J and K inputs. Unlike a zero in the product term section, a zero may be found alone on the line. It is used to toggle the flip-flop upon a clock. Counters may be efficiently constructed using this feature.

A dash (–) indicates that the product term does not connect to either the J or K. The flip-flop will remain in it's current state while being clocked.

An "H" indicates the product term connects to only the J input of the flip-flop. If the product term is HIGH and after a clock occurs, the flip-flop output will be HIGH.

An "L" indicates the product term connects to only the K input of the flip-flop. If the product term is HIGH and after a clock occurs, the flip-flop output will be LOW.

Sometimes columns 18 - 25 are called the "present state" inputs because they come directly from the buried flip-flops. Columns 26 - 33 are call the "next state" outputs as they connect to the buried flip-flops inputs and control to which state the flip-flops will transition.

Looking at the above program table we can determine into which state this machine will go given a present state. Assuming that an INIT pulse occurred, all flip-flops will be LOW (this was read from the second line). This will make the very first product term (third line) active or HIGH. Upon the rising edge of a clock pulse, the state will change to HLL (P2-P0) and the output also will change to HLL (F7-F5). The second product term (line four) will become HIGH and force a jump to HHH upon the next clock. This will cause the product term of line 10 to become active and force a jump to LHH. You should be able to follow the state machine from here back to state LLL.

Although this state machine did not use any of the direct inputs, adding a pattern to a product term would be quite easy. It would cause this state machine to wait in a state until the particular input pattern occurred on the input pins before proceeding to the next state.

Columns 0 and 1 show the fusing of the two complement arrays. A complement array is actually a NOR gate whose input is connectable to any or all product term outputs and whose input is connectable to any or all of the product terms input. It can be used as an illegal state detector, forcing a jump to a known state, or as an "ELSE" jump generator

The complement array's column is a little different from what we've seen so far. This is because the complement array input spans all of the product terms output (like a regular OR gate) but it's output is fed back into the product term input's section. Two fuses are represented by each character in the complement array column. A zero (0) indicates both the output of the product term is connected to the input of the complement array and the output of the complement array is connected to the product term's input. This condition is not used for a product term that has other inputs programmed because it could cause oscillations.

A dash (–) indicates neither the output of the product term is connected to the complement array or the output of the complement array is connected to the input of the product term.

An "A" denotes connection only between the product term output and the input of the complement array. A dot (.) denotes a connection only between the complement array output and the input of the product term. Graphical representations of these connection options are listed in the PLUS405 data sheet.

A portion of a PLHS501 program table is shown in below.

```
HHHH
--------------------------------.....................................................................
H-L-------------------------------.....................................................................
--------------------------------..A...................................................................
--------------------------------AA..................................................................
--------------------------------.....................................................................
```

The first line indicates the state of the fuses enabling outputs B3-B0. An "H" indicates the 3-State output buffer is enabled. An "L" indicates the specific B pin's output buffer is permanently in the high-impedance mode.

The remaining lines of the PLHS501 program table indicate how the inputs to each NAND gate are configured. In the above representation, the dashes and dots occur on different lines. While viewing the program table with SLICE, the 32 dashes and 72 dots occur on one line. Cursor control keys may be used to scroll the screen horizontally and vertically. The upper portion of the program table display inputs to NAND gate that connect to output buffers followed by the 72 foldback NAND gates. The upper right status box of SLICE's program table editor always displays the name of the NAND gate currently under the cursor as well as which input is at the cursor intersection.

Each NAND gate of the PLHS501 has as it's inputs 24 dedicated input buffer outputs, 8 bidirectional pins feedback buffer outputs, and the outputs of 72 foldback NAND gates! That adds up to a 104 input NAND gate and the PLHS501 has 120 of them! The dashed portion of the line represents the 24 input and 8 bidirectional pins feedback buffer connections. Valid entries are H, L, –, and 0. The meanings are exactly like the inputs to product terms described in the previous device examples.

The remaining portion of the line contains dots (.) or "A" characters. This represents no connection or a connection to a foldback NAND gate's output. The specific NAND gate's name will be listed in the status box of the editor when the cursor is under an "A" character.

In the above example, the first NAND gate does not have anything connected to it. The second has I0 (pin 41) and I2 (pin 43). The output of this NAND gate will go LOW only when I0 is HIGH and I2 is LOW. The third NAND gate doesn't have any pin buffer inputs, but it does have the output of a foldback NAND gate (FB2) as an input. The fourth NAND gate has two foldback NAND gate outputs as inputs. They are FB0 and FB1. The fourth NAND gate's output will only go active LOW when both outputs of FB0 and FB1 are HIGH.

The fusetable or program table for a PLUS153 is actually quite simple. It is divided into two main sections which represent the AND array and the OR array sections of the actual device. These sections contain characters which represent the fusing connections of the arrays.

In a PLUS153, there are 18 buffers feeding into the inputs of 42 AND gates. Eight of these buffers are from input only pins (I0-I7) while the remaining 10 are from the bidirectional pins (B0-B9). Each buffer has a non-inverting and inverting output. Therefore, there are four possible output connections from each buffer to the input of an AND gate.

Notice in the program table the H,L,– and 0 characters which are located left of the 'A' and dot (.) characters. These characters represent the four possible input buffer connections to product terms (AND gates) and are read horizontally. There are 18 columns in this section, one for each buffer and there are 42 rows, one for each product term.

A zero (0) is the default or virgin state designator for the connection between a buffer and product term of the PLUS153. It indicates that both the non-inverting and inverting outputs from the buffer are connected to a product term's input. This has the effect of holding the product term's input and thus it's output LOW. A zero is usually not found on a row alone. To hold a product term low, it is better to connect all inputs of a product term to all buffer outputs. This is because the two paths through a buffer do not have equal delays. If only one buffer was used to hold a product term LOW, any signal on the input of the buffer may cause a glitch on the output of the product term.

A dash (–) is the opposite of a zero. It denotes neither the non-inverting or inverting output of a buffer is connected to the product term. If all of the inputs to a product term are dashed, then an internal pull-up guarantees that the output of the product term will be HIGH. This used frequently for product terms controlling the PLUS153's 3-State output buffers.

The H and L characters denote respectively a connection between only the non-inverting and inverting buffer outputs and the product term's input. Reading the H and L characters on a specific product term's row almost makes the device appear to be many comparators. For example, if a product term had "———H–L————" listed as it's inputs, then the output will only be HIGH when the inputs match that pattern. In other words, the output will only be HIGH when I0 is LOW AND I2 is HIGH.

The OR gate input connections are represented by the other half of the program table. There are 10 columns, one for each output and 24 rows, one for each possible product term connection (the other 10 product terms control the 3-State output buffers). We noted in the preceding paragraphs that each input buffer had both inverting and non-inverting outputs and thus four characters were required to describe possible connections. The AND gates only have only one output and therefore only 2 characters are needed the represent a connection and lack thereof. This is denoted by an A and a dot (.) respectively. Also, this section is read vertically, NOT horizontally as the product term inputs. If a PLUS153 logic diagram is rotated 90 degrees, the relationship to the program table should be obvious.

For example, a section of the adder example is shown below.

```
------LH----------A.AAAAAAAA
------HL----------A.AAAAAAAA
------HH----------.AAAAAAAAA
00000000000000000..AAAAAAAA
00000000000000000..AAAAAAAA
00000000000000000..AAAAAAAA
```

In this example the outputs B(9) and B(8) were named SUM and CY. The remaining outputs were not used. The first and second product terms are connected to SUM and the third is connected to CY. Notice that these product terms are also connected to all unused outputs. This does not cause any problems because of the 3-State control fusing as shown by the following segment from the end of the program table.

```
00000000000000000..AAAAAAAA
00000000000000000..AAAAAAAA
00000000000000000
00000000000000000
00000000000000000
00000000000000000
00000000000000000
00000000000000000
00000000000000000
00000000000000000
------------------
------------------
HHLLLLLLLL
```

The outputs SUM and CY have their 3-State output buffer constantly enabled as shown by the dashed product terms. The other enabling product terms are all zeroed, forcing the unused B pins into their high-impedance 3-State mode.

Leaving product terms connected to unused B pins gives an advantage if additional output pins are added at a later time. The PLA architecture of the PLUS153 allows product terms to be shared between two or more outputs. If another output is added that requires a product term which is already used by an output, then it may be possible to reprogram the old device with the new pattern.

A minor section of the PLUS153 program table occurs as the last line as shown above. It consists of 10 characters which may be either H or L. These characters show the polarity of the outputs. An 'H' denotes no inversion or the output is 'Active-High'. An 'L' denotes an inversion or the output is 'Active-Low'. In the adder example, SUM and CY are both 'Active-High'.

So, just to quickly review the adder example program table, three product terms were programmed. Two for the SUM output which when read from the fusemap translates to SUM = I0 * /I1 + /I0 * I1. This is an AND-OR implementation of the XOR function. Output CY used one product term of CY = I0 * I1. Both outputs were 'active-high' and constantly enabled.

Section 9
Third-Party Programmer/Software Support

INDEX

Signetics PLD programming guide

SIGNETICS PRODUCT NAME	ADVANTEST R4971 Revision	ADVIN PILOT-U84 Revision	BASIC UP2000 Revision	BP MICROSYSTEMS PLD-1100 Software Revision	BP MICROSYSTEMS CP-1128 Software Revision	DATA I/O* UNISITE Revision	DATA I/O* MODEL 2900 System Revision	DATA I/O* MODEL 3900 System Revision
PAL® DEVICES								
10H20EV8-4	–	–	2.25	1.45	1.78	3.8	–	–
10020EV8-4	–	–	2.25	1.45	1.78	3.8	–	–
PHD16N8-5	–	10.16	2.25	1.45	1.78	2.4	–	1.0
PHD48N22-7	–	–	2.25	–	–	3.4	–	1.1
PL22V10-10/-12/-15	–	10.32	2.28	1.81	1.81	3.5	1.5	1.1
PLC18V8Z-25/-35	–	10.16	2.25	1.45	1.78	2.6	1.0	1.0
PLUS16L8-7/D	C50	10.16	2.25	1.34	1.78	3.8	1.0	1.2
PLUS16R4-7/D	C50	10.16	2.25	1.34	1.78	3.8	1.0	1.2
PLUS16R6-7/D	C50	10.16	2.25	1.34	1.78	3.8	1.0	1.2
PLUS16R8-7/D	C50	10.16	2.25	1.34	1.78	3.8	1.0	1.2
PLUS20L8-7/D	C50	10.16	2.25	1.34	1.78	3.9	1.0	1.0
PLUS20R4-7/D	C50	10.16	2.25	1.34	1.78	3.9	1.0	1.0
PLUS20R6-7/D	C50	10.16	2.25	1.34	1.78	3.9	1.0	1.0
PLUS20R8-7/D	C50	10.16	2.25	1.34	1.78	3.9	1.0	1.0
PLA DEVICES								
PLS100	C50	10.35	–	–	1.78	2.2	1.0	1.0
PLS101	C50	10.35	–	–	1.78	2.2	1.0	1.0
PLS153/153A	C50	10.35	2.25	1.34	1.78	2.8	1.0	1.0
PLS173	C50	10.35	2.25	1.34	1.78	1.7	1.0	1.0
PLUS153-10/D/B	C50	10.35	2.25	1.34	1.78	3.6	1.0	1.1
PLUS173-10/D/B	C50	10.35	2.25	1.34	1.78	2.3	1.0	1.1
PLS DEVICES								
PLC415-16	–	–	2.25	–	1.78	2.6	1.0	1.0
PLC42VA12	–	10.32	2.25	1.50	1.78	3.5	1.6	1.0
PLS105/105A	C50	10.35	2.25	–	1.78	1.5	1.0	1.0
PLS155	C50	10.35	2.25	1.34	1.78	1.5	1.0	1.0
PLS157	C50	10.35	2.25	1.34	1.78	1.5	1.0	1.0
PLS159A	C50	10.35	2.25	1.34	1.78	3.0	1.0	1.0
PLS167/167A	C50	10.35	2.25	1.34	1.78	1.5	1.0	1.0
PLS168/168A	C50	10.35	2.25	1.34	1.78	1.5	1.0	1.0
PLS179	C50	10.35	2.25	1.34	1.78	3.3	1.0	1.0
PLUS105-55/-45	C50	–	2.25	–	1.78	3.6	1.6	1.0
PLUS405-55/-45/-37	C50	10.35	2.25	–	1.78	3.6	1.6	1.0
PML DEVICES								
PLHS501/501I	–	–	2.25	–	–	1.7	–	1.1
PML2552-35/-50	–	–	2.25	–	–	2.8	–	1.1
PML2852-35/-50	–	–	2.28	–	–	3.5	–	–

* See individual programmer reference guide for more details.
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Signetics PLD programming guide

DATA I/O* (continued)		LOGICAL DEVICES		SMS	STAG*	STREBOR	SYSTEM GENERAL	
MODEL 29B	**MODEL 60**	**ALLPRO40**	**ALLPRO88**	**SPRINT PLUS**	**ZL30A**	**PLP-S1A**	**SGUP-85A**	**TURPRO-1**
303A-011A Revision	**System Revision**	**Software Revision**	**Software Revision**	**System Revision**	**System Revision**	**Software Revision**	**System Revision**	**System Revision**
PAL® DEVICES								
–	–	1.50C	2.10	2/91	–	–	2.4	1.42
–	–	1.50C	2.10	2/91	–	–	2.4	1.42
V12	V15	1.50C	2.10	2/91	30A36	–	2.4	1.42
–	–	–	2.10	2/91	–	–	–	–
V14	V18	–	–	2/91	30B01	–	–	1.42
V09	V15	1.50C	2.10	2/91	30A31	–	2.4	1.42
V08	V14.2	1.50C	2.10	2/91	30A31	–	2.4	1.42
V08	V14.2	1.50C	2.10	2/91	30A31	–	2.4	1.42
V08	V14.2	1.50C	2.10	2/91	30A31	–	2.4	1.42
V08	V14.2	1.50C	2.10	2/91	30A31	–	2.4	1.42
V08	V14.2	1.50C	2.10	2/91	30A31	–	2.4	1.42
V08	V14.2	1.50C	2.10	2/91	30A31	–	2.4	1.42
V08	V14.2	1.50C	2.10	2/91	30A31	–	2.4	1.42
V08	V14.2	1.50C	2.10	2/91	30A31	–	2.4	1.42
PLA DEVICES								
V05*	V01	1.50C	2.10	2/91	30A01	–	–	–
V05*	V01	1.50C	2.10	2/91	30A01	–	–	–
V02	V12	1.50C	2.10	2/91	30A01	–	2.4	1.42
V02	V12	1.50C	2.10	2/91	30A01	–	2.4	1.42
V07	V15	1.50C	2.10	2/91	30A40	–	2.4	1.42
V07	V15	1.50C	2.10	2/91	30A40	–	2.4	1.42
PLS DEVICES								
V10	V17.1	1.50C	2.10	2/91	30A34	–	–	–
V12	V15	1.50C	2.10	2/91	30A34	–	2.4	1.42
V02	V12	1.50C	2.10	2/91	30A01	–	2.4	1.42
V02	V12	1.50C	2.10	2/91	30A01	–	2.4	1.42
V02	V13	1.50C	2.10	2/91	30A01	–	2.4	1.42
V02	V12	1.50C	2.10	2/91	30A25	–	2.4	1.42
V02	V12	1.50C	2.10	2/91	30A01	–	2.4	1.42
V02	V12	1.50C	2.10	2/91	30A01	–	2.4	1.42
V02	–	1.50C	2.10	2/91	30A27	–	2.4	1.42
V09	–	1.50C	2.10	2/91	30A37	–	–	1.42
V07	–	1.50C	2.10	2/91	30A31	–	2.4	1.42
PML DEVICES								
–	–	1.50C	2.10	4/91	30A22	FA	2.4	1.50
–	–	–	–	4/91	–	FC	–	1.50
–	–	–	–	–	–	FD	–	1.50

PLD programmer reference guide — Data I/O Corporation

Data I/O Corporation
10524 Willows Road, N.E.
Redmond, Washington 98073-9746
Telephone Number: (800) 247-5700

Signetics Part Number	Device Code	MODEL 29B Adapter Revision		UNISITE		MODEL 2900	MODEL 3900	MODEL 60 Adapter Revision		
		DIP	PLCC	Site 40/48	Chip/ Pin Site			System Revision	DIP	PLCC
PHD										
PHD16N8	1B8F	303A-011A;V12	303A-011B;V05	V2.4	V3.4	TBD	1.0	V15	360A001	360A006
PHD48N22	0960B2	—	—	V3.4****	V3.4**	—	1.1	—	—	—
ECL										
10H20EV8	14013B	—	—	V2.7	V2.7	—	—	—	—	—
10020EV8	14013B	—	—	V3.0	TBD	—	—	—	—	—
PAL®										
PLC18V8Z-35/-25	864F	303A-011A;V09	303A-011B;V04	V2.6	V2.8	1.0	1.0	V15	360A001	360A006
PL22V10	A628	303A-011A;V14	303A-011B;V04	V3.5	V3.5	1.5	1.1	V18	360A001	360A006
PLUS16L8	1B17	303A-011A;V08	303A-011B;V04	V3.8*	V3.8*	1.0	1.2	V14.2	360A001	360A006
PLUS16R8/R6/R4	1B24	303A-011A;V08	303A-011B;V04	V3.8*	V3.8*	1.0	1.2	V14.2	360A001	360A006
PLUS20L8	1B26	303A-011A;V08	303A-011B;V04	V3.9*	V3.9*	1.0	1.0	V14.2	360A001	360A006
PLUS20R8/R6/R4	1B27	303A-011A;V08	303A-011B;V04	V3.9*	V3.9*	1.0	1.0	V14.2	360A001	360A006
PLA										
PLS100/101	9601	303A-001;V01	—	—	—	1.0	1.0	—	—	—
PLS100/101	9661	303A-001;V05	—	V2.2	V2.2	1.0	1.0	V01	360A003	—
PLS153/A	9665	303A-011A;V02	303A-011B;V02	V2.8	—	1.0	1.0	V01	360A002	A ONLY
PLS153/A	9665	303A-001;V05	303A-011B;V02	V2.8	V2.8	1.0	1.0	V12	360A009	A ONLY
PLS173	9676	303A-011A;V02	303A-011B;V02	V1.7	—	1.0	1.0	V08	360A002	—
PLS173	9676	303A-001;V06	303A-011B;V02	V1.7	V1.7	1.0	1.0	V12	—	360A009
PLUS153B/D/-10	1B65	303A-011A;V07	303A-011B;V03	V3.6	V3.6	1.0	1.1	V15	360A001	360A009
PLUS173B/D/-10	1B76	303A-011A;V07	303A-011B;V03	V2.3	V2.3	1.0	1.1	V15	360A002	360A009
PLS										
PLC415-16	86AA	303A-011A;V10	303A-011B;V04	V2.6	V2.7	1.0	1.0	V17.1	360A003	TBD
PLC42VA12	868A	303A-011A;V12	303A-011B;V05	V3.5	V3.5	1.6	1.0	V15	360A002	TBD
PLS105/A	9603	303A-011A;V02	—	V1.5	—	1.0	1.0	V01	360A003	A ONLY
PLS105/A	9603	303A-001;V01	—	—	—	1.0	1.0	V12	—	—
PLS105/A	9663	303A-001;V05	303A-011B;V02	V1.5	—	1.0	1.0	—	360A003	—
PLS105/A	9663	303A-011A;V02	303A-011B;V02	V1.5	V1.5	1.0	1.0	V01	—	360A008
PLUS105-45/-55	1B63	303A-011A;V09	303A-011B;V04	V3.6	V3.6	1.6	1.0	—	—	—
PLS155	9667	303A-011A;V02	303A-011B;V02	V1.5	—	1.0	1.0	V01	360A002	—
PLS155	9667	303A-001;V05	303A-011B;V02	V1.5	V1.5	1.0	1.0	V12	—	360A009
PLS157	9668	303A-001;V05	303A-011B;V02	V1.5	—	1.0	1.0	V13	360A002	—
PLS157	9668	303A-011A;V02	303A-011B;V02	V1.5	V1.5	1.0	1.0	V13	—	360A009
PLS159A	6466	303A-011A;V02	303A-011B;V02	V3.0	V2.8	1.0	1.0	V12	360A002	360A009
PLS159A	6466	—	—	V3.0	—	1.0	1.0	—	—	—
PLS167/A	9660	303A-011A;V02	303A-011B;V02	V1.5	V1.5	1.0	1.0	V05	360A002	—
PLS167/A	9660	—	—	—	—	1.0	1.0	V12	—	360A009
PLS168/A	9674	303A-011A;V02	303A-011B;V02	V1.5	V1.5	1.0	1.0	V05	360A002	—
PLS168/A	9674	303A-001;V06	—	—	—	1.0	1.0	V12	—	360A009
PLS179	9677	303A-011A;V02	303A-011B;V02	V3.3	V3.3	1.0	1.0	TBD	TBD	TBD
PLUS405-37/-45/-55	1B79	303A-011A;V07	303A-011B;V04	V3.6	V3.6	1.6	1.0	TBD	TBD	TBD

PLD programmer reference guide — Data I/O Corporation

Signetics Part Number	Device Code	MODEL 29B Adapter Revision		UNISITE		MODEL 2900	MODEL 3900	MODEL 60 Adapter Revision		
		DIP	PLCC	Site 40/48	Chip/ Pin Site			System Revision	DIP	PLCC
PML										
PLHS501	1002	—	—	—	V1.7	—	1.1	—	—	—
PLHS502	01C05E	—	—	V2.4***	V3.2**	—	—	—	—	—
PML2552-35/-50	15908C	—	—	V2.8****	V3.1**	—	1.1	—	—	—
PML2852-35/-50	TBD	—	—	V3.5*****	V3.5	—	—	—	—	—

NOTES:

1. The software and hardware revisions listed are the first revisions released. All following revisions maintain support.
2. FOR UNISITE USERS: PLCC packages can be programmed on either the Chipsite or Pinsite adaptors.
3. FOR UNISITE USERS ONLY: Family codes listed above (the first two digits) must be preceeded with a "0" for PLCC packages. Pin codes listed above (the last two digits) must be preceeded with a "7" or "6" for PLCC packages. Also, product name might be preceeded by "-FN".
4. * This version required to program security fuse on newer product.
   Older parts can use Version 2.3 or later.
   ** Pinsite adaptor required to program and functionally test these products without a DIP to PLCC adaptor.
   *** Needs a 40-Pin DIP to 68-Pin PLCC adaptor available from Emulation Technology. Part Number: AS-68-40-O1P-6
   Pinsite is also available for programming and functional testing without an adaptor.
   **** Needs a 40-Pin DIP to 68-Pin PLCC adaptor that is available from Emulation Technology. Part Number: AS-68-40-04P-6
   Pinsite is also available for programming and functional testing without an adaptor.
   ***** Needs a 40-Pin DIP to 84-Pin PLCC adaptor available from Emulation Technology Part Number: AS-84-40-O1P-6YAM
   EMULATION TECHNOLOGY, INC.
   2368B Walsh Avenue, Building D
   Santa Clara, California 95051
   Telephone No. (408) 982-0660
   Fax. No. (408) 982-0664
5. DEVICE CODE: XXYY
   XX = FAMILY CODE
   YY = PIN CODE

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PLD programmer reference guide — Stag Micro Systems, Inc.

STAG MICRO SYSTEMS, INC.

Western Area:
1600 Wyatt Drive, Suite 3
Santa Clara, CA 95054
(408) 988-1118

Eastern Area:
3 Northern Blvd., Suite B4
Amherst, NH 03031
(603) 673-4380

SIGNETICS PART NUMBER	DEVICE CODES		MODEL ZL30	MODEL ZL30A	
	FAMILY CODES	PIN CODES	(DIP ONLY)	SYSTEM REVISION	PLCC ADAPTER
PHD DEVICES					
PHD16N8-5	10	167	30A36	30A36	30A001
ECL DEVICES					
10H/10020EV8	--	--	--	--	--
PAL® DEVICES					
PL22V10-10/-12/-15	12	070	--	30B01	TBA
PLC18V8Z	12	205	30A34	30A34	30A001
PLUS20L8D/-7	11	56	30A31	30A31	30A001
PLUS20R8D/-7	11	57	30A31	30A31	30A001
PLUS20R6D/-7	11	58	30A31	30A31	30A001
PLUS20R4D/-7	11	59	30A31	30A31	30A001
PLUS16L8D/-7	11	29	30A31	30A31	30A001
PLUS16R8D/-7	11	30	30A31	30A31	30A001
PLUS16R6D/-7	11	31	30A31	30A31	30A001
PLUS16R4D/-7	11	32	30A31	30A31	30A001
PLA DEVICES					
PLS100/101	13	00	30A01	30A01	30A001
PLS153/153A	14	05	30A01	30A01	30A001
PLUS153B/D/-10	11	05	30A39S	30A39S	30A001
PLS173	15	96	30A01	30A01	TBA
PLUS173B/D/-10	11	96	30A39S	30A39S	TBA
PLS DEVICES					
PLS105/105A	13	02	30A01	30A01	30A001
PLUS105-45/-55	11	02	30A39	30A37	30A001
PLC415	12	177	30A34	30A34	30A001
PLC42VA12	12	197	30A45	30A45	30A001
PLS155	14	06	30A01	30A01	30A001
PLS157	14	07	30A01	30A01	30A001
PLS159A	13	08	30A25	30A25	30A001
PLS167/167A	15	91	30A01	30A01	30A001
PLS168/168A	15	97	30A01	30A01	30A001
PLS179	15	130	30A27	30A27	30A001
PLUS405-37/-45/-55	11	138	30A31	30A31	30A001
PML DEVICES					
PLHS501	10	133	N/A	30A22♦	30A101

NOTES:
The software and hardware revisions listed are the earliest revisions that support these products. Later revisions can also be assumed to support these products.

♦ Requires 30A101 adaptor; includes PLCC support.

PLD programmer vendors contact guide

COMPANY	LOCATION	PERSON TO CONTACT	CERTIFICATION
Advantest Corporation	3945 Freedom Circle., Ste. 1100 Santa Clara, CA 95054	Bud Howard (408) 970-9922	Certified 3/89
Advin Systems	1050-L E. Duane Avenue Sunnyvale, CA 94086	Wing F. Hui (408) 243-7000	Pending Update 75% done
American Reliance	9952 Eash Bladwin Place El Monte, CA 91731	John Goosseff Tel: (800) 654-9838 (818) 575-5110	Vendor to provide equipment
Aval Data	Daisan-Maruzen Building 6-16-6 Nishishinjuku Shinjuku-ku, Tokyo Japan 160	Toshiko Ishii 03-3344-2001	Vendor to provide equipment
B&C Microsystems	750 N. Pastoria Avenue Sunnyvale, CA 94086	(408) 730-5511	Pending new update
Basic Computer Systems AG	Wolfgang–Pauli–Gasse A–1140 Wien–Auhof, Austria	Tel: +43–222–9736360 Fax: +43–222–975915	Certified 4/89 UP2000
BP Microsystems	10681 Haddington, #190 Houston, TX 77043	Linda Morris (800) 225-2102	Certified PLD1100, CP1128
Data I/O	10525 Willow Road, N.E. Redmond, WA 98073-9746	(800) 247-5700	Certified Model 29/60 UNISITE, S1000, 2900
Eden Engineering	12505 Loma Rica Drive Grass Valley, CA 95945	Dan Mower (916) 272-2770	Vendor to provide eq.
Elan Digital Systems	538 Valley Way Milpitas, CA 95035	Tim Morse (800) 541-ELAN (408) 946-8495	Vendor to provide eq.
HiLo/Tribal Microsystems	44388 S. Grimmer Blvd. Fremont, CA 94538	Peter Huang (415) 623-8859	Pending new update
Logical Devices	1201 N.W. 65th Place Fort Lauderdale, FL 33309	Jeff Williams (800) 331-7766 (305) 974-0967 (FL only)	ALLPRO 40 Certified 7/91
Minato	3628 Madison Avenue, Ste. 5 North Highlands, CA 95660	Tel: (916) 348-6066 Fax: (916)348–0926	Certified System 1891 & 1910
Red Square Co.	2098 South Grand Avenue Suite H Santa Ana, CA 92705	Stanley Fiala (714) 751-1373	Vendor to provide eq.
SMS Sprint Plus/Expert	13720 Midway Road, Suite 105 Dallas, TX 75244	Encore Tech. Corp., Bob Trout (214) 233-3122	Certified Sprint Plus
	SMS – W. Steudel Im Morgental 13 D–8994 Hergatz, Germany	Tel: +49–7522–4460 Fax: +49–7522–8929	
Stag	1600 Wyatt Drive, Suite 3 Santa Clara, CA 95054	Terry Hepner (408) 988-1118	Certified ZL30A
Strebor PML Support Only	1008 North Nob Hill Drive America Fork, UT 84003	Larry Roberts (801) 756-3605	Certified PLP-S1/S1A
Sunrise Electronics	524 South Vermont Glendora, CA 81740	Larry Reese (818) 914-1926	Vendor to provide eq.
System General	510 South Park Victoria Dr. P.O. Box 361898 Milpitas, CA 95036-1898	Gary DeLucchi (408) 263-6667	Certified - SGUP-85/85A TURPRO-1
Xeltek	764 San Aleso Avenue Sunnyvale, CA 94086	Young Oh (408) 745-7974 (800) 541-1975	Pending new update

Approved software support

SIGNETICS PRODUCT NAME	SIGNETICS		ACUGEN	DATA I/O	ISDATA	LOGICAL DEVICES	MINC
	SLICE	SNAP	ATGEN	ABEL	LOG/iC	CUPL	PLDesigner
	Revision	Revision	Revision	Revision	Revision	Revision	Revision
PAL® DEVICES							
10H20EV8-4	1.0	1.6	2.47	3.1	3.4	4.2A	2.1
10020EV8-4	1.0	1.6	2.47	3.1	3.4	4.2A	2.1
PHD16N8-5	1.0	1.6	2.47	4.0	3.3	2.50A	2.1
PHD48N22-7	1.0	1.6	–	4.0	3.6	4.2A	–
PL22V10-10/-12/-15	1.05	1.8	2.47	3.1	3.4	2.11A	3.0
PLC18V8Z-25/-35	1.05	1.8	–	4.1	3.4	4.2A	2.1
PLUS16L8-7/D	1.0	1.6	2.47	3.1	3.3	1.01A	2.1
PLUS16R4-7/D	1.0	1.6	2.47	3.1	3.3	1.01A	2.1
PLUS16R6-7/D	1.0	1.6	2.47	3.1	3.3	1.01A	2.1
PLUS16R8-7/D	1.0	1.6	2.47	3.1	3.3	1.01A	2.1
PLUS20L8-7/D	1.0	1.6	2.47	3.1	3.3	2.0A	2.1
PLUS20R4-7/D	1.0	1.6	2.47	3.1	3.3	2.0A	2.1
PLUS20R6-7/D	1.0	1.6	2.47	3.1	3.3	2.0A	2.1
PLUS20R8-7/D	1.0	1.6	2.47	3.1	3.3	2.0A	2.1
PLA DEVICES							
PLS100	1.05	1.8	2.47	3.1	3.3	2.0A	2.1
PLS101	1.05	1.8	2.47	3.1	3.3	2.0A	2.1
PLS153/153A	1.0	1.6	2.47	3.1	3.3	2.15A	2.1
PLS173	1.0	1.6	2.47	3.1	3.3	2.15A	2.1
PLUS153-10/D/B	1.0	1.6	2.47	3.1	3.3	2.15A	2.1
PLUS173-10/D/B	1.0	1.6	2.47	3.1	3.3	2.1A	2.1
PLS DEVICES							
PLC415-16	1.0	1.6	2.47	4.0	–	4.0A	2.1
PLC42VA12	1.05	1.8	2.47	4.1	–	4.2A	–
PLS105/105A	1.0	1.6	2.47	3.1	3.3	2.0A	2.1
PLS155	1.05	1.8	2.47	3.1	3.3	2.0A	2.1
PLS157	1.05	1.8	2.47	3.1	3.3	2.0A	2.1
PLS159A	1.05	1.8	2.47	3.1	3.3	2.0A	2.1
PLS167/167A	1.05	1.8	2.47	3.1	3.3	2.0A	2.1
PLS168/168A	1.05	1.8	2.47	3.1	3.3	2.1A	2.1
PLS179	1.05	1.8	2.47	3.1	3.3	3.0A	2.1
PLUS105-55/-45	1.0	1.6	2.47	3.1	3.3	3.0A	3.0
PLUS405-55/-45/-37	1.0	1.6	2.47	3.1	3.3	3.0A	2.1
PML DEVICES							
PLHS501/501I	1.0	1.6	2.47	3.1	–	3.2A	–
PML2552-35/-50	1.0	1.6	–	–	–	–	–
PML2852-35/-50	1.05	1.8	–	–	–	–	–

®PAL is a registered trademark of Advanced Micro Devices, Inc.

Third-party software support

ABEL

Data I/O Corporation
10525 Willows Road N.E.
P.O. Box 97046
Redmond, WA 98073–9746
Telephone: (206) 881-6444

PART NUMBER	TYPE	PACKAGE	# PINS	DEVICE FILE	ABEL REV.
10020EV8	PAL®	DIP	24	EC20EV8A	3.1
10020EV8	PAL	PLCC	28	EC20EV8AC	4.2
10H20EV8	PAL	DIP	24	EC20EV8A	3.1
10H20EV8	PAL	PLCC	28	EC20EV8AC	4.2
PHD16N8	PAL	DIP	20	P16N8	4.0
PHD16N8	PAL	PLCC	20	P16N8	4.0
PHD48N22	PAL	PLCC	68	P48N22	4.0
PL22V10	PAL	DIP	24	P22V10	3.4
PL22V10	PAL	PLCC	28	P22V10C	3.4
PLC18V8Z	EPLD	DIP	20	P18V8Z	4.1
PLC18V8Z	EPLD	PLCC	20	P18V8Z	4.1
PLC415	FPLS	DIP	28	F415	4.0
PLC415	FPLS	PLCC	28	F415	4.0
PLC42VA12	FPLS	DIP	24	F42VA12	4.1
PLC42VA12	FPLS	PLCC	28	F42VA12	4.2
PLHS501	PML	PLCC	52	PML501	3.1
PLS100	FPLA	DIP	28	F100	3.1
PLS100	FPLA	PLCC	28	F100	3.1
PLS101	FPLA	DIP	28	F100	3.1
PLS101	FPLA	PLCC	28	F100	3.1
PLS105/105A	FPLS	DIP	28	F105	3.1
PLS105/105A	FPLS	PLCC	28	F105	3.1
PLS153/153A	FPLA	DIP	20	F153	3.1
PLS153/153A	FPLA	PLCC	20	F153	3.1
PLS155	FPLS	DIP	20	F155	3.1
PLS155	FPLS	PLCC	20	F155	3.1
PLS157	FPLS	DIP	20	F157	3.1
PLS157	FPLS	PLCC	20	F157	3.1
PLS159A	FPLS	DIP	20	F159	3.1
PLS159A	FPLS	PLCC	20	F159	3.1
PLS167/167A	FPLS	DIP	24	F167	3.1
PLS167/167A	FPLS	PLCC	28	F167C	4.2
PLS168/168A	FPLS	DIP	24	F168	3.1
PLS168/168A	FPLS	PLCC	28	F168C	4.2
PLS173	FPLA	DIP	24	F173	3.1
PLS173	FPLA	PLCC	28	F173C	4.2
PLS179	FPLS	DIP	24	F179	3.1
PLS179	FPLS	PLCC	28	F179C	4.2
PLUS105	FPLS	DIP	28	F105	3.1
PLUS105	FPLS	PLCC	28	F105	3.1
PLUS153	FPLA	DIP	20	F153	3.1
PLUS153	FPLA	PLCC	20	F153	3.1
PLUS16L8	PAL	DIP	20	P16L8	3.1
PLUS16L8	PAL	PLCC	20	P16L8	3.1
PLUS16R4	PAL	DIP	20	P16R4	3.1
PLUS16R4	PAL	PLCC	20	P16R4	3.1
PLUS16R6	PAL	DIP	20	P16R6	3.1
PLUS16R6	PAL	PLCC	20	P16R6	3.1
PLUS16R8	PAL	DIP	20	P16R8	3.1
PLUS16R8	PAL	PLCC	20	P16R8	3.1
PLUS173	FPLA	DIP	24	F173	3.1
PLUS173	FPLA	PLCC	28	F173C	4.2

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Third-party software support

ABEL – Data I/O Corporation (CONTINUED)

PART NUMBER	TYPE	PACKAGE	# PINS	DEVICE FILE	ABEL REV.
PLUS20L8	PAL	DIP	24	P20L8	3.1
PLUS20L8	PAL	PLCC	28	P20L8C	4.1
PLUS20R4	PAL	DIP	24	P20R4	3.1
PLUS20R4	PAL	PLCC	28	P20R4C	4.1
PLUS20R6	PAL	DIP	24	P20R6	3.1
PLUS20R6	PAL	PLCC	28	P20R6C	4.1
PLUS20R8	PAL	DIP	24	P20R8	3.1
PLUS20R8	PAL	PLCC	28	P20R8C	4.1
PLUS405	FPLS	DIP	28	F405	3.1
PLUS405	FPLS	PLCC	28	F405	3.1

Third-party software support

CUPL

Logical Devices, Inc.
1201 N.W. 65th Place
Ft. Laudedale, FL 33309
Telephone: (305) 974-0967

PART NUMBER	DEVICE MNEMONIC	# PINS	# FUSES	# OF P-TERMS	CUPL REV.
10020EV8	P1020EV8	24	3616	80	4.2a
10H20EV8	P1020EV8	24	3616	80	4.2a
82S100	F100	28	1928	48	2.00a
82S101	F100	28	1928	48	2.00a
82S105/105A	F105	28	3553	48	2.00a
82S153/153A	F153	20	1842	42	2.15a
PHD16N8	P16N8	20	512	16	2.50a
PHD48N22	F48N22	68	7008	73	4.2a
PLC18V8Z	F18V8Z	20	2689	72	4.2a
PLC415	F415	28	5751	68	4.0a
PLC42VA12	F42VA12	24	8994	10	4.2a
PLHS501	F501	52	15780	112	3.2a
PLS100	F100	28	1928	48	2.00a
PLS101	F100	28	1928	48	2.00a
PLS105/105A	F105	28	3553	48	2.00a
PLS153/153A	F153	20	1842	42	2.15a
PLS155	F155	20	2108	43	2.00a
PLS157	F157	20	2108	43	2.00a
PLS159A	F159	20	2108	43	2.00a
PLS167/167A	F167	24	3361	48	2.00a
PLS168/168A	F168	24	3553	48	2.10a
PLS173	F173	24	2178	42	2.15a
PLS179	F179	24	2452	43	3.0a
PLUS105-45/-55	F105	28	3553	48	3.0a
PLUS153B/D/-10	F153	20	1842	42	2.15a
PLUS16L8D/-7	F16L8	20	2048	64	1.01a
PLUS16R4D/-7	P16R4	20	2048	64	1.01a
PLUS16R6D/-7	P16R6	20	2048	64	1.01a
PLUS16R8D/-7	P16R8	20	2048	64	1.01a
PLUS173B/D/-10	P173	24	2178	42	2.10a
PLUS20L8D/-7	P20L8	24	2560	64	2.00a
PLUS20R4D/-7	P20R4	24	2560	64	2.00a
PLUS20R6D/-7	P20R6	24	2560	64	2.00a
PLUS20R8D/-7	P20R8	24	2560	64	2.00a
PLUS405	F405	28	5410	64	3.0a
PL22V10	P22V10	24	5828	130	2.11a

Third-party software support

PLDesigner

Minc, Incorporated
6755 Earl Drive
Colorado Springs, CO 80918
Telephone: (719) 590-1155

PART NUMBER	TEMPLATE NAME	TECHNOLOGY	PACKAGES	REVISION
PLS100	A100	TTL	DIP/PLCC	2.1
PLS101	A100	TTL	DIP/PLCC	2.1
PLS153/153A	A153	TTL	DIP/PLCC	2.1
PLUS153	A153	TTL	DIP/PLCC	2.1
PLS173	A173	TTL	DIP/PLCC	2.1
PLUS173	A173	TTL	DIP/PLCC	2.1
10020EV8-4	P20EV8	ECL	CDIP/PLCC	2.1
10H20EV8-4	P20EV8	ECL	CDIP/PLCC	2.1
PLUS16L8	P16L8	TTL	DIP/PLCC	2.1
PHD16N8-5	P16N8	TTL	DIP/PLCC	2.1
PLUS16R4	P16R4	TTL	DIP/PLCC	2.1
PLUS16R6	P16R6	TTL	DIP/PLCC	2.1
PLUS16R8	P16R8	TTL	DIP/PLCC	2.1
PLC18V8Z35	P18V8S	CMOS	DIP/CDIP/PLCC	2.1
PLUS20L8	P20L8	TTL	DIP/PLCC	2.1
PLUS20R4	P20R4	TTL	DIP/PLCC	2.1
PLUS20R6	P20R6	TTL	DIP/PLCC	2.1
PLUS20R8	P20R8	TTL	DIP/PLCC	2.1
PL22V10	P22V10	CMOS	DIP/PLCC	3.0
PLS105/105A	S105	TTL	DIP/PLCC	2.1
PLUS105	S105	TTL	DIP/PLCC	3.0
PLS155	S155	TTL	DIP/PLCC	2.1
PLS157	S157	TTL	DIP/PLCC	2.1
PLS159A	S159	TTL	DIP/PLCC	2.1
PLS167/167A	S167	TTL	DIP/PLCC	2.1
PLS168/168A	S168	TTL	DIP/PLCC	2.1
PLS179	S179	TTL	DIP/PLCC	2.1
PLUS405	S405	TTL	DIP/PLCC	2.1
PLC415	S415	CMOS	DIP/CDIP/PLCC	2.1

PLD software vendors contact guide

PRODUCT	LOCATION	CONTACT NUMBER
*Signetics SNAP/SLICE	811 E. Arques Avenue Sunnyvale, CA 94086	(800) 451-6644 Bulletin board #
ACUGEN Software, Inc. ATGEN	427-3 Amherst St., Ste. 391 Nashua, NH 03063	(603) 881-8821
Data I/O ABEL	10525 Willow Rd., N.E. Redmond, WA 98073-9746	(800) 247-5700
Logical Devices CUPL	1201 N.W. 65th Place Ft. Lauderdale, FL 33309	(800) EE1-PROM
Daisy/Cadnetix PLD Master	5775 Flatiron Parkway Boulder, CO 80301	(303) 444-8075
MINC PLD Designer	6755 Earl Drive Colorado Springs, CO 80918	(719) 590-1155
Mentor Graphics Corp. PLD Synthesis	8500 S.W. Creekside Place Beaverton, OR 97005	(503) 626-7000
OrCAD Systems ORCAD/PLD	1049 S.W. Baseline St., Suite 500 Hillsboro, OR 97123	(503) 640-9488
ISDATA LOG/ic	800 Airport Road Monterey, CA 93940	Shay Adams (800) 777-7359
	ISDATA GmbH Daimlerstr. 51 D–7500 Karlsruhe 21 Germany	Tel: +49–721–751087 Fax: +49–721–752634
Logic Automation	19500 N.W. Gibbs Drive P.O. Box 310 Beaverton, OR 87075	(503) 690-6900

* The SNAP and SLICE phone number connects to the SPG bulletin board. Compatible with 1200/2400 baud modems, messages can be left, problem files uploaded, and solution files downloaded.

Section 10
Package Outlines

INDEX

Package outlines

PLCC

1. Package dimensions conform to JEDEC specifications for standard Plastic Leaded Chip Carrier outline (PLCC) package.
2. Controlling dimensions are given in inches with dimensions in millimeters contained in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M – 1982.
4. "D–E" and "F–G" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm (0.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise when viewed from the top.
6. Lead material: Olin 194 (Copper Alloy) or equivalent, solder dipped.
7. Body material: Plastic (Epoxy).
8. Thermal resistance values are determined by Temperature Sensitive Parameter (TSP) method. This method uses the forward voltage drop of a calibrated diode to measure the change in junction temperature due to a known power application. Test conditions for these values are:

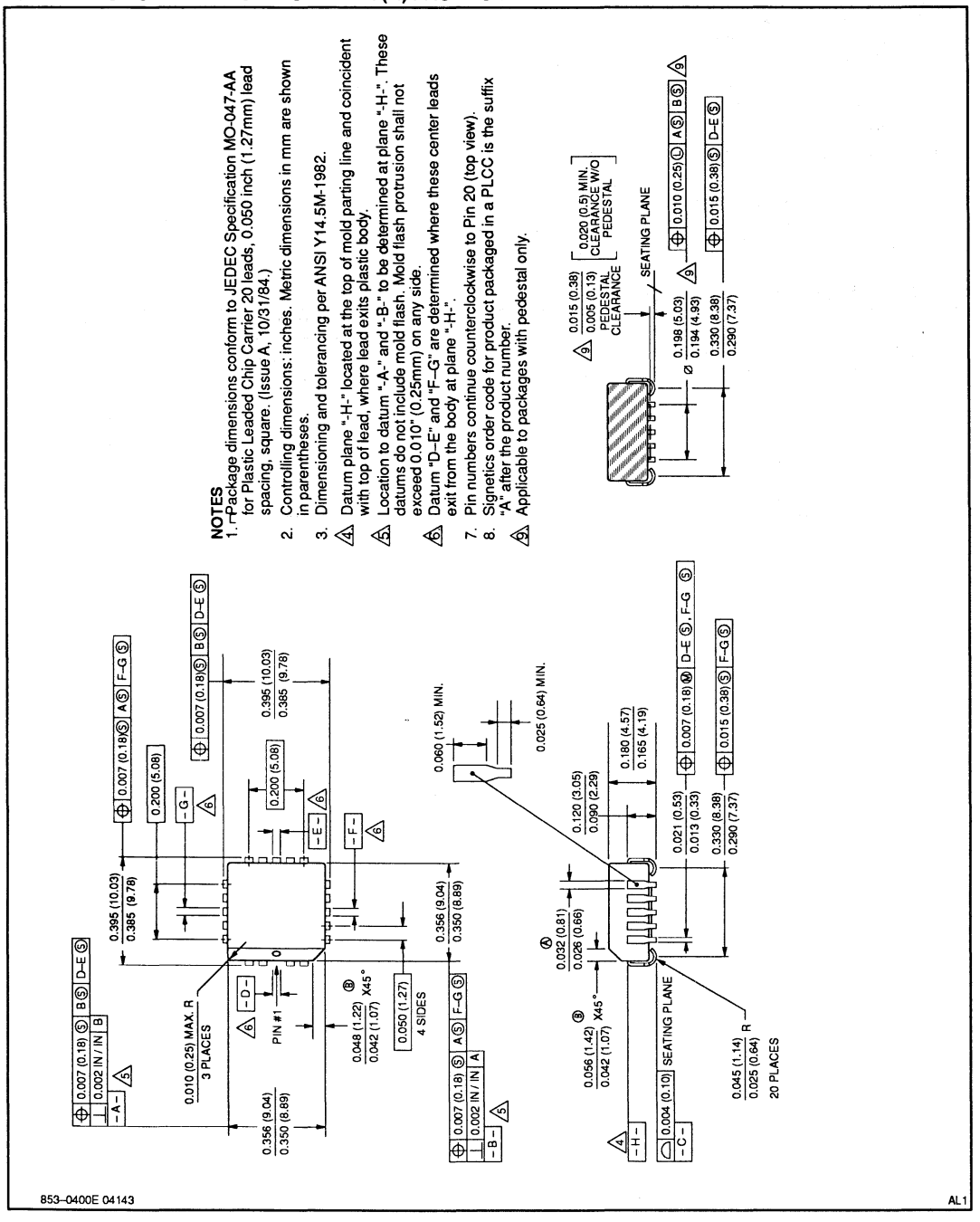
   Test Ambient—Still Air
   Test Fixture— θ_{JA}–Glass epoxy test board (2.24" × 2.24" × 0.062")
   θ_{JC}–Water cooled heat sink

PLASTIC LEADED CHIP CARRIER (PLCC)

NO. OF LEADS	PACKAGE CODE	DESCRIPTION	TYPICAL θ_{JA}/θ_{JC} VALUES (°C/W)	
			Average θ_{JA}	Average θ_{JC}
20	A	350mil-wide	70	30
28	A	450mil-wide	61	26
52	A	750mil-wide	42	14
68	A	950mil-wide	42	14
84	A	1150mil-wide	TBD	TBD

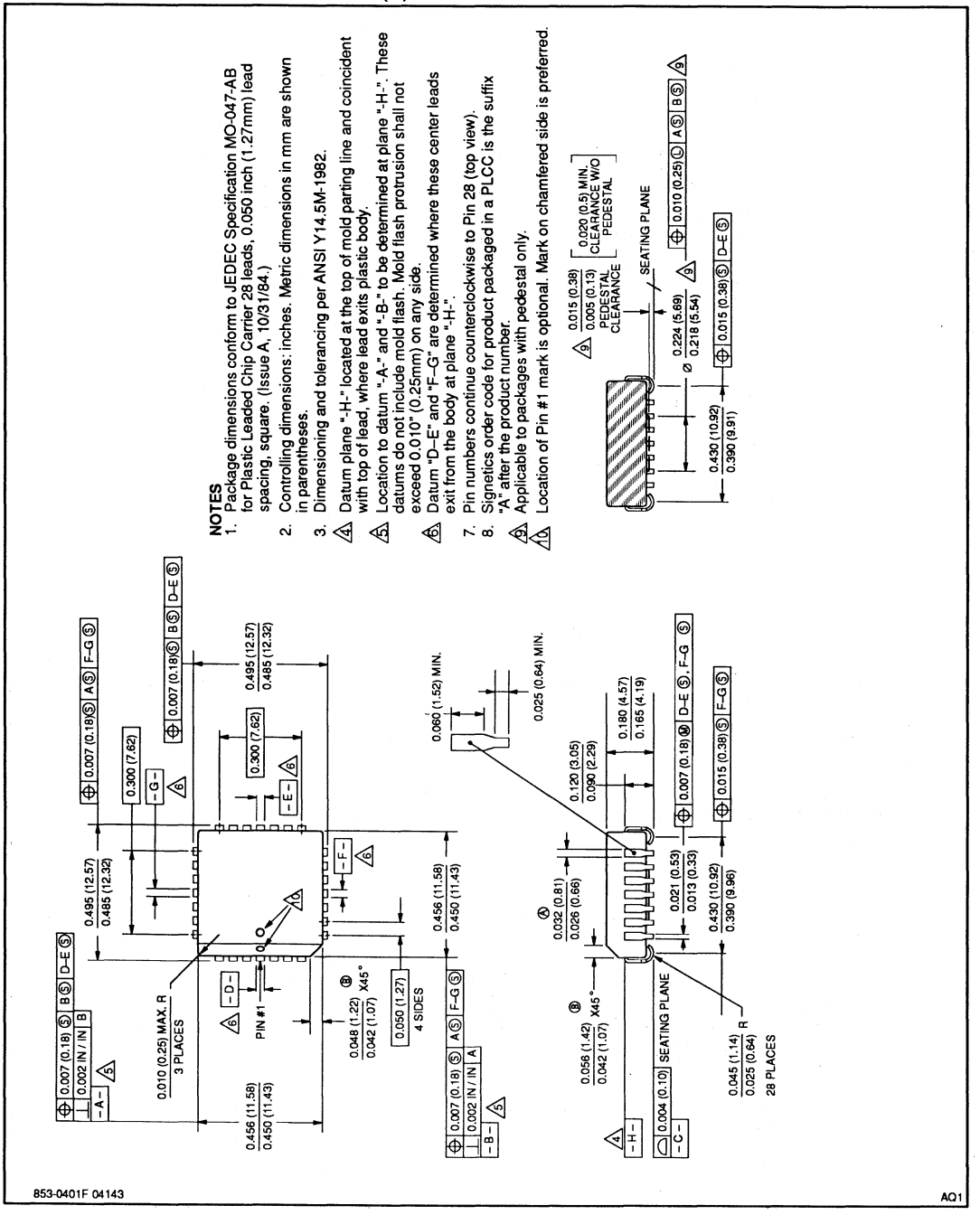
Package outlines

20-PIN PLASTIC LEADED CHIP CARRIER (A) PACKAGE



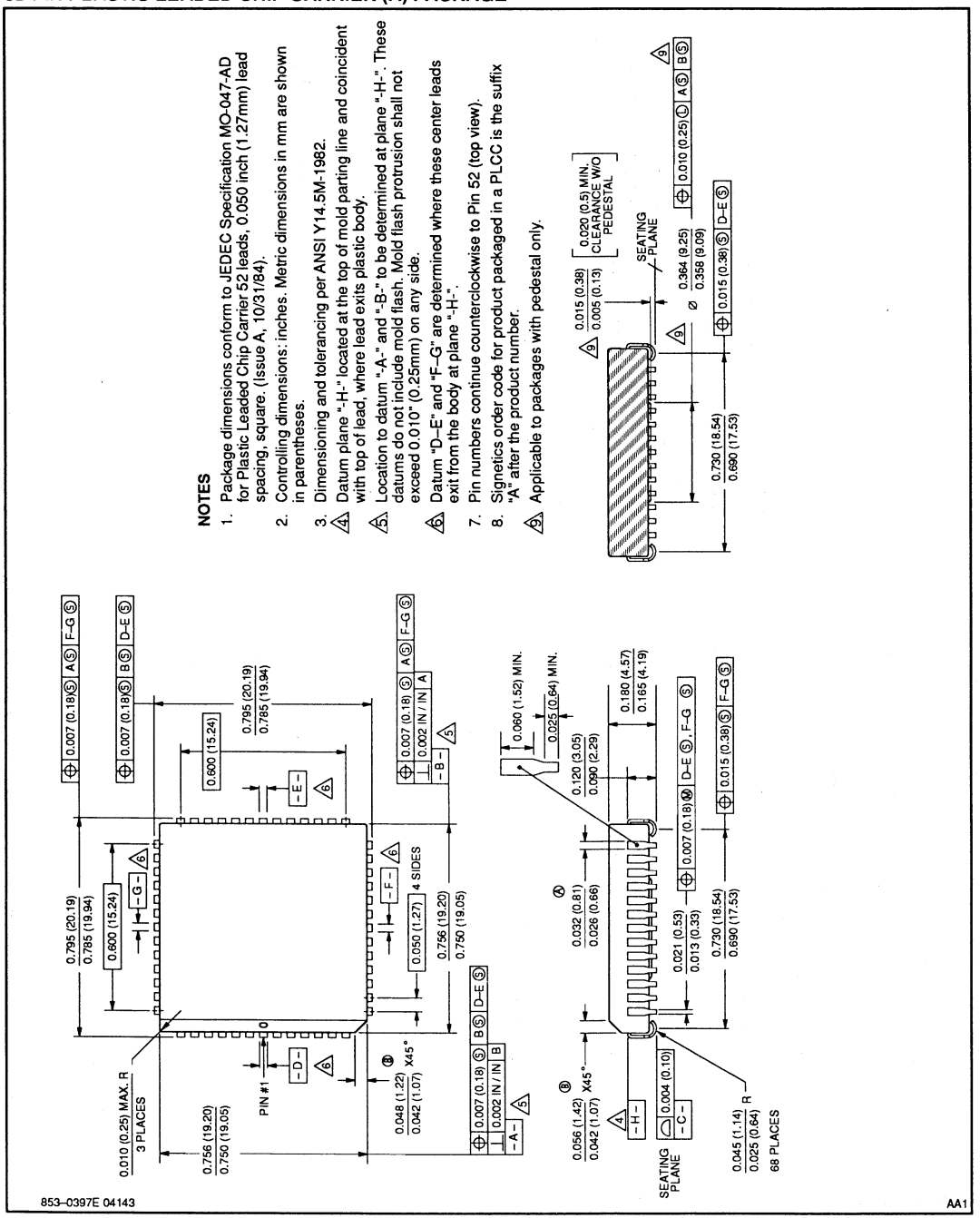
Package outlines

28-PIN PLASTIC LEADED CHIP CARRIER (A) PACKAGE



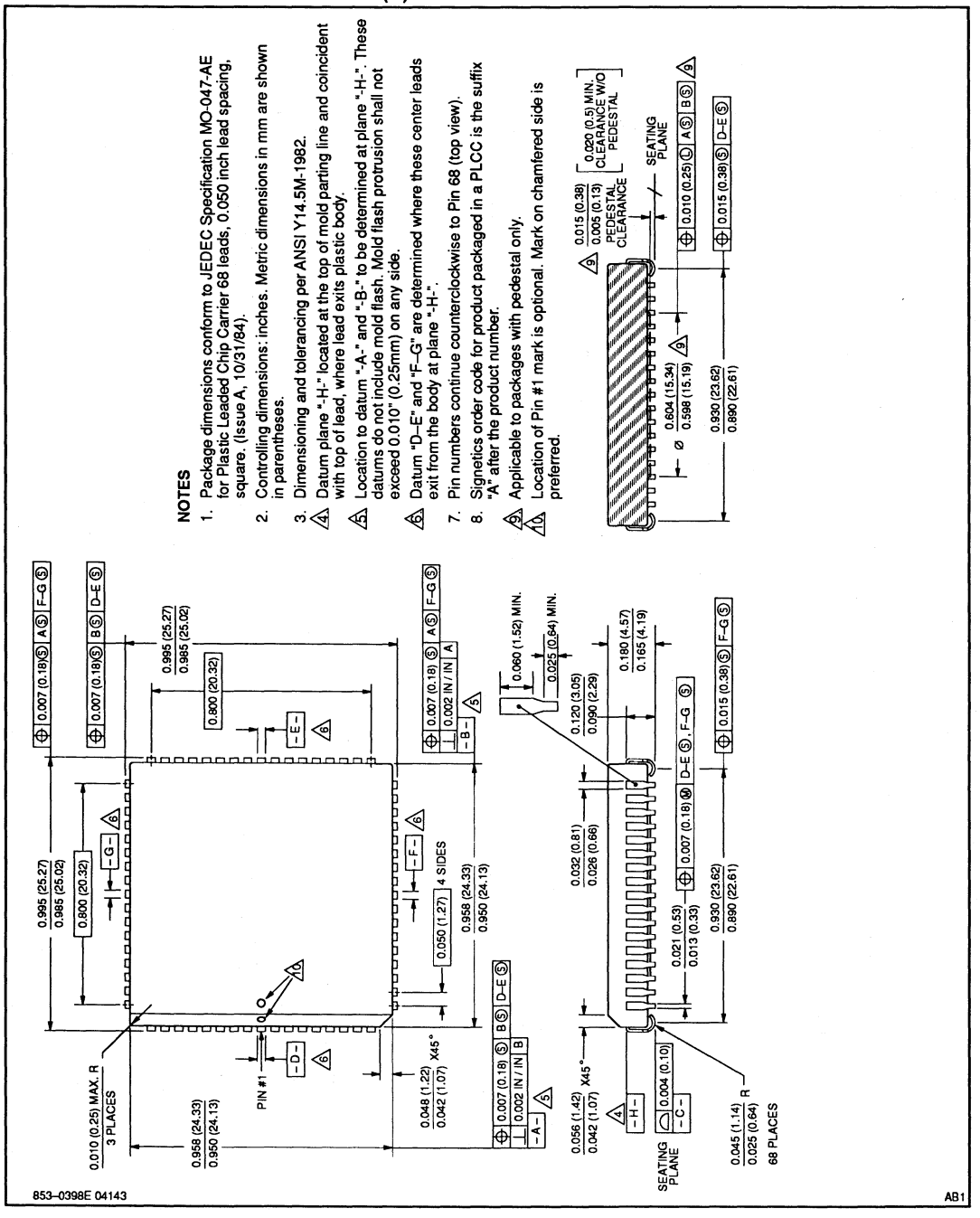
Package outlines

52-PIN PLASTIC LEADED CHIP CARRIER (A) PACKAGE



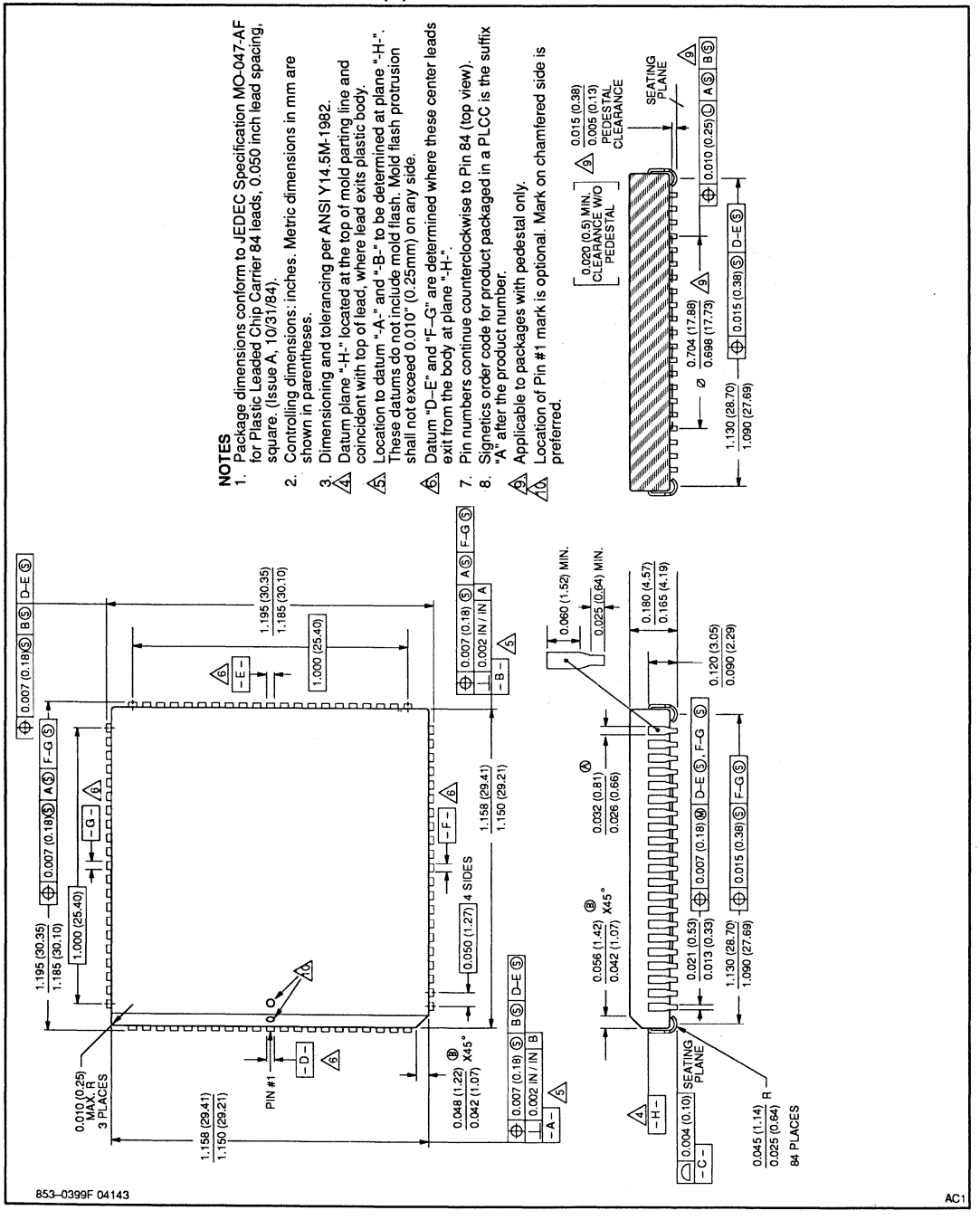
Package outlines

68-PIN PLASTIC LEADED CHIP CARRIER (A) PACKAGE



Package outlines

84-PIN PLASTIC LEADED CHIP CARRIER (A) PACKAGE



Package outlines

HERMETIC CERDIP

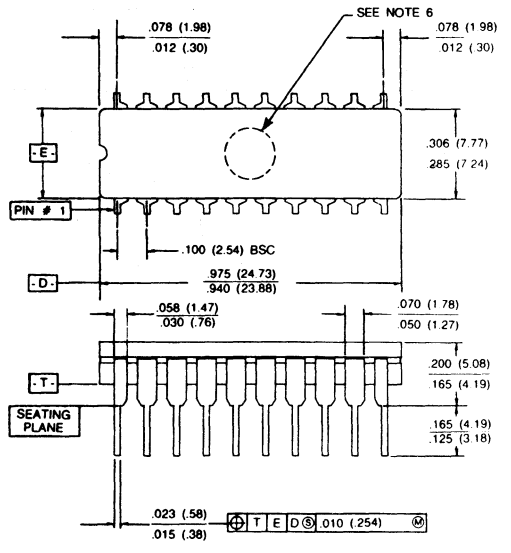
1. Package dimensions conform to JEDEC specifications for standard Ceramic Dual Inline (CERDIP) package.
2. Controlling dimensions are given in inches with dimensions in millimeters, mm, contained in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M – 1982.
4. Pin numbers start with pin #1 and continue counterclockwise when viewed from the top.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Lead material: ASTM alloy F-30 (Alloy 42) or equivalent – tin plated or solder dipped.
7. Body material: Ceramic with glass seal at leads.
8. Thermal resistance values are determined by Temperature Sensitive Parameter (TSP) method. This method uses the forward voltage drop of a calibrated diode to measure the change in junction temperature due to a known power application. Test conditions for these values follow:

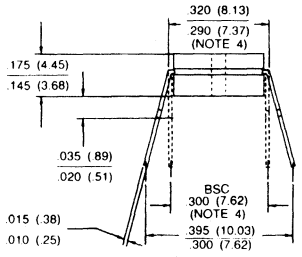
   Test Ambient—Still Air
   Test Fixture—θ_{JA}–Textool ZIF socket with 0.04" stand-off
   θ_{JC}–Water cooled heat sink

CERAMIC DUAL IN-LINE PACKAGES

NO. OF LEADS	PACKAGE CODE	DESCRIPTION	TYPICAL θ_{JA}/θ_{JC} VALUES (°C/W)	
			Average θ_{JA}	Average θ_{JC}
20	F, FA	300mil-wide	72	8
24	F, FA	300mil-wide	62	7
28	F, FA	600mil-wide	45	6

20-PIN (300 mils wide) CERAMIC DUAL IN-LINE (F) PACKAGE
20-PIN (300 mils wide) CERAMIC DUAL IN-LINE WITH QUARTZ WINDOW (FA) PACKAGE



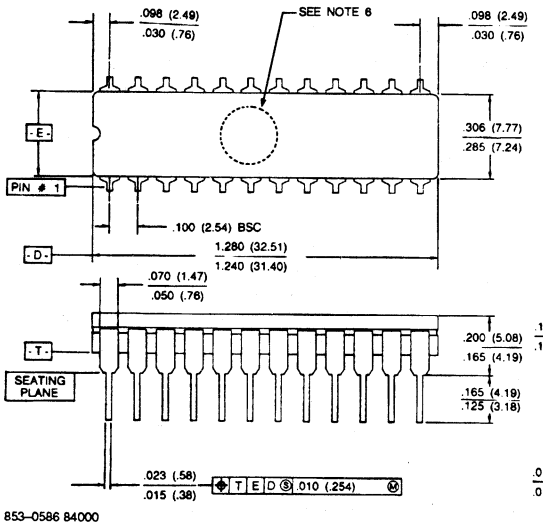


NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M - 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from the top.
6. Denotes window location for EPROM products.

853-0584 88099 FL1

Package outlines

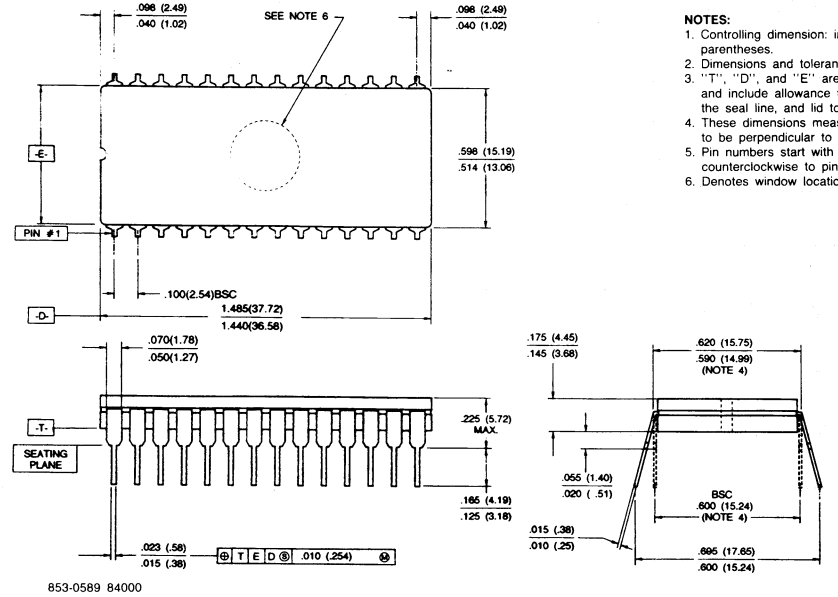
24-PIN (300 mils wide) CERAMIC DUAL IN-LINE (F) PACKAGE
24-PIN (300 mils wide) CERAMIC DUAL IN-LINE WITH QUARTZ WINDOW (FA) PACKAGE



853-0586 84000

NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M - 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from the top.
6. Denotes window location for EPROM products.

28-PIN (600 mils wide) CERAMIC DUAL IN-LINE (F) PACKAGE
28-PIN (600 mils wide) CERAMIC DUAL IN-LINE WITH QUARTZ WINDOW (FA) PACKAGE



853-0589 84000

NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M - 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #28 when viewed from the top.
6. Denotes window location for EPROM products.

Package outlines

CERQUAD J-BEND WITH QUARTZ WINDOW

NO. OF LEADS	PACKAGE CODE	DESCRIPTION	TYPICAL θ_{JA}/θ_{JC} VALUES (°C/W)	
			Average θ_{JA}	Average θ_{JC}
68	KA	930mil-wide	44.5[1]	TBD
84	KA	1130mil-wide	TBD	TBD

NOTE:
1. For die size of 55K mils^2, 1W power dissipation, soldered.

68-PIN CERQUAD J-BEND WITH QUARTZ WINDOW (KA) PACKAGE

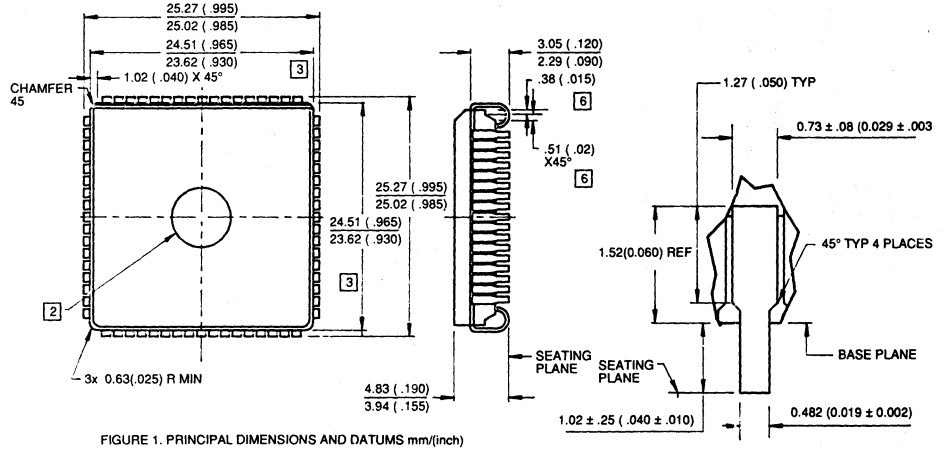


FIGURE 1. PRINCIPAL DIMENSIONS AND DATUMS mm/(inch)

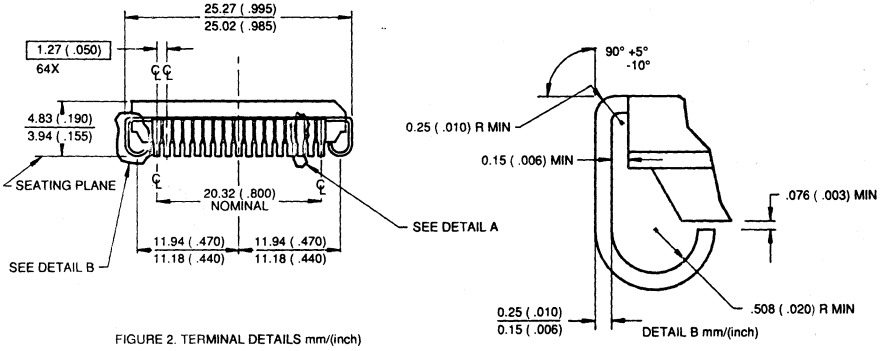


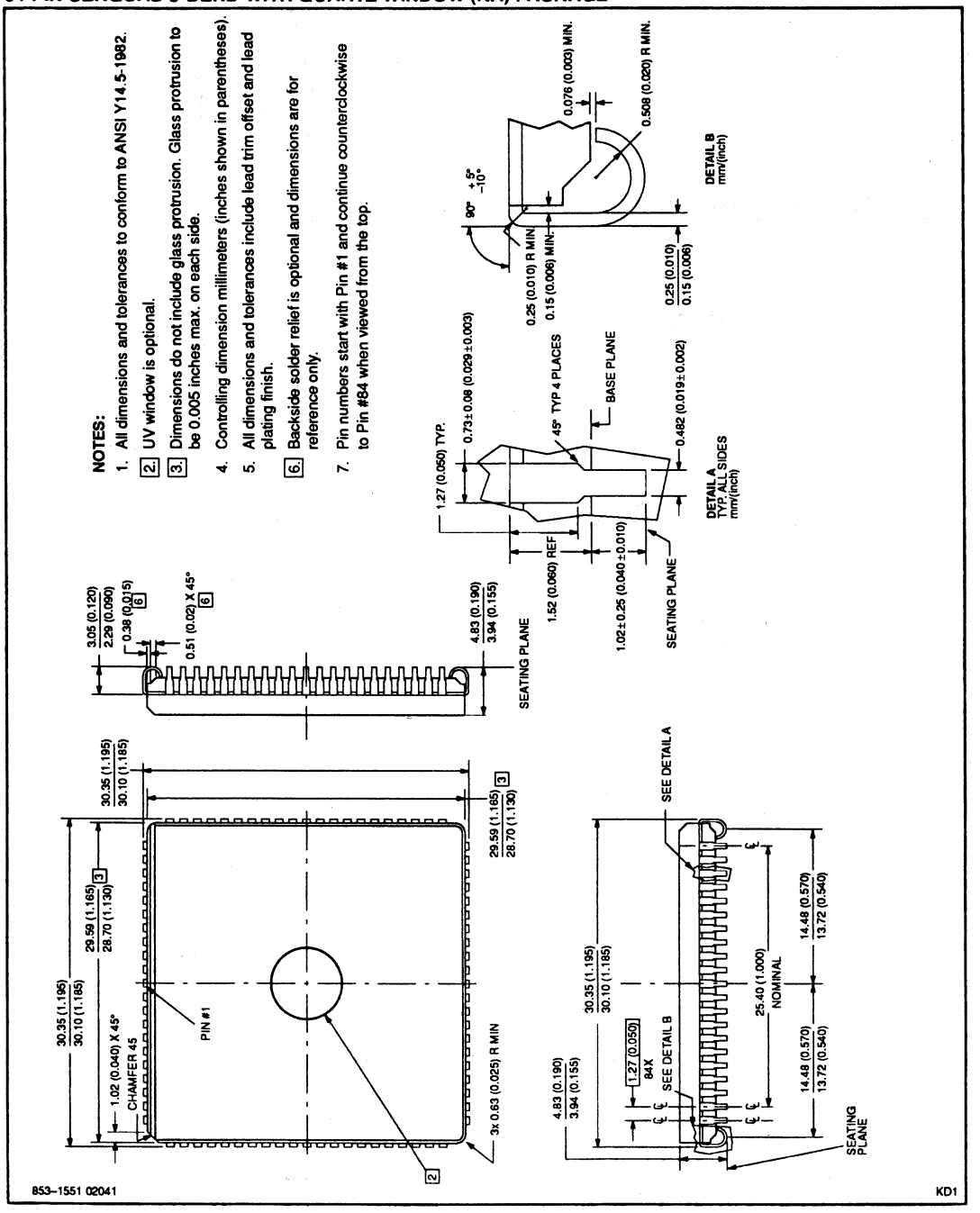
FIGURE 2. TERMINAL DETAILS mm/(inch)

1. ALL DIMENSIONS AND TOLERANCES TO CONFORM TO ANSI Y14.5-1982.
2. UV WINDOW IS OPTIONAL.
3. DIMENSIONS DO NOT INCLUDE GLASS PROTRUSION. GLASS PROTRUSION TO BE 0.005 INCHES MAX ON EACH SIDE.
4. CONTROLLING DIMENSION MILLIMETERS.
5. ALL DIMENSIONS AND TOLERANCES INCLUDE LEAD TRIM OFFSET AND LEAD PLATING FINISH.
6. BACKSIDE SOLDER RELIEF IS OPTIONAL AND DIMENSIONS ARE FOR REFERENCE ONLY.

853-1473 00441 KC1

Package outlines

84-PIN CERQUAD J-BEND WITH QUARTZ WINDOW (KA) PACKAGE



Package outlines

PLASTIC DIP

1. Package dimensions conform to JEDEC specification MS–001–AA for standard Plastic Dual Inline (DIP) package.
2. Controlling dimensions are given in inches with dimensions in millimeters, mm, contained in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M – 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.01 inch (0.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise when viewed from the top.
7. Lead material: Olin 194 (Copper Alloy) or equivalent, solder dipped.
8. Body material: Plastic (Epoxy).
9. Thermal resistance values are determined by Temperature Sensitive Parameter (TSP) method. This method uses the forward voltage drop of a calibrated diode to measure the change in junction temperature due to a known power application. Test conditions for these values are:

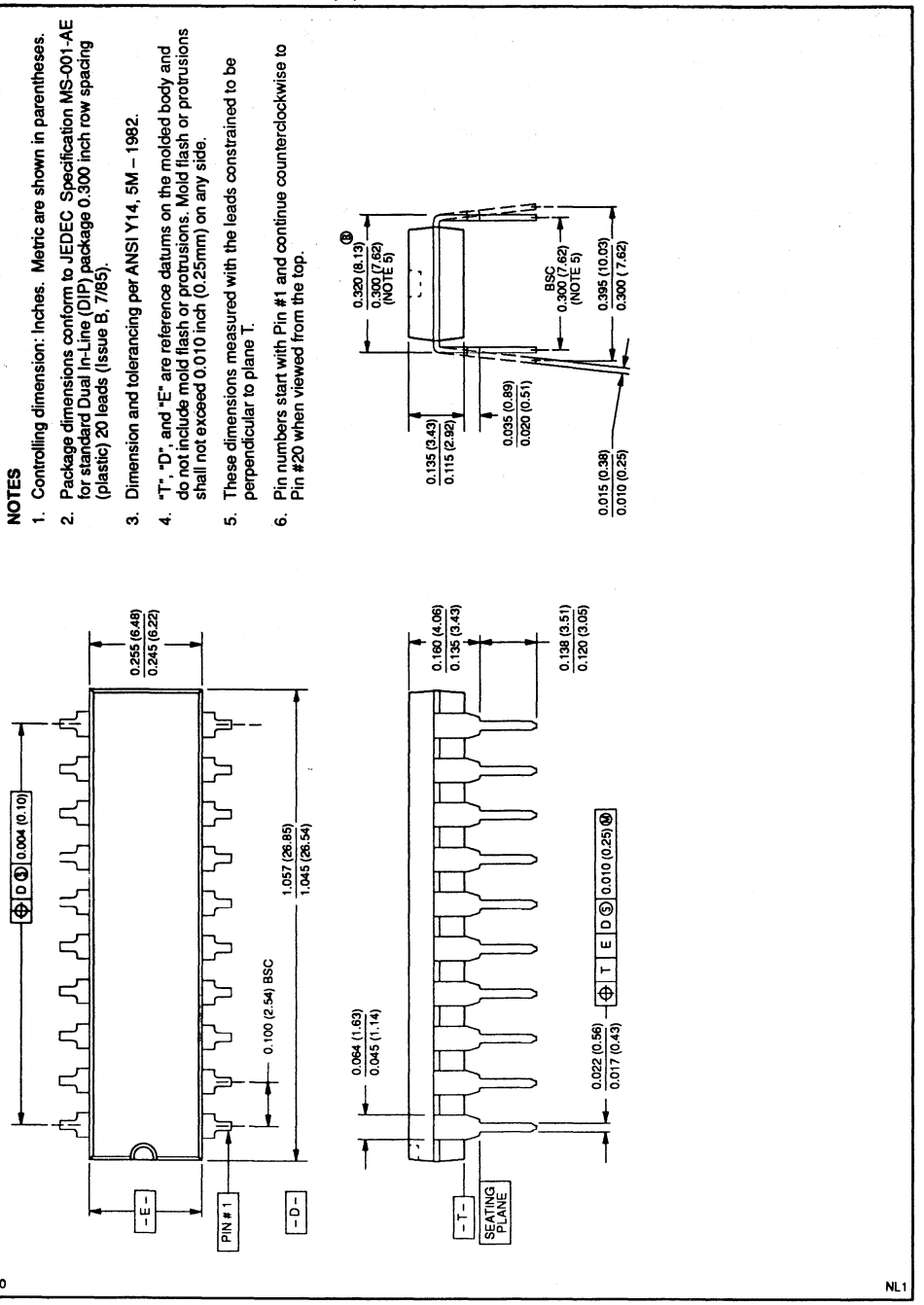
   Test Ambient—Still Air
   Test Fixture— θ_{JA}– Textool ZIF socket with 0.04" stand-off
   θ_{JC}– Water cooled heat sink

PLASTIC DUAL IN-LINE PACKAGES

NO. OF LEADS	PACKAGE CODE	DESCRIPTION	TYPICAL θ_{JA}/θ_{JC} VALUES (°C/W)	
			Average θ_{JA}	Average θ_{JC}
20	N	Cu. Lead Frame 300mil-wide	63	27
24	N	Cu. Lead Frame 300mil-wide	56	26
28	N	Cu. Lead Frame 600mil-wide	46	18
28	N3	Cu. Lead Frame 300mil-wide	53	24

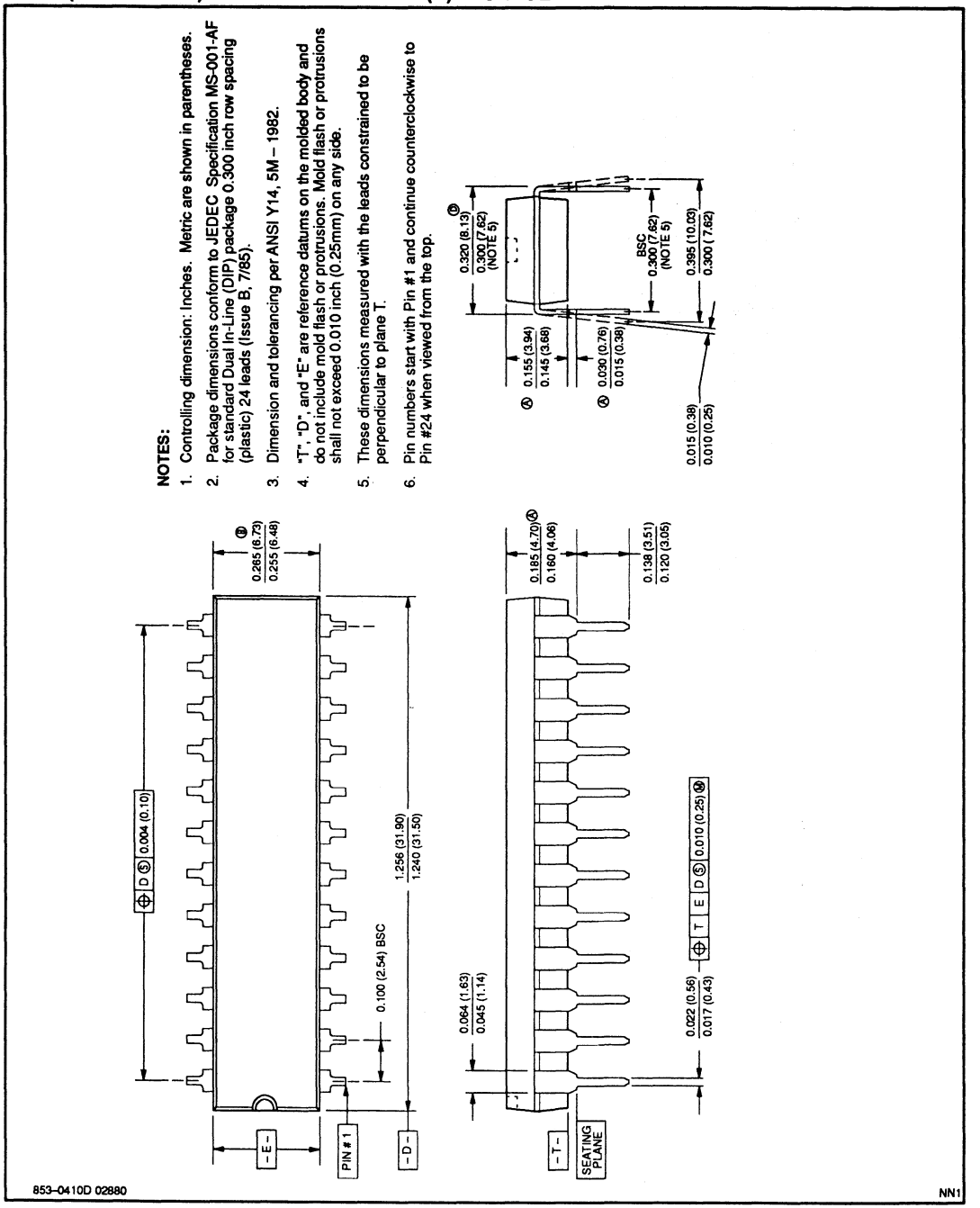
Package outlines

20-PIN (300 mils wide) PLASTIC DUAL IN-LINE (N) PACKAGE



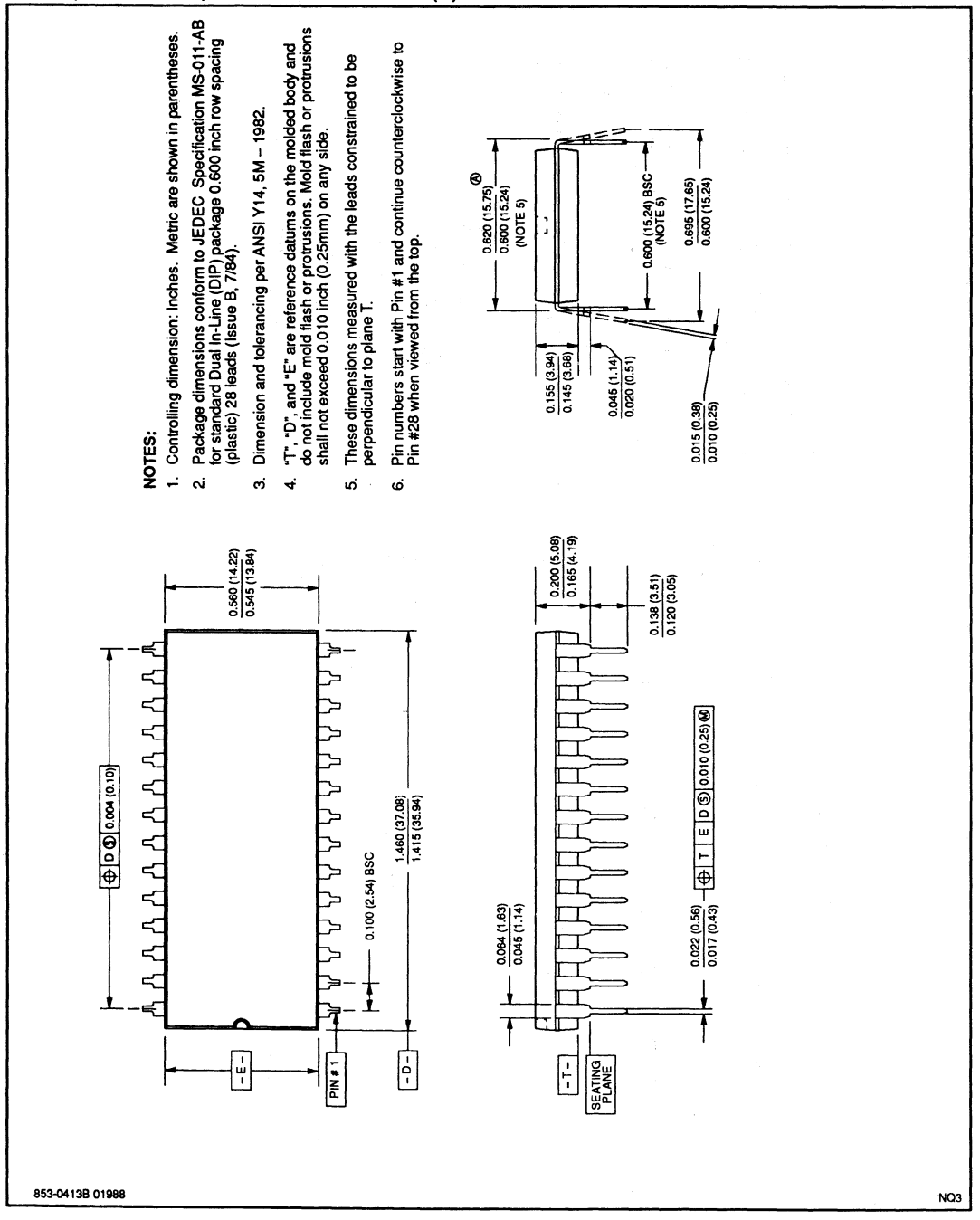
Package outlines

24-PIN (300 mils wide) PLASTIC DUAL IN-LINE (N) PACKAGE



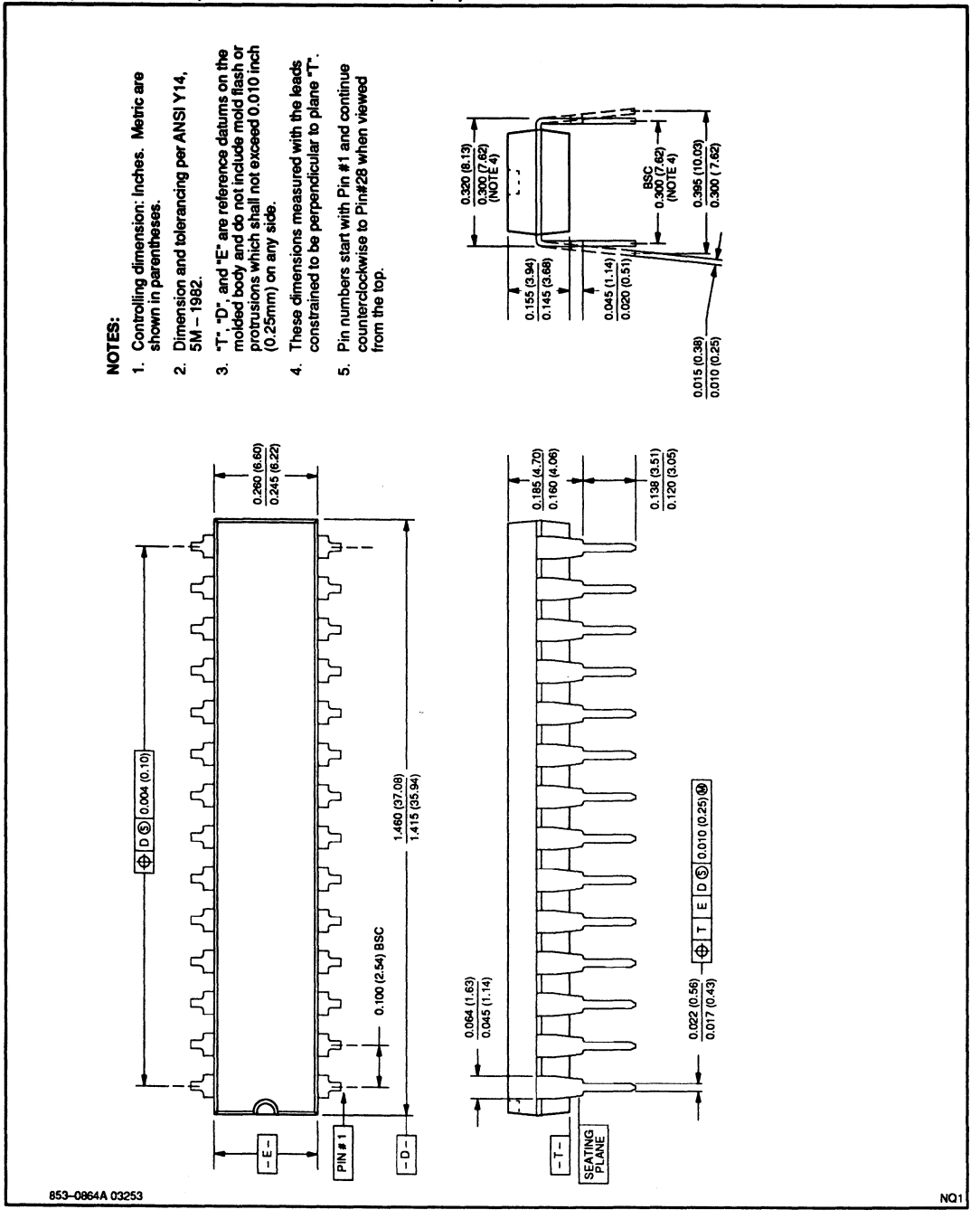
Package outlines

28-PIN (600 mils wide) PLASTIC DUAL IN-LINE (N) PACKAGE



Package outlines

28-PIN (300 mils wide) PLASTIC DUAL IN-LINE (N3) PACKAGE



Section 11
Sales Offices, Representatives & Distributors

Sales Offices, Representatives and Distributors

SIGNETICS HEADQUARTERS
811 East Arques Avenue
P.O. Box 3409
Sunnyvale, CA 94088-3409

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(714) 752-2780

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Richardson
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SIGNETICS CANADA, LTD.
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Phone: (416) 626-6676

Nepean, Ontario
Phone: (613) 225-5467

REPRESENTATIVES

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Tech-Trek, Ltd.
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Phone: (604) 276-8735

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Mectron Group
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Anthem Electronics
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Falcon Electronics, Inc.
Gerber Electronics
Hamilton/Avnet Electronics
Marshall Industries
Wyle/EMG
Zentronics, Ltd.

03/05/92

Data handbook system — Appendix A

INTRODUCTION

Our data handbook system comprises more than 65 books with subjects including electronic components, subassemblies and magnetic products. The handbooks are classified into seven series:

INTEGRATED CIRCUITS;
DISCRETE SEMICONDUCTORS;
DISPLAY COMPONENTS;
PASSIVE COMPONENTS;
PROFESSIONAL COMPONENTS;
MAGNETIC PRODUCTS;
LIQUID CRYSTAL DISPLAYS.

Data handbooks contain all pertinent data available at the time of publication and each is revised and reissued regularly.

Loose data sheets are sent to subscribers to keep them up-to-date on additions or alterations made during the lifetime of a data handbook.

Catalogs are available for selected product ranges (some catalogs are also on floppy discs).

For more information about data handbooks, catalogs and subscriptions, contact one of the organizations listed on the back cover of this handbook. Product specialists are at your service and inquiries are answered promptly.

INTEGRATED CIRCUITS

IC01	Radio, Audio and Associated Systems Bipolar, MOS
IC02a/b	Video and Associated Systems Bipolar, MOS
IC03	ICs for Telecom Subscriber Sets, Cordless, Mobile and Cellular Telephones, Radio Pagers
IC04	HE4000B Logic Family CMOS
IC05	Advanced Low-power Schottky (ALS) Logic Series
IC06	High-speed CMOS; 74HC/HCT/HCU Logic Family
IC07	Advanced CMOS Logic (ACL)
IC08	10/100k ECL Logic/Memory/PLD
IC09	TTL Logic Series

INTEGRATED CIRCUITS (continued)

IC10	Memories MOS, TTL, ECL
IC11	Linear Products
IC12	I^2C-bus-compatible ICs
IC13	Programmable Logic Devices
IC14	8048-Based 8-Bit Microcontrollers
IC15	FAST TTL Logic Series
IC15 supplement: Additional FAST Data	
IC16	CMOS Integrated Circuits for Clocks and Watches
IC17	ICs for Telecom ISDN
IC18	Microprocessors and Peripherals
IC19	Data Communication Products
IC20	80C51-Based 8-Bit Microcontrollers
IC23	Advanced BiCMOS Interface Logic

DISCRETE SEMICONDUCTORS

SC01	Diodes
SC02	Power Diodes
SC03	Thyristors and Triacs
SC04	Small Signal Transistors
SC05	Low-frequency Power Transistors and Hybrid IC Power Modules
SC06	High-voltage and Switching Power Transistors
SC07	Small-signal Field-effect Transistors
SC08a	RF Power Bipolar Transistors
SC08b	RF Power MOS Transistors
SC09	RF Power Modules
SC10	Surface Mounted Semiconductors
SC12	Optocouplers
SC13	Power MOS Transistors
SC14	Wideband Transistors and Wideband Hybrid IC Modules
SC15	Microwave Transistors
SC17	Semiconductor Sensors

Data handbook system — Appendix A

DISPLAY COMPONENTS

DC01	Colour Display Components Colour TV Picture Tubes and Assemblies Color Monitor Tube Assemblies
DC02	Monochrome Monitor Tubes and Deflection Units
DC03	Television Tuners, Coaxial Aerial Input Assemblies
DC04	Loudspeakers
DC05	Flyback Transformers, Mains Transformers and General-purpose FXC Assemblies

PASSIVE COMPONENTS

PA01	Electrolytic Capacitors; Solid and Non-solid
PA02	Varistors, Thermistors and Sensors
PA03	Potentiometers and Switches
PA04	Variable Capacitors
PA05	Film Capacitors
PA06	Ceramic Capacitors
PA07	Piezoelectric Quartz Devices
PA08	Fixed Resistors
PA11	Quartz Oscillators

PROFESSIONAL COMPONENTS

PC01	High-power Klystrons and Accessories
PC02	Cathode-ray Tubes
PC03	Geiger-Muller Tubes
PC04	Photo Multipliers
PC05	Plumbicon Camera Tubes and Accessories
PC06	Circulators and Isolators
PC07	Vidicon and Newvicon Camera Tubes and Deflection Units
PC08	Image Intensifiers
PC09	Dry-reed Switches
PC11	Solid-state Image Sensors and Peripheral Integrated Circuits
PC12	Electron Multipliers

MAGNETIC PRODUCTS

MA01	Soft Ferrites
MA02	Permanent Magnet Materials
MA03	Piezoelectric Ceramics

LIQUID CRYSTAL DISPLAYS

LCD01	Liquid Crystal Displays and Driver ICs for LCDs

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