Panasonic

Bipolar Digital IC
LS-TTL
DN 74 LS

The circuit examples appearing in this manual have been used to describe the characteristics and properties of these products.
The contents of the manual are complete as far as necessary to assure accuracy and reliability, and Panasonic assumes no responsibility with respect to problems resulting from the use of the circuits described herein or patents by third persons.
Specifications may also be changed without notice in order to make improvements.

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Numerical Index

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Descriptions

1. Outline of DN74LS TTL

The bipolar logic IC TTL (transistor-transistor logic) which appeared on the market in the early 1960s is widely utilized in computer and other applications ranging from industrial to consumer products. As MOS LSI became high speed, this required that peripheral circuits also be high speed and consume little power.

The low-power Schottky TTL, LS TTL for short, which utilizes a transistor for saturation control by means of a Schottky barrier-diode clamp, became very popular.

TTL in which high resistance has been attained through the introduction of the Schottky barrier and ion implantation and which realizes high speed and low power consumption. The series includes more than 100 items.

Fig. 1 is a cross-sectional view of the SBD clamp transistor.

This manual utilizes the MIL (U. S. military specifications) logic symbols which are shown in Fig. 2.

- **Features of the DN74LS TTL**

(1) Utilizes the Schottky barrier diode (SBD)
(2) High-resistance by ion implantation
(3) High-speed operation: 9ns per gate
(4) Low power consumption: 2mW per gate
(5) Wide operational temperature range: $-20 \sim +75°C$
(6) All products employ the highly reliable DIL plastic package and Panaflat package.
(7) Fully compatible with SN74LS TTL
(8) Schottky diode input clamp

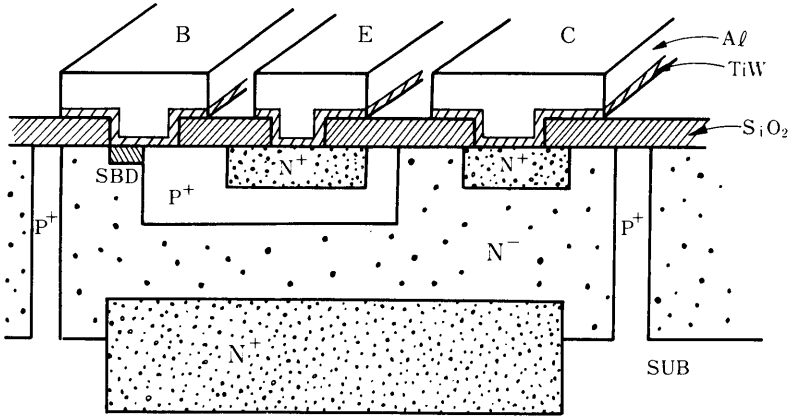


Fig. 1 Cross-sectional view of SBD clamp transistor

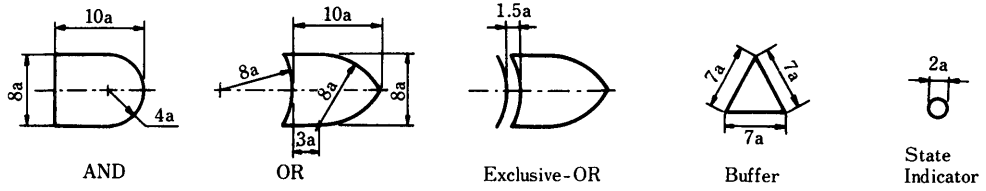


Fig. 2 Logic symbols

3. Symbols and Terms

In individual specifications various symbols, the voltage, current, time, etc., which cannot be written into a full name, are noted by abbreviations. Even in specifications charts, omitted data are often generally referred to by symbols, and so here we have provided explanations of these terms and the meanings of the symbols together with short descriptions.

DC Characteristics

	Symbol	Term.	Description.
Voltages	V_{IH}	Input HIGH voltage	Voltage applied to an input terminal as High level. Minimum level is specified and is sometimes noted as V_{IH}(min). Maximum level is specified by input voltages for absolute maximum ratings.
	V_{IL}	Input LOW voltage	Voltage applied to an input terminal as Low level. Maximum level is specified and is sometimes noted as V_{IL}(max).
	V_{OH}	Output HIGH voltage	Output voltage when the output current I_{OH} specified for an output terminal (e.g. the maximum current at the assumed maximum fan-out) flows out under input conditions to make the output HIGH.
	V_{OL}	Output LOW voltage	Output voltage when the output current I_{OL} specified for an output terminal (e.g. the maximum outflow current at the assumed maximum fan-out) flows in under input conditions to make the output LOW.
	V_{IK}	Input clamp voltage	Input voltage when the specified current flows from an input terminal (specified for an input of the device which has a clamping diode at its input terminal).
	V_T^+	Input positive-going threshold voltage	Input voltage when the operation of a logic element varies when the input is raised from a voltage level lower than the input negative-going threshold voltage V_T^-.
	V_T^-	Input negative-going threshold voltage	Input voltage when the operation of a logic element varies when the input is lowered from a voltage level higher than the input positive-going threshold voltage V_T^+.
	$V_{O(on)}$	Output ON voltage	Output terminal voltage with respect to an output current specified under input conditions such to make output ON. ng (This characteristic is specified with respect to an output without an internal pull-up element and a 3-state output.)
	$V_{O(off)}$	Output OFF voltage	Output terminal voltage with respect to an output current specified under input conditions to make the output OFF. ng (This characteristic is specified with respect to an output without an internal pull-up element and a 3-state output.
Currents	I_{IH}	Input HIGH current	Input current flowing in when the voltage of a high level specified for an input is applied.
	I_{IL}	Input LOW current	Input current flowing in when the voltage of a LOW level specified for an input is applied.
	I_{OH}	Output HIGH current	Current flowing out when an input is fixed so that the output becomes HIGH under specified conditions.
	I_{OL}	Output LOW current	Current flowing in when an input is fixed so that the output becomes LOW under specified conditions.

3. Symbols and Terms

	Symbol	Term.	Description.
	I_{OS}	Output short-circuit current	The current is specified when an output terminal is shorted with ground under a HIGH output condition. I_{OS} is used to determine switching capabilities during capacitive load. When measuring, avoid shorting more than one output at a time and stay within one second.
	I_I	Input current	Input current flowing in when the maximum input voltage specified for an input terminal is applied.
	I_{CCH}	Output HIGH supply current	Current flowing into a power supply terminal (V_{CC}) when all of the outputs are HIGH.
	I_{CCL}	Output LOW supply current	Current flowing into a power supply terminal (V_{CC}) when all of the outputs are LOW.
	I_{CC}	Supply current	When I_{CC} is specified by I_{CCH} and I_{CCL}, it is specified by their average values. When I_{CC} is not specified by I_{CCH} and I_{CCL}, it is specified by the input condition when the current flowing into the power supply terminal becomes maximum.
	$I_{O(off)}$	Output OFF current	Output current flowing in when an output voltage specified under such input conditions as the output becoming off is applied (specified with respect to open collector outputs that drive elements other than logic circuits).
	I_{OZ}	Output OFF current (High impedance)	Current which flows in an output of an element with 3-state output when the input condition is set to make its output high impedance.
	I_T^+	Input positive-going threshold current	Current flowing out when a threshold voltage VT^+ is applied to an input terminal.
	I_T^-	Input negative-going threshold current	Current flowing out when a threshold voltage VT^- is applied to an input terminal.

AC characteristics

Symbol	Term	Description
t_{pd}	Propagation delay time	Time it takes variations in an input to appear in the output.
f_{max}	Maximum clock frequency	Maximum repeating clock frequency that can maintain variations in a stable output logic in the specified sequence when the input/output conditions are fixed so that variations in the output will occur through the clock pulse.
t_r	Rise time	Specifies the maximum time required for the amplitude of an input clock pulse to go from 10% to 90% when the pulse changes from LOW to HIGH. When an output pulse is specified, it is referred to as t_{TLH}.
t_f	Fall time	Specifies the maximum time required for the amplitude of an input clock pulse to go from 90% to 10% when the pulse changes from HIGH to LOW. When an output pulse is specified, it is referred to as t_{THL}.
t_{PLH}	Output rise propagation delay time	Delay time between the specified voltage levels of input and output voltage waveforms under fixed load conditions when the output changes from LOW to HIGH.
t_{PHL}	Output fall propagation delay time	Delay time between the specified voltage levels of input and output voltage waveforms under fixed load conditions when the output changes from HIGH to LOW.

Symbol	Term	Description
t_{HZ}	3-state output disable time (HIGH)	Delay time between the specified voltage levels of input and output voltage waveforms under fixed load conditions when the 3-stage output changes from HIGH to high impedance.
t_{LZ}	3-state output disable time (LOW)	Delay time between the specified voltage levels of input and output voltage waveforms under fixed load conditions when the 3-stage output changes from LOW to high impedance.
t_{ZH}	3-state output enable time (HIGH)	Delay time between the specified voltage levels of input and output voltage waveforms under fixed loads conditions when the 3-stage output changes from high impedance to HIGH.
t_{ZL}	3-state output enable time (LOW)	Delay time between the specified voltage levels of input and output voltage waveforms under fixed loads conditions when the 3-state output changes from high impedance to LOW.
t_W	Pulse width	Specifies the minimum time interval between the rise and fall of the specified voltage of input waveforms applied to flip-flop (referred to as FF below) ICs.
t_h	Hold time	Time the data at the specified input terminal must be retained after changes at other related input terminals (e.g. clock input) occur.
t_{su}	Setup time	Time the data at the specified input terminal must be applied and stabilized before changes at other retated input terminals (e.g. clock input) occur.
t_{rec}	Recovery time	Related to FF ICs and is the time between the specified voltages of the effective edges for cancellation of the reset input and operation of an input clock pulse.
$t_{release}$	Release time	Time from when the data at the specified input terminal is cancelled until other related input terminals (e.g. clock input) can be caused to change.

Function chart

Symbol	Description
H	High level (steady state) (Referred to as HIGH in the text.)
L	LOW level (steady state) (Referred to as LOW in the text.)
↑	Transistion from low level to high level
↓	Transistion from high level to low level
X	Neither HIGH nor LOW
Z	OFF state of 3-state output (high impedance)
a ... h	Steady-state input levels at each input between A and H
Q_o	Q level immediately before establishment of the indicated input conditions
$\overline{Q_o}$	Complement of Q_O
Q_n	Q level immediately before the most recent active change (↓ or ↑) occurs
⎍	One high-level pulse
⎍	One low-level pulse
Toggle	Each output is changed to the complement of the previous state by an active change (↓ or ↑) of the input.
F_o	Fan-out; indicates how many IC inputs of the same kind can be connected to the output.

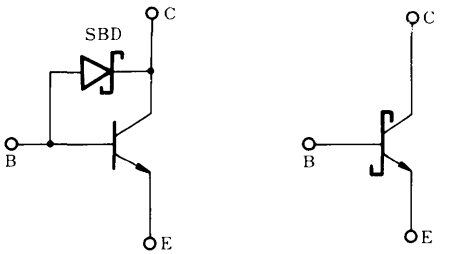
4. Basic Circuitry

In a standard TTL series when the transistor is on, it is completely saturated and then utilized. In this state, a minority carrier accumulates in the base region, and the time it takes the transistor to switch from ON to OFF is limited by the time it takes the minority carrier to dissipate.

In the DN74LS series a small forward-voltage Schottky barrier diode (SBD) is attached between the base and collector of transistors which are saturated. When a transistor is ON, the excess base current is passed through this SBD and drained off to the collector, thereby preventing accumulation of minority carriers in the base region and improving speed.

However, because this SBD clamp causes the saturation voltage of the transistor to increase, the V_{OL} when the load current is maximum increases by about 0.1V.

The SBD is inserted as shown in Fig. 3 (a) but is represented by the symbol in Fig. 3 (b).



(a) SBD clamp transistor

(b) Symbol for SBD clamp transistor

Fig. 3 Schottky diode clamp transistor

The basic circuitry for the NAND gate is shown in Fig. 4. For example, when A input is LOW (GND), current flows from V_{CC} through R_1 and Q_1, and a LOW input current I_{IL} flows and Q_1 becomes a diode ($\cong$ 0.7V). As a result Q_3, Q_4, Q_5, Q_8, and Q_9 are OFF, the current passes from V_{CC} through R_2 to Darlington transistors Q_6 and Q_7, and the output is HIGH.

On the other hand, when inputs A and B are both HIGH (e.g. V_{CC}), Q_1 and Q_2 are OFF and the base current flows from V_{CC} through R_1 to Q_4. Thus, Q_4, Q_5 and Q_8 are ON and the output is LOW.

Q_9 stops the output voltage from changing to the threshold voltage when the input changes from LOW to HIGH.

Q_3, D_3 and D_5 work to increase the switching speed. As can be seen, by this operation transistors Q_1, Q_2, Q_3, and Q_7, which are not saturated, are not clamped by the SBD, but the other transistors are clamped thus increasing the speed.

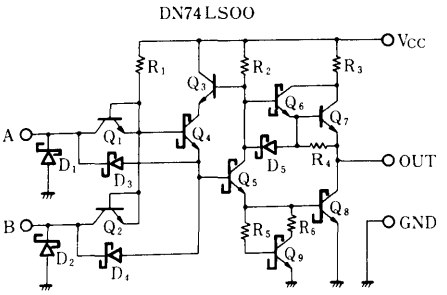


Fig. 4 Basic circuitry for the NAND gate

5. DN74LS TTL Panaflat Package

DN74LS TTL uses both the standard DIL plastic package and the compact panaflat package and distinguishes between the two as follows:

(1) Standard DIL package products: DN74LS00

(2) Panaflat package products: DN74LS00S

"S" indicates Panaflat package.

Panasonic Panaflat package is a new ultra-compact package for ICs and LSI developed for devices requiring hybrid ICs or that have to be ultra-compact or ultra-thin. Recently, the advancement of electronics in all fields and the miniaturization and reduction in weight of electronic devices for both consumer and industrial use has drawn attention to the miniaturization of electronic parts beginning with transistors and ICs due to the demands of high-density mounting. Panaflat package ICs are a family of ultra-compact ICs which satisfy those demands because they are ideal for mounting on a circuit board as a single unit or assembly into hybrid ICs. Fig. 5 is an external view of some Panaflat packages. Recent tendencies have been to assemble monolithic IC chips into hybrid ICs; however the assembly of plain chips cannot be said to be very good when various factors such as handling, mass production, their electrical performance, and guarantee of quality are considered.

Panaflat package ICs compensate for these drawbacks.

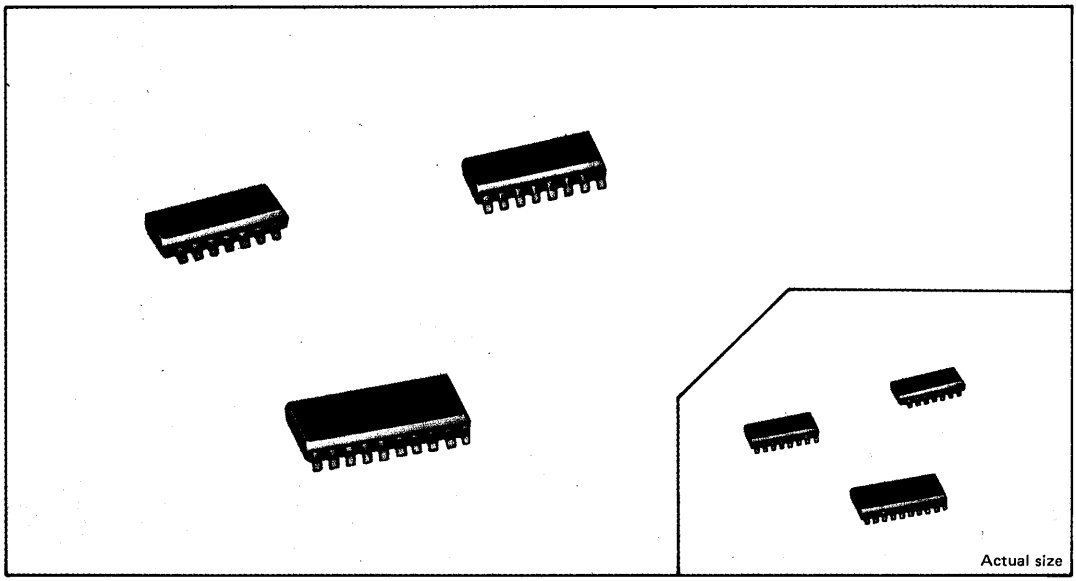


Fig. 5 External view of Panaflat packages

5.1 Features of Panaflat package ICs

Panaflat package ICs have the following advantages when compared with conventional IC chips used in hybrid ICs and beam leads.

- High mounting density making possible the extensive miniaturization and increased density of hybrid ICs and circuit boards
- Easier to handle than IC chips and soldering is possible by reflow
- Sufficient electrical characteristics can be guaranteed
- Encased in a special magazine for automatic parts placement

5.2 Production of Panaflat package ICs

Production of Panaflat ICs is based on the production technology of conventional plastic molded ICs and the mini-type molded transistors and incorporates a completely automatic sealing system developed by Panasonic and an automated production line which makes use of precise processing technologies.

5.3 Electrical characteristics

The absolute maximum ratings and electrical characteristics of Panaflat package ICs is basically the same as that of conventional plastic DIL package products.

By mounting a Panaflat IC on the circuit board of a hybrid IC and then coating it further with resin, the thermal resistance is improved over that of a single unit because of the dissipation of heat from the single unit because of the discharge of heat from the leads and resin surface.

Table 1 shows a comparison of the thermal resistance of different types of mountings.

For example, by mounting on a ceramic circuit board and coating with resin, an allowance equivalent to or better than that of conventional 18-pin plastic DIL packages (DIL-18) may be achieved.

Please make sufficient assessment of the actual mounting conditions concerning heat dissipation during actual use.

Table 1 Comparison of the thermal resistance for the mounting of panaflat packages (SO-18D)
Values represent the improvement in thermal resistance using the thermal resistance of a single IC placed at 1 as a reference.

	Epoxy circuit board (55 x 10 x 0.7mm)	General use ceramic circuit board (37 x 12 x 0.6mm)
Mounted on the circuit board	0.68 (1.45)	0.57 (1.75)
Coated with resin after mounting on the circuit board	0.52 (1.81)	0.40 (2.47)

(Values in parenthesis indicate ratio of allowable loss P_D.)

5.4 Reliability

With respect to the reliability of Panaflat package ICs, testing is performed periodically according to the evaluation method in Table 2, as is done with conventional plastic packages. The level of reliability is the same as that of conventional plastic package products.

5.5 Mounting precautions

Compared with conventional packages, the structure of the Panaflat package is much smaller and thinner, and so particular attention should be given to the mounting procedures as these products are susceptible to the thermal and mechanical stresses applied during mounting. Pay particular attention to the following points.

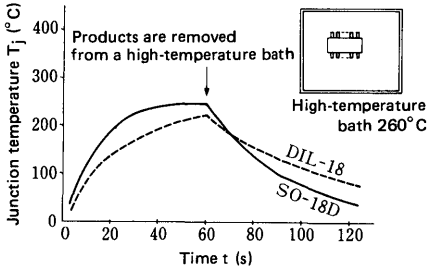
(1) Soldering

Because of their small size, SO ICs are susceptible to the influence of heat applied from outside and respond rapidly as shown in Fig. 6. For this reason, the influence of thermal stress should be minimized. Thermal stress causes expansion and contraction of the resin which causes stress inside the package. Therefore, when exposing to high temperatures of soldering, keep the operation as short as possible.

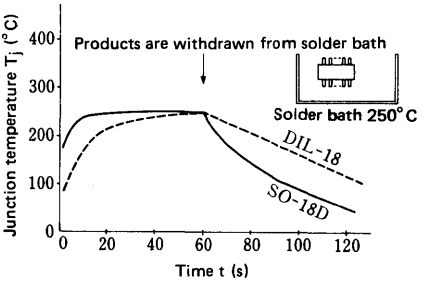
Requirements for soldering

(1) Use a reflow method such as that in Fig. 7 to keep the temperature as low, below 260°C, as possible and the time as short, less than 10 seconds, as possible.
Please use a soldering paste conforming to these requirements.

(2) For fluxing after soldering, momentarily wash with Tri-Ethane or a similar solution.



(b) High-temperature bath



(a) Solder bath 250°C

Fig. 6 Comparison of junction temperatures according to the external conditions of the Panaflat package (SO-18D) and the conventional package (DIL-18)

Table 2 Reliability test

Test	Condition
External dimensions	According to individual package
Vibration test	100 ~ 2000Hz 20G, 4min/1 time (X, Y, Z each 4 times)
Drop test	Maple board, 1m, 3 times
Terminal pull	0.5kg in direction of lead axis for 10sec
Terminal bending	0.25kg to 45° back and forth 2 times
Saltwater spray	35°C at 5% for 24 hours
Temperature cycle (gaseous phase)	Tstg. max ↔ Tstg. min, 10 cycles (30min) (30min)
Thermal shock (liquid phase)	100°C ↔ 0°C, 10 cycles (5min) (5min)
Boiling test	Pure water at 100°C for 100hrs
Pressure cooker	Steam saturation at 2atm for 60hrs
Solderability	230°C, 1 time for 5sec with flux
Solder-heat resistance	260°C, 5sec
High-temperature storage	Ta = Tstg. max 1000hrs
Low-temperature storage	Ta = Tstg. min 1000hrs
High-temperature, high-humidity storage	Ta = 85°C, RH = 85% for 500hrs
Operating life	Ta = Topr max 1000hrs, maximum loss and T_j(max)
High-temperature, high-humidity bias	Ta = 85°C and RH = 85% for 500 hrs, steady bias

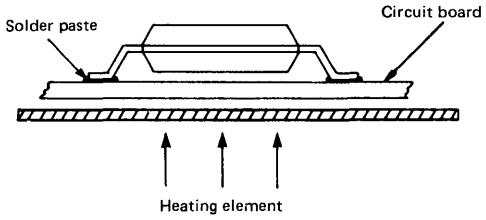


Fig. 7 Diagram showing reflow-system soldering

(2) Mechanical stress

- Because of the small, thin structure of the SO IC, the strength of the lead wires, in comparison with conventional plastic packages, is as shown in Fig. 8. Thus, particular attention must be paid to their handling.
- Furthermore, because of their thin shape, they are susceptible to stress applied during mounting or through the resin surface after mounting, and this may change their characteristics. Be careful that no stress is applied to the resin surface.

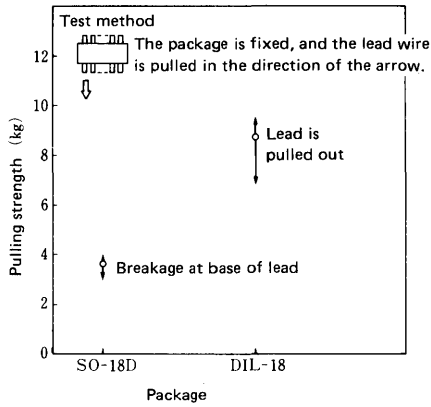


Fig. 8 Results of lead terminal pulling test

(3) Heat discharge after mounting

The heat discharge of SO ICs is greatly influenced by mounting to the circuit board and coating with resin, and so please determine the heat discharge with the IC in its mounted condition. The following is a simple estimation method for the chip temperature in the mounted condition.

Estimation of the chip temperature by measuring the package surface temperature

By putting the Panaflat package IC in an operating condition, the chip temperature (T_j) rises. After sufficient time (approx. 10min) the package surface temperature (T_s) becomes saturated and the T_s is measured and used to estimate T_j.

$T_s < T_j(max) - (Rthj\text{-}c \times Ptot) - (Topr - Ta)$

T_s: Package surface temperature
Ta: Measured ambient temperature
T_j(max): Storage temperature noted in the product's ratings
Topr: Operating temperature noted in the product's ratings
Rthj-c: Thermal resistance between the chip and package = 40°C/W
Ptot: Power consumption of IC during operation (under most unfavorable conditions)

When the estimated value of T_s is smaller than the calculated value on the right, even at Topr(max) T_j will be below Tj(max).

(4) Moisture considerations

Because SO ICs are ultra-compact and the resin thickness is very thin, the leakage path is short, and so it is necessary to pay particular attention to moisture. Generally accepted air-tight sealing or damp-proof resin coating may be used as measures to prevent moisture from entering, but when coating with a resin, particular care should be given to selecting a resin that will satisfy the requirements of reliability.

6. Reliability

There are basically two types of tests used to check new products and mass-produced products to confirm their reliability, consistent high quality, and ability to withstand use for long periods under severe environmental conditions: life tests and environmental tests.

In order to design tests with conditions which can be recreated, Panasonic bases their tests on MIL ratings and other standard ratings such as EIAJ. For the conditions of these reliability tests, refer to Table 3 "Reliability evaluation test parameters and passing standards". In addition, the failure standards used when carrying out these tests are listed in Table 4.

For the periodic reliability confirmation tests for mass-produced products, the matrices, which are classified as diffusion process (wafer) and assembly process (package), are divided into sub-groups and representative products of each sub-group are then selected to undergo tests to confirm reliability. The testing frequency varies from one to six months, depending on the type of product. The results of the reliability tests for the TTL Series are shown in Table 5. In addition, the characteristics changes which appeared in the high time acceleration factor THB tests and life tests for representative products are shown in Figs. 9 ~ 12. The results of these tests are ample proof of the consistently high reliability of Panasonic products.

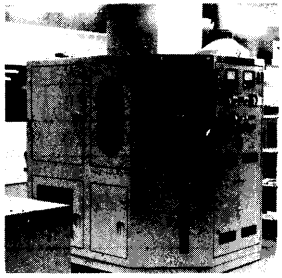
Even though these products are plastic sealed, mass production of products easily capable of being used in industrial fields has become possible through the development of high-purity resin, the introduction of a new sealing technology and the establishment of a technology for making protective films. We at Panasonic are nor going to stop at the present high level of reliability out products have achieved, and we are constantly working to attain even greater improvements. To accompany the high reliability of our products, we have made advancements in the development of a system to carry out tests to confirm reliability in as short a time as possible and quickly relate the information to the appropriate sections. This system includes the accumulation of test data, analysis of statistical and physical information on the quality of products on the market, and feedback of all this to the pertinent sections.

Table 3 Reliability evaluation test parameters and passing standards

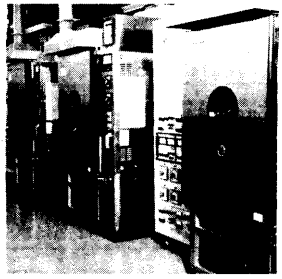
Group	Parameter	Test conditions	Judging standards LPTD (r/N)	Testing standards	
				New products test	Periodic reliability test
1	Initial characteristics	All parameters of inspection ratings specified for each product type.	5% (0/45)	○	
	Temperature characteristics	Characteristics test of product's rated operating ambient temperature range.	50% (0/5)	○	
	Voltage characteristics	Characteristics test of product's rated power supply voltage range.	50% (0/5)	○	
	Heat resistance		50% (0/5)	○	
2	Soldering	Immersed for 5±0.5 seconds in 230±5°C solder bath up to 1.5mm from the main part of the unit. Flux used is 35% pine oil solution.	15% (0/15)	○	○
	External dimensions	According to the product's rated external dimensions.	15% (0/15)	○	
3	Thermal shock	10 cycles Tmin (−65°C, 1min or more) Tmax (150°C, 1min or more) Both testing baths are liquid baths.			
	Thermal fatique	Conditions at $T_j$max or $P_D$max determined according to configuration type.	15% (0/15)	○	

Group	Test	Test conditions	Judging standards LPTD (r/N)	Testing standards	
				New product qualification	Periodic reliability test
3	Soldering thermal stability	Immersed for 10±1 seconds in 300^{+0}_{-10}°C solder bath up to 1±0.1mm from the main part of the unit.	15% (0/15)	○	
4	Drop test	Dropped 3 times from a height of 1m onto a maple board.	50% (0/5)	○	
	Lead bend	Bent 90° with an applied force of 230g and then returned.	50% (0/5)	○	
	Lead pull	2kg of force applied for 30±1 seconds in lead axial direction.	50% (0/5)	○	
5	Salt water spraying	Sprayed continuously for 24 hours at concentration of 5%, temperature 35°C.	50% (0/5)	○	○
6	High temperature and humidity	Kept for 1000 hours at Ta = 85°C, RH≧85%.	15% (0/15)	○	
	T.H.B	Kept for 1000 hours at Ta = 85°C, RH≧85%. Testing circuits normal actual use, ON/OFF = 1h/3h.	15% (0/15)	○	○
	Pressure cooker	Kept for 60 hours at 2 atmospheres of pressure and then allowed to cool naturally for 16 hours.	15% (0/15)	○	○
	Boiling	Kept at boiling for 50 hours.	15% (0/15)	○	
	Hermeticity	He leakage $< 1 \times 10^{-7}$ cc/s Corresponds to ceramic or metal packages.	15% (0/15)	○	
7	Low temperature	Kept at Ta = −55°C for 1000 hours.	15% (0/15)	○	
	High temperature	Kept at Ta = 150°C for 1000 hours.	15% (0/15)	○	
8	Operating life	1000 hours at Vcc (max) or Tj (max) conditions at maximum ambient temperature; ON/OFF = 2.5h/0.5h.	15% (0/15)	○	○
9	Fireproofing	Because plastic material used passes UL94 and V-0, test on completed products omitted.	50% (0/5)	○	

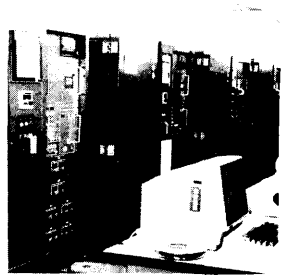
Note: The testing conditions listed above are official values; the actual tests are carried out under even stricter conditions according to our own internal standards.



Thermal shock test



THB test



Operating life test

Table 4 Reliability test failing standards

	Parameter	Failing standards		Remarks
		Lower limit	Upper limit	
Electrical characteristics	Output voltage V_{OH}, V_{OL} (V)	L x 0.9	U x 1.1	
	Output current I_{OH}, I_{OL} (A)		U x 1.1	
	Input voltage V_{IH}, V_{IL} (V)	L x 0.9	U x 1.1	
	Input current I_{IH}, I_{IL} (A)		U x 1.1	
	Supply current I_{CCH}, I_{CCL} (A)		U x 2	
	Leakage current I_I (A)		U x 2	
Appearance, Other	Dimensions	According to product's specified dimensions.		
	Corrosion, discoloration	None when observed with 10-power microscope.		Because these are physical inspections by observation and judgement might differ from one inspector to another, a limit sample is used for comparison.
	Solderability	Minimum 95% adhesion when observed with 10-power microscope.		
	Brand adherence	Markings do not come off.		

U : Upper value of initial rating L : Lower value of initial rating

Table 5 Results of reliability tests

Parameter	Test conditions	Test results
Solderability	230 ± 5°C, 5 ± 0.5 seconds	0/220
Thermal shock	−65°C ↔ +150°C Liquid phase : 10 cycles	0/425
Thermal fatigue	Ta = 25°C, Po max. t = 1000 hours ON/OFF = 5 min/5 min	0/80
Soldering thermal stability	300^{+5}_{0}°C, 10 ± 1 second	0/220
Lead bend	230g, bent 90° and returned	0/80
Lead pull	2kg, 30 seconds	0/80
Salt water spray	5%, 35°C, 24 hours	0/80
High temperature and humidity	Ta = 85°C, RH = 85% t = 1000 hours	0/425
T.H.B.	Ta = 85°C, RH = 85% t = 1000 hours, Vcc = 5V ON/OFF = 1 hour/3 hours	0/220
Pressure cooker	2 atmospheres, 60 hours	0/590
Boiling	50 hours	0/220
Low temperature	Ta = −55°C, 1000 hours	0/220
High temperature	Ta = 150°C, 1000 hours	0/220
Operating life	Ta = 75°C, Vcc = 5.5V t = 1000 hours ON/OFF = 2.5 hours/0.5 hour	0/240

7. Use and Handling

In order to design highly reliable equipment it is obviously necessary to select highly reliable parts; this reliability, however, is also greatly affected by the user's circuit conditions, environmental conditions, and all the other conditions of use. Therefore, in order to preserve the high level of reliability of these products we have listed below some cautions to be followed.

7.1 Static electricity

Although the structure of MOS ICs makes them susceptible to damage caused by static electricity, bipolar ICs do not require quite as much care as MOS ICs. However, excessively strong static electricity can also cause damage to bipolar ICs.

The charge is especially high on clothing made of synthetic fibers, and on dry days it can be as high as 10 to 30kV. If this voltage is discharged throught the terminals of an IC, damage could easily result. It is therefore necessary to take the following precautions when handling ICs.

(1) For storage, it is necessary to either short the terminals by using some electroconductive material or to wrap the entire IC in aluminum foil. Also, because containers made of nylon or plastic are easily charged, do not store or ship ICs in such containers.

(2) During use, be sure to ground the person handling the ICs and also any charged materials on the work table so that the static electricity in the area is safely discharged.

(3) Avoid using work clothing made of nylon or other synthetic fibers.

7.2 Mounting

(1) Unused input terminals

When assembling a system of various TTL devices there may be several terminals which will not be used. When an input circuit is in an open condition, it is HIGH logic at a level slightly above the threshold voltage. However, left in this condition it is susceptible to influence from noise, and so in order to increase the reliability of the system it is necessary to connect them in some way.

For unused input terminals of AND and NAND gates, apply a voltage above V_{IH}(min) that does not exceed the maximum rated voltage. Examples of actual methods for this treatment are shown below.

(a) Attach unused terminals to V_{CC} through an appropriate resistance. (Fig. 13)

(b) If there is an unused NAND gate or inverter, ground the input and connect the unused terminals to that output. (Fig. 14)

(c) Connect unused terminals to used terminals. In this instance, the input load coefficient does not change for a LOW level but will increase in proportion to the number connected when HIGH level, and so the HIGH output coefficient of the previous stage must have sufficient allowance.

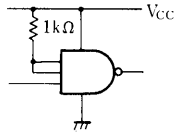


Fig. 13

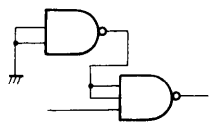
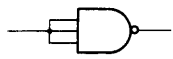


Fig. 14



Input load coefficient LOW 1
HIGH 3

Fig. 15

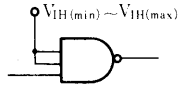


Fig. 16

(2) Output short-circuit

Shorting output terminals to GND when the output is HIGH is something that should be avoided as much as possible in consideration of such things as the heat generated by the element. However, in instances where it cannot be avoided, it is possible to short only one output to GND, as long as it is within one second.

(3) When bending leads be careful that no stress is applied to the main body of the device.

(4) When attaching to a printed circuit board, be absolutely certain the direction is correct. Particularly in the case of TTL, when the direction is reversed, the power supply (V_{CC}) and ground are reversed, and when energized the IC may be damaged.

(5) The connection for some pins is not clearly indicated in the equivalent circuit diagram, and at first observation they may appear to be empty pins, but they should not be used as relay pins. They are sometimes connected inside (not used as an external terminal), and even if they actually are empty, connecting them may result in unexpected problems such as oscillation.

(6) Soldering should be performed at as low a temperature as possible and for as short a time as possible. Panasonic test ratings for solder heat resistance are 300°C for 10 sec (DIL plastic package) and 260°C for 5 sec (Panaflat package). Therefore, be careful not to exceed these conditions during solder operations.
(7) For the soldering flux, use a neutral type with a non-conductive residue.

Common Specifications

1. Absolute Maximum Ratings

Maximum ratings are generally handled as absolute maximum ratings, so that under all conditions the rated values must not be exceeded. Doing so may cause deterioration or breakdown, and the characteristics may not return to their original values. Furthermore, any two ratings must not be reached at the same time. Table 6 shows the absolute maximum rating values for Panasonic's TTL, and each item is described below in order.

(1) Power supply voltage (V_{CC})
This is the maximum voltage that can be applied between the power supply terminal and the ground terminal.

(2) Input voltage (V_I)
This is the maximum voltage that can be applied to an input terminal.

(3) Output voltage (V_O)
This is the maximum voltage that can be applied to an output terminal.

(4) Output current (I_O)
This is the maximum current that can flow into or out of an output.

(5) Allowable loss (P_D)
This is the maximum power consumption allowable within the IC.

(6) Operating temperature (Topr)
The function of the circuitry in the IC can be guaranteed within these temperature limits. However, electrical characteristics indicated by Ta = 25°C cannot necessarily be guaranteed.

(7) Storage temperature (Tstg)
Temperature range when the IC is stored and not put into operation.

Table 6 Absolute maximum ratings

Item	Symbol	DN74LSXX series		DN74LSXXS series		Unit
Power supply voltage*	V_{CC}	7.0		7.0		V
Input voltage**	V_I	−0.5	+7.0	−0.5	+7.0	V
Output voltage**	V_O	−0.5	$+V_{CC}$	−0.5	$+V_{CC}$	V
Output current	I_O	Refer to the respective recommended operating conditions.				mA
Allowable loss	P_D	400		400		mW
Operating temperature range	Topr	−20 ~ +75		−20 ~ +75		°C
Storage temperature	Tstg	−65 ~ +150		−65 ~ +125		°C

* Defined with respect to the ground terminal as long as the voltage is not particularly designated.
** Some absolute maximum ratings will be different for some products.

Ratings for items (terminals) designated for the following products are listed in the table below.

Product*	Item	Symbol	Rating		Unit
LS196 · 197	Input voltage (all input terminals)				
LS90 · 92 · 93, LS245 LS290 · 293, LS390 · 393	Input voltage (A, B)	V_I	−0.5	+5.5	V
LS490	Input voltage (clock)		−0.5	+5.5	
LS26, LS145	Output voltage (all output terminals)	V_O	−0.5	+15	V

* Same for DN74LSXXS series

2. Recommended Operating Conditions

LS TTL devices do have maximum ratings and electrical characteristics; however, there are recommended operating conditions to satisfy those ratings.
Accordingly, if used under these conditions, the stated rated values will be guaranteed, and it will be possible to design a highly reliable circuit.
Moreover, it is possible to go outside the recommended operating conditions as long as the maximum ratings are not exceeded, but it is recommended to stay within these conditions.
Table 7 lists the recommended operating conditions for DC characteristics of the basic gate. For items such as flip-flops and 3-state buffers, whose output current conditions vary somewhat, refer to the individual specifications sheet. Also refer to this sheet when conditions concerning switching times are required.

Table 7 Recommended operating conditions

Item	Symbol	DN74LSXX series			DN74LSXXS series			Unit
		Minimum	Typical	Maximum	Minimum	Typical	Maximum	
Power supply	V_{CC}	4.75	5.00	5.25	4.75	5.00	5.25	V
Output current	I_{OH}	–	–	−400	–	–	−400	μA
Output current	I_{OL}	–	–	8	–	–	8	mA
Output voltage	V_{OH}	–	–	5.5	–	–	5.5	V
Operating temperature	Topr	−20	–	+75	−20	–	+75	°C

HIGH output current (I_{OH})
The meaning of HIGH output current differs depending on whether the output system is a totem pole (active pull-up output) or an open collector.
In a totem-pole output, the maximum current that can flow out of an output pin is the range in which the minimum value (V_{OH}(min) $\geqq$ 2.7V) of the HIGH voltage can be assured as specified. This value is related to how many subsequent load inputs can be driven by one output when the output is HIGH.
The I_{OH} in an open collector specifies the maximum current that flows into an output pin through an external resistance (pull-up resistor); however, this value influences the voltage drop at the pull-up resistor.

LOW output current (I_{OL})
The LOW output current is the specified maximum current that can flow into an output pin in the range in which the maximum value (V_{OL}(max) $\leqq$ 0.5V) of the LOW. This value is related to how many subsequent load inputs can be driven by one output when the output is LOW, and as with I_{OH} it is related to the connection method; therefore refer to fan-out under the following section.

HIGH output voltage (V_{OH})
This refers to the maximum voltage that can be applied when the output is HIGH, and it indicates the withstand voltage (V_{OH} $\leqq$ 5.5 or 15V) of output transistors in ICs with an open-collector output.

3. Fan-out

Fan-out is the number of loads that can be connected to the output of a logic circuit.
Actually, the fan-out number (F_O) is determined by using the most unfavorable conditions (electrical characteristics specifications) of the input circuit current shown in Fig. 17 as a reference.

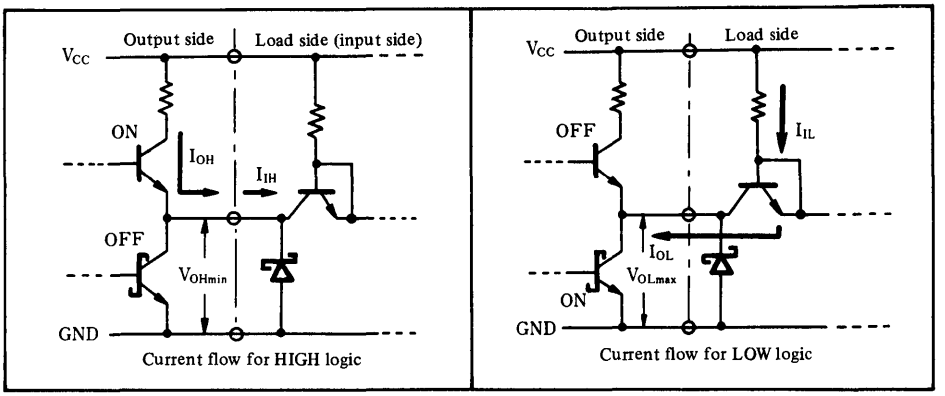


Fig. 17 Input/output circuit current flow

$$\text{Fan-out number for HIGH logic: } F_{OH} \leqq \left|\frac{I_{OH}}{I_{IH}}\right|$$

$$\text{Fan-out number for LOW logic: } F_{OL} \leqq \left|\frac{I_{OL}}{I_{IL}}\right|$$

The F_O value will change when typical, highspeed or low-power TTL is used on the load side. Furthermore, even when connecting similar types, the input conditions (I_{IH} and I_{IL} specifications) will be different depending on the type, and so care must be taken as the F_O will change.

As examples for reference, Tables 8 ~ 10 use 74LS as a reference and list representative samples of input current conditions and fan-out numbers for 74, 74S, 74H and 74L when interconnected.

Table 8 Input/output current examples using the LS type as a drive reference

Drive side conditions (LS type)		Load side input current conditions									
		74 L S		74		74 S		74 H		74 L	
I_{OH}(mA)	I_{OL}(mA)	I_{IH}(mA)	I_{IL}(mA)	I_{IH}(mA)	I_{IL}(mA)	I_{IH}(mA)	I_{IL}(mA)	I_{IH}(mA)	I_{IL}(mA)	I_{IH}(mA)	I_{IL}(mA)
0.02	(8.0)	(0.02)	0.02	(0.04)	(1.6)	(0.05)	1.6	(0.05)	(2.0)	(0.01)	0.10
0.10	24.0	0.04	0.2	0.08	3.2	0.10	(2.0)	0.10	4.0	0.02	(0.18)
0.25		0.06	(0.4)	0.12	4.8	0.15	4.0	0.15	8.0	0.03	0.36
(0.40)		0.08	0.8	0.16	6.4	0.20	6.0	0.20		0.04	0.54
1.00		0.10	1.2	0.20	8.0		8.0			0.06	0.72
2.60		0.12	1.6				10.0			0.08	0.80
15.00		0.16	2.0				14.0			0.10	3.2
		0.20	2.4							0.40	4.2
			3.2								

Table 9 Examples of fan-out numbers limited by input currents

Fan-out number for HIGH logic: $\left(\frac{I_{OH}}{I_{IH}}\right)$						Fan-out number for LOW logic: $\left(\frac{I_{OL}}{I_{IL}}\right)$					
I_{OH} (mA)	I_{IH} (mA)/F_{OH}					I_{OL} (mA)	I_{IL} (mA)/F_{OL}				
	74 LS	74	74S	74H	74L		74 LS	74	74S	74H	74L
0.4	0.02 / 20	0.04 / 10	0.05 / 8.0	0.05 / 8.0	0.01 / 40	8.0	0.02 / 400	1.6 / 5.0	1.6 / 5.0	2.0 / 4.0	0.10 / 80
	0.04 / 10	0.08 / 5.0	0.10 / 4.0	0.10 / 4.0	0.02 / 20		0.2 / 40	3.2 / 2.5	2.0 / 4.0	4.0 / 2.0	0.18 / 44.4
	0.06 / 6.7	0.12 / 3.3	0.15 / 2.7	0.15 / 2.7	0.03 / 13.3		0.4 / 20	4.8 / 1.7	4.0 / 2.0	8.0 / 1.0	0.36 / 22.2
	0.08 / 5.0	0.16 / 2.5	0.20 / 2.0	0.20 / 2.0	0.04 / 10		0.8 / 10	6.4 / 1.25	6.0 / 1.3		0.54 / 14.8
	0.10 / 4.0	0.20 / 2.0			0.06 / 6.7		1.2 / 6.7	8.0 / 1.0	8.0 / 1.0		0.72 / 11.1
	0.12 / 3.3				0.08 / 5		1.6 / 5.0		10.0 / 0.8		0.80 / 10.0
	0.16 / 2.5				0.10 / 4		2.0 / 4.0		14.0 / 0.57		3.2 / 2.5
	0.20 / 2.0				0.40 / 1		2.4 / 3.3				4.2 / 1.9
							3.2 / 2.5				

The number is parentheses in Table 8 are representative input/output current values. I_{OH} is specified for totem-pole or 3-state outputs by $V_{OH} \geqq 2.4 \sim 2.7V$.
In open-collector types the value for V_{OH} is specified as $5.5V < V_{OH} \leqq 15$ under fixed conditions for I_{OH}.
Therefore, the meaning of I_{OH} for open-collector types differs somewhat from totem-pole and 3-state types. The I_{OH} will change according to the voltage when an external resistance and power supply are used, and so a normal fan-out is not indicated.
Table 10 shows some actual examples of fan-out.

Table 10 Fan-out examples

TTL combinations						F_{OH} $\left(\frac{I_{OH}}{I_{IH}}\right)$	F_{OL} $\left(\frac{I_{OH}}{I_{IH}}\right)$
Drive output side			Load input side				
Sample	I_{OH} (mA)	I_{OL} (mA)	Sample	I_{IH} (mA)	I_{IL} (mA)		
DN74LS00	0.4	8.0	DN74LS00	0.02	0.4	20	20
DN74LS14	0.4	8.0	DN74LS90	Reset input 0.02	Reset input 0.4	20	20
				A input 0.04	A input 2.4	10	3.3
				B input 0.08	B input 3.2	5	2.5
DN74LS365	2.6	24.0	DN74LS283A	C_O input 0.02	C_O input 0.4	130	60
				Input except C_O 0.04	Input except C_O 0.8	65	30

Whichever is smaller, F_{OH} or F_{OL}, becomes the maximum fan-out number (often represented by F_{OL}). When $F_O \leqq 1$ is the normal condition, it is necessary to consider going through a buffer driver (I_{OL} = 24mA).

4. Electrical Characteristics

4.1 DC characteristics

These characteristics specify the voltage and current applied to the input pins and power supply pins of an IC under the most unfavorable conditions specified for the product's dispersion and variations in the power supply voltage and ambient temperature.

4.2 AC characteristics

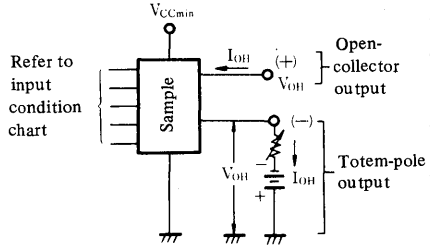
These characteristics specify the propagation delay time and maximum repeated frequency under conditions including an ambient temperature of Ta = 25°C and power supply voltage of V_{CC} = 5V.
The input pulse fixes the specified pulse width (t_w), pulse amplitude (V_P), input repeated frequency (PRR), rise time (t_r), and fall time (t_f), and they are measured with the output connected to a specified load.

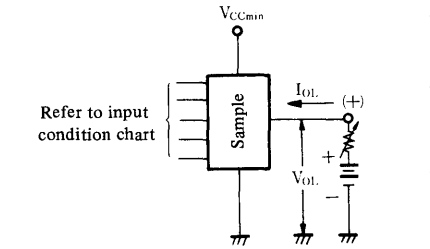
4.3 Measuring DC characteristics

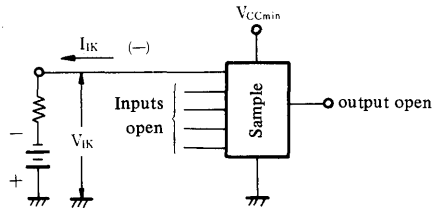
The measuring method for each characteristic is shown. For particularly ambiguous conditions for MSI, etc., they are specified on the individual specification sheets.

Table 11 Measuring methods for DC characteristics

<table>
<tr><th>Item</th><th>Measuring method</th><th>Function</th><th>Input conditions</th></tr>
<tr><td>(4.3.1)

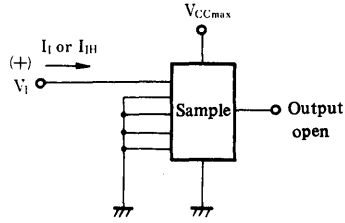
V_{IH}
V_{IL}
V_{OH}
I_{OH}</td><td> 
</td><td>NAND</td><td>Measured inputs are $V_{IL(max)}$; all others are 4.5V.</td></tr>
<tr><td></td><td></td><td>AND</td><td>All inputs are $V_{IH(min)}$.</td></tr>
<tr><td></td><td></td><td>NOR</td><td>All inputs are $V_{IL(max)}$.</td></tr>
<tr><td></td><td></td><td>OR</td><td>Measured inputs are $V_{IH(min)}$; all others are GND.</td></tr>
<tr><td></td><td></td><td>AND-OR-INVERT</td><td>Measured inputs (1 input of each AND gate) are $V_{IL(max)}$; all others are 4.5V.</td></tr>
<tr><td></td><td></td><td colspan="2">Note:
The ICs with a 3-state output structure fix the input conditions so that the output will be enabled (low impedance).</td></tr>
<tr><td>(4.3.2)

V_{IH}
V_{IL}
V_{OL}</td><td> 
</td><td>NAND</td><td>All inputs are $V_{IH(min)}$.</td></tr>
<tr><td></td><td></td><td>AND</td><td>Measured inputs are $V_{IL(max)}$; all others are 4.5V.</td></tr>
<tr><td></td><td></td><td>NOR</td><td>Measured inputs are $V_{IL(min)}$; all others are GND.</td></tr>
<tr><td></td><td></td><td>OR</td><td>All inputs are $V_{IL(max)}$.</td></tr>
<tr><td></td><td></td><td>AND-OR-INVERT</td><td>All measured inputs of AND gates are $V_{IH(min)}$; all others are GND.</td></tr>
<tr><td></td><td></td><td colspan="2">Note:
For ICs with a 3-state output structure, fix the input conditions so that the output will be enabled (low impedance).</td></tr>
<tr><td>(4.3.3)

V_{IK}</td><td colspan="3"> 

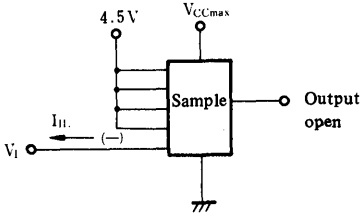
Note: Measured for each input.</td></tr>
</table>

(4.3.4) I_I, I_{IH}



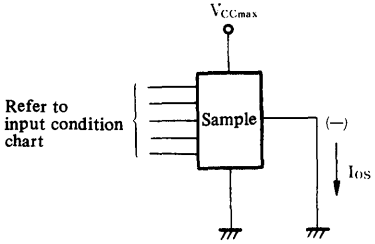
Note:
1. Measured for each input.
2. When measuring AND-OR-INVERT gates, the inputs of the AND gates not being measured are open when measuring I_I and grounded when measuring I_{IH}.
3. When measuring I_{IN}, V_I is 2.7V, and when measuring I_I, refer to the individual data sheets for conditions of V_I.

(4.3.5) I_{IL}



Note:
1. Measured for each input.
2. When measuring AND-OR-INVERT gates, the AND gates not being measured are open.

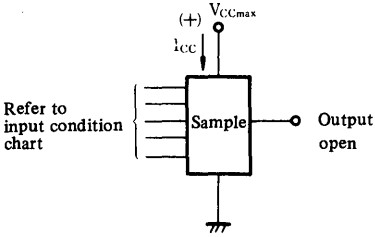
(4.3.6) I_{OS}



Function	Input conditions
NAND	All inputs are GND.
AND	All inputs are 4.5V.
NOR	All inputs are GND.
OR	All inputs are 4.5V.
AND-OR-INVERT	All inputs are GND.

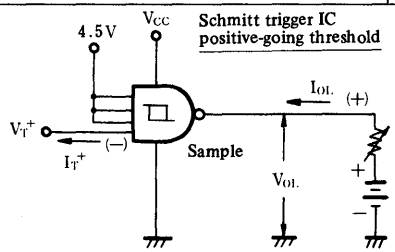
Note:
1. For ICs with a 3-state output structure, fix the input conditions so that the output will be enabled (low impedance).
2. Do not ground two or more outputs at a time. Perform measurements quickly.

(4.3.7) I_{CC}

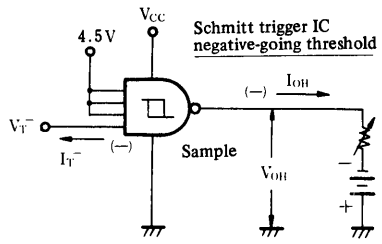
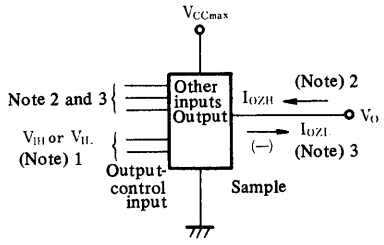


Function	Input conditions	
	I_{CCH}	I_{CCL}
NAND	All inputs are GND.	All inputs are 4.5V.
AND	All inputs are 4.5V.	All inputs are GND.
NOR	All inputs are GND.	One input is 4.5V; all others are GND.
OR	One input is 4.5V; all others are GND.	All inputs are GND.
AND-OR-INVERT	All inputs are GND.	All inputs of one AND gate are 4.5V; all other inputs are GND.

(4.3.8) V_T^+, I_T^+, V_{OL}



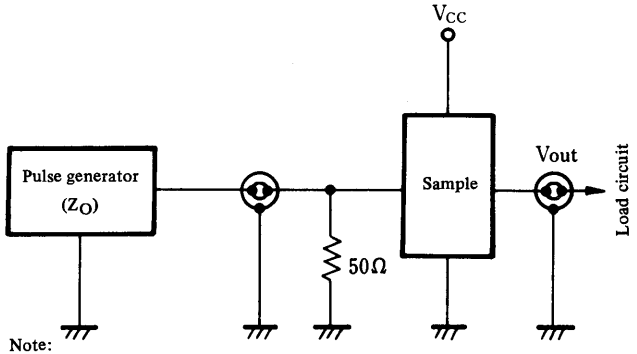
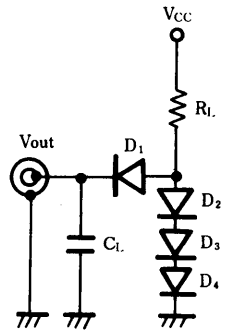
Note:
1. When measuring V_T^+ and I_T^+, V_{CC} is either 5V or $V_{CC(min)}$ depending on the type of IC. It is $V_{CC(min)}$ when measuring V_{OL}.
2. Measured for each input.

Item	Measuring method
(4.3.9) V_T^- I_T^- V_{OH}	 Note: 1. V_{CC} is either 5V or V_{CC}(min) when measuring V_T^- and I_T^- depending on the type of IC. V_{CC} is $V_{CC(min)}$ when measuring V_{OH}. 2. Measured for all inputs.
(4.3.10) I_{OZH} I_{OZL}	Current when 3-state output is disabled  Note: 1. The input conditions are fixed so that the output is disabled and becomes high impedance. 2. When applying the voltage of a HIGH level to the output and measuring, these input conditions are fixed so that if the output is enabled it becomes LOW. 3. When applying the voltage of a LOW level to the output and measuring, these input conditions are fixed so that if the output is enabled it becomes HIGH.

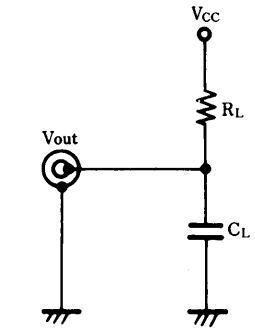
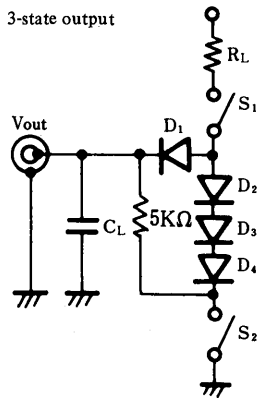
4.4 Measuring AC characteristics

The measuring methods for the switching characteristics and maximum frequency are shown. For particularly ambiguous conditions for MSI, etc., they are specified on the individual specification sheets, so please refer there.

Table 12 Measuring method for AC characteristics

Item	Measuring method	Output load circuit
(4.4.1) f_{max} t_{PHL} t_{PLH} t_{HZ} t_{LZ} t_{ZH} t_{ZL}	 Note: 1. Requirements for pulse generator PRR = 1 MHz, $t_r \leqq 6$ns, $t_f \leqq 6$ns $t_W = 500$ns, $V_P = 3V_{P-P}$, $Z_O = 50\Omega$	Totem-pole output 

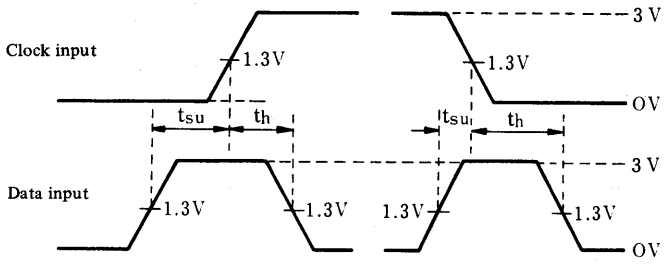
(Cont'd)

Item	Measuring method	Output load circuit
(4.4.1) (Cont'd) f_{max} t_{PHL} t_{PLH} t_{HZ} t_{LZ} t_{ZH} t_{ZL}	2. The electrostatic capacity C_L includes the suspension capacity of both the probe and measuring device. 3. Measurement of f_{max} is performed at $t_r = t_f \leqq 2.5$ns 4. All diodes ($D_1 \sim D_4$) used are MA161. 5. The relationship between SW_1 and SW_2 and characteristics in ICs with a 3-stage output structure are shown below. 6. Refer to the individual data sheets for conditions for R_L and C_L. Normally R_L = 2kΩ and C_L = 15 PF; for buffer driver ICs the values of R_L and C_L are different.	Open-collector output  3-state output 

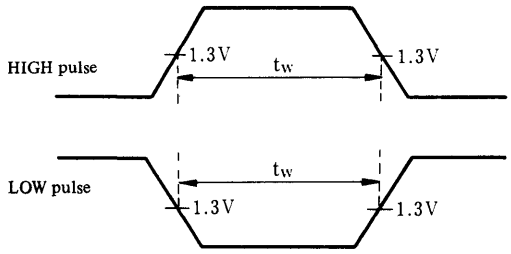
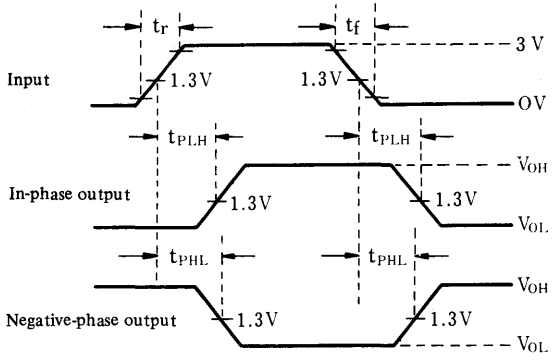
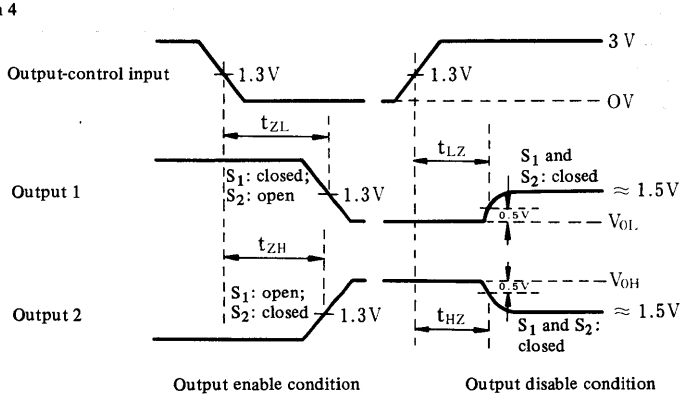
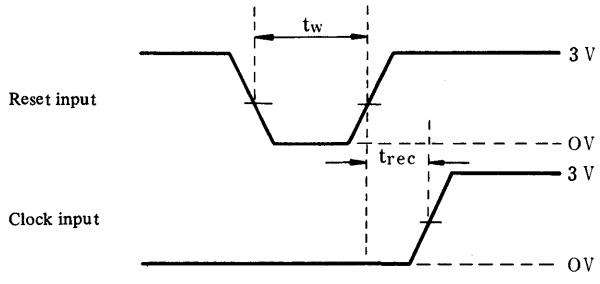
Item	S_1	S_2	Output condition
t_{PHL}	Closed	Closed	Low impedance (output enable)
t_{PLH}			
t_{ZH}	Closed	Closed	
t_{ZL}	Closed	Open	
t_{HZ}	Closed	Closed	High impedance (output disable)
t_{LZ}	Closed	Closed	

4.5 Interrelationships of input/output waveforms

Diagrams of the interrelationships of the set-up (t_{su}) and hold (t_h) times for the pulse voltage waveforms, pulse widths (t_w), propagation delay times (t_{PHL}, t_{PLH}), enable and disable times for 3-state outputs, and recovery times are shown.

Interrelationships of input/output waveforms	
Set-up and hold times	Waveform 1 

(Cont'd)

Interrelationships of input/output waveforms	
Pulse widths	Waveform 2 
Propagation delay times	Waveform 3 
Enable and disable times for 3-state outputs	Waveform 4 
Recovery times	Waveform 5 

5. Typical Characteristics of the Basic Gate

Typical characteristics of the basic gate for DN74LS TTL are diagrammed. Figs. 18 ~ 31 show the typical characteristics of the Schmitt trigger.

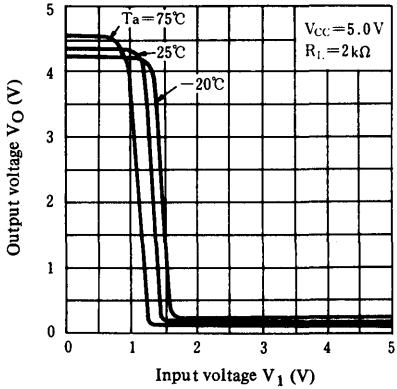


Fig. 18 Input/output transfer characteristics

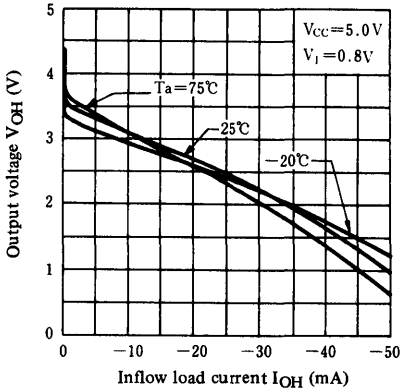


Fig. 19 HIGH output characteristics

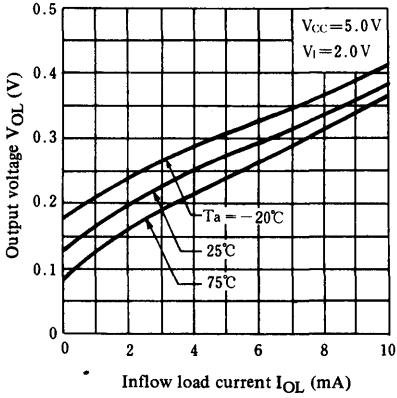


Fig. 20 LOW output characteristics

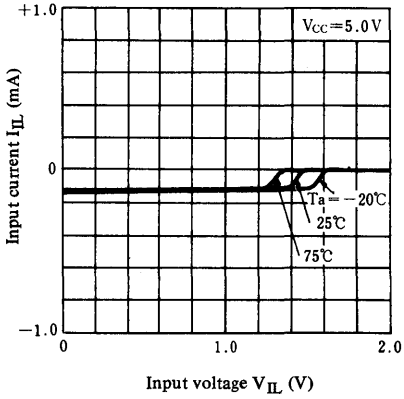


Fig. 21 Input voltage current characteristics

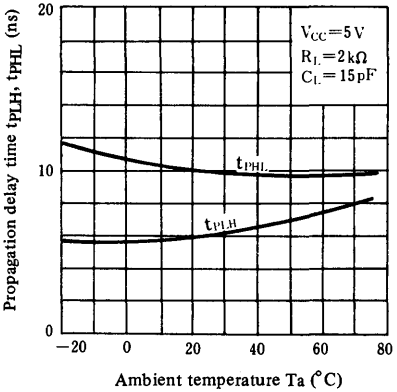


Fig. 22 Propagation time vs. ambient temperature characteristics

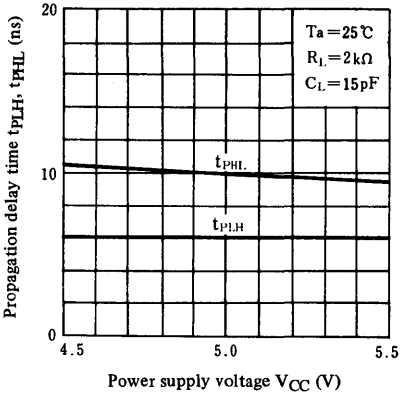


Fig. 23 Propagation time vs. power supply voltage characteristics

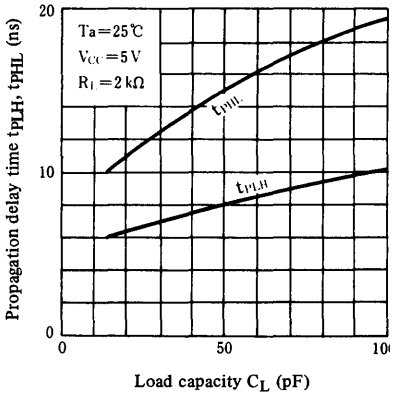


Fig. 24 Propagation time vs. load capacity characteristics

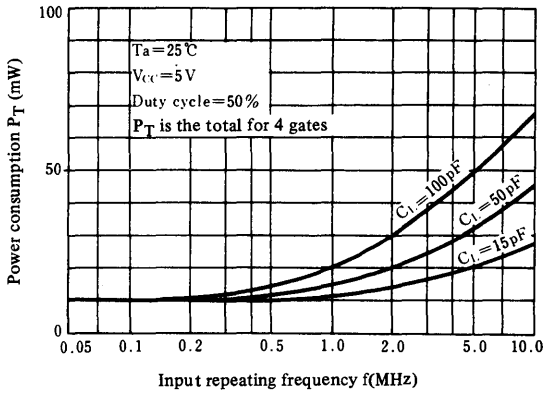


Fig. 25 Power consumption vs. input frequency characteristics

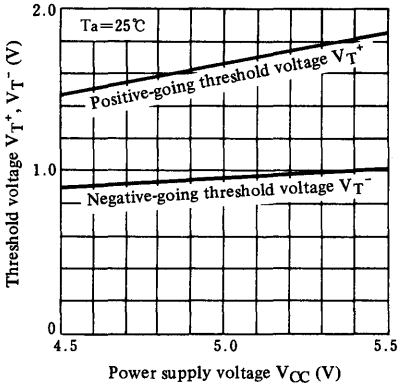


Fig. 26 Threshold voltage vs. power supply voltage

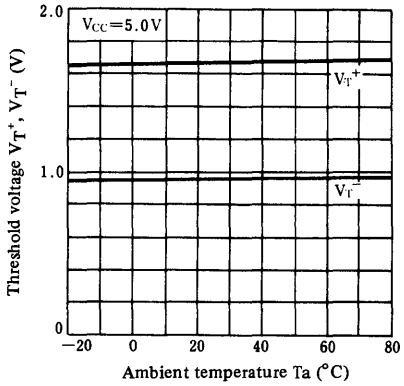


Fig. 27 Threshold voltage vs. ambient temperature

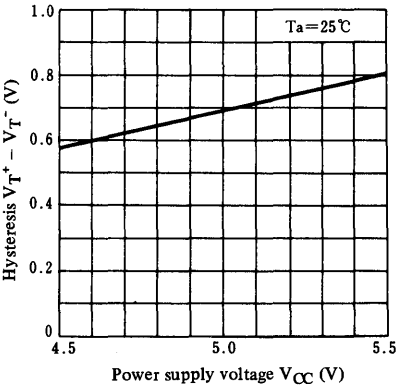


Fig. 28 Hysteresis vs. power supply voltage

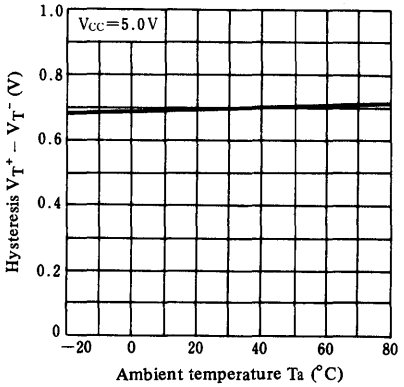


Fig. 29 Hysteresis vs. ambient temperature

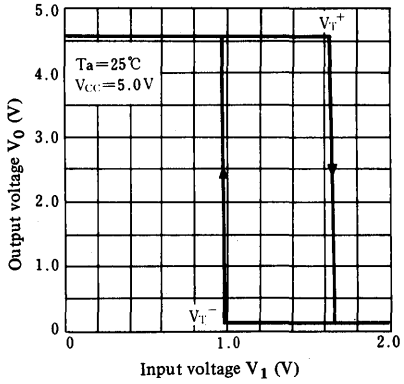


Fig. 30 Input/output propagation characteristics

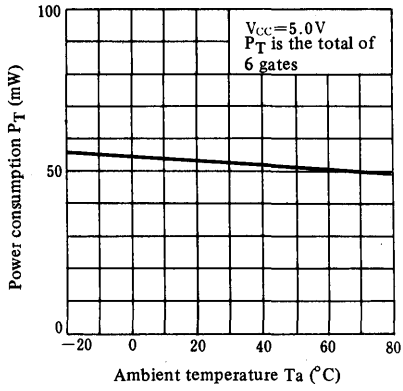


Fig. 31 Power consumption vs. ambient temperature

6. External Diagrams of Packages

Unit: mm

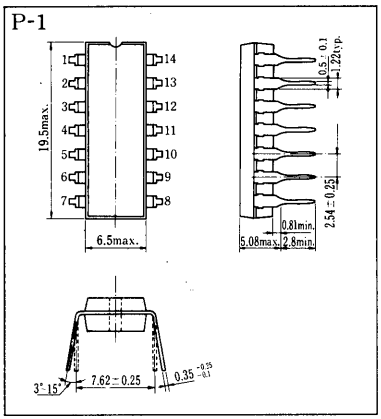


Fig. 32 Plastic DIL-14 pin

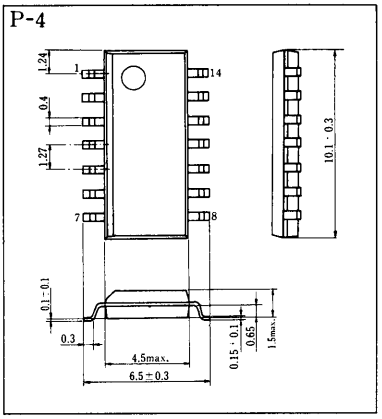


Fig. 33 Plastic SO-14 pin

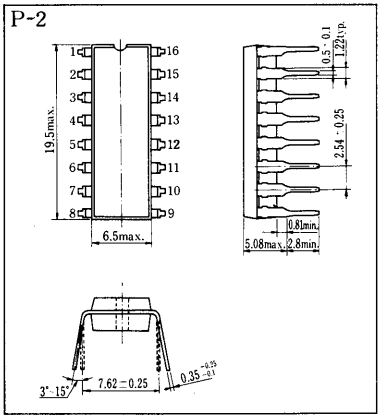


Fig. 34 Plastic DIL-16 pin

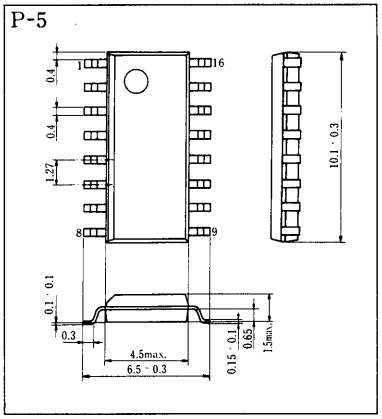


Fig. 35 Plastic SO-16 pin

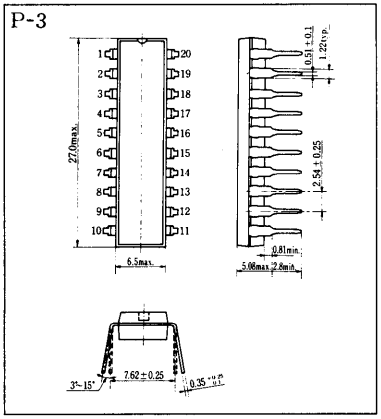


Fig. 36 Plastic DIL-20 pin

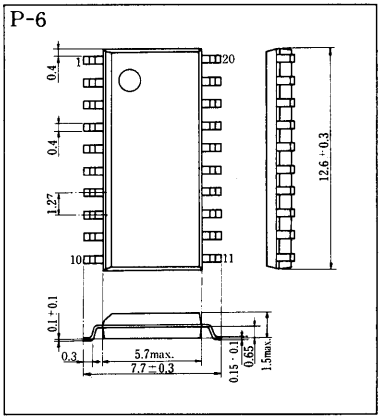


Fig. 37 Plastic SO-20 pin

Individual Specifications

DN74LS00

Quad 2-input Positive NAND Gates

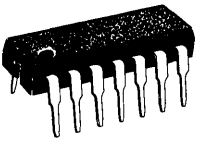
■ Description

DN74LS00 Contains four 2-input positive isolation NAND gate circuits.

■ Features

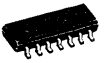
- Low power consumption (P_d = 8mW typical)
- High speed (t_{pd} = 9.5ns typical)
- Low output impedance
- Wide operating temperature range (Ta = −20 to +75°C)

P-1



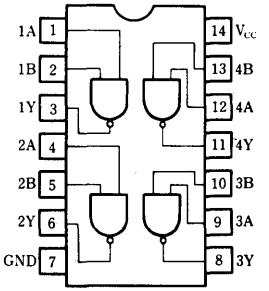
14-pin plastic DIL package

P-4



14-pin Panaflat package (SO-14D)

Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−400	μA
	I_{OL}			8	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2.0V$ $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	3.4		V
	V_{OL1}	$V_{CC}=4.75V$ $V_{IH}=2V$	$I_{OL}=4mA$		0.25	0.4	V
	V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				20	μA
	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.4	mA
	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.1	mA
Output short circuit current**	I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−100	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current	I_{CCH}	$V_{CC}=5.25V$			0.8	1.6	mA
	I_{CCL}	$V_{CC}=5.25V$			2.4	4.4	mA

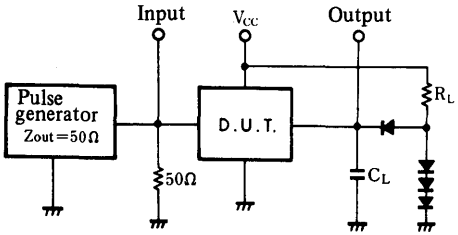
* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	$C_L=15pF$, $R_L=2k\Omega$		9	15	ns
	t_{PHL}			10	15	ns

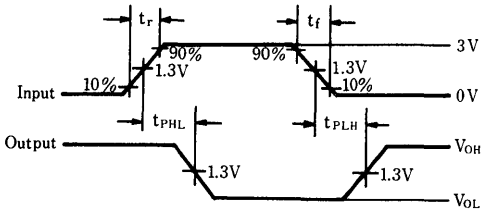
※ Switching parameter measurement information

1. Measurement circuit



Notes
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161.

2. Waveforms



Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.

DN74LS01

Quad 2-input Positive NAND Gates (with Open Collector Outputs)

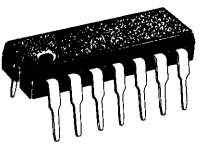
■ Description

DN74LS01 contains four 2-input positive isolation NAND gate circuits with open collector outputs.

■ Features

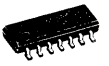
- "Wired" AND capability
- Low power consumption (P_d = 8mW typical)
- High speed (t_{pd} = 16ns typical)
- Wide operating temperature range (Ta = −20 to +75°C)

P-1



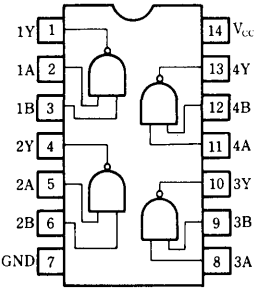
14-pin plastic DIL package

P-4



14-pin Panaflat package (SO-14D)

Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
HIGH level output voltage	V_{OH}			5.5	V
LOW level output voltage	I_{OL}			8	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OL1}	$V_{CC}=4.75V$ $V_{IH}=2V$	$I_{OL}=4mA$		0.25	0.4	V
	V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				20	μA
	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.4	mA
	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.1	mA
Output current	I_{OH}	$V_{CC}=4.75V$, $V_{IL}=0.8V$ $V_{OH}=5.5V$				100	μA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current	I_{CCH}	$V_{CC}=5.25V$			0.8	1.6	mA
	I_{CCL}	$V_{CC}=5.25V$			2.4	4.4	mA

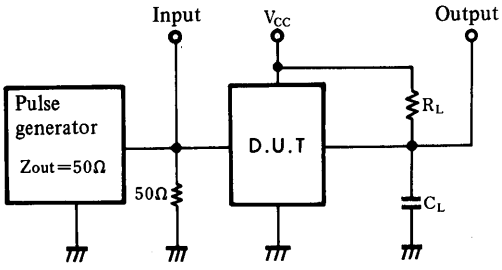
* When constant at V_{CC} = 5V, Ta = 25°C.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	$C_L=15pF$, $R_L=2k\Omega$		17	32	ns
	t_{PHL}			15	28	ns

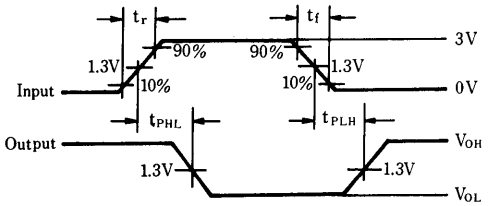
※ Switching parameter measurement information

1. Measurement circuit



Notes
1. C_L includes probe and tool floating capacitance.

2. Waveforms



Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.

DN74LS02

Quad 2-input Positive NOR Gates

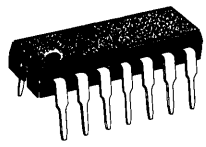
■ Description

DN74LS02 contains four 2-input positive isolation NOR gate circuits.

■ Features

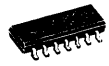
- Low power consumption (P_d = 11mW typical)
- High speed (t_{pd} = 10ns typical)
- Low output impedance
- Wide operating temperature range (Ta = −20 to +75°C)

P-1



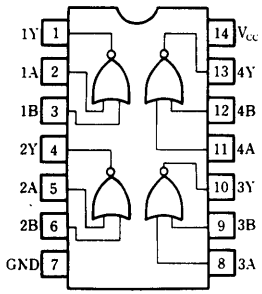
14-pin plastic DIL package

P-4



14-pin Panaflat package (SO-14D)

Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−400	μA
	I_{OL}			8	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IL}=0.8V$ $I_{OH}=-400\mu A$		2.7	3.4		V
	V_{OL1}	$V_{CC}=4.75V$ $V_{IH}=2V$	$I_{OL}=4mA$		0.25	0.4	V
	V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				20	μA
	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.4	mA
	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.1	mA
Output short circuit current**	I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−100	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current	I_{CCH}	$V_{CC}=5.25V$,			1.6	3.2	mA
	I_{CCL}	$V_{CC}=5.25V$,			2.8	5.4	mA

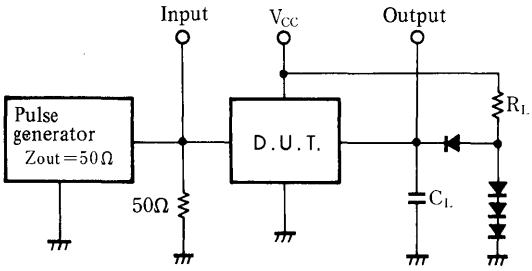
* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	$C_L=15pF$, $R_L=2k\Omega$		10	15	ns
	t_{PHL}			10	15	ns

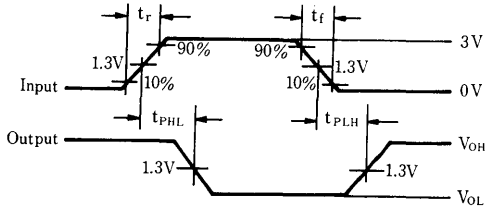
※ Switching parameter measurement information

1. Measurement circuit



Notes
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161.

2. Waveforms



Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.

DN74LS03

Quad 2-input Positive NAND Gates (with Open Collector Outputs)

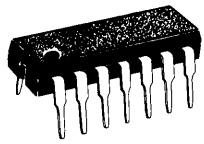
■ Description

DN74LS03 contains four 2-input positive isolation NAND gate circuits with open collector outputs.

■ Features

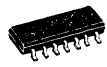
- "Wired" AND capability
- Low power consumption (P_d = 8mW typical)
- High speed (t_{pd} = 16ns typical)
- Wide operating temperature range (Ta = –20 to +75°C)

P-1



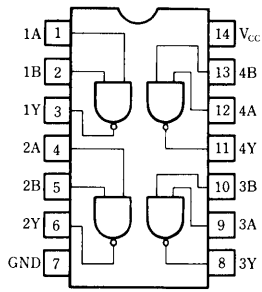
14-pin plastic DIL package

P-4



14-pin Panaflat package (SO-14D)

Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
HIGH level output voltage	V_{OH}			5.5	V
LOW level output voltage	I_{OL}			8	mA
Operating temperature range	Topr	–20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OL1}	$V_{CC}=4.75V$, $V_{IH}=2V$	$I_{OL}=4mA$		0.25	0.4	V
	V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
	I_I	$V_{CC}=5.25V$, $V_I=7V$				0.1	mA
Output current	I_{OH}	$V_{CC}=4.75V$, $V_{IL}=0.8V$, $V_{OH}=5.5V$				100	μA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$, $I_I=-18mA$				−1.5	V
Supply current	I_{CCH}	$V_{CC}=5.25V$			0.8	1.6	mA
	I_{CCL}	$V_{CC}=5.25V$			2.4	4.4	mA

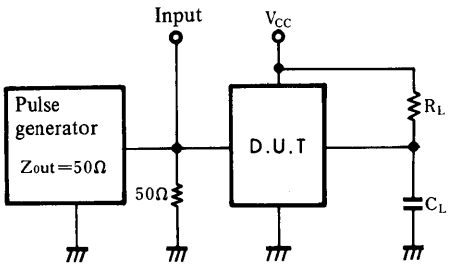
* When constant at V_{CC} = 5V, Ta = 25°C.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	$C_L=15pF$, $R_L=2k\Omega$		17	32	ns
	t_{PHL}			15	28	ns

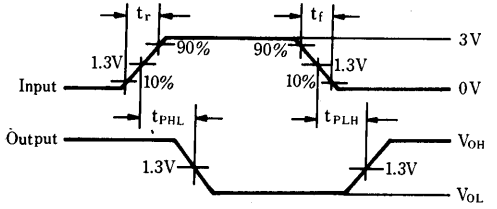
※ Switching parameter measurement information

1. Measurement circuit



Notes
1. C_L includes probe and tool floating capacitance.

2. Waveforms



Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.

DN74LS04

Hex Inverters

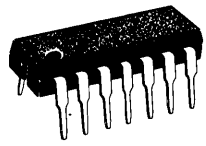
■ Description

DN74LS04 contains six inverter circuits.

■ Features

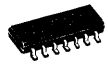
- Low power consumption (P_d = 12mW typical)
- High speed (t_{pd} = 9.5 ns typical)
- Low output impedance
- Wide operating temperature range (Ta = −20 to +75°C)

P-1



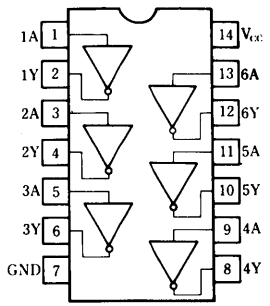
14-pin plastic DIL package

P-4



14-pin Panaflat package (SO-14D)

Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−400	μA
	I_{OL}			8	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IL}=0.8V$ $I_{OH}=-400\mu A$		2.7	3.4		V
	V_{OL1}	$V_{CC}=4.75V$ $V_{IH}=2V$	$I_{OL}=4mA$		0.25	0.4	V
	V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				20	μA
	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.4	mA
	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.1	mA
Output short circuit current**	I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−100	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current	I_{CCH}	$V_{CC}=5$ [illegible]			1.2	2.4	mA
	I_{CCL}	$V_{CC}=5.25V$,			3.6	6.6	mA

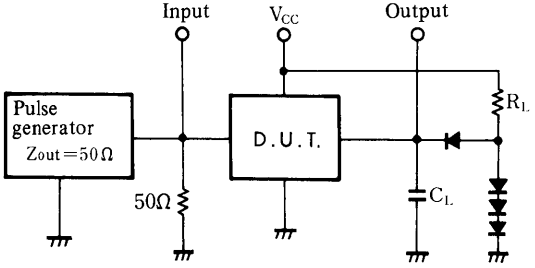
* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

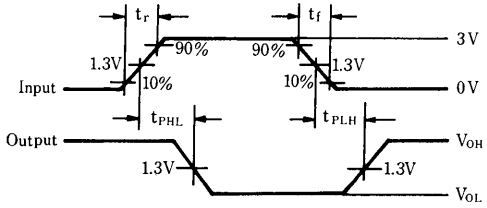
Parameter	Sym	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	$C_L=15pF$, $R_L=2k\Omega$		9	15	ns
	t_{PHL}			10	15	ns

※ Switching parameter measurement information

1. Measurement circuit



2. Waveforms



Notes
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161.

Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.

DN74LS05

Hex Inverters (with Open Collector Outputs)

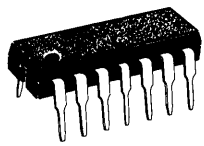
■ Description

DN74LS05 contains six inverter circuits with open collector outputs.

■ Features

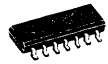
- "Wired" AND capability
- Low power consumption (P_d = 12mW typical)
- High speed (t_{pd} = 16ns typical)
- Wide operating temperatures range (Ta = −20 to +75°C)

P-1



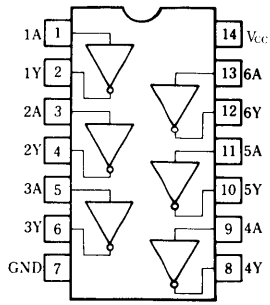
14-pin plastic DIL package

P-4



14-pin Panaflat package (SO-14D)

Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
HIGH level output voltage	V_{OH}			5.5	V
LOW level output voltage	I_{OL}			8	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OL1}	$V_{CC}=4.75V$, $V_{IH}=2V$	$I_{OL}=4mA$		0.25	0.4	V
	V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
	I_I	$V_{CC}=5.25V$, $V_I=7V$				0.1	mA
Output current	I_{OH}	$V_{CC}=4.75V$, $V_{IL}=0.8V$, $V_{OH}=5.5V$				100	μA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$, $I_I=-18mA$				−1.5	V
Supply current	I_{CCH}	$V_{CC}=5.25V$			1.2	2.4	mA
	I_{CCL}	$V_{CC}=5.25V$			3.6	6.6	mA

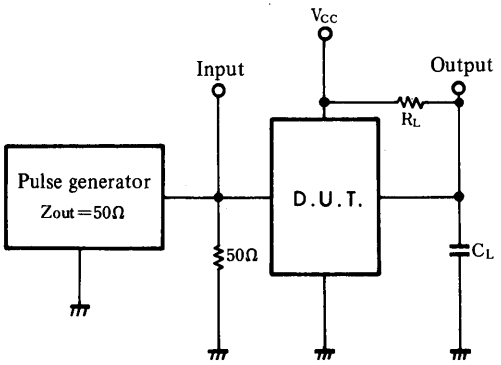
* When constant at V_{CC} = 5V, Ta = 25°C.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	$C_L=15pF$, $R_L=2k\Omega$		17	32	ns
	t_{PHL}			15	28	ns

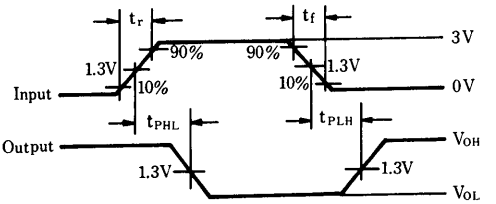
※ Switching parameter measurement information

1. Measurement circuit



Notes
1. C_L includes probe and tool floating capacitance.

2. Waveforms



Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.

DN74LS08

Quad 2-input Positive AND Gates

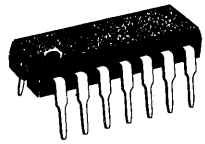
■ Description

DN74LS08 contains four 2-input positive isolation AND gate circuits.

■ Features

- Low power consumption (P_d = 17mW typical)
- High speed (t_{pd} = 9ns typical)
- Low output impedance
- Wide operating temperature range (Ta = −20 to +75°C)

P-1

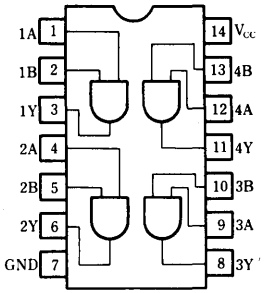


14-pin plastic DIL package

P-4

14-pin Panaflat package (SO-14D)

Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−400	μA
	I_{OL}			8	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$ $I_{OH}=-400\mu A$		2.7	3.4		V
	V_{OL1}	$V_{CC}=4.75V$	$I_{OL}=4mA$		0.25	0.4	V
	V_{OL2}	$V_{IL}=0.8V$	$I_{OL}=8mA$		0.35	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				20	μA
	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.4	mA
	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.1	mA
Output short circuit current**	I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−100	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current	I_{CCH}	$V_{CC}=5.25V$,			2.4	4.8	mA
	I_{CCL}	$V_{CC}=5.25V$,			4.4	8.8	mA

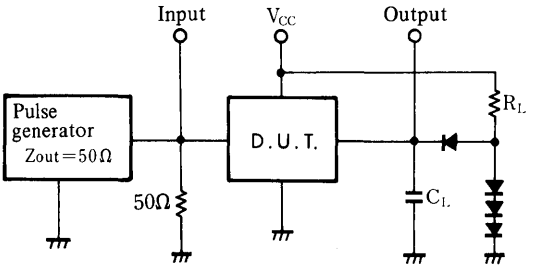
* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	$C_L=15pF$, $R_L=2k\Omega$		8	15	ns
	t_{PHL}			10	20	ns

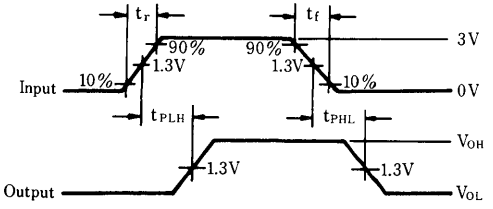
※ Switching parameter measurement information

1. Measurement circuit



Notes
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161.

2. Waveforms



Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.

DN74LS09

Quad 2-input Positive AND Gates (with Open Collector Outputs)

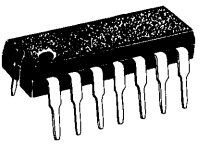
■ Description

DN74LS09 contains four 2-input positive isolation AND gate circuits with open collector outputs.

■ Features

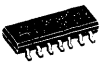
- "Wired" AND capability
- Low power consumption (P_d = 17mW typical)
- High speed (t_{pd} = 18.5ns typical)
- Wide operating temperature range (Ta = −20 to +75°C)

P-1



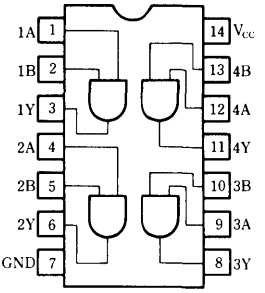
14-pin plastic DIL package

P-4



14-pin Panaflat package (SO-14D)

Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
HIGH level output voltage	V_{OH}			5.5	V
LOW level output voltage	I_{OL}			8	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OL1}	$V_{CC}=4.75V$, $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
	V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
	I_I	$V_{CC}=5.25V$, $V_I=7V$				0.1	mA
Output current	I_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{OH}=5.5V$				100	μA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$, $I_I=-18mA$				−1.5	V
Supply current	I_{CCH}	$V_{CC}=5.25V$			2.4	4.8	mA
	I_{CCL}	$V_{CC}=5.25V$			4.4	8.8	mA

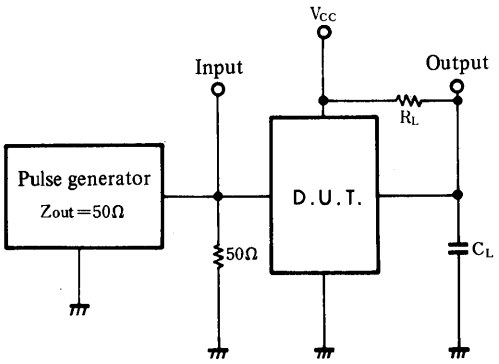
* When constant at V_{CC} = 5V, Ta = 25°C.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	$C_L=15pF$, $R_L=2k\Omega$		20	35	ns
	t_{PHL}			17	35	ns

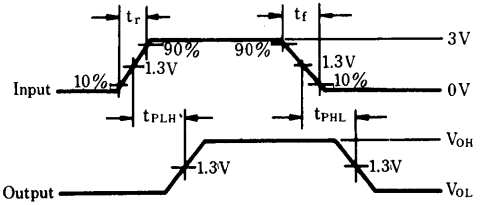
※ Switching parameter measurement information

1. Measurement circuit



Notes
1. C_L includes probe and tool floating capacitance.

2. Waveforms



Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.

DN74LS10

Triple 3-input Positive NAND Gates

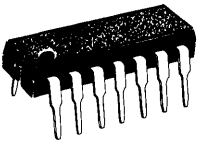
■ Description

DN74LS10 contains three 3-input positive isolation NAND gate circuits.

■ Features

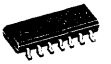
- Low power consumption (P_d = 6mW typical)
- High speed (t_{pd} = 10ns typical)
- Low output impedance
- Wide operating temperature range (Ta = –20 to +75°C)

P-1



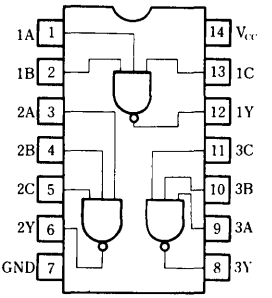
14-pin plastic DIL package

P-4



14-pin Panaflat package (SO-14D)

Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−400	μA
	I_{OL}			8	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IL}=0.8V$ $V_{IH}=2V$, $I_{OH}=-400\mu A$		2.7	3.4		V
	V_{OL1}	$V_{CC}=4.75V$ $V_{IH}=2V$	$I_{OL}=4mA$		0.25	0.4	V
	V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				20	μA
	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.4	mA
	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.1	mA
Output short circuit current**	I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−100	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current	I_{CCH}	$V_{CC}=5.25V$,			0.6	1.2	mA
	I_{CCL}	$V_{CC}=5.25V$,			1.8	3.3	mA

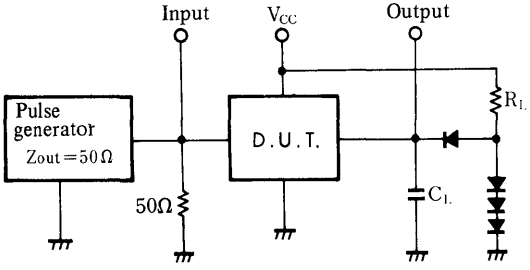
* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	$C_L=15pF$, $R_L=2k\Omega$		9	15	ns
	t_{PHL}			10	15	ns

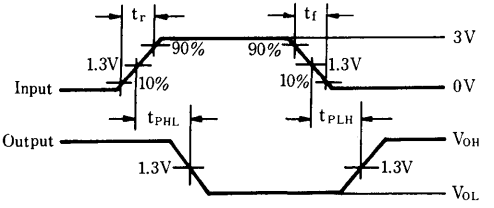
※ Switching parameter measurement information

1. Measurement circuit



Notes
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161.

2. Waveforms



Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.

DN74LS11

Triple 3-input Positive AND Gates

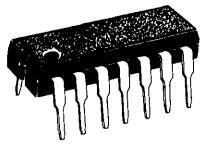
■ Description

DN74LS11 contains three 3-input positive isolation AND gate circuits.

■ Features

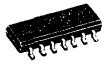
- Low power consumption (P_d = 13mW typical)
- High speed (t_{pd} = 9ns typical)
- Low output impedance
- Wide operating temperature range (Ta = −20 to +75°C)

P-1



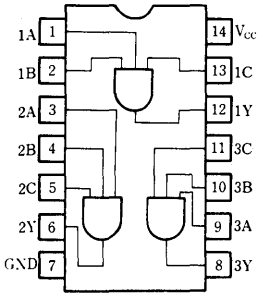
14-pin plastic DIL package

P-4



14-pin Panaflat package (SO-14D)

Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−400	μA
	I_{OL}			8	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IL}=0.8V$ $V_{IH}=2V$, $I_{OH}=-400\mu A$		2.7	3.4		V
	V_{OL1}	$V_{CC}=4.75V$ $V_{IH}=2.0V$	$I_{OL}=4mA$		0.25	0.4	V
	V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				20	μA
	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.4	mA
	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.1	mA
Output short circuit current**	I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−100	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current	I_{CCH}	$V_{CC}=5.25V$,			1.8	3.6	mA
	I_{CCL}	$V_{CC}=5.25V$,			3.3	6.6	mA

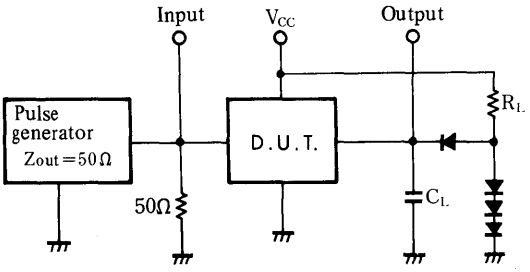
* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

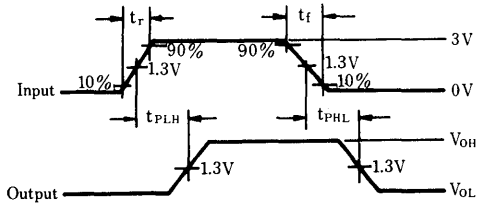
Parameter	Sym	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	$C_L=15pF$, $R_L=2k\Omega$		8	15	ns
	t_{PHL}			10	20	ns

※ Switching parameter measurement information

1. Measurement circuit



2. Waveforms



Notes
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161.

Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.

DN74LS12

Triple 3-input Positive NAND Gates (with Open Collector Outputs)

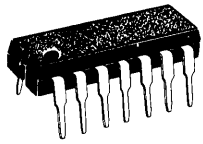
■ Description

DN74LS12 contains three 3-input positive isolation NAND gate circuits with open collector outputs.

■ Features

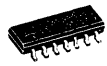
- "Wired" AND capability
- Low power consumption (P_d = 6mW typical)
- Wide operating temperature range (Ta = –20 to +75°C)

P-1



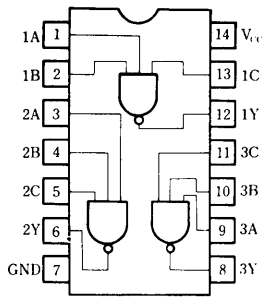
14-pin plastic DIL package

P-4



14-pin Panaflat package (SO-14D)

Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
HIGH level output voltage	V_{OH}			5.5	V
LOW level output voltage	I_{OL}			8	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OL1}	$V_{CC}=4.75V$, $V_{IH}=2V$	$I_{OL}=4mA$		0.25	0.4	V
	V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
	I_I	$V_{CC}=5.25V$, $V_I=7V$				0.1	mA
Output current	I_{OH}	$V_{CC}=4.75V$, $V_{IL}=0.8V$, $V_{OH}=5.5V$				100	μA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$, $I_I=-18mA$				−1.5	V
Supply current	I_{CCH}	$V_{CC}=5.25V$			0.7	1.4	mA
	I_{CCL}	$V_{CC}=5.25V$			1.8	3.3	mA

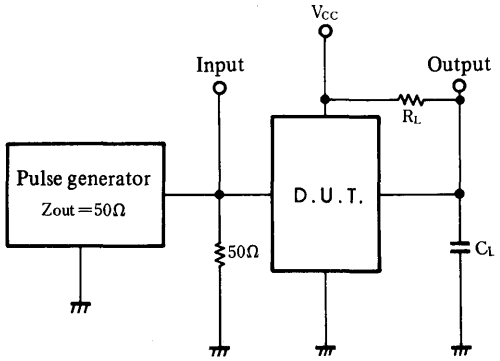
* When constant at V_{CC} = 5V, Ta = 25°C.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	$C_L=15pF$, $R_L=2k\Omega$		17	32	ns
	t_{PHL}			15	28	ns

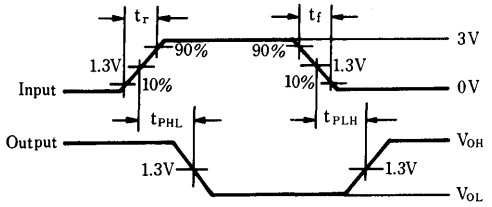
※ Switching parameter measurement information

1. Measurement circuit



Notes
1. C_L includes probe and tool floating capacitance.

2. Waveforms



Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.

DN74LS13

Dual 4-input Positive NAND Schmitt-Triggers

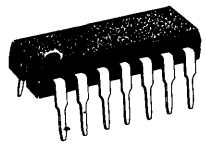
■ Description

DN74LS13 contains two 4-input positive isolation NAND circuits with Schmitt triggers.

■ Features

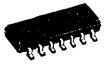
- Ideal for waveform shaping
- Wide hysteresis width (0.8V typical), high noise margin
- Low power consumption (P_d = 17.5mW typical)
- High speed (t_{pd} = 17ns typical)
- Wide operating temperature (Ta = −20 to +75°C)

P-1



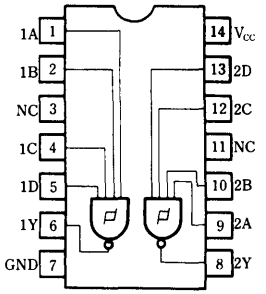
14-pin plastic DIL package

P-4



14-pin Panaflat package (SO-14D)

Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−400	μA
	I_{OL}			8	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input threshold voltage	V_{T+}	$V_{CC}=5V$		1.4	1.6	1.9	V
	V_{T-}	$V_{CC}=5V$		0.5	0.8	1.0	V
Hysteresis	$V_{T+}-V_{T-}$	$V_{CC}=5V$		0.4	0.8		V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $I_{OH}=-400\mu A$ $V_I=0.5V$		2.7	3.4		V
	V_{OL1}	$V_{CC}=4.75V$	$I_{OL}=4mA$		0.25	0.4	V
	V_{OL2}	$V_{CC}=4.75V$	$I_{OL}=8mA$		0.35	0.5	V
Input threshold current	I_{T+}	$V_{CC}=5V$ $V_I=V_{T+}$			−0.14		mA
	I_{T-}	$V_{CC}=5V$ $V_I=V_{T-}$			−0.18		mA
Input current	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				20	μA
	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.4	mA
	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.1	mA
Output short circuit current**	I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−100	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current	I_{CCH}	$V_{CC}=5.25V$			2.9	6	mA
	I_{CCL}	$V_{CC}=5.25V$			4.1	7	mA

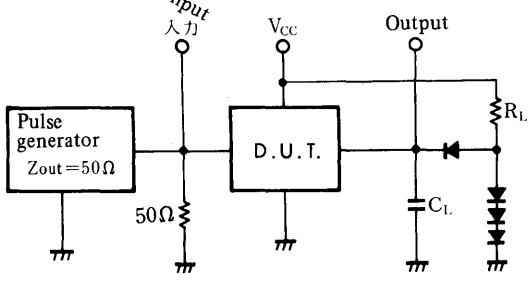
* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	$C_L=15pF$, $R_L=2k\Omega$		15	22	ns
	t_{PHL}			18	27	ns

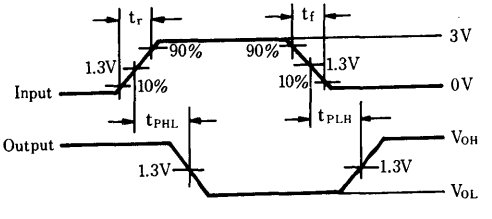
※ Switching parameter measurement information

1. Measurement circuit



Notes
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161.

2. Waveforms



Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.

DN74LS14

Hex Schmitt-Trigger Inverters

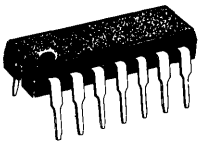
■ Description

DN74S14 contains six inverter circuits with Schmitt triggers.

■ Features

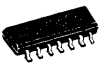
- Ideal for waveform shaping
- Low power consumption (P_d = 50mW typical)
- High speed (t_{pd} = 15ns typical)
- Wide operating temperature range (Ta = −20 to +75°C)

P-1



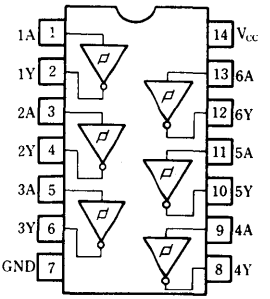
14-pin plastic DIL package

P-4



14-pin Panaflat package (SO-14D)

Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−400	μA
	I_{OL}			8	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions	Min	Typ*	Max	Unit
Input threshold voltage	V_T+	$V_{CC}=5V$	1.4	1.6	1.9	V
	V_T-	$V_{CC}=5V$	0.5	0.8	1.0	V
Hysteresis	$\triangle V_T$	$V_{CC}=5V$	0.4	0.8		V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $I_{OH}=-400\mu A$ $V_I=0.5V$	2.7	3.4		V
	V_{OL}	$V_{CC}=4.75V$, $I_{OL}=4mA$ $V_I=1.9V$		0.25	0.4	V
	V_{OL}	$V_{CC}=4.75V$, $I_{OL}=8mA$ $V_I=1.9V$		0.35	0.5	V
Input threshold current	I_T+	$V_{CC}=5V$ $V_I=V_T+$		−0.14		mA
	I_T-	$V_{CC}=5V$ $V_I=V_T-$		−0.18		mA
Input current	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$			20	μA
	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$			−0.4	mA
	I_I	$V_{CC}=5.25V$ $V_I=7V$			0.1	mA
Output short circuit current**	I_{OS}	$V_{CC}=5.25V$ $V_O=0V$	−15		−100	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$ $V_I=-18mA$			−1.5	V
Supply current	I_{CCH}	$V_{CC}=5.25V$		8.6	16	mA
	I_{CCL}	$V_{CC}=5.25V$		12	21	mA

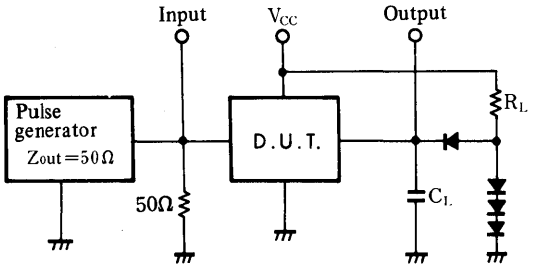
* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	$C_L=15pF$, $R_L=2k\Omega$		15	22	ns
	t_{PHL}			15	22	ns

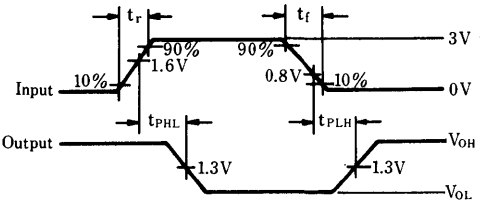
※ Switching parameter measurement information

1. Measurement circuit



Notes
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161.

2. Waveforms



Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.

DN74LS15

Triple 3-input Positive AND Gates (with Open Collector Outputs)

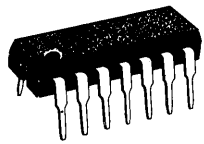
■ Description

DN74LS15 contains three 3-input positive isolation AND gate circuits with open collector outputs.

■ Features

- "Wired" AND capability
- Low power consumption (P_d = 13mW typical)
- High speed (t_{pd} = 18.5ns typical)
- Wide operating temperature range (Ta = –20 to +75°C)

P-1

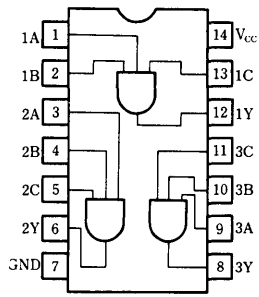


14-pin plastic DIL package

P-4

14-pin Panaflat package (SO-14D)

Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
HIGH level output voltage	V_{OH}			5.5	V
LOW level output voltage	I_{OL}			8	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OL1}	$V_{CC}=5.25V$	$I_{OL}=4mA$		0.25	0.4	V
	V_{OL2}	$V_{IL}=0.8V$	$I_{OL}=8mA$		0.35	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
	I_I	$V_{CC}=5.25V$, $V_I=7V$				0.1	mA
Output current	I_{OH}	$V_{CC}=4.75V$, $V_{OH}=5.5V$				100	μA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$, $I_I=-18mA$				−1.5	V
Supply current	I_{CCH}	$V_{CC}=5.25V$			1.8	3.6	mA
	I_{CCL}	$V_{CC}=5.25V$			3.3	6.6	mA

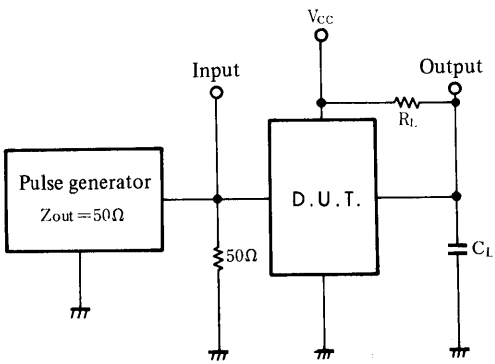
* When constant at V_{CC} = 5V, Ta = 25°C.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	$C_L=15pF$, $R_L=2k\Omega$		20	35	ns
	t_{PHL}			17	35	ns

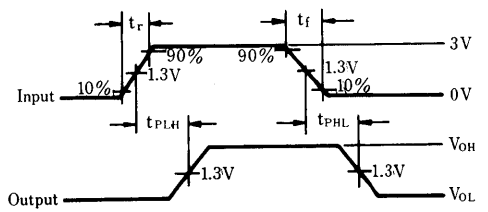
※ Switching parameter measurement information

1. Measurement circuit



Notes
1. C_L includes probe and tool floating capacitance.

2. Waveforms



Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.

DN74LS20

Dual 4-input Positive NAND Gates

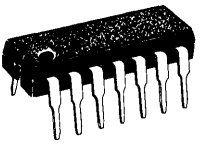
■ Description

DN74LS20 contains two 4-input positive isolation NAND gate circuits.

■ Features

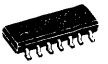
- Low power consumption (P_d = 4mW typical)
- High speed (t_{pd} = 10ns typical)
- Low output impedance
- Wide operating temperature range (Ta = −20 to +75°C)

P-1



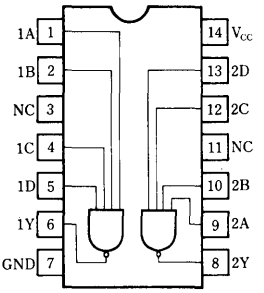
14-pin plastic DIL package

P-4



14-pin Panaflat package (SO-14D)

Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−400	μA
	I_{OL}			8	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IL}=0.8V$ $I_{OH}=-400\mu A$, $V_{IH}=2.0V$		2.7	3.4		V
	V_{OL1}	$V_{CC}=4.75V$	$I_{OL}=4mA$		0.25	0.4	V
	V_{OL2}	$V_{IH}=2V$, $V_{IL}=0.8V$	$I_{OL}=8mA$		0.35	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				20	μA
	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.4	mA
	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.1	mA
Output short circuit current**	I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−100	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current	I_{CCH}	$V_{CC}=5.25V$,			0.4	0.8	mA
	I_{CCL}	$V_{CC}=5.25V$,			1.2	2.2	mA

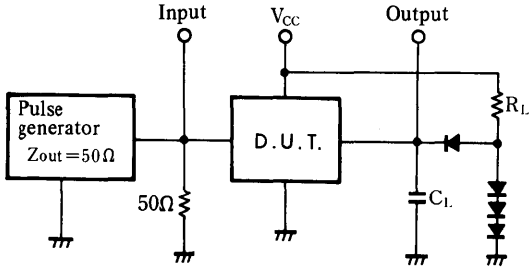
* When constant at V_{CC} = 5V, Ta = 25°C.
** On ly one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	$C_L=15pF$, $R_L=2k\Omega$		9	15	ns
	t_{PHL}			10	15	ns

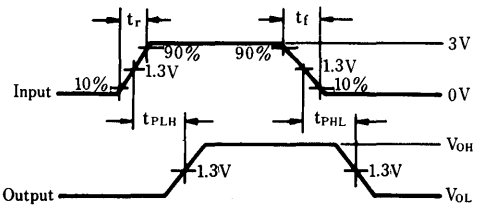
※ Switching parameter measurement information

1. Measurement circuit



Notes
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161.

2. Waveforms



Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.

DN74LS21

Dual 4-input Positive AND Gates

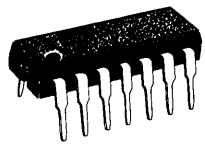
■ Description

DN74LS21 contains two 4-input positive isolation AND gate circuits.

■ Features

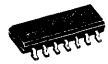
- Low power consumption (P_d = 8.5 mW typical)
- High speed (t_{pd} = 9ns typical)
- Wide operating temperature range (Ta = –20 to +75°C)

P-1



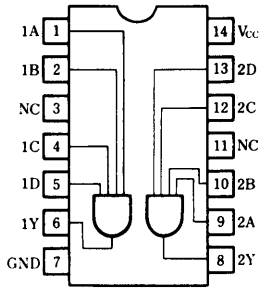
14-pin plastic DIL package

P-4



14-pin Panaflat package (SO-14D)

Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−400	μA
	I_{OL}			8	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$ $I_{OH}=-400\mu A$		• 2.7	3.4		V
	V_{OL1}	$V_{CC}=4.75V$, $V_{IH}=2V$ $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
	V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				20	μA
	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.4	mA
	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.1	mA
Output short circuit current**	I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−100	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current	I_{CCH}	$V_{CC}=5.25V$,			1.2	2.4	mA
	I_{CCL}	$V_{CC}=5.25V$,			2.2	4.4	mA

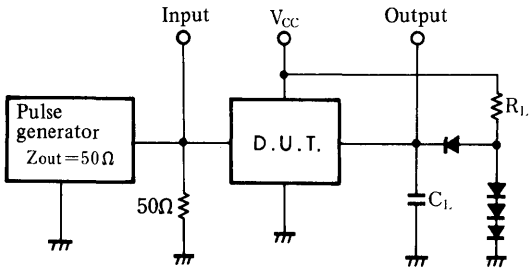
* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

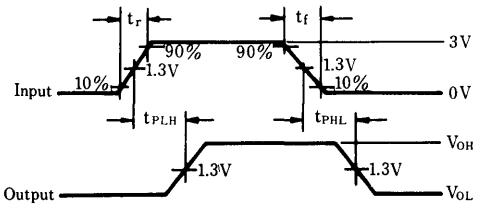
Parameter	Sym	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	$C_L=15pF$, $R_L=2k\Omega$		8	15	ns
	t_{PHL}			10	20	ns

※ Switching parameter measurement information

1. Measurement circuit



2. Waveforms



Notes
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161.

Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.

DN74LS22

Dual 4-input Positive NAND Gates (with Open Collector Outputs)

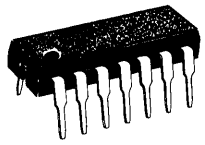
■ Description

DN74LS22 contains two 4-input positive isolation NAND gate circuits with open collector outputs.

■ Features

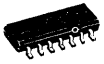
- "Wired" AND capability
- Low power consumption (P_d = 4mW typical)
- High speed (t_{pd} = 17ns typical)
- Wide operating temperature range (Ta = −20 to +75°C)

P-1



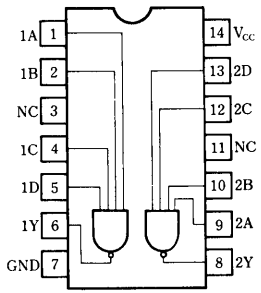
14-pin plastic DIL package

P-4



14-pin Panaflat package (SO-14D)

Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
HIGH level output voltage	V_{OH}			5.5	V
LOW level output voltage	I_{OL}			8	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OL1}	$V_{CC}=4.75V$, $V_{IH}=2V$	$I_{OL}=4mA$		0.25	0.4	V
	V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
	I_I	$V_{CC}=5.25V$, $V_I=7V$				0.1	mA
Output current	I_{OH}	$V_{CC}=4.75V$, $V_{IL}=0.8V$, $V_{OH}=5.5V$				100	μA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$, $I_I=-18mA$				−1.5	V
Supply current	I_{CCH}	$V_{CC}=5.25V$			0.4	0.8	mA
	I_{CCL}	$V_{CC}=5.25V$			1.2	2.2	mA

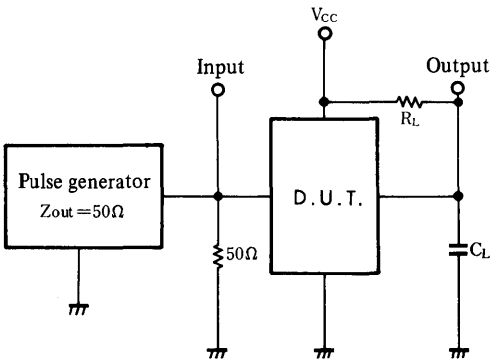
* When constant at V_{CC} = 5V, Ta = 25°C.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	$C_L=15pF$, $R_L=2k\Omega$		17	32	ns
	t_{PHL}			15	28	ns

※ Switching parameter measurement information

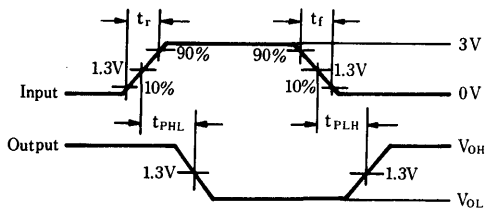
1. Measurement circuit



Notes

1. C_L includes probe and tool floating capacitance.

2. Waveforms



Notes

1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.

DN74LS26

Quad 2-input High-Voltage Interface Positive NAND Gates

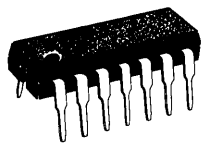
■ Description

DN74LS26 contains four 2-input positive isolation NAND buffer gate circuits.

■ Features

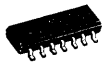
- "Wired" AND capability
- High output withstand voltage ($V_{OH} \leqq 15V$ maximum)
- Low power consumption (P_d = 8mW typical)
- High speed (t_{pd} = 16ns typical)
- Wide operating temperature range (Ta = −20 to +75°C)

P-1



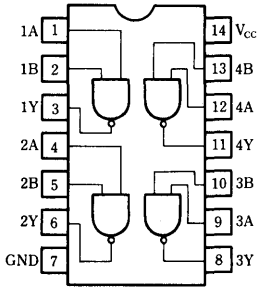
14-pin plastic DIL package

P-4



14-pin Panaflat package (SO-14D)

ピン配置図（上面図）



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
HIGH level output voltage	V_{OH}			15	V
LOW level output voltage	I_{OL}			8	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics (Ta = −20 ~ +75℃)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OL1}	V_{CC} = 4.75V, V_{IH} = 2V	I_{OL} = 4mA		0.25	0.4	V
	V_{OL2}		I_{OL} = 8mA		0.35	0.5	V
Input current	I_{IH}	V_{CC} = 5.25V, V_I = 2.7V				20	μA
	I_{IL}	V_{CC} = 5.25V, V_I = 0.4V				−0.4	mA
	I_I	V_{CC} = 5.25V, V_I = 7V				0.1	mA
Output current	I_{OH}	V_{CC} = 4.75V, V_{IL} = 0.8V	V_{OH} = 12V			50	μA
			V_{OH} = 15V			1	mA
入力クランプ電圧	V_{IK}	V_{CC} = 4.75V, I_I = −18mA				−1.5	V
Supply current	I_{CCH}	V_{CC} = 5.25V			0.8	1.6	mA
	I_{CCL}	V_{CC} = 5.25V			2.4	4.4	mA

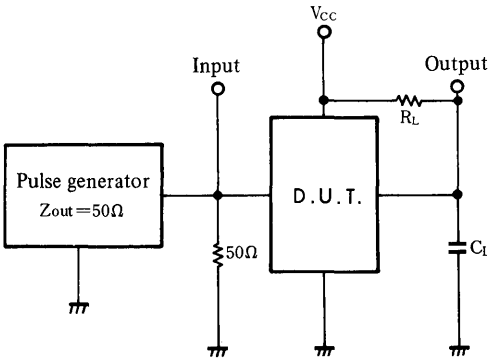
* When constant at V_{CC} = 5V, Ta = 25°C.

■ Switching characteristics (V_{CC} = 5V, Ta = 25℃)

Parameter	Sym	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	C_L = 15pF, R_L = 2kΩ		17	32	ns
	t_{PHL}			15	28	ns

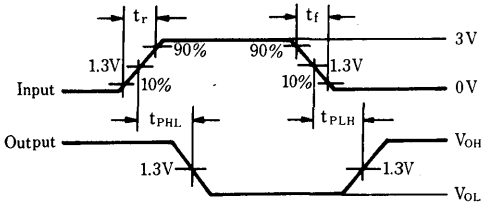
※ Switching parameter measurement information

1. Measurement circuit



Notes
1. C_L includes probe and tool floating capacitance.

2. Waveforms



Notes
1. Input waveform: $t_r \leqq 15$ns, $t_f \leqq 6$ns, PRR = 1MHz, duty cycle = 50%.

DN74LS27

Triple 3-input Positive NOR Gates

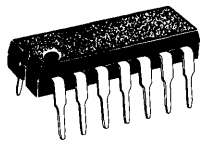
■ Description

DN74LS27 contains three 3-input positive isolation NOR gate circuits.

■ Features

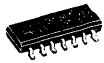
- Low power consumption (P_d = 13.5mW typical)
- High speed (t_{pd} = 10ns typical)
- Low output impedance
- Wide operating temperature range (Ta = −20 to +75°C)

P-1



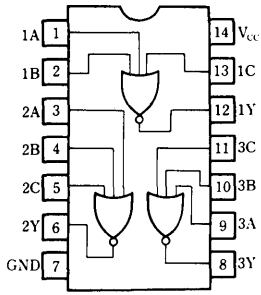
14-pin plastic DIL package

P-4



14-pin Panaflat package (SO-14D)

Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−400	μA
	I_{OL}			8	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IL}=0.8V$ $I_{OH}=-400\mu A$		2.7	3.4		V
	V_{OL1}	$V_{CC}=4.75V$ $V_{IH}=2V$	$I_{OL}=4mA$		0.25	0.4	V
	V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				20	μA
	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.4	mA
	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.1	mA
Output short circuit current**	I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−100	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current	I_{CCH}	$V_{CC}=5.25V$,			2.0	4.0	mA
	I_{CCL}	$V_{CC}=5.25V$,			3.4	6.8	mA

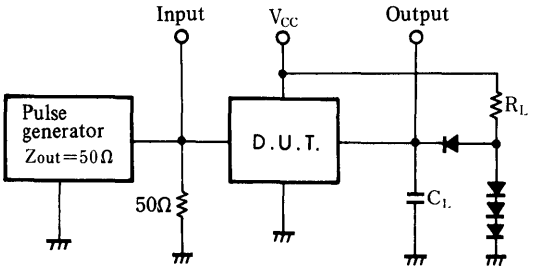
* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	$C_L=15pF$, $R_L=2k\Omega$		10	15	ns
	t_{PHL}			10	15	ns

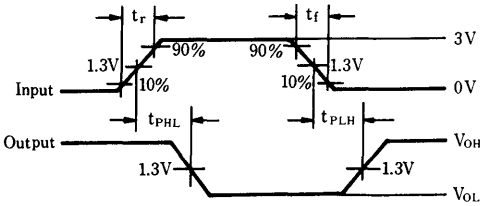
※ Switching parameter measurement information

1. Measurement circuit



Notes
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161.

2. Waveforms



Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.

DN74LS28

Quad 2-input Positive NOR Buffers

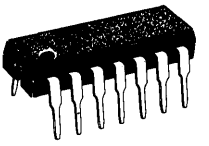
■ Description

DN 74LS28 contains four 2-input positive isolation NOR buffer gate circuits.

■ Features

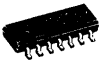
- High fan-out (I_{OL} = 24mA, I_{OH} = −1.2mA)
- Low power consumption (P_d = 22mW typical)
- High speed (t_{pd} = 12ns typical)
- Wide operating temperature range (Ta = −20 to +75°C)

P-1



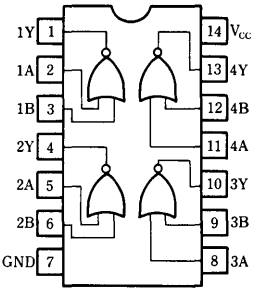
14-pin plastic DIL package

P-4



14-pin Panaflat package (SO-14D)

Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−1.2	mA
	I_{OL}			24	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions	Min	Typ*	Max	Unit
Input voltage	V_{IH}		2.0			V
	V_{IL}				0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$	2.7	3.4		V
	V_{OL1}	$V_{CC}=4.75V$, $V_{IH}=2V$, $I_{OL}=4mA$		0.25	0.4	V
	V_{OL2}	$V_{CC}=4.75V$, $V_{IH}=2V$, $8mA$		0.35	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$			20	μA
	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$			−0.4	mA
	I_I	$V_{CC}=5.25V$, $V_I=7V$			0.1	mA
Output short circuit current**	I_{OS}	$V_{CC}=5.25V$, $V_O=0V$	−15		−100	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$, $I_I=-18mA$			−1.5	V
Supply current	I_{CCH}	$V_{CC}=5.25V$,		1.8	3.6	mA
	I_{CCL}	$V_{CC}=5.25V$,		6.9	13.8	mA

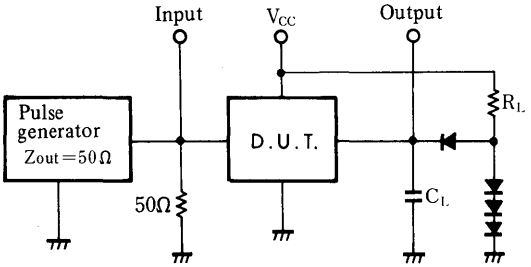
* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	$C_L=15pF$, $R_L=2k\Omega$		12	24	ns
	t_{PHL}			12	24	ns

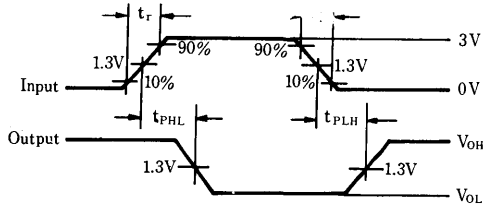
※ Switching parameter measurement information

1. Measurement circuit



Notes
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161.

2. Waveforms



Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.

DN74LS30

8-input Positive NAND Gates

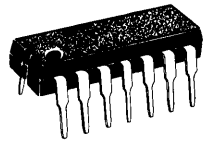
■ Description

DN74LS30 contains one 8-input positive isolation NAND gate circuit.

■ Features

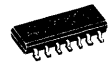
- Low power consumption (P_d = 2.5mW typical)
- High speed (t_{pd} = 11ns typical)
- Low output impedance
- Wide operating temperature range (Ta = –20 to +75°C)

P-1



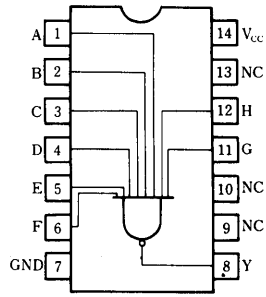
14-pin plastic DIL package

P-4



14-pin Panaflat package (SO-14D)

Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−400	μA
	I_{OL}			8	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IL}=0.8V$ $I_{OH}=-400\mu A$		2.7	3.4		V
	V_{OL1}	$V_{CC}=4.75V$ $V_{IH}=2V$	$I_{OL}=4mA$		0.25	0.4	V
	V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				20	μA
	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.4	mA
	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.1	mA
Output short circuit current**	I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−100	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current	I_{CCH}	$V_{CC}=5.25V$,			0.35	0.5	mA
	I_{CCL}	$V_{CC}=5.25V$,			0.6	1.1	mA

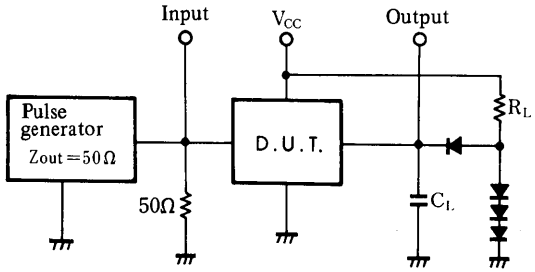
* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	$C_L=15pF$, $R_L=2k\Omega$		8	15	ns
	t_{PHL}			13	20	ns

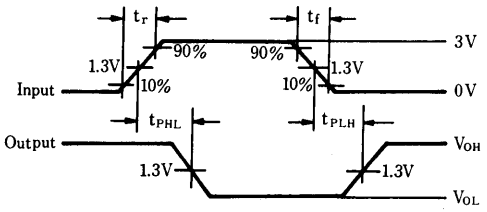
※ Switching parameter measurement information

1. Measurement circuit



Notes
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161.

2. Waveforms



Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.

DN74LS32

Quad 2-input Positive OR Gates

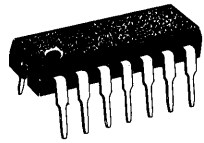
■ Description

DN74LS32 contains four 2-input positive isolation OR gate circuits.

■ Features

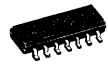
- Low power consumption (P_d = 20mW typical)
- High speed (t_{pd} = 14ns typical)
- Low output impedance
- Wide operating temperature range (Ta = −20 to +75°C)

P-1



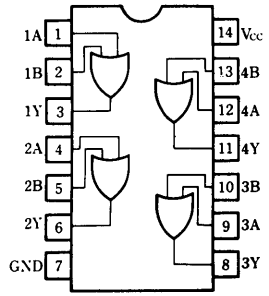
14-pin plastic DIL package

P-4



14-pin Panaflat package (SO-14D)

Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−400	μA
	I_{OL}			8	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$ $I_{OH}=-400\mu A$		2.7	3.4		V
	V_{OL1}	$V_{CC}=4.75V$ $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
	V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				20	μA
	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.4	mA
	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.1	mA
Output short circuit current**	I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−100	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current	I_{CCH}	$V_{CC}=5.25V$,			3.1	6.2	mA
	I_{CCL}	$V_{CC}=5.25V$,			4.9	9.8	mA

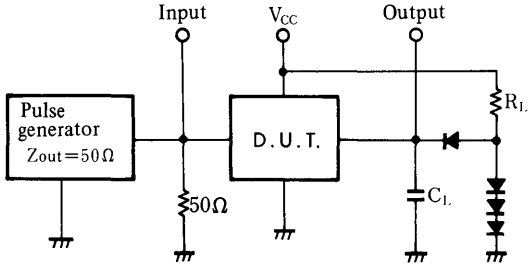
* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	$C_L=15pF$, $R_L=2k\Omega$		14	22	ns
	t_{PHL}			14	22	ns

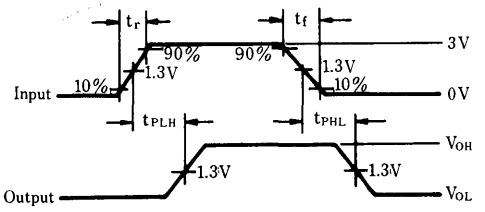
※ Switching parameter measurement information

1. Measurement circuit



Notes
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161.

2. Waveforms



Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.

DN74LS33

Quad 2-input Positive NOR Buffers (with Open Collector Outputs)

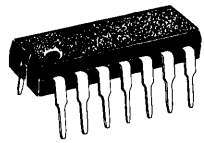
■ Description

DN74LS33 contains four 2-input positive isolation NOR buffer gates with open collector outputs.

■ Features

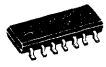
- "Wired" AND capability
- High fan-out (I_{OL} = 24mA maximum)
- Low power consumption (P_d = 20mW typical)
- High speed (t_{pd} = 19ns typical)
- Wide operating temperature range (Ta = −20 to +75°C)

P-1



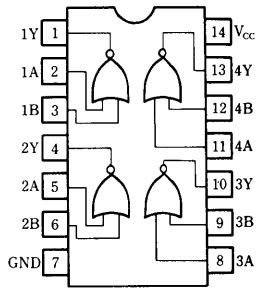
14-pin plastic DIL package

P-4



14-pin Panaflat package (SO-14D)

Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
HIGH level output voltage	V_{OH}			5.5	V
LOW level output voltage	I_{OL}			24	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OL1}	$V_{CC}=4.75V$, $V_{IH}=2V$	$I_{OL}=4mA$		0.25	0.4	V
	V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
	I_I	$V_{CC}=5.25V$, $V_I=7V$				0.1	mA
Output current	I_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{OH}=5.5V$				250	μA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$, $I_I=-18mA$				−1.5	V
Supply current	I_{CCH}	$V_{CC}=5.25V$			1.8	3.6	mA
	I_{CCL}	$V_{CC}=5.25V$			6.9	13.8	mA

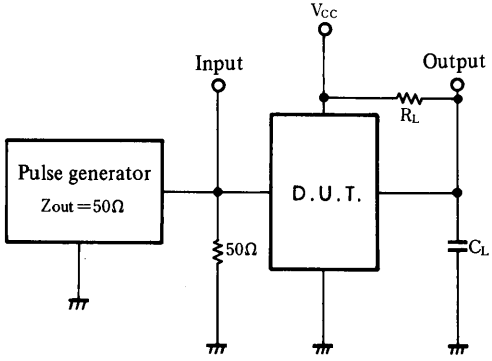
* When constant at V_{CC} = 5V, Ta = 25°C.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	$C_L=45pF$, $R_L=667\Omega$		20	32	ns
	t_{PHL}			18	28	ns

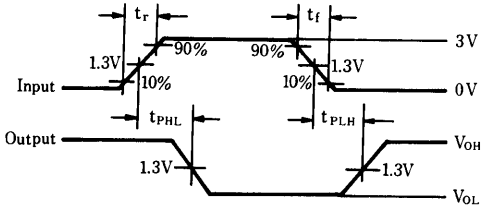
※ Switching parameter measurement information

1. Measurement circuit



Notes
1. C_L includes probe and tool floating capacitance.

2. Waveforms



Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.

DN74LS37

Quad 2-input Positive NAND Buffers

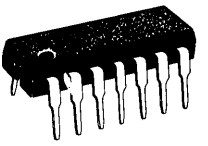
■ Description

DN74LS37 contains four 2-input positive isolation NAND buffer gate circuits.

■ Features

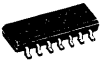
- High fan-out (I_{OL} = 24mA, I_{OH} = −1.2mA)
- Low power consumption (P_d = 17.5mW typical)
- High speed (t_{pd} = 12ns typical)
- Low output impedance
- Wide operating temperature range (Ta = −20 to +75°C)

P-1



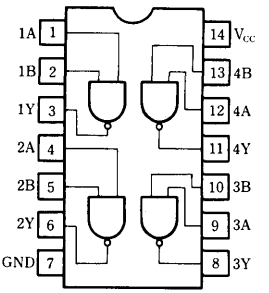
14-pin plastic DIL package

P-4



14-pin Panaflat package (SO-14D)

Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
HIGH level output voltage	I_{OH}			1200	μA
LOW level output voltage	I_{OL}			24	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IL}=0.8V$ $I_{OH}=-1.2mA$		2.7	3.4		V
	V_{OL1}	$V_{CC}=4.75V$ $V_{IH}=2V$	$I_{OL}=12mA$		0.25	0.4	V
	V_{OL2}		$I_{OL}=24mA$		0.35	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				20	μA
	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.4	mA
	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.1	mA
Output short circuit current**	I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−100	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current	I_{CCH}	$V_{CC}=5.25V$,			0.9	2.0	mA
	I_{CCL}	$V_{CC}=5.25V$,			6	12	mA

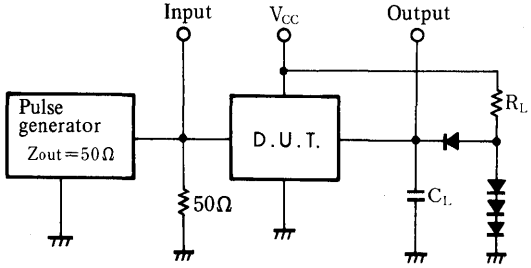
* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	$C_L=45pF$, $R_L=667\Omega$		12	24	ns
	t_{PHL}			12	24	ns

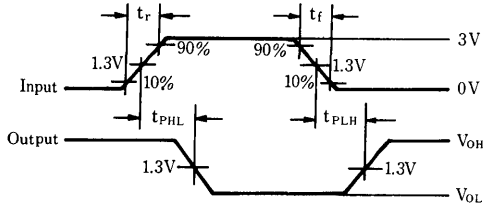
※ Switching parameter measurement information

1. Measurement circuit



Notes
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161.

2. Waveforms



Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.

DN74LS38

Quad 2-input Positive NAND Buffers (with Open Collector Outputs)

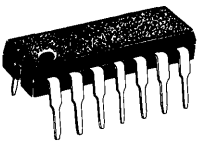
■ Description

DN74LS38 contains four 2-input positive isolation NAND buffer gate circuits with open collector outputs.

■ Features

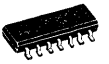
- "Wired" AND capability
- High fan-out (I_{OL} = 24mA maximum)
- Low power consumption (P_d = 17.5mW typical)
- High speed (t_{pd} = 19ns typical)
- Wide operating temperature range (Ta = −20 to +75°C)

P-1



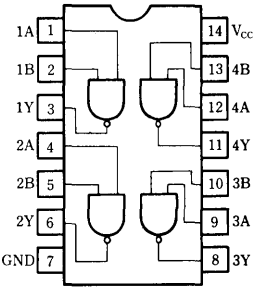
14-pin plastic DIL package

P-4



14-pin Panaflat package (SO-14D)

Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
HIGH level output voltage	V_{OH}			5.5	V
LOW level output voltage	I_{OL}			24	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics (Ta = −20 ~ +75℃)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OL1}	V_{CC} = 4.75V, V_{IH} = 2V	I_{OL} = 12mA		0.25	0.4	V
	V_{OL2}		I_{OL} = 24mA		0.35	0.5	V
Input current	I_{IH}	V_{CC} = 5.25V, V_I = 2.7V				20	μA
	I_{IL}	V_{CC} = 5.25V, V_I = 0.4V				−0.4	mA
	I_I	V_{CC} = 5.25V, V_I = 7V				0.1	mA
Output current	I_{OH}	V_{CC} = 4.75V, V_I = 0.8V, V_{OH} = 5.5V				250	μA
Input clamp voltage	V_{IK}	V_{CC} = 4.75V, I_I = −18mA				−1.5	V
Supply current	I_{CCH}	V_{CC} = 5.25V			0.9	2.0	mA
	I_{CCL}	V_{CC} = 5.25V			6	12	mA

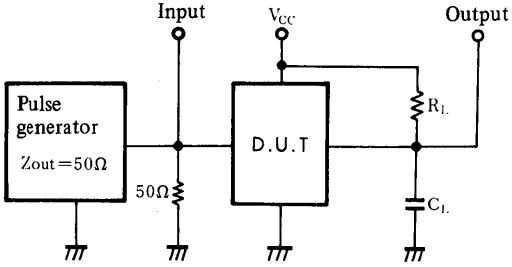
* When constant at V_{CC} = 5V, Ta = 25°C.

■ Switching characteristics (V_{CC} = 5V, Ta = 25℃)

Parameter	Sym	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	C_L = 45pF, R_L = 667Ω		20	32	ns
	t_{PHL}			18	28	ns

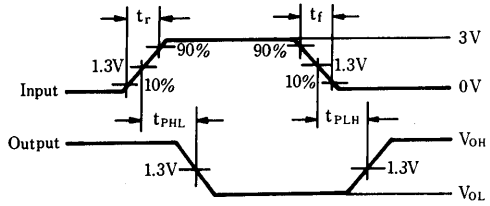
※ Switching parameter measurement information

1. Measurement circuit



Notes
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161 or equivalent.

2. Waveforms



Notes
1. Input waveform: $t_r \leqq 15$ns, $t_f \leqq 6$ns, PRR = 1MHz, duty cycle = 50%.

DN74LS40

Dual 4-input Positive NAND Buffers

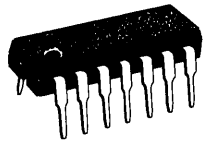
■ Description

DN74LS40 contains two 4-input positive isolation NAND buffer gate circuits.

■ Features

- High fan-out (I_{OL} = 24mA, I_{OH} = −1.2mA)
- Low power consumption (P_d = 9mW typical)
- High speed (t_{pd} = 12ns typical)
- Wide operating temperature range (Ta = −20 to +75°C)

P-1

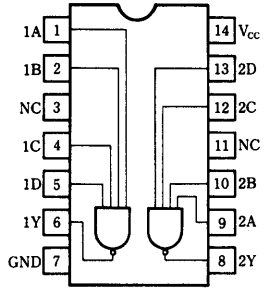


14-pin plastic DIL package

P-4

14-pin Panaflat package (SO-14D)

Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			1200	μA
	I_{OL}			24	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IL}=0.8V$, $I_{OH}=-1.2mA$		2.7	3.4		V
	V_{OL1}	$V_{CC}=4.75V$, $V_{IH}=2V$	$I_{OL}=12mA$		0.25	0.4	V
	V_{OL2}		$I_{OL}=24mA$		0.35	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
	I_I	$V_{CC}=5.25V$, $V_I=7V$				0.1	mA
Output short circuit current**	I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−100	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$, $I_I=-18mA$				−1.5	V
Supply current	I_{CCH}	$V_{CC}=5.25V$,			0.45	1.0	mA
	I_{CCL}	$V_{CC}=5.25V$,			3	6	mA

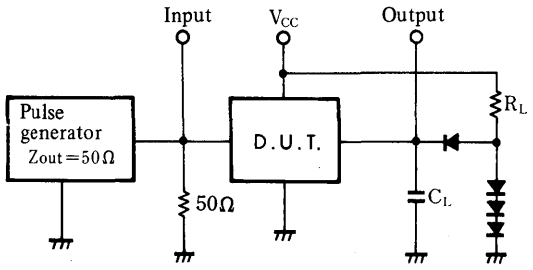
* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	$C_L=45pF$, $R_L=667Ω$		12	24	ns
	t_{PHL}			12	24	ns

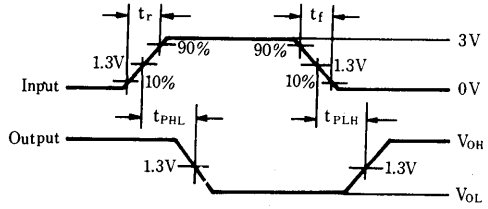
※ Switching parameter measurement information

1. Measurement circuit



Notes
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161 or equivalent.

2. Waveforms



Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%

DN74LS42

BCD to Decimal Decoders

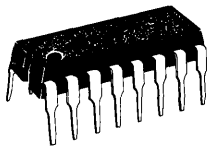
■ Description

DN74LS42 is a binary-coded decimal to decimal decoder.

■ Features

- During invalid input, all inputs become HIGH
- Also can be used as 3-bit binary to octal decoder
- Wide operating temperature range (Ta = −20 to +75°C)

P-2

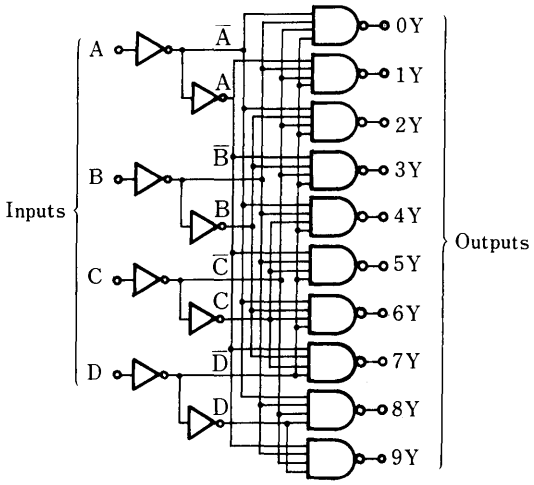


16-pin plastic DIL package

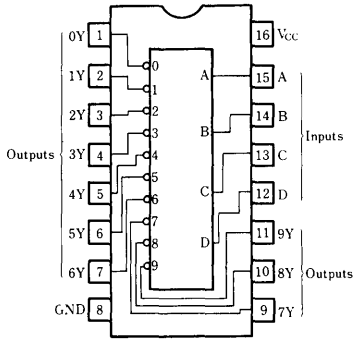
P-5

16-pin Panaflat package (SO-16D)

■ Logic diagram



Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−400	μA
	I_{OL}			8	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$ $V_{IH}=2V$ $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	3.4		V
	V_{OL1}	$V_{CC}=4.75V$ $V_{IH}=2V$ $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
	V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				20	μA
	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.4	mA
	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.1	mA
Output short circuit current**	I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−100	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current***	I_{CC}	$I_{CC}=5.25V$			7	13	mA

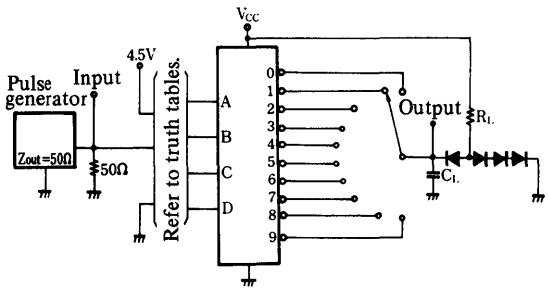
* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.
*** Measured with all outputs open and all inputs grounded.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter		Sym	Test conditions	Min	Typ	Max	Unit
Propagation delay time	2 stage	t_{PLH}	$C_L=15pF$ $R_L=2k\Omega$		15	25	ns
	3 stage				20	30	ns
	2 stage	t_{PHL}			15	25	ns
	3 stage				20	30	ns

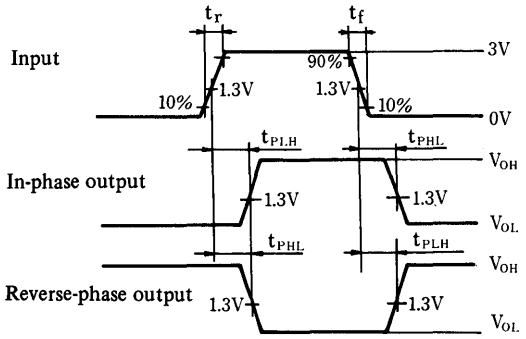
※ Switching parameter measurement information

1. Measurement circuit



Notes
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161 or equivalent.

2. Waveforms



Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.

■ Truth tables

NO.	BCD Inputs				Decimal Outputs									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

Notes

1. H: HIGH voltage level.
2. L: LOW voltage level.

DN74LS51

2-wide 3-input, 2-wide 2-input AND-OR-INVERT Gates

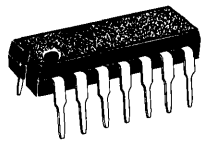
■ Description

DN74LS51 contains two 2-input and two 3-input AND-OR-INVERT gates.

■ Features

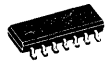
- Low power consumption (P_d = 5.5mW typical)
- High speed (t_{pd} = 12ns typical)
- Low output impedance
- Wide operating temperature range (Ta = −20 to +75°C)

P-1



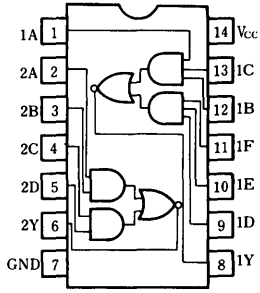
14-pin plastic DIL package

P-4



14-pin Panaflat package (SO-14D)

Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−400	μA
	I_{OL}			8	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	3.4		V
	V_{OL1}	$V_{CC}=4.75V$, $V_{IH}=2V$	$I_{OL}=4mA$		0.25	0.4	V
	V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
	I_I	$V_{CC}=5.25V$, $V_I=7V$				0.1	mA
Output short circuit current**	I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−100	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$, $I_I=-18mA$				−1.5	V
Supply current	I_{CCH}	$V_{CC}=5.25V$,			0.8	1.6	mA
	I_{CCL}	$V_{CC}=5.25V$,			1.4	2.8	mA

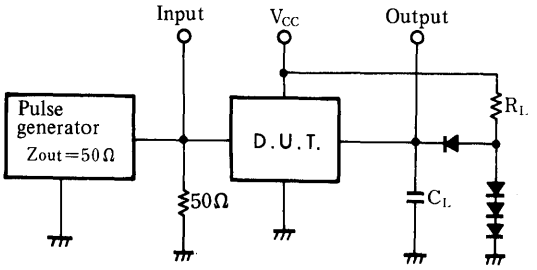
* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	$C_L=15pF$, $R_L=2k\Omega$		12	20	ns
	t_{PHL}			12.5	20	ns

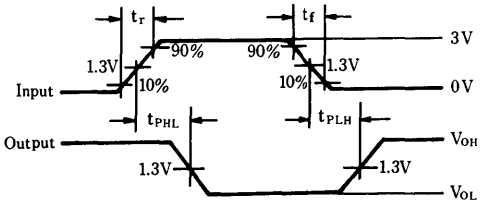
※ Switching parameter measurement information

1. Measurement circuit



Notes
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161 or equivalent.

2. Waveforms



Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.

DN74LS54

4-wide AND-OR-INVERT Gates

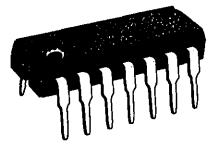
■ Description

DN74LS54 contains four 2-input and four 3-input AND-OR-INVERT gates.

■ Features

- Low power consumption (P_d = 4.5mW typical)
- High speed (t_{pd} = 12ns)
- Low output impedance
- Wide operating temperature range (Ta = –20 to +75°C)

P-1

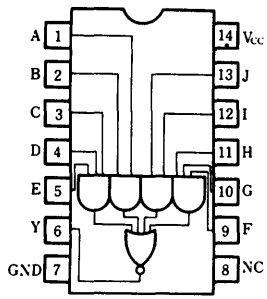


14-pin plastic DIL package

P-4

14-pin Panaflat package (SO-14D)

Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			–400	μA
	I_{OL}			8	mA
Operating temperature range	Topr	–20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IL}=0.8V$ $I_{OH}=-400\mu A$		2.7	3.4		V
	V_{OL1}	$V_{CC}=4.75V$ $V_{IH}=2V$	$I_{OL}=4mA$		0.25	0.4	V
	V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				20	μA
	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.4	mA
	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.1	mA
Output short circuit current**	I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−100	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current	I_{CCH}	$V_{CC}=5.25V$,			0.8	1.6	mA
	I_{CCL}	$V_{CC}=5.25V$,			1.0	2.0	mA

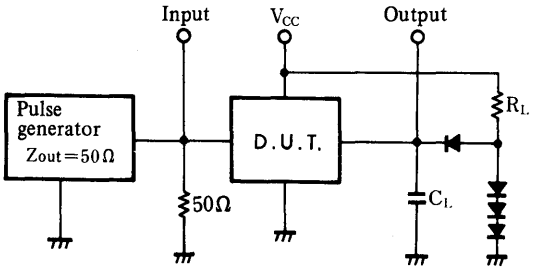
* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	$C_L=15pF$, $R_L=2k\Omega$		12	20	ns
	t_{PHL}			12.5	20	ns

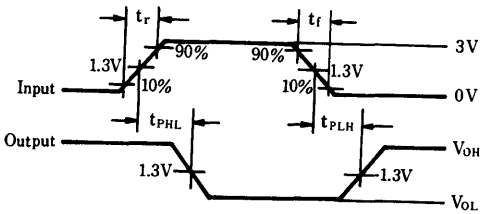
※ Switching parameter measurement information

1. Measurement circuit



Notes
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161 or equivalent.

2. Waveforms



Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.

DN74LS55

2-wide 4-input AND-OR-INVERT Gates

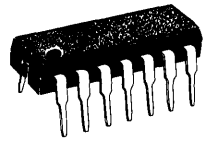
■ Description

DN74LS55 contains two 4-input AND-OR-INVERT gates.

■ Features

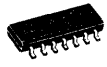
- Low power consumption (P_d = 2.75mW typical)
- High speed (t_{pd} = 12ns typical)
- Low output impedance
- Wide operating temperature range (Ta = −20 to +75°C)

P-1



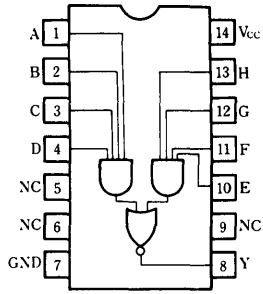
14-pin plastic DIL package

P-4



14-pin Panaflat package (SO-14D)

Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−400	μA
	I_{OL}			8	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IL}=0.8V$ $I_{OH}=-400\mu A$		2.7	3.4		V
	V_{OL1}	$V_{CC}=4.75V$ $V_{IH}=2V$	$I_{OL}=4mA$		0.25	0.4	V
	V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				20	μA
	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.4	mA
	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.1	mA
Output short circuit current**	I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−100	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current	I_{CCH}	$V_{CC}=5.25V$			0.4	0.8	mA
	I_{CCL}	$V_{CC}=5.25V$			0.7	1.3	mA

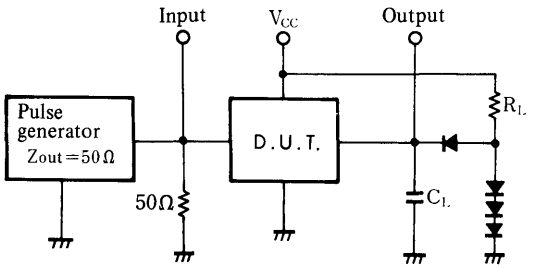
* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	$C_L=15pF$, $R_L=2k\Omega$		12	20	ns
	t_{PHL}			12.5	20	ns

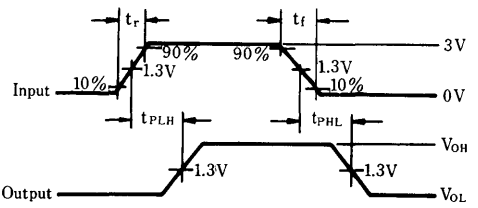
※ Switching parameter measurement information

1. Measurement circuit



Notes
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161 or equivalent.

2. Waveforms



Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.

DN74LS73

Dual J-K Flip-Flops (with Reset)

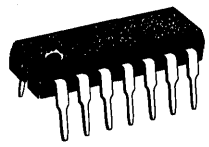
■ Description

DN74LS73 contains two negative-edge triggered J-K flip-flop circuit, each with independent clock CP, J, K, and direct-coupled reset input terminals.

■ Features

- Negative-edge trigger
- Independent input terminals for each flip flop
- Direct-coupled reset input
- Q and $\overline{Q}$ outputs
- Wide operating temperature range (Ta = −20 to +75°C)

P-1

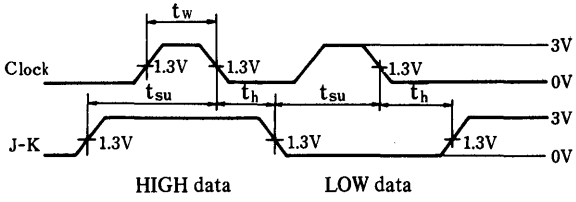


14-pin plastic DIL package

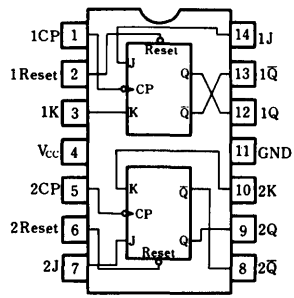
P-4

14-pin Panaflat package (SO-14D)

■ Timing definition



Pin configuration (top view)



■ Recommended operating conditions

Parameter		Sym	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}			−400	μA
		I_{OL}			8	mA
Operating temperature range		Topr	−20	25	75	℃
Clock frequency		f_{clock}	0		30	MHz
Pulse width	Clock High	t_w	20			ns
	Reset Low		25			ns
Set-up time	HIGH data	t_{su}	20 ↓			ns
	LOW data		20 ↓			ns
Hold time		t_h	0 ↓			ns

Notes 1. ↓: Indicates fall edge of standard clock pulse.

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter		Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Output voltage		V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$ $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	3.4		V
		V_{OL1}	$V_{CC}=4.75V$ $V_{IH}=2V$ $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
		V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	J, K	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				20	μA
	Reset						60	μA
	Clock						80	μA
	J, K	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.4	mA
	Reset						−0.8	mA
	Clock						−0.8	mA
	J, K	I_I	$V_{CC}=5.25V$				0.1	mA
	Reset						0.3	mA
	Clock						0.4	mA
Output short circuit current**		I_{OS}	$V_{CC}=5.25$, $V_O=0V$		−15		−100	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$, $I_I=-18mA$				−1.5	V
Supply current***		I_{CC}	$V_{CC}=5.25V$			4	8	mA

* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.
*** Measured with all outputs open, Q and $\overline{Q}$ outputs alternately HIGH, and clock inputs grounded.

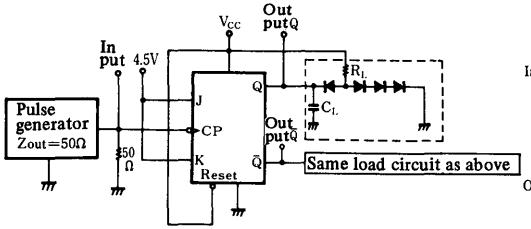
■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Maximum clock frequency	f_{max}			$C_L=15pF$ $R_L=2K\Omega$	30	45		MHz
Propagation delay time	t_{PLH}	Reset clock	Q, $\overline{Q}$			11	20	ns
	t_{PHL}					15	30	ns

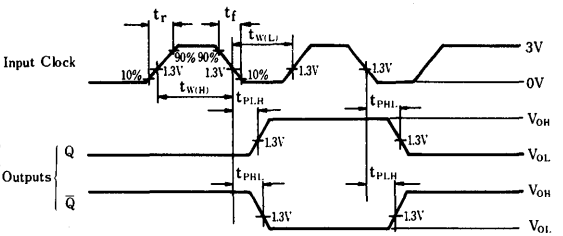
※ Switching parameter measurement information

〔1〕 f_{max}, t_{PLH}, t_{PHL} (Clock → Q, $\overline{Q}$)

1. Measurement circuit



2. Waveforms

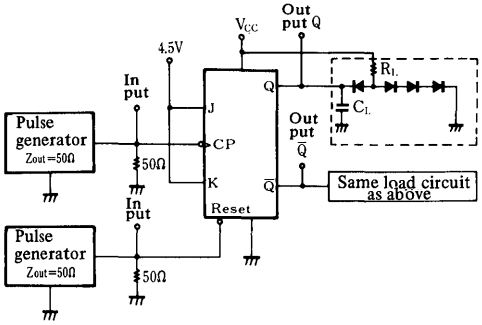


Notes
1. Clock input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR=1MHz, duty cycle 50%
2. When measuring f_{max}, t_r and $t_f \leqq 2.5ns$.

1. Measurement made for each flip flop.
2. C_L includes probe and tool floating capacitance.
3. Diodes are all MA161 or equivalent.

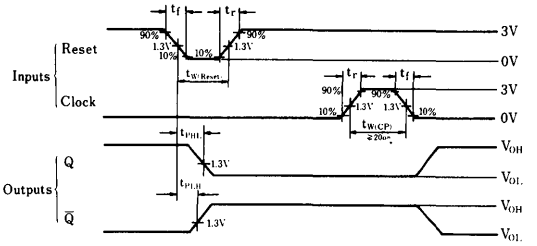
[2] t_{PHL}(Reset → Q), t_{PLH} (Reset → $\overline{Q}$)

1. Measurement circuit



1. Measurement made for each flip flop.
2. C_L includes probe and tool floating capacitance.
3. Diodes are all MA161 or equivalent.

2. Waveforms



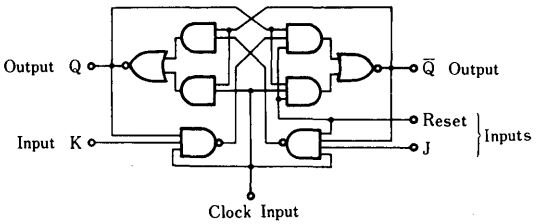
Notes
1. Set and clock waveforms: $t_r \leqq 15$ns, $t_f \leqq 6$ns, PRR = 1MHz.

■ Truth tables

Inputs				Outputs	
Reset	Clock	J	K	Q	$\overline{Q}$
L	×	×	×	L	H
H	↓	L	L	Q_0	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	Toggle	
H	H	×	×	Q_0	$\overline{Q}_0$

Notes
1. H: HIGH voltage level.
2. L: LOW voltage level.
3. ↓: Change from HIGH to LOW.
4. X: Either HIGH or LOW; doesn't matter.
5. Q_0: Q level prior to determination of input condition shown in table.
6. $\overline{Q}_0$: $\overline{Q}$ level prior to determination of input condition shown intable.
7. Toggle: With ↓ change, outputs become compliment of previous condition.

■ Logic diagram (1/2)



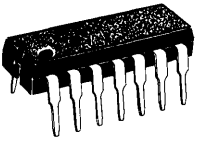
DN74LS74A

Dual D-type Positive Edge-triggered Flip-Flops (with Set and Reset)

■ Description

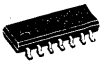
DN74LS74A contains two positive-edge triggered D-type flip-flop circuits, each with independent clock-CP data-D, and direct-coupled set and reset input terminals.

P-1



14-pin plastic DIL package

P-4

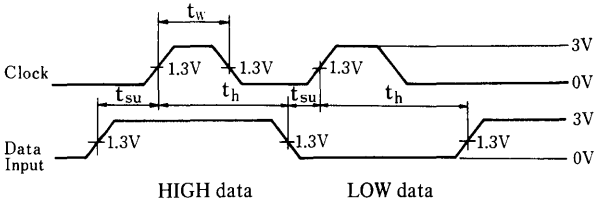


14-pin Panaflat package (SO-14D)

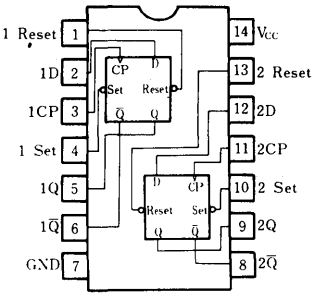
■ Features

- Each flip flop can be used independently
- Direct-coupled set and reset inputs
- Positive-edge trigger
- Q and $\overline{Q}$ outputs
- Wide operating temperature range (Ta = −20 to +75°C)

■ Timing definition



Pin configuration (top view)



■ Recommended operating conditions

Parameter		Sym	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}			−400	μA
		I_{OL}			8	mA
Operating temperature range		Topr	−20	25	75	℃
Clock frequency		f_{clock}	0		25	MHz
Pulse width	Clock High	t_w	25			ns
	Set or reset Low		25			ns
Set-up time	HIGH data	t_{su}	20 ↑			ns
	LOW data		20 ↑			ns
Hold time		t_h	5 ↑			ns

Notes 1. ↓: Indicates fall edge of standard clock pulse.

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter		Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Output voltage		V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$,	$I_{OH}=-400\mu A$	2.7	3.4		V
		V_{OL1}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
		V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	D	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
	Reset						40	μA
	Set						40	μA
	Clock						20	μA
	D	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
	Reset						−0.8	mA
	Set						−0.8	mA
	Clock						−0.4	mA
	D	I_I	$V_{CC}=5.25V$, $V_I=7V$				0.1	mA
	Reset						0.2	mA
	Set						0.2	mA
	Clock						0.1	mA
Output short circuit current**		I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−100	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$, $I_I=-18mA$				−1.5	V
Supply current***		I_{CC}	$V_{CC}=5.25V$			4	8	mA

* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.
*** Measured with all outputs open, Q and $\overline{Q}$ outputs alternately HIGH, and clock inputs grounded.

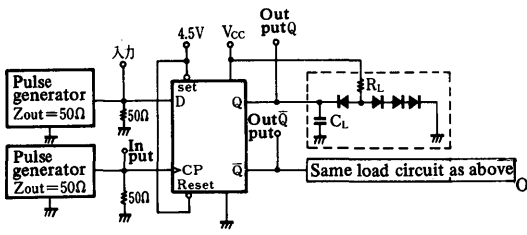
■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Maximum clock frequency	f_{max}			$C_L=15pF$, $R_L=2k\Omega$	25	33		MHz
Propagation delay time	t_{PLH}	Clock, Reset or set	Q, $\overline{Q}$			13	25	ns
	t_{PHL}					25	40	ns

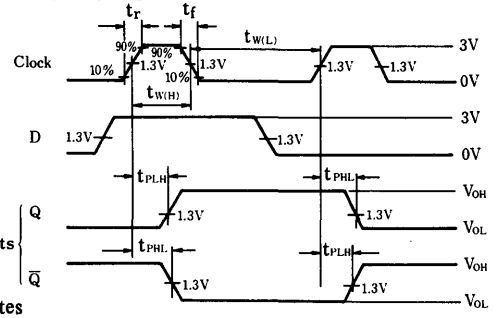
※ Switching parameter measurement information

〔1〕 f_{max}, t_{PLH}, t_{PHL} (Clock → Q, $\overline{Q}$)

1. Measurement circuit



2. Waveforms



Notes

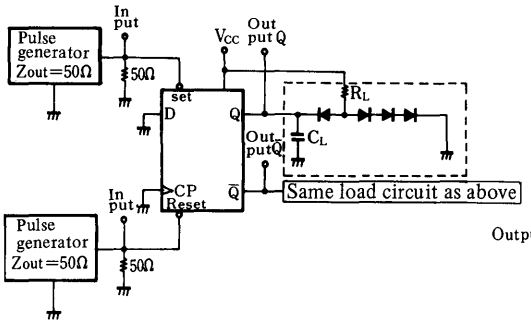
1. Measurement made for each flip flop.
2. C_L includes probe and tool floating capacitance.
3. Diodes are all MA161 or equivalent.

Notes

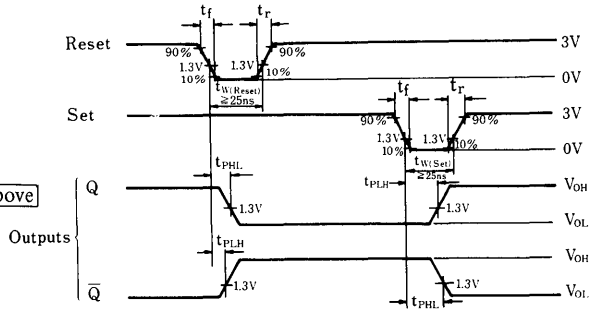
1. Clock input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR=1MHz, duty cycle 50%
2. When measuring f_{max}, t_r and $t_f \leqq 2.5ns$.

〔2〕 t_{PHL}, t_{PLH} (Reset or Set → Q, $\overline{Q}$)

1. Measurement circuit



2. Waveforms



Notes
1. Measurement made for each flip flop.
2. C_L includes probe and tool floating capacitance.
3. Diodes are all MA161.

Notes
1. Reset, Set Input waveform: $t_r \leqq 15$ ns, $t_f \leqq 6$ ns, PRR = 1MHz

■ Truth tables

Inputs				Outputs	
Set	Reset	Clock	D	Q	$\overline{Q}$
L	H	×	×	H	L
H	L	×	×	L	H
L	L	×	×	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	×	Q_0	$\overline{Q}_0$

Notes
1. H: HIGH voltage level.
2. L: LOW voltage level.
3. ↑: Change from LOW to HIGH.
4. X: Either HIGH or LOW; doesn't matter.
5. Q_0: Q level prior to determination of input condition shown in table.
6. $\overline{Q}_0$: $\overline{Q}$ level prior to determination of input condition shown in table.
7. H*: When set and reset are LOW, Q and $\overline{Q}$ are HIGH; however, when set and reset simultaneously change to HIGH, requirements of Q and $\overline{Q}$ cannot be predicted.

DN74LS75

4-bit Bistable Latches

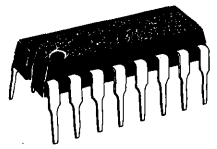
■ Description

DN74LS75 contains four bistable latches with Q and $\overline{Q}$ output terminals.

■ Features

- Common enable inputs for each two circuits
- Q and $\overline{Q}$ outputs
- Wide operating temperature range (Ta = –20 to +75°C)

P-2



16-pin plastic DIL package

P-5

16-pin Panaflat package (SO-16D)

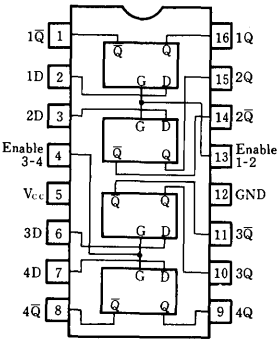
■ Truth tables

Inputs		Outputs	
D	G	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
×	L	Q_0	$\overline{Q}_0$

Notes

1. H: HIGH voltage level.
2. L: LOW voltage level.
3. X: Either HIGH or LOW; doesn't matter.
4. Q_0: Q level prior to determination of input condition shown in table.
5. $\overline{Q}_0$: $\overline{Q}$ level prior to determination of input condition shown in table.

Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			–400	μA
	I_{OL}			8	mA
Operating temperature range	Topr	–20	25	75	℃
Pulse width	t_w	20			ns
Set-up time	t_{su}	20			ns
Hold time	t_h	5			ns

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter		Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Output voltage		V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$ $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	3.4		V
		V_{OL1}	$V_{CC}=4.75V$ $V_{IH}=2V$ $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
		V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	D input	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				20	μA
	G input						80	μA
	D input	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.4	mA
	G input						−1.6	mA
	D input	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.1	mA
	G input						0.4	mA
Output short circuit current**		I_{OS}	$V_{CC}=5.25V$ $V_O=0V$		−15		−100	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current***		I_{CC}	$V_{CC}=5.25V$			6.3	12	mA

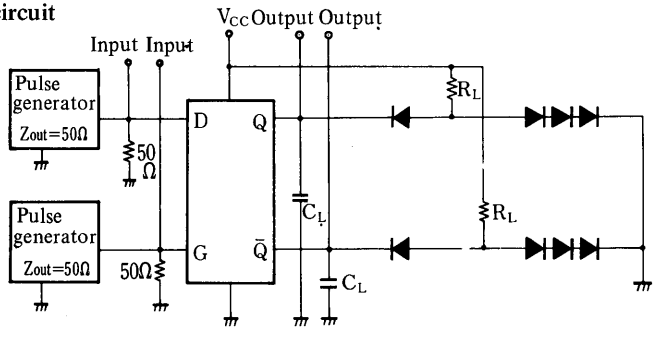
* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.
*** I_{CC} is measured with all outputs open and all inputs grounded.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	D	Q	$C_L=15pF$ $R_L=2k\Omega$		15	27	ns
	t_{PHL}					9	17	ns
	t_{PLH}	D	$\overline{Q}$			12	20	ns
	t_{PHL}					7	15	ns
	t_{PLH}	G	Q			15	27	ns
	t_{PHL}					14	25	ns
	t_{PLH}	G	$\overline{Q}$			16	30	ns
	t_{PHL}					7	15	ns

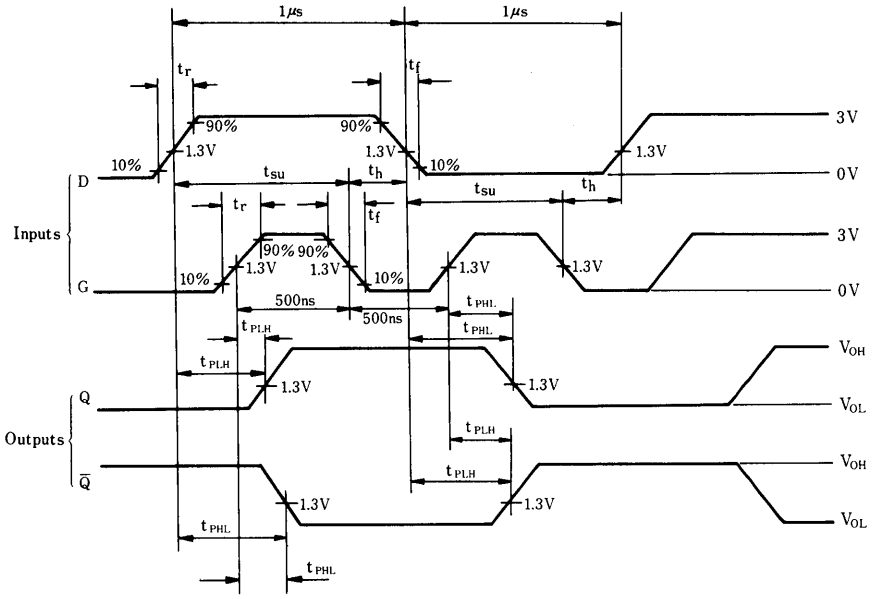
※ Switching parameter measurement information

1. Measurement circuit



Notes
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161.

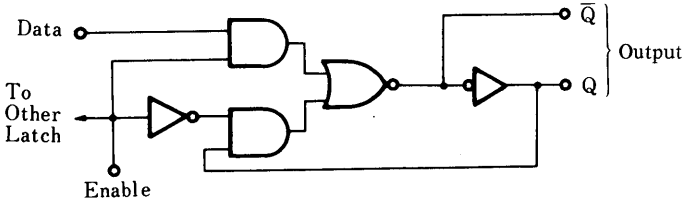
2. Waveforms



Notes

1. Input waveform: D input PRR = 500kHz, G input PRR = 1MHz, $t_r \leqq 10$ns, $t_f \leqq 10$ns.
2. When measuring from D input, G input is maintained at 3V.

■ Logic diagram (1/4)



DN74LS76

Dual J-K Flip-Flops (with Set and Reset)

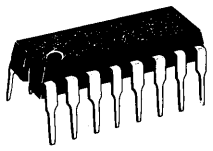
■ Description

DN74LS76 contains two negative-edge triggered J-K flip-flop circuits, each with independent clock-CP, J, K, and direct-coupled set and reset input terminals.

■ Features

- Negative-edge trigger
- Independent input and output terminals for each flip flop
- Direct-coupled set and reset
- Q and $\overline{Q}$ outputs
- Wide operating temperature range (Ta = −20 to +75°C)

P-2

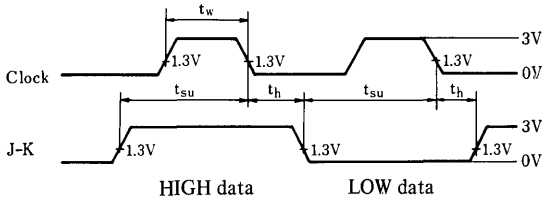


16-pin plastic DIL package

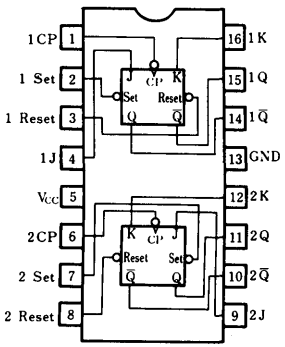
P-5

16-pin Panaflat package (SO-16D)

■ Timing definition



Pin configuration (top view)



■ Recommended operating conditions

Parameter		Sym	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}			−400	μA
		I_{OL}			8	mA
Operating temperature range		Topr	−20	25	75	℃
Clock frequency		f_{clock}	0		30	MHz
Pulse width	Clock High	t_w	20			ns
	Reset Low		25			ns
Set-up time	HIGH data	t_{su}	20 ↓			ns
	LOW data		20 ↓			ns
Hold time		t_h	0 ↓			ns

Notes 1. ↓: Indicates fall edge of standard clock pulse.

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter		Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Output voltage		V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$ $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	3.4		V
		V_{OL1}	$V_{CC}=4.75V$ $V_{IH}=2V$ $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
		V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	J-K	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				20	μA
	Reset						60	μA
	Set						60	μA
	Clock						80	μA
	J-K	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.4	mA
	Reset						−0.8	mA
	Set						−0.8	mA
	Clock						−0.8	mA
	J-K	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.1	mA
	Reset						0.3	mA
	Set						0.3	mA
	Clock						0.4	mA
Output short circuit current**		I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−100	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current***		I_{CC}	$V_{CC}=5.25V$			4	8	mA

* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.
*** Measured with all outputs open, Q and $\overline{Q}$ outputs alternately HIGH, and clock inputs grounded.

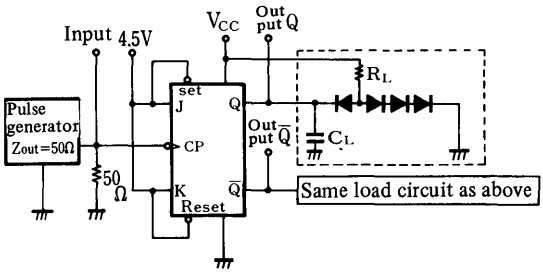
■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Maximum clock frequency	f_{max}			$C_L=15pF$ $R_L=2k\Omega$	30	45		MHz
Propagation delay time	t_{PLH}	Reset or set Clock	Q, $\overline{Q}$			11	20	ns
	t_{PHL}					15	30	ns

※ Switching parameter measurement information

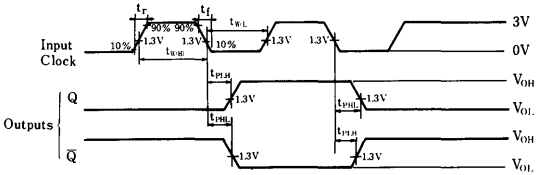
〔1〕 f_{max}, t_{PLH}, t_{PHL} (Clock → Q, $\overline{Q}$)

1. Measurement circuit



1. Measurement made for each flip flop.
2. C_L includes probe and tool floating capacitance.
3. Diodes are all MA161 or equivalent.

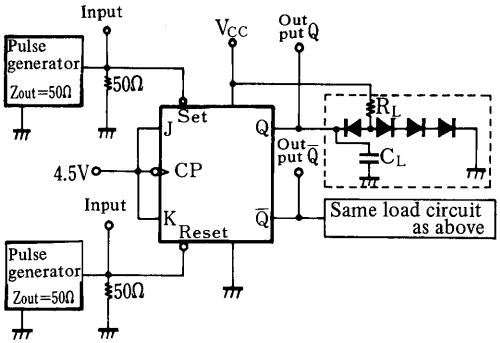
2. Waveforms



Notes
1. Clock input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.
2. When measuring f_{max}, t_r and $t_f \leqq 2.5ns$.

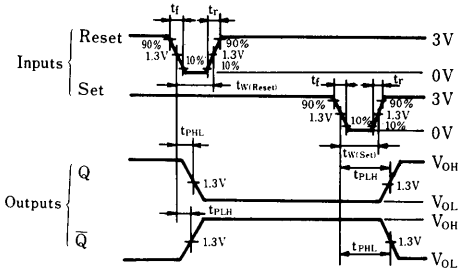
〔2〕 t_{PHI} , t_{PLH}(Reset, Set → Q, $\overline{Q}$)

1. Measurement circuit



Notes
1. Measurement made for each flip flop.
2. C_L includes probe and tool floating capacitance.
3. Diodes are all MA161.

2. Waveforms



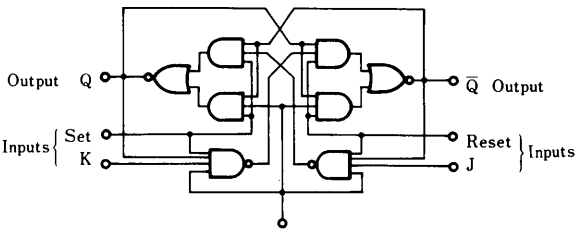
Notes
1. Reset, Set Input waveform: $t_r \leqq 15$ ns, $t_f \leqq 6$ ns, PRR = 1MHz

■ Truth tables

Inputs					Outputs	
Set	Reset	Clock	J	K	Q	$\overline{Q}$
L	H	×	×	×	H	L
H	L	×	×	×	L	H
L	L	×	×	×	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	×	×	Q_0	$\overline{Q}_0$

Notes
1. H: HIGH voltage level.
2. L: LOW voltage level.
3. ↓: Change from HIGH to LOW.
4. X: Either HIGH or LOW; doesn't matter.
5. Q_0: Q level prior to determination of input condition shown in table.
6. $\overline{Q}_0$: $\overline{Q}$ level prior to determination of input condition shown in table.
7. Toggle: With ↓ change, outputs become compliment of previous condition.
8. H*: When set and reset are LOW, Q and $\overline{Q}$ are HIGH; however, when set and reset simultaneously change to HIGH, requirements of Q and $\overline{Q}$ cannot be predicted.

■ Logic diagram (1/2)



DN74LS78

Dual J-K Flip-Flops (with Set, Common Reset and Common Clock)

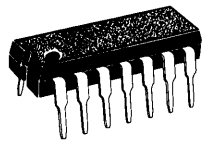
■ Description

DN74LS78 contains two negative-edge triggered J-K flip-flop circuits with common clock-CP, and direct-coupled reset input terminals, and independent J and K input terminals.

■ Features

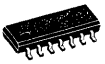
- Negative-edge trigger
- Common clock and direct-coupled reset inputs
- Q and $\overline{Q}$ outputs
- Wide operating temperature range (Ta = −20 to +75°C)

P-1



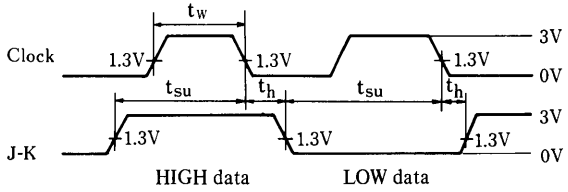
14-pin plastic DIL package

P-4

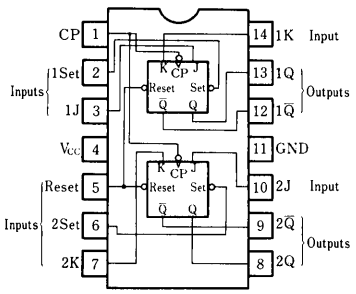


14-pin Panaflat package (SO-14D)

■ Timing definition



Pin configuration (top view)



■ Recommended operating conditions

Parameter		Sym	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}			−400	μA
		I_{OL}			8	mA
Operating temperature range		Topr	−20	25	75	℃
Clock frequency		f_{clock}	0		30	MHz
Pulse width	Clock High	t_w	20			ns
	Reset Low		25			ns
Set-up time	HIGH data	t_{su}	20 ↓			ns
	LOW data		20 ↓			ns
Hold time		t_h	0 ↓			ns

Notes 1. ↓: Indicates fall edge of standard clock pulse.

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter		Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Output voltage		V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2.7V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	3.4		V
		V_{OL1}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
		V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	J-K	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
	Reset						120	μA
	Set						60	μA
	Clock						160	μA
	J-K	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
	Reset						−1.6	mA
	Set						−0.8	mA
	Clock						−1.6	mA
	J-K	I_I	$V_{CC}=5.25V$, $V_I=7V$				0.1	mA
	Reset						0.6	mA
	Set						0.3	mA
	Clock						0.8	mA
Output short circuit current**		I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−100	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$, $I_I=-18mA$				−1.5	V
Supply current***		I_{CC}	$V_{CC}=5.25V$			4	8	mA

* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.
*** Measured with all outputs open, Q and $\overline{Q}$ outputs alternately HIGH, and clock inputs grounded.

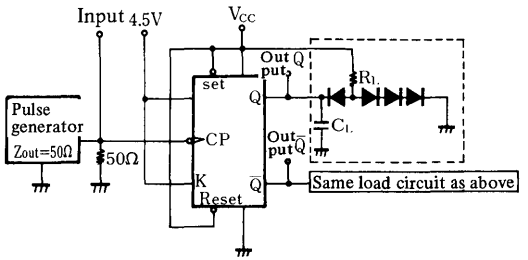
■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Maximum clock frequency	f_{max}			$C_L=15pF$, $R_L=2k\Omega$	30	45		MHz
Propagation delay time	t_{PLH}	Reset or set Clock	Q, $\overline{Q}$			11	20	ns
	t_{PHL}					15	30	ns

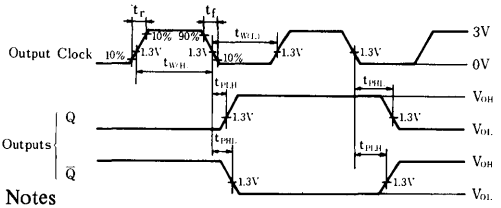
※ Switching parameter measurement information

〔1〕 f_{max}, t_{PLH}, t_{PHL} (Clock → Q, $\overline{Q}$)

1. Measurement circuit



2. Waveforms

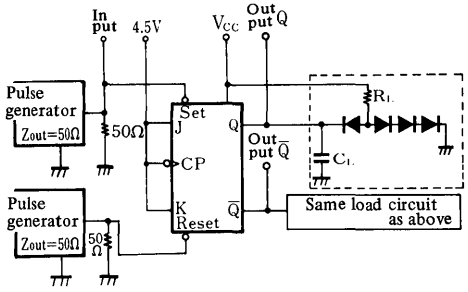


Notes
1. Clock input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.
2. When measuring f_{max}, t_r and $t_f \leqq 2.5ns$.

1. Measurement made for each flip flop.
2. C_L includes probe and tool floating capacitance.
3. Diodes are all MA161 or equivalent.

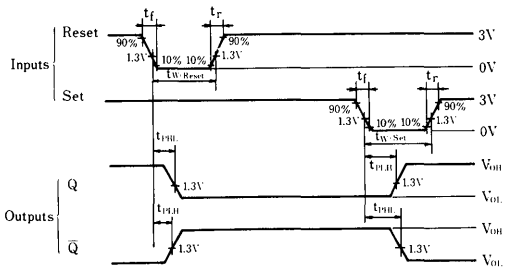
〔2〕 t_{PHL}, t_{PLH}(Reset, Set → Q, $\overline{Q}$)

1. Measurement circuit



Notes
1. Measurement made for each flip flop.
2. C_L includes probe and tool floating capacitance.
3. Diodes are all MA161.

2. Waveforms



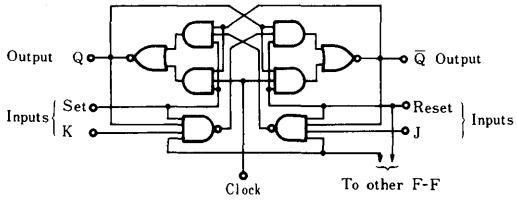
Notes
1. Reset, Set Input waveform:
$t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR=1MHz

■ Truth tables

Inputs					Outputs	
Set	Reset	Clock	J	K	Q	$\overline{Q}$
L	H	×	×	×	H	L
H	L	×	×	×	L	H
L	L	×	×	×	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	×	×	Q_0	$\overline{Q}_0$

Notes
1. H: HIGH voltage level.
2. L: LOW voltage level.
3. ↓: Change from HIGH to LOW.
4. X: Either HIGH or LOW; doesn't matter.
5. Q_0: Q level prior to determination of input condition shown in table.
6. $\overline{Q}_0$: $\overline{Q}$ level prior to determination of input condition shown in table.
7. Toggle: With ↓ change, outputs become compliment of previous condition.
8. H*: When set and reset are LOW, Q and $\overline{Q}$ are HIGH; however, when set and reset simultaneously change to HIGH, requirements of Q and $\overline{Q}$ cannot be predicted.

■ Logic diagram (1/2)



DN74LS83A

4-bit Binary Full Adders (with Fast Carry)

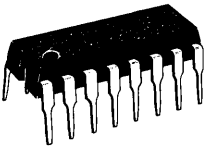
■ Description

DN74LS83A is a 4-bit full-adder with a "look-ahead" carry.

■ Features

- "Look-ahead" carry for high speed
- Partial "look-ahead" carry for system capability
- Wide operating temperature range (Ta = −20 to +75°C)

P-2

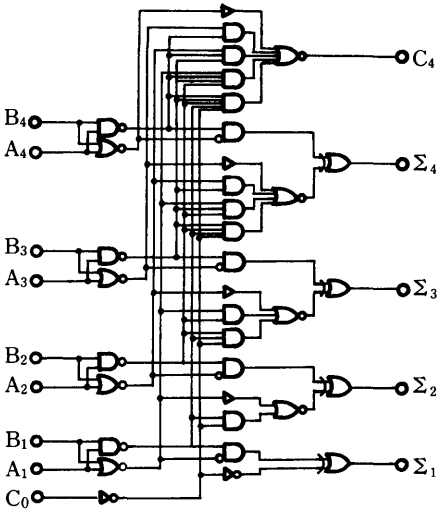


16-pin plastic DIL package

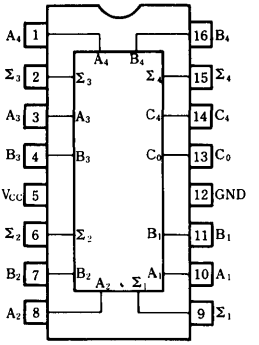
P-5

16-pin Panaflat package (SO-16D)

■ Logic diagram



Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−400	μA
	I_{OL}			8	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter		Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Output voltage		V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	3.4		V
		V_{OL1}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
		V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	Inputs other than C_0	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$				40	μA
	C_0						20	μA
	Inputs other than C_0	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$				−0.8	mA
	C_0						−0.4	mA
	Inputs other than C_0	I_I	$V_{CC}=5.25V$, $V_I=7V$				0.2	mA
	C_0						0.1	mA
Output short circuit current**		I_{OS}	$V_{CC}=5.25$, $V_O=0V$		−15		−100	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$, $I_I=-18mA$				−1.5	V
Supply current***		I_{CC}	$V_{CC}=5.25V$	All inputs = 0V		22	39	mA
				B input = 0.8V, Other inputs = 4.5V		19	34	mA
				All inputs = 4.5V		19	34	mA

* When constant at V_{CC} = 5V, Ta = 25°C.

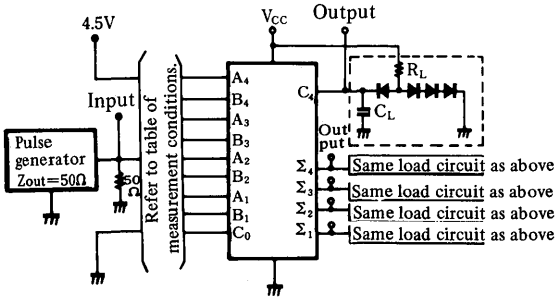
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

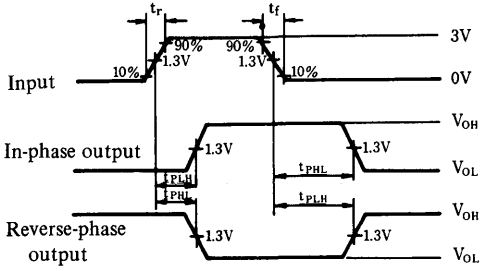
Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	C_0	Σi	$C_L=15pF$, $R_L=2k\Omega$		16	24	ns
	t_{PHL}					15	24	ns
	t_{PLH}	Ai, Bi	Σi			15	24	ns
	t_{PHL}					15	24	ns
	t_{PLH}	C_0	C_4			11	17	ns
	t_{PHL}					15	22	ns
	t_{PLH}	Ai, Bi	C_4			11	17	ns
	t_{PHL}					12	17	ns

※ Switching parameter measurement information

1. Measurement circuit



2. Waveforms



Notes

1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161 or equivalent.

Notes

1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.

3. Table of measurement conditions

Parameter	Input / Output	Inputs									Outputs				
		B_4	A_4	B_3	A_3	B_2	A_2	B_1	A_1	C_0	C_4	Σ_4	Σ_3	Σ_2	Σ_1
	C_0 → Σi or C_4	GND	GND	GND	GND	GND	GND	GND	GND	IN					OUT
		GND	4.5V	GND	4.5V	GND	4.5V	GND	4.5V	IN	OUT	OUT	OUT	OUT	OUT
	Ai or Bi → Σi or C_4	GND	GND	GND	GND	GND	GND	GND / IN	IN / GND	GND					OUT
		GND	GND	GND	GND	GND / IN	IN / GND	GND	GND	GND				OUT	
		GND	GND	GND / IN	IN / GND	GND	GND	GND	GND	GND			OUT		
t_{PLH} / t_{PHL}		GND / IN	IN / GND	GND	GND	GND	GND	GND	GND	GND		OUT			
		GND	GND	GND	GND	GND	GND	4.5V / IN	IN / 4.5V	GND				OUT	OUT
		GND	GND	GND	GND	4.5V / IN	IN / 4.5V	GND	GND	GND			OUT	OUT	
		GND	GND	4.5V / IN	IN / 4.5V	GND	GND	GND	GND	GND		OUT	OUT		
		4.5V / IN	IN / 4.5V	GND	GND	GND	GND	GND	GND	GND	OUT	OUT			

■ Truth tables

Inputs				Outputs					
				When C_0 = L/When C_2 = L			When C_0 = H/When C_2 = H		
A_1 / A_3	B_1 / B_3	A_2 / A_4	B_2 / B_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

Notes
1. H: HIGH voltage level.
2. L: LOW voltage level.
3. A_1, B_1, A_2, and B_2 input requirements are used to determine the values of Z_1, Z_2, and the internal carry C_2. Next, C_2, A_3, B_3, A_4, and B_4 values are used to determine output Σ_3 and Σ_4. (C_2 is not output as an external signal.)

DN74LS85

4-bit Magnitude Comparators

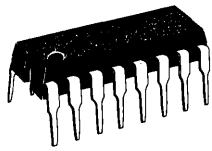
■ Description

DN74LS85 is a 4-bit digital comparator.

■ Features

- Number of bits easily increased
- Low output impedance
- Wide operating temperature range (Ta = −20 to +75°C)

P-2

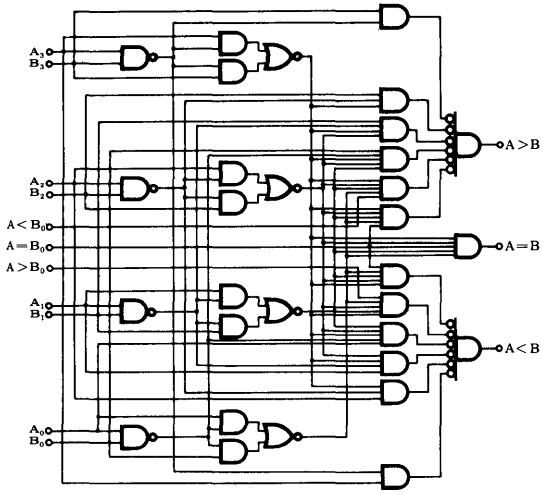


16-pin plastic DIL package

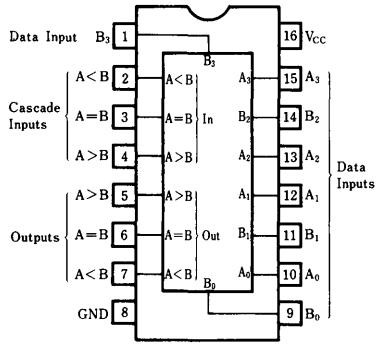
P-5

16-pin Panaflat package (SO-16D)

■ Logic diagram



Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−400	μA
	I_{OL}			8	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter		Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Output voltage		V_{OH}	$V_{CC}=4.75V$, $I_{OH}=-400\mu A$ $V_{IH}=2V$, $V_{IL}=0.8V$		2.7	3.4		V
		V_{OL1}	$V_{CC}=4.75V$ $V_{IH}=2V$ $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
		V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	Inputs where A ⟨ B, A ⟩ B	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				20	μA
	Other inputs						60	μA
	Inputs where A ⟨ B, A ⟩ B	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.4	mA
	Other inputs						−1.2	mA
	Inputs where A ⟨ B, A ⟩ B	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.1	mA
	Other inputs						0.3	mA
Output short circuit current**		I_{OS}	$V_{CC}=5.25V$ $V_O=0V$		−15		−100	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current***		I_{CC}	$V_{CC}=5.25V$			10.4	20	mA

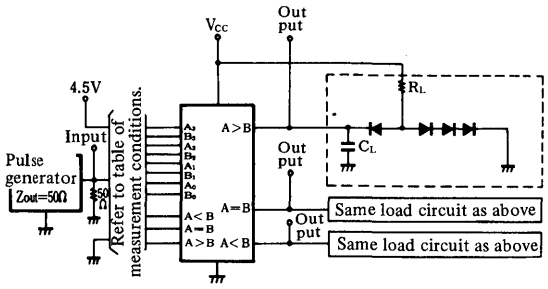
* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.
*** I_{CC} is measured with all outputs open, A = B input terminal grounded, and 4.5V applied to other input terminals.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

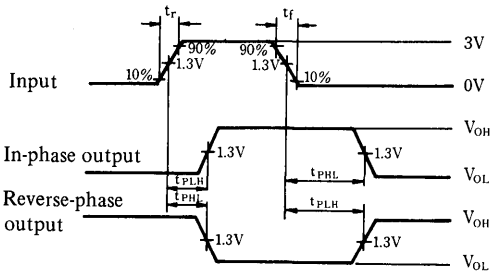
Parameter	Sym	Inputs	Outputs	Gate level	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	Any A or B data Input	A⟨B A⟩B	1	$C_L=15pF$ $R_L=2k\Omega$		14		ns
				2			19		ns
				3			24	36	ns
			A=B	4			27	45	ns
	t_{PHL}	Any A or B data Input	A⟨B A⟩B	1			11		ns
				2			15		ns
				3			20	30	ns
			A=B	4			23	45	ns
	t_{PLH}	A⟨B or A=B	A⟩B	1			14	22	ns
	t_{PHL}	A⟨B or A=B	A⟩B	1			11	17	ns
	t_{PLH}	A=B	A=B	2			13	20	ns
	t_{PHL}	A=B	A=B	2			13	26	ns
	t_{PLH}	A⟩B or A=B	A⟨B	1			14	22	ns
	t_{PHL}	A⟩B or A=B	A⟨B	1			11	17	ns

※ Switching parameter measurement information

1. Measurement circuit



2. Waveforms



1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161 or equivalent.

Notes
1. Input waveform: $t_r \leqq 15$ns, $t_f \leqq 6$ns, PRR = 1MHz, duty cycle = 50%.

3. Table of measurement conditions

Para-meter	DC inputs											Output waveforms		
	A_3	B_3	A_2	B_2	A_1	B_1	A_0	B_0	A>B	A=B	A<B	A>B	A=B	A<B
	IN	4.5V	4.5V	GND	GND	GND	GND	GND	GND	GND	GND	A		B
	4.5V	IN	GND	4.5V	GND	GND	GND	GND	GND	GND	GND	B		A
	GND	GND	IN	4.5V	4.5V	GND	GND	GND	GND	GND	GND	A		B
	GND	GND	4.5V	IN	GND	4.5V	GND	GND	GND	GND	GND	B		A
	GND	GND	GND	GND	IN	4.5V	4.5V	GND	GND	GND	GND	A		B
	GND	GND	GND	GND	4.5V	IN	GND	4.5V	GND	GND	GND	B		A
t_{PLH}	GND	GND	GND	GND	GND	GND	IN	4.5V	4.5V	GND	GND	A		B
t_{PHL}	GND	GND	GND	GND	GND	GND	4.5V	IN	GND	GND	4.5V	B		A
	GND	GND	GND	GND	GND	GND	IN	4.5V	GND	4.5V	GND		A	B
	GND	GND	GND	GND	GND	GND	4.5V	IN	GND	4.5V	GND	B	A	
	GND	GND	GND	GND	GND	GND	GND	GND	IN	GND	GND			B
	GND	GND	GND	GND	GND	GND	GND	GND	GND	IN	GND	B	A	B
	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	IN	B		

■ Truth tables

Inputs				Previous stage direct coupled inputs			Outputs		
A_3, B_3	A_2, B_2	A_1, B_1	A_0, B_0	A>B	A<B	A=B	A>B	A<B	A=B
$A_3 > B_3$	×	×	×	×	×	×	H	L	L
$A_3 < B_3$	×	×	×	×	×	×	L	H	L
$A_3 = B_3$	$A_2 > B_2$	×	×	×	×	×	H	L	L
$A_3 = B_3$	$A_2 < B_2$	×	×	×	×	×	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 > B_1$	×	×	×	×	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 < B_1$	×	×	×	×	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 > B_0$	×	×	×	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 < B_0$	×	×	×	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	H	L	L	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	H	L	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	L	H	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	×	×	H	L	L	H
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	H	H	L	L	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	L	L	H	H	L

Notes

1. H: HIGH voltage level.
2. L: LOW voltage level.
3. X: Either HIGH or LOW; doesn't matter.

DN74LS86

Quad 2-input Exclusive OR Gates

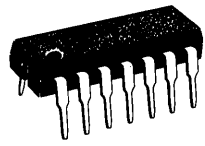
■ Description

DN74LS86 contains four 2-input exclusive OR gate circuits.

■ Features

- Low power consumption (P_d = 30.5mV typical)
- High speed (t_{pd} = 10ns typical)
- Low output impedance
- Wide operating temperature range (Ta = −20 to +75°C)

P-1



14-pin plastic DIL package

P-4

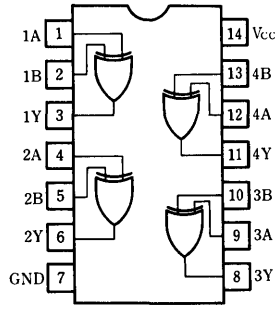
14-pin Panaflat package (SO-14D)

■ Truth tables

Inputs		Outputs
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

Notes
1. H: HIGH voltage level.
2. L: LOW voltage level.

Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−400	μA
	I_{OL}			8	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$ $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	3.4		V
	V_{OL1}	$V_{CC}=4.75V$ $V_{IH}=2V$ $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
	V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				40	μA
	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.8	mA
	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.2	mA
Output short circuit current**	I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−100	mA
Input clamp voltage	V_{IK}	$V_{CC}=5.25V$ $I_I=-18mA$				−1.5	V
Supply current***	I_{CC}	$I_{CC}=5.25V$			6.1	10	mA

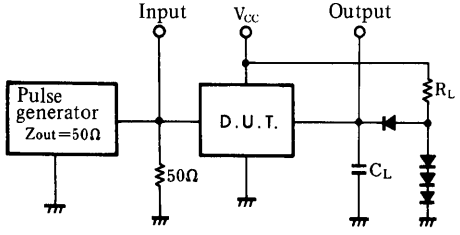
* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.
*** I_{CC} is measured with all outputs open and all inputs grounded.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Test conditions		Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	A or B	$C_L=15pF$ $R_L=2k\Omega$	Other input = 0V		12	23	ns
	t_{PHL}					10	17	
	t_{PLH}	A or B		Other input = 4.5V		20	30	ns
	t_{PHL}					13	22	

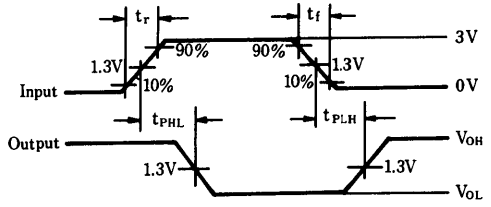
※ Switching parameter measurement information

1. Measurement circuit



Notes
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161 or equivalent.

2. Waveforms



Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.

DN74LS90

Decade Counters

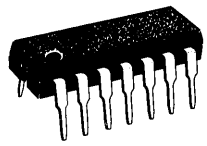
Description

DN74LS90 is an asynchronous decade counter with direct-coupled reset input and nine direct-coupled set input terminals.

Features

- Direct-coupled reset input
- Nine direct-coupled set inputs
- Capability for independent use as binary and quinary counters
- High-speed counting (f_{max} = 42MHz typical)
- Wide operating temperature range (Ta = −20 to +75°C)

P-1

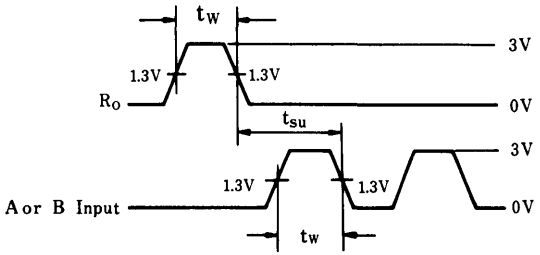


14-pin plastic DIL package

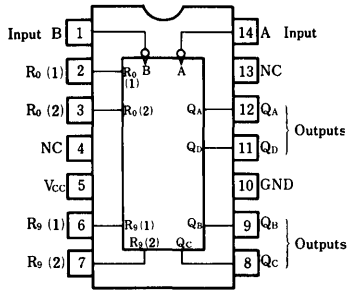
P-4

14-pin Panaflat package (SO-14D)

Timing definition



Pin configuration (top view)



Absolute maximum ratings

Parameter		Sym.	Rating		Unit
Input voltage	R	V_I	−0.5	7.0	V
	A, B		−0.5	5.5	

* Refer to the family ratings for other parameters.

Recommended operating conditions

Parameter		Sym	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}			−400	μA
		I_{OL}			8	mA
Operating temperature range		Topr	−20	25	75	℃
Count frequency	A input	f_{count}	0		32	MHz
	B input		0		16	MHz
Pulse width	A input	t_W	15			ns
	B input		30			ns
	Reset input		15			ns
Set-up time		t_{su}	25			ns

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter		Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Output voltage**		V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$ $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	3.4		V
		V_{OL1}	$V_{CC}=4.75V$ $V_{IH}=2V$ $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
		V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	Any Reset	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				20	μA
	A input						40	μA
	B input						80	μA
	Any Reset	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.4	mA
	A input						−2.4	mA
	B input						−3.2	mA
	Any Reset	I_I	$V_{CC}=5.25V$	$V_I=7V$			0.1	mA
	A input			$V_I=5.5V$			0.2	mA
	B input						0.4	mA
Output short circuit current***		I_{OS}	$V_{CC}=5.25$ $V_O=0V$		−15		−100	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current****		I_{CC}	$V_{CC}=5.25V$			9	15	mA

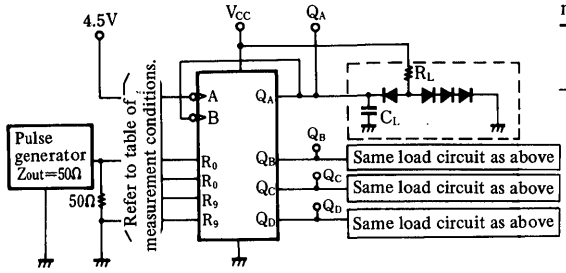
* When constant at V_{CC} = 5V, Ta = 25°C.
** When testing Q_A output, it is set to specified I_{OL} and rated upper limit of B input I_{IL} is applied.
*** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.
**** I_{CC} is measured with all outputs open; 4.5V is applied momentarily to both R_O inputs, following which they are grounded.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Maximum count frequency	f_{max}	A	Q_A	$C_L=15pF$ $R_L=2k\Omega$	32	42		MHz
		B	Q_B		16			MHz
Propagation delay time	t_{PLH}	A	Q_A			10	16	ns
	t_{PHL}					12	18	ns
	t_{PLH}	A	Q_D			32	48	ns
	t_{PHL}					34	50	ns
	t_{PLH}	B	Q_B			10	16	ns
	t_{PHL}					14	21	ns
	t_{PLH}	B	Q_C			21	32	ns
	t_{PHL}					23	35	ns
	t_{PLH}	B	Q_D			21	32	ns
	t_{PHL}					23	35	ns
	t_{PHL}	Set-to-0	$Q_A \sim Q_D$			26	40	ns
	t_{PLH}	Set-to-9	Q_A, Q_D			20	30	ns
	t_{PHL}		Q_B, Q_C			26	40	ns

※ Switching parameter measurement information

1. Measurement circuit



1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161.

2. Table of measurement conditions

Parameter	Input / Output	Inputs A	Inputs B	Inputs R_0	Inputs R_9	Outputs Q_A	Outputs Q_B	Outputs Q_C	Outputs Q_D
f_{max}	A→Q	IN	to Q_A	GND	GND	Out	Out	Out	Out
	B**→Q	4.5V	IN	GND	GND		Out	Out	Out
t_{PLH} t_{PHL}	A→Q_A	IN	to Q_A	GND	GND	Out			
	A→Q_D	IN	to Q_A	GND	GND				Out
	B**→Q_B	4.5V	IN	GND	GND		Out		
	B**→Q_C	4.5V	IN	GND	GND			Out	
	B**→Q_D	4.5V	IN	GND	GND				Out
	R_0***→Q	IN *	to Q_A	IN	GND	Out	Out	Out	Out
	R_9***→Q	IN *	to Q_A	GND	IN	Out	Out	Out	Out

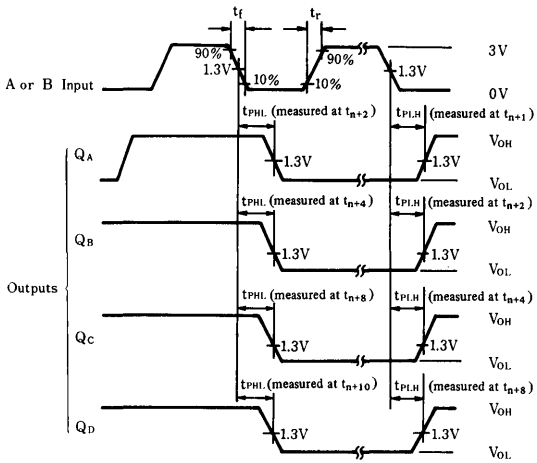
* Applied for initialization.

** For characteristic measurement from B input, Q_A and B are disconnected and pulse is applied to B input.

*** Measured for each terminal; 4.5V applied to terminals to which input pulse is not applied.

3.Waveforms

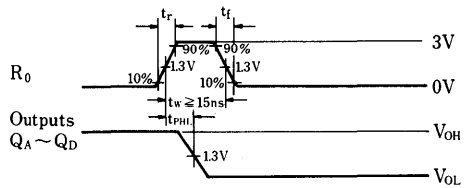
Waveforms-1



Notes

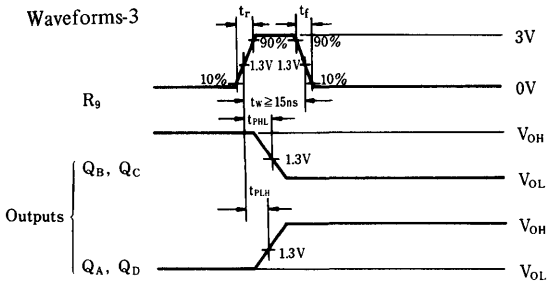
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 5ns$, PRR = 1MHz, duty cycle = 50%.
2. When measuring f_{max}, t_r and $t_f \leqq 2.5ns$.
3. t_n is the bit time when all outputs are LOW.

Waveforms-2



Notes $t_r \leqq 15ns$, $t_f \leqq 5ns$

Waveforms-3



Notes $t_r \leqq 15ns$, $t_f \leqq 5ns$

■ Truth tables

1. Reset/count truth table

Reset inputs				Outputs			
$R_0(1)$	$R_0(2)$	$R_9(1)$	$R_9(2)$	Q_D	Q_C	Q_B	Q_A
H	H	L	×	L	L	L	L
H	H	×	L	L	L	L	L
×	×	H	H	H	L	L	H
×	L	×	L	Count			
L	×	L	×	Count			
L	×	×	L	Count			
×	L	L	×	Count			

2. BCD count sequence**

Count	Outputs			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

During BCD count, output Q_A is connected to input B.

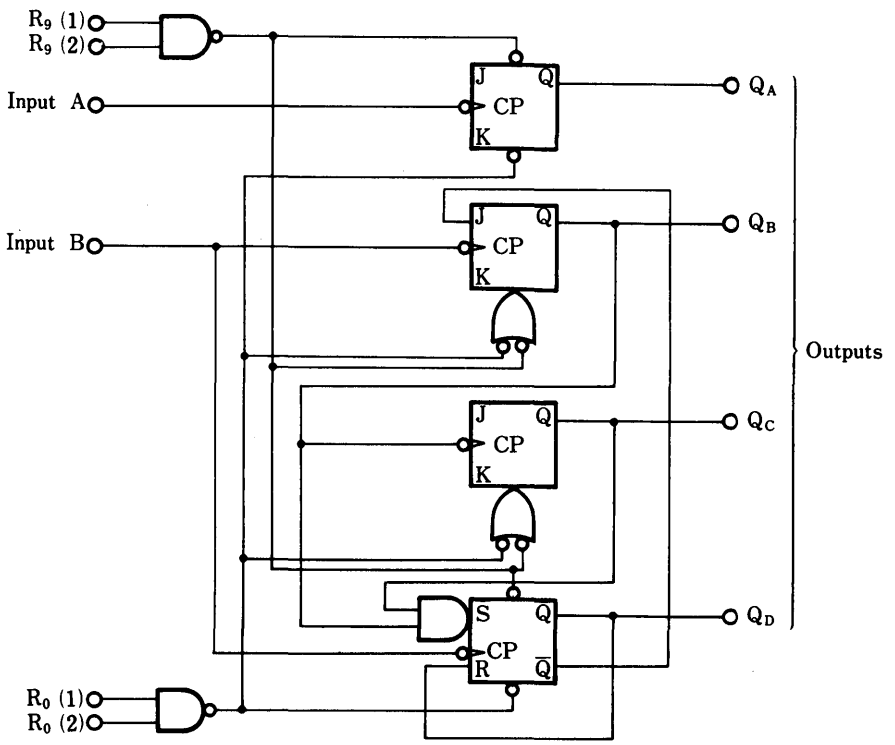
3. Bi-quinary count sequence**

Count	Outputs			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

During bi-quinary count, output Q_D is connected to input A.

Notes
1. H: HIGH voltage level.
2. L: LOW voltage level.
3. X: Either HIGH or LOW; doesn't matter.

■ Logic diagram



DN74LS92

Divide-by-Twelve Counters

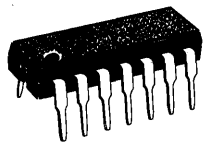
■ Description

DN74LS92 is an asynchronous duodecimal counter with direct-coupled reset input.

■ Features

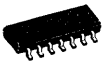
- Direct-coupled reset input
- Capability for independent use as binary and hex counters
- High-speed counting (f_{max} = 42MHz typical)
- Wide operating temperature range (Ta = −20 to +75°C)

P-1



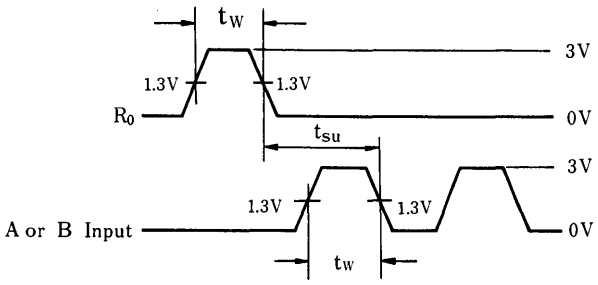
14-pin plastic DIL package

P-4

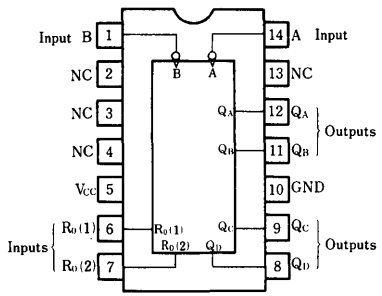


14-pin Panaflat package (SO-14D)

■ Timing definition



Pin configuration (top view)



■ Absolute maximum ratings

Parameter		Sym.	Rating		Unit
Input voltage	R	V_I	−0.5	7.0	V
	A, B		−0.5	5.5	

* Refer to the family ratings for other parameters.

■ Recommended operating conditions

Parameter		Sym	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}			−400	μA
		I_{OL}			8	mA
Operating temperature range		Topr	−20	25	75	℃
Count frequency	A input	f_{count}	0		32	MHz
	B input		0		16	MHz
Pulse width	A input	t_W	15			ns
	B input		30			ns
	Reset input		15			ns
Set-up time		t_{su}	25			ns

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter		Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Output voltage**		V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$ $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	3.4		V
		V_{OL1}	$V_{CC}=4.75V$ $V_{IH}=2V$ $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
		V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	Any Reset	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				20	μA
	A input						40	μA
	B input						80	μA
	Any Reset	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.4	mA
	A input						−2.4	mA
	B input						−3.2	mA
	Any Reset	I_I	$V_{CC}=5.25V$	$V_I=7V$			0.1	mA
	A input			$V_I=5.5V$			0.2	mA
	B input						0.4	mA
Output short circuit current***		I_{OS}	$V_{CC}=5.25$ $V_O=0V$		−15		−100	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current****		I_{CC}	$V_{CC}=5.25V$			9	15	mA

* When constant at V_{CC} = 5V, Ta = 25°C.

** When testing Q_A output, it is set to specified I_{OL} and rated upper limit of B input I_{IL} is applied.

*** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

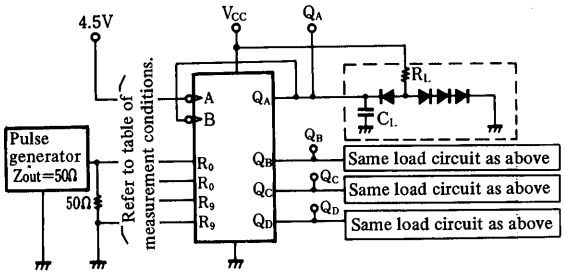
**** I_{CC} is measured with all outputs open; 4.5V is applied momentarily to both R_O inputs, following which they are grounded.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Maximum count frequency	f_{max}	A	Q_A	$C_L=15pF$ $R_L=2k\Omega$	32	42		MHz
		B	Q_B		16			MHz
Propagation delay time	t_{PLH}	A	Q_A			10	16	ns
	t_{PHL}					12	18	ns
	t_{PLH}	A	Q_D			32	48	ns
	t_{PHL}					34	50	ns
	t_{PLH}	B	Q_B			10	16	ns
	t_{PHL}					14	21	ns
	t_{PLH}	B	Q_C			10	16	ns
	t_{PHL}					14	21	ns
	t_{PLH}	B	Q_D			21	32	ns
	t_{PHL}					23	35	ns
	t_{PHL}	Set-to-0	$Q_A \sim Q_D$			26	40	ns

※ Switching parameter measurement information

1. Measurement circuit



1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161.

2. Table of measurement conditions

Parameter	Input / Output	Inputs A	Inputs B	Inputs R_0	Outputs Q_A	Outputs Q_B	Outputs Q_C	Outputs Q_D
f_{max}	A→Q	IN	to Q_A	GND	Out	Out	Out	Out
	B**→Q	4.5V	IN	GND		Out	Out	Out
t_{PLH} t_{PHL}	A→Q_A	IN	to Q_A	GND	Out			
	A→Q_D	IN	to Q_A	GND				Out
	B**→Q_B	4.5V	IN	GND		Out		
	B**→Q_C	4.5V	IN	GND			Out	
	B**→Q_D	4.5V	IN	GND				Out
	R_0***→Q	IN*	to Q_A	IN	Out	Out	Out	Out

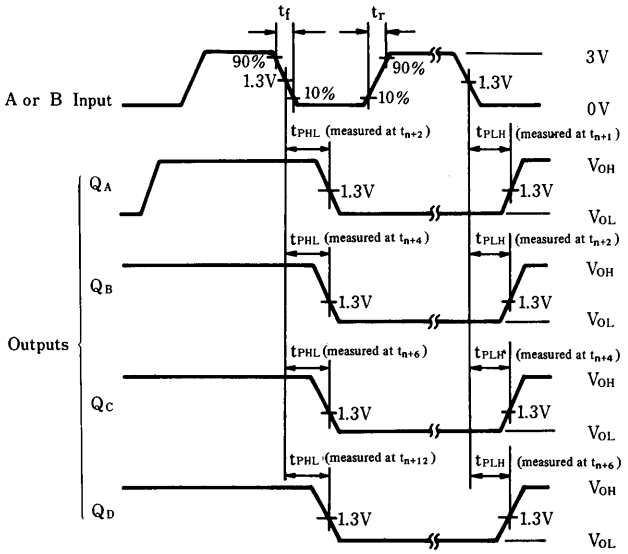
* Applied for initialization.

** For characteristic measurement from B input, Q_A and B are disconnected and pulse is applied to B input.

*** Measured for each terminal; 4.5V applied to terminals to which input pulse is not applied.

3.Waveforms

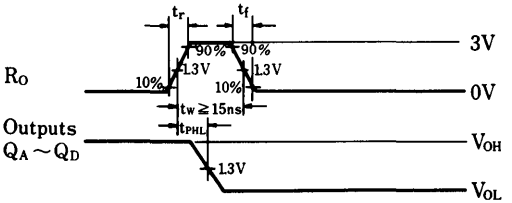
Waveforms-1



Notes

1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 5ns$, PRR = 1MHz, duty cycle = 50%.
2. When measuring f_{max}, t_r and $t_f \leqq 2.5ns$.
3. t_n is the bit time when all outputs are LOW.

Waveforms-2



Notes $t_r \leq 15ns$, $t_f \leq 5ns$

■ Truth tables

1. Reset/count truth table

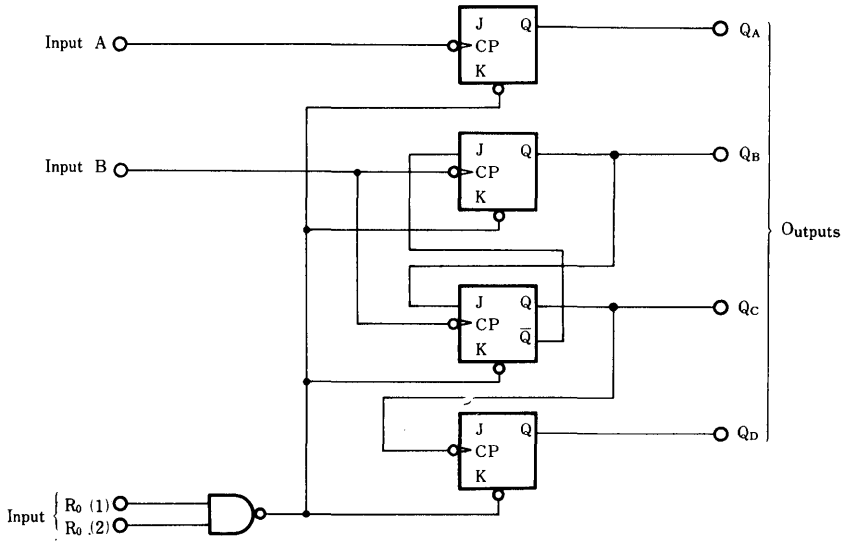
Reset inputs		Outputs			
$R_0(1)$	$R_0(2)$	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	×	Count			
×	L	Count			

2. Count sequence (See note 1.)

Count	Outputs			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	H	H
10	H	H	L	L
11	H	H	L	H

Notes
1. Output Q_A is connected to input B.
2. H: HIGH voltage level.
3. L: LOW voltage level.
4. X: Either HIGH or LOW; doesn't matter.

■ Logic diagram



DN74LS93

4-bit Binary Counters

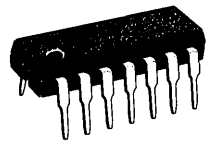
■ Description

DN74LS93 is an asynchronous 4-bit binary (hexadecimal) counter with direct-coupled reset input.

■ Features

- Direct-coupled reset input
- Capability for independent use as binary and octal counters
- High-speed counting (f_{max} = 42MHz typical)
- Wide operating temperature range (Ta = −20 to +75°C)

P-1

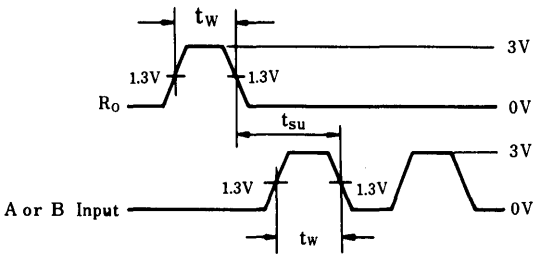


14-pin plastic DIL package

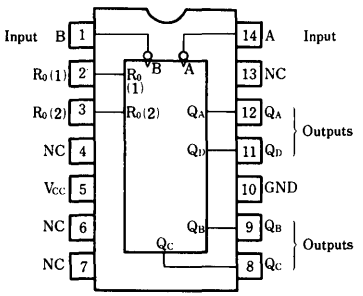
P-4

14-pin Panaflat package (SO-14D)

■ Timing definition



Pin configuration (top view)



■ Absolute maximum ratings

Parameter		Sym.	Rating		Unit
Input voltage	R	V_I	−0.5	7.0	V
	A, B		−0.5	5.5	

* Refer to the family ratings for other parameters.

■ Recommended operating conditions

Parameter		Sym	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}			−400	μA
		I_{OL}			8	mA
Operating temperature range		Topr	−20	25	75	℃
Count frequency	A input	f_{count}	0		32	MHz
	B input		0		16	MHz
Pulse width	A input	t_W	15			ns
	B input		30			ns
	Reset input		15			ns
Set-up time		t_{su}	25			ns

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter		Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Output voltage**		V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	3.4		V
		V_{OL1}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
		V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	Any Reset	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
	A input						40	μA
	B input						40	μA
	Any Reset	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
	A input						−2.4	mA
	B input						−1.6	mA
	Any Reset	I_I	$V_{CC}=5.25V$	$V_I=7V$			0.1	mA
	A input			$V_I=5.5V$			0.2	mA
	B input						0.2	mA
Output short circuit current***		I_{OS}	$V_{CC}=5.25$, $V_O=0V$		−15		−100	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$, $I_I=-18mA$				−1.5	V
Supply current****		I_{CC}	$V_{CC}=5.25V$			9	15	mA

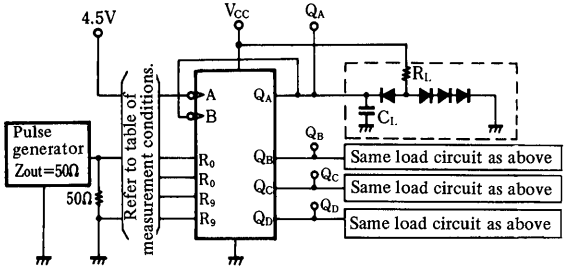
* When constant at V_{CC} = 5V, Ta = 25°C.
** When testing Q_A output, it is set to specified I_{OL} and rated upper limit of B input I_{IL} is applied.
*** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.
**** I_{CC} is measured with all outputs open; 4.5V is applied momentarily to both R_O inputs, following which they are grounded.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Maximum count frequency	f_{max}	A	Q_A	$C_L=15pF$, $R_L=2k\Omega$	32	42		MHz
		B	Q_B		16			MHz
Propagation delay time	t_{PLH}	A	Q_A			10	16	ns
	t_{PHL}					12	18	ns
	t_{PLH}	A	Q_D			46	70	ns
	t_{PHL}					46	70	ns
	t_{PLH}	B	Q_B			10	16	ns
	t_{PHL}					14	21	ns
	t_{PLH}	B	Q_C			21	32	ns
	t_{PHL}					23	35	ns
	t_{PLH}	B	Q_D			34	51	ns
	t_{PHL}					34	51	ns
	t_{PHL}	Set-to-O	$Q_A \sim Q_D$			26	40	ns

※ Switching parameter measurement information

1. Measurement circuit



1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161.

2. Table of measurement conditions

Parameter	Input / Output	Inputs A	Inputs B	Inputs R_0	Outputs Q_A	Outputs Q_B	Outputs Q_C	Outputs Q_D
f_{max}	A→Q	IN	t_0 Q_A	GND	Out	Out	Out	Out
	B**→Q	4.5V	IN	GND		Out	Out	Out
t_{PLH} t_{PHL}	A→Q_A	IN	t_0 Q_A	GND	Out			
	A→Q_D	IN	t_0 Q_A	GND				Out
	B**→Q_B	4.5V	IN	GND		Out		
	B**→Q_C	4.5V	IN	GND			Out	
	B**→Q_D	4.5V	IN	GND				Out
	R_0***→Q	IN*	t_0 Q_A	IN	Out	Out	Out	Out

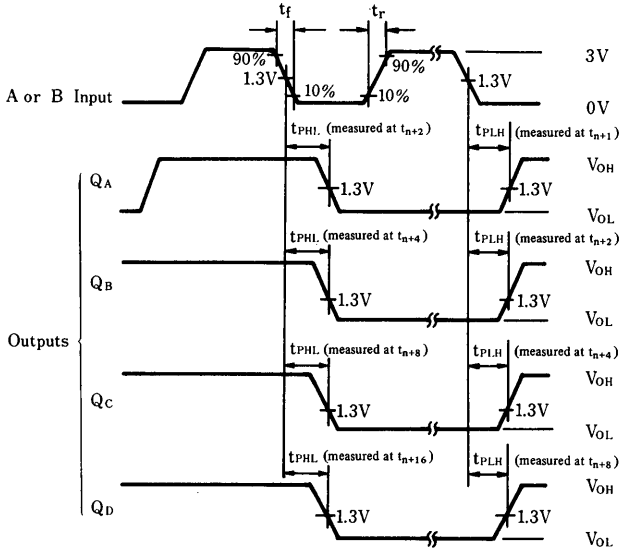
* Applied for initialization.

** For characteristic measurement from B input, Q_A and B are disconnected and pulse is applied to B input.

*** Measured for each terminal; 4.5V applied to terminals to which input pulse is not applied.

3.Waveforms

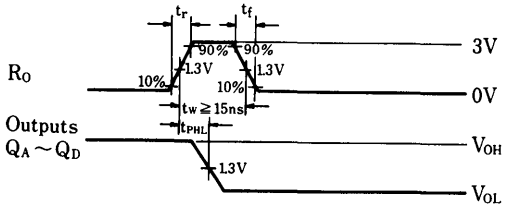
Waveforms-1



Notes

1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 5ns$, PRR = 1MHz, duty cycle = 50%.
2. When measuring f_{max}, t_r and $t_f \leqq 2.5ns$.
3. t_n is the bit time when all outputs are LOW.

Waveforms-2



Notes $t_r \leq 15ns$, $t_f \leq 5ns$

■ Truth tables

1. Reset/count truth table

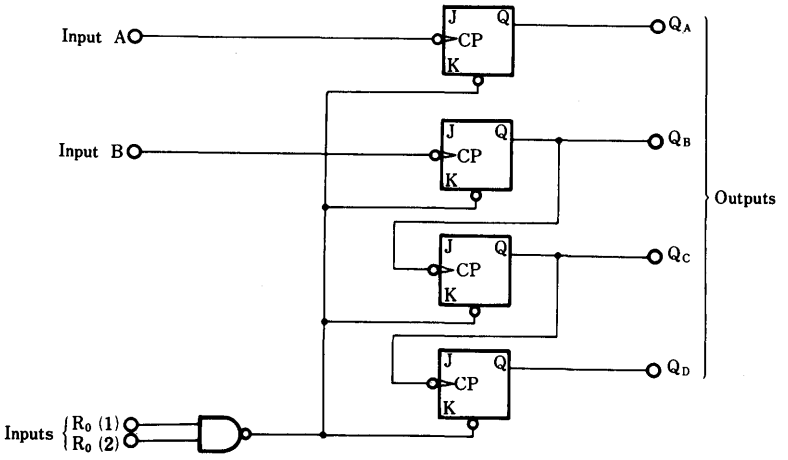
Reset inputs		Outputs			
$R_0(1)$	$R_0(2)$	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	×	Count			
×	L	Count			

2. Count sequence (See note 1.)

Count	Outputs			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

Notes
1. Output Q_A is connected to input B.
2. H: HIGH voltage level.
3. L: LOW voltage level.
4. X: Either HIGH or LOW; doesn't matter.

■ Logic diagram



DN74LS95B

4-bit Parallel-Acces Shift Registers

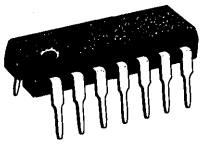
■ Description

DN74LS95B is a 4-bit serial/parallel input to serial/parallel output shift register.

■ Features

- Synchronous serial/parallel input to serial/parallel output
- Right shift
- Left shift capability with external connection
- Exclusive input for left shift and right shift
- Wide operating temperature range (Ta = −20 to +75°C)

P-1

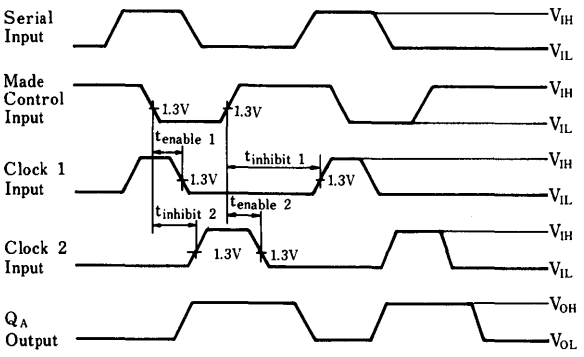


14-pin plastic DIL package

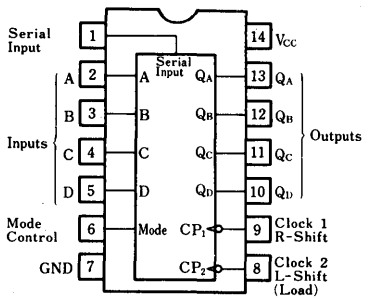
P-4

14-pin Panaflat package (SO-14D)

■ Timing definition



Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−400	μA
	I_{OL}			8	mA
Operating temperature range	Topr	−20	25	75	℃
Clock frequency	f_{clock}	0		25	MHz
Clock pulse width	t_w(CP)	25			ns
Set-up time	t_{su}	20			ns
Hold time	t_h	10			ns
Enable time 1	$t_{enable\ 1}$	20			ns
Enable time 2	$t_{enable\ 2}$	20			ns
Inhibit time 1	$t_{inhibit\ 1}$	20			ns
Inhibit time 2	$t_{inhibit\ 2}$	20			ns

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$ $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	3.4		V
	V_{OL1}	$V_{CC}=4.75V$ $V_{IH}=2V$ $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
	V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				20	μA
	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.4	mA
	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.1	mA
Output short circuit current**	I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−100	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current***	I_{CC}	$I_{CC}=5.25V$			13	21	mA

* When constant at V_{CC} = 5V, Ta = 25°C.

** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

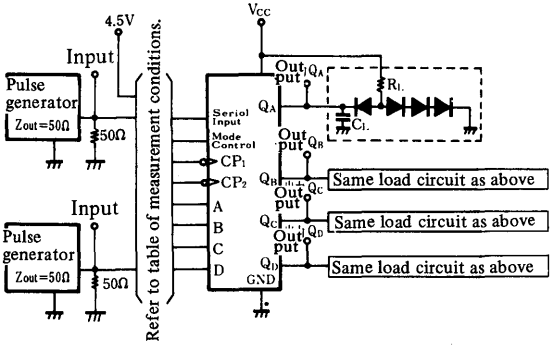
*** Measured with all outputs and serial inputs open, A, B, C, and D inputs grounded, and 4.5V applied to mode control; also, 3V applied momentarily to both clock inputs, following which they are grounded.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Test conditions	Min	Typ	Max	Unit
Maximum clock frequency	f_{max}	$C_L=15pF$ $R_L=2k\Omega$	25	36		MHz
Propagation delay time	t_{PLH}			18	27	ns
	t_{PHL}			21	32	ns

※ Switching parameter measurement information

1. Measurement circuit

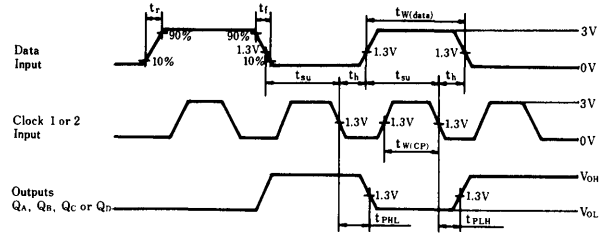


1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161.

2. Table of measurement conditions

Para-meter	Input Output	Inputs								Outputs			
		CP-1	CP-2	Mode Control	Serial Input	A	B	C	D	Q_A	Q_B	Q_C	Q_D
f_{max}	CP-1→Q	IN	4.5V	0V	IN	4.5V	4.5V	4.5V	4.5V	Out	Out	Out	Out
	CP-2→Q	4.5V	IN	4.5V	4.5V	IN	IN	IN	IN	Out	Out	Out	Out
t_{PLH} t_{PHL}	CP-1→Q	IN	4.5V	0V	IN	4.5V	4.5V	4.5V	4.5V	Out	Out	Out	Out
	CP-2→Q	4.5V	IN	4.5V	4.5V	IN	IN	IN	IN	Out	Out	Out	Out

3.Waveforms



Notes

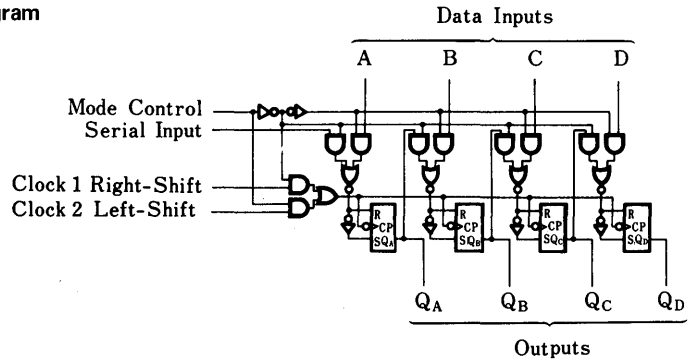
Input waveform ; t_r, $t_f \leqq 10$ns, Data PRR=500kHz, Clock PRR=1MHz

■ Truth tables

Mode Control	Clocks 2 (L)	Clocks 1 (R)	Serial	Parallel A	Parallel B	Parallel C	Parallel D	Q_A	Q_B	Q_C	Q_D
H	H	×	×	×	×	×	×	Q_{AO}	Q_{BO}	Q_{CO}	Q_{DO}
H	↓	×	×	a	b	c	d	a	b	c	d
H	↓	×	×	Q_B^+	Q_C^+	Q_D^+	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d
L	L	H	×	×	×	×	×	Q_{AO}	Q_{BO}	Q_{CO}	Q_{DO}
L	×	↓	H	×	×	×	×	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	×	↓	L	×	×	×	×	L	Q_{An}	Q_{Bn}	Q_{Cn}
↑	L	L	×	×	×	×	×	Q_{AO}	Q_{BO}	Q_{CO}	Q_{DO}
↓	L	L	×	×	×	×	×	Q_{AO}	Q_{BO}	Q_{CO}	Q_{DO}
↓	L	H	×	×	×	×	×	Q_{AO}	Q_{BO}	Q_{CO}	Q_{DO}
↑	H	L	×	×	×	×	×	Q_{AO}	Q_{BO}	Q_{CO}	Q_{DO}
↑	H	H	×	×	×	×	×	Q_{AO}	Q_{BO}	Q_{CO}	Q_{DO}

Note
1. H: HIGH voltage level.
2. L: LOW voltage level.
3. X: Either HIGH or LOW; doesn't matter.
4. ↑: Change from LOW to HIGH.
5. ↓: Change from HIGH to LOW.
6. a ~ b: Constant condition input level of inputs A through D.
7. Q_{Ao} ~ Q_{Do}: Levels of Q_A, Q_B, Q_C, and Q_D prior to determination of input requirements shown in table.
8. Q_{An} ~ Q_{Dn}: Levels of Q_A, Q_B, Q_C, and Q_D prior to nearest clock ↑ (↓) change.
9. Q_B^+, Q_C^+, Q_D^+: For a left shift, there is external linking of A to B_B, B to Q_C, C to Q_D, and serial date is applied to D.

■ Logic diagram



DN74LS107

Dual J-K Flip-Flops (with Reset)

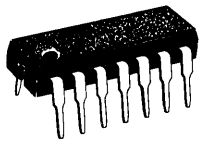
■ Description

DN74LS107 contains two negative-edge triggered J-K flip-flop circuits, each with independent clock-CP, J, K, and direct-coupled reset input terminals.

■ Features

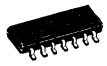
- Negative-edge trigger
- Independent input and output terminals for each flip-flop
- Direct-coupled reset inputs
- Q and $\overline{Q}$ outputs
- Wide operating temperature range (Ta = −20 to +75°C)

P-1



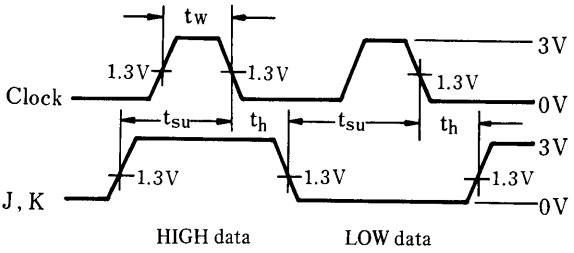
14-pin plastic DIL package

P-4

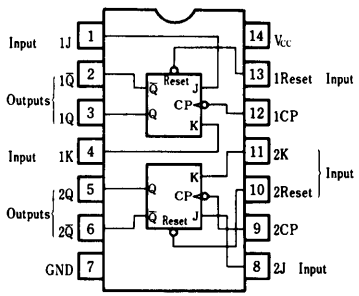


14-pin Panaflat package (SO-14D)

■ Timing definition



Pin configuration (top view)



■ Recommended operating conditions

Parameter		Sym	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}			−400	μA
		I_{OL}			8	mA
Operating temperature range		Topr	−20	25	75	℃
Clock frequency		f_{clock}	0		30	MHz
Pulse width	Clock High	t_w	20			ns
	Reset Low		25			ns
Set-up time	HIGH data	t_{su}	20 ↓			ns
	LOW data		20 ↓			ns
Hold time		t_h	0 ↓			ns

Notes 1. ↓: Indicates fall edge of standard clock pulse.

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter		Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Output voltage		V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	3.4		V
		V_{OL1}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
		V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	J-K	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
	Reset						60	μA
	Clock						80	μA
	J-K	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
	Reset						−0.8	mA
	Clock						−0.8	mA
	J-K	I_I	$V_{CC}=5.25V$, $V_I=7V$				0.1	mA
	Reset						0.3	mA
	Clock						0.4	mA
Output short circuit current**		I_{OS}	$V_{CC}=5.25$, $V_O=0V$		−15		−100	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$, $I_I=-18mA$				−1.5	V
Supply current***		I_{CC}	$V_{CC}=5.25V$			4.0	8.0	mA

* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.
*** Measured with all outputs open, Q and $\overline{Q}$ outputs alternately HIGH, and clock inputs grounded.

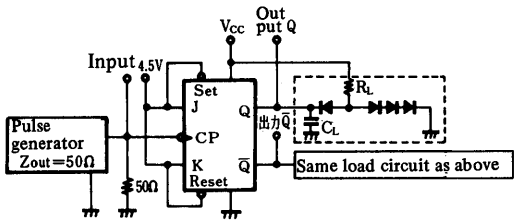
■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Maximum clock frequency	f_{max}			$C_L=15pF$, $R_L=2k\Omega$	30	45		MHz
Propagation delay time	t_{PLH}	Reset, Clock	Q, $\overline{Q}$			11	20	ns
	t_{PHL}					15	30	ns

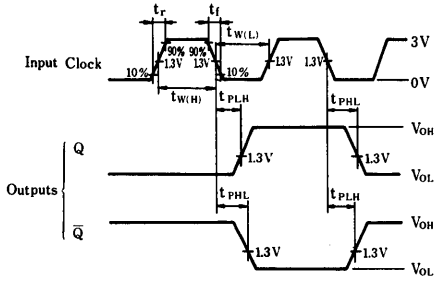
※ Switching parameter measurement information

〔1〕 f_{max}, t_{PLH}, t_{PHL} (Clock → Q, $\overline{Q}$)

1. Measurement circuit



2. Waveforms

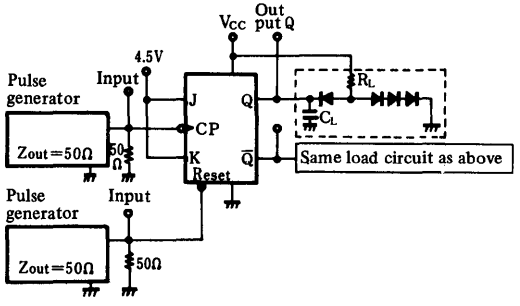


Notes
1. Clock input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.
2. When measuring f_{max}, t_r and $t_f \leqq 2.5ns$.

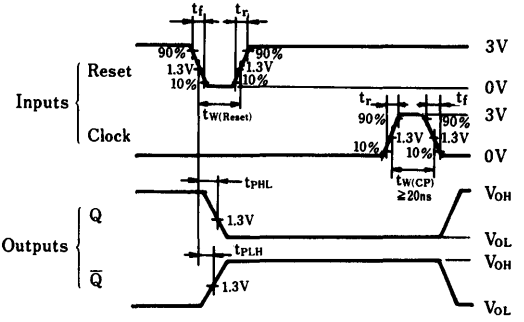
1. Measurement made for each flip flop.
2. C_L includes probe and tool floating capacitance.
3. Diodes are all MA161 or equivalent.

[2] t_{PHL} (Reset → Q), t_{PLH} (Set → $\overline{Q}$)

1. Measurement circuit



2. Waveforms



1. Measurement made for each flip flop.
2. C_L includes probe and tool floating capacitance.
3. Diodes are all MA161.

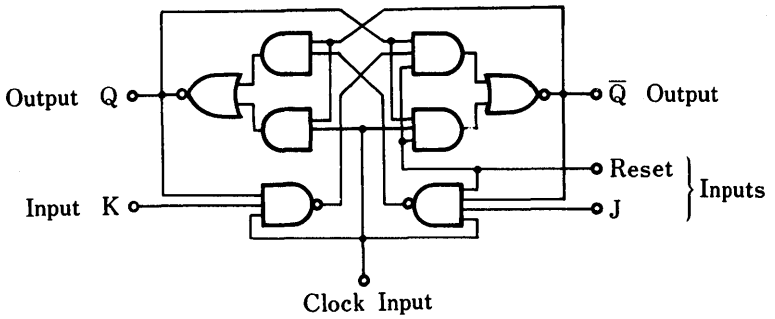
Notes
1. Input waveform: $t_r \leqq 15$ns, $t_f \leqq 6$ns, PRR = 1MHz, duty cycle = 50%.

■ Truth tables

Inputs				Outputs	
Reset	Clock	J	K	Q	$\overline{Q}$
L	×	×	×	L	H
H	↓	L	L	Q_0	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	Toggle	
H	H	×	×	Q_0	$\overline{Q}_0$

Notes
1. H: HIGH voltage level.
2. L: LOW voltage level.
3. ↓: Change from HIGH to LOW.
4. X: Either HIGH or LOW; doesn't matter.
5. Q_0: Q level prior to determination of input condition shown in table.
6. $\overline{Q}_0$: $\overline{Q}$ level prior to determination of input condition shown intable.
7. Toggle: With ↓ change, outputs become compliment of previous condition.

■ Logic diagram (1/2)



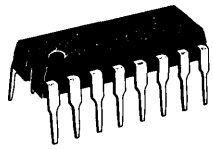
DN74LS109

Dual J-$\overline{K}$ Positive Edge-Triggered Flip-Flops (with Set and Reset)

■ Description

DN74LS109 contains two positive-edge triggered J-K flip-flop circuits, each with independent clock-CP, J, K, and direct-coupled set and reset input terminals.

P-2



16-pin plastic DIL package

P-5

16-pin Panaflat package (SO-16D)

■ Features

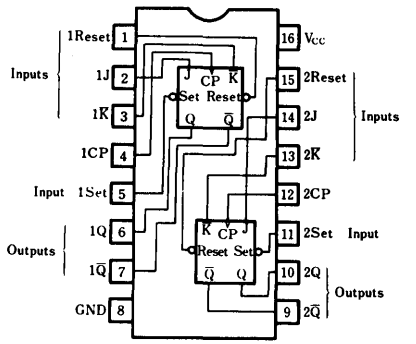
- Positive-edge trigger
- Independent input and output terminals for each flip-flop
- Direct-coupled set and reset inputs
- J and K inputs
- Q and $\overline{Q}$ outputs
- Wide operating temperature range (Ta = −20 to +75°C)

■ Truth tables

Inputs					Outputs	
Set	Reset	Clock	J	$\overline{K}$	Q	$\overline{Q}$
L	H	×	×	×	H	L
H	L	×	×	×	L	H
L	L	×	×	×	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	Toggle	
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	×	×	Q_0	$\overline{Q}_0$

Notes
1. H: HIGH voltage level.
2. L: LOW voltage level.
3. ↑: Change from LOW to HIGH.
4. X: Either HIGH or LOW; doesn't matter.
5. Q_0: Q level prior to determination of input condition shown in table.
6. $\overline{Q}_0$: $\overline{Q}$ level prior to determination of input condition shown in table.
7. Toggle: With ↑ change, outputs become compliment of previous condition.
8. H*: When set and reset are LOW, Q and $\overline{Q}$ are HIGH; however, when set and reset simultaneously change to HIGH, requirements of Q and $\overline{Q}$ cannot be predicted.

Pin configuration (top view)



■ Recommended operating conditions

Parameter		Sym	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}			−400	μA
		I_{OL}			8	mA
Operating temperature range		Topr	−20	25	75	℃
Clock frequency		f_{clock}	0		30	MHz
Pulse width	Clock High	t_w	25			ns
	Set or Reset Low		25			ns
Set-up time	HIGH data	t_{su}	20 ↑			ns
	LOW data		20 ↑			ns
Hold time		t_h	5 ↑			ns

Notes 1. ↑: Indicates rise edge of standard clock pulse.

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter		Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Output voltage		V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$ $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	3.4		V
		V_{OL1}	$V_{CC}=4.75V$ $V_{IH}=2V$ $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
		V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	J-$\overline{K}$	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				20	μA
	Reset						40	μA
	Set						40	μA
	Clock						20	μA
	J-$\overline{K}$	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.4	mA
	Reset						−0.8	mA
	Set						−0.8	mA
	Clock						−0.4	mA
	J-$\overline{K}$	I_I	$V_{CC}=5.25V$ $V_I=5.5V$				0.1	mA
	Reset						0.2	mA
	Set						0.2	mA
	Clock						0.1	mA
Output short circuit current**		I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−100	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current***		I_{CC}	$V_{CC}=5.25V$			4	8	mA

* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.
*** Measured with all outputs open, Q and Q outputs alternately HIGH, and clock inputs grounded.

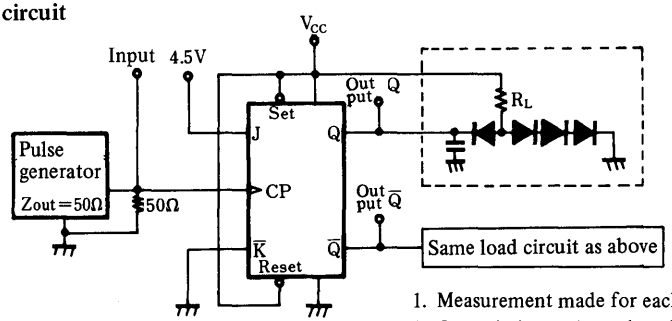
■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Maximum clock frequency	f_{max}			$C_L=15pF$ $R_L=2k\Omega$	25	33		MHz
Propagation delay time	t_{PLH}	Reset Set Clock	Q, $\overline{Q}$			13	25	ns
	t_{PHL}					25	40	ns

※ Switching parameter measurement information

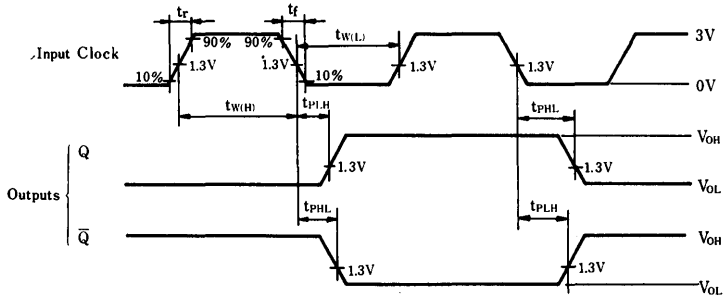
〔1〕 f_{max}, t_{PLH}, t_{PHL} (Clock → Q, $\overline{Q}$)

1. Measurement circuit



1. Measurement made for each flip flop.
2. C_L includes probe and tool floating capacitance.
3. Diodes are all MA161.

2. Waveforms

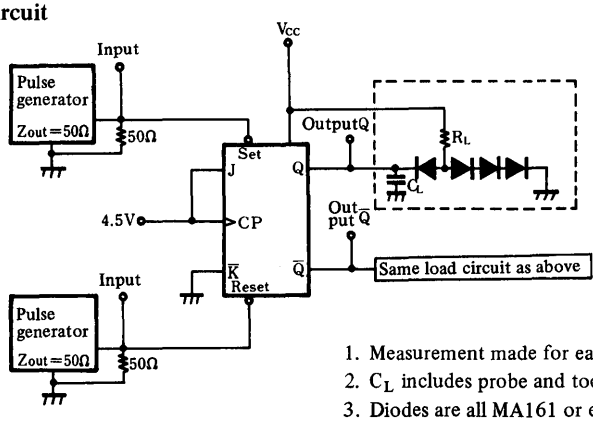


Notes

1. Clock input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR=1MHz, duty cycle 50%
2. When measuring f_{max}, t_r and $t_f \leqq 2.5ns$.

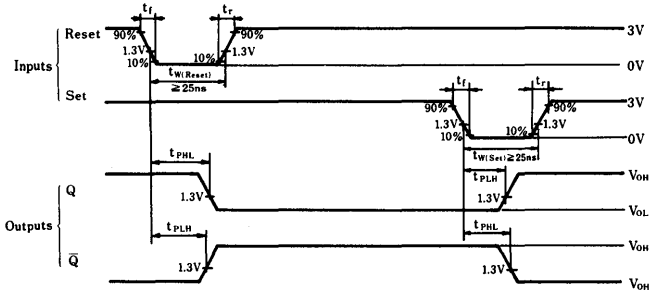
[2] t_{PLH}, t_{PHL}(Reset, Set → Q, $\overline{Q}$)

1. Measurement circuit



1. Measurement made for each flip flop.
2. C_L includes probe and tool floating capacitance.
3. Diodes are all MA161 or equivalent.

2. Waveforms



Notes

1. Set and clock waveforms: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz.

DN74LS112

Dual J-K Negative Edge-Triggered Flip-Flops (with Set and Reset)

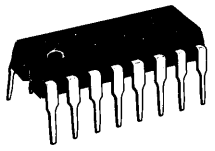
■ Description

DN74LS112 contains two negative-edge triggered J-K flip-flop circuits, each with independent clock-CP, J, K, and direct-coupled set and reset input terminals.

■ Features

- Negative-edge trigger
- Independent input and output terminals for each flip-flop
- Direct-coupled set and reset inputs
- Q and $\overline{Q}$ outputs
- Wide operating temperature range (Ta = −20 to +75°C)

P-2

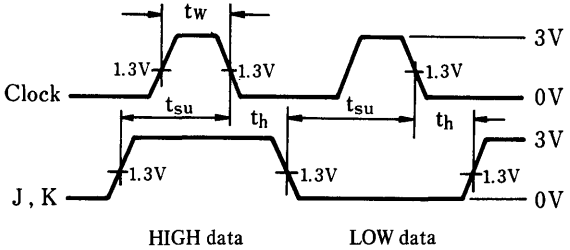


16-pin plastic DIL package

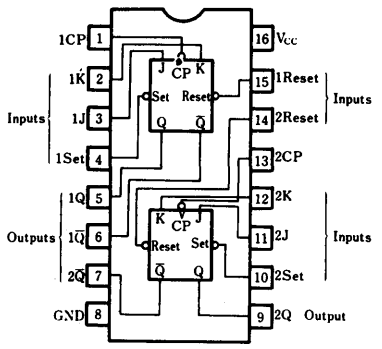
P-5

16-pin Panaflat package (SO-16D)

■ Timing definition



Pin configuration (top view)



■ Recommended operating conditions

Parameter		Sym	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}			−400	μA
		I_{OL}			8	mA
Operating temperature range		Topr	−20	25	75	℃
Clock frequency		f_{clock}	0		30	MHz
Pulse width	Clock High	t_w	25			ns
	Set or Reset Low		25			ns
Set-up time	HIGH data	t_{su}	20 ↓			ns
	LOW data		20 ↓			ns
Hold time		t_h	5 ↓			ns

Notes 1. ↓: Indicates fall edge of standard clock pulse.

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter		Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Output voltage		V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$,	$I_{OH}=-400\mu A$	2.7	3.4		V
		V_{OL1}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
		V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	J-K	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
	Reset						60	μA
	Set						60	μA
	Clock						80	μA
	J-K	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
	Reset						−0.8	mA
	Set						−0.8	mA
	Clock						−0.8	mA
	J-K	I_I	$V_{CC}=5.25V$, $V_I=7V$				0.1	mA
	Reset						0.3	mA
	Set						0.3	mA
	Clock						0.4	mA
Output short circuit current**		I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−100	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$, $I_I=-18mA$				−1.5	V
Supply current***		I_{CC}	$V_{CC}=5.25V$			4.0	8.0	mA

* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.
*** Measured with all outputs open, Q and $\overline{Q}$ outputs alternately HIGH, and clock inputs grounded.

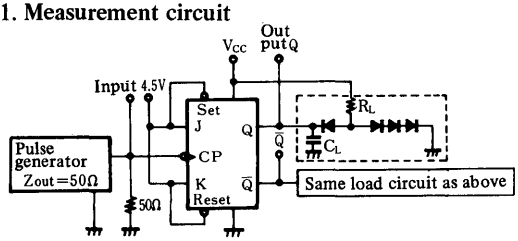
■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

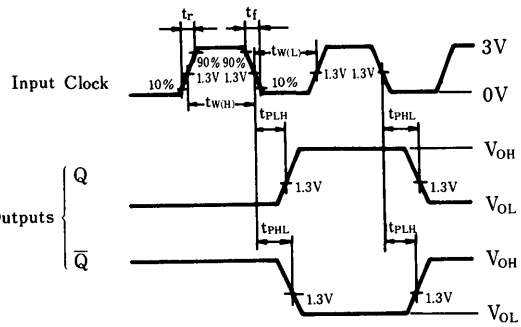
Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Maximum clock frequency	f_{max}			$C_L=15pF$, $R_L=2k\Omega$	30	45		MHz
Propagation delay time	t_{PLH}	Reset, Set, Clock	Q, $\overline{Q}$			11	20	ns
	t_{PHL}					15	30	ns

※ Switching parameter measurement information

〔1〕 f_{max}, t_{PLH}, t_{PHL} (Clock → Q, $\overline{Q}$)

1. Measurement circuit



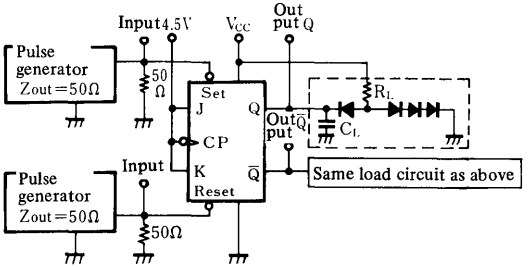


1. Measurement made for each flip flop.
2. C_L includes probe and tool floating capacitance.
3. Diodes are all MA161 or equivalent.

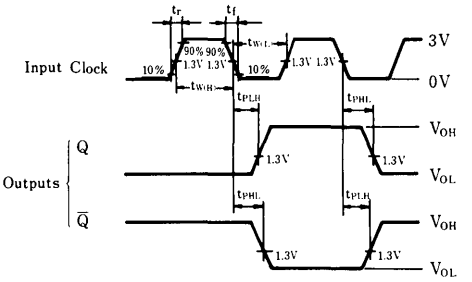
1. Clock input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR=1MHz, duty cycle 50%
2. When measuring f_{max}, t_r and $t_f \leqq 2.5ns$.

〔2〕 t_{PLH}, t_{PHL}(Reset, Set → Q, $\overline{Q}$)

1. Measurement circuit



2. Waveforms



1. Measurement made for each flip flop.
2. C_L includes probe and tool floating capacitance.
3. Diodes are all MA161.

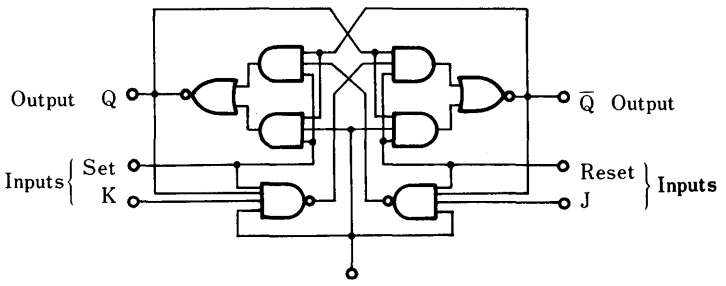
Notes
1. Reset, Set Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR=1MHz

■ Truth tables

Inputs					Outputs	
Set	Reset	Clock	J	K	Q	$\overline{Q}$
L	H	×	×	×	H	L
H	L	×	×	×	L	H
L	L	×	×	×	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	×	×	Q_0	$\overline{Q}_0$

Notes
1. H: HIGH voltage level.
2. L: LOW voltage level.
3. ↓: Change from HIGH to LOW.
4. X: Either HIGH or LOW; doesn't matter.
5. Q_O: Q level prior to determination of input condition shown in table.
6. $\overline{Q}_O$: $\overline{Q}$ level prior to determination of input condition shown in table.
7. Toggle: With ↓ change, outputs become compliment of previous condition.
8. H*: When set and reset are LOW, Q and $\overline{Q}$ are HIGH; however, when set and reset simultaneously change to HIGH, requirements of Q and $\overline{Q}$ cannot be predicted.

■ Logic diagram (1/2)



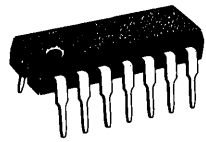
DN74LS113

Dual J-K Negative Edge-Triggered Flip-Flops (with Set)

■ Description

DN74LS113 contains two negative-edge triggered J-K flip-flop circuits, each with independent clock-CP, J, K, and direct-coupled set input terminals.

P-1



14-pin plastic DIL package

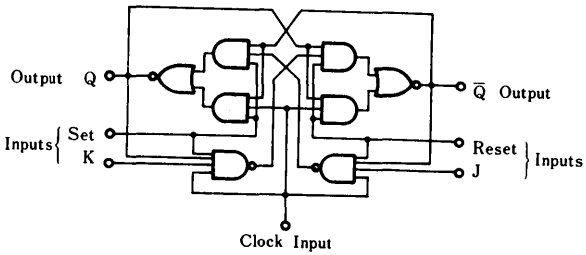
P-4

14-pin Panaflat package (SO-14D)

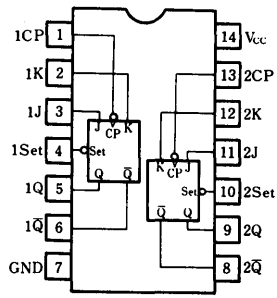
■ Features

- Negative-edge trigger
- Independent input and output terminals for each flip-flop
- Direct-coupled set
- Q and $\overline{Q}$ outputs
- Wide operating temperature range (Ta = −20 to +75°C)

■ Logic diagram (1/2)



Pin configuration (top view)



■ Recommended operating conditions

Parameter		Sym	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}			−400	μA
		I_{OL}			8	mA
Operating temperature range		Topr	−20	25	75	℃
Clock frequency		f_{clock}	0		30	MHz
Pulse width	Clock High	t_w	20			ns
	Set or Reset Low		25			ns
Set-up time	HIGH data	t_{su}	20 ↓			ns
	LOW data		20 ↓			ns
Hold time		t_h	0 ↓			ns

Notes 1. ↓: Indicates fall edge of standard clock pulse.

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter		Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Output voltage		V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$ $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	3.4		V
		V_{OL1}	$V_{CC}=4.75V$ $V_{IH}=2V$ $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
		V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	J-K	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				20	μA
	Set						60	μA
	Clock						80	μA
	J-K	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.4	mA
	Set						−0.8	mA
	J-K						−0.8	mA
	J-K	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.1	mA
	Set						0.3	mA
	Clock						0.4	mA
Output short circuit current**		I_{OS}	$V_{CC}=5.25$ $V_O=0V$		−15		−100	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current***		I_{CC}	$V_{CC}=5.25V$			4	8	mA

* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.
*** Measured with all outputs open, Q and $\overline{Q}$ outputs alternately HIGH, and clock inputs grounded.

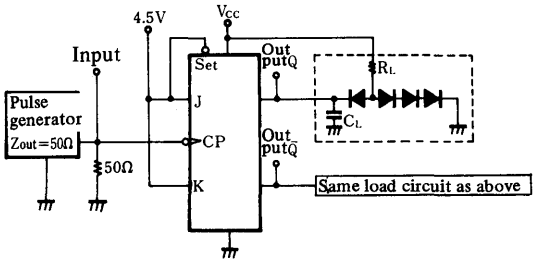
■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Maximum clock frequency	f_{max}			$C_L=15pF$ $R_L=2k\Omega$	30	45		MHz
Propagation delay time	t_{PLH}	Set Clock	Q, $\overline{Q}$			11	20	ns
	t_{PHL}					15	30	ns

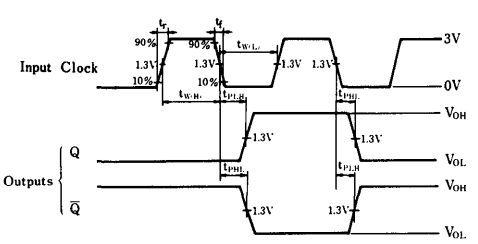
※ Switching parameter measurement information

〔1〕 f_{max}, t_{PLH}, t_{PHL} (Clock → Q, $\overline{Q}$)

1. Measurement circuit



2. Waveforms

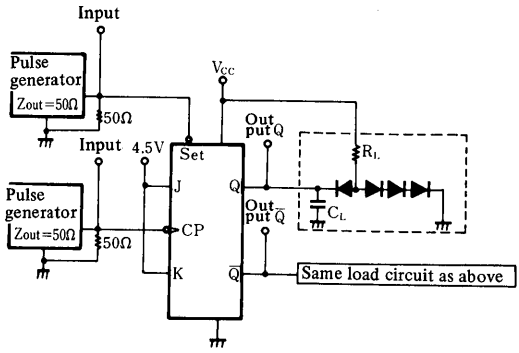


1. Measurement made for each flip flop.
2. C_L includes probe and tool floating capacitance.
3. Diodes are all MA161 or equivalent.

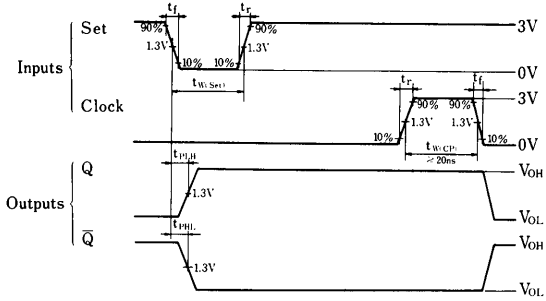
Notes
1. Clock input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR=1MHz, duty cycle 50%
2. When measuring f_{max}, t_r and $t_f \leqq 2.5ns$.

〔2〕 t_{PHL} (Set → $\overline{Q}$), t_{PLH} (Set → $\overline{Q}$)

1. Measurement circuit



2. Waveforms



1. Measurement made for each flip flop.
2. C_L includes probe and tool floating capacitance.
3. Diodes are all MA161.

Notes 1. Set, Clock Input waveform: $t_r \leqq 15$ns, $t_f \leqq 6$ns, PRR=1MHz

■ Truth tables

Inputs				Outputs	
Set	Clock	J	K	Q	$\overline{Q}$
L	×	×	×	H	L
H	↓	L	L	Q_0	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	Toggle	
H	H	×	×	Q_0	$\overline{Q}_0$

Notes
1. H: HIGH voltage level.
2. L: LOW voltage level.
3. X: Either HIGH or LOW; doesn't matter.
4. ↓: Change from HIGH to LOW.
5. Q_0: Q level prior to determination of input condition shown in table.
6. $\overline{Q}_0$: Q level prior to determination of input condition shown intable.
7. Toggle: With ↓ change, outputs become compliment of previous condition.

DN74LS114

Dual J-K Negative Edge-Triggered Flip-Flops (with Set, Common Reset and Common Clock)

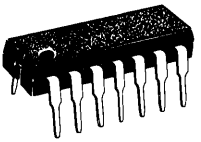
■ Description

DN74LS114 contains two negative-edge triggered J-K flip-flop circuits with common clock-CP and direct-coupled reset input terminals, and independent J, K, and direct-coupled set input terminals.

■ Features

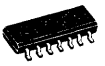
- Negative-edge trigger
- Common clock and direct-coupled reset inputs
- Independent direct-coupled set input
- Q and $\overline{Q}$ outputs
- Wide operating temperature range (Ta = −20 to +75°C)

P-1



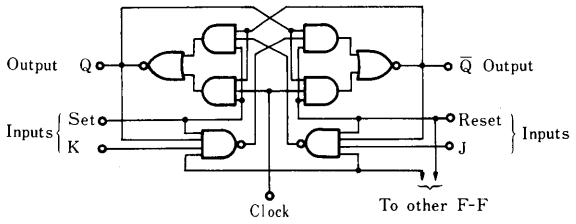
14-pin plastic DIL package

P-4

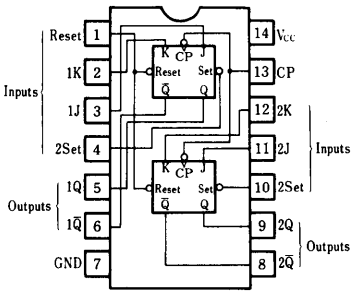


14-pin Panaflat package (SO-14D)

■ Logic diagram (1/2)



Pin configuration (top view)



■ Recommended operating conditions

Parameter		Sym	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}			−400	μA
		I_{OL}			8	mA
Operating temperature range		Topr	−20	25	75	℃
Clock frequency		f_{clock}	0		30	MHz
Pulse width	Clock High	t_w	20			ns
	Set or Reset Low		25			ns
Set-up time	HIGH data	t_{su}	20 ↓			ns
	LOW data		20 ↓			ns
Hold time		t_h	0 ↓			ns

Notes

1. ↓: Indicates fall edge of standard clock pulse.

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter		Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Output voltage		V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	3.4		V
		V_{OL1}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
		V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	J-K	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
	Reset						120	μA
	Set						60	μA
	Clock						160	μA
	J-K	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
	Reset						−1.6	mA
	Set						−0.8	mA
	Clock						−1.6	mA
	J-K	I_I	$V_{CC}=5.25V$, $V_I=7V$				0.1	mA
	Reset						0.6	mA
	Set						0.3	mA
	Clock						0.8	mA
Output short circuit current**		I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−100	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$, $I_I=-18mA$				−1.5	V
Supply current***		I_{CC}	$V_{CC}=5.25V$			4	8	mA

* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.
*** Measured with all outputs open, Q and $\overline{Q}$ outputs alternately HIGH, and clock inputs grounded.

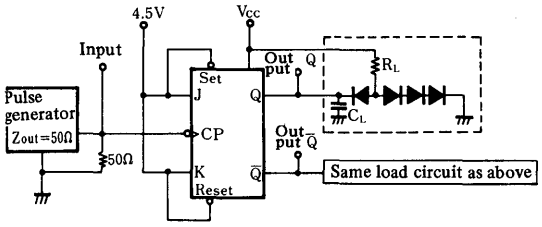
■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Maximum clock frequency	f_{max}			$C_L=15pF$, $R_L=2k\Omega$	30	45		MHz
Propagation delay time	t_{PLH}	Reset, Set, Clock	Q, $\overline{Q}$			11	20	ns
	t_{PHL}					15	30	ns

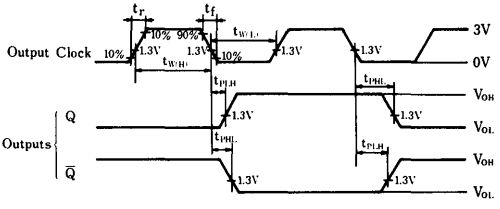
※ Switching parameter measurement information

〔1〕 f_{max}, t_{PLH}, t_{PHL} (Clock → Q, $\overline{Q}$)

1. Measurement circuit



2. Waveforms

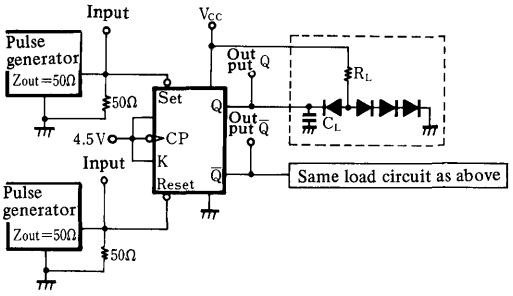


1. Measurement made for each flip flop.
2. C_L includes probe and tool floating capacitance.
3. Diodes are all MA161 or equivalent.

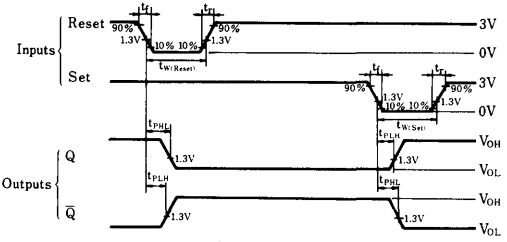
1. Clock input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR=1MHz, duty cycle 50%
2. When measuring f_{max}, t_r and $t_f \leqq 2.5ns$.

〔2〕 t_{PLH}, t_{PHL}(Reset, Set → Q, $\overline{Q}$)

1. Measurement circuit



2. Waveforms



1. Measurement made for each flip flop.
2. C_L includes probe and tool floating capacitance.
3. Diodes are all MA161.

Notes
1. Reset, Set Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR=1MHz

■ Truth tables

Inputs					Outputs	
Set	Reset	Clock	J	K	Q	$\overline{Q}$
L	H	×	×	×	H	L
H	L	×	×	×	L	H
L	L	×	×	×	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	×	×	Q_0	$\overline{Q}_0$

Notes
1. H: HIGH voltage level.
2. L: LOW voltage level.
3. X: Either HIGH or LOW; doesn't matter.
4. ↓: Change from HIGH to LOW.
5. Q_0: Q level prior to determination of input condition shown in table.
6. $\overline{Q}_0$: $\overline{Q}$ level prior to determination of input condition shown intable.
7. Toggle: With ↓ change, outputs become compliment of previous condition.
8. H*: When set and reset are LOW, Q and $\overline{Q}$ are HIGH; however, when set and reset simultaneously change to HIGH, requirements of Q and $\overline{Q}$ cannot be predicted.

DN74LS123

Dual Retriggerable Monostable Multivibrators (with Reset)

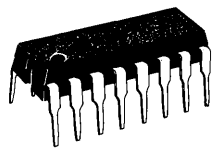
■ Description

DN74LS123 contains two retriggerable monostable multivibrator circuits with direct-coupled reset input terminals.

■ Features

- Retriggerable for long output pulse width generation capability
- Direct-coupled reset input for output pulse interruption capability
- Complementary A and B inputs
- Q and $\overline{Q}$ outputs
- Wide operating temperature range (Ta = −20 to +75°C)

P-2

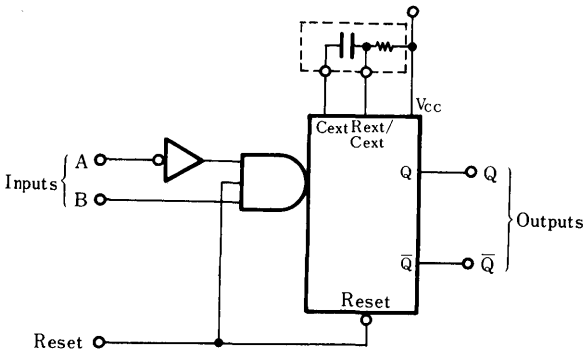


16-pin plastic DIL package

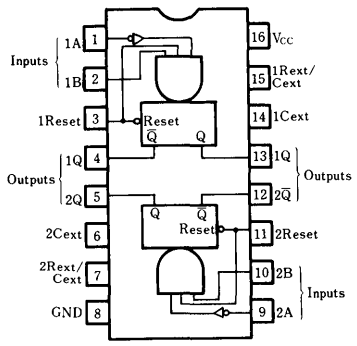
P-5

16-pin Panaflat package (SO-16D)

■ Logic diagram (1/2)



Pin configuration (top view)



■ Recommended operating conditions

Parameter			Sym	Min	Typ	Max	Unit
Supply voltage			V_{CC}	4.75	5.00	5.25	V
Output current			I_{OH}			−400	μA
			I_{OL}			8	mA
Operating temperature range			Topr	−20	25	75	℃
Input pulse width	A, B	"H"	$t_{w(in)}$	40			ns
		"L"		40			ns
	Reset	"L"		40			ns
External timing resistance			Rext	5		260	kΩ
External capacitance			Cext	Unlimited			
Wiring capacitance (R_{ext}/C_{ext} terminals)						50	pF

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$ $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	3.4		V
	V_{OL1}	$V_{CC}=4.75V$ $V_{IH}=2V$ $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
	V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				20	μA
	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.4	mA
	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.1	mA
Output short circuit current**	I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−100	mA
Input clamp voltage	V_{IK}	$V_{CC}=5.25V$, $I_I=-18mA$				−1.5	V
Supply current***	I_{CC}	$I_{CC}=5.25V$			12	20	mA

* When constant at V_{CC} = 5V, Ta = 25°C.

** V_{OH} of Q, V_{OL} of $\overline{Q}$, and I_{OS} of Q are measured with R_{ext}/C_{ext} grounded, 2V applied to B and reset inputs, and a pulse from 2V to 0V then applied to A.

*** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

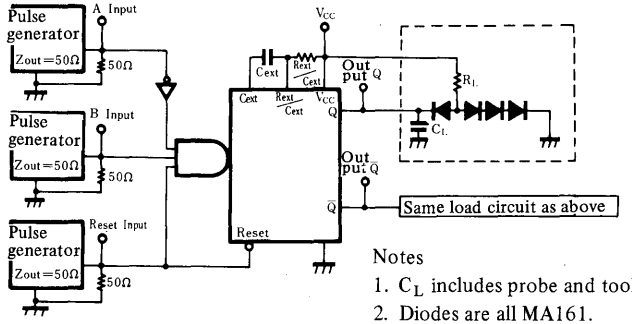
**** I_{CC} is measured with all outputs open and 4.5V applied to reset and B inputs; also, A input is grounded momentarily, following which 4.5V is applied to it.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	A	Q	$C_{ext}=0pF$ $R_{ext}=5K\Omega$ $C_L=15pF$ $R_L=2k\Omega$		23	33	ns
	t_{PHL}		$\overline{Q}$			23	45	
	t_{PLH}	B	Q			32	44	
	t_{PHL}		$\overline{Q}$			34	56	
	t_{PLH}	Reset	Q			20	27	
	t_{PHL}		$\overline{Q}$			28	45	
Minimum output pulse width	$t_W(out)min$	A, B	Q			116	200	
Output pulse width	$t_W(out)$			$C_{ext}=1000pF$, $R_L=2k\Omega$ $R_{ext}=10k\Omega$, $C_L=15pF$	4	4.5	5	μs

※ Switching parameter measurement information

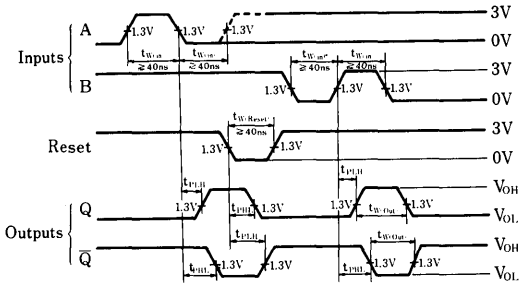
1. Measurement circuit



Notes

1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161.

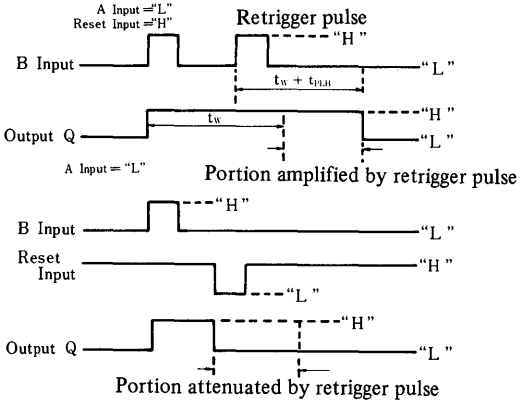
2. Waveforms (A, B, R_{reset} → Q, $\overline{Q}$)



Notes

1. Input waveform: $t_r \geqq 15ns$, $t_f \geqq 6ns$, (10% — 90%)

■ Typical examples of responses to output pulses



■ Truth tables

Inputs			Outputs	
Reset	A	B	Q	$\overline{Q}$
L	×	×	L	H
×	H	×	L	H
×	×	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

Notes
1. H: HIGH voltage level.
2. L: LOW voltage level.
3. ↓: Change from HIGH to LOW.
4. ↑: Change from LOW to HIGH.
5. X: Either HIGH or LOW; doesn't matter.
6. ⎍ : One HIGH level pulse.
7. ⎎ : One LOW level pulsse.
8. External timing capacitance is connected between C_{ext} and R_{ext}/C_{ext}.

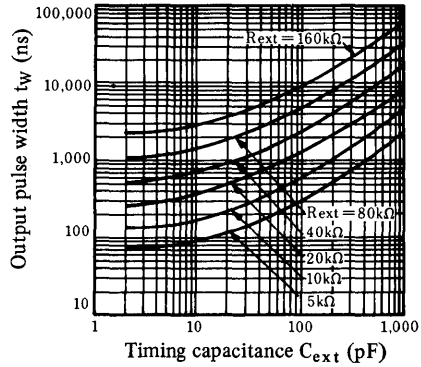
■ Typical function example

The basic output pulse width is determined by the externally connected capacitance and timing resistance.

※ Timing component connection method

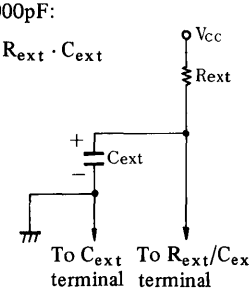
(1) When $C_{ext} \leqq 1000pF$ (refer to the illustration below):

* Output pulse width verses timing capacitance ($C_{ext} \leqq 1000pF$)



(2) When $C_{ext} \leqq 1000pF$:

$t_{W(ext)} = 0.45 \cdot R_{ext} \cdot C_{ext}$



DN74LS125A

Quad Bus Buffer Gates (with 3-state Outputs)

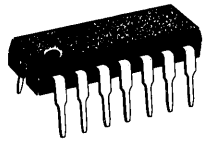
■ Description

DN74LS125A contains four 3-state output buffer gate circuits, each with independent output-control input-C terminals.

■ Features

- All 4 circuits have independent output-control inputs
- Low power consumption (P_d = 55mW typical)
- High speed (t_{pd} = 8ns typical)
- Wide operating temperature range (Ta = –20 to +75°C)

P-1



14-pin plastic DIL package

P-4

14-pin Panaflat package (SO-14D)

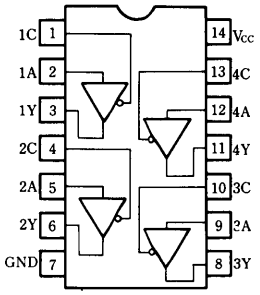
■ Truth tables

Inputs		Outputs
C	A	Y
H	×	Z
L	L	L
L	H	H

Notes

1. H: HIGH voltage level.
2. L: LOW voltage level.
3. X: Either HIGH or LOW; doesn't matter.
4. Z: High impedance.

Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−2.6	mA
	I_{OL}			24	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$ $V_{IL}=0.8V$, $I_{OH}=-2.6mA$		2.4	3.4		V
	V_{OL1}	$V_{CC}=4.75V$ $V_{IH}=2V$ $V_{IL}=0.8V$	$I_{OL}=12mA$		0.25	0.4	V
	V_{OL2}		$I_{OL}=24mA$		0.35	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				20	μA
	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.4	mA
	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.1	mA
Output OFF current	I_{OZ1}	$V_{CC}=5.25V$ $V_{IH}=2V$ $V_{IL}=0.8V$	$V_O=0.4V$			−20	μA
	I_{OZ2}		$V_O=2.4V$			20	μA
Output short circuit current**	I_{OS}	$V_{CC}=5.25V$ $V_O=0V$		−15		−130	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current***	I_{CC}	$V_{CC}=5.25V$			11	20	mA

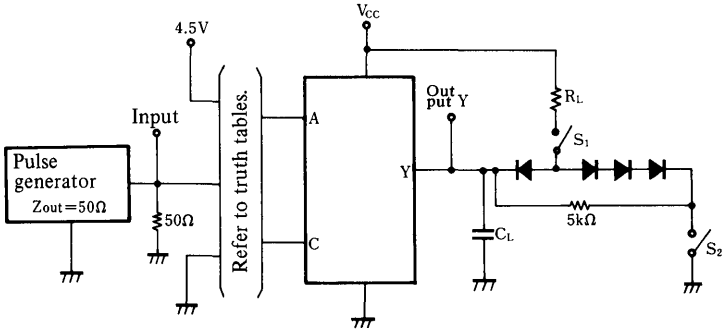
* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	$C_L=45pF$ $R_L=667Ω$		9	15	ns
	t_{PHL}			7	18	ns
Output enable time	t_{PZH}			12	20	ns
	t_{PZL}			15	25	ns
Output disable time	t_{PHZ}	$C_L=5pF$ $R_L=667Ω$			20	ns
	t_{PLZ}				20	ns

※ Switching parameter measurement information

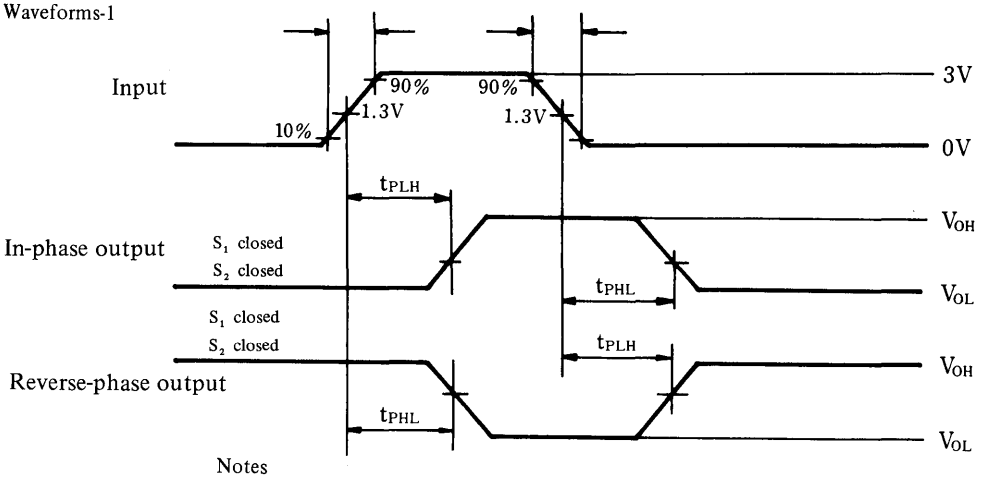
1. Measurement circuit



Notes
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161.

2. Waveforms

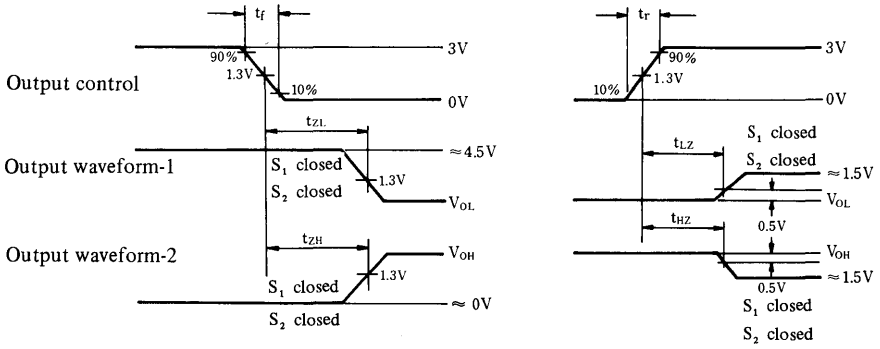
Waveforms-1



Notes

1. Reset, Set Input waveform: $t_r \leqq 15$ ns, $t_f \leqq 6$ ns, PRR = 1MHz

Waveforms-2



Notes

1. Input waveform: $t_r \leqq 15$ns, $t_f \leqq 6$ns, PRR = 1MHz, duty cycle = 50%.
2. Except when the output is disabled by the output control, output waveform-1 occurs as a result of internal conditions such as a LOW voltage level.
3. Except when the output is disabled by the output control, output waveform-2 occurs as a result of internal conditions such as a HIGH voltage level.
4. When measuring t_{PLH} and t_{PHL}, S_1 and S_2 are ON.

DN74LS132

Quad 2-input Positive NAND Schmitt-Triggers

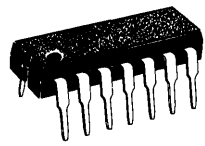
■ Description

DN74LS132 contains four 2-input positive-logic NAND gate circuits with Schmitt triggers.

■ Features

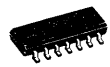
- Ideal for waveform shaping
- Wide hysteresis width (0.8V typical) and high noise margin
- Low power consumption (P_d = 35mW typical)
- High speed (t_{pd} = 15ns typical)
- Wide operating temperature range (Ta = −20 to +75°C)

P-1



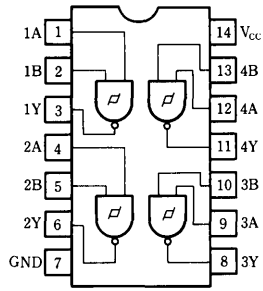
14-pin plastic DIL package

P-4



14-pin Panaflat package (SO-14D)

Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−400	μA
	I_{OL}			8	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input threshold voltage	V_T+	$V_{CC}=5V$		1.4	1.6	1.9	V
	V_T-	$V_{CC}=5V$		0.5	0.8	1.0	V
Hysteresis width	V_T+-V_T-	$V_{CC}=5V$		0.4	0.8		V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_I=0.5V$ $I_{OH}=-400\mu A$		2.7	3.4		V
	V_{OL1}	$V_{CC}=4.75V$ $V_I=1.9V$	$I_{OL}=4mA$		0.25	0.4	V
	V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input threshold current	I_T+	$V_{CC}=5V$ $V_I=V_T+$			−0.14		mA
	I_T-	$V_{CC}=5V$ $V_I=V_T-$			−0.18		mA
Input current	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				20	μA
	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.4	mA
	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.1	mA
Output short circuit current**	I_{OS}	$V_{CC}=5.25V$ $V_O=0V$		−15		−100	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current	I_{CCH}	$V_{CC}=5.25V$,			5.9	11	mA
	I_{CCL}	$V_{CC}=5.25V$,			8.2	14	mA

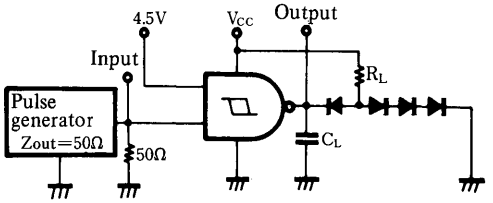
* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	$C_L=15pF$ $R_L=2k\Omega$		15	22	ns
	t_{PHL}			15	22	ns

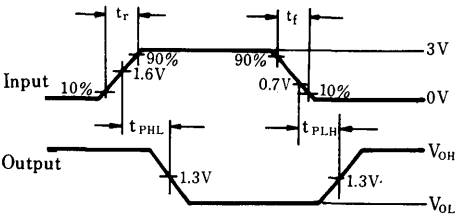
※ Switching parameter measurement information

1. Measurement circuit



Notes
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161 or equivalent.

2. Waveforms



Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.

DN74LS136

Quad 2-input Exclusive OR Gates (with Open Collector Outputs)

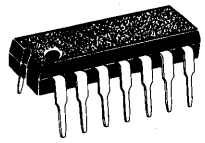
■ Description

DN74LS136 contains four 2-input exclusive OR gate circuits with open collector outputs.

■ Features

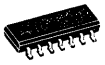
- "Wired" AND capability
- Low power consumption (P_d = 30.5mW typical)
- High speed (t_{pd} = 18ns typical)
- Wide operating temperature range (Ta = −20 to +75°C)

P-1



14-pin plastic DIL package

P-4



14-pin Panaflat package (SO-14D)

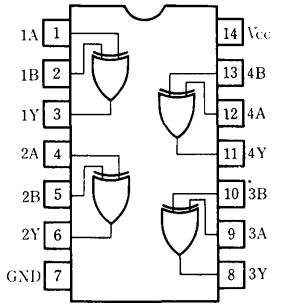
■ Truth tables

Inputs		Outputs
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

Notes

1. H: HIGH voltage level.
2. L: LOW voltage level.

Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
HIGH level output voltage	V_{OH}			5.5	V
LOW level output voltage	I_{OL}			8	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output current	I_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$ $V_{IL}=0.8V$, $V_{OH}=5.5V$				100	μA
Output voltage	V_{OL1}	$V_{CC}=4.75V$ $V_{IH}=2V$ $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
	V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				40	μA
	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.8	mA
	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.2	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current**	I_{CC}	$V_{CC}=5.25V$			6.1	10	mA

* When constant at V_{CC} = 5V, Ta = 25°C.

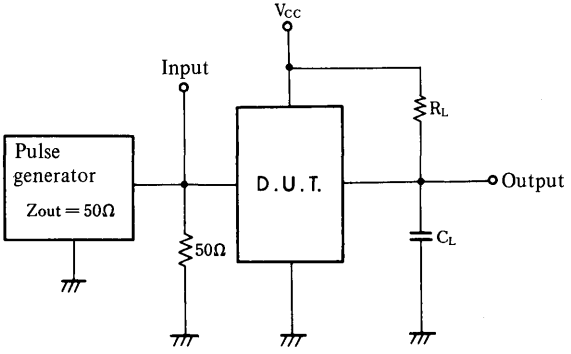
** I_{CC} is measured with all outputs open and 4.5V applied to one side of each gate while the other side is grounded.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Test conditions		Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	A or B	Other input = LOW	$C_L=15pF$ $R_L=2K\Omega$		18	30	ns
	t_{PHL}					18	30	
	t_{PLH}	A or B	Other input = HIGH			18	30	ns
	t_{PHL}					18	30	

※ Switching parameter measurement information

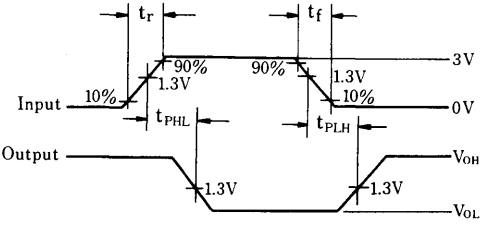
1. Measurement circuit



Notes

1. C_L includes probe and tool floating capacitance.

2. Waveforms



Notes

1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR=1MHz duty cycle 50%

DN74LS138

3-line to 8-line Decoders / Demultiplexers

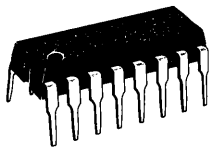
■ Description

DN74LS138 is a 3-bit decimal to octal decoder/demultiplexer with enable inputs.

■ Features

- Three types of enable inputs
- Quaternary to hexadecimal decoder/demultiplexer capability with no externally connected parts
- Wide operating temperature range (Ta = −20 to +75°C)

P-2

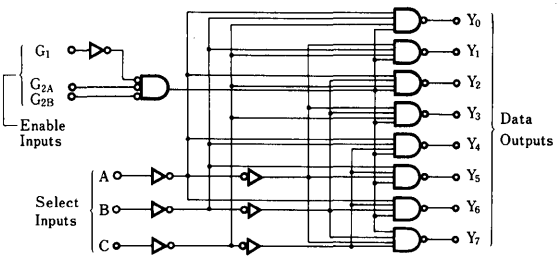


16-pin plastic DIL package

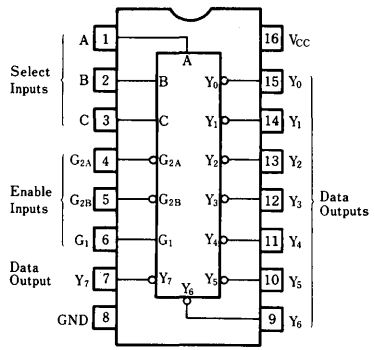
P-5

16-pin Panaflat package (SO-16D)

■ Logic diagram



Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−400	μA
	I_{OL}			8	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$ $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	3.4		V
	V_{OL1}	$V_{CC}=4.75V$ $V_{IH}=2V$ $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
	V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				20	μA
	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.4	mA
	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.1	mA
Output short circuit current**	I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−100	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current***	I_{CC}	$I_{CC}=5.25V$			6.3	10	mA

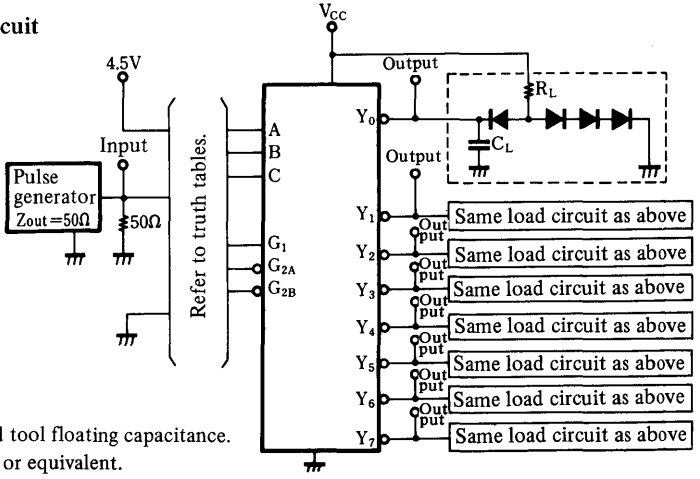
* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.
*** Measured with all outputs open and in enable condition.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Outputs	Delay level	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	Binary Seleet A, B, C	Y	2	$C_L=15pF$ $R_L=2k\Omega$		13	20	ns
	t_{PHL}						27	41	ns
	t_{PLH}			3			18	27	ns
	t_{PHL}						26	39	ns
	t_{PLH}	Enable G_{2A}, G_{2B}	Y	2			12	18	ns
	t_{PHL}						21	32	ns
	t_{PLH}	Enable G_1		3			17	26	ns
	t_{PHL}						25	38	ns

※ Switching parameter measurement information

1. Measurement circuit

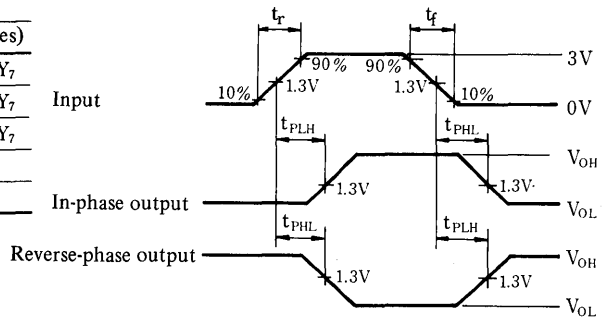


Notes
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161 or equivalent.

2. Relationships of inputs/outputs to delay level

Input	Output							
	Delay level (2-stages)				Delay level (3-stages)			
A	Y_0	Y_2	Y_4	Y_6	Y_1	Y_3	Y_5	Y_7
B	Y_0	Y_1	Y_4	Y_5	Y_2	Y_3	Y_6	Y_7
C	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
G_1					$Y_0 \sim Y_7$			
G_{2A}, G_{2B}	$Y_0 \sim Y_7$							

3.Waveforms



Notes

1. Input waveform: $t_r \leqq 15$ns, $t_f \leqq 6$ns, PRR = 1MHz, duty cycle = 50%.

■ Truth tables

Inputs					Outputs							
Enable		Select										
G_1	G_2*	C	B	A	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
×	H	×	×	×	H	H	H	H	H	H	H	H
L	×	×	×	×	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

Notes

1. * $G_2 = G_{2A} + G_{2B}$
2. H: HIGH voltage level.
   L: LOW voltage level.
   X: Either HIGH or LOW; doesn't matter.

DN74LS139

Dual 2-line to 4-line Decoders / Demultiplexers

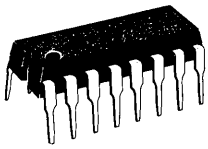
■ Description

DN74LS139 contains two 2-bit binary to quaternary decoder/demultiplexer circuits, each with independent enable input terminals.

■ Features

- Enable inputs
- Both circuits completely independent
- Wide operating temperature range (Ta = −20 to +75°C)

P-2



16-pin plastic DIL package

P-5

16-pin Panaflat package (SO-16D)

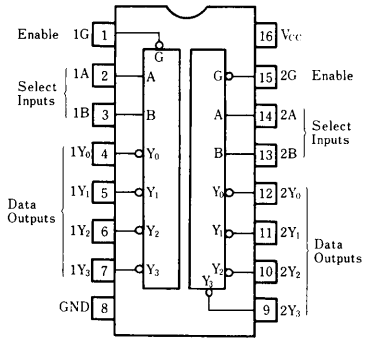
■ Truth tables

Inputs			Outputs			
Enable	Select					
G	B	A	Y_0	Y_1	Y_2	Y_3
H	×	×	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

Notes

1. H: HIGH voltage level.
2. L: LOW voltage level.
3. X: Either HIGH or LOW; doesn't matter.

Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−400	μA
	I_{OL}			8	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$ $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	3.4		V
	V_{OL1}	$V_{CC}=4.75V$ $V_{IH}=2V$ $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
	V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				20	μA
	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.4	mA
	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.1	mA
Output short circuit current**	I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−100	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current***	I_{CC}	$I_{CC}=5.25V$			6.8	11	mA

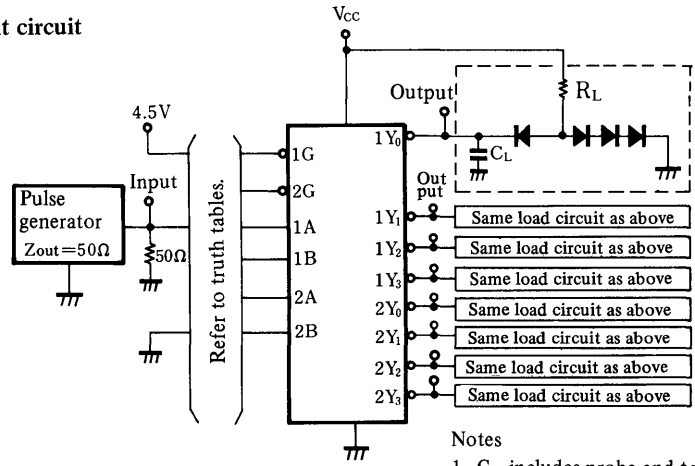
* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.
*** Measured with all outputs open and all inputs grounded.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Outputs	Delay level	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	Binary select 1A, 1B 2A, 2B	$1Y_0 \sim 1Y_3$ $2Y_0 \sim 2Y_3$	2	$C_L=15pF$ $R_L=2k\Omega$		13	20	ns
	t_{PHL}						22	33	ns
	t_{PLH}			3			18	29	ns
	t_{PHL}						25	38	ns
	t_{PLH}	Enable 1G, 2G	$1Y_0 \sim 1Y_3$ $2Y_0 \sim 2Y_3$	2			16	24	ns
	t_{PHL}						21	32	ns

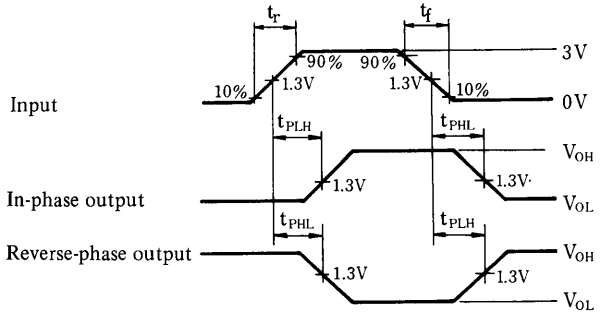
※ Switching parameter measurement information

1. Measurement circuit



Notes
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161 or equivalent.

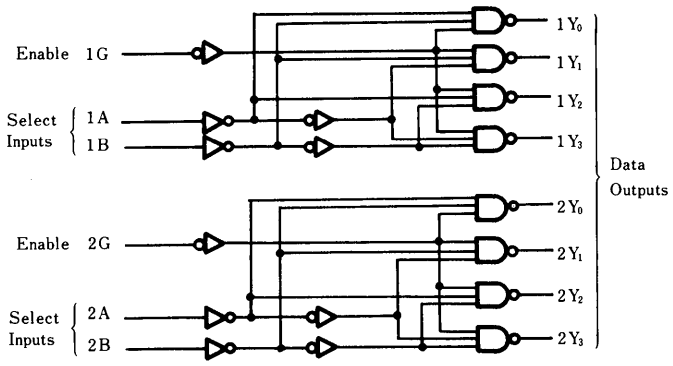
2. Waveforms



Notes

1. Input waveform: $t_r \leqq 15$ns, $t_f \leqq 6$ns, PRR = 1MHz, duty cycle = 50%.

■ Logic diagram



DN74LS145

BCD to Decimal Decoders / Drivers

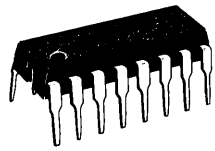
■ Description

DN74LS145 is a BCD to decimal decoder/ driver with open collector outputs.

■ Features

- Large output current ($I_{OL} \leq 80mA$ maximum)
- High withstand voltage level ($V_O \leq 15V$ maximum)
- All output become HIGH during invalid input
- Wide operating temperature range (Ta = −20 to +75°C)

P-2

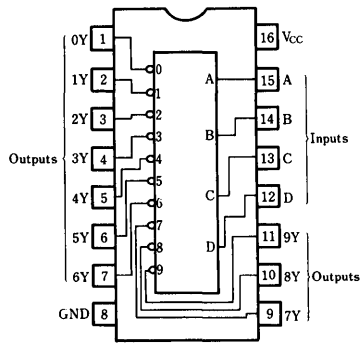


16-pin plastic DIL package

P-5

16-pin Panaflat package (SO-16D)

Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output voltage	$V_{O(off)}$			15	V
Output current	I_{OL}			80	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics (Ta=−20～+75℃)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output current	$I_{O(off)}$	V_{CC}=4.75V, V_{IH}=2V V_{IL}=0.8V, $V_{O(off)}$=15V				250	μA
Output voltage	$V_{O(on)}$	V_{CC}=4.75V V_{IH}=2V V_{IL}=0.8V	I_{OL}=12mA		0.25	0.4	V
			I_{OL}=24mA		0.35	0.5	V
			I_{OL}=80mA		2.3	3.0	V
Input current	I_{IH}	V_{CC}=5.25V V_I=2.7V				20	μA
	I_{IL}	V_{CC}=5.25V V_I=0.4V				−0.4	mA
	I_I	V_{CC}=5.25V V_I=7V				0.1	mA
Input clamp voltage	V_{IK}	V_{CC}=4.75V I_I=−18mA				−1.5	V
Supply current**	I_{CC}	V_{CC}=5.25V			7	13	mA

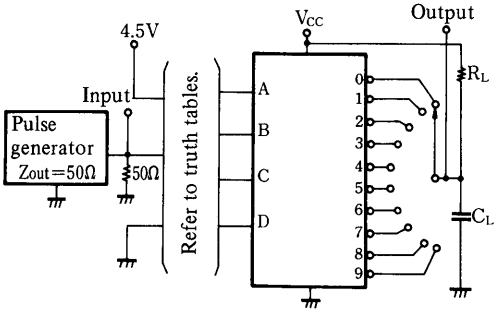
* When constant at V_{CC} = 5V, Ta = 25°C.
** Measured with all outputs open and all inputs grounded.

■ Switching characteristics (V_{CC}=5V, Ta=25℃)

Parameter	Sym	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	C_L=45pF R_L=665Ω			50	ns
	t_{PHL}				50	

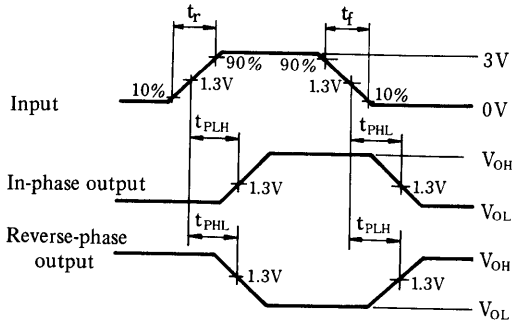
※ Switching parameter measurement information

1. Measurement circuit



Notes
1. C_L includes probe and tool floating capacitance.

2. Waveforms



Notes
1. Input waveform: $t_r \leqq 15$ns, $t_f \leqq 6$ns, PRR = 1MHz, duty cycle = 50%.

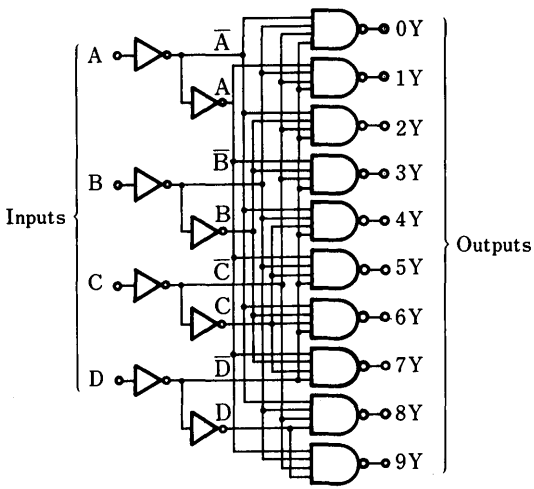
■ Truth tables

No.	Inputs				Outputs									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

Notes

1. H: HIGH voltage level.
2. L: LOW voltage level.

■ Logic diagram



DN74LS151

8-line to 1-line Data Selectors / Multiplexers

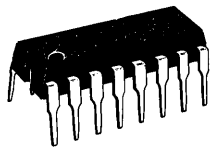
■ Description

DN74LS151 is an 8-line to 1-line data selector/multiplexer.

■ Features

- Enable input
- Complementary outputs
- Low output impedance
- Wide operating temperature range (Ta = −20 to +75°C)

P-2

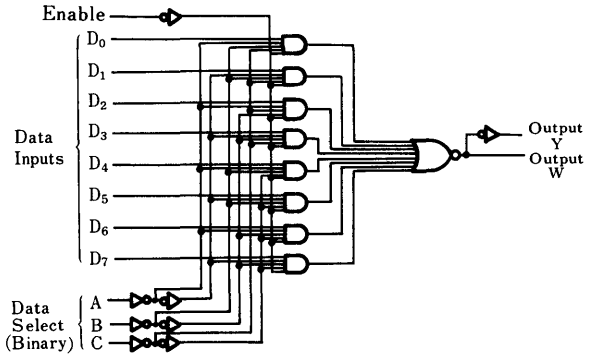


16-pin plastic DIL package

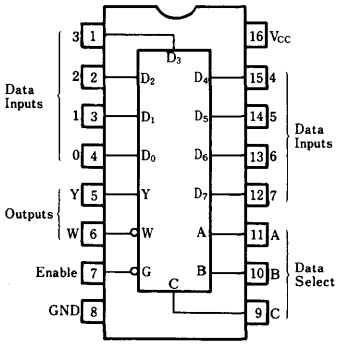
P-5

16-pin Panaflat package (SO-16D)

■ Logic diagram



Pin configuration (top view)



■ Recommended operating conditions

Parameter	記号	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−400	μA
	I_{OL}			8	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	3.4		V
	V_{OL1}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
	V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
	I_I	$V_{CC}=5.25V$, $V_I=7V$				0.1	mA
Output short circuit current**	I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−100	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$, $I_I=-18mA$				−1.5	V
Supply current***	I_{CC}	$I_{CC}=5.25V$			6	10	mA

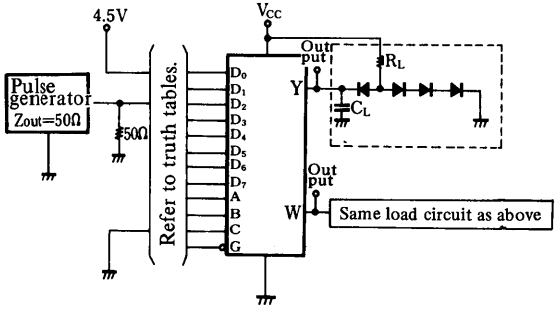
* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.
*** Measured with all outputs open and 4.5V applied to all inputs.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	A, B, C (4 levels)	Y	$C_L=15pF$, $R_L=2k\Omega$		27	43	ns
	t_{PHL}					18	30	ns
	t_{PLH}	A, B, C (3 levels)	W			14	23	ns
	t_{PHL}					20	32	ns
	t_{PLH}	Enable	Y			26	42	ns
	t_{PHL}					20	32	ns
	t_{PLH}	Enable	W			15	24	ns
	t_{PHL}					18	30	ns
	t_{PLH}	D	Y			20	32	ns
	t_{PHL}					16	26	ns
	t_{PLH}	D	W			13	21	ns
	t_{PHL}					12	20	ns

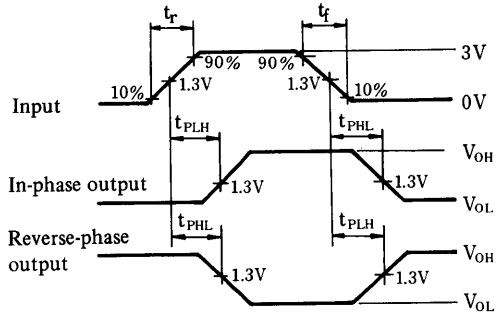
※ Switching parameter measurement information

1. Measurement circuit



Notes
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161 or equivalent.

2. Waveforms



Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.

■ Truth tables

Inputs				Outputs	
Select			Enable	Y	W
C	B	A	S		
×	×	×	H	L	H
L	L	L	L	D_0	$\overline{D}_0$
L	L	H	L	D_1	$\overline{D}_1$
L	H	L	L	D_2	$\overline{D}_2$
L	H	H	L	D_3	$\overline{D}_3$
H	L	L	L	D_4	$\overline{D}_4$
H	L	H	L	D_5	$\overline{D}_5$
H	H	L	L	D_6	$\overline{D}_6$
H	H	H	L	D_7	$\overline{D}_7$

Notes

1. H: HIGH voltage level.
2. L: LOW voltage level.
3. X: Either HIGH or LOW; doesn't matter.

DN74LS153

Dual 4-line to 1-line Data Selectors / Multiplexers

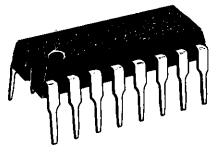
■ Description

DN74LS153 contains two 4-line to 1-line data selector/ multiplexer circuits.

■ Features

- Independent enable input for each circuit
- Common selection input for both circuits
- Low output impedance
- Wide operating temperature range (Ta = −20 to +75°C)

P-2

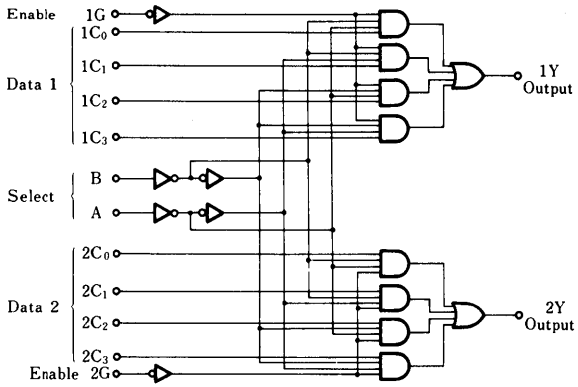


16-pin plastic DIL package

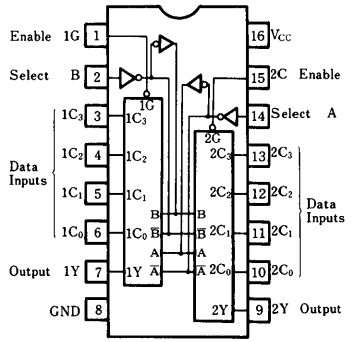
P-5

16-pin Panaflat package (SO-16D)

■ Logic diagram



Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−400	μA
	I_{OL}			8	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$ $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	3.4		V
	V_{OL1}	$V_{CC}=4.75V$ $V_{IH}=2V$ $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
	V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				20	μA
	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.4	mA
	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.1	mA
Output short circuit current**	I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−100	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current***	I_{CC}	$I_{CC}=5.25V$			6.2	10	mA

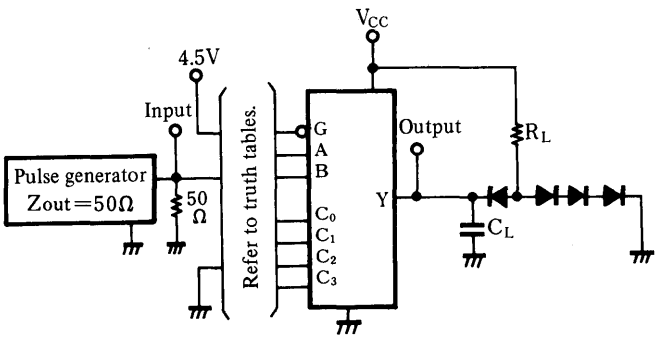
* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.
*** Measured with all outputs open and all inputs grounded.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	Data	Y	$C_L=15pF$ $R_L=2k\Omega$		10	15	ns
	t_{PHL}					17	26	ns
	t_{PLH}	Select	Y			19	29	ns
	t_{PHL}					25	38	ns
	t_{PLH}	Enable	Y			16	24	ns
	t_{PHL}					21	32	ns

※ Switching parameter measurement information

1. Measurement circuit (1/2)



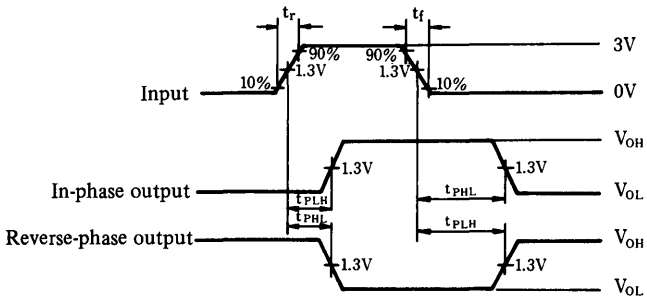
Notes
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161.

2. Table of measurement conditions

Parameter	Inputs							Outputs
	B	A	C_0	C_1	C_2	C_3	G	Y
t_{PLH} t_{PHL}	GND	GND	IN	×	×	×	GND	OUT
	GND	4.5V	×	IN	×	×	GND	OUT
	4.5V	GND	×	×	IN	×	GND	OUT
	4.5V	4.5V	×	×	×	IN	GND	OUT
	GND	IN	GND	4.5V	×	×	GND	OUT
			4.5V	GND				
	IN	GND	GND	×	4.5V	×	GND	OUT
			4.5V		GND			
	GND	GND	4.5V	×	×	×	IN	OUT

Note 1. X: Either HIGH or LOW; doesn't matter.

3.Waveforms



Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR=1MHz, duty cycle 50%

■ Truth tables

Inputs							Outputs
Select		Data				Enable	Y
B	A	C_0	C_1	C_2	C_3	G	
×		×	×	×	×	H	L
L	L	L	×	×	×	L	L
L	L	H	×	×	×	L	H
L	H	×	L	×	×	L	L
L	H	×	H	×	×	L	H
H	L	×	×	L	×	L	L
H	L	×	×	H	×	L	H
H	H	×	×	×	L	L	L
H	H	×	×	×	H	L	H

Notes 1. H: HIGH voltage level.
2. L: LOW voltage level.
3. X: Either HIGH or LOW; doesn't matter.

DN74LS155

Dual 2-line to 4-line Decoders / Demultiplexers

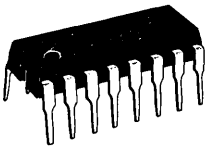
■ Description

DN74LS155 contains two 2-bit binary to quarternary decoder/demultiplexer circuits.

■ Features

- Low output impedance
- Enable inputs
- Capability for composition of 8-bit output decoder/ demultiplexer without connection of external gate
- Wide operating temperature range (Ta = −20 to +75°C)

P-2

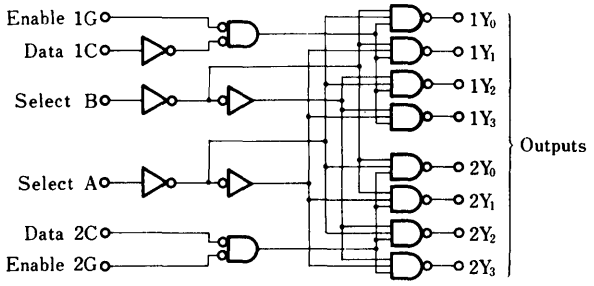


16-pin plastic DIL package

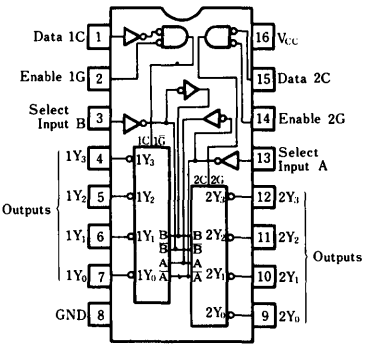
P-5

16-pin Panaflat package (SO-16D)

■ Logic diagram



Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−400	μA
	I_{OL}			8	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	3.4		V
	V_{OL1}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
	V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
	I_I	$V_{CC}=5.25V$, $V_I=7V$				0.1	mA
Output short circuit current**	I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−100	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$, $I_I=-18mA$				−1.5	V
Supply current***	I_{CC}	$I_{CC}=5.25V$			6.1	10	mA

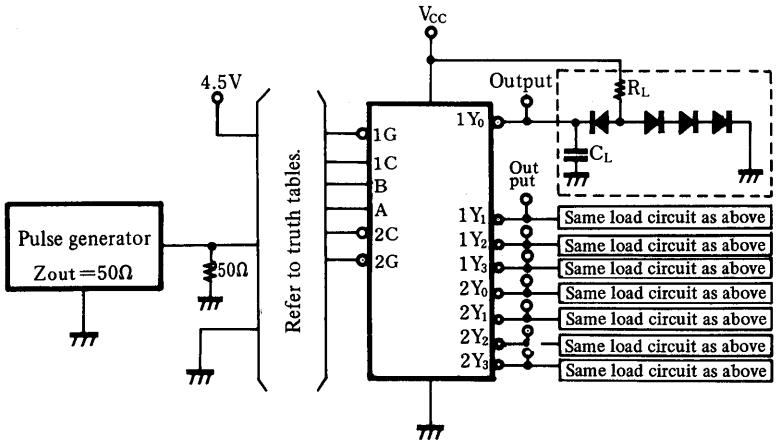
* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.
*** Measured with all outputs open, 4.5V applied to A, B, and 1C inputs, and 2C, 1G, and 2G inputs grounded.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Outputs	Delay level	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	A, B, 2C 1G or 2G	Y	2	$C_L=15pF$, $R_L=2k\Omega$		10	15	ns
	t_{PHL}						19	30	ns
	t_{PLH}	A or B	Y	3			17	26	ns
	t_{PHL}						19	30	ns
	t_{PLH}	1C	Y	3			18	27	ns
	t_{PHL}						18	27	ns

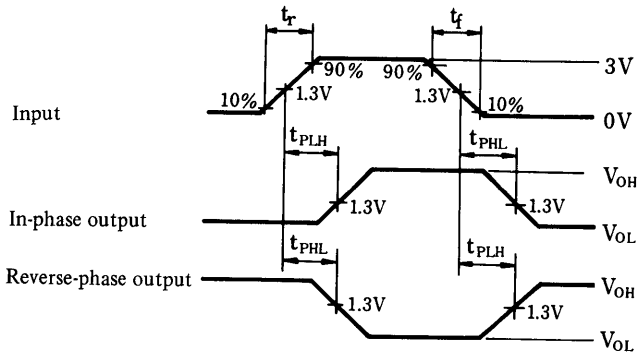
※ Switching parameter measurement information

1. Measurement circuit



Notes
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161 or equivalent.

2. Waveforms



Notes
1. Input waveform: $t_r \leqq 15$ns, $t_f \leqq 6$ns, PRR = 1MHz, duty cycle = 50%.

■ Truth tables

○2-line to 4-line Decoder/1-line to 4-line Demultiplexer

Inputs				Outputs			
Select		Enable	Data				
B	A	1G	1C	$1Y_0$	$1Y_1$	$1Y_2$	$1Y_3$
×	×	H	×	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
×	×	×	L	H	H	H	H

Inputs				Outputs			
Select		Enable	Data				
B	A	2G	2C	$2Y_0$	$2Y_1$	$2Y_2$	$2Y_3$
×	×	H	×	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
×	×	×	H	H	H	H	H

Notes
1. H: HIGH voltage level.
2. L: LOW voltage level.
3. X: Either HIGH or LOW; doesn't matter.

○3-line to 8-line Decoder/1-line to 8-line Demultiplexer

Inputs				Outputs							
Select			Enable Data	0	1	2	3	4	5	6	7
C	B	A	G	$2Y_0$	$2Y_1$	$2Y_2$	$2Y_3$	$1Y_0$	$1Y_1$	$1Y_2$	$1Y_3$
×	×	×	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

Notes
1. H: HIGH voltage level.
2. L: LOW voltage level.
3. X: Either HIGH or LOW; doesn't matter.
4. C: Interconnected 1C and 2C inputs.
5. G: Interconnected 1G and 2G inputs.

DN74LS156

Dual 2-line to 4-line Decoders / Demultiplexers (with Open Colector Outputs)

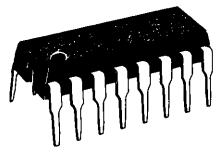
■ Description

DN74LS156 contains two 2-bit binary to quarternary decoder/demultiplexer circuits with open collector outputs.

■ Features

- "Wired" AND capability
- Enable inputs
- Capability for composition of 8-bit output decoder/ demultiplexer without connection of external gate
- Wide operating temperature range (Ta = −20 to +75°C)

P-2

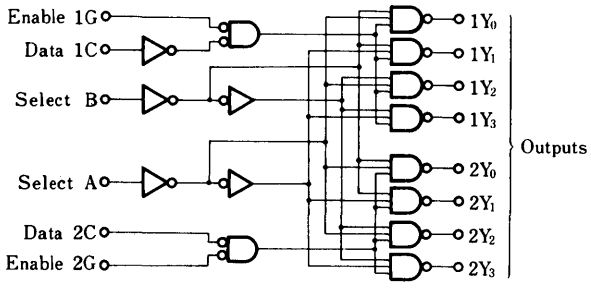


16-pin plastic DIL package

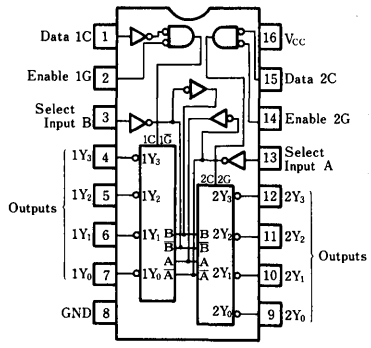
P-5

16-pin Panaflat package (SO-16D)

■ Logic diagram



Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
HIGH level output voltage	V_{OH}			5.5	V
LOW level output voltage	I_{OL}			8	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta=-20\sim+75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OL1}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
	V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
	I_I	$V_{CC}=5.25V$, $V_I=7V$				0.1	mA
Output current	I_{OH}	$V_{CC}=4.75V$, $V_{OH}=5.5V$, $V_{IH}=2V$, $V_{IL}=0.8V$				100	μA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$, $I_I=-18mA$				−1.5	V
Supply current**	I_{CC}	$V_{CC}=5.25V$			6.1	10	mA

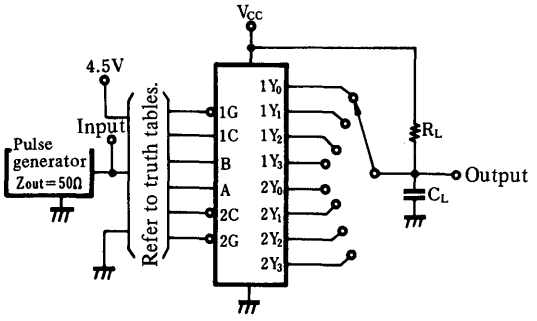
*When constant at $V_{CC}=5V$, Ta=25°C.
**Measured with all outputs open, 4.5 V applied to A, B, and 1C inputs, and 2C, 1G, and 2G inputs grounded.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Outputs	ゲートのレベル	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	A,B,2C,1G or 2G	Y	2	$C_L=15pF$, $R_L=2k\Omega$		25	40	ns
	t_{PHL}	A,B,2C,1G or 2G	Y	2			34	51	ns
	t_{PLH}	A or B	Y	3			31	46	ns
	t_{PHL}	A or B	Y	3			34	51	ns
	t_{PLH}	1C	Y	3			32	48	ns
	t_{PHL}	1C	Y	3			32	48	ns

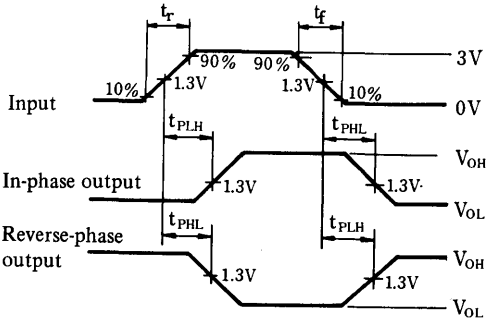
※ Switching parameter measurement information

1. Measurement circuit



Notes
1. C_L includes probe and tool floating capacitance.

2. Waveforms



Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.

■ Truth tables

1. 2-line to 4-line Decoder / 1-lin to 4-line Demultiplexer

Inputs				Outputs				Inputs				Outputs			
Select		Enable	Data					Select		Enable	Data				
B	A	1G	1C	$1Y_0$	$1Y_1$	$1Y_2$	$1Y_3$	B	A	2G	2C	$2Y_0$	$2Y_1$	$2Y_2$	$2Y_3$
×	×	H	×	H	H	H	H	×	×	H	×	H	H	H	H
L	L	L	H	L	H	H	H	L	L	L	L	L	H	H	H
L	H	L	H	H	L	H	H	L	H	L	L	H	L	H	H
H	L	L	H	H	H	L	H	H	L	L	L	H	H	L	H
H	H	L	H	H	H	H	L	H	H	L	L	H	H	H	L
×	×	×	L	H	H	H	H	×	×	×	H	H	H	H	H

2. 3-line to 8-line Decoder / 1-line to 8-line Demultiplexer

Inputs				Outputs							
Select			Enable or Data	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C*1	B	A	G*2	$2Y_0$	$2Y_1$	$2Y_2$	$2Y_3$	$1Y_0$	$1Y_1$	$1Y_2$	$1Y_3$
×	×	×	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

Notes

1. H: HIGH voltage level.
2. L: LOW voltage level.
3. X: Either HIGH or LOW; doesn't matter.

*1 C: Interconnected 1C and 2C inputs.

*2 G: Interconnected 1G and 2G inputs.

DN74LS157

Quad 2-line to 1-line Data Selectors / Multiplexers

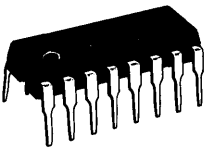
■ Description

DN74LS157 contains four 2-line to 1-line data selector/ multiplexer circuits.

■ Features

- Common enable input for all four circuits
- Common select input for all four circuits
- Low output impedance
- Wide operating temperature range (Ta = −20 to +75°C)

P-2



16-pin plastic DIL package

P-5

16-pin Panaflat package (SO-16D)

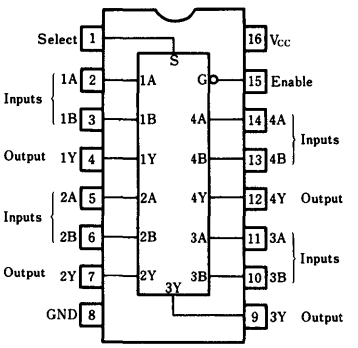
■ Truth tables

Inputs				Outputs
Enable	Select	A	B	Y
H	×	×	×	L
L	L	L	×	L
L	L	H	×	H
L	H	×	L	L
L	H	×	H	H

Notes

1. H: HIGH voltage level.
2. L: LOW voltage level.
3. X: Either HIGH or LOW, doesn't matter.

Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−400	μA
	I_{OL}			8	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter		Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Output voltage		V_{OH}	$V_{CC}=4.75V$, $I_{OH}=-400\mu A$ $V_{IH}=2V$, $V_{IL}=0.8V$		2.7	3.4		V
		V_{OL}	$V_{CC}=4.75V$ $V_{IH}=2V$ $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
				$I_{OL}=8mA$		0.35	0.5	V
Input current	S, G	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				40	μA
	A, B						20	μA
	S, G	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.8	mA
	A, B						−0.4	mA
	S, G	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.2	mA
	A, B						0.1	mA
Output short circuit current**		I_{OS}	$V_{CC}=5.25V$ $V_O=0V$		−15		−100	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current***		I_{CC}	$V_{CC}=5.25V$			9.7	16	mA

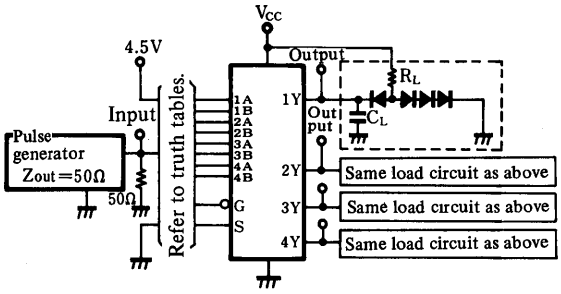
* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.
*** Measured with all outputs open and 4.5V applied to all inputs.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

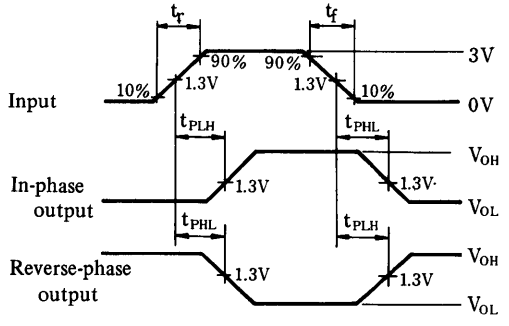
Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	Data	Y	$C_L=15pF$ $R_L=2k\Omega$		9	14	ns
	t_{PHL}					9	14	ns
	t_{PLH}	Enable	Y			13	20	ns
	t_{PHL}					14	21	ns
	t_{PLH}	Select	Y			15	23	ns
	t_{PHL}					18	27	ns

※ Switching parameter measurement information

1. Measurement circuit



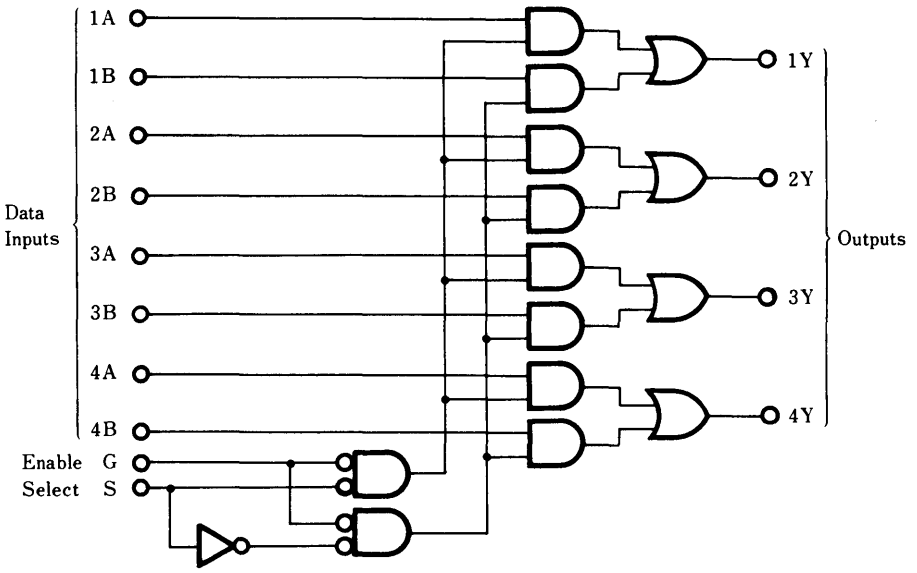
2. Waveforms



Notes
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161 or equivalent.

Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.

■ Logic diagram



DN74LS158

Quad 2-line to 1-line Data Selectors / Multiplexers

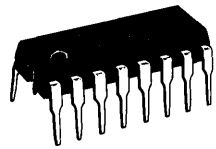
■ Description

DN74LS158 contains four 2-line to 1-line data selector/ multiplexer circuits.

■ Features

- Inverted output
- Common enable input for all four circuits
- Common select input for all four circuits
- Low output impedance
- Wide operating temperature range (Ta = −20 to +75°C)

P-2



16-pin plastic DIL package

P-5

16-pin Panaflat package (SO-16D)

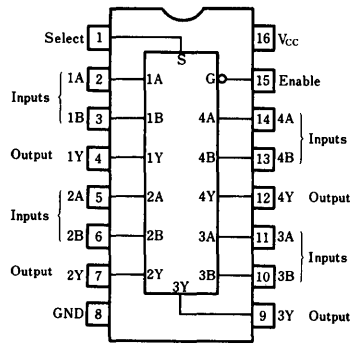
■ Truth tables

Inputs				Outputs
Enable	Select	A	B	Y
H	×	×	×	H
L	L	L	×	H
L	L	H	×	L
L	H	×	L	H
L	H	×	H	L

Notes

1. H: HIGH voltage level.
2. L: LOW voltage level.
3. X: Either HIGH or LOW; doesn't matter.

Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−400	μA
	I_{OL}			8	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter		Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Output voltage		V_{OH}	$V_{CC}=4.75V$, $I_{OH}=-400\mu A$ $V_{IH}=2V$, $V_{IL}=0.8V$		2.7	3.4		V
		V_{OL}	$V_{CC}=4.75V$ $V_{IH}=2V$ $V_{IL}=0.8V$,	$I_{OL}=4mA$		0.25	0.4	V
				$I_{OL}=8mA$		0.35	0.5	V
Input current	S, G	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				40	μA
	A, B						20	μA
	S, G	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.8	mA
	A, B						−0.4	mA
	S, G	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.2	mA
	A, B						0.1	mA
Output short circuit current**		I_{OS}	$V_{CC}=5.25V$ $V_O=0V$		−15		−100	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current***		I_{CC}	$V_{CC}=5.25V$			4.8	8	mA

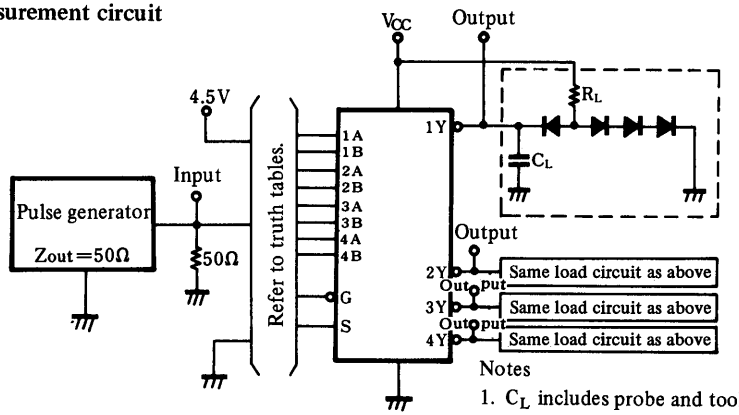
* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.
*** Measured with all outputs open and 4.5V applied to all inputs.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	Data	Y	$C_L=15pF$ $R_L=2k\Omega$		7	12	ns
	t_{PHL}					7	15	ns
	t_{PLH}	Enable	Y			11	17	ns
	t_{PHL}					12	24	ns
	t_{PLH}	Select	Y			13	20	ns
	t_{PHL}					16	24	ns

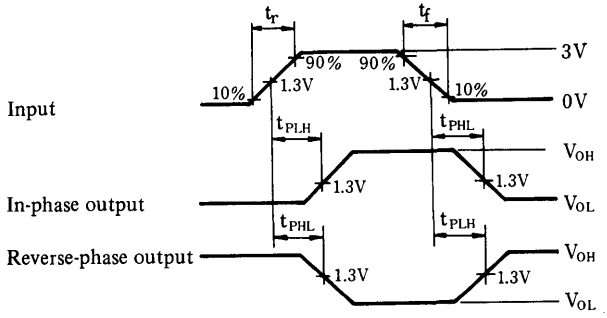
※ Switching parameter measurement information

1. Measurement circuit



Notes
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161.

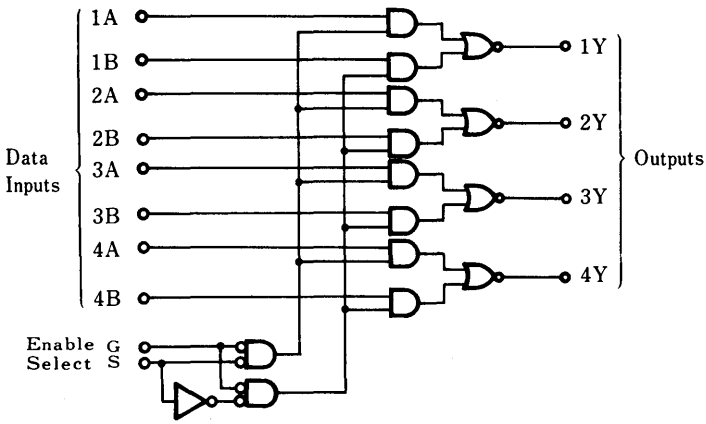
2. Waveforms



Notes

1. Input waveform: $t_r \leqq 15$ns, $t_f \leqq 6$ns, PRR = 1MHz, duty cycle = 50%.

■ Logic diagram



DN74LS160A

Synchronous Decade Counters

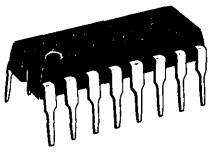
■ Description

DN74LS160A is a settable synchronous decade counter with direct-coupled reset input.

■ Features

- Direct-coupled reset input and synchronous set input
- Carry output and enable input for cascade connection
- High-speed counting (f_{max} = 32MHz typical)
- Wide operating temperature range (Ta = −20 to +75°C)

P-2

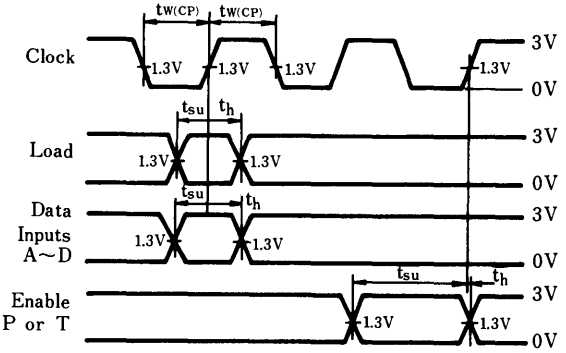


16-pin plastic DIL package

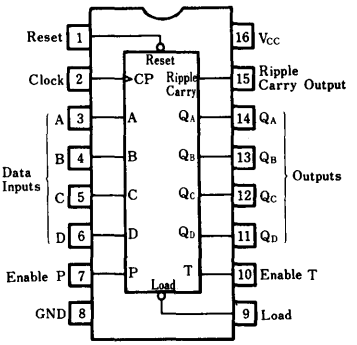
P-5

16-pin Panaflat package (SO-16D)

■ Timing definition



Pin configuration (top view)



■ Recommended operating conditions

Parameter		Sym	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}			−400	μA
		I_{OL}			8	mA
Operating temperature range		Topr	−20	25	75	℃
Clock frequency		f_{clock}	0		25	MHz
Clock pulse width		$t_{W(CP)}$	25			ns
Reset pulse width		$t_{W(Reset)}$	20			ns
Set-up time	Data A, B, C, D	t_{su}	20			ns
	Enable P, T		20			ns
	Load		20			ns
Hold time		t_h	0			ns

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter		Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Output voltage		V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$ $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	3.4		V
		V_{OL1}	$V_{CC}=4.75V$ $V_{IH}=2V$ $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
		V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	Data, Enable, P	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				20	μA
	Load, Clock, Enable, T						40	μA
	Reset						20	μA
	Data, Enable, P	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.4	mA
	Load, Clock, Enable, T						−0.8	mA
	Reset						−0.4	mA
	Data, Enable, P	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.1	A
	Load, Clock, Enable, T						0.2	mA
	Reset						0.1	mA
Output short circuit current**		I_{OS}	$V_{CC}=5.25V$ $V_o=0V$		−15		−100	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current***		I_{CCH}	$V_{CC}=5.25V$			18	31	mA
		I_{CCL}	$V_{CC}=5.25V$			19	32	mA

* When constant at V_{CC} = 5V, Ta = 25°C.

** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

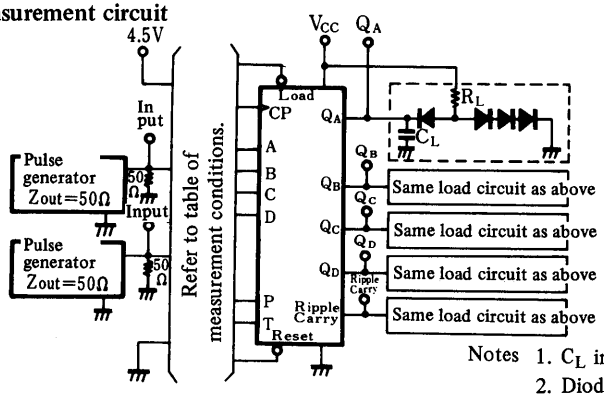
*** I_{CCH} is measured first with all outputs open and all inputs at HIGH; next it is measured again under the same conditions except with the load inputs at LOW.
I_{CCL} is measured first with all outputs open and all inputs at LOW; next it is measured again under the same condition except with the clock inputs at LOW.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Maximum clock frequency	f_{max}	Clock	$Q_A \sim Q_D$	$C_L=15pF$ $R_L=2k\Omega$	25	32		MHz
Propagation delay time	t_{PLH}	Clock	Ripple Carry			20	35	ns
	t_{PHL}					18	35	ns
	t_{PLH}	Clock (Load="H")	$Q_A \sim Q_D$			13	24	ns
	t_{PHL}					18	27	ns
	t_{PLH}	Clock (Load="L")	$Q_A \sim Q_D$			13	24	ns
	t_{PHL}					18	27	ns
	t_{PLH}	Enable T	Ripple Carry			9	16	ns
	t_{PHL}					9	25	ns
	t_{PHL}	Reset	$Q_A \sim Q_D$			20	28	ns

※ Switching parameter measurement information

1. Measurement circuit



Notes 1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161.

2. Table of measurement conditions

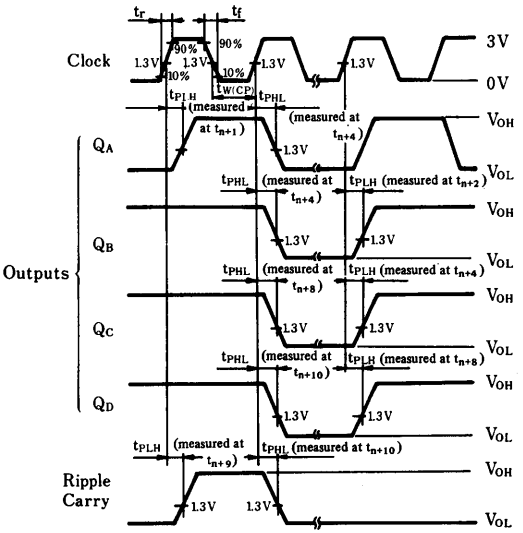
Parameter	Inputs/Outputs	Inputs									Outputs				
		Reset	Load	Enable		Clock	Data				Q_A	Q_B	Q_C	Q_D	Ripple Carry
				P	T		A	B	C	D					
f_{max}		4.5V	4.5V	4.5V	4.5V	IN	GND	GND	GND	GND	OUT	OUT	OUT	OUT	OUT
t_{PLH} t_{PHL}	CP→Ripple Carry	4.5V	4.5V	4.5V	4.5V	IN	GND	GND	GND	GND					OUT
	CP→Q	4.5V	4.5V	4.5V	4.5V	IN	GND	GND	GND	GND	OUT	OUT	OUT	OUT	
	CP→Q	4.5V	GND	GND	GND	IN	IN*	IN*	IN*	IN*	OUT	OUT	OUT	OUT	
	Enable T→Ripple Carry	4.5V	GND	4.5V	IN	IN**	4.5V	GND	GND	4.5V					OUT
	Reset→Q	IN	GND	GND	GND	IN**	4.5V	4.5V	4.5V	4.5V	OUT	OUT	OUT	OUT	

* Set to this state in accordance with measured output so that none of the various outputs, Q_A, Q_B, Q_C, and Q_D, exceeds HIGH, LOW, LOW, and HIGH, respectively.

** Applied for initialization.

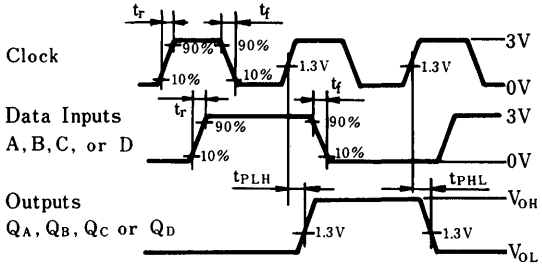
3.Waveforms

Waveforms-1 f_{max}, t_{PLH}, t_{PHL} (Clock → Q, Ripple Carry)



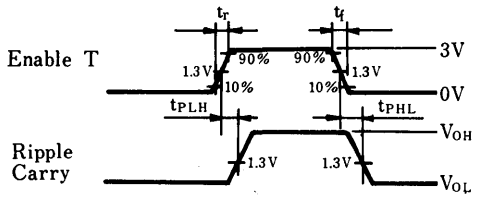
Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 5ns$, PRR = 1MHz, duty cycle = 50%.
2. When measuring f_{max}, t_r and $t_f \leqq 2.5ns$.
3. t_n is the bit time when all outputs are LOW.

Waveforms-2 t_{PLH}, t_{PHL} (Clock → Q)



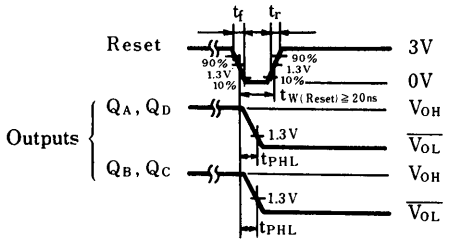
Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$.
2. Clock input: PRR = 1MHz, duty cycle = 50%.
3. Data input: PRR = 500kHz, duty cycle = 50%.

Waveforms-3 t_{PLH}, t_{PHL} (Enable T→Ripple Carry)



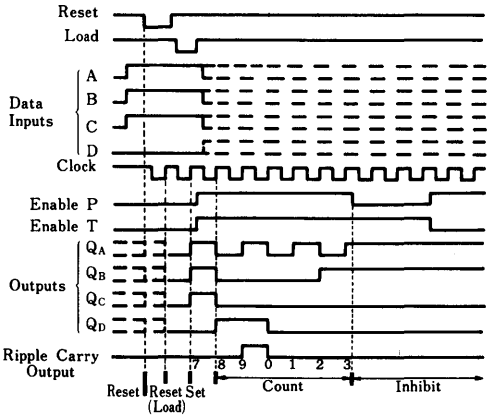
Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR=1MHz

Waveforms-4 t_{PHL} (Reset → Q)

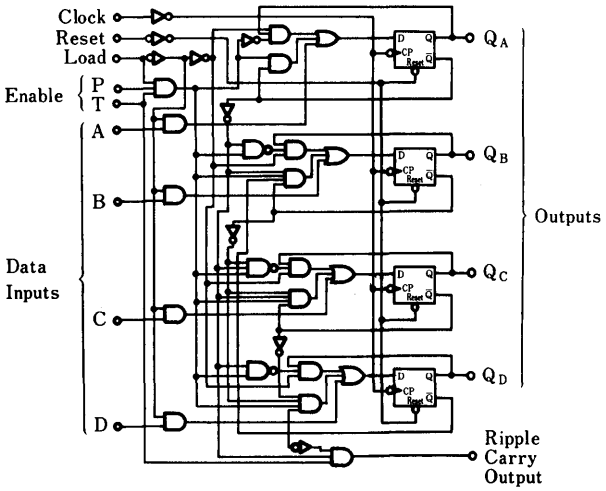


Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$

■ Timing chart



■ Logic diagram



DN74LS161A

Synchronous 4-bit Binary Counters

■ Description

DN74LS161A is a settable synchronous 4-bit binary (hexadecimal) counter with direct-coupled reset input.

■ Features

- Direct coupled reset input and synchronous set input
- Carry output and enable input for cascade connection
- High-speed counting (f_{max} = 32MHz typical)
- Wide operating temperature range (Ta = −20 to +75°C)

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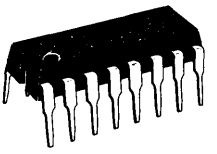
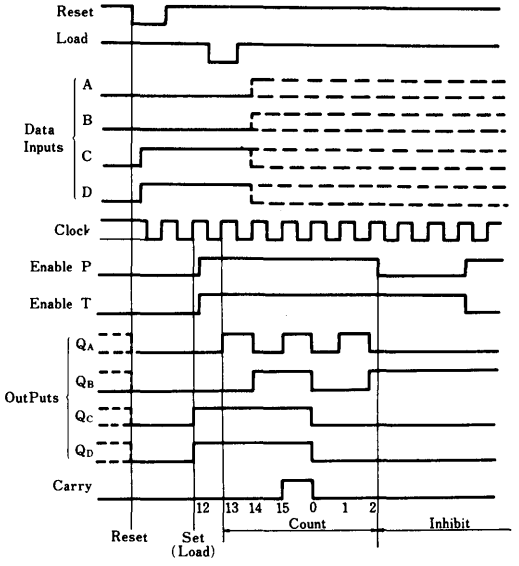


16-pin plastic DIL package

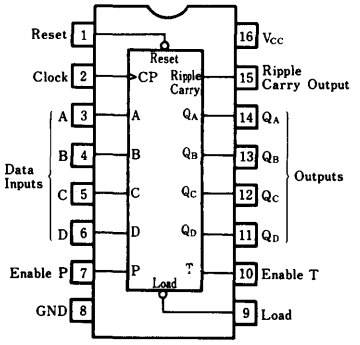
P-5

16-pin Panaflat package (SO-16D)

■ Timing definition



Pin configuration (top view)



■ Recommended operating conditions

Parameter		Sym	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}			−400	μA
		I_{OL}			8	mA
Operating temperature range		Topr	−20	25	75	℃
Clock frequency		f_{clock}	0		25	MHz
Clock pulse width		$t_{W(CP)}$	25			ns
Reset pulse width		$t_{W(Reset)}$	20			ns
Set-up time	Data A, B, C, D	t_{su}	20			ns
	Enable P, T		20			ns
	Load		20			ns
Hold time		t_h	0			ns

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter		Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Output voltage		V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	3.4		V
		V_{OL1}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
		V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	Data, Enable, P	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
	Load, Clock, Enable, T						40	μA
	Reset						20	μA
	Data, Enable, P	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
	Load, Clock, Enable, T						−0.8	mA
	Reset						−0.4	mA
	Data, Enable, P	I_I	$V_{CC}=5.25V$, $V_I=7V$				0.1	mA
	Load, Clock, Enable, T						0.2	mA
	Reset						0.1	mA
Output short circuit current**		I_{OS}	$V_{CC}=5.25V$, $V_o=0V$		−15		−100	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$, $I_I=-18mA$				−1.5	V
Supply current***		I_{CCH}	$V_{CC}=5.25V$			18	31	mA
		I_{CCL}	$V_{CC}=5.25V$			19	32	mA

* When constant at V_{CC} = 5V, Ta = 25°C.

** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

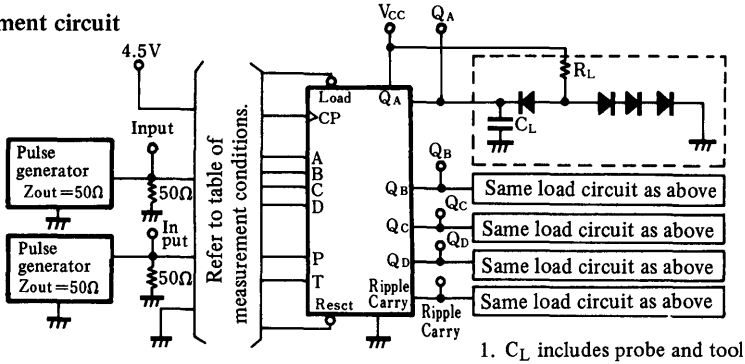
*** I_{CCH} is measured first with all outputs open and all inputs at HIGH; next it is measured again under the same conditions except with the load inputs at LOW.
I_{CCL} is measured first with all outputs open and all inputs at LOW; next it is measured again under the same condition except with the clock inputs at LOW.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Maximum clock frequency	f_{max}	Clock	$Q_A \sim Q_D$	$C_L=15pF$, $R_L=2k\Omega$	25	32		MHz
Propagation delay time	t_{PLH}	Clock	Ripple Carry			20	35	ns
	t_{PHL}					18	35	ns
	t_{PLH}	Clock (Load="H")	$Q_A \sim Q_D$			13	24	ns
	t_{PHL}					18	27	ns
	t_{PLH}	Clock (Load="L")	$Q_A \sim Q_D$			13	24	ns
	t_{PHL}					18	27	ns
	t_{PLH}	Enable T	Ripple Carry			9	16	ns
	t_{PHL}					9	25	ns
	t_{PHL}	Reset	$Q_A \sim Q_D$			20	28	ns

※ Switching parameter measurement information

1. Measurement circuit



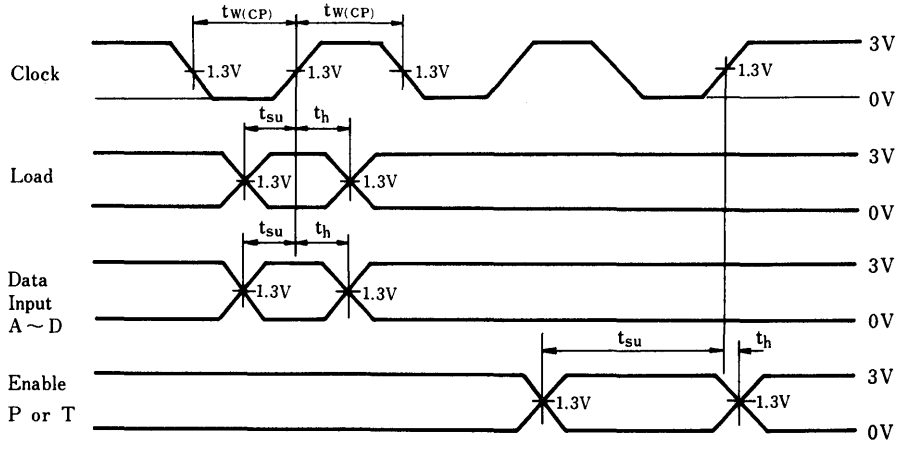
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161.

2. Table of measurement conditions

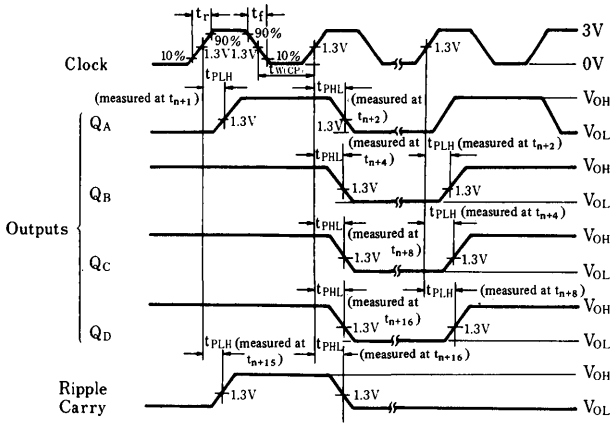
Parameter	Inputs/Outputs	Inputs									Outputs				
		Reset	Load	Enable		Clock	Data				Q_A	Q_B	Q_C	Q_D	Ripple Carry
				P	T		A	B	C	D					
f_{max}		4.5V	4.5V	4.5V	4.5V	IN	GND	GND	GND	GND	OUT	OUT	OUT	OUT	OUT
t_{PLH} t_{PHL}	CP→Ripple Carry	4.5V	4.5V	4.5V	4.5V	IN	GND	GND	GND	GND					OUT
	CP→Q	4.5V	4.5V	4.5V	4.5V	IN	GND	GND	GND	GND	OUT	OUT	OUT	OUT	
	CP→Q	4.5V	GND	GND	GND	IN	IN*	IN*	IN*	IN*	OUT	OUT	OUT	OUT	
	Enable T→Ripple Carry	4.5V	GND	4.5V	IN	IN*	4.5V	GND	GND	4.5V					OUT
	Reset→Q	IN	GND	GND	GND	IN*	4.5V	4.5V	4.5V	4.5V	OUT	OUT	OUT	OUT	

* Applied for initialization.

■ Timing chart



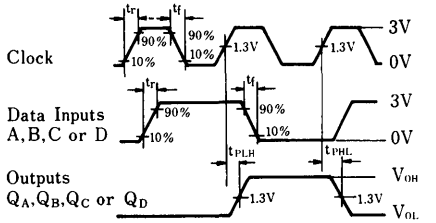
Waveforms-1 f_{max}, t_{PLH}, t_{PHL} (Clock → Q, Ripple Carry)



Notes

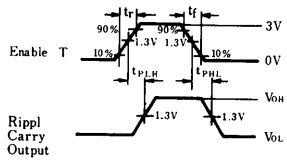
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 5ns$, PRR = 1MHz, duty cycle = 50%.
2. When measuring f_{max}, t_r and $t_f \leqq 2.5ns$.
3. t_n is the bit time when all outputs are LOW.

Waveforms-2 t_{PLH}, t_{PHL} (Clock → Q)



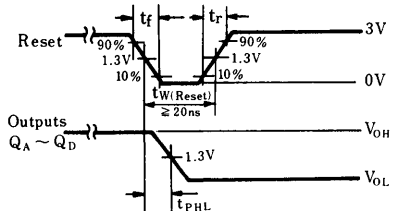
Note 1. Clock input: f = 1MHz, duty cycle = 50%
Data input: f = 500kHz, duty cycle = 50%

Waveforms-3 t_{PLH}, t_{PHL} (Enable T → Ripple Carry



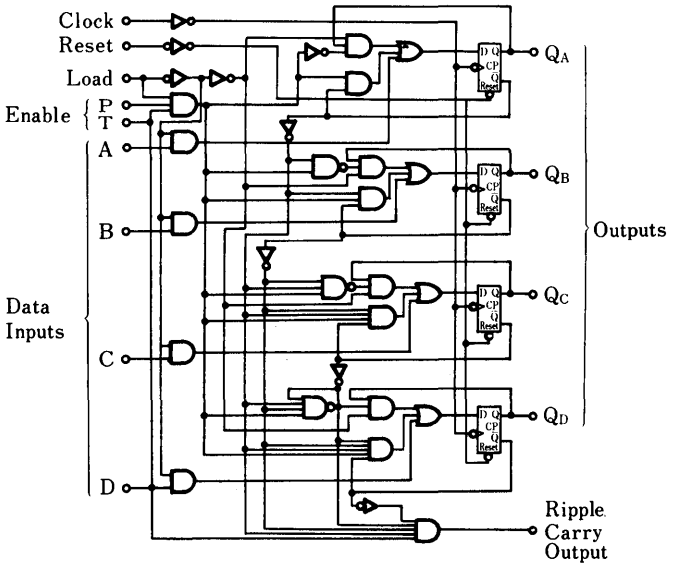
Notes 1. $t_r \leqq 15ns$, $t_f = 6ns$, PRR = 1MHz

Waveforms-4 t_{PHL} (Reset → Q)



Notes 1. $t_r \leqq 15ns$, $t_f \leqq 6ns$

Logic diagram



DN74LS162A

Synchronous Decade Counters

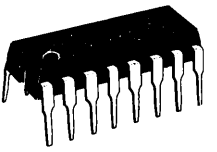
■ Description

DN74LS162A is a settable synchronous decade counter with synchronous reset input.

■ Features

- Synchronous reset and set inputs
- Carry output and enable input for cascade connection
- High-speed counting (f_{max} = 32MHz typical)
- Wide operating temperature range (Ta = −20 to +75°C)

P-2

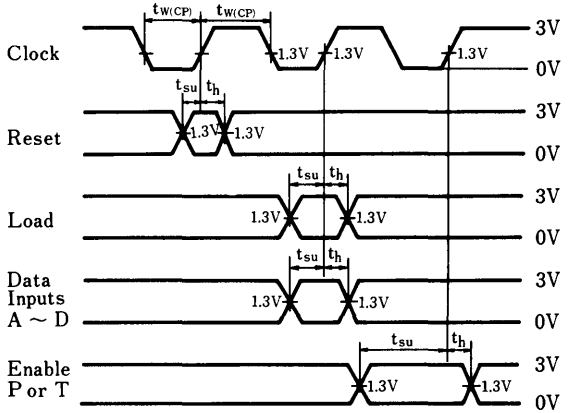


16-pin plastic DIL package

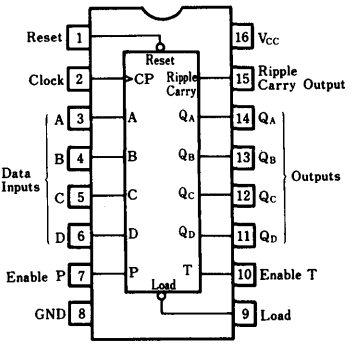
P-5

16-pin Panaflat package (SO-16D)

■ Timing definition



Pin configuration (top view)



■ Recommended operating conditions

Parameter		Sym	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}			−400	μA
		I_{OL}			8	mA
Operating temperature range		Topr	−20	25	75	℃
Clock frequency		f_{clock}	0		25	MHz
Clock pulse width		$t_{W(CP)}$	25			ns
Reset pulse width		$t_{W(Reset)}$	20			ns
Set-up time	Data A, B, C, D	t_{su}	20			ns
	Enable P, T		20			ns
	Load		20			ns
Hold time		t_h	0			ns

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter		Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Output voltage		V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$ $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	3.4		V
		V_{OL1}	$V_{CC}=4.75V$ $V_{IH}=2V$ $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
		V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	Data, Enable, P	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				20	μA
	Load, Clock, Enable, T						40	μA
	Reset						40	μA
	Data, Enable, P	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.4	mA
	Load, Clock, Enable, T						−0.8	mA
	Reset						−0.8	mA
	Data, Enable, P	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.1	mA
	Load, Clock, Enable, T						0.2	mA
	Reset						0.2	mA
Output short circuit current**		I_{OS}	$V_{CC}=5.25V$ $V_o=0V$		−15		−100	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current***		I_{CCH}	$V_{CC}=5.25V$			18	31	mA
		I_{CCL}	$V_{CC}=5.25V$			19	32	mA

* When constant at V_{CC} = 5V, Ta = 25°C

** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

*** I_{CCH} is measured first with all outputs open and all inputs at HIGH; next it is measured again under the same conditions except with the load inputs at LOW.

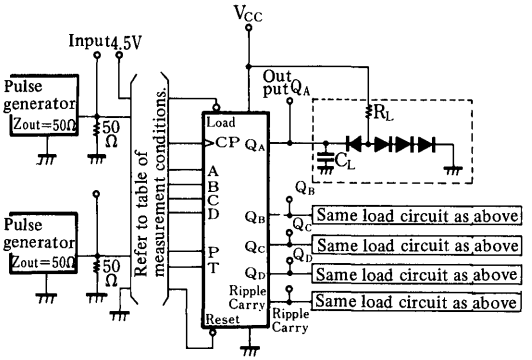
I_{CCL} is measured first with all outputs open and all inputs at LOW; next it is measured again under the same condition except with the clock inputs at LOW.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Maximum clock frequency	f_{max}	Clock	$Q_A \sim Q_D$	$C_L=15pF$ $R_L=2k\Omega$	25	32		MHz
Propagation delay time	t_{PLH}	Clock	Ripple Carry			20	35	ns
	t_{PHL}					18	35	ns
	t_{PLH}	Clock (Load="H")	$Q_A \sim Q_D$			13	24	ns
	t_{PHL}					18	27	ns
	t_{PLH}	Clock (Load="L")	$Q_A \sim Q_D$			13	24	ns
	t_{PHL}					18	27	ns
	t_{PLH}	Enable T	Ripple Carry			9	16	ns
	t_{PHL}					9	25	ns
	t_{PHL}	Reset	$Q_A \sim Q_D$			20	28	ns

※ Switching parameter measurement information

1. Measurement circuit



1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161.

2. Table of measurement conditions

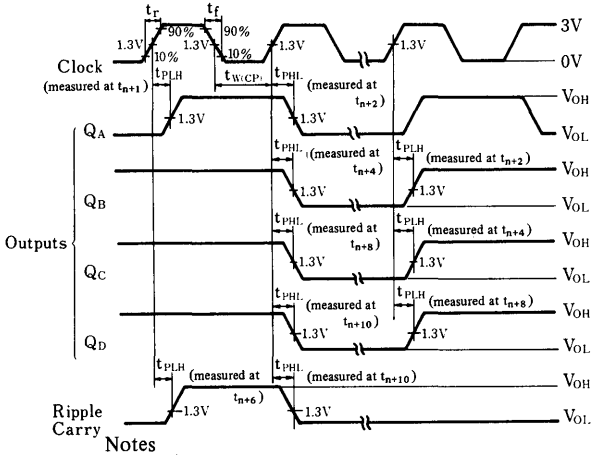
Parameter	Inputs/Outputs	Inputs									Outputs				
		Reset	Load	Enable		Clock	Data				Q_A	Q_B	Q_C	Q_D	Ripple Carry
				P	T		A	B	C	D					
f_{max}		4.5V	4.5V	4.5V	4.5V	IN	GND	GND	GND	GND	OUT	OUT	OUT	OUT	OUT
t_{PLH} t_{PHL}	CP→Ripple Carry	4.5V	4.5V	4.5V	4.5V	IN	GND	GND	GND	GND					OUT
	CP→Q	4.5V	4.5V	4.5V	4.5V	IN	GND	GND	GND	GND	OUT	OUT	OUT	OUT	
	CP→Q	4.5V	GND	GND	GND	IN	IN*	IN*	IN*	IN*	OUT	OUT	OUT	OUT	
	Enable T→Ripple Carry	4.5V	GND	4.5V	IN	IN**	4.5V	GND	GND	4.5V					OUT
	Reset→Q	IN	GND	GND	GND	IN**	4.5V	4.5V	4.5V	4.5V	OUT	OUT	OUT	OUT	

* Set to this state in accordance with measured output so that none of the various outputs, Q_A, Q_B, Q_C, and Q_D, exceeds HIGH, LOW, LOW, and HIGH, respectively.

** Applied for initialization.

3.Waveforms

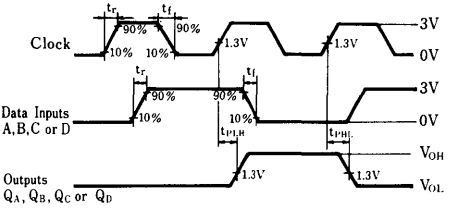
Waveforms-1 f_{max}, t_{PLH}, t_{PHL} (Clock → Q, Ripple Carry)



Notes

1. Input waveform: $t_r \leqq 15$ns, $t_f \leqq 5$ns, PRR = 1MHz, duty cycle = 50%.

Waveforms-2 t_{PLH}, t_{PHL} (Clock → Q)

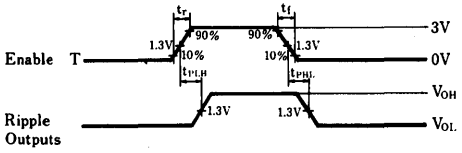


Notes

1. Input waveform: $t_r \leqq 15$ns, $t_f \leqq 6$ns.
2. Clock input: PRR = 1MHz, duty cycle = 50%.
3. Data input: PRR = 500kHz, duty cycle = 50%.

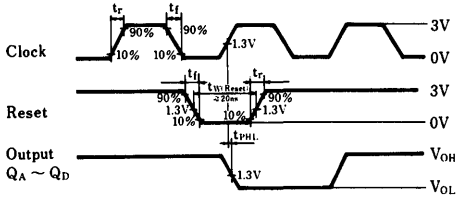
2. When measuring f_{max}, t_r and $t_f \leqq 2.5$ns.
3. t_n is the bit time when all outputs are LOW.

Waveforms-3 t_{PLH}, t_{PHL} (Enable T→Ripple Carry)



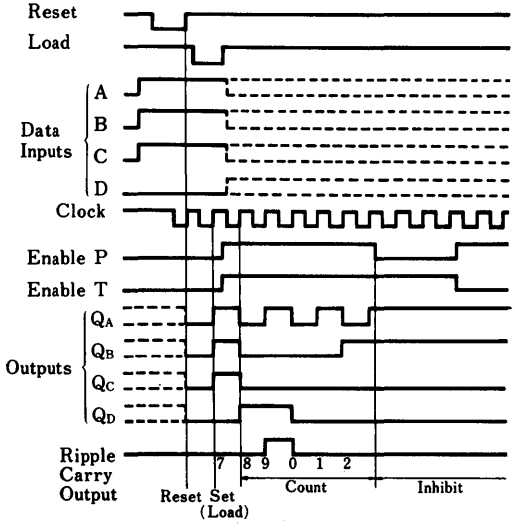
Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz.

Waveforms-4 t_{PHL} (Reset → Q)

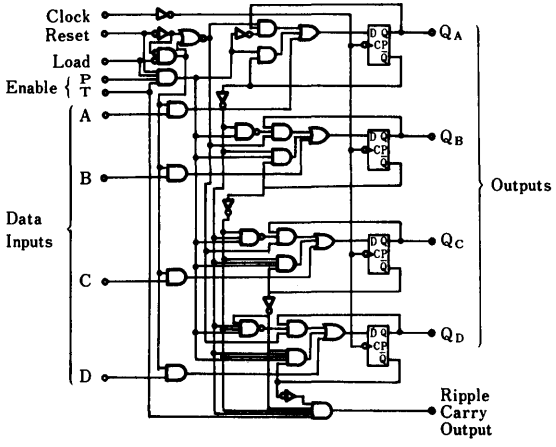


Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$

■ Timing chart



■ Logic diagram



DN74LS163A

Synchronous 4-bit Binary Counters

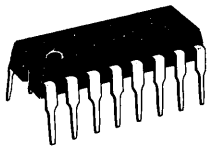
■ Description

DN74LS163A is a settable synchronous 4-bit binary (hexadecimal) counter with synchronous reset input.

■ 特 長

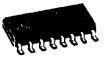
- Synchronous reset and set inputs
- Carry output and enable input for cascade connection
- High-speed counting (f_{max} = 32 MHz typical)
- Wide operating temperature range (Ta = −20 to +75°C)

P-2



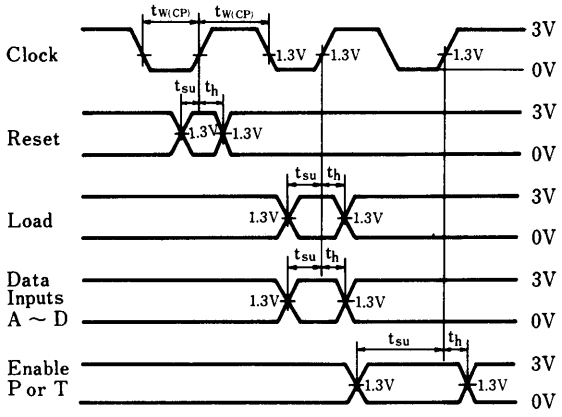
16-pin plastic DIL package

P-5

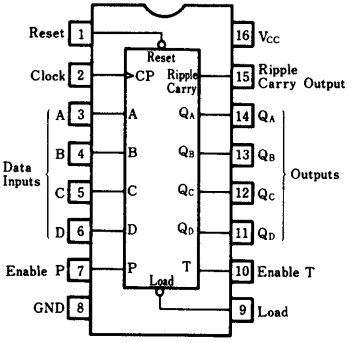


16-pin Panaflat package (SO-16D)

■ Timing definition



Pin configuration (top view)



■ Recommended operating conditions

Parameter		Sym	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}			−400	μA
		I_{OL}			8	mA
Operating temperature range		Topr	−20	25	75	℃
Clock frequency		f_{clock}	0		25	MHz
Clock pulse width		$t_{W(CP)}$	25			ns
Reset pulse width		$t_{W(Reset)}$	20			ns
Set-up time	Data A, B, C, D	t_{su}	20			ns
	Enable P, T		20			ns
	Load		20			ns
Hold time		t_h	0			ns

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter		Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Output voltage		V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	3.4		V
		V_{OL1}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
		V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	Data, Enable, P	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
	Load, Clock, Enable, T						40	μA
	Reset						40	μA
	Data, Enable, P	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
	Load, Clock, Enable, T						−0.8	mA
	Reset						−0.8	mA
	Data, Enable, P	I_I	$V_{CC}=5.25V$, $V_I=7V$				0.1	mA
	Load, Clock, Enable, T						0.2	mA
	Reset						0.2	mA
Output short circuit current**		I_{OS}	$V_{CC}=5.25V$, $V_o=0V$		−15		−100	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$, $I_I=-18mA$				−1.5	V
Supply current***		I_{CCH}	$V_{CC}=5.25V$			18	31	mA
		I_{CCL}	$V_{CC}=5.25V$			19	32	mA

* When constant at V_{CC} = 5V, Ta = 25°C.

** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

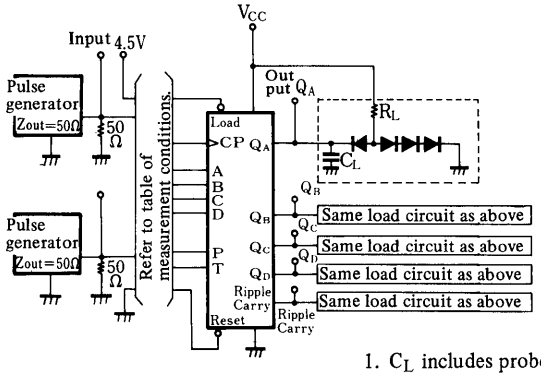
*** I_{CCH} is measured first with all outputs open and all inputs at HIGH; next it is measured again under the same conditions except with the load inputs at LOW.
I_{CCL} is measured first with all outputs open and all inputs at LOW; next it is measured again under the same condition except with the clock inputs at LOW.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Maximum clock frequency	f_{max}	Clock	$Q_A \sim Q_D$	$C_L=15pF$, $R_L=2k\Omega$	25	32		MHz
Propagation delay time	t_{PLH}	Clock	Ripple Carry			20	35	ns
	t_{PHL}					18	35	ns
	t_{PLH}	Clock (Load="H")	$Q_A \sim Q_D$			13	24	ns
	t_{PHL}					18	27	ns
	t_{PLH}	Clock (Load="L")	$Q_A \sim Q_D$			13	24	ns
	t_{PHL}					18	27	ns
	t_{PLH}	Enable T	Ripple Carry			9	16	ns
	t_{PHL}					9	25	ns
	t_{PHL}	Reset	$Q_A \sim Q_D$			20	28	ns

※ Switching parameter measurement information

1. Measurement circuit



1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161.

2. Table of measurement conditions

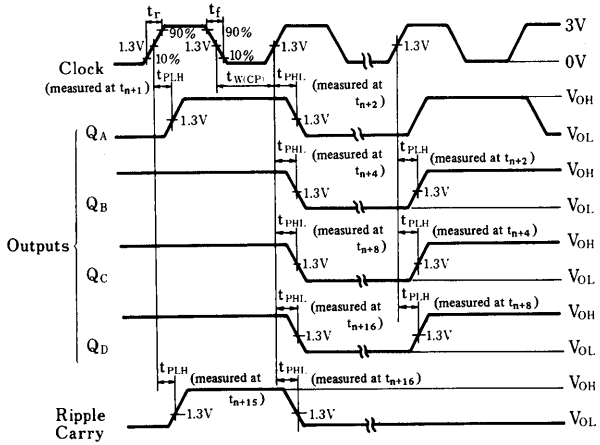
Parameter	Inputs/Outputs	Inputs									Outputs				
		Reset	Load	Enable		Clock	Data				Q_A	Q_B	Q_C	Q_D	Ripple Carry
				P	T		A	B	C	D					
f_{max}		4.5V	4.5V	4.5V	4.5V	IN	GND	GND	GND	GND	OUT	OUT	OUT	OUT	OUT
t_{PLH} t_{PHL}	CP→Ripple Carry	4.5V	4.5V	4.5V	4.5V	IN	GND	GND	GND	GND					OUT
	CP→Q	4.5V	4.5V	4.5V	4.5V	IN	GND	GND	GND	GND	OUT	OUT	OUT	OUT	
	CP→Q	4.5V	GND	GND	GND	IN	IN*	IN*	IN*	IN*	OUT	OUT	OUT	OUT	
	Enable T→Ripple Carry	4.5V	GND	4.5V	IN	IN**	4.5V	GND	GND	4.5V					OUT
	Reset→Q	IN	GND	GND	GND	IN**	4.5V	4.5V	4.5V	4.5V	OUT	OUT	OUT	OUT	

* Set to this state in accordance with measured output so that none of the various outputs, Q_A, Q_B, Q_C, and Q_D, exceeds HIGH, LOW, LOW, and HIGH, respectively.

** Applied for initialization.

3. Waveforms

Waveforms-1 f_{max}, t_{PLH}, t_{PHL} (Clock → Q, Ripple Carry)

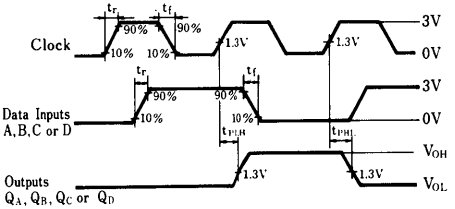


Notes 1. Input waveform: $t_r \leqq 15$ns, $t_f \leqq 5$ns, PRR = 1MHz, duty cycle = 50%.

2. When measuring f_{max}, t_r and $t_f \leqq 2.5$ns.

3. t_n is the bit time when all outputs are LOW.

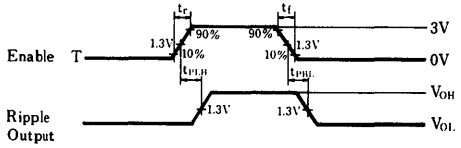
Waveforms-2 t_{PLH}, t_{PHL} (Clock → Q)



Notes

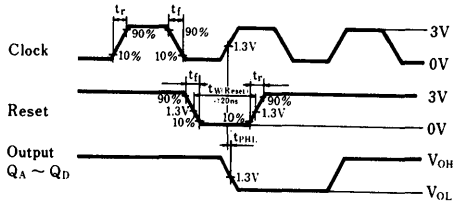
1. Input waveform: $t_r \leqq 15$ns, $t_f \leqq 6$ns.
2. Clock input: PRR = 1MHz, duty cycle = 50%.
3. Data input: PRR = 500kHz, duty cycle = 50%.

Waveforms-3 t_{PLH}, t_{PHL} (Enable T→Ripple Carry)



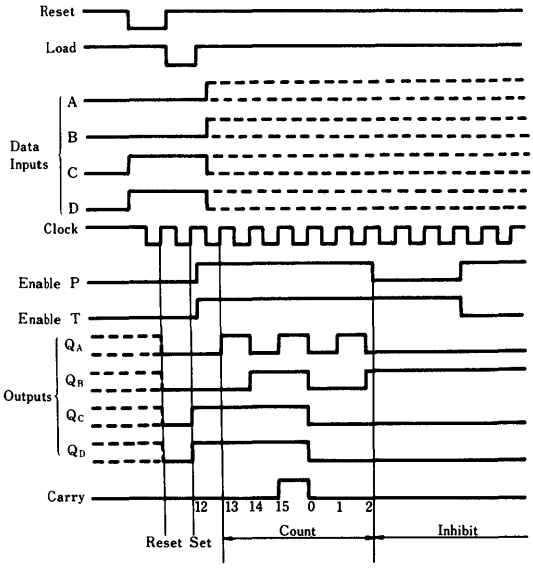
Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR=1MHz

Waveforms-4 t_{PHL} (Reset → Q)

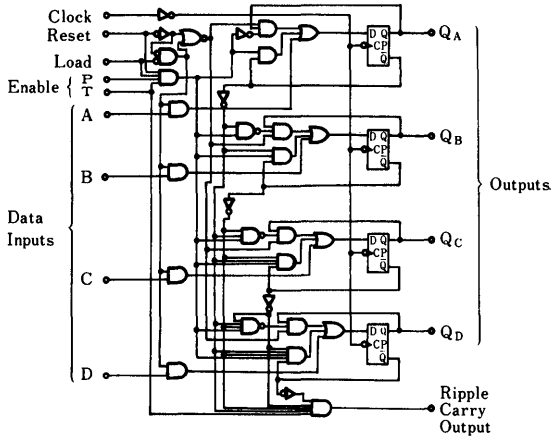


Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$

■ Timing chart



■ Logic diagram



DN74LS164

8-bit Parallel-out Serial Shift Registers

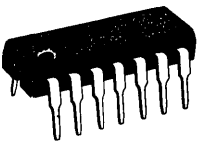
■ Description

DN74LS164 is an 8-bit serial input to serial/parallel output shift register with direct-coupled reset input.

■ Features

- Serial input to serial/parallel output
- Direct-coupled reset input
- Eight bits for large space factor
- Input load coefficient for each input is 1
- Wide operating temperature range (Ta = −20 to +75°C)

P-1



14-pin plastic DIL package

P-4

14-pin Panaflat package (SO-14D)

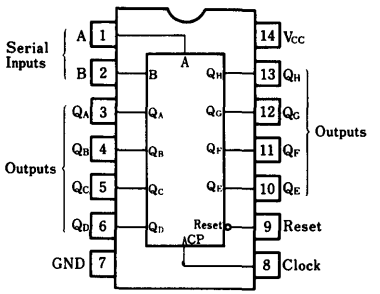
■ Truth tables

Inputs				Outputs		
Reset	Clock	A	B	Q_A	Q_B·····Q_H	
L	×	×	×	L	L	L
H	L	×	×	Q_{AO}	Q_{Bo}	Q_{Ho}
H	↑	H	H	H	Q_{An}	Q_{Gn}
H	↑	L	×	L	Q_{An}	Q_{Gn}
H	↑	×	L	L	Q_{An}	Q_{Gn}

Notes

1. H: HIGH voltage level.
2. L: LOW voltage level.
3. X: Either HIGH or LOW; doesn't matter.
4. ↑: Change from LOW to HIGH.
5. Q_{Ao}, Q_{Bo}, Q_{Ho}: Q_A, Q_B, and Q_H levels prior to determination of input requirements shown in table.
6. Q_{An}, Q_{Gn}: Q_A, Q_B, Q_H levels prior to nearest clock ↑ change.

Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−400	μA
	I_{OL}			8	mA
Operating temperature range	Topr	−20	25	75	℃
Clock frequency	f_{clock}	0		25	MHz
Clock pulse width	$t_{W(CP)}$	20			ns
Reset pulse width	$t_{W(Reset)}$	20			ns
Data set-up time	t_{su}	15			ns
Data hold time	t_h	5			ns

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$ $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	3.4		V
	V_{OL1}	$V_{CC}=4.75V$ $V_{IH}=2V$ $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
	V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				20	μA
	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.4	mA
	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.1	mA
Output short circuit current**	I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−100	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current***	I_{CC}	$I_{CC}=5.25V$			16	27	mA

* When constant at V_{CC} = 5V, Ta = 25°C.

** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

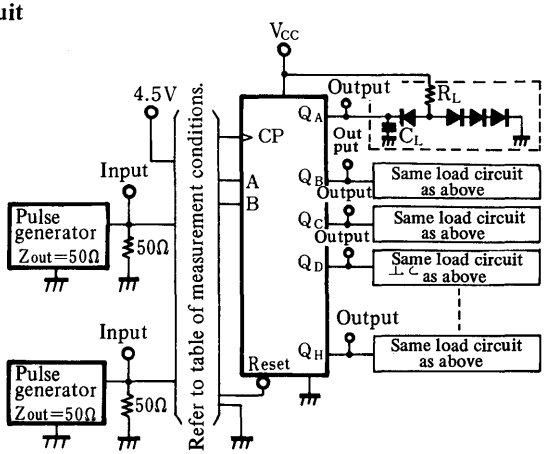
*** Measured with all outputs open, serial inputs grounded, and 2.4V applied to clock inputs; also, reset inputs are grounded momentarily, following which 4.5V is applied to them.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Maximum clock frequency	f_{max}				25	36		MHz
Propagation delay time	t_{PHL}	Reset	Q	$C_L=15pF$		24	36	ns
	t_{PLH}	Clock	Q	$R_L=2k\Omega$		17	27	ns
	t_{PHL}	Clock	Q			21	32	ns

※ Switching parameter measurement information

1. Measurement circuit

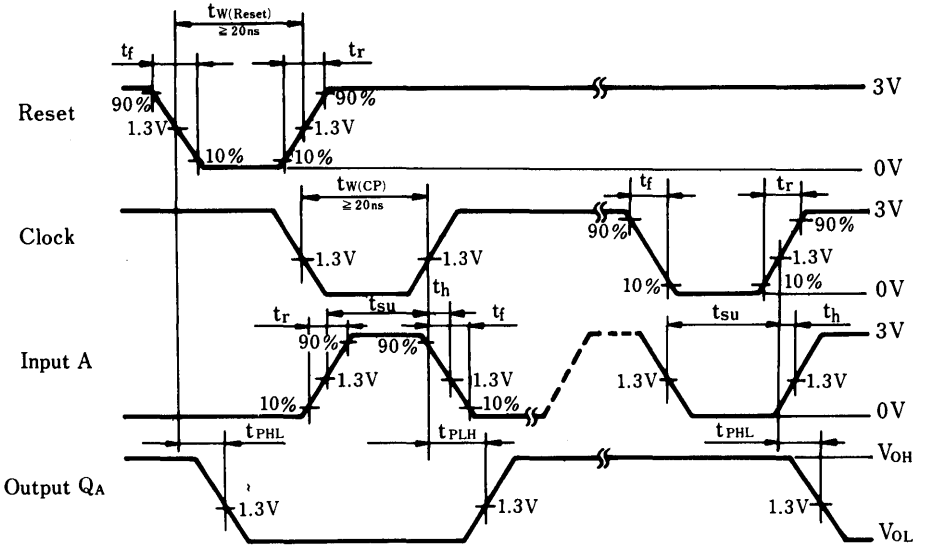


1. Number of pulse generators increased as needed.
2. C_L includes probe and tool floating capacitance.
3. Diodes are all MA161.

2. Table of measurement conditions

Parameter	Input Output	Inputs				Outputs							
		Reset	Clock	A	B	Q_A	Q_B	Q_C	Q_D	Q_E	Q_F	Q_G	Q_H
f_{max}		4.5V	IN	IN	4.5V	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT
t_{PLH}	Reset→Q	IN	IN	IN	4.5V	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT
t_{PHL}	Clock→Q	4.5V	IN	IN	4.5V	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT

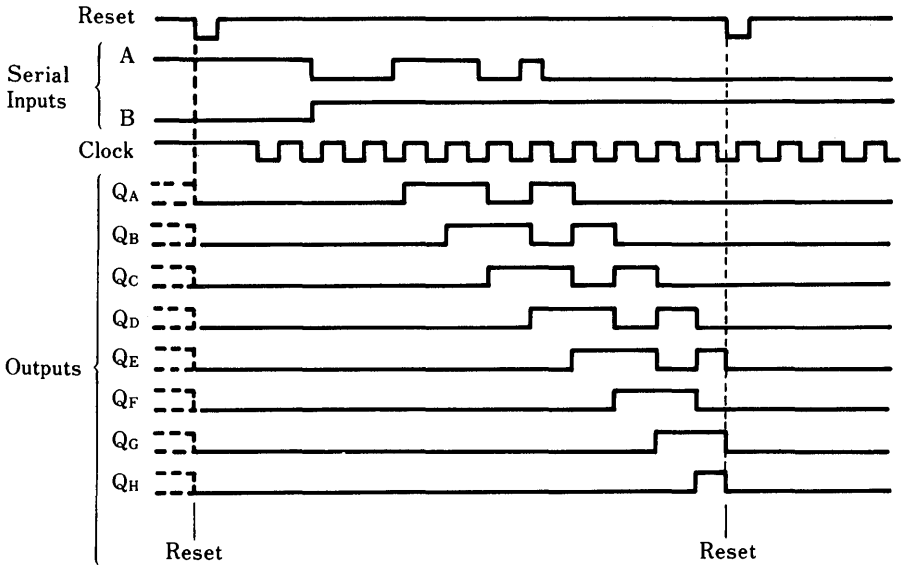
3.Waveforms



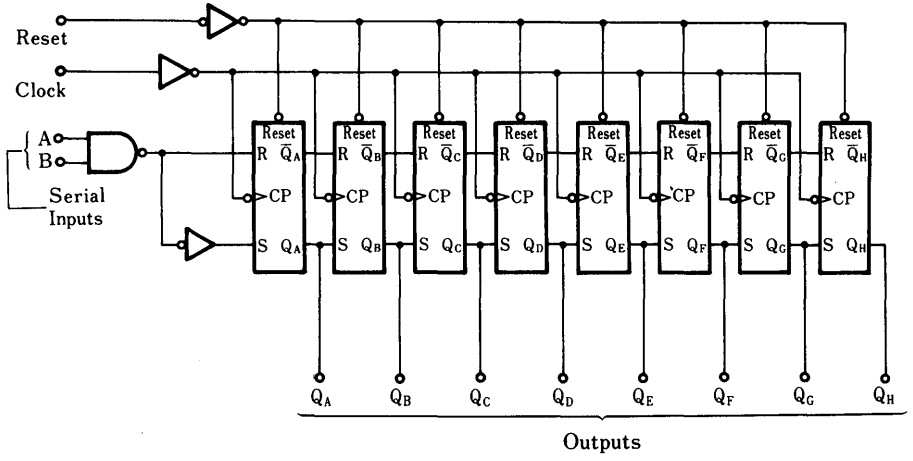
Notes

1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, clock and reset PRR = 1MHz, A and B PRR = 500kHz.
2. The above illustration is for output Q_A; refer to the timing chart for the timing of outputs Q_B through Q_H.

■ Timing chart



■ Logic diagram



DN74LS170

4-by-4 Register Files (with Open Collector Outputs)

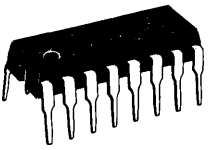
■ Description

DN74LS170 is a 4-word by 4-bit register file with open collector outputs.

■ Features

- Independent read address and write address for simultaneous data reading and writing
- Read and write enable inputs
- Memory capacity easily increased by using enable inputs
- "Wired" AND capability
- Wide operating temperature range (Ta = −20 to +75°C)

P-2

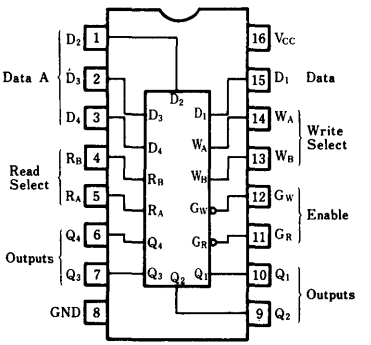


16-pin plastic DIL package

P-5

16-pin Panaflat package (SO-16D)

Pin configuration (top view)



■ Recommended operating conditions

Parameter		Sym	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
HIGH level output voltage		V_{OH}			5.5	V
LOW level output current		I_{OL}			8	mA
Operating temperature range		Topr	−20	25	75	℃
Pulse width	Read Enable	t_W	25			ns
	Write Enable		25			ns
Set-up time	Data Input	t_{SU}	10			ns
	Write Select		15			ns
Hold time	Data Input	th	15			ns
	Write Select		5			ns
Latch time		tlatch	25			ns

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter		Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Output voltage		V_{OL}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
				$I_{OL}=8mA$		0.35	0.5	V
Input current	Any D, R, or W	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
	G_R or G_W						40	μA
	Any D, R, or W	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
	G_R or G_W						−0.8	mA
	Any D, R, or W	I_I	$V_{CC}=5.25V$, $V_I=7V$				0.1	mA
	G_R or G_W						0.2	mA
Output short circuit current**		I_{OS}	$V_{CC}=4.75V$, $V_{OH}=5.5V$, $V_{IL}=0.8V$, $V_{IH}=2V$		−15		−100	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$, $I_I=-18mA$				−1.5	V
Supply current***		I_{CC}	$V_{CC}=5.25V$			25	40	mA

* When constant at V_{CC} = 5V, Ta = 25°C.

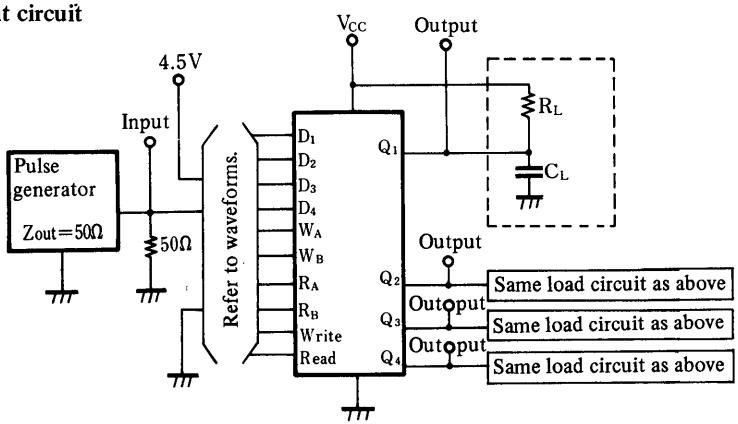
** I_{CC} is measured with all outputs open and 4.5V applied to data inputs and enable inputs.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	Read Enable	any Q	$C_L=15pF$, $R_L=2k\Omega$		20	30	ns
	t_{PHL}					20	30	ns
	t_{PLH}	Read Select	any Q			25	40	ns
	t_{PHL}					24	40	ns
	t_{PLH}	Write Enable	any Q			30	45	ns
	t_{PHL}					26	40	ns
	t_{PLH}	Data	any Q			30	45	ns
	t_{PHL}					22	35	ns

※ Switching parameter measurement information

1. Measurement circuit

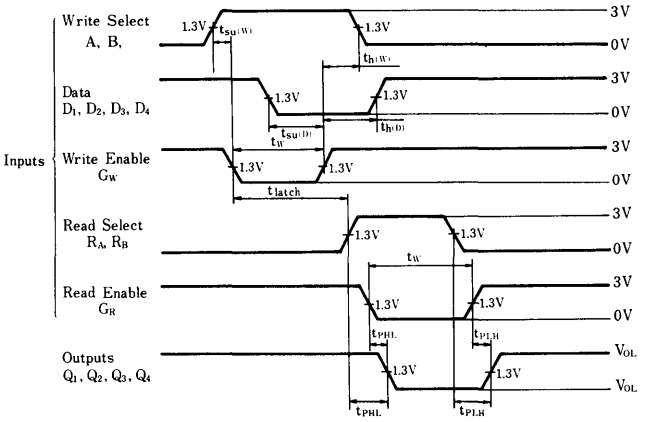


Notes

1. C_L includes probe and tool floating capacitance.

2. Waveforms

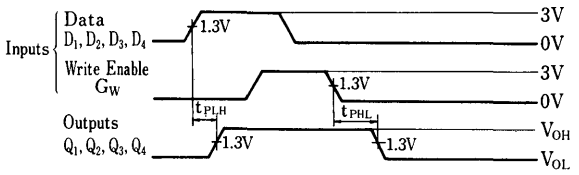
Waveforms-1



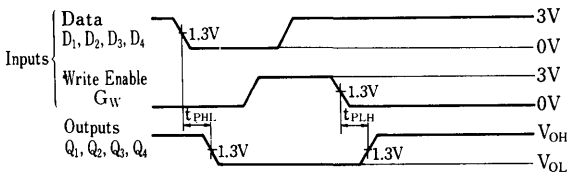
Notes

1. Input waveform; $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR=1MHz, duty cycle 50%

Waveforms-2



Waveforms-3



Notes

1. Input waveform; $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR=1MHz duty cycle 50%

■ .Truth tables

○Write Function Table

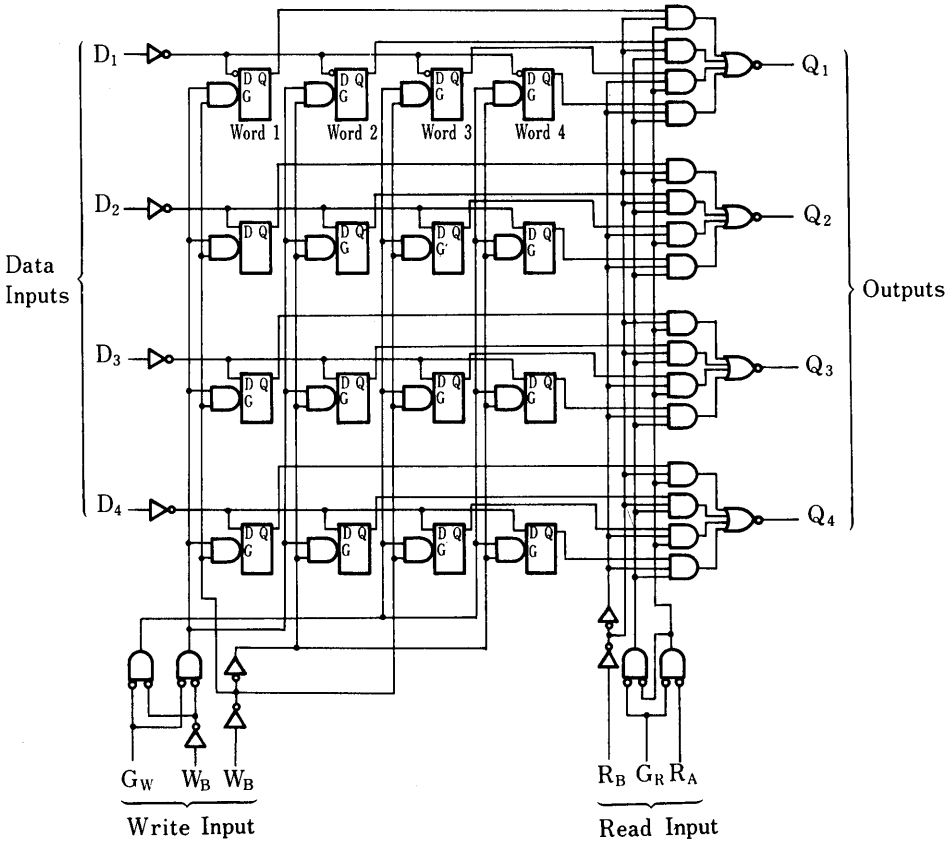
Write Inputs			Word			
W_B	W_A	G_W	0	1	2	3
L	L	L	Q=D	Q_0	Q_0	Q_0
L	H	L	Q_0	Q=D	Q_0	Q_0
H	L	L	Q_0	Q_0	Q=D	Q_0
H	H	L	Q_0	Q_0	Q_0	Q=D
×	×	H	Q_0	Q_0	Q_0	Q_0

○Read Function Table

Read Input			output			
R_B	R_A	G_R	Q_1	Q_2	Q_3	Q_4
L	L	L	W_{0B1}	W_{0B2}	W_{0B3}	W_{0B4}
L	H	L	W_{1B1}	W_{1B2}	W_{1B3}	W_{1B4}
H	L	L	W_{2B1}	W_{2B2}	W_{2B3}	W_{2B4}
H	H	L	W_{3B1}	W_{3B2}	W_{3B3}	W_{3B4}
×	×	H	H	H	H	H

Notes
H: HIGH voltage level.
L: LOW voltage level.
X: Either HIGH or LOW: doesn't matter.
Q_0: No change in word contents.
Q=D: Data input contents are written into specified word.
$W_X B_Y$: Indicates word X and bit Y contents.

■ Logic diagram



DN74LS173

4-bit D-type Registers (with 3-state Outputs)

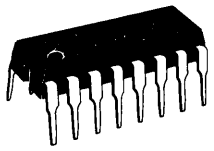
■ Description

DN74LS173 is a 4-bit register with 3-state outputs.

■ Features

- Capability for data holding irrespective of clock pulse number
- Data nondestructive during 3-state output
- Positive-edge trigger
- Number of bits easily increased
- Wide operating temperature range (Ta = −20 to +75°C)

P-2

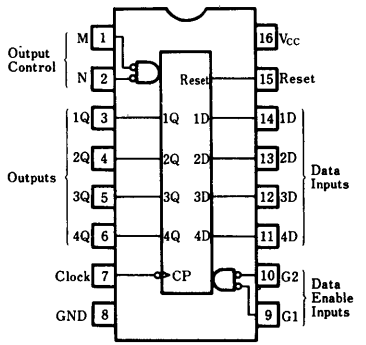


16-pin plastic DIL package

P-5

16-pin Panaflat package (SO-16D)

Pin configuration (top view)



■ Recommended operating conditions

Parameter		Sym	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}			−2.6	mA
Output current		I_{OL}			24	mA
Operating temperature range		Topr	−20	25	75	℃
Input clock frequency		f_{clock}	0		30	MHz
Clock and reset pulse widths		t_w	20			ns
Set-up time	Data Enable	t_{su}	35			ns
	Data		17			ns
	Reset Inactive State		17			ns
Hold time	Data Enable	t_h	0			ns
	Data		0			ns

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.4	3.1		V
	V_{OL1}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$	$I_{OL}=12mA$		0.25	0.4	V
	V_{OL2}		$I_{OL}=24mA$		0.35	0.5	V
Output OFF current	$I_{O(off)}$	$V_{CC}=5.25V$, $V_{IH}=2V$	$V_O=2.7V$			20	V
			$V_O=0.4V$			−20	V
Input current	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
	I_I	$V_{CC}=5.25V$, $V_I=7V$				0.1	mA
Output short circuit current**	I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−130	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$, $I_I=-18mA$				−1.5	V
Supply current***	I_{CC}	$I_{CC}=5.25V$			20	30	mA

* When constant at V_{CC} = 5V, Ta = 25°C.

** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

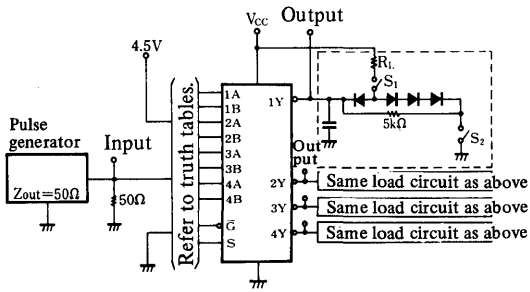
*** I_{CC} is measured with all outputs open, N, G_1, G_2 and all data inputs grounded, and 4.5V applied to clock inputs and M; 4.5V is applied momentarily to reset inputs, following which they are grounded.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Test conditions		Min	Typ	Max	Unit
Maximum clock frequency	f_{max}	$C_L=45pF$, $R_L=667\Omega$		30	50		MHz
Propagation delay time	t_{PHL}	Reset→Q	$C_L=45pF$, $R_L=667\Omega$		20	35	ns
	t_{PLH}	Clock→Q			16	25	ns
	t_{PHL}				20	30	ns
Tri-state outputs Enable time	t_{ZH}	$C_L=45pF$, $R_L=667\Omega$			13	23	ns
	t_{ZL}				24	27	ns
Tri-state outputs Disable time	t_{HZ}	$C_L=5pF$, $R_L=667\Omega$			11	17	ns
	t_{LZ}				15	17	ns

※ Switching parameter measurement information

1. Measurement circuit

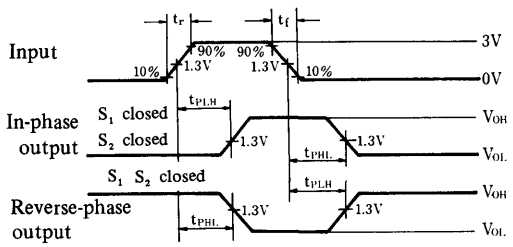


Notes

1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161 or equivalent.

2. Waveforms

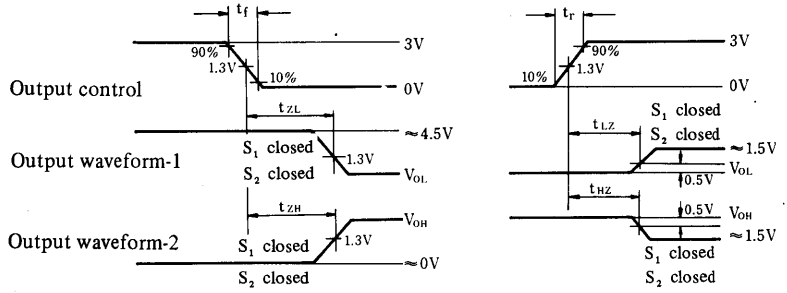
Waveforms−1



Notes

1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.

Waveforms-2



Notes

1. Input waveform: $t_r \leqq 15$ns, $t_f \leqq 6$ns, PRR = 1MHz, duty cycle = 50%.
2. Except when the output is disabled by the output control, output waveform-1 occurs as a result of internal conditions such as a LOW voltage level.
3. Except when the output is disabled by the output control, output waveform-2 occurs as a result of internal conditions such as a HIGH voltage level.
4. When measuring t_{PLH} and t_{PHL}, S_1 and S_2 are closed.

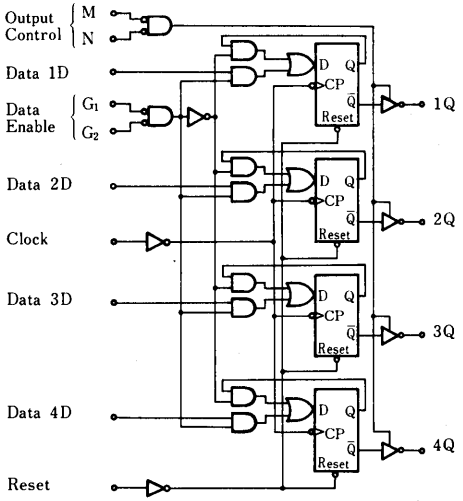
■ Truth tables

Inputs					Outputs
Reset	Clock	Data Enable		Data	
		G_1	G_2	D	Q
H	×	×	×	×	L
L	L	×	×	×	Q_0
L	↑	H	×	×	Q_0
L	↑	×	H	×	Q_0
L	↑	L	L	L	L
L	↑	L	L	H	H

Notes

1. H: HIGH voltage level.
2. L: LOW voltage level.
3. X: Either HIGH or LOW; doesn't matter.
4. When either or both output control inputs M and N are HIGH, the output is disabled to a high-impedance state. At this time, there is no effect on the continuous operation of the flip flop.

■ Logic diagram



DN74LS174

Hex D-type Flip Flops (with Reset)

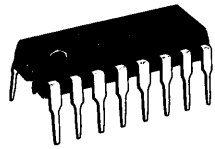
■ Description

DN74LS174 contains six positive-edge triggered D-type flip-flop circuits with common clock-CP and direct-coupled reset inputs, and independent data-D inputs.

■ Features

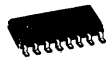
- Positive-edge trigger
- Common clock and direct-coupled reset inputs for all six circuits
- Q output
- Wide operating temperature range (Ta = −20 to +75°C)

P-2



16-pin plastic DIL package

P-5



16-pin Panaflat package (SO-16D)

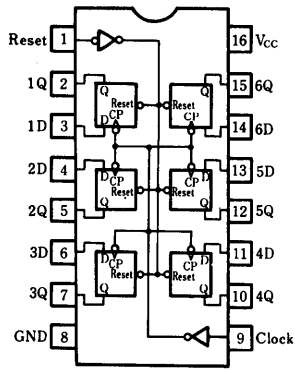
■ Truth tables

Inputs			Outputs
Reset	Clock	D	Q
L	×	×	L
H	↑	H	H
H	↑	L	L
H	L	×	Q_0

Notes

1. H: HIGH voltage level.
2. L: LOW voltage level.
3. X: Either HIGH or LOW; doesn't matter.
4. ↑: Change from LOW to HIGH.
5. Q_0: Q level prior to determination of constant condition input requirement.

Pin configuration (top view)



■ Recommended operating conditions

Parameter		Sym	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}			−400	μA
		I_{OL}			8	mA
Operating temperature range		Topr	−20	25	75	℃
Clock frequency		f_{clock}	0		30	MHz
Clock pulse width		$t_{W(CP)}$	20			ns
Reset pulse width		$t_{W(Reset)}$	20			ns
Set-up time	Data input	$t_{su(D)}$	20			ns
	Reset (non-operating condition)	$_{Reset)}$	25			ns
Data hold time		$t_{h(D)}$	5			ns

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$ $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	3.4		V
	V_{OL1}	$V_{CC}=4.75V$ $V_{IH}=2V$ $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
	V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				20	μA
	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.4	mA
	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.1	mA
Output short circuit current**	I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−100	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current***	I_{CC}	$V_{CC}=5.25V$			16	26	mA

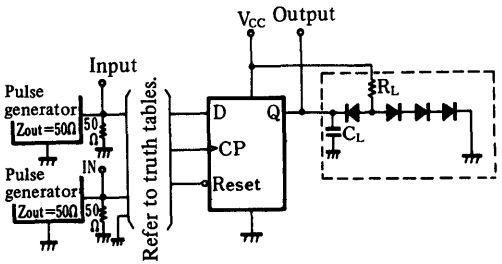
* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.
*** Measured with all outputs open and 4.5V applied to all data and reset inputs; clock inputs grounded momentarily, following which they are grounded.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Maximum clock frequency	f_{max}	Clock	Q	$C_L=15pF$ $R_L=2k\Omega$	30	40		MHz
Propagation delay time	t_{PHL}	Reset	Q			23	35	ns
	t_{PLH}	Clock	Q			20	30	ns
	t_{PHL}					21	30	ns

※ Switching parameter measurement information

1. Measurement circuit

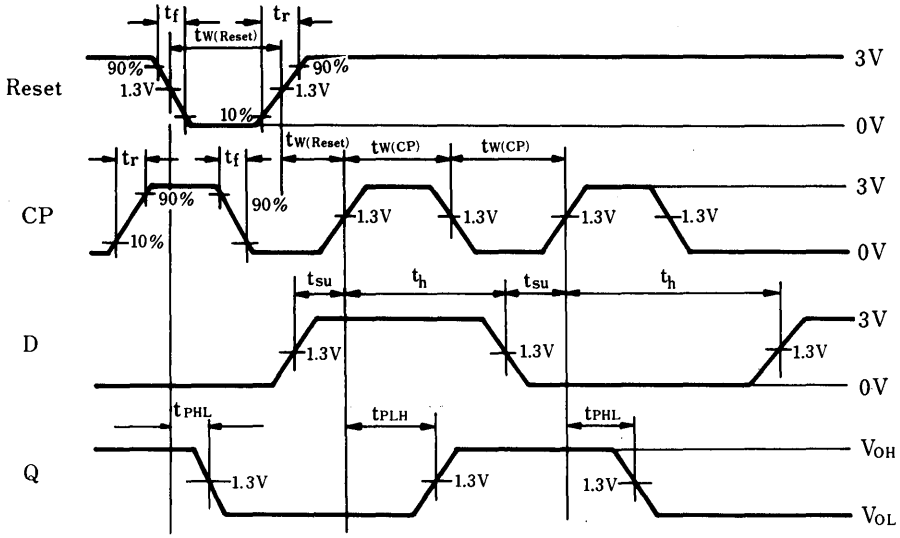


2. Table of measurement requirements

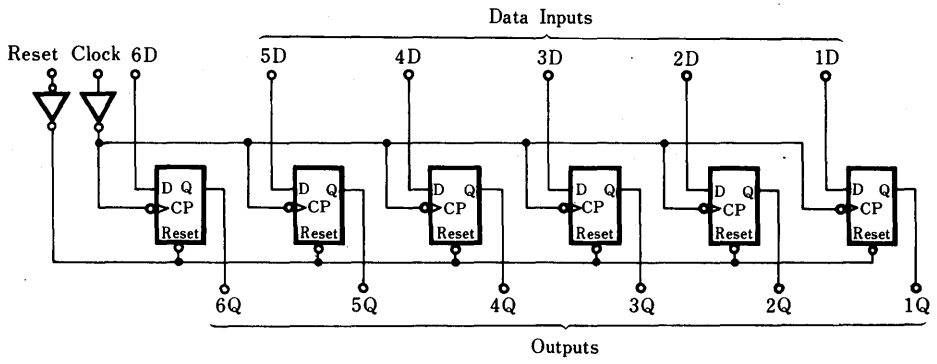
Parameter	Input / Output	Inputs			Outputs
		Reset	Clock	D	Q
f_{max}	CP→Q	4.5V	IN	IN	OUT
t_{PLH}	CP→Q	4.5V	IN	IN	
t_{PHL}	Resct→Q	IN	IN	4.5V	

1. Measurement made for each flip flop.
2. C_L includes probe and tool floating capacitance.
3. Diodes are all MA161.

3.Waveforms



■ Logic diagram



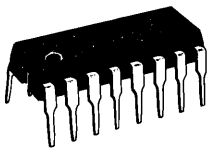
DN74LS175

Quad D-type Flip-Flops (with Reset)

■ Description

DN74LS175 contains four positive-edge triggered D-type flip-flop circuits with common clock-CP and direct-coupled reset inputs, and independent data-D inputs.

P-2



16-pin plastic DIL package

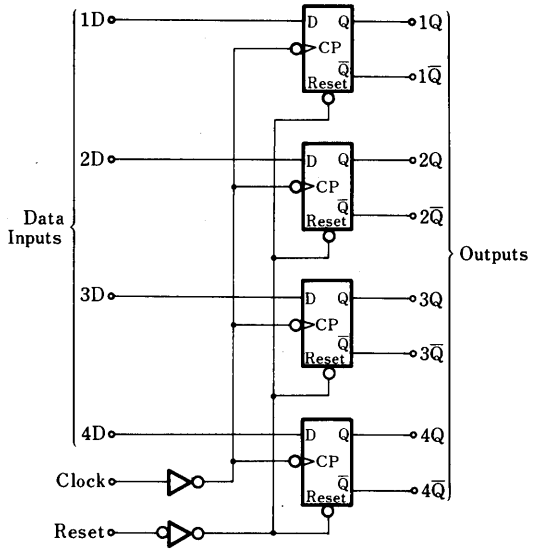
P-5

16-pin Panaflat package (SO-16D)

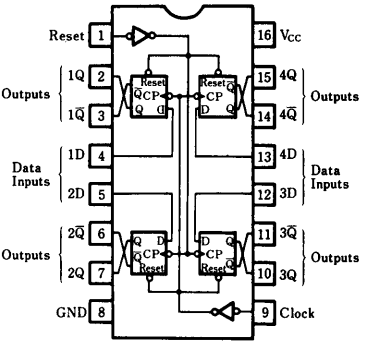
■ Features

- Positive-edge trigger
- Common clock and direct-coupled reset inputs for all four circuits
- Q and $\overline{Q}$ outputs
- Wide operating temperature range (Ta = −20 to +75°C)

■ Logic diagram



Pin configuration (top view)



■ Recommended operating conditions

Parameter		Sym	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}			−400	μA
		I_{OL}			8	mA
Operating temperature range		Topr	−20	25	75	℃
Clock frequency		f_{clock}	0		30	MHz
Clock pulse width		$t_{W(CP)}$	20			ns
Reset pulse width		$t_{W(Reset)}$	20			ns
Set-up time	Data input	$t_{su(D)}$	20			ns
	Reset (non-operating condition)	$t_{su(R)}$	25			ns
Data hold time		$t_{h(D)}$	5			ns

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$ $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	3.4		V
	V_{OL1}	$V_{CC}=4.75V$ $V_{IH}=2V$ $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
	V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				20	μA
	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.4	mA
	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.1	mA
Output short circuit current**	I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−100	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current***	I_{CC}	$V_{CC}=5.25V$			11	18	mA

* When constant at V_{CC} = 5V, Ta = 25°C.

** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

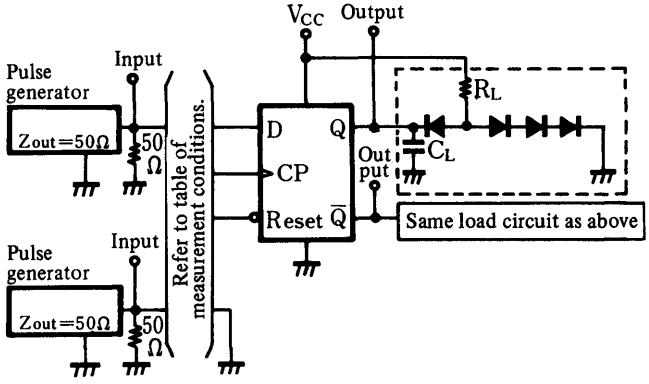
*** Measured with all outputs open and 4.5V applied to all date and reset inputs; clock inputs grounded momentarily, following which they are grounded.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Maximum clock frequency	f_{max}	Clock	Q, $\overline{Q}$	$C_L=15pF$ $R_L=2k\Omega$	30	40		MHz
Propagation delay time	t_{PLH}	Reset	$\overline{Q}$			16	25	ns
	t_{PHL}		Q			23	35	ns
	t_{PLH}	Clock	Q, $\overline{Q}$			20	30	ns
	t_{PHL}					21	30	ns

※ Switching parameter measurement information

1. Measurement circuit

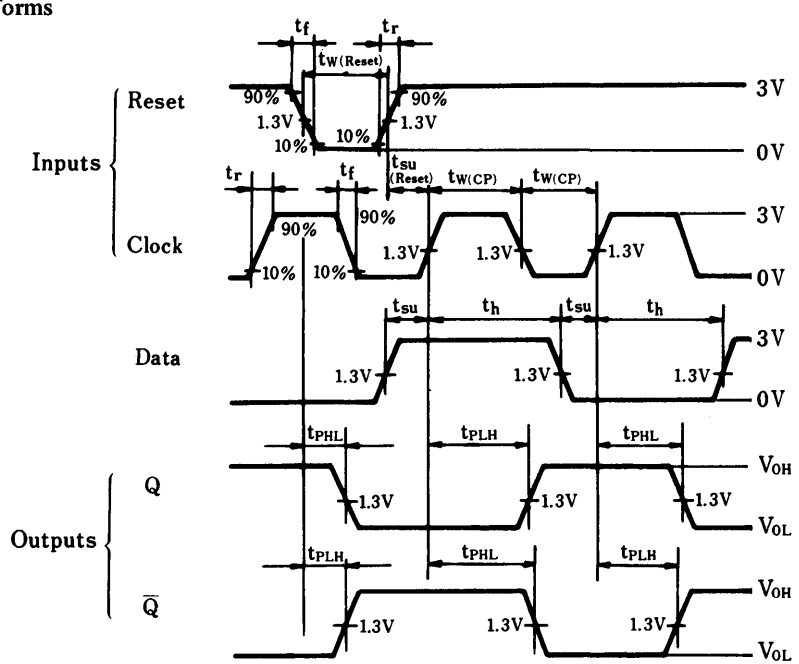


1. Measurement made for each flip flop.
2. C_L includes probe and tool floating capacitance.
3. Diodes are all MA161 or equivalent.

2. Table of measurement conditions

Parameter	Inputs/Outputs	Inputs			Outputs	
		Reset	CP	D	Q	$\overline{Q}$
f_{max}	CP→Q, $\overline{Q}$	4.5V	IN	IN	OUT	OUT
t_{PLH}	CP→Q, $\overline{Q}$	4.5V	IN	IN		
t_{PHL}	Reset→Q, $\overline{Q}$	IN	IN	4.5V		

3.Waveforms



Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz.
2. When measuring f_{max}, t_r and $t_f \leqq 2.5ns$.

■ Truth tables

Inputs			Outputs	
Reset	Clock	D	Q	$\overline{Q}$
L	×	×	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	×	Q_0	$\overline{Q}_0$

Notes
1. H: HIGH voltage level.
   L: LOW voltage level.
2. ↑: Change from LOW to HIGH.
3. X: Either HIGH or LOW; doesn't matter.
4. Q_0: Q level prior to determination of constant input requirement.

DN74LS190

Synchronous BCD Up / Down Counters (with Up / Down Mode Control)

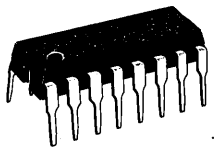
■ Description

DN74LS190 is a synchronous decade up/down counter with up/down control inputs and set inputs.

■ Features

- Up/down switching according to up/down control input
- Asynchronous set input
- Enable input
- Easy cascade connection
- High-speed counting (f_{max} = 25MHz typical)
- Wide operating temperature range (Ta = −20 to +75°C)

P-2

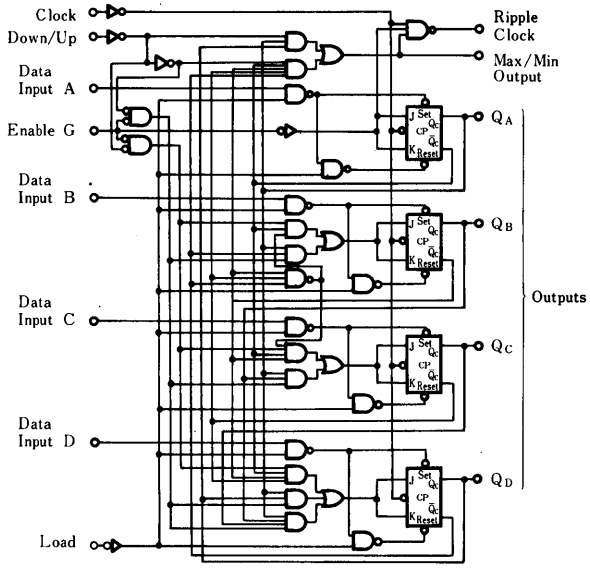


16-pin plastic DIL package

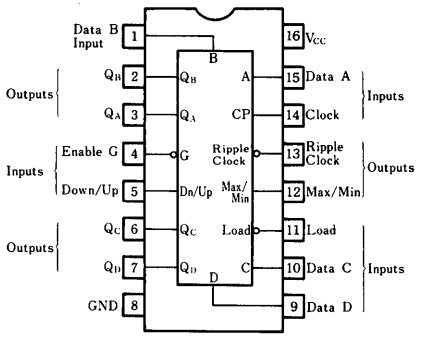
P-5

16-pin Panaflat package (SO-16D)

■ Logic diagram



Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−400	μA
	I_{OL}			8	mA
Operating temperature range	Topr	−20	25	75	℃
Clock frequency	f_{clock}	0		20	MHz
Clock pulse width	$t_{W(CP)}$	30			ns
Load pulse width	$t_{W(Load)}$	35			ns
Set-up time	t_{su}	20			ns
Hold time	t_h	0			ns
Enable time	t_{enable}	40			ns

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter		Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Output voltage		V_{OH}	$V_{CC}=4.75V$, $I_{OH}=-400\mu A$ $V_{IH}=2V$, $V_{IL}=0.8V$		2.7	3.4		V
		V_{OL}	$V_{CC}=4.75V$ $V_{IH}=2V$ $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
				$I_{OL}=8mA$		0.35	0.5	V
Input current	Enable	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				60	μA
	Others						20	μA
	Enable	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−1.2	mA
	Others						−0.4	mA
	Enable	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.3	mA
	Others						0.1	mA
Output short circuit current**		I_{OS}	$V_{CC}=5.25V$ $V_O=0V$		−15		−100	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current***		I_{CC}	$V_{CC}=5.25V$			20	35	mA

* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.
*** Measured with all outputs open and all inputs grounded.

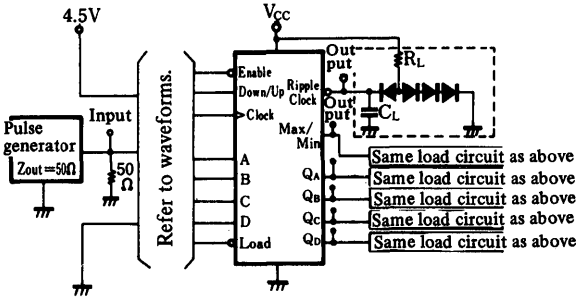
■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Maximum clock frequency	f_{max}	Clock	Q_A, Q_B Q_C, Q_D	$C_L=15pF$ $R_L=2k\Omega$	20	25		MHz
Propagation delay time	t_{PLH}	Load	Q_A, Q_B Q_C, Q_D			22	30	ns
	t_{PHL}					33	50	ns
	t_{PLH}	A, B C, D	Q_A, Q_B Q_C, Q_D			20	32	ns
	t_{PHL}					27	50	ns
	t_{PLH}	Clock	Ripple Clock			13	20	ns
	t_{PHL}					16	24	ns
	t_{PLH}	Clock	Q_A, Q_B Q_C, Q_D			16	24	ns
	t_{PHL}					24	42	ns
	t_{PLH}	Clock	Max/Min			28	42	ns
	t_{PHL}					37	52	ns
	t_{PLH}	Down/Up	Ripple Clock			30	45	ns
	t_{PHL}					30	45	ns
	t_{PLH}	Down/Up	Max/Min			21	33	ns
	t_{PHL}					22	33	ns
	t_{PLH}	Enable	Ripple Clock			21	33	ns
	t_{PHL}					22	33	ns

※ Switching parameter measurement information

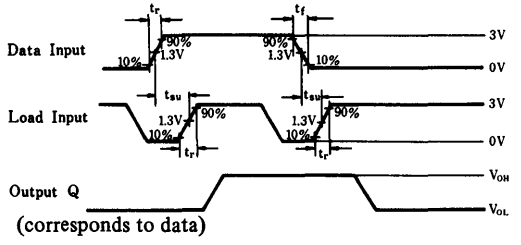
〔1〕 f_{max}, t_{PLH}, t_{PHL} (Clock → Q, $\overline{Q}$)

1. Measurement circuit



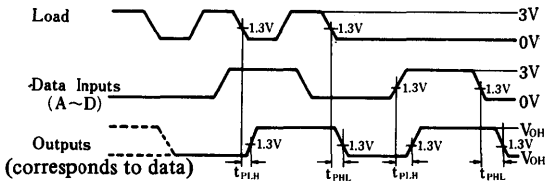
1. Number of pulse generators increased as needed.
2. C_L includes probe and tool floating capacitance.
3. Diodes are all MA161.

2. Waveforms



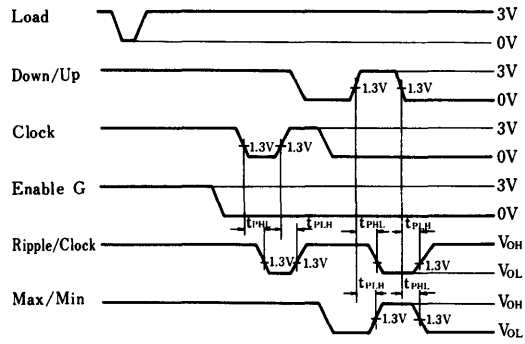
Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.

Waveforms-1 Load → Q, Date → Q



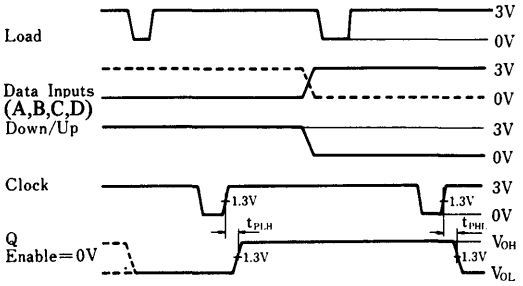
Notes
1. All other inputs are 4.5V.

Waveforms-2 G → Ripple CP, CP → Ripple CP, Down/UP → Ripple CP, Down/ Up → Max/Min



Notes
1. All data inputs are 0V.

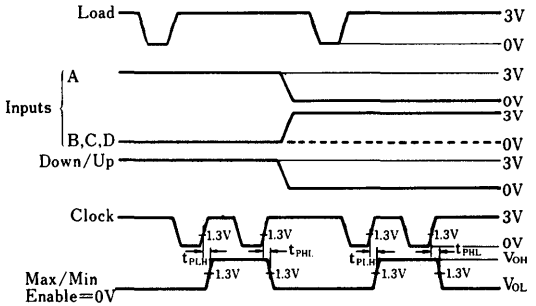
Waveforms-3 Clock → Q



Notes

1. When measuring Q_A, Q_B, and Q_C outputs, refer to the solid line for data inputs A, B, and C, and to the dashed line for input D.
2. When measuring Q_D output, refer to the solid line for data inputs A and D; B and C inputs are 0V.

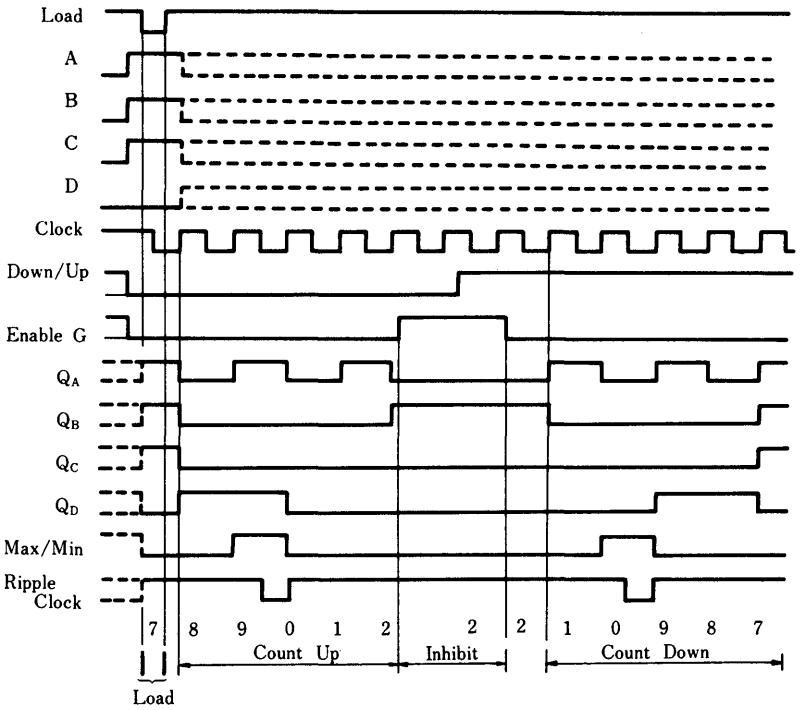
Waveforms-4 Clock → Max/Min



Notes

1. Refer to the dashed line for data inputs B and C, and to the solid line for data input D.

■ Timing chart



Count order

1. Load (set) at 7 (BCD).
2. Count up at 8, 9 (max), 0, 1, 2.
3. Inhibit.
4. Count down at 1, 0 (min), 9, 8, 7.

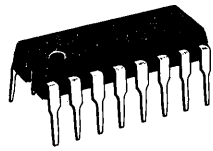
DN74LS191

Synchronous 4-bit Binary Up / Down Counters (with Up / Down Mode Control)

■ Description

DN74LS191 is a synchronous 4-bit binary (hexadecimal) couter with up/down control inputs and set input.

P-2



16-pin plastic DIL package

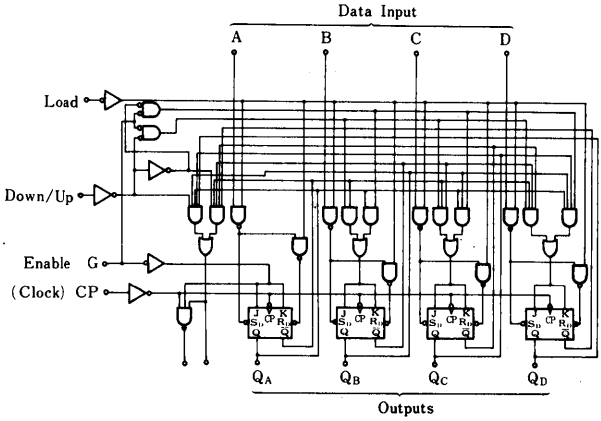
P-5

16-pin Panaflat package (SO-16D)

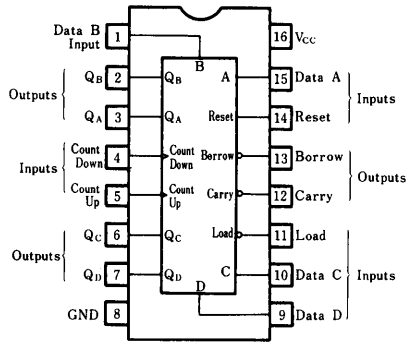
■ Features

- Up/down switching according to up/down control input
- Asynchronous set input
- Enable input
- Easy cascade connection
- High-speed counting (f_{max} = 25MHz typical)
- Wide operating temperature range (Ta = −20 to +75°C)

■ Logic diagram



Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−400	μA
	I_{OL}			8	mA
Operating temperature range	Topr	−20	25	75	℃
Clock frequency	f_{clock}	0		20	MHz
Clock pulse width	$t_{W(CP)}$	25			ns
Load pulse width	$t_{W(Load)}$	35			ns
Set-up time	t_{su}	20			ns
Hold time	t_h	5			ns
Enable time	t_{enable}	40			ns

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter		Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Output voltage		V_{OH}	$V_{CC}=4.75V$, $I_{OH}=-400\mu A$ $V_{IH}=2V$, $V_{IL}=0.8V$		2.7	3.4		V
		V_{OL}	$V_{CC}=4.75V$ $V_{IH}=2V$ $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
				$I_{OL}=8mA$		0.35	0.5	V
Input current	Enable	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				60	μA
	Others						20	μA
	Enable	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−1.2	mA
	Others						−0.4	mA
	Enable	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.3	mA
	Others						0.1	mA
Output short circuit current**		I_{OS}	$V_{CC}=5.25V$ $V_O=0V$		−15		−100	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current***		I_{CC}	$V_{CC}=5.25V$			20	35	mA

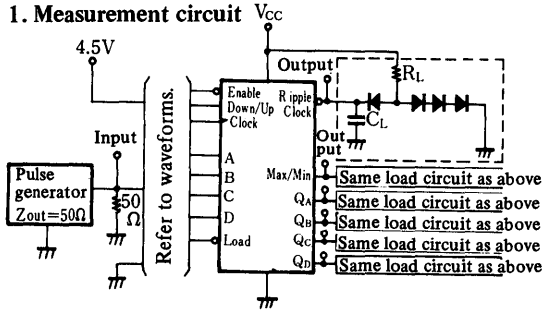
* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.
*** Measured with all outputs open and all inputs grounded.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$ constant)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Maximum clock frequency	f_{max}			$C_L=15pF$ $R_L=2k\Omega$	20	25		MHz
Propagation delay time	t_{PLH}	Load	Q_A, Q_B Q_C, Q_D			22	33	ns
	t_{PHL}					23	50	ns
	t_{PLH}	Data A, B, C, D	Q_A, Q_B Q_C, Q_D			20	32	ns
	t_{PHL}					33	40	ns
	t_{PLH}	Clock	Ripple Clock			13	20	ns
	t_{PHL}					16	24	ns
	t_{PLH}	Clock	Q_A, Q_B Q_C, Q_D			16	24	ns
	t_{PHL}					24	36	ns
	t_{PLH}	Clock	Max/Min			28	42	ns
	t_{PHL}					37	52	ns
	t_{PLH}	Down / Up	Ripple Clock			30	45	ns
	t_{PHL}					30	45	ns
	t_{PLH}	Down / Up	Max/Min			21	33	ns
	t_{PHL}					22	33	ns
	t_{PLH}	Enable	Ripple Clock			21	33	ns
	t_{PHL}					22	33	ns

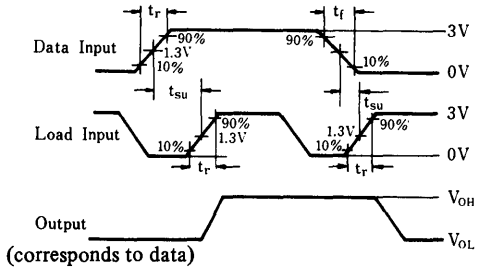
※ Switching parameter measurement information

1. Measurement circuit V_{CC}



1. Number of pulse generators increased as needed.
2. C_L includes probe and tool floating capacitance.
3. Diodes are all MA161.

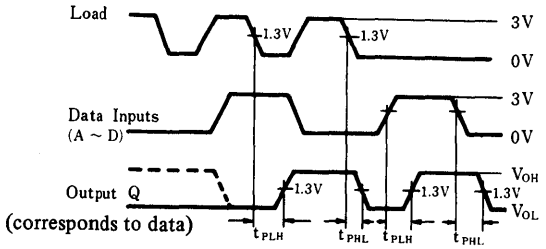
2. Waveforms



Notes

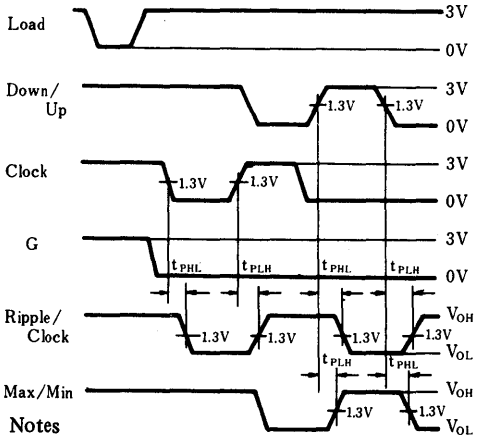
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.

Waveforms-1 Load → Q, Data → Q



Note: All other inputs are 4.5V.

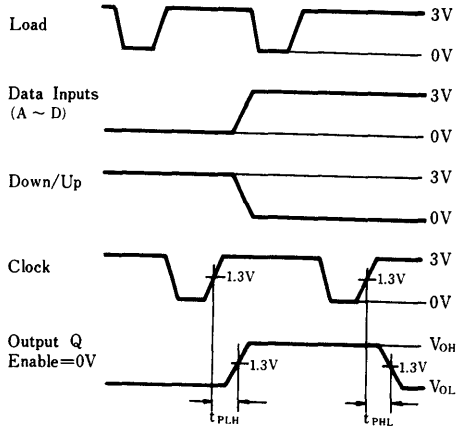
Waveforms-2 G → Ripple CP, CP → Ripple CP, Down/Up → Ripple CP, Down/UP → Max/Min



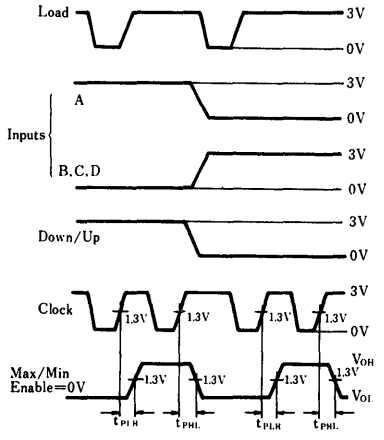
Notes

1. All data inputs are 0V.

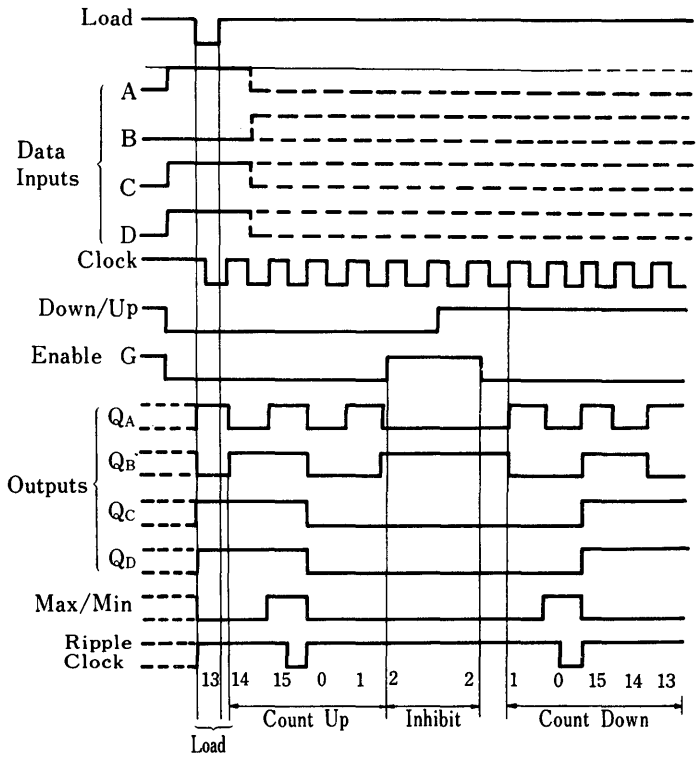
Waveforms-3 Clock → Q



Waveforms-4 Clock → Max/Min



■ Timing chart



Count order
1. Load (set) at binary 13.
2. Count up at 14, 15 (max), 0, 1, 2.
3. Inhibit.
4. Count down at 2, 1, 0 (min), 15, 14, 13.

DN74LS192

Synchronous BCD Up / Down Dual Clock Counters (with Reset)

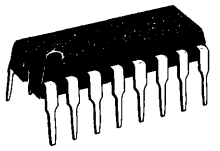
■ Description

DN74LS192 is a synchronous decade up/down counter with direct-coupled reset input and set input.

■ Features

- Exclusive clock input for up count and down count
- Asynchronous set input
- Direct-coupled reset input
- Easy cascade connection
- High-speed counting (f_{max} = 32MHz typical)
- Wide operating temperature range (Ta = −20 to +75°C)

P-2

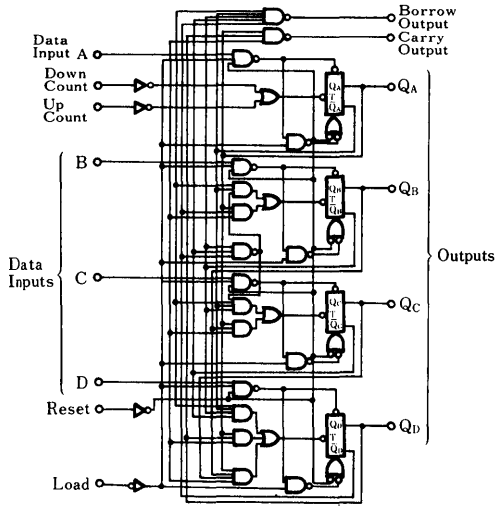


16-pin plastic DIL package

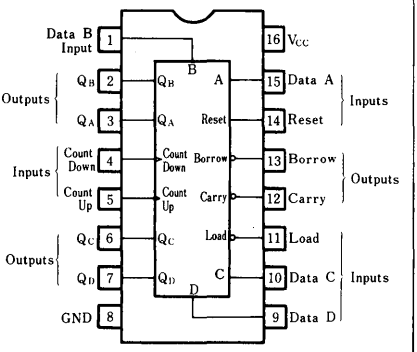
P-5

16-pin Panaflat package (SO-16D)

■ Logic diagram



Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−400	μA
	I_{OL}			8	mA
Operating temperature range	Topr	−20	25	75	℃
Clock frequency	f_{clock}	0		20	MHz
Clock pulse width	$t_{W(CP)}$	20			ns
Load pulse width	$t_{W(Load)}$	20			ns
Set-up time	t_{su}	20			ns
Hold time	t_h	5			ns
Enable time	t_{enable}	40			ns

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$ $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	3.4		V
	V_{OL1}	$V_{CC}=4.75V$ $V_{IH}=2V$ $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
	V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				20	μA
	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.4	mA
	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.1	mA
Output short circuit current**	I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−100	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current***	I_{CC}	$V_{CC}=5.25V$			19	34	mA

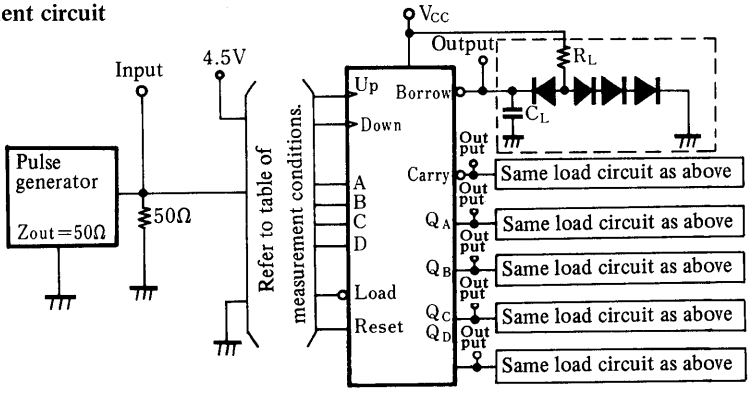
* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.
*** Measured with all outputs open, reset and load inputs grounded, and 4.5V applied to all other inputs.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Maximum clock frequency	f_{max}			$C_L=15pF$ $R_L=2k\Omega$	25	32		MHz
Propagation delay time	t_{PLH}	Count up	Carry			17	26	ns
	t_{PHL}					18	24	ns
	t_{PLH}	Count down	Borrow			16	24	ns
	t_{PHL}					15	24	ns
	t_{PLH}	Either count	Q			27	38	ns
	t_{PHL}		Q			30	47	ns
	t_{PLH}	Load	Q			24	40	ns
	t_{PHL}		Q			25	40	ns
	t_{PHL}	Reset	Q			23	35	ns

※ Switching parameter measurement information

1. Measurement circuit



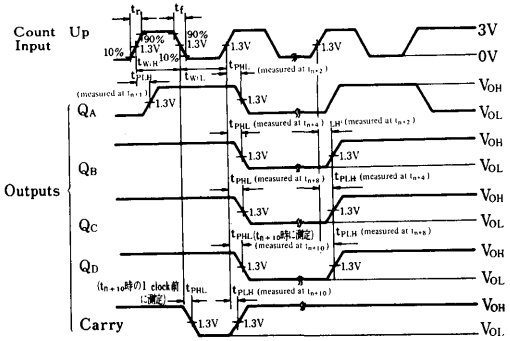
2. Table of measurement conditions

Para-meter	Input Output	Inputs								Outputs					
		Reset	Load	Up	Down	A	B	C	D	Q_A	Q_B	Q_C	Q_D	Carry	Borrow
f_{max}		GND	4.5V	IN	4.5V	GND	GND	GND	GND	OUT	OUT	OUT	OUT	OUT	
		GND	4.5V	4.5V	IN	GND	GND	GND	GND	OUT	OUT	OUT	OUT		OUT
t_{PLH} t_{PHL}	Up Count	GND	4.5V	IN	4.5V	GND	GND	GND	GND	OUT	OUT	OUT	OUT	OUT	
	Down Count	GND	4.5V	4.5V	IN	GND	GND	GND	GND	OUT	OUT	OUT	OUT		OUT
	Load→Q	GND	IN	GND	GND	IN	IN	IN	IN	OUT	OUT	OUT	OUT		
	Reset→Q	IN	IN*	GND	GND	4.5V	4.5V	4.5V	4.5V	OUT	OUT	OUT	OUT		

* Applied for initialization.

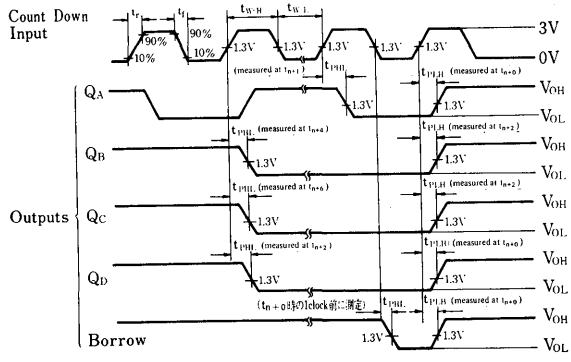
3.Waveforms

Waveforms-1 f_{max}, t_{PLH}, t_{PHL} (Count Up時)



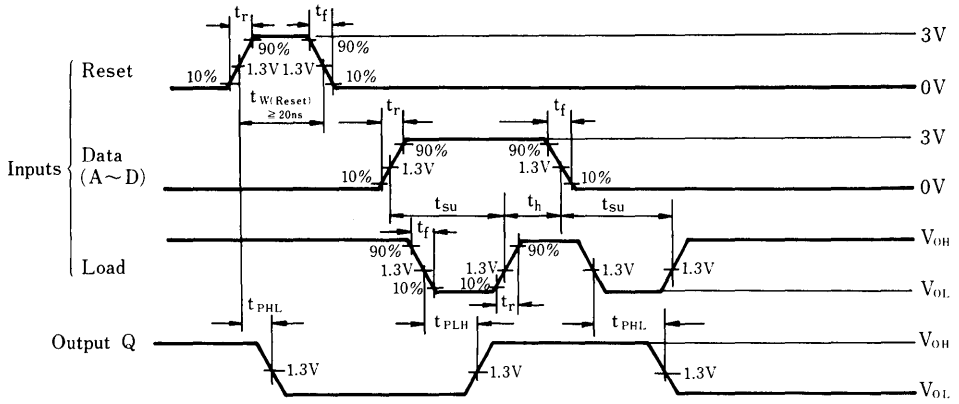
Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.
2. Pulse generator output impedance: Z_{out} = 50 ohms.
3. t_n is the bit time when all outputs are LOW.

Waveforms-2 f_{max}, t_{PLH}, t_{PHL} (Count Down時)



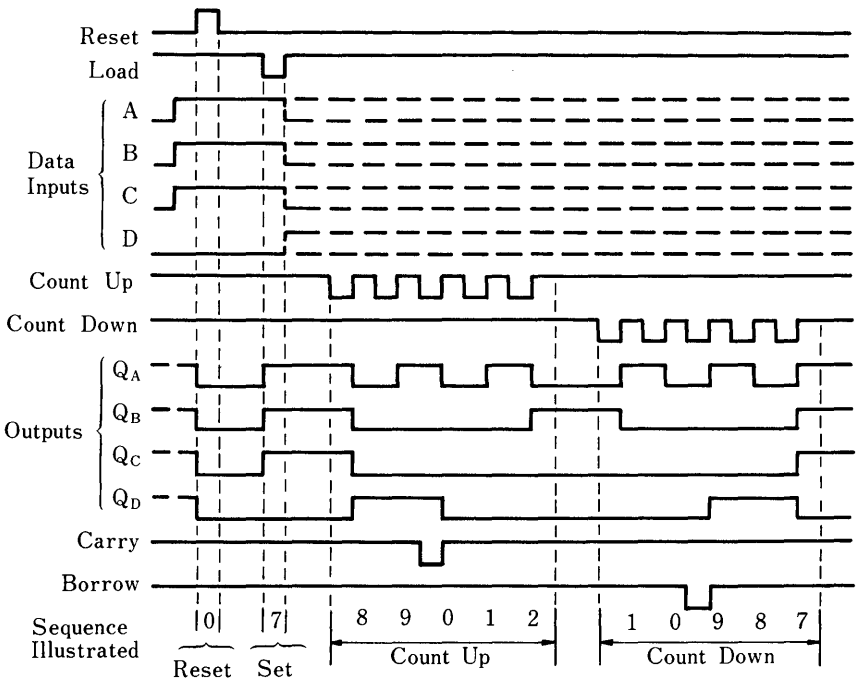
Notes
1. When measuring f_{max}, t_r and $t_f \leqq 2.5ns$.
2. t_n is the bit time when all outputs are LOW.

Waveforms—3 t_{PLH}, t_{PHL} (Load, Reset → Q)



Notes
1. Input waveform ; $t_r \leqq 7ns$, $t_f \leqq 7ns$

■ Timing chart



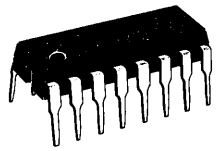
DN74LS193

Synchronous 4-bit Binary Up / Down Dual Clock Counters (with Reset)

■ Description

DN74LS193 is a synchronous hexadecimal (4-bit binary) up/down counter with direct-coupled reset input and set input.

P-2



16-pin plastic DIL package

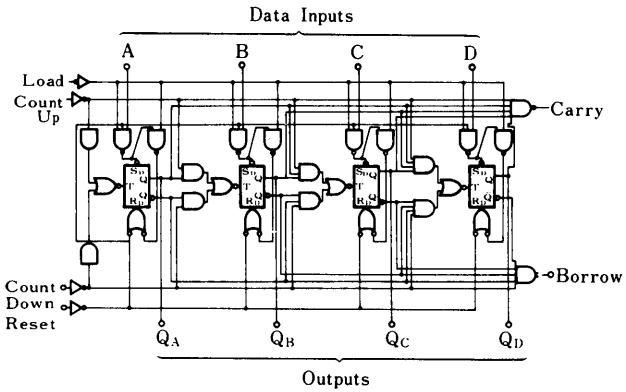
P-5

16-pin Panaflat package (SO-16D)

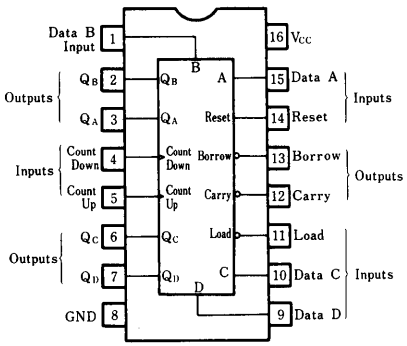
■ Features

- Exclusive clock input for up count and down count
- Asynchronous set input
- Direct-coupled reset input
- Easy cascade connection
- High-speed counting (f_{max} = 32MHz typical)
- Wide operating temperature range (Ta = −20 to +75°C)

■ Logic diagram



Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−400	μA
Output current	I_{OL}			8	mA
Operating temperature range	Topr	−20	25	75	℃
Clock frequency	f_{clock}	0		25	MHz
Pulse width	t_W	20			ns
Set-up time (reset)	t_{su} (Reset)	20			ns
Set-up time	t_{su}	20			ns
Hold time	t_h	5			ns
Enable time	t_{enable}	40			ns

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$ $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	3.4		V
	V_{OL1}	$V_{CC}=4.75V$ $V_{IH}=2V$ $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
	V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				20	μA
	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.4	mA
	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.1	mA
Output short circuit current**	I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−100	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current***	I_{CC}	$V_{CC}=5.25V$			19	34	mA

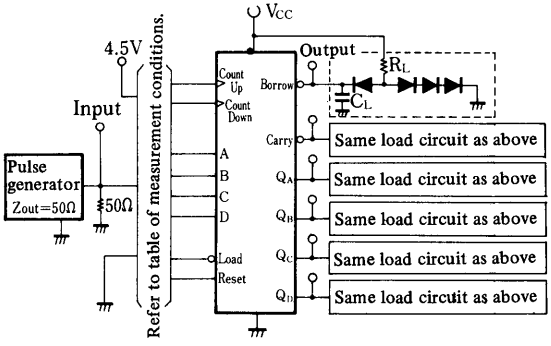
* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 sec.
*** Measured with all outputs open, reset and load inputs grounded, and 4.5V applied to all other inputs.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Maximum clock frequency	f_{max}			$C_L=15pF$ $R_L=2k\Omega$	25	32		MHz
Propagation delay time	t_{PLH}	Count Up	Carry			17	26	ns
	t_{PHL}					18	24	ns
	t_{PLH}	Count Down	Borrow			16	24	ns
	t_{PHL}					15	24	ns
	t_{PLH}	Either Count	Q			27	38	ns
	t_{PHL}					30	47	ns
	t_{PLH}	Load	Q			24	40	ns
	t_{PHL}					25	40	ns
	t_{PHL}	Reset	Q			23	35	ns

※ Switching parameter measurement information

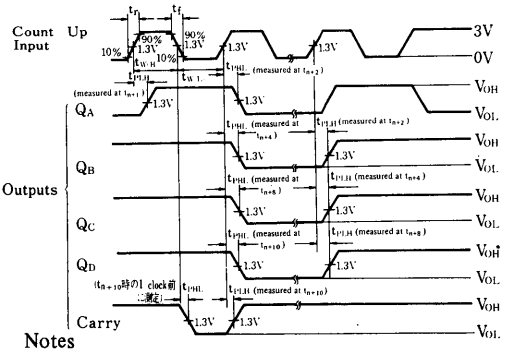
1. Measurement circuit



1. Number of pulse generators increased as needed.
2. C_L includes probe and tool floating capacitance.
3. Diodes are all MA161.

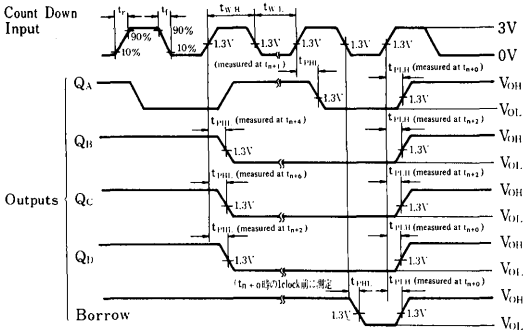
2. Waveforms

Waveforms-1 . f_{max}, t_{PLH}, t_{PHL} (Count Up時)

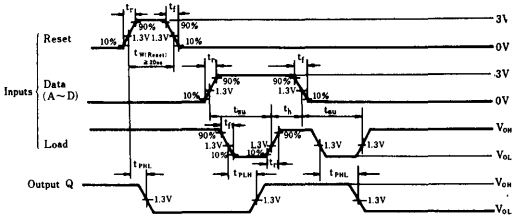


Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 5ns$, PRR = 1MHz, duty cycle = 50%.
2. When measuring f_{max}, t_r and $t_f \leqq 2.5ns$.
3. t_n is the bit time when all outputs are LOW.

Waveforms-2 f_{max}, t_{PLH}, t_{PHL} (Count Down時)



Waveforms-3 t_{PLH}, t_{PHL} (Load, Reset → Q)



Notes
1. Input waveform: $t_r \leqq 7$ ns, $t_f \leqq 7$ns, PRR = 1 MHz, duty cycle = 50%.
2. When measuring f_{max}, t_r and $t_f \leqq 2.5$ns.
3. t_n is the bit time when all outputs are HIGH.

Notes
1. Input waveform: $t_r \leqq 7$ns, $t_f \leqq 7$ns

3. Table of measurement conditions

Parameter	Mode	Inputs					Outputs		
		Reset	Load	Count up	Count down	$D_A \sim D_D$	$Q_A \sim Q_D$	Carry	Borron
f_{max}	Count up	GND	4.5V	IN	4.5V	GND	OUT	OUT	
	Count down	GND	4.5V	4.5V	IN	GND	OUT		OUT
t_{PLH} t_{PHL}	Count up	GND	4.5V	IN	4.0V	GND	OUT	OUT	
	Count down	GND	4.5V	4.5V	N	GND	OUT		OUT
	Load	GND	IN	GND	GND	IN	OUT		
	Reset	IN	IN*	GND	GND	4.5V	OUT		

* Applied for initialization.

■ Input pulse conditions

t_W = min 20ns (Count up/Count down/Load/Reset)
t_S = min 20ns (Data to Load)
t_h = min 0ns (Data to Load)
t_r = min 40ns (Load/Reset to Count up/Count down)

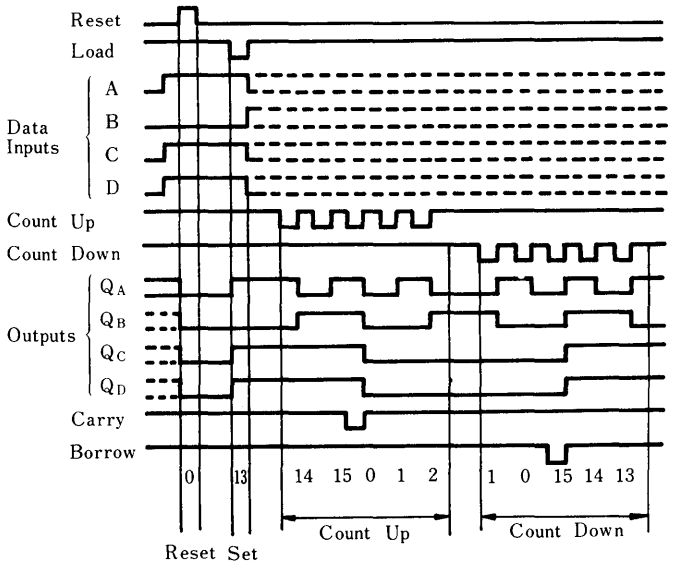
■ Truth tables

Operation mode	Inputs								Outputs					
	Reset	Lood	Count Up	Count Down	D_A	D_B	D_C	D_D	Q_A	Q_B	Q_C	Q_D	Carry	Borrow
Reset	H	×	×	L	×	×	×	×	L	L	L	L	H	L
	H	×	×	H	×	×	×	×	L	L	L	L	H	H
Load	L	L	×	L	L	L	L	L	L	L	L	L	H	L
	L	L	×	H	L	L	L	L	L	L	L	L	H	H
	L	L	L	×	H	H	H	H	H	H	H	H	L	H
	L	L	H	×	H	H	H	H	H	H	H	H	H	H
Count up	L	H	⊓	H	×	×	×	×	Count up				H [1]	H
Count down	L	H	H	⊓	×	×	×	×	Count down				H	H [2]

1) Carry = Count up, $Q_A \cdot \overline{Q_B} \cdot \overline{Q_C} \cdot \overline{Q_D}$
2) Borrow = Count down, $\overline{Q_A} \cdot \overline{Q_B} \cdot \overline{Q_C} \cdot \overline{Q_D}$

Notes
1. H: HIGH voltage level.
2. L: LOW voltage level.
3. X: Either HIGH or LOW; doesn't matter.
4. ⊓ : Change from LOW to HIGH.

■ Timing chart



Notes
1. Reset takes preference over load, data, and count inputs.
2. During the count up the count down input is HIGH, and during the count down the count up input is HIGH.

DN74LS194A

4-bit Bidirectional Universal Shift Registers

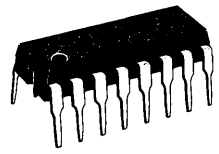
■ Description

DN74LS194A is a bidirectional 4-bit serial/parallel input to serial/parallel output shift register.

■ Features

- Synchronous serial/parallel input to serial/parallel output
- Right shift and left shift
- Mode-control input
- Direct-coupled reset input
- Hold mode function
- Wide operating temperature range (Ta = −20 to +75°C)

P-2

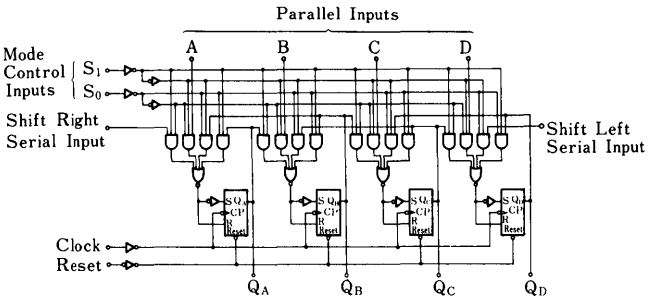


16-pin plastic DIL package

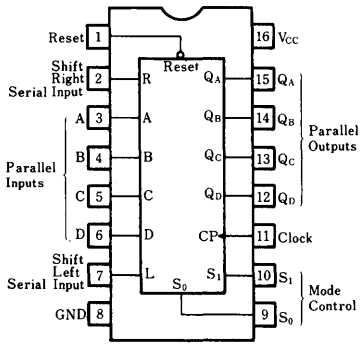
P-5

16-pin Panaflat package (SO-16D)

■ Logic diagram



Pin configuration (top view)



■ Recommended operating conditions

Parameter		Sym	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}			−400	μA
		I_{OL}			8	mA
Operating temperature range		Topr	−20	25	75	℃
Clock frequency		f_{clock}	0		25	MHz
Clock pulse width		$t_{W(CP)}$	20			ns
Reset pulse width		$t_{W(Reset)}$	20			ns
Set-up time	Mode Contorol	t_{su}	20			ns
	A, B, C, D, R, L		30			ns
	Reset (non-operating condition)		30			ns
Hold time		t_h	0			ns

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$ $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	3.5		V
	V_{OL1}	$V_{CC}=4.75V$ $V_{IH}=2V$ $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
	V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				20	μA
	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.4	mA
	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.1	mA
Output short circuit current**	I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−100	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current	I_{CC}	$V_{CC}=5.25V$			15	23	mA

* When constant at V_{CC} = 5V, Ta = 25°C.

** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

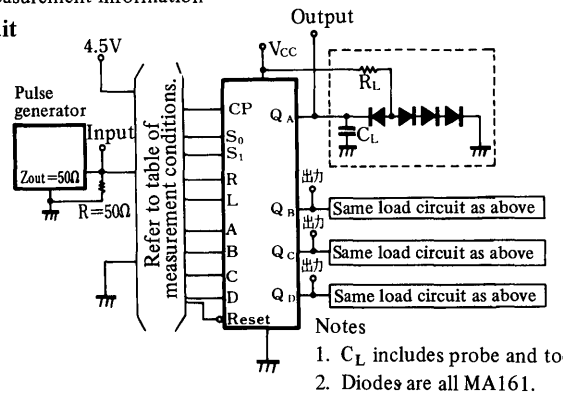
*** Measured with all outputs open, A through D inputs grounded, and 4.5 V applied to S_0, S_1, reset and serial inputs; clock input momentarily grounded, following which 4.5 V is applied to it.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Maximum clock frequency	f_{max}				25	36		MHz
Propagation delay time	t_{PHL}	Reset	Q	$C_L=15pF$ $R_L=2k\Omega$		19	30	ns
	t_{PLH}	Clock				14	22	ns
	t_{PHL}					17	26	ns

※ Switching parameter measurement information

1. Measurement circuit



Notes

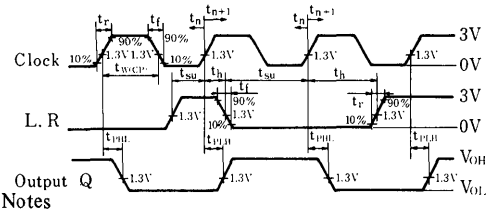
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161.

2. Table of measurement conditions

Parameter	Input Output	Inputs										Outputs			
		Reset	S_0	S_1	CP	L	R	A	B	C	D	Q_A	Q_B	Q_C	Q_D
f_{max}	Right shift	4.5V	4.5V	GND	IN	4.5V	IN	GND	GND	GND	GND	OUT	OUT	OUT	OUT
	Left shift	4.5V	GND	4.5V	IN	IN	4.5V	GND	GND	GND	GND	OUT	OUT	OUT	OUT
t_{PHL} t_{PLH}	Reset→Q	IN	4.5V	4.5V	IN	GND	GND	4.5V	4.5V	4.5V	4.5V	OUT	OUT	OUT	OUT
	Clock→Q	4.5V	4.5V	GND	IN	4.5V	IN	GND	GND	GND	GND	OUT	OUT	OUT	OUT
		4.5V	4.5V	GND	IN	IN	4.5V	GND	GND	GND	GND	OUT	OUT	OUT	OUT

3.Waveforms

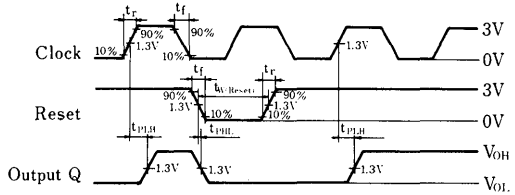
Waveforms-1 (f_{max}, CP → Q)



Notes

1. During right shifts, measurement made with:
   $Q_A = t_{n+1}$, $Q_B = t_{n+2}$, $Q_C = t_{n+3}$, $Q_D = t_{n+4}$
   During left shifts, measurement made with:
   $Q_A = t_{n+4}$, $Q_B = t_{n+3}$, $Q_C = t_{n+2}$, $Q_D = t_{n+1}$
2. Clock waveform: $t_r \leqq 15$ns, $t_f \leqq 6$ns, PRR = 1MHz, duty cycle = 50%.
3. L or R waveform: $t_r \leqq 15$ns, $t_f \leqq 6$ns.

Waveforms-2 (Reset → Q)



Notes

1. Input waveform: $t_r \leqq 15$ns, $t_f \leqq 6$ns

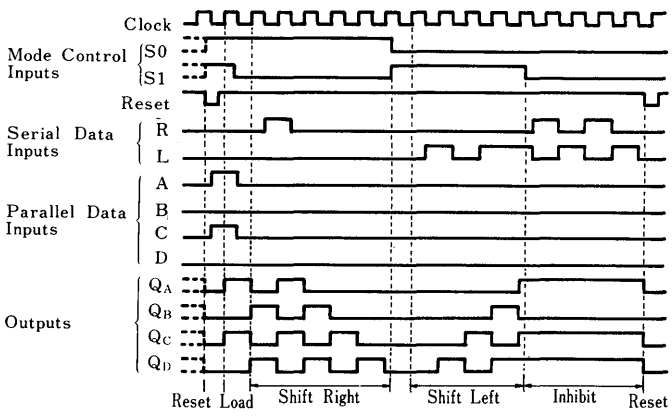
■ Truth tables

Inputs										Outputs			
Reset	Mode		Clock	Serial		Parallel				Q_A	Q_B	Q_C	Q_D
	S_1	S_0		Left	Right	A	B	C	D				
L	×	×	×	×	×	×	×	×	×	L	L	L	L
H	×	×	L	×	×	×	×	×	×	Q_{Ao}	Q_{Bo}	Q_{Co}	Q_{Do}
H	H	H	↑	×	×	a	b	c	d	a	b	c	d
H	L	H	↑	×	H	×	×	×	×	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	×	L	×	×	×	×	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	×	×	×	×	×	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	×	×	×	×	×	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	×	×	×	×	×	×	×	Q_{Ao}	Q_{Bo}	Q_{Co}	Q_{Do}

Notes

1. H: HIGH voltage level.
2. L: LOW voltage level.
3. X: Either HIGH or LOW; doesn't matter.
4. ↑: Change from LOW to HIGH.
5. a, b, c, d: Constant input level of inputs A, B, C, D.
6. Q_{Ao}, Q_{Bo}, Q_{Co}, Q_{Do}: Q_A, Q_B, Q_C, and Q_D levels prior to determination of input requirement shown in table.
7. Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn}: Q_A, Q_B, Q_C, and Q_D levels prior to nearest clock change.

■ Timing chart



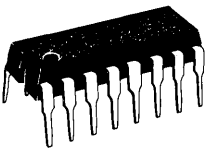
DN74LS195A

4-bit Parallel-Access Shift Registers

■Description

DN74LS195A is a 4-bit serial/parallel input to serial/parallel output shift register with direct-coupled reset inputs.

P-2



16-pin plastic DIL package

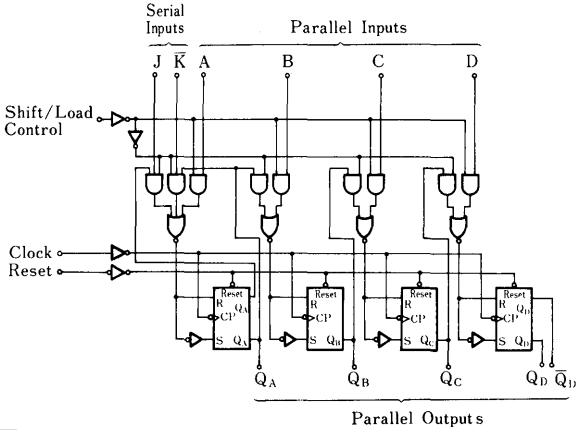
P-5

16-pin Panaflat package (SO-16D)

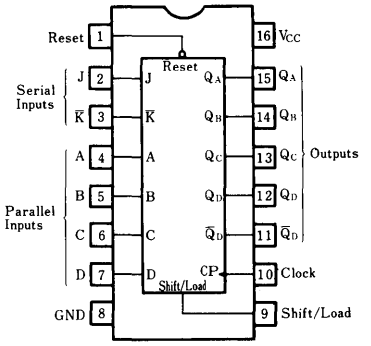
■ Features

- Synchronous serial/parallel input to serial/parallel output
- Right shift
- Left shift capability with external connection
- J and K serial inputs
- Mode-control inputs
- Direct-coupled reset inputs
- Q_D and $\overline{Q}_D$ outputs
- Wide operating temperature range (Ta = −20 to +75°C)

■ Logic diagram



Pin configuration (top view)



■ Recommended operating conditions

Parameter		Sym	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}			−400	μA
Output current		I_{OL}			8	mA
Operating temperature range		Topr	−20	25	75	℃
Clock frequency		fclock	0		30	MHz
Clock Pulse width		$t_{W(CP)}$	16			ns
Reset Pulse width		$t_{W(Reset)}$	12			ns
Set-up time	Shift / Load	tsu	25			ns
	Seiral and Parallel Data		15			ns
	Reset Inactive State		25			ns
Release time		trelease			10	ns
Hold time		th	0			

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$ $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	3.4		V
	V_{OL1}	$V_{CC}=4.75V$ $V_{IH}=2V$ $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
	V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				20	μA
	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.4	mA
	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.1	mA
Output short circuit current**	I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−100	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current***	I_{CC}	$V_{CC}=5.25V$			14	21	mA

* When constant at V_{CC} = 5V, Ta = 25°C.

** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

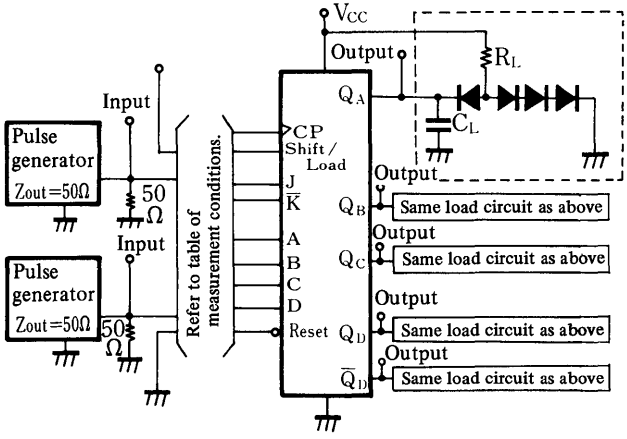
*** Measured with all outputs open, shift/load inputs grounded, 4.5V applied to J, K, and data inputs; reset inputs are momentarily grounded, following which 4.5V is applied to them; next, clock inputs are momentarily grounded and then 4.5V is applied to them.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Maximum clock frequency	f_{max}	Clock	$Q_A \sim Q_D$		30	39		MHz
Propagation delay time	t_{PHL}	Reset	$Q_A \sim Q_D$	$C_L=15pF$		19	30	ns
	t_{PLH}	Clock	$Q_A \sim Q_D$	$R_L=2k\Omega$		14	22	ns
	t_{PHL}		$\overline{Q}_D$			17	26	ns

※ Switching parameter measurement information

1. Measurement circuit



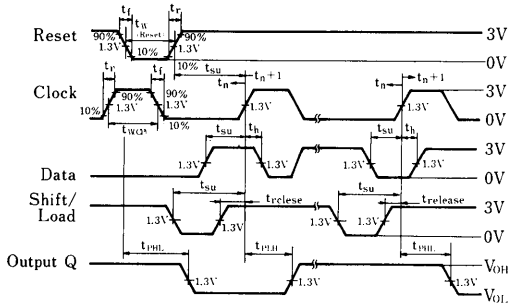
Notes

1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161.

2. Table of measurement conditions

Parameter	Input / Output	Inputs									Outputs				
		Reset	Shift/Load	J	$\overline{K}$	CP	A	B	C	D	Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
f_{max}		4.5V	4.5V	4.5V	GND	IN	4.5V	4.5V	4.5V	4.5V	OUT	OUT	OUT	OUT	OUT
t_{PHL}	Reset→ Q_A~Q_D	IN	GND	4.5V	4.5V	IN	4.5V	4.5V	4.5V	4.5V	OUT	OUT	OUT	OUT	
t_{PLH}	Clock →	4.5V	4.5V	4.5V	GND	IN	4.5V	4.5V	4.5V	4.5V	OUT	OUT	OUT	OUT	OUT
t_{PHL}	Q_A~Q_D, $\overline{Q}_D$	4.5V	GND	4.5V	4.5V	IN	IN	IN	IN	IN	OUT	OUT	OUT	OUT	OUT

3.Waveforms



Notes

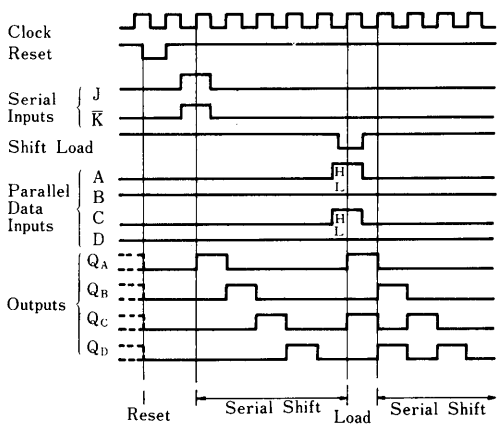
1. Input waveform: $t_r \leqq 15$ns, $t_f \leqq 6$ns, PRR = 1MHz, duty cycle = 50%.
2. The reset pulse is applied before each test.
3. t_{PHL} and t_{PLH} are measured at t_{n+1} and confirmed through a correct data shift function test at t_{n+4}.
4. Except when the shift load is HIGH, J and K inputs are measured the same as A, B, C, and D inputs.
5. t_n: Bit time before clock conversion.
   t_{n+1}: Bit time after one clock application.
   t_{n+4}: Bit time after four clock applications.

■ Truth tables

Inputs									Outputs				
Reset	Shift / Load	Clock	Serial		Parallel				Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
			J	$\overline{K}$	A	B	C	D					
L	×	×	×	×	×	×	×	×	L	L	L	L	H
H	L	↑	×	×	a	b	c	D	a	b	c	d	$\overline{d}$
H	H	L	×	×	×	×	×	×	Q_{Ao}	Q_{Bo}	Q_{Co}	Q_{Do}	$\overline{Q}_{Do}$
H	H	↑	L	H	×	×	×	×	Q_{An}	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	×	×	×	×	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	×	×	×	×	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	×	×	×	×	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

Notes
1. H: HIGH voltage level.
2. L: LOW voltage level.
3. X: Either HIGH or LOW; doesn't matter.
4. ↑: Change from LOW to HIGH.
5. a ~d: Constant input levels of inputs A through D.
6. Q_{Ao} ~ Q_{Do}: Levels of Q_A through Q_D prior to determination of input requirements shown in table.
7. Q_{An} ~ Q_{Cn}: Levels of Q_A, Q_B, and Q_C prior to nearest clock ↑ change.

■ Timing chart



DN74LS196

30MHz Settable Decade Counters / Latches

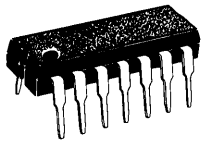
■ Description

DN74LS196 is an asynchronous decade counter with direct-coupled reset input and set input.

■ Features

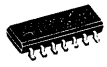
- Direct-coupled reset input and asynchronous set input
- Capability for independent use as binary and quinary counters
- High-speed counting (f_{max} = 40MHz typical)
- Wide operating temperature range (Ta = −20 to +75°C)

P-1



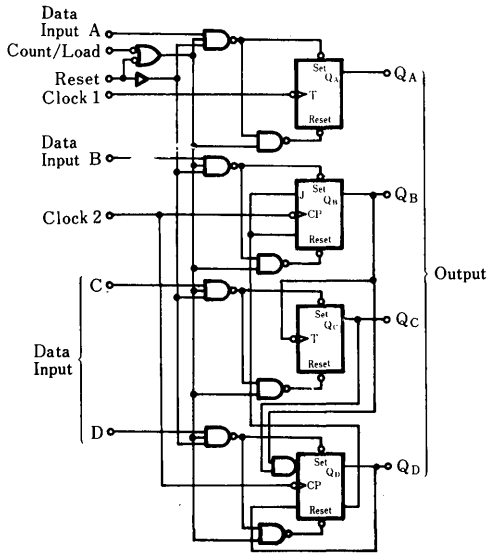
14-pin plastic DIL package

P-4

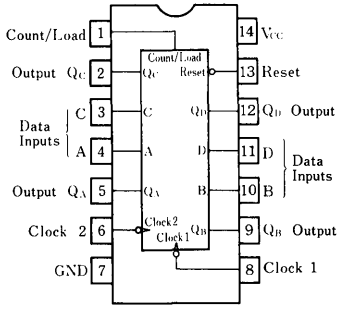


14-pin Panaflat package (SO-14D)

■ Logic diagram (1/2)



Pin configuration (top view)



■ Absolute maximum ratings

Parameter	Sym.	Rating		Unit
Input voltage	V_I	−0.5	5.5	V

* Refer to the family ratings for other parameters.

■ Recommended operating conditions

Parameter		Sym	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}			−400	μA
		I_{OL}			8	mA
Operating temperature range		Topr	−20	25	75	℃
Count frequency	Clock 1 Input	t_{count}	0		30	MHz
	Clock 2 Input		0		15	
Pulse width	Clock 1 Input	t_w	20			ns
	Clock 2 put		30			
	Reset		15			
	Load		20			
Set-up time	High Level Data	t_{su}	10			ns
	Low Level Data		15			
Hold time	High Level Data	t_h	20			ns
	Low Level Data		20			
Enable time		t_{enable}	30			ns

■ DC characteristics (Ta = −20 ~ +75℃)

Parameter		Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Output voltage**		V_{OH}	V_{CC}=4.75V, V_{IH}=2V V_{IL}=0.8V, I_{OH}=−400μA		2.7	3.4		V
		V_{OL1}	V_{CC}=4.75V V_{IH}=2V	I_{OL}=4mA		0.25	0.4	V
		V_{OL2}	V_{IL}=0.8V	I_{OL}=8mA		0.35	0.5	V
Input current	Data, Count / Load	I_{IH}	V_{CC}=5.25V V_I=2.7V				20	μA
	Reset, Clock-1						40	μA
	Clock-2						80	μA
	Data, Count / Load	I_{IL}	V_{CC}=5.25V V_I=0.4V				−0.4	mA
	Reset						−0.8	mA
	Clock-1						−2.4	mA
	Clock-2						−2.8	mA
	Data, Count / Load	I_I	V_{CC}=5.25V V_I=5.5V				0.1	mA
	Reset, Clock-1						0.2	mA
	Clock-2						0.4	mA
Output short circuit current***		L_{OS}	V_{CC}=5.25V V_o=0V		−15		−100	mA
Input clamp voltage		V_{IK}	V_{CC}=4.75V I_I=−18mA				−1.5	V
Supply current***		I_{CC}	V_{CC}=5.25V			16	27	mA

* When constant at V_{CC} = 5V, Ta = 25°C.

** When testing Q_A output, a current to which the rated upper limit value for the I_{IL} of the clock-2 input has been added is applied to the specified I_{OL}.

*** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

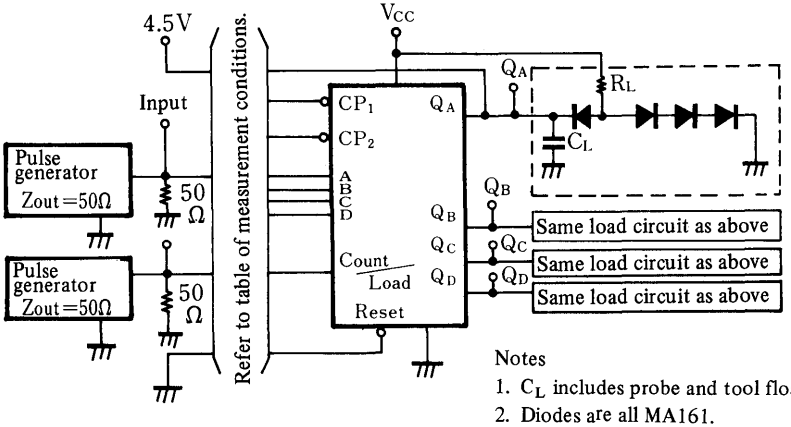
**** Measured with all outputs open and all inputs grounded.

■ Switching characteristics (V_{CC}=5V, Ta=25℃)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Maximum clock frequency	f_{max}	Clock 1	Q_A	C_L=15pF, R_L=2kΩ	30	40		MHz
Propagation delay time	t_{PLH}	Clock 1	Q_A			8	15	ns
	t_{PHL}					13	20	
	t_{PLH}	Clock 2	Q_B			16	24	ns
	t_{PHL}					22	33	
	t_{PLH}	Clock 2	Q_C			38	57	ns
	t_{PHL}					41	62	
	t_{PLH}	Clock 2	Q_D			12	18	ns
	t_{PHL}					30	45	
	t_{PLH}	A, B, C, D	Q_A, Q_B Q_C, Q_D			20	30	ns
	t_{PHL}					29	44	
	t_{PLH}	Load	Q_A~Q_D			27	41	ns
	t_{PHL}					30	45	
	t_{PHL}	Reset	Q_A~Q_D			34	41	ns

※ Switching parameter measurement information

1. Measurement circuit



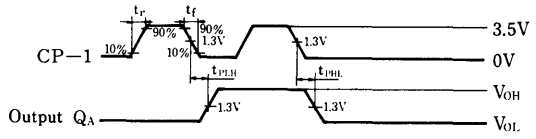
Notes
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161.

2. Table of measurement conditions

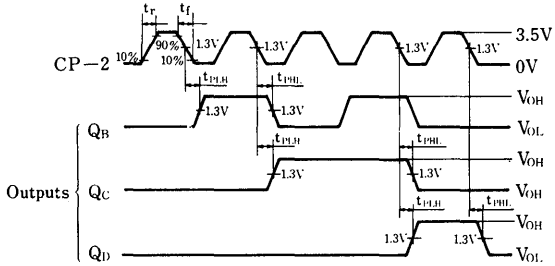
Parameter	Inputs/Outputs	Inputs								Outputs			
		Reset	Count/Load	CP-1	CP-2	Data A	Data B	Data C	Data D	Q_A	Q_B	Q_C	Q_D
f_{max}		4.5V	4.5V	IN	Linked to Q_A	GND	GND	GND	GND	OUT	OUT	OUT	OUT
t_{PLH} t_{PHL}	CP-1→Q_A	4.5V	4.5V	IN	Linked to Q_A	GND	GND	GND	GND	OUT			
	CP-2→Q_B,Q_C Q_D	4.5V	4.5V	4.5V	IN	GND	GND	GND	GND		OUT	OUT	OUT
	A, B C,D→Q_A,Q_B Q_C,Q_D	4.5V	GND	4.5V	Linked to Q_A	IN	IN	IN	IN	OUT	OUT	OUT	OUT
	Load→Q_A,Q_B Q_C,Q_D	4.5V	IN	4.5V	Linked to Q_A	4.5V or GND	4.5V or GND	4.5V or GND	4.5V or GND	OUT	OUT	OUT	OUT
	Reset→Q_A,Q_B Q_C,Q_D	IN	IN	4.5V	Linked to Q_A	4.5V	4.5V	4.5V	4.5V	OUT	OUT	OUT	OUT

3.Waveforms

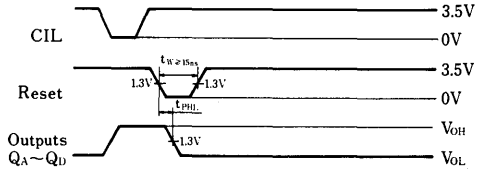
Waveforms-1 f_{max}(CP−1), t_W(CP−1), t_{PLH}, t_{PHL}(CP → Q_A)



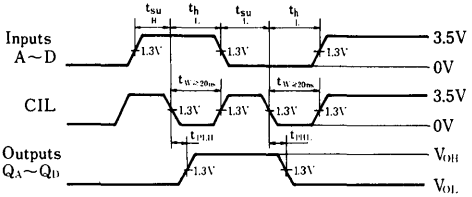
Waveforms-2 f_{max} (CP−2), t_W(CP−2), t_{PLH}, t_{PHL} (CP−2 → Q_B, Q_C, Q_D)



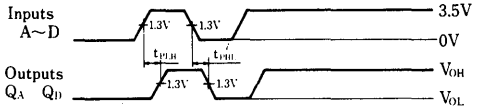
Waveforms-3 t_W(Reset), t_{PHL}(Reset → Q)



Waveforms-4 t_W(Load), t_{su}, t_h(H, L), t_{PHL}, t_{PLH}(Load → Q)



Waveforms-5 t_{PLH}, t_{PHL}(Data → Q)



Notes
1. CP-1 and CP-2 waveforms:
   $t_r \leqq 15$ns, $t_f \leqq 6$ns, PRR = 1MHz, duty cycle = 50%.
2. When measuring f_{max}, t_r and $t_f \leqq 2.5$ns.

■ Truth tables

1. decode. (BCD)

Count	Outputs			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

Notes 1. Q_A is connected to CP-2.
2. H: HIGH voltage level.
3. L: LOW voltage level.

2. Bi-quinary

Count	Outputs			
	Q_A	Q_D	Q_B	Q_C
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	H
6	H	L	L	L
7	H	L	H	H
8	H	L	H	L
9	H	H	L	H

Notes 1. Q_D is connected to CP-1.
2. H: HIGH voltage level.
3. L: LOW voltage level.

DN74LS197

30MHz Settable Binary Counters / Latches

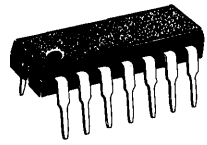
■ Description

DN74LS197 is an asynchronous hexadecimal (4-bit binary) counter with direct-coupled reset input and set input.

■ Features

- Direct-coupled reset input and asynchronous set input
- Capability for independent use as binary and octal counters
- High-speed counting (f_{max} = 40 MHz typical)
- Wide operating temperature range (Ta = −20 to +75°C)

P-1

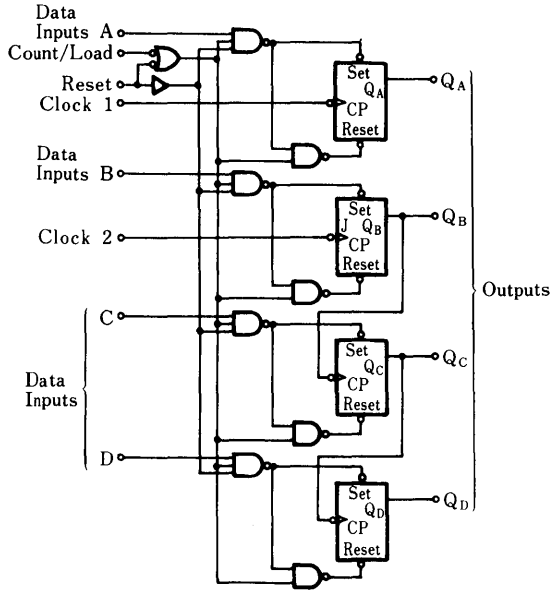


14-pin plastic DIL package

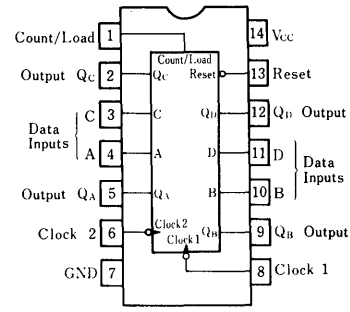
P-4

14-pin Panaflat package (SO-14D)

■ Logic diagram



Pin configuration (top view)



■ Absolute maximum ratings

Parameter	Sym.	Rating		Unit
Input voltage	V_I	−0.5	5.5	V

* Refer to the family ratings for other parameters.

■ Recommended operating conditions

Parameter		Sym	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}			−400	μA
		I_{OL}			8	mA
Operating temperature range		Topr	−20	25	75	℃
Count frequency	Clock 1 Input	t_{count}	0		30	MHz
	Clock 2 Input		0		15	
Pulse width	Clock 1 Input	t_w	20			ns
	Clock 2 put		30			
	Reset		15			
	Loacb		20			
Set-up time	High Level Data	t_{su}	10			ns
	Low Level Data		15			
Hold time	High Level Data	t_h	20			ns
	Low Level Data		20			
Enable time		t_{enable}	30			ns

■ DC characteristics (Ta = −20 ~ +75℃)

Parameter		Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Output voltage**		V_{OH}	V_{CC} = 4.75V, V_{IH} = 2V V_{IL} = 0.8V, I_{OH} = −400μA		2.7	3.4		V
		V_{OL1}	V_{CC} = 4.75V V_{IH} = 2V V_{IL} = 0.8V	I_{OL} = 4mA		0.25	0.4	V
		V_{OL2}		I_{OL} = 8mA		0.35	0.5	V
Input current	Data, Count / Load	I_{IH}	V_{CC} = 5.25V V_I = 2.7V				20	μA
	Reset, Clock-1						40	μA
	Clock-2						80	μA
	Data, Count / Load	I_{IL}	V_{CC} = 5.25V V_I = 0.4V				−0.4	mA
	Reset						−0.8	mA
	Clock-1						−2.4	mA
	Clock-2						−1.3	mA
	Data, Count / Load	I_I	V_{CC} = 5.25V V_I = 5.5V				0.1	mA
	Reset, Clock-1						0.2	mA
	Clock-2						0.4	mA
Output short circuit current***		I_{OS}	V_{CC} = 5.25V V_o = 0V		−15		−100	mA
Input clamp voltage		V_{IK}	V_{CC} = 4.75V I_I = −18mA				−1.5	V
Supply current***		I_{CC}	V_{CC} = 5.25V			16	27	mA

* When constant at V_{CC} = 5V, Ta = 25°C.

** When testing Q_A output, a current to which the rated upper limit value for the I_{IL} of the clock-2 input has been added is applied to the specified I_{OL}.

*** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

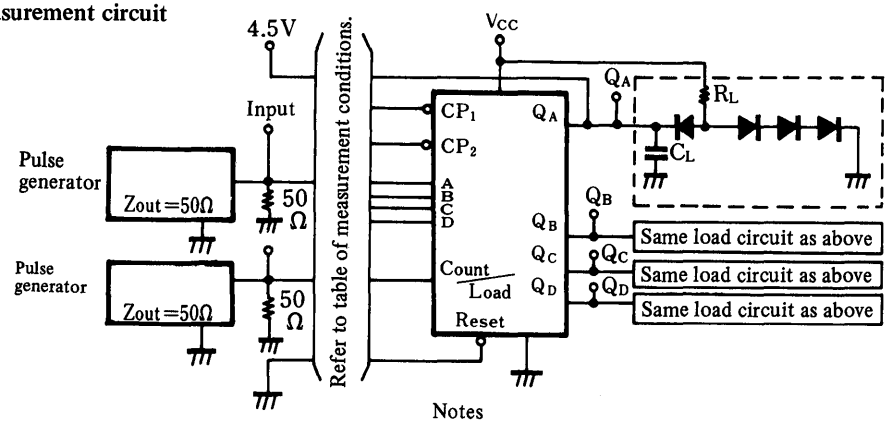
**** Measured with all outputs open and all inputs grounded.

■ Switching characteristics (V_{CC}=5V, Ta=25℃)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Maximum clock frequency	f_{max}	Clock 1	Q_A	C_L=15pF, R_L=2kΩ	30	40		MHz
Propagation delay time	t_{PLH}	Clock 1	Q_A			8	15	ns
	t_{PHL}					14	21	
	t_{PLH}	Clock 2	Q_B			12	19	ns
	t_{PHL}					23	35	
	t_{PLH}	Clock 2	Q_C			34	51	ns
	t_{PHL}					42	63	
	t_{PLH}	Clock 2	Q_D			55	78	ns
	t_{PHL}					63	95	
	t_{PLH}	A, B, C, D	Q_A, Q_B Q_C, Q_D			18	27	ns
	t_{PHL}					29	44	
	t_{PLH}	Load	Q_A~Q_D			26	39	ns
	t_{PHL}					30	45	
	t_{PHL}	Reset	Q_A~Q_D			34	51	ns

※ Switching parameter measurement information

1. Measurement circuit



Notes

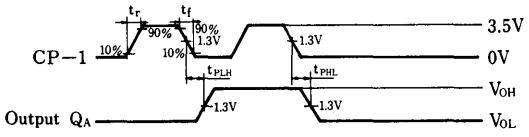
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161.

2. Table of measurement conditions

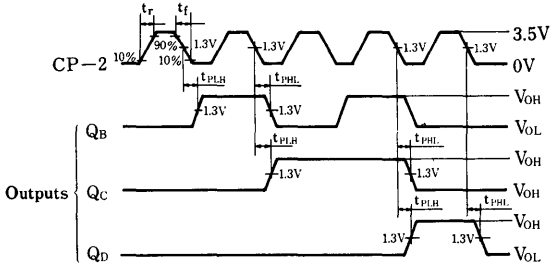
Parameter	Inputs/Outputs	Inputs								Outputs			
		Reset	Count/Load	CP-1	CP-2	Data A	Data B	Data C	Data D	Q_A	Q_B	Q_C	Q_D
f_{max}		4.5V	4.5V	IN	Linked to Q_A	GND	GND	GND	GND	OUT	OUT	OUT	OUT
t_{PLH} t_{PHL}	CP-1→Q_A	4.5V	4.5V	IN	Linked to Q_A	GND	GND	GND	GND	OUT			
	CP-2→Q_B, Q_C Q_D	4.5V	4.5V	4.5V	IN	GND	GND	GND	GND		OUT	OUT	OUT
	A, B C, D→Q_A, Q_B Q_C Q_D	4.5V	GND	4.5V	Linked to Q_A	IN	IN	IN	IN	OUT	OUT	OUT	OUT
	Load→Q_A, Q_B Q_C, Q_D	4.5V	IN	4.5V	Linked to Q_A	4.5V or GND	4.5V or GND	4.5V or GND	4.5V or GND	OUT	OUT	OUT	OUT
	Reset→Q_A, Q_B Q_C, Q_D	IN	IN	4.5V	Linked to Q_A	4.5V	4.5V	4.5V	4.5V	OUT	OUT	OUT	OUT

3.Waveforms

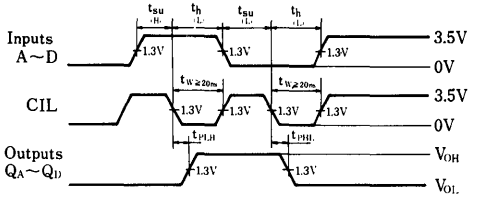
Waveforms-1 f_{max}(CP−1), t_W(CP−1), t_{PLH}, t_{PHL}(CP → Q_A)



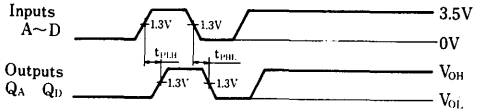
Waveforms-2 f_{max} (CP−2), t_W(CP−2), t_{PLH}, t_{PHL} (CP−2 → Q_B, Q_C, Q_D)



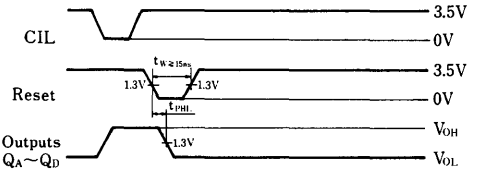
Waveforms-3 t_W(Reset), t_{PHL}(Reset → Q)



Waveforms-4 t_W(Load), t_{su}, t_h(H, L), t_{PHL}, t_{PLH}(Load → Q)



Waveforms-5 t_{PLH}, t_{PHL}(Data → Q)



Notes
1. CP-1 and CP-2 waveforms:
   $t_r \leqq 15$ns, $t_f \leqq 6$ns, PRR = 1MHz, duty cycle = 50%.
2. When measuring f_{max}, t_r and $t_f \leqq 2.5$ns.

■ Truth tables

Count	Outputs			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

Notes 1. Output Q_A is connected to clock CP-2. 2. H: HIGH voltage level. 3. L: LOW voltage level.

DN74LS240

Octal Buffers AND Line Drivers (with 3-state Outputs)

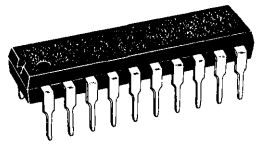
■ Description

DN74LS240 contains two buffer blocks, each with independent output-control inputs common to four circuits and 3-state inverted outputs.

■ Features

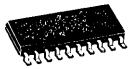
- Low input load coefficient (pnp input)
- Hysteresis (width = 400mV typical)
- Two circuit in-phase output-control inputs ($\overline{G}_1$ and $\overline{G}_2$)
- High fan-out 3-state outputs (I_{OL} = 24mA, I_{OH} = −15mA)
- Wide operating temperature range (Ta = −20 to +75°C)

P-3



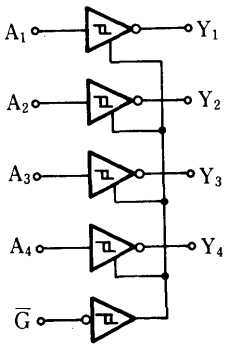
20-pin plastic DIL package

P-6

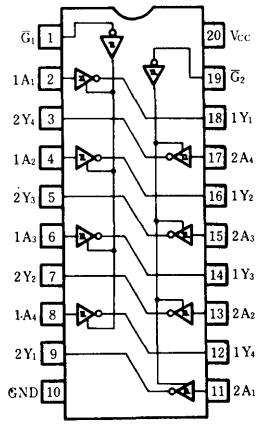


20-pin Panaflat package (SO-20D)

■ Logic diagram (1/2)



Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−15	mA
	I_{OL}			64	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter		Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Hysteresis		$V_T^+ - V_T^-$	$V_{CC} = 4.75V$		0.2	0.4		V
Output voltage		V_{OH1}	$V_{CC} = 4.75V$, $V_{IH} = 2V$ $V_{IL} = 0.5V$, $I_{OH} = -15mA$		2.0			V
		V_{OH2}	$V_{CC} = 4.75V$, $V_H = 2V$ $V_{IL} = 0.8V$, $I_{OH} = -3mA$		2.4	3.4		V
		V_{OL1}	$V_{CC} = 4.75V$ $V_{IH} = 2V$ $V_{IL} = 0.8V$	$I_{OL} = 12mA$		0.25	0.4	V
		V_{OL2}		$I_{OL} = 24mA$		0.35	0.5	V
Output current		I_{OZH}	$V_{CC} = 4.75V$ $V_{IH} = 2V$ $V_{IL} = 0.8V$	$V_O = 2.7V$			20	μA
		I_{OZL}		$V_O = 0.4V$			−20	μA
Input current		I_H	$V_{CC} = 5.25V$, $V_I = 2.7V$				20	μA
		I_L	$V_{CC} = 5.25V$, $V_I = 0.4V$				−0.2	mA
		I_I	$V_{CC} = 5.25V$, $V_I = 7V$				0.1	mA
Output short circuit current**		I_{OS}	$V_{CC} = 5.25V$, $V_I = 0V$		−15		−130	mA
Input clamp voltage		V_{IK}	$V_{CC} = 4.75V$, $I_{IN} = -18mA$				−1.5	V
Supply current ***	All outputs HIGH	I_{CC}	$V_{CC} = 5.25V$			13	23	mA
	All outputs LOW					26	46	mA
	Disable output					29	54	mA

* When constant at V_{CC} = 5V, Ta = 25°C.

** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

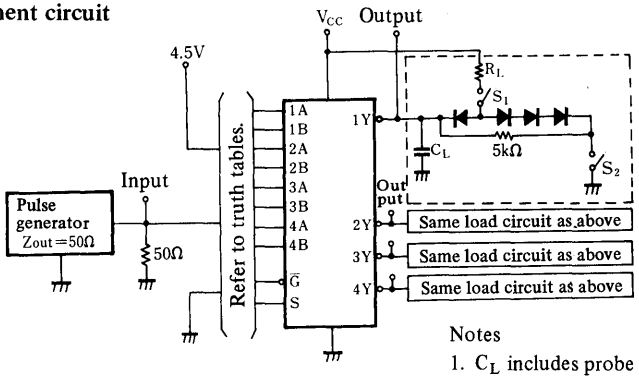
*** I_{CC} is measured with all outputs open.

■ Switching characteristics ($V_{CC} = 5V$, $Ta = 25℃$)

Parameter	Sym	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	$C_L = 45pF$ $R_L = 667\Omega$		9	14	ns
	t_{PHL}			12	18	ns
Output enable time	t_{ZL}			20	30	ns
	t_{ZH}			15	23	ns
Output disable time	t_{LZ}	$C_L = 5pF$ $R_L = 667\Omega$		15	25	ns
	t_{HZ}			10	18	ns

※ Switching parameter measurement information

1. Measurement circuit

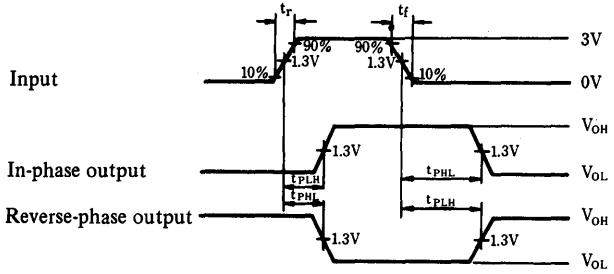


Notes

1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161 or equivalent.

2. Waveforms

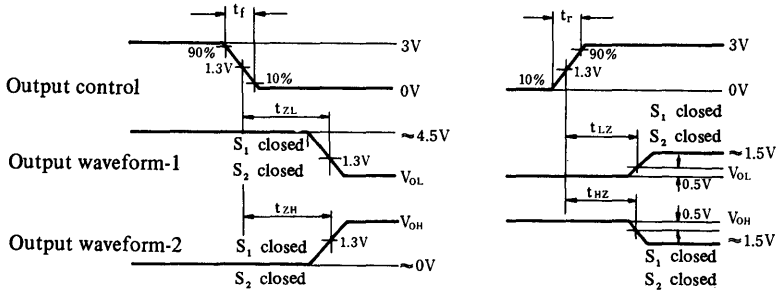
Waveforms-1



Notes

1. Input waveform: $t_r \leqq 15$ns, $t_f \leqq 6$ns, PRR = 1MHz, duty cycle = 50%.

Waveforms-2



Notes

1. Input waveform: $t_r \leqq 15$ns, $t_f \leqq 6$ns, PRR = 1MHz, duty cycle = 50%.
2. Except when the output is disabled by the output control, output waveform-1 occurs as a result of internal conditions such as a LOW voltage level.
3. Except when the output is disabled by the output control, output waveform-2 occurs as a result of internal conditions such as a HIGH voltage level.
4. When measuring t_{PLH} and t_{PHL}, S_1 and S_2 are closed.

■ Truth tables

Inputs		Outputs
$\overline{G}$	A	Y
H	×	Z
L	H	L
L	L	H

Notes

1. H: HIGH voltage level.
2. L: LOW voltage level.
3. X: Either HIGH or LOW; doesn't matter.
4. Z: High impedance.

DN74LS241

Octal Buffers AND Line Drivers (with 3-state Outputs)

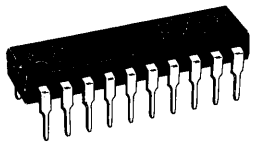
■ Description

DN74LS241 contains two buffer blocks, each with independent output-control inputs common to four circuits and 3-state non-inverted outputs.

■ Features

- Low input load coefficient (pnp input)
- Hysteresis (width = 400mV typical)
- Complementary output-control inputs ($\overline{G}_1$, and $\overline{G}_2$)
- High fan-out 3-state outputs (I_{OL} = 24mA, I_{OH} = −15mA)
- Wide operating temperature range (Ta = −20 to +75°C)

P-3

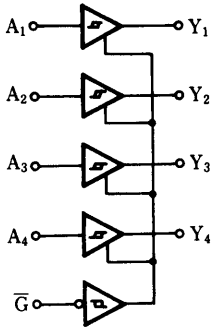


20-pin plastic DIL package

P-6

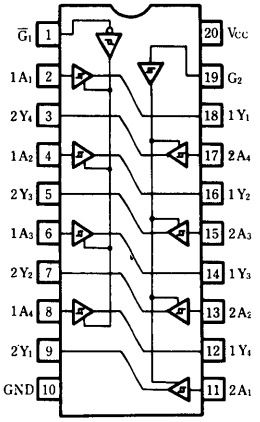
20-pin Panaflat package (SO-20D)

■ Logic diagram (1/2)



Note

Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−15	mA
	I_{OL}			64	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter		Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Hysteresis		$V_T^+ - V_T^-$	$V_{CC} = 4.75V$		0.2	0.4		V
Output voltage		V_{OH1}	$V_{CC} = 4.75V$, $V_{IH} = 2V$, $V_{IL} = 0.5V$, $I_{OH} = -15mA$		2.0			V
		V_{OH2}	$V_{CC} = 4.75V$, $V_H = 2V$, $V_{IL} = 0.8V$, $I_{OH} = -3mA$		2.4	3.4		V
		V_{OL1}	$V_{CC} = 4.75V$, $V_{IH} = 2V$, $V_{IL} = 0.8V$	$I_{OL} = 12mA$		0.25	0.4	V
		V_{OL2}		$I_{OL} = 24mA$		0.35	0.5	V
Output current		I_{OZH}	$V_{CC} = 4.75V$, $V_{IH} = 2V$, $V_{IL} = 0.8V$	$V_O = 2.7V$			20	μA
		I_{OZL}		$V_O = 0.4V$			−20	μA
Input current		I_H	$V_{CC} = 5.25V$, $V_I = 2.7V$				20	μA
		I_L	$V_{CC} = 5.25V$, $V_I = 0.4V$				−0.2	mA
		I_I	$V_{CC} = 5.25V$, $V_I = 7V$				0.1	mA
Output short circuit current**		I_{OS}	$V_{CC} = 5.25V$, $V_I = 0V$		−15		−130	mA
Input clamp voltage		V_{IK}	$V_{CC} = 4.75V$, $I_I = -18mA$				−1.5	V
Supply current ***	All outputs HIGH	I_{CC}	$V_{CC} = 5.25V$			17	27	mA
	All outputs LOW					27	46	mA
	Disable output					32	54	mA

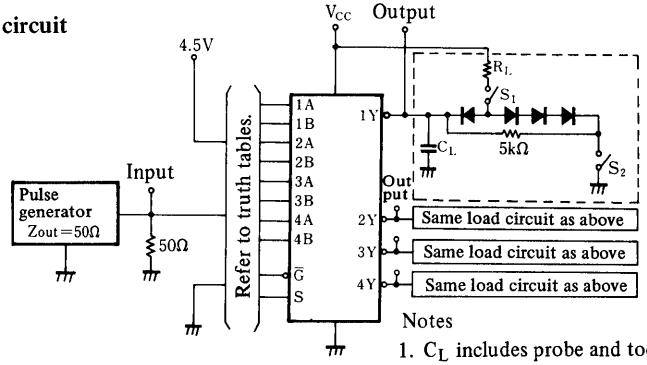
* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.
*** I_{CC} is measured with all outputs open.

■ Switching characteristics (V_{CC}= 5V, Ta = 25℃)

Parameter	Sym	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	$C_L = 45pF$, $R_L = 667\Omega$		12	14	ns
	t_{PHL}			12	18	ns
Output enable time	t_{ZL}			20	30	ns
	t_{ZH}			15	23	ns
Output disable time	t_{LZ}	$C_L = 5pF$, $R_L = 667\Omega$		15	25	ns
	t_{HZ}			10	18	ns

※ Switching parameter measurement information

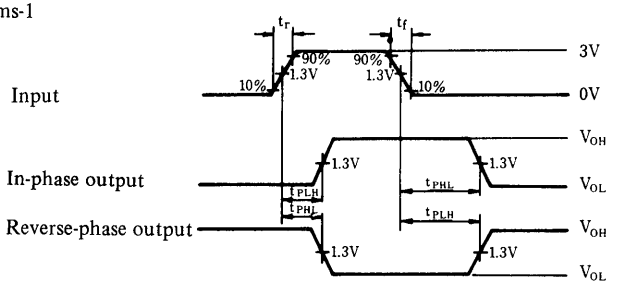
1. Measurement circuit



Notes
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161 or equivalent.

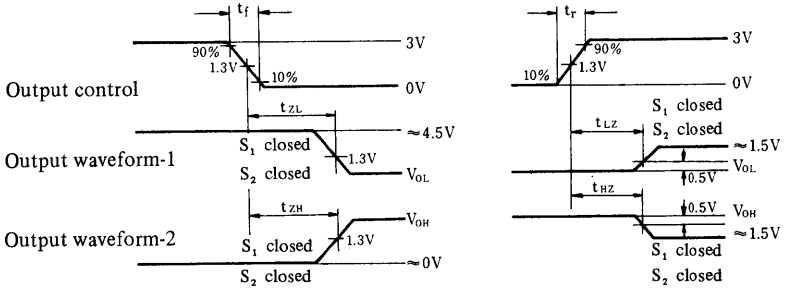
2. Waveforms

Waveforms-1



Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.

Waveforms-2



Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.
2. Except when the output is disabled by the output control, output waveform-1 occurs as a result of internal conditions such as a LOW voltage level.
3. Except when the output is disabled by the output control, output waveform-2 occurs as a result of internal conditions such as a HIGH voltage level.
4. When measuring t_{PLH} and t_{PHL}, S_1 and S_2 are closed.

■ Truth tables

Inputs			Outputs
$\overline{G}_1$	G_2	A	Y
H	L	×	Z
L	H	H	H
L	H	L	L

Notes
1. H: HIGH voltage level.
2. L: LOW voltage level.
3. X: Either HIGH or LOW; doesn't matter.
4. Z: High impedance.

DN74LS244

Octal Buffers AND Line Drivers (with 3-state Outputs)

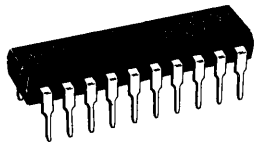
■ Description

DN74LS244 contains two buffer blocks, each with independent output-control inputs common to four circuits and 3-stage non-inverted outputs.

■ Features

- Low input load coefficient (pnp input)
- Hysteresis (width = 400mV typical)
- Two-circuit in-phase output-control inputs ($\overline{G_1}$ and $\overline{G_2}$)
- High fan-out 3-state outputs (I_{OH} = 24mA, I_{OH} = −15mA)
- Wide operating temperature range (Ta = −20 to +75°C)

P-3

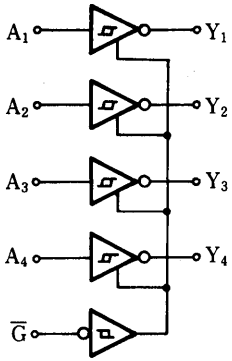


20-pin plastic DIL package

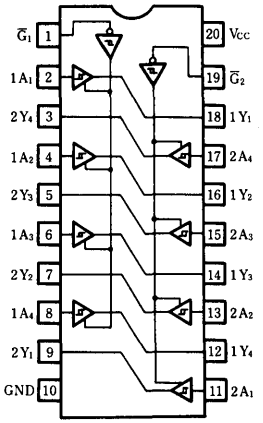
P-6

20-pin Panaflat package (SO-20D)

■ Logic diagram (1/2)



Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−15	mA
	I_{OL}			64	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter		Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Hysteresis		$V_T^+ - V_T^-$	$V_{CC} = 4.75V$		0.2	0.4		V
Output voltage		V_{OH1}	$V_{CC} = 4.75V$, $V_{IH} = 2V$, $V_{IL} = 0.5V$, $I_{OH} = -15mA$		2.0			V
		V_{OH2}	$V_{CC} = 4.75V$, $V_H = 2V$, $V_{IL} = 0.8V$, $I_{OH} = -3mA$		2.4	3.4		V
		V_{OL1}	$V_{CC} = 4.75V$, $V_{IH} = 2V$, $V_{IL} = 0.8V$	$I_{OL} = 12mA$		0.25	0.4	V
		V_{OL2}		$I_{OL} = 24mA$		0.35	0.5	V
Output current		I_{OZH}	$V_{CC} = 4.75V$, $V_{IH} = 2V$, $V_{IL} = 0.8V$	$V_O = 2.7V$			20	μA
		I_{OZL}		$V_O = 0.4V$			−20	μA
Input current		I_H	$V_{CC} = 5.25V$, $V_I = 2.7V$				20	μA
		I_L	$V_{CC} = 5.25V$, $V_I = 0.4V$				−0.2	mA
		I_I	$V_{CC} = 5.25V$, $V_I = 7V$				0.1	mA
Output short circuit current**		I_{OS}	$V_{CC} = 5.25V$, $V_I = 0V$		−15		−130	mA
Input clamp voltage		V_{IK}	$V_{CC} = 4.75V$, $I_I = -18mA$				−1.5	V
Supply current ***	All outputs HIGH	I_{CC}	$V_{CC} = 5.25V$			17	27	mA
	All outputs LOW					27	46	mA
	Disable output					32	54	mA

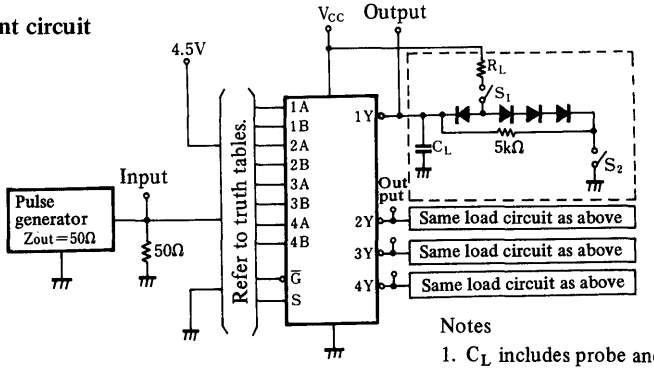
* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.
*** I_{CC} is measured with all outputs open.

■ Switching characteristics ($V_{CC} = 5V$, $Ta = 25℃$)

Parameter	Sym	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	$C_L = 45pF$, $R_L = 667\Omega$		12	18	ns
	t_{PHL}			12	18	ns
Output enable time	t_{ZL}			20	30	ns
	t_{ZH}			15	23	ns
Output disable time	t_{LZ}	$C_L = 5pF$, $R_L = 667\Omega$		15	25	ns
	t_{HZ}			10	18	ns

※ Switching parameter measurement information

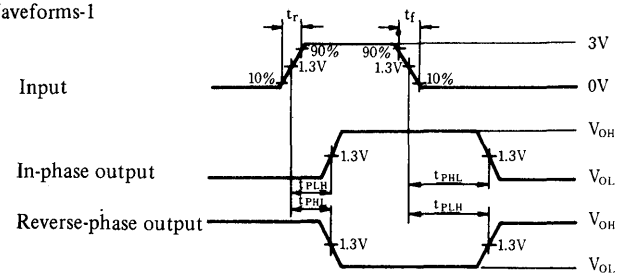
1. Measurement circuit



Notes
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161 or equivalent.

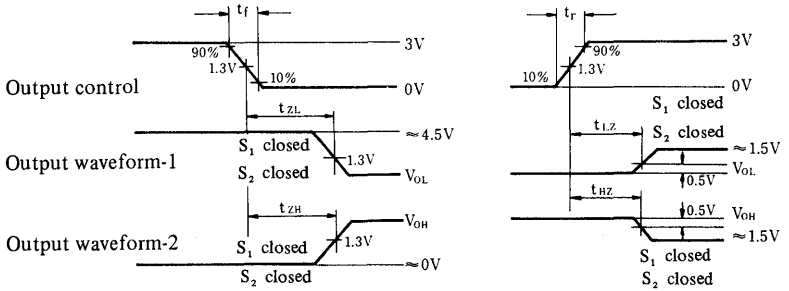
2. Waveforms

Waveforms-1



Notes
1. Input waveform: $t_r \leqq 15$ns, $t_f \leqq 6$ns, PRR = 1MHz, duty cycle = 50%.

Waveforms-2



Notes
1. Input waveform: $t_r \leqq 15$ns, $t_f \leqq 6$ns, PRR = 1MHz, duty cycle = 50%.
2. Except when the output is disabled by the output control, output waveform-1 occurs as a result of internal conditions such as a LOW voltage level.
3. Except when the output is disabled by the output control, output waveform-2 occurs as a result of internal conditions such as a HIGH voltage level.
4. When measuring t_{PLH} and t_{PHL}, S_1 and S_2 are closed.

■ Truth tables

Inputs		Outputs
$\overline{G}$	A	Y
H	×	Z
L	H	H
L	L	L

Notes
1. H: HIGH voltage level.
2. L: LOW voltage level.
3. X: Either HIGH or LOW; doesn't matter.
4. Z: High impedance.

DN74LS245

Octal Bus Transceivers (with 3-state Outputs)

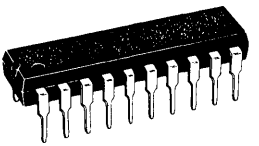
■ Description

DN74LS245 contains eight bus transmitter/reciver circuits with non-inverted outputs.

■ Features

- Bidirectional transfer or separation capability for two 8-bit data
- Low input load coefficient (pnp input)
- Hysteresis for input/output A and output/input B (width = 400mV typical)
- High fan-out (I_{OL} = 24mA, I_{OH} = −15mA)
- Wide operating temperature range (Ta = −20 to +75°C)

P-3

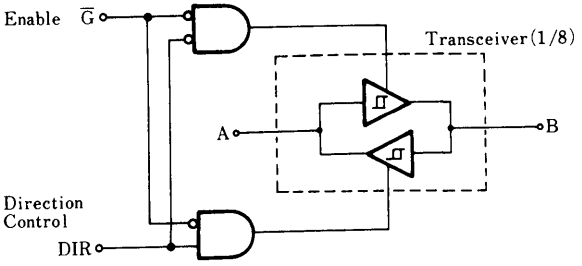


20-pin plastic DIL package

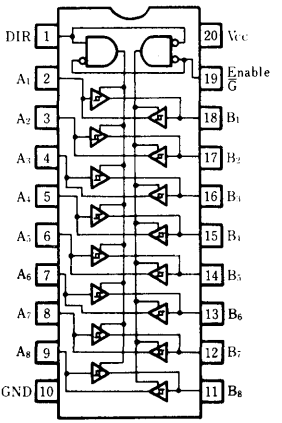
P-6

20-pin Panaflat package (SO-20D)

■ Logic diagram (1/2)



Pin configuration (top view)



■ Absolute maximum ratings

Parameter		Sym.	Rating		Unit
Input voltage	DIR, $\overline{G}$	V_I	−0.5	7.0	V
	A, B		−0.5	5.5	

* Refer to the family ratings for other parameters.

■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−15	mA
	I_{OL}			24	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input threshold voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OH1}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$	$I_{OH}=-3mA$	2.4	3.4		V
	V_{OH2}		$I_{OH}=-15mA$	2.0			V
	V_{OL1}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$	$I_{OL}=12mA$			0.4	V
	V_{OL2}		$I_{OL}=24mA$			0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$, $V_{IH}=2.7V$				20	μA
	I_{IL}	$V_{CC}=5.25V$, $V_{IH}=0.4V$				−0.2	mA
A or B	I_{I1}	$V_{CC}=5.25V$	$V_I=5.5V$			0.1	mA
DIR or $\overline{G}$	I_{I2}		$V_I=7V$			0.1	mA
Output current	I_{OZH}	$V_{CC}=5.25V$, $\overline{G}=2V$	$V_O=2.7V$			20	μA
	I_{OZL}		$V_O=0.4V$			−200	μA
Hysteresis	$V_T^+-V_T^-$	$V_{CC}=4.75V$		0.2	0.4		V
Output short circuit current**	I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−130	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$, $I_I=-18mA$				−1.5	V
Supply current	I_{CCH}	$V_{CC}=5.25V$, 出力開放			48	70	mA
	I_{CCL}	$V_{CC}=5.25V$, 出力開放			62	90	mA
	I_{CCZ}	$V_{CC}=5.25V$, 出力開放			64	95	mA

* When constant at V_{CC} = 5V, Ta = 25°C.

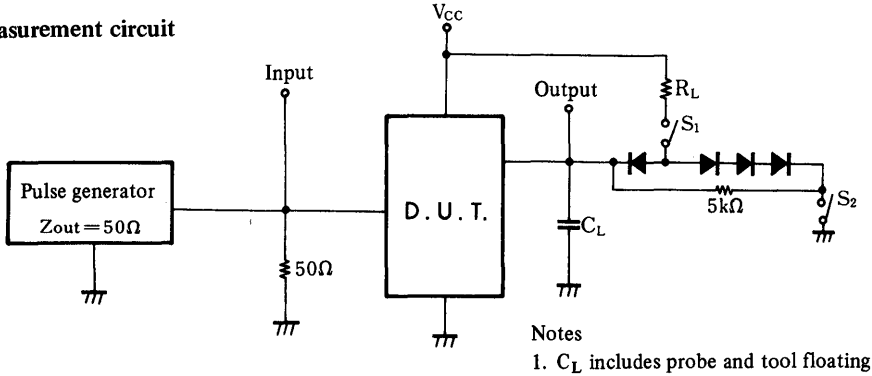
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	$C_L=45pF$, $R_L=667Ω$		8	12	ns
	t_{PHL}			8	12	ns
Output enable time	t_{ZH}			25	40	ns
	t_{ZL}			27	40	ns
Output disable time	t_{HZ}	$C_L=5pF$, $R_L=667Ω$		15	25	ns
	t_{LZ}			15	25	ns

※ Switching parameter measurement information

1. Measurement circuit

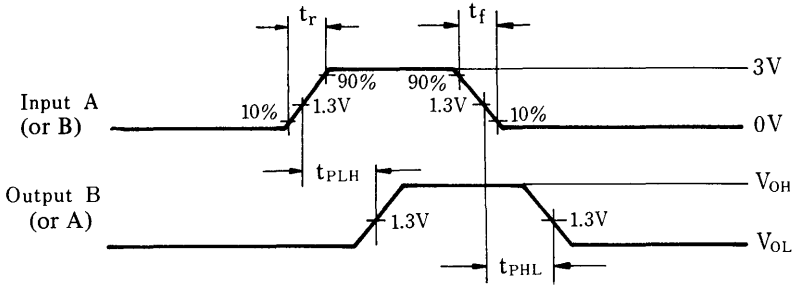


Notes

1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161 or equivalent.

2. Waveforms

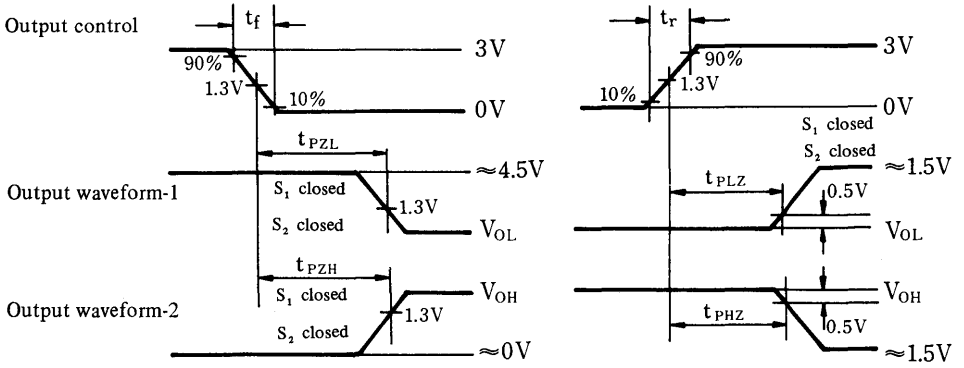
Waveforms-1



Notes

1. Input waveform ; $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR=1MHz, duty cycle 50%

Waveforms-2



Notes

1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.
2. Except when the output is disabled by the output control, output waveform-1 occurs as a result of internal conditions such as a LOW voltage level.
3. Except when the output is disabled by the output control, output waveform-2 occurs as a result of internal conditions such as a HIGH voltage level.
4. When measuring t_{PLH} and t_{PHL}, S_1 and S_2 are closed.

■ Truth tables

Enable $\overline{G}$	Direction Control DIR	Operation
L	L	B data to A bus
L	H	A data to A bus
H	×	Isolation

Notes

1. H: HIGH voltage level.
2. L: LOW voltage level.
3. X: Either HIGH or LOW; doesn't matter.

DN74LS251

8-line to 1-line Data Selectors / Multiplexers (with 3-state Outputs)

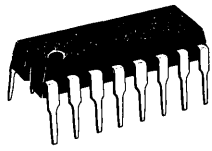
■ Description

DN74LS251 is an 8-line to 1-line data selector/multiplexer with 3-state outputs.

■ Features

- 3-state outputs
- Complementary outputs
- Wide operating temperature range (Ta = –20 to +75°C)

P-2

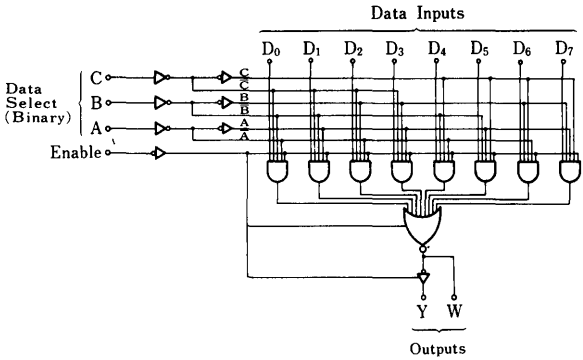


16-pin plastic DIL package

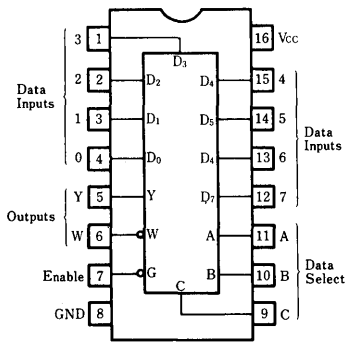
P-5

16-pin Panaflat package (SO-16D)

■ Logic diagram (1/2)



Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−2.6	mA
	I_{OL}			24	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$ $V_{IL}=0.8V$, $I_{OH}=-2.6mA$		2.7	3.1		V
	V_{OL1}	$V_{CC}=4.75V$ $V_{IH}=2V$ $V_{IL}=0.8V$	$I_{OL}=12mA$		0.25	0.4	V
	V_{OL2}		$I_{OL}=24mA$		0.35	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
	I_I	$V_{CC}=5.25V$, $V_I=7V$				0.1	mA
Output current	I_{OZ1}	$V_{CC}=5.25V$ $V_{IH}=2V$	$V_O=2.7V$			20	μA
	I_{OZ2}		$V_O=0.4V$			−20	μA
Output short circuit current**	I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−130	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$, $I_I=-18mA$				−1.5	V
Supply current***	I_{CC}	$V_{CC}=5.25V$	Measurement condition A		7	12	mA
			Measurement condition B		8.5	15	mA

* When constant at V_{CC} = 5V, Ta = 25°C.

** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

*** I_{CC} is measured with all outputs open, 4.5V applied to all data and select inputs, and the following conditions:

A: enable grounded.

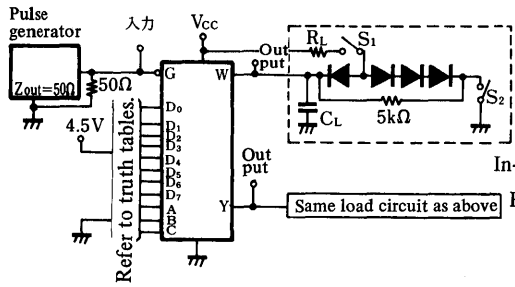
B: 4.5V applied.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	A, B, C (4 levels)	Y	$C_L=15pF$ $R_L=2k\Omega$		29	45	ns
	t_{PHL}					28	45	ns
	t_{PLH}	A, B, C (3 levels)	W			20	33	ns
	t_{PHL}					21	33	ns
	t_{PLH}	Data	Y			17	28	ns
	t_{PHL}					18	28	ns
	t_{PLH}	Data	W			10	15	ns
	t_{PHL}					9	15	ns
Output enable time	t_{PZH}	Enable	Y			30	45	ns
	t_{PZL}					26	40	ns
	t_{PZH}	Enable	W			17	27	ns
	t_{PZL}					24	40	ns
Output disable time	t_{PHz}	Enable	Y	$C_L=5pF$ $R_L=2k\Omega$		30	45	ns
	t_{PLZ}					15	25	ns
	t_{PHZ}	Enable	W			37	55	ns
	t_{PLZ}					15	25	ns

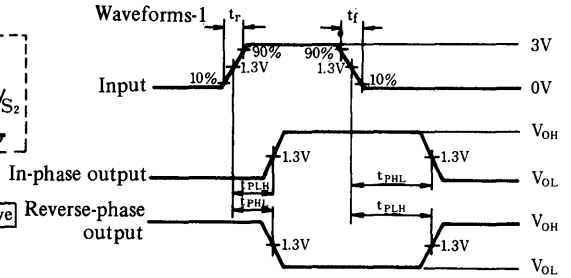
※ Switching parameter measurement information

1. Measurement circuit



1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161.

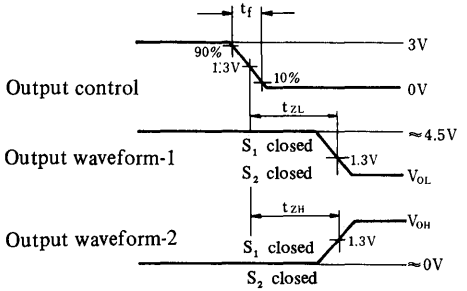
2. Waveforms



Notes

1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.

Waveforms-2



Notes

1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.
2. Except when the output is disabled by the output control, output waveform-1 occurs as a result of internal conditions such as a LOW voltage level.
3. Except when the output is disabled by the output control, output waveform-2 occurs as a result of internal conditions such as a HIGH voltage level.
4. When measuring t_{PLH} and t_{PHL}, S_1 and S_2 are closed.

■ Truth tables

Inputs				Outputs	
Select			Enable	Y	W
C	B	A	S		
×	×	×	H	Z	Z
L	L	L	L	D_0	$\overline{D_0}$
L	L	H	L	D_1	$\overline{D_1}$
L	H	L	L	D_2	$\overline{D_2}$
L	H	H	L	D_3	$\overline{D_3}$
H	L	L	L	D_4	$\overline{D_4}$
H	L	H	L	D_5	$\overline{D_5}$
H	H	L	L	D_6	$\overline{D_6}$
H	H	H	L	D_7	$\overline{D_7}$

Notes

1. H: HIGH voltage level.
2. L: LOW voltage level.
3. X: Either HIGH or LOW; doesn't matter.
4. Z: High impedance (OFF).
5. $D_0 \sim D_7$: Levels of related D inputs.

DN74LS253

Dual 4-line to 1-line Data Selectors/Multiplexers (with 3-state Outputs)

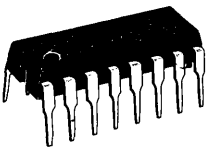
■ Description

DN74LS253 contains two 4-line to 1-line data selector/multiplexer circuits with 3-state outputs.

■ Features

- Independent output-control inputs for each circuit
- Common selector inputs for both circuits
- 3-state outputs
- Wide operating temperature range (Ta = −20 to +75°C)

P-2

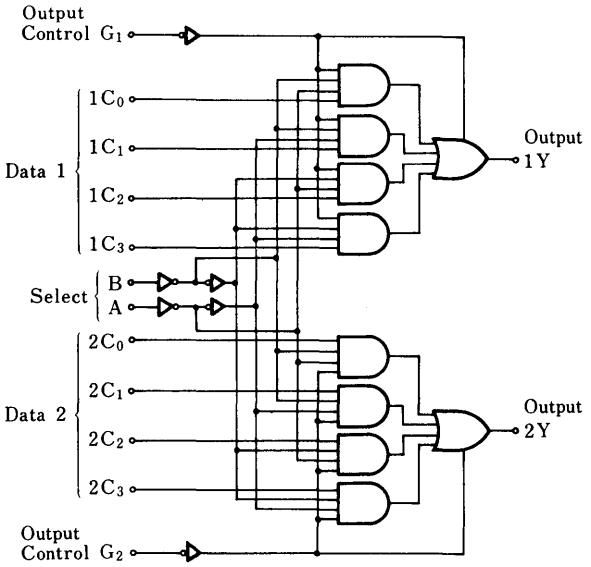


16-pin plastic DIL package

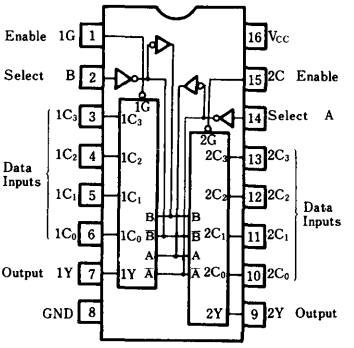
P-5

16-pin Panaflat package (SO-16D)

■ Logic diagram



Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−2.6	mA
	I_{OL}			8	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-2.6mA$		2.4	3.1		V
	V_{OL1}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
	V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
	I_I	$V_{CC}=5.25V$, $V_I=7V$				0.1	mA
Output current	I_{OZ1}	$V_{CC}=5.25V$, $V_{IH}=2V$	$V_O=2.7V$			20	μA
	I_{OZ2}		$V_O=0.4V$			−20	μA
Output short circuit current**	I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−130	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$, $I_I=-18mA$				−1.5	V
Supply current	I_{CC}	$V_{CC}=5.25V$	Measurement condition A		7	12	mA
			Measurement condition B		8.5	14	mA

* When constant at V_{CC} = 5V, Ta = 25°C.

** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

*** I_{CC} is measured with all outputs grounded and the following conditions:

A: all inputs grounded.

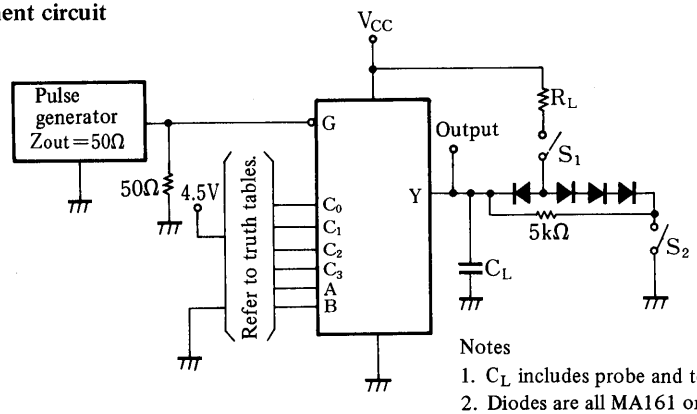
B: 4.5V applied to output control and all inputs grounded.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	Data	Y	$C_L=15pF$, $R_L=2k\Omega$		17	25	ns
	t_{PHL}					13	20	ns
	t_{PLH}	Select	Y			30	45	ns
	t_{PHL}					21	32	ns
Output enable time	t_{ZH}	Output Control	Y			15	28	ns
	t_{ZL}					15	23	ns
Output disable time	t_{HZ}	Output Control	Y	$C_L=5pF$, $R_L=2k\Omega$		27	41	ns
	t_{LZ}					18	27	ns

※ Switching parameter measurement information

1. Measurement circuit

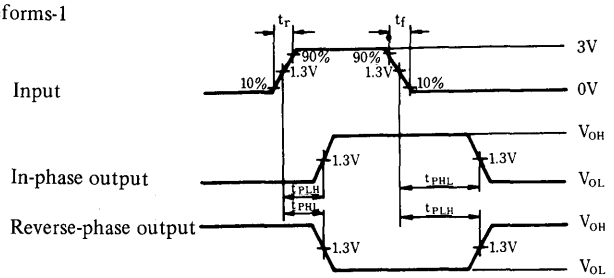


Notes

1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161 or equivalent.

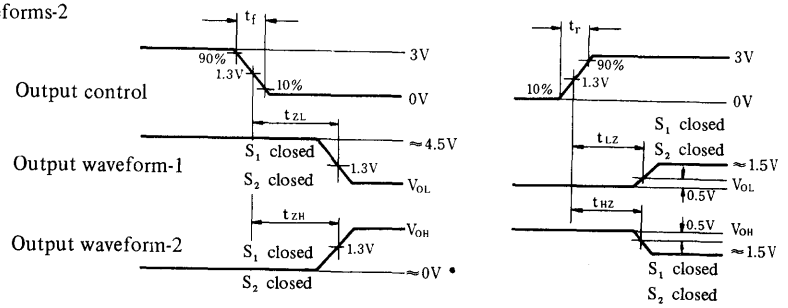
2. Waveforms

Waveforms-1



Notes
1. Input waveform: $t_r \leqq 15$ns, $t_f \leqq 6$ns, PRR = 1MHz, duty cycle = 50%.

Waveforms-2



Notes
1. Input waveform: $t_r \leqq 15$ns, $t_f \leqq 6$ns, PRR = 1MHz, duty cycle = 50%.
2. Except when the output is disabled by the output control, output waveform-1 occurs as a result of internal conditions such as a LOW voltage level.
3. Except when the output is disabled by the output control, output waveform-2 occurs as a result of internal conditions such as a HIGH voltage level.
4. When measuring t_{PLH} and t_{PHL}, S_1 and S_2 are closed.

■ Truth tables

Select inputs		Data inputs				Output control	Outputs
B	A	C_0	C_1	C_2	C_3	G	Y
×	×	×	×	×	×	H	Z
L	L	L	×	×	×	L	L
L	L	H	×	×	×	L	H
L	H	×	L	×	×	L	L
L	H	×	H	×	×	L	H
H	L	×	×	L	×	L	L
H	L	×	×	H	×	L	H
H	H	×	×	×	L	L	L
H	H	×	×	×	H	L	H

Notes
1. H: HIGH voltage level.
2. L: LOW voltage level.
3. X: Either HIGH or LOW; doesn't matter.
4. Address inputs A and B are the same for both.

DN74LS257A

Quad 2-line to 1-line Data Selectors / Multiplexers (with 3-state Outputs)

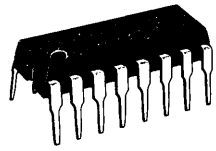
■ Description

DN74LS257A contains four 2-line to 1-line data selector/multiplexer circuits with 3-state outputs.

■ Features

- Common output-control input for all four circuits
- Common select input for all four circuits
- 3-state outputs
- Wide operating temperature range (Ta = −20 to +75°C)

P-2

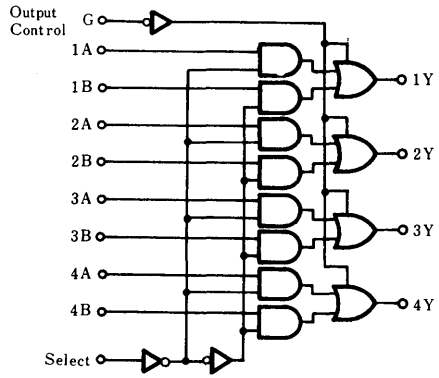


16-pin plastic DIL package

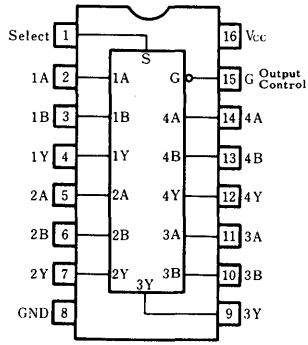
P-5

16-pin Panaflat package (SO-16D)

■ Logic diagram



Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−2.6	mA
	I_{OL}			24	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter		Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Output voltage		V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$ $V_{IL}=0.8V$, $I_{OH}=-2.6mA$		2.4	3.1		V
		V_{OL1}	$V_{CC}=4.75V$ $V_{IH}=2V$ $V_{IL}=0.8V$	$I_{OL}=12mA$		0.25	0.4	V
		V_{OL2}		$I_{OL}=24mA$		0.35	0.5	V
Input current	S	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				40	μA
	Inputs other than S						20	μA
	S	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.8	mA
	Inputs other than S						−0.4	mA
	S	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.2	mA
	Inputs other than S						0.1	mA
Output current**		I_{OZH}	$V_{CC}=5.25V$ $V_{IH}=2V$	$V_O=2.4V$			20	μA
		I_{OZL}		$V_O=0.4V$			−20	μA
Output short circuit current***		I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−130	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$, $I_I=-18mA$				−1.5	V
**** Supply current	All outputs HIGH	I_{CC}	$V_{CC}=5.25V$			6.2	10	mA
	All outputs LOW					10	16	mA
	All outputs OFF					12	19	mA

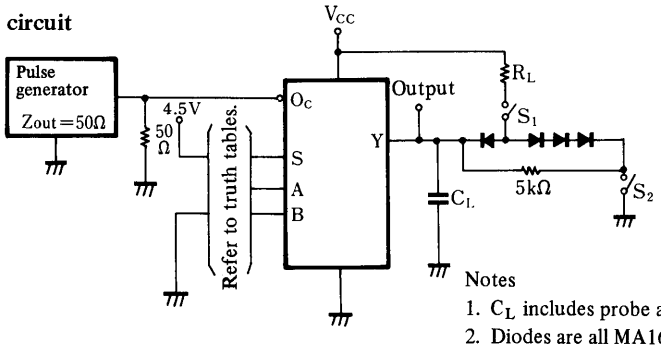
* When constant at V_{CC} = 5V, Ta = 25°C.
** OFF condition (high impedance condition).
*** Only one output at a time short circuited to GND. Also, short circuit time to GND within 7 seconds.
**** Measured with all outputs open and all possible inputs grounded in the range that fulfills the desired output condition.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	A, B	Y	$C_L=45pF$ $R_L=667Ω$		12	18	ns
	t_{PHL}					12	18	ns
	t_{PLH}	S	Y			14	21	ns
	t_{PHL}					14	21	ns
Output enable time	t_{ZH}	G	Y			20	30	ns
	t_{HZ}					20	30	ns
Output disable time	t_{HZ}	G	Y	$C_L=5pF$ $R_L=667Ω$		18	30	ns
	t_{LZ}					16	25	ns

※ Switching parameter measurement information

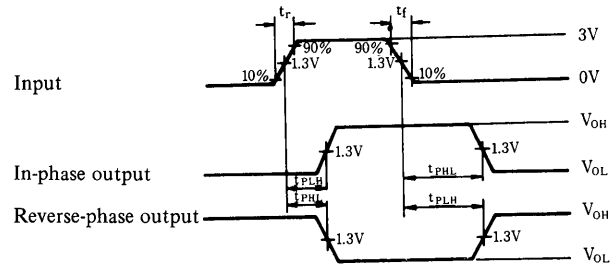
1. Measurement circuit



Notes
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161.

2. Waveforms

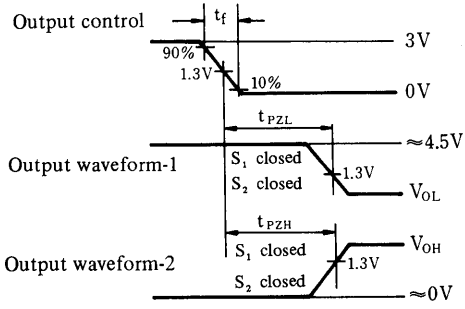
Waveforms-1

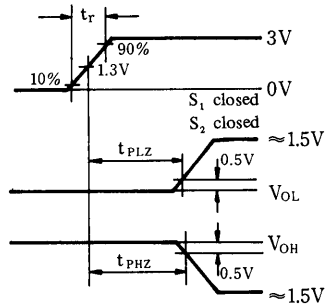


Notes

1. Input waveform: $t_r \leqq 15$ns, $t_f \leqq 6$ns, PRR = 1MHz, duty cycle = 50%.

Waveforms-2





Notes

1. Input waveform: $t_r \leqq 15$ns, $t_f \leqq 6$ns, PRR = 1MHz, duty cycle = 50%.
2. Except when the output is disabled by the output control, output waveform-1 occurs as a result of internal conditions such as a LOW voltage level.
3. Except when the output is disabled by the output control, output waveform-2 occurs as a result of internal conditions such as a HIGH voltage level.

■ Truth tables

Inputs				Outputs
G	S	A	B	
H	×	×	×	Z
L	L	L	×	L
L	L	H	×	H
L	H	×	L	L
L	H	×	H	H

Notes

1. H: HIGH voltage level.
2. L: LOW voltage level.
3. X: Either HIGH or LOW; doesn't matter.
4. Z: High impedance.

DN74LS258A

Quad 2-line to 1-line Data Selectors / Multiplexers (with 3-state Outputs)

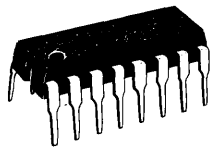
■ Description

DN74LS258A contains four 2-line to 1-line data selector/multiplexer circuits with 3-state outputs.

■ Features

- Inverted output
- Common output-control input for all four circuits
- Common select input for all four circuits
- 3-state outputs
- Wide operating temperature range (Ta = –20 to +75°C)

P-2

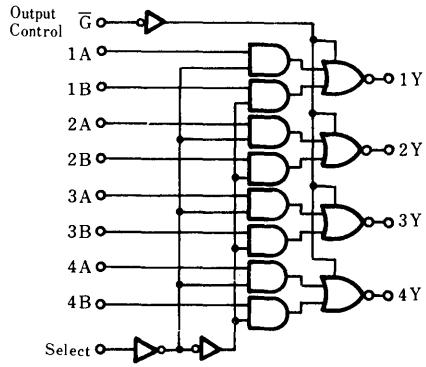


16-pin plastic DIL package

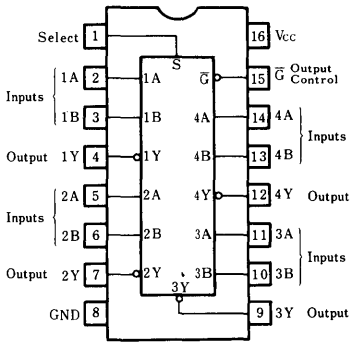
P-5

16-pin Panaflat package (SO-16D)

■ Logic diagram



Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−2.6	mA
	I_{OL}			24	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics (Ta = −20 ~ +75℃)

Parameter		Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Output voltage		V_{OH}	V_{CC} = 4.75V, V_{IH} = 2V V_{IL} = 0.8V, I_{OH} = −2.6mA		2.4	3.1		V
		V_{OL1}	V_{CC} = 4.75V V_{IH} = 2V V_{IL} = 0.8V	I_{OL} = 12mA		0.25	0.4	V
		V_{OL2}		I_{OL} = 24mA		0.35	0.5	V
Input current	S	I_{IH}	V_{CC} = 5.25V V_I = 2.7V				40	μA
	Inputs other than S						20	μA
	S	I_{IL}	V_{CC} = 5.25V V_I = 0.4V				−0.8	mA
	Inputs other than S						−0.4	mA
	S	I_I	V_{CC} = 5.25V V_I = 7V				0.2	mA
	Inputs other than S						0.1	mA
Output current**		I_{OZH}	V_{CC} = 5.25V V_{IH} = 2V	V_O = 2.4V			20	μA
		I_{OZL}		V_O = 0.4V			−20	μA
Output short circuit current***		I_{OS}	V_{CC} = 5.25V, V_O = 0V		−15		−130	mA
Input clamp voltage		V_{IK}	V_{CC} = 4.75V, I_I = −18mA				−1.5	V
**** Supply current	All outputs HIGH	I_{CC}	V_{CC} = 5.25V			4	7	mA
	All outputs LOW					8.8	14	mA
	All outputs OFF					12	19	mA

* When constant at V_{CC} = 5V, Ta = 25°C.

** OFF condition (high impedance condition).

*** Only one output at a time short circuited to GND. Also, short circuit time to GND within 7 seconds.

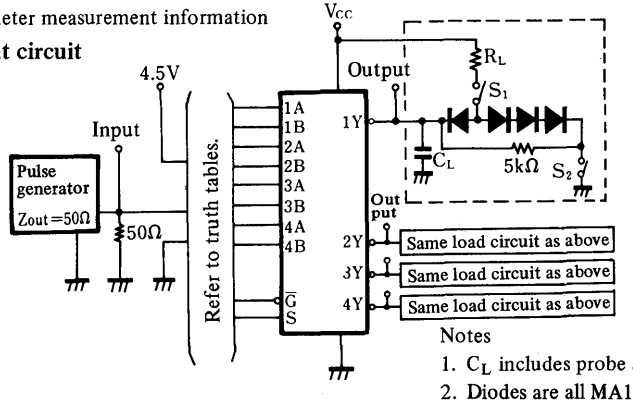
**** Measured with all outputs open and all possible inputs grounded in the range that fulfills the desired output condition.

■ Switching characteristics (V_{CC} = 5V, Ta = 25℃)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	A, B	Y	R_L = 667Ω C_L = 45pF		12	18	ns
	t_{PHL}					12	18	ns
	t_{PLH}	S	Y			14	21	ns
	t_{PHL}					14	21	ns
Output enable time	t_{PZH}	G	Y			20	30	ns
	t_{PZL}					20	30	ns
Output disable time	t_{PHZ}	G	Y	R_L = 667Ω C_L = 5pF		18	30	ns
	t_{PLZ}					18	25	ns

※ Switching parameter measurement information

1. Measurement circuit

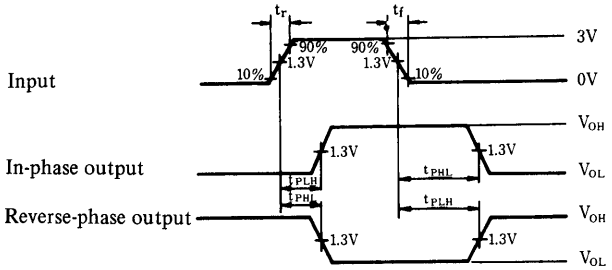


Notes

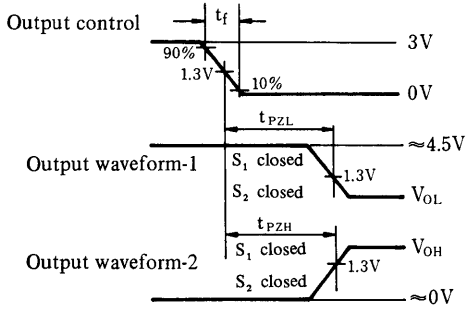
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161 or equivalent.

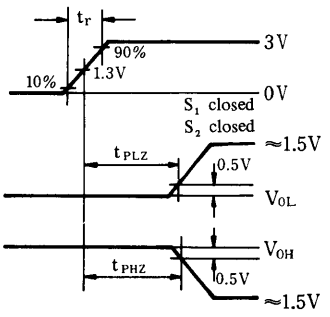
2. Waveforms

Waveforms-1



Notes
1. Input waveform: $t_r \leqq 15$ns, $t_f \leqq 6$ns, PRR = 1MHz, duty cycle = 50%.





Notes
1. Input waveform: $t_r \leqq 15$ns, $t_f \leqq 6$ns, PRR = 1MHz, duty cycle = 50%.
2. Except when the output is disabled by the output control, output waveform-1 occurs as a result of internal conditions such as a LOW voltage level.
3. Except when the output is disabled by the output control, output waveform-2 occurs as a result of internal conditions such as a HIGH voltage level.
4. When measuring t_{PLH} and t_{PHL}, S_1 and S_2 are closed.

■ Truth tables

Inputs				Outputs
G	S	A	B	Y
H	×	×	×	Z
L	L	L	×	H
L	L	H	×	L
L	H	×	L	H
L	H	×	H	L

Notes
1. H: HIGH voltage level.
2. L: LOW voltage level.
3. X: Either HIGH or LOW; doesn't matter.
4. Z: High impedance.

DN74LS260

Dual 5-input Positive NOR Gates

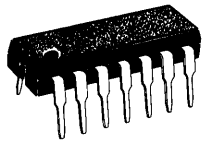
■ Description

DN74LS60 contains two 5-input positive-logic NOR gate circuits.

■ Features

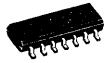
- Low power consumption (P_d = 20mW typical)
- High speed (t_{pd} = 9ns typical)
- Low output impedance
- Wide operating temperature range (Ta = −20 to +75°C)

P-1



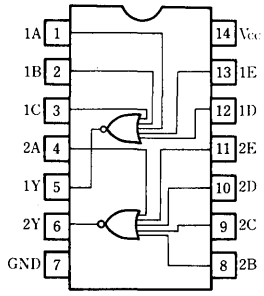
14-pin plastic DIL package

P-4



14-pin Panaflat package (SO-14D)

Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−400	μA
	I_{OL}			8	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IL}=0.8V$ $I_{OH}=-400\mu A$		2.7	3.4		V
	V_{OL1}	$V_{CC}=4.75V$ $V_{IH}=2V$	$I_{OL}=4mA$		0.25	0.4	V
	V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				20	μA
	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.4	mA
	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.1	mA
Output short circuit current**	I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−100	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current***	I_{CCH}	$V_{CC}=5.25V$,				4	mA
	I_{CCL}	$V_{CC}=5.25V$,				5.5	mA

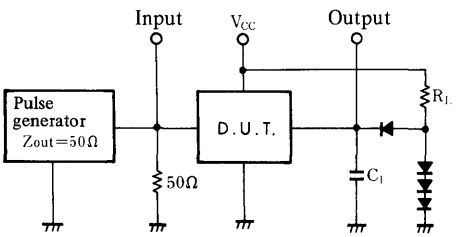
* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	$C_L=15pF$ $R_L=2K\Omega$			12	ns
	t_{PHL}				12	ns

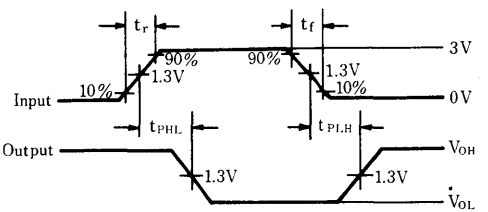
※ Switching parameter measurement information

1. Measurement circuit



Notes
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161.

2. Waveforms



Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.

DN74LS266

Quad 2-input Exclusive NOR Gates (with Open Collector Outputs)

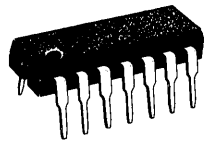
■ Description

DN74LS266 contains four 2-input exclusive NOR gate circuits with open collector outputs.

■ Features

- "Wired" AND capability
- Low power consumption (P_d = 40mW typical)
- Wide operating temperature range (Ta = −20 to +75°C)

P-1



14-pin plastic DIL package

P-4

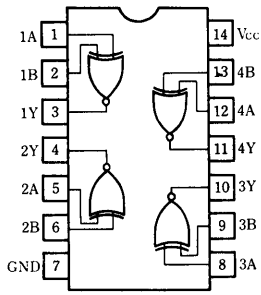
14-pin Panaflat package (SO-14D)

■ Truth tables

Inputs		Outputs
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

Notes:
1. H: HIGH voltage level
2. L: LOW voltage level

Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
HIGH level output voltage	V_{OH}			5.5	V
LOW level output voltage	I_{OL}			8	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OL1}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
	V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$				40	μA
	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$				−0.8	mA
	I_I	$V_{CC}=5.25V$, $V_I=7V$				0.2	mA
Output current	I_{OH}	$V_{CC}=4.75V$, $V_{OH}=5.5V$, $V_{IH}=2V$, $V_{IL}=0.8V$				100	μA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$, $I_I=-18mA$				−1.5	mA
Supply current**	I_{CC}	$V_{CC}=5.25V$			8	13	V

* When constant at V_{CC} = 5V, Ta = 25°C.

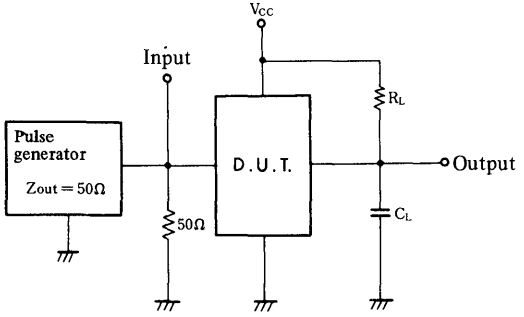
** Measured with all outputs open and input on one side of each gate grounded while 4.5V is applied to the other side.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Test conditions		Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	A or B	other input Low	$C_L=15pF$, $R_L=2k\Omega$		18	30	ns
	t_{PHL}					18	30	ns
	t_{PLH}	A or B	other input Low			18	30	ns
	t_{PHL}					18	30	ns

※ Switching parameter measurement information

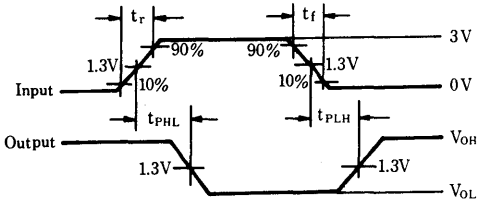
1. Measurement circuit



Notes

1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161.

2. Waveforms



Notes

1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.

DN74LS279

Quad $\overline{S}$-$\overline{R}$ Latches

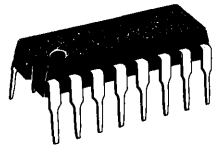
■ Description

DN74LS279 contains four R-S flip-flop circuits.

■ Features

- Low power consumption (P_d = 19mW typical)
- Low output impedance
- Wide operating temperature range (Ta = –20 to +75°C)

P-2

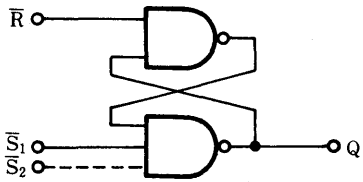


16-pin plastic DIL package

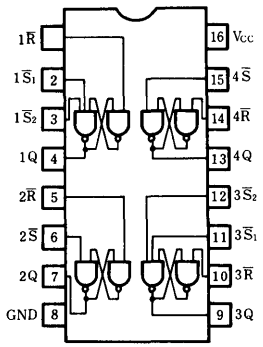
P-5

16-pin Panaflat package (SO-16D)

■ Logic diagram (1/4)



Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−400	μA
	I_{OL}			8	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$ $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	3.4		V
	V_{OL1}	$V_{CC}=4.75V$ $V_{IH}=2V$ $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
	V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				20	μA
	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.4	mA
	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.1	mA
Output short circuit current**	I_{OS}	$V_{CC}=4.75V$, $V_O=0V$		−15		−100	mA
Input clamp voltage	V_{IK}	$V_{CC}=5.25V$ $I_I=-18mA$				−1.5	V
Supply current***	I_{CC}	$V_{CC}=5.25V$			3.8	7	mA

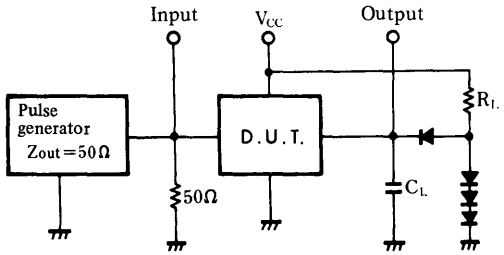
* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.
*** Measured with all outputs open, all R inputs grounded, and 4.5V applied to all S inputs.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	$\overline{S}$	Q	$C_L=15pF$ $R_L=2k\Omega$		12	22	ns
	t_{PHL}					13	21	ns
	t_{PHL}	$\overline{R}$				15	27	ns

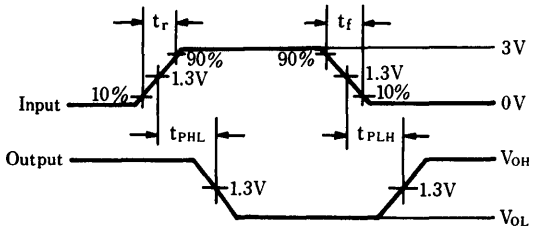
※ Switching parameter measurement information

1. Measurement circuit



Notes
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161.

2. Waveforms



Notes

1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.

■ Truth tables

Inputs		Outputs
$\overline{S}$ **	$\overline{R}$	Q
H	H	Q_0
L	H	H
H	L	L
L	L	H *

Notes

1. H: HIGH voltage level.
2. L: LOW voltage level.
3. Q_0: Level of Q prior to determination of input requirement.
   State of Q cannot be predicted when set and reset simultaneously become HIGH.
   Regarding the two S inputs:
   H indicates that both inputs are HIGH.
   L indicates that either one or both of the inputs are LOW.

DN74LS283

4-bit Binary Full Adders (with Fast Carry)

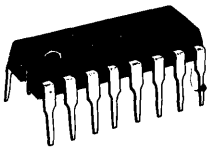
■ Description

DN74LS283 is a 4-bit full adder with a "look-ahead" carry.

■ Features

- "Look-ahead" carry for high speed
- System capability with partial "look-ahead" carry.
- Wide operating temperature range (Ta = −20 to +75°C)

P-2

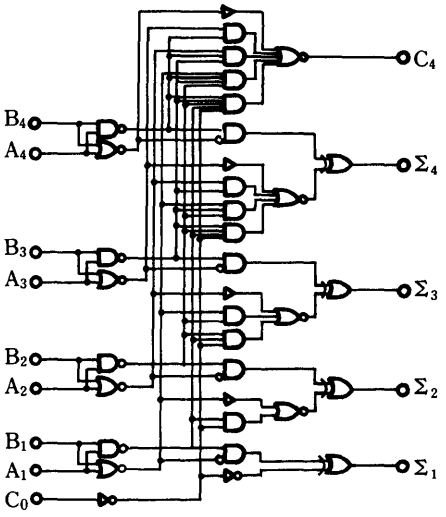


16-pin plastic DIL package

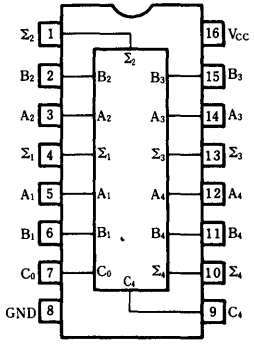
P-5

16-pin Panaflat package (SO-16D)

■ Logic diagram



Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−400	μA
	I_{OL}			8	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter		Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Output voltage		V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$ $V_{IL}=0.8V$,	$I_{OH}=-2.6mA$	2.7	3.4		V
		V_{OL1}	$V_{CC}=4.75V$ $V_{IH}=2V$ $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
		V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	Inputs other than C_O	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				40	μA
	C_O						20	μA
	Inputs other than C_O	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.8	mA
	C_O						−0.4	mA
	Inputs other than C_O	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.2	mA
	C_O						0.1	mA
Output short circuit current**		I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−100	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$, $I_I=-18mA$				−1.5	V
Supply current	All outputs HIGH	I_{CC}	$V_{CC}=5.25V$			22	39	mA
	All outputs LOW					19	34	mA
	All outputs OFF					19	34	mA

* When constant at V_{CC} = 5V, Ta = 25°C.

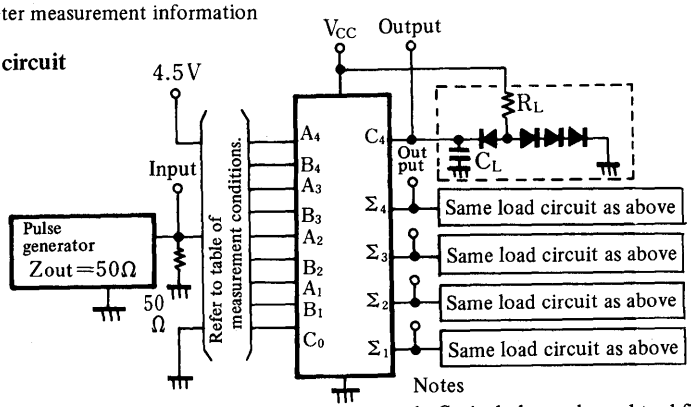
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 7 seconds.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	C_O	Σ	$C_L=15pF$ $R_L=2k\Omega$		16	24	ns
	t_{PHL}					15	24	ns
	t_{PLH}	Ai, Bi	Σi			15	24	ns
	t_{PHL}					15	24	ns
	t_{PLH}	C_O	C_4			11	17	ns
	t_{PHL}					11	22	ns
	t_{PLH}	Ai, Bi	C_4			11	17	ns
	t_{PHL}					12	17	ns

※ Switching parameter measurement information

1. Measurement circuit



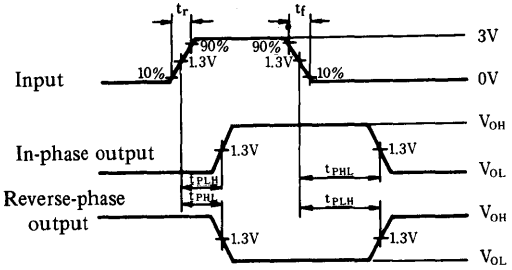
Notes

1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161 or equivalent.

2. Table of measurement conditions

Parameter	Input / Output	Inputs									Outputs				
		B_4	A_4	B_3	A_3	B_2	A_2	B_1	A_1	C_0	C_4	Σ_4	Σ_3	Σ_2	Σ_1
t_{PLH} t_{PHL}	C_0 →Σi or C_4	GND	GND	GND	GND	GND	GND	GND	GND	IN					OUT
		GND	4.5V	GND	4.5V	GND	4.5V	GND	4.5V	IN	OUT	OUT	OUT	OUT	OUT
	Ai or Bi →Σi or C_4	GND	GND	GND	GND	GND	GND	GND / IN	IN / GND	GND					OUT
		GND	GND	GND	GND	GND / IN	GND / IN	GND	GND	GND				OUT	
		GND	GND	GND / IN	IN / GND	GND	GND	GND	GND	GND			OUT		
		GND	IN / GND	GND	GND	GND	GND	GND	GND	GND		OUT			
		GND	GND	GND	GND	GND	GND	4.5V / IN	IN / 4.5V	GND				OUT	OUT
		GND	GND	GND	GND	4.5V / IN	IN / 4.5V	GND	GND	GND			OUT	OUT	
		GND	GND	4.5V / IN	IN / 4.5V	GND	GND	GND	GND	GND		OUT	OUT		
		4.5V / IN	IN / 4.5V	GND	GND	GND	GND	GND	GND	GND	OUT	OUT			

3. Waveforms



Notes

1. Input waveform: $t_r \leqq 15$ns, $t_f \leqq 6$ns, PRR = 1MHz, duty cycle = 50%.

■ Truth tables

Inputs				Outputs					
				When C_0 = L			When C_0 = H		
				When C_2 = L			When C_2 = H		
A_1 / A_3	B_1 / B_3	A_2 / A_4	B_2 / B_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

Notes

1. A_1, B_1, A_2, B_2, and C_0 input requirements are used to determine values for. Σ_1, Σ_2, and the internal carry C_2. C_2, A_3, B_3, A_4, and B_4 values are used to determine the outputs Σ_3, Σ_4, C_4. (C_2 is not output as an external signal.)
2. H: HIGH voltage level.
3. L: LOW voltage level.

DN74LS290

Decade Counters

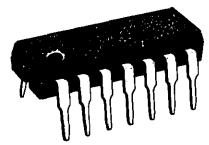
■ Description

DN74LS290 is an asynchronous decade counter with a direct-coupled reset input and nine direct-coupled set inputs.

■ Features

- Direct-coupled reset input
- Nine direct-coupled set inputs
- Capability for independent use as binary and quinary counters
- High-speed counting (f_{max} = 42MHz typical)
- Wide operating temperature range (Ta = −20 to +75°C)

P-1

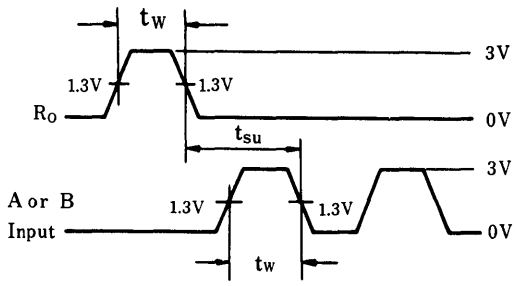


14-pin plastic DIL package

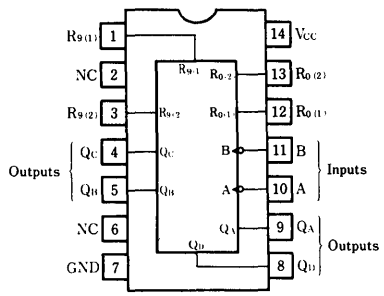
P-4

14-pin Panaflat package (SO-14D)

■ Timing definition



Pin configuration (top view)



■ Absolute maximum ratings

Parameter		Sym.	Rating		Unit
Input voltage	R	V_I	−0.5	7.0	V
	A, B		−0.5	5.5	

* Refer to the family ratings for other parameters.

■ Recommended operating conditions

Parameter		Sym	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}			−400	μA
		I_{OL}			8	mA
Operating temperature range		Topr	−20	25	75	℃
Count frequency	A input	f_{count}	0		32	MHz
	B input		0		16	MHz
Pulse width	A input	t_W	15			ns
	B input		30			ns
	Reset input		15			ns
Set-up time		t_{su}	25			ns

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter		Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Output voltage**		V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$ $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	3.4		V
		V_{OL1}	$V_{CC}=4.75V$ $V_{IH}=2V$ $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
		V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	Any Reset	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				20	μA
	A input						40	μA
	B input						80	μA
	Any Reset	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.4	mA
	A input						−2.4	mA
	B input						−3.2	mA
	Any Reset	I_I	$V_{CC}=5.25V$	$V_I=7V$			0.1	mA
	A input			$V_I=5.5V$			0.2	mA
	B input						0.4	mA
Output short circuit current***		I_{OS}	$V_O=0V$ $V_{CC}=5.25$		−15		−100	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current****		I_{CC}	$V_{CC}=5.25V$			9	15	mA

* When constant at V_{CC} = 5V, Ta = 25°C.

** When testing Q_A output, a current to which the rated upper limit value for the I_{IL} of the B input has been added is applied to the specified I_{OL}.

*** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

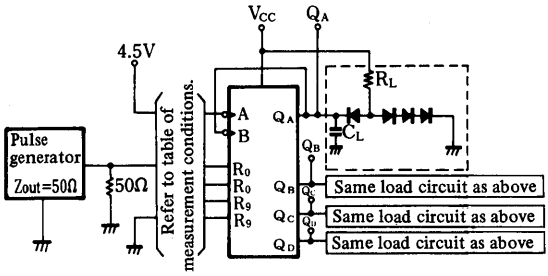
**** I_{CC} is measured with all outputs open and all inputs except both R_O inputs grounded; 4.5V applied momentarily to both R_O inputs, following which they are grounded.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Maximum count frequency	f_{max}	A	Q_A	$R_L=2k\Omega$ $C_L=15pF$	32	42		MHz
		B	Q_B		16			MHz
Propagation delay time	t_{PLH}	A	Q_A			10	16	ns
	t_{PHL}					12	18	ns
	t_{PLH}	A	Q_D			32	48	ns
	t_{PHL}					34	50	ns
	t_{PLH}	B	Q_B			10	16	ns
	t_{PHL}					14	21	ns
	t_{PLH}	B	Q_C			21	32	ns
	t_{PHL}					23	35	ns
	t_{PLH}	B	Q_D			21	32	ns
	t_{PHL}					23	35	ns
	t_{PHL}	Set-to-0	$Q_A \sim Q_D$			26	40	ns
	t_{PLH}	Set-to-9	Q_A, Q_D			20	30	ns
	t_{PHL}		Q_B, Q_C			26	40	ns

※ Switching parameter measurement information

1. Measurement circuit



1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161.

2. Table of measurement conditions

Parameter	Input Output	Inputs				Outputs			
		A	B	R_0	R_9	Q_A	Q_B	Q_C	Q_D
f_{max}	A →Q	IN	to Q_A	GND	GND	OUT	OUT	OUT	OUT
	B**→Q	4.5V	IN	GND	GND		OUT	OUT	OUT
t_{PLH} t_{PHL}	A →Q_A	IN	to Q_A	GND	GND	OUT			
	A →Q_D	IN	to Q_A	GND	GND				OUT
	B**→Q_B	4.5V	IN	GND	GND		OUT		
	B**→Q_C	4.5V	IN	GND	GND			OUT	
	B**→Q_D	4.5V	IN	GND	GND				OUT
	R_0 →Q***	IN*	to Q_A	IN	GND	OUT	OUT	OUT	OUT
	R_9 →Q***	IN*	to Q_A	GND	IN	OUT	OUT	OUT	OUT

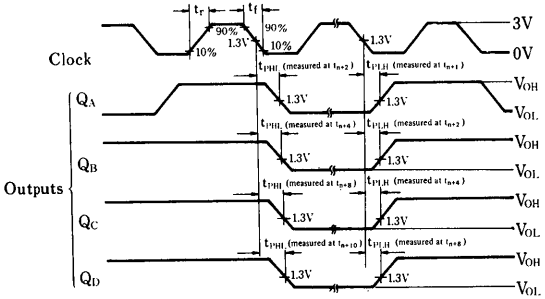
* Applied for initialization.

** For characteristic measurement from B input, Q_A and B are disconnected and pulse is applied to B input.

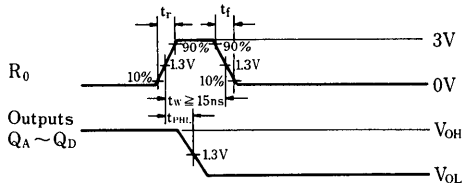
*** Measured for each terminal; 4.5V applied to terminals to which input pulse is not applied.

3.Waveforms

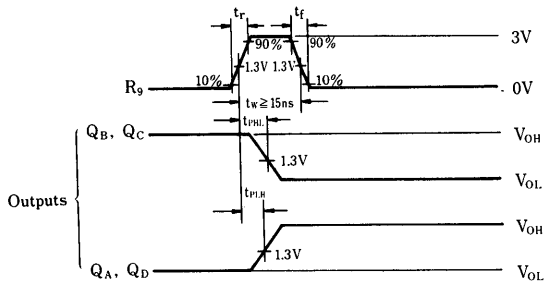
Waveforms-1 f_{max}, t_{PLH}, t_{PHL} (Clock → Q)



Waveforms-2 t_{PHL} (R_0 → Q)



Waveforms-3 t_{PLH}, t_{PHL} (R_9 → Q)

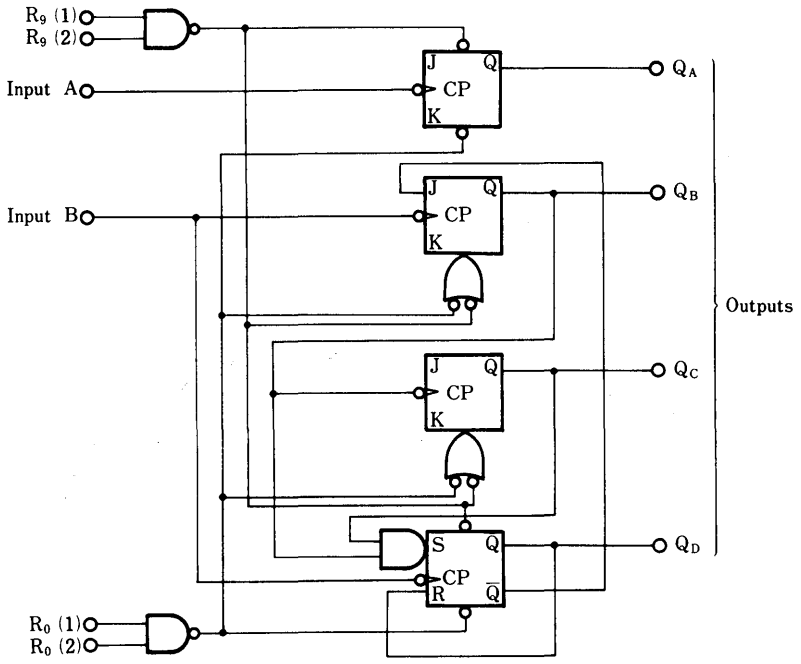


Notes

1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$,
   PRR = 1MHz, duty cycle = 50%.
2. Pulse generator output impedance: $Z_{out} = 50$ ohms.
3. t_n is the bit time when all outputs are LOW.

Notes 1. $t_r \leqq 15ns$, $t_f \leqq 5ns$

■ Logic diagram



DN74LS293

4-bit Binary Counters

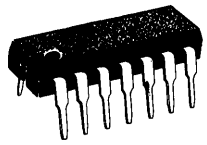
■ Description

DN74LS293 is an asynchronous 4-bit binary (hexadecimal) counter with direct-coupled reset input.

■ Features

- Direct-coupled reset input
- Capability for independent use as binary and octal counters
- High-speed counting (f_{max} = 42MHz typical)
- Wide operating temperature range (Ta = –20 to +75°C)

P-1

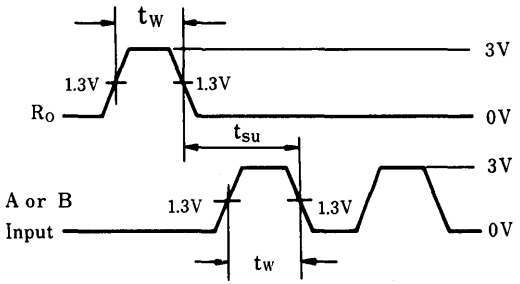


14-pin plastic DIL package

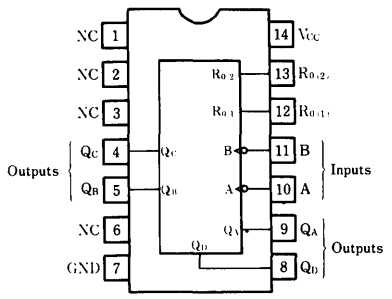
P-4

14-pin Panaflat package (SO-14D)

■ Timing definition



Pin configuration (top view)



■ Absolute maximum ratings

Parameter		Sym.	Rating		Unit
Input voltage	R	V_I	–0.5	7.0	V
	A, B		–0.5	5.5	

* Refer to the family ratings for other parameters.

■ Recommended operating conditions

Parameter		Sym	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}			–400	μA
		I_{OL}			8	mA
Operating temperature range		Topr	–20	25	75	℃
Count frequency	A input	f_{count}	0		32	MHz
	B input		0		16	MHz
Pulse width	A input	t_W	15			ns
	B input		30			ns
	Reset input		15			ns
Set-up time		t_{su}	25			ns

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter		Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Output voltage**		V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$ $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	3.4		V
		V_{OL1}	$V_{CC}=4.75V$ $V_{IH}=2V$ $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
		V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	Any Reset	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				20	μA
	A input						40	μA
	B input						40	μA
	Any Reset	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.4	mA
	A input						−2.4	mA
	B input						−1.6	mA
	Any Reset	I_I	$V_{CC}=5.25V$	$V_I=7V$			0.1	mA
	A input			$V_I=5.5V$			0.2	mA
	B input						0.2	mA
Output short circuit current***		I_{OS}	$V_O=0V$ $V_{CC}=5.25$		−15		−100	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				1.5	V
Supply current****		I_{CC}	$V_{CC}=5.25V$			9	15	mA

* When constant at V_{CC} = 5V, Ta = 25°C.

** When testing Q_A output, a current to which the rated upper limit value for the I_{IL} of the B input has been added is applied to the specified I_{OL}.

*** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

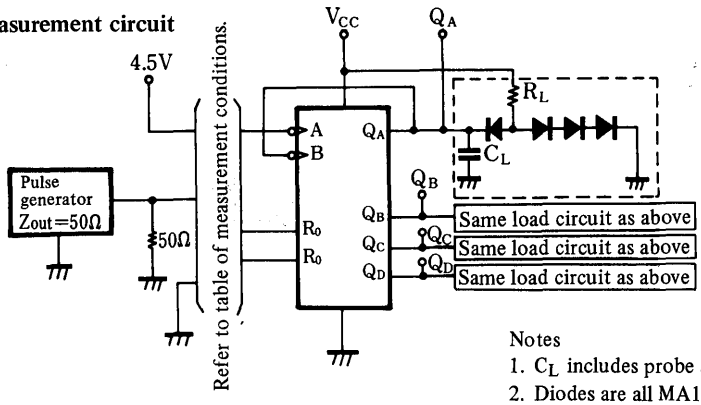
**** I_{CC} is measured with all outputs open and all inputs except both R_O inputs grounded; 4.5V applied momentarily to both R_O inputs, following which they are grounded.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Maximum count frequency	f_{max}	A	Q_A	$C_L=15pF$ $R_L=2k\Omega$	32	42		MHz
		B	Q_B		16			MHz
Propagation delay time	t_{PLH}	A	Q_A			10	16	ns
	t_{PHL}					12	18	ns
	t_{PLH}	A	Q_D			46	70	ns
	t_{PHL}					46	70	ns
	t_{PLH}	B	Q_B			10	16	ns
	t_{PHL}					14	21	ns
	t_{PLH}	B	Q_C			21	32	ns
	t_{PHL}					23	35	ns
	t_{PLH}	B	Q_D			34	51	ns
	t_{PHL}					34	51	ns
	t_{PHL}	Set-to-0	$Q_A \sim Q_D$			26	40	ns

※ Switching parameter measurement information

1. Measurement circuit



Notes
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161.

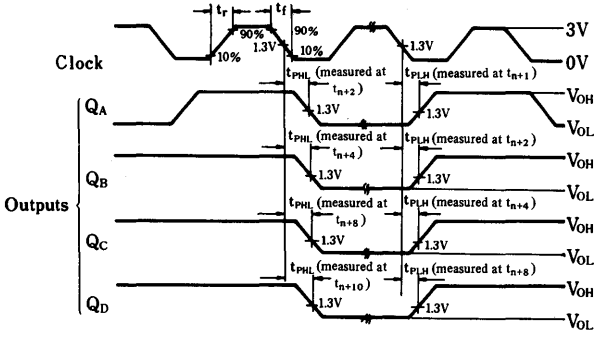
2. Table of measurement conditions

Parameter	Inputs/Outputs	Inputs			Outputs			
		A	B	R_0	Q_A	Q_B	Q_C	Q_D
f_{max}	A →Q	IN	to Q_A	GND	OUT	OUT	OUT	OUT
	B **→Q	4.5V	IN	GND		OUT	OUT	OUT
t_{PLH} t_{PHL}	A →Q_A	IN	to Q_A	GND	OUT			
	A →Q_D	IN	to Q_A	GND				OUT
	B **→Q_B	4.5V	IN	GND		OUT		
	B **→Q_C	4.5V	IN	GND			OUT	
	B **→Q_D	4.5V	IN	GND				OUT
	R_0 →Q	IN *	to Q_A	IN	OUT	OUT	OUT	OUT

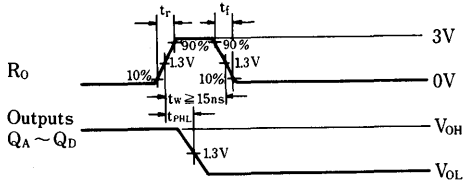
* Applied for initialization.
** For characteristic measurement from B input, Q_A and B are disconnected and pulse is applied to B input.
*** Measured for each input terminal; 4.5V applied to terminals to which input pulse is not applied.

3.Waveforms

Waveforms-1 f_{max}, t_{PLH}, t_{PHL} (Clock → Q)



Waveforms-2 t_{PHL} (R_0 → Q)



Notes 1. $t_r \leqq 15ns$, $t_f \leqq 5ns$

Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.
2. Pulse generator output impedance: Z_{out} = 50 ohms.
3. t_n is the bit time when all outputs are LOW.

■ Truth tables

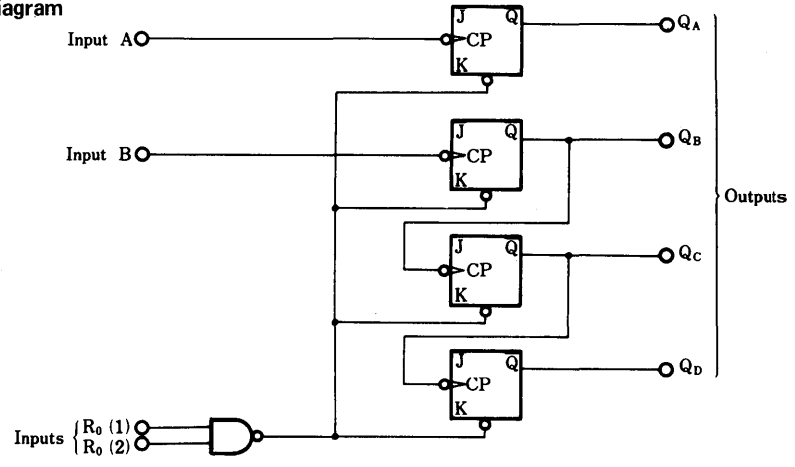
Reset inputs		Outputs			
$R_{O(1)}$	$R_{O(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	×	Count			
×	L	Couot			

Count	Outputs			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

Notes

1. H: HIGH voltage level.
2. L: LOW voltage level.
3. X: Either HIGH or LOW; doesn't matter.
4. Output Q_A is connected to input B and count pulse is applied to input A.

■ Logic diagram



DN74LS365A

Hex Bus Drivers (with 3-state Outputs)

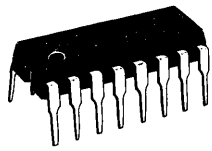
■ Description

DN74LS365A contains six 3-state output buffer circuits with common output-control inputs $\overline{G}_1$ and $\overline{G}_2$.

■ Features

- High fan-out (I_{OL} = 24mA, I_{OH} = −2.6mA)
- Wide operating temperature range (Ta = −20 to +75°C)

P-2



16-pin plastic DIL package

P-5

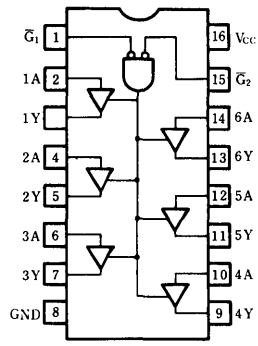
16-pin Panaflat package (SO-16D)

■ Truth tables

Inputs			Outputs
$\overline{G}_1$	$\overline{G}_2$	A	Y
L	L	L	L
L	L	H	H
×	H	×	Z
H	×	×	Z

Notes:
1. H: HIGH voltage level
2. L: LOW voltage level
3. X: Either HIGH or LOW; doesn't matter
4. Z: High impedance

Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−2.6	mA
	I_{OL}			24	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter		Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Output voltage		V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$,	$I_{OH}=-2.6mA$	2.4	3.1		V
		V_{OL1}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$	$I_{OL}=12mA$		0.25	0.4	V
		V_{OL2}		$I_{OL}=24mA$		0.35	0.5	V
Output OFF current		I_{OZH}	$V_{CC}=5.25V$, $V_{IH}=2V$, $V_{IL}=0.8V$	$V_O=2.4V$			20	μA
		I_{OZL}		$V_O=0.4V$			−20	μA
Input current		I_{IH}	$V_{CC}=5.25V$, $V_{IH}=2.7V$				20	μA
	A input	I_{IL}	$V_{CC}=5.25V$, either G input = 2V, $V_I=0.5V$,				−20	μA
			$V_{CC}=5.25V$, both G inputs=0.4V, $V_I=0.4V$,				−0.4	mA
	$\overline{G}$ input		$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
		I_I	$V_{CC}=5.25V$, $V_I=7V$				0.1	mA
Output short circuit current**		I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−130	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$, $I_I=-18mA$				−1.5	V
Supply current***		I_{CC}	$V_{CC}=5.25V$			14	24	mA

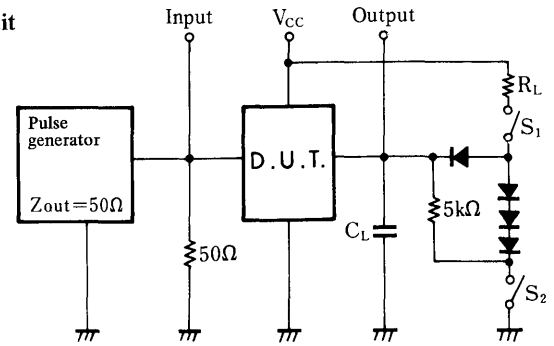
* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. also, short circuit time to GND within 1 second
*** Measured with all outputs open, all inputs grounded, and 4.5V applied to all $\overline{G}$ inputs.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	$C_L=45pF$, $R_L=667\Omega$		10	16	ns
	t_{PHL}			9	22	ns
Output enable time	t_{PZH}			19	35	ns
	t_{PZL}			24	40	ns
Output disable time	t_{PHZ}	$C_L=5pF$, $R_L=667\Omega$			30	ns
	t_{PLZ}				35	ns

※ Switching parameter measurement information

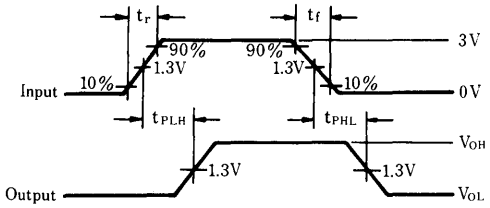
1. Measurement circuit



Notes
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161.

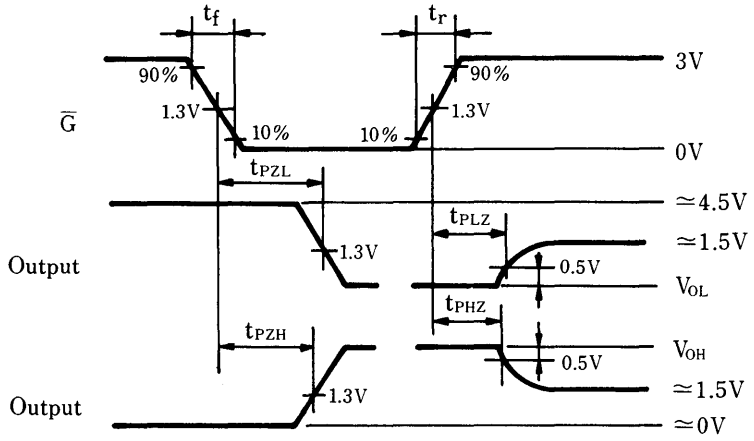
2. Waveforms

Waveforms-1



Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.

Waveforms-2



Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$

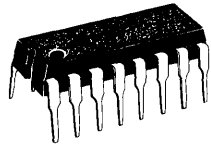
DN74LS366A

Hex Bus Drivers (with 3-state Outputs)

■ Description

DN74LS366A contains six 3-state output inverter buffer circuits with common output-control inputs $\overline{G}_1$ and $\overline{G}_2$.

P-2



16-pin plastic DIL package

P-5

16-pin Panaflat package (SO-16D)

■ Features

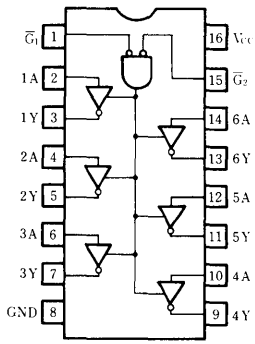
- Common output-control inputs for all six circuits
- High fan-out (I_{OL} = 24mA, I_{OH} = −2.6mA)
- Wide operating temperature range (Ta = −20 to +75°C)

■ Truth tables

Inputs			Outputs
$\overline{G}_1$	$\overline{G}_2$	A	Y
H	×	×	Z
×	H	×	Z
L	L	H	L
L	L	L	H

Notes
1. H: HIGH voltage level.
2. L: LOW voltage level.
3. X: Either HIGH or LOW; doesn't matter.
4. Z: High impedance.

Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−2.6	mA
	I_{OL}			24	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter		Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Output voltage		V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-2.6mA$		2.4	3.1		V
		V_{OL1}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$	$I_{OL}=12mA$		0.25	0.4	V
		V_{OL2}		$I_{OL}=24mA$		0.35	0.5	V
Output OFF current		I_{OZH}	$V_{CC}=5.25V$, $V_{IH}=2V$, $V_{IL}=0.8V$	$V_O=2.4V$			20	μA
		I_{OZL}		$V_O=0.4V$			−20	μA
Input current		I_{IH}	$V_{CC}=5.25V$, $V_{IH}=2.7V$				20	μA
	A input	I_{IL}	$V_{CC}=5.25V$, either G input = 2V, $V_I=0.5V$,				−20	μA
			$V_{CC}=5.25V$, both G inputs=0.4V, $V_I=0.4V$,				−0.4	mA
	$\overline{G}$ input		$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
		I_I	$V_{CC}=5.25V$, $V_I=7V$				0.1	mA
Output short circuit current**		I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−130	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$, $I_I=-18mA$				−1.5	V
Supply current***		I_{CC}	$V_{CC}=5.25V$			12	21	mA

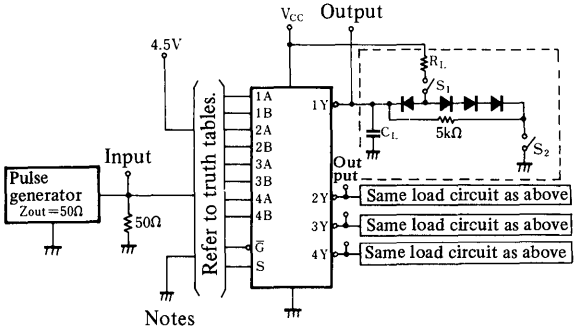
* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. also, short circuit time to GND within 1 second
*** Measured with all outputs open, all inputs grounded, and 4.5V applied to all G inputs.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	$C_L=45pF$, $R_L=667\Omega$		7	15	ns
	t_{PHL}			12	18	ns
Output enable time	t_{ZH}			18	35	ns
	t_{ZL}			28	45	ns
Output disable time	t_{HZ}	$C_L=5pF$, $R_L=667\Omega$			32	ns
	t_{LZ}				35	ns

※ Switching parameter measurement information

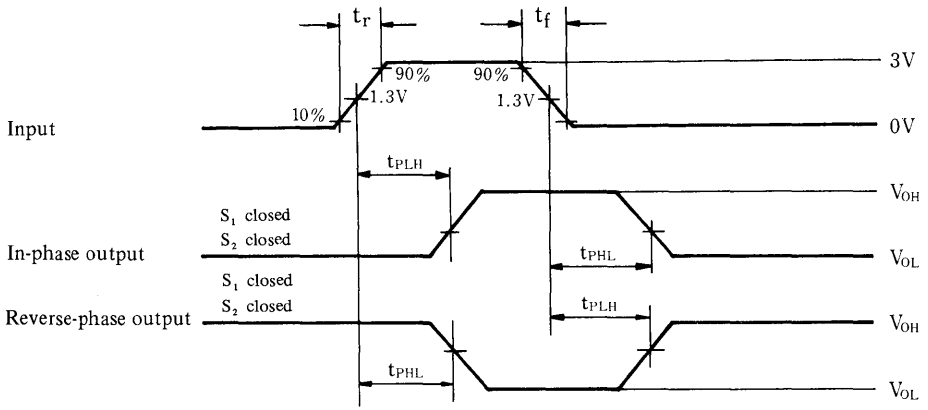
1. Measurement circuit



Notes
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161 or equivalent.

2. Waveforms

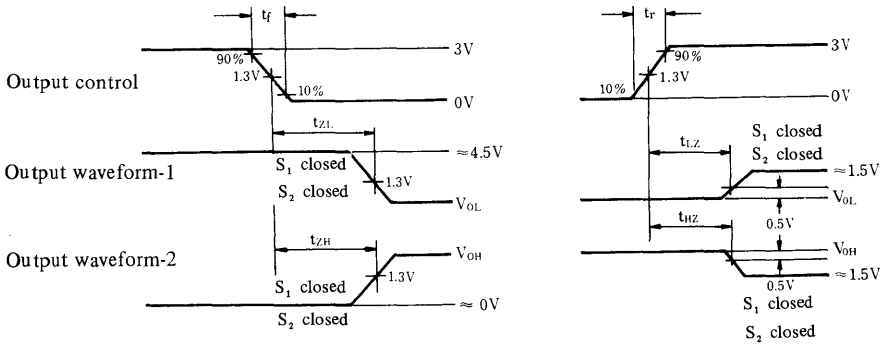
Waveforms-1



Notes

1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%

Waveforms-2



Notes

1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.
2. Except when the output is disabled by the output control, output waveform-1 occurs as a result of internal conditions such as a LOW voltage level.
3. Except when the output is disabled by the output control, output waveform-2 occurs as a result of internal conditions such as a HIGH voltage level.
4. When measuring t_{PLH} and t_{PHL}, S_1 and S_2 are closed.

DN74LS367A

Hex Bus Drivers (with 3-state Outputs)

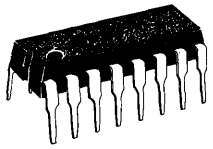
■ Description

DN74LS367A contains six 3-state output buffer circuits with common output-control inputs $\overline{G}_1$ and G_2 for four circuits and two circuits respectively.

■ Features

- Common output-control inputs four circuits and two circuits respectively
- High fan-out (I_{OL} = 24mA, I_{OH} = −2.6mA)
- Wide operating temperature range (Ta = −20 to +75°C)

P-2



16-pin plastic DIL package

P-5

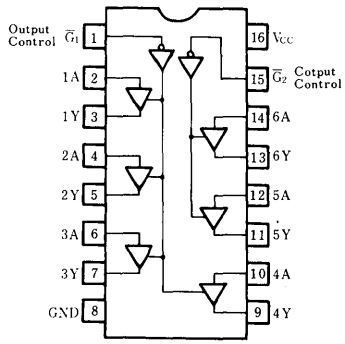
16-pin Panaflat package (SO-16D)

■ Truth tables

Inputs		Outputs
$\overline{G}$	A	Y
L	L	L
L	H	H
H	×	Z

Notes
1. H: HIGH voltage level.
2. L: LOW voltage level.
3. X: Either HIGH or LOW; doesn't matter.
4. Z: High impedance.

Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−2.6	mA
	I_{OL}			24	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter		Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Output voltage		V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$,	$I_{OH}=-2.6mA$	2.4	3.1		V
		V_{OL1}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$	$I_{OL}=12mA$		0.25	0.4	V
		V_{OL2}		$I_{OL}=24mA$		0.35	0.5	V
Output current		I_{OZH}	$V_{CC}=5.25V$, $V_{IH}=2V$, $V_{IL}=0.8V$	$V_O=2.4V$			20	μA
		I_{OZL}		$V_O=0.4V$			−20	μA
Input current		I_{IH}	$V_{CC}=5.25V$, $V_{IH}=2.7V$				20	μA
	A input	I_{IL}	$V_{CC}=5.25V$, either G input = 2V, $V_I=0.5V$,				−20	μA
	A input		$V_{CC}=5.25V$, both G inputs=0.4V, $V_I=0.4V$,				−0.4	mA
	$\overline{G}$ input		$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
		I_I	$V_{CC}=5.25V$, $V_I=7V$				0.1	mA
Output short circuit current**		I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−130	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$, $I_I=-18mA$				−1.5	V
Supply current***		I_{CC}	$V_{CC}=5.25V$			14	24	mA

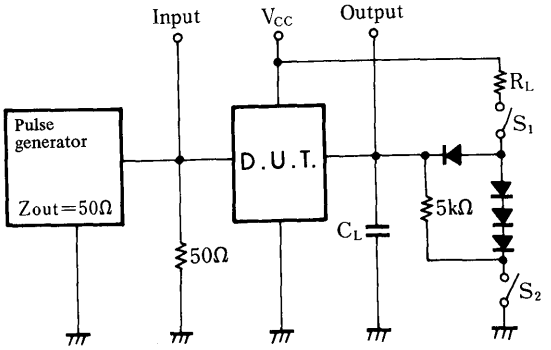
* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. also, short circuit time to GND within 1 second
*** Measured with all outputs open, all inputs grounded, and 4.5V applied to all $\overline{G}$ inputs.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	$C_L=45pF$, $R_L=667\Omega$		10	16	ns
	t_{PHL}			9	22	ns
Output enable time	t_{PZH}			19	35	ns
	t_{PZL}			24	40	ns
Output disable time	t_{PHZ}	$C_L=5pF$, $R_L=667\Omega$			30	ns
	t_{PLZ}				35	ns

※ Switching parameter measurement information

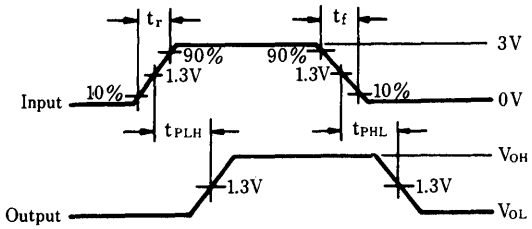
1. Measurement circuit



Notes
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161.

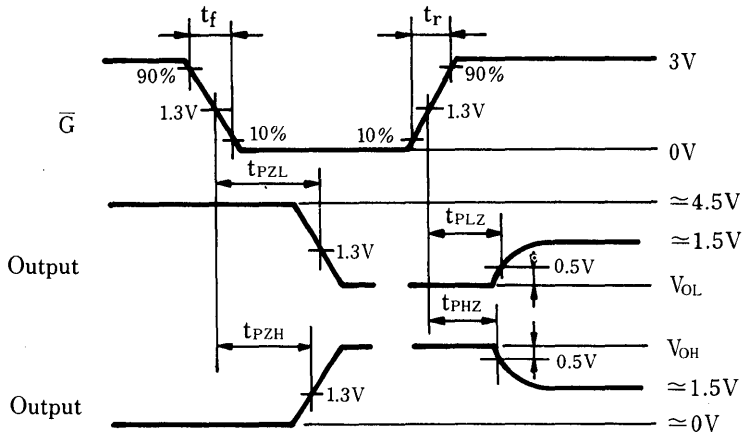
2. Waveforms

Waveforms-1



Notes
1. Input waveform: $t_r \leqq 15$ns, $t_f \leqq 6$ns, PRR = 1MHz, duty cycle = 50%.

Waveforms-2



Notes
1. Input waveform: $t_r \leqq 15$ns, $t_f \leqq 6$ns

DN74LS368A

Hex Bus Drivers (with 3-state Outputs)

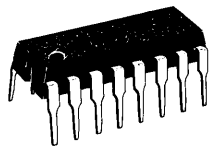
■ Description

DN74LS368A contains six 3-state output inverter buffer circuits with output-control inputs $\overline{G}_1$ and G_2 for four and two circuits respectively.

■ Features

- Common output-control inputs for four circuits and two circuits respectively
- High fan-out (I_{OL} = 24mA, I_{OH} = −2.6mA)

P-2



16-pin plastic DIL package

P-5

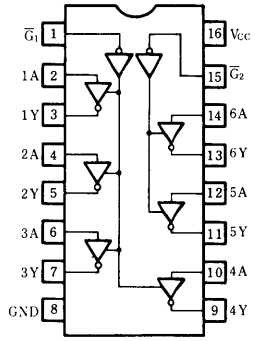
16-pin Panaflat package (SO-16D)

■ Truth tables

Inputs		Outputs
$\overline{G}$	A	Y
L	L	H
L	H	L
H	×	Z

Notes
1. H: HIGH voltage level.
2. L: LOW voltage level.
3. X: Either HIGH or LOW; doesn't matter.
4. Z: High impedance.

Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−2.6	mA
	I_{OL}			24	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter		Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Output voltage		V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-2.6mA$		2.4	3.1		V
		V_{OL1}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$	$I_{OL}=12mA$		0.25	0.4	V
		V_{OL2}		$I_{OL}=24mA$		0.35	0.5	V
Output current		I_{OZH}	$V_{CC}=5.25V$, $V_{IH}=2V$, $V_{IL}=0.8V$	$V_O=2.4V$			20	μA
		I_{OZL}		$V_O=0.4V$			−20	μA
Input current		I_{IH}	$V_{CC}=5.25V$, $V_{IH}=2.7V$				20	μA
	A input	I_{IL}	$V_{CC}=5.25V$, either G input = 2V, $V_I=0.5V$,				−20	μA
	A input		$V_{CC}=5.25V$, both $\overline{G}$ inputs=0.4V $V_I=0.4V$,				−0.4	mA
	$\overline{G}$ input		$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
		I_I	$V_{CC}=5.25V$, $V_I=7V$				0.1	mA
Output short circuit current**		I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−130	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$, $I_I=-18mA$				−1.5	V
Supply current***		I_{CC}	$V_{CC}=5.25V$			12	21	mA

* When constant at V_{CC} = 5V, Ta = 25°C.

** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

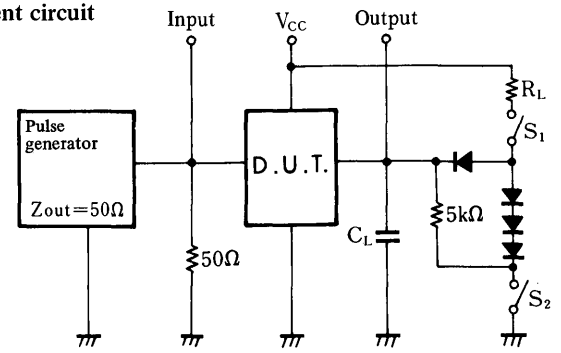
*** Measured with all outputs open, all inputs grounded, and 4.5V applied to all $\overline{G}$ inputs.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	$C_L=45pF$, $R_L=667\Omega$		7	15	ns
	t_{PHL}			12	18	ns
Output enable time	t_{PZH}			18	35	ns
	t_{PZL}			28	45	ns
Output disable time	t_{PHZ}	$C_L=5pF$, $R_L=667\Omega$			32	ns
	t_{PLZ}				35	ns

※ Switching parameter measurement information

1. Measurement circuit

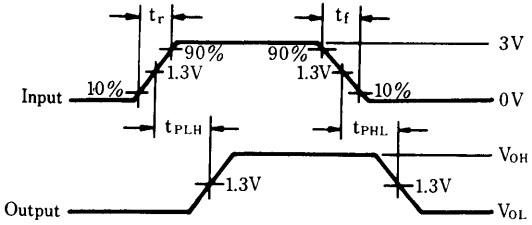


Notes

1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161.

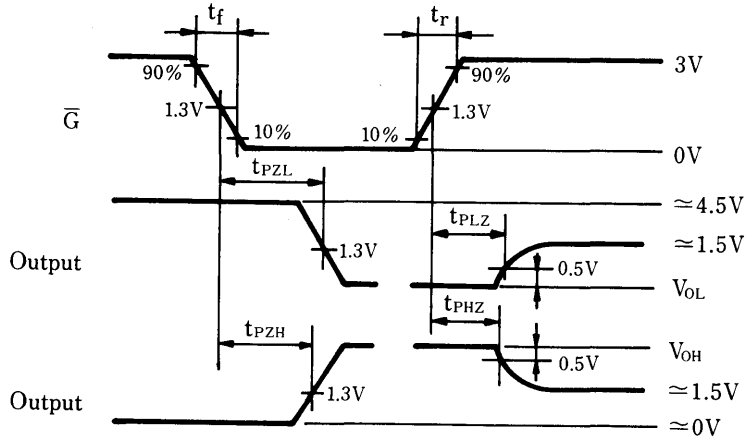
2. Waveforms

Waveforms-1



Notes
1. Input waveform: $t_r \leqq 15$ns, $t_f \leqq 6$ns, PRR = 1MHz, duty cycle = 50%.

Waveforms-2



Notes
1. Input waveform: $t_r \leqq 15$ns, $t_f \leqq 6$ns

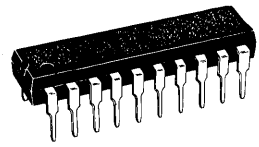
DN74LS373

Octal D-type Transparent Latches (with 3-state Outputs)

■ Description

DN74LS373 contains eight 3-state output D-type latch circuits with common output-control enable inputs for all circuits.

P-3



20-pin plastic DIL package

P-6

20-pin Panaflat package (SO-20D)

■ Features

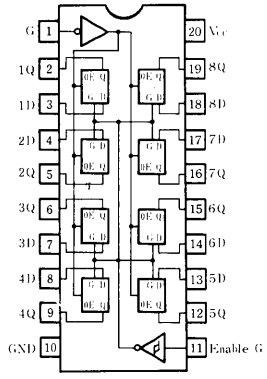
- 3-state high fan-out outputs (I_{OH} = 24mA, I_{OH} = −2.6mA)
- pnp output-control and enable inputs for small input load coefficient
- High noise margin for enable input (hysteresis width = 400mV typical)
- Eight circuits for high mounting density
- Common output-control and enable inputs for all eight circuits
- Wide operating temperature range (Ta = −20 to +75°C)

■ Truth tables

Outputs	Enable Inputs		Outputs
	G	D	
L	H	H	H
L	H	L	L
L	L	×	Q_0
H	×	×	Z

Notes
1. H: HIGH voltage level.
2. L: LOW voltage level.
3. X: Either HIGH or LOW; doesn't matter.
4. Z: High impedance.
5. Q_0: Q level before determination of the input conditions shown in the table.

Pin configuration (top view)



■ Recommended operating conditions

Parameter		Sym	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
		I_{OH}			−2.6	mA
Output current		I_{OL}			24	mA
Operating temperature range		Topy	−20	25	75	℃
Pulse width	"H"	t_W	15			ns
	"L"		15			ns
Set-up time		t_{su}	5↓			ns
Hold time		th	20↓			ns

Note: ↓: Change from HIGH to LOW.

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$ $V_{IL}=0.8V$, $I_{OH}=-26mA$		2.4	3.1		V
	V_{OL1}	$V_{CC}=4.75V$ $V_{IH}=2V$ $V_{IL}=0.8V$	$I_{OL}=12mA$		0.25	0.4	V
	V_{OL2}		$I_{OL}=24mA$		0.35	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				20	μA
	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.4	mA
	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.1	mA
Output current	I_{OZ1}	$V_{CC}=5.25V$ $V_{IH}=2V$	$V_O=0.4V$			−20	μA
	I_{OZ2}		$V_O=2.7V$			20	μA
Output short circuit current**	I_{OS}	$V_{CC}=5.25V$ $V_O=0V$		−15		−130	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current	I_{CC}	$V_{CC}=5.25V$			24	40	mA

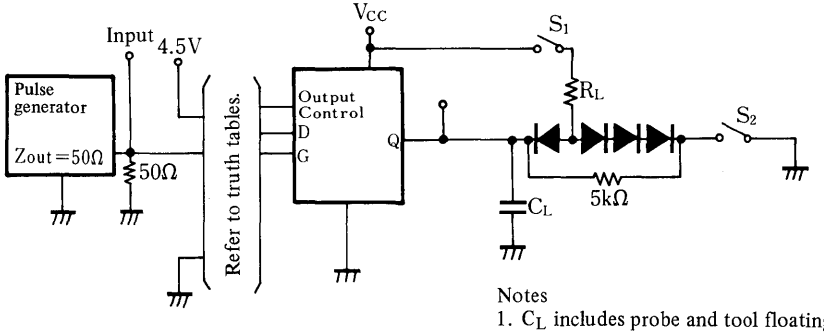
* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	Data	any Q	$C_L=45pF$ $R_L=667Ω$		12	18	ns
	t_{PHL}					12	18	ns
	t_{PLH}	Clock or Enable	any Q			20	30	ns
	t_{PHL}					18	30	ns
	t_{PZH}	Output Control	any Q			15	28	ns
	t_{PZL}					25	36	ns
	t_{PHZ}	Output Control	any Q	$C_L=5pF$ $R_L=667Ω$		12	20	ns
	t_{PLZ}					15	25	ns

※ Switching parameter measurement information

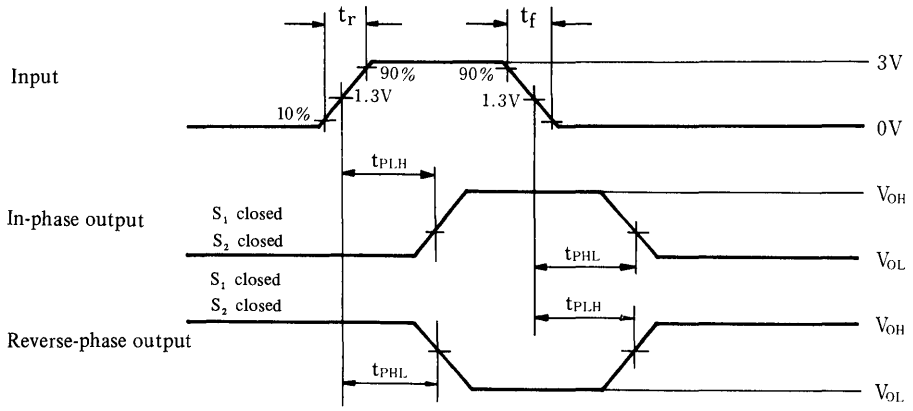
1. Measurement circuit



Notes
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161.

2. Waveforms

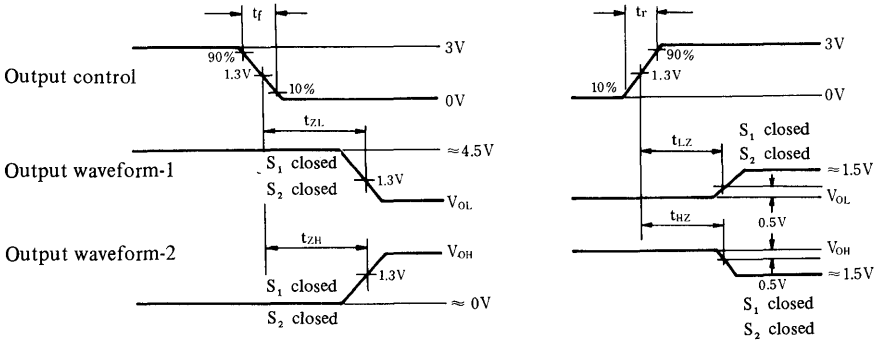
Waveforms-1



Notes

1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.

Waveforms-2



Notes

1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.
2. Except when the output is disabled by the output control, output waveform-1 occurs as a result of internal conditions such as a LOW voltage level.
3. Except when the output is disabled by the output control, output waveform-2 occurs as a result of internal conditions such as a HIGH voltage level.
4. When measuring t_{PLH} and t_{PHL}, S_1 and S_2 are ON.

DN74LS386

Quad 2-input Exclusive OR Gates

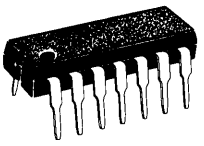
■ Description

DN74LS386 contains four 2-input exclusive OR gate circuits.

■ Features

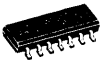
- Low power consumption (P_d = 30.5mW typical)
- High speed (t_{pd} = 11ns typical)
- Low output impedance
- Wide operating temperature range (Ta = –20 to +75°C)

P-1



14-pin plastic DIL package

P-4



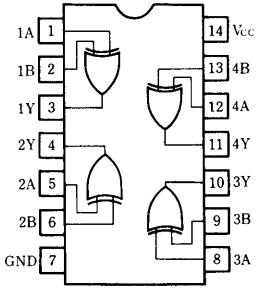
14-pin Panaflat package (SO-14D)

■ Truth tables

Inputs		Outputs
A	B	
L	L	L
L	H	H
H	L	H
H	H	L

Notes
1. H: HIGH voltage level.
2. L: LOW voltage level.

Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−400	μA
	I_{OL}			8	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$ $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	3.4		V
	V_{OL1}	$V_{CC}=4.75V$ $V_{IH}=2V$ $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
	V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				40	μA
	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.8	mA
	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.2	mA
Output short circuit current**	I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−100	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current***	I_{CC}	$V_{CC}=5.25V$			6.1	10	mA

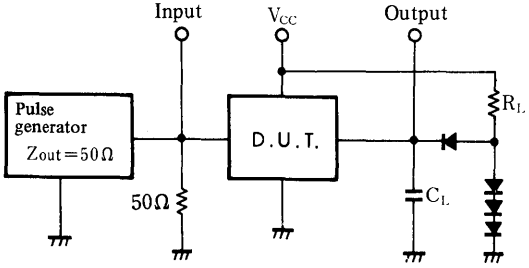
* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.
*** Measured with all outputs open and all inputs grounded.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Test conditions		Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	A or B	Other input = LOW	$C_L=15pF$ $R_L=2k\Omega$		12	23	ns
	t_{PHL}					10	17	
	t_{PLH}	A or B	Other input = HIGH			20	30	ns
	t_{PHL}					13	22	

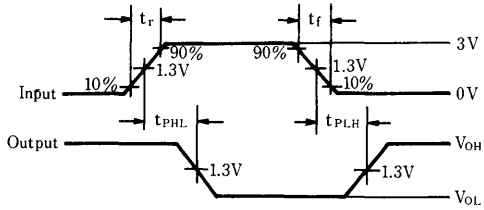
※ Switching parameter measurement information

1. Measurement circuit



Notes
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161 or equivalent.

2. Waveforms



Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.

DN74LS390

Dual Decade Counters

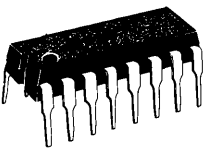
■ Description

DN74LS390 contains two asynchronous decade counter circuits with direct-coupled reset inputs.

■ Features

- Includes two circuits corresponding to LS90 and LS290 for high-density mounting
- Independent direct-coupled reset input for each circuit
- Capability for independent use as binary and quinary counter
- High-speed counting (f_{max} = 35MHz typical)
- Wide operating temperature range (Ta = –20 to +75°C)

P-2

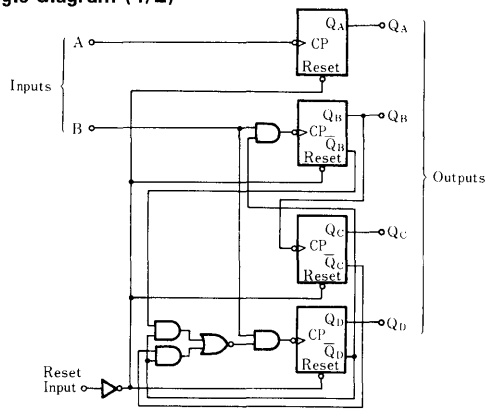


16-pin plastic DIL package

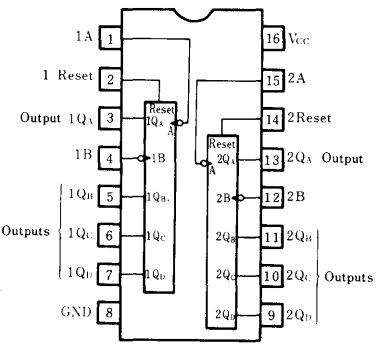
P-5

16-pin Panaflat package (SO-16D)

■ Logic diagram (1/2)



Pin configuration (top view)



■ Absolute maximum ratings

Parameter		Sym.	Rating		Unit
Input voltage	Reset	V_I	–0.5	7.0	V
	A, B		–0.5	5.5	

* Refer to the family ratings for other parameters.

■ Recommended operating conditions

Parameter		Sym	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}			–400	μA
		I_{OL}			8	mA
Operating temperature range		Topr	–20	25	75	℃
Count frequency	A input	f_{count}	0		25	MHz
	B input		0		20	MHz
Pulse width	A input	t_W	20			ns
	B input		40			ns
	Reset input		20			ns
Set-up time		t_{su}	25 ↓			ns

Note: ↓: Indicates fall edge of standard clock pulse.

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter		Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Output voltage		V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$ $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	3.4		V
		V_{OL1}	$V_{CC}=4.75V$ $V_{IH}=2V$ $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
		V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	Data, Enable, P	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				20	μA
	Load, Clock, Enable, T						100	μA
	Reset						200	μA
	Data, Enable, P	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.4	mA
	Load, Clock, Enable, T						−1.6	mA
	Reset						−2.4	mA
	Data, Enable, P	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.1	mA
	Load, Clock, Enable, T						0.2	mA
	Reset						0.4	mA
Output short circuit current**		I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−100	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current***		I_{CC}	$V_{CC}=5.25V$			15	26	mA

* When constant at V_{CC} = 5V, Ta = 25°C.

** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

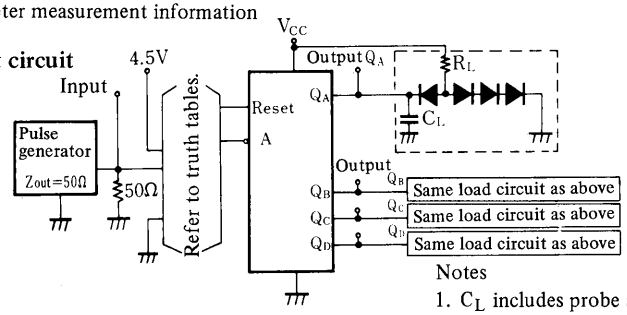
*** I_{CC} measured with all outputs open and all inputs except reset grounded; 4.5V applied momentarily applied to both reset terminals, following which they are grounded.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Maximum clock frequency	f_{max}	A	Q_A	$C_L=15pF$ $R_L=2k\Omega$	25	35		MHz
		B	Q_B		20	30		
Propagation delay time	t_{PLH}	A	Q_A			12	20	ns
	t_{PHL}					13	20	ns
	t_{PLH}	A	Q_C			37	60	ns
	t_{PHL}					39	60	ns
	t_{PLH}	B	Q_B			13	21	ns
	t_{PHL}					14	21	ns
	t_{PLH}	B	Q_C			24	39	ns
	t_{PHL}					26	39	ns
	t_{PLH}	B	Q_D			13	21	ns
	t_{PHL}					14	21	ns
	t_{PHL}	Reset	Any			24	39	ns

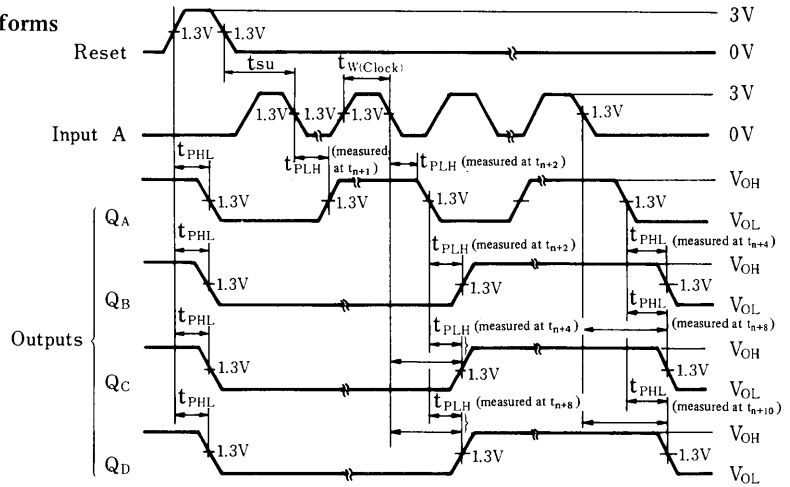
※ Switching parameter measurement information

1. Measurement circuit



Notes
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161.

2. Waveforms



Notes
1. Input waveform: $t_r \leqq 15$ns, $t_f \leqq 6$ns, PRR = 1MHz, duty cycle = 50%.
2. Pulse generator output impedance: Z_{out} = 50 ohms.
3. t_n is the bit time when all outputs are LOW.

■ Truth tables

1. BCD count sequence

Count	Outputs			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

Notes 1. H: HIGH voltage level.
2. L: LOW voltage level.
3. Output Q_A is connected to input B.

2. Bi-Quinary

Count	Outputs			
	Q_A	Q_B	Q_C	Q_D
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

Notes 1. H: HIGH voltage level.
2. L: LOW voltage level.
3. Output Q_D is connected to input A.

DN74LS393

Dual 4-bit Binary Counters

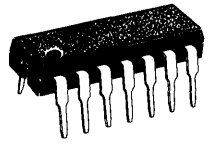
■ Description

DN74LS393 contains two asynchronous 4-bit binary (hexa-decimal) counter circuits with direct-coupled reset inputs.

■ Features

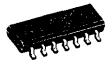
- Two circuits corresponding to LS93 and LS293 for high mounting density
- Independent direct-coupled reset inputs for each circuit
- High-speed counting (f_{max} = 35MHz typical)
- Wide operating temperature range (Ta = –20 to +75°C)

P-1



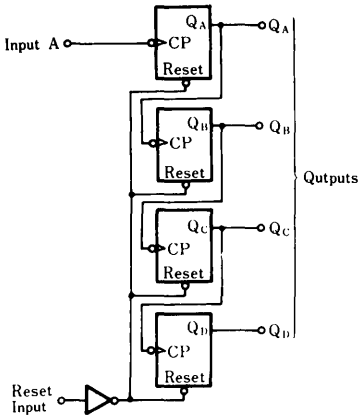
14-pin plastic DIL package

P-4

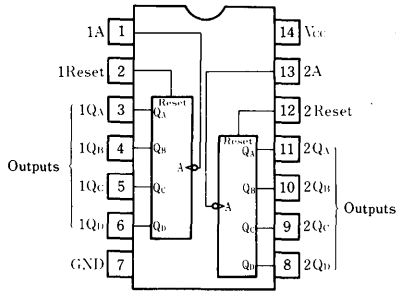


14-pin Panaflat package (SO-14D)

■ Logic diagram (1/2)



Pin configuration (top view)



■ Absolute maximum ratings

Parameter		Sym.	Rating		Unit
Input voltage	Reset	V_I	−0.5	7.0	V
	A, B		−0.5	5.5	

* Refer to the family ratings for other parameters.

■ Recommended operating conditions

Parameter		Sym	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}			−400	μA
		I_{OL}			8	mA
Operating temperature range		Topr	−20	25	75	℃
Count frequency	A input	f_{count}	0		25	MHz
Pulse width	A input High or Low	t_W	20			ns
	Reset High		20			
Set-up time		t_{su}	25↓			ns

Note: ↓: Indicates time from fall of clock.

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter		Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Output voltage		V_{OH}	$V_{CC}=4.75V$, $I_{OH}=-400\mu A$ $V_{IH}=2V$, $V_{IL}=0.8V$		2.7	3.4		V
		V_{OL}	$V_{CC}=4.75V$ $V_{IH}=2V$ $V_{IL}=2.7V$	$I_{OL}=4mA$		0.25	0.4	V
				$I_{OL}=8mA$		0.35	0.5	V
Input current	Reset	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				20	μA
	A input						100	μA
	Reset	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.4	mA
	A input						−1.6	mA
	Reset	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.1	mA
	A input						0.2	mA
Output short circuit current**		I_{OS}	$V_{CC}=5.25V$ $V_O=0V$		−15		−100	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current***		I_{CC}	$V_{CC}=5.25V$			15	26	mA

* When constant at V_{CC} = 5V, Ta = 25°C.

** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

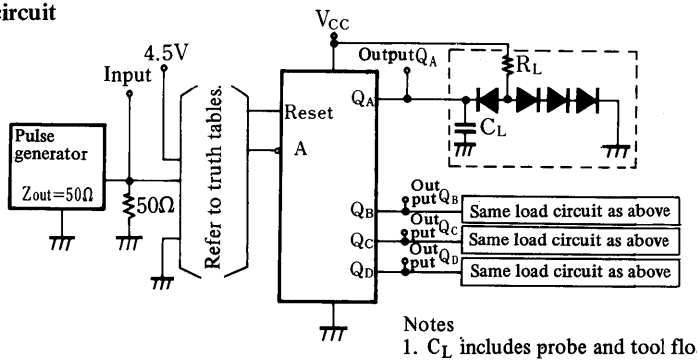
*** I_{CC} measured with all outputs open and all inputs except reset grounded; 4.5V applied momentarily to both reset terminals, following which they are grounded.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Maximum clock frequency	f_{clock}	A	Q_A	$C_L=15pF$ $R_L=400\Omega$	25	35		MHz
Propagation delay time	t_{PLH}	A	Q_A			12	20	ns
	t_{PHL}					13	20	ns
	t_{PLH}	A	Q_D			40	60	ns
	t_{PHL}					40	60	ns
	t_{PHL}	Reset	ony			24	39	ns

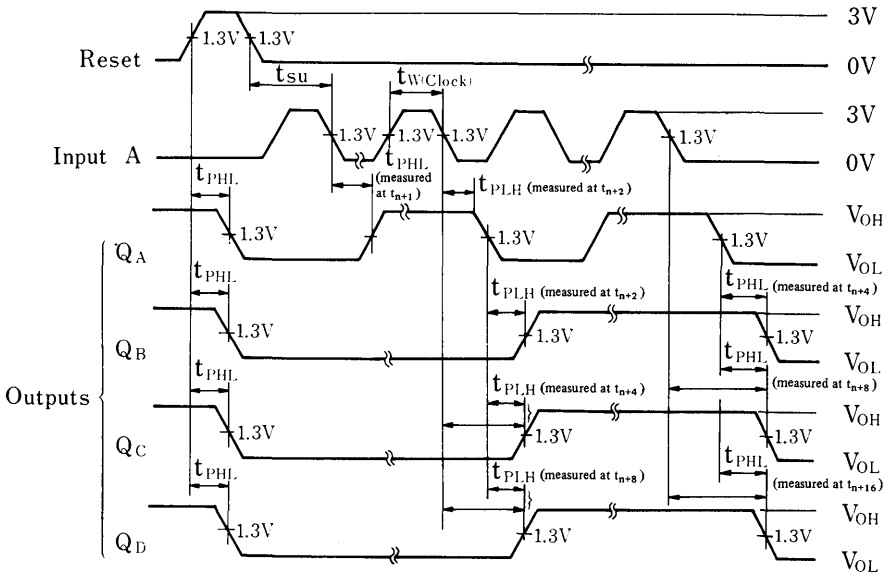
※ Switching parameter measurement information

1. Measurement circuit



Notes
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161 or equivalent.

2. Waveforms



Notes

1. Input waveform: $t_r \leqq 15$ns, $t_f \leqq 6$ns, PRR=1MHz, duty cycle 50%

■ Truth tables

Count sequence

Count	Outputs			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

Notes 1. H: HIGH voltage level.
2. L: LOW voltage level.

DN74LS395A

4-bit Cascadable Shift Registers (with 3-state Outputs)

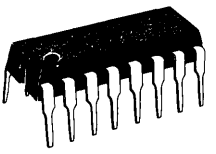
■ Description

DN74LS395A is a 4-bit serial/parallel input to serial/parallel output shift register with 3-state outputs.

■ Features

- Synchronous serial/parallel input to serial/parallel output
- Right shift
- Left shift capability with external connection
- Mode-control input
- Output-control input
- "Wired" AND capability for Q_A through Q_D (with 3-state outputs)
- Number of bits easily increased
- Wide operating temperature range (Ta = –20 to +75°C)

P-2

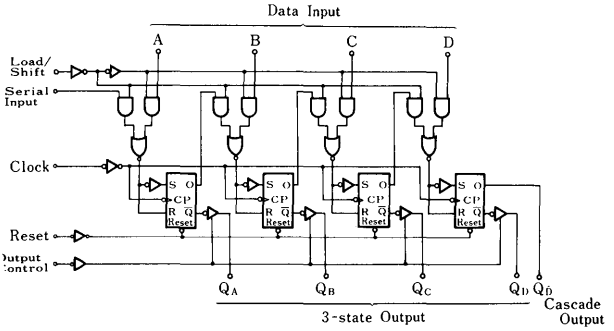


16-pin plastic DIL package

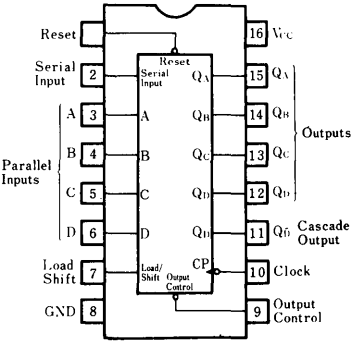
P-5

16-pin Panaflat package (SO-16D)

■ Logic diagram



Pin configuration (top view)



■ Recommended operating conditions

Parameter		Sym		Min	Typ	Max	Unit
Supply voltage		V_{CC}		4.75	5.00	5.25	V
Output current		I_{OH}	Q_A, Q_B, Q_C, Q_D			–2.6	mA
			$Q_{\bar{D}}$			–400	μA
Output current		I_{OL}	Q_A, Q_B, Q_C, Q_D			24	mA
			$Q_{\bar{D}}$			8	mA
Operating temperature range		Topr		–20	25	75	℃
Clock frequency		f_{clock}		0		25	MHz
Pulse width		$t_{W(CP)}$		16			ns
Set-up time	High-Level or Low-Level Data	t_{su}		20			ns
	Load / Shift Input			40			ns
Hold time		t_h		10			ns

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions			Min	Typ*	Max	Unit
Input voltage	V_{IH}				2			V
	V_{IL}						0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$ $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		Q_A, Q_B, Q_C, Q_D	2.4	3.1		V
				$Q_{\bar{D}}$	2.7	3.4		V
	V_{OL}	$V_{CC}=4.75V$ $V_{IL}=0.8V$ $V_{IH}=2V$	Q_A, Q_B Q_C, $Q_{\bar{D}}$	$I_{OL}=12mA$		0.25	0.4	V
				$I_{OL}=24mA$		0.35	0.5	V
			$Q_{\bar{D}}$	$I_{OL}=4mA$		0.25	0.4	V
				$I_{OL}=8mA$		0.35	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$					20	μA
	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$					−0.4	mA
	I_I	$V_{CC}=5.25V$, $V_I=7V$					0.1	mA
Output current	I_{OZH}	$V_{CC}=5.25V$, $V_{IH}=2V$ $V_O=2.7V$		Q_A, Q_B, Q_C, Q_D			20	μA
	I_{OZL}	$V_{CC}=5.25V$, $V_{IH}=2V$ $V_O=0.4V$		Q_A, Q_B, Q_C, Q_D			−20	μA
Output short circuit current**	I_{OS}	$V_{CC}=5.25V$		Q_A, Q_B, Q_C, Q_D	−15		−130	mA
				Q_D	−15		−100	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$, $I_I=-18mA$					−1.5	V
Supply current***	I_{CC}	$V_{CC}=5.25V$		Condition A		19	34	mA
				Condition B		19	31	mA

* When constant at V_{CC} = 5V, Ta = 25°C.

** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

*** I_{CC} is measured with all outputs open, 4.5V applied to all inputs, and the following conditions:

A: 4.5V is applied to output control inputs; 3V is added momentarily, following which they are grounded.

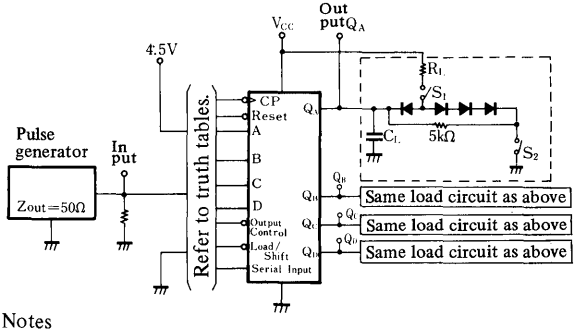
B: output control inputs and clock inputs are grounded.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Maximum clock frequency	f_{max}			Q_A, Q_B, Q_C, Q_D $R_L=667\Omega$ $C_L=45pF$ $Q_{\bar{D}}$ $R_L=667\Omega$ $C_L=15pF$	30	45		MHz
Propagation delay time	t_{PHL}	Clock	$Q_A \sim Q_D$, $Q_{\bar{D}}$			22	30	ns
	t_{PLH}					15	30	ns
	t_{PHL}	Reset	$Q_A \sim Q_D$, $Q_{\bar{D}}$			20	35	ns
Output enable time	t_{ZH}			$R_L=667\Omega$ $C_L=45pF$		15	25	ns
	t_{ZL}					17	25	ns
Output disable time	t_{HZ}			$R_L=667\Omega$ $C_L=5pF$		11	17	ns
	t_{LZ}					12	20	ns

※ Switching parameter measurement information

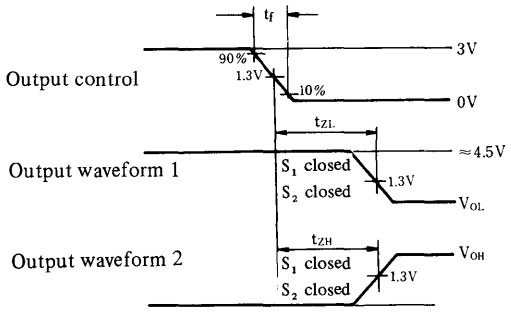
1. Measurement circuit



Notes
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161.

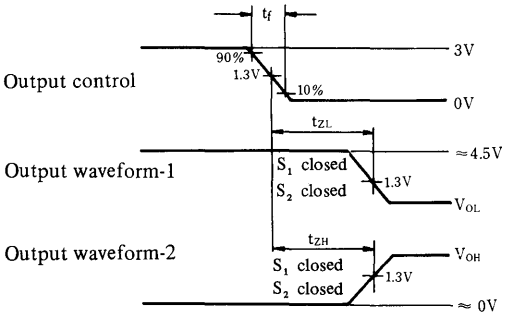
2. Waveforms

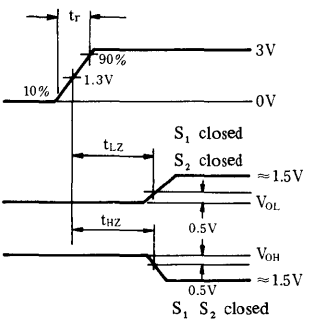
Waveforms-1



Notes
1. Reset and clock input waveforms: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz.

Waveforms-2





Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.
2. Except when the output is disabled by the output control, output waveform-1 occurs as a result of internal conditions such as a LOW voltage level.
3. Except when the output is disabled by the output control, output waveform-2 occurs as a result of internal conditions such as a HIGH voltage level.
4. When measuring t_{PLH} and t_{PHL}, S_1 and S_2 are closed.

■ Truth tables

Inputs								3-State Outputs				Cascade Outputs
Reset	Load/Shift Control	Clock	Serial	Parallel				Q_A	Q_B	Q_C	Q_D	$Q_{D'}$
				A	B	C	D					
L	×	×	×	×	×	×	×	L	L	L	L	L
H	H	H	×	×	×	×	×	Q_{Ao}	Q_{Bo}	Q_{Co}	Q_{Do}	Q_{Do}
H	H	↓	×	a	b	c	d	a	b	c	d	d
H	L	H	×	×	×	×	×	Q_{Ao}	Q_{Bo}	Q_{Co}	Q_{Do}	Q_{Do}
H	L	↓	H	×	×	×	×	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Cn}
H	L	↓	L	×	×	×	×	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Cn}

Notes
1. H: HIGH voltage level.
2. L: LOW voltage level.
3. ↓: Change from HIGH to LOW.
4. X: Either HIGH or LOW; doesn't matter.
5. a ~ d: Constant condition input level of inputs A through D.
6. Q_{Ao} ~ Q_{Do}: Levels of Q_A, Q_B, Q_C, and D_D prior to determination of input requirements shown in table.
7. Q_{An} ~ Q_{Dn}: Levels of Q_A, Q_B, and Q_C prior to nearest clock ↓ change.

DN74LS490

Dual 4-bit Decade Counters

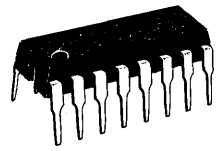
■ Description

DN74LS490 contains two asynchronous decade counter circuits with direct coupled reset input and nine direct-coupled set inputs.

■ Features

- Two circuits corresponding to LS90 and LS290 for high mounting density
- Independent direct-coupled reset input and nine direct-coupled set inputs for each circuit
- High-speed counting (f_{max} = 35MHz typical)
- Wide operating temperature range (Ta = −20 to +75°C).

P-2



16-pin plastic DIL package

P-5

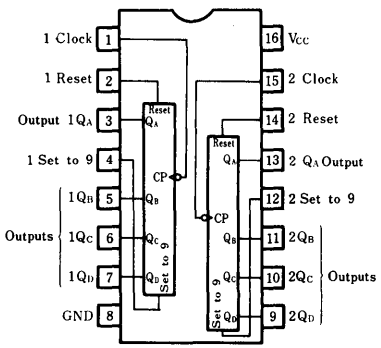
16-pin Panaflat package (SO-16D)

■ Absolute maximum ratings

Parameter		Sym.	Rating		Unit
Input voltage	Reset Set to 9	V_I	−0.5	7.0	V
	Clock		−0.5	5.5	

* Refer to the family ratings for other parameters.

Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−400	μA
Output current	I_{OL}			8	mA
Operating temperature range	Topr	−20	25	75	℃
Count frequency	f_{count}	0		25	MHz
Pulse width	t_W	20			ns
Set or set-to-9 set-up time	t_{su}	25↓			ns

Note: ↓: Indicates time from fall of clock.

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter		Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Output voltage		V_{OH}	$V_{CC}=4.75V$, $I_{OH}=-400\mu A$ $V_{IH}=2V$, $V_{IL}=0.8V$		2.7	3.4		V
		V_{OL}	$V_{CC}=4.75V$ $V_{IH}=2V$ $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
				$I_{OL}=8mA$		0.35	0.5	V
Input current	Reset, Set-to-9	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				20	μA
	Clock						100	μA
	Reset, Set-to-9	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.4	mA
	Clock						−1.6	mA
	Reset, Set-to-9	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.1	mA
	Clock						0.2	mA
Output short circuit current**		I_{OS}	$V_{CC}=5.25V$ $V_O=0V$		−15		−100	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current***		I_{CC}	$V_{CC}=5.25V$			15	26	mA

* When constant at V_{CC} = 5V, Ta = 25°C.

** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

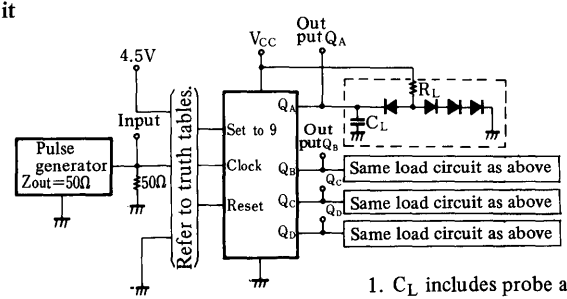
*** I_{CC} measured with all outputs open and all inputs except reset grounded; 4.5V applied momentarily to both reset terminals, following which they are grounded.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Maximum clock frequency	f_{max}	Clock	Q_A	$C_L=15pF$ $R_L=2k\Omega$	25	35		MHz
Propagation delay time	t_{PLH}	Clock	Q_A			12	20	ns
	t_{PHL}					13	20	ns
	t_{PLH}	Clock	Q_B, Q_D			24	39	ns
	t_{PHL}					26	39	ns
	t_{PLH}	Clock	Q_C			32	54	ns
	t_{PHL}					36	54	ns
	t_{PHL}	Reset	Any			24	39	ns
	t_{PLH}	Set-to-9	Q_A, Q_D			24	39	ns
	t_{PHL}		Q_B, Q_C			20	36	ns

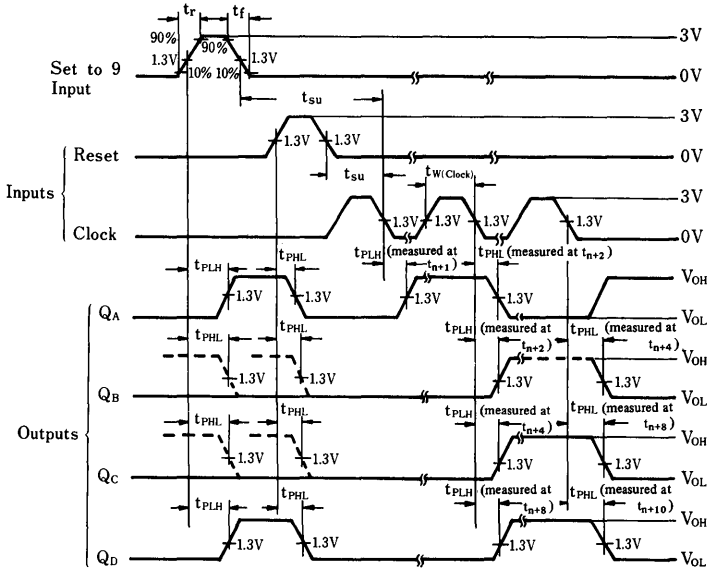
※ Switching parameter measurement information

1. Measurement circuit



1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161 or equivalent.

2. Waveforms



Notes

1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.
2. When measuring f_{max}, t_r and $t_f \leqq 2.5ns$.
3. t_n is the bit time when all outputs are LOW.

■ Truth tables

○ BCD Count sequence

Count	Outputs			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

Notes 1. H: HIGH voltage level.
2. L: LOW voltage level.

○ Reset / Set to 9

Inputs		Outputs			
Reset	Set to 9	Q_A	Q_B	Q_C	Q_D
H	L	L	L	L	L
L	H	H	L	L	H
L	L	Count			

Notes 1. H: HIGH voltage level.
2. L: LOW voltage level.

New Product Information

Number	Function	PIN
DN74LS126	Quad Bus Buffer Gates (with 3-state Output)	14
△DN74LS154	4-line to 16-line Decoders/Demultiplexers	24
DN74LS165	Parallel Load 8-bit Shift Registers	16
DN74LS166	8-bit Shift Registers	16
△DN74LS181	Arithmetic Logic Units/Function Generators	24
DN74LS242	Quad Bus Transceivers (with 3-state Output)	14
DN74LS243	Quad Bus Transceivers (with 3-state Output)	14
DN74LS247	BCD-to-7-segment Decoders/Drivers (with Open Collector Output)	16
DN74LS248	BCD-to-7-segment Decoders/Drivers	16
DN74LS249	BCD-to-7-segment Decoders/Drivers (with Open Collector Output)	16
△DN74LS259	8-bit Addresable Latches	16
△DN74LS261	2-bit by 4-bit Paralell Binaly Multiplexers	16
DN74LS273	Octal D-type Flip-Flop (with Reset)	20
△DN74LS280	9-bit Odd/Even Parity Generators/Checkers	14
△DN74LS295B	4-bit Right-Shift Left-Shift Registers (with 3-state Output)	14
△DN74LS298	Quad 2-input Multiplexers (with Storage)	16
△DN74LS352	Dual 4-line to 1-line Data Selectors/Multiplexers	16
DN74LS363	Octal Transparent Latces (with 3-state Output)	20
△DN74LS364	Octal D-type Flip-Flops (with 3-state Output)	20
△DN74LS374	Octal D-type Edge-Triggered Flip-Flops (with 3-state Output)	20
△DN74LS375	4-bit Bistable Latches	16
DN74LS377	Octal D-type Flip-Flops (with Enable)	20
DN74LS378	Hex D-type Flips (with Enable)	16
△DN74LS445	BCD to Decimal Decoders /Drivers	16
DN74LS640	Octal Bus Transceivers (with 3-state Output)	20
△DN74LS642	Octal Bus Transceivers (with Open Collector Output)	20
△DN74LS645	Octal Bus Transceivers (with 3-state Output)	20
△DN74LS670	4-by-4 Register Files (with 3-state Output)	16
△DN74LS673	16-bit Shift Registers	24

△ Under development

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