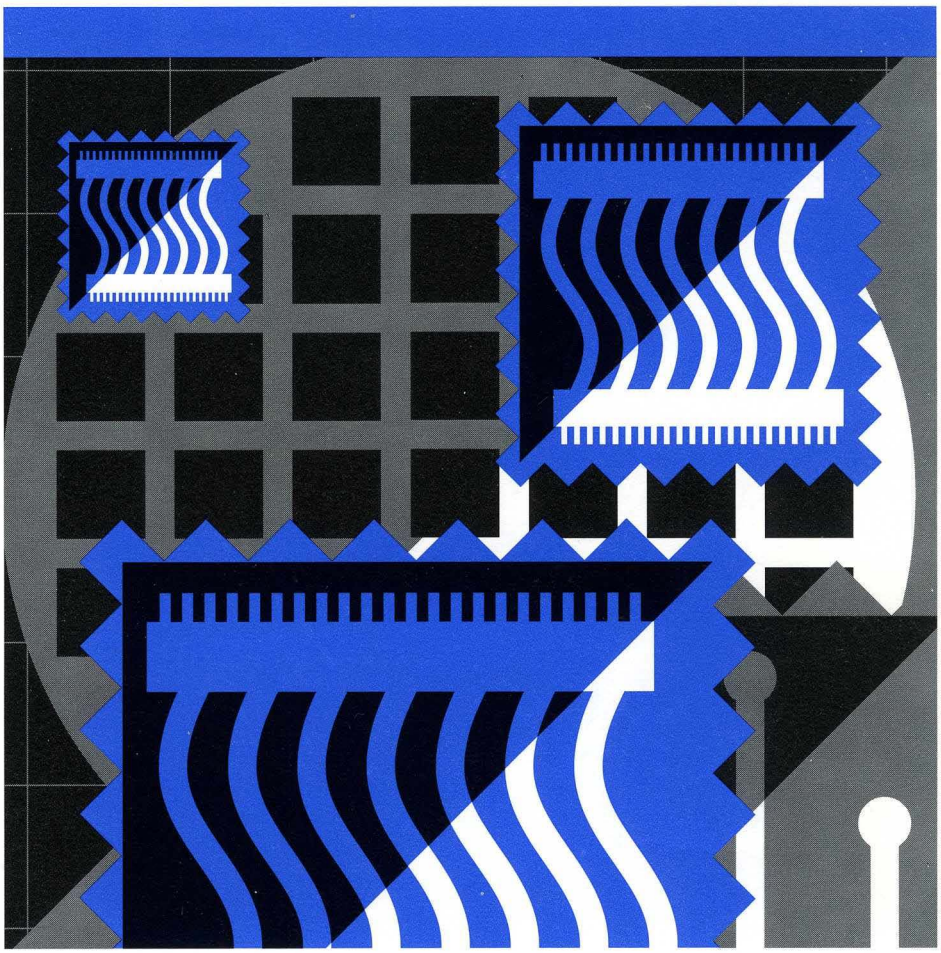
NCR 53CF90A, 53CF90B
SCSI I/O Processors

NCR



Data Manual

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Preface

SCSI Specifications

This manual assumes some prior knowledge of current and proposed SCSI standards. For background information, please contact:

ANSI
11 West 42nd Street
New York, NY 10036
(212) 642-4900
Ask for document number X3.131-1986 (SCSI-1)

Global Engineering Documents
2805 McGaw
Irvine, CA 92714
(800)-854-7179 or (714) 261-1455
Ask for document number X3.131-199X (SCSI-2)

ENDL Publications
14426 Black Walnut Court
Saratoga, CA 95070
(408) 867-6642
Document names: *SCSI Bench Reference, SCSI Encyclopedia*

Prentice Hall
Englewood Cliffs, NJ 07632
(201) 767-5937
Ask for document number ISBN 0-13-796855-8, *SCSI: Understanding the Small Computer System Interface*

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Chapter One
Introduction

General Description

The NCR 53CF90A and 53CF90B Fast SCSI Controllers (FSC) are high performance CMOS devices designed to maximize SCSI transfer rates. They are pin, function, and software-compatible with the NCR 53C90A and 53C90B Advanced SCSI Controllers, and conform to ANSI standards X3.131-1986 (SCSI-1) and X3.131-199X (SCSI-2).

Both chips include all the functionality of the 53C90A and 53C90B, plus additional features including Fast SCSI. The 53CF90B includes all the functionality of the 53CF90A, plus pass through parity. Both are software-compatible with the industry standard 53C90 family.

The 53CF90A and 53CF90B are second generation SCSI controllers that reduce protocol overhead by automating critical SCSI sequences in hardware. They will operate at sustained asynchronous data transfer rates up to 7 megabytes per second (MB/s), and fast synchronous data transfer rates of 10 MB/s using a 40 MHz clock. The normal SCSI-1 transfer rate of 5 MB/s is also supported.

The FSC has on-chip 48 mA drivers for single-ended transmission, allowing direct connection to the SCSI bus, which minimizes board space requirements. Differential mode is also provided to allow for data transfers over longer distances. The FSC operates in Initiator and Target modes, and can therefore be used in both host adapter and peripheral applications.

Both chips are packaged in a 68-pin PLCC and an 80-pin PQFP.

Independent of microprocessor intervention, the FSC performs arbitration, selection, or reselection. It also independently handles message, command, status, and data transfer between the SCSI bus and the chip's 16-byte internal FIFO, or a buffer memory.

FSC Features Summary

- SCSI-2 compatible
- Up to 10 MB/s sustained synchronous SCSI transfer rate
- Up to 7 MB/s sustained asynchronous SCSI transfer rate
- Up to 13.3 MB/s DMA burst transfer rate (FASTCLK enabled)
- Up to 12 MB/s DMA burst transfer rate (FASTCLK disabled)
- 24-bit transfer counter eliminates inter-sector transfer delays and allows single transfers up to 16 MB
- Part unique ID code
- Differential mode selection
- Active negation in differential mode for REQO/ and ACKO/
- Differential SCSI bus I/O delay
- On-chip 48 mA single-ended drivers and receivers
- SCSI-2 tagged-queuing compatible
- 16-byte FIFO
- Supports clock frequencies from 10-40 MHz
- Software compatible with the 53C90 family
- High performance CMOS technology
- 68-pin PLCC and 80-pin PQFP

Figure 1-1. NCR 53CF90A, 53CF90B Block Diagram

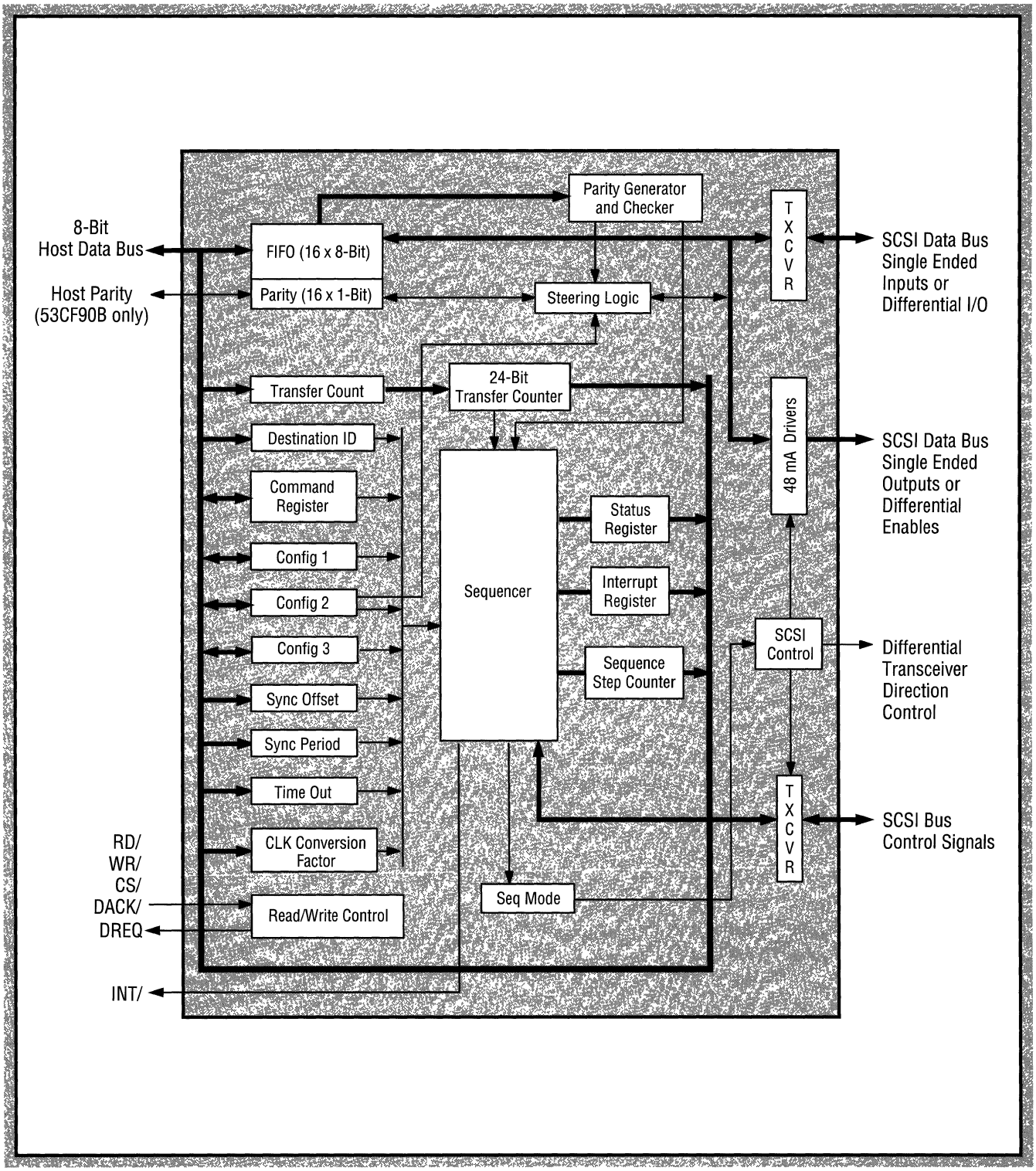
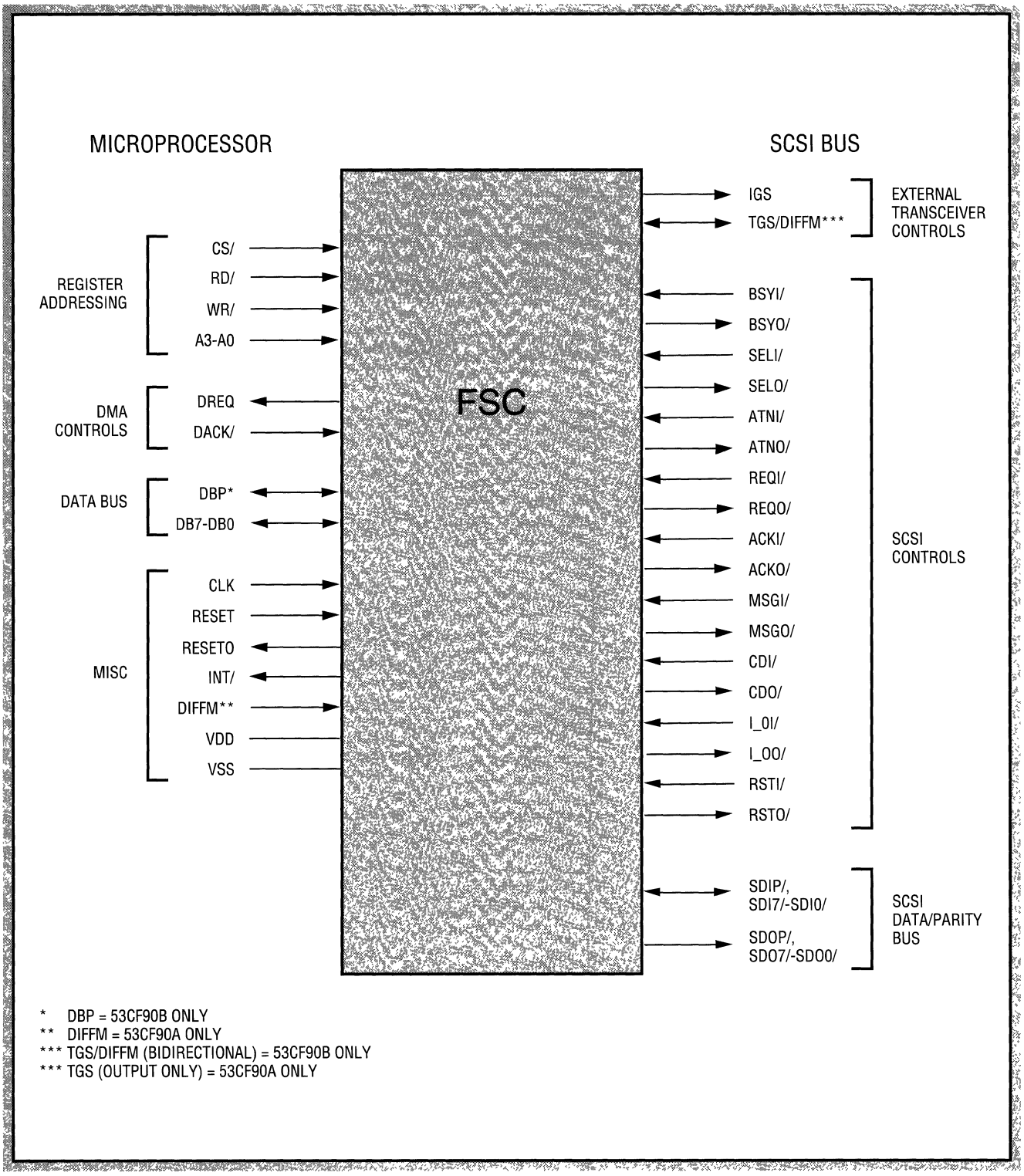


Figure 1-2. NCR 53CF90A, 53CF90B Functional Signal Grouping



Chapter Two
Functional Description

The Fast SCSI Controller (FSC) has a command set that allows it to perform common SCSI sequences at hardware speed without host intervention. Its on-chip FIFO may be accessed simultaneously by the SCSI bus and either the microprocessor or the host DMA controller. All command, data, status and message bytes pass through the FIFO on the way to or from the SCSI bus.

Most FSC commands have two versions: DMA and non-DMA. When DMA instructions are used, data will pass between memory and the SCSI bus with the FIFO acting as temporary storage when the DMA channel is temporarily shut down by a higher priority event, such as DRAM refresh.The FIFO also helps speed execution during non-DMA transfers. For example, in initiator role, the microprocessor will load the Command Descriptor Block (CDB) and optionally, one or three message bytes into the FIFO. It will then issue one of several selection commands and wait for an interrupt. The FSC will wait for bus free, arbitrate for the bus until it acquires it, send the message bytes followed by the CDB, then generate an interrupt. Meanwhile, a multi-tasking host may continue with other tasks.

An 8-bit part unique ID code for the FSC is available in the Transfer Counter High register (at address 0Eh). This ID can be used to differentiate a slow SCSI device from a fast SCSI device.

Typical SCSI Operation

With the FSC in target role, the microprocessor enables selection and waits for an interrupt. Eventually an initiator selects the FSC, which then automatically steps through the selection and command phases before generating an interrupt to the microprocessor. When the interrupt occurs, the entire CDB will be in the FIFO along with any message bytes sent by the initiator.

After the selection phase has been successfully completed, the FSC may transfer bytes in any SCSI information phase whether it is operating in initiator or target role. The FSC supports disconnect/reselect in both initiator and target roles, making it easy to implement high performance multi-threaded systems.

The FSC may transfer data phase bytes across the bus synchronously, at speeds up to 10 MB/s, or asynchronously, at speeds up to 7 MB/s. Refer to the *Data Transfer Rate* section in this chapter for more information. The difference between asynchronous and synchronous operation is transparent to the user except that the Synchronous Offset and the Synchronous Transfer Period registers (at addresses 06h and 07h) must be programmed prior to synchronous data transfer. The default, after hardware or software reset, is asynchronous transmission.

Data bytes will usually be transferred using DMA. The microprocessor will program an external DMA controller, program the FSC Transfer Count registers (00h, 01h, and 0Eh), issue one of

several FSC data transfer commands, then wait for an interrupt. The DMA controller and the FSC will transfer all the data without microprocessor intervention.

To end the SCSI transaction, the FSC target will place a status byte and a message byte in the FIFO. It will then issue one of two single commands which will cause the FSC to first assert Status phase, send the first byte, assert Message In phase, send the second byte, disconnect from the SCSI bus (after the initiator releases ACK) and interrupt the microprocessor.

The end of a SCSI transaction is similar for an FSC initiator except that it receives two bytes into its FIFO. The FSC prevents the target from disconnecting by holding ACK asserted on the bus while the microprocessor examines the status and message bytes. If both bytes are acceptable, the Message Accepted command is used to instruct the FSC to release ACK, which allows the target to disconnect and causes the FSC to interrupt its host and report the disconnect. If the status and message bytes are not acceptable, the host could first issue the Set Attention (ATN) command before issuing the Message Accepted command. This instructs the FSC to assert ATN before releasing ACK, which should cause the target to request Message Out phase rather than disconnect.

Bus Initiated Sequences

- Selection
- Reselection
- SCSI bus reset

Selection or reselection sequences occur in the disconnected state when the FSC is selected or reselected by another initiator or target, if the Enable Selection or Reselection command has previously been issued to the FSC.

In addition to responding to bus initiated events, the FSC may initiate a bus event by using one of several selection or reselection commands. If one of these commands starts executing, the Enable Selection or Reselection command will be cleared after arbitration has been won, preventing the FSC from responding to a Select or Reselect command. Normally the microprocessor will have 250 ms (ANSI recommended selection time-out period) after the chip disconnects from the bus to re-enable bus initiated events. If the time-out period is exceeded, an initiator or target attempting to connect to the FSC may time-out and abort.

If, on the other hand, the bus initiated event occurs before the command starts executing, the FIFO and Command registers (02h and 03h) will be cleared and any further writes by the microprocessor will be ignored until the Interrupt register (05h) is read. Since a selection or reselection command requires that something be placed in the FIFO, these bytes will be lost, as will any command written to the Command register. The interrupt handler that services a selection or reselection command will have to examine the bits in the Interrupt register to determine if the FSC selected another device, or if it was selected by another device. The former case will cause a Function Complete interrupt, the latter case will cause a Selection or Reselection interrupt.

Bus Initiated Selection

When the FSC has been selected as a target, the following data will be in its FIFO:

- Bus ID
- Identify message
- Optional two-byte command queuing message
- Command Descriptor Block (CDB)

The bus ID will always be present and will always be one byte. It is an unencoded version of the state of the bus during Selection phase. Any SCSI data bits that were true during Selection phase will be set. The target ID must always be set. In arbitrating systems, the initiator ID must also be set. The initiator ID is optional in non-arbitrating systems. If parity checking is enabled, parity must be valid during the bus initiated selection. If parity is not valid, the FSC will not respond to bus initiated selection.

The identify message, if sent, will also be placed in the FIFO. The identify message is optional in SCSI-1 systems but will always be one byte if it is used. In SCSI-2 systems a one or three byte message will be sent, consisting of the one-byte identify message and an optional two-byte command queuing message. If the identify message is not sent, the FSC places a null byte (00h) into the second FIFO element, behind the bus ID. If the FSC is selected with ATN deasserted, it will store a null byte in the FIFO behind the bus ID, then begin requesting command phase bytes. A detected parity error will cause the FSC to interrupt and stop, if parity checking is enabled.

If the FSC is selected with ATN asserted and the SCSI-2 bit (bit 3, Configuration 2 register) is not set, it will request one message byte and place it in the FIFO behind the bus ID. It then requests Command phase bytes unless the message byte is not a valid identify message, or a parity error is detected, which will cause the FSC to interrupt and stop. The Sequence Step register (06h) can then be examined to determine what events have been completed.

If the FSC is selected with ATN asserted and the SCSI-2 bit is set, the FSC will examine both the message byte and the ATN signal to determine how many bytes to request. If the first byte is a valid identify message and if ATN is deasserted after receiving the first byte, the FSC will change to Command phase. If the first byte is a valid identify message byte and ATN is still asserted, it will request two more message bytes. After requesting the message bytes, the FSC requests Command phase bytes unless one of the following situations occurs:

1) The first byte is not a valid identify message
2) A parity error is detected
3) ATN is deasserted between the second and third bytes
4) ATN remains asserted but the SCSI-2 bit is false.

All of these conditions cause the FSC to interrupt and stop.

To determine if one of the above situations has occurred, examine the Sequence Step register (06h).

The CDB will always begin at the third or fifth byte in the FIFO, assuming selection completed normally. The CDB may be 6, 10 or 12 bytes long. Thus, in SCSI-2, the entire FIFO may be filled if a tagged-queuing 12-byte command is used.

Bus Initiated Reselection

The FSC will allow itself to be reselected as an initiator by a target if it has previously received the Enable Selection/Reselection command. If the sequence completes normally, the following information will be in the FIFO:

- Bus ID
- Identify message
- Optional 2-byte queue tag message

The bus ID will always be present and will always be one byte. It is an unencoded version of the state of the bus during Reselection phase.

The identify message will always be present and will always be one byte.

If queue tagging is enabled, and the target is sending a queue tag message, the target will send two queue tag message bytes which will also be in the FIFO.

Bus Initiated Reset

A SCSI bus initiated reset will be recognized by the FSC at any time. When SCSI RST/ pulses true, the FSC will disconnect from the bus and reset its internal sequencer. If the SCSI Reset Reporting Interrupt bit (bit 6 in the Configuration l register) is not set, the FSC will generate a SCSI reset detected interrupt.

Parity Checking and Generation

The FSC has six bits that control parity generation and checking. These bits are listed in Table 2-1. If parity checking is disabled, the FSC does not check for parity errors. In this document, the word *detected* in conjunction with *parity error* should be understood to imply that parity checking has previously been enabled.

Table 2-1. Parity Control Bits

Register	Bit	Bit Name
Configuration 1 (08h)	4	Enable Parity Checking
Configuration 1 (08)	5	Parity Test Mode
Status (04h)	5	Parity Error
Configuration 2 (0Bh)	0	DMA Parity Enable (53CF90B only)
Configuration 2 (0Bh)	1	Register Parity Enable (53CF90B 0nly)
Configuration 2 (0Bh)	2	Target Bad Parity Abort

Parity From the SCSI Bus

The Enable Parity Checking bit (bit 4, Configuration 1 register) enables parity checking on bytes received from the SCSI bus. When this bit is set, the FSC checks parity on incoming SCSI bytes during any Information Transfer phase, except when receiving pad bytes. The 53CF90B (only) passes parity from the SCSI bus to buffer memory. If the FSC detects a parity error, the Parity Error bit (bit 5, Status register) is set, but no interrupt is generated. If the chip is in Initiator mode, ATN is asserted on the SCSI bus.

When the Enable Parity Checking bit is reset to zero, parity on bytes received from the SCSI bus is not checked and the FSC generates parity for each byte received.

Table 2-2. Parity From the SCSI Bus

Configuration 1 Register Parity Checking (Bit 4)	Parity Pass-Through (53CF90B Only) Register Access	Parity Pass-Through (53CF90B Only) DMA Access	Parity Check (SCSI to FIFO)
0	No	No	No
1	Yes	Yes	Yes

Target Bad Parity Abort

The Target Bad Parity Abort bit (bit 2, in the Configuration 2 register), allows special handling of parity errors. When this bit is set, the chip will abort a Receive command or Receive Data command if bad parity is received from the SCSI bus. If a parity error occurs when the Target Bad Parity Abort bit is set, the Parity Error bit (bit 5, Status register) will be set, but no additional bits will be set in the Interrupt or Status registers (05h and 04h) after bad parity is detected. The Transfer Counter registers (00h, 001h, 0Eh) and FIFO Flags register (07h) contain a record of how many bytes were transferred before the command was aborted.

Parity to the SCSI Bus (53CF90B Only)

Parity checking on bytes passed through the 53CF90B from buffer memory to the SCSI bus is controlled by the Register Parity Enable bit and the DMA Parity Enable bit (bits 1 and 0 in the Configuration 2 register).

When the Register Parity Enable bit is set, the DBP pin (53CF90B only) is loaded into the FIFO during register writes to the FIFO. Parity may then pass between the SCSI and host buses without change.

If the Register Parity Enable bit is not set, the 53CF90B generates parity for bytes received during register writes to the FIFO. The parity bit is always loaded into the FIFO along with the data byte. After that, it moves through the FIFO along with the data byte. Parity errors are flagged if the DMA Parity Enable bit is set.

When the DMA Parity Enable bit is set, parity from the DBP pin (53CF90B only) is loaded into the FIFO during DMA writes to the FIFO. The parity is checked and passed to the SCSI bus along with the data bytes. If a parity error is detected, the Parity Error bit (bit 5 in the Status register) is set, but no interrupt is generated.

When the DMA Parity Enable bit is not set, the 53CF90B generates parity for bytes received from buffer memory during DMA writes to the FIFO. The bit is loaded into the FIFO along with the data bytes, and passed to the SCSI bus with the data bytes. Parity errors are flagged if the Register Parity Enable bit is set.

Table 2-3. Parity to the SCSI Bus (53CF90B Only)

Configuration 2 Register		Parity Pass-Through		
Register Parity (BIT 1)	DMA Parity (Bit 0)	Register Access	DMA Access	Parity Check (FIFO to SCSI)
0	0	No	No	No
0	1	No	Yes	Yes
1	0	Yes	No	Yes
1	1	Yes	Yes	Yes

Parity Test Mode

The Parity Test Mode bit (bit 5, Configuration 1 register) is used to create parity errors for system debug purposes. Setting this bit causes the parity output to the SCSI bus to be read from bit 7 of the transmitted byte, rather than from the parity bit. This facilitates system debug by allowing the microprocessor to force bad parity on any byte. This bit must not be enabled in normal operation.

DMA Operation

The FSC generates DMA cycles to the buffer memory to move data between the buffer memory and the SCSI bus via the FIFO. A cycle is generated when any one of the following three conditions is true:

- Receiving from buffer memory
  AND the top FIFO cell not full
  AND the Transfer Counter is not zero
- Transmitting to buffer memory
  AND the bottom FIFO cell is full
  AND not Initiator Synchronous Data In
- Transmitting to buffer memory
  AND the bottom FIFO cell is full
  AND Initiator Synchronous Data In
  AND the Transfer Counter is not zero

Data Transfer Rate

Performance numbers for the FSC are based on single-ended connection to the SCSI bus with no external transceivers. In a differential system, external transceivers are required. This will slow asynchronous transmission by the propagation delay of the chosen transceiver, but will not slow synchronous transmission.

Asynchronous Operation

The asynchronous transmission rate will vary with cable length and the CLK period. The FSC can reach sustained transfer rates of 7 MB/s on short (one foot) cables using typical devices operating at or near nominal voltage and temperature. The typical transfer rate on a six meter cable is 4 MB/s using two typical FSCs talking to each other. The worst case asynchronous transmission rate, over voltage, temperature, and process variations is 3 MB/s on a maximum length (six meters), single-ended cable and 4 MB/s on a one foot cable.

The asynchronous transmission rate is only slightly affected by the CLK frequency when sending data. The FSC will drive the data bus for a minimum of one CLK period (plus any additional time required to meet the ANSI required 55 ns setup time) before asserting REQ or ACK. The CLK frequency does not affect the asynchronous transfer rate when receiving data.

Synchronous Operation

The synchronous data transmission period is equal to the CLK input frequency multiplied by the encoded value in the Synchronous Transfer Period register (06h). Sustained synchronous transfer rates of 10 MB/s are attainable across the commercial voltage and temperature range.

The FSC can transfer synchronous SCSI data in both initiator and target modes at transfer rates up to 10 MB/s, using an input clock frequency of 40 MHz. The SCSI-1 and Fast SCSI-2 minimum timing requirements are listed below:

Mode	Setup	Hold	Assert/Negate
SCSI-1	55 ns	100 ns	90 ns
Single-ended Fast SCSI-2	25 ns	35 ns	30 ns
Differential Fast SCSI-2	35 ns	45 ns	30 ns

To support maximum Fast SCSI transfer rates and SCSI-1 transfer requirements, the FASTSCSI (bit 1) and FASTCLK (bit 0) bits have been added to the Configuration 3 register (0Ch). They modify the SCSI state machine to provide fast and normal synchronous timings depending upon the clock frequency. Full description of the operations of these bits and the required clock frequencies are provided in the Configuration 3 register description in Chapter Four, *Registers*.

During synchronous SCSI transfers, the assertion and deassertion of the REQ and ACK signals are programmable using the FASTCLK bit and other bits in the Synchronous Offset register (07h). The input clock duty cycle affects the half clock assertion/deassertion delays. For more information, see the Synchronous Offset register description in Chapter Four, *Registers*.

Note: DMA must be used for synchronous transfers.

SCSI Modes

SCSI single-ended and differential modes of operation are selected by the DIFFM pin.

Note: The 53CF90B has an internal pullup for the TGS/DIFFM pin to place it in single-ended mode, but requires an external 1 K pulldown to place it in differential mode. For the 53CF90A, a high signal on the DIFFM pin selects differential mode and a low selects single-ended mode.

Single-Ended Mode

In single-ended mode, the SCSI input pins are externally connected to their corresponding output pins, forming bi-directional connections to the SCSI bus. The IGS and TGS signals are not used. Appendix C contains a wiring diagram showing connections between the FSC and the SCSI bus in single-ended mode.

Two termination methods for single-ended mode are described in the ANSI SCSI-2 specification. Alternative 1 reflects the SCSI-1 specification, with 220 ohms to the TERMPWR line and 330 ohms to ground. To improve noise margins, 1% resistors should be used and TERMPWR should be between 5.0 V and 5.25 V.

Alternative 2 reflects the SCSI-2 specification, and is the recommended termination method. An adjustable voltage regulator, powered by TERMPWR, supplies 2.85 V to 110 ohm 1% resistors. This more accurately matches the characteristic impedance of the cable, resulting in better signal quality. Integrated versions from multiple vendors are also available.

Differential Mode

In differential mode, the SDI7/-0/ and SDIP/ pins carry bidirectional data and the SDO7/-0/ and SDOP/ pins configure the direction of the external transceivers. Appendix C contains a wiring diagram showing connections between the FSC and the SCSI bus in differential mode.

During arbitration and selection, the FSC drives the SCSI data output lines with the appropriate ID bit set, which sets the direction of the selected differential transceiver to out. The other transceivers are configured for input, allowing the FSC to determine if it has won arbitration. During information transfers, the output lines are driven either all high or all low to configure the transceivers for output or input respectively.

All other SCSI bus signals have separate input and output pins. The direction of the transceivers for ATN/ and ACK/ is selected by the IGS signal (in initiator mode). The direction of the transceivers for REQ/, MSG/, C_D/, and I_O/ is selected by the TGS signal (in target mode). The direction of the transceivers for BSY/, SEL/, and RST/ is enabled by BSYO/, SELO/, and RSTO/ respectively.

Pullups must be used for all signals except REQO/ and ACKO/. Pullups should not be used on the REQO/ and ACKO/ pins in differential mode because, in this mode, an internal totem-pole driver is enabled.

Differential SCSI Bus Delay

When the Features Enable bit (bit 6 in the Configuration 2 register) is set, the FSC delays the SCSI bus input or output enable signals from becoming active for two to three clock cycles after the chip stops driving the SCSI data lines. With a 40 MHz clock, this provides a minimum 50 ns turn off time for the external transceivers. This delay prevents bus contention between the FSC and the transceivers when the SCSI bus changes direction.

When the SCSI bus changes direction from input to output, this feature delays the output on the SDIP/ and SDI7/-0/ lines, giving the SDOP/ and SDO7/-0/ lines time to reverse direction on the differential drivers.

When the SCSI bus changes direction from output to input, this feature delays the output on the SDIP and SDO7/-0/ lines, giving the SDIP/ and SDI7/-0/ lines time to reverse direction.

Chip Reset

The FSC has the following three levels of reset: Hard, Soft, and Disconnect.

Hard Reset

A hard reset is executed at power up, when using the Reset Chip command, or when the RESET pin is asserted by external hardware. It stops all chip operations, resets all functions in the chip, and returns the chip to a disconnected state. The Reset Chip command remains at the top of the Command register (03h) FIFO, which locks the chip and all registers in a reset state until a NOP command is issued.

Soft Reset

A soft reset is applied when the SCSI bus reset condition is received through the RSTI/ pin, or when the Reset SCSI Bus command is issued, which asserts the RSTO/ pin. This condition resets the following subset of the functions reset by the hard reset:

- Resets DMA interface
- Resets bus-initiated selection/reselection module
- Resets command sequence module
- Resets Sequence Step and clears Sequencer Mode bits (Enable Select/Reselect = 0, Target = 0, Initiator = 0)
- Initializes Command register FIFO to empty
- Releases all SCSI signals except RSTO/
- Resets disconnect, initiator, and target command modules

The Reset SCSI Bus command will cause the RSTO/ signal to be asserted. When an external device on the bus responds, the RSTI/ signal will also be asserted. See Chapter Five, *Command Set*, for further description of this command.

A SCSI bus reset may occur in any mode. The RSTI/ signal is asserted by another SCSI device on the bus, and returns the chip to a disconnected state. The chip generates a SCSI reset interrupt to the microprocessor if the interrupt is not disabled by bit 6 of the Configuration 1 register (08h). If the SCSI bus reset is still active when the microprocessor clears the interrupt, a new interrupt is generated. This new interrupt must be serviced.

The Reset SCSI Bus command asserts the SCSI RSTO/ pin for approximately 25 µs and returns the chip to disconnected status. No interrupt is generated when the command is completed. However, if the RSTI/ pin is externally connected to the RSTO/ pin, a SCSI reset interrupt is generated if the interrupt is not disabled by Bit 6 of the Configuration 1 register (08h).

Disconnect Reset

The disconnect reset is caused by various circumstances that result in the chip becoming disconnected from the SCSI bus, as described below:

- The Target Mode Disconnect, Disconnect Sequence, or Terminate Sequence command is issued to the chip.
- The chip is in initiator mode and the SCSI bus changes to the bus free state.
- The Select or Reselect command terminates with a selection time-out.

A disconnect reset resets the following subset of the functions reset by the Soft Reset:

- Sequencer Mode bits are cleared (target = 0 and initiator = 0).
- Initializes Command register FIFO to empty.
- Releases all SCSI signals except RSTO/
- Resets disconnect, initiator, and target command modules.

Chapter Three
Signal Descriptions

This chapter contains signal descriptions and pin diagrams for the 68-pin PLCC and 80-pin PQFP packages. The signal descriptions are the same for the 53CF90A and 53CF90B. A slash (/) indicates an active low signal, I = an input signal, and O = an output signal. Figures 3-1 and 3-2 on the following pages are the pin diagrams for each chip.

Figure 3-1. NCR 53CF90A Pin Configurations

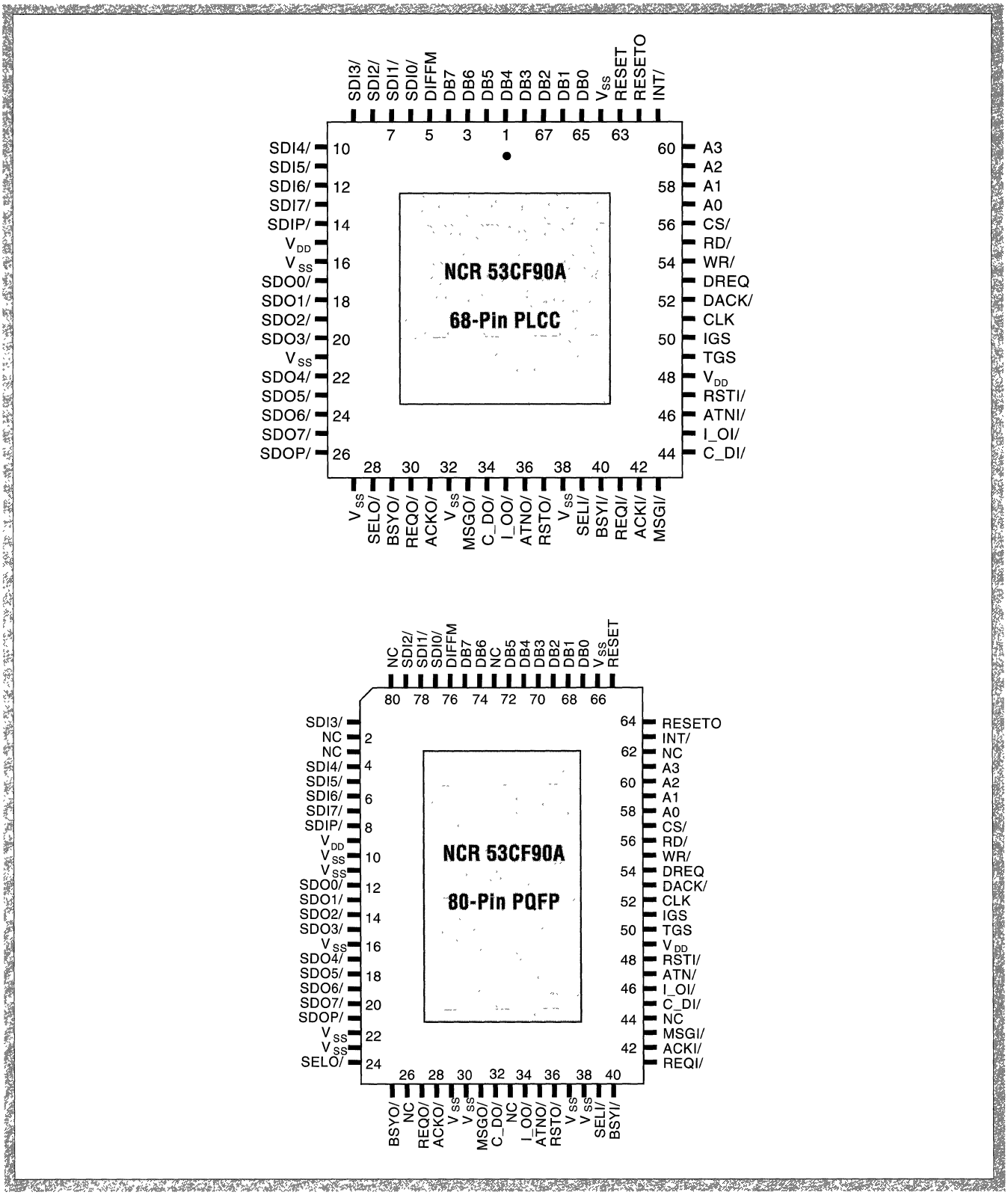


Figure 3-2. NCR 53CF90B Pin Configurations

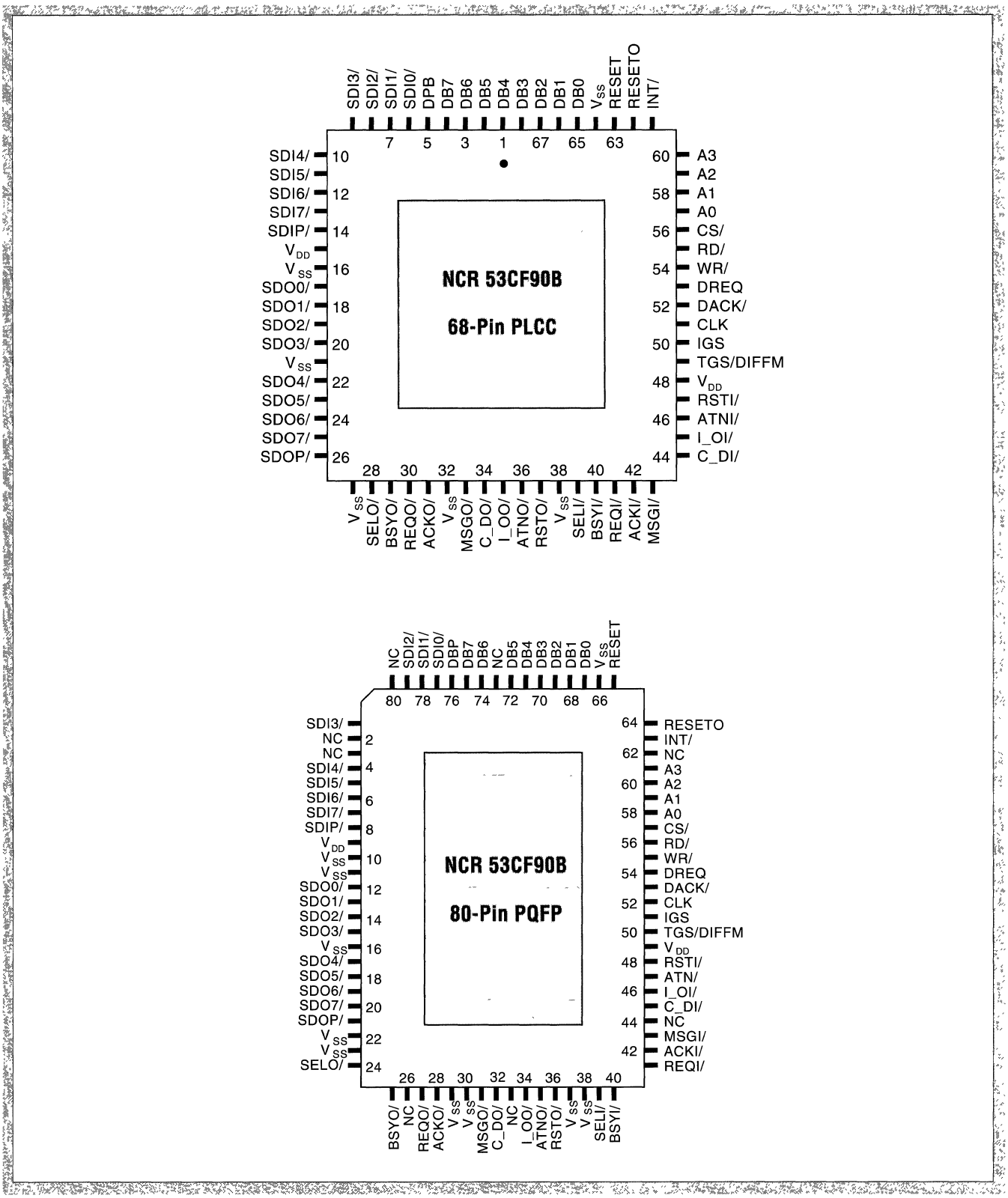


Table 3-1. Host Microprocessor and DMA Interface Pins

Symbol	Pin No. 80-Pin PQFP	Pin No. 68-Pin PLCC	Type	Description
DB7-DB0	75, 74, 72-67	4-1, 68-65	I/O	Active high data bus connected to the CPU data bus.
RESET	65	63	I	Active high chip reset. Must be asserted for at least two CLK periods after the voltage on the power pins has reached minimum V_{DD}.
RESETO	64	62	O	Active high reset output. Asserted when RESET is true or when a SCSI reset interrupt time-out occurs.
INT/	63	61	O	Active low, open drain interrupt signal to the microprocessor. Cleared when the chip is reset or the Interrupt register (05h) is read.
A3-A0	61-58	60-57	I	Active high address bus. Used with CS/ to specify an FSC register for reading or writing.
CS/	57	56	I	Active low chip select. Enables access to the selected FSC register. CS/ and DACK/ must never be active at the same time.
RD/	56	55	I	Active low read strobe. Enables FSC register data onto DB7-DB0. CS/ or DACK/ must also be active.
WR/	55	54	I	Active low write strobe. Transfers data from DB7-DB0 into an FSC register. CS/ or DACK/ must also be active.
DREQ	54	53	O	Tristate active high DMA request. Indicates when the FSC is ready to transfer data.
DACK/	53	52	I	Active low DMA acknowledge. Used with RD/ or WR/ to transfer data. DACK/ and CS/ must never be active at the same time.
CLK	52	51	I	Clock signal. Generates internal chip timing. Maximum frequency is 40 MHz (FASTCLK bit set) or 25 MHz (FASTCLK bit reset).
DBP	76	5	I/O	**(53CF90B Only)** Active high data bus parity. Odd parity for DB7-DB0.

Table 3-2. SCSI Bus Interface Pins

Symbol	Pin No. 80-Pin PQFP	Pin No. 68-Pin PLCC	Type	Description
SDIP/ SDI7/-SDI0/	8 7-4,1, 79-77	14 13-6	I/O	Schmitt trigger, active low, SCSI data/parity bus. In single-ended mode, these inputs are SCSI data bus signals. In differential mode, these are bi-directional data and parity signals for external SCSI bus transceivers. Odd SCSI parity is assumed.
SDOP/ SDO7/-SDO4/ SDO3/-SDO0/	21 20-17, 15-12	26 25-22, 20-17	O	Open drain, 48 mA, SCSI data/parity bus. In single-ended mode these outputs are active low SCSI data signals. In differential mode these outputs are used to control the direction of external differential transceivers, with high indicating output to the SCSI bus, and low indicating input from the SCSI bus. SCSI parity out is odd.
SELO/	24	28	O	Open drain, 48 mA, SCSI select. Asserted by the FSC to select a Target or reselect an Initiator. Active low in single-ended mode, active high in differential mode.
BSYO/	25	29	O	Open drain, 48 mA SCSI busy signal. Asserted by the FSC to gain use of the SCSI bus. Active low in single-ended mode, active high in differential mode.
REQO/	27	30	O	Open drain, 48 mA signal (single-ended mode) or totem-pole, 4mA signal (differential mode). Asserted by the FSC only in Target mode to request a data transfer over the SCSI bus.
ACKO/	28	31	O	Open drain, 48 mA signal (single-ended mode) or totem-pole, 4mA signal (differential mode). Asserted bt the FSC only in Initiator mode to acknowledge a request for a data transfer over the SCSI bus.
MSGO/	31	33	O	Open drain, 48 mA SCSI phase signal. Asserted by the FSC only in Target mode to initiate a Message In or a Message Out phase.
C_DO/	32	34	O	Open drain, 48 mA SCSI phase signal. Asserted by the FSC only in Target mode to indicate that it is transferring control or data information on the SCSI bus.

Table 3-2. SCSI Bus Interface Pins, Continued

Symbol	Pin No. 80-Pin PQFP	Pin No. 68-Pin PLCC	Type	Description
I_OO/	34	35	O	Open drain, 48 mA SCSI phase signal. Asserted by the FSC only in Target mode to indicate that the direction of data movement on the SCSI bus is from the FSC to the Initiator. This signal also distinguishes between Selection and Reselection phases.
ATNO/	35	36	O	Open drain, 48 mA SCSI attention signal. Asserted by the FSC only in Initiator mode. Alerts the Target SCSI device that the FSC has a command or message to transfer.
RSTO/	36	37	O	Open drain, 48 mA SCSI reset signal. Active low in single-ended mode, active high in differential mode. The FSC drives this signal true only when the host writes the SCSI Bus reset command to the Command register (03h).
SELI/	39	39	I	Schmitt trigger, active low SCSI select input. Selects the FSC as a Target or Reselects the FSC as an Initiator.
BSYI/	40	40	I	Schmitt trigger, active low SCSI busy input. Indicates to the FSC that the SCSI bus is in use.
REQI/	41	41	I	Schmitt trigger, active low SCSI request input. Indicates to the FSC, as Initiator, that a Target device is requesting a data transfer on the SCSI bus.
ACKI/	42	42	I	Schmitt trigger, active low SCSI acknowledge input. Asserted by an Initiator to acknowledge a request by the FSC for a data transfer on the SCSI bus.
MSGI/	43	43	I	Schmitt trigger, active low SCSI message input. Indicates to the FSC that a Target device has initiated a SCSI Message In or Message Out phase.
C_DI/	45	44	I	Schmitt trigger, active low SCSI control/data input. Signals the FSC that a Target device is transferring control or data information on the SCSI bus.

Table 3-2. SCSI Bus Interface Pins, Continued

Symbol	Pin No. 80-Pin PQFP	Pin No. 68-Pin PLCC	Type	Description
I_OI/	46	45	I	Schmitt trigger, active low SCSI input/output input. Alerts the FSC, as Initiator, that the direction of data movement on the SCSI bus is into the chip. This signal also distinguishes between Selection and Reselection phases.
ATNI/	47	46	I	Schmitt trigger, active low SCSI attention input. Indicates to the FSC that an Initiator device is ready to transfer a message or a command.
RSTI/	48	47	I	Schmitt trigger, active low SCSI reset input. When this signal is true, the FSC and all other SCSI devices will disconnect from the SCSI bus.
IGS	51	50	O	Active high initiator group select signal. Indicates the FSC is in Initiator mode. Used to enable external drivers for the Initiator signals ACKO/ and ATNO/.
TGS	50	49	O	**(53CF90A Only)** Active high Target group select signal. Indicates the FSC is in Target mode. Used to enable external drivers for the Target signals REQO/, MSGO/, C_DO/, and I_OO/.
DIFFM	76	5	I	**(53CF90A Only)** Differential mode enable. A low input enables single-ended mode. A high input enables differential mode.
TGS/DIFFM	50	49	I/O	**(53CF90B Only)** This pin is sampled during a hard reset, and latched afterwards, to put the FSC in single-ended or differential mode. High enables single-ended, low enable differential. The 53CF90B has an internal pullup on this pin to place the chip in single-ended mode, but requires an external 1 K pulldown to place it in differential mode. The signal then switches function to become the TGS output as described above for the 53CF90A.

Table 3-3. Power and Ground Pins

Symbol	Pin No.		Description
	80-Pin PQFP	68-Pin PLCC	
V_{DD}	9, 49	15,48	+5 Volt power input
V_{SS}	66, 38, 37, 30, 29, 23, 22, 16, 11, 10	64,38,32, 27, 21, 16	Ground. NCR recommends use of a ground plane.

Chapter Four
Registers

The FSC registers allow the microprocessor to configure, command, and monitor the SCSI bus, and to pass data through the chip to the SCSI bus. See Table 4-1 for a listing of these registers in address order, and Appendix C for a summary of register bits.

The terms "set" and "assert" are used to refer to bits that are programmed to binary one. Similarly, the terms "reset", "clear", or "deassert" are used to refer to bits that are programmed to binary zero.

Reserved bits should always be written as zero and should be masked when read, as they may be set during chip operations. Some registers have different functions for reads and writes.

Table 4-1. Register Definition Summary

Address (hex)	Read Register	Write Register
00	Transfer Counter Low	Transfer Count Low
01	Transfer Counter Mid	Transfer Count Mid
02	FIFO	FIFO
03	Command	Command
04	Status	Destination ID
05	Interrupt	Time-Out
06	Sequence Step	Synchronous Transfer Period
07	FIFO Flags	Synchronous Offset
08	Configuration 1	Configuration 1
09	Reserved	Clock Conversion
0A	Reserved	Test
0B	Configuration 2	Configuration 2
0C	Configuration 3	Configuration 3
0E	Transfer Counter High/ID	Transfer Count High

Transfer Counter Register
Address 00h, 01h Read Only

CTR7	CTR6	CTR5	CTR4	CTR3	CTR2	CTR1	CTR0
7	6	5	4	3	2	1	0
Default>>>							
X	X	X	X	X	X	X	X

These registers form a 16-bit transfer counter used for DMA data operations. They combine with the Transfer Counter High register (0Eh) to form a 24-bit transfer counter when the Features Enable bit (bit 6 in the Configuration 2 register) is set. A read from these addresses will return the value currently in the counter. DMA commands use the counter to terminate a transfer. Any DMA command will load the count value into the counter. A DMA NOP (80h) will load the counter while the non-DMA NOP (00h) will not. During the SCSI Data phase, the Transfer Counter decrements on the leading edge of:

Target	**Decremented by**
Data In	DACK/
Data Out	REQO/
Initiator	**Decremented by**
Synchronous Data In	DACK/
Asynchronous Data In	ACKO/
Data Out	DACK/

The counter counts bytes. It decrements by one when transferring a single byte; or by two when transferring a word.

Note that DACK/ can decrement the counter even if RD/ or WR/ do not go true. A false DACK/ can cause the counter to get out of synch with the data stream, leading to subtle errors. When a false DACK/ is expected to interfere with a temporarily suspended DMA operation, the DREQ Hi-Z bit (bit 4) in the Configuration 2 register (0Bh) should be set.

Transfer Count Register
Address 00h, 01h Write Only

CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0
7	6	5	4	3	2	1	0
Default>>>							
X	X	X	X	X	X	X	X

These two registers, together with the Transfer Count High register (0Eh), form a 24-bit register which stores the transfer count value for DMA data operations. They specify the number of bytes that are to be transferred over the SCSI bus. Values written to these registers will be stored internally and loaded into the Transfer Counter register by any DMA command. These values remain unchanged while the transfer counter decrements. Thus, successive blocks of equal size may be transferred without reprogramming the count. The values may be reprogrammed any time after the previous DMA operation has started, whether it has finished or not.

When the Features Enable bit (bit 6 in the Configuration 2 register) is clear, the Transfer Count High register is disabled. Therefore, zero in registers 00h and 01h specifies a maximum length count of 64 K. When the Features Enable bit is set, the Transfer Count High register is enabled. Then, zero in registers 00h, 01h, and 0Eh specifies a maximum length count of 16 MB. These registers are not changed by any reset, and their states are unpredictable after power-up.

Note: The value loaded into the Transfer Count register can be verified by issuing a DMA NOP command (80h) and reading the value at address 00h, 01h, and 0Eh.

FIFO Register
Address 02h Read/Write

FIFO 7	FIFO 6	FIFO 5	FIFO 4	FIFO 3	FIFO 2	FIFO 1	FIFO 0
Default>>>							
0	0	0	0	0	0	0	0

The FIFO register acts as a 16-byte first-in-first-out buffer between the SCSI bus and buffer memory. It is used to transfer SCSI data to and from the FSC. The FIFO is zeroed when a hard reset or a Flush FIFO command occurs. It is cleared if the phase changes from an output phase to Synchronous Data In during a Transfer Pad or Transfer Information command.

Command Register
Address 03h Read/Write

EnDMA 7	CmCd 6	CmCd 5	CmCd 4	CmCd 3	CmCd 2	CmCd 1	CmCd 0
Default>>>							
X	X	X	X	X	X	X	X

The Command register functions as a two-deep, 8-bit FIFO, enabling the microprocessor to stack commands to the FSC. Up to two commands may be stacked in the Command register. The second Command may be written before the FSC completes (or even starts) the first. The register is read from the bottom and returns the value of the last executed, or currently executing, command. Reading the register does not affect the contents.

Execution of a command begins within six clock cycles after it drops to the bottom of the Command register. Exceptions to this are the Reset Chip, Reset SCSI Bus, and Stop DMA commands, which execute within four clock cycles of being loaded into the top of the Command register. An interrupt is generated, if applicable, at command completion.

If two commands are placed in the Command register, two interrupts may result. If the first interrupt is not serviced before the second command finishes, the second interrupt is stacked behind the first. When the Interrupt register (05h) is read by the host to service the first interrupt, the contents of the Status register (04h), Sequence Step register (06h), and Interrupt register will change to describe the second interrupt.

The conditions listed below will clear the command FIFO and cause it to be held reset until the Interrupt register (05h) is read.

- Hardware reset
- Software reset
- SCSI bus reset
- SCSI bus disconnect
- Bus-initiated Selection or Reselection
- Select command
- Reconnect command if ATN is set
- Select or Reselect time-out
- Target Terminate command
- Parity error detected in Target mode
- Assertion of ATN in Target mode
- Any phase change in Initiator mode
- Illegal command

If the Features Enable bit (bit 6, Configuration 2 register) is not set, a SCSI Bus reset clears the Command register FIFO, but does not cause it to be held reset until the Interrupt register is read. Then if the Command register is loaded with a command while the register is in the reset condition, and before the Interrupt register is read, the chip attempts to execute the loaded command causing undesirable command execution. This condition is avoided by setting the Features Enable bit.

Bit 7 Enable DMA

When this bit is set, the command is a DMA instruction. When it is not set, the command is a non-DMA instruction. DMA instructions will load the transfer counter with the value in the Transfer Count register (00h, 01h, and 0Eh) without changing the register. Data transfers will continue until the count decrements to zero. If the transfer terminates prematurely, the bits in the Status register (04h), Sequence Step register (06h), and Interrupt register (05h) will indicate the reason.

Bits 6-0 Command Code

The FSC commands are shown in Chapter Five, *Command Set*. Bits six, five, and four specify a mode group, as illustrated below. Commands from the Miscellaneous group may be may be issued at any time (except Target Stop DMA). Commands from the Disconnected, Target, or Initiator groups will only be accepted by the FSC if it is in the same mode as the command when that command falls to the bottom of the Command register. Otherwise, an Illegal Command interrupt will be generated. For example, after a hardware or software reset, the FSC will be in the disconnected state. A command from either the target group or the initiator group will cause an Illegal Command interrupt. An Enable Selection/Reselection command by itself will not change modes. However, if another SCSI device then selects the FSC, it will be in the target state. If another device reselects the FSC, it will then be in the initiator state. Similarly, any Select command will place the FSC in Initiator mode, while the Reselect Sequence command will place the FSC in Target mode.

Bits 6, 5, 4	Command Mode
000	Miscellaneous
001	Initiator
010	Target
100	Disconnected State

Status Register
Address 04h Read Only

INT	GE	PE	TC	VGC	MSG	C/D	I/O
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	X	X	X

The Status register contains important flags that indicate certain events have occurred. Bits 7-3 are cleared by a hard reset, or when the Interrupt register (05h) is read while an interrupt is pending. The Phase bits 2-0 are live indicators of the state of the SCSI bus, and are not normally latched. They may be latched (for stacked commands) by setting the Features Enable bit in the Configuration 2 register (0Bh). The Status register should always be read prior to reading the Interrupt register.

Bit 7 Interrupt

This bit is set whenever the FSC drives the INT/ output true. It may be polled. It is buffered from the actual output so that in wired-OR (shared interrupt) designs, this bit will indicate whether the FSC is attempting to interrupt the microprocessor. Hardware reset, the Reset Chip command, or a read from the Interrupt register will release an active INT/ signal and also clear this bit.

Bit 6 Gross Error

This bit is set when one of the following errors occurs:

- The top of the Data FIFO is overwritten
- The top of the Command FIFO is over written
- Direction of DMA transfer is opposite to the direction of the SCSI transfer
- An unexpected phase change in initiator role during Synchronous Data phase

These conditions do not cause an interrupt. A gross error may be detected only while servicing another interrupt. This bit is cleared by reading the Interrupt register (05h) if the interrupt output is asserted. It will also be cleared by a hardware reset or the Reset Chip command, but not by SCSI reset.

Bit 5 Parity Error

This bit will be set if parity checking is enabled in the Configuration 1 register (08h), and the FSC detects a SCSI parity error on incoming command, data, status, or message bytes. It will be cleared by reading the Interrupt register (05h) if the interrupt output is asserted. Hardware reset or the Reset Chip command will clear this bit, but SCSI reset will not.

Bit 4 Terminal Count

This bit is set when the transfer counter decrements to zero. It is not set by loading a zero into the Transfer Count register (00h, 01h, and 0Eh). It is reset when the Transfer Counter register (00h, 01h, and 0Eh) is loaded with a DMA command. Since a DMA NOP (80h) command will load the transfer counter, it will also clear this bit. A non-DMA NOP (00h) will not load the counter and will not clear this bit. Reading the Interrupt register (05h) will not clear this bit. Hardware reset or the Reset Chip command will clear it, but the SCSI reset will not.

Bit 3 Valid Group Code

When the FSC is selected, this bit decodes the group code field in the first byte of the CDB (Command Descriptor Block). If the group code matches one defined in ANSI X3.131-1986, this bit will be set. An undefined group code (designated reserved by the ANSI committee) leaves it not set. If the SCSI-2 bit is set in the Configuration 2 register (0Bh), Group 2 commands will be recognized as ten-byte commands and this bit will be set. If the SCSI-2 bit is cleared, Group 2 commands will be treated as reserved commands. Group 3 and 4 are always treated as reserved commands. A reserved group command will cause the FSC to request six command bytes, The

FSC recognizes Group 6 as 6-byte vendor unique commands and Group 7 as ten-byte vendor unique commands. The Valid Group Code bit will be cleared by reading the Interrupt register (05h) if the interrupt out put is asserted. It will also be cleared by a hardware reset or the Reset Chip command, but not by a SCSI reset.

Bits 2-0 Phase Bits

These bits indicate the phase on the SCSI bus. They may be latched or unlatched, depending on the Features Enable bit (bit 6 in the Configuration 2 register).

When not latched, they indicate the phase at the time the Status register was read. In keeping with the ANSI definition of the phase signals, these bits must be stable during the Status register read that follows an interrupt generated by the FSC.

When the latch is enabled, the SCSI phase is latched upon command completion. These values are latched only if the Features Enable bit is set. The transparent latch is reopened when the Interrupt register (05h) is read.

Bits 2 (MSG)	Bits 1 (C/D)	Bits 0 (I/O)	SCSI Bus Phase
0	0	0	Data Out
0	0	1	Data In
0	1	0	Command
0	1	1	Status
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Message Out
1	1	1	Message In

Destination ID Register
Address 04h Write Only

RES 7	RES 6	RES 5	RES 4	RES 3	DID2 2	DID1 1	DID0 0
Default>>>							
0	0	0	0	0	X	X	X

The least significant three bits of this register specify the encoded destination bus ID for a Selection or Reselection command. These bits are binary encoded, with 111 representing device ID 7 which appears as 80h on the SCSI bus. The most significant five bits are reserved. The destination ID is not changed by any reset, and the states of these bits are unpredictable after power-up.

Interrupt Register
Address 05h Read Only

SRD	IL	DIS	BS	FC	RESEL	SATN	SEL
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

This 8-bit register is used in conjunction with the Status register (04h) and Sequence Step register (06h) to determine the cause of an interrupt. Reading this register when the interrupt output is true will clear all three registers. The entire Interrupt register will be cleared to zeros by a hardware reset or the Reset Chip command, but not by SCSI reset.

Note: This register should only be read when an interrupt is pending. The Sequence Step and Status registers should be read prior to reading this register.

Bit 7 SCSI Reset Detected
This bit is set if the SCSI Reset Reporting Interrupt Disable bit (bit 6 in the Configuration 1 register) is cleared, and the chip detects a reset on the SCSI bus.

Bit 6 Illegal Command
This bit is set when a reserved code is placed in the Command register (03h) or when the command is from a mode group different than the mode the FSC is currently in. Refer to the Command register definition. An interrupt is generated when this bit is set.

Bit 5 Disconnect
In initiator mode, this bit is set when the target disconnects or a Selection or Reselection timeout occurs. When the FSC is in Target mode, this bit is set if a Terminate Sequence or Command Complete Sequence command causes the FSC to disconnect from the bus.

Bit 4 Bus Service
This bit indicates that another device is requesting service. In Target mode, it is set whenever the initiator asserts ATN (Attention). In Initiator mode, it is set whenever the target is requesting an Information Transfer phase.

Bit 3 Function Complete
This bit will be set after any Target mode command has completed. In Initiator mode, it is set after a target has been selected (before transferring any command phase bytes), after Command Complete finishes, or after a Transfer Information command when the target is requesting Message In phase.

Bit 2 Reselected
This bit is set during Reselection phase to indicate that the FSC has been reselected as an initiator.

Bit 1 Selected With ATN
This bit is set during Selection phase to indicate that the FSC has been selected as a target and that Attention (ATN) was asserted on the SCSI bus.

Bit 0 Selected
This bit is set during Selection phase to indicate that the FSC has been selected as a target and that ATN was false during selection.

Time-Out Register
Address 05h Write Only

TO7	TO6	TO5	TO4	TO3	TO2	TO1	TO0
7	6	5	4	3	2	1	0
Default>>>							
X	X	X	X	X	X	X	X

This 8-bit, write only register specifies the amount of time the FSC will wait for a response during selection or reselection. The FSC can not time-out if it never wins arbitration, and would keep trying indefinitely. The Time-Out register is normally loaded to specify a time-out period of 250 ms to comply with the ANSI standard. The register value (RV) may be calculated from:

$$RV = \frac{\text{(Time-out period) (CLK frequency)}}{\text{8192 (Clock conversion factor)}}$$

For example, at 25 MHz, the register value that gives a 250 ms time-out period is 153 decimal or 99 hexadecimal. The clock conversion factor is defined in the description of the Clock Conversion register (09h). To compute the register value using the above formula when the clock conversion factor is zero, use eight, the number of clocks, rather than zero. The Time-Out register remains unchanged by any reset. The states of these bits are unpredictable after powerup.

Sequence Step Register
Address 06h Read Only

RES	RES	RES	RES	SOM	SS2	SS1	SS0
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

The lower three bits of this register are used to indicate how far the internal sequencer was able to proceed in executing a sequenced command. This counter will be incremented at certain points in sequenced commands to aid in error recovery if the command does not complete normally.

Reading the Interrupt register (05h) while an interrupt is pending clears the Sequence Step register to zero. The Sequence Step register is also cleared by a hard or soft reset.

Bits 7-4 Reserved

Bit 3 Synchronous Offset Max

When this bit is clear, the synchronous offset counter has reached its maximum value.

Bits 2-0 Sequence Step

The sequence step counter is set to zero at the beginning of certain commands. The counter is then incremented at specific points in the various algorithms to aid in error recovery. The possible states are described in Chapter Five, *Command Set.*

Synchronous Transfer Period Register Address 06h Write Only

RES 7	RES 6	RES 5	STP4 4	STP3 3	STP2 2	STP1 1	STP0 0
Default>>>							
0	0	0	0	0	1	0	1

Bits 4-0 of this register specify the minimum time between leading edges of successive request or acknowledge pulses. Synchronous data will be transmitted or received at the rate of one byte every N clocks (CLK). The variable N is related to the register value as shown below.

40 MHz Clock (FASTCLK bit set)

FAST SCSI bit value	Register Value (h)	Clocks per byte	Transfer Rate MB/sec
1	04	4	10.0
1	05	5	8.0
1	06	6	6.6
1	07	7	5.7
0	08	8	5.0
0	09	9	4.4
0	0A	10	4.0
0	0B	11	3.6
0	0C	12	3.3
0	0D	13	3.0
0	0E	14	2.8
0	0F	15	2.6
0	10	16	2.5
0	11	17	2.3
0	12	18	2.2
0	13	19	2.1
0	14	20	2.0
.	.	.	.
.	.	.	.
.	.	.	.
0	1F	31	1.29
0	00	32	1.25
0	01	33	1.21
0	02	34	1.18
0	03	35	1.14

25 MHz Clock (FASTCLK bit clear)

FAST SCSI bit value	Register Value (h)	Clocks per byte	Transfer Rate MB/sec
0	05	5	5.0
0	06	6	4.2
0	07	7	3.6
0	08	8	3.1
0	09	9	2.8
0	0A	10	2.5
0	0B	11	2.3
0	0C	12	2.1
0	0D	13	1.9
.	.	.	.
.	.	.	.
.	.	.	.
0	19	25	1.0

The transfer rate is calculated by dividing the clock frequency by the number of clocks per byte specified in this register. If the result is greater than five the FASTSCSI bit (bit 1, Configuration 3 register) must be set.

Missing entries in the tables above follow the binary code. The upper three bits are reserved by NCR. This register defaults to five after hardware reset or software chip reset, and is left unchanged by a SCSI reset.

Note: Four is the minimum number of clocks per byte allowed.

Note: Any combination not listed in the above tables violates ANSI standards and should not be used.

Refer to the descriptions for the FASTCLK and FASTSCSI bits (bits 0 and 1 in Configuration 3 register) for information on Fast SCSI operation.

FIFO Flags Register
Address 07h Read Only

SS2	SS1	SS0	FF4	FF3	FF2	FF1	FF0
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

The least significant five bits of this register indicate how many bytes are currently in the FIFO. The value is binary encoded. The flags should not be polled while transferring data because they will not be stable while the SCSI interface is changing the contents of the FIFO.

The upper three bits are duplicates of the Sequence Step register (06h) bits in normal mode. If Test Mode is enabled, bit 5 is set to indicate that the offset counter is not zero. Not zero means that synchronous data may continue to be transferred. Zero means that the synchronous offset count has expired and the FSC will not transfer any more data until it receives an acknowledge.

Synchronous Offset Register
Address 07h Write Only

DC1	DC0	AC1	AC0	S/AT	S/AT	S/AT	S/AT
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bits 7-6 Deassertion Control
These bits control when the REQ and ACK signals deassert by selecting one of four clock edges. These bits only affect a Synchronous Data In or Synchronous Data Out phase. The control over deassertion of these signals is measured in input clock cycles and is dependent on the status of the FASTCLK bit (bit 0 in the Configuration 3 register) as shown below.

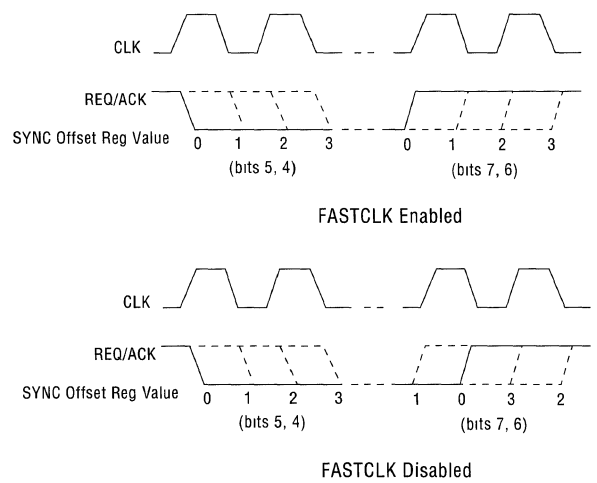
FASTCLK Status	Synchronous Offset Register bits 7-6	REQ/ACK Deassertion Delay (input clock cycles)
1	00	No Delay (Default)
1	01	1/2 clock
1	10	1 clock
1	11	1 1/2 clocks
0	00	No Delay
0	01	1/2 clock early
0	10	1 clock
0	11	1/2 clock

Bits 5-4 Assertion Control

Bits five and four control when REQ or ACK asserts by selecting one of four input clock edges. Assertion of the REQ and ACK signals is not dependent on the FASTCLK bit. The assertion delay is shown below.

Synchronous Offset Register bits 5-4	REQ/ACK Assertion Delay (input clock cycles)
00	0 (Default)
01	1/2 clock
10	1 clock
11	1 1/2 clock

Figure 4-1. REQ/ACK Deassertion Delay



Note The input clock duty cycle affects the half clock assertion/deassertion delays

Bits 3-0 Sync/Async Transfer

The least significant four bits of this register specify whether the FSC will transfer data phase bytes synchronously or asynchronously. Zero specifies asynchronous transfer. Any other value specifies the synchronous offset, the number of data phase bytes that may be sent synchronously without an acknowledge (either REQ or ACK), depending on whether the FSC is in initiator or target mode.

When transmitting to the SCSI bus, the FSC will stop sending bytes when it reaches this offset, and thereafter send one byte for every acknowledge it receives from the other SCSI device.

When receiving from the SCSI bus, the FSC will send an acknowledge every time a byte is removed from its FIFO on the DMA (or microprocessor) interface. The maximum offset of 15 allows a receiving FSC to store data in its FIFO while the external DMA controller gains control of the memory bus.

The synchronous offset is cleared (00) by hardware reset or a software Chip Reset, but not by SCSI reset.

Configuration 1 Register
Address 08h Read/Write

SCM	SRD	PTM	EPC	CTEn	My Bus ID		
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

This read/write register specifies various operating conditions for the FSC. Any bit pattern written to this register may be read back and should be identical.

Bit 7 Slow Cable Mode

Slow cable mode is needed when cabling conditions cause SCSI bus violations. It compensates for excessive capacitive loading on the SCSI data signals by inserting an extra CLK period between data being asserted on the bus and REQ or ACK being driven true. This bit is cleared by hardware reset or the Chip Reset command, but not by SCSI reset.

Bit 6 SCSI Reset Reporting Interrupt Disable

This disables the reporting of a SCSI reset. If the SCSI reset signal goes true when this bit is set, the FSC will disconnect from the SCSI bus and remain idle in the disconnected state without interrupting the host. If this bit is not set, the FSC will respond to the SCSI reset by interrupting the host microprocessor. If the SCSI reset is still active when the microprocessor clears the interrupt, a new interrupt is generated and must be serviced. This bit is cleared by hardware reset or the Chip Reset command, but not by SCSI reset.

Bit 5 Parity Test Mode

When this bit is set, the parity output to the SCSI bus will be read from bit 7 of the transmitted byte, rather than from the parity bit. This allows parity errors to be created so that hardware and software may be tested. This bit must not be set during normal operation. This bit is cleared by hardware reset or the Chip Reset command, but not by SCSI reset.

Bit 4 Enable Parity Checking

Setting this bit causes the FSC to check parity on incoming SCSI bytes during any information transfer phase except when receiving pad bytes. Detecting parity errors will cause the Parity Error bit to be set in the Status register (04h), but will not cause an interrupt. In initiator role, bad parity will also set ATN (Attention) on the SCSI bus. When this bit is not set, parity will not be checked, the bit in the Status register will not be set, and ATN will not be asserted. Refer to *Parity Checking and Generation* in Chapter Two. This bit is cleared by hardware reset or the Chip Reset command, but not by SCSI reset.

Bit 3 Chip Test Mode Enable

When this bit is set, the chip is placed in a special test mode which enables the Test register (0Ah). Once it has been set, the chip must be reset (hard or soft but not SCSI) before normal operation can begin. This bit should not be set during normal operation. This bit is cleared by hardware reset or the Chip Reset command, but not by SCSI reset.

Bits 2-0 My Bus ID

These bits are the bus ID of this device. It is the ID to which the FSC responds during bus initiated selection or reselection, and the ID that it uses to arbitrate for the bus. This three bit field is binary encoded, and must be loaded at powerup. These bits are cleared by hardware reset or the Chip Reset command, but not by SCSI reset.

Clock Conversion Register
Address 09h Write Only

RES 7	RES 6	RES 5	RES 4	RES 3	CCF2 2	CCF1 1	CCF0 0
Default>>>							
0	0	0	0	0	0	1	0

Bits 7-3 Reserved

Bits 2-0 Clock Conversion Factor

These bits must be set according to the clock (CLK) input frequency. All timings longer than 400 ns depend on these bits agreeing with the CLK frequency. The clock conversion factor is equal to 200 ÷ the input clock period in nanoseconds. It should be set to one of the seven values below.

CLK Frequency (MHz)	Clock Conversion Factor
10	010
10.01 to 15	011
15.01 to 20	100
20.01 to 25	101
25.01 to 30	110
30.01 to 35	111
35.01 to 40	000

Note: A clock conversion factor of zero (000) indicates eight clocks.

These bits must never be loaded with a binary one (001). Hardware reset or the Reset Chip command will set these bits to the default value (010). SCSI reset will not affect this register.

Test Register
Address 0Ah Write Only

RES 7	RES 6	RES 5	RES 4	RES 3	Hi-Z 2	IM 1	TM 0
Default>>>							
0	0	0	0	0	0	0	0

This register is enabled by setting the special test mode bit (bit 3 in the Configuration 1 register). After test mode has been entered, a hardware reset or a Reset Chip command must occur before normal operation can begin. These bits must not be set during normal chip operation.

Bits 7-3 Reserved

Bit 2 All Outputs to High Impedance

When this bit is set, all bidirectional and all output pins go to high impedance and will not significantly load a TTL or compatible device.

Bit 1 Initiator Mode

When this bit is set, the FSC is artificially forced into initiator mode. Any initiator command will be accepted by the FSC. For example, a Set ATN command will cause ATN to be driven on the SCSI bus even if the FSC is disconnected.

Bit 0 Target Mode

When this bit is set, the FSC is artificially forced into target mode. Any target command will be accepted by the FSC. For example, a DMA command will load or unload the FIFO and set the SCSI phase, Data and REQ signals even if arbitration have not occurred.

Configuration 2 Register
Address 0Bh Read/Write

RES	FE	RES	DHZ	SCSI2	TBPA	RPE	DPE
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

The bits in this register determine different operating options for the FSC. After hardware reset or the Reset Chip command the register is cleared. Any bit pattern written to this register may be read back and should be identical.

Bit 7 Reserved

Bit 6 Features Enable

When set, this bit will enable the following features:

- The SCSI phase is latched at each command completion. This permits simpler software routines for stacked commands. When the Features Enable bit is not set, the phase bits (bits 2-0 in the Status register) are live indicators of the state of the SCSI phase lines.
- During differential mode operation when the SCSI phase changes from in to out, the SCSI Data In and Parity lines are delayed two or three CLKs before asserting. When the phase changes from out to in, the SCSI Data Out and Parity lines are delayed two or three CLKs before deasserting. At 40 MHz, this provides a minimum 50 ns turn-off time for the external transceivers. This will improve SCSI Data timings in differential mode by preventing electrical bus contention between the chip and the SCSI bus transceivers when the bus changes phase.
- The Transfer Counter High register at address 0Eh is enabled, which extends the transfer counter from 16 to 24 bits.
- If other conditions are met, setting the Features Enable bit also allows the chip revision code to be read (see the Transfer Counter High register description for more information on this feature).

Bit 5 Reserved

Bit 4 DREQ High Impedance

When this bit is set, the DREQ output (DMA request) goes to high impedance and will not significantly load a TTL compatible device. This is useful when several devices share the DMA request line (known as wired-OR). When this bit is set, the FSC will ignore any activity on the DACK/ (DMA acknowledge) input.

When this bit is cleared, the DREQ output is enabled. Also, DACK/ is enabled to decrement the transfer counter and load or unload the FIFO, depending on WR/ or RD/. DACK/ should not pulse true without RD/ or WR/ because the transfer counter may decrement with out transferring any data. Refer to the Transfer Counter register description for more information.

Bit 3 SCSI-2

Setting this bit allows the FSC to support two new features adopted in SCSI-2: the 3-byte message exchange for tagged-queuing, and Group 2 commands. These features can also be selected separately using bits two and three in the Configuration 3 register (0Ch).

Tagged-Queuing

When this bit is set, and the FSC is selected with ATN (Attention), it will request either one or three message bytes depending on whether ATN remains true or goes false. If ATN is still true after the first byte has been received, the FSC may request two more message bytes before switching to command phase. If ATN goes false, it will switch to command phase after the first message byte. When the SCSI-2 bit is not set it will request a single message byte (as a target) when selected with ATN, and abort the selection sequence

(as an initiator) if the target does not switch to command phase after one message byte has been transferred. Refer to *Bus Initiated Selection* in Chapter Two.

Group 2 Commands
When the SCSI-2 bit is set, Group 2 commands are recognized as 10-byte commands. Receiving a Group 2 command with this bit set will set the Valid Group Code bit in the Status register (04h). If the SCSI-2 bit is not set, the FSC will treat Group 2 commands as reserved commands; it will request only six bytes in command phase, and will not set the Valid Group Code status bit.

Bit 2 Target Bad Parity Abort
When this bit is set, the FSC will abort a Receive command or Receive Data sequence when it detects a parity error.

Bit 1 Register Parity Enable (53CF90B Only)
When this bit is set, parity from the host DBP pin (53CF90B only) will be loaded into the FIFO when CS/ and WR/ are both true. When this bit is not set, the FSC generates parity from the host data bus when CS/ and WR/ are both true and places it in the FIFO along with the data from which it was generated.

When the FSC is moving data from the FIFO to the SCSI bus, it will flag outgoing parity errors if either this bit or the DMA Parity Enable bit is set.

Bit 0 DMA Parity Enable (53CF90B Only)
When this bit is set, parity from the host DBP pin (53CF90B only) will be loaded into the FIFO when DACK/ and WR/ are both true. When this bit is not set, the FSC generates parity from the host data bus when DACK/ and WR/ are both true and places it in the FIFO along with the data from which it was generated.

When the FSC is moving data from the FIFO to the SCSI bus, it will flag outgoing parity errors if either this bit or the Register Parity Enable bit is set.

Configuration 3 Register
Address 0Ch Read/Write

RES	RES	RES	IDM	QTE	CDB	FSCSI	FCLK
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

After hardware reset or a Reset Chip command the bits in this register are all cleared. Any bit pattern written to this register may be read back and should be identical.

Bits 7-5 Reserved

Bit 4 ID Message Reserved Check
This bit allows a second level of checking for the validity of an ID message. The most significant bit of an ID message byte is always checked, and must be one, or the chip interrupts. When this bit is set, bits 5-3 of the ID message are also checked and must be zero, or the chip interrupts. This check occurs in two cases: if the chip is selected with ATN true, or during reselection. If the validation check fails, the selection or reselection sequence halts and the chip generates an interrupt.

Bit 3 Queue Tag Enable
When this bit is set, the FSC can receive 3-byte messages during bus-initiated select with ATN. This feature is also enabled by setting bit 3 in the Configuration 2 register (0Bh). The message bytes consist of a 1-byte Identify message and a 2-byte Queue Tag message. The middle byte is the tagged queue message itself and the last byte is the tag value (0 to 255). When this bit is set, the second byte is checked to see if it is a valid queue tagging message. If the value of the byte is not 20h, 21h, or 22h, the sequence halts and an interrupt is generated. When this bit is not set, the chip aborts the select with ATN sequence after it receives one Identify message byte, if ATN is still asserted.

Bit 2 CDB10

When this bit is set, 10-byte Group 2 commands are recognized as valid Command Descriptor Blocks (CDB). The target command sequence receives ten Group 2 command bytes and sets the Valid Group Code bit (Status register, bit 3). When this bit is not set, the target command sequence receives only six Group 2 command bytes and does not set the Valid Group Code bit. The group code defines how many bytes to request while driving command phase. This feature is also enabled or disabled by setting or clearing bit 3 in the Configuration 2 register (0Bh).

Bit 1 FASTSCSI

Bit 0 FASTCLK

Bits one and zero in this register are used to inform the device that it is connected to a fast clock, and to select between Fast SCSI timings and SCSI-1 timings. Fast SCSI operation requires a fast clock. A fast clock is one with a frequency greater than 25 MHz. These bits affect the SCSI transfer rate as follows:

Bit 1	Bit 0	Min clocks/byte async	Min clocks/byte sync	SyncTransfer (MB/s)
X	0	2	5	5
0	1	3	8	5
1	1	3	4	10

Note: 10 MB/s transfer rates require a clock of 40 MHz.

Transfer Counter High/ID Register
Address 0Eh Read Only

TCRH7	TCRH6	TCRH5	TCRH4	TCRH3	TCRH2	TCRH1	TCRH0
7	6	5	4	3	2	1	0
Defaults>>>							
X	X	X	X	X	X	X	X

This register extends the transfer counter to 24 bits. Like the other transfer counter registers, this register is not affected by any reset condition. After power-up or a chip reset, and until Transfer Counter High register is loaded, the FSC part unique ID code is readable from this register. The Transfer Counter High register is only enabled when the Features Enable bit (bit 6 in the Configuration 2 register) is set. Refer to the descriptions for Transfer Counter Low register (00h) and Transfer Counter Mid register (01h) for more information on the transfer counter.

An 8-bit, part unique ID code is available in the Transfer Counter High register. To read the ID value, do the following:

1) Hardware reset or issue a Reset Chip command
2) Issue two successive DMA NOP commands (80h)
3) Read the register

Bits 7-3 indicate the chip family code. Bits 2-0 indicate the revision level of the chip. The FSC family code is zero and the revision level is two.

Transfer Count High Register
Address 0Eh Write Only

TCH7	TCH6	TCH5	TCH4	TCH3	TCH2	TCH1	TCH0
7	6	5	4	3	2	1	0
Default>>>							
X	X	X	X	X	X	X	X

This register extends the Transfer Count to 24 bits. Like the other transfer count registers, this register is not affected by any reset condition. This register is only enabled when the Features Enable bit (bit 6 in the Configuration 2 register) is set. Refer to the descriptions for Transfer Count Low register (00h) and Transfer Count Mid register (01h) for more information on the transfer count.

Chapter Five
Command Set

Introduction

Most FSC instructions have both DMA and non-DMA command forms. DMA commands move data between memory and the SCSI bus, and require an external DMA controller to move data between memory and the FIFO. Non-DMA commands move data between the FIFO and the SCSI bus, and require the microprocessor to move data between the FIFO and memory.

Commands get to the FSC by writing an 8-bit command code to the Command register (at address 03h). When bit seven of this code is set, the command is a DMA instruction. When it is not set, the command is a non-DMA instruction.

DMA commands will load the Transfer Counter register (at addresses 00h, 01h, and 0Eh) with the value in the Transfer Count register(same addresses), so the transfer count must be loaded before any DMA command is issued. A DMA command terminates when the transfer counter decrements to zero.

Non-DMA commands provide a fast, efficient way to transfer a small number of bytes, such as Command Descriptor Blocks (CDB), or synchronous negotiation messages across the SCSI bus. The Transfer Counter register is not loaded or changed during these transfers. All non-DMA commands terminate when the FIFO becomes empty.

If a non-DMA command is issued, or the NOP command is issued with bit 7 of the command code set, the value in the Transfer Count register is loaded into the Transfer Counter register. However, the count is not decremented, and no DMA transfer takes place.

In either a DMA or non-DMA command, the word "sequence" in the command name indicates that the Sequence Step register (at address 06h) is affected by executing the command. Check the Sequence Step register after using these commands to verify the command completed normally, or to aid in data recovery if the command did not complete normally.

Command Groups

The FSC commands form four mode groups specified by bits six, five and four of the command code. These are labeled Initiator State, Target State, Disconnect State, and Miscellaneous. The Initiator State commands can be used only when the FSC is connected on the SCSI bus as an initiator. These commands are used to select a target, send a Command Descriptor Block (CDB), assert the ATN signal, and receive status and message bytes. If the FSC is not connected as an initiator, and an Initiator State command is attempted, an Illegal Command interrupt is generated to the processor.

The Target State commands can only be used when the FSC is connected on the SCSI bus as a target. These commands are used to receive a CDB, respond to the ATN signal, and send status and message bytes.

The Disconnected State commands are used when the SCSI bus is idle. They are used to arbitrate for the bus, select a target or reselect an initiator, then optionally send one or three bytes of message information before interrupting the processor. Most of the commands in this group are sequence commands that perform more than one task before interrupting the processor. This results in fewer interrupts, and less time spent in interrupt service routines.

The Miscellaneous commands may be used at any time. These include resetting the FSC or the SCSI bus, flushing the FIFO, or performing a NOP.

Stacked Commands

The Command register (03h) functions as a two deep eight-bit command FIFO enabling the processor to stack DMA commands to the FSC. Non-DMA commands should not be stacked. Commands that transfer data in one direction should not be stacked with commands that transfer data in the other direction.

For stacked DMA commands, the Transfer Count register (00h, 01h, and 0Eh) must be loaded prior to loading the command code in the Command register. Command stacking should be used only during SCSI DATA IN or DATA OUT transfers. In Initiator mode, care must be taken since the SCSI phase lines in the Status register (04h) are not latched at the time an interrupt is reported. The SCSI phase lines can be latched at the end of a command by enabling the Features Enable bit (bit 6, Configuration 2 register). This allows the host to determine the ending phase of the interrupting command even though phase changes may have occurred after the stacked command began executing.

Illegal Commands

Writing an illegal command to the Command register (03h) will cause an Illegal Command interrupt. An illegal command is one written to the chip specifying an unsupported command mode, or a command not allowed in the specified command mode. Unsupported commands (see the 'Note" at the end of Table 5-1) may also cause illegal command interupts. An Illegal Command interrupt must be cleared prior to writing another command to the Command register.

Table 5-1. 53CF90A, 53CF90B Command Set

DMA	Non-DMA	Command Register	Command	Interrupt*
		7 6 5 4 3 2 1 0	**MISCELLANEOUS GROUP**	
80	00	X 0 0 0 0 0 0 0	NOP	no
-	01	0 0 0 0 0 0 0 1	Flush FIFO	no
-	02	0 0 0 0 0 0 1 0	Reset chip	no
-	03	0 0 0 0 0 0 1 1	Reset SCSI bus	yes**
			DISCONNECTED STATE GROUP	
C0	40	X 1 0 0 0 0 0 0	Reselect sequence	yes
C1	41	X 1 0 0 0 0 0 1	Select without ATN sequence	yes
C2	42	X 1 0 0 0 0 1 0	Select with ATN sequence	yes
C3	43	X 1 0 0 0 0 1 1	Select with ATN and stop sequence	yes
C4	44	X 1 0 0 0 1 0 0	Enable selection/reselection	no
-	45	0 1 0 0 0 1 0 1	Disable selection/reselection	yes
C6	46	X 1 0 0 0 1 1 0	Select with ATN3 sequence	yes
C7	47	X 1 0 0 0 1 1 1	Reselect3 sequence	yes

Table 5-1. 53CF90A, 53CF90B Command Set (Continued)

DMA	Non-DMA	Command Register	Command	Interrupt*
			INITIATOR GROUP	
90	10	X 0 0 1 0 0 0 0	Transfer information	yes
91	11	X 0 0 1 0 0 0 1	Initiator command complete sequence	yes
-	12	0 0 0 1 0 0 1 0	Message accepted	yes
98	-	1 0 0 1 1 0 0 0	Transfer pad	yes
-	1A	0 0 0 1 1 0 1 0	Set ATN	no
-	1B	0 0 0 1 1 0 1 1	Reset ATN	no
			TARGET GROUP	
A0	20	X 0 1 0 0 0 0 0	Send message	yes
A1	21	X 0 1 0 0 0 0 1	Send status	yes
A2	22	X 0 1 0 0 0 1 0	Send data	yes
A3	23	X 0 1 0 0 0 1 1	Disconnect sequence	yes
A4	24	X 0 1 0 0 1 0 0	Terminate sequence	yes
A5	25	X 0 1 0 0 1 0 1	Target command complete sequence	yes
-	27	0 0 1 0 0 1 1 1	Disconnect	no
A8	28	X 0 1 0 1 0 0 0	Receive message	yes
A9	29	X 0 1 0 1 0 0 1	Receive command	yes
AA	2A	X 0 1 0 1 0 1 0	Receive data	yes
AB	2B	X 0 1 0 1 0 1 1	Receive command sequence	yes
-	04	0 0 0 0 0 1 0 0	Target abort DMA	no***

* A 'yes' in the Interrupt column indicates that an interrupt is generated after command completion.

** The command will cause an interrupt, if the SCSI Reset Reporting bit is not cleared in the Configuration 1 register (at address 08h).

*** The command itself does not cause an interrupt. However, it may allow a stalled command to finish and generate an interrupt.

Note: A dash (-) in the DMA or Non-DMA column means the command is not supported and should not be used in that mode, as unreliable results are possible.

Miscellaneous Command Group

Miscellaneous commands can be executed and are valid in any mode.

Table 5-2. Miscellaneous Commands

DMA	Non-DMA	Mnemonic
80	00	No Operation (NOP)
-	01	Flush FIFO
-	02	Reset chip
-	03	Reset SCSI bus

NOP

No-Operation (NOP). The FSC requires this command only after hardware reset or the Reset Chip command to free the Command register (at address 03h). A DMA NOP (80h) may be used to load the transfer counter with the value in the Transfer Count register (at addresses 00h, 01h, and 0Eh). No interrupt is generated from this command.

Flush FIFO

The Flush FIFO command initializes the FIFO to the empty condition by resetting the FIFO flags and setting the bottom byte of the FIFO to zero.

Reset Chip

This command resets all functions in the chip and returns it to a disconnected state. The command has the same effect as a hardware reset.

Reset SCSI Bus

This command will assert the RSTO/ (SCSI Reset Output) signal for T2 µs, where

$$T2 = 130 \text{ (CLK period) (CCF)}$$

CCF = Clock Conversion Factor.

Refer to the description of the Clock Conversion register (09h) in Chapter Four. For CCF = 0, indicating 8 clocks, substitute 8 for 0 in this calculation. CLK is the clock input to the FSC. This command does not cause an interrupt; however, since RSTI/ may be externally connected to RSTO/ (in single-ended mode), an interrupt will be generated unless it is disabled in the Configuration 1 register (at address 08h).

Disconnected State Command Group

If any of the disconnected state commands are received by the FSC when it is not in the disconnected state, the command will be ignored, the Command register (03h) will be cleared, and the FSC will generate an illegal command interrupt.

Table 5-3. Disconnected State Commands

DMA	Non-DMA	Mnemonic
C0	40	Reselect Sequence
C1	41	Select without ATN sequence
C2	42	Select with ATN sequence
C3	43	Select with ATN and stop sequence
C4	44	Enable selection and reselection
-	45	Disable selection and reselection
C6	46	Select with ATN3 sequence
C7	47	Reselect3 Sequence

Reselect Sequence

This command will cause the FSC target to arbitrate for the bus and then enter the Reselection phase when it wins arbitration. The Identify message, required by SCSI protocol, must either be placed in the FIFO by the microprocessor before issuing the command, or must be transferred by DMA, which involves setting the transfer count to one and setting up the external DMA controller. In either case, the Time-Out and Destination ID registers (at addresses 05h and 04h) must have been programmed previously. The sequence will terminate early if a Reselect time-out occurs. If it terminates normally, a Function Complete interrupt will occur.

Select Without ATN Sequence

This command will cause the FSC initiator to arbitrate for the bus, enter the Selection phase when it wins, and send the CDB (Command Descriptor Block). The 6, 10 or 12-byte CDB must have either been placed in the FIFO previously by the microprocessor; or must be transferred by DMA, which involves setting the transfer count to 6, 10 or 12 and programming the external DMA controller. In either case, the Time-Out and Destination ID registers (at addresses 05h and 04h) must have been programmed previously. This command terminates early if a reselection time-out occurs, the target does not assert Command phase or the target removes Command phase too early. If it terminates normally, a Function Complete and Bus Service interrupt will be generated.

Table 5-4. Initiator Select without ATN Sequence

Sequence Step	Interrupt Register	Interpretation
2 1 0	**7 6 5 4 3 2 1 0**	
0 0 0	0 0 1 0 0 0 0 0	Arbitration complete; selection time-out; disconnected.
0 1 0	0 0 0 1 1 0 0 0	Arbitration and selection complete; stopped because target did not assert Command phase.
0 1 1	0 0 0 1 1 0 0 0	Stopped during command transfer because target prematurely changed phase.
1 0 0	0 0 0 1 1 0 0 0	Select sequence complete.

Select With ATN Sequence

This command will cause the FSC initiator to arbitrate for the bus, select a device with ATN true, then send one Message phase byte followed by 6, 10 or 12 Command phase bytes. The message and command bytes must have either been placed in the FIFO by the microprocessor or must be transferred by DMA, which involves setting the transfer count to 7, 11 or 13 and programming the external DMA controller. In either case, the Time-Out and Destination ID registers (05h and 04h) must have previously been programmed. This command terminates early if a select time-out occurs, the target does not assert Message Out phase followed by Command phase, or the target removes Command phase early. If it completes normally, a Function Complete and Bus Service interrupt will be generated.

Table 5-5. Initiator Select with ATN Sequence

Sequence Step	Interrupt Register	Interpretation
2 1 0	**7 6 5 4 3 2 1 0**	
0 0 0	0 0 1 0 0 0 0 0	Arbitration complete; selection time-out; disconnected.
0 0 0	0 0 0 1 1 0 0 0	Arbitration and selection complete; stopped because target did not assert Message Out phase; ATN still asserted by FSC.
0 1 0	0 0 0 1 1 0 0 0	Arbitration, selection, and Message out complete; sent one message byte with ATN true, then released ATN; stopped because target did not assert Command phase after message byte was sent.
0 1 1	0 0 0 1 1 0 0 0	Stopped during command transfer due to premature phase change; Some CDB bytes may not have been sent; check FIFO flags.
1 0 0	0 0 0 1 1 0 0 0	Selection With ATN Sequence complete. One message byte and all command bytes have been sent.

Select With ATN and Stop Sequence

This command should be used in place of Select With ATN when multiple Message phase bytes are to be sent (for example, a synchronous negotiation message). The command will select a target with ATN asserted, send one Message phase byte that had previously been stored in the FIFO, generate a Bus Service interrupt and a Function Complete interrupt, and stop. After the interrupt, the FIFO may be filled with other message bytes. A Transfer Information command will then transfer bytes with ATN true until the FIFO empties. If a DMA Transfer Information command is used, ATN will remain true until the transfer counter decrements to zero.

Table 5-6. Initiator Select with ATN and Stop Sequence

Sequence Step	Interrupt Register	Interpretation
2 1 0	**7 6 5 4 3 2 1 0**	
0 0 0	0 0 1 0 0 0 0 0	Arbitration complete; selection time-out; disconnected.
0 0 0	0 0 0 1 1 0 0 0	Arbitration and selection complete; stopped because target did not assert Message Out phase; ATN still asserted by FSC.
0 0 1	0 0 0 1 1 0 0 0	Message out complete; sent one message byte; ATN on.

Enable Selection/Reselection

After receiving this command, the FSC will respond to bus initiated selection or reselection. A command that causes the FSC to select or reselect will cancel this command. This command must be re-issued within 250 ms after the FSC disconnects to preserve ANSI recommended timings. If DMA is enabled, incoming information will be placed in memory. If DMA is not enabled, incoming information will remain in the FIFO.

Table 5-7. Target Selected without ATN Sequence

Sequence Step	Interrupt Register	Interpretation
2 1 0	**7 6 5 4 3 2 1 0**	
0 0 0	0 0 0 0 0 0 0 1	Selected, loaded bus ID into FIFO, loaded null-byte message into FIFO.
0 0 1	0 0 0 0 0 0 0 1	Stopped in Command phase due to parity error; some command descriptor block bytes may not have been received; check FIFO flags.
0 0 1	0 0 0 1 0 0 0 1	Same as above, initiator asserted ATN during Command phase
0 1 0	0 0 0 0 0 0 0 1	Selected, received entire command descriptor block; check Valid Group Code bit.
0 1 0	0 0 0 1 0 0 0 1	Same as above, initiator asserted ATN during Command phase.

Table 5-8. Target Selected with ATN Sequence (SCSI-2 Bit Not Set)

Sequence Step	Interrupt Register	Interpretation
2 1 0	**7 6 5 4 3 2 1 0**	
0 0 0	0 0 0 0 0 0 1 0	Selected with ATN, stored bus ID and one message byte; stopped due either to parity error or invalid ID message.
0 0 0	0 0 0 1 0 0 1 0	Selected with ATN, stored bus ID and one message byte; stopped because ATN remained true after first message byte.
0 0 1	0 0 0 0 0 0 1 0	Stopped in Command phase due to parity error; some CDB bytes not received; check Valid Group Code bit and FIFO flags.
0 0 1	0 0 0 1 0 0 1 0	Stopped in Command phase; parity error and ATN true.
0 1 0	0 0 0 0 0 0 1 0	Selection complete; received one message byte and the entire command descriptor block.
0 1 0	0 0 0 1 0 0 1 0	Same as above, initiator asserted ATN during Command phase.

Table 5-9. Target Selected with ATN Sequence (SCSI-2 Bit Set)

Sequence Step	Interrupt Register	Interpretation
2 1 0	7 6 5 4 3 2 1 0	
0 0 0	0 0 0 0 0 0 1 0	Selected with ATN, stored bus ID and one message byte; stopped due to either parity error or invalid ID message.
0 0 1	0 0 0 0 0 0 1 0	Initiator released ATN after one message byte received. Stopped in Command phase due to parity error; some CDB bytes not received; check Valid Group Code bit and FIFO flags.
0 0 1	0 0 0 1 0 0 1 0	Initiator released ATN after one message byte received. Stopped in Command phase; parity error and ATN true.
0 1 0	0 0 0 0 0 0 1 0	Initiator released ATN after one message byte received. Selection complete; received one message byte and the entire command descriptor block.
0 1 0	0 0 0 1 0 0 1 0	Same as above, initiator asserted ATN during Command phase.
1 0 0	0 0 0 0 0 0 1 0	Parity error during second or third message byte.
1 0 0	0 0 0 1 0 0 1 0	ATN remained true after third message byte.
1 0 1	0 0 0 0 0 0 1 0	Received 3 message bytes then stopped in Command phase due to parity error; some CDB bytes not received; check Valid Group Code bit and FIFO flags.
1 0 1	0 0 0 1 0 0 1 0	Stopped in Command phase; parity error and ATN true.
1 1 0	0 0 0 0 0 0 1 0	Selection complete; received three message bytes and the entire command descriptor block.

Disable Selection/Reselection

This command disables an earlier Enable Selection/Reselection command. If bus initiated selection or reselection has not begun when this command is received by the FSC, it will generate a Function Complete interrupt. If bus initiated selection or reselection has begun, this command (and all other commands) will be ignored. Refer to *Bus Initiated Selection* and *Bus Initiated Reselection* in Chapter Two, *Functional Description.*

Once this command is loaded into the Command register (at address 03h), any bus-initiated selection or reselection that is already requested begins immediately. Since there is no delay in execution of the selection or reselection, the Function Complete Interrupt bit will not be set inadvertently if the selection or reselection sequence continues after this command has been loaded.

Select With ATN3 Sequence

This command is similar to the Select With ATN command, but sends three message bytes instead of one. It will cause the FSC initiator to arbitrate for the bus, select a device with ATN asserted, send three Message phase bytes, deassert ATN, then send 6, 10 or 12 command phase bytes. The message and command bytes must have either been placed in the FIFO by the microprocessor or must be transferred by DMA. This involves setting the transfer count to 9, 13 or 15 and programming the external DMA controller. In either case, the Time-Out and Destination ID registers (at addresses 05h and 04h) must have previously been programmed. This command terminates early if a selection time-out occurs, the target does not assert Message Out phase followed by Command phase, or the target removes Command phase early. If it completes normally, a Function Complete and Bus Service interrupt will be generated.

Reselect3 Sequence

This command reselects an initiator and sends three message bytes: a one-byte Identify Message and a two-byte Queue Tag message. If DMA is not enabled, the three message bytes must be loaded into the FIFO before this command is issued.

Table 5-10. Initiator Select with ATN3 Sequence

Sequence Step	Interrupt Register	Interpretation
2 1 0	7 6 5 4 3 2 1 0	
0 0 0	0 0 1 0 0 0 0 0	Arbitration complete; selection time-out; disconnected.
0 0 0	0 0 0 1 1 0 0 0	Arbitration and selection complete; stopped because target did not assert Message Out phase; ATN still asserted by FSC.
0 1 0	0 0 0 1 1 0 0 0	Sent 1, 2 or 3 message bytes; stopped because target prematurely changed from Message Out phase or did not assert Command phase after third message byte; ATN released only if third message byte was sent.
0 1 1	0 0 0 1 1 0 0 0	Stopped during command transfer due to premature phase change; some CDB bytes may not have been sent; check FIFO flags.
1 0 0	0 0 0 1 1 0 0 0	Selection With ATN3 Sequence complete. Three message bytes and all command bytes were sent.

Initiator Command Group

If the FSC is not in initiator state when it receives one of these commands, the command will be ignored, an Illegal Command interrupt will be generated and the Command register will be cleared. Refer to the description of the Command register (03h) in Chapter Four, *Registers*.

If BSY is deasserted while the FSC is connected as an initiator, it will generate a disconnected interrupt. The interrupt output will occur 1.5 to 3.5 CLK cycles after BSY goes false.

When the FSC receives the last byte of a Message In phase, it will leave ACK asserted on the bus to prevent the target from sending any more bytes until the initiator decides to accept or reject the message. If the initiator accepts the command, it will issue a Message Accepted command. If the initiator does not accept the message, a Set ATN command should be issued before the Message Accepted command, causing the target to change to Message Out phase. For non-DMA commands, an empty FIFO means that the last byte has been sent. For DMA commands, the transfer counter signals the last byte.

If parity checking is enabled and the FSC detects a parity error while in Initiator mode, it will automatically assert ATN prior to deasserting ACK for the byte which has the error. The one exception is after a phase change to Synchronous Data In, and is described as follows.

If the Synchronous Offset register (07h) is non-zero (synchronous) and the phase changes to Data In, the DMA interface is immediately disabled and the reporting of a parity error during Data In phase is delayed. The phase change to Data In will: latch the FIFO flags to indicate how many bytes were in the FIFO (these bytes will be lost); clear the FIFO; load the FIFO with the first Data In byte; generate an interrupt; and continue to load the FIFO with incoming Data In bytes as long as the target sends them, but not more than the specified offset. To continue receiving Data In bytes, the microprocessor would normally issue the Transfer Information command to re-enable the DMA interface. If parity checking is enabled and a parity error occurred on a previous input phase (Message In or Status), then the parity error flag will be set in the Status register and ATN will be set on the SCSI bus. If a parity error occurred during the Data In phase, the parity bit will not be set nor will ATN be asserted until after the FSC receives the subsequent Transfer Information command.

Table 5-11. Initiator Commands

DMA	Non-DMA	Mnemonic
90	10	Transfer Information
91	11	Initiator Command Complete Sequence
-	12	Message Accepted
98	-	Transfer Pad
-	1A	Set ATN (Attention)
-	1B	Reset ATN

Transfer Information

This command can be used to send or receive any Information phase bytes, but is most often used for data transfer. **Note:** For synchronous transfer, DMA must be used. The FSC will continue to transfer information until one of the following terminating events occurs:

- Transfer is complete. Successful completion will generate a Bus Service interrupt. For a DMA Transfer Information, the transfer is complete when the transfer counter decrements to zero, the FIFO is empty and the target asserts REQ for the next byte. For non-DMA Transfer Information in which the FSC is sending bytes to the SCSI bus, the

transfer is complete when the FIFO empties and the target asserts REQ for the next byte. For non-DMA Transfer Information in which the FSC is receiving bytes from the SCSI bus, transfer is complete after one byte is received and the target asserts REQ for the next byte. Thus non-DMA Transfer Information commands will generate an interrupt for every byte received.

- If the phase is Message Out, the FSC removes ATN prior to asserting ACK for the last byte of the message. For non-DMA, the FIFO flags indicate the last byte. For DMA, the transfer counter indicates the last byte.
- Target changes phase. The FSC clears the Command register (03h) and generates a Bus Service interrupt after the target asserts REQ for the next byte.
- Target releases BSY (Busy). The FSC generates a Disconnected interrupt.
- The FSC receives the last byte of a Message In phase. (For non-DMA every byte is assumed to be the last byte. For DMA, the transfer counter signals the last byte). The FSC leaves ACK asserted and generates a Function Complete interrupt.

  All Message In and Status phase transfers are handled one byte at a time. If DMA is enabled, the next byte will not be received until the current byte has been written to buffer memory and the FIFO is empty. If DMA is not enabled, each byte will create an interrupt.

Initiator Command Complete Sequence

This command will cause the FSC to receive a status byte followed by a message byte. It terminates early if the target does not assert Message In phase, or if the target disconnects. After receiving the message byte, the FSC leaves ACK asserted on the bus to allow the initiator to assert ATN if the message is unacceptable.

Message Accepted

This command deasserts the ACK signal on the SCSI bus. Any of the commands that receive bytes during message phase will leave ACK asserted after receiving the last message byte. To accept the message, issue this command. To reject the message, set ATN then issue this command.

Transfer Pad

Transfer Pad is usually an error recovery technique. It is useful when a target requests more bytes than an initiator has to send, or when an initiator must receive and discard a number of bytes from a target.

When transmitting to the SCSI bus, Transfer Pad will fill the FIFO with null bytes and send them to the SCSI bus. When receiving from the SCSI bus, Transfer Pad will receive bytes, place them on the top of the FIFO and discard them from the bottom of the FIFO.

When sending pad bytes to the SCSI bus, DMA must be enabled. No DMA requests are actually made, but the FSC uses the transfer counter to end the transfer.

The command terminates under the same conditions as the Transfer Information command, except that the FSC does not leave ACK asserted on the last byte of a Message In phase. If the command terminates before the transfer counter reaches zero (due to phase change or disconnect) the FIFO may contain pad bytes.

Set ATN

This command asserts attention on the SCSI bus. No interrupt is generated from this command. ATN stays asserted until the last byte of a message out phase. This command will not preempt a command in progress; attention will be asserted after the current command is completed.

DMA commands use the transfer counter to indicate the last byte. For non-DMA commands, the last byte means that the FIFO is empty. For DMA transfers, the last byte means that the transfer counter is zero. ATN will also be released if the target disconnects prematurely.

Reset ATN

This command causes ATN to be released. It does not cause an interrupt.

Note: This command should not normally be used when connected to a SCSI-2 device. The FSC obeys SCSI-2 protocol by releasing ATN on the last byte of a Message Out phase. The Reset ATN command is provided for devices which do not respond properly to the ATN condition.

Target Command Group

If the FSC receives any of these commands when it is not in target state, it will ignore the command, clear the Command register, and generate an Illegal Command interrupt. Refer to the Command register (03h) description in Chapter Four.

Normal completion of these commands will cause a Function Complete interrupt. If ATN is asserted, the Bus Service bit will be set in the Status register and an interrupt will be generated. If the FSC was idle when ATN was asserted, a Bus Service interrupt will be generated, the Function Complete bit will be zero, and the Command register will be cleared.

Table 5-12. Target Commands

DMA	Non-DMA	Mnemonic
A0	20	Send Message
A1	21	Send Status
A2	22	Send Data
A3	23	Disconnect Sequence
A4	24	Terminate Sequence
A5	25	Target Command Complete Sequence
-	27	Disconnect
A8	28	Receive Message
A9	29	Receive Command
AA	2A	Receive Data
AB	2B	Receive Command Sequence
-	04	Target Abort DMA

Send Message

This command will cause the FSC to assert Message In phase and send bytes until the FIFO is empty or the transfer counter is zero (if DMA).

Send Data

This command will cause the FSC to assert Data In phase and send bytes until the FIFO is empty or the transfer counter is zero (if DMA).

Send Status

This command will cause the FSC to assert Status phase and send bytes until the FIFO is empty or the transfer counter is zero (if DMA).

Disconnect Sequence

This command will cause the FSC to assert Message In phase, send two bytes, then disconnect from the SCSI bus. Normally, the first byte will be a Save Data Pointers message and the second will be a Disconnect message. These bytes must be loaded into the FIFO by the microprocessor, or may be loaded by DMA. If ATN is asserted by the initiator, the Bus Service and Function Complete bits will be set and an interrupt will be generated, but the FSC will not disconnect.

Table 5-13. Target Disconnect Sequence

Sequence Step	Interrupt Register	Interpretation
2 1 0	**7 6 5 4 3 2 1 0**	
0 0 0	0 0 0 1 1 0 0 0	Sent one message byte; stopped because initiator set ATN.
0 0 1	0 0 0 1 1 0 0 0	Sent two message bytes; stopped because initiator set ATN.
0 1 0	0 0 1 0 1 0 0 0	Disconnect Sequence complete; disconnected, bus is free.

Table 5-14. Target Terminate Sequence

Sequence Step	Interrupt Register	Interpretation
2 1 0	**7 6 5 4 3 2 1 0**	
0 0 0	0 0 0 1 1 0 0 0	Sent one status byte; stopped because initiator set ATN.
0 0 1	0 0 0 1 1 0 0 0	Sent status and message bytes; stopped because initiator set ATN.
0 1 0	0 0 1 0 1 0 0 0	Terminate Sequence complete; disconnected, bus is free.

Terminate Sequence

This command will cause the FSC to first assert Status phase, send one byte; then assert Message In phase, send one more byte, and disconnect. These bytes must be loaded into the FIFO by the microprocessor, or may be loaded by DMA. If ATN is asserted by the initiator, the Bus Service and Function Complete bits will be set and an interrupt will be generated, but the FSC will not disconnect. If ATN is not asserted by the initiator, a disconnect interrupt is generated.

Target Command Complete Sequence

This command is similar to Terminate Sequence, but is used for linked commands. It will cause the FSC to first assert Status phase, send one byte, then assert Message In phase and send one more byte. The message byte will normally be a Command Complete message. If ATN is asserted by the initiator, the Bus Service and Function Complete bits will be set and an interrupt will be generated, but the FSC will not disconnect. If ATN is not asserted by the initiator, a function complete interrupt is generated.

Table 5-15. Target Command Complete Sequence

Sequence Step	Interrupt Register	Interpretation
2 1 0	7 6 5 4 3 2 1 0	
0 0 0	0 0 0 1 1 0 0 0	Sent one status byte; stopped because initiator set ATN.
0 0 1	0 0 0 1 1 0 0 0	Sent status and message bytes; stopped because initiator set ATN.
0 1 0	0 0 0 0 1 0 0 0	Command Complete Sequence complete.

Disconnect

This command causes the FSC to release all SCSI bus signals except RSTO (once triggered, RSTO is driven true for 25 µs or so, depending on CLK frequency and clock conversion factor). The FSC returns to the Disconnected state without generating an interrupt.

Receive Message

This command will cause the FSC to assert Message Out phase and receive one byte, then generate a function complete interrupt.

Receive Command

This command will cause the FSC to assert Command phase and receive bytes from the initiator. For non-DMA Receive command, only one byte per interrupt may be received. DMA Receive Command will interrupt after the transfer counter decrements to zero. This command terminates by generating a function complete interrupt.

Receive Data

This command will cause the FSC to assert Data Out phase and receive bytes from the initiator. For non-DMA Receive Data, only one byte per interrupt may be received. DMA Receive Data will interrupt after the transfer counter decrements to zero. This command terminates by generating a function complete interrupt.

Receive Command Sequence

This command will cause the FSC to assert Command phase and receive a number of bytes, which will vary according to the group code field of the first byte. If the SCSI-2 bit is set in the Configuration 2 register (0Bh), Group 2 commands will be recognized as 10-byte commands. If the SCSI-2 bit is cleared, Group 2 commands will be recognized as reserved commands. Groups 3 and 4 are always reserved. The FSC will request six bytes for reserved commands, six bytes for Group 6 vendor unique commands, and 10 bytes for Group 7 vendor unique commands.

Table 5-16. Target Receive Command Sequence

Sequence Step	Interrupt Register	Interpretation
2 1 0	**7 6 5 4 3 2 1 0**	
0 0 1	0 0 0 0 1 0 0 0	Stopped during command transfer due to parity error; check FIFO flags.
0 0 1	0 0 0 1 1 0 0 0	Stopped during command transfer due to parity error; ATN asserted by initiator.
0 1 0	0 0 0 0 1 0 0 0	Received entire command descriptor block.
0 1 0	0 0 0 1 1 0 0 0	Received entire CDB, initiator asserted ATN.

Target Abort DMA

The Target Abort DMA command allows the microprocessor to stop a target data transfer command whose progress has been halted due to inactivity on the DMA channel. One potential application is a system containing a microprocessor and an intelligent buffer controller that handles buffer management. The microprocessor sets up the buffer controller and over-programs the transfer counter prior to issuing a SCSI transfer command to the chip. When the buffer controller runs out of buffers, it interrupts the microprocessor. The microprocessor stops the chip and commands it to disconnect from the SCSI bus.

Note: The Target Abort DMA command should be used with extreme caution. Before using this command, verify that the removal of DREQ by this command does not confuse the system's DMA controller.

The abort DMA command executes from the top of the command FIFO. If there is a stacked command waiting to execute, it is overwritten and the Gross Error bit (bit 6 in the Status register) is set. The abort DMA command clears itself from the command stack after being decoded.

The abort DMA command can only be used when all of the following conditions are true:

1) Either the Target Send Data or Target Receive Data command is operating
2) The DMA controller has halted
3) The chip is in a steady state:

   Send Data - the DMA FIFO is empty

   Receive Asynchronous Data - The FIFO is full (FIFO Flags Register = 10h), or the Transfer Counter is zero (Status Register bit 4 = 1)

   Receive Synchronous Data - The Transfer Counter is zero, or the Offset Counter is at maximum value (Sequence Step Register bit 3 = 0)

When these conditions are true, the chip halts with DREQ asserted. If the chip is in Synchronous Transfer mode when halted, some ACK responses from the SCSI bus may not have been received and remain outstanding. Upon receiving the Abort DMA command, the chip resets the DMA interface, including the DREQ output pin, and terminates the command in progress. The chip completes any ongoing SCSI process. Send Asynchronous Data transfers complete immediately. Send Synchronous Data transfers complete when the offset counter is zero. Receive Asynchronous Data transfers complete immediately. Data left in the FIFO should be removed by the microprocessor. Receive Synchronous Data operations complete when all outstanding SCSI ACKs have been received. No extra bits are set in the Interrupt or Status registers (at addresses 05h and 04h). The microprocessor receives the interrupt from the command that was in progress, and the command FIFO is cleared.

Chapter Six
Electrical Characteristics

Absolute Maximum Stress Ratings

Symbol	Parameter	Min	Max	Unit	Test Condition
T_{STG}	Storage Temperature	-55	150	°C	-
V_{DD}	Supply Voltage	-0.5	7.0	V	-
V_{IN}	Input Voltage	V_{SS}-0.5	V_{DD}+0.5	V	-
I_{LP}	Latch-up Current	-100	100	mA	-2V < V_{PIN} < +8V
ESD	Electrostatic Discharge	TBD	-	V	-

Note: Conditions that exceed the Absolute Maximum limits may destroy the device. Conditions that exceed the Operating limits may cause the device to function incorrectly.

Operating Conditions

Symbol	Parameter	Min	Max	Unit	Test Condition
V_{DD}	Supply Voltage	4.5	5.5	V	-
I_{DD}	Supply Current	-	4	mA	Static*
I_{DD}	Supply Current	-	TBD	mA	Dynamic
T_A	Ambient Temperature	0	70	°C	-
U_{JA}	Thermal Resistance, junction/ambient				
	68-pin PLCC	-	39.97	°C/V	-
	80-pin PQFP	-	50.00	°C/V	-

* *Static means all inputs are deasserted, all outputs floating, and all bidirectional pins configured as inputs.*

DC Electrical Characteristics

Inputs: A3-A0, WR/, DIFFM

Symbol	Parameter	Min	Max	Unit	Test Condition
V_{IH}	Input High Voltage	2	V_{DD} + 0.5	V	-
V_{IL}	Input Low Voltage	V_{SS} - 0.5	0.8	V	-
I_{IN}	Input Leakage Current	-10	10	µA	$0 < V_{IN} < V_{DD}$
C_{IN}	Capacitance	-	10	pF	-

Inputs: CS/, RD/, DACK/,CLK, RESET

Symbol	Parameter	Min	Max	Unit	Test Condition
V_{IH}	Input High Voltage	2	V_{DD} + 0.5	V	-
V_{IL}	Input Low Voltage	V_{SS} - 0.5	0.8	V	-
V_{H}	Hysteresis	200	700	mV	-
I_{IN}	Input Leakage Current	-10	10	µA	$0 < V_{IN} < V_{DD}$
C_{IN}	Capacitance	-	10	pF	-

Inputs: ATNI/, ACKI/, BSYI/, REQI/, RSTI/, SELI/, MSGI/, CDI/, I_O/

Symbol	Parameter	Min	Max	Unit	Test Condition
V_{IH}	Input High Voltage	2	V_{DD} + 0.5	V	-
V_{IL}	Input Low Voltage	V_{SS} - 0.5	0.8	V	-
V_{H}	Hysteresis	200	700	mV	-
I_{IL}	Input Leakage Current	-10	10	µA	$0 < V_{IN} < V_{DD}$
C_{IN}	Capacitance	-	10	pF	-

Outputs: DREQ, IGS

Symbol	Parameter	Min	Max	Unit	Test Condition
V_{OH}	Output High Voltage	2.4	-	V	I_{OH} = -4mA
V_{OL}	Output Low Voltage	-	0.4	V	I_{OL} = 4 mA
I_{OZ}	High-Z State Leakage	-10	10	µA	$0 < V_{OUT} < V_{DD}$
C_{OUT}	Capacitance	-	10	pF	-

Outputs: INT/

Symbol	Parameter	Min	Max	Unit	Test Condition
V_{OL}	Output Low Voltage	-	0.4	V	I_{OL} = 4 mA
I_{OZ}	High-Z State Leakage	-10	10	µA	$0 < V_{OUT} < V_{DD}$
C_{OUT}	Capacitance	-	10	pF	-

Outputs: RESETO

Symbol	Parameter	Min	Max	Unit	Test Condition
V_{OH}	Output High Voltage	2.4	-	V	I_{OH} = -8mA
V_{OL}	Output Low Voltage	-	0.4	V	I_{OL} = 8 mA
I_{OZ}	High-Z State Leakage	-10	10	µA	$0 < V_{OUT} < V_{DD}$
C_{OUT}	Capacitance	-	10	pF	-

Outputs: ACKO/, ATNO/, REQO/, BSYO/, RSTO/, SELO/, MSGO/, CDO/, I_OO/, SDOP/, SDO7/-SDO0/

Symbol	Parameter	Min	Max	Unit	Test Condition
V_{OL}	Output Low Voltage	-	0.5	V	I_{OL} = 48 mA
I_{OZ}	High-Z State Leakage	-10	10	µA	$0 < V_{OUT} < V_{DD}$
S_{FT}	Signal Fall Time	4	-	ns	SCSI Termination
C_{OUT}	Capacitance	-	10	pF	-

Bidirectional Pins: DB7-DB0, DBP*

Symbol	Parameter	Min	Max	Unit	Test Condition
V_{IH}	Input High Voltage	2	V_{DD} + 0.5	V	-
V_{IL}	Input Low Voltage	V_{SS} - 0.5	0.8	V	-
I_{IL}	Input Low Leakage	-600	-75	µA	V_{IN} = 0
I_{IH}	Input High Leakage	0	20	µA	V_{IN} = V_{DD}
V_{OH}	Output High Voltage	2.4	-	V	I_{OH} = -4mA
V_{OL}	Output Low Voltage	-	0.4	V	I_{OL} = 4 mA
C_{IO}	Capacitance	-	10	pF	-

* *DBP applies to the 53CF90B only.*

Bidirectional Pins: SDIP/, SDI7/-SDI0/

Symbol	Parameter	Min	Max	Unit	Test Condition
V_{IH}	Input High Voltage	2	V_{DD} + 0.5	V	-
V_{IL}	Input Low Voltage	V_{SS} - 0.5	0.8	V	-
V_{H}	Hysteresis	200	700	mV	-
I_{IN}	Input Current	0	10	µA	$0 < V_{IN} < V_{DD}$
V_{OH}	Output High Voltage	2.4	-	V	I_{OH} = -4mA
V_{OL}	Output Low Voltage	-	0.4	V	I_{OL} = 4 mA
C_{IO}	Capacitance	-	10	pF	-

Bidirectional Pins: TGS*

Symbol	Parameter	Min	Max	Unit	Test Condition
V_{IH}	Input High Voltage	2	V_{DD} + 0.5	V	-
V_{IL}	Input Low Voltage	V_{SS} - 0.5	0.8	V	-
I_{IL}	Input Low Leakage	-600	-75	µA	V_{IN} = 0
I_{IH}	Input High Leakage	0	20	µA	V_{IN} = V_{DD}
V_{OH}	Output High Voltage	2.4	-	V	I_{OH} = -8mA
V_{OL}	Output Low Voltage	-	0.4	V	I_{OL} = 8 mA
C_{IO}	Capacitance	-	10	pF	-

* *In the 53CF90A, TGS is an output signal only.*

AC Electrical Characteristics

The AC characteristics described in this section apply over the operating voltage V_{DD} equal to 5 V ± 5%, and the temperature range 0 to 70 °C. Output timing is based on simulation under worst case conditions (4.75 v, 70 °C), and worst case processing, using the termination values listed below. All timings in this specification are taken from the 10% and 90% points with respect to the specified V_{OL} and V_{OH} of the waveforms.

Pin	Termination
DREQ, TGS, IGS, RESETO SDIP/, SDI7/-SDI0/	50 pF
INT/	50 pF, 1 KΩ pullup
DB7-DB0, DBP	85 pF
RSTO/, SELO/, BSYO/, ATNO/, MSGO/, CDO/, I_OO/, REQO/, ACKO/, SDOP/, SDO7/-SDO0/	200 pF, 110 Ω pullup, 165 Ω pulldown

System Interface Timing

Clock Input

Symbol	Parameter	Min	Max	Unit	Note
t_{CP}	Clock Period (1÷ Freq)	-	-	ns	-
t_{CS}	Synchronization Latency	t_{CL}	$t_{CL} + t_{CP}$	ns	-

Symbol	Parameter (FASTCLK bit cleared)	Min	Max	Unit	Note
t_{CPA}	Clock Frequency, Async	12	25	MHz	-
t_{CPS}	Clock Frequency, Sync	20	25	MHz	-
t_{CH}	Clock High	14.58	$0.65 \cdot t_{CP}$	ns	1
t_{CL}	Clock Low	14.58	$0.65 \cdot t_{CP}$	ns	1

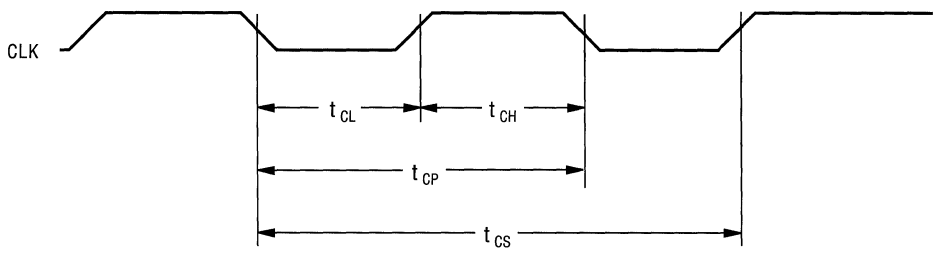
Symbol	Parameter (FASTCLK bit set)	Min	Max	Unit	Note
t_{CPA}	Clock Frequency, Async	20	40	MHz	-
t_{CPS}	Clock Frequency, Sync	38	40	MHz	-
t_{CH}	Clock High	$0.40 \cdot t_{CP}$	$0.60 \cdot t_{CP}$	ns	-
t_{CL}	Clock Low	$0.40 \cdot t_{CP}$	$0.60 \cdot t_{CP}$	ns	-

1 *For synchronous SCSI transfers and FASTCLK disabled, the clock must meet the following requirements:*

$2 \cdot t_{CP} + t_{CL} \geq 97.92\ ns$

$2 \cdot t_{CP} + t_{CH} \geq 97.92\ ns$

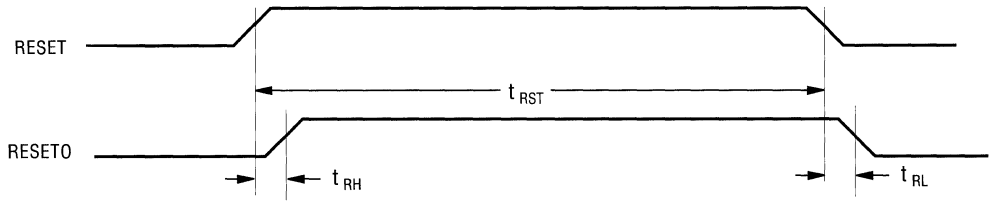
Figure 6-1. Clock Input



Reset Input

Symbol	Parameter	Min	Max	Unit	Note
t_{RST}	RESET pulse width	200	-	ns	-
t_{RH}	RESET high to RESETO high	-	50	ns	-
t_{RL}	RESET low to RESETO low	-	50	ns	-

Figure 6-2. Reset Input

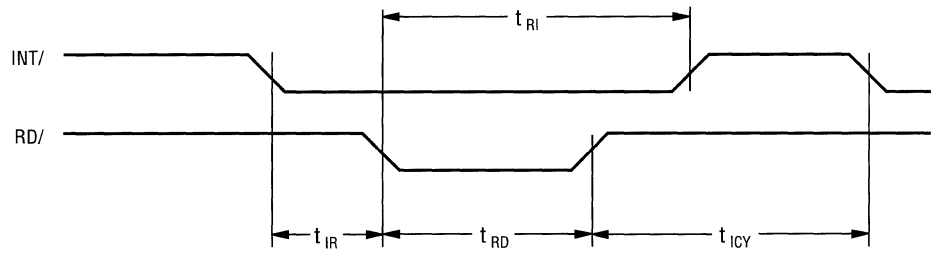


Interrupt Output

Symbol	Parameter	Min	Max	Unit	Note
t_{IR}	INT/ low to RD/ low	0	-	ns	1
t_{RD}	RD/ pulse width	25	-	ns	2
t_{RI}	RD/ low to INT/ high	-	75	ns	-
t_{ICY}	RD/ high to INT/ low	t_{CS}	-	ns	-

1 *The Interrupt register should not be read when INT/ is false.*
2 *Refer to the register read specifications for timing requirements of CS/, RD/, and address for reading the Interrupt register.*

Figure 6-3. Interrupt Output



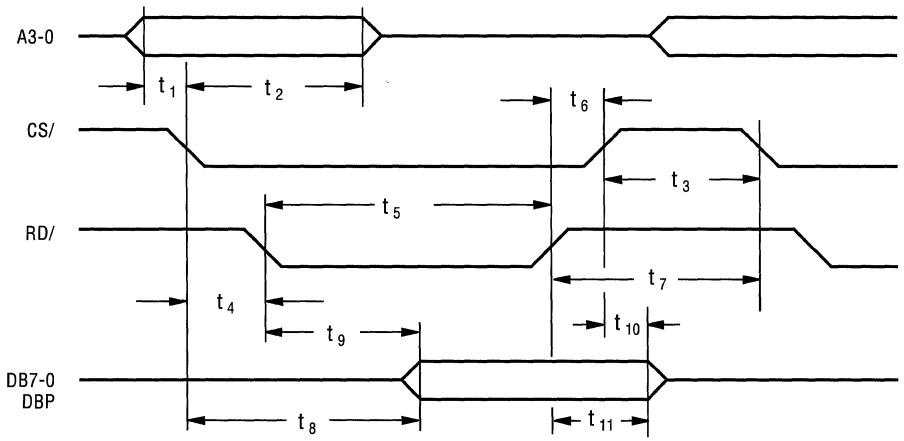
Register Interface Timing

Register Read Cycle

Symbol	Parameter	Min	Max	Unit	Note
t_1	Address setup to CS/ low	0	-	ns	-
t_2	Address Hold from CS/ low	50	-	ns	-
t_3	CS/ high to CS/ low	40	-	ns	-
t_4	CS/ low to RD/ low	0	-	ns	-
t_5	RD/ pulse width	25	-	ns	-
t_6	RD/ high to CS/ high	0	-	ns	-
t_7	RD/ high to CS/ low	40	-	ns	-
t_8	CS/ low to data valid	0	40	ns	1
t_9	RD/ low to data valid	0	25	ns	1
t_{10}	CS/ high to data release	2	25	ns	2
t_{11}	RD/ high to data release	2	25	ns	2

1 *Both t_8 and t_9 specifications must be met.*
2 *RD/ edges may precede or follow CS/ edges.*

Figure 6-4. Register Read Cycle Timing

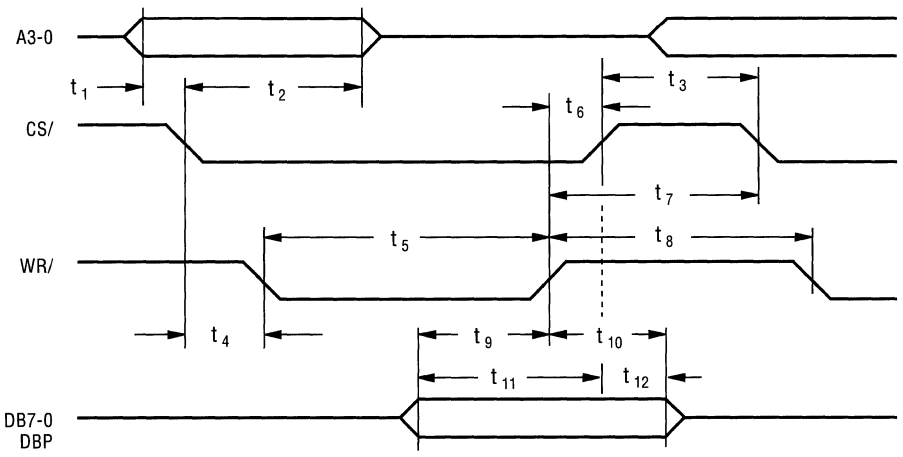


Register Write Cycle

Symbol	Parameter	Min	Max	Unit	Note
t_1	Address setup to CS/ low	0	-	ns	-
t_2	Address Hold from CS/ low	50	-	ns	-
t_3	CS/ high to CS/ low	40	-	ns	1
t_4	CS/ low to WR/ low	0	-	ns	2
t_5	WR/ pulse width	25	-	ns	-
t_6	WR/ high to CS/ high	0	-	ns	2
t_7	WR/ high to CS/ low	40	-	ns	-
t_8	WR/ high to WR/ low	40	-	ns	1
t_9	Data setup to WR/ high	8	-	ns	3
t_{10}	Data hold from WR/ high	0	-	ns	4
t_{11}	Data setup to CS/ high	10	-	ns	3
t_{12}	Data hold from CS/ high	35	-	ns	4

1 *If WR/ is held low t_3 is 35 ns (min).*
2 *WR/ edges may precede or follow CS/ edges.*
3 *Either t_9 or t_{11} specification must be met.*
4 *Either t_{10} or t_{12} specification must be met.*

Figure 6-5. Register Write Cycle Timing



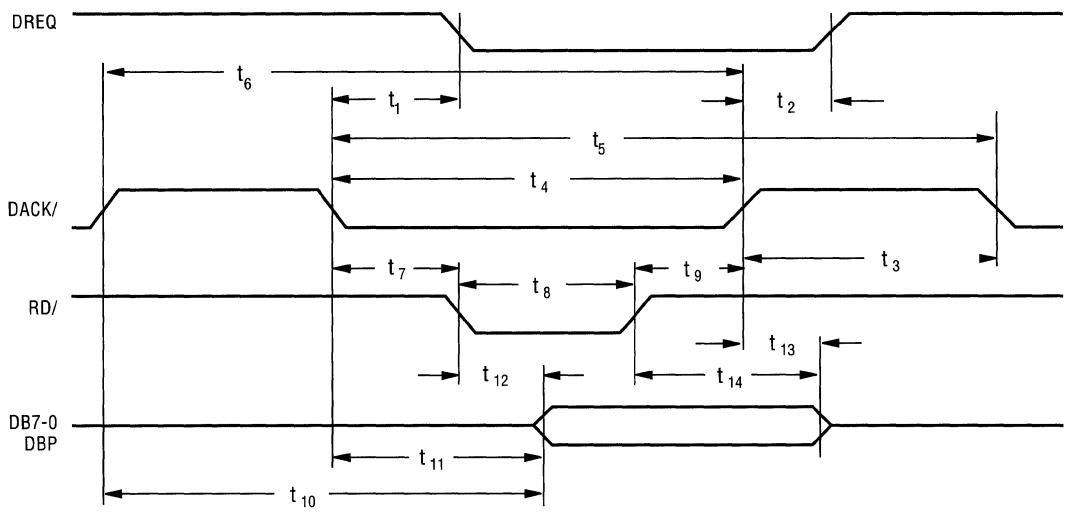
DMA Interface Timing

DMA Read Cycle

Symbol	Parameter	Min	Max	Unit	Note
t_1	DACK/ low to DREQ low	-	20	ns	1
t_2	DACK/ high to DREQ high	-	20	ns	2
t_3	DACK/ high to DACK/ low	12	-	ns	-
t_4	DACK/ pulse width	35	-	ns	-
t_5	DACK/ low to DACK/ low	75	-	ns	-
t_6	DACK/ high to DACK/ high	$t_{CS} + 30 - t_3$ and $2t_{CP}$	-	ns	3, 4
t_6	DACK/ high to DACK/ high	$2t_{CS} + 35 - t_3$ and $3t_{CP}$	-	ns	3, 5
t_7	DACK/ low to RD/ low	0	-	ns	6
t_8	RD/ pulse width	t_{12}	-	ns	-
t_9	RD/ high to DACK/ high	0	-	ns	7
t_{10}	DACK/ high to data valid	-	30	ns	8
t_{11}	DACK/ low to data valid	-	25	ns	8
t_{12}	RD/ low to data valid	-	25	ns	8
t_{13}	DACK/ high to data release	2	25	ns	-
t_{14}	RD/ high to data release	2	25	ns	-

1 *Negation pending.*
2 *Assertion pending.*
3 *Synchronous transfers only.*
4 *FASTCLK disabled.*
5 *FASTCLK enabled.*
6 *RD/ low may precede DACK/ low.*
7 *RD/ high may follow DACK/ high.*
8 *Both t_{10} and t_{11} specifications must be met.*

Figure 6-6. DMA Read Cycle Timing

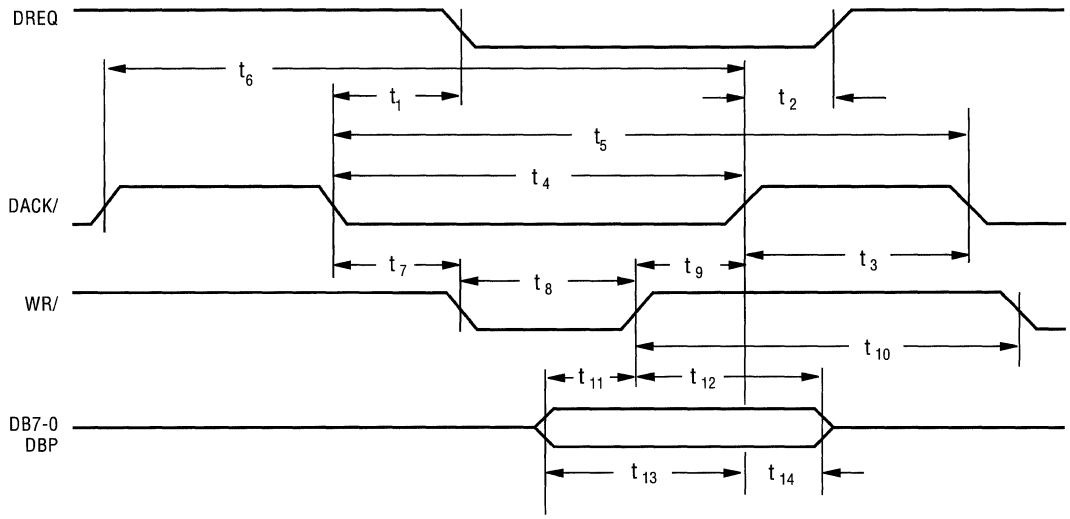


DMA Write Cycle

Symbol	Parameter	Min	Max	Unit	Note
t_1	DACK/ low to DREQ low	-	20	ns	1
t_2	DACK/ high to DREQ high	-	20	ns	2
t_3	DACK/ high to DACK/ low	12	-	ns	3
t_4	DACK/ pulse width	35	-	ns	-
t_5	DACK/ low to DACK/ low	75	-	ns	-
t_6	DACK/ high to DACK/ high	$t_{CS} + 30 - t_3$ and $2t_{CP}$	-	ns	4, 5
t_6	DACK/ high to DACK/ high	$2t_{CS} + 35 - t_3$ and $3t_{CP}$	-	ns	4, 6
t_7	DACK/ low to WR/ low	0	-	ns	7
t_8	WR/ pulse width	30	-	ns	-
t_9	WR/ high to DACK/ high	0	-	ns	8
t_{10}	WR/ high to WR/ low	30	-	ns	-
t_{11}	Data setup to WR/ high	8	-	ns	9
t_{12}	Data hold from WR/ high	0	-	ns	10
t_{13}	Data setup to DACK/ high	10	-	ns	9
t_{14}	Data hold from DACK/ high	10	-	ns	10

1 *Negation pending.*
2 *Assertion pending.*
3 *If WR/ is held low t_3 = 30 ns (min).*
4 *Synchronous transfers only.*
5 *FASTCLK disabled.*
6 *FASTCLK enabled.*
7 *WR// low may precede DACK/ low.*
8 *WR/ high may follow DACK/ high.*
9 *Either t_{11} or t_{13} specification must be met.*
10 *Either t_{12} or t_{14} specification must be met.*

Figure 6-7. DMA Write Cycle Timing



SCSI Interface Timing

SCSI Asynchronous Timing

Symbol	Parameter	Min	Max	Unit	Note
	SINGLE-ENDED MODE [1]				
t_1	ACKI/ low to REQO/ high	-	50	ns	-
t_2	ACKI/ high to REQO/ low	-	45	ns	3, 6
t_3	REQI/ high to ACKO/ high	-	50	ns	-
t_4	REQI/ low to ACKO/ low	-	50	ns	4, 6
	Output Cycle				
t_5	Data setup to REQO/ low	60	-	ns	-
t_5	Data setup to ACKO/ low	60	-	ns	-
t_6	Data hold from REQI/ high	5	-	ns	5
t_6	Data hold from ACKI/ low	5	-	ns	5
	DIFFERENTIAL MODE [2]				
t_1	ACKI/ low to REQO/ high	-	30	ns	-
t_2	ACKI/ high to REQO/ low	-	30	ns	3, 6
t_3	REQI/ high to ACKO/ high	-	25	ns	-
t_4	REQI/ low to ACKO/ low	-	30	ns	4, 6
	Output Cycle				
t_5	Data setup to REQO/ low	70	-	ns	-
t_5	Data setup to ACKO/ low	70	-	ns	-
t_6	Data hold from REQI/ high	5	-	ns	5
t_6	Data hold from ACKI/ high	5	-	ns	5
	INPUT CYCLE				
t_7	Data setup to REQI/ low	0	-	ns	-
t_7	Data setup to ACKI/ low	0	-	ns	-
t_8	Data hold from REQI/ low	-	18	ns	-
t_8	Data hold from ACKI/ low	-	18	ns	-

1 *200pF loading, data out on lines SDOP/, SDO7/-0/.*
2 *Data out on lines SDIP/, SDI7/-0/.*
3 *Data setup to REQO/ low specification must also be met (output cycle only).*
4 *Data setup to ACKO/ low specification must also be met (output cycle only).*
5 *FIFO is not empy.*
6 *FIFO is not full (input cycle only).*

Figure 6-8. SCSI Asynchronous Output

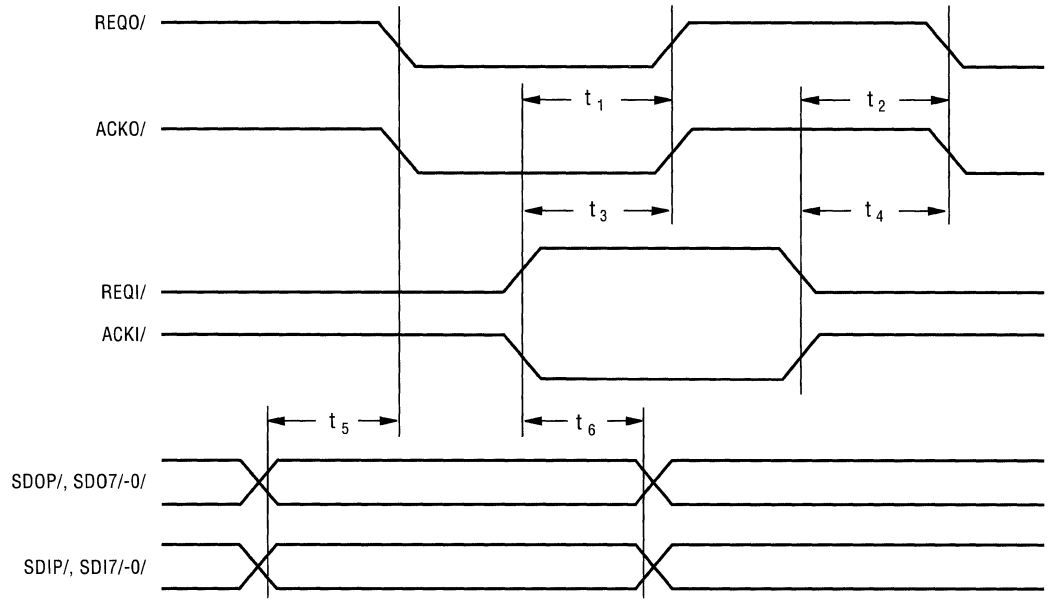
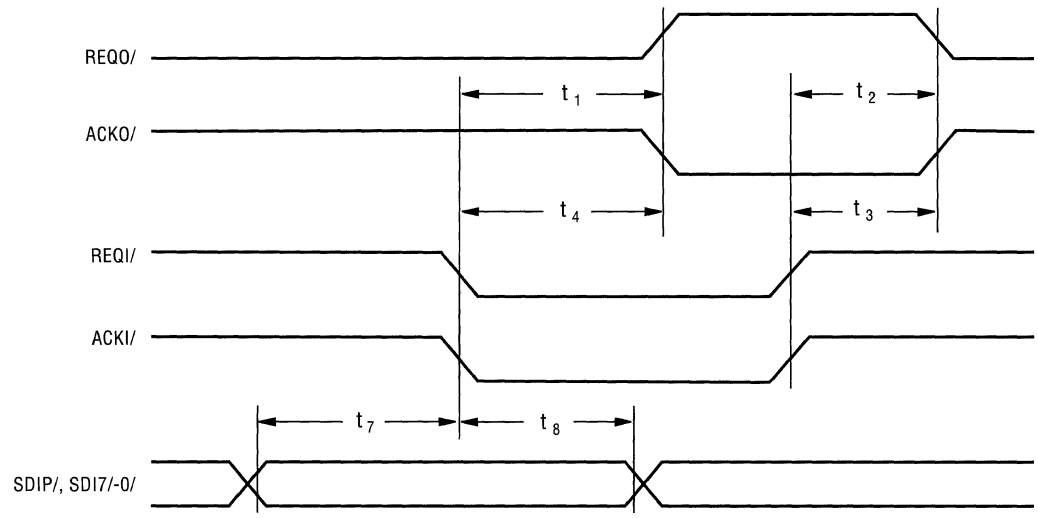


Figure 6-9. SCSI Asynchronous Input



SCSI Synchronous Timing

Symbol	Parameter	Min	Max	Unit	Note
	OUTPUT CYCLE				
	Normal SCSI, Single-Ended Mode [1]				
t_1	REQO/, ACKO/ assertion period	90	-	ns	-
t_2	REQO/, ACKO/ negation period	90	-	ns	-
t_3	Data setup to REQO/ low, ACKO/ low	55	-	ns	-
t_4	Data hold from REQO/ low, ACKO/ low	100	-	ns	-
	Normal SCSI, Differential Mode [2]				
t_1	REQO/, ACKO/ assertion period	96	-	ns	-
t_2	REQO/, ACKO/ negation period	96	-	ns	-
t_3	Data setup to REQO/ low, ACKO/ low	65	-	ns	-
t_4	Data hold from REQO/ low, ACKO/ low	110	-	ns	-
	Fast SCSI, Single-Ended Mode [3]				
t_1	REQO/, ACKO/ assertion period	30	-	ns	-
t_2	REQO/, ACKO/ negation period	30	-	ns	-
t_3	Data setup to REQO/ low, ACKO/ low	25	-	ns	-
t_4	Data hold from REQO/ low, ACKO/ low	35	-	ns	-
	Fast SCSI Differential Mode [4]				
t_1	REQO/, ACKO/ assertion period	40	-	ns	-
t_2	REQO/, ACKO/ negation period	40	-	ns	-
t_3	Data setup to REQO/ low, ACKO/ low	35	-	ns	-
t_4	Data hold from REQO/ low, ACKO/ low	45	-	ns	-
	INPUT CYCLE				
t_5	REQI/ assertion period	27	-	ns	-
t_6	REQI/ negation period	20	-	ns	-
t_7	ACKI/ assertion period	20	-	ns	-
t_8	ACKI/ negation period	20	-	ns	-
t_9	Data setup to REQI/ low, ACKI/ low	5	-	ns	-
t_{10}	Data hold from REQI/ low, ACKI/ low	15	-	ns	-

1 *5 MB/s max, data out lines SDOP/, SDO7/-0/.*
2 *5 MB/s max, data out on lines SDIP/, SDI7/-0/.*
3 *10 MB/s max, data out lines SDOP/, SDO7/-0/.*
4 *10 MB/s max, data out on lines SDIP/, SDI7/-0/.*

Figure 6-10. SCSI Synchronous Output

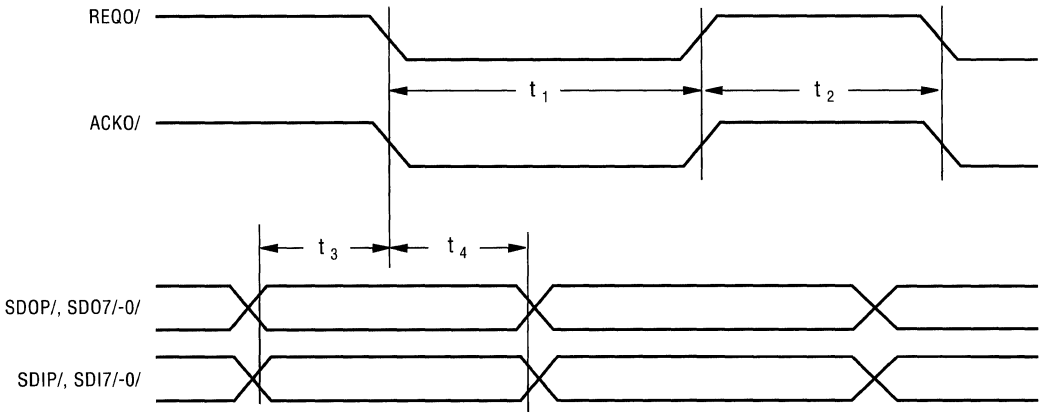
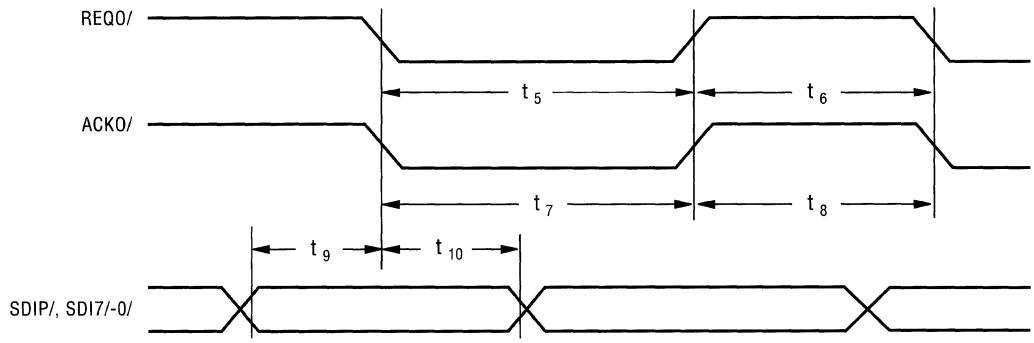
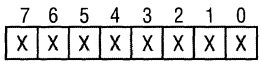


Figure 6-11. SCSI Synchronous Input

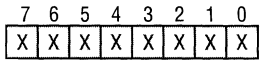


Appendix A
Register Summary

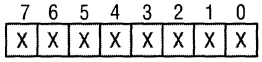
Transfer Counter Register R (00)



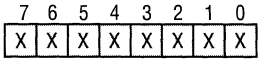
Transfer Count Register W (00)



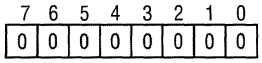
Transfer Counter Register R (01)



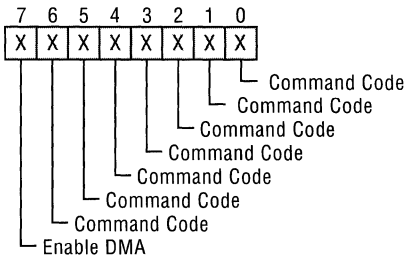
Transfer Count Register W (01)



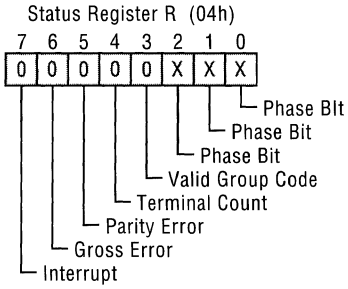
FIFO Register R/W (02)



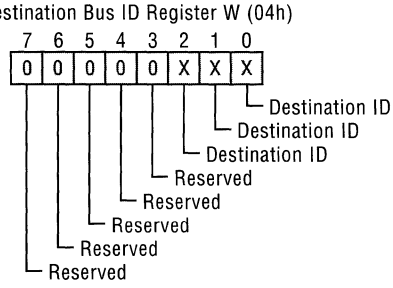
Command Register R/W (03h)



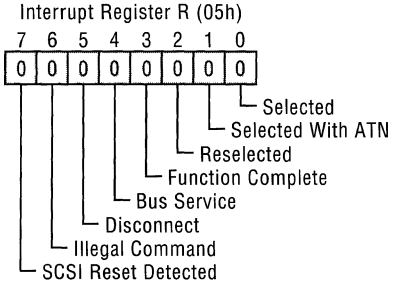
Status Register R (04h)



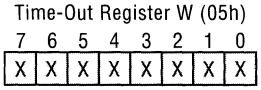
Destination Bus ID Register W (04h)



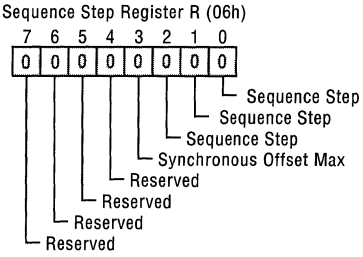
Interrupt Register R (05h)



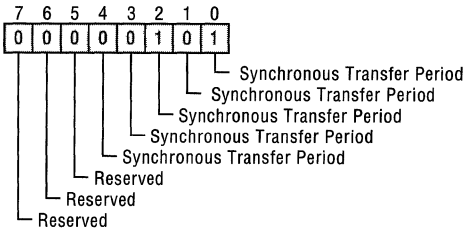
Time-Out Register W (05h)



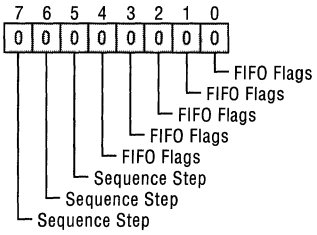
Sequence Step Register R (06h)



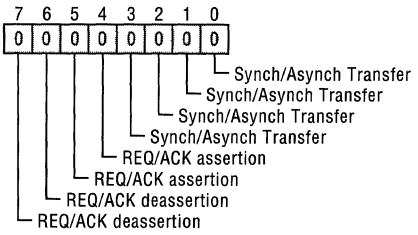
Synchronous Transfer Period Register W (06h)



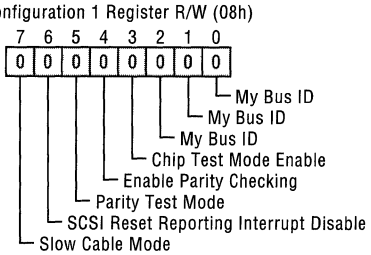
FIFO Flags Sequence Step Register R (07h)



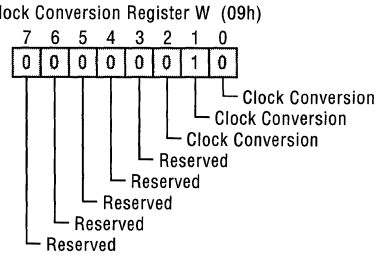
Synchronous Offset Register W (07h)



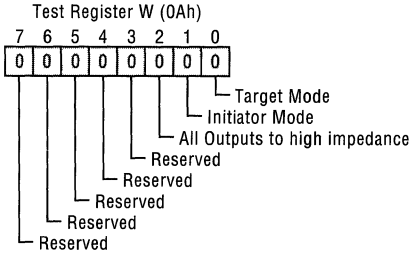
Configuration 1 Register R/W (08h)



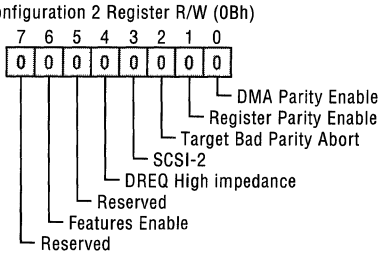
Clock Conversion Register W (09h)



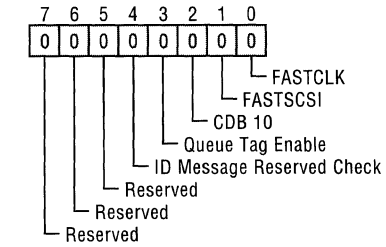
Test Register W (0Ah)



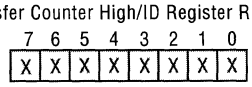
Configuration 2 Register R/W (0Bh)



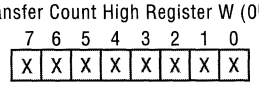
Configuration 3 Register R/W (0Ch)



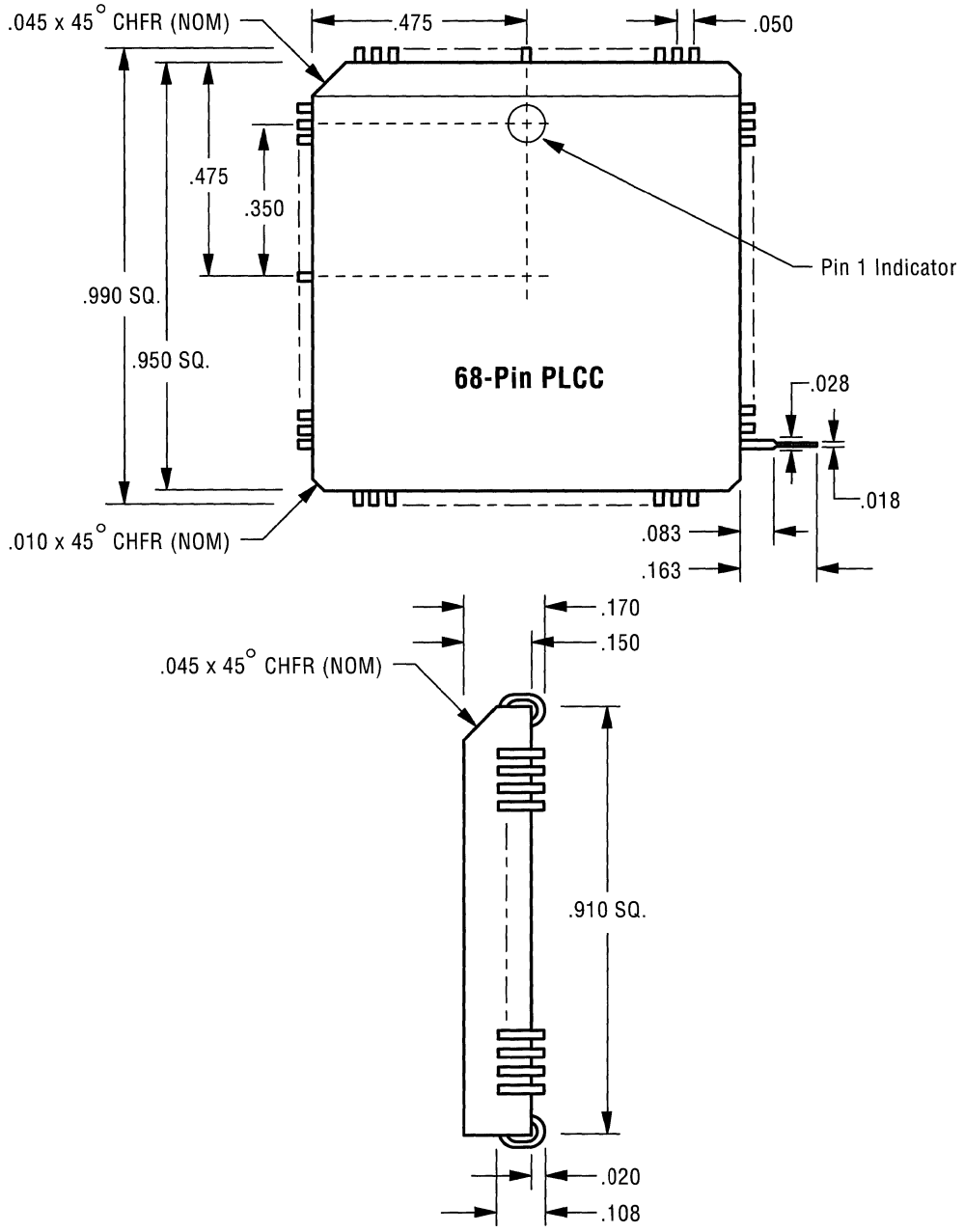
Transfer Counter High/ID Register R (0Eh)



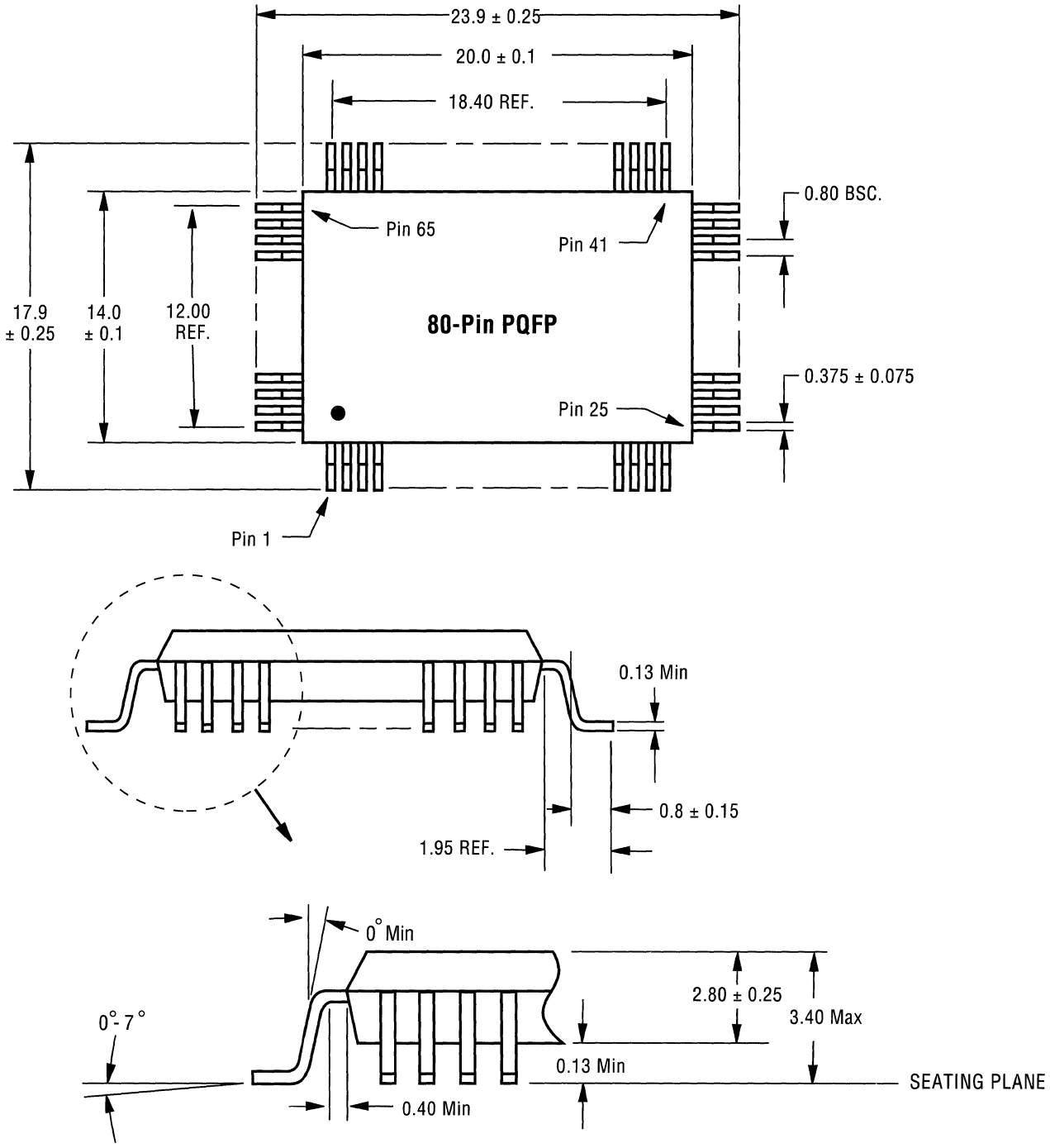
Transfer Count High Register W (0Eh)



Appendix B
Mechanical Drawings



Note: All dimensions are in inches



Note: All dimensions are in millimeters

Appendix C
Wiring Diagrams

Figure C-1. NCR 53CF90A, 53CF90B Single-Ended SCSI Bus Interface

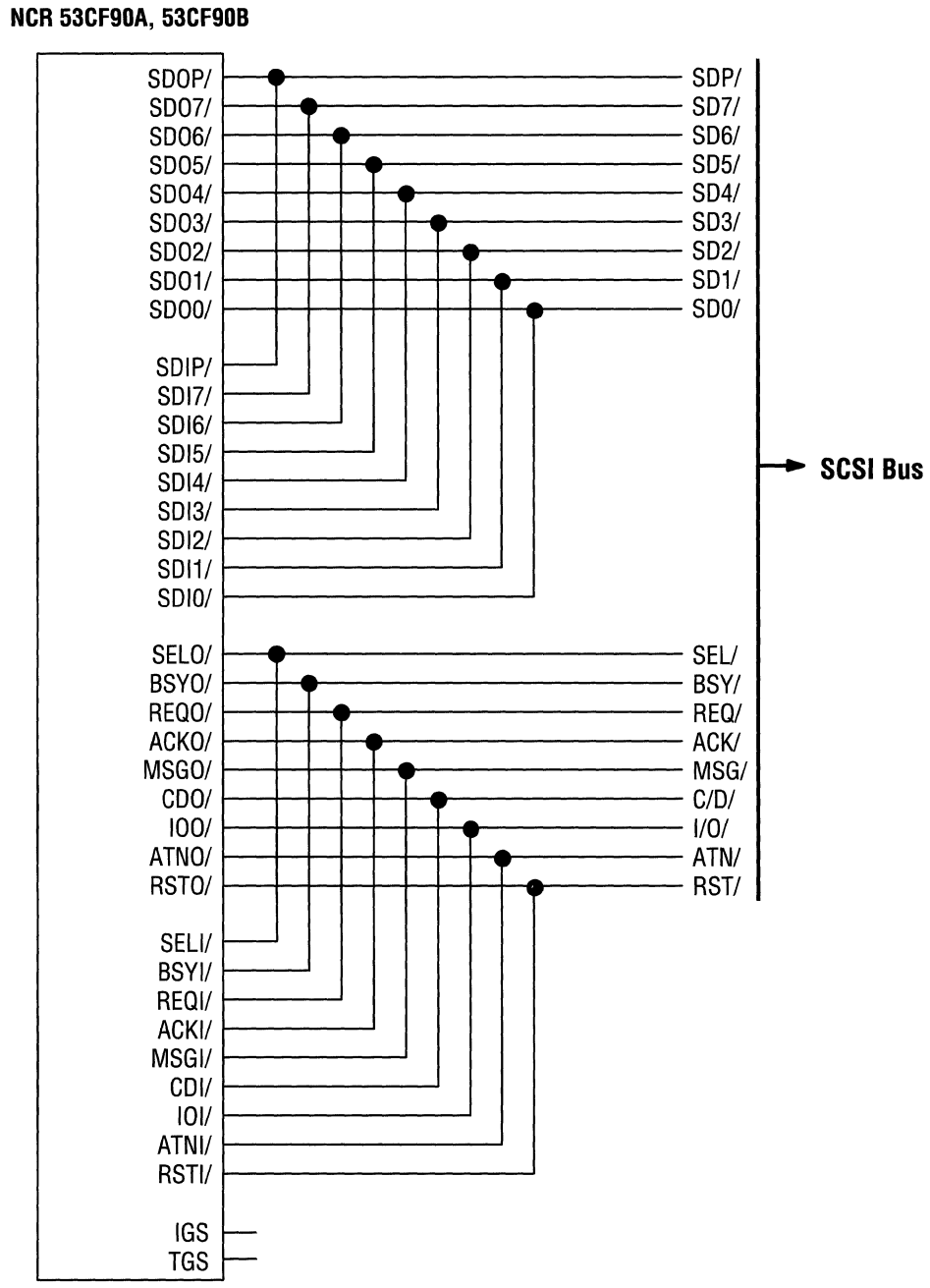
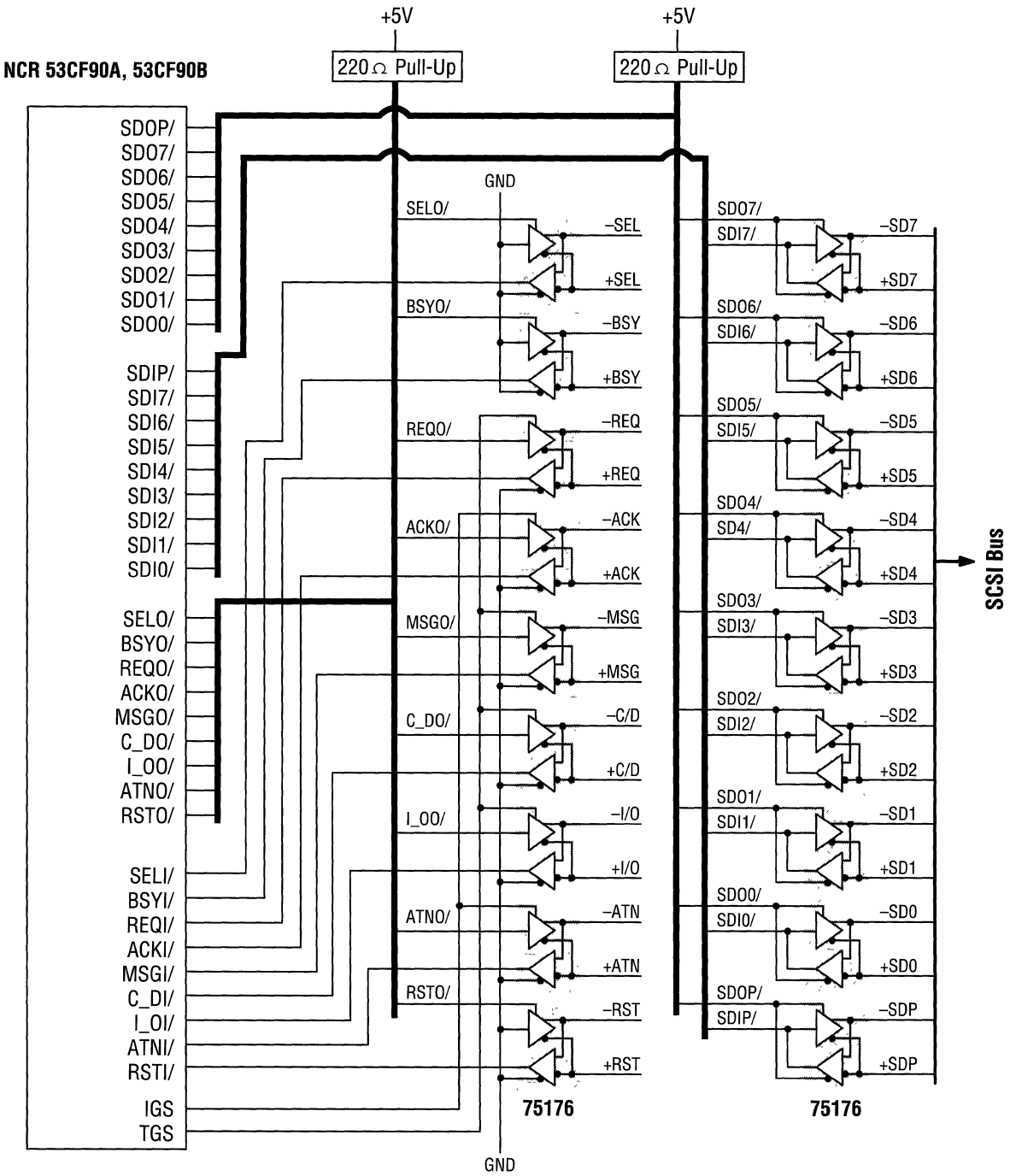


Figure C-2. NCR 53CF90A, 53CF90B Differential SCSI Bus Interface



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