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MOS BRIEF 11

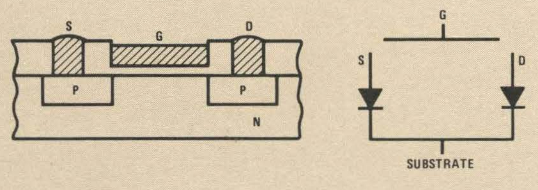
MOS AND BIPOLAR COMPATIBILITY—FACT OR FICTION

Now that MOS has been accepted into the design engineers bag of tricks, its compatibility with other forms of logic is the main issue. In the beginning, MOS and bipolar devices were not compatible at all; negative power supplies of 27 and 13 volts, threshold levels of −3 to −6 volts, slower speed, electrically fragile, etc. Sometimes the objections are more against MOS than the compatibility of the two families. Now, process refinements and design expertise have minimized these differences. Any designer that wants to intermix devices can do it if he really chooses. When linear circuits were first made available, the objection was that −6 and +12 volts or ±15 volts were not standard power supplies, MOS can use these same supplies if we manipulate the data sheet requirements.

LEVEL TRANSLATION

There is only one thing to remember about working with any logic element: it doesn't matter what the supply voltages are as long as the absolute magnitude across the device is maintained. A TTL element can operate between 25 and 30 volts or −10 and −5 volt busses because there are only 5 volts across the device. The only restriction is that the ground pin, being the reference point, must always be *more* negative than the V_{CC} pin.

This freedom of power supply levels is also a feature of MOS integrated circuits. Since it is normal procedure to bias the ground pin, it has been renamed the V_{SS} pin. It is the reference point and, for the P channel technology, must always be more positive than any other pin. Let's review why this is true. Consider the structure of an MOS device. A cross sectional view shows two diffused junctions in an N-type substrate. A channel is



induced between these two junctions to cause operation. The electrical symbol shows the device to be no more than two diodes with a common cathode. The junctions are used merely as contact points for the Source and Drain. If forward biasing occurred without current limiting, the junctions would be destroyed. As long as the substrate remains more positive, the diodes never become forward biased. The gate is electrically isolated by a thin oxide layer.

Process innovations, as stated before, have provided the designer with a method of achieving compatibility between MOS and bipolar IC's. The use of 1-0-0 crystal orientation silicon has yielded threshold voltages in the −1.8 to −2.5 volt range. These levels allow operation with +5 and −12 volt power supplies. Typical voltage levels for several different design configurations are shown below.

SHIFT REGISTER OPERATION

Most all low threshold voltage devices have characteristics like those shown under "existing register voltages" below. The National Semiconductor dynamic and static registers numbered MM400/500 through MM407/507, for example, fit this category. Newer designs such as the MM4015/5015, MM4050/5050, MM4051/5051 and many more to come will be designed with the "newer designs" logic levels shown.

	OUTPUT LEVELS		INPUT LEVELS		POWER SUPPLIES			
	V_{IL}	V_{IH}	V_{OL}	V_{OH}	V_{DD}	V_{GG}	V_{SS}	V_{ϕ}
Existing register voltages	−2.5	−7.0	−1.5	−8.0	−10	−16	GND	0 to −16
Newer designs register voltages	−2.5	−4.0	−1.5	−6.0	−10	−16	GND	0 to −16

These voltage values can be shifted to any convenient level as long as all voltages are shifted by the same potential. To make the "newer designed" registers shown above operate in a bipolar system, the levels can be shifted positive by +5.0 or +10.0 volts with the following results.

V_{IL}	V_{IH}	V_{OL}	V_{OH}	V_{DD}	V_{GG}	V_{SS}	V_{ϕ}
−2.5	−4.0	−1.5	−6.0	−10	−16	GND	0 to −16
+2.5	+1.0	+3.5	−1.0	−5	−11	+5	+5 to −11
+7.5	+6.0	+8.5	+4.0	GND	−6	+10	+10 to −6

Since these power supply voltages shown are nominal supplies, the device could operate satisfactorily between +5 and −12 volts, standard power supply values. This example shows that the popular misconception that MOS operates on negative voltages should be put to bed. They can be operated in the manner indicated: +5 and −12 volts, or +10 and −6 volts. A resistive pull-up on the input and a current sinking resistor on the output provides bipolar compatibility as shown. Second generation shift register designs such as the MM5050 will eliminate the resistors.

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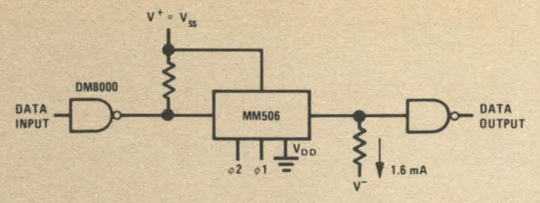
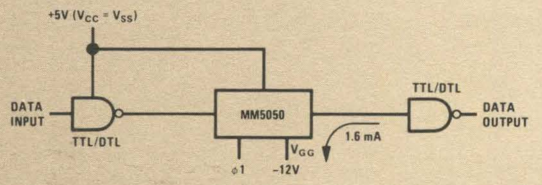
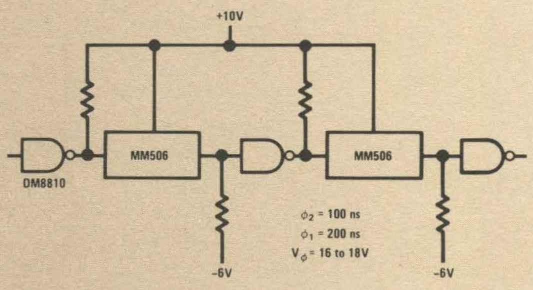




This form of interface can even be used to improve the operating frequency of MOS devices. When the MOS shift register is driving TTL, the total signal swing from a logic "0" to a logic "1" is reduced, hence the delay time is minimized. A long serial delay line, consisting of 1 MHz operating frequency shift registers, can be made to operate at 2.0 MHz by this method.

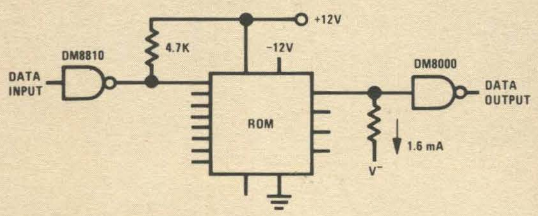


COST PROJECTIONS

Improved circuit design and process innovations are continually pushing aside objections to the MOS/bipolar hybrid system. The cost advantage and systems size reduction realized by utilizing long MOS shift registers in memory applications have come of age. Long shift registers compete favorably in price with magneto-strictive and glass delay lines. Price projections show 1970 pricing for long registers to achieve a penny a bit. The price coupled with the handling ease and smaller size of MOS registers will make replacement of delay lines a necessity during 1970.

READ ONLY MEMORY OPERATION

The read only memory designs have been made around ±12 volt operation. The rules, however, remain the same. MOS transistor threshold voltage is between −1.8 to −3.0 volts and bipolar compatibility is again maintained. The series 54/74 or DM8810 devices have the ability to hold off 12 volts on their output. The DM8810 Quad Gate and DM8812 Hex Inverter have an output breakdown specified at 14 volts. The interface between these elements is again a pull-up resistor on the input and a current sinking resistor on the output as shown.



Application briefs have been written to describe a character generator system or a delay line application that mixes the two worlds. By using a ROM for micro-programming, code conversion, character generation, table lookup and so forth, a system becomes fewer and fewer components. In fact, any random logic function that can be expressed in a truth table can be programmed into a ROM. Just try it.

CLOCK DRIVERS

The shift registers must be clocked and the clock must be generated from some source that will provide clock pulse amplitudes of 10 to 18 volts. Clock drivers that provide proper level translation have been developed by National. The NH0007 is a single phase clock driver capable of driving about 800 pF of clock line capacitance at 1.0 MHz and the NH0009 and NH0013 are two phase clock drivers capable of driving 1600 pF per line at 1.0 MHz. Another driver, the NH0012 has been developed for those clock driver applications requiring 10.0 MHz operation. The limiting parameter for these devices is power dissipation. The NH0007 is in a TO-5 can and is capable of dissipating about 300 milliwatts of power. The NH0009, NH0012 and NH0013 are in TO-8 cans and are capable of dissipating about 1.5 watts of power. The transient power for the driver is a function of speed, voltage amplitude, and load capacitance. The drive capability must be restricted so that the maximum power rating is observed. To calculate the power dissipated, the AC power is given by $P_{AC} = CV^2 f$. The standby power is a small percentage of the total power dissipated. For further details, refer to MOS Brief 9.

CONCLUSION

Our goal is to provide complete systems capability. We have achieved this with the availability of our MOS product line; bipolar logic for data manipulation, and MOS shift registers and read only memories for memory and micro-programming applications.

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