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National Semiconductor

May 1995

CROSSVOLT™ LCX Family

Low-Voltage High Speed CMOS Logic Datasheets

Includes Gates/MSI Functions &
Revised 16-bit Specifications

CROSSVOLT™ LCX FAMILY

LOW-VOLTAGE HIGH SPEED CMOS LOGIC DATASHEETS

May 1995

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National Semiconductor

PRELIMINARY

74LCX00
Low Voltage Quad 2-Input NAND Gate with 5V Tolerant Inputs

General Description

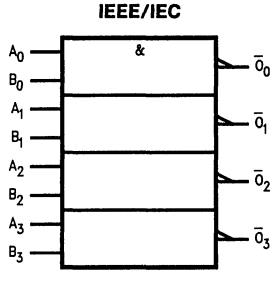
The LCX00 contains four 2-input NAND gates. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

The 74LCX00 is fabricated with advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

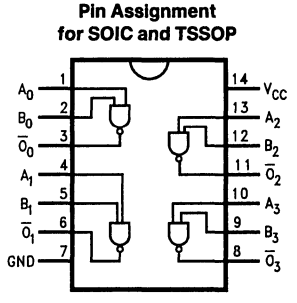
- 5V tolerant inputs
- 5.2 ns t_{PD} max, 10 μA I_{CCQ} max
- Power down high impedance inputs and outputs
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 00
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbol



TL/F/12408–1

Connection Diagram



TL/F/12408–2

Pin Names	Description
A_n, B_n	Inputs
$\overline{O}_n$	Outputs

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LCX00M 74LCX00MX	74LCX00SJ 74LCX00SJX	74LCX00MTC 74LCX00MTCX
See NS Package Number	M14A	M14D	MTC14

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		100	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics (Preliminary)

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PHL}	Propagation Delay	1.5	5.2	1.5	6.0	ns
t_{PLH}		1.5	5.2	1.5	6.0	
t_{OSHL}	Output to Output Skew (Note 1)		1.0			ns
t_{OSLH}			1.0			

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

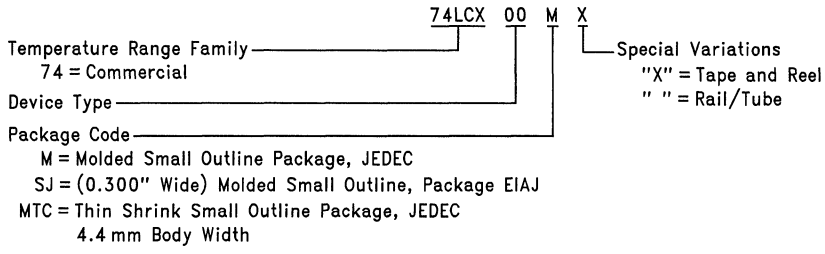
Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Unit
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	25	pF

74LCX00 Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



TL/F/12408–3

National Semiconductor

PRELIMINARY

74LCX02
Low Voltage Quad 2-Input NOR Gate with 5V Tolerant Inputs

General Description

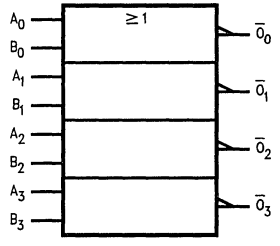
The LCX02 contains four 2-input NOR gates. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

The 74LCX02 is fabricated with advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs
- 5.2 ns t_{PD} max, 10 μA I_{CCQ} max
- Power down high impedance inputs and outputs
- 2.0V–3.6V V_{CC} supply operation
- 24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 02
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbol



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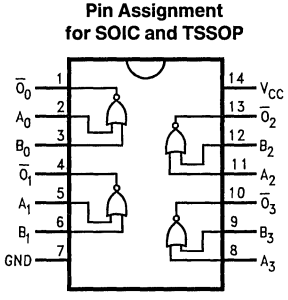
Connection Diagram



TL/F/12409–2

Pin Names	Description
A_n, B_n	Inputs
$\overline{O}_n$	Outputs

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LCX02M 74LCX02MX	74LCX02SJ 74LCX02SJX	74LCX02MTC 74LCX02MTCX
See NS Package Number	M14A	M14D	MTC14

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		100	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics (Preliminary)

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay Time	1.5 1.5	5.2 5.2	1.5 1.5	6.0 6.0	ns
t_{OSHL}, t_{OSLH}	Output to Output Skew (Note 1)		1.0 1.0			ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

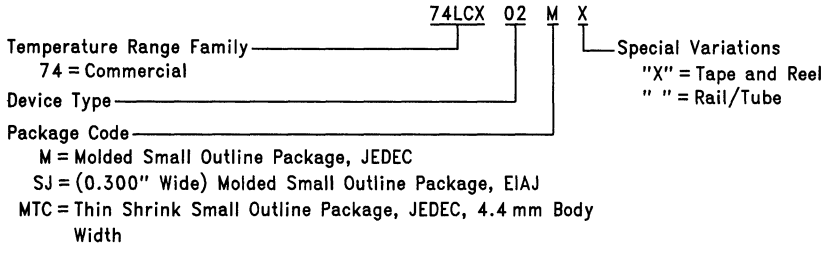
Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	25	pF

74LCX02 Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



TL/F/12409–3

National Semiconductor

PRELIMINARY

74LCX04
Low Voltage Hex Inverter with 5V Tolerant Inputs

General Description

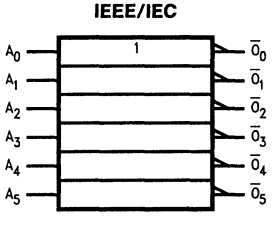
The LCX04 contains six inverters. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

The 74LCX04 is fabricated with advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs
- 5.2 ns t_{PD} max, 10 μA I_{CCQ} max
- Power down high impedance inputs and outputs
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patentend Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 04
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbol



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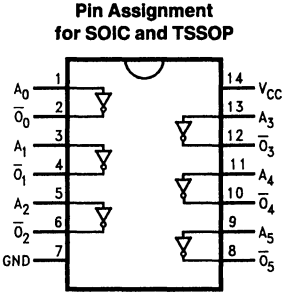
Connection Diagram



TL/F/12410–2

Pin Names	Description
A_n	Inputs
$\overline{O}_n$	Outputs

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LCX04M 74LCX04MX	74LCX04SJ 74LCX04SJX	74LCX04MTC 74LCX04MTCX
See NS Package Number	M14A	M14D	MTC14

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V–3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		100	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics (Preliminary)

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay Time	1.5 1.5	5.2 5.2	1.5 1.5	6.0 6.0	ns
t_{OSHL}, t_{OSLH}	Output to Output Skew (Note 1)		1.0 1.0			ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (T_{OSLH}).

Dynamic Switching Characteristics

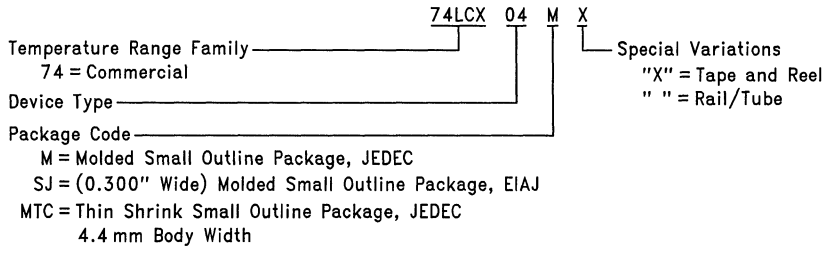
Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	25	pF

74LCX04 Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



TL/F/12410–3

National Semiconductor

ADVANCE INFORMATION

74LCX05
Hex Inverter (Open Drain) with 5V Tolerant Inputs

General Description

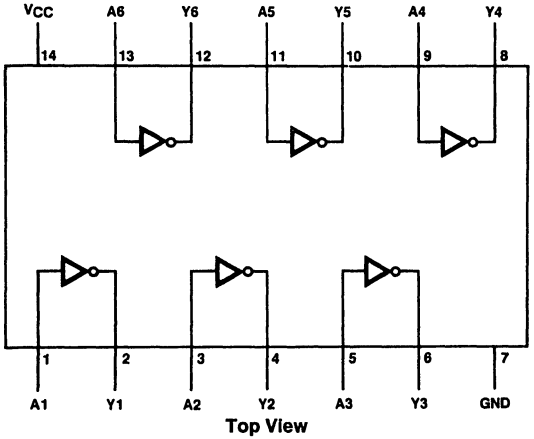
The 74LCX05 is an open drain hex inverter. The 74LCX05 requires the addition of an external resistor to perform a wire-NOR function. LCX devices are designed for low voltage (3.3V) operation with the added capability of interfacing to a 5V signal environment.

The 74LCX05 is fabricated with advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs
- Power down high impedance inputs and outputs
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 05
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Connection Diagram



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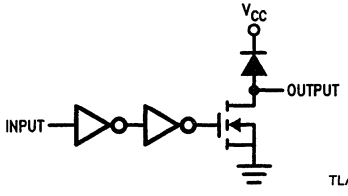
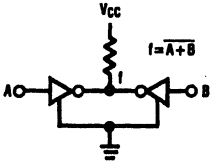
Top View

Logic Diagram



TL/F/12425–2

Typical Application



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Note: Can be extended to more than 2 inputs.

National Semiconductor

PRELIMINARY

74LCX08
Low Voltage Quad 2-Input AND Gate with 5V Tolerant Inputs

General Description

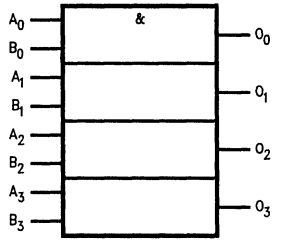
The LCX08 contains four 2-input AND gates. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

Features

- 5V tolerant inputs
- 5.5 ns t_{PD} max, 10 μA I_{CCQ} max
- Power down high impedance inputs and outputs
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 08
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbol

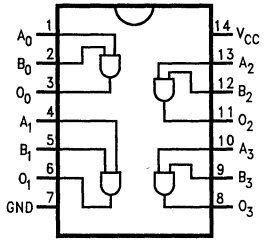
IEEE/IEC



TL/F/12411–1

Connection Diagram

Pin Assignment
for SOIC JEDEC, EIAJ and TSSOP



TL/F/12411–2

Pin Names	Description
A_n, B_n	Inputs
O_n	Outputs

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LCX08M 74LCX08MX	74LCX08SJ 74LCX08SJX	74LCX08MTC 74LCX08MTCX
See NS Package Number	M14A	M14D	MTC14

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		100	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay	1.5 1.5	5.5 5.5	1.5 1.5	6.2 6.2	ns
t_{OSLH} t_{OSHL}	Output to Output Skew (Note 1)		1.0 1.0			ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

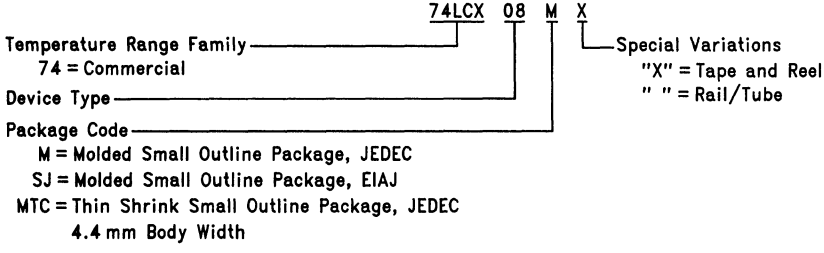
Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$ Typical	Units
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	25	pF

74LCX08 Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



TL/F/12411–3

National Semiconductor

ADVANCE INFORMATION

74LCX10
Triple 3-Input NAND Gate with 5V Tolerant Inputs

General Description

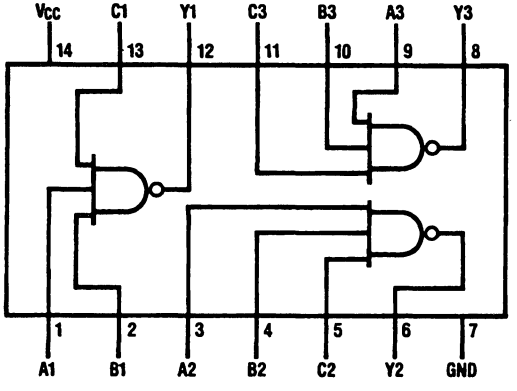
The 74LCX10 is a triple 3-input NAND gate with buffered outputs. LCX devices are designed for low voltage (3.3V) operation with the added capability of interfacing to a 5V signal environment.

The 74LCX10 is fabricated with advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs
- Power down high impedance inputs and outputs
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 10
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Connection and Logic Diagrams



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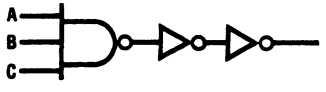
Top View



$Y = \overline{ABC}$

TL/F/12427–2

National Semiconductor

ADVANCE INFORMATION

74LCX11
Triple 3-Input AND Gate with 5V Tolerant Inputs

General Description

The 74LCX11 is a triple 3-input AND gate with buffered outputs. LCX devices are designed for low voltage (3.3V) operation with the added capability of interfacing to a 5V signal environment.

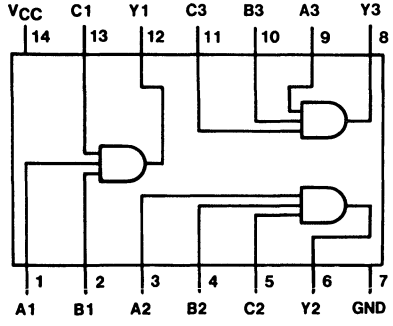
The 74LCX11 is fabricated with advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs
- Power down high impedance inputs and outputs
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 11
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

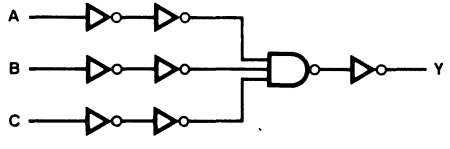
Connection and Logic Diagrams

Dual-In-Line Package



TL/F/12426–1

Top View



TL/F/12426–2

National Semiconductor

PRELIMINARY

74LCX14
Low Voltage Hex Inverter with 5V Tolerant Schmitt Trigger Inputs

General Description

The LCX14 contains six inverter gates each with a Schmitt trigger input. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have a greater noise margin than conventional inverters.

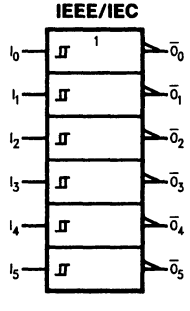
The LCX14 has hysteresis between the positive-going and negative-going input thresholds (typically 1.0V) which is determined internally by transistor ratios and is essentially insensitive to temperature and supply voltage variations.

The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

Features

- 5V tolerant inputs
- 6.5 ns t_{PD} max, 10 μA I_{CCQ} max
- Power-down high impedance inputs and outputs
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/ EMI reduction circuitry
- Functionally compatible with 74 series 14
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbol



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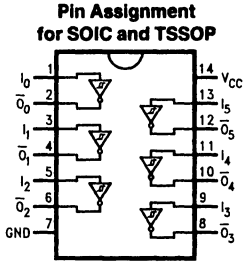
Connection Diagram



TL/F/12412–2

Pin Names	Description
I_n	Inputs
$\overline{O}_n$	Outputs

Truth Table

Input	Output
A	$\overline{O}$
L	H
H	L

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LCX14M 74LCX14MX	74LCX14SJ 74LCX14SJX	74LCX14MTC 74LCX14MTCX
See NS Package Number	M14A	M14D	MTC14

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{t+}	Positive Input Threshold		3.0	1.2	2.2	V
V_{t-}	Negative Input Threshold		3.0	0.6	1.5	V
V_H	Hysterisis		3.0	0.4	1.2	
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		100	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay	1.5 1.5	6.5 6.5	1.5 1.5	7.5 7.5	ns
t_{OSLH} t_{OSHL}	Output to Output Skew (Note 1)		1.0 1.0			ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

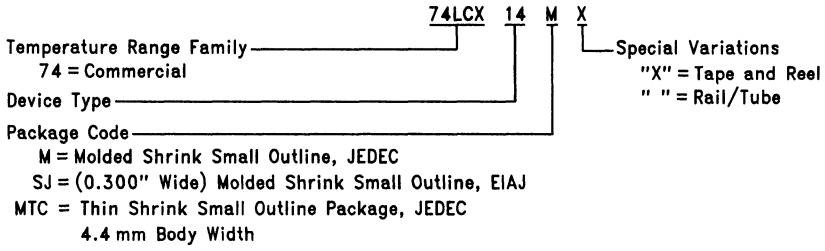
Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$ Typical	Units
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	25	pF

74LCX14 Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



TL/F/12412–3

National Semiconductor

PRELIMINARY

74LCX32
Low Voltage Quad 2-Input OR Gate with 5V Tolerant Inputs

General Description

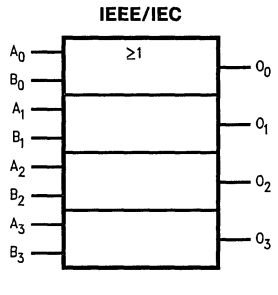
The LCX32 contains four 2-input OR gates. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

The 74LCX32 is fabricated with advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs
- 5.5 ns t_{PD} max, 10 μA I_{CCQ} max
- Power down high impedance inputs and outputs
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 32
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbol



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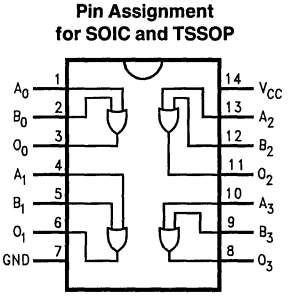
Connection Diagram



TL/F/12413–2

Pin Names	Description
A_n, B_n	Inputs
O_n	Outputs

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LCX32M 74LCX32MX	74LCX32SJ 74LCX32SJX	74LCX32MTC 74LCX32MTCX
NS Package Number	M14A	M14D	MTC14

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		100	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics (Preliminary)

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay	1.5 1.5	5.5 5.5	1.5 1.5	6.2 6.2	ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 1)		1.0 1.0			ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Unit
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	25	pF

National Semiconductor

PRELIMINARY

74LCX74
Low Voltage Dual D-Type Positive Edge-Triggered Flip-Flop with 5V Tolerant Inputs

General Description

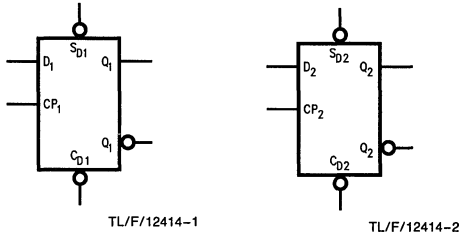
The LCX74 is a dual D-type flip-flop with Asynchronous Clear and Set inputs and complementary (Q, $\overline{Q}$) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

Asynchronous Inputs:
- LOW input to $\overline{S}_D$ (Set) sets Q to HIGH level
- LOW input to $\overline{C}_D$ (Clear) sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

Features

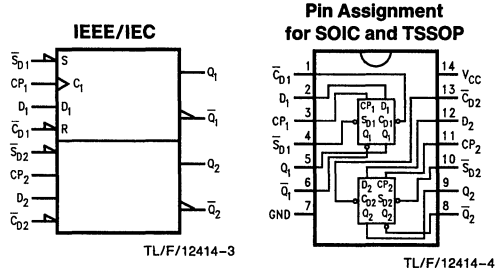
- 5V tolerant inputs
- 7.0 ns t_{PD} max, 10 μA I_{CCQ} max
- Power down high impedance inputs and outputs
- 2.0V–3.6V V_C supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 74
- Latch-up performance exceeds 500 mA
- ESD performance:
  - Human body model > 2000V
  - Machine model > 200V

Logic Symbols



TL/F/12414–1 TL/F/12414–2

Connection Diagram



TL/F/12414–3 TL/F/12414–4

Pin Names	Description
D_1, D_2	Data Inputs
CP_1, CP_2	Clock Pulse Inputs
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs
Q_1, $\overline{Q}_1$, Q_2, $\overline{Q}_2$	Outputs

Truth Table (Each Half)

Inputs				Outputs	
$\overline{S}_D$	$\overline{C}_D$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	↗	H	H	L
H	H	↗	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

↗ = LOW-to-HIGH Clock Transition
Q_0($\overline{Q}_0$) = Previous Q($\overline{Q}$) before LOW-to-HIGH Transition of Clock

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LCX74M 74LCX74MX	74LCX74SJ 74LCX74SJX	74LCX74MTC 74LCX74MTCX
See NS Package Number	M14A	M14D	MTC14

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		100	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics (Preliminary)

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	150				MHz
t_{PHL} t_{PLH}	Propagation Delay CP to Q	1.5 1.5	7.0 7.0	1.5 1.5	8.0 8.0	ns
t_{PHL} t_{PLH}	Propagation Delay S/R	1.5 1.5	7.0 7.0	1.5 1.5	8.0 8.0	ns
t_S	Setup Time	2.5		2.5		ns
t_H	Hold Time	1.5		1.5		ns
t_W	Pulse Width CP and S/R	3.3		3.3		ns
t_{rem}	Removal Time	0.0		0.0		ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 1)		1.0 1.0			ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

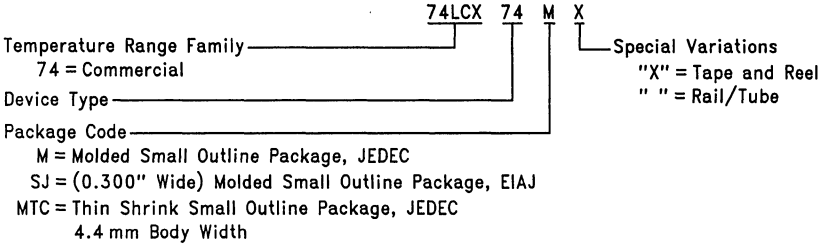
Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Unit
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	25	pF

74LCX74 Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



TL/F/12414–5

National Semiconductor

PRELIMINARY

74LCX86
Low Voltage Quad 2-Input Exclusive-OR Gate with 5V Tolerant Inputs

General Description

The LCX86 contains four 2-input exclusive-OR gates. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

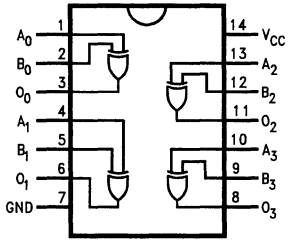
The 74LCX is fabricated with advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs
- 6.5 ns t_{PD} max, 10 μA I_{CCQ} max
- Power down high impedance inputs
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 86
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbol

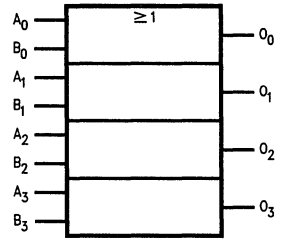
IEEE/IEC



TL/F/12415–2

Connection Diagram

Pin Assignment for SOIC, SSOP and TSSOP



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Pin Names	Description
A_0–A_3	Inputs
B_0–B_3	Inputs
O_0–O_3	Outputs

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LCX86M 74LCX86MX	74LCX86SJ 74LCX86SJX	74LCX86MTC 74LCX86MTCX
See NS Package Number	M14A	M14D	MTC14

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V–3.6V V_{CC} = 2.7V		±24 ±12	mA
(T_A)	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		100	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay	1.5 1.5	6.5 6.5	1.5 1.5	7.0 7.0	ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 1)		1.0 1.0			ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

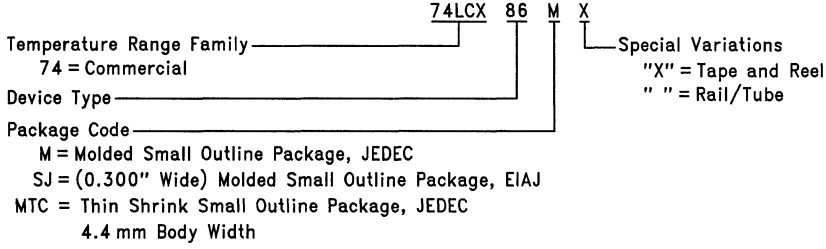
Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	25	pF

74LCX86 Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



TL/F/12415–3

National Semiconductor

ADVANCE INFORMATION

74LCX109
Dual J-$\overline{K}$ Flip-Flops with Preset and Clear with 5V Tolerant Inputs

General Description

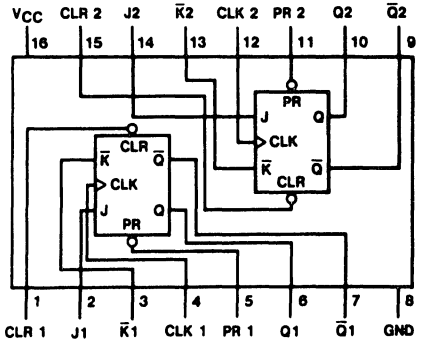
The 74LCX109 are dual J-$\overline{K}$ flip-flops. Each flip-flop has independent J, $\overline{K}$, PRESET, CLEAR, and CLOCK inputs and Q, $\overline{Q}$ outputs. These devices are edge sensitive and change state on the negative going transition of the clock pulse. Clear and preset are independent of the clock and accomplished by a low logic level on the corresponding input. LCX devices are designed for low voltage (3.3V) operation with the added capability of interfacing to a 5V signal environment.

The 74LCX109 is fabricated with advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs
- Power down high impedance inputs and outputs
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 109
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Connection and Logic Diagrams



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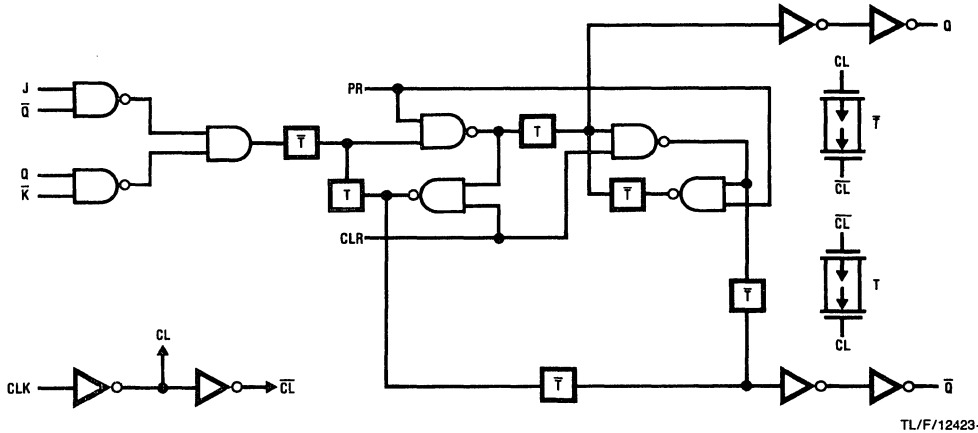
Function Table

Inputs					Outputs	
PR	CLR	CLK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q0	$\overline{Q}$0
H	H	↑	H	H	H	L
H	H	L	X	X	Q0	$\overline{Q}$0



TL/F/12423–2

National Semiconductor

ADVANCE INFORMATION

74LCX112
Dual J-K Flip-Flops with Preset and Clear with 5V Tolerant Inputs

General Description

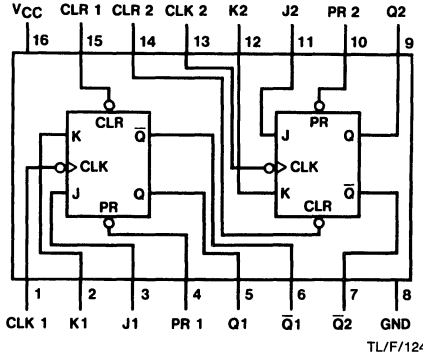
The 74LCX112 are dual J-K flip-flops. Each flip-flop has independent J, K, PRESET, CLEAR, and CLOCK inputs Q, $\overline{Q}$ outputs. These devices are edge sensitive and change state on the negative going transition of the clock pulse. Clear and preset are independent of the clock and accomplished by a low logic level on the corresponding input. LCX devices are designed for low voltage (3.3V) operation with the added capability of interfacing to a 5V signal environment.

The 74LCX112 is fabricated with advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs
- Power down high impedance inputs and outputs
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 112
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Connection and Logic Diagrams



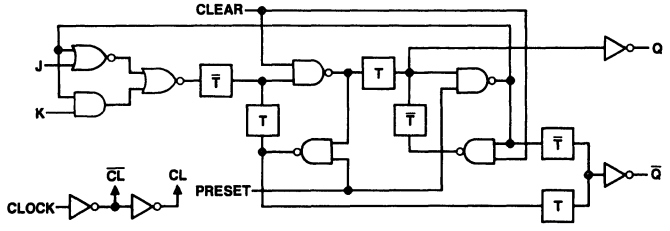
TL/F/12424–1

Top View

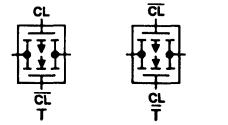
Truth Table

Inputs					Outputs	
PR	CLR	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	L*	L*
H	H	↓	L	L	Q0	$\overline{Q}$0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q0	$\overline{Q}$0

*This is an unstable condition, and is not guaranteed.



TL/F/12424–2



TL/F/12424–3

National Semiconductor

PRELIMINARY

74LCX125
Low-Voltage Quad Buffer with 5V Tolerant Inputs and Outputs

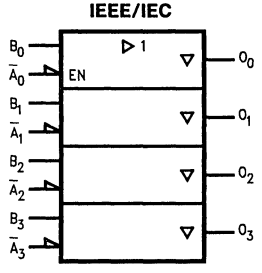
General Description

The LCX125 contains four independent non-inverting buffers with TRI-STATE outputs. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

Features

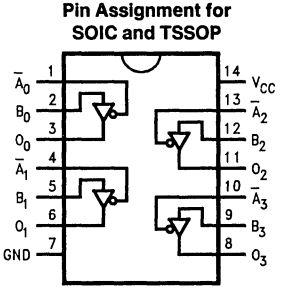
- 5V tolerant inputs and outputs
- 6.0 ns t_{PD} max, 10 μA I_{CCQ} max
- Power down high impedance inputs and outputs
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 125
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbol



TL/F/12416–1

Connection Diagram



TL/F/12416–2

Pin Names	Description
A_n, B_n	Inputs
O_n	Outputs

Truth Table

Inputs		Output
A_n	B_n	O_n
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
Z = High Impedance
X = Immaterial

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LCX125M 74LCX125MX	74LCX125SJ 74LCX125SJX	74LCX125MTC 74LCX125MTCX
See NS Package Number	M14A	M14D	MTC14

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V–3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE Output Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		100	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay	1.5 1.5	6.0 6.0	1.5 1.5	6.5 6.5	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5 1.5	7.0 7.0	1.5 1.5	8.0 8.0	ns
t_{PLZ} t_{PHZ}	Output Disable Time	1.5 1.5	6.0 6.0	1.5 1.5	7.0 7.0	ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 1)		1.0 1.0			ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

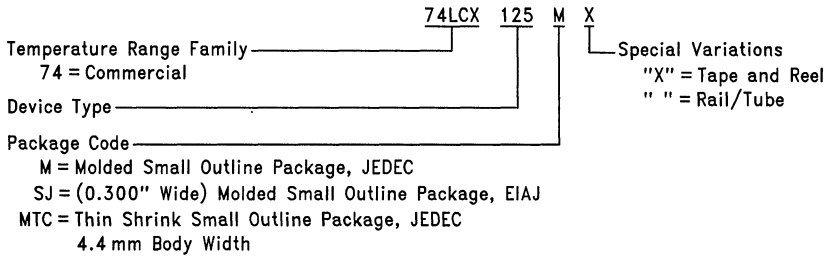
Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$ Typical	Units
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
$C_{I/O}$	Input/Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	25	pF

74LCX125 Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



TL/F/12416–3

National Semiconductor

PRELIMINARY

74LCX138
Low Voltage 1-of-8 Decoder/Demultiplexer with 5V Tolerant Inputs

General Description

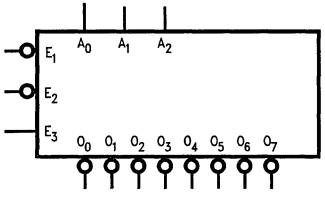
The LCX138 is a high-speed 1-of-8 decoder/demultiplexer. This device is ideally suited for high-speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three LCX138 devices or a 1-of-32 decoder using four LCX138 devices and one inverter.

The 74LCX138 is fabricated with advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

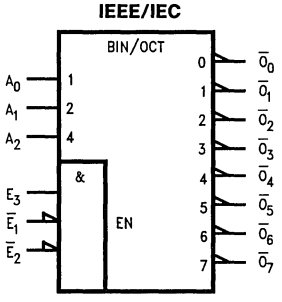
Features

- 5V tolerant inputs
- 6.0 ns t_{PD} max, 10 μA I_{CCQ} max
- Power down high impedance inputs and outputs
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 138
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbols

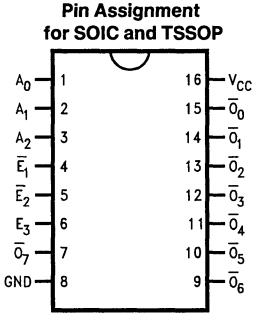


TL/F/12417–1



TL/F/12417–2

Connection Diagram



TL/F/12417–3

Pin Names	Description
A_0–A_2	Address Inputs
$\overline{E}_1$–$\overline{E}_2$	Enable Inputs
E_3	Enable Input
$\overline{O}_0$–$\overline{O}_7$	Outputs

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LCX138M 74LCX138MX	74LCX138SJ 74LCX138SJX	74LCX138MTC 74LCX138MTCX
See NS Package Number	M16A	M16D	MTC16

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

Functional Description

The LCX138 high-speed 1-of-8 decoder/demultiplexer accepts three binary weighted inputs (A_0, A_1, A_2) and, when enabled, provides eight mutually exclusive active-LOW outputs ($\overline{O}_0$–$\overline{O}_7$). The LCX138 features three Enable inputs, two active-LOW ($\overline{E}_1$, $\overline{E}_2$) and one active-HIGH (E_3). All outputs will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH.

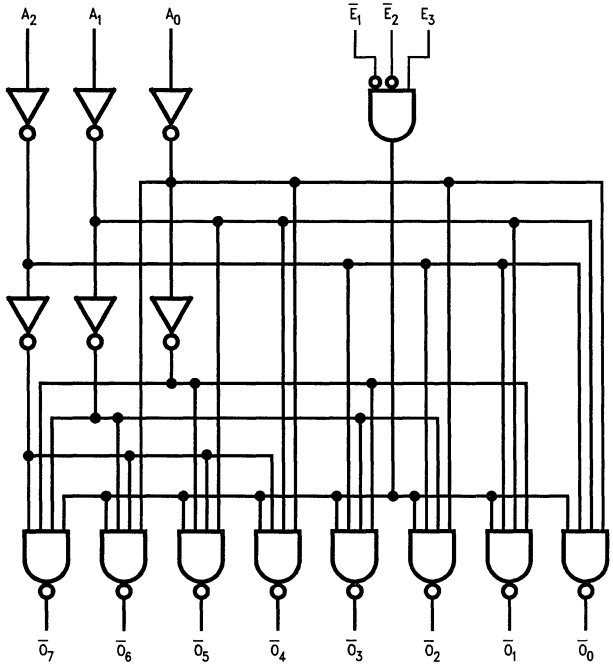
The LCX138 can be used as an 8-output demultiplexer by using one of the active LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active-HIGH or active-LOW state.

Truth Table

Inputs						Outputs							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



TL/F/12417–4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V–3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		100	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics (Preliminary)

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay A–Y	1.5 1.5	6.0 6.0	1.5 1.5	7.0 7.0	ns
t_{PHL} t_{PLH}	Propagation Delay E3–Y	1.5 1.5	6.5 6.5	1.5 1.5	7.5 7.5	ns
t_{PHL} t_{PLH}	Propagation Delay En–Y	1.5 1.5	6.0 6.0	1.5 1.5	7.0 7.0	ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 1)		1.0 1.0			ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

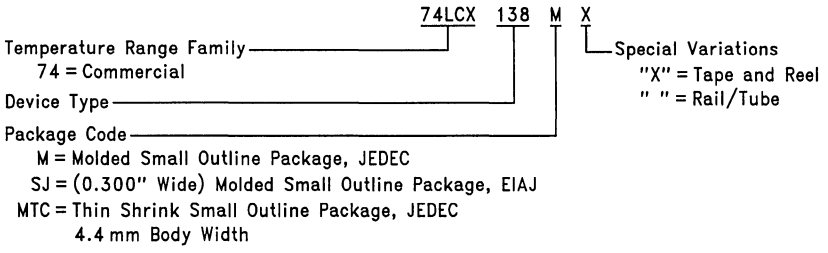
Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	25	pF

74LCX138 Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



TL/F/12417–5

National Semiconductor

74LCX240
Low-Voltage Octal Buffer/Line Driver with 5V Tolerant Inputs and Outputs

General Description

The LCX240 is an inverting octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver. The device is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX240 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

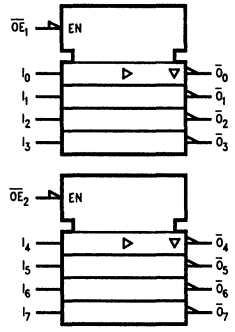
- Power-down high impedance inputs and outputs
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with the 74 series 240
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human Body Model > 2000V
  Machine Model > 200V

Features

- 5V tolerant inputs and outputs
- 6.5 ns t_{PD} max, 10 μA I_{CCQ} max

Logic Symbol

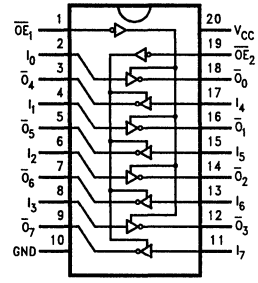
IEEE/IEC



TL/F/11993–1

Connection Diagram

Pin Assignment for SOIC, SSOP and TSSOP



TL/F/11993–2

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	TRI-STATE® Output Enable Inputs
I_0–I_7	Inputs
$\overline{O}_0$–$\overline{O}_7$	Outputs

Truth Tables

Inputs		Outputs (Pins 12, 14, 16, 18)
$\overline{OE}_1$	I_n	
L	L	H
L	H	L
H	X	Z

Inputs		Outputs (Pins 3, 5, 7, 9)
$\overline{OE}_2$	I_n	
L	L	H
L	H	L
H	X	Z

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial Z = High Impedance

	SOIC JEDEC	SOIC EIAJ	SSOP Type II	TSSOP
Order Number	74LCX240WM 74LCX240WMX	74LCX240SJ 74LCX240SJX	74LCX240MSA 74LCX240MSAX	74LCX240MTC 74LCX240MTCX
See NS Package Number	M20B	M20D	MSA20	MTC20

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V–3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE Output Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		100	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} − 0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay Data to Output	1.5 1.5	6.5 6.5	1.5 1.5	7.5 7.5	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5 1.5	8.0 8.0	1.5 1.5	9.0 9.0	ns
t_{PLZ} t_{PHZ}	Output Disable Time	1.5 1.5	7.0 7.0	1.5 1.5	8.0 8.0	ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 1)		1.0 1.0			ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

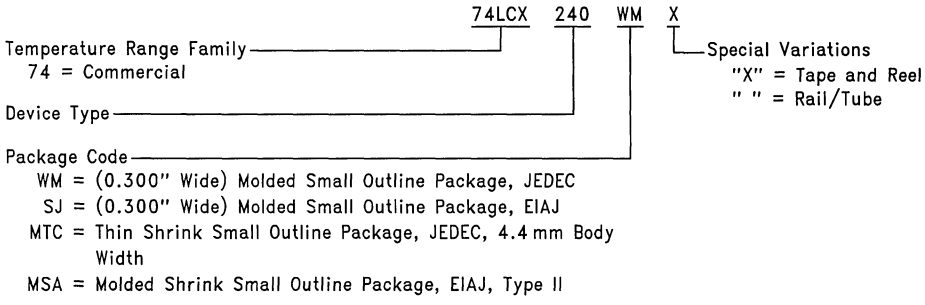
Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	25	pF

74LCX240 Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



TL/F/11993–3

National Semiconductor

74LCX244
Low-Voltage Buffer/Line Driver with 5V Tolerant Inputs and Outputs

General Description

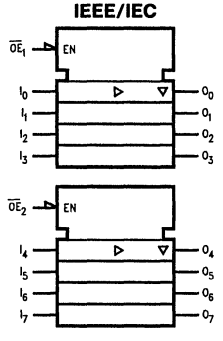
The LCX244 contains eight non-inverting buffers with TRI-STATE® outputs. The device may be employed as a memory address driver, clock driver and bus-oriented transmitter/receiver. The LCX244 is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX244 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

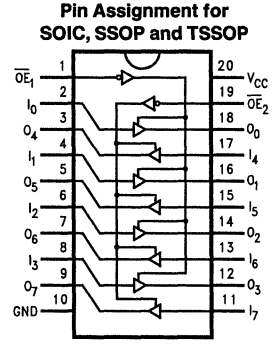
- 5V tolerant inputs and outputs
- 6.5 ns t_{PD} max, 10 μA I_{CCQ} max
- Power down high impedance inputs and outputs
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with the 74 series 244
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbol



TL/F/11994–1

Connection Diagram



TL/F/11994–2

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	TRI-STATE Output Enable Inputs
I_0–I_7	Inputs
O_0–O_7	Outputs

Truth Tables

Inputs		Outputs (Pins 12, 14, 16, 18)
$\overline{OE}_1$	I_n	
L	L	L
L	H	H
H	X	Z

Inputs		Outputs (Pins 3, 5, 7, 9)
$\overline{OE}_2$	I_n	
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level X = Immaterial L = LOW Voltage Level Z = High Impedance

	SOIC JEDEC	SOIC EIAJ	SSOP Type II	TSSOP JEDEC
Order Number	74LCX244WM 74LCX244WMX	74LCX244SJ 74LCX244SJX	74LCX244MSA 74LCX244MSAX	74LCX244MTC 74LCX244MTCX
See NS Package Number	M20B	M20D	MSA20	MTC20

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE Output Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		100	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay Data to Output	1.5 1.5	6.5 6.5	1.5 1.5	7.5 7.5	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5 1.5	8.0 8.0	1.5 1.5	9.0 9.0	ns
t_{PLZ} t_{PHZ}	Output Disable Time	1.5 1.5	7.0 7.0	1.5 1.5	8.0 8.0	ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 1)		1.0 1.0			ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

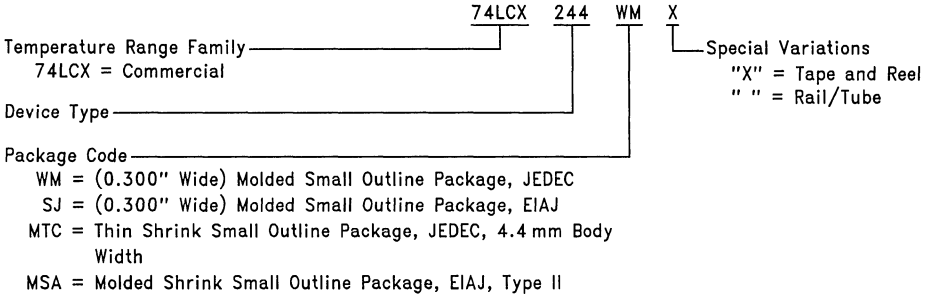
Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	25	pF

74LCX244 Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



TL/F/11994–4

National Semiconductor

74LCX245
Low-Voltage Bidirectional Transceiver with 5V Tolerant Inputs and Outputs

General Description

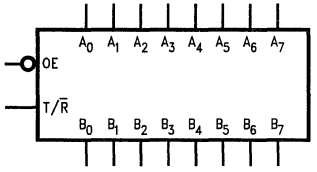
The LCX245 contains eight non-inverting bidirectional buffers with TRI-STATE® outputs and is intended for bus oriented applications. The device is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment. The T/$\overline{R}$ input determines the direction of data flow through the device. The $\overline{OE}$ input disables both the A and B ports by placing them in a high impedance state.

The LCX245 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

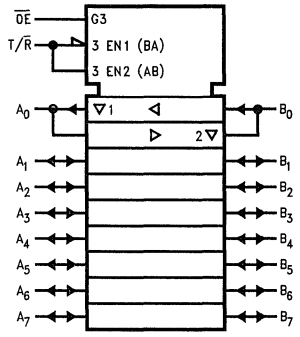
- 5V tolerant inputs and outputs
- 7.0 ns t_{PD} max, 10 μA I_{CCQ} max
- Power down high impedance inputs and outputs
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with the 74 series 245
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbols



TL/F/12006–1

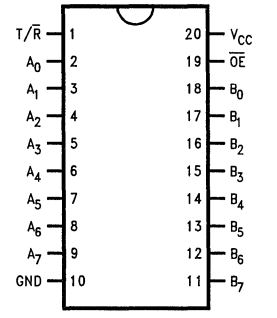
IEEE/IEC



TL/F/12006–2

Connection Diagram

Pin Assignment for SOIC, SSOP and TSSOP



TL/F/12006–3

Pin Names	Description
$\overline{OE}$	Output Enable Input
T/$\overline{R}$	Transmit/Receive Input
A_0–A_7	Side A Inputs or TRI-STATE Outputs
B_0–B_7	Side B Inputs or TRI-STATE Outputs

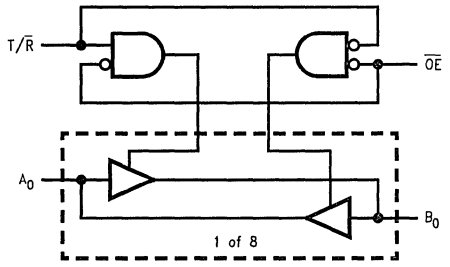
	SOIC JEDEC	SOIC EIAJ	SSOP Type II	TSSOP JEDEC
Order Number	74LCX245WM 74LCX245WMX	74LCX245SJ 74LCX245SJX	74LCX245MSA 74LCX245MSAX	74LCX245MTC 74LCX245MTCX
See NS Package Number	M20B	M20D	MSA20	MTC20

Truth Table

Inputs		Outputs
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B_0–B_7 Data to Bus A_0–A_7
L	H	Bus A_0–A_7 Data to Bus B_0–B_7
H	X	HIGH Z State on A_0–A_7, B_0–B_7

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



TL/F/12006–4

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE I/O Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		100	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay A_n to B_n or B_n to A_n	1.5 1.5	7.0 7.0	1.5 1.5	8.0 8.0	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_{PLZ} t_{PHZ}	Output Disable Time	1.5 1.5	7.5 7.5	1.5 1.5	8.5 8.5	ns
t_{OSHL}, t_{OSLH}	Output to Output Skew (Note 1)		1.0 1.0			ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
$C_{I/O}$	Input/Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	25	pF

74LCX245 Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

74LCX 245 WM X

Temperature Range Family
74 = Commercial

Device Type

Special Variations
"X" = Tape and Reel
" " = Rail/Tube

Package Code
WM = (0.300" Wide) Molded Small Outline Package, JEDEC
SJ = (0.300" Wide) Molded Small Outline Package, EIAJ
MTC = Thin Shrink Small Outline Package, JEDEC, 4.4 mm Body Width
MSA = Molded Shrink Small Outline Package, EIAJ, Type II

TL/F/12006–5

National Semiconductor

74LCX373
Low-Voltage Octal Transparent Latch with 5V Tolerant Inputs and Outputs

General Description

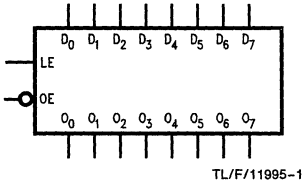
The LCX373 consists of eight latches with TRI-STATE® outputs for bus organized system applications. The device is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX373 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

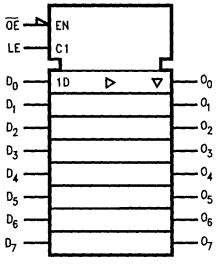
- 5V tolerant inputs and outputs
- 8.0 ns t_{PD} max, 10 μA I_{CCQ} max
- Power-down high impedance inputs and outputs
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with the 74 series 373
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human Body Model > 2000V
  Machine Model > 200V

Logic Symbols



TL/F/11995–1

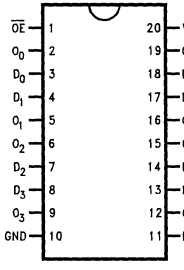
IEEE/IEC



TL/F/11995–2

Connection Diagram

Pin Assignment for SOIC, SSOP and TSSOP



TL/F/11995–3

Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	Output Enable Input
O_0–O_7	TRI-STATE Latch Outputs

	SOIC JEDEC	SOIC EIAJ	SSOP Type II	TSSOP JEDEC
Order Number	74LCX373WM 74LCX373WMX	74LCX373SJ 74LCX373SJX	74LCX373MSA 74LCX373MSAX	74LCX373MTC 74LCX373MTCX
See NS Package Number	M20B	M20D	MSA20	MTC20

Functional Description

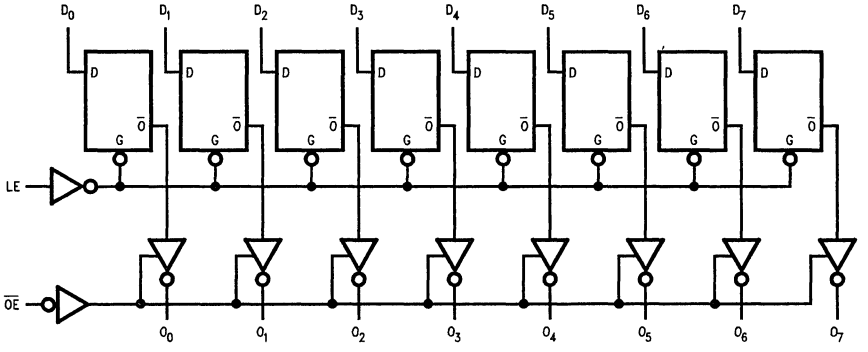
The LCX373 contains eight D-type latches with TRI-STATE standard outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE standard outputs are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the standard outputs are in the 2-state mode. When $\overline{OE}$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

Inputs			Outputs
LE	$\overline{OE}$	D_n	O_n
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

H = HIGH Voltage Level
L = LOW Voltage Level
Z = High Impedance
X = Immaterial
O_0 = Previous O_0 before HIGH to LOW transition of Latch Enable

Logic Diagram



TL/F/11995–4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V–3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE Output Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		100	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} − 0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay D_n to O_n	1.5 1.5	8.0 8.0	1.5 1.5	9.0 9.0	ns
t_{PHL} t_{PLH}	Propagation Delay LE to O_n	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_{PLZ} t_{PHZ}	Output Disable Time	1.5 1.5	7.5 7.5	1.5 1.5	8.5 8.5	ns
t_S	Setup Time, D_n to LE	2.5		2.5		ns
t_H	Hold Time, D_n to LE	1.5		1.5		ns
t_W	LE Pulse Width	3.3		3.3		ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 1)		1.0 1.0			ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

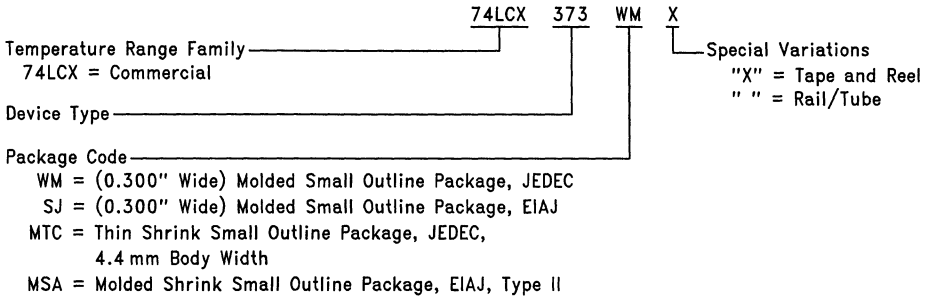
Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	25	pF

74LCX373 Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



TL/F/11995–5

National Semiconductor

74LCX374
Low-Voltage Octal D Flip-Flop with 5V Tolerant Inputs and Outputs

General Description

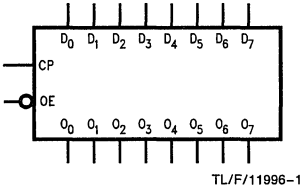
The LCX374 consists of eight D-type flip-flops featuring separate D-type inputs for each flip-flop and TRI-STATE® outputs for bus-oriented applications. A buffered clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops. The LCX374 is designed for low-voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX374 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

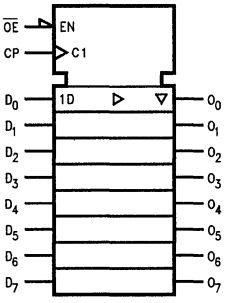
- 5V tolerant inputs and outputs
- 8.5 ns t_{PD} max, 10 μA I_{CCQ} max
- Power-down high impedance inputs and outputs
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with the 74 series 374
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human Body Model > 2000V
  Machine Model > 200V

Logic Symbols



TL/F/11996–1

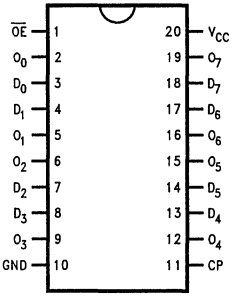
IEEE/IEC



TL/F/11996–2

Connection Diagram

Pin Assignment for SOIC, SSOP and TSSOP



TL/F/11996–3

Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	Output Enable Input
O_0–O_7	TRI-STATE Outputs

	SOIC JEDEC	SOIC EIAJ	SSOP Type II	TSSOP JEDEC
Order Number	74LCX374WM 74LCX374WMX	74LCX374SJ 74LCX374SJX	74LCX374MSA 74LCX374MSAX	74LCX374MTC 74LCX374MTCX
See NS Package Number	M20B	M20D	MSA20	MTC20

Functional Description

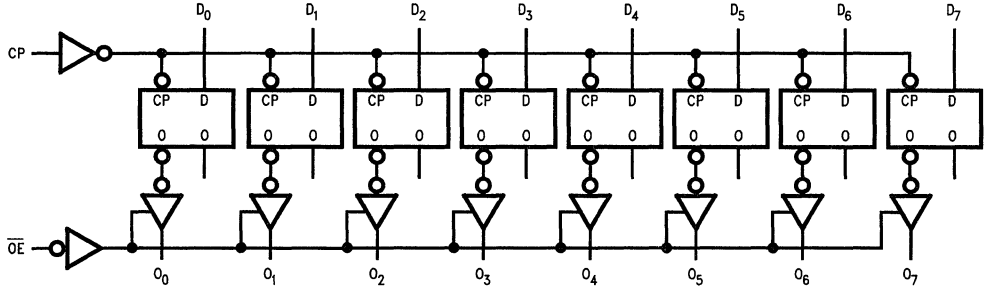
The LCX374 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Truth Table

Inputs			Outputs
D_n	CP	$\overline{OE}$	O_n
H	⌐	L	H
L	⌐	L	L
X	L	L	O_0
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
⌐ = LOW-to-HIGH Transition
O_0 = Previous O_0 before HIGH to LOW of CP

Logic Diagram



TL/F/11996–4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V–3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE Output Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		100	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} − 0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	150				MHz
t_{PHL} t_{PLH}	Propagation Delay CP to O_n	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_{PLZ} t_{PHZ}	Output Disable Time	1.5 1.5	7.5 7.5	1.5 1.5	8.5 8.5	ns
t_S	Setup Time	2.5		2.5		ns
t_H	Hold Time	1.5		1.5		ns
t_W	Pulse Width	3.3		3.3		ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 1)		1.0 1.0			ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

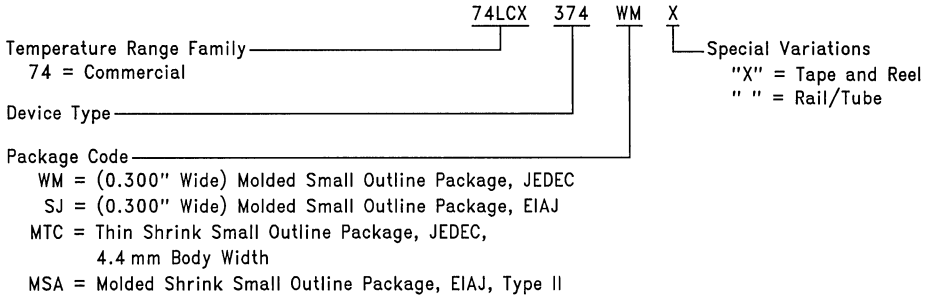
Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	25	pF

74LCX374 Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



TL/F/11996–5

National Semiconductor

PRELIMINARY

74LCX540
Octal Buffer/Line Driver with 5V Tolerant Inputs and Outputs

General Description

The LCX540 is an octal buffer/line drivers designed to be employed as memory and address drivers, clock drivers and bus oriented transmitter/receivers.

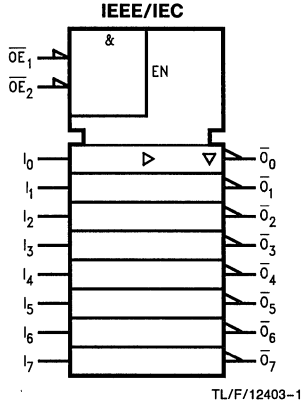
These devices are similar in function to the 'LCX240 while providing flow-through architecture (inputs on opposite side from outputs). This pinout arrangement makes these devices especially useful as output ports for microprocessors, allowing ease of layout and greater PC board density.

The LCX540 is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment. The LCX540 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

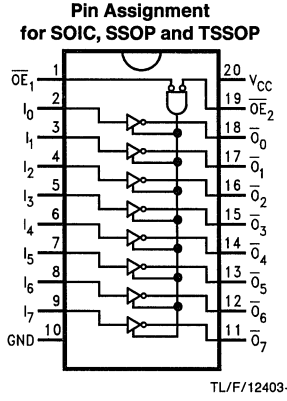
- 5V tolerant inputs and outputs
- 6.5 ns t_{PD} max, 10 μA I_{CCQ} max
- Power down high impedance inputs and outputs
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 540
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbol



TL/F/12403–1

Connection Diagram



TL/F/12403–2

Truth Table

Inputs			Outputs
$\overline{OE}_1$	$\overline{OE}_2$	I	
L	L	H	L
H	X	X	Z
X	H	X	Z
L	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

	SOIC JEDEC	SOIC EIAJ	SSOP Type II	TSSOP JEDEC
Order Number	74LCX540WM 74LCX540WMX	74LCX540SJ 74LCX540SJX	74LCX540MSA 74LCX540MSAX	74LCX540MTC 74LCX540MTCX
See NS Package Number	M20B	M20D	MSA20	MTC20

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE Output Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		100	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay	1.5 1.5	6.5 6.5	1.5 1.5	7.5 7.5	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5 1.5	8.0 8.0	1.5 1.5	9.0 9.0	ns
t_{PLZ} t_{PHZ}	Output Disable Time	1.5 1.5	7.0 7.0	1.5 1.5	8.0 8.0	ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 1)		1.0 1.0			ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

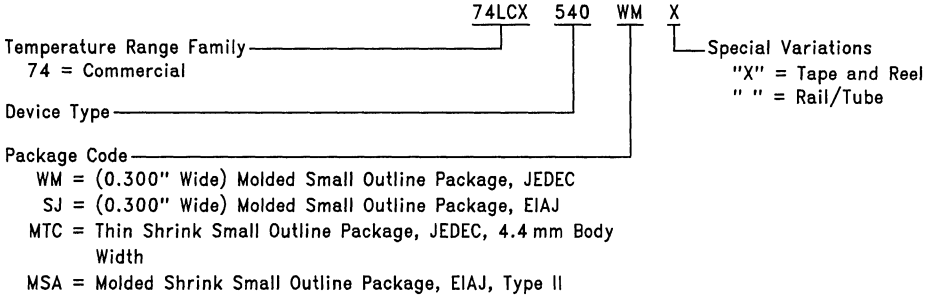
Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	25	pF

74LCX540 Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



TL/F/12403–4

National Semiconductor

PRELIMINARY

74LCX541
Octal Buffer/Line Driver with 5V Tolerant Inputs and Outputs

General Description

The 'LCX541 is an octal buffer/line driver designed to be employed as memory and address drivers, clock drivers and bus oriented transmitter/receivers. The 'LCX541 is a noninverting option of the 'LCX540.

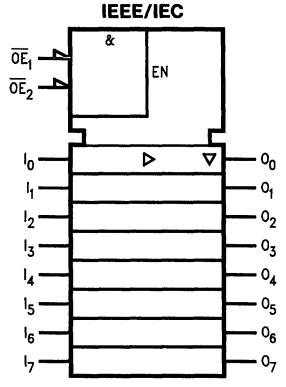
This device is similar in function to the 'LCX244 while providing flow-through architecture (inputs on opposite side from outputs). This pinout arrangement makes this device especially useful as an output port for microprocessors, allowing ease of layout and greater PC board density.

The 'LCX541 is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment. The 'LCX541 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

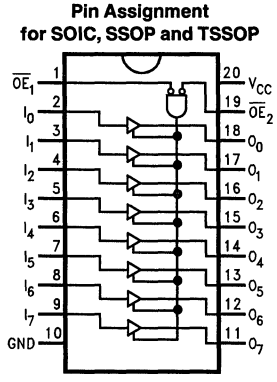
- 5V tolerant input and outputs
- 6.5 ns t_{PD} max, 10 μA I_{CCQ} max
- Power-down high impedance inputs and outputs
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/ EMI reduction circuitry
- Functionally compatible with 74 series 541
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbol



TL/F/12404–1

Connection Diagram



TL/F/12404–2

Truth Table

Inputs			Outputs
$\overline{OE}_1$	$\overline{OE}_2$	I	
L	L	H	H
H	X	X	Z
X	H	X	Z
L	L	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

	SOIC JEDEC	SOIC EIAJ	SSOP Type II	TSSOP JEDEC
Order Number	74LCX541WM 74LCX541WMX	74LCX541SJ 74LCX541SJX	74LCX541MSA 74LCX541MSAX	74LCX541MTC 74LCX541MTCX
See NS Package Number	M20B	M20D	MSA20	MTC20

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE Output Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		100	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics (Preliminary)

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay	1.5 1.5	6.5 6.5	1.5 1.5	7.5 7.5	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5 1.5	8.0 8.0	1.5 1.5	9.0 9.0	ns
t_{PLZ} t_{PHZ}	Output Disable Time	1.5 1.5	7.0 7.0	1.5 1.5	8.0 8.0	ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 1)		1.0 1.0			ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

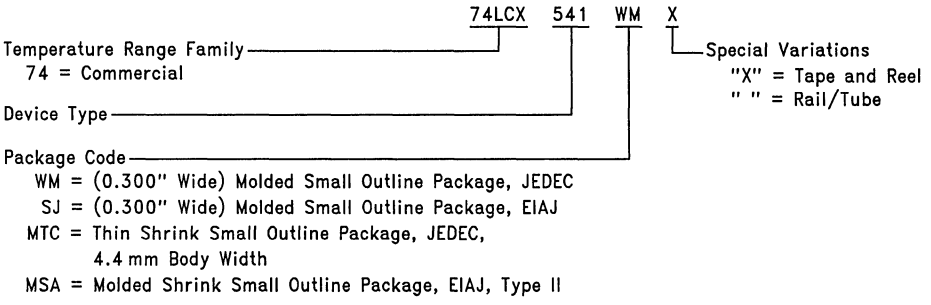
Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$ Typical	Units
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	25	pF

74LCX541 Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



TL/F/12404–4

National Semiconductor

74LCX573
Octal Latch with 5V Tolerant Inputs and Outputs

General Description

The 'LCX573 is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ($\overline{OE}$) inputs.

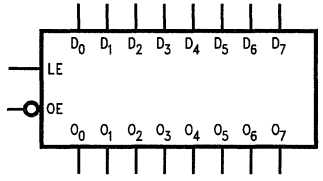
The 'LCX573 is functionally identical to the 'LCX373 but has inputs and outputs on opposite sides.

The 'LCX573 is designed for low voltage (3.3V) applications with capability of interfacing to a 5V signal environment. The 'LCX573 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

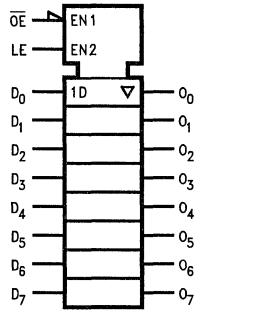
- 5V tolerant inputs and outputs
- 7.0 ns t_{PD} max, 10 μA I_{CCQ} max
- Power down high impedance inputs and outputs
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 573
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbols



TL/F/12405–1

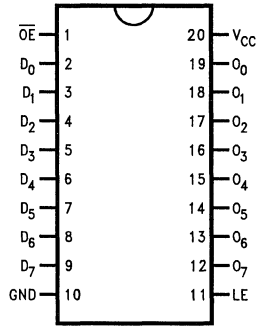
IEEE/IEC



TL/F/12405–2

Connection Diagrams

Pin Assignment for SOIC, SSOP and TSSOP



TL/F/12405–3

Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	TRI-STATE Output Enable Input
O_0–O_7	TRI-STATE Latch Outputs

	SOIC JEDEC	SOIC EIAJ	SSOP TYPE II	TSSOP JEDEC
Order Number	74LCX573WM 74LCX573WMX	74LCX573SJ 74LCX573SJX	74LCX573MSA 74LCX573MSAX	74LCX573MTC 74LCX573MTCX
See NS Package Number	M20B	M20D	MSA20	MTC20

Functional Description

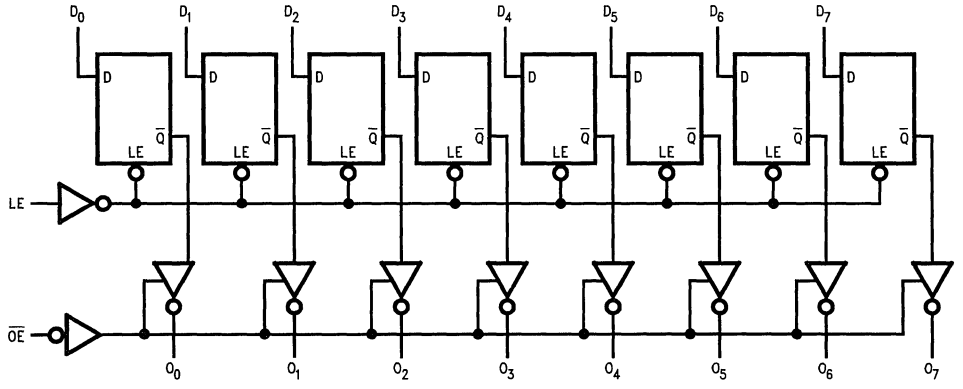
The 'LCX573 contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are enabled. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

Inputs			Outputs
$\overline{OE}$	LE	D	O_n
L	H	H	H
L	H	L	L
L	L	X	O_0
H	X	X	Z

H = HIGH Voltage
L = LOW Voltage
Z = High Impedance
X = Immaterial
O_0 = Previous O_0 before HIGH-to-LOW transition of Latch Enable

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V−3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V−2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE Output Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		100	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay D_n to O_n	1.5 1.5	7.0 7.0	1.5 1.5	7.5 7.5	ns
t_{PHL} t_{PLH}	Propagation Delay LE to O_n	1.5 1.5	7.5 7.5	1.5 1.5	8.5 8.5	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5 1.5	7.5 7.5	1.5 1.5	8.0 8.0	ns
t_{PLZ} t_{PHZ}	Output Disable Time	1.5 1.5	6.0 6.0	1.5 1.5	6.5 6.5	ns
t_S	Setup Time, D_n to LE	2.5		2.5		ns
t_H	Hold Time, D_n to LE	1.5		1.5		ns
t_W	LE Pulse Width	3.3		3.3		ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 1)		1.0 1.0			ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

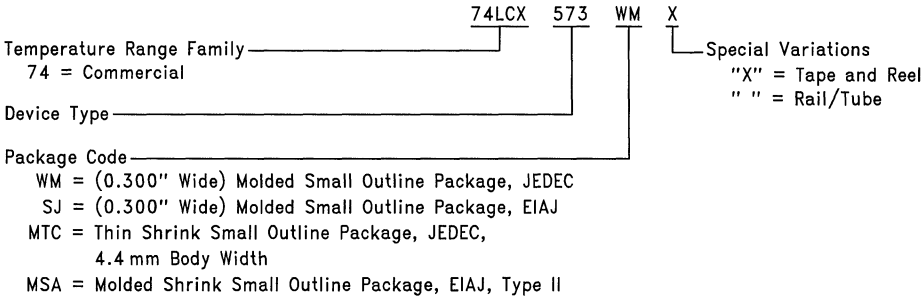
Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	25	pF

74LCX573 Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



TL/F/12405–6

National Semiconductor

74LCX574
Octal D-Type Flip-Flop with 5V Tolerant Inputs and Outputs

General Description

The 'LCX574 is a high-speed, low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable ($\overline{OE}$). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

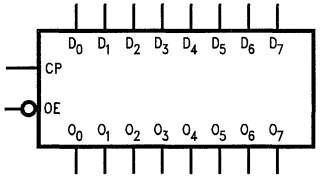
The 'LCX574 is functionally identical to the LCX374 except for the pinouts.

The 'LCX574 is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment. The 'LCX574 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

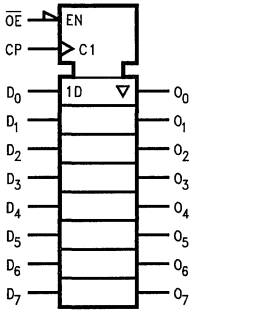
- 5V tolerant inputs and outputs
- 7.5 ns t_{PD} max, 10 μA I_{CCQ} max
- Power down high impedance inputs and outputs
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 574
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbols



TL/F/12406–1

IEEE/IEC

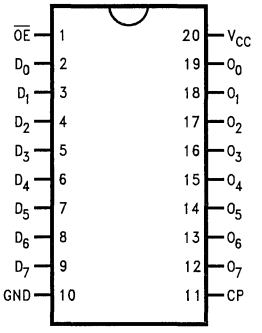


TL/F/12406–4

Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	TRI-STATE® Output Enable Input
O_0–O_7	TRI-STATE Outputs

Connection Diagrams

Pin Assignment for SOIC, SSOP and TSSOP



TL/F/12406–2

	SOIC JEDEC	SOIC EIAJ	SSOP Type II	TSSOP JEDEC
Order Number	74LCX574WM 74LCX574WMX	74LCX574SJ 74LCX574SJX	74LCX574MSA 74LCX574MSAX	74LCX574MTC 74LCX574MTCX
See NS Package Number	M20A	M20D	MSA20	MTC20

Functional Description

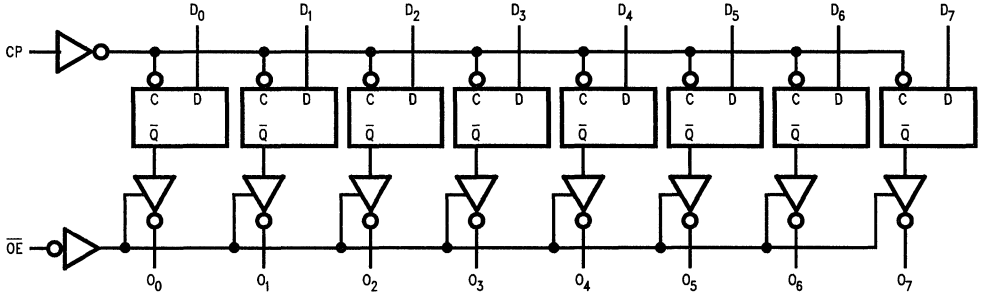
The 'LCX574 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Function Table

Inputs			Internal	Outputs	Function
$\overline{OE}$	CP	D	Q	O_N	
H	H	L	NC	Z	Hold
H	H	H	NC	Z	Hold
H	↗	L	L	Z	Load
H	↗	H	H	Z	Load
L	↗	L	L	L	Data Available
L	↗	H	H	H	Data Available
L	H	L	NC	NC	No Change in Data
L	H	H	NC	NC	No Change in Data

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
↗ = LOW-to-HIGH Transition
NC = No Change

Logic Diagram



TL/F/12406–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V−3.6V V_{CC} = 2.7V		±24 ±12	mA
(T_A)	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE Output Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		100	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	150				MHz
t_{PHL} t_{PLH}	Propagation Delay CP to O_n	1.5 1.5	7.5 7.5	1.5 1.5	8.5 8.5	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5 1.5	7.5 7.5	1.5 1.5	8.0 8.0	ns
t_{PLZ} t_{PHZ}	Output Disable Time	1.5 1.5	6.0 6.0	1.5 1.5	6.5 6.5	ns
t_S	Setup Time	2.5		2.5		ns
t_H	Hold Time	1.5		1.5		ns
t_W	Pulse Width	3.3		3.3		ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 1)		1.0 1.0			ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	25	pF

74LCX574 Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

74LCX 574 WM X

Temperature Range Family
74 = Commercial

Device Type

Package Code
WM = (0.300" Wide) Molded Small Outline Package, JEDEC
SJ = (0.300" Wide) Molded Small Outline Package, EIAJ
MTC = Thin Shrink Small Outline Package, JEDEC, 4.4 mm Body Width
MSA = Molded Shrink Small Outline Package, EIAJ, Type II

Special Variations
"X" = Tape and Reel
" " = Rail/Tube

TL/F/12406–6

National Semiconductor

74LCX646
Low-Voltage Octal Transceiver/Register with 5V Tolerant Inputs and Outputs

General Description

The LCX646 consists of registered bus transceiver circuits, with outputs, D-type flip-flops, and control circuitry providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Data on the A or B bus will be loaded into the respective registers on the LOW-to-HIGH transition of the appropriate pin (CPAB or CPBA). The four fundamental handling functions available are illustrated in *Figure 1* through *Figure 4*.

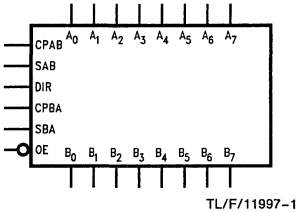
The LCX646 is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX646 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs and outputs
- 7.0 ns t_{PD} max, 10 μA I_{CCQ} max
- Power down high impedance inputs and outputs
- 2.0V–3.6V V_{CC} supply operation
- ±2.4 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with the 74 series 646
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbols



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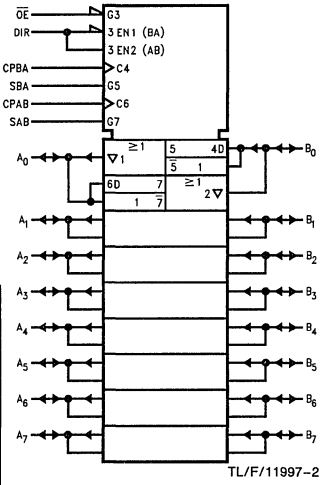
IEEE/IEC

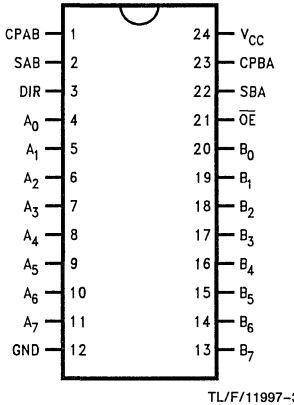


TL/F/11997–2

Pin Names	Description
A_0–A_7	Data Register A Inputs Data Register A Outputs
B_0–B_7	Data Register B Inputs Data Register B Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Transmit/Receive Inputs
$\overline{G}$	Output Enable Input
DIR	Direction Control Input

Connection Diagram

Pin Assignment for SOIC, SSOP and TSSOP



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	SOIC JEDEC	SSOP Type II	TSSOP
Order Number	74LCX646WM 74LCX646WMX	74LCX646MSA 74LCX646MSAX	74LCX646MTC 74LCX646MTCX
See NS Package Number	M24B	MSA24	MTC24

Real Time Transfer A-Bus to B-Bus

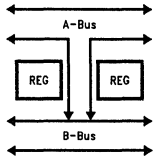

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FIGURE 1

Real Time Transfer B-Bus to A-Bus

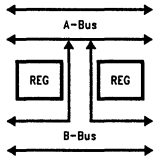

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FIGURE 2

Storage from Bus to Register

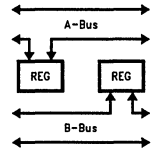

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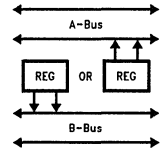
FIGURE 3

Transfer from Register to Bus



TL/F/11997–7

FIGURE 4

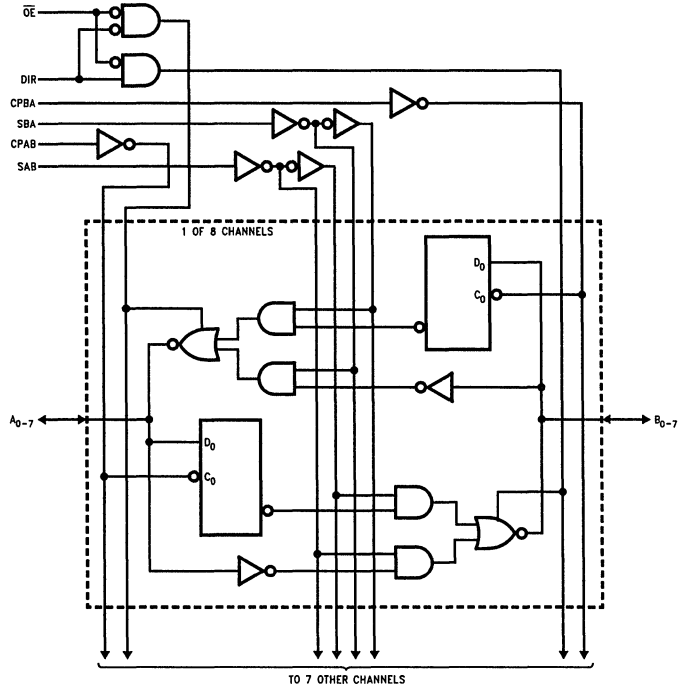
Function Table (Note)

Inputs						Data I/O		Function
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA	A_0–A_7	B_0–B_7	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	↗	X	X	X			Clock A_n Data into A Register
H	X	X	↗	X	X			Clock B_n Data into B Register
L	H	X	X	L	X	Input	Output	A_n to B_n—Real Time (Transparent Mode)
L	H	↗	X	L	X			Clock A_n Data into A Register
L	H	H or L	X	H	X			A Register to B_n (Stored Mode)
L	H	↗	X	H	X			Clock A_n Data into A Register and Output to B_n
L	L	X	X	X	L	Output	Input	B_n to A_n—Real Time (Transparent Mode)
L	L	X	↗	X	L			Clock B_n Data into B Register
L	L	X	H or L	X	H			B Register to A_n (Stored Mode)
L	L	X	↗	X	H			Clock B_n Data into B Register and Output to A_n

Note: The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs.

H = HIGH Voltage Level X = Immaterial L = LOW Voltage Level ↗ = LOW-to-HIGH Transition

Logic Diagram



TL/F/11997–8

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE®	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE I/O Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		100	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	150				MHz
t_{PHL} t_{PLH}	Propagation Delay Bus to Bus	1.5 1.5	7.0 7.0	1.5 1.5	8.0 8.0	ns
t_{PHL} t_{PLH}	Propagation Delay Clock to Bus	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_{PHL} t_{PLH}	Propagation Delay Select to Bus	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_{PLZ} t_{PHZ}	Output Disable Time	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_S	Setup Time	2.5		2.5		ns
t_H	Hold Time	1.5		1.5		ns
t_W	Pulse Width	3.3		3.3		ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 1)		1.0 1.0			ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

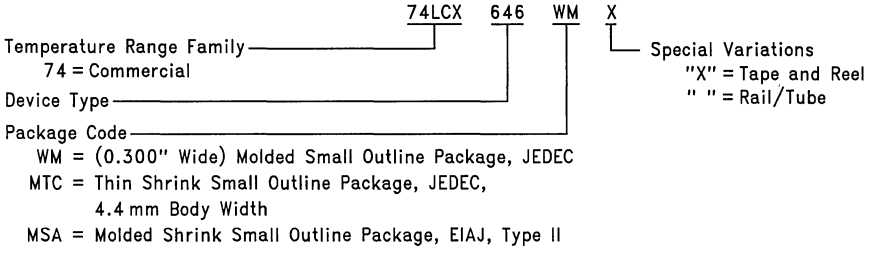
Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
$C_{I/O}$	Input/Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	25	pF

74LCX646 Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



TL/F/11997–9

National Semiconductor

74LCX652
Low-Voltage Transceiver/Register with 5V Tolerant Inputs and Outputs

General Description

The LCX652 consists of bus transceiver circuits with D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to the HIGH logic level. Output Enable pins (OEAB, $\overline{OEBA}$) are provided to control the transceiver function.

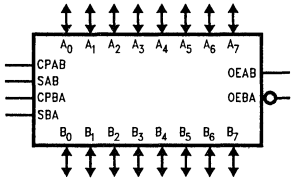
The LCX652 is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX652 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

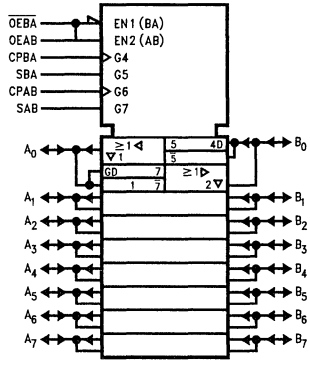
- 5V tolerant inputs and outputs
- 7.0 ns t_{PD} max, 10 μA I_{CCQ} max
- Power down high impedance inputs and outputs
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 652
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbols



TL/F/11998–3

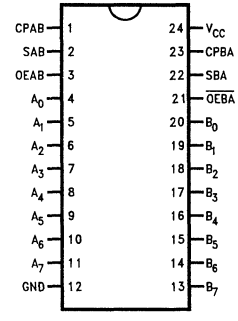
IEEE/IEC



TL/F/11998–1

Connection Diagram

Pin Assignment for SOIC, SSOP and TSSOP



TL/F/11998–2

Pin Names	Description
A_0–A_7, B_0–B_7	A and B Inputs/TRI-STATE® Outputs
CPAB, CPBA	Clock Inputs
SAB, SBA	Select Inputs
OEAB, $\overline{OEBA}$	Output Enable Inputs

	SOIC JEDEC	SSOP Type II	TSSOP JEDEC
Order Number	74LCX652WM 74LCX652WMX	74LCX652MSA 74LCX652MSAX	74LCX652MTC 74LCX652MTCX
See NS Package Number	M24B	MSA24	MTC24

Functional Description

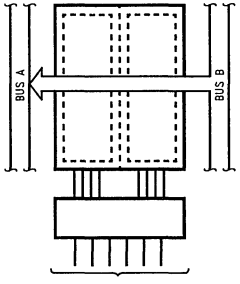
In the transceiver mode, data present at the HIGH impedance port may be stored in either the A or B register or both.

The select (SAB, SBA) controls can multiplex stored and real-time.

The examples in *Figure 1* demonstrate the four fundamental bus-management functions that can be performed with the Octal bus transceivers and receivers.

Data on the A or B data bus, or both can be stored in the internal D flip-flop by LOW to HIGH transitions at the appropriate Clock Inputs (CPAB, CPBA) regardless of the Select or Output Enable Inputs. When SAB and SBA are in the real time transfer mode, it is also possible to store data without using the internal D flip-flops by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. In this configuration each Output reinforces its Input. Thus when all other data sources to the two sets of bus lines are in a HIGH impedance state, each set of bus lines will remain at its last state.

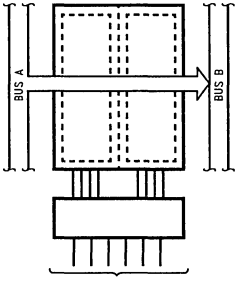
Real-Time Transfer
Bus B to Bus A



TL/F/11998–5

OEAB	$\overline{\text{OEBA}}$	CPAB	CPBA	SAB	SBA
L	L	X	X	X	L

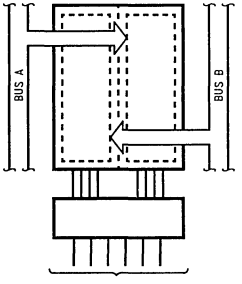
Real-Time Transfer
Bus A to Bus B



TL/F/11998–6

OEAB	$\overline{\text{OEBA}}$	CPAB	CPBA	SAB	SBA
H	H	X	X	L	X

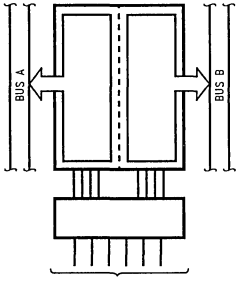
Storage



TL/F/11998–7

OEAB	$\overline{\text{OEBA}}$	CPAB	CPBA	SAB	SBA
X	H	↓	X	X	X
L	X	X	↓	X	X
L	H	↓	↓	X	X

Transfer Storage
Data to A or B

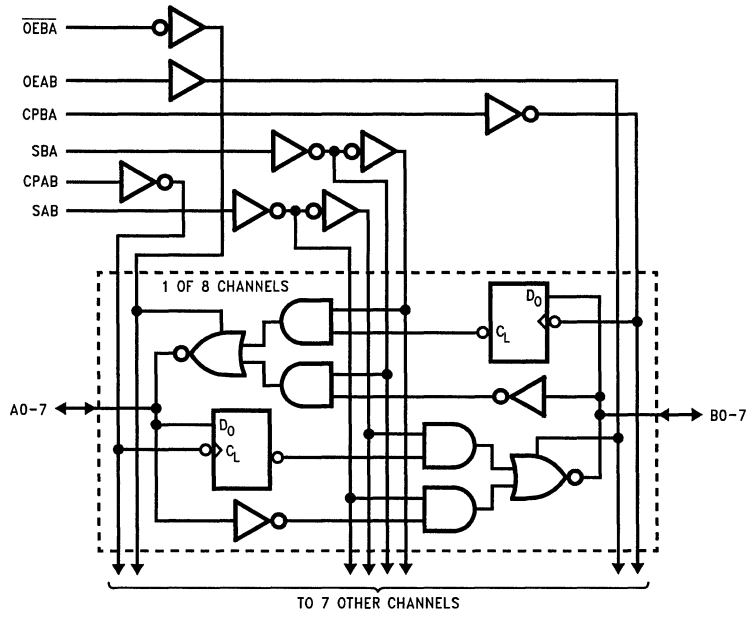


TL/F/11998–8

OEAB	$\overline{\text{OEBA}}$	CPAB	CPBA	SAB	SBA
H	L	H or L	H or L	H	H

FIGURE 1

Logic Diagram



TL/F/11998–4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Function Table (Note)

Inputs						Inputs/Outputs		Operating Mode
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA	A_0 thru A_7	B_0 thru B_7	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	⌐	⌐	X	X			Store A and B Data
X	H	⌐	H or L	X	X	Input	Not Specified	Store A, Hold B
H	H	⌐	⌐	X	X	Input	Output	Store A in Both Registers
L	X	H or L	⌐	X	X	Not Specified	Input	Hold A, Store B
L	L	⌐	⌐	X	X	Output	Input	Store B in Both Registers
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Store B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW to HIGH Clock Transition

Note: The data output functions may be enabled or disabled by various signals at OEAB or OEBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW to HIGH transition on the clock inputs.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V–3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE I/O Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		100	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency	150				MHz
t_{PHL} t_{PLH}	Propagation Delay Bus to Bus	1.5 1.5	7.0 7.0	1.5 1.5	8.0 8.0	ns
t_{PHL} t_{PLH}	Propagation Delay Clock to Bus	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_{PHL} t_{PLH}	Propagation Delay Select to Bus	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_{PLZ} t_{PHZ}	Output Disable Time	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_S	Setup Time	2.5		2.5		ns
t_H	Hold Time	1.5		1.5		ns
t_W	Pulse Width	3.3		3.3		ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 1)		1.0 1.0			ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Dynamic Switching Characteristics

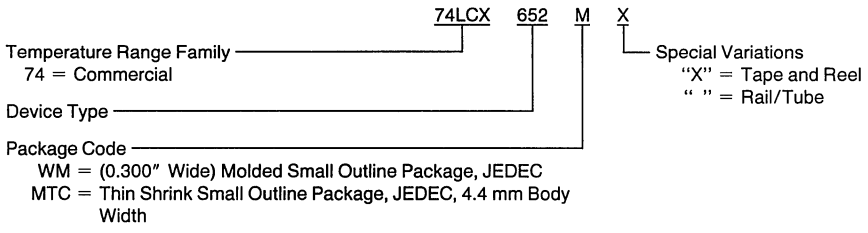
Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Unit
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
$C_{I/O}$	Input/Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	25	pF

74LCX652 Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



National Semiconductor

74LCX16240
Low-Voltage 16-Bit Inverting Buffer/Line Driver with 5V Tolerant Inputs/Outputs

General Description

The LCX16240 contains sixteen inverting buffers with TRI-STATE® outputs designed to be employed as a memory and address driver, clock driver, or bus-oriented transmitter/receiver. The device is nibble controlled. Each nibble has separate TRI-STATE control inputs which can be shorted together for full 16-bit operation.

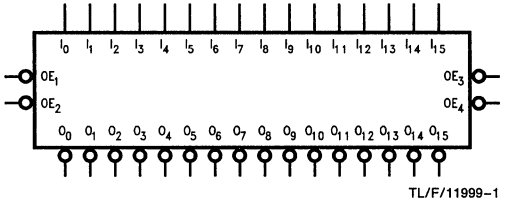
The LCX16240 is designed for low voltage (3.3V) V_{CC} applications with capacity of interfacing to a 5V signal environment.

The LCX16240 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 4.5 ns t_{PD} max, 20 μA I_{CCQ} max
- 5V tolerant inputs and outputs
- Power down high impedance inputs and outputs
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with the 74 series 16240
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2500V
  Machine model > 200V

Logic Symbol



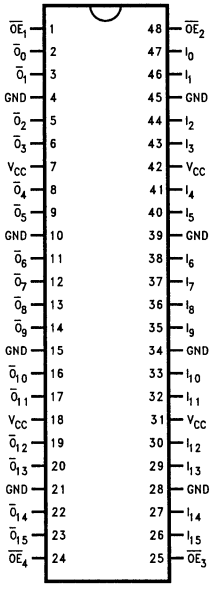
TL/F/11999–1

Pin Names	Description
$\overline{OE}_n$	Output Enable Inputs (Active Low)
I_0–I_{15}	Inputs
$\overline{O}_0$–$\overline{O}_{15}$	Outputs

	SSOP	TSSOP
Order Number	74LCX16240MEA 74LCX16240MEAX	74LCX16240MTD 74LCX16240MTDX
See NS Package Number	MS48A	MTD48

Connection Diagram

Pin Assignment for SSOP and TSSOP

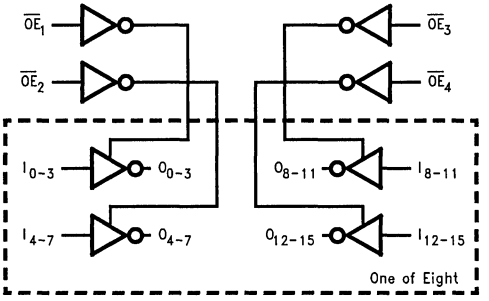


TL/F/11999–2

Functional Description

The LCX16240 contains sixteen inverting buffers with TRI-STATE standard outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of the other. The control pins may be shorted together to obtain full 16-bit operation. The TRI-STATE outputs are controlled by an Output Enable ($\overline{OE}_n$) input for each nibble. When $\overline{OE}_n$ is LOW, the outputs are in 2-state mode. When $\overline{OE}_n$ is HIGH, the outputs are in the high impedance mode, but this does not interfere with entering new data into the inputs.

Logic Diagram



TL/F/11999–3

Truth Tables

Inputs		Outputs
$\overline{OE}_1$	I_0–I_3	$\overline{O}_0$–$\overline{O}_3$
L	L	H
L	H	L
H	X	Z

Inputs		Outputs
$\overline{OE}_2$	I_4–I_7	$\overline{O}_4$–$\overline{O}_7$
L	L	H
L	H	L
H	X	Z

Inputs		Outputs
$\overline{OE}_3$	I_8–I_{11}	$\overline{O}_8$–$\overline{O}_{11}$
L	L	H
L	H	L
H	X	Z

Inputs		Outputs
$\overline{OE}_4$	I_{12}–I_{15}	$\overline{O}_{12}$–$\overline{O}_{15}$
L	L	H
L	H	L
H	X	Z

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE Output Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		100	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		20	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±20	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay Data to Output	1.5 1.5	4.5 4.5	1.5 1.5	5.3 5.3	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5 1.5	5.4 5.4	1.5 1.5	6.0 6.0	ns
t_{PLZ} t_{PHZ}	Output Disable Time	1.5 1.5	5.3 5.3	1.5 1.5	5.4 5.4	ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 1)		1.0 1.0			ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagaton delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

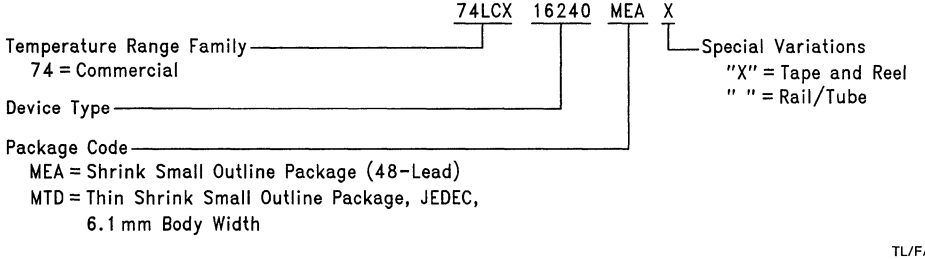
Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Unit
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	20	pF

74LCX16240 Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



TL/F/11999–4

National Semiconductor

74LCX16244
Low-Voltage 16-Bit Buffer/Line Driver with 5V Tolerant Inputs and Outputs

General Description

The 74LCX16244 contains sixteen non-inverting buffers with TRI-STATE® outputs designed to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is nibble controlled. Each nibble has separate TRI-STATE control inputs which can be shorted together for full 16-bit operation.

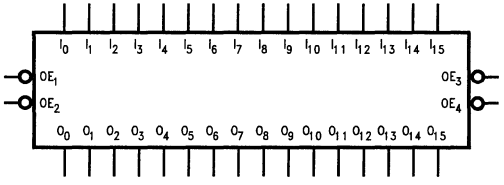
The LCX16244 is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX16244 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs and outputs
- 4.5 ns t_{PD} max, 10 μA I_{CCQ} max
- Power down high impedance inputs and outputs
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 16244
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbol



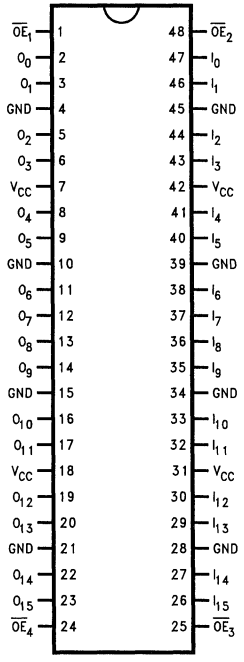
TL/F/12000–1

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active Low)
I_0–I_{15}	Inputs
O_0–O_{15}	Outputs

	SSOP	TSSOP
Order Number	74LCX16244MEA 74LCX16244MEAX	74LCX16244MTD 74LCX16244MTDX
See NS Package Number	MS48A	MTD48

Connection Diagram

Pin Assignment for SSOP and TSSOP



TL/F/12000–2

Functional Description

The LCX16244 contains sixteen non-inverting buffers with TRI-STATE standard outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation. The TRI-STATE outputs are controlled by an Output Enable ($\overline{OE}_n$) input for each nibble. When $\overline{OE}_n$ is LOW, the outputs are in 2-state mode. When $\overline{OE}_n$ is HIGH, the outputs are in the high impedance mode, but this does not interfere with entering new data into the inputs.

Truth Tables

Inputs		Outputs
$\overline{OE}_1$	I_0–I_3	O_0–O_3
L	L	L
L	H	H
H	X	Z

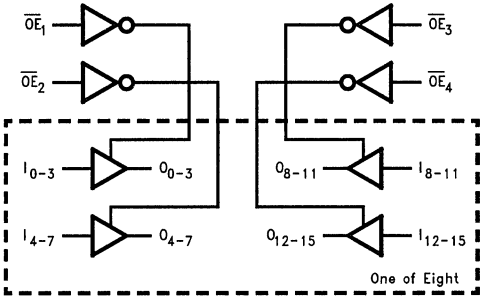
Inputs		Outputs
$\overline{OE}_2$	I_4–I_7	O_4–O_7
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_3$	I_8–I_{11}	O_8–O_{11}
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_4$	I_{12}–I_{15}	O_{12}–O_{15}
L	L	L
L	H	H
H	X	Z

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



TL/F/12000–3

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V–3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE Output Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		100	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		20	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±20	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay Data to Output	1.5 1.5	4.5 4.5	1.5 1.5	5.2 5.2	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5 1.5	5.5 5.5	1.5 1.5	6.3 6.3	ns
t_{PLZ} t_{PHZ}	Output Disable Time	1.5 1.5	5.4 5.4	1.5 1.5	5.7 5.7	ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 1)		1.0 1.0			ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Dynamic Switching Characteristics

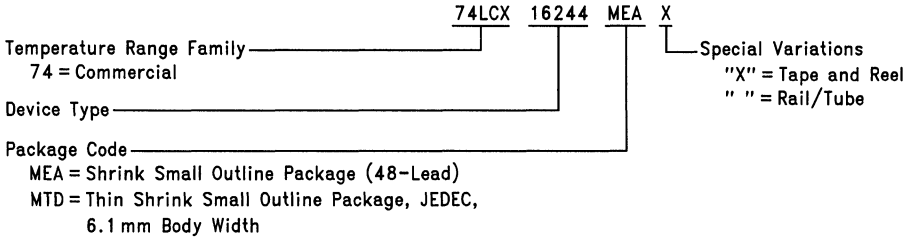
Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	20	pF

74LCX16244 Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



TL/F/12000–4

National Semiconductor

74LCX16245
Low-Voltage 16-Bit Bidirectional Transceiver with 5V Tolerant Inputs and Outputs

General Description

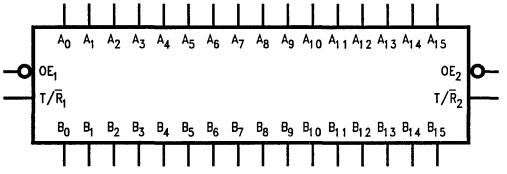
The 74LCX16245 contains sixteen non-inverting bidirectional buffers with TRI-STATE® outputs and is intended for bus oriented applications. The device is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment. The device is byte controlled. Each byte has separate control inputs which could be shorted together for full 16-bit operation. The $T/\overline{R}$ inputs determine the direction of data flow through the device. The $\overline{OE}$ inputs disable both the A and B ports by placing them in a high impedance state.

The LCX16245 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 4.5 ns t_{PD} max, 20 μA I_{CCQ} max
- 5V tolerant inputs and outputs
- Power down high impedance inputs and outputs
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 16245
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbol



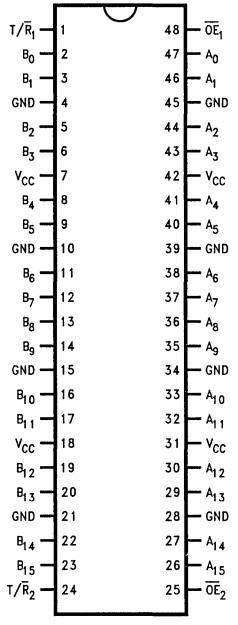
TL/F/12001–1

Pin Names	Description
$\overline{OE}$	Output Enable Input
$T/\overline{R}$	Transmit/Receive Input
A_0–A_{15}	Side A Inputs or TRI-STATE Outputs
B_0–B_{15}	Side B Inputs or TRI-STATE Outputs

	SSOP	TSSOP
Order Number	74LCX16245MEA 74LCX16245MEAX	74LCX16245MTD 74LCX16245MTDX
See NS Package Number	MS48A	MTD48

Connection Diagram

Pin Assignment for SSOP and TSSOP



TL/F/12001–2

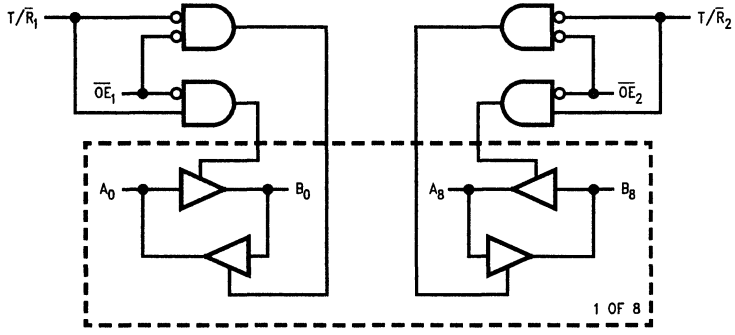
Truth Tables

Inputs		Outputs
$\overline{OE}_1$	$T/\overline{R}_1$	
L	L	Bus B_0–B_7 Data to Bus A_0–A_7
L	H	Bus A_0–A_7 Data to Bus B_0–B_7
H	X	HIGH Z State on A_0–A_7, B_0–B_7

Inputs		Outputs
$\overline{OE}_2$	$T/\overline{R}_2$	
L	L	Bus B_8–B_{15} Data to Bus A_8–A_{15}
L	H	Bus A_8–A_{15} Data to Bus B_8–B_{15}
H	X	HIGH Z State on A_8–A_{15}, B_8–B_{15}

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



TL/F/12001–3

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	3.6	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE I/O Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		100	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		20	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±20	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay A_n to B_n or B_n to A_n	1.5 1.5	4.5 4.5	1.5 1.5	5.2 5.2	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5 1.5	6.5 6.5	1.5 1.5	7.2 7.2	ns
t_{PLZ} t_{PHZ}	Output Disable Time	1.5 1.5	6.4 6.4	1.5 1.5	6.9 6.9	ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 1)		1.0 1.0			ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Dynamic Switching Characteristics

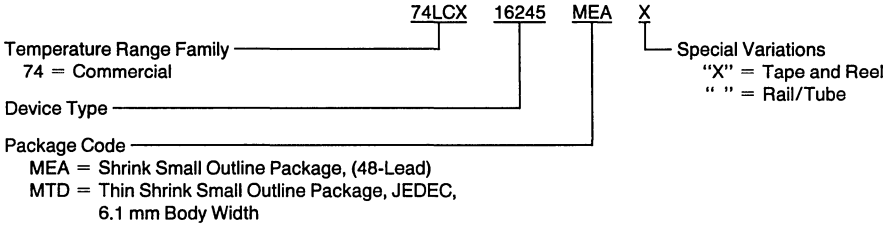
Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	20	pF

74LCX16245 Ordering Information

The device number is used to form part of a simplified purchasing code where the package type is defined as follows:



National Semiconductor

74LCX16373
Low-Voltage 16-Bit Transparent Latch with 5V Tolerant Inputs and Outputs

General Description

The LCX16373 contains sixteen non-inverting latches with TRI-STATE® outputs and is intended for bus oriented applications. The device is byte controlled. The flip-flops appear transparent to the data when the Latch Enable (LE) is HIGH. When LE is low, the data that meets the setup time is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH, the outputs are in high Z state.

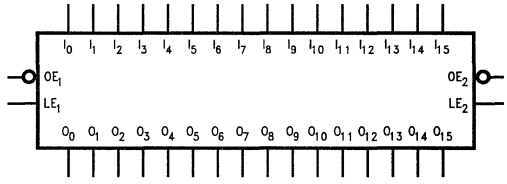
The LCX16373 is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX16373 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5.4 ns t_{PD} max, 20 μA I_{CCQ} max
- 5V tolerant inputs and outputs
- Power down high impedance inputs and outputs
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with the 74 series 16373
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbol



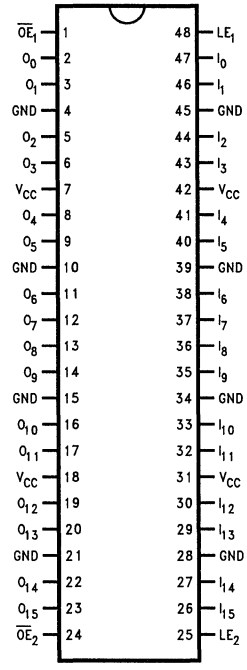
TL/F/12002–1

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active Low)
LE_n	Latch Enable Input
I_0–I_{15}	Inputs
O_0–O_{15}	Outputs

	SSOP	TSSOP
Order Number	74LCX16373MEA 74LCX16373MEAX	74LCX16373MTD 74LCX16373MTDX
See NS Package Number	MS48A	MTD48

Connection Diagram

Pin Assignment for SSOP and TSSOP



TL/F/12002–2

Functional Description

The LCX16373 contains sixteen D-type latches with TRI-STATE standard outputs. The device is byte controlled with each byte functioning identically, but independent of the other. Control pins can be shorted together to obtain full 16-bit operation. The following description applies to each byte. When the Latch Enable (LE_n) input is HIGH, data on the D_n enters the latches. In this condition the latches are transparent, i.e. a latch output will change states each time its D input changes. When LE_n is LOW, the latches store information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE_n. The TRI-STATE standard outputs are controlled by the Output Enable ($\overline{OE}_n$) input. When $\overline{OE}_n$ is LOW, the standard outputs are in the 2-state mode. When $\overline{OE}_n$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

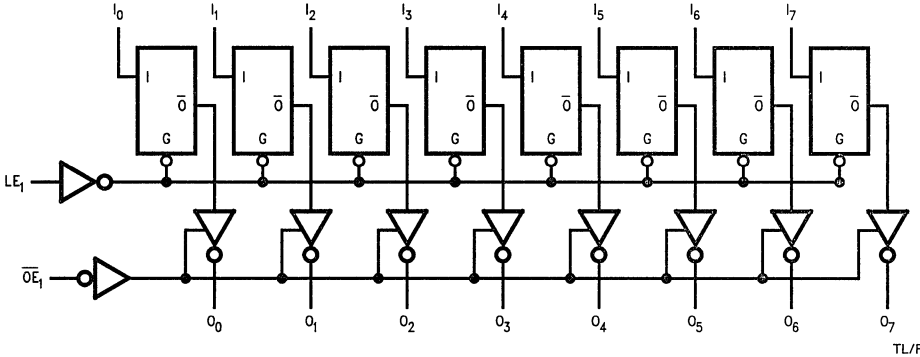
Truth Tables

Inputs			Outputs
LE_1	$\overline{OE}_1$	I_0–I_7	O_0–O_7
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

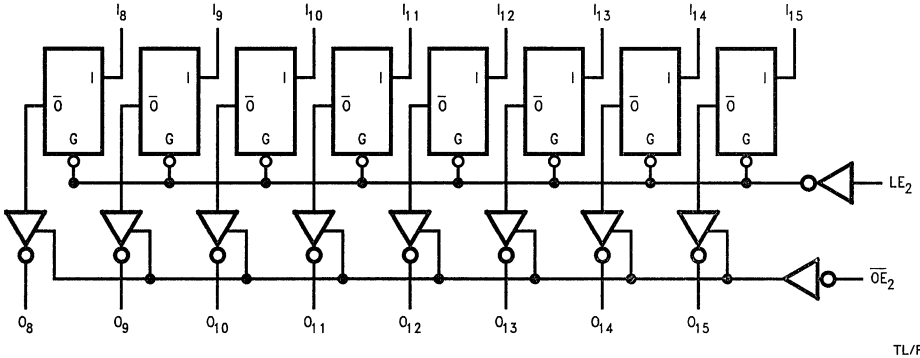
Inputs			Outputs
LE_2	$\overline{OE}_2$	I_8–I_{15}	O_8–O_{15}
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance
O_0 = Previous O_0 before HIGH to LOW transition of Latch Enable

Logic Diagrams



TL/F/12002–3



TL/F/12002–4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V–3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE Output Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		100	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		20	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±20	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay D_n to O_n	1.5 1.5	5.4 5.4	1.5 1.5	5.9 5.9	ns
t_{PHL} t_{PLH}	Propagation Delay LE to O_n	1.5 1.5	5.5 5.5	1.5 1.5	6.4 6.4	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5 1.5	6.1 6.1	1.5 1.5	6.5 6.5	ns
t_{PLZ} t_{PHZ}	Output Disable Time	1.5 1.5	6.0 6.0	1.5 1.5	6.3 6.3	ns
t_S	Setup Time, D_n to LE	2.5		2.5		ns
t_H	Hold Time, D_n to LE	1.5		1.5		ns
t_W	LE Pulse Width	3.0		3.0		ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 1)		1.0 1.0			ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Dynamic Switching Characteristics

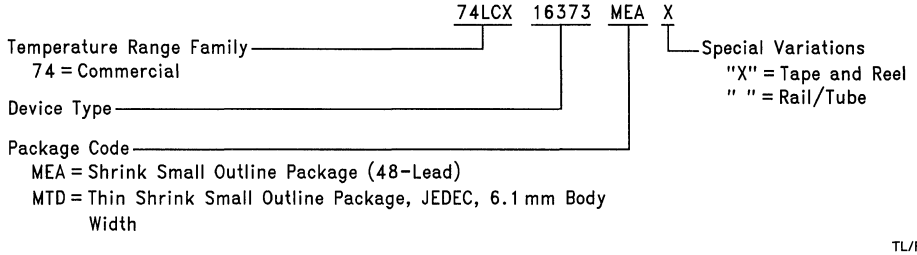
Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	20	pF

74LCX16373 Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



TL/F/12002–5

National Semiconductor

74LCX16374
Low-Voltage 16-Bit D Flip-Flop with 5V Tolerant Inputs and Outputs

General Description

The LCX16374 contains sixteen non-inverting D flip-flops with TRI-STATE® outputs and is intended for bus oriented applications. The device is byte controlled. A buffered clock (CP) and Output Enable (CE) are common to each byte and can be shorted together for full 16-bit operation.

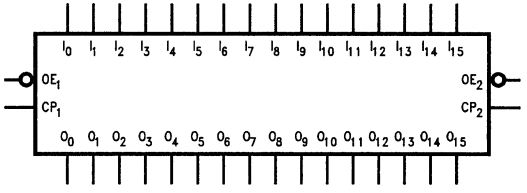
The LCX16374 is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX16374 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 6.2 ns t_{PD} max, 20 μA I_{CCQ} max
- 5V tolerant inputs and outputs
- Power down high impedance inputs and outputs
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with the 74 series 16374
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbol



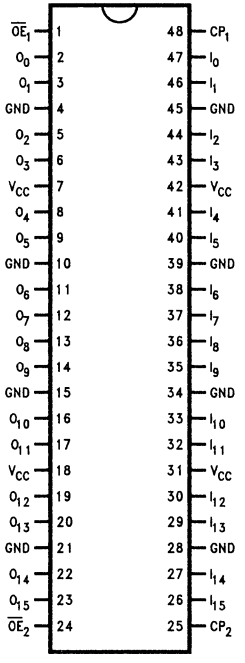
TL/F/12003–1

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active Low)
CP_n	Clock Pulse Input
I_0–I_{15}	Inputs
O_0–O_{15}	Outputs

	SSOP	TSSOP
Order Number	74LCX16374MEA 74LCX16374MEAX	74LCX16374MTD 74LCX16374MTDX
See NS Package Number	MS48A	MTD48

Connection Diagram

Pin Assignment for SSOP and TSSOP



TL/F/12003–2

Functional Description

The LCX16374 consists of sixteen edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation. Each byte has a buffered clock and buffered Output Enable common to all flip-flops within that byte. The description which follows applies to each byte. Each flip-flop will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP_n) transition. With the Output Enable ($\overline{OE}_n$) LOW, the contents of the flip-flops are available at the outputs. When $\overline{OE}_n$ is HIGH, the outputs go to the high impedance state. Operation of the OE_n input does not affect the state of the flip-flops.

Truth Tables

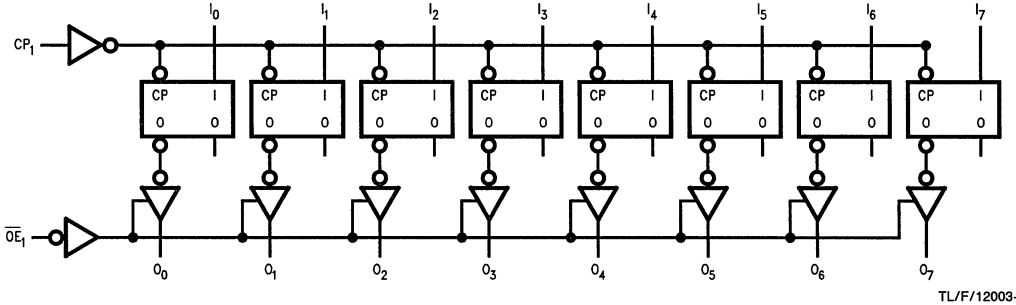
Inputs			Outputs
CP_1	$\overline{OE}_1$	I_0–I_7	O_0–O_7
↑	L	H	H
↑	L	L	L
L	L	X	O_0
X	H	X	Z

Inputs			Outputs
CP_2	$\overline{OE}_2$	I_8–I_{15}	O_8–O_{15}
↑	L	H	H
↑	L	L	L
L	L	X	O_0
X	H	X	Z

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance
O_0 = Previous O_0 before HIGH to LOW of CP

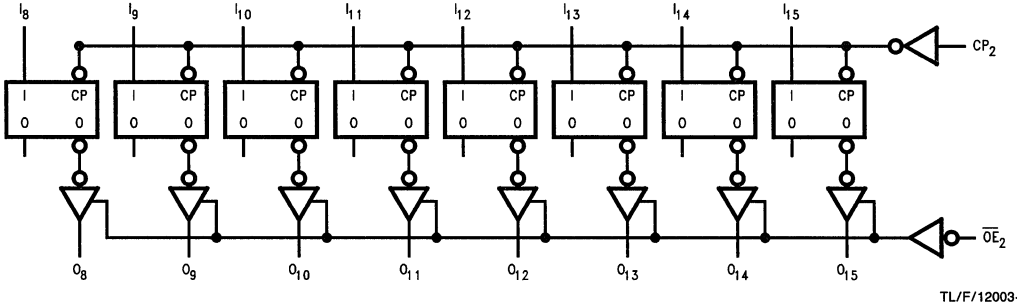
Logic Diagrams

Byte 1 (0:7)



TL/F/12003–3

Byte 2 (8:15)



TL/F/12003–4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE Output Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		100	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		20	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±20	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	170				MHz
t_{PHL} t_{PLH}	Propagation Delay CP to O_n	1.5 1.5	6.2 6.2	1.5 1.5	6.5 6.5	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5 1.5	6.1 6.1	1.5 1.5	6.3 6.3	ns
t_{PLZ} t_{PHZ}	Output Disable Time	1.5 1.5	6.0 6.0	1.5 1.5	6.2 6.2	ns
t_S	Setup Time	2.5		2.5		ns
t_H	Hold Time	1.5		1.5		ns
t_W	Pulse Width	3.0		3.0		ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 1)		1.0 1.0			ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two seperate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Dynamic Switching Characteristics

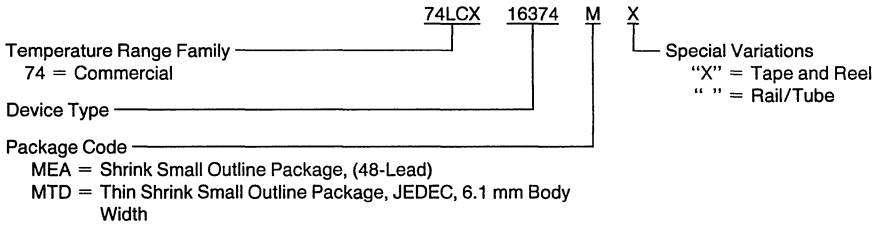
Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	20	pF

74LCX16374 Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



National Semiconductor

PRELIMINARY

74LCX16500
18-Bit Universal Bus Transceivers with 5V Tolerant Inputs and Outputs

General Description

These 18-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable (OEAB and $\overline{\text{OEBA}}$), latch-enable (LEAB and LEBA), and clock ($\overline{\text{CLKAB}}$ and $\overline{\text{CLKBA}}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{\text{CLKAB}}$ is held at a high or low logic level. If LEAB is low, the A bus data is stored in the latch/flip-flop on the high-to-low transition of $\overline{\text{CLKAB}}$. Output-enable OEAB is active-high. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{\text{OEBA}}$, LEBA, and $\overline{\text{CLKBA}}$. The output enables are complementary (OEAB is active high and $\overline{\text{OEBA}}$ is active low).

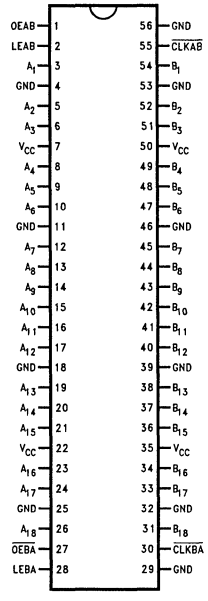
To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Features

- 6.0 ns t_{PD} max, 20 µA I_{CCQ} max
- 5V tolerant inputs and outputs
- Power down high impedance inputs and outputs
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 16500
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Connection Diagram

Pin Assignment for SSOP and TSSOP



TL/F/12407–1

Function Table†

Inputs				Output
OEAB	LEAB	$\overline{\text{CLKAB}}$	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	B_0‡
H	L	L	X	B_0§

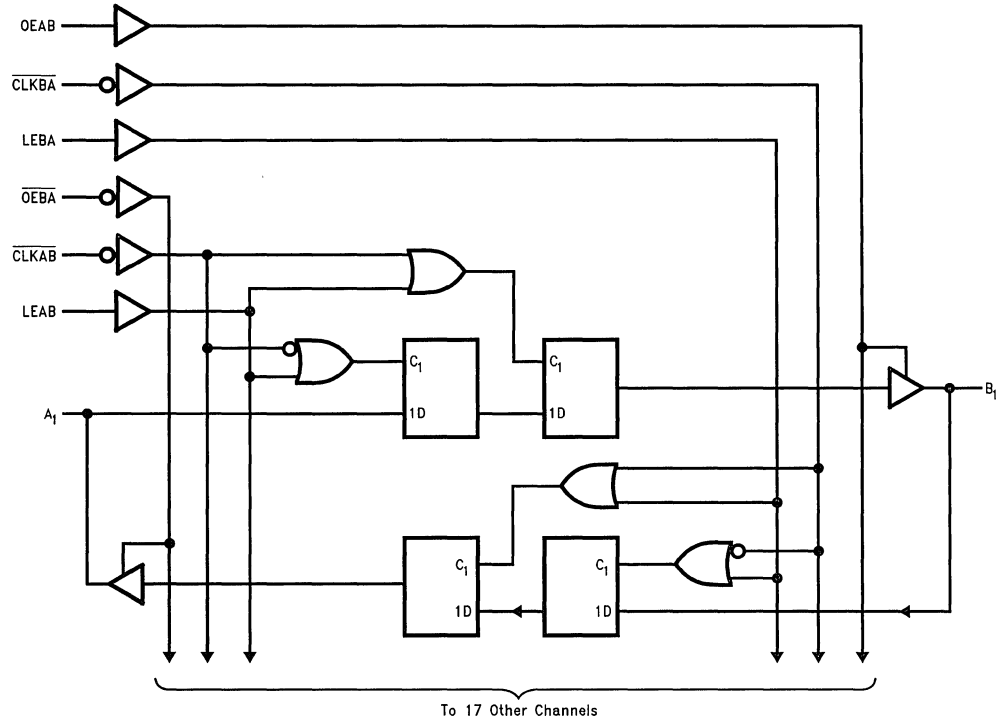
† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{\text{OEBA}}$, LEBA, and $\overline{\text{CLKBA}}$.

‡ Output level before the indicated steady-state input conditions were established.

§ Output level before the indicated steady-state input conditions were established, provided that $\overline{\text{CLKAB}}$ was low before LEAB went low.

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

Logic Diagram



TL/F/12407–2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE®	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE I/O Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		100	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		20	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±20	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max (Note 1)	Min	Max (Note 1)	
f_{max}	Maximum Clock Frequency	170				MHz
t_{PHL} t_{PLH}	Propagation Delay Bus to Bus	1.5 1.5	6.0 6.0	1.5 1.5	7.0 7.0	ns
t_{PHL} t_{PLH}	Propagation Delay Clock to Bus	1.5 1.5	6.5 6.5	1.5 1.5	7.5 7.5	ns
t_{PHL} t_{PLH}	Propagation Delay LE to Bus	1.5 1.5	6.5 6.5	1.5 1.5	7.5 7.5	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5 1.5	7.5 7.5	1.5 1.5	8.5 8.5	ns
t_{PLZ} t_{PHZ}	Output Disable Time	1.5 1.5	6.0 6.0	1.5 1.5	7.0 7.0	ns
t_S	Setup Time	2.5		2.5		ns
t_H	Hold Time	1.5		1.5		ns
t_W	Pulse Width	3.0		3.0		ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 2)		1.0 1.0			ns

Note 1: The Maximum AC limits are design target. Actual performance will be specified upon completion of characterization.

Note 2: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}), or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

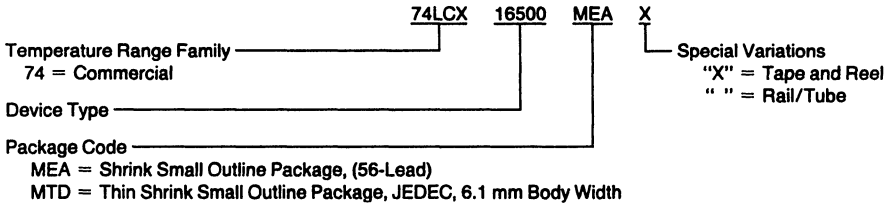
Symbol	Parameter	Conditions	V_{CC} (V)	T_A = 25°C Typical	Units
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	C_L = 50 pF, V_{IH} = 3.3V, V_{IL} = 0V	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	C_L = 50 pF, V_{IH} = 3.3V, V_{IL} = 0V	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, V_I = 0V or V_{CC}	7	pF
C_{OUT}	Output Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}, F = 10 MHz	20	pF

74LCX16500 Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



National Semiconductor

PRELIMINARY

74LCX16646
Low-Voltage 16-Bit Transceiver/Register with 5V Tolerant Inputs and Outputs

General Description

The LCX16646 contains sixteen non-inverting bidirectional registered bus transceivers with TRI-STATE® outputs, providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Each byte has separate control inputs which can be shorted together for full 16-bit operation. The DIR inputs determine the direction of data flow through the device. The CPAB and CPBA inputs load data into the registers on the LOW-to-HIGH transition. The four fundamental handling functions available are illustrated in *Figure 1* thru *Figure 4*.

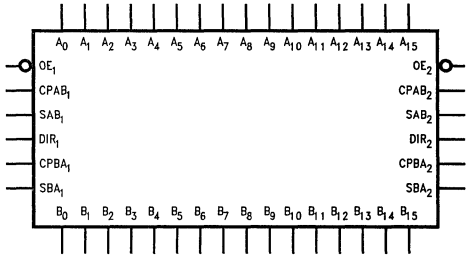
The LCX16646 is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX16646 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5.0 ns t_{PD} max, 20 μA I_{CCQ} max
- 5V tolerant inputs and outputs
- Power down high impedance inputs and outputs
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with the 74 series 16646
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human Body Model < 2000V
  Machine Model < 200V

Logic Symbol

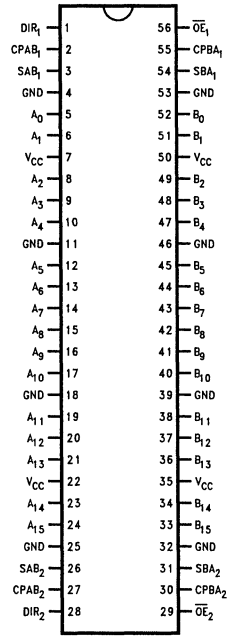


TL/F/12004–1

	SSOP	TSSOP
Order Number	74LCX16646MEA 74LCX16646MEAX	74LCX16646MTD 74LCX16646MTDX
See NS Package Number	MS56A	MTD56

Connection Diagram

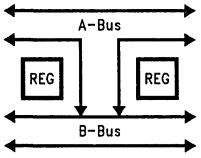
Pin Assignment for SSOP and TSSOP



TL/F/12004–2

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

Real Time Transfer A-Bus to B-Bus



TL/F/12004–3

FIGURE 1

Real Time Transfer B-Bus to A-Bus

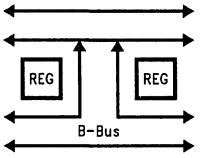


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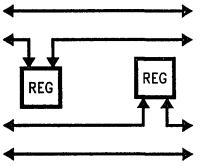
FIGURE 2

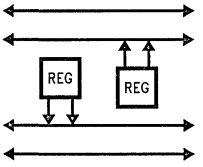
Storage from Bus to Register



TL/F/12004–5

FIGURE 3

Transfer from Register to Bus



TL/F/12004–6

FIGURE 4

Function Table (Note)

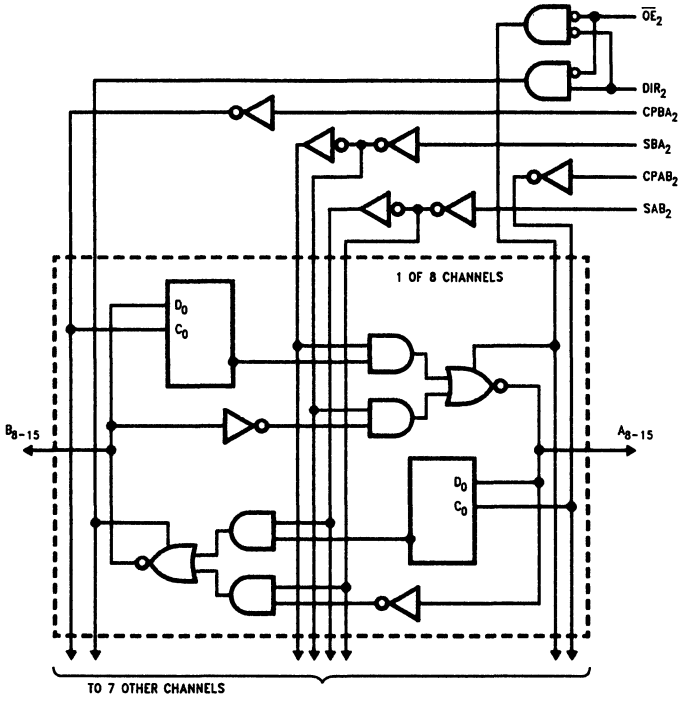
Inputs						Data I/O		Output Operation Mode
$\overline{OE}_1$	DIR_1	$CPAB_1$	$CPBA_1$	SAB_1	SBA_1	A_{0-7}	B_{0-7}	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	↗	X	X	X			Clock An Data into A Register
H	X	X	↗	X	X			Clock Bn Data Into B Register
L	H	X	X	L	X	Input	Output	An to Bn—Real Time (Transparent Mode)
L	H	↗	X	L	X			Clock An Data to A Register
L	H	H or L	X	H	X			A Register to Bn (Stored Mode)
L	H	↗	X	H	X			Clock An Data into A Register and Output to Bn
L	L	X	X	X	L	Output	Input	Bn to An—Real Time (Transparent Mode)
L	L	X	↗	X	L			Clock Bn Data into B Register
L	L	X	H or L	X	H			B Register to An (Stored Mode)
L	L	X	↗	X	H			Clock Bn into B Register and Output to An

Note: The data output functions may be enabled or disabled by various signals at the G and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs. Also applies to data I/O (A and B: 8-15) and #2 control pins.

H = HIGH Voltage Level X = Immaterial

L = LOW Voltage Level ↗ = LOW-to-HIGH Transition.

Logic Diagrams



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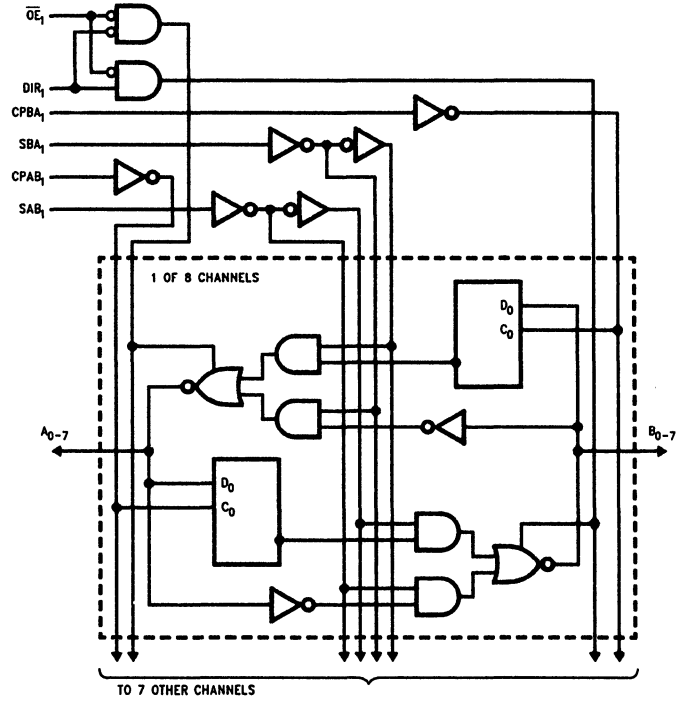


TL/F/12004–8

Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE I/O Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		100	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		20	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±20	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics (Preliminary)

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	170				ns
t_{PHL} t_{PLH}	Propagation Delay Bus to Bus	1.5 1.5	5.0 5.0	1.5 1.5	6.0 6.0	ns
t_{PHL} t_{PLH}	Propagation Delay Clock to Bus	1.5 1.5	6.0 6.0	1.5 1.5	7.0 7.0	ns
t_{PHL} t_{PLH}	Propagation Delay Select to Bus	1.5 1.5	6.0 6.0	1.5 1.5	7.0 7.0	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5 1.5	7.5 7.5	1.5 1.5	8.5 8.5	ns
t_{PLZ} t_{PHZ}	Output Disable Time	1.5 1.5	6.0 6.0	1.5 1.5	7.0 7.0	ns
t_S	Setup Time	2.5		2.5		ns
t_H	Hold Time	1.5		1.5		ns
t_W	Pulse Width	3.0		3.0		ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 1)		1.0 1.0			ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Dynamic Switching Characteristics

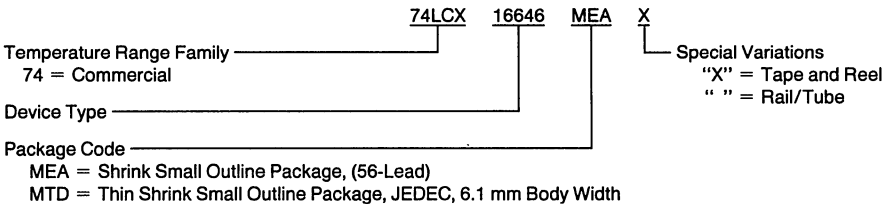
Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	20	pF

74LCX16646 Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



National Semiconductor

PRELIMINARY

74LCX16652
Low-Voltage Transceiver/Register with 5V Tolerant Inputs and Outputs

General Description

The LCX16652 contains sixteen non-inverting bidirectional bus transceivers with TRI-STATE® outputs providing multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to the HIGH logic level. Output Enable pins (OEAB, $\overline{OEBA}$) are provided to control the transceiver function.

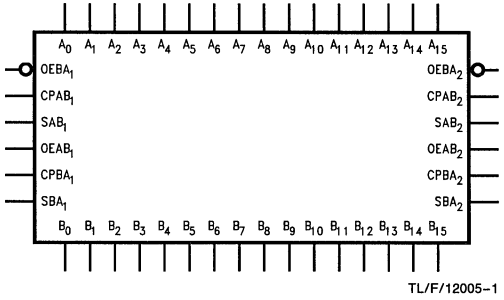
The LCX16652 is designed for low-voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX16652 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5.0 ns t_{PD} max, 20 μA I_{CCQ} max
- 5V tolerant inputs and outputs
- Power down high impedance inputs and outputs
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 16652
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbol

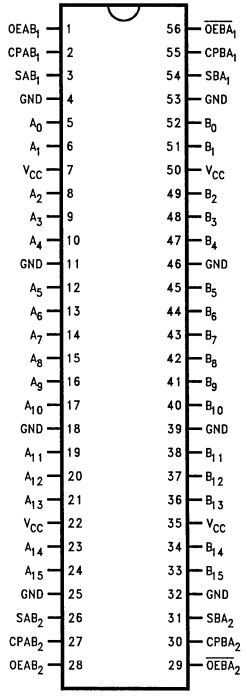


TL/F/12005–1

Pin Names	Description
A_0–A_{15}	Data Register A Inputs/ TRI-STATE Outputs
B_0–B_{15}	Data Register B Inputs/ TRI-STATE Outputs
$CPAB_n$, $CPBA_n$	Clock Pulse Inputs
SAB_n, SBA_n	Select Inputs
$OEAB_n$, $\overline{OEBA}_n$	Output Enable Inputs

Connection Diagram

Pin Assignment for SSOP and TSSOP



TL/F/12005–2

	SSOP	TSSOP
Order Number	74LCX16652MEA 74LCX16652MEAX	74LCX16652MTD 74LCX16652MTDX
See NS Package Number	MS56A	MTD56

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

Functional Description

In the transceiver mode, data present at the HIGH impedance port may be stored in either the A or B register or both.

The select (SAB_n, SBA_n) controls can multiplex stored and real-time.

The examples in *Figure 1* demonstrate the four fundamental bus-management functions that can be performed with the 74LCX16652.

Data on the A or B data bus, or both can be stored in the internal D flip-flop by LOW to HIGH transitions at the appropriate Clock Inputs ($CPAB_n$, $CPBA_n$) regardless of the Select or Output Enable Inputs. When SAB and SBA are in the real time transfer mode, it is also possible to store data without using the internal D flip-flops by simultaneously enabling $OEAB_n$ and $\overline{OEBA}_n$. In this configuration each Output reinforces its Input. Thus when all other data sources to the two sets of bus lines are in a HIGH impedance state, each set of bus lines will remain at its last state.

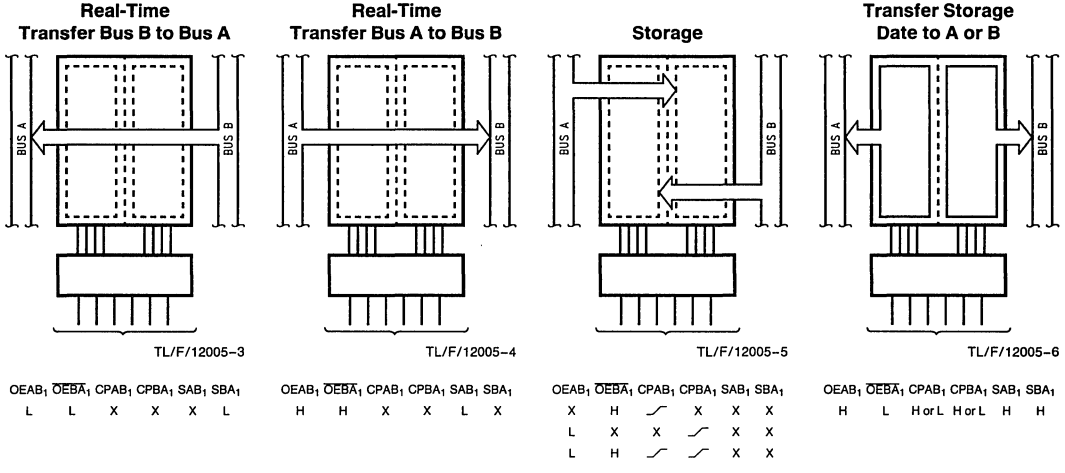


FIGURE 1

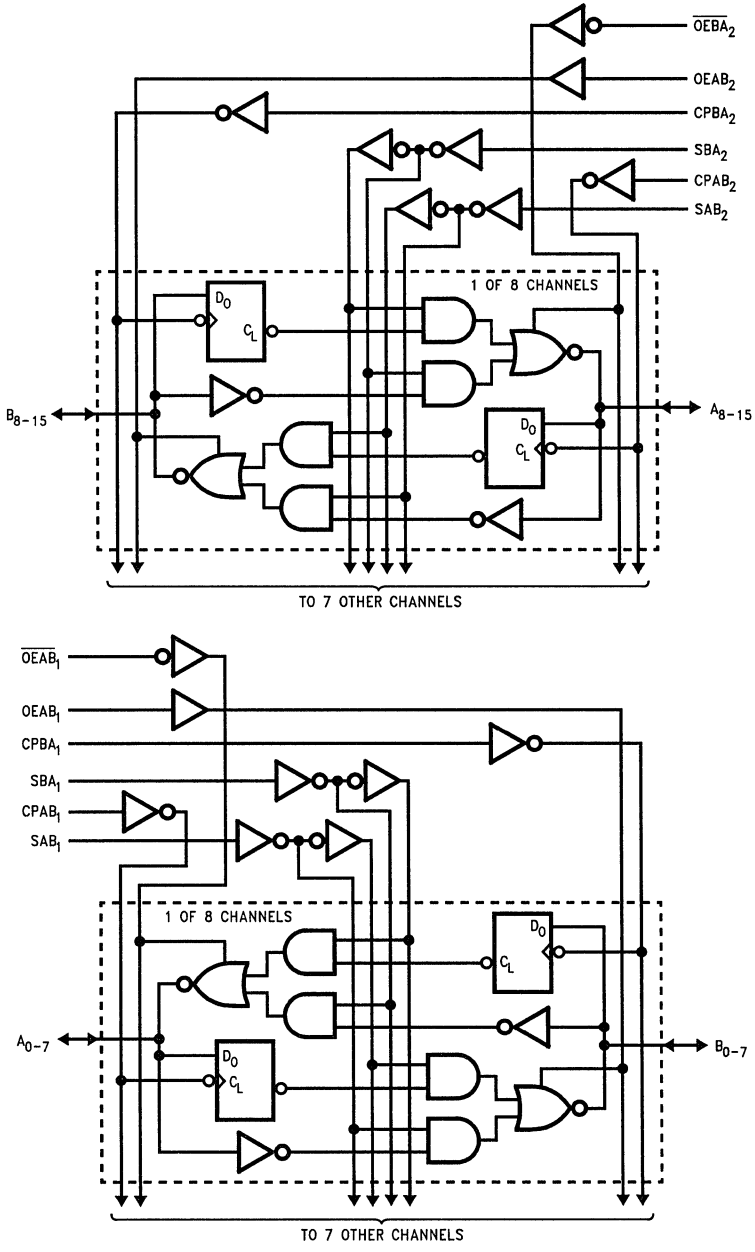
Function Table (Note)

Inputs						Inputs/Outputs		Operating Mode
$OEAB_1$	$\overline{OEBA}_1$	$CPAB_1$	$CPBA_1$	SAB_1	SBA_1	A_0 thru A_7	B_0 thru B_7	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↗	↗	X	X			Store A and B Data
X	H	↗	H or L	X	X	Input	Not Specified	State A, Hold B
H	H	↗	↗	X	X	Input	Output	Store A in Both Registers
L	X	H or L	↗	X	X	Not Specified	Input	Hold A, Store B
L	L	↗	↗	X	X	Output	Input	Store B in Both Registers
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Store B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↗ = LOW to HIGH Clock Transition

Note: The data output functions may be enabled or disabled by various signals at OEAB or OEBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW to HIGH transition on the clock inputs. This also applies to data I/O (A and B: 8–15) and #2 control pins.

Logic Diagram



TL/F/12005–7

Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V–3.6V V_{CC} = 2.7V		±24 ±12	mA
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −18 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 16 mA	3.0		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.7–3.6		±5.0	μA
I_{OZ}	TRI-STATE I/O Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.7–3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		100	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		20	μA
		3.6V ≤ V_I, V_O ≤ 5.5V	2.7–3.6		±20	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency	170				MHz
t_{PHL} t_{PLH}	Propagation Delay Bus to Bus	1.5 1.5	5.0 5.0	1.5 1.5	6.0 6.0	ns
t_{PHL} t_{PLH}	Propagation Delay Clock to Bus	1.5 1.5	6.0 6.0	1.5 1.5	7.0 7.0	ns
t_{PHL} t_{PLH}	Propagation Delay Select to Bus	1.5 1.5	6.0 6.0	1.5 1.5	7.0 7.0	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5 1.5	7.5 7.5	1.5 1.5	8.5 8.5	ns
t_{PLZ} t_{PHZ}	Output Disable Time	1.5 1.5	6.0 6.0	1.5 1.5	7.0 7.0	ns
t_S	Setup Time	2.5		2.5		ns
t_H	Hold Time	1.5		1.5		ns
t_W	Pulse Width	3.0		3.0		ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 1)		1.0 1.0			ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Dynamic Switching Characteristics

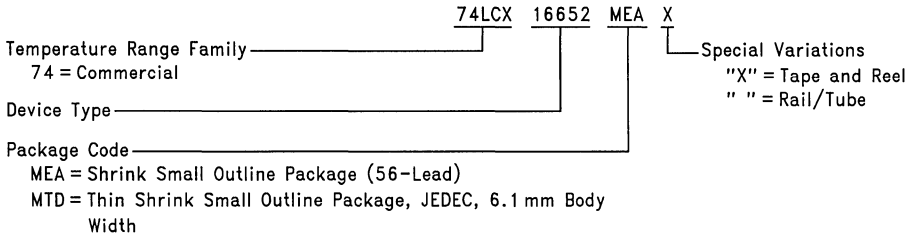
Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	20	pF

74LCX16652 Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

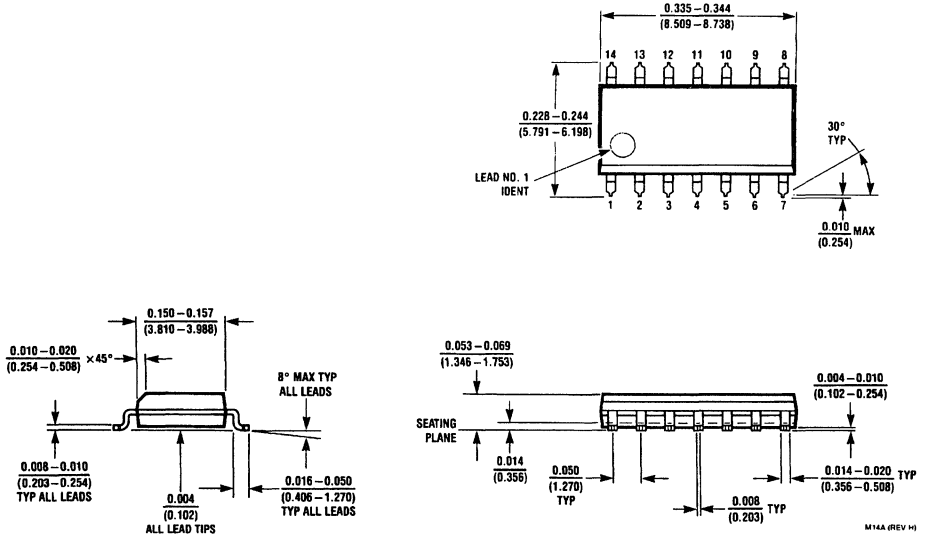


TL/F/12005–8

National Semiconductor

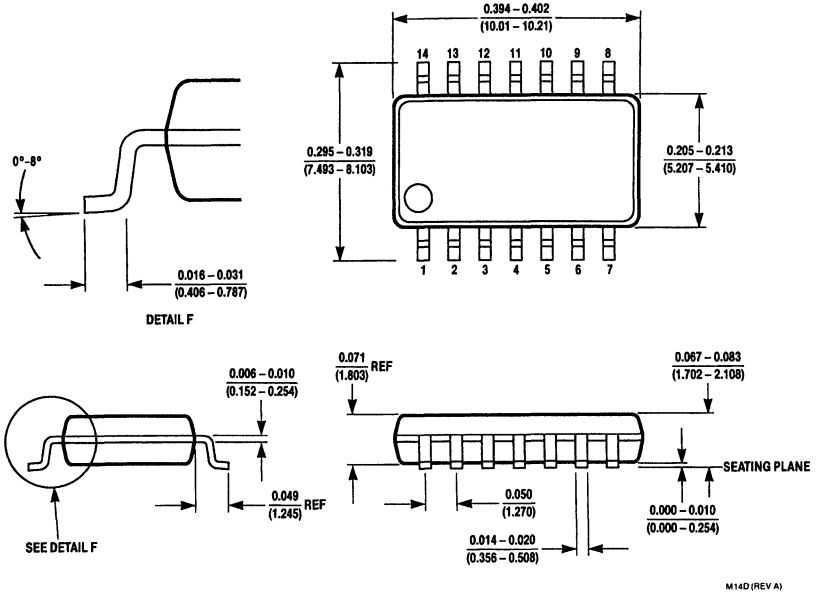
14 Lead (0.150" Wide) Molded Small Outline Package, JEDEC
NS Package Number M14A

All dimensions are in inches (millimeters)



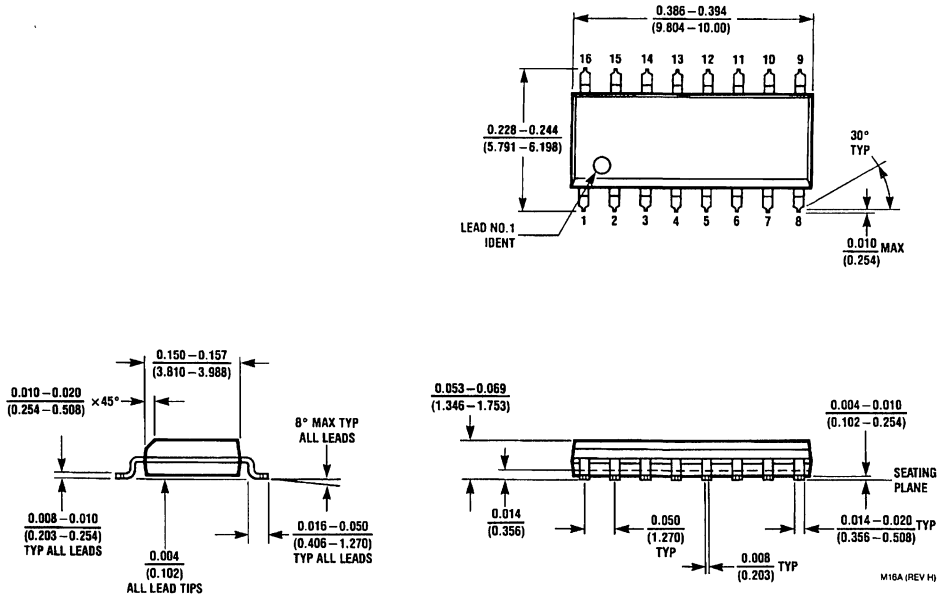
14 Lead (0.300" Wide) Molded Small Outline Package, EIAJ
NS Package Number M14D

All dimensions are in inches (millimeters)



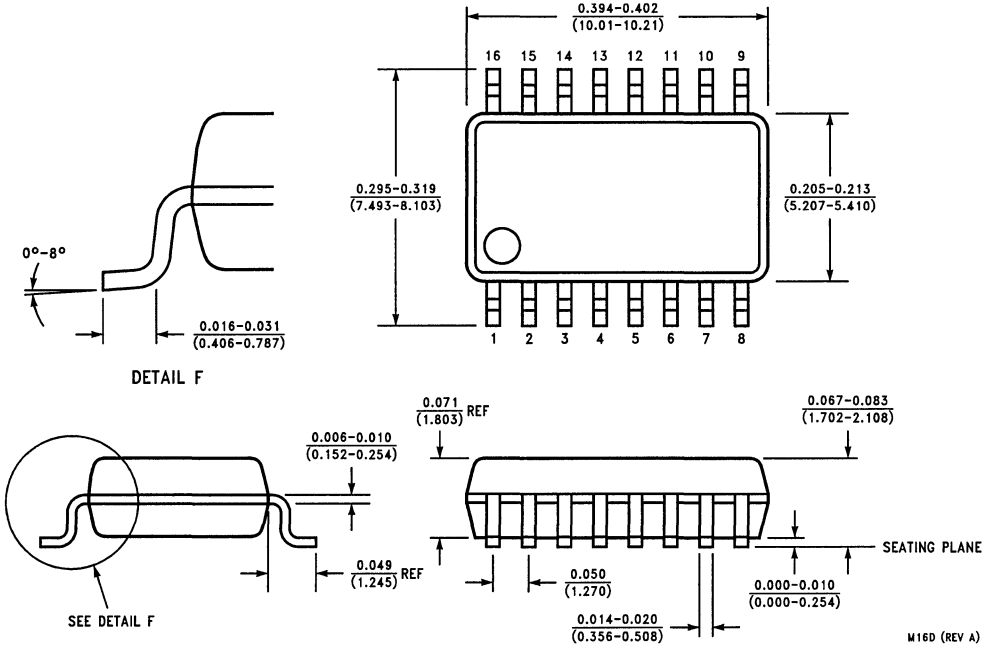
16 Lead (0.150" Wide) Molded Small Outline Package, JEDEC
NS Package Number M16A

All dimensions are in inches (millimeters)



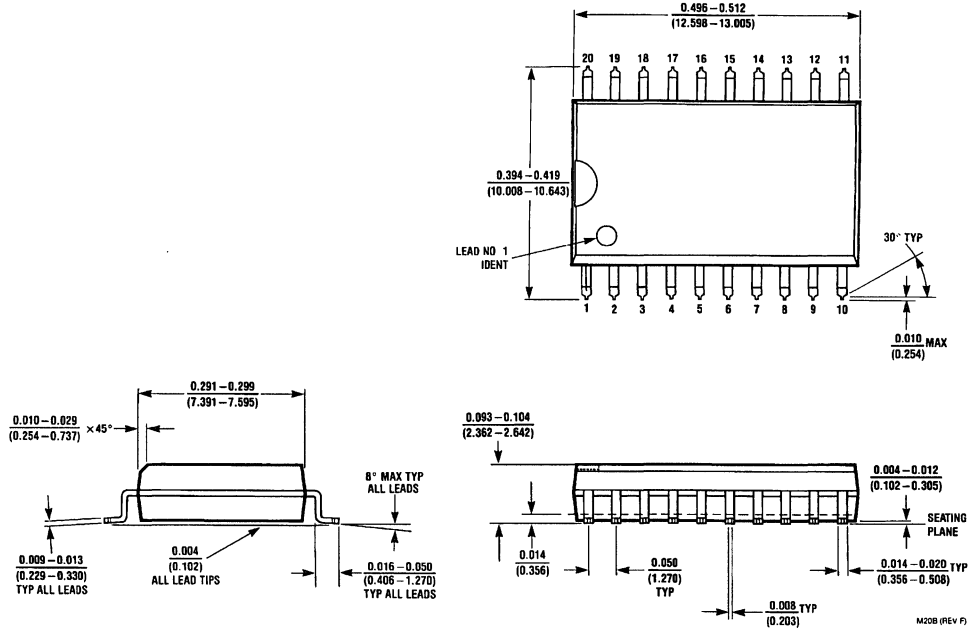
16 Lead (0.300" Wide) Molded Small Outline Package, EIAJ
NS Package Number M16D

All dimensions are in inches (millimeters)



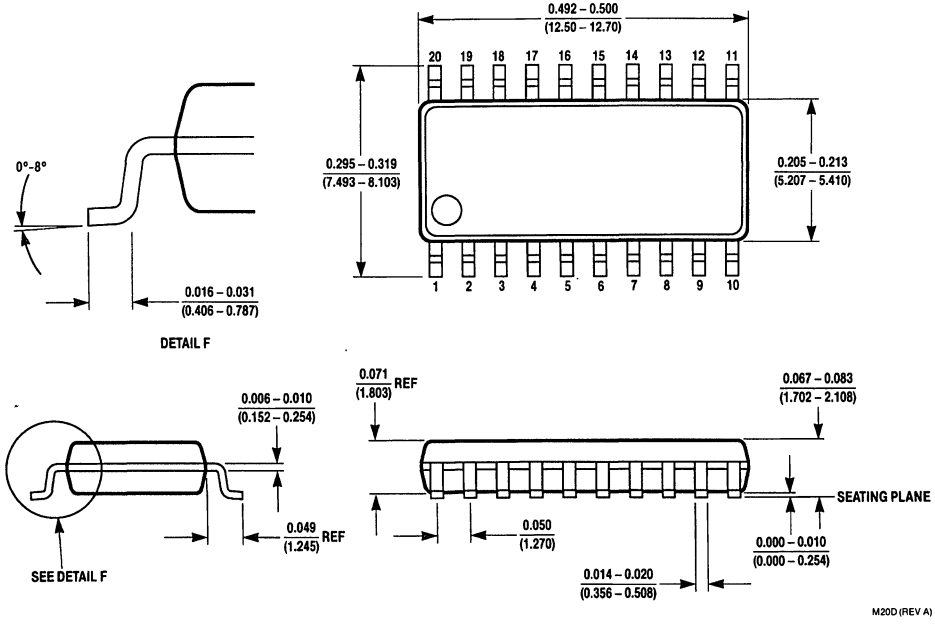
20 Lead (0.300" Wide) Molded Small Outline Package, JEDEC
NS Package Number M20B

All dimensions are in inches (millimeters)



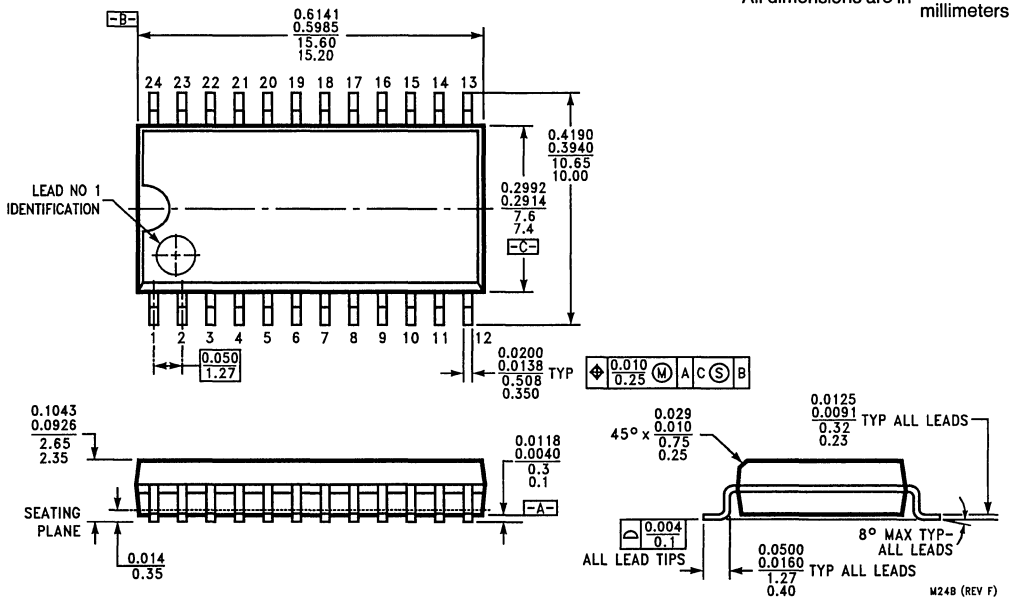
20 Lead (0.300" Wide) Molded Small Outline Package, EIAJ
NS Package Number M20D

All dimensions are in inches (millimeters)



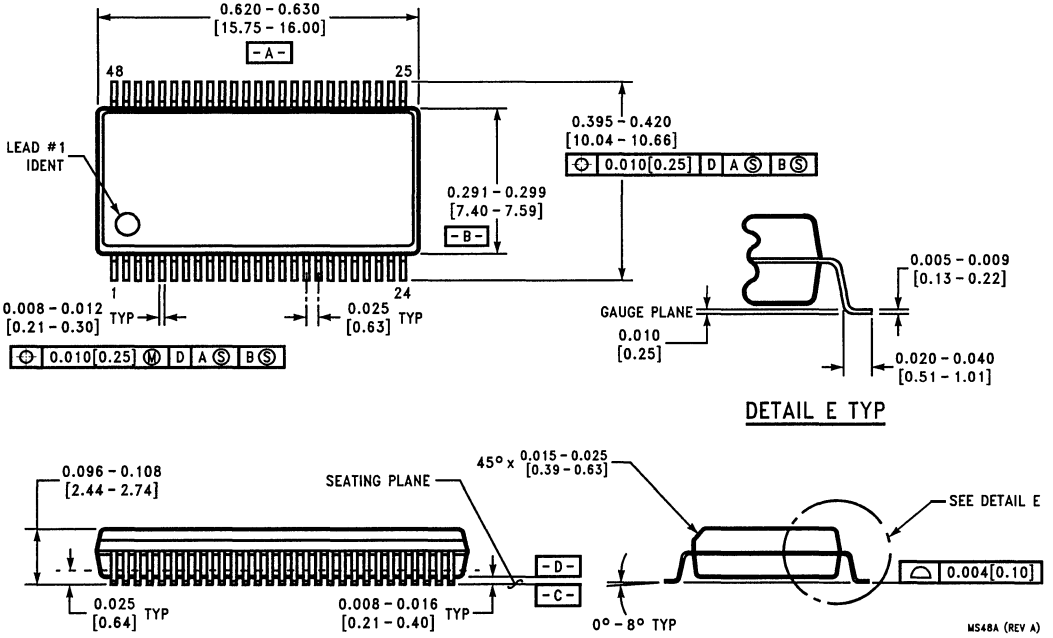
24 Lead (0.300" Wide) Molded Small Outline Package, JEDEC
NS Package Number M24B

All dimensions are in $\frac{\text{inches}}{\text{millimeters}}$



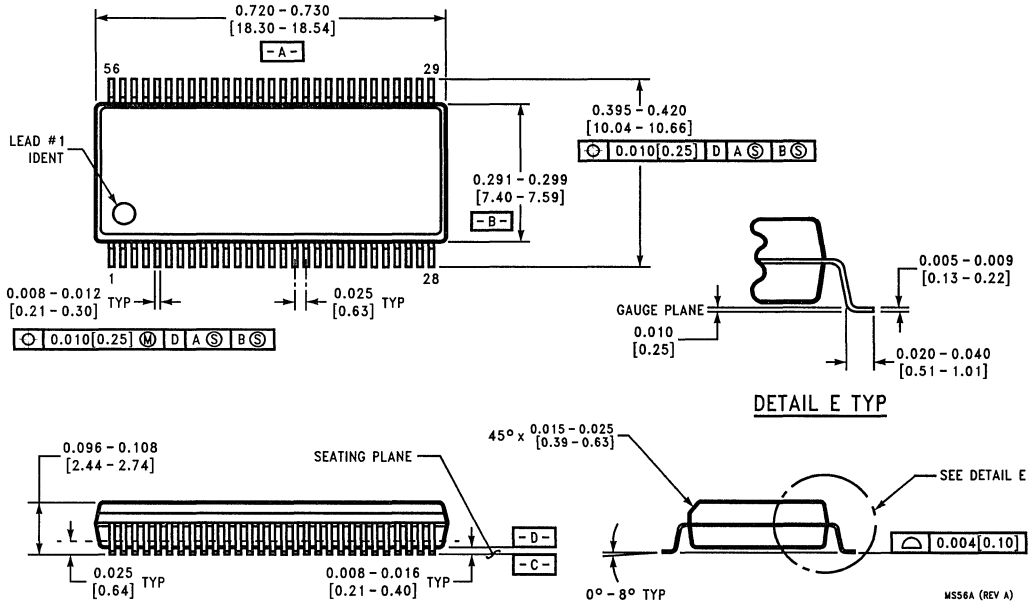
48 Lead (0.300" Wide) Molded Shrink Small Outline Package, JEDEC
NS Package Number MS48A

All dimensions are in inches [millimeters]



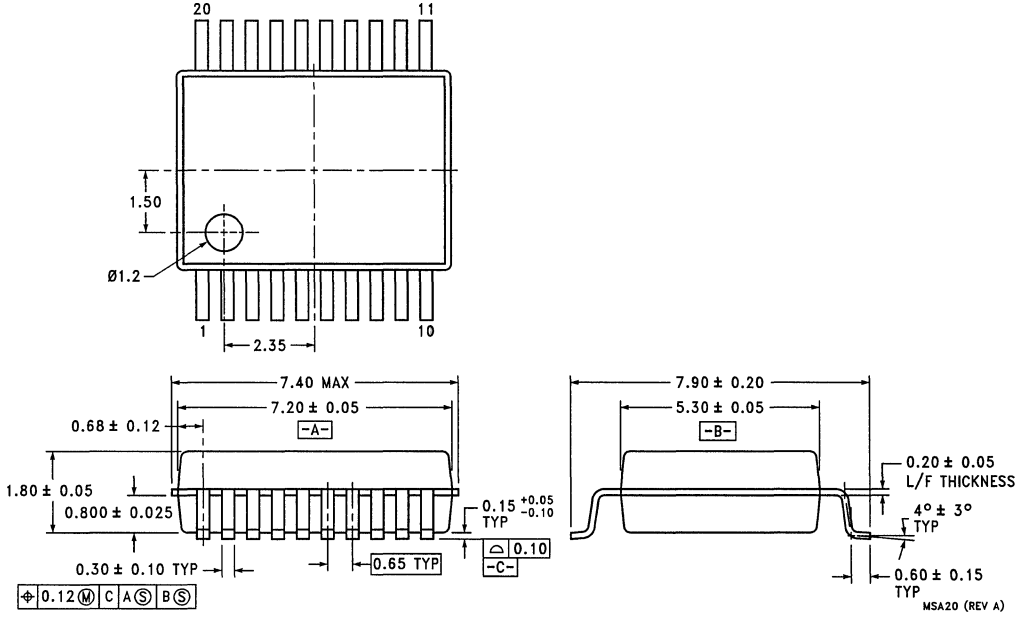
56 Lead (0.300" Wide) Molded Shrink Small Outline Package, JEDEC
NS Package Number MS56A

All dimensions are in inches [millimeters]



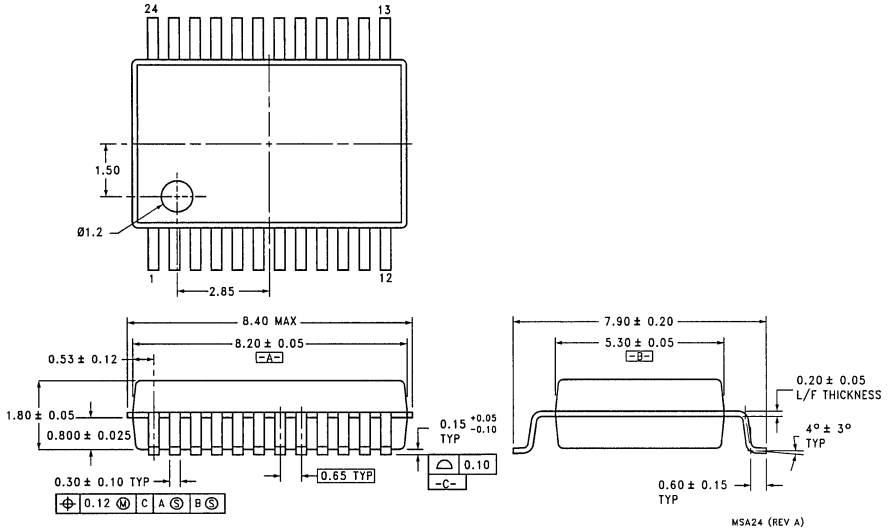
20 Lead Molded Shrink Small Outline Package, EIAJ, Type II
NS Package Number MSA20

All dimensions are in millimeters



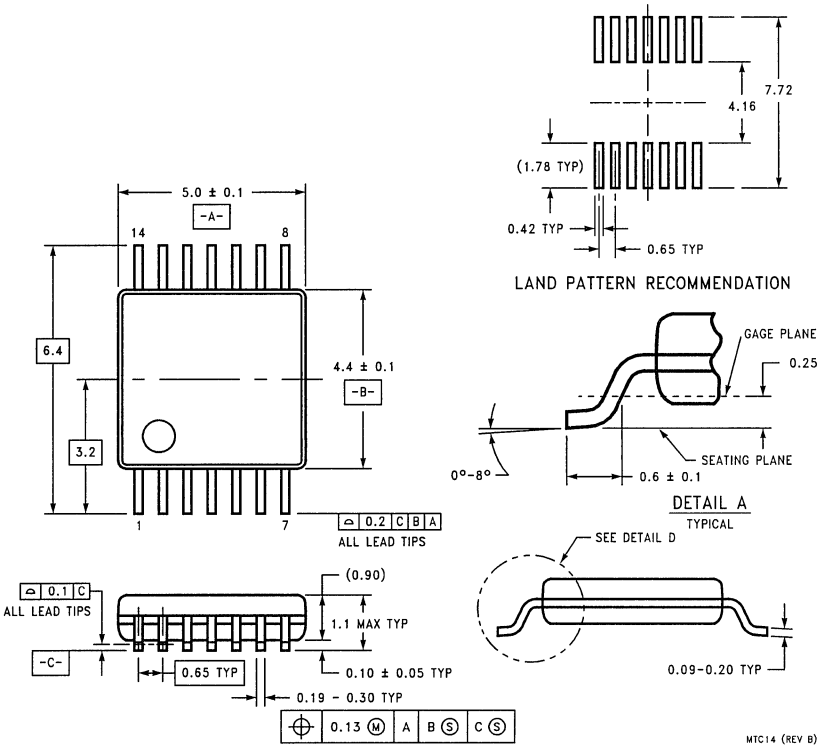
24 Lead Molded Shrink Small Outline Package, EIAJ, Type II
NS Package Number MSA24

All dimensions are in millimeters



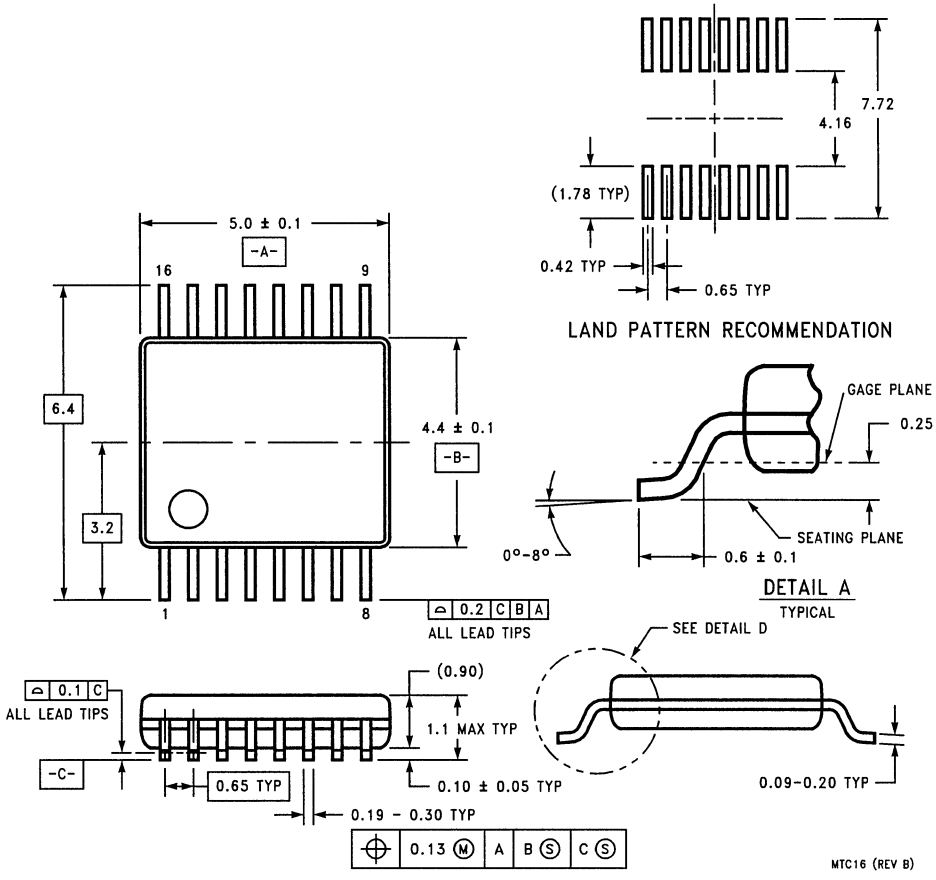
14 Lead Molded Thin Shrink Small Outline Package, JEDEC
NS Package Number MTC14

All dimensions are in millimeters



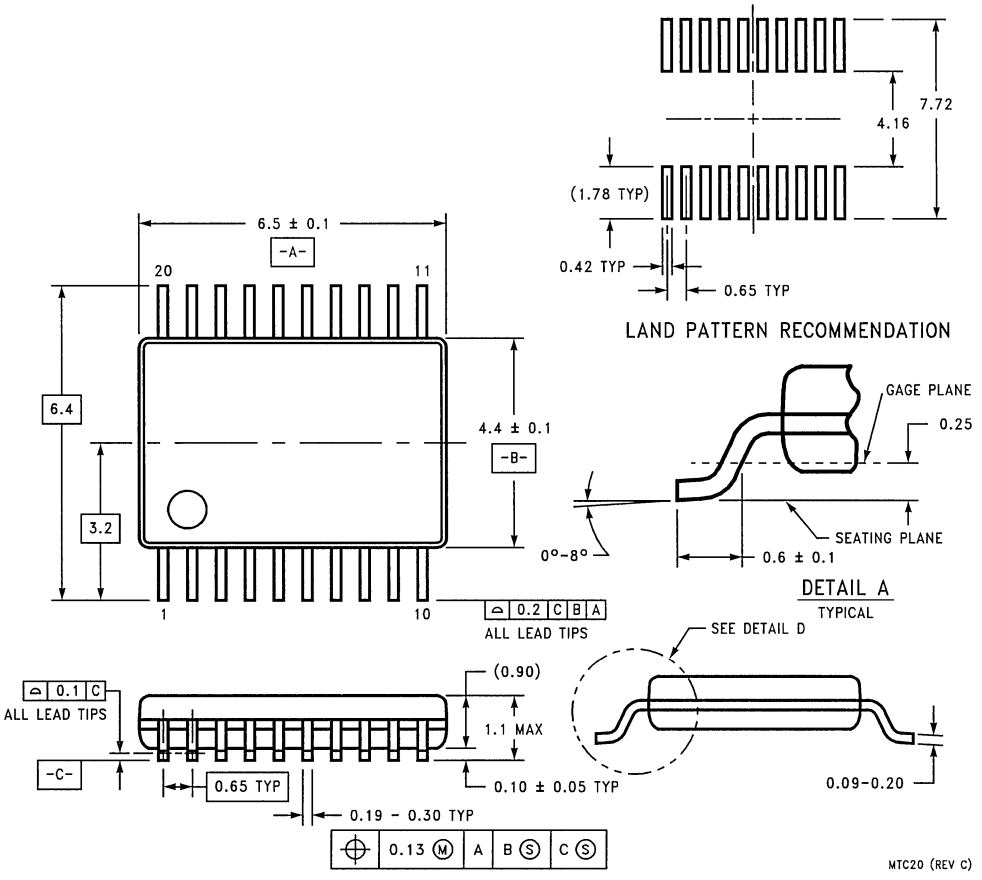
16 Lead Molded Thin Shrink Small Outline Package, JEDEC
NS Package Number MTC16

All dimensions are in millimeters



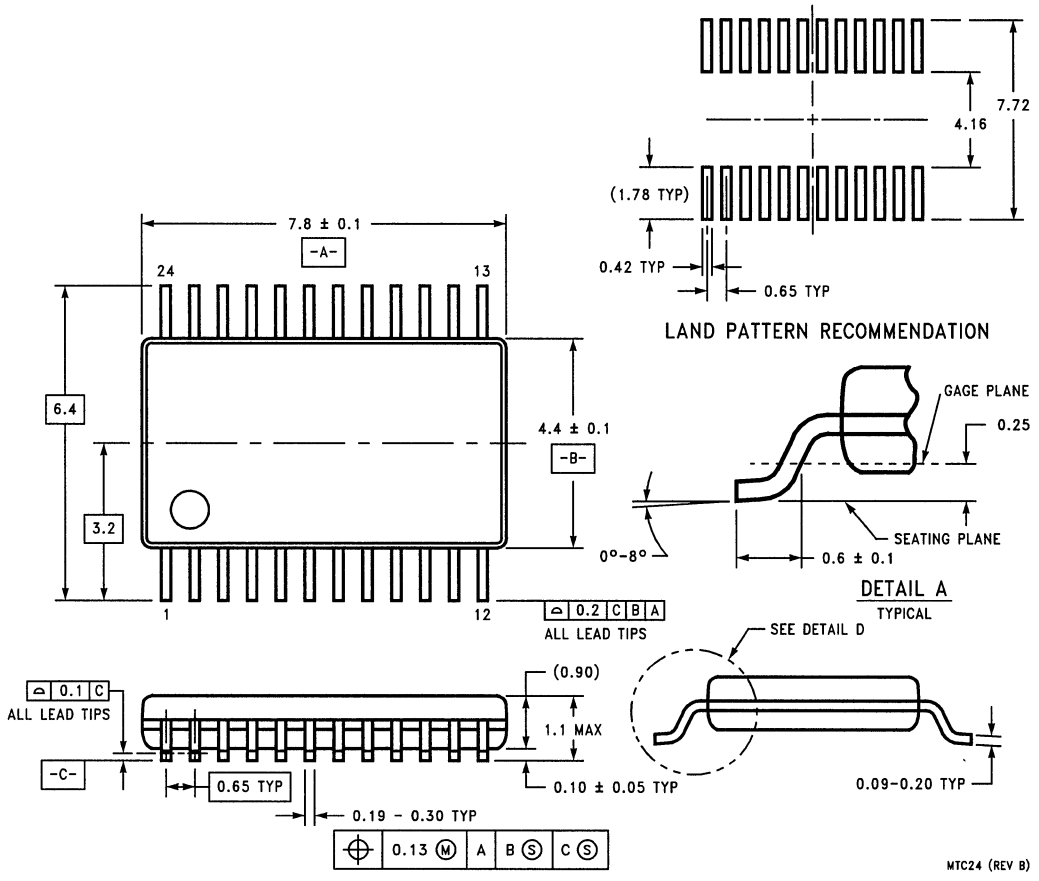
20 Lead Molded Thin Shrink Small Outline Package, JEDEC
NS Package Number MTC20

All dimensions are in millimeters



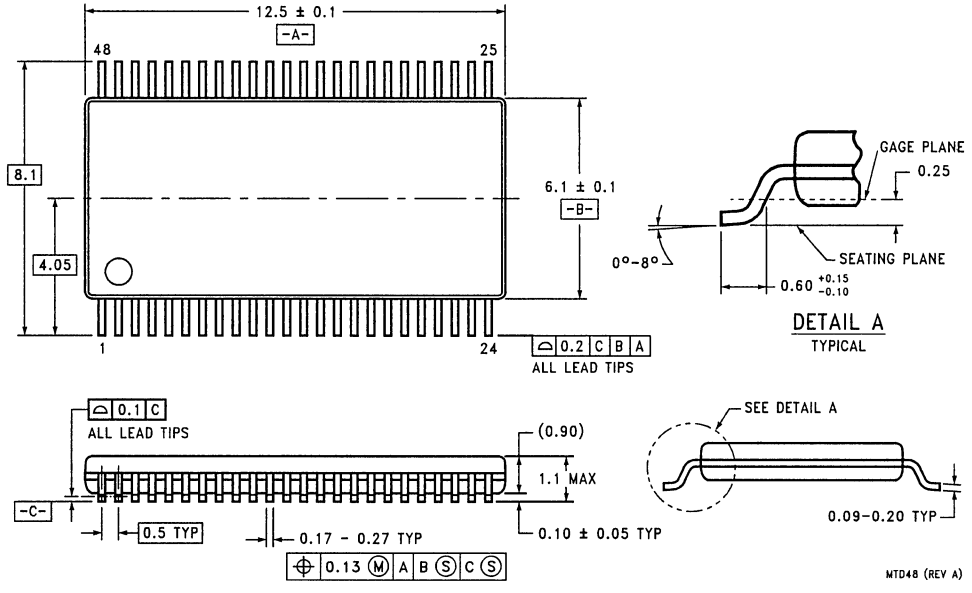
24 Lead Molded Thin Shrink Small Outline Package, JEDEC
NS Package Number MTC24

All dimensions are in millimeters



48 Lead Molded Thin Shrink Small Outline Package, JEDEC
NS Package Number MTD48

All dimensions are in millimeters



56 Lead Molded Thin Shrink Small Outline Package, JEDEC
NS Package Number MTD56

All dimensions are in millimeters