National Semiconductor

570180-002

1992 Guide to Video Products

National Semiconductor, an industry leader in the manufacture of high quality, high reliability integrated circuits, is proud to provide the enclosed information on semiconductor products for video applications. Our presence in the video field continues to produce the best ICs available. This booklet introduces some new products to the market, most notably the *LM1202* 230 MHz video preamp system.

Aside from the video products for CRT display systems, we have included some general purpose video products and are also introducing the *LM6181* 100MHz, 100mA current-feedback op amp -- best-in-class for current-mode amplifiers.

National Semiconductor stands ready to help you with our highly trained sales, applications, and marketing staff. Local sales offices are located on the back cover of this guide.

National Semiconductor

Guide to Video Products

September 1991

LH2422/LH2424
CRT Video Amplifiers

General Description

The LH2422 and LH2424 are wide bandwidth and high voltage CRT video amplifiers. These amplifiers are specifically designed to directly drive the cathode of high resolution CRT monitors. Both amplifiers work on the transimpedance principle, about ±6.5 mA input current results in an output swing of ±20V relative to the quiescent output DC level. These amplifiers can easily energize 10 ns pixels and are well suited for monitors with 1280 x 1024 or higher display resolutions. The LH2422 and LH2424 are identical except that the LH2424 has faster rise and fall times and wider bandwidth than LH2422. Both amplifiers can interface to National's LM1201 and LM1203 preamplifiers.

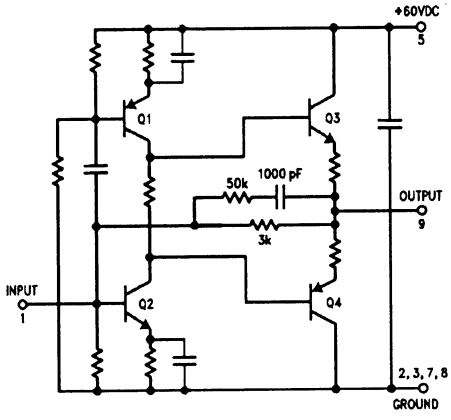
Features

- LH2424: BW = 175 MHz
  Rise/Fall Time = 2 ns
- LH2422: BW = 120 MHz
  Rise/Fall Time = 3 ns
- Drives 8.5 pF capacitive load
- Pin compatible with CR2424
- DC coupled for output level adjust
- Output signal can swing 50V

Applications

- CRT driver for color and monochrome monitors
- High voltage transimpedance amplifier

Schematic and Connection Diagrams



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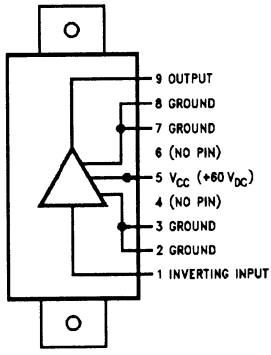

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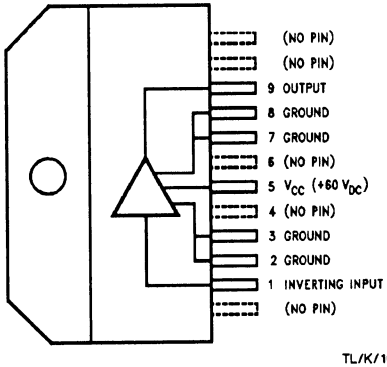
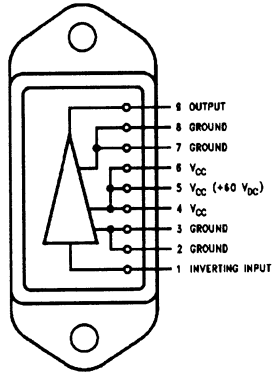
Order Number LH2422AJ or LH2424AJ
See NS Package Number HY07A



TL/K/10128–12

Order Number LH2422S or LH2424S
See NS Package Number HY07B



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Order Number LH2422D-MIL
See NS Package Number HY09B

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC} +70V

Storage Temperature Range, TSTG −40°C to +125°C

Operating Temperature Range, T_{case} −20°C to +90°C

Lead Temperature (Soldering, <10 sec) 300°C

ESD Tolerance >4KV

DC Electrical Characteristics

Unless otherwise noted, the following specifications apply for V_{CC} = +60V, R1 = 215Ω, C1 = 60 pF (for LH2422), C1 = 90 pF (for LH2424), C_{LOAD} = 8.5 pF, 40 V_{P-P} swing with 30 VDC offset, and T_{CASE} = 25°C. See test circuit, *Figure 1.*

Symbol	Parameter	Conditions	Min (Note 3)	Typ (Note 2)	Max (Note 3)	Units
I_{CC}	Supply Current	Input/Output Open Circuit	35	43.5	47.5	mA
V_{INDC}	Input Offset Voltage (LH2422)	Input/Output Open Circuit	1.15	1.55	1.7	V
	Input Offset Voltage (LH2424)	Input/Output Open Circuit	1.15	1.55	1.65	V
V_{OUTDC}	Output Offset Voltage	Input/Output Open Circuit	26	30	34	V
P_D	Power Dissipation (LH2422) Power Dissipation (LH2424)	50 MHz Square Wave 50 MHz Square Wave		4.5 4	6 6	W W
LE	Linearity Error	V_{OUT} from +5V to +55V		1	5	%

AC Electrical Characteristics

Unless otherwise noted, the following specifications apply for V_{CC} = +60V, R1 = 215Ω, C1 = 60 pF (for LH2422), C1 = 90 pF (for LH2424), C_{LOAD} = 8.5 pF, 40 V_{P-P} swing with 30 VDC offset, and T_{CASE} = 25°C. See test circuit, *Figure 1.* (Note 1)

Symbol	Parameter	Conditions	LH2422			LH2424			Units
			Min (Note 3)	Typ (Note 2)	Max (Note 3)	Min (Note 3)	Typ (Note 2)	Max (Note 3)	
t_R	Rise Time	10% to 90% (Note 4)		3	4		2	2.9	ns
t_F	Fall Time	90% to 10% (Note 4)		3	4		2	2.9	ns
V_{TILT}	Low Frequency Tilt Voltage	1 kHz Square Wave		1.3			1.3		V
$f_{-3\,dB}$	−3 dB Bandwidth	(Note 5)		120			175		MHz
A_V	Voltage Gain	50Ω Source Impedance (Note 6)	11.5	13	14.5	11.5	13	14.5	V/V
OS	Overshoot			10			10		%

LH2422D-MIL (Note 7)

DC Electrical Characteristics Unless otherwise noted, the following specifications apply for V_{CC} = +60V, R1 = 215Ω, C1 = 60 pF, C_{LOAD} = 8.5 pF, 40 V_{P-P} swing with 30 V_{DC} offset. See test circuit, *Figure 1.*

Symbol	Parameter	Conditions	T_A = 0°C		T_A = +25°C		T_A = +70°C		Units
			Min (Note 3)	Max (Note 3)	Min (Note 3)	Max (Note 3)	Min (Note 3)	Max (Note 3)	
I_{CC}	Supply Current	Input/Output Open Circuit	32	47.5	35	47.5	32	47.5	mA
V_{INDC}	Input Offset Voltage	Input/Output Open Circuit	1.15	1.8	1.15	1.7	1.15	1.8	V
V_{OUTDC}	Output Offset Voltage	Input/Output Open Circuit	26	34	26	34	26	34	V
P_D	Power Dissipation	50 MHz Square Wave		6		6		6	W
LE	Linearity Error	V_{OUT} from +5V to +55V		8		5		8	%

LH2422D-MIL (Note 7)

AC Electrical Characteristics Unless otherwise noted, the following specifications apply for V_{CC} = +60V, R1 = 215Ω, C1 = 60 pF, C_{LOAD} = 8.5 pF, 40 V_{P-P} swing with 30 V_{DC} offset. See test circuit, *Figure 1.*

Symbol	Parameter	Conditions	T_A = +25°C		Units
			Min (Note 8)	Max (Note 8)	
t_R	Rise Time	10% to 90% (Note 4)		4	ns
t_F	Fall Time	90% to 10% (Note 4)		4	ns
A_V	Voltage Gain	50Ω Source Impedance (Note 6)	11.5	14.5	V/V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: Typical specifications are at +25°C and represent the most likely parametric norm.

Note 3: Min/Max limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 4: Input signal t_r, t_f < 1 ns.

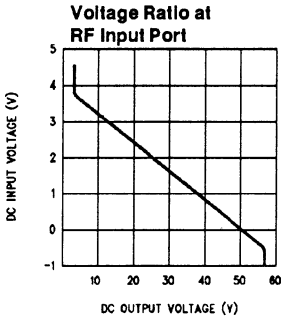
Note 5: −3 dB bandwidth is calculated from the equation; $f_{-3\,dB} = 0.35/t_R$.

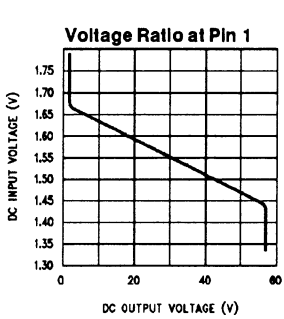
Note 6: Voltage gain is the ratio of the output voltage to the voltage at the RF input port (*Figure 1*).

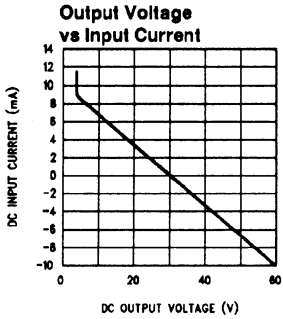
Note 7: A military RETS specification is available on request. At the time of printing, LH2422D-Mil RETS specification complied with the limits in this Electrical Characteristics table.

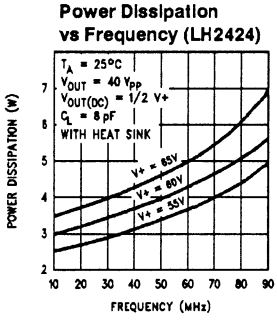
Note 8: Min and Max limits are 100% tested.

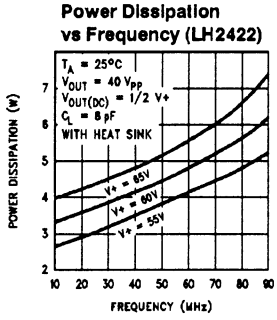
Typical Performance Characteristics











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Application Hints

OUTPUT INFORMATION

The LH2422 and LH2424 are wide bandwidth high voltage amplifiers that can directly drive the cathode of high resolution Cathode Ray Tubes (CRTs). The outputs of both amplifiers are biased at half the supply voltage. With a +60V supply, an output swing of ±20V relative to a 30V output DC bias can easily be achieved. When driving an 8.5 pF capacitance the typical rise and fall times of 2 ns and 3 ns were measured for the LH2424 and LH2422 respectively. During normal CRT operation, tube arcing may occasionally occur. Spark gap protectors are widely used to limit the voltage at the output of the amplifier. In addition a 50Ω to 100Ω resistor is also used in series with the output of the amplifier so as to limit the arc current. This current limiting resistor and the capacitive load offered by the CRT's cathode will degrade the effective rise and fall times at the cathode. Adding a small inductor in series with the amplifier's output will increase the rise and fall times at the cathode due to high frequency peaking of the amplifier's pulse response. This inductor is often referred to as a peaking inductor or peaking coil. At best, the value of the inductor is emperically determined. For the LH2422 and LH2424, a 100 nH to 200 nH inductor is quite adequate.

SHORT CIRCUIT PROTECTION

The LH2424 and LH2422 do not include short circuit protection. If the amplifiers are used to drive a resistive load connected to either ground or V_{CC} then the load must be greater than 600Ω.

INPUT INFORMATION

The "Output Voltage vs Input Current" graph shows that a ±20V swing (from a 30V output DC bias) can be achieved with an input current swing of only ±6.5 mA. For the circuit shown in *Figure 1*, the "Voltage Ratio at RF Input Port" graph relates the input voltage as measured at the RF input port to the voltage at the output; note that the amplifier is phase inverting. With 215Ω for R1 in *Figure 1*, the voltage gain is approximately 13.5, and the low frequency input impedance at the RF input port is approximately 230Ω. The "Voltage Ratio at Pin 1" graph relates the voltage at the input of the amplifier (pin 1) to the output voltage, the output voltage to input voltage ratio is approximately 240V and the low frequency input impedance is approximately 13Ω. With the RF input port open circuited and V_{CC} = 60V, the input of the amplifer (pin 1) is self biased at typically 1.55V while the output is biased at 30V.

SETTING UP GAIN

The LH2424 and LH2422 work on the transimpedance principle. An internal 3 kΩ feedback resistor connected between the input and output converts the input current to output voltage.

For the circuit in *Figure 1*, ±1.43V (referenced to 1.55 V_{DC}) across the 214Ω input resistor results in ±6.65 mA. This current flowing through the 3 kΩ internal feedback resistor results in a ±20V swing at the output.

Application Hints (Continued)

TYPICAL TEST CIRCUIT

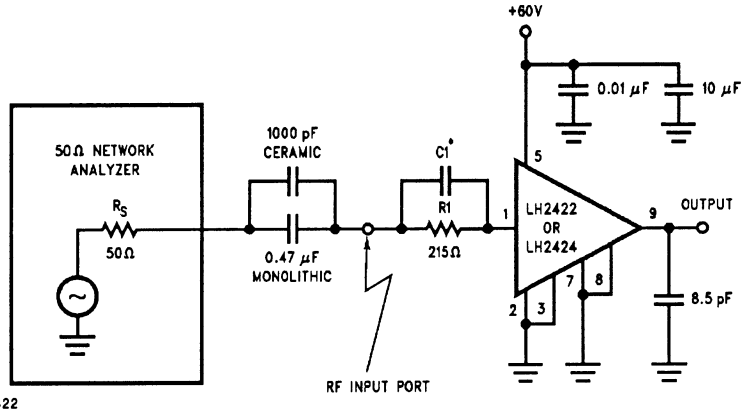
The test circuit in *Figure 1* is driven from either a fast pulse generator with a 50Ω output impedance or network analyzer. The cable between the generator and DUT should be of minimum length. The generator's DC level should be about 1.55V. Use a FET probe with 100X attenuation when using an oscilloscope. Total load capacitance (including probe capacitance) should be limited to 8.5 pF.

The input circuit RC network is tuned to produce peaking when driven from a 50Ω source.

Thermal Considerations

The LH2422 and LH2424 require that the package be heatsunk for proper operation under any condition. Maximum ratings require that the device case temperature be limited to 90°C maximum. Thus at 50°C maximum ambient temperature and 6W maximum power dissipation, the thermal resistance of the heat sink should be less than (90−50)°C/6W = 6.7°C/W. Several approaches to heat sinking may be taken. The simplest is a sheet of aluminum with a volume of 4 cubic inches or an area of 32 sq. inches and a thickness of 0.125 inches.

Commercially available heatsinks such as Thermalloy 15509 extrusion would result in size reduction. *Figures 2* and *3* show the two approaches for proper heat sinking. Note that an aluminum spacer must be placed between the package and the heatsink block so as to prevent the device output from being shorted to ground. In the absence of a series current limiting resistor at the output, the device will be destroyed if the output is inadvertently shorted to ground or V_+.



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*C1 = 60 pF for LH2422
C1 = 90 pF for LH2424

FIGURE 1. Typical AC Test Circuit

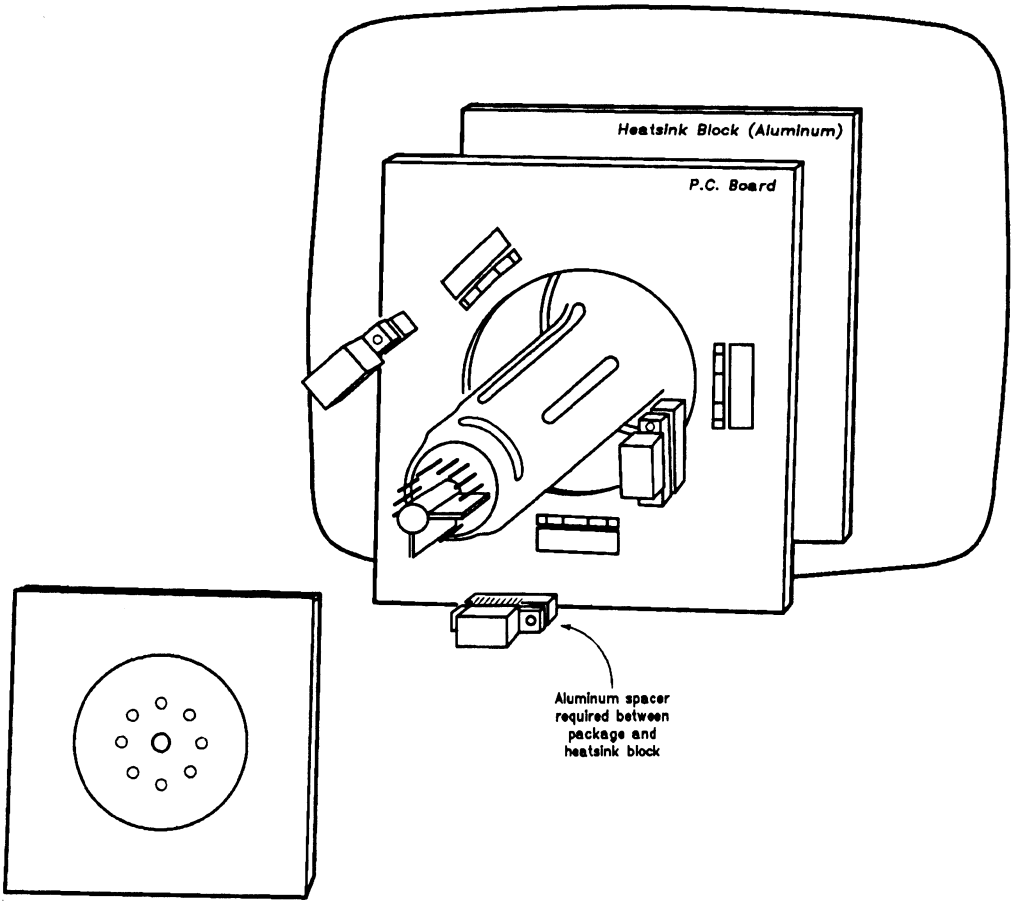

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FIGURE 2. Heat Sinking with an Aluminum Block

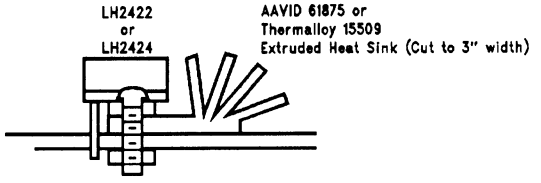

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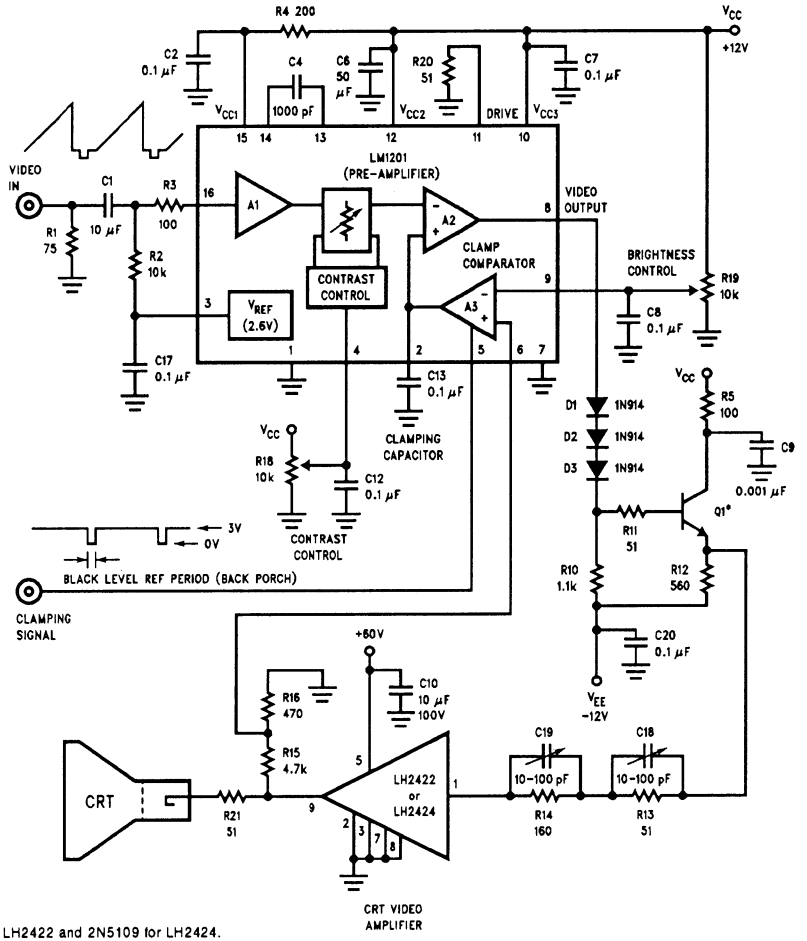
FIGURE 3. Heat Sinking with the Thermalloy 15509 Extrusion

Application Circuits



*Q1 is 2N5770 for LH2422 and 2N5109 for LH2424.

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FIGURE 4. Circuit shows how the LM1201 pre-amplifier and LH2422/LH2424 CRT Video Amplifier may be used to build a 100 MHz Monochrome Monitor

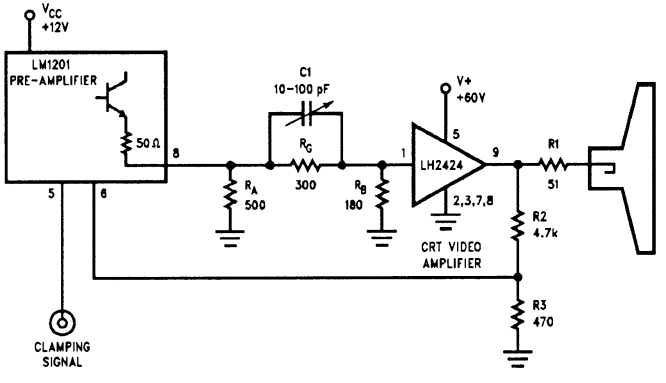

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FIGURE 5. Circuit shows a simple RC interface network which eliminates the need for a level shift stage and additional V_{EE} supply of *Figure 4.*

Evaluation Board

The evaluation board is intended to demonstrate the capabilities of the LH2422 CRT Video Amplifier. The board may be used to interface the amplifier to a CRT display or to evaluate the frequency response or pulse response in a 50Ω system.

Figure 6 shows the schematic of the LH2422 evaluation board. R1 sets the overall gain of the fixture. The test circuit used 220Ω to provide a gain of 13.5. C1 is a 10 pF–100 pF variable capacitor. Adjust this capacitor to optimize pulse response.

A large bypass capacitor, C2, is needed to reduce lower frequency ringing caused by the power supply wires.

The input is designed to be fed from a 50Ω generator, however, the input impedance at V_{IN} is not well matched to 50Ω and if a long cable is used between the generator and the input, reflections will occur giving unpredictable responses. Two things can be done to get around this problem:

1. Use a very short connector (less than 2 inches) between the generator and the input.
2. Use a 6 dB pad between the cable and the input. This will reduce reflections and provide a 50Ω source to the circuit board.

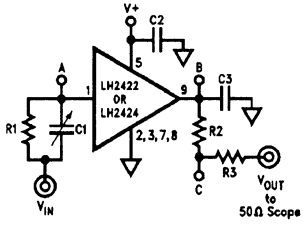

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FIGURE 6. Schematic of LH2422 Evaluation Circuit

The output of the amplifier can drive the CRT cathode directly from point B, while R2 and R3 are used as a 100 to 1 (40 dB) attenuator to a 50Ω scope or network analyzer input. Two resistors are used in series to reduce capacitance and attempt to compensate the frequency response. The layout of the board *(Figure 7)* includes a trace at point C to connect R2 and R3; unfortunately, the capacitance to ground at this point is about 0.6 pF, enough to cause a 20% bandwidth reduction in the response of the attenuator resistors. The resistors should be wired "floating" above the board.

Capacitor C3 is used to simulate the input capacitance at the CRT cathode. The board exhibits about 4.5 pF at the output node of the LH2422. A capacitor of 4 pF will increase it to the specified value of 8.5 pF.

PARTS LIST

RESISTORS:

R1 220Ω, ¼W, 5%
R2 2.2 kΩ, ¼W, 5%
R3 2.7 kΩ, ¼W, 5%

CAPACITORS:

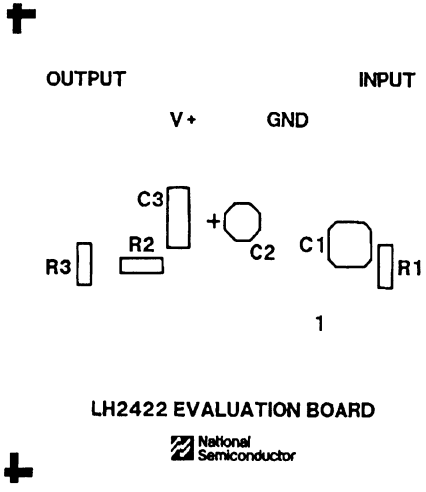
C1 10 pF – 120 pF (muRata ERIE P/N TZ03R121E)
C2 10 µF, 100V, 10%
C3 4 pF, 50V, 10%

HARDWARE:

BNC CONNECTORS (KINGS P/N KC-79-237-MO6)
BANANA JACKS (JOHNSON P/N 108-09XX-001)
HOLTITE SOCKET (AUGAT P/N 8134-HC-5P2)

Evaluation Board (Continued)

(a) Component Placement Guide



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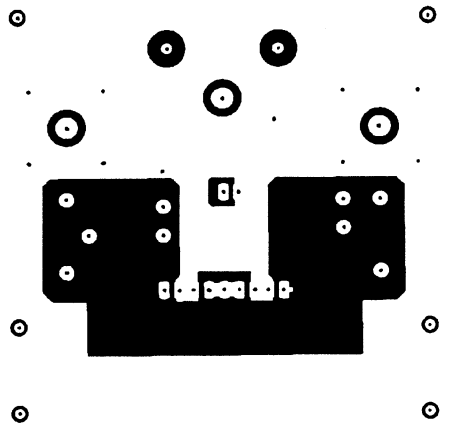
(b) Component (Top) Side



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(c) Solder (Bottom) Side

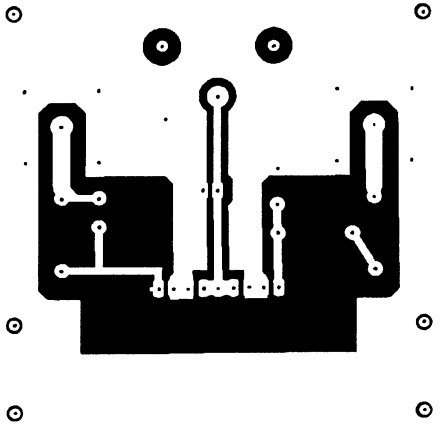

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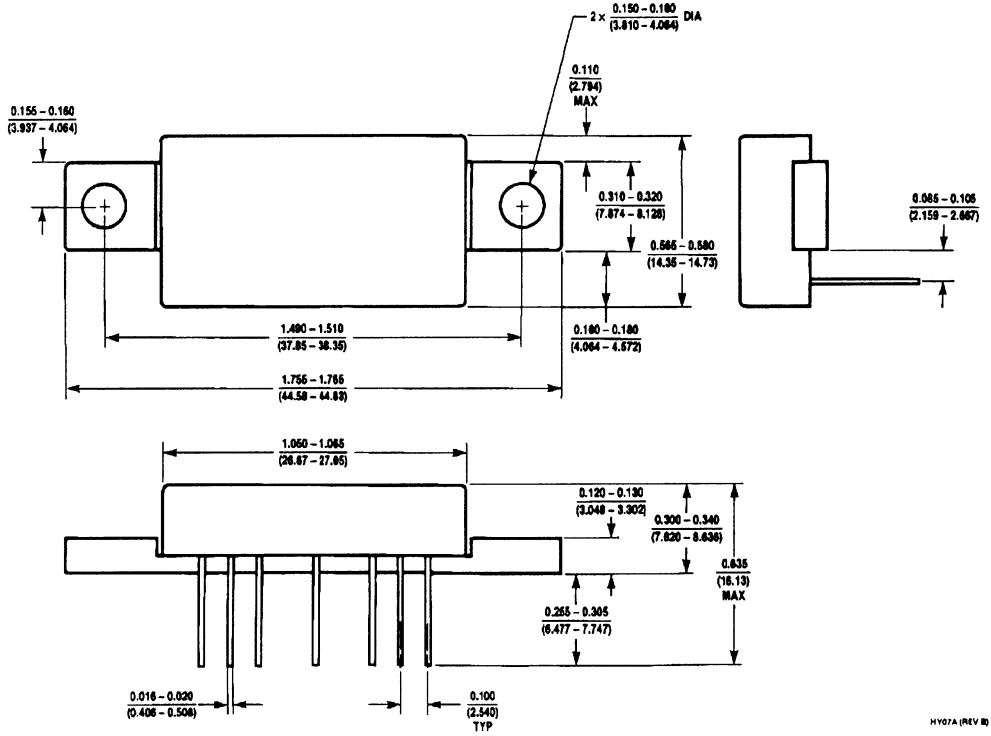
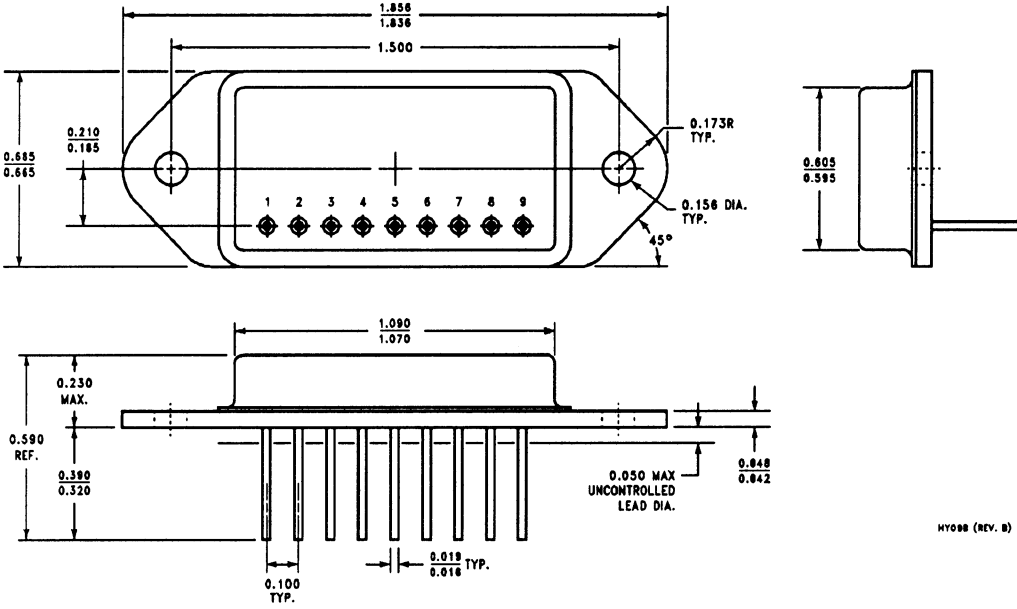
FIGURE 7. PC Board Layout and Component Placement Guide

Physical Dimensions inches (millimeters)



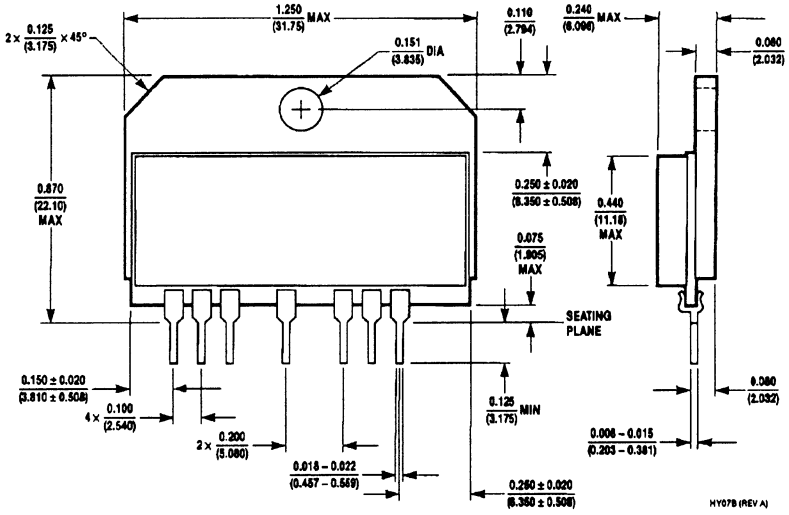
7-Lead SIP Hybrid Package (J)
Order Number LH2422AJ or LH2424AJ
NS Package Number HY07A

Physical Dimensions inches (millimeters) (Continued)



9-Lead Hybrid Metal Can (D)
Order Number LH2422D-MIL
NS Package Number HY09B

Physical Dimensions inches (millimeters) (Continued)



9-Lead Single-In-Line Package (S)
Order Number LH2422S or LH2424S
NS Package Number HY07B

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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National Semiconductor

Competition Philips
50 V_{pp} ~125MHz

August 1990

LH2426
Triple 80 MHz CRT Driver

General Description

The LH2426 contains three wide bandwidth, large signal amplifiers designed for large voltage swings at high frequencies. The amplifiers work on a transimpedance principal i.e., an input current swing of ±4.38 mA results in an output voltage swing of ±25V. The device is intended for use in color CRT monitors and is a low cost solution to designs conforming to the IBM® 8514 graphics standard.

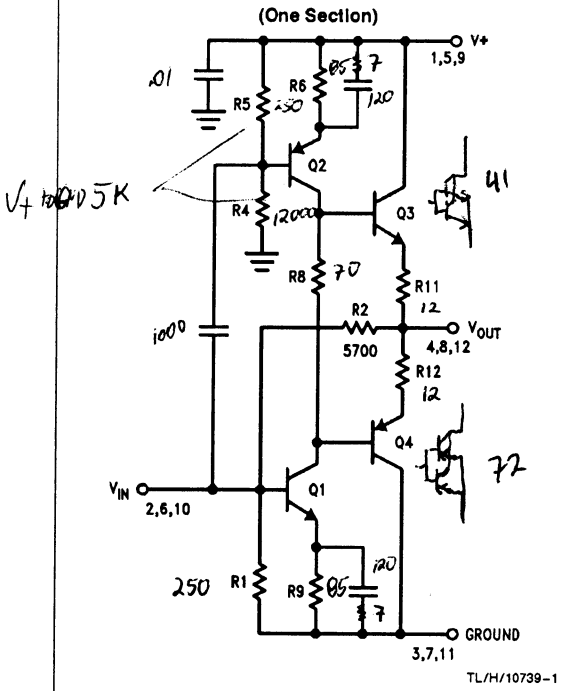
Features

- Operation from 80V power supply
- 80 MHz bandwidth at 50 V_{PP} swings
- Rise/fall time less than 4 ns
- Output signal can swing 70V
- Drives CRT directly

Applications

- CRT driver for RGB monitors
- High voltage transimpedance amplifiers

Schematic and Connection Diagrams



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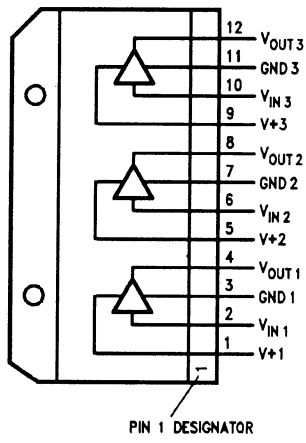

TL/H/10739–2

Top View
Order Number LH2426S
See NS Package Number HY12B

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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V^+	+85V
Power Dissipation, P_D	10W
Storage Temperature Range, T_{STG}	−25°C to +100°C
Operating Temperature Range, T_{CASE}	−20°C to +90°C
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Tolerance	TBD

DC Electrical Characteristics

V_+ = 80V, R1 = 430Ω, C1 = 82 pF, C_L = 8 pF, 50 V_{PP} output swing with 40V DC offset. See *Figure 1*. T_{CASE} = 25°C unless otherwise noted.

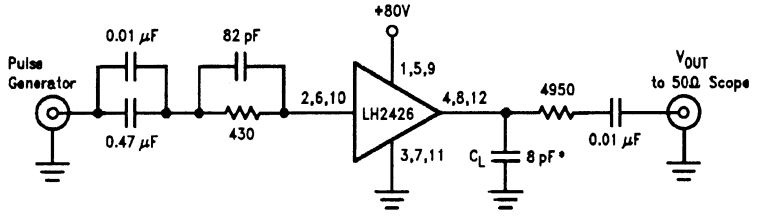
Symbol	Parameter	Conditions	LH2426			Units
			Min	Typical	Max	
V^+	Supply Current (per Amplifier)	No Input or Output Load		24	30	mA
V_{INDC}	Input Offset Voltage		1.4	1.6	1.8	V
V_{OUTDC}	Output Offset Voltage		34	40	46	V
t_R	Rise Time	10% to 90%		3.5	5	ns
t_F	Fall Time	90% to 10%		3.5	5	ns
BW	Bandwidth	−3 dB		100		MHz
Av	Voltage Gain		11	13	14	V/V
OS	Overshoot			10		%
LE	Linearity Error	V_{OUT} from +10V to +70V Note 1		5		%
Δ Av	Gain Matching	Note 2		0.2		dB

Note 1: Linearity error is defined as: The variation in small signal gain from +20V to +70V output with a 100 mVAC, 1 MHz, input signal.

Note 2: Calculated value from voltage gain test on each channel.

Typical Performance Characteristics

Typical Test Circuit (One Section)



TL/H/10739–3

FIGURE 1. Test Circuit (One Section)

***Note:** 8 pF is total load capacitance. It includes all parasitic capacitances.

Figure 1 shows a typical test circuit for evaluation of the LH2426. This circuit is designed to allow testing of the LH2426 in a 50Ω environment such as a pulse generator, oscillosope or network analyzer. To calibrate pulse generator, set to 2.4 Vpp into 50Ω.

Application Hints

The LH2426 is designed as a triple power amplifier for delivering red, blue and green video signals to a cathode ray tube (CRT). It can provide 50V output swing and energize a 12 ns pixel. The input capacitance of a CRT grid is typically 8 pF.

THEORY OF OPERATION

The LH2426 is a two stage amplifier (see schematic on front page). Both stages are in push pull configuration. Q_2 is biased with two resistors, Q_1 gets its bias through the 5700Ω feedback resistor and the input biasing current. The bases of Q_1 and Q_2 are capacitively coupled and therefore Q_2 is also actively driven.

The LH2426 is a transimpedance amplifier: an input current is translated into an output voltage. An input current of about ±4.5 mA will provide full output swing of ±25V. A resistor in series with the input converts the LH2426 into a voltage amplifier, with 430Ω the voltage gain becomes −13.

Application Hints (Continued)

The emitter resistors of Q_1 and Q_2 are bypassed with small capacitors. This increases the gain to the stage for high frequencies and increases the bandwidth of the amplifier.

The power supply is internally bypassed. If low frequencies are present in the power supply line, an electrolytic capacitor is recommended.

INPUT NETWORKS

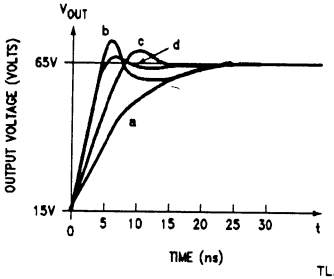
The voltage gain and the response of the amplifiers can be set by adding an R–C to the input.

A 430Ω resistor in series, will set the voltage gain to 13. This will increase the rise and fall times of the system. (See *Figure 2a*) Bypassing the resistor with a capacitor of about 50 pF will restore the rise/fall times but will result in some overshoot. *(Figure 2b)*

Adding a resistor in series with the capacitor will reduce the overshoot but also increase the rise and fall times. *(Figure 2c)*

The addition of a second capacitor will restore the rise and fall times without significant overshoot. *(Figure 2d)*

Suggested values for the resistors and capacitors are shown, however, optimum values may differ depending upon the stray inductances and capacitances present in different board layouts.



TL/H/10739–8

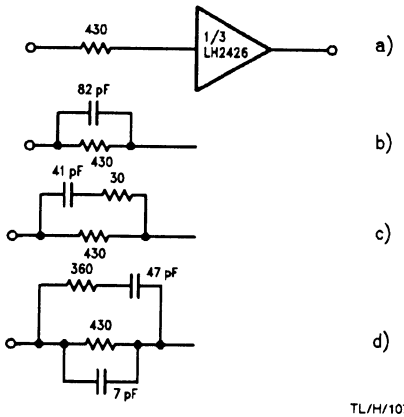


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FIGURE 2. Influence of Input Networks on Switching Performance

Figure 2 compares different input networks and their influence on the switching waveform.

DROOP COMPENSATION

When low frequency square waves are amplified, some droop will occur due to the large change in the thermal dissipation in the input transistors. If this causes a problem, it can be compensated with R-C feedback. Figure 3 illustrates the circuit and recommended component values.

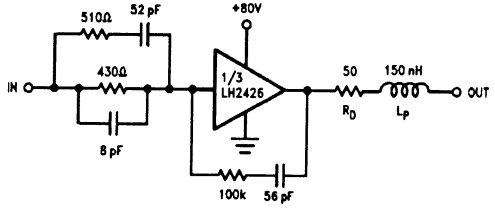
PROTECTING AMPLIFIER OUTPUT FROM TUBE ARCING

During normal CRT operation, internal arcing may occasionally occur. Spark gap protectors do limit the maximum voltage, but to a value that is much higher than allowable on the LH2426. This fast, high voltage, high current pulse can damage the LH2426 output. The addition of a current limiting resistor of 50Ω to 100Ω will provide protection but will slow down response. Adding a series peaking inductor of 100 nH to 150 nH will restore the bandwidth and provide additional protection. (See *Figure 3*)

The value of the inductor can be calculated from:

$$L_P = \left[\frac{(R_0 + R_D)^2}{2.4}\right]C$$

where C is the total load and R_0 is the intrinsic high frequency output resistance of the amplifier, generally 160Ω.



TL/H/10739–7

FIGURE 3. One Section of the LH2426 with Damping Resistor R_D and Peaking Inductance L_P in the Output

SUPPLY BYPASSING

Although the LH2426 has internal supply bypassing, some values of supply line inductance can cause ringing in the supply lines. If this occurs, an additional bypass capacitor or a low-pass filter should be placed near the supply pins.

CAPACITIVE LOADS

The LH2426 is designed to drive capacitive loads, however the very high output slew rate of about 13,700 V/μs can result in charging currents of over 200 mA into a 20 pF load. These very high currents can damage the output transistors.

SHORT CIRCUIT PROTECTION

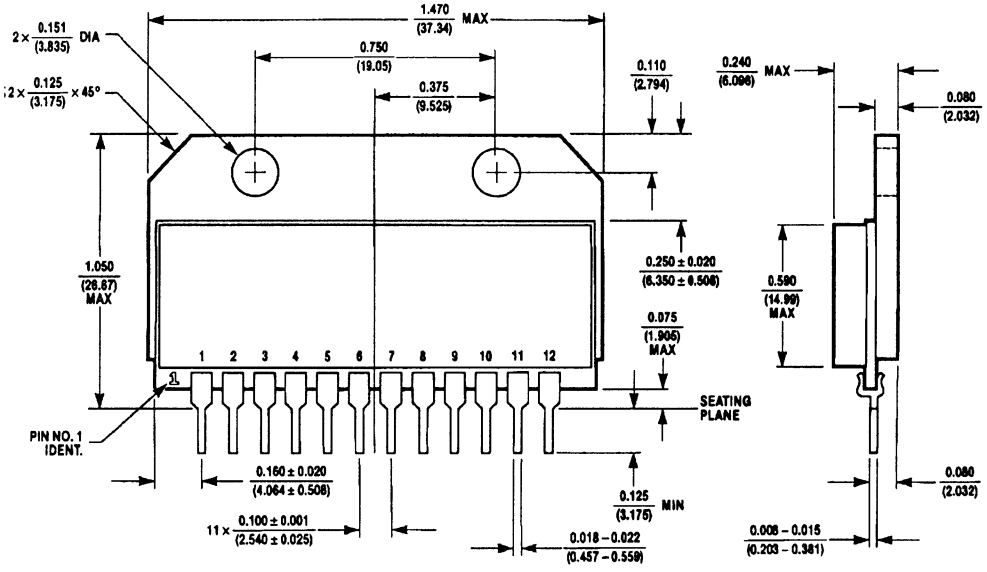
Warning! To provide maximum output speed, the LH2426 does not have short circuit protection. Shorting the output can destroy the device. The lowest value load the LH2426 is designed to drive is 600Ω. If the device is used in an application where the output may be shorted, 600Ω should be placed in series with the output.

HEAT SINKING

As the LH2426 will dissipate up to 10W, an external heatsink is always required. The maximum allowed case temperature is 90°C. To calculate maximum heatsink thermal resistance, use the following formula:

$$R_{th} = (90°C - \text{Max Ambient})/10$$

Physical Dimensions inches (millimeters)



HY12B (REV A)

Note 1: Substrate: 96% alumina.

Note 2: Lid seal: epoxy.

Note 3: Leads: phos. bronze alloy or equiv. with 95 Sn/5 Ag solder DIP.

Note 4: Four radius bumps on corners of lid are optional. Not shown on drawing.

Order Number LH2426S
NS Package Number HY12B

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National Semiconductor

PRELIMINARY
February 1990

LH2440/LH2440A
CRT Preamplifier and Driver

General Description

The LH2440 is a wide band amplifier for high resolution CRT monitors. The device includes a low level amplifier with DC contrast/brightness control and circuitry for black level clamping to accomplish DC restoration. Also included is a high voltage output stage to directly drive a CRT's cathode. The LH2440 provides almost the entire circuitry needed in the video channel between the monitor input connection and the CRT cathode.

The LH2440 can swing 40 V_{PP} into an 8.5 pF load with 4 ns rise and fall times. The device requires minimum external components, thus, facilitating video amplifier design. Moreover, high frequency bypassing for the high voltage amplifier is internally provided for ease of use.

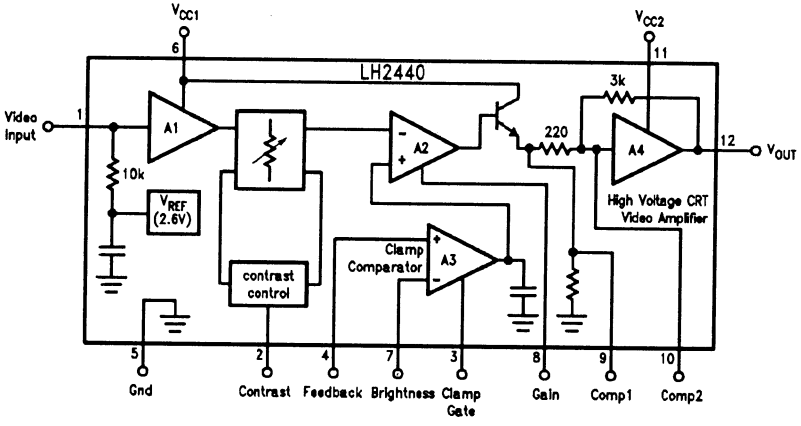
Features

- 90 MHz bandwidth at 40 V_{PP} swing
- Rise/fall times of 4 ns
- DC contrast and brightness controls
- Externally gated comparator for DC restoration of video signal
- Ease of use

Applications

- Video preamplifier and CRT driver for high resolution monitors.

Block and Connection Diagrams



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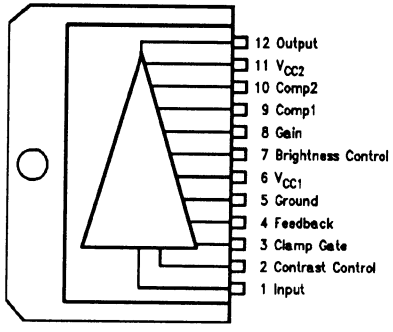


TL/K/10460–2

Order Number LH2440S or LH2440AS
See NS Package Number HY12A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC1} +13.5V

Supply Voltage, V_{CC2} +70V

Power Dissipation, P_D -25 to 107W

Storage Temperature Range, T_{STG} ~~-40°C to +125°C~~

Operating Temperature Range, T_{case} −20°C to +80°C

Lead Temperature (Soldering, < 10 Sec.) 300°C

ESD Tolerance 2 kV

Electrical Characteristics

V_{CC1} = 12V, V_{CC2} = 60V, C_{LOAD} = 8.5 pF, V_{OUT} = 40 V_{PP} Swing with 30 V_{DC} Offset Unless Otherwise Specified
T_{case} = 25°C Unless Otherwise Noted (Note 1).

Symbol	Parameter	Conditions	LH2440/LH2440A			Units (Max. Unless Otherwise Noted)
			Typical	Tested Limit (Note 2)	Design Limit (Note 3)	
I_{CC1}	Supply Current	No Output Load	80	90		mA
I_{CC2}			43	48		mA
V_{BIAS}	Video Input BIAS Voltage		2.6	2.4		Volts (Min)
				2.8		Volts
V_{CL}	Clamp Gate Low Input V	Clamp Comparator ON		0.8		V
V_{CH}	Clamp Gate High Input V	Clamp Comparator OFF		2.0		V(Min)
I_{CL}	Clamp Gate Low Input Current	V4 = 0V	−0.5	−5		µA
I_{CH}	Clamp Gate High Input Current	V4 = 12V	0.005	1		µA
V_{OS}	Comparator Input Offset Voltage	V5 − V7	±0.5	±50		mV
$V_{OUT(DC)}$	Output Offset Voltage		30	34		V
				26		V(Min)
OVR	Output Voltage Range	V7 = 0V to 10V	5 to 55	10 to 50		V
t_R	Rise Time	R_S = 50Ω, LH2440	4	6		ns
t_F	Fall Time	R_S = 50Ω, LH2440	4	6		ns
t_R	Rise Time	R_S = 50Ω, LH2440A	4	5		ns
t_F	Fall Time	R_S = 50Ω, LH2440A	4	5		ns
$A_{V(Max)}$	Gain	V3 = 12V @ 2 MHz	85	70		V/V(Min)
A_V 5V	Attenuation @ 5V	V3 = 5V	10			dB
A_V 2V	Attenuation @ 2V	V3 = 2V	45			dB
T_C (A_V)	Gain Drift	25°C ≤ T_C ≤ 80°C	0.1			% per °C
GS	Gain Stability	V_{CC1} = 10V to 13V V_{CC2} = 55V to 65V	4.3 0.4			% per V
t_s	Settling Time	to ±5%	18			ns
V_{Tilt}	Low Frequency Tilt Voltage	64 KHz Square Wave	2.2			V
BW	Bandwidth (−3 dB)		90			MHz
OS	Overshoot		10			%
THD	Distortion	@ 2 MHz	0.14			%

Note 1: Boldface limits are guaranteed over full temperature range.

Note 2: Tested limits are guaranteed and 100% production tested.

Note 3: Design limits are guaranteed (but not production tested) over the indicated temperature range. These limits are not used to calculate outgoing quality level.

Applications Hints

OUTPUT INFORMATION

Precautions must be taken to prevent excessive overshoot and ringing caused by the inductance of the wire used to connect the LH2440's output to the CRT;s cathode. Since the wire's inductance and the capacitance at the cathode form an LC tank circuit when driven by the amplifier, at the resonant frequency the circuit may introduce overshoot and ringing. A damping resistor in series with the output of the LH2440 can critically damp the output ringing. The resistor value may be calculated from the following equation:

Damping Resistor, $R > 2\sqrt{L/C}$

where , L = Inductance of output wire
C = Capacitance at CRT cathode

Usually, a 50Ω–100Ω damping resistor is adequate. As an added advantage, the damping resistor also protects the amplifier's output against arcing by providing current limiting. Keep in mind that the damping resistor should not be too large; otherwise, the output signal's rise/fall time may be significantly affected due to the RC time constant formed by the damping resistor and the cathode's capacitance.

GROUND CONNECTION

LH2440's ground connection is internally connected to the package's metal tab. Thus, for proper operation, the tab should be connected to the power supply ground.

SHORT CIRCUIT PROTECTION

The LH2440 is designed to drive the capacitive load at the CRT's cathode and does not include short circuit protection. With no series current limiting resistor at the output, the LH2440 will be destroyed if the output is inadvertantly shorted to ground or V^+. When driving a resistive load, it is recommended that the load be greater than 600Ω.

THERMAL CONSIDERATIONS

The LH2440 requires that the package be heat sunk for proper operation under any condition. The worst case power dissipation occurs during full scale transitions i.e., when verticle lines of black and white stripes are displayed on the screen. The amplifier's power dissipation depends on the power supply voltage as well as operating frequency. For instance at V_{CC1} = 12V, V_{CC2} = 60V, and 50 MHz (10 ns pixel), the power dissipation is 5 watts. Such high power dissipation demands that proper care be exercised to ensure sufficient heat sinking.

LH2440's maximum ratings require that the device case temperature be limited to 80°C. Thus at 50°C ambient temperature and 5 watts power dissipation, the thermal resistance of the heat sink should be less than (80°C − 50°C) = 6°C/W. Several approaches to heat sinking may be taken. The simplest is a slug of aluminum with a volume of 3 cu. inches or a sheet of aluminum with an area of 30 sq. inches and a thickness of 0.1 inches. Alternatively, commercially available heat sinks may be used.

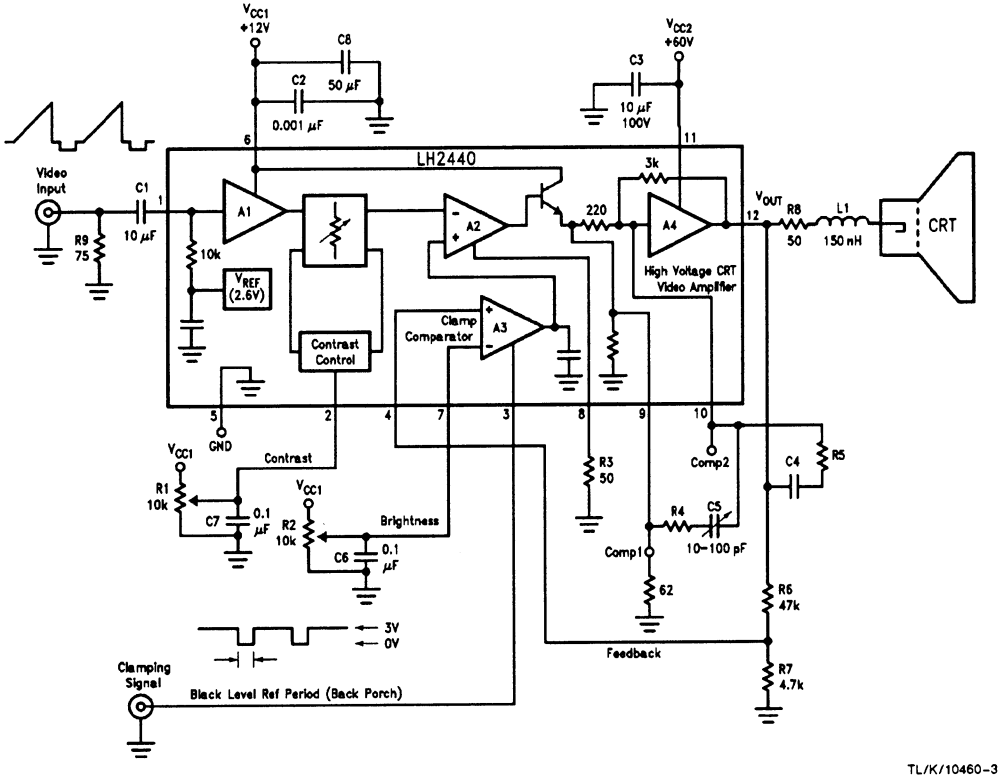
Typical Application

The LH2440 provides a single chip solution for almost all the video signal processing and signal amplification requirements in a high resolution CRT monitor. The blanking function is not included in the LH2440. Blanking is usually done by applying a large negative pulse at the CRT's control grid (G1) during the blanking interval. The LH2440 includes a low voltage preamplifier with contrast and brightness control, and, black level clamping function for DC restoration of the video signal. Also, a wide bandwidth and high voltage amplifier is included to drive the CRT's cathode with a 40 V_{PP} signal. The device is simple to use and requires minimum external components.

Figure 1 shows how the LH2440 may be used to amplify and process the video signal and to drive the CRT's cathode. The video signal is ac coupled to the input of LH2440 through a blocking capacitor, C1, and is referenced to 2.6V by an internal bias voltage. Amplifiers A1 and A2 (see *Figure 1*) are low voltage amplifiers that amplify the 1 V_{PP} video input signal. In addition, A2 drives the high voltage CRT video amplifier, A4, with the proper DC bias.

The potentiometer R1 provides a variable voltage at the LH2440's contrast control pin (pin 2) which allows attenuation of the video output signal. A nearly linear 0 dB to 30 dB attenuation can be obtained by varying the contrast voltage. Contrast control adjustment thus allows the user to vary the video signal level by varying the gain of the amplifier. Maximum gain is achieved when the potential at pin 2 is the same as that of the low voltage power supply, V_{CC1}. With 0 dB attenuation, the gain from input to output is typically 100. Adjusting the potentiometer at the brightness control pin (pin 7) varies the DC offset of the output signal. This feature allows the user to vary the overall brightness or luminance of the picture displayed on the screen.

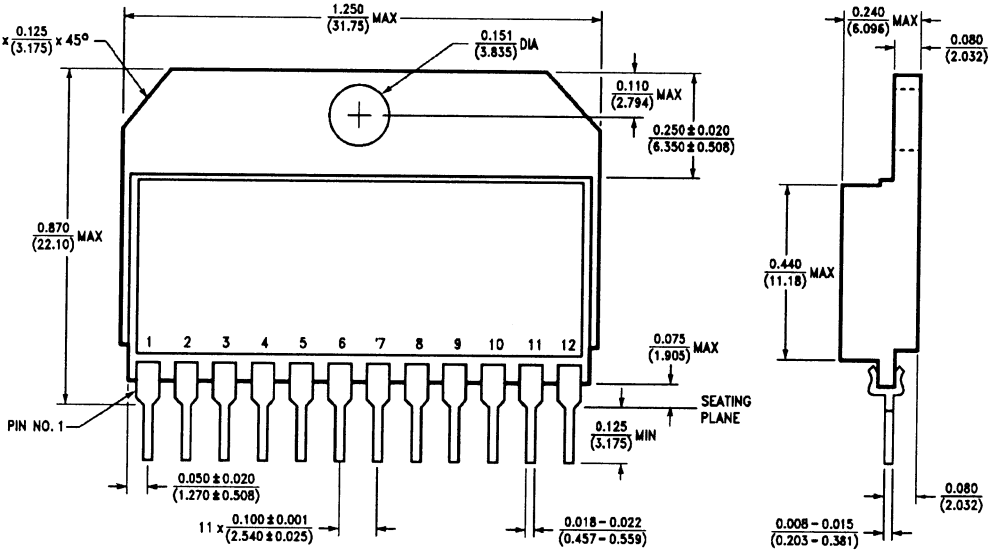
The LH2440 uses black level clamping at the back porch of the video signal to accomplish DC restoration. The clamping signal at the clamp gate (pin 3) enables the clamp comparator A3 during the black level reference period to provide a sample and hold function. DC feedback taken from the output during the black level reference period is compared with the voltage set by the brightness control potentiometer R3. Depending on the output voltage, an internal clamping capacitor is either charged or discharged so that the feedback loop consisting of amplifiers A2, A3 and A4 is stabilized and the output is restored to the black level. All this occurs during the horizontal retrace interval. During the video portion of the signal, A3 is disabled and the clamping capacitor holds the fixed black level reference voltage. Since the beginning of each line starts from a fixed reference voltage corresponding to the black level, the DC component of each line is restored. Adjusting the contrast control varies the amplitude of the video signal relative to the fixed black level. For the circuit of *Figure 1*, rise and fall times of 4 ns were measured at the cathode with a 40 V_{PP} output signal. This corresponds to a bandwidth of over 90 MHz.



TL/K/10460-3

FIGURE 1. Circuit shows how the LH2440 may be used in a high resolution monitor. LH2440 also provides brightness/contrast control and black level clamping.

Physical Dimensions inches (millimeters)



12-Lead Single-In-Line Package (J)
Order Number LH2440S
NS Package Number HY12A

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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National Semiconductor

October 1991

LH3422/LH3424
CRT Video Amplifiers

General Description

The LH3422 and LH3424 are wide bandwidth and high voltage CRT video amplifiers. These amplifiers are specifically designed to directly drive the cathode of high resolution CRT monitors. Both amplifiers work on the transimpedance principle, about ±5 mA input current results in an output swing of ±20V relative to the quiescent output DC level. These amplifiers can easily energize 10 ns pixels and are well suited for monitors with 1280 x 1024 or higher display resolutions. The LH3422 and LH3424 are identical except that the LH3424 has faster rise and fall times and wider bandwidth than LH3422. Both amplifiers can interface to National's LM1201 and LM1203 preamplifiers.

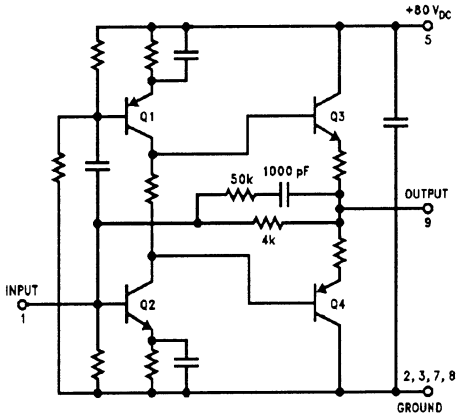
Features

- LH3424: BW = 175 MHz
  Rise/Fall Time = 2 ns
- LH3422: BW = 120 MHz
  Rise/Fall Time = 3 ns
- Drives 8.5 pF capacitive load
- Pin compatible with CR3424
- DC coupled for output level adjust
- Output signal can swing 60V

Applications

- CRT driver for color and monochrome monitors
- High voltage transimpedance amplifier

Schematic and Connection Diagrams



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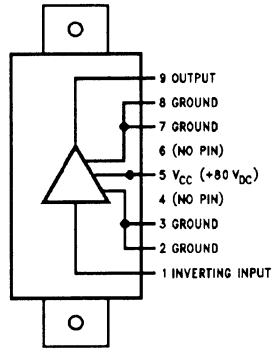
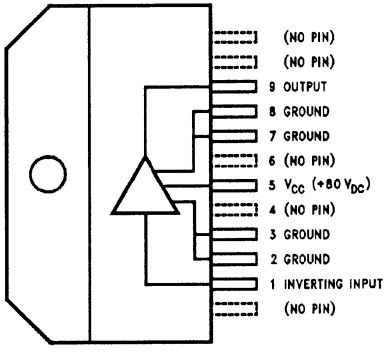


TL/K/11266–2

Order Number LH3422AJ or LH3424AJ
See NS Package Number HY07A



TL/K/11266–3

Order Number LH3422S or LH3424S
See NS Package Number HY07B

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC} +90V

Storage Temperature Range, TSTG −40°C to +125°C

Operating Temperature Range, T_{case} −20°C to +90°C

Lead Temperature (Soldering, <10 sec) 300°C

ESD Tolerance >4KV

DC Electrical Characteristics

Unless otherwise noted, the following specifications apply for V_{CC} = +80V, R1 = 300Ω, C1 = 60 pF (for LH3422), C1 = 90 pF (for LH3424), C_{LOAD} = 8.5 pF, 40 V_{P-P} swing with 40 VDC offset, and T_{CASE} = 25°C. See test circuit, *Figure 1.*

Symbol	Parameter	Conditions	Min (Note 3)	Typ (Note 2)	Max (Note 3)	Units
I_{CC}	Supply Current	Input/Output Open Circuit	35	43.5	47.5	mA
V_{INDC}	Input Offset Voltage	Input/Output Open Circuit	1.15	1.55	1.8	V
V_{OUTDC}	Output Offset Voltage	Input/Output Open Circuit	36	40	44	V
P_D	Power Dissipation (LH3422) Power Dissipation (LH3424)	50 MHz Square Wave 50 MHz Square Wave		6 6	8 8	W W
LE	Linearity Error	V_{OUT} from +10V to +70V		1	5	%

AC Electrical Characteristics

Unless otherwise noted, the following specifications apply for V_{CC} = +80V, R1 = 300Ω, C1 = 60 pF (for LH3422), C1 = 90 pF (for LH3424), C_{LOAD} = 8.5 pF, 40 V_{P-P} swing with 40 VDC offset, and T_{CASE} = 25°C. See test circuit, *Figure 1.* (Note 1)

Symbol	Parameter	Conditions	LH3422			LH3424			Units
			Min (Note 3)	Typ (Note 2)	Max (Note 3)	Min (Note 3)	Typ (Note 2)	Max (Note 3)	
t_R	Rise Time	10% to 90% (Note 4)		3	4		2	2.9	ns
t_F	Fall Time	90% to 10% (Note 4)		3	4		2	2.9	ns
V_{TILT}	Low Frequency Tilt Voltage	1 kHz Square Wave		1.3			1.3		V
$f_{-3\,dB}$	−3 dB Bandwidth	(Note 5)		120			175		MHz
A_V	Voltage Gain	50Ω Source Impedance (Note 6)	11.5	13	14.5	11.5	13	14.5	V/V
OS	Overshoot			10			10		%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: Typical specifications are at +25°C and represent the most likely parametric norm.

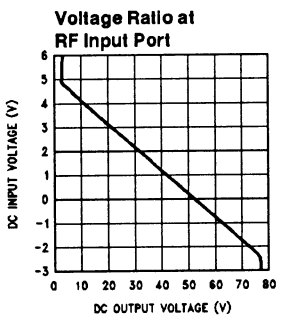
Note 3: Min/Max limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

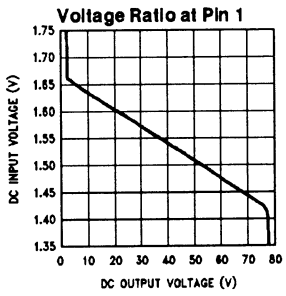
Note 4: Input signal t_r, t_f < 1 ns.

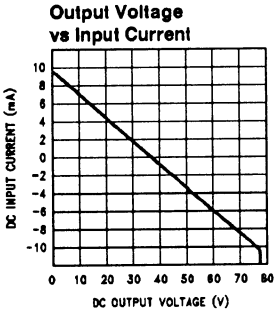
Note 5: −3 dB bandwidth is calculated from the equation; $f_{-3\,dB} = 0.35/t_R$.

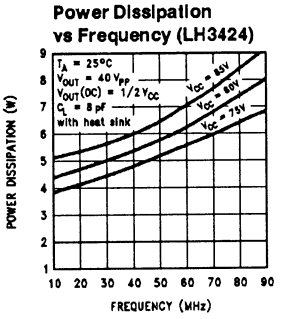
Note 6: Voltage gain is the ratio of the output voltage to the voltage at the RF input port *(Figure 1).*

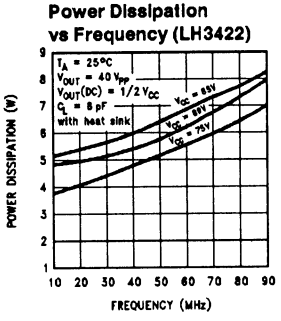
Typical Performance Characteristics











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Application Hints

OUTPUT INFORMATION

The LH3422 and LH3424 are wide bandwidth high voltage amplifiers that can directly drive the cathode of high resolution Cathode Ray Tubes (CRTs). The outputs of both amplifiers are biased at half the supply voltage. With a +80V supply, an output swing of ±20V relative to a 40V output DC bias can easily be achieved. When driving an 8.5 pF capacitance the typical rise and fall times of 2 ns and 3 ns were measured for the LH3424 and LH3422 respectively. During normal CRT operation, tube arcing may occasionally occur. Spark gap protectors are widely used to limit the voltage at the output of the amplifier. In addition a 50Ω to 100Ω resistor is also used in series with the output of the amplifier so as to limit the arc current. This current limiting resistor and the capacitive load offered by the CRT's cathode will degrade the effective rise and fall times at the cathode. Adding a small inductor in series with the amplifier's output will increase the rise and fall times at the cathode due to high frequency peaking of the amplifier's pulse response. This inductor is often referred to as a peaking inductor or peaking coil. At best, the value of the inductor is emperically determined. For the LH3422 and LH3424, a 100 nH to 200 nH inductor is quite adequate.

SHORT CIRCUIT PROTECTION

The LH3424 and LH3422 do not include short circuit protection. If the amplifiers are used to drive a resistive load connected to either ground or V_{CC} then the load must be greater than 600Ω.

INPUT INFORMATION

The "Output Voltage vs Input Current" graph shows that a ±20V swing (from a 40V output DC bias) can be achieved with an input current swing of only ±6.5 mA. For the circuit shown in *Figure 1*, the "Voltage Ratio at RF Input Port" graph relates the input voltage as measured at the RF input port to the voltage at the output; note that the amplifier is phase inverting. With 300Ω for R1 in *Figure 1*, the voltage gain is approximately 13.5, and the low frequency input impedance at the RF input port is approximately 315Ω. The "Voltage Ratio at Pin 1" graph relates the voltage at the input of the amplifier (pin 1) to the output voltage, the output voltage to input voltage ratio is approximately 325 and the low frequency input impedance is approximately 13Ω. With the RF input port open circuited and V_{CC} = 80V, the input of the amplifer (pin 1) is self biased at typically 1.55V while the output is biased at 40V.

SETTING UP GAIN

The LH3424 and LH3422 work on the transimpedance principle. An internal 4 kΩ feedback resistor connected between the input and output converts the input current to output voltage.

For the circuit in *Figure 1*, ±2.25V (referenced to 1.55 V_{DC}) across the 300Ω input resistor results in ±7.5 mA. This current flowing through the 4 kΩ internal feedback resistor results in a ±30V swing at the output.

Application Hints (Continued)

TYPICAL TEST CIRCUIT

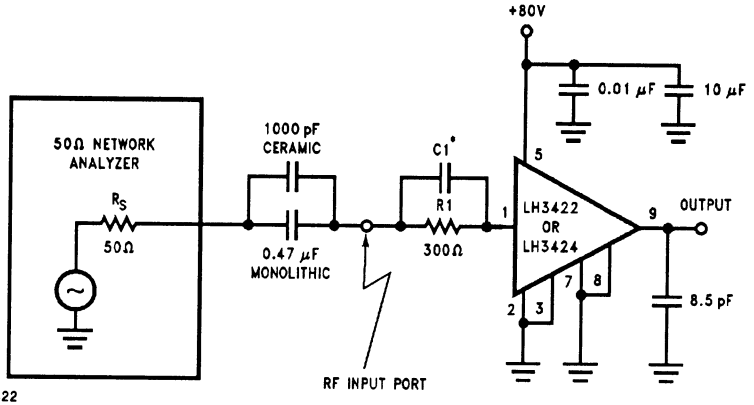
The test circuit in *Figure 1* is driven from either a fast pulse generator with a 50Ω output impedance or network analyzer. The cable between the generator and DUT should be of minimum length. The generator's DC level should be about 1.55V. Use a FET probe with 100X attenuation when using an oscilloscope. Total load capacitance (including probe capacitance) should be limited to 8.5 pF.

The input circuit RC network is tuned to produce peaking when driven from a 50Ω source.

Thermal Considerations

The LH3422 and LH3424 require that the package be heatsunk for proper operation under any condition. Maximum ratings require that the device case temperature be limited to 90°C maximum. Thus at 50°C maximum ambient temperature and 5.0W maximum power dissipation, the thermal resistance of the heat sink should be less than (90−50)°C/6W = 6.7°C/W. Several approaches to heat sinking may be taken. The simplest is a sheet of aluminum with a volume of 4 cubic inches or an area of 43 sq. inches and a thickness of 0.125 inches.

Commercially available heatsinks such as Thermalloy 15509 extrusion would result in size reduction. *Figures 2* and *3* show the two approaches for proper heat sinking. Note that an aluminum spacer must be placed between the package and the heatsink block so as to prevent the device output from being shorted to ground. In the absence of a series current limiting resistor at the output, the device will be destroyed if the output is inadvertently shorted to ground or V_+.



*C1 = 60 pF for LH3422
C1 = 90 pF for LH3424

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FIGURE 1. Typical AC Test Circuit

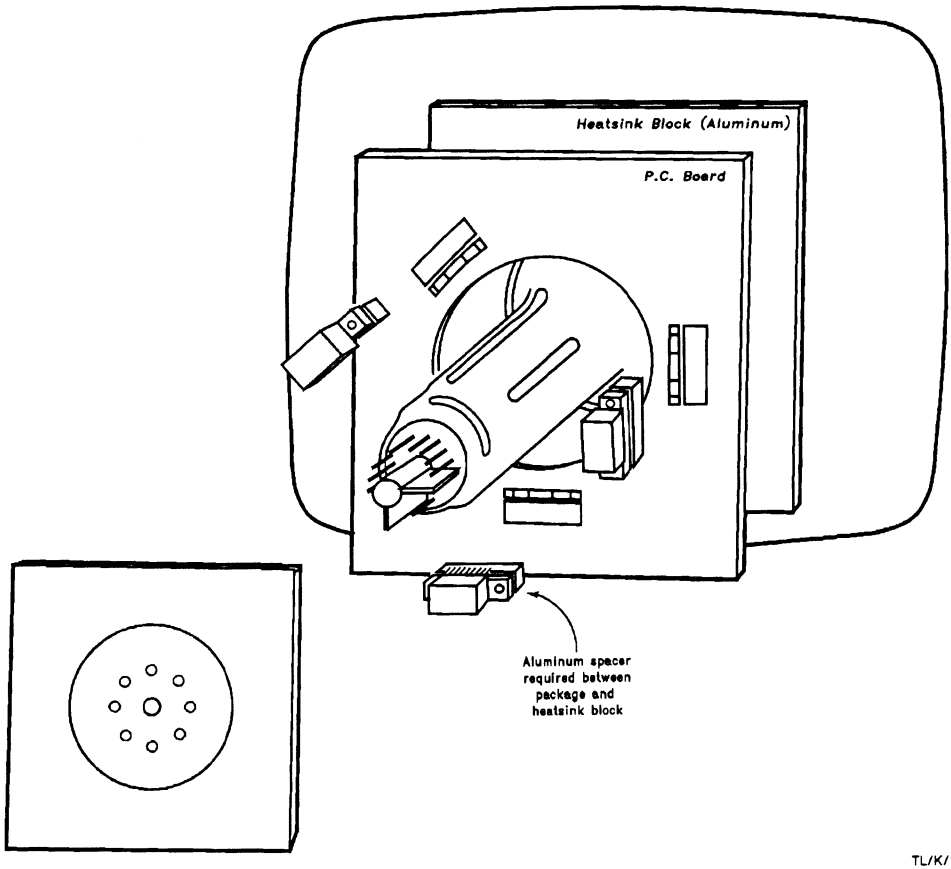

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FIGURE 2. Heat Sinking with an Aluminum Block

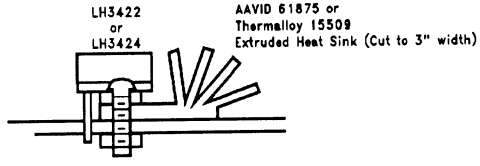

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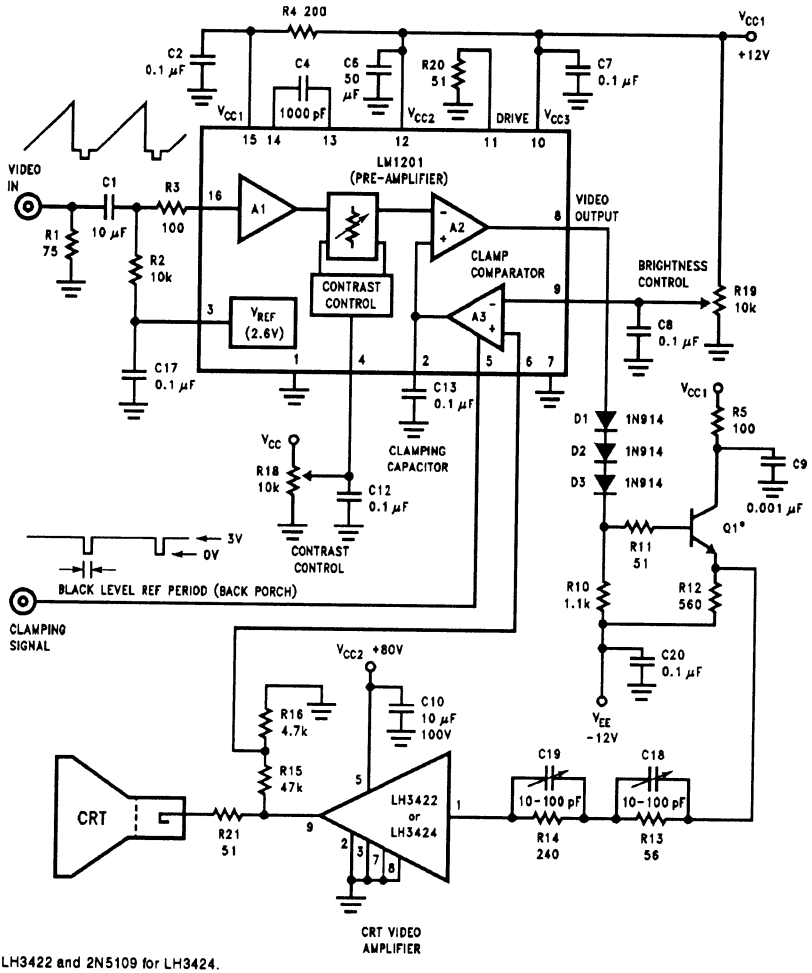
FIGURE 3. Heat Sinking with the Thermalloy 15509 Extrusion

Application Circuits



*Q1 is 2N5770 for LH3422 and 2N5109 for LH3424.

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FIGURE 4. Circuit shows how the LM1201 pre-amplifier and LH3422/LH3424 CRT Video Amplifier may be used to build a 100 MHz Monochrome Monitor

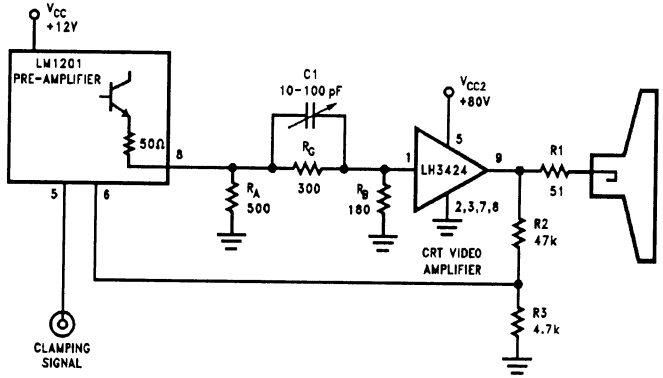

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FIGURE 5. Circuit shows a simple RC interface network which eliminates the need for a level shift stage and additional V_{EE} supply of *Figure 4*.

Evaluation Board

The evaluation board is intended to demonstrate the capabilities of the LH3422 or LH3424 CRT Video Amplifier. The board may be used to interface the amplifier to a CRT display or to evaluate the frequency response or pulse response in a 50Ω system.

Figure 6 shows the schematic of the LH3422 evaluation board. R1 sets the overall gain of the fixture. The test circuit used 300Ω to provide a gain of 13. C1 is a 10 pF–100 pF variable capacitor. Adjust this capacitor to optimize pulse response.

A large bypass capacitor, C2, is needed to reduce lower frequency ringing caused by the power supply wires.

The input is designed to be fed from a 50Ω generator, however, the input impedance at V_{IN} is not well matched to 50Ω and if a long cable is used between the generator and the input, reflections will occur giving unpredictable responses. Two things can be done to get around this problem:

1. Use a very short connector (less than 2 inches) between the generator and the input.
2. Use a 6 dB pad between the cable and the input. This will reduce reflections and provide a 50Ω source to the circuit board.

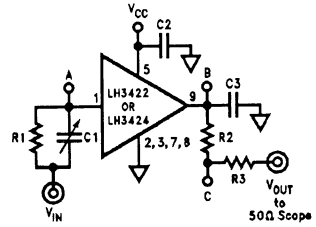

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FIGURE 6. Schematic of LH3422 Evaluation Circuit

The output of the amplifier can drive the CRT cathode directly from point B, while R2 and R3 are used as a 100 to 1 (40 dB) attenuator to a 50Ω scope or network analyzer input. Two resistors are used in series to reduce capacitance and attempt to compensate the frequency response. The layout of the board *(Figure 7)* includes a trace at point C to connect R2 and R3; unfortunately, the capacitance to ground at this point is about 0.6 pF, enough to cause a 20% bandwidth reduction in the response of the attenuator resistors. The resistors should be wired "floating" above the board.

Capacitor C3 is used to simulate the input capacitance at the CRT cathode. The board exhibits about 4.5 pF at the output node of the driver. A capacitor of 4 pF will increase it to the specified value of 8.5 pF.

PARTS LIST

RESISTORS:

R1 300Ω, ¼W, 5%
R2 2.2 kΩ, ¼W, 5%
R3 2.7 kΩ, ¼W, 5%

CAPACITORS:

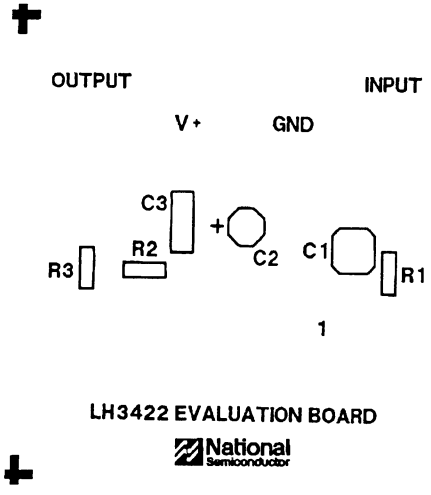
C1 10 pF – 120 pF (muRata ERIE P/N TZ03R121E)
C2 10 µF, 100V, 10%
C3 4 pF, 50V, 10%

HARDWARE:

BNC CONNECTORS (KINGS P/N KC-79-237-MO6)
BANANA JACKS (JOHNSON P/N 108-09XX-001)
HOLTITE SOCKET (AUGAT P/N 8134-HC-5P2)

Evaluation Board (Continued)

(a) Component Placement Guide



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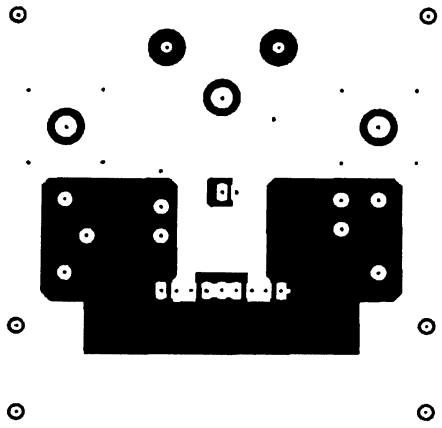
(b) Component (Top) Side



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(c) Solder (Bottom) Side

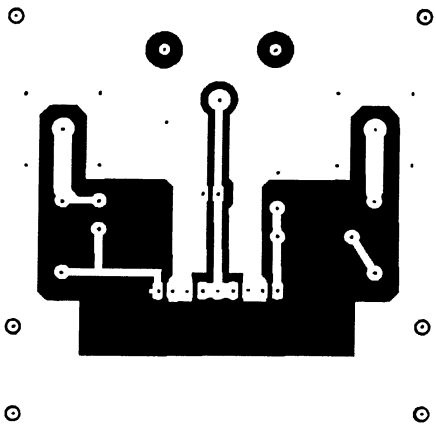

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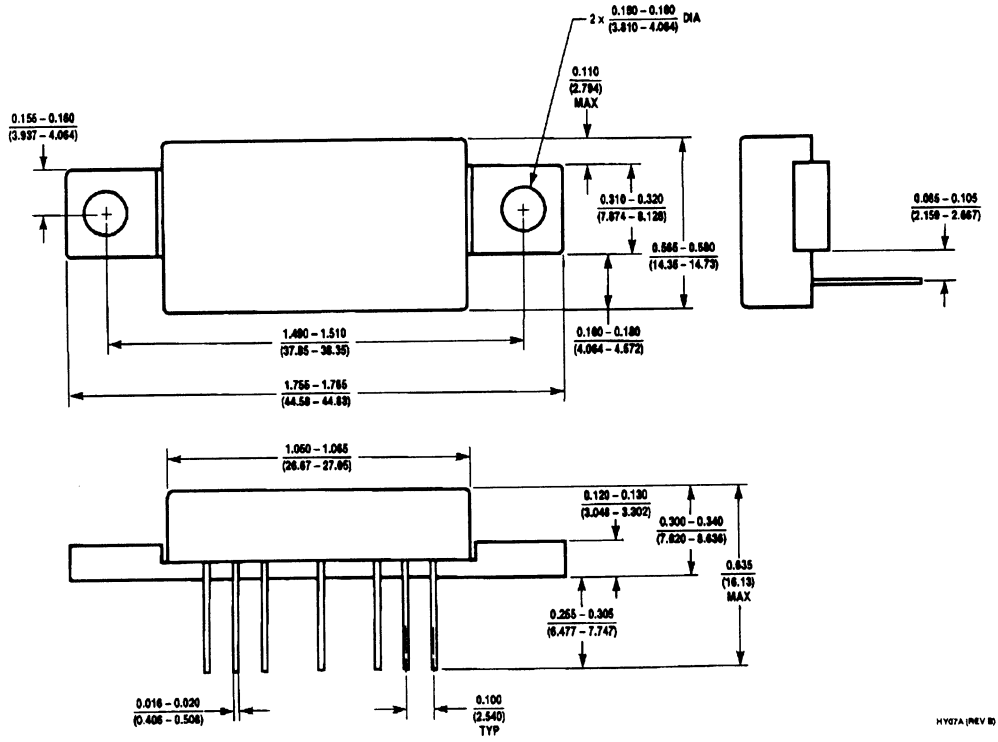
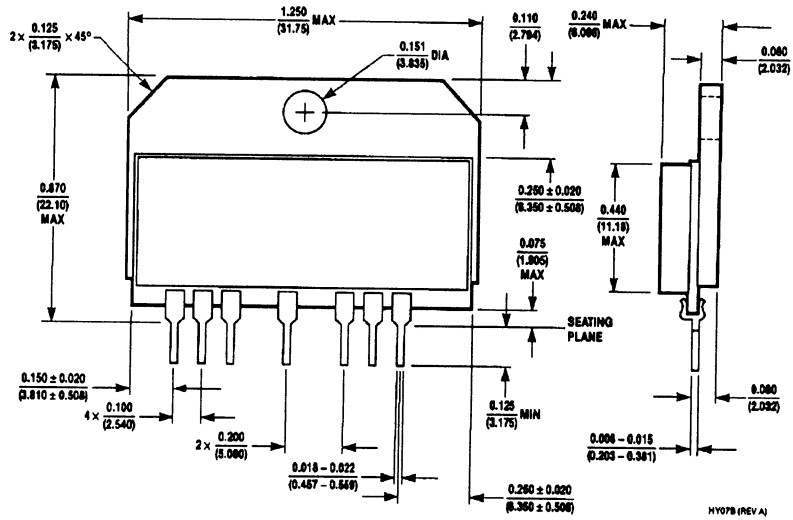
FIGURE 7. PC Board Layout and Component Placement Guide

Physical Dimensions inches (millimeters)



7-Lead SIP Hybrid Package (J)
Order Number LH3422AJ or LH3424AJ
NS Package Number HY07A

Physical Dimensions inches (millimeters) (Continued)



9-Lead Single-In-Line Package (S)
Order Number LH3422S or LH3424S
NS Package Number HY07B

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National Semiconductor

LM1201 Video Amplifier System

General Description

The LM1201 is a wideband video amplifier system intended for high resolution monochrome or RGB monitor applications. In addition to the wideband video amplifier the LM1201 contains a gated differential input black level clamp comparator for brightness control and an attenuator circuit for contrast control. The LM1201 also contains a voltage reference for the video input. For medium resolution RGB color monitor applications also see the LM1203 Video Amplifier System data sheet.

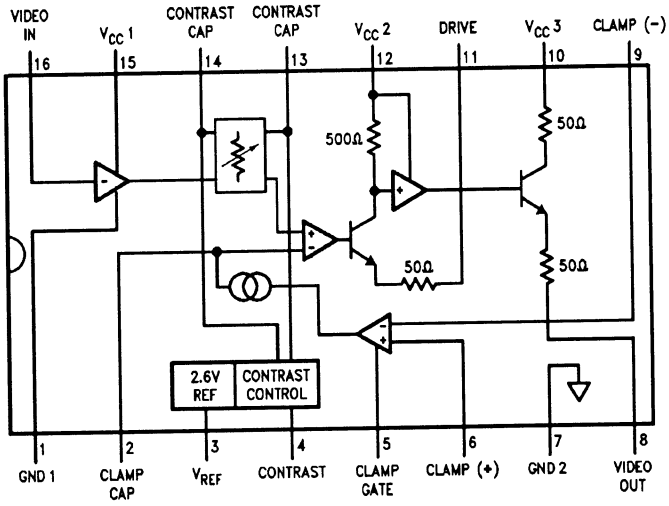
Features

- Wideband video amplifier (200 MHz @ −3 dB)
- Attenuator circuit for contrast control (>40 dB range)
- Externally gated comparator for brightness control
- Provisions for external gain set and peaking of video amplifier
- Video input voltage reference
- Low impedance output driver

Typical Applications

- CRT video amplifiers
- Video switches
- High frequency video preamplifiers
- Wideband gain controls
- PC monitors
- Workstations
- Facsimile machines
- Printers

Block and Connection Diagram



TL/H/10006–1

FIGURE 1

Order Number LM1201M or LM1201N
See NS Package Number M16A or N16E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage V_{CC} Pins 10, 12, 15 to Ground Pins, 1, 7	13.5V
Voltage at Any Input Pin (V_{IN})	$V_{CC} \geq V_{IN} \geq GND$
Video Output Current (I_8)	28 mA
Package Power Dissipation at $T_A = 25°C$ (Above 25°C derate based on (θ_{JA} and T_J)	1.56W
Package Thermal Resistance (θ_{JA}) N16E	80°C/W
Package Thermal Resistance (θ_{JA}) M16A	100°C/W

Junction Temperature (T_J)	150°C
Operating Temperature Range (T_A)	0°C to +70°C
Storage Temperature Range (T_{STG})	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	265°C
ESD Susceptibility	2 kV

Human body model: 100 pF discharged through a 1.5 kΩ resistor

Electrical Characteristics

See Test Circuit (Figure 2), $T_A = 25°C$; $V_{CC1} = V_{CC2} = V_{CC3} = 12V$

DC Static Tests

S9 Open; V4 = 6V; V5 = 0V; V6 = 2.0V unless otherwise stated

Symbol	Parameter	Conditions	Typical	Tested Limit (Note 1)	Design Limit (Note 2)	Units (Limits)
I_S	Supply Current	V_{CC} Pins 12, 15 Only	45	57		mA(max)
V_3	Video Input Reference Voltage		2.65	2.4		V(min)
				2.95		V(max)
I_{16}	Video Input Bias Current	$(V_3-V_{16})/10\,k\Omega$	5.0	20		μA(max)
V_{5L}	Clamp Gate Low Input Voltage	Clamp Comparator On	1.2	0.8		V(min)
V_{5H}	Clamp Gate High Input Voltage	Clamp Comparator Off	1.6	2.0		V(max)
I_{5L}	Clamp Gate Low Input Current	$V_5 = 0V$	−0.5	−5.0		μA(max)
I_{5H}	Clamp Gate High Input Current	$V_5 = 12V$	0.005	1		μA(max)
I_{2+}	Clamp Cap Charge Current	$V_2 = 0V$	1	0.55		mA(min)
I_{2-}	Clamp Cap Discharge Current	$V_2 = 5V$	−1	−0.55		mA(min)
V_{8L}	Video Output Low Voltage	$V_2 = 0V$	0.5	0.9		V(max)
V_{8H}	Video Output High Voltage	$V_2 = 5V$	8.5	8.0		V(min)
V_{OS}	Comparator Input Offset Voltage	V_6-V_9	±0.5	±25		mV(max)

AC Dynamic Tests

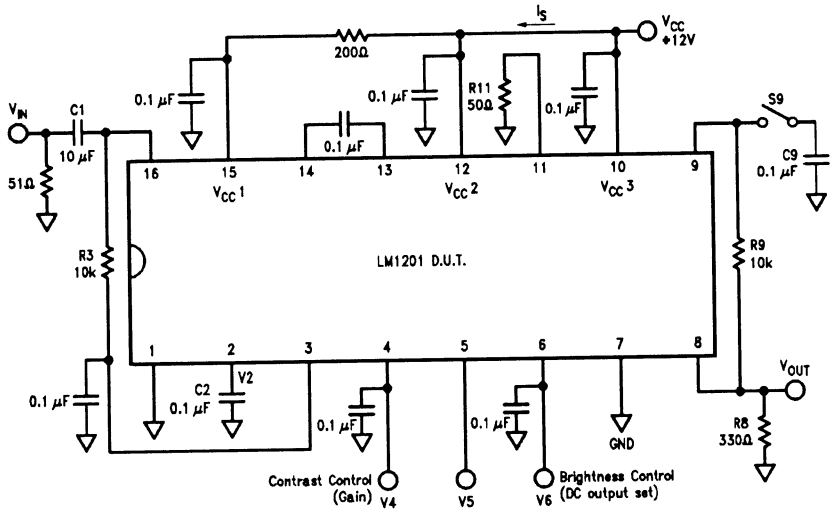
S9 Closed, $V_5 = 0V$, $V_6 = 4V$

Symbol	Parameter	Conditions	Typ	Tested Limit (Note 1)	Design Limit (Note 2)	Units (Limits)
Av max	Video Amplifier Gain	$V_4 = 12V$	8	5.5		V/V(min)
ΔAv 5V	Attenuation @ 5V	Ref: Av max, $V_4 = 5V$	−10			dB
ΔAv 2V	Attenuation @ 2V	Ref: Av max, $V_4 = 2V$	−45			dB
THD	Video Amplifier Distortion	$V_4 = 5V$, $V_O = 1\,V_{p-p}$	0.3			%
f(−3dB)	Video Amplifier Bandwidth (Note 3)	$V_4 = 12V$, $V_O = 100\,mV_{rms}$	200		170	MHz(min)
t_r	Output Rise Time (Note 3)	$V_O = 4\,V_{p-p}$	2.5			ns
t_f	Output Fall Time (Note 3)	$V_O = 4\,V_{p-p}$	3			ns

Note 1: These parameters are guaranteed and 100% production tested.

Note 2: Design limits are guaranteed (but not 100% production tested). These limits are not used to calculate outgoing quality levels.

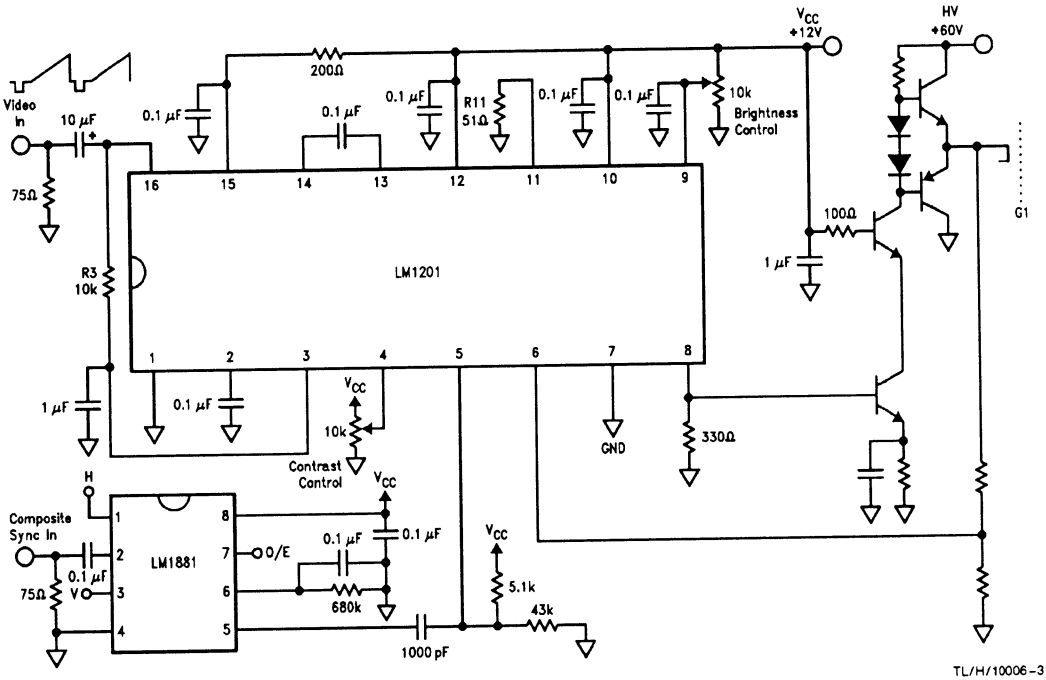
Note 3: When measuring video amplifier bandwidth or pulse rise and fall times, a double sided full ground plane printed circuit board without socket is recommended.



TL/H/10006–2

FIGURE 2. LM1201 AC/DC Test Circuit

Note: When $V_S \leq 0.8V$ and S9 is closed, DC feedback around the Video Amplifier is provided by the clamp comparator. Under these conditions sine wave or 50% duty cycle square waves can be used for test purposes. The low frequency dominant pole is determined by C2 at Pin 2. Capacitor C9 at pin 9 prevents overloading the clamp comparator inverting input. See applications section for additional information.



TL/H/10006–3

FIGURE 3. Typical Application of the LM1201

APPLICATIONS INFORMATION

Figure 4 shows the block diagram of a typical analog monochrome monitor. The monitor is used with CAD/CAM work stations, PCs, arcade games and in a wide range of other applications that benefit from the use of high resolution display terminals. Monitor characteristics may differ in such ways as sweep rates, screen size, or in video amplifier speed but will still be generally configured as shown in *Figure 4*. Separate horizontal and vertical sync signals may be required or they may be contained as a composite signal in the video input signal. The video input signal is usually supplied by coaxial cable which is terminated in 75Ω at the monitor input and internally AC coupled to the video amplifier. The input signal is approximately 1V peak-to-peak in amplitude and at the input of the high voltage video section, approximately 6V peak-to-peak. At the cathode of the CRT the video signals can be as high as 60V peak to peak. The block in *Figure 4* labeled "Video Amplification with DC Controlled Gain/Black Level" contains the function of the LM1201 video amplifier system.

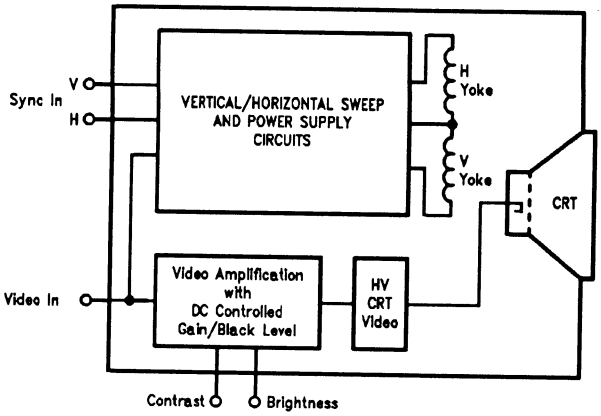


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FIGURE 4. Typical Monochrome Monitor Block Diagram

Circuit Description

Figure 5 is a block diagram of the LM1201 along with the contrast and brightness controls. The contrast control is a DC operated attenuator which varies the AC gain of the amplifier without introducing any signal distortions or DC output shift. The brightness control function requires a "sample and hold" circuit (black level clamp) which holds the DC bias of the video amplifier and CRT cathodes constant during the black level reference portion of the video waveform. The clamp comparator, when gated on during this reference period, will charge or discharge the clamp capacitor until the non-inverting input of the clamp comparator matches that of the inverting input voltage which was set by the brightness control.

Figure 6 is a simplified schematic of the LM1201 video amplifier along with the recommended external components. The IC pin numbers are circled with all external components shown outside of the dashed line. The video input is applied to pin 16 via the 10 μF coupling capacitor. DC bias to the video input is through the 10 kΩ resistor which is connected to the 2.6V reference at pin 3. The low frequency roll-off of the amplifier is set by these two components. Transistor Q1 buffers the video signal to the base of Q2. The Q2 collector current is then directed to the V_{CC1} supply through Q3 or to V_{CC2} through Q4 and the 500Ω load resistor depending upon the differential DC voltage at the bases of Q3 and Q4. The Q3 and Q4 differential base voltage is determined by the contrast control circuit which is described below. The black level DC voltage at the collector of Q4 is maintained by Q5 and Q6 which are part of the black level clamp circuit also described below. The video signal appearing at the collector of Q4 is then buffered by Q7 and level shifted down by Z1 and Q8 to the base of Q9 which will then provide additional system gain.

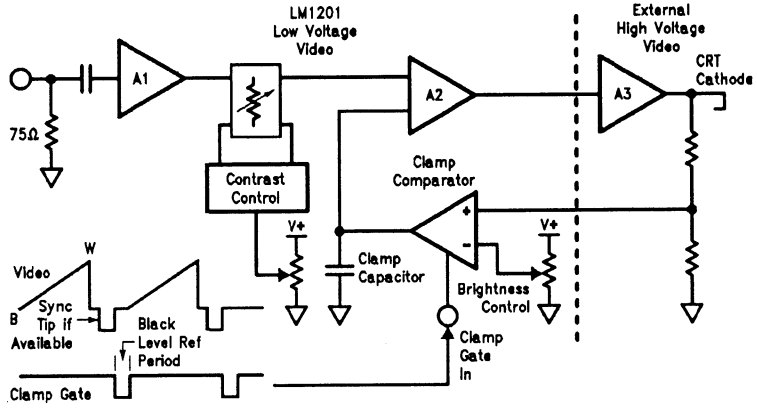

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FIGURE 5. Block Diagram of LM201 Video Amplifier with Contrast and Black Level Control

Circuit Description (Continued)

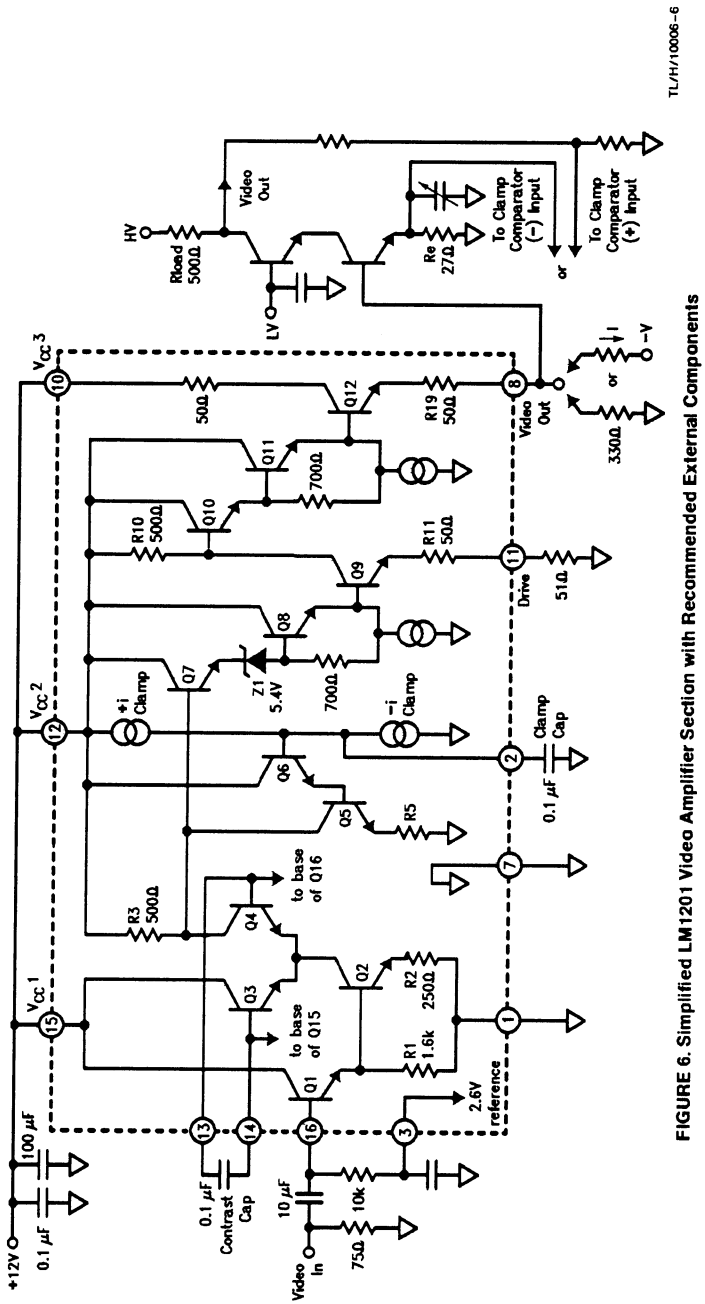

FIGURE 6. Simplified LM1201 Video Amplifier Section with Recommended External Components

Circuit Description (Continued)

The "Drive" pin will allow the user to set the maximum gain of the amplifier based on the range of input video signal levels and the CRT stage gain if it is fixed or limited. When using three LM1201 devices for high resolution RGB applications, the "Drive" pin allows the user to trim the gain of each channel to correct for differences in the three CRT cathodes. A small capacitor (12 pF) in shunt with a 51Ω drive resistor at this pin will extend the high frequency gain of the video amplifier by compensating for some of the internal high frequency roll off. The 51Ω resistor will set the system gain to approximately 8 or 18 dB. The video signal at the collector of Q9 is buffered and level shifted down by Q10 and Q11 to the base of the output emitter follower Q12. Between the emitter of Q12 and the video output pin is a 50Ω resistor which is included to prevent spurious oscillations when driving capacitive loads. An external emitter resistor must be added between the video output pin and ground. The value of this resistor should not be less than 330Ω, otherwise package power limitations may be exceeded when worst case (high supply, max supply current, max temp) calculations are made. If negative going pulse slewing is a problem because of high capacitive loads (>10 pF), a more efficient method of emitter pull down would be to connect a suitable resistor to a negative supply voltage. This has the effect of a current source pull down when the minus supply voltage is −12V, and the emitter current is approximately 10 mA. The system gain will also increase slightly because less signal will be lost across the internal 50Ω resistor. Precautions must be taken to prevent the video output pin from going below ground since IC substrate currents may cause erratic operation. The collector current from the video output transistor is returned to the power supply at V_{CC3}, pin 10. When making power dissipation calculations note that the datasheet specifies only the V_{CC1} and V_{CC2} supply currents at 12V. The IC power dissipation contribution of V_{CC3} is dependent upon the video output emitter pull down load.

In normal operation the minimum black level voltage that can be set at the video output pin is approximately 2V at maximum contrast setting. In applications that require a lower black level voltage, a resistor (approximately 16 kΩ) can be added from pin 3 to ground. This has the effect of raising the DC voltage at the collector of Q4 which will extend the range of the black level clamp by allowing Q5 to remain active. In applications that require video amplifier shutdown due to fault conditions detected by monitor protection circuits, pin 3 and the wiper arms of the contrast and brightness controls can be grounded without harming the IC. This assumes some series resistance between the top of the control potentiometers and V_{CC}.

Figure 7 shows the internal construction of the pin 3 2.6V reference circuit which is used to provide temperature and supply voltage tracking compensation for the video amplifier input. The value of the external DC biasing resistors should not be larger than 10 kΩ when using more than one LM1201 (e.g. in RGB systems) because minor differences in input bias currents on the individual video amplifiers may cause offsets in gain.

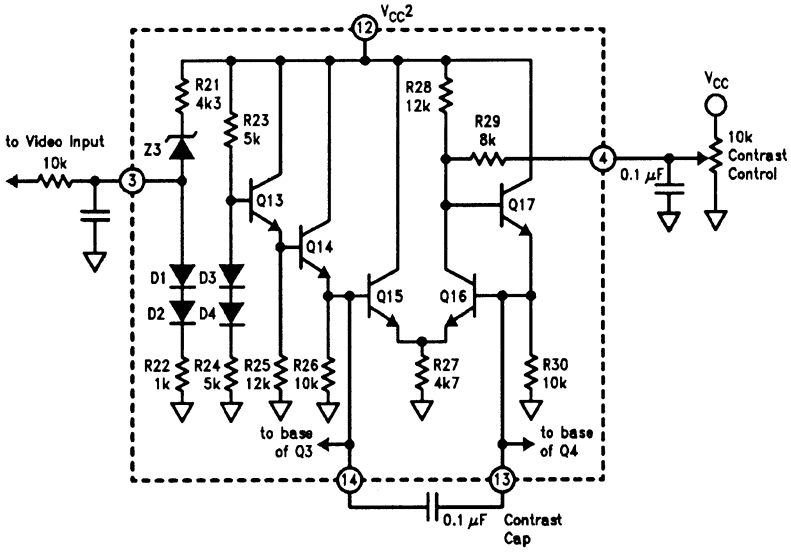

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FIGURE 7. LM1201 Video Input Voltage Reference and Contrast Control Circuits

Circuit Description (Continued)

Figure 7 also shows how the contrast control circuit is configured. Resistors R23, R24, diodes D3, D4, and transistor Q13 are used to establish a low impedance zero TC half supply voltage reference at the base of Q14. The differential amplifier formed by Q15, Q16 and feedback transistor Q17 along with resistors R27, R28 establish a differential base voltage for Q3 and Q4 in *Figure 6*. When externally adding or subtracting current from the collector of Q16, a new differential voltage is generated that reflects the change in the ratio of currents in Q15 and Q16. To provide voltage control of the Q16 current, resistor R29 is added between the Q16 collector and pin 4. A capacitor should be added from pin 4 to ground to prevent noise from the contrast control pot from entering the IC.

Figure 8 is a simplified schematic of the clamp gate and clamp comparator section of the LM1201. The clamp gate circuit consists of a PNP input buffer transistor (Q18), a PNP emitter coupled pair referenced on one side to 2.1V (Q19, Q20) and an output switch (Q21). When the clamp gate input at pin 5 is high (>1.5V), the Q21 switch is on and shunts the I1 1mA current to ground. When pin 5 is low (<1.3V), the Q21 switch is off and the I1 1mA current source is mirrored or "turned around" by reference diode D5 and Q26 to provide a 1mA current source for the clamp comparator. The inputs to the comparator are similar to the clamp gate input except that an NPN emitter coupled pair is used to control the current which will charge or discharge the clamp capacitor at pin 2. PNP transistors are used at the inputs because they offer a number of advantages over NPNs. PNPs will operate with base voltages at or near ground and will usually have a greater reverse emitter-base breakdown voltage (BVebo). Because the differential input voltage to the clamp comparator during the video scan period could be greater than the BVebo of NPN transistors, resistor R34 with a value one half that of R33 or R35 is connected between the bases of Q23 and Q27. This resistor will limit the maximum differential input to Q24, Q25 to approximately 350 mV. The clamp comparator common mode range extends from ground to approximately 9V and the maximum differential input voltage is V_{CC} and ground.

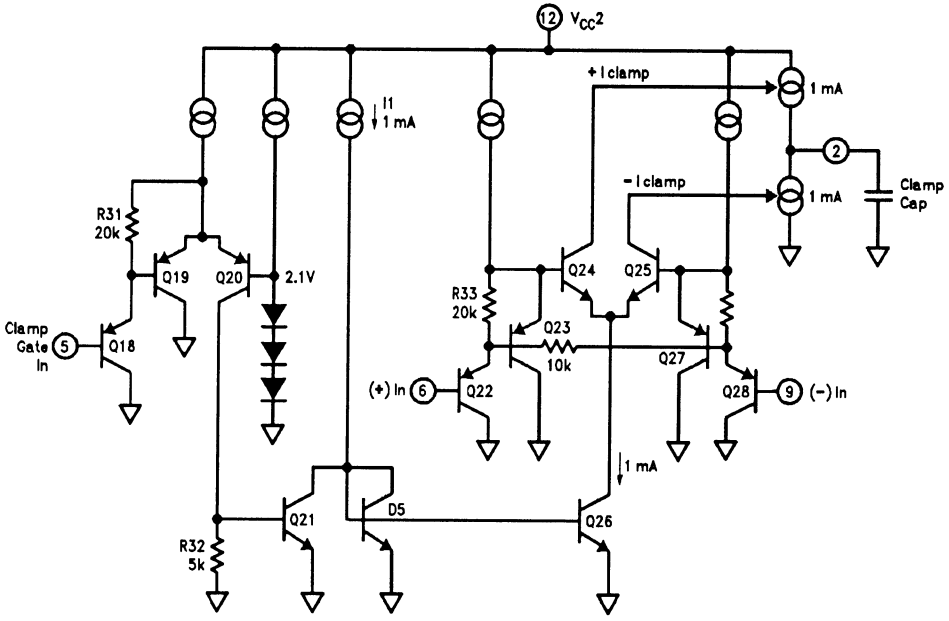

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FIGURE 8. Simplified Schematic of LM1201 Clamp Gate and Clamp Comparator Circuits

Applications Information

Figure 9 shows the configuration of a high frequency amplifier with non-gated DC feedback. Pin 5 is tied low to turn on the clamp comparator (feedback amplifier). The inverting input (pin 9) is connected to the amplifier output from a low pass filter. Additional low frequency filtering is provided by the clamp capacitor. The Drive pin is grounded to allow for the widest range of output signals. Maximum output swing is achieved when the DC output is set to approximately 4.5V.

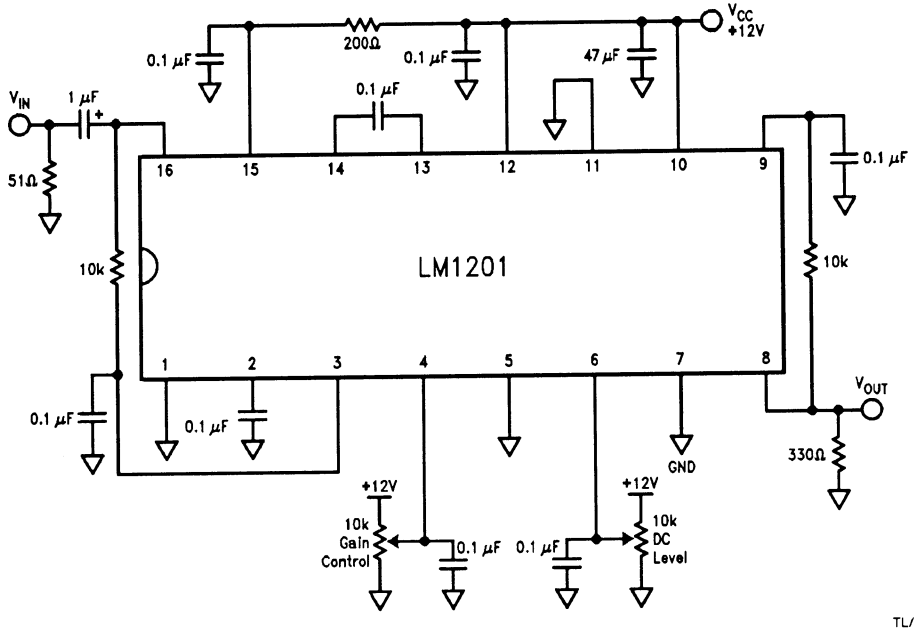

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FIGURE 9. High Frequency Amplifier/Attenuator Circuit with Non-Gated DC Feedback (Non-Video Applications)

Applications Information (Continued)

Figure 10 shows the LM1201 set up as a video amplifier with biphase outputs. Because the collector of output transistor Q12 is the only internal connection to V_{CC3}, a 75Ω termination to the power supply voltage allows one to obtain inverted video at pin 10. Black level on the non-inverted video output (pin 8) is set to 1.5V by the voltage divider on pin 6.

Figure 11 shows how a high frequency video switch may be designed using multiple LM1201 devices. All outputs can be OR'ed together assuming no more than one channel is selected at any given time. Channel selection is accomplished by keeping the appropriate SELECT SWITCH open. Closing the SELECT SWITCH on a given channel disables that channel's output (pin 8) leaving it in a high impedance state. A single pair of contrast and brightness potentiometers control the selected channel's gain and output DC level.

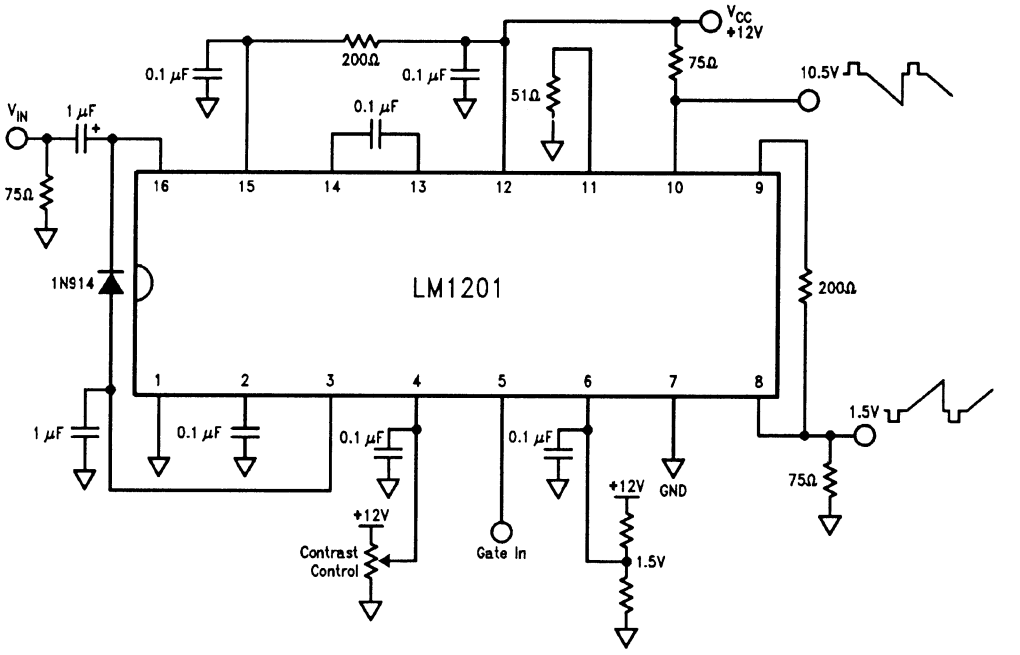

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FIGURE 10. Preclamped Video Amplifier with Biphase Outputs

Applications Information (Continued)

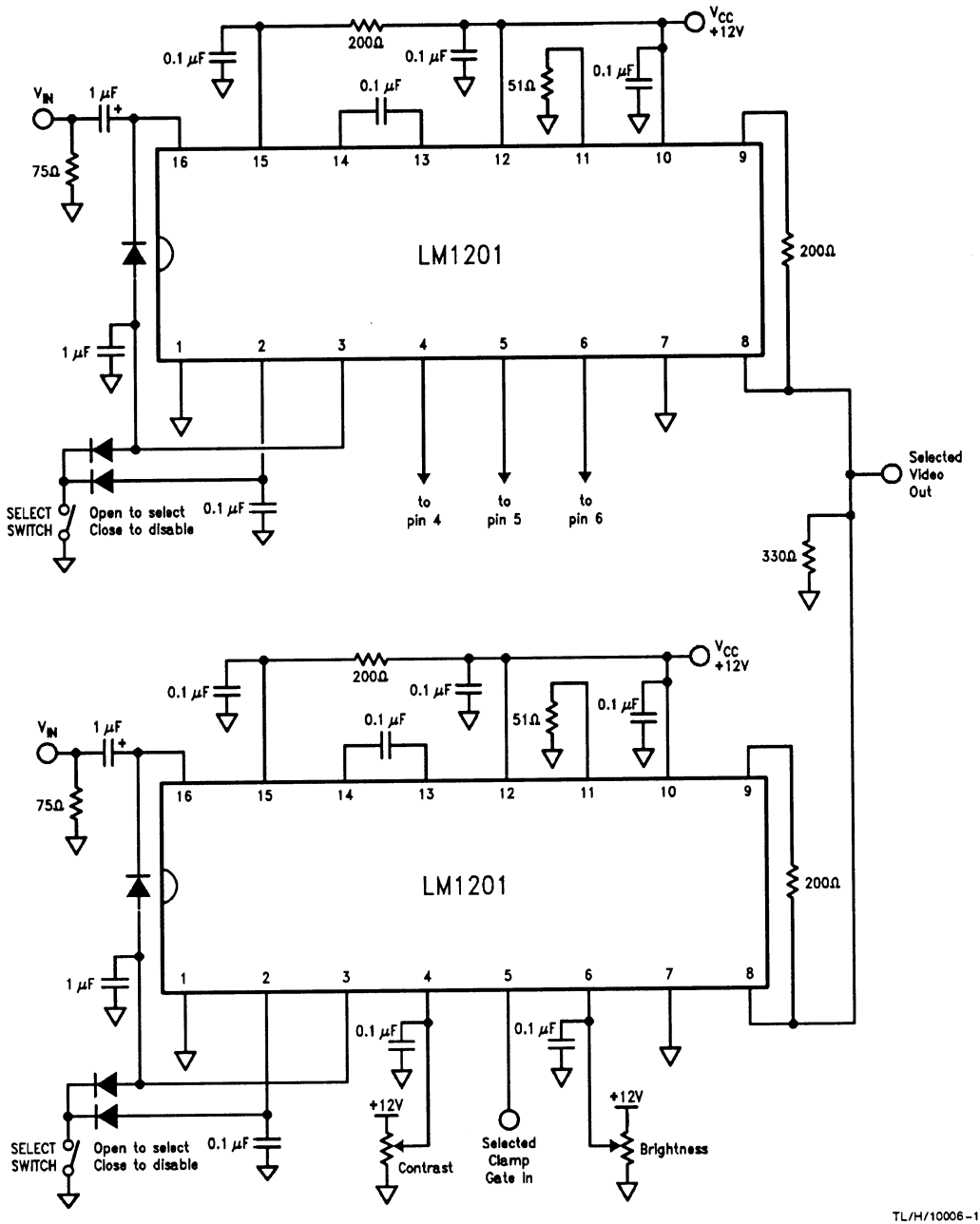

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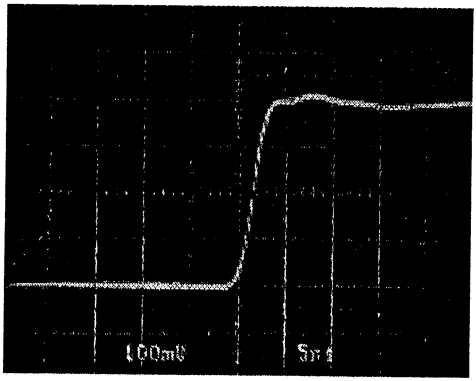
FIGURE 11. High Frequency Video Switch with Common Contrast and Brightness Controls

Rise Time No Socket



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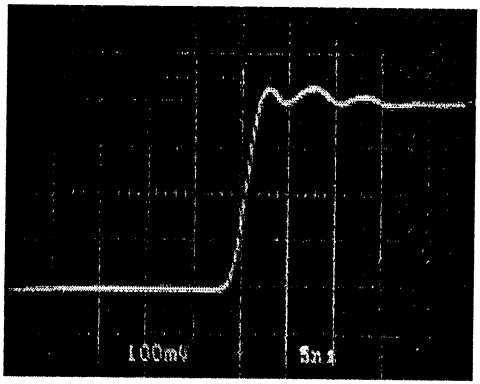
Rise Time In Socket



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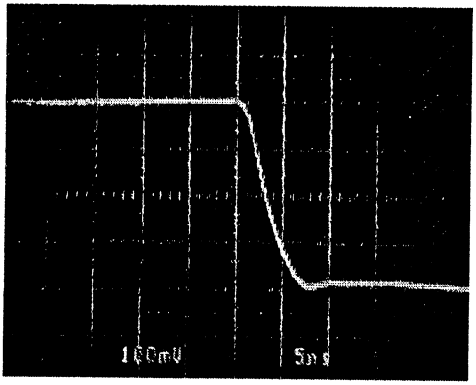
Fall Time No Socket



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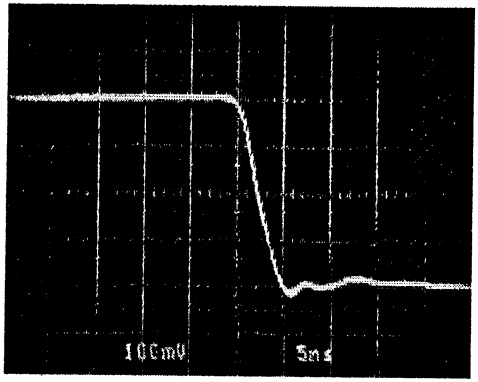
Fall Time In Socket

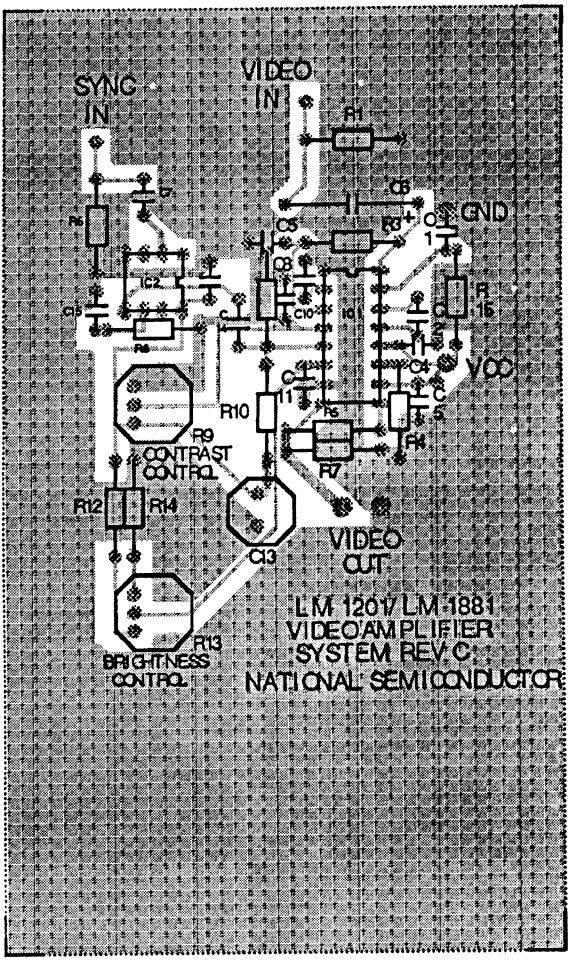


TL/H/10006–15

HP8082 pulse generator
HP10241A 10:1 voltage divider
HP1120A 500 MHz FET probe
Tektronix 2465A 350 MHz scope

Scale for All Photos—Vert: 1V/Div
Horiz: 5 ns/Div

- Actual output signal swings 4 V_{p-p} (10:1 divider is used)
- Contrast is set to maximum
- V_{IN} = 500 mV_{p-p}
- R_{DRIVE} = 50Ω
- Vertical scale is actually 1V/div and not 100 mV/div due to 10:1 attenuator used.
- Outputs are centered at 4V DC.



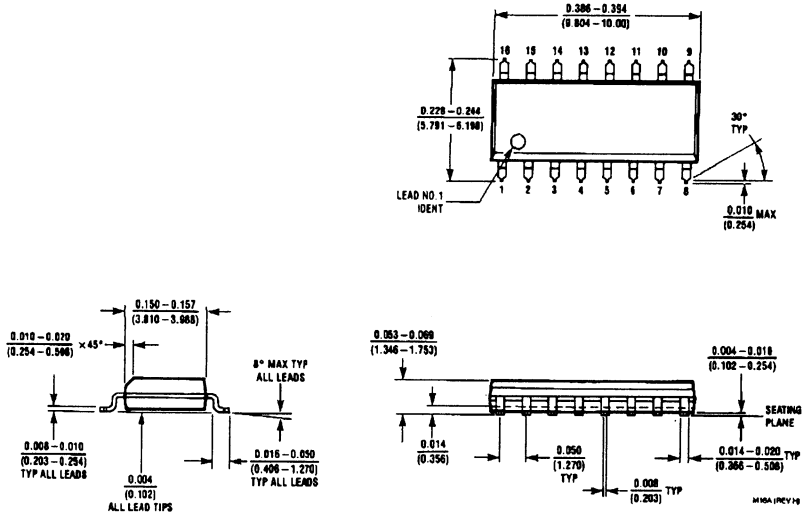
TL/H/10006–16

Note: The p.c.b. layout shown above is suitable for evaluating the performance of the LM1201. Although it is similar to the typical application circuit of Figure 3, there is no c.r.t. driver stage. Instead, a feedback resistor is connected between Pins 8 and 9 and the brightness control is connected to Pin 6. Again, for best results, a socket should not be used for the LM1201.

COMPONENT VALUES:

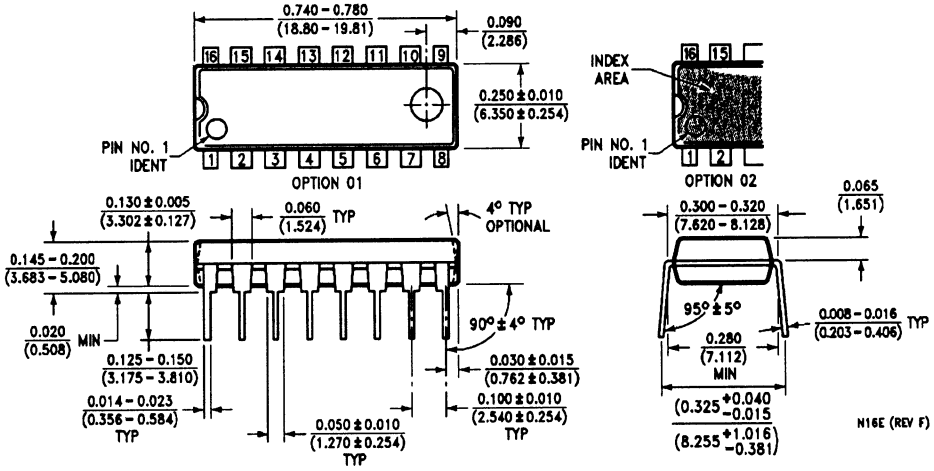
R1	75Ω, 5%, 1/4 watt, carbon composition	C1	0.1 μF, ceramic
R3	10 kΩ, 5%, 1/4 watt, carbon composition	C2	0.1 μF, ceramic
R4	50Ω, 5%, 1/4 watt, carbon composition	C4	0.1 μF, ceramic
R5	200Ω, 5%, 1/4 watt, carbon composition	C5	0.1 μF, ceramic
R6	75Ω, 5%, 1/4 watt, carbon composition	C6	10 μF/6V, electrolytic
R7	330Ω, 5%, 1/4 watt, carbon composition	C7	0.1 μF, ceramic
R8	680 kΩ, 5%, 1/4 watt, carbon composition	C8	0.1 μF, ceramic
R9	10 kΩ, trim pot, helitrim model 91	C9	0.1 μF, ceramic
R10	5.1 kΩ, 5%, 1/4 watt, carbon composition	C10	0.1 μF, ceramic
R11	43 kΩ, 5%, 1/4 watt, carbon composition	C11	0.1 μF, ceramic
R12	12 kΩ, 5%, 1/4 watt, carbon composition	C12	0.1 μF, ceramic
R13	10 kΩ, trim pot, helitrim model 91	C13	100 μF/15V, electrolytic
R14	2 kΩ, 5%, 1/4 watt, carbon composition	C14	0.001 μF, mica
R15	200Ω, 5%, 1/4 watt, carbon composition	C15	0.1 μF, ceramic
IC1	LM1201		
IC2	LM1881		

Physical Dimensions inches (millimeters)



16-Lead (0.1500″ Wide) Small Outline Molded Package (M)
Order Number LM1201M
NS Package Number M16A

Physical Dimensions inches (millimeters) (Continued)



16-Lead Molded Dual-In-Line Package (N)
Order Number LM1201N
NS Package Number N16E

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April 1, 1992

National Semiconductor

Preliminary : Information contained in this data sheet is preliminary and is subject to change without notice.

LM1202 230MHz Video Amplifier System

General Description

The LM1202 is a very high frequency video amplifier system intended for use in high resolution monochrome or RGB color monitor applications. In addition to the wideband video amplifier the LM1202 contains a gated differential input black level clamp comparator for brightness control, a DC controlled attenuator for contrast control and a DC controlled sub contrast attenuator for drive control. The DC control for the contrast attenuator is pinned out separately to provide a more accurate control system for RGB color monitor applications. All DC controls offer a high input impedance and operate over a 0 to 4 volt range for easy interface to buss controlled alignment systems. The LM1202 operates from a nominal 12 volt supply but can be operated with supply voltages down to 10 volts for applications that require reduced IC package power dissipation characteristics. The LM1202 is packaged in a 20 lead DIP with special emphasis placed on pin positions for the video input/output, supply and ground connections.

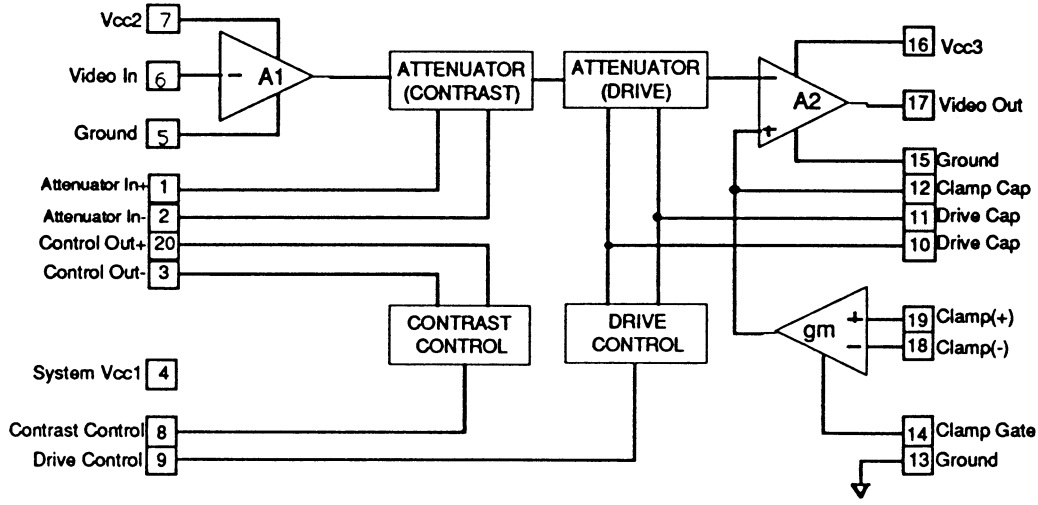
Features

- Wideband video amplifier (f_{-3dB} = 230 MHz at $V_o = 4V_{pp}$)
- t_r, t_f = 1.5 ns at V_o = 4 Vpp
- Externally gated comparator for brightness control
- 0 to 4 volt high input impedance DC contrast control (>40dB range)
- 0 to 4 volt high input impedance DC drive control (±3dB range)
- Easy to parallel three LM1202s for optimum color tracking in RGB systems
- Output stage clamps to 0.5v (min) and provides up to 8 volts output voltage swing
- Output stage directly drives most hybrid or discrete CRT amplifier stages

Applications

High resolution CRT monitors
Video switches
Video AGC amplifier
Wideband amplifier with gain and dc offset control

Block Diagram and Connection Diagram



Ordering Information Order number LM1202N
See NS package Number N20A

Absolute Maximum Ratings (Note 1)

Supply Voltage Vcc Pins 4,7,16 to Ground Pins 5,13,15	13.5V
Voltage at any input Pin (V_{in})	$V_{CC} \geq V_{IN} \geq GND$
Video Output Current (I_{17})	28mA
Package Power Dissipation at T_A = 25°C	1.56W
(Above 25°C derate based on θ_{ja} and T_j)	
Package Thermal Resistance (θ_{ja}) N20A	TBD°C/W
Junction Temperature (T_j)	TBD°C/W
Operating Temperature Range (T_A)	150°C
Storage Temperature Range (T_{stg})	0°C to +70°C
Lead Temperature (Soldering, 10 Seconds)	-65°C to +150°C
ESD Susceptibility	265°C
Human Body Model: 100pF Discharged Through a 1.5 KΩ Resistor	TBD

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Electrical Characteristics See Test Circuit (Figure 1), T_A = 25°C, V4 = V7 = V16 = 12V

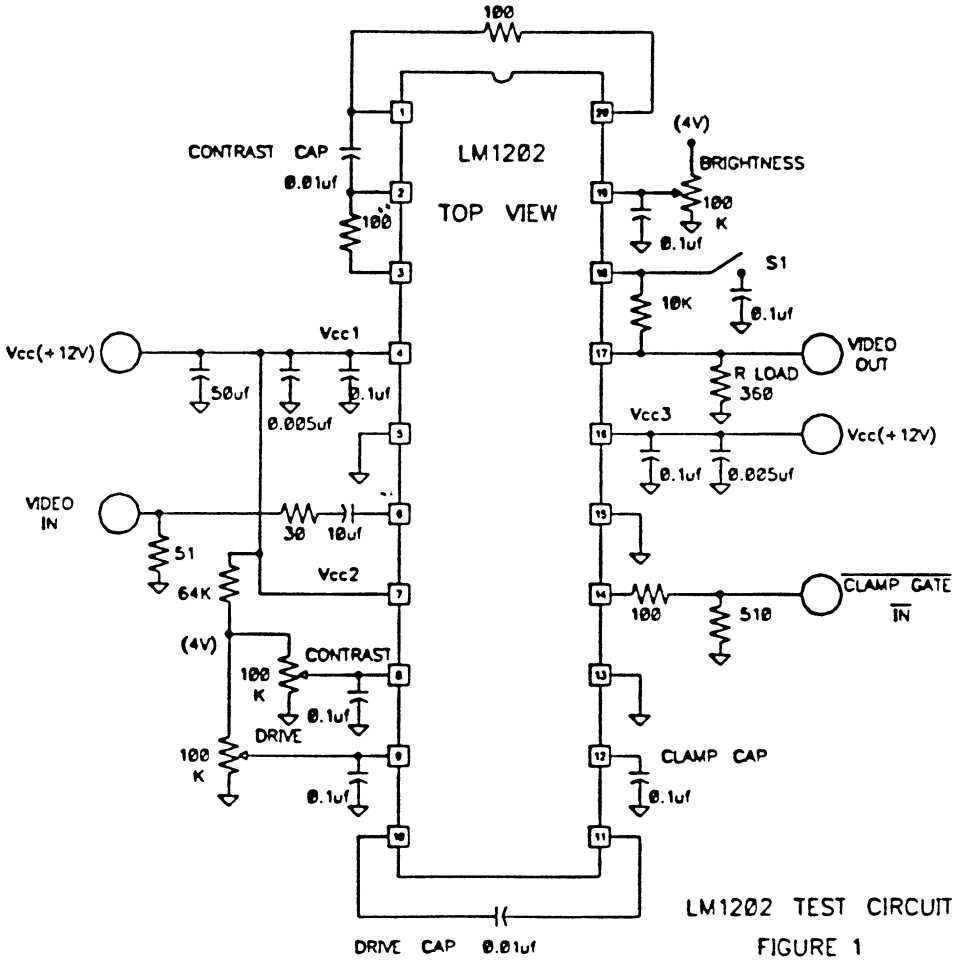
DC Static Test S1 Open, V_{19} = 4V, V_8 = 4V, V_9 = 4V, V_{14} = 0V unless otherwise noted.

Symbol	Parameter	Conditions	LM 1202			Units
			Typical (Note 2)	Tested Limit (Note 3)		
$I_{S\ 4,7,16}$	Supply Current (Total)	$R_{Load} = \infty$	47			mA(max)
V_6	Video Input Voltage		2.6			V(min)
V_{14L}	Clamp Gate Low Input Voltage	Clamp Comparator On	1.2			V(min)
V_{14H}	Clamp Gate High Input Voltage	Clamp Comparator Off	1.6			V(max)
I_{14L}	Clamp Gate Low Input Current	V_{14} = 0V	-0.5			μA(max)
I_{14H}	Clamp Gate High Input Current	V_{14} = 12V	0.005			μA(max)
I_{12+}	Clamp Cap Charge Current	V_{12} = 0V	800			μA
I_{12-}	Clamp Cap Discharge Current	V_{12} = 5V	-800			μA
V_{17L}	Video Output Low Voltage	V_{12} = 0V	0.1			V(max)
V_{17H}	Video Output High Voltage	V_{12} = 6V	9.7			V(max)
V_{OS}	Comparator Input Offset Voltage	$V_{18} - V_{19}$	±0.5	±25		mV(max)

AC Dynamic Test S_1 Closed, V_{14} = 0V, V_{19} = 4V

R_{IN}	Video Amplifier Input Resis.		20kΩ			
Av max	Video Amplifier Gain	V_8 = 4V, V_9 = 4V	20			V/V(min)
ΔAv 2V	Attenuation @ 2V	Ref: Av max, V_8 = 4V	-6			dB
ΔAv 0.5V	Attenuation @ 0.5V	Ref: Av max, V_8 = 2V	-28			dB
ΔDrive	ΔGain Range	V_9 = 0 to 4V	±3			dB
THD	Video Amplifier (Distortion)	V_O = 1 Vp-p	0.33			%
f(-3dB)	Video Amplifier Bandwidth	V_4 = 12V, V_O = 4 Vp-p	230			MHz(min)
t_r	Output Rise Time (Note 3)	V_O = 4 V_{p-p}	1.5			ns
t_f	Output Fall Time (Note 3)	V_O = 4 V_{p-p}	1.5			ns

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.
Note 2: Typical specifications are specified at + 25°C and represent the most likely parametric norm.
Note 3: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).



LM1202 TEST CIRCUIT

FIGURE 1

Circuit Description

Figure.2 shows a block diagram of the LM1202 video amplifier along with contrast and brightness (black level) control. Contrast control is a dc - operated attenuator which varies the ac gain of the amplifier. Signal attenuation (contrast) is achieved by varying the base drive to a differential pair and thereby unbalancing the current through the differential pair. As shown in Figure.2, pin 20 provides a 5.3V bias voltage for the positive input of the attenuator (pin 1). Pin 3 provides a control voltage for the negative input (pin 2) of the attenuator. The voltage at pin 3 varies as the voltage at the contrast control input (pin 8) varies thus providing signal attenuation. The gain is maximum (0 dB attenuation) if the voltage at pin 8 is 4 V and is minimum (maximum attenuation) if the voltage at pin 8 is 0V. The 0 to 4V dc - operated drive control at pin 9 provides a 6 dB gain adjustment range. This feature is necessary for RGB applications where independant adjustment of each channel is required.

The brightness or black level clamping requires a " sample and hold " circuit which holds the dc bias of the video amplifier constant during the black level reference portion of the video waveform. Black level clamping, often referred to as dc restoration is accomplished by applying a back porch clamp signal to the clamp gate input pin (pin 14). The clamp comparator is enabled when the clamp signal goes low during the black level reference period (see Figure. 2). When the clamp comparator is enabled, the clamp capacitor connected to pin 12 is either charged or discharged until the voltage at the minus input of the comparator matches the voltage set at the plus input of the comparator. During the video portion of the signal, the clamp comparator is disabled and the clamp capacitor holds the proper dc bias. In a dc coupled cathode drive application, picture brightness function can be achieved by varying the voltage at the comparator's plus input.

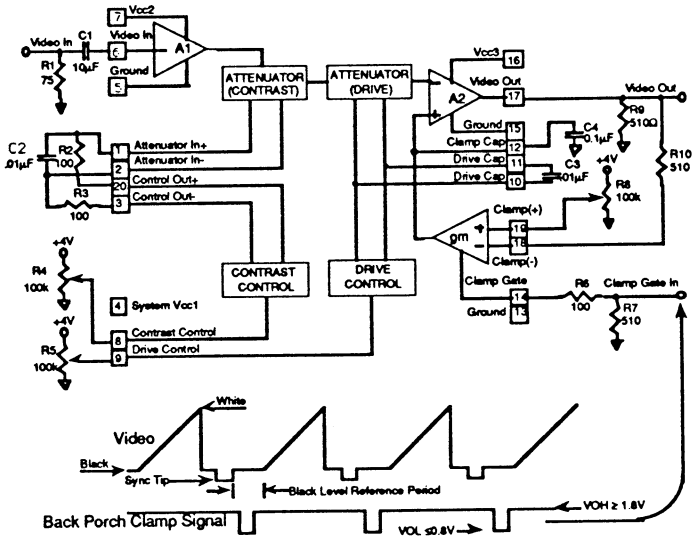


FIGURE 2. Block Diagram of LM1202 Video Amplifier with Contrast and Brightness (black level) control.

Circuit Description (Continued)

Video Amplifier section (Input stage)

A simplified schematic of LM1202's video amplifier input stage is shown in Figure. 3. The 5.4V zener diode, Q1, Q6 and R2 bias the base of Q7 at 2.6 V. The ac coupled video signal applied to pin 6 is referenced to the 2.6 V bias voltage. Transistor Q7 buffers the video signal, Vin, and Q8 converts the voltage to current. The ac collector current through Q8 is I_{c8} = Vin / R9. Under maximum gain condition, transistors Q9 and Q11 are off and all of I_{c8} flows through the load resistors R10 and R11. The maximum signal gain at the base of Q13 is,
A_{v1} = - (R10 + R11) / R9 = -2. Signal attenuation is achieved by varying the base drive to the differential pairs Q9, Q10 and Q11, Q12 thereby unbalancing the collector currents through the transistor pairs. Base of Q10 is biased at 5.3V by externally connecting pin 1 to pin 20 through a 100 Ω resistor. Pin 2 is connected to pin 3 through a 100 Ω resistor. Adjusting the contrast voltage at pin 8 produces a control voltage at pin 3 which drives the base of Q9. By varying the voltage at the base of Q9, Q8's collector current (I_{c8}) is diverted away from the load resistors R10 and R11 thereby providing signal attenuation. Maximum attenuation is achieved when all of I_{c8} flows through Q9 and no current flows through the load resistors.

The differential pair Q11 and Q12 provide drive control. Q12's base is internally biased at 7.3V. Adjusting the voltage at the drive control input (pin 9) produces a control voltage at the base of Q11. With Q9 off and Q12 off, all of I_{c8} flows through R10 thus providing a gain of
A_{v1} = - (R10 / R9) x Vin = - 1. Drive control thus provides a 6 dB attenuation range.

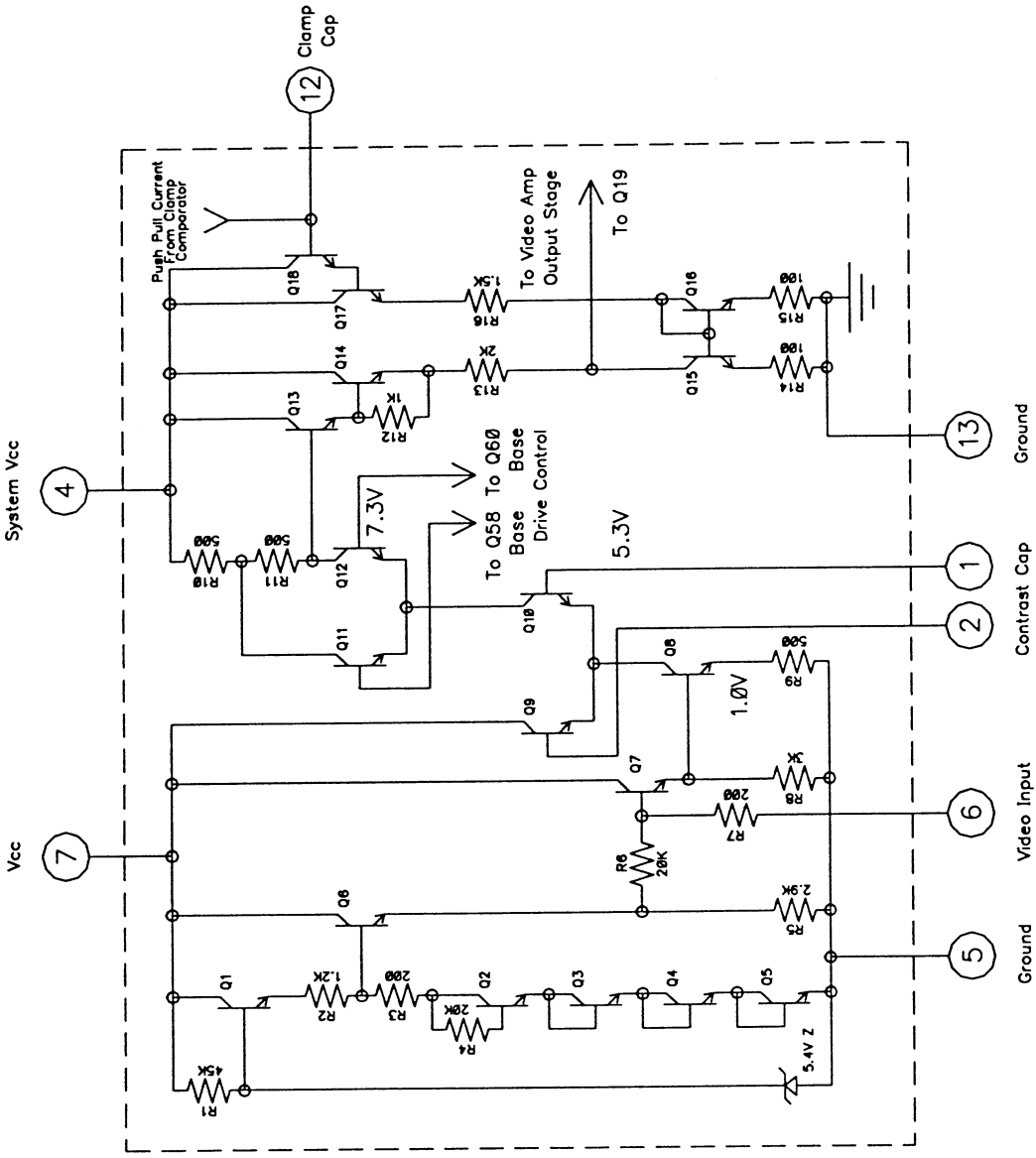


FIGURE 3. Simplified Schematic of LM1202 Video Amplifier Input Stage

Circuit Description (continued)

Video Amplifier section (output stage)

A simplified schematic of LM1202's video amplifier output stage is shown in Figure. 4. The output stage is the second gain stage. Ideally the gain of the second gain stage would be A_{v2} = - R21 / R18 = -16. Because of the output stage's low open loop gain, the gain is approximately A_{v2} = -10. Thus the maximum gain of the video amplifier is Av = A_{v1} x A_{v2} = 20. Transistor Q23 and Q24 provide a push - pull drive to the load. The output voltage can swing from 0.1V to 9.7V.

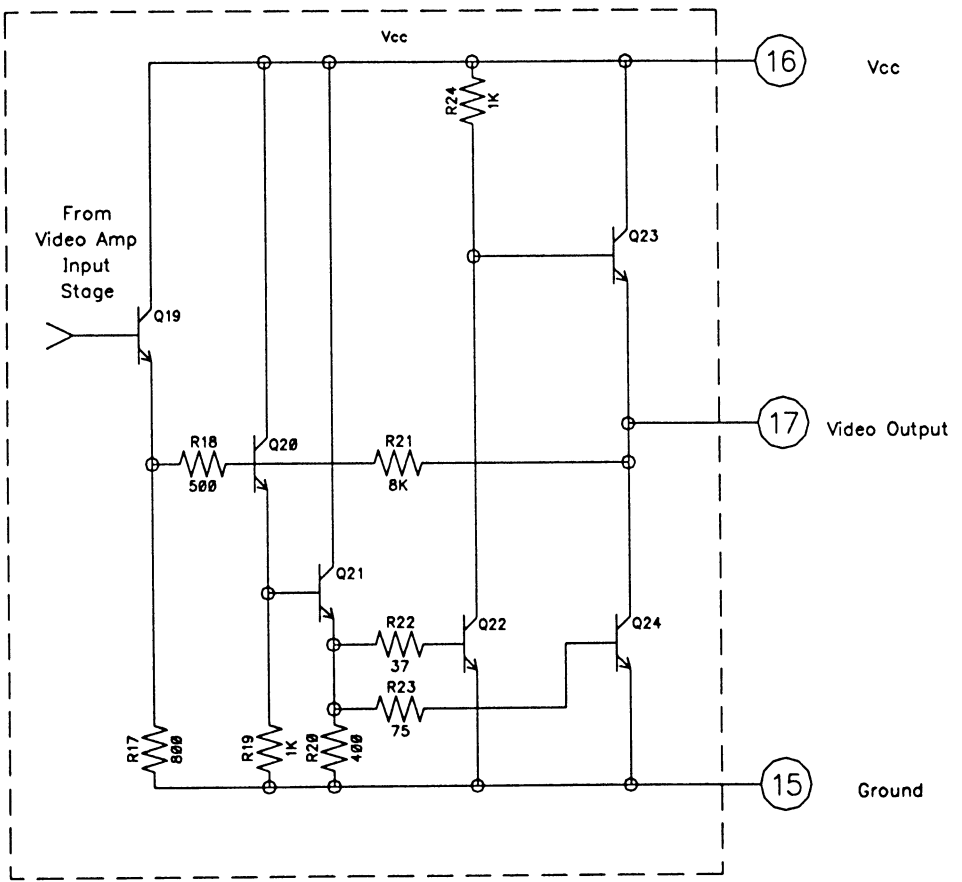


FIGURE 4. Simplified Schematic of LM1202 Video Amplifier Output Stage

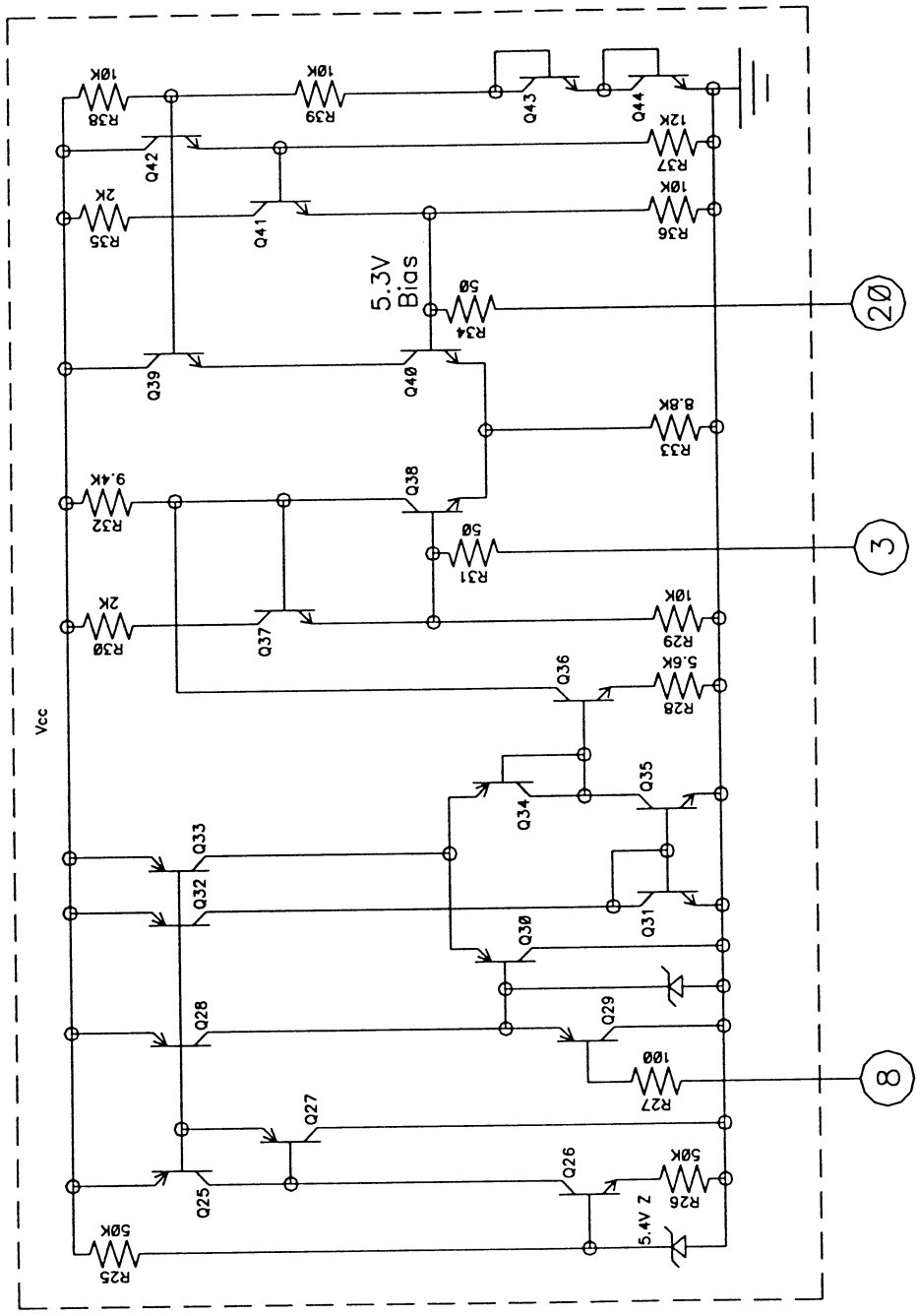
Circuit Description (continued)

Contrast Control section

A simplified schematic of LM1202's contrast control section is shown in Figure.5. A 0 to 4V dc voltage is applied at the contrast input (pin 8). Transistors Q29, Q30 and Q34 buffer and level shift the contrast voltage to the base of Q36. The voltage at the emitter of Q36 equals the contrast voltage, V_{cont} and the current through Q36's collector is given by $I_{C36} = V_{cont} / R28$.

Transistor Q36's collector current is used to unbalance the current through the differential pair comprised of Q38 and Q40. Q40's base is internally biased at 5.3V and made available at pin 20. Pin 20 is externally connected to pin 1 through a 100 Ω resistor (see Figures 2 and 3). The base of Q38 (pin 3) is externally connected to pin 2 through a 100 Ω resistor (see Figures 2 and 3). With V_{cont} = 2V, the differential pair (Q38, Q40) is balanced and the voltage at pins 1 and 2 is 5.3V. Under this conmdition, Q8's collector current is equally split between Q9 qnd Q10 (see Figure. 3) and the amplifier's gain is half the maximum gain. If contrast voltage at pin 8 is greater than 2V then Q36's collector current increases thus pulling Q38's collector node lower and consequently moving Q38's base below 5.3V. With pin 2 at a lower voltage than pin 1, current through Q10 (see Figure. 3) increases and the amplifier's gain increases. With V_{cont} = 4V, the amplifier's gain is maximum.

If the contrast voltage at pin 8 is less than 2V then Q36's collector current decreases and Q38's base is pulled above 5.3V. With pin 2 voltage greater than pin 1 voltage, less current flow through Q10 (see Figure. 3), consequently the amplifier's gain decreases. With V_{cont} = 0V, the amplifier's gain is minimum (i.e maximum attenuation).



Contrast Control Input

FIGURE 5. Simplified Schematic of LM1202 Contrast Control

Circuit Description (continued)

Drive control section

A simplified schematic of LM1202'sdrive control section is shown in Figure.6. A 0 to 4V dc voltage is applied at the drive control input (pin 9). Transistors Q49, Q50 and Q54 buffer and level shift the contrast voltage to the base of Q56. The voltage at the emitter of Q56 equals the drive voltage, V_{drive} and the current through Q56's collector is given by $I_{C56} = V_{drive} / R43$.

Transistor Q56's collector current is used to unbalance the current through the differential pair comprised of Q58 and Q60. Q60's base is internally biased at 7.3V and and connected to the base of Q12 (see Figure. 3). Q58's base is internally connected to the base of Q11 (see Figure. 3). With $V_{cont} = 2V$, the differential pair (Q58, Q60) is balanced and the voltage at the bases of Q11 and Q12 is 7.3V. Under this condition, Q10's collector current is equally split between Q11 and Q12 (see Figure. 3). If contrast voltage at pin 9 is greater than 2V then Q56's collector current increases thus pulling Q58's collector node lower and consequently moving Q58's base below 7.3V. With base of Q11 below 7.3V, current through Q12 (see Figure. 3) increases and the amplifier's gain increases. With $V_{drive} = 4V$, the amplifier's gain is maximum under maximum contrast condition (i.e $V_{cont} = 4V$).

If the drive voltage at pin 8 is less than 2V then 56's collector current decreases and Q58's base is pulled above 7.3V. With base of Q11 greater than 7.3V, less current flow through Q12 (see Figure. 3), consequently the amplifier's gain decreases. With $V_{drive} = 0V$, the amplifier's gain is 6 dB less than the maximum gain.

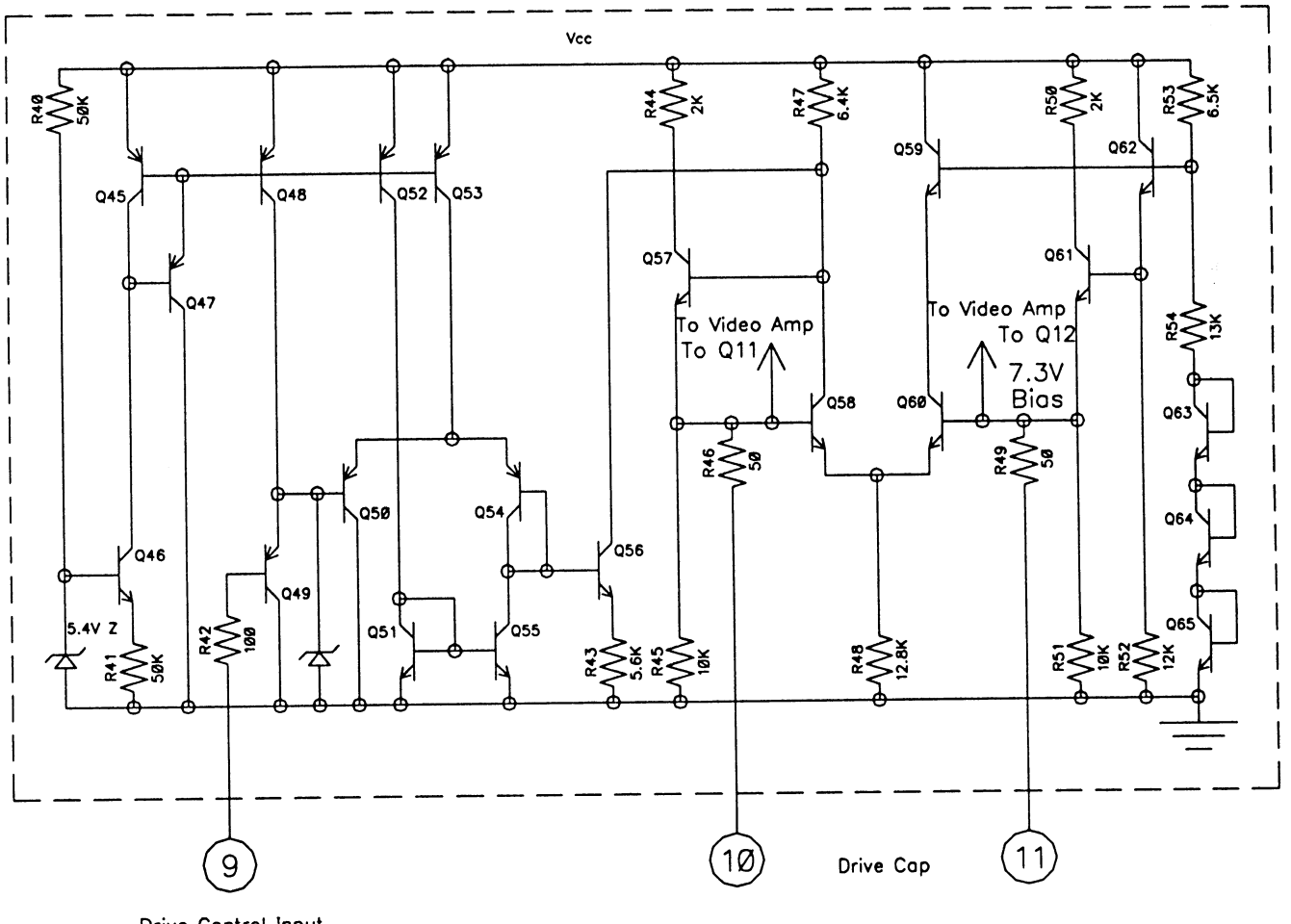


FIGURE 6. Simplified Schematic of LM1202 Drive Control

Circuit Description (continued)
Clamp gate and clamp comparator section

Figures 7 and 8 show simplified schematics of the clamp gate and clamp comparator circuits. The clamp gate circuit (Figure 7) consists of a PNP input buffer transistor (Q82), a PNP emitter coupled pair (Q85 and Q86) referenced on one side to 2.1V and an output switch transistor Q89. When the clamp gate input at pin 14 is high (> 1.5V) the Q89 switch is on and shunts the 200 μA current from current source Q90 to ground. When pin 14 is low (< 1.3V) the Q89 switch is off and the 200 μA current is mirrored by the current mirror comprised of Q91 and Q75 (see Figure 8). Consequently the clamp comparator comprised of the differential pair Q74 and Q77 is enabled. The input of the clamp comparator is similar to the clamp gate except that an NPN emitter coupled pair is used to control the current that will charge or discharge the clamp capacitor externally connected from pin 12 to ground. PNP transistors are used at the inputs because they offer a number of advantages over NPNs. PNPs will operate with base voltages at or near ground and will usually have a greater emitter base breakdown voltage (BVebo). Because the differential input voltage to the clamp comparator during the video scan period could be greater than the BVebo of NPN transistors a resistor (R63) with a value one half that of R60 or R68 is connected between the bases of Q71 and Q79. The clamp comparator's common mode range is from ground to approximately 9V and the maximum differential input voltage is Vcc and ground.

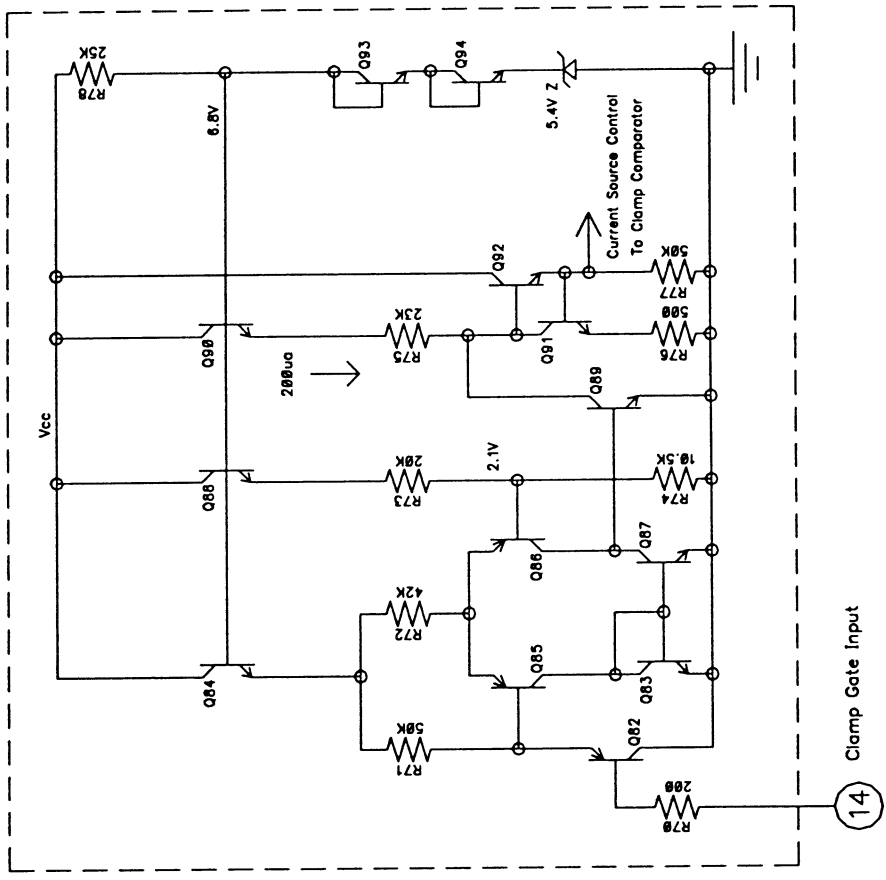


FIGURE 7. Simplified Schematic of LM1202 Clamp Gate Circuit

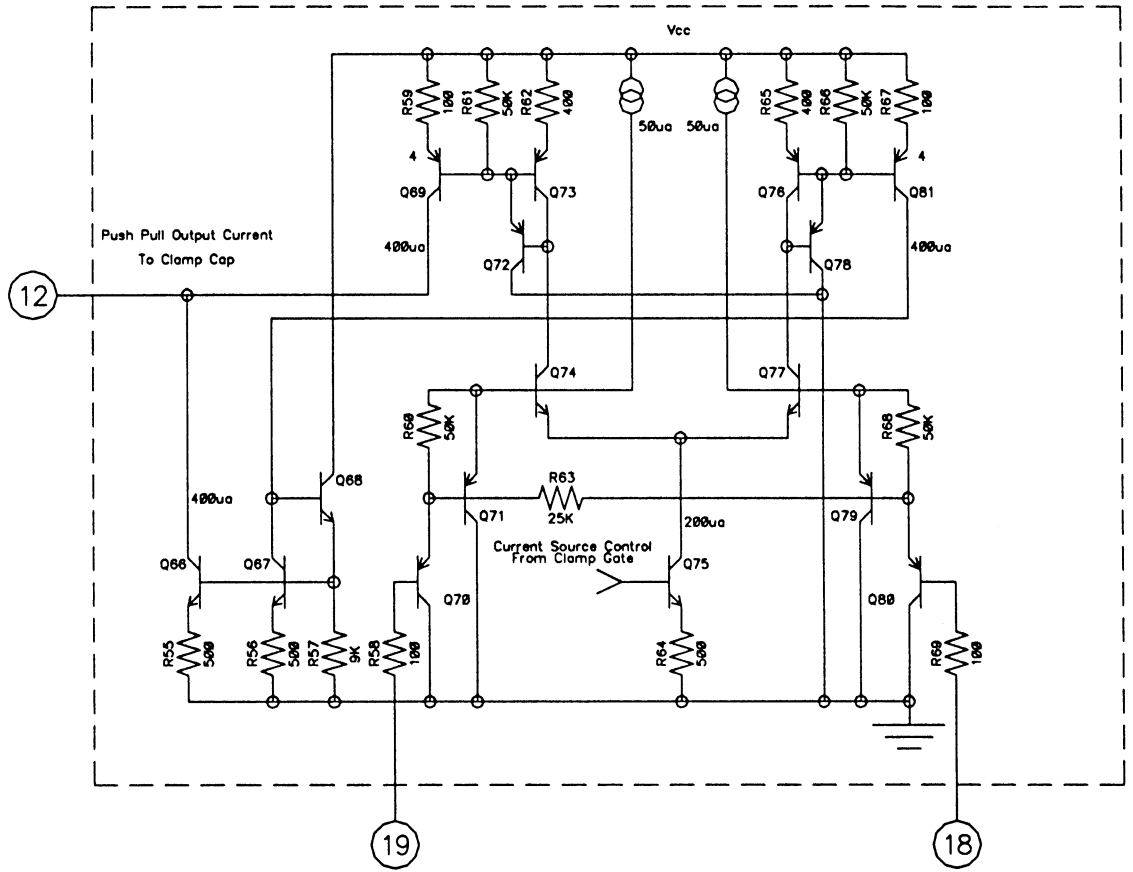


FIGURE 8. Simplified Schematic of LM1202 Clamp Comparator Circuit

Applications of LM1202

Single video channel

A typical application for a single video channel is shown in Figure.9. The video signal is ac coupled to pin 6. The LM1202 internally biases the video signal to 2.6 V_{DC}. Contrast control is achieved by applying a 0 to 4V dc voltage at pin 8. The amplifier's gain is minimum (i.e maximum signal attenuation) if pin 8 is at 0V and is maximum if pin 8 is at 4V. With pin 9 (drive control at 0 V, the amplifier has a maximum gain of 20 dB.

For dc restoration, a clamp signal must be applied to the clamp gate input (pin 14). The clamp signal should be logic low (less than 0.8 V) only during the back porch (black level reference period) interval. The clamp gate input is TTL compatible. Brightness control is provided by applying a 0 V to 4 V dc voltage at pin 19. For example, if pin 19 is biased at 1 V then the video signal's black level will be clamped at 1 V. A 510 Ω load resistor is connected from the video output pin (pin 17) to ground. This resistor biases the Class A output stage of the amplifier. For power dissipation considerations, the load resistor should not be much less than 510 Ω.

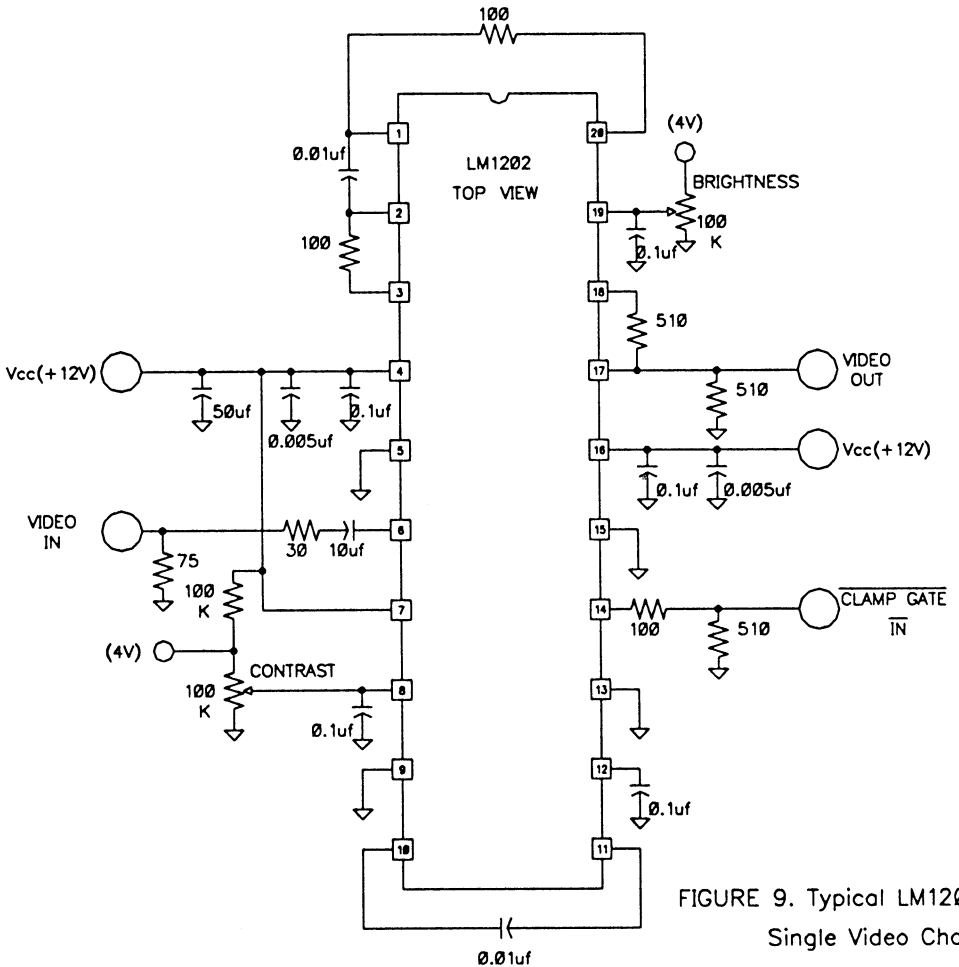


FIGURE 9. Typical LM1202 Application
Single Video Channel

Applications of LM1202 (continued)

RGB video preamplifier

Figure.10 shows an RGB video preamplifier circuit using three LM1202s. Note that pins 1 and 2 of IC1 are connected to pins 1 and 2 of IC2 and IC3 respectively. This allows IC1 to provide a master contrast control and optimum contrast tracking. Adjusting the contrast voltage at pin 8 of IC1 will vary the gain of all three video channels. Drive control input (pin 9) of each LM1202 allows individual gain adjustment for achieving white balance.

The black level of each video channel can be individually adjusted to the desired voltage by adjusting the voltage at pin 19. In a dc coupled cathode drive application, adjusting the voltage at pin 19 of each IC will provide cutoff adjustment. In an ac coupled cathode drive application, the video signal is ac coupled and dc restored at the cathode. In such an application, the video signal's black level may be clamped to the desired level by simply biasing pin 19 to that voltage by using a voltage divider at pin 19.

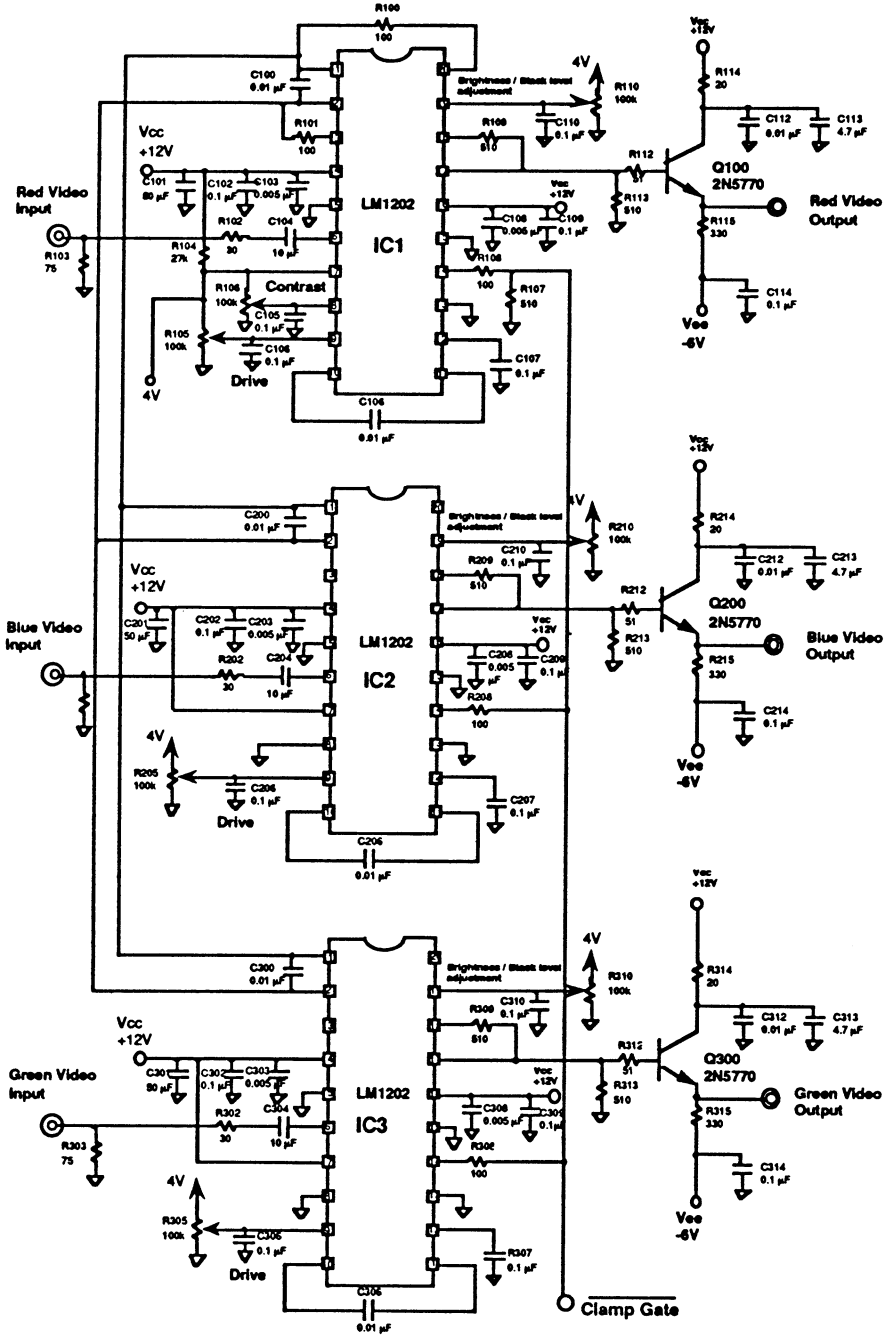


Figure.10 Typical RGB application with contrast, drive and black level (cutoff) control.

National Semiconductor

November 1988

LM1203 RGB Video Amplifier System

General Description

The LM1203 is a wideband video amplifier system intended for high resolution RGB color monitor applications. In addition to three matched video amplifiers, the LM1203 contains three gated differential input black level clamp comparators for brightness control and three matched attenuator circuits for contrast control. Each video amplifier contains a gain set or "Drive" node for setting maximum system gain (Av = 4 to 10) as well as providing trim capability. The LM1203 also contains a voltage reference for the video inputs. For high resolution monochrome monitor applications see the LM1201 Video Amplifier System datasheet.

Features

- Three wideband video amplifiers (70 MHz @ −3dB)
- Inherently matched (±0.1 dB or 1.2%) attenuators for contrast control
- Three externally gated comparators for brightness control
- Provisions for independent gain control (Drive) of each video amplifier
- Video input voltage reference
- Low impedance output driver

Block and Connection Diagram

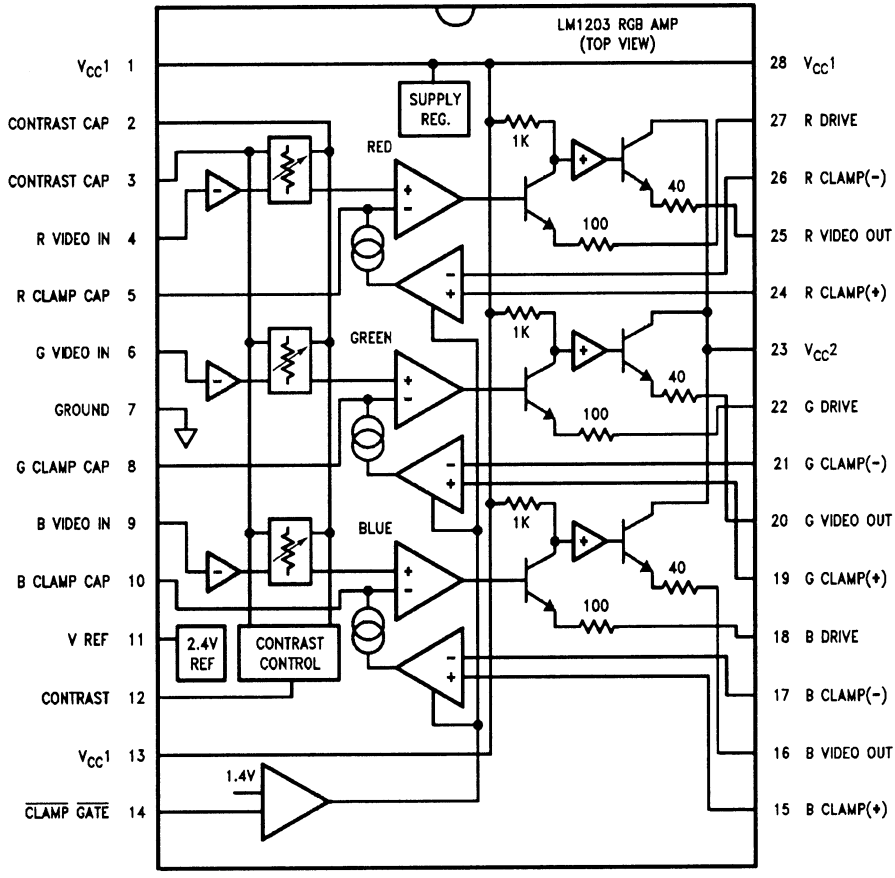


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FIGURE 1
Order Number LM1203N
See NS Package Number N28B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC} Pins 1, 13, 23, 28 (Note 1) 13.5V

Voltage at Any Input Pin, V_{IN} $V_{CC} \geq V_{IN} \geq$ GND

Video Output Current, I16, 20 or 25 28 mA

Power Dissipation, P_D 2.5W

(Above 25°C) Derate Based on θ_{JA} and T_J

Thermal Resistance, θ_{JA} 50°C/W

Junction Temperature, T_J 150°C

Operating Temperature Range, T_A 0°C to +70°C

Storage Temperature Range, T_{STG} −65°C to +150°C

Lead Temperature, (Soldering, 10 sec.) 265°C

ESD susceptibility 2 kV

Human body model: 100 pF discharged through a 1.5 kΩ resistor

Electrical Characteristics See Test Circuit *(Figure 2)*, T_A = 25°C; $V_{CC1} = V_{CC2}$ = 12V

DC Static Tests S17, 21, 26 Open; V12 = 6V; V14 = 0V; V15 = 2.0V unless otherwise stated

Label	Parameter	Conditions	Typ	Tested Limit (Note 2)	Design Limit (Note 3)	Units (Limits)
Is	Supply Current	V_{CC} 1 only	73	90.0		mA(max)
V11	Video Input Reference Voltage		2.4	2.2		V(min)
				2.6		V(max)
Ib	Video Input Bias Current	Any One Amplifier	5.0	20		µA(max)
V14 l	Clamp Gate Low Input Voltage	Clamp Comparators On	1.2	0.8		V(min)
V14 h	Clamp Gate High Input Voltage	Clamp Comparators Off	1.6	2.0		V(max)
I14 l	Clamp Gate Low Input Current	V14 = 0V	−0.5	−5.0		µA(max)
I14 h	Clamp Gate High Input Current	V14 = 12V	0.005	1		µA(max)
Iclamp+	Clamp Cap Charge Current	V5, 8 or 10 = 0V	850	500		µA(min)
Iclamp−	Clamp Cap Discharge Current	V5, 8 or 10 = 5V	−850	−500		µA(min)
Vol	Video Output Low Voltage	V5, 8 or 10 = 0V	0.9	1.25		V(max)
Voh	Video Output High Voltage	V5, 8 or 10 = 5V	8.9	8.2		V(min)
ΔVo(2V)	Video Output Offset Voltage	Between Any Two Amplifiers V15 = 2V	±0.5	±50		mV(max)
ΔVo(4V)	Video Output Offset Voltage	Between Any Two Amplifiers V15 = 4V	±0.5	±50		mV(max)

AC Dynamic Tests S17, 21, 26 Closed; V14 = 0V; V15 = 4V; unless otherwise stated

Symbol	Parameter	Conditions	Typ	Tested Limit (Note 2)	Design Limit (Note 3)	Units (Limits)
Av max	Video Amplifier Gain	V12 = 12V, V_{IN} = 560 mVp-p	6.0	4.5		V/V(min)
ΔAv 5V	Attenuation @ 5V	Ref: Av max, V12 = 5V	−10			dB
ΔAv 2V	Attenuation @ 2V	Ref: Av max, V12 = 2V	−40			dB
Av match	Absolute gain match @ Av max	V12 = 12V (Note 5)	±0.5			dB
ΔAv track1	Gain change between amplifiers	V12 = 5V (Notes 5, 8)	±0.1		±0.5	dB(max)
ΔAv track2	Gain change between amplifiers	V12 = 2V (Notes 5, 8)	±0.3		±0.7	dB(max)
THD	Video Amplifier Distortion	V12 = 3V, V_O = 1 Vp-p	0.5			%
f(−3 dB)	Video Amplifier Bandwidth (Notes 4, 6)	V12 = 12V, V_O = 100 mV_{rms}	70			MHz
t_r	Output Rise Time (Note 4)	V_O = 4 Vp-p	5			ns
t_f	Output Fall Time (Note 4)	V_O = 4 Vp-p	7			ns

AC Dynamic Tests S17, 21, 26 Closed; V14 = 0V; V15 = 4V; unless otherwise stated (Continued)

Symbol	Parameter	Conditions	Typ	Tested Limit (Note 2)	Design Limit (Note 3)	Units
Vsep 10 kHz	Video Amplifier 10 kHz Isolation	V12 = 12V (Note 7)	−65			dB
Vsep 10 MHz	Video Amplifier 10 MHz Isolation	V12 = 12V (Notes 4, 7)	−46			dB

Note 1: V_{CC} supply pins 1, 13, 23, 28 must be externally wired together to prevent internal damage during V_{CC} power on/off cycles.

Note 2: These parameters are guaranteed and 100% production tested.

Note 3: Design limits are guaranteed (but not 100% production tested). These limits are not used to calculate outgoing quality levels.

Note 4: When measuring video amplifier bandwidth or pulse rise and fall times, a double sided full ground plane printed circuit board without socket is recommended. Video Amplifier 10 MHz isolation test also requires this printed circuit board.

Note 5: Measure gain difference between any two amplifiers. V_{IN} = 1 Vp-p.

Note 6: Adjust input frequency from 10 kHz (Av_{max} ref level) to the −3 dB corner frequency (f −3 dB).

Note 7: Measure output levels of the other two undriven amplifiers relative to driven amplifier to determine channel separation. Terminate the undriven amplifier inputs to simulate generator loading. Repeat test at f_{IN} = 10 MHz for Vsep = 10 MHz.

Note 8: ΔAv track is a measure of the ability of any two amplifiers to track each other and quantifies the matching of the three attenuators. It is the difference in gain change between any two amplifiers with the Contrast Voltage V12 at either 5V or 2V measured relative to an Av max condition V12 = 12V. For example, at Av max the three amplifiers gains might be 17.4 dB, 16.9 dB, and 16.4 dB and change to 7.3 dB, 6.9 dB, and 6.5 dB respectively for V12 = 5V. This yields the measured typical ±0.1 dB channel tracking.

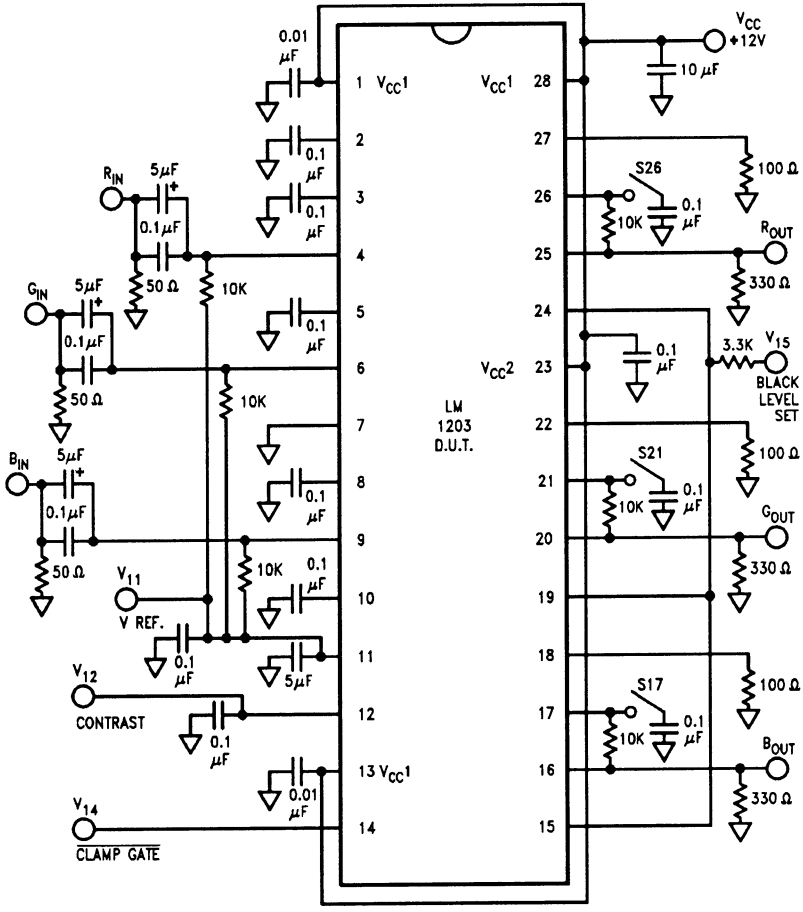

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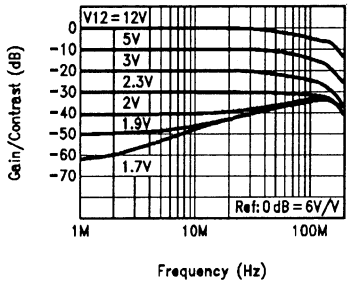
FIGURE 2. LM1203 Test Circuit

Typical Performance Characteristics

Contrast vs Frequency



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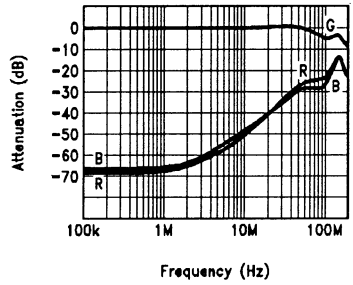
Crosstalk vs Frequency



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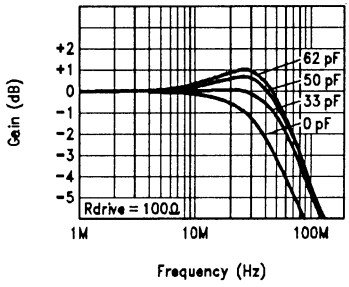
Frequency Response Using Various Peaking Caps



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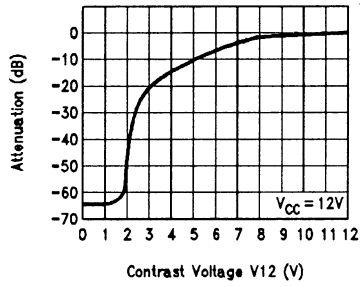
Attenuation vs Contrast Voltage



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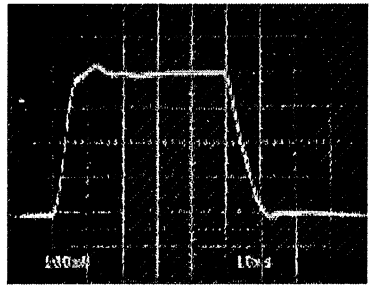
Pulse Response



Rise & Fall Times
Vert. = 1V/Div.
Horiz. = 10 ns/Div.

– – GND

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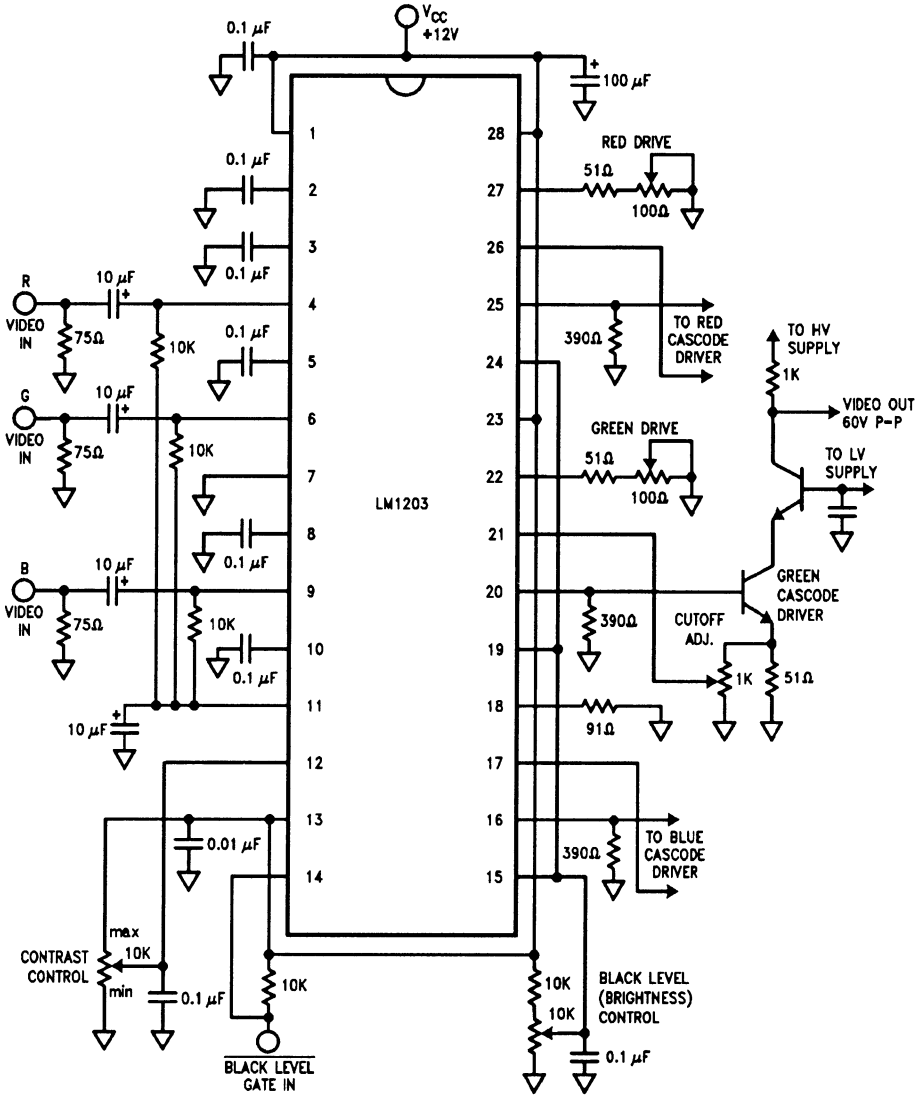

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FIGURE 3. LM1203 Typical Application

Applications Information

Figure 4 shows the block diagram of a typical analog RGB color monitor. The RGB monitor is used with CAD/CAM work stations, PC's, arcade games and in a wide range of other applications that benefit from the use of color display terminals. The RGB color monitor characteristics may differ in such ways as sweep rates, screen size, CRT color trio spacing (dot pitch), or in video amplifier bandwidths but will still be generally configured as shown in *Figure 4*. Separate horizontal and vertical sync signals may be required or they may be contained in the green video input signal. The video input signals are usually supplied by coax cable which is terminated in 75Ω at the monitor input and internally ac coupled to the video amplifiers. These input signals are approximately 1 volt peak to peak in amplitude and at the input of the high voltage video section, approximately 6V peak to peak. At the cathode of the CRT the video signals can be as high as 60V peak to peak. One important requirement of the three video amplifiers is that they match and track each other over the contrast and brightness control range. The *Figure 4* block labeled "VIDEO AMPLIFICATION WITH GAIN AND DC CONTROL" describes the function of the LM1203 which contains the three matched video amplifiers, contrast control and brightness control.

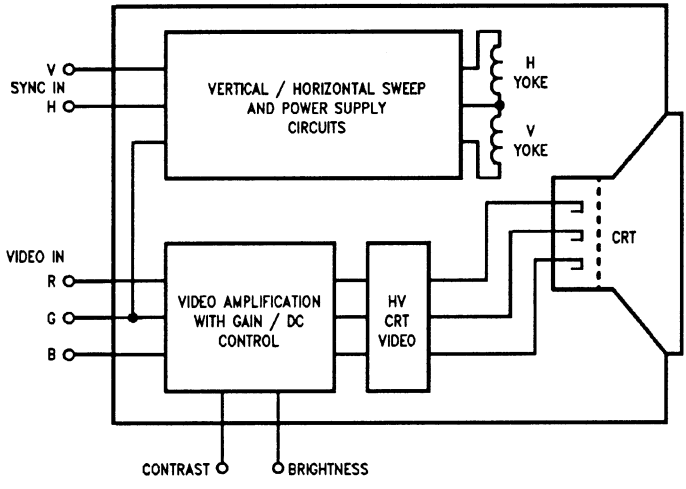

FIGURE 4. Typical RGB Color Monitor Block Diagram

Circuit Description

Figure 5 is a block diagram of one of the video amplifiers along with the contrast and brightness controls. The contrast control is a dc-operated attenuator which varies the ac gain of all three amplifiers simultaneously while not introducing any signal distortions or tracking errors. The brightness control function requires a "sample and hold" circuit (black level clamp) which holds the dc bias of the video amplifiers and CRT cathodes constant during the black level reference portion of the video waveform. The clamp comparator, when gated on during this reference period, will charge or discharge the clamp capacitor until the plus input of the clamp comparator matches that of the minus input voltage which was set by the brightness control.

Figure 6 is a simplified schematic of one of the three video amplifiers along with the recommended external components. The IC pin numbers are circled with all external components shown outside of the dashed line. The video input is applied to pin 6 via the 10 μF coupling capacitor. DC bias to the video input is through the 10 kΩ resistor which is connected to the 2.4V reference at pin 11. The low frequency roll-off of the amplifier is set by these two components. Transistor Q1 buffers the video signal to the base of Q2. The Q2 collector current is then directed to the V_{CC} 1 supply directly or through the 1k load resistor depending upon the differential DC voltage at the bases of Q3 and Q4. The Q3 and Q4 differential base voltage is determined by the contrast control circuit which is described below. RF decoupling capacitors are required at pins 2 and 3 to insure high frequency isolation between the three video amplifiers which share these common connections. The black level dc voltage at the collector of Q4 is maintained by Q5 and Q6 which are part of the black level clamp circuit also described below. The video signal appearing at the collector of Q4 is then buffered by Q7 and level shifted down by Z1 and Q8 to the base of Q9 which will then provide additional system gain.

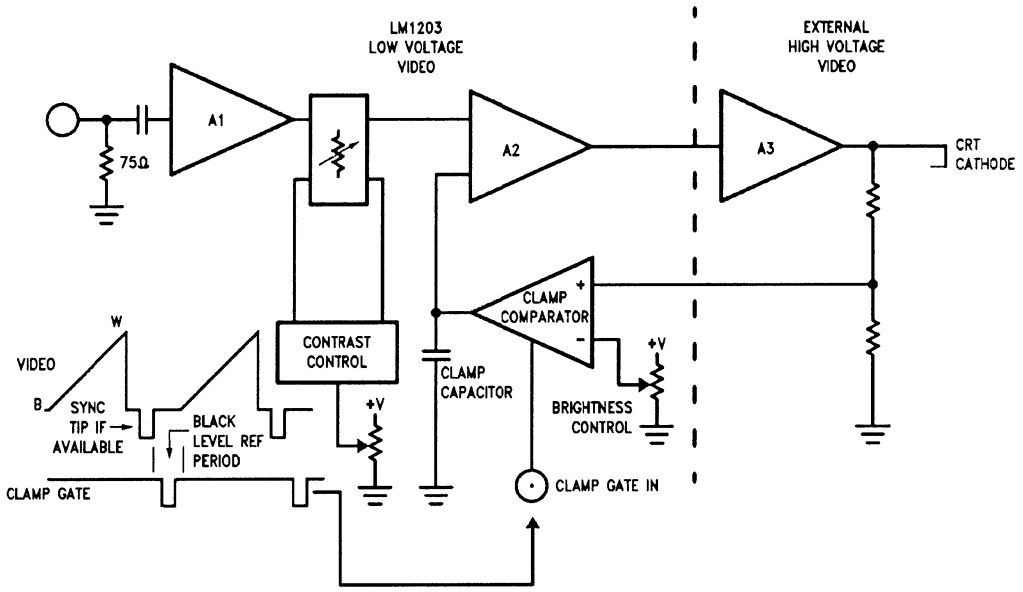

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FIGURE 5. Block Diagram of LM1203 Video Amplifier with Contrast and Black Level Control

Circuit Description (Continued)

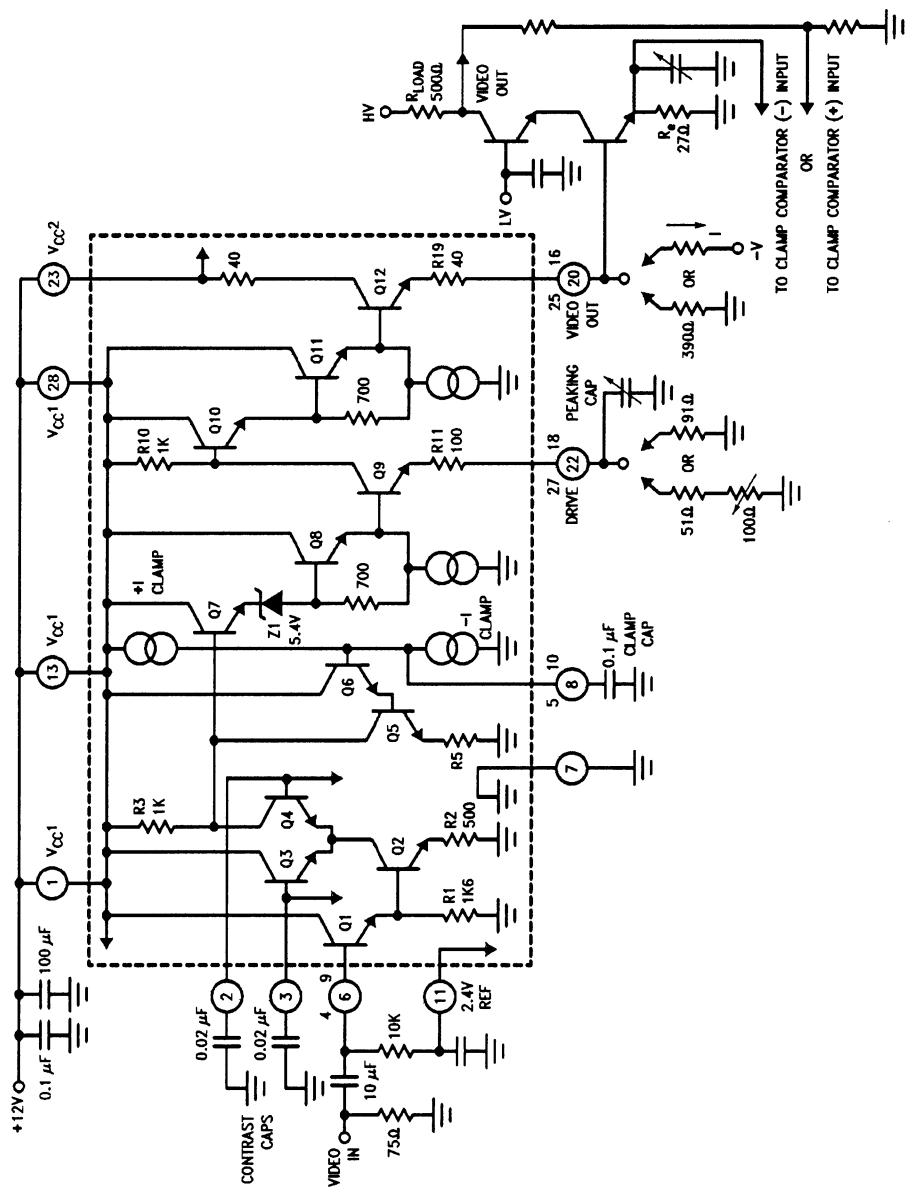

FIGURE 6. Simplified LM1203 Video Amplifier Section with Recommended External Components

Circuit Description (Continued)

The "Drive" pin will allow the user to trim the Q9 gain of each amplifier to correct for differences in the CRT and high voltage cathode driver gain stages. A small capacitor (33 pF) at this pin will extend the high frequency gain of the video amplifier by compensating for some of the internal high frequency roll off. To use this capacitor and still provide variable gain adjustment, the 51Ω and series 100Ω pot should be used with the red and green drive pins. The 91Ω resistor used with the blue drive pin will set the system gain to approximately 6.2 and allow adjustment of the red and green gains to 6.2 plus or minus 25%. The video signal at the collector of Q9 is buffered and level shifted down by Q10 and Q11 to the base of the output emitter follower Q12. Between the emitter of Q12 and the video output pin is a 40Ω resistor which was included to prevent spurious oscillations when driving capacitive loads. An external emitter resistor must be added between the video output pin and ground. The value of this resistor should not be less than 390Ω or package power limitations may be exceeded when worst case (high supply, max supply current, max temp) calculations are made. If negative going pulse slewing is a problem because of high capacitive loads (>10 pF), a more efficient method of emitter pull down would be to connect a suitable resistor to a negative supply voltage. This has the effect of a current source pull down when the minus supply voltage is −12V and the emitter current is approximately 10 mA. The system gain will also increase slightly because less signal will be lost across the internal 40Ω resistor. Precautions must be taken to prevent the video output pin from going below ground because IC substrate currents may cause erratic operation. The collector currents from the video output transistors are returned to the power supply at V_{CC} 2 pin 23. When making power dissipation calculations note that the data sheet specifies only the V_{CC} 1 supply current at 12V. The IC power dissipation contribution of V_{CC} 2 is dependent upon the video output emitter pull down load.

In applications that require video amplifier shut down because of fault conditions detected by monitor protection circuits, pin 11 and the wiper arms of the contrast and brightness controls can be grounded without harming the IC. This assumes some series resistance between the top of the control pots and V_{CC}.

Figure 7 shows the internal construction of the pin 11 2.4V reference circuit which is used to provide temperature and supply voltage tracking compensation for the video amplifier inputs. The value of the external DC biasing resistors should not be larger than 10 kΩ because minor differences in input bias currents to the individual video amplifiers may cause offsets in gain.

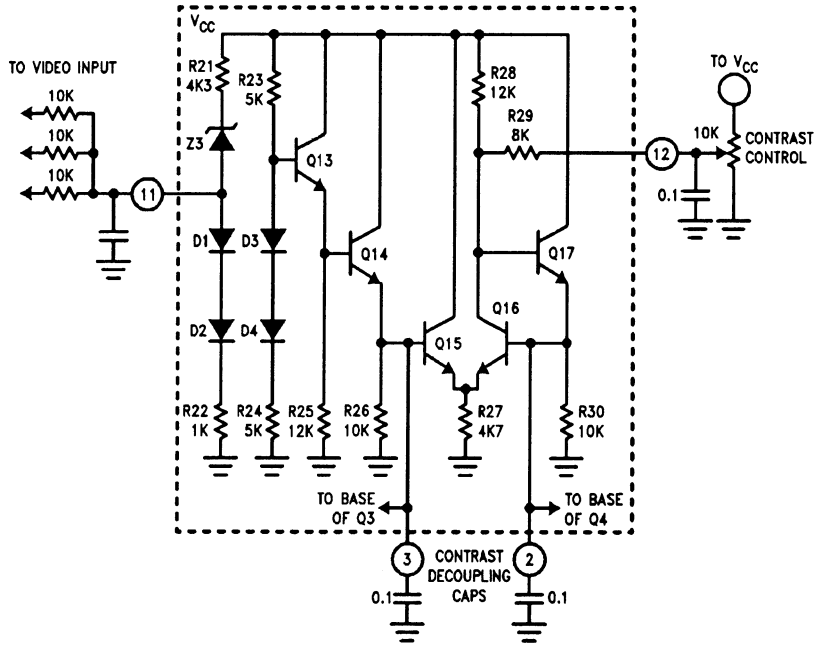

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FIGURE 7. LM1203 Video Input Voltage Reference and Contrast Control Circuits

Circuit Description (Continued)

Figure 7 also shows how the contrast control circuit is configured. Resistors R23, 24, diodes D3, 4 and transistor Q13 are used to establish a low impedance zero TC half supply voltage reference at the base of Q14. The differential amplifier formed by Q15, 16 and feedback transistor Q17 along with resistors R27, 28 establish a diferential base voltage for Q3 and Q4 in *Figure 6*. When externally adding or subtracting current from the collector of Q16, a new differential voltage is generated that reflects the change in the ratio of currents in Q15 and Q16. To provide voltage control of the Q16 current, resistor R29 is added between the Q16 collector and pin 12. A capacitor should be added from pin 12 to ground to prevent noise from the contrast control pot from entering the IC.

Figure 8 is a simplified schematic of the clamp gate and clamp comparator sections of the LM1203. The clamp gate circuit consists of a PNP input buffer transistor (Q18), a PNP emitter coupled pair referenced on one side to 2.1V (Q19, 20) and an output switch (Q21). When the clamp gate input at pin 14 is high (>1.5V) the Q21 switch is on and shunts the I1 850 μA current to ground. When pin 14 is low (<1.3V) the Q21 switch is off and the I1 850 μA current source is mirrored or "turned around" by reference diode D5 and Q26 to provide a 850 μA current source for the clamp comparator(s). The inputs to the comparator are similar to the clamp gate input except that an NPN emitter coupled pair is used to control the current which will charge or discharge the clamp capacitors at pins 5, 8, or 10. PNP transistors are used at the inputs because they offer a number of advantages over NPNs. PNPs will operate with base voltages at or near ground and will usually have a greater reverse emitter base breakdown voltage (BVebo). Because the differential input voltage to the clamp comparator during the video scan period could be greater than the BVebo of NPN transistors a resistor (R34) with a value one half that of R33 or R35 is connected between the bases of Q23 and Q27. This resistor will limit the maximum differential input to Q24, 25 to approximately 350 mV. The clamp comparator common mode range is from ground to approximately 9V and the maximum differential input voltage is V_{CC} and ground.

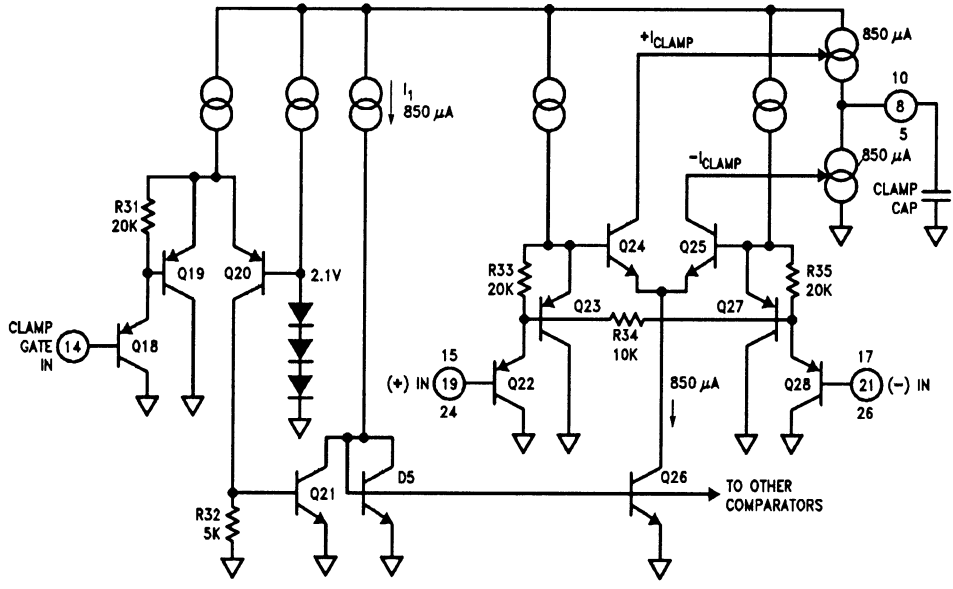

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FIGURE 8. Simplified Schematic of LM1203 Clamp Gate and Clamp Comparator Circuits

Additional Applications of the LM1203

Figure 9 shows how the LM1203 can be set up as a video buffer which could be used in low cost video switcher applications. Pin 14 is tied high to turn off the clamp comparators. The comparator input pins should be grounded as shown. Sync tip (black level if sync is not included) clamping is provided by diodes at the amplifier inputs. Note that the clamp cap pins are tied to the Pin 11 2.4V reference. This was done, along with the choice of 200Ω for the drive pin resistor, to establish an optimum DC output voltage. The contrast control (Pin 12) will provide the necessary gain or attenuation required for channel balancing. Changing the contrast control setting will cause minor DC shifts at the amplifier output which will not be objectionable as the output is AC coupled to the load. The dual NPN/PNP emitter follower will provide a low impedance output drive to the AC coupled 75Ω output impedance setting resistor. The dual 500 µF capacitors will set the low frequency response to approximately 4 Hz.

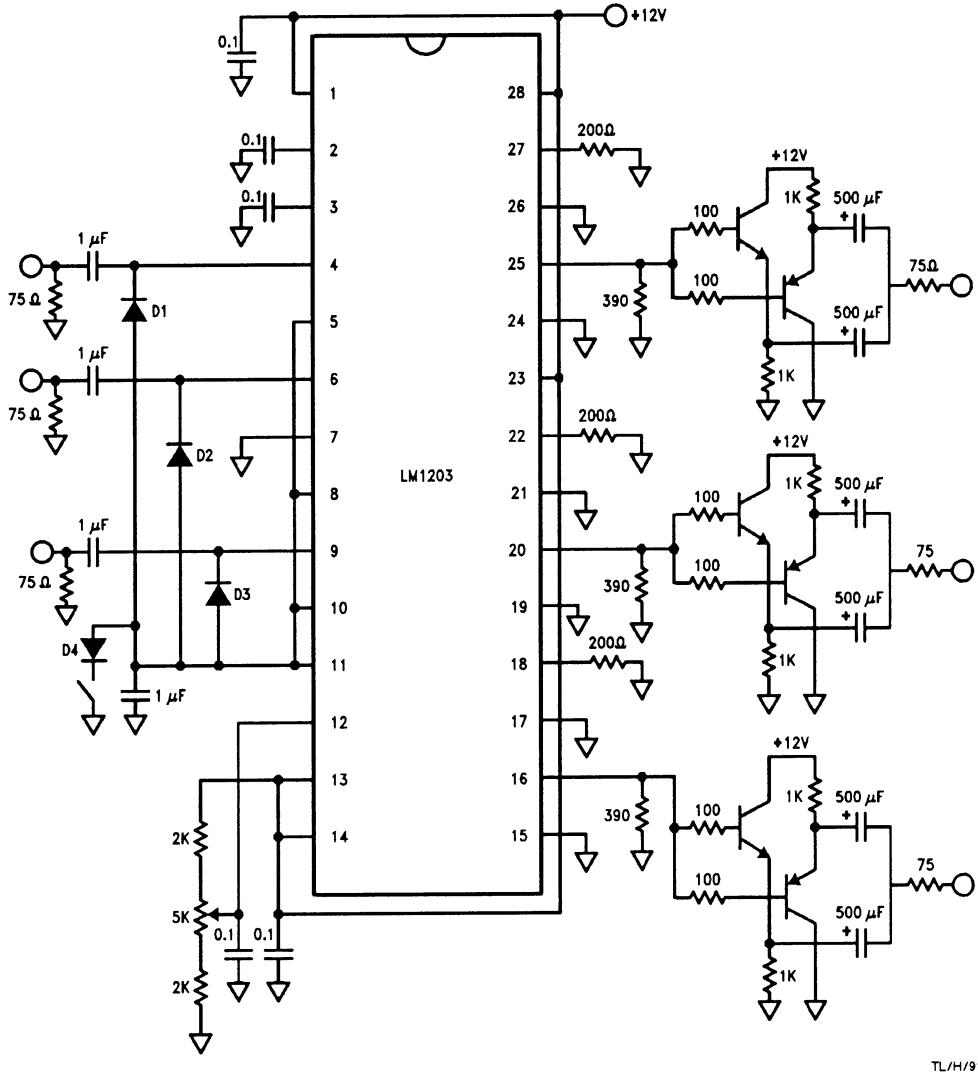

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FIGURE 9. RGB Video Buffer with Diode Sync Tip Clamps and 75Ω Cable Driver

Additional Applications of the LM1203 (Continued)

When diode D4 at Pin 11 is switched to ground the input video signals will be DC shifted down and clamped at a voltage near ground (approximately 250 mV). This will disable the video amplifiers and force the output DC level low. The DC outputs from other similarly configured LM1203s could overide this lower DC level and provide the output signals to the 75Ω cable drivers. In this case any additional LM1203s would share the same 390Ω output resistor. The maximum DC plus peak white output voltage should not be allowed to exceed 7V because the "off" amplifier output stage could suffer internal zener damage. See *Figure 3* and text for a description of the internal configuration of the video amplifier.

Figure 10 shows the configuration for a three channel high frequency amplifier with non gated DC feedback. Pin 14 is tied low to turn on the clamp comparators (feedback amplifiers). The inverting inputs (Pins 17, 21, 26) are connected to the amplifier outputs from a low pass filter. Additional low frequency filtering is provided by the clamp caps. The drive resistors can be made variable or fixed at values between 0 and 300Ω. Maximum output swings are achieved when the DC output is set to approximately 4V. The high frequency response will be dependent upon external peaking at the drive pins.

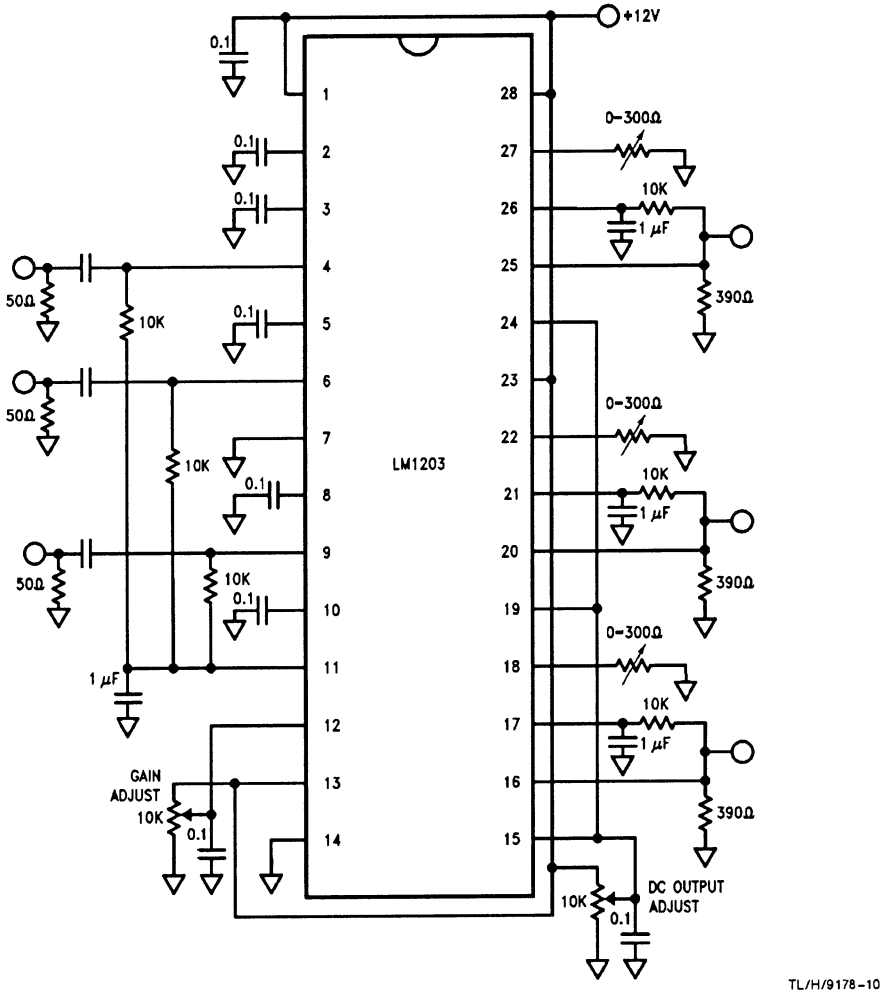

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FIGURE 10. Three Channel High Frequency Amplifier with Non-gated DC Feedback (Non-video Applications)

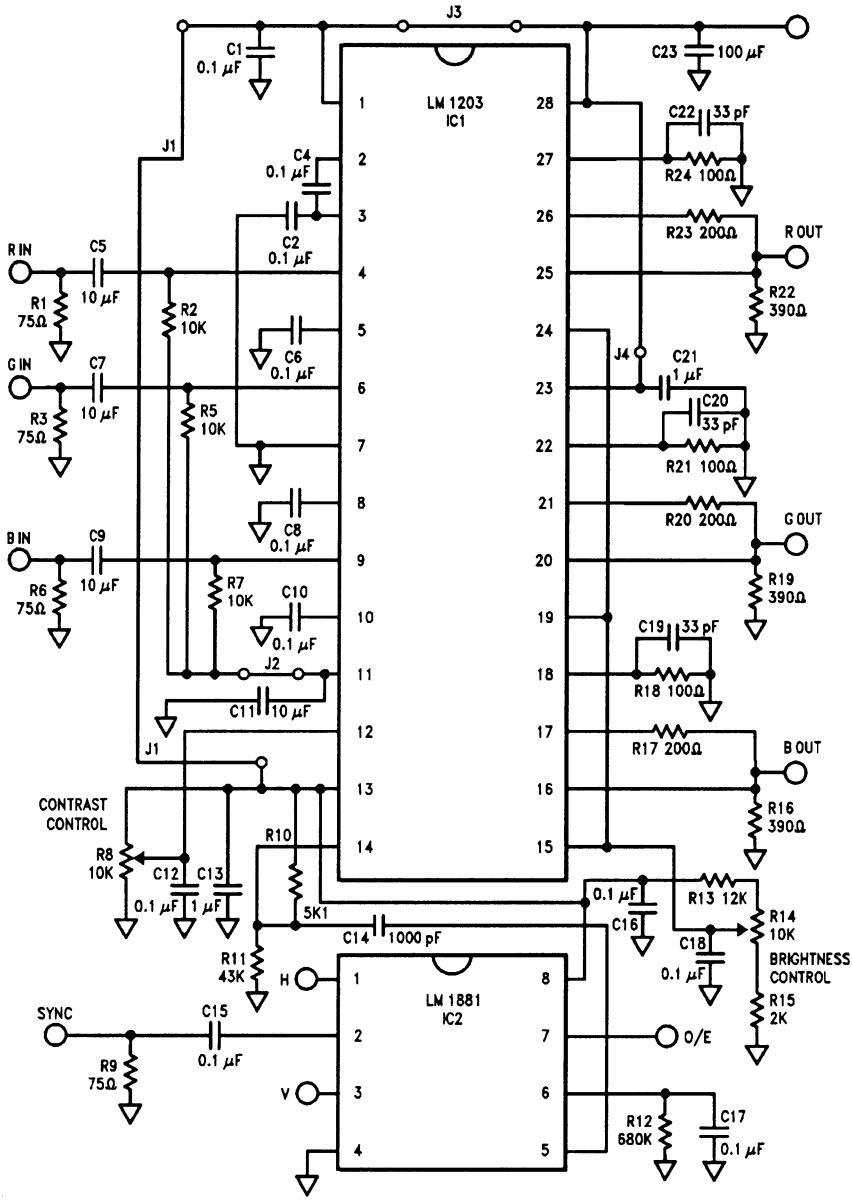

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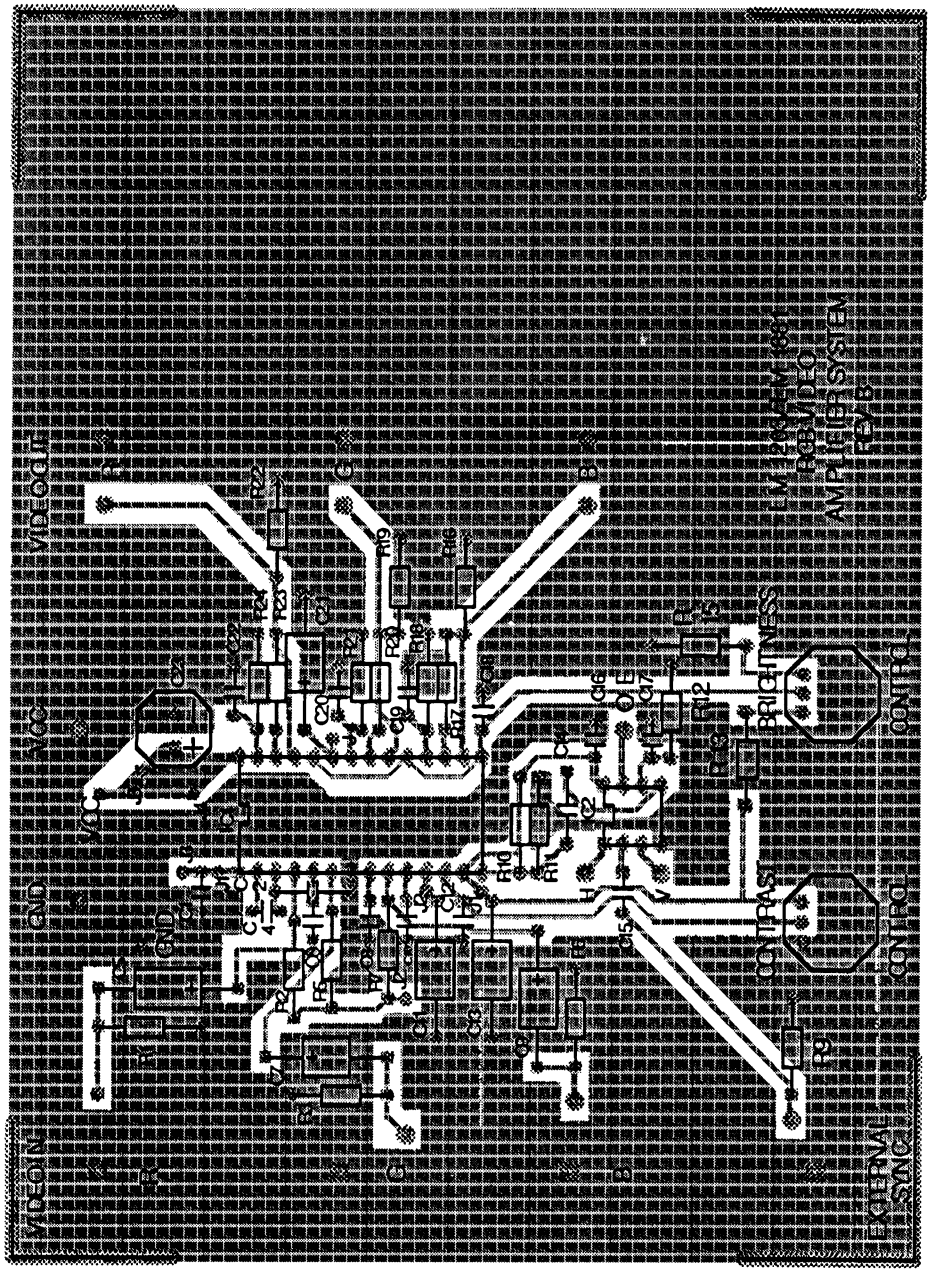
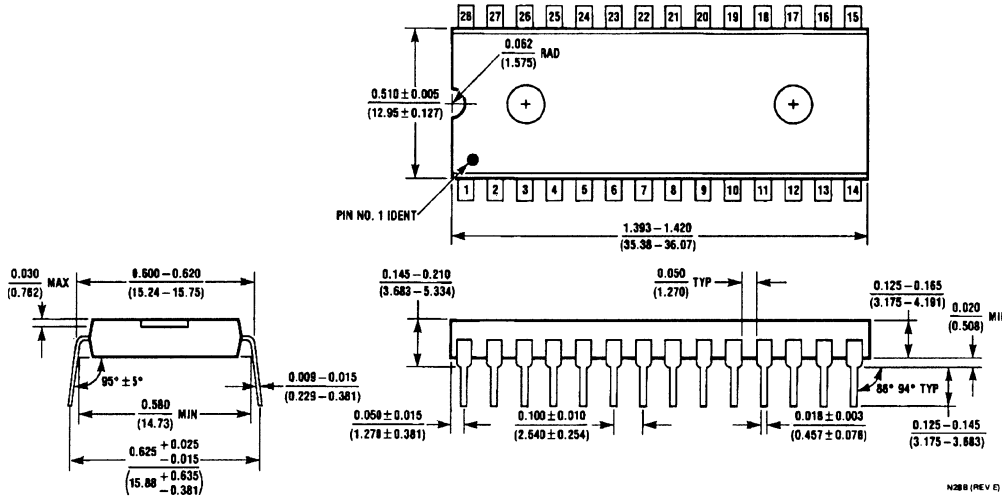
FIGURE 11. LM1203/LM1881 Application Circuit for PC Board



PC Board with Components

TL/H/9178–17

Physical Dimensions inches (millimeters)



28-Lead Molded Dual-In-Line Package (N)
Order Number LM1203N
NS Package Number N28B

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March, 1992

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LM1203A 100 MHz RGB Video Amplifier System

General Description

The LM1203A is an improved version of the popular LM1203 wideband video amplifier system. The device is intended for high resolution RGB CRT monitors. In addition to three matched video amplifiers, the LM1203A contains three gated differential input black level clamp comparators for brightness control and three matched attenuator circuits for contrast control. Each video amplifier contains a gain set or "Drive" node for setting maximum system gain or providing gain trim capability for white balance. The LM1203A also contains a voltage reference for the video inputs. The LM1203A is pin and function compatible with the LM1203.

Features

- Three wideband video amplifiers (100 MHz @ -3dB)
- Matched (± 0.1 dB or 1.2 %) attenuators for contrast control
- Three externally gated comparators for brightness control
- Provisions for individual gain control (Drive) of each video amplifier

- Video input voltage reference
- Low impedance output driver

Improvements over LM1203

- 100 MHz vs 70 MHz bandwidth
- Vout low : 0.25V vs 0.9V
- tr , tf : 4ns vs 7ns
- Built in power down spot killer
- Lower supply current

Applications

- High resolution RGB CRT monitors
- Video AGC amplifiers
- Wideband amplifiers with gain and DC offset controls
- 100 MHz Video Switcher

Block Diagram and Connection Diagram

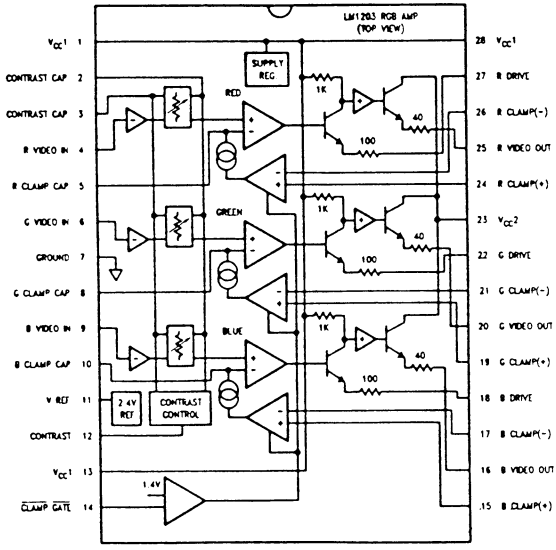

Figure 1

Ordering Information

Order Number LM1203AN
See NS Package Number N28B

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Absolute Maximum Ratings (Note 1)

Supply Voltage, Vcc	13.5V
Pins 1, 13, 23, 28 (Note 3)	
Peak video output source current (any one amp) pins 16, 20 or 25	28 mA
Voltage at any input pin, V_{in}	$V_{cc} \geq V_{in} \geq GND$
Power Dissipation, P_D (Above 25 °C derate based on θ_{ja} and T_j)	2.5W
Thermal Resistance, θ_{ja}	50 °C/W
Junction Temperature, T_j	150 °C
ESD Susceptibility (Note 4)	2kV
Storage Temperature	-65 °C to 150 °C
Lead Temperature	
Soldering , 10 sec	265 °C

Operating Ratings (Note 2)

Temperature Range	-20°C to 80 °C
Supply Voltage, V_{cc}	$10.8V \leq Vcc \leq 13.2V$

DC Electrical Characteristics See Test Circuit (Figure 2), $T_A = 25\ ^0C$; $V_{CC1} = V_{CC2} = 12V$. S17, 21, 26 Open; V12 = 6V; V14 = 0V; V15 = 2.0V unless otherwise stated

Symbol	Parameter	Conditions	Typical (note 5)	Limit (note 6)	Units
I_S	Supply Current	Vcc 1 + Vcc 2, RL = ∞ (note 7)	75	90	mA (max)
V11	Video Input Reference Voltage		2.8	2.4	V(min)
				3.2	V(max)
I_b	Video Input Bias Current	Any one amplifier	7	25	µA (max)
V_{14l}	Clamp Gate Low Input Voltage	Clamp comparators on	1.2	0.8	V(max)
V_{14h}	Clamp Gate High Input Voltage	Clamp comparators off	1.6	2.0	V(min)
I_{14l}	Clamp Gate Low Input Current	V14 = 0V	-0.8		µA (max)
I_{14h}	Clamp Gate High Input Current	V14 = 12V	0.005		µA (max)
I_{clamp+}	Clamp Cap Charge Current	V5,8 or 10 = 0V	750		µA(min)
I_{clamp-}	Clamp Cap Discharge Current	V5,8 or 10 = 5V	-750		µA(min)
V_{ol}	Video Output Low Voltage	V5,8 or 10 = 0V	0.15	0.5	V(max)
V_{oh}	Video Output High Voltage	V5,8 or 10 = 5V	7.5	6.5	V(min)
$\Delta V_{o(2V)}$	Video Output Offset Voltage	Between any two amplifiers, V15 = 2V	0.5		mV (max)
$\Delta V_{o(4V)}$	Video Output Offset Voltage	Between any two amplifiers, V15 = 4V	0.5		mV (max)

AC Electrical Characteristics See Test Circuit (Figure 2), T_A = 25 °C; V_{CC1} = V_{CC2} = 12V. S17, 21, 26 Closed; V14 = 0V; V15 = 4V unless otherwise stated

Symbol	Parameter	Conditions	Typical (note 5)	Limit (note 6)	Units
A_V max	Video Amplifier Gain	V12 = 12V, V_{IN} = 560 mVpp	6.0		V/V (min)
ΔA_V 5V	Attenuation @ 5V	Ref: A_V max, V12 = 5V	-10		dB
ΔA_V 2V	Attenuation @ 2V	Ref: A_V max, V12 = 2V	-40		dB
A_V match	Absolute Gain Match @ A_V max	V12 = 12V (Note8)	± 0.5		dB
ΔA_V track 1	Gain Change Between Amplifiers	V12 = 5V (Notes 8, 9)	±0.1		dB (max)
ΔA_V track 2	Gain Change Between Amplifiers	V12 = 2V (Notes 8, 9)	±0.3		dB (max)
THD	Video Amplifier Distortion	V12 = 3V, Vo = 1Vpp	0.5		%
f (-3dB)	Video Amplifier Bandwidth (Notes 10,11)	V12 = 12V, V_o = 4Vpp (No external peaking capacitor)	100		MHz
t_r	Output Rise Time (Note 10)	V_o = 4 Vpp (No external peaking capacitor)	3.6		ns
t_f	Output Fall Time (Note 10)	V_o = 4 Vpp (No external peaking capacitor)	4.0		ns
V_{sep} 10 kHz	Video Amplifier 10kHz Isolation	V12 = 12V (Note 12)	-65		dB
V_{sep} 10 MHz	Video Amplifier 10 MHz Isolation	V12 = 12V (Notes 10, 12)	-46		dB

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

Note 2: Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 3 : Vcc supply pins 1, 13, 23, 28 must be externally wired together to prevent internal damage during Vcc power on / off cycles.

Note 4 : Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Typical specifications are specified at + 25 °C and represent the most likely parametric norm.

Note 6: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 7 : The supply current specified is the quiescent current for Vcc1 and Vcc2 with RL = ∞, see Fig.2 's test circuit. The supply current for Vcc2 (pin 23) also depends on the output load. With video output at 4V DC, the additional current through Vcc2 is 36 mA for Fig 2's test circuit.

Note 8: Measure gain difference between any two amplifiers. V_{IN} = 1 Vpp.

Note 9: ΔA_V track is a measure of the ability of any two amplifiers to track each other and quantifies the matching of the three attenuators. It is the difference in gain change between any two amplifiers with the contrast voltage (V12) at either 5V or 2V measured relative to an A_V max condition, V12 = 12V. For example, at A_V max the three amplifiers' gains might be 17.4 dB, 16.9 dB and 16.4 dB and change to 7.3 dB, 6.9 dB, and 6.5 dB respectively for V12 = 5V. This yields the measured typical $\pm$ 0.1 dB channel tracking.

Note 10: When measuring video amplifier bandwidth or pulse rise and fall times, a double sided full ground plane printed circuit board without socket is recommended. Video amplifier 10 MHz isolation test also requires this printed circuit board.

Note 11: Adjust input frequency from 10 kHz (A_V max reference level) to the -3dB corner frequency (f_{-3dB}).

Note 12 : Measure output levels of the other two undriven amplifiers relative to the driven amplifier to determine channel separation. Terminate the undriven amplifier inputs to simulate generator loading. Repeat test at f_{IN} = 10 MHz for V_{sep} = 10 MHz.

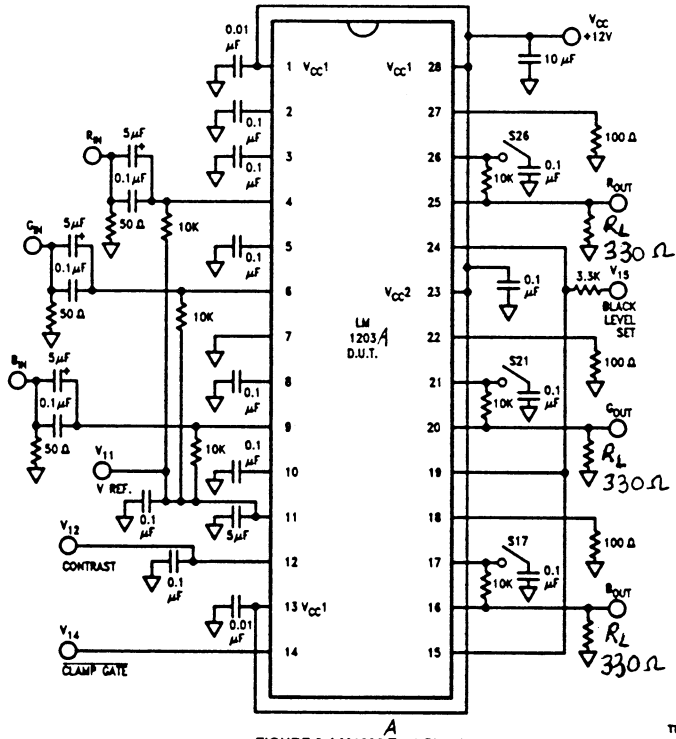

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FIGURE 2. LM1203 Test Circuit

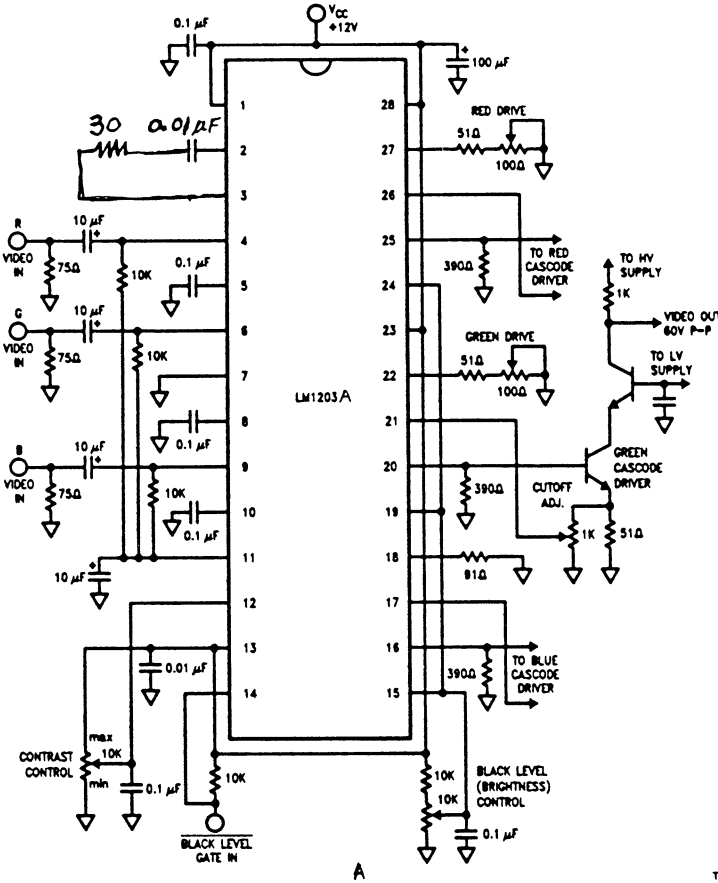

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FIGURE 3. LM1203 Typical Application

Applications Information

Figure 4 shows the block diagram of a typical analog RGB color monitor. The RGB monitor is used with CAD/CAM work stations, PC's, arcade games and in a wide range of other applications that benefit from the use of color display terminals. The RGB color monitor characteristics may differ in such ways as sweep rates, screen size, CRT color trio spacing (dot pitch), or in video amplifier bandwidths but will still be generally configured as shown in *Figure 4*. Separate horizontal and vertical sync signals may be required or they may be contained in the green video input signal. The video input signals are usually supplied by coax cable which is terminated in 75Ω at the monitor input and internally ac coupled to the video amplifiers. These input signals are approximately 1 volt peak to peak in amplitude and at the input of the high voltage video section, approximately 6V peak to peak. At the cathode of the CRT the video signals can be as high as 60V peak to peak. One important requirement of the three video amplifiers is that they match and track each other over the contrast and brightness control range. The *Figure 4* block labeled "VIDEO AMPLIFICATION WITH GAIN AND DC CONTROL" describes the function of the LM1203 which contains the three matched video amplifiers, contrast control and brightness control.

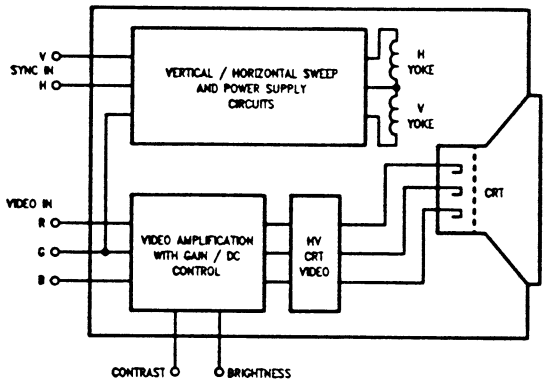

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FIGURE 4. Typical RGB Color Monitor Block Diagram

Circuit Description

Figure 5 is a block diagram of one of the video amplifiers along with the contrast and brightness controls. The contrast control is a dc-operated attenuator which varies the ac gain of all three amplifiers simultaneously while not introducing any signal distortions or tracking errors. The brightness control function requires a "sample and hold" circuit (black level clamp) which holds the dc bias of the video amplifiers and CRT cathodes constant during the black level reference portion of the video waveform. The clamp comparator, when gated on during this reference period, will charge or discharge the clamp capacitor until the plus input of the clamp comparator matches that of the minus input voltage which was set by the brightness control.

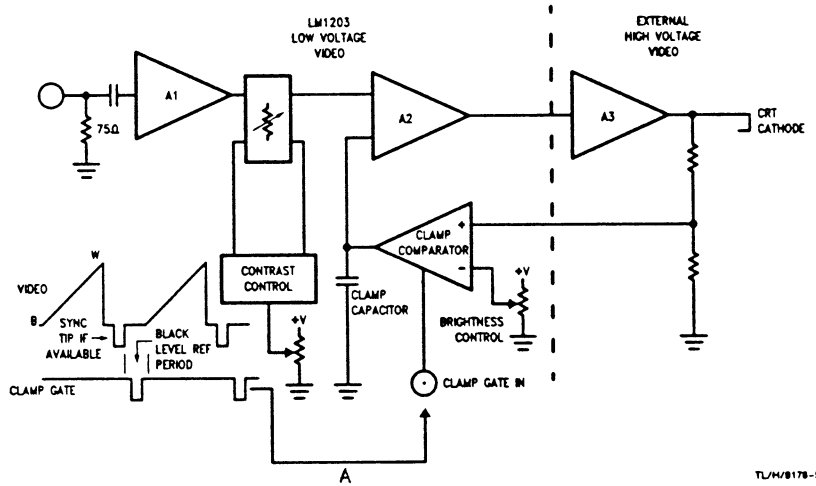


FIGURE 5. Block Diagram of LM1203 Video Amplifier with Contrast and Black Level Control

Circuit Description (Continued)

Video amplifier section

Figure 6 is a simplified schematic of one of the three video amplifiers along with the recommended external components. The IC pin numbers are circled and all external components are shown outside the dashed line. The video input is applied to pin 6 via a 10 µF coupling capacitor. DC bias for the video input is through the 10k resistor connected to the 2.8V reference at pin 11. The low frequency roll - off of the amplifier is set by these two components. Transistor Q1 buffers the video signal to the base of Q2. Q2's collector current is then directed to the Vcc1 supply directly or through the 2k load resistor depending upon the differential DC voltage at the bases of Q3 and Q4. This differential DC voltage is generated by the contrast control circuit which is described in the following sections. An RF decoupling capacitor is required between pins 2 and 3 to ensure high frequency isolation between the three video amplifiers which share these common connections. The video signal is buffered by Q5 and Q6 and DC level shifted by the voltage drop across R5. The magnitude of the current through R5 is determined by the voltage at pin 8. The voltage at pin 8 is set by the clamp comparator output current which charges or discharges the clamp hold capacitor during the black level period of the video waveform. Transistors Q9 and Q10 are darlington connected to ensure a minimum discharge of the clamp hold capacitor during the time that the clamp capacitor is gated off. Q7, Q8 and R6 form a current mirror which sets a voltage at the base of Q11. Q11 buffers the video signal to the base of Q12 which provides additional signal gain. The " Drive " pin allows the user to trim the Q12 gain of each amplifier to correct for gain differences in the CRT and high voltage cathode driver gain stages. A small capacitor (several pico-Farads) from the " Drive " pin to ground will cause high frequency peaking and slightly improve the amplifier's bandwidth.

For individual gain adjustment of each video channel, a 51 ohm resistor in series with a 100 ohm potentiometer should be used with the red and green channel drive pins. A 91 ohm resistor used with the blue channel drive pin sets the blue channel amplifier gain at approximately 6.2. The 100 ohm potentiometers at the red and green channel drive pins allow a gain of 6.2 with ± 25 % gain adjustment. The video signal at the collector of Q12 is buffered and level shifted down by Q13, Q14 and Q15 to the base of the output emitter follower Q16. A 50 ohm decoupling resistor is included in series with the emitter of Q16 and the video output pin so as to prevent oscillations when driving capacitive loads. An external resistor should be connected between the video output pin and ground. The value of this resistor should not be less than 390 ohms or else package power limitations may be exceeded under worse case conditions (High supply voltage, maximum current, maximum temperature). The collector current from the video output transistor of each video channel is returned to the power supply at Vcc2, pin 23. When making power dissipation calculations note that the data sheet specifies only the Vcc1 supply current at 12V supply voltage. The IC power dissipation due to Vcc2 is dependant upon the external video output pull down resistor.

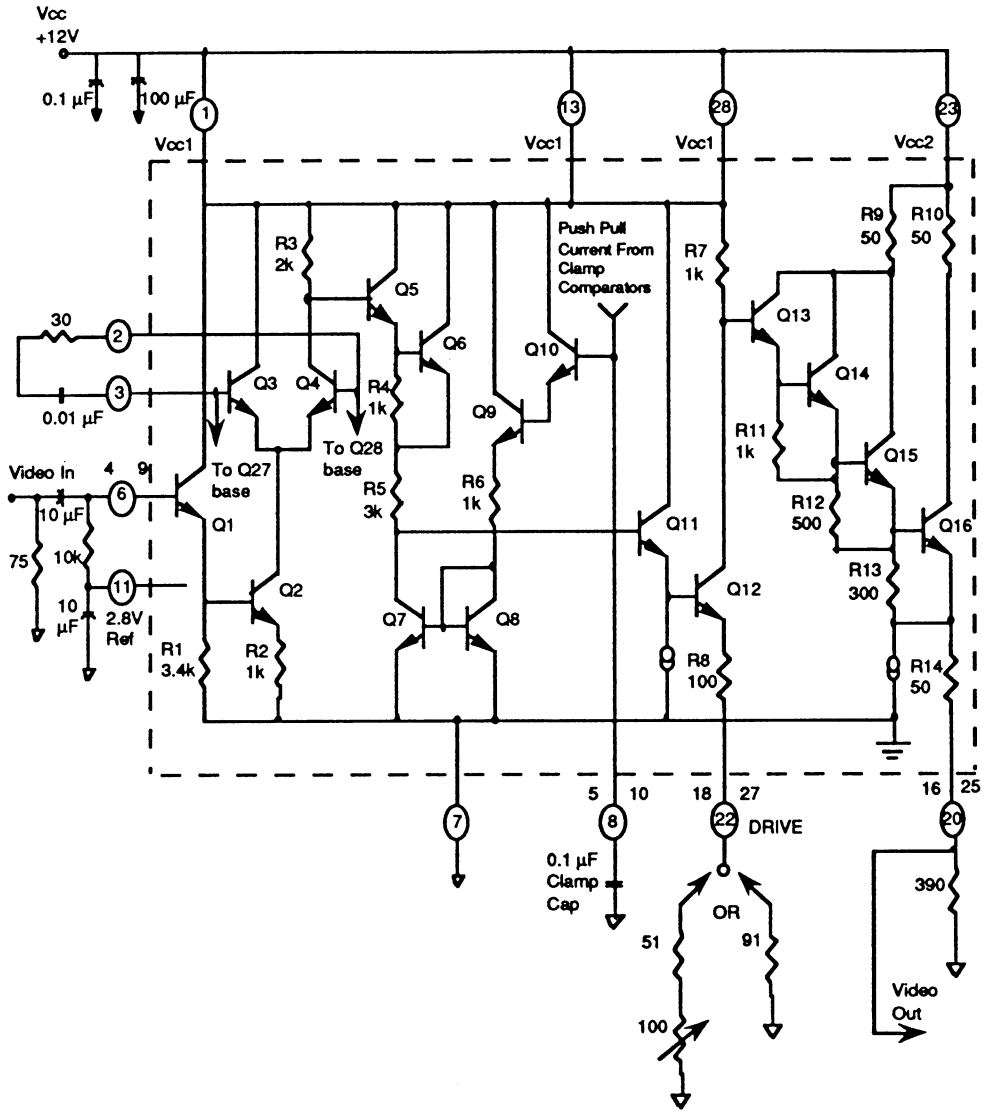


Figure 6. Simplified schematic of LM1203A video amplifier section with recommended external components.

Circuit Decsription (Continued)

Input reference and contrast control section

Figure 7 shows the input reference and contrast control circuitry. A temperature compensated 2.8V reference voltage is made available at pin 11. The external DC biasing resistors shown should not be larger than 10k because minor differences in input bias currents of the individual video amplifiers may cause offsets in gain. Figure 7 also shows how the contrast control circuit is configured. R21, R22, Q22, Q23 and Q24 establish a low impedance zero TC half supply voltage reference at the base of Q25. The differential amplifier formed by Q27, Q28 and feedback transistor Q29 along with R28 and R29 establish a differential base voltage for Q3 and Q4 in Figure 6. When externally adding or subtracting current from the colector of Q28, a new differential voltage is generated that reflects the change in the ratio of currents in Q27 and Q28. To allow voltage control of the current through Q28, resistor R27 is added between the collector Q28 and pin 12. A capacitor should be connected from pin 12 to ground to prevent noise from the contrast control potentiometer from entering the IC.

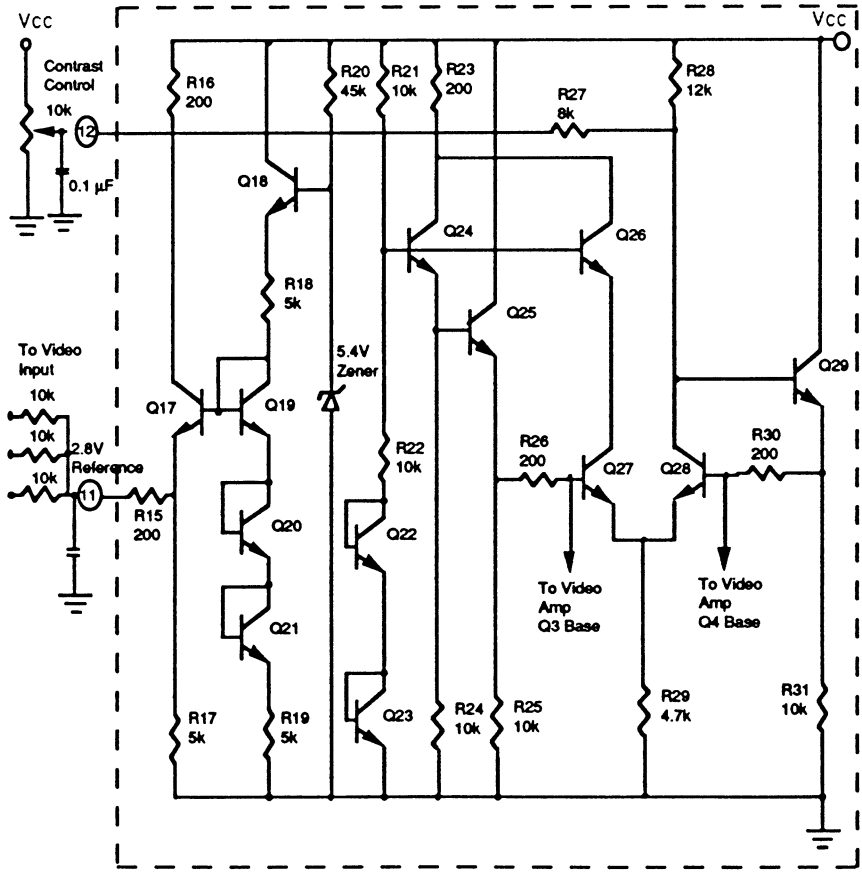


Figure 7. Simplified schematic of LM1203A video input reference and contrast control circuits.

Circuit Description (Continued)
Clamp gate and clamp comparator section

Figures 8 and 9 show simplified schematics of the clamp gate and clamp comparator circuits. The clamp gate circuit (Figure 8) consists of a PNP input buffer transistor (Q46), a PNP emitter coupled pair (Q47 and Q49) referenced on one side to 2.1V and an output switch transistor Q53. When the clamp gate input at pin 14 is high (> 1.5V) the Q53 switch is on and shunts the 200 µA current from current source Q54 to ground. When pin 14 is low (< 1.3V) the Q53 switch is off and the 200 µA current is mirrored by the current mirror comprised of Q55 and Q36 (see Figure 9). Consequently the clamp comparator comprised of the differential pair Q35 and Q37 is enabled. The input of each clamp comparator is similar to the clamp gate except that an NPN emitter coupled pair is used to control the current that will charge or discharge the clamp capacitors at pins 5, 8 and 10. PNP transistors are used at the inputs because they offer a number of advantages over NPNs. PNPs will operate with base voltages at or near ground and will usually have a greater emitter base breakdown voltage (BVebo). Because the differential input voltage to the clamp comparator during the video scan period could be greater than the BVebo of NPN transistors a resistor (R37) with a value one half that of R36 or R39 is connected between the bases of Q34 and Q38. The clamp comparator's common mode range is from ground to approximately 9V and the maximum differential input voltage is Vcc and ground.

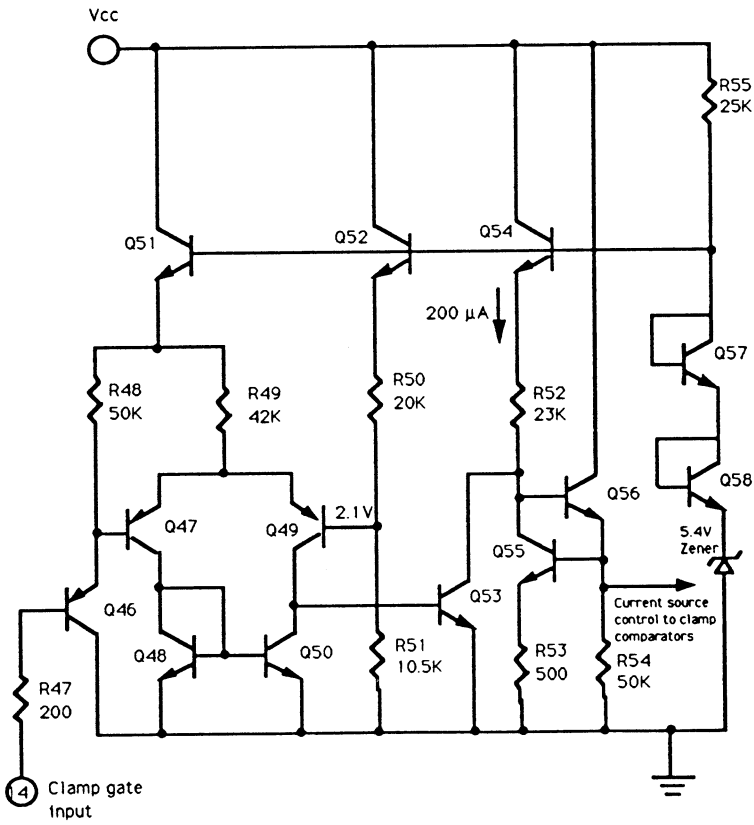


Figure 8. Simplified schematic of LM1203A clamp gate circuit.

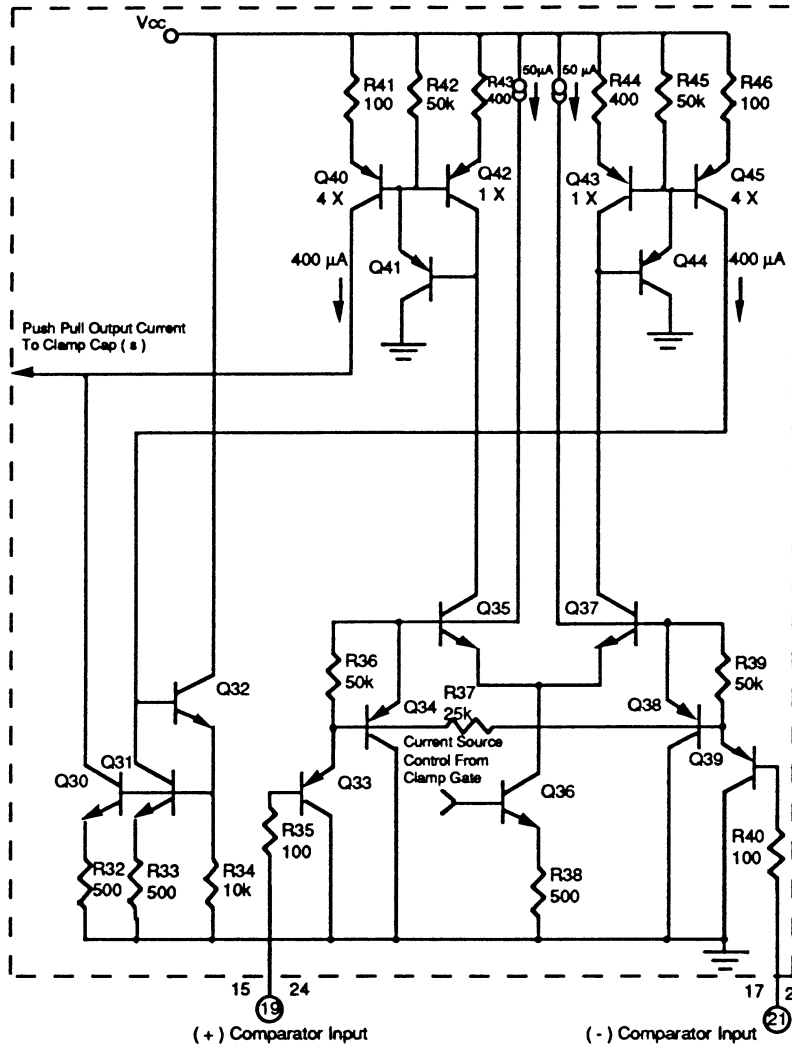


Figure 9. Simplified schematic of LM1203A clamp comparator circuits.

Additional Applications of the LM1203A

Figure 10 shows the configuration for a three channel high frequency amplifier with non gated DC feedback. Pin 14 is tied low to turn on the clamp comparators (feedback amplifiers). The inverting inputs (Pins 17, 21, 26) are connected to the amplifier outputs from a low pass filter. Additional low frequency filtering is provided by the clamp caps. The drive resistors can be made variable or fixed at values between 0 and 300Ω. Maximum output swings are achieved when the DC output is set to approximately 4V. The high frequency response will be dependent upon external peaking at the drive pins.

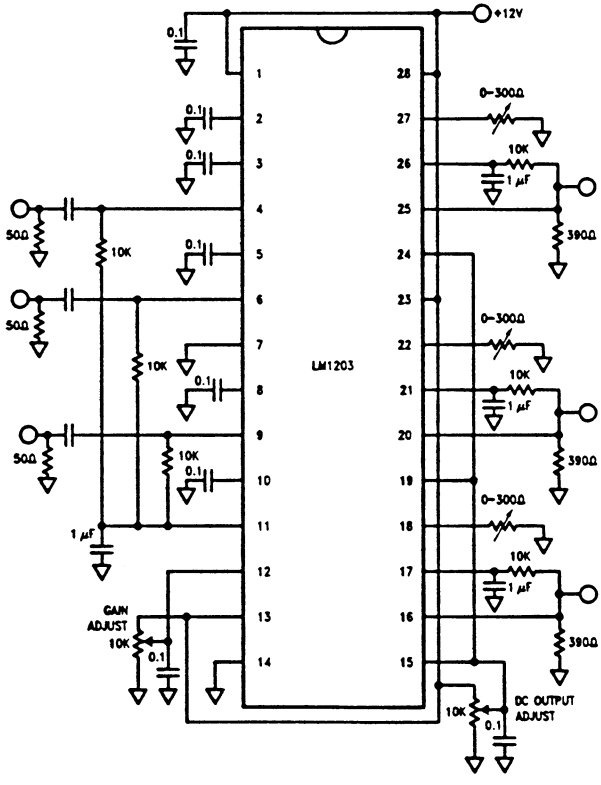


FIGURE 10. Three Channel High Frequency Amplifier with Non-gated DC Feedback (Non-video Applications)

Additional Applications of the LM1203A (Continued)

Figure.11 shows a complete RGB video preamplifier circuit using the LM1203A. A quad Exclusive - Or gate (MM74HC86) is used to generate the back porch clamp signal from the composite sync input signal. The composite H Sync input signal may have either polarity. The back porch clamp signal applied to LM1203A's pin 14 allows clamping the video output signals to the black reference level thereby providing DC restoration. The back porch clamp pulse width is determined by the time constant due to the product of R11 and C15. For fast horizontal scan rates, the back porch clamp pulse width can be made narrower by decreasing the value of R11 or C15 or both. Note that an MM74C86 Exclusive - Or gate may also be used, however, the pin out is different than that of the MM74HC86.

For optimum performance and maximum bandwidth, high speed buffer transistors (Q1, Q2 and Q3 in Figure.11) are recommended. The 2N5770 NPN transistors maintain high speed at high currents when driving the inputs of high voltage CRT drivers.

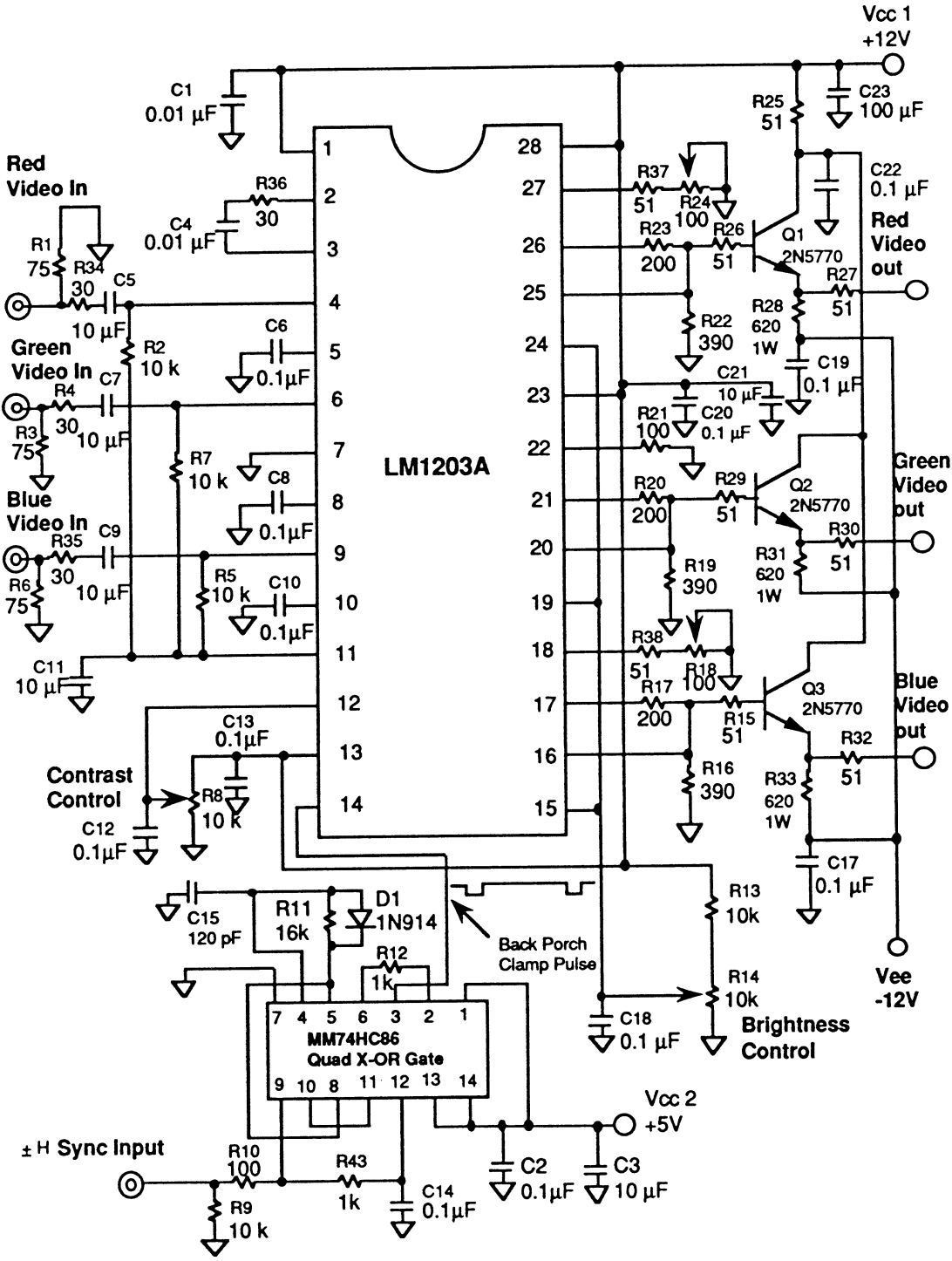


Figure 11. LM1203A applications circuit.

LM1203A versus LM1203

LM1203A is an improved version of the LM1203 RGB video amplifier system and is pin and function compatible with the LM1203. LM1203A's output voltage can swing as low as 0.25V as opposed to 0.9V for the LM1203. This eliminates the need for a level shift stage between the preamplifier and the CRT driver in most applications.

The LM1203A also offers faster rise and fall times of 4 ns versus 7 ns for the LM1203 and 100 MHz bandwidth versus 70 MHz for LM1203. Because of LM1203A's wide bandwidth, the device may oscillate if plugged directly into an existing LM1203 board. For optimum performance and stable operation, a double sided printed circuit board with adequate ground plane and power supply decoupling as close to the Vcc pins as possible is recommended. Figure 12 shows the layout of the PC board for Figure 11's circuit. For suggestions on optimum PC board layout, please see the reference section below.

The LM1203A also includes a built in power down spot killer to prevent a flash on the screen upon power down. In some preamplifiers, the video output signal may go high as the device is being powered down. This may cause a whiter than white level at the output of the CRT driver thus causing a flash on the screen.

Reference :

Ott, Henry. W, Noise Reduction Techniques in Electronic Systems, John Wiley & Sons, New York.

National Semiconductor

September 1991

LM1204 150 MHz RGB Video Amplifier System

General Description

The LM1204 is a triple 150 MHz video amplifier system designed specifically for high resolution RGB video display applications. In addition to three matched video amplifiers, the LM1204 contains a DC operated contrast control, a DC operated drive control for each amplifier, and a dual clamping system for both brightness control and video blanking. The LM1204 also contains a back porch clamp pulse generator which is activated by an externally supplied ±H/HV sync signal or by an external composite video signal. The ±H/HV sync input will have priority over the composite video input. A single −H/HV sync output is provided for the automatically selected sync input signal. The back porch clamp pulse width is user adjustable from 0.3 μs to 4 μs.

The LM1204 video output stage will directly drive most Hybrid or discrete CRT amplfier input stages without the need for an external buffer transistor. The device has been designed to operate from a 12V supply with all DC controls operating over a 0V to 4V range providing for an easy interface to serial digital buss controlled monitors.

Features

- Built-in video blanking function
- Built-in sync separator for composite video input
- Includes DC restoration of video signals
- Back porch clamp pulse width user adjustable
- DC control of brightness, contrast, blanking level, drive and cutoff
- DC controls are 0V to 4V for easy interfacing to a digitally controlled system

Key Specifications

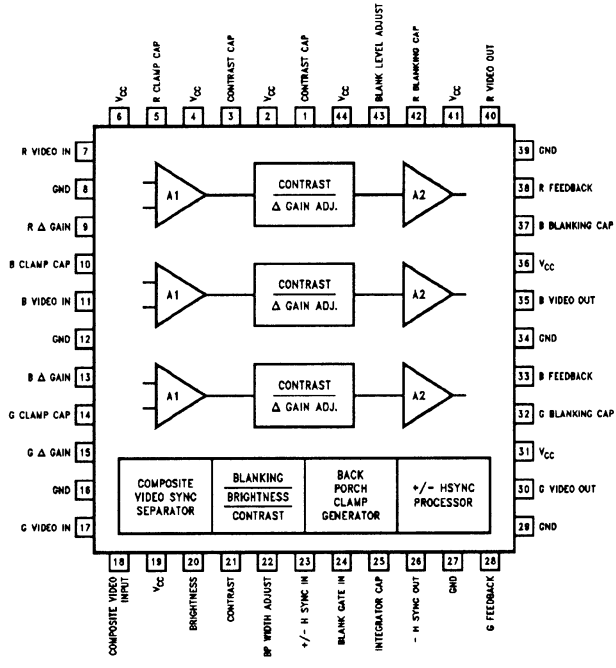
- 150 MHz large signal bandwidth (typ)
- 2.6 ns rise/fall times (typ)
- 0.1 dB contrast tracking (typ)
- ±3 dB drive (Δ gain) adjustments on R, G, B channels (typ)

Applications

- High resolution CRT monitors
- Video AGC amplifier
- Wideband amplifier with gain and DC offset control

Block Diagram and Connection Diagram

Top View



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Ordering Information

Order Number LM1204V
See NS Package Number V44A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC} Pins 2, 4, 6, 19, 31, 41, 44 (Note 3)	13.5V
Peak Video Output Source Current (Any One Amplifier) Pins 30, 35 or 39	30 mA
Voltage at Any Input Pin, V_{IN}	GND ≤ V_{IN} ≤ V_{CC}
Maximum ±H Sync Input Voltage	5.5 V_{PP}
Power Dissipation, PD (Above 25°C Derate Based on θ_{JA} and T_J)	2.4W
Thermal Resistance, θ_{JA}	52°C/W
Junction Temperature, T_J	150°C
ESD Susceptibility (Note 4)	2.5 kV
Storage Temperature	−65°C to 150°C
Lead Temperature	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

Operating Ratings (Note 2)

Temperature Range	0°C to 70°C
Supply Voltage, V_{CC}	10.8V ≤ V_{CC} ≤ 13.2V

DC Electrical Characteristics (Video Amplifier Section)

The following specifications apply for V_{CC} (pins 2, 4, 6, 19, 31, 36, 41 and 44) = 12V and T_A = 25°C unless otherwise specified. S1 = B, S2 = B, S3, 4, 5 closed, V9, 13, 15 = 2V, V20, 21, 22, 24, 43 = 0.5V unless otherwise specified; see test circuit, *Figure 1*.

Symbol	Parameter	Conditions	Typical (Note 5)	Limit (Note 6)	Units
I_S	Supply Current	No Video or Sync Input Signals, S1 = A	100	125	mA (Max)
I_B	Input Bias Current (Pin 9, 13, 15, 20, 21 or 22)	S1 = A	0.3	2	µA (Max)
I_{24h}	Blank Gate Input High Current	V24 = 4V	0.01	2	µA (Max)
I_{24l}	Blank Gate Input Low Current	V24 = 0V	2	5	µA (Max)
I_{FB}	Feedback Input Current (Pin 28, 33 or 38)		150		nA
I_{Blank+}	Blank Cap Charge Current	$V_{32,37,42}$ = 0V	185	75	µA (Min)
I_{Blank-}	Blank Cap Discharge Current	$V_{32,37,42}$ = 5V	−185	−75	µA (Min)
I_{BB}	Blank Cap Bias Current (Pins 32, 37, 42)		20		nA
I_{Clamp+}	Clamp Cap Charge Current	$V_{5,10,14}$ = 0V	185	75	µA (Min)
I_{Clamp-}	Blank Cap Discharge Current	$V_{5,10,14}$ = 5V	−185	−75	µA (Min)
I_{CB}	Clamp Cap Bias Current (Pins 5, 10, 14)		20		nA
V_{24h}	Blank Gate High Input Voltage	Input Signal is Not Blanked		2	V (Min)
V_{24l}	Blank Gate Low Input Voltage	Input Signal is Blanked		0.8	V (Max)
	Blank Comparator Offset Voltage	Voltage between V43 and Any One Video Output	2	50	mV (Max)
V_H	Video Output High Voltage (Pins 30, 35, 40)	R_L = 350Ω V28, 33, 38 = 0V	8.7	7	V(Min)
V_L	Video Output Low Voltage (Pins 30, 35, 40)	R_L = 350Ω V28, 33, 38 = 4V	0.1	0.5	V(Max)
V_{CM43}	Common Mode Range of Blank Comparator (Pins 43, 28, 33, 38)			0.5 4	V(Min) V(Max)

DC Electrical Characteristics (Sync Separator/Processor Section)

The following specifications apply for V_{CC} (Pins 2, 4, 6, 19, 31, 36, 41 and 44) = 12V and T_A = 25°C, unless otherwise specified. S1 = B, S2 = B, S3, 4, 5 closed, V9, 13, 15 = 2V, V20, 21, 22, 24, 43 = 0.5V, unless otherwise specified; see Test Circuit *Figure 1.*

Symbol	Parameter	Conditions	Typical (Note 5)	Limit (Note 6)	Units
$-H\ V_{OH}$	−H Sync Output Logic High (Pin 26)		4.2	2.4	V(Min)
$-H\ V_{OL}$	−H Sync Output Logic Low (Pin 26)		0.1	0.4	V(Max)
V_{23}	Quiescent DC Voltage at ±H Sync Input		3		V

AC Electrical Characteristics (Video Amplifier Section)

The following specifications apply for V_{CC} (Pins 2, 4, 6, 19, 31, 36, 41 and 44) = 12V and T_A = 25°C, unless otherwise specified. S1 = B, S2 = B, S3, 4, 5 closed, V9, 13, 15, 21, 24, 43 = 4V, V20 = 2V, unless otherwise specified; see Test Circuit *Figure 1.*

Symbol	Parameter	Conditions	Typical (Note 5)	Limit (Note 6)	Units
R_{IN}	Video Amplifier Input Resistance		20		kΩ
A_{Vmax}	Maximum Video Amplifier Gain	f_{IN} = 12 kHz	10	5.5	V/V(Min)
ΔA_{Vtrack}	Amplifier Gain (Contrast) Tracking (Note 7)		0.1		dB
ΔA_{V2V}	Attenuation at 2V	Ref: $A_{V_{max}}$ V21 = 2V	6		dB
$\Delta A_{V0.5V}$	Attenuation at 0.5V	Ref: $A_{V_{max}}$ V21 = 0.5V	28	20	dB(Min)
ΔGain	Δ Gain Range (Pins 9, 13, 15)	V9, 13, 15 = 0V to 4V	±3		dB
ΔV_O	Max Brightness Tracking Error (Note 8)		100		mV
$f_{-3\,dB}$	Video Amplifier Bandwidth (Note 9)	V_{OUT} = 3.5 V_{PP}	150		MHz
THD	Video Amplifier Distortion	V_{OUT} = 1 V_{PP}, f = 12 kHz	0.3		%
t_R	Video Output Rise Time (Note 9)	Square Wave Input V_{OUT} = 3.5 V_{PP}, R_L = 350Ω	2.6		ns
t_F	Video Output Fall Time (Note 9)	Square Wave Input V_{OUT} = 3.5 V_{PP}, R_L = 350Ω	2.6		ns
$V_{ISO\ (1\ MHz)}$	Video Amplifier 1 MHz Isolation (Notes 9, 10)		−50		dB
$V_{ISO\ (130\ MHz)}$	Video Amplifier 130 MHz Isolation (Notes 9, 10)		−10		dB

AC Electrical Characteristics (Sync Separator/Processor Section)

The following specifications apply for V_{CC} (Pins 2, 4, 6, 19, 31, 36, 41 and 44) = 12V and T_A = 25°C, unless otherwise specified. S1 = A, S2 = B, S3, 4, 5 closed, V9, 13, 15, 20, 21, 43 = 2V, unless otherwise specified; see Test Circuit *Figure 1* and Timing Diagram for input waveform.

Symbol	Parameter	Conditions	Typical (Note 5)	Limit (Note 6)	Units
$V_{18(Min)}$	Composite Video Input Voltage (Pin 18)	S2 = A, Input = 10% Duty Cycle, Test for Loss of BP Pulse at Pin 26		0.15	V_{PP} (Min)
$V_{18(Max)}$	Composite Video Input Voltage (Pin 18)			2	V_{PP} (Max)
V_{23}	±H Sync Input Voltage (Pin 23)	Input = 10% Duty Cycle		1.6	V_{PP} (Min)
	Back Porch Clamp Pulse Width at V_{24} = 1V	S2 = A, Pin 26 = BP Output	1	1.4	µs (Max)
	Back Porch Clamp Pulse Width at V_{24} = 4V		300	600	ns (Max)
	Maximum ±H Sync Input Frequency		600		KHz
D_{HI}	Max Duty Cycle of Active High H Sync (Pin 23)	Test for Loss of Sync at Pin 26	22		%
D_{LO}	Max Duty Cycle of Active Low H Sync (Pin 23)		22		%
t_{pdl1}	±H Sync Input to −H Sync Output Low Delay	Input = 10% Duty Cycle	100		ns
t_{pdh1}	±H Sync Input to −H Sync Output High Delay	Input = 10% Duty Cycle	65		ns
t_{pd1}	±H Sync Input Trailing Edge to Back Porch Clamp Output Delay	Input = 10% Duty Cycle, S2 = A	70		ns
t_{pdl2}	Composite Video Input to −H Sync Output Low Delay	Input = 10% Duty Cycle	106		ns
t_{pdh2}	Composite Video Input to −H Sync Output High Delay	Input = 10% Duty Cycle	68		ns
t_{pd2}	Composite Video Input Trailing Edge to Back Porch Clamp Output Delay	Input = 10% Duty Cycle S2 = A	78		ns
$t_{pdl2}-t_{pdl1}$	Composite Video and ±H Sync Input to −H Sync Output Delta Delay	Input = 10% Duty Cycle	6		ns

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

Note 2: Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 3: V_{CC} supply pins 2, 4, 6, 19, 31, 36, 41 and 44 must be externally wired together to prevent internal damage during V_{CC} power on/off cycle.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Typical specifications are specified at +25°C and represent the most likely parametric norm.

Note 6: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 7: ΔA_V tracking is a measure of the ability of any two amplifiers to track each other and quantifies the matching of the three attenuators. It is the difference in gain change between any two amplifiers with the contrast voltage, V21, at either 4V or 2V measured relative to an A_V max condition V21 = 4V. For example, at A_V max, the three amplifier gains might be 17.4 dB, 16.9 dB and 16.4 dB and change to 7.3 dB, 6.9 dB and 6.5 dB respectively for V21 = 2V. This yields the measured typical ±0.1 dB channel tracking.

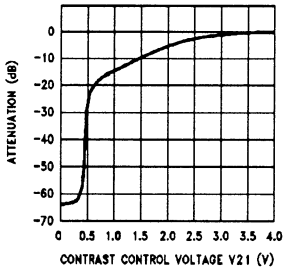
Note 8: Brightness tracking error is measured with all three video channels set for equal gain. The measured value is limited by the resolution of the measurement equipment.

Note 9: When measuring video amplifier bandwidth or pulse rise and fall times, a double sided full ground plane printed circuit board is recommended. Video amplifier isolation tests also require this printed circuit board. The measured rise and fall times are effective rise and fall times, taking into account the rise and fall times of the generator.

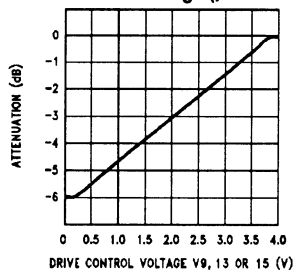
Note 10: Measure output levels of either undriven amplifier relative to the driven amplifier to determine channel isolation. Terminate the undriven amplifier inputs.

Typical Performance Characteristics V_{CC} = 12V, T_A = 25°C unless otherwise specified

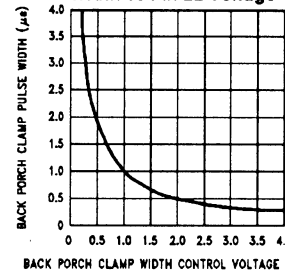
Attenuation vs Contrast Control Voltage (f = 12 kHz)



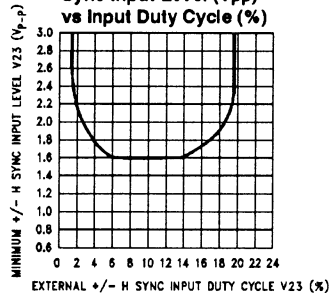
Attenuation vs Drive Control Voltage (f = 12 kHz)



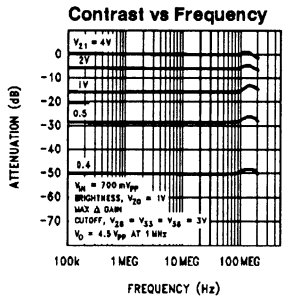
Back Porch Clamp Pulse Width vs Pin 22 Voltage



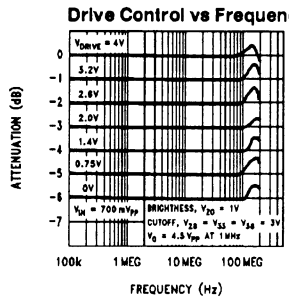
Minimum External ±H Sync Input Level (V_{PP}) vs Input Duty Cycle (%)



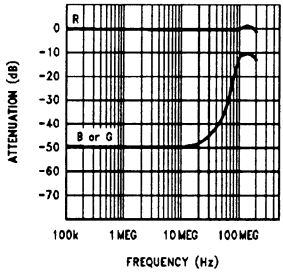
Contrast vs Frequency



Drive Control vs Frequency



Crosstalk vs Frequency



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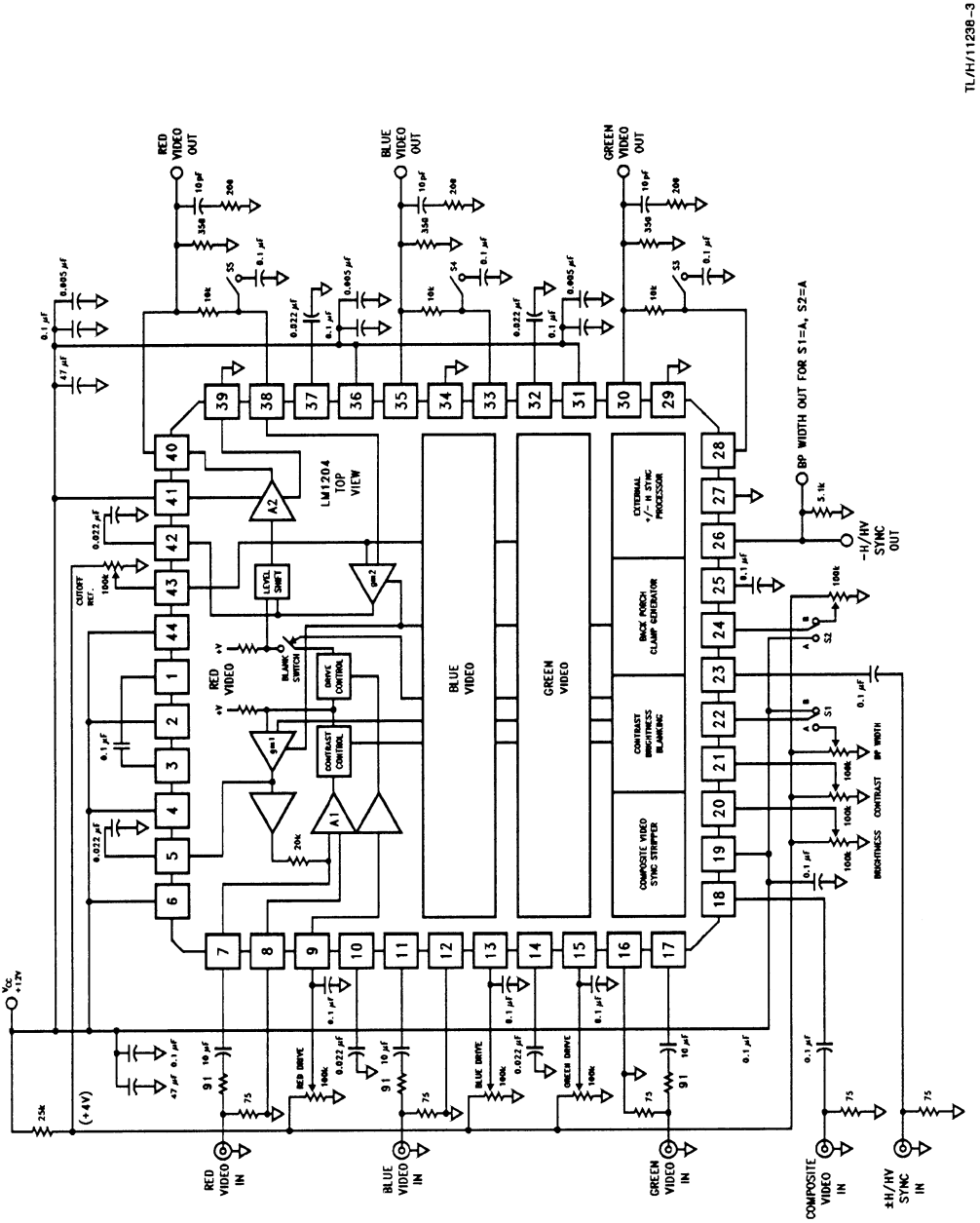

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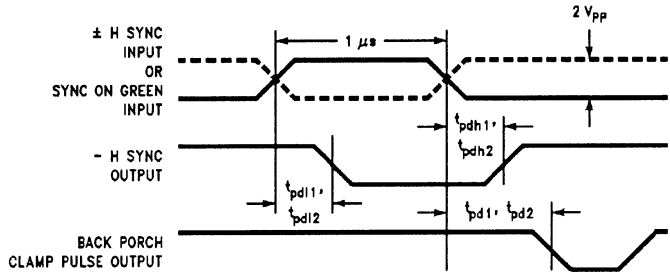
FIGURE 1. LM1204 Test Circuit

Timing Diagram



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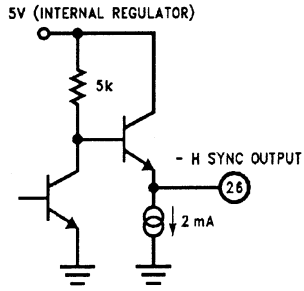
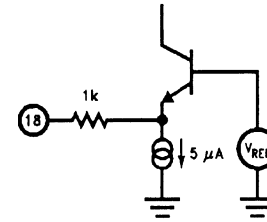
Input/Output Stages

–H Sync Output Stage



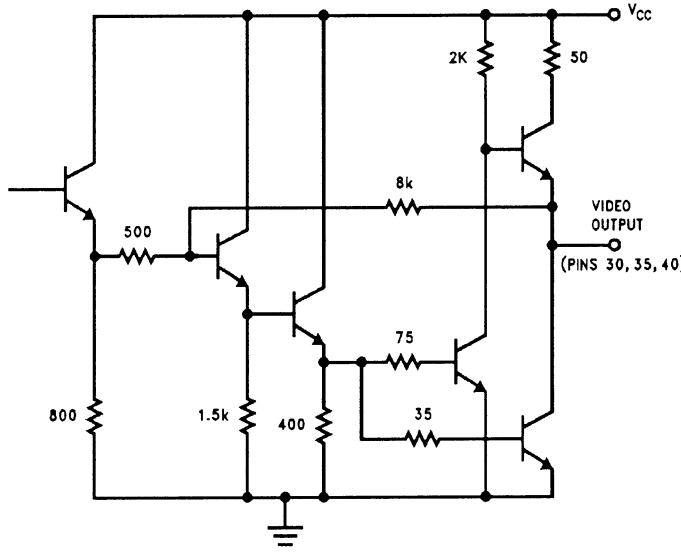
TL/H/11238–5

Composite Video Input



TL/H/11238–6

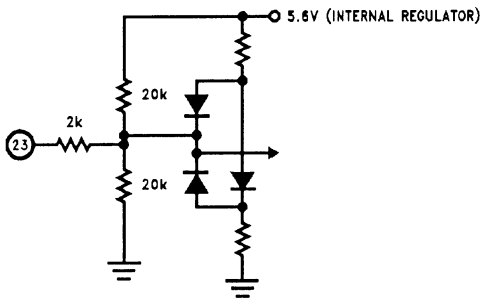
Video Output Stage



TL/H/11238–21

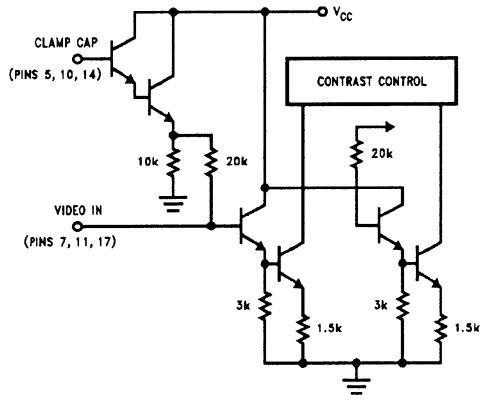
Input/Output Stages (Continued)

±H/HV Sync Input



TL/H/11238–7

Video Input Stage



TL/H/11238–8

Pin Descriptions

V_{CC} (Pins 2, 4, 6, 19, 31, 36, 41, 44)	All V_{CC} pins must be externally wired together. For stable operation, each supply pin should be bypassed with a 0.01 μF and a 0.1 μF capacitor connected as close to the pin as is possible.
Contrast Cap (Pins 1, 3)	An external decoupling capacitor of value 0.1 μF should be connected between pins 1 and 3 for contrast control.
R Clamp Cap (Pin 5)	A 0.022 μF to 0.1 μF capacitor should be connected from this pin to ground. This capacitor allows clamping of the red channel video signal to the reference black level.
B Clamp Cap (Pin 10)	A 0.022 μF to 0.1 μF capacitor should be connected from this pin to ground. This capacitor allows clamping of the blue channel video signal to the reference black level.
G Clamp Cap (Pin 14)	A 0.022 μF to 0.1 μF capacitor should be connected from this pin to ground. This capacitor allows clamping of the green channel video signal to the reference black level.
R Video In (Pin 7)	This is the input for the red channel video signal, the signal should be AC coupled to the input through a 10 μF capacitor.
B Video In (Pin 11)	This is the input for the blue channel video signal, the signal should be AC coupled to the input through a 10 μF capacitor.
G Video In (Pin 17)	This is the input for the green channel video signal, the signal should be AC coupled to the input through a 10 μF capacitor.
R Δ Gain (Pin 9)	This is the gain adjustment pin for the red video channel. A 0V to 4V_{DC} voltage is applied to this pin to vary the gain of the red channel. Usually, the red channel is set for maximum gain and the gains of the blue and green channels are reduced relative to the red channel until white balance is achieved on the CRT screen.
B Δ Gain (Pin 13)	This is the gain adjustment pin for the blue video channel. A 0V to 4 V_{DC} voltage is applied to this pin to vary the gain of the blue channel.
G Δ Gain (Pin 15)	This is the gain adjustment pin for the green video channel. A 0V to 4 V_{DC} voltage is applied to this pin to vary the gain of the green channel.
Compose Video Input (Pin 18)	This is the sync separator input pin. For Sync on Green systems, the green channel video signal should be AC coupled to pin 18 through a 0.1 μF capacitor.
Brightness Control (Pin 20)	If the LM1204 is used without blanking then this pin should be biased at 2.0 V_{DC}. Brightness control for all three video channels is now controlled by pin 43 (blank level adjust pin). See *Figure 4*. If the LM1204 is used with blanking then this pin allows the user to simultaneously DC offset the video portion of the output signals of all three channels thus allowing brightness control (See *Figure 5*).
Contrast Control (Pin 21)	This pin simultaneously controls the gain of all three video channels. A 0V to 4 V_{DC} input voltage is applied to this pin, with 0V corresponding to minimum gain (i.e., maximum attenuation of video signal) and 4V corresponding to maximum gain (i.e., minimum attenuation of the video signal).

Pin Descriptions (Continued)

Back Porch Clamp Width Adjust (Pin 22)	The LM1204 provides DC restoration or clamping during the back porch interval of the video signal. The width of LM1204's internally generated back porch clamp signal can be varied by applying a 0V to 4 V_{DC} voltage to this pin. The back porch clamp signal width can be varied from approximately 0.3 μs to 4.0 μs by applying 4V to 0.5V respectively. By connecting the blank gate input pin (pin 24) to V_{CC}, the back porch clamp pulse can be monitored on the −H Sync output pin (pin 26). See *Figures 4* and *5*. By connecting pin 22 to V_{CC}, the LM1204 functions as a non-gated amplifier requiring no clamping. See Section 4 under application hints for further information.
±H Sync In (Pin 23)	This is the external sync input pin, it accepts a negative or positive polarity signal, either horizontal sync or a composite sync (1.2 V_{PP} minimum amplitude). The LM1204 also provides a negative polarity (TTL compatible) horizontal sync or composite sync output on pin 26. If the composite video input (pin 18) is not used then an H Sync signal should be AC coupled to this pin through a 0.1 μF capacitor. The ±H Sync input has priority over the composite video input if both signals are present.
Blank Gate In (Pin 24)	This is the blank gate input pin. The LM1204 allows video blanking at the preamplifier. If blanking is desired then a TTL compatible, negative polarity blanking signal should be applied to this pin. During the blanking interval, all three video outputs are level shifted to the blank level set by the voltage at pin 43. If blanking is not required then, pin 24 should be biased at 4V. Connecting pin 24 to V_{CC} will cause pin 26 to output the internally generated back porch clamp signal. The user can observe the change in back porch width as the potential at pin 22 is varied (see *Figures 4* and *5*).
Integrator Cap (Pin 25)	A 0.1 μF capacitor should be connected from this pin to ground. This capacitor allows the LM1204 to integrate the ±H Sync input signal and genreate the proper polarity switch for −H Sync output.
−H Sync Out (Pin 26)	This output pin provides a negative polarity horizontal sync signal for other system uses. There is approximately 100 ns delay between the ±H Sync input signal at pin 23 and the −H Sync output signal at pin 26. Connecting pin 24 to V_{CC} will cause pin 26 to output the internally generated back porch clamp signal. The user can observe the change in back porch clamp pulse width as the potential at pin 22 is varied (See *Figures 4* and *5*).
G Feedback (Pin 28)	This is the cutoff adjustment input for the green video channel. The green video output signal from pin 30 is fed back to this input through a potentiometer thus allowing the user to individually adjust the cutoff (black reference) level for each gun. The signal level at this pin should be between 0.5V and 4V.
B Feedback (Pin 33)	This is the cutoff adjustment input for the blue video channel. The blue video output signal from pin 35 is fed back to this input through a potentiometer thus allowing the user to individually adjust the cutoff (black reference) level for each gun. The signal level at this pin should be between 0.5V and 4V.
R Feedback (Pin 38)	This is the cutoff adjustment input for the red video channel. The red video output signal from pin 40 is fed back to this input through a potentiometer thus allowing the user to individualy adjust the cutoff (black reference) level for each gun. The signal level at this pin should be between 0.5V and 4V.
G Video Output (Pin 30)	This is the green channel video output.
B Video Output (Pin 35)	This is the blue channel video output.
R Video Output (Pin 40)	This is the red channel video output.
G Blank Clamp Cap (Pin 32)	A 0.022 μF to 0.1 μF capacitor should be connected from this pin to ground. This capacitor allows blanking for the green video channel.
B Blank Clamp Cap (Pin 37)	A 0.022 μF to 0.1 μF capacitor should be connected from this pin to ground. This capacitor allows blanking for the blue video channel.
R Blank Clamp Cap (Pin 42)	A 0.022 μF to 0.1 μF capacitor should be connected from this pin to ground. This capacitor allows blanking for the red video channel.
Blank Level Adjust (Pin 43)	This pin serves two functions depending on whether the LM1204 is used with blanking or without blanking. If blanking is not selected then pin 20 should be biased at 2.0 V_{DC} and pin 43 assumes the role of brightness control. Varying the potential at pin 43 will simultaneously DC offset the video output signals of all three channels (See *Figure 4*). If the LM1204 is used with blanking then during the blanking interval, all three video output signals will be level shifted to the blank level. The desired blank level can be set by adjusting the potential at pin 43. Brightness control is now made possible by varying the potential at pin 20. Adjusting the brightness control DC offsets the video portion of the signal relative to the fixed blank level (all channels are affected simultaneously). See *Figure 5*.
GND (Pins 8, 12 16, 27, 29, 34, 39)	Ground. All ground pins must be connected to the ground plane.

Applications Hints

The LM1204 is a wideband video amplifier system designed specifically for high resolution RGB CRT monitors. The device includes circuitry for DC restoration of video signals and also allows contrast and brightness control. DC restoration is done during the back porch interval of the video signal. An internal sync separator generates a back porch clamp signal either from a "Sync on Green" signal applied to the composite video input (pin 18) or from an externally supplied ±H Sync signal . The LM1204 first looks at the ±H Sync input (pin 23), if an external horizontal sync signal is not present then the device syncs off the composite video input. The internally generated back porch clamp pulse width is user adjustable.

A blanking function is also included. This allows the user to cutoff the beam current in the CRT's guns during the blanking interval thereby preventing horizontal retrace lines from being visible. Normally blanking is done by applying a high voltage pulse at the grid. However, blanking at the cathode using the LM1204 leads to ease of design and lowered cost.

Figure 2 shows the block diagram of the green video channel and the control logic. The two modes of operation, with and without blanking, are described below in detail.

1.0 Operation without Blanking

For operation without blanking, the blank gate input (pin 24) should be connected to +4V. This causes the blank comparator to connect switch S2 to position Y (See *Figure 2*).

Furthermore, the brightness control input pin (pin 20) should be biased at a potential between 1V (Min) and 3.8V (Max), it is best to bias this pin at 2V. The video signal is AC coupled to the input of the LM1204 as shown for the green channel in *Figure 2*. During the back porch interval of the video signal (See *Figure 3*), the internally generated back porch clamping pulse goes low, causing switches S1A and S1B to be closed. The closure of S1A causes g_m1 to charge capacitor C2 to a potential determined by the DC voltage at pin 20. This allows g_m1 to set up an average DC bias for the AC coupled video signal at the input of A1. When the back porch clamping pulse is high, S1A and S1B are opened. With S1A open, g_m1 is effectively disconnected from C2, C2 now holds the DC bias voltage. The transconductance stage g_m1 therefore functions as a sample and hold device and holds the input of A1 at the desired DC bias.

The LM1204 uses black level clamping at the back porch of the video signal to accomplish DC restoration. The transconductance stage g_m2 is enabled during the back porch clamp period to provide a sample and hold function. During the back porch clamp period, DC feedback from LM1204's video output is compared with the voltage set by potentiometer R9. Depending on A2's output voltage, C6 is either charged or discharged so that the feedback loop consisting of g_m2 and A2 is stabilized and the output is clamped to the black level. All this occurs during the back porch clamp period. During the video portion of the signal, g_m2 is disabled and C6 holds the fixed black level reference voltage. The beginning of each new line on the raster always starts from a fixed reference black level thus restoring the DC component of each line.

A2 is a summing amplifier that adds a DC offset component from g_m2 to the video signal from the multiplier. Adjusting R9 will DC offset the output signals of all three channels thus providing brightness control. Individual cutoff adjustment for each channel is done by varying the feedback voltage at each of the R, G and B feedback inputs (Pins 38, 28 and 33). For example, cutoff adjustment for the green channel is done by potentiometer R8 shown in *Figure 2*.

Adjusting the contrast control (potentiometer R3 in *Figure 2*) varies the peak to peak amplitude (includes sync tip if present) of all three video output signals relative to their black reference level. The Δ Gain adjust (pins 9, 15 and 13 for R, G, and B channels respectively) allows the user to individually adjust the AC gain of each channel. For example the AC gain of the green channel is adjusted using potentiometer R5 as shown in *Figure 2*. Normally the red channel is set for maximum gain and the gains of the blue and green channels are reduced until white balance is achieved on the CRT monitor's screen. *Figure 4* shows the adjustments for operation without blanking.

2.0 Operation with Blanking

Much of what was discussed in Section 1.0 also applies when the LM1204 is used with the blanking function. However, there are notable differences as described herein. For operation with blanking, a TTL compatible blanking signal must be applied to the blank gate input (pin 24).

During the blanking period, the blanking comparator connects switch S2 to position X (See *Figure 2*). This causes the LM1204 to level shift the video output signal to the blank level. Adjusting R9 will adjust the blank level of all three channels. Individual blank level adjustment for each channel is done by varying the feedback voltage at each of the R, G and B feedback inputs (pin 38, 28 and 33). In *Figure 2* this is done by adjusting potentiometer R8 for the green channel.

During the video portion of the video signal, S2 is connected to position Y. Brightness control is now accomplished by varying the potential at the brightness control pin (pin 20). Adjusting R6 offsets the video portion of all three output signals relative to the fixed blank level, restoring the DC level of the video signal. *Figure 5* shows the adjustments for operation with blanking.

3.0 Stability Considerations

For optimum performance and stable operation, a double sided PC board with adequate ground plane is essential. Moreover, soldering the LM1204 on to the PC board will yield best results. Each supply pin (pins 2, 4, 6, 19, 31, 36, 41 and 44) should be bypassed with a 0.01 μF and a 0.1 μF capacitor connected as close to the supply pin as is possible.

When driving the LM1204 from a 75Ω video source, the cable is terminated with 75Ω to minimize reflections caused by transmission line effects. However, the input impedance of LM1204 is capacitive and is also affected by the stray capacitance of the PC board. Thus the input impedance is a function of frequency. This changes the impedance of the cable termination. This can introduce overshoot and ringing in LM1204's pulse response. A 100Ω resistor in series with the blocking capacitor at the video input will minimize overshoot and ringing (see *Figure 8*). The value of the resistor is empirically determined. 100Ω is a good starting value.

Since the LM1204 is a wide bandwidth amplifier with high gain at high frequencies, the device may oscillate when driving a large capacitive/inductive load. To prevent oscillation, the amplifier's gain is rolled off at high frequencies. This is accomplished by an RC network comprised of a resistor in

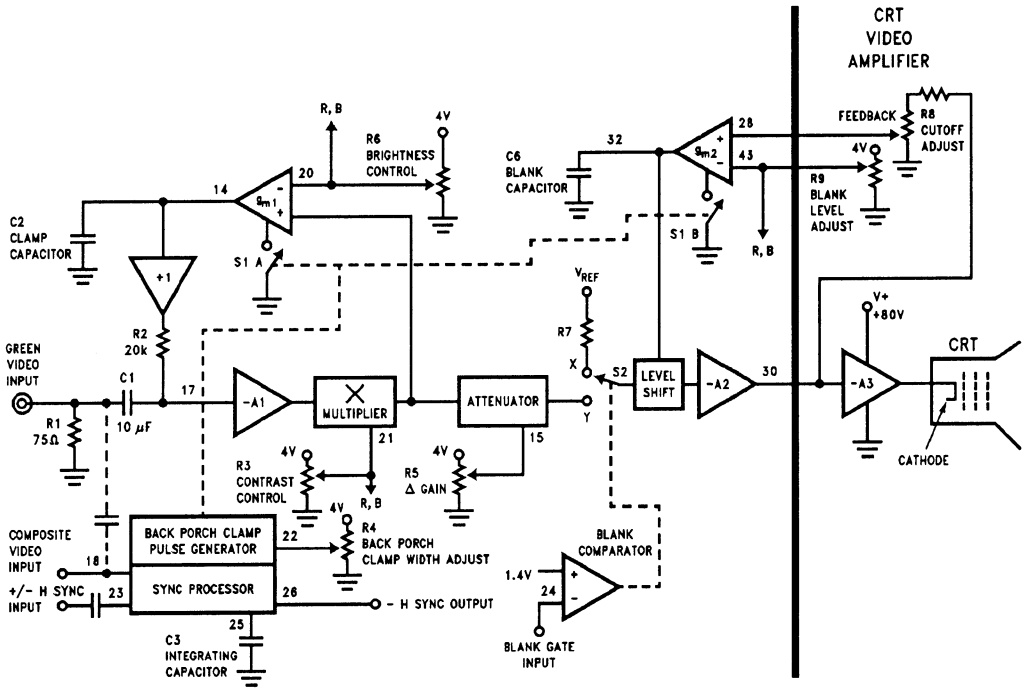
3.0 Stability Considerations (Continued)

series with a capacitor connected from the video output pin to ground (see Test Circuit, *Figure 1*). A 110Ω to 200Ω resistor in series with 10 pF is quite adequate for most applications. However, if oscillations don't cease then the value of the resistor should be decreased or the value of the capacitor should be increased or a combination of the two.

Non-Gated High Frequency Application

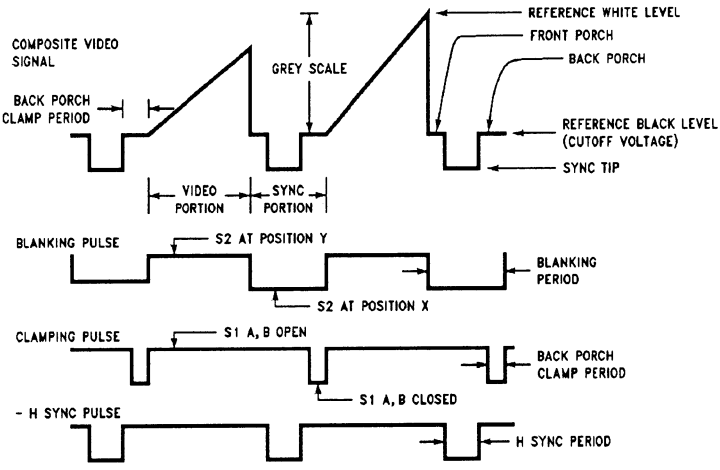
By connecting the back porch width adjust pin (pin 22) to V_{CC}, the LM1204 functions as a non-gated amplifier requiring no sync or blanking signals. *Figure 9* shows a triple high frequency amplifier with variable gain and DC offset control. In this mode of operation, filtered DC feedback must be provided to pins 28, 33 and 38 as shown in *Figure 9*.

LM1204



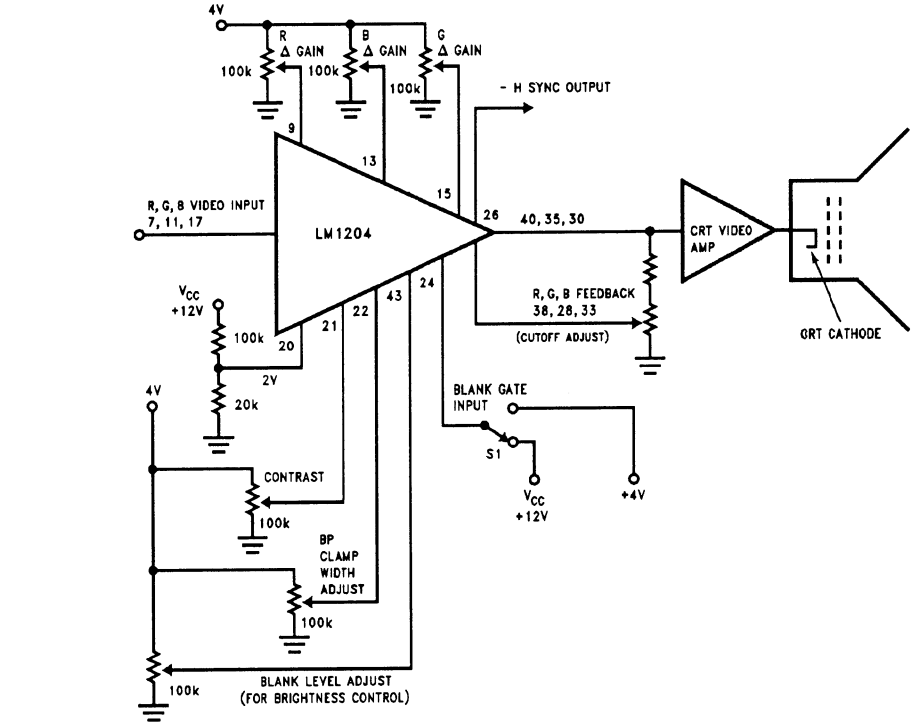
TL/H/11238-9

FIGURE 2. Block Diagram Showing Timing Circuitry and Green Video Channel



TL/H/11238-10

FIGURE 3. Composite Video and Timing Signals



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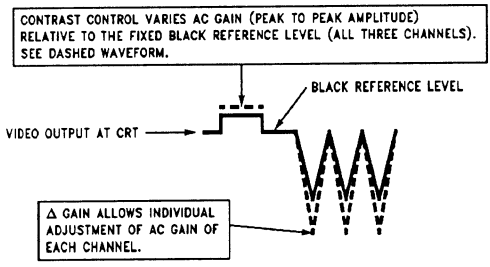

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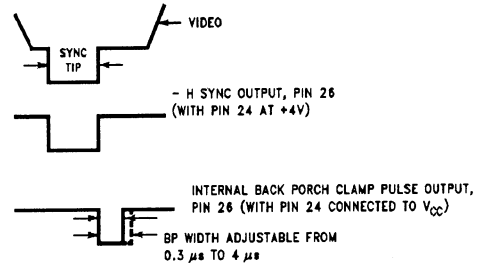
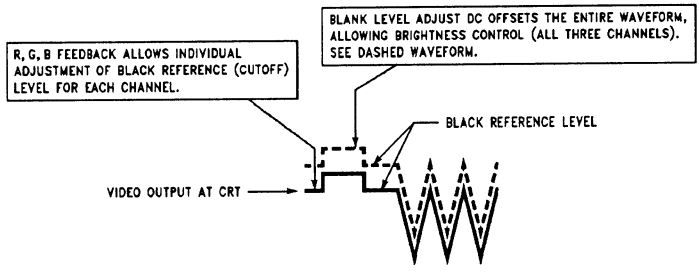
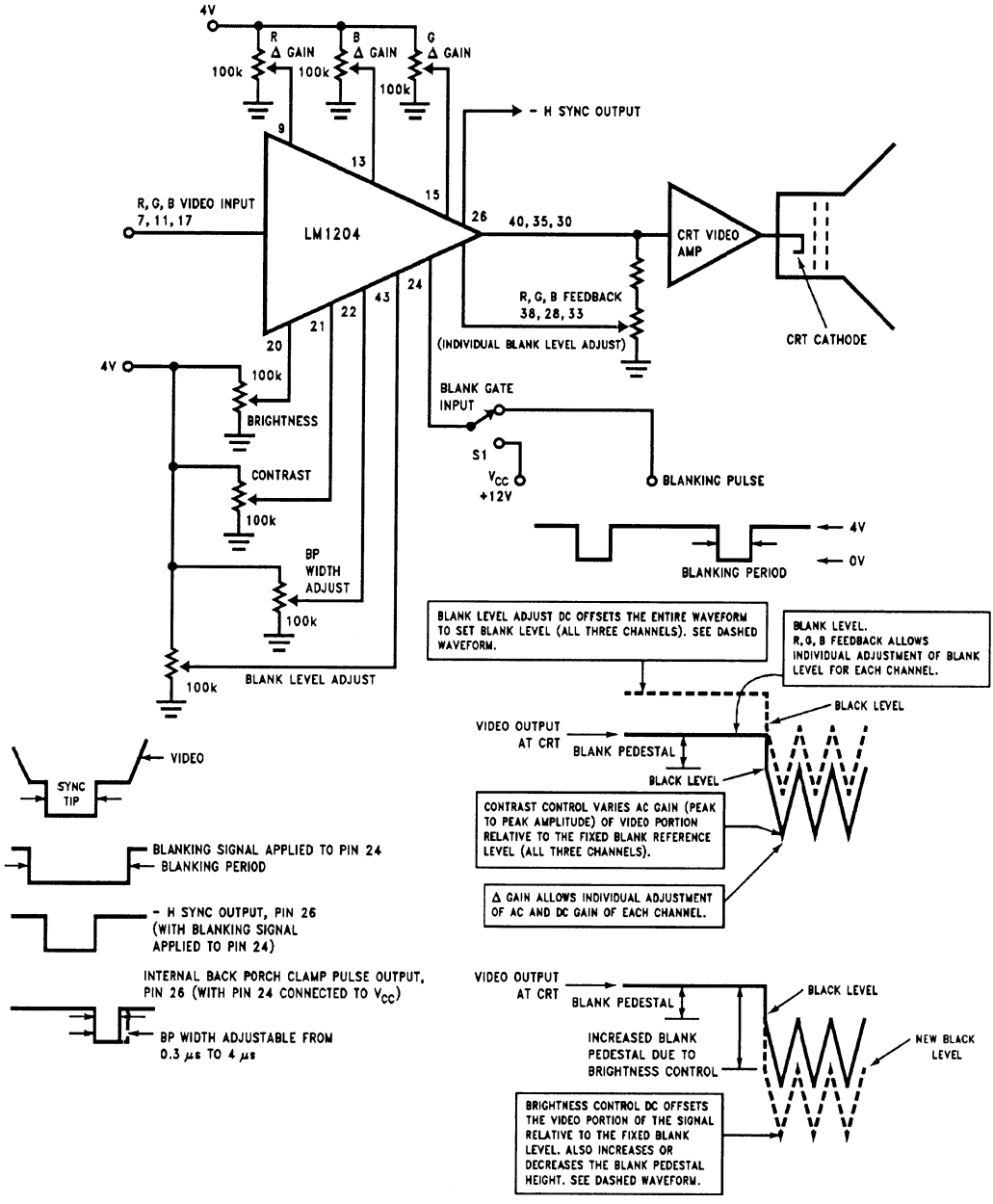


TL/H/11238–13



TL/H/11238–14

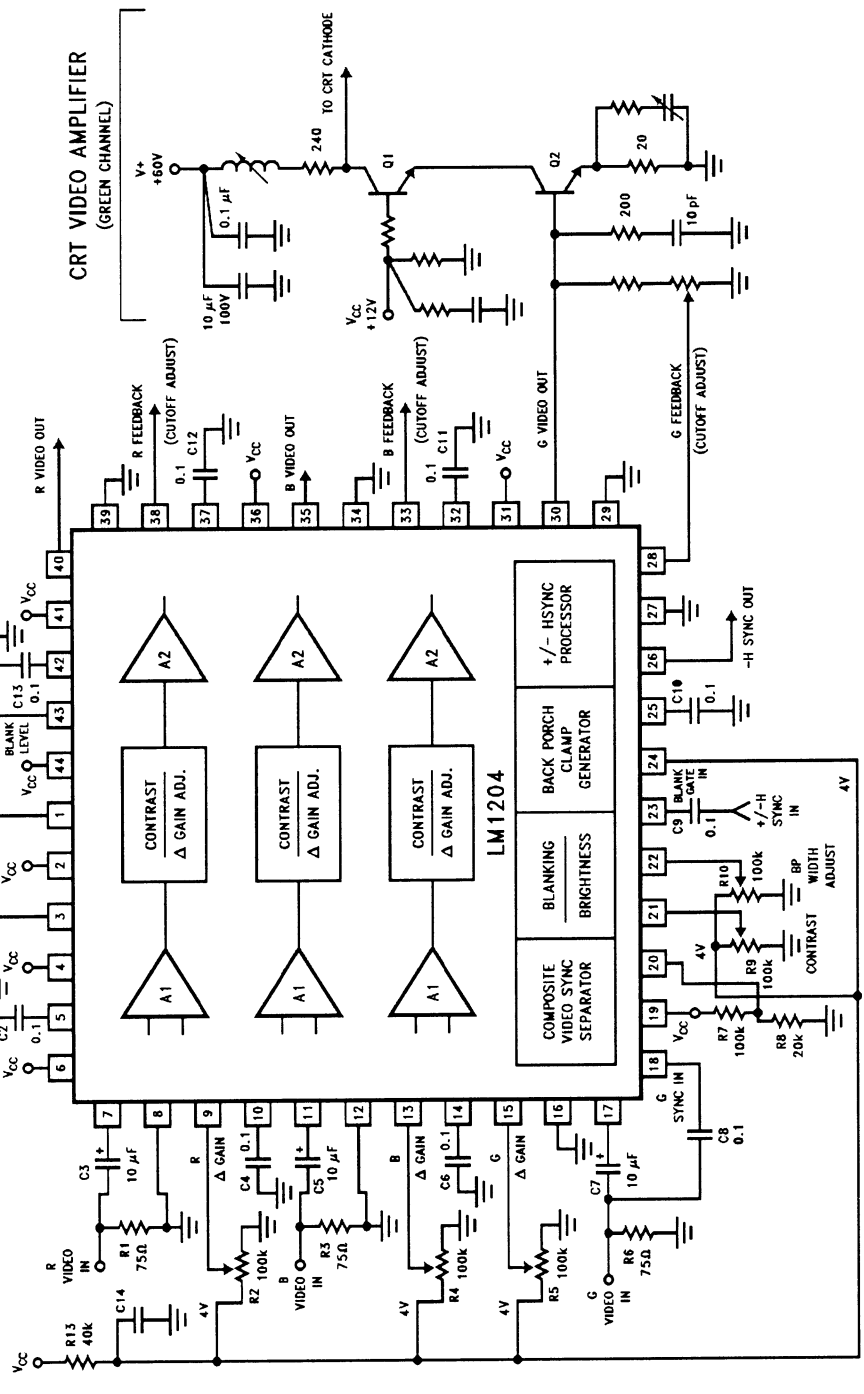
FIGURE 4. LM1204 Adjustments without Blanking



TL/H/11238–15

FIGURE 5. LM1204 Adjustments with Blanking

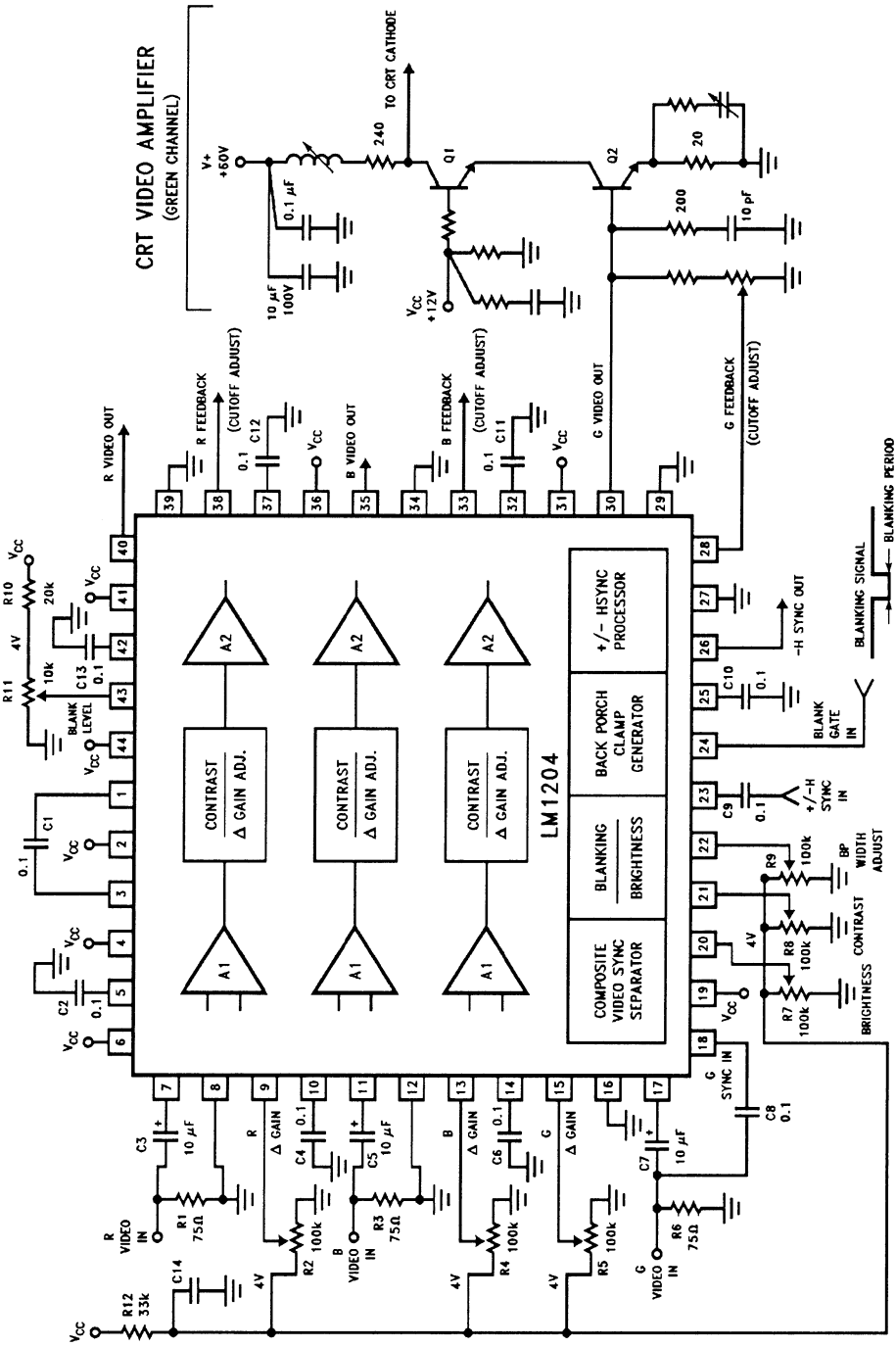
Typical Applications Circuits



TL/H/11238–16

FIGURE 6. The LM1204 driving cascode CRT video amplifiers and operating without blanking. Brightness control is accomplished by potentiometer R12 (See *Figure 4* for explanation of adjustments). Each V_{CC} pin should be bypassed with a 0.01 μF and a 0.1 μF capacitor connected as close to the pin as is possible.

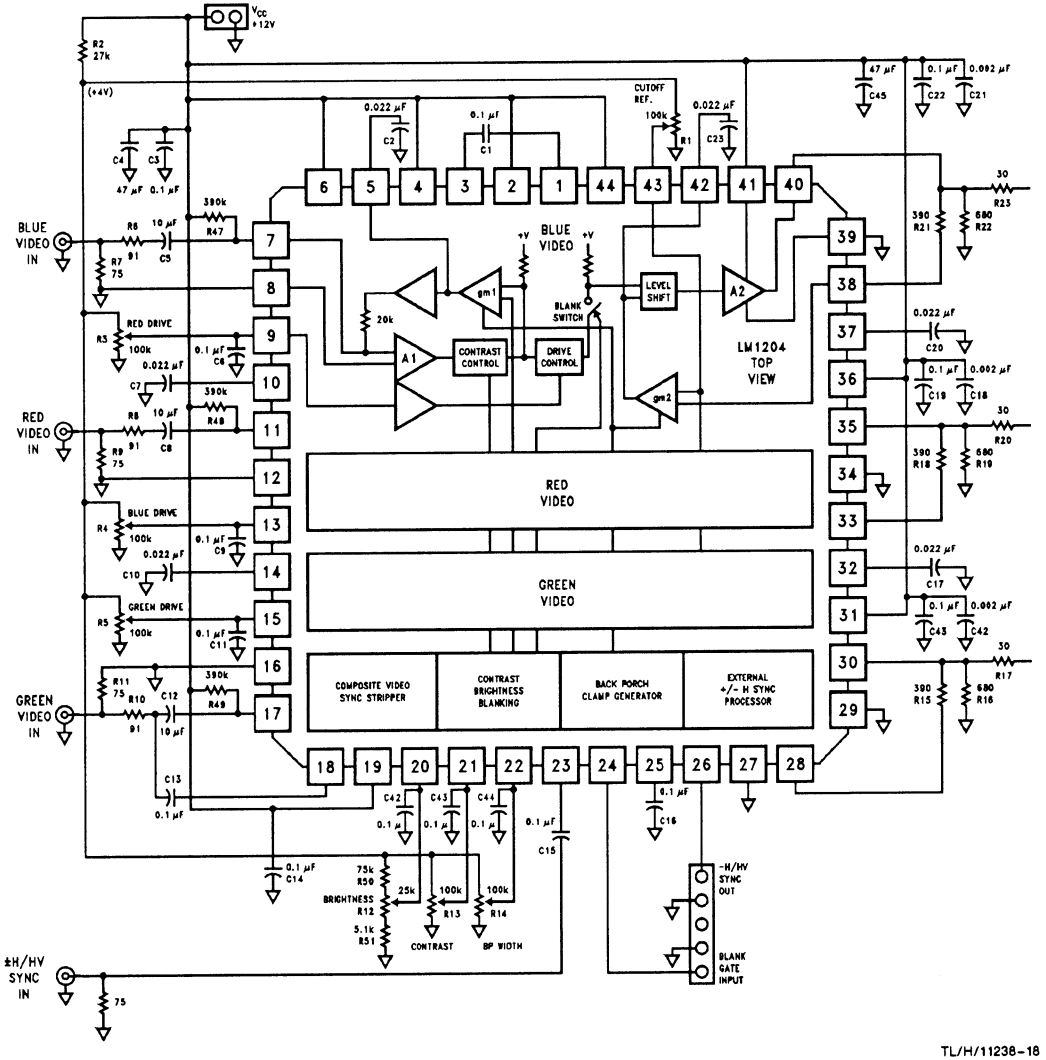
Typical Applications Circuits (Continued)



TL/H/11230–17

FIGURE 7. The LM1204 driving cascode CRT video amplifiers and operating with blanking. The video signal is level shifted to the user adjustable blank level during the blanking period. Brightness control DC offsets the video signal relative to the fixed blank level and is accomplished by potentiometer R7. See *Figure 5* for explanation of adjustments. Each V_{CC} pin should be bypassed with a 0.01 μF and a 0.1 μF capacitor connected as close to the pin as is possible.

Typical Applications Circuits (Continued)



TL/H/11238–18

FIGURE 8. Complete circuitry for an RGB CRT video board using the LM1204 and LH2426AS. The video output signals from LH2426AS are AC coupled and diode clamped to greater than 80V.

Typical Applications Circuits (Continued)

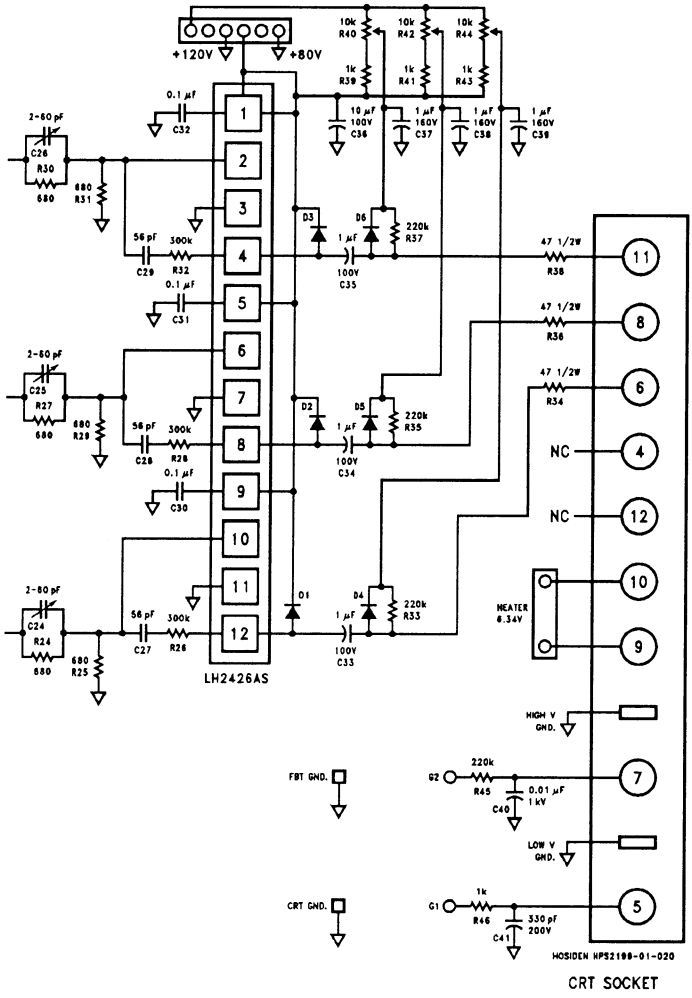


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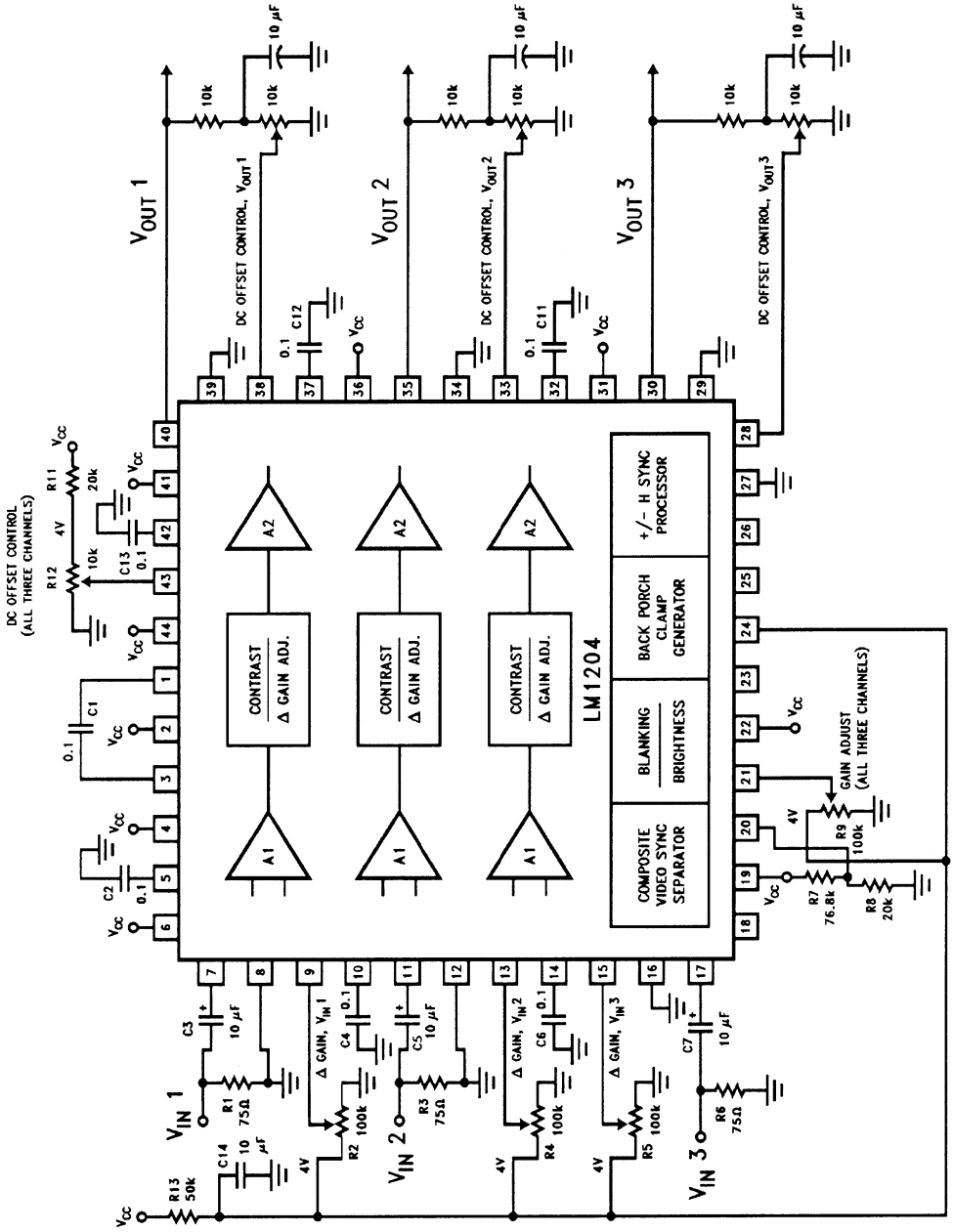
FIGURE 8. (Continued)

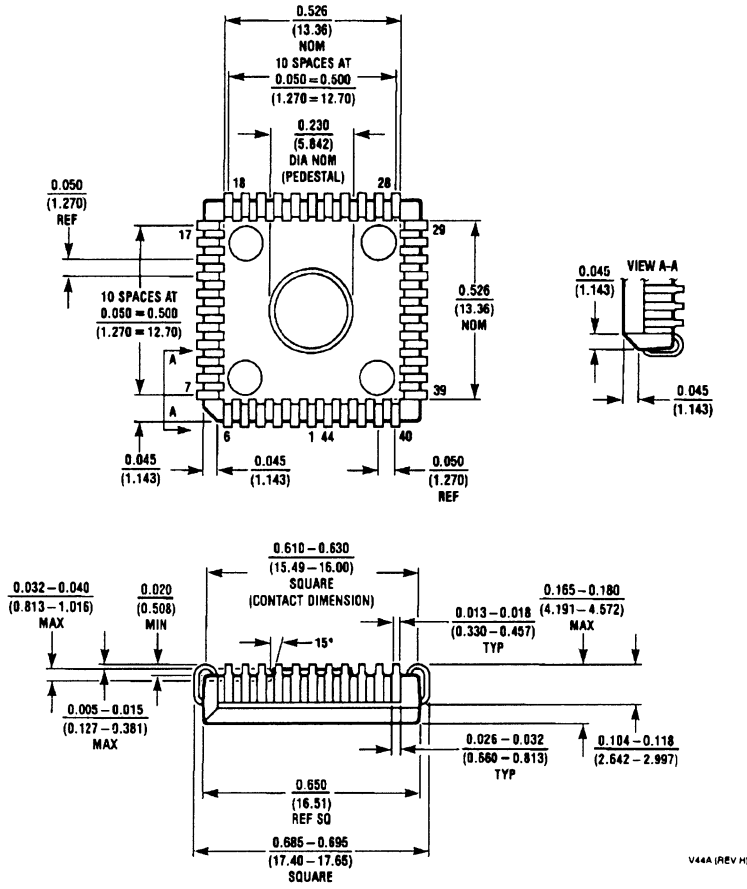
Typical Applications Circuits (Continued)



TL/H/11238–19

FIGURE 9. Three channel high frequency amplifier with gain and DC offset control (non-video application). Each V_{CC} pin should be bypassed with a 0.01 µF and a 0.1 µF capacitor connected as close to the pin as is possible.

Physical Dimensions inches (millimeters)



Order Number LM1204V
NS Package Number V44A

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National Semiconductor

July 1987

LM1391 Phase-Locked Loop

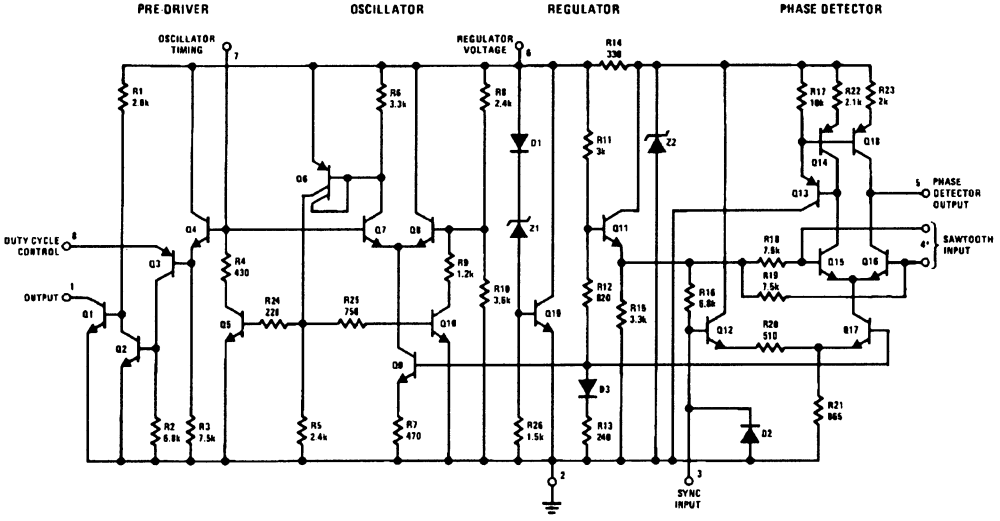
General Description

The LM1391 integrated circuit has been designed primarily for use in the horizontal section of TV receivers, but may find use in other low frequency signal processing applications. It includes a stable VCO, linear pulse phase detector, and variable duty cycle output driver.

Features

- Internal active regulator for improved supply rejection
- Uncommitted collector of output transistor
- Output transistor with low saturation and high voltage swing
- APC of the oscillator with a synchronizing signal
- DC controlled output duty cycle
- ±300 Hz typical pull-in
- Linear balanced phase detector
- Low thermal frequency drift
- Small static phase error
- Adjustable DC loop gain

Schematic Diagram



TL/H/7889–1

(*) Pin 4 Base of Q16 (LM1391) for use with (+) flyback pulse

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Current	40 mA_{DC}
Output Voltage	40 V_{DC}
Output Current	30 mA_{DC}
Sync Input Voltage (Pin 3)	5.0 Vp-p
Flyback Input Voltage (Pin 4)	5.0 Vp-p
Power Dissipation (Package Limitation) Plastic Package (Note 1)	1000 mW
Operating Temperature Range (Ambient)	0°C to + 70°C
Storage Temperature Range	−65°C to + 150°C
Lead Temperature (Soldering, 10 sec.)	260°C

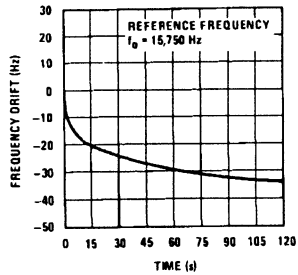
Electrical Characteristics T_A = 25°C (see test circuit, all switches in position 1)

Parameter	Conditions	Min	Typ	Max	Units
Regulated Voltage (Pin 6)	I_6 = 22 mA_{DC}	8.0	8.6	9.2	V_{DC}
Supply Current (Pin 6)			20		mA_{DC}
Collector-Emitter Saturation Voltage of Output Transistor (Pin 1)	I_{C1} = 20 mA		0.30	0.40	V_{DC}
Pin 4 Voltage			2.0		V_{DC}
Oscillator Pull-in Range	Adjust R_H		± 300		Hz
Oscillator Hold-in Range	Adjust R_H		± 900		Hz
Static Phase Error	Δf = 300 Hz		0.5		μs
Free-running Frequency Supply Dependance	S1 in position 2		± 3.0		Hz/V_{DC}
Phase Detector Leakage (Pin 5)	All switches in position 2			± 1.0	μA
Sync Input Voltage (Pin 3)		2.0		5.0	Vp-p
Sawtooth Input Voltage (Pin 4)		1.0		3.0	Vp-p
Maximum Oscillator Frequency			500		kHz

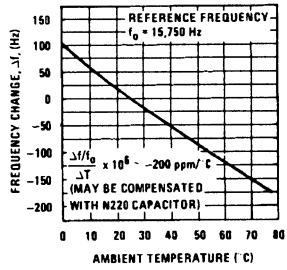
Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 120°C/W junction to ambient.

Typical Performance Characteristics

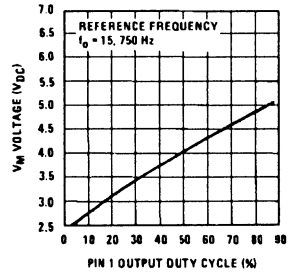
Frequency Drift vs Warm-Up Time



Frequency vs Temperature



Output Duty Cycle vs V_M Voltage



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Application Information

The following equations may be considered when using the LM1391 in a particular application.

$$R201 = R301 = \frac{V_{CC} - 8.6}{0.02}\ \Omega$$

$$f_O \cong \frac{1}{0.6\ R_O C_O}\ \text{Hz}\quad 1.5k \le R_O < 51k$$

$$R204 \cong 10\ R_O$$

$$C203 = C204 \cong \frac{1}{600\ f_O(\text{Hz})}\ \text{F}$$

DC Loop Gain $\mu\beta \cong 3.2 \times 10^{-5}\ R_O f_O$ Hz/rad

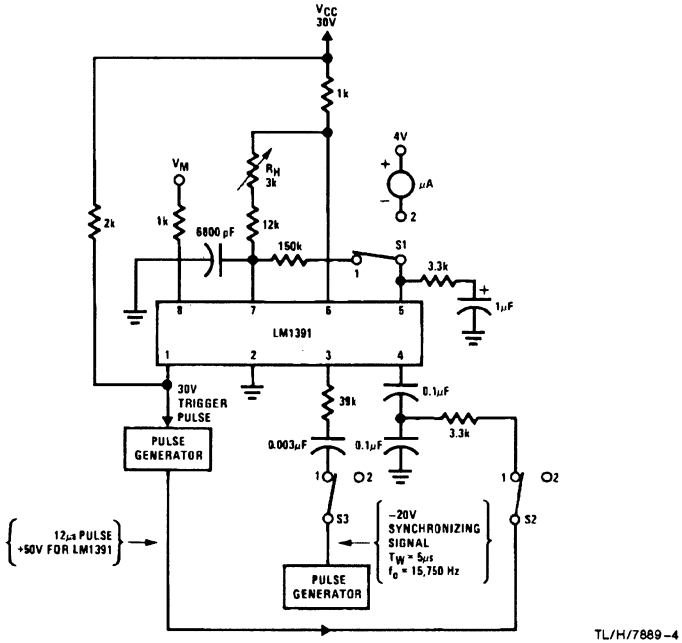
Noise Bandwidth

$$f_{nn} \cong \frac{1 + 2\pi \frac{R_X^2}{R_Y} C_C\ \mu\beta}{4 R_X C_C}\ \text{Hz}$$

Damping Factor

$$K \cong \frac{\pi}{2} \frac{R_X^2}{R_Y} C_C\ \mu\beta$$

Test Circuit



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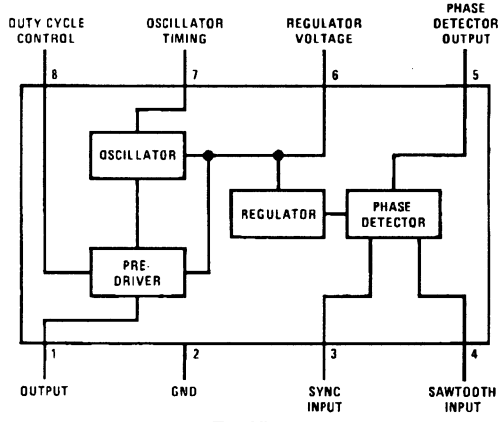
Connection Diagram

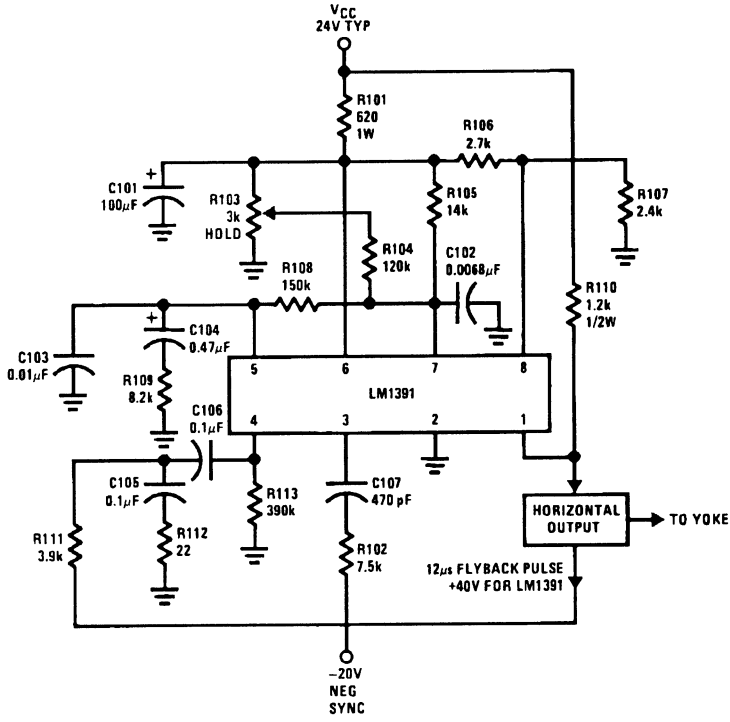
Dual-In-Line Package



TL/H/7889–2

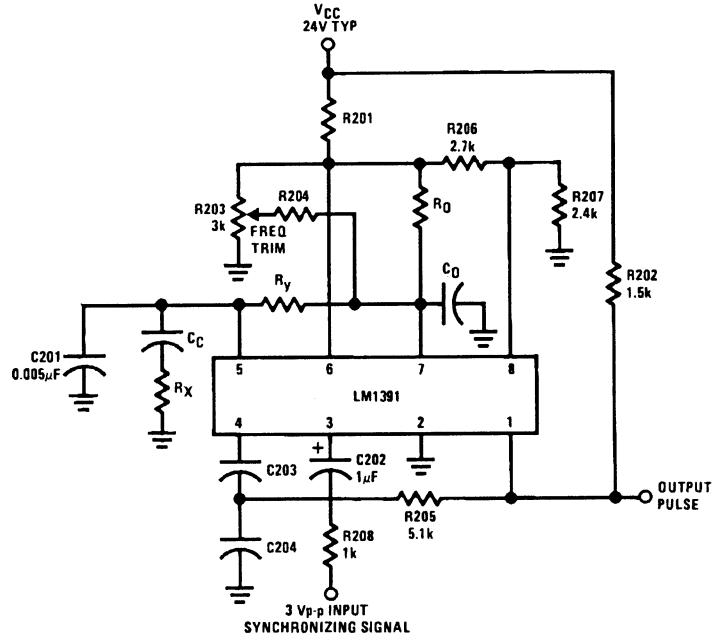
Top View
Order Number LM1391N
See NS Package Number N08E

Typical Applications



TL/H/7889–5

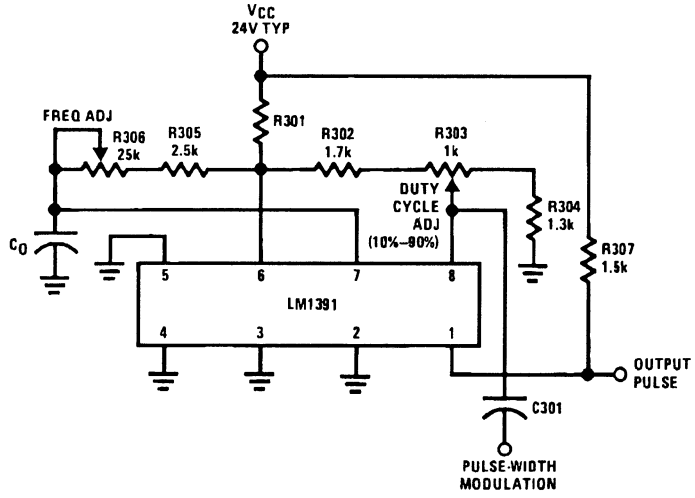
FIGURE 1. TV Horizontal Processor



TL/H/7889–6

FIGURE 2. General Purpose Phase-Lock Loop
(See Applications Information)

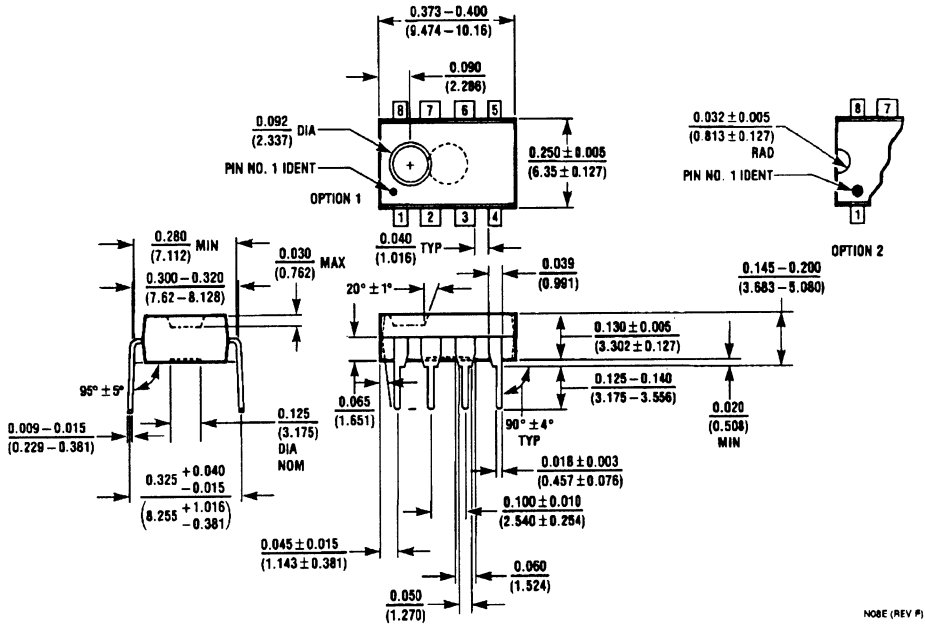
Typical Applications (Continued)



TL/H/7889–7

FIGURE 3. Variable Duty Cycle Oscillator (See Applications Information)

Physical Dimensions inches (millimeters)



Molded Dual-In-Line Package (N)
Order Number LM1391N
NS Package Number N08E

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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PRELIMINARY
April 1989

LM1881 Video Sync Separator

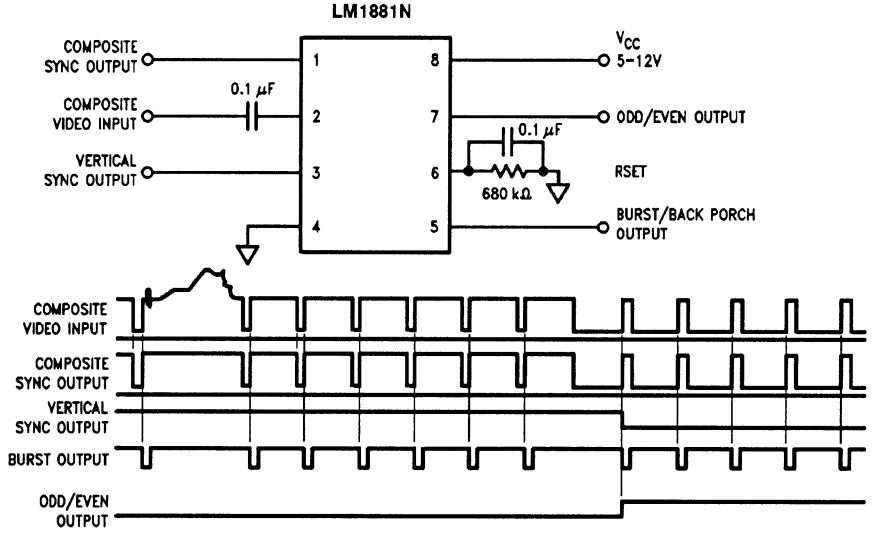
General Description

The LM1881 Video sync separator extracts timing information including composite and vertical sync, burst/back porch timing, and odd/even field information from standard negative going sync NTSC, PAL®, and SECAM video signals with amplitude from 0.5V to 2V p-p. The integrated circuit is also capable of providing sync separation for non-standard, faster horizontal rate video signals by changing an external horizontal scan rate setting resistor. The vertical output is produced on the rising edge of the first serration in the vertical sync period. A default vertical output is produced after a time delay if the rising edge mentioned above does not occur within the internally set delay period, such as might be the case for a non-standard video signal.

Features

- AC coupled composite input signal
- >10 kΩ input resistance
- <10 mA power supply drain current
- Composite sync and vertical outputs
- Odd/even field output
- Burst gate/back porch output
- Resistor programmable horizontal scan rate (up to 64 kHz)
- Edge triggered vertical output
- Default triggered vertical output for non-standard video signal (video games-home computers)

Connection Diagram



TL/H/9150–1

Order Number LM1881M or LM1881N
See NS Package Number M08A or N08E

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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	13.2V
Input Voltage	3 Vp-p
Output Sink Currents; Pins 1, 3, 5	5 mA
Output Sink Current; Pin 7	2 mA
Package Dissipation (Note 1)	1100 mW
Operating Temperature Range	0°C − 70°C
Storage Temperature Range	−65°C to +150°C
ESD Susceptibility (Note 2)	2 kV
Soldering Information	
Dual-In-Line Package (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics

V_{CC} = 5V; Rset = 680 kΩ; T_A = 25°C; Unless otherwise specified

Parameter	Conditions		Typ	Tested Limit (Note 3)	Design Limit (Note 4)	Units (Limits)
Supply Current	Outputs at Logic 1	V_{CC} = 5V	5.2	10		mAmax
		V_{CC} = 12V	5.5	12		mAmax
DC Input Voltage	Pin 2		1.5	1.3		Vmin
				1.8		Vmax
Input Threshold Voltage	Note 5		70	55		mVmin
				85		mVmax
Input Discharge Current	Pin 2; V_{IN} = 2V		11	6		μAmin
				16		μAmax
Input Clamp Charge Current	Pin 2; V_{IN} = 1V		0.8	0.2		mAmin
R_{SET} Pin Reference Voltage	Pin 6; Note 6		1.22	1.10		Vmin
				1.35		Vmax
Composite Sync. & Vertical Outputs	I_{OUT} = 40 μA; Logic 1	V_{CC} = 5V	4.5	4.0		Vmin
		V_{CC} = 12V		11.0		Vmin
	I_{OUT} = 1.6 mA Logic 1	V_{CC} = 5V	3.6	2.4		Vmin
		V_{CC} = 12V		10.0		Vmin
Burst Gate & Odd/Even Outputs	I_{OUT} = 40 μA; Logic 1	V_{CC} = 5V	4.5	4.0		Vmin
		V_{CC} = 12V		11.0		Vmin
Composite Sync. Output	I_{OUT} = −1.6 mA; Logic 0; Pin 1		0.2	0.8		Vmax
Vertical Sync. Output	I_{OUT} = −1.6 mA; Logic 0; Pin 3		0.2	0.8		Vmax
Burst Gate Output	I_{OUT} = −1.6 mA; Logic 0; Pin 5		0.2	0.8		Vmax
Odd/Even Output	I_{OUT} = −1.6 mA; Logic 0; Pin 7		0.2	0.8		Vmax
Vertical Sync Width			230	190		μsmin
				300		μsmax
Burst Gate Width	2.7 kΩ from Pin 5 to V_{CC}		4	2.5		μsmin
				4.7		μsmax
Vertical Default Time	Note 7		65	32		μsmin
				90		μsmax

Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a package thermal resistance of 110° C/W, junction to ambient.

Note 2: ESD susceptibility test uses the "human body model, 100 pF discharged through a 1.5 kΩ resistor".

Note 3: Typicals are at T_J = 25°C and represent the most likely parametric norm.

Note 4: Tested Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

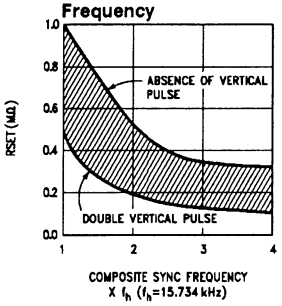
Note 5: Relative difference between the input clamp voltage and the minimum input voltage which produces a horizontal output pulse.

Note 6: Careful attention should be made to prevent parasitic capacitance coupling from any output pin (Pins 1, 3, 5, and 7) to the R_{SET} pin (Pin 6).

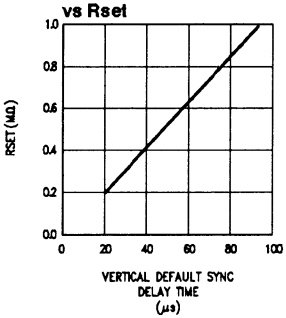
Note 7: Delay time between the start of vertical sync (at input) and the vertical output pulse.

Typical Performance Characteristics

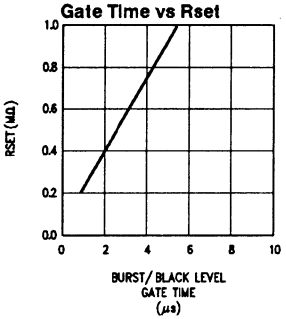
Rset Value Selection vs Composite Sync Frequency



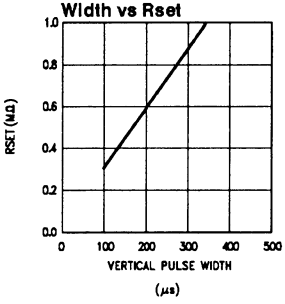
Vertical Default Sync Delay Time vs Rset



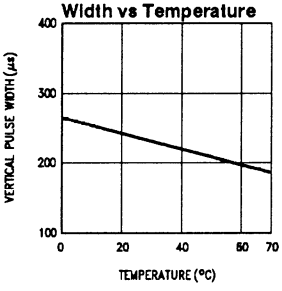
Burst/Black Level Gate Time vs Rset



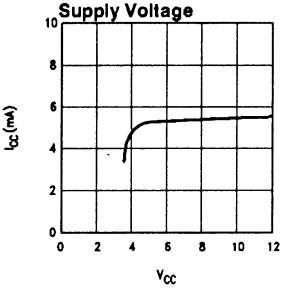
Vertical Pulse Width vs Rset



Vertical Pulse Width vs Temperature



Supply Current vs Supply Voltage



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Application Notes

The LM1881 is designed to strip the synchronization signals from composite video sources that are in, or similar to, the N.T.S.C. format. Input signals with positive polarity video (increasing signal voltage signifies increasing scene brightness) from 0.5V (p-p) to 2V (p-p) can be accommodated. The LM1881 operates from a single supply voltage between 5V DC and 12V DC. The only required external components beside power supply and set current decoupling are the input coupling capacitor and a single resistor that sets internal current levels, allowing the LM1881 to be adjusted for source signals with line scan frequencies differing from 15.734 kHz. Four major sync signals are available from the I/C: composite sync including both horizontal and vertical scan timing information; a vertical sync pulse; a burst gate or back porch clamp pulse; and an odd/even output. The odd/even output level identifies which video field of an interlaced video source is present at the input. The outputs from the LM1881 can be used to gen-lock video camera/VTR signals with graphics sources, provide identification of video fields for memory storage, recover suppressed or contaminated sync signals, and provide timing references for the extraction of coded or uncoded data on specific video scan lines.

To better understand the LM1881 timing information and the type of signals that are used, refer to *Figure 2(a–e)* which shows a portion of the composite video signal from the end of one field through the beginning of the next field.

COMPOSITE SYNC OUTPUT

The composite sync output, *Figure 2(b)*, is simply a reproduction of the signal waveform below the composite video black level, with the video completely removed. This is obtained by clamping the video signal sync tips to 1.5V DC at Pin 2 and using a comparator threshold set just above this voltage to strip the sync signal, which is then buffered out to Pin 1. The threshold separation from the clamped sync tip is nominally 70 mV which means that for the minimum input level of 0.5V (p-p), the clipping level is close to the halfway point on the sync pulse amplitude (shown by the dashed line on *Figure 2(a)*). This threshold separation is independent of the signal amplitude, therefore, for a 2V (p-p) input the clipping level occurs at 11% of the sync pulse amplitude. The charging current for the input coupling capacitor is 0.8 mA, whereas the discharge current is only 11 μA, typically. This allows relatively small capacitor values to be used—0.1 μF is generally recommended.

Normally the signal source for the LM1881 is assumed to be clean and relatively noise-free, but some sources may have excessive video peaking, causing high frequency video and chroma components to extend below the black level reference. Some video discs keep the chroma burst pulse present throughout the vertical blanking period so that the burst actually appears on the sync tips for three line periods instead of at black level. A clean composite sync signal can be generated from these sources by filtering the input signal. When the source impedance is low, typically 75Ω, a 620Ω resistor in series with the source and a 510 pF capacitor to ground will form a low pass filter with a corner frequency of 500 kHz. This bandwidth is more than sufficient to pass the sync pulse portion of the waveform; however, any subcarrier content in the signal will be attenuated by almost 18 dB, effectively taking it below the comparator threshold. Filtering will also help if the source is contaminated with thermal noise. The output waveforms will become delayed from between 40 ns to as much as 200 ns due to this filter. This much delay will not usually be significant but it does contribute to the sync delay produced by any additional signal processing. Since the original video may also undergo processing, the need for time delay correction will depend on the total system, not just the sync stripper.

VERTICAL SYNC OUTPUT

A vertical sync output is derived by internally integrating the composite sync waveform *(Figure 3)*. Horizontal sync pulses are not able to charge the integrating capacitor sufficiently because of their short duty cycle, but when the vertical retrace interval is reached, the broad serrated pulse charges the capacitor past a fixed threshold. Once the threshold is reached, the next serration in the sync waveform triggers an R-S flipflop and starts the vertical output pulse at Pin 3. Simultaneously an internal oscillator begins clocking a counter. When a count of eight is reached the vertical output pulse is terminated and the circuit resets. Both the time required to reach the integrator threshold and the period of the oscillator are programmed by an external resistor at Pin 6. For an N.T.S.C. signal with 32 μs between serrations, a 680 kΩ resistor will ensure the vertical output pulse will start coincident with the leading edge of the first vertical serration *(Figure 2c)*. If the resistor value gets too small it becomes possible for the oscillator circuit to time out before the input vertical sync period has ended. When this is the case, the sequence will repeat and a double vertical output pulse will appear. Therefore, the resistor value for a given horizontal scan rate is chosen small enough to trigger the vertical output pulse on the first serration yet not so small as to give a double pulse, rather than attempting to choose a value that gives a specific output pulse width. If the incoming vertical sync is not serrated, the integrating capacitor is allowed to charge to a second threshold which automatically initiates the vertical output pulse sequence. In this instance, the start of the vertical pulse as well as the pulse period will be dependent on the resistor value.

ODD/EVEN FIELD PULSE

An unusual feature of LM1881 is an output level from Pin 7 that identifies the video field present at the input to the LM1881. This can be useful in frame memory storage applications or in extracting test signals that occur only in alternate fields. For a composite video signal that is interlaced, one of the two fields that make up each video frame or picture must have a half horizontal scan line period at the end of the vertical scan—i.e., at the bottom of the picture. This is called the "odd field" or "field 1". The "even field" or "field 2" has a complete horizontal scan line at the end of the field. An odd field starts on the leading edge of the first equalizing pulse, whereas the even field starts on the leading edge of the second equalizing pulse of the vertical retrace interval. *Figure 2(a)* shows the end of the even field and the start of the odd field.

To detect the odd/even fields the LM1881 again integrates the composite sync waveform *(Figure 3)*. A capacitor is charged during the period between sync pulses and discharged when the sync pulse is present. The period between normal horizontal sync pulses is enough to allow the capacitor voltage to reach a threshold level of a comparator that clears a flipflop which is also being clocked by the sync waveform. When the vertical interval is reached, the shorter integration time between equalizing pulses prevents this

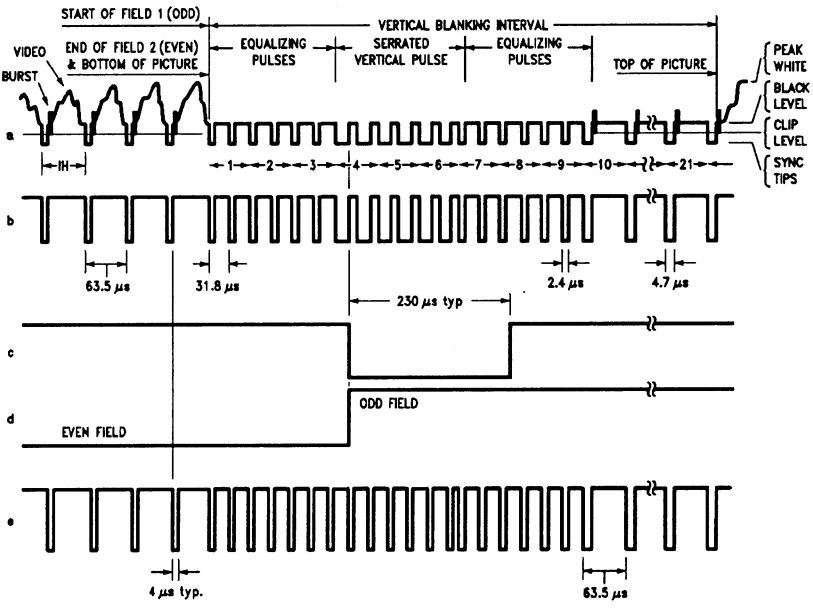

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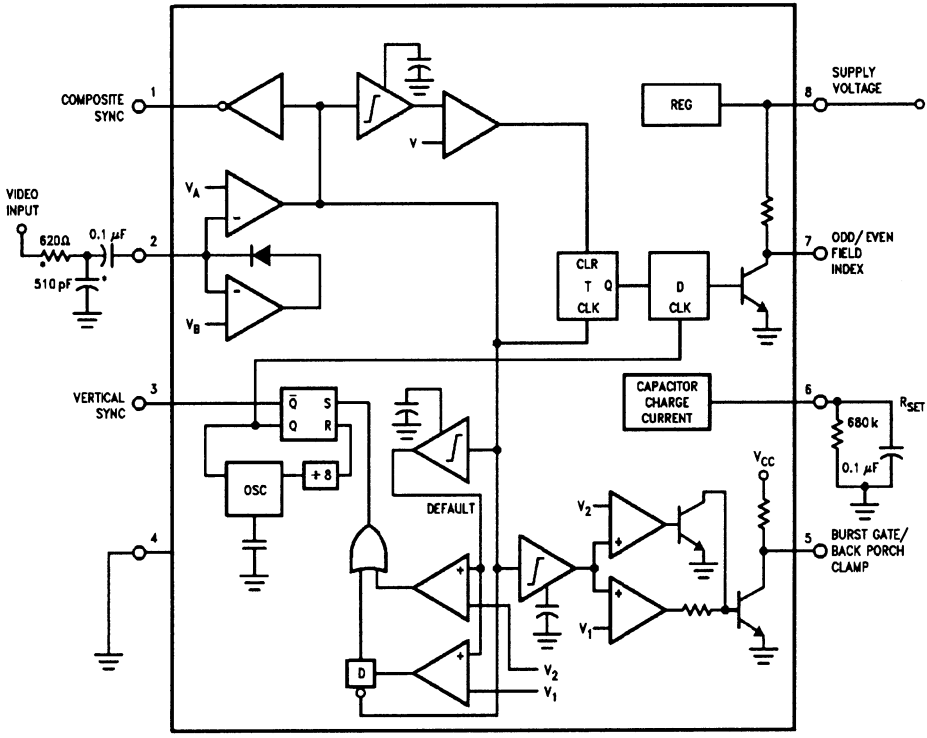
FIGURE 2. (a) Composite Video; (b) Composite Sync; (c) Vertical Output Pulse; (d) Odd/Even Field Index; (e) Burst Gate/Back Porch Clamp



*Components Optional, See Text

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FIGURE 3

threshold from being reached and the Q output of the flip-flop is toggled with each equalizing pulse. Since the half line period at the end of the odd field will have the same effect as an equalizing pulse period, the Q output will have a different polarity on successive fields. Thus by comparing the Q polarity with the vertical output pulse, an odd/even field index is generated. Pin 7 remains low during the even field and high during the odd field.

BURST/BACKPORCH OUTPUT PULSE

In a composite video signal, the chroma burst is located on the backporch of the horizontal blanking period. This period, approximately 4.8 μs long, is also the black level reference for the subsequent video scan line. The LM1881 generates a pulse at Pin 5 that can be used either to retrieve the chroma burst from the composite video signal (thus providing a subcarrier synchronizing signal) or as a clamp for the DC restoration of the video waveform. This output is obtained simply by charging an internal capacitor starting on the trailing edge of the horizontal sync pulses. Simultaneously the output of Pin 5 is pulled low and held until the capacitor charge circuit times out—4 μs later. A shorter output burst gate pulse can be derived by differentiating the burst output using a series C-R network. This may be necessary in applications which require high horizontal scan rates in combination with normal (60–120 Hz) vertical scan rates.

APPLICATIONS

Apart from extracting a composite sync signal free of video information, the LM1881 outputs allow a number of interesting applications to be developed. As mentioned above, the burst gate/backporch clamp pulse allows DC restoration of the original video waveform for display or remodulation on an R.F. carrier, and retrieval of the color burst for color synchronization and decoding into R.G.B. components. For frame memory storage applications, the odd/even field level allows identification of the appropriate field ensuring the correct read or write sequence. The vertical pulse output is particularly useful since it begins at a precise time—the rising edge of the first vertical serration in the sync waveform. This means that individual lines within the vertical blanking period (or anywhere in the active scan line period) can easily be extracted by counting the required number of transitions in the composite sync waveform following the start of the vertical output pulse.

The vertical blanking interval is proving popular as a means to transmit data which will not appear on a normal T.V. receiver screen. Data can be inserted beginning with line 10 (the first horizontal scan line on which the color burst appears) through to line 21. Usually lines 10 through 13 are not used which leaves lines 14 through 21 for inserting signals, which may be different from field to field. In the U.S., line 19 is normally reserved for a vertical interval reference signal (VIRS) and line 21 is reserved for closed caption data for the hearing impaired. The remaining lines are used in a number of ways. Lines 17 and 18 are frequently used during studio processing to add and delete vertical interval test signals (VITS) while lines 14 through 18 and line 20 can be used for Videotex/Teletext data. Several institutions are proposing to transmit financial data on line 17 and cable systems use the available lines in the vertical interval to send decoding data for descrambler terminals.

Since the vertical output pulse from the LM1881 coincides with the leading edge of the first vertical serration, sixteen positive or negative transitions later will be the start of line 14 in either field. At this point simple counters can be used to select the desired line(s) for insertion or deletion of data.

VIDEO LINE SELECTOR

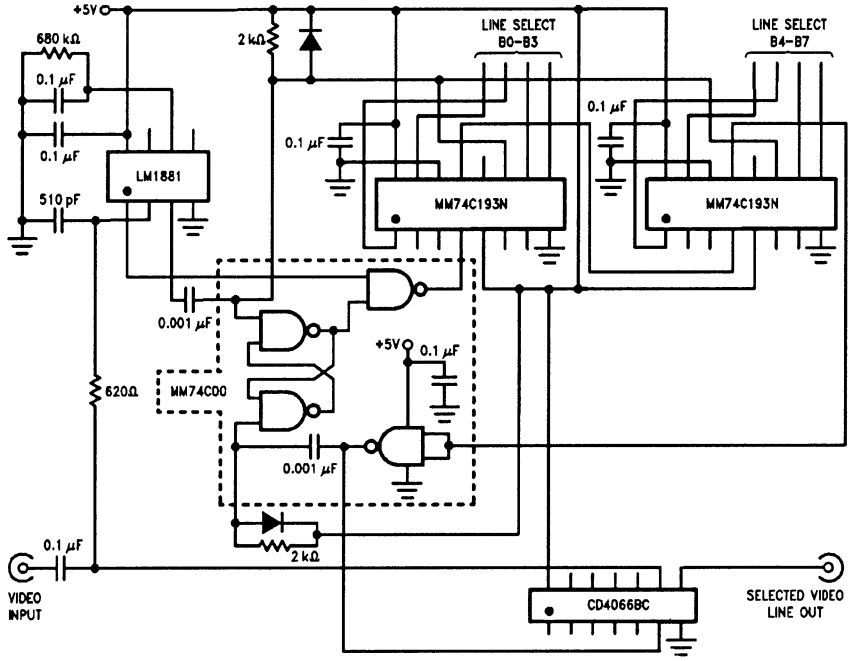
The circuit in *Figure 4* puts out a single video line according to the binary coded information applied to line select bits b0–b7. A line is selected by adding two to the desired line number, converting to a binary equivalent and applying the result to the line select inputs. The falling edge of the LM1881's vertical pulse is used to load the appropriate number into the counters (MM74C193N) and to set a start count latch using two NAND gates. Composite sync transitions are counted using the borrow out of the desired number of counters. The final borrow out pulse is used to turn on the analog switch (CD4066BC) during the desired line. The falling edge of this signal also resets the start count latch, thereby terminating the counting.

The circuit, as shown, will provide a single line output for each field in an interlaced video system (television) or a single line output in each frame for a non-interlaced video system (computer monitor). When a particular line in only one field of an interlaced video signal is desired, the odd/even field index output must be used instead of the vertical output pulse (invert the field index output to select the odd field). A single counter is needed for selecting lines 3 to 14; two counters are needed for selecting lines 15 to 253; and three counters will work for up to 2046 lines. An output buffer is required to drive low impedance loads.

MULTIPLE CONTIGUOUS VIDEO LINE SELECTOR WITH BLACK LEVEL RESTORATION

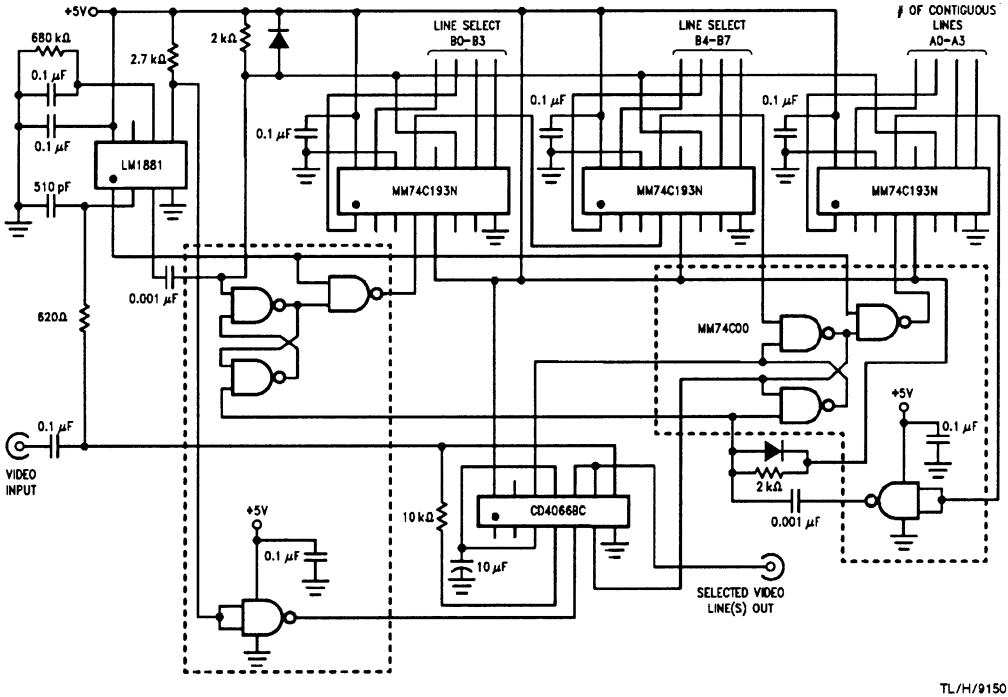
The circuit in *Figure 5* will select a number of adjoining lines starting with the line selected as in the previous example. Additional counters can be added as described previously for either higher starting line numbers or an increased number of contiguous output lines. The back porch pulse output of the LM1881 is used to gate the video input's black level through a low pass filter (10 kΩ, 10 μF) providing black level restoration at the video output when the output selected line(s) is not being gated through.

Typical Applications



TL/H/9150–5

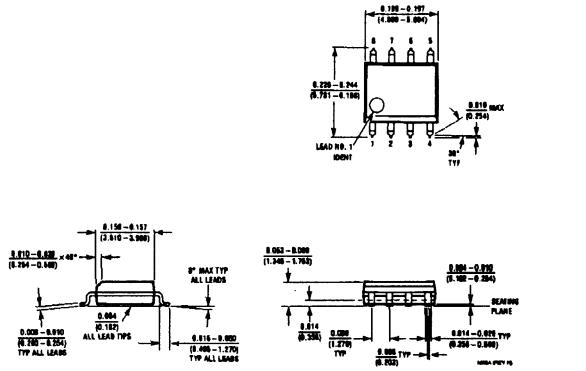
FIGURE 4. Video Line Selector



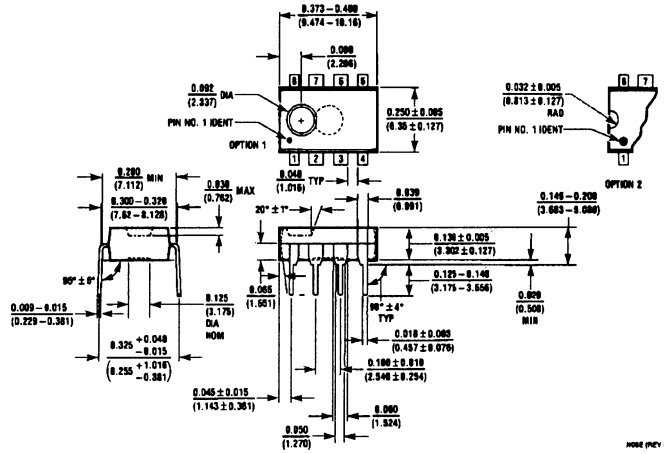
TL/H/9150–6

FIGURE 5. Multiple Contiguous Video Line Selector With Black Level Restoration

Physical Dimensions inches (millimeters)



Molded Small Outline Package (M)
Order Number LM1881M
NS Package Number M08A



Molded Dual-In-Line Package (N)
Order Number LM1881N
NS Package Number N08E

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National Semiconductor

June 1990

54ACT/74ACT715•LM1882
Programmable Video Sync Generator

General Description

The 'ACT715/LM1882 is a 20-pin TTL-input compatible device capable of generating Horizontal, Vertical and Composite Sync and Blank signals for televisions and monitors. All pulse widths are completely definable by the user. The device is capable of generating signals for both interlaced and noninterlaced modes of operation. Equalization and serration pulses can be introduced into the Composite Sync signal when needed.

Four additional signals can also be made available when Composite Sync or Blank are used. These signals can be used to generate horizontal or vertical gating pulses, cursor position or vertical Interrupt signal.

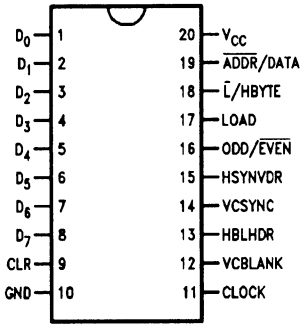
The 'ACT715/LM1882 makes no assumptions concerning *the system architecture. Line rate and field/frame rate are all a function of the values programmed into the data registers*, the status register, and the input clock frequency.

Features

- Maximum Input Clock Frequency > 100 MHz
- Interlaced and non-interlaced formats available
- Separate or composite horizontal and vertical Sync and Blank signals available
- Complete control of pulse width via register programming
- All inputs are TTL compatible
- 8 mA drive on all outputs
- Default RS170/NTSC values mask programmed into registers
- Orderable as linear device LM1882CN or LM1882CM

Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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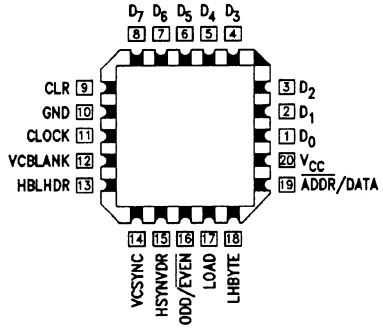
Pin Assignment for LCC



TL/F/10137–2

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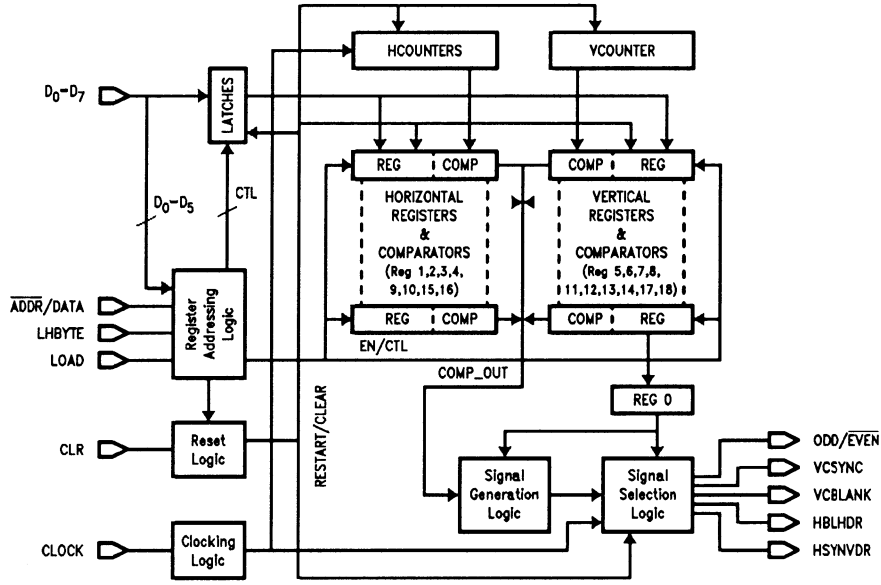
Logic Block Diagram



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Pin Description

There are a Total of 13 inputs and 5 outputs on the 'ACT715/LM1882.

Data Inputs D0–D7: The Data Input pins connect to the Address Register and the Data Input Register.

ADDR/DATA: The ADDR/DATA signal is latched into the device on the falling edge of the LOAD signal. The signal determines if an address (0) or data (1) is present on the data bus.

L/HBYTE: The L/HBYTE signal is latched into the device on the falling edge of the LOAD signal. The signal determines if data will be read into the 8 LSB's (0) or the 4 MSB's (1) of the Data Registers. A 1 on this pin when an ADDR/DATA is a 0 enables Auto-Load Mode.

LOAD: The Load control pin loads data into the Address or Data Registers on the rising edge. ADDR/DATA and L/HBYTE data is loaded into the device on the falling edge of the clock. The Load pin has been implemented as a Schmitt trigger input for better noise immunity.

CLOCK: System Clock input from which all timing is derived. The clock pin has been implemented as a Schmitt trigger for better noise immunity.

CLR: The Clear pin is an asynchronous input that initializes the device when it is high. Initialization consists of setting all registers to their mask programmed values, and initializing all counters, comparators and registers. The clear pin has been implemented as a Schmitt trigger for better noise immunity.

ODD/EVEN: Output that identifies if display is in odd (HIGH) or even (LOW) field of interlace when device is in interlaced mode of operation. In noninterlaced mode of operation this input is always HIGH. Data can be serially scanned out on this pin during test mode.

VCSYNC: Outputs Vertical or Composite Sync signal based on value of the Status Register.

VCBLANK: Outputs Vertical or Composite Blanking signal based on value of the Status Register.

HBLHDR: Outputs Horizontal Blanking signal, Horizontal Gating signal or cursor position based on value of the Status Register.

HSYNVDR: Outputs Horizontal Sync signal, Vertical Gating signal or Vertical Interrupt signal based on value of Status Register.

Register Description

All of the data registers are 12 bits wide. Width's of all pulses are defined by specifying the start count and end count of all pulses. Horizontal pulses are specified with-respect-to the number of clock pulses per line and vertical pulses are specified with-respect-to the number of lines per frame.

REG0—STATUS REGISTER

The Status Register controls the mode of operation, the signals that are output and the polarity of these outputs.

Bits 0–2

B_2	B_1	B_0	VCBLANK	VCSYNC	HBLHDR	HSYNVDR
0	0	0	CBLANK	CSYNC	HGATE	VGATE
0	0	1	VBLANK	CSYNC	HBLANK	VGATE
0	1	0	CBLANK	VSYNC	HGATE	HSYNC
0	1	1	VBLANK	VSYNC	HBLANK	HSYNC
1	0	0	CBLANK	CSYNC	CURSOR	VINT
1	0	1	VBLANK	CSYNC	HBLANK	VINT
1	1	0	CBLANK	VSYNC	CURSOR	HSYNC
1	1	1	VBLANK	VSYNC	HBLANK	HSYNC

Register Description (Continued)

Bits 3-4

B_4	B_3	Mode of Operation
0	0	Interlaced Double Serration and Equalization
0	1	Non Interlaced Double Serration
1	0	Illegal State
1	1	Non Interlaced Single Serration and Equalization

Bits 5-8

Bits 5 through 8 control the polarity of the outputs. A value of zero in these bit locations indicates a pulse active LOW. A value of 1 indicates an active HIGH pulse.

B5— VCBLANK Polarity

B6— VCSYNC Polarity

B7— HBLHDR Polarity

B8— HSYNVDR Polarity

Bits 9-11

Bits 9 through 11 enable several different features of the device.

B9— Enable Equalization/Serration Pulses (0)
Disable Equalization/Serration Pulses (1)

B10— Disable System Clock (0)
Enable System Clock (1)

B11— Disable Counter Test Mode (0)
Enable Counter Test Mode (1)

HORIZONTAL INTERVAL REGISTERS

The Horizontal Interval Registers determine the number of clock cycles per line and the characteristics of the Horizontal Sync and Blank pulses.

REG1— Horizontal Front Porch

REG2— Horizontal Sync Pulse End Time

REG3— Horizontal Blanking Width

REG4— Horizontal Interval Width # of Clocks per Line

VERTICAL INTERVAL REGISTERS

The Vertical Interval Registers determine the number of lines per frame, and the characteristics of the Vertical Blank and Sync Pulses.

REG5— Vertical Front Porch

REG6— Vertical Sync Pulse End Time

REG7— Vertical Blanking Width

REG8— Vertical Interval Width # of Lines per Frame

EQUALIZATION AND SERRATION PULSE SPECIFICATION REGISTERS

These registers determine the width of equalization and serration pulses and the vertical interval over which they occur.

REG 9— Equalization Pulse Width End Time

REG10— Serration Pulse Width End Time

REG11— Equalization/Serration Pulse Vertical Interval Start Time

REG12— Equalization/Serration Pulse Vertical Interval End Time

VERTICAL INTERRUPT SPECIFICATION REGISTERS

These Registers determine the width of the Vertical Interrupt signal if used.

REG13— Vertical Interrupt Activate Time

REG14— Vertical Interrupt Deactivate Time

CURSOR LOCATION REGISTERS

These 4 registers determine the cursor position location, or they generate separate Horizontal and Vertical Gating signals.

REG15— Horizontal Cursor Position Start Time

REG16— Horizontal Cursor Position End Time

REG17— Vertical Cursor Position Start Time

REG18— Vertical Cursor Position End Time

Signal Specification

HORIZONTAL SYNC AND BLANK SPECIFICATIONS

All horizontal signals are defined by a start and end time. The start and end times are specified in number of clock cycles per line. The start of the horizontal line is considered pulse 1 not 0. The horizontal counters start at 1 and count until HMAX. The value of HMAX must be divisible by 2. This limitation is imposed because during interlace operation this value is internally divided by 2 in order to generate serration and equalization pulses at 2 × the horizontal frequency. Horizontal signals will change on the falling edge of the CLOCK signal. Signal specifications are shown below.

Horizontal Period (HPER) = REG(4) × ckper

Horizontal Blanking Width = [REG(3) − 1] × ckper

Horizontal Sync Width = [REG(2) − REG(1)] × ckper

Horizontal Front Porch = [REG(1) − 1] × ckper

VERTICAL SYNC AND BLANK SPECIFICATION

All vertical signals are defined in terms of number of lines per frame. This is true in both interlaced and noninterlaced modes of operation. Care must be taken to not specify the Vertical Registers in terms of lines per field. The vertical counter starts at the value of 1 and counts until the value of VMAX. No restrictions exist on the values placed in the vertical registers. Vertical Blank will change on the leading edge of HBLANK. Vertical Sync will change on the leading edge of HSYNC.

Vertical Frame Period (VPER) = REG(8) × hper

Vertical Field Period (VPER/n) = REG(8) × hper/n

Vertical Blanking Width = [REG(7) − 1] × hper/n

Vertical Syncing Width = [REG(6) − REG(5)] × hper/n

Vertical Front Porch = [REG(5) − 1] × hper/n

where n = 1 for noninterlaced
n = 2 for interlaced

COMPOSITE SYNC AND BLANK SPECIFICATION

Composite Sync and Blank signals are created by logically ANDing (ORing) the active LOW (HIGH) signals of the corresponding vertical and horizontal components of these signals. The Composite Sync signal may also include serration and/or equalization pulses. The serration pulse interval occurs in place of the Vertical Sync interval. Equalization puls-

Signal Specification (Continued)

es occur preceding and/or following the serration pulses. The width and location of these pulses can be programmed through the registers shown below.

Horizontal Equalization PW = [REG(9) − REG(1)] × ckper

Horizontal Serration PW = [REG(4)/n + REG(1) − REG(10)] × ckper

Where n = 1 for noninterlaced single serration/equalization
n = 2 for noninterlaced double serration/equalization
n = 2 for interlaced operation

HORIZONTAL AND VERTICAL GATING SIGNALS

Horizontal and Vertical Gating Signals are available for use when Composite Sync and Blank signals are selected and the value of bit 2 of the status register is 0. The Vertical Gating signal will change in the same manner as that specified for the Vertical Blank.

Horizontal Gating Signal Width = [REG(16) − REG(15)] × ckper

Vertical Gating Signal Width = [REG(18) − REG(17)] × hper

CURSOR POSITION AND VERTICAL INTERRUPT

The Cursor Position and Vertical Interrupt signal are available when Composite Sync and Blank signals are selected and bit 2 of the Status Register is set to the value of 1. The cursor position generates a single pulse of n clocks wide during every line that the cursor is specified. The signals are generated by logically ORing (ANDing) the active LOW (HIGH) signals specified by the registers used for generating Horizontal and Vertical Gating signals. The Vertical Interrupt signal generates a pulse during the vertical interval specified. The Vertical Interrupt signal will change in the same manner as that specified for the Vertical Blanking signal.

Horizontal Cursor Width = [REG(16) − REG(15)] × ckper

Vertical Cursor Width = [REG(18) − REG(17)] × hper

Vertical Interrupt Width = [REG(14) − REG(13)] × hper

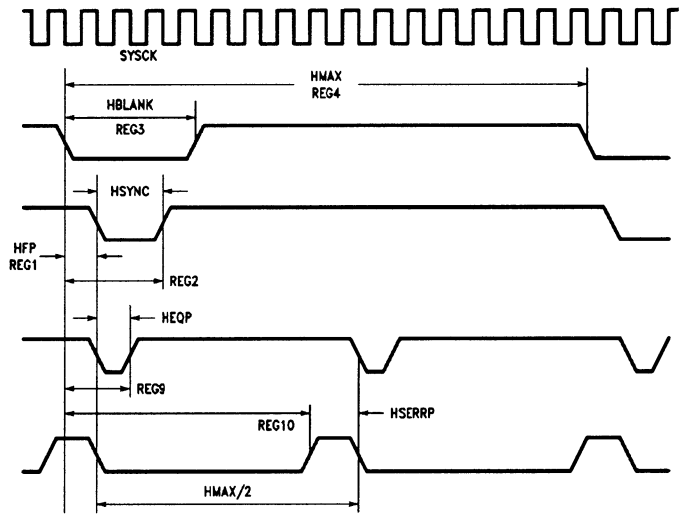


FIGURE 1. Horizontal Waveform Specification

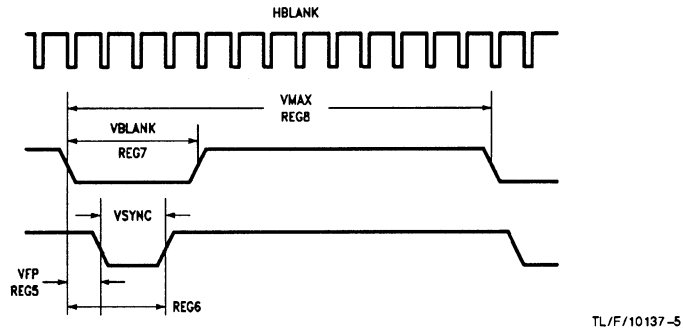


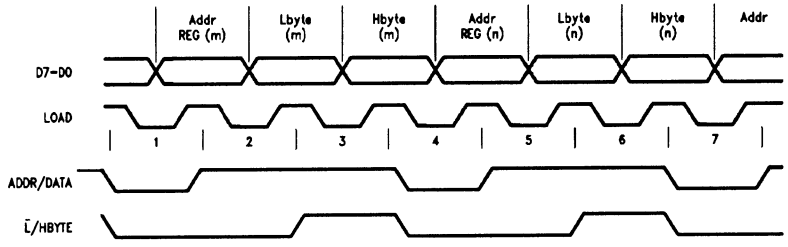
FIGURE 2. Vertical Waveform Specification

Addressing Logic

The register addressing logic is composed of two blocks of logic. The first is the address register and counter (ADDRCNTR), and the second is the address decode (ADDRDEC).

ADDRCNTR LOGIC

Addresses for the data registers can be generated by one of two methods. Manual addressing requires that each byte of each register that needs to be loaded needs to be addressed. To load both bytes of all 19 registers would require a total of 57 Load cycles (19 Address and 38 Data cycles). Auto Addressing requires that only the initial register value be specified. The Auto Load sequence would require only 39 Load cycles to completely program all registers (1 Address and 38 Data). In the auto load sequence the low order byte of the data register will be written first followed by the high order byte on the next load cycle. At the time the High Byte is written the address counter is incremented by 1. The counter has been implemented to loop on the initial value loaded into the address register. For example: If a value of 0 was written into the address register then the counter would count from 0 to 18 before resetting back to 0. If a value of 15 was written into the address register then the counter would count from 15 to 18 before looping back to 15. If a value greater than or equal to 18 is placed into the address register the counter will continuously loop on this value. Auto addressing is initiated on the falling edge of load when ADDRDATA is 0 and LHBYTE is 1. Incrementing and loading of data registers will not commence until the falling edge of LOAD after ADDRDATA goes to 1. The next rising edge of LOAD will load the first byte of data. Auto Incrementing is disabled on the falling edge of load after ADDRDATA and LHBYTE goes low.



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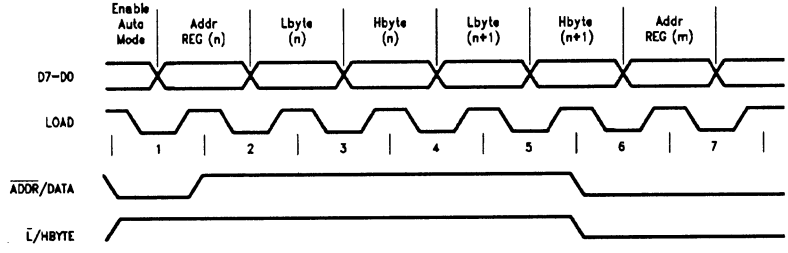
Manual Addressing Mode

Cycle #	Load Falling Edge	Load Rising Edge
1	Enable Manual Addressing	Load Address m
2	Enable Lbyte Data Load	Load Lbyte m
3	Enable Hbyte Data Load	Load Hbyte m
4	Enable Manual Addressing	Load Address n
5	Enable Lbyte Data Load	Load Lbyte n
6	Enable Hbyte Data Load	Load Hbyte n



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Auto Addressing Mode

Cycle #	Load Falling Edge	Load Rising Edge
1	Enable Auto Addressing	Load Start Address n
2	Enable Lbyte Data Load	Load Lbyte (n)
3	Enable Hbyte Data Load	Load Hbyte (n); Inc Counter
4	Enable Lbyte Data Load	Load Lbyte (n + 1)
5	Enable Hbyte Data Load	Load Hbyte (n + 1); Inc Counter
6	Enable Manual Addressing	Load Address

Addressing Logic (Continued)

ADDRDEC LOGIC

The ADDRDEC logic decodes the current address and generates the enable signal for the appropriate register. The enable values for the registers and counters change on the falling edge of LOAD. Since the data registers are disabled at this time any overlap of enable signals will not cause register data to change. The following Addresses are used by the device.

Address 0 Status Register REG0
Address 1-18 Data Registers REG1-REG18
Address 19-21 Unused
Address 22/54 Restart Vector (Restarts Device)
Address 23/55 Clear Vector (Zeros All Registers)
Address 24-31 Unused
Address 32-50 Register Scan Addresses
Address 51-53 Counter Scan Addresses
Address 56-63 Unused

At any given time only one register at most is selected. It is possible to have no registers selected.

VECTORED CLEAR ADDRESS

Addresses 23 (17H) or 55 (37H) is used to clear all registers simultaneously. This function may be desirable to use prior to loading new data into the Data or Status Registers. This address is read into the device in a similar fashion as all of the other registers.

VECTORED RESTART ADDRESS

The function of addresses 22 (16H) or 54 (36H) are similar to that of the CLR pin except that the programming of the registers is not affected. It is recommended but not required that this address is read after the initial device configuration load sequence.

SCAN MODE LOGIC

A scan mode is available in the ACT715/LM1882 that allows the user to non-destructively verify the contents of the registers. Scan mode is invoked through reading a scan address into the address register. The scan address of a given register is defined by the Data register address + 32. The internal Clocking signal is disabled when a scan address is read. Disabling the clock freezes the device in it's present state. Data can then be serially scanned out of the data registers through the ODD/EVEN Pin. The value of the two horizontal counters and 1 vertical counter can also be scanned out by using address numbers 51-53.

Normal device operation can be resumed by latching in a non-scan address. As the scanning of the registers is a non-destructive scan, the device will resume correct operation from the point at which it was halted.

RS170 Default Register Values

The tables below show the values programmed for the RS170 Format and how they compare against the actual EIA RS170 Specifications. The default signals that will be displayed are CSYNC, CBLANK, HDRIVE and VDRIVE. The device initially starts at the beginning of the odd field of interlace. All signals have active low pulses and the clock is disabled at power up. Registers 13 and 14 are not involved in the actual signal information. If the Vertical Interrupt was selected a pulse indicating the active lines would be displayed.

Reg	D Value	H	Register Description
REG0	0	000	Status Register
REG1	23	017	HFP End Time
REG2	91	05B	HSYNC Pulse End Time
REG3	157	09D	HBLANK Pulse End Time
REG4	910	38E	Total Horizontal Clocks
REG5	7	007	VFP End Time
REG6	13	00D	VSYNC Pulse End Time
REG7	41	029	VBLANK Pulse End Time
REG8	525	20D	Total Vertical Lines
REG9	57	038	Equalization Pulse End Time
REG10	410	19A	Serration Pulse Start Time
REG11	1	001	Pulse Interval Start Time
REG12	19	013	Pulse Interval End Time
REG13	41	029	Vertical Interrupt Activate Time
REG14	526	20E	Vertical Interrupt Deactivate Time
REG15	911	38F	Horizontal Drive Start Time (1)
REG16	92	05C	Horizontal Drive End Time
REG17	1	001	Vertical Drive Start Time
REG18	21	015	Vertical Drive End Time

	Rate	Period
Input Clock	14.31818 MHz	69.841 ns
Line Rate	15.73426 kHz	63.556 µs
Field Rate	59.94 Hz	16.683 ms
Frame Rate	29.97 Hz	33.367 ms

Signal	Width	µs	%H	Specification (µs)
HFP	22 Clocks	1.536		1.5 ±0.1
HSYNC Width	68 Clocks	4.749	7.47	4.7 ±0.1
HBLANK Width	156 Clocks	10.895	17.15	10.9 ±0.2
HDRIVE Width	91 Clocks	6.356	10.00	0.1H ±0.005H
HEQP Width	34 Clocks	2.375	3.74	2.3 ±0.1
HSERR Width	68 Clocks	4.749	7.47	4.7 ±0.1
HPER IOD	910 Clocks	63.556	100	

RS170 Default Register Values (Continued)

Signal	Width	μs	%V	Specification
VFP	3 Lines	190.67		6 EQP Pulses
VSYNC Width	3 Lines	190.67		6 Serration Pulses
VBLANK Width	20 Lines	1271.12	7.62	0.075V ± 0.005V
VDRIVE Width	11.0 Lines	699.12	4.20	0.04V ± 0.006V
VEQP Intrvl	9 Lines		3.63	9 Lines/Field
VPERIOD (field)	262.5 Lines	16.683 ms		16.683 ms/Field
VPERIOD (frame)	525 Lines	33.367 ms		33.367 ms/Frame

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) −0.5V to +7.0V

DC Input Diode Current (I_{IK})
- $V_I = -0.5V$ −20 mA
- $V_I = V_{CC} + 0.5V$ +20 mA

DC Input Voltage (V_I) −0.5V to V_{CC} + 0.5V

DC Output Diode Current (I_{OK})
- $V_O = -0.5V$ −20 mA
- $V_O = V_{CC} + 0.5V$ +20 mA

DC Output Voltage (V_O) −0.5V to V_{CC} + 0.5V

DC Output Source or Sink Current (I_O) ±15 mA

DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND}) ±20 mA

Storage Temperature (T_{STG}) −65°C to +150°C

Junction Temperature (T_J)
- CDIP 175°C
- PDIP 140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- 'ACT/LM1882 4.5V to 5.5V

Input Voltage (V_I) 0V to V_{CC}

Output Voltage (V_O) 0V to V_{CC}

Operating Temperature (T_A)
- 74ACT/LM1882 −40°C to +85°C
- 54ACT/LM1882 −55°C to +125°C

Minimum Input Edge Rate ($\Delta V/\Delta t$)
'AC Devices
V_{IN} from 30% to 70% of V_{CC}
V_{CC} @ 3.3V, 4.5V, 5.5V 125 mV/ns

Minimum Input Edge Rate ($\Delta V/\Delta t$)
'ACT/LM1882 Devices
V_{IN} from 0.8V to 2.0V
V_{CC} @ 4.5V, 5.5V 125 mV/ns

DC Characteristics For 'ACT Family Devices over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	V_{CC} (V)	74ACT/LM1882 $T_A = +25°C$, $C_L = 50$ pF	54ACT/LM1882 $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT/LM1882 $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits			
V_{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	V	$I_{OUT} = -50\ \mu A$
		5.5	5.49	5.4	5.4	V	
		4.5		3.86	3.76	V	*$V_{IN} = V_{IL}/V_{IH}$
		5.5		4.86	4.76	V	$I_{OH} = -8$ mA
V_{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	V	$I_{OUT} = 50\ \mu A$
		5.5	0.001	0.1	0.1	V	
		4.5		0.36	0.44	V	*$V_{IN} = V_{IL}/V_{IH}$
		5.5		0.36	0.44	V	$I_{OH} = +8$ mA
I_{OLD}	Minimum Dynamic Output Current	5.5			32.0	mA	$V_{OLD} = 1.65V$

*All outputs loaded; thresholds on input associated with input under test.

DC Characteristics

For 'ACT Family Devices over Operating Temperature Range (unless otherwise specified) (Continued)

Symbol	Parameter	V_{CC} (V)	74ACT/LM1882 $T_A = +25°C$, $C_L = 50$ pF		54ACT/LM1882 $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT/LM1882 $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OHD}	Minimum Dynamic Output Current	5.5				−32.0	mA	$V_{OHD} = 3.85V$
I_{IN}	Maximum Input Leakage Current	5.5		±0.1		±1.0	μA	$V_I = V_{CC}$, GND
I_{CC}	Supply Current Quiescent	5.5		8.0		80	μA	$V_{IN} = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6			1.5	mA	$V_{IN} = V_{CC} - 2.1V$

Note 1: Test Load 50 pF, 500Ω to Ground.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	74ACT/LM1882 $T_A = +25°C$, $C_L = 50$ pF			54ACT/LM1882 $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT/LM1882 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	Min	Max	
f_{MAXI}	Interlaced f_{MAX} (HMAX/2 is ODD)	5.0	170	190				150		MHz
f_{MAX}	Non-Interlaced f_{MAX} (HMAX/2 is EVEN)	5.0	190	220				175		MHz
t_{PLH1} t_{PHL1}	Clock to Any Output	5.0	4.0	13.0	15.5			3.5	18.5	ns
t_{PLH2} t_{PHL2}	Clock to ODDEVEN (Scan Mode)	5.0	4.5	15.0	17.0			3.5	20.5	ns
t_{PLH3}	Load to Outputs	5.0	4.0	11.5	16.0			3.0	19.5	ns

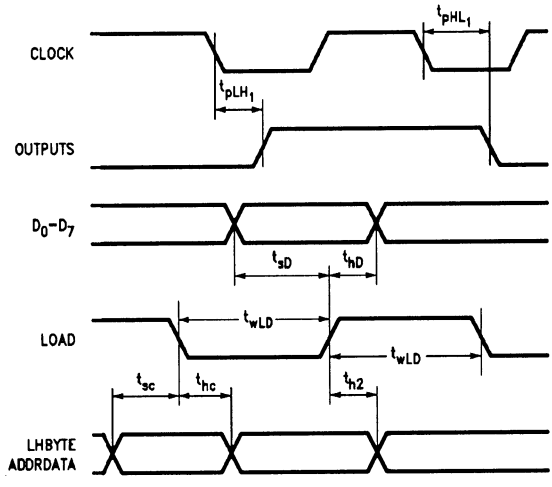
Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	7.0	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	17.0	pF	$V_{CC} = 5.0V$

AC Operating Requirements

Symbol	Parameter	V_{CC} (V)	74ACT/LM1882		54ACT/LM1882	74ACT/LM1882	Units
			T_A = +25°C		T_A = −55°C to +125°C	T_A = −40°C to +85°C	
			Typ	Guaranteed Minimums			
	Control Setup Time						
t_{sc}	ADDR/DATA to LOAD−	5.0	3.0	4.0		4.5	ns
t_{sc}	L/HBYTE to LOAD−		3.0	4.0		4.5	ns
	Data Setup Time						
t_{sd}	D7–D0 to LOAD+	5.0	2.0	4.0		4.5	ns
	Control Hold Time						
t_{hc}	LOAD− to ADDR/DATA	5.0	0	1.0		1.0	ns
	LOAD− to L/HBYTE		0	1.0		1.0	ns
	Data Hold Time						
t_{hd}	LOAD+ to D7–D0	5.0	1.0	2.0		2.0	ns
t_{rec}	LOAD+ to CL− (Note 1)	5.0	5.5	7.0		8.0	ns
	Pulse Width						
t_{wld-}	Load Low	5.0	3.0	5.5		5.5	ns
t_{wld+}	Load High	5.0	3.0	5.0		7.5	ns
t_{wclr}	CLR Pulse Width HIGH	5.0	5.5	6.5		9.5	ns
t_{wck}	CLOCK Width (High or Low)	5.0	2.5	3.0		3.5	ns

Note 1: Removal of Vectored Reset to Clock.

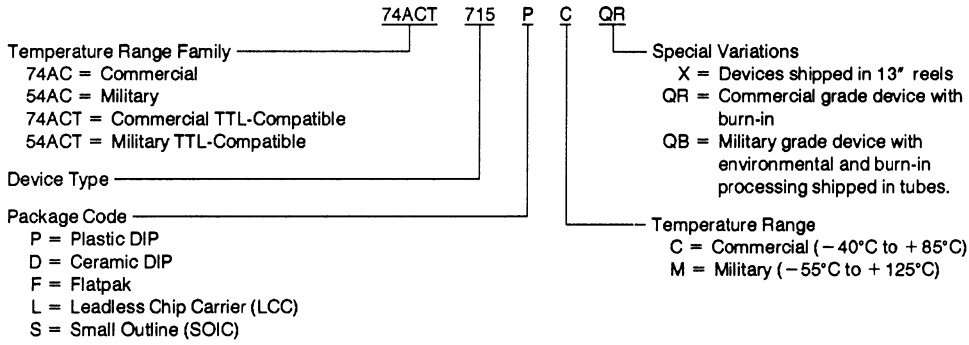


TL/F/10137–6

FIGURE 3. AC Specifications

Ordering Information

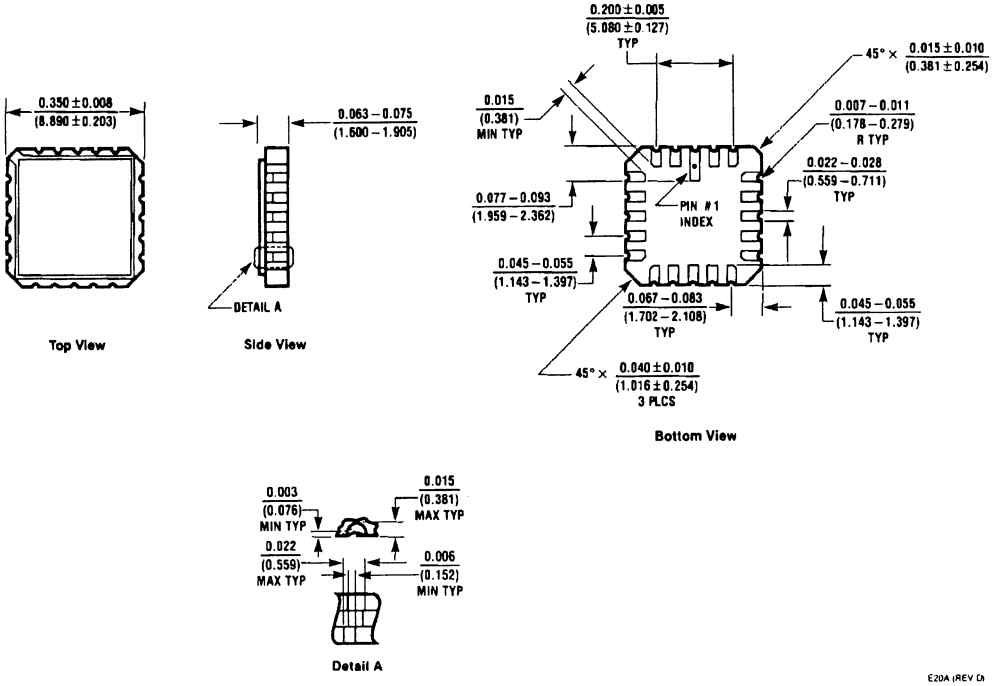
The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:



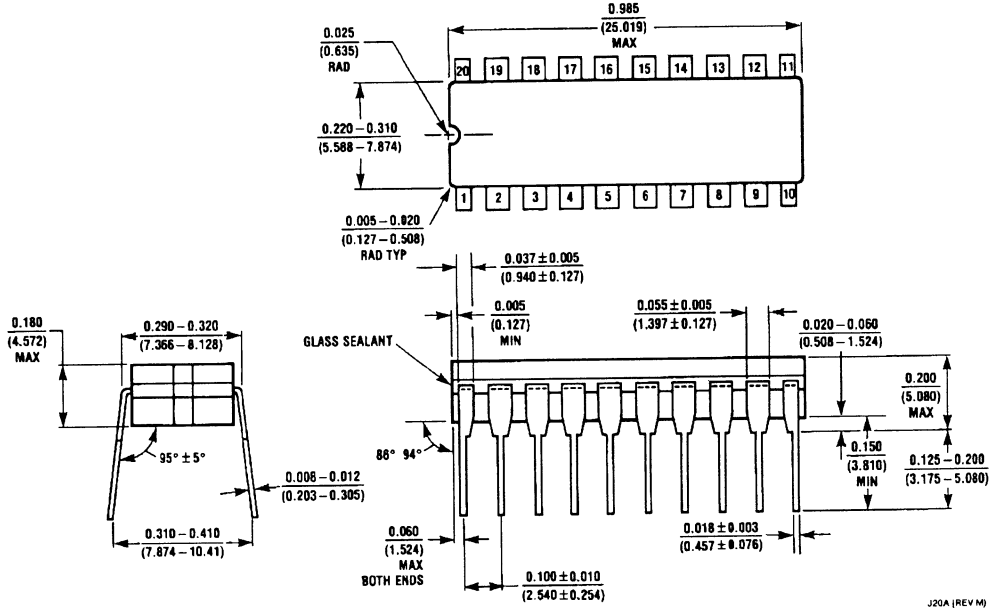
OR

LM1882CM — Commercial Small Outline (SOIC)
LM1882CN — Commercial Plastic DIP

Physical Dimensions inches (millimeters)

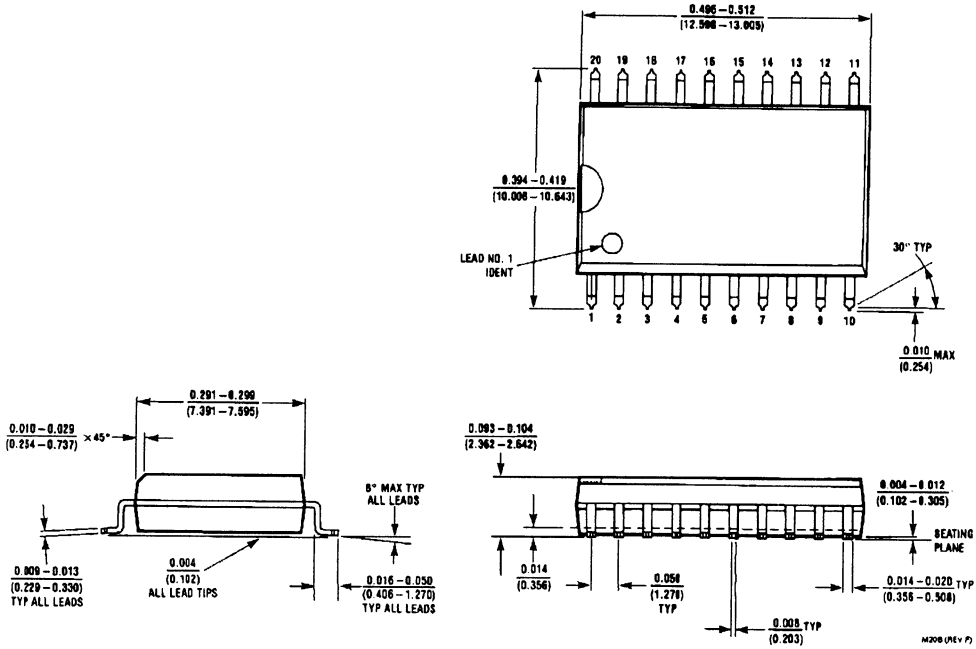


20-Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E20A

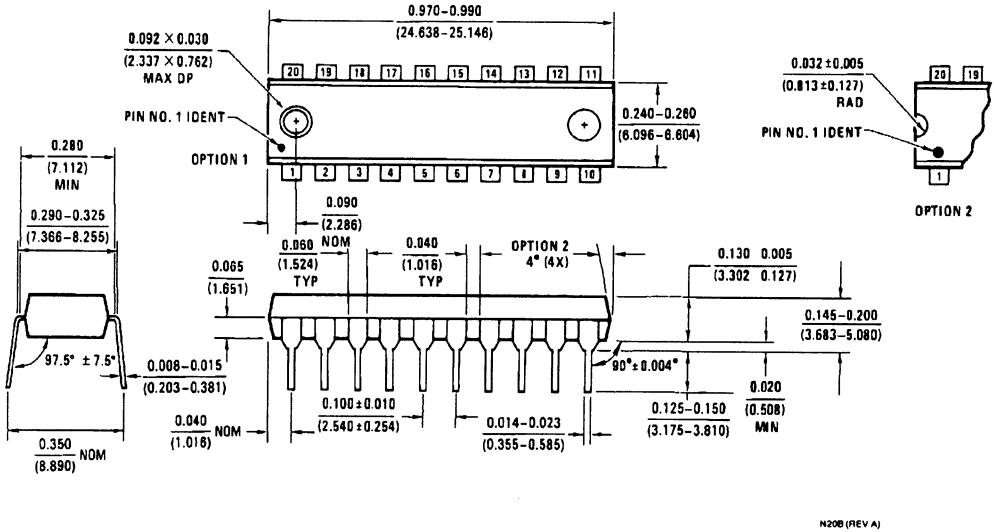


20-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J20A

Physical Dimensions inches (millimeters) (Continued)

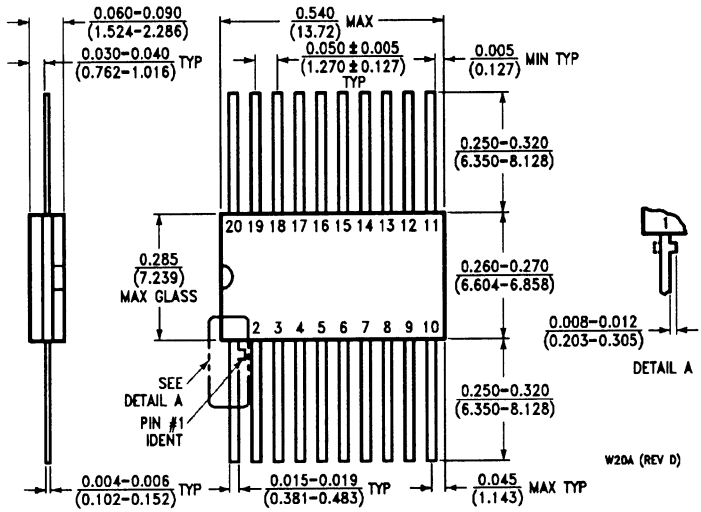


20-Lead Small Outline Integrated Circuit (S)
NS Package Number M20B



20-Lead Plastic Dual-In-Line Package (P)
NS Package Number N20B

Physical Dimensions inches (millimeters)



20-Lead Ceramic Flatpak (F)
NS Package Number W20A

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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National Semiconductor

September 1991

PRELIMINARY

LM2412 60MHz CRT Driver

General Description

The LM2412 CRT Video Driver is a wide bandwidth, large signal amplifier designed to swing large voltages with a short rise time. This amplifier is a fixed gain cascode circuit. The primary application for this very fast slewing amplifier is for driving High Resolution Monochrome or Color graphics monitors.

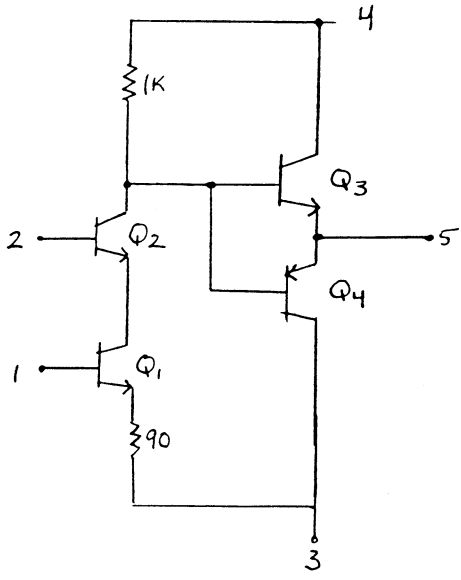
Features

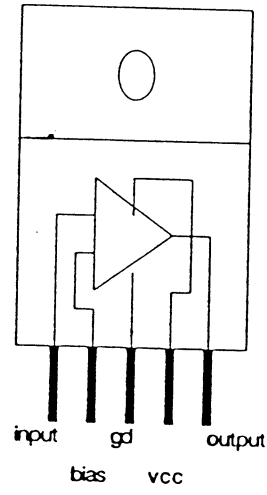
- Operation from 70V power supply
- 60 MHz bandwidth at 45 Vpp swings
- Rise/fall times less than 10ns
- Output signal can swing 45V
- Drives 8 pF capacitive load
- Low power consumption

Applications

- CRT driver for color and monochrome monitors
- High voltage amplifiers

Block and Connection Diagrams





Order Number LM2412T
See NS Package Number T05A

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications

Absolute Maximum Ratings)

Supply Voltage, V^+	75V
Power Dissipation, Pd	10W
Storage Temp Range, Tstg	-25 C to + 100 C
Operating Temp Range, Tcase	-20 C to + 90 C
Lead Temp (Soldering, <10sec)	300 C
ESD Tolerance	4kV

Electrical Characteristics The following specifications apply for V^+ = 70V, CL = 8 pF, DC input bias, Vin = 3.6 Vdc, 45 Vpp output swing, Vbias = +12V. Ta = 25 C unless otherwise noted.

Symbol	Parameter	Conditions		Typical	Units
I_{CC}	Supply Current	No Input or Output Load		33	mA
V_{OUT}	Output Offset Voltage	V_{IN} = 3.6V		35	V_{DC}
Tr	Rise Time	10% to 90%		7	ns
Tf	Fall Time	10% to 90%		5	ns
BW	Bandwidth	-3dB		60	MHz
Av	Voltage Gain			12	V/V
OS	Overshoot			0	%
LE	Linearity Error			10	%

National Semiconductor

November 1990

LM2416/LM2416C Triple 50 MHz CRT Driver

General Description

The LM2416 contains three wide bandwidth, large signal amplifiers designed for large voltage swings. The amplifiers have a gain of 13. The device is intended for use in color CRT monitors and is a low cost solution to designs conforming to VGA, Super VGA and the IBM® 8514 graphics standard.

The part is housed in the industry standard 11-lead TO-220 molded power package. The heat sink is floating and may be grounded for ease of manufacturing and RFI shielding.

Features

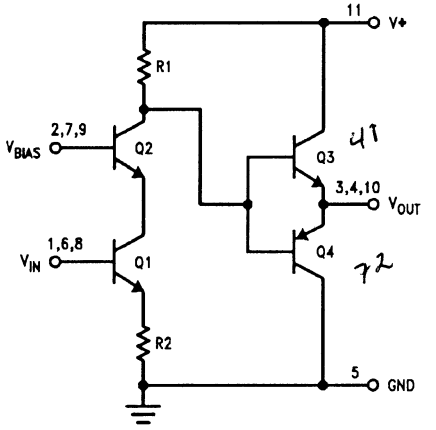
- 50 Vpp output at 45 MHz drives CRT directly
- Rise/fall time typically 10 ns with 8 pF load
- 65V output swing capability

Applications

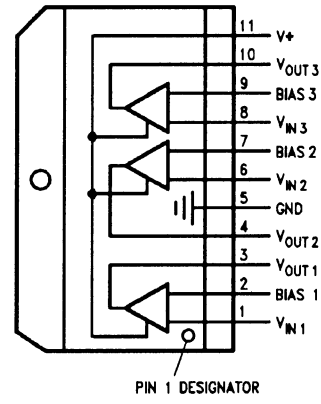
- CRT driver for RGB monitors
- High voltage amplifiers

Schematic and Connection Diagram

(One Section)



TL/K/10738–1



TL/K/10738–2

Top View

Order Number LM2416T or LM2416CT
See NS Package Number TA11B

IBM®8514 is a registered trademark of International Business Machines Corporation.

Absolute Maximum Ratings

Supply Voltage, V^+	+85V
Power Dissipation, P_D	10W
Storage Temperature Range, T_{STG}	−25°C to +100°C
Operating Temperature Range, T_{CASE}	−20°C to +90°C
Lead Temperature (Soldering, <10 sec.)	300°C
ESD Tolerance	4 kV

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Electrical Characteristics

V^+ = 80V, C_L = 8 pF, DC input bias, V_{IN} = 3.6 V_{DC}. 50 V_{PP} output swing, V_{BIAS} = +12V. See *Figure 1*. T_A = 25°C unless otherwise noted.

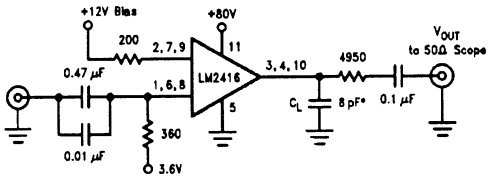
Symbol	Parameter	Conditions	LM2416			LM2416C			Units
			Min	Typical	Max	Min	Typ	Max	
I_{CC}	Supply Current (per Amplifier)	No Input or Output Load	18	22	26	16	22	28	mA
V_{OUT}	Output Offset Voltage	V_{IN} = 3.6V	38	42	46	35	42	48	V_{DC}
t_r	Rise Time	10% to 90% (Note 3)		8	13		12	16	ns
t_f	Fall Time	10% to 90% (Note 3)		10	13		12	16	ns
BW	Bandwidth	−3 dB		42			35		MHz
A_V	Voltage Gain		11	13	15	10	13	16	V/V
OS	Overshoot	*Figure 1*		0			0		%
LE	Linearity Error	(Note 1)		8			10		%
ΔA_V	Gain Matching	(Note 2)		0.2			0.5		dB

Note 1: Linearity Error is defined as the variation in small signal gain from +20V to +70V output with a 100 mV AC, 1 MHz, input signal.

Note 2: Calculated value from Voltage Gain test on each channel.

Note 3: Guaranteed parameter, not tested.

Test Circuit



TL/K/10738–3

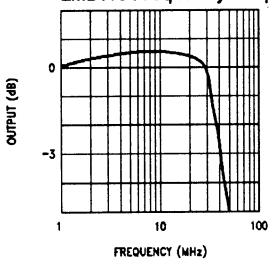
* 8 pF is total load capacitance. It includes all parasitic capacitance.

FIGURE 1. Test Circuit (One Section)

Figure 1 shows a typical test circuit for evaluation of the LM2416. This circuit is designed to allow testing of the LM2416 in a 50Ω environment such as a pulse generator, oscilloscope or network analyzer.

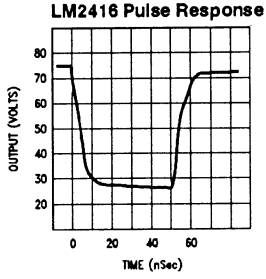
Typical Performance Characteristics

LM2416 Frequency Response



TL/K/10738–4

LM2416 Pulse Response

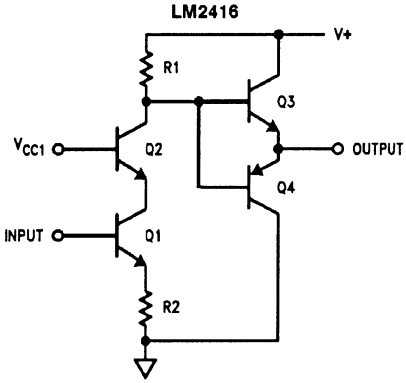


TL/K/10738–5

LM2416—Theory of Operation

The LM2416 is a high voltage triple CRT driver suitable for VGA, Super VGA, IBM 8514 and 1K by 768 non-interlaced display applications. The LM2416 features 80 volt operation and low power dissipation. The part is housed in the industry standard 11 lead TO-220 molded power package. The heat sink is floating and may be grounded for ease of manufacturing and RFI shielding.

The circuit diagram of the LM2416 is shown in *Figure 2*. Q1 and R1 provides a conversion of input voltage to current, while Q2 acts as a common base or cascode amplifier stage to drive the load resistor R1. Emitter followers Q3 and Q4 isolate the impedance of R1 from the capacitance of the CRT cathode, and make the circuit relatively insensitive to load capacitance. The gain of this circuit is R1/R2 and is fixed at 13. The bandwidth of the circuit is set by the collector time constant formed by the load resistor R1 and associated capacitance of Q2, Q3, Q4, and stray layout capacitance. Proprietary transistor design allows for high bandwidth with low operating power.



TL/K/10738–6

FIGURE 2. LM2416 CRT Driver (One Section)

Thermal Considerations

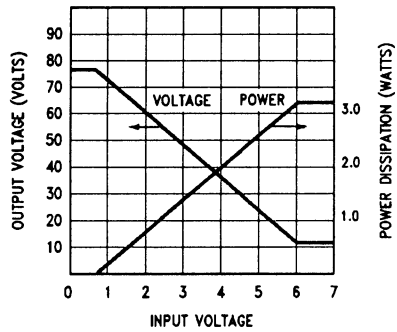
The transfer characteristics of the amplifier are shown in *Figure 3*. Since this is a class A input stage, power supply current increases as the input signal increases and consequently power dissipation also increases. Average dissipation per stage is 1.8W, increasing to 3.2W at minimum output voltage.

The LM2416 cannot be used without heat sinking. *Figure 3* shows the power dissipated in each channel over the operating voltage range of the device. Typical "average" power dissipation with the device output voltage at one half the supply voltage is 1.8W per channel for a total dissipation of 5.4W package dissipation. Under white screen conditions, i.e.: 15V output, dissipation increases to 3W per channel or 9W total. The LM2416 case temperature must be maintained below 90°C. If the maximum expected ambient temperature is 50°C, then a heat sink is needed with thermal resistance equal to or less than:

$$R_{th} = \frac{(90 - 50°C)}{9W} = 4.4°C/W$$

The Thermalloy #6400 is one example of a heatsink that meets this requirement.

WARNING: THE LM2416 IS NOT PROTECTED AGAINST OUTPUT SHORT CIRCUITS. The maximum DC load the LM2416 can drive is 600Ω to ground or V^+.



TL/K/10738–7

FIGURE 3. LM2416 DC Characteristics

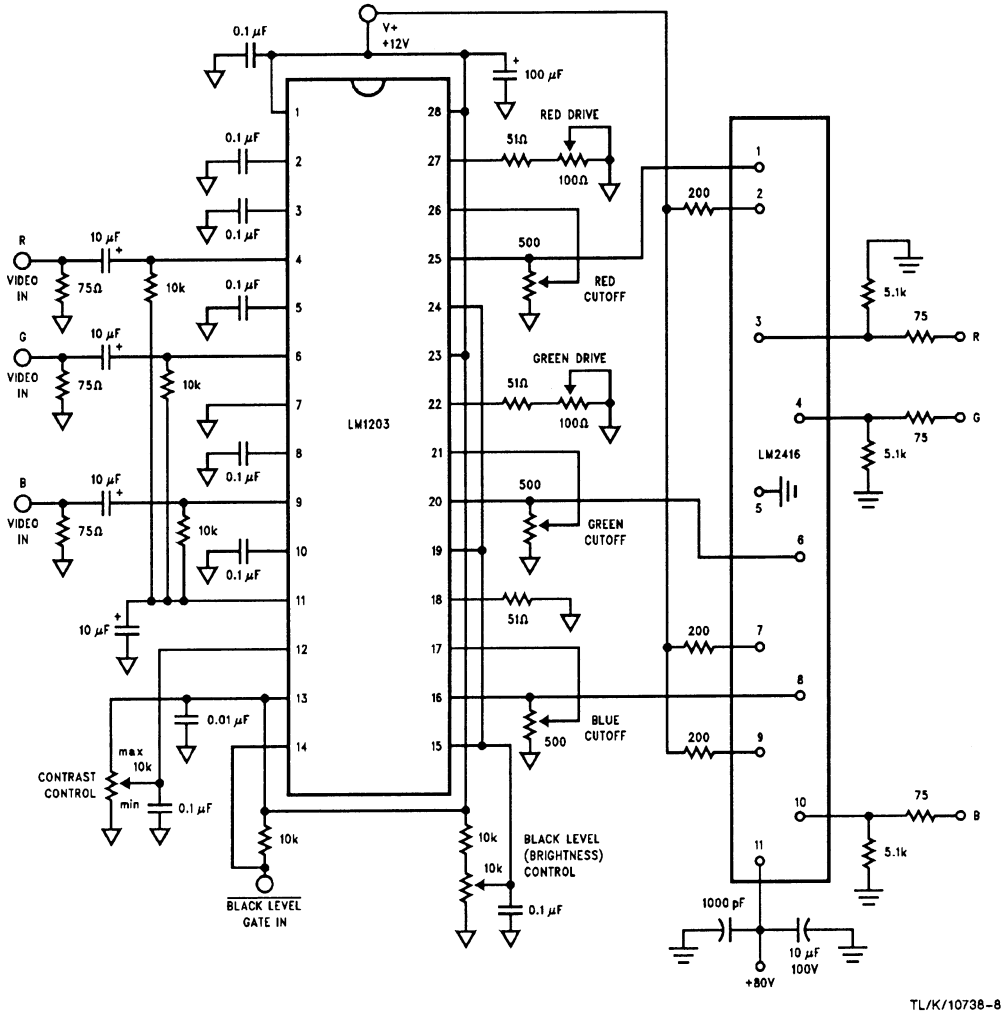
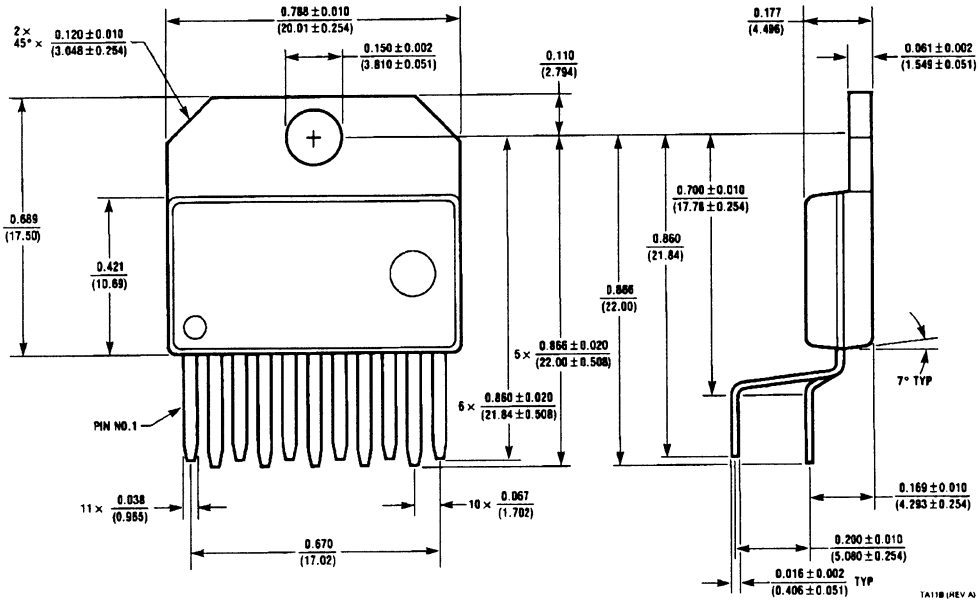


FIGURE 4. Typical Application LM1203-LM2416 Application

A typical application of the LM2416 is shown in *Figure 4*. Used in conjunction with a LM1203, a complete video channel from monitor input to CRT cathode is shown. Performance is satisfactory for all applications to 1k by 768 non-interlaced. Typical rise-fall times are 12 ns, with better than 50V p-p drive signals available to an 8 pF load. In this application, feedback is local to the LM1203. An alternative scheme would be feedback from the output of the LM2416 to the positive clamp inputs of the LM1203. This would provide slightly better black level control of the system.

Physical Dimensions inches (millimeters)



11 Lead TO-220 Molded Package (T)
Order Number LM2416T or LM2416CT
NS Package Number TA11B

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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National Semiconductor

January 1992

LM2418 Triple 30 MHz CRT Driver

General Description

The LM2418 contains three large signal voltage amplifiers designed to directly drive CRT cathodes for VGA Color Graphics Displays. Output swings greater than 50 V_{PP} are achieved with a 90V power supply. The nominal voltage gain of each amplifier is 18 with gain matching of 1.0 dB between amplifiers.

Packaging is the industry standard molded 11 lead TO-220. The heatsink tab is isolated and may be grounded to improve RFI shielding and simplify assembly.

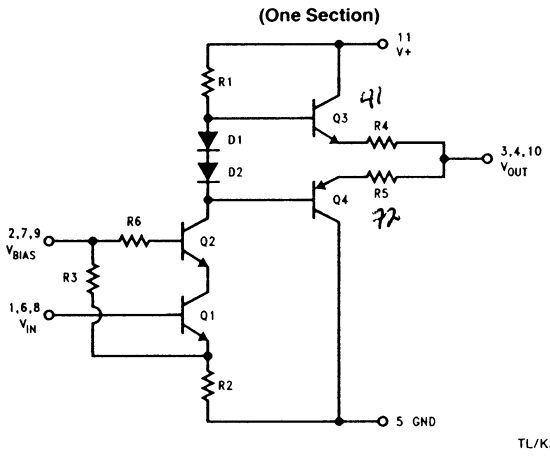
Features

- 50 Vpp output at 30 MHz drives CRT directly
- Rise/fall time typically 12 ns with 8 pF load
- 65V output swing capability
- Optimized output stage for low crossover distortion
- Gain matching of 1 dB
- Voltage gain of 18
- Includes oscillation supression resistors

Applications

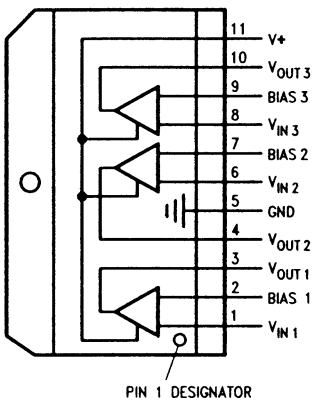
- CRT driver for RGB monitors
- High voltage amplifiers

Schematic and Connection Diagram



TL/K/11125-1

FIGURE 1



TL/K/11125-2

Top View

Order Number LM2418T
See NS Package Number TA11B

 TL/K/11125

RRD-B20M32/Printed in U. S. A.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V^+ +95V

Storage Temperature Range, T_{STG} −25°C to +100°C

Operating Temperature Range, T_{CASE} −20°C to +100°C

Lead Temperature (Soldering, <10 sec.) 300°C

ESD Tolerance tbd

Electrical Characteristics

V^+ = 90V, C_L = 8 pF, DC input bias, V_{IN} = 3.6 V_{DC}. 50 V_{PP} output swing, V_{BIAS} = +12V. T_A = 25°C unless otherwise noted.

Symbol	Parameter	Conditions	LM2418			Units
			Min	Typ	Max	
I_{CC}	Supply Current (per Amplifier)	No Input or Output Load		18	26	mA
V_{OUT}	Output Offset Voltage	V_{IN} = 3.6V	46	53	60	V_{DC}
t_r	Rise Time	10% to 90% (Note 3)		12	20	ns
t_f	Fall Time	10% to 90% (Note 3)		12	20	ns
BW	Bandwidth	−3 dB		30		MHz
A_V	Voltage Gain		15	18	21	V/V
OS	Overshoot			5		%
LE	Linearity Error	(Note 1)		8		%
ΔA_V	Gain Matching	(Note 2)		1.0		dB

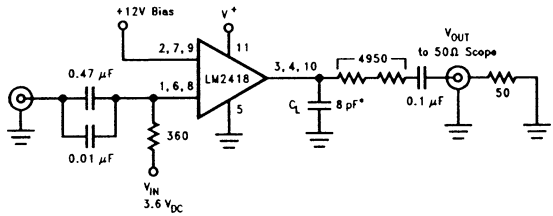
Note 1: Linearity Error is defined as the variation in small signal gain from +20V to +70V output with a 100 mV AC, 1 MHz, input signal.

Note 2: Calculated value from Voltage Gain test on each channel.

Note 3: Guaranteed parameter, not tested.

AC Test Circuit

Figure 2 shows a typical test circuit for evaluation of the LM2418. This circuit is designed to allow testing of the LM2418 in a 50Ω environment such as a pulse generator, oscilloscope or network analyzer.



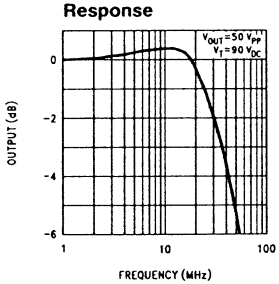
TL/K/11125-3

*8 pF is total load capacitance. It includes all parasitic capacitance.

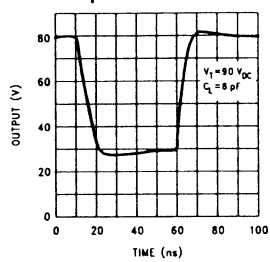
FIGURE 2. Test Circuit (One Section)

Typical Performance Characteristics

LM2418 Frequency Response



LM2418 Pulse Response



TL/K/11125-4

TL/K/11125-5

FIGURE 3

LM2418—Theory of Operation

The LM2418 is a high voltage triple CRT driver suitable for VGA display applications. The LM2418 features 90V operation and low power dissipation. The part is housed in the industry standard 11-lead TO-220 molded power package. The heat sink is electrically isolated from the circuitry and may be grounded for ease of manufacturing and RFI shielding.

The circuit diagram of the LM2418 is shown in *Figure 1*. Q1 and R1 provide a conversion of input voltage to current, while Q2 acts as a common base or cascode amplifier stage to drive the load resistor R1. Emitter followers Q3 and Q4 isolate the impedance of R1 from the capacitance of the CRT cathode, and make the circuit relatively insensitive to load capacitance. The gain of this circuit is R1/R2 and is fixed at 18. The bandwidth of the circuit is set by the collector time constant formed by the load resistor R1 and associated capacitance of Q2, Q3, Q4, and stray layout capacitance. Diodes D1 and D2 provide forward bias to the output stage to reduce crossover distortion at low signal levels, while R3 provides a DC bias offset to match the output level characteristics of the LM1203 RGB Video Amplifier System. Proprietary transistor design allows for high bandwidth with low operating power.

Figure 2 shows a typical test circuit for evaluation of the LM2418. This circuit is designed to allow testing of the LM2418 in a 50Ω environment such as a pulse generator and a scope, or a network analyzer. In this test circuit, two resistors in series totaling 4.95 kΩ form a wideband low capacitance probe to match the output of the LM2418 to a 50Ω cable and load. Typical AC performance of the circuit is shown in *Figure 3*. The input signal is AC coupled to the base of Q1, while a DC bias of 12V is applied to the base of Q2.

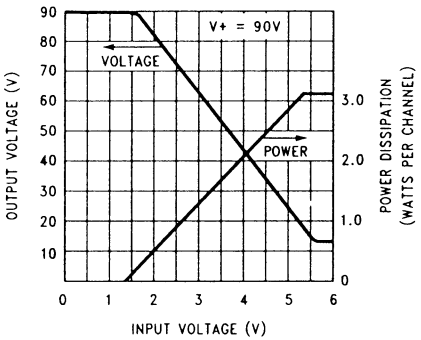
Thermal Considerations

The transfer characteristics of the amplifier are shown in *Figures 4* and *5*. Since this is a class A input stage, power supply current increases as the input signal increases and consequently power dissipation also increases. Average dissipation per stage is 1.1W, increasing to 1.85W per stage at minimum output voltage.

The LM2418 cannot be used without heat sinking. *Figure 5* shows the power dissipated in each channel over the operating voltage range of the device. Typical "average" power dissipation with the device output voltage at one half the supply voltage is 1.8W per channel for a total dissipation of 5.4W package dissipation. Under white screen conditions, i.e., 20V output, dissipation increases to 3.0W per channel or 9W total. The LM2418 case temperature must be maintained below 100°C. If the maximum expected ambient temperature is 60°C, then a maximum heat sink thermal resistance can be calculated:

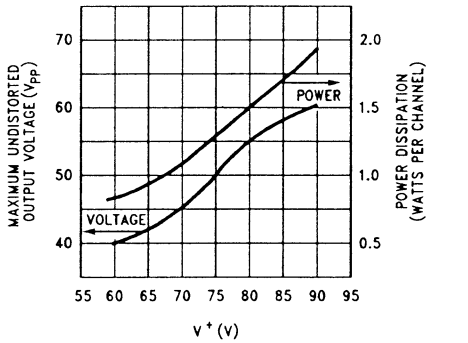
$$R_{th} = \frac{(100°C - 60°C)}{9W} = 4.4°C/W$$

PRECAUTION: THE LM2418 IS NOT PROTECTED AGAINST OUTPUT SHORT CIRCUITS. The maximum DC load the LM2418 can drive is 800Ω to ground or V^+.



TL/K/11125-7

FIGURE 4. LM2418 DC Characteristics



TL/K/11125-9

FIGURE 5. LM2418 Output Swing and Power Characteristics

Typical Application

A typical application of the LM2418 is shown in *Figure 6.* Used in conjunction with an LM1203, a complete video channel from monitor input to CRT cathode is shown. Performance is satisfactory for all applications up to 640 by 480 lines. Typical rise/fall times of this circuit are 15 ns, with better than 50 V_{PP} drive signals available to a 10 pF load. In this application, feedback is local to the LM1203, an alternative scheme would feed back from the output of the LM2418 to the positive clamp inputs of the LM1203. This would provide better black level control of the system.

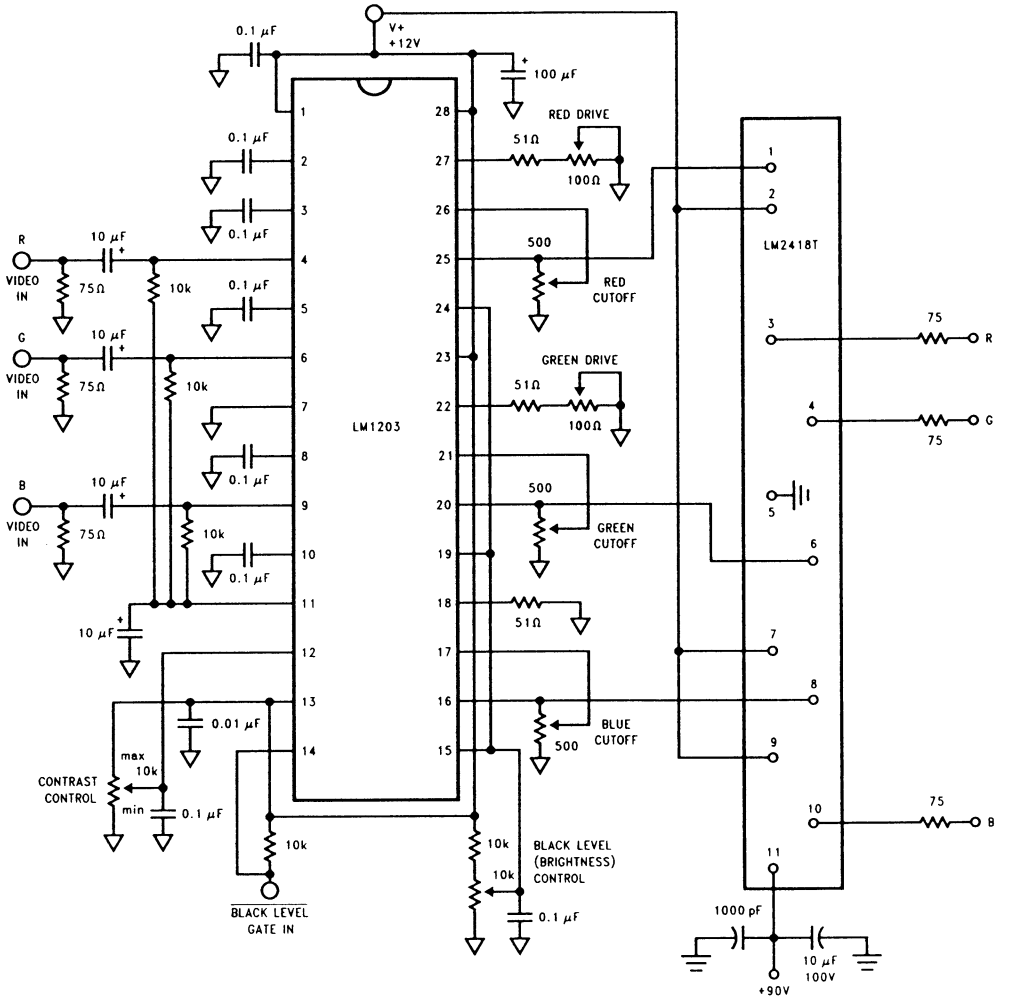
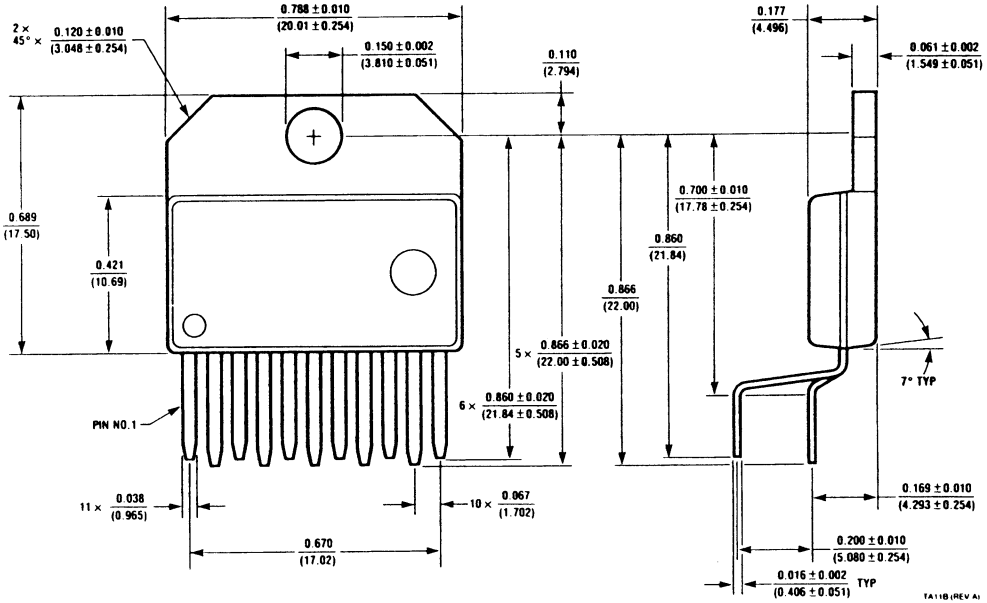


FIGURE 6. Typical Application LM1203-LM2418 Application

Physical Dimensions inches (millimeters)



11 Lead TO-220 Molded Package (T)
Order Number LM2418T
NS Package Number TA11B

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Preliminary

Warning : All Information contained herein is subject to change without notice

LM2419 Triple 65 MHz CRT Driver

General Description

The LM2419 contains three wide bandwidth, large signal amplifiers designed for large voltage swings. The amplifiers have a gain of 15. The device is intended for use in color CRT monitors and is a low cost solution to designs conforming to 1024 x 768 display resolution.

The device is mounted in the industry standard 11 - lead TO - 220 molded power package. The heat sink is electrically isolated and may be grounded for ease of manufacturing and EMI / RFI shielding.

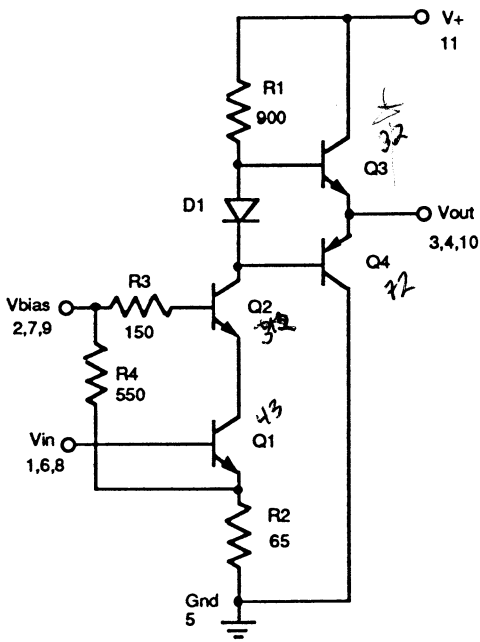
Features

- 50 Vpp output swing at 65 MHz
- Rise / Fall time < 7ns with 12 pF load
- 60 Vpp output swing capability
- Pin and function compatible with LM2416

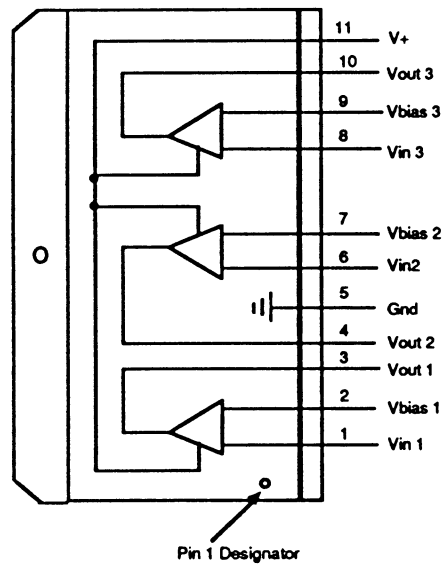
Applications

- CRT driver for SVGA, IBM 8514 and 1024 x 768 display resolution RGB monitors

Schematic and Connection Diagrams



One Channel



Order Number LM2419T
See NS Package Number TA11B

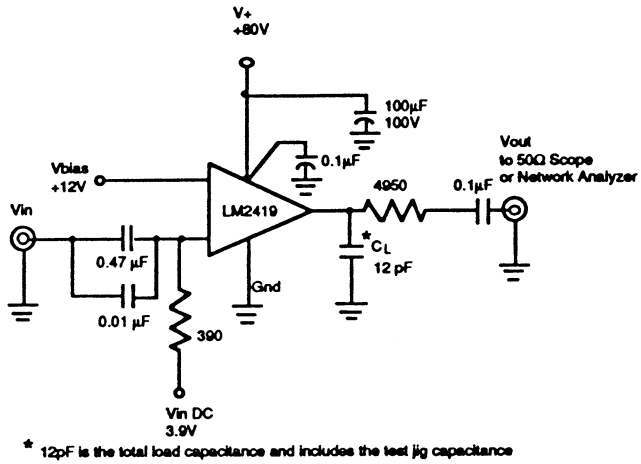


Fig 1. Test Circuit (One Section)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Absolute Maximum Ratings (Note 1)

Supply Voltage, V+	+85V Max
Storage Temperature, TSTG	-25 °C to 100 °C
Operating Case Temperature, T_{Case}	-20 °C to 90 °C
Lead Temperature (soldering < 10 sec)	300 °C
ESD Tolerance	TBD

Electrical Characteristics

Unless otherwise specified, the following specifications apply for V+ = 80V, DC input bias, $V_{in\ DC}$ = 3.9V; 50 Vpp output swing; frequency = 1 MHz; Vbias = 12V; CL = 12 pF; T_A = 25 °C; see test circuit, Fig.1 .

Symbol	Parameter	Conditions	Min (Note 3)	Typical (Note 2)	Max (Note 3)	Units (limit)
I_{cc}	Supply Current (per amplifier)	Input / Output open circuit		TBD		mA
V_{out}	Output Offset Voltage			50		V
t_r	Rise Time	10 % to 90 % (Note 4)		4		ns
t_f	Fall Time	10 % to 90 % (Note 4)		5		ns
BW	Bandwidth	f_{-3dB}		65		MHz
	Tilt	1 kHz				
A_V	Voltage Gain			15		V/V
OS	Over shoot	tr, tf = 5ns		4		%
OS	Overshoot	(Note 4)		TBD		%
LE	Linearity Error	Vout = 25V to 75V		TBD		%
...	Gain Matching			0.2		dB

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

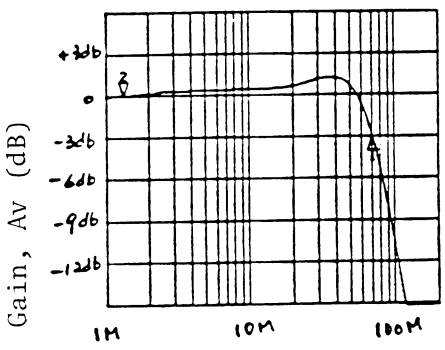
Note 2: Typical specifications are at 25 °C and represent the most likely parametric norm.

Note 3: Min / Max limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 4: Input signal t_r, t_f < 2ns.

Typical Performance Characteristics (T_A = 25 °C, Test Circuit - Fig.1)

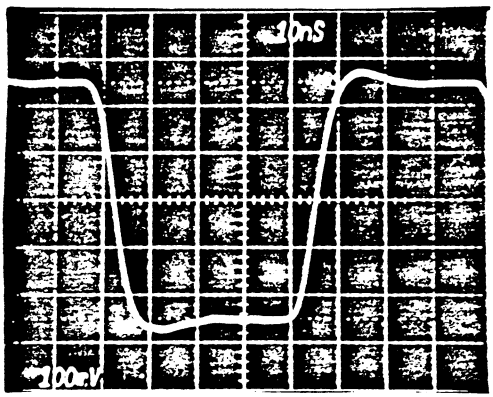
Frequency Response



Gain, Av (dB)

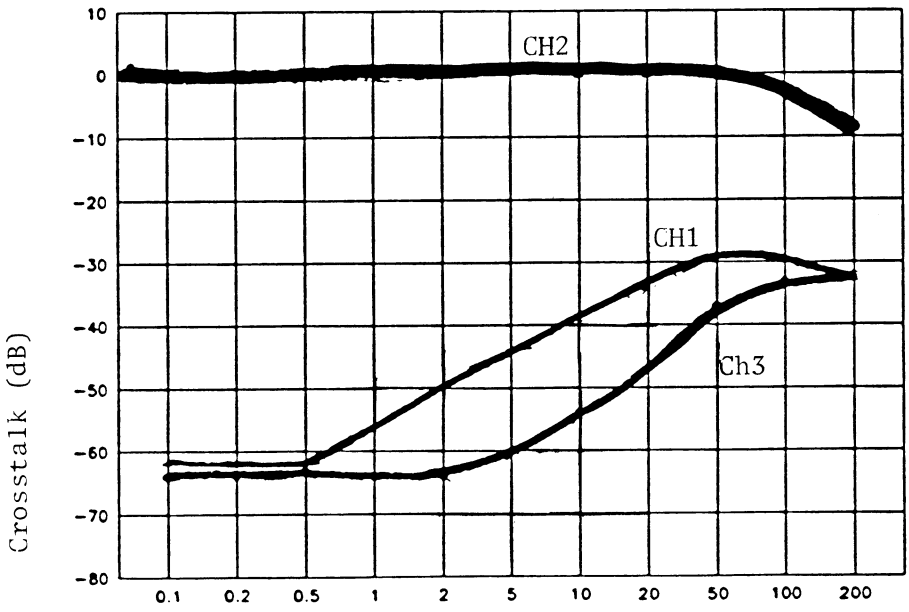
Frequency (Hz)

Pulse Response



Vert: 10V/div
Horiz: 10ns/div

Crosstalk vs Frequency



Crosstalk (dB)

Frequency (Hz)

Test Circuit

Figure.1 shows a typical test circuit for evaluation of the LM2419. The input signal is ac coupled into the input of LM2419 and is referenced to 3.9V DC using an external 3.9V DC bias through a 390 Ω resistor. The test circuit is designed to allow testing of the LM2419 in a 50 Ω environment such as a 50 Ω oscilloscope or network analyzer. The 4950 Ω resistor in series with the output of the LM2419 forms a 100 : 1 voltage divider when interfaced to a 50 Ω oscilloscope or network analyzer.

Theory of Operation

The LM2419 is a high voltage triple CRT driver suitable for SVGA, IBM 8514 and 1024 x 768 display resolution monitors. The device is packaged in the industry standard 11 - lead TO - 220 molded power package. The heat sink is electrically isolated and may be grounded for ease of manufacturing and RFI / EMI shielding.

The schematic diagram of LM2419 is shown in Figure.2. Q1 and R2 provide a conversion of the input voltage to current while Q2 acts as a common base amplifier to drive the load resistor, R1. Resistor R4 along with R2 sets up the dc bias at the base of Q1. Emitter followers Q3 and Q4 isolate R1 from the capacitive load at the output, thus making the rise and fall times relatively insensitive to the load capacitance.

The gain of the amplifier is - R1 / (R2 || R4) and is fixed at approximately -15. The bandwidth of LM2419 is primarily limited by the time constant due to R1 and the capacitances associated with D1, Q2, Q3 and Q4. Diode D1 is used to provide some bias voltage for Q3 and Q4 so as to reduce small signal cross over distortion. Resistor R3 is used to prevent Q2 from oscillating at high frequencies.

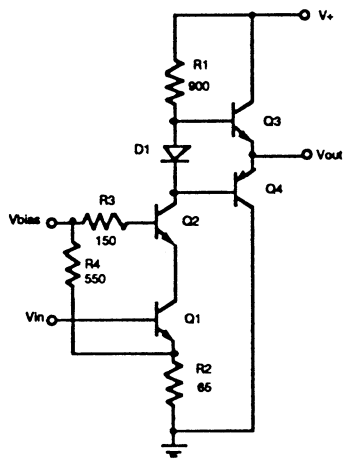


Figure. 2 . Schematic diagram of one section of LM2419.

Application Hints

Arc protection

The LM2419 must be protected from arcing within the CRT. To limit the arcover voltage, a 200V spark gap is recommended at the cathode. Clamp diodes D1 and D2 (as shown in Figure.3) are used to clamp the voltage at the output of LM2419 to a safe level. The clamp diodes used should have high current rating, low series impedance and low shunt capacitance. Resistor R2 in Figure.3 limits the arcover current while R1 limits the current into LM2419 and reduces the power dissipation of the output transistors when the output is stressed beyond the supply voltage. Having large value resistors for R1 and R2 would be desirable but this has the effect of reducing rise and fall times.

Improving rise and fall times

Because of an emitter follower output stage, the rise and fall times of the LM2419 are relatively unaffected by capacitive loading. However, the series resistors R1 and R2 (see Figure.3) will reduce the rise and fall times when driving the CRT's cathode which appears as a capacitive load. The capacitance at the cathode typically ranges from 8pF to 12pF.

To improve the rise and fall times at the cathode, a small inductor is often used in series with the output of the amplifier. The inductor L1 in Figure.3 peaks the amplifier's frequency response at the cathode thus improving rise and fall times. The inductor value is emperically determined and is dependant on the load. An inductor value of 0.1μH is a good starting value. Note that peaking

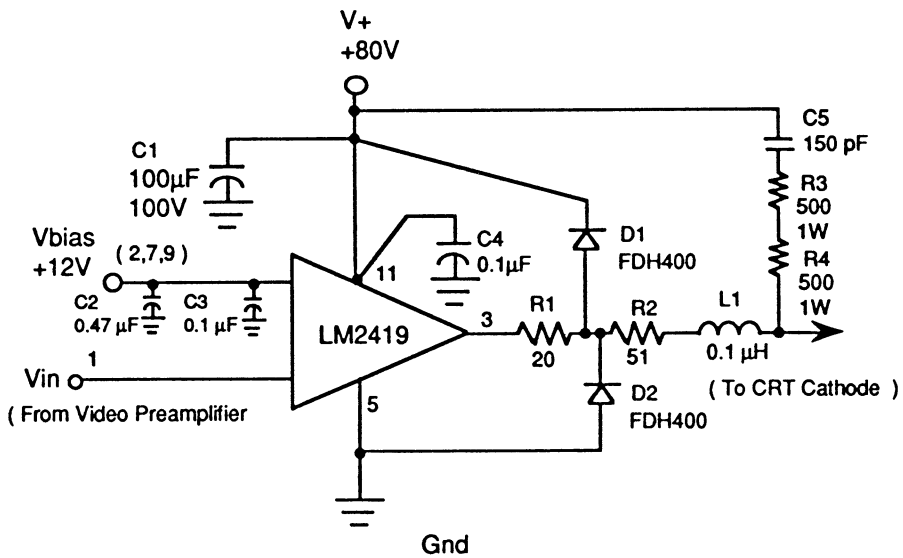


Figure.3 Typical application circuit (one channel).

the amplifier's frequency response will increase the overshoot.

Reducing overshoot

LM2419's overshoot is a function of both the input signal rise and fall times and the capacitive loading. The overshoot is increased by either more capacitive loading or faster rise and fall times of the input signal.

Table.1 shows the overshoot for a typical device with different capacitive loads and different input signal rise and fall times. As can be observed from Table.1, overshoot is large for large capacitive loads and faster input signal rise and fall times. In an actual application, the LM2419 is driven from a preamplifier with rise and fall times of 3ns to 7ns. When driven from LM1203 preamplifier (see application circuit, Figure.6) the overshoot is 4 % with 12 pF capacitive load. The overshoot can be reduced by including a resistor in series with LM2419's output as in Figure.3. Larger value resistors for R1 and R2 would reduce overshoot but this also increases the rise and fall times at the output.

Resistors R3 and R4 and capacitor C5 in Figure.3 also reduce the overshoot considerably without adversely affecting the rise and fall times. Capacitor C5's value should not be increased too much otherwise power dissipated by R3 and R4 would increase significantly at high frequencies. The value of R3 and R4 is emperically determined, 500 Ω is a good starting value. Two resistors are used because lower wattage resistors can be used and also the effective shunt capacitance of two resistors is less than that of a single resistor.

Overshoot (%)

t_r / t_f	C_L			
	5pF	8pF	11pF	15pF
1.2ns	4%	6%	7%	8%
7ns	4%	5%	6%	7%

Table.1 LM2419 overshoot versus capacitive loading for a typical device.

Short Circuit Protection

The output of LM2419 is not short circuit protected. Shorting the output to either ground or to V_+ will destroy the device. The maximum DC load the LM2419 can drive is 600 Ω ???? to ground or V_+.

RGB Video Application

A complete video section for an RGB CRT monitor is shown in Figiure. 6. The LM1203 video preamplifier and the LM2419 include almost all the circuitry required between the video input connection and the CRT's cathodes. However, an externally generated back porch clamp signal is required to accomplish DC restoration of the video signal.

Performance is satisfactory for a non - interlaced 1024 x 768 display resolution application. With 50 Vpp output swing and 12 pF load, the rise / fall time for Figure. 6's circuit was measured at 6.5 ns. In this application, feedback is local to the LM1203. An alternative scheme would be feedback from the output of the LM2419 to the positive clamp inputs of the LM1203. This would provide better black level stability in a DC coupled cathode drive application. For detailed information on the LM1203, please refer to the LM1203 data sheet.

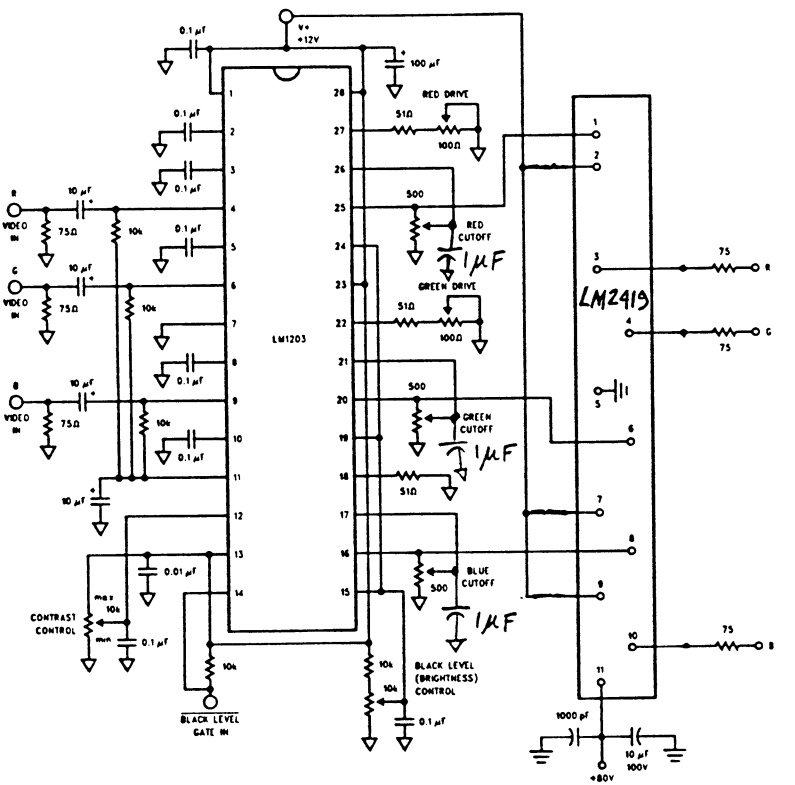


FIGURE 6. Typical Application LM1203-LM2419 Application

Gain versus output DC level

Figure. 4 shows LM2419's gain versus output DC level. A 100 mV_{pp} ac signal is applied at the LM2419's input and the input signal's DC level is swept. As can be seen from Figure. 4, the amplifier's gain is constant at approximately 13.6 (Vout = 1.36 Vpp) for output DC level between 30V and 70V.

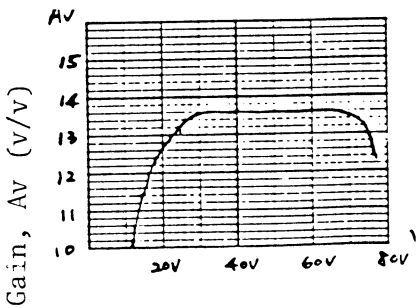
If the amplifier's output signal swings well beyond the 30V to 70V range then the amplifier's transfer function will start approaching the non - linear region. For optimum performance, it is recommended that LM2419's output low voltage be at 25V or above. With 50 V_{pp} swing, the output high voltage is 75V.

Thermal Considerations

LM2419's transfer characteristic and power dissipation versus DC input voltage is shown in Figure. 5. Power supply current increases as the input voltage increases, consequently power dissipation increases. Considering a 20 % black retrace time in a 1024 x 768 display resolution application, the average power dissipation for continuous white screen is approximately 4.3 W per channel with 50V_{pp} output signal (black level at 75V and white level at 25V). For thermal and gain linearity considerations, the output low voltage (white level) should be maintained above 20V. If the device is operated at an output low voltage below 20V, the power dissipation might exceed 4.7W per channel (i.e 14W power dissipation for the device). Note that the device can be operated at lower power by reducing the peak to peak video output voltage to less than 50V and clamping the video black level close to the supply voltage.

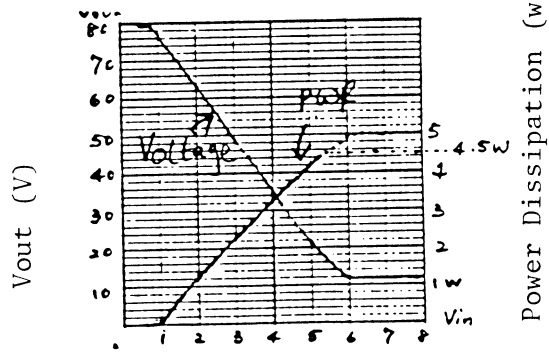
The LM2419 requires that the package be properly heat sunk under all operating conditions. Maximum ratings require that the device case temperature be limited to 90 °C maximum. Thus for 50 °C maximum ambient temperature and 13W power dissipation, the thermal resistance of the heat sink should be :

$$\theta_{sa} \leq (90 - 50)\,^{\circ}C \,/\, 13\,W = 3\,^{\circ}C/W$$



V_{out} (DC)

Fig. 4 Gain vs V_{out} (DC), Vin = 100 mVpp



Vin (V)

Fig.5 V_{out} & P.D vs Vin

PC Board Layout Considerations

For optimum performance, adequate ground plane, isolation between channels, good supply bypassing and minimizing unwanted feedback are necessary. The following book is highly recommended :

Ott, Henry. W, Noise Reduction Techniques in Electronic Systems,
John Wiley & Sons, New York, 1976.

LM6118/LM6218A/LM6218
Fast Settling Dual Operational Amplifier

General Description

The LM6118 series are monolithic fast-settling unity-gain-compensated dual operational amplifiers with ±20 mA output drive capability. The PNP input stage has a typical bias current of 200 nA, and the operating supply voltage is ±5V to ±20V.

These dual op amps use slew enhancement with special mirror circuitry to achieve fast response and high gain with low total supply current.

The amplifiers are built on a junction-isolated VIP™ (Vertically Integrated PNP) process which produces fast PNP's that complement the standard NPN's.

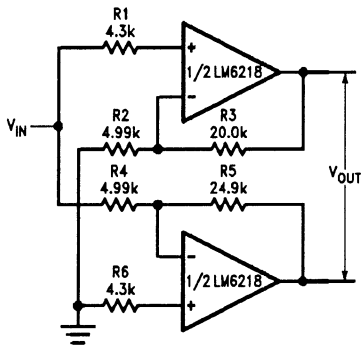
Features

	Typical
■ Low offset voltage	0.2 mV
■ 0.01% settling time	400 ns
■ Slew rate $A_V = -1$	140 V/μs
■ Slew rate $A_V = +1$	75 V/μs
■ Gain bandwidth	17 MHz
■ Total supply current	5.5 mA
■ Output drives 50Ω load (±1V)	

Applications

- D/A converters
- Fast integrators
- Active filters

Typical Applications



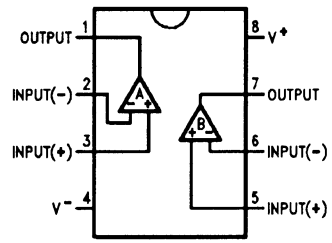
TL/H/10254–1

Single ended input to differential output
A_V = 10, BW = 3.2 MHz
40 V_{p-p} Response = 1.4 MHz
V_S = ±15V

Wide-Band, Fast-Settling 40 V_{p-p} Amplifier

Connection Diagrams and Order Information

Dual-In-Line Package (J or N)

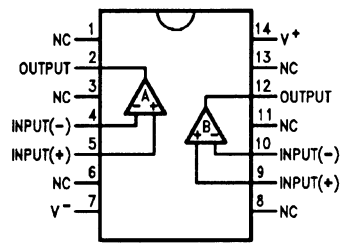


TL/H/10254–4

Top View

Order Number LM6118N, LM6118J/883, LM6218AN or LM6218N
See NS Package Number J08A or N08E

Small Outline Package (WM)



TL/H/10254–3

Top View

Order Number LM6218AWM or LM6218WM
See NS Package Number M14B

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Total Supply Voltage	42V
Input Voltage	(Note 2)
Differential Input Current (Note 3)	±10 mA
Output Current (Note 4)	Internally Limited
Power Dissipation (Note 5)	500 mW
ESD Tolerance (C = 100 pF, R = 1.5 kΩ)	±2 kV
Maximum Junction Temperature	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

Operating Temp. Range

LM6118, LM6118J/883	−55°C to +125°C
LM6218A	−40°C to +85°C
LM6218	−40°C to +85°C

Electrical Characteristics

$\pm 5V \le V_S \le \pm 20V$, $V_{CM} = 0V$, $V_{OUT} = 0V$, $I_{OUT} = 0A$, unless otherwise specified. Limits with standard type face are for $T_J = 25°C$, and **Bold Face Type** are for **Temperature Extremes.**

Parameter	Conditions	Typ 25°C	LM6118 Limits (Notes 6 & 7)	LM6218A Limits (Note 6)	LM6218 Limits (Note 6)	Units
Input Offset Voltage	$V_S = \pm 15V$	0.2	1 **2**	1 **2**	3 **4**	mV (max)
Input Offset Voltage	$V^- + 3V \le V_{CM} \le V^+ - 3.5V$	0.3	1.5 **2.5**	1.5 **2.5**	3.5 **4.5**	mV (max)
Input Offset Current	$V^- + 3V \le V_{CM} \le V^+ - 3.5V$	20	50 **250**	50 **100**	100 **200**	nA (max)
Input Bias Current	$V^- + 3V \le V_{CM} \le V^+ - 3.5V$	200	350 **950**	350 **950**	500 **1250**	nA (max)
Input Common Mode Rejection Ratio	$V^- + 3V \le V_{CM} \le V^+ - 3.5V$ $V_S = \pm 20V$	100	90 **85**	90 **85**	80 **75**	dB (min)
Positive Power Supply Rejection Ratio	$V^- = -15V$ $5V \le V^+ \le 20V$	100	90 **85**	90 **85**	80 **75**	dB (min)
Negative Power Supply Rejection Ratio	$V^+ = 15V$ $-20V \le V^- \le -5V$	100	90 **85**	90 **85**	80 **75**	dB (min)
Large Signal Voltage Gain	$V_{out} = \pm 17V$ $R_L = 10k$ $V_S = \pm 20V$	500	150 **100**	150 **100**	100 **70**	V/mV (min)
	$V_{out} = \pm 10V$ $R_L = 500$ $V_S = \pm 15V$ (± 20 mA)	200	50 **30**	50 **30**	40 **25**	V/mV (min)
Total Supply Current	$V_S = \pm 15V$	5.5	7 **7.5**	7 **7.5**	7 **7.5**	mA (max)
Output Current Limit	$V_S = \pm 15V$, Pulsed	65	100	100	100	mA (max)
Slew Rate, Av = −1	$V_S = \pm 15V$, $V_{out} = \pm 10V$ $R_S = R_f = 2k$, $C_f = 10$ pF	140	100 **50**	100 **50**	100 **50**	V/μs (min)
Slew Rate, Av = +1	$V_S = \pm 15V$, $V_{out} = \pm 10V$ $R_S = R_f = 2k$, $C_f = 10$ pF	75	50 **30**	50 **30**	50 **30**	V/μs (min)
Gain-Bandwidth Product	$V_S = \pm 15V$, $f_o = 200$ kHz	17	14	14	13	MHz (min)
0.01% Settling Time $A_V = -1$	$\Delta V_{out} = 10V$, $V_S = \pm 15V$, $R_S = R_f = 2k$, $C_f = 10$ pF	400				ns
Input Capacitance	Inverter	5				pF
	Follower	3				pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: Input voltage range is $(V^+ - 1V)$ to (V^-).

Note 3: The inputs are shunted with three series-connected diodes back-to-back for input differential clamping. Therefore differential input voltages greater than about 1.8V will cause excessive current to flow unless limited to less than 10 mA.

Note 4: Current limiting protects the output from a short to ground or any voltage less than the supplies. With a continuous overload, the package dissipation must be taken into account and heat sinking provided when necessary.

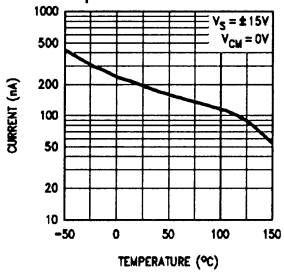
Note 5: Devices must be derated using a thermal resistance of 90°C/W for the N, J and WM packages.

Note 6: Limits are guaranteed by testing or correlation.

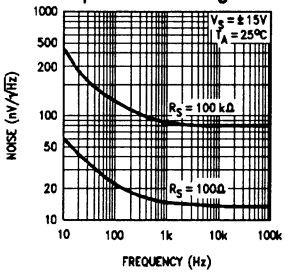
Note 7: A military RETS specification is available on request. At the time of printing, LM6118J/883 RETS spec complied with the **Boldface** limits in this column. The LM6118J/883 may also be procured as Standard Military Drawing device #5962-9156501MPX.

Typical Performance Characteristics

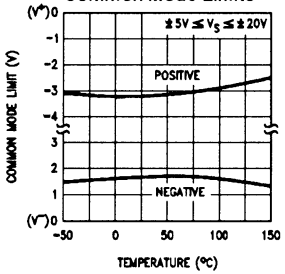
Input Bias Current



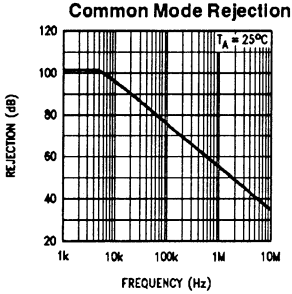
Input Noise Voltage



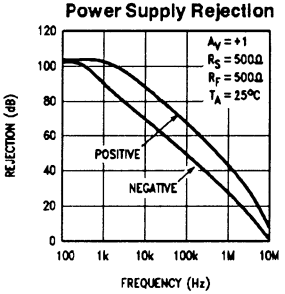
Common Mode Limits



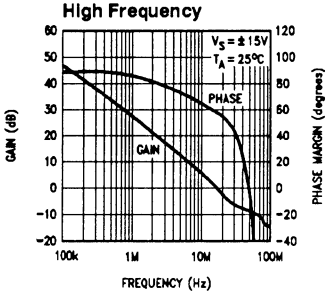
Common Mode Rejection



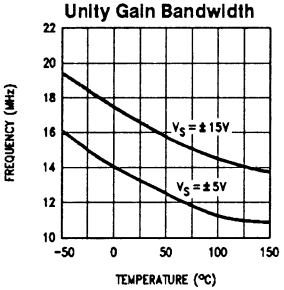
Power Supply Rejection



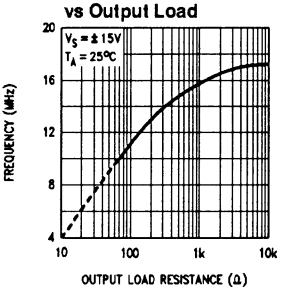
Frequency Response High Frequency



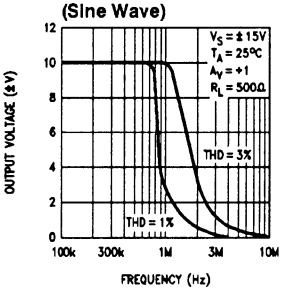
Unity Gain Bandwidth



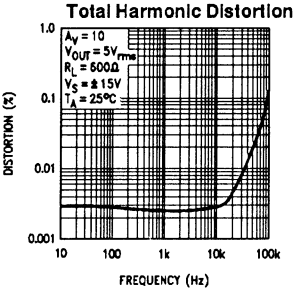
Unity Gain Bandwidth vs Output Load



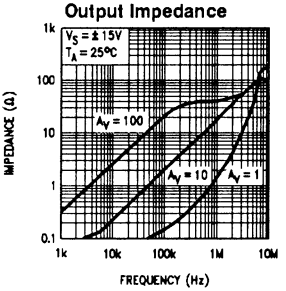
Large Signal Response (Sine Wave)



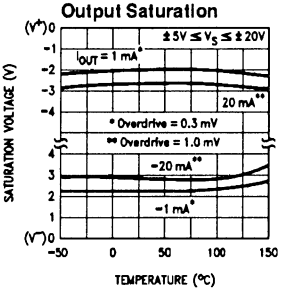
Total Harmonic Distortion



Output Impedance



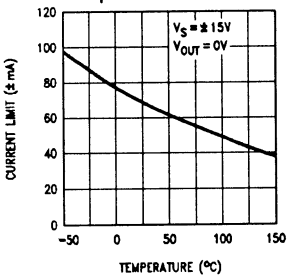
Output Saturation



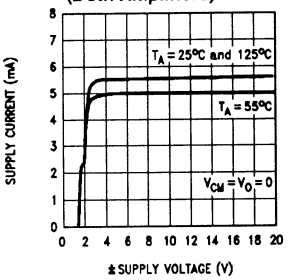
TL/H/10254–5

Typical Performance Characteristics (Continued)

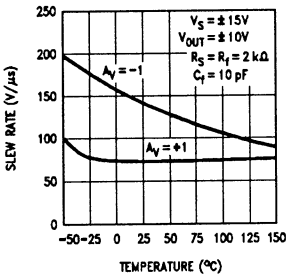
Output Current Limit



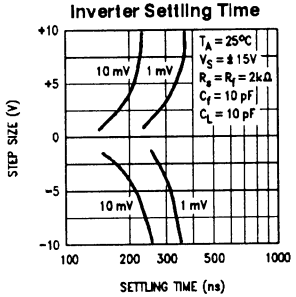
Supply Current (Both Amplifiers)



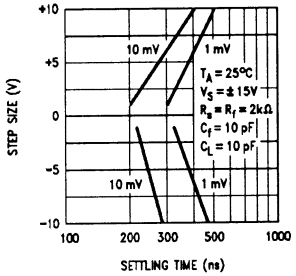
Slew Rate



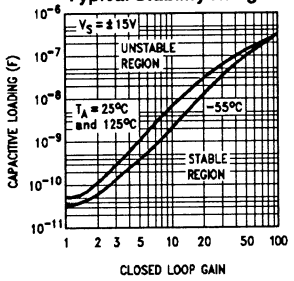
Inverter Settling Time



Follower Settling Time

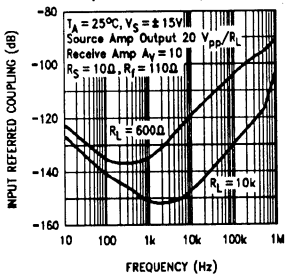


Typical Stability Range



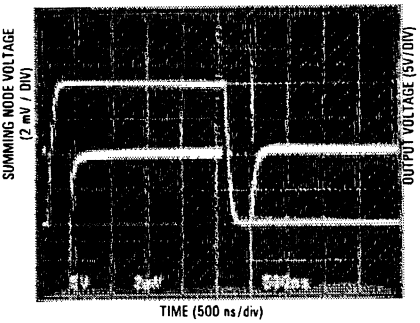
TL/H/10254–6

Amplifier to Amplifier Coupling



TL/H/10254–23

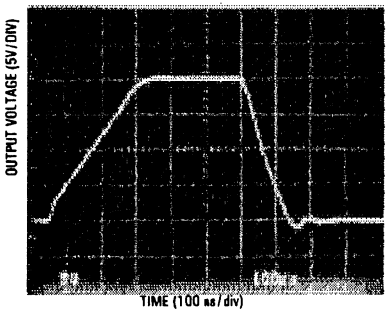
Settling Time, Vs = ± 15V



TL/H/10254–7

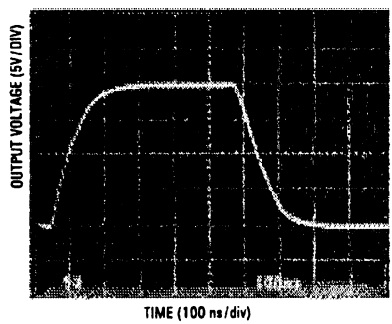
Typical Performance Characteristics (Continued)

Step Response, Av = +1, Vs = ±15V



TL/H/10254–8

Step Response, Av = −1, Vs = ±15V



TL/H/10254–9

Application Information

General

The LM6118 series are high-speed, fast-settling dual op-amps. To insure maximum performance, circuit board layout is very important. Minimizing stray capacitance at the inputs and reducing coupling between the amplifier's input and output will minimize problems.

Supply Bypassing

To assure stability, it is recommended that each power supply pin be bypassed with a 0.1 µF low inductance capacitor near the device. If high frequency spikes from digital circuits or switching supplies are present, additional filtering is recommended. To prevent these spikes from appearing at the output, R-C filtering of the supplies near the device may be necessary.

Power Dissipation

These amplifiers are specified to 20 mA output current. If accompanied with high supply voltages, relatively high power dissipation in the device will occur, resulting in high junction temperatures. In these cases the package thermal resistance must be taken into consideration. (See Note 5 under Electrical Characteristics.) For high dissipation, an N package with large areas of copper on the pc board is recommended.

Amplifier Shut Down

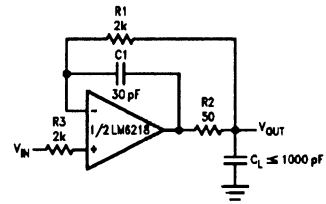
If one of the amplifiers is not used, it can be shut down by connecting both the inverting and non-inverting inputs to the V^- pin. This will reduce the power supply current by approximately 25%.

Capacitive Loading

Maximum capacitive loading is about 50 pF for a closed-loop gain of +1, before the amplifier exhibits excessive ringing and becomes unstable. A curve showing maximum capacitive loads, with different closed-loop gains, is shown in the Typical Performance Characteristics section.

To drive larger capacitive loads at low closed-loop gains, isolate the amplifier output from the capacitive load with 50Ω. Connect a small capacitor directly from the amplifier output to the inverting input. The feedback loop is closed from the isolated output with a series resistor to the inverting input.

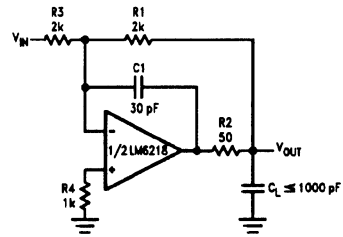
Voltage Follower



TL/H/10254–10

For C_L = 1000 pF, Small signal BW = 5 MHz
20 V_{p-p} BW = 500 kHz

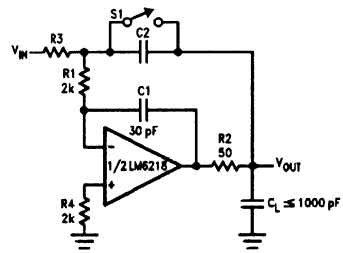
Inverter



TL/H/10254–11

Settling time to 0.01%, 10V Step
For C_L = 1000 pF, settling time ≈ 1500 ns
For C_L = 300 pF, settling time ≈ 500 ns

Integrator



TL/H/10254–12

Application Information (Continued)

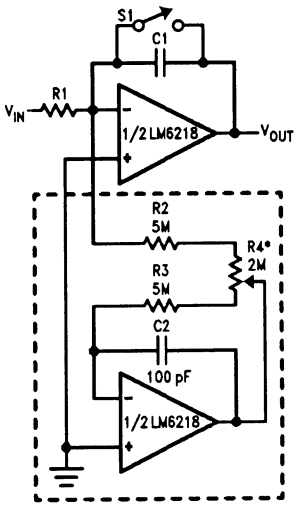
Examples of unity gain connections for a voltage follower, Inverter, and integrator driving capacitive loads up to 1000 pF are shown here. Different R1–C1 time constants and capacitive loads will have an effect on settling times.

Input Bias Current Compensation

Input bias current of the first op amp can be reduced or balanced out by the second op amp. Both amplifiers are laid out in mirror image fashion and in close proximity to each other, thus both input bias currents will be nearly identical and will track with temperature. With both op amp inputs at the same potential, a second op amp can be used to convert bias current to voltage, and then back to current feeding the first op amp using large value resistors to reduce the bias current to the level of the offset current.

Examples are shown here for an inverting application, (a) where the inputs are at ground potential, and a second circuit (b) for compensating bias currents for both inputs.

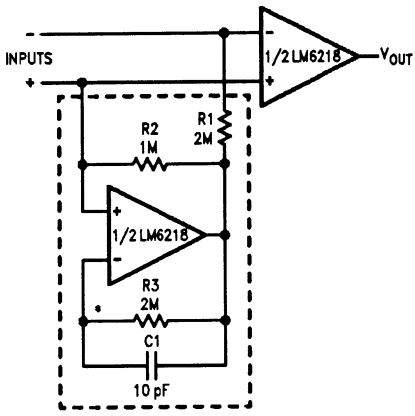
Bias Current Compensation



TL/H/10254–13

*adjust for zero integrator drift

(a) Inverting Input Bias Compensation for Integrator Application

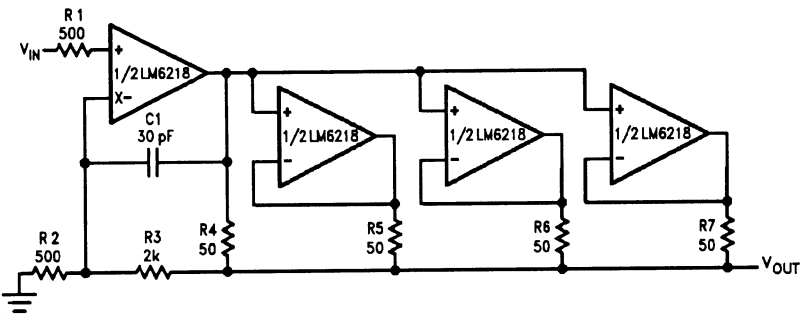


TL/H/10254–14

*mount resistor close to input pin to minimize stray capacitance

(b) Compensation to Both Inputs

Amplifier/Parallel Buffer



TL/H/10254–15

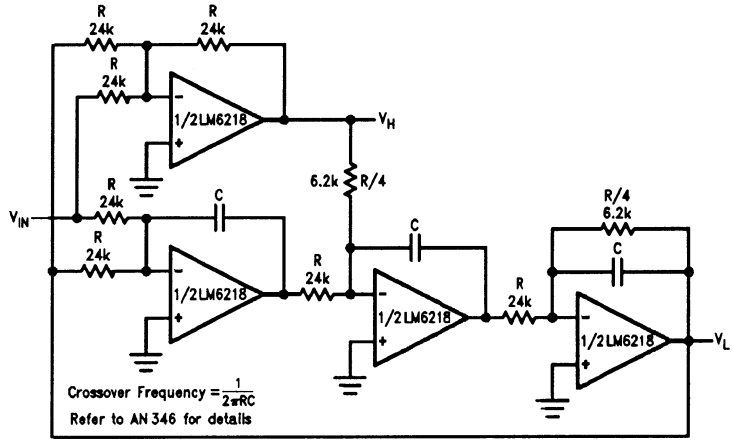
A_V = +5, $I_{OUT} \leq$ 80 mA

V_S = ±15V, $C_L \leq$ 0.01 µF

Large and small signal B.W. = 1.3 MHz (THD = 3%)

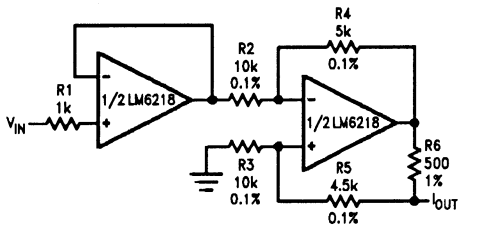
Application Information (Continued)

Constant-Voltage Crossover Network With 12 dB/Octave Slope



TL/H/10254–16

Bilateral Current Source



TL/H/10254–17

$V_S = \pm 15V$, $-10 \leq V_{IN} \leq 10V$

$\frac{I_{OUT}}{V_{IN}} = \frac{R4}{R2\ R6} = \frac{1\ mA}{1V}$

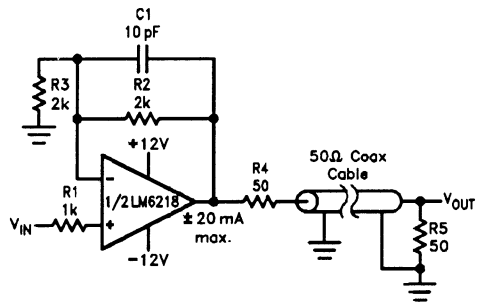
Output dynamic range = 10V − R6 I_{OUT}

R_L = 500Ω, small signal BW = 6 MHz

Large signal response = 800 kHz

C_{out} equiv. = $\frac{R2 + R4}{2\pi\ f_O\ R2\ R6}$ = 32 pF (f_O = 15 MHz)

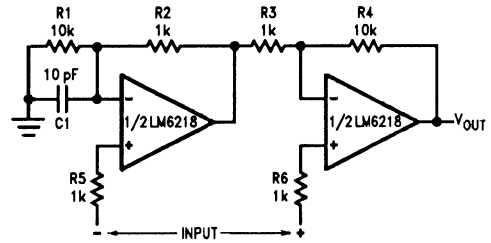
Coaxial Cable Driver



TL/H/10254–19

Small signal (200 mV_{p-p}) BW ≈ 5 MHz

Instrumentation Amplifier

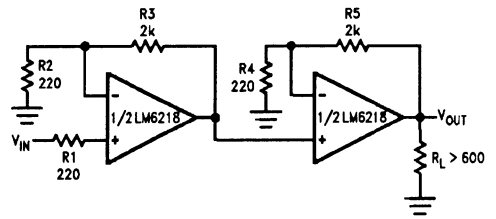


TL/H/10254–18

A_V = 10, $V_S = \pm 15V$, All resistors 0.01%

Small signal and large signal (20 V_{P-P}) B.W. ≈ 800 kHz

150 MHz Gain-Bandwidth Amplifier



TL/H/10254–20

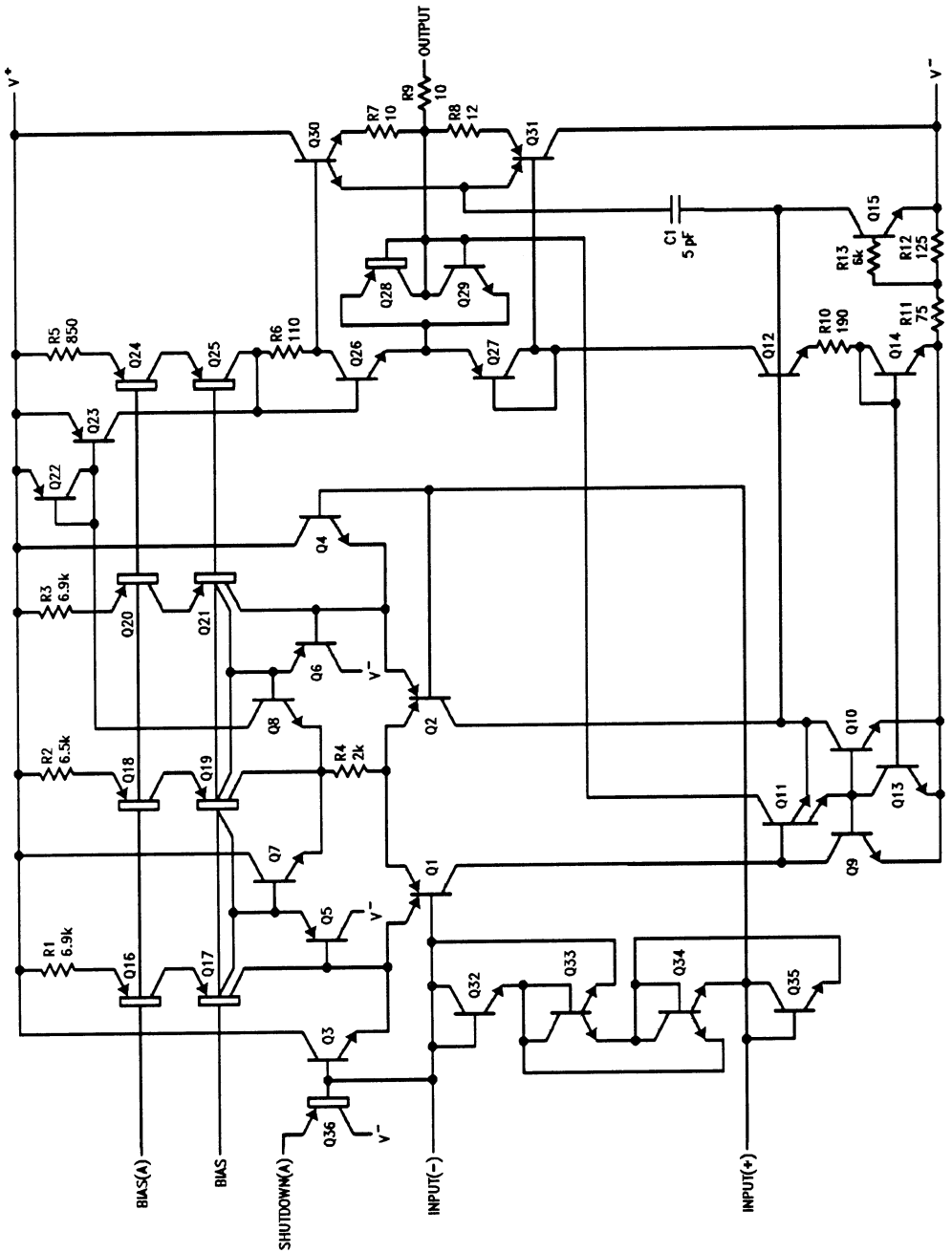
A_V = 100, $V_S = \pm 15V$,

Small signal BW ≈ 1.5 MHz

Large signal BW (20 V_{p-p}) ≈ 800 kHz

Schematic Diagram

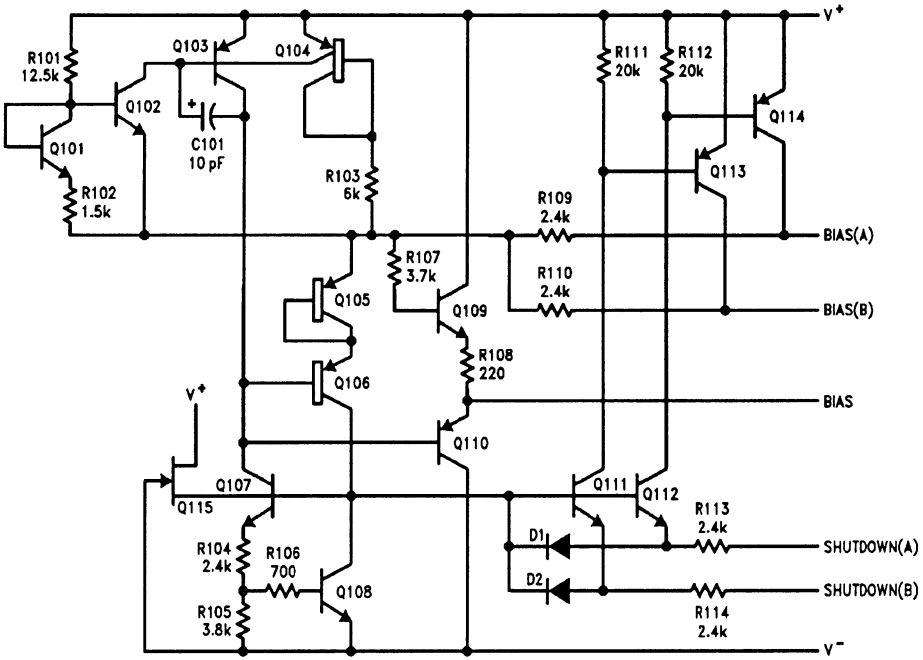
½ LM6118 (Op Amp A)



TL/H/10254–21

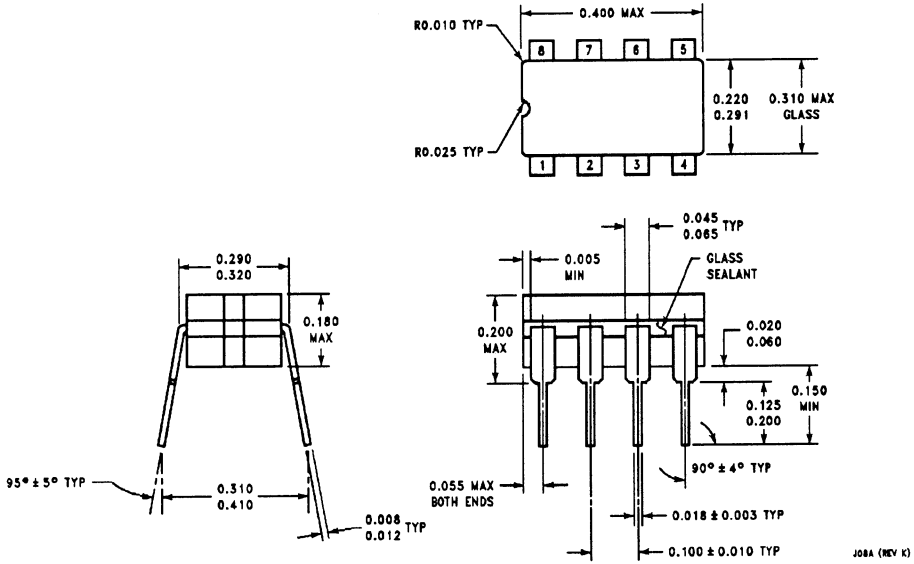
Schematic Diagram (Continued)

Bias Circuit



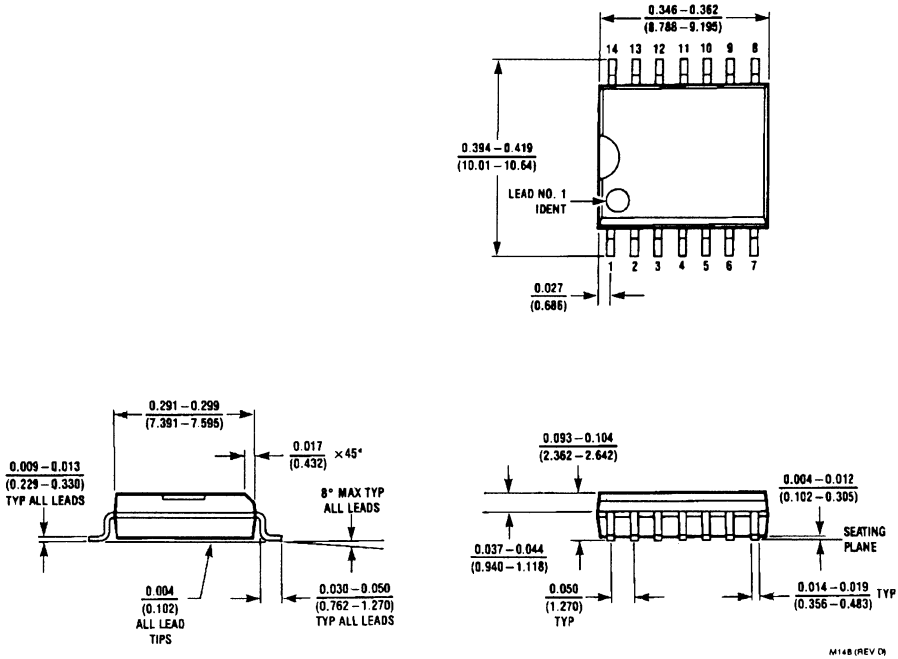
TL/H/10254–22

Physical Dimensions inches (millimeters)



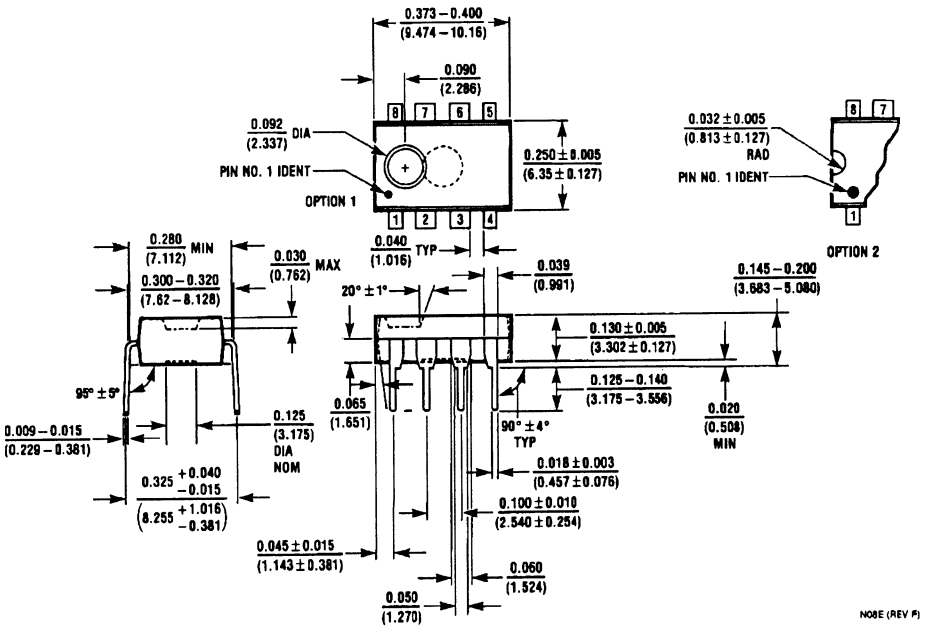
8-Lead Ceramic Dual-In-Line Package (J)
Order Number LM6118J/883
NS Package Number J08A

Physical Dimensions inches (millimeters)



8-Lead Molded Small Outline Package (M)
Order Number LM6218AWM or LM6218WM
NS Package Number M14B

Physical Dimensions inches (millimeters) (Continued)



8-Lead Molded Dual-In-Line Package (N)
Order Number LM6118N, LM6218AN or LM6218N
NS Package Number N08E

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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National Semiconductor

November 1990

LM6162/LM6262/LM6362
High Speed Operational Amplifier

General Description

The LM6362 family of high-speed amplifiers exhibits an excellent speed-power product, delivering 300 V/μs and 100 MHz gain-bandwidth product (stable for gains as low as +2 or −1) with only 5 mA of supply current. Further power savings and application convenience are possible by taking advantage of the wide dynamic range in operating supply voltage which extends all the way down to +5V.

These amplifiers are built with National's VIP™ (Vertically Integrated PNP) process which provides fast transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

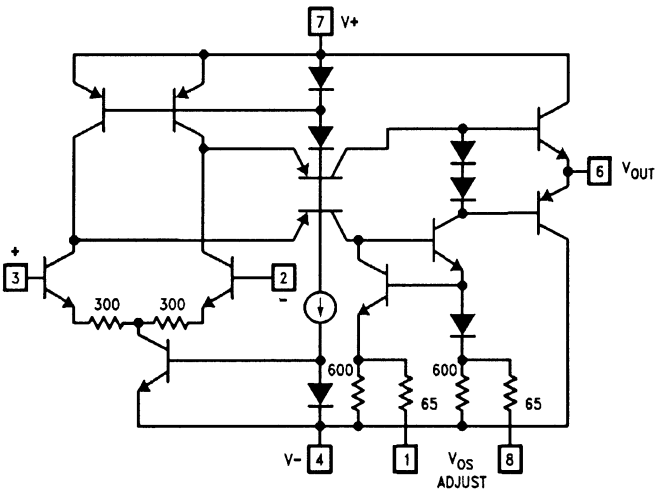
Features

- High slew rate — 300 V/μs
- High gain-bandwidth product — 100 MHz
- Low supply current — 5 mA
- Fast settling time — 120 ns to 0.1%
- Low differential gain — <0.1%
- Low differential phase — <0.1°
- Wide supply range — 4.75V to 32V
- Stable with unlimited capacitive load
- Well behaved; easy to apply

Applications

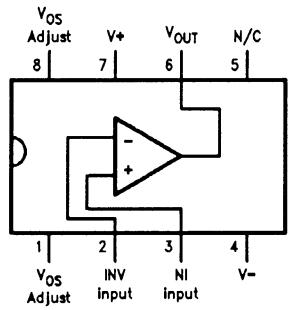
- Video amplifier
- Wide-bandwidth signal conditioning for image processing (FAX, scanners, laser printers)
- Hard disk drive preamplifier
- Error amplifier for high-speed switching regulator

Simplified Schematic



TL/H/11061–1

Connection Diagram



TL/H/11061–2

Order Number LM6162N, LM6262N or LM6362N
See NS Package Number N08E

Order Number LM6262M or LM6362M
See NS Package Number M08A

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	36V
Differential Input Voltage (Note 2)	±8V
Common-Mode Input Voltage (Note 3)	($V^+ - 0.7V$) to ($V^- - 0.3V$)
Output Short Circuit to GND (Note 4)	Continuous
Soldering Information	
Dual-In-Line Package (N)	
Soldering (10 seconds)	260°C
Small Outline Package (M)	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Storage Temperature Range	$-65°C \le T_J \le +150°C$
Max Junction Temperature	150°C
ESD Tolerance (Note 5)	±1100V

Operating Ratings

Temperature Range (Note 6)	
LM6162	$-55°C \le T_J \le +125°C$
LM6262	$-25°C \le T_J \le +85°C$
LM6362	$0°C \le T_J \le +70°C$
Supply Voltage Range	4.75V to 32V

DC Electrical Characteristics

These limits apply for supply voltage = ±15V, V_{CM} = 0V, and $R_L \ge 100\ k\Omega$, unless otherwise specified. Limits in standard typeface are for $T_A = T_J = 25°C$; limits in **boldface type** apply over the **Operating Temperature Range.**

Symbol	Parameter	Conditions	Typical (Note 7)	LM6162 Limit (Note 8)	LM6262 Limit (Note 8)	LM6362 Limit (Note 8)	Units
V_{OS}	Input Offset Voltage		±3	±5 **±8**	±5 **±8**	±13 **±15**	mV max
$\frac{\Delta V_{OS}}{\Delta Temp}$	Input Offset Voltage Average Drift		7				µV/°C
I_{bias}	Input Bias Current		2.2	3 **6**	3 **5**	4 **6**	µA max
I_{OS}	Input Offset Current		±150	±350 **±800**	±350 **±600**	±1500 **±1900**	nA max
$\frac{\Delta I_{OS}}{\Delta Temp}$	Input Offset Current Average Drift		0.3				nA/°C
R_{IN}	Input Resistance	Differential	180				kΩ
C_{IN}	Input Capacitance		2.0				pF
A_{VOL}	Large Signal Voltage Gain	V_{OUT} = ±10V, R_L = 2 kΩ (Note 9)	1400	1000 **500**	1000 **700**	800 **650**	V/V min
		R_L = 10 kΩ	6500				V/V
V_{CM}	Input Common-Mode Voltage Range	Supply = ±15V	+14.0	+13.9 **+13.8**	+13.9 **+13.8**	+13.8 **+13.7**	V min
			−13.2	−12.9 **−12.7**	−12.9 **−12.7**	−12.9 **−12.8**	V max
		Supply = +5V (Note 10)	4.0	3.9 **3.8**	3.9 **3.8**	3.8 **3.7**	V min
			1.6	1.8 **2.0**	1.8 **2.0**	1.9 **2.0**	V max
CMRR	Common-Mode Rejection Ratio	$-10V \le V_{CM} \le +10V$	100	83 **79**	83 **79**	76 **74**	dB min
PSRR	Power Supply Rejection Ratio	$\pm 10V \le V_S \le \pm 16V$	93	83 **79**	83 **79**	76 **74**	dB min
V_O	Output Voltage Swing	Supply = ±15V, R_L = 2 kΩ	+14.2	+13.5 **+13.3**	+13.5 **+13.3**	+13.4 **13.3**	V min
			−13.4	−13.0 **−12.7**	−13.0 **−12.8**	−12.9 **−12.8**	V max

DC Electrical Characteristics (Continued)

These limits apply for supply voltage = ±15V, V_{CM} = 0V, and $R_L \geq 100\ k\Omega$, unless otherwise specified. Limits in standard typeface are for $T_A = T_J = 25°C$; limits in **boldface type** apply over the **Operating Temperature Range.**

Symbol	Parameter	Conditions	Typical (Note 7)	LM6162 Limit (Note 8)	LM6262 Limit (Note 8)	LM6362 Limit (Note 8)	Units
V_O	Output Voltage Swing	Supply = +5V and R_L = 2 kΩ (Note 10)	4.2	3.5 **3.3**	3.5 **3.3**	3.4 **3.3**	V min
			1.3	1.7 **2.0**	1.7 **1.9**	1.8 **1.9**	V max
I_{OSC}	Output Short Circuit Current	Sourcing	65	30 **20**	30 **25**	30 **25**	mA min
		Sinking	65	30 **20**	30 **25**	30 **25**	mA min
I_S	Supply Current		5.0	6.5 **6.8**	6.5 **6.7**	6.8 **6.9**	mA max
GBW	Gain-Bandwidth Product	f = 20 MHz	100	80 **55**	80 **65**	75 **65**	MHz min
		Supply = ±5V	70				MHz
SR	Slew Rate	A_V = +2 (Note 11)	300	200 **180**	200 **180**	200 **180**	V/μs min
		Supply = ±5V	200				V/μs
PBW	Power Bandwidth	V_{OUT} = 20 V_{PP}	4.5				MHz
t_s	Settling Time	10V step, to 0.1% A_V = −1, R_L = 2 kΩ	100				ns
ϕ_m	Phase Margin	A_V = +2	45				deg
	Differential Gain	NTSC, A_V = +2	<0.1				%
	Differential Phase	NTSC, A_V = +2	<0.1				deg
e_n	Input Noise Voltage	f = 10 kHz	10				nV/√Hz
i_n	Input Noise Current	f = 10 kHz	1.2				pA/√Hz

Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: The ESD protection circuitry between the inputs will begin to conduct when the differential input voltage reaches 8V.

Note 3: a) In addition, the voltage between the V^+ pin and either input pin must not exceed 36V.
b) When the voltage applied to an input pin is driven more than 0.3V below the negative supply pin voltage, a substrate diode begins to conduct. Current through this pin must then be kept less than 20 mA to limit damage from self-heating.

Note 4: Although the output current is internally limited, continuous short-circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

Note 5: This value is the average voltage that the weakest pin combinations can withstand and still conform to the datasheet limits. The test circuit used consists of the human body model, 100 pF in series with 1500Ω.

Note 6: The typical thermal resistance, junction-to-ambient, of the molded plastic DIP (N package) is 105°C/W. For the molded plastic SO (M package), use 155°C/W. All numbers apply for packages soldered directly into a printed circuit board.

Note 7: Typical values are for T_J = 25°C, and represent the most likely parametric norm.

Note 8: Limits are guaranteed, by testing or correlation.

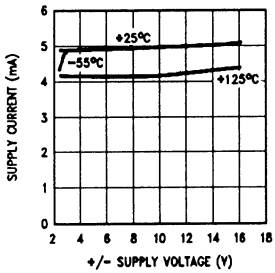
Note 9: Voltage Gain is the total output swing (20V) divided by the magnitude of the input signal required to produce that swing.

Note 10: For single-supply operation, the following conditions apply: V^+ = 5V, V^- = 0V, V_{CM} = 2.5V, V_{OUT} = 2.5V. Pin 1 and Pin 8 (V_{OS} Adjust pins) are each connected to pin 4 (V^-) to realize maximum output swing. This connection will increase the offset voltage.

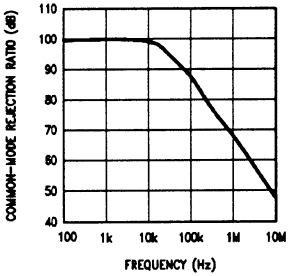
Note 11: V_{IN} = 10V step. For ±5V supplies, V_{IN} = 1V step.

Typical Performance Characteristics $R_L = 10\,k\Omega$, $T_A = 25°C$ unless otherwise noted

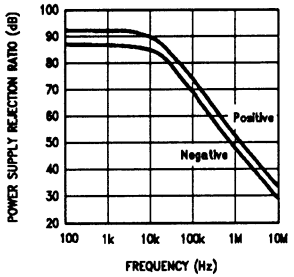
Supply Current vs Supply Voltage



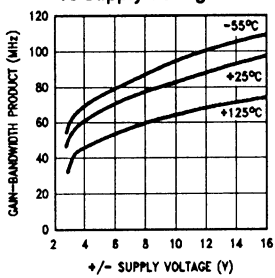
Common-Mode Rejection Ratio



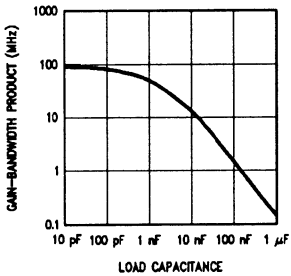
Power Supply Rejection Ratio



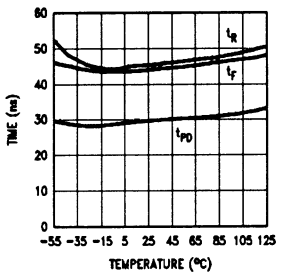
Gain-Bandwidth Product vs Supply Voltage



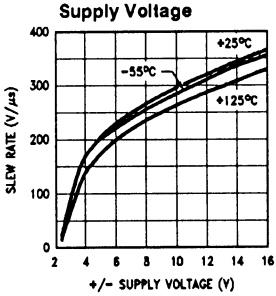
Gain-Bandwidth Product vs Load Capacitance



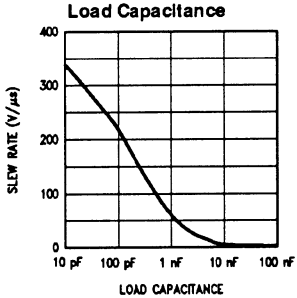
Propagation Delay, Rise and Fall Times



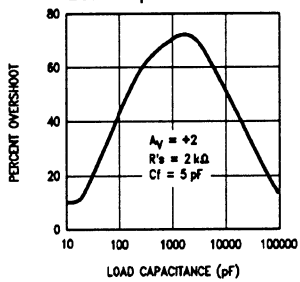
Slew Rate vs Supply Voltage



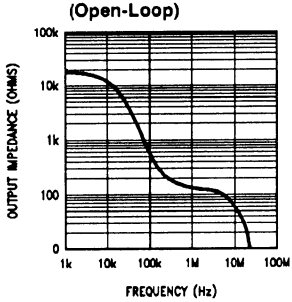
Slew Rate vs Load Capacitance



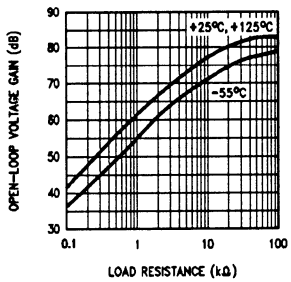
Overshoot vs Load Capacitance



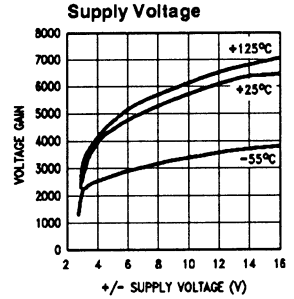
Output Impedance (Open-Loop)



Voltage Gain vs Load Resistance



Voltage Gain vs Supply Voltage

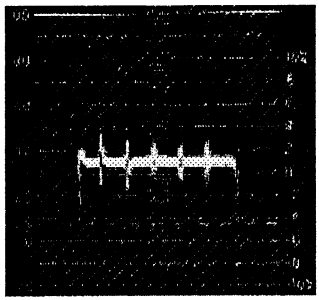


TL/H/11061–3

Typical Performance Characteristics (Continued)

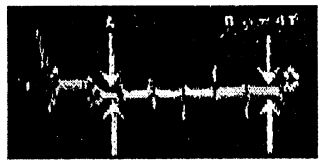
R_L = 10 kΩ, T_A = 25°C unless otherwise noted

Differential Gain (Note)



TL/H/11061–4

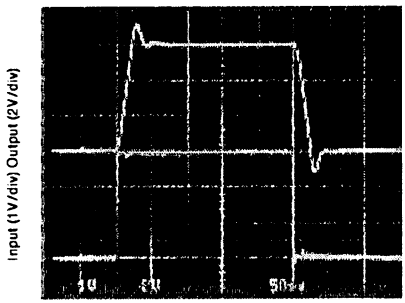
Differential Phase (Note)



TL/H/11061–5

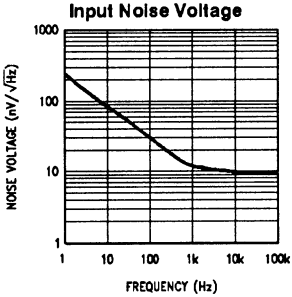
Note: Differential gain and differential phase measured for four series LM6362 op amps configured with gain of +2 each, in series with a 1:16 attenuator and an LM6321 buffer. Error added by LM6321 is negligible. Test performed using Tektronix Type 520 NTSC test system.

Step Response; Av = +2

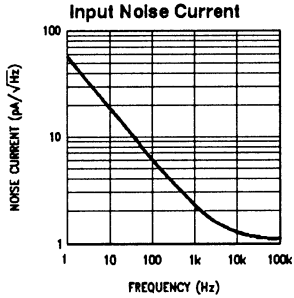


TL/H/11061–6

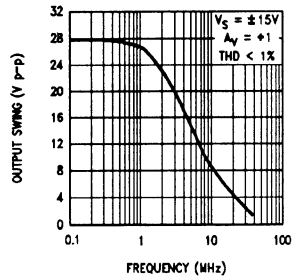
Input Noise Voltage



Input Noise Current



Power Bandwidth

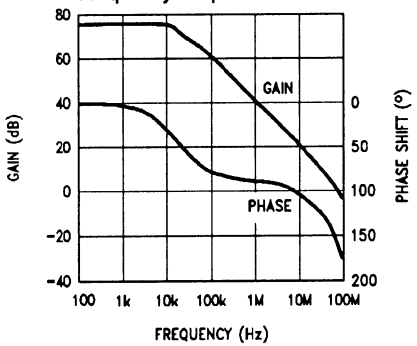


TL/H/11061–7

Typical Performance Characteristics (Continued)

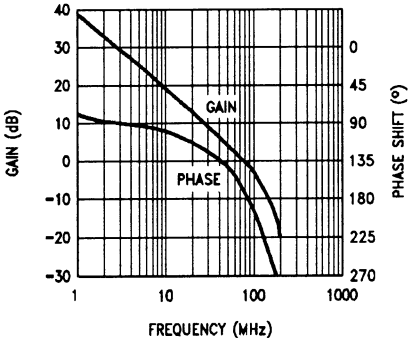
R_L = 10 kΩ, T_A = 25°C unless otherwise noted

Open-Loop Frequency Response



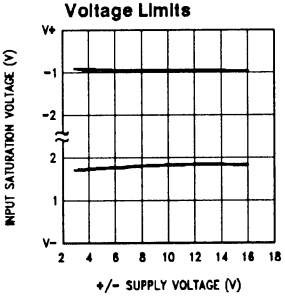
TL/H/11061–8

Open-Loop High-Frequency Response

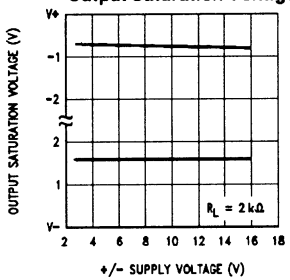


TL/H/11061–9

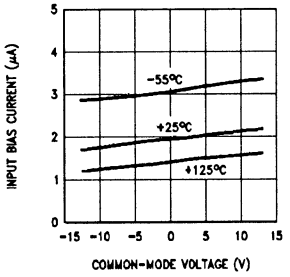
Common-Mode Input Voltage Limits



Output Saturation Voltage



Bias Current vs Common-Mode Voltage



TL/H/11061–10

Application Tips

The LM6362 has been decompensated for a wider gain-bandwidth product than the LM6361. However, the LM6362 still offers stability at gains of 2 (and −1) or greater over the specified ranges of temperature, power supply voltage, and load. Since this decompensation involved reducing the emitter-degeneration resistors in the op amp's input stage, the DC precision has been increased in the form of lower offset voltage and higher open-loop gain.

Other op amps in this family include the LM6361, LM6364, and LM6365. If unity-gain stability is required, the LM6361 should be used. The LM6364 has been decompensated for operation at gains of 5 or more, with corresponding greater gain-bandwidth product (125 MHz, typical) and DC precision. The fully-uncompensated LM6365 offers gain-bandwidth product of 725 MHz, typical, and is stable for gains of 25 or more. All parts in this family, regardless of compensation, have the same high slew rate of 300 V/μs (typ).

The LM6362 is unusually tolerant of capacitive loads. Most op amps tend to oscillate when their load capacitance is greater than about 200 pF (in low-gain circuits). However, load capacitance on the LM6362 effectively increases its compensation capacitance, thus slowing the op amp's response and reducing its bandwidth. The compensation is not ideal, though, and ringing may occur in low-gain circuits with large capacitive loads.

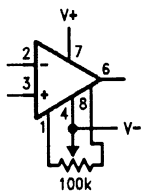
Power supply bypassing is not as critical for LM6362 as it is for other op amps in its speed class. However, bypassing will improve the stability and transient response of the LM6362, and is recommended for every design. 0.01 μF to 0.1 μF ceramic capacitors should be used (from each supply "rail" to ground); if the device is far away from its power supply source, an additional 2.2 μF to 10 μF of tantalum may be required for extra noise reduction.

Keep all leads short to reduce stray capacitance and lead inductance, and make sure ground paths are low-impedance, especially where heavier currents will be flowing. Stray capacitance in the circuit layout can cause signal coupling from one pin, input or lead to another, and can cause circuit gain to unintentionally vary with frequency.

Breadboarded circuits will work best if they are built using generic PC boards with a good ground plane. If the op amps are used with sockets, as opposed to being soldered into the circuit, the additional input capacitance may degrade circuit frequency response. At low gains (+2 or −1), a feedback capacitor C_f from output to inverting input will compensate for the phase lag caused by capacitance at the inverting input. Typically, values from 2 pF to 5 pF work well; however, best results can be obtained by observing the amplifier pulse response and optimizing C_f for the particular layout.

Typical Applications

Offset Voltage Adjustment



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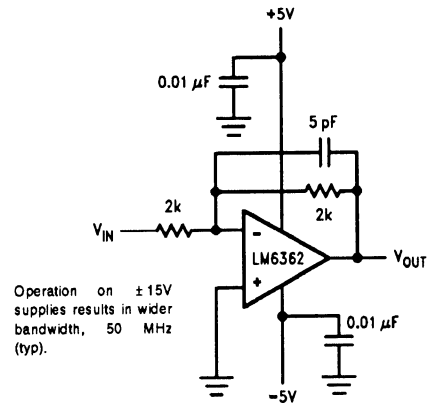
Inverting Amplifier, 30 MHz Bandwidth

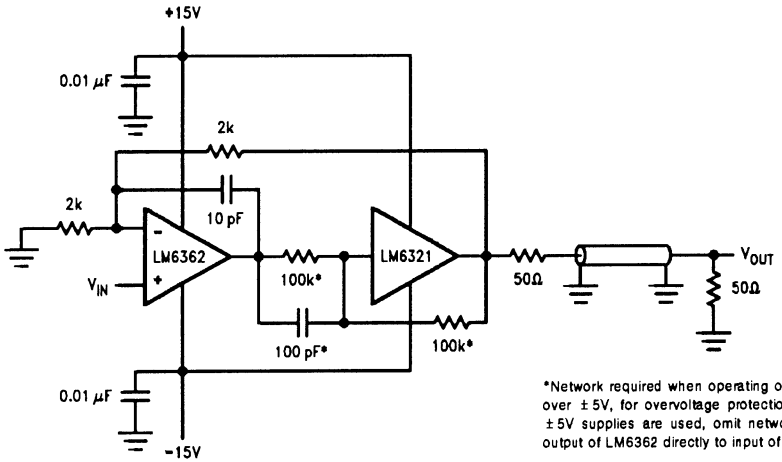


Operation on ±15V supplies results in wider bandwidth, 50 MHz (typ).

TL/H/11061-12

Typical Applications (Continued)

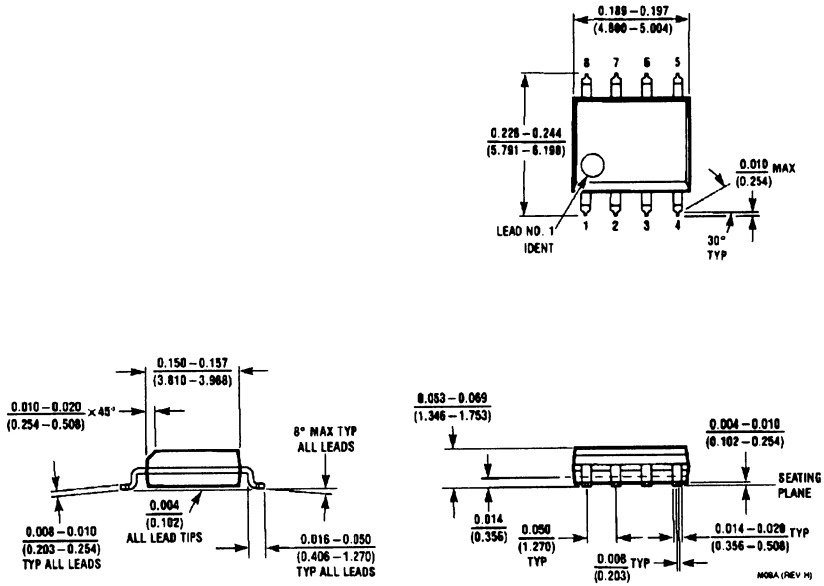
Video Cable Driver



*Network required when operating on supply voltage over ±5V, for overvoltage protection of LM6321. If ±5V supplies are used, omit network and connect output of LM6362 directly to input of LM6321.

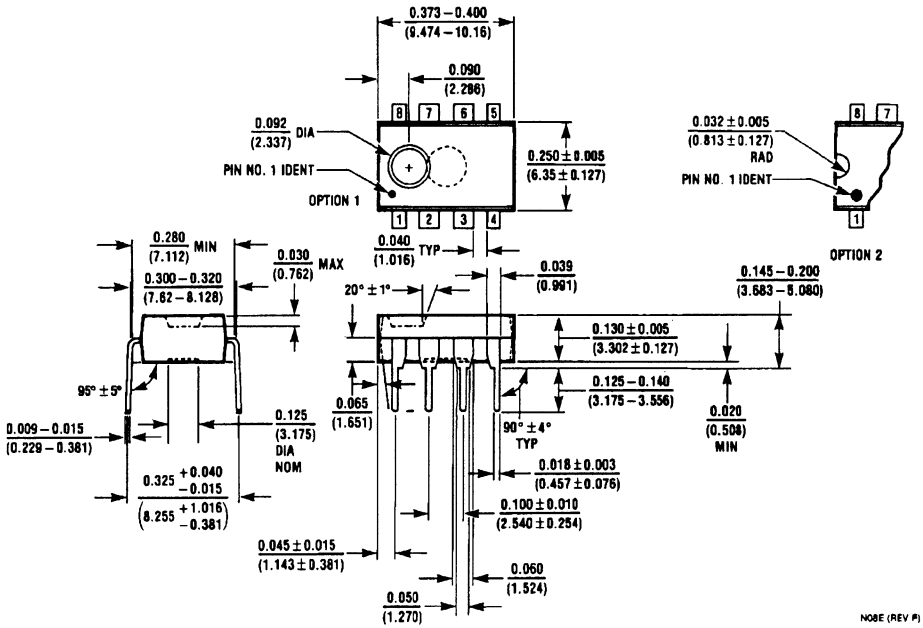
TL/H/11061–13

Physical Dimensions inches (millimeters)



Molded Package SO (M)
Order Number LM6262M or LM6362M
NS Package Number M08A

Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)
Order Number LM6162N, LM6262N or LM6362N
NS Package Number N08E

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National Semiconductor

April 1992

LM6181 100 mA, 100 MHz Current Feedback Amplifier

General Description

The LM6181 current-feedback amplifier offers an unparalleled combination of bandwidth, slew-rate, and output current. The amplifier can directly drive up to 100 pF capacitive loads without oscillating and a 10V signal into a 50Ω or 75Ω back-terminated coax cable system over the full industrial temperature range. This represents a radical enhancement in output drive capability for an 8-pin high-speed amplifier making it ideal for video applications.

Built on National's advanced high-speed VIP™ II (Vertically Integrated PNP) process, the LM6181 employs current-feedback providing bandwidth that does not vary dramatically with gain; 100 MHz at $A_V = -1$, 60 MHz at $A_V = -10$. With a slew rate of 2000V/μs, 2nd harmonic distortion of −50 dBc at 10 MHz and settling time of 50 ns (0.1%) the LM6181 dynamic performance makes it ideal for data acquisition, high speed ATE, and precision pulse amplifier applications.

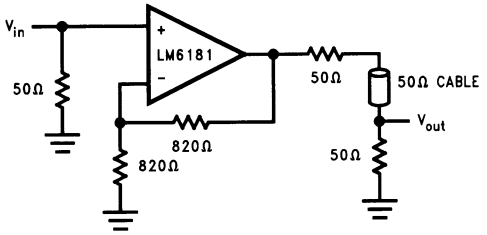
Features (Typical unless otherwise noted)

- Slew rate 2000 V/μs
- Settling time (0.1%) 50 ns
- Characterized for supply ranges ±5V and ±15V
- Low differential gain and phase error 0.05%, 0.04°
- High output drive ±10V into 100Ω
- Guaranteed bandwidth and slew rate
- Improved performance over EL2020, OP160, AD844, LT1223 and HA5004

Applications

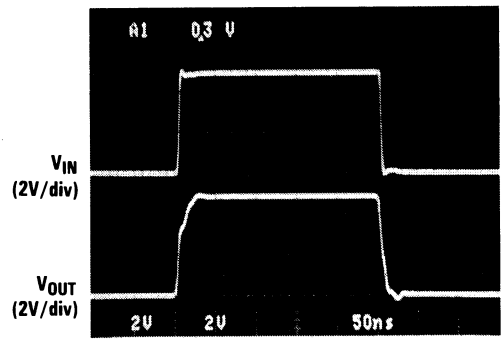
- Coax cable driver
- Video amplifier
- Flash ADC buffer
- High frequency filter

Typical Application



TL/H/11328–1

Cable Driver

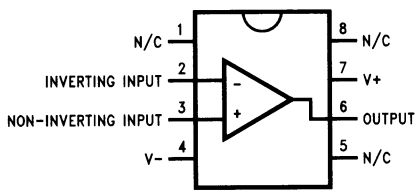


TIME (50ns/div)

TL/H/11328–2

Connection Diagrams (For Ordering Information See Back Page)

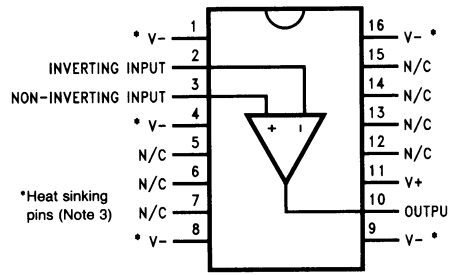
Dual-In-Line Package (N)



TL/H/11328–3

Order Number LM6181IN, LM6181AIN or LM6181AMN
See NS Package Number N08E

Small Outline Package (M)



TL/H/11328–4

Order Number LM6181IM or LM6181AIM
See NS Package Number M16A

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 TL/H/11328

RRD-B20M42/Printed in U. S. A.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±18V
Differential Input Voltage	±6V
Input Voltage	±Supply Voltage
Inverting Input Current	15 mA
Soldering Information	
Dual-In-Line Package (N) Soldering (10 sec)	260°C
Small Outline Package (M)	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
Output Short Circuit	(Note 7)
Storage Temperature Range	$-65°C \le T_J \le +150°C$
Maximum Junction Temperature	150°C
ESD Rating (Note 2)	±3000V

Operating Ratings

Supply Voltage Range	7V to 32V
Junction Temperature Range (Note 3)	
LM6181AM	$-55°C \le T_J \le +125°C$
LM6181AI, LM6181I	$-40°C \le T_J \le +85°C$

DC Electrical Characteristics

The following specifications apply for **Supply Voltage** = ±**15V**, and R_L = 1 kΩ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits T_J = 25°C.

Symbol	Parameter	Conditions	LM6181AM		LM6181AI		LM6181I		Units
			Typical (Note 4)	Limit (Note 5)	Typical (Note 4)	Limit (Note 5)	Typical (Note 4)	Limit (Note 5)	
V_{OS}	Input Offset Voltage		2.0	5.0 **5.0**	2.0	5.0 **5.0**	3.5	7.0 **7.0**	mV max
TC V_{OS}	Input Offset Voltage Drift		5.0		5.0		5.0		µV/°C
I_B	Inverting Input Bias Current		2.0	5.0 **12.0**	2.0	5.0 **12.0**	5.0	10 **17.0**	µA max
	Non-Inverting Input Bias Current		0.5	1.5 **3.0**	0.5	1.5 **3.0**	2.0	3.0 **5.0**	
TC I_B	Inverting Input Bias Current Drift		30		30		30		nA/°C
	Non-Inverting Input Bias Current Drift		10		10		10		
I_B PSR	Inverting Input Bias Current Power Supply Rejection	V_S = ±4.5V, ±16V	0.3	0.5 **3.0**	0.3	0.5 **3.0**	0.3	0.75 **4.5**	µA/V max
	Non-Inverting Input Bias Current Power Supply Rejection	V_S = ±4.5V, ±16V	0.05	0.5 **1.5**	0.05	0.5 **1.5**	0.05	0.5 **3.0**	
I_B CMR	Inverting Input Bias Current Common Mode Rejection	$-10V \le V_{CM} \le +10V$	0.3	0.5 **0.75**	0.3	0.5 **0.75**	0.3	0.75 **1.0**	
	Non-Inverting Input Bias Current Common Mode Rejection	$-10V \le V_{CM} \le +10V$	0.1	0.5 **0.5**	0.1	0.5 **0.5**	0.1	0.5 **0.5**	
CMRR	Common Mode Rejection Ratio	$-10V \le V_{CM} \le +10V$	60	50 **50**	60	50 **50**	60	50 **50**	dB min
PSRR	Power Supply Rejection Ratio	V_S = ±4.5V, ±16V	80	70 **70**	80	70 **70**	80	70 **65**	dB min
R_O	Output Resistance	A_V = −1, f = 300 kHz	0.2		0.2		0.2		Ω
R_{IN}	Non-Inverting Input Resistance		10	5.0 **5.0**	10	5.0 **5.0**	10	2.5 **2.5**	MΩ min
V_O	Output Voltage Swing	R_L = 1 kΩ	12	11 **11**	12	11 **11**	12	11 **11**	V min
		R_L = 100Ω	11	10 **7.5**	11	10 **8.0**	11	10 **8.0**	
I_{SC}	Output Short Circuit Current		130	100 **75**	130	100 **85**	130	100 **85**	mA min

DC Electrical Characteristics (Continued)

The following specifications apply for **Supply Voltage** = ±**15V**, and R_L = 1 kΩ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits T_J = 25°C.

Symbol	Parameter	Conditions	LM6181AM		LM6181AI		LM6181I		Units
			Typical (Note 4)	Limit (Note 5)	Typical (Note 4)	Limit (Note 5)	Typical (Note 4)	Limit (Note 5)	
Z_T	Transimpedance	R_L = 1 kΩ	1.8	1.0 **0.6**	1.8	1.0 **0.6**	1.8	0.8 **0.6**	MΩ min
		R_L = 100Ω	1.4	0.8 **0.45**	1.4	0.8 **0.5**	1.4	0.7 **0.45**	
I_S	Supply Current	No Load, V_O = 0V	7.5	10 **10**	7.5	10 **10**	7.5	10 **10**	mA max
V_{CM}	Input Common Mode Voltage Range		V^+ − 1.7V V^- + 1.7V		V^+ − 1.7V V^- + 1.7V		V^+ − 1.7V V^- + 1.7V		V

AC Electrical Characteristics

The following specifications apply for **Supply Voltage** = ±**15V**, R_L = 1 kΩ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits T_J = 25°C.

Symbol	Parameter	Conditions	LM6181AM		LM6181AI		LM6181I		Units
			Typical (Note 4)	Limit (Note 5)	Typical (Note 4)	Limit (Note 5)	Typical (Note 4)	Limit (Note 5)	
BW	Closed Loop Bandwidth −3 dB	A_V = +2	100		100		100		MHz min
		A_V = +10	80		80		80		
		A_V = −1	100	80	100	80	100	80	
		A_V = −10	60		60		60		
PBW	Power Bandwidth	A_V = −1, V_O = 5 V_{PP}	60		60		60		
SR	Slew Rate	Overdriven	2000		2000		2000		V/μs min
		A_V = −1, V_O = ±10V (Note 6)	1400	1000	1400	1000	1400	1000	
t_s	Settling Time (0.1%)	A_V = −1, V_O = ±5V R_L = 150Ω	50		50		50		ns
t_r, t_f	Rise and Fall Time	V_O = 1 V_{PP}	5		5		5		
t_p	Propagation Delay Time	V_O = 1 V_{PP}	6		6		6		
$i_{n(+)}$	Non-Inverting Input Noise Current Density	f = 1 kHz	3		3		3		pA/√Hz
$i_{n(-)}$	Inverting Input Noise Current Density	f = 1 kHz	16		16		16		pA/√Hz
e_n	Input Noise Voltage Density	f = 1 kHz	4		4		4		nV/√Hz
	Second Harmonic Distortion	2 V_{PP}, 10 MHz	−50		−50		−50		dBc
	Third Harmonic Distortion	2 V_{PP}, 10 MHz	−55		−55		−50		
	Differential Gain	R_L = 150Ω A_V = +2 NTSC	0.05		0.05		0.05		%
	Differential Phase	R_L = 150Ω A_V = +2 NTSC	0.04		0.04		0.04		Deg

DC Electrical Characteristics

The following specifications apply for **Supply Voltage** = ±**5V**, and R_L = 1 kΩ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits T_J = 25°C.

Symbol	Parameter	Conditions	LM6181AM		LM6181AI		LM6181I		Units
			Typical (Note 4)	Limit (Note 5)	Typical (Note 4)	Limit (Note 5)	Typical (Note 4)	Limit (Note 5)	
V_{OS}	Input Offset Voltage		1.5	3.0 **3.0**	1.5	3.0 **3.0**	3.0	5.0 **5.0**	mV max
TC V_{OS}	Input Offset Voltage Drift		2.5		2.5		2.5		µV/°C
I_B	Inverting Input Bias Current		5.0	10 **22**	5.0	10 **22**	5.0	17.5 **27.0**	µA max
	Non-Inverting Input Bias Current		0.25	1.5 **1.5**	0.25	1.5 **1.5**	0.25	3.0 **5.0**	
TC I_B	Inverting Input Bias Current Drift		50		50		50		nA/°C
	Non-Inverting Input Bias Current Drift		3.0		3.0		3.0		
I_B PSR	Inverting Input Bias Current Power Supply Rejection	V_S = ±4.0V, ±6.0V	0.3	0.5 **0.5**	0.3	0.5 **0.5**	0.3	1.0 **1.0**	µA/V max
	Non-Inverting Input Bias Current Power Supply Rejection	V_S = ±4.0V, ±6.0V	0.05	0.5 **0.5**	0.05	0.5 **0.5**	0.05	0.5 **0.5**	
I_B CMR	Inverting Input Bias Current Common Mode Rejection	−2.5V ≤ V_{CM} ≤ +2.5V	0.3	0.5 **1.0**	0.3	0.5 **1.0**	0.3	1.0 **1.5**	
	Non-Inverting Input Bias Current Common Mode Rejection	−2.5V ≤ V_{CM} ≤ +2.5V	0.12	0.5 **1.0**	0.12	0.5 **0.5**	0.12	0.5 **0.5**	
CMRR	Common Mode Rejection Ratio	−2.5V ≤ V_{CM} ≤ +2.5V	57	50 **47**	57	50 **47**	57	50 **47**	dB min
PSRR	Power Supply Rejection Ratio	V_S = ±4.0V, ±6.0V	80	70 **70**	80	70 **70**	80	64 **64**	
R_O	Output Resistance	A_V = −1, f = 300 kHz	0.25		0.25		0.25		Ω
R_{IN}	Non-Inverting Input Resistance		8	5 **2.5**	8	5 **2.5**	8	2.5 **2.0**	MΩ min
V_O	Output Voltage Swing	R_L = 1 kΩ	2.6	2.25 **2.2**	2.6	2.25 **2.25**	2.6	2.25 **2.25**	V min
		R_L = 100Ω	2.2	2.0 **2.0**	2.2	2.0 **2.0**	2.2	2.0 **2.0**	
I_{SC}	Output Short Circuit Current		100	75 **70**	100	75 **70**	100	75 **70**	mA min
Z_T	Transimpedance	R_L = 1 kΩ	1.4	0.75 **0.5**	1.4	0.75 **0.5**	1.0	0.6 **0.4**	MΩ min
		R_L = 100Ω	1.0	0.5 **0.25**	1.0	0.5 **0.3**	1.0	0.4 **0.25**	
I_S	Supply Current	No Load, V_O = 0V	6.5	8.5 **8.5**	6.5	8.5 **8.5**	6.5	8.5 **8.5**	mA max
V_{CM}	Input Common Mode Voltage Range		V^+ − 1.7V V^- + 1.7V		V^+ − 1.7V V^- + 1.7V		V^+ − 1.7V V^- + 1.7V		V

AC Electrical Characteristics

The following specifications apply for **Supply Voltage** = ±**5V**, R_L = 1 kΩ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits T_J = 25°C.

Symbol	Parameter	Conditions	LM6181AM		LM6181AI		LM6181I		Units
			Typical (Note 4)	Limit (Note 5)	Typical (Note 4)	Limit (Note 5)	Typical (Note 4)	Limit (Note 5)	
BW	Closed Loop Bandwidth −3 dB	A_V = +2	50		50		50		MHZ min
		A_V = +10	40		40		40		
		A_V = −1	55	35	55	35	55	35	
		A_V = −10	35		35		35		
PBW	Power Bandwidth	A_V = −1, V_O = 4 V_{PP}	40		40		40		
SR	Slew Rate	A_V = −1, V_O = ±2V (Note 6)	500	375	500	375	500	375	V/μs min
t_s	Settling Time (0.1%)	A_V = −1, V_O = ±2V R_L = 150Ω	50		50		50		ns
t_r, t_f	Rise and Fall Time	V_O = 1 V_{PP}	8.5		8.5		8.5		
t_p	Propagation Delay Time	V_O = 1 V_{PP}	8		8		8		
$i_{n(+)}$	Non-Inverting Input Noise Current Density	f = 1 kHz	3		3		3		pA/√Hz
$i_{n(-)}$	Inverting Input Noise Current Density	f = 1 kHz	16		16		16		pA/√Hz
e_n	Input Noise Voltage Density	f = 1 kHz	4		4		4		nV/√Hz
	Second Harmonic Distortion	2 V_{PP}, 10 MHz	−45		−45		−45		dBc
	Third Harmonic Distortion	2 V_{PP}, 10 MHz	−55		−55		−55		
	Differential Gain	R_L = 150Ω A_V = +2 NTSC	0.063		0.063		0.063		%
	Differential Phase	R_L = 150Ω A_V = +2 NTSC	0.16		0.16		0.16		Deg

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions the device is intended to be functional, but device parameter specifications may not be guaranteed under these conditions. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: Human body model 100 pF and 1.5 kΩ.

Note 3: The typical junction-to-ambient thermal resistance of the molded plastic DIP(N) package soldered directly into a PC board is 102°C/W. The junction-to-ambient thermal resistance of the S.O. surface mount (M) package mounted flush to the PC board is 70°C/W when pins 1, 4, 8, 9 and 16 are soldered to a total 2 in^2 1 oz. copper trace.

Note 4: Typical values represent the most likely parametric norm.

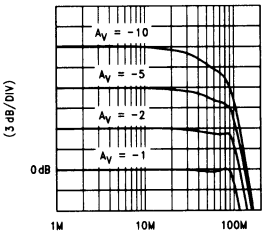
Note 5: All limits guaranteed at room temperature (standard type face) or at operating temperature extremes (**bold face type**).

Note 6: Measured from +25% to +75% of output waveform.

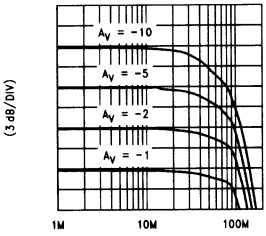
Note 7: Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±130 mA over a long term basis may adversely affect reliability.

Typical Performance Characteristics T_A = 25°C unless otherwise noted

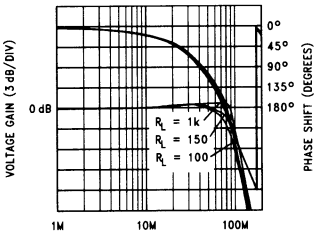
CLOSED-LOOP FREQUENCY RESPONSE
V_S = ±15V; R_f = 820Ω; R_L = 1 kΩ



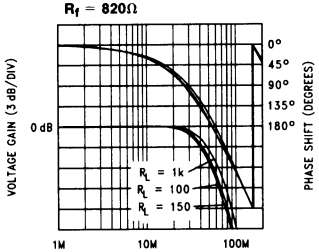
CLOSED-LOOP FREQUENCY RESPONSE
V_S = ±15V; R_f = 820Ω; R_L = 150Ω



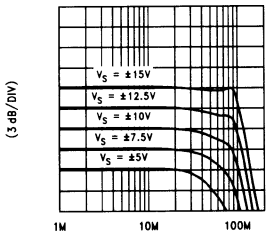
UNITY GAIN FREQUENCY RESPONSE
V_S = ±15V; A_V = +1; R_f = 820Ω



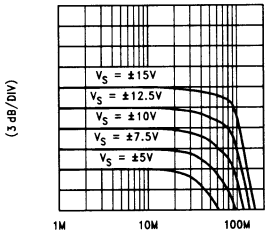
UNIT GAIN FREQUENCY RESPONSE
V_S = ±5V; A_V = +1; R_f = 820Ω



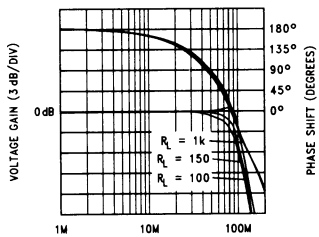
FREQUENCY RESPONSE vs SUPPLY VOLTAGE
A_V = −1; R_f = 820Ω; R_L = 1 kΩ



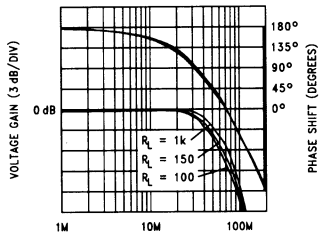
FREQUENCY RESPONSE vs SUPPLY VOLTAGE
A_V = −1; R_f = 820Ω; R_L = 150Ω



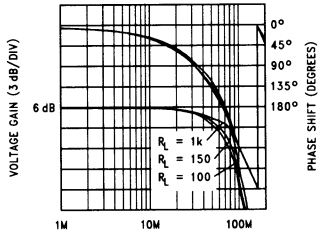
INVERTING GAIN FREQUENCY RESPONSE
V_S = ±15V; A_V = −1; R_f = 820Ω



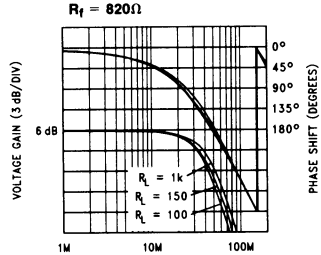
INVERTING GAIN FREQUENCY RESPONSE
V_S = ±5V; A_V = −1; R_f = 820Ω



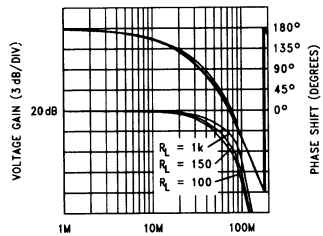
NON-INVERTING GAIN FREQUENCY RESPONSE
V_S = ±15V; A_V = +2; R_f = 820Ω



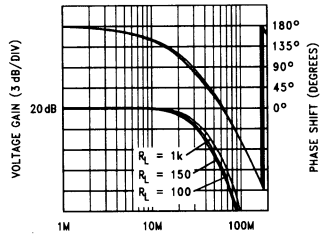
NON-INVERTING GAIN FREQUENCY RESPONSE
V_S = ±5V; A_V = +2; R_f = 820Ω



INVERTING GAIN FREQUENCY RESPONSE
V_S = ±15V; A_V = −10; R_f = 820Ω



INVERTING GAIN FREQUENCY RESPONSE
V_S = ±5V; A_V = −10; R_f = 820Ω



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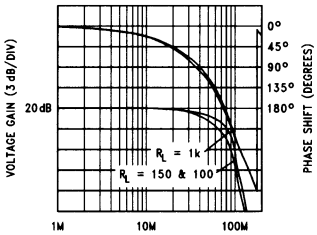
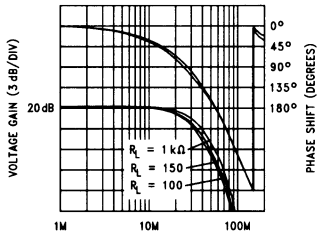
Typical Performance Characteristics $T_A = 25°C$ unless otherwise noted (Continued)

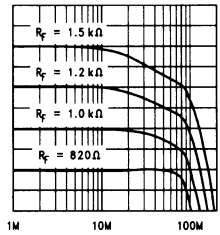
NON-INVERTING GAIN FREQUENCY RESPONSE
$V_S = \pm 15V$; $A_V = +10$;
$R_f = 820\Omega$



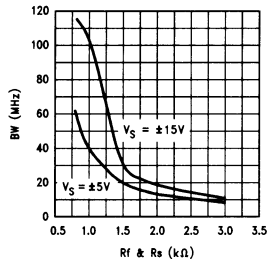
NON-INVERTING GAIN FREQUENCY RESPONSE
$V_S = \pm 5V$; $A_V = +10$;
$R_f = 820\Omega$



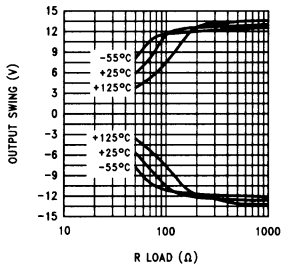
NON-INVERTING GAIN FREQUENCY COMPENSATION
$V_S = \pm 15V$; $A_V = +2$;
$R_L = 150\Omega$



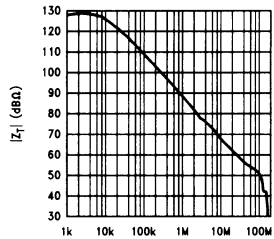
BANDWIDTH vs R_f & R_S
$A_V = -1$, $R_L = 1$ kΩ



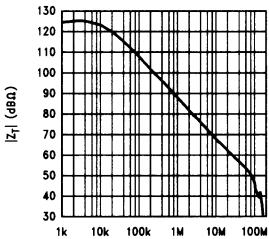
OUTPUT SWING vs R_{LOAD} PULSED, $V_S = \pm 15V$, $I_{IN} = \pm 200\ \mu A$, $V_{IN+} = 0V$



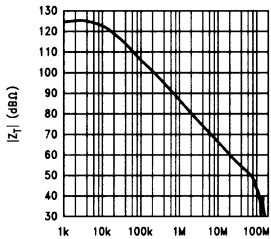
TRANSIMPEDANCE vs FREQUENCY
$V_S = \pm 15V$
$R_L = 1$ kΩ



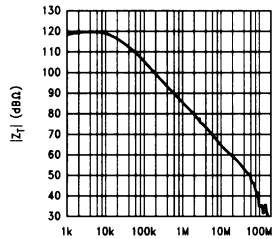
TRANSIMPEDANCE vs FREQUENCY
$V_S = \pm 15V$
$R_L = 100\Omega$



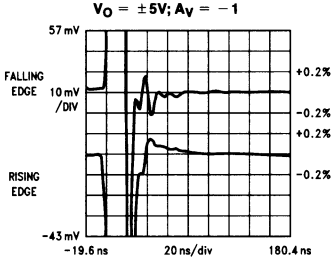
TRANSIMPEDANCE vs FREQUENCY
$V_S = \pm 5V$
$R_L = 1$ kΩ



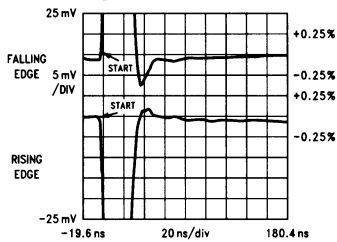
TRANSIMPEDANCE vs FREQUENCY
$V_S = \pm 5V$
$R_L = 100\Omega$



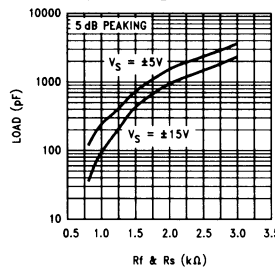
SETTLING RESPONSE
$V_S = \pm 15V$; $R_L = 150\Omega$;
$V_O = \pm 5V$; $A_V = -1$



SETTLING RESPONSE
$V_S = \pm 5V$; $R_L = 150\Omega$;
$V_O = \pm 2V$; $A_V = -1$



SUGGESTED R_f and R_S for C_L
$A_V = -1$; $R_L = 150\Omega$



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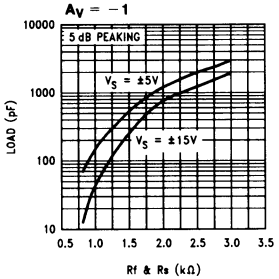
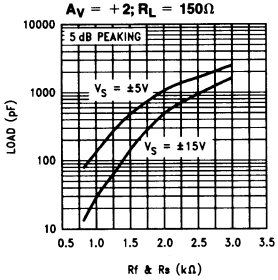
Typical Performance Characteristics T_A = 25°C unless otherwise noted (Continued)

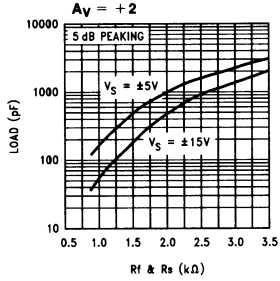
SUGGESTED R_f and R_S FOR C_L
A_V = −1



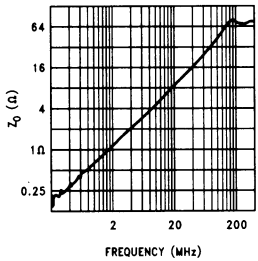
SUGGESTED R_f and R_S FOR C_L
A_V = +2; R_L = 150Ω



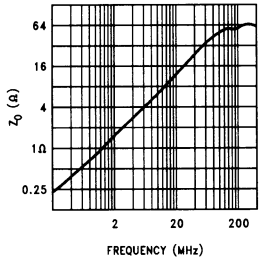
SUGGESTED R_f and R_S FOR C_L
A_V = +2



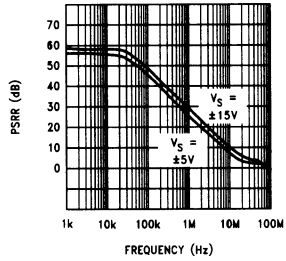
OUTPUT IMPEDANCE vs FREQ
V_S = ±15V; A_V = −1
R_f = 820Ω



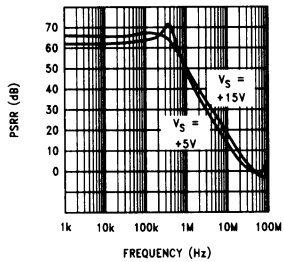
OUTPUT IMPEDANCE vs FREQ
V_S = ±5V; A_V = −1
R_f = 820Ω



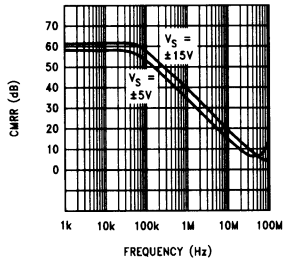
PSRR (V_S^+) vs FREQUENCY



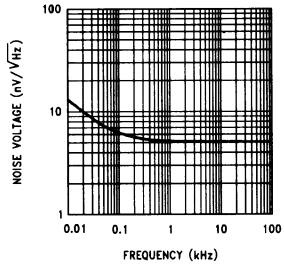
PSRR (V_S^-) vs FREQUENCY



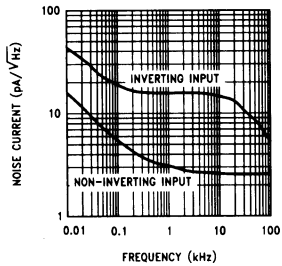
CMRR vs FREQUENCY



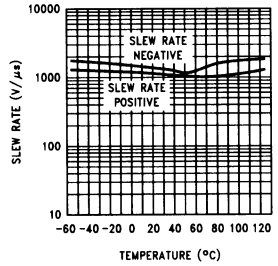
INPUT VOLTAGE NOISE vs FREQUENCY



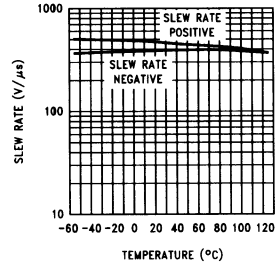
INPUT CURRENT NOISE vs FREQUENCY



SLEW RATE vs TEMPERATURE A_V = −1; R_L = 150Ω, V_S = ±15V



SLEW RATE vs TEMPERATURE A_V = −1; R_L = 150Ω, V_S = ±5V



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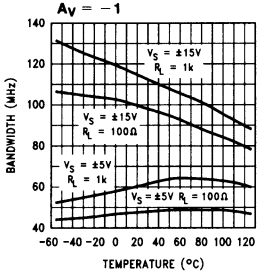
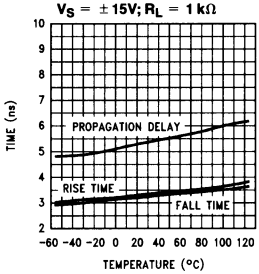
Typical Performance Characteristics T_A = 25°C unless otherwise noted (Continued)

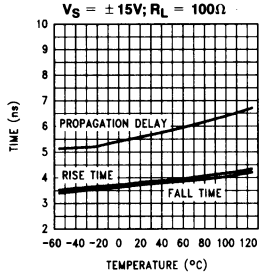
−3 dB BANDWIDTH vs TEMPERATURE
A_V = −1



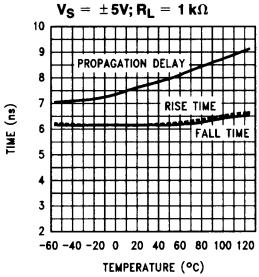
SMALL SIGNAL PULSE RESPONSE vs TEMP, A_V = +1
V_S = ±15V; R_L = 1 kΩ



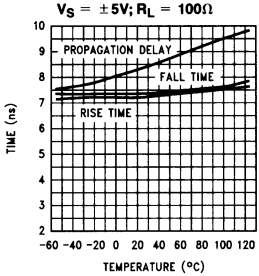
SMALL SIGNAL PULSE RESPONSE vs TEMP, A_V = +1
V_S = ±15V; R_L = 100Ω



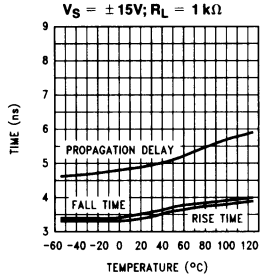
SMALL SIGNAL PULSE RESPONSE vs TEMP, A_V = +1
V_S = ±5V; R_L = 1 kΩ



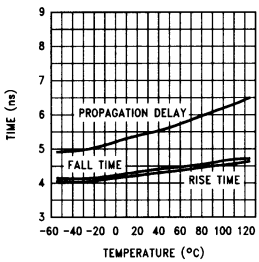
SMALL SIGNAL PULSE RESPONSE vs TEMP, A_V = +1
V_S = ±5V; R_L = 100Ω



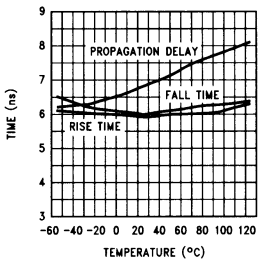
SMALL SIGNAL PULSE RESPONSE vs TEMP, A_V = −1
V_S = ±5V; R_L = 1 kΩ



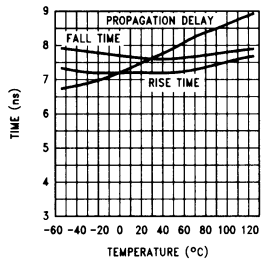
SMALL SIGNAL PULSE RESPONSE vs TEMP, A_V = −1
V_S = ±15V; R_L = 100Ω



SMALL SIGNAL PULSE RESPONSE vs TEMP, A_V = −1
V_S = ±5V; R_L = 1 kΩ



SMALL SIGNAL PULSE RESPONSE vs TEMP, A_V = −1
V_S = ±5V; R_L = 100Ω



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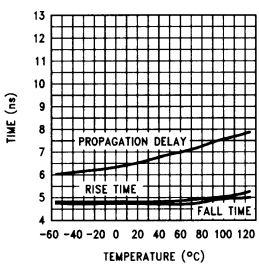
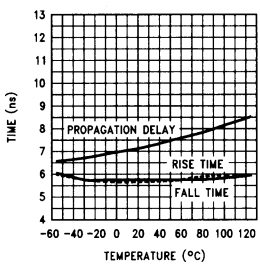
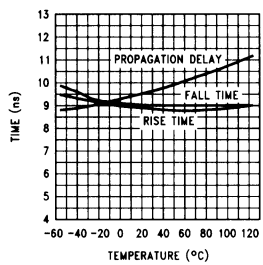
V_S = ±15V; R_L = 1 kΩ



SMALL SIGNAL PULSE RESPONSE vs TEMP, A_V = +2
V_S = ±15V; R_L = 100Ω



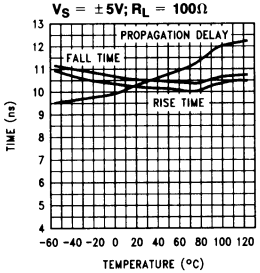
SMALL SIGNAL PULSE RESPONSE vs TEMP, A_V = +2
V_S = ±5V; R_L = 1 kΩ



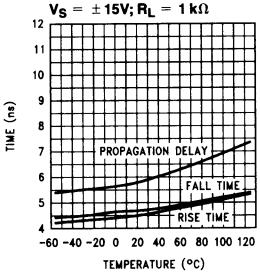
TL/H/11328–29

Typical Performance Characteristics T_A = 25°C unless otherwise noted (Continued)

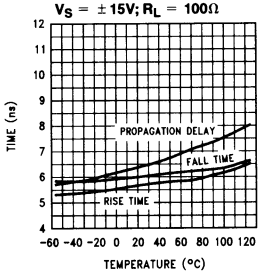
SMALL SIGNAL PULSE RESPONSE vs TEMP, A_V = +2
V_S = ±5V; R_L = 100Ω



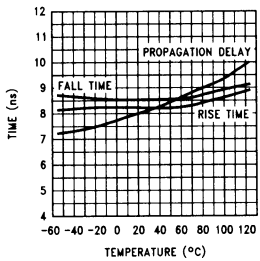
SMALL SIGNAL PULSE RESPONSE vs TEMP, A_V = −10
V_S = ±15V; R_L = 1 kΩ



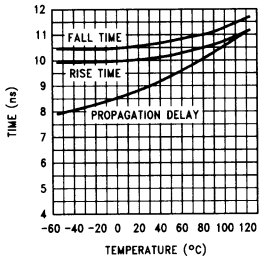
SMALL SIGNAL PULSE RESPONSE vs TEMP, A_V = −10
V_S = ±15V; R_L = 100Ω



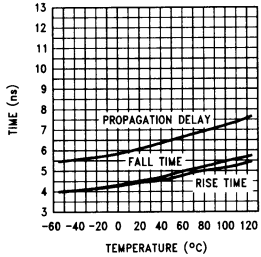
SMALL SIGNAL PULSE RESPONSE vs TEMP, A_V = −10
V_S = ±5V; R_L = 1 kΩ



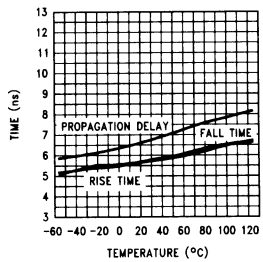
SMALL SIGNAL PULSE RESPONSE vs TEMP, A_V = −10
V_S = ±5V; R_L = 100Ω



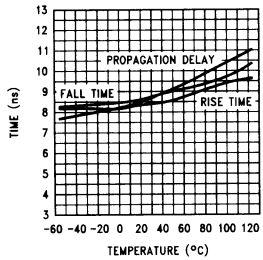
SMALL SIGNAL PULSE RESPONSE vs TEMP, A_V = +10
V_S = ±15V; R_L = 1 kΩ



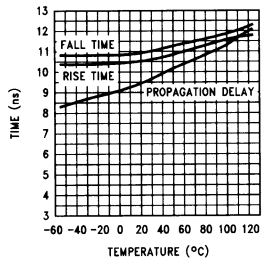
SMALL SIGNAL PULSE RESPONSE vs TEMP, A_V = +10
V_S = ±15V; R_L = 100Ω



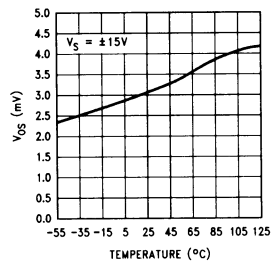
SMALL SIGNAL PULSE RESPONSE vs TEMP, A_V = +10
V_S = ±5V; R_L = 1 kΩ



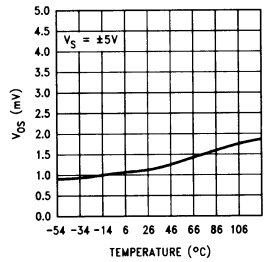
SMALL SIGNAL PULSE RESPONSE vs TEMP, A_V = +10
V_S = ±5V; R_L = 100Ω



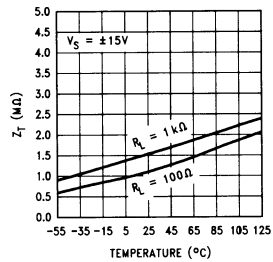
OFFSET VOLTAGE vs TEMPERATURE



OFFSET VOLTAGE vs TEMPERATURE



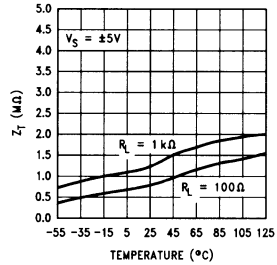
TRANSIMPEDANCE vs TEMPERATURE



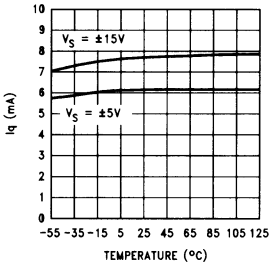
TL/H/11328–8

Typical Performance Characteristics T_A = 25°C unless otherwise noted (Continued)

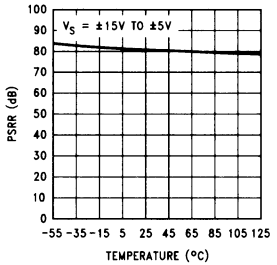
TRANSIMPEDANCE vs TEMPERATURE



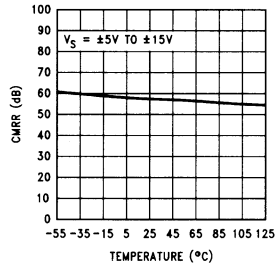
QUIESCENT CURRENT vs TEMPERATURE



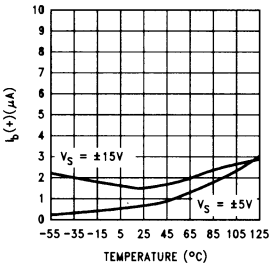
PSRR vs TEMPERATURE



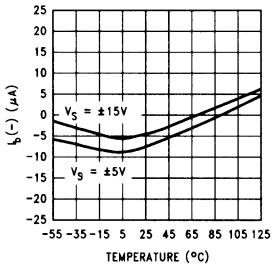
CMRR vs TEMPERATURE



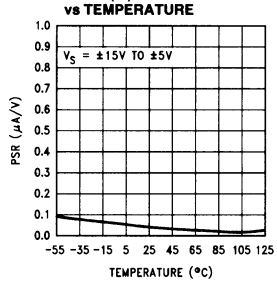
NON-INVERTING BIAS CURRENT vs TEMPERATURE



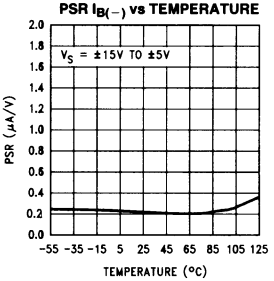
INVERTING BIAS CURRENT vs TEMPERATURE



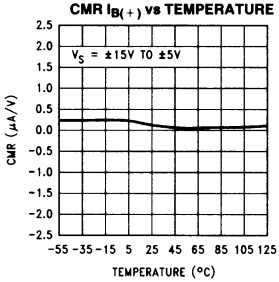
PSR $I_{B(+)}$ vs TEMPERATURE



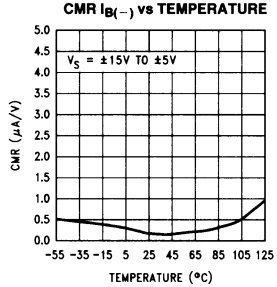
PSR $I_{B(-)}$ vs TEMPERATURE



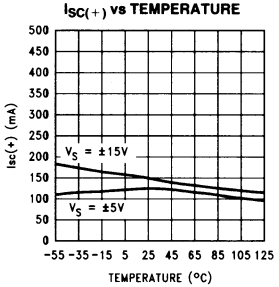
CMR $I_{B(+)}$ vs TEMPERATURE



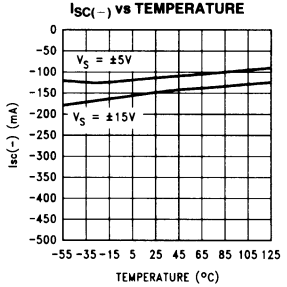
CMR $I_{B(-)}$ vs TEMPERATURE



$I_{SC(+)}$ vs TEMPERATURE



$I_{SC(-)}$ vs TEMPERATURE



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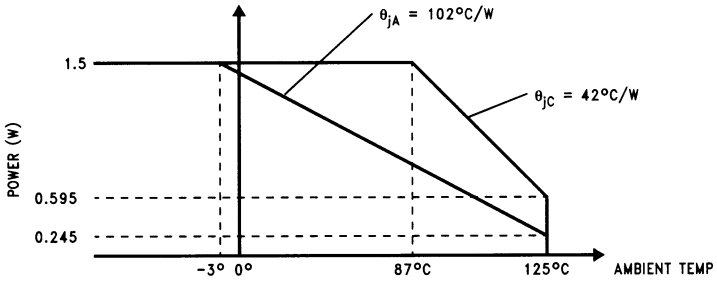
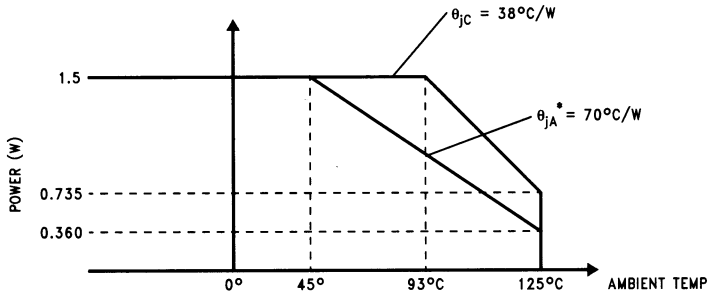
Typical Performance Characteristics

Power Derating Curves



N – PACKAGE

TL/H/11328–30



M – PACKAGE

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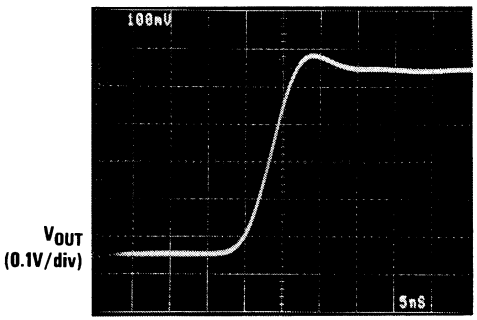
***θ_{JA} = Thermal Resistance with 2 Square Inches of 1 Ounce Copper Tied to Pins 1, 8, 9 and 16**

Typical Applications

CURRENT FEEDBACK TOPOLOGY

For a conventional voltage feedback amplifier the resulting small-signal bandwidth is inversely proportional to the desired gain to a first order approximation based on the gain-bandwidth concept. In contrast, the current feedback amplifier topology, such as the LM6181, transcends this limitation to offer a signal bandwidth that is relatively independent of the closed-loop gain. *Figures 1a* and *1b* illustrate that for closed loop gains of −1 and −5 the resulting pulse fidelity suggests quite similar bandwidths for both configurations.



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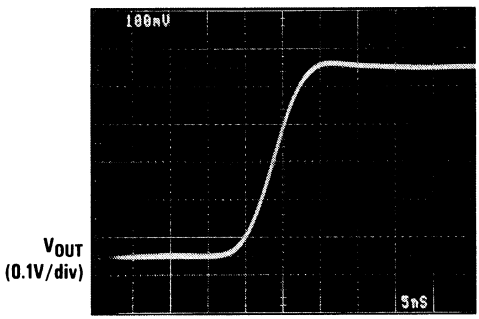
1a



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1b

FIGURES 1a, 1b: Variation of Closed Loop Gain from −1 to −5 Yields Similar Responses

The closed-loop bandwidth of the LM6181 depends on the feedback resistance, R_f. Therefore, R_S and not R_f, must be varied to adjust for the desired closed-loop gain as in *Figure 2*.

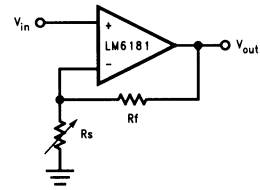

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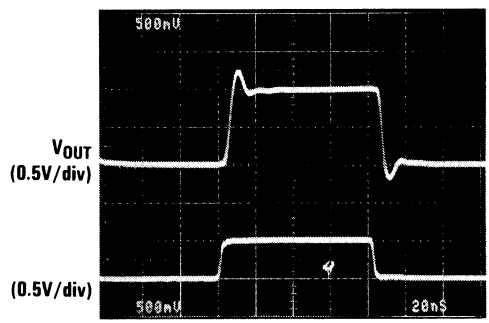
FIGURE 2. R_S Is Adjusted to Obtain the Desired Closed Loop Gain, A_{VCL}

POWER SUPPLY BYPASSING AND LAYOUT CONSIDERATIONS

A fundamental requirement for high-speed amplifier design is adequate bypassing of the power supply. It is critical to maintain a wideband low-impedance to ground at the amplifiers supply pins to insure the fidelity of high speed amplifier transient signals. 10 μF tantalum and 0.1 μF ceramic bypass capacitors are recommended for each supply pin. The bypass capacitors should be placed as close to the amplifier pins as possible (0.5″ or less).

FEEDBACK RESISTOR SELECTION: R_f

Selecting the feedback resistor, R_f, is a dominant factor in compensating the LM6181. For general applications the LM6181 will maintain specified performance with an 820Ω feedback resistor. Although this value will provide good results for most applications, it may be advantageous to adjust this value slightly. Consider, for instance, the effect on pulse responses with two different configurations where both the closed-loop gains are 2 and the feedback resistors are 820Ω, and 1640Ω, respectively. *Figures 3a* and *3b* illustrate the effect of increasing R_f while maintaining the same closed-loop gain—the amplifier bandwidth decreases. Accordingly, larger feedback resistors can be used to slow down the LM6181 (see −3 dB bandwidth vs R_f typical curves) and reduce overshoot in the time domain response. Conversely, smaller feedback resistance values than 820Ω can be used to compensate for the reduction of bandwidth at high closed loop gains, due to 2nd order effects. For example *Figure 4* illustrates reducing R_f to 500Ω to establish the desired small signal response in an amplifier configured for a closed loop gain of 25.



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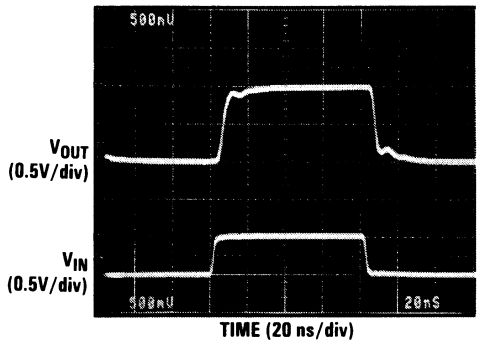
3a: R_f = 820Ω

Typical Applications (Continued)



TL/H/11328–16

3b: $R_f = 1640\Omega$

FIGURES 3a, b: Increasing Compensation with Increasing R_f

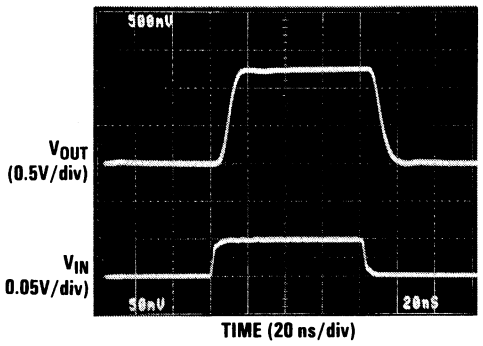


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FIGURE 4: Reducing R_f for Large Closed Loop Gains, $R_f = 500\Omega$

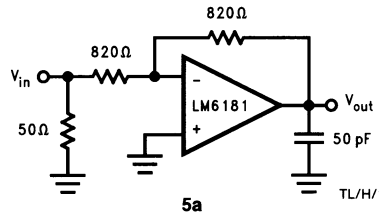
SLEW RATE CONSIDERATIONS

The slew rate characteristics of current feedback amplifiers are different than traditional voltage feedback amplifiers. In voltage feedback amplifiers slew rate limiting or non-linear amplifier behavior is dominated by the finite availability of the 1st stage tail current charging the compensation capacitor. The slew rate of current feedback amplifiers, in contrast, is not constant. Transient current at the inverting input determines slew rate for both inverting and non-inverting gains. The non-inverting configuration slew rate is also determined by input stage limitations. Accordingly, variations of slew rates occur for different circuit topologies.

DRIVING CAPACITIVE LOADS

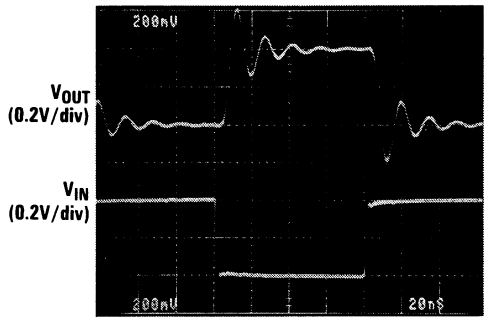
The LM6181 can drive significantly larger capacitive loads than many current feedback amplifiers. Although the LM6181 can directly drive as much as 100 pF without oscillating, the resulting response will be a function of the feedback resistor value. *Figure 5* illustrates the small-signal pulse response of the LM6181 while driving a 50 pF load. Ringing persists for approximately 70 ns. To achieve pulse responses with less ringing either the feedback resistor can be increased (see typical curves Suggested R_f and R_S for C_L), or resistive isolation can be used (10Ω–51Ω typically works well). Either technique, however, results in lowering the system bandwidth.

Figure 6 illustrates the improvement obtained with using a 47Ω isolation resistor.



5a

TL/H/11328–18



5b

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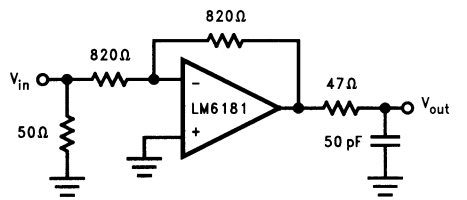
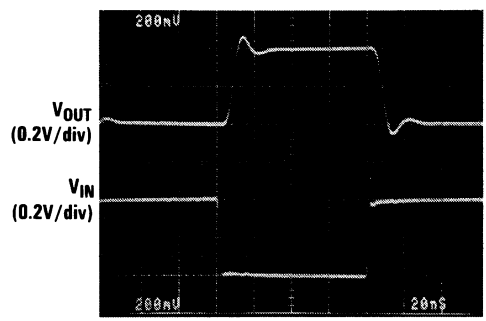
FIGURES 5a, b: $A_V = -1$, LM6181 Can Directly Drive 50 pF of Load Capacitance with 70 ns of Ringing Resulting in Pulse Response



6a

TL/H/11328–20



6b

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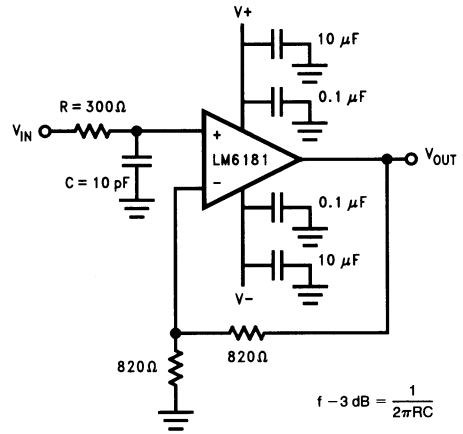
FIGURES 6a, b: Resistive Isolation of C_L Provides Higher Fidelity Pulse Response. R_f and R_S Could Be Increased to Maintain $A_V = -1$ and Improve Pulse Response Characteristics.

Typical Applications (Continued)

CAPACITIVE FEEDBACK

For voltage feedback amplifiers it is quite common to place a small lead compensation capacitor in parallel with feedback resistance, R_f. This compensation serves to reduce the amplifier's peaking in the frequency domain which equivalently tames the transient response. To limit the bandwidth of current feedback amplifiers, do not use a capacitor across R_f. The dynamic impedance of capacitors in the feedback loop reduces the amplifier's stability. Instead, reduced peaking in the frequency response, and bandwidth limiting can be accomplished by adding an RC circuit, as illustrated in *Figure 7b.*



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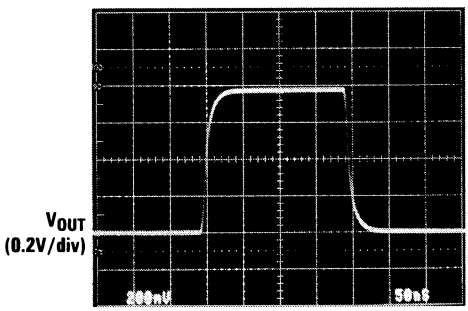
7a



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7b

FIGURES 7a, b: RC Limits Amplifier Bandwidth to 50 MHz, Eliminating Peaking in the Resulting Pulse Response

Typical Performance Characteristics

OVERDRIVE RECOVERY

When the output or input voltage range of a high speed amplifier is exceeded, the amplifier must recover from an overdrive condition. The typical recovery times for open-loop, closed-loop, and input common-mode voltage range are illustrated in *Figures 9, 11* and *12,* respectively.

The open-loop circuit of *Figure 8* generates an overdrive response by allowing the ±0.5V input to exceed the linear input range of the amplifier. Typical positive and negative overdrive recovery times shown in *Figure 9* are 5 ns and 25 ns, respectively.

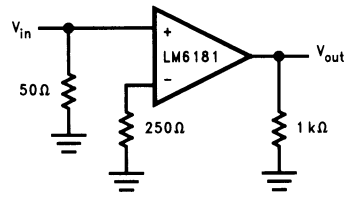

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FIGURE 8

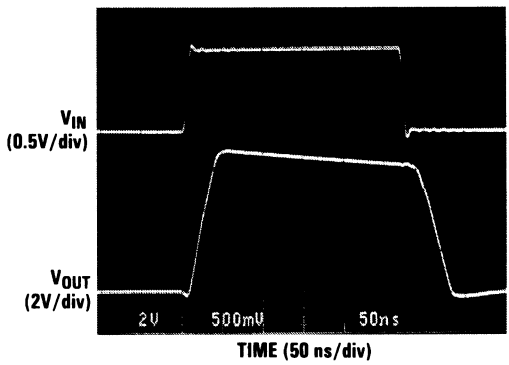

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FIGURE 9. Open-Loop Overdrive Recovery Time of 5 ns, and 25 ns from Test Circuit in *Figure 8*

Typical Performance Characteristics (Continued)

The large closed-loop gain configuration in *Figure 10* forces the amplifier output into overdrive. *Figure 11* displays the typical 30 ns recovery time to a linear output value.

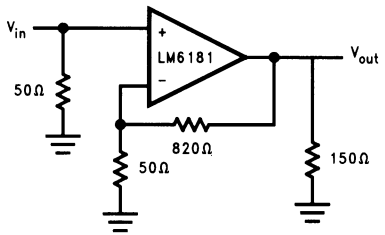

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FIGURE 10

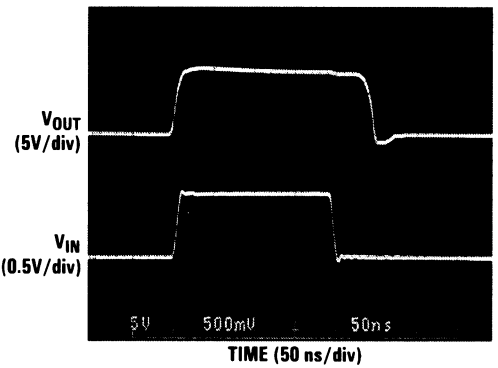

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FIGURE 11. Closed-Loop Overdrive Recovery Time of 30 ns from Exceeding Output Voltage Range from Circuit in *Figure 10*

The common-mode input of the circuit in *Figure 10* is exceeded by a 5V pulse resulting in a typical recovery time of 310 ns shown in *Figure 12*. The LM6181 supply voltage is ±5V.

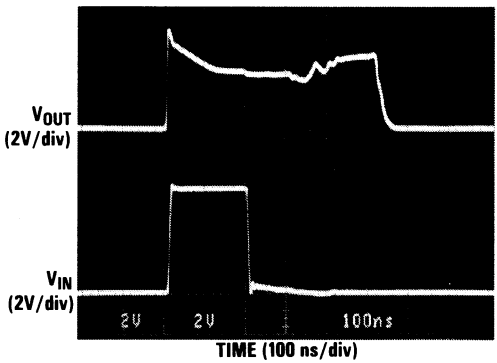

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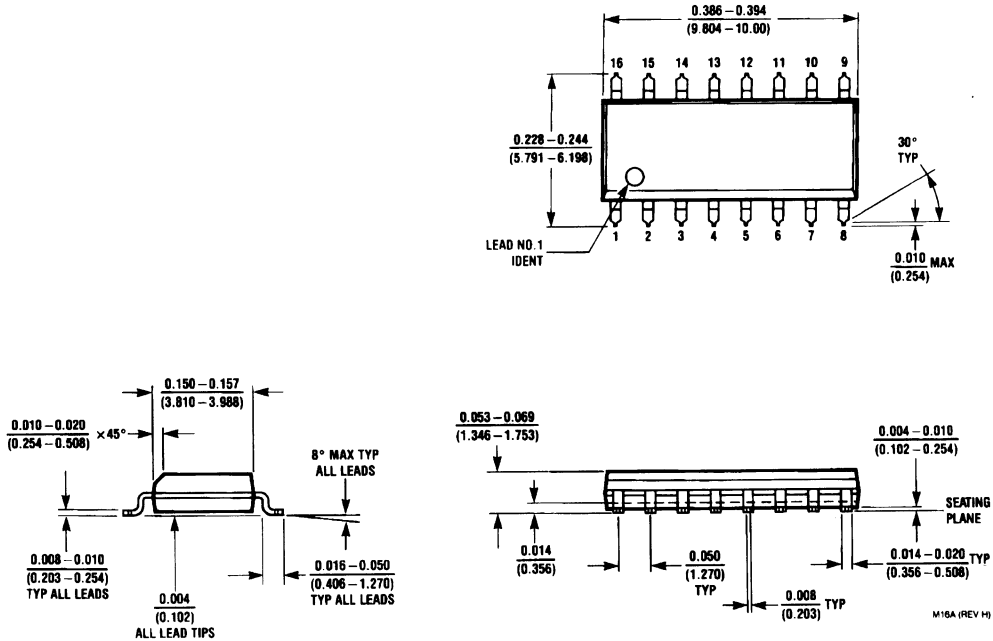
FIGURE 12. Exceptional Output Recovery from an Input that Exceeds the Common-Mode Range

Ordering Information

Package	Temperature Range		NSC Drawing
	Military −55°C to +125°C	Industrial −40°C to +85°C	
8-Pin Molded DIP	LM6181AMN	LM6181AIN LM6181IN	N08E
16-Pin Small Outline		LM6181AIM LM6181IM	M16A

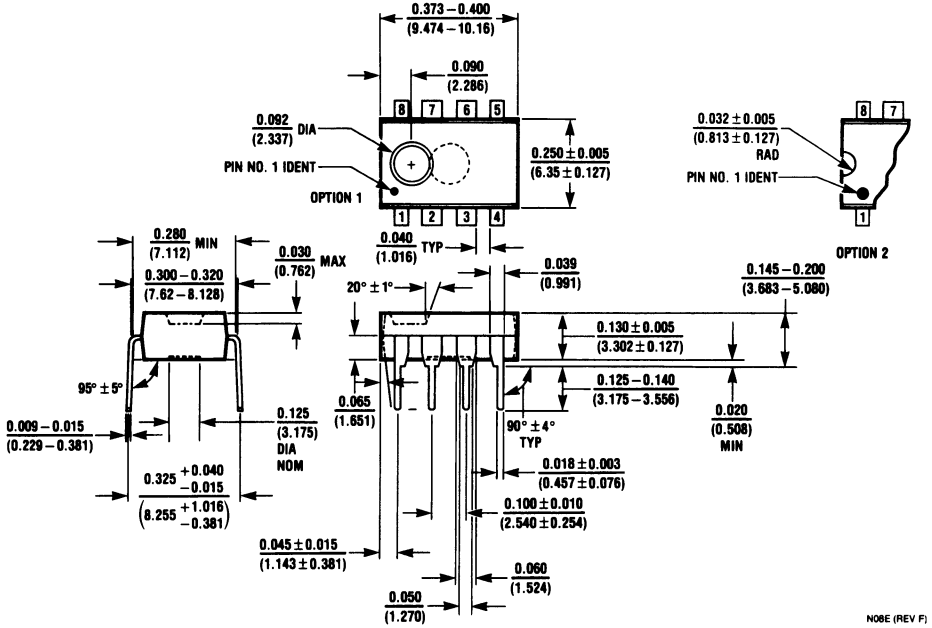
If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office or Distributors for availability and specifications.

Physical Dimensions inches (millimeters)



Small Outline Package (M)
Order Number LM6181IM or LM6181AIM
NS Package Number M16A

Physical Dimensions inches (millimeters) (Continued)



Dual-In-Line-Package (N)
Order Number LM6181AIN, LM6181IN or LM6181AMN
NS Package Number N08E

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110 MHz CRT Video Amplifier Fulfills Demands of High Resolution Monitors

National Semiconductor
Application Note 598
Zahid Rahim
April 1989

Over the years there has been a continuing trend toward high resolution monitors. Such monitors have finally made possible PC based desk top publishing (DTP) which allows the user to merge text and graphics and produce documents that rival typeset documents from publishing houses. In addition, high resolution monitors have also made possible high end work stations for sophisticated CAD/CAM applications and 3D modeling. At the low end of the spectrum there is IBM's CGA color display monitor with 320 x 200 pixel resolution. However, at the other end of the spectrum, there is the Hitachi color monitor that boasts 2048 x 2048 pixel resolution; allowing the user to produce photo quality graphics.

A simplified block diagram of a typical color monitor is shown in *Figure 1*. In most cases, a properly terminated transmission line or a coaxial cable carries the video signal from the host computer to the monitor. The video signal is usually 1 V_{pp} and thus requires amplification before the signal can be applied to the cathode. The amplification of the video signal is usually done in two stages. A low voltage amplifier, often called a pre-amplifier, amplifies the 1 V_{pp} signal to a 4–6 V_{pp} signal. In addition to amplification, a pre-amplifier may also provide contrast and brightness control. Note that contrast control allows the user to vary the gain of the video signal and thereby vary the sharpness of the image. Meanwhile, brightness control allows the user to change the brightness of the image by varying the DC offset of the video signal. Keep in mind that in color monitors; a single contrast control knob varies the contrast level for all three guns simultaneously. Also, a single brightness control knob varies the brightness level for all three guns simultaneously. Most pre-amplifiers also provide DC restoration or black level clamping for the video signal, as described in Section 8.

As shown in *Figure 1*, the green channel usually carries a composite video signal. The composite video signal not only contains gray scale information (i.e., the video signal amplitude) but also the timing information required for horizontal and vertical synchronization. The sync separator separates the horizontal and vertical sync signals from the composite

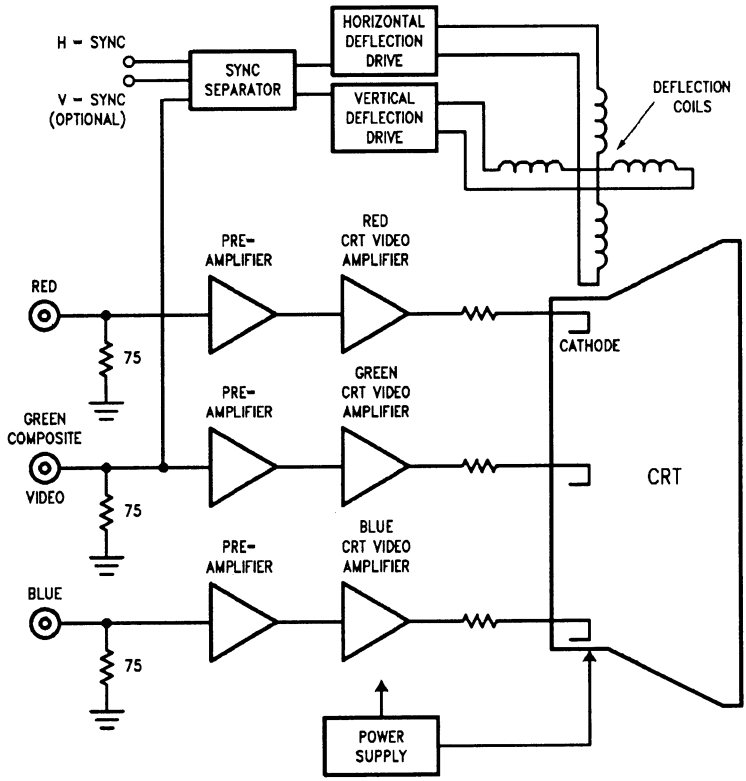

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FIGURE 1. Simplified RGB Monitor Block Diagram

signal. The horizontal and vertical deflection circuits in turn drive their respective deflection coils with linear sawtooth current waveforms (current ramps). The current ramps produce magnetic fields whose strength is proportional to the amount of current passing through the coils. These magnetic fields in turn deviate the electron beam thus accomplishing the task of horizontal and vertical scanning.

The CRT video amplifier is the second stage of amplification, it amplifies the 4–6 V_{pp} video signal to a 40–60 V_{pp} signal that the cathode requires to energize each phosphor dot (also called pixel) on the screen. Thus, by modulating the voltage of each of the three cathodes, the corresponding pixel is energized at varying intensities, thereby producing various shades of color. To change a pixel from black to peak white, the CRT video amplifier may be required to swing as much as 40 V_{pp}, and all this in as short a duration as possible. One of the major limitations in building high resolution monitors is the difficulty in designing high voltage and wide bandwidth CRT video amplifiers. At bandwidths exceeding 80 MHz, discrete designs become impractical because of the stray capacitance on the PC board. Moreover, the performance requirements of the transistors are by no means trivial. On the one hand the transistors should have breakdown voltages of 70V to 100V depending on the application, while on the other hand the transistors should maintain f_ts of 1 GHz to 2 GHz at 100 mA or more collector current.

Table I illustrates the key requirements for various pixel display resolution currently available in the market. Note that the maximum pixel time is derived assuming 60 Hz refresh rate and retrace time equivalent to 30% of each frame time. Also, as a rule of thumb, 33% of the pixel time is generally allocated to the rise/fall time of the signal at the CRT cathode. For ease of analysis we may assume that the CRT video amplifier is linear and has a single pole roll off thus allowing us to approximate the bandwidth as $f_{-3\ dB} = (0.35)/t_r$, where t_r is the signal rise time. The LH2422, a hybrid CRT video amplifier, is specifically designed to fulfill the needs of high resolution monitors and is the subject of this paper. LH2422's rise and fall times of 3.3 ns and 110 MHz bandwidth at 40 V_{pp} output makes it ideal for use in 1024 x 1024 pixel display monitors that require each pixel to be energized in 12 ns.

1.0 LH2422 CRT VIDEO AMPLIFIER—THEORY OF OPERATION

The LH2422 is essentially a transimpedance amplifier with an internal 3k feedback resistor as shown in the block diagram of *Figure 2*. Since the device is powered by a single power supply, some form of biasing is required to bias the output half way between the power supply so that symmetrical output swing can be achieved. This is accomplished by a supply dependent bias voltage V_B, and a 165Ω resistor R_B connected between the inverting input and ground. In the absence of any external input signal, the quiescent output DC voltage can be predicted from the following equation:

$$V_{OUT}(DC) = (1 + R_F/R_B) \times V_B \qquad (1)$$

At 60V power supply, V_B is approximately 1.55V, thus from equation (1), $V_{OUT}(DC) \cong 30V$. Note that any current injected at the summing node (inverting input) flows entirely through the feedback resistor because the current through R_B remains unchanged due to the voltage V_B impressed across it. Thus, ±6.67 mA current at the summing node causes the output to swing ±20V from its quiescent output DC voltage.

Voltage to voltage gain is easily accomplished by inserting a gain setting resistor, R_G, in series with the input signal (V_{IN}) and the summing node of LH2422. Keep in mind that for proper operation, V_{IN} should be centered on a DC voltage equal to LH2422's internal bias voltage, V_B, at the summing node. Thus, at DC there is no current flowing through R_G, consequently LH2422's output is biased at half the supply voltage ($V_+/2$ volts). The ac gain of the properly biased input signal can be predicted from the following equation:

$$A_V = -(R_F/R_G) \qquad (2)$$

TABLE I

Display Resolution	Maximum Pixel Time	Minimum Video Update Rate	Minimum Dot Clock Rate	Required Rise Time at CRT Cathode	Required Bandwidth ($f_{-3\ dB}$) of CRT Video Amplifier
320 x 200	200 ns	5 MHz	2.5 MHz	66 ns	5 MHz
640 x 350	57 ns	18 MHz	9 MHz	19 ns	18 MHz
640 x 480	42 ns	25 MHz	12.5 MHz	14 ns	25 MHz
800 x 560	29 ns	35 MHz	17.5 MHz	9.6 ns	36 MHz
1024 x 900	14 ns	72 MHz	36 MHz	4.6 ns	76 MHz
1024 x 1024	12 ns	82 MHz	41 MHz	4 ns	86 MHz
1280 x 1024	9.8 ns	102 MHz	51 MHz	3.2 ns	110 MHz
1664 x 1200	6.4 ns	156 MHz	78 MHz	2.1 ns	166 MHz
2048 x 2048	3.0 ns	330 MHz	165 MHz	1 ns	350 MHz

Note: This table assumes 60 Hz refresh rate and retrace time equivalent to 30% of each frame time.

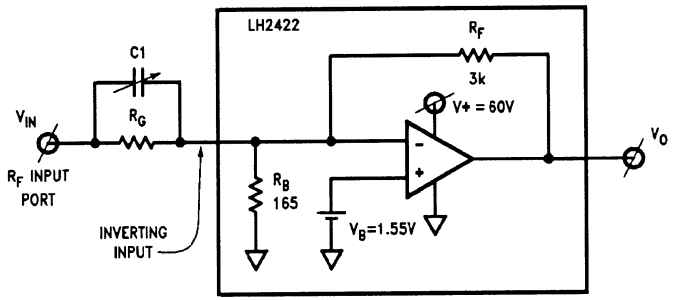

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FIGURE 2. Block Diagram shows LH2422 as a transimpedance amplifier with 3k internal feedback resistor. An external gain setting resistor (R_G) accomplishes the task of voltage to voltage gain.

An equation that combines both the ac and DC components of the output signal is as follows:

$$V_O = V_B(1 + R_F/R_B + R_F/R_G) - V_{IN}(R_F/R_G) \quad (3)$$

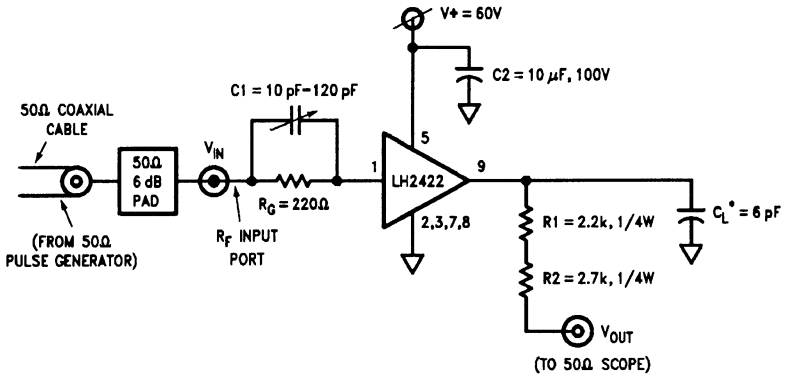
Equation (3) thus allows us to predict the output voltage for any given input voltage. It should be noted that in practice, the output voltage may differ from that predicted by equation (3) because of the tolerance of R_F and V_B, caused by process variation. However, very accurate predictions can be made by measuring V_B and by applying equation (3).

2.0 PEAKING CAPACITOR IMPROVES PULSE RESPONSE

For high resolution monitors, a video signal having a fast rise and fall time is crucial. There is a finite pixel time available for a gun to excite each pixel, thus if the video signal's rise and fall times are too long then the pixel will be energized to the peak voltage for a shorter duration than a signal with faster rise and fall time. As an example, if the video signal's rise and fall times are too slow then vertical lines of alternate black and white stripes (which would require full scale transition between adjacent pixels) would appear dimmer in comparison with horizontal lines. As a rule of thumb, the video signal's rise and fall times should be no more than 33% of the pixel time. With this is mind, a peaking capacitor can significantly improve the pulse response of LH2422. The capacitor, C1, is usually a variable capacitor and is connected across the gain setting resistor, R_G, as shown in *Figure 2*. When driven from a 50Ω source, C1 forms an RC peaking network. At high frequency, C1 bypasses R_G and significantly increases the amplifier's closed loop gain thus causing high frequency peaking. By varying C1, LH2422's pulse response can be optimized for fast rise/fall time and low overshoot.

The test circuit of *Figure 3* shows a typical setup for measuring rise/fall time and frequency response. A fast 50Ω pulse generator (HP 8082A) is used to drive the LH2422 with pulses having rise/fall time of 1 ns or less. Since a 50Ω coaxial cable connects the pulse generator to the amplifier, a 50Ω 6 dB pad is used to terminate the cable at the amplifier's input. Terminating the cable with it's characteristic impedance minimizes ringing of the input signal due to reflection. To observe the high voltage output of the amplifier, some form of attenuation of the signal is required so as not to overdrive the oscilloscope's internal amplifier. R1 and R2 together with the scope's 50Ω input impedance provide a 100:1 attenuation of the amplifier's output signal. Two series resistors, R1 and R2, are used as opposed to a single 4.95k resistor so as to reduce the effective shunt capacitance across the resistor. Note that care should be taken so that there is minimal stray capacitance at the junction of R1 and R2. Alternately, a 100:1 passive probe or a FET probe may be used. For proper measurements, the DC offset of the pulse from the pulse generator is adjusted so that the amplifier's output signal is centered at 30V. With a 220Ω resistor, ac gain of approximately 13.6 is realized as per equation (2). Thus, a 3 V_{pp} signal at the R_F input port produces a 40 V_{pp} signal at the amplifier's output. Peaking capacitor C1 is adjusted until an optimum pulse response with fast rise/fall time and low overshoot is observed on the scope. A 50Ω 1 GHz bandwidth plug in (Tektronix 7A29) was used to measure rise and fall times.

The scope photographs of *Figures 4(a)* and *4(b)* show the rise and fall time response of the LH2422's 40 V_{pp} output signal. Note that the pulse generator's rise (fall) time as observed on the scope must be subtracted from the output signal's observed fall (rise) time. As can be seen from the scope photographs, rise and fall times of 3.3 ns and 3.1 ns respectively can be easily achieved. The amplifier's excellent response to 40 V_{pp} output signal at 10 MHz and 50 MHz (10 ns pixel) are shown by the scope photographs of *Figures 4(c)* and *4(d)*.



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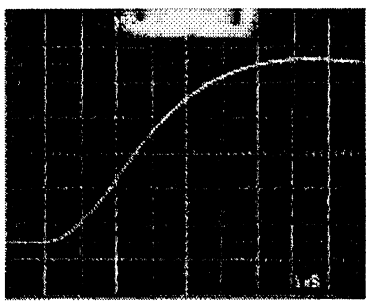
*Note: C_L includes the load capacitance as well as the stray capacitance of the test jig.

FIGURE 3. ac Test Circuit for Measuring Rise/Fall Time and Frequency Response



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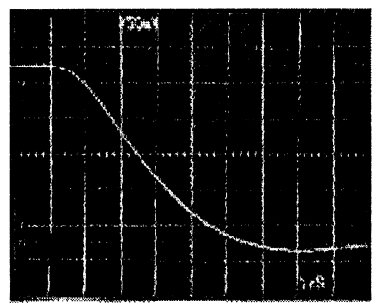
(a)

$t_r = \sqrt{(3.6)^2 - (1.4)^2} = 3.3$ ns



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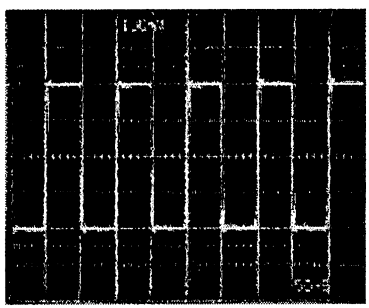
(b)

$t_f = \sqrt{(3.4^2 - (1.4)^2} = 3.1$ ns



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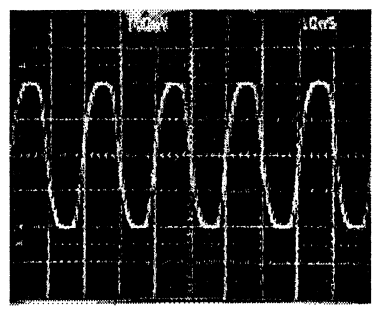
(c)



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(d)

FIGURE 4. Scope photographs show typical rise and fall times of 3.3 ns (a) and 3.1 ns (b) respectively. The output signal's peaks remain relatively flat at 10 MHz (c) and 50 MHz (d).

An HP network analyzer was used with the AC test circuit of *Figure 3* to measure the amplifier's frequency response (note that the signal was ac coupled to the amplifier's R_F input). *Figure 5(a)* shows the effect of gain peaking caused by the peaking capacitor, moreover, the bandwidth ($f_{-3\ dB}$) is measured at over 120 MHz for a 40 V_{pp} output signal. An important feature to keep in mind is that for lower output signals, the amplifier's bandwidth increases along with a corresponding decrease in rise and fall times. As can be evidenced from *Figure 5(b)*, the same device shows a 145 MHz bandwidth at 20 V_{pp} output. It should be kept in mind that although faster and higher resolution monitors

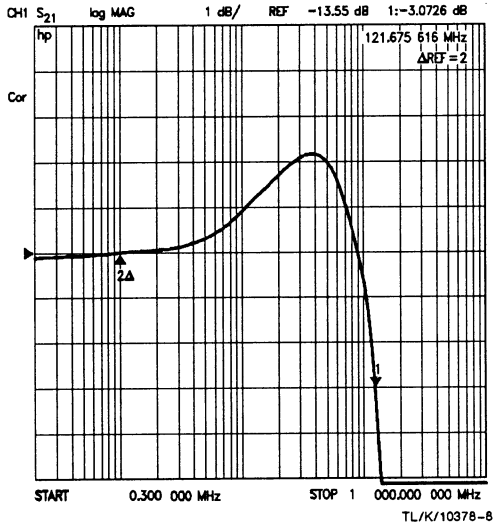

FIGURE 5(a). At 40 V_{pp} output, the amplifier's 3 dB bandwidth is better than 120 MHz. The hump in the frequency response is caused by the peaking capacitor.

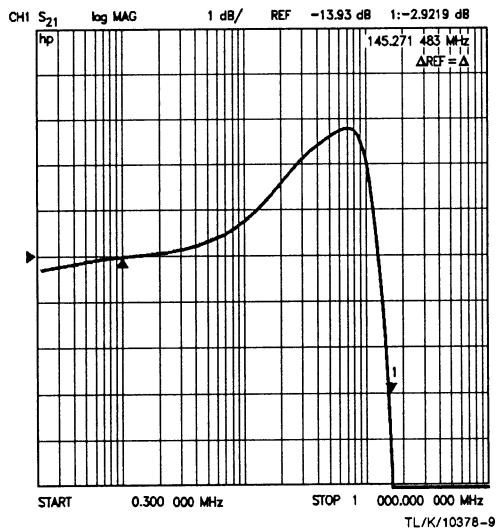

FIGURE 5(b). Decreasing the Amplifier's Output Swing to 20 V_{pp} Increases the 3 dB Bandwidth to 145 MHz

can be designed by limiting the amplifier's output swing, the image would not be as sharp or bright because of less energy available to energize each pixel.

3.0 IMPROVING SETTLING TIME FOR HIGH BIT RESOLUTION MONITORS

So far we have only discussed display resolution which in effect determines the maximum number of pixels that can be displayed. When viewing arcs or curved images, the display resolution of the monitor becomes particularly evident, a low resolution monitor would show jagged edges as opposed to smooth and sharply defined edges for a high resolution monitor. A monitor's bit resolution on the other hand is an indication of the number of colors that can be displayed. An analog monitor for instance accepts analog signals from a video D/A converter (DAC) located in the host computer.

For example, if 4-bit video DACs are used for each of the three guns in the color monitor then each gun must be able to resolve 16 (i.e., 2^4) levels of the video signal's gray scale. In this case the total bit resolution of the monitor is 12 (i.e., 4 x 3) because each color word would consist of 4 bits each of blue, red and green information. The total number of available colors, also known as the color palette would then be 4096 (i.e., 2^{4x3}). Since each gun must resolve the video signal's gray scale to any one of 16 levels, settling time specification becomes very important. The CRT video amplifier is thus required to settle within a specified error band, usually $\pm\frac{1}{2}$ LSB. Note that as bit resolution increases, the amplifier's output is required to settle within a smaller and smaller error band. For instance, a triple 8-bit monitor would require the video amplifier's output to settle within $\pm 0.2\%$ of the final value as opposed to $\pm 3\%$ for a triple 4-bit monitor. Clearly, it becomes evident that for higher bit resolution the video amplifier's settling time would increase. Consequently at high bit resolutions, the pixel display resolution decreases so that the pixel time is long enough to accommodate the increased settling time of the video amplifier.

Significant settling time improvement of LH2422's output signal can be made by making a simple modification to the amplifier's peaking network. Note that although the peaking capacitor improves the rise/fall time of LH2422, the capacitor also introduces overshoot. Excessive overshoot and ringing of the output signal results in a longer time for the output to settle within the specified error band. Including a resistor R1 in series with the peaking capacitor C1 (as in *Figure 6*) can improve settling time by reducing overshoot, but, the rise and fall times increase. We can however achieve optimum settling time at the expense of increased rise/fall times by taking advantage of this tradeoff, as illustrated by curves A and B in *Figure 6*. Table II clearly illustrates the effect of R1 on settling time and rise/fall time of a typical device. The settling time t_{sr} is measured from 10% of the output signal's rising edge to the point where the output settles to within a specified error band. Meanwhile, t_{sf} is the settling time measured for 90% of the output signal's falling edge to the point where the output settles to within a specified error band. From Table II, the worst case settling time to within $\pm 5\%$ of the final value is 7.1 ns while the worst case rise/fall time is 3.2 ns at R1 = 0Ω. Increasing R1 to 15Ω causes a significant drop in the settling time to 3.8 ns due to reduced overshoot, but, the rise/fall time increases to 3.4 ns. A further increase in R1 to 24Ω however increases the settling time to 4.2 ns due to the increased rise/fall time of 3.6 ns. Thus, as shown in Table II, R1 = 15Ω provides an optimum pulse response by achieving the desired

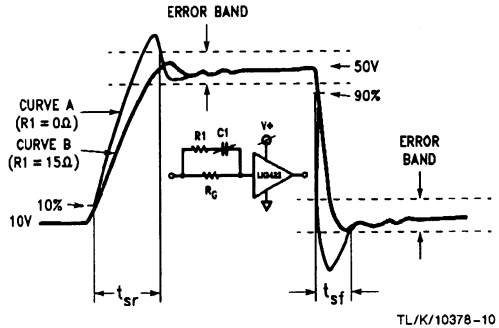

FIGURE 6. Including the Right Value of Resistor in Series with the Peaking Capacitor Can Significantly Reduce Settling Time by Reducing the Overshoot as Shown by Curves A and B

TABLE II. Settling Time Characteristics for Output Settling to within ±5% of Final Value*

R1	t_{sr}	t_r	t_{sf}	t_f
0Ω	7.1 ns	3.2 ns	6.7 ns	3.0 ns
15Ω	3.8 ns	3.4 ns	3.8 ns	3.3 ns
24Ω	4.2 ns	3.6 ns	3.8 ns	3.5 ns

*C1 adjusted for optimum pulse response

TABLE III. Settling Time Characteristics for Output Settling to within ±2.5% of Final Value*

R1	t_{sr}	t_r	t_{sf}	t_f
0Ω	8.5 ns	3.2 ns	8.9 ns	3.0 ns
15Ω	6.3 ns	3.4 ns	3.8 ns	3.3 ns
24Ω	6.1 ns	3.6 ns	4.2 ns	3.5 ns

*C1 adjusted for optimum pulse response

tradeoff between settling time and rise/fall time. The settling time for the same device measured to within ±2.5% of the final value is shown in Table III. The trend is clear, as R1 increases from 0Ω to 24Ω the worst case settling time decreases from 8.9 ns to 6.1 ns. As R1 is further increased, an optimum value will be reached where the settling time is minimum and any incremental change in R1 will degrade the settling time.

4.0 PROTECTING AMPLIFIER OUTPUT FROM TUBE ARCING

Arcing within the CRT is a rare phenomenon, however, during the life of the tube arcing may occur. Spark gaps are widely used at the CRT's cathode and the grids to protect against arcing. Spark gaps have low capacitance and a fast turn on time. When the potential across the spark gap exceeds the specified threshold, the spark gap turns on and provides a low impedance ground return for the high arc-over current. Once the accumulated charge has been discharged, the CRT can no longer sustain arcing and the spark gap returns to its high impedance normally off state. A 50Ω–100Ω resistor is also connected between the CRT video amplifier and the cathode. The resistor provides current limiting in the presence of a high arc-over voltage.

5.0 PREVENTING SPURIOUS OSCILLATIONS

The LH2422 includes a high frequency bypass capacitor mounted near the supply pin thus making the device less prone to oscillations. However, precautions must be taken to prevent excessive overshoot and ringing caused by the output wire inductance. Usually a piece of wire connects the video amplifier's output to the CRT's cathode. The wire's inductance and the capacitance at the cathode form an LC tank circuit when driven by the amplifier. At it's resonant frequency, the tank circuit may introduce overshoot and ringing. A damping resistor in series with the output can critically damp the output ringing. The resistor value may either be emperically determined or it may be calculated from the following equation :

$$\text{Damping Resistor, } R > 2\sqrt{L/C} \qquad (4)$$

Where, L = Inductance of output wire
C = Capacitance at CRT cathode

Usually a 50Ω–100Ω damping resistor is adequate. As an added advantage, the damping resistor also protects the amplifier's output against tube arcing by providing current limiting. Keep in mind that the damping resistor should not be too large otherwise the output signal's rise/fall time may be significantly affected due to the RC time constant formed by the damping resistor and the cathode's capacitance.

6.0 CONTROLLING ELECTROMAGNETIC INTERFERENCE (EMI)

There are stringent requirements on the manufacturers of electronic products to control the emission of electromagnetic waves. Electromagnetic waves not only interfere with radio and TV reception but may also affect other electronic devices in the vicinity of the source of radiation.

Voltage spikes caused by fast switching currents and the impedance of the supply line and ground connection give rise to EMI radiation. An effective way to combat EMI radiation is by making use of power supply filtering and generous use of a ground plane on the printed circuit board. The ground plane provides a low impedance return for the fast switching current, thereby suppressing EMI radiation. Note that LH2422's metal tab is internally connected to the device's ground pins. Thus connecting the amplifier's metal tab to the printed circuit board's ground plane through a heatsink accomplishes both heat sinking and suppression of EMI radiation. Additionally, CRT manufacturer's also use conductive shield enclosures to not only minimize emission of EMI radiation but also to prevent EMI radiation from entering the Monitor. In response to the offending electromagnetic field, the shield produces currents which in turn produce magnetic fields that oppose and cancel the inducing field. A steel enclosure provides excellent attenuation of EMI radiation through reflection and absorption loss (caused by the exponential decay of the electromagnetic wave's amplitude as it travels through the medium). Some monitors may have an electrically conductive polymer coating applied to the interior of its plastic cover.

7.0 MANAGING POWER DISSIPATION

Lets face it, the LH2422 is power hungry and requires that the package be heat sunk for proper operation under any condition. The worst case power dissipation occurs during full scale transitions i.e., when vertical lines of alternate black and white stripes are displayed on the screen. As shown by the curves in *Figure 7*, the power dissipation of the amplifier not only depends on the power supply but also increases linearly with frequency. For instance, at 60V power supply and 50 MHz (10 ns pixel), the power dissipation is 4.5W. Such high power dissipation demands that proper care be exercised to insure sufficient heat sinking.

LH2422's maximum ratings require that the device case temperature be limited to 80°C maximum. Thus at 50°C maximum ambient temperature and 4.5W maximum power dissipation, the thermal resistance of the heat sink should be less than (80°C − 50°C)/4.5W = 5.7°C/W. Several approaches to heat sinking may be taken. The simplest is a slug of aluminum with a volume of 4 cu. inches or a sheet of aluminum with an area of 32 square inches and a thickness of 0.125 inches. Alternately, commercially available heat sinks such as Thermalloy 15509 or AAvid 61875 extrusion (see *Figure 8*) may be used. The following guidelines should be followed for best results:

(a) Use a thermal joint compound (such as Thermacote from Thermalloy or the 340 silicone heat sink compound from Dow Corning) between the heat sink and the LH2422's metal tab. The thermal joint compound is a grease that establishes a low thermal resistance between the package and the heat sink by displacing the air gaps.

(b) Apply proper torquing (i.e., mechanical stress) so that good thermal contact is established.

(c) Mount the heat sink vertically. This causes the heat sink to lose heat because of cold air moving from bottom to top due to convection and is especially useful for heat sinks with fins (such as Thermalloy 15509 or AAvid 61875).

(d) Paint the heat sink with black oil paint or apply a dark varnish. This further reduces the heat sink's thermal resistance due to better radiation heat transfer.

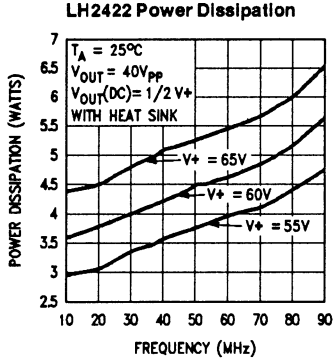

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FIGURE 7. LH2422's Power Dissipation Increases Almost Linearly with Increasing Frequency

8.0 BUILDING A 100 MHz HIGH RESOLUTION MONOCHROME MONITOR

Figure 9 shows the circuitry required to amplify and process the video signal and to drive the CRT cathode. The LM1201 pre-amplifier in *Figure 9* not only amplifies the 1 V_{pp} video signal but also provides brightness control, contrast control and black level clamping as will be discussed in this section.

The composite video signal from the host computer is ac coupled to the input of LM1201 through a blocking capacitor, C1, and is referenced to 2.6V by an internal reference. Amplifiers A1 and A2 shown in the block diagram of LM1201 (see *Figure 9*) provide a gain of 8; shorting the drive resistor, R20, will provide additional gain. The potentiometer R18 provides a variable voltage at LM1201's contrast control pin (pin 4) thus allowing attenuation of the video output signal. A nearly linear 0 dB to 30 dB attenuation can be obtained by varying the contrast voltage. Contrast control adjustment thus allows the user to vary the gain of the video signal.

The LH2422 in *Figure 9* is configured for midband gain of 13.6 as per equation (2). Variable capacitors C18 and C19 provide gain peaking at high frequencies and should thus be adjusted for best rise/fall time and low overshoot at the CRT cathode. To obtain a 40 V_{pp} output signal at the cathode, a 3 V_{pp} signal centered on 1.5 V_{DC} is required at the R_F input port of LH2422. This requires a signal swing from 0V to 3V but the video output signal of LM1201 does not swing all the way down to ground. In order to interface the LM1201 and the LH2422 and yet accommodate the quiescent voltage requirements of the two devices, level shift diodes D1, D2, D3 and a high speed buffer transistor Q1 (2N5770) where included. Adjusting the potentiometer at the brightness control pin (pin 9) of LM1201 allows the user to vary the DC offset of LM1201's output signal at pin 8 which in turn varies the DC level of the input signal at LH2422's R_F input port. Brightness control thus allows the user to vary the overall brightness or luminance of the picture displayed on the screen.

In addition to brightness and contrast control, LM1201 also accomplishes black level clamping. To understand the role of black level clamping we need to look back at the video signal.

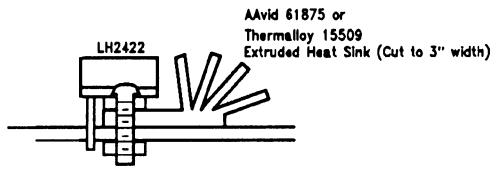

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FIGURE 8. Heat Sinking with an Extruded Heat Sink such as Thermalloy 15509 or AAvid 61875

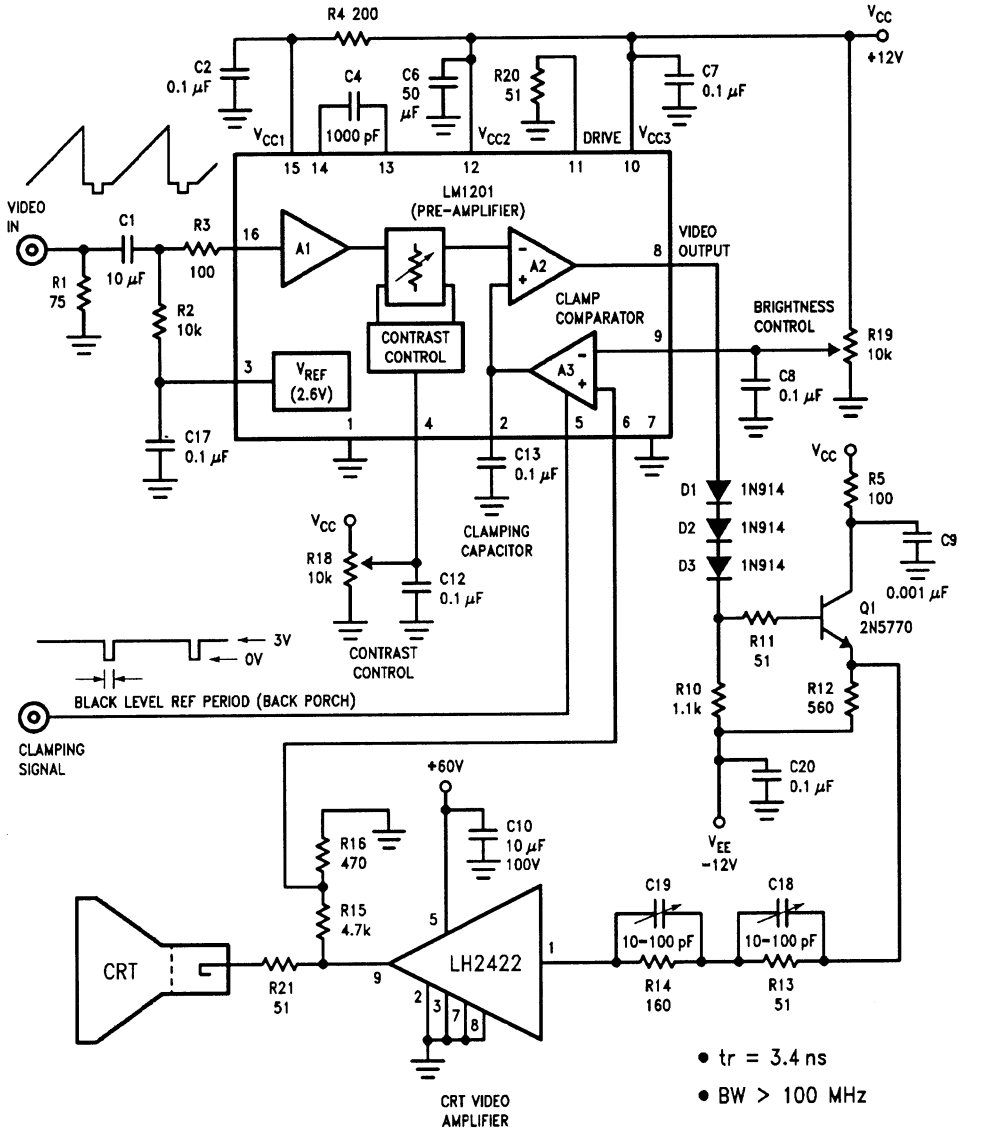

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FIGURE 9. Circuit shows how the LM1201 pre-amplifier and LH2422 CRT Video Amplifier may be used to build a 100 MHz monochrome monitor.

Manufacturers of computers and monitors generally follow the EIA standard RS-343 for video signal. The RS-343 standard specifies the various video signal levels relative to a reference level. Usually the black level is used as a reference. It is interesting to note that no DC component is specified, the reason is that the standard was developed for television. Since the TV signal travels through air, the DC component of the signal is lost. At the receiving end, the signal is ac coupled. However, a DC restoration circuit is required to reinsert the DC component of the video signal. By reinserting the DC component of the video signal, brightness of each line is restored since the brightness level may be different for each line. DC restoration is thus essential for producing the correct background illumination or shading. Likewise for monitors, the video signal is ac coupled at the input so that the monitor can easily interface with computers from various manufacturers.

Figure 10(a) shows the 1 V_{pp} composite video signal with sync tip. Meanwhile the signal at the cathode is an amplified signal of opposite phase as shown in *Figure 10(b)*. Since the video signal is amplitude modulated, the signal's amplitude relative to the reference black level specifies the relative brightness of the signal. The black level corresponds to the CRT cathode's beam cutoff. In most monitors, a large negative potential is applied to the CRT's grid during the blanking interval thus preventing the retrace lines from being displayed. The LM1201 uses black level clamping at the back porch of the video signal to accomplish DC restoration. LM1201's clamp comparator, A3, is enabled during the black level reference period to provide a sample and hold function. DC feedback taken from LH2422's output during the black level reference period is compared with the voltage set by the brightness control potentiometer R19. Depending on the LH2422's output voltage, the clamping capacitor is charged or discharged so that the feedback loop consisting of amplifiers A2, A3 and LH2422 is stabilized and that LH2422's output is restored to the black level. All this occurs during the horizontal retrace interval. During the video portion of the signal, A3 is disabled and clamping capacitor, C13, holds the fixed black level reference voltage. The beginning of each new line thus always starts from a fixed reference black level and the DC component of each line is restored. Adjusting the contrast control varies the amplitude of the video signal on each line relative to the fixed black level. For the complete circuit of *Figure 9* (from video input to the CRT cathode), rise and fall times of 3.4 ns and 3 ns respectively were measured at the cathode. This corresponds to a bandwidth of over 100 MHz. Note that damping resistor, R21, was not used.

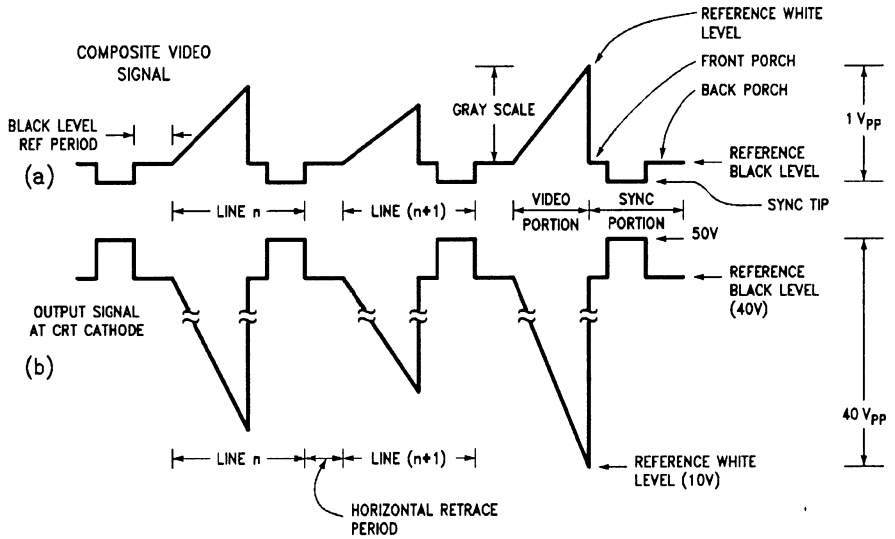

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FIGURE 10. The CRT Video amplifier is a high voltage wide bandwidth inverting amplifier that amplifies the 1 V_{pp} composite video signal (a) to a 40 V_{pp} signal at the CRT cathode (b).

A much simpler interface network for the LM1201 and LH2422 may be used (see *Figure 11*). The RC interface network of *Figure 11* not only eliminates the need for a handfull of discrete components such as the level shift diodes, resistors and transistor Q1 in *Figure 9* but also the additional negative supply, V_{EE}, is no longer required. A pull down resistor, R_A, is required to bias the emitter follower transistor of LM1201. As discussed earlier, the quiescent voltage of LM1201 output is much higher than what's required at LH2422's input. In the absence of R_B, LH2422's output would be in negative saturation because of its inverting gain. Connecting a resistor R_B from LH2422's input to ground causes the inverting amplifier's output to rise, thus counteracting the effect of LM1201's high quiescent output voltage. To select the appropriate resistor values, the DC level of LM1201's output pulse should be measured first. Package power dissipation considerations for LM1201 require that the average current from LM1201's output be limited to about 20 mA, this requirement thus puts a limit on how low the resistor values can be. The DC voltage of LM1201's pulse output for this setup was measured at 4.6V. Using a 500Ω resistor for R_A biases LM1201's emitter follower at a DC current of 9 mA. A 300Ω resistor was selected for R_G so as to provide an ac gain of 10 for the LH2422. A bias voltage of V_B = 1.6V was measured at LH2422's input. Finally to bias the output of LH2422 to $V_+/2$ = 30V, the required resistor value R_B can easily be calculated by substituting the values for R_G, R_F, V_B and V_{IN} (LM1201's DC output voltage) in equation (3). Alternately, a potentiometer may initially be substituted for R_B, the potentiometer is then adjusted so that the ac signal at LH2422's output is centered on $V_+/2$ volts. If desired, the potentiometer may be replaced with a fixed resistor corresponding to the desired value. Note that brightness control at LM1201 provides additional control over LH2422's output offset. A resistor value of R_B = 180Ω seemed to do the job well. Since LH2422's inverting input is clamped at 1.6V the DC current through R_G is 10 mA (i.e., [4.6V−1.6V]/300Ω). Thus with 9 mA DC current through R_A and 10 mA through R_G, the average current drawn from LM1201's output is 19 mA and within the power dissipation limits of the device.

Note that although the interface circuit of *Figure 11* is much simpler than that of *Figure 9*, there is a penalty for speed. The rise and fall times at the cathode (without the damping resistor, R_1) was measured at 4.2 ns and 3.2 ns respectively for the same devices used in *Figure 9*'s circuit. The bandwidth of *Figure 11*'s circuit is over 80 MHz. Thus there are tradeoffs between the circuits of *Figure 9* and *Figure 11* as summarized in Table IV.

TABLE IV. Comparison of Circuits in *Figure 9* and *Figure 11*

Circuit	t_r	t_f	BW	Comments
Figure 9	3.4 ns	3 ns	>100 MHz	Requires Discrete Level Shift Stage and an Additional Negative Supply Voltage
Figure 11	4.2 ns	3.2 ns	>80 MHz	Requires Simple RC Interface Network and Works from Single Positive Supplies

9.0 BUILDING A HIGH RESOLUTION COLOR MONITOR

A high resolution color monitor can be easily designed using a pair of LM1201 pre-amplifier and LH2422 CRT video amplifier for each channel (see *Figure 12*). The contrast control pins (pin 4) of each pre-amplifier are connected together, meanwhile, potentiometer R13 provides a common contrast adjustment for all three guns. For best tracking of contrast control, pin 14 of each pre-amplifier are connected together. Furthermore, pin 13 of green channel's pre-amplifier is connected to the corresponding pin of red and blue channel pre-amplifiers through 10Ω decoupling resistors, R14 and R15. R14 and R15 are required to prevent loop instability.

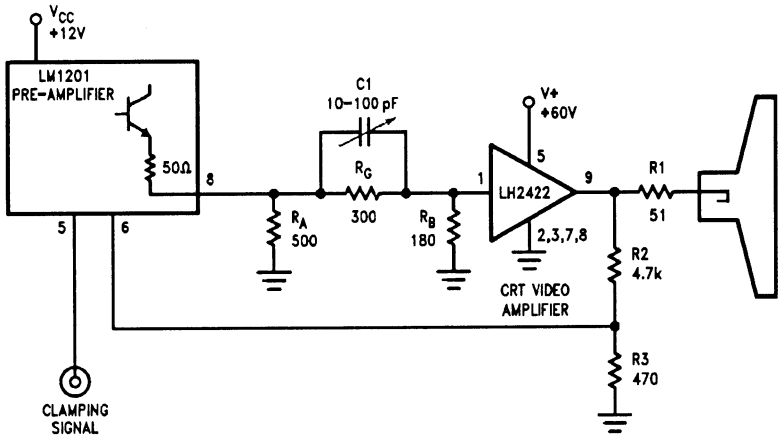

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FIGURE 11. Circuit shows a simple RC interface network for LM1201 and LH2422 which eliminates the need for a level shift stage and additional V_{EE} supply of *Figure 9*.

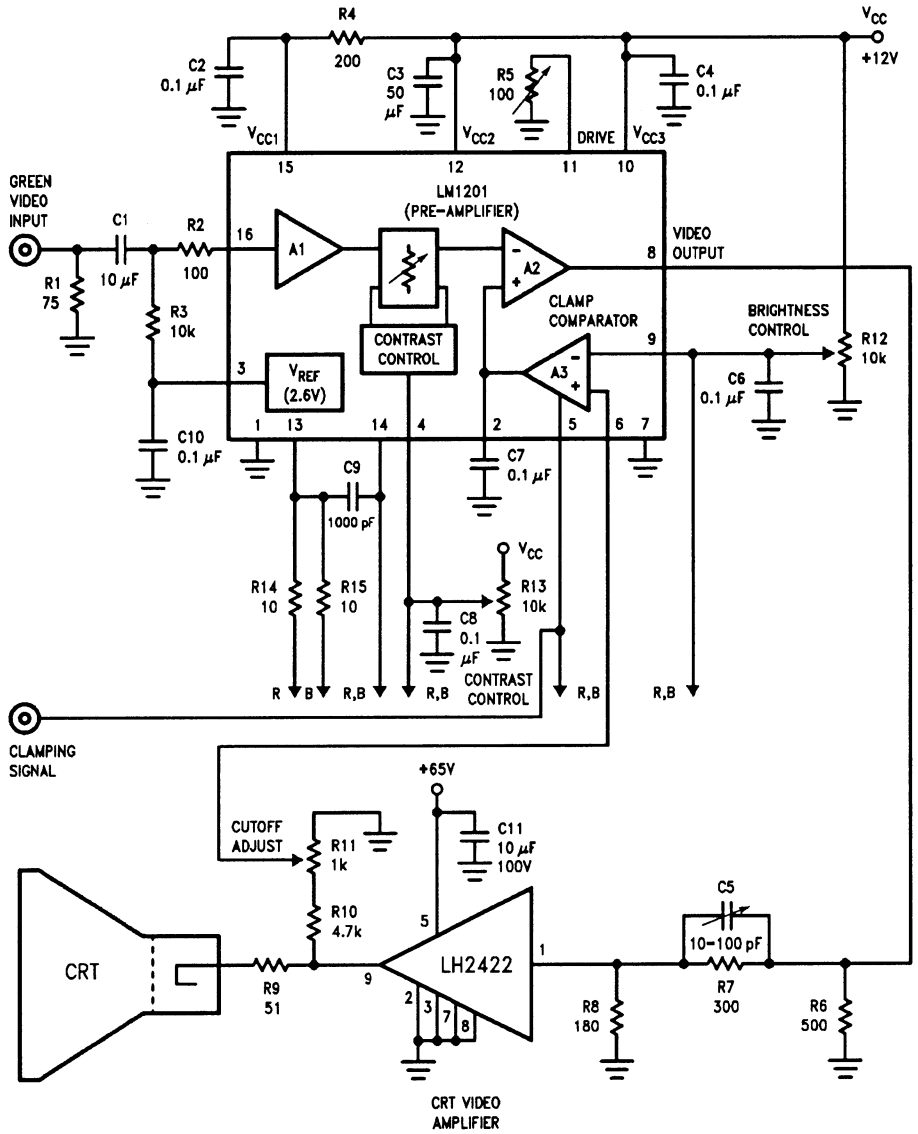

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FIGURE 12. Circuit for a low voltage color monitor uses a pair of LM1201 pre-amplifier and LH2422 CRT video amplifier for each channel.

Note that the drive resistor, R5, connected between the pre-amplifier's pin 11 and ground controls the ac gain of the video signal. By making the drive resistor variable, the mismatch in the ac drive levels for each of the three guns can be compensated. The spot cutoff voltage for each gun corresponds to the potential applied at the CRT cathode which causes the beam spot to disappear from the screen, thereby establishing the black level. The cutoff voltage of each gun within the same tube are not matched and thus require different cathode potentials to bring each gun to cutoff. By making the clamp feedback resistor R11 variable, individual cutoff adjustment for each gun is easily achieved. With pin 9 of each pre-amplifier connected together, potentiometer R12 allows a common brightness control adjustment for all three guns. Note that the circuit of *Figure 12* works well for a low voltage color monitor that has a very narrow spread in cutoff voltages. The major limitation is set by LH2422's maximum 70V supply voltage, which requires that the worst case cutoff voltage be below 65V since the amplifier's linear range extends to within 5V off each supply rail.

Many CRTs have a spread of as much as 25V or more in cutoff voltages for the three guns within the same tube. To accommodate such a large variation in cutoff voltages, LH2422's output can no longer be DC coupled to the CRT's cathode. The output can, however, be ac coupled. A black level clamping circuit using diodes must then be included at the output to restore the DC component of the video signal.

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Understanding The Operation of a CRT Monitor

National Semiconductor
Application Note 656
Zahid Rahim
November 1989

Computer technology is going to see major advances in the 1990s. Users will see desk top computers with the computational power of today's super-computers. Even graphics capabilities for sophisticated 3 dimensional modeling and image processing would be available to the average user at a reasonable cost. In the area of electronic publishing; users will be able to store video images in the computer, merge the images with text and graphics and produce true color photorealistic hardcopies. Ultra high resolution monitors will be required to make such graphics capabilities available.

Display systems are available in various technologies such as cathode ray tubes (CRTs), liquid crystal displays (LCDs), electroluminescent displays (EL), plasma displays, and light emitting diodes (LEDs). However, for high resolution monitors the CRT has been and continues to be the technology of choice. Besides its awkward shape, weight and high voltage requirements, the CRT offers many advantages over its competitors. As opposed to other display systems that require a driver for each picture element (pixel), the CRT requires a single driver to drive the tube's cathode or three drivers for a color display. CRTs also offer excellent contrast, luminance and better display resolution than its counterparts. Even though the brightness of the CRT's screen is not uniform across the face of the screen, the variation from the center to the corners is gradual and may be unnoticeable to most viewers. In the case of LCD or LED displays, however, a very tight brightness level matching is required among the adjacent pixels. Continued improvements over the years and declining prices have made the CRT a popular choice for high resolution monitors.

The operation of a CRT monitor is basically very simple. A heating element in a CRT heats the cathode and causes it to emit electrons which are accelerated and focused on a phosphor screen by means of high voltage grids. An image (raster) is displayed by scanning the electron beam across the screen. Since the phosphor's luminance begins to fade after a short time, the image needs to be refreshed continually. In order to eliminate flicker, most monitors refresh the screen at a 60 Hz rate.

Figure 1 shows a simplified block diagram of a color CRT monitor. The entire circuitry within the monitor can be grouped into three main categories: video signal processing and amplification, horizontal/vertical deflection and synchronizing, and power supply. As shown in *Figure 1*, a transmission line or a coaxial cable carries the video signal from the host computer to the monitor. The video signal is usually a 1 V_{PP} signal and thus requires amplification before the signal can be applied to the CRT's cathode. The amplification of the video signal is usually done in two stages. A low voltage amplifier, often called a preamplifier, amplifies the 1 V_{PP} signal to a 4–6 V_{PP} signal. In addition to amplification, the preamplifier also provides contrast and brightness control. Contrast control allows the user to vary the gain of the video amplifier. Increasing the contrast for instance increases the video signal's level and thus causes the lighter portions of the raster to be brighter than the darker portions. The result is a sharp picture with contrasting light and dark. Brightness control on the other hand allows the user to change the brightness of the raster by varying the DC offset of the video signal. Increasing brightness in effect makes both the light and dark portions of the image brighter. Most preamplifiers also provide DC restoration or black level clamping which makes the brightness control possible. This will be described later in the text.

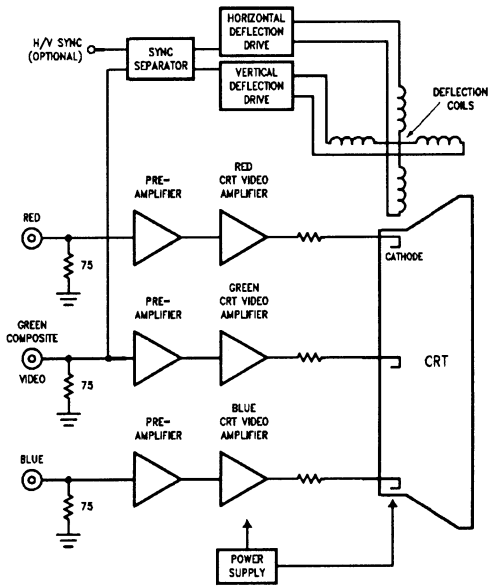

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FIGURE 1. Simplified Block Diagram of an RBG Monitor

CRT VIDEO AMPLIFIER PROVIDES HIGH VOLTAGE AMPLIFICATION

The CRT video amplifier is the second stage amplifier, it amplifies the preamplifier's 4–6 V_{PP} signal to a 40–60 V_{PP} signal that the cathode requires to energize each phosphor dot on the screen. In a color monitor, there is a trio of red, green and blue phosphor dots. Together, each trio constitutes a picture element, often called a pixel for short. The light emitted by the phosphor dot is proportional to the number of electrons striking the phosphor. Thus by modulating the voltage of each of the three cathodes in a color monitor, the corresponding phosphor dot is energized at varying intensities, thereby producing various shades of color. To change a pixel from black to peak white, the CRT video amplifier may be required to swing as much as 40 V_{PP}. The higher the display resolution of a monitor, the shorter the time available to energize each pixel. Thus high resolution monitors demand wide bandwidth amplifiers, which is generally not a problem when designing preamplifiers because of its low voltage swings of 4–6 V_{PP}. However, achieving wide bandwidth from a CRT video amplifier is no trivial task. The transistors required should not only have breakdown voltages of 70–80V but must also maintain f_T of 1 GHz to 2 GHz at high collector currents.

Table I illustrates the key requirements for various pixel display resolution monitors currently available in the market. Note that the maximum pixel time is derived assuming a 60 Hz frame refresh rate and retrace time equivalent to 30% of each frame time. Also as a rule of thumb, 33% of the pixel time is generally allocated to the rise/fall time of the signal at the CRT cathode. For ease of analysis we may assume that the CRT video amplifier is linear and has a single pole roll off. Thus the amplifier's bandwidth may be approximated as $f_{-3\ dB} = (0.35)/t_r$, where t_r is the signal rise time.

Figure 2(a) shows a simplified cross-sectional view of a color CRT. A heating element biased at approximately 6V and 500 mA to 2A (depending on the tube) heats up the cathodes. Heating the cathodes energizes the electrons in the cathodes and greatly aids in the emission of electrons. A large DC potential, on the order of several hundred volts more positive than the cathode is applied at the second grid, G2. This causes the electron beam to be accelerated towards the screen. Since the beam emerging from the cathode tends to diverge, a negative potential with respect to the cathode is applied at grid G1. By making G1 (also called control grid) more negative than the cathode, the electron beam begins to converge as shown in *Figure 2(b)*. This action is similar to beam focusing using an optical lense. Furthermore, by modulating the potential difference between the cathode and the control grid, the beam intensity and hence the brightness level is modulated. Finally the beam is electrostatically focused on the screen by adjusting grid G3's potential until the desired focus is achieved.

TABLE I

Display Resolution	Maximum Pixel Time	Minimum Pixel Clock Frequency	Required Rise Time at CRT Cathode	Required System Bandwidth ($f_{-3\ dB}$)
320 x 200	182 ns	5 MHz	60 ns	6 MHz
640 x 350	52 ns	19 MHz	17 ns	20 MHz
640 x 480	38 ns	26 MHz	12.5 ns	28 MHz
800 x 560	26 ns	38 MHz	8.6 ns	41 MHz
1024 x 900	12.6 ns	80 MHz	4.2 ns	84 MHz
1024 x 1024	11 ns	90 MHz	3.7 ns	95 MHz
1280 x 1024	8.9 ns	112 MHz	2.9 ns	120 MHz
1664 x 1200	5.8 ns	170 MHz	1.9 ns	180 MHz
2048 x 2048	2.8 ns	360 MHz	1 ns	380 MHz
4096 x 3300	860 ps	1.2 GHz	280 ps	1.23 GHz

Note: This table assumes 60 Hz refresh rate and retrace time equivalent to 30% of each frame time.

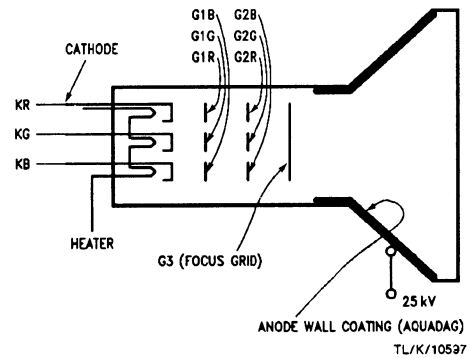

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FIGURE 2(a). A cross-sectional view of a color tube shows the arrangement of the grids.

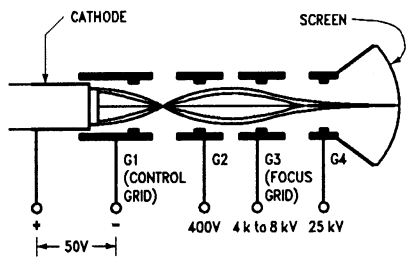

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FIGURE 2(b). The electron beam is accelerated and electrostatically focused by applying the appropriate potential at the respective grids.

COLOR TUBES REQUIRE ADJUSTMENTS TO BALANCE THE GUNS

As the cathode potential is increased with respect to G1, a potential is reached at which the beam spot on the screen disappears. This potential is called the spot cutoff voltage and thus corresponds to the voltage that produces the black level. The cutoff voltage is usually different for each of the three guns in a color tube. Thus the cutoff voltage needs to be individually adjusted for each gun so that at cutoff all three guns are at the black level. For a picture tube of the type shown in *Figure 2*, the adjustment can be made by individually adjusting the potential at the corresponding control grid, G1. However, most modern day color tubes uses a unitized gun in which G1 and G2 are common to all three guns. Among the advantages of a unitized gun are that it produces a better spot size resulting in bright pictures and better gray scale tracking. Cutoff voltage adjustment in a unitized gun now requires that the cathode voltages be adjusted. This places a burden on the CRT video amplifier because the large variation of cutoff voltages within the tube must now be compensated by adjusting the video amplifier's DC offset. The spot cutoff design curves for a typical unitized tube is shown in *Figure 3*. At grid 2 to grid 1 voltage ($V_{G2}-V_{G1}$) of 400V the cathode to grid 1 cutoff voltage varies from 50V to 70V as shown by the curves. Thus if the CRT video amplifiers are coupled directly to the cathodes and with V_{G1} = 0V, the amplifiers must be designed to be able to swing at least as high as 70V because of the 20V variation between the guns within the tube. Note that biasing G2 at a higher potential would be desirable because of the improved spot size, consequently a brighter picture. However, doing so would require a higher cutoff voltage and thus place a heavier burden on the amplifier driving the cathode. In contrast, a monochrome CRT doesn't have this problem because of the single gun.

Neutral white is the most difficult color to produce in a color monitor because the light emitting efficiency of R, G and B phosphors is different. Thus a specific proportion of R, G and B drive levels are required at the three cathodes to produce neutral white. The peak amplitude of the cathode drive signal determines the shade of white that will be displayed. Thus neutral white is produced by adjusting the AC gain of each of the three preamplifiers. Usually the red gun is driven at maximum gain because of red phosphors's lowest efficiency, and, the gain of the green and blue guns are reduced until the desired balance is achieved. Keep in mind that once the gain adjustments have been made, the contrast control will vary the gain of all three guns simultaneously. Also the color on the screen should not change as the screen's brightness level is changed, this is often referred to as gray scale tracking. Good gray scale tracking requires that the amplifiers have good differential gain characteristics as well as good DC output tracking capability. Furthermore, the amplifiers should also track well over a wide range of contrast adjustment.

Manufacturers of computers and monitors generally follow the EIA standard RS-343 for video signal. The RS-343 standard specifies the various video signal levels relative to a reference level. It is interesting to note that no DC component is specified, the reason is that the standard was developed for television. Since the video signal in broadcast television travels through air, the DC component of the signal is lost. At the receiving end the signal is AC coupled. However, a DC restoration circuit is required to reinsert the DC component of the video signal. By reinserting the DC component of the video signal, brightness of each line is restored since the brightness may be different for each line. DC restoration is thus essential for producing the correct background illumination or shading. Likewise for monitors, the video signal is AC coupled at the input so that the monitor can easily interface with computers from various manufacturers.

Figure 4a shows the 1 V_{PP} composite video signal with sync tip. The signal at the cathode is an amplified signal of opposite phase as shown in *Figure 4b*. The video signal for three

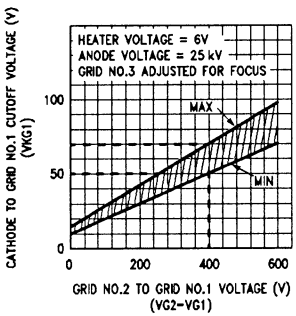

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FIGURE 3. Spot Cutoff Characteristics for a Typical Color Tube

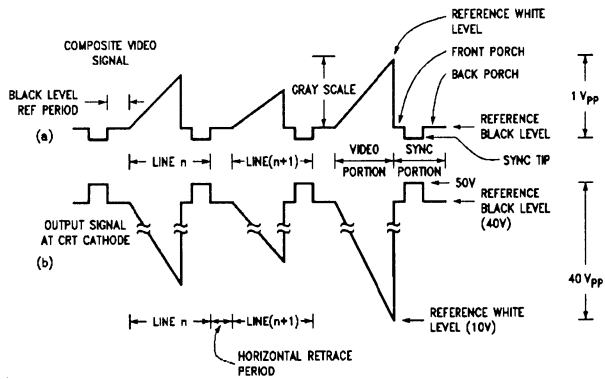

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FIGURE 4. The composite video signal is a 1 V_{PP} signal that carries both the amplitude and sync information (a). A wide bandwidth inverting amplifier amplifies the signal at the cathode (b).

lines of the raster are shown. Since the video signal is amplitude modulated, the signal's amplitude relative to the reference black level specifies the relative DC component of each line on the raster. The DC component of the video signal is thus restored by clamping the black level at a fixed reference potential (e.g., 40V), corresponding to the CRT's beam cutoff voltage. The video signal's video portion contains the gray scale information (i.e., the signal's amplitude) whereas the sync portion contains the timing information required for horizontal and vertical synchronization.

DC restoration of the video signal can be done in two ways. The first method is to use a simple diode clamp to clamp the signal at the reference black level. Diode clamping can be done either at the AC coupled input of the preamplifier or at the AC coupled output of the CRT video amplifier. The disadvantage of diode clamping is that the black level is sensitive to fluctuations in the power supply as well as noise coupling and temperature drift of the diode's forward drop. A more effective approach for DC restoration is to do a dynamic black level clamping at the back porch of each video signal. This requires the use of comparator within the feedback loop of the CRT video amplifier and the preamplifier. During the horizontal retrace period, the comparator compares the DC feedback taken from the CRT video amplifier's output with the voltage set by the brightness control potentiometer. Depending on the CRT video amplifier's output voltage, a clamping capacitor at the output of the comparator is either charged or discharged so that the feedback loop is stabilized and the video signal is restored to the black level. During the video portion of the signal, the comparator is disabled and the clamping capacitor holds the black level reference voltage until it is refreshed at the beginning of the next line. The beginning of each new line always starts from a fixed reference black level and the DC component of each line is restored. This approach not only offers excellent power supply rejection but also there is minimal black level drift because the black level is brought back to the correct reference potential during each horizontal retrace period.

WITHOUT DEFLECTION CIRCUITRY THERE WOULD BE NO RASTER

An image is displayed in a CRT by scanning the electron beam across the face of the screen. The beam is scanned from left to right on each line, moreover, at the end of each line the beam drops down to the beginning of the next line. The motion from right to left is called horizontal retrace. During the horizontal retrace interval the electron gun is biased at a potential such that the retrace lines are invisible. Note that the horizontal retrace interval coincides with the horizontal blanking interval (part of the composite signal's sync portion). There are two methods of accomplishing blanking. The first approach is to disable the preamplifier during the blanking interval and bias the CRT video amplifier at a potential higher than the CRT's spot cutoff voltage. This effectively prevents the retrace lines from being visible. The second approach involves the application of a large negative potential at the control grid (G1) during the blanking interval.

Once all lines on the screen are traced, the beam moves from the bottom to the top during the vertical retrace interval. The composite video signal contains the horizontal sync pulse which is repeated at the horizontal scan rate. The horizontal scan rate may be anywhere from 15 kHz to 240 kHz depending on the resolution of the monitor. The vertical sync pulse is much wider than the horizontal sync pulse and occurs at the end of the raster, i.e., after all lines in the frame have been traced. The vertical sync pulse is repeated at a 60 Hz rate. For proper operation, a sync separator separates the horizontal and vertical sync pulses from the composite video signals.

The simplified block diagram of *Figure 5* shows the circuitry required for horizontal and vertical scanning, also shown is a high voltage flyback power supply. The composite video signal is AC coupled to the input of the sync amplifier Q1, whose gain is determined by the ratio of its collector and emitter resistors. The inverted video signal appears at the collector of Q1 and is buffered by the emitter follower Q2. Q3 is essentially a saturating sync switch that removes the signals' video portion and leaves only the sync pulses. Resistors R8 and R9 bias Q3's base at a potential below the cutin voltage of the transistor so that Q3 is normally off. When the composite video signal's level is between the blanking level and the sync tip, Q3 saturates and produces a negative going pulse at Q3's collector. The buffered output of Q4 is a composite sync signal that contains both the horizontal and vertical sync pulses. A two stage RC low pass filter separates the 60 Hz vertical sync pulses from the composite signal.

The vertical sync pulses trigger the vertical oscillator so that the oscillator is locked at 60 Hz. The vertical oscillator is usually a relaxation oscillator and drives the power transistor Q5 with a 60 Hz sawtooth voltage waveform. Q5 in turn energizes the vertical deflection coils with a 60 Hz sawtooth current ramp. The linear current ramp produces a magnetic field in the vertical deflection coil and causes the electron beam to move from top to bottom at a uniform speed. This accomplishes the task of moving the beam progressively from one line to the next as the raster is scanned. During the vertical retrace interval there is a rapid decrease in Q5's collector current, causing the beam to retrace rapidly from the bottom of the raster to the top. The amplitude of the current ramp is usually made adjustable because this allows the user to adjust the height of the raster.

The horizontal sweep circuit works similar to the vertical sweep circuit, however, there are some major differences. Since the horizontal sync pulses are narrow and operate at high frequency, they are susceptible to noise impulses. In order to maintain trouble free synchronization, an automatic frequency control (AFC) circuit is used. Moreover, the horizontal oscillator is a voltage controlled oscillator (VCO) as opposed to the triggered relaxation oscillator for the vertical sweep circuit. The AFC compares the phase of the horizontal sync signal with that of a sample of the horizontal output signal and produces a DC correction voltage proportional to the phasing of the two signals. The AFC's output signal is an error signal that locks the VCO such that the sync signal and the horizontal output signal are maintained at the sync signal's frequency. Without horizontal synchronization, the picture would tear up diagonally. Finally, a power output transistor, Q6, drives the horizontal deflection coils with several hundred milliamps of current depending on the mA/inch deflection ratings of the tube.

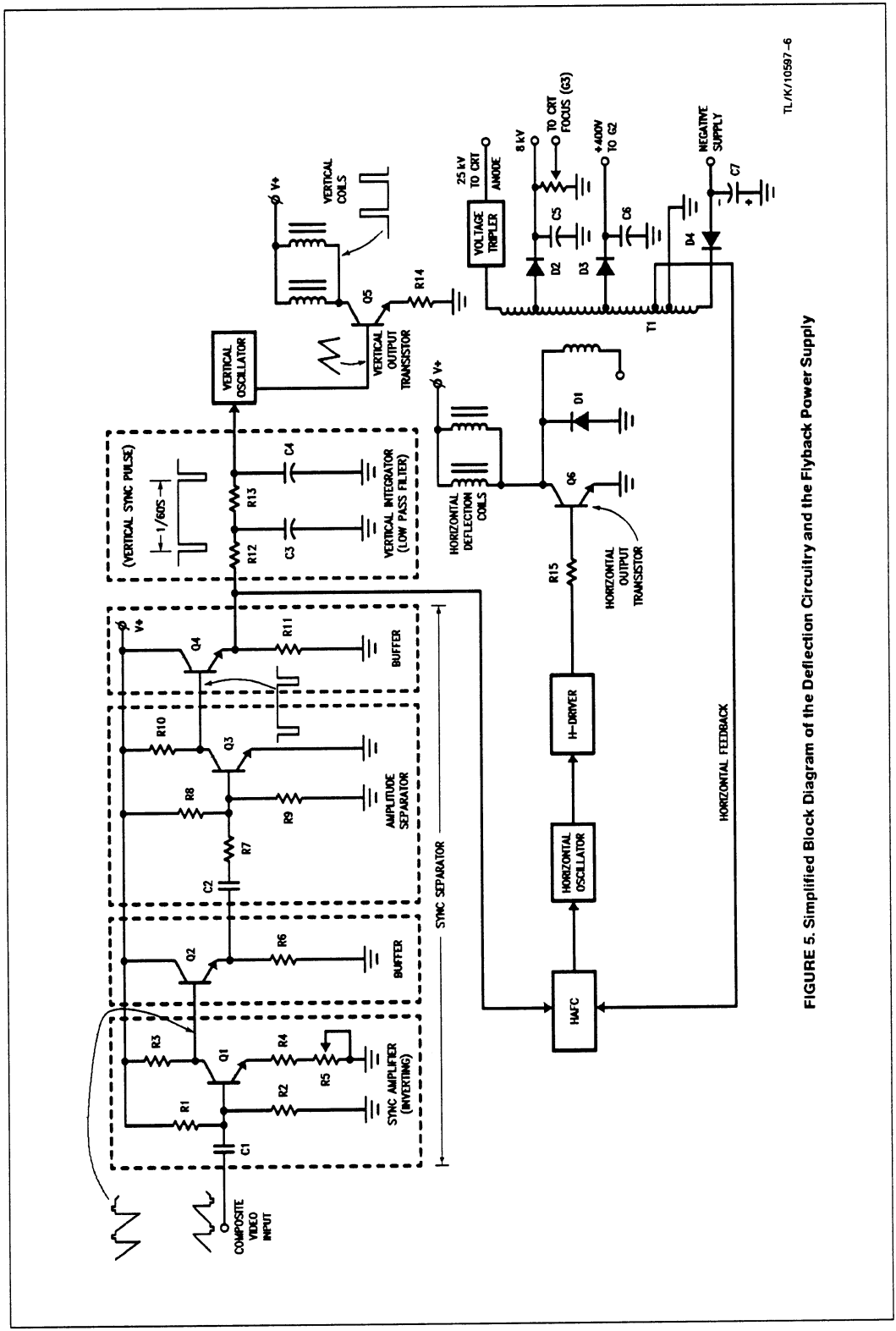

FIGURE 5. Simplified Block Diagram of the Deflection Circuitry and the Flyback Power Supply

THE SWEEP CIRCUIT ALSO GENERATES HIGH VOLTAGES

A switching regulator is used to produce a regulated DC voltage to power the low voltage circuits and the horizontal/vertical scanning circuit. The high voltages required for the CRT's grids and the high voltage anode are derived by the transformer action. The horizontal output transistor Q6 not only drives the horizontal deflection coils but it also drives the primary of the step up transformer T1.

During the horizontal retrace interval, the collector current of Q6 drops rapidly causing the transformer's magnetic field to collapse. The transformer's primary coil in turn produces a back EMF to sustain the current thus raising Q6's collector to a high potential. Through the transformer action, T1's secondary coil produces high voltages. A voltage multiplier circuit consisting of a diode and capacitor network multiplies the secondary coil's voltage to a 25,000V potential that the tube's high voltage anode requires. Other high voltages are derived by tapping various points on the secondary coil. A diode and capacitor network is used to rectify and filter the power supply voltage. A power supply of this type is often called a scanning or flyback voltage supply because of its association with the horizontal sweep circuit.

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