Interconnecting National Semiconductor's TP3420A SID to Motorola SCP/HDLC Devices

National Semiconductor
Application Note 931
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When interconnecting the National Semiconductor's TP3420A to a Motorola SCP/HDLC device (such as the MC68302), it is necessary to consider the timings for two separate ports. The MICROWIRE™ to SCP connections for the device control and secondly the transfer to B and D channel data between the HDLC ports and the TP3420A Digital System Interface prot.

1.0 MICROWIRE/SCP CONNECTIONS

NSC MICROWIRE and Motorola Serial Control Port (SCP) are examples of serial communication formats typically used to configure Telecom/ISDN components. They both consist of a 5-pin port.

— Clock pin CCLK/SPCKL,
— Data input pin CI/SPRXD
— Data output tpin CO/SPTXD
— A chip select pin/CS
— An interrupt line from the transceiver TP3420A to the controller to indicate a change of status.

There are 4 different modes for the relationship between the clock edges and data input/output for a serial communications port.

1. CCLK idling LOW, pulsing HIGH, then returning back to LOW for idle condition; data output on CO pin on the negative edge and data sampled in on the positive edge of CCLK (normal MICROWIRE mode).
2. CCLK idling HIGH, pulsing LOW, then returning back to HIGH for idle condition; data output on CO pin on the negative edge and data sampled in on the positive edge of CCLK (supported by enhanced MICROWIRE on TP3420A and SCP).
3. CCLK idling LOW pulsing HIGH, then returning back to LOW for idle condition; data output on CO pin on the positive edge and data sampled in on the negative edge of CCLK (supported only on the SCP).
4. CCLK idling HIGH, pulsing LOW, then returning back to HIGH for idle condition; data output on CO pin on the positive edge and data sampled in on the negative edge of CCLK.

The TP3420A SID supports modes 1 (NORMAL MICROWIRE mode) and mode 2. The SCP port of Mot 68302 supports modes 2 and 3. Hence set the SCP clock master to run in mode 2 above when interworking with the TP3420A (see *Figure 1* and *2*).

Set the 68302 SCP Master as follows:

Set CI = 1 in SPMODE register
Set the PM3–PM0 in SPMODE register to select clock rate (up to 2.048 MHz)
Use an I/O pin to perfrom chip select function $\overline{CS}$.
SCP port generates 8 clocks per command transfer which is compatible with the TP3420A.

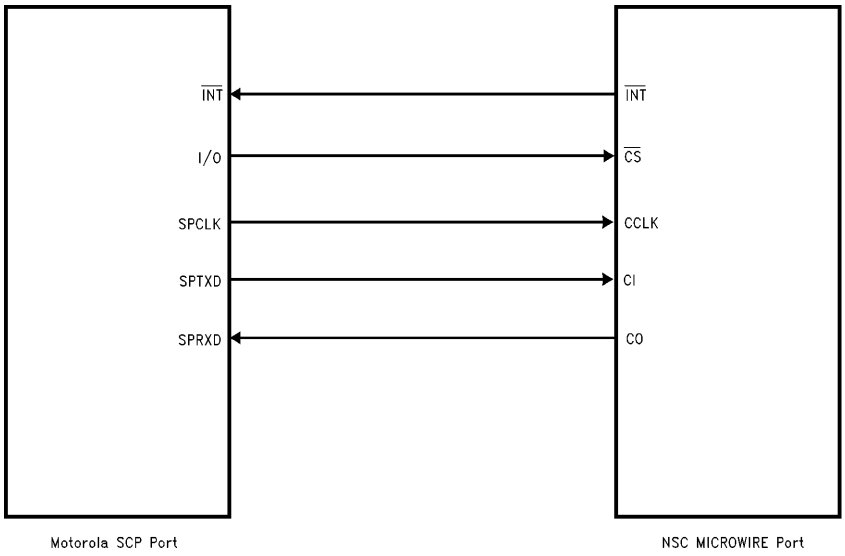

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FIGURE 1. MICROWIRE to SCP Connections

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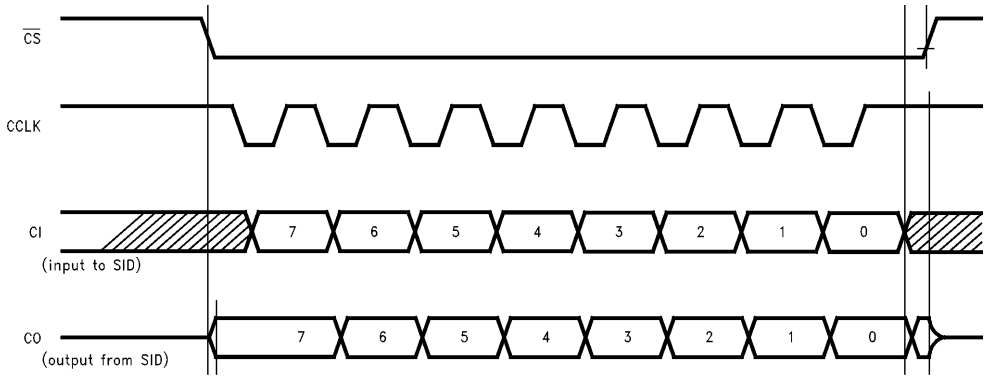

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FIGURE 2. TP3420A MICROWIRE/SCP Timing

2.0 B AND D CHANNELS CONNECTIONS BETWEEN TP3420A AND MOTOROLA HDLC DEVICES

The 2B channel data and the D-Channel data can be connected between the TP3420A (Rev 3.6) and the Motorola devices without any additional glued logic (TP3420A Rev 3.5 or prior revision devices when used in TEM application, will take a package of NOR gates and a TRI-STATE® buffer as shown in Appendix A). The following configurations should be used for the TP3420A (Rev 3.6) and the Motorola devices:

FOR TEM APPLICATIONS ONLY:

Settings For TP3420A:

- TEM (TE Clock Master) Mode
- DIF4A (Digital Interface Format 5)
  If the MC68302 operates in PCM Highway mode, the TP3420A may be set in DIF1 instead of DIF4A.
- D-Channel Clock Enable, DCKE.

Settings for MC145488:

- Channel 0 routed to the IDL interface to cover a B channel
- Channel 1 routed to the NMSI interface to cover the D channel

Its connection with the TP3420A (Rev 3.6) is shown in *Figure 3*

Settings for MC68302:

One SCC routed to the IDL interface to cover a B channel. For datacom applications, 2 SCCs routed to the same IDL interface to cover both B channels.

One SCC routed to the NMSI interface.

It is also possible to use PCM Highway Interface instead of the IDL interface in the MC68302, but this is not shown here.

Its connection with the TP3420A (Rev 3.6) is shown in *Figure 4*.

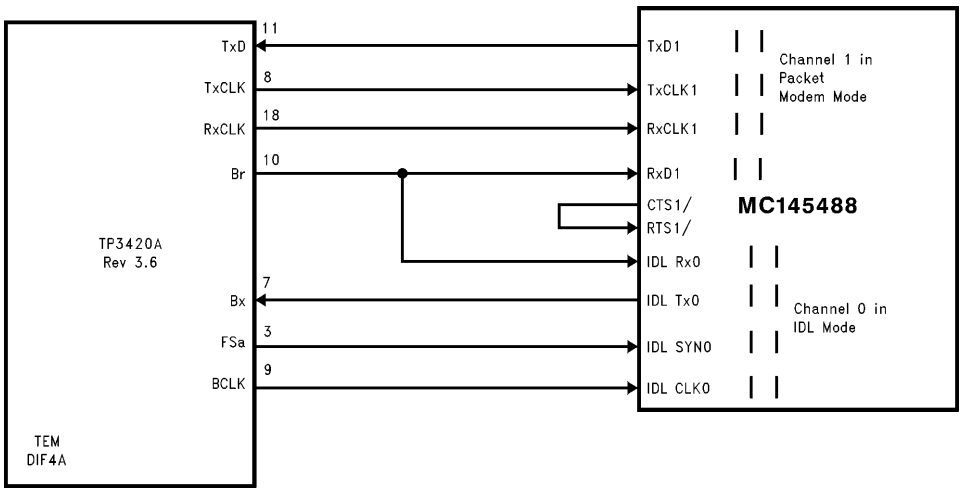

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FIGURE 3. 2B + D Interconnection between the TP3420A (Rev 3.6) and the MC145488

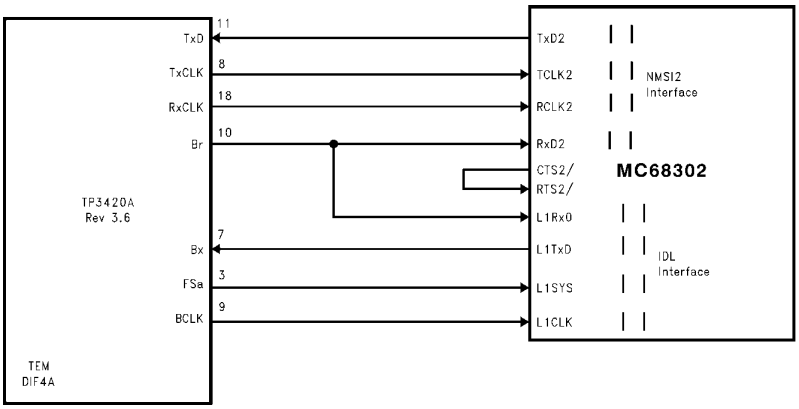

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FIGURE 4. 2B + D Interconnection between the TP3420A (Rev 3.6) and the MC68302

The digital interconnection signals are shown in *Figures 3* and *4* and the relevant timings are shown in *Figure 5*. The Motorola devices operate on the B-Channel data via its IDL interface, and on D-Channel data via its NMSI interface. For voice applications, one B-Channel data can be directly connected to a NSC COMBO such as the TP3076. For Datacom applications, both B-Channel data can be connected to the MC68302 to the same IDL interface.

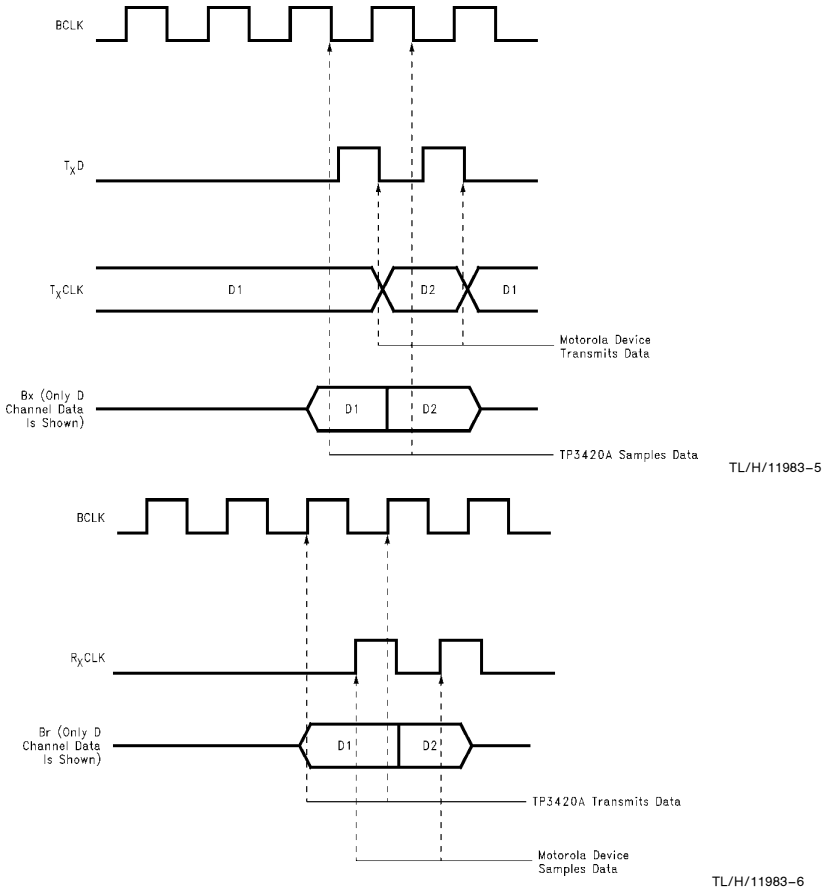

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FIGURE 5. Timing Diagrams

The B-Channel connection is straight forward, since DIF5 in the TP3420A is compatible with the IDL mode, its detailed operation is discussed in both the TP3420A Data Sheet, and the Motorola device Data Sheet. For the D-Channel connection, however, its data is shifted out from the TP3420A on BR output rising edge of the BCLK, and shifted into the TP3420A on the TxD input on the falling edge of BCLK. They both occur on the D-Channel timeslot. The RxCLK output generates 2 clock pulses every 125 μs frame (2 D bits per frame) on the assigned D-Channel timeslot. The Motorola uses this as its external clock input to shift D-Channel data in from BR. However, in TEM mode, the number of clock pulses the TxCLK output generates are controlled by the internal D-Channel Access circuitry. They can be 0, 1, or 2 clock pulses. For example, a DREQ1 (DREQ2) command is sent to the TP3420A to begin a packet transmission, the TxCLK starts pulsing (2 BCLKs per frame) and the TP3420A waits for an opening flag on TxD pin. During this time, the TxCLK may stay idle (no pulses at all). It then checks to see if the D-Channel timeslot on the S-Bus is available by counting the consecutive number of binary 1's present the Echoed bit. If these conditions are met, the TP3420A will transmit the packet data by again pulsing the TxCLK until it detects a closing flag at TxD pin or a collision is detected on the S-Bus. Notice that TxCLK and RxCLK phases are inverted from the BCLK's.

Recommended Software Steps:

1. Prepare the Packet for transmission on the D-Channel. Setup the DMA and HDLC registers and start the transmitter. The $\overline{\text{RTS}}$ will become active forcing its own $\overline{\text{CTS}}$ and the HDLC hardware is primed.
2. Send the DREQ1 (or DREQ2) Command to TP3420 via MICROWIRE/SCP port. This will cause TxCLK to generate clock pulses, when D-channel is available, to shift the data out.
3. At the End of successful transmission of Packet. The SID will generate the EOM Interrupt status (serviced via MICROWIRE/SCP port). The software now knows about the successful transmission of the packet and may send the next one. Also the HDLC0 hardware will reset the $\overline{\text{RTS}}$ and thus $\overline{\text{CTS}}$ signals.
4. If a D-channel Contention occurs, the SID will generate a CON interrupt status (serviced via the MICROWIRE/SCP port). The software must Reset the HDLC and DMA hardware and preset the buffer pointers. Note that the $\overline{\text{CTS}}$ does not indicate contention (CON interrupt) in this scheme (as it normally works in a complete Motorola architecture). When the HDLC hardware is set, the $\overline{\text{RTS}}$ goes inactive.

SID can inter-work directly with HDLC controllers from Motorola (MC145488 or the MC68302). This allows the user more flexibility in the choice of Microprocessor while gaining the benefits of good transceiver performance of the TP3420A SID and the programmable features of NSC COMBO II™ TP3076.

FOR NT OR TES APPLICATIONS:

When the TP3420As are used in these applications, the D-Channel Access algorithm is disabled. The 2B + D Channel data can be connected between the TP3420A and the Motorola via the IDL bus. (Other physical interfaces are also possible). The connection diagrams are shown in *Figures 7* and *8*.

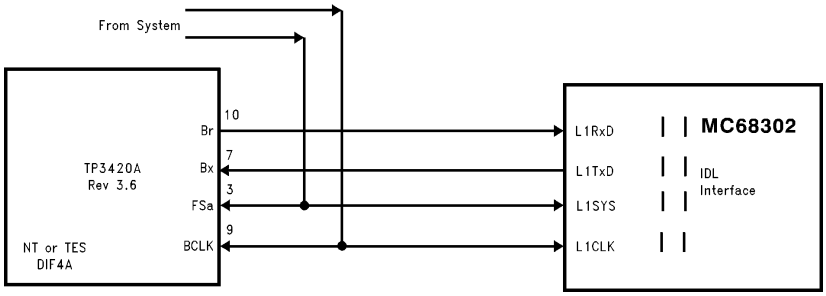

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FIGURE 7. 2B + D Interconnection between the TP3420A (either in NT or TES Mode) and the MC68302

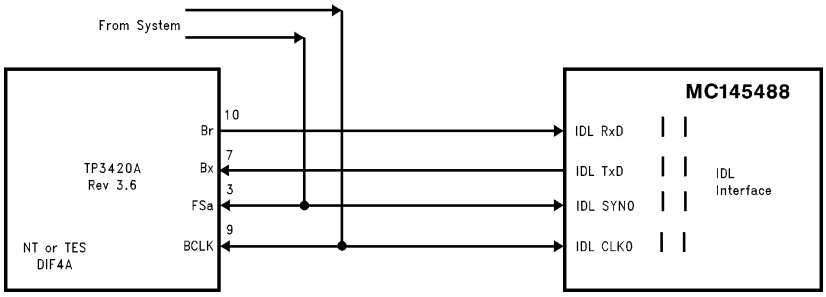

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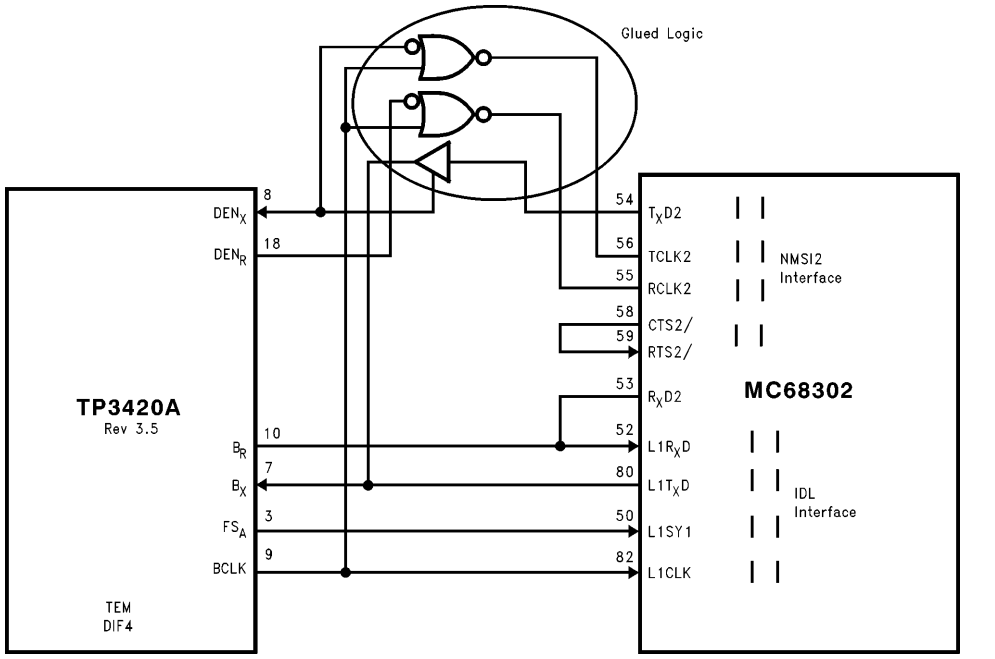
FIGURE 8. 2B + D Interconnection between the TP3420A (either in NT or TES Mode) and the MC145488

APPENDIX A

TP3420A REV 3.5 AND MC68302 INTERCONNECTION



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