

Power-Fail Circuit— Working with NS32FX200

INTRODUCTION

The purpose of the freeze mode is the preserve important information and time indications during a period of power failure. Two kinds of information are saved:

- Important information—saved in the SRAM as long as the back-up battery provides a sufficient voltage level.
- Temporary information (e.g., received fax or voice messages)—saved in the DRAM for a period which is programmable on the NS32FX200.

The Elapsed Time Counter (ETC) operates in the NS32FX200 as long as the back-up battery provides a sufficient voltage level.

GENERAL DESCRIPTION

The power-fail circuit detects failure of the V_{CC} power input. It generates the PWFL signal when V_{CC} falls below 4.75V.

The PWFL signal, activates a Non Maskable Interrupt (NMI), which is transferred to the processor. The software enters an NMI routine that prepares the system for power down (performs all the book-keeping required for recovery). It then enters a delay loop and waits till the PWFL signal is stable (wait time depends on the type of power supply). When the PWFL signal is stable, the software generates a WATCHDOG™ event by writing three times, consecutively, to the WATCHDOG Counter (WDC) of the NS32FX200. This activates the WATCHDOG Trap (WDT) pin which generates a RESET signal to the CPU and the system. The WDT pin remains active as long as PWFL and RST are active.

The PWFL signal is also used to connect a 6V back-up battery (NICAD) to the NS32FX200, SRAM and the DRAM. The NMI routine switches the NS32FX200 to the slow-clock mode, maintaining the ETC and the DRAM refresh. The software programs the Elapsed Time Counter (ETC) of the NS32FX200 to time a predetermined period during which the DRAM is refreshed.

When the ETC expires (reaches zero), the DRAM's refresh is stopped. The RAS1 signal is also used to trigger a retriggerable one-shot whose output disconnects the DRAM from the battery when the refresh is stopped for a long period. The NS32FX200 and the SRAM remain connected to the battery. At this time, only the ETC is active, counting the duration of the power failure. When power returns, the PWFL signal (which indicates power fail to the NS32FX200) is deactivated only after V_{CC} rises above 4.75V. The WATCHDOG remains active until the PWFL signal rises. This keeps the system in reset conditions until the power is stable, and prevents false writing to memory. After the RESET period expires, the WATCHDOG should be reprogrammed by the software. A typical hysteresis of 15 mV is guaranteed by the voltage comparator of the power-fail detector.

The Reset and NMI operations are affected by the power-fail circuit, which should be connected as described below.

RESET AND NMI CIRCUITS

The Reset circuit should generate a RESET signal to the system when:

- Power, V_{CC} is turned on (Power-up Reset).

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- The Reset Switch, or the Remote Reset, is activated.
- The WATCHDOG Counter (WDC) of the NS32FX200 is activated.

The Non Maskable Interrupt circuit should generate an NMI to the system when:

- The NMI Switch, or Remote Reset, is activated.
- Power-fail of V_{CC} is detected.

DETAILED DESCRIPTION

Figure 1 shows the power-fail circuitry.

The LP2951 (U2) is a power-fail detector. When V_{CC} falls below 4.75V (asserted to the SENSE input of LP2951), the PWFL signal is activated. This signal has four functions:

- Transfers the NS32FX200 to freeze mode
- Causes an NMI event to the CPU
- Connects the regulated back-up voltage to the NS32FX200, SRAM and DRAM by ending the "Shut-Down". (The "Shut-Down" condition applies during normal operation according to the SD input of the second LP2951-U1).
- Disconnects the NS32FX200, SRAM and DRAM from V_{CC} by cutting-off transistors Q1 and Q3.

When the 12V power supply is operational, a NICAD battery is charged through diode D1 and resistor R9. In the event of a power failure, the SD input of U1 is low, and the battery provides the power. U1 operates as a controlled 5V regulator, which provides regulated 5V to the NS32FX200, SRAM and DRAM. The diode D1 prevents current flow from the battery to the power supply. A mono-stable circuit (based on Q4 and C5) connects the DRAM to the power supply (through Q2), as long as the refresh mode continues (RAS1 is not continuously low). After a period of time, whose length is programmed on the NS32FX200, the refresh stops (\overline{RAS} and \overline{CAS} remain low), and the power supply to the DRAM is disconnected. Power is supplied to both the NS32FX200 and the SRAM, to maintain the clock and to preserve important information.

DIFFERENCES FROM THE FX164-EDB

In this application, there are two differences from the FX164-EDB:

- The FX164-EDB uses one free inverter (a Darlington pair) of U12 (UA9667). In this application, this is replaced by two transistors (Q5 and Q6), as UA9667 is not used.
- The FX164-EDB uses LP2950 as a 5V regulator. This regulator is smaller than the 5V regulator (LP2951) that is used in this application. The LP2950 is better for high density applications because it is physically smaller. However, while using the LP2950 the voltage from the battery has one drop-out on the LP2951, and one on the LP2950. In this application (using two LP2951s), there is only one drop-out voltage on U1. Each drop-out is about 0.2V @ 10 mA, so the regulated 5V in the FX164-EDB remains till the voltage of the battery decreases to 5.4V. In this application, it remains till the voltage of the battery decreases to 5.2V.

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