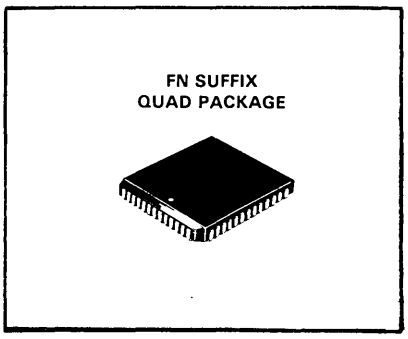
MC68HC99

Product Preview

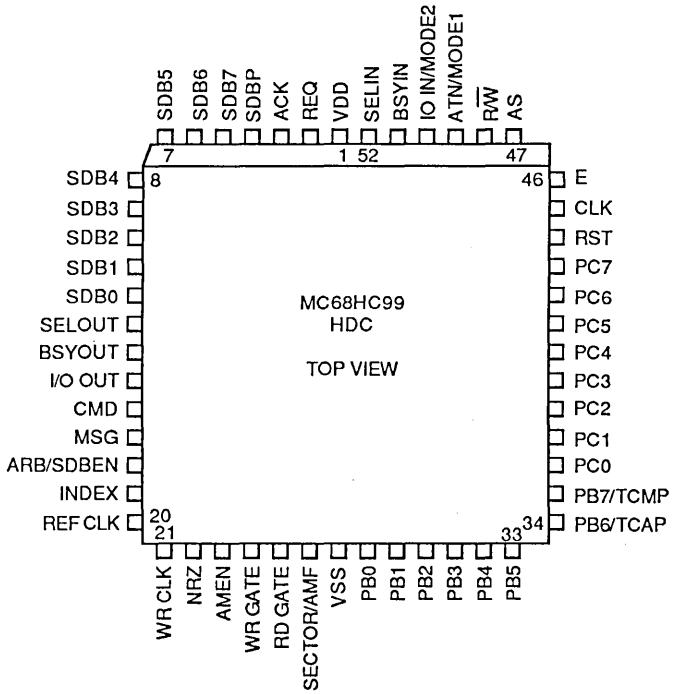
Hard Disk Controller (HDC)



The MC68HC99 hard disk controller (HDC) provides an economical solution to the problem of controlling one or more 3.5 or 5.25 inch hard-disk units. In a single package the HDC contains a host interface, disk interface, rotating data buffers, and error detection and correction circuitry. The host interface is the proposed ANSI X3T9.3 small computer system interface (SCSI) which is compatible with the Shugart Associates system interface (SASI). It supports single or multi-host SCSI systems and bus disconnection and reconnection. Disk interfaces supported are: ST506, 412HP, ESDI step mode, and ESDI serial mode. Two on-chip data buffers provide fast data throughput without the need for sector interleaving. The error detection and correction circuitry is based on Reed-Solomon codes and all detection and correction is done without host system interaction. The HDC also has 12K bytes of mask-programmable ROM which is available for user developed firmware.

- Low Power HCMOS Technology
- SCSI Bus Comaptible
- SCSI Data Bus Parity Programmable
- Two On-Chip 512 Byte Rotating Data Buffers
- Reed-Solomon Error Detection and Correction Circuitry
- MC68HC11 CPU Core with 256 Bytes RAM and 12K Bytes ROM
- 16-Bit Timer with Input Capture and Output Compare Functions
- Four Operating Modes:
  - Single Chip (all Firmware in On-Chip ROM; External Timer Functions)
  - Simple Expanded (for Extral Peripheral Devices)
  - ROM Expanded (for Additional Firmware Space)
  - ROM Expanded with Timer (Adds External Timer Functions)

PIN ASSIGNMENT



PRODUCT DESCRIPTION

Like its board-level equivalents, the HDC (Figure 1) is a microprocessor-based system complete with RAM, ROM, parallel ports, and serial data control circuitry.

The HDC is a modular design built around the core of the MC68HC11 microcomputer. The CPU has two 8-bit accumulators which can be concatenated into one 16-bit accumulator. It also has two 16-bit index registers, a 16-bit stack pointer, a 16-bit program counter, and an 8-bit condition code register. A 256 byte RAM is available as a scratchpad workspace and the first 192 bytes of that RAM are located in page zero memory allowing direct addressing. The 12K byte mask-programmable ROM is used to contain the HDC firmware and interrupt vector table.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

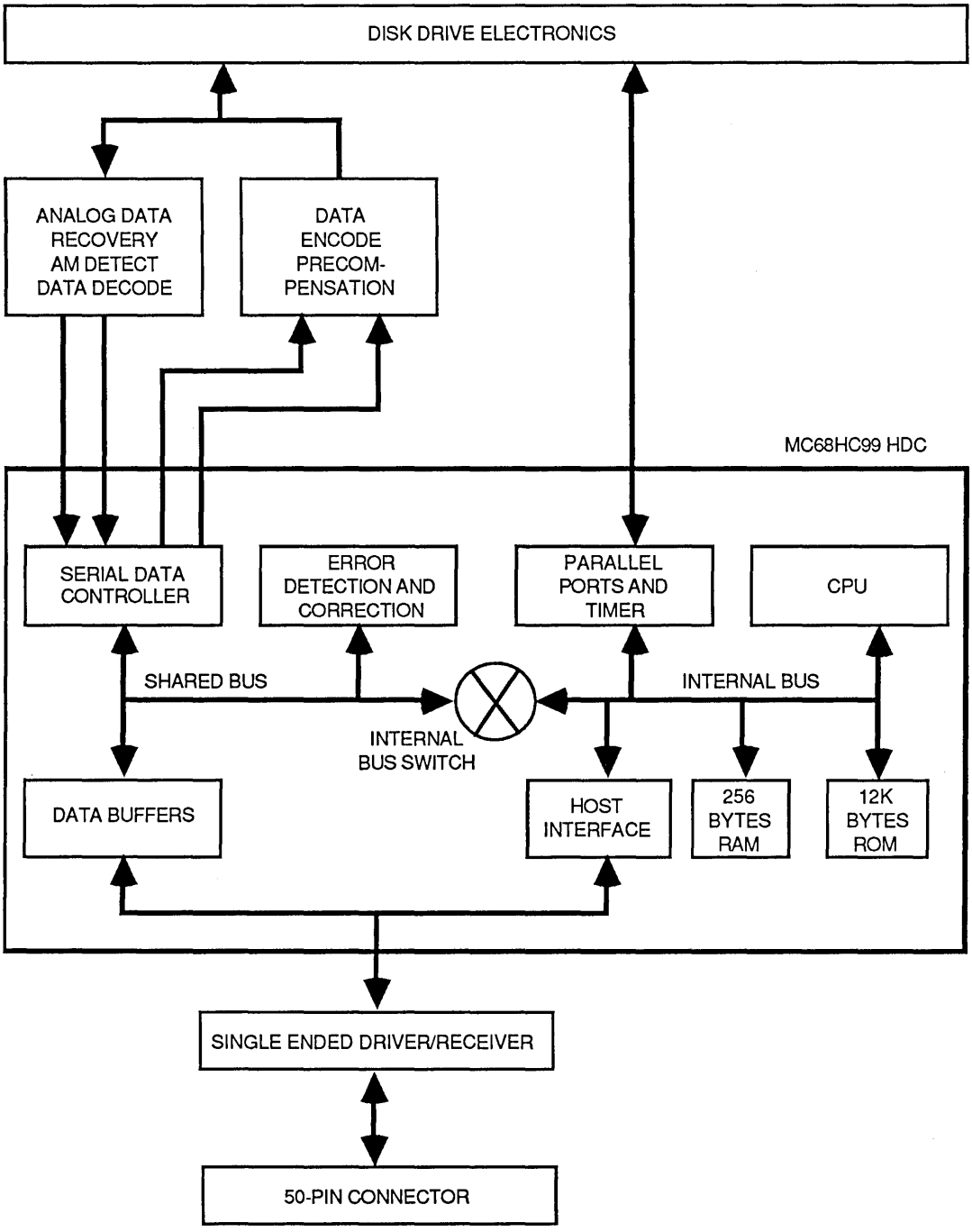


Figure 1. MC68HC99 Hard Disk Controller — Block Diagram

PARALLEL PORTS AND TIMER

There are two 8-bit bidirectional data ports which act as parallel ports in the single-chip operating mode and as the multiplexed address/data bus expansion in the expanded-chip operating modes. A port replacement part, the M68HC24, is available to replace the on-chip parallel ports when the HDC is used in one of the expanded-chip operating modes. The parallel ports are used to manipulate the disk drive control signals (STEP, drive selects, etc.).

The HDC timer is the same timer as is in the MC68HC05C4. It is a 16-bit free running counter, a 16-bit output compare register, and a 16-bit input capture register. The output compare function causes a flag in the status register to be set and the output compare pin to be asserted to a programmable level when the value in the register matches the value of the counter. The input capture function causes a flag to be set in the status register and causes the counter value to be latched in the input capture register when the correct edge (programmable) is detected on the input capture pin. The output compare and input capture functions can be used only when the HDC is in either the single-chip or expanded-ROM with timer operating modes because two of the parallel port pins are used for the output compare and input capture pins.

HDC TO HOST INTERFACE

The host interface of the HDC is a semi-intelligent module that has the capability to detect the various SCSI bus phases such as bus free, select phase, or attention phase and manipulate the SCSI bus under firmware control. It works in all SCSI configurations (single/multiple host, disconnection/reconnection) and it also works in the older SASI single-host bus configuration. The host interface will also work with other interfaces and system buses.

Data Buffers

The two rotating data buffers are large enough to handle sector sizes up to 512 bytes. Because each buffer holds a full sector of data no sector interleaving is required for consecutive sector transfers. The buffers are used to transfer data, commands, status, or messages between the host system and the disk drive unit. Parity is implemented on each buffer to assure data integrity between the host and the disk drive unit.

Serial Data Controller

The serial data controller is a highly sophisticated, programmable module that allows the HDC to handle the ST506, HP412, and ESDI disk interfaces. Data formats are fully programmable and allow for ESDI soft- and fixed-sectored as well as ST506 formats. An external data separator is necessary to provide the HDC with NRZ data. Data read and write operations, format operations, and compare operations can be performed. All operations are done on a track-by-track basis. Placing the HDC directly on the hard-disk drive unit can make data transfer rates of up to 24 MHz possible.

Error Detection and Correction Circuitry

The HDC uses an interleaved Reed-Solomon code to detect and correct errors in the data field. It operates on symbols one byte at a time, rather than one bit at a time, and three check bytes are used per interleave. This gives the code the capability to correct any single byte error in each interleave. The HDC can also correct a single burst error per record. If errors occur in multiple interleaves, the error locations must be contiguous for the correction to occur. Restricting the correction to a single burst significantly reduces the probability of miscorrecting an error that is bigger than the code's detection capability. Table 1 summarizes the error correcting circuitry parameters.

Table 1. Error Correcting Parameters

Interleave/ ECC Field Size	1/3	2/6	3/9	5/15
Single Burst Detect (Bits)	9	17	41	73
Single Burst Correct (Bits)	*	9	17	33
Double Burst Detect (Bits)	1	9	17	33

*Interleave of 1 is used for header field protection – no correction is attempted.

When an error is detected data transfer is halted and the on-chip CPU is notified of the error. This CPU can interrogate the error detection circuitry to determine the type of error and get the information needed to correct the data in the data buffer.

OPERATING MODES

The HDC can be configured to work in four different operating modes: single chip, simple expanded, ROM expanded, and ROM expanded with timer. The operating mode is established at reset by the levels on the ATN/MODE1 and I/O IN/MODE2 pins. Also determined at reset are the HDC's SCSI bus ID and parity.

Single Chip

When the HDC is configured in the single chip operating mode all resources are on the chip. The vector table and firmware are completely contained in the 12K byte ROM and parallel ports B and C are active. If the timer input capture and output compare functions are enabled (under firmware control) then port B, bits 7 and 6 are used as TCMP and TCAP, respectively.

Simple Expanded

When the HDC is configured in the simple extended operating mode *most* of the resources are on the chip. This operating mode is used when the internal 12K byte ROM is large enough to contain the firmware, but additional RAM, parallel ports, or other peripheral devices are needed. In this mode, the parallel port pins are used as a multiplexed address and data bus for bus expansion. The vector table is the same as in the single-chip operating mode. The timer input capture and output compare functions cannot be used in this mode.

ROM Expanded

When the HDC is configured in the ROM expanded operating mode the vector table and ROM are external to the HDC. The internal 12K byte ROM remains accessible unless removed from the memory map (giving more external ROM space) by the firmware. In this operating mode, the parallel port pins are used as a multiplexed address and data bus for bus expansion. The timer input capture and output compare functions cannot be used in this mode.

ROM Expanded with Timer

When the HDC is configured in the ROM expanded with timer operating mode it functions the same as the ROM expanded operating mode except that the timer input capture and output comare functions are useable. TCMP and TCAP are multiplexed with address pins A15 and A14 respectively.

FIRMWARE

Motorola will provide firmware in the HDC which will work with ST506, 412HP, ESDI step mode, and ESDI serial mode disk drive units. This firmware is released to the public domain for companies wishing to use it for a base part. All required SCSI commands are implemented.

The Motorola firmware has the necessary "hooks" to allow expansion of the command set externally when either of the ROM expanded operating modes are used. The firmware will control only one hard-disk drive unit.

Another feature of the Motorola firmware is its ability to handle alternate and defective sectors and tracks. Error

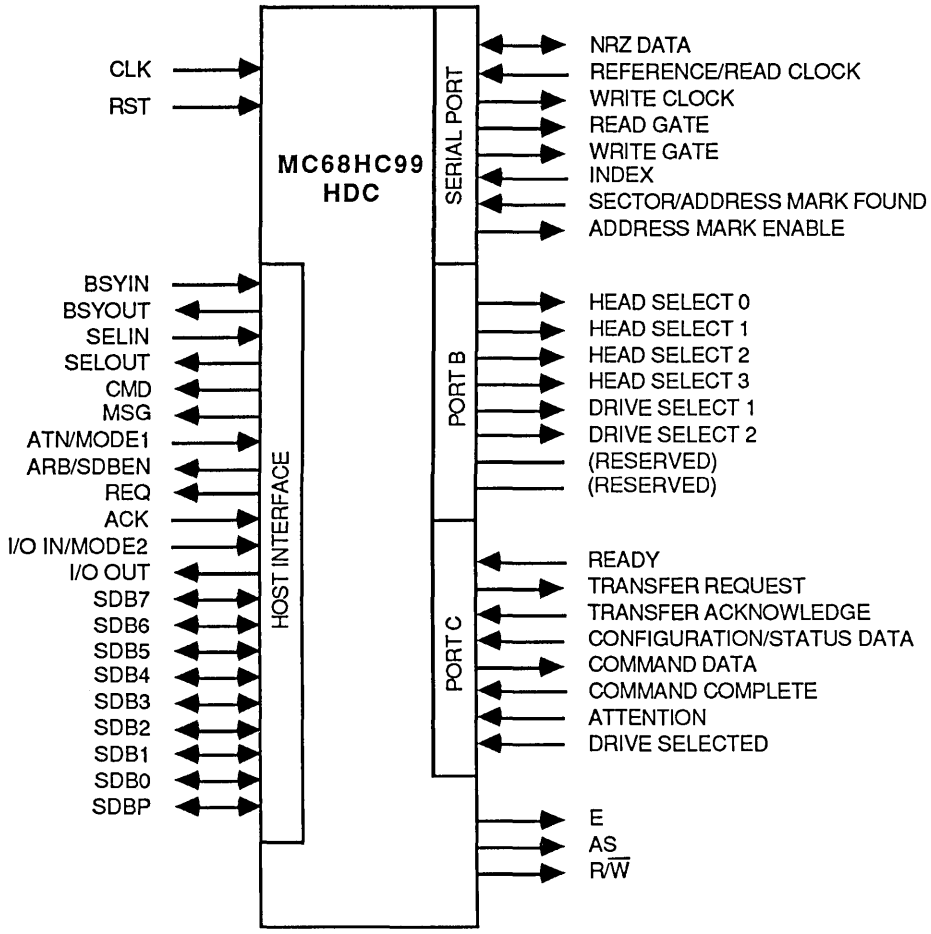


Figure 2. HDC as an ESDI Serial Mode Controller with SCSI Interface

correction on read operations is programmable to allow multiple attempts at reading a bad sector before resorting to correction and whether the host will be notified about the error.

PACKAGING AND PINOUT

The HDC will be available in a 52-lead quad pack. The basic pinout is given on the front page of this document. Figure 2 shows the HDC as an ESDI serial mode controller and Figure 3 shows the HDC as an ST506/412HP/ESDI step mode controller.

TYPICAL HARD DISK CONTROLLER SYSTEM

In the current hard-disk-drive controller market the available controllers are board-level products, most of which are microprocessor based with RAM, ROM, parallel port, and serial data controller circuits. Most are able to control two to four disk drive units; some are also able to control floppy-disk drive units as well. Figure 4 illustrates a typical computer system with a host, one disk controller, and two hard-disk drives. This sytem requires one 50-pin ribbon cable (plus driver/receiver circuits) to connect the disk controller to the host. It also requires two 20- and one 34-pin ribbon cables (plus driver/receiver circuits) for the data and control connections between the disk controller and the disk drive units. Additionally the disk controller needs a medium-duty power supply.

MC68HC99 HDC SYSTEMS

Computer systems based on the HDC typically will control only one hard-disk drive unit and can place the disk controller directly on the disk drive unit. Figure 5 illustrates the same system configuration as shown in Figure 4 but using two HDCs. This configuration removes the need for (and reduces the cost of) the data and controller cables (plus the associated driver/receiver circuits) and reduces the power supply requirements. The HDC can also replace the microprocessor on the drive unit because the MC68HC99 CPU can operate concurretly with the serial data functions.

It is also possible to use the HDC separately from the disk drive unit. Figure 6 illustrates a system configuration wherein the HDC is place on a separate controller board, possibly with external ROM, RAM, and/or other periphral devices. Figure 7 illustrates a system where the HDC is mounted in the host system with a bus adapter.

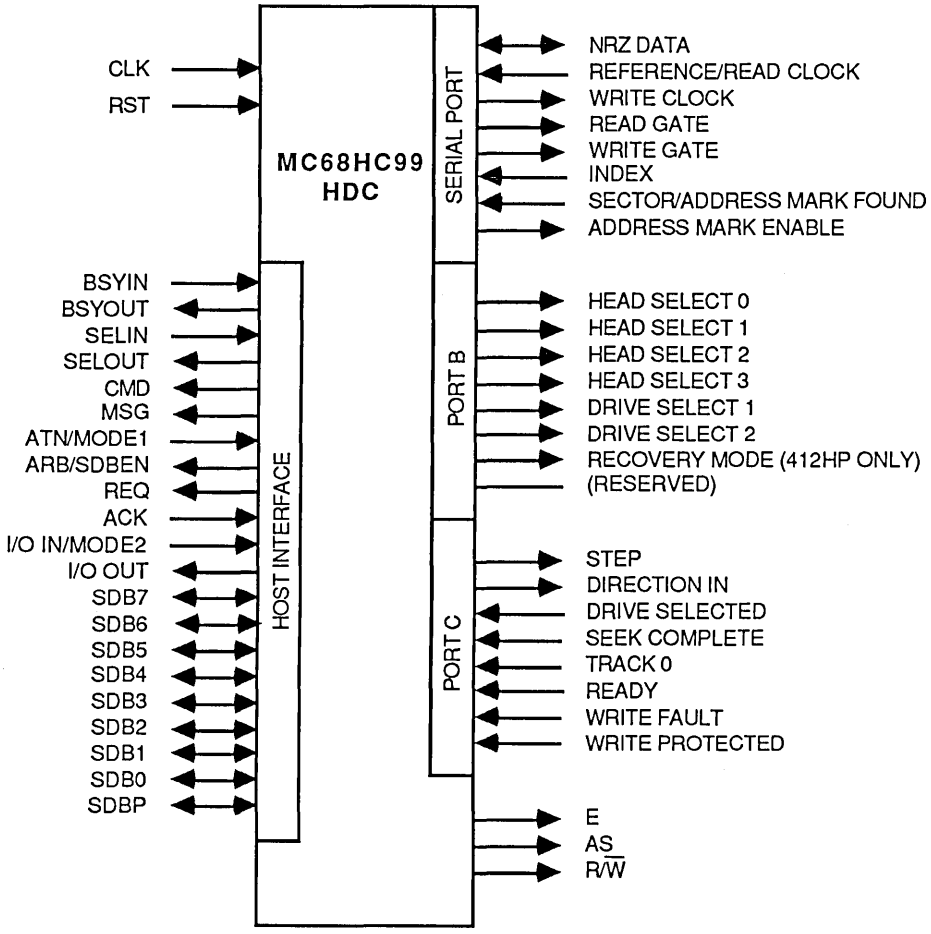


Figure 3. HDC as an ST506/412HP/ESDI Step Controller with SCSI Interface

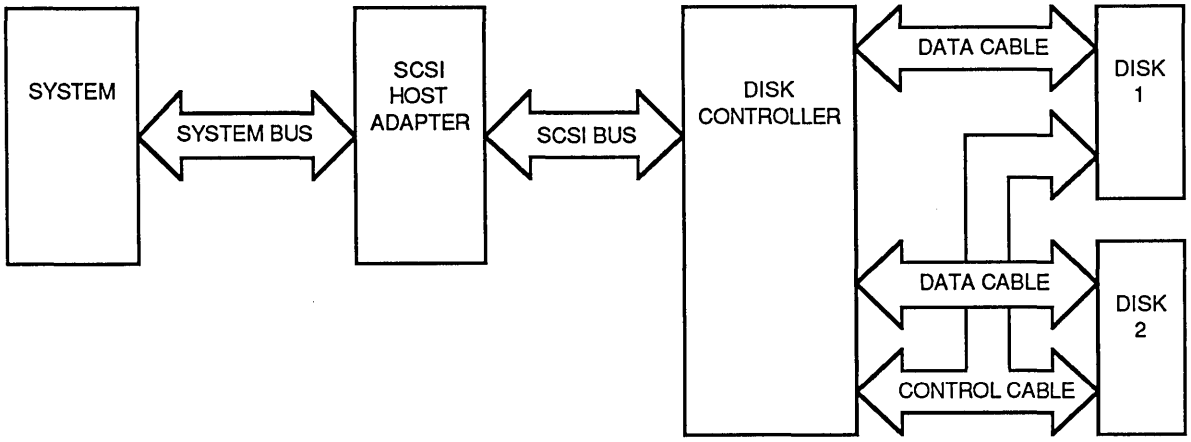


Figure 4. Typical Hard Disk System

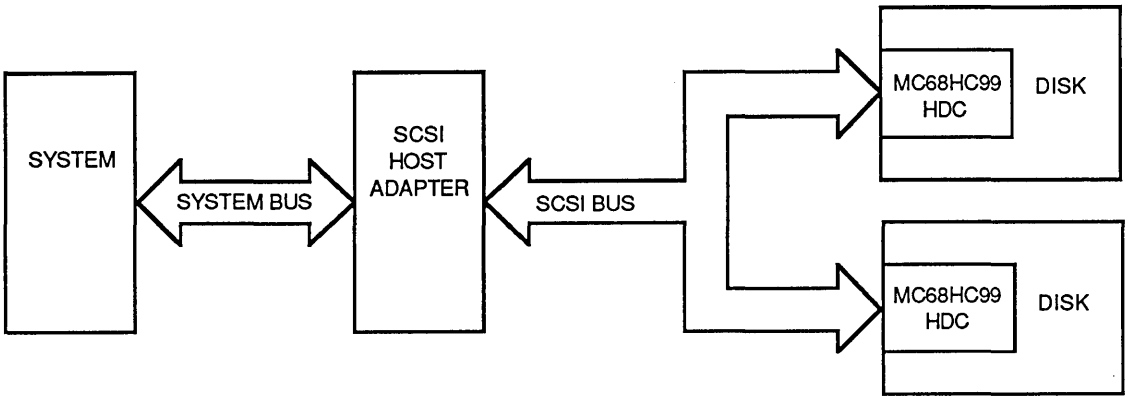


Figure 5. MC68HC99 HDC Configuration — Option 1

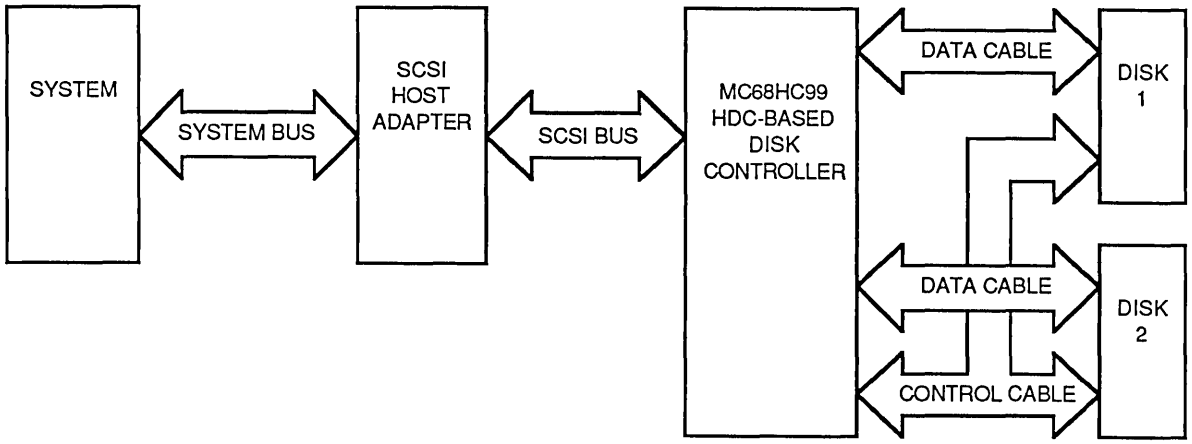


Figure 6. MC68HC99 HDC Configuration — Option 2

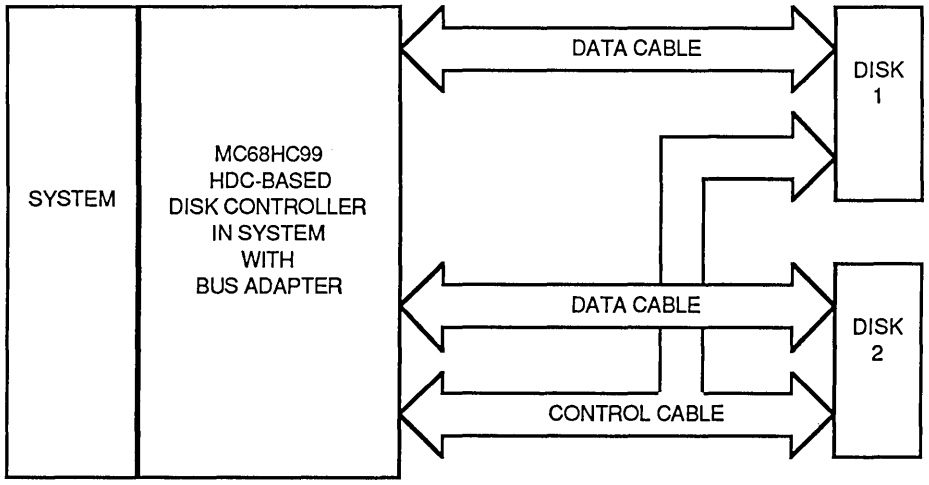
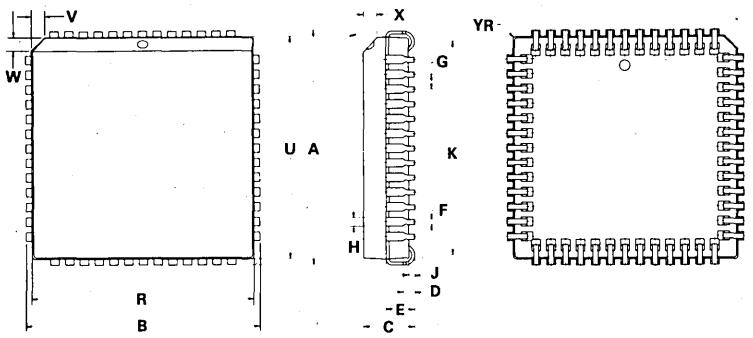


Figure 7. MC68HC99 HDC Configuration — Option 3

MECHANICAL DATA

FN SUFFIX
QUAD PACK
CASE 778-01



NOTES:
1. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: INCH

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	19.94	20.19	0.785	0.795
B	19.94	20.19	0.785	0.795
C	4.19	4.57	0.165	0.180
D	0.64	1.01	0.025	0.040
E	2.16	2.79	0.085	0.110
F	0.33	0.53	0.013	0.021
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.38	0.63	0.015	0.025
K	17.52	18.54	0.690	0.730
R	19.05	19.20	0.750	0.756
U	19.05	19.20	0.750	0.756
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	0.00	0.50	0.000	0.020

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