MOTOROLA
Semiconductor Products Inc.

AN-844
Application Note

EXTENDING THE CAPABILITIES OF THE MC10315/10317 FLASH A-D CONVERTERS

INTRODUCTION

The parallel flash A-D converter, while simple in concept and principle of operation, has until recently defied the capability of the manufacturing world to be produced in monolithic form. The reasons are obvious upon inspecting the analog section of such a device — the number of comparators and reference points increases exponentially with the number of bits resolution. (The number is equal to $2^n - 1$). Placing this large number of functional blocks on a chip is not the challenge, (microprocessor chips contain **thousands** of functional blocks) but rather it is the fact that the operation of each of the comparators must be matched to a very tight tolerance. The cumulative errors of the reference voltage, comparator offset, common mode rejection, bandwidth, and propagation delay cannot exceed ½LSB over time, temperature, power supply variations, and frequency.

Recent advances in manufacturing capabilities have provided the means to produce 7-bit flash converters in monolithic form. This Application Note will discuss some of the means whereby the user may extend the resolution and speed of the basic devices.

COMPONENT DESCRIPTION

The MC10315 and MC10317 are 7-bit flash A-D converters, with accuracy in excess of 7 bits, whose operation differ only in the overrange function. In the MC10315, the outputs remain high (Logic "1") when an overrange condition is reached, whereas in the MC10317 the outputs switch to low (Logic "0") on reaching an overrange condition. This difference is necessary in order to be able to parallel devices into configurations with greater than 7-bit resolution.

The digital output of a flash converter is determined by comparing the analog input to a voltage on a resistor divider reference network. The digital outputs are Logic "0" when the analog input is within ½LSB of the most negative reference voltage (V_{RB}), or less. The outputs are at a Logic "1" when the input is within 1½LSB to ½LSB below the most positive reference voltage (V_{RT}). In between these values are the remaining 126 possible binary codes. When the input exceeds V_{RT} – ½LSB, the overrange output is high. The reference span (V_{RT} – V_{RB}) is to be between 1.0 and 2.0 volts, within an absolute voltage range of +2.0 to –2.0 volts.

The Flash converter requires a clock input. When the clock is high, the 128 input comparators are latched (effectively a sample-and-hold function), allowing the subsequent logic to decode their outputs into a 7-bit binary code, plus overrange. During this time, the output latches are transparent, and the output data is not stable for the first (approximate) 43 ns. When the clock goes low the outputs are latched, and the comparators resume tracking the input signal. See Figure 2. Maximum guaranteed clock (sampling) frequency is 14.5 MHz, with the requirement that the clock be low 25 ns (min) and high for 44 ns (min). Frequencies less than 11.3 MHz may have a symmetrical clock signal.

The outputs and Clock signal are ECL compatible, the outputs therefore requiring pull-down resistors. The analog input impedance is minimum 5.0 kΩ in parallel with a variable capacitance of 40 to 70 pF (C_{in} = 40 pF @ A_{in} = V_{RB}; C_{in} = 70 pF @ A_{in} = V_{RT}) See Below. The input signal (A_{in}) may be unipolar or bipolar.

The reference resistor ladder has a typical impedance of 64 ohms (0.5 ohm per resistor) resulting in a reference current of 31 mA (when V_{RT} – V_{RB} = 2.0 V).

$$C_{in} = \left[\frac{30\ pF}{(V_{RT} - V_{RB})} \times (A_{in} - V_{RB})\right] + 40\ pF$$

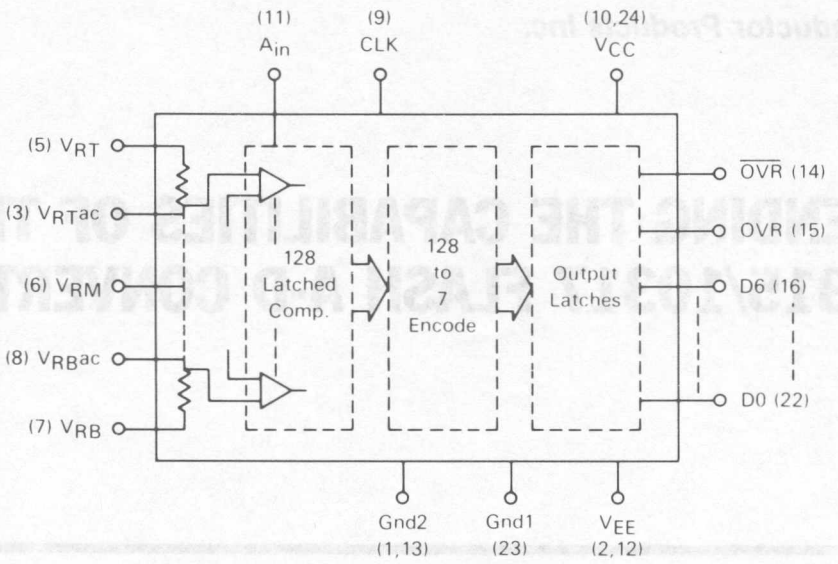
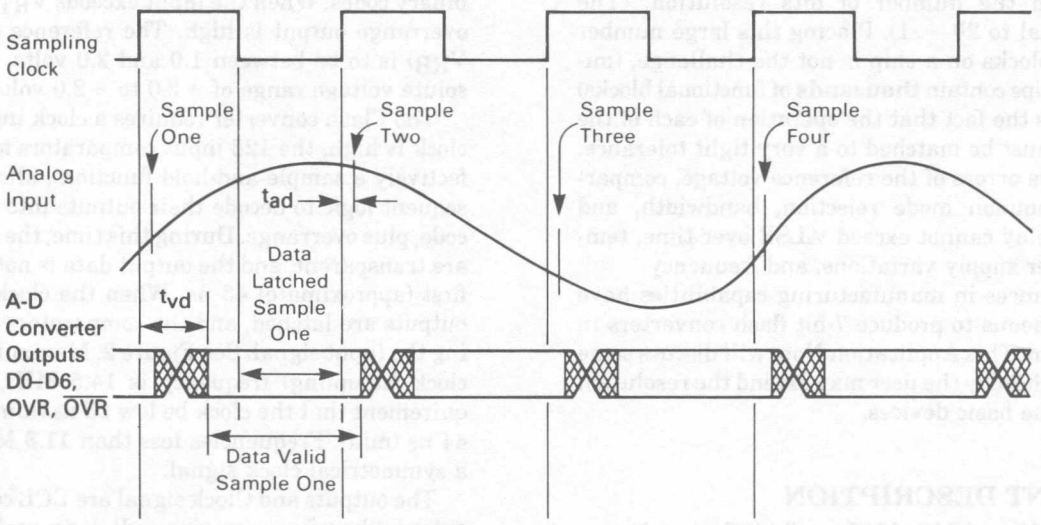


FIGURE 1. — Block Diagram



NOTES: t_{ad} = APERTURE DELAY TIME – 3.0 ns TYP
t_{vd} = DATA VALID DELAY TIME – 43 ns MAX
CLOCK RISE AND FALL TIME < 7.0 ns

FIGURE 2. — A-D Conversion Timing

8-BIT A-D SYSTEM

Figure 3 shows the manner in which two flash converters may be configured to produce 8-bits of resolution. The reference ladders are connected in series in order to provide the 256 thresholds required. The analog input (A_{in}) is applied to both devices simultaneously, but actually only one device will be active at any instant. The outputs are wired-OR as shown, with the Overrange output of the MC10317 becoming the MSB. Operation is as follows:

- When A_{in} is equal to, or below, V_{RB} of the MC10317, D7–D0 will be at Logic "0".
- When A_{in} is between V_{RB} and (V_{RT} – ½LSB) of the MC10317, D7 will be Logic "0", and D6–D0 will be at a binary value representative of A_{in}.
- When A_{in} is at V_{RT} of the MC10317 (mid-point of the total reference span), D7 will be at a Logic "1", and D6–D0 will switch to Logic "0".
- When A_{in} is between V_{RB} and (V_{RT} – ½LSB) of the MC10315, D7 will remain at a Logic "1", and D6–D0 of the MC10315 will provide the binary value representative of A_{in}.
- When A_{in} reaches or exceeds V_{RT} – ½LSB of the MC10315, the OVR output and D7–D0 will be at Logic "1".

An advantage available with the MC10315/MC10317 combination is that the reference span for **each** device can be set at the maximum of 2.0 Volts (total span = 4.0 volts), thus maintaining a 15.6 mV quantitization step, which in turn, provides for maximum accuracy and performance. The mid-point of the total reference ladder (@ V_{RB} of the MC10315) is shown connected to the reference supply for adjustment to the exact midpoint voltage required. Due to the ±20% tolerance of the total resistor value in each device, simply connecting them in series cannot assure equal voltage span for each device. If the total reference span is to be symmetrically bipolar (e.g., ±2.0 volts), the midpoint can be connected to ground.

The input signal (A_{in}) will have to drive a load of approximately 2.5 kΩ in parallel with 140 pF (max). At the maximum allowable slew rate of 50 V/μs (e.g., 4.0 V p-p sinewave @ 4.0 MHz), maximum input current will be ≈7.0 mA.

If the 8-bit system is to be operated at or near the maximum sampling rate, slight timing differences (aperture delay difference) between the two devices may cause a small amount of error noticeable when A_{in} crosses the midpoint of the reference span. If this is of concern to the user, the clock signal to one device would have to be adjusted in time (<0.1 ns) to compensate for the difference.

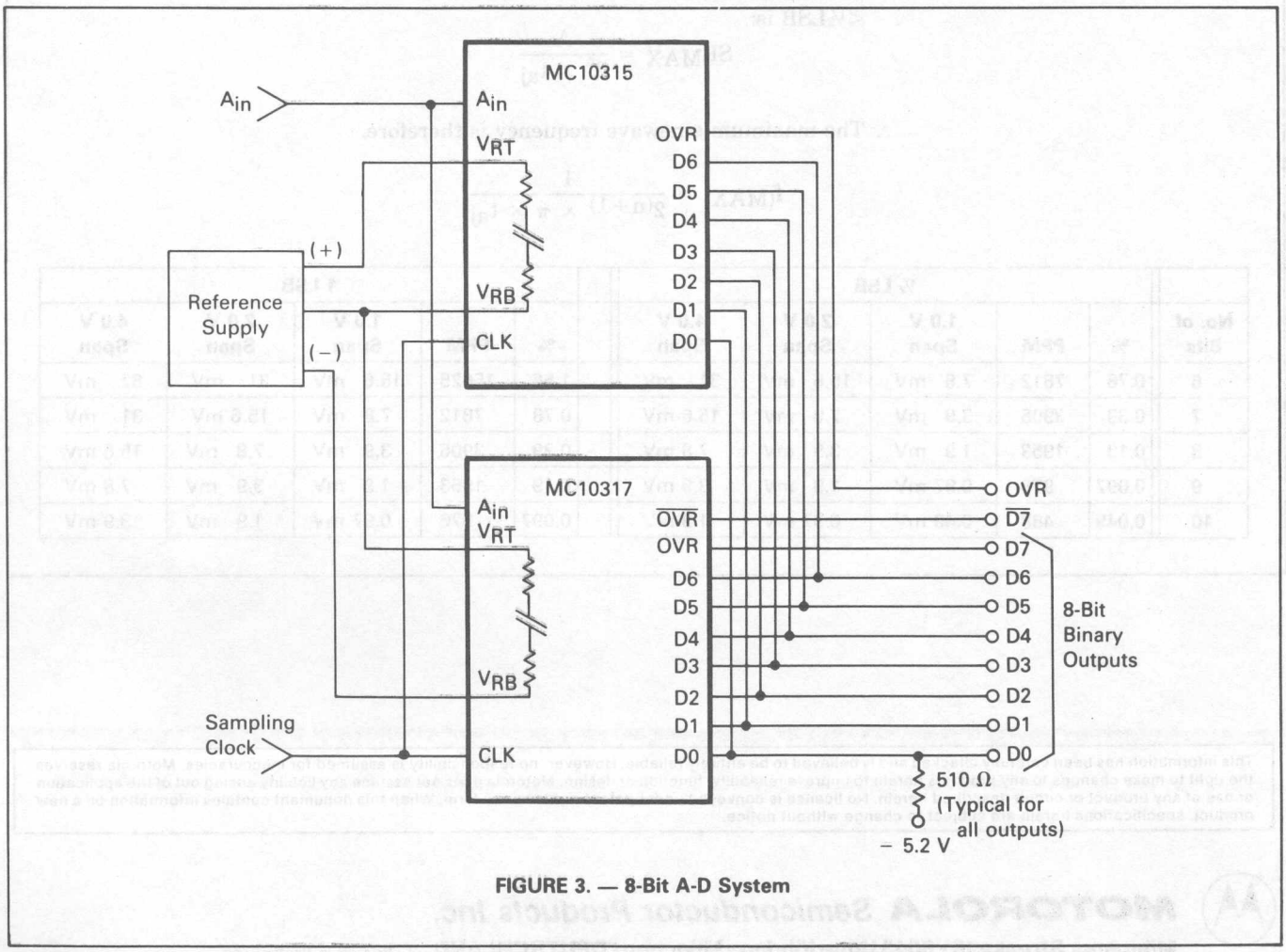


FIGURE 3. — 8-Bit A-D System

9-BIT A-D SYSTEM

Figure 4 is an extension of the 8-bit system, described previously, designed to provide 9 bits of resolution. The system consists of one MC10315 and three MC10317's, and one MC10102 NOR gate, wired as shown. The reference ladders are connected in series in order to provide the 512 thresholds required. The analog input (A_{in}) is applied to all devices simultaneously, but actually only one device will be active at any one instant. The outputs are wired-OR as shown, with the Overrange outputs of the lower 3 devices providing the 2 MSB's. When A_{in} is equal to (or below) V_{RB} of the lowest MC10317, all of the outputs will be at a Logic "0". As A_{in} varies through the four reference spans, the binary equivalent will be produced at D8–D0. When A_{in} exceeds V_{RT} – ½LSB of the MC10315, the OVR output, as well as D8–D0, will be at a Logic "1".

Since the maximum absolute voltages which can be applied to any reference input are +2.0 and −2.0 volts, each device (in this configuration) will have 1.0 volt across its reference ladder. V_{RT} of the MC10315 will be set at +2.0 volts, and V_{RB} of the lowest MC10317 will be set at −2.0 volts. 1.0 LSB will be equal to 7.8 mV. As explained in the 8-Bit System, each V_{RB}-to-V_{RT} jumper (between adjacent devices) is shown wired to the reference supply in order that they may be adjusted to the exact values required.

The input signal (A_{in}) will have to drive a load of approximately 1.25 kΩ in parallel with 280 pF (maximum). At the maximum allowable slew rate of 50 V/μs (e.g., 4.0 V p-p sinewave @ 4.0 MHz), maximum input current will be ≈14 mA.

Due to the propagation delay of the NOR gate, D7 will have a slight timing difference from the other bits. If this poses a problem to the user, external latches can be used, wired to latch on the positive edge of the sampling clock signal.

If the 9-bit system is to be operated at or near the maximum sampling rate, slight timing differences (aperture delay difference) between the devices may cause a small amount of error noticeable when A_{in} reaches a value equal to the V_{RB}/V_{RT} junction of two adjacent devices. If this is of concern to the user, timing of the clock signal to each device would have to be adjusted, as necessary, to compensate for the difference.

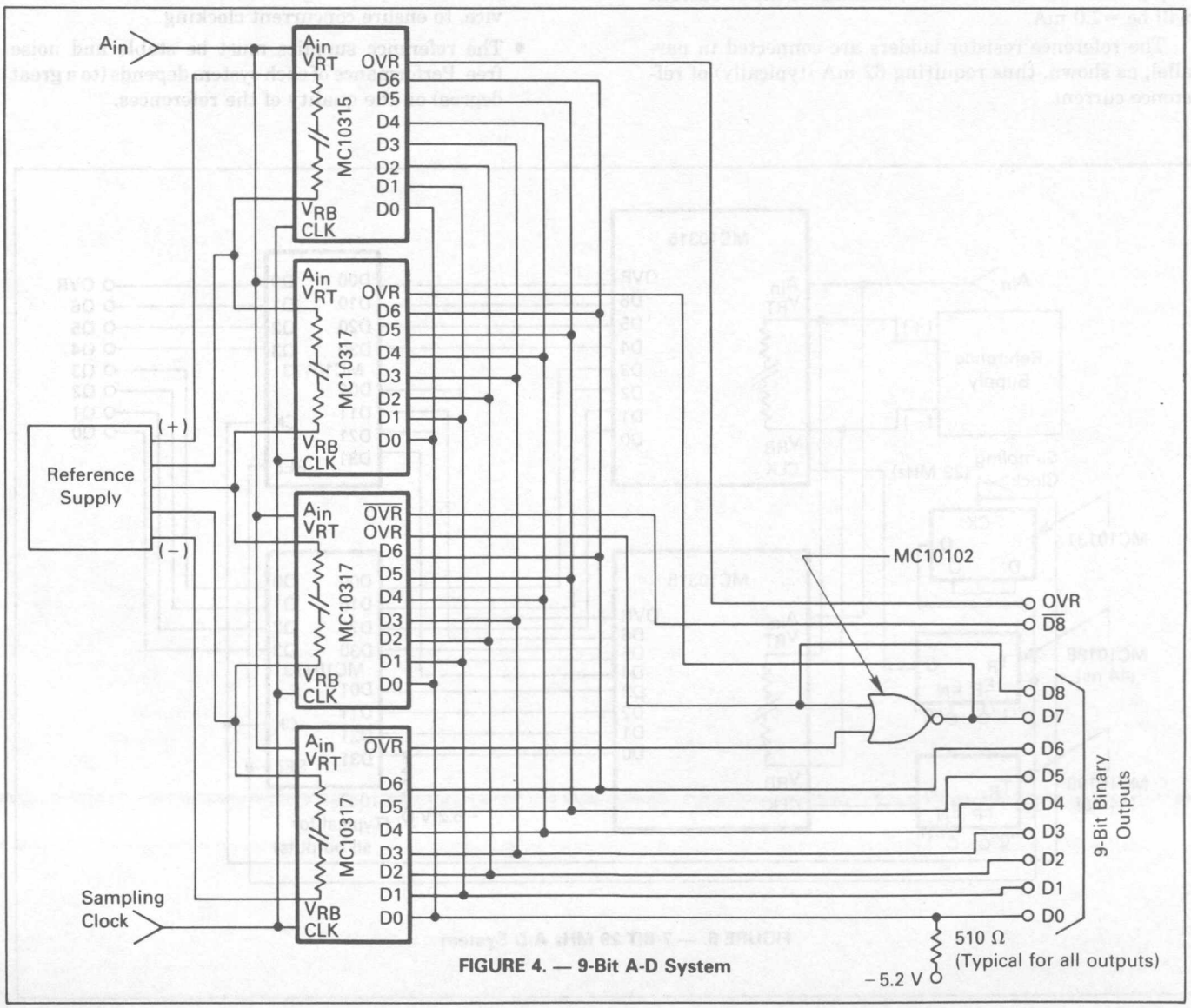


FIGURE 4. — 9-Bit A-D System

7-BIT, 29 MHz A-D SYSTEM

Although the maximum guaranteed sampling rate of the MC10315 (and MC10317) is 14.5 MHz, a higher sampling rate can be obtained by configuring two devices into a Flip-Flop operation. Figure 5 illustrates the necessary circuitry. While the two A-D converters are basically wired in parallel, their operation is such that while one is sampling A_{in}, the other is outputting data.

At maximum frequency, the clock signal to each converter must be 44 ns high (min), and 25 ns low (min). The 14.5 MHz output of the MC10131 (D-Type F/F) triggers the MC10198 One-Shot's to produce a 44 ns high clock pulse once every 69 ns. The MC10198 for the upper MC10135 triggers on the positive edge, while the other MC10198 triggers on the negative edge. Thus the A-D converters are clocked at a 14.5 MHz rate each, while the MC10173's, which provide the multiplexing and latching functions, are toggled at 29 MHz. Thus the outputs of the two converters are alternately presented as Q6–Q0, and OVR, at a 29 MHz update rate.

The analog signal input (A_{in}) will have to drive a load of approximately 2.5 kΩ in parallel with 140 pF (max.) At a maximum allowable slew rate of 50 V/μs (e.g., 2.0 V p-p sinewave @ 8.0 MHz), maximum input current will be ≈7.0 mA.

The reference resistor ladders are connected in parallel, as shown, thus requiring 62 mA (typically) of reference current.

MISCELLANEOUS

The schematics are shown simplified for clarity's sake. The following points, however, must be observed when constructing any of the circuits discussed:

- The MC10315 and MC10317 have two pins for V_{CC} (+5.0 V), two pins for V_{EE} (−5.2 V), and two pins for Gnd2. Both pins in each case must be connected to the appropriate voltage for optimum performance. Leaving either pin of a pair open will result in undesirable internal IR losses.
- PC board layout should keep the analog and digital grounds separate up to the power supplies. Gnd1 should be connected to the digital ground, and Gnd2 to the analog ground.
- Bypass capacitors (0.1 μF) should be provided at all power supply pins, reference input pins, and at $V_{RB}ac$ and $V_{RT}ac$ (Pins 3 and 8).
- Pull-down resistors must be provided at all ECL outputs, physically located at the receiving end of the interconnection. Recommended values are 510 ohms to −5.2 V, or 51 ohms to −2.0 V.
- The PC board traces for the sampling clock signal should be equal length from the source to each device, to ensure concurrent clocking.
- The reference supplies must be stable and noise free. Performance of each system depends (to a great degree) on the quality of the references.

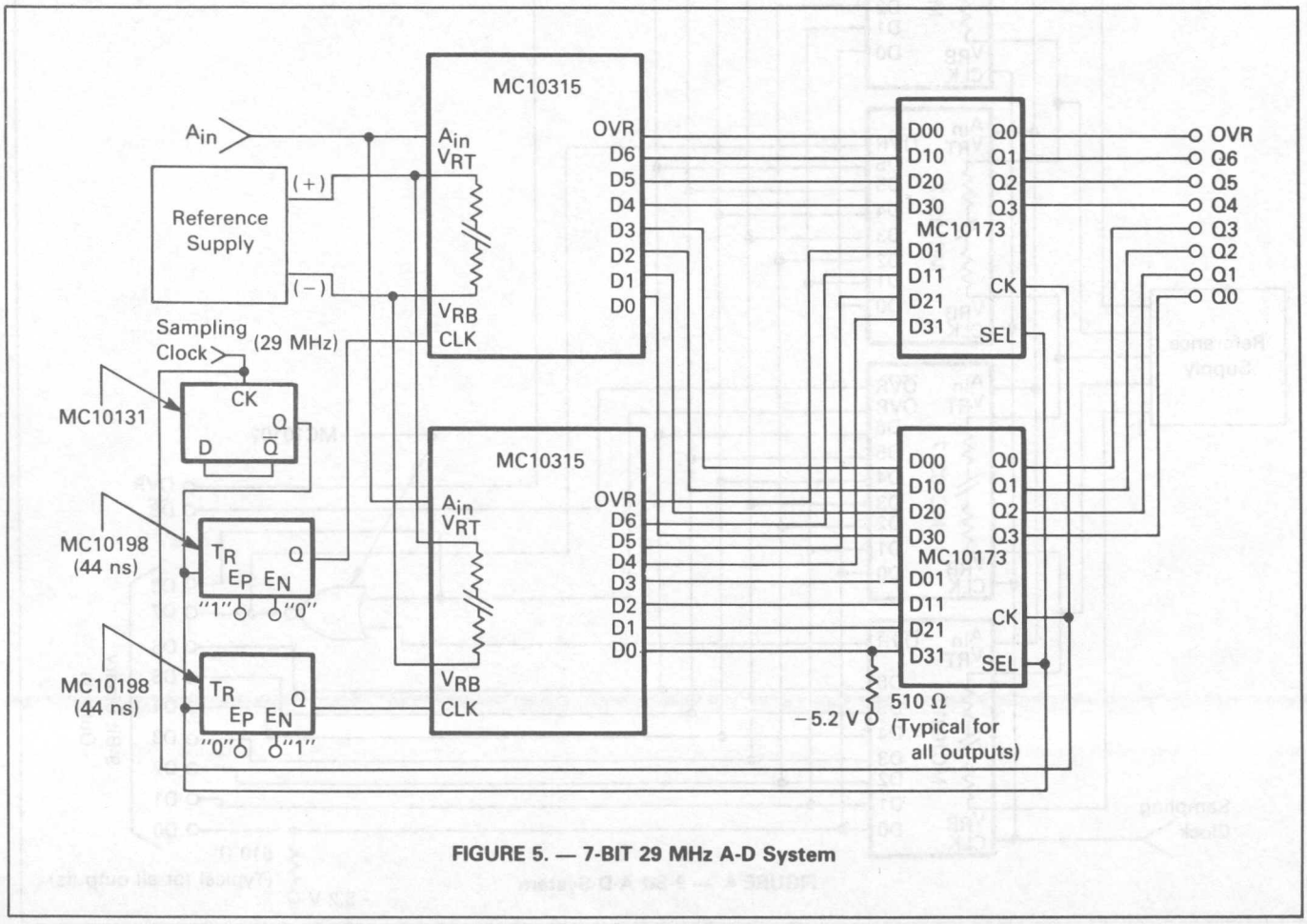


FIGURE 5. — 7-BIT 29 MHz A-D System

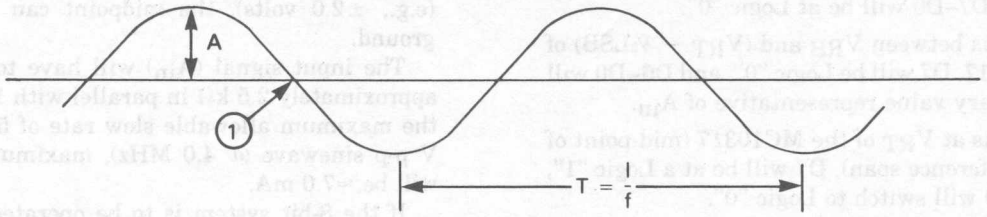
- The reader should refer to the MECL System Design Handbook, the appropriate data sheets, and AN-848, for further details.

CONCLUSION

The MC10315 and MC10317 flash A-D converters provide a parallel conversion which is simple and straightforward in principle. The bipolar input, adjustable reference points, and uncommitted ECL outputs permit a wide degree of flexibility in their implementation. Possible applications include radar and video digitizing, time base correction, random number generation (using a white noise source at A_{in}), one-step amplitude modulation and digitizing, and others.

APPENDIX

Equations and information applicable to flash A-D converters are presented here:



For a sine wave of amplitude A and frequency f:

- $V = A \sin (2 \pi ft)$
- Max slew rate $= 2 \pi fA$ at point ①.
- 1 LSB $= \frac{A}{2^{(n-1)}}$ (n = no. of bits resolution)
- When aperture jitter (t_{aj}) of a flash converter is known, maximum slew rate for an error of <½LSB is:

$$SR_{MAX} = \frac{A}{2^n \times t_{aj}}$$

∴ The maximum sinewave frequency is therefore:

$$f_{(MAX)} = \frac{1}{2^{(n+1)} \times \pi \times t_{aj}}$$

	½ LSB					1 LSB				
No. of Bits	%	PPM	1.0 V Span	2.0 V Span	4.0 V Span	%	PPM	1.0 V Span	2.0 V Span	4.0 V Span
6	0.78	7812	7.8 mV	15.6 mV	31 mV	1.56	15625	15.6 mV	31 mV	62 mV
7	0.39	3906	3.9 mV	7.8 mV	15.6 mV	0.78	7812	7.8 mV	15.6 mV	31 mV
8	0.19	1953	1.9 mV	3.9 mV	7.8 mV	0.39	3906	3.9 mV	7.8 mV	15.6 mV
9	0.097	976	0.97 mV	1.9 mV	3.9 mV	0.19	1953	1.9 mV	3.9 mV	7.8 mV
10	0.049	488	0.49 mV	0.97 mV	1.9 mV	0.097	976	0.97 mV	1.9 mV	3.9 mV

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