



COLOR GRAPHICS FOR THE MC68000 USING THE MC6847

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Color graphics can be a valuable addition to a variety of MC68000 applications. Typically, color graphics circuits are expensive and complicated. These same color graphics circuits generally have limited capabilities and are very hardware intensive. The MC6847 Video Display Generator (VDG) offers a low cost, versatile, easy to use alternative.

The VDG creates a composite video signal according to information read from the display memory in the mode defined by the VDG control pins. The composite video signal can be used to modulate the input of any commercially available color or black and white television receiver. The VDG has 12 distinct display modes available and allows certain variations within certain modes. All display modes and their variations are controlled by the state of eight different VDG pins. The eight display mode pins give the user the ability to combine display modes within a single display frame, e.g., alphanumeric and a compatible graphics mode.

The 16-bit data bus of the MC68000 can be used to give the user full control of all VDG display modes on-the-fly. This additional control over the VDG display modes, combined with the ability of the MC68000 to manipulate data through its extended arithmetic capabilities and its ability to move blocks of data quickly and efficiently, gives the user the capability to monitor and display changing data quickly and efficiently as might be necessary in commercial, industrial, or scientific applications. The MC68000/MC6847 interface described in this application note, or a variation of it, could be used in a typical application.

BASIC IMPLEMENTATION

Since the display information for the VDG is stored in memory, the MC68000 can alter the display by changing the contents of that memory. The MC68000/MC6847 interface then becomes a shared-memory interface. The primary problem then becomes a matter of guaranteeing that memory is accessed by only one device at a time. Figure 1 is a block diagram of the MC68000/MC6847 interface.

The MC68000 is buffered from the display memory by three-state buffers and transceivers which are active only during a processor access of display memory. During a processor access, the VDG address bus is forced to a high-

impedance state. Display memory is only 12 bits wide, and a 4-bit latch is used to capture data for some of the VDG control pins. Not all of the VDG display modes may be used in the same frame without some additional attention by the user; however, the latch could be replaced with an additional 6K by 4 bits of memory. A data transfer acknowledge (DTACK) signal is generated so that either fast or slow memory can be efficiently used.

CIRCUIT DESCRIPTION

A schematic diagram of the MC68000/MC6847 interface is given in Figure 2. The select circuitry is formed around two SN74LS138 1-of-8 decoders. If the MC68000 accesses any of the 6K of memory, pin 8 of the SN74LS21 outputs a signal which switches the display memory bus from the VDG to the MC68000. First, the VDG address bus is put into a high-impedance state. Next, SN74LS138-2 is deselected so that only the memory selected by the MC68000 is accessed. Finally, the data and address buffers connect the MC68000 address and data bus to the display memory. If the MC68000 is not accessing memory, then the MC68000 is isolated from the display memory by placing the data and address buffers in the high-impedance state. Decoder SN74LS138-2 is selected and accesses the display memory required by the VDG. The VDG is then released to scan the memories (MCM2114) for display information.

In order to guarantee that no incompatible display modes are used within the same scan frame, only the last data write to any even memory location can alter the latch; therefore, the VDG will always read the same data from the SN74LS75 latch between MC68000 writes to the display memory. However, the user could still adversely affect the display if the MC68000 writes occurred within the VDG display scan. The frame sync pin of the VDG is low when the VDG is not in the active display window and could be used as an interrupt or polled to determine when the MC68000 can safely write to the display memory.

The DTACK signal is generated by the SN74LS95 shift register and is necessary for the completion of any MC68000 display memory access. The shift register will add two additional wait states for each successive output; i.e., Q1 gives

two wait states, Q2 gives four wait states. Output Q0 will give no wait states. Table 1 lists the two critical memory specifications: data setup time and access time and the shift register output necessary to guarantee operation.

Typically, access time is the more critical specification. Output Q1 was chosen to be used with the MCM2114-30 (300 ns access time) memories used in this application although faster or slower memories could have been used. The speed of the display memory determines the rate at which data can be moved into the display memory. Other factors determining the speed of the data transfer are: the

method used to determine when the VDG is out of the active display area; and the software routine used to move the data.

CONCLUSION

The MC68000/MC6847 interface described in this application can be expanded or limited, according to the user's application, with relative hardware ease. Any approach of shared memory could be used as long as no bus conflicts result. Even the simple approach taken in this application results in a powerful, low cost color graphics system for the MC68000.

Table 1. Required Shift Register Output

	Q0	Q1	Q2	Q3
Data Setup Time (ns)	230	355	480	605
Access Time (ns)	250	375	500	625

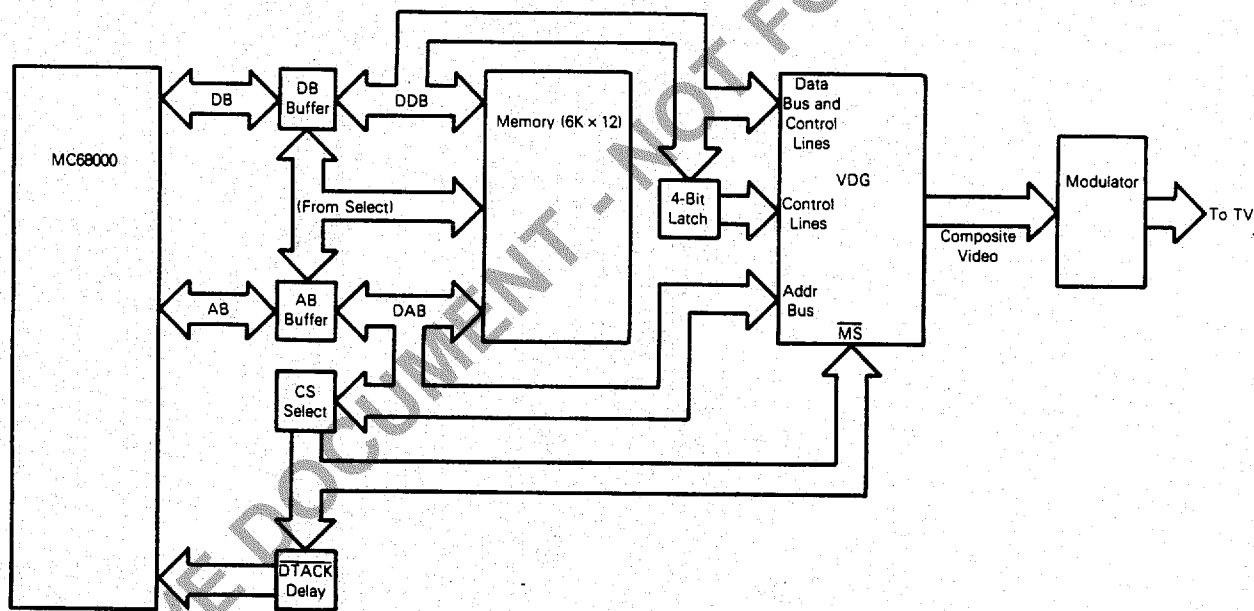


Figure 1. MC68000/MC6847 Interface — Block Diagram

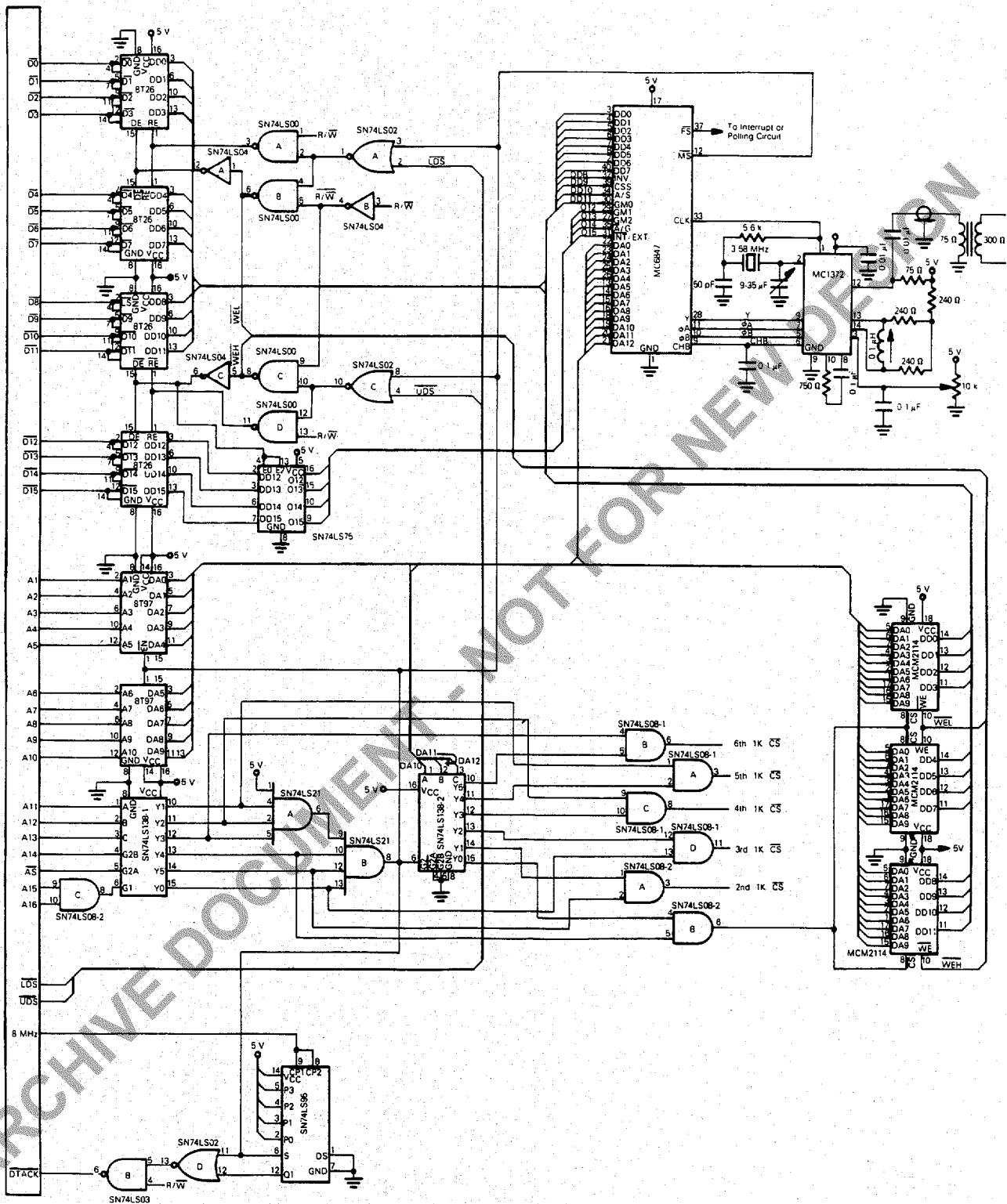


Figure 2. MC68000/MC6847 — Schematic Diagram

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