

MOSTEK 1980

MICRO SYSTEMS DATA BOOK



**1980
Micro Systems
Data Book**

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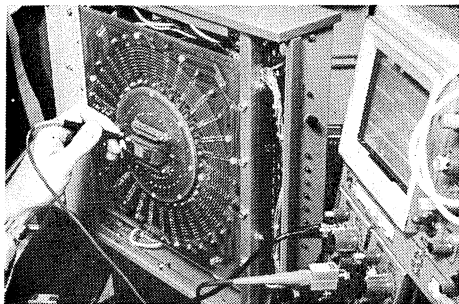
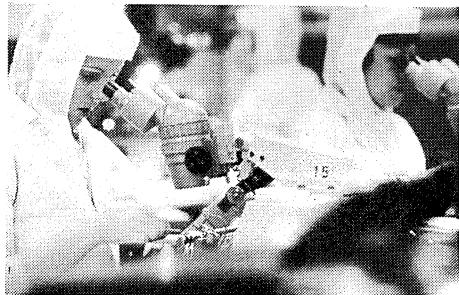
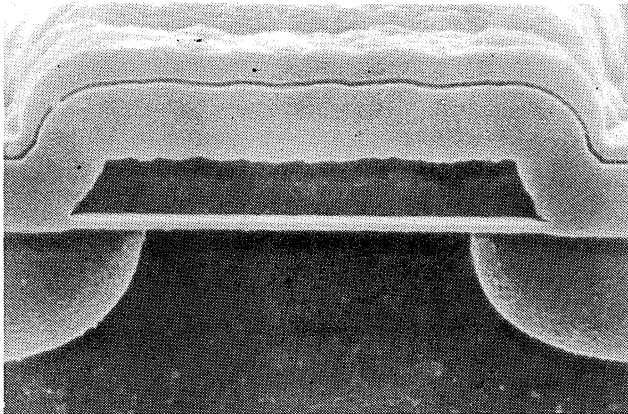
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Mostek - Technology For Today And Tomorrow



GENERAL
INFORMATION

TECHNOLOGY

From the beginning, Mostek has been recognized as an innovator. In 1970, Mostek developed the MK4006 1K dynamic RAM and the world's first single-chip calculator circuit, the MK6010. These technical breakthroughs proved the benefits of ion-implantation and cost-effectiveness of MOS. Now, Mostek represents one of the industry's most productive bases of MOS/LSI technology. Each innovation - in memories, microcomputers and telecommunications - adds to that technological capability.

QUALITY

The worth of a Mostek product is measured by its quality; how well it's designed, manufactured and tested; how well it works in your system.

In design, production and testing, our goal is meeting the spec every time. This goal requires a strict discipline, both from the company and from the individual. This discipline, coupled with a very personal pride, has driven Mostek to build in quality at every level, until every product we take to the market is as well-engineered as can be found in the industry.

PRODUCTION CAPABILITY

Mostek's commitment to increasing pro-

duction capability has made us the world's largest manufacturer of dynamic RAMs. In 1979 we shipped 25 million 4K and 16K dynamic RAMs. We built our first telecommunication tone dialer in 1974; since then, we've shipped over 5 million telecom circuits. The MK3870 single-chip microprocessor is also a large volume product with over two million in application around the world. To meet the demand for our products, production capability must be constantly increased. To accomplish this, Mostek has been in a constant process of expanding and refining our production capabilities.

THE PRODUCTS

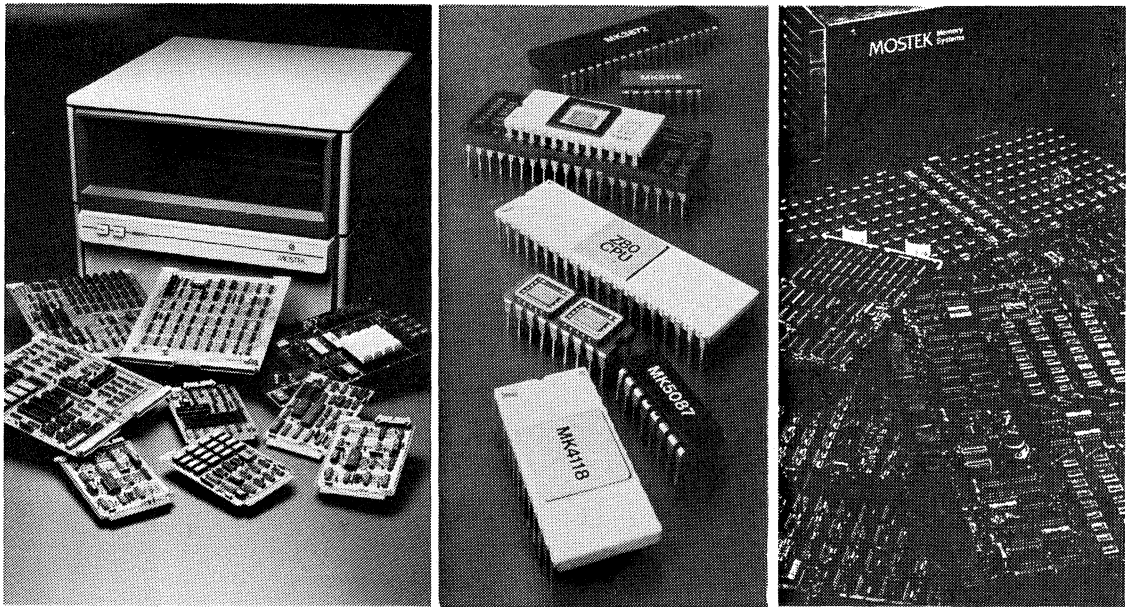
Telecommunications and Industrial Products

Mostek has made a solid commitment to telecommunications with a new generation of products, such as Integrated Pulse Dialers, Tone Dialers, CODECs, monolithic filters, tone receivers, A/D converters and counter time-base circuits.

Since 1974 over five million telecom circuits have been shipped, making Mostek the leading supplier of tone/pulse dialers and CODECs.

Memory Products

Through innovations in both circuit design, wafer processing and production, Mostek



has become the industry's leading supplier of memory products.

An example of Mostek leadership is our new BYTEWYDE™ family of static RAMs, ROMs, and EPROMs. All provide high performance, N words x 8-bit organization and common pin configurations to allow easy system upgrades in density and performance. Another important product area is fast static RAMs. With major advances in technology, Mostek static RAMs now feature access times as low as 55 nanoseconds. With high density ROMs and PROMs, static RAMs, dynamic RAMs and pseudostatic RAMs, Mostek now offers one of industry's broadest and most versatile memory families.

Microcomputer Components

Mostek's microcomputer components are designed for a wide range of applications.

Our Z80 family is the highest performance 8-bit microcomputer available today. The MK3870 family is one of the industry's most popular 8-bit single-chip microcomputers, offering upgrade options in ROM, RAM, and I/O, all in the same socket. The MK3874 EPROM version supports and prototypes the entire family.

Microcomputer Systems

Supporting the entire component product line is the powerful MATRIX™ microcomputer development system, a Z80-based,

dual floppy-disk system that is used to develop and debug software and hardware for all Mostek microcomputers.

A software operating system, FLP-80DOS, speeds and eases the design cycle with powerful commands. BASIC and FORTRAN are also available for use on the MATRIX.

Mostek's MD Series™ features both stand-alone microcomputer boards and expandable microcomputer boards. The expandable boards are modularized by function, reducing system cost because the designer buys only the specific functional modules his system requires. All MDX boards are STD-Z80 BUS compatible.

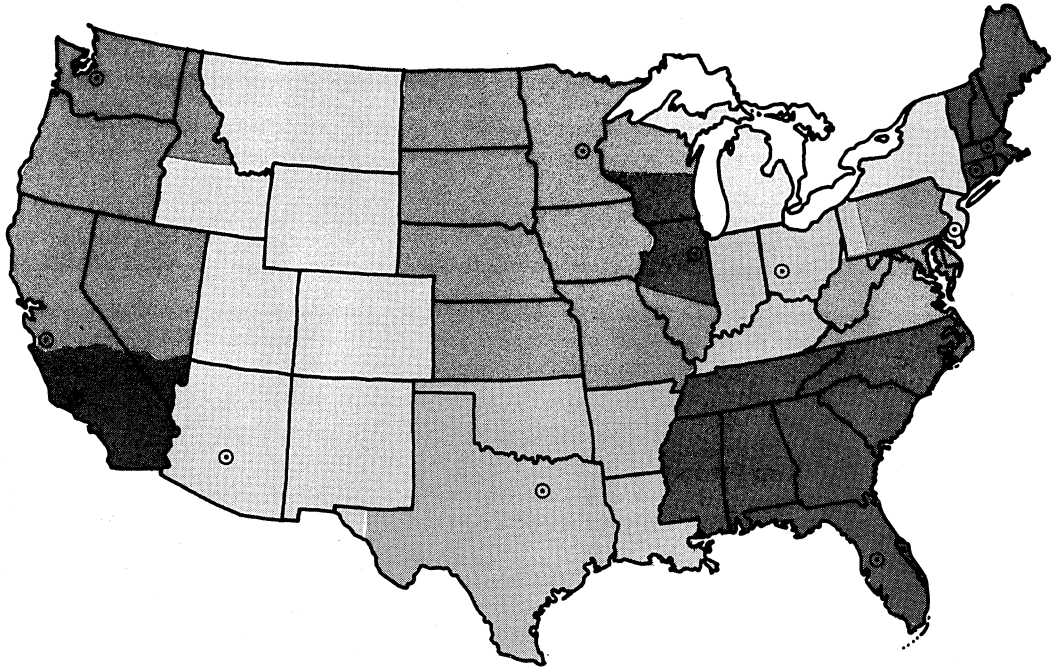
The STD-Z80 BUS is a multi-sourced motherboard interconnect system designed to handle any MDX card in any card slot.

Memory Systems

Taking full advantage of our leadership in memory components technology, Mostek Memory Systems offers a broad line of products, all with the performance and reliability to match our industry-standard circuits. Mostek Memory Systems offers add-in memory boards for popular DEC and Data General minicomputers.

Mostek also offers special purpose and custom memory boards for special applications.

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MICRO SYSTEMS DATA BOOK

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MOSTEK

MICRO SYSTEMS

STD-Z80 Bus Systems

STD-Z80
BUS

INTRODUCTION

The STD BUS concept is a joint design between Mostek and Pro-Log to satisfy the need for cost-effective OEM Microcomputer Systems. The definition of the STD BUS and the MD Series™ of OEM microcomputer modules is a result of years of microcomputer component and module manufacturing experience. The STD BUS uses a motherboard interconnect system concept and is designed to handle any MD Series™ card in any card slot. Modules for the STD BUS range from CPU, RAM and EPROM Modules to Input, Output, A/D and TRIAC control modules.

Printed circuit modules for the STD BUS are a compact 4.5 x 6.5 inches providing for system partitioning by function (RAM, PROM, I/O). This smaller module size makes system packaging easier while increasing MOS-LSI densities provide high functionality per module. Mostek has defined the STD-Z80 BUS which is a subset of the general-purpose STD BUS. This bus is defined extensively for the Z80

microprocessor and its supporting peripherals. By specifying the STD-Z80 BUS, exact functional pin descriptions and bus timing can be given. A STD-Z80 system will be guaranteed to work with all STD-Z80-designed boards. The STD-Z80 BUS fully supports the powerful Mode 2 interrupt capability of the Z80 microprocessor.

The MD Series™ provides both STD-Z80 BUS expandable modules, designated as MDX, and single-board stand-alone modules, designated as MD. For those applications requiring bus expandability, the MDX-CPU series provides that capability; if a single-board microcomputer is sufficient, the MD-SBC1 provides the system designer with a powerful Z80-based microcomputer solution.

The MD Series™ of OEM microcomputer boards and the STD-Z80 BUS offer the most cost-effective system configuration available to the OEM system designer.

MD-STD-Z80 BUS DESCRIPTION

BUS PIN	MNEMONIC	DESCRIPTION
1	+5V	+5Vdc system power
2	+5V	+5Vdc system power
3	GND	Ground-System signal ground and DC return
4	GND	Ground-System signal ground and DC return
5	-5V	-5Vdc system power
6	-5V	-5Vdc system power
7	D3	Data Bus (Tri-state, input/output, active high). D0-D7 constitute an 8-bit bidirectional data bus. The data bus is used for data exchange with memory and I/O devices.
8	D7	
9	D2	
10	D6	
11	D1	
12	D5	
13	D0	
14	D4	
15	A7	Address Bus (tri-state, output, active high). A0-A15 make up a 16-bit address bus. The address bus provides the address for memory (up to 65K bytes) data exchanges and for I/O device data exchanges. I/O addressing uses the lower 8 address bits to allow the user to directly select up to 256 input or 256 output ports. A0 is the least significant address bit. During refresh time, the lower 7 bits contain a valid refresh address for dynamic memories.
16	A15	
17	A6	
18	A14	
19	A5	
20	A13	
21	A4	
22	A12	
23	A3	
24	A11	
25	A2	
26	A10	
27	A1	
28	A9	
29	A0	
30	A8	
31	/WR	Write (Tri-state, active low). /WR indicates that the CPU data bus holds valid data to be stored in the addressed memory or I/O device.
32	/RD	Read (Tri-state, output, active low). /RD indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.
33	/IORQ	Input/Output Request (Tri-state, output, active low). The /IORQ signal indicates that the lower half of the address bus holds a valid I/O address for an I/O read or write operation. An /IORQ signal is also generated with an /M1 signal when an interrupt is being acknowledged to indicate that an interrupt response vector can be placed on the data bus. Interrupt Acknowledge operations occur during /M1 time, while I/O operations never occur during /M1 time.
34	/MEMRQ	Memory Request (Tri-state, output, active low). The /MEMRQ signal indicates that the address bus holds a valid address for a memory read or memory write operation.

BUS PIN	MNEMONIC	DESCRIPTION
35	/IOEXP	I/O Expansion, not used on Mostek MD cards. (Normally strapped to ground on the Mostek motherboard)
36	/MEMEX	Memory Expansion, not used on Mostek MD cards. (Normally strapped to ground on the Mostek motherboard)
37	/REFRESH	REFRESH (Tri-state, output, active low). /REFRESH indicates that the lower 7 bits of the address bus contain a refresh address for dynamic memories and the /MEMRQ signal should be used to perform a refresh cycle for all dynamic RAMs in the system. During the refresh cycle, A7 is a logic 0 and the upper 8 bits of the address bus contain the I register.
38	/MCSYNC	Not generated by the Mostek CPU cards. /MCSYNC can be generated by gating the following signals: /RD + /WR + /INTAK. By connecting a jumper on the MDX-CPU, this line becomes /DEBUG (Input). /DEBUG is used in conjunction with the DDT-80 operating system on the MD-DEBUG card and the MD-SST card for implementing a hardware single step function. When pulled low, the /DEBUG line will set an address modification latch which will force the upper three address lines A15, A14, and A13 to a logic 1. These address lines will remain at a logic 1 until reset by performing any I/O operation.
39	/STATUS 1 (M1)	Machine Cycle One. (Tri-state, output, active low). /M1 indicates that the current machine cycle is in the op code fetch cycle of an instruction. Note that during the execution of two byte opcodes, /M1 will be generated as each op code is fetched. These two byte opcodes always begin with a CBh, DDh, or FDh. /M1 also occurs with /IORQ to indicate an interrupt acknowledge cycle.
40	/STATUS 0	Not used on Mostek MD cards.
41	/BUSAK	Bus Acknowledge (Output, active low). Bus acknowledge is used to indicate to the requesting device that the CPU address bus, data bus, and control bus signals have been set to their high impedance state and the external device can now control the bus.
42	/BUSRQ	Bus Request (Input, active low). The /BUSRQ signal is used to request the CPU address bus, data bus, and control signal bus to go to a high impedance state so that other devices can control those buses. When /BUSRQ is activated, the CPU will set these buses to a high impedance state as soon as the current CPU machine cycle is terminated and the /BUSAK signal is activated.
43	/INTAK	Interrupt Acknowledge (Tri-state, output, active low). The /INTAK signal indicates that an interrupt acknowledge cycle is in progress, and the interrupting device should place its response vector on the data bus. The /INTAK signal is equivalent to an /IORQ during an /M1.

BUS PIN	MNEMONIC	DESCRIPTION
44	/INTRQ	Interrupt Request (Input, active low). The Interrupt Request signal is generated by I/O devices. A request will be honored at the end of the current instruction if the internal software controlled interrupt enable flip flop (IFF) is enabled and if the /BUSRQ signal is not active. When the CPU accepts the interrupt, an interrupt acknowledge signal /INTAK (/IORQ during an /M1) is sent out at the beginning of the next instruction.
45	/WAITRQ	Wait Request (Input, active low). Wait Request indicates to the CPU that the addressed memory or I/O device is not ready for a data transfer. The CPU continues to enter wait states for as long as this signal is active. This signal allows memory or I/O devices of any speed to be synchronized to the CPU. Use of this signal postpones refresh as long as it is held active.
46	/NMIRQ	Non Maskable Interrupt Request (Input, negative edge triggered). The Non Maskable Interrupt Request line has a higher priority than the /INTRQ line and is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop. /NMIRQ automatically forces the CPU to restart to location 0066h. The program counter is automatically saved in the external stack so that the user can return to the program that was interrupted. Note that continuous WAIT cycles can prevent the current instruction from ending, and that a /BUSRQ will override a /NMIRQ.
47	/SYSRESET	System Reset (Output, active low). The System Reset line indicates that a reset has been generated either from an external reset or the power on reset circuit. The system reset will occur only once per reset request and will be approximately 2 μ s in duration. A system reset will also force the CPU program counter to zero, disable interrupts, set the I register to 00h, set the R register to 00h, and set Interrupt Mode 0.
48	/PBRESET	Push Button Reset (Input, active low). The Push Button Reset will generate a debounced system reset.
49	/CLOCK	Processor Clock (Output, active low). Single phase system clock.
50	/CNTRL	Not used on Mostek MD cards.
51	PCO	Priority Chain Output (Output, active high). This signal is used to form a priority interrupt daisy chain when more than one interrupt driven device is being used. A high level on this pin indicates that no other devices of higher priority are being serviced by a CPU interrupt service routine.
52	PCI	Priority Chain In (Input, active high). This signal is used to form a priority interrupt daisy chain when more than one interrupt driven device is being used. A high level on this pin indicates that no other devices of higher priority are being serviced by a CPU interrupt service routine.
53	AUX GND	Auxiliary Ground (Bussed)
54	AUX GND	Auxiliary Ground (Bussed)

BUS PIN	MNEMONIC	DESCRIPTION
55	+12V	+12Vdc system power
56	-12V	-12Vdc system power

NOTES

1. Input/Output references of each signal are made with respect to MDX-CPU module.
2. The following signals have pull-up resistors: /WR, /RD, /IORQ, /MEMRQ, /REFRESH, /DEBUG, /M1, /BUSRQ, /INTAK, /INTRO, /WAITRQ, /NMIRQ, /SYSRESET, /PBRESET and /CLOCK.

STD-780
BUS

MICRO SYSTEMS DATA BOOK

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MOSTEK®

MDX SERIES DATA PROCESSING

MDX-CPU1

MK77850-0, MK77850-4

MDX SERIES
DATA PROCESSING

FEATURES

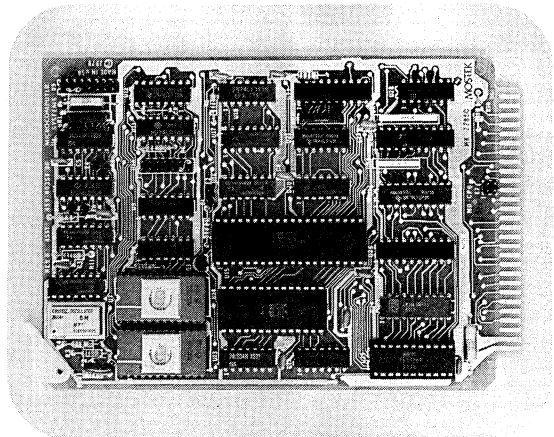
- STD-Z80 BUS-compatible
- 4K x 8 EPROM (two 2716's, customer-provided)
- 256 x 8 Static RAM (compatible with DDT-80 debugger)
- Flexible Memory decoding for EPROM and RAM
- Four counter/timer channels
- Restart to 0000H or E0000H (strapping option)
- Debug-compatible for single step in DDT-80
- 2.5MHz version (-0)
- 4MHz version (-4)
- +5V only
- Fully-buffered signals for system expandability
- Z80 CPU

MDX-CPU1 DESCRIPTION

The Mostek MDX-CPU1 is the heart of an MD Series Z80 system. Based on the powerful Z80 microprocessor, the MDX-CPU1 can be used with great versatility in an OEM microcomputer system application. This is done simply by inserting custom ROM or EPROM memories into the sockets provided on the board and configuring them virtually anywhere within the Z80 memory map.

On-board memory is provided in the form of sockets for 4K of EPROM (2-2716's) and 256 bytes of scratchpad RAM as pictured in the block diagram. Either 2716 EPROM can be located at any 2K boundary within any given 16K block in the Z80 memory map via a jumper arrangement. In

MDX-CPU 1 BOARD

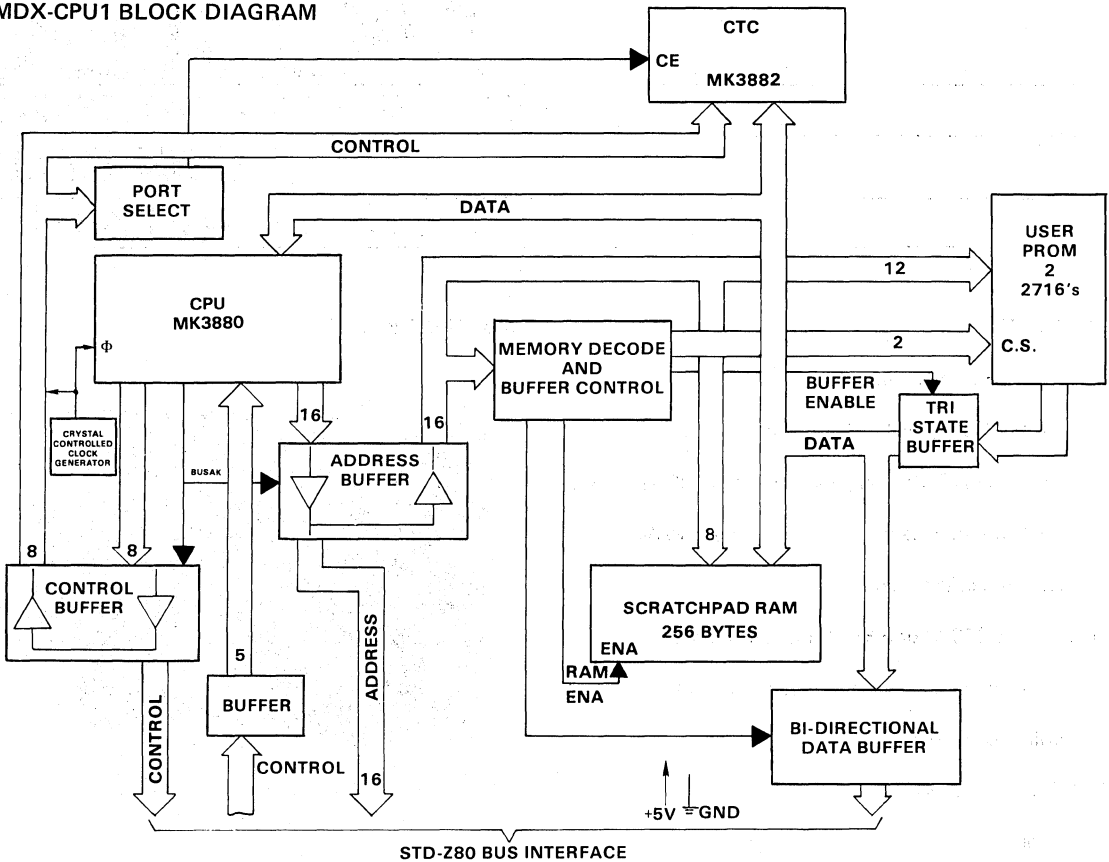


addition, an MK3882 Counter Timer Circuit is included on the MDX-CPU1 to provide counting and timing functions for the Z80.

The MDX-CPU1 can be used in conjunction with the MDX-DEBUG and MDX-DRAM modules to utilize DDT-80 and ASMB-80 in system development. This is accomplished by strapping the scratchpad RAM to reside at location FFOOH so that it will act as the Operating System RAM for DDT-80.

The MDX-CPU1 is also available in a 4MHz version (MDX-CPU1-4). In this version, one wait state is automatically inserted each time that the on-board memory is accessed by a read or write cycle. This is necessary to make the access times of the 2716 PROMs and the 3539 scratchpad RAM compatible with the MK3880 4MHz Z80-CPU.

MDX-CPU1 BLOCK DIAGRAM



WORD SIZE

Instruction: 8, 16, 24, or 32 bits
Data: 8 bits

CYCLE TIME

Clock period (T state) 400ns @ 2.5MHz
250ns @ 4.0MHz
Instruction Cycle: Min. 4 T States
Max. 23 T States

MEMORY CAPACITY

On-Board EPROM - 4K bytes (sockets only)
On-Board RAM - 256 bytes
Off-Board Expansion - Up to 65,536 byte, with user-specified combinations of RAM, ROM, PROM.

MEMORY ADDRESSING

On-Board EPROM: jumper-selectable for any 2K boundary within a 16K block of Z80 memory map.
On-Board RAM: FF00-FFFF

MEMORY REFRESH

The MDX-CPU1 generates all address and control signals necessary to refresh dynamic RAM (such as MDX-DRAM) modules. Refresh occurs automatically during each OP-code fetch cycle and is therefore transparent to system throughput.

MEMORY SPEED REQUIRED

MEMORY	ACCESS TIME	CYCLE TIME
2716*	450ns	450ns

*Single 5-volt type required

I/O ADDRESSING

The on-board 4-channel programmable timer is hardwired to the following port addresses:

PORT ADDRESS (HEX)	MK3882 CHANNEL
7C	0
7D	1
7E	2
7F	3

I/O CAPACITY

Up to 252 port addresses can be decoded off board. Four port addresses are on board. $252 + 4 = 256$ total I/O ports.

INTERRUPTS

The Z80-CPU may be programmed to process interrupts in any of three different modes (mode 0, 1 or 2 as described in the MK3880 Technical Manual). Mode 2 operation (vectored interrupts) is by far the most powerful and is compatible with Mostek MDX Series cards.

Multi-level interrupt processing is also possible with the Z80 CPU. The level of stacking is limited only by available memory space.

The MDX-CPU1 will also accept nonmaskable interrupts which force a restart at location 0066H.

SYSTEM INTERRUPT UNITS (SIU) = 1

SYSTEM CLOCK

MDX-CPU1	2.5 MHz \pm 0.05%
MDX-CPU1-4	4.0 MHz \pm 0.05%

STD BUS INTERFACE

Inputs: One 74LS load max.

Outputs: $I_{OL} = 24$ mA min. at $V_{OL} = 0.5$ Volts
 $I_{OH} = -3$ mA min. at $V_{OH} = 2.4$ Volts

OPERATING TEMPERATURE

0°C to 60°C

POWER SUPPLY REQUIREMENTS

5V \pm 5% at 1.2 A (excluding memory power requirements)

CARD DIMENSIONS

4.50 in. (11.43 cm.) wide by 6.50 in. (16.51 cm.) long
0.48 in. (1.22 cm.) maximum height
0.062 in. (0.16 cm.) printed-circuit-board thickness

CONNECTORS

FUNCTION	CONFIGURATION	MATING CONNECTOR
STD-Z80 BUS	56-pin	Printed Circuit Viking 3VH28/1CE5 Wire-Wrap Viking 3VH28/1CND5 Solder Lug Viking 3VH28/1CN5

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
MDX-CPU1	Module with Operation Manual less EPROMs and mating connectors. 2.5MHz version.	MK77850-0
MDX-CPU1-4	Module with Operations Manual less EPROMs and mating connectors. 4.0MHz version.	MK77850-4
	MDX-CPU1 and MDX-CPU1-4 Operations Manual Only	MK79612

MOSTEK®

MDX SERIES DATA PROCESSING

MDX-CPU2

MK77853-0, MK77853-4

MDX SERIES
DATA PROCESSING

FEATURES

- STD-Z80 BUS compatible
- Utilizes the powerful Z80 Microprocessor
- Six 24-pin sockets which may be strapped to accept any combination of the following industry-standard memory devices:

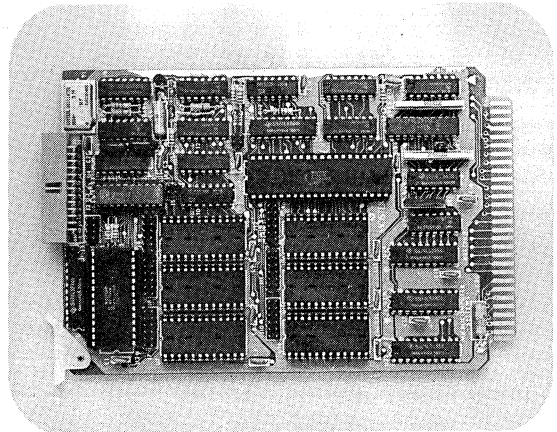
EPROM	STATIC RAM	ROM
2758 (1K x 8)	MK4118 (1K x 8)	MK34000 (2K x 8)
2716 (2K x 8)	MK4801 (1K x 8)	
2732 (4K x 8)	MK4802 (2K x 8)	

- Flexible memory decoding on any 1K boundary
- Bidirectional address, data and control busses to permit external DMA
- Four cascadable counter/timer channels
- Automatic, transparent dynamic memory refresh
- Fully-buffered signals for system expandability
- Selectable reset address to either 0000H or E000H
- Selectable wait-state generator
- Compatible with MDX-SST for single step operation during debugging
- 4 MHz version available
- Single +5 Volt supply

DESCRIPTION

The MDX-CPU2 features six 24-pin memory sockets which enable the user to populate the module with any combination of designated ROM, RAM, and EPROM.

MDX-CPU2 BOARD PHOTO

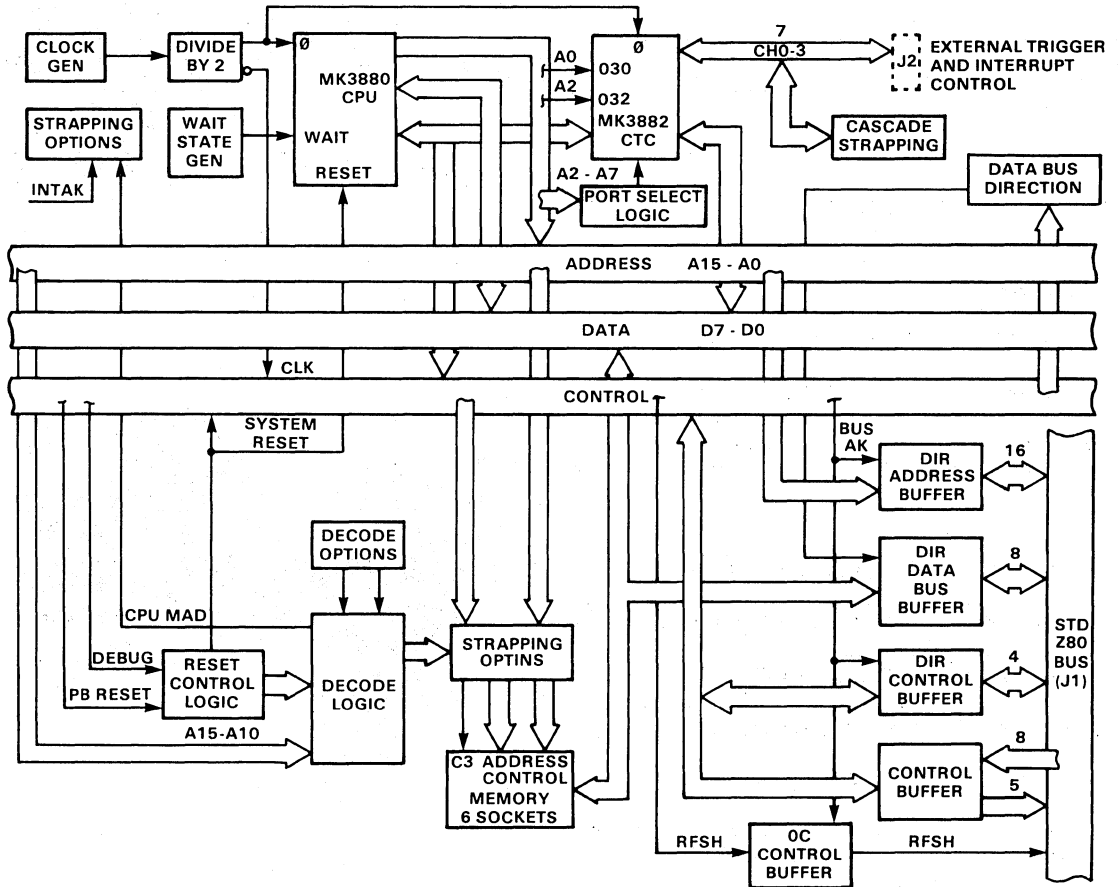


Flexible address decoding allows the user to configure each memory device within any 1K boundary of the 64K memory map. A PROM decoder is supplied which will allow the user to choose one of four preselected memory configurations or, if desired, the user may, by programming a decoder PROM, assign any of the six sockets to memory addresses as required by his application needs. Address, data and control busses have been made bidirectional to allow external masters to directly access CPU memory.

A 4-channel counter/timer circuit (MK3882) is included on-board for software-controlled counting and time functions. The CTC Trigger inputs and Zero Count outputs are buffered and brought out to a connector for off-board control. In addition, a strapping option makes it possible to cascade the four CTC channels for long count sequences.

Another strapping option allows the user to select a reset address of either 0000H or E000H for compatibility with Mostek standard software.

MDX-CPU2 BLOCK DIAGRAM



A 4 MHz version of MDX-CPU2 is also available (MDX-CPU2-4). To ensure sufficient memory access time at 4 MHz operation, a jumper option enables automatic insertion of one WAIT state for those memory devices identified as "slow" in the decoder PROM. The standard decoder PROM supplied with MDX-CPU2-4 is pre-programmed for use with MK2716 EPROMs and MK4118 Static RAMs, and identifies 2716 sockets as "slow" and 4118 sockets as "fast."

WORD SIZE

Instruction: 8, 16, 24, or 32 bits
Data: 8 bits

CYCLE TIME

Clock period (T state): 400 ns @ 2.5 MHz
250 ns @ 4.0 MHz
Instruction Cycle: Min. 4 T states
Max. 23 T states

MEMORY CAPACITY

Six 24-pin sockets are provided which may be populated with any mixture of the following devices:

- 2758 (1K x 8 EPROM)
- 2716 (2K x 8 EPROM)
- 2732 (4K x 8 EPROM)
- MK4118 (1K x 8 Static RAM)
- MK4801 (1K x 8 Static RAM)
- MK4802 (2K x 8 Static RAM)
- MK34000 (2K x 8 ROM)

MEMORY ADDRESSING

On-board PROM decoding allows any on-board memory to be configured on any 1K boundary of the Z80 CPU memory map.

Off-board expansion to a total of 65,536 bytes is possible with the use of various MDX memory modules.

MEMORY REFRESH

The MDX-CPU2 generates all address and control signals necessary to refresh dynamic RAM (such as MDX-DRAM) modules. Refresh occurs automatically during each OP code fetch cycle and is therefore transparent to system throughput.

I/O ADDRESSING

The on-board 4-channel programmable timer is hard-wired to the following addresses:

MK3882 Channel	Port Address (Hex)
0	7C
1	7D
2	7E
3	7F

I/O CAPACITY

The Z80 CPU utilizes the lower 8 bits of its address bus for I/O addressing to yield a total of 256 possible port addresses.

INTERRUPTS

The Z80-CPU may be programmed to process interrupts in any of three different modes (mode 0, 1 or 2 as described in the MK3880 Technical Manual). Mode 2 operation (vectored interrupts) is by far the most powerful and is compatible with Mostek MDX Series cards.

CONNECTORS

Function	Configuration	Mating Connectors
STD-Z80 BUS	56-Pin 0.125 in. centers	PRINTED CIRCUIT Viking 3VH28/1CE5 WIRE-WRAP Viking 3VH28/ 1CND5 SOLDER LUG Viking 3VH28/ 1CN5
CTC I/O	26-Pin 0.100 in. centers	FLAT RIBBON Ansley 609-2600M DISCRETE WIRES Winchester PGB26A (Housing) Winchester 100- 70020 (Contacts)

Multi-level interrupt processing is also possible with the Z80 CPU. The level of stacking is limited only by available memory space.

The MDX-CPU2 will also accept nonmaskable interrupts which force a restart at location 0066H.

SYSTEM INTERRUPT UNITS (SIU) = 1

SYSTEM CLOCK

MDX-CPU2	2.5 MHz \pm 0.05%
MDX-CPU2-4	4.0 MHz \pm 0.05%

STD BUS INTERFACE

Inputs:	One 74LS load max.
Outputs:	I_{OL} = 24 mA min. @ V_{OL} 0.5 Volts I_{OH} = -3 mA min. @ V_{OH} 2.4 Volts

OPERATING TEMPERATURE

0°C to 60°C

POWER SUPPLY REQUIREMENTS

5V \pm 5% at 1.2 A (excluding memory power requirements)

CARD DIMENSIONS

4.50 in. (11.43 cm.) wide by 6.50 in. (16.51 cm.) long
0.48 in. (1.22 cm.) maximum height
0.062 in. (0.16 cm.) printed circuit board thickness

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
MDX-CPU2	2.5 MHz CPU2 module with Operations Manual (less memory and mating connectors)	MK77853-0
MDX-CPU2-4	4.0 MHz CPU2 module with Operations Manual (less memory and mating connectors)	MK77853-4
	MDX-CPU2 and MDX-CPU2-4 Operations Manual Only	MK79711

MOSTEK[®]

MDX SERIES DATA PROCESSING

MDX-MATH

MK77852-0

MDX SERIES
DATA PROCESSING

FEATURES

- STD-Z80 BUS compatible
- Fixed-point 16 and 32-bit operations
- Floating point 32-bit operations
- Binary data formats
- Add, Subtract, Multiply and Divide
- Trigonometric and inverse trigonometric functions
- Square roots, logarithms, exponentials
- Float-to-fixed and fixed-to-float conversions
- Stack-oriented operand storage
- On-board wait-state insertion circuitry

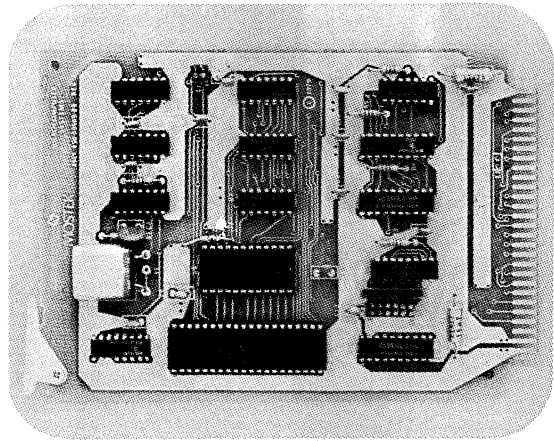
DESCRIPTION

The MDX-MATH board is offered as one of Mostek's complete line of STD-Z80 BUS-compatible microcomputer modules. The MDX-MATH board, based on the AM9511 Arithmetic Processing Unit (APU), provides high performance fixed and floating point trigonometric and mathematical operations. It can be used to enhance the computational capability of a wide variety of STD-Z80 BUS systems.

Figure 1 is a block diagram which illustrates the functional elements of the MDX-MATH board.

The Arithmetic Processing Unit is a monolithic MOS/LSI device that performs all of the mathematical operations. All transfers to and from the APU take place over the 8-bit, bi-directional data bus. Operands are pushed onto an

MDX-MATH BOARD PHOTO

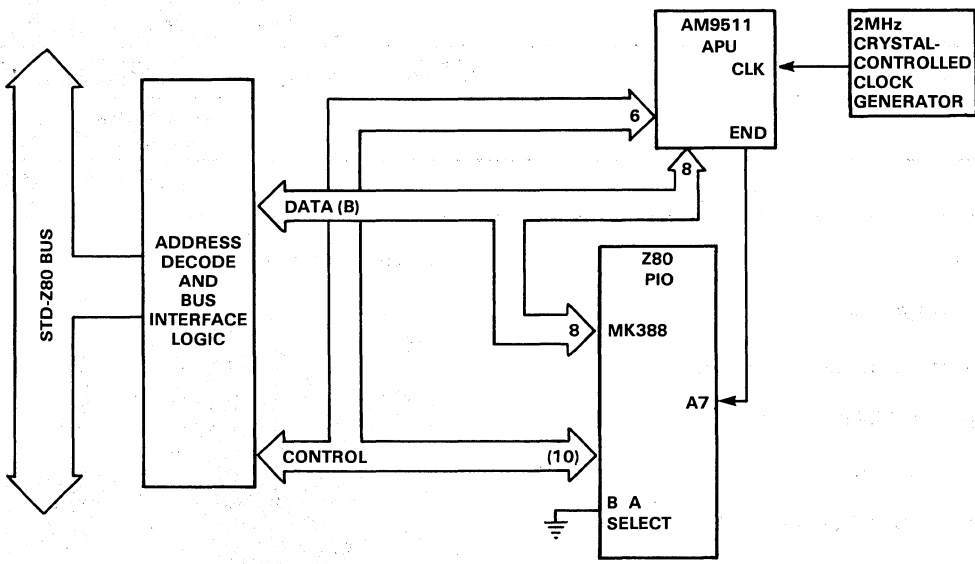


internal stack within the APU and a command is issued to perform operations on the data in the stack. Results are then available to be retrieved from the stack, or additional commands may be entered.

Side A of the MK3881 PIO can be utilized to provide a Z80 Mode 2 interrupt response when the APU completes the execution of a command and pulls its END line low. If the PIO has been programmed to interrupt on the high-to-low transition of port bit A7, it will provide a vectored interrupt and maintain the daisy-chain-priority interrupt logic compatible with the STD-Z80 BUS.

Each MDX-MATH board has a total of five registers; three WRITE only and two READ only. These registers appear as three I/O port addresses and are defined in Table 1.

MDX-MATH BLOCK DIAGRAM



MDX-MATH REGISTERS

Table 1

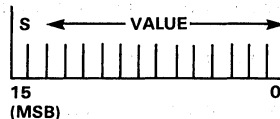
Port Address	Read	Write
X X X X X 0 0	APU Status	APU Command
X X X X X 0 1	Undefined	PIO Side A Control
X X X X X 1 0	APU Stack	APU Stack

The "X" symbols are "don't cares" and are jumper-selectable. These port addresses are fully decoded.

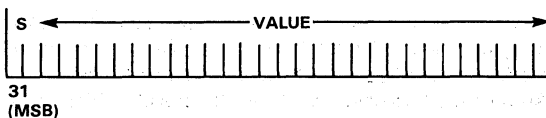
The MDX-MATH board operates from an independent 2 MHz, crystal-controlled, clock generator circuit. The time required by the AM9511 to execute some of its commands can exceed 4 milliseconds. Because of this, there is circuitry designed to block any access to the APU which would cause wait states to be inserted for such long periods of time during the execution of a command. This action prevents any interference with dynamic memory refresh as well as any sacrifice of Z80 processing time.

The Arithmetic Processing Unit handles operands in both fixed point and floating point formats. Fixed point operands may be represented in either single (16-bit operands) or double precision (32-bit operands) and are always represented as binary, two's complement values.

16-BIT FIXED POINT FORMAT

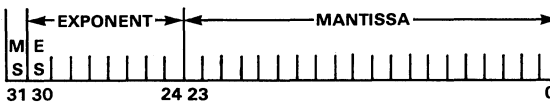


32-BIT FIXED POINT FORMAT



FLOATING POINT FORMAT

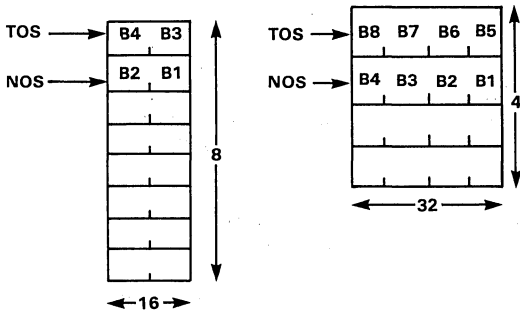
The format for floating point values is given. The mantissa is expressed as a 24-bit (fractional) value; the exponent is expressed as an unbiased two's complement 7-bit value having a range of -64 to +63. The most significant bit is the sign of the mantissa (0 = positive, 1 = negative), for a total of 32 bits. The binary point is assumed to be to the left of the most significant mantissa bit (bit 23). All floating point data values must be normalized. Bit 23 must be equal to 1, except for the value zero, which is represented by all zeros.



The range of values that can be represented in this format is $\pm (2.7 \times 10^{-20}$ to $9.2 \times 10^{18})$ and zero.

STACK CONTROL

The user interface includes access to an 8-level, 16-bit-wide data stack. Since single-precision, fixed-point operands are 16 bits in length, eight such values may be maintained in the stack. When using double-precision, fixed point or floating point formats, four values may be stored. The stack in these two configurations can be visualized as shown.

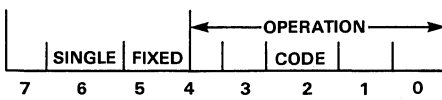


Data is written onto the stack, eight bits at a time, in the order shown (B1, B2, B3, ...). Data is removed from the stack in reverse byte order (B8, B7, B6, ...). Data should be transferred into or out of the stack in multiples of the number of bytes appropriate to the chosen data format.

COMMAND STRUCTURE

Figure 2 lists the commands and their mnemonics.

Each command consists of a single 8-bit byte having the format illustrated.

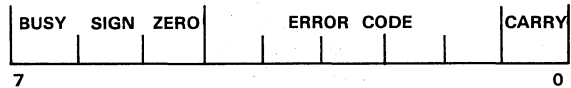


Bits 0-4 select the operation to be performed. Bits 5-6 select the data format for the operation. If bit 5 is a 1, a fixed point data format is specified. If bit 5 is a 0, the floating point

format is specified. Bit 6 selects the precision of the data to be operated on by fixed point commands (if bit 5 = 0, bit 6 must be 0). If bit 6 is a 1, single-precision (16-bit) operands are indicated; if bit 6 is a 0, double-precision (32-bit) operands are indicated. Results are undefined for all illegal combinations of bits in the command byte.

DEVICE STATUS

Device status is provided by means of an internal status register whose format is shown.



- BUSY:** Indicates that the MDX-MATH board is currently executing a command (1 = Busy).
- SIGN:** Indicates that the value on the top of stack is negative (1 = Negative).
- ZERO:** Indicates that the value on the top of stack is zero (1 = Value is zero).
- ERROR CODE:** This field contains an indication of the validity of the result of the last operation. The error codes are:
 - 0000 - No error
 - 1000 - Divide by zero
 - 0100 - Square root or log of negative number
 - 1100 - Argument of inverse sine, cosine, or e^x too large
 - XX10 - Underflow
 - XX01 - Overflow
- CARRY:** Previous operation resulted in carry or borrow from most significant bit. (1 = Carry/Borrow, 0 = No Carry/No Borrow)

The BUSY bit in the status register can be read by the Z80 CPU at any time whether an operation is in progress or not.

COMMAND SUMMARY

Figure 2

ACOS	ARCCOSINE	LOG	COMMON LOGARITHM
ASIN	ARCSINE	LN	NATURAL LOGARITHM
ATAN	ARCTANGENT	NOP	NO OPERATION
CHSD	CHANGE SIGN DOUBLE	POPD	POP STACK DOUBLE
CHSF	CHANGE SIGN FLOATING	POPF	POP STACK FLOATING
CHSS	CHANGE SIGN SINGLE	POPS	POP STACK SINGLE
COS	COSINE	PTOD	PUSH STACK DOUBLE
DADD	DOUBLE ADD	PTOF	PUSH STACK FLOATING
DDIV	DOUBLE DIVIDE	PTOS	PUSH STACK SINGLE
DMUL	DOUBLE MULTIPLY LOWER	PUPI	PUSH
DMUU	DOUBLE MULTIPLY UPPER	PWR	POWER (XY)
DSUB	DOUBLE SUBTRACT	SADD	SINGLE ADD
EXP	EXPONENTIATION (e ^x)	SDIV	SINGLE DIVIDE
FADD	FLOATING ADD	SIN	SINE
FDIV	FLOATING DIVIDE	SMUL	SINGLE MULTIPLY LOWER
FIXD	FIX DOUBLE	SMUU	SINGLE MULTIPLY UPPER
FIXS	FIX SINGLE	SQRT	SQUARE ROOT
FLTD	FLOAT DOUBLE	SSUB	SINGLE SUBTRACT
FLTS	FLOAT SINGLE	TAN	TANGENT
FMUL	FLOATING MULTIPLY	XCHD	EXCHANGE OPERANDS DOUBLE
FSUB	FLOATING SUBTRACT	XCHF	EXCHANGE OPERANDS FLOATING
		XCHS	EXCHANGE OPERANDS SINGLE

WORD SIZE

Data: 8 bits
I/O Addressing: 8 bits

I/O ADDRESSING

On-board programmable - See Table 1

I/O CAPACITY

Five parallel 8-bit ports. Three WRITE Only and two READ only. (See Table 1)

INTERRUPTS

Vectored interrupt generated. Daisy-chained interrupt priority. Interrupt vector programmable upon initialization.

SYSTEM INTERRUPT UNITS (SIU) = 1

SYSTEM CLOCK

	MIN	MAX
MDX-MATH	250kHz	2.5 MHz

The MDX-MATH board operates from an independent 2MHz clock.

OPERATING TEMPERATURE RANGE

0°C to 60°C

POWER SUPPLY REQUIREMENTS

+12V ± 5% at 120 mA max
+5V ± 5% at 0.9 A max

STD BUS INTERFACE

Inputs: One 74LS Load max
Outputs: I_{OH} = -3mA min at 2.4 Volts
I_{OL} = 24mA min at 0.5 Volts

CARD DIMENSIONS

4.5 in. (11.43cm) high by 6.50 in. (16.51cm) long
0.48 in. (1.22cm) maximum profile thickness
0.062 in. (0.16cm) printed-circuit-board thickness

CONNECTORS

Function	Configuration	Mating Connector
STD-Z80 BUS	56-pin dual readout 0.125 in. centers	PRINTED CIRCUIT Viking 3VH28/1CE5 WIRE WRAP Viking 3VH28/ 1CND5 SOLDER LUG Viking 3VH28/ 1CN5

MDX SERIES
DATA PROCESSING

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
MDX-MATH	Module with Operations Manual; 2.5 MHz version.	MK77852-0
	MDX-MATH Operations Manual Only	MK79741

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MOSTEK®

MD SERIES

System Interrupt Units

CARD	SIU's
MDX-CPU1	1
MDX-CPU2	1
MDX-DRAM8/16/32	0
MDX-EPROM/UART	0
MDX-DEBUG	0
MDX-PIO	2
MDX-SIO	1
MDX-SST	0
MDX-FLP	1
MDX-MATH	1
MDX-A/D8	1
MDX-AIO	0
MDX-A/D12	1
MDX-D/A8	0
MDX-D/A12	0
MDX-UMC	0
MDX-SRAM4/8/16	0
MDX-EPROM	0
MDX-INT	1
MDX-SC/D	1

MD SERIES
INPUT/OUTPUT

MOSTEK®

MD SERIES I/O CARDS

MDX-A/D8

MK77669-0, MK77669-4

FEATURES

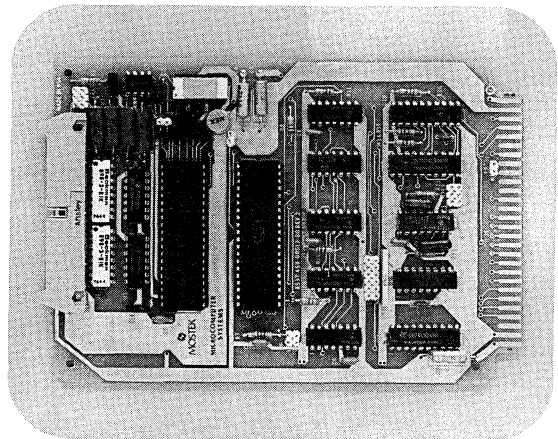
- STD-Z80 BUS compatible
- 8-Bit A/D converter with 16 single-ended analog inputs
- 0 to +5 Volts Full Scale Input Range
- Total unadjusted error $< \pm \frac{1}{2}$ LSB
- Linearity error $< \pm \frac{1}{2}$ LSB
- No missing codes
- Guaranteed monotonicity
- No zero-adjust required
- No full-scale adjust required
- Provisions for additional channel expansion
- Single +5 Volt supply
- Address programmable
- 4MHz option

DESCRIPTION

The Analog to Digital Converter Module, MDX-A/D8, is designed to be a 16-channel single-ended A/D module for the STD-Z80 BUS. The module is designed around the Mostek MK50816 8-bit A/D converter/16 channel analog multiplexer. Additional provisions have been included to allow further analog expansion if desired. Figure 1 is a block diagram of the MDX-A/D8 showing the major elements of the module.

The first element of this board is the multiplexer. This 16-channel multiplexer can directly access any one of 16 single-ended analog channels and provides logic for additional channel expansion. All analog input lines contain a diode/resistor protection circuit to reduce potential damage from overvoltage and transient inputs.

MDX-A/D8 BOARD PHOTO



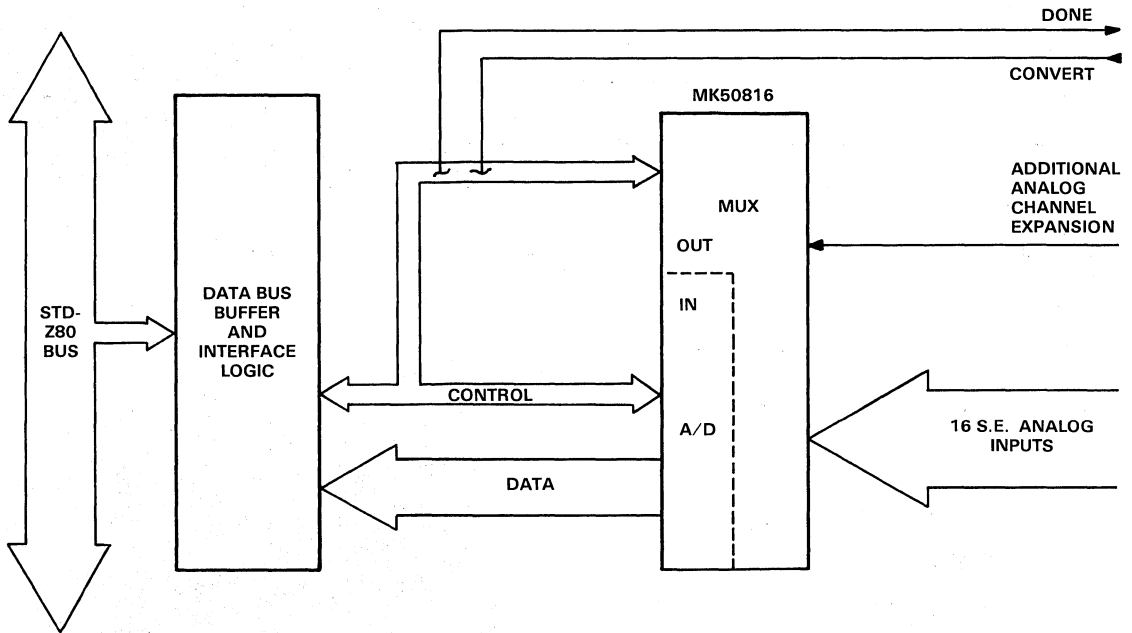
MD SERIES
INPUT/OUTPUT

The other half of the MK50816 is the A/D converter. The 8-bit A/D consists of 256 series resistors with an analog switch tree, a chopper-stabilized comparator and a successive approximation register. The series resistor approach guarantees monotonicity and no missing codes. The need for external zero and full-scale adjustments has been eliminated and an absolute accuracy of ≤ 1 LSB including quantizing error is provided. A start convert signal initiates the conversion process and can be jumper-selected from either an external source or under program control. Upon completion, a DONE signal is generated to indicate end of conversion. This signal is used to flag the program as well as any external device.

The Data Bus Buffer and Interface Logic allows the MDX-A/D8 module to interface with the STD-Z80 BUS. It provides buffering for all signals as well as address decoding and A/D port control. A total of four port address locations are required and can start on any four-word boundary.

MDX-A/D8 BLOCK DIAGRAM

Figure 1



WORD SIZE

Data: 8 bits
I/O Addressing: 8 bits

I/O CAPACITY

Eight-bit analog-to-digital converter with up to sixteen single-ended analog input channels. Channel expansion available. Start-conversion and done-handshake signals available at the edge connector.

I/O ADDRESSING

On-board programmable on 4-word boundaries
 X X X X X 0 0 A/D Port Configuration Data
 X X X X X 0 1 A/D Port Configuration Control
 X X X X X 1 0 A/D Data Input/Output Port
 X X X X X 1 1 Data Control Port

X = don't care

CONVERSION TIME

138 microseconds max.

INTERRUPTS

Vectored interrupts generated. Interrupt vector programmable upon initialization. Daisy-chained interrupt priority. Interrupts are controlled by a Mostek MK3881 Parallel I/O controller chip.

SYSTEM INTERRUPT UNITS (SIU) = 1

SYSTEM CLOCK

	MIN.	MAX.
MDX-A/D	250kHz	2.5 MHz
MDX-A/D-4	250kHz	4.0 MHz

STD BUS INTERFACES

Inputs: One 75LS Load
 Outputs: $I_{OH} = -3\text{mA min. at } 2.4\text{ Volts}$
 $I_{OL} = 24\text{mA max. at } 0.5\text{ Volts}$

OPERATING TEMPERATURE RANGE

0°C +60°C

POWER SUPPLY REQUIREMENTS

+5 Volts $\pm 5\%$ at 0.6 A max.

CARD DIMENSIONS

4.5 in. (11.43cm) high by 6.50 in. (16.51 cm) long
 0.48 in. (1.22cm) maximum profile thickness
 0.062 in. (0.16cm) printed-circuit-board thickness

CONNECTORS

Function	Configuration	Mating Connector
STD-Z80 BUS	56-pin 0.125-in. centers	PRINTED CIRCUIT Viking 3VH28/1CE5 WIRE WRAP Viking 3VH28/1CND5 SOLDER LUG Viking 3VH28/1CN5
Analog I/O	40-pin 0.100 in. centers	Ansley 609-4000

**MD SERIES
INPUT/OUTPUT**

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
MDX-A/D8	Module with Operation Manual less mating connector 2.5 MHz version	MK77669-0
MDX-A/D8-4	Module with Operation Manual less mating connector 4.0 MHz version	MK77669-4
	MDX-A/D8 Operations Manual Only	MK79632

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MD SERIES I/O CARDS

MDX-AIO

MK77654

FEATURES

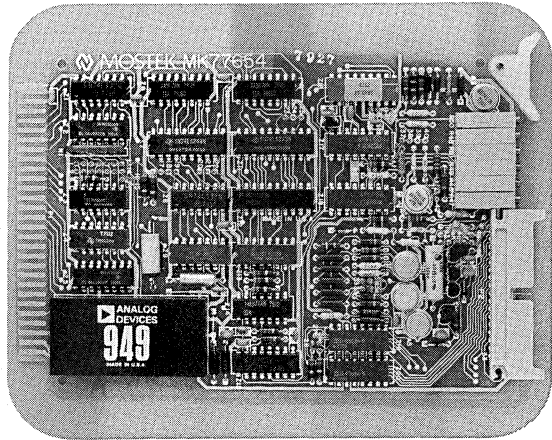
- STD and STD-Z80 BUS compatible
- Memory-mapped I/O
- Combination Analog Input and Output
- 8 Differential Analog Inputs or 16 Single-Ended Analog Inputs
- Two channels of 8-bit Analog Output
- Input overvoltage protection to ± 35 volts
- Sample-and-Hold Amplifier On-Board
- Monolithic 10-Bit A/D Converter
- Single On-Board Precision Reference Circuit
- Single +5-Volt Supply

DESCRIPTION

The MDX-AIO Analog Data Acquisition and Control Board comprises a complete analog I/O subsystem which simplifies the interface of real-time analog signals to MD Series microcomputer systems.

The analog signals are connected to the board through a pin connector mounted at the opposite board edge from the digital bus. The MDX-AIO comes complete with its own DC/DC converter so that the board can operate directly from the +5 volt supply.

MDX-AIO BOARD PHOTO

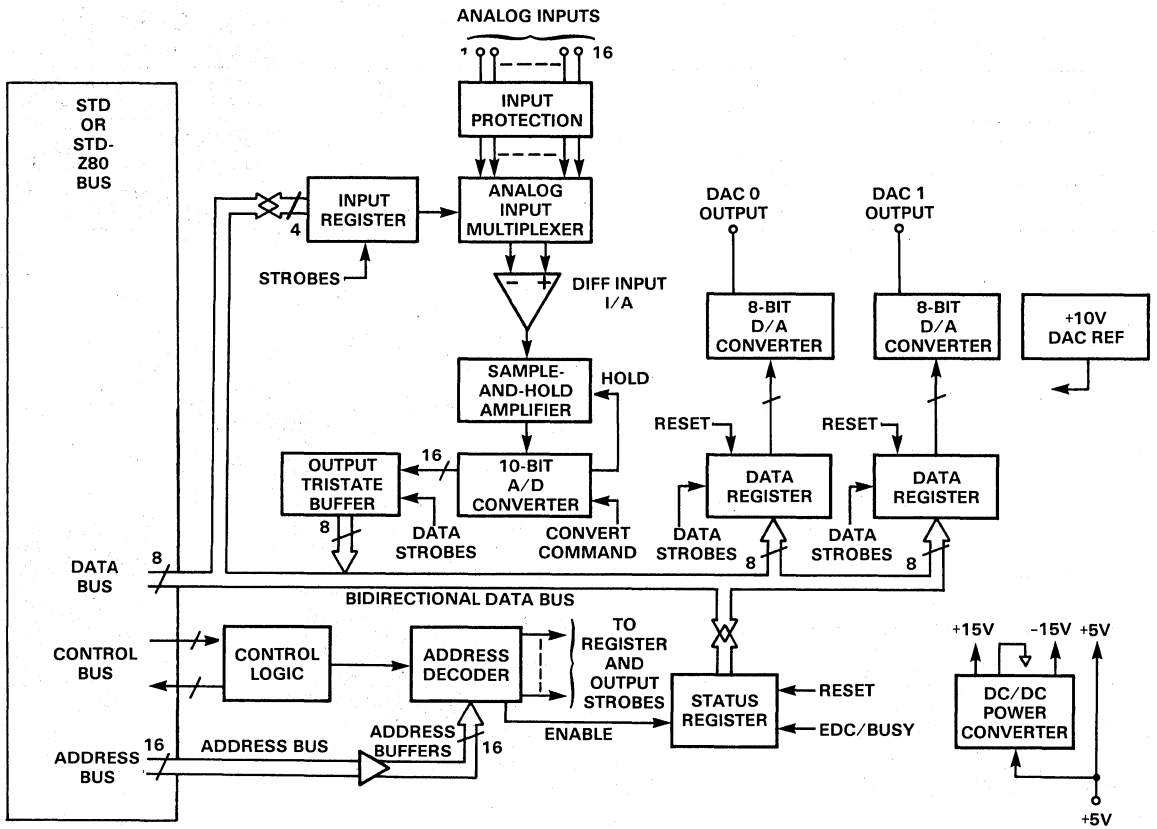


MD SERIES
INPUT/OUTPUT

The MDX-AIO has eight differential or 16 single-ended input capability while also providing for two channels of analog output with 8-bit resolution. The board also features input overvoltage protection to ± 35 volts. A Sample-and-Hold Amplifier is contained on the board along with a 10-bit A/D converter.

The MDX-AIO operates as a memory-mapped I/O system. Each board can be configured as a block of five contiguous memory locations, as shown in Table 1.

MDX-AIO BLOCK DIAGRAM



MEMORY MAP OF MDX-AIO

Table 1

BYTE ADDRESS	BYTE FORMAT								BYTE FUNCTION	OPERATION
	MSB B ₀	B ₁	B ₂	B ₃	B ₄	B ₅	B ₆	LSB B ₇		
X F X B	0	0	0	0	M ₀	M ₁	M ₂	M ₃	MUX ADDR & CONV. CMD	WRITE
X F X C	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	D ₈	LSB	LOWER ADC DATA BYTE	READ
X F X D	BUSY	0	0	0	0	0	MSB	D ₁	STATUS & UPPER ADC DATA BYTE	READ
X F X E	MSB ← DAC 0 DATA → LSB								DAC 0 DATA BYTE	WRITE
X F X F	MSB ← DAC 1 DATA → LSB								DAC 1 DATA BYTE	WRITE

NOTES:

1. "X" HEX address digits are user-selectable.
2. 0 bits are ignored on write and indeterminate on read.
3. Busy bit is "1" during conversions and "0" when done.
4. Writing the MUX number to location XFXB sets the input channel and initiates a conversion.

ANALOG INPUT SECTION

(All accuracy specifications typical at +25°C with $\pm 10V$ FSR unless otherwise noted)

Input Channels	16 Single-Ended or 8 Differential
Input Protection	$\pm 35V$
Input Range	0V to 10V, $\pm 5V$, $\pm 10V$
Input Impedance	100M Ω min.
Instrument Amplifier Gain	1V/V
Input Bias Current	50nA
CMV Range	$\pm 10V$
CMRR @ 60Hz	60dB min.
ADC Resolution	10 Bits
Conversion Time	40 microseconds
Monotonicity	Guaranteed 0 to 50°C
Overall System Error	$\pm 0.15\%$ F.S.R.
Offset Error	Adjustable to Zero
Gain Error	Adjustable to Zero
Noise Error RTI	$\pm \frac{1}{2}$ LSB
Nonlinearity	± 1 LSB max.
Offset Drift	50ppm/°C
Gain Drift	100ppm/°C

ANALOG OUTPUT SECTION

(All accuracy specifications typical at +25°C with $\pm 10V$ FSR unless otherwise noted)

Output Channels	2
Resolution	8 Bits
Output Ranges	0V to 10V, $\pm 5V$, $\pm 10V$
Output Current	5mA @ $\pm 10V$
Settling Time (20V Step)	30 microseconds to $\pm \frac{1}{2}$ LSB
Monotonicity	Guaranteed 0 to +50°C
Nonlinearity	$\pm \frac{1}{2}$ LSB max.
Offset Error	Adjustable to Zero
Gain Error	Adjustable to Zero
Offset Drift	30 microseconds V/°C
Gain Drift	50ppm/°C

SYSTEM INTERRUPT UNITS (SIO) = 0

SYSTEM CLOCK

	MIN	MAX
MDX-AIO	250kHz	4.0MHz

STD BUS INTERFACE

Inputs:	One 74LS Load
Outputs:	$I_{OH} = -3$ mA min. at 2.4 volts
	$I_{OL} = 24$ mA min. at 0.5 volts

OPERATING TEMPERATURE RANGE

0°C to +60°C
5% to 95% R.H. without Condensation
25 to 32 inches of Mercury

STORAGE TEMPERATURE RANGE

-36°C to +85°C

POWER SUPPLY REQUIREMENTS

+5 volts $\pm 5\%$ at 750 mA max.

CARD DIMENSIONS

4.5 in. (11.43 cm) high by 6.50 in. (16.51 cm) long
0.48 in. (1.22 cm) max. profile thickness
0.062 in. (0.16 cm) printed-circuit-board thickness

CONNECTORS

Function	Configuration	Mating Connector
STD-Z80 BUS	56 pin 0.125 in. centers	PRINTED CIRCUIT Viking 3VH28/1CE5 WIRE WRAP Viking 3VH28/1CND5 SOLDER LUG Viking 3VH28/1CN5
Analog I/O	34-pin	3M Type Ribbon Cable Connector ADI P/N AC1562

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
MDX-AIO	Module with Operation Manual less mating connectors.	MK77654
	MDX-AIO Operations Manual only	MK79775

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MD SERIES I/O CARDS

MDX-A/D12

MK77655-0

FEATURES

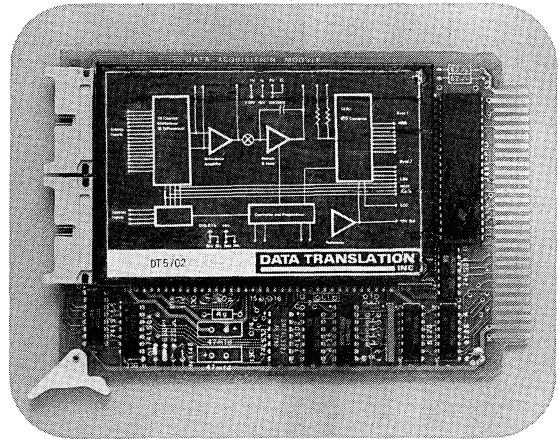
- STD-Z80 BUS compatible
- 12-bit A/D Converter
- 16 Single-Ended or Eight Differential Input Channels
- Sample and Hold
- Two Analog Input Ranges
± 5 Volts, 0 to 5 Volts
- Provisions for input channel expansion
- Address programmable

DESCRIPTION

The Analog-to-Digital Converter Family, MDX-A/D12, encompasses five different modules, each of which has different input ranges. The boards allow for high-level, wide range, and wide range isolated inputs.

The MDX-A/D12 board provides 16 single-ended or eight differential input channels. It also has the capability for expansion up to 64 single-ended or 32 differential input

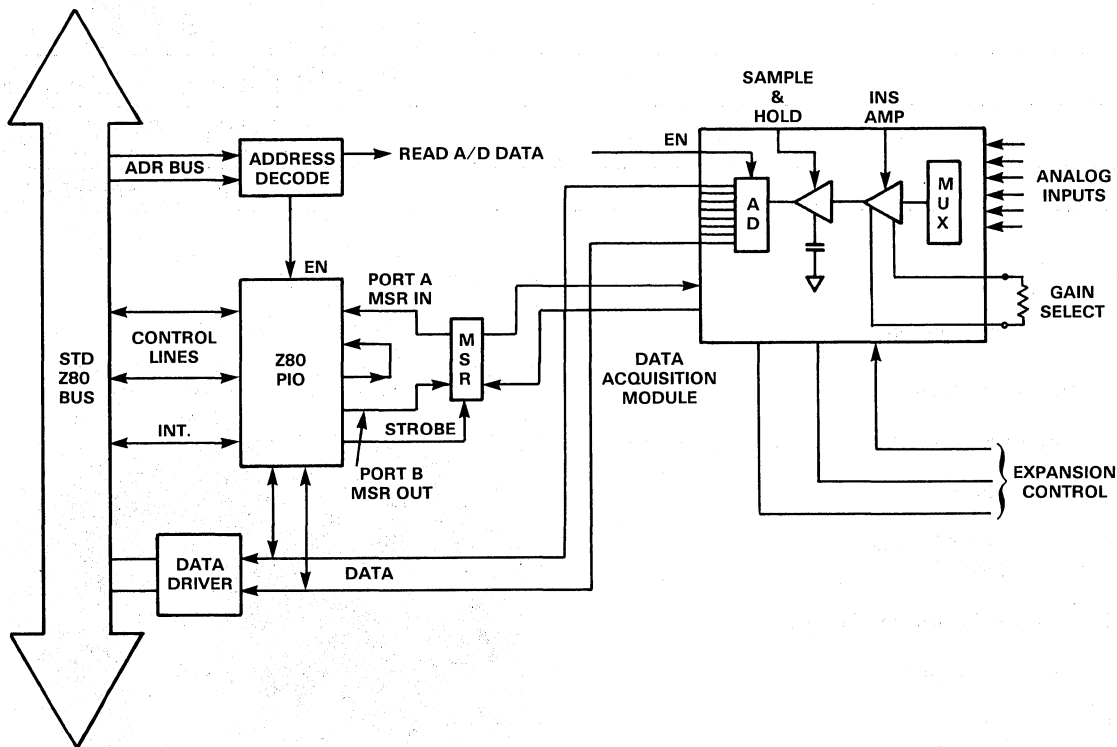
MDX-A/D 12 BOARD PHOTO



MD SERIES
INPUT/OUTPUT

channels. The full-scale input ranges are ± 5 volts or 0 to 5 volts. These are jumper-selectable. Throughput for this module is 33 microseconds.

MDX-A/D12 BLOCK DIAGRAM



ANALOG INPUT PARAMETERS

Number of Channels: 16 single-ended or eight differential (jumper selectable)

Input Impedance: 100 megohm

Sample-and-Hold Aperture Uncertainty: 10 nanoseconds

Conversion Resolution: 12 bits

Inherent Quantizing Error: $\pm 1/2$ LSB

Stability: ± 25 ppm/ $^{\circ}$ C FSR

Linearity: $\pm 1/2$ LSB

Analog-Input-System Accuracy: $\pm 0.03\%$ FSR

Throughput: 33 microseconds

DIGITAL PARAMETERS

WORD SIZE

Data: 8 bits

I/O Addressing: 8 bits

I/O ADDRESSING

On board, upper five bits programmable

INTERRUPTS

Vectored interrupts generated. Interrupt vector programmable upon initialization. Daisy-chained interrupt priority. Selected bit channels can be masked out under program control.

SYSTEM INTERRUPT UNITS (SIU) = 1

SYSTEM CLOCK

	MIN	MAX
MDX-A/D12 Family	250 kHz	2.5 MHz

STD BUS INTERFACE

Inputs: One 74LS Load max.

Outputs: $I_{OH} = -3$ mA min. at 2.4 Volts

$I_{OL} = 24$ mA min. at 0.5 volts

OPERATING TEMPERATURE RANGE

0°C to 60°C

POWER SUPPLY REQUIREMENTS

+5V ± 5% at 500mA
 + 12V ± 5% at 75mA

CARD DIMENSIONS

4.5 in. (11.43cm) high by 6.50 in. (16.51cm) long
 0.48 in (1.22cm) maximum profile thickness
 0.062 in (0.16cm) printed-circuit-board thickness

CONNECTORS

Function	Configuration	Mating Connector
STD-Z80 BUS	56-pin 0.125 in. centers	PRINTED CIRCUIT Viking 3VH28/1CE5 WIRE WRAP Viking 3VH28/1CND5 SOLDER LUG Viking 3VH28/1CN5
*ANALOG CONN	20-pin	3M type 3421

*MDX-A/D12 may have up to two 20-pin 3M-type connectors. Connector J1 is used for connection of analog input signals and EXT TRIG INPUTS. Connector J2 is used for multiplexer channel expansion.

**MD SERIES
INPUT/OUTPUT**

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
MDX-A/D12	High-Level 12-bit, 16-channel SE (8 channel DI) A/D. Less mating connector with Operations Manual.	MK77655-0
	MDX-A/D12 Operations Manual Only	MK79774

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MD SERIES I/O CARDS

MDX-D/A 8

MK77666-0

FEATURES

- STD-Z80 and STD BUS compatible
- 8 Bit D/A Converter
- Four independent channels
- Output voltage ranges of $\pm 5V$, 0 to 5V, $\pm 10V$, 0 to 10V
- Output current range of 4 to 20 mA
- 15V optional models available
- Programmable address
- 2.5 and 4.0MHz Operation

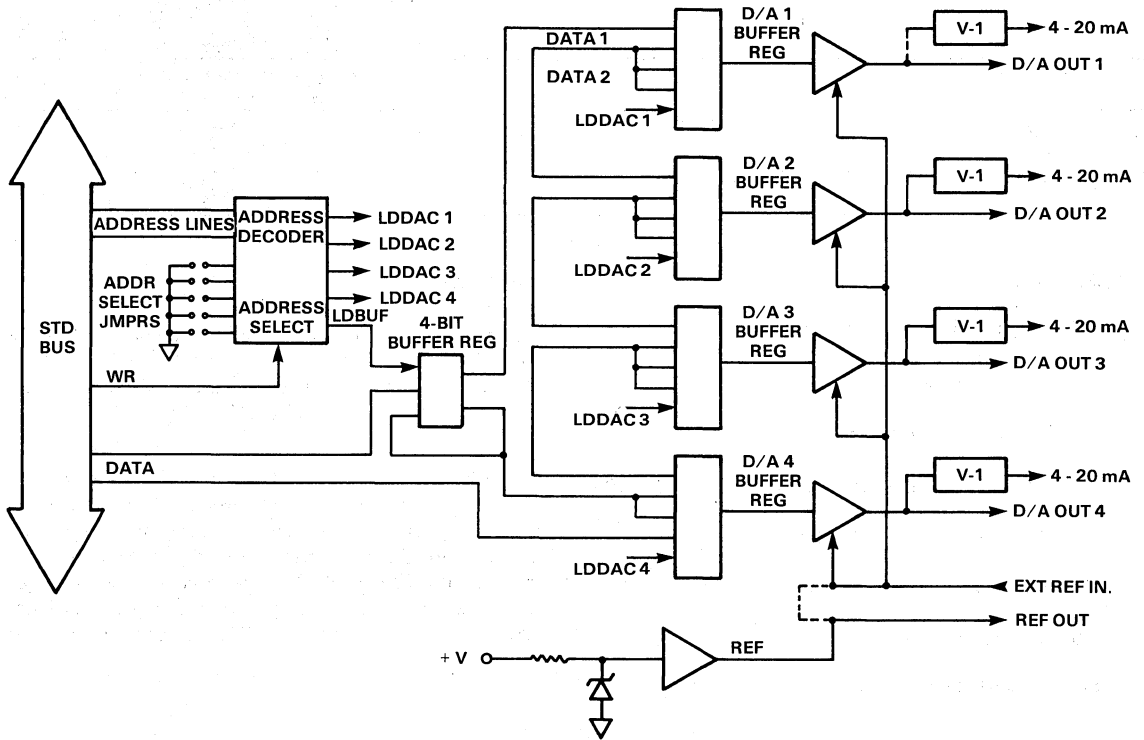
DESCRIPTION

Designed as a part of the MD Series Analog I/O systems, the MDX-D/A8 features four completely independent analog output channels. Each channel has user-selectable output ranges of $\pm 5V$ and 0 to 5V.

The MDX-D/A8 can be used as either a memory-mapped peripheral or as an I/O port through a user-selectable jumper option. When used in the memory-mapped environment, the device base address can be assigned any value in the 8000H to FFF8H memory address space. When used as an I/O port, the base port address can be assigned any address in the 0000H to 00F8H I/O port address space.

MD SERIES
INPUT/OUTPUT

MDX-D/A 8 BLOCK DIAGRAM



ANALOG OUTPUT PARAMETERS

Resolution: 8 bits

No. of Channels: 4

Linearity: $\pm \frac{1}{2}$ LSB
 $\pm 0.2\%$ FSR

Differential Linearity: $\pm 1/2$ LSB

Gain and Offset Error: Adjustable to Zero

Gain Drift: ± 60 PPM/ $^{\circ}$ C

Offset Drift: ± 10 PPM/ $^{\circ}$ C unipolar
 ± 30 PPM/ $^{\circ}$ C bipolar

Settling Time: 35 microseconds to 0.01% FSR (10-volt step)

Slew Rate: 0.33V/microsecond

Output Voltage Range: ± 5 V, 0 to 5V (MDX-D/A 8)

DC Output Impedance: < 0.1 ohm

WORD SIZE

Data: 8 bits
 I/O Addressing: 8 bits

I/O ADDRESSING OR MEMORY ADDRESSING

On-board programmable

SYSTEM CLOCK

	MIN.	MAX.
MDX - D/A8	250 kHz	2.5 MHz

SYSTEM INTERRUPT UNITS (SIU) = 0

STD BUS INTERFACE

Inputs: One 74LS load max.
 Outputs: I_{OH} = -3 mA min. at 2.4 volts
 I_{OL} = 24 mA max. at 0.5 volts

OPERATING TEMPERATURE RANGE

0°C to 60°C

POWER SUPPLY REQUIREMENTS

+5V ± 5% at 550 mA
 ± 15V or ± 12V ± 5% at 50 mA and load current

CARD DIMENSIONS

4.5 in. (11.43 cm) high by 6.50 in. (16.51 cm) long
 0.48 in. (1.22 cm) maximum profile thickness
 0.062 in. (0.16 cm) printed-circuit-board thickness

CONNECTORS

Function	Configuration	Mating Connector
STD-Z80 BUS	56-pin 0.125 in. centers	PRINTED CIRCUIT Viking 3VH28/ 1CE5 WIRE WRAP Viking 3VH28/ 1CND5 SOLDER LUG Viking 3VH28/ 1CN5
ANALOG CONN	20-Pin	3M type 3421

MD SERIES
INPUT/OUTPUT

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
MDX-D/A8	4-Channel 8-bit D/A converter with manual less mating connector	MK77666
	MDX-D/A8 Operation Manual Only	MK79824

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MD SERIES I/O CARDS

MDX-D/A 12

MK77665-0

FEATURES

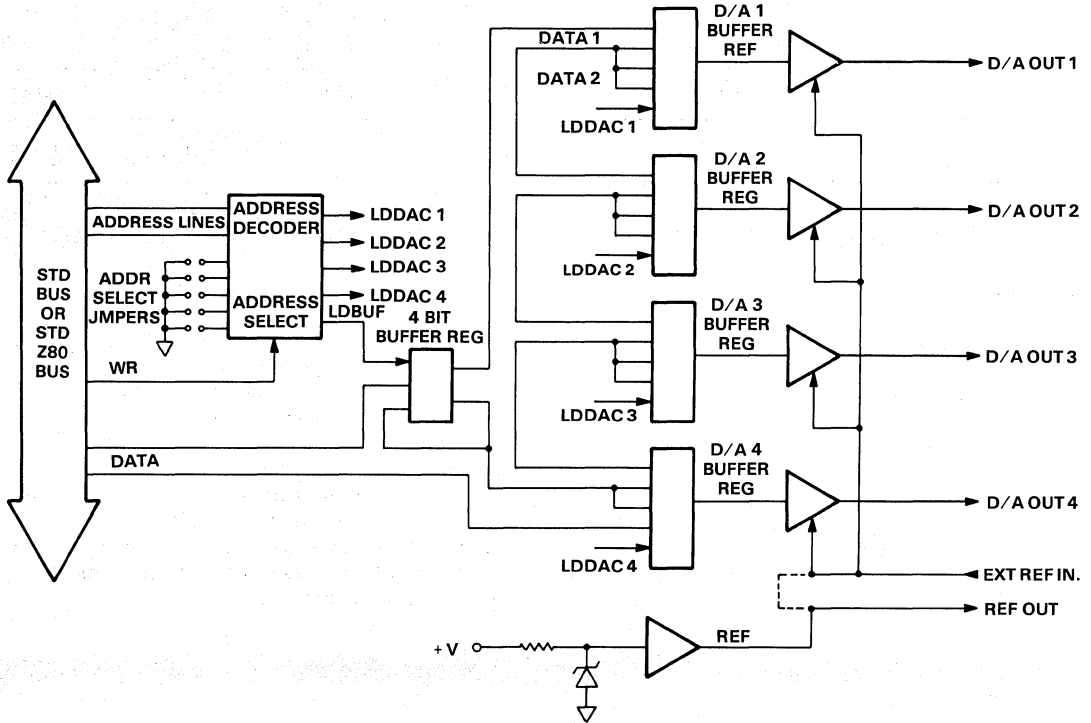
- STD-Z80 BUS compatible
- 12-bit D/A converter
- Four independent channels
- Output voltage ranges of $\pm 5V$, 0 to 5V, $\pm 10V$, 0 to 10V
- Programmable address
- Both 2.5MHz and 4.0MHz

DESCRIPTION

Designed as a part of the MD Series Analog I/O systems, the MDX-D/A 12 features four completely independent analog output channels. Each channel has users-selectable output ranges of $\pm 5V$ and 0 to 5V. The MDX-D/A 12 can be used as either a memory-mapped peripheral or as an I/O port through a user-selectable jumper option. When used in the memory-mapped environment, the device base address can be assigned any value in the 8000_H to $FFF8_H$ memory address space. When used as an I/O port, the base port address can be assigned any address in the $00F8_H$ to $00FF_H$ I/O port address space.

MD SERIES
INPUT/OUTPUT

MDX-D/A 12 BLOCK DIAGRAM



ANALOG OUTPUT PARAMETERS

Resolution: 12 bits

No. of channels: 4

Output Voltage Range: $\pm 5V$, 0 to 5V

Linearity: $\pm 1/2$ LSB
 $\pm 0.02\%$ FSR

Differential Linearity: $\pm 1/2$ LSB

D.C. Output Impedance: < 0.1 ohm

Gain and Offset Error: Adjustable to zero

Gain Drift: ± 30 ppm/ $^{\circ}C$

Offset Drift: ± 3 ppm/ $^{\circ}C$ unipolar
 ± 18 ppm/ $^{\circ}C$ bipolar

Settling Time: 35 microseconds to 0.01% FSR (10 volt step)

Slew Rate: 0.33 V/microsecond

DIGITAL PARAMETERS

WORD SIZE

Data: 8 bits

I/O Addressing: 8 bits

I/O ADDRESSING OR MEMORY ADDRESSING

On-board programmable

INTERRUPTS

No interrupts are generated

SYSTEM INTERRUPT UNITS (SIU) = 0

SYSTEM CLOCK

	MIN	MAX
MDX-D/A 12	250kHz	2.5MHz

STD BUS INTERFACE

Inputs: One 74LS load max.
 Outputs: $I_{OH} = -3\text{mA}$ min. at 2.4 Volts
 $I_{OL} = 24\text{mA}$ min. at 0.5 Volts

OPERATING TEMPERATURE RANGE

0°C to 60°C

POWER SUPPLY REQUIREMENTS

+5V $\pm 5\%$ at 550mA

CARD DIMENSIONS

4.5 in (11.43cm) high by 6.50 in. (16.51cm) long
 0.48 in (1.22cm) maximum profile thickness
 0.062 in (0.16cm) printed-circuit-board thickness

CONNECTORS

Function	Configuration	Mating Connector
STD-Z80 BUS	56-pin 0.125 in. centers	PRINTED CIRCUIT Viking 3VH28/ 1CE5 WIRE WRAP Viking 3VH28/ 1CND5 SOLDER LUG Viking 3VH28/ 1CN5
ANALOG CONN	20-pin	3M type 3421

**MD SERIES
INPUT/OUTPUT**

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
MDX-D/A 12	4-channel 12-bit D/A converter with manual less mating connector.	MK77665-0
	MDX-D/A 12 Operation Manual Only	MK79824

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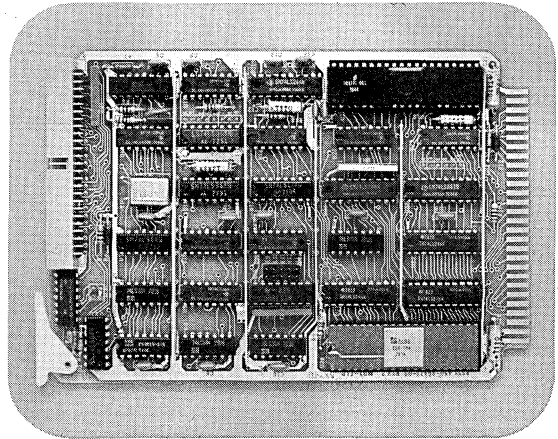
MD SERIES I/O CARDS

MDX-FLP MK77652-0

FEATURES

- STD-Z80 BUS compatible
- One to four drives; four software-controlled select lines
- 5-inch or 8-inch drives, single- or dual-sided, jumper-selectable. All drives connected to one MDX-FLP board must be the same type
- Single-density operation
- Soft-sector operation including variable-length sectors
- Compatibility with IBM 3740 or other formats
- Single-sector, multi-sector or full-track data transfers
- Automatic track seek with verification capability
- Diskette initialization/formatting capability
- Software-programmable step rate, head settling and engage times
- DMA or programmed data transfer
- Interrupt-driven or polled operation
- Automatic CRC checking and generation on read and write operations.
- 8-inch drives supported under FLP-80DOS and MITE-80 software; 5-inch drives under MITE-80
- Port addresses jumper-selectable to a block of eight anywhere in the address space
- 2.5 MHz operation (system clock)
- Provision for DMA daisy chain operation (simultaneous operation of multiple DMA devices requires on-board jumper and backplane modification)

MDX-FLP BOARD PHOTO



MD SERIES
INPUT/OUTPUT

DESCRIPTION

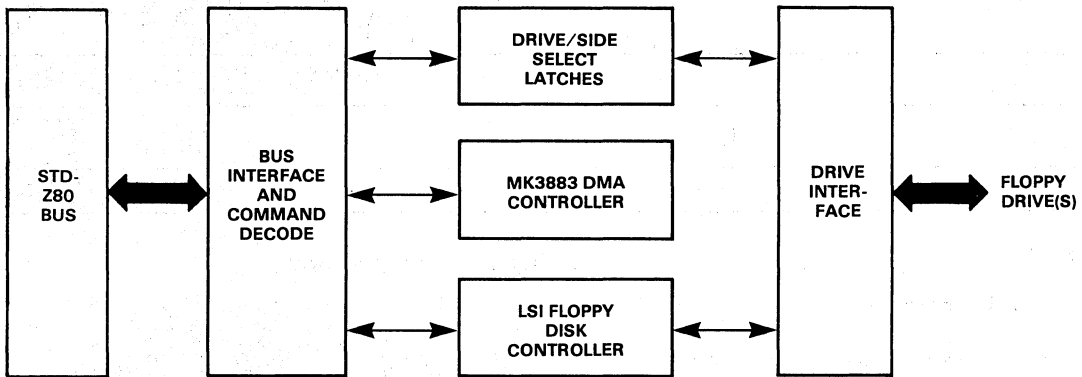
The single MDX-FLP board provides all required controlling/formatting/interfacing logic between the STD-Z80 BUS and one to four floppy disk drives. The board is based upon an LSI controller chip and MK3883 DMA controller.

The MDX-FLP module is compatible with the following floppy disk drives.

Siemens FDD 100-8, 200-8, 100C, 200C.
Shugart Associates SA800, SA850, SA400, SA450.
Pertec FD600, FD650, FD200, FD250.
Memorex 550, 552.

and with any equivalent drive which utilizes the signals shown in Table 1. (All signals are TTL; directions are referenced to the board.)

BLOCK DIAGRAM



FLOPPY DISC INTERFACE SIGNALS

Table 1

Signal	Direction	MDX-FLP Pin
Drive Select 1,2,3,4	Out	26,28,30,32
Side Select	Out	14 and 16
Step	Out	36
Write Data	Out	38
Write Gate	Out	40
Direction	Out	34
Head Load	Out	18
Read Data	In	46
Index	In	24(5") or 20(8")
Track 0	In	42
Write Protect	In	44
Drive Ready	In	22

The MDX-FLP board will work with 5-inch or 8-inch single- or dual-sided, single-density drives; however, 5- and 8-inch drives may not be driven by the same board.

MICROPROCESSOR INTERFACE

Connector, signals, and pinouts are STD-Z80 BUS compatible. With the addition of jumper E16, the Bus Acknowledge Out Signal is presented at pin 40 (STATUS 0) for DMA daisy-chain operation.

PORT MAP

Jumpers E9 through E13 select the high-order port address on A7-A3 to which the board will respond. Thus the board uses a block of eight contiguous port addresses, which are arranged for maximum compatibility with FLP-80DOS. Port utilization is as shown in Table 2.

PORT UTILIZATION

Table 2

A2	A1	A0	
0	0	0	DMA Controller
0	0	1	Unused
0	1	0	Board Status
0	1	1	Drive Selection
1	0	0	Controller Command/Status
1	0	1	Track Register
1	1	0	Sector Register
1	1	1	Data Register

WORD SIZE

Data: 8 bits
I/O Addressing: 8 bits

I/O ADDRESSING

On-board programmable - See Table 2.

INTERRUPTS

Vectored interrupts generated. Interrupt vector programmable upon initialization. Daisy chained interrupt priority.

SYSTEM INTERRUPT UNITS (SIU) = 1

SYSTEM CLOCK

	MIN	MAX
MDX-FLP	250kHz	2.5MHz

STD BUS INTERFACE

Inputs One 74LS Load Max.
 Outputs $I_{OH} = 3 \text{ mA min. at 2.4 volts}$
 $I_{OH} = 24 \text{ mA min. at 0.5 volts}$

POWER SUPPLY REQUIREMENTS

+5 volts $\pm 5\%$ at 1.2A max.
 +12 volts $\pm 5\%$ at 10mA max.
 -12 volts $\pm 5\%$ at 4mA max.

OPERATING TEMPERATURE RANGE

0°C to 60°C

CARD DIMENSIONS

4.5 in. (11.43cm) high by 6.50 in. (16.51 cm) long
 0.48 in. (1.22cm) maximum profile thickness
 0.062 in. (0.16cm) printed-circuit-board thickness

CONNECTORS

Function	Configuration	Mating Connectors
STD-Z80 BUS	56-pin	PRINTED CIRCUIT Viking 3VH28/ 1CE5
	0.125 in. centers	WIRE WRAP Viking 3VH28/ 1CND5 SOLDER LUG Viking 3VH28/ 1CN5
Drive Interface	50-pin	Ansley 609-5000M w/o strain relief
	0.100 in. centers	Ansley 609-5001M with strain relief

**MD SERIES
INPUT/OUTPUT**

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
MDX-FLP	Module with Operation Manual less mating connectors. 2.5MHz version	MK77652-0
	MDX-FLP Operations Manual Only	MK79639

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MD SERIES I/O CARDS

MDX-PIO

MK77650-0, MK77650-4

FEATURES

- STD-Z80 BUS compatible
- Four 8-bit I/O ports with two handshake lines per port
- All I/O lines fully buffered
- I/O lines TTL-compatible with provision for termination resistor networks
- Jumper options for inverted or non-inverted handshake
- Two 8-bit ports capable of true bidirectional I/O
- Programmable In only, Out only, or Bidirectional
- Output data buffers selectable to provide inverted or non-inverted drive capability
- Interrupt-driven programmability
- Address strap-selectable
- 4 MHz option
- Fully buffered for MD Series expandability

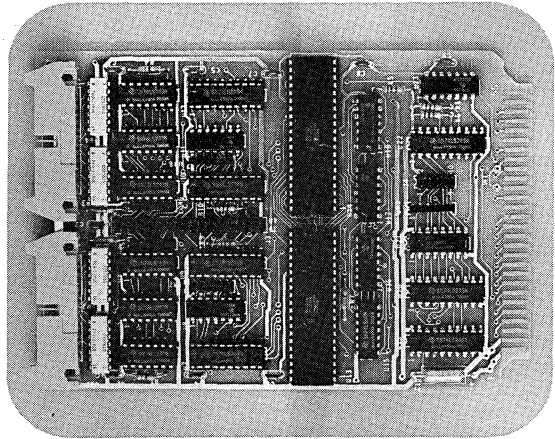
DESCRIPTION

The parallel I/O controller (MDX-PIO) is a highly versatile unit designed to provide a variety of methods for inputting and outputting data from the MD Series microcomputer system. The system is designed around two Mostek MK3881 Z80-PIO parallel I/O controllers which give four independent 8-bit I/O ports with two handshake (data transfer) control lines per port. The Z80-PIO's are designated PIO1 and PIO2. Each has an I/O port pair designated A and B. Each port pair of each PIO have similar output circuitry.

All I/O lines are buffered and have provisions for termination resistors on board. All port lines are brought to two 26-pin connectors, two ports per connector.

Figure 1 illustrates in block diagram form the major functional elements of port pair A and B of PIO1. These elements can be defined as the resistor termination networks, data buffers, port configuration control, MK3881

MDX-PIO BOARD PHOTO



MD SERIES
INPUT/OUTPUT

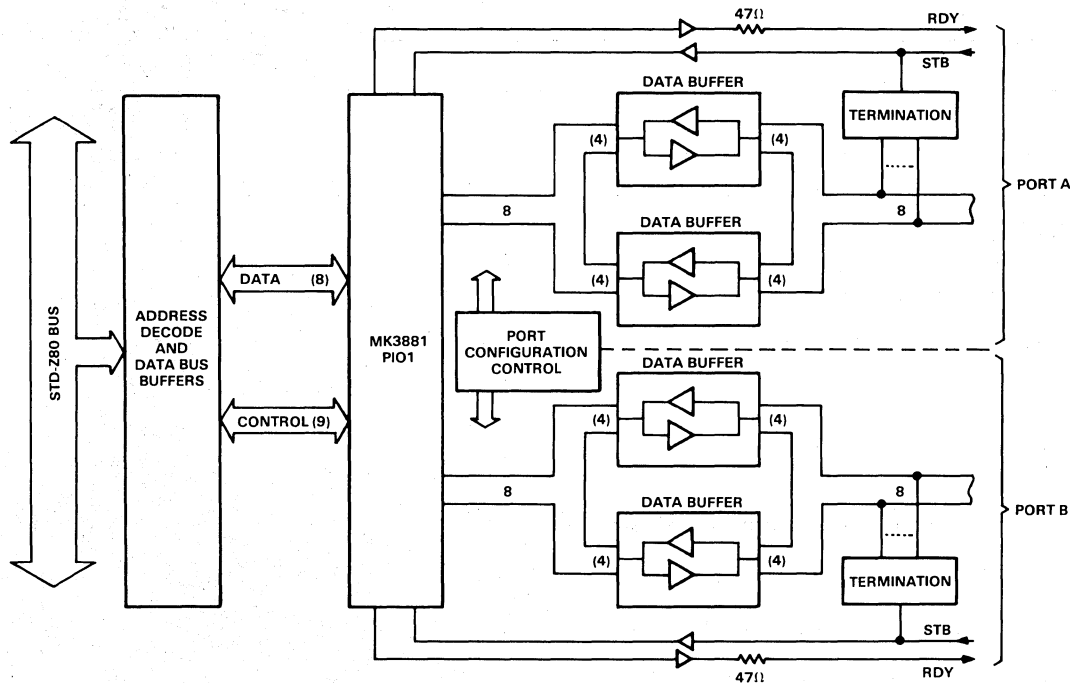
PIO, and address decode and data bus buffers. Input and output from the ports are provided through J1, a 26-pin connector. This connector provides data paths for the two ports and their respective handshake signals.

One 14-pin socket is provided per port for resistor dual inline packages so that terminations may be placed on the data lines. A parallel termination is provided for each 8-bit port data line plus the input strobe (STB) handshake line. The MDX-PIO is normally shipped with 1K pullup terminators. In addition to the parallel termination resistors, the ready (RDY) handshake output line is series-terminated with a 47 Ω resistor. This is used to damp and reduce reflections on this output line.

Port A and B data bus lines are buffered using quadruple non-inverting transceivers. The buffers can be configured using port configuration jumpers to provide fixed Input, fixed Output or Bidirectional (Port A only) signals. Further, the transceivers are configured such that port direction can be selected in 4-bit sections. The transceivers are mounted in sockets so that they can be easily replaced with their complements in order to achieve a polarity change if desired.

MDX-PIO BLOCK DIAGRAM FOR PIO1 (PIO2 IS IDENTICAL)

Figure 1



The handshake lines are also fully buffered. The port configuration control provides jumper options to independently control the polarity or "sense" of each handshake line so as to further ease the interfacing between the MDX-PIO and peripheral devices.

The MK3881 PIO is the heart of the module. This circuit is a fully-programmable two-port device which provides a wide range of configuration options. Any one of four distinct modes of operation can be selected for a port. They are byte output, byte input, byte bidirectional (Port A only), and bit control mode. The PIO also automatically generates all handshaking signals in all the above modes.

The PIO permits total interrupt control so that full usage of the Z80 interrupt capabilities can be utilized during I/O transfers. Also, the PIO can be programmed to interrupt the CPU on the occurrence of a specified status condition in a specific peripheral device. The PIO circuit will provide vectored interrupts and maintain the daisy chain priority interrupt logic compatible with the STD-Z80 BUS.

The address decoding, interface and bus management for the board are performed by the address decode and data bus circuit. Each MDX-PIO port has two addresses, one for Control and one for Data. A total of eight addresses are utilized per board. These addresses are defined in Table 1.

MDX-PIO ADDRESSES

Table 1

	PIO1		PIO2	
	PORT A	PORT B	PORT A	PORT B
Data	XX0g	XX2g	XX4g	XX6g
Control	XX1g	XX3g	XX5g	XX7g

The XX symbols stand for the upper five bits of the I/O channel address. These bits are jumper-selectable on the MDX-PIO board in order to provide address-selectable fully-decoded ports.

The circuitry for the other two ports provided by PIO2 is identical to PIO1. The port configuration logic, buffers, termination and pin out on connector J2 is duplicated for PIO2. These two ports share the address-decode and data-bus-buffer circuitry with PIO1. The only differences are in the address decoding as given in the port address table, and PIO2 is lower priority in the daisy-chain interrupt structure.

WORD SIZE

Data: 8 bits
I/O Addressing: 8 bits

I/O ADDRESSING

On-board programmable - See Table 1

I/O CAPACITY

Four parallel 8-bit ports. On-board jumper, selectable in 4-bit bytes as either In only, Out only, or Bidirectional (Port 1A or 2A only). Automatic handshake provided with each port.

I/O DRIVERS

Table 2 lists the pin-compatible I/O drivers which can be used in the MDX-PIO.

I/O DRIVERS

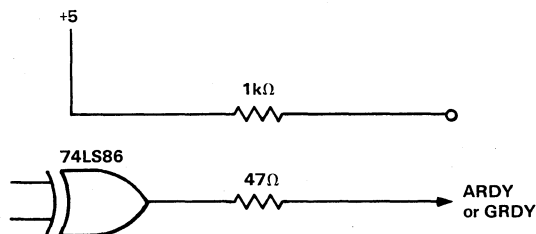
Table 2

Signals	Type	Output	Sink Current (mA)
I/O Ports 1A and 2A	*74LS244	Non-Inverting Tri-State Bidirectional	24
	74LS241	Inverting Tri-State Bidirectional	24
I/O Ports 1B and 2B	*74LS243	Non-Inverting Tri-State Bidirectional	24
	74LS242	Non-Inverting Tri-State Bidirectional	24
Handshake: RDY	74LS86	Inverting/Non-Inverting (strap selectable)	8

*These devices are supplied with the board. They may be exchanged with the other unit listed to provide the alternate signal polarity.

TERMINATORS

1k ohm resistors on all I/O port lines.



INTERRUPTS

Vectored interrupts generated. Interrupt vector programmable upon initialization. Daisy-chained interrupt priority. Selected bit channels can be masked out under program control.

SYSTEM INTERRUPT UNITS (SIU) = 2

SYSTEM CLOCK

	MIN.	MAX.
MDX-PIO	250kHz	2.5 MHz
MDX-PIO-4	250kHz	4.0 MHz

STD BUS INTERFACE

Inputs: One 74LS Load max.
Outputs: $I_{OH} = -3mA$ min. at 2.4 Volts
 $I_{OL} = 24mA$ min. at 0.5 Volts

OPERATING TEMPERATURE RANGE

0°C to 60°C

POWER SUPPLY REQUIREMENTS

+5 volts \pm 5% at 1.1A max.

CARD DIMENSIONS

4.5 in. (11.43cm) high by 6.50 in. (16.51 cm) long
0.48 in. (1.22cm) maximum profile thickness
0.062 in. (0.16cm) printed-circuit-board thickness

CONNECTORS

Function	Configuration	Mating Connector
STD-Z80 BUS	56-pin	PRINTED CIRCUIT Viking 3VH28/ 1CE5
	0.125 in. centers	WIRE WRAP Viking 3VH28/ 1CND5 SOLDER LUG Viking 3VH28/ 1CN5
Parallel I/O	26-pin 0.100 in. centers	FLAT RIBBON Ansley 609- 2600M DISCRETE WIRES Winchester PGB26A (housing) Winchester 100- 70020S (contacts)

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
MDX-PIO	Module with Operation Manual less mating connectors (2.5MHz version).	MK77650-0
MDX-PIO-4	Module with Operation Manual less mating connectors (4.0 MHz version).	MK77650-4
	MDX-PIO Operations Manual only	MK79606

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MD SERIES I/O CARDS

MDX-SIO

MK77651-0, MK77651-4

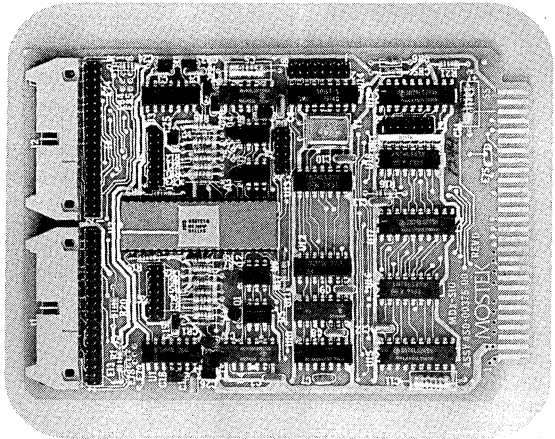
FEATURES

- STD-Z80 BUS compatible
- Two independent full-duplex channels
- Independent programmable Baud-rate clocks
- Asynchronous data rates-110 to 19.2k bits per second
- Receiver data registers quadruply-buffered
- Transmitter data registers double-buffered
- Asynchronous operation
- Binary synchronous operation
- HDLC or SDLC operation
- Both CRC-16 and CRC-CCITT (-0 and -1) hardware implemented
- Modem control
- Operates as DTE or DCE
- Serial input and output as either RS-232 or 20mA current loop
- Current loop optically isolated
- Current loop selectable for either active or passive mode
- Address programmable
- 4 MHz option

DESCRIPTION

The Serial Input/Output Module, MDX-SIO, is designed to be a multiprotocol asynchronous or synchronous I/O module for the STD-Z80 BUS. The module is designed around the Mostek MK3884 Z80-SIO which provides two full duplex, serial data channels. Each channel has an independent programmable baud-rate clock generator to increase module flexibility. The MDX-SIO is capable of handling asynchronous, synchronous, and synchronous bit-oriented protocols such as Bi-SYNC, SDLC, HDLC and

MDX-SIO BOARD PHOTO



MD SERIES
INPUT/OUTPUT

virtually any other serial protocol. It can generate CRC codes in any synchronous mode and can be programmed by the CPU for any traditional asynchronous format. The serial input and output data are fully buffered and are provided at the connector as either 20mA current loop or RS-232-C levels. A modem control section is also provided for handshaking and status. The MDX-SIO module can be jumper-configured as a data terminal (DTE) or as a modem (DCE) in order to facilitate a variety of interface configurations.

Figure 1 is a block diagram of the MDX-SIO module. It consists of five main elements. They are the channel configuration headers, line drivers and receivers, MK3884 Z80-SIO, programmable baud-rate generators, and address decode and data bus buffers. Input and output to the board is provided via two 26-pin connectors. One connector is dedicated for each channel.

Several features are available as options that are selected via the channel configuration headers, which are used to select the orientation of the data communication interface and the mode of the 20mA current loop. The MDX-SIO can be selected to act as either a terminal or processor (Data

Terminal Equipment-DTE) or as the modem (Data Communications Equipment-DCE). The header allows reconfiguration of both data interchange and modem control signals. This allows increased flexibility necessary to link different hardware elements in OEM data-link systems and networks. The module is shipped from the factory wired as a DTE interface.

The MDX-SIO has different selectable options for the 20mA current loop. Receiver and transmitter functions can be reconfigured on the module to allow reorientation of these signals. Also, the receive and transmit circuits can be selected to function in either an active or passive mode. In the active mode, the MDX-SIO module provides the 20mA current source. In the passive mode, the module requires that the loop current be provided. The latter is the same mode as that of a Teletype.

An RS-232-C and 20mA current loop interface circuit is used to provide the necessary level shifting and signal conditioning between the MK3884 Z80-SIO and the connector. These line drivers and receivers provide the correct electrical signal levels, slew rate, and impedance for interfacing RS-232-C and 20mA current loop peripherals. Additionally, optical isolation is provided for both transmit and receive circuits in the 20mA current loop mode.

The Mostek MK3884 Z80-SIO is the central element of this module. It is a multifunction component designed to satisfy a wide variety of serial data communications requirements in microcomputer systems. Its basic role is that of a serial-to-parallel, parallel-to-serial converter/controller, but

within that role it is configured by software programming so that its function can be optimized for a given serial data communications application. The MK3884 provides two independent full duplex channels, A and B.

Asynchronous operation (Channel A and B)

- 5, 6, 7, or 8 bits/character
- 1, 1½ or 2 stop bits
- Even, odd or no parity
- x1, x16, x32 and x64 clock modes
- Break generation and detection
- Parity, Overrun and Framing error detection

Binary Synchronous operation (Channel A only)

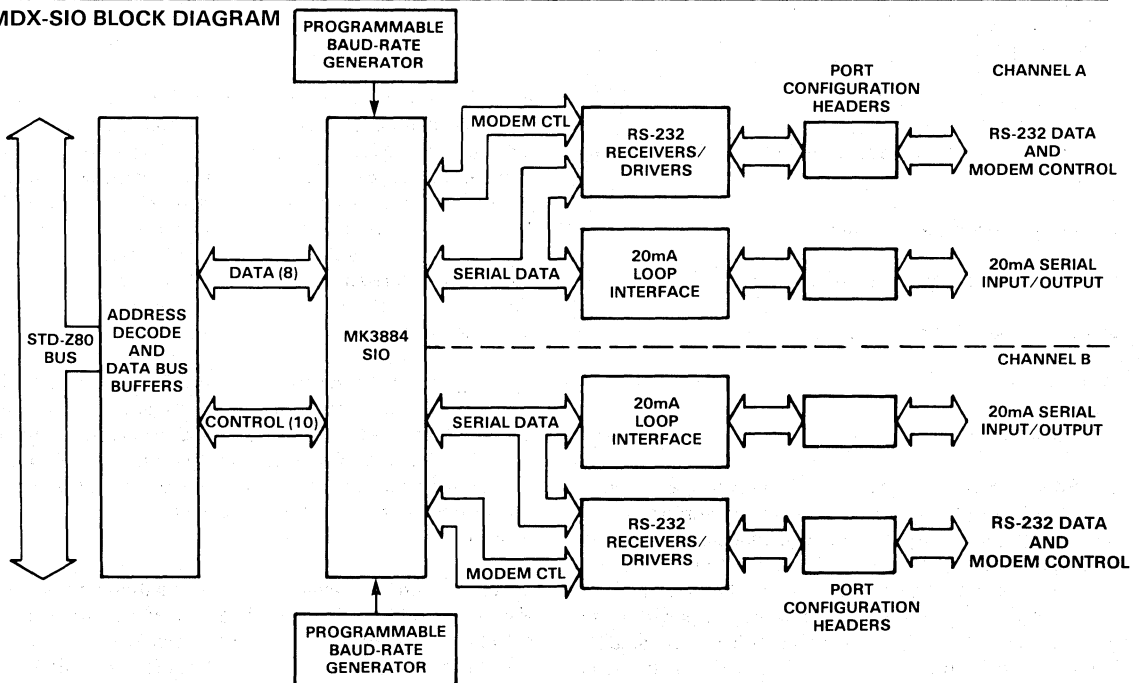
- One or two Sync characters in separate registers
- Automatic Sync character insertion
- CRC generation and checking

HDLC or SDLC operation (Channel A only)

- Automatic Zero Insertion and Deletion
- Automatic Flag Insertion
- Address Field Recognition
- I-Field Residue Handling
- Valid receive messages protected from overrun
- CRC Generation and Checking

The MK3884 also provides modem control inputs and outputs as well as daisy chain priority interrupt logic. Eight different interrupt vectors are generated by the SIO in response to various conditions affecting the data communications channel transmission and reception.

MDX-SIO BLOCK DIAGRAM



Address decoding, STD-Z80 BUS interface and bus management for the module are performed by the Address Decode and Data Bus circuit. The MDX-SIO contains command registers that are programmed to select the desired operational mode. The addressing scheme is as follows:

XXXXXX 00 Channel A Data
 XXXXXX 01 Channel A Control Status

XXXXXX 10 Channel B Data
 XXXXXX 11 Channel B Control Status

XXXXXX indicates the binary code necessary to represent which one of the 64 port addresses is selected by on-board strapping.

Each channel has an individual programmable baud-rate generator. The x1 multiplier on the Z80-SIO must be used in the synchronous modes. The x16, x32 or x64 Z80-SIO clock rate can be specified for asynchronous mode. Table 1 indicates the possible Baud rates available for both operation modes with the Z80-SIO Data Rate Multipliers.

Table 1

SYNCHRONOUS	BAUD RATE (HZ)			
	X1	X16	X32	X64
800	50	25	12.5	
1200	75	37.5	18.75	
1760	110	55	27.50	
2152	134.5	67.25	33.63	
2400	150	75	37.50	
4800	300	150	75	
9600	600	300	150	
19200	1200	600	300	
28800	1800	900	450	
32000	2000	1000	500	
38400	2400	1200	600	
57600	3600	1800	900	
76800	4800	2400	1200	
115200	7200	3600	1800	
153600	9600	4800	2400	
307200	19200	9600	4800	

WORD SIZE

Data: 8 bits
 I/O addressing: 8 bits

I/O CAPACITY

Serial - Two full duplex serial ports. Channel A is capable of synchronous and asynchronous operation. Channel B is asynchronous only. Special control registers and circuitry to permit implementation of SDLC, BiSync, MonoSync, HDLC. Other formats can be programmed on Channel A only.

I/O ADDRESSING

On board upper six bits programmable

SERIAL COMMUNICATION INTERFACE

Signal	20mA Loop	RS-232-C
Transmitted data	Output	Output
Received data	Input	Input
Data Terminal Ready (DTR)		Input/Output
Request to Send (RTS)		Input/Output
Clear to Send (CTS)		Output/Input
Carrier Detect (CDET)		Output/Input

MD SERIES INPUT/OUTPUT

INTERRUPTS

Generates vectored interrupts to eight different locations corresponding to conditions within both channels. Interrupt vector location programmable. Daisy-chained priority hardware interrupt circuitry.

SYSTEM INTERRUPT UNITS (SIU) = 1

SYSTEM CLOCK

	MIN.	MAX.
MDX-SIO-0	250kHz	2.5 MHz
MDX-SIO-4	250kHz	4.0 MHz

STD BUS INTERFACE

Inputs: One 74LS load max.
 Outputs: I_{OH} = -3mA min. at 2.4 Volts
 I_{OL} = 24mA min. at 0.5 Volts

OPERATING TEMPERATURE

0°C to 60°C

POWER SUPPLY REQUIREMENTS

+12 volts ± 5% at 72mA max.
 -12 volts ± 5% at 46mA max.
 +5 volts ± 5% at 650mA max.

CARD DIMENSIONS

4.5 in. (11.43cm) high by 6.50 in. (16.51 cm) long
 0.48 in. (1.22cm) maximum profile thickness
 0.062 in. (0.16cm) printed-circuit-board thickness

CONNECTORS

Function	Configuration	Mating Connector
STD-Z80 BUS	56-pin 0.125 in. centers	PRINTED CIRCUIT Viking 3VH28/ 1CE5 WIRE WRAP Viking 3VH28/ 1CND5 SOLDER LUG Viking 3VH28/ 1CN5
Serial I/O	26-pin 0.100 in. center	FLAT RIBBON Ansley 609- 2600M DISCRETE WIRES Winchester PGB26A (housing) Winchester 100-70020S (contacts)

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
MDX-SIO	Module less mating connectors with Operations Manual (2.5MHz version).	MK77651-0
MDX-SIO-4	Module with Operations Manual less mating connectors (4.0MHz version).	MK77651-4
	MDX-SIO Operations Manual Only	MK79608

MICRO SYSTEMS DATA BOOK

I	Table of Contents
II	General Information
III	STD-Z80 BUS
IV	MDX Series Data Processing
V	MD Series Input/Output
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VIII	MD Series Accessories
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MOSTEK®

MD SERIES MEMORY CARDS

MDX-DRAM

**MK77750-0, MK77754-0, MK77754-4,
MK77752-0, MK77752-4**

FEATURES

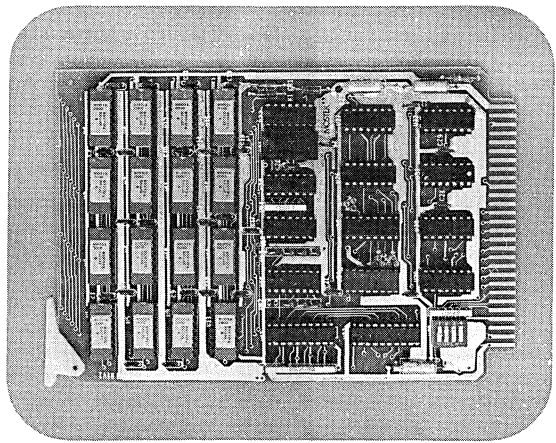
- STD-Z80 BUS compatible
- Three memory sizes:
 - 8K x 8 (MDX-DRAM8)
 - 16K x 8 (MDX-DRAM16)
 - 32K x 8 (MDX-DRAM32)
- Selectable addressing on 4K boundaries
- 4MHz version available (MDX-DRAM-4)

DESCRIPTION

The MDX-DRAM is designed to be a RAM memory expansion board for the Mostek MD Series™ of Z80-based microcomputers. It is available in three memory capacities: 8K bytes (MDX-DRAM8), 16K bytes (MDX-DRAM16), and 32K bytes (MDX-DRAM32). Additionally, the MDX-DRAM16 and the MDX-DRAM32 are available in a 4MHz version. Thus, the designer can choose from the various options to tailor his add-on dynamic RAM directly to his system requirements.

The MDX-DRAM8 is designed using Mostek's MK4108, 8,192-bit dynamic RAM. The MDX-DRAM16 and MDX-DRAM32 utilize high-performance MK4116, 16,384-bit dynamic RAMs which allow 4MHz versions of these boards to be offered. No wait-state insertion circuitry is required on

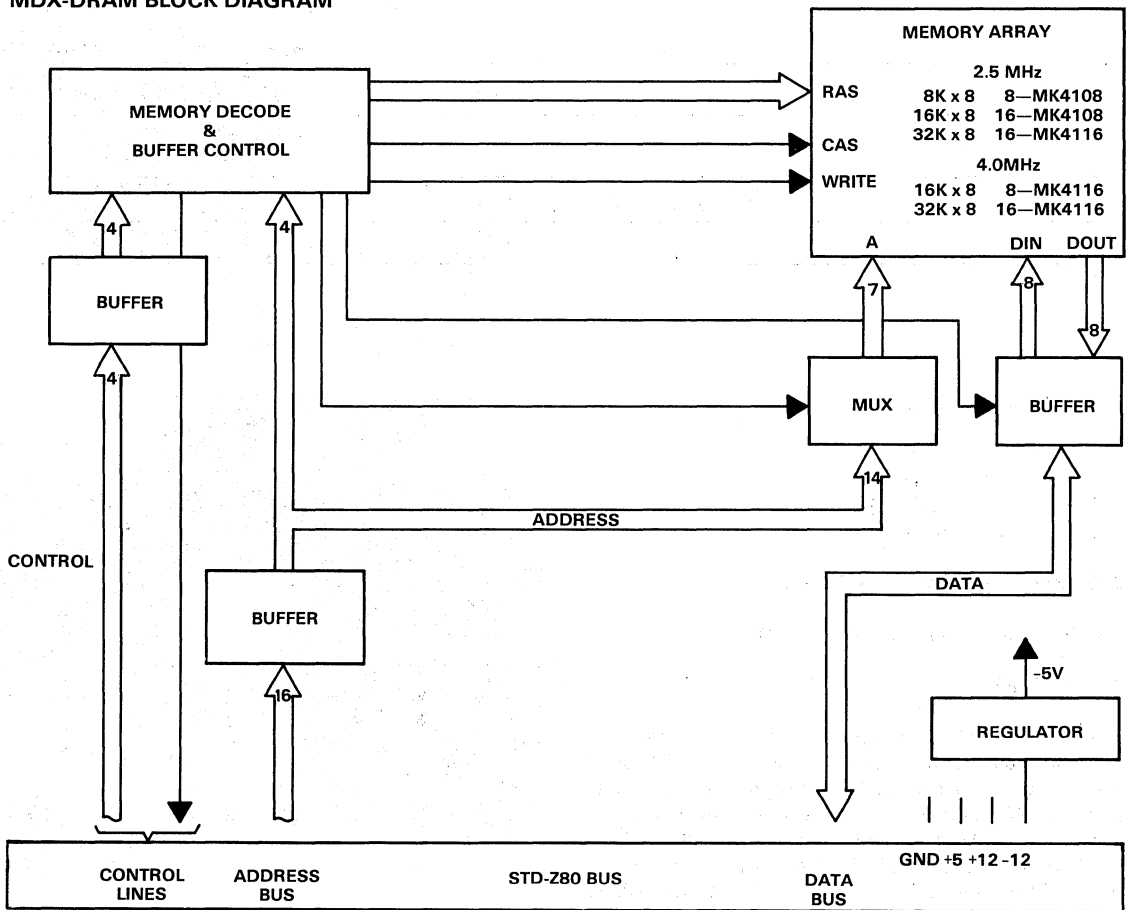
MDX-DRAM BOARD PHOTO



MD SERIES
MEMORY

any of the RAM cards. Memory refresh signals are provided on the Z80 based MDX-CPU boards. Address selection is provided on all MDX-DRAM cards for positioning the 8K, 16K, or 32K of memory to start on any 4K boundary.

MDX-DRAM BLOCK DIAGRAM



WORD SIZE

8 Bits

MEMORY SIZE

MDX-DRAM8 - 8,192 bytes
 MDX-DRAM16 - 16,384 bytes
 MDX-DRAM32 - 32,768 bytes

ADDRESS SELECTION

Selection of 8K, 16K, or 32K contiguous memory blocks to reside at any 4K boundary.

ACCESS TIMES

System Clock		Memory Access Times	Memory Cycle Times
MDX-DRAM	2.5MHz	350ns max.	465ns min.
MDX-DRAM-4	4.0MHz	200ns max.	325ns min.

SYSTEM INTERRUPT UNITS (SIU) = 0

SYSTEM CLOCK

	MIN	MAX
MDX-DRAM	1.25MHz	2.5MHz
MDX-DRAM-4	1.25MHz	4.0MHz

STD BUS INTERFACE

Inputs: One 74LS load max.
 Outputs: $I_{OH} = -3\text{mA}$ min. at 2.4 volts
 $I_{OL} = 24\text{mA}$ min. at 0.5 volts

OPERATING TEMPERATURE

0°C to 60°C

POWER SUPPLY REQUIREMENTS

+5V \pm 5% at 0.6A max.
 +12V \pm 5% at 0.25A max.
 -12V \pm 5% at 0.03A max.

CARD DIMENSIONS

4.5 in. (11.43 cm) high by 6.50 in. (16.51 cm) long
 0.48 in. (1.22 cm) maximum profile thickness
 0.062 in. (0.16 cm) printed-circuit-board thickness

CONNECTORS

Function	Configuration	Mating Connector
STD-Z80 BUS	56-pin 0.125 in centers	PRINTED CIRCUIT Viking 3VH28/ ICE5 WIRE WRAP Viking 3VH28/ 1CND5 SOLDER LUG Viking 3VH28/ 1CN5

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
MDX-DRAM8	Module with Operation Manual less mating connectors 8K Bytes (4108's) 2.5MHz	MK77750-0
MDX-DRAM16	16K Bytes (4116's) 2.5 MHz	MK77754-0
MDX-DRAM32	32K Bytes (4116's) 2.5MHz	MK77752-0
MDX-DRAM16-4	16K Bytes (4116's) 4.0MHz	MK77754-4
MDX-DRAM32-4	32K Bytes (4116's) 4.0MHz	MK77752-4
	MDX-DRAM Operations Manual Only	MK79624

MD SERIES
MEMORY

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MD SERIES MEMORY CARDS

MDX-EPROM

MK77758

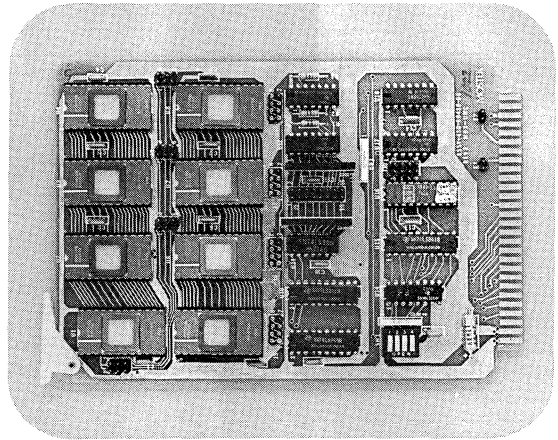
FEATURES

- STD and STD-Z80 BUS compatible
- Accepts the following industry standard EPROMS:
 - 2758 (1K x 8)
 - 2716 (2K x 8)
 - 2732 (4K x 8)
- Eight EPROM sockets for maximum storage of:
 - 8K x 8 using 2758's
 - 16K x 8 using 2716's
 - 32K x 8 using 2732's
- Wait-state generator for 4MHz operation
- Selectable addressing on 4K boundaries
- Operates at 2.5MHz or 4.0MHz system speed
- Single +5 Volt supply
- 8-2716 EPROM's supplied

DESCRIPTION

The MDX-EPROM is designed to be an EPROM memory expansion board for the Mostek MD Series™ of Z80-based microcomputers. The MDX-EPROM accepts the following EPROMs: 2758 (1K x 8), 2716 (2K x 8) and 2732 (4K x 8)

MDX-EPROM BOARD PHOTO

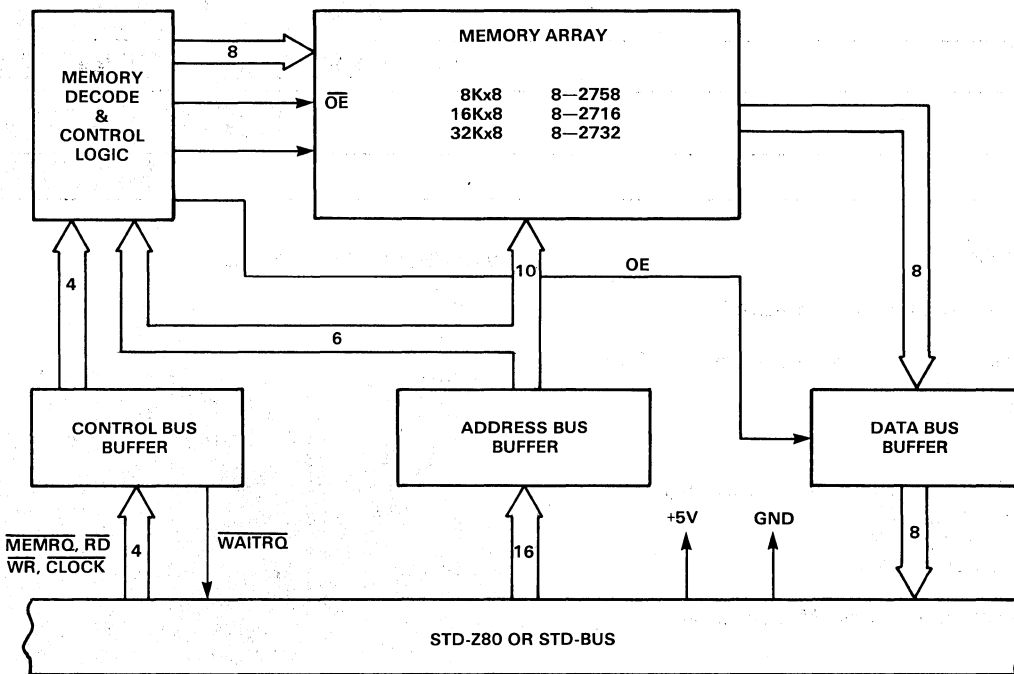


MD SERIES
MEMORY

which gives a maximum storage capacity of 8K, 16K, or 32K bytes respectively.

Starting address selection is provided for positioning the MDX-EPROM on any 4K boundary. A wait-state generator is also provided for optional 4MHz operation.

MDX-EPROM BLOCK DIAGRAM



WORD SIZE

8 Bits

MEMORY SIZE

8K x 8 using eight 2758's
 16K x 8 using eight 2716's*
 32K x 8 using eight 2732's

*Shipped configuration

ADDRESS SELECTION

4K boundaries

REQUIRED ACCESS TIME

Memory Time	Min Access Time	Cycle Time
2758, 2716, 2732	450ns*	450ns

*One wait state must be added for 4MHz operation.

SYSTEM INTERRUPT UNITS (SIU) = 0

STD BUS INTERFACE

Inputs: One 74LS load max.
 Outputs: $I_{OH} = -3mA$ min. at 2.4 Volts
 $I_{OL} = 24mA$ min. at 0.5 Volts

OPERATING TEMPERATURE

0°C to 60°C

POWER SUPPLY REQUIREMENTS+ 5 Volts \pm 5% at 0.45A*

*Does not include EPROMs. Add 100 mA for each EPROM.

CARD DIMENSIONS

4.5 in. (11.43 cm) high by 6.50 in. (16.51 cm) long

0.48 in. (1.22 cm) maximum profile thickness

0.062 in. (0.16 cm) printed-circuit-board thickness

CONNECTORS

Function	Configuration	Mating Connector
STD-Z80 BUS	56-Pin 0.125 in. centers	PRINTED CIRCUIT Viking 3VH28/ 1CE5 WIRE WRAP Viking 3VH28/ 1CND5 SOLDER LUG Viking 3VH28/ 1CN5

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
MDX-EPROM	Module with Operation Manual less mating connectors Includes eight 2716 EPROMs.	MK77758
	MDX-EPROM Operations Manual only	MK79671

MOSTEK®

MD SERIES MEMORY CARDS

MDX-EPROM/UART

MK77753-0, MK77753-4

FEATURES

- STD and STD-Z80 BUS compatible
- 10K x 8 EPROM/ROM (2716's not included)
- Selectable addressing on 2K boundaries
- Serial I/O channel:
 - RS - 232 and 20 mA interface
 - Reader-step control for Teletypes
 - Baud-rate generator (110-19200 Baud)
- 4MHz version available (MDX-EPROM/UART-4)
- Strap-selectable address

DESCRIPTION

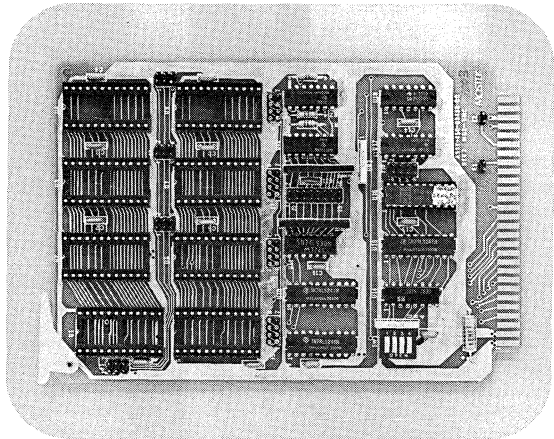
The MDX-EPROM/UART is one of Mostek's complete line of STD-Z80 BUS-compatible Z80 microcomputer modules.

Designed as a universal EPROM add-on module for the STD-Z80 BUS, the MDX-EPROM/UART provides the system designer with sockets to contain up to 10K x 8 of EPROM memory (5-2716's) as shown in the Block Diagram.

The EPROM memories can be positioned to start on any 2K boundary within a 16K block of memory via a strapping option provided on the MDX-EPROM/UART.

Included on-board the MDX-EPROM/UART is a fully buffered asynchronous I/O port with a Teletype reader-step control. The address of the serial port is strap-selectable to one of 64 locations via six jumpers. A full duplex UART is used to receive and transmit data at the serial port. Operation and UART options are under software control. Once the unit has been programmed, no further changes

MDX-EPROM/UART BOARD PHOTO



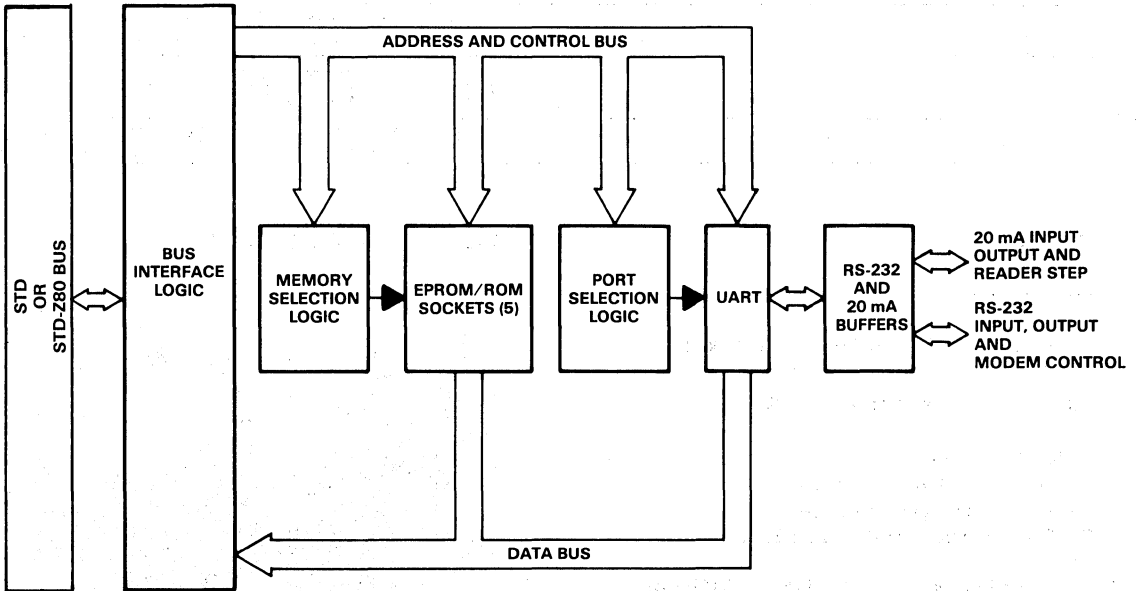
MD SERIES
MEMORY

are necessary unless there is a modification of the serial data format. Features of the UART include:

- Full-duplex operation
- Start-bit verification
- Data word size variable from 5 to 8 bits
- One or two stop-bit selection
- Odd, even, or no parity option
- One-word buffering on both transmit and receive

The MDX-EPROM/UART is also available in a 4MHz version. Circuitry is provided to force one wait-state each time on-board EPROMs or the UART are accessed.

MDX-EPROM/UART BLOCK DIAGRAM



WORD SIZE

8 Bits for PROM
5 to 8 Bits for Serial I/O

I/O TRANSFER RATE

110, 300, 600, 1200, 2400, 4800, 9600, 19200 Baud

MEMORY SIZE

10K bytes of 2716 memory
(2716's not included)

SERIAL COMMUNICATIONS INTERFACE

MEMORY ADDRESSING

ROM/EPROM
2K blocks jumper-selectable for any 2K boundary within a given 16K block of the Z80 memory map.

Signal	Buffered For 20mA Current Loop	RS-232
Transmitted data	Output	Output
Received data	Input	Input
Reader Step Relay (RSR)	Output (40mA)	
Data Terminal Ready (DTR)		Input
Request to Send (RTS)		Input
Carrier Detect (CDET)		Output
Clear to Send (CTS)		Output
Data Set Ready (DSR)		Output

MEMORY SPEED REQUIRED

Memory	Access Time	Cycle Time
2716*	450ns	450ns

* Single 5-Volt type required

SYSTEM INTERRUPT UNITS (SIU) = 0

I/O ADDRESSING

On-board Serial I/O Port
Control Port XXXXXX01
Data Port XXXXXX00
Modem and Reader Step Control XXXXXX10
XXXXXX represents six strap-selectable address bits

SYSTEM CLOCK

	MIN.	MAX.
MDX-EPROM/UART	250kHz	2.5 MHz
MDX-EPROM/UART-4	250kHz	4.0 MHz

STD BUS INTERFACE

Inputs: One 74LS Load max.
 Outputs: $I_{OH} = -3\text{mA min. at 2.4 Volts}$
 $I_{OL} = 24\text{mA min. at 0.5 Volts}$

OPERATING TEMPERATURE RANGE

0°C to +60°C

POWER SUPPLY REQUIREMENTS

+12 Volts $\pm 5\%$ at 50 mA max.
 -12 Volts $\pm 5\%$ at 35 mA max.
 + 5 Volts $\pm 5\%$ at 1.2 A max.

CARD DIMENSIONS

4.5 in. (11.43cm) high by 6.50 in. (16.51 cm) long
 0.48 in. (1.22cm) maximum profile thickness
 0.062 in. (0.16cm) printed-circuit-board thickness

CONNECTORS

Function	Configuration	Mating Connector
STD-Z80 BUS	56-pin 0.125 in. centers	PRINTED CIRCUIT Viking 3VH28/ 1CE5 WIRE WRAP Viking 3VH28/ 1CND5 SOLDER LUG Viking 3VH28/ 1CN5
Serial I/O	26-pin 0.100 in. grid	FLAT RIBBON Ansley 609 2600M DISCRETE WIRES Winchester PGB26A (housing) Winchester 100-70020S (contacts)

MD SERIES
MEMORY

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
MDX-EPROM/UART	Module with Operation Manual less EPROMs and mating connectors (2.5MHz version).	MK77753-0
MDX-EPROM/UART-4	Module with Operation Manual less EPROMs and mating connectors (4.0 MHz version).	MK77753-4
	MDX-EPROM/UART Operations Manual Only	MK79604

MOSTEK®

MD SERIES MEMORY CARDS

MDX-SRAM

MK77755, MK77756

FEATURES

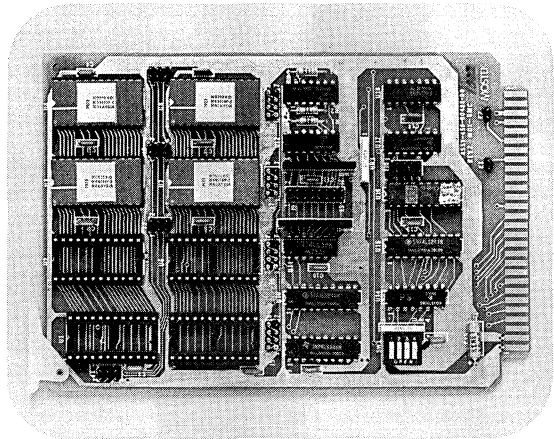
- STD and STD-Z80 BUS compatible
- Three memory sizes:
 - 4K x 8 (MDX-SRAM4)
 - 8K x 8 (MDX-SRAM8)
- Selectable starting address on 4K boundaries
- 2.5 MHz and 4.0 MHz compatible
- Single +5 Volt supply

DESCRIPTION

The MDX-SRAM is designed to be a static RAM Memory expansion board for the Mostek MD Series™ of Z80-based microcomputers. It is available in two memory capacities: 4K bytes (MDX-SRAM4) and 8K bytes (MDX-SRAM8). Additionally, all MDX-SRAM boards are 2.5MHz and 4.0MHz compatible. Thus, the designer can choose from two options available and tailor the add-on static RAM directly to the system requirements.

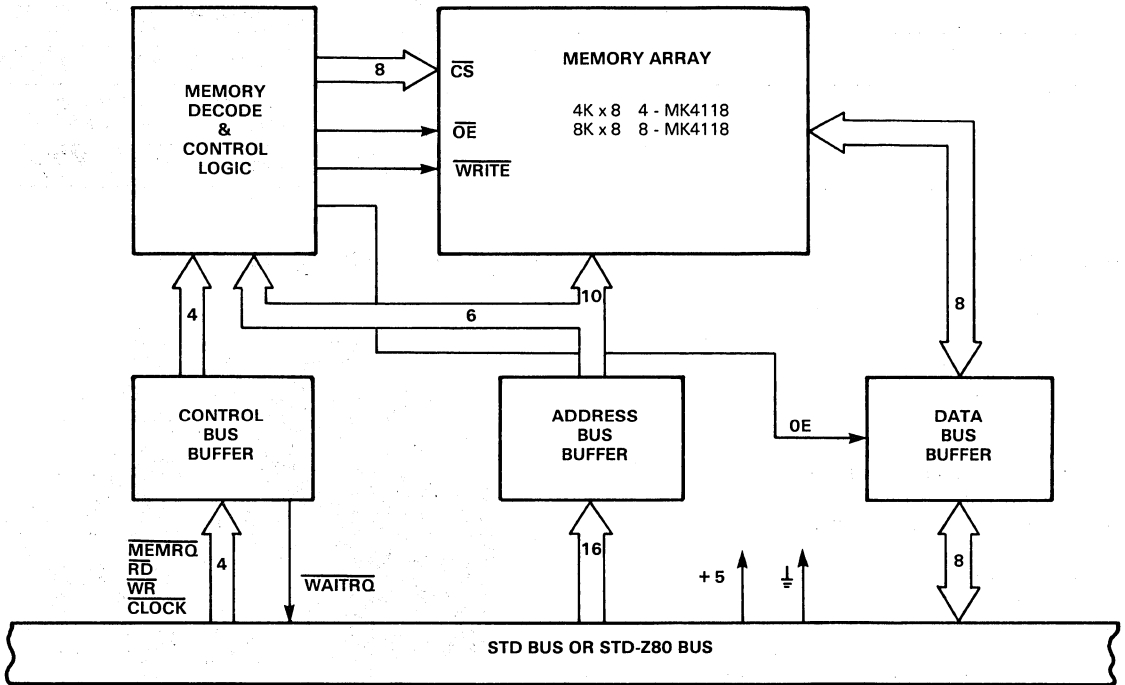
The MDX-SRAM is designed using the state-of-art MK4118 (1K x 8) static RAM memory devices. No wait

MDX-SRAM BOARD PHOTO



states are necessary for operating the MDX-SRAM at 2.5MHz or 4.0MHz. Address selection is provided on all MDX-SRAM cards for positioning the 4K or 8K of memory to start on any 4K boundary.

MDX-SRAM BLOCK DIAGRAM



WORD SIZE

8 Bits

MEMORY SIZE

MDX-SRAM4 - 4,096 Bytes
MDX-SRAM8 - 8,192 Bytes

ADDRESS SELECTION

Selection of 4K or 8K contiguous memory blocks to begin on any 4K boundary.

TIMING

	Memory Access	Memory Cycle
MDX-SRAM	250ns max.	250ns min.

SYSTEM INTERRUPT UNITS (SIU) = 0

STD BUS INTERFACE

Inputs: One 74LS load max.
Outputs: $I_{OH} = -3mA$ min. at 2.4 Volts
 $I_{OL} = 24mA$ min. at 0.5 Volts

OPERATING TEMPERATURE

0°C to 60°C

POWER SUPPLY REQUIREMENTS

Boards	Current at +5V ± 5%
MDX-SRAM4	0.8A max
MDX-SRAM8	1.2A max

CARD DIMENSIONS

4.5 in. (11.43 cm) high by 6.50 in. (16.51 cm) long
 0.48 in. (1.22 cm) maximum profile thickness
 0.062 in. (0.16 cm) printed-circuit-board thickness

CONNECTORS

Function	Configuration	Mating Connector
STD-Z80 BUS	56-pin	PRINTED CIRCUIT Viking 3VH28/ 1CE5
	0.125 in. centers	WIRE WRAP Viking 3VH28/ 1CND5 SOLDER LUG Viking 3VH28/ 1CN5

**ORDERING INFORMATION**

DESIGNATOR	DESCRIPTION	PART NO.
MDX-SRAM4	4K Bytes (4118's) module with operation manual less mating connectors	MK77755
MDX-SRAM8	8K Bytes (4118's) module with operation manual less mating connectors	MK77756
	MDX-SRAM Operations Manual Only	MK79673

MOSTEK®

MD SERIES MEMORY CARDS

MDX-UMC

MK77759

FEATURES

- STD and STD-Z80 BUS compatible
- Can be strapped to accept the following industry-standard memory devices:

EPROM	STATIC RAM	ROM
2758 (1K x 8)	MK4118 (1K x 8)	
2716 (2K x 8)	MK4802 (2K x 8)	MK34000 (2K x 8)
2732 (4K x 8)		

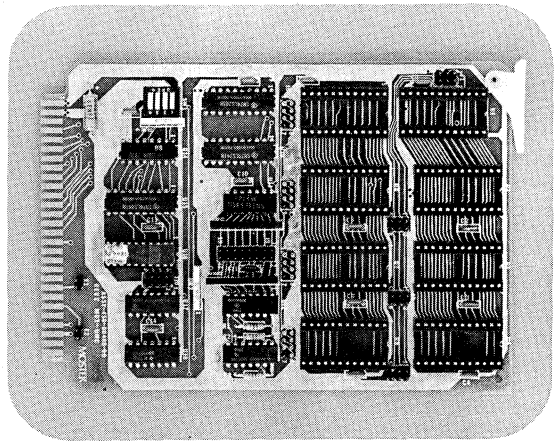
- Memories can be mixed to form a combination memory board
- Operates at 2.5MHz and 4.0MHz system clocks speeds
- Wait-state generator provided
- Single +5 Volt supply

DESCRIPTION

The MDX-UMC is one of Mostek's complete line of STD-Z80 BUS-compatible microcomputer modules.

Designed as a universal memory card for the STD-Z80 BUS, the MDX-UMC provides the user with the capability of configuring the board to meet the system requirement of ROM/EPROM and/or RAM. By the use of strapping options, the user is able to configure pairs of sockets for

MDX-UMC BOARD PHOTO

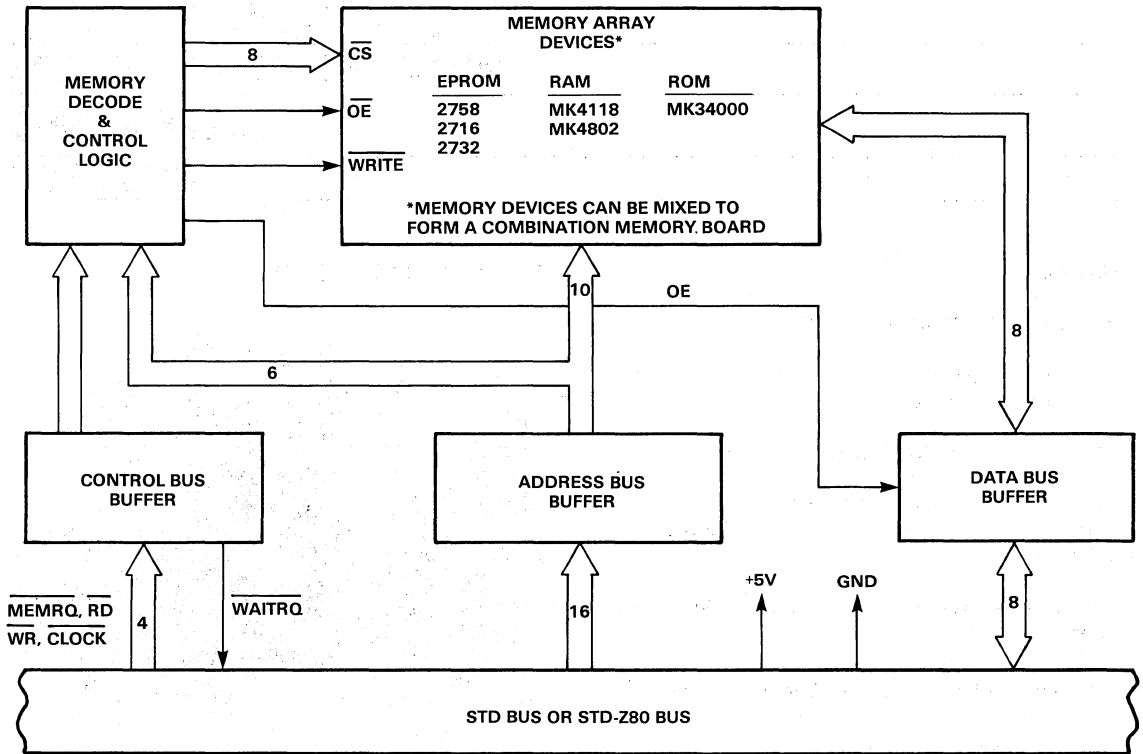


MD SERIES
MEMORY

ROM/EPROM/RAM to form a combination memory board.

Other MDX-UMC features include 4K boundary addressing and an optional wait-state generator to accommodate slower memories for 4MHz system clock operations.

MDX-UMC BLOCK DIAGRAM



WORD SIZE

8 Bits

MEMORY SIZE

8 sockets

Sockets are strapped in pairs to accommodate the following memories.

EPROM	STATIC RAM	ROM
2758	MK4118	
2716	MK4802	MK34000
2732		

MEMORY ADDRESSING

4K boundaries

SYSTEM INTERRUPT UNITS (SIU) = 0

STD-BUS INTERFACE

Inputs: One 74LS load max.
 Outputs: $I_{OH} = -3mA$ min. at 2.4 Volts
 $I_{OL} = 24mA$ min. at 0.5 Volts

OPERATING TEMPERATURES

0°C to 60°C

POWER REQUIREMENTS

+5V \pm 5% at 0.450 A max.
 Does not include power for memories

CARD DIMENSIONS

4.5 in. (11.43cm) high by 6.50 in. (16.51cm) long
 0.48 in. (1.22cm) maximum profile thickness
 0.062 in. (0.16cm) printed-circuit-board thickness

CONNECTORS

Function	Configuration	Mating Connector
STD-Z80 BUS	56-pin	PRINTED CIRCUIT Viking 3VH28/ 1CE5
	0.125 in. centers	WIRE WRAP Viking 3VH28/ 1CND5 SOLDER LUG Viking 3VH28/ 1CN5

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
MDX-UMC	Module with operation manual less mating connectors	MK77759
	MDX-UMC Operation Manual Only	MK79667

**MD SERIES
MEMORY**

MICRO SYSTEMS DATA BOOK

I	Table of Contents
II	General Information
III	STD-Z80 BUS
IV	MDX Series Data Processing
V	MD Series Input/Output
VI	MD Series Memory
VII	MD Series Special Functions
VIII	MD Series Accessories
IX	MD Series Data Processing
X	SDE Series Data Processing
XI	SDE Series Input/Output
XII	SDE Series Memory
XIII	SDE Series Accessories
XIV	Software Disk Based
XV	Development Systems
XVI	Systems Emulation Boards
XVII	Peripherals

MOSTEK®

MDX SERIES

System Interrupt Units

CARD	SIU's
MDX-CPU1	1
MDX-CPU2	1
MDX-DRAM8/16/32	0
MDX-EPROM/UART	0
MDX-DEBUG	0
MDX-PIO	2
MDX-SIO	1
MDX-SST	0
MDX-FLP	1
MDX-MATH	1
MDX-A/D8	1
MDX-AIO	0
MDX-A/D12	1
MDX-D/A8	0
MDX-D/A12	0
MDX-UMC	0
MDX-SRAM4/8/16	0
MDX-EPROM	0
MDX-INT	1
MDX-SC/D	1

MD SERIES
SPECIAL FUNCTIONS

MOSTEK®

MD SERIES SPECIAL FUNCTIONS

MDX-DEBUG

MK77950-0, MK77950-4

HARDWARE FEATURES

- STD-Z80 BUS compatible
- 4 MHz version available
- Serial I/O Channel
- 10K bytes of ROM contain the following firmware:
DDT-80, ASMB-80

DEBUGGER FEATURES

- Z80 Operating System with debug capability
- Channelized I/O for versatility
- I/O peripheral drivers supplied
- ROM-based

TEXT EDITOR FEATURES

- Input and modification of ASCII Text
- Line and character editing
- Alternate command buffers for pseudo-macro command capability
- ROM-based

ASSEMBLER FEATURES

- Assembles all Z80 mnemonics
- Object output in industry-standard hexadecimal format extended for Relocatable and Linkable Programs
- Over fifteen pseudo-ops
- Two-pass assembly
- ROM-based

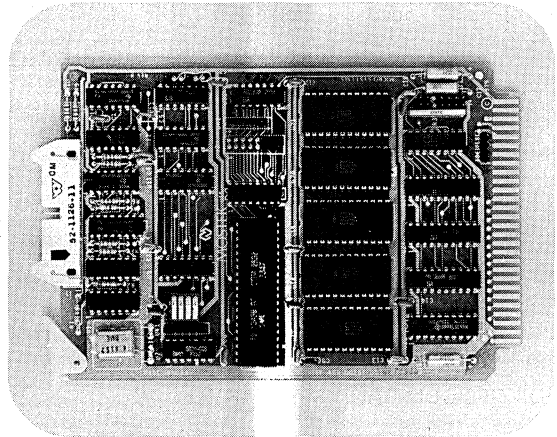
LINKING LOADER FEATURES

- Loads into memory both relocatable and non-relocatable object output of the assembler
- Loads Relocatable modules anywhere in memory
- Automatically provides linkage of global symbols between object modules as they are loaded
- Prints system load map
- ROM-based

HARDWARE DESCRIPTION

The MDX-DEBUG module has sockets for 10K bytes of masked ROM that are filled with a Z80 firmware package

MDX-DEBUG BOARD PHOTO



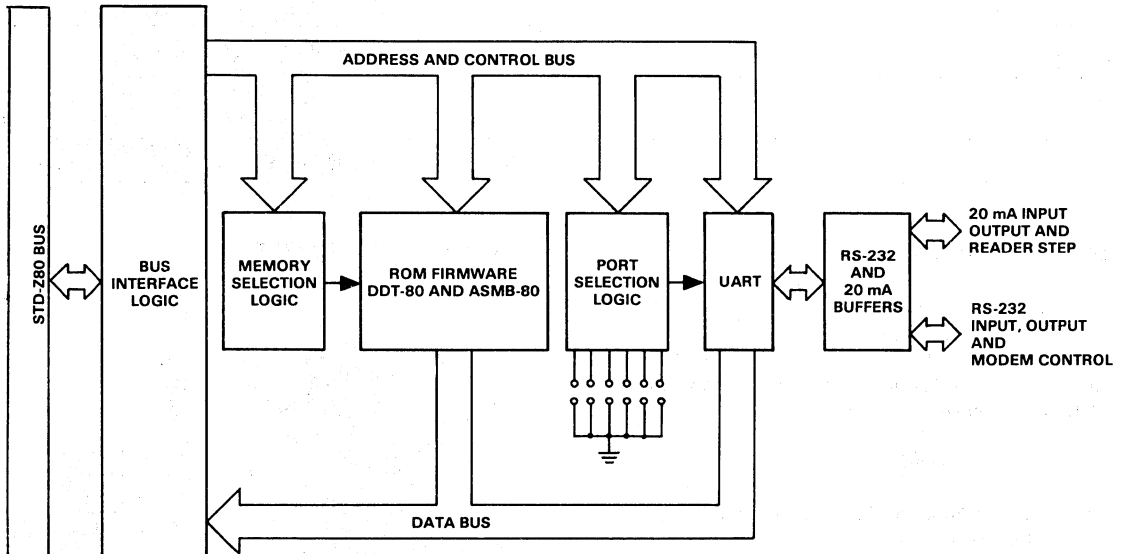
MD SERIES
SPECIAL FUNCTIONS

(DDT-80/ASMB-80). This module has a STD-Z80 BUS interface and is available in both 2.5 MHz and 4.0 MHz version. Included on-board is a fully buffered asynchronous I/O port capable of 110-19200 Baud rates. Serial data interfaces are available for 20 mA current loop (with reader-step control) and RS-232. The on-board Baud Rate Generator is selectable to all common Baud rates from 110 to 19,200 Baud. The address of the serial port is selectable via 6 on-board jumpers.

DEBUGGER DESCRIPTION

DDT-80 is the Operating System for the MDX-DEBUG Module, residing in a 2K ROM (MK34000 Series) on the module itself. It provides the necessary tools and techniques to operate the system, i.e., to efficiently and conveniently perform the tasks necessary to develop microcomputer software. DDT-80 is designed to support the user from initial design through production testing. It allows the user to display and update memory, registers, and ports, load and dump object files, set breakpoints, copy blocks of memory, and execute programs.

MDX-DEBUG BLOCK DIAGRAM



DDT-80 COMMAND SUMMARY

- | | |
|-----------|---|
| M s | - Display and/or update the contents of memory location s. |
| M s, f | - Tabulate the contents to memory locations s through f. |
| P s | - Display and/or update the content of I/O ports. |
| D s, f | - Dump the contents of memory locations s through f in a format suitable to be read by the L command. |
| L | - Load, into memory, data which is in the appropriate format. |
| E s | - Transfer control from DDT-80 to a user's program starting at location s. |
| H | - Perform 16-bit hexadecimal addition and/or subtraction. |
| C s, f, d | - Copy the contents of memory locations s through f to another location in memory starting at location d. |
| B s | - Insert a breakpoint in a user's program (must be in RAM) at location s which transfers control back to DDT-80. This allows the user to intercept his program at a specific point (location s) and examine memory and CPU registers to determine if this program is working correctly. |
| Rx | - Display the contents of the user registers. |

The s, f, and d represent start, finish, and destination operands required for each command.

MEMORY, PORT AND REGISTER COMMANDS (M, P, R)

The M, P, and R commands provide the means for displaying the contents of specified memory locations, port addresses, or CPU registers. The M and P commands sequentially access memory locations or ports and display their contents. The user has the option of updating the content of the memory location or port. (Note some ports are output only and their contents cannot be displayed). The M command also gives the user access to the CPU registers through an area in RAM called the Register Map (discussed in the Execute and Breakpoint section below).

The M and R commands are used to tabulate blocks of memory locations (M) or the CPU registers (R). The M command will accept two operands, the starting and ending address of the block to be tabulated. The R command will accept either no operand or one. If no operand is specified, the CPU registers will be displayed without a heading. If an operand is specified, then a heading which labels the registers' contents will be displayed as well.

EXECUTE AND BREAKPOINT (E, B)

The E command is used to execute all programs, including aids such as the Assembler. The B command is used to set a breakpoint to exit from a program at some predetermined location for debugging purposes. At the instant of a breakpoint exit, the contents of all CPU registers are saved in a designated area of RAM called the Register Map. In the

Register Map, the register contents may be examined or mapped using the M command and a predefined mnemonic (or absolute address) of the storage location for that register (example :PC, :A, ..., :SP). The Register Map is also used to initialize the CPU registers whenever execution is initiated or resumed. Thus the E and B commands can be used together to initialize, execute, and examine the results of individual program segments.

The B command gives the user the option of having all CPU registers displayed when the breakpoint is encountered. This is done by entering a second operand to the B command. Otherwise, DDT-80 defaults to displaying the PC and AF registers. When all CPU registers are displayed, the format is the same as for the R command previously discussed.

LOAD, DUMP, AND COPY (L, D, C)

The L and D commands load and dump object files through the object I/O channel in standard Hex format. Checksums are used for error detection, and the addresses of questionable blocks are typed automatically while loading.

The C command will copy the contents of the memory block specified to another block of memory. There are no restrictions on the direction of the copy or on whether the blocks overlap.

HEXADEXIMAL ARITHMETIC (H)

The H command is a dummy command used to allow hexadecimal addition and subtraction for expression evaluation without performing any other operation.

DDT-80 I/O CAPABILITIES

DDT-80 specifies I/O channels, designated 'Console', 'Object', and 'Source', to which any suitable devices may be assigned. The Channel Assignment Table is located in RAM where it may be examined or modified using the M command. The table addresses correspond to the I/O channels and the table contents correspond to the addresses of the peripheral driver routines. A channel which has a device assignment may have that device assignment changed using the M command. This is accomplished by merely modifying the table contents of that channel's table address to correspond to the new peripheral driver routine. A set of peripheral driver routines is supplied and listed below. This scheme also allows the user to write a driver routine for his own peripheral, load it into memory, and easily configure that peripheral into the system.

DDT-80 I/O PERIPHERAL DRIVERS

1. A serial input driver (usually a keyboard).
2. A serial output driver (usually a CRT or teletype typehead).

3. A serial input driver which sends out a reader-step signal (usually a teletype reader).
4. A serial output driver which forces a delay after a carriage return (usually a Silent 700 typehead).
5. A parallel input driver (usually for high-speed paper tape input).
6. A parallel output driver (usually for high-speed paper tape output).
7. A parallel output driver (usually for a line printer).

TEXT EDITOR DESCRIPTION

The Text Editor permits random-access editing of ASCII character strings. It can be used as a line or character-oriented editor. Individual characters may be located by position or context. The Editor works on blocks of characters which are typically read into memory from magnetic tape or paper tape. Each edited block can be output to magnetic tape or paper tape after editing is completed. While the primary application for the Text Editor is in editing assembly language source statements, it may be applied to any ASCII text delimited by "carriage returns".

The Editor has a macro command processing option. Up to two sets of commands may be stored and processed at any time during the editing process.

All I/O is done via the DDT-80 channels. The Editor can be used with the ASMB-80 Assembler and Loader to edit, assemble, and load programs in memory without the need for external media for intermediate storage.

The following commands are recognized by the Text Editor:

- | | |
|--------------|---|
| An - | Advance record pointer n records |
| Bn - | Backup record pointer n records |
| Cn dS1dS2d - | Change string S1 to string S2 for n occurrences |
| Dn - | Delete next n records |
| E - | Exchange current record with records to be inserted |
| I - | Insert records |
| Ln - | Go to line number n |
| Mn - | Enter command buffers (pseudo-macro) |
| N - | Print top, bottom, and current line number |
| Pn - | Punch n records from buffer |
| R - | Read source records into buffer |
| Sn dS1d - | Search for nth occurrence of string S1 |

ASSEMBLER DESCRIPTION

The Assembler reads Z80 source mnemonics and pseudo-ops and outputs an assembly listing and object code. The assembly listing shows address, machine code, statement number, and source statement. The object code is in industry-standard hexadecimal format modified for relocatable, linkable assemblies.

The Assembler supports conditional assemblies, global symbols, relocatable programs, and a printed symbol table. It can assemble any length program limited only by a symbol table size which is user-selectable. Expressions involving addition and subtraction are allowed. A global symbol is categorized as "internal" if it appears as a label in the program; otherwise it is an "external" symbol. The printed symbol table shows which symbols are internal and which are external. The Assembler allows the user to select relocatable or non-relocatable assembly via the "PSECT" pseudo-op. Relocation records are placed in the object output for relocatable assemblies (the Mostek object format is defined below). The Assembler can be run as a single-pass assembler or as a learning tool. (In this mode, global symbols and forward references are not allowed.)

The following pseudo-ops are recognized by the Assembler:

ORG -	program origin
EQU -	equate label
DEFL -	define label
DEFM -	define message
DEFB -	define byte
DEFW -	define word
DEFS -	define storage
END -	end statement
NAME -	program name definition
PSECT -	program section definition
GLOBAL -	global symbol definition

Supports the following assembler pseudo-ops

EJECT -	eject a page of listing
TITLE -	place heading at top of each page
LIST -	turn listing on
NLIST -	turn listing off

RELOCATING LINKING LOADER DESCRIPTION

The Relocating Linking Loader provides state-of-the-art capability for loading programs into memory by allowing loading and linking of any number of relocatable and non-relocatable object modules. Non-relocatable modules are always loaded at their starting address as defined by the ORG pseudo-op during assembly. Relocatable object modules can be positioned anywhere in memory at an offset address.

The loader automatically links any relocator global symbols which are used to provide communication or linkage between program modules. As object programs are loaded,

a table containing global symbol references and definitions is built up. At the end of each module, the loader resolves all references to global symbols which are defined by either the current or a previously loaded module. It also prints on the console device the number of defined global symbols that have been referenced. The symbol table can be printed to list all global symbols and their load addresses. The number of object modules which can be loaded by the Loader is limited only by the amount of RAM available for the modules and the symbol table. Space for the symbol table is allocated dynamically downward in memory from either the top of memory or from a specified address entered as an operand of the load command.

All I/O is done via the DDT-80 channels. Assemblies can be done from source statements stored in memory (by the Editor). The object output can be directed to a memory buffer rather than to an external device. Thus, assembly and loading can be done without external storage media.

The Loader prints the beginning and ending address of each module as it is loaded. The transfer address as defined by the END pseudo-ops is printed for the first module loaded. The Loader execute command (E) can be used to automatically start execution at the transfer address.

The Loader Commands are the following:

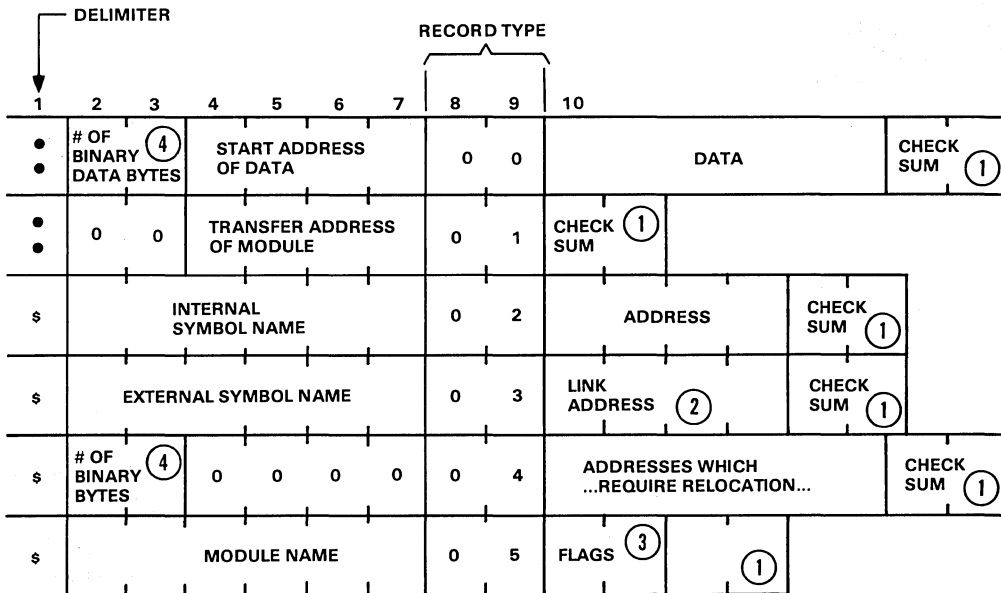
L offset -	load object module at address "off-set" plus program origin address
E -	execute loaded program at transfer address of first module
T -	print global symbol table

MOSTEK OBJECT OUTPUT DEFINITION

Each record of an object module begins with a delimiter (colon or dollar sign) and ends with carriage return and line feed. A colon (:) is used for data records and the end-of-file record. A dollar sign (\$) is used for records containing relocation information and linking information. All information is in ASCII. Each record is identified by "type". The type is determined by the 8th and 9th bytes of the record which can take the following values:

00 -	data
01 -	end-of-file
02 -	internal symbol
03 -	external symbol
04 -	relocation information
05 -	module definition

OBJECT MODULE TYPES



NOTES:

1. Check Sum is negative of the binary sum of all bytes except delimiter and carriage return/line feed.
2. Link Address points to last address in the data which uses the external symbol. This starts a backward link list through the data records for that external symbol. The list terminates at OFFFH.
3. The flags are one binary byte. Bit 0 is defined as:
0 - absolute module
1 - relocatable module
4. Maximum of 64 ASCII bytes.

MD SERIES
SPECIAL FUNCTIONS

WORD SIZE

8 bits for PROM
5 to 8 bits for serial I/O

MEMORY SIZE

10K bytes of firmware

MEMORY ADDRESSING

2K blocks jumper-selectable for any 2K boundary within a given 16K block of the Z80 memory map. MDX-DEBUG has ROMS strapped every 2K beginning at C0000H.

I/O ADDRESSING

On board Serial I/O Port
Control Port: XXXXXX01
Data Port: XXXXXX00
Module and Reader Step Control Port: XXXXXX10
XXXXXX represents 6 strap-selectable address bits.

I/O TRANSFER RATE

110, 300, 600, 1200, 2400, 4800, 9600, 19200 BAUD

SERIAL COMMUNICATIONS INTERFACE

SIGNAL

BUFFERED FOR

20 mA
Current
Loop

RS-232

Transmitted data
Received data
Data Terminal Ready (DTR)
Request to Send (RTS)
Carrier Detect (CDET)
Clear to Send (CTS)
Data Set Ready (DSR)
Reader Step relay (RS)

Output	Output
Input	Input
	Input
	Input
	Output
	Output
Output (40 mA)	Output

SYSTEM CLOCK

	MIN	MAX
MDX-DEBUG	1.25 MHz	2.5 MHz
MDX-DEBUG-4	1.25 MHz	4.0 MHz

SYSTEM INTERRUPT UNITS (SIU) = 0

STD BUS INTERFACE

Inputs: One 74LS load max.
Outputs: $I_{OH} = -3$ mA min. at 2.4 Volts
 $I_{OL} = 24$ mA min. at 0.5 Volts

OPERATING TEMPERATURE

0°C to +60°C

POWER SUPPLY REQUIREMENT

+12 Volts \pm 5% at 50 mA max.
-12 Volts \pm 5% at 35 mA max.
+5 Volts \pm 5% at 1.2 A max.

CARD DIMENSIONS

4.5 in. (11.43 cm) high by 6.50 in. (16.51 cm) long
0.48 in. (1.22 cm) maximum profile thickness
0.062 in. (0.16 cm) printed-circuit-board thickness

CONNECTORS

Function	Configuration	Mating Connector
STD-Z80 BUS	56-pin 0.125 in. centers	PRINTED CIRCUIT Viking 3VH28/ 1CE5 WIRE WRAP Viking 3VH28/ 1CND5 SOLDER LUG Viking 3VH28/ 1CN5
Serial I/O	26-pin 0.1 in. grid	FLAT RIBBON Ansley 609-2600M DISCRETE WIRES Winchester PGB26A (housing) Winchester 100-70020S (contacts)

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
MDX-DEBUG	Module with 10K bytes of firmware and Operations Manual. No mating connectors. 2.5 MHz version.	MK77950-0
MDX-DEBUG-4	Module with 10K bytes of firmware and Operations Manual. No mating connectors. 4.0 MHz version	MK77950-4
	MDX-DEBUG Operations Manual only.	MK79611
	Program Source Listing of 10K byte firmware package (DDT/ASMB-80) including comments and flow charts. (Available free with purchase of either MDX-DEBUG Module.)	MK78536 and MK78534

* The DDT-80 and ASMB-80 listings are available directly from Mostek by filling out a copy of the Software Licensing Agreement and returning it with the appropriate payment of Customer Purchase Order to:

Mostek Corporation
Microcomputer Systems Div.
1215 West Crosby Road
Carrollton, Texas 75006

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Order Number	Description	Price*

Ship To: _____ Bill To: _____

Method of Shipment: _____ Customer P.O. Number _____

Agreed To:

PURCHASER	MOSTEK CORPORATION
By: _____	By: _____
Title: _____	Title: _____
Date: _____	Date: _____

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**MD SERIES
SPECIAL FUNCTIONS**

MOSTEK®

MD SERIES SPECIAL FUNCTIONS

MDX-INT

MK77967

FEATURES

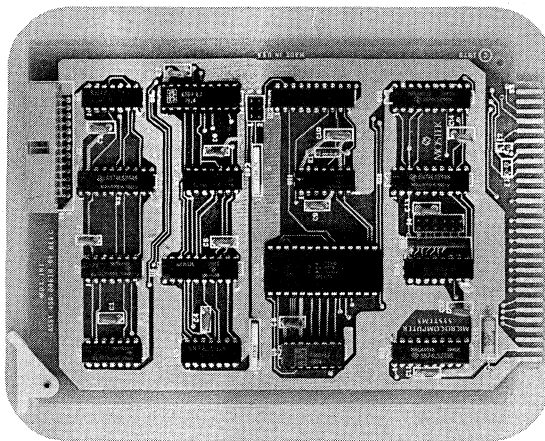
- STD-Z80 BUS compatible
- User-programmable CTC provides:
 - Four external vectored interrupts or
 - Four cascadable counter/timer channels or
 - any combination of the above
- Z80 Daisy Chain Interrupt Expansion
 - Allows up to 40 interrupt devices
 - User selectable expansion of System Interrupt Units (SIU)
 - Required for systems over five SIU's
- Nonmaskable Interrupt Input
- All input/output signals buffered
- 4MHz compatible (14, 24, 34, SIU)
- +5 Volt operation only

DESCRIPTION

The Interrupt-Timer Expansion Module, MDX-INT, is designed to be a versatile multimode unit. It provides external interrupt expansion of up to four lines, a non-maskable interrupt input, up to four cascadable timer channels, and internal interrupt expansion capability of up to 40 System Interrupt Units. All interrupts are Z80 compatible with full Mode 2 interrupt capability.

The MDX-INT permits up to four external interrupt inputs. This is possible by programming the MK3882 Counter Timer to function as an interrupt controller. When programming the CTC, the selected input channel is programmed to be in the counter mode with count set to one. The active edge as well as the interrupt vector locations are also specified by the user's program. When an active input occurs, a Mode 2 interrupt is generated by the CTC and the MDX-CPU can vector directly to a service routine. After the interrupt, the CTC down counter is automatically reloaded with a count of one and the CTC begins looking for

MDX-INT BOARD PHOTO



MD SERIES
SPECIAL FUNCTIONS

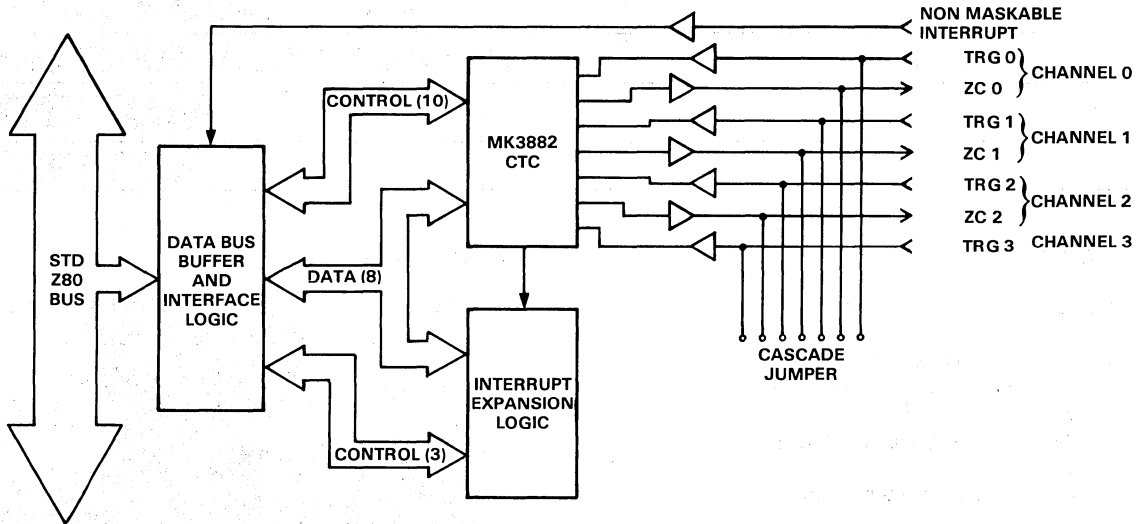
another active edge. Therefore, once initialized, a channel will automatically provide external interrupt capability.

Up to four channels can be used to provide external interrupts. Input is provided through the TRG0 to TRG3 lines for channels zero thru three. When multiple channels are used, priorities are resolved within the CTC if more than one interrupt request is made simultaneously. Each channel has a unique vector address and each channel can be independently "masked" by disabling that channel's local interrupt.

The nonmaskable interrupt is also provided as an input through this board. This line is tested by the MDX-CPU at the end of each instruction. It has priority over the normal interrupt and cannot be disabled under software control. Its usual function is to provide response to signals requiring immediate response, such as an impending power failure.

Each of the four CTC channels has an 8-bit Prescaler and 8-bit Down Counter that allows the circuit to be used as a counter or a timer as well as an interrupt generator. In the counter mode, a Zero Count output is provided that allows cascading of successive counters. In the counter mode,

MDX-INT BLOCK DIAGRAM



external inputs can be counted automatically by the CTC and interrupt the processor after a predefined number of counts. In the timer mode, the CTC can generate timing intervals that are integer multiples of the system clock period. The Zero Count output can generate a uniform pulse train of the precise period. Therefore, precise time measurements can be made that are a function of a crystal clock's accuracy and stability.

The MDX-INT also provides internal interrupt expansion through a concept of System Interrupt Units (SIU). The interrupt system of STD-Z80 compatible CPU's will allow up to five System Interrupt Units without need of expansion. The MDX-INT has circuitry to allow expansion of board with up to 40 SIU's. It must be the last card (the lowest priority) in the interrupt daisy chain. An SIU is defined as an interval of time equivalent to the worst-case propagation delay of the the priority daisy chain through an MD board. A board with one interrupting peripheral component, such as an MDX-SIO, has one SIU. A board with two interrupting peripheral components, such as an MDX-PIO, has two SIU's. A board with no interrupt capability has zero SIU's.

The SIU expansion circuitry on the MDX-INT card monitors the data bus and PCI lines. Wait states are added during the RETI opcode to allow the PCI and PCO lines to stabilize. The Wait state generator on the MDX-INT is enabled when an interrupt is pending or under service and will insert a predetermined number wait states for 15, 25, or 40 SIU's. The number of SIU's that the system can handle is hardware-selectable on-board.

SYSTEM CLOCK

	MIN.	MAX.
MDX-INT	250 kHz	4.0 MHz

STD BUS INTERFACE

Inputs: One 74LS Load max.
 Outputs: $I_{OH} = -3mA$ min. at 2.4 Volts
 $I_{OL} = 24mA$ min. at 0.5 Volts

SYSTEM INTERRUPT UNITS (SIU) = 1

POWER SUPPLY REQUIREMENTS

+5 Volts $\pm 5\%$ at 1.2 A Max.

WORD SIZE

Data: 8 Bits I/O
 Address: 8 Bits using 4 Ports with 6-Bits Jumper Option

OPERATING TEMPERATURE RANGE

0°C to 60°C

INTERRUPTS

External Interrupts are handled to provide prioritized, maskable, Mode 2 interrupts compatible with the STD-Z80 Bus requirements. The external interrupts are edge-triggered with the active edge software-programmable.

Up to four external interrupt inputs can be handled. These are prioritized with channel 0 being highest priority.

The nonmaskable interrupt is provided as an input. It has priority over any maskable interrupt and forces the MDX-CPU to a restart location of 066H.

TIMER

Up to four counter/timer channels are available. The outputs can be cascaded for long word counts. Zero Count/Timeout outputs are provided on three channels.

CARD DIMENSIONS

4.5 in. (114.3 mm) wide by 6.5 in. (165.1 mm) long
 0.48 in. (12.2 mm) maximum profile thickness
 0.062 in. (01.6 mm) printed-circuit-board thickness

CONNECTORS

Function	Configuration	Mating Connectors
STD-Z80 BUS	56-pin 0.125 in. centers	PRINTED CIRCUIT Viking 3VH28/1CE5 WIRE-WRAP Viking 3VH28/1CND5 SOLDER LUG Viking 3VH28/1CN5
CTC I/O	26-pin 0.100 in. centers	FLAT RIBBON Ansley 609-2600M DISCRETE WIRES Winchester PGB26A (housing) Winchester 100-70020S (contacts)

MD SERIES
SPECIAL FUNCTIONS

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
MDX-INT	2.5 MHz or 4.0 MHz board with Operations Manual less Mating Connector	MK77967
	MDX-INT Operations Manual only	MK79780

MOSTEK®

MD SERIES SPECIAL FUNCTIONS

MDX-SC/D

MK77963-0, MK77963-4

FEATURES

- STD-Z80 BUS compatible
- Provides an operator interface; switches and lamps
- 10K x 8 EPROM (2716's not included)
- Dual-purpose card, memory and/or diagnostic interface
- Interrupt-driven programmability
- Strap-selectable address
- 4 MHz Option
- Fully-buffered for MD Series expandability
- Diagnostic software package

DESCRIPTION

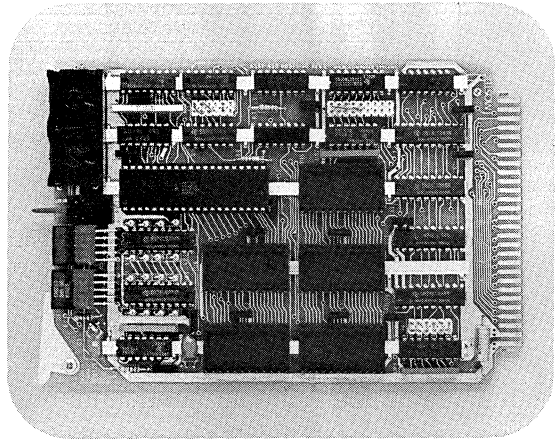
Designed as a system controller/diagnostics board, the MDX-SC/D provides the system designer with a tool to verify that various other MD Series modules are operational. The board is equipped with sockets to contain up to 10K x 8 of EPROM memory (5-2716's) as shown in the Block Diagram. The EPROM's can contain the diagnostic programs necessary for testing the modules or can contain user application programs.

The EPROM memories can be positioned to start on any 2K boundary within a 16K block of memory via a strapping option provided on the board.

For the 4MHZ version, circuitry is provided to force one wait state each time on-board EPROM's are accessed.

A three-position switch is provided at the top of the board.

MDX-SC/D BOARD PHOTO

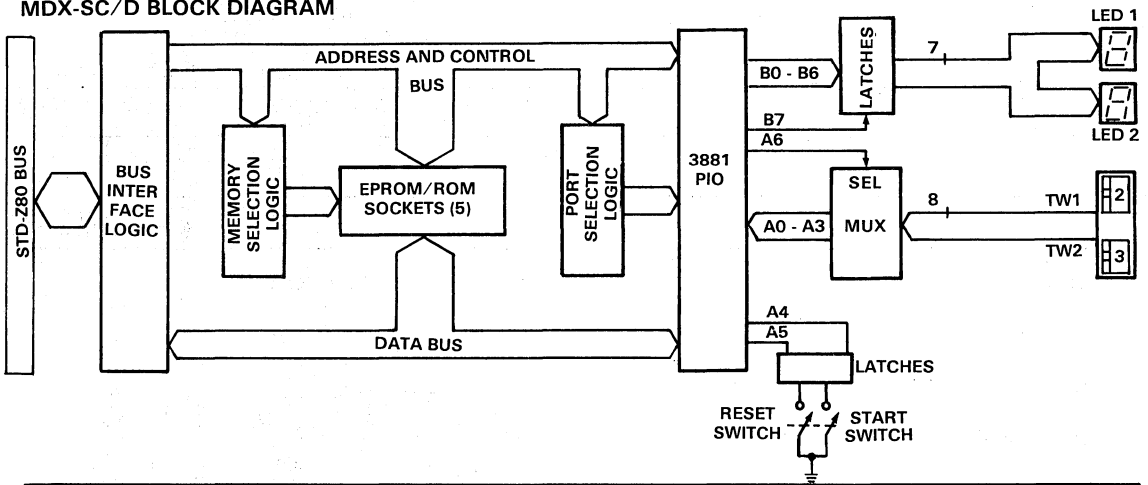


MD SERIES
SPECIAL FUNCTIONS

The switch is springloaded to the OFF position. The RESET position initializes the hardware and software diagnostics elements. The START position begins the diagnostic test which had been preset by the thumbwheel switches, also on the top of the board. At the conclusion of the test, the results are displayed by the LED Readouts. Data transfers from the switches to the bus and from the bus to the readouts are accomplished by the MK3881 PIO.

The PIO also permits total interrupt control so that full usage of the CPU interrupt capabilities can be utilized during data transfers. The PIO provides vectored interrupts and maintains the daisy-chain, priority interrupt logic compatible with the STD-Z80 BUS.

MDX-SC/D BLOCK DIAGRAM



The address decoding, interface and bus management for the board are performed by the address decode and data bus circuit. The PIO ports have two addresses each; these are summarized below.

	PORT A	PORT B
DATA	XXXX X000	XXXX X010
CONTROL	XXXX X001	XXXX X011

The XX symbols stand for the upper five bits of the I/O channel address. These bits are jumper-selectable on the board in order to provide address-selectable, fully decoded ports.

MEDEX-80

MEDEX-80 is a diagnostic software package designed to operate with the MDX-SC/D card's thumbwheels, switch and display. The package consists of a control monitor, MDX-SC/D card interface handler, and numerous diagnostic tests. The package can operate as a stand-alone program or can be integrated with a user program. MEDEX-80 is designed to allow user-developed diagnostics to be adapted as extensions to the package.

WORD SIZE

8 bits

MEMORY SIZE

10K bytes of 2716 memory (2716's not included)

MEMORY ADDRESSING

EPROM - 2K blocks jumper-selectable for any 2K boundary within a given 16K boundary of Z80 memory map.

MEMORY SPEED REQUIRED

Memory	Access Time	Cycle Time
* 2716	450 ns	450 ns

* Single 5-Volt type required

INPUT/OUTPUT

Controlled by spring-loaded RESET/START switch with center off.

Test selected by two thumbwheel switches.

Test results indicated by two 7-segment LEDs.

INTERRUPTS

Vectored interrupts generated. Interrupt vector programmable upon initialization. Daisy-chained interrupt priority. Selected bit channels can be masked out under program control.

SYSTEM INTERRUPT UNITS (SIU) = 1

SYSTEM CLOCK

	MIN.	MAX.
MDX-SC/D	250 kHz	2.5 MHz
MDX-SC/D-4	250 kHz	4.0 MHz

STD BUS INTERFACE

Inputs: One 74LS Load max.

Outputs: I_{OH} = -3mA min. at 2.4 Volts

I_{OL} = 24mA min. at 0.5 Volts

OPERATING TEMPERATURE RANGE

0°C to 60°C

POWER SUPPLY REQUIREMENTS

+5 Volts \pm 5% at 1.2 A max.

CARD DIMENSIONS

4.5 in. (11.43cm) high by 6.50 in. (16.51cm) long

0.48 in. (1.22cm) maximum profile thickness

0.062 in. (0.16cm) printed-circuit-board thickness

CONNECTORS

Function	Configuration	Mating Connector
STD-Z80 BUS	56-pin 0.125 in. centers	PRINTED CIRCUIT Viking 3VH28/1CE5 WIRE WRAP Viking 3VH28/1CND5 SOLDER LUG Viking 3VH28/1CN5

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
MDX-SC/D	Module with Operation Manual, 2.5 MHZ version	MK77963-0
MDX-SC/D-4	Module with Operation Manual, 4.0 MHZ version	MK77963-4
	MDX-SC/D Operation Manual Only	MK79678
MEDEX-80	Diagnostic software for various MDX Series cards, distributed on diskette in Z80 Assembly source form	MK77968

MD SERIES
SPECIAL FUNCTIONS

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MD SERIES SPECIAL FUNCTIONS

MDX-SST MK77958

FEATURES

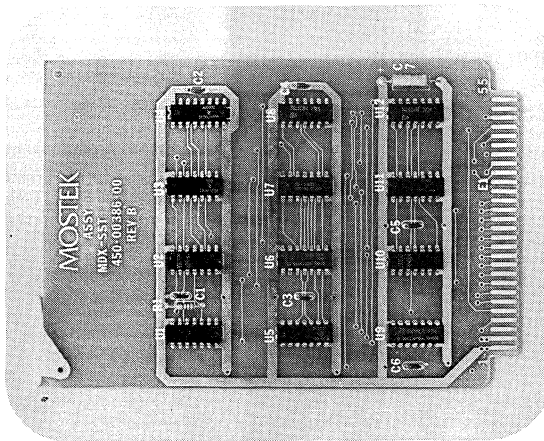
- STD-Z80 BUS compatible
- Hardware single-step capability
- Compatible with DDT-80 Operating System
- +5 Volt only
- Both 2.5MHz and 4.0MHz

DESCRIPTION

The Mostek MDX-SST was designed to enhance the hardware and software debug capability for MD Series systems. The use of the MDX-SST with the MDX-CPU1, MDX-CPU2 and MDX-DEBUG boards allows the user to single-step instructions through RAM and/or EPROM/ROM with the capability of displaying all of the CPU registers on each instruction execution.

The MDX-SST board is implemented using the CPU's nonmaskable interrupt and is controlled by firmware from the keyboard. When the command to single step an instruction is given, the sequence of events is the same as executing a program except that a "1" is output to the single step control port (DFH) instead of a "0". The circuit decodes the double M1 instructions (CBH, DDH, EDH, or FDH) and M1 is used to clock a shift register circuit which (if a "1" is output to port DFH) generates a nonmaskable interrupt at the start of the instruction to be single stepped. The nonmaskable interrupt saves the address of execution on the stack and causes the next instruction to be fetched from address E066H. The shift register is clocked twice after the

MDX-SST BOARD PHOTO

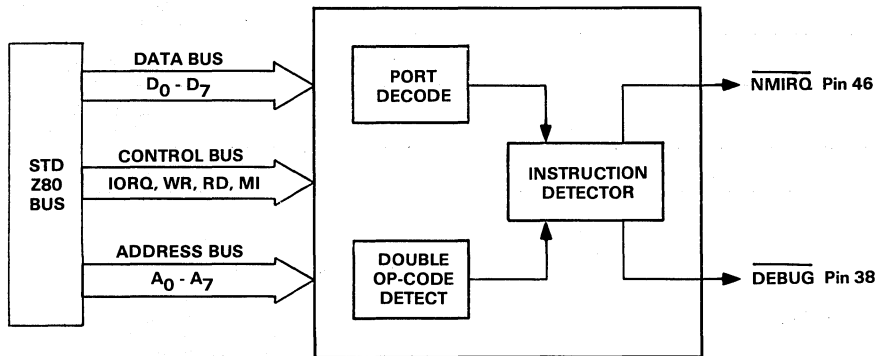


MD SERIES
SPECIAL FUNCTIONS

nonmaskable interrupt, causing the signal DEBUG to go low, forcing "E" on the most significant address lines, and causing the instruction to be fetched from E066H in the operating system RAM. The operating system then jumps to E069H, clears the debug flip-flop by reading PORT DFH, saves the CPU registers in the scratch RAM, and waits for the next command.

The single-step command is implemented in DDT-80, which resides on the MDX-DEBUG board and has the following format.

MDX-SST BLOCK DIAGRAM



S COMMAND (Single-step)

This command allows the user to start single-stepping from a given location for a given number of instructions and to display the CPU registers after each step.

Format:

- .S aaaa,nn,b(cr) start single-stepping at location aaaa for nn steps or instructions. If b=0, display only the PC and AF registers; if b≠0, display all the CPU registers.
- .S aaaa,nn(cr) the same as above with b=0 assumed.
- .S aaaa(cr) the same as above with nn=1 and b=0 assumed.
- .S (cr) b=0 assumed; aaaa is set equal to the contents of the user's PC.

The use of the MDX-SST board requires the MDX-CPU1 or MDX-CPU2 and the MDX-DEBUG. Also, system RAM must be present from FF00 to FFFF.

PORT ADDRESS (HEX)

DF

SYSTEM CLOCK

MIN.	MAX.
500kHz	4.0MHz

SYSTEM INTERRUPT UNITS (SIU) = 0

STD BUS INTERFACE

Inputs: One 74LS load max.
 Outputs: $I_{OH} = -3mA$ min. at 2.4 volts
 $I_{OL} = 24mA$ min. at 0.5 volts

OPERATING TEMPERATURE

0°C to 60°C

POWER SUPPLY REQUIREMENTS

+5VDC at 85mA

CARD DIMENSIONS

4.5 in (11.43cm) high by 6.50 in. (16.51cm) long
 0.48 in (1.22cm) maximum profile thickness
 0.062 in. (0.16cm) printed-circuit-board thickness

CONNECTORS

Function	Configuration	Mating Connector
STD-Z80 BUS	56-pin 0.125 in. centers	PRINTED CIRCUIT Viking 3VH28/1CE5 WIRE WRAP Viking 3VH28/ 1CND5 SOLDER LUG Viking 3VH28/ 1CN5

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
MDX-SST	Single-Step Module, includes Operations Manual	MK77958
	MDX-SST Operations Manual Only	MK79638

**MD SERIES
SPECIAL FUNCTIONS**

MICRO SYSTEMS DATA BOOK

I	Table of Contents
II	General Information
III	STD-Z80 BUS
IV	MDX Series Data Processing
V	MD Series Input/Output
VI	MD Series Memory
VII	MD Series Special Functions
VIII	MD Series Accessories
IX	MD Series Data Processing
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XII	SDE Series Memory
XIII	SDE Series Accessories
XIV	Software Disk Based
XV	Development Systems
XVI	Systems Emulation Boards
XVII	Peripherals

MOSTEK®

MD SERIES ACCESSORIES

MD-ACC

**MK77952, MK77953, MK77955,
MK77956, MK77957, MK77959,
MK77969, MK77970, MK77973, MK79089**

INTRODUCTION

The following items are available as accessories to support design, development, and production of products designed around the Mostek MD Series Z80* microcomputer modules:

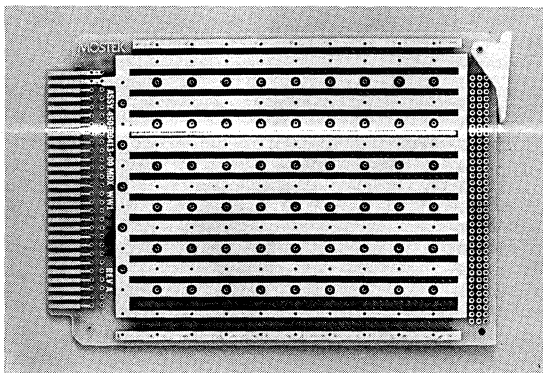
MDX-WW1	Wire-wrap card with bussed power and ground
MDX-WW2	Wire-wrap card without bussed power and ground
MD-EXT	Extender card
MD-232DCE-C	25-pin D female MD cable
MD-232DTE-C	25-pin D male MD cable
MD-TTY-C	Molex-TTY cable
MD-PPG-C	PROM Programmer (PPG-8/16) interface cable
MD-CPRT-C	MDX-PIO to Centronics Line Printer Interface Cable
MD-CC6	6-slot card cage
MD-CC12	12-slot card cage

WIRE-WRAP CARDS

The MDX-WW1 (MK77959) is a wire-wrap card with bussed power and ground lines on the board to facilitate fabrication of circuits using wire-wrap sockets. A series of plated-through holes are available on the top of the card for mounting connectors.

WW1 PHOTO MK77959

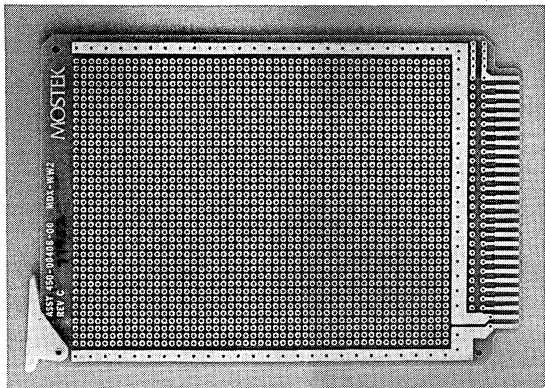
Figure 1



The MDX-WW2 (MK77952) is a wire-wrap card with all plated-through holes on a 0.100-inch grid. This allows mounting of both DIP sockets and discrete components for circuit fabrication. The plated-through holes accept 0.025-inch square posts.

WW2 PHOTO MK77952

Figure 2

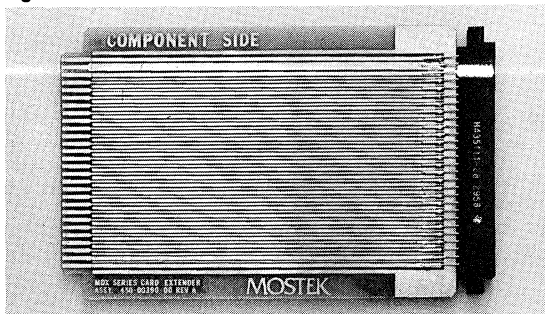


EXTENDER CARD

The MD-EXT (MK77953) is a card that allows extending cards for ready access. The card has a ground trace in between each signal line to minimize stray coupling of the bus signals.

MD-EXT PHOTO MK77953

Figure 3



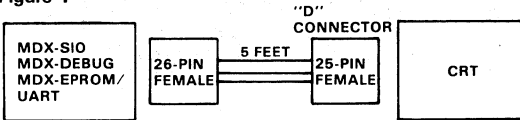
*Z80 is a register Trademark of ZILOG

CABLES

The MD-232DCE-C (MK77955) is a cable designed to interface with either the MDX-SIO or MDX-EPROM/UART. One end has a 26-pin socket to connect to the board. The other end has a 25-pin female "D"-type connector. This allows the board to provide a Data Communication Equipment interface.

MD-232DCE-C MK77955

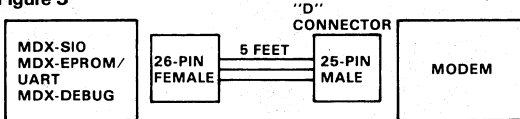
Figure 4



The MD-232DTE-C (MK77970) is a cable designed to interface with either the MDX-SIO or MDX-EPROM/UART. One end has a 26-pin socket to connect to the board. The other end has a 25-pin male "D"-type connector. This allows the board to provide a Data Terminal Equipment interface.

MD-232DTE-C MK77970

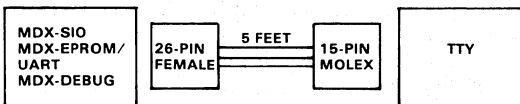
Figure 5



The MD-TTY-C (MK77956) is a cable designed to interface with either the MDX-SIO or MDX-EPROM/UART. One end has a 26-pin socket to connect to the board. The other end has a Molex connector that allows connection to the terminal block in a teletype.

MD-TTY-C MK77956

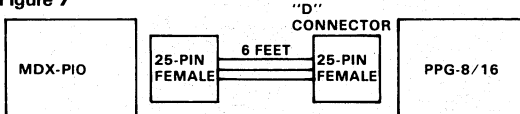
Figure 6



The MD-PPG-C (MK77957) is a cable designed to interface the MDX-PIO with the PPG-8/16 PROM Programmer.

MD-PPG-C MK77957

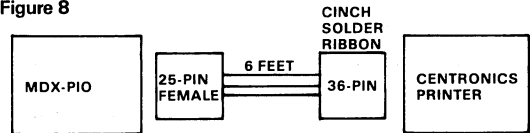
Figure 7



The MD-CPRT-C (MK79089) is a cable designed to interface the MATRIX System or the MDX-PIO with the Centronics Line Printer.

MD-CPRT-C MK79089

Figure 8

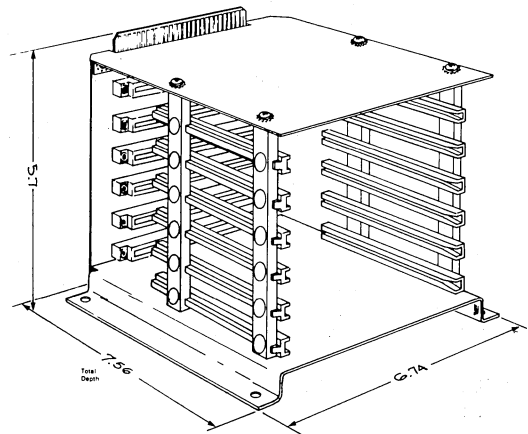


CARD CAGES

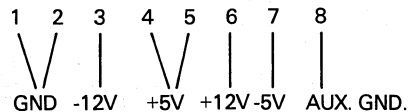
Two card cage versions, MD-CC6 (MK77973) and MD-CC12 (MK77969), are available from Mostek. Both models have connectors on 0.75-inch centers and the cards are inserted horizontally.

MD-CC6 DRAWING WITH DIMENSIONS

Figure 9



The motherboard has eight plated-thru holes in which to insert 16-gauge wire (max.) for the power and ground connections. These are designated below:



The pins are denoted from left to right on the fab side of the motherboard.

Table 1 shows the interconnection of the power plane to the STD BUS.

Table 1

Connection Pins (Left to Right)	Designator	STD Bus Pin No.
1, 2	GND	3, 4
3	-12V	56
4, 5	+5V	1, 2
6	+12V	55
7	-5V	5, 6
8	AUX. GND	53, 54

A connector is available on the lower-right edge of the motherboard for remoting +12V for a lamp and PB RESET if the user desires a remote reset switch. The configuration is shown below.

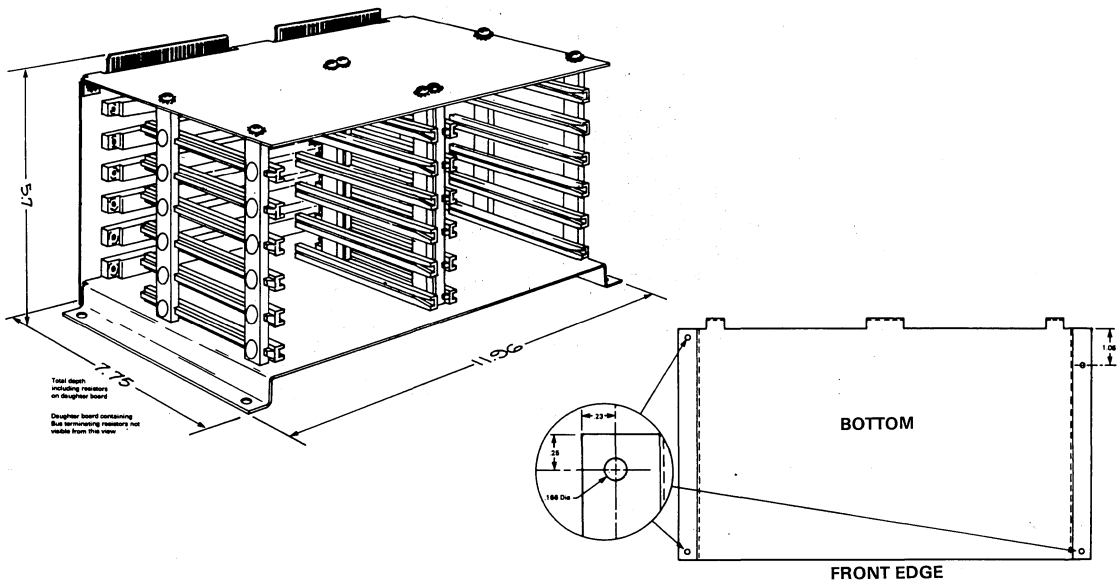
5	+12V
4	GND
3	PB RESET
2	GND
1	KEY

Wire is not supplied with the card cage modules.

The diagram shows the relative location of the connectors on the fab side of the motherboard.

MD-CC12 DRAWING WITH DIMENSIONS

Figure 10



MD SERIES ACCESSORIES

MD-CC6/MD-CC12 MOTHERBOARD (FAB SIDE)

NOTE: Two stake pins are provided which are connected to bus pins 35 (IOEXP) and 36 (MEMEX). These signals are not used on Mostek MK cards and, if desired, can be wire-wrapped to the ground stake pins provided at the bottom of the motherboard (as shown).

The priority interrupt for the twelve-slot card cage (MD-CC12) is from bottom to top on the right side, then from bottom to top on the left side when viewed from the front with the components facing upward. Thus the bottom-most right-hand board is the highest priority board and the top-most left-hand board is the lowest priority board.

PRIORITY INTERRUPT CHAIN

If a card slot is not used, the user can maintain the priority interrupt chain by strapping across the unused connector to the stake pins provided on the assembly side of the motherboard opposite pins 51 and 52.

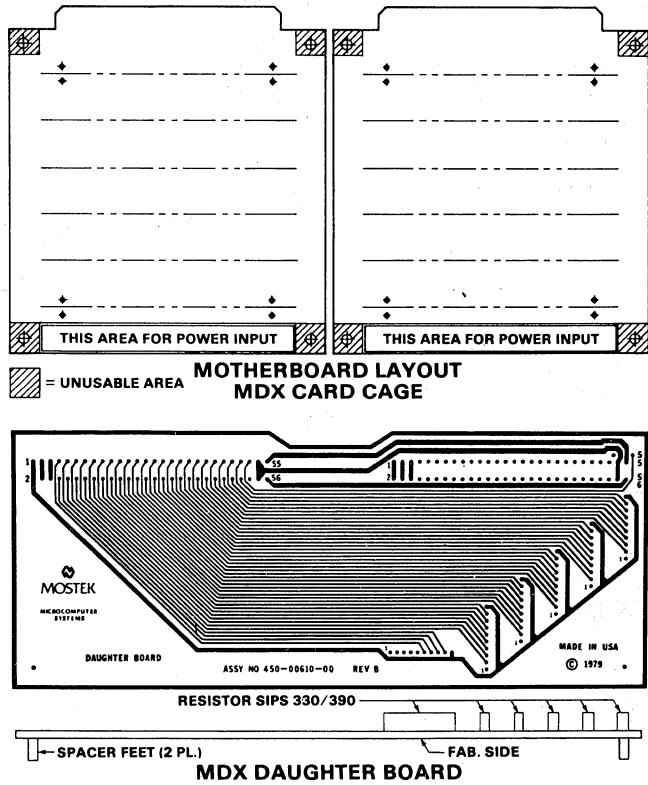
CARD DIMENSIONS

The priority interrupt is from bottom to top on the six-slot card cage (MD-CC6) when viewed from the front with the components facing upward.

4.5 in. (11.43 cm) high by 6.50 in. (16.51 cm) long
 0.680 in. (1.71 cm) maximum profile thickness
 0.062 in. (0.16 cm) printed-circuit-board thickness

MD-CC6/MD-CC12 MOTHERBOARD

Figure 11



CONNECTORS

Function	Configuration	Mating Connector
STD-Z80 BUS	56-pin 0.125 in. centers	PRINTED CIRCUIT Viking 3VH28/ICE5
		WIRE WRAP Viking 3VH28/ICND5
		SOLDER LUG Viking 3VH28/ICN5
Remote	5-pin SIP 0.100 in. centers	CONN. HOUSING AMP 87499-9 CONTACT PINS AMP87046-1

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
MDX-WW1	MD Series wire-wrap card with bussed power and ground	MK77959
MDX-WW2	MD Series wire-wrap card without bussed power and ground	MK77952
MD-EXT	MD Series extender card	MK77953
MD-CC6	MD Series 6-slot card cage with STD BUS motherboard	MK77973
MD-CC12	MD Series 12-slot card cage with STD BUS motherboard	MK77969
MD-232DCE-C	26-pin to 25-pin D -RS232 cable	MK77955
MD-232DTE-C	MD Cable 25-pin D plug to 26-pin socket	MK77970
MD-TTY-C	26-pin to Molex-TTY connector	MK77956
MD-PPG-C	PROM Programmer (PPG-8/16) Interface Cable to MDX-PIO	MK77957
MD-CPRT-C	Centronics Line Printer Interface Cable to MDX-PIO	MK79089

**MD SERIES
ACCESSORIES**

MOSTEK®

MD SERIES ACCESSORIES

MD-PWR1

MK77964

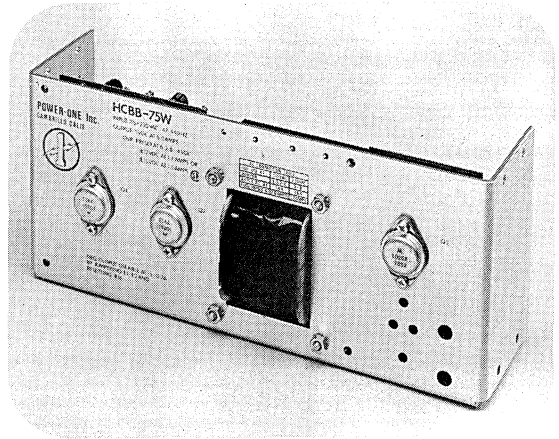
FEATURES

- Triple output supply: +5 volts and ± 12 volts
- 115/230 vac $\pm 10\%$, 47-440 Hz
- Remote sensing on 5V output
- Overvoltage protection on 5V output (standard); optional on $\pm 12V$ outputs
- $\pm 0.05\%$ regulation
- Foldback current limit
- I.C. regulated design
- UL recognized
- CSA certified

DESCRIPTION

The MD-PWR1 is an open-frame power supply. Designed to furnish power for the MDX-PROTO kit, the MD-PWR1 operates from 115/230 vac $\pm 10\%$ at a frequency range of

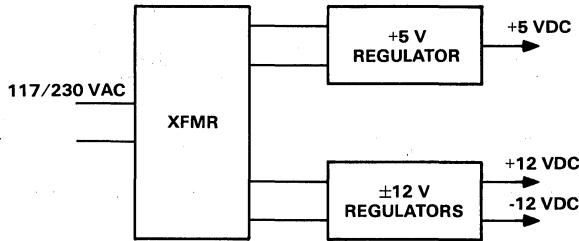
MD-PWR1 PHOTO



MD SERIES
ACCESSORIES

47 to 440 Hz. This input power is then transformed and regulated into the three output voltages, +5 VDC and ± 12 VDC. The open-frame design allows for adequate cooling.

MD-PWR1 BLOCK DIAGRAM



AC INPUT

115/230 vac, 47-440 Hz

DC OUTPUT

+5V @ 6.0A

± 12V @ 1.7A

(Derate output current 10% for 50 Hz operation)

LINE REGULATION

±.05% for a 10% line change

LOAD REGULATION

± .05% for a 50% load change

OUTPUT RIPPLE

3.0 mV Pk-Pk max.

TRANSIENT RESPONSE

30 microseconds for 50% load change

SHORT CIRCUIT AND OVERVOLTAGE PROTECTION

Automatic current limit/foldback

REVERSE VOLTAGE PROTECTION

Provided on output and pass element

OVERVOLTAGE PROTECTION

Optional on ± 12V outputs

REMOTE SENSING

Provided on 5V output, open-sense-lead protection built-in

STABILITY

± 0.3% for 24 hours after warm up

TEMPERATURE RATING

0°C to 50°C full rated

(derate linearly to 40% at 70°C)

TEMPERATURE COEFFICIENT

± .03%/°C max.

EFFICIENCY

5V output: 45%, ± 12V output: 55%

VIBRATION AND SHOCK

Per MIL-STD-810B

SIZE

4.75 in (12.07 cm) wide x 11.0 in (27.94 cm) long x

2.75 in (6.99 cm) high

WEIGHT

8 lbs (3.6 kg)

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
MD-PWR1	Power Supply Module with prestripped and tinned wires	MK77964

MOSTEK®

MD SERIES ACCESSORIES

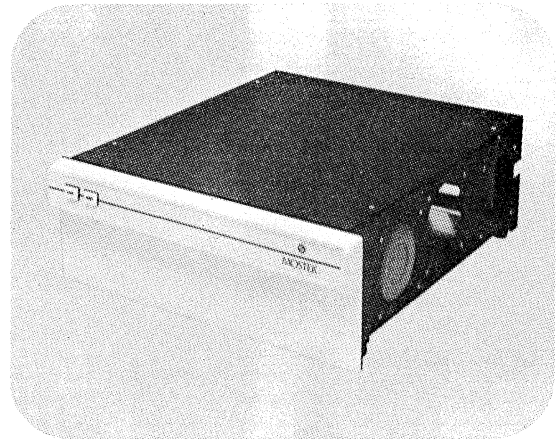
MD-RMC12

MK77966, MK77975

FEATURES

- Standard 19-inch rack-mountable chassis
- Removable structural-foam front panel for internal access
- Front panel RESET switch and POWER indicator
- 12-slot card cage
- Cards mounted horizontally for ease of cooling and cable routing
- Self-contained power supply and 115 CFM fan
- 100/115/230 Volt 50/60 Hz operation

MD-RMC12 - Frontview

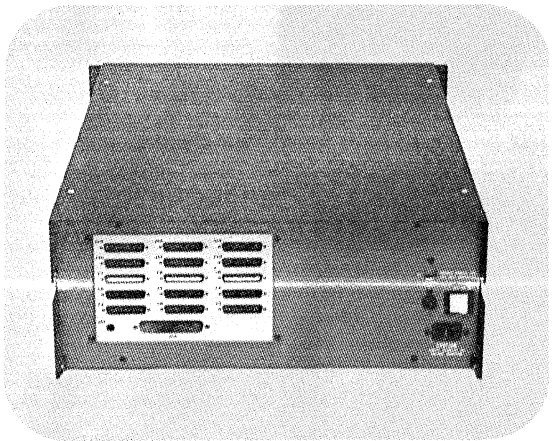


MD SERIES
ACCESSORIES

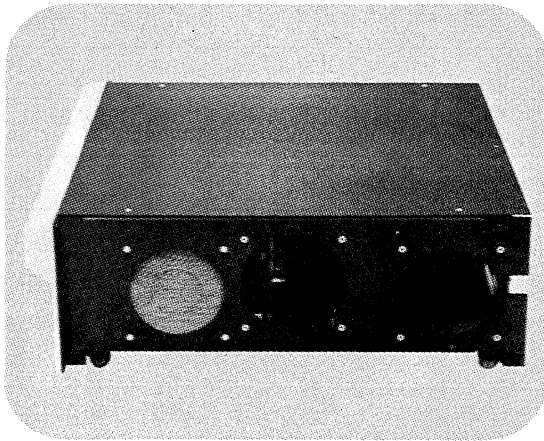
DESCRIPTION

The Mostek MD SERIES Rack-Mounted System (MD-RMC12) provides rack mounting for the MD Series Microcomputer modules. The system features a self-contained power supply designed to work on voltages and frequencies available world wide. A structural foam front panel is provided with system RESET and POWER indicator. The front panel is designed with quick-release ball studs so that it can be quickly removed for access to internal components. Card cage and power supply may be removed individually from front or top for improved access. The cards are mounted in a horizontal plane with provisions for cabling over the card cage to the rear I/O panel. The back panel has an I/O panel pre-punched for twelve 25-pin "D" type connectors, one 50-pin "D" connector and one BNC connector. AC components on the back panel include: On/Off switch, voltage selection switch, fuse holder (3AG or 5 x 20 mm), and AC input receptacle/line filter.

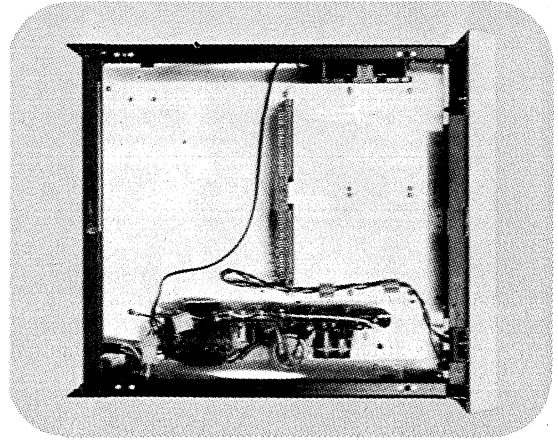
MD-RMC 12 - Rearview



MD-RMC 12 - Sideview



MD-RMC 12 - Topview, inside



INPUT POWER: 100/115/230 Volts AC \pm 10%
50/60Hz

DC POWER AVAILABLE: +5 VDC at 12A max.
+12 VDC at 1.7A max.
-12 VDC at 1.7A max.

LOAD REGULATION: \pm .05% for a 50% load change

OUTPUT RIPPLE: 3.0 mV Pk-Pk max.

TRANSIENT RESPONSE: 30 microseconds for a 50%
load change

**SHORT CIRCUIT AND
OVERLOAD PROTECTION:** Automatic current
limit/foldback

OVERVOLTAGE PROTECTION: +5 Volt output, set to
6.2 \pm 0.4 Volts

STABILITY: \pm 0.3% for 24 hours after warmup

THERMAL PROTECTION: Bi-metal thermostat on
primary AC line set to cut
out at 180°F (82°C)

CARD CAGE: Twelve-slot for MD series module
11.4cm x 16.5 cm (4.5 x 6.5 in). No PC
modules are supplied.

FUSING:

Line

Voltage
110/115V
230 V

MK77966
3 Amp 3AG*
1.5 Amp 3AG

MK77975
3 Amp 5 x 20 mm
1.5 Amp
5 x 20mm*

*Configuration as shipped

LINE CORD SUPPLIED:

MK77966

Similar to Belden model
17205B

MK77975

Similar to Feller model
1100

FRONT PANEL CONTROLS: RESET switch
POWER ON Indicator

REAR PANEL CONTROLS: AC Power On/Off
AC fuse holder
AC line receptacle/filter
AC line voltage selector

WEIGHT: 25 lbs (11.3 kg)

CHASSIS: a) 19" rack-mountable using the two rails
supplied
b) Slide mounting available with optional slide
mounting kit. Requires two inches of panel
space below the unit.

OPERATING TEMPERATURE RANGE: 0°C to 60°C

HEIGHT: 7.0 in. (17.8cm) panel space
7.3 in. (18.5cm) overall, including feet

WIDTH: 19.0 in. (48.3cm) at front panel
17.5 in. (44.5cm) behind front panel

DEPTH: 21.1 in. (53.6cm) with all protrusions
20.0 in. (50.8 cm) without foam front

HUMIDITY: Up to 90% relative, non-condensing

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
MD-RMC12	Rack-mounted CPU subsystem with MD series 12-slot card cage with U.S. line cord and fuse. 100/115/230 Volts 50/60Hz AC operation, front panel, support bracket for rack mounting, and Operation Manual included.	MK77966
MD-RMC12-50	Same as above except with 5 x 20mm fuse and European line cord.	MK77975
	MD-RMC12 Operations Manual Only	MK79738

MD SERIES
ACCESSORIES

MOSTEK®

PERIPHERAL

R MDFSS

MK78183, MK78185

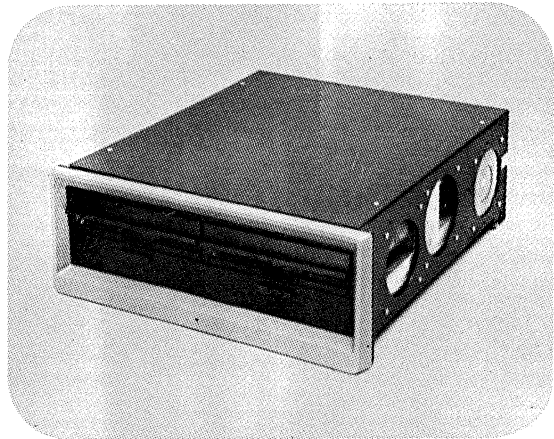
FEATURES

- Standard 19-inch rack-mountable chassis; 7-inch panel height
- Removable structural foam disk bezel for internal access
- Front panel POWER-ON indicator
- Mounts two standard 8-inch floppy disk drives
- Disks mounted horizontally for low profile
- Self-contained power supply and 115 CFM fan
- 100/115/230 Volt, 50/60 Hz operation

GENERAL DESCRIPTION

The Mostek R MDFSS offers a solution to rack mounting two standard 8-inch floppy disk drives. The system features a self-contained power supply designed to work on voltages and frequencies available worldwide. An attractive structural foam-front disk bezel is provided with a power-on indicator. The disk bezel is designed with quick-release ball studs so that it can be easily removed for access to the drives. The drives are mounted in a horizontal plane for a low-profile appearance and to conserve panel height in the rack. Drives and power supply may be removed individually

R MDFSS PHOTO



from front or top for ease of maintenance. The back panel has an I/O panel prepunched for one 50-pin "D" interface to the disk controller. AC components on the back panel include: On/Off switch, voltage selection switch, fuse holder (3AG or 5 x 20 mm) and AC input receptacle/line filter.

MD SERIES
ACCESSORIES

INPUT POWER100/115/230 Volts AC \pm 10% 50/60Hz

50Hz	60Hz
MK78185	MK78183

DC POWER AVAILABLE

+5 VDC at 3.0A max.
 -5 VDC at 0.5A max.
 +24 VDC at 3.4A max.

LOAD REGULATION \pm .05% for a 50% load change**OUTPUT RIPPLE**

3.0 mV PK-PK max.

TRANSIENT RESPONSE

30 microseconds for a 50% load change

SHORT CIRCUIT AND OVERLOAD PROTECTION

Automatic current limit/foldback

OVERVOLTAGE PROTECTION+5 Volt output set to 6.2 ± 0.4 Volts**STABILITY** \pm 0.3% for 24 hours after warmup**THERMAL PROTECTION**

Bi-metal thermostat on primary AC line set to cut out at 180°F (82°C)

DISK DRIVES

Shugart 800-2 or equivalent

FUSING

Line Voltage	MK78183	MK78185
110/115V	3 Amp 3AG*	3 Amp 5 x 20 mm
230 V	1.5 Amp 3AG	1.5 Amp 5 x 20mm*

*Configuration as shipped

LINE CORD SUPPLIED

MK78183	MK78185
Similar to Belden model 17205B	Similar to Feller model 1100

FRONT PANEL INDICATOR

Power-on

REAR PANEL CONTROLS

AC Power On/Off
 AC fuse holder
 AC line receptacle/filter
 AC line voltage selector

WEIGHT

50 lbs (22.7 kg)

OPERATING TEMPERATURE RANGE

0°C to 40°C (Disk Media Limitation)

DIMENSIONS

Height: 7.0 in. (17.8 cm) panel space
 7.3 in. (18.5 cm) overall, includes feet

Width: 19.0 in. (48.3 cm) at front panel
 17.5 in. (44.5 cm) behind front panel

Depth: 21.1 in. (54.0 cm) with all protrusions
 20.0 in. (50.8 cm) without foam front

HUMIDITY

Up to 90% relative, noncondensing.

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
R MDFSS	Rack-mountable dual floppy enclosure with 8-inch drives for 100/115/230 Volt operation. Includes interface cable to SDE-RMC6 or MD-RMC12, front disk bezel, support bracket for rack mounting and Operations Manual. 60Hz model.	MK78183
R MDFSS-50	50 Hz model.	MK78185
	R MDFSS Operations Manual Only	MK79740

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MOSTEK®

MD SERIES DATA PROCESSING

MD-SBC1 MK77851-0

FEATURES

- Z80 Microprocessor
- 2K byte RAM capacity with 1K included
- Sockets for 8K bytes 2716 EPROM
- Crystal clock - 2.5 MHz
- Three TTL-buffered 8-bit OUTPUT ports
- Two TTL-buffered 8-bit INPUT ports
- Two interrupt inputs
- Single +5 volt power supply

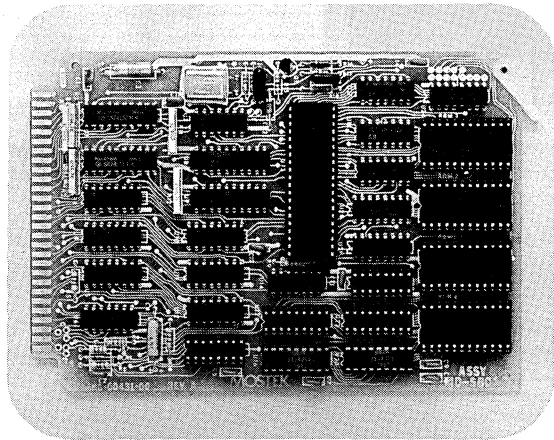
DESCRIPTION

The MD-SBC1 is a complete Z80-based microcomputer on a 4½ inch by 6½ inch circuit module. All I/O is fully TTL-buffered and is brought to a 56-pin edge connector.

The smaller card size and the single power supply makes the MD-SBC1 easier to package and easier to use than most other modules. While the module size is small, no compromises have been made in computing power due to increasing MOS-LSI densities and the use of the Z80 microcomputer. The 40 buffered TTL I/O lines and the 8K bytes of EPROM provide the capability to solve many control problems encountered by the OEM microcomputer user. The expandable MD Series (MDX) has the same form factor allowing easy expansion to a multi-board system with increased capability.

Figure 1 is a block diagram of the MD-SBC1. The basic module comes with 1K bytes of RAM expandable to 2K bytes by the addition of two 2114-type RAMs. Four 2716

MD-SBC1 BOARD PHOTO



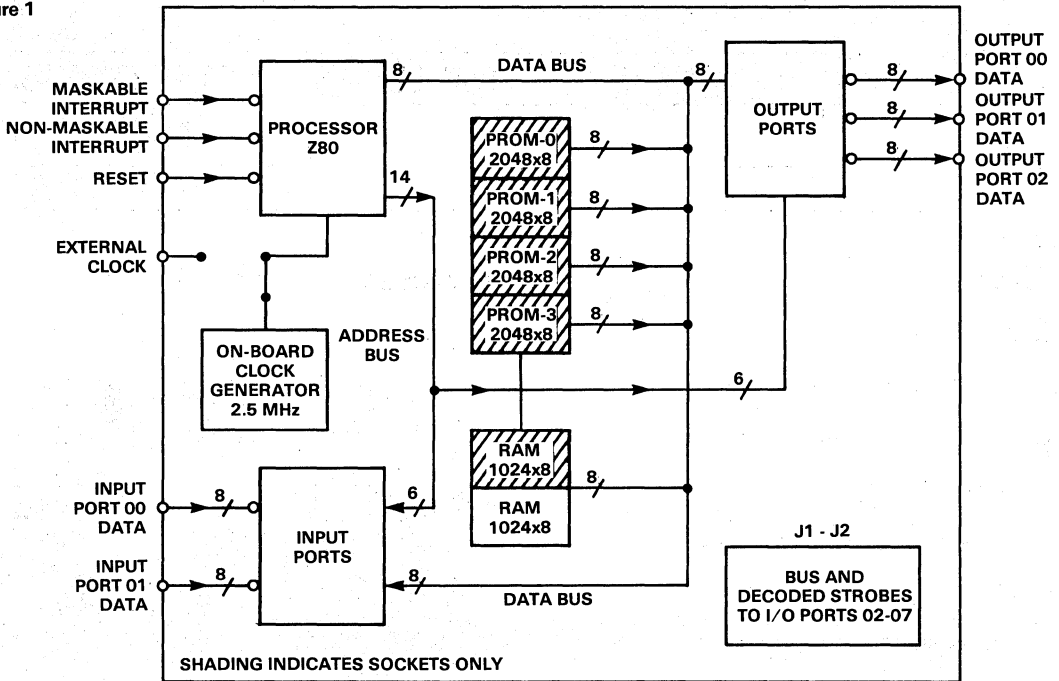
MD SERIES
DATA PROCESSING

sockets are provided for up to 8K byte of EPROM, and are decoded in 2K blocks starting at address zero. The output ports are 74LS244 latches which are brought to the card cage connector. The input ports are 74LS240 Octal Buffers with 4.7K Ohm pull-up resistors on the inputs. These input lines are also brought to the edge connector. The Z80-CPU is driven by a crystal clock at 2.5MHz (400nsec T-State).

Both the $\overline{\text{NMI}}$ and $\overline{\text{INT}}$ interrupt inputs to the Z80-CPU are terminated with 4.7K Ohm pull ups and brought to the card edge connector. An external clock can be used by changing strapping options on the board. Power-on-reset circuitry is included on the CPU's RESET input. Provision is made to expand the I/O capability through the use of on-board connectors.

MD-SBC1 BLOCK DIAGRAM

Figure 1



WORD SIZE

Instruction: 8, 16, 24 or 32 bits
 Data: 8 bits

CYCLE TIME

Clock period (T state): 400 ns at 2.5 MHz
 Instruction Cycle: Min. 4 T states
 Max. 23 T states

MEMORY CAPACITY

8K bytes of 2716 memory (none included)
 2K bytes of 2114 memory (1K bytes included)

MEMORY ADDRESSING

EPROM Number	HEX Address
0	0000-07FF
1	0800-0FFF
2	1000-17FF
3	1800-1FFF
RAM Number	HEX Address
Standard	2000-23FF
Optional	2400-27FF

MEMORY SPEED REQUIRED

Memory	Access Time Required	Cycle Time Required
2716*	450nsec	450nsec
2114	450nsec	450nsec

*Single 5 volt type required

I/O ADDRESSING AND CAPACITY

Port Type	HEX Address	Data Capacity
Input	00 and 01	16 lines
Output	00, 01, 02	24 lines

I/O INTERFACES

Inputs: One 74LS load plus a 4.7K-Ohm pull up resistor

Outputs: $I_{OH} = -3mA$ at $V_{OH} = 2.4$ volts
 $I_{OL} = 24mA$ at $V_{OL} = 0.5$ volts

INTERRUPTS

Two (active low): NMI and INT. See Z80 CPU (MK3880) Technical Manual for a full description of Z80 interrupts.

SYSTEM CLOCK

	MIN	MAX
MD-SBC1	250kHz	2.5MHz

CARD DIMENSIONS

4.5 in. (11.43 cm) high by 6.50 in. (16.51 cm) long
 0.48 in. (1.22 cm) maximum profile thickness
 0.062 in. (0.16 cm) printed circuit board thickness

CONNECTORS

Function	Configuration	Mating Connector
STD-Z80 BUS	56-pin 0.125 in. centers	PRINTED CIRCUIT Viking 3VH-28/ 1CE5 WIRE WRAP Viking 3VH-28/ 1CND5 SOLDER LUG Viking 3VH-28/ 1CN5

OPERATING TEMPERATURE RANGE

0°C to 60°C

POWER SUPPLY REQUIREMENTS

+5 volts \pm 5% at 1.2A max (fully loaded)
 (100mA per RAM, 100mA per EPROM)

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
MD-SBC1	Complete Z80 Single Board Computer with Operations Manual less EPROMs and mating connector.	MK77851-0
	MD-SBC1 Operations Manual only.	MK79609

MD SERIES
DATA PROCESSING

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SDE SERIES DATA PROCESSING

OEM-80E

MK78122, MK78124-3

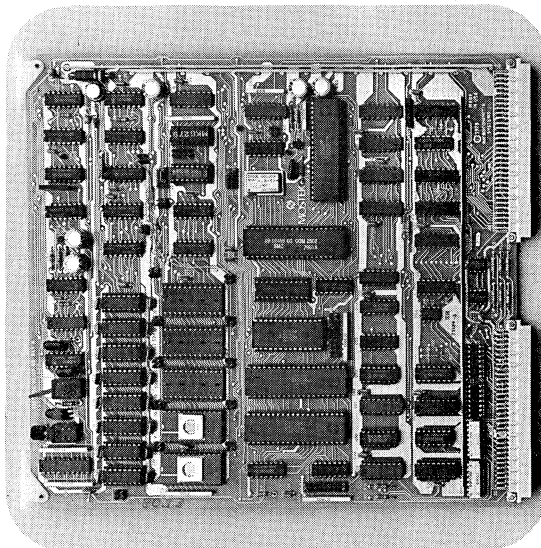
FEATURES

- Z80 CPU
- 20K x 8 EPROM
- Accepts 2708, 2716, or 2532 EPROM's
- 256 x 8 static scratchpad RAM on-board
- 16K (4K) x 8 dynamic RAM
- Z80 CTC - four counter/timer channels
- Restart to 0000H or E000H (switch option)
- On-board serial I/O port
- Software-programmable baud rate
- Current loop or RS-232-C (V.24) interface
- Four 8-bit parallel ports with handshake
- Ports buffered with TTL, socket-programmed
- Port direction in 4-bit blocks
- Programmable polarity on strobe lines
- Halt lamp
- Power-on-reset logic
- Fully hysteresis-buffered SDE bus

DESCRIPTION

The OEM-80E is a Z80 CPU-based computer board. The card has sufficient on-board I/O and memory to be used in a stand-alone mode in many applications, yet it is fully expandable to support more memory and I/O in applications requiring it. The five EPROM sockets on-board can be strapped to use a number of standard 24-pin ROM/EPROM products including PROMs and ROMs with capacities of up to 4K bytes each. The eight RAM sockets can be strapped for 4K or 16K RAMs, giving a maximum

OEM-80E BOARD PHOTO



16K bytes on-board. The Z80 built-in refresh logic reduces the area taken by the dynamic RAMs to that required by other manufacturers' 1K byte static RAM, the cost per bit being significantly reduced. Also on-board are two memory-decoding bipolar PROMs. These allow a wide range of RAM/PROM/ROM combinations to be selected by the user; if the exact combination required is not already supported, new PROMs can be easily programmed.

The user switch-selectable restart address allows the DDT-80 debug program to reside in the system without conflict with the user's own PROM-based software. If a problem develops, the user can switch from address 0 reset to address E000 (where DDT-80 resides) and use the powerful commands of the 2K byte DDT-80 to localize the problem.

The "E" format and DIN connectors allow quick integration into the user's system hardware. Putting all connectors on one card edge is a unique feature in microcomputer modules, although it is standard design practice for many large system builders. The simplified maintenance and clean cabling made possible by this technique should be appreciated by all experienced users.

SDE SERIES
DATA PROCESSING

MEMORY ADDRESSING AND CAPACITY

The recommended memory map is shown below:

0000-3FFF PROM (1 TO 16K)
4000-7FFF RAM (4 TO 16K)
8000-DFFF EXTERNAL MEMORY
E000-E7FF DDT-80 (2K)
E800-FEFF EXTERNAL MEMORY
FF00-FFFF SCRATCHPAD RAM (256 bytes,
needed only if DDT-80 is used)

Memory cycle time required for the PROMs is 450 ns.

SERIAL I/O PORTS

A UART with 20mA current loop and RS-232-C (V.24) buffers/drivers provides a serial communication channel for interfacing to TTY or CRT terminals or serial printers. The baud rate is software-programmable over the range of 110 to 9600 baud.

PARALLEL I/O PORTS

The four parallel ports are designed to allow maximum flexibility in matching the MOS I/O ports to the real world of long lines or high voltages. Two ports support bidirectional TTL I/O with hysteresis inputs. The ports can also be programmed for input or output only. The other ports are supplied with sockets which support a number of standard TTL devices for buffering. A list of pin-compatible devices is given below:

TYPE	USE
7400	16mA TTL inverting output
7402	TTL inverting input
7408	16mA TTL non-inverting output
7426	16mA high-voltage inverting open-collector output
7437	48mA TTL inverting output
7438	48mA TTL inverting open-collector output

COUNTER/TIMER CHANNELS

Four counter/timer channels are provided on the card in a Z80-CTC chip. One channel is used as the baud rate generator of the serial I/O port. The other three channels are available to the user. The channels may be programmed as delay generators, event counters or simply discrete interrupt inputs with a programmable edge trigger. The device can generate four interrupts.

INTERRUPTS

The OEM-80E has nine on-board interrupts. They are:

One Z80 CPU NMI (non-maskable interrupt)
Four Z80 PIO(2) Mod 2 Interrupts
Four Z80 CTC Mod 2 Interrupts

More interrupt devices (up to 128 total) can be added to the SDE bus.

BUS INTERFACE

All Z80 signals are buffered before leaving the OEM-80E. The buffering protects the MOS components from static charge during handling and from bus transients which could otherwise destroy these devices. The bus supports DMA transfers and the daisy-chained, multi-level interrupt structure of the Z80. The bus uses hysteresis-input receivers and current-limited bus drivers to improve the noise margin of the bus. Switching the bus drivers on only when data is needed and stable further reduces the noise on the bus.

POWER REQUIREMENTS

+5V \pm 5% at 1.5 A
+12V \pm 5% at 0.175 A
-12V \pm 5% at 0.1 A

OPERATING TEMPERATURE RANGE

0°C to 50°C

BOARD SIZE

233.4mm (9.19 in) X 250 mm (9.84 in.)

CONNECTORS

Two 64-pin DIN 41612 (a-c) indirect, male

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
OEM-80E/4	OEM-80E/4 with 4K bytes of RAM (MK4027), 5 sockets for EPROM or ROM, 2 PIOs with sockets for TTL buffering logic, CTC, UART, socket for 256-byte scratch-pad RAM and sockets for memory mapping PROMs.	MK78122
OEM-80E/16	Same as OEM-80E/4 except with 16K bytes of RAM (MK4116)	MK78124
	OEM-80E Operations Manual only	MK78548

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MOSTEK®

SDE SERIES INPUT/OUTPUT

A/D-80E

**MK78172-42, MK78172-56,
MK78175-40, MK78177-26**

FEATURES

A/D-80E/1791 - Analog Input/Output Board

MK78172-42

- Input ranges: $\pm 5V$
 - $\pm 10V$
 - 0 - 10V
 - 0 - 5V
- 16 Single Ended Input Channels
- 12 Bit A/D Converter
- Programmable Gain Option
- 2 D/A Output Channels with Scope Control

A/D-80E/1791 - Analog Input/Output Board

MK78172-56

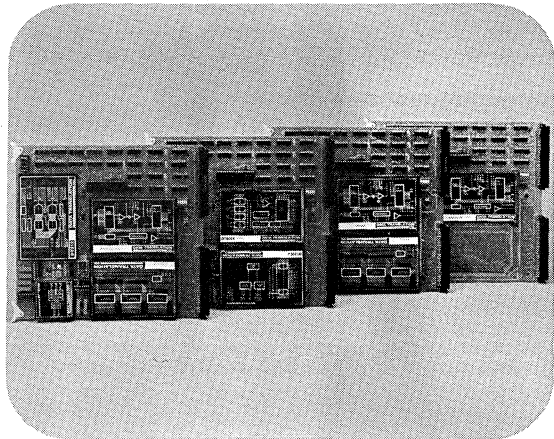
- Input ranges: $\pm 5V$
 - $\pm 10V$
 - 0 - 10V
 - 0 - 5V
- 32 Differential Input Channels
- 12 Bit A/D Converter
- Programmable Gain Option
- 2 D/A Output Channels with Scope Control

A/D-80E-1795 - Analog Input/Output Board

MK78175-40

- Low-level, Wide-range Input
- Input Ranges: $\pm 10mV$ to $\pm 10V$
- 16 Single Ended Input Channels

A/D-80E BOARD PHOTOS



- 12 Bit A/D Converter
- 2 D/A Output Channels with Scope Control

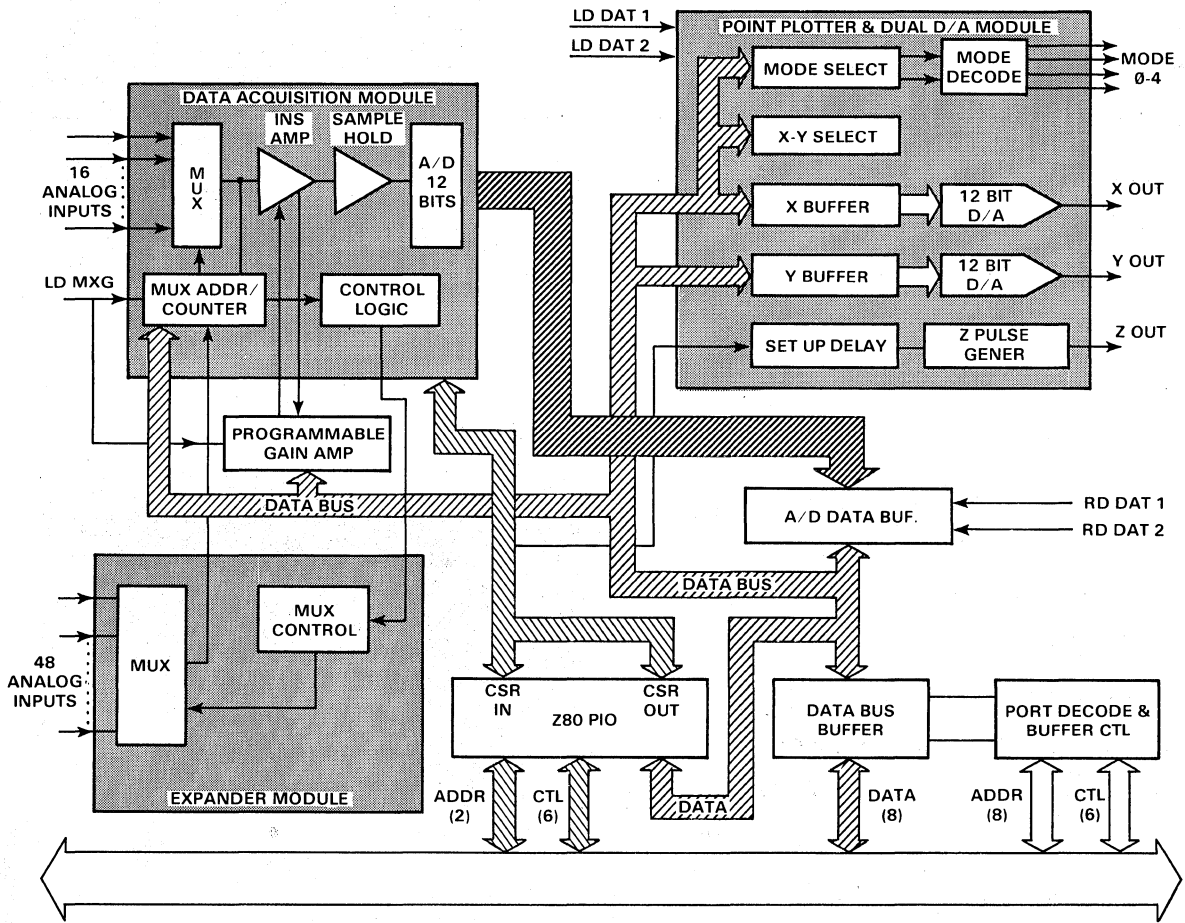
A/D-80E-1798 - Analog Input Board

MK78177-26

- Wide-range, Isolated Inputs
- Input Ranges: $\pm mV$ to $\pm 10V$
- 4 Double Ended Input Channels
- 12 Bit A/D Converter
- Programmable Gain Option

SDE SERIES
INPUT/OUTPUT

A/D-80E BLOCK DIAGRAM



DESCRIPTION

The A/D-80E line of analog I/O systems is offered as a part of the SD Series. Available in four different versions with various user-specified options, the A/D-80E can be contoured with the right combination of analog I/O to meet the system designer's needs.

The A/D-80E line of analog I/O boards has been designed using DATA-X-II™ data acquisition modules manufactured by Data Translation, Inc. Each DATA-X module is a complete self-contained unit with multiple shielding for operation in a microprocessor system. This eliminates ground-loop and noise problems inherent in interconnection of separate modules.

A/D-80E INTERFACE

The Z80-PIO chip and some external logic are utilized to provide the interface for the A/D-80E. In this manner, the Z80-PIO chip is used to provide all the interrupt circuitry for Z80-Mode 2 operation, i.e., a vectored daisy chain priority interrupt structure.

A/D-80E ANALOG INPUT SPECIFICATION

	A/D-80E/1791	A/D-80E/1795	A/D-80E/1798
Number of channels	16 single ended or 32 differential	16 single ended	4 differential
Input Impedance	100 megOhm	100 megOhm	10 megOhm
Input Overvoltage	±35V non-destructive	±15V non-destructive	15V DC max.
Input Range	0-5V, ±5V, 0-10V, ±10V	±10mV to ±10V	0-10V unipolar, ±10V bipolar
Optional programmable	gains: 1, 2, 4, 8	Not Available	gains: 1, 10, 100, 500
Conversion resolution	12 bits	12 bits	12 bits
Linearity	±½ LSB	±½ LSB	±½ LSB
Inherent quantizing error	±½ LSB	±½ LSB	±½ LSB
Stability Tempco	±25ppm/°C, F.S.R.	±30ppm/°C	Zero - ±20 micro Volt/°C Full Scale - ±30ppm/°C
Throughput	35kHz stand. 100kHz optional	31 kHz	20 Hz random 40 Hz sequential
Power Requirements	+5V @ 2.0A Max	+5V @ 2.0A Max	+5V @ 2.0A Max
Mechanical printed-circuit board	8.5" x 12.0" x .65"	8.5" x 12.0" x .65"	8.5" x 12.0" x .65"
Temperature	0° - 70°	0° - 70°	0° - 70°
Implementation	Programmed I/O and Interrupt Functions	Programmed I/O and Interrupt Functions	Programmed I/O and Interrupt Functions
Device address	Selectable via jumper	Selectable via jumper	Selectable via jumper

ANALOG OUTPUT SPECIFICATIONS

Resolution -	12 Bits	Z Axis Control -	The Interface contains all the control circuitry of Z axis and scope control mode bits
Linearity -	±½ LSB	Z Output (Intensity) -	LO (0.8V) to HI (2.4V) TTL compatible into 50 Ohm termination
Range -	±10V, 0-10V; @ 25mA minimum current output, all jumper selectable	Z Risetime -	100 nsec into 50 ft. of terminated COAX
Relative Accuracy -	±0.025%	Z Pulse Width -	Jumper Selectable a. 0.5 microsecond b. 5 microsecond c. external RC 1 microsecond to 0.5 msec
Full Scale Settling -	0.1% - 1 microsecond, 0.01% - 3 microsecond into 50 ft., coaxial cable terminated with 470 Ohm		
Temperature Coefficient -	25ppm/°C		

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
A/D-80E/1791-16	High Level, Analog Input/Output (16 S.E. Inputs)	MK78172-42
A/D-80E/1791-32	High Level, Analog Input/Output (32 D.E. Inputs)	MK78172-56
A/D-80E/1795	Low Level, Non-Isolated Analog Input/Output	MK78175-40
A/D-80E/1798	Wide Range Isolated Analog Input	MK78177-26
	A/D-80E Operations Manual Only	MK79660

MOSTEK®

SD SERIES INPUT/OUTPUT

DCC-80E

MK78192

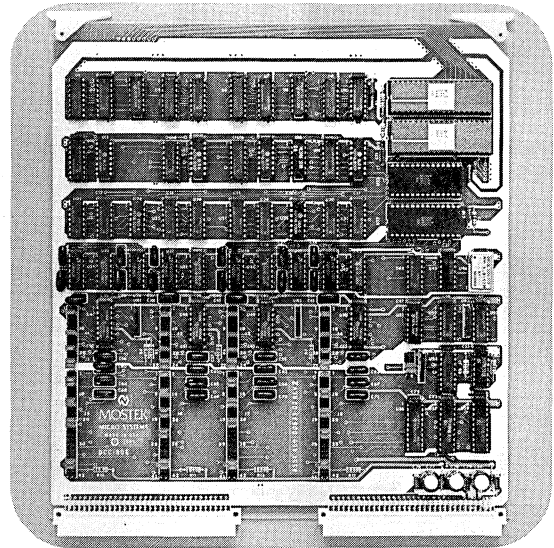
FEATURES

- Four independent full-duplex channels
- Independent programmable baud rate clocks
- Data rates - 75 to 38.4K bits per second
- Receiver data registers quadruply-buffered
- Transmitter data registers double-buffered
- Asynchronous operation
- Binary synchronous operation
- HDLC or IBM SDLC operation
- Both CRC-16 and CRC-CCITT (-0 and -1) hardware implemented
- Modem control
- Operates as DTE or DCE
- Serial input and output as RS-232-C
- Address programmable
- Compatible with SDE BUS
- 4-Channel NRZI encoder/decoder

DESCRIPTION

The Multichannel Serial Input/Output Module, DCC-80E, is designed to be a multiprotocol asynchronous or synchronous I/O module for the SDE BUS. The module is designed around the Mostek® MK3887™ Z80-SIO which provides two full-duplex serial data channels. Each channel has an independent programmable baud rate clock generator to increase module flexibility. Each channel is capable of handling asynchronous, synchronous, and synchronous bit-oriented protocols such as IBM BiSync, SDLC, HDLC, and virtually any other serial protocol. It can generate CRC codes in any synchronous mode and can be programmed by the CPU for any traditional asynchronous format. The serial

DCC-80E BOARD PHOTO



input and output data is fully buffered and is provided at the connector as RS-232-C levels. A modem control section is also provided for handshaking and status. The module can be jumper-configured as a data terminal (DTE) or as a modem (DCE) in order to facilitate a variety of interface configurations.

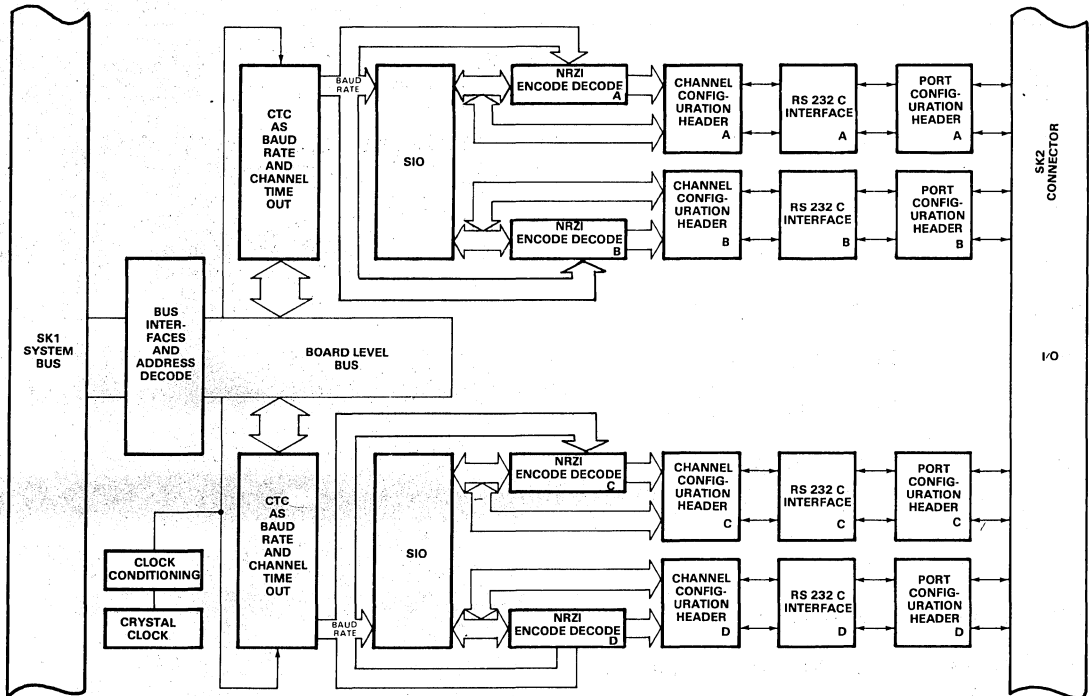
Figure 1 is a block diagram of the DCC-80E module which consists of eight main elements: the channel configuration headers, line drivers and receivers, MK3887 Z80-SIO, programmable CTC baud rate generators, address decode, NRZI encoder/decoder, clock circuitry, and data bus buffers. Input and output to the board is provided via the SK2 connector. The configuration and pin out headers of each channel are identical.

Several features are available as options that are selected by the port-configuration header. The headers are used to select the orientation of the data communication interface. The DCC-80E can be selected to act as either a terminal or processor (Data Terminal Equipment - DTE) or as the modem (Data Communications Equipment - DCE). The channel-configuration

SDE SERIES
INPUT/OUTPUT

DCC-80E BLOCK DIAGRAM

Figure 1



headers allow reconfiguration of data interchange and signals. This allows the data to be asynchronous or synchronous serial stream or synchronous NRZI encoded.

Line drivers and receivers provide the correct electrical signal levels, slew rate and impedance for interfacing RS-232-C peripherals.

The Mostek MK3887 Z80-SIO is the central element of this module. This device is a multifunction component designed to satisfy a wide variety of serial data communications requirements in microcomputer systems. Its basic role is that of a serial-to-parallel, parallel-to-serial converter/controller, but within that role it is configured by software programming so that its function can be optimized for a given serial data communications application. The MK3887 provides two independent, full-duplex channels: A and B. Each channel features the following:

ASYNCHRONOUS OPERATION

- 5, 6, 7, or 8 bits/character
- 1, 1 1/2 or 2 stop bits
- Even, odd or no parity

- X1, x16, x32, and x64 clock modes
- Break generation and detection
- Parity, Overrun, and Framing error detection

BINARY SYNCHRONOUS OPERATION

- One or two sync characters in separate registers
- Automatic sync character insertion
- CRC generation and checking

HDLC OR IBM SDLC OPERATION

- Automatic Zero Insertion and Deletion
- Automatic Flag Insertion
- Address Field Recognition
- I-Field Residue Handling
- Overrun protection for valid receive messages
- CRC generation and checking

The MK3887 also provides modem control inputs and outputs as well as daisy-chain priority interrupt logic. Eight different interrupt vectors can be generated by the SIO in response to various conditions affecting the data communications channel transmission and reception.

Address decoding, SDE BUS interface and bus management for the module are performed by the Address Decode and Data Bus circuit. The DCC-80E

contains command registers that are programmed to select the desired operational mode. The addressing scheme is as follows:

PORT ADDRESS	PORT FUNCTION
X 0 _H ...	CTC as baud-rate generator for Channel A
X 1 _H ...	CTC as programmable timer
X 2 _H ...	SIO Data Input/Output of Channel A
X 3 _H ...	SIO Status/Control for Channel A
X 4 _H ...	CTC as baud rate generator for Channel B
X 5 _H ...	CTC as programmable timer
X 6 _H ...	SIO Data Input/Output of Channel B
X 7 _H ...	SIO Status/Control for Channel B
X 8 _H ...	CTC as baud rate generator for Channel C
X 9 _H ...	CTC as programmable timer
X A _H ...	SIO Data Input/Output of Channel C
X B _H ...	SIO Status/Control for Channel C
X C _H ...	CTC as baud generator for Channel D
X D _H ...	CTC as programmable timer
X E _H ...	SIO Data Input/Output of Channel D
X F _H ...	SIO Status/Control for Channel D

The CTC channels used as baud rate generators are controlled through ports X0H, X4H, X8H, and XCH.

Remaining ports (X1H, X5H, X9H, XDH) may be used as programmable timers for Time-Out checks.

Ports X2H, X6H, XAH, and XEH are data channels of Z80-SIO devices. The CPU loads them with data to be sent and conversely reads back data assembled in the receiver buffer.

The write registers 0-7 of the SIO are preset by write operation on ports X3H, X7H, XBH, AND XFH to control proper operation.

(The X indicates the binary code necessary to represent which one of the 64 port addresses is selected.)

SERIAL BAUD RATES

Each channel has an individual programmable baud rate generator. The X1 multiplier on the Z80-SIO must be used in the synchronous mode. The X16, X32, or X64 Z80-SIO clock rate can be specified for the asynchronous mode. Table 1 indicates the possible baud rates available for both operation modes.

STANDARD BAUD RATE

Table 1

Standard Baud Rate	
Asynchronous	Synchronous
50	
75	
110	
150	600
300	1200
600	2400
1200	4800
2400	9600
4800	19,200
9600	38,400
19,200	
38,400	

OPERATIONAL FEATURES

The channel interface connects DCC-80E to data terminal/communications equipment. It consists of four basic parts.

1. Drivers and Receivers for RS-232-C
2. NRZI encoder
3. NRZI clock recovery circuit

Operation of DCC-80E can be tailored to any functional environment by means of prewiring two jumper fields, per channel, to one desired configuration.

WORD SIZE

Data: 5,6,7,8 bits
I/O addressing: 8-bits

I/O CAPACITY

Serial: Four full-duplex serial ports, either synchronous or asynchronous. Special control registers and circuitry to permit implementation of SDLC, BiSync, Monosync, HDLC, and other formats can be programmed. All synchronous formats can be NRZI encoded.

I/O ADDRESSING

On-board fully programmable

SIO SERIES
INPUT/OUTPUT

INTERRUPTS

Generates vectored interrupts to 32 different locations corresponding to conditions within four SIO channels and four CTC channels. Interrupt vector location programmable. Daisy-chained priority interrupt circuitry.

SYSTEM CLOCK

	MIN.	MAX.
DCC-80E	250kHz	2.5MHz

SYSTEM INTERRUPT UNITS (SIU) = 3

OPERATING TEMPERATURE

0°C to 50°C

POWER SUPPLY REQUIREMENTS

+12 volts \pm 5% at 120mA max.
 -12 volts \pm 5% at 80mA max.
 +5 volts \pm 5% at 1.2 A max.

CARD DIMENSIONS

233.4 mm x 257.62 mm x 25 mm

ORDER INFORMATION

DESIGNATOR	DESCRIPTION	PART NUMBER
DCC-80E	Four-channel data communication controller module with operations manual.	MK78192
	DCC-80E Operations Manual Only	MK79812

MOSTEK®

SD SERIES INPUT/OUTPUT

FLP-80E

MK78146

FEATURES

- Soft-sector format compatible with IBM 3740 data entry system format
- Capable of controlling up to four flexible disk drives per subsystem
- Full disk initialization (Formatting)
- Full-sector (128 bytes) FIFO buffering for data
- Double buffering for control and status
- Automatic track-seek with verification
- Completely interruptable for real-time systems

APPLICATIONS

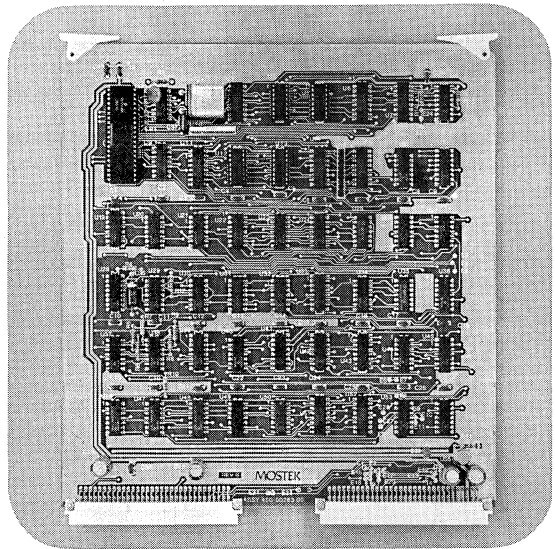
- Flexible disk-drive interface for use with Mostek's Software Development Board (OEM-80E) in a disk-based Z80 Development System (MATRIX).
- Single or multiple flexible disk-drive controller/formatter for disk-based OEM systems using the OEM-80E Single Board Computer.

DESCRIPTION

The FLP-80E is an add-on flexible disk controller module used to interface up to four flexible disk drives to the Mostek Software Development Board (OEM-80E).

The FLP-80E provides the necessary electronics to

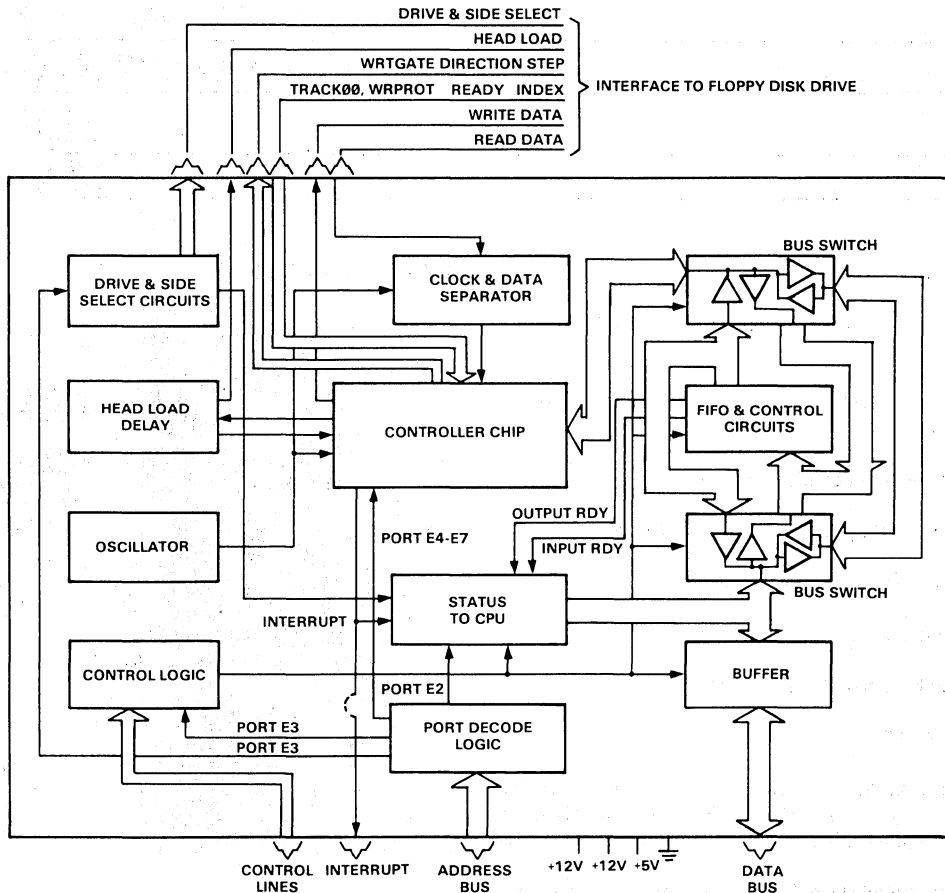
FLP-80E BOARD PHOTO



accomplish track selection, head loading, data transfer, error detection, flexible drive interface, status reporting and format generation/recognition. The FLP-80E is designed to operate with either Shugart SA-800 Single-Sided or SA-850 Double-Sided Flexible Disk Drives. In addition to functioning as an add-on card to the OEM-80E system, the FLP-80E may be utilized directly in OEM applications to control/format up to four flexible disk drives of either single- or dual-sided type in 8080A or Z80 systems.

SDE SERIES
INPUT/OUTPUT

FLP-80E BLOCK DIAGRAM



AVAILABLE SOFTWARE

Software for the FLP-80E disk controller is the Mostek Disk Operating System (FLP-80DOS). A user can easily design his own OEM software package around 20 powerful disk operating system commands permitting complex record insertion, deletion, and position manipulation. Other software includes application packages such as an advanced monitor and debugger, disk-based Text Editor, Z80 Assembler, Relocating Linking Loader, Peripheral Interchange Program, and a channelized I/O system for each peripheral interface. These programs provide state-of-the-art software for developing Z80 programs as well as establishing a firm basis for OEM products. Further information is provided in the FLP-80DOS Data Sheet, MK78556.

OPERATING TEMPERATURE RANGE

-0°C to 50°C

POWER SUPPLY REQUIREMENTS (Typical)

+12V ± 5% at 0.006A
 +5V ± 5% at 1.1A
 -12V ± 5% at 0.03A

INTERFACE LEVELS

TTL Compatible

BOARD SIZE

250mm x 233.4mm x 18mm

BOTTOM CONNECTOR

Dual 64-pin Eurocard Connector, DIN 41612 form D; A and C pinned.

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
FLP-80E	FLP-80E Disk Controller Board with Operations Manual, FLP-80DOS bootstrap PROMs and diskette with FLP-80DOS Operations Manual.	MK78146
	FLP-80E Operations Manual. Detailed description of use and operation of FLP-80E.	MK78561
FLP-80DOS Data Sheet	Disk Operating System data sheet.	MK78556
	FLP-80DOS Operations Manual. Detailed description of the use and operation of FLP-80DOS.	MK78557

SDE SERIES
SUT SERIES
INPUT/OUTPUT

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MOSTEK®

SDE SERIES MEMORY

RAM-80E

MK78109, MK78110

FEATURES

- Memory Capacity
 - RAM-80AE — 16,384 (16K) bytes using MK4027 RAM
 - RAM-80BE — 16,384 (16K) bytes expandable to 65,536 (65K) bytes using MK4116 RAM
 - RAM-80BE under page-mode operation — up to one megabyte of memory
- I/O Capacity (RAM-80BE only)
 - Four 8-bit ports with handshake lines

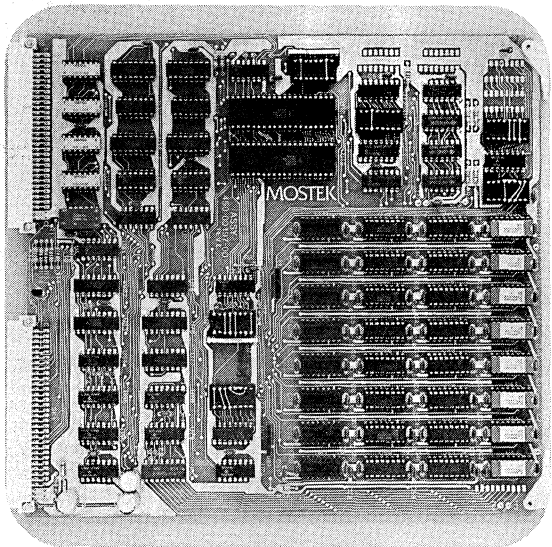
DESCRIPTION

The RAM-80E is designed to provide RAM expansion capability for the Z80-based OEM-80E microcomputer. For user flexibility, it is offered in two basic configurations designated RAM-80AE and RAM-80BE.

The RAM-80AE is the basic 16K-byte RAM board for users requiring the most economical means for adding RAM to an OEM-80E microcomputer. It is designed using the high-performance MK4027-4, 4096 x 1-bit dynamic RAM, and includes address strapping options for positioning the decoded memory space to start on any 4K incremental address boundary.

The RAM-80BE is a combination memory and I/O expansion board. The memory may be configured to have a memory capacity of 16K, 32K, 48K, or 65K bytes of RAM. This on-board memory expandability is made possible by population options of either eight, sixteen, twenty-four or thirty-two MK4116-4 (16,384 x 1 MOS dynamic RAM)

RAM-80E BOARD PHOTO

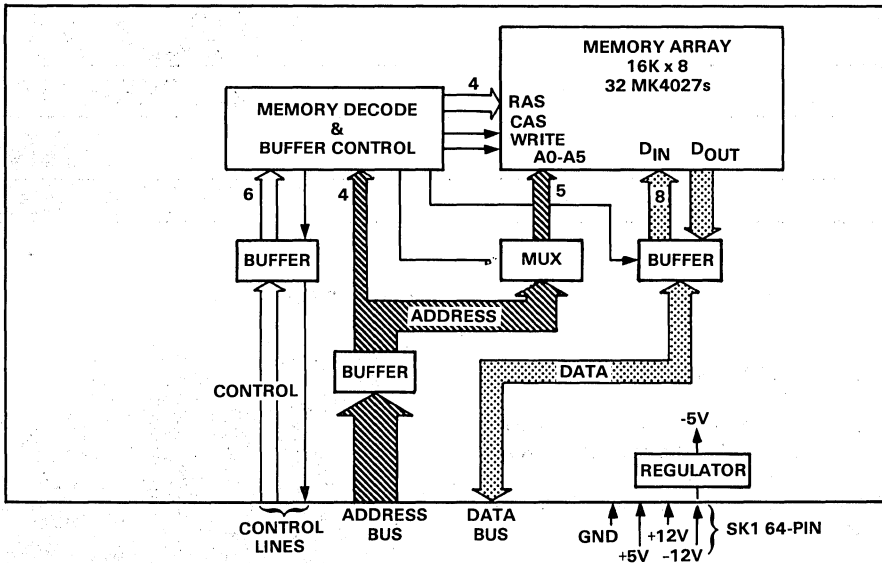


memories. The RAM-80BE provides strapping options for positioning the decoded memory space to start on any 16K address boundary. In addition to the add-on memory, the RAM-80BE provides four 8-bit I/O ports from the two on-board MK3881 Z80 PIO circuits. Each I/O port is fully TTL-buffered and has two handshake lines per I/O port. The RAM-80BE also includes logic for "Page-Mode Operation" which permits up to 1 megabyte of memory (sixteen 65K x 8 RAM-80BEs) to be used in a single OEM-80E system.

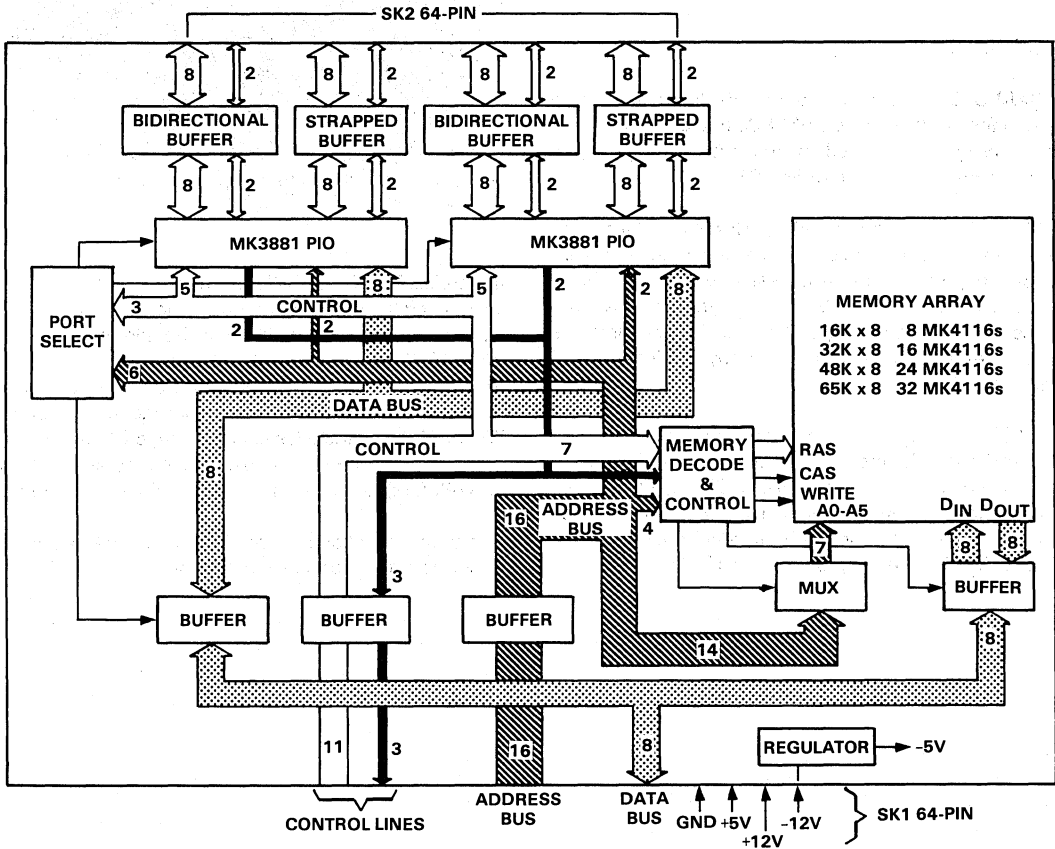
A complete set of documentation for each RAM-80E board is available to ensure easy utilization.

SDE SERIES
MEMORY

RAM-80AE BLOCK DIAGRAM



RAM-80BE BLOCKDIAGRAM



MEMORY ACCESS TIME

345ns (maximum)

MEMORY CYCLE TIME

450ns (minimum)

OPERATING TEMPERATURE

0°C to 50°C

POWER SUPPLY REQUIREMENTS

Voltage	RAM-80AE	RAM-80BE
+12V±5%	200mA typ. 575mA max.	200mA typ. 575mA max.
-12V±5%	25mA typ. 30mA max.	25mA typ. 30mA max.
+5V±5%	370mA typ. 550mA max.	1.1A typ. 1.5A max.

BOARD SIZE

250 mm x 233.4 mm x 18 mm

CONNECTOR

Dual 64-pin Eurocard Connector

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
RAM-80AE	16,384-byte RAM board with 32-MK4027s	MK78109
RAM-80BE	Expandable 16,384-byte RAM board with 8-MK4116s, sockets for additional MK4116s, 2—MK3881 Z80 PIOs, plus page-mode capability.	MK78110
	RAM-80BE Operations Manual. Complete description of the electrical specifications, timing, and circuit operation of the RAM-80BE. Also includes a detailed schematic diagram, assembly drawing and parts list.	MK78555
	RAM-80AE Operations Manual. Complete description of the electrical specifications, timing, and circuit operation of the RAM-80AE. Also includes a detailed schematic diagram, assembly drawing, and parts list.	MK78574

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MOSTEK[®]

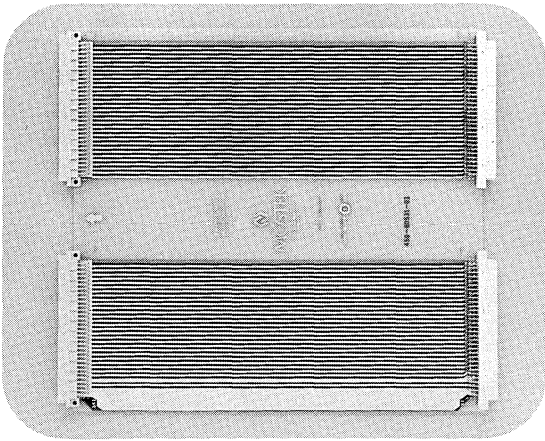
SDE SERIES ACCESSORIES

SDE-ACC

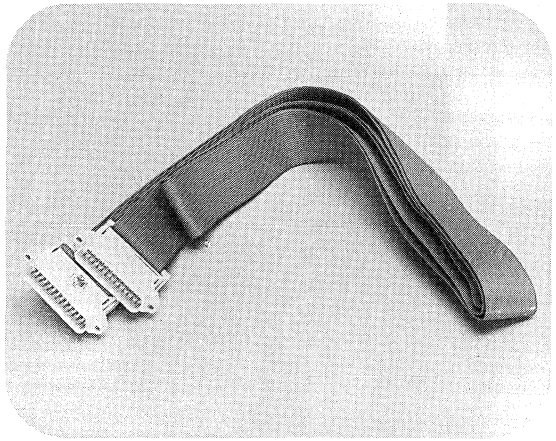
MK78152, MK79062, MK79088

The following SD Accessories are available.

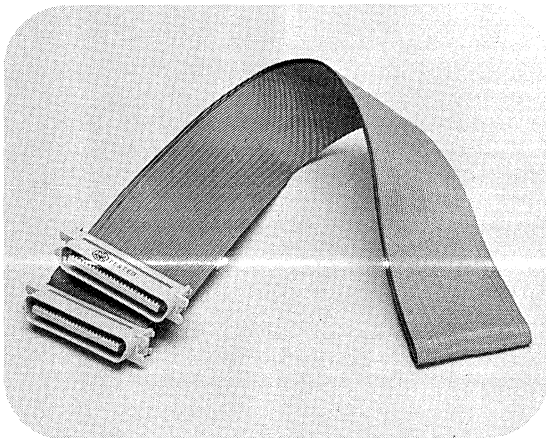
SDE-EXTENDER BOARD



SDE-RMC6 to CRT CABLE



RMS-DFE CABLE 50 PIN



SDE SERIES
ACCESSORIES

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
SDE-EXT	SDE Extender Board	MK79062
SDE-RMC6 to CRT	Interface Cable to CRT	MK78152
RMS-DFE Cable 50 Pin	Interface Cable to Floppy Disc Enclosure	MK79088

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SD SERIES ACCESSORIES

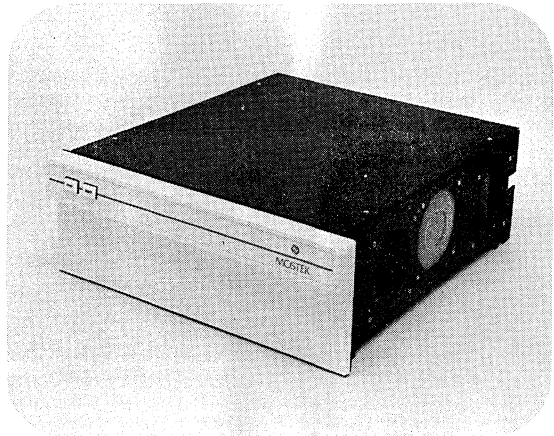
SDE-RMC6

MK78182-1, MK78182-2

FEATURES

- Standard 19-inch rack-mountable chassis; 7-inch panel height
- Removable structural foam front panel for internal access
- Front panel RESET switch and POWER-ON indicator
- Six-slot card cage
- Cards mounted horizontally for ease of cooling and cable routing
- Self-contained power supply and 115 CFM fan
- 100/115/230 Volt 50/60 Hz operation

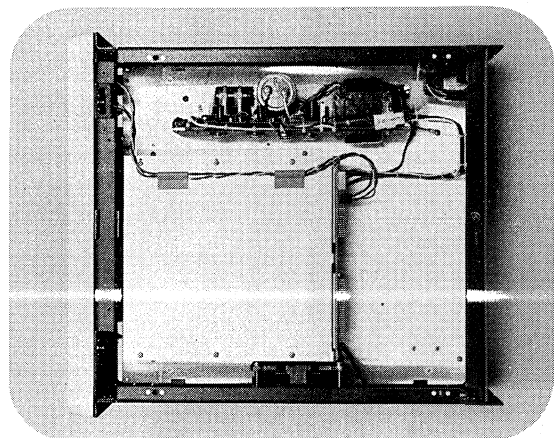
SD-RMC6 PHOTO



DESCRIPTION

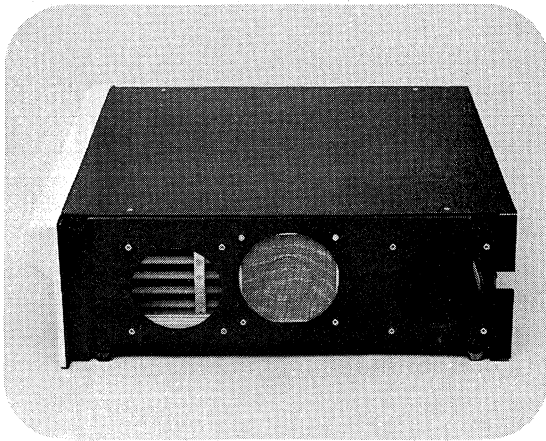
The Mostek SD Series rack-mount system (SDE-RMC6) offers a solution to rack mounting the line of SDE Series Microcomputer modules. The system features a self-contained power supply designed to work on voltages and frequencies available world-wide. All components are easily removed from front or top for improved maintenance. An attractive structural foam front panel is provided with system RESET switch and POWER-ON indicator. The front panel is designed with quick-release ball studs so that it can be quickly removed for access to internal components. The cards are mounted in a horizontal plane with I/O cabling at the rear of the card cage. The back panel has an I/O panel pre-punched for twelve 25-pin "D" type connectors, one 50-pin "D" connector, and one BNC connector for versatility. AC components on the back panel were selected to meet UL and VDE requirements and include: On/Off switch, voltage selection switch, fuse holder (3AG or 5 x 20 mm), and AC input receptacle/line filter.

SD-RMC6 Interior View

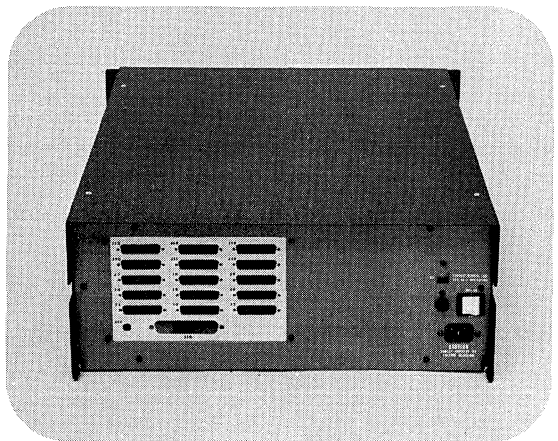


SDE SERIES
ACCESSORIES

SE-RMC6 Side View



SD-RMC6 Rear View



INPUT POWER

100/115/230 volts AC \pm 10% 50/60Hz

DC POWER AVAILABLE

+5 VDC at 12A max.
+12 VDC at 1.7A max.
-12 VDC at 1.7A max.

LOAD REGULATION

\pm .05% for a 50% load change

OUTPUT RIPPLE

3.0 mV PK-PK max.

TRANSIENT RESPONSE

30 microseconds for a 50% load change

SHORT CIRCUIT AND OVERLOAD PROTECTION

Automatic current limit/foldback

OVERVOLTAGE PROTECTION

+5 Volt output, set to 6.2 ± 0.4 volts

STABILITY

\pm 0.3% for 24 hours after warmup

THERMAL PROTECTION

Bi-metal thermostat or primary AC line set to cut out at 180°F (82°C)

CARD CAGE

Six slot for SD/E series module (250mm x 233.4mm) (9.19 x 9.84 in). Wire-wrap tail connector provided for SK2 I/O connectors. All SK1 connectors wired one-to-one. No PC modules supplied.

FUSING

Line Voltage	MK78182	MK78182-E
110/115V	3 Amp 3AG*	3 Amp 5 x 20 mm
230 V	1.5 Amp 3AG	1.5 Amp 5 x 20mm*

*Configuration as shipped

LINE CORD SUPPLIED

MK78182	MK78182-E
Similar to Belden model 17205B	Similar to Feller model 1100

FRONT PANEL CONTROLS

RESET switch
POWER ON Indicator

REAR PANEL CONTROLS

AC Power On/Off
AC fuse holder
AC line receptacle/filter
AC line voltage selector

WEIGHT

25 lbs (11.3 kg)

CHASSIS

- a) 19" rack-mountable using the two rails supplied.
- b) Slide mounting available with optional slide mounting bit and requires two inches of panel space below the unit.

OPERATING TEMPERATURE RANGE

0°C to 60°C

HUMIDITY

Up to 90% relative, non-condensing

DIMENSIONS

Height: 7.0 in. (17.8 cm) panel space
7.3 in. (18.5 cm) overall, including feet

Width: 19.0 in. (48.3 cm) at front panel
17.5 in. (44.5 cm) behind front panel

Depth: 21.1 in. (53.6 cm) with all protrusions
20.0 in. (50.8 cm) without foam front

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
SDE-RMC6	Rack-mounted CPU subsystem with SD/E series six-slot card cage with U.S. line cord and fuse. 100/115/230 Volts 50/60 Hz AC operation front panel, rails for rack mounting and operation manual included.	MK78182-1
SDE-RMC6-50	Same as above except with 5 x 20 mm fuse and European line cord.	MK78182-2
SDE-RMC6 to CRT	CRT Interface Cable Only	MK78152
	SDE-RMC6 Operations Manual Only	MK79783

The following Mostek modules are compatible with the above CPU subsystem

OEM-80E	CPU Module Data Sheet	MK78550
RAM-80E	RAM Expander Data Sheet	MK78590
FLP-80E	Floppy Disk Interface Data Sheet	MK78572
VDI	Video Display Interface Data Sheet	MK78591
A/D-80E	A/D-D/A Interface Data Sheet	MK79709

SDE SERIES
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MOSTEK®

SOFTWARE DISK BASED

FLP-80DOS

MK78142, MK77962

INTRODUCTION

The Mostek FLP-80DOS software package is designed for the Mostek dual floppy disk Z80 Development System or an MD board system. Further information on this system can be found in the MATRIX™ Data Sheet. FLP-80DOS includes:

- Monitor
- Debugger
- Text Editor
- Z80 Assembler
- Relocating Linking Loader
- Peripheral Interchange Program
- Linker
- A Generalized I/O System For Peripherals

These programs provide state-of-the-art software for developing Z80 programs as well as establishing a firm basis for OEM products.

MONITOR

The Monitor provides user interface from the console to the rest of the software. The user can load and run system programs, such as the Assembler, using one simple command. Programs in object and binary format can be loaded into and dumped from RAM. All I/O is done via channels which are identified by Logical Unit Numbers. The Monitor allows any software device handler to be assigned to any Logical Unit Number. Thus, the software provides complete flexibility in configuring the system with different peripherals. The Monitor also allows two-character mnemonics to represent 16-bit address values. Using mnemonics simplifies the command language. Certain mnemonics are reserved for I/O device handlers such as 'DK' for the flexible disk handler. The user can create and assign his own mnemonics at any time from the console, thus simplifying the command language for his own use. The Monitor also allows "batch mode operation" from any input device or file.

The Monitor commands are:

- \$ASSIGN** - assign a Logic Unit Number to a device.
- \$CLEAR** - remove the assignment of a Logical Unit Number to a device.
- \$RTABLE** - print a list of current Logic Unit Number-to-Device assignments.

FLP-80DOS BOARD PHOTO



- \$DTABLE** - print default Logical Unit Number-to-Device assignments.
- \$LOAD** - load object modules into RAM.
- \$GTABLE** - print a listing of global symbol table.
- \$GINIT** - initialize global symbol table.
- \$DUMP** - dump RAM to a device in object format.
- \$GET** - load a binary file into RAM from disk.
- \$SAVE** - save a binary file on disk.
- \$BEGIN** - start execution of a loaded program.
- \$INIT** - initialize disk handler.
- \$DDT** - enter DDT debug environment.
- IMPLIED RUN COMMAND** - get and start execution of a binary file.

DESIGNER'S DEVELOPMENT TOOL - DDT

The DDT debugger program is supplied in a combination of ... on the FLP-80DOS diskette... and absolute Z80 programs. Standard commands allow displaying and modifying memory and CPU registers, setting breakpoints, and executing programs. Mnemonics are used to represent Z80 registers, thus simplifying the command language.

SOFTWARE
DISK BASED

The allowed commands are:

- B - Insert a breakpoint in user's program.
- C - Copy contents of a block of memory to another location in memory.
- E - Execute a program.
- F - Fill an area of RAM with a constant.
- H - 16-bit hexadecimal arithmetic.
- L - Locate and print every occurrence of an 8-bit pattern.
- M - Display, update, or tabulate the contents of memory.
- P - Display or update the contents of a port.
- R - Display the contents of the user's register.
- S - Hardware single step - requires Mostek's AIM-80 board or AIM-Z80A board.
- W - Software single step.
- V - Verify memory (compare two blocks and print differences).

TEXT EDITOR - EDIT

The FLP-80DOS Editor permits random-access editing of ASCII character strings. The Editor works on blocks of characters which are rolled in from disk. It can be used as a line-or character-oriented editor. Individual characters may be located by position or context. Each edited block is automatically rolled out to disk after editing. Although the Editor is used primarily for creating and modifying Z80 assembly language source statements, it may be applied to any ASCII text delimited by "carriage returns".

The Editor has a pseudo-macro command processing option. Up to two sets of commands may be stored and processed at any time during the editing process. The Editor allows the following commands:

- An - Advance record pointer n records.
- Bn - Backup record pointer n records.
- Cn dS1dS2d - Change string S1 to string S2 for n occurrences.
- Dn - Delete the next n records.
- En - Exchange current records with records to be inserted.
- Fn - If n = 0, reduce printout to console device (for TTY and slow consoles).
- I - Insert records.
- Ln - Go to line number n.
- Mn - Enter commands into one of two alternate command buffers (pseudo-macro).
- Q - Quit - Return to Monitor.
- Sn dS1d - Search for nth occurrence of string S1.
- T - Insert records at top of file before first record.
- Vn - Output n records to console device.
- Wn - Output n records to Logical Unit Number five (LUN 5) with line numbers.
- Xn - Execute alternate command buffer n.

Z80 ASSEMBLER - ASM

The FLP-80DOS Assembler reads standard Z80 source

mnemonics and pseudo-ops and outputs an assembly listing and object code. The assembly listing shows address, machine code, statement number, and source statement. The code is in industry-standard hexadecimal format modified for relocatable, linkable assemblies.

The Assembler supports conditional assemblies, global symbols, relocatable programs, and a printed symbol table. It can assemble any length program, limited only by a symbol table size of over 400 symbols. Expressions involving arithmetic and logical operations are allowed. Although normally used as a two-pass assembler, the Assembler can also be run as a single-pass assembler or as a learning tool. The following pseudo-ops are supported:

- COND - same as IF.
- DEFB - define byte.
- DEFL - define label.
- DEFM - define message (ASCII).
- DEFS - define storage.
- DEFW - define word.
- END - end statement.
- ENDC - same as ENDIF.
- ENDIF - end of conditional assembly.
- EQU - equate label.
- GLOBAL - global symbol definition.
- IF - conditional assembly.
- INCLUDE - include another file within an assembly.
- NAME - program name definition.
- ORG - program origin.
- PSECT - program section definition.
- EJECT - eject a page of listing.
- TITLE - place heading at top of each page of listing.
- LIST - turn listing on.
- NLIST - turn listing off.

RELOCATING LINKING LOADER - RLL

The Mostek FLP-80DOS Relocating Linking Loader provides state-of-the-art capability for loading programs into memory. Loading and linking of any number of relocatable or nonrelocatable object modules is done in one pass. A non-relocatable module is always loaded at its starting address as defined by the ORG pseudo-op during assembly. A relocatable object module can be positioned anywhere in memory at an offset address.

The Loader automatically links and relocates global symbols which are used to provide communication or linkage between program modules. As object modules are loaded, a table containing global symbol references and definitions is built up. The symbol table can be printed to list all global symbols and their load address. The number of object modules which can be loaded by the Loader is limited only by the amount of RAM available for the modules and the symbol table.

The Loader also loads industry-standard non-relocatable, non-linkable object modules.

LINKER - LINK

The Linker provides capability for linking object modules together and creating a binary (RAM image) file on disk. A binary file can be loaded using the Monitor GET or IMPLIED RUN command. Modules are linked together using global symbols for communication between modules. The linker produces a global symbol table and a global cross reference table which may be listed on any output device.

The Linker also provides a library search option for all global symbols undefined after the specified object modules are processed. If a symbol is undefined, the Linker searches the disk for an object file having the file-name of the symbol. If the file is found, it is linked with the main module in an attempt to resolve the undefined symbol.

PERIPHERAL INTERCHANGE PROGRAM - PIP

The Peripheral Interchange Program provides complete file maintenance facilities for the system. In addition, it can be used to copy information from any device or file to any other device or file. The command language is easy to use and resembles that used on DEC minicomputers. The following commands are supported:

COMMAND	FUNCTION
APPEND	Append files.
COPY	Copy files from any device to another device or file.
DIRECT	List Directory of specified Disk Unit.
ERASE	Delete a file.
FORMAT	Format a disk.
INIT	Initialize the disk handler.
RENAME	Rename a file.
STATUS	List number of used and available sectors on specified disk unit.
QUIT	Return to Monitor.

The first letter only of each command may be used.

DISK OPERATING SOFTWARE

The disk software, as well as being the heart of the MATRIX development system, can be used directly in OEM applications. The software consists of two programs which provide a complete disk handling facility.

INPUT/OUTPUT CONTROL SYSTEM - IOCS

The first package is called the I/O Control System (IOCS). This is a generalized blocker/deblocker which can interface to any device handler. Input and output can be done via the IOCS in any of four modes:

1. Single-byte transfer.
2. Line at a time, where the end of a line is defined by carriage return.
3. Multibyte transfers, where the number of bytes to be transferred is defined as the logical record length.
4. Continuous transfer to end-of-file, which is used for binary (RAM-image) files.

The IOCS provides easy application of I/O oriented packages to any device. There is one entry point, and all parameters are passed via a vector defined by the calling program. Any given handler defines the physical attributes of its device which are, in turn, used by the IOCS to perform blocking and deblocking.

FLOPPY DISK HANDLER - FDH

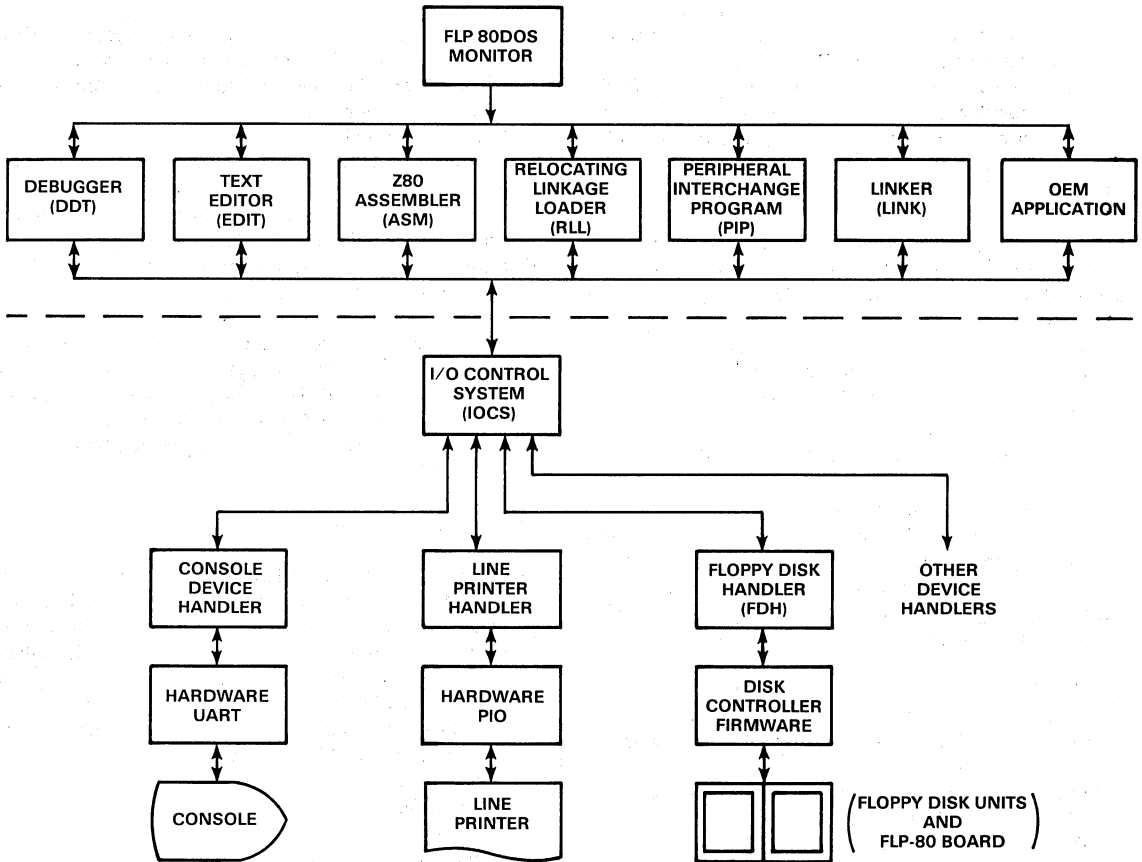
The Floppy Disk Handler (FDH) interfaces from the IOCS to a firmware controller for up to four floppy disk units. The FDH provides a sophisticated command structure to handle advanced OEM products. The firmware controller interfaces to Mostek's FLP-80E Controller Board. The disk format is IBM 3740 soft sector. The software can be easily adapted to double-sided and double-density disks. The Floppy Disk Handler commands include:

- erase file
- create file
- open file
- close file
- rename file
- rewind file
- read next n sectors
- reread current sector
- read previous sector
- skip forward n sectors
- skip backward n sectors
- replace (rewrite) current sector
- delete n sectors

The FDH has advanced error recovery capability. It supports a bad sector map and an extensive directory which allows multiple users. The file structure is doubly-linked to increase data integrity on the disk, and a bad file can be recovered from either its start or end.

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FLP-80 DOS BLOCK DIAGRAM



ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
FLP-80DOS	SDE based development system software (SD PROMs)	MK78142
FLP-80DOS	MD based development system software (MD PROMs)	MK77962
	FLP-80DOS Operations Manual Only	MK78557

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SOFTWARE DISK BASED

MITE-80/BIOS

MK77972

FEATURES

- Multi-tasking executive
- Debugger which recognizes task data structures
- Macro files to facilitate building tasks
- Memory-pool manager
- Timer handler which simulates any number of timers using one hardware timer
- I/O drivers for line printer, terminal, and floppy disk
- Basic I/O service subroutines to facilitate building new I/O drivers
- Error-handler task which provides standard system error recovery

INTRODUCTION

The Mostek MITE-80 software package is designed for applications requiring asynchronous event handling of multiple tasks. MITE-80 provides the basic services for managing the CPU's resources in a real-time, multi-task environment. MITE-80 is a software package provided on diskette and includes:

- MITE-80
- MITE-80 Debug
- MITE-80 MACROS
- MITE-80 System Linkages
- MITE-80 Timer Handler
- MITE-80 Memory-Pool Manager

These programs provide the capability for controlling real-time, multiple-task applications as well as providing a way of developing and debugging real-time programs. The programs can be developed using a Mostek FLP-80DOS software package that includes a MACRO-80 Assembler.

MITE-80/BIOS is the Mostek Basic Input/Output Services software package. It provides a common set of routines to facilitate the design of I/O drivers and includes the I/O drivers for terminal, printer, and floppy disk. All of the MITE-80/BIOS modules are designed to operate under MITE-80. The MITE-80/BIOS package supplements MITE-80 in that

the routines and drivers provided are designed for real-time multiple asynchronous applications. The MITE-80/BIOS package is provided on diskette and includes:

- MITE-80/BIOS Terminal Driver
- MITE-80/BIOS Printer Driver
- MITE-80/BIOS Floppy-Disk Driver
- MITE-80/BIOS Basic I/O Service Routines
- MITE-80/BIOS MACRO Files
- MITE-80/BIOS Equate Files
- MITE-80/BIOS Error-HandlerTask

MITE-80

MITE-80 provides a user with centralized control of the Z80 CPU's resources. In managing this control, MITE-80 uses two data structures, a Task Control Block (TCB), and a Message Block (MB), as well as several system services that are callable from user programs.

TASK CONTROL BLOCK (TCB)

A TCB uniquely identifies a task within the system. Each TCB is a minimum 10 bytes in length and contains the task status, task priority, system link, message pointer, stack pointer, and task name. Each task is also required to provide a minimum of 16 bytes of stack area for MITE-80 usage. The number of tasks that MITE-80 can accommodate is limited only by the amount of user-allocated TCB memory. The determination of which task executes, and when, is accomplished by a status byte and a priority level. A task can be assigned any one of 127 priority levels and any number of tasks can share the same priority level.

MESSAGE BLOCK (MB)

An MB is used to transfer information between tasks. Each MB is a minimum eight bytes in length and contains status, message priority, system link, receiver pointer, and sender pointer. An optional data field can follow the MB; its contents and length are defined by user application. MBs can be sent with a queuing option of FIFO or LIFO and with the option of either specified priority or task priority. The order in which a task processes MBs is determined by the MB's priority level. Any one of 127 priority levels can be selected.

SERVICES

The MITE-80 services provided allow for the handling of

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messages between tasks and for task creation and cancelling. Additional services allow for the control of interrupt events and CPU interrupts.

The Services provided are:

- M8SN - Send a message to a task
- M8SNW - Send a message to a task and wait for a message to be available.
- M8RSN - Resend a message to a task.
- M8RSNW - Resend a message to a task and wait for a message to be available.
- M8RCV - Receive a message if one is available.
- M8RCVW - Receive a message, otherwise wait until one is available.
- M8FWD - Forward a message to a task.
- M8FWDW - Forward a message to a task and wait for a message to be available.
- M8RET - Return a message to the sending task.
- M8RETW - Return a message to the sending task and wait until a message is available.
- M8CAN - Cancel a message sent to a task.
- M8FIND - Find the TCB address of a specified task name.
- M8WINT - Wait for an interrupt event to be posted.
- M8PINT - Post an interrupt event which is completed.

MITE-80 DEBUG

The MITE-80 DEBUG program provides a facility for interactively debugging relative and absolute Z80 programs executing under MITE-80. The various commands allow displaying and modifying memory and CPU registers, setting breakpoints, and executing programs. Additional commands allow for breakpoints on tasks and services, for service history, and for displaying Task Control Block and Message Block contents. Mnemonics are used to represent Z80 registers and MITE-80 services, thus simplifying the command language.

The commands provided are:

- B - Insert a breakpoint in the user's program.
- C - Copy the contents of a block of memory to another location in memory.
- D - Display the past history of Tasks executed along with the MITE-80 services used.
- E - Execute program.
- F - Fill memory limits with an 8-bit data pattern.
- H - Perform 16-bit hexadecimal addition and/or subtraction.
- J - Snap-shot a Task Control Block and its queued Message Blocks.
- K - Breakpoint on a Task calling MITE-80.
- L - Locate all occurrences of an 8-or 16-bit data pattern.
- M - Display, update, or tabulate the contents of memory.
- O - Set the offset constant.
- P - Display or update the contents of an I/O port.
- Q - Quit MITE-80 DEBUG.
- R - Display the contents of the user registers.
- V - Verify that two blocks of memory are equal.
- W - Software single step.
- X - Duplicate console output to printer device.

MITE-80 SYSTEM LINKAGES

A system linkage file is provided which contains linkage addresses for the system routines. The user can link unique application programs to the MITE-80 services with this file. This file will minimize any impact on user programs whenever MITE-80 is enhanced.

MITE-80 TIMER HANDLER

A Timer Handler is provided for control over an MK3882 Counter Timer Circuit (CTC) chip. The timer can be used for applications requiring event time delays or for event watchdog alerts. The timer executes as a MITE-80 task. A maximum time duration of approximately 14 minutes in increments of 12.8 milliseconds is provided.

MITE-80 MEMORY-POOL MANAGER

A Memory-Pool Manager provides the user with a way of allocating and deallocating memory blocks. The user can configure an area of memory in up to 253 memory pools, with each pool consisting of a unique memory-block size. A macro is provided in the MITE-80 MACRO FILE to aid the user in configuring the pools.

MITE-80 MACROS

A macro file is provided to aid the user in defining and developing MITE-80 TCBs. The macros will construct and integrity-check a TCB from user-specified parameters. The macros will also generate code which will install the TCB into the MITE-80 system.

MITE-80/BIOS TERMINAL DRIVER

The Terminal Driver provides asynchronous input and output interface between user tasks operating under MITE-80 and an operator's terminal interfaced to an MDX-EPROM/UART Card. The Driver operates as a task under MITE-80 and can accommodate multiple terminal devices. Various parameters are user-configurable to allow the specifying of unique characteristics for each terminal.

MITE-80/BIOS PRINTER DRIVER

The Printer Driver provides output control between user tasks operating under MITE-80 and a printer interfaced to a Mostek MDX-PIO Card. The Driver operates as a task under MITE-80 and can accommodate multiple printer devices. Various Driver parameters are user-configurable to allow the specifying of unique characteristics for each printer.

MITE-80/BIOS FLOPPY-DISK DRIVER

The Floppy-Disk Driver provides input and output control between user tasks operating under MITE-80 and a floppy-disk drive interfaced to an MDX-FLP Card. The Driver operates as a task under MITE-80 and can accommodate multiple disk drives. The Driver can handle the standard

eight-inch and the mini 5.25-inch disk drives. Various Driver parameters are user-configurable to allow the specifying of unique characteristics for each disk drive.

MITE-80/BIOS BASIC I/O SERVICE ROUTINES

The basic I/O routines provide a common set of I/O services which can be used to facilitate the design of user-developed drivers. The routines provide functions that all drivers need, such as user-buffer-pointer maintenance, hardware initialization and character interpretation. All of the routines are re-entrant and can be used by as many Driver tasks as required by the application. The routines work with data provided in the calling task's Task Control Block and the Message Block currently being serviced by the Driver task.

The Mostek-supplied drivers for Terminal, Printer, and Floppy Disk all use the basic I/O routines. Memory savings can be realized by using the basic I/O routines since common functions such as buffer-pointer maintenance and special-character interpretation (carriage return, line feed, tab) required by many I/O drivers are centralized in the basic I/O service routines.

MITE-80/BIOS provides seven callable routines for accessing the common services:

CALL NAME	SERVICES
--------------	----------

IO?WHY	- Common decode of request and initialization
IO?GNC	- Get next character from buffer, for output
IO?PNC	- Put next character into buffer, for input
IO?ISR	- Interrupt service handling
IO?OPN	- Open device
IO?EOB	- End-of-Block Routine
IO?ILL	- Illegal operation processor

MITE-80/BIOS MACRO FILES

A pair of I/O macro files is provided to assist in constructing the Driver's Task Control Block along with their unique device characteristics. A general-purpose I/O task macro is also included for constructing the mandatory TCB parameters on user-developed Drivers.

MITE-80/BIOS EQUATE FILES

Two equate files are provided to support MITE-80/BIOS. The file IOTASK.EQU provides default definitions for various MITE-80/BIOS macros. The file BIOS.EQU provides definitions for the MITE-80/BIOS extensions to the MITE-80 task control block (TCB) and message block (MB).

MITE-80/BIOS ERROR-HANDLER TASK

The Error-Handler task provides a common facility for I/O error recovery for all MITE-80/BIOS driver tasks.

CONFIGURATION

The various modules of MITE-80/BIOS are designed to work with specific Mostek hardware:

Terminal Driver:

MDX-EPROM/UART Card and one CTC Channel (MK3883 available on MDX-CPU Card), interfaced to a Hazeltine or equivalent terminal.

Printer Driver:

MDX-PIO Card interfaced to a Centronics type printer or equivalent.

Floppy-Disk Driver:

MDX-FLP Card interfaced to a Shugart type disk drive or equivalent.

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
MITE-80/BIOS	MITE-80/BIOS Software Package. The software is supplied on Mostek diskette as relocatable object. The software includes MITE-80, MITE-80 DEBUG, MACROS, EQUATES, BIOS Timer Handler, Terminal Driver, Floppy-Disk Driver, Printer Driver, and Memory-Pool Manager. MITE-80/BIOS Operation Manual is included. The attached Standard Software License Agreement and Registration Form must accompany the Purchase Order.	MK77972
	MITE-80 Operation Manual. Detailed description of the operation and use of the MITE-80 software package.	MK79726
	BIOS Operation Manual. Detailed description of the operation and use of the BIOS-80 software package.	MK79784

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SOFTWARE DISK BASED

ANSI BASIC Software Interpreter

MK78157

FEATURES

- Meets ANSI standard on BASIC (X3.60 - 1978)
- Direct access to CPU I/O Ports
- Ability to read or write any memory location (PEEK, POKE)
- Arrays with up to 255 dimensions
- Dynamic allocation and deallocation of arrays
- IF . . . THEN . . . ELSE and IF . . . GO TO (both if's may be nested)
- Direct (immediate) execution of statements
- Error trapping, with error messages in English
- Four variable types: Integer, string, real and double-precision real
- Long variable names significant up to 40 characters
- Full PRINT USING capabilities for formatted output
- Extensive program editing facilities
- Trace facilities
- Can call any number of assembly-language subroutines
- Boolean (logical) operations
- Supports up to six sequential and random access files on floppy disk
- Variable record length in random access files from one to 128 bytes/record
- Complete set of file manipulation statements
- Occupies only 23K bytes, not including operating system
- Supports console and line printer I/O
- Allows console output to be redirected to the line printer
- WHILE . . . WEND structured construct
- Programs can be saved on disk in a protected format that cannot be listed on console

DESCRIPTION

Mostek ANSI BASIC is an extensive implementation of Microsoft BASIC for the Z80 microprocessor. Its features are comparable to the BASICs found on minicomputers and large mainframes. Mostek ANSI BASIC is among the fastest microprocessor BASICs available. Designed to operate on Mostek Systems with FLP-80DOS V2.1 and with 48K bytes or more memory, Mostek BASIC provides a sophisticated software development tool.

Mostek ANSI BASIC is implemented as an interpreter and is highly suitable for user-interactive processing. Programs and data are stored in a compressed internal format to maximize memory utilization. In a 64K system, 28K of user's program and data storage area are available.

Unique features include long variable names, substring assignments and hexadecimal and octal constants. Many other features ease the task of programming complex functions. The Programmer is seldom limited by array size (up to 255 dimensions, with run-time allocation and deallocation) or I/O restrictions. Full PRINT USING capabilities allow formatted output, while both input and output may be performed with multiple sequential and random files on floppy disk as well as with the CPU I/O ports. Editing, error trapping, and trace facilities greatly simplify program debugging.

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Commands:

AUTO	CLEAR	CONT	DELETE	EDIT
FILES	LIST	LLIST	LOAD	MERGE
NEW	NULL	RENUM	RESET	RUN
SAVE	SYSTEM	TRON	TROFF	WIDTH

Program Statements:

CALL	CHAIN	COMMON	DEF DBL	DEF FN
DEFINT	DEFSNG	DEFSTR	DEFUSR	DIM
END	ERASE	ERROR	FOR . . . NEXT	GOSUB . . . RETURN
GOTO	IF . . . THEN(ELSE)	IF . . . GOTO	LET	ON ERROR GOTO
ON . . . GOSUB	ON . . . GOTO	OPTION BASE	RANDOMIZE	
REM	RESUME	STOP	SWAP	
WHILE . . . WEND				

Input/Output Statements:

CLOSE	DATA	FIELD	GET	INPUT
INPUT#	KILL	LINE INPUT	LINE INPUT#	LPRINT
LPRINT USING	LSET	NAME	OPEN	OUT
PRINT	PRINT USING	PRINT#	PRINT# USING WRITE	PUT
READ	RESTORE	RESET	RSET	WRITE#

Operators:

=	-	+	*	/
^	\	>	<	<=
>=	◇	MOD	NOT	AND
OR	XOR	IMP	EQU	

Arithmetic Functions:

ABS	ATN	CDBL	CINT	COS	CSNG
EXP	ERR	ERL	FIX	FRE	INT
LOG	RND	SGN	SIN	SQR	TAN
USR	VARPTR				

String Functions:

ASC	CHR\$	HEX\$	INSTR	LEFT	LEN
MID\$	OCT	RIGHT\$	SPACE\$	SPC\$	STR\$
STRINGS	VAL				

Input/Output Functions:

CVI	CVS	CVD	DSKF	EOF	INP
INPUT\$	LOC	LOF	LOG	LPOS	MKD\$
MKI\$	MKS\$	PEEK	POKE	POS	TAB
WAIT					

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
Mostek ANSI BASIC	BASIC INTERPRETER high-level language to run on FLP-80DOS. Requires 48K or more bytes of memory.	MK78157
	BASIC Operation Manual Only	MK79708

In order to receive Mostek ANSI BASIC, the Mostek BASIC non-disclosure agreement must be signed and returned with each purchase order.

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SOFTWARE DISK BASED

FORTRAN IV Compiler

MK78158

FEATURES

- All of ANSI standard FORTRAN IV (X3.9-1966) except complex data type
- Generates relocatable linkable object code
- Subroutines may be compiled separately and stored in a system library
- Compiles several hundred statements per minute in a single pass
- Enhancements include
 1. LOGICAL variables which can be used as integer quantities
 2. LOGICAL DO loops for tighter, faster execution of small-valued integer loops
 3. Mixed-mode arithmetic
 4. Hexadecimal constants
 5. Literals and Holleriths allowed in expressions
 6. Logical operations on integer data. .AND., .OR., .NOT. and .XOR. can be used for 16-bit or 8-bit Boolean operations
 7. READ/WRITE End-of-File or Error Condition transfer. END=n and ERR=n (where n is the statement number) can be included in READ or WRITE statements to transfer control to the specified statement on detection of an error or end-of-file condition
 8. ENCODE/DECODE for FORMAT operations to memory
- Long descriptive error messages
- Extended optimizations
- Z80-assembly-language subprograms may be called from FORTRAN programs

DESCRIPTION

Mostek's FORTRAN IV Compiler package provides new capabilities for users of Z80-based microcomputer systems. Mostek FORTRAN is comparable to FORTRAN compilers on large mainframes and minicomputers. All of ANSI Standard FORTRAN X3.9-1966 is included except the COMPLEX data type. Therefore, users may take advantage of the many applications programs already written in FORTRAN.

FORTRAN IV COMPILER PHOTO



Mostek FORTRAN IV is unique in that it provides a microprocessor FORTRAN development package that generates relocatable object modules. This means that only the subroutines and system routines required to run FORTRAN programs are loaded before execution. Subroutines can be placed in a system library so that users can develop a common set of subroutines that are used in their programs. Also, if only one module of a program is changed, it is necessary to re-compile only that module.

The standard library of subroutines supplied with FORTRAN includes:

ABS	IABS	DABS	AINT
INT	IDINT	AMOD	MOD
AMAX0	AMAX1	MAX0	MAX1
DMAX1	AMINO	AMIN1	MINO
MIN1	DMIN1	FLOAT	IFX
SIGN	ISIGN	DSIGN	DIM
IDIM	SNGL	DBLE	EXP
DEXP	ALOG	DLOG	ALOG10
DLOG10	SIN	DSIN	COS
DCOS	TANH	SQRT	DSQRT
ATAN	DATAN	ATAN2	DATAN2
DMOD	PEEK	POKE	INP
OUT			

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The library also contains routines for 32-bit and 64-bit floating point addition, subtraction, multiplication, division, etc. These routines are among the fastest available for performing these functions on the Z80.

A minimum system size of 48K bytes (including FLP-80DOS) is required to provide efficient optimization. The Mostek FORTRAN compiler optimizes the generated object code in several ways:

1. Common subexpression elimination. Common sub-expressions are evaluated once, and the value is substituted in later occurrences of the subexpression.
2. Peephole Optimization. Small sections of code are replaced by more-compact, faster code in special cases.
3. Constant folding. Integer constant expressions are evaluated at compile time.
4. Branch Optimizations. The number of conditional jumps in arithmetic and logical IFs is minimized.

Long descriptive error messages are another feature of the compiler. For instance:

?Statement unrecognizable

is printed if the compiler scans a statement that is not an assignment or other FORTRAN statement. The last twenty characters scanned before the detected error are also printed.

As an option, the compiler generates a fully symbolic listing of the machine language to be generated. At the end of the listing, the compiler produces an error summary and tables

showing the addresses assigned to labels, variables and constants.

LINKER

A relocating linking loader (LINK-80) and a library manager (LIB-80) are included in the Mostek FORTRAN package.

LINK-80 resolves internal and external references between the object modules loaded and also performs library searches for system subroutines and generates a load map of memory showing the locations of the main program, subroutines and common areas.

LIBRARY MANAGER

LIB-80 allows users to customize libraries of object modules. LIB-80 can be used to insert, replace or delete object modules within a library, or create a new library from scratch. Library modules and the symbol definitions they contain may also be listed.

XCPM UTILITY

A utility program (XCPM) is included which allows the user to copy FORTRAN source programs from CP/M diskettes to FLP-80DOS diskettes. At this point the programs can be compiled using the Mostek FORTRAN compiler.

FTRANS UTILITY

FTRANS allows the user to convert object programs produced by the Mostek Z80 assembler to a form that is linkable to FORTRAN programs.

DESIGNATOR	DESCRIPTION	PART NO.
Mostek FORTRAN IV	FORTRAN IV high-level compiler to run on FLP-80DOS. Requires 48K bytes of RAM. Includes Operations Manual.	MK78158
	Mostek FORTRAN IV Operations Manual only	MK79643

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SOFTWARE DISK BASED

MACRO-70

MK79085

FEATURES

- Assembles standard 3870/F8 instruction set to produce relocatable, linkable object modules.
- Provides nested conditional assembly, an extensive expression evaluation capability, and an extended set of assembler pseudo-ops:

ORG	- origin
EQU	- equate
DC	- define constant
DEFL	- set/define macro label
DEFM	- define message
DEFB	- define byte
DEFW	- define word
DEFS	- define storage
END	- end of program
GLOBAL	- global symbol definition
NAME	- module name definition
PSECT	- program section definition
IF/ENDIF	- conditional assembly
INCLUDE	- include another file in source module
LIST/NLIST	- list on/off
CLIST	- code listing only of macro expansions
ELIST	- list/no list of macro expansions
EJECT	- eject a page of listing
TITLE	- place title on listing

- Provides options for obtaining a printed cross-reference listing, terminating after pass one if errors are encountered, redefining standard MK3870 opcodes via macros, and obtaining an unused-symbol reference table.
- Provides the most advanced macro handling capability on the microcomputer market which includes:
 - optional arguments
 - default arguments
 - looping capability
 - global/local macro labels
 - nested/recursive expansions
 - integer/boolean variables
 - string manipulation
 - conditional expansion based on symbol definition
 - call-by-value facility
 - expansion of code-producing statements only
 - expansion of macro-call statements only

- An extended instruction set for the MK3870 is defined via a macro definition file and is shipped with the MACRO-70 diskette.
- Listing and object modules can be output on disk files or any device.
- Compatible with other Mostek 3870/F8 assemblers and FLP-80DOS Version 2.0 or higher. Requires 32K or more of system RAM.

DESCRIPTION

MACRO-70 is an advanced upgrade from the 3870/F8 Cross Assembler (FZCASM). In addition to its macro capabilities, it provides for nested conditional assembly and allows symbol lengths of any number of characters. It supports global symbols, relocatable programs, a symbol cross-reference listing, and an unused-symbol reference table. MACRO-70 is upward compatible with all other Mostek 3870/F8 Assemblers.

The Mostek 3870/F8 Macro Assembler (MACRO-70) is designed to run on the Mostek Dual-Disk Development System with 32K or more of RAM. It requires FLP-80DOS, Version 2.0 or higher. Macro pseudo-ops include the following:

MACRO/MEND	- define a macro
MNEXT	- step to next argument
MIF	- evaluate expression and branch to local macro label if true
MGOTO	- branch to local macro label
MEXIT	- terminate macro expansion
MERROR	- print error message in listing
MLOCAL	- define local macro label

Predefined macro-related parameters include the following:

%NEXP	- current number of this expansion
%NARC	- number of arguments passed to expansion
#PRM	- expand last-used argument
%NPRM	- number of last-used argument
%NCHAR	- number of characters in argument

The operations manual describes in detail all facilities available in MACRO-70 and provides a host of examples

and sample print-outs. An extended instruction set which is designed to ease programming for the MK3870 is defined in the manual. The new instructions are provided on the MACRO-70 diskette in the form of a macro definition file

which can be included in a source program. Downloading to other Mostek systems is facilitated by a utility program called F8DUMP, which is supplied on the MACRO-70 diskette.

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
MACRO-70	3870/F8 Macro Cross Assembler, binary program supplied on a standard FLP-80DOS diskette. Includes F8DUMP utility, an extended instruction set, macro definition file, and the Operations Manual.	MK79085
	MACRO-70 Operations Manual	MK79635

MOSTEK®

SOFTWARE DISK BASED

MACRO-80

MK78165

FEATURES

- Assembles standard Z80 instruction set to produce relocatable, linkable, object modules
- Provides nested conditional assembly, an extensive expression evaluation capability, and an extended set of assembler pseudo-ops:

ORG	- origin
EQU	- equate
DEFL	- set/define macro label
DEFM	- define message
DEFB	- define byte
DEFW	- define word
DEFS	- define storage
END	- end of program
GLOBAL	- global symbol definition
NAME	- module name definition
PSECT	- program section definition
IF/ENDIF	- conditional assembly
INCLUDE	- include another file in source module
LIST/NLIST	- list on/off
CLIST	- code listing only of macro expansions
ELIST	- list/no list of macro expansions
EJECT	- eject a page of listing
TITLE	- place title on listing

- Provides options for obtaining a printed cross-reference listing, terminating after pass one if errors are encountered, redefining standard Z80 opcodes via macros, and obtaining an unused-symbol reference table.
- Provides the most advanced macro handling capability in the microcomputer market which includes:
 - optional arguments
 - default arguments
 - looping capability
 - global/local macro labels
 - nested/recursive expansions
 - integer/boolean variables
 - string manipulation
 - conditional expansion based on symbol definition
 - call-by-value facility
 - expansion of code-producing statements only
 - expansion of macro-call statement only

- Listing and object modules can be output on disk files or any device.
- Compatible with other Mostek Z80 assemblers and FLP-80DOS Version 2.0 or higher. Requires 32K or more of system RAM.

DESCRIPTION

MACRO-80 is an advanced upgrade from the FLP-80DOS Assembler (ASM). In addition to its macro capabilities, it provides for nested conditional assembly and allows symbol lengths of any number of characters. It supports global symbols, relocatable programs, a symbol cross-reference listing, and an unused-symbol reference table. MACRO-80 is upward compatible with all other Mostek Z80 assemblers.

The Mostek Z80 Macro Assembler (MACRO-80) is designed to run on the Mostek Dual-Disk Development System with 32K or more of RAM. It requires FLP-80DOS, Version 2.0 or higher. Macro pseudo-ops include the following:

MACRO/MEND	- define a macro
MNEXT	- step to next argument
MIF	- evaluate expression and branch to local macro label if true
MGOTO	- branch to local macro label
MEXIT	- terminate macro expansion
MERROR	- print error message in listing
MLOCAL	- define local macro label

Predefined macro-related parameters include the following:

%NEXP	- current number of this expansion
%NARC	- number of arguments passed to expansion
#PRM	- expand last-used argument
%NPRM	- number of last-used argument
%NCHAR	- number of characters in argument

The operations manual describes in detail all facilities available in MACRO-80 and provides a host of examples and sample print-outs.

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
MACRO-80	Z80 Macro Assembler, binary program supplied on a standard FLP-80DOS diskette, with Operations Manual.	MK78165
	MACRO-80 Operations Manual	MK79635

MOSTEK®

SOFTWARE DISK BASED

MEDEX-80

MK77968

FEATURES

- Modular MDX board-level software
- User-expandable diagnostic software
- Stand-alone or integrated diagnostic package execution
- Interrupt-or non-interrupt-driven diagnostics
- Board-level diagnostics for:

CPU	SC/D	A/D 8
RAM	FLP	
ROM	MATH	

DESCRIPTION

MEDEX-80 is a diagnostic software package for the MDX series of cards. MEDEX-80 is an acronym for MDX Expandable Diagnostic Exercise software for the Z80. It is a modular software package designed to diagnose faulty MDX card(s) within a system configuration. MEDEX-80 can function as a stand-alone package or it can be integrated into a user's software package. Only those modules applicable to a user's requirements need be used.

MEDEX-80 can reside in either RAM or EPROM, and the amount of memory required is dependent on the standard modules selected and the unique user modules included in the package. This diagnostic software package is designed to operate with the following minimum hardware configuration:

- Mostek MDX-CPU card (MDX-CPU1 or CPU2)
- Mostek MDX-SC/D card

SOFTWARE DESCRIPTION

MEDEX-80 is comprised of system software and diagnostic software. The system software consists of initialization, monitor, and MDX-SC/D card handler. The diagnostics software consists of test programs for only those MDX cards having little or no on-card user configurability. For those MDX cards having extensive on-card user configur-

ability, the diagnostic programs can be supplied by the user. The expandable structure of MEDEX-80 permits the inclusion of user-developed diagnostic programs within its structure. The diagnostic software modules that are supplied in MEDEX-80, version 2.0 are as follows:

1. **MDINI** - Initialization which provides the set-up requirements of other MEDEX-80 modules.
2. **MDMON** - Monitor which provides control supervision and interface to rest of diagnostic modules.
3. **MDSCH** - MDX-SC/D card handler which provides user interface to the card's I/O devices.
4. **MDRAM** - Diagnostic RAM test which provides confidence test of RAM areas by means of pattern tests.
5. **MDROM** - Diagnostic ROM test which provides confidence test of ROM areas by means of checksums.
6. **MDCTC** - Diagnostic CTC test which provides confidence test of MDX-CPU card's CTC by means of functional exercising.
7. **MDSCD** - SC/D card test which provides confidence test of MDX-SCD card by means of functional exercising.
8. **MDFLP** - Diagnostic Floppy Disk card test which provides confidence test of MDX-FLP card by means of functional exercising.
9. **MDMTH** - Diagnostic Math Card test which provides confidence test of AM 9511 Math Chip and MDX-MATH card by means of functional testing.
10. **MDAD8** - Diagnostic A/D 8 card test which provides confidence test which provides confidence test of MDX-A/D 8 card by means of functional exercising.

A software users manual for each diagnostic module is provided on the MEDEX-80 diskette and provides indepth description of each module.

SOFTWARE
DISK BASED

THEORY OF OPERATION

The basic theory of operation of both MEDEX-80 and the MDX-SC/D Card is as follows. The user provides a CPU control transfer to the MEDEX-80 initialization module through a jump instruction or a depressed switch action. This initialization module sets up the MEDEX-80 monitor, other MDX cards that need initialization, and the MDX-SC/D card. Once initialization is complete, the monitor takes control of the diagnostic system. To perform a test, the operator selects the desired diagnostic test number via the thumbwheels on the SC/D card. The RESET/START switch is then momentarily depressed to the Start position to activate the specified test number. The monitor validates the test number and transfers CPU control to the proper diagnostic test program. The display will indicate a "test in progress" readout. If the test is permitted to execute until completion of the selected diagnostic test, then, upon completion, the test results will be indicated in the display. The display indication of pass or fail, and type of fail, is dependent on the diagnostic test program. A different or same diagnostic test can now be executed following the cycle as just described. If the operator desires to terminate a diagnostic test in progress, or to reinitialize the diagnostic system, the RESET/START switch is momentarily depressed to the RESET position. The depression to the RESET position will cause the MEDEX-80 initialization module to again be executed, or cause execution of the users initialization (0000H) routine if the Reset Switch is strapped to PBRESET.

INTERRUPTS

MEDEX-80 utilizes the mode 2 interrupts of the Z80. Each diagnostic module's initialization process will load its respective interrupt vector(s) on its respective MDX card. MEDEX-80 will initialize the CPU's I register during its initialization. Whenever an interrupt occurs, the MDX Card's interrupt vector is linked with the I register, forming an address which points to the respective entry address of the Diagnostic Interrupt Vector Table. An indirect branch to the address within this entry is then performed by the CPU and process control is transferred to the specified interrupt service routine.

The handling of an interrupt from an MDX card is the responsibility of the respective card's diagnostic module. If a user elects not to involve interrupts within the diagnostic module test, then, during the diagnostic module's initialization, the user should configure the MDX card's

interrupt control word to disable interrupts. During the MEDEX-80 initialization phase, the Z80 system-wide interrupt capability is disabled. MEDEX-80 will enable system-wide interrupt capability after all diagnostic modules have completed their unique initialization. During each diagnostic module's initialization, the user should disable the unique MDX card's interrupt. When the diagnostic module is selected to execute, the first operation should be to enable its respective MDX card's interrupt capability, and upon completion of the test, the card's interrupt capability should be disabled.

CONCEPT OF DIAGNOSTIC MODULE

The diagnostic module is a program which executes a specific test or tests, and, upon completion, outputs the test results to the operator display in the form of a coded number.

Each diagnostic module is composed of the following programs, or submodules:

1. **Initialization** - Provides the unique initialization requirements.
2. **Test** - Provides the unique test(s) to exercise and determine specific faults, determines the pass/fail decision on the performed test, and provides coded operator display.
3. **ISR** - Provides the unique interrupt service routine handling if applicable to this diagnostic module.

MEDEX-80 DISKETTE

A floppy diskette formatted in the IBM 3740 soft-sectored single-density fashion is provided with the SC/D Card. The diskette is readable on a FLP-80DOS-based MDX or MATRIX system. The diskette includes the following:

1. **Modules** - An assembly source-code file of each of the MEDEX-80 modules.
2. **User Manuals** - A software user manual for each of the above source modules. The user manual files are in ASCII text format for output to a printer. Each user manual has a unique section number which permits, once all sections are printed, the assembling into one MEDEX-80 User Manual.

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NUMBER
MEDEX-80	MEDEX-80 diskette with 10 diagnostic software modules and a user manual (in ASCII test format) for each of the modules.	MK77968
	MEDEX-80 Users Manual Only	MK79873

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Mostek Corporation
1215 W. Crosby Road
P.O. Box 169
Carrollton, Texas 75006

***NOTE:** Mostek will not ship this software product to customer until this signed form is received by the Mostek software librarian.

FEATURES

- Includes 23 useful subroutines and programs for the Z80, including:
 - Lawrence Livermore Lab's Basic
 - Generalized sort program for up to eight fields per record
 - 8080 - Z80 source-code converter
 - Fast disk-to-disk copy utility
 - Hexadecimal Dump Utility to dump memory on files
 - Assembly Language Formatter Utility to format Z80 source into columns
 - Word Processor Program Version 2.0, used to format documents
 - Disk Recovery Utility used to recover bad disk files
- All programs are supplied in source, object, and binary format with complete documentation on a standard FLP-80DOS diskette
- Requires FLP-80DOS Version 2.0 or higher

DESCRIPTION

The Mostek FLP-80DOS Software Library is a collection of

programs of general utility that run under FLP-80DOS Version 2.0 or higher. These programs are used quite extensively at Mostek. They are being offered in source format on diskette so that the user may not only use them as supplied, but may use them as a base for individually-tailored software.

This software library differs from other libraries in that all programs in the library have been developed or modified in-house. All programs in the library are in use at Mostek and all have some utility.

The FLP-80DOS Software Library Volume 1 consists of a User's Guide and two diskettes containing the source and binary (or object for subroutines) forms for each one of the twenty-three included programs. In order to reduce the cost of the library, printed source listing are not supplied. The user can obtain a source listing easily by assembling the required source program. A brief User's Guide is a part of each program source.

The FLP-80DOS Software Library is a "Level 2" product. "Level 2" software products are supplied by Mostek but are not supported in the areas of technical assistance or updates.

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
LIB-80 Volume 1	Software Library including source, object, and binary formats on diskette, and a printed user's guide.	MK78164
	Software Library Operation Manual Only	MK79621

MICRO SYSTEMS DATA BOOK

I	Table of Contents
II	General Information
III	STD-Z80 BUS
IV	MDX Series Data Processing
V	MD Series Input/Output
VI	MD Series Memory
VII	MD Series Special Functions
VIII	MD Series Accessories
IX	MD Series Data Processing
X	SDE Series Data Processing
XI	SDE Series Input/Output
XII	SDE Series Memory
XIII	SDE Series Accessories
XIV	Software Disk Based
XV	Development Systems
XVI	Systems Emulation Boards
XVII	Peripherals

MOSTEK®

DEVELOPMENT SYSTEMS

MATRIX™-80/SDS

MK78188, MK78189

INTRODUCTION

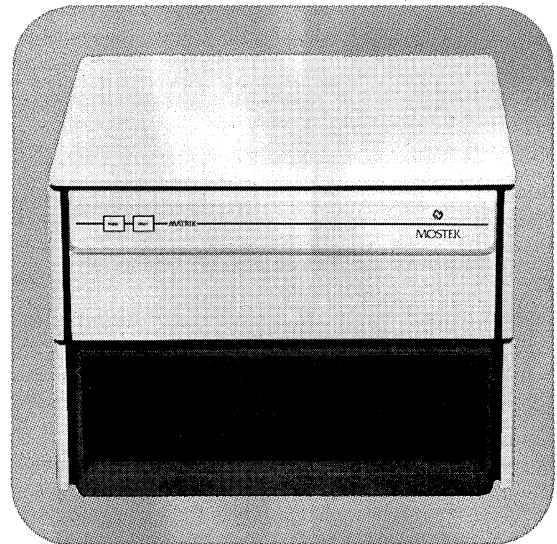
The Mostek MATRIX™ is a complete state-of-the-art, floppy disk-based computer. Not only does it provide all the necessary tools for software development, but it provides complete hardware/software debug through Mostek's AIM™ series of in-circuit emulation cards for the Z80, 8086, and 8088 as well as the 3870 family of single-chip microcomputers. The MATRIX has at its heart the powerful OEM-80E (Single Board Computer), the RAM-80BE (RAM I/O add-on board), and the FLP-80E (floppy disk controller board). Because these boards and software are available separately to OEM users, the MATRIX serves as an excellent test bed for developing systems applications.

The disk-based system eliminates the need for other mass storage media and provides ease of interface to any peripheral normally used with computers. The file-based structure for storage and retrieval consolidates the data base and provides a reliable portable media to speed and facilitate software development.

The FLP-80DOS Disk Operating System is designed for maximum flexibility both in use and expansion to meet a multitude of end-user or OEM needs. FLP-80DOS is compatible with Mostek's SD and MD Series of OEM boards, allowing software designed on the MATRIX to be directly used in OEM board applications.

Development System Features

The MATRIX is an excellent integration of both hardware and software development tools for use throughout the complete system design and development phase. The software development is begun by using the combination of Mostek's Text Editor with "roll in-roll out" virtual memory operation and the Mostek relocating assembler. Debug can then proceed inside the MATRIX domain using its resources as if they were in the final system. Using combinations of the Monitor, Designer's Debugging Tool, execution time breakpoints, and single step/ multistep operation along with a formatted memory dump, provides control for attacking those tough problems. The use of the Mostek AIM™ options provides extended debug with versatile hardware breakpoints on memory or port locations, a buffered in-circuit emulation cable for extending the



software debug into its own natural hardware environment, and a history memory to capture bus transactions in real time for later examination.

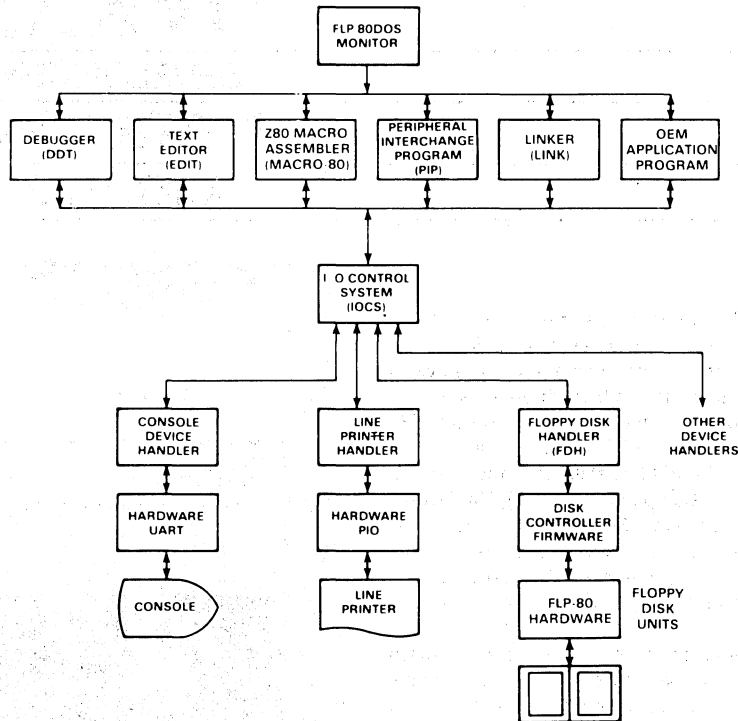
The relocatable and linking feature of the assembler enables the use of contemporary modular design techniques whereby major system alterations can be made in small tractable modules. Using the Linker, the small modules can be combined to form a run-time module without major reassembly of the entire program.

Package System Features

From a system standpoint, the MATRIX has been designed to be the basis of an end product such as a small business/industrial computer. The flexibility provided in the FLP-80DOS operating system permits application programs to be as diverse as a high-level language compiler or a supervisory control system in the industrial environment. Other hardware options are available, with even more to be added. Expansion of the disk drive units to a total of four single-sided or double-sided units provides up to two megabytes of storage. This computer uses the third-generation Z80 processor supported with the power of a



FLP-80DOS BLOCK DIAGRAM



complete family of peripheral chips. Through the use of its 158 instructions, including 16-bit arithmetic, bit manipulation, advanced block moves and interrupt handling, almost any application from communication concentrators to general purpose accounting systems is made easy.

OEM Features

The hardware and software basis for the MATRIX is also available separately to the OEM purchaser. Through a software licensing agreement, all Mostek software can be utilized on these OEM series of cards.

MATRIX SYSTEM SPECIFICATIONS

- Z80 CPU
- 4K-byte PROM bootstrap and Z80 debugger
- 60K bytes user RAM (56K contiguous)
- 4K bytes PROM bootstrap
- Eight 8-bit I/O ports using four PIOs with user-definable drivers/receivers
- Serial port: RS-232C and 20 mA current loop
- 4 channel counter/timer (CTC)
- Two single-density, single-sided disk drives; 250K bytes per floppy disk
- Three positions for AIM modules, A/D cards, Serial Interface, etc.

- Device drivers for paper tape readers, punches, card readers, line printers, Silent 700's, Teletypes and CRT's are included. Others can be added.
- PROM programmer I/O port. Programmer itself is optional.
- Bus compatible with Mostek SDE series of OEM boards

MATRIX RESIDENT SOFTWARE (FLP-80DOS)

A totally integrated package of resident software is offered in conjunction with the MATRIX consisting of:

Monitor
 Text Editor
 MACRO 80 Assembler
 Linker
 DDT-80 with extended debug through AIM™ modules
 Peripheral Interchange Program
 Floppy Disk Handler
 I/O Control System
 Device Driver Library
 Batch Mode Operation

Monitor

The FLP-80DOS Monitor is the environment from which all activity in the system initiates. From the Monitor, any system routine such as PIP or a user-generated program is

begun by simply entering the program name. FLP-80DOS I/O is done in terms of logical unit numbers, as is commonly done in FORTRAN. A set of logical units is pre-assigned to default I/O drivers upon power up or reset. From the console the user can reassign any logical unit to any new I/O device and can also display logical unit assignments. Executable file creation can be done by the Save command; printable absolute object files can be produced using the Dump command.

Text Editor

The Text Editor permits editing/creating of any source file independent of the language being written. The Editor is both line and string oriented to give maximum utility and user flexibility. The Editor, through its virtual memory "roll in-roll out" technique, can edit a file whose length is limited only by maximum diskette storage. Included in the repertoire of #15 commands are macro commands to save time when encountering a redundant editing task. The Editor is also capable of performing in one operation all the commands which will fit into an 80-column command buffer.

The video Editor displays the text to be edited directly on the CRT screen as if it were a window into memory.

The window and cursor need only be positioned over the character to be changed. Then the new text can be added or the old deleted with the changed data displayed immediately on the screen. The video Editor allows programs (or any text) to be entered or corrected much more quickly and easily than TTY-oriented Editors allow.

Z80 Macro Assembler (MACRO-80)

The Mostek Z80 Macro Assembler (MACRO-80) is the most powerful macro assembler in the microcomputer market. In addition to its macro capabilities, it provides for nested conditional assembly and allows symbol lengths of any number of characters. It supports global symbols and relocatable programs. Features of MACRO-80 include the following:

- Assembles standard Z80 instruction set to produce relocatable, linkable, object modules.
- Provides nested conditional assembly, an extensive expression evaluation capability, and an extended set of assembler pseudo-ops:

ORG	- orgin
EQU	- equate
DEFL	- set/define macro label
DEFM	- define message
DEFB	- define byte
DEFW	- define word

DEFS	- define storage
END	- end of program
GLOBAL	- global symbol definition
NAME	- module name definition
PSECT	- program section definition
IF/ENDIF	- conditional assembly
INCLUDE	- include another file in source module
LIST/NLIST	- list on/off
CLIST	- code listing only of macro expansions
ELIST	- list/no list of macro expansions
EJECT	- eject a page of listing
TITLE	- place title on listing

Provides options for obtaining a printed cross-reference listing, terminating after pass one if errors are encountered, redefining standard Z80 opcodes via macros, and obtaining an unused symbol reference table.

- Listing and object modules can be output on disk files or any device.
- Compatible with other Mostek Z80 assemblers and FLP-80DOS Version 2.0 higher.
- Provides the most advanced macro handling capability in the microcomputer market which includes:
 - optional arguments
 - default arguments looping capability
 - global/local macro labels
 - nested/recursive expansions
 - integer/boolean variables
 - string manipulation
 - conditional expansion based on symbol definition
 - call by value facility
 - expansion of code-producing statements only
 - expansion of macro call statement only

Macro pseudo-ops include the following:

MACRO/	
MEND	- define a macro
MNEXT	- step to next argument
MIF	- evaluate expression and branch to local macro label if true
MGOTO	- branch to local macro label
MEXIT	- terminate macro expansion
MERROR	- print error message in listing
MLOCAL	- define local macro label

Predefined macro-related parameters include the following:

%NEXP	- current number of this expansion
%NARC	- number of arguments passed to expansion
#PRM	- expand last used argument
%NPRM	- number of last used argument
%NCHAR	- number of characters in argument

The operations manual describes in detail all facilities available in MACRO-80 and provides a host of examples and sample print-outs.

Linker

The Linker program provides the capability of linking assembler-generated, absolute or relocatable object modules together to create a binary or run-time file. This process permits generation of programs which may require the total memory resources of the system. The linking process includes the library search option which, if elected, will link in standard library object files (device drivers, math pack functions) from disk to resolve undefined global symbols. Another option selects a complete global symbol cross-reference listing.

Peripheral Interchange Program (PIP)

PIP provides complete file maintenance activity for operations such as copy file from disk to disk, disk to peripheral, or any peripheral to any other peripheral supporting both file-structured and character-oriented devices. Key operations such as renaming, appending, and erasing files also exist along with status commands for diskette ID and vital statistics. PIP can search the diskette directories for any file or a file of a specific name, extension, and user number. The PIP operations are:

- Append - appends file 1 to file 2 without changing file 1.
- Copy - copies input files or data from an input device to an output file or device. The Copy command can be used for a variety of purposes such as listing files, concatenating individual files, or copying all the files on a single file from one disk unit (e.g. DK0) to a second disk unit (e.g. DK1)
- Date - allows the specifying of the date in day, month, and year format. The date specified will be used to date tag any file which is created or edited.
- Directory - lists the directory of a specified disk unit (DK0, DK1, etc.). The file name, extension, user number and creation or edited date are listed for each file in the directory. The user can also request listing-only files of a specified name, only files of a specified extension, or only files of a specified user number. The list device can be any device supported by the system as well as a file.

- Erase - erases a single file or files from a diskette in a specified disk unit. The user has the option to erase all files, only files of a specified file name, or only files of a specified user number.
- Format - takes completely-unformatted soft-sectored diskettes, formats to IBM 3740, and prepares to be a system diskette. Operation is performed on diskette unit 1 and a unique 11-character name is assigned to that diskette, if specified.
- Init - initializes maps in the disk handler when a new diskette has been inserted while in the PIP environment.
- Rename - renames a file, its extension, and user number to a file of name X, extension Y, and user Z.
- Status - lists all vital statistics of a disk unit to any device. These include the number of allocated records, the number of used records, and the number of bad records
- Quit - returns to Monitor Environment.

DOS/Disk Handler

The heart of the FLP-80DOS software package is the Disk Operating System. Capable of supporting up to four single-density, single- or double-sided units, the system provides a file-structure orientation timed and optimized for rapid storage and retrieval. Program debug is enhanced by complete error reporting supplied with the DOS. Additionally, extensive error recovery and bad sector allocation insure data and file integrity. The DOS not only provides file reading and writing capability, but special pointer manipulation, record deletions, record insertions, skip records both forward and backward, as well as directory manipulation such as file creation, renaming, and erasure. The DOS is initiated by a calling vector which is a subset of the I/O control system vector or through the standard IOCS calling sequence to elect buffer allocation, blocking, and deblocking of data to a user-selectable, logical record type.

A unique dynamic allocation algorithm makes optimal use of disk storage space. Run-time (Binary) files are given first priority to large blocks of free space to eliminate overhead in operating system and overlay programs. The algorithm marks storage fragments as low priority and uses them only when the diskette is nearing maximum capacity. The DOS permits seven files to be opened for operations at any one time, thus permitting execution of complex application programs.

I/O Control System

The I/O Control System provides a central facility from which all calls to I/O can be structured. This permits a system applications program to dissolve any device dependence by utilizing the logical unit approach of large, main-frame computers. For example, a programmer may want to structure the utility to use logical unit No. 5 as the list device which normally in the system defaults to the line printer. He may, however, at run time, assign a different device for logical unit No. 5. The application program remains unchanged.

Interface by a user to IOCS is done by entering a device mnemonic in a table and observing the calling sequence format. IOCS supplies a physical buffer of desired length, handles buffer allocation, blocking, deblocking, and provides a logical record structure as specified by the user.

Batch-Mode Operation

In Batch-Mode Operation, a command file is built on disk or assigned to a peripheral input device such as a card reader. The console input normally taken from the keyboard is taken from this batch device or batch file. While operating under direction of a batch file, the console output prompts the user as normal, or the prompting can be directed to any other output device. The Batch operation is especially useful for the execution of redundant procedures not requiring constant attention of the operator.

HARDWARE DESCRIPTION

OEM-80E

The OEM-80E provides the essential CPU power of the system. While using the Z80 as the central processing unit, the OEM-80E is provided with other Z80 family peripheral chip support. Two Z80 PIO's give four completely programmable 8-bit parallel I/O ports with handshake from which the standard system peripherals are interfaced. Also on the card is the Z80-CTC counter/timer circuit which has three free flexible channels to perform critical counting and timing functions. Along with 16K of RAM, the OEM-80E provides five ROM/PROM sockets which can be utilized for 10/20K of ROM or 5/10K PROM. Four sockets contain the firmware portion of FLP-80DOS. The remaining socket can be strapped for other ROM/PROM elements.

RAM-80BE

The RAM-80BE adds additional memory with Mostek's MK4116 16K dynamic memory along with more I/O. These two fully-programmable 8-bit I/O ports with handshake

provide additional I/O expansion as system needs grow. Standard system configuration is 48K bytes for a system total of 60K bytes user RAM (56K contiguous).

FLP-80E

Integral to the MATRIX system is the floppy controller. The FLP-80E is a complete IBM 3740 single-density/double-sided controller for up to four drives. The controller has 128 bytes of FIFO buffer resulting in a completely interruptable disk system.

OPTIONAL MODULES COMPATIBLE WITH MATRIX

AIM-80E (2.5 MHz max. clock rate)

The AIM-80E module provides extended debug for the MATRIX. In Z80 development, real-time in-circuit emulation permits debug of the hardware and the software at the most intimate level. Hardware single-step/multi-step with register trace, execution intercept on memory access, port access, or external trigger provides absolute control over any system regardless of how complex it is. The "pushbutton intercept" enables the programmer to perform a controlled recovery for those extremely difficult-to-trace processor-lock-out loops. With the memory clock selectable history module, any past 256 events of data, address, or control bus operation are captured in real time and may be displayed.

The AIM-80E includes 8K bytes of ROM firmware introducing unique software including a mnemonic disassembler for inverse assembly of history module contents of single-step/multi-step operations. "In-line" code disassembled to language mnemonics provides insight into execution results as if examining an assembler-generated listing. Extra added capability is the ROM-resident self-test of OEM-80E or target RAM.

AIM-Z80AE (4.0 MHz max. clock rate)

The AIM-Z80AE is an improved version of the above module usable at Z80-CPU clock rates of up to 4MHz. The AIM-Z80AE is a two-processor solution to in-circuit emulation which utilizes a Z80-CPU in the buffer box for accurate emulation at high clock rates with minimum restrictions on the target system. The AIM-Z80AE provides real-time emulation (no WAIT states) while providing full access to RESET, NMI and INT control lines. Eight single-byte software breakpoints (in RAM) are provided as well as one hardware trap (RAM or ROM). The emulation RAM on the AIM-Z80A is mappable into the target system in 256-byte



increments. A 1024 word x 48-bit history memory is triggerable by the hardware intercept and can be read back to the terminal to provide a formatted display of the Z80-CPU address, data, and control busses during the execution of the program under test. Several trigger options are available to condition the loading of the history memory.

A/D-80E

A family of 12-bit A/D and D/A modules for the MATRIX system. Options include single-ended or differential inputs up to 64 channels per module.

AIM-72E

The AIM-72E module provides debug and in-circuit emulation capabilities for the 3870 series microcomputers (3870, 3872, 3874 and 3876) on the MATRIX. Multiple-breakpoint capability and single-step operation allow the designer complete control over the execution of the 3870 Series microcomputer.

Register, Port display, and modification capability provides information needed to find system "bugs." All I/O is in the user's system connected to AIM-72 by a 40-pin interface cable.

The debugging operation is controlled by ZAIM-72, a mnemonic debugger which controls the interaction between the Z80 host computer and the 3870 slave. It includes a history module for the last 1024 CPU cycles and also supports all 3870 family circuits.

Assembly and linking is done using the MACRO-70 Assembler and the standard FLP-80DOS linker.

DDT

The Designer's Debugging Tool consists of commands for facilitating an otherwise difficult debugging process. The MATRIX rapid source changes through the editor and re-assemblies, followed by DDT operations close the loop on the debug cycle. The DDT commands include:

- Memory - display, update, or tabulate memory
- Port - display, update or tabulate I/O ports
- Execute - execute user's program
- Hexadecimal - performs 16 bit add/sub
- Copy - copy one block to another

Summary of Editor Commands

- Advance N - advance line pointer N line
- Backup N - backs up N lines
- Change N/S1/S2 - change N occurrences of String 1. to String 2
- Delete N - delete current line plus next N-1 lines of text
- Exchange N - exchanges current line plus next N-1 lines with lines to be inserted while in insert mode
- Get file - reads another file and inserts it into the file being edited after the current line
- Insert - place Editor in insert mode. Text will be inserted after present line
- Line N - place line pointer on Line N.
- Macro 1 or Macro 2 - defines Macro 1 or Macro 2 by the following string of Text Editor commands.
- Put N file - outputs N lines of the file being edited to another disk file.
- Quit - stores off file under editing process and returns to Monitor environment
- Search N/S1 - searches from existing pointer location until Nth occurrence of string S1 is located and prints it.
- Top - inserts records at top of file before first line.
- Verify N - print current record to console plus next N-1 records while advancing pointer N records ahead.
- Write N - prints current records plus next N-1 records to source output device while advancing pointer N records.
- eXecute N - executes Macro 1 or Macro 2 as defined by Macro command.
- Breakpoint - sets software trap in user code for interrupting execution in order to examine CPU registers
- Register - displays contents of user's registers
- Offset - enters address adder for debug of relocatable modules
- Fill - fills specified portion of memory with 8 bit byte
- Verify - compares two blocks of memory
- Walk - software single step/multistep
- Quit - returns to Monitor

Debuggers for other processors have similar or enhanced capability and are included with the appropriate AIM™.

INPUT VOLTAGE

100/115/230 volts AC± 10%
50 Hz (MK78189) or 60 Hz (MK78188)

OUTPUT VOLTAGES

CPU subsystem +5 VDC at 12 A max.
+12 VDC at 1.7 A max.
-12 VDC at 1.7 A max.
Disk subsystem +5 VDC at 3.0 A max.
-5 VDC at 0.5 A max.
+24 VDC at 3.4 A max.

OPERATING TEMPERATURE

+10°C to +40°C

OVERALL DIMENSIONS

CPU subsystem - 8" high x 21" wide x 22" deep
(20.3 cm x 53.3 cm x 55.8 cm)

Disk subsystem - 8" high x 21" wide x 22" deep
(20.3 cm x 53.3 cm x 55.8 cm)

HUMIDITY

Up to 90% relative, noncondensing.

MATERIAL

Structural Foam (Noryl)

WEIGHT

CPU Subsystem 25 lbs. (11.3 Kg)
Disk Subsystem 50 LBS. (22.7 Kg)

FAN CAPACITY

115 CFM

CARD CAGE

Six slots DIN 41612 type connectors

ORDERING INFORMATION

BASIC SYSTEM

DESIGNATOR	DESCRIPTION	PART NO.
MATRIX™	Z80 floppy disk-based microcomputer with 60K bytes of RAM (56K bytes contiguous RAM), 4K bytes PROM bootstrap, two 250K-byte single-density floppy disk drives with Operations Manual. Includes the software packages of FLP-80DOS and MACRO-80 distributed on diskette. Requires signed license agreement with purchase order.	MK78188 (60 Hz) MK78189 (50 Hz)
	MATRIX™ Operations Manual Only	MK79730
	FLP-80DOS Operations Manual Only	MK78557
	MACRO-80 Operations Manual Only	MK79635

IN-CIRCUIT EMULATION MODULES

DESIGNATOR	DESCRIPTION	PART NO.
AIM-80E	2.5 MHz RAM-based Z80 In-Circuit Emulator with buffer box, cables and Operations Manual	MK78106
	AIM-80E Operations Manual Only	MK78559
AIM-Z80AE	4.0 MHz RAM-based Z80 In-Circuit Emulator with expanded history trace, buffer box, cables and Operations Manual 16K Bytes emulation RAM 32K Bytes emulation RAM	MK78181-1 MK78181-2
	AIM-Z80AE Operations Manual Only	MK79650
AIM-72E	RAM-based In-Circuit Emulator for the 3870 series of single-chip microcomputers (3870, 3872, 3874 and 3876) with cables and Operations Manual	MK79077
	AIM-72E Operations Manual Only	MK79079

PRELIMINARY

MOSTEK[®]

DEVELOPMENT SYSTEMS

MATRIX-80/SDT

MK78197

FEATURES

- Z80 CPU based
- 4K-byte PROM bootstrap and Z80 debugger
- RAM option of 48K or 64K bytes
- Two 8-bit I/O ports for Line Printer PROM programmer
- Serial port: RS-232C and 20mA current Loop
- One single-density, single-sided disk drive; 250K bytes per floppy disk
- Device drivers for paper tape readers, punches, card readers, line printers, Silent 700's, Teletypes and CRT's are included. Others can be added
- PROM programmer I/O port. Programmer itself is optional
- BUS compatible with Mostek STD-Z80 MD Series boards

DEVELOPMENT
SYSTEMS

MOSTEK®

DEVELOPMENT KITS

MDX-PROTO

MK77951-0, MK77951-4

FEATURES

- STD-Z80 Bus compatible
- 6-slot card cage with mother board (MK77954)
- MDX-CPU1 module (MK77850-0, MK77850-4)
- MDX-DRAM8 module (MK77750-0): 2.5MHz version
- MDX-DRAM16-4 module (MK77754-4): 4MHz version
- MDX-DEBUG module (MK77950-0, MK77950-4)
- MD-WW2 Wire-wrap board (MK77952)
- MD-EXT Extender board (MK77593)
- Cables for RS-232 device (MK77955) or TTY (MK77956)
- 4MHz option available (MDX-PROTO-4)

DESCRIPTION

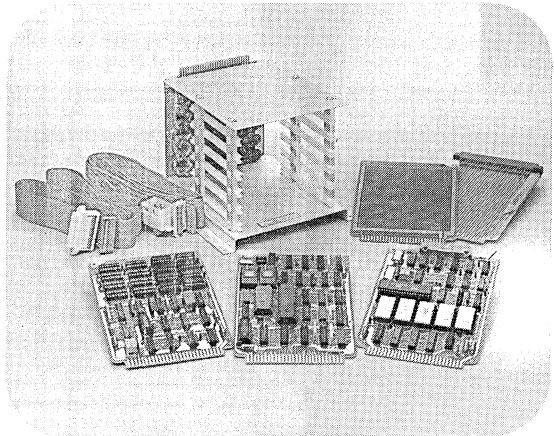
The Mostek MDX-CPU1 is the heart of an MD Series Z80 system. Based on the powerful Z80 microprocessor, the MDX-CPU1 can be used with great versatility in an OEM microcomputer system application. This is done simply by inserting custom ROM or EPROM memories into the sockets provided on the board and configuring them virtually anywhere within the Z80 memory map.

On-board memory is provided in the form of 4K of EPROM (two-2716's) and 256 bytes of scratchpad RAM as pictured in the block diagram. In addition, a MK3882 Counter/Timer Circuit is included on the MDX-CPU1 to provide counting and timing functions for the Z80. Either 2716 EPROM can be located at any 2K boundary within any given 16K block in the Z80 memory map via a jumper arrangement.

The MDX-CPU1 can be used in conjunction with the MDX-DEBUG and MDX-DRAM modules to utilize DDT-80 and ASMB-80 in system development. This is accomplished by strapping the scratchpad RAM to reside at location F00 so that it will act as the Operating System RAM for DDT-80.

The MDX-CPU1 is also available in a 4MHz version (MDX-

MDX-PROTO BOARD PHOTO



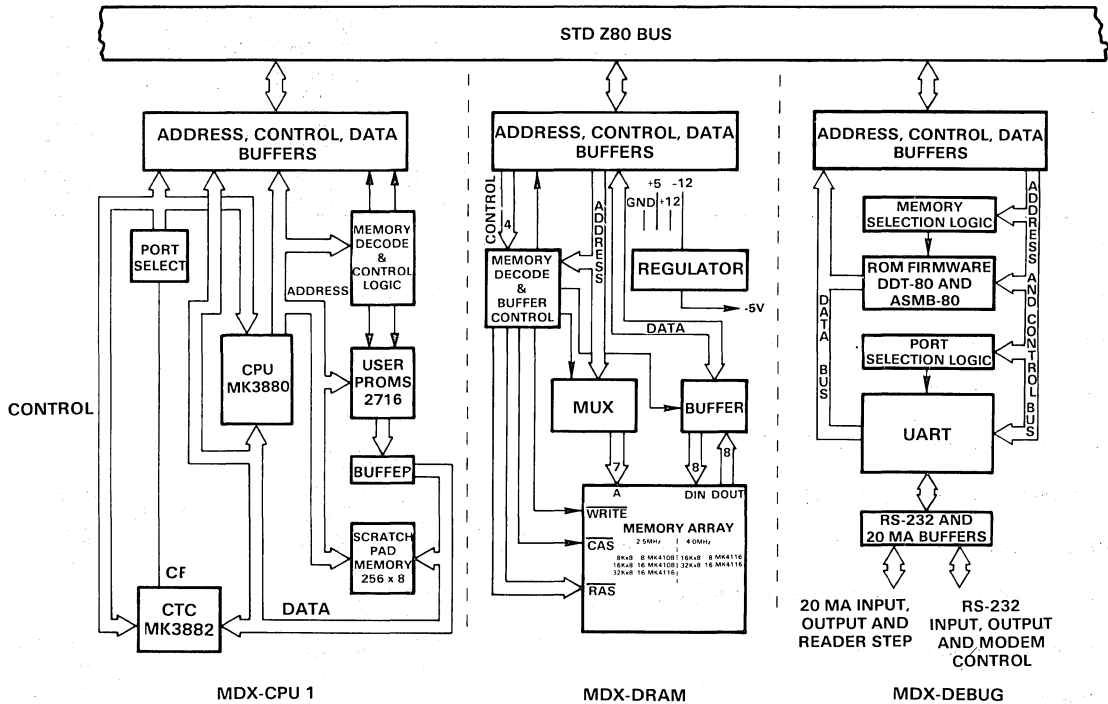
CPU1-4). In this version, one wait cycle is automatically inserted each time on-board memory is accessed by a read or write cycle. This is necessary to make the access times of the 2716 PROMs and the 3539 scratchpad RAM compatible with the MK3880-4 4MHz Z80-CPU.

MDX-DRAM DESCRIPTION

The MDX-DRAM is designed to be a RAM memory expansion board for the Mostek MD Series of Z80 based microcomputers. It is available in three memory capacities: 8K bytes (MDX-DRAM8), 16K bytes (MDX-DRAM16), and 32K bytes (MDX-DRAM32). Additionally, the MDX-DRAM16 and the MDX-DRAM32 are available in a 4MHz version. Thus, the designer can choose from the various options to tailor his add-on dynamic RAM directly to his system requirements.

The MDX-DRAM8 is designed using Mostek's MK4108 8,192-bit dynamic RAM. The MDX-DRAM32 utilizes high-performance MK4116, 16K-bit dynamic RAMs which allow 4MHz versions of these boards to be offered. No wait-state insertion circuitry is required on any of the RAM cards.

MDX-PROTO BLOCK DIAGRAM



Address selection is provided on all MDX-DRAM cards for positioning the 8K, 16K, or 32K of memory to start on any 4K boundary.

MDX-DEBUG DESCRIPTION

The MDX-DEBUG Module has sockets for 10K bytes of masked ROM that are populated with a Z80 firmware package (DDT-80/ASMB-80). This module has a STD BUS interface and is available in both 2.5MHz and 4.0MHz versions. Included on board is a fully buffered asynchronous I/O port capable of 110-19200 baud rates. Serial Data interfaces are available for 20mA current loop (with reader step control) and RS-232.

DEBUGGER DESCRIPTION

DDT-80 is the Operating System for the MDX-DEBUG Module and resides in a 2K ROM (MK34000 series). It provides the necessary tools and techniques to operate the system i.e., to efficiently and conveniently develop microcomputer software. DDT-80 is designed to support the user from initial design through production testing. It allows the user to display and update memory, registers and ports, load and dump object files, set breakpoints, copy blocks of memory, and execute programs.

DDT-80 COMMAND SUMMARY

- M s - Display and/or update the contents of memory location s.
- M s, f - Tabulate the contents of memory locations s through f.
- P s - Display and/or update the contents of I/O port s.
- D s,f - Dump the contents of memory locations s through f in a format suitable to be read by the L command.
- L - Load data which is in the appropriate format into memory.
- E s - Transfer control from DDT-80 to a user's program starting at location s.
- H - Perform 16-bit hexadecimal addition and/or subtraction.
- C s,f,d - Copy the contents of memory locations s through f to another location in memory starting at location d.
- B s - Insert a breakpoint in the user's program (must be in RAM) at location s which transfers control back to DDT-80. This allows the user to intercept his program at a specific point (location s) and examine memory and CPU registers to determine if his program is working correctly.
- R - Display the contents of user registers.

The s,f, and d represent start, finish, and destination operands required for each command.

MEMORY, PORT AND REGISTER COMMANDS (M,P,R)

The M, P, and R commands provide the means for displaying the contents of specified memory locations, port addresses, or CPU registers. The M and P commands sequentially access memory locations or ports and display their contents. The user has the option of updating the content of the memory location or port. (Note some ports are output only and their contents cannot be read or displayed.) The M command also gives the user access to the CPU registers through an area in RAM called the Register Map (discussed in the Execute and Breakpoint section below).

The M and R commands are used to tabulate blocks of memory locations (M) or the CPU registers (R). The M command will accept two operands, the starting and ending addresses of the memory block to be tabulated. The R command will accept either no operand or one. If no operand is specified, the CPU registers will be displayed without a heading. If an operand is specified, then a heading which labels the register contents will be displayed as well.

EXECUTE AND BREAKPOINT (E,B)

The E command is used to execute all programs, including aids such as the Assembler. The B command is used to set a breakpoint to exit from a program at some predetermined location for debugging purposes. At the instant of a breakpoint exit, the contents of all CPU registers are saved in a designated area of MDX-DEBUG RAM called the Register Map. In the Register Map, the register contents may be examined or modified using the M command and a predefined mnemonic (or absolute address) of the storage location for that register (example: PC, :A,....,SP). The Register Map is also used to initialize the CPU registers whenever execution is initiated or resumed. Thus the E and B commands can be used together to initialize, execute, and examine the results of individual program segments.

The B command gives the user the option of having all CPU registers displayed when the breakpoint is encountered. This is done by entering a second operand to the B command. Otherwise, DDT-80 defaults to displaying the PC and AF registers. When all CPU registers are displayed, the format is the same as for the R command previously discussed.

LOAD, DUMP, AND COPY, (L,D,C)

The L and D commands load and dump object files through the object I/O channel in standard industry Hex format. Check sums are used for error detection, and the addresses of questionable blocks are typed automatically while loading.

The C command will copy the contents of the memory block specified to another block of memory. There are no restrictions on the direction of the copy or on whether the blocks overlap.

HEXADECIMAL ARITHMETIC (H)

The H command is a dummy command used to allow hexadecimal addition and subtraction for expression evaluation without performing any other operation.

DDT-80 I/O CAPABILITIES

DDT-80 specifies I/O channels, designated 'Console', 'Object', and 'Source', to which any suitable devices may be assigned. The Channel Assignment Table is located in RAM where it may be examined or modified using the M command. The table addresses correspond to the I/O channels and the table contents correspond to the addresses of the peripheral driver routines. A channel which has a device assignment may have that device assignment changed using the M command. This is accomplished by merely modifying the table contents of that channel's table address to correspond to the new peripheral driver routine. A set of peripheral driver routines is supplied and listed below. This scheme also allows the user to write a driver routine for his own peripheral, load it into memory, and easily configure that peripheral into the system.

DDT-80 I/O PERIPHERAL DRIVERS

1. A serial input driver (usually a keyboard).
2. A serial output driver (usually a CRT or teletype typehead).
3. A serial input driver which sends out a reader step signal (usually a teletype reader).
4. A serial output driver which forces a delay after a carriage return (usually a Silent 700 typehead).
5. A parallel input driver (usually for high-speed paper tape input)
6. A parallel output driver (usually for high-speed paper tape output).
7. A parallel output driver (usually for a line printer).

TEXT EDITOR DESCRIPTION

The Text Editor permits random access editing of ASCII character strings. It can be used as a line or character-oriented editor. Individual characters may be located by position or context. The Editor works on blocks of characters which are typically read into memory from magnetic tape or paper tape. Each edited block can be output to magnetic tape or paper tape after editing is completed. While the primary application for the Text Editor is in editing assembly language source statements, it may be applied to any ASCII test delimited by "carriage returns".

The Editor has a macro command processing option. Up to two sets of commands may be stored and processed at any time during the editing process. All I/O is done via the DDT-80 channels. The Editor can be used with the Mostek

ASMB-80 Assembler and Loader to edit, assemble, and load programs in memory without the need for external media for intermediate storage.

LIST - turn listing on
NLIST - turn listing off

The following commands are recognized by the Text Editor:

An - Advance record pointer n records
Bn - Backup record pointer n records
Cn dS1dS2D - Change string S1 to string S2 for n occurrences
Dn - Delete n records
E - Exchange current record with records to be inserted
I - Insert records
Ln - Go to line number n.
Mn - Enter command buffers (pseudo-macro)
N - Print top, bottom and current line number
Pn - Punch n records from buffer
R - Read source records into buffer
Sn dS1d - Search for nth occurrence of signal S1

ASSEMBLER DESCRIPTION

The Assembler reads Z80 source mnemonics and pseudo-ops and outputs an assembly listing and object code. The assembly listing shows address, machine code, statement number, and source statement. The object code is in industry-standard hexadecimal format modified for relocatable, linkable assemblies.

The Assembler supports conditional assemblies, global symbols, relocatable programs and a printed symbol table. It can assemble any length program, limited only by a symbol table size which is user-selectable. Expressions involving addition and subtraction are allowed. A global symbol is categorized as "internal" if it appears as a label in the program; otherwise it is an "external" symbol. The printed symbol table shows which symbols are internal and which are external. The assembler allows the user to select relocatable or non-relocatable assembly via the "PSECT" pseudo-op. Relocation records are placed in the object output for relocatable assemblies. (The Mostek object format is defined below.) The Assembler can be run as a single-pass assembler or as a learning tool. (In this mode, global symbols and forward references are not allowed.) The following pseudo-ops are recognized by the Assembler:

EQU - equate label
DEFL - define label
DEFM - define message
DEFB - define byte
DEFW - define word
DEFS - define storage
END - end statement
NAME - program name definition
PSECT - global symbol definition
Supports the following assembler pseudo-ops
EJECT - eject a page of listing
TITLE - place heading at top of each page

RELOCATING LINKING LOADER DESCRIPTION

The Mostek Relocating Linking Loader provides state-of-the-art capability for loading programs into memory by allowing loading and linking of any number of relocatable and non-relocatable object modules. Non-relocatable modules are always loaded at their starting address as defined by the ORG pseudo-op during assembly. Relocatable object modules can be positioned anywhere in memory at an offset address.

The Loader automatically links and relocates global symbols which are used to provide communication or linkage between program modules. As object programs are loaded, a table containing global symbol references and definitions is built up. At the end of each module, the loader resolves all references to global symbols which are defined by either the current or a previously loaded module. It also prints on the console device the number of defined global symbols that have been referenced. The symbol table can be printed in order to list all global symbols and their load address. The number of object modules which can be loaded by the Loader is limited only by the amount of RAM available for the modules and the symbol table. Space for the symbol table is allocated dynamically downward in memory from either the top of memory or from a specified address entered as an operand of the load command.

All I/O is done via the DDT-80 channels. Assemblies can be done from source statements stored in memory (by the Editor). The object output can be directed to a memory buffer rather than to an external device. Thus, assembly and loading can be done without external storage media.

The Loader prints the beginning and ending address of each module as it is loaded. The transfer address as defined by the END pseudo-op is printed for the first module loaded. The Loader execute command (E) can be used to automatically start execution at the transfer address.

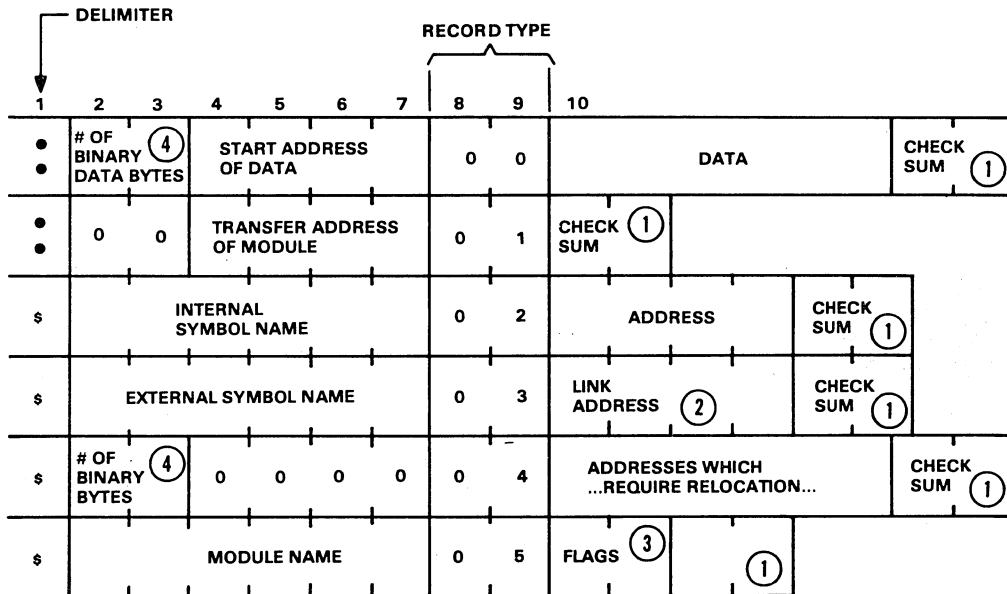
The Loader Commands are the following:

L offset - load object module at address "offset" plus program origin address
E - execute loaded program at transfer address of first module
T - print global symbol table

MOSTEK OBJECT OUTPUT DEFINITION

Each record of an object module begins with a delimiter (colon or dollar sign) and ends with carriage return and line feed. A colon (:) is used for data records and end-of-file record. A dollar sign (\$) is used for records containing relocation information and linking information. All information is in ASCII. Each record is identified by "type". The type is determined by the 8th and 9th bytes of the record which

OBJECT MODULE TYPES



NOTES:

1. Check Sum is negative of the binary sum of all bytes except delimiter and carriage return/line feed.
2. Link Address points to last address in the data which uses the external symbol. This starts a backward link list through the data records for that external symbol. The list terminates at OFFFHH.
3. The flags are one binary byte. Bit 0 is defined as:
0 - absolute module
1 - relocatable module
4. Maximum of 64 ASCII bytes.

can take the following values:

- 00 - data
- 01 - end-of-file
- 02 - internal symbol
- 03 - external symbol
- 04 - relocation information
- 05 - module definition

MDX-CPU1 SPECIFICATIONS

WORD SIZE

Instruction: 8, 16, 24, or 32 bits
Data: 8 bits

CYCLE TIME

Clock period or T state = 0.4 microsecond at 2.5MHz
0.25 microsecond at 4.0MHz
Instructions required from 4 to 23 T states

MEMORY CAPACITY

On-Board EPROM - 4K bytes (sockets only)
On-Board RAM-256 bytes
Off-Board Expansion - Up to 65,536 bytes with user-Board Expansion - specified combinations of RAM, ROM, PROM

MEMORY ADDRESSING

On-Board EPROM: jumper-selectable for any 2K boundary within a 16K block of Z80 memory map.
On-Board RAM: FF00-FFFF

MEMORY SPEED REQUIRED

Memory	Access Time	Cycle Time
2716*	450ns	450ns

*Single 5-volt type required

I/O ADDRESSING

On-Board Programmable Timer

Port Address (HEX)	MK3882 Channel
7C	0
7D	1
7E	2
7F	3

I/O CAPACITY

Up to 252 port address can be decoded off-board. Four port addresses are on-board. $252 + 4V = 256$ total I/O ports.

INTERRUPTS

Multi-level with three vectoring modes (Mode 0,1,2). Interrupt requests may originate from user-specified I/O or from the on-board MK3882 CTC.

SYSTEM CLOCK

	MIN	MAX
MDX-CPU1	500 kHz	2.50MHz
MDX-CPU-4	500 kHz	4.0MHz

SYSTEM INTERRUPT UNITS (SIU) = 1

STD BUS INTERFACE

Inputs: One 74LS load max.
Outputs: $I_{OH} = -3mA$ min. at 2.4 volts
 $I_{OL} = 24mA$ min. at 0.5 volts

OPERATING TEMPERATURE

0°C to 60°C

POWER SUPPLY REQUIREMENTS

5V \pm 5% at 1.1A maximum

MDX-DRAM SPECIFICATIONS

WORD SIZE

8 bits

MEMORY SIZE

MDX-DRAM8 - 8,192 bytes
MDX-DRAM16 - 16,384 bytes
MDX-DRAM32 - 32,768 bytes

ADDRESS SELECTION

Selection of 8K, 16K, or 32K contiguous memory blocks to reside at any 4K boundary.

ACCESS TIME

	System Clock	Memory Access Times	Memory Cycle Times
MDX-DRAM	2.5MHz	350ns max.	465ns min.
MDX-DRAM-4	4.0MHz	200ns max.	325ns min.

SYSTEM CLOCK

	MIN	MAX
MDX-DRAM	1.25MHz	2.5MHz
MDX-DRAM-4	1.25MHz	4.0MHz

SYSTEM INTERRUPT UNITS (SIU) = 1

STD BUS INTERFACE

Inputs: One 74LS load max.
Outputs: $I_{OH} = -3mA$ min. at 2.4 volts
 $I_{OL} = 24mA$ min. at 0.5 volts

OPERATING TEMPERATURE

0°C to 60°C

POWER SUPPLY REQUIREMENTS

+5V \pm 5% at 0.6A max.
+12V \pm 5% at 0.25A max.
-12V \pm 5% at 0.03A max.

MDX-DEBUG SPECIFICATIONS

WORD SIZE

8 bits for PROM
5 to 8 bits for serial I/O

MEMORY SIZE

10K bytes of firmware

MEMORY ADDRESSING

2K blocks jumper-selectable for any 2K boundary within a given 16K block of the Z80 memory map. MDX-DEBUG has ROMs strapped every 2K beginning at C000H.

I/O ADDRESSING

On-board Serial I/O Port
 Control Port: XXXXXX01
 Data Port: XXXXXX00
 Module and Reader Step Control Port: XXXXXX10
 XXXXXX represents six strap-selectable address bits

SYSTEM CLOCK

	MIN.	MAX.
MDX-DEBUG	250KHz	2.5MHz
MDX-DEBUG-4	250KHz	4.0MHz

SERIAL COMMUNICATIONS INTERFACE

SIGNAL	BUFFERED FOR:	
	20mA Current Loop	RS-232
Transmitted data	Output	Output
Received data	Input	Input
Data Terminal Read (DTR)		Input
Request to Send (RTS)		Input
Carrier Detect (CDET)		Output
Clear to Send (CTS)		Output
Data Set Ready (DSR)		Output
Reader Step relay (RS)	Output (40mA)	

SYSTEM INTERRUPT UNITS (SIU) = 0

STD BUS INTERFACE

Inputs: One 74LS load max.
 Outputs: $I_{OH} = -3\text{mA min. at } 2.4\text{ volts}$
 $I_{OL} = 24\text{mA min. at } 0.5\text{ volts}$

OPERATING TEMPERATURE

0°C to 60°C

POWER SUPPLY REQUIREMENTS

+12 Volts $\pm 5\%$ at 50 mA max.
 -12 Volts $\pm 5\%$ at 35 mA max.
 +5 Volts $\pm 1.2\text{ mA max.}$

I/O TRANSFER RATE

110, 300, 600, 1200, 2400, 4800, 9600, 19200 baud

CARD DIMENSIONS

4.5 in. (11.43 cm) high by 6.50 in. (16.51 cm) long
 0.48 in. (1.22 cm) maximum profile thickness
 0.062 in. (.016 cm) printed-circuit-board thickness

CONNECTORS

Function	Configuration	Mating Connector
STD-Z80 BUS	56-pin	PRINTED CIRCUIT Viking 3VH28/ 1 CE5
	0.125 in. centers	WIRE WRAP Viking 3VH28/ 1 CND5 SOLDER LUG Viking 3VH28/ 1 CN5
Serial I/O	26-pin	FLAT RIBBON Ansley 609 2600M
	0.100 in. grid	DISCRETE WIRES Winchester PGB26A (housing) Winchester 100-700205 (contacts)



ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
MDX-PROTO	Prototyping package with Operations Manuals, 2.5 MHz version. Note: 2.5 MHz version includes 8K dynamic RAM board MDX-DRAM8 only.	MK77951
MDX-PROTO-4	Prototyping package with Operations Manuals. 4.0 MHz version. Note: 4.0 MHz version includes 16K dynamic RAM board MDX-DRAM16-4.	MK77951-4

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HARDWARE FEATURES

- Direct interface with OEM-80E
- Single-step/multistep with register trace
- Execution intercept (breakpoint) intercepts on memory access, port access, external trigger, event counter, or delay counter
- Push-button execution intercept
- 256 x 32 history memory which samples Data Bus, Address Bus, M1, MREQ, RD, IORQ, and four external probes
- History memory clock-selectable from M1, MREQ, IORQ, or INTERRUPT ACKNOWLEDGE
- Selectable history memory clock conditions: read only, write only, DMA only, or external probe only (high or low)
- 8K x 8 ROM memory (firmware)

SOFTWARE FEATURES

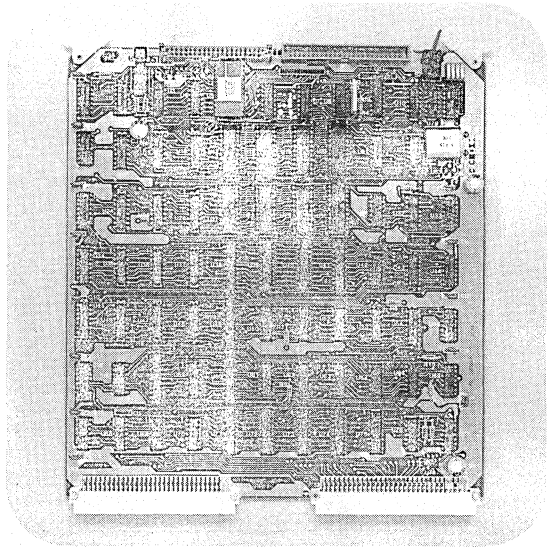
- ROM-resident mnemonic dis-assembler
- ROM-resident RAM test for SDB or target RAM

DESCRIPTION

AIM-80E provides Z80 system debug assistance for both software and hardware via in-circuit emulation. (See Block Diagram)

Single-step/multistep allows the programmer to trace through a program and display the CPU registers after each instruction. The execution intercept feature allows suspending program execution on the nth occurrence of an address or other specified condition. If the program has begun an unknown sequence, the intercept pushbutton will

AIM-80E BOARD PHOTO

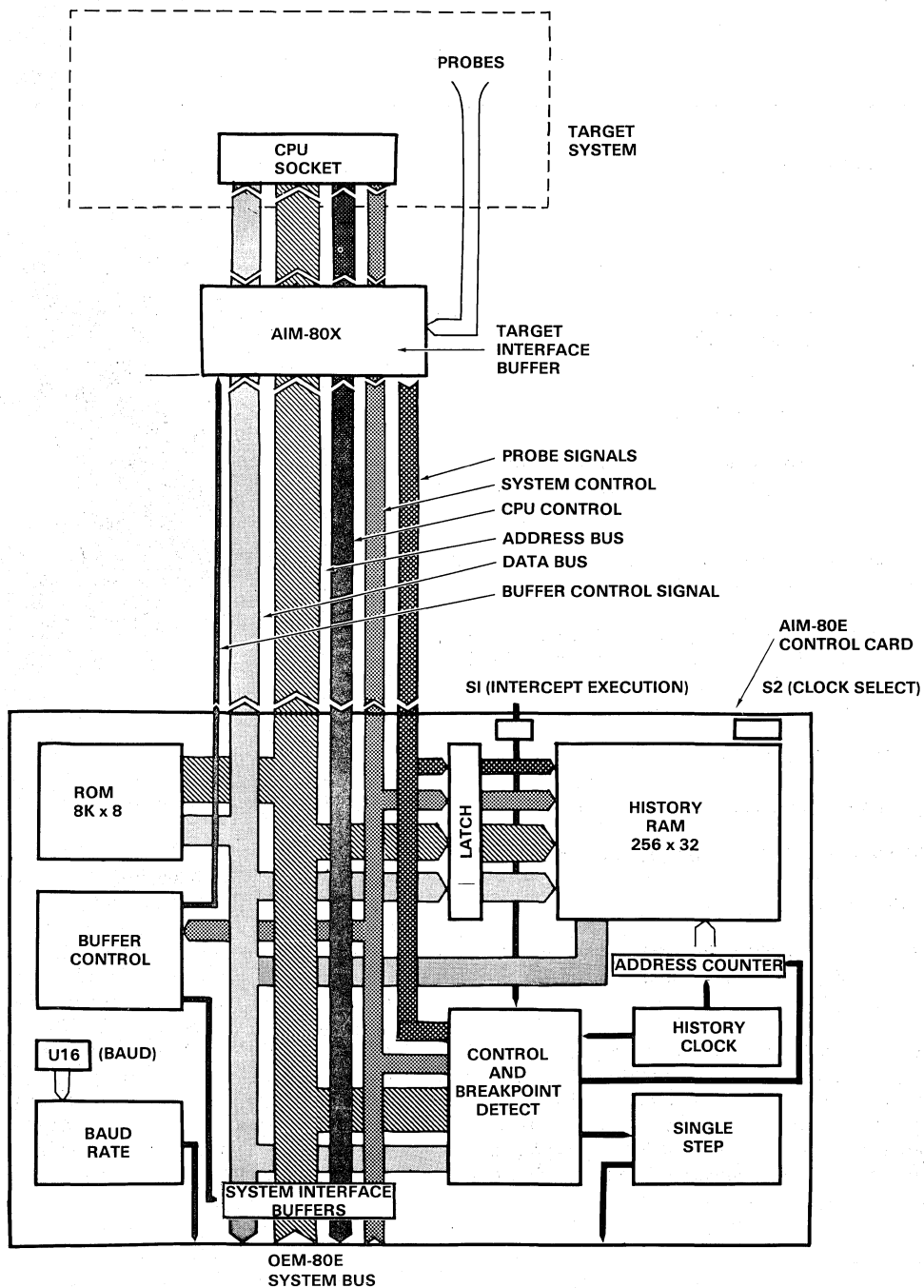


return the system to the single-step mode. Single-step and execution intercept (breakpoint) operate in RAM or ROM/PROM.

Hardware debugging is aided greatly by use of the 256 x 32 history memory which monitors bus transactions for a specified period. This information may then be displayed on the console. The data bus, address bus, M1, MREQ, RD, IORQ, and inputs from four probes are sampled and stored in the history memory upon every occurrence of the user-specified clock (M1, MREQ, IORQ, or interrupt acknowledge) qualified by the user-specified conditions (read only, write only, DMA only, probe High only, or probe Low only). Upon the occurrence of the selected intercept, AIM-80E returns control to the system debug (DDT-80). The history memory may then be displayed (See Figure 1) with or without mnemonic dis-assembly.

* Trademark of Mostek Corporation

BLOCK DIAGRAM



AIM-80E PRINT OUT EXAMPLE
(User entries underlined>)

.I 2, T 2

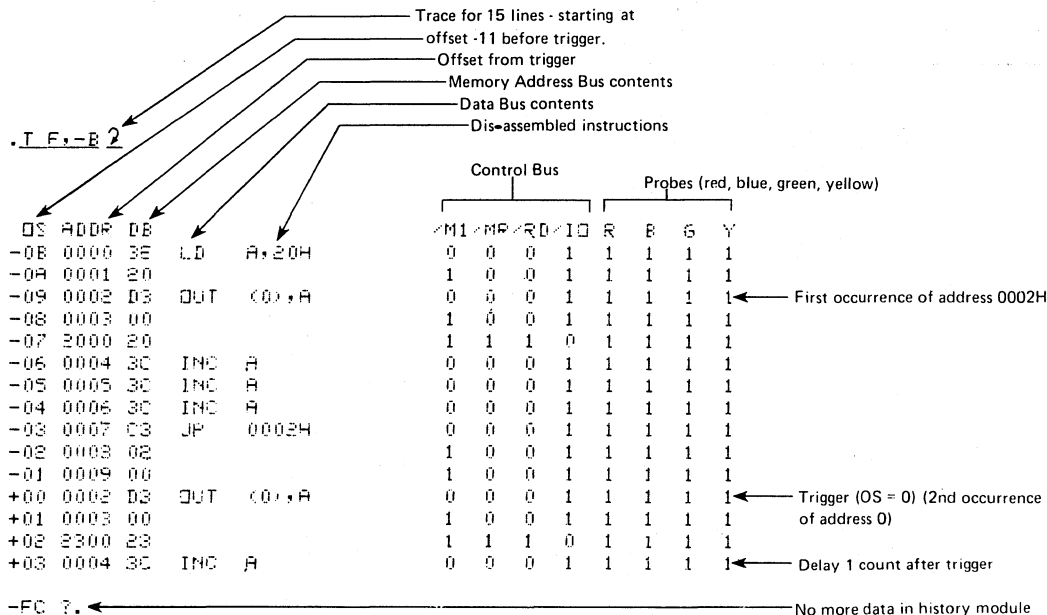
Set intercept at address 0002H with trigger option

TRIG ON (MREQ/IOREQ/+-) M
EVENT CNT (1-FF) 2
DELAY CNT (0-FF) 3
CLOCK ON (M1, MREQ, IOREQ, INTA) MR IO
ONLY IF (RD/WR/DMA/HOLD)

Trigger on MREQ
After 2 occurrences
Delay 1 clock after trigger
Clock history (sample) memory on MREQ or IOREQ
No qualifying conditions selected
Begin execution at address 0002H
Intercept occurs at second occurrence of address 2 with a delay of one.

.E 0 2
0005 2421

At this point the history memory contains the bus transactions which occurred before the intercept.



USING THE AIM-80E

AIM-80E may be added directly to any OEM-80E system. All system bus signals are wired one to one between OEM-80E and AIM-80E. Voltage requirements for the AIM-80E are the same as for the OEM-80E. Programs may be debugged in OEM-80E memory space or, with the target interface buffer box (AIM-80X), may be debugged in the target environment. Dynamic memory mapping allows target memory to be simulated using OEM-80E system RAM. All peripheral devices of the OEM-80E are still functions with the AIM-80E.

SYSTEM FIRMWARE

To minimize the impact of the AIM-80E, firmware is resident in one MK36000, 8K x 8 ROM. This firmware is completely compatible with DDT-80 firmware and includes five new commands for control of the AIM-80E. The interactive nature of the commands makes operation simple and avoids operator errors. The ROM-resident dis-

assembler makes correlation with the user's source listing easier and reduces the necessity of memorizing op codes.

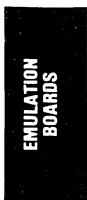
OPERATING FREQUENCY
2.5 MHz (with OEM-80E)

INTERFACE
OEM-80E compatible

TOP CONNECTORS
One 40-pin 3M ribbon
One 50-pin 3M ribbon

OPERATING TEMPERATURE RANGE
0°C to +50°C

POWER SUPPLY REQUIREMENTS (Typical)
+12V ± 5% at 12mA
+5V ± 5% at 1.0 Amp



BOARD SIZE
250mm x 233.4mm x 18mm

BOTTOM CONNECTORS
Dual 64-pin Eurocard
Connector, DIN 41612, form
D; A and C Pinned

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
AIM-80E	AIM-80E Control Card includes AIM-80E Firmware and AIM-80E Operations Manual Target Interface Buffer (AIM-80X) includes: cables, connectors, 4 probe clips	MK78106
	AIM-80E Operations Manual only	MK78559

MOSTEK®

DEVELOPMENT SYSTEMS EMULATION BOARDS

AIM*-Z80AE

MK78181-1, MK78181-2

HARDWARE FEATURES

- Direct interface to Mostek's development system
- In-circuit emulation of Z80 or Z80A microprocessors
- Real-time execution (4 MHz - no wait states)
- Flexible breakpoints (hardware and eight single-byte software)
- Single-step execution
- 16K bytes emulation RAM (expandable to 32K bytes)
- Memory Mappable into Target system in 256 byte blocks
- Illegal write to memory detection
- Nonexistent memory access detect
- Forty-eight channel by 1024 words history memory
- Event counter
- Delay counter
- Execution T-state timer
- Keyboard escape function

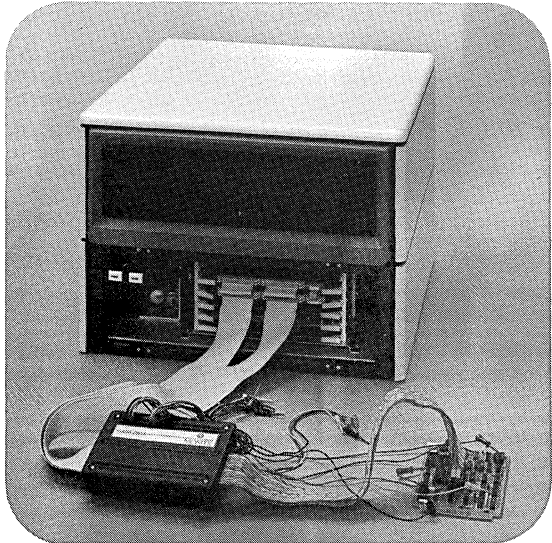
SOFTWARE FEATURES

- Simple-to-use, single character commands
- Flexible display format includes disassembly of opcodes
- System configuration parameters stored on disk for future use

DESCRIPTION

AIM-Z80AE is an advanced development tool which provides debug assistance for both software and hardware via in-circuit emulation of the Z80 microprocessor. Use of the AIM-Z80AE is completely transparent to the user's final system configuration (referred to as the Target). No memory

AIM-Z80AE SYSTEM PHOTOGRAPH



space or ports are used and all signals including $\overline{\text{RESET}}$, $\overline{\text{INT}}$ and NMI are functional during emulation.

Single-step circuitry allows the user to execute Target instructions one at a time to see the exact effect of each instruction. Single step is functional in ROM as well as RAM.

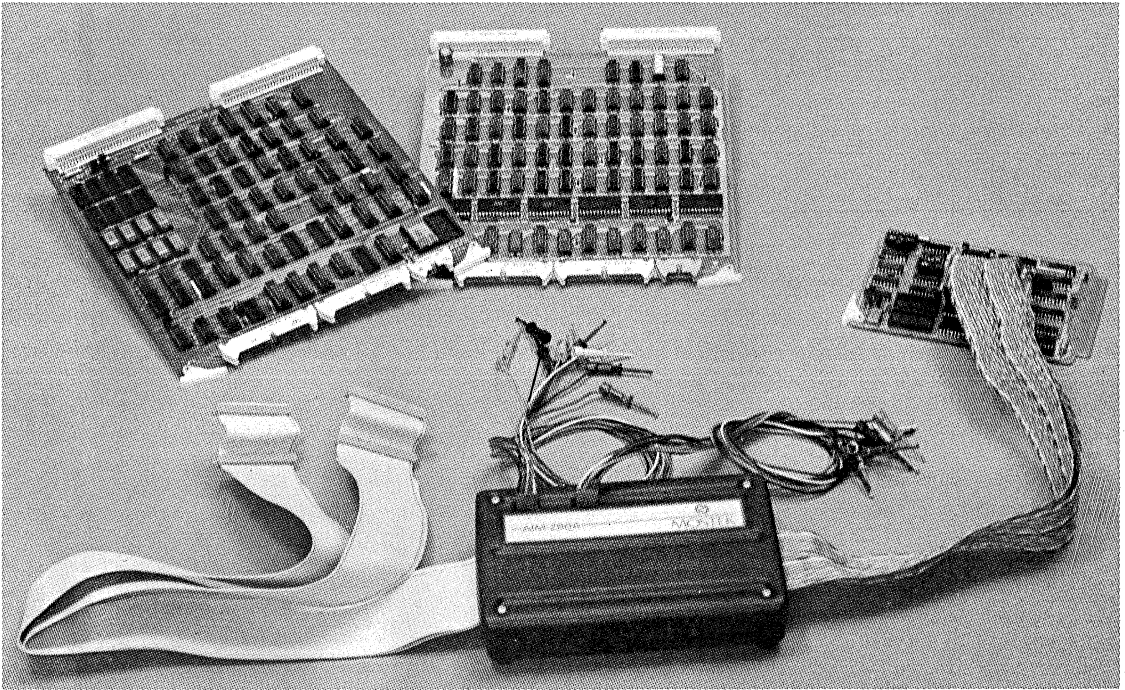
Sixteen K bytes of emulation RAM may be mapped into the Target memory map at any desired address so that software may be developed even before Target memory is available.

Breakpoint-detect circuitry allows real-time execution to proceed to any desired point in the user's program and then terminate with all registers and status information saved so that execution may later be resumed. Real-time execution may also be terminated at any time by enabling the Escape Key. EVENT and DELAY counters give added flexibility for viewing the exact point of interest in the user's program.

A 48-channel history circuit will simultaneously record any bus transaction which the user may desire to see. The address bus, data bus and control signals plus eighteen external probes which can be used to monitor the Target system's circuitry at other points are recorded by the History circuit.

*Trademark of Mostek Corporation

SYSTEM PHOTOGRAPH
AIM-Z80AE



USING THE AIM-Z80AE

AIM-Z80AE is partitioned on three modules. The Control and History modules are installed directly into the development system. Cables from these modules connect to the Buffer module which plugs directly into the Target system's Z80 CPU socket. After AIM-Z80AE is installed, the development system is powered up and the system booted up as normal. All development system software and

hardware are still functional. The software to control AIM-Z80AE (AIMZ80) is initialized by using the implied run command. AIMZ80 will sign on, take control of the Target system and allow the user to initialize the Target system and use any of the AIMZ80 commands to load, test, and debug his Target program. An example of the use of some of the AIMZ80 commands is given in the following examples.

AIM-Z80AE INITIALIZATION
EXAMPLE 1

```

$AIMZ80(CR)          <Run AIM-Z80AE control program      (1)
AIMZ80 VERSION 1.0   <Sign on message                          (2)
,I E000,FFFF(CR)    <Initialize Target memory map                    (3)
IS THIS BLOCK SYSTEM MEMORY? (Y/N) Y_(CR)
ARE WRITES ALLOWED? (Y/N) Y_(CR)
,I_(CR)              <Display Target memory map                    (4)
S = SYSTEM MEMORY  T = TARGET MEMORY  P = WRITES PROTECTED

```

```

0000  T T T T      T T T T      T T T T      T T T T
1000  T T T T      T T T T      T T T T      T T T T
2000  T T T T      T T T T      T T T T      T T T T
3000  T T T T      T T T T      T T T T      T T T T
4000  T T T T      T T T T      T T T T      T T T T
5000  T T T T      T T T T      T T T T      T T T T
6000  T T T T      T T T T      T T T T      T T T T
7000  T T T T      T T T T      T T T T      T T T T
8000  T T T T      T T T T      T T T T      T T T T
9000  T T T T      T T T T      T T T T      T T T T
A000  T T T T      T T T T      T T T T      T T T T
B000  T T T T      T T T T      T T T T      T T T T
C000  T T T T      T T T T      T T T T      T T T T
D000  T T T T      T T T T      T T T T      T T T T
E000  S S S S      S S S S      S S S S      S S S S
F000  T T T T      T T T T      T T T T      T T T T

```

In the above example the system was initialized by entering AIMZ80 (1), the sign on message was printed (2), and then the I command was used to map Target address space E000 through EFFF to use the System

Emulation RAM (3). The I command with no operands was then used to display the current Target memory map configuration (4).



**SOFTWARE BREAKPOINT
EXAMPLE 2**

```
,M E000 (CR)           <Examine Target memory starting at address E000      (1)
E000 3E (CR)
E001 00 (CR)
E002 3C (CR)
E003 3C (CR)
E004 C3 (CR)
E005 00 (CR)
E006 E0 .
```

```
,B E004 (CR)           <Set software breakpoint at address E004      (2)
```

```
,E E000 (CR)           <Begin execution at address E000      (3)
```

```
,SWBP ENCOUNTERED     <Software breakpoint encountered      (4)
```

PC	AF	I	IF	BC	DE	H1	A'F'	B'C'	D'E'	H'L'	IX	IY	SP
E004	0200	0040	02FF	0000	0200	0041	0101	FFFF	0200	FFFF	FFFF	01E9	

```
,I 4, -4 (CR)         <Tabulate 4 history samples starting 4 samples (5)
                        before the breakpoint
```

OFFS	ADDR	DB	DISASSEMBLY	TYPE	PA8-----PA0	PB8-----PB0
-004	E000	3E	LD A,0	FETC	1 1111 1111	1 1111 1111
-003	E001	00		MRD	1 1111 1111	1 1111 1111
-002	E002	3C	INC A	FETC	1 1111 1111	1 1111 1111
-001	E003	3C	INC A	FETC	1 1111 1111	1 1111 1111
+000	E004	5B	BREAKPOINT CODE	FETC	1 1111 1111	1 1111 1111

```
,B C,A (CR)           <Clear all breakpoints      (7)
```

In this example, the M command is used to examine Target memory locations E000 through E006 (1), then a software breakpoint is set at address E004 (2), and execution is started at address E000 (3). The Software breakpoint is encountered at (4), and the current state of the Z80 registers is displayed. The T command is then

used to tabulate 4 history samples starting 4 samples prior to the breakpoint last encountered (5). Carriage Return is then entered to display the next sample which is the breakpoint code (6). Next all breakpoints are cleared (7).

SPECIFYING HISTORY OPTIONS

EXAMPLE 3

B, H, 0 (CR) <Specify history options (1)

TRIGGER WORD IS: PA7----PA0 A15-----A0
 XXXX XXXX 0000 0000 0000 0000
UPDATE: XXXX XXXX 1110 0000 0000 0000 (2)

TRIGGER STROBE IS (MRD,LE) ;TO CHANGE SELECT ONE: (3)
 MRD(0) MWR(1) MREQ(2) IORD(3)
 IOWR(4) IORQ(5) INTA(6) PA8(7) [,LE(8) ,TE(9)]

EVENT COUNT IS: 0001 2(CR) (4)

DELAY COUONT IS: 000 4(CR) (5)

HISTORY CLOCK IS (MRD MWR IORD IOWR) ;TO CHANGE SELECT ANY: (6)
 MRD(0) MWR(1) MRF(2)
 IORD(3) IOWR(4) PA8+(5) PA8-(6) 0,1,2,3,4(CR)

HISTORY CLOCK ENABLE IS (ALL) CYCLES ;TO CHANGE SELECT ONE: (7)
 ALL(0) DMA(1) CPU(2) PA7L(3) PA7H(4)
 TWORD(6) [, PB8L(8) ,PB8H(9)]

In this example, the H,O option is selected to specify History or Hardware breakpoint options (1). The system then allows the user to update the trigger word (2), the

trigger strobe (3), the EVENT COUNT (4), the DELAY COUNT (5), the history clock source (6), and finally the history clock enable signal.

HARDWARE BREAKPOINT

EXAMPLE 4

```
,B E000,H(CR)      < Set hardware breakpoint at E000          (1)
,E E000 (CR)       < Begin execution at E000                 (2)
,HVBP ENCOUNTERED < Hardware breakpoint encountered         (3)
```

PC	AF	IF	BC	DE	HI	A'F'	B'C'	D'E'	H'L'	IX	IY	SP
E003	0100	0040	02FF	0000	0200	0041	0101	FFFF	0200	FFFF	FFFF	01E9

```
,T(CR)             < Tabulate history starting at earliest sample. (4)
```

OFFS	ADDR	DB	DISASSEMBLY	TYPE	PAB-----PAO	PBS-----PBO
-00B	E000	3E	LD A,0	FETC	1 1111 1111	1 1111 1111
-00A	0038	3E		RFSH	1 1111 1111	1 1111 1111
-009	E001	00		MRD	1 1111 1111	1 1111 1111
-008	E002	3C	INC A	FETC	1 1111 1111	1 1111 1111
-007	0039	3C		RFSH	1 1111 1111	1 1111 1111
-006	E003	3C	INC A	FETC	1 1111 1111	1 1111 1111
-005	003A	3C		RFSH	1 1111 1111	1 1111 1111
-004	E004	C3	JP ,0E000H	FETC	1 1111 1111	1 1111 1111
-003	003B	C3		RFSH	1 1111 1111	1 1111 1111
-002	E005	00		MRD	1 1111 1111	1 1111 1111
-001	E006	E0		MRD	1 1111 1111	1 1111 1111
+000	E000	3E	LD A,0	FETC	1 1111 1111	1 1111 1111
+001	003C	3E		RFSH	1 1111 1111	1 1111 1111
+002	E001	00		MRD	1 1111 1111	1 1111 1111
+003	E002	3C	INC A	FETC	1 1111 1111	1 1111 1111
+004	003D	3C		RFSH	1 1111 1111	1 1111 1111
END OF HISTORY						

In this example, a hardware breakpoint is set at address E000 (1), and execution is started at address E000 (2). After the EVENT COUNT and DELAY COUNT are satisfied, the hardware breakpoint is encountered (3) and the Z80 registers are printed. Next the T command is used to tabulate the history memory starting at the earliest sample (4). The history memory tabulation gives the offset from the breakpoint, the address bus, the data bus, the disassembled opcodes, the type of bus cycle, the A probes and the B probes (5).

BLOCK DIAGRAM DESCRIPTION

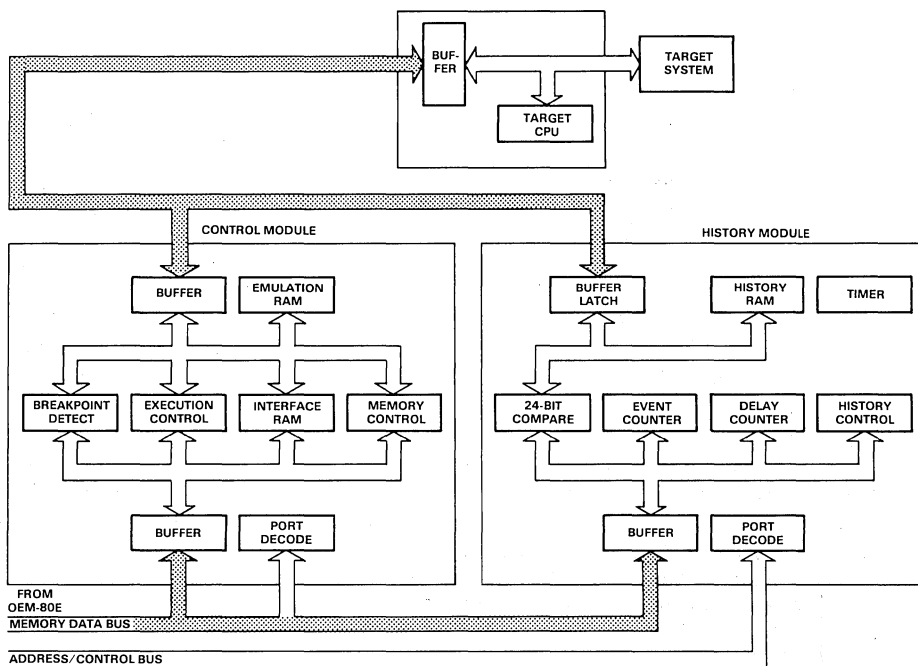
As shown in the block diagram, AIM-Z80AE consists of three modules. The buffer module, which contains the Target Z80A CPU, plugs directly into the Target system CPU socket. Address, data and control signals are buffered and cabled to the Control and History modules which are

installed in the development system.

The control module has the circuitry for detecting the breakpoint conditions. It forces execution to begin in the System Interface RAM which is loaded with an interface program and is shadowed into the Target memory space. This control program makes the Target CPU a slave to the development system. When the user desires to resume execution, the control program activates the execution control circuit and execution resumes at the desired address. The 16K byte emulation RAM may be mapped to appear at any address space in the Target memory map.

The History module has a 24-bit comparator circuit to detect the hardware breakpoint condition, the event counter, and the delay counter. Sampling into the 48 channel-by-1024 word history RAM is controlled by the History control circuit. The Timer circuit is used to count Target processor clocks for logging elapsed execution time.

AIM-Z80AE BLOCK DIAGRAM



AIM-Z80AE SOFTWARE

AIMZ80 is the software designed to operate the AIM-Z80AE system on Mostek's Dual Floppy Disk Microcomputers. It is supplied on standard FLP-80DOS diskette. The software has the same command structure as other Mostek debuggers. The commands available with AIMZ80 are summarized below. Designations s, f, and d stand for operands.

- ,B s,f Set hardware or software breakpoint at memory location s.
- ,C s,f, d Copy the Target memory block s through f to Target memory starting at d.
- ,D s,f Dump the Target memory block s through f to any desired disk file.
- ,E s,f Begin real time execution at Target memory address s with an optional breakpoint set at f.
- ,F s,f,d Fill the Target memory block s through f with data d.
- ,G s Get binary file s and load it into Target memory.
- ,H Hexadecimal arithmetic.
- ,I s,f Initialize the memory map for the Target memory block s through f.
- ,L s,f,d Locate data d in Target memory range s through f.
- ,M s Display and update Target memory at location s.
- ,M s,f,d Tabulate Target memory locations s through f. Option d specifies disassemble of Target memory.
- ,O s Set relative offset equal to s for all address operands. Extremely useful in debugging relocatable modules.
- ,P s Display and update Target port number s.
- ,Q Quit and return to FLP-80DOS Monitor.
- ,R s,f Display Target registers, Option s specifies the number of registers to be displayed and option f specifies if the heading is to be included.
- ,S s,f Single step starting at Target location s for f number of steps.
- ,T s,f Tabulate s locations of the history RAM starting at an offset of f locations from the breakpoint address.
- ,V s,f,d Verify Target memory block s through f against file d.
- ,W s Write in parallel to logical unit s all output.

Target system programs are developed using the Mostek resident assembler or Macro assembler and linked using the resident Linker. AIMZ80 is then used to complete debugging on the user's Target system.

ELECTRICAL SPECIFICATIONS

Operating Temperature Range 0°C to +50°C

Target Power Supply Requirements (typical)

+5V 5% @ 500mA

System Power Supply Requirements (typical)

+5V 5% @ 2.5A

+12V 5% @ 100mA

-12V 10% @ 10mA

Interface- MATRIX and SYS-80F compatible

Operating Frequency - 500KHz to 4MHz (Z80 PHI clock)

Target Interface - All signals meet the specifications for the MK3880-4 (Z80A CPU) with the following exceptions:

1. The output low voltage is 0.5 v max at 1.8 mA for the ADDRESS, DATA, IORQ, RFSH, HALT, and BUSAK signals.
2. The input low current is 400µa max for the PHI clock, RESET, INT, NMI, and DATA signals.
3. The input high current is 20µa max for the PHI clock, RESET, INT, NMI, and DATA signals.
4. The signals M1, MREQ, RD, and WR have a maximum of 25 ns added propagation delay.
5. The input signals RESET, INT, and NMI have a maximum of 45ns added propagation delay.

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO
AIM-Z80AE-16	Includes the AIM-Z80AE in circuit emulation control module, history module, buffer modules, cabling, operation manual and software on diskette. The emulation Control module is capable of simulating up to 16K bytes of Target memory.	MK78181-1
AIM-Z80AE-32	Same as AIM-Z80AE-16 but the emulation Control module is capable of simulating up to 32K bytes of Target memory.	MK78181-2
	AIM-Z80AE Operation manual only	MK79650

MICRO SYSTEMS DATA BOOK

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MOSTEK®

PERIPHERAL

CRT

MK78190-1, MK78190-2

FEATURES

- Interfaces directly to MATRIX™
- All 128 ASCII codes
- 32 displayable control codes (in monitor mode)
- Displays up to 96 characters, including lower case
- Keyboard layout similar to that of typewriter
- Separate 18 key numeric pad
- Switch-selectable inverse video
- Cursor addressing
- EIA interface
- Baud rates up to 9.6 KB
- Auxiliary unidirectional EIA output controlled by DC2 (on) and DC4 (off)
- 5 x 8 Dot Matrix

DESCRIPTION

The Mostek CRT is a high-performance, keyboard display unit that is fully compatible with the MATRIX™ microcomputer system.

The character set consists of 96 displayable upper and lower-case characters with lower-case descenders. The

CRT PHOTO



display may be switch-selected to be standard video (white on black) or reverse video (black on white).

The Mostek CRT can be interfaced to any computer system that provides a RS-232 serial asynchronous interface.

OPERATING CHARACTERISTICS

TERMINAL CONTROL

	Keyboard	Remote Command
CLEAR SCREEN	•	•
CLEAR TO END OF LINE	•	•
CLEAR TO END OF SCREEN	•	•
AUDIBLE ALARM	•	•
BACKSPACE	•	•
KEYBOARD LOCK		•
KEYBOARD UNLOCK		•
TAB		•
MONITOR MODE	•	•

CURSOR CONTROL

	Keyboard	Remote Command
CURSOR ADDRESS (XY)	•	•
INCREMENTAL CURSOR CONTROL	•	•
HOME CURSOR	•	•

SPECIFICATION

DISPLAY CHARACTERISTICS

Characters per line: 80
 Lines per display: 24
 Screen capacity: 1920 characters
 All 128 ASCII codes
 96 displayable characters including lower case
 32 displayable control codes

Character size: 5 x 8 dot matrix
 Refresh rate: 50/60 frames/sec
 Cursor: Block, Flashing Block, Underline, or Flashing Underline

INTERFACE

Full or Half Duplex (W.E. modem 103A compatible or W.E. Modem 202C/D using character turnaround).

EIA RS-232-C connector.

Eight Baud Rates: 110, 150, 300, 1200, 1800, 2400, 4800, 9600.

Parity: Odd, Even, 1, 0 or off

No. of Stop Bits: one (two at 110 Baud)

EXTERNAL CONTROLS

Auto Scroll
 Contrast
 Power On/Off
 Half Duplex/Full Duplex
 Auto LF/CR Control
 Reverse Video or Standard Video
 Upper/Lower Case
 Parity
 Baud rate
 EIA or Current Loop

ELECTRICAL

Power consumption: 60 watts, nominal
 Power input: 115 V, 60 Hz; 115 V, 50 Hz

MECHANICAL

Size (nominal): 15 in. (38 cm) high, 18.5 in. (47 cm) wide, 23.25 in. (59 cm) deep

Weight: 38 lbs. (17 kg)

ENVIRONMENTAL

Temperature: 10°C to 40°C
 Storage Temperature: 0°C to 85°C
 Humidity: 10 to 90% relative, non-condensing

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
CRT	Mostek CRT terminal featuring all 128 ASCII codes, 96 displayable characters including lower case, 80 characters by 24 lines, typewriter-like keyboard layout, cursor addressing, EIA interface and Baud rates to 9.6 K Baud. Includes RS-232 interface cable (MK78152).	MK78190-1
CRT-50	Same as above but for 50 Hz operation.	MK78190-2
SDE-RMC6 to CRT	CRT interface cable only.	MK78152
MD-232 DCE-C	CRT to MDX-SIO, MDX-DEBUG or MDX-EPROM/UART	MK77955

MOSTEK®

PERIPHERAL

Line Printer

MK78191-1, MK78191-2

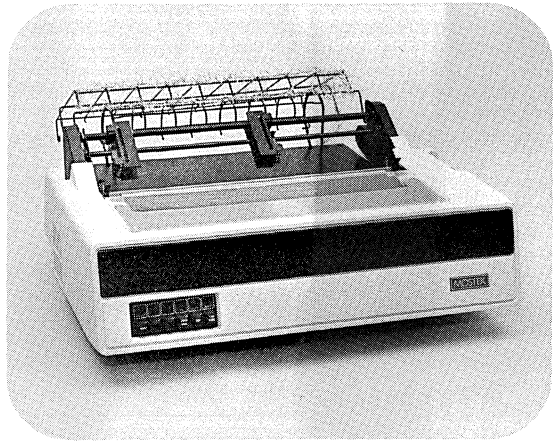
FEATURES

- Interfaces directly to MATRIX™
- Prints 120 characters per second
- Up to 132 characters per line
- Prints original plus five copies
- Character elongation
- Eight inches per second paper slew rate
- Ribbon cartridge
- 7x7 dot matrix, 64-character ASCII
- Tractor feed/Pin feed platen
- Parallel interface

DESCRIPTION

The Mostek line printer is a state-of-the-art microprocessor-controlled, dot matrix line printer that prints at the rate of 120 characters per second. The printer has a maximum print width of 132 characters with a horizontal format of ten characters per inch and six lines per inch vertical. Elongated

LINE PRINTER PHOTO



(double-width) characters are software-selectable.

The Mostek line printer interfaces directly to the MATRIX™ Microcomputer System and can be interfaced easily to other computer systems supporting parallel I/O.

SPECIFICATIONS

Print performance - Minimum throughput

Printer	Print Speed (cps)	Max Print	10Char/Line (lpm)	80Char/Line (lpm)	132Char/Line (lpm)
702	120	132...	200	74	47

Character

7x7 dot matrix

Format

Ten Characters per inch horizontal

Six Lines per inch vertical

Elongated (double-width) characters software-selectable

Forms Handling

Tractor feed, for rear or bottom feed forms

8 ips slew rate

Usable paper 4 in. (102 mm) to 17.3 in. (439 mm) width

Paper tension adjustment

Ribbon System

Ribbon cartridge

Continuous ribbon 9/16 in. (14 mm) wide, 20 yards (18.3 meters) long.

Mobius loop allows printing on upper and lower portion on alternate passes.

Panel Indicators

Power On: Indicates AC power is applied to printer.

Select: Indicates printer can receive data.

Alert: Indicates operator-correctable error condition.

Operator Controls

Select/deselect

Forms thickness

Top of form

Horizontal forms positioning

Vertical forms positioning

Power ON/OFF

Single line feed

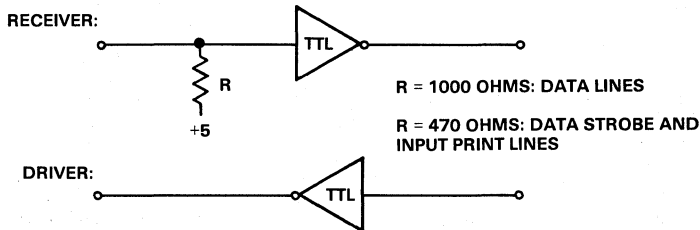
Paper empty override

Self-test

INTERFACE DRIVERS AND RECEIVERS

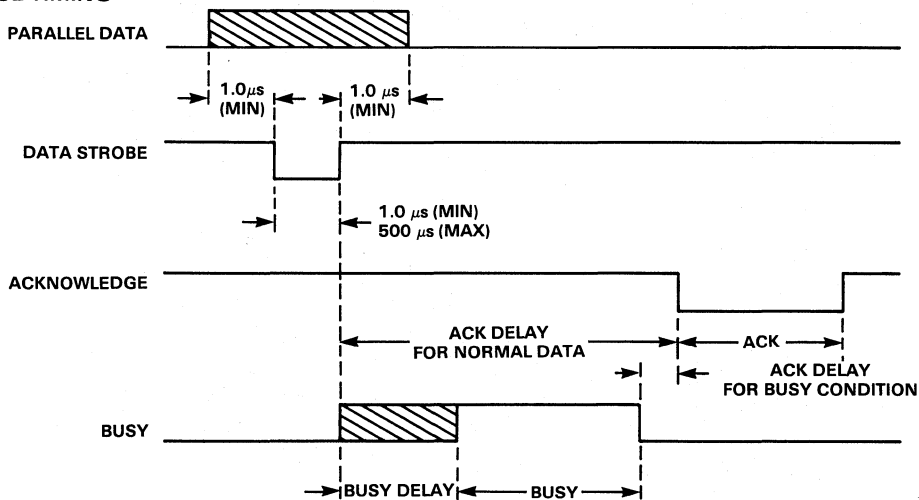
ALL INPUT/OUTPUT SIGNALS ARE TTL COMPATIBLE

LO: 0.4 VOLTS HI: 2.4 VOLTS



CONNECTOR: AMPHENOL 57 40360 SERIES, 36-PIN
(CENTRONICS 31310019)

INTERFACE TIMING



Internal Controls

Auto motor control: Turns stepping motors off when no data is received.

Electronic top of form: Allows paper to space to top of form when command is received.

Preset for 11 in. (279 mm) or 12 in. (305 mm) forms Opt. VFU must be used for other form lengths.

Data Input

7- or 8-bit ASCII parallel; microprocessor electronics; TTL levels with strobe.

Acknowledge pulse indicates that data was received.

INTERFACING**Electrical Requirements**

50/60 Hz, 115/230 VAC; -10%/-15% of Nominal
Tappable Transformer (100, 110, 115, 120, 200, 220, 230, 240 VAC).

Physical Dimensions**Model 702**

Weight: 60 lbs. (27 Kg)
Width: 24.5 in. (622 mm)
Height: 8 in. (203 mm)
Depth: 18 in. (457 mm)

Temperature

Operating: 40° to 100°F (4.4° to 37.7°C)
Storage: -10° to 160°F (-40° to 71.1°C)

Humidity

Operating: 20% to 90% (No condensation)
Storage: 5% to 95% (No condensation)

Normal Data Input Timing	ACK Delay ACK	2 - 6 μ sec 4 μ sec
BUSY CONDITION TIMING	BUSY DELAY	0 - 1.5 μ sec
	ACK DELAY	1 - 6 μ sec
	ACK	4 μ sec
	BUSY DURATION:	
	Line Feed	350 - 500 μ sec
	Vertical Tab (1-in.)	135 - 145 msec
	Form Feed (11-in.)	1.48 - 1.50 sec
	Delete	160 - 400 μ sec
	Bell	0
	Select*	0 - 1.5 μ sec
Deselect	Unit Printer is selected	
Printer	8.33 msec/char; plus 148 msec non-printing time/line	

*No busy if inhibit prime on select option is used.

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
LP	Mostek line printer featuring 120 cps operation, 7x7 dot matrix, 10 cpi, and paper slew rate of 8 ips. Includes MATRIX™ cable, 60 Hz operation.	MK78191-1
LP-50	Same as above but for 50 Hz operation.	MK78191-2
MD-CPRT-C	MATRIX System or MDX-PIO to Centronics Line Printer Interface cable.	MK79089

PPG 8/16-PROM Programmer

MK79181-1

FEATURES

- Programs, reads, and verifies 2708-, 2758-, and 2716-type PROMs (2758 and 2716 PROMS must be 5-Volt only type)
- Interfaces to MATRIX and MDX-PIO
- Driver software included on system diskette for FLP-80DOS
- Zero-insertion-force socket
- Power and programming indicators

DESCRIPTION

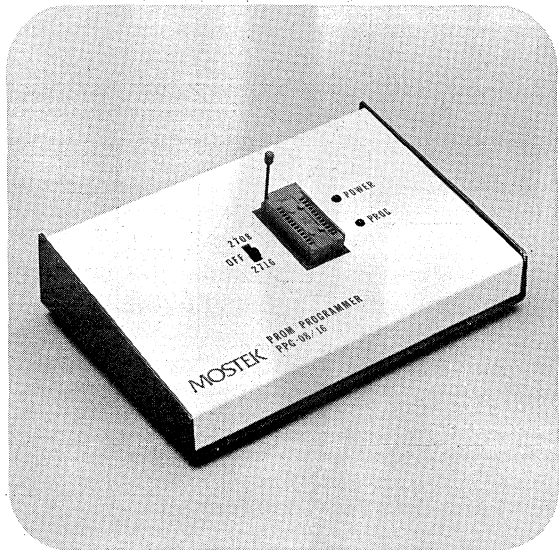
The PPG-8/16 PROM Programmer is a peripheral which provides a low-cost means of programming 2708, 2758, or 2716 PROMs. It is compatible with Mostek's MATRIX Microcomputer Development System and the MDX-PIO. The PPG-8/16 has a generalized computer interface (two 8-bit I/O ports) allowing it to be controlled by other types of host computers with user-generated driver software. A complete set of documentation is provided with the PPG-8/16 which describes the internal operation and details user's operating procedures

The PPG-8/16 is available in a metal enclosure for use with the MATRIX™ and the MDX-PIO. Interface cables for either the MATRIX or MDX-PIO must be purchased separately.

SOFTWARE DESCRIPTION

The driver software accomplishes four basic operations.

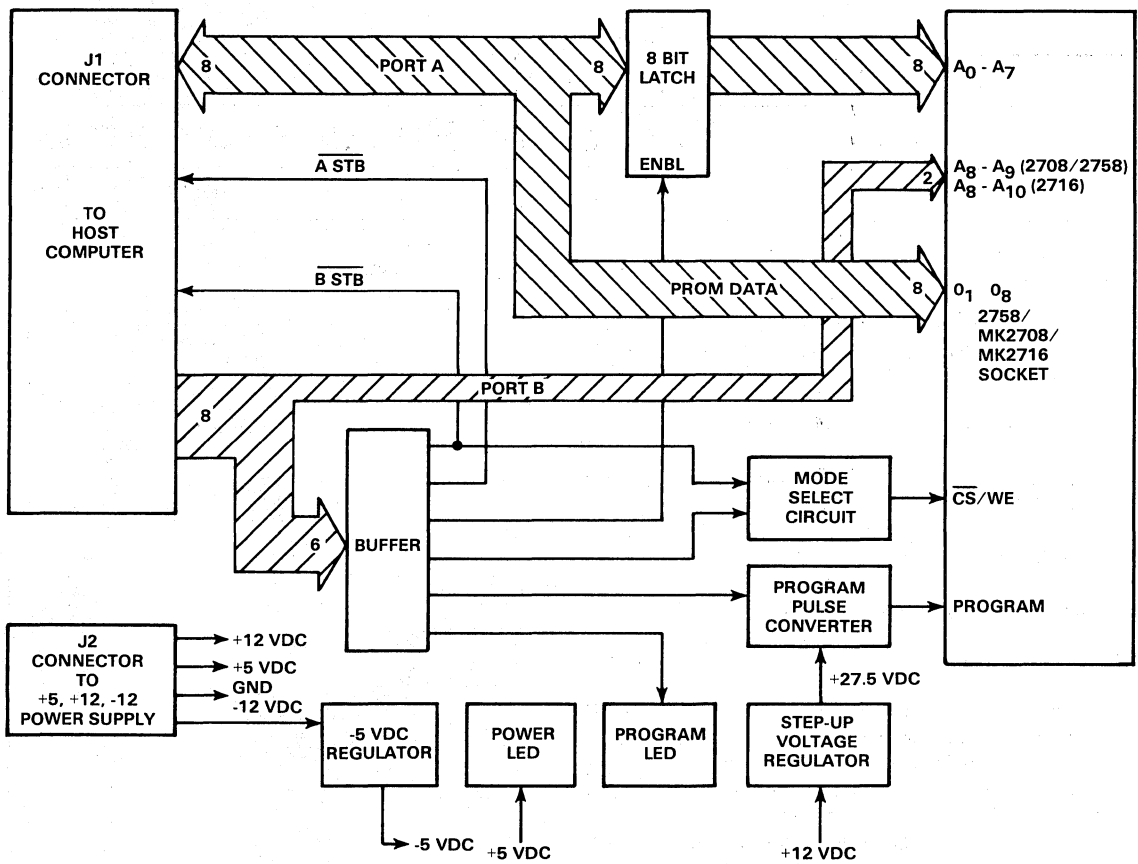
PPG 8/16 PHOTO



These are (1) loading data into host computer memory, (2) reading the contents of a PROM into host computer memory, (3) programming a PROM from the contents of the host computer memory, and (4) verifying the contents of a PROM with the contents of the host computer memory.

The driver software is provided on the FLP-80DOS system diskette. The user documentation provided with the PPG-8/16 fully explains programming procedures to enable a user to develop a software driver on a different host computer.

PPG8/16 BLOCK DIAGRAM



INTERFACE

25-pin control connector (D type)
 40-pin control connector (0.1-in. centers card edge)
 for AID-80F, SDB-80, SDB-50/70, or MATRIX™
 12-pin power connector (0.156-in. centers card edge)
 All control signals are TTL-compatible

POWER REQUIREMENTS

+12 VDC at 250mA typical
 +5 VDC at 100mA typical
 -12 VDC at 50mA typical

OPERATING TEMPERATURE

0°C -60°C

PROGRAMMING TIME

2708 - 2.5 minutes
 2758 - 0.9 minutes
 2716 - 1.8 minutes

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
PPG-8/16	PROM Programmer for 2708/2758/2716 PROMs with Operations Manual for interface with MATRIX.	MK79081-1
MATRIX to PPG-8/16	PPG-8/16 Interface Cable for MATRIX	MK79090
MD-PPG-C	PPG-8/16 Interface Cable for MDX-PIO	MK77957
	PPG-8/16 Operations Manual	MK79603

*NOTE: The PPG-8/16 will only program the 2708, 2758, and 2716 PROMs. The 2758 and 2716 are 5 Volt only type PROMs. THE PPG-8/16 WILL NOT PROGRAM THE TI2716 MULTIPLE-VOLTAGE 2K x 8 PROM.

MOSTEK®

PERIPHERAL

R MDFSS

MK78183, MK78185

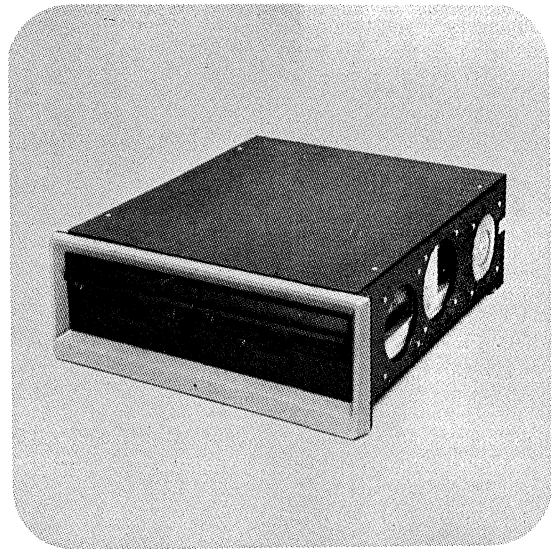
FEATURES

- Standard 19-inch rack-mountable chassis; 7-inch panel height
- Removable structural foam disk bezel for internal access
- Front panel POWER-ON indicator
- Mounts two standard 8-inch floppy disk drives
- Disks mounted horizontally for low profile
- Self-contained power supply and 115 CFM fan
- 100/115/230 Volt, 50/60 Hz operation

GENERAL DESCRIPTION

The Mostek R MDFSS offers a solution to rack mounting two standard 8-inch floppy disk drives. The system features a self-contained power supply designed to work on voltages and frequencies available worldwide. An attractive structural foam-front disk bezel is provided with a power-on indicator. The disk bezel is designed with quick-release ball studs so that it can be easily removed for access to the drives. The drives are mounted in a horizontal plane for a low-profile appearance and to conserve panel height in the rack. Drives and power supply may be removed individually

R MDFSS PHOTO



from front or top for ease of maintenance. The back panel has an I/O panel prepunched for one 50-pin "D" interface to the disk controller. AC components on the back panel include: On/Off switch, voltage selection switch, fuse holder (3AG or 5 x 20 mm) and AC input receptacle/line filter.

INPUT POWER100/115/230 Volts AC \pm 10% 50/60Hz**50Hz**
MK78185**60Hz**
MK78183**LINE CORD SUPPLIED****MK78183**
Similar to Belden
model
17205B**MK78185**
Similar to Feller
model
1100**DC POWER AVAILABLE**+5 VDC at 3.0A max.
-5 VDC at 0.5A max.
+24 VDC at 3.4A max.**LOAD REGULATION** \pm .05% for a 50% load change**OUTPUT RIPPLE**

3.0 mV PK-PK max.

TRANSIENT RESPONSE

30 microseconds for a 50% load change

SHORT CIRCUIT AND OVERLOAD PROTECTION

Automatic current limit/foldback

OVERVOLTAGE PROTECTION+5 Volt output set to 6.2 ± 0.4 Volts**STABILITY** \pm 0.3% for 24 hours after warmup**THERMAL PROTECTION**

Bi-metal thermostat on primary AC line set to cut out at 180°F (82°C)

DISK DRIVES

Shugart 800-2 or equivalent

FUSING

Line Voltage	MK78183	MK78185
110/115V	3 Amp 3AG*	3 Amp 5 x 20 mm
230 V	1.5 Amp 3AG	1.5 Amp 5 x 20mm*

*Configuration as shipped

FRONT PANEL INDICATOR

Power-on

REAR PANEL CONTROLSAC Power On/Off
AC fuse holder
AC line receptacle/filter
AC line voltage selector**WEIGHT**

50 lbs (22.7 kg)

OPERATING TEMPERATURE RANGE

0°C to 40°C (Disk Media Limitation)

DIMENSIONSHeight: 7.0 in. (17.8 cm) panel space
7.3 in. (18.5 cm) overall, includes feetWidth: 19.0 in. (48.3 cm) at front panel
17.5 in. (44.5 cm) behind front panelDepth: 21.1 in. (54.0 cm) with all protrusions
20.0 in. (50.8 cm) without foam front**HUMIDITY**

Up to 90% relative, noncondensing.

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
R MDFSS	Rack-mountable dual floppy enclosure with 8-inch drives for 100/115/230 Volt operation. Includes interface cable to SDE-RMC6 or MD-RMC12, front disk bezel, support bracket for rack mounting and Operations Manual. 60Hz model.	MK78183
R MDFSS-50	50 Hz model.	MK78185
	R MDFSS Operations Manual Only	MK79740

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