

MITSUBISHI 1987 SEMICONDUCTORS

HIGH SPEED CMOS LOGIC

DAIN BOOK



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GUIDANCE 1

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	M74HC253P/FP/DP	Dual 4-Input Data Selector/Multiplexer with 3-State Outputs		
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	M74HC354P/FP/DWP	8-Input Data Selector/Multiplexer with Data and Address Latches and with 3-State Outputs ···		
**	M74HC356P/FP/DWP	8-Input Data Selector/Multiplexer with Data and Address Latches and with 3-State Outputs \cdots		
	M74HC365P/FP/DP	Hex 3-State Noninverting Buffer with Common Enables		
	M74HC366P/FP/DP	Hex 3-State Inverting Buffer with Common Enables		
	M74HC367P/FP/DP	Hex 3-State Noninverting Buffer with Separate 2-Bit and 4-Bit Sections		
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	M74HC374P/FP/DWP	Octal 3-State Noninverting D-Type Flip-Flop		
	M74HC374-1P/FP/DWP	Octal 3-State Noninverting D-Type Flip-Flop ·····		
**	M74HCT374-1P/FP/DWP	Octal 3-State Noninverting D-Type Flip-Flop with LSTTL-Compatible Inputs	2	443
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××	M74HCT640-1P/FP/DWP	Octal 3-State Inverting Bus Transceiver with LSTTL-Compatible Inputs Octal 3-State Inverting and Noninverting Bus Transceiver	2	53/ E41
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	M74HC643-1P/FP/DWP			
××	M74HCT643-1P/FP/DWP	Octal 3-State Inverting and Noninverting Bus Transceiver with LSTTL-Compatible Inputs······ Octal 3-State Noninverting Bus Transceiver······		
	M74HC645P/FP/DWP	Octal 3-State Noninverting Bus Transceiver		
	M74HC645-1P/FP/DWP M74HCT645-1P/FP/DWP	Octal 3-State Noninverting Bus Transceiver with LSTTL-Compatible Inputs·····		
	M74HC646P/FP/DWP	Octal 3-State Noninverting Bus Transceiver with LSTTL-Compatible Inputs Octal 3-State Noninverting Bus Transceiver and D-Type Flip-Flop Octal 3-State Noninverting Bus Transceiver and D-Type Flip-Flop Octal 3-State Noninverting Bus Transceiver with LSTTL-Compatible Inputs	2	56F
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	M74HC670P/FP/DP	4-By-4 Register File with 3-State Outputs		
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M74HC4002P/FP/DP	Dual 4-Input Positive NOR Gate	2 -586
★★ M74HC4017P/FP/DP	Decade Counter/Divider	2 -589
★★ M74HC4020P/FP/DP	14-Stage Binary Ripple Counter·····	2 -595
★★ M74HC4022P/FP/DP	Octal Counter/Divider·····	2 599
M74HC4024P/FP/DP	7-Stage Binary Ripple Counter ······	2 -605
★★ M74HC4040P/FP/DP	12-Stage Binary Ripple Counter	
M74HC4049BP/FP/DP	Hex Inverting Buffer/Logic-Level Down Converter	2 613
M74HC4050BP/FP/DP	Hex Noninverting Buffer/Logic-Level Down Converter ·····	
★★ M74HC4051P/FP/DP	8-Channel Analog Multiplexer/Demultiplexer······	
★★ M74HC4052P/FP/DP	Dual 4-Channel Analog Multiplexer/Demultiplexer·····	
★★ M74HC4053P/FP/DP	Triple 2-Channel Analog Multiplexer/Demultiplexer	
M74HC4066P/FP/DP	Quadruple Analog Switch/Multiplexer/Demultiplexer with Enhanced ON-Resistance Linearity · · · · · · · · · · · · · · · · · · ·	
M74HC4075P/FP/DP	Triple 3-Input OR Gate ······	
M74HC4078P/FP/DP	8-Input Positive NOR/OR Gate ·····	
★★ M74HC4511P/FP/DP	BCD-to-Seven-Segment Latch/Decoder/Display Driver	2647
★★ M74HC4514P/FP/DWP	1-of-16 Decoder/Demultiplexer with Address Latch("H" Level Output)	
★★ M74HC4515P/FP/DWP	1-of-16 Decoder/Demultiplexer with Address Latch("L" Level Output)	
★★ M74HC4538P/FP/DP	Dual Precision Monostable Multivibrator(Retriggerable, Resettable)	
** M74HC4543P/FP/DP	BCD-to Seven-Segment Latch/Decoder/Display Driver for Liquid-Crystal Displays ······	

Note: M74HC266 is equivalent with 74HC7266 which other venders supply.

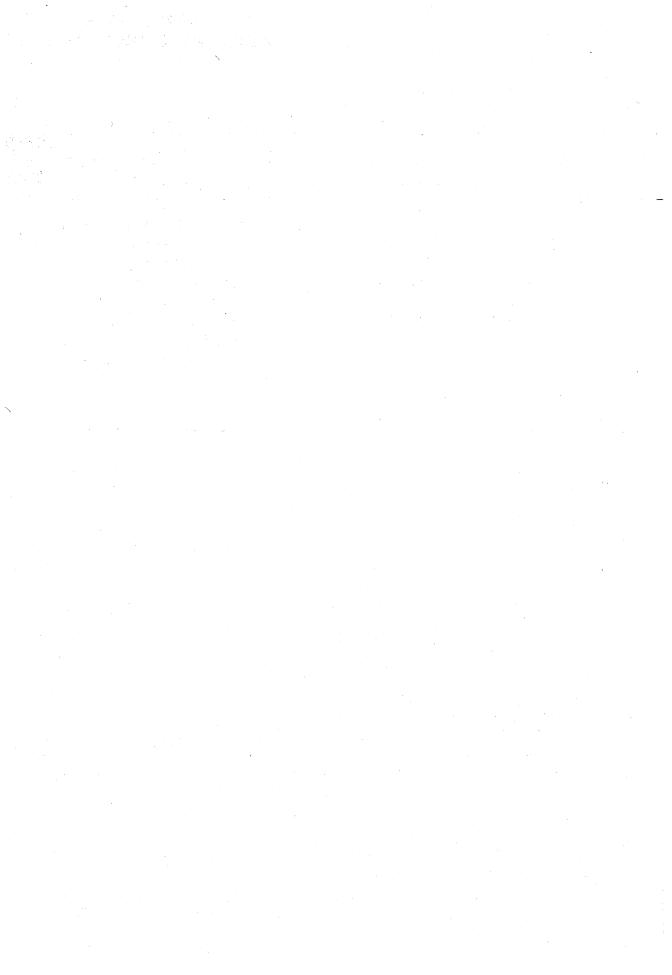
M74HC266A has an open-drain output and corresponds to the 74LS266.

M74HC266A is equivalent with other vender's 74HC266.



GUIDANCE

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MITSUBISHI HIGH SPEED CMOS INDEX BY FUNCTION

INDEX BY FUNCTION (★★: under development)

Conditions (Rated at V_{CC} =4.5V and T_a =-40~+85°C, Switching specifications apply at C_L =50pF)

INVERTERS

		Ε	lectrical cl	cs			
Туре	Description		Low- level output current (mA)	high-level output propagation	High-level to low-level output propagation time (ns)	Outline	Page
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M74HCU04FP	Hex Unbuffered Inverter	-4				14P2N	2 —18
M74HCU04DP						14P2P	
M74HC04P					24	14P4	2-15
M74HC04FP	Hex Inverter	-4	4	24		14P2N	
M74HC04DP						14P2P	
M74HCT04P ★★						14P4	
M74HCT04FP ★★	Hex Inverter with LSTTL-Compatible Inputs	-4	4	24	24	14P2N	2 21
M74HCT04DP★★				1		14P2P	
M74HC05P						14P4	2 —24
M74HC05FP	Hex Inverter with Open-Drain Outputs	-	— 4	29	21	14P2N	
M74HC05DP	•				1	14P2P	

NAND GATES

M74HC00P	·					14P4	
M74HC00FP	Quadruple 2-Input Positive NAND Gate	-4	4	23	23	14P2N	2 - 3
M74HC00DP						14P2P	
M74HCT00P	Ouadwinle 2 Innut Besitive NAND Cote with					14P4	
M74HCT00FP	Quadruple 2-Input Positive NAND Gate with	-4	4	24	24	14P2N	2 - 6
M74HCT00DP	LSTTL-Compatible Inputs]				14P2P	
M74HC03P	Overdrupte 2 Input Besitive NAND Cate with					14P4	
M74HC03FP	Quadruple 2-Input Positive NAND Gate with	-	4	32	32	14P2N	2 — 12
M74HC03DP	Open-Drain Outputs					14P2P	
M74HC10P		-4		24	24	14P4	
M74HC10FP	Triple 3-Input Positive NAND Gate		4			14P2N	2 — 33
M74HC10DP						14P2P	
M74HC20P				23		14P4	2 — 42
M74HC20FP	Dual 4-Input Positive NAND Gate	-4	1 4		23	14P2N	
M74HC20DP						14P2P	
M74HC30P						14P4	
M74HC30FP	8-Input Positive NAND Gate	-4	4	42	42	14P2N	2 - 49
M74HC30DP						14P2P	1
M74HC133P						16P4	2 —131
M74HC133FP	13-Input Positive NAND Gate	-4	-4 4	42	42	16P2N	
M74HC133DP					}	16P2P	

AND GATES

M74HC08P						14P4	
M74HC08FP	Quadruple 2-Input Positive AND Gate	-4	4	30	30	14P2N	2 27
M74HC08DP						14P2P	
M74HC09P	Overdening 2 Invest Desitive AND Octovith					14P4	
M74HC09FP	Quadruple 2-Input Positive AND Gate with	-	4	31	25	14P2N	2 30
M74HC09DP	Open-Drain Outputs					14P2P	
M74HC11P						14P4	
M74HC11FP	Triple 3-Input Positive AND Gate	-4	4	31	31	14P2N	2 36
M74HC11DP						14P2P	
M74HC21P ★★						14P4	
M74HC21FP ★★	Dual 4-Input Positive AND Gate	-4	4	26	26	14P2N	2 45
M74HC21DP ★★						14P2P]



NOR GATES

		E	lectrical cl	naracteristic	cs .	Outline	
Туре	Description	High- level output current (mA)	Low- level output current (mA)	high-level output propagation	High-level to low-level output propagation time (ns)		Page
M74HC02P						14P4	
M74HC02FP	Quadruple 2-Input Positive NOR Gate	-4	-4 4	23	23	14P2N	2 — 9
M74HC02DP						14P2P	
M74HC27P						14P4	
M74HC27FP	Triple 3-Input Positive NOR Gate	-4	4 23	23	23	14P2N	2 — 46
M74HC27DP				ì		14P2P	
M74HC4002P						14P4	
M74HC4002FP	Dual 4-Input Positive NOR Gate	-4	4	30	30	14P2N	2 -586
M74HC4002DP	·					14P2P	
M74HC4078P						14P4	
M74HC4078FP	8-Input Positive NOR/OR Gate	-4	4	33	33	14P2N	2 -643
M74HC4078DP						14P2P	

OR GATES

M74HC32P						14P4	
M74HC32FP	Quadruple 2-Input Positive OR Gate	-4	4	25	25	14P2N	2 — 52
M74HC32DP						14P2P	
M74HC4075P					29	14P4	2 —640
M74HC4075FP	Triple 3-Input OR Gate	-4	4	` 29		14P2N	
M74HC4075DP						14P2P	
M74HC4078P						14P4	2 —643
M74HC4078FP	8-Input Positive NOR/OR Gate	-4	4	33	33	14P2N	
M74HC4078DP						14P2P	

EXCLUSIVE OR GATES

M74HC86P						14P4	
M74HC86FP	Quadruple 2-Input Exclusive OR Gate	-4	4	30	30	14P2N	2 86
M74HC86DP	•					14P2P	

EXCLUSIVE NOR GATES

M74HC266P						14P4	
M74HC266FP	Quadruple 2-Input Exclusive NOR Gate	-4	4	30	30	14P2N	2 -365
M74HC266DP						14P2P	
M74HC266AP						14P4	
M74HC266AFP	Quadruple 2-Input Exclusive NOR Gate with	-	4	31	25	14P2N	2 -368
M74HC266ADP	Open-Drain Outputs					14P2P	

AND-OR-INVERTER GATES

1	M74HC51P	,					14P4	
	M74HC51FP	2-Wide, 2-Input/2-Wide, 3-Input AND-OR-INVERT Gates	-4	4	32	32	14P2N	2 59
-	M74HC51DP						14P2P	



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BUFFERS/LINE DRIVERS

		Ou	tput	E	lectrical c	naracteristi	cs		
Туре	Description	Two-state	Three-state	High- level output current (mA)	Low- level output current (mA)	Low-level to high-level output propagation time (ns)		Outline	Page
M74HC125P	Our double 2 Chate Naminus dina Duffer				_	OF.	25	14P4	2 120
M74HC125FP M74HC125DP	Quadruple 3-State Noninverting Buffer		NI	-6	6	25	25	14P2N 14P2P	2 —120
M74HC126P								14P4	
M74HC126FP	Quadruple 3-State Noninverting Buffer		NI	-6	6	25	25	14P2N	2 124
M74HC126DP								14P2P	
M74HC240P	Octol 2 State Investing Buffer/Line Driver							20P4	
M74HC240FP	Octal 3-State Inverting Buffer/Line Driver /Line Receiver		. 1	-6	6	25	25	20P2N	2 —273
M74HC240DWP	/Lille Receiver							20P2V	
M74HC240-1P	Octol 2 State Investing Buffor/Line Driver							20P4	
M74HC240-1FP	Octal 3-State Inverting Buffer/Line Driver		1	-24	24	19	19	20P2N	2 —277
M74HC240-1DWP	/Line Receiver		l					20P2V	
M74HCT240P	0-1-1-2-01-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1							20P4	
M74HCT240FP	Octal 3-State Inverting Buffer/Line Driver		1	-6	6	29	29	20P2N	2 —281
M74HCT240DWP	/Line Receiver with LSTTL-Compatible Inputs							20P2V	
M74HCT240-1P **								20P4	
M74HCT240-1FP ★★	Octal 3-State Inverting Buffer/Line Driver		1	-24	24	19	19	20P2N	2 - 285
M74HCT240-1DWP ★★	/Line Receiver with LSTTL-Compatible Inputs							20P2V	
M74HC241P		*****						20P4	
M74HC241FP	Octal 3-State Noninverting Buffer/Line Driver		NI	— 6	6	29	29	20P2N	2 —289
M74HC241DWP	/Line Receiver							20P2V	
M74HC241-1P	* g ₁₁							20P4	
M74HC241-1FP	Octal 3-State Noninverting Buffer/Line Driver		NI	-24	24	23	23	20P2N	2 293
M74HC241-1DWP	/Line Receiver							20P2V	
M74HCT241P					-			20P4	
M74HCT241FP	Octal 3-State Noninverting Buffer/Line Driver		NI	_ ₆	6	32	32	20P2N	2 —297
M74HCT241DWP	/Line Receiver with LSTTL-Compatible Inputs					02	02	20P2V	
M74HCT241-1P ★★								20P4	
M74HCT241-1FP ★★	Octal 3-State Noninverting Buffer/Line Driver		NI	-24	24	23	23	20P2N	2 —301
M74HCT241-1DWP ★★	/Line Receiver with LSTTL-Compatible Inputs							20P2V	
M74HC244P			_			<u> </u>		20P4	7.1
M74HC244FP	Octal 3-State Noninverting Buffer/Line Driver		NI ·	– 6	6	29	29	20P2N	2 —313
M74HC244DWP	/Line Receiver	· ·			1		2.0	20P2V	2 0.0
M74HC244-1P					-			20P4	
M74HC244-1FP	Octal 3-State Noninverting Buffer/Line Driver		NI	-24	24	23	23	20P2N	2 —317
M74HC244-1DWP	/Line Receiver	l i	1					20P2V	2 0.7
M74HCT244P						-		20P4	
M74HCT244FP	Octal 3-State Noninverting Buffer/Line Driver		NI	-6	6	32	32	20P2N	2 —321
M74HCT244DWP	/Line Receiver with LSTTL-Compatible Inputs		1					20P2V	
M74HCT244-1P **							-	20P4	
M74HCT244-1FP **	Octal 3-State Noninverting Buffer/Line Driver		NI	-24	24	23	23	20P2N	2 —325
M74HCT244-1DWP ★★	/Line Receiver with LSTTL-Compatible Inputs				-			20P2V	_ 52.5
M74HC365P			-					16P4	
M74HC365FP	Hex 3-State Noninverting Buffer with		NI	_ ₆	6	30	30	16P2N	2 —404
M74HC365DP	Common Enables				"	30	50	16P2P	54
M74HC366P			_		 	-		16P4	
M74HC366FP	Hex 3-State Inverter Buffer with			– 6	6	24	24	16P2N	2 -408
M74HC366DP	Common Enables			Ŭ				16P2P	50
M74HC367P								16P4	
M74HC367FP	Hex 3-State Noninverting Buffer with	ļ	NI	6	6	30	30	16P2N	2 -412
M74HC367DP	Separate 2-Bit and 4-Bit Sections	}	'"	"		30	30	16P2P	- 712
M74HC368P					-			16P4	
M74HC368FP	Hex 3-State Inverting Buffer with		1	_ ₆	6	24	24	16P2N	2 —416
M74HC368DP	Separate 2-Bit and 4-Bit Sections		'	6	0	24	24		2 -416
W/400308DP		L		L	1		L	16P2P	



BUFFERS/LINE DRIVERS (continued)

		Out	tput	E	lectrical cl	naracteristic	cs				
Туре	Description	Two-state	Three-state	High- level output current (mA)	Low- level output current (mA)	high-level output propagation	High-level to low-level output propagation time (ns)	Outline	Page		
M74HC540P	Ontol 2 State Invention Buffer/Line Datum							20P4			
M74HC540FP	Octal 3-State Inverting Buffer/Line Driver		ı	-6	6	25	25	20P2N	2 -490		
M74HC540DWP	/Line Receiver							20P2V			
, M74HC541P	0.112.011.11.11.11.11.11.11.11.11.11.11.11.11							20P4			
M74HC541FP	Octal 3-State Noninverting Buffer/Line Driver		NI	-6	6	29	29	20P2N	2 494		
M74HC541DWP	/Line Receiver							20P2V			
M74HC4049BP	the beautiful Butter to the second							16P4			
M74HC4049BFP	Hex Inverting Buffer/Logic-Level	1		6	6	20	19	16P2N	2 -613		
M74HC4049BDP	Down Converter		ĺ					16P2P			
M74HC4050BP	U. N. S.							16P4			
M74HC4050BFP	Hex Noninverting Buffer/Logic-Level	NI	NI	NI	Ì	-6	6	20	19	16P2N	2 -616
M74HC4050BDP	Down Converter							16P2P	1		

I: Inverting output NI: Noninverting output

BUS TRANSCEIVERS

M74HC242P							14P4	
M74HC242FP	Quadruple 3-State Inverting Bus Transceiver	l l	-6	.6	25	25	14P2N	2 305
M74HC242DP		_					14P2P	
M74HC243P							14P4	
M74HC243FP	Quadruple 3-State Noninverting Bus Transceiver	NI.	-6	6	25	25	14P2N	2 -309
M74HC243DP		·			L		14P2P	
M74HC245P			1				20P4	
M74HC245FP	Octal 3-State Noninverting Bus Transceiver	NI	6	6	28	28	20P2N	2 329
M74HC245DWP							20P2V	
M74HC245-1P ★★							20P4	
M74HC245-1FP ★★	Octal 3-State Noninverting Bus Transceiver	NI	-24	24	21	21	20P2N	2 -333
M74HC245-1DWP ★★							20P2V	
M74HCT245-1P ★★	Octal 3-State Noninverting Bus Transceiver						20P4	
M74HCT245-1FP ★★	with LSTTL-Compatible Inputs	NI	-24	24	21	21	20P2N	2 —337
M74HCT245-1DWP ★★	with EST L-Compatible inputs						20P2V	
M74HC640P							20P4	
M74HC640FP	Octal 3-State Inverting Bus Transceiver	1	-6	6	28	28	20P2N	2 -529
M74HC640DWP							20P2V	
M74HC640-1P ★★							20P4	
M74HC640-1FP ★★	Octal 3-State Inverting Bus Transceiver	1	-24	24	21	21	20P2N	2 -533
M74HC640-1DWP★★							20P2V	
M74HCT640P-1 ★★	Octal 3-State Inverting Bus Transceiver						20P4	
M74HCT640-1FP ★★	with LSTTL-Compatible Inputs	1	-24	24	21	21	20P2N	2 -537
M74HCT640-1DWP ★★	with ESTTE-Compatible inputs						20P2V	
M74HC643P	Octal 3-State Inverting and Noninverting			4.			20P4	
M74HC643FP	Bus Transceiver	NI, I	6	6	28	28	20P2N	2 -541
M74HC643DWP	Dus Transcorren	`			<u> </u>		20P2V	
M74HC643-1P ★★	Octal 3-State Inverting and Noninverting						20P4	
M74HC643-1FP ★★	Bus Transceiver	NI, I	-24	24	21	21	20P2N	2 -545
M74HC643-1DWP★★	Dus Transcores						20P2V	
M74HCT643-1P ★★	Octal 3-State Inverting and Noninverting Bus			1			20P4	
M74HCT643-1FP ★★	Transceiver with LSTTL-Compatible Inputs	NI,I	-24	24	21	21	20P2N	2 —549
M74HCT643-1DWP ★★	The control of the companion inputs						20P2V	
M74HC645P	·						20P4	
M74HC645FP	Octal 3-State Noninverting Bus Transceiver	NI	6	6	28	28	20P2N	2 -553
M74HC645DWP					L		20P2V	

BUFFERS/LINE DRIVERS (continued)

		Ou	tput	E	lectrical cl	naracteristi	cs		
Туре	Description	Two-state	Three-state	High- level output current (mA)	Low- level output current (mA)	high-level output propagation	High-level to low-level output propagation time (ns)	Outline	Page
M74HC645-1P ★★								20P4	,
M74HC645-1FP ★★	Octal 3-State Noninverting Bus Transceiver		NI -	-24	24	21	21	20P2N	2557
M74HC645-1DWP★★					ĺ			20P2V	:
M74HCT645-1P ★★	Ostal 2 State Meninyarting Bus Transacius							20P4	
M74HCT645-1FP ★★	Octal 3-State Noninverting Bus Transceiver	1	NI	-24	24	21	21	20P2N	2 -561
M74HCT645-1DWP ★★	with LSTTL-Compatible Inputs				Ì			20P2V	
M74HC646P ★★	Ostal 3 Ctata Maninusation Bus Transcrius and							24P4D	
M74HC646FP ★★	Octal 3-State Noninverting Bus Transceiver and	1	NI	6	6	43	43	24P2	2 565
M74HC646DWP ★★	D-Type Flip-Flop							24P2V	
M74HC648P ★★	Oatal 2 State Investing Bus Transacives and							24P4D	
M74HC648FP ★★	Octal 3-State Inverting Bus Transceiver and		1	6	6	43	43	24P2	2 572
M74HC648DWP ★★	D-Type Flip-Flop							24P2V	

I: Inverting output NI: Noninverting output

SCHMITT TRIGGERS

		E	lectrical ch	aracteristic	cs	-	
Туре	Description	going	Negative- going threshold voltage (V)	high-level output propagation	High-level to low-level output propagation time (ns)	Outline	Page
M74HC14P						14P4	,
M74HC14FP	Hex Schmitt-Trigger Inverter	1.55~3.15	0.9~2.45	31	31	14P2N	2 39
M74HC14DP					1	14P2P	
M74HC132P						14P4	
M74HC132FP	Quadruple 2-Input Schmitt-Trigger Positive NAND Gate	1.55~3.15	0.9~2.45	32	32	14P2N	2 128
M74HC132DP						14P2P	

J-K FLIP FLOPS

		Electric	al charact	eristics				ĺ.	
		Opera-	Setup	Hold	Trigger	L	te		_
Туре	Description	ting	time	time	Ę	Set	Reset	Outline	Page
		frequency (MHz)	(ns)	(ns)					
M74HC73P								14P4	
M74HC73FP	Dual J-K Flip-Flop with Reset	21	25	0	1	—	П	14P2N	2 - 62
M74HC73DP								14P2P	
M74HC76P								16P4	
M74HC76FP	Dual J-K Flip-Flop with Set and Reset	21	25	0	1	П	밉니	16P2N	2 — 76
M74HC76DP								16P2P	
M74HC107P								14P4	
M74HC107FP	Dual J-K Flip-Flop with Reset	21	25	0	↓	—	[]	14P2N	2 — 89
M74HC107DP					<u> </u>		14P2P		
M74HC109P	-							16P4	
M74HC109FP	Dual J-K Flip-Flop with Set and Reset	21	25	5	1	L	냅니	16P2N	2 - 94
M74HC109DP						<u></u>		16P2P	
M74HC112P						ł		16P4	l
M74HC112FP	Dual J-K Flip-Flop with Set and Reset	21	25	0	1] []	П	16P2N	2 — 99
M74HC112DP								16P2P	
M74HC113P	·				1			14P4	}
M74HC113FP	Dual J-K Flip-Flop with Set	21	25	0	1	П	_	14P2N	2 104
M74HC113DP								14P2P	
M74HC114P								14P4]
M74HC114FP	Dual J-K Flip-Flop with Set and Common Reset	21	25	0	1	L	П	14P2N	2 -109
M74HC114DP					l			14P2P	l

^{↑ :} Positive-going edge ↓ : Negative-going edge ∐ : Active low



D-TYPE FLIP FLOPS

		Electric	al charact	eristics					
	•	Opera-	Setup	Hold	_		ايدا		
Type	Description	ting	time	time	Trigger	Set	Reset	Outline	Page
		frequency			ļΈ		Œ		
	*	(MHz)	(ns)	(ns)					
M74HC74P		, ,						14P4	
M74HC74FP	Dual D-Type Flip-Flop with Set and Reset	21	25	0	†	П	П	14P2N	2 - 67
M74HC74DP								14P2P	
M74HC173P	Quadruple 3-State D-Type Flip-Flop with							16P4	
M74HC173FP	Common Clock and Reset	21	25	0	1	-	Л	16P2N	2 —225
M74HC173DP	Common Clock and Neset				1.			16P2P	
M74HC174P							1	16P4	
M74HC174FP	Hex D-Type Flip-Flop with Common Clock and Reset	21	25	5	1	-	П	16P2N	2 —230
M74HC174DP					1			16P2P	
M74HC175P	Overdrupte D Type Elip Elep with					1		16P4	
M74HC175FP	Quadruple D-Type Flip-Flop with	24	25	5	1		IJ	16P2N	2 -234
M74HC175DP	Common Clock and Reset,			ŀ				16P2P	
M74HC273P					1.			20P4	
M74HC273FP	Octal D-Type Flip-Flop with Common Clock and Reset	21	25	0	1	-	П	20P2N	2 —371
M74HC273DWP				İ				20P2V	
M74HC374P								20P4	
M74HC374FP	Octal 3-State Noninverting D-Type Flip-Flop	24	18	12	1	—	<u> </u> —	20P2N	2 —433
M74HC374DWP								20P2V	
M74HC374-1P **	V							20P4	
M74HC374-1FP ★★	Octal 3-State Noninverting D-Type Flip-Flop	26	13	6	t	_	l —	20P2N	2 - 438
M74HC374-1DWP ★★		ļ						20P2V	
M74HCT374-1P ★★	_							20P4	
M74HCT374-1FP ★★	Octal 3-State Noninverting D-Type Flip-Flop	26	13	6	1	_		20P2N	2 443
M74HCT374-1DWP ★★	with LSTTL-Compatible Inputs			1				20P2V	
M74HC377P ★★					1			20P4	,
M74HC377FP ★★	Octal D-Type Flip-Flop with Common Clock and Enable	_	<u>-</u>		1		l —	20P2N	2 -451
M74HC377DWP ★★						İ		20P2V	
M74HC534P					1	ļ		20P4	
M74HC534FP	Octal 3-State Inverting D-Type Flip-Flop	24	18	12	1		_	20P2N	2 - 476
M74HC534DWP	*				'			20P2V	1
M74HC534-1P ★★	,							20P4	
M74HC534-1FP ★★	Octal 3-State Inverting D-Type Flip-Flop	26	13	6	1	l —	-	20P2N	2 -481
M74HC534-1DWP ★★				1	'			20P2V	1
M74HCT534-1P ★★		l .			†	 	t	20P4	
M74HCT534-1FP ★★	Octal 3-State Inverting D-Type Flip-Flop	26	13	6	1	_		20P2N	2 - 486
M74HCT534-1DWP ★★	with LSTTL-Compatible Inputs				`			20P2V	
M74HC564P ★★								20P4	
M74HC564FP **	Octal 3-State Inverting D-Type Flip-Flop	24	25	0	1	_	_	20P2N	2 -503
M74HC564DWP **				•	'			20P2V	1 - 333
M74HC574P **		-			1	 	 	20P4	
M74HC574FP ★★	Octal 3-State Noninverting D-Type Flip-Flop	24	25	0	1		_	20P2N	2 -512
M74HC574DWP ★★	Total Country and Deligion in Priop				'			20P2V	
M74HC646P **					1-	-	 	24P4D	
M74HC646FP ★★	Octal 3-State Noninverting Bus Transceiver and	21	25	0	1		_	24P2	2 -565
M74HC646DWP ★★	D-Type Flip-Flop	-		"	1 '			24P2V	- 303
M74HC648P **		-			+	\vdash	+	24P4D	
M74HC648FP **	Octal 3-State Inverting Bus Transceiver and	21	25	0	1	_	_	24P4D 24P2	2 — 572
M74HC648DWP **	D-Type Flip-Flop	21	25	"	'	_	_	24P2 24P2V	2 -5/2
m/400048UWP **					1	1		24P2V	1

^{↑ :} Positive-going edge ☐ : Active low

SYNCHRONOUS BINARY COUNTERS

Туре	Description	Electrical characteristics Count frequency (MHz)	Trigger	Set	Reset	Outline	Page
M74HC161P		, , , , ,				16P4	
M74HC161FP	Presettable 4-Bit Binary Counter with Asynchronous Reset	21	1	S	∐(A)	16P2N	2 - 190
M74HC161DP						16P2P	
M74HC163P						16P4	let en
M74HC163FP	Presettable 4-Bit Binary Counter with Synchronous Reset	21	1	S]](S	16P2N	2 —202
M74HC163DP						16P2P	
M74HC191P ★★						16P4	
M74HC191FP ★★	Presettable 4-Bit Binary Up/Down Counter	_	†	A		16P2N	2 - 241
M74HC191DP **						16P2P	
M74HC193P ★★						16P4	
M74HC193FP ★★	Presettable 4-Bit Binary Up/Down Counter with Reset	14	Ť	A	∐(A)	16P2N	2 - 249
M74HC193DP ★★						16P2P	
M74HC669P **						16P4	
M74HC669FP ★★	Presettable 4-Bit Binary Up/Down Counter	_	†	S		16P2N	2 —579
M74HC669DP ★★				-		16P2P	

: Positive-going edge : Active high	U.	: Active low	(A) :	Asynchronous	S	Synchronous
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SYNCHRONOUS DECADE COUNTERS

M74HC160P						16P4	r
		-	1.1	_			
M74HC160FP	Presettable BCD Counter with Asynchronous Reset	21	1	S	Πæ	16P2N	2 — 184
M74HC160DP					1 '	16P2P	
M74HC162P						16P4	
M74HC162FP	Presettable BCD Counter with Synchronous Reset	21	 	S	∏(S)	16P2N	2 - 196
M74HC162DP						16P2P	
M74HC190P **	The Parising of the Parising o					16P4	
M74HC190FP ★★	Presettable BCD Up/Down Counter	_	1	A	-	16P2N	2 —239
M74HC190DP ★★						16P2P	
M74HC192P ★★						16P4	
M74HC192FP ★★	Presettable BCD Up/Down Counter with Reset	14	f ↓	(A)	Π®	16P2N	2 - 243
M74HC192DP ★★						16P2P	
M74HC4017P ★★						16P4	
M74HC4017FP ★★	★ Decade Counter/Divider	16	Note		Πæ	16P2N	2 -589
M74HC4017DP★★						16P2P	}

used with CP high.

OCTAL COUNTER/DIVIDERS

M74HC4022P **							16P4	
M74HC4022FP ★★	Octal Counter/Divider	16	ò	Note	—	П	16P2N	2 —599
M74HC4022DP★★				,			16P2P	

☐ : Active high

: Positive-going edge when the CLOCK pin is used with CE low, negative-going edge when the CLOCK ENABLE pin is used with CP high.

MONOSTABLE MULTIVIBRATORS

		Electrical characteristics	function	ē		
Туре	Description	Resistance/capacitance connected to control output pulse width	Retrigger fund	Reset function	Outline	Page
M74HC123P ★★					16P4	
M74HC123FP ★★	Dual Retriggerable Monostable Multivibrator	1~1MΩ/No limits			16P2N	2 -114
M74HC123DP★★					16P2P	
M74HC221P ★★					16P4	
M74HC221FP ★★	Dual Monostable Multivibrator	1~1MΩ/No limits			16P2N	2 - 265
M74HC221DP ★★					16P2P	
M74HC4538P ★★	B - I B				16P4	
M74HC4538FP ★★	Dual Precision Monostable Multivibrator	1~1MΩ/No limits	•	•	16P2N	2 -662
M74HC4538DP ★★	(Retriggerable, Resettable)	· ·			16P2P	



MITSUBISHI HIGH SPEED CMOS INDEX BY FUNCTION

LATCHES

		E	lectrical ch	aracteristic	cs				
Туре	Description	Low-level to high-level output propagation time (ns)	High-level to low-level output propagation time (ns)	Setup time (ns)	Hold time (ns)	Enable	Reset	Outline	Page
M74HC75P				(114)	(1.0)	 	ļ —	16P4	
M74HC75FP	Dual 2-Bit Transparent Latch	32	32	25	5	11 [l	16P2N	2 - 72
M74HC75DP					_	_		16P2P	
M74HC259P								16P4	
M74HC259FP	8-Bit Addressable Latch/1-of-8 Decoder	54	54	25	0	Ιл	lэr	16P2N	2 360
M74HC259DP					' '		16P2P		
M74HC279P **							T	16P4	
M74HC279FP ★★	Quadruple R-S Latch		_	_		l_		16P2N	2 —37
M74HC279DP **						}	}	16P2P	
M74HC354P **							<u> </u>	20P4	
M74HC354FP ★★	8-Input Data Selector/Multiplexer with Data and	59	59	13	5	П	-	20P2N	2 —39
M74HC354DWP **	Address Latches and with 3-State Outputs					_		20P2V	
M74HC356P **						1-	ļ	20P4	
M74HC356FP **	8-Input Data Selector/Multiplexer with Data and	63	63	10	5	1		20P2N	2 —398
M74HC356DWP **	Address Latches and with 3-State Outputs					'		20P2V	- 33
M74HC373P			·			 	+-	20P4	· ·
M74HC373FP	Octal 3-State Noninverting D-Type Transparent Latch	38	38	18	12	П	l_	20P2N	2 42
M74HC373DWP	Cotar o State Heliminorally D Type Halloparont Eastern		00	'	'-	_		20P2V	- "-
M74HC373-1P **	<u> </u>					+		20P4	
M74HC373-1FP **	Octal 3-State Noninverting D-Type Transparent Latch	25	25	13	6	П	l_	20P2N	2 —42
M74HC373-1DWP★★	Cotal 5-State Northing 5-Type Transparent Eaton	25	23	. '3	"			20P2V	
M74HCT373-1P ★★			1			+	 	20P4	
M74HCT373-1FP ★★	Octal 3-State Noninverting D-Type Transparent Latch	25	25	13	6	T		20P2N	2 —42
M74HCT373-1DWP ★★	with LSTTL-Compatible Inputs			"		_		20P2V	- "-
M74HC375P		<u> </u>				+	 	16P4	
M74HC375FP	Dual 2-Bit Transparent Latch	32	32	25	5	11	1	16P2N	2 —44
M74HC375DP	Duar 2- Sit Transparorit Eaton	52	32					16P2P	~ ''
M74HC533P		.				+	1	20P4	
M74HC533FP	Octal 3-State Inverting D-Type Transparent Latch	38	38	18	12	111		20P2N	2 —46
M74HC533DWP	Octal 3-State inverting D-Type Transparent Catch	30	30	'0	'2			20P2V	1 70
M74HC533-1P **						+		20P4	-
M74HC533-1FP ★★	Octal 3-State Inverting D-Type Transparent	25	25	13	6	1, ,	_	20P2N	2 - 46
M74HC533-1DWP★★	Cotal 5-State inverting D-Type Transparent	23	23	'3	"	П		20P2V	1 40
M74HCT533-1P ★★								20P2V	
M74HCT533-1FP ★★	Octal 3-State Inverting D-Type Transparent Latch	25	25	- 13	6	17 [20P4 20P2N	2 - 47
M74HCT533-1DWP ★★	with LSTTL-Compatible Inputs	25	25	13	"		_	20P2N	1 2 -4/
M74HC563P ★★		 	-		 	+	 	20P2V 20P4	-
M74HC563FP ★★	Octal 3-State Inverting D-Type Transparent Latch		20	10	6	1, ,		20P4 20P2N	2 —49
M74HC563DWP ★★	4	ch 28	ch 28 28	19	0	T	_	20P2N 20P2V	1 2 -48
		1	-			+	-		
M74HC573P **	Oatel 2 State Naningarting D Type Transparent Latel	Latch 28	00	19 6		1, ,		20P4	1 2 50
M74HC573FP **			Latch 28 28 1		П		20P2N	2 50	
M74HC573DWP ★★	<u> </u>							20P2V	L

 \sqcup : Active low \sqcap : Active high \uparrow : Positive-going edge

SHIFT REGISTERS

		Electrical			Mode										
Туре	Description	Clock frequency (MHz)	igger	Right shift	Left shift	Parallel load	Reset	Outline	Page						
M74HC164P	,						-	14P4							
M74HC164FP	8-Bit Serial-Input/Parallel-Output Shift Register	21	1	0	-		U	14P2N	2 208						
M74HC164DP								14P2P							
M74HC165P ★★								16P4							
M74HC165FP ★★	8-Bit Serial-or Parallel-Input/Serial-Output Shift Register	21	†	0		0	_	16P2N	2 213						
M74HC165DP★★					Ì	l		16P2P							
M74HC166P	8-Bit Serial-or Parallel-Input/Serial-Output Shift Register with							16P4							
M74HC166FP		25	1	0	1 —	\circ	П	16P2N	2 219						
M74HC166DP	Reset							16P2P							
M74HC194P								16P4							
M74HC194FP	4-Bit Bidirectional Universal Shift Register	24	Ţ	0	0	0	L	16P2N	2 255						
M74HC194DP	•							16P2P]						
M74HC195P								16P4							
M74HC195FP	4-Bit Universal Shift Register	24	t	1	†	1	Ť	t	t	0	<u> </u>	0	U	16P2N	2 - 260
M74HC195DP					ļ			16P2P							
M74HC299P **	O Dia Didica di anal Halinana I ObiA Danish							20P4							
M74HC299FP ★★	8-Bit Bidirectional Universal Shift Register with	20	t	0	0	0	П	20P2N	2 384						
M74HC299DWP ★★	3-State Parallel Outputs							20P2V							
M74HC323P ★★	O Dia Didius salamat their second Chiff Demissary with							20P4							
M74HC323FP ★★	8-Bit Bidirectional Universal Shift Register with	_	1	0	0	0	П	20P2N	2 391						
M74HC323DWP ★★	3-State Parallel Outputs			l	l			20P2V							
M74HC595P	9 Dis Ocalet Innus/Ocalet on Decellat Outras Obits D							16P4							
M74HC595FP	8-Bit Serial-Input/Serial-or Parallel-Output Shift Register with	21	t	0	-	—	U	16P2N	2 517						
M74HC595DP	Latched 3-State Outputs	-						16P2P]						
M74HC597P **	8-Bit Serial-or Parallel-Input Serial-Output Shift Posistor with			+-				16P4							
M74HC597FP ★★	8-Bit Serial-or Parallel-Input Serial-Output Shift Register with	21 †	1	0		0	IJ	16P2N	2 523						
M74HC597DP **	Input Latch							16P2P	1						

^{↑ :} Positive-going edge ☐ : Active low

BINARY RIPPLE COUNTERS

Туре	Description	Electrical characteristics Count frequency (MHz)	Trigger	Reset	Outline	Page
M74HC393P					14P4	
M74HC393FP	Dual 4-Stage Binary Ripple Counter	21	1	П	14P2N	2 457
M74HC393DP			İ		14P2P	
M74HC4020P ★★		16			16P4	
M74HC4020FP ★★	14-Stage Binary Ripple Counter		↓	П	16P2N	2 595
M74HC4020DP★★					16P2P	
M74HC4024P					14P4	
M74HC4024FP	7-Stage Binary Ripple Counter	21	1	Л	14P2N	2605
M74HC4024DP					14P2P	
M74HC4040P ★★					16P4	
M74HC4040FP ★★	12-Stage Binary Ripple Counter	16	ţ	Л	16P2N	2 609
M74HC4040DP **					16P2P	1

 $[\]downarrow$: Negative-going edge $\ \ \square$: Active high

ASYNCHRONOUS DECADE COUNTER

M74HC390P					16P4	
M74HC390FP	Dual 4-Stage Binary Ripple Counter with ÷2 and ÷5 Sections	21	ţ	Л	16P2N	2452
M74HC390DP					16P2P	

∴ Negative-going edge	Π	Ĺ:	Active	high
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ANALOG SWITCHES/MULTIPLEXERS

		Ele	ectrical charac	teristics		
Туре		"ON"	Propaga	ition time(ns)] _	_
Туре	Description	resistance, V _i =2.5V (Ω)	From Data input to output	From Control inhibit to output	Outline	Page
M74HC4051P ★★				,	16P4	
M74HC4051FP ★★	8-Channel Analog Multiplexer/Demultiplexer	215	15	93	16P2N	2 -619
M74HC4051DP★★					16P2P	1
M74HC4052P ★★		,			16P4	
M74HC4052FP ★★	Dual 4-Channel Analog Multiplexer/Demultiplexer	215	15	93	16P2N	2625
M74HC4052DP★★					16P2P	
M74HC4053P ★★					16P4	
M74HC4053FP ★★	Triple 2-Channel Analog Multiplexer/Demultiplexer	215	15	93	16P2N	2 -630
M74HC4053DP ★★		·			16P2P	1
M74HC4066P	0				14P4	
M74HC4066FP	Quad Analog Switch/Multiplexer/Demultiplexer with	215	13	29	14P2N	2635
M74HC4066DP	Enhanced ON-Resistance Linearity				14P2P	1

DATA SELECTORS/DIGITAL MULTIPLEXERS

			Elect	rical characte	ristics		
_		Output	Pro	pagation time	(ns)]	_
Туре	Description	type	Strobe inhibit to output	Select input to output	Data input to output	Outline	Page
M74HC151P						16P4	
M74HC151FP	8-Input Data Selector/Multiplexer	NI, I	35	63	49	16P2N	2 161
M74HC151DP		<u> </u>				16P2P	
M74HC153P						16P4	
M74HC153FP	Dual 4-Input Data Selector/Multiplexer	NI 24	44	35	16P2N	2 166	
M74HC153DP						16P2P	
M74HC157P						16P4	
M74HC157FP	Quadruple 2-Input Noninverting Data Selector/Multiplexer	NI	29	32	32	16P2N	2 —176
M74HC157DP						16P2P	
M74HC158P						16P4	
M74HC158FP	Quadruple 2-Input Inverting Data Selector/Multiplexer	1	29	32	32	16P2N	2 —180
M74HC158DP		L				16P2P	
M74HC251P						16P4	
M74HC251FP	8-Input Data Selector/Multiplexer with 3-State Outputs	3S, NI, I	NI, I 55	51	49	16P2N	2 —341
M74HC251DP						16P2P	
M74HC253P	Dual 4-Input Data Selector/Multiplexer with					16P4	
M74HC253FP	3-State Outputs	3S, NI	38	44	35	16P2N	2 —346
M74HC253DP	3-otate Outputs					16P2P	
M74HC257P	Quadruple 2-Input Data Selector/Multiplexer with					16P4	
M74HC257FP	3-State Outputs	3S, NI	38	25	25	16P2N	2 -351
M74HC257DP	5-Otate Outputs				1.	16P2P	
M74HC258P ★★	Quadruple 2-Input Data Selector/Multiplexer with					16P4	
M74HC258FP ★★	3-State Outputs	3S, I	38	25	- 25	16P2N	2 —356
M74HC258DP ★★	o oldico outputo					16P2P	
M74HC298P ★★	Quadruple 2-Input Data Selector/Multiplexer with					16P4	ŀ
M74HC298FP ★★	Output Latch	NI		_	. —	16P2N	2 —383
M74HC298DP ★★	Output Later	ļ .				16P2P	
M74HC354P ★★	8-Input Data Selector/Multiplexer with Data and					20P4	
M74HC354FP ★★	Address Latches and with 3-State Outputs	3S, NI, I	68	71	59	20P2N	2 —392
M74HC354DWP ★★						20P2V	
M74HC356P ★★	8-Input Data Selector/Multiplexer with Data and					20P4	
M74HC356FP ★★	Address Latches and with 3-State Outputs	3S, NI, I	41	71	63	20P2N	2 —398
M74HC356DWP ★★	Addition Edition and Willing-Otate Outputs					20P2V	

 $[\]textbf{I}: \textbf{Inverting output} \quad \textbf{NI}: \textbf{Noninverting output} \quad \textbf{3S}: \textbf{Three-state output}$



MITSUBISHI HIGH SPEED CMOS INDEX BY FUNCTION

DECODERS

		Elec	trical		
Туре	Description	Low-level to high-level output propagation time (ns)	High-level to	Outline	Page
M74HC42P				16P4	
M74HC42FP 1-of-1	0 Decoder	38	38	16P2N	2 55
M74HC42DP				16P2P	
M74HC137P				16P4	
M74HC137FP 1-of-8	Decoder/Demultiplexer with Address Latch	43	60	16P2N	2 —134
M74HC137DP	•			16P2P	
M74HC138P				16P4	
M74HC138FP 1-of-8	B Decoder/Demultiplexer	38	50	16P2N	2 -139
M74HC138DP			-	16P2P	
M74HCT138P **		-		16P4	
	Decoder/Demultiplexer with LSTTL-Compatible Inputs	38	50	16P2N	2 —144
M74HC138DP **	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2			16P2P	- '''
M74HC139P		-		16P4	
	1-of-4 Decoder/Demultiplexer	55	55	16P2N	2 148
M74HC139DP	1-01-4 Decoder Demaniplexer	33	33	16P2P	2 170
M74HC154P **		1,		24P4D	
	6 Decoder/Demultiplexer	42	42	24P2	2 —171
M74HC154DWP **	o Decoder/Demaniplexer	42	44	24P2V	2 1/1
M74HC155P				16P4	
	1 of 4 December/Demoultiplesses				2 —175
M74HC155DP	1-of-4 Decoder/Demultiplexer			16P2N 16P2P	2 - 1/3
M74HC193DF				16P2P	
	Deceder/Demolisimle van with Address Lately	59	47	16P2N	2 —267
M74HC237DP	B Decoder/Demultiplexer with Address Latch	59	47		2 - 267
M74HC237DF	ti	+		16P2P 16P4	
	Daniel (Daniel Walter)			16P2N	2 272
M74HC238DP **	B Decoder/Demultiplexer	_			2-212
				16P2P	
M74HC259P M74HC259FP 8-Bit	Address to Late 11 of 0 December			16P4	200
M74HC259DP	Addressable Latch/1-of-8 Decoder	54	54	16P2N	2 —360
		-		16P2P	
M74HC4511P ** BCD-1	Course Commont Lately (Decoder (Display Driver	151	151	16P4	2 647
	o-Seven-Segment Latch/Decoder/Display Driver	151	151	16P2N	2 —647
M74HC4511DWP **		ļ		16P2P	
M74HC4514P **	C. Danadau/Danadainlana mish Adduna Lasak (81181 L. C. C.)	- 50	,,	24P4D	0 050
	6 Decoder/Demultiplexer with Address Latch ("H" Level Output)	58	44	24P2	2652
M74HC4514DWP **		-		24P2V	
M74HC4515P **				24P4D	
	6 Decoder/Demultiplexer with Address Latch ("L" Level Output)	58	44	24P2	2 - 657
M74HC4515DWP **				24P2V	
M74HC4543P **		1		16P4	
	o-Seven-Segment Latch/Decoder/Display Driver for Liquid-Crystal Displays	96 ,	96	16P2N	2665
M74HC4543DP ★★				16P2P	

DISPLAYED CHARACTERS

M74HC4511P, M74HC4511FP, M74HC4543P, M74HC4543FP

Decimal value	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Display	0	1	2	3	Ţ	S	Ь	7	8	9	·			-		-



ENCODERS

		Elec charac	trical teristics		
Туре	Description	Low-level to high-level output propagation time (ns)	output propagation	Outline	Page
M74HC147P				16P4	
M74HC147FP	10-Line Decimal to 4-Line BCD Priority Encoder	38	38	16P2N	2 152
M74HC147DP		ļ		16P2P	
M74HC148P				16P4	
M74HC148FP	8-Line to 3-Line Priority Encoder	38	38	16P2N	2 156
M74HC148DP				16P2P	

COMPARATORS

M74HC85P				16P4	
M74HC85FP	4-Bit Magnitude Comparator	58	58	16P2N	2 — 81
M74HC85DP				16P2P	1
M74HC688P				20P4	
M74HC688FP	8-Bit Equality Comparator	53	53	20P2N	2 582
M74HC688DWP				20P2V	1

FULL ADDERS

M74HC283P				16P4	\neg
M74HC283FP	4-Bit Binary Full Adder with Fast Carry	51	51	16P2N 2 -	-379
M74HC283DP				16P2P	

PARITY GENERATOR/CHECKERS

M74HC280P				14P4	
M74HC280FP	9-Bit Odd/Even Parity Generator/Checker	52	52	14P2N	2 —376
M74HC280DP				14P2P	1.5

REGISTER FILES

ſ	M74HC670P ★★				16P4	
ſ	M74HC670FP ★★	4-By-4 Register File with 3-State Outputs	_	. —	16P2N	2 581
Γ	M74HC670DP ★★				16P2P	



MITSUBISHI HIGH SPEED CMOS SYMBOLOGY

SYMBOLOGY

Symbol		Discription
Cı	Input capacitance	The output capafitance at input terminals
CL	Load capacitance	Extenally connected output capacitance
Co	Output disable capacitance	The output capacitance when the output is in the high-impedance state
C _{PD}	Power dissipation capacitance	The internal capacitance of the IC calculated from the power dissipation
C _x	External timing capacitance	The capacitance connected to set the pulse width of monostable multivibrators
fı	Input frequency	The sine wave frequency applied to the input terminal.
fmax	Maximum repetition frequency	The maximum frequency of repetitive inputs at which the device operates normally
GND	Ground	,
Н	High level	Used as a suffix for current and voltage parameters to indicate the high logic level
1	Current or input	Currents flowing into the IC are positive; currents flowing out of the IC are negative
Icc	Supply current	The current flowing into the IC at the V _{CC} pin
IDD	Supply current	The current flowing into the IC at the V _{DD} pin
I _I	Input current	The current that flows into the IC when an input voltage is applied
l _{IH}	High-level input current	The input current for a high-level input
I _{IL}	Low-level input current	The input current for a low-level input
I _O	Output current	Currents flowing into the IC are positive; currents flowing out of the IC are negative
_	Input off-state leak current	
I _{OFF}	· ·	The leakage between the input and output terminals of an analog switch in the off state Output load current in the high-level output state
I _{ОН}	High-level output curent Low-level output current	
l _{oL}	Off-state high-level output current	Output load current in the low-level output state
I _{OZH}		Output current when logic high is applied to an output in the high-impedance state
lozL	Off-state low-level output current	Output current when logic low is applied to an output in the high-impedance state
L	Low level	Used as a suffix for current and voltage parameters to indicate the low logic level
0	Output	Indicates output
P _d	Power dissipation	The product of the supply voltage and supply current
R _i	Input resistance	External resistance connected at input
R _L	Load resistance	External load resistance
R _{OFF}	Analog switch off resistance	The DC resistance of an analog switch in the off state
Ron	Analog switch on resistance	The DC resistance of an analog switch in the on state
R _×	External timing resistance	The resistance connected to set the pulse width of monostable multivibrators
T _a	Ambient temperature	The air temperature in the vicinity of the IC
t _f	Fall time	The period for an input pulse to change from logic high to low
th —	Hold time	The period other specified inputs must be held after a single specified input is changed
Topr	Operating (ambient) temperatuer	The ambient temperature range over which the IC will operate correctly
^t pd	Propagation delay time	The average period from when the specified input is applied until the specified output changes
t _{PHL}	High-level to low-level output propaga-	The period required for the output to change from logic high to low after the specified input is applied
t_{PHZ}	Output disable time from high-level	The period required for the output to change from logic high to the high-impedance state
t _{PLH}	Low-level to high-level output prop-	after the specified input is applied The period required for the output to change from logic low to high after the specified input
-PLH	agation time	is applied
t _{PLZ}	Output disable time from low-level	The period required for the output to change from logic low to the high-impedance state after the specified input is applied
t _{PZH}	Output enable time to high-level	The period required for the output to change from the high-impedance state to logic high after the specified input is applied
t _{PZL}	Output enable time to low-level	The period required for the output to change from the high-impedance state to logic low after the specified input is applied
t _r .	Rise time	The period for an input pulse to change from logic low to high
t _{rec}	Recovery time	The period required from when the input state is released until the next clock pulse can be
,		applied
T _{stg}	Storage temperature	The temperature range over which the IC can be safely stored



Symbol		Discription
t _{su}	Setup time	The period that other specified inputs must be held before the specified input can be applied
t _{THL}	High-level to low-level output transition time	The time required for the output to fall after the specified input is applied
t _{TLH}	Low-level to high-level output transition time	The time required for the output to fall after the specified input is applied
tw	Pulse width	The period over which a pulse remains within the reference voltage range
two	Output pulse width	The pulse width at the output of a monostable multivibrator
Vcc	Supply voltage	The voltage applied at the V _{CC} pin
V_{DD}	Supply voltage	The voltage applied at the V _{DD} pin
VEE	Supply voltage	The voltage applied at the V _{EE} pin
V _H	Hysteresis voltage	The difference between the Positive-going and Negative going threshold voltages of a Schmitt trigger circuit
V_1	Input voltage	The voltage applied to an input
ViH	High-level input voltage	The logic high voltage applied to an input
VIL	Low-level input voltage	The logic low voltages applied to an input
Vo	Output voltage	The voltage applied to or appearing at an output
V _{OH}	High-level output voltage	The voltage at the ouptut in the high-level state.
VoL	Low-level output voltage	The voltage at the output in the low-level state
Vss	Supply voltage	The voltage applied at the V _{SS} pin
V _T	Threshold voltage	When an input crosses this voltage level, the output state changes
V _{T+}	Positive-going threshold voltage	The threshold voltage for the low-to-high state change
V_{T-}	Negative-going threshold voltage	The threshold voltage for the high-to low state change
Z	High-impedance state	Indicates an output in the high-impedance state

MITSUBISHI HIGH SPEED CMOS INTRODUCTION

INTRODUCTION

The Mitsubishi M74HC series high-speed CMOS devices provide the high-speed operation and high-current drive capacity of bipolar LSTTL while retaining the low power consumption and other advantages of CMOS devices.

The M74HC series devices satisfy JEDEC Standard No. 7.

The M74HC series devices satisfy JEDEC Standard No. 7, and provide the following advatages over LSTTL devices:

- Low power dissipation: P_d=5µW/package, max.
 (V_{CC}=5V, T_a=25°C, quiesent state)
- High noise margin: 30% of V_{CC}, min. (V_{CC}=4.5V, 6V)
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=-40~+80°C
- Low input current: $|I_1| \le 1\mu A$, max.

These characteristics make the series ideally suited to applications in both industrial and consumer digital equipment.

Ratings

The M74HC series is available in three types: the HC type with waveform-regenerator buffered outputs, the unbuffered HCU type, and the HCT type with TTL-level inputs. JEDEC standards have been adopted for all three types. Table 1 shows the JEDEC absolute maximum ratings, Table 2 the recommended operating conditions, and Tables 3 and 4, the electrical characteristics. Tables 5~8 show the corresponding data for Mitsubishi M74HC series.

The characteristics of the Schmitt triggers, open drain outputs, and analog switches do vary somewhat from the JEDEC standards. For detailed information on these differences, please check the individual data sheets of the device in question.

Table 1 JEDEC 74C/HCU/HCT Series Absolute Maximum Ratings

Symbol	Parameter	Туре	Conditions	Ratings	Unit
Vcc	Supply voltage			−0.5~+7.0	V
V _I	Input voltage			-0.5~V _{cc} +0.5	V
V _o	Output voltage			-0.5~V _{cc} +0.5	V
	1-1-1-1-1-1		V ₁ < 0V	-20	
IIK	Input protection diode current		V _I > V _{CC}	20	mA
			V ₀ < 0V	-20	T
lok	Output parasitic diode current		Vo > Vcc	20	mA
		Standard		±25	
lo	Output current	Buffered		±35	mA ·
	0 1 (0)10	Standard	V OND	±50	
lcc	Supply/GND current	Buffered	V _{CC} , GND	±70	m'A
Tstg	Storage temperature range			-65~+150	°C

Table 2 JEDEC 74HC/HCT Series Recomended Operating Conditions

Comple ed	D		T				
Symbol	Paramet	er	Type	Min	Тур	Max	Unit
.,	0		HC/HCU	2		6	.,
Vcc	Supply voltage		HCT	4.5		5.5	V
Vı	Input voltage			0		Vcc	V
Vo	Output voltage	Output voltage				V _{cc}	٧
Topr	Operating temperature ra	inge		-40		+85	ဗ
		V _{CC} = 2.0V		0		1000	
		$V_{CC} = 4.5V$	нс	0		500	
t _r , t _f	Input risetime, falltime	V _{CC} = 6.0V		0		400	ns
			HCT	. 0		500	

Table 3 JEDEC 74HC/HCU Series Electrical characteristics

	1.							Limits			
Symbol	Parameter	Type	Test	conditions			25℃		-40~	+85℃	Uni
·					V _{cc} (V)	Min	Тур	Max	Min	Max	
					2.0	1.5			1.5		
		HC			4.5	3. 15		{	3.15		
	111-5 1 1		$V_0 = 0.1V, V_0$	c-0.1V	6.0	4.2			4.2		
/н	High-level input voltage		$ I_0 = 20 \mu A$		2.0	1.7			1.7		٧
	.[HCU			4.5	3.6		1	3.6		
					6.0	4.8			4.8		
					2.0			0.3		0.3	
		HC	1		4.5	. 1		0.9		0.9	
_			$V_0 = 0.1V, V_C$	c-0.1V	6.0			1.2		1.2	
/ _{IL}	Low-level input voltage		$ I_0 = 20\mu A$	-	2.0			0.3		0.3	
		HCU			4.5	ĺ		0.8		0.8	
					6.0			1.1		1.1	
	† 		 	$I_{OH} = -20\mu A$	2.0	1.9			1.9		
	'			$I_{OH} = -20\mu A$	4.5	4.4		ļ ļ	4.4	ļ.	
		HC	$V_1 = V_{1H}, V_{1L}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		
		Standard	VI — VIH, VIL		4.5	3.98		 	3.84		
			-	$I_{OH} = -4.0 \text{mA}$	1	1		1		1	
				$I_{OH} = -5.2 \text{mA}$	6.0	5.48			5.34		
				$I_{OH} = -20\mu A$	2.0	1.9		li	1.9		
_		HC		$I_{OH} = -20\mu A$	4.5	4.4			4. 4		
′он	High-level output voltage	Buffered	$V_i = V_{iH}, \ V_{iL}$	$I_{OH} = -20\mu A$	6.0	5. 9			5.9		· V
				$I_{OH} = -6.0 \text{mA}$	4.5	3.98			3. 84	l i	
				$I_{OH} = -7.8 \text{mA}$	6.0	5. 48			5. 34		
				$I_{OH} = -20\mu A$	2.0	1.8		1	1.8))	
			V _I = V _{IL}	$I_{OH} = -20\mu A$	4.5	4.0			4.0		
		HCU		$I_{OH} = -20\mu A$	6.0	5.5			5.5		
			V _I = GND	$I_{OH} = -4.0 \text{mA}$	4.5	3. 86			3.76		
			VI - GND	$I_{OH} = -5.2 \text{mA}$	6.0	5.36			5. 26	Ì	
				$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
				$I_{OL} = 20 \mu A$	4.5			0.1		0.1	
		HC	$V_{i} = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	
	,	Standard		I _{OL} = 4.0mA	4.5			0.26		0. 33	
				I _{OL} = 5. 2mA	6.0	ļ.		0. 26	,	0.33	
				$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
			Ì	$I_{OL} = 20 \mu A$	4.5			0.1		0.1	
OL	Low-level output voltage	HC	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
OL	2011 TOTOL Suspen Totago	Buffered		1 _{OL} = 6. 0mA	4.5		<u> </u>	0.26		0.33	•
				I _{OL} = 7.8mA	6.0			0.26		0.33	
				$I_{OL} = 20\mu A$	2.0			0.20		0.33	
			l.,,		1			1	,	1	
		uou	$V_i = V_{iH}$	$I_{OL} = 20 \mu A$	4.5			0.5		0.5	
	1	HCU	<u> </u>	$I_{OL} = 20 \mu A$	6.0			0.5	<u> </u>	0.5	
			$V_i = V_{CC}$	I _{OL} = 4.0mA	4.5			0.32		0.37	
		· ·		I _{OL} = 5. 2mA	6.0	-		0.32		0.37	 -
:Н -	High-level input current		V ₁ = 6V		6.0	<u></u>		0.1		1.0	μΙ
IL	Low-level input current		V ₁ = 0V		6.0			-0.1		-1.0	μΙ
OZH	Off-state high-level output current		$V_i = V_{iH}, \ V_{iL},$		6.0	ļ		0.5	ļ	5.0	μΙ
OZL	Off-state low-level output current		$V_{l} = V_{lH}, V_{lL},$	Vo = GND	6.0			-0.5		-5.0	μΙ
		Gate	Į					2.0		20.0	
cc	Quiescent supply current	F/F	$V_i = V_{CC}$, GNI	$0, I_0 = 0 \mu A$	6.0			4.0		40.0	μ
	()	MSI	1		1	1	1	8.0	1 ~	80.0	



Table 4 JEDEC 74HCT Serieis Electrical Characteristics

								Limits			
Symbol	Parameter	Туре	Test	conditions			25℃		~40~	+85°C	Unit
			V _{cc} (V)		Min	Тур	Max	Min	Max		
V _{IH}	High-level input voltage		$V_0 = 0.1V, V_0$ $ I_0 = 20\mu A$	$V_0 = 0.1V$, $V_{CC} = 0.1V$ $I_0 = 20\mu A$		2. 0			2, 0		>
VIL	Low-level input voltage		$V_0 = 0.1V, V_{CO}$ $ I_0 = 20\mu A$	$V_0 = 0.1V$, $V_{CC} - 0.1V$ $I_0 = 20\mu A$				0.8		0.8	v
		Standard	VI = VIH, VIL	$I_{OH} = -20\mu A$ $I_{OH} = -4.0 \text{mA}$	4.5	4. 4 3. 98			4. 4 3. 84		
V _{OH}	High-level output voltage	Buffered V _i = V _{IH} , V _{IL}	$I_{OH} = -20\mu A$	4.5	4. 4			4.4		V	
				$I_{OH} = -6.0 \text{mA}$ $I_{OL} = 20 \mu \text{A}$	4.5	3, 98		0. 1	3.84	0. 1	
		Standard	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 4.0 \text{mA}$	4.5			0. 7		0.33	
VoL	Low-level output voltage	Buffered	$V_{l} = V_{lH}, V_{lL}$	$I_{OL} = 20 \mu A$ $I_{OL} = 6.0 mA$	4.5	_		0. 26		0. 33	٧
I _{IH}	High-level input current		V ₁ = 5.5V	100	5.5			0.1		1.0	μΑ
I _{IL}	Low-level input current		V ₁ = 0V		5.5			-0.1		-1.0	μΑ
l _{ozh}	Off-state high-level output current		$V_i = V_{iH}, V_{iL},$	$v_0 = v_{cc}$	5.5			0.5		5.0	μA
lozL	Off-state low-level output current		$V_{i} = V_{iH}, V_{iL},$	Vo = GND	5.5			-0.5		-5.0	μΑ
		Gate						2.0		20.0	
lcc	Quiescent supply current	F/F	VI = VCC, GNE	$I_0 = 0\mu A$	5.5			4.0		40.0	μΑ
	MSI	<u> </u>				8.0		80.0			
Δlcc	Maximum quiescent supply current		V ₁ = 2.4V (Note	e 1)	5.5			2.7		2.9	mA

Note 1: Only one input is set at this value and all other inputs are fixed at V_{CC} or GND.

Table 5 Mitsubishi M74HC/HCU/HCT Series Absolute Maximum Ratings

Symbol	Parameter	Туре	Conditions	Ratings	Unit
Vcc	Supply voltage			-0.5~+7.0	V
V _I	Input voltage			-0.5~V _{cc} +0.5	V
Vo	Output voltage			-0.5~V _{cc} +0.5	V
			V ₁ < 0V	-20	
İıK	Input protection diode current		V _I > V _{CC}	20	mA
			V ₀ < 0V	-20	
lok	Output parasitic diode current	l	Vo > Vcc	20	mA
		Standard		±25	
lo	Output current	Buffered		±35	mA
		Standard		±50	
Icc	Supply/GND current	Buffered	V _{CC} , GND	土75	mA
Pd	Power dissipation			500	mV
Tstg	Storage temperature range			−65∼+150	င

Table 6 Mitsubishi M74HC/HCU/HCT Series Recommended Operating Conditions

Charach al	Davamat		Туре		Unit		
Symbol	Paramet	Parameter			Тур	Max	Unit
	0		HC/HCU	2		6	v
Vcc	Supply voltage		HCT	4.5		5.5	\ \
Vı	Input voltage			0		Vcc	٧
Vo	Output voltage		0		V _{cc}	٧	
Topr	Operating temperature ra	inge		40		+85	ొ
		V _{CC} = 2.0V		0		1000	
		$V_{CC} = 4.5V$	нс	0		500	
t _r , t _f	Input risetime, falltime	$V_{CC} = 6.0V$		0		400	ns
			HCT	0		500	
			HCU		No	limit	

Table 7 Mitsubishi M74HC/HCU/HCT Series Electrical Characteristics (Ta=-40~+80°C)

		_						Limits			
Symbol	Parameter	Туре	Test	conditions			25℃		-40~	+85℃	Uni
	·				V _{CC} (V)	Min	Тур	Max	Min	Max	
			$V_0 = 0.1V, V_{CC}$	-0.1V	2.0	1.5			1.5		
	,	HC	$ I_0 = 20\mu A$	0.19	4.5	3.15))	3. 15		
	Illah I I I I I		1101 - 20AA		6.0	4.2		1 1	4.2		v
∕ıн	High-level input voltage		$V_0 = 0.2V, I_0 $	= 20µA	2.0	1.7			1.7		. •
		HCU	$V_0 = 0.5V, I_0$	$=20\mu A$	4.5	3.6		{	3.6		
*			$V_0 = 0.5V, I_0$	$ = 20 \mu A$	6.0	4.8			4.8		
					2.0			0.5		0.5	1
		HC .	$V_0 = 0.1V$, V_{CC}	-0.17	4.5			1.35		1.35	
			$ I_0 = 20\mu A$		6.0			1.8		1.8	
/ _{IL}	Low-level input voltage		$V_0 = V_{CC} - 0.2V$	$ = 20 \mu A$	2.0	-		0.3		0.3	V
		HCU	$V_{\rm o} = V_{\rm cc} - 0.5V$	-	4.5			0.8		0.8	
			$V_0 = V_{CC} - 0.5V$		6.0			1.1		1.1	
	 		70 VCC 0101	$I_{OH} = -20\mu A$	2.0	1.9		 	1.9	•	-
			,	$I_{OH} = -20\mu A$	4.5	4.4			4.4		
		HC	V. = V V.	$I_{OH} = -20\mu A$	6.0	-1			i e		
		Standard	$V_{I} = V_{IH}, \ V_{IL}$			5.9	 -	 	5.9		
	1			I _{OH} = -4.0mA	4.5	4.18			4.13		
				$I_{OH} = -5.2 \text{mA}$	6.0	5. 68		ļ	5. 63		
	. 1			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
		нс		$I_{OH} = -20\mu A$	4.5	4.4			4.4		
⁄он	High-level output voltage	Buffered	$V_i = V_{iH}, \ V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9		· ·	5.9		١
•		54,10,104		$I_{OH} = -6.0 \text{mA}$	4.5	4. 18			4.13		
				$I_{OH} = -7.8 \text{mA}$	6.0	5. 68			5. 63		
				$I_{OH} = -20\mu A$	2.0	1.8			1.8		
			$V_i = V_{iL}$	$I_{OH} = -20\mu A$	4.5	4.0			4.0	,	
		HCU	-	$I_{OH} = -20\mu A$	6.0	5.5			5.5		
		1	OND	$I_{OH} = -4.0 \text{mA}$	4.5	3. 98			3.84		
		,	V _I = GND	$I_{OH} = -5.2 \text{mA}$	6.0	5. 48			5.34	,	
				$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
			-	$I_{OL} = 20 \mu A$	4.5			0.1		0.1	ł
		HC	$V_i = V_{iH}, \dot{V}_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	
	1	Standard		I _{OL} = 4.0mA	4.5			0. 26		0.33	
				I _{OL} = 5. 2mA	6.0			0. 26		0.33	
			 	$I_{OL} = 20\mu A$	2.0		<u> </u>	0. 20		0.1	
	· · · · · ·			$I_{OL} = 20\mu A$	4.5			0.1		0.1	Ì
<i>1</i>	Low-level output voltage	HC	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20\mu A$	6.0			0.1		0.1	\
OL.	LOW-level output voltage	Buffered	VI - VIH, VIL		4, 5	-	<u> </u>	0.1	ļ	0.33	`
				I _{OL} = 6.0mA	1			Į į		Į.	
				I _{OL} = 7.8mA	6.0			0.26		0.33	
			., ,,	$I_{OL} = 20 \mu A$	2.0			0.2		0.2	ĺ
			$V_i = V_{iH}$	$I_{OL} = 20\mu A$	4.5			0.5	ĺ	0.5	
	.	HCU		$I_{OL} = 20 \mu A$	6.0			0.5		0.5	1
			$V_1 = V_{CC}$	I _{OL} = 4.0mA	4.5			0. 26		0.33	
				$I_{OL} = 5.2 \text{mA}$	6.0			0.36		0.33	-
н	High-level input current	1	V ₁ = 6V	<u> </u>	6.0	-		0.1	1	1.0	μ
IL	Low-level input current		$V_i = 0V$		6.0			—0. 1		-1.0	μ
оzн	Off-state high-level output current		$V_i = V_{iH}, \ V_{iL}, \ V_{iL}$	/o = Vcc	6.0			0.5		5.0	μ
OZL	Off-state low-level output current		$V_i = V_{iH}, \ V_{iL}, \ V_{iL}$		6.0			-0.5		-5.0	μ
		Gate			T			1.0		10.0	
cc	Quiescent supply current	F/F	VI = VCC, GND	$I_{0} = 0 \mu A$	6.0			2.0		20.0	μ
	1	MSI	1		1			4.0		40.0	1

MITSUBISHI HIGH SPEED CMOS INTRODUCTION

Table 8 Mitsubishi M74HCT Series Electrical Characteristics (Ta=-40~+80℃)

							Limits			
Symbol	Parameter	Туре		Test conditions		25℃		-40~	+85℃	Unit
	. *					Тур	Max	Min	Max	
V _{IH}	High-level input voltage		$ V_0 = 0.1V, V_{CO} $ $ I_0 = 20\mu A$					2.0		٧
VIL	Low-level input voltage		$V_0 = 0.1V, V_{00}$ $ I_0 = 20\mu A$;-0.1V			0.8		0.8	٧
				$I_{OH} = -20\mu A$	V _{cc} -0.1			V _{cc} -0.1		
		Standard	$V_i = V_{iH}, \ V_{iL}$	$I_{OH} = -4.0 \text{mA}, V_{CC} = 4.5 \text{V}$ $I_{OH} = -4.8 \text{mA}, V_{CC} = 5.5 \text{V}$	4. 18 5. 18			4. 13 5. 13		
V _{OH}	High-level output voltage			$I_{OH} = -20\mu A$	V _{CC} -0.1			V _{CC} -0.1		٧
		Buffered	$V_i = V_{iH}, V_{iL}$	$I_{OH} = -6.0 \text{mA}, V_{CC} = 4.5 \text{V}$	4.18			4. 13		
				$I_{OH} = -7.2 \text{mA}, V_{CC} = 5.5 \text{V}$	5.18			5.13		
				$I_{OL} = 20\mu A$			0.1		0.1	
	·	Standard	$V_i = V_{iH}, \ V_{iL}$	$I_{OL} = 4.0 \text{mA}, \ V_{CC} = 4.5 \text{V}$			0.26		0.33	
VoL	Low-level output voltage			$I_{OL} = 4.8 \text{mA}, \ V_{CC} = 5.5 \text{V}$			0.26		0.33	v
VOL	Low-level output voltage			$I_{OL} = 20\mu A$			0. 1		0.1	•
		Buffered	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 6.0 \text{mA}, V_{CC} = 4.5 \text{V}$			0.26		0.33	
				$I_{OL} = 7.2 \text{mA}, V_{CC} = 5.5 \text{V}$			0.26		0.33	
h _H	High-level input current		$V_i = V_{CC}$				0. 1		1.0	μA
l _{IL}	Low-levelinput current		V _i = GND				-0.1		-1.0	μA
lozh	Off-state high-level output current		$V_i = V_{iH}, \ V_{iL}, \ V_{iL}$	/ _o =. V _{cc}			0.5		5.0	μΑ
lożL	Off-state low-level output current		$V_i = V_{iH}, \ V_{iL}, \ V_{iL}$	o = GND			-0.5		-5. 0	μA
		Gate					1.0		10.0	
lcc	Quiescent supply current	F/F	Vi = Vcc, GND	$I_0 = 0 \mu A$			2. 0		20.0	μA
		MSI					4.0		40.0	
ΔI_{CC}	Maximum quiescent supply current		$V_1 = 2.4V, 0.4V$	/ (Note 3)			2.7		2.9	mA

Note $\,3\,:\,$ Only one is set at this value and other inputs are fixed at V_{CC} or GND

1. Basic Structure

Fig.1 shows the circuit structures of the M74HC series high-speed CMOS logic and the M4000B series (conventional) CMOS logic. The principal difference between the two is that the M4000B series employs aluminum gates, while the M74HC series employs a silicon-gate process. This fine pattern process has enabled us to increase the MOS transistor drive current capability and reduce the parasitic capacitances. (These two improvements allow the new structure to operate at frequencies as fast as LSTTL speed.)

2. Operational Description

Fig.2 show the one stage inverter circuit that is the basis of the high-speed CMOS logic. Fig.3 shows the behavior of this circuit (supply current $I_{\rm CC}$ and output voltage $V_{\rm O}$) when the supply voltage is $V_{\rm CC}$ and the input voltage $V_{\rm I}$ is raised from GND to $V_{\rm CC}$.

The characteristic curves of the logic are classified by dividing the graph into three regions according to the input voltage.

- I : In this region, only p-channel transistor T_2 is on. V_O is at V_{CC} and I_{CC} is negligible.
- II: In this region, V_{O} varies as a function of V_{I} . As V_{I} increases, n-channel transistor T_{1} turns on, causing V_{O} to fall. The slope of the descent steepens abruptly, and the value of V_{I} at that point is referred to as the threshold voltage of the circuit. Increases of V_{I} about this value bring V_{O} very close to GND level.

The value of V_O in region $I\!I$ is determined by the relative on resistances of T_1 and T_2 . I_{CC} is constantly flowing, and reaches a maximum where V_1 equals the threshold voltage.

III : In this region, only T₁ is on. V_O is at GND level, and I_{CC} is negligible.

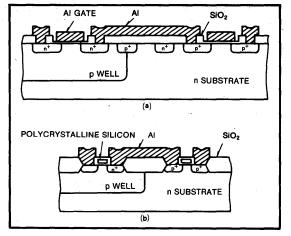


Fig.1 CMOS device structures

- (a) AI-GATE CMOS (4000B SERIES)
- (b) Si-GATE CMOS (M74HC SERIES)

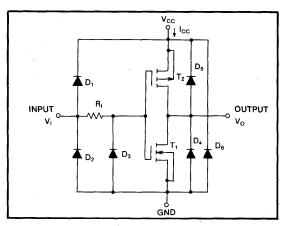


Fig.2 The one stage inverter circuit

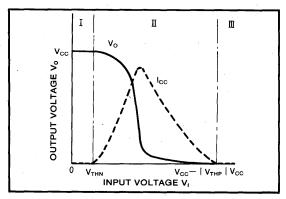


Fig.3 I/O and supply current characteristics of the one stage inverter



3. Transfer Characteristics

In high-speed CMOS logic, the circuit threshold voltage is designed approximately $1/2V_{\rm CC}$, far superior to the TTL and LSTTL logic, where the threshold voltage is independent of the supply voltage.

The M74HC series includes three devices types. The HC type has CMOS-level I/O with buffered outputs. The HCU types has CMOS-level I/O and a single stage of gates. The HCT type has TTL-level inputs and CMOS-level buffered outputs. The accompanying figures show the transfer char-

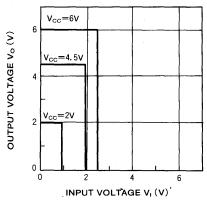


Fig.4-a Output voltage vs. input voltage (M74HC00)

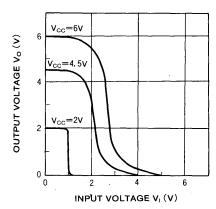


Fig.5-a Output voltage vs. input voltage (M74HCU04)

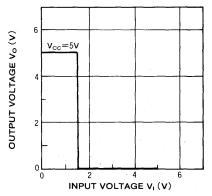


Fig.6-a Output voltage vs. input voltage (M74HCT240)

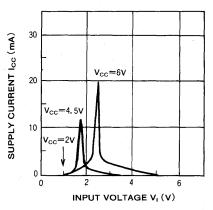


Fig.4-b Supply current vs. input voltage (M74HC00)

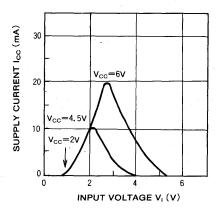


Fig.5-b Supply current vs. input voltage (M74HCU04)

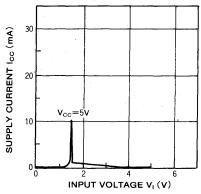


Fig.6-b Supply current vs. input voltage (M74HCT240)



acteristics of representative devices: Fig.4 shows the characteristics of M74HC00, Fig.5 those of M74HCU04, and Fig.6 those of M74HCT240. The left side of the figures (a) shows the output voltage $V_{\rm O}$ vs. the input voltage $V_{\rm I}$. The right side shows the supply current $I_{\rm CC}$ vs the input voltage $V_{\rm I}$.

In the HC type, when the input voltage reaches the thresold voltage, the output rieses abruptly and the supply current steeply and then drops steeply. Therefore, even if a slow-changing signal is applied to the input, the output voltage will be controlled by the steep characteristic curves at the threshold voltage, with the effect of regenerating the input waveforms. These characteristics also prevent the increase in power dissipation that occurs when slow-changing signals are applied to the HCU type.

The output voltage of the HCU type responds more slowly to input voltage variations.

This characteristics make the type suitable for applications in oscillators and other linear circuits. The use of slowly varying input signals, however, will increase the power dissipation.

The HCT type has steep threshold characteristics like the HC type that regenerate the input waveform, but with the HCT type, the input is TTL-level.



4. Switching Characteristics

The propagation time is one of the principal switching characteristics of an IC. In high-speed CMOS, the propagation time is determined by the internal time constant set by the on-state resistances of the p- and n-channel transistors and the capacitance of the wiring and of the next-stage gate. If a capacitive load is connected to the output terminals, the propagation time will be determined by the time constant of the output-stage p- and n-channel transistor on-state resistances and the load capacitance. The supply voltage V_{CC}, the load capacitances C_L, the input rise time t_r, the input fall time t_r, and the ambient temperature T_a all affect the propagation time.

The standard and buffered devices have different output drive-current capacities that cause the two types to exhibit differing relationships between the load capacitance and the propagation delay. Figs. 9 and 10 show the propagation delay vs C_L , Fig. 9 for the standard-type M74HC00, Fig. 10 for buffered-type M74HC240. The propagation delay of the buffered type shows only a small dependence on C_L . In addition, the higher the supply voltage is, the shorter the delay, and the lower the delay dependence on C_L . The delay increase with respect to the load capacitance is linear.

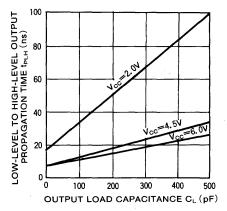


Fig.7-a Low-level to high-level output propagation time (M74HC00)

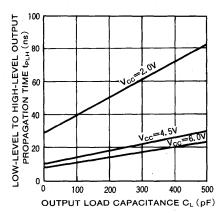


Fig.8-a Low-level to high-level output propagation time (M74HC240)

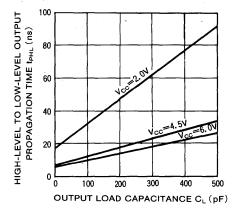


Fig.7-b High-level to low-level output propagation time (M74HC00)

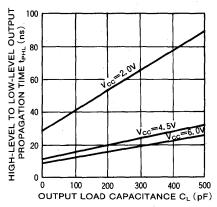


Fig.8-b High-level to low-level output propagation time (M74HC240)

5. Power Dissipation

The high-speed CMOS logic gates consist of n- and p-channel transistors that are serial-connected between $V_{\rm CC}$ and GND. While the gate is held at either $V_{\rm CC}$ or GND, one of the two transistors will be off, which means that while the input is tied to either $V_{\rm CC}$ or GND, the only current drain between $V_{\rm CC}$ and GND ($I_{\rm CC}$) will be that due to the leakage current of the pn junctions. As a result, the sink current is just 50pA at an ambient temperature $T_a=20^{\circ}\text{C}$, and still only several nA at $T_a=85^{\circ}\text{C}$.

As explained in the section 3, high-speed CMOS logic draws greater power during switching, when a current flows between $V_{\rm CC}$ and GND. The higher the supply voltage $V_{\rm CC}$, and the higher the switching frequency, the larger this current becomes. Capacitive loads at the output due to components or a large fanout will also draw charging currents that further increase the power dissipation. The power dissipation of the HCU type will also rise when driven by input signals with long rise and fall times $(t_{\rm f}, t_{\rm f})$.

Fig.9 shows typical power dissipation vs. operating frequency characteristics per gate of M74HC00 and M74LS00 devices with a capacitive load C_L of 0, 15, and 50pF. The power dissipation of the M74HC00 increases in proportion to the frequency. At a load of 15pF and operating frequency of 10MHz or over, the power dissipation of the M74HC00 exceeds that of the M74LS00, but for must applications, high-speed CMOS logic can substantially reduce power dissipation. When an ideal input waveform is applied, the power dissipation of this logic is given by:

$$P_d = (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f + I_{CC} \cdot V_{CC}$$

where C_{PD} is the internal power dissipation capacitance, C_L is the load capacitance, and f is the frequency. So simply connection a capacitive load to the M74HC00 will increase the power dissipation by only the capacitive charging and discharging currents. The same relation holds true in principle for the M74LS00, but even at low frequencies, its power dissipation remains high due to other factors. Another characteristics of high-speed CMOS logic is that the load capacitance is charged at V_{CC} and discharged at GND level, while LSTTL is limited to within the $0.2\!\sim\!4V$ range. This means that the M74HC00 is more greatly influenced by C_L , so at higher C_L values the bandwidth over which the M74HC00 dissipates less power become narrower. Therefore, good circuit design demands that the capacitative loads be kept as low as possible.

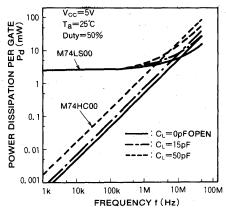


Fig.9 Power dissipation per gate vs. frequency for the M74HC00 and M74LS00

6. Noise Margin

As explained in the section 3, the threshold voltage of high-speed CMOS logic is approximately 1/2 of the supply voltage $V_{\rm CC}$. In addition, when there is no load, the high-level output voltage $V_{\rm OH}$ is nearly equal to $V_{\rm CC}$, and the low-level output voltage $V_{\rm OL}$ nearly at GND level. This gives high-speed CMOS logic a much high DC noise margin than LSTTL.

The high-level noise margin V_{HN} and low-level noise margin V_{LN} are given by $V_{HN} = V_{OH} - V_{IL}$, and $V_{LH} = V_{OL} - V_{IL}$. Fig.10 compares V_{HN} and V_{LN} of LSTTL and high-speed CMOS logic at a 5V supply voltage. V_{HN} and V_{LN} are both 1.4 for high-speed CMOS logic, a great improvement over the much lower values of LSTTL. In addition the threshold voltage of LSTTL has a temperature dependence of about $-2\text{mV}/^{\circ}\text{C}$, while high-speed CMOS logic has no such dependence — guaranteeing a constant noise margin over a wide temperature range.

The AC noise margins of LSTTL and high-speed CMOS logic is similar. At a 5V supply voltage, the typical propagation time of both is about 10ns, and both offer similar noise immunity.



INTRODUCTION

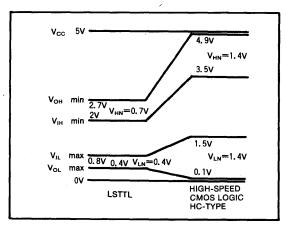


Fig.10 A comparison of LSTTL and high-speed CMOS DC noise margins (V_{CC}=5V)

7. Fanout

Unlike TTL and LSTTL, CMOS logic features an extremely high input impedance, so that when CMOS logic is being driven, high fanout will result in no DC problems. In AC terms, however, the capacitive load increase by the wiring capacitance and about 5pF per driven gate. This increases the propagation time, as shown in Figs. 7 and 8.

8. Input and Output Protection Circuit

The transistors employed in high-speed CMOS logic have a gate-oxide-layer thickness of $0.06\mu m$. This thin oxide layer has an insulation breakdown voltage of only 100V, therefore any larger voltages applied on the gate will destroy the IC. To prevent this from occuring, all devices in the M74HC series feature an input protection circuit consisting of diodes D_1 , D_2 , and D_3 , and resistor R_1 in place of a conventional direct input.

When a steeply sloped positive overvoltage pulse is applied to the input, it charges the parasitic capacitor formed by R_1 in parallel with $D_1,\,D_2,\,$ and $D_3.$ The time constant of this circuit delays the voltage rise on the gate, while D_1 passes a current to $V_{CC},\,$ this clamps the input voltage at $V_{CC},\,$ and prevents high voltages from appearing on the gate oxide layer.

If a steeply sloped negative overvoltage pulse is applied to the input, D_2 and D_3 clamp the gate voltage at their forward-bias voltage level. This means that the circuit can withstand inputs over 500V producted by discharge of a 200pF capacitor, or inputs over 3kV produced by discharge of a 100pF capacitor with a 1.5k Ω resistance. These values are comparable with LSTTL and TTL.

 D_4 and D_5 protect the circuit against overvoltages at applied at the outputs. When a surge voltage is applied at

 V_{CC} , D_6 forms protective circuit. These diodes respond quickly to overvoltages and ensure adequate protection against transients, but extended operation outside the absolute maximum ratings will destroy the protective diodes and the circuit function.

In addition to protection against conditions arising under ordinary use, the M74HC series has been designed to withstand I/O surge currents of up to ±20mA without demage. Although the individual data sheets for the series may not show this I/O protection circuit, each device incorporates this circuit, each device incorporates this circuit,

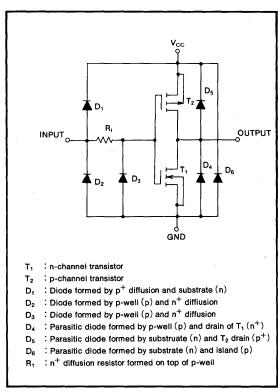


Fig.11 The protection circuit of the M74HC series

DEFINITIONS AND TEST METHODS FOR SPECIFICATIONS AND TYPICAL CHARACTERISTICS

This section lists ratings that must be followed to ensure that high-speed CMOS devices operate properly. We define these ratings, describe the test conditions used to measure them, and list standard characteristics.

1. Absolute Maximum Ratings

These are the absolute limits at which the manufacturer guarantees device reliability. None of these ratings may be exceeded, even momentarily, without risking reduced reliability or destruction of the device. Absolute maximum ratings include the following items.

- (1) Supply voltage (V_{CC})
- (2) Input voltage (V_I)
- (3) Switching I/O voltage (VIO)
- (4) Output voltage (V_O)
- (5) Input protection diode current (IIK)
- (6) Output parasitic diode current (IOK)
- (7) Output current (Io)
- (8) Supply/GND current (I_{CC})
- (9) Power dissipation (Pd)
- (10) Storage temperature range (Tstg)

1-1 Supply Voltage (V_{CC})

Specifies the range of supply voltages that may be safely applied at $V_{\rm CC}$ terminal with respect to ground. This range includes voltage surges that exceed standard operating conditions.

When the applied voltage exceeds this range, parasitic bipolar transistors turn on, and this thyristor operation causes a large current to flow from $V_{\rm CC}$ to GND. This phenomenon, known as "latchup", may either destroy the IC or greatly reduce its reliability.

1-2 Input Voltage (V_I)

Indicates the permissible applied voltage at the input terminals with respect to GND. Exceeding this value may cause latchup.

1-3 Switching I/O Voltage (V_{IO})

Applies to devices containing analog switching circuits such as M74HC4066, and specifies the maximum permissible voltage that may be applied to the switching input or output terminals without causing latchup.

1-4 Output Voltage (Vo)

Usually, fixed voltages are not applied to the output terminals under normal operating conditions, this ratings specifies the maximum surge voltages allowable at the output terminals. When the output state is high, these surges must remain below $V_{\rm CC}+0.5V$, when the output state is low, they cannot drop below -0.5V. Surges exceeding the high-state value will cause a current to flow into the IC, which may either destroy the output protection diodes or cause latchup. Surges exceeding the low-state value will cause a current to flow out of the IC with equally damaging effects.

1-5 Input Protection Diode Current (IIK)

Usually, fixed currents are not applied to the input terminals under normal operating conditions, specifies the maximum

surge current allowable at the input terminals. Surges exceeding this value may destroy the input protection diodes or cause latchup.

1-6 Output Parasitic Diode Current (I_{OK})

Fixed currents are not applied to the output terminals under normal operating conditions.

Specifies the maximum surge currents allowable at the output terminals. The high-state value applies to incoming currents when output is high; the low-state value to outflowing currents when the output is low. Surges exceeding these values may either destroy the output protection diodes or cause latchup.

1-7 Output Current (Io)

Specifies the maximum allowable currents at the output terminals during normal operation. The high-state value indicates the current outflow, the low-state value, the current influx. Currents exceeding these values may destroy the IC or greatly reduce its reliability.

1-8 Supply/GND current (I_{CC})

Specifies the maximum allowable current flow from V_{CC} to GND during normal operation. Currents exceeding this value may destroy the IC or greatly reduce its reliability.

1-9 Power Dissipation (Pd)

Specifies the maximum allowable power dissipation for the printed-circuit-board-mounted IC at operating temperature (Topr).

1-10 Storage Temperature Range (Tstg)

Specifies the ambient temperature limits at which the device can be stored when no voltages are applied to either inputs or outputs. Care is especially important when devices are being stored in unheated warehouses or shipped via air freight.

2. Recommended Operating Conditions

These parameters indicate limits of the supply voltage, I/O conditions, and other important factors that must be met for the IC to perform properly under normal use. If these conditions are exceeded, proper operation cannot be guaranteed, even if the device is still operating within the absolute maximum ratings.

2-1 Supply Voltage (V_{CC})

Specifies the supply voltage applied at V_{CC} with respect to ground. The supply voltage of high-speed CMOS devices is $2\sim6V$ (4.5 $\sim5.5V$ for type HCT), which is much wider than TTL devices (4.75 $\sim5.25V$).

2-2 Input Voltage (V_I)

Specifies the optimum input voltage range. This range is the same for all supply voltage range of $V_{CC}=2\sim6V$.

2-3 Output Voltage (Vo)

Specifies desirabel limits for transient voltages at the output pins. This range is the same for all supply voltage range of $V_{\rm CC}=2\sim6V$.

2-4 Operating Temperature Range (Topr)

Specifies the ambient tmeperature range within which the



device exhibits the specified electrical characteristics and performs normally.

2-5 Rise and Fall Times (tr, tf)

Specifies the optimum rise and fall times of the input waveforms. These limits should be followed at all supply voltages of $V_{\rm CC}=2$, 4.5, and 6V, otherwise output oscillation, timing problems, or excessive power dissipation may result. This restriction does not apply to devices incorporating Schmitt trigger inputs.

3. Function

The functional behavior of the device is indicated by either a function table or a timing diagram. These characteristics are checked over the $2\sim6V$ supply voltage range. The inputs are set high or low as specified, and the output conditions monitored.

4. Electrical Characteristics (see Section 7-1)

These characteristics are measured at input and output and power supply terminals at temperature T_a under worst-case conditions. All parameters are guaranteed at 2, 4.5, and 6V supply voltages, except for I_{IH} , I_{IL} , I_{OZH} , I_{OZL} , and I_{CC} , which are guaranteed at V_{CG} =6V only.

4-1 High-Level Input Voltage (VIH)

Specifies the high-level input voltage required to generate the specified output conditions.

4-2 Low-level Input Voltage (VIL)

Specifies the low-level input voltage required to generate the specified output conditions.

4-3 Positive-going Threshold Voltage (V_{T+})

In devices with Schmitt trigger inputs, this parameter indicates the voltage at which the output state inverts as the input voltage is increased from a level below the negative-going threshold voltage (V_{T-}) .

4-4 Negative-going Threshold Voltage (V_T-)

In devices with Schmitt trigger inputs, this parameter indicates the voltage at which the output state inverts as the input voltage is decreased from a level above the positive-going threshold voltage (V_{T+}) .

4-5 Hysteresis Voltage (VH)

In devices with Schmitt trigger inputs, this parameter indicates the difference between the positive-going and negative-going threshold voltages.

4-6 High-level Output Voltage (V_{OH})

Indicates the high-level output voltage obtained at the outputs when high-level input voltage V_{IH} (V_{T+} for Schmitt trigger devices) and low-level input voltage V_{IL} (V_{T-} for Schmitt trigger devices) are applied as specified to the input terminals indicated to the input.

4-7 Low-Level Output Voltage (VoL)

Similar to the above. Indicates the low-level output voltage obtained under the specified conditions.

4-8 Maximum Output Leak Current (Io)

In devices with open drain outputs, this parameter indicates the current outflow with 0V applied at the output voltage or current influx with 6V applied at the output. The supply voltage is 6V.

4-9 On-State Resistance (RoN)

Applies to devices containing analog switching circuits. Indicates the DC on-state resistance of the analog switches. Guaranteed for input voltage of 0 to $V_{\rm CC}$.

4-10 On-State Resistance Variation (△R_{ON})

Indicates the difference between the maximum and minimum on-state resistance values (R_{ON}) for analog switches in a single device.

4-11 Off-State Input-to-Output Leak Current (IOFF)

Indicates the leakage current that flows from the input to the output of analog switches when 6V is applied. Specified at V_{CC} =6V.

4-12 High-Level Input Current (IIH)

Indicates the current that flows into the device when 6V is applied to the input at $V_{\rm CC}\!=\!6V$. $I_{\rm IH}$ for type HCT is determined with input and supply voltages of 5.5V.

4-13 Low-Level Input Current (IIL)

Indicates the current that flows out of the device when 0V is applied to the input at $V_{\rm CC}$ =6V. $I_{\rm IL}$ for type HCT is determined with a supply voltage of 5.5V.

4-14 Off-state High-Level Output Current (I_{OZH})

Applies to devices with three-state outputs. Indicates the current that flows into the device when 6V is applied to an output in the high-impedance state at $V_{\rm CC}=6V$. $I_{\rm OZH}$ for type HCT is determined with input and supply voltage of 5.5V. When the outputs are not in the high-impedance state, they are kept low by selection of the input conditions.

4-15 Off-State Low-Level Output Current (IOZL)

Applies to devices with three-state outputs. Indicates the current that flows out of the device when 0V is applied to an output in the high-impedance state at $V_{\rm CC}=6V$. $I_{\rm OZL}$ for type HCT is determined with a supply voltage of 5.5V. when the outputs are not in the high-impedance state, they are kept high by selection of the input conditions.

4-16 Quiescent Supply Currnet (I_{CC})

Indicates the current that flows at $V_{\rm CC}$ when the output conditions are stable. The stated values are guaranteed when the input conditions are set according to the function table with high-level inputs at $V_{\rm CC}$ and low-level inputs at ground.

4-17 Maximum Quiesenct Supply Current (△I_{CC})

Applies to device with TTL-level inputs (type HCT). Indicates the current that flows at $V_{\rm CC}$ when the output conditions are stable. The current is specified with 2.4V and 0.4V applied at a single input while all other inputs are held at $V_{\rm CC}$ or ground and $V_{\rm CC}$ is at 5V \pm 10%.

4-18 Active-State Supply Currnet (I_{CC})

Applies to one-shot multivibrator circuits. Indicates the current that flows at $V_{\rm CC}$ when the timing circuit constate $R_{\rm X}/C_{\rm X}$ is 1/2 $V_{\rm CC}$. The stated values are guaranteed when the



input conditions are set according to the function table with high-level inputs at V_{CC} and low-level inputs at GND.

5. Switching Characteristics (see sections 7-2, 7-3, and 7-4)

5-1 Low-Level to High-Level Output Transistion Time (t_{TLH})

Indicates the time required for the output waveform to change from 10% to 90% of $V_{\rm CC}$ when inputs are applied to cause the output to change from low to high.

5-2 High-Level to Low-Level Output Transition Time (t_{THL})

Indicates the time required for the output waveform to change from 90% to 10% of $V_{\rm CC}$ when inputs are applied to cause the output to change from high to low.

5-3 Low-Level to High-Level Output Propagation Time (t_{PLH})

Indicates the time required from when the input conditions are changed until the output voltage crosses the specified voltage range moving from low to high.

5-4 High-Level Low-Level Output Propagation Time (t_{PLH})

Indicates the time required from when the input conditions are changed until the output voltage crosses the specified voltage range moving from high to low.

5-5 Output enable time to high-level (t_{PZH})

Applies to devices with three-state outputs. Indicates the time required from when the input conditions are changed until the output state changes from the high-impedance state to logic high.

5-6 Output enable time to low-level (t_{PZL})

Applies to devices with three-state outputs. Indicates the time required from when the input conditions are changed until the output state changes from the high-impedance state to logic low.

5-7 Output disable time from high-level (t_{PHZ})

Applies to devices with three-state outputs. Indicates the time required from when the input conditions are changed until the output state changes from logic high to the high-impedance state.

5-8 Output disable time from low-level (t_{PLZ})

Applies to devices with three-state outputs. Indicates the time required from when the input conditions are changed until the output state changes from logic low to the high-impedance state.

5-9 Maximum clock Frequency (fmax)

Applies to devices containing flip flops. Indicates the maximum frequency at which clock signals can be applied

while maintaingin stable output waveforms in the specified sequence. The input conditions are set so that each clock pulse will cause a change in the output state.

5-10 Sine Wave Distortion

Applies to devices containing analog switches, indicates the distortion of sine waves passing through analog switches in the "on" state. The sine wave frequency is 1kHz, and the amplitude 1.25V_{P-P}. Measurements are performed at $V_{\rm CC}=2.5V$, and $V_{\rm SS}=-2.5V$.

5-11 Maximum Transmission Frequency (f_{max}(I/O))

Applies to devices containing analog switches. Indicates the frequency bandwidth transmitted by analog switches in the "on" state. A 1.25V_{P-P} sine wave is applied at the I/O terminals and the frequency is increased until the output is 3dB down from the input level (about 7/10). This frequency is designated at f_{max} (I/O). Measurements are performed at V_{CC}=2.5V, and V_{SS}=-2.5V.

5-12 Feedthrough

Applies to devices containing analog switches. Indicates the degree of isolation between the I/O terminals of a switch in the off-state. When a sine wave signal is applied at one side of an off-state switch, it is transmitted through the static capacitnace of IC to the other side of the switch at a level that increases proportionally with the frequency of the applied signal. The frequency at which the output voltage is 50dB down from the input voltage (about 1/316), is defined as the feedthrough level.

5-13 Crosstalk (Control-Input-to-Switch)

Applies to devices containing analog switches. Indicates the degree of interference between signals at the control inputs and those at the I/O pins of the analog switches. A pulse is applied to a control input, and the pulse level at an switch terminal is measured with no inputs applied to the switch inputs.

5-14 Crosstalk (Switch-to-Switch)

Applies to devices containing analog swithces. Indicates the degree of interference between signals at the I/O terminals of independent switches. A pulse is applied at an on-state switch input, and the pulse level at the output of a separate off-state switch is measured.

5-15 Maximum Control Frequency (fmax (C))

Applies to devices containing analog switches. Indicates the maximum allowable frequency of the signals applied to the control inputs. A standard square-wave signal is applied at a control input, and the frequency is increased until the output level falls to 1/2 of the output level at an input frequency of 1kHz. This frequency is defined as f_{max} (C).

5-16 Input Capacitance (C_I)

Indicates the capacitance between an input terminal and GND. It is normally measured at 0V and f=1MHz.

5-17 Feedthrough Capacitance $(C_{X-Y}, Y-X)$

Applies to devices containing analog switches. Indicates the capacitance between I/O terminals of a switch in the off state.



5-18 Off-State Output Capacitance (Co)

Applies to devices with three-state or open-drain outputs. Indicates the capacitance between outputs in the high-impedance state and ground.

5-19 Power Dissipation Capacitance (Cpd)

Indicates the internal capacitnace of the device, calculated on the basis of the power dissipation during no-load operation. The no-load power dissipation is calculated as;

$$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$$

6. Timing Requirements (see sections 7-2 and 7-3)

These parameters specify the input timing requirements for clock pulses, reset pulses, etc. required by devices containing flip flops to maintain stable output waveforms in the specified sequence.

Timing requirements are measured at $T_a=25 \, ^{\circ}\!\!\! {\rm C}$, and include pulse width, setup time, hold time, and recovery time.

6-1 Pulse Width (tw)

Specifies the minimum interval between the standard voltage levels on the leading and trailing edges of input pulses. Shorter pulses may be ignored or may cause misoperation.

6-2 Setup Time (tsu)

For input data to be read correctly when a clock pulse or similar read signal is applied, the input conditions must be set in advance by a specified interval termed as the setup time. The setup time is defined as the period from the standard voltage levels of the active edges of the input signals until the standard voltage level of the read signal active edge. Negative setup times indicate that the input conditions can be set after the read signal.

6-3 Hold Time (th)

For input data to be read correctly when a clock pulse or similar read signal is applied, the input conditions must be held for specified interval after the read signal is applied. This interval is termed as the hold time. Negative hold times indicate that the input conditions can be changed before the read signal is applied.

6-4 Recovery Time (trec)

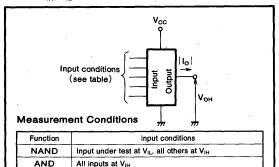
The recovery time indicates the interval after a read operation has been performed until a clock pulse can be applied to initiate the next read operation. It is specified as the period between the read operation and the standard voltage level of the clock pulse active edge.

7. Test Circuits

This sections shows typical test circuits used to measure the above paramenters. For detailed test conditions specific to individual devices, refer to the individual data sheets.

7-1 DC Test Circuits

7-1-1 V_{IH}, V_{IL}(1)



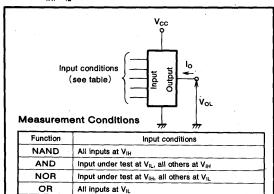
OR Input under test at V_{IH}, all others at V_{IL}

Note: The input conditions of devices with three-state inputs are set to place the outputs in the active (low-impedance) state

All inputs at VIL

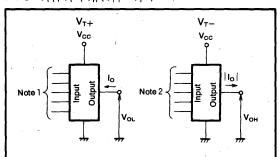
7-1-2 VIH, VIL (2)

NOR



Note: The input conditions of devices with three-state inputs are set to place the outputs in the active (low-impedance) state

7-1-3 $V_{T+}, V_{T-}, V_H (V_{T+} - V_{T-})$

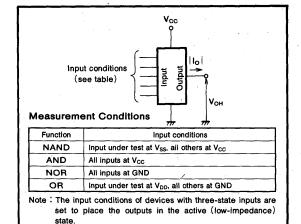


Note 1: When measuring $V_{T+},$ all inputs are set at $V_{T+}. \\$

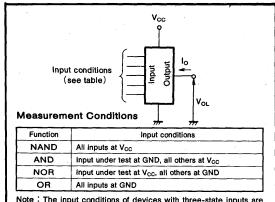
te 2: When measuring V_{T-} , the input under test is set at V_{T-} ,

and all others at V_{T+} . Note 3: Measured at all inputs.

7-1-4 Voh

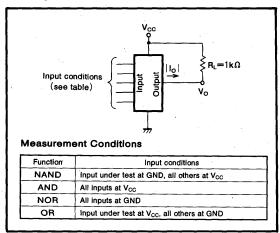


7-1-5 V_{OL}



Note: The input conditions of devices with three-state inputs are set to place the outputs in the active (low-impedance) state.

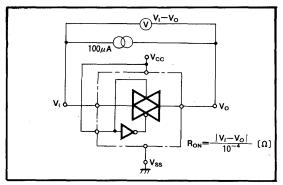
7-1-6 lo



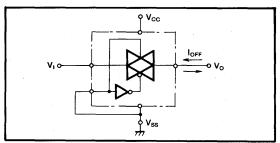
Note: Measured at all inputs

DEFINITIONS AND TEST METHODS FOR SPECIFICATIONS AND TYPICAL CHARACTERISTICS

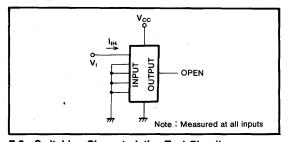
7-1-7 On-State Resistance (Ron)



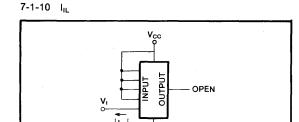
7-1-8 I_{OFF}



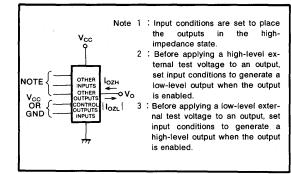
7-1-9 I_{IH}

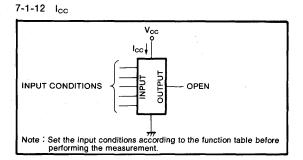


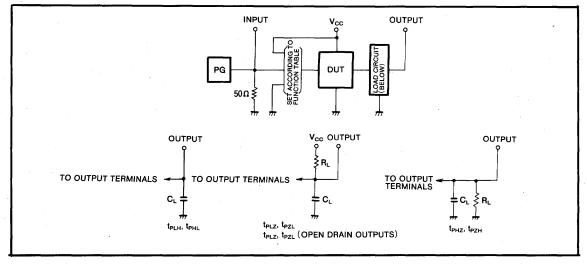
7-2 Switching Characteristics Test Circuits



7-1-11 I_{OZH}, I_{OZL}



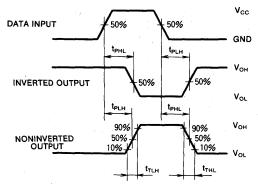


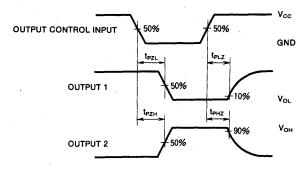


7-3 Timing Charts

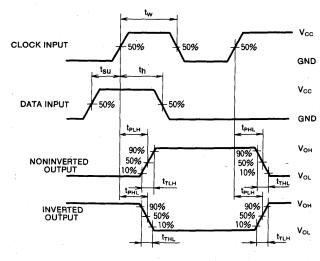
7-3-1 Types HC and HCU

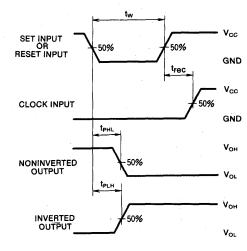
OTypical Gate (including gates with three-state outputs)



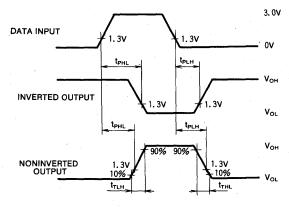


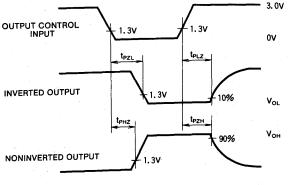
O Typical Flip Flop





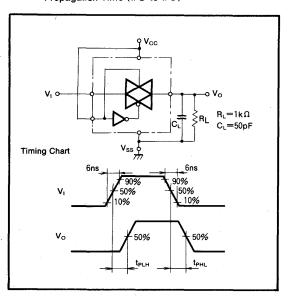
7-3-2 Type HCT



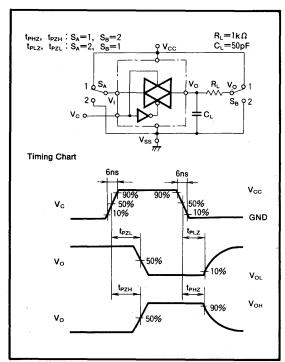


7-4 Switching Characteristic Test Circuits for Analog Switchs

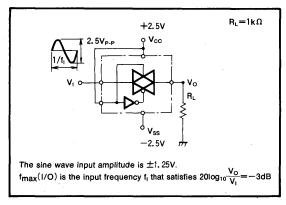
7-4-1 Low-Level to High-Level and High-Level to Low-Level Propagation Time (I/O-to-I/O)



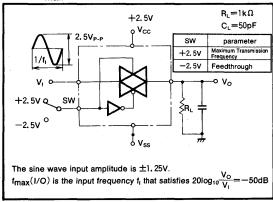
7-4-2 Low-Level to High-Level and High-Level to Low-Level Propagation Time (Control-Input-to-I/O)



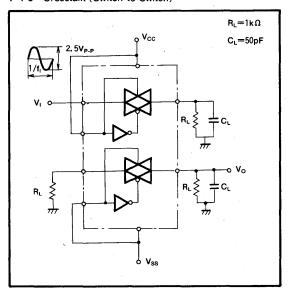
7-4-3 Sine Wave Transmission



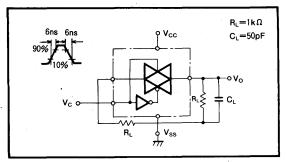
7-4-4 Feedthrough, Maximum Transmission Frequency (f_{max}(I/O))



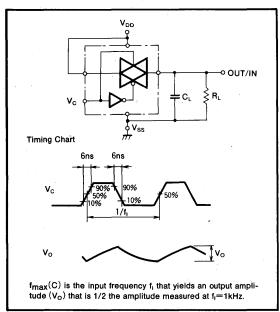
7-4-5 Crosstalk (Switch-to-Switch)



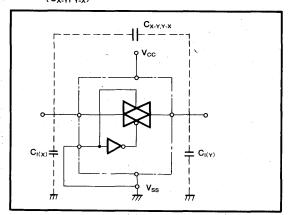
7-4-6 Crosstalk (Control-Input-to-Switch)

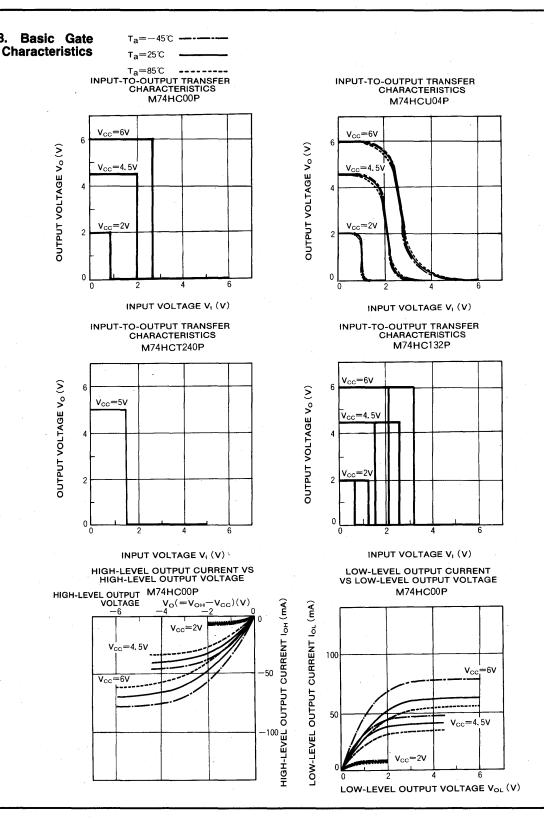


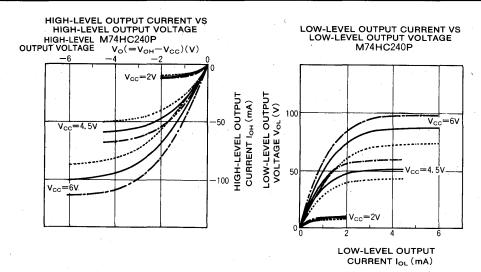
7-4-7 Maximum Control Frequency (fmax(C))



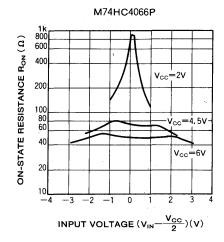
7-4-8 Input Capacitance C_{l_1} , Feedthrough Capacitance $(C_{X-Y,\ Y-X})$



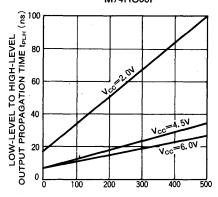




ANALOG SWITCH ON-STATE RESISTANCE

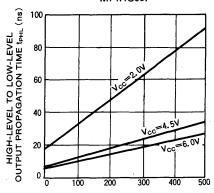


LOW-LEVEL TO HIGH-LEVEL OUTPUT PROPAGATION TIME VS LOAD CAPACITANCE M74HC00P



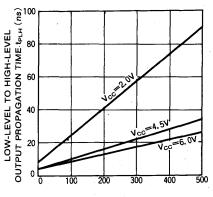
OUTPUT LOAD CAPACITANCE Co (pF)

HIGH-LEVEL TO LOW-LEVEL OUTPUT PROPAGATION TIME VS LOAD CAPACITANCE M74HC00P



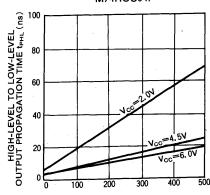
OUTPUT LOAD CAPACITANCE Co (pF)

LOW-LEVEL TO HIGH-LEVEL OUTPUT PROPAGATION TIME VS LOAD CAPACITANCE M74HCU04P



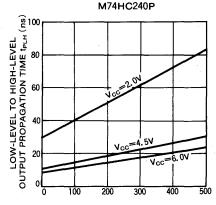
OUTPUT LOAD CAPACITANCE Co (pF)

HIGH-LEVEL TO LOW-LEVEL OUTPUT PROPAGATION TIME VS LOAD CAPACITANCE M74HCU04P



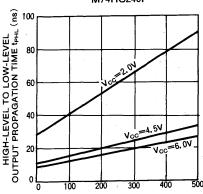
OUTPUT LOAD CAPACITANCE Co (pF)

LOW-LEVEL TO HIGH-LEVEL OUTPUT PROPAGATION TIME VS LOAD CAPACITANCE



OUTPUT LOAD CAPACITANCE Co (pF)

HIGH-LEVEL TO LOW-LEVEL OUTPUT PROPAGATION TIME VS LOAD CAPACITANCE M74HC240P



OUTPUT LOAD CAPACITANCE Co (pF)

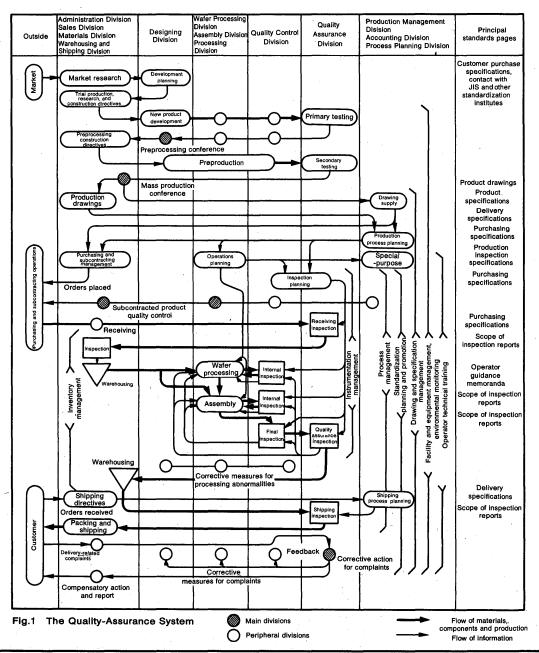
1. Introduction

Technical advances in recent years have allowed manufactures to repidly improve the speed, integration scale, and other facets of IC performance. At the same time, the greater complexity and reliability demands of the electronic-equipment market and the heavy use ICs in automatic insertion and assembly operations mean that manufacturers need reliable devices with consistent performance paramenters. This section introduces the quality-assurance sys-

tem and reliablility test procedures used at Mitsubishi Electric to guarantee that our customers receive highly uniform and reliable products.

2. The Quality-Assurance System

This system consists of quality-assurance procedures in the design and production processes. Fig. 1 shows the entire system.



2-1 Design Quality Assurance

Quality is maintained through use of two methods:

- Breadboard test circuits are configured from ICs and other standard components, and the characteristics and quality are evaluated.
- (2) Circuit and device design are performed using CAD technology and systematic documented design standards

2-2 Production Quality Assurance

Quality is maintained by the following management and inspection operations:

- (1) Environmental management
- (2) Regular and systematic inspection and maintenance of the design, tools, and instrumentation.
- (3) Purchased materials quality management
- (4) In-process management
- (5) Internal inspections performed during wafer processing and assembly
- (6) Final pass/fail inspections of finished product appearance, dimensions, construction, and electrical characteristics
- (7) Final quality assurance inspection performed from the customer standpoint. This inspection assesses the overall product quality and approves the products for warehousing.

Per Lot Inspection: Visual, labeling, and electrical characteristics

Regular Inspection: Devices are periodically drawn from passed lots for reliability tests including environ-

mental tests and mechanical durability tests, and aging tests. This inspection is performed once in several months.

2-3 Reliability Evaluation from Development Testing through Mass Production

To verify device reliability as described in sections 2-1 and 2-2, evaluations are performed during trial production, preproduction and mass production stages.

Only when the device passes the primary tests during trial production does it move into preproduction and secondary testing. The preproduction stage involves higher production volumes, and the secondary tests confirm that the quality and reliability verified in the primary testing are maintained. Quality-assurance inspections are also conducted during mass production to ensure continuing quality and reliability.

3. Reliability Tests

3-1 Methods of Determining and Ensuring Reliability

The reliability of high-speed CMOS ICs is evaluated in the following manner:

- (1) The basic operation of the circuits is checked at the transistor and cell level using breadboarded circuits. These measurements are used to determine the basic reliability of the wafer process and the design.
- (2) A simple block circuit is evaluated.
- (3) The products are evaluated as the intergration scale is raised successively to ensure overall reliability. Fig. 2 shows the elements of these processes.

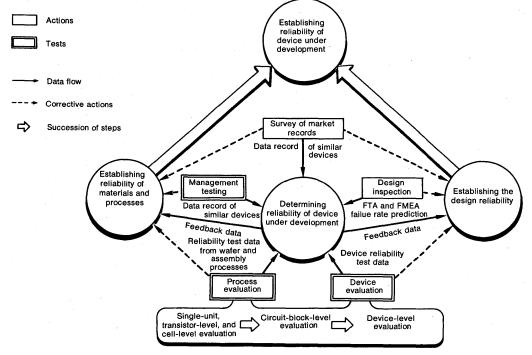


Fig.2 Methods of Determining and Ensuring Reliability



3-2 Test Items and Conditions

Table 1 Reliability Test Items and Conditions for the M74HC00P Series

Test item		Conditions	Measured parameters	
Solderability test	•	Wetted with rosin-base flux and immersed up to stoppers for 5sec in 230℃ solder bath.	Visual inspection	
Soldering reliability test		260°C, 10sec		
Thermal stress	Thermal shock test	-40~125℃, 15cycles, 10min/cycle	Electrical characteristics	
	Temperature cycle test	-65~150℃, 1 hr/cycle	·	
Lead strength test		250g, 90°, bent three times	Visual inspection	
	Shock test	1500G, 0. 5msec, 3times each along X, Y, and Z axes		
Mechanical stress	Natural drop test	75cm to a wooden board, Y ¹ direction, 3times	Electrical characteristics	
Mechanical stress	Vibration test	20G, 100~2000Hz, 4times each along X, Y, and Z axes	Electrical characteristics	
Constant acceration test		20000G, Y direction, 1min	<u> </u>	
High-temperature op	eration life test	Ta=85°C, 125°C, 150°C V _{CC} =6V, 8.5V	Electrical characteristics	
High-temperature sto	orage life test	Ta=150°C	Electrical characteristics	
	High-temperature high- humidity storage test	85°C, 85%RH		
Humidity resistance Humidity resistance Pressure-cooker test (saturated) Pressure-cooker test (unsaturated)		85°C, 85%RH V _{CC} =6V		
		121°C, 2atm, 100%	Electrical characteristics	
		130°C, 85%RH, V _{CC} =6V		

Table 2 Reliability Test Items and Conditions for the M74HC00FP Series

Test item	Conditions	Measured parameters
Solderbility test	Wetted with rosin-base flux and immersed up to stoppers for 5sec in 230°C solder bath.	Visual inspection
Soldering thermal stress test (1)	Entire surface immersed in solder (260°C, 10sec, 3times)	Electrical characteristics
	₽	,
	High-temperature, high-humidity blas test (85℃, 85%RH, V _{CC} =6V, 1000hr)	
Soldering thermal stress test (2)	Entire surface immersed in solder (260°C, 10sec, 3times)	Electrical characteristics
	₽	
	Pressure-cooker test (121°C, 2atm, 240hr)	
Soldering thermal stress test (3)	High-temperature high-humidity storage (85℃, 85%RH, 24hr)	Electrical characteristics
	₽.	
	Entire surface immersed in solder (260°C, 10sec, 3times)	
	Φ	1
	High-temperature, high-humidity bias test (85℃, 85%RH, V _{CC} =6V, 1000hr)	
Thermal stress test	Entire surface immersed in solder (260°C, 10sec, 3times)	Electrical characteristics
	D	
	Thermal shock test (-40~+125°C, 15cycles)	
	\hat{v}	
	Temperature cycle test (−65~+150°C, 500cycles)	
High-temperature, high-humidity bias test	85°C, 85%RH, V _{CC} =6.0V, 1000hr	Electrical characteristics
Pressure-cooker test (saturated)	121°C, 2atm, 240hr	Electrical characteristics
Pressure-cooker test (unsaturated)	130°C, 85%RH, V _{CC} =6.0V, 1000hr	Electrical characteristic
Lead strength test	250g, 90°, bent three times	Visual inspection
High-temperature operation life test	Ta=125°C, V _{CC} =6.0V, 1000hr	Electrical characteristics
High-temperature storage life test	T _a =150℃, 1000hr	Electrical characteristic



3-3 Deveice Failure Cirteria

(1) Electrical Characteristics

Table 3 Device Failure Criteria

Parameter	Failure	points	Unit
Parameter	Lower	Upper	Unit
High-level output voltage (V _{OH})	LX0.9	-	٧
Low-level output voltage (V _{OL})	_	UX1.1	V
High-level output current (I _{OH})	L×0.8	_	mA
Low-level output current (IoL)	L×0.8	- 1	mA
High-level input voltage (V _{IH})	L×0.8	-	٧
Low-level input voltage (VIL)	_	UX1.2	٧
Input current (I _I)	_	U×2.0	μΑ
Quiescent supply current (I _{CC})	_	UX2.0	μΑ
Functional fault	Short, open.	misoperation	_

L: Lower limit U: Upper limit

(2) Solderability

Solder adheres to less than 95% of the wetted area.

(3) Terminal Strength

Lead separation or damage is observed.

3-4 Results of Reliability Tests

Table 4 shows the results of reliability tests on M74HC00P series DIP devices, and Table 5 those of M74HC00FP SOP devices.

(1) High-Temperature Operation Tests

Tests were conducted under the following conditions: $V_{CC}=6$, 8.5V (6V only for SOPs), and $T_a=85$, 125, 150°C (125°C only for SOPs). Table 6 shows the failure ratios based on this data. At $T_a=25$ °C, the statistical failure ratio is 0.0012% /1,000hr (1.2FIT), and at $T_a=55$ °C, it is 0.001%/1,000hr (10FIT).

(2) High-Temperature Storage Test

Devices were stored for 2,000 hours (1,000 for SOPs) without any failures.

(3) Humidity Tests

Test items included 2,000 hours of high-temperature, high-humidity storage, 2,000 hours of high-temperature, high-humidity bias (1,000hr for SOPs), and 240 hours each of saturated and unsaturated pressure-cooker tests. No devices failed, indicating that no humidity-related application problems will develop.

(4) Soldering Termal Stress Test

The results show that the heat stress problems generally associated with surface-mounted SOPs have been solved.

- (5) Solderability, Thermal Stress, Mechanical Stress, and Terminal Strength Tests
 - No devices failed during any of these tests. Table 7 shows the results of reliability tests performed on samples drawn from lots at periodic intervales.
- (6) Electro-Static Discharge Test
 - Table 8 shows the results of a electro-static discharge test performed using the capacitor charging method (Mil. Std. 883-C, Method 3015, C=100pF, R=1.5k Ω) Fig.3 shows the test circuit.
 - M74HC series employ thinner gate oxide layers and use finer patterns than those of M4000B series. This render M74HC series highly vulnerable to static destruction. This potential drawback has been overcome through improved layout and I/O protection circuit design. All pins of all devices can withstand at least ±3kV.
- (7) Latchup Resistance Test

Although static electricity would readily cause latchup in previous CMOS devices, the pattern layout and I/O protection of Mitsubishi M74HC series high-speed CMOS devices has eliminated this source of latchup.

In-house checks of latchup resistance were performed using the capacitor-charging and current-injection methods, and in no case did a device fail due to latchup. Instead, the breakdown characteristics were the limiting factor.

Table 9 shows the results determined by the capacitor charging method (Fig.4) based on C=200pF and R=0 Ω . The latchup resistance was evaluated at inputs, outputs and V_{CC} .

Fig.10 shows the latchup resistance determined using the current-injection method at the input and output pins. Trigger currnets were typically near ±300mA, indicating extermely high latchup resistance.

Table 4 Results of Reliability Tests on the M74HC00P Series

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Test item		Conditions	Qty	Failures
Solderability test		Wetted with rosin-base flux and immersed up to stoppers for 5sec in 230℃ solder bath.	264	0
	Soldering reliability test	260°C, 10sec	836	0
Thermal stress	Thermal shock test	-40~125℃, 15cycles, 10min/cycle	836	0
	Temperature cycle test	-65~150℃, 1 hr/cycle	836	0
	Shock test	1500G, 0.5msec, 3times each along X, Y, and Z axes	132	0
Machaniani alesa	Natural drop test	75cm to a wooden board, Y ¹ direction, 3times	132	0
Mechanical stress	Vibration test	20G, 100~2000Hz, 4times each along X, Y, and Z axes	132	0
	Constant acceration test	2000G, Y direction, 1min	132	0
Lead strength test		250g, 90°, bent three times	198	0
High-temperature operation life test (1)		85℃, V _{CC} =6V, 2000hr		0
High-temperature operation life test (2)		85°C, V _{CC} =8.5V, 2000hr	376	0
High-temperature operation life test (3)		125°C, V _{CC} =6V, 2000hr	298	0
High-temperature op	eration life test (4)	125°C, V _{CC} =8.5V, 2000hr		1(I _{CC} over)
High-temperature op	eration life test (5)	150°C, V _{CC} =6V, 1000hr		0
High-temperature sto	orage life test	150°C, 2000hr		. 0
	High-temperature high- humidity storage test	85°C, 85%RH, 2000hr	308	0
High-temperature high-		85°C, 85%RH, V _{CC} =6V 2000hr	452	0
Humidity resistance	Pressure-cooker test (saturated)	121°C, 2atm, 240hr	439	0
Pressure-cooker test (unsaturated)		130°C, 85%RH, V _{CC} =6V, 500hr	302	0

Table 5 Results of Reliability Tests on the M74HC00FP Series

Test item	Conditions	Qty	Failures
Solderbility test	Wetted with rosin-base flux and immersed up to stoppers for 5sec in 230°C solder bath.	110	0
Soldering thermal stress test (1)	Entire surface immersed in solder (260°C, 10sec, 3times) U High-temperature, high-humidity bias test (85°C, 85%RH, Vcc=6V, 1000hr)	110	0
Soldering thermal stress test (2)	Entire surface immersed in solder (260°C, 10sec, 3times)		
Soldering marinal suess test (2)	Pressure-cooker test (121°C, 2atm, 240hr)	110	0
Soldering thermal stress test (3)	High-temperature high-humidity storage (85℃, 85%RH, 24hr)		
	.		
	Entire surface immersed in solder (260°C, 10sec, 3times)	110	0
and the second of the second of the second	₽		
	High-temperature, high-humidity bias test (85°C, 85%RH, V _{CC} =6V, 1000hr)		ļ
Thermal stress test	Entire surface immersed in solder (260°C, 10sec, 3times)		1
	. ♦		1
	Thermal shock test (-40~+125°C, 15cycles)	110	0
	•		
	Temperature cycle test (−65~+150°C, 500cycles)		
High-temperature, high-humidity bias test	85°C, 85%RH, V _{CC} =6.0V, 1000hr	110	0
Pressure-cooker test (saturated)	121°C, 2atm, 240hr	110	0
Pressure-cooker test (unsaturated)	130°C, 85%RH, V _{CC} =6.0V, 1000hr	110	0
Lead strength test	250g, 90°, bent three times	75	0
High-temperature operation life test	T _a =125℃, V _{CC} =6. 0V, 1000hr	. 190	0
High-temperature storage life test	T _a =150°C, 1000hr	110	0

Table 6 High-Temperature Operation Test Data and Probable Failure Ratio

T-sk-sediki	T4	Failure ratio (FIT)			Ddes
Test conditions	Test results	25℃	40°C	55℃	Remarks
85℃, V _{CC} =6~8.5V, 2000hr	0/936				
125℃, V _{CC} =6~8.5V, 2000hr	1/444			10	
125°C, V _{CC} =6V, 1000hr	0/1368	1.2	3, 5		Activation energy :
125°C, V _{CC} =6V, 3000~5000hr	0/328				0. 6eV
150℃, V _{CC} =6V, 1000hr	0/158				

Table 7 Results of Tests on Periodic Sampling (M74HC00P Series)

Test item		Total Conditions	0.	Failure ratio (FIT)				0
		Test Conditions	Qty	96H	H 240H 500I		1000H	Remarks
High	temperature operation life test	125℃ V _{CC} =6V	1368	0	0	0	. 0	
	temperature storage life test	150℃	792	0	0	0	0	
၌ ၌	High-temperature high-humidity bias test	85°C, 85%RH V _{CC} =6V	912	0	0	0	0	
Humidity resistance	Pressure-cooker test (saturated)	121°C, 2atm, 100%	1824	0	0	0	3*	* 1 : Al corrosion 2 : Icc over
Pressure-cooker test (unsaturated)		130℃, 85%RH V _{CC} =6V	1053	0	0	0	. –	
Tem	perature cycle test (1)	-65~+150℃, 1hr/cycle, 100 cycles	1824			0		
Temperature cycle test (2)		-65~+150℃, 1hr/cycle, 1,000 cycles	528	0				
Solderability test		Wetted with rosin-base flux and immersed up	1056					
Solut	erability test	to stoppers for 5sec in 230°C solder bath.	1056	6 0		. '		

Table 8 Results of Electro-Static Discharge Test

	+	B-11	04.		Breakdown v	voltage	
Туре	Test pin	Polarity	Qty	1k\	/ 2kV	· 3kV	
	Input	±	5	-		-	•
M74HC20P	Output	±	5				
N474110000	Input	±	5			→	
M74HC32P	Output	±	5			→	
1474110400	Input	±	5			→	
M74HC42P	Output	±	5			→	
M74110400D	Input	±	5			→	
M74HC160P	Output	±	5			-	
M74110164B	Input	±	5			-	
M74HC164P	Output	±	5	,		-	

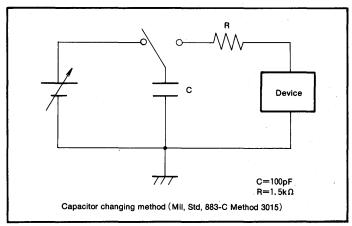


Fig.3 Breakdown voltage test circuit

Table 9	Results of Latchup	Resistance	Tests Using the	Capacitor Charge Method

Туре	Test pin	Polarity	Qty	Test results
	Input	±	5	No latchup
M74HC20P	Output	±	5	,
	Vcc	±	5	,
	Input	±	5	No latchup
M74HC32P	Output	±	5	,
	Vcc	±	5	,
	Input	±	5	No latchup
M74HC42P	Output	±	5	,
	Vcc	+ '	5	,
	Input	±	5	No latchup
M74HC160P	Output	±	5	,
	Vcc	±	5	, ,
	Input	±	5	No latchup
M74HC164P	Output	±	5	,
	Vcc	±	5	,

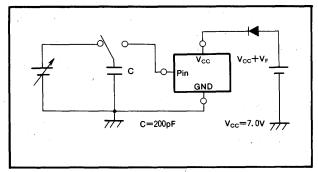


Fig.4 Latchup resistance test circuit (capacitor charing method)

Table 10 Results of Latchup Resistance Tests Using the Current Injection Method

			Input	Outpu	ıt
Type Qty	Qty	+	_	+	_
M74HC20P	5	>300mA	<-300mA	>300mA	<-300mA
M74HC32P	5	"	,	,	"
M74HC42P	5		,	,	,
M74HC160P	5	,	,	,	"
M74HC164P	5	/,	"	,	"

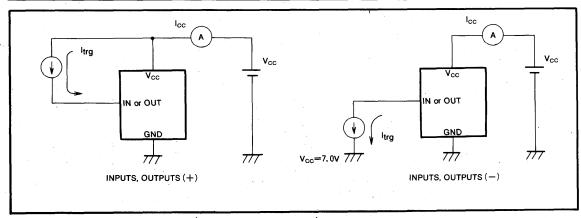


Fig.5 Latchup resistance test circuit (current-injection method)



MITSUBISHI HIGH SPEED CMOS APPLICATION NOTES

1. Introduction

The low power dissipation, high noise margin, and wide supply-voltage and operating temperature ranges of high-speed CMOS devices makes them suitable for digital applications in a wide range of industrial and consumer digital equipment. CMOS circuits differ substantially from bipolar logic such as TTL and LSTTL, and therefore require special care.

2. Handling Unused Pins

Unlike bipolar logic, high-speed CMOS logic involves voltage control: input voltages are applied to transistor gates, and these voltage levels determine whether the transistors are on or off. If CMOS input pins are left floating, the output logic level will fluctuate, and erroneous operation may result. Therefore, all unused input pins should be tied to either $V_{\rm CC}$ or GND as described below:

- (1) NAND and AND Gates
 - Tie unused inputs to V_{CC} or other inputs that are in use.
- (2) NOR and OR Gates Tie unused inputs to GND or other inputs that are in use.
- (3) Other Types of Circuits

Tie other unused inputs to either V_{CC} or GND. Check the function tables in the individual device data sheets to determine the appropriate level.

If and entire functional block is to be left unused, the input pins should be linked to $V_{\rm CC}$ or GND. Otherwise, $I_{\rm CC}$ may increase unpredicatably.

3. AND Ties

As with TTL and LSTTL, the impedance of both low- and high-level outputs of high-speed CMOS logic is low. This means that if output pins of differing states are linked together in "AND" ties, logic outputs will deviate from standard levels, risking misoperation, higher sink currents, and imparied reliability.

4. Output Load Capacitance

In many high-speed CMOS applications, capacitors are connected between I/O pins and either $V_{\rm CC}$ or GND to increase the propagation delay and to remove signal noises. Capacitors of up to 500pF can be connected directly. Larger capacacitors should be linked through a resistor to keep the charging or discharging currents within 20mA. This design will prevent large currents that could cause latchup during power-supply switching or impair reliability.

5. Shorting of Output to V_{CC} or GND

The p- and n-channel transistors used in CMOS logic do not have output-current limiting. If output pins are accidentally shorted to $V_{\rm CC}$ or GND, excessive currents will flow. For example, when an output pin of buffer IC such as M74HC240 is connected to GND, about 100mA current

flows. When the output is tied to $V_{\rm CC}$, about 80mA current flows. These currents may cause latchup, overheating, damage to the IC's internal wiring, and loss of reliability. Therefore, output pins should never be tied to $V_{\rm CC}$, GND, or any other fixed voltage level.

6. Power Supply Lines

When high-speed CMOS logic is quiescent, the supply current is extermely small. This would seem to indicate that the power-supply capacitance could also be low; however, when CMOS logic changes state, large transient current spikes flow, just as in TTL and LSTTL devices. To soak up such spikes, the impedances of both the power supply and the supply lines must be low. One method to lower this supply-line impedance is to connect a $0.01 \sim 0.22 \mu F$ plastic-film or ceramic capacitor with good high-frequency characteristics between the $V_{\rm CC}$ and GND lines. $10 \sim 100 \mu F$ electrolytic or tantalum capacitors should also be connected on each printed-circuit board.

The power dissipation current varies widely with the operating frequency, supply voltage, capacitive load, supply voltage, and input signal rise and fall times. The effect of this factors should be considered when designing the power supply.

When CMOS devices are being used with high-current drivers, separate power supplies should be used for the logic and driver circuit, and common loads should be avoided.

7. Preventing Damage by Static Electricity

Static electricity is generated under low-humidity conditions by the friction of clothing, containers and other objects. Most MOS ICs are easily damaged by high-voltage static-electric discharges, but through use of protective circuits Mitshbishi high-speed CMOS devices can tolerate static voltages of over 3kV. This places them on equal footing with TTL and LSTTL devices.

The protection diodes that prevent static damage can to tolerated only limited forward- and reverse-bias currents. Large energy inputs should be avoided, as they will destroy there diodes and thin oxide layers at the transistor input gates. The following measures are recommended to prevent this type of damage.

- To prevent static damage during shipping, all ICs are shipped in conductive tubes. After receipt, the ICs should always be stored in conductive tubes or other conductive containers.
- (2) Static charges on the body or clothing should be drained off by grounding through 100k Ω ~1M Ω resistors
- (3) All assembly tables, insertion machines, and measuring instruments, and other objects that will come in contact with the ICs should be grounded.



MITSUBISHI HIGH SPEED CMOS APPLICATION NOTES

- (4) Soldering irons and baths must have power-supply insulation resistances of over 10M Ω to prevent powersupply leakage to the ICs. This equipment should also be grounded.
- (5) Printed-circuit boards with ICs installed should be protected from shock, vibration, and friction. To keep potentials from building up, the boards should stored in conductive envelopes, or the terminals should be shorted together.
- (6) The humidity of the transport, storage and assembly environments should always be maintained at safe levels.

8. Latchup

The CMOS circuit structure inherently cointains parasitic bipolar transistors. These transistors function as thyristors (SCRs): when they are triggered by an external surge, they turn on, causing a current to flow from V_{CC} to GND. Even after the trigger current ceases, this current continues to

flow. The current is very large, and can easily damage or destroy the IC. For this reason, the phenomenon is called "latchup".

8-1 The Latchup Mechanism

Fig.1 shows the structure of a CMOS inverter and its parasitic bipolar transistors, and Fig.2 the thyristor circuit that results in latchup. T_{Γ_1} and T_{Γ_2} have pnpn thyristor structures. If any one of T_{Γ_3} , T_{Γ_4} , T_{Γ_5} , or T_{Γ_6} turn on due to a current surge, a base current will flow to T_{Γ_1} or T_{Γ_2} , initiating latchup.

The following external factors can initiate latchup:

- Input voltage (V₁) exceeds supply voltage (V_{CC}).
 V₁>V_{CC}
- (2) Input voltage (V_I) falls below GND. V_I<GND
- (3) Output voltage (V_O) exceeds supply voltage (V_{CC}).V_O>V_{CC}
- (4) Output voltage (V_O) falls below GND. V_O < GND</p>
- (5) Supply voltage (V_{CC}) becomes excessive.

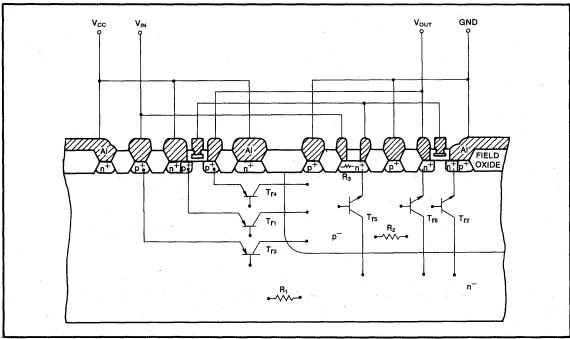


Fig.1 A CMOS inverter and its parasitic transistors

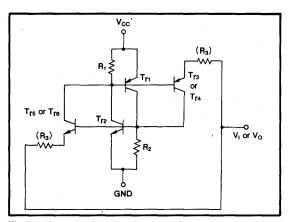


Fig.2 The parasitic transistor circuit that causes latchup

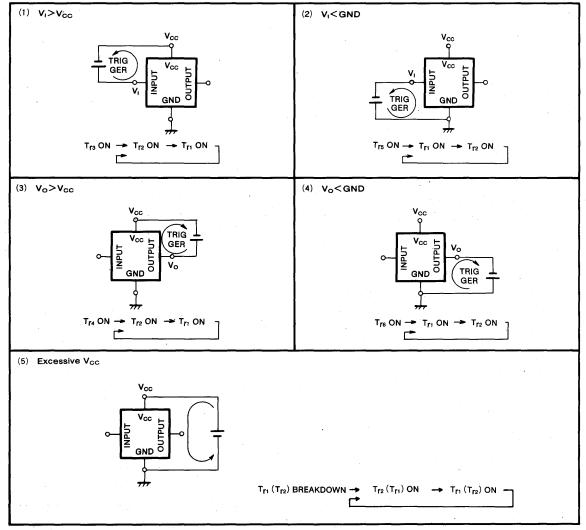


Fig.3 Latchup mechanisms

Note: The recirculating arrow indicates latchup.

8-2 Prevention of Latchup

The following steps can be taken to prevent the five conditions listed in section 8-1 from arising.

(1) $V_1 > V_{CC}$ and $V_1 < GND$

When using two power supplies

When two supplies are used to power CMOS devices, the differing rise times can readily cause latchup. This problem is avoided by connecting series resistor R to limit the maximum current to 20mA (Fig.4).

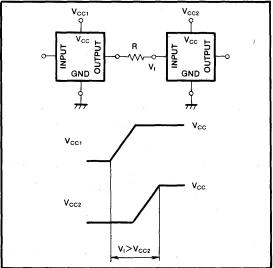


Fig.4 Preventing latchup when dual power supplies are used

When using a differential circuit

When a differential circuit is used, the input voltage V_I may exceed V_{CC} or drop below GND, causing latchup. This danger is avoided by connecting voltage-clamp diodes and current-limiting resistors (Fig. 5).

9. Mechanical and Thermal Stress

Cutting or deforming the external leads can result in lead breakage or humidity-induced corrosion. Mechanical stress should be avoided when mounting the ICs.

The component materials of ICs have widely varying thermal-expansion coefficients, so rapid temperature changes, extended soldering and other thermal stresses should be avoided as far as possible. Such stresses can damage the semiconductors or break the internal wiring.

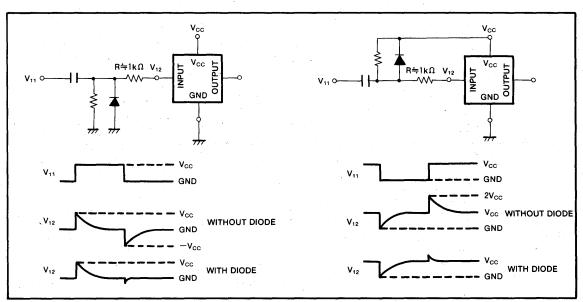
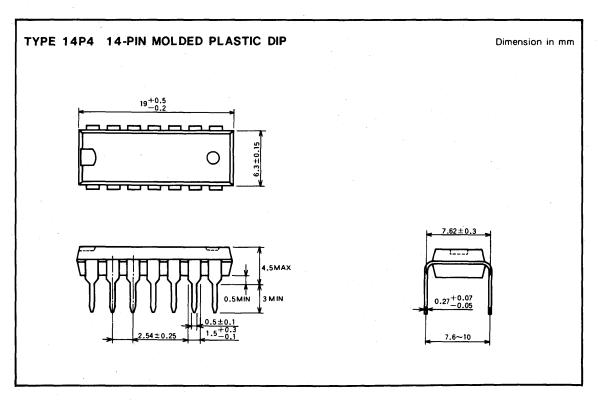
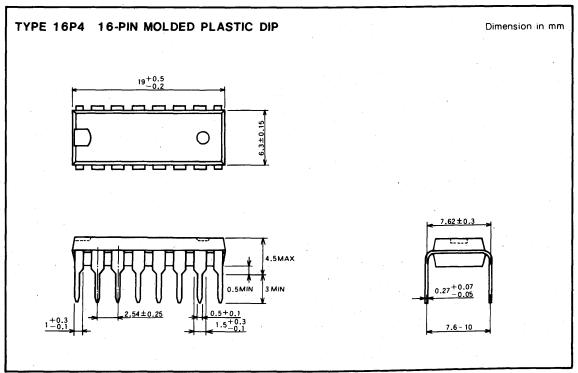


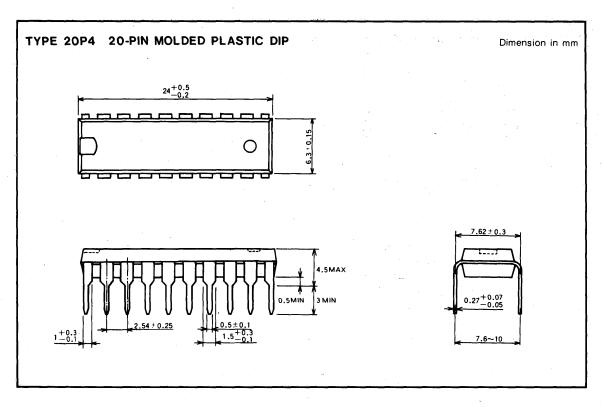
Fig.5 Preventing latchup when a differential circuit is used



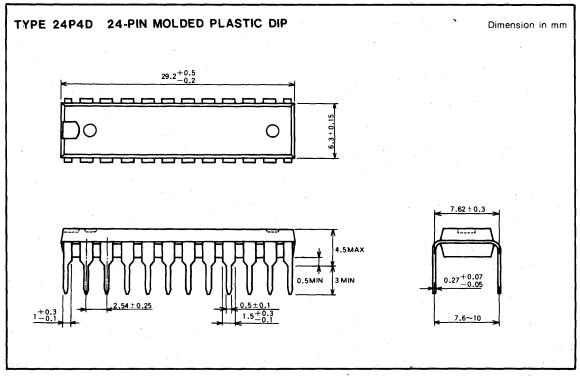
MITSUBISHI HIGH SPEED CMOS PACKAGE OUTLINES

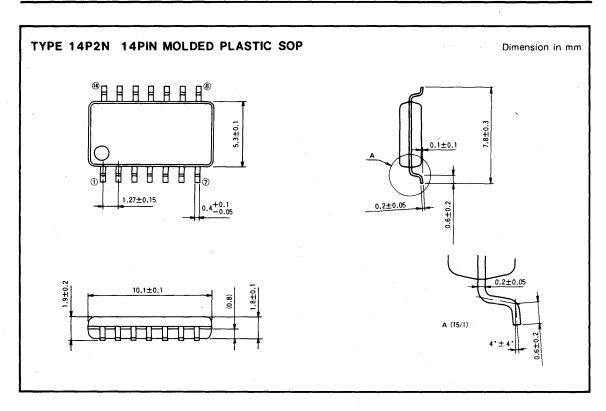


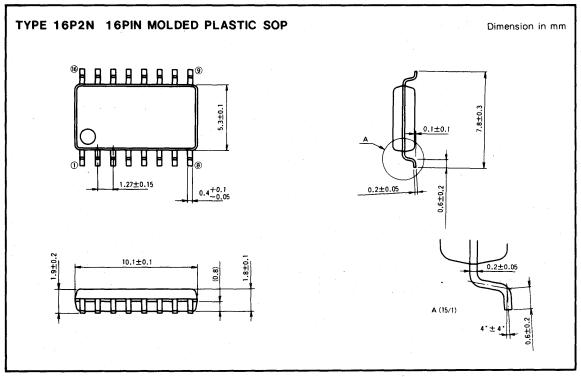


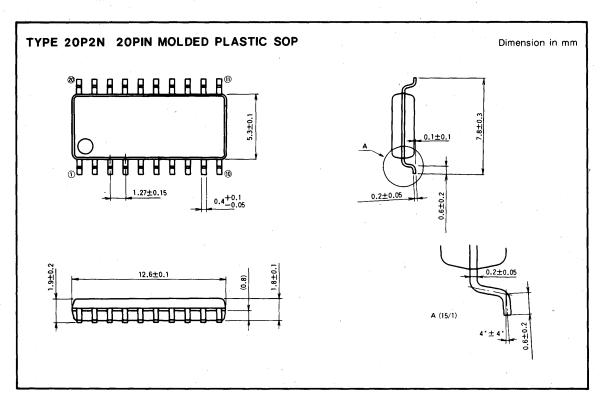


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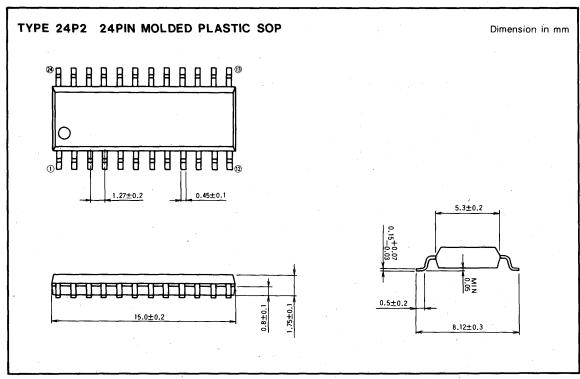




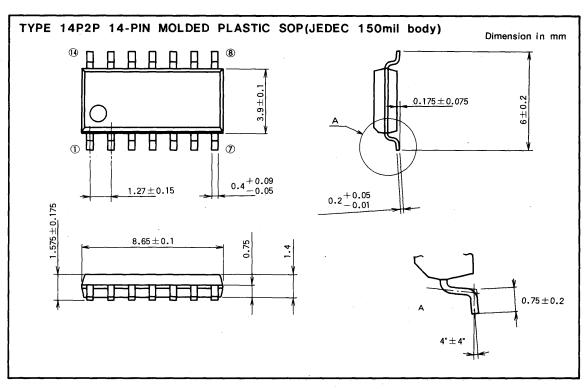


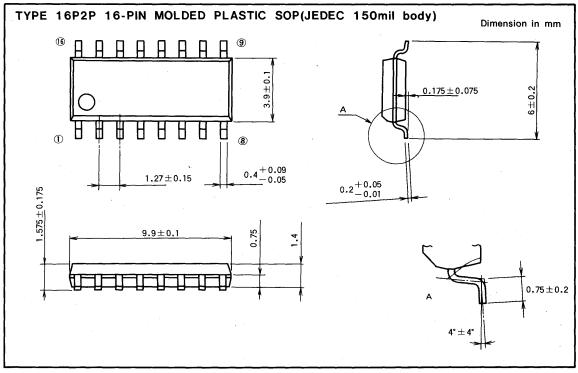


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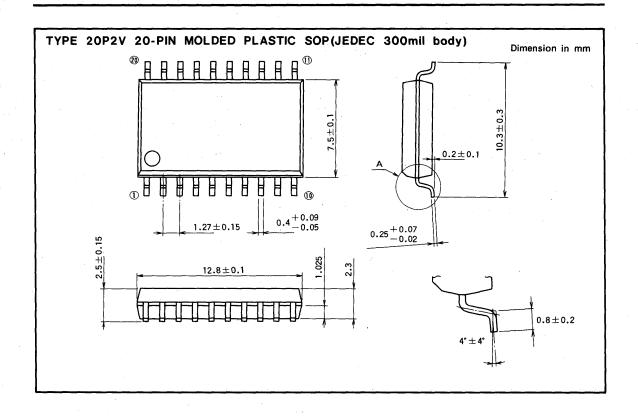


MITSUBISHI HIGH SPEED CMOS PACKAGE OUTLINES





MITSUBISHI HIGH SPEED CMOS PACKAGE OUTLINES



DATASHEETS 2



MITSUBISHI HIGH SPEED CMOS

M74HC00P/FP/DP

QUADRUPLE 2-INPUT POSITIVE NAND GATE

DESCRIPTION

The M74HC00 is a semiconductor integrated circuit consisting of four 2-input positive-logic NAND gates, usable as negative-logic NOR gates.

FEATURES

- High-speed: 8ns typ. (C_L=15pF, Vcc=5V)
- Low power dissipation: 5µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads*
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=-40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

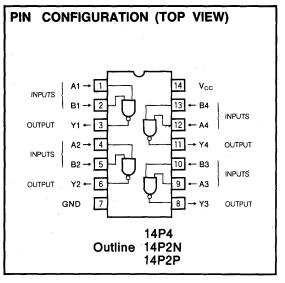
Use of silicon gate technology allows the M74HC00 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS00.

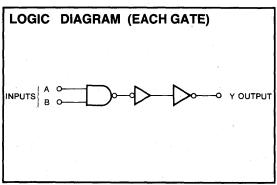
Buffered outputs Y improve input-to-output transfer characteristics and reduce to a minimum output impedance variations with respect to input voltage variations.

When both inputs A and B are high, the output Y will become low, and when at least one of the inputs is low, the output Y will become high.

FUNCTION TABLE

Inp	Output	
Α	В	Y
L	L	н
н	L	н
L	Н	н
н	Н	L





ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85 ^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit	
Vcc	Supply voltage		−0.5∼+7.0	V	
Vi	Input voltage		-0.5~V _{cc} +0.5	V	
Vo	Output voltage		-0.5~V _{cc} +0.5	V	
		V ₁ < 0V	-20	mA	
lık	Input protection díode current	V _I > V _{CC}	20	IIIA	
	Outro American Manager and American	V _o < 0V	-20	mA	
Ток	Output parasitic diode current	V _o > V _{cc}	20	IIIA	
lo	Output current per output pin		±25	mA	
Icc	Supply/GND current	V _{CC} , GND	±50	mA	
Pd	Power dissipation	(Note 1)	500	mW	
Tstg	Storage temperature range		-65~+150	ဗ	

Note 1 : M74HC00FP, $T_a = -40 \sim +60^{\circ}$ C and $T_a = 60 \sim 85^{\circ}$ C are derated at -6mW/°C. M74HC00DP, $T_a = -40 \sim +50^{\circ}$ C and $T_a = 50 \sim 85^{\circ}$ C are derated at -5mW/°C.



CARREST OF THE PROPERTY OF THE

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85 c)$

Symbol	Parameter			Limits				
Syllibol			Min	Тур	Max	Unit		
Vcc	Supply voltage	Supply voltage			6	V :		
V _I	Input voltage	0		Vcc	V			
Vo	Output voltage	Output voltage			Vcc	V		
Topr	Operating temperature ra	ange	-40		+85	င		
		V _{CC} = 2.0V	0		1000			
tr, tf	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns		
	$V_{CC} = 6.0V$		0		400			

ELECTRICAL CHARACTERISTICS

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							Limits			
Symbol	Parameter	Test	conditions		25°C			-40~+85°C		Unit
			Vcc		Min	Тур	Max	Min	Max	1
		V = 0.1V V	Vo = 0.1V, Vcc-0.1V		1.5			1.5		
VIH	High-level input voltage	1	5—0 . 1 V	4.5	3.15	}		3. 15		V
	ļ	$ I_0 = 20\mu A$		6.0	4.2		1	4.2		-
		V -V 01					0.5		0.5	
V _I ∟	Low-level input voltage	$V_0 = V_{CC} - 0.1$,	4.5			1.35		1.35	V
1		1101 = 20µA	$ I_0 = 20\mu A$				1.8		1.8	
			$I_{OH} = -20\mu A$	2, 0	1.9			1.9		
}		(·	$I_{OH} = -20\mu A$	4.5	4.4	ł	[4.4	}	
V _{OH}	High-level output voltage	$V_{l} = V_{lH}, V_{lL}$	$I_{OH} = -20\mu A$	6.0	5.9		Į	5.9		V
i		1	I _{OH} = -4.0mA	4.5	4. 18			4. 13		
		}	$I_{OH} = -5.2 mA$	6.0	5. 68	1	1	5. 63		
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
ĺ		1	$I_{OL} = 20 \mu A$	4.5	ļ	[.	0.1		0.1	
VOL	Low-level output voltage	$V_I = V_{IH}$	$I_{OL} = 20 \mu A$	6.0		ł	0.1	1	0.1	V
l .	1		I _{OL} = 4.0mA	4.5			0. 26		0.33	
			IoL = 5. 2mA	6.0	ļ		0.26		0.33	
I _{IH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	
l _{IL}	Low-level input current	$V_i = 0V$	$V_1 = 0V$				-0.1		-1.0	μA
lcc	Quiescent supply current	$V_{i} = V_{CC}$, GND	$I_0 = 0\mu A$	6.0			1.0		10.0	μA

QUADRUPLE 2-INPUT POSITIVE NAND GATE

SWITCHING CHARACTERISTICS ($v_{cc} = 5v$, $\tau_a = 25^{\circ}$)

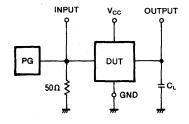
Symbol	Parameter	Test conditions		Unit		
Symbol	, apanietei	rest conditions	Min	Тур	Max	Unit
t _{TLH}	Low-level to high-level and high-level to low-level				10	
t _{THL}	output transition time	C ₁ = 15pF (Note 3)			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	$C_{L} = 15pr (Note 3)$			15	
t _{PHL}	output propagation time				15	ns

SWITCHING CHARACTERISTICS ($v_{cc} = 2\sim 6v$, $\tau_a = -40\sim +85\%$)

		Test conditions		Limits					
Symbol	Parameter			25℃			-40~+85℃		Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0			75		95	
t _{TLH}	Low-level to high-level and		4.5		l	15		19	,
	Low lover to high lover and		6.0			13		16	
	high-level to low-level		2.0			75		95	ns
t _{THL} output t	output transition time		4.5			15		19	
			6.0			13		16	ļ
		$C_L = 50 pF \text{ (Note 3)}$	2.0			90		113	
t _{PLH}	Low-level to high-level and		4.5			18		23	
	_	- 1	6.0			15		19	
	high-level to low-level	-	2.0			90		113	ns
t _{PHL}	output propagation time		4.5			18	Į.	23	
-			6.0		(15	1	19	
Cı	Input capacitance					10		10	pF
C _{PD}	Power dissipation capacitance (Note 2)				25				pF

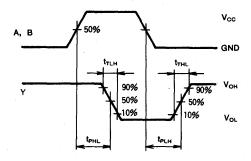
Note 2: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per gate)
The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$

Note 3: Test Circuit



- (1) The pulse generator (PG) has the following characteristics (10%~90%): t_f = 6ns, t_f = 6ns
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



QUADRUPLE 2-INPUT POSITIVE NAND GATE WITH LSTTL-COMPATIBLE INPUTS

DESCRIPTION

The M74HCT00P is a semiconductor integrated circuit consisting of four 2-input positive-logic NAND gates, usable as negative-logic NOR gates.

FEATURES

- TTL level input V_{IL} = 0.8V max V_{IH} = 2.0V min
- High-speed: 8ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5µW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- Capable of driving 10 74LSTTL loads
- Wide operating temperature range: Ta=-40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HCT00 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS00.

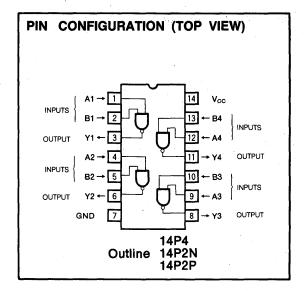
As the inputs are TTL level, the device can be used as a level converter from LSTTL to high-speed CMOS. In that case, no pull-up resistors are required.

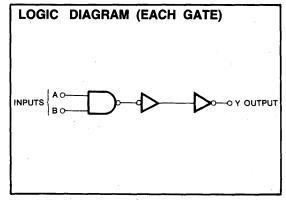
Buffered Y outputs improve input-to-output transfer characteristics and reduce output impedance variations to a minimum with respect to input voltage variations.

When both inputs A and B inputs are high, the output Y will become low, and when at least one of the inputs is low, the output Y will become high.

FUNCTION TABLE

Inp	uts	Output
Α	В	Υ
L		н
Н	L	Н
L	Н	Н
Н	Н	L







QUADRUPLE 2-INPUT POSITIVE NAND GATE WITH LSTTL-COMPATIBLE INPUTS

ABSOLUTE MAXIMUM RATINGS $(\tau_a = -40 \sim +85^{\circ}C)$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit	
V _{cc}	Supply voltage		-0.5~+7.0	V	
Vi	Input voltage		-0.5~V _{cc} +0.5	V	
Vo	Output voltage		-0.5~V _{cc} +0.5	V	
	Input protection diode current	V ₁ < 0V	-20	mA	
ик		V _I > V _{CC}	20		
	Output managitic diada aumant	V ₀ < 0V	-20		
lok	Output parasitic diode current	$V_0 > V_{CC}$	20	mA	
lo	Output current, per output pin		±25	mA	
Icc	Supply/GND current	V _{CC} , GND	±50	mA	
Pd	Power dissipation	(Note 1)	500	mW	
Tstg	Storage temperature range		-65∼+150	°C	

Note 1 : M74HCT00FP, T $_{\rm a}=-40\sim+60^\circ$ C and T $_{\rm a}=60-85^\circ$ C are derated at -6mW/°C. M74HCT00DP, T $_{\rm a}=-40\sim+50^\circ$ C and T $_{\rm a}=50-85^\circ$ C are derated at -5mW/°C.

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85^{\circ}\text{C})$

Comple ed	Parameter			Limits				
Symbol			Min	Тур	Max	Unit		
V _{CC}	Supply voltage	4.5	4.5		V			
V _I	Input voltage		0	0		٧		
Vo	Output voltage		0		Vcc	٧		
Topr	Operating temperature ra	ange	-40		+85	က်		
	Input risetime, falltime	$V_{CC} = 2.0V$	0		1000			
t _r , t _f		$V_{CC} = 4.5V$	0	1.	500	ns		
	$V_{CC} = 6.0V$		0		400			

ELECTRICAL CHARACTERISTICS ($v_{cc} = 5v \pm 10\%$, unless otherwise noted)

		Test conditions		Limits					
Symbol	Parameter			25℃			-40~+85℃		Unit
				Min	Тур	Max	Min	Max	
V _{IH}	High-level input voltage	$V_0 = 0.1V, V_{CC} = 0.1V$ $ I_0 = 20\mu A$		2.0			2.0		V
VIL	Low-level input voltage	V _{cc} -0.1V t ₀ = 20μA				0.8		0.8	, v
			$I_{OH} = -20 \mu A$	V _{cc} -0.1			V _{cc} -0.1		
V_{OH}	High-level output voltage	$V_i = V_{iH}, \ V_{iL}$	$I_{OH} = -4.0 \text{mA}, V_{CC} = 4.5 \text{V}$	4.18			4.13		V
			$I_{OH} = -4.8 \text{mA}, V_{CC} = 5.5 \text{V}$	5.18			5.13		
			$I_{OL} = 20 \mu A$		-	0.1		0.1	
VoL	Low-level output voltage	$V_I = V_{IH}$	I _{OL} = 4.0mA, V _{CC} = 4.5V			0.26		0.33	V
			$I_{OL} = 4.8 \text{mA}, V_{CC} = 5.5 \text{V}$			0.26		0.33	
I _{IH}	High-level input current	$V_1 = 5.5V$				0.1		1.0	
I _{IL}	High-level input current	$V_1 = 0V$				-0.1		-1.0	μA
Icc	Quiescent supply current	$V_i = V_{CC}$, GND,	$I_0 = 0\mu A$			1.0		10.0	μA
Δlcc	Maximum quiescent state supply current	$V_1 = 2.4V, 0.4V$	(Note 2)			2.7		2.9	mA

Note $\,2\,$: Only one input is set at this value and all others are fixed at V_{CC} or GND.

QUADRUPLE 2-INPUT POSITIVE NAND GATE WITH LSTTL-COMPATIBLE INPUTS

SWITCHING CHARACTERISTICS $(V_{cc} = 5V, T_a = 25\%)$

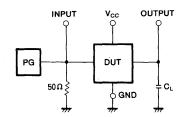
Combal	Parameter	Test conditions		Unit		
Symbol	Parameter	rest conditions	Min	Тур	Max) Unit
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time	0 -15-5 (Not- 4)			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = 15pF (Note 4)			15	ns
tpHL	output propagation time				15	ns

SWITCHING CHARACTERISTICS ($v_{cc} = 5v \pm 10\%$, $T_a = -40 \sim +85^{\circ}C$)

				1.				
Symbol	Parameter	Test conditions	25℃			-40~+85°C		Unit
			Min	Тур	Max	Min	Max	
t _{TLH}	Low-level to high-level and high-level				15		19	ns
t _{THL}	to low-level output transition time	50.5(1)(1)			15		19	ns
t _{PLH}	Low-level to high-level and high-level	$C_L = 50 pF \text{ (Note 4)}$			18		24	ns
t _{PHL}	to low level output propagation time				18		24	ns
Cı	Input capacitance				10		10	pF
C _{PD}	Power dissipation capacitance (Note 3)							ρF

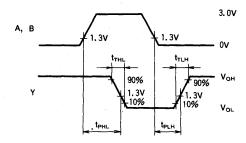
Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per gate)
The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$

Note 4: Test Circuit



- (1) The pulse generator (PG) has the following characteristics (10%~90%): t_f = 6ns, t_f = 6ns
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



MITSUBISHI HIGH SPEED CMOS

M74HC02P/FP/DP

QUADRUPLE 2-INPUT POSITIVE NOR GATE

DESCRIPTION

The M74HC02 is a semiconductor integrated circuit consisting of four 2-input positive-logic NOR gates, usable as negative-logic NAND gates.

FEATURES

- High-speed: 8ns typ. (C_L=15pF, Vcc=5V)
- Low power dissipation: 5μW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

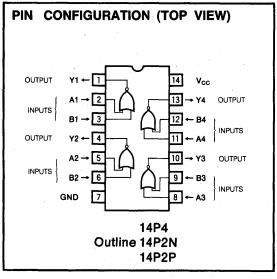
Use of silicon gate technology allows the M74HC02 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS02.

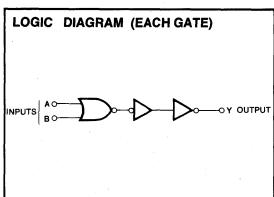
Buffered outputs Y improve input-to-output transfer characteristics and reduce to a minimum output impedance variations with respect to input voltage variations.

When both inputs A and B are low, the output Y will become high, and when at least one of the inputs is high, the output Y will become low.

FUNCTION TABLE

Inp	uts	Output		
Α	В	Υ		
. L	L L			
н	H L			
L	н	L		
н	н н			





ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85$ °C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit	
V _{CC}	Supply voltage		−0.5~+7.0	. V	
V ₁	Input voltage		-0.5~V _{cc} +0.5	٧.	
Vo	Output voltage		-0.5~V _{cc} +0.5	V	
		V ₁ < 0V			
l _{IK}	Input protection diode current $V_1 > V_{CC}$		20	mA	
		V ₀ < 0V	-20		
lok	Output parasitic diode current	Vo > Vcc	20	mA	
lo	Output current per output pin		±25	mA	
Icc	Supply/GND current	V _{CC} , GND	±50	mA	
Pd	Power dissipation	(Note 1)	500	mW	
Tstg	Storage temperature range		-65~+150	°C	

Note 1 : M74HC02FP, $T_a=-40\sim+60^\circ\text{C}$ and $T_a=60\sim85^\circ\text{C}$ are derated at -6mW/°C. M74HC02DP, $T_a=-40\sim+50^\circ\text{C}$ and $T_a=50\sim85^\circ\text{C}$ are derated at -5mW/°C.



QUADRUPLE 2-INPUT POSITIVE NOR GATE

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85\%)$

Ob1				Limits				
Symbol	Pai	Parameter		Тур	Max	Unit		
Vcc	Supply voltage	2		6	٧			
V ₁	Input voltage	0		Vcc	٧			
v _o	Output voltage	0		Vcc	V			
Topr	Operating themperature	ange	-40		+85	°C		
		V _{CC} = 2.0V	0		1000			
t _r , t _f	Input risetime, falltime	V _{CC} = 4.5V	0		500	ns		
	$V_{CC} = 6.0V$		0		400	1		

							Limits			
Symbol	Parameter	Test	conditions		,	25℃		−40~	+85℃	Unit
			V _{CC}		Min	Тур	Max	Min	Max	
		V _O = 0.1V		2.0	1.5			1.5		
V _{IH}	High-level input voltage	$ V_0 = 0.1V$ $ I_0 = 20\mu A$		4.5	3. 15		}	3. 15		v
		$ 10\rangle = 20\mu\text{A}$		6.0	4.2			4.2		
		V =0.1V V	- 0.11/	2.0			0.5		0.5	
\ \V _{IL}	Low-level input voltage		$V_0 = 0.1V, V_{CC} = 0.1V$ $ I_0 = 20\mu A$			ļ:	1.35		1.35	, v
		$ 1_0 = 20\mu\text{A}$					1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
1			$I_{OH} = -20 \mu A$	4.5	4.4		·	4.4		
V _{OH}	High-level output voltage	$V_i = V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		V ·
į.			$I_{OH} = -4.0 \text{mA}$. 4. 5	4.18	}		4.13		
			$I_{OH} = -5.2 \text{mA}$	6.0	5. 68			5. 63	.*	
			$I_{OL} = 20 \mu A$	2.0			0. 1		0.1	,
1			$I_{OL} = 20 \mu A$	4.5	Ì .	1	0.1	,	0.1	
VoL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0. 1		0. 1	· V
			I _{OL} = 4.0mA	4.5			0.26		0.33	
			I _{OL} = 5. 2mA	6.0			0.26		0.33	
l _{iH}	High-level input current	V ₁ = 6V		6.0			0. 1		1.0	μA
l _{IL}	Low-level input current	V ₁ = 0V		6.0			—0. 1		-1.0	μΑ
loc	Quiescent supply current	VI = VCC, GND	$I_0 = 0 \mu A$	6.0			1.0		10.0	μA

QUADRUPLE 2-INPUT POSITIVE NOR GATE

SWITCHING CHARACTERISTICS (Vcc = 5V, Ta = 25°C)

O b1	Parameter	Test conditions	Limits			Unit
Symbol		rest conditions	Min	Тур	Max) Olik
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time	C _L = 15pF (Note 3)			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	CL = 15pr (Note 3)			15	ns
t _{PHL}	output propagation time	·			15	ns

SWITCHING CHARACTERISTICS ($V_{cc} = 2\sim 6V$, $T_a = -40\sim +85^{\circ}C$)

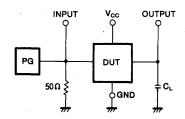
						Limits			i
Symbol	Parameter	Test conditions		25℃			-40~+85℃		Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max]
		1	2.0			75		95	
t _{TLH}	Low-level to high-level and		4.5		1	15		19	ns
			6.0			13		-16	
	high-level to low-level		2.0			75		95	
t _{THL} output	output transition time	*	4.5			15		19	ns
	1	50.7(00)	6.0			13		16	
		$C_L = 50 pF \text{ (Note 3)}$	2.0			90		113	
t _{PLH}	Low-level to high-level and		4.5			18		23	ns
	1		6.0			15		19	
	high-level to low-level		2.0			90		113	
t _{PHL}	output propagation time		4.5			18		23	ns
PHL		6.0			15		19		
Cı	Input capacitance					10		10	pF
C _{PD}	Power dissipation capacitance (Note 2)				31				pF

Note 2: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per gate)

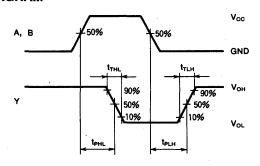
The power dissipated during operation under no-load conditions is calculated using the following formula:

P_D = C_{PD} · V_{CC}² · f₁+I_{CC} · V_{CC}

Note 3 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.





M74HC03P/FP/DP

QUADRUPLE 2-INPUT POSITIVE NAND GATE WITH OPEN-DRAIN OUTPUTS

DESCRIPTION

The M74HC03 is a semiconductor integrated circuit consisting of four 2-input positive-logic NAND gates usable as negative-logic NOR gates, with open-drain outputs.

FEATURES

- Open-drain outputs
- High-speed: 10ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5µW/package, max
 (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

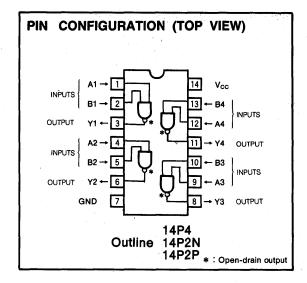
Use of silicon gate technology allows the M74HC03 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS03.

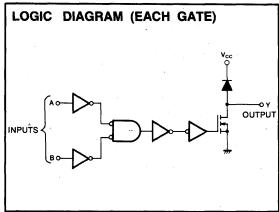
Open-drain outputs allow a versatile selection of high output impedances by connecting external load resistors. This enalbes "AND ties" which are not possible using normal gates. When both inputs A and B are high, the output Y will become low, and when at least one of the inputs is low, Y will become high.

Note that this IC differs from the 74LS03 and a voltage higher than V_{CC} can not be applied to the output.

FUNCTION TABLE

Inpi	uts	Output
Α	В	Υ
L	L	н
L	н	Н
Н	L	Н
Н	Н	L





QUADRUPLE 2-INPUT POSITIVE NAND GATE WITH OPEN-DRAIN OUTPUTS

ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85$ °C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
Vi	Input voltage		-0.5~V _{cc} +0.5	·V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
		V ₁ < 0V	-20	
lik	Input protection diode current	V _I > V _{CC}	20	mA
	0.4.4	V _o < 0V	-20	
lok	Output parasitic diode current	Vo > Vcc	20	mA
lo	Output current per output pin		+25	mA -
loc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		-65~+150	င

Note 1 : M74HC03FP, $T_a=-40\sim+60$ °C and $T_a=60\sim85$ °C are derated at -6mW/°C. M74HC03DP, $T_a=-40\sim+50$ °C and $T_a=50\sim85$ °C are derated at -5mW/°C.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85^{\circ}C)$

Symbol	Parameter		L			
Зупрог	Fai	ameter	Min	Тур	Max	Unit
V _{CC}	Supply voltage		2		6	V
Vi	Input voltage		0		Vcc	٧
V _o	Output voltage		0		Vcc	٧
Topr	Operating temperature ra	ange	-40		+85	°
		$V_{CC} = 2.0V$	0		1000	
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns
		$V_{CC} = 6.0V$	0		400	

Symbol	Parameter	Te	st conditions			25℃			+85℃	Unit
		V _{cc} (V)		V _{cc} (V)	Min	Тур	Max	Min	Max]
		V = 0 1V X	$V_0 = 0.1V$, $V_{CC} = 0.1V$		1.5			1.5		
VIH	High-level input voltage	$ I_0 = 20\mu A$		4.5	3. 15	1		3.15	-	v
				6.0	4.2			4.2		
		$V_0 = V_{CC} - 0$.	11/	2.0			0.5		0.5	
V _{IL}	Low-level input voltage	$ V_0 - V_{CC} - 0.$ $ V_0 = 20 \mu A$	ı v	4.5			1.35		1.35	v
		Πο1 — 20μΑ		6.0			1.8		1.8	
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
			$I_{OL} = 20 \mu A$	4.5			0.1		0.1	
VoL	Low-level output voltage	$V_i = V_{iH}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	v
		,	I _{OL} = 4.0mA	4.5			0. 26		0.33	
			I _{OL} == 5. 2mA	6.0			0. 26	* .	0.33	
I _{IH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μА
IIL	Low-level input current	$V_i = 0V$		6.0			-0.1		-1.0	μΑ
lo '	Maximum output leakage current	$V_i = V_{iH}, \ V_{iL},$	$V_0 = V_{CC}$	6.0			0.5		5.0	
·o .	waximum output leakage current	$V_{i} = V_{iH}, \ V_{iL},$	$V_i = V_{iH}, \ V_{iL}, \ V_O = GND \qquad \qquad 6.0$				-0.5		-5.0	μA
Icc	Quiescent supply current	VI = VCC, GN	ID, $I_0 = 0\mu A$	6.0			1.0		10.0	μΑ

QUADRUPLE 2-INPUT POSITIVE NAND GATE WITH OPEN-DRAIN OUTPUTS

SWITCHING CHARACTERISTICS ($v_{cc} = 5v$, $\tau_a = 25^{\circ}$ C)

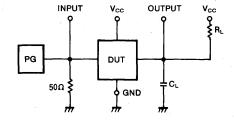
Symbol	Parameter	Test conditions		Unit		
Symbol	Parameter	rest conditions	Min	Тур	Max	Onit
t _{THL}	High-level to low-level output transition time	$R_L = 1k\Omega$ $C_L = 15pF (Note 3)$			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	$R_L = 1k\Omega$, $C_L = 5pF$ (Note 3)			. 20	ns
t _{PHL}	output propagation time	$R_L = 1 k\Omega$, $C_L = 15 pF$ (Note 3)			20	ns

SWITCHING CHARACTERISTICS ($V_{cc} = 2\sim6V$, $T_a = -40\sim+85^{\circ}C$)

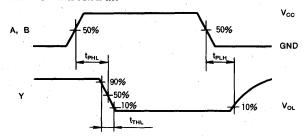
		Test conditions				Limits	Limits					
Symbol	Parameter				25℃			+85℃	Unit			
			V _{cc} (V)	Min	Тур	Max	Min	Max				
			2.0			75		95				
t _{THL}	High-level to low-level		4.5	1		15		19	ns			
	output transition time		6.0	ļ	}	13	1	16				
		1	2.0			125		158				
t _{PLH}	t _{PLH} Low-level to high-level and	$R_L = 1k\Omega$	4.5	1	1	25	, ,	32	ns			
	Note that the second	C _L = 50pF (Note 3)	6.0			21		27				
	high-level to low-level	. *	2.0			125		158				
t _{PHL}	output propagation time		4.5	1		25	1	32	ns			
			6.0			21		27	_			
Cı	Input capacitance					10		10	pF			
Со	Output capacitance	A or B = GND				10		10	pF			
C _{PD}	Power dissipation capacitance (Note 2)				11				pF			

Note 2: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per gate)
The power dissipation during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$

Note 3: Test Circuit



- (1) The pulse generator (PG) has the following characteristics (10% \sim 90%): $t_f = 6$ ns, $t_f = 6$ ns
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.



MITSUBISHI HIGH SPEED CMOS

M74HC04P/FP/DP

HEX INVERTER

DESCRIPTION

The M74HC04 is a semiconductor integrated circuit consisting of six inverters.

FEATURES

- High-speed: 10ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide supply voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

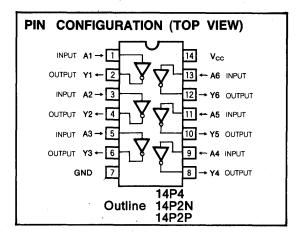
General purpose, for use in industrial and consumer digital equipment.

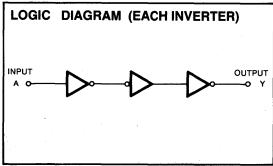
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC04 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS04.

Buffered outputs Y improve input-to-output transfer characteristics and reduce to a minimum output impedance variations with respect to input voltage variations.

When input A is high, the output Y will become low, and when input A is low, the output Y will become high.





FUNCTION TABLE

Input	Output
Α	Y
L	н
Н	L

ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85 \degree$ C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	·V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
	Input protection diode current	V ₁ < 0V	-20	
l _{iK}	input protection diode current	V _I > V _{CC}	20	mA
	Outs. A secolate disease	V _o < 0V	-20	
lok	Output parasitic diode current	V _o > V _{cc}	20	mA
lo	Output current per output pin		±25	mA
I _{cc}	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65~+150	င

Note 1 : M74HC04FP, $T_a=-40\sim+60^\circ$ C and $T_a=60\sim85^\circ$ C are derated at $-6mW/^\circ$ C. M74HC04DP, $T_a=-40\sim+50^\circ$ C and $T_a=50\sim85^\circ$ C are derated at $-5mW/^\circ$ C.

HEX INVERTER

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85 \degree C)$

Symbol	De	rameter		Limits				
Symbol	Pa	Min	Тур	Max	Unit			
Vcc	Supply voltage		2		6	V		
V,	Input voltage		0	-	Vcc	V		
V _o	Output voltage		0		Vcc	· V		
Topr	Operating temperature re	inge	-40		.+85	ొ		
		$V_{CC} = 2.0V$	0		1000			
t _r , t _f	Input risetime, falltime	V _{CC} = 4.5V	0		500	ns		
	$V_{CC} = 6.0V$		0		400			

ELECTRICAL CHARACTERISTICS

电压力设计器 医抗结肠 医皮脂酶 网络阿拉特森美国德

						Limits				
Symbol	Parameter	Test	Test conditions		25℃			-40~+85℃		Unit
				V _{cc} (V)	Min	Тур	Max	Min	Max	1 .
		V = 0.1V		2.0	1.5			1.5		
VIH	High-level input voltage	$V_0 = 0.1V$		4, 5	3, 15		-	3.15		V
	$ I_0 = 20\mu A$	$ I_0 = 20\mu A$		6.0	4. 2			4.2		
				2.0			0.5		0.5	
VIL	Low-level input voltage	$V_0 = V_{CC} - 0.1V$		4.5			1.35		1.35	V
		$ I_0 = 20\mu A$		6.0			1.8	ļ	1.8	
			$I_{OH} = -20 \mu A$	2.0	1.9			1.9		
			$I_{OH} = -20 \mu A$	4.5	4. 4			4.4		
V _{OH}	High-level output voltage	$V_I = V_{IL}$	$I_{OH} = -20\mu A$	6.0	5. 9		1	5.9		V
			I _{OH} = -4.0mA	4.5	4.18			4.13		
			$I_{OH} = -5.2 \text{mA}$	6.0	5. 68			5.63		
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
			$I_{OL} = 20 \mu A$	4. 5			0.1		0.1	
VoL	Low-level output voltage	$V_{l} = V_{lH}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	v
			I _{OL} = 4.0mA	4.5			0.26		0.33	
			I _{OL} = 5. 2mA	6.0			0.26		0.33	
l _{iH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μΑ
1 _{IL}	Low-level input current	V ₁ = 0V		6.0			-0.1		-1.0	μA
loc	Quiescent supply current	VI = VCC, GND.	$I_0 = 0\mu A$	6.0			1.0		10.0	μА

HEX INVERTER

SWITCHING CHARACTERISTICS $(v_{cc} = 5v, \tau_a = 25^{\circ})$

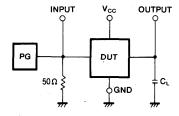
Cumbal	Parameter	Test conditions	Limits			Unit
Symbol	Parameter	Test conditions	Min	Тур	Max	OIII.
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time	C ₁ = 15pF (Note 3)			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = 15pr (Note 5)			17	ns
t _{PHL}	output propagation time		1		17	ns

SWITCHING CHARACTERISTICS ($v_{cc} = 2\sim6V$, $T_a = -40\sim+85$ °C)

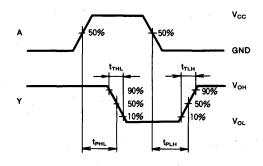
				Limits					
Symbol	Parameter	Test conditions			25℃		-40~	+85℃	Unit
		V _{cc} (v)		Min	Тур	Max	Min	Max	
			2.0			75		95	
tTLH	Low-level to high-level and	e e	4.5			15		19	ns
			6.0			13		16	
	high-level to low-level		2.0	,		75		95	
t _{THL}	output transition time	·	4.5			15		19	ns
		0 - 50-5 (N-4-3)	6.0			13		16	
		C _L = 50pF (Note 3)	2.0			86		108	
t _{PLH}	Low-level to high-level and		4.5		1	19		24	ns
	h		6.0			16		20	
	high-level to low-level		2.0			86		108	
t _{PHL}	output propagation time		4.5			19	,	24	ns
			6.0			16		20	
Cı	Input capacitance					10		10	рF
C _{PD}	Power dissipation capacitance (Note 2)				26				pF

Note 2 : CPD is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per inverter) The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$

Note 3: Test Circuit



- (1) The pulse generator (PG) has the following characteristics (10% \sim 90%): $t_r = 6ns$, $t_f = 6ns$ (2) The capacitance C_L includes stray wiring
- capacitance and the probe input capacitance.



MITSUBISHI HIGH SPEED CMOS

M74HCU04P/FP/DP

HEX UNBUFFERED INVERTER

DESCRIPTION

The M74HCU04 is a semiconductor integrated circuit consisting of six unbuffered inverters.

FEATURES

- High-speed: 7ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide supply voltage range: V_{CC}=2∼6V
- Wide operating temperature range: Ta=-40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

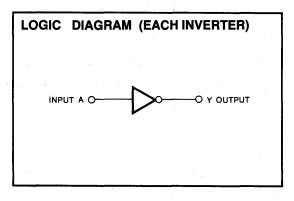
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HCU04 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS04.

Unbuffered outputs Y make this device suitable for linear circuit applications such as oscillators and amplifier circuits as well as logic system applications. However, consideration must be given in linear circuit applications dissipated power is much greater than of the 4000B series.

When input A is high, the output Y will become low, and when input A is low, the output Y will become high.

PIN CONFIGURATION (TOP VIEW) - A6 INPLIT OUTPUT Y6 INPUT INPUT OUTPUT Α5 10 Y5 OUTPUT INPUT OUTPUT Y3 INPUT GND OUTPUT 14P4 Outline 14P2N 14P2P



FUNCTION TABLE

Input	Output
Α	Y
L	н
Н	L

ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85$ °C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit		
Vcc	Supply voltage		-0.5~+7.0	V		
Vı	Input voltage		-0.5~V _{cc} +0.5	V		
Vo	Output voltage		-0.5~V _{cc} +0.5	٧		
		V ₁ < 0V	—20			
lık	Input protection diode current	$V_{i} > V_{CC}$	20	mA		
		V ₀ < 0V	20			
юк	Output parasitic diode current	Vo > Vcc	20	. mA		
lo	Output current per output pin		±25	mA		
loc	Supply/GND current	V _{CC} , GND	±50	mA		
Pd	Power dissipation	(Note 1)	500	mW		
Tstg	Storage temperature range		-65~+150	င		

Note 1 : M74HCU04FP, T $_a$ = $-40\sim+60^\circ$ C and T $_a$ = $60\sim85^\circ$ C are derated at -6mW/°C. M74HCU04DP, T $_a$ = $-40\sim+50^\circ$ C and T $_a$ = $50\sim85^\circ$ C are derated at -5mW/°C.



M74HCUO4P/FP/DP

HEX UNBUFFERED INVERTER

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85 \%)$

Symbol	Dorometer		Limits				
Symbol	Parameter	Min	Тур	Max	Unit		
V _{cc}	Supply voltage	2		6	٧		
V _i	Input voltage	0		Vcc	V		
V _o	Output voltage	0		Vcc	٧		
Topr	Operating temperature range	-40		+85	°C		
t _r , t _f	Input risetime, falltime	No limit			ns		

				Limits					
Symbol	Parameter	Test conditions	Test conditions		25°C			-40~+85℃	
			V _{cc} (V)	Min	Тур	Max	Min	Max	
		$V_0 = 0.2V, I_0 = 20\mu A$	2.0	1.7	-		1.7		
V_{1H}	High-level input voltage	$V_0 = 0.5V, I_0 = 20\mu A$	4.5	3.6			3.6		٧
		$V_0 = 0.5V, I_0 = 20\mu A$	6.0	4.8			4.8		
		$V_0 = V_{CC} - 0.2V$, $ I_0 = 20\mu A$	2.0			0.3		0.3	
VIL	Low-level input voltage	$V_0 = V_{CC} - 0.5V$, $ I_0 = 20\mu A$	4.5			0.8		0.8	V
		$V_0 = V_{CC} - 0.5V$, $ I_0 = 20\mu A$	6.0			1.1		1.1	
			2.0	1.8			1.8		
		$V_i = V_{iL}, i_{OH} = -20\mu A$	4.5	4.0			4.0	1.	
V _{OH}	High-level output voltage		6.0	5.5		1.	5.5		V
		$V_I = GND$, $I_{OH} = -4.0 mA$	4.5	3. 98			3.84		
		$V_1 = GND, I_{OH} = -5.2 mA$	6.0	5. 48			5. 34		
			2.0			0.2		0.2	
		$V_I = V_{IH}$, $I_{OL} = 20\mu A$	4.5			0.5		0.5	
VoL	Low-level output voltage		6.0			0.5		0.5	٧
		$V_I = V_{CC}, I_{OL} = 4.0 \text{mA}$	4.5			0.26		0.33	
		$V_I = V_{CC}, I_{OL} = 5.2 \text{mA}$	6.0			0.26		0.33	
I _{tH}	High-level input current	V₁ == 6V	6.0			0.1		1.0	μА
l _{IL} e	Low-level input current	V ₁ = 0V	6.0			-0.1		-1.0	μΑ
Icc	Quiescent supply current	$V_1 = V_{CC}$, GND, $I_0 = 0\mu A$	6.0			1.0		10.0	μА

SWITCHING' CHARACTERISTICS $(V_{cc} = 5V, T_a = 25\%)$

Combal	Parameter	Test conditions		Unit		
Symbol	Symbol	l est conditions	Min	Тур	Max	Unit
t _{TLH}	Low-level to high-level andhigh-level to low-level				10	ns
t _{THL}	output transition time	C ₁ = 15pF (Note 3)			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = 15pF (Note 5)			13	ns
t _{PHL}	output propagation time				13	ns

SWITCHING CHARACTERISTICS ($V_{cc} = 2\sim6V$, $T_a = -40\sim+85^{\circ}C$)

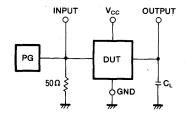
		Test conditions							
Symbol	Parameter			25℃			-40~+85℃		Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0			75		95	
t _{TLH}	Low-level to high-level and		4.5		1	15		19	ns
	high toward to have been	*	6.0			13		16	
-	high-level to low-level		2.0			75		95	
t _{THL}	t _{THL} output transition time	50.5(1) (3)	4.5			15		19	ns
			6.0			13	l	16	
		$C_L = 50 pF \text{ (Note 3)}$	2.0			82		103	
t _{PLH}	Low-level to high-level and		4.5			16		21	ns
	his touch to low touch		6.0		1	14		18	
	high-level to low-level		2.0			82		103	
t _{PHL}	output propagation time	·	4.5		ł	16		21	ns
			6.0			14	-	18	
Cı	Input capacitance					15		15	рF
CPD	Power dissipation capacitance (Note 2)				25				pF

Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per inverter)

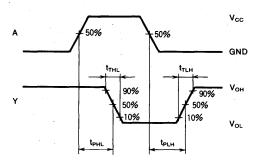
The power dissipated during operation under no-load conditions is calculated using the following formula:

P_D = C_{PD} · V_{CC}² · f₁+I_{CC} · V_{CC}

Note 3 : Test Circuit



- (1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns (2) The caracteristics (10% of the characteristics) (10% of the
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.





MITSUBISHI HIGH SPEED CMOS

M74HCT04P/FP/DP

HEX INVERTER WITH LSTTL-COMPATIBLE INPUTS

DESCRIPTION

The M74HCT04 is a semiconductor integrated circuit consisting of six inverters.

FEATURES

- TTL level input V_{IL}=0.8V, max V_{IH}=2.0V, min
- High-speed: 10ns typ. (C_L=15pF, Vcc=5V)
- Low power dissipation: 5µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- Capable of driving 10 74LSTTL loads
- Wide operating temperature range: T_a=-40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

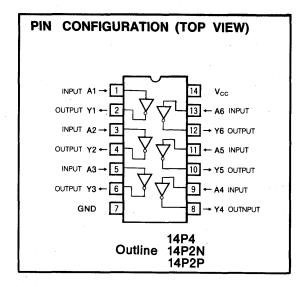
FUNCTIONAL DESCRIPTION

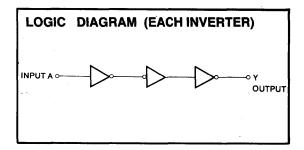
Use of silicon gate technology allows the M74HCT04 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS04.

As the inputs are TTL level, the device can be used as a level converter from LSTTL to high-speed CMOS. In that case, no pull-up resistors are required.

Buffered outputs Y improve input-to-output transfer characteristics and reduce to a minimum output impedance variations with respect to input voltage variations.

When input A is high, the output Y will become low, and when input A is low, the output Y will become high.





FUNCTION TABLE

Input	Output
A	Υ
L ·	Н
Н	L

ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85 ^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
V _I	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
	Input protection diode current	V ₁ < 0V	-20	
I _{IK}		V _i > V _{CC}	20	mA
		V ₀ < 0V	-20	
lok	Output parasitic diode current	Vo > Vcc	20	mA
lo	Output current per output pin		±25	mA
lcc	Supply/GND current	V _{CC} , GND	±50	.mA
Pd	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65 ~ +150	ဗ

Note 1 : M74HCT04FP, T $_a$ = $-40\sim+60^\circ$ C and T $_a$ = $60\sim85^\circ$ C are derated at -6mW/°C. M74HCT04DP, T $_a$ = $-40\sim+50^\circ$ C and T $_a$ = $50\sim85^\circ$ C are derated at -5mW/°C.

HEX INVERTER WITH LSTTL-COMPATIBLE INPUTS

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85 \degree C)$

Symbol	Parameter	İ	11-14		
	Parameter	Min	Тур	Max	Unit
Vcc	Supply voltage	4.5		5.5	V
Vı	Input voltage	. 0		Vcc	٧
V _o	Output voltage	0		Vcc	٧
Topr	Operating temperature range	—40		+85	Ç
t _r , t _f	Input risetime, falltime	0		500	ns

ELECTRICAL CHARACTERISTICS (V_{cc} = 5V±10%, unless otherwise noted)

	·					Limits			
Symbol	Parameter		Test conditions		25°C			+85℃	Unit
					Тур	Max	Min	Max	l
V _{IH}	High-level input voltage	$V_0 = 0.1V$ $ I_0 = 20\mu A$		2. 0			2.0		٧
VIL	Low-level input voltage	$V_0 = V_{CC} - 0.1V$ $ I_0 = 20\mu A$				0.8		0.8	٧
	V _{OH} High-level ouutput voltage		$I_{OH} = -20\mu A$	V _{cc} -0.1			V _{cc} -0.1		
VoH		$V_i = V_{iL}$	$I_{OH} = -4.0 \text{mA}, V_{CC} = 4.5 \text{V}$	4.18			4.13		V
	i		$I_{OH} = -4.8 \text{mA}, V_{CC} = 5.5 \text{V}$	5.18		1	5.13		
			$I_{OL} = 20\mu A$			0.1		0.1	
VoL	Low-level output voltage	$V_i = V_{iH}$	I _{OL} = 4.0mA, V _{CC} = 4.5V			0. 26		0.33	V
	·		$I_{OL} = 4.8 \text{mA}, \ V_{CC} = 5.5 \text{V}$			0. 26		0.33	ı
I _{IH}	High-level input current	$V_i = V_{CC}$				0.1		1.0	μA
I _{IL}	Low-level input current	V _i = GND				-0.1		-1.0	μΑ
loc	Quiescent supply current	$V_1 = V_{CC}$, GND, $I_0 = 0\mu A$				1.0		10.0	μA
Δlcc	Maximum quiescent supply current	V ₁ = 2.4V, 0.4	V (Note 2)			2.7		2.9	mA

Note 2: Only one input is set at this value and all other inputs are fixed at V_{CC} or GND.

SWITCHING CHARACTERISTICS ($V_{cc} = 5V$, $T_a = 25^{\circ}C$)

Symbol	Parameter	Test conditions		Unit		
Symbol		lest collutions	Min	Тур	Max] "" [
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time	C = 15-5 (Note 4)			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = 15pF (Note 4)			15	ns
t _{PHL}	output propagation time				. 15	ns

SWITCHING CHARACTERISTICS ($v_{cc} = 5v \pm 10\%$, $T_a = -40 \sim +85\%$)

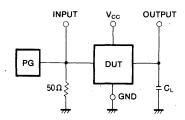
				Limits					
Symbol	Parameter	est conditions		25℃			-40~+85°C		
			Min	Тур	Max	Min	Max		
t _{TLH}	Low-level to high-level and				15		19	ns	
t _{THL}	high-level to low-level output transition time	C ₁ = 50pF (Note 4)			15		19	ns	
t _{PLH}	Low-level to high-level and	CL = 50pr (Note 4)			18		24	ns	
t _{PHL}	high-level to low-level output propagation time				18		24	ns ·	
Cı	Input capacitance				10		10	рF	
C _{PD}	Power dissipation capacitance (Note 3)							рF	

Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per inverter) The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$

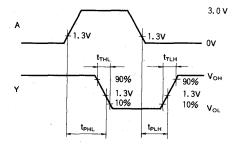


HEX INVERTER WITH LSTTL-COMPATIBLE INPUTS

Note 4: Test Circuit



- (1) The pulse generator (PG) has the following characteristics (10% \sim 90%): t_r = 6ns, t_f = 6ns (2) The capacitance C_L includes stray wiring
- capacitance and the probe input capacitance.



M74HC05P/FP/DP

HEX INVERTER WITH OPEN-DRAIN OUTPUTS

DESCRIPTION

The M74HC05 is a semiconductor integrated circuit consisting of six inverters with open-drain outputs.

FEATURES

- Open-drain outputs
- High-speed: 8ns typ. (C_LP=15pF, Vcc=5V)
- Low power dissipation: 5µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: Ta=-40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC05 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS05.

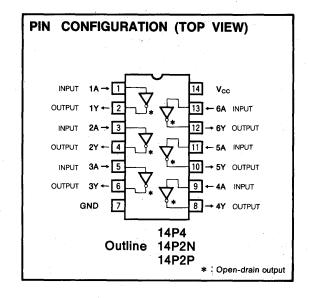
Open-drain outputs allow a versatile selection of high output impedances by connecting external load resistors.

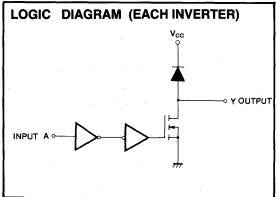
This enables "AND ties" which are not possible using normal gates. When input A is high, the output Y will become low, and when A is low, Y will become high.

Note that this IC differs from the 74LS05 and a voltage higher than Vcc can not be applied to the output.

FUNCTION TABLE

Input	Output
Α.	Y
L	Н
н	L .





HEX INVERTER WITH OPEN-DRAIN OUTPUTS

ABSOLUTE MAXIMUM RATINGS ($\tau_a = -40 \sim +85^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
		V ₁ < 0V	20	
lıк	Input protection diode current	V _I > V _{CC}	20	mA
•		V ₀ < 0V	-20	
lok	Output parasitic diode current	$V_0 > V_{CC}$	20	⊢ mA
lo	Output current per output pin		±25	mA
loc	Supply/GND current	V _{cc} , GND	±50	mA
Pd	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		-65~+150	င

Note 1 : M74HC05FP, $T_a=-40\sim+60^\circ\text{C}$ and $T_a=60\sim85^\circ\text{C}$ are derated at -6mW/°C. M74HC05DP, $T_a=-40\sim+50^\circ\text{C}$ and $T_a=50\sim85^\circ\text{C}$ are derated at -5mW/°C.

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85\%)$

Symbol	Parameter			11-:4			
Зупьог	га	Min	Тур	Max	Unit		
Vcc	Supply voltage	2		6	V		
Vı	Input voltage	0		V _{CC}	٧		
V _o	Output voltage	0		Vcc	V		
Topr	Operating temperature ra	inge	-40		+85	°C	
		$V_{CC} = 2.0V$. 0		1000		
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns	
	$V_{CC} = 6.0V$		0		400		

			Test conditions		Limits					
Symbol	Parameter	Test			25℃			−40 ~	+85°C	Unit
		V _{cc} (V)		Min	Тур	Max	Min	Max		
		V = 0.1V		2.0	1.5			1.5		
ViH	High-level input voltage	$V_0 = 0.1V$		4.5	3. 15			3. 15		V
		$ I_0 = 20\mu A$		6.0	4. 2			4.2		
		v – v 0 1		2.0			0.5		0.5	
V_{IL}	Low-level input voltage	$V_0 = V_{CC} - 0.1$	V	4.5		1	1.35		1.35	V
		$ I_0 = 20\mu A$		6.0			1.8		1.8	
	,		$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
			$I_{OL} = 20 \mu A$	4.5			0.1		0.1	
VoL	Low-level output voltage	$V_I = V_{IH}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
	la de la companya de la companya de la companya de la companya de la companya de la companya de la companya de		I _{OL} = 4.0mA	4.5			0. 26		0.33	
			$I_{OL} = 5.2 mA$	6.0	!		0. 26		0.33	
I _{IH}	High-level output current	V _I = 6V		6.0			0.1		1.0	μА
I _{IL}	Low-level input current	V _I == 0V		6.0			-0.1		-1.0	μА
		$V_i = V_{iL}, \ V_O =$	V _{CC}	6.0			0.5		5.0	
lo ,	Maximum output leakage current	$V_I = V_{IL}, \ V_O =$	$V_1 = V_{1L}, \ V_0 = GND \qquad \qquad 6.0$				-0.5		-5. 0	μА
lcc	Quiescent supply current	Vi = Vcc, GNE	$I_0 = 0 \mu A$	6.0			1.0		10.0	μА

HEX INVERTER WITH OPEN-DRAIN OUTPUTS

SWITCHING CHARACTERISTICS (V_{cc} = 5V, T_a = 25°C)

Symbol	Parameter	Test conditions	Visit	Limits			Unit
Symbol		rest conditions		Min	Тур	Max	Unit
t _{THL}	High-level to low-level output transition time	$R_{L} = 1k\Omega$ $C_{L} = 15pF \text{ (Note 3)}$				10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	$R_L = 1 k\Omega$, $C_L = 5 pF$ (Note 3)				20	ns
t _{PHL}	output propagation time	$R_L = 1k\Omega$, $C_L = 15pF$ (Note 3)				14	ns

SWITCHING CHARACTERISTICS ($V_{cc} = 2\sim 6V$, $T_a = -40\sim +85^{\circ}C$)

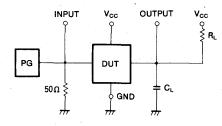
					Limits						
Symbol	Parameter	Test conditions V _{CC} (V)		. 25℃			-40~+85°C		Unit		
	. **			V _{cc} (V)	Min	Тур	Max	Min	Max		
	IN-E-IIA-III			2.0			75		95		
tTHL	High-level to low-level			4.5			15		19	ns	
	output transition time			6.0			13		16	ļ	
t _{PLH}				2.0			:115		145		
	Low-level to high-level and	$R_L = 1k\Omega$		4.5			23		29	ns	
		$C_L = 50 pF (Note 3)$		6.0		1 7	20		25	4, 44	
	high-level to low-level			2.0			85	4.0	105		
t _{PHL}	output propagation time			4.5		ļ	17		21	ns	
				6.0			14		18		
Ci	Input capacitance				· · · ·		10		10	pF	
Co	Output capacitance	A = GND					10		10	pF	
CPD	Power dissipation capacitance (Note 2)					8.				pF	

Note 2: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per gate)

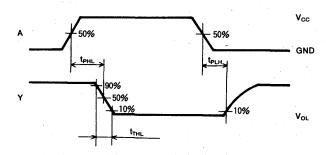
The power dissipated during operation under no-load conditions is calculated using the following formula:

P_D = C_{PD} · V_{CC}² · f₁+I_{CC} · V_{CC}

Note 3: Test Circuit



- (1) The pulse generator (PG) has the following characteristics (10% \sim 90%): $t_f = 6$ ns, $t_f = 6$ ns
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.



MITSUBISHI HIGH SPEED CMOS

M74HC08P/FP/DP

QUADRUPLE 2-INPUT POSITIVE AND GATE

DESCRIPTION

The M74HC08 is a semiconductor integrated circuit consisting of four 2-input positive-logic AND gates, usable as negative-logic OR gates.

FEATURES

- High-speed: 9.5ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

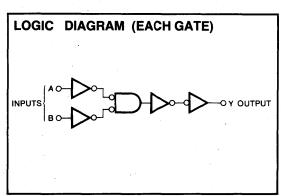
Use of silicon gate technology allows the M74HC08 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS08.

Buffered outputs Y improve input-to-output transfer characteristics and minimizes output impedance variations with respect to input voltage variations.

When both inputs A and B are high, the output Y will become high, and when at least one of the inputs is low, Y will become low.

FUNCTION TABLE

Inp	uts	Output		
Α	В	Y		
L	L	L		
Н	L	L		
L	Н	L		
Н	н н			



ABSOLUTE MAXIMUM RATINGS ($\tau_a = -40 \sim +85 \, ^{\circ} \text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage		-0.5~+7.0	٧
Vı	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
l _{ik}	In the second se	V ₁ < 0V	-20	
ΊK	Input protection diode current	$V_1 > V_{CC}$. 20	mA
	Output parasitic diode current	V ₀ < 0V	20	mA
ок	Output parastic diode current	Vo > Vcc	20	IIIA .
l _o	Output current per output pin		±25	mA
Icc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		-65~+150	°C

Note 1 : M74HC08FP, $T_a=-40\sim+60^\circ$ C and $T_a=60\sim85^\circ$ C are derated at -6mW/°C. M74HC08DP, $T_a=-40\sim+50^\circ$ C and $T_a=50\sim85^\circ$ C are derated at -5mW/°C.

QUADRUPLE 2-INPUT POSITIVE AND GATE

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85^{\circ}C)$

Symbol	Ba.	Parameter		Limits				
Зуппоог	rai	ameter	Min	Тур	Max	Unit		
V _{cc}	Supply voltage	Supply voltage			6	V		
V _I	Input voltage	. 0		Vcc	٧			
Vo	Output voltage	0		Vcc	V			
Topr	Operating temperature re	inge	-40		+85	°		
		$V_{CC} = 2.0V$	0		1000			
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns		
	$V_{CC} = 6.0V$		0		400			

					Limits					
Symbol	Parameter	Test	conditions		25℃			-40~+85℃		Unit
			V _{cc} (V)		Min	Тур	Max	Min	Max	
		V = 0.1V V	0.114	2.0	1.5			1.5		
V _{IH}	High-level input voltage	$V_0 = 0.1V, V_0$ $ I_0 = 20\mu A$	c—0.1 V	4.5	3.15			3.15		V
		$ 1_0 = 20\mu A$		6.0	4.2		1	4.2		ĺ
		$V_0 = 0.1V$	1	2.0			0.5		0.5	
VIL	Low-level input voltage	1 -		4.5			1.35		1.35	\ \ \
	, ,	$ 10 = 20\mu\text{A}$	$ I_{O} = 20\mu A$				1.8	i	1.8	İ
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
	· ·		$I_{OH} = -20\mu A$	4.5	4.4			4. 4		
V _{OH}	High-level output voltage $V_1 = V_{1H}$	$V_i = V_{iH}$	$I_{OH} = -20\mu A$	6.0	5.9	\		5.9		V
			$I_{OH} = -4.0 \text{mA}$	4.5	4. 18			4.13		
			$I_{OH} = -5.2 \text{mA}$	6.0	5.68			5.63		
	4		$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
			$I_{OL} = 20 \mu A$	4.5		ļ	0.1	ļ.	0.1	1
VoL	Low-level output voltage	$V_l = V_{lH}, V_{lL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
			I _{OL} = 4.0mA	4.5			0.26		0, 33	
			I _{OL} = 5. 2mA	6.0		}	0.26		0.33	
I _{IH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μА
f ₁ L	Low-level input current	V ₁ = 0V		6.0	~		-0.1		-1.0	μA
Icc	Quiescent supply current	VI = VCC, GNE	$0, \ I_0 = 0\mu A$	6.0			1.0		10.0	μΑ

QUADRUPLE 2-INPUT POSITIVE AND GATE

SWITCHING CHARACTERISTICS (Vcc = 5V, Ta = 25°C)

Symbol	Parameter	Test conditions		Unit		
Symbol		rest conditions	Min	Тур	Max	l Oline
t _{TLH}	Low-level to high-level and high-level to low-level	- C _L = 15pF (Note 3)			10	ns
t _{THL}	output transition time				10	ns
t _{PLH}	Low-level to high-level and high-level to low-level				15	ns
tent	output propagation time				20	ns ·

SWITCHING CHARACTERISTICS $(V_{CC} = 2\sim6V, T_{a} = -40\sim+85^{\circ}C)$

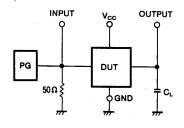
		-				Limits			
Symbol	Parameter	Test conditions			25℃		-40~+85°C		Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0			75		95	
t _{TLH}	Low-level to high-level and	· ·	4.5			15		19	ns
			6.0			13		16	
,	high-level to low-level		2.0			75		95	
t _{THL} output transition time	output transition time		4.5			15		19	ns
	·	50 5 (11 1 2)	6.0			13		16	
		C _L = 50pF (Note 3)	2.0			121		151	
t _{PLH}	Low-level to high-level and		4.5			24		30	ns
			6.0	-		20		25	
	high-level to low-level		2.0	********		121		151	
t _{PHL}	output propagation time		4.5			24		30	ns
			6.0			20		25	
Cı	Input capacitance				,	10		10	pF
CPD	Power dissipation capacitance (Note 2)				40				pF

Note 2: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per gate)

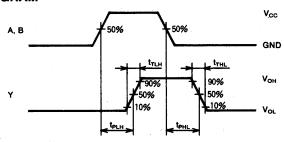
The power dissipation during operation under no-load conditions is calculated using the following formula:

P_D = C_{PD} · V_{CC}² · f₁+I_{CC} · V_{CC}

Note 3: Test Circuit



- (1) The pulse generator (PG) has the following characteristics (10%~90%): t_f = 6ns, t_f = 6ns
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.



M74HC09P/FP/DP

QUADRUPLE 2-INPUT POSITIVE AND GATE WITH OPEN-DRAIN OUTPUTS

DESCRIPTION

The M74HC09 is a semiconductor integrated circuit consisting of four 2-input positive-logic AND gates usable as negative-logic OR gates, with open-drain outputs.

FEATURES

- Open-drain outputs
- High-speed: 10ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5µW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2∼6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

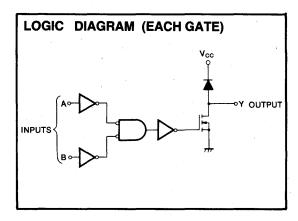
Use of silicon gate technology allows the M74HC09 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS09.

Open-drain outputs allow a versatile selection of high output impedances by connecting external load resistors. This enables "AND ties" which are not possible using normal gates.

When both inputs A and B are high, the output Y will become high, and when either A or B is low, Y will become low.

Note that this IC differs from 74LS09 and a voltage higher than Vcc can not be applied to the outputs.

PIN CONFIGURATION (TOP VIEW) INPUTS B1 + 2 OUTPUT Y1 + 3 A2 + 4 INPUTS B2 + 5 OUTPUT Y2 + 6 GND 7 WHEW) 14 OUTPUT 14 OUTPUT 14 OUTPUT 14 OUTPUT 14 OUTPUT 14 OUTPUT 14 OUTPUT 14 OUTPUT 14 OUTPUT 14 OUTPUT 14 OUTPUT 14 14 OUTPUT 15 OUTPUT 16 OUTPUT 16 OUTPUT 16 OUTPUT 17 OUTPUT 17 OUTPUT 18 O



FUNCTION TABLE

Inp	uts	Output	
Α	A B		
L	L .	L	
Н	L	L	
L	н	L	
Н	н	H	



QUADRUPLE 2-INPUT POSITIVE AND GATE WITH OPEN-DRAIN OUTPUTS

ABSOLUTE MAXIMUM RATINGS $(\tau_a = -40 \sim +85 \degree\text{C}, \text{ unless otherwise noted})$

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		−0.5~+7.0	٧
V _i	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
lik	Insula anatoration disease account	V ₁ < 0V	-20	
lik .	Input protection diode current	$V_{l} > V_{CC}$	20	mA
, , , , , , , , , , , , , , , , , , , ,	0.44	V _o < 0V	-20	
Ток	Output parasitic diode current	Vo > Vcc	20	mA
lo	Output current per output pin		±25	mA
Icc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		-65~+150	°C

Note 2 : M74HC09FP, $T_a=-40\sim+60^\circ\text{C}$ and $T_a=60\sim85^\circ\text{C}$ are derated at -6mW/°C. M74HC09DP, $T_a=-40\sim+50^\circ\text{C}$ and $T_a=50\sim85^\circ\text{C}$ are derated at -5mW/°C.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85 \degree C)$

				Limits					
Symbol	Pa	rameter	Min	Тур	Max	Unit			
V _{CC}	Supply voltage		2		6	V			
V _I	Input voltage		0		Vcc	٧			
Vo	Output voltage	Output voltage			Vcc	٧			
Topr	Operating temperature ra	ange	-40		+85	ိ			
		$V_{CC} = 2.0V$	0		1000				
t _r , t _f	t _r , t _f Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns			
	$V_{CC} = 6.0V$		0		400				

	-						Limits			
Symbol	Parameter	Test	conditions		25℃			-40~+85°C		Unit
		V _{CC} (V		V _{CC} (V)	Min	Тур	Max	Min.	Max	
		V 0.1V V	0.114	2.0	1.5			1.5		
VIH	High-level input voltage	$V_0 = 0.1V, V_{CI}$	C-0.1V	4.5	3.15			3.15		· v
		$ I_0 = 20\mu A$	= 20μA		4.2			4.2		
	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	V = 0.1V		2.0			0.5		0.5	
V_{IL}	Low-level input voltage	$V_0 = 0.1V$		4.5			1.35		1.35	. V
		$ I_0 = 20\mu A$		6.0			1.8		1.8	
			$I_{OL} = 20 \mu A$	2.0	-		0.1		0.1	
		-	$I_{OL} = 20 \mu A$	4.5			0.1		0.1	
VoL	Low-level output voltage	$V_{I} = V_{IH}, V_{IL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
			I _{OL} = 4.0mA	4.5			0.26		0.33	
			$I_{OL} = 5.2 \text{mA}$	6.0	-		0.26		0.33	
I _{IH}	High-level input current	V _I = 6V		6.0			0. 1		1.0	μA
I _{IL}	Low-level input current	$V_1 = 0V$		6.0			-0.1		-1.0	μÀ
	Maria	$V_i = V_{iH}, V_O =$	V _{CC}	6.0			0.5		5.0	^
lo	Maximum output leakage current	$V_I = V_{IH}, V_O =$	GND	6.0			-0.5		-5.0	μA
Icc	Quiescent supply current	VI = VCC, GNE	$I_0 = 0\mu A$	6.0			1.0		10.0	μΑ

QUADRUPLE 2-INPUT POSITIVE AND GATE WITH OPEN-DRAIN OUTPUTS

SWITCHING CHARACTERISTICS (V_{cc} = 5V, T_a = 25°C)

Γ	Symbol	Parameter	Test conditions		Unit		
1		Parameter	rest conditions	Min	Тур	Max	Jiii
	t _{THL}	High-level to low-level output transition time	$R_L = 1k\Omega$ $C_L = 15pF (Note 3)$			10	ns
ſ	t _{PLH}	Low-level to high-level and high-level to low-level	$R_L = 1k\Omega$, $C_L = 5pF$ (Note 3)			18	ns
I	t _{PHL}	output propagation time	$R_L = 1k\Omega$, $C_L = 15pF$ (Note 3)			18	ns

SWITCHING CHARACTERISTICS $(V_{cc} = 2 \sim 6V, T_a = -40 \sim +85 ^{\circ}C)$

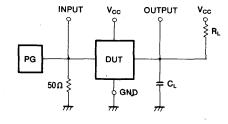
						Limits			
Symbol	Parameter	Test conditions		25℃			-40~+85℃		Unit
		·	V _{cc} (V)	Min	Тур	Max	Min	Max	
	Lifet total to love lovel		2.0			75		95	
t _{THL}	High-level to low-level	,	4.5			15		19	ns
	output transition time		6.0			13		16	
		1 - 110	2.0			105		131	
t _{PLH}	Low-level to high-level and	$R_{L} = 1 k \Omega$ $C_{I} = 50 pF (Note 3)$	4.5			25		31	ns
	Atab touchtain faunt	C _L = 50pF (Note 3)	6.0			23	ļ. ·	27	
	high-level to low-level		2.0			100		125	
t _{PHL}	output propagation time		4.5			20		25	ns
			6.0			17		21	
Cı	Input capacitance					10		10	pF
Со	Output capacitance	A, B = V _{CC}				10		10	pF
C _{PD}	Power dissipation capacitance (Note 2)				10				pF

Note 2: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per gate)

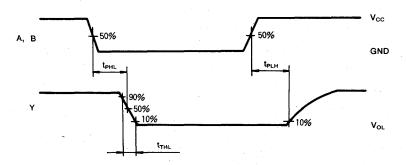
The power dissipated during operation under no-load conditions is calculated using the following formula:

P_D = C_{PD} · V_{CC}² · f₁+I_{CC} · V_{CC}

Note 3: Test Circuit



- (1) The pulse generator (PG) has the following characteristics (10%~90%): $t_{\rm f}=6{\rm ns},\,t_{\rm f}=6{\rm ns}$
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.





MITSUBISHI HIGH SPEED CMOS

M74HC10P/FP/DP

TRIPLE 3-INPUT POSITIVE NAND GATE

DESCRIPTION

The M74HC10 is a semiconductor integrated circuit consisting of three 3-input positive-logic NAND gates, usable as negative-logic NOR gates.

FEATURES

- High-speed: 10ns typ. (C₁=15pF, V_{CC}=5V)
- Low power dissipation: 5μW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: Ta=-40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC10 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS10.

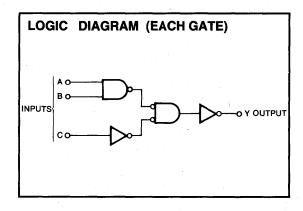
Buffered outputs Y improve input-to-output transfer characteristics and reduce to a minimium output impedance variations with respect to input voltage variations.

When all inputs A, B and C are high, the output Y will become low, and when at least one of the inputs is low, the output Y will become high.

FUNCTION TABLE

Inp	Inputs		
Α	N	Υ	
L	L	H	
Н	H L		
L	Н	Н	
H	Н	L_	

 $N = B \cdot C$



ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85$ °C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
V _i	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		$-0.5 \sim V_{cc} + 0.5$	V
,		V ₁ < 0V	-20	
f _{IK} ,	Input protection diode current	$V_{i} > V_{CC}$	20	mA
	Output paralitie diede euwent	V _o < 0V	-20	А
юк	Output parasitic diode current	V _o > V _{cc}	20	mA_
lo	Output current per output pin		±25	mA
lcc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		-65~+150	ဗ

Note 1 : M74HC10FP, $T_a=-40\sim+60^\circ\text{C}$ and $T_a=60\sim85^\circ\text{C}$ are derated at -6mW/C. M74HC10DP, $T_a=-40\sim+50^\circ\text{C}$ and $T_a=50\sim85^\circ\text{C}$ are derated at -5mW/C.



TRIPLE 3-INPUT POSITIVE NAND GATE

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85 ^{\circ}C)$

0		Parameter		Limits				
Symbol	Parameter		Min	Тур	Max	Unit		
V _{CC}	Supply voltage		2		6	V		
V _I	Input voltage		0		V _{CC}	V		
V _o	Output voltage		0		V _{cc}	V		
Topr	Operating temperature ra	ange	40		+85	∵ ℃		
		$V_{CC} = 2.0V$	0		1000			
r, tf	Input risetime, falltime	$\dot{V_{CC}} = 4.5V$	0		500	ns		
	V _{CC} = 6.0V		0		400]		

ELECTRICAL CHARACTERISTICS

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							Limits			
Symbol	Parameter	Test	Test conditions V _{cc} (V)		25℃			-40~+85℃		Unit
	1				Min	Тур	Max	Min	Max	
		$V_0 = 0.1V, V_{CC} = 0.1V$		2.0	1.5			1.5		
V_{IH}	High-level input voltage	$ 1_0 = 20\mu A$	C-0.14	4.5	3.15			3.15		V
		1101 - 20AA	$ = 20 \mu A$		4.2			4.2		
		$V_0 = V_{CC} - 0.1$		2.0			0.5		0.5	
VIL	Low-level input voltage	$ I_0 = 20\mu A$	•	4.5			1.35		1.35	V
		$ I_0 = 20\mu\text{A}$		6.0			1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
	High-level output voltage $V_{I} = V_{IH}, \ V_{I}$	$V_{I} = V_{IH}, V_{IL}$	$I_{OH} = -20 \mu A$	4.5	4.4			4.4		
VoH			$I_{OH} = -20\mu A$	6.0	5.9			5.9		v
			$I_{OH} = -4.0 \text{mA}$	4.5	4.18			4. 13		
			$I_{OH} = -5.2 \text{mA}$	6.0	5. 68			5. 63		
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
			$I_{OL} = 20 \mu A$	4.5		-	0.1		0.1	
VoL	Low-level output voltage	$V_i = V_{IH}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	v
			$I_{OL} = 4.0 \text{mA}$	4.5			0. 26		0.33	
			I _{OL} = 5. 2mA	6.0			0. 26		0.33	
I _{IH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μF
IIL	Low-level input current	V ₁ = 0V		6.0			-0.1		-1.0	μA
Icc	Quiescent pupply current	VI = VCC, GNE	$I_0 = 0\mu A$	6.0			1.0		10.0	μA

TRIPLE 3-INPUT POSITIVE NAND GATE

SWITCHING CHARACTERISTICS ($V_{cc} = 5V$, $T_a = 25^{\circ}C$)

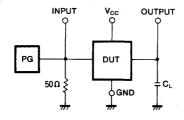
Or made at	Parameter	Total and distance		Limits				
Symbol		Test conditions	Min	Тур	Max	Unit		
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns		
t _{THL}	output transition time	0 - 15-5 (N-4-2)	-		10	ns		
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = 15pF (Note 3)			15	ns		
t _{PHL}	output propagation time				15	ns		

SWITCHING CHARACTERISTICS ($V_{cc} = 2\sim 6V$, $T_a = -40\sim +85^{\circ}C$)

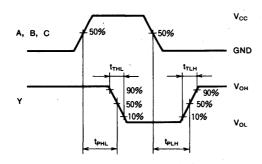
						Limits			
Symbol	Parameter	Test conditions		25℃			-40~+85℃		Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0			75		95	
t _{TLH}	Low-level to high-level and		4.5		İ	15		19	ns
	Bink towal to Java Lovel	'	6.0			13		16	
	high-level to low-level		2.0			75		95	
t _{THL}	output transition time		4.5		ļ	15		19	ns
		0 = 50.5 (No. 2)	6.0			13		16	
		C _L = 50pF (Note 3)	2.0			95		120	
t _{PLH}	Low-level to high-level and		4.5			19		24	ns
		•	6.0			16		20	
	high-level to low-level		2.0			95		120	
t _{PHL}	output propagation time		4.5			19		24	ns
			6.0			16		20	
C ₁	Input capacitance					10		10	pF
C _{PD}	Power dissipation capacitance (Note 2)				36				pF

Note 2 : CPD is the internal capacitance of the IC per gate calculated from operation supply current under no-load conditions. (per gate) The power dissipatiod during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$

Note 3: Test Circuit



- (1) The pulse generator (PG) has the following characteristics (10% \sim 90%): $t_r = 6ns$, $t_f = 6ns$ (2) The capacitance C_L includes stray wiring
- capacitance and the probe input capacitance.





M74HC11P/FP/DP

TRIPLE 3-INPUT POSITIVE AND GATE

DESCRIPTION

The M74HC11 is a semiconductor integrated circuit consisting of three 3-input positive-logic AND gates, usable as negative-logic OR gates.

FEATURES

- High-speed: 12ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5μW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC11 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS11.

Buffered outputs Y improve input-to-output transfer characteristics and minimizes output impedance variations with respect to input voltage variations.

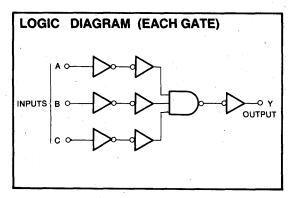
When all inputs A, B and C are high, the output Y will become high, and when at least one of the inputs is low, Y will become low.

FUNCTION TABLE

Inp	uts	Output
Α	N	Y
L	L	L
Н	L	L
L	Н	L
н	Н	Н

 $N = B \cdot C$

PIN CONFIGURATION (TOP VIEW) INPUTS $A1 \rightarrow 1 \qquad 14 \qquad V_{cc}$ $B1 \rightarrow 2 \qquad 13 \rightarrow C1 \quad \text{INPUT}$ $A2 \rightarrow 3 \qquad 12 \rightarrow Y1 \quad \text{OUTPUT}$ $B2 \rightarrow 4 \qquad 10 \rightarrow B3 \quad \text{INPUTS}$ $Y2 \leftarrow 6 \qquad 9 \rightarrow A3 \qquad \text{INPUTS}$ $Y2 \leftarrow 6 \qquad 9 \rightarrow A3 \qquad \text{OUTPUT}$ $Outline \qquad 14P4$ $Outline \qquad 14P2N$ 14P2P



ABSOLUTE MAXIMUM RATINGS $(T_a = -40 \sim +85\%$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
V _I	Input voltage	1.	-0.5~V _{cc} +0.5	V
V _o	Output voltage		-0.5~V _{cc} +0.5	V
	Input protection diode current	V ₁ < 0V	20	
lik	input protection alode current	$V_{i} > V_{CC}$	20	mA
	Outros appoints diada assess	V ₀ < 0V	-20	mA
ок	Output parasitic diode current	$V_0 > V_{CC}$	20] mA
lo	Output current per output pin		±25	mA
Icc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65~ +150	°C

Note 1 : M74HC11FP, $T_a=-40\sim+60^\circ$ C and $T_a=60\sim85^\circ$ C are derated at -6mW/°C. M74HC11DP, $T_a=-40\sim+50^\circ$ C and $T_a=50\sim85^\circ$ C are derated at -5mW/°C.



TRIPLE 3-INPUT POSITIVE AND GATE

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85^{\circ}C)$

0	n-	Parameter		Limits				
Symbol	Pai			Тур	Max	Unit		
V _{CC}	Supply voltage		2		6	٧		
Vı	Input voltage		0		V _{cc}	٧		
Vo	Output voltage		0		Vcc	٧		
Topr	Operating temperature ra	ange	40		+85	℃		
		$V_{CC} = 2.0V$	0		1000			
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns		
	,, 4	$V_{CC} = 6.0V$	0		400			

	-		,				Limits			
Symbol	Parameter	Test	conditions		25℃			-40~+85℃		Unit
			V _{cc} (V		Min	Тур	Max	Min	Max	1
		N - 0 111 11	0.114	2.0	1.5			1.5		
VIH	High-level input voltage	$V_0 = 0.1V, V_{CO}$	5—0.1 V	4.5	3.15			3.15		V
		$ 1_0 = 20\mu$ A	$ I_0 = 20\mu A$		4. 2		·	4.2		
		V -0 1V		2.0			0.5		0.5	
VIL	Low-level input voltage	$V_0 = 0.1V$		4.5			1.35		1.35	V
		$ I_{O} = 20\mu A$		6.0			1.8		1.8	İ
			$I_{OH} = -20 \mu A$	2.0	1.9			1.9		
	·		$I_{OH} = -20\mu A$	4.5	4.4			4. 4		
VoH	High-level output voltage	$V_i = V_{iH}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		V
			$I_{OH} = -4.0 \text{mA}$	4.5	4. 18			4.13		
			$I_{OH} = -5.2 \text{mA}$	6.0	5. 68			5.63		
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
			$I_{OL} = 20 \mu A$	4.5	ļ		0.1		0.1	
VoL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
			I _{OL} = 4.0mA	4.5			0.26		0.33	1
			$I_{OL} = 5.2 mA$	6.0			0.26		0.33	
I _{IH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μA
IIL	Low-level input current	V ₁ = 0V		6.0			-0.1		-1.0	μA
Icc	Quiescent supply current	VI = VCC, GND	$I_0 = 0\mu A$	6.0			1.0		10.0	μA

TRIPLE 3-INPUT POSITIVE AND GATE

SWITCHING CHARACTERISTICS ($v_{cc} = 5v$, $T_a = 25°C$)

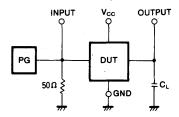
Symbol	Parameter	Test conditions		Unit		
- Cyllibol	i, di diffotol	rest conditions	Min	Тур	Max	Onn
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time	0 - 15-5 (11-1-2)			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = 15pF (Note 3)			20	ns
t _{PHL}	output propagation time				20	ns

SWITCHING CHARACTERISTICS ($v_{cc} = 2\sim 6v$, $T_a = -40\sim +85^{\circ}C$)

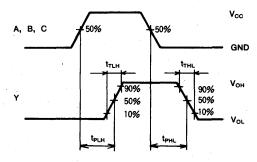
						Limits			
Symbol	Parameter	Test conditions		25℃			-40~+85℃		Unit .
			V _{cc} (V)	Min	Тур	Max	Min	Max	1.
			2.0			75		95	
t _{TLH}	Low-level to high-level and		4.5		Ì	15		19	ns
	1		6.0			13		16	
	high-level to low-level		2.0			75		95	
t _{THL} output transition time	output transition time		4.5			15		-19	ns
		50.5(44.50)	6.0		1	13		16	
		C _L = 50pF (Note 3)	2.0			125		156	
t _{PLH}	Low-level to high-level and		4.5		ĺ	25		31	ns
			6.0			21		27	
	high-level to low-level	1	2.0			125		156	
tent	output propagation time		4.5			25		31	ns
			6.0	1		21		27	
Cı	Input capacitance	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,		-		10		10	pF
C _{PD}	Power dissipation capacitance (Note 2)				34			1	pF

Note 2 : CPD is the internal capacitance of the IC calculated from operating supply current under no-load conditions. (per gate) The power dissipation during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$

Note 3: Test Circuit



- (1) The pulse generator (PG) has the following characteristics (10%∼90%): t_f = 6ns, t_f = 6ns (2) The capacitance C_L includes stray wiring
- capacitance and the probe input capacitance.



M74HC14P/FP/DP

HEX SCHMITT-TRIGGER INVERTER

DESCRIPTION

The M74HC14 is a semiconductor integrated circuit consisting of six Schmitt-trigger inverters.

FEATURES

- High-speed: 12ns typ. (C_L=15pF, Vcc=5V)
- Wide hysteresis voltage width: 0.8V (V_{CC}=5V, typ)
- Low power dissipation: 5µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

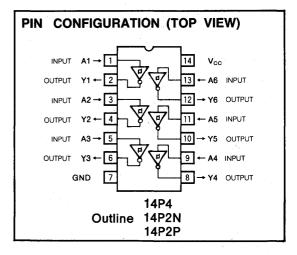
General purpose, for use in industrial and consumer digital equipment.

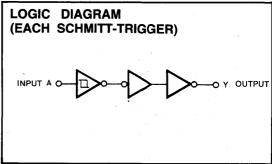
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC14 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS14.

Built-in Schmitt-trigger circuits prevent the occurrence of incorrect oscillations even when input signals having slow rise and fall times are applied. The Schmitt triggers ensure a signal of restored waveshape will appear at the output.

When input A is high, the output Y will become low, and when input A is low, the output Y will become high.





FUNCTION TABLE

Input	Output
Α	Y
L	н
Н	L

ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	V
V _o	Output voltage		-0.5~V _{cc} +0.5	V
	land and advantage	V ₁ < 0V	-20	4
lik .	Input protection diode current	$V_{I} > V_{CC}$	20	mA
	Out at a second and a second	V ₀ < 0V	-20	
Ток	Output parasitic diode current	Vo > Vcc	20	⊢ mA
lo	Output current per output pin		±25	mA
Icc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65~ + 150	°C

Note 1 : M74HC14FP, $T_a = -40 \sim +60^{\circ}\text{C}$ and $T_a = 60 \sim 85^{\circ}\text{C}$ are derated at -6mW/°C. M74HC14DP, $T_a = -40 \sim +50^{\circ}\text{C}$ and $T_a = 50 \sim 85^{\circ}\text{C}$ are derated at -5mW/°C.



HEX SCHMITT-TRIGGER INVERTER

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85 ^{\circ}C)$

Symbol	Parameter		Limits				
	Parameter	Min	Тур	Max	Unit		
Vcc	Supply voltage	2		6	٧		
V,	Input voltage	0		Vcc	٧		
Vo	Output voltage	0		Vcc	V		
Topr	Operating temperature range	-40		+85	c		
tr, tr	Input risetime, failtime	N	ns				

ELECTRICAL CHARACTERISTICS

2016年,因名图1gg 15 1**5 15** 1**5** 27 1

10.00mm (1.10mm) (1.10mm)

							Limits			
Symbol	Parameter	Test	conditions		25℃			−40 ~	Unit	
			V _{CC} (V)		Min	Тур	Max	Min	Max	·
		V = 0.1V		2.0	0. 7		1.5	0.7	1.5	
V_{T+}	Positive-going threshold voltage	$V_0 = 0.1V$ $ I_0 = 20\mu A$		4.5	1.55		3.15	1.55	3.15	V
		$ 10 = 20\mu\text{A}$		6.0	2.1		4. 2	2.1	4.2	
		V V 0 1	,	2.0	0.3		1.0	0.3	1.0	
V_{T-}	Negative-going threshold voltage		$V_0 = V_{CC} - 0.1V$	4.5	0.9		2.45	0.9	2. 45	V
		$ I_0 = 20\mu A$		6.0	1.2		3. 2	1.2	3.2	
	V ₀ = 0.1V V ₀		0.114	2.0	0.2	i i	1.2	0.2	1.2	
V _H	V _H Hysteresis voltage	$ V_0 = 0.1V, V_{CO} $ $ I_0 = 20\mu A$	$V_0 = 0.1V, V_{CC} - 0.1V$		0.4		2.1	0.4	2.1	V
		11 ₀ 1 = 20µA		6.0	0.5		2.5	0.5	2.5	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
			$I_{OH} = -20\mu A$	4.5	4.4			4.4		
VoH	High-level output voltage	$V_I = V_{T-}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		v
	La company of the com		$I_{OH} = -4.0 \text{mA}$	4.5	4.18			4.13		
		*	$I_{OH} = -5.2 \text{mA}$	6.0	5. 68			5. 63		
-			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
	1		$I_{OL} = 20 \mu A$	4.5			0.1	}	0.1	
VoL	Low-level output voltage	$V_1 = V_{T+}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
			I _{OL} = 4.0mA	4.5	,		0.26		0.33	
			I _{OL} = 5. 2mA	6.0			0.26	}	0.33	
I _{IH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μА
IIL	Low-level input current	V ₁ = 0V		6.0			-0.1		-1.0	μА
loc	Quiescent supply current	$V_{I} = V_{CC}$, GND	$I_0 = 0\mu A$	6.0			1.0		10.0	μA

HEX SCHMITT-TRIGGER INVERTER

SWITCHING CHARACTERISTICS ($v_{cc} = 5v$, $T_a = 25^{\circ}C$)

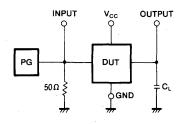
Cumbal	Parameter	Test conditions		Unit		
Symbol		l est conditions	Min	Тур	Max	l one
tTLH	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time	0 = 15-5 (N-4-2)			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = 15pF (Note 3)			- 22	ns
t _{PHL}	output propagation time				22	ns

SWITCHING CHARACTERISTICS $(v_{cc} = 2\sim6v, T_a = -40\sim+85^{\circ}C)$

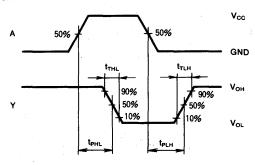
						Limits			
Symbol	Parameter	Test conditions		25℃			-40~+85℃		Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	1
	·		2.0			75		95	
t _{TLH}	Low-level to high-level and		4.5			15	ĺ	19	ns
	high level to tour		6.0			13		16	
	high-level to low-level		2.0			75		95	
t _{THL}	output transition time		4.5			15		19	ns
		0 = 50=5 (N=4= 3)	6.0			13	-	16	į l
		C _L = 50pF (Note 3)	2.0			125		156	
t _{PLH}	Low-level to high-level and		4.5			25		31	ns
			6.0			21		26	į l
	high-level to low-level		2.0			125		156	
t _{PHL}	output propagation time		4.5			25	1	31	ns
			6.0			21		26	
Cı	Input capacitance					10		10	pF
C _{PD}	Power dissipation capacitance (Note 2)				29				pF

Note 2: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per inverter) The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$

Note 3: Test Circuit



- (1) The pulse generator (PG) has the following characteristics (10%~90%): t_f = 6ns, t_f = 6ns
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.



MITSUBISHI HIGH SPEED CMOS

M74HC20P/FP/DP

DUAL 4-INPUT POSITIVE NAND GATE

DESCRIPTION

The M74HC20 is a semiconductor integrated circuit consisting of two 4-input positive-logic NAND gates, usable as negative-logic NOR gates.

FEATURES

- High-speed: 8ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5μW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=-40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC20 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS20.

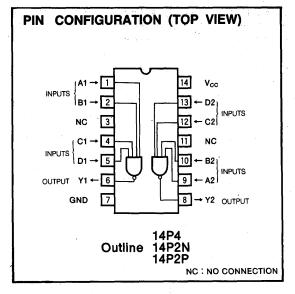
Buffered output Y improve input-to-output transfer characteristics and reduce to a minimium output impedance variations with respect to input voltage variations.

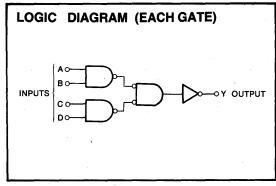
When all inputs A, B, C and D are high, the output Y will become low, and when at least one of the inputs is low, the output Y will become high.

FUNCTION TABLE

Inp	Inputs		
Α	N	Υ	
L	L	н	
н	L	Н	
L	Н	Н	
Н	Н	L	

 $N = B \cdot C \cdot D$





ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85$ °C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V _{cc}	Supply voltage		-0.5~+7.0	V
V _i	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{CC} +0.5	V
1	land A wash ables all ad a summer	V ₁ < 0V	—20	
lık	Input protection diode current	$V_{\rm I} > V_{\rm CC}$	20	mA
	Outside associate disease.	V _o < 0V	-20	
Гок	Output parasitic diode current	Vo > Vcc	20	mA
lo	Output current per output pin		±25	mA
Icc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65~ +150	°C

Note 1 : M74HC20FP, $T_a=-40\sim+60^\circ$ C and $T_a=60\sim85^\circ$ C are derated at $-6mW/^\circ$ C. M74HC20DP, $T_a=-40\sim+50^\circ$ C and $T_a=50\sim85^\circ$ C are derated at $-5mW/^\circ$ C.



M74HC20P/FP/DP

DUAL 4-INPUT POSITIVE NAND GATE

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85 \degree c)$

O b. ad	Parameter			Limits				
Symbol			Min	Тур	Max	Unit		
V _{CC}	Supply voltage		2		6	V		
Vı	Input voltage	0		V _{CC}	V			
Vo	Output voltage		0		Vcc	V		
Topr	Operating temperature ra	inge	40		+85	°C		
		V _{CC} = 2.0V	0		1000			
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns		
	$V_{CC} = 6.0V$		0		400			

						Limits				
Symbol	Parameter	Test	Test conditions $V_{CC}(V)$		25℃		•	-40~+85°C		Unit
					Min	Тур	Max	Min	Max	
	/	V = 0.1V V	$V_0 = 0.1V, V_{CC} = 0.1V$		1.5			1.5		
V _{IH}	High-level input voltage	1 -	c—0.1 V	4.5	3. 15			3.15		V
	$ I_0 = 20\mu A$		6.0	4.2			4.2			
		V - V -0 11	$V_0 = V_{CC} - 0.1V$				0.5		0.5	
VIL	Low-level input voltage	$ V_0 - V_{CC} - 0.1 $	•	4.5			1.35		1.35	V
	1101 -	1101 - 20µA		6.0			1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
			$I_{OH} = -20\mu A$	4.5	4.4			4.4		
VoH	High-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		V
			$I_{OH} = -4.0 \text{mA}$	4.5	4. 18			4.13		
			$I_{OH} = -5.2 \text{mA}$	6.0	5. 68			5. 63		
			$I_{OL} = 20 \mu A$	2.0			0. 1		0.1	
			$I_{OL} = 20 \mu A$	4.5			0. 1		0.1	
VoL	Low-level output voltage	$V_i = V_{iH}$	$I_{OL} = 20 \mu A$	6.0			0. 1		0.1	V
	'		I _{OL} = 4.0mA	4.5			0.26		0.33	
*			I _{OL} = 5. 2mA	6.0			0.26		0.33	
l _{IH} .	High-level input current	V ₁ = 6V		6.0			0. 1		1.0	μA
I _{IL}	Low-level input current	$V_i = 0V$		6.0			-0.1		-1.0	μA
lcc	Quiescent supply current	VI = VCC, GNE	$I_0 = 0\mu A$	6.0			1.0		10.0	μA

DUAL 4-INPUT POSITIVE NAND GATE

SWITCHING CHARACTERISTICS (V_{cc} = 5V, T_B = 25°C)

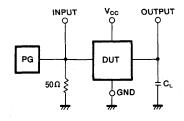
Symbol	Parameter	Test conditions		Unit		
Symbol		rest conditions	Min	Тур	Max	Uill
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time	C ₁ = 15pF (Note 3)			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = (Spr (Note 3)			15	ns
t _{PHL}	output propagation time				15	ns

SWITCHING CHARACTERISTICS ($v_{cc} = 2\sim6$ V, $T_a = -40\sim+85$ °C)

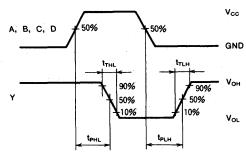
					Limits					
Symbol	Parameter	Test conditions		25℃			-40~+85℃		Unit	
			V _{cc} (V)	Min	Тур	Max	Min	Max]	
			2.0			75		95		
t _{TLH}	Low-level to high-level and	:	4.5			15		19	ns	
			6.0		İ	13		16		
	high-level to low-level		2.0			75		95		
t _{THL}	output transition time		4.5			15		19	ns	
			6.0			13		16		
		C _L = 50pF (Note 3)	2.0			90		113		
t _{PLH}	Low-level to high-level and		4.5			18	ì	23	ns	
	1		6.0			15		19		
	high-level to low-level		2.0	·		90		113	1	
t _{PHL}	output propagation time		4.5			18		23	ns	
			6.0			15		19		
Cı	Input capacitance					10		10	pF	
C _{PD}	Power dissipation capacitance (Note 2)	,			34	-	1	T	pF	

Note 2: C_{PD} is the internal capacitance of the IC per gate calculated from operation supply current under no-load conditions (per gate) The power dissipation during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$

Note 3: Test Circuit



- (1) The pulse generator (PG) has the following characteristics (10%~90%): t_f = 6ns, t_f = 6ns
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.





MITSUBISHI HIGH SPEED CMOS M74HC21P/FP/DP

DUAL 4-INPUT POSITIVE AND GATE

DESCRIPTION

The M74HC21 is a semiconductor integrated circuit consisting of two 4-input positive-logic AND gates, usable as negative-logic OR gates.

FEATURES

- High-speed: 12ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise marging: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2∼6V
- Wide operating temperature range: T_a=-40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC21 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS locig 4000B series while giving high-speed performance equivalent to the 74LS21.

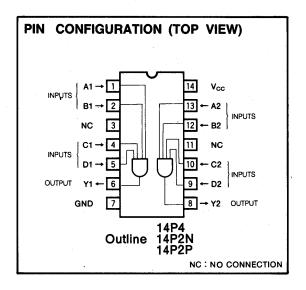
Buffered outputs improve input-to-output transfer characteristics and minimizes output impedance variations with respect to input voltage variations.

When all inputs A, B, C and D are high, the output Y will become high, and when at least one of the inputs is low, Y will become low.

FUNCTION TABLE

Inp	Inputs		
A N		Y	
L	L	L	
Н	H L		
L	н	L	
н	н	н	

 $N = B \cdot C \cdot D$



M74HC27P/FP/DP

TRIPLE 3-INPUT POSITIVE NOR GATE

DESCRIPTION

The M74HC27 is a semiconductor integrated circuit consisting of three 3-input positive-logic NOR gates, usable as negative-logic NAND gates.

FEATURES

- High-speed: 8ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2∼6V
- Wide operating temperature range: T_a=-40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC27 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS27.

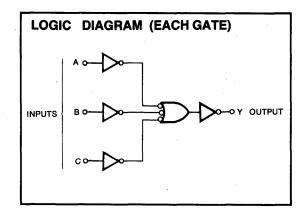
Buffered outputs Y improve input-to-output transfer characteristics and reduce to a minimum output impedance variations with respect to input voltage variations.

When all inputs A, B and C are low, the output Y will become high, and when at least one of the inputs is high, the output Y will become low.

FUNCTION TABLE

Inp	uts	Output
Α	N	·Y
L	L	Н
Н	L	L
L	H	L
Н	Н	L

N = B + C



ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85$ °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Ratings	Unit	
Vcc	Supply voltage		-0.5~+7.0	V	
V _I	Input voltage		-0.5~V _{cc} +0.5	V	
Vo	Output voltage		-0.5~V _{cc} +0.5	V	
		V ₁ < 0V	-20		
ıĸ	Input protection diode current	V _I > V _{CC}	20	mA.	
	Outside and the state of the st	V ₀ < 0V	20		
Іок	Output parasitic diode current	Vo > Vcc	20	mA	
lo	Output current per output pin		±25	mA	
lcc	Supply/GND current	V _{CC} , GND	±50	mA	
Pd	Power dissipation	(Note 1)	500	mW	
Tsta	Storage temperature range		-65~+150	င	

Note 1 : M74HC27FP, $T_a = -40 \sim +60 ^{\circ} C$ and $T_a = 60 \sim 85 ^{\circ} C$ are derated at $-6 mW/^{\circ} C$. M74HC27DP, $T_a = -40 \sim +50 ^{\circ} C$ and $T_a = 50 \sim 85 ^{\circ} C$ are derated at $-5 mW/^{\circ} C$.



TRIPLE 3-INPUT POSITIVE NOR GATE

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85\%)$

Symbol	Do	Parameter		Limits				
Symbol	Pa			Тур	Max	Unit		
Vcc	Supply voltage		2		6	. V		
V ₁	Input voltage		0		Vcc	٧		
Vo	Output voltage		0		Vcc	V		
Topr	Operating temperature ra	ange	-40		+85	ొ		
		$V_{CC} = 2.0V$	0		1000			
t _r , t _f Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns			
		$V_{CC} = 6.0V$	0		400			

ELECTRICAL CHARACTERISTICS

					Limits					Unit
Symbol	Parameter	Test	Test conditions V _{CC} (V)		25°C			-40~+85°C		
					Min	Тур	Max	Min	Max	
		$V_0 = 0.1V$		2.0	1.5			1.5		
ViH	High-level input voltage	$ V_0 - 0.1V $ $ I_0 = 20\mu A$		4.5	3.15			3.15		V
		1101 - 20AA		6.0	4.2		i '	4.2		
	-	V = 0.1V V	$V_{\rm O} = 0.1 V$, $V_{\rm CC} = 0.1 V$				0.5		0.5	-
VIL.	Low-level input voltage	$ I_{O} = 20\mu A$	5—0.1 V	4.5			1.35		1.35	V
		$ I_0 = 20\mu A$		6.0			1.8		1.8	
			$l_{OH} = -20\mu A$	2.0	1.9			1.9		
		$I_{OH} = -20\mu A$	4.5	4. 4			4.4			
VoH	High-level output voltage $V_i = V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		V	
			$l_{OH} = -4.0 \text{mA}$	4.5	4.18			4.13		
			$I_{OH} = -5.2 \text{mA}$	6.0	5.68			5.63		
			$I_{OL} = 20 \mu A$	2.0			0. 1		0.1	
			$I_{OL} = 20 \mu A$	4.5			0.1		0.1	
VoL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
			I _{OL} = 4.0mA	4.5			0.26		0.33	
			$I_{OL} = 5.2 mA$	6.0			0.26		0.33	
l _{ін}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μΑ
l _{i∟.}	Low-level input current	V ₁ = 0V		6.0			-0.1		-1.0	μA
Icc	Quiescent supply current	VI = VCC, GND	$I_0 = 0\mu A$	6.0			1.0		10.0	μA

TRIPLE 3-INPUT POSITIVE NOR GATE

SWITCHING CHARACTERISTICS (Voc = 5V, Ta = 25°C)

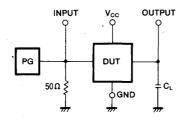
Symbol	Parameter	Test conditions		Limits		
Symbol	Farameter	l est conditions	Min	Тур	Max	Unit
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time	C = 15-5 (Note 2)			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = 15pF (Note 3)			15	ns
tehl	output propagation time				15	ns

SWITCHING CHARACTERISTICS ($v_{cc} = 2\sim6$ V, $T_a = -40\sim+85$ °C)

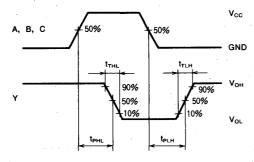
						Limits			
Symbol	Parameter	Test conditions	t conditions		25℃		-40~+85°C		Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0			75		95	
t _{TLH}	Low-level to high-level and		4.5			15		19	ns
	high touch to touch		6.0			13		16	
	high-level to low-level	•	2.0			75		95	
t _{THL}	output transition time		4.5		ļ	15	ļ	19	ns
	0 - 50-5 (N-4- 2)	6.0			13	1: .	16	1	
	CL	C _L = 50pF (Note 3)	2.0			90		113	
t _{PLH}	Low-level to high-level and		4.5			18		23	ns
	Nach January Lauri	*	6.0			15		19	
	high-level to low-level		2.0			90		. 113	
t _{PHL}	output propagation time		4.5	,		18	1	23	ns
			6.0			15		19	
Cı	Input capacitance		1			10		10	pF
C _{PD}	Power dissipation capacitance (Note 2)				34				pF

Note 2: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per gate)
The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$

Note 3 : Test Circuit



- (1) The pulse generator (PG) has the following characteristics (10% \sim 90%): t_f = 6ns, t_f = 6ns
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.



MITSUBISHI HIGH SPEED CMOS

M74HC30P/FP/DP

8-INPUT POSITIVE NAND GATE

DESCRIPTION

The M74HC30 is a semiconductor integrated circuit consisting of an 8-input positive-logic NAND gates, usable as negative-logic NOR gates.

FEATURES

- High-speed: 20ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=-40~+85℃

APPLICATION

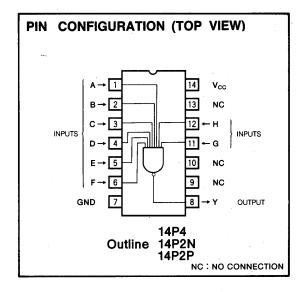
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC30 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS30.

Buffered Y outputs improve input-to-output propagation characteristics and reduce output impedance variations with respect to input voltage variations.

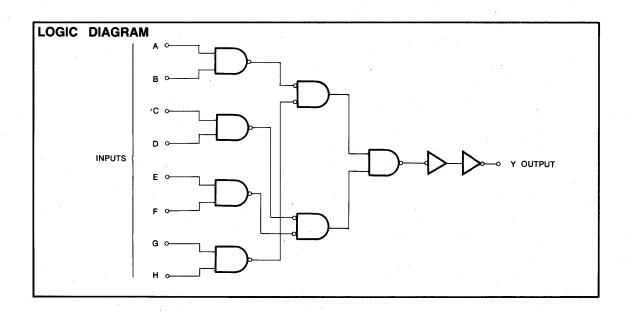
When all inputs A, B, C, D, E, F, G and H are high, the output Y will become low, and when at least one of the inputs is high, the output Y will become high.



FUNCTION TABLE

Input	ts	Output
Α	N	Y
L	L	Н
н	L	Н
L	н	Н
н	Н	L

 $N = B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H$





8-INPUT POSITIVE NAND GATE

ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85^{\circ}C$, unless otherwise noted)

\$ 60 mm - 30

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	٧ .
Vo	Output voltage		-0.5~V _{cc} +0.5	, V
1		V ₁ < 0V	-20	
1 _{IK}	Input protection diode current	V _I > V _{CC}	20	mA
	Output parasitic diode current	V ₀ < 0V	-20	· A
юк	Output parasitic diode current	v _o > v _{cc}	20	mA .
lo	Output current per output pin		±25	mA
Icc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65~+150	°C

Note 1 : M74HC30FP, $T_a=-40\sim+60^\circ\text{C}$ and $T_a=60-85^\circ\text{C}$ are derated at -6mW/C M74HC30DP, $T_a=-40\sim+50^\circ\text{C}$ and $T_a=50-85^\circ\text{C}$ are derated at -5mW/C.

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85 \degree C)$

Symbol	. no.	Parameter		Limits				
Symbol	Falanietei		Min	Тур	Max	Unit		
Vcc	Supply voltage	Supply voltage			6	. V		
Vı	Input voltage		. 0		Vcc	V		
Vo	Output voltage		0		Vcc	٧		
Topr	Operating temperature ra	ange	-40		+85	င		
		V _{CC} = 2.0V	. 0		1000			
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns		
		$V_{CC} = 6.0V$. 0		400			

ELECTRICAL CHARACTERISTICS

							Limits			
Symbol	Parameter Test condition			25℃			-40~+85°C		Unit	
			V _{CC} (V)		Min	Тур	Max	Min	Мах	
		V =0.1V V	0.11/	2.0	1.5	·		1.5		
V_{lH}	High-level input voltage	$V_0 = 0.1V, V_{CO}$	-0.1 v	4.5	3.15		-	3. 15		V
		$ I_0 = 20\mu A$		6.0	4.2	-		4.2		
		V - V 0 1		2.0		٠,	0.5	,	0.5	
V_{IL}	Low-level input voltage	$ V_0 = V_{CC} - 0.1V$ $ I_0 = 20\mu A$		4.5			1.35		1.35	V
				6.0			1.8		1.8	
			$I_{OH} = -20\mu A$. 2.0	1.9			1.9		
	•		$I_{OH} = -20\mu A$	4.5	4.4			4. 4		
V _{OH}	High-level output voltage	it voltage $V_{i} = V_{iH}, \ V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9		-	5.9		V
			$I_{OH} = -4.0 \text{mA}$	4.5	4. 18			4.13		
			$I_{OH} = -5.2 \text{mA}$	6.0	5.68			5. 63		
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
		* -	$I_{OL} = 20 \mu A$	4.5	· 1	1	0.1		0.1	
VoL	Low-level output voltage	$V_I = V_{IH}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
	•		I _{OL} = 4.0mA	4.5			0.26		0.33	-
			$I_{OL} = 5.2 \text{mA}$	6.0			0. 26		0.33	
I _{IH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μΑ
I _{IL}	Low-level input current	$V_1 = 0V$		6.0			-0.1		-1.0	μΑ
Icc	Quiescent supply current	VI = VCC, GND	$I_0 = 0\mu A$	6.0			1.0		10.0	μΑ

8-INPUT POSITIVE NAND GATE

SWITCHING CHARACTERISTICS (V_{cc} = 5V, T_a = 25°C)

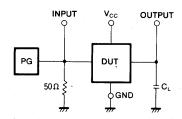
Symbol	Parameter	Test conditions		Unit		
Symbol		rest conditions	Min	Тур	Max	Unit
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time	0 = 15-5 (Non- 0)			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = 15pF (Note 3)			30	ns
t _{PHL}	output propagation time				30	ns

SWITCHING CHARACTERISTICS ($V_{cc} = 2\sim 6V$, $T_a = -40\sim +85°C$)

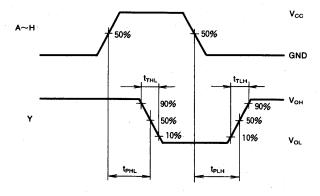
						Limits			ļ
Symbol	Parameter	Test conditions			25℃		-40~+85°C		Unit
		V _{cc} (V)		Min	Тур	Max	Min	Max] •
			2.0			75		95	
t _{TLH}	Low-level to high-level and		4.5			15		19	ns
	high level to take level		6.0	-	İ	13		16	
	high-level to low-level		2.0			75		95	
t _{THL}	output transition time		4.5			15		19	ns
		0 - 50-5 (N-4- 2)	6.0			13		16	
		$C_L = 50pF (Note 3)$	2.0			160		190	
t _{PLH}	Low-level to high-level and		4.5			35		42	ns
	high level to law level	,	6.0			30		36	
	high-level to low-level		2.0			160		190	
t _{PHL}	output propagation time		4.5			35		42	ns
			6.0			30		36	}
Cı	Input capacitance		-			10		10	pF
C _{PD}	Power dissipation capacitance (Note 2)	-			33				pF

Note 2: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per gate)
The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$

Note 3: Test Circuit



- (1) The pulse generator (PG) has the following characteristics (10% \sim 90%): $t_{\rm f} = 6$ ns, $t_{\rm f} = 6$ ns
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.



M74HC32P/FP/DP

QUADRUPLE 2-INPUT POSITIVE OR GATE

DESCRIPTION

The M74HC32 is a semiconductor integrated circuit consisting of four 2-input positive-logic OR gates, usable as negative-logic AND gates.

FEATURES

- High-speed: 10ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2∼6V
- Wide operating temperature range: T_a=-40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

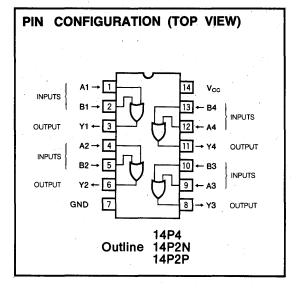
Use of silicon gate technology allows the M74HC32 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS32.

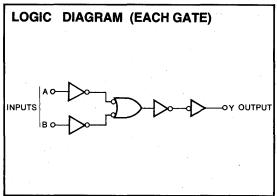
Buffered outputs Y improve input-to-output transfer characteristics and reduce to a minimum output impedance variations with respect to input voltage variations.

When both inputs A and B are low, output Y will become low, and when at least one of the inputs is high, the output Y will become high.

FUNCTION TABLE

Inpi	Inputs			
Α	В	Y		
L	L	L		
н	Ļ	н		
L	Н	н		
н	Н	Н		





ABSOLUTE MAXIMUM RATINGS $(\tau_a = -40 \sim +85^{\circ}C)$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
,	Input protection diode current	V ₁ < 0V	-20	
lik	Input protection diode current	V _I > V _{CC}	20	mA
-,	Output parasitic diode current	$V_0 < 0V$	-20	A
Ток	Output parasitic diode current	$V_0 > V_{CC}$	20	mA
lo	Output current per output pin		±25	mA
loc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65~+150	ကိ

Note 1 : M74HC32FP, $T_a=-40\sim+60^\circ\text{C}$ and $T_a=60\sim85^\circ\text{C}$ are derated at $-6\text{mW}/^\circ\text{C}$. M74HC32DP, $T_a=-40\sim+50^\circ\text{C}$ and $T_a=50\sim85^\circ\text{C}$ are derated at $-5\text{mW}/^\circ\text{C}$.



QUADRUPLE 2-INPUT POSITIVE OR GATE

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85^{\circ}C)$

Complete al	Parameter			Limits		Unit
Symbol	Pa	Min	Тур	Max	Unit	
Vcc	Supply voltage	ipply voltage			6	.V
Vı	Input voltage	nput voltage			Vcc	٧
Vo	Output voltage	Output voltage			Vcc	٧
Topr	Operating temperature ra	ange	-40		+85	ç
		$V_{CC} = 2.0V$. 0		1000	
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$. 0		500	ns
		$V_{CC} = 6.0V$			400	,

ELECTRICAL CHARACTERISTICS

							Limits			
Symbol	Parameter	Test	conditions	,	25℃			-40~+85°C		Unit
			V _{cc} (V)		Min	Тур	Max	Min	Max	
		V - V 0 1	,	2.0	1.5			1.5		
ViH	High-level input voltage		$V_0 = V_{CC} - 0.1V$ $ I_0 = 20\mu A$		3. 15		[.	3. 15		V
		1101 - 20µA			4.2			4.2		
		V = 0.1V V	-0.17	2.0			0.5		0.5	
VIL	Low-level input voltage		$V_0 = 0.1V, V_{CC} - 0.1V$ $ I_0 = 20\mu A$				1.35		1.35	V
	1101 =			6.0			1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
	High-level output voltage	$V_i = V_{iH}, \ V_{iL}$	$I_{OH} = -20\mu A$	4.5	4.4			4. 4		
V _{OH}			$I_{OH} = -20\mu A$	6.0	5.9			5. 9		v
			I _{OH} == -4.0mA	4.5	4. 18			4.13		
			$I_{OH} = -5.2 \text{mA}$	6.0	5. 68		1	5.63		
			$I_{OL} = 20 \mu A$	2.0			0.1	1	0.1	
		-	$I_{OL} = 20 \mu A$	4.5			0.1		0.1	
VoL	Low-level output voltage	$V_i = V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
			I _{OL} = 4.0mA	4.5			0. 26		0.33	
		$I_{OL} = 5.2 \text{mA}$	6.0	-		0. 26		0.33		
I _{IH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μA
I _I L	Low-level input current	V ₁ = 0V		6.0			-0.1		-1.0	μA
Icc	Quiescent supply current	VI = VCC, GND	$I_0 = 0\mu A$	6.0			1.0		10.0	μA

QUADRUPLE 2-INPUT POSITIVE OR GATE

SWITCHING CHARACTERISTICS (V_{cc} = 5V, T_a = 25°C)

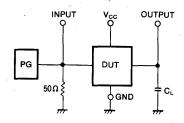
		T-4		Unit		
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time	$C_1 = 15pF $ (Note 3)		-	10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	$C_L = 15pF \text{ (Note 3)}$			18	ns
t _{PHL}	output propagation time				18	ns

SWITCHING CHARACTERISTICS ($V_{cc} = 2\sim 6V$, $T_a = -40\sim +85$ °C)

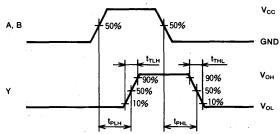
						Limits		,	
Symbol	Parameter	Test conditions		25℃			-40~+85℃		Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0			75		95	
t _{TLH}	Low-level to high-level and		4.5	1	1	15		19	ns
	high-level to low-level		6.0			13		16	
	nign-level to low-level		2.0			75		95	
t _{THL}	t _{THL} output transition time		4.5		1	15		19	ns
		0 50 5(11 1 0)	6.0			13		16	
		$C_L = 50 pF \text{ (Note 3)}$	2.0			100		125	
t _{PLH}	Low-level to high-level and		4.5			20		25	ns
			6.0			17	·	21	
	high-level to low-level		2.0			100		125	
t _{PHL}	output propagation time		4.5			20	1	25	ns
			6.0			17	1	21	Ì
C _I	Input capacitance					10	**	10	pF
C _{PD}	Power dissipation capacitance (Note 2)				30				рF

Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per gate)
The power dissipation during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$

Note 3: Test Circuit



- (1) The pulse generator (PG) has the following characteristics (10% \sim 90%): t_f = 6ns, t_f = 6ns
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.





M74HC42P/FP/DP

1-OF-10 DECODER

DESCRIPTION

The M74HC42 is a semiconductor integrated circuit consisting of a BCD to decimal decoder.

FEATURES

- Active-low output
- High-speed: 17ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85°C

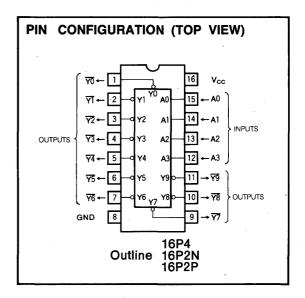
APPLICATION

General purpose, for use in industrial and consumer digital equipment.

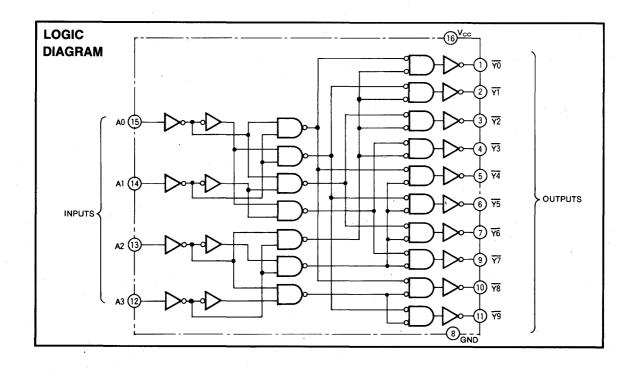
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC42 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS42.

When a BCD code is applied to inputs A0, A1, A2 and A3, one of outputs $\overline{Y0}$ through $\overline{Y9}$ corresponding to this value will become low and all others will become high. Use A0 for the least significant bit and A3 for the most significant bit. If



a value of ten or greater is applied to the inputs (A0 through A3), all outputs will become high.



1-OF-10 DECODER

FUNCTION TABLE

Decimal		Inp	uts						Out	puts				
number	А3	A2	A1	A0	<u>70</u>	Y1	Y2	<u>73</u>	¥4	₹5	<u>₹6</u>	¥7	Y8	₹9
0	L	L	- L	L	L	Н	н	. н	Н	Н	H	Н	Н	Н
1	L	L	L	Η	Н	L	н	Н	Н	Н	Н	н	Н	Н
2	L	L	Н	L	. н	Н	L	н	Н	н	H	Н	Н	Н
3	L	L	н	Н	Н	Н	Н	L	Н	н	н	н	Н	Н
4	L	Н	L	L.	Н	Н	Н	Н	L	Н	Н	Н	Н	Н
5	L	Н	L	Н	Н	Н	Н	Н	Н	L	н	Н	Н	Н
6	L	Н	Н	L	Н	Н	Н	Н	Н	Н	L	Н	н.	Н
7	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	н	L	н	н
8	Н	L	L	L	Н	н	Н	н	н	н	Н	Н	L	Н
9	Н	L	L	Н	Н	Н	Н	Н	Н	н	н	Н	Н.	L
10	Н	L	н	L	Н	Н	н	Н	н	Н	Н	Н	Н	Н
11	Н	L	Н	H	Н	Н	Н	Н	н	н	Н	Н	Н	н
12	Н	Н	L	L	Н	Н	Н	Н	Н	н	Н	Н	Н	Н
13	Н	н	L	Н	Н	Н	Н	Н	Н	н	Н	Н	Н	Н
14	H	Н	Н	L	Н	Н	н	н	н	H	Н	Н	Н	Н
15	Н	Н	Н	Н	Н	Н	Н	н	Н	Н	н	Н	н	H)

ABSOLUTE MAXIMUM RATINGS ($\tau_a = -40 \sim +85 ^{\circ} \text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage		−0.5∼+7.0	V
V _I	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
		V ₁ < 0V	-20	mA
liK.	Input protection diode current	$V_i > V_{CC}$	20	T MA
		V ₀ < 0V	-20	
Гок	Output parasitic diode current	Vo > Vcc	20	mA
lo	Output current per output pin		±25	mA
Icc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	. (Note 1)	500	mW
Tstg	Storage temperature range		-65~+150	င

Note 1 : M74HC42FP, $T_a=-40\sim+70^\circ\mathrm{C}$ and $T_a=70\sim85^\circ\mathrm{C}$ are derated at $-6\mathrm{mW/C}$. M74HC42DP, $T_a=-40\sim+50^\circ\mathrm{C}$ and $T_a=50\sim85^\circ\mathrm{C}$ are derated at $-5\mathrm{mW/C}$.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85\%)$

•	Parameter			Limits					
Symbol	Pai	rameter	Min	Тур	Max	Unit			
Vcc	Supply voltage		2		6	٧			
Vı	Input voltage	put voltage			Vcc	٧			
Vo	Output voltage	Output voltage			Vcc	٧			
Topr	Operating temperature ra	inge	-40		+85	°C			
		$V_{CC} = 2.0V$	0		1000				
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns-			
		$V_{CC} = 6.0V$			400				

M74HC42P/FP/DP

1-OF-10 DECODER

ELECTRICAL CHARACTERISTICS

	į.						Limits			
Symbol	Parameter	Test	conditions		25°C			-40~+85℃		Unit
_			V _{cc} (V)		Min	Тур	Max	Min	Max	Ī
		V = 0 1V V	$V_0 = 0.1V, V_{CC} = 0.1V$ $ I_0 = 20\mu A$		1.5			1.5		
VIH	High-level input voltage				3. 15		ĺ	3. 15		\ \ \
		- 101 - 20μΑ			4.2			4.2		
		V = 0 1V V	-0.1V	2.0			0.5		0.5	
VIL	Low-level input voltage		$V_0 = 0.1V, V_{CC} - 0.1V$ $ I_0 = 20\mu A$				1. 35	ĺ	1.35	V
_		1101 - 20μΑ					1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
	•		$I_{OH} = -20\mu A$	4.5	4.4			4.4		1
VoH	High-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		v
			$I_{OH} = -4.0 \text{mA}$	4.5	4. 18			4. 13		1
			$I_{OH} = -5.2 \text{mA}$	6.0	5. 68			5. 63	1	i
			$I_{OL} = 20\mu A$	2.0			0.1		0.1	
			$I_{OL} = 20 \mu A$	4.5			0.1		0.1	
VoL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
			I _{OL} = 4.0mA	4. 5			0. 26		0.33	
			I _{OL} = 5. 2mA	6.0			0. 26		0.33	
I _{IH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μА
1 _{IL}	Low-level input current	V ₁ = 0V		6.0			-0.1		-1.0	μА
Icc	Quiescent supply current	VI = VCC, GND	$I_0 = 0\mu A$	6.0			4.0		40.0	μА

SWITCHING CHARACTERISTICS ($v_{cc} = 5v$, $T_a = 25^{\circ}C$)

Sumbal	Parameter	Test conditions			Unit	
Symbol		l'est conditions	Min	Тур	Max	Unit
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time	C ₁ = 15pF (Note 3)			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = 15pr (Note 3)			25	ns
t _{PHL}	output propagation time				25	ns

SWITCHING CHARACTERISTICS $(v_{cc} = 2\sim 6V, T_a = -40\sim +85^{\circ}C)$

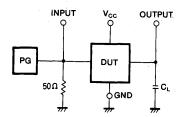
			-			Limits			
Symbol	Parameter	Test conditions	-	25℃			-40~+85°C		Unit
			V _{cc} (V)	Min-	Тур	Max	Min	Max	
			2.0			75		95	
t _{TLH}	Low-level to high-level and		4.5		}	15		19	ns
	high-level to low-level		6.0			13		16	ļ
nign-level to low-level		2.0			75		95		
t _{THL}	output transition time		4.5		1	15		19	ns
		50 5 (00 00)	6.0			13		16	
		$C_L = 50 pF (Note 3)$	2.0			150		189	
t _{PLH}	Low-level to high-level and		4.5			30		38	ns
			6.0		-	26		32	
	high-level to low-level		2.0			150		189	
t _{PHL}	output propagation time		4.5			30		38	ns
	· ·		6.0			26		32	
Cı	Input capacitance					10		10	pF
C _{PD}	Power dissipation capacitance (Note 2)				86		****		pF

Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$



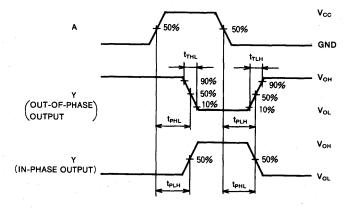
1-OF-10 DECODER

Note 3: Test Circuit



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- (1) The pulse generator (PG) has the following characteristics (10%∼90%): t_r = 6ns, t_r = 6ns (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.



M74HC51P/FP/DP

2-WIDE, 2-INPUT/2-WIDE, 3-INPUT AND-OR-INVERT GATES

DESCRIPTION

The M74HC51 is a semiconductor integrated circuit consisting of a 2-wide, 2-input/2-wide, 3-input AND-OR-INVERT gate.

FEATURES

- High speed: 9ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5μW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2∼6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

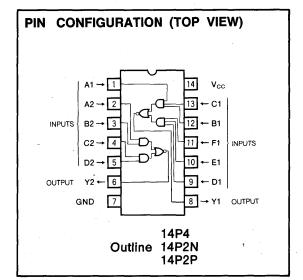
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC51 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS51.

The M74HC51 consists of two NOR gate, one using two 2-inputs AND gates for the input and the other using two 3-input AND gates for the input. The characteristics are described by the following logical equations.

$$Y1 = A1 \cdot B1 \cdot C1 \cdot D1 \cdot E1 \cdot F1$$

$$Y2 = \overline{A2 \cdot B2 + C2 \cdot D2}$$



FUNCTION TABLE (Note 1)

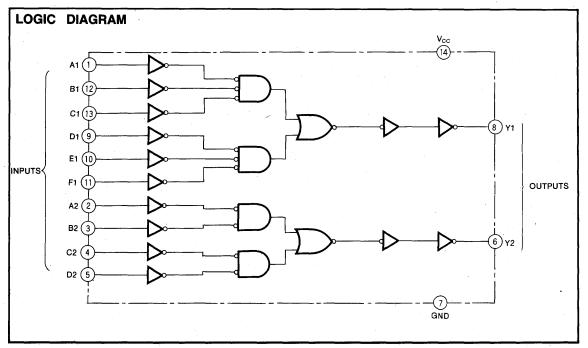
Inp	uts	Output
М	N	Y
L	L	Н
Н	L	L
L.	н	L
Н	Н	L

Note 1: $M=A1 \cdot B1 \cdot C1$ $N=D1 \cdot E1 \cdot F1$

N ≈DI • EI • F

M=A2 · B2

 $N = C2 \cdot D2$



2-WIDE,2-INPUT/2-WIDE,3-INPUT AND-OR-INVERT GATES

ABSOLUTE MAXIMUM RATINGS $(T_a = -40 \sim +85^{\circ}C, \text{ unless otherwise noted})$

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
	India and add and and	V ₁ < 0V	-20	
lıĸ	Input protection diode current	V _I > V _{CC}	20	mA
1.	0. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1.	V ₀ < 0V	-20	
lok	Output parasitic diode current	Vo > Vcc	20	mA
lo	Output current, per output pin		±25	mA
lcc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼ +150	ာ

Note 2. M74HC51FP, T $_{\rm a}=-40\sim+60^{\circ}$ C and T $_{\rm a}=60\sim85^{\circ}$ C are derated at -6mW/°C. M74HC51DP, T $_{\rm a}=-40\sim+50^{\circ}$ C and T $_{\rm a}=50\sim85^{\circ}$ C are derated at -5mW/°C.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85 °C)$

Comple ed	Parameter			Unit		
Symbol	Pa.	rameter	Min	Тур	Max	Unit
Vcc	Supply voltage		2		6	V
Vi	Input voltage		. 0		Vcc	٧
Vo	Output voltage		0		Vcc	V
Topr	Operating temperature ra	ange	-40		+85	င
		V _{CC} = 2.0V	0		1000	
t _r , t _f	Input risetime, falltime	V _{CC} = 4.5V	0		500	ns
		$V_{CC} = 6.0V$	0		400	

ELECTRICAL CHARACTERISTICS

							Limits			
Symbol	Parameter	Test	conditions		25℃			-40~	+85℃	Unit
			V _{CC} (V)		Min	Тур	Max	Min	Max	
		V -0 1V V	0.114	2.0	1.5			1.5	,	
V _{IH}	High-level input voltage	' ' '	$V_0 = 0.1V, V_{CC} - 0.1V$ $ I_0 = 20\mu A$		3.15	Ì		3.15		V
ı		$ 1_0 = 20\mu A$			4.2			4.2		
		V = 0.1V V	$V_0 = 0.1V, V_{CC} - 0.1V$				0.5		0.5	
VIL	Low-level input voltage	$ I_0 = 20\mu A$	5—0.1 V	4.5			1.35		1.35	V
		1101 - 20µA		6.0			1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
		'	$I_{OH} = -20\mu A$	4.5	4.4			4.4		
VoH	High-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9		<u> </u>	5.9		V
			$I_{OH} = -4.0 \text{mA}$	4.5	4. 18			4.13		
			$I_{OH} = -5.2 \text{mA}$	6.0	5. 68			5. 63		
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
	4		$I_{OL} = 20 \mu A$	4.5			0.1	Ì	0.1	
VoL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
		1	I _{OL} = 4.0mA	4.5			0.26	1	0.33	
			I _{OL} = 5. 2mA	6.0			0. 26		0.33	
I _{IH} \	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μA
l _{IL}	Low-level input current	V ₁ = 0V		6.0			-0.1		-1.0	μA
loc	Quiescent supply current	VI = VCC, GND	$I_0 = 0\mu A$	6.0			1.0		10.0	μA

2-WIDE.2-INPUT/2-WIDE,3-INPUT AND-OR-INVERT GATES

SWITCHING CHARACTERISTICS ($v_{cc} = 5v$, $\tau_a = 25^{\circ}$)

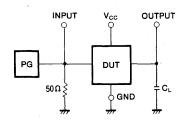
O	2	T dial		Unit		
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
tTLH	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time	C = 15 = 5 (Nicho 4)			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = 15pF (Note 4)			20	ns
t _{PHL}	output propagation time				20	ns

SWITCHING CHARACTERISTICS $(V_{CC} = 2\sim6V, T_a = -40\sim+85^{\circ}C)$

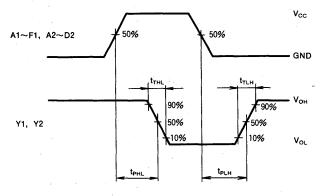
						Limits			
Symbol	Parameter	Test conditions		25℃			-40~+85℃		Unit
	·		V _{cc} (V)	Min	Тур	Max	Min	Max	1
			2.0			75		95	
t _{TLH}	Low-level to high-level and		4.5		[15		19	ns
	high-level to low-level		6.0			13		16	
	1		2.0			75		95	
t _{THL}	output transition time		4.5			15		19	ns
		0 50.7(1)	6.0			13		16	
		$C_L = 50 pF (Note 4)$	2.0			125		158	
t _{PLH}	Low-level to high-level and		4.5		Ì	25		32	ns
			6.0			21		27	
	high-level to low-level		2.0			125		158	
t _{PHL}	output propagation time		4.5			25		32	ns
			6.0			21		27	
C _i	Input capacitance					10		10	pF
C _{PD}	Power dissipation capacitance (Note 3)				35				pF

Note 3: CPD is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per gate) The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$

Note 4: Test Circuit



- (1) The pulse generator (PG) has the following
- characteristics (10% \sim 90%): $t_r = 6$ ns, $t_f = 6$ ns (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.



M74HC73P/FP/DP

DUAL J-K FLIP-FLOP WITH RESET

DESCRIPTION

The M74HC73 is a semiconductor integrated circuit consisting of two negative-edge triggered J-K flip flops with independent control inputs.

FEATURES

- High-speed: 50MHz clock frequency typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 10μW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

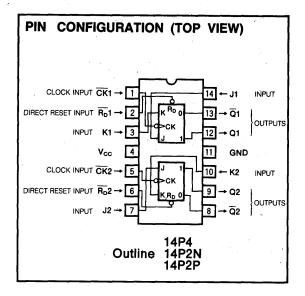
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC73 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS73.

The M74HC73 contains two edge-triggered J-K flip flops, each circuit with independent clock input \overline{CK} , direct reset input $\overline{R_D}$, and both inputs J and K.

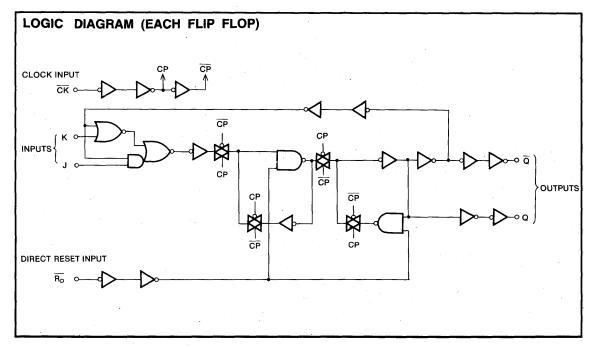
When \overline{CK} is high, the J and K signals can be read. When \overline{CK} changes from high-level to low-level, the signals just



previousy input at J and K appear at outputs Q and \overline{Q} in accordance with the function table given. When $\overline{R_D}$ is low, Q and \overline{Q} will become low and high respectively, irrespective of other inputs. When used as a J-K flip flop, $\overline{R_D}$ should be maintained at high-level.

A unit, the M74HC107, having the same functions and electrical characteristics as the M74HC73 is also available.

This offers easy mounting with pins 7 and 14 being GND and V_{CC} respectively.





M74HC73P/FP/DP

DUAL J-K FLIP-FLOP WITH RESET

FUNCTION TABLE (Note 1)

	Inp	uts		Out	puts
R _D	CK	J	K	Q	Q
L	х	×	X	L	Н
Н	Į.	L	L	Q°	Q٥
Н	1	L	н	L	н
Н	1	Н	L	н	L
н	1	Н	н	Tog	ggle
Н	L	х	×	Qº	Q°
Н	Н	x ′	×	Q٥	Q°
н	Ť	X	х	Q°	Q°

Note 1: † : Change from low to high

Change from high to low

X : Irrelevant

 $\begin{array}{ll} \underline{Q}^0 & \text{: Output state } \underline{Q} \text{ before clock input changed} \\ \overline{Q}^0 & \text{: Output state } \overline{Q} \text{ before clock input changed} \\ \text{Toggle: Inversion state before clock input changed} \end{array}$

ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85 \degree$ C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit			
V _{CC}	Supply voltage		-0.5~+7.0	V			
V _I	Input voltage		-0.5~V _{cc} +0.5	V			
Vo	Output voltage		-0.5~V _{cc} +0.5	· V			
	Input protection diode current	V ₁ < 0V		-20			
l _{IK}	input protection diode current	put protection diode current $V_{\rm l} > V_{\rm CC}$		mA			
		V ₀ < 0V	-20				
Іок	Output parasitic diode current	Vo > Vcc	20	mA			
lo	Output current per output pin		±25	mA			
loc	Supply/GND current	V _{CC} , GND	±50	mA			
Pd	Power dissipation	(Note 2)	500	mW			
Tstg	Storage temperature range		−65~+150	°C			

Note 2 : M74HC73FP, $T_a=-40\sim+60^\circ\text{C}$ and $T_a=60\sim85^\circ\text{C}$ are derated at -6mW/°C. M74HC73DP, $T_a=-40\sim+50^\circ\text{C}$ and $T_a=50\sim85^\circ\text{C}$ are derated at -5mW/°C.

DUAL J-K FLIP-FLOP WITH RESET

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85\%)$

Ob. ad	Parameter			Limits				
Symbol	Pa	Falanielei			Max	Unit,		
Vcc	Supply voltage		.2		6	٧٠		
V _i	Input voltage		0		Vcc	٧		
V _o	Output voltage	0		Vcc	V			
Topr	Operating temperature ra	inge	-40		+85	ဗ		
		$V_{CC} = 2.0V$	0		1000			
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns		
	$V_{CC} = 6.0V$		0		400			

ELECTRICAL CHARACTERISTICS

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· 约4. 网络马克拉斯马德斯斯特

							Limits		` .	
Symbol	Parameter	Test	Test conditions V _{CC} (V)		25°C			-40~+85℃		Unit
					Min	Тур	Max	Min	Max	
		V -0.1V V	0.11/	2.0	1.5			1.5		
VIH	High-level input voltage	$ V_0 = 0.1V, V_{CI}$	$V_0 = 0.1V, V_{CC} = 0.1V$		3.15		1	3.15		V
		$ 1_0 = 20\mu A$	1161 — 20µA		4.2			4.2		
	,	V =0.1V V	V ₂ = 0.1V, V ₂ = 0.1V				0.5		0.5	
V_{IL}	Low-level input voltage	1 -	V ₀ = 0.1V, V _{CC} -0.1V]		1.35		1.35	V .
	I _O = 20µA	•	6.0			1.8		1.8		
			$I_{OH} = -20\mu A$	2.0	1.9		,	1.9		
	-		$I_{OH} = -20 \mu A$	4.5	4.4			4.4		
V_{OH}	High-level output voltage	$V_{I} = V_{IH}, V_{IL}$	$I_{OH} = -20\mu A$	6.0	5.9			5. 9		V
			$I_{OH} = -4.0 \text{mA}$	4.5	4. 18			4.13		
			$I_{OH} = -5.2 \text{mA}$	6.0	5.68			5.63		
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
			$I_{OL} = 20 \mu A$	4.5]		0.1		0.1	
Vol	Low-level output voltage	$V_{l} = V_{lH}, V_{lL}$	$I_{OL} = 20 \mu A$	6.0	٠.		0.1		0.1	V
	• .		I _{OL} = 4.0mA	4.5			0.26		0.33	
	. '		I _{OL} = 5. 2mA	6.0			0.26		0, 33	:
l _{iH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μА
-I _{IL}	Low-level input current	$V_1 = 0V$		6.0			-0.1		-1.0	μA
Icc	Quiescent supply current	VI = VCC, GNE	$I_{O} = 0\mu A$	6.0			2.0		20.0	μΑ

M74HC73P/FP/DP

DUAL J-K FLIP-FLOP WITH RESET

SWITCHING CHARACTERISTICS $(v_{cc} = 5v, T_a = 25^{\circ}C)$

Symbol	Parameter	Test conditions		Unit		
Symbol	Parameter	rest conditions	Min	Тур	Max	Unit
fmax	Maximum clock frequency		30			MHz
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time				10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = 15pF (Note 4)			28	ns
t _{PHL}	output propagation time $(\overline{CK} - Q, \overline{Q})$				28	ns
t _{PLH}	Low-level to high-level and high-level to low-level				34	ns
t _{PHL}	output propagation time $(\overline{R_D} - Q, \overline{Q})$				34	ns

SWITCHING CHARACTERISTICS $(V_{cc} = 2\sim6V, T_a = -40\sim+85^{\circ}C)$

						Limits			
Symbol	Parameter	Test conditions	_		25℃		-40~	+85℃	Unit
	<u> </u>	V _{cc} (V)		Min	Тур	Max	Min	Max	1
			2.0	5			4		
fmax	Maximum clock frequency		4.5	27			21		MHz
			6.0	31		1	24		
			2.0			75		95	
t _{TLH}	Low-level to high-level and		4.5			15		19	ns
			6.0		l	13		16	
	high-level to low-level		2.0			75		95	
t _{THL}	output transition time		4.5			15		19	ns
			6.0			13		16	
			2.0			160		195	
t _{PLH}	Low-level to high-level and	C _L = 50pF (Note 4)	4.5			32		39	ns
	high-level to low-level	• •	6.0		1	28		34	1.
	output propagation time		2.0			160		195	
t _{PHL}	(CK - Q, Q)		4.5	1		32	ļ	39	ns
			6.0			28		34	
			2.0			195		235	
t _{PLH}	Low-level to high-level and		4.5			39	i	47	ns
	high-level to low-level		6.0		L	34		40	L
	output propagation time		2.0			195		235	
t _{PHL}	$(\overline{R_D} - Q, \overline{Q})$	`	4.5	}	1	39		47	ns
			6.0			34		40	
C ₁	Input capacitance					10		10	pF
C _{PD}	Power dissipation capacitance (Note 3)				52				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per flip flop)

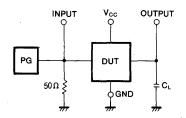
The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS ($v_{cc} = 2\sim 6v$, $T_a = -40\sim +85^{\circ}C$)

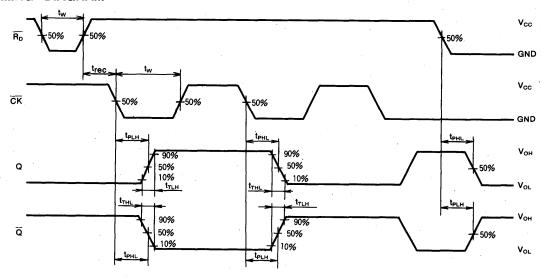
						Limits			
Symbol	Parameter	Test conditions	-	-	25℃		-40~	+85°C	Unit
'			V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0	80			101		
tw	CK, R _D pulse width	1.	4.5	16			20	Į	ns
			6.0	14			17		
	I K and the street with	1	2.0	100			125		
tsu	J, K setup time with respect to CK		4.5	20			25		ns
	respect to CK		6.0	17	l		21	_	
	1 K hald time with		2.0	0			0		
th	J, K hold time with respect to CK	1	4.5	0	1	1	0	1	ns
	respect to CK		6.0	0			0		
	R _D recovery time with		2.0	100			125		
trec	respect to CK		4.5	20			25		ns
	respect to OK		6.0	17			21		

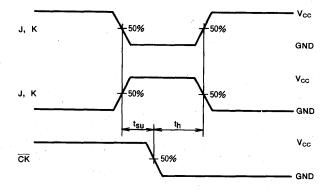
DUAL J-K FLIP-FLOP WITH RESET

Note 4: Test Circuit



- (1) The pulse generator (PG) has the following
- characteristics (10%~90%): t_t = 6ns, t_f = 6ns (2) The capacitance C_t · includes stray wiring capacitance and the probe input capacitance.





MITSUBISHI HIGH SPEED CMOS

M74HC74P/FP/DP

DUAL D-TYPE FLIP-FLOP WITH SET AND RESET

DESCRIPTION

The M74HC74 is a semiconductor integrated circuit consisting of two positive-edge triggered D-type flip flops with independent clock, data, and direct set and reset inputs.

FEATURES

- High-speed: (clock frequency)40MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 10µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: Ta=-40~+85℃

APPLICATION

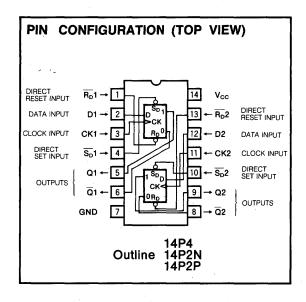
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC74 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS74.

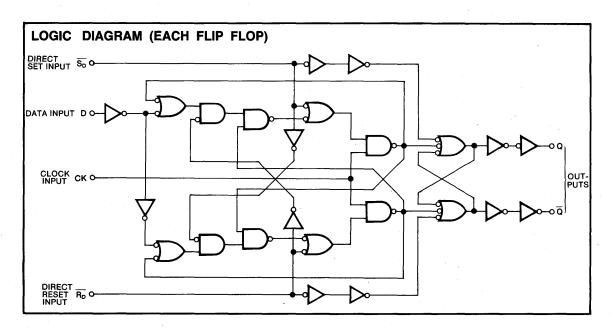
The M74HC74 contains two independent D-type flip flops with independent clock input CK, direct set input $\overline{S_D}$ and direct reset input $\overline{R_D}$.

When used as a D-type flip flop, $\overline{S_D}$ and $\overline{R_D}$ should be maintained at high-level. When CK changes from low-level to high-level, the signals just previously input present at D



appears at outputs $\mathbf Q$ and $\overline{\mathbf Q}$ in accordance with the function table given.

Use of $\overline{S_D}$ and $\overline{R_D}$ permits direct R-S flip flop operation. When $\overline{S_D}$ and $\overline{R_D}$ are low, Q and \overline{Q} will both become high. When $\overline{S_D}$ and $\overline{R_D}$ simultaneously become high , the condition of Q and \overline{Q} cannot be predetermined.



FUNCTION TABLE (Note 1)

	Inp	uts		Out	puts
SD	Rp	CK	D	/ Q	Q
L	н	×	х	н.	L
н	L	×	. X	L	Н
L	L	х	X	Н*	н*
н,	Н	L	×	Q°	Q°
Н	Н	Ť	Н	Н	L
Н	н	Ť.	L	L	Н
Н	Н	Н	X	Q°	ĝ
Н	Н	Ţ	X	Q°	Q°

Note 1 : X : irrelevant

: Change from low to high

: Change from high to low

Qº : Output state Q before clock input changed

© : Output state Q before clock input changed

*: When So and Ro are low, Q and Q will become both high. When So and $\overline{R_D}$ simultaneously become high the condition of Q and \overline{Q} cannot be predetermined.

ABSOLUTE MAXIMUM RATINGS ($\tau_a = -40 \sim +85 \, \text{°C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
•		V ₁ < 0V	20	
lik	Input protection diode current	$V_1 > V_{CC}$. 20	- mA
		V ₀ < 0V	-20	
юк	Output parasitic diode current	Vo > Vcc	20	mA mA
lo ·	Output current per output pin		±25	mA
lcc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		-65∼+150	°C

Note 2 : M74HC74FP, $T_a=-40\sim+60^\circ\text{C}$ and $T_a=60\sim85^\circ\text{C}$ are derated at -6mW/°C. M74HC74DP, $T_a=-40\sim+50^\circ\text{C}$ and $T_a=50\sim85^\circ\text{C}$ are derated at -5mW/°C.

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85^{\circ}C)$

Comple et	Parameter			Limits				
Symbol	Pa	Min	Тур	Max	Unit			
V _{CC}	Supply voltage		2		6	٧		
Vı	Input voltage		0		Vcc	٧		
Vo	Output voltage		0		Vcc	٧		
Topr	Operating temperature ra	inge	-40		+85	°C		
		$V_{CC} = 2.0V$	0		1000			
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns		
	$V_{CC} = 6.0V$		0		400	}		

ELECTRICAL CHARACTERISTICS

					Limits					
Symbol	Parameter	Test	Test conditions $V_{CC}(V)$		25℃			-40~+85℃		Unit
					Min	Тур	Max	Min	Max	l
		$V_{O} = 0.1V, V_{CO}$	_0.11/	2.0	1.5			1.5		
VIH	High-level input voltage		5—0.1 V	4.5	3. 15			3. 15		V
		1101 - 20µA	$ I_0 = 20\mu A$		4.2			4.2		
		V = 0.1V V	0.11/	2.0			0.5		0.5	
VIL	Low-level input voltage	$V_0 = 0.1V, V_{CC}$	2—0* 1 Å	4.5			1.35		1.35	v
	$ I_0 = 20\mu A$		6.0	ĺ		1.8		1.8		
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
			$I_{OH} = -20\mu A$	4.5	4.4			4.4		
V _{OH}	High-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		V
			$I_{OH} = -4.0 \text{mA}$	4.5	4. 18			4.13		
			$I_{OH} = -5.2 \text{mA}$	6.0	5. 68			5.63		
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
			$I_{OL} = 20 \mu A$	4.5			0.1	ļ	0.1	1
VoL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1	i	0.1	v
			I _{OL} = 4.0mA	4.5			0.26		0.33	
			$I_{OL} = 5.2 \text{mA}$	6.0			0.26		0.33	ĺ
l _{IH}	High-level input current	V ₁ == 6V		6.0			0.1		1.0	μА
I _{IL}	Low-level input current	V ₁ = 0V		6.0			-0.1		-1.0	μA
Icc	Quiescent supply current	VI = VCC, GND	$l_0 = 0 \mu A$	6.0			2.0		20.0	μΑ

SWITCHING CHARACTERISTICS ($v_{cc} = 5v$, $\tau_a = 25$ °C)

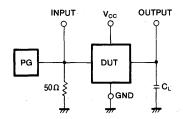
Symbol	Parameter	Test conditions		Unit		
Symbol	Parameter	l'est conditions	Min	Тур	Max	Unit
fmax	Maximum clock frequency		30			MHz
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time				10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = 15pF (Note 4)			30	ns
t _{PHL}	output propagation time (CK — Q, Q)				30	ns
t _{PLH}	Low-level to high-level and high-level to low-level	1 .		:	40	ns
t _{PHL}	output propagation time $(\overline{S_D}, \overline{R_D} - Q, \overline{Q})$				40	ns

SWITCHING CHARACTERISTICS $(v_{cc} = 2\sim6v, T_a = -40\sim+85^{\circ}C)$

						Limits			
Symbol	Parameter	Test conditions			25℃		40~	+85℃	Unit
		V _{cc} (V)		Min Typ		Max	Min Max]
			2.0	5			4		
fmax	Maximum clock frequency		4.5	27			21	İ	MHz
	J ¹		6.0	32	Ì		25	Ì	
]	2.0			75		95	
t _{TLH}	Low-level to high-level and		4.5			15		19	ns
	high lavel to lave lavel		6.0		}	13	}	16	
	high-level to low-level		2.0			75		95	
t _{THL}	output transition time		4.5		1	15]	19	ns
	-		6.0			13	<u> </u>	16	
]	2.0			175		220	
tpLH	Low-level to high-level and	C _L = 50pF (Note 4)	4.5			35	1	44	ns
	high-level to low-level		6.0			30		37	
	output propagation time		2.0			175		220	
t _{PHL}	(CK - Q, Q)		4.5		ļ	35	ļ	44	ns
			6.0		<u> </u>	30		37	
			2.0			230		290	
t _{PLH}	Low-level to high-level and		4. 5			46		58	ns
	high-level to low-level	·	6.0		<u> </u>	39		49	
	output propagation time		2.0			230		290	
t _{PHL}	$(\overline{S_D}, \overline{R_D} - Q, \overline{Q})$		4.5			46		58	ns
	.		6.0		L	39		49	
Cı	Input capacitance					10		10	pF
C _{PD}	Power dissipation capacitance (Note 3)				47				pF

Note 3 : CPD is the internal capacitance of the IC calculated from operation supply current under no-load conditions.(per flip-flop) The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$

Note 4: Test Circuit

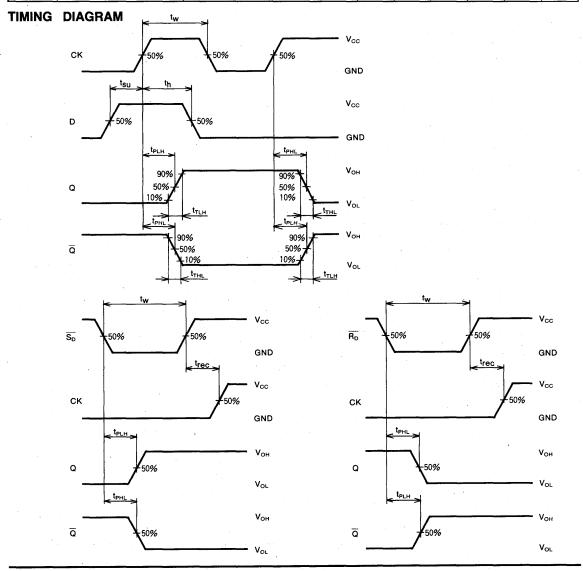


⁽¹⁾ The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns (2) The capacitance C_L includes stray wiring

capacitance and the probe input capacitance.

TIMING REQUIREMENTS ($V_{co} = 2\sim 6V$, $T_a = -40\sim +85^{\circ}C$)

				Limits					
Symbol	Parameter	Test conditions		25℃			-40~+85°C		Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	
			2. 0	, 80			101		
tw	CK, S _D , R _D pulse width		4. 5	16			20		ns
			6.0	14			17		ļ.
			2.0	100			126		
tsu	D setup time with		4.5	20			25		ns
	respect to CK		6.0	17		1	21	Ì	1
	21.1111	1	2.0	. 0			0		
th	D hold time with		4.5	0.			0		ns
	respect to CK		6.0	0			0		
			2.0	5			5		
trec	R _D , S _D recovery time with		4.5	5			5		ns
	respect to CK		6.0	5			5		



MITSUBISHI HIGH SPEED CMOS

M74HC75P/FP/DP

DUAL 2-BIT TRANSPARENT LATCH

DESCRIPTION

The M74HC75 is a semiconductor integrated circuit consisting of four bistable latches with outputs Q and \overline{Q} .

FEATURES

- High-speed: 14ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 10μW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

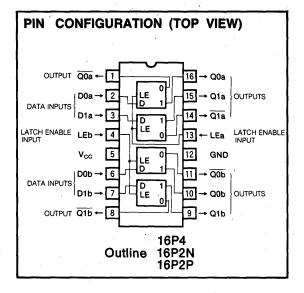
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC75 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS75.

The use of buffered outputs Q and \overline{Q} improves the input to output transfer characteristics and minimizes output impedance variations with respect to input voltage variations.

The M74HC75 has four D-type latches, and is provided with latch enable inputs LE common to two circuits each. When LE is high, the data from the data input D will appear in the outputs Q and \overline{Q} . When the D signal changes, the signal that appears in outputs Q and \overline{Q} also will change. When LE changes from high to low, the status of D immediately before the change will be latched. While LE is low, Q and \overline{Q} will not change even if D changes.

A unit, the M74HC375 having the same functions and elec-

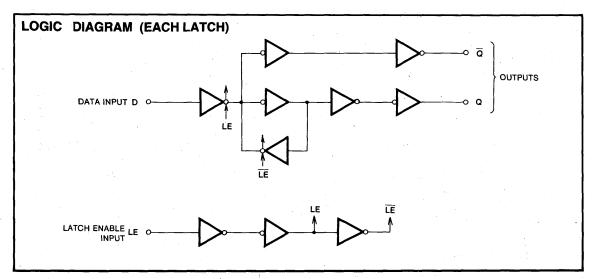


trical characteristics as the M74HC75 is also available. This offers easy mounting with pin 8 and 16 being GND and V_{CC} respectively.

FUNCTION TABLE (Note 1)

Int	outs	Outputs				
LE	D	Q	Q			
Н	Н	Н	, L			
Н	L	L	н			
L	X	Q°	Q°			

Note 1 : Q^0 , \overline{Q}^0 : Output state Q, \overline{Q} before input condition is set X : Irrelevant





M74HC75P/FP/DP

DUAL 2-BIT TRANSPARENT LATCH

ABSOLUTE MAXIMUM RATINGS $(T_a = -40 \sim +85 ^{\circ}C)$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage		-0.5~+7.0	V
Vi	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
		V ₁ < 0V	-20	
lικ	Input protection diode current	$V_1 > V_{CC}$	20	. mA
		V ₀ < 0V	-20	
Гок	Output parasitic diode current	Vo > Vcc	20	mA
lo	Output current per output pin		±25	mA
lcc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65~ + 150	°C

Note 2 : M74HC75FP, $T_a=-40\sim+70^\circ\mathrm{C}$ and $T_a=70\sim85^\circ\mathrm{C}$ are derated at $-6\mathrm{mW/C}$. M74HC75DP, $T_a=-40\sim+50^\circ\mathrm{C}$ and $T_a=50\sim85^\circ\mathrm{C}$ are derated at $-5\mathrm{mW/C}$.

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85 \degree c)$

O	Parameter						
Symbol	Pa	rameter	Γ	Min	Тур	Max	Unit
Vcc	Supply voltage			2		6	٧
V _I	Input voltage			0		Vcc	٧
Vo	Output voltage			0		Vcc	٧
Topr	Operating temperature ra	ange		-40		+85	Ç
		$V_{CC} = 2.0V$		0		1000	-
tr, tf	Input risetime, falltime	$V_{CC} = 4.5V$		0	1	500	ns
		$V_{CC} = 6.0V$		0		400	

ELECTRICAL CHARACTERISTICS

	1	1			Limits					
Symbol	Parameter	Test	Test conditions $V_{CC}(V)$		25°C			-40~+85℃		Unit
•		1			Min	Тур	Max	Min	Max	
		$V_0 = 0.1V, V_{00}$	- 0.11/	2.0	1.5			1.5		
V _{IH}	High-level input voltage	$ I_0 = 20\mu A$	c—0.1 V	4.5	3.15			3.15		V
		$ 10 = 20\mu\text{A}$		6.0	4.2			4.2		
		V = 0.1V V	-0.14	2.0			0.5		0.5	
VIL	Low-level input voltage]	$V_0 = 0.1V, V_{CC} - 0.1V$ $ I_0 = 20\mu A$	4.5			1.35		1.35	V
	* *	$ 1_0 = 20\mu A$		6.0			1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
	High-level output voltage $V_i = V_{iH}, \ V_{iL}$	$I_{OH} = -20\mu A$	4.5	4.4			4. 4			
V _{OH}		$V_{I} = V_{IH}, V_{IL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		v
			$I_{OH} = -4.0 \text{mA}$	4.5	4.18			4.13		
			$I_{OH} = -5.2 \text{mA}$	6.0	5.68			5.63		
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
	· ·		$I_{OL} = 20 \mu A$	4.5			0.1		0.1	
VoL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1	!	0.1	v
			I _{OL} = 4.0mA	4. 5			0. 26		0.33	
ĺ			I _{OL} == 5. 2mA	6.0			0. 26		0.33	
I _{IH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μA
I _{IL}	Low-level input current	V ₁ = 0V		6.0			-0.1		-1.0	μF
cc	Quiescent supply current	VI = VCC, GND	$I_0 = 0 \mu A$	6.0			2.0		20.0	μF

DUAL 2-BIT TRANSPARENT LATCH

SWITCHING CHARACTERISTICS ($V_{cc} = 5V$, $T_a = 25^{\circ}C$)

Comple ed	Do	Took conditions	Limits			Unit
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time				10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	·			23	ns
t _{PHL}	output propagation time (D — Q)				23	ns
t _{PLH}	Low-level to high-level and high-level to low-level	0 15 5 (11 1)			20	ns
t _{PHL}	output propagation time $(D-\overline{Q})$	C _L = 15pF (Note 4)			20	ns
tpLH	Low-level to high-level and high-level to low-level				27	ns
t _{PHL}	output propagation time (LE - Q)				27	ns
t _{PLH}	Low-level to high-level and high-level to low-level	·			23	ns
t _{PHL}	output propagation time (LE $-\overline{\mathbf{Q}}$)				23	ns

SWITCHING CHARACTERISTICS ($V_{cc} = 2\sim 6V$, $T_a = -40\sim +85^{\circ}C$)

						Limits			Ì
Symbol	Parameter	Test conditions			25℃		−40 ~	+85℃	Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max] .
			2.0			75		95	
t _{TLH}	Low-level to high-level and		4.5			15		19	ns
			6.0			13	i	16	}
	high-level to low-level	•	2.0			-75		95	
t _{THL}	output transition time		4.5			15	İ	19	ns
			6.0		ł	13	}	16	
		Ī	2.0			125		156	<u> </u>
tpLH	Low-level to high-level and		4.5			25		32	ns
	high-level to low-level		6.0			21	ļ	27	\
	output propagation time		2.0			125		156	
t _{PHL}	(D-Q)		4.5		Ì	25)	32	ns
			6.0			21	Ĭ	27	
		1	2.0			110		138	
t _{PLH}	Low-level to high-level and		4.5			22		28	ns
	high-level to low-level		6.0		ļ	19	ļ	24	
	output propagation time	C _L = 50pF (Note 4)	2.0			110		138	
tpHL	$(D-\overline{Q})$		4.5			22	ł	28	ns
			6.0		ĺ	19	ļ	24	
		1	2.0	7.		145		181	
t _{PLH}	Low-level to high-level and		4.5			29	1	36	ns
	high-level to low-level		6.0			25	ĺ	31	
	output propagation time		2.0			145		181	
tenL	(LE - Q)		4.5		1	29		36	ns
			6.0			25		31	
		1	2.0		-	125		156	
tpLH	Low-level to high-level and	1	4.5			25		31	ns
	high-level to low-level		6.0		1	- 22		28	
	output propagation time		2.0			125		156	
t _{PHL}	(LE - Q)		4.5	*.		25		31	ns
		·	6.0			22		28	
Cı	Input capacitance					10		10	ρF
C _{PD}	Power dissipation capacitance (Note 3)				46		 	 	pF

Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per latch)
The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$

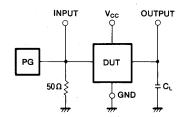


DUAL 2-BIT TRANSPARENT LATCH

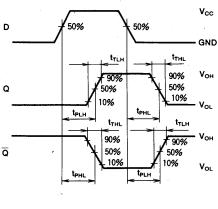
TIMING REQUIREMENT $(v_{cc} = 2\sim 6v, T_a = -40\sim +85^{\circ}C)$

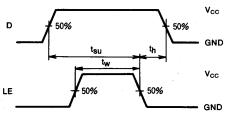
						Limits			
Symbol	Parameter	Test conditions			25℃		−40 ~	+85℃	Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0	- 80			100		
tw	LE pulse width		4.5	16		i	20		ns
		,	6.0	14			18		
	D		2.0	100			125		
t _{su}	D setup time with respect to LE		4.5	20			25		ns
	respect to LE		6.0	• 17			21		
	D hold time with]	2.0	5			5		
th	respect to LE		4.5	5			5	}	ns
	respect to LE		6.0	5			5		

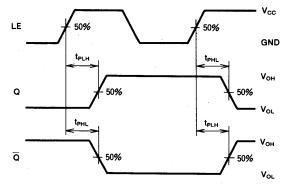
Note 4: Test Circuit



- (1) The pulse generator (PG) has the following characteristics (10%~90%): $\rm t_f=6ns, \ t_f=6ns$
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.







M74HC76P/FP/DP

DUAL J-K FLIP-FLOP WITH SET AND RESET

DESCRIPTION

The M74HC76 is a semiconductor integrated circuit consisting of two negative-edge triggered J-K flip flops with independent control inputs.

FEATURES

- High-speed: 50MHz clock frequency typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 10µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85°C

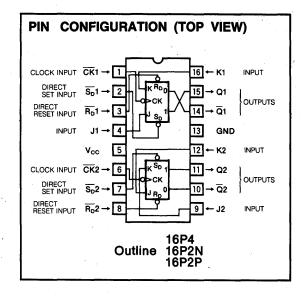
APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

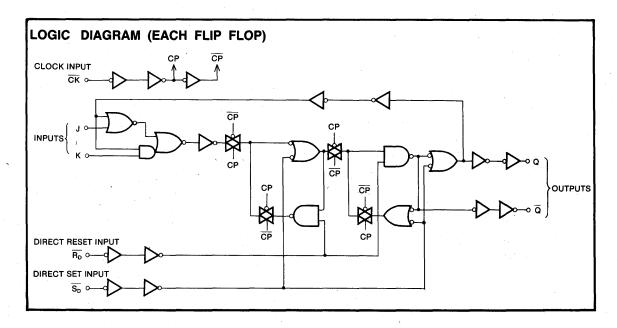
Use of silicon gate technology allows the M74HC76 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS76.

The M74HC76 contains two edge-triggered J-K flip flops, each circuit with independent clock input \overline{CK} , direct set input $\overline{S_D}$ and direct reset input $\overline{R_D}$, and both inputs J and K. When \overline{CK} is high, the J and K signals can be read. When \overline{CK} changes from high-level to low-level, the signals just previously input at J and K appear at outputs Q and \overline{Q} in



accordance with the function table given. Use of $\overline{S_D}$ and $\overline{R_D}$ permits direct R-S flip flop operation. When $\overline{S_D}$ and $\overline{R_D}$ are low, Q and \overline{Q} will both become high but when $\overline{S_D}$ and $\overline{R_D}$ simultaneously become high, the condition of Q and \overline{Q} cannot be predetermined. When used as a J-K flip flop, $\overline{S_D}$ and $\overline{R_D}$ should be maintained at high-level.

A unit, the M74HC112, having the same functions and electrical characteristics as the M74HC76 is also available. This offers easy mounting with pin 8 and 16 being GND and $V_{\rm CC}$ respectively.



FUNCTION TABLE (Note 1)

		Inputs			Out	puts
S _D	R _D	CK	J.	K	Q	[Q
L	Н	X	X	X	Н	L
Н	L	X	×	×	L	н
L	L	х	X	х	н*	н*
Н	Н	ţ	L	L	Q°	Q°
Н	H.	↓	L	Н	L	н
Н	Н	. ↓	н	L	н	L
н	н	. ↓	н	Н	Тор	gle
Н	Н	L	X	×	Q°	Q°
Н	Н	н .	X	×	Q°	Q٥
Н	н	t	X	x	Q°	Q°

Note 1:

: Change from low to high : Change from high to low

: Irrelevant

x <u>Q</u>° Q°

: Output state Q before clock input changed Output state Q before clock input changed Toggle: Inversion state before clock input changed

: When $\overline{S_D}$ and $\overline{R_D}$ are low, Q and \overline{Q} becomes high. When $\overline{S_D}$ and $\overline{R_D}$ become high simultaneously the condition of Q and \overline{Q} cannot be prodetermined.

ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85 \degree$ C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
		V ₁ < 0V	-20	
lik	Input protection diode current	$v_i > v_{cc}$	20	mA mA
		V ₀ < 0V	-20	
lok	Output parasitic diode current	Vo > Vcc	20	mA
lo	Output current per output pin		±25	mA
Icc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65~+150	ဗ

Note 2 : M74HC76FP, $T_a=-40\sim+70^{\circ}C$ and $T_a=70\sim85^{\circ}C$ are derated at -6mW/°C. M74HC76DP, $T_a=-40\sim+50^{\circ}C$ and $T_a=50\sim85^{\circ}C$ are derated at -5mW/°C.

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85 \degree c)$

Oursels at	D	ameter		Limits		· I I mil
Symbol	Pai	Min	Тур	Max	Unit	
Vcc	Supply voltage		2		6	٧
V _i	Input voltage		0		Vcc	٧
V _o	Output voltage		0		Vcc	٧
Topr	Operating temperature ra	inge	-40		+85	°
		$V_{CC} = 2.0V$	0		1000	
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns
		$V_{CC} = 6.0V$	0		400	

ELECTRICAL CHARACTERISTICS

					Limits					
Symbol	Parameter	Test	Test conditions V _{CC} (V)		25℃			-40~+85°C		Unit
					Min	Тур	Max	Min	Max]
		Vo = 0.1V, Vo	-0.11/	2.0	1.5			1.5		
VIH	High-level input voltage	$ I_0 = 20\mu A$	50. I V	4.5	3.15			3. 15		V
		$ 1_0 = 20\mu\text{A}$		6.0	4.2			4. 2		
		V = 0.1V V	-0.11/	2.0			0.5		0.5	
VIL	Low-level input voltage	$V_0 = 0.1V, V_{CO}$ $ I_0 = 20\mu A$	0-0.1 V	4.5			1.35	,	1.35	V
		1101 — 20μΑ		6.0			1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
			$I_{OH} = -20 \mu A$	4.5	4. 4			4.4		
V _{OH}	High-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		V
			$I_{OH} = -4.0 \text{mA}$	4.5	4. 18			4.13		1 .
			$I_{OH} = -5.2 \text{mA}$	6.0	5. 68			5. 63		
	,		$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
			$I_{OL} = 20 \mu A$	4.5			0.1		0.1	Į.
VoL	Low-level output voltage	$V_i = V_{iH}, \ V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
			I _{OL} = 4.0mA	4.5			0. 26		0.33	
			$I_{OL} = 5.2 \text{mA}$	6.0		-	0. 26		0.33	
l _{IH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μA
I _{IL}	Low-level input current	V ₁ = 0V		6.0			-0.1		-1.0	μА
Icc	Quiescent supply current	VI = VCC, GND	$l_0 = 0 \mu A$	6.0			2.0		20.0	μA

SWITCHING CHARACTERISTICS $(v_{cc} = 5v, \tau_a = 25^{\circ}C)$

			Limits			Unit
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
fmax	Maximum clock frequency		30			MHz
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time	1			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level				26	ns
t _{PHL}	output propagation time (CK - Q, Q)	C _L = 15pF (Note 4)			26	ns
t _{PLH}	Low-level to high-level and high-level to low-level				, 33	ns
t _{PHL}	output propagation time $(\overline{R_D} - Q, \overline{Q})$				33	ns
t _{PLH}	Low-level to high-level and high-level to low-level	1			33	ns
t _{PHL}	output propagation time (SD - Q, Q)				33	ns

SWITCHING CHARACTERISTICS ($V_{cc} = 2\sim6V$, $T_a = -40\sim+85^{\circ}C$)

						Limits			
Symbol	Parameter	Test conditions			25℃		−40 ~	+85°C	Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0	5			4		
fmax	Maximum clock frequency		4.5	27			21		MHz
			6.0	31			24		-
			2.0			75		95	
t _{TLH}	Low-level to high-level and		4.5			15		19	ns
	hish tourist to law touri		6.0			13		16	
	high-level to low-level	·	2.0			75		95	
t _{THL}	output transition time		4.5			15		19	ns
		·	6.0			13		16	l
		-	2.0			150		180	
t _{PLH}	Low-level to high-level and		4.5			30		36	ns
	high-level to low-level		6.0			26		32	
	output propagation time		2.0			150		180	
t _{PHL}	$(\overline{CK} - Q, \overline{Q})$	C _L = 50pF (Note 4)	4.5			30		36	ns
			6.0			26		32	
			2.0			190		230	
t _{PLH}	Low-level to high-level and		4.5			38		46	ns
	high-level to low-level	•	6.0			33		40	
	output propagation time		2.0			190		230	
t _{PHL}	$(\overline{R_D} - Q, \overline{Q})$		4.5			38		46	ns
		•	6.0			33	-	40	
			2.0			190		230	,
t _{PLH}	Low-level to high-level and		4.5			38		46	ns
	high-level to low-level		6.0			33		40	
	output propagation time		2.0			190		230	
t _{PHL}	$(\overline{S_D} - Q, \overline{Q})$		4.5			38		46	ns
			6.0			33		40	
Cı	Input capacitance					10		10	pF
C _{PD}	Power dissipation capacitance (Note 3)				56			,	pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per flip flop)

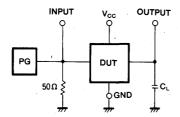
The power dissipated during operation under no-load conditions is calculated using the following formula:

P_D = C_{PD} · V_{CC}² · f₁+I_{CC} · V_{CC}

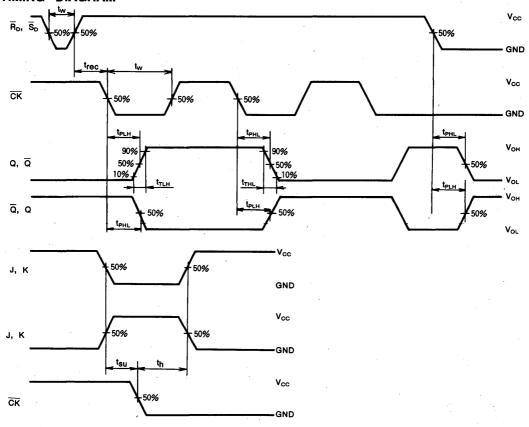
TIMING REQUIREMENTS ($v_{cc} = 2\sim6$ V, $\tau_a = -40\sim+85$ °C)

						Limits			
Symbol	Parameter	Test conditions			25℃	*	-40~	+85°C	Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0	80			101		
tw	CK, S _D , R _D pulse width		4.5	16			20		ns
			6.0	14			17	1	
·		7	2.0	100			125		
tsu	J, K setup time with		4.5	20			25		ns
	respect to CK		6.0	17		1	21		
			2.0	0			. 0		
th	J, K hold time with		4.5	0			0		ns
	respect to CK		6.0	0			0		
			2.0	100			125		
trec	R _D , S _D recovery time with		4.5	20			25		ns
	respect to CK		6.0	17			21		

Note 4: Test Circuit



- (1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns (2) The capacitance C_L includes stray wiring
- capacitance and the probe input capacitance.



MITSUBISHI HIGH SPEED CMOS

M74HC85P/FP/DP

4-BIT MAGNITUDE COMPARATOR

DESCRIPTION

The M74HC85 is a semiconductor intergrated circuit consisting of a 4-bit digital comparator.

FEATURES

- High-speed: 21ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2∼6V
- Wide operating temperature range: Ta=−40~+85°C

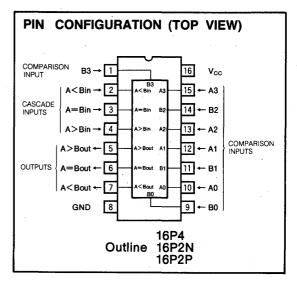
APPLICATION

General purpose, for use in industrial and consumer digital equipment.

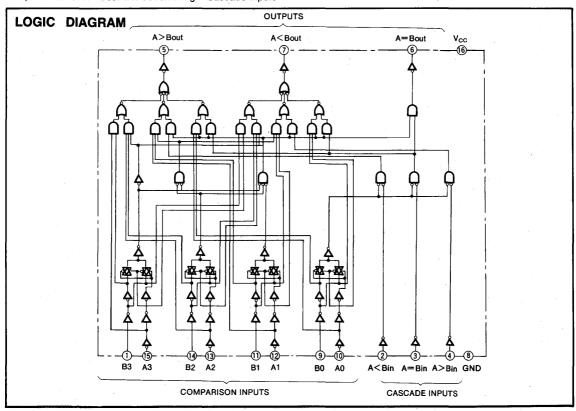
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC85 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS85.

When two 4-bit binary A and B are applied to comparison inputs A0~A3, B0~B3, and cascade input A=Bin is high, the values will be compared and the appropriate output A>Bout, A=Bout or A<Bout will become high. Cascade inputs



A>Bin, A=Bin and A<Bin can be connected in cascade to increase the number of bits. (Refer to Application Example)





M74HC85P/FP/DP

4-BIT MAGNITUDE COMPARATOR

FUNCTION TABLE (Note 1)

			Inputs					Outputs	
A3, B3	A2, B2	A1, B1	A0, B0	A>Bin	A <bin< th=""><th>A≔Bin</th><th>A>Bout</th><th>A<bout< th=""><th>A=Bout</th></bout<></th></bin<>	A≔Bin	A>Bout	A <bout< th=""><th>A=Bout</th></bout<>	A=Bout
A3>B3	X	×	×	×	X	х	Н	L	L
A3 <b3< td=""><td>X</td><td>X</td><td>×</td><td>×</td><td>×</td><td>×</td><td>L</td><td>н</td><td>L</td></b3<>	X	X	×	×	×	×	L	н	L
A3=B3	A2>B2	X	Х	Χ	×	×	Н	L	L
A3=B3	A2 <b2< td=""><td>×</td><td>×</td><td>X</td><td>×</td><td>×</td><td>· L</td><td>Н</td><td>L</td></b2<>	×	×	X	×	×	· L	Н	L
A3=B3	A2=B2	A1>B1	×	X	×	X	н	L	L
A3=B3	A2≔B2	A1 <b1< td=""><td>X</td><td>х</td><td>×</td><td>x</td><td>L</td><td>• н</td><td>L</td></b1<>	X	х	×	x	L	• н	L
A3=B3	A2=B2	A1=B1	A0>B0	х	×	Х	Н	. L	L
A3=B3	A2=B2	A1=B1	A0 <b0< td=""><td>X</td><td>x</td><td>×</td><td>. L</td><td>н</td><td>L</td></b0<>	X	x	×	. L	н	L
A3=B3	A2=B2	A1=B1	A0=B0	Н	L	L	Н	L	L
A3=B3	A2=B2	A1≕B1	A0=B0	L	H	L	L,	Н	L
A3=B3	A2=B2	A1=B1	A0=B0	х	х	Н	L	L	Н
A3=B3	A2=B2	A1=B1	A0=B0	Н	Н	L	L	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	L	Н	Н	L

Note 1 : X: Irrelevant

ABSOLUTE MAXIMUM RATINGS ($\tau_a = -40 \sim +85$ °C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		<i>-</i> 0.5∼+7.0	V
V _I	Input voltage		-0.5~V _{cc} +0.5	V
V _o	Output voltage		-0.5~V _{cc} +0.5	V
	1	v _i < 0v	-20	
l _{iK}	Input protection diode current	$v_i > v_{cc}$	20	mA
	Out-of-seconds diede conset	V ₀ < 0V	-20	
юк	Output parasitic diode current	Vo > Vcc	20	mA
l _o	Output current per output pin		±25	mA
Icc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		-65∼+150	°C

Note 2 : M74HC85FP, $T_a=-40\sim+70^\circ$ C and $T_a=70\sim85^\circ$ C are derated at -6mW/°C. M74HC85DP, $T_a=-40\sim+50^\circ$ C and $T_a=50\sim85^\circ$ C are derated at -5mW/°C.

4-BIT MAGNITUDE COMPARATOR

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85 \degree C)$

Symbol	Dor		Unit				
Syllibol	rai	ameter	Min	Тур	Max	Omi	
Vcc	Supply voltage	2		6	>		
Vı	Input voltage		0		Vcc	٧	
Vo	Output voltage		0		V _{cc}	٧	
Topr	Operating temperature ra	nge	-40		+85	°	
		V _{CC} = 2.0V	0		1000		
t _r , t _f	Input rise time, fall time	$V_{CC} = 4.5V$	0		500	ns	
		$V_{CC} = 6.0V$	0		400	1	

ELECTRICAL CHARACTERISTICS

							Limits			
Symbol	Parameter	Test	conditions			25℃		-40~	+85℃	Unit
			V _{cc} (V)		Min	Тур	Max	Min	Max	
		, y = 0.1V, y	$V_0 = 0.1V, V_{CC} - 0.1V$		1.5			1.5		
V_{1H}	High-level input voltage			4.5	3.15			3.15		V
		$ 1_0 = 20\mu A$	$ I_0 = 20\mu A$		4.2			4.2		
		V = 0.1V V					0.5		0.5	
V_{IL}	Low-level input voltage	$V_0 = 0.1V, V_{CO}$ $ I_0 = 20\mu A$	5—0. T V	4.5	1.		1.35		1.35	V
		$ 1_0 = 20\mu A$		6.0			1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9	· .	
			$I_{OH} = -20\mu A$	4.5	4.4			4. 4		
V _{OH}	High-level output voltage	$V_i = V_{iH}, \ V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		V
			$I_{OH} = -4.0 \text{mA}$	4.5	4.18			4.13		
			$I_{OH} = -5.2 \text{mA}$	6.0	5. 68			5. 63		
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
			$I_{OL} = 20 \mu A$	4.5			0.1		0.1	
VoL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
	· ·		I _{OL} = 4.0mA	4. 5			0.26		0.33	
-			$I_{OL} = 5.2 \text{mA}$	6.0			0.26		0.33	
l _{iH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μA
l _{IL}	Low-level input current	$V_i = 0V$	V _i = 0V				—0. 1		-1.0	μA
Icc	Quiescent supply current	VI = VCC, GND	$I_0 = 0 \mu A$	6.0			4.0		40.0	μА

SWITCHING CHARACTERISTICS ($v_{cc} = 5v$, $t_a = 25^{\circ}C$)

Symbol	Parameter	Took and distant	Limits			Unit
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time				10	ns
t _{PLH}	Low-level to high-level and high-level to low-level				40	ns
t _{PHL}	output propagation time (A, B $-$ A $>$ Bout, A $<$ Bout)				40	ns
t _{PLH}	Low-level to high-level and high-level to low-level	· ·			35	ns
t _{PHL}	output propagation time (A, B $-$ A $=$ Bout)	0 = 15-5 (N-4-4)			35	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = 15pF (Note 4)			30	ns
t _{PHL}	output propagation time (A < Bin, A = Bin - A > Bout)				30	ns
t _{PLH}	Low-level to high-level and high-level to low-level				30	ns
t _{PHL}	output propagation time (A > Bin, A = Bin - A < Bout)	'	-		30	ns
t _{PLH}	Low-level to high-level and high-level to low-level				25	ns
t _{PHL}	output propagation time(A = Bin - A = Bout)			,	25	ns

MITSUBISHI HIGH SPEED CMOS M74HC85P/FP/DP

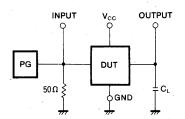
4-BIT MAGNITUDE COMPARATOR

SWITCHING CHARACTERISTICS ($V_{cc} = 2\sim 6V$, $T_a = -40\sim +85$ °C)

Cumbal	Peremeter	Took conditions			25%	Limits	40-	1.05%	
Symbol	Parameter	Test conditions	()		25℃			+85°C	Uni
			V _{cc} (V)	Min	Тур	Max	Min	Max	-
	1	_	2.0			75		95	
t _{TLH}	Low-level to high-level and		4.5			15		19	ns
	high-level to low-level		6.0			13		16	
			2.0			75		95	
t _{THL}	output transition time		4.5			15		19	ns
			6.0		1.1	13		16	
			2, 0		1	230	· .	290	
t _{PLH}	Low-level to high-level and		4.5			. 46		58	ns
	high-level to low-level		6.0			39		49	
	output propagation time		2.0			230		290	
t _{PHL}	(A, B - A > Bout, A < Bout)		4.5			46	1	58	ns
			6.0	-		39		49	1
			2.0			200		252	
t _{PLH}	Low-level to high-level and		4.5			40		50	ns
	high-level to low-level	1	6.0			34		43	
•	output propagation time		2.0			200		252	
t _{PHL}	(A, B-A=Bout)		4.5			40		50	ns
			6.0			34		43	
		C _L = 50pF (Note 4)	2.0			175		221	
t _{PLH}	Low-level to high-level and		4.5			35		44	l ns
T-CH	high-level to low-level		6.0			30		37	
	output propagation time		2.0			175		221	
t _{PHL}	(A < Bin, A = Bin - A > Bout)		4.5		1	35		44	ns
PHL	(A Com, A Om A Odd)		6.0			30		37	'''
		-	2. 0		1	175	 	221	
+	Low-level to high-level and		4.5			35	1	44	ns
t _{PLH}	high-level to low-level		6.0			30		37	"
	-					175	-		
	output propagation time		2.0 4.5			35		221 44	
t _{PHL}	(A > Bin, A = Bin - A < Bout)		1						ns
		1	6.0		 	30		37	
	Law laws to bish laws to a	`	2.0			145		183	
t _{PLH}	Low-level to high-level and		4.5	•		29		37	ns
	high-level to low-level	1	6.0	-		25	ļ	31	
_	output propagation time		2.0			145		183	Ì
t _{PHL}	(A = Bin - A = Bout)		4.5			29		37	ns
			6.0			25	ļ	31	ļ
Cı	Input capacitance					10	1	10	pF
CPD	Power dissipation capacitance (Note 3)				81.				pF

Note 3: CPD is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$

Note 4: Test Circuit

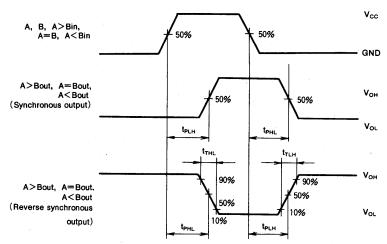


- (1)The pulse generator (PG) has the following characteristics (10% \sim 90%): $t_{\rm f}=6{\rm ns},\,t_{\rm f}=6{\rm ns}$ (2) The capacitance $C_{\rm L}$ includes stray wiring
- capacitance and the probe input capacitance.

M74HC85P/FP/DP

4-BIT MAGNITUDE COMPARATOR

TIMING DIAGRAM



MITSUBISHI HIGH SPEED CMOS

M74HC86P/FP/DP

QUADRUPLE 2-INPUT EXCLUSIVE OR GATE

DESCRIPTION

The M74HC86 is a semiconductor integrated circuit consisting of four 2-input exclusive OR gates.

FEATURES

- High-speed: 9ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC86 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS86.

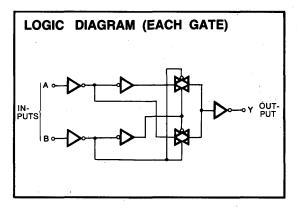
Buffered outputs Y improve input-to-output transfer characteristics and reduce to a minimum output impedance variations with respect to input voltage variations.

When both inputs A and B are either high or low, the output Y will become low, and when the level of A and B are opposite, Y will become high.

FUNCTION TABLE

Inp	uts	Output	
Α	A B		
L	L	L	
Н	L	H.	
L	Н	Н	
н	Н	L	

PIN CONFIGURATION (TOP VIEW) INPUTS OUTPUT Y1 + 3 OUTPUT Y2 + 6 GND 7 INPUTS 14P4 Outline 14P4 Outline 14P2N 14P2P



ABSOLUTE MAXIMUM RATINGS $(\tau_a = -40 \sim +85 \degree$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	٧
\mathbf{V}_{l}	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
	4	V ₁ < 0V	-20	4
lik	Input protection diode current	$V_i > V_{CC}$	20	mĄ.
	O to A consider diada	V ₀ < 0V	-20	
lok	Output parasitic diode current	Vo > Vcc	20	mA
lo	Output current per output pin		±25	· mA
lcc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65~+150	°C

Note 1 : M74HC86FP, T $_a$ = $-40\sim$ +60°C and T $_a$ = $60\sim$ 85°C are derated at -6mW/°C. M74HC86DP, T $_a$ = $-40\sim$ +50°C and T $_a$ = $50\sim$ 85°C are derated at -5mW/°C.



QUADRUPLE 2-INPUT EXCLUSIVE OR GATE

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85^{\circ}C)$

Complement	Do			Limits				
Symbol	Pa	rameter	Min	Min Typ		Unit		
Vcc	Supply voltage		. 2		- 6	٧		
Vı	Input voltage		0		Vcc	٧		
Vo	Output voltage		0		Vcc	٧		
Topr	Operating temperature ra	ange	-40		+85	°C		
		$V_{CC} = 2.0V$	0		1000			
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns		
		$V_{CC} = 6.0V$			400			

ELECTRICAL CHARACTERISTICS

			<u></u>				Limits			
Symbol	Parameter	Test	conditions			25℃		−40~		Unit
1				V _{cc} (V)	Min	Тур	Max	Min	Max	•
		V - 0 1V V	$V_0 = 0.1V, V_{CC} = 0.1V$		1.5			1.5		
VIH	High-level input voltage	$ V_0 = 0.1V, V_{C} $ $ I_0 = 20\mu A$		4.5	3. 15			3.15		V
		$ 10 = 20\mu$ A	$ I_0 = 20\mu$ A		4.2			4.2		
		V -0.1V V	$V_0 = 0.1V, V_{CC} = 0.1V$				0.5		0.5	
VIL	Low-level input voltage	$ V_0 = 0.1V, V_{CI}$ $ I_0 = 20\mu A$	C-0.1V	4.5	i		1.35		1.35	V
	e e e e	1101 - 20µA		6.0			1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
			$I_{OH} = -20\mu A$	4.5	4. 4			4. 4		
VoH	High-level output voltage	$V_{I} = V_{IH}, V_{IL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		V,
			$I_{OH} = -4.0 \text{mA}$	4.5	4. 18			4.13		
			$I_{OH} = -5.2 \text{mA}$	6.0	5. 68			5.63		
	·	,	$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
	1		$I_{OL} = 20 \mu A$	4.5		1.	0.1		0.1	
VOL	Low-level output voltage	$V_{l} = V_{lH}, V_{lL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
			$I_{OL} = 4.0 \text{mA}$	4.5			0.26		0.33	
			I _{OL} = 5. 2mA	6.0			0. 26		0.33	
I _{IH}	High-level input current	V ₁ = 6V		6.0			0. 1		1.0	μΑ
I _{IL}	Low-level input current	$V_i = 0V$		6.0			-0.1		-1.0	μA
Icc	Quiescent supply current	VI = VCC, GND	$I_0 = 0\mu A$	6.0			1.0		10.0	μΑ

SWITCHING CHARACTERISTICS $(v_{cc} = 5v, T_a = 25\%)$

Symbol	Parameter	Test conditions		Unit		
Symbol	Falametei	Test conditions	Min	Тур	Max	Oint
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time	C ₁ = 15pF (Note 3)			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	CL — 15pr (Note 5)			20	ns
t _{PHL}	output propagation time				20	ns

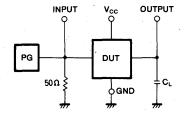
QUADRUPLE 2-INPUT EXCLUSIVE OR GATE

SWITCHING CHARACTERISTICS ($V_{cc} = 2\sim6V$, $T_a = -40\sim+85$ °C)

					Limits				
Symbol	Parameter	Test conditions V _{CC} (V)		25℃			-40~+85°C		Unit
				Min	Тур	Max	Min	Max	
			2.0			75		95	
t _{TLH}	Low-level to high-level and	. "	4.5		ļ.	15		19	ns
			6.0			13		16	
	high-level to low-level		2.0			75		95	
t _{THL}	output transition time		4.5		Į	-15		19	ns
	ļ	50.5(0) . 0)	6.0]	13		16	
		$C_L = 50 pF \text{ (Note 3)}$	2.0			120		151	
t _{PLH}	Low-level to high-level and		4.5			24		30	ns
	1		6.0			20		26	
	high-level to low-level		2.0			120		151	
t _{PHL}	output propagation time	· ·	4.5]	24		30	ns
	¥		6.0		1	20		26	
c	Input capacitance					10		1.0	рF
C _{PD}	Power dissipation capacitance (Note 2)				41				pF

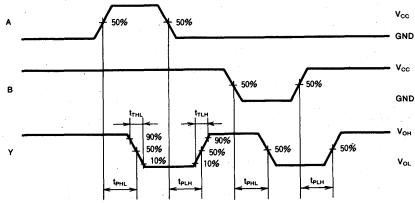
Note 2: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.(per gate) The power dissipated during operation under no-load conditions is calculated using the following formula: $P_{D} = C_{PD} \cdot V_{CC}^2 \cdot f_{|+} I_{CC} \cdot V_{CC}$

Note 3: Test Circuit



- (1) The pulse generator (PG) has the following characteristics (10% \sim 90%): $t_{\rm f}=6$ ns, $t_{\rm f}=6$ ns
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



MITSUBISHI HIGH SPEED CMOS

M74HC107P/FP/DP

DUAL J-K FLIP-FLOP WITH RESET

DESCRIPTION

The M74HC107 is a semiconductor integrated circuit consisting of two negative-edge triggered J-K flip flops with independent control inputs

FEATURES

- High-speed: 50MHz clock frequency typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 10µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=-40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

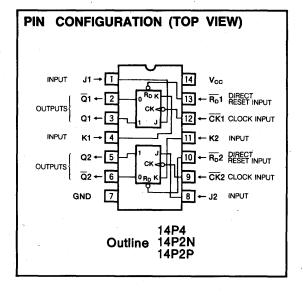
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC107 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS107.

The M74HC107 contains two edge-triggered J-K flip flops, each circuit with independent clock input \overline{CK} , direct reset input $\overline{R_D}$, and both inputs J and K.

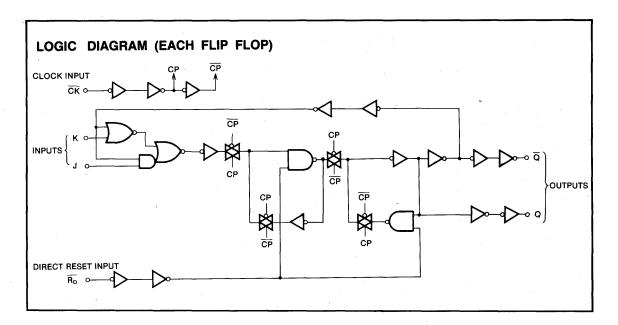
When \overline{CK} is high, the J and K signals can be read.

When CK changes from high-level to low-level, the signals just previously input at J and K appear at outputs Q and \overline{Q}



in accordance with the function table given. When $\overline{R_D}$ is low, Q and \overline{Q} will become low and high respectively, irrespective of other inputs. When used as a J-K flip flop, $\overline{R_D}$ should be maintained at high-level.

M74HC107 is the same functions and electrical characteristics as M74HC73, differing only pin connections.



DUAL J-K FLIP-FLOP WITH RESET

FUNCTION TABLE (Note 1)

Control of the State of the state of the state of

	Inp	outs		Out	puts
R _D	CK	J	к	Q	Q
L	X	×	×	L	Н
Н	Į.	L	L	Q°	Q٥
Н	Ţ	L	н	L	Н
Н	1	н	L	Н	L
Н	↓ .	Н	Н	Tog	gle
н	L	х	×	Q°	Q°
Н	Н	x	×	Q°	Q٥
н	1	X	×	Qº	Q٥

Note 1:

: Change from low to high

↓ : Change from high to low

X : Irrelevant

Q° : Output state Q before clock input changed Q° : Output state Q before clock input changed Toggle : Inversion state before clock input changed

ABSOLUTE MAXIMUM RATINGS ($\tau_a = -40 \sim +85$ °C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
Vi	Input voltage		-0.5~V _{cc} +0.5	V
V _o	Output voltage		-0.5~V _{cc} +0.5	V
		V ₁ < 0V	-20	
lıĸ	Input protection diode current	V _I > V _{CC}	20	mA mA
		V ₀ < 0V	-20	
lok ·	Output parasitic diode current	Vo > Vcc	20	mA.
lo	Output current per output pin		±25	mA
Icc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65~+150	°C

Note 2 : M74HC107FP, T_a = $-40\sim+60^\circ$ C and T_a = $60\sim85^\circ$ C are derated at -6mW/°C. M74HC107DP, T_a = $-40\sim+50^\circ$ C and T_a = $50\sim85^\circ$ C are derated at -5mW/°C.

RECOMMENDED OPERATING CONDITIONS (Ta = -40~+85°C)

Cumbal	Do	rameter		Limits				
Symbol	Pa	rameter	Min	Тур	Max	Unit		
Vcc	Supply voltage	2		6	v			
Vı	Input voltage	0		V _{cc}	V			
Vo	Output voltage		. 0		Vcc	V		
Topr	Operating temperature ra	ange	40		+85	င		
,	20	$V_{CC} = 2.0V$	0		1000			
t _r , t _f	r, tf Input risetime, failtime	V _{CC} = 4.5V	0		500	ns		
		$V_{CC} = 6.0V$			400			

M74HC107P/FP/DP

DUAL J-K FLIP-FLOP WITH RESET

ELECTRICAL CHARACTERISTICS

							Limits			
Symbol	Parameter	Test	Test conditions $V_{CC}(V)$		25℃			-40~+85°C		Unit
					Min	Тур	Max	Min	Max	1
		$V_0 = 0.1V, V_{C}$	_0.1v	2.0	1.5			1.5		
ViH	High-level input voltage	$ I_0 = 20\mu A$	5—0.14	4.5	3.15	-		3.15		V
	·	1101 - 20μΑ		6.0	4.2			4.2		
		V- = 0 1V V-	$V_0 = 0.1V, V_{CC} = 0.1V$				0.5		0.5	
VIL	Low-level input voltage	$ I_0 = 20\mu A$	5 0.14	4.5			1.35		1.35	V
		$ 1_0 = 20\mu A$		6.0			1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
		İ	$I_{OH} = -20\mu A$	4. 5	4. 4			4. 4		
V _{OH}	High-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		٧
			$I_{OH} = -4.0 \text{mA}$	4. 5	4. 18			4.13		
14			$t_{OH} = -5.2 \text{mA}$	6.0	5. 68			5. 63		
			$I_{OL} = 20 \mu A$	2.0			. 0. 1		0.1	
			$I_{OL} = 20 \mu A$	4. 5			0.1		0.1	
VoL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
			I _{OL} = 4.0mA	4. 5			0. 26		0.33	
			I _{OL} = 5. 2mA	6.0			0.26		0.33	
l _{iH}	High-level input current	V₁ = 6V		6.0			0.1		1.0	μA
I _{IL}	Low-level input current	V ₁ == 0V		6.0			-0.1		-1.0	μΑ
Icc	Quiescent supply current	VI = VCC, GND	$I_0 = 0 \mu A$	6.0			2.0		20.0	μA

SWITCHING CHARACTERISTICS $(v_{cc} = 5V, T_a = 25\%)$

		Task and distance		Unit		
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
fmax	Maximum clock frequency		30			MHz
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time				10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = 15pF (Note 4)		-	21	ns
t _{PHL}	output propagation time ($\overline{CK} - Q, \ \overline{Q}$)				21	ns
t _{PLH}	Low-level to high-level and high-level to low-level				26	ns
t _{PHL}	output propagation time $(\overline{R}_D - Q, \overline{Q})$				26	ns

DUAL J-K FLIP-FLOP WITH RESET

SWITCHING CHARACTERISTICS ($v_{cc} = 2\sim 6V$, $T_a = -40\sim +85^{\circ}C$)

						Limits			
Symbol	Parameter	Test conditions			25℃		-40~	+85℃	Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0	5			4		
fmax	Maximum clock frequency		4.5	27			21		MHz
	,		6.0	31			24	ļ	
		·	2.0			75		.95	
tTLH	Low-level to high-level and		4.5			15	-	19	ns
	hish laws to law town	,	6.0			. 13		16.	
	high-level to low-level	-	2.0			75		95	
t _{THL}	output transition time		4.5			15	l	19	ns
			6.0			13	-	16	
			2.0	,		126		160	
tpLH	Low-level to high-level and	C _L = 50pF (Note 4)	4.5			25		32	ns
	high-level to low-level		6.0			21		27	
	output propagation time	5 p	2.0			126		160	
tehl	$(\overline{CK} - Q, \overline{Q})$		4.5			25	ì	32	ns
	4		6.0			21	ŧ	27	ļ.
		1	2.0			155		194	
t _{PLH}	Low-level to high-level and		4.5			31		39	ns
	high-level to low-level		6.0	Į	į.	26		32	ļ
	output propagation time		2.0	l		155		194	
t _{PHL}	$(\overline{R_D} - Q, \overline{Q})$		4.5	·		31	1	39	กร
			6.0	Į.		26		32	
C _I	Input capacitance					10		10	pF
C _{PD}	Power dissipation capacitance (Note 3)				. 55				pF

Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per flip flop)

The power dissipated during operation under no-load conditions is calculated using the following formula:

P_D = C_{PD} · V_{CC}² · f₁+I_{CC} · V_{CC}

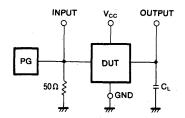
TIMING REQUIREMENTS ($V_{cc} = 2\sim 6V$, $T_a = -40\sim +85$ °C)

						Limits			
Symbol	Parameter	Test conditions			25℃		-40~	+85℃	Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	
	t _W		2.0	80			101		
tw			4.5	16	1		20		ns
			6.0	14	<u> </u>		17		
	I. K and up diene width		2.0	100			125		
tsu	J, K setup time with respect to CK		4.5	20			25		ns
	respect to CK	*	6.0	17		<u> </u>	21		
	1 K hald time with	•	2.0	0			0		
th	J, K hold time with respect to CK		4.5	0	1		0		ns
	respect to CK		6.0	0_	<u> </u>		0		
			2.0	100			125		
trec	rec respect to CK		4.5	20			25		ns
	Lesbect to CV		6.0	17			21		

DUAL J-K FLIP-FLOP WITH RESET

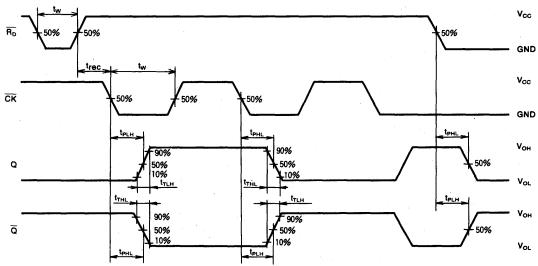
Note 4: Test Circuit

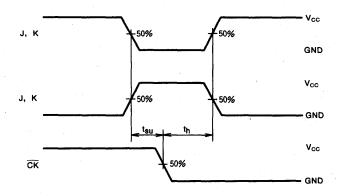
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- (1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
 (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





M74HC109P/FP/DP

DUAL J-K FLIP-FLOP WITH SET AND RESET

DESCRIPTION

The M74HC109 is a semiconductor integrated circuit consisting of two positive-edge triggered J- \overline{K} flip flops with independent control inputs.

FEATURES

- High-speed: 50MHz clock frequency typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 10µW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

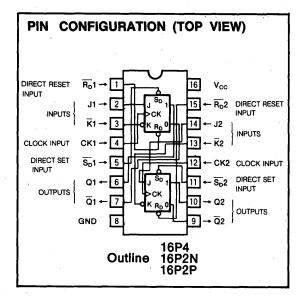
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC109 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS109.

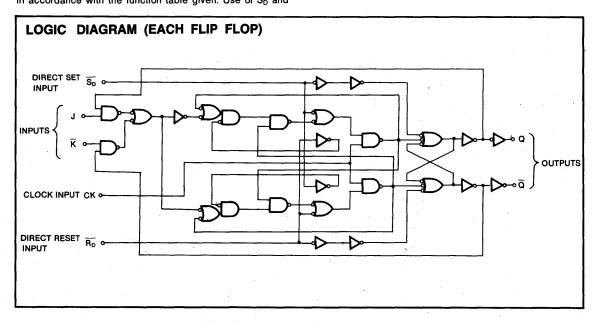
The M74HC109 contains two edge-triddered J- \overline{K} flip flops, each circuit with independent clock input CK, direct set input $\overline{S_D}$, direct reset input $\overline{R_D}$ and both inputs J and \overline{K} . When \overline{CK} is high, the J and K signals can be read.

When CK changes from low-level to high-level, the signals just previously input at J and \overline{K} appear at outputs Q and \overline{Q} in accordance with the function table given. Use of $\overline{S_D}$ and



 $\overline{R_D}$ permits direct R-S flip flop operation. When $\overline{S_D}$ and $\overline{R_D}$ are low, Q and \overline{Q} will both become high but when $\overline{S_D}$ and $\overline{R_D}$ simultaneously become high, the condition of Q and \overline{Q} cannot be predetermined. When used as a J- \overline{K} flip flop, $\overline{S_D}$ and $\overline{R_D}$ should be maintained at high-level.

Connecting J and \overline{K} will permit the M74HC109 to be used as a D-type flip flop.





DUAL J-K FLIP-FLOP WITH SET AND RESET

FUNCTION TABLE (Note 1)

		Inputs			Out	puts
SD	R₀	CK	J	ĸ	Q	Q
L	Н	Х	X	X	Н	L
Н	L	×	X	X	L	н
L	L	Х	Х	×	н*	Н*
н	Н	t	L	L	L	Н
н	Н	t	Н	L	·Tog	gle
Н	Н	1	L	Н	Q٥	Q°
Н	Н	1	Н	Н	Н	L
Н	н	L	x	X	Q°	Q٥

Note 1: † : Change from low to high

X : Irrelevant

 $\begin{array}{ll} \underline{Q}^0 & : \text{Output state } \underline{Q} \text{ before clock input changed} \\ \overline{Q}^0 & : \text{Output state } \overline{Q} \text{ before clock input changed} \\ \text{Toggle} : \text{Inversion state before clock input changed} \end{array}$

* : When $\overline{S_D}$ and $\overline{R_D}$ are low, Q and \overline{Q} become high, when $\overline{S_D}$ and $\overline{R_D}$ simultaneously

become high, the outputs of Q and Q cannot be predetermined.

ABSOLUTE MAXIMUM RATINGS $(T_a = -40 \sim +85 ^{\circ}C)$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Suppl voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
,		V ₁ < 0V	-20	
ItK	input protection diode current	$V_{\rm I} > V_{\rm CC}$	20	mA .
	0.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1	V ₀ < 0V	-20	
lok	Output parasitic diode current	t voltage $v_i < v_i < 0 V$ $v_i < 0 V$ $v_i > V_{CC}$ $v_i < 0 V$ $v_i > V_{CC}$ $v_i < 0 V$ $v_i > V_{CC}$ $v_i < 0 V$ $v_i > V_{CC}$ $v_i < 0 V$ $v_i > V_{CC}$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$ $v_i < 0 V$	20	mA mA
lo	Output current per output pin		±25	mA
Icc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65~+150	°C

Note 2 : M74HC109FP, T $_{\rm a}=-40\sim+70^{\circ}$ and T $_{\rm a}=70\sim85^{\circ}$ C are derated at -6mW/°C. M74HC109DP, T $_{\rm a}=-40\sim+50^{\circ}$ C and T $_{\rm a}=50\sim85^{\circ}$ C are derated at -5mW/°C.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85^{\circ}C)$

Common ad	Do	Parameter		Limits					
Symbol	Pai	rameter	Min	Тур	Max	Unit			
Vcc	Supply voltage		2		6	٧			
V _I	Input voltage		. 0		Vcc	٧			
V _o	Output voltage		0		Vcc	٧			
Topr	Operating temperature ra	inge	-40		+85	က			
,		$V_{CC} = 2.0V$	0		1000				
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns			
	input nooning, ramanie	$V_{CC} = 6.0V$. 0		400				

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DUAL J-K FLIP-FLOP WITH SET AND RESET

ELECTRICAL CHARACTERISTICS

CHOOKE, BOOK BERRY, JOHN

							Limits			
Symbol	Parameter	Test	conditions		25℃			-40~+85℃		Unit
			V _{cc} (V)		Min	Тур	Max	Min	Max	
		V =0.1V V	-0.11/	2. 0	1.5			1.5		
ViH	High-level Input voltage	$ I_0 = 20\mu A$	$V_0 = 0.1V$, $V_{CC} - 0.1V$		3.15		1	3.15	Ì	V
		$ 10 = 20\mu$ A		6.0	4.2		ļ	4.2		
		V =0.1V V	$V_0 = 0.1V, V_{CC} - 0.1V$				0.5		0.5	
VIL	Low-level input voltage		5-0.1 V	4.5			1.35		1.35	V
-		$ 10\rangle = 20\mu$ A	$ I_0 = 20\mu A$			٠.	1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
			$I_{OH} = -20\mu A$	4.5	4.4		ļ	4.4	ļ	
VoH	High-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9		l	5.9	ĺ	V
			$I_{OH} = -4.0 \text{mA}$	4.5	4. 18			4.13		
		ĺ	I _{OH} = -5. 2mA	6.0	5. 68		1	5.63		
			$I_{OL} = 20\mu A$	2.0			0.1		0.1	
			$I_{OL} = 20 \mu A$	4.5		Ì	0.1		0.1	
VoL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
			I _{OL} = 4.0mA	4.5			0.26		0.33	
			$I_{OL} = 5.2 \text{mA}$	6.0			0. 26		0.33	
I _{IH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μA
I _{IL}	Low-level input current	V ₁ = 0V	V ₁ = 0V				-0.1		-1.0	μA
Icc	Quiescent supply current	VI = VCC, GND	$I_0 = 0\mu A$	6.0			2.0		20.0	μА

SWITCHING CHARACTERISTICS ($V_{cc} = 5V$, $T_a = 25^{\circ}$)

Symbol	Parameter	Test conditions		Unit		
Symbol	Falallielei	Test conditions	Min	Тур	Max	Unit
fmax	Maximum clock frequency		30			MHz
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time				10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = 15pF (Note 4)			30	ns
t _{PHL}	output propagation time (CK — Q, Q)				30	ns
t _{PLH}	Low-level to high-level and high-level to low-level				40	ns
t _{PHL}	output propagation time $(\overline{S_D}, \overline{R_D} - Q, \overline{Q})$				40	ns

DUAL J-K FLIP-FLOP WITH SET AND RESET

SWITCHING CHARACTERISTICS $(v_{cc} = 2\sim6v, \tau_a = -40\sim+85^{\circ}C)$

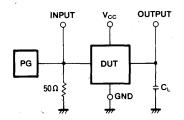
						Limits			
Symbol	Parameter	Test conditions			25°C		−40 ~	+85℃	Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0	5			4		
fmax	Maximum clock frequency		4.5	27			21		мна
			6.0	31		i	24		
		1	2.0			75		95	
t _{TLH}	Low-level to high-level and		4.5			15		19	ns
	Note to the last to the last		6.0		ĺ	13		16	
	high-level to low-level		2.0			75		95	
t _{THL}	output transition time	*	4.5		}	15		19	ns
			6.0			13		16	
			2.0			175		221	
t _{PLH}	Low-level to high-level and	C _L = 50pF (Note 4)	4.5			35		44	ns
	high-level to low-level		6.0	-		30	-	37	
	output propagation time	• '	2.0			175		221	
t _{PHL}	(CK - Q, Q)		4.5			35		44	ns
			6.0			30		37	
			2.0			230		290	
t _{PLH}	Low-level to high-level and		4.5			46		58	ns
	high-level to low-level		6.0			39		49	
	output propagation time		2.0			230		290	
t _{PHL}	$(\overline{S}_D, \overline{R}_D - Q, \overline{Q})$		4.5			46		58	ns
			6.0			39		49	
Cı	Input capacitance					10		10	рF
C _{PD}	Power dissipation capacitance (Note 3)				45				pF

Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per flip flop) The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS ($v_{cc} = 2\sim6v$, $T_a = -40\sim+85$ °C)

	[]					Limits			
Symbol	Parameter	Test conditions			25℃		-40~	+85℃	Unit
			V _{cc} (v)	Min	Тур	Max	Min	Max	
			2.0	80			101		
tw	CK, Sp, Rp pulse width		4.5	16			20		ns
			6.0	14		}	17	L	<u> </u>
	. =		2.0	100			126		
tsu	J, K setup time with		4.5	20		i	25		ns
	respect to CK		6.0	17			21		
	. =		2.0	5			5		
th	J, K hold time with		4.5	- 5			5	1	ns
,	respect to CK	•	6.0	5			5		
			2.0	5			5]
trec	R _D , S _D recovery time with	-	4.5	5			5	}	ns
	respect to CK		6.0	5			5		l

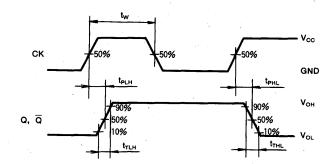
Note 4: Test Circuit

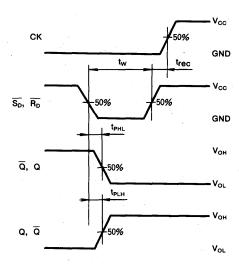


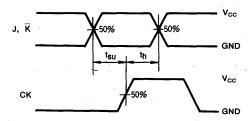
- (1) The pulse generator (PG) has the following characteristics (10% \sim 90%): $t_{\rm f}=6$ ns, $t_{\rm f}=6$ ns
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

DUAL J- $\overline{\mathbf{K}}$ FLIP-FLOP WITH SET AND RESET

TIMING DIAGRAM







MITSUBISHI HIGH SPEED CMOS

M74HC112P/FP/DP

DUAL J-K FLIP-FLOP WITH SET AND RESET

DESCRIPTION

The M74HC112 is a semiconductor integrated circuit consisting of two negative-edge triggered J-K flip flops with independent control inputs.

FEATURES

- High-speed: 50MHz clock frequency typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 10μW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: Ta=-40~+85℃

APPLICATION

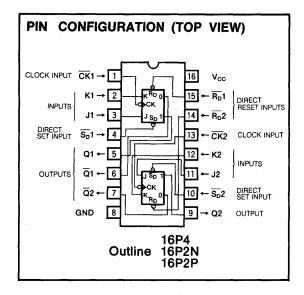
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC112 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS112.

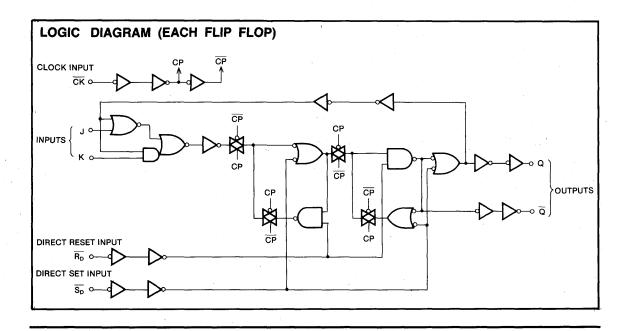
The M74HC112 contains two edge-triggered J-K flip flops, each circuit with independent clock input \overline{CK} , direct set input $\overline{S_D}$ and direct reset input $\overline{R_D}$, and both inputs J and K. When \overline{CK} is high, the J and K signals can be read.

When \overline{CK} changes from high-level to low-level, the signals just previously input at J and K appear at outputs Q and \overline{Q} in accordance with the function table given. Use of $\overline{S_D}$ and



 $\overline{R_D}$ permits airect R-S flip flop operation. When $\overline{S_D}$ and $\overline{R_D}$ are low, Q and \overline{Q} will both become high but when $\overline{S_D}$ and $\overline{R_D}$ simultaneously become high, the condition of Q and \overline{Q} cannot be predetermined. When used as a J-K flip flop, $\overline{S_D}$ and $\overline{R_D}$ should be maintained at high-level.

M74HC112 is the same functions and electrical characteristics as M74HC76, differing only pin connections.



DUAL J-K FLIP-FLOP WITH SET AND RESET

FUNCTION TABLE (Note 1)

		Inputs .			Out	puts
SD	R _D	CK	J	K	Q	Q
L	Н	. x	х	×	Н	L
н	L	Χ .	X	×	L	Н
L	L	×	×	×	н*	н*
н	н	1	L	L	Q°	Q°
н	Н	+	L	н	L.	Н
Н	Н	1	Н	. L	Н	L
н	Н	+	н	Н	To	ggle
н	Н	L	×	×	Q°	Q٥
н	Н	Н	×	×	Q°	Q°
Н	н.	t	×	×	Q°	Q°

Note 1:

: Change from low to high : Change from high to low

: Irrelevant

. Х О : Output state before clock input changed

: Output state before clock input changed

Toggle: Inversion state before clock input changed

: When $\overline{S_D}$ and $\overline{R_D}$ are low, Q and \overline{Q} both becomes high. When $\overline{S_D}$ and $\overline{R_D}$ becomes high, simultaneously, the condition of Q and Q cannot be predetermined.

ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85 \degree$ C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
Vi	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
		V₁ < 0V	-20	
Чк,	input protection diode current	V _I > V _{CC}	20	mA
		V ₀ < 0V	-20	
юк	Output parasitic diode current	Vo > Vcc	20	mA.
I _o	Output current per output pin		±25	mA
lcc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65~ +150	ာ

Note 2 : M74HC112FP, T $_a$ = $-40\sim+70^\circ$ C and T $_a$ = $70\sim85^\circ$ C are derated at -6mW/°C. M74HC112DP, T $_a$ = $-40\sim+50^\circ$ C and T $_a$ = $50\sim85^\circ$ C are derated at -5mW/°C.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85 ^{\circ}C)$

Symbol	Do.	ameter		Limits		Unit
Symbol	Pa	ameter	Min	Тур	Max	Unit
Vcc	Supply voltage		2		6	٧
V _i	Input voltage		0		Vcc	٧
Vo	Output voltage		0		Vcc	٧
Topr	Operating temperature re	inge	-40		+85	ဗ
		$V_{CC} = 2.0V$. 0		1000	
tr, tr	Input risetime, falltime	V _{CC} = 4.5V	0		500	ns
		$V_{CC} = 6.0V$.0		400	

M74HC112P/FP/DP

DUAL J-K FLIP-FLOP WITH SET AND RESET

ELECTRICAL CHARACTERISTICS

							Limits			
Symbol	Parameter	Test	conditions	• .		25℃	- "	-40~	+85°C	Unit
					Min	Тур	Max	Min	Max	
		$V_0 = 0.1V, V_{CC}$	_0.1v	2, 0	1.5			1.5		
VIH	High-level input voltage	$ I_{\rm O} = 20\mu{\rm A}$	50. TV	4.5	3.15			3.15		V
		1101 — 20μΑ	1101 20474		4. 2			4. 2		
	,	$V_{0} = 0.1V, V_{CC}$	_0.1v	2.0			0.5		0.5	
V_{IL}	Low-level input voltage		5—0.1 V	4.5			1. 35		1.35	V
		$ 10\rangle = 20\mu$ A	$ I_0 = 20\mu A$				1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
			$I_{OH} = -20\mu A$	4.5	4. 4		1	4.4		
V _{OH}	High-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OH} = -20 \mu A$	6.0	5.9			5.9		v
			$I_{OH} = -4.0 \text{mA}$	4.5	4. 18			4.13]
	*		I _{OH} == -5. 2mA	6.0	5. 68			5. 63		
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
	1.		$I_{OL} = 20 \mu A$	4.5			0.1		0.1	
Vol	Low-level output voltage	VI = VIH, VIL	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	v
			I _{OL} = 4.0mA	4.5			0. 26		. 0.33	1
	,		I _{OL} = 5. 2mA	6.0			0. 26		0.33	
l _{iH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μА
I _{IL}	Low-level input current	V ₁ = 0V		6.0			-0.1		-1.0	μA
Icc	Quiescent supply current	VI = VCC, GND	$I_0 = 0 \mu A$	6.0			2.0		20.0	μΑ

SWITCHING CHARACTERISTICS (V_{cc} = 5V, T_a = 25°C)

0	D	To all and distance		Limits		
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
fmax	Maximum clock frequency		30			MHz
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time				10	ns
t _{PLH}	Low-level to high-level and high-level to low-level				26	ns
teHL	output propagation time $(\overline{CK} - Q, \overline{Q})$	C _L = 15pF (Note 4)			26	ns
t _{PLH}	Low-level to high-level and high-level to low-level				31	ns
t _{PHL}	output propagation time $(\overline{R_D} - Q, \overline{Q})$				31	ns
t _{PLH}	Low-level to high-level and high-level to low-level	1			31	ns
t _{PHL}	output propagation time $(\overline{S}_D - Q, \overline{Q})$				31	ns

DUAL J-K FLIP-FLOP WITH SET AND RESET

SWITCHING CHARACTERISTICS ($V_{cc} = 2\sim6V$, $T_a = -40\sim+85^{\circ}C$)

						Limits]
Symbol	Parameter	Test conditions			25℃		-40~	+85°C	Unit
	1		V _{CC} (V).	Min	Тур	Max	Min	Max	
		1	2.0	5			4		
fmax	Maximum clock frequency	· .	4.5	27	l		21	ļ	мн
			6.0	31			24		
			2.0			75		95	
tTLH	Low-level to high-level and		4.5			15		19	ns
	high tours to the tours		6.0			13	·	16	
	high-level to low-level		2.0			75		95	
t _{THL}	output transition time	•	4.5		ľ	15		19	ns
			6.0			13		16	
			2.0			150		190	
t _{PLH}	Low-level to high-level and	,	4.5			30		38	ns
	high-level to low-level	1	6.0	-	1	26		33	İ
	output propagation time	,	2.0			150		190	
t _{PHL}	(CK - Q, Q)	C _L = 50pF (Note 4)	4.5			30	-	38	ns
			6.0			26	,	. 33	
			2.0			180		225	
t _{PLH}	Low-level to high-level and		4.5			36		45	ns
	high-level to low-level		6.0	<u> </u>		31		38	
	output propagation time		2.0			180		225	
t _{PHL}	$(\overline{R}_D - Q, \overline{Q})$		4.5			36		45	ns
·			6.0	ŀ	l	31		38	
			2.0			180		225	
t _{PLH}	Low-level to high-level and		4.5			36		45	ns
	high-level to low-level		6.0			31		38	
	output propagation time		2.0			180		225	
t _{PHL}	$(\overline{S_D} - Q, \overline{Q})$		4. 5			36	İ	45	ns
			6.0	Ì		31		38	
Cı	Input capacitance					10		10	pF
C _{PD}	Power dissipation capacitance (Note 3)				55				pF

Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per flip flop)
The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$

7 J - 7 J - 7 G - 4 7 G G - 7 G G

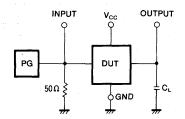
TIMING REQUIREMENTS ($v_{cc} = 2\sim 6V$, $T_a = -40\sim +85^{\circ}C$)

						Limits			ļ
Symbol	Parameter	Test conditions			25℃		-40~	+85℃	Unit
	\	`	V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0	80			101		
tw	CK, Sp, Rp pulse width		4.5	16			20		ns
			6.0	14			17		
			2.0	100			125		
tsu	J, K setup time with		4.5	20		Ì	25	-	ns
•	respect to CK		6.0	17	ł	ļ	21		
			2.0	0			0		
th	J, K hold time with		4.5	0	ļ)	0		ns
	respect to CK		6.0	0			0		·
			2.0	100			125		
trec	R _D , S _D recovery time with		4.5	20	1	Ì	25		ns
	respect to CK		6.0	17	Į		21		

DUAL J-K FLIP-FLOP WITH SET AND RESET

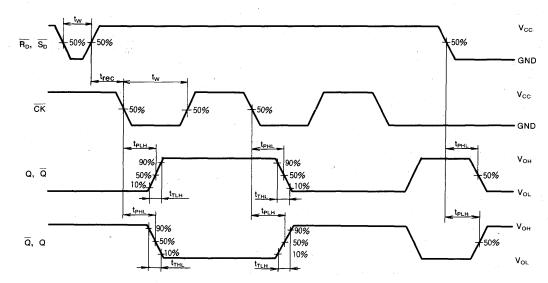
Note 4: Test Circuit

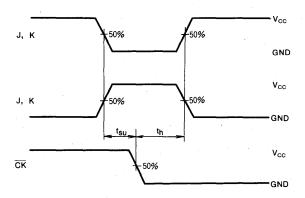
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- (1) The pulse generator (PG) has the following characteristics (10% \sim 90%): t_r = 6ns, t_f = 6ns (2) The capacitance C_L includes stray wiring
- capacitance and the probe input capacitance.

TIMING DIAGRAM





MITSUBISHI HIGH SPEED CMOS

M74HC113P/FP/DP

DUAL J-K FLIP-FLOP WITH SET

DESCRIPTION

The M74HC113 is a semiconductor integrated circuit consisting of two negative-edge triggered J-K flip flops with independent control inputs.

FEATURES

- High-speed: 50MHz clock frequency typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 10μW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2∼6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

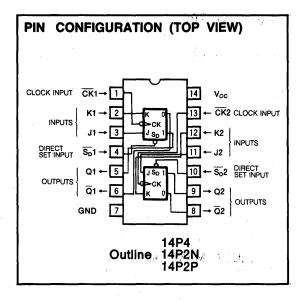
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC113 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS113.

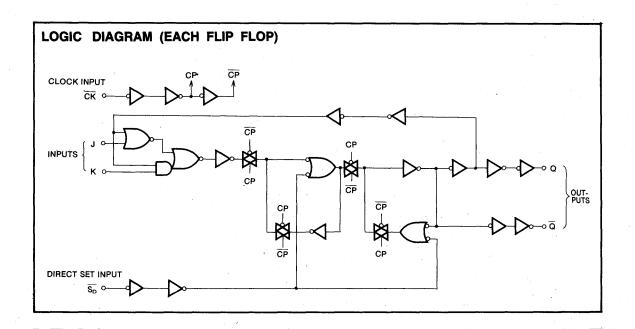
The M74HC113 contains two edge-triggered J-K flip flops, each circuit with independent clock input \overline{CK} , direct set input \overline{Sp} , and both inputs J and K.

When CK is high, the J and K signals can be read.

When $\overline{\text{CK}}$ changes from high-level to low-level, the signals



just previously input at J and K appear at outputs Q and \overline{Q} in accordance with the function table given. When $\overline{S_D}$ is low, Q and \overline{Q} will become high and low respectively, irrespective of other inputs. When used as a J-K flip flop, $\overline{S_D}$ should be maintained at high-level.



M74HC113P/FP/DP

DUAL J-K FLIP-FLOP WITH SET

FUNCTION TABLE (Note 1)

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	d Assessment &	-			
	Inp	uts		Ou	puts
S _D	CK	J	К	Q	Q
L	X	Х	x	Н	L
Н	1	L	L	Q°	Q°
Н	1	L	Н	L	Н
Н	Ţ	Н	L	н	L
. Н	1	н	Н	То	ggle
н	L	×	х	Q°	Q°
Н	н	×	X	Q°	Q°
. Н	1	X	х	Q°	Q°

Note 1 : †

: Change from low to high

↓ : Change from high to low

: Irrelevant

Q⁰ : Output state before clock input changed

Q° : Output state before clock input changed
Toggle: Inversion state before clock input changed

ABSOLUTE MAXIMUM RATINGS $(T_a = -40 \sim +85^{\circ}C)$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage		-0.5~+7.0	V
Vi	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
		V ₁ < 0V	-20	
l _{IK}	Input protection diode current	V _I > V _{CC}	20	mA
		V ₀ < 0V	-20	
Іок	Output parasitic diode current	V _o > V _{cc}	20	mA
lo	Output current per output pin		±25	mA
Icc	Supply/GND current	V _{CC} , GND	±50	mA .
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65~+150	°C

Note 2 : M74HC113FP, T $_a$ = $-40\sim$ +60°C and T $_a$ = 60~85°C are derated at -6mW/°C. M74HC113DP, T $_a$ = $-40\sim$ +50°C and T $_a$ = $50\sim$ 85°C are derated at -5mW/°C.

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85 \degree c)$

		rameter		Limits		Unit
Symbol	Pai	Min	Тур	Max	Unit	
Vcc	Supply voltage		2		6	٧
Vı	Input voltage		0		Vcc	>
Vo	Output voltage		0		Vcc	V
Topr	Operating temperature ra	ange	-40		+85	ာင
-		$V_{CC} = 2.0V$	0		1000	
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns
		$V_{CC} = 6.0V$	0		400	

M74HC113P/FP/DP

DUAL J-K FLIP-FLOP WITH SET

ELECTRICAL CHARACTERISTICS

The transport of the first series of the series of the series

							Limits			
Symbol	Parameter	Test	conditions		25℃			-40~+85°C		Unit
	-		V _{cc} (V)		Min	Тур	Max	Min	Max	
		V -01V V	0.11/	2.0	1.5			1.5		
VIH	High-level input voltage	V ₀ = 0.1V, V ₀		4.5	3. 15			3. 15		V
	•	$ I_0 = 20\mu A$		6.0	4.2			4. 2		
			0.114	2.0			0.5		0.5	
VIL	Low-level input voltage	$V_0 = 0.1V, V_{CC}$	5—0.1 V	4.5	,		1.35		1.35	v
		$ I_0 = 20\mu A$		6.0		ĺ	1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
			$I_{OH} = -20\mu A$	4.5	4. 4			4.4		
Voh	High-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9		}	5.9	}	v
			$I_{OH} = -4.0 mA$	4.5	4.18			4.13		
			$I_{OH} = -5.2 mA$	6.0	5. 68			5.63		
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
	·		$I_{OL} = 20 \mu A$	4.5	ŀ		0.1		0.1	
Vol	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0		\ .	0.1		0.1	V
			I _{OL} = 4.0mA	4.5			0.26		0.33	
	<u> </u>		I _{OL} = 5. 2mA	6.0			0.26		0.33	
I _{IH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μA
I _{IL}	Low-level input current	V ₁ = 0V		6.0			-0.1		-1.0	μA
Icc	Quiescent supply current	VI = VCC, GND	$h_0 = 0\mu A$	6.0			2.0		20.0	μA

SWITCHING CHARACTERISTICS (V_{cc} = 5V, T_a = 25°C)

0		TA		Limits			
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit	
fmax	Maximum clock frequency		30			MHz	
t _{TLH}	Low-level to high-level and high-level to low-level	1 .			10	ns	
t _{THL}	output transition time				10	ns	
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = 15pF (Note 4)			21	ns	
t _{PHL}	output propagation time ($\overline{CK} - Q, \ \overline{Q}$)				21	ns	
t _{PLH}	Low-level to high-level and high-level to low-level	•	7		26	ns	
t _{PHL}	output propagation time $(\overline{S_D} - Q, \overline{Q})$				26	ns	

DUAL J-K FLIP-FLOP WITH SET

SWITCHING CHARACTERISTICS ($V_{cc} = 2\sim 6V$, $T_a = -40\sim +85^{\circ}C$)

	,					Limits			
Symbol	Parameter	Test conditions			25℃		-40~	+85°C	Unit
		,	V _{cc} (V)	Min Typ Max		Max	Min Max		
			2.0	5			4		
fmax	Maximum clock frequency		4. 5	27			21	!	MHz
		·	6.0	- 31			24		
			2.0			75		. 95	
t _{TLH}	Low-level to high-level and		4.5		ļ	15		19	ns
	high-level to low-level		6.0			13		16	
	Ilign-level to low-level	·	2.0			75		95	
t _{THL}	output transition time	• •	4.5		,	15		19	ns
			6.0			13		16	
			2.0			126	1	160	
t _{PLH}	Low-level to high-level and	C _L = 50pF (Note 4)	4.5			25		32	ns
	high-level to low-level		6.0			21		27	
	output propagation time		2.0			126		160	
t _{PHL}	(CK - Q, Q)		4.5			25		32	ns
			6.0		1	21		27	j
,			2.0			165		210	
t _{PLH}	Low-level to high-level and		4.5			33		41	ns
_	high-level to low-level		6.0			28		- 35	
_	output propagation time		2.0			165		210	
t _{PHL}	$(\overline{S_D} - Q, \overline{Q})$		4.5			33		41	ns
			6.0			28		35	
Cı	Input capacitance					10		10	pF
C _{PD}	Power dissipation capacitance (Note 3)				52				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per flip flop)

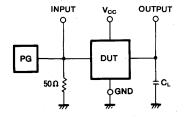
The power dissipated during operation under no-load conditions is calculated using the following formula:

P_D = C_{PD} • V_{CC}² • f₁+I_{CC} • V_{CC}

TIMING REQUIREMENTS $(V_{cc} = 2\sim 6V, T_a = -40\sim +85^{\circ})$

						Limits			
Symbol	Parameter	Test conditions		25℃		40~	+85℃	Unit	
			V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0	80			101		
tw	CK, Sp pulse width		4.5	16			20	-	ns
			6.0	14		İ	17	-	
			2.0	100			125		
tsu	J, K setup time with		4.5	20	1		25		ns
	respect to CK		6.0	17			21		
			2.0	0			0		
th	J, K hold time with		4.5	0			0		ns
	respect to CK	•	6.0	0			0		
			2. 0	100			125		
trec	S _D recovery time with		4.5	20			25		ns
	respect to CK		6.0	17			21		

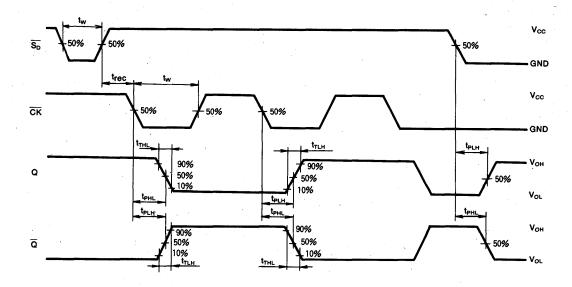
Note 4: Test Circuit

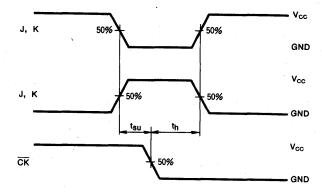


- (1) The pulse generator (PG) has the following
- characteristics (10%~90%): t₁ = 6ns, t₂ = 6ns (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

DUAL J-K FLIP-FLOP WITH SET

TIMING DIAGRAM





M74HC114P/FP/DP

DUAL J-K FLIP-FLOP WITH SET AND COMMON RESET

DESCRIPTION

The M74HC114 is a semiconductor integrated circuit consisting of two negative-edge triggered J-K flip flops with independent control inputs.

FEATURES

- High-speed: 50MHz clock frequency typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 10μW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85°C

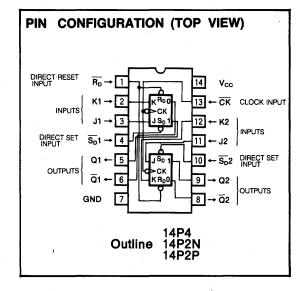
APPLICATION

General purpose, for use in industrial and consumer digital equipment.

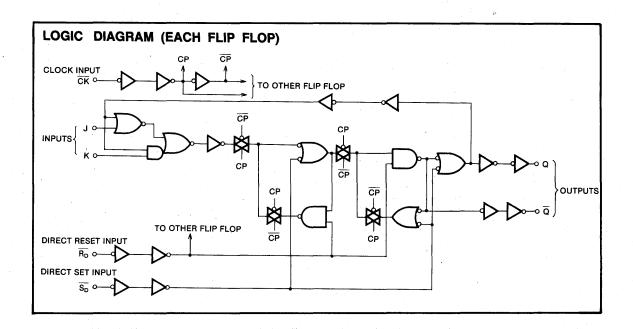
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC114 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS114.

The M74HC114 contains two edge-triggered J-K flip flops, each circuit with independent direct set input $\overline{S_D}$, inputs J and K, common clock input \overline{CK} , and direct reset input $\overline{R_D}$. When \overline{CK} is high, the J and K signals can be read. When \overline{CK} changes from high-level to low-level, the signals just



previously input at J and K appear at outputs Q and \overline{Q} in accordance with the function table given. Use of $\overline{S_D}$ and $\overline{R_D}$ permits direct R-S flip flop operation. When $\overline{S_D}$ and $\overline{R_D}$ are low, Q and \overline{Q} will both become high but when $\overline{S_D}$ and $\overline{R_D}$ simultaneously become high, the condition of Q and \overline{Q} cannot be predetermined. When used as a J-K flip flop, $\overline{S_D}$ and $\overline{R_D}$ should be maintained at high.



DUAL J-K FLIP-FLOP WITH SET AND COMMON RESET

FUNCTION TABLE (Note 1)

		Inputs			Out	puts
SD	R _D	ĊK	J	K	Q	Q
L	н	X	×	×	н	L
Н	L	X	×	×	L	Н
L	L	X	X	х	н*	,H*
н.	н	ţ	L	L	Q°	Q٥
Н	, н	†	Ĺ	Н	L	н
Н	Н	, †	н	L	Н	L
Н	Н	ţ	Н	Н	Тор	gle
Н	н	L	×	× .	Q°	Q٥
н	н	н	x	×	Q°	Q٥
Н	н	†	X	×	Q°	Q°

Note 1 : †

: Change from low to high

↓ :

: Change from high to low

X : Irrelevant

Q⁰ : Output state before clock input changed

Q⁰ : Output state before clock input changed Toggle : Inversion state before clock input changed

: When \overline{S}_D and \overline{R}_D are low, Q and \overline{Q} will both become high. When \overline{S}_D and \overline{R}_D become high simultaneously, the condition of Q and \overline{Q} cannot be predetermined.

ABSOLUTE MAXIMUM RATINGS $(\tau_a = -40 \sim +85 \degree\text{C}, \text{ unless otherwise noted})$

Symbol	Parameter	Conditions	Ratings	Unit
Voc	Supply voltage		-0.5~+7.0	V
V _I	Input voltage		-0.5~V _{cc} +0.5	V
V _o	Output voltage		-0.5~V _{cc} +0.5	V
	hand and all all all all and	V ₁ < 0V	-20	
lik .	Input protection diode current	V _I > V _{CC}	20	→ mA
		V ₀ < 0V	-20	
юк	Output parasitic diode current	Vo > Vcc	20	→ mA
lo	Output current per output pin		±25	mA
Icc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 2)	500	mW
Tsta	Storage temperature range		−65~+150	င

Note 2 : M74HC114FP, T $_a$ = $-40\sim+60^\circ$ C and T $_a$ = $60\sim85^\circ$ C are derated at -6mW/°C. M74HC114DP, T $_a$ = $-40\sim+50^\circ$ C and T $_a$ = $50\sim85^\circ$ C are derated at -5mW/°C.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85 \degree C)$

· O bl			Limits					
Symbol	Par	Min	Min Typ Max		Unit			
Vcc	Supply voltage		2		6	٧		
V _I	Input voltage		0		V _{cc}	٧		
V _o	Output voltage		. 0		Vcc	V		
Topr	Operating temperature ra	inge	-40		+85	°C		
		$V_{CC} = 2.0V$	0		1000			
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns		
		V _{CC} = 6.0V	0		400			

DUAL J-K FLIP-FLOP WITH SET AND COMMON RESET

ELECTRICAL CHARACTERISTICS

						,	Limits				
Symbol	Parameter	Test	Test conditions V _{CC} (V)		25℃		-40~+85°C		Unit		
		-			Min	Тур	Max	Min	Max	l	
		$V_0 = 0.1V, V_{CC} = 0.1V$		2.0	1.5			1.5			
VIH	High-level input voltage	$ I_0 = 20\mu A$	5—0. T V	4.5	3.15			3. 15		٧	
· ·		1101 — 20μΑ		6.0	4.2			4.2			
		$V_0 = 0.1V, V_{CC}$	-0 1V	2.0			0.5		0.5		
VIL	Low-level input voltage	1	5—0.1 V	4.5			1.35		1.35	V	
	$ I_0 = 20\mu A$			6.0			1.8		1.8		
			$I_{OH} = -20\mu A$	2.0	1.9			1.9			
			$I_{OH} = -20\mu A$	4.5	4. 4			4.4			
V_{OH}	High-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OH} = -20\mu A$	6.0	5. 9			5.9		V	
			$I_{OH} = -4.0 \text{mA}$	4.5	4.18			4.13			
			$I_{OH} = -5.2 \text{mA}$	6.0	5.68			5. 63			
			$I_{OL} = 20 \mu A$	2.0			0.1		0. 1		
			$I_{OL} = 20 \mu A$	4.5			0.1		0.1		
VoL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V	
			I _{OL} = 4.0mA	4.5			0. 26		0.33		
			I _{OL} = 5. 2mA	6.0			0.26		0.33		
l _{IH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μА	
I _{IL}	Low-level input current	$V_1 = 0V$		6.0			-0.1		-1.0	μA	
Icc	Quiescent supply current	Vi = Vcc, GND	$I_0 = 0 \mu A$	6.0			2.0		20.0	μA	

SWITCHING CHARACTERISTICS $(v_{cc} = 5V, T_a = 25\%)$

S	Parameter	Test conditions		Unit		
Symbol	Parameter	rest conditions	Min	Тур	Max	Unit
fmax	Maximum clock frequency		30			MHz
t _{TLH}	Low-level to high-level and high-level to low-level] '			10	ns
t _{THL}	output transition time	· ·			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level] .			26	ns
t _{PHL}	output propagation time ($\overline{CK} - Q, \overline{Q}$)	C _L = 15pF (Note 4)			26	ns
t _{PLH}	Low-level to high-level and high-level to low-level	,			31	ns
t _{PHL}	output propagation time $(\overline{R_D} - Q, \overline{Q})$				31	กร
t _{PLH}	Low-level to high-level and high-level to low-level				31	ns
t _{PHL}	output propagation time $(\overline{S_D} - Q, \overline{Q})$				31	ns

A SAME STAND COMMON RESET

SWITCHING CHARACTERISTICS ($v_{cc} = 2\sim6$ V, $T_a = -40\sim+85$ °C)

Quintann (1985) 4.70 (1985) 28 (28) **28 (28)** 28 (28)

-						Limits			
Symbol	Parameter	Test conditions			25℃		-40~	+85°C	Unit
			V _{cc} (v)	Min Typ		Max	Min	Max]
			2.0	5			.4		
fmax	Maximum clock frequency		4. 5	27			21	ĺ	MHz
			6.0	31			24		
	,		2.0			75		95	
t _{TLH}	Low-level to high-level and	·	4.5			- 15		19	ns
	Note to the tour tours.	·	6.0		-	13		16	
	high-level to low-level		2.0			75		95	
t _{THL}	output transition time		4.5			15		19	ns
			6.0			13		16	
			2.0			150		190	
t _{PLH}	Low-level to high-level and		4.5			30		38	ns
	high-level to low-level		6.0			26		33	
	output propagation time	The second secon	2.0			150		190	
t _{PHL}	$(\overline{CK} - Q, \overline{Q})$	C _L = 50pF (Note 4)	4.5			30		38	ns
			6.0			26		33	
		<u>'</u>	2.0			180		225	
t _{PLH}	Low-level to high-level and		4.5			36		45	ns
	high-level to low-level		6.0			31		38	
	output propagation time		2.0			180		225	
t _{PHL}	$(\overline{R_p} - Q, \overline{Q})$		4.5		,	36	1	45	ns
			6.0			31		38	
			2.0			180		225	
t _{PLH}	Low-level to high-level and		4.5	'		36		45	ns
	high-level to low-level		6.0	ĺ		31		38	
	output propagation time		2.0			180		225	
t _{PHL}	$(\overline{S_D} - Q, \overline{Q})$		4.5			36		45	ns
,			6.0			31		38	
Cı	Input capacitance		1.			10		10	pF
C _{PD}	Power dissipation capacitance (Note 3)				95	1			pF

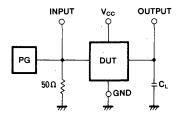
Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per flip flop)
The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS ($V_{cc} = 2\sim 6V$, $T_a = -40\sim +85^{\circ}C$)

						Limits			
Symbol	Parameter	Test conditions		25℃			−40~	+85℃	Unit
			V _{CC} (V)		Тур	Max	Min	Max	
			2.0	80			101		
tw	CK, S _D , R _D pulse width		4.5	16		ļ	20		ns
		4.5	6.0	14			17		
			2.0	100			125		
tsu	J, K setup time with		4.5	20	١.		25		ns
	respect to CK	e e e e e e e e e e e e e e e e e e e	6.0	17			21		
		7	2.0	0		,	0		
th	J, K hold time with		4.5	0			0 -		ns
''	respect to CK		6.0	о			0		
		<u> </u>	2.0	100			125		
trec	R _D , S _D recovery time with		4.5	20			25		ns
	respect to CK		6.0	17			21		

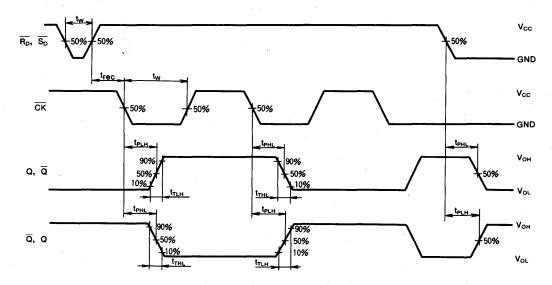
DUAL J-K FLIP-FLOP WITH SET AND COMMON RESET

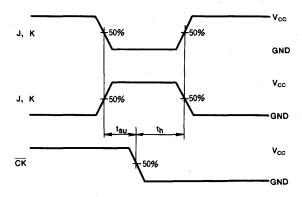
Note 4: Test Circuit



- (1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns (2) The capacitance C_L includes stray wiring
- capacitance and the probe input capacitance.

TIMING DIAGRAM





MITSUBISHI HIGH SPEED CMOS

M74HC123P/FP/DP

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

DESCRIPTION

The M74HC123 is a semiconductor integrated circuit consisting of two retriggerable monostable multivibrators with direct reset inputs.

FEATURES

- Retriggerable multivibrator can generate wide output pulses.
- Direct reset input can interrupt output pulses.
- High-speed: 28ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide supply voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85°C

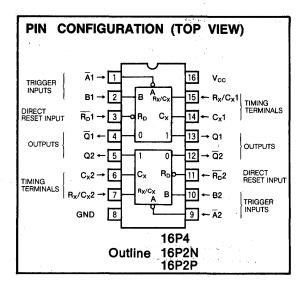
APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

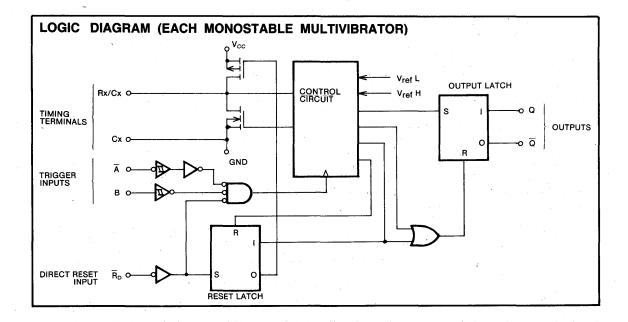
Use of silicon gate technology allows the M74HC123 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS123.

When external resistor R_X and electrostatic capacitor C_X are connected to timing terminals R_X/C_X and C_X as shown in Fig. 1, and trigger pulses are applied at inputs \overline{A} or B, positive pulses will appear at Q and negative pulses at \overline{Q} . (Fig. 2-(a))



The pulse width t_{WQ} is set by R_X and C_X . The trigger is applied when \overline{A} changes from high-level to low-level or when B changes from low-level to high-level. The retrigger function is used to obtain longer pulse width and output pulses can be extended by retriggering at \overline{A} or B before the output pulse is completed. (Fig. 2-(b))

When direct reset input \overline{R}_D is set low, Q will be reset low and \overline{Q} will be reset high, irrespective of the output state, allowing output pulses to be narrower by \overline{R}_D . (Fig. 2-(c)) When \overline{R}_D changes from low-level to high-level while A is low and B is high, the trigger is applied and Q and \overline{Q} change state.



DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

FUNCTION TABLE (Note 1)

	Inputs		Out	puts
R _D	Ā	В	Q	Q
L	×	Χ	L	Н
×	н	x	L	Н
×	×	L	L	Н
Н	L	1	Л	U
Н	1	н	Л	IJ
†	L	Н	П	U

- Note 1: † : Change from low to high level : Change from high to low level
 - : Positive one-shot operation
 - \coprod : Negative one-shot operation
 - X: Irrelevant

OPERATION

1. How to use the timing terminals

Resistor R_X and capacitor C_X are connected to timing terminals R_X/C_X and C_X , as shown in Fig. 1. If C_X is polar, the positive lead should be connected to the R_X/C_X side, and the negative lead to the Cx side. A diode is connected to prevent latchup.

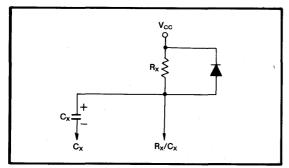


Fig.1 Connection of external resistor Rx and capacitor C_X to timing terminals R_X/C_X and C_X

2. Output Pulse Width two

The output pulse width t_{WQ} is determined as follows: When $C_X > 100000pF$, $R_X \ge 10k\Omega$ $t_{WQ}=0.46C_{x}\cdot R_{x}$ (ns) C_X is given in pF, and R_X in $k\Omega$

Output Pulse Width Control

The output pulse width can be controlled in the following three ways.

3-1 Normal Use

Fig. 2-(a) is the directions as ordinary monostable multivibrator operation and the output pulse width t_{WQ} can be set by using the formula and figure shown in section 2 above.

3-2 Extendtion of the output pulse width with retrigger function

As shown in Fig. 2-(b), the output pulse width can be extended at will by applying additional trigger pulses before the output is completed.

3-3 Shortening of the output pulse width with $\overline{R_D}$ signal As shown in Fig. 2-(c), the output pulse which has been generated by the trigger signal can be terminated with the $\overline{R_D}$ signal and it is possible to shorten its width as reguired.

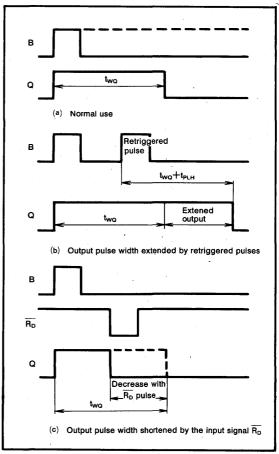


Fig.2 Output pulse width control

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

4. Precations for Use

- 4-1 Additional trigger pulses must be applied at least trr later after the previous trigger pulse has been applied. The retrigger pulse during this period is ineffective.
- 4-2 The lead length of external resistor $R_{\rm X}$ and capacitor $C_{\rm X}$ should be as short as possible (less than 3cm) to minimize stray wiring capacitance and to prevent misoperation due to noise. Care should also be taken to isolate this circuit from noise sources as far as possible.
- 4-3 Insert a capacitor of $0.01\sim0.1\mu F$ with good high-frequency characteristics between V_{GG} and GND.
- 4-4 Output pulses may be generated when the power is switched on.
- 4-5 Capacitor discharge when the power is turned off may cause thermal breakdown or latchup, so a diode should be connected as shown in Fig. 1.

ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85$ °C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	V
V _o	Output voltage		-0.5~V _{cc} +0.5	V
l _{ik}	Input protection diode current	V ₁ < 0V	-20	
		V _i > V _{cc}	20	mA.
lok	Output parasitic diode current	V ₀ < 0V	-20	
		Vo > Vcc	20	mA
l _o	Output current, per output pin		±25	mA
Icc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65~+150	ာ

Note 2 : M74HC123FP, T $_a$ = $-40\sim+70^\circ$ C and T $_a$ = $70\sim85^\circ$ C are derated at -6mW/°C. M74HC123DP, T $_a$ = $-40\sim+50^\circ$ C and T $_a$ = $50\sim85^\circ$ C are derated at -5mW/°C.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85 ^{\circ}C)$

Symbol	Parameter			Limits		
Symbol			Min	Тур	Max	Unit
Vcc	Supply voltage		2		6	V
V _I	Input voltage		0		Vcc	V
V _o	Output voltage		0		Vcc	V
Topr	Operating temperature range		40		+85	ဗ
	Input risetime, falltime (A, B)		n	no restriction		ns
	Input risetime, falltime ($\overline{R_D}$)	V _{CC} = 2.0V	0		1000	ns
t _r , t _f		$V_{CC} = 4.5V$	0		500	
		$V_{CC} = 6.0V$	0		400	
D	External timing resistance	V _{CC} =2.0V	5		1000	kΩ
Rx		V _{CC} ≥3.0V	1		1000	
C _x	External timing capacitance		n	no restriction		

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

ELECTRICAL CHARACTERISTICS

							Limits			
Symbol	Parameter	Test	conditions			25℃		-40~+85°C		Unit
				V _{cc} (V)	Min	Тур	Max	Min	Max	
,		$V_0 = 0.1V, V_{CO}$	0.154	2. 0	1.5			1.5		
V _{IH}	High-level input voltage	$ V_0 = 0.1V, V_{CO} $ $ I_0 = 20\mu A$;u. r v	4.5	3.15			3. 15		V
	·	11 ₀ = 20μΑ		6.0	4.2			4.2		
		$V_0 = 0.1V, V_{CC}$	0.114	2.0			0.5		0.5	
VIL	Low-level input voltage	$ V_0 = 0.1V, V_{CC} $;—0. 1 v	4.5			1.35		1.35	V
		$ 1_0 = 20\mu$ A	•	6.0			1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
	,		$I_{OH} = -20\mu A$	4.5	4. 4			4. 4		
V _{OH}	High-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		V
			$I_{OH} = -4.0 \text{mA}$	4.5	4.18			4. 13		
		1	$I_{OH} = -5.2 \text{mA}$	6.0	5.68			5. 63		
			$I_{OL} = 20 \mu A$	2.0			0. 1		0.1	
			$I_{OL} = 20 \mu A$	4.5	-		0.1		0.1	
VoL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
			I _{OL} = 4.0mA	4.5			0.26		0, 33	
	-		I _{OL} = 5. 2mA	6.0			0.26		0.33	
I _{IH}	High-level input current (A, B, RD)	V ₁ = 6V		6.0			0. 1		1.0	μA
I _{IL}	Low-level input current (A, B, RD)	$V_1 = 0V$		6.0			0.1		-1.0	μ A .
l _{iH}	High-level input current (R _X /C _X)	V ₁ = 6V		6.0			0.5		5.0	
I _{IL}	Low-level input current (R _X /C _X)	$V_i = 0V$		6.0			-0.5		-5.0	μА
Icc	Quiescent supply current	VI = VCC, GND	$I_0 = 0 \mu A$	6.0			4. 0		40.0	μA
			. ,	2.0			120		160	
·lcc	Active supply current	VI = VCC, GND,	$R_X/C_X = 0.5V_{CC}$	4.5			300		400	μA
							600		800	

SWITCHING CHARACTERISTICS ($V_{cc} = 5V$, $T_a = 25^{\circ}C$)

Symbol	Parameter	Test conditions		Unit		
Symbol	Parameter	lest conditions	Min	Тур	Max	Unit
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time				10	ns
t _{PLH}	Low-level to high-level and high-level to low-level				43	ns
t _{PHL}	output propagation time (A, B-Q, Q)	C ₁ = 15pF (Note 4)			43	ns
t _{PLH}	Low-level to high-level and high-level to low-level	CL—15PF (Note 4)			46	ns
t _{PHL}	output propagation time (Trigger input)(\$\overline{R}_D - Q\$, \$\overline{Q}\$)				46	ns
t _{PLH}	Low-level to high-level and high-level to low-level				35	ns
t _{PHL}	output propagation time (Reset input)($\overline{R_D}$ -Q, \overline{Q})				35	ns

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

SWITCHING CHARACTERISTICS ($V_{cc} = 2\sim6V$, $T_a = -40\sim+85^{\circ}C$)

Symbol	Parameter	Test conditions			25℃		-40~	+85°C	Uni
. Symbol	Falameter	rest conditions	V _{cc} (V)	Min	Тур	Max	Min	Max	0111
			2.0	Min	тур	75	MID	95	
	Law level to high level and		4.5			15		19	İ
t _{TLH}	Low-level to high-level and		6.0	ļ		13		16	ns
	high-level to low-level		2.0			75		95	
	output transition time		4.5			ns			
t _{THL}	output transition time	+	6.0			13		16	118
			2.0		-	240		300	
.	Low-level to high-level and	· 1	4.5	ļ		48		60	ns
t _{PLH}	high-level to low-level		6.0			41		51	118
	output propagation time		2.0			240		300	
	$(\overline{A}, B-Q, \overline{Q})$	the second second	4.5			48		60	ns
t _{PHL}	(A, B—Q, Q)		6.0			41	_	51	T IR
		C _L = 50pF (Note 4)	2.0			265		330	
	Low-fevel to high-level and		4.5			53		66	ns
t _{PLH}	high-level to low-level		6.0	İ		45		55	118
	output propagation time		2, 0			265		330	
	(Trigger input)		4.5			53		66	
t _{PHL} (R _D -	$(\overline{R_D} - Q, \overline{Q})$		6.0			45		55	n
		· · · · · · · · · · · · · · · · · · ·	2.0			195		245	-
	Low-level to high-level and		4.5			39		49	ns
t _{PLH}	high-level to low-level	,	6.0		-	33	1	49	118
	output propagation time		2.0		 	195		245	
	(Reset input)					39		49	
t _{PHL}	$(\overline{R_D}-Q,\overline{Q})$		4.5	1				49	ns
	Duta wight difference		6.0		-	33		42	
	Pulse width difference						:		%
Δt_{WQ}	between circuits in	*							70
*	the same package	C _x =0pF (Note 4)			 	1000		1050	
twa	Minimum output pulse	$R_X=5k\Omega$ (V _{CC} =2V)	2.0 4.5		1	1000	-	1250 250	
(MIN)	width	$R_{X}=3k\Omega (V_{CC}=2V)$ $R_{X}=1k\Omega (V_{CC}=4.5,6V)$	6.0			180		230	ns
		C _x =100pF	2, 0	47		67		67	-
		$R_X=10k\Omega$	4.5	47		57		57	
		C _L =50pF (Note 4)	6.0	47		57		57	μ
twa	Output pulse width	C _L =50pr (Note 4) C _X =0.1µF	2.0	0.42	-	0.54	0.42	0.50	
		$R_x=10k\Omega$	4.5	0.42		0.54	0.42	0.50	
		C _L =50pF (Note 4)	6.0	0.42		0.50	0.42	0.50	l m
Cı	Input consolitance	OL-Supr (Note 4)	6.0	0.42		10	0.42	10	-
	Input capacitance	<u> </u>		-	 	10	<u> </u>	10	pF pF
C _{PD}	Power dissipation capacitance (Note:	5)		1		<u> </u>	L		<u> </u>

Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot v_{CC}^2 \cdot f_i + I_{CC} \cdot v_{CC}$

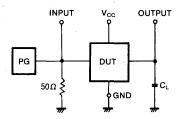
TIMING REQUIERMENTS ($v_{cc} = 2\sim 6v$, $T_a = -40\sim +85^{\circ}C$)

					Limits					
Symbol	Parameter	Test conditions	Test conditions		25℃			+85°C	Unit	
		V _{cc} (V)		Min	Тур	Max	Min	Max]	
			2.0		,	100		120		
tw ->	Minimum trigger pulse		4.5			20		24	ns	
(A, B)	(Ā, B) width		6.0			17		21		
			2.0			75		90		
t _w	Minimum direct reset		4.5	1		15		18	ns	
(R _D)	pulse width		6.0		1	13		16		
		C _X =100pF	4. 5							
	trr Minimum retrigger time	R _X =1kΩ	6.0						ns	
trr		C _X =0.1µF	4.5							
		R _X =1kΩ	6.0						ns	

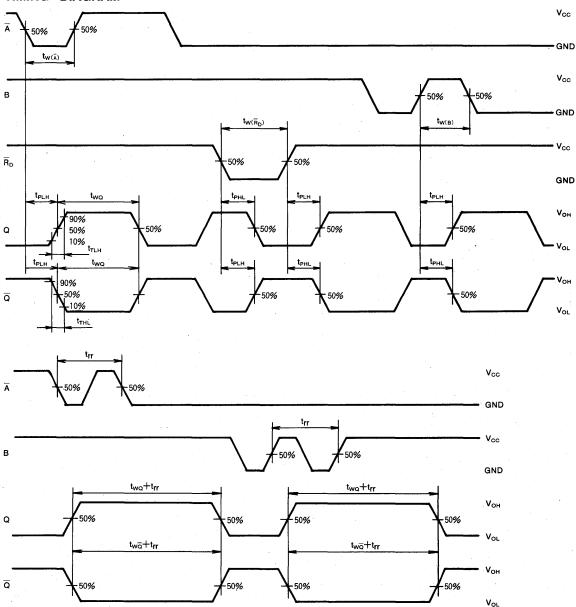


DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

Note 4: Test Circuit



- (1) The pulse generator (PG) has the following characteristics (10% \sim 90%): $t_f=6 n s, t_f=6 n s$
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.



M74HC125P/FP/DP

QUADRUPLE 3-STATE NONINVERTING BUFFER

DESCRIPTION

The M74HC125 is a semiconductor integrated circuit consisting of four buffers each with 3_7 state noninverted outputs and independent output-enable inputs.

FEATURES

- High-speed: 13ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2∼6V
- Wide operating temperature range: T_a=-40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC125 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS125.

When output-enable input \overline{OE} is low and input A is high then output Y will become high. However, if A is low then Y will become low. When \overline{OE} is high then Y will become high-impedance state, irrespective of A, making the device suitable for a bus line driver.

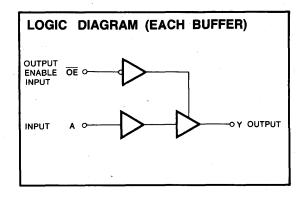
FUNCTION TABLE (Note 1)

Inp	Inputs		
ŌĒ	Α	Y	
L	L	L	
L	н	Н	
Н	×	Z	

Note 1: X: Irrelevant

Z : High impedance

PIN CONFIGURATION (TOP VIEW) OUTPUT ENABLE INPUT OE1 14 Vcc OE4 ENABLE INPUT 13 INPLIT OUTPUT Y1 12 INPUT OUTPUT OUTPUT NABLE INPUT OE2 11 OE3 OUTPUT 10 INPUT A2 OUTPUT INPLIT OUTPUT GND Outline



ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85$ °C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
V _I	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
	IK Input protection diode current	V ₁ < 0V	-20	
lικ		V _I > V _{CC}	20	mA
	0.4-4	V ₀ < 0V	-20	
lok	Output parasitic diode current	Vo > Vcc	20	, mA
l _o	Output current per output pin		±35	mA
lcc	Supply/GND current	V _{CC} , GND	±75	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		-65~+150	င

Note 2 : M74HC125FP, $T_a = -40 \sim +60 ^{\circ} C$ and $T_a = 60 \sim 85 ^{\circ} C$ are derated at -6mW/°C. M74HC125DP, $T_a = -40 \sim +50 ^{\circ} C$ and $T_a = 50 \sim 85 ^{\circ} C$ are derated at -5mW/°C.



RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85^{\circ}C)$

0	D-	Parameter		Limits				
Symbol	Parameter		Min	Тур	Max	Unit		
V _{CC}	Supply voltage		. 2		6	V		
Vı	Input voltage		0		Vcc	٧		
Vo	Output voltage		0		Vcc	٧		
Topr	Operating temperature ra	ange	40	_	+85	က		
		V _{CC} = 2.0V	0		1000			
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns		
		$V_{CC} = 6.0V$	0		400	ĺ		

ELECTRICAL CHARACTERISTICS

							Limits			
Symbol	Parameter	Test	conditions		25℃			-40~+85°C		Unit
		V _{cc} (V)		V _{cc} (V)	Min	Тур	Max	Min	Max	
		$V_0 = V_{cc} - 0.1$,	2.0	1.5			1.5		
VIH	High-level input voltage	$ V_0 = V_{CC} - 0.11$ $ I_0 = 20\mu A$		4.5	3.15			3.15		V
		1101 - 20µA	$_{\rm I} = 20 \mu A$		4.2		1	4.2		
		$V_{\rm O} = 0.1V, V_{\rm CO}$	-0.11/	2.0			0.5		0.5	
VIL	Low-level input voltage	$ V_0 - 0.1V, V_{CO} $ $ I_0 = 20\mu A$	5—0.1 V	4.5			1.35		1.35	V
	* * * * * * * * * * * * * * * * * * *	1161 - 20µA		6.0			1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
			$I_{OH} = -20\mu A$	4.5	4. 4			4.4	ì	
V_{OH}	High-level output voltage	$V_I = V_{IH}, \ V_{IL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		V
			$t_{OH} = -6.0 \text{mA}$	4.5	4. 18			4.13		
			$I_{OH} = -7.8 \text{mA}$	6.0	5. 68			5.63		
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
			$I_{OL} = 20 \mu A$	4.5			0.1		0.1	
Vol	Low-level output voltage	$V_i = V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
	•		$I_{OL} = 6.0 \text{mA}$	4.5			0.26		0.33	
			I _{OL} = 7.8mA	6.0			0.26		0.33	
l _{iH}	High-level input current	$V_i = 6V$		6.0			0.1		1.0	μA
l _{IL}	Low-level input current	$V_i = 0V$		6.0			-0. 1		-1.0	μA
lozh	Off-state high-level output current	$V_i = V_{iH}, \ V_{iL}, \ V_{iL}$	vo = vcc	6.0			0.5		5.0	μA
lozL	Off-state low-level output current	$V_i = V_{iH}, \ V_{iL}, \ V_O = GND$		6.0			-0. 5		-5. 0	μA
loc	Quiescent supply current	VI = VCC, GND	$I_0 = 0 \mu A$	6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (Voc = 5V, Ta = 25°C)

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Symbol	Parameter	Test conditions		Limits			
- Cyllibol	Parameter	rest conditions	Min	Тур	Max	Unit	
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns	
tTHL	output transition time	C _L = 50pF (Note 4)			10	ns	
t _{PLH}	Low-level to high-level and high-level to low-level	CL — SUPP (NOIG 4)			18	ns	
tpHL	output propagation time (A-Y)			1	18	ns	
t _{PLZ}	Output disable time from low-level and high-level	C _L = 5pF (Note 4)	* .		25	ns	
t _{PHZ}	(OE-Y)	CL — Spr (Note 4)			25	ns	
tpzL	Output enable time to low-level and high-level	C _L = 50pF (Note 4)			25	ns	
t _{PZH}	(OE-Y)	CL - SUPP (NOTE 4)			25	ns	

SWITCHING CHARACTERISTICS ($V_{cc} = 2\sim 6V$, $T_a = -40\sim +85$ °C)

Symbol	Parameter	Test conditions			25℃	Limits	40~	+85°C	Unit
Эупион	Parameter	1 est conditions	V (V)	A4:-		May			Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	
	1		2.0			60		75	
t _{TLH}	Low-level to high-level and		4.5			12		15	ns
	high-level to low-level	C _L = 50pF (Note 4).	6.0			10		13	
			2.0			60		75	
t _{THL}	output transition time		4.5			12		15	ns
	ļ	<u> </u>	6.0	·		10		13	
_			2.0			100		125	
t _{PLH}			4.5			20		25	ns
		C _L = 50pF (Note 4)	6.0			17		21	
			2.0			100		125	
t _{PHL}	Low-level to high-level and		4.5			20		25	ns
	high-level to low-level		6.0			17		21	
	output propagation time		2.0			. 130		163	İ
t _{PLH}	(A - Y)		4.5	ı		26		33	ns
		C _L = 150pF(Note 4)	6.0			22		28	
		CE = 13001 (14018 4)	2,0	1.00		. 130	* '*	163	
t _{PHL}			4.5			26		33	ns
	<u> </u>	I	6.0			. 22		28	l
			2. 0			125		156	
t _{PLZ}	Output disable time from		4.5			25		- 31	ns
	1	50 5 (11 11)	6.0			21		26	
,	low-level and high-level	C _L = 50pF (Note 4)	2.0			125		156	
t _{PHZ}	(OE - Y)	}	4.5			25		31	ns
			6.0			.21		26	
			2.0	-		125		156	
t _{PZL}			4.5			25		31	ns
			6.0			21		26	
		C _L = 50pF (Note 4)	2.0			125		156	
t _{PZH}	Output enable time to low-level		4.5			25		31	ns
			6.0			21		26	
	and high-level		2.0			140		175	T
tezL	(O Ē — Y)		4.5			28		35	ns
-, <u>Z</u> L			6.0	**		24		30	
	†	C _L = 150pF (Note 4)	2.0		<u> </u>	140		175	+
t _{PZH}		,	4.5			28		35 ns	
*F4M .			6.0	1		24		30	113
C,	Input capacitance	†·				10		10	pF
Co	Off-state output capacitance	$\overline{OE} = V_{CC}$			 	15		15	pF
C _{PD}	Power dissipation capacitance (Note 3)			 	42	+ 13		13	pF

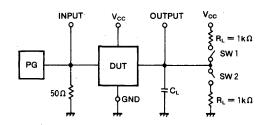
Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per buffer)

The power dissipated during operation under no-load conditions is calculated using the following formula:

P_D = C_{PD} · V_{CC}² · f₁+I_{CC} · V_{CC}

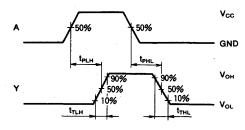


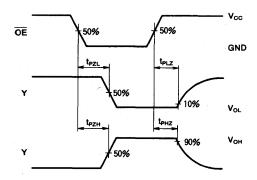
Note 4: Test Circuit



Parameter	SW 1	SW 2
t _{TLH} , t _{THL} t _{PLH} , t _{PHL}	Open	Open
t _{PLZ}	Closed	Open
t _{PHZ}	Open	Closed
t _{PZL}	Closed	Open
t _{PZH}	Open	Closed

(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.





MITSUBISHI HIGH SPEED CMOS

M74HC126P/FP/DP

QUADRUPLE 3-STATE NONINVERTING BUFFER

DESCRIPTION

The M74HC126 is a semiconductor integrated circuit consisting of four buffers each with 3-state noninverted outputs and independent output-enable inputs.

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FEATURES

- High-speed: 13ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{cc}=2~6V
- Wide operating temperature range: T_a=-40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC126 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS126.

When output-enable input OE is high and input A is high then output Y will become high. However, if A is low then Y will become low. When OE is low then Y will become high-impedance state, irrespective of A, making the device suitable for a bus line driver.

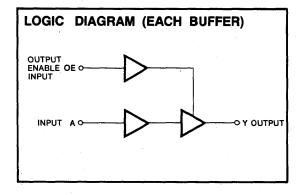
FUNCTION TABLE (Note 1)

Inp	Inputs		
OE	Α	Y	
Н	L	L	
н	н	Н	
L	X	Z	

Note 1: X:Irrelevant

Z : High impedance

PIN CONFIGURATION (TOP VIEW) OUTPUT OE1 Vcc OE4 OUTPUT INPUT A1 OUTPUT ENABL INPUT OE2 OUTPUT OE3 OUTPUT ENABLE INPUT INPUT A2 A3 INPUT OUTPUT Y2 GND Y3 OUTPUT Outline 14P2N



ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85 ^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	ν
Vo	Output voltage		-0.5~V _{cc} +0.5	V
	land and add a summer	V ₁ < 0V	-20	
İIK	Input protection diode current	$V_1 > V_{CC}$	20	, mA
1	Outros de constituir di ada constituir de co	V ₀ < 0V	-20	
Іок	Output parasitic diode current	Vo > Vcc	20	mA
lo	Output current per output pin		±35	` mA
Icc	Supply/GND current	V _{CC} , GND	土75	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65~+150	ဗ

Note 2 : M74HC126FP, T $_a$ = $-40\sim+60^\circ$ C and T $_a$ = $60\sim85^\circ$ C are derated at -6mW/°C. M74HC126DP, T $_a$ = $-40\sim+50^\circ$ C and T $_a$ = $50\sim85^\circ$ C are derated at -5mW/°C.



RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85^{\circ}C)$

Symbol	Parameter			Limits				
Зуппон	Pa	rameter	Min	Тур	Max	Unit		
Vcc	Supply voltage		2		6	. V		
V ₁	Input voltage		0		Vcc	V		
Vo	Output voltage		0		Vcc	٧		
Topr	Operating temperature ra	inge	-40		+85	°C		
	Input risetime, falltime	$V_{CC} = 2.0V$	0		1000			
t _r , t _f		$V_{CC} = 4.5V$	0		500	ns		
	V _{CC} = 6.0V		0		400	-		

ELECTRICAL CHARACTERISTICS

							Limits			
Symbol	Parameter	Test	Test conditions		25℃			-40~	+85°C	Unit
	·	V _{cc} (V)		Min	Тур	Max	Min	Max		
		$V_{\rm O} = 0.1 V, V_{\rm C}$	_0.1v	2.0	1.5			1.5		
V_{IH}	High-level input voltage	$ V_0 = 0.1V, V_{CO}$ $ I_0 = 20\mu A$	50. T V	4.5	3.15			3.15		v
		$ 1_0 = 20\mu\text{A}$	• .	6.0	4.2	i		4. 2.		
		$V_0 = 0.1V$		2.0			0.5		0.5	
VIL	Low-level input voltage	$ V_0 = 0.1 \text{ V}$ $ V_0 = 20 \mu \text{A}$		4.5			1.35		1.35	v
		$ 10\rangle = 20\mu$ A		6.0			1.8		1.8	
		,	$I_{OH} = -20\mu A$	2.0	1.9			1.9		
			$I_{OH} = -20\mu A$	4.5	4.4			4. 4		
V _{OH}	High-level output voltage	$V_i = V_{iH}$	$I_{OH} = -20\mu A$	6.0	5.9		J	5.9	j	V
			$I_{OH} = -6.0 \text{mA}$	4. 5	4. 18	_		4.13		
			$I_{OH} = -7.8 \text{mA}$	6.0	5. 68			5.63		
			$I_{OL} = 20 \mu A$	2.0			0. 1		0.1	
	*		$I_{OL} = 20 \mu A$	4. 5			0. 1		0.1	
VoL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
			I _{OL} = 6.0mA	4.5			0.26		0.33	
		:	$I_{OL} = 7.8 \text{mA}$	6.0			0.26		0.33	
l _{IH}	High-level input current	$V_i = 6V$		6.0			0. 1		1.0	μA
l _{IL}	Low-level input current	$V_i = 0V$		6.0			-0.1		-1.0	μA
lozh	Off-state high-level output current	$V_i = V_{iH}, \ V_{iL}, \ V_{iL}$	$V_{O} = V_{CC}$	6.0			0.5		5.0	μА
lozL	Off-state low-level output current	$V_i = V_{iH}, \ V_{iL}, \ V_{iL}$	Vo = GND	6.0			-0.5		-5.0	μA
loc	Quiescent supply current	Vi = Vcc, GND	$I_0 = 0 \mu A$	6.0			4.0		40.0	μА

SWITCHING CHARACTERISTICS ($v_{cc} = 5v$, $\tau_a = 25\%$)

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Symbol	Parameter	Test conditions		Limits			
Syllibol		rest conditions	Min	Тур	Max	Unit	
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns	
t _{THL}	output transition time	C _L = 50pF (Note 4)			10	. ns	
t _{PLH}	Low-level to high-level and high-level to low-level				18	ns	
t _{PHL}	output propagation time (A-Y)				18	ns	
t _{PLZ}	Output disable time from low-level and high-level	C _L = 5pF (Note 4)			25	ns	
t _{PHZ}	(OE-Y)	CL — Spr (Note 4)			25	ns	
t _{PZL}	Output enable time to low-level and high-level	C _L = 50pF (Note 4)			25	ns	
t _{PZH}	(OE-Y)	C _L = 50pr (Note 4)			- 25	ns	

SWITCHING CHARACTERISTICS $(V_{cc} = 2\sim 6V, T_a = -40\sim +85^{\circ}C)$

						Limits			
Symbol	Parameter	Test conditions			25℃		40~	+85℃	Unit
			V _{cc} (V)	. Min	Тур	Max	Min	Max	
			2.0			60		75	
t _{TLH}	Low-level to high-level and		4.5		`	12		15	ns
	high-level to low-level	C _L = 50pF (Note 4)	6.0	į		10		13	
	riign-level to low-level	CL = SOPF (Note 4)	2.0			60		75	
t _{THL}	output transition time		4.5			12		15	ns
			6.0			10		13	
			2.0			100		125	
t _{PLH}			4.5			20		25	ns
		C _L = 50pF (Note 4)	6.0			17		21	
	1	C _L = 50pr (Note 4)	2.0		1	100		125	
t _{PHL}	Low-level to high-level and	ĺ	4.5	1	1	20	1	25	ns
	high-level to low-level		6.0		1	17		21	
	output propagation time		2.0			130		163	
t _{PLH}	(A—Y)	1	4.5			26	1	33	ns
		150 = (1) (1)	6.0	ļ	ļ	22	İ	28	ļ
	· ·	C _L = 150pF (Note 4)	2.0			130		163	
t _{PHL}		4.5			26		33	ns	
			6.0			22		28	
			2.0			125		156	
tpLZ	Output disable time from	m	4.5		1	25	1	31	ns
	ľ		6.0			21		26	
,	low-level and high-level	C _L = 50pF (Note 4)	2.0		1	125		156	
t _{PHZ}	(OE-Y)		4.5	1		25		31	ns
			6.0			21		26	
			2.0	1		125		156	
t _{PZL}	1		4.5			25		31	ns ·
			6.0			21		26	
****		C _L = 50pF (Note 4)	2, 0			125		156	-
t _{PZH}	Output enable time to low-level		4.5			25		31	ns
	l		6.0	ľ		21		26	
	and high-level		2.0	T		140		175	
t _{PZL}	(OE-Y)		4.5			28		35	ns
· 			6.0			24		30	
	1	C _L = 150pF (Note 4)	2.0			140		175	
t _{PZH}			4.5			28		35	ns
			6.0			24		30	
Cı	Input capacitance					10		10	ρF
Co	Off-state output capacitance	OE = GND			1	15		15	ρF
C _{PD}	Power dissipation capacitance (Note 3)			<u> </u>	43	1	1	1	pF

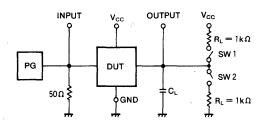
Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per buffer)

The power dissipation during operation under no-load conditions is calculated using the following formula:

P_D = C_{PD} · V_{CC}² · f₁+I_{CC} · V_{CC}

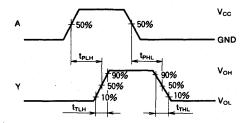


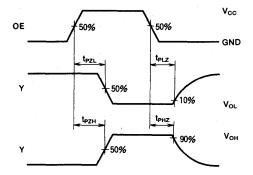
Note 4: Test Circuit



Parameter	SW 1	SW 2
t _{TLH} , t _{THL}	Open	Open
t _{PLZ}	Closed	Open
t _{PHZ}	Open	Closed
t _{PZL}	Closed	Open
t _{PZH}	Open	Closed

- (1) The pulse generator (PG) has the following
- characteristics (10%~90%): t_f = 6ns, t_f = 6ns (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.





M74HC132P/FP/DP

QUADRUPLE 2-INPUT SCHMITT-TRIGGER POSITIVE NAND GATE

DESCRIPTION

The M74HC132 is a semiconductor integrated circuit consisting of four 2-input Schmitt-trigger positive-logic NAND gates, usable as negative-logic NOR gates.

FEATURES

- High-speed: 13ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range : V_{CC} =2∼6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC132 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS132.

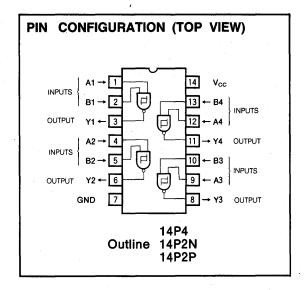
Built-in Schmitt-trigger circuits prevent the occurrence of incorrect oscillations even when input signals having slow rise and fall times are applied. The Schmitt triggers ensure a signal of restored waveshape will appear at the output.

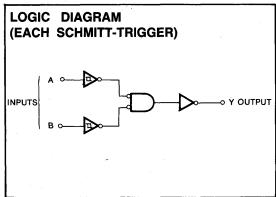
When both A and B inputs are high the output Y will be-

When both A and B inputs are high, the output Y will become low, and when at least one of the inputs is low, the output Y will become high.

FUNCTION TABLE

Inp	Inputs		
Α	В	Υ	
Ł	L	Н	
Н	L	Н	
L	Н	н	
Н	Н	L	





ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85 ^{\circ}$ C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
V _I	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
	Innut and other died and	V ₁ < 0V	-20	
lık	Input protection diode current	$v_i > v_{cc}$	20	mA
		V ₀ < 0V	-20	^
lok	Output parasitic diode current	Vo > Vcc	20	mA
lo	Output current per output pin		±25	mA
Icc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		-65~+150	ో

Note 1 : M74HC132FP, T $_a=-40\sim+65^\circ$ C and T $_a=65\sim85^\circ$ C are derated at -6mW/°C. M74HC132DP, T $_a=-40\sim+50^\circ$ C and T $_a=50\sim85^\circ$ C are derated at -5mW/°C.



QUADRUPLE 2-INPUT SCHMITT-TRIGGER POSITIVE NAND GATE

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85 \degree C)$

0	B		Unit		
Symbol	Parameter	Min	Тур	Max	Unit
V _{CC}	Supply voltage	2		6	V
V _i	Input voltage	0		Vcc	V
Vo	Output voltage	0		Vcc	V
Topr	Operating temperature range	-40		+85	္ဇင
. t _r , t _f	Input risetime, falltime	No restriction			_

ELECTRICAL CHARACTERISTICS

							Limits			
Symbol	Parameter	Test	Test conditions $\boxed{ V_{CC}(V) }$			25℃		-40~+85°C		Unit
					Min	Тур	Max	Min	Max	
	Positive-going	V = 0.1V V	$V_0 = 0.1V, V_{CC} - 0.1V$		0.7		1.5	0.7	1.5	
V _{T+}		1 -	- 0.10	4.5	1.55		3. 15	1.55	3.15	V
· ·	threshold voltage	1101 — 20µA	$ I_0 = 20\mu A$		2.1		4. 2	2.1	4.2	
	Negative-going $V_0 = V_{CC} - 0.1V$		v	2.0	0.3		1.0	0.3	1.0	
V _T		$ V_0 = V_{CC} - 0.1$ $ I_0 = 20\mu A$	v	4.5	0.9		2. 45	0.9	2. 45	V
	threshold voltage	$ I_0 = 20\mu\text{A}$		6.0	1.2		3.2	1.2	3. 2	
		V = 0.1V V	0.11/	2.0	0.2		1.2	0.2	1.2	
V _H	Hysteresis voltage	$V_0 = 0.1V, V_{CC} - 0.1V$ $ I_0 = 20\mu A$		4.5	0.4		2.1	0.4	2. 1	V
		1101 = 20µA	1101 - 20#A		0.5		2.5	0.5	2.5	
	High-level output voltage V		$I_{OH} = -20\mu A$	2.0	1.9			1.9		
		$V_1 = V_{T+}, V_{T-}$	$I_{OH} = -20\mu A$	4.5	4. 4			4. 4		
VoH			$I_{OH} = -20\mu A$	6.0	5.9	l		5.9		· v
			$I_{OH} = -4.0 \text{mA}$	4.5	4. 18			4. 13		
			$I_{QH} = -5.2 \text{mA}$	6.0	5. 68			5. 63		
			$I_{OL} = 20 \mu A$	2.0	-		0.1		0.1	
			$I_{OL} = 20 \mu A$	4.5			0.1		0.1	
VoL	Low-level output voltage	$V_1 = V_{T+}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	· v
			I _{OL} = 4.0mA	4.5			0. 26		0.33	
			$I_{OL} = 5.2 \text{mA}$	6.0			0.26		0.33	
I _{IH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μA
I _{IL}	Low-level input current	$V_1 = 0V$		6.0			-0.1		-1.0	μA
Icc	Quiecent supply current	VI = VCC, GND	$I_0 = 0 \mu A$	6.0			1.0		10.0	μA

QUADRUPLE 2-INPUT SCHMITT-TRIGGER POSITIVE NAND GATE

SWITCHING CHARACTERISTICS (Voc = 5V, Ta = 25°C)

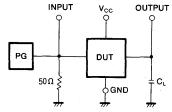
Sumbol	Parameter	Tret conditions	Limits			Unit
Symbol		Test conditions	Min	Тур	Max	Unit
t _{TLH}	Low-level to high-level and high-level to low-level				10	<u> </u>
t _{THL}	output transition time	C ₁ = 15pF (Note 3)			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	CL = 15pF (Note 5)			22	
t _{PHL}	output propagation time				22	ns

SWITCHING CHARACTERISTICS $(V_{cc} = 5V \pm 10\%, T_a = -40 \sim +85\%)$

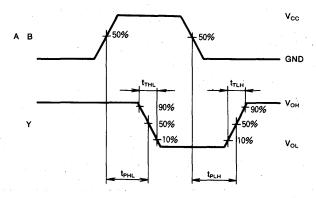
						Limits			T
Symbol	Parameter Test conditions			25℃			-40~+85°C		Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	_
			2.0			75		95	
t _{TLH}	Low-level to high-level and		4.5			15		19	ns
	Rich Issuel As Issuel		6.0			13		16	
	high-level to low-level		2. 0			75		95	
t _{THL}	output transition time		4.5			15		19	ns
		(i)	6.0			13		16	
		$C_L = 50 pF \text{ (Note 3)}$	2.0			125		158	
t _{PLH}	Low-level to high-level and		4.5			25		32	ns
	l		6.0			21		27	
	high-level to low-level		2.0			125		158	
t _{PHL}	output propagation time		4.5			25		32	ns
		-	6.0			21		27	
Cı	Input capacitance					10		10	pF
CPD	Power dissipation capacitance (Note 2)				37				pF.

Note 2 : CPD is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per gate) The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC} \cdot f_1 + I_{CC} \cdot V_{CC}$

Note 3: Test Circuit



- (1) The pulse generator (PG) has the following
- characteristics $(10\% \sim 90\%)$: $t_r = 6ns$, $t_f = 6ns$ (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.



MITSUBISHI HIGH SPEED CMOS

M74HC133P/FP/DP

13-INPUT POSITIVE NAND GATE

DESCRIPTION

The M74HC133 is a semiconductor integrated circuit consisting of a 13-input positive-logic NAND gates, usable as negative-logic NOR gates.

FEATURES

- High-speed: 20ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2∼6V
- Wide operating temperature range: Ta=−40~+85°C

APPLICATION

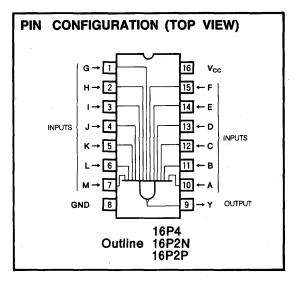
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC133 to maintain the low power dissipation and high noise margin of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS133.

Buffered output Y improve input-to-output transfer characteristics and reduce to a minimum output impedance variations with respect to input voltage variations.

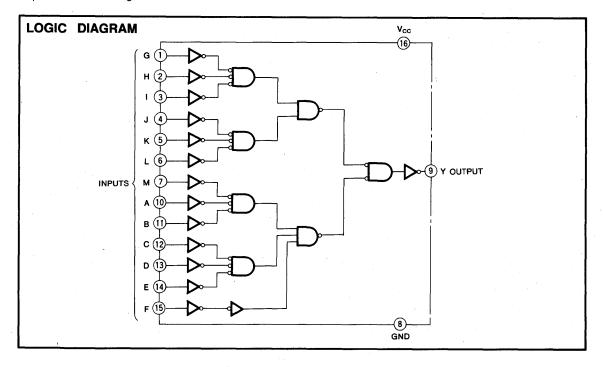
When inputs A through M are all high, the output Y will become low and when at least one of A through M is low, the output Y will become high.



FUNCTION TABLE

Inp	uts	Output
A	N	Y
· L	L	Н
Н	L	Н
L	н	Н
Н	Н	L

 $N = B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H \cdot I \cdot J \cdot K \cdot L \cdot M$





13-INPUT POSITIVE NAND GATE

ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85 ^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	V-
Vo	Output voltage		-0.5~V _{cc} +0.5	V
		V ₁ < 0V	-20	
· lik	Input protection diode current	$V_1 > V_{CC}$	20	mA .
		V ₀ < 0V	-20	
юк	Output parasitic diode current	Vo > Vcc	20	mA
lo	Output current per output pin		±25	mA
loc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		-65~,+ 150	ာ

Note 1 : M74HC133FP, $T_a = -40 \sim +70 ^{\circ}$ and $T_a = 70 \sim 85 ^{\circ}$ are derated at -6mW/°C. M74HC133DP, $T_a = -40 \sim +50 ^{\circ}$ and $T_a = 50 \sim 85 ^{\circ}$ are derated at -5mW/°C.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85 °C)$

Cumbal	Do	rameter		Limits					
Symbol	Pa	Min	Тур	Max	Unit				
Vcc	Supply voltage		2		6	ν			
Vı	Input voltage		0		Vcc	٧			
Vo	Output voltage		. 0		Vcc	٧			
Topr	Operating temperature ra	ange	-40		+85	°C			
		$V_{CC} = 2.0V$	0		1000				
tr, tf	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns			
		$V_{CC} = 6.0V$	0		400				

ELECTRICAL CHARACTERISTICS

							Limits			
Symbol	Parameter	Test	conditions			25℃		-40~	+85℃	Unit
			-		Min	Тур	Max	Min	Max	
		$V_0 = 0.1V, V_{CC}$	_0.1v	2.0	1.5			1.5		
VIH	High-level input voltage	$ V_0 = 0.1V, V_{CC}$ $ I_0 = 20\mu A$	—0.1 V	4.5	3.15		1	3.15		٧
		101 - 20µA		6.0	4.2			4.2		
		V - V 0 1V		2.0			0.5		0.5	
V _{1L}	Low-level input voltage	$V_0 = V_{CC} - 0.1V$ $ I_0 = 20\mu A$		4.5			1.35		1.35	· v
		$ 1_0 = 20\mu$ A		6.0			1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
			$I_{OH} = -20\mu A$	4.5	4.4			4.4		
VoH	High-level output voltage	$V_{l} = V_{lH}, V_{lL}$	$I_{OH} = -20 \mu A$	6.0	5.9			5.9		v
			$I_{OH} = -4.0 \text{mA}$	4.5	4.18			4.13		
			$I_{OH} = -5.2 \text{mA}$	6.0	5. 68			5. 63		
			$I_{OL} = 20 \mu A$	2.0		1, 1	0.1		0.1	
			$I_{OL} = 20 \mu A$	4.5			0.1	{	0.1	
VoL	Low-level output voltage	$V_i = V_{iH}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	v
			I _{OL} = 4.0mA	4.5			0.26		0.33	
			$I_{OL} = 5.2 \text{mA}$	6.0			0.26		0.33	
l _{iH}	High-level input current	V ₁ = 6V		6.0			0. 1		1.0	μА
l _{IL}	Low-level input current	V ₁ = 0V		6.0			0.1		-1.0	μA
Icc	Quiescent supply current	VI = VCC, GND	$I_0 = 0\mu A$	6.0			1.0		10.0	μΑ

13-INPUT POSITIVE NAND GATE

SWITCHING CHARACTERISTICS (V_{cc} = 5V, T_a = 25°C)

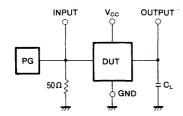
Symbol	Parameter	Test conditions			Unit	
Symbol	Parameter	l'est conditions	Min	Тур	Max	Unit
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time	C ₁ = 15pF (Note 3)			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = 15pF (Note 5)			30	ns
t _{PHL}	output propagation time (A, B, C, D, E, F, G, H, I, J, K, L or $M-Y$)				30	ns

SWITCHING CHARACTERISTICS ($V_{cc} = 2\sim6V$, $T_a = -40\sim+85^{\circ}C$)

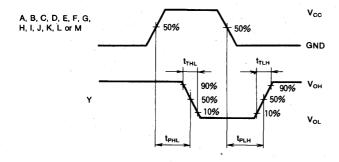
						Limits			
Symbol	Parameter	Test conditions			25℃		-40~	-+85°C	Unit
		,	V _{cc} (V)	Min	Тур	Max	Min	Max	-
			2.0			75		95	
t _{TLH}	Low-level to high-level and		4.5			15		19	ns
	No.		6.0			13		16	
	high-level to low-level		2.0			75		95	
t _{THL}	output transition time	-	4.5			15	l	19	ns
		0 -50 5 (9 + 0)	6.0			13		16	
		$C_L = 50 pF \text{ (Note 3)}$	2.0			160		190	
t _{PLH}	Low-level to high-level and		4.5			35		42	ns
	high-level to low-level		6.0			30		. 36	
	output propagation time		2.0			160		190	
t _{PHL}	(A, B, C, D, E, F, G, H, I, J)		4.5			35		42	ns
	(K, L or M — Y		6.0			30		36	
C _i	Input capacitance					10		10	pF
CPD	Power dissipation capacitance (Note 2)				32				pF

Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per gate)
The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$

Note 3: Test Circuit



- (1) The pulse generator (PG) has the following characteristics (10% \sim 90%): $t_{\rm f}=6{\rm ns},\,t_{\rm f}=6{\rm ns}$
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.



M74HC137P/FP/DP

1-OF-8 DECODER/DEMULTIPLEXER WITH ADDRESS LATCH

DESCRIPTION

The M74HC137 is a semiconductor integrated circuit consisting of a 3-bit binary to 8-line decoder/demultiplexer with address latch.

FEATURES

- Built-in address latch
- High-speed: 17ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85°C

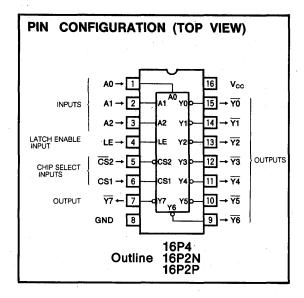
APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC137 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS137.

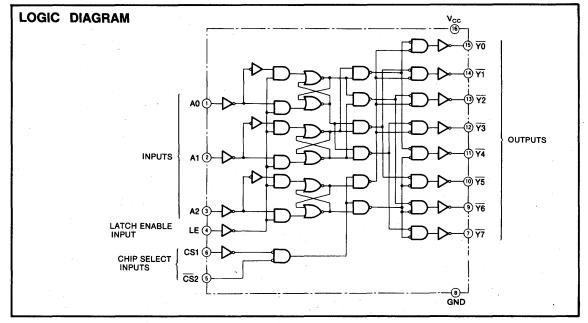
The M74HC137 consists of a 3-bit binary to 8-line decoder/demultiplexer with an address latch to store the signals of inputs A0 through A2. When latch-enable input LE is low, a 3-bit binary code is applied to inputs A0 through A2 goes through the latch and becomes a code input signal. In this case, one of outputs $\overline{Y0}$ through $\overline{Y7}$ corresponding to this value will become low and the other outputs will all be-



come high. In this case, chip select inputs CS1 and $\overline{\text{CS2}}$ should be maintained at high and low, respectively. When CS1 and $\overline{\text{CS2}}$ are in conditions other than those given above, all outputs will become high.

When LE is high, the A0 through A2 signals exisiting immediately prior to the high-level setting will be stored in the latch. In this case, those stored contens will not change even if A0 through A2 are changed.

When operated as a 1-of-8 demultiplexer, CS1 or CS2 is used as a data input and A0 through A2 are used as selecting inputs.





FUNCTION TABLE (Note 1)

		Inp	uts						Out	puts			
LE	CS1	CS2	A2	A1	A0	, Y0	<u>Y1</u>	Y2	Y3	¥4	Y5	<u>Y6</u>	
Х	X	H	Х	X	х	н	н	Н	н	Н	Н	H	Н
Х	L	X	Х	Х	Х	н	н	Н	Н	Н	Н	н	Н
L	Н	L	L	L	L	L	Н	Н	Н	Н	н	H	Н
L	Н	L	L	L	Н	Н	L	Н	Н	Н	Н	Н	Н
L	Н	L	L	Н	L	н	н	L	Н	Η.	н	Н	Н
L	Н	L	L	Н	Н	н	Н	Н	L	Н	Н	Н	Н
L	Н	L	Н	L	L	Н	Н	Н	H	L	Н	Н	Н
L	Н	L	Н	L	н	Н	Н	Н	Н	Н	L	Н	Н
L	Н	7	н	Н	L	Н	Н	Н	Н	Н	Н	L	Н
L	Н	L	Н	.H	Н	н	Н	Н	Н	Н	Н	Н	L.
Н	Н	L	Х	Х	Х	Y0°	Y10	Y20	Y3°	Y40	Y5 ⁰	Y6°	Y7º

Note 1 : X : Irrelevant

Y⁰ : Output state Y before LE changed to high level.

ABSOLUTE MAXIMUM RATINGS $(T_a = -40 \sim +85^{\circ}C)$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
Vi	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
		V ₁ < 0V	-20	4
lik	Input protection diode current	$V_{l} > V_{CC}$	20	mA
,		V ₀ < 0V	-20	
lok	Output parasitic diode current	V _o > V _{cc}	20	mA
lo	Output current per output pin		±25	mA
Icc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		-65~+150	C

Note 2 : M74HC137FP, T $_a$ = $-40\sim+70^\circ$ C and T $_a$ = $70\sim85^\circ$ C are derated at -6mW/°C. M74HC137DP, T $_a$ = $-40\sim+50^\circ$ C and T $_a$ = $50\sim85^\circ$ C are derated at -5mW/°C.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85 ^{\circ}C)$

C	Da	Parameter				Unit
Symbol	Parameter			Тур	Max	Unit
Vcc	Supply voltage		2		6	٧
Vı	Input voltage		. 0		Vcc	٧
Vo	Output voltage		0		Vcc	٧
Topr	Operating temperature ra	ange	-40		+85	°C
•		V _{CC} = 2.0V	0		1000	
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns
		V _{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

							Limits			
Symbol	Parameter	Test	Test conditions			25℃		-40~	+85℃	Unit
					Min	Тур	Max	Min	Max]
		$V_0 = 0.1V, V_{C}$	_0.1V	2.0	1.5			1.5		
V _{IH}	High-level input voltage	$ I_0 = 20\mu A$	c—0.1 V	4.5	3.15			3.15		v
		1101 - 20µA	·	6.0	4.2			4.2	·	}
	-	$V_{O} = 0.1V, V_{C}$	-0.11/	2.0			0.5		0.5	
VIL	Low-level input voltage	$ \mathbf{l}_0 = 20\mu \mathbf{A}$	c-0.1 v	4.5			1.35		1.35	l v
		(10) - 20µA		6.0			1.8		1.8]
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
			$I_{OH} = -20\mu A$	4.5	4.4		,	4.4	}	\
V _{OH}	High-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		V
	·		$I_{OH} = -4.0 \text{mA}$	4.5	4. 18			4.13		1
		1	$I_{OH} = -5.2 \text{mA}$	6.0	5. 68			5.63		
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
			$I_{OL} = 20 \mu A$	4.5			0.1		0.1)
VoL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
			I _{OL} = 4.0mA	4.5			0.26		0.33	1
	1		$I_{OL} = 5.2 mA$	6.0			0.26		0.33	
. I _{IH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μA
I _{IL}	Low-level input current	V ₁ = 0V		6.0			-0. 1		-1.0	μA
Icc	Quiescent supply current	VI = VCC, GNE	$I_0 = 0\mu A$	6.0			4.0		40.0	μА

SWITCHING CHARACTERISTICS ($V_{cc} = 5V$, $T_a = 25^{\circ}C$)

0		Total conditions		Limits		Unit
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
t _{TLH}	Low-level to high-level and high-level to low-level		-		10	ns
t _{THL}	output transition time				10	ns
t _{PLH}	Low-level to high-level and high-level to low-level				29	ns
t _{PHL}	output propagation time $(A - \overline{Y})$				42	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C ₁ = 15pF (Note 4)			22	ns
t _{PHL}	output propagation time $(\overline{CS2} - \overline{Y})$	CL = 15pr (Note 4)			34	ns
t _{PLH}	Low-level to high-level and high-level to low-level				25	ns
t _{PHL}	output propagation time (CS1 $-\overline{Y}$)				34	ns
t _{PLH}	Low-level to high-level and high-level to low-level				30	ns
t _{PHL}	output propagation time (LE $-\overline{Y}$)				44	ns

SWITCHING CHARACTERISTICS ($V_{cc} = 2\sim6V$, $T_a = -40\sim+85^{\circ}C$)

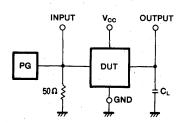
						Limits			
Symbol	Parameter	Test conditions			25℃			+85℃	Uni
			V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0			75		95	
t _{TLH}	Low-level to high-level and		4.5			15		19	ns
	high-level to low-level		6.0			13		16	
	Ingri-level to low-level		2.0			75		95	
t _{THL}	output transition time		4.5			15		19	ns
			6.0			13		16	
			2.0			170		214	
t _{PLH}	Low-level to high-level and	*	4.5			34		43	ns
	high-level to low-level		6.0			29		36	
•	output propagation time		2.0			240		302	
t _{PHL}	$(A - \overline{Y})$		4.5			48	-	60	ns
			6.0	ļ	1	41		51	
			2.0			130	,	164	
t _{PLH}	Low-level to high-level and		4.5			26		33	ns
	high-level to low-level		6.0			22		28	
	output propagation time	$C_L = 50pF (Note 4)$	2.0			195		246	
t _{PHL} .	$(\overline{CS2} - \overline{Y})$		4.5	,		39		49	ns
			6.0			33		42	
			2.0			150		189	
t _{PLH}	Low-level to high-level and		4.5			30		38	ns
	high-level to low-level	•	6.0			26		32	
	output propagation time		2.0			195		246	
t _{PHL}	$(csi - \overline{Y})$		4.5			39		49	ns
			6.0	ŀ		33		42	
		1	2.0			175		221	
t _{PLH}	Low-level to high-level and		4.5			35		44	ns
	high-level to low-level		6.0			30		37	
	output propagation time		2.0			250		315	\vdash
t _{PHL}	$(LE - \overline{Y})$	·	4.5			50		63	ns
·PHL	'/		6.0			43		54	"
Cı	Input capacitance			<u> </u>	 	10		10	pf
C _{PD}	Power dissipation capacitance (Note 3)		1		108				pl

Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot v_{CC}^2 \cdot f_1 + I_{CC} \cdot v_{CC}$

TIMING REQUIREMENTS ($V_{cc} = 2\sim 6V$, $T_a = -40\sim +85^{\circ}$)

						Limits			·
Symbol	Parameter	Test conditions			25℃	-40~+85°C Max Min Max 101 20 17 126 25 21 63 13			Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max]
100000			2.0	80			101		
t _w	LE pulse width		4.5	16			20		ns
	-		6.0	14			17		
-	A		2.0	100			126		
tsu	A setup time with respect to LE		4.5	20			25		ns
	respect to LE		6.0	17			21		
	A hold time with		2.0	50			63		
th	· ·		4.5	10	1		13		ns
	respect to LE		6.0	9			11		

Note 4: Test Circuit



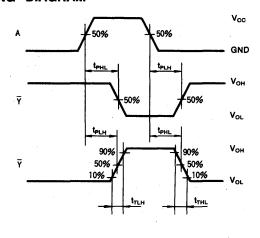
(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
 (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

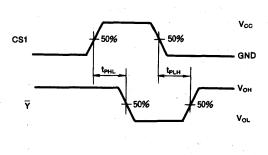
A 50% 50% GND V_{CC}

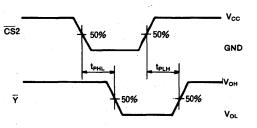
50% GND V_{CC}

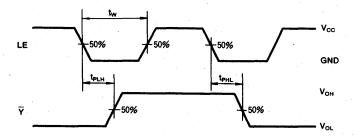
50% GND V_{CC}

50% GND V_{CC}









MITSUBISHI HIGH SPEED CMOS

M74HC138P/FP/DP

1-OF-8 DECODER/DEMULTIPLEXER

DESCRIPTION

The M74HC138 is a semiconductor integrated circuit consisting of a 3-bit binary to 8-line decoder/demultiplexer with chip select inputs.

FEATURES

- Three types of chip select inputs
- Expandable to 24 outputs without extenally connected components
- High-speed: 17ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2∼6V
- Wide operating temperature range: T_a=−40~+85°C

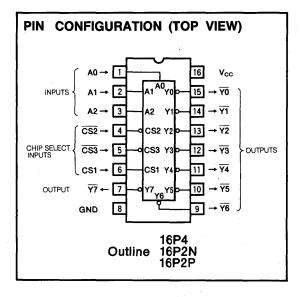
APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC138 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS138.

When operated as a decoder, a 3-bit binary code are applied to inputs A0, A1 and A2, one of outputs $\overline{Y0}$ through $\overline{Y7}$ corresponding to this value will become low and the other

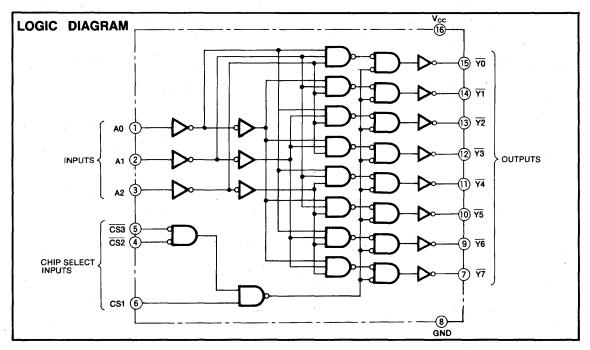


outputs will all become high.

In this case, chip select input CS1 should be maintained at high while $\overline{\text{CS2}}$ and $\overline{\text{CS3}}$ should be maintained at low.

When CS1, $\overline{\text{CS2}}$ and $\overline{\text{CS3}}$ are in conditions other than those given above, all outputs will become high irrespective of A0 through A2.

When operated as a 1-of-8 demultiplexer, CS1, $\overline{\text{CS2}}$, or $\overline{\text{CS3}}$ is used as data input and A0 through A2 input are used as slecting input.



1-OF-8 DECODER/DEMULTIPLEXER

FUNCTION TABLE (Note 1)

		Inputs					1	Out	puts			
CS1	CSX	A2	A1	A0	ΥO	<u>Y1</u>	Y2 .	Y3	¥4	Y5	¥6	¥7
X	Н	X	X	Х	Н	Н	Н	Н	Н	Н	Н	Н
L	Х	Х	х	Х	н	Н	Н	Н	Н	Н	Н	Н
н	L,	L	L	L	L	Ŧ	Н	н	Н	Н	Н	Н
Н	L	L	L	Н	Н	L	Н	Н	Н	Н	Н	Н
Н	L	L	Н	L	H	Ŧ	L	Н	Н	Н	Н	Н
н	L	L	н	Н	H	H	Н	L	н	Н	Н	н
Н	L	Н	L	L	Н	Н	Н	Н	L	н	Н	Н
Н	L	H	, L	Н	H	Н	Н	Н	н	L	Н	Н
Н	L	Н	н	L	н	н	Н	Н	Н	Н	L	Н
Н	L	H	Н	Н	Н	H	Н	Н	Н	Н	Н	L'

Note 1 : $\overline{CSX} = \overline{CS2} + \overline{CS3}$

X: Irrelevant

ABSOLUTE MAXIMUM RATINGS $(T_a = -40 \sim +85 \degree\text{C}, \text{ unless otherwise noted})$

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		−0.5~+7.0	V
V,	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
		V ₁ < 0V	-20	
l _{iK}	Input protection diode current	V _I > V _{CC}	20	mA mA
		V ₀ < 0V	-20	
ок	Output parasitic diode current	Vo > Vcc	20	mA
lo	Output current per output pin		±25	mA
Icc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65~+150	°C

Note 2 : M74HC138FP, T_a = $-40\sim+70^\circ$ C and T_a = $70\sim85^\circ$ C are derated at -6mW/°C. M74HC138DP, T_a = $-40\sim+50^\circ$ C and T_a = $50\sim85^\circ$ C are derated at -5mW/°C.

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85 \degree C)$

Completed.	n-			Limits				
Symbol	Pa	rameter	Min	Тур	Max	Unit		
Vcc	Supply voltage		2		6	٧		
V _I	Input voltage		0		Vcc	٧		
V _o	Output voltage		0		Vcc	٧		
Topr	Operating temperature ra	inge	-40		+85	°C		
		V _{CC} = 2.0V	0		1000			
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns		
		$V_{CC} = 6.0V$	0		400	1		

M74HC138P/FP/DP

1-OF-8 DECODER/DEMULTIPLEXER

ELECTRICAL CHARACTERISTICS

		-					Limits			
Symbol	Parameter	Test	conditions			25℃		-40~	+85℃	Unit
				V _{CC} (V)	Min	Тур	Max	Min	Max]
		V = 0.1V V	$V_{O} = 0.1V$, $V_{CC} = 0.1V$ 2. $ I_{O} = 20\mu A$ 6.		1.5			1.5		
ViH	High-level input voltage				3.15		1	3.15		V
		1101 = 20µA			4.2			4.2		
		V = 0.1V V	$V_0 = 0.1V, V_{CC} - 0.1V$				0.5		0.5	
VIL	Low-level input voltage	1	$ V_0 = 0.1V, V_{CC} = 0.1V$ $ I_0 = 20\mu A$ 4.5				1.35		1.35	V
	110	$ I_0 = 20\mu A$					1.8	,	1.8	ĺ
			$l_{OH} = -20\mu A$	2.0	1.9	1		1.9		
			$I_{OH} = -20\mu A$	4.5	4.4			4.4		
VoH	High-level output voltage	$V_i = V_{iH}, \ V_{iL}$	$I_{OH} = -20\mu A$	4.5 4.4 6.0 5.9		5.9		V		
	•		$I_{OH} = -4.0 \text{mA}$	4.5	4.18			4.13		}
	-		$I_{OH} = -5.2 mA$	6.0	5.68			5. 63		İ
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
			$I_{OL} = 20 \mu A$	4.5			0.1		0.1	
VoL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	v
			I _{OL} = 4.0mA	4.5			0. 26		0.33	ĺ
			I _{OL} = 5. 2mA	-6. O			0. 26		0.33	
l _{iH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μA
I _{IL}	Low-level input current	V ₁ = 0V	V ₁ = 0V				-0.1		-1.0	μΑ
Icc	Quiescent supply current	VI = VCC, GND	$I_0 = 0 \mu A$	6.0			4.0		40.0	μА

SWITCHING CHARACTERISTICS ($v_{cc} = 5v$, $\tau_a = 25^{\circ}$)

0	2	T-A-SHA		Limits		Unit
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
tTLH	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time				10	ns
t _{PLH}	Low-level to high-level and high-level to low-level				25	ns
t _{PHL}	output propagation time (A - Y)	0 = 15-5 (Note 4)			35	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = 15pF (Note 4)		-	25	ns
t _{PHL}	output propagation time (CS1 $-\overline{Y}$)				25	ns
t _{PLH}	Low-level to high-level and high-level to low-level				25	ns
t _{PHL}	output propagation time $(\overline{CS2}, \overline{CS3} - \overline{Y})$				30	ns

1-OF-8 DECODER/DEMULTIPLEXER

SWITCHING CHARACTERISTICS ($v_{cc} = 2\sim6V$, $T_a = -40\sim+85$ °C)

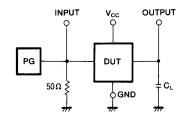
						Limits			
Symbol	Parameter	Test conditions	 		25℃		-40~	+85℃	Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0			75		95	
t _{TLH}	Low-level to high-level and		4.5			15		19	ns
	high-level to low-level		6.0			13		16	
	Tilgii-level to low-level	, .	2.0			75		95	
t _{THL}	output transition time		4.5			15		19	ns
			6.0			13		16	
] .	2.0			150		189	
t _{PLH}	Low-level to high-level and		4.5			30		38	ns
	high-level to low-level		6.0	1		26		32	
	output propagation time		2.0			200		252	
t _{PHL}	$(A - \overline{Y})$,	4.5			40		50	ns
		C = 50=5 (N=4= 4)	6.0			. 34		43	-
		C _L = 50pF (Note 4)	2.0			150		189	
t _{PLH}	Low-level to high-level and		4.5	l		30		38	ns
	high-level to low-level		6.0			26		32	
	output propagation time		2.0			150		189	
t _{PHL}	(CS1 − \(\overline{Y} \)		4.5			30		38	ns
		* * * * * * * * * * * * * * * * * * * *	6.0			26		32	
			2.0			150		189	
t _{PLH}	Low-level to high-level and		4.5			30		38	ns
	high-level to low-level		6.0			26		32	
	output propagation time		2.0			175		221	
t _{PHL}	$(\overline{CS2}, \overline{CS3} - \overline{Y})$		4.5			35		44	ns
	· ·		6.0			30		37	
Cı	Input capacitance				100	10		10	pF
C _{PD}	Power dissipation capacitance (Note 3)				82				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$



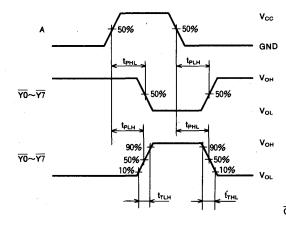
1-OF-8 DECODER/DEMULTIPLEXER

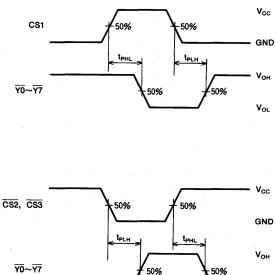
Note 4: Test Circuit



- (1) The pulse generator (PG) has the following characteristics (10% \sim 90%): t_r = 6ns, t_r = 6ns (2) The capacitance C_L includes stray wiring
- capacitance of includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





Vol

M74HCT138P/FP/DP

1-OF-8 DECODER/DEMULTIPLEXER WITH LSTTL-COMPATIBLE INPUTS

DESCRIPTION

The M74HCT138 is a semiconductor integrated circuit consisting of a 3-bit binary-to 8-line decoder/demultiplexer with chip-select inputs.

FEATURES

- TTL level input V_{IL} = 0.8V max V_{IH} = 2.0V min
- Three types of chip-select inputs
- High-speed: 17ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC} + 2∼6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

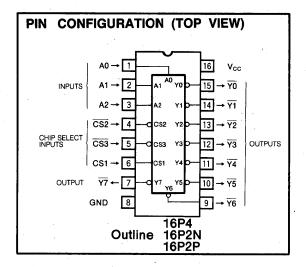
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HCT138 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS138.

As the inputs are TTL level, the device can be used as a level converter from LSTTL to high-speed CMOS. In that case, no pull-up resistors are required.

When operated as a decoder, a 3-bit binary code are applied to inputs A0, A1 and A2, one of outputs $\overline{Y0}$ through $\overline{Y7}$

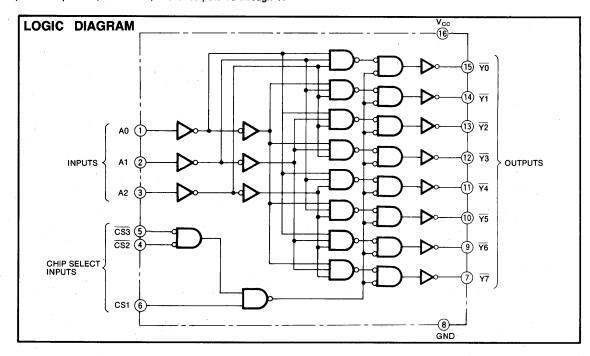


corresponding to this value will become low and the other outputs will all become high.

In this case, chip select input CS1 should be maintained at high while $\overline{\text{CS2}}$ and $\overline{\text{CS3}}$ should be maintained at low.

When CS1, $\overline{\text{CS2}}$ and $\overline{\text{CS3}}$ are in conditions other than those given above, all outputs will become high irrespective of A0 through A2.

When operated as a 1-of-8 demultiplexer, CS1, $\overline{\text{CS2}}$ or $\overline{\text{CS3}}$ is used as data input and A0 through A2 input are used as slecting input.



1-OF-8 DECODER/DEMULTIPLEXER WITH LSTTL-COMPATIBLE INPUTS

FUNCTION TABLE (Note 1)

		Inputs					1	Out	puts			
CS1	CSX	A2	A1	A0	YO	<u>Y1</u>	Y2	Y3	<u>¥4</u>	¥5	Y6	¥7
Х	H	Х	х	X	.H	Н	Н	Н	Н	Н	Н	Н
L	X	х	Х	Х	Н	н	Н	н	Н	Н	Н	Н
Н	L	L	L	L	L	Н	Н	н	Н	Н	Н	Н
Н	L	L	L	н	Н	L	Н	Н	Н	Н	Н	Н
Н	L	L	Н	L	н	н	L	Н	Н	Н	Н	Н
Н	L	L	Н	Н	н	н	Н	L	н	Н	Н	Н
н	L	Н	L	L	н	Н	Н	Н	L	Н	Н	Н
н	_	Н	L	Н	Н	Н	Н	Н	Н	L	Н	Н
н	L	Н	Н	L	Н	H	Н	Н	Н	Н	L	H
Н	L	Н	Н	Н	H-	Н	Н	н	Н	Н	Н	L

Note 1 : $\overline{CSX} = \overline{CS2} + \overline{CS3}$

X: Irrelevant

$\textbf{ABSOLUTE} \quad \textbf{MAXIMUM} \quad \textbf{RATINGS} \ (\textbf{T}_a = -40 \sim +85 °\text{C}, \text{ unless otherwise noted})$

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage		-0.5~+7.0	V
Vi	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
	In the second se	V ₁ < 0V	-20	
l _{IK}	Input protection diode current	$V_1 > V_{CC}$	20	mA
	0 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4	V ₀ < 0V	-20	
lok	Output parasitic diode current	$v_o > v_{cc}$	20	mA mA
lo	Output current, per output pin		±25	mA
Icc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65~ + 150	င

Note 2 : M74HC138FP, T $_{\rm a}=-40\sim+70^\circ{\rm C}$ and T $_{\rm a}=70\sim85^\circ{\rm C}$ are derated at -6mW/°C. M74HC138DP, T $_{\rm a}=-40\sim+50^\circ{\rm C}$ and T $_{\rm a}=50\sim85^\circ{\rm C}$ are derated at -5mW/°C.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85 \degree C)$

0			Limits Max 4.5 5.5 O V _{CC} O V _{CC} -40 +85 O 1000 O 500		11-14	
Symbol	Pa	rameter	Min	Тур	Max	Unit
Vcc	Supply voltage		4.5		5. 5	V
V _i	Input voltage		0		V _{cc}	V
Vo	Output voltage		0		Vcc	V
Topr	Operating temperature ra	ange	-40		+85	င
		$V_{CC} = 2.0V$	0		1000	
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns .
		$V_{CC} = 6.0V$	0		400	

1-OF-8 DECODER/DEMULTIPLEXER WITH LSTTL-COMPATIBLE INPUTS

ELECTRICAL CHARACTERISTICS ($V_{cc} = 5V \pm 10\%$, unless otherwise noted)

						Limits				
Symbol	Parameter	-	Test conditions		25℃		-40~	-40~+85°C		
			Min	Тур	Max	Min	Max			
V _{IH}	High-level input voltage	$V_{O} = 0.1V$ $ I_{O} = 20\mu A$	$I_{O} =20\mu A$			1	2.0		V	
VIL	Low-level input voltage	$V_{CC} = 0.1 \text{ V}, V_{CC}$ $ I_0 = 20 \mu \text{ A}$	-0.1V			0.8		0.8	٧	
			$I_{OH} = -20\mu A$	V _{CC} -0.1			V _{CC} -0.1			
VoH	High-level output voltage	V _I = V _{IL}	$I_{OH} = -4.0 \text{mA}, V_{CC} = 4.5 \text{V}$	4.18			4.13		V	
			$I_{OH} = -4.8 \text{mA}, V_{CC} = 5.5 \text{V}$	5.18		ļ	5.13			
			$I_{OL} = 20\mu A$			0.1		0.1		
VoL	Low-level output voltage	$V_{l} = V_{lH}, V_{lL}$	$I_{OL} = 4.0 \text{mA}, V_{CC} = 4.5 \text{V}$			0. 26		0.33	V	
	1		$I_{OL} = 4.8 \text{mA}, V_{CC} = 5.5 \text{V}$			0. 26		0. 33		
I _{IH}	High-level input current	V ₁ = 5.5V			No.	0.1		1.0		
I _{IL}	Low-level input current	$V_i = 0V$				-0.1		-1.0	μΑ	
Icc	Quiescent supply current	VI = VCC, GND	$I_0 = 0\mu A$			4.0		40.0	μΑ	
ΔI_{CC}	Maximum quiescent state supply current	$V_1 = 2.4V, 0.4V$	/ (Note 3)			2.7		2.9	mA	

Note $\,3\,:\,$ Only one input is set at this value and all others are fixed at V_{CC} or GND.

SWITCHING CHARACTERISTICS ($v_{cc} = 5v$, $T_a = 25^{\circ}C$)

Complete	Danner	T4		Limits		
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
t _{TLH}	Low-level to high-level and high-level to low-level			-	10	ns
t _{THL}	output transition time	A Company of the Comp		-	10	ns
t _{PLH}	Low-level to high-level and high-level to low-level		7 7 7		25	ns
t _{PHL}	output propagation time $(A - \overline{Y})$	O == 15=5 (Note 5)			35	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = 15pF (Note 5)			25	ns
t _{PHL}	output propagation time (CS1 $-\overline{Y}$)				25	ns
t _{PLH}	Low-level to high-level and high-level to low-level	1			25	ns
t _{PHL}	output propagation time ($\overline{CS2}$, $\overline{CS3} - \overline{Y}$)			1	30	ns

SWITCHING CHARACTERISTICS ($V_{cc} = 5V \pm 10\%$, $T_a = -40 \sim +85^{\circ}C$)

					Limits			
Symbol	Parameter	Test conditions		25°C	-40~+85℃		Unit	
	,		Min	Тур	Max	Min	Max	
t _{TLH}	Low-level to high-level and high-level				15		19	ns
t _{THL}	to low-level output transition time		-		15		19	ns
t _{PLH}	Low-level to high-level and				30		38	ns
t _{PHL}	high-level to low-level output propagation time (A-Y)	C = 50-5 (Note: 5)			40		50	ns
t _{PLH}	Low-level to high-level and	C _L = 50pF (Note 5)			30		38	ns
t _{PHL}	high-level to low-level output propagation time (CS1-Y)			٠.	30		38	ns
t _{PLH}	Low-level to high-level and high-level to low-level output				30		38	ns
t _{PHL}	propagation time (CS2, CS3-Y)				35		43	ns
Cı	Input capacitance				10		10	pF
C _{PD}	Power dissipation capacitance (Note 4)		1.					pF

Note 4: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.

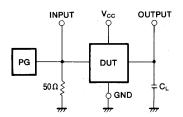
The power dissipated during operation under no-load conditions is calculated using the following formula:

P_D = C_{PD} · V_{CC}² · f₁+I_{CC} · V_{CC}

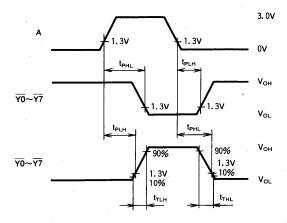


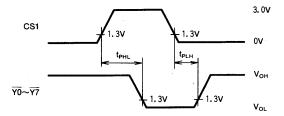
1-OF-8 DECODER/DEMULTIPLEXER WITH LSTTL-COMPATIBLE INPUTS

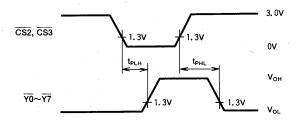
Note 5: Test Circuit



- (1) The pulse generator (PG) has the following characteristics (10% \sim 90%): $t_r = 6ns$, $t_f = 6ns$ (2) The capacitance C_L includes stray wiring
- capacitance and the probe input capacitance.







M74HC139P/FP/DP

DUAL 1-OF-4 DECODER/DEMULTIPLEXER

DESCRIPTION

The M74HC139 is a semiconductor integrated circuit consisting of a 2-bit binary to divide-by-4 decoder/demultiplexer with chip select inputs.

FEATURES

- Chip select inputs
- High-speed: 19ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=-40~+85℃

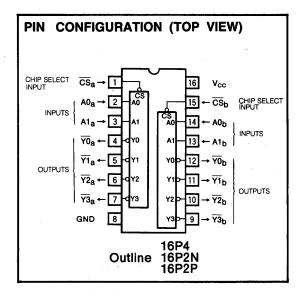
APPLICATION

General purpose, for use in industrial and consumer digital equipment.

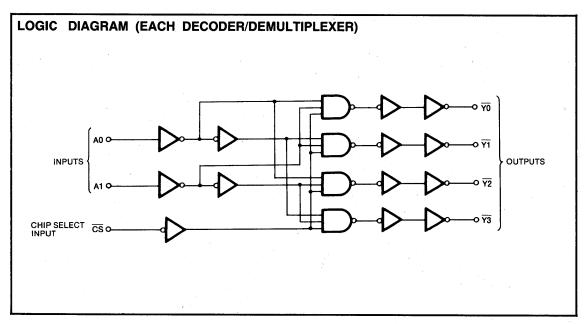
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC139 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS139.

When operated as a decoder, a 2-bit binary code are applied to inputs A0 and A1, one of outputs $\overline{Y0}$ through $\overline{Y3}$ corresponding to this value will become low and the other outputs will all become high. In this case, chip select input \overline{CS} should be maintained at low. When \overline{CS} is high, all outputs will become high irrespective of A0 and A1.



When operated as a 1-of-4 demultiplexer, \overline{CS} is used as a data input and A0 and A1 are used as slecting inputs.





DUAL 1-OF-4 DECODER/DEMULTIPLEXER

FUNCTION TABLE (Note 1)

	Inputs		Outputs			
CS	A1	A0	ΥÖ	<u> 71</u>	<u>Y2</u>	Y3
L	L	L	L	н	Н	Н
L	L	Н	н	L	Н	Н
L	Н	L	н	н	L	Н
L	н	Н	Н	Н	Н	L
Н	x	Х	н	н	н	н

Note 1 : X: Irrelevant

ABSOLUTE MAXIMUM RATINGS $(T_a = -40 \sim +85 \degree\text{C}, \text{ unless otherwise noted})$

Symbol	Parameter	Conditions	Ratings	Unit		
Vcc	Supply voltage		-0.5~+7.0	V		
Vı	Input voltage		-0.5~V _{cc} +0.5	V		
V _o	Output voltage		-0.5~V _{cc} +0.5	V		
I _{IK}	Input protection diode current	V ₁ < 0V	-20	mA		
	input protection diode current	V ₁ > V _{CC}	20			
,		V ₀ < 0V				
юк	Output parasitic diode current	Vo > Vcc	20	mA.		
lo .	Output current per output pin		±25	mA		
Icc	Supply/GND current	V _{CC} , GND	±50	mA		
Pd	Power dissipation	(Note 2)	500	mW		
Tstg	Storage temperature range		-65~+150	င		

Note 2 : M74HC139FP, T $_{\rm a}=-40\sim+70$ °C and T $_{\rm a}=70\sim85$ °C are derated at -6mW/°C. M74HC139DP, T $_{\rm a}=-40\sim+50$ °C and T $_{\rm a}=50\sim85$ °C are derated at -5mW/°C.

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85\%)$

				Limits				
Symbol	Pa	rameter	Min	Тур				
V _{CC}	Supply voltage		2		6	٧		
Vı	Input voltage		0		Vcc	V		
Vo	Output voltage		0		Vcc	٧		
Topr	Operating temperature range		-40		+85	ပ္		
		V _{CC} = 2.0V	0		1000			
t _r , t _f	Input risetime, falltime	V _{CC} = 4.5V	0		500	ns		
,		$V_{CC} = 6.0V$	0		400	-		

ELECTRICAL CHARACTERISTICS

						Limits				_].	
Symbol	Parameter	Test	conditions			25℃		-40~	-40~+85℃		
	. "			V _{CC} (V)	Min	Тур	Max	Min	Max		
		$V_0 = 0.1V, V_0$	0.11/	2.0	1.5			1.5			
VIH	High-level input voltage	$ V_0 = 0.1V, V_0 $ $ I_0 = 20\mu A$		4.5	3. 15			3. 15	0. 5 1. 35 1. 8	V	
		$ 1_0 = 20\mu A$		6.0	4. 2			4.2			
		$V_0 = 0.1V, V_{C}$	0 11/	2.0			0.5		0.5		
VIL	Low-level input voltage	$ V_0 = 0.1V, V_0 $ $ I_0 = 20\mu A$	50. TV	4.5			1.35		1.35	V	
	·	101 = 20µA		6.0	ļ	į	1.8	ļ	1.8		
			$I_{OH} = -20 \mu A$	2.0	1.9			1.9			
		,	$I_{OH} = -20\mu A$	4.5	4. 4			4.4			
VOH	High-level output voltage	$V_i = V_{iH}, \ V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		V	
			I _{OH} = -4.0mA	4.5	4. 18			4.13			
	*		$I_{OH} = -5.2 \text{mA}$	6.0	5.68			5. 63			
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1		
			$I_{OL} = 20 \mu A$	4,5		į	0.1		0.1		
Vol .	Low-level output voltage	$V_i = V_{iH}, \ V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	v	
			I _{OL} = 4.0mA	4.5			0. 26		0.33		
			I _{OL} = 5. 2mA	6.0			0. 26		0.33		
l _{iH}	High-level input current	$V_t = 6V$		6.0			0.1		1.0	μА	
I _{IL}	Low-level input current	V ₁ = 0V		6.0			-0.1		-1.0	μA	
lcc	Quiescent supply current	VI = VCC, GND	$I_0 = 0 \mu A$	6.0			4.0		40.0	μA	

DUAL 1-OF-4 DECODER/DEMULTIPLEXER

SWITCHING CHARACTERISTICS ($v_{cc} = 5v$, $\tau_a = 25^{\circ}C$)

Symbol	Barranatar	Test conditions		Limits		Unit
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time	C ₁ = 15pF (Note 4)			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level .	C _L = 15pF (Note 4)			30	ns
t _{PHL}	output propagation time $(\overline{CS} - \overline{Y})$				30	ns
t _{PLH}		Number of delay		1	30	ns
t _{PHL}	Low-level to high-level and high-level to low-level output propagation time (A $-\overline{Y}$)	gate stages 4			30	ns
t _{PLH}		Number of delay			38	ns
t _{PHL}		gate stages 5			38	ns

SWITCHING CHARACTERISTICS $(V_{cc} = 2\sim6V, T_{a} = -40\sim+85^{\circ}C)$

						Limits			
Symbol	Parameter	Test conditions			25℃		-40~	+85℃	Unit
		•	V _{cc} (V)	Min	Тур	Max Min	Min	Max	
			2.0			75		95	
t _{TLH}	Low-level to high-level and		4.5			15		19	ns
	high lavel to law level		6.0			13		- 16	
	high-level to low-level	·	2.0			75		95	
t _{THL}	output transition time	,	4.5		1	15		19	ns
		C _L = 50pF (Note 4)	6.0			13		16	
		CL = 50pr (Note 4)	2.0			175		219	
t _{PLH}	Low-level to high-level and		4.5			35		44	ns
	high-level to low-level	·	6.0			30		38	
output propagation time t_{PHL} $(\overline{CS} - \overline{Y})$	output propagation time		2.0	,		175		219	
	$(\overline{CS} - \overline{Y})$		4.5			- 35		44	ns
			6.0			30		38	
		,	2.0			175		219	
t _{PLH}		Number of delay	4.5			35		44	ns
		Number of delay	6.0			30		38	-
	1		2.0			175		219	
t _{PHL}	Low-level to high-level and	gate stages 4	4.5			35		.44	ns
	high-level to low-level		6.0			30		38	
	output propagation time		2.0			220		275	
t _{PLH}	$(A - \overline{Y})$	Number of delay	4.5			44		55	ns
		Number of delay	6.0			38	,	47	
	7		2.0			220		275	
t _{PHL}		gate stages 5	4.5			44		55	ns
			6.0			38		47	
Cı	Input capacitance					10		10	pF
C _{PD}	Power dissipation capacitance (Note 3)				62	×			pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per decoder)

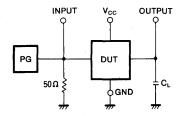
The power dissipated during operation under no-load conditions is calculated using the following formula:

P_D = C_{PD} · V_{CC}² · f₁+I_{CC} · V_{CC}

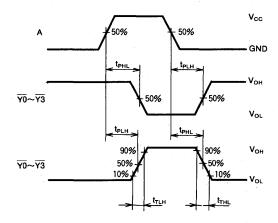


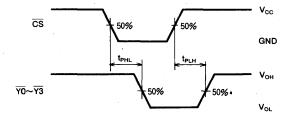
DUAL 1-OF-4 DECODER/DEMULTIPLEXER

Note 4: Test Circuit



- (1) The pulse generator (PG) has the following characteristics (10%~90%): $\rm t_f=6ns, \ t_f=6ns$
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.





M74HC147P/FP/DP

10-LINE DECIMAL TO 4-LINE BCD PRIORITY ENCODER

DESCRIPTION

The M74HC147 is a semiconductor integrated circuit consisting of a 10-line decimal to 4-line BCD encoder with priority.

FEATURES

- Priority for data input
- High-speed: 16ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85°C

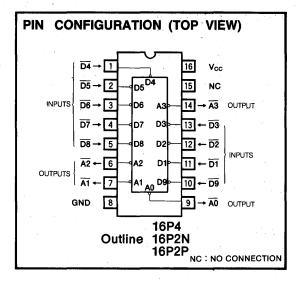
APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

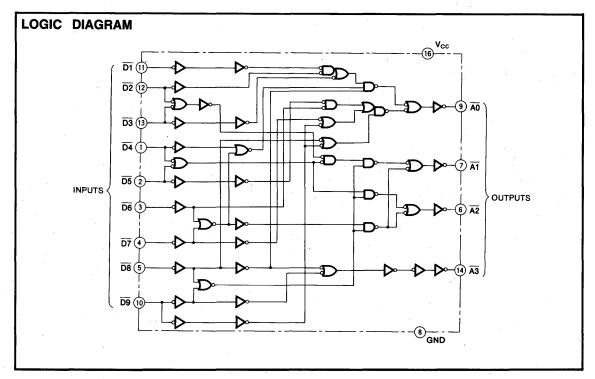
Use of silicon gate technology allows the M74HC147 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS147.

When an input is applied to one of the nine input lines $\overline{D1}$ through $\overline{D9}$, the corresponding inverted BCD code is output



at $\overline{A0}$ through $\overline{A3}$. When more than one input is applied simultaneously, the signal at the highest order input pin is given priority.

DO does not exist as an input, and when all inputs are high, all outputs will become high, allowing zero to be obtained. The device is ideal for Keyboard encoders or range selectors.



10-LINE DECIMAL TO 4-LINE BCD PRIORITY ENCODER

FUNCTION TABLE (Note 1)

				Inputs						Out	puts	
D1	D2	D3	D4	D5	D6	D7	D8	D9	A3	A2	A1	Ã0
• Н	Н	Н	Н	Н	Н	Н	н	Н	Н	Н	Н	Н
Х	X	Х	X	X	Х	х	Х	L	L	Н.	Н	L
Х	Х	Х	х	X	х	х	L	Н	L	Н	н	Н
х	Х	×	х	X	х	L	Н	Н	Н	L	L	L
Х	X	х	X	х	L	Н	Н	Н	Н	L	L	Н
Х	Х	X	Х	L	Н	H.	Н	Н	Н	L	Н	٦
X	Х	Х	L	Н	Н	Н	Н	Н	Н	L	Н	Н
X	X	L	Н	Н	Н	Н	Н	H	Н	Н	L	L
X	L	Н	Н	Н	Н	н	Н	Н	Н	Н	L	Н
L	H	Н	Н	Н	Н	Н	Н	Η	Н	Н	Н	L

Note 1: X: Irrelevant

ABSOLUTE MAXIMUM RATINGS $(T_a = -40 \sim +85^{\circ}C)$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	,	−0.5∼+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage	·	-0.5~V _{cc} +0.5	٧
	In the second se	V ₁ < 0V	-20	
1 _{IK}	Input protection diode current	$V_1 > V_{CC}$	20	mA
	Outrook to annuality add and a command	V ₀ < 0V	-20	
1 _{OK}	Output parasitic diode current	V _o > V _{cc}	20	mA
lo	Output current per, output pin		±25	mA
Icc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		-65∼+150	င

Note 2 : M74HC147FP, $T_a = -40 \sim +70^\circ C$ and $T_a = 70 \sim 85^\circ C$ are derated at -6mW/°C. M74HC147DP, $T_a = -40 \sim +50^\circ C$ and $T_a = 50 \sim 85^\circ C$ are derated at -5mW/°C.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85\%)$

0		Parameter			Limits					
Symbol	Pai	rameter	Min	Тур	Max	Unit				
V _{CC}	Supply voltage		2		6	V				
Vı	Input voltage	0		V _{CC}	V					
Vo	Output voltage	Output voltage			V _{cc}	٧				
Topr	Operating temperature ra	ange	40		+85	င				
		V _{CC} = 2.0V	. 0	-	1000					
t _r , t _f	Input risetime, falltime	V _{CC} = 4.5V	0		500	ns				
		0	0							

10-LINE DECIMAL TO 4-LINE BCD PRIORITY ENCODER

ELECTRICAL CHARACTERISTICS

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					Limits					
Symbol	Parameter	Test	conditions		25℃			-40~	+85°C	Unit
				V _{cc} (V)	Min	Тур	Max	Min	Max	ĺ
		N - 0 111 11	^ 11.í	2.0	1.5			1.5		
VIH	High-level input voltage	$V_0 = 0.1V$, V_{cc}	;0.1V	4.5	3.15			3.15		V
	1	$ I_0 = 20\mu A$	$ 10 = 20\mu\text{A}$		4.2		•	4.2		
		V -0.111 V	A 114	2.0			0.5	"	0.5	
VIL	Low-level input voltage	$V_0 = 0.1V, V_{CO}$	<u>-0.1V</u>	4.5			1.35		1.35	v
		$ I_{O} = 20\mu A$		6.0		1	1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
			$I_{DH} = -20 \mu A$	4.5	4.4			4. 4		
VoH	High-level output voltage	$V_{I} = V_{IH}, V_{IL}$	$I_{OH} = -20\mu A$	6.0	5.9			5. 9		v
		l.	$I_{OH} = -4.0 \text{mA}$	4.5	4.18		1.3	4.13	400	<u> </u>
			$I_{OH} = -5.2 mA$	6.0	5. 68			5. 63		
			$I_{OL} = 20 \mu A$	2.0			0.1		0. 1	
			$I_{OL} = 20 \mu A$	4.5			.0.1		0. 1	
VoL	Low-level output voltage	$V_{I} = V_{IH}, V_{IL}$	$I_{OL} = 20 \mu A$	6.0			0.1	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	0.1	V
			I _{OL} = 4.0mA	4. 5			0.26		0, 33	
			$I_{OL} = 5.2 \text{mA}$	6.0			0.26		0.33	
I _{IH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μΑ
I _{IL}	Low-level input current	V ₁ = 0V		6.0			—0. 1		-1.0	μA
Icc	Quiescent supply current	Vi = Vcc, GND	$I_0 = 0 \mu A$	6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS $(V_{cc} = 5V, T_a = 25^{\circ}C)$

		T4		Limits			
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit	
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns	
t _{THL}	output transition time	0 = 15-5 (N-4-4)			10	ns	
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = 15pF (Note 4)			26	ns	
t _{PHL}	output propagation time $(\overline{D1} \sim \overline{D9} - \overline{A0} \sim \overline{A3})$				26	ns	

SWITCHING CHARACTERISTICS $(V_{cc} = 2\sim6V, T_a = -40\sim+85^{\circ}C)$

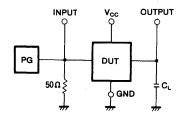
		7							
Symbol	Parameter	Test conditions			25℃		-40~	+85℃	Unit
	1.0		V _{cc} (V)	Min	Тур	Max	Min	Max	_
			2.0		1	75		95	
t _{TLH}	Low-level to high-level and		4.5			15		19	ns
			6.0			13		16	
	high-level to low-level		2.0			75		95	
t _{THL}	output transition time	the state of the s	4.5			15		19	ns
		50 5/44 . 4	6.0			13		.16	
· · · · · · · · · · · · · · · · · · ·		$C_L = 50 pF \text{ (Note 4)}$	2.0			150	,	190	
t _{PLH}	Low-level to high-level and		4.5			30		38	ns
	high-level to low-level		6.0			26		33	
	output propagation time		2.0			150		190	
t _{PHL}	$(\overline{D} - \overline{A})$	•	4.5	i		30	}	38	ns
			6.0	-	,	26		33	
Cı	Input capacitance					10		10	pF
C _{PD}	Power dissipation capacitance (Note 3)	,							pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{|} + I_{CC} \cdot V_{CC}$



10-LINE DECIMAL TO 4-LINE BCD PRIORITY ENCODER

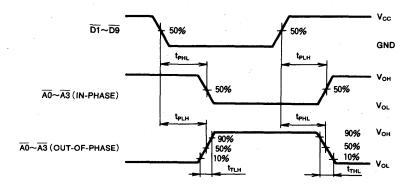
Note 4: Test Circuit



- (1) The pulse generator (PG) has the following
- characteristics (10%~90%): t_r = 6ns, t_f = 6ns

 (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



M74HC148P/FP/DP

8-LINE TO 3-LINE PRIORITY ENCODER

DESCRIPTION

The M74HC148 is a semiconductor integrated circuit consisting of an 8-line binary octal encoder with priority.

FEATURES

- Priority for date input
- Easily expandable number of input bits
- High-speed: 16ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: Ta=-40~+85℃

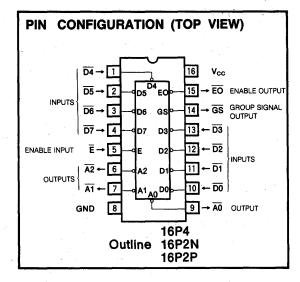
APPLICATION

General purpose, for use in industrial and consumer digital equipment.

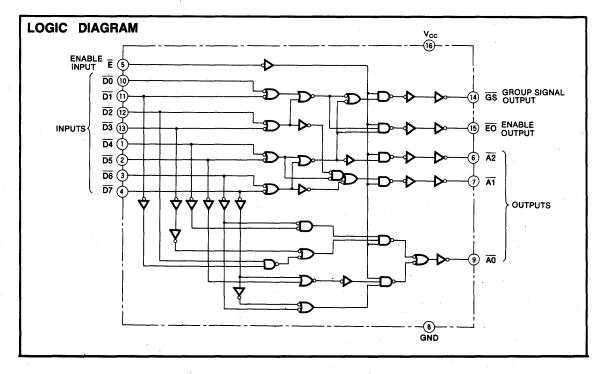
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC148 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS148.

When an input is applied to one of the eight input lines $\overline{D0}$ through $\overline{D7}$, the corresponding 3-bit binary code is output at $\overline{A0}$ through $\overline{A2}$. When more than one input is applied simultaneously, the highest order pin is given priority. By using



enable-input \overline{E} , enable-output \overline{EO} , and group-signal output \overline{GS} , the number of lines can be easily expanded, making the device ideal for keyboard encoders and range selectors.





8-LINE TO 3-LINE PRIORITY ENCODER

FUNCTION TABLE (Note 1)

				Inputs							Outputs		
Ē	D0	D1	D2	D3	D4	D5	D6	D7	Ā2	A1	ÃÔ	GS	EO
Н	Χ.	×	X	X	Х	Х	Х	Х	н	н	Н	Н	Н
L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L
L	Х	X	х	X	Х	Х	х	L	L	L	L	L	Н
L	Х	Х	X	X	X	Х	L	Н	L	L	н	L	н
L	, X	X	X	X	Х	L	Н	Н	L	Н	L	L	Н
L	X	Х	Х	Х	L	Н	Н	Н	L	Н	Н	L	Н
L	X	х	х	L	Н	Н	н	н	Н	L	L	L	н
L	Х	Х	L	Н	н	н	н	Н	Н	L	Н	L	н
L	Х	L	Н	Н	Н	Н	Н	н	Н	Н	L	L	Н
L	L	Н	Н	Н	Н	Н	Н	Н	. н	Н	Н	L	н

Note 1: X: Irrelevant

ABSOLUTE MAXIMUM RATINGS $(T_a = -40 \sim +85^{\circ}C)$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	٧
	Innut avatastica diada aumant	V ₁ < 0V	-20	
lik .	Input protection diode current	V _i > V _{CC}	20	mA
	Output paraditio diada aureant	V ₀ < 0V	-20	
lok	Output parasitic diode current	Vo > Vcc	20	mA
lo	Output current per, output pin		±25	mA
Icc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		-65~+150	က်

Note 2 : M74HC148FP, T_a = $-40\sim+70^\circ$ C and T_a = $70\sim85^\circ$ C are derated at -6mW/°C. M74HC148DP, T_a = $-40\sim+50^\circ$ C and T_a = $50\sim85^\circ$ C are derated at -5mW/°C.

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85 \degree C)$

Cumbal	000	rameter		Limits					
Symbol	Pa	rameter	Min	Тур	Max	Unit			
V _{CC}	Supply voltage		2		6	V			
V _I	Input voltage		0		Vcc	V			
V _o	Output voltage	Output voltage			Vcc	V			
Topr	Operating temperature ra	ange	40	-	+85	°C			
		V _{CC} = 2.0V	0		1000				
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns			
		V _{CC} = 6.0V	0 -		400	1			

8-LINE TO 3-LINE PRIORITY ENCODER

ELECTRICAL CHARACTERISTICS

					Limits]
Symbol	Parameter	Test	conditions		25℃			-40~	+85℃	Unit
				V _{CC} (V)	Min	Тур	Max	Min	Max	
		V = 0.1V V	$V_0 = 0.1V, V_{CC} = 0.1V$		1.5			1.5		
V _{IH}	High-level input voltage	$ 1_0 = 20 \mu A$	3 0.1.¥	4. 5	3. 15			3. 15	·	V
-		6.		6.0	4. 2			4.2		
		$V_0 = 0.1V, V_{CC} = 0.1V$		2.0			0.5		0.5	
VIL	Low-level input voltage	$ I_0 = 20\mu A$	50.1 V	4.5			1.35		1.35	
		1101 = 20µA		6.0			1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		,
		$I_{OH} = -20\mu A$	4.5	4.4			4. 4			
V _{OH}	High-level output voltage	$V_l = V_{lH}, V_{lL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		. v
			$I_{OH} = -4.0 \text{mA}$	4.5	4. 18			4.13		}
		,	$I_{OH} = -5.2 mA$	6.0	5. 68			5.63		
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
			$I_{OL} = 20 \mu A$	4.5			0.1	200	0.1	
VoL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	l v
			I _{OL} = 4.0mA	4.5			0. 26		0.33	1
			I _{OL} = 5. 2mA	6.0			0. 26		0.33	
I _{IH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	
I _{IL}	Low-level input current	V ₁ = 0V		6.0			-0.1		-1.0	μA
Icc	Quiescent supply current	VI = VCC, GND	$I_0 = 0\mu A$	6.0			4.0		40.0	μΑ

SWITCHING CHARACTERISTICS (Vcc = 5V, Ta = 25°C)

O		T-skdistance	Limits			Unit
Symbol	Parameter	Test conditions	Min	Тур	Max	Omt
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time				10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	· · · · · · · · · · · · · · · · · · ·			26	ns
t _{PHL}	output propagation time $(\overline{D0} \sim \overline{D7} - \overline{A0} \sim \overline{A2})$		[26	. ns
t _{PLH}	Low-level to high-level and high-level to low-level	7			28	ns
t _{PHL}	output propagation time (D0~D7 - E0, GS)	0 = 15=5 (N=== 4)			28	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = 15pF (Note 4)			20	ns
t _{PHL}	output propagation time $(\overline{E} - \overline{E0})$				20	ns
t _{PLH}	Low-level to high-level and high-level to low-level				20	ns
t _{PHL}	output propagation time (E - GS)				20	ns
t _{PLH}	Low-level to high-level and high-level to low-level	7			21	ns
t _{PHL}	output propagation time (E - A0~A2)				21	ns

M74HC148P/FP/DP

8-LINE TO 3-LINE PRIORITY ENCODER

SWITCHING CHARACTERISTICS ($V_{cc} = 2\sim 6V$, $T_a = -40\sim +85^{\circ}C$)

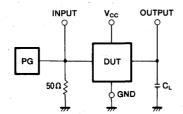
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	and the second of the second o	·				Limits			
Symbol	Parameter	Test conditions			25℃		−40 ~	+85°C	Unit
			V _{CC} (V)	Min	Тур	Max	Min	Max	
			2.0			75		95	į.
t _{TLH}	Low-level to high-level and		4.5			15		.19	ns
	high lovel to law lovel		6.0			13	·	16	
	high-level to low-level		2. 0			75		95	
t _{THL}	output transition time		4.5		-	15		19	ns
			6.0			13		16	
			2.0			150		190	
t _{PLH}	Low-level to high-level and		4.5			30		- 38	ns
	high-level to low-level		6.0			26		33	
	output propagation time		2. 0			150		190	
t _{PHL}	$(\overline{D0} \sim \overline{D7} - \overline{A0} \sim \overline{A2})$		4, 5			30	ļ	38	ns
			6.0			26		33	
	14. S	1	2.0			165		205	
t _{PLH}	Low-level to high-level and		4.5			33		41	ns
	high-level to low-level		6.0			28		35	
	output propagation time		2. 0			165		205	
t _{PHL}	(D0 ∼ D7 − E0 , GS)		4.5			33	}	41	ns
		50-5 (11-1-4)	6.0	-		28		35	
		C _L = 50pF (Note 4)	2.0			120		150	
t _{PLH}	Low-level to high-level and		4.5			24		30	ns
	high-level to low-level		6.0			20		26	
	output propagation time		2.0			120		150	
t _{PHL}	$(\overline{E} - \overline{E0})$		4.5	1		24		30	ns
			6. 0			20		26	
		1	2.0			115		145	
t _{PLH}	Low-level to high-level and		4.5			23		29	ns
	high-level to low-level		6.0			20		25	
	output propagation time		2.0			115		145	
t _{PHL}	$(\overline{E} - \overline{GS})$		4.5			23		29	ns
			6.0			20		25	
		1	2. 0			125		155	
t _{PLH}	Low-level to high-level and		4.5			25		31	ns
	high-level to low-level		6.0			21		26	
	output propagation time		2.0			125		155	
t _{PHL}	$(\overline{E} - \overline{A0} \sim \overline{A2})$		4.5			25		31	ns
			6.0	an ar a		21		26	
Cı	Input capacitance					10		10	pF
C _{PD}	Power dissipation capacitance (Note 3)					†		<u> </u>	pF

Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$

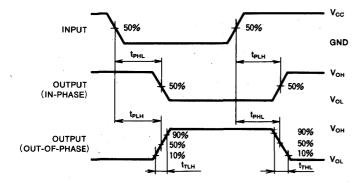
8-LINE TO 3-LINE PRIORITY ENCODER

Note 4: Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_f = 6ns, t_f = 6ns
 (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



M74HC151P/FP/DP

8-INPUT DATA SELECTOR/MULTIPLEXER

DESCRIPTION

The M74HC151 is a semiconductor integrated circuit consisting of an 8-line to 1-line date selector/multiplexer.

FEATURES

High-speed: 22ns typ. (C_L=15pF, V_{CC}=5V)

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- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide supply voltage range: V_{CC}=2∼6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

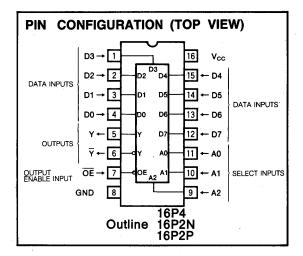
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC151 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS151.

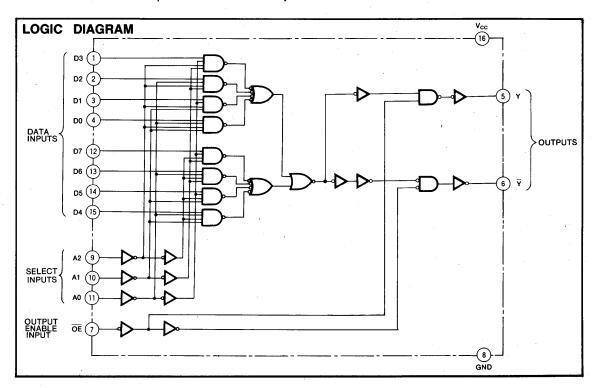
The M74HC151 consists of data selector functions for selecting one of eigh input line signals and multiplexer functions for converting 8-bit parallel data into serial data using time-division.

The 8-line signal is applied to data inputs D0 through D7, and after one of the data inputs has been selected by



select inputs A0 through A2, that input signal will be output at Y or an inverted signal will be output at \overline{Y} . By applying 8-bit parallel data to D0 through D7, and connecting the output of a synchronous octal counter to A0 through A2, D0 through D7 data will be output at Y synchronous with the clock pulse in the order of D0-D7. When output-enable input \overline{OE} is high, Y will become low and \overline{Y} will become high irrespective of other inputs.

The M74HC151 has the same functions and pin connections as the M74HC251, but the latter has a 3-state output.



FUNCTION TABLE (Note 1)

					Inp	uts						Out	puts
A2	A1	. A0	ŌĒ	D0	D1	D2	D3	D4	D5	D6	D7	Ÿ	Y
X	Х	X	Н	X	Х	· X	Х	X	Х	X	х	L	Н
L	L	L	L	L	Х	X	Х	Х	X	Х	Х	L	Н
L	L	L	L	н	Х	×	Х	Х	Х	Х	Х	н	L
L	L	н	L	Х	L	Х	Х	Х	X	. X	X	L	н
L	L	Ή	L	Х	H	Х	X	Х	X	Х	X	Н	L
L	Н	L	L	Х	Х	L	X	Х	, X	X	Х	L	H
L	Н	· L	L	Х	Х	н	Х	Х	Х	Х	Х	H	L
L	Н	Н	ı,	Х	Х	Х	L	Х	Х	Х	Х	L	Н
L	Н	Н	٦	Х	Х	X	Н	Х	Х	Х	Х	Н	L
Н	L	L	L	Х	Х	х	Х	L	X	Х	- , X	L	н
Н	L	L	Γ.	X	Х	X ?	Х	Н	Х	Х	Х	Н	L
Н	L	Н	٦	X	Х	Х	X	х	L	Х	Х	L	Н
Н	L	Н	L	Х	Х	х	X	х	Н	х	Х	Н	L
Н	н	L	L	Х	Х	Х	Х	Х	Х	L	Х	L	Н
Н	н	L	L	Х	X	χ.	Х	Х	Х	Н	Х	н	L
н	Н	Н	L .	х	Х	х	Х	X	Х	Х	L	L	Н
Н	Н	н	Ŀ	Х	Х	X	Х	Х	Х	Х	Н	Н	L

Note 1 : X: Irrelevant

ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
V _I	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
	land and alice discussion	V ₁ < 0V	-20	
I _{IK}	Input protection diode current	$V_1 > V_{CC}$	20	mA
	Output persolate diede aurent	V ₀ < 0V	-20	
Іок	Output parasitic diode current	$V_{o} > V_{cc}$	20	mA.
l _o	Output current per output pin		±25	mA
Icc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		-65∼+150	င

Note 2 : M74HC151FP, T $_{\rm a}$ = $-40\sim+70^{\circ}$ C and T $_{\rm a}$ = $70\sim85^{\circ}$ C are derated at -6mW/°C. M74HC151DP, T $_{\rm a}$ = $-40\sim+50^{\circ}$ C and T $_{\rm a}$ = $50\sim85^{\circ}$ C are derated at -5mW/°C.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85^{\circ}C)$

Symbol	, Do	rameter	L	Limits					
Symbol	Pai	ameter	Min	Тур	Max	Unit			
Vcc	Supply voltage		2		6	٧			
V _i	Input voltage		0		Vcc	٧			
V _o	Output voltage		. 0		Vcc	٧			
Topr	Operating temperature ra	inge	-40		+85	°C			
		$V_{CC} = 2.0V$	0	,,,,,	1000				
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ņs			
		$V_{CC} = 6.0V$. 0		400				

ELECTRICAL CHARACTERISTICS

	The state of the s						Limits			
Symbol	Parameter	Test	conditions			. 25℃		-40~	+85℃	Unit
				V _{cc} (V)	Min	Тур	Max	Min	Max	
		$V_{\rm O} = 0.1 V, \ V_{\rm CO}$	-0.17	2.0	1.5			1.5		
ViH	High-level input voltage	$ I_0 = 20\mu A$		4.5	3.15			3. 15		V
		101 - 20μΑ		6.0	4.2			4.2		
		$V_0 = 0.1V, V_{CC}$	0.17	2.0			0.5		0.5	
V _{IL}	Low-level input voltage	$ V_0 - 0.1V, V_{CO} $ $ I_0 = 20\mu A$	5—0.1 V	4.5			1.35		1.35	V
		$ I_0 = 20\mu A$		6.0			1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
			$I_{OH} = -20\mu A$	4.5	4.4			4.4		
V _{OH}	High-level output voltage	$V_I = V_{IH}, \ V_{IL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		V
			$I_{OH} = -4.0 \text{mA}$	4.5	4. 18			4.13		
			$I_{OH} = -5.2 \text{mA}$	6.0	5.68			5.63		
	-		$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
		,	$I_{OL} = 20 \mu A$	4.5			0.1		0, 1	
VoL	Low-level output voltage	$V_I = V_{IH}, V_{IL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
			I _{OL} = 4.0mA	4.5			0. 26		0.33	
			$I_{OL} = 5.2 mA$	6.0			0. 26		0.33	
I _{IH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μА
I _{IL}	Low-level input current	V ₁ = 0V		6.0			-0.1	,	-1.0	μA
Icc	Quiescent supply current	VI = VCC, GND	$I_0 = 0 \mu A$	6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS $(v_{cc} = 5v, T_a = 25\%)$

Symbol	Parameter	Test conditions		Limits		Unit
Symbol	Parameter	Test conditions	Min	Тур	Max	Ullit
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time				10	ns
t _{PLH}	Low-level to high-level and high-level to low-level				29	ns
t _{PHL}	output propagation time (D — Y)				29	ns
· t _{PLH}	Low-level to high-level and high-level to low-level				32	ns
t _{PHL}	output propagation time $(D - \overline{Y})$				32	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C ₁ = 15pF (Note 4)			43	ns
t _{PHL}	output propagation time (A — Y)	CL — 15pF (Note 4)			43	ns
t _{PLH}	Low-level to high-level and high-level to low-level				35	ns
t _{PHL}	output propagation time $(A - \overline{Y})$	•			35	ns
t _{PLH}	Low-level to high-level and high-level to low-level				23	ns
t _{PHL}	output propagation time (OE - Y)				23	ns
t _{PLH}	Low-level to high-level and high-level to low-level				21	ns
t _{PHL}	output propagation time $(\overline{\sf OE} - \overline{\sf Y})$	-			21	ns

SWITCHING CHARACTERISTICS $(v_{cc} = 2\sim6v, \tau_a = -40\sim+85^{\circ}C)$

Comme to and	B	Took conditions			25°C		40-	+85°C	Uni
Symbol	Parameter	Test conditions							Gill
	<u> </u>		V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0			75		95	
t _{TLH}	Low-level to high-level and		4.5			15		19	ns
			6.0			13		16	}
	high-level to low-level		2.0			75		95	
+	output transition time		4.5	[15		19	ns
t _{THL}	output transition time		1			13		16	"
	 	•	6.0						ļ
		*	2.0			195		244	l
t _{PLH}	Low-level to high-level and		4.5			39		49	ns
	high-level to low-level		6.0			- 33		41	
	output propagation time		2.0			195		244	
t _{PHL}	(D-Y)		4.5			39		49	ns
			6.0			33		41	
	 	·	2.0			185		231	
	Law laws to black to the d	,	I						
t _{PLH}	Low-level to high-level and		4.5			37		46	ns
	high-level to low-level		6.0			32		40	
	output propagation time		2.0			185		231	
t _{PHL}	$(D-\overline{Y})$		4.5			37		46	ns
7			6.0			32		40	
		1	2.0			250		312	
•	Low-level to high-level and	1	4.5			50		63	ns
t _{PLH}		ŀ	1					54	118
	high-level to low-level	C _L = 50pF (Note 4)	6.0			43			<u> </u>
	output propagation time		2.0			250	İ	312	
t _{PHL}	(A - Y)		4.5			50		63	ne
			6.0			43		54	
-			2.0			205		256	
t _{PLH}	Low-level to high-level and		4.5	· i		41		51	ns
	high-level to low-level		6.0	ì ì		35	···	44	
	⊣		2.0			205		256	┼─
	output propagation time	·	1						
t _{PHL}	$(A - \overline{Y})$		4.5			41		51	ns
			6.0			35		44	
	,		2.0			140		175	
t _{PLH}	Low-level to high-level and	\	4.5	1		28	Ì	35	ns
	high-level to low-level	t .	6.0			24		30	1
	output propagation time		2.0			140		175	
t _{PHL}	(OE - Y)	1	4.5			28	1	35	n:
*PHL	102 17		6.0			24		30	"
	1.	-					 	+	+
	1:		2.0			127	1	159]
t _{PLH}	Low-level to high-level and		4.5			25	İ	32	, na
	high-level to low-level		6.0			22		28	
	output propagation time	1	2.0			127		159	
t _{PHL}	$(\overline{OE} - \overline{Y})$	· ·	4.5			25		32	n
			6.0			22		28	
Cı	Input capacitance		+			10	 	10	р
	input capacitation	1	1			1 10	1	1 10	l bi

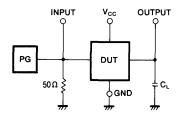
Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.

The power dissipated during operation under no-load conditions is calculated using the following formula:

P_D = C_{PD} · V_{CC}² · f₁+I_{CC} · V_{CC}

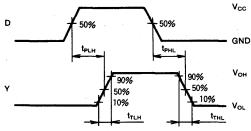


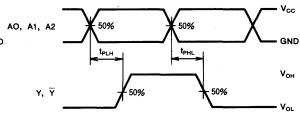
Note 4: Test Circuit

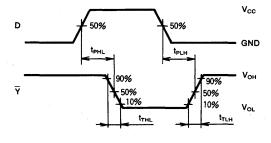


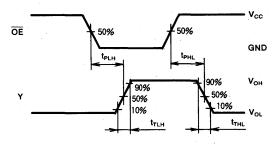
- (1) The pulse generator (PG) has the following characteristics (10%~90%): $\rm t_f=6ns, \, t_f=6ns$
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

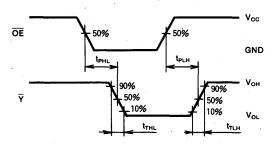
TIMING DIAGRAM











M74HC153P/FP/DP

DUAL 4-INPUT DATA SELECTOR/MULTIPLEXER

DESCRIPTION

The M74HC153 is a semiconductor integrated circuit consisting of two 4-line to 1-line data selectors/multiplexers.

FEATURES

- High-speed: 13ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5, 6V)
- Capable of driving 10 74LSTTL loads
- Wide supply voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=-40~+85℃

APPLICATION

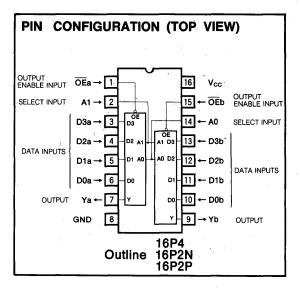
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

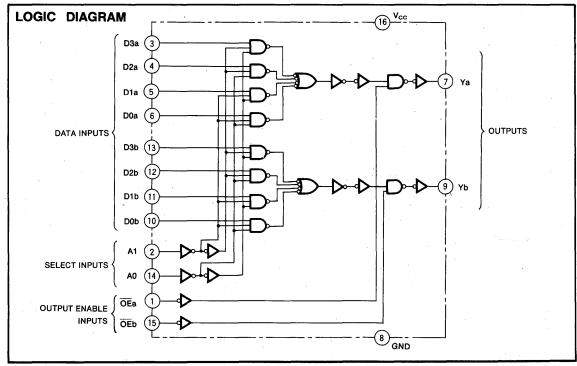
Use of silicon gate technology allows the M74HC153 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS153.

The M74HC153 consists of data selector functions for selecting one of four input line signals and multiplex functions for converting 4-bit parallel data into serial data using time-division.

The 4-line signal is applied to data inputs D0 through D7, and after one of the data inputs has been selected by select inputs A0 and A1, that input signal will be output at



Y. By applying 4-bit parallel data to D0 through D3 and connecting the output of a synchronous quadruple counter to A0 and A1, D0 through D3 data will be output at Y synchronous with the clock pulse in the order of D0-D3. Select inputs A are common to the two circuits while the outputenable inputs \overline{OE} are independent. When \overline{OE} is high, Y will become low irrespective of other inputs.





FUNCTION TABLE (Note 1)

			Inputs				Output
A1	A0	D0	D1	D2	D3	OE	Υ
Х	X	Х	Х	Х	Х	Н	L
L	L	L	Х	Х	X	L	L
L	L	Н	х	×	Х	L	н
L	Н	Х	L	X	х	L	L
L	Н	х	Н	х	X	L	Н
Н	L	Х	х	L	х	L	L
Н	L	Х	Х	Н	х	L	н
Н	Н	х	х	X	L	L	L,
, н	н	Х	х	Х	Н	L	Н

Note 1: X: Irrelevant

ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85 \degree$ C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage		-0.5~+7.0	٧.
V _I	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	·V
		V ₁ < 0V	-20	
l _{IK}	Input protection diode current	V _I > V _{CC}	20	mA
	Out-of-consists dis-d-	V ₀ < 0V	-20	
lok	Output parasitic diode current	Vo > Vcc	20	mA
lo	Output current per output pin		±25	mA
Icc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		-65~+150	°C

Note 2 : M74HC153FP, T $_a$ = $-40\sim+70^\circ$ C and T $_a$ = $70\sim85^\circ$ C are derated at -6mW/°C. M74HC153DP, T $_a$ = $-40\sim+50^\circ$ C and T $_a$ = $50\sim85^\circ$ C are derated at -5mW/°C.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85 ^{\circ}C)$

O				Limits		11-14
Symbol	Pai	rameter	Min	Тур	Max	Unit
Vcc	Supply voltage		2		6	V
V _I	Input voltage		0		Vcc	٧
Vo	Output voltage		0		Vcc	V
Topr	Operating temperature ra	inge	-40		+85	ဗ
		V _{CC} = 2.0V	0		1000	
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns
		$V_{CC} = 6.0V$	0		400	1

ELECTRICAL CHARACTERISTICS

							Limits			
Symbol	Parameter	Test	conditions			25℃		-40~	+85℃	Unit -
	· ·			V _{cc} (V)	Min	Тур	Max	Min	Max	
		Vo = 0.1V, Voc	0.11/	2.0	1.5			1.5		
V _{IH}	High-level input voltage	$ V_0 = 0.1V, V_{CO}$	5-0.1 V	4.5	3.15			3.15		v
		$ 1_0 = 20\mu\text{A}$	* .	6.0	4. 2			4.2		
		$V_0 = 0.1V, V_{CC}$	_0.1v	2.0			0.5		0.5	
VIL	Low-level input voltage	$ I_0 = 20\mu A$	5—0.1 v	4.5			1.35		1.35	V
		1101 - 20µA		6.0			1.8		1.8	
1			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
			$I_{OH} = -20\mu A$	4.5	4. 4			4.4		
V _{OH}	High-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		V
			$I_{OH} = -4.0 \text{mA}$	4.5	4.18			4. 13		
			$I_{OH} = -5.2 \text{mA}$	6.0	5.68			5. 63		
	·		$I_{OL} = 20 \mu A$	2, 0			0.1		0.1	
			$I_{OL} = 20 \mu A$	4.5		ľ .	0.1		0.1	
VoL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1	N. 186 1 . 1	0.1	, V
			I _{OL} = 4.0mA	4.5			0. 26	10 11 92	0.33	
			$I_{OL} = 5.2 mA$	6.0			0.26	-1	0.33	
I _{IH} .	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μA
I _{IL}	Low-level input current	V ₁ = 0V		6.0			-0.1		-1.0	μA
Icc	Quiescent supply current	VI = VCC, GND	$I_0 = 0 \mu A$	6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS $(V_{cc} = 5V, T_a = 25^{\circ})$

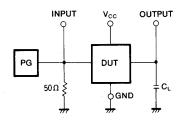
Symbol	Parameter	Test conditions		Limits		Unit
Symbol	Falameter	rest conditions	Min	Тур	Max	Unit
t _{TLH}	Low-level to high-level and high-level to low-level		. ,		10	ns
t _{THL}	output transition time				10	ns
t _{PLH}	Low-level to high-level and high-level to low-level				23	ns
t _{PHL}	output propagation time (D — Y)	0 = 15-5 (Nov. 4)			23	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = 15pF (Note 4)			30	ns
t _{PHL}	output propagation time (A — Y)				30	ns
t _{PLH}	Low-level to high-level and high-level to low-level				. 15	ns
t _{PHL}	output propagation time (OE - Y)				15	ns

SWITCHING CHARACTERISTICS ($v_{cc} = 2\sim 6V$, $T_a = -40\sim +85^{\circ}C$)

						Limits			
Symbol	Parameter	Test conditions			25℃		−40 ~	+85°C	Unit
			V _{CC} (V)	Min	Тур	Max	Min	Max	
			2.0			75		95	
t _{TLH}	Low-level to high-level and		4.5			15	ĺ	19	ns
	high-level to low-level		6.0			13		16	
	might-level to low-level		2.0			75		95	
t _{THL}	output transition time		4.5			15		19	ns
			6.0			13		16	
			2.0			126		158	
t _{PLH}	Low-level to high-level and		4.5			28		35	ns
	high-level to low-level		6.0			23		29	
	output propagation time		2. 0			126	Ĭ .	158	
t _{PHL}	(D - Y)		4.5			28	1	35	ns
		$C_1 = 50 pF \text{ (Note 4)}$	6.0			23		29	
		C _L = 50pr (Note 4)	2.0			158		198	
t _{PLH}	Low-level to high-level and		4.5	X		35		44	ns
	high-level to low-level		6.0	,		30	1	38	
	output propagation time		2.0			158		198	
tent	(A — Y)	,	4.5			35	İ	44	ns
			6.0			30		38	
			2.0			95		120	
t _{PLH}	Low-level to high-level and	,	4.5		:	19		24	ns
	high-level to low-level		6.0			16		20	
	output propagation time		2.0			95		120	
t _{PHL}	$(\overline{OE} - Y)$		4.5			19		.24	ns
-			6.0			16		20	
Cı	Input capacitance					10		10	pF
C _{PD}	Power dissipation capacitance (Note 3)				48				pF

Note 3: CPD is the internal capacitance of the IC caluculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following iormula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$

Note 4: Test Circuit

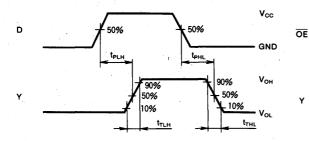


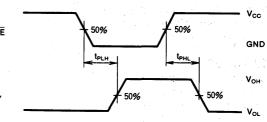
- (1) The pulse generator (PG) has the following
- characteristics (10%~90%): t_f = 6ns, t_f = 6ns (2) The capacitance C_L: includes stray wiring capacitance and the probe input capacitance.

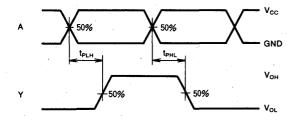
M74HC153P/FP/DP

DUAL 4-INPUT DATA SELECTOR/MULTIPLEXER

TIMING DIAGRAM









MITSUBISHI HIGH SPEED CMOS

M74HC154P/FP/DWP

1-OF-16 DECODER/DEMULTIPLEXER

DESCRIPTION

The M74HC154 is a semiconductor integrated circuit consisting of a 4-bit binary to 16-line decoder/demultiplexer with chip select inputs.

FEATURES

- Two chip select inputs
- High-speed: 21ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: Ta=−40~+85°C

APPLICATION

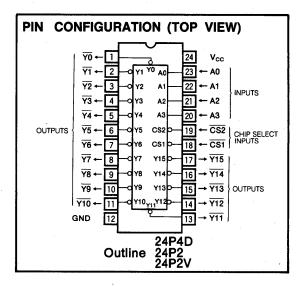
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC154 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS154.

When operated as a 1-of-16 decoder, by applying a 4-bit binary code to inputs A0 through A3, the corresponding output. $\overline{Y0}$ through $\overline{Y15}$ will become low and all the others will become high.

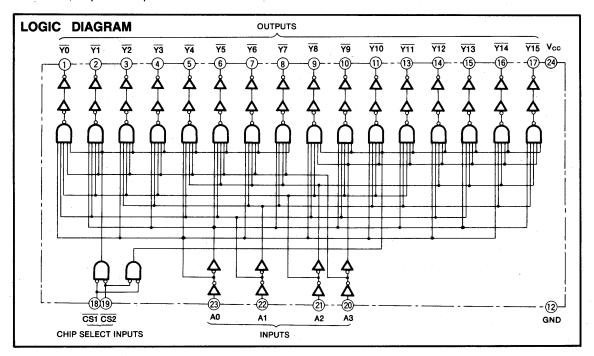
In this case, chip select inputs $\overline{\text{CS1}}$ and $\overline{\text{CS2}}$ should be



maintained low

When both $\overline{CS1}$ and $\overline{CS2}$ are not low, all outputs will become high irrespective of A0 through A3.

When operated as a 1-of-16 demultiplexer, $\overline{\text{CS1}}$ or $\overline{\text{CS2}}$ is used as a data input and A0 through A3 are used as selecting inputs.



1-OF-16 DECODER/DEMULTIPLEXER

FUNCTION TABLE (Note 1)

		Inp	uts										Out	puts							
CS1	CS2	АЗ	A2	A1	A0	ΥO	Y1	Y2	Y3	Y4	Y5	Y6	Y7 .	¥8	<u>79</u>	Y10	Y11	Y12	Y13	Y14	Y15
L	L	L	Ļ	Ĺ	L	Ļ.,	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	H	Н	H
L	L	L	Ĺ	L	Н	Ι	L	Н	Н	Н	Н	Н	Н	Н	['] H	Н	Н	Н	Н	Н	Н
L	L	L	L	Н	L	H	Η	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Ή	Н
L	L.	L	J	Ι	Н	Ξ	Ι	Н	L	H	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	H
L	L	L	I	٦	L	Н	Н	Н	Н	L	Н	Н	Н	· H	Н	Н	Н	H	Н	Η	H
L	L	L.	Ι	L	H	Η	Η	Н	Н	Н	L	Ι	H	Н	Η	Н	Н	Н	Н	Н	Н
L.	L	L	Ħ	Н	L	Н	Н	Н	Н	Н	Н	L	Н	·H	Н	Н	Н	Н	Н	I	H
L	L	L	Н	н	н	Н	Н	Н	н	Н	Н	Н	L	Н	Ξ	н	Н	Н	н	Н	Н
L	L	Н	·L	L	L	Н	Η	Н	Н	Н	Н	Н	Н	L	Н	Н	Н	Н	Н	Н	Н
L	L,	Н	١	L	Н	H	Н	н	Н	Н	н	Н	Н	Н	L	Н	Н	Н	H	Н	Н
L	L	Н	L	Ή,	L	Н	н	н	Н	Н	Н	H	H	Н	Н	L	Н	Н	Н	Н	Н
L	L	Н	L.	н	н	н	н	н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	Н	H	Н
L	L	Н	Н	L	L	Н	· H	Н	Н	н	Н	Н	Н	Н	Н	Н	Н	Ŀ	· H	Н	Н
L	L	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	н	Н	н	Н	H	Н	L	Н	H
L	L	Н	Н	Η.	L	Н	н	Н	Н	Н	н	Н	H	Н	Н	Н	, н	Н	н	L	Н
L	L	Н	ŀН	H.	н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	H	Н	H	Н	Η	L
L	н	Х	Х	Х	Х	Н	н	Н	н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
Н	L	Х	Х	Х	Х	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	H	Н	Н	Н	Н
H	Н	Х	X	X .	Х	Н	Н	Н	Н	н	н	Н	Н	Н	Н	H	Н	Н	Н	Н	Н

Note 1: X: Irrelevant

ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85 \degree$ C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit	
Vcc	Supply voltage		-0.5~+7.0	V	
Vı	Input voltage		-0.5~V _{cc} +0.5	V	
Vo	Output voltage		-0.5~V _{cc} +0.5	٧.	
	India and add all and annual	V ₁ < 0V	-20	4	
lik	Input protection diode current	$V_1 > V_{CC}$	20	mA	
		V ₀ < 0V	-20		
lok	Output parasitic diode current	V _o > V _{cc}	20	mA	
lo	Output current per output pin		±25	mA	
Icc	Supply/GND current	V _{CC} , GND	±50	mA	
Pd	Power dissipation	(Note 2)	500	mW	
Tstg	Storage temperature range		−65∼+150	င	

Note 2 : M74HC154FP, $T_a=-40\sim+80^\circ\text{C}$ and $T_a=80\sim85^\circ\text{C}$ are derated at -7mW/°C . M74HC154DWP, $T_a=-40\sim+80^\circ\text{C}$ and $T_a=80\sim85^\circ\text{C}$ are derated at -7mW/°C .

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85 ^{\circ}C)$

Comple ed	n	<u> </u>		Limits		
Symbol	Pa	ameter	Min	Тур	Max	Unit
Vcc	Supply voltage		2		6	V.
Vı	Input voltage		0		Vcc	V
Vo	Output voltage		0		Vcc	٧
Topr	Operating temperature ra	inge	-40		+85	င
		V _{CC} = 2.0V	0		1000	
tr, tf	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns
	V _{CC} = 6.0V		0		400	

1-OF-16 DECODER/DEMULTIPLEXER

ELECTRICAL CHARACTERISTICS

							I			
Symbol	Parameter	Test	conditions			25℃		-40~	+85℃	Unit
				V _{CC} (V)	Min	Тур	Max	Min	Max	1
		$V_{\rm O} = 0.1 V, V_{\rm CO}$	_0.11/	2.0	1.5			1.5		
VIH	High-level input voltage	$ I_0 = 20\mu A$	5—0. 1 v	4.5	3.15			3, 15		V
	1,	1101 - 20μΑ	101 2007		4.2			4.2		
		$V_0 = 0.1V, V_{CC}$	_0 1V	2.0	7.3000		0.5		0.5	
VIL.	Low-level input voltage	$ V_0 = 0.1V, V_{CO}$ $ I_0 = 20\mu A$	5—0. 1 v	4.5			1.35		1.35	V
		1101 - 20µA		6.0			1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
	High-level output voltage		$I_{OH} = -20\mu A$	4.5	4.4			4.4		
VoH		$V_i = V_{iH}, \ V_{iL}$	$I_{OH} = -20\mu A$	6.0	5. 9			5.9		v
			$I_{OH} = -4.0 \text{mA}$	4.5	4.18			4. 13		
	1		$I_{OH} = -5.2 mA$	6.0	5. 68			5.63		
			$I_{OL} = 20\mu A$	2.0			0, 1		0.1	
			I _{OL} = 20μA	4.5			0.1	}	0.1	
VoL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
			I _{OL} = 4.0mA	4.5			0. 26		0.33	
		1	I _{OL} = 5. 2mA	6.0			0.26		0.33	
I _{IH}	High-level input current	V _I = 6V		6.0			0.1		1.0	μA
l _{IL}	low-level input current	V ₁ = 0V	$V_1 = 0V$				-0.1		-1.0	μА
Icc	Quiescent supply current	VI = VCC, GND	$I_0 = 0 \mu A$	6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS ($v_{cc} = 5v$, $\tau_a = 25^{\circ}C$)

Symbol	Down-r-to-	T4		Limits				
Symbol	Parameter	Test conditions	Min	Тур	Max 10 10 32 32 32	Unit		
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns		
t _{THL}	output transition time				10	ns		
t _{PLH}	Low-level to high-level and high-level to low-level	0 = 15-5 (N-4-4)	1		32	ns		
t _{PHL}	output propagation time $(A - \overline{Y})$	C _L = 15pF (Note 4)			32	ns		
t _{PLH}	Low-level to high-level and high-level to low-level		-		32	ns		
t _{PHL}	output propagation time (CS1, CS2 - Y)				32	ns		

SWITCHING CHARACTERISTICS $(v_{cc} = 2\sim6V, T_a = -40\sim+85\%)$

	·			Limits					
Symbol	Parameter	Test conditions	Test conditions V _{CC} (V)		25℃			-40~+85°C	
		·			Тур	Max	Min	Max	1
·			2.0			75		95	1
tTLH	Low-level to high-level and	•	4.5			15		19	ns
	high lavel & lave lavel		6.0			13		16	
	high-level to low-level	and the second second	2.0			75		95	
t _{THL}	output transition time		4.5			15		19	ns
			6.0			13		16	
			2.0			160		190	
t _{PLH}	Low-level to high-level and		4.5			36		42	ns
	high-level to low-level	C _L = 50pF (Note 4)	6.0			30		35	
	output propagation time	CL — SUPF (Note 4)	2. 0			160		190	
t _{PHL}	$(A - \overline{Y})$		4.5		İ	36	!	42	ns
			_6.0			30		35	
		-	2.0			160		190	
t _{PLH}	Low-level to high-level and		4.5			36		42	ns
	high-level to low-level		6.0			30		35	<u> </u>
	output propagation time		2.0			160		190	1
t _{PHL}	$(\overline{CS1}, \overline{CS2} - \overline{Y})$		4.5			36		42	ns
			6.0			30		35	
Cı	Input capacitance					10		10	pF
CPD	Power dissipation capacitance (Note 3)								pF

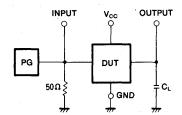
Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.

The power dissipated during operation under no-load conditions is calculated using the following formula: P_D = C_{PD} • V_{CC}² • f₁+I_{CC} • V_{CC}



1-OF-16 DECODER/DEMULTIPLEXER

Note 4: Test Circuit



- (1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
 (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.
- TIMING DIAGRAM V_{CC} 50% 50% GND t_{PLH} t_{PHL} Voh <u>Y0</u>~<u>Y15</u> 50% 50% Vol t_{PHL} t_{PLH} 90% 90% Voh <u>70</u>~<u>715</u> 50% 50% 10% 10% V_{OL} t_{TLH} t_{THL} Vcc CS1, CS2 50% 50% GND VoH 50% **Y0~Y15**

M74HC155P/FP/DP

DUAL 1-OF-4 DECODER/DEMULTIPLEXER

DESCRIPTION

The M74HC155 is a semiconductor integrated circuit consisting of two 2-bit binary to 4-line decoders/demultiplexers.

FEATURES

- High-speed: 19ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=-40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

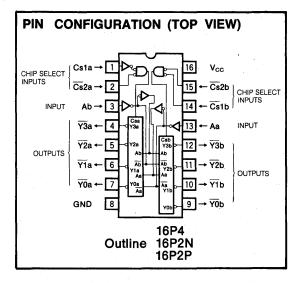
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC155 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS155.

When operated as a 2-bit binary to 4-line decoder, by applying 2-bit binary data to inputs Aa and Ab, the corresponding output $\overline{Y0}$ through $\overline{Y3}$ will become low and all the others will become high.

In this case, chip select inputs $\overline{Cs}1a$ and $\overline{Cs}1b$ should be maintained at high and low respectively, and chip select inputs $\overline{Cs}2a$ and $\overline{Cs}2b$ should be maintained low.

When both Cs2a and Cs2b are high, all the outputs will be-



come high.

When operated as a 3-bit binary to 8-line decoder, by applying 3rd-bit binary data to connected Cs1a and $\overline{\text{Cs}}2\text{b}$, the output signals will appear at $\overline{\text{Y0}}\text{b}$ through $\overline{\text{Y3}}\text{b}$ and $\overline{\text{Y0}}\text{a}$ through $\overline{\text{Y3}}$ a in accordance with the function table given.

When operated as a 1-of-4 demultiplexer, by using Cs1a and $\overline{\text{Cs}}$ 1b as data inputs, and by using Aa and Ab as select inputs, the output signals will appear at $\overline{\text{Y0}}$ through $\overline{\text{Y3}}$.

When operated as a 1-of-8 demultiplexer, by using connected Cs1a and $\overline{\text{Cs1b}}$ as 3rd-bit select input, and by using connected $\overline{\text{Cs2a}}$ and $\overline{\text{Cs2b}}$ as data input, the output signals will appear at $\overline{\text{Y0b}}$ through $\overline{\text{Y3b}}$ and $\overline{\text{Y0a}}$ through $\overline{\text{Y3a}}$.

FUNCTION TABLE (Note 1)

(2-BIT BINARY TO 4-LINE DECODER/1-LINE TO 4-LINE DEMULTIPLEXER)

	in	outs		Outputs					
Ab	Aà	Cs2a	Cs1a	Y0a	Y1a	Y2a	Y3a		
Х	×	н	Х	Н	Н	Н	Н		
L	L	L	Н	L	Н	Н	Н		
L	Н	L	Н	н	L	Н	Н		
Н	L	L	Н	Н	Н	L	Н		
Н	Н	L	Н	Н	Н	Н	L		
X	х	Х	L	н	Н	Н	Н		

	In	outs			Out	puts	
Ab	Aa	Cs2b	Cs1b	YÖb	Y1b	Y2b	Y3b
·X	X	Н	Х	Н	H	Н	Н
L	L	L	L	L	Н	Н	Н
L	Н	L	L	Ŧ	L	Н	Н
Н	L	L	L	Τ	Η	L	Н
Н	н	L	L	Н	Н	Н	L
X	Х	Х	Н	Н	Н	Н	Н

<3-BIT BINARY TO 8-LINE DECODER/1-LINE TO 8-LINE DEMULTIPLEXER>

	Inp	outs			Outputs								
Ac	Ab	Aa	Cs	₹0b	Y1b	Y2b	Y3b	₹0a	Y1a	Y2a	Y3a		
Х	Х	Х	Н	Н	Н	Н	Н	Н	Н	Н	Н		
L	L	L	L	L	Н	Н	Н	Н	Н	н	H		
L	L.	Н	L	Н	L	Н	Н	Н	Н	Н	Н		
L	Н	L	L	Н	Н	L	Н	Н	Н	Н	Н		
L	Н	Н	L	Н	Н	Н	L	Н	Н	Н	Н		
Н	L	L	L	Н	Н	Н	Н	L	Н	Н	Н		
Н	L	Н	L	H.	Н	Н	Н	Н	L	Н	Н		
Н	Н	L	L	Н	Н	Н	Н	Н	Н	L	Н		
Н	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	L		

Note 1: X : Irrelevant

Ac : Cs1a and Cs1b (when connected)
Cs : Cs2a and Cs2b (when connected)

M74HC157P/FP/DP

QUADRUPLE 2-INPUT NONINVERTING DATA SELECTOR/MULTIPLEXER

DESCRIPTION

The M74HC157 is a semiconductor integrated circuit consisting of four 2-line to 1-line data selectors/multiplexers.

FEATURES

- High-speed: 12ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2∼6V
- Wide operating temperature range: Ta=−40~+85°C

APPLICATION

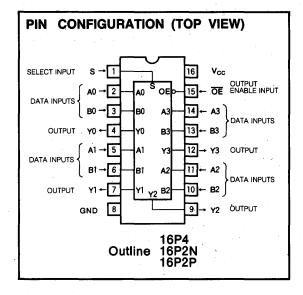
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC157 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS157.

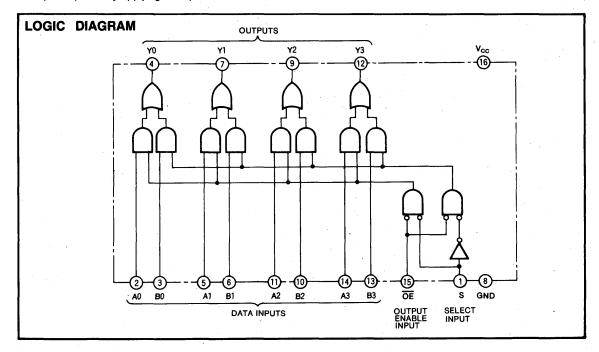
The M74HC157 consists of four circuits each containing data selector functions for selecting one of two input line signals and multiplexer functions for converting 2-bit parallel data into serial data using time-division.

The 2-line signal is applied to data inputs A and B, and after one of the inputs has been selected by select input S, it is output at pin Y. By applying 2-bit parallel data to A and



B, and connecting the output of a binary counter to S, A and B date will be output at Y synchronous with the clock pulse in the order A-B. S and output-enable input \overline{OE} are common to all four circuits. When \overline{OE} is high, all outputs, Y will become low irrespective of other inputs.

M74HC157 is the same functions and pin connections as M74HC257, differing in that the output of M74HC257 is 3-state.





QUADRUPLE 2-INPUT NONINVERTING DATA SELECTOR/MULTIPLEXER

FUNCTION TABLE (Note 1)

	Inp	outs		Output
OE	S	Α	В	Y
Н	×	х	×	L
L	L	L	х.	L
L	L	н	×	н
L	Н	×	L	L
L	Н	X	Н	н

Note 1 : X : Irrelevant

ABSOLUTE MAXIMUM RATINGS $(T_a = -40 \sim +85^{\circ}C)$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
		V ₁ < 0V	-20	
. I _{IK}	Input protection diode current	V _I > V _{CC}	20	mA
	Outrat annulate disease	v _o < 0v	-20	
lok	Output parasitic diode current	V _o > V _{cc}	20	mA
l _o	Output current per output pin		±25	mA
Icc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		-65~+150	င

Note 2 : M74HC157FP, $T_a = -40 \sim +70 ^\circ C$ and $T_a = 70 \sim 85 ^\circ C$ are derated at $-6 mW/^\circ C$. M74HC157DP, $T_a = -40 \sim +50 ^\circ C$ and $T_a = 50 \sim 85 ^\circ C$ are derated at $-5 mW/^\circ C$.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85 \degree C)$

0				Limits		l lada
Symbol	Pa	rameter	Min	Тур	Max	Unit
Vcc	Supply voltage		2		6	V
Vı	Input voltage		0		Vcc	V
Vo	Output voltage		0		V _{CC}	V
Topr	Operating temperature ra	ange	-40		+85	ဗ
		V _{CC} = 2.0V	0		1000	
t _r , t _f	Input risetime, falltime	V _{CC} = 4.5V	0		500	ns
		V _{CC} = 6.0V	0		400]

QUADRUPLE 2-INPUT NONINVERTING DATA SELECTOR/MULTIPLEXER

ELECTRICAL CHARACTERISTICS

					Limits					Unit
Symbol	Parameter	Test	Test conditions $V_{CC}(V)$		25℃			-40~+85℃		
					Min	Тур	Max	Min	Max	
***************************************		$V_0 = 0.1V, V_{CC}$	_0.1v	2, 0	1.5			1.5		
VIH	High-level input voltage	$ V_0 = 0.1V, V_{CO}$	50. T V	4.5	3.15	1		3. 15		V
		1101 - 20µA		6.0	4. 2			4.2		
		$V_{0} = 0.1V, V_{CO}$	_0.1V	2.0			0.5	*	0.5	
V _{IL}	Low-level input voltage	$ V_0 = 0.1V, V_{CO} $ $ I_0 = 20\mu A$	5—0. I V	4.5			1.35		1.35	V
		$ 1_0 = 20\mu\text{A}$		6.0			1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
			$I_{OH} = -20\mu A$	4.5	4.4			4.4		
V _{OH}	High-level output voltage	$V_{l} = V_{lH}, V_{lL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		V
			$I_{OH} = -4.0 mA$	4.5	4.18			4.13		
			$I_{OH} = -5.2 \text{mA}$	6.0	5.68			5.63		
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
			$I_{OL} = 20 \mu A$	4.5			0.1		0.1	
VoL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1	1 1 11	0.1	V
			I _{OL} = 4.0mA	4.5			0.26		0.33	İ
			$I_{OL} = 5.2 \text{mA}$	6.0			0.26		0.33	
I _{IH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μΑ
I _{IL}	Low-level input current	V ₁ = 0V		6.0			—0. 1		-1.0	μΑ
Icc	Quiescent supply current	VI = VCC, GNE	$I_0 = 0 \mu A$	6.0			4.0		40.0	μА

SWITCHING CHARACTERISTICS ($v_{cc} = 5v$, $\tau_a = 25\%$)

Oursell and	Parameter	Test conditions		Limits		Unit
Symbol	Parameter	rest conditions	Min	Тур	Max	Unit
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time				10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	· ·			20	ns
t _{PHL}	output propagation time (A, B — Y)	C _L = 15pF (Note 4)			20	ns
t _{PLH}	Low-level to high-level and high-level to low-level	CL — ISPF (Note 4)			20	ns
t _{PHL}	output propagation time (S - Y)				20	ns
t _{PLH}	Low-level to high-level and high-level to low-level				18	ns
t _{PHL}	output propagation time (OE - Y)			-	18	ns

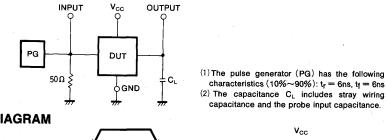
QUADRUPLE 2-INPUT NONINVERTING DATA SELECTOR/MULTIPLEXER

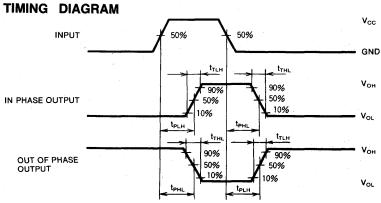
SWITCHING CHARACTERISTICS $(v_{cc} = 2\sim6V, T_a = -40\sim+85^{\circ}C)$

						Limits			
Symbol	Parameter	Test conditions			25℃		−40 ~	+85℃	Unit
_			V _{cc} (V)	Min	Тур	Max	Min	Max	
		*	2.0			75		95	
t _{TLH}	Low-level to high-level and	,	4.5			15		19	ns
	high-level to low-level	·	6.0			13		16	
	Ingri-level to low-level		2.0			75		95	
t _{THL}	output transition time		4. 5			15		19	ns
	<u> </u>	,	6.0			13		16	
			2.0			125		158	
t _{PLH}	Low-level to high-level and		4.5			25		32	ns
	high-level to low-level		6.0			21		27	
	output propagation time		2.0			125		158	
t _{PHL}	(A, B-Y)		4.5			25		32	ns
_		$C_1 = 50 pF \text{ (Note 4)}$	6.0			21		27	
		CL = SOPF (Note 4)	2.0			125		158	
t _{PLH}	Low-level to high-level and		4. 5			25		32	ns
	high-level to low-level		6.0			21		27	
	output propagation time		2.0			125		158	
t _{PHL}	(S-Y)		4.5			25		32	ns
			6.0			21		27	
]	2.0			115		145	
t _{PLH}	Low-level to high-level and		4.5			23		29	· ns
	high-level to low-level		6.0			20		25	
	output propagation time		2.0			115		145	
t _{PHL}	(OE - Y)		4.5	i i		23		29	ns
		·	6.0			20		25	
Cı	Input capacitance					10		10	pF
C _{PD}	Power dissipation capacitance (Note 3)				51				pF

Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipation during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$

Note 4: Test Circuit





M74HC158P/FP/DP

QUADRUPLE 2-INPUT INVERTING DATA SELECTOR MULTIPLEXER

DESCRIPTION

The M74HC158 is a semiconductor integrated circuit consisting of four 2-line to 1-line data selectors/multiplexers.

FEATURES

- High-speed: 12ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=-40~+85℃

APPLICATION

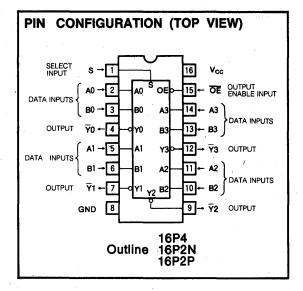
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

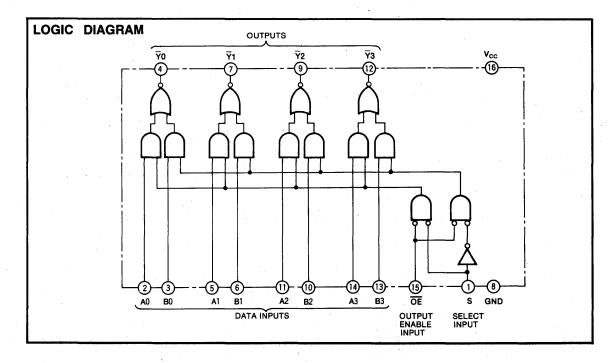
Use of silicon gate technology allows the M74HC158 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS158.

The M74HC158 consists of four circuits each containing date selector functions for selecting one of two input line signals and multiplexer functions for converting 2-bit parallel data into serial data using time-division.

The 2-line signal is applied to data inputs A and B, and after one of the data inputs has been selected by select in-



put S, it is inverted and output at pin \overline{Y} . By applying 2-bit parallel data to A and B, and connecting the output of a binary counter to S, the inverted A and B data will be output at \overline{Y} synchronous with the clock pulse in the order A-B. S and output-enable input \overline{OE} are common to all four circuits. When \overline{OE} is high, all outputs, Y will become high irrespective of other inputs.





QUADRUPLE 2-INPUT INVERTING DATA SELECTOR/MULTIPLEXER

FUNCTION TABLE (Note 1)

	Inp	outs		Output
OE	S	Α	В	Ÿ
н	×	×	Х	Н
L	L	L	Х	Н
L	L	н	Х	L
L	Н	х	L	Н
L	Н	x	Н	L

Note 1 : X : Irrelevant

ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
V _I	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
	l	V _i < 0V	-20	
lik	Input protection diode current	V _I > V _{CC}	20	mA _
	Outside diada	V ₀ < 0V	-20	
Іок	Output parasitic diode current	Vo > Vcc	20	⊢ mA
lo	Output current per output pin		±25	mA
Icc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65~+150	°C

Note 2 : M74HC158FP, T $_{\rm a}=-40\sim+70^{\circ}{\rm C}$ and T $_{\rm a}=70\sim85^{\circ}{\rm C}$ are derated at $-6{\rm mW/C}$. M74HC158DP, T $_{\rm a}=-40\sim+50^{\circ}{\rm C}$ and T $_{\rm a}=50\sim85^{\circ}{\rm C}$ are derated at $-5{\rm mW/C}$.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85 \degree C)$

Cumbal	no.	rameter		Unit		
Symbol	Pa	rameter	Min	Тур	Max	Unit
V _{cc}	Supply voltage		2		6	٧
V _I	Input voltage		0		Vcc	٧
Vo	Output voltage		0		Vcc	٧
Topr	Operating temperature ra	inge	-40	,	+85	Ĵ
		V _{CC} = 2.0V	0		1000	
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns
	'	$V_{CC} = 6.0V$	0		400	

QUADRUPLE 2-INPUT INVERTING DATA SELECTOR/MULTIPLEXER

ELECTRICAL CHARACTERISTICS

							Limits			
Symbol	Parameter	Test	conditions			25℃		-40~	+85℃	Unit
			V _{cc} (V)		Min	Тур	Max	Min	Max	
		V -0.1V V	0.114	2.0	1.5			1.5		
V _{IH}	High-level input voltage		$V_0 = 0.1V, V_{CC} - 0.1V$		3. 15			3. 15		v
		$ I_0 = 20\mu A$		6.0	4.2			4.2		
		V -0.1V V	0.114	2.0			0.5		0.5	
V_{IL}	Low-level input voltage	$V_0 = 0.1V, V_{CC}$	50. TV	4.5			1.35		1.35	V
		$ I_0 = 20\mu A$		6.0			1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
			$I_{OH} = -20\mu A$	4.5	4.4			4.4		
V _{OH}	High-level output voltage	$V_{l} = V_{lH}, V_{lL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		٧
			$I_{OH} = -4.0 mA$	4.5	4.18			4.13		
			$I_{OH} = -5.2 mA$	6.0	5. 68			5.63		
			$I_{OL} = 20 \mu A$	2, 0		-	0.1		0.1	
			$I_{OL} = 20 \mu A$	4.5			0.1		0.1	
VoL	Low-level output voltage	$V_{i} = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
			I _{OL} = 4.0mA	4.5			0.26		0.33	
			I _{OL} = 5. 2mA	6.0			0.26		0.33	
I _{IH}	High-level input current	V ₁ = 6V	-	6.0			0.1		1.0	μΑ
l _{IL}	Low-level input current	V _I = 0V		6.0			-0.1		-1.0	μA
lcc	Quiescent supply current	VI = VCC, GND	$I_0 = 0 \mu A$	6.0			4.0		40.0	μΑ

SWITCHING CHARACTERISTICS ($V_{cc} = 5V$, $T_a = 25^{\circ}C$)

		*		Limits		Unit
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time	,			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level				20	ns
t _{PHL}	output propagation time (A, $B - \overline{Y}$)	$C_1 = 15pF (Note 4)$			20	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = 15pF (Note 4)			20	ns
t _{PHL}	output propagation time (S $-\overline{Y}$)	•			20 ,	ns
t _{PLH}	Low-level to high-level and high-level to low-level				18	ns
t _{PHL}	output propagation time $(\overline{OE} - \overline{Y})$				18	ns

QUADRUPLE 2-INPUT INVERTING DATA SELECTOR/MULTIPLEXER

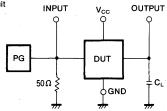
SWITCHING CHARACTERISTICS ($V_{cc} = 2\sim 6V$, $T_a = -40\sim +85^{\circ}C$)

						Limits			
Symbol	Parameter	Test conditions			25℃		−40 ~	+85℃	Uni
		<u> </u>	V _{cc} (V)	Min	Тур	Max	Min	Max	
	-		2.0			75		95	
t _{TLH}	Low-level to high-level and		4.5		İ	-15		19	ns
	hink lavel &s lave lavel		6.0			13		16	
	high-level to low-level		2.0			75		95	
t _{THL}	output transition time		4.5		ł	15		19	ns
			6.0			13		16	
			2. 0			125		158	
t _{PLH}	Low-level to high-level and		4. 5			25		32	ns
	high-level to low-level		6.0			21		27	-
	output propagation time		2.0			125		158	
t _{PHL}	$(A, B-\overline{Y})$		4.5			25		32	ns
		C _L = 50pF (Note 4)	6.0		1	21]	27	
		C _L = SUPF (Note 4)	2.0			125		158	
t _{PLH}	Low-level to high-level and		4.5		•	25		32	ns
	high-level to low-level		6.0			21		27	
	output propagation time		2.0			125		158	
t _{PHL}	$(S-\widetilde{Y})$		4.5			25		32	ns
	*		6.0			21		27	
			2.0			115		145	
t _{PLH}	Low-level to high-level and	1	4.5			23	1	29	ns
	high-level to low-level		6.0			20		25	
,	output propagation time		2.0			115		145	
t _{PHL}	$(\overline{OE} - \overline{Y})$		4.5		İ	23		29	ns
			6.0		1	20		25	
C,	Input capacitance					. 10		10	pF
C _{PD}	Power dissipation capacitance (Note 3)				82				pF

Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.

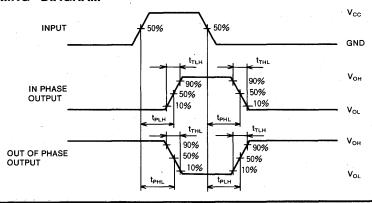
The power dissipation during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$





- (1) The pulse generator (PG) has the following characteristics (10% \sim 90%): $t_r = 6ns$, $t_f = 6ns$
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



M74HC160P/FP/DP

PRESETTABLE BCD COUNTER WITH ASYNCHRONOUS RESET

DESCRIPTION

The M74HC160 is a semiconductor integrated circuit consisting of a presettable synchronous BCD counter with an asynchronous reset input.

FEATURES

- Asynchronous reset and synchronous preset inputs
- Enable input and ripple carry output allow cascade connection
- Count frequency 45MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- Wide supply voltage range: V_{CC}=2∼6V
- Wide operating temperature range: T_a=-40~+85℃

APPLICATION

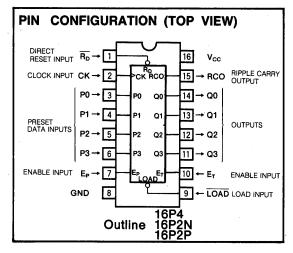
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC160 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS160.

When the count pulse is applied to clock input CK, the number of count pulses will be output at outputs Q0 through Q3 synchronous with the count pulse in BCD code. Counting takes place when CK changes from low-level to high-level.

The preset functions synchronously with the count pulse. By supplying data to preset data inputs P0 through P3 and setting load input $\overline{\text{LOAD}}$ to low-level, when CK changes from

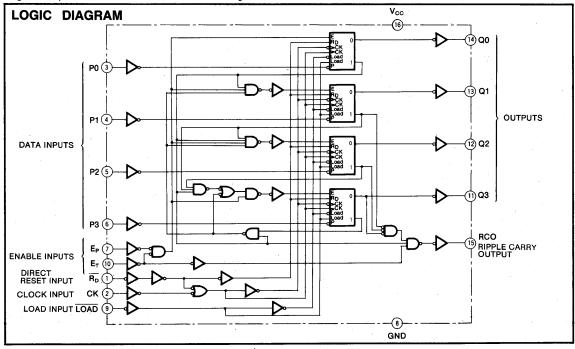


low-level to high-level, the P0 through P3 signals will be output to Q0 through Q3, respectively, irrespective of enable inputs E_{P} and E_{T} . This permits persetting of the counter.

When values greater than 10 are preset, the count advances as shown in the State Transition Diagram.

The reset operates asynchronously, and by setting direct reset input $\overline{R_D}$ to low-level, Q0 through Q3 will become low irrespective of other inputs.

The ripple carry output RCO will become high only when Q0 is high, Q1 is low, Q2 is low, Q3 is high and E_T is high. E_P , E_T and RCO are used in cascade connections of the counter synchronous from when the counter is used as a nbit counter. (See the Application Example.)



FUNCTION TABLE (Note 1)

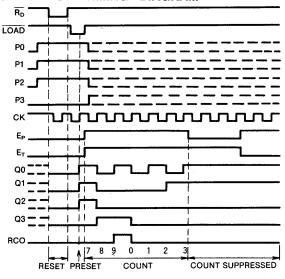
		Inputs			Outputs					
R₀	LOAD	Eτ	E _P	СК	QQ	Q1	Q2	Q3	RCO	
L	X	Х	Х	Х	L	L	L	L	L	
Н	L	L	Х	1	PO	P1	P2	P3	L	
Н	L	Н	х	1	PU	PI	12	P3	L*	
н	н	Н	Н	1	Cou	nt			L*	
Н	н	L	Х	Х	Cou	L				
н	Н	Н	L	X	Cou	nt sup	presse	d	L*	

Note 1: † : Change from low to high (positive-edge trigger)

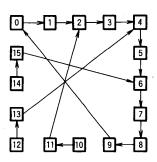
 * : RCQ is normally low, but will become high when Q0 is high, Q1 is low, Q2 is low, Q3 is high and E_T is high. Accordingly RCO = Q0 ⋅ Q1 ⋅ Q2 ⋅ Q3 ⋅ E_T

X: Irrelevant

OPERATION TIMING DIAGRAM



STATE TRANSITION DIAGRAM



ABSOLUTE MAXIMUM RATINGS ($\tau_a = -40 \sim +85$ °C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage	-	-0.5~+7.0	V
Vi	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
		V ₁ < 0V	-20	
l _{IK}	Input protection diode current	$V_{i} > V_{CC}$	20	mA.
		V ₀ < 0V	-20	
lok	Output parasitic diode current	V _o > V _{cc}	20	⊢ mA
Io	Output current per output pin		±25	mA
Icc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		-65~+150	င

Note 2 : M74HC160FP, $T_a = -40 \sim +70 ^{\circ}\text{C}$ and $T_a = 70 \sim 85 ^{\circ}\text{C}$ are derated at -6 mW/°C. M74HC160DP, $T_a = -40 \sim +50 ^{\circ}\text{C}$ and $T_a = 50 \sim 85 ^{\circ}\text{C}$ are derated at -5 mW/°C.

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85\%)$

0		Parameter		Limits				
Symbol	Pai	rameter	Min	Тур	Max	Unit		
V _{CC}	Supply voltage		2		6	٧		
V _I	Input voltage		0		Vcc	٧		
V _o	Output voltage	***	0		Vcc	٧		
Topr	Operating temperature ra	inge	-40		+85	င		
		$V_{CC} = 2.0V$	0		1000			
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns		
		$V_{CC} = 6.0V$	0		400			

ELECTRICAL CHARACTERISTICS

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2. 医电影 (1985年 - 1985年 - 1985年 - 1986年

		Test conditions $V_{CC}(V)$		Limits						
Symbol	Parameter				25℃			-40~+8		Unit
				V _{cc} (V)	Min	Тур	Max	Min	Max	
	High-level input voltage	$V_{O} = 0.1V, V_{CC} = 0.1V$ $ I_{O} = 20\mu A$		2.0	1.5			1.5		
VIH				4.5	3.15			3.15		v
				6.0	4. 2	L		4.2		
		$V_{O} = 0.1V, V_{CC} = 0.1V$ $ I_{O} = 20\mu A$		2.0			0.5		0.5	
VIL	Low-level input voltage			4.5		ļ	1.35		1.35	V
				6.0			1.8		1.8	
	High-level output voltage	$V_i = V_{iH}, \ V_{iL}$	$I_{OH} = -20\mu A$	2.0	1.9			1.9		
			$I_{OH} = -20\mu A$	4.5	4.4			4.4		v
V _{OH}			$I_{OH} = -20\mu A$	6.0	5.9			5.9		
			$I_{OH} = -4.0 \text{mA}$	4.5	4. 18			4.13		
			$I_{OH} = -5.2 \text{mA}$	6.0	5. 68	_		5, 63		
	Low-level output voltage	$V_{l} = V_{lH}, \ V_{lL}$	$I_{OL} = 20 \mu A$	2.0			0.1		.0. 1	
			$I_{OL} = 20 \mu A$	4.5			0.1		0.1	
VoL			$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
			I _{OL} = 4.0mA	4.5	17		0. 26		0.33	
			$I_{OL} = 5.2 mA$	6.0		_	0. 26		0.33	
I _{IH}	High-level input current	V ₁ == 6V		6.0			0.1		1.0	μA
I _{IL}	Low-level input current	$V_1 = 0V$		6.0			-0. 1		-1.0	μA
Icc	Quiescent supply current	VI = VCC, GND	$I_0 = 0 \mu A$	6.0			4.0		40.0	μΑ

SWITCHING CHARACTERISTICS $(v_{cc} = 5v, \tau_a = 25^{\circ}c)$

Symbol	Boyomatay	Test conditions		Limits		
Буппроі	Parameter			Тур	Max	Unit
fmax	Maximum clock frequency		30			MHz
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time				10	ns
t _{PLH}	Low-level to high-level and high-level to low-level				28	ns
t _{PHL}	output propagation time (CK — Q)	C _L = 15pF (Note 4)			34	ns
t _{PHL}	High-level to low-level output propagation time $(\overline{R}_D - Q)$				36	ns
t _{PLH}	Low-level to high-level and high-level to low-level				26	ns
t _{PHL}	output propagation time (E _T — RCO)				32	ns
t _{PLH}	Low-level to high-level and high-level to low-level				30	ns
t _{PHL}	output propagation time (CK — RCO)				36	ns
t _{PHL}	High-level to low-level output propagation time (RD - RCO)				38	ns

SWITCHING CHARACTERISTICS ($v_{cc} = 2\sim6v$, $T_a = -40\sim+85^{\circ}C$)

Symbol	Parameter			Limits					
		Test conditions		25℃			-40~+85°C		Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0	5			4		
fmax	Maximum clock frequency		4.5	27			21		мна
			6.0	32			25		
			2.0			75		95	
t _{TLH}	Low-level to high-level and		4.5			15		19	ns
	high touch a low bound		6.0			13		16	
	high-level to low-level		2.0			75		95	
t _{THL}	output transition time		4.5		İ	15		19	ns
		,	6.0		ļ	13		16	
		1	2.0			170		214	
t _{PLH}	Low-level to high-level and		4.5			34	Ì	43	ns
	high-level to low-level		6.0			29		36	
	output propagation time		2.0			205		258	
t _{PHL}	(CK - Q)		4.5			41		52	ns
			6.0			35		44	
t _{PHL}	High-level to low-level	1	2. 0			210		265	1
	output propagation time	C _L = 50pF (Note 4)	4.5			42		53	ns
	$(\overline{R_D} - Q)$		6.0			36		45	
]	2.0			160		202	
t _{PLH}	Low-level to high-level and		4.5			32		40	ns
	high-level to low-level		6.0			27		34	
	output propagation time		2.0			195		246	
t _{PHL}	(E _T - RCO)		4.5			39		49	ns
	,	· ·	6.0			33		42	
		1	2.0			175		221	
t _{PLH}	Low-level to high-level and		4.5			35		44	ns
	high-level to low-level	` .	6.0			30		37	
t _{PHL}	output propagation time		2.0			215		271	
	(CK - RCO)		4.5			43		54	ns
			6.0			37		46	
t _{PHL}	High-level to low-level	1	2.0			220		277	
	output propagation time		4.5			44		55	ns
	(RD - RCO)		6.0			37		47	
Cı	Input capacitance					10		10	рF
C _{PD}	Power dissipation capacitance (Note 3)				57				pF

Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.

The power dissipated during operation under no-load conditions is calculated using the following formula:

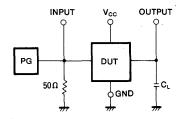
P_D = C_{PD} · V_{CC}² · f₁+I_{CC} · V_{CC}



TIMING REQUIERMENTS ($v_{cc} = 2\sim6v$, $T_a = -40\sim+85$ °C)

Symbol /				Limits					Unit
	Parameter	Test conditions		25℃			-40~+85°C		
			V _{CC} (V)	Min	Тур	Max	Min	Max	
			2.0	80			101		
tw(ck)	Clock pulse width		4.5	16			20		ns
			6.0	14			17		
		·	2.0	80			101		
tw(RD)	Direct reset pulse width		4.5	16			20		ns
-			6.0	14			17		
	P setup time with		2.0	150			189		
t _{SU(P)}	respect to CK		4.5	30		-	38		ns
	respect to CK		6.0	26		\	32	_	Ì
	LOAD setup time with		2.0	135			170		
tsu(LOAD)	respect to CK	•	4.5	27		-	34		ns.
	respect to CK		6.0	23			29		
	E _T , E _P setup time with		2.0	200			250		
t _{su(E)}	respect to CK		4.5	40			50		ns
	respect to CK		6.0	34			43		
	P hold time with		2.0	50			63		
th(P)			4.5	- 10			13		ns
	respect to CK		6.0	9			11		
	LOAD hold time with		2.0	0			0		
th(LOAD)	respect to CK		4.5	0			0		ns
	respect to CK		6.0	0			0		
	E _T , E _P hold time with]	2.0	0			0		
th(E)			4.5	0			0		ns
	respect to CK		6.0	0			0		
	R _D recovery time with		2.0	125			158	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	
trec(RD)			4.5	25			32		ns
	respect to CK	j	6.0	21			27		1
	LOAD recovery time with		2.0	125			158		
trec(LOAD)	respect to CK		4.5	25			32		ns
	respect to CK	· ·	6.0	21			27		

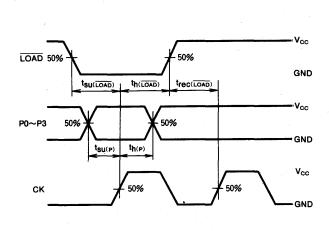
Note 4: Test Circuit

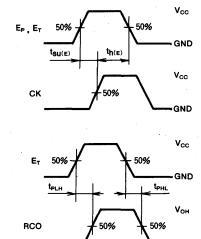


 ⁽¹⁾ The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
 (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM V_{CC} RD 50% GND tw(RD trec(RD) tw(ck) Vcc 50% 50% СК 50% GND t_{PHL} t_{PLH} V_{OH} 90% 90% Q0~Q3 50% 50% 50% RCO 10% 10% VoL

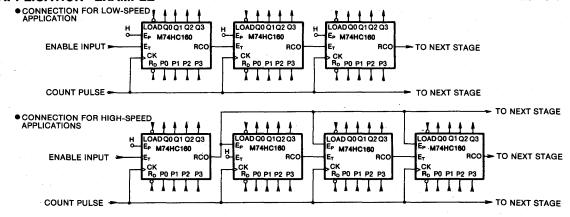
t_{TLH}





t_{THL}

APPLICATION EXAMPLE CONFIGURATION OF A 10" COUNTER USING CASCADE CONNECTION



M74HC161P/FP/DP

PRESETTABLE 4-BIT BINARY COUNTER WITH ASYNCHRONOUS RESET

DESCRIPTION

The M74HC161 is a semiconductor integrated circuit consisting of a presettable synchronous 4-bit binary (hexadecimal) counter with direct reset input.

FEATURES

- Direct reset and synchronous preset inputs
- Enable input and ripple carry output for cascade connection
- Count frequency 45MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=-40~+85℃

APPLICATION

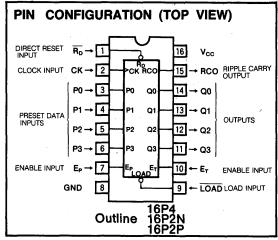
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC161 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS161.

When the count pulse is applied to clock input CK, the number of count pulses will be output at outputs Q0 through Q3 synchronous with the count pulse in 4-bit binary code. Counting takes place when CK changes from low-level to high-level.

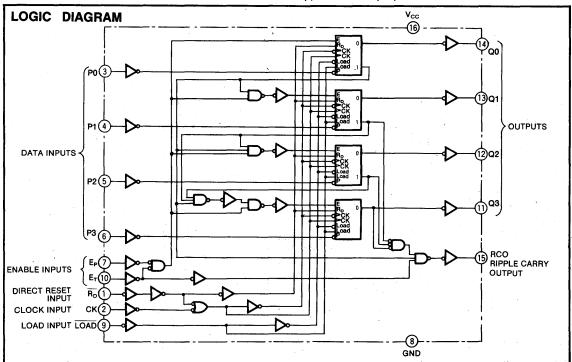
The preset functions synchronously with the count pulse. By



supplying data to PERSET data inputs P0 through P3 and setting load input \overline{LOAD} to low-level, when CK changes from low-level to high-level, the P0 through P3 signals will be output to Q0 through Q3, respectively, irrespective of enable inputs E_P and E_T . This permits persetting of the counter

The reset operates asynchronously, and by setting direct reset input \overline{R}_D to low-level. Q0 through Q3 will become low, irrespective of other inputs.

The ripple carry output RCO will become high only when all of Q0, Q1, Q2, Q3 and E_T are high. E_P , E_T and RCO are used in cascade connections of the counter in synchronous from when the counter is used as a n-bit counter. (See the Application Example.)



FUNCTION TABLE (Note 1)

		Inputs					Output	s	
R _D	LOAD	Eτ	Ep	СК	Q0	Q3	RCO		
L	x	Х	Х	×	L	L	L	L	L
Н	L	L	Х	1					L
Н	L	Н	Х	Ť	P0	P1	P2	P3	L*
Н	н	Н	Н	Ť	Cou	nt			L*
Н	н	L	Х	х	Cou	L			
Н	Н	Н		X	Cou	nt sun	nresse	ď	1 *

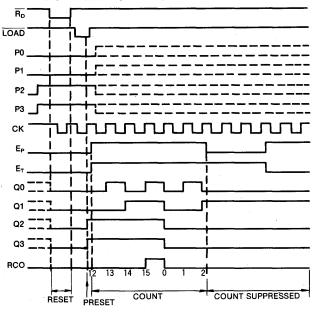
Note 1: † : Change from low to high level (positive-edge trigger)

 RCO is normally low, but will become high when all of Q0, Q1, Q2, Q3 and E_T are high. Accordingly, RCO =

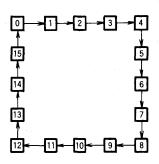
Q0 · Q1 · Q2 · Q3 · E₇

X : Irrelevant

OPERATION TIMING DIAGRAM



STATE TRANSITION DIAGRAM



ABSOLUTE MAXIMUM RATINGS $(\tau_a = -40 \sim +85^{\circ}C)$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage		-0.5~+7.0	V
V _i	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
	Insulation died accord	V ₁ < 0V	-20	
lıĸ	Input protection diode current	$V_i > V_{CC}$	20	mA
	Outside and a second	V _o < 0V	-20	
lok	Output parasitic diode current	$v_o > v_{cc}$. 20	mA
lo	Output current per output pin		±25	mA
Icc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65~+150	°C

Note 2 : M74HC161FP, $T_a = -40 \sim +70 ^{\circ} C$ and $T_a = 70 \sim 85 ^{\circ} C$ are derated at -6 mW/C. M74HC161DP, $T_a = -40 \sim +50 ^{\circ} C$ and $T_a = 50 \sim 85 ^{\circ} C$ are derated at -5 mW/C.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85 \degree C)$

Comphal	0-		Limits					
Symbol	Pai	rameter	Min	Тур	Max	Unit		
Vcc	Supply voltage	2		6	٧			
V _I	Input voltage		0		Vcc	٧		
V _o	Output voltage	Output voltage			Vcc	٧		
Topr	Operating temperature ra	ange	-40		+85	င		
		$V_{CC} = 2.0V$	0		1000			
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns		
		0		400				

ELECTRICAL CHARACTERISTICS

							Limits			
Symbol	Parameter	Test	conditions			25℃		-40~	+85℃	Unit
			Vcc		Min	Тур	Max	Min	Max	
		V = 0.1V V	0.114	2.0	1.5			1.5		
V _{IH}	High-level input voltage	1 -	$_{\rm O} = 0.1 \text{V}, \ \text{V}_{\rm CC} = 0.1 \text{V}$ $_{\rm O} = 20 \mu \text{A}$		3.15]	3. 15		V
		$ 1_0 = 20\mu\text{A}$			4.2	l	l	4. 2		
		V -0.1V V	0.114	2.0			0.5		0.5	-
VIL	Low-level input voltage	$V_0 = 0.1V, V_{CO}$	5—0.1 V	4.5		<u> </u>	1.35		1.35	V
		$ I_0 = 20\mu A$		6.0			1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
		10	$I_{OH} = -20\mu A$	4.5	4.4			4.4		
V _{OH}	High-level output voltage	$V_{I} = V_{IH}, V_{IL}$	$I_{OH} = -20\mu A$	6.0	5.9		ĺ	5.9		V
		ļ	$I_{OH} = -4.0 \text{mA}$	4.5	4.18			4.13		
			$I_{OH} = -5.2 \text{mA}$	6.0	5. 68		l	5.63		
			$I_{OL} = 20 \mu A$	2.0			0.1		0. 1	
			$I_{OL} = 20 \mu A$	4.5			0.1		0.1	
VoL	Low-level output voltage	$V_{I} = V_{IH}, V_{IL}$	$I_{OL} = 20 \mu A$	6.0	1	Ì	0.1		0.1	V
			I _{OL} = 4.0mA	4.5			0.26		0.33	
	1 -		$I_{OL} = 5.2 \text{mA}$	6.0	L		0.26		0.33	
I _{tH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μA
l _{IL}	Low-level input current	$V_i = 0V$		6.0			-0.1		-1.0	μА
Icc	Quiescent supply current	$V_{I} = V_{CC}$, GND	$I_0 = 0\mu A$	6.0			4.0		40.0	μА

SWITCHING CHARACTERISTICS ($V_{cc} = 2\sim 6V$, $T_a = -40\sim +85^{\circ}C$)

0		TA		Limits		Unit
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
fmax	Maximum clock frequency		30			MHz
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time				10	ns
t _{PLH}	Low-level to high-level and high-level to low-level				28	ns
t _{PHL}	output propagation time (CK - Q)				34	ns
t _{PHL}	High-level to low-level output propagation time $(\overline{R}_D - Q)$	C _L = 15pF (Note 4)			36	ns
t _{PLH}	Low-level to high-level and high-level to low-level				26	ns
t _{PHL}	output propagation time (E _T — RCO)				32	ns
t _{PLH}	Low-level to high-level and high-level to low-level		-		30	ns
t _{PHL}	output propagation time (CK - RCO)				36	ns
t _{PHL}	High-level to low-level output propagation time (Rp - RCO)				38	ns

SWITCHING CHARACTERISTICS ($V_{cc} = 2\sim 6V$, $T_a = -40\sim +85^{\circ}C$)

			4			Limits			[·
Symbol	Parameter	Test conditions			25℃		-40~	+85℃	Unit
		·	V _{CC} (V)	Min	Тур	Max	Min	Max	
			2.0	5			4		
fmax	Maximum clock frequency		4.5	27			21		MHz
			6.0	32	L		25		
			2.0			75		95	
t _{TLH}	Low-level to high-level and		4.5	ı		15		19	ns
	high-level to low-level		6.0			13		16	
	Ingli-level to low-level		2.0			75		95	
t _{THL}	output transition time		4.5			15		19	ns
			6.0			13		16	
			2.0			170		214	
t _{PLH}	Low-level to high-level and		4.5			34	[43	ns
	high-level to low-level		6.0			29		36	
	output propagation time	•	2.0			205		258	
t _{PHL}	(CK - Q)		4.5			41		52	ns
	1		6.0		1	35	ļ	44	ļ
	High-level to low-level	·	2.0			210		265	
t _{PHL}	output propagation time	C _L = 50pF (Note 4)	4.5			42		53	ns
	$(\overline{R_D} - Q)$		6.0			36		45	
			2.0			160		202	
t _{PLH}	Low-level to high-level and		4.5	ľ		32	l	40	ns
	high-level to low-level		6.0			27		34	
	output propagation time		2.0			195		246	
t _{PHL}	(E _T - RCO)		4.5			39		49	ns
			6.0			33		42	
			2.0			175		221	
t _{PLH}	Low-level to high-level and		4.5			35		44	ns
	high-level to low-level		6.0			30		37	
	output propagation time		2.0			215		271	
t _{PHL}	(CK - RCO)		4.5		1	43		54	ns
			6.0			37	1	46	
	High-level to low-level		2.0			220		277	
t _{PHL}	output propagation time		4.5			44		55	ns
	(RD - RCO)		6.0			37		47	
Cı	Input capacitance					10		10	pF
C _{PD}	Power dissipation capacitance (Note 3)				57				pF

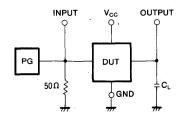
Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$



TIMING REQUIREMENTS ($V_{cc} = 2\sim 6V$, $T_a = -40\sim +85^{\circ}C$)

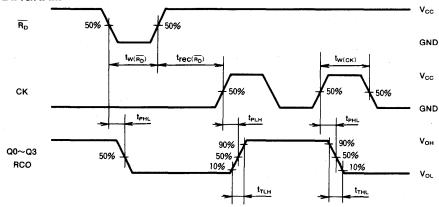
						Limits			
Symbol	Parameter	Test conditions			25℃		-40~	+85°C	Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	
`		,	2.0	80			101		
tw(ck)	Clock pulse width		4.5	16			20		ns
		-	6.0	14			17		
			2.0	80			101		
$t_{W(\overline{R_D})}$	Direct reset pulse width		4.5	16			20		ns
			6.0	14			17		_
	P setup time with		2. 0	150			189		
t _{su(P)}	respect to CK		4.5	30			38		ns
	lespect to CK		6.0	26			32		
	LOAD setup time with		2.0	135		-	170		
tsu(LOAD)	respect to CK		4. 5	27			34		ns
	respect to CK		6.0	23			29		
	E _T , E _P setup time with		2.0	200			250		
t _{su(E)}	respect to CK		4.5	40	Ì	1	50	}	ns
	respect to CK	,	6.0	34			43		
	Phold time with		2.0	50			63		
th(P)	respect to CK		4.5	10	ł		13		ns
	Tespect to CK		6.0	9			11	1	
	LOAD hold time with		2.0	0			0		
th(LOAD)	respect to CK		4.5	0		i	0		ns
	respect to CK		6.0	0			0	<u> </u>	
	E _T , E _P hold time with		2.0	0			0		
t _{h(E)}	respect to CK		4.5	0			0		ns
	Tespect to CK		6.0	0_			0	Ì	
	R _D recovery time with		2.0	125			158		
$t_{rec(\overline{R_D})}$	respect to CK		4.5	25			32		ns
	respect to OK		6.0	21			27		
	LOAD recovery time with		2.0	125			158		
trec(LOAD)	respect to CK		4.5	25			32	1	ns
	respect to OK		6.0	21	1		27		

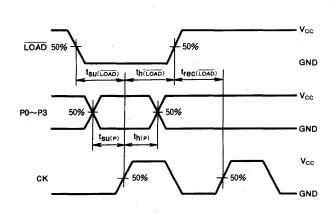
Note 4: Test Circuit

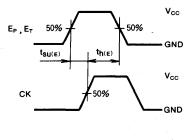


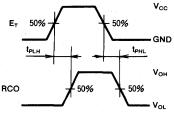
 ⁽¹⁾ The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
 (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



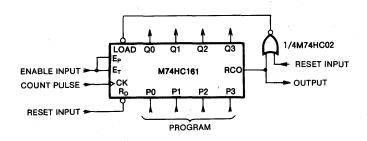






APPLICATION EXAMPLE

CONFIGURATION OF A PROGRAMMABLE DIVIDER



Note 5: The reset function is invoked by setting the reset input to high and applying a count pulse. The $\overline{R_D}$ pin cannot be used in this application because it sets Q0 through Q3 to low.

P0	P1	P2	P3	Rate of division
L	L	L	L	1/16
н	· L	L	L	1/15
L	Н	L	L	1/14
н	Н	L	L	1/13
L	L	Н	L	1/12
Н	L.	Н	L	1/11
L	Н	Ι	L	1/10
H	Н	H	L	1/9
L	L	L	Н	1/8
Н	L	L	Н	1/7
L	Н	L	Н	1/6
Η	Н	L	Н	1/5
L	L	Н	• Н	1/4
Н	L	Н	Н	1/3
1	Н	Ι	Ι	1/2



M74HC162P/FP/DP

PRESETTABLE BCD COUNTER WITH SYNCHRONOUS RESET

DESCRIPTION

The M74HC162 is a semiconductor integrated circuit consisting of a presettable synchronous BCD counter with a synchronous reset input.

FEATURES

- Synchronous reset and preset inputs
- Enable input and ripple-carry output allow cascade connection
- Count frequency 45MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- Wide supply voltage range: V_{CC}=2∼6V
- Wide operating temperature range: Ta=−40~+85°C

APPLICATION

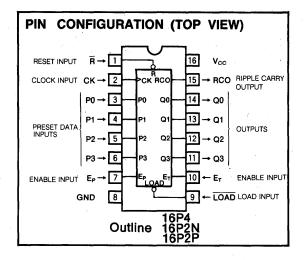
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC162 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS162.

When the count pluse is applied to clock input CK, the number of count pulses will be output at outputs Q0 through Q3 synchronous with the count pulse in BCD code. Counting takes place when CK changes from low-level to high-level.

The preset functions synchronously with the count pulse. By supplying data to PERSET data inputs P0 through P3 and setting load input $\overline{\text{LOAD}}$ to low-level, when CK changes

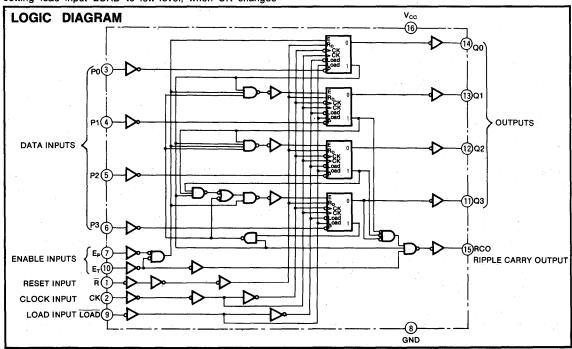


from low-level to high-level, the P0 through P3 signals will be output to Q0 through Q3, respectively, irrespective of enable inputs E_{P} and E_{T} . This permits presetting of the counter.

When values greater than 10 are preset, the count advances as shown in the State Transition Diagram.

The reset operates synchronously with the count pules, and by setting reset input \overline{R} to low-level, Q0 through Q3 will become low when CK changes from low-level to high-level.

The ripple carry output RCO will become high only when Q0 is high, Q1 is low, Q2 is low, Q3 is high and E_T is high. E_P , E_T and RCO are used in cascade connections of the counter in synchronous from when the counter is used as a n-bit counter. (See the Application Example.)



FUNCTION TABLE (Note 1)

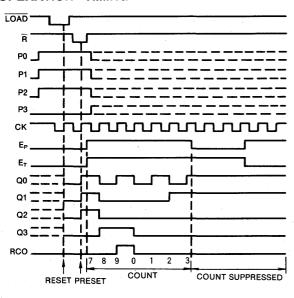
		Inputs							
R	LOAD	Ет	E _P	СК	Q0	Q1	Q2	Q3	RCO
L	X	Х	Х	1	L	L.	L	L	L
Н	L	L	Х	1		-			L
Н	L	Н	х	1	P0	P1	P2	P3	L*
Н	Н	Н	Н	1	Cou	nt		*	L*
Н	Н	L	Х	Х	Cou	nt sup	presse	d	L
н	Н	Н	L	×	Cou	nt sup	presse	d	L*

Note 1: 1: Change from low to high (positive-edge trigger)

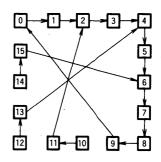
* : RCO is normally low, but will become high when Q0 is high, Q1 is low, Q2 is low, Q3 is high and E_T is high. Accordingly RCO = Q0 ⋅ Q1 ⋅ Q2 ⋅ Q3 ⋅ E_T

X : Irrelevant

OPERATION TIMING DIAGRAM



STATE TRANSITION DIAGRAM



ABSOLUTE MAXIMUM RATINGS $(\tau_a = -40 \sim +85^{\circ}C, \text{ unless otherwise noted})$

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
V _I	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
		V ₁ < 0V	-20	
lıĸ	Input protection diode current	$V_{l} > V_{CC}$	20	mA
	Cutantitis diad-	V ₀ < 0V	-20	
Іок	Output parasitic diode current	$V_{o} > V_{cc}$	20	mA mA
l _o	Output current per output pin		±25	mA
loc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		-65∼+150	°C

Note 2 : M74HC162FP, T $_a$ = $-40\sim+70^\circ$ C and T $_a$ = $70\sim85^\circ$ C are derated at -6mW/°C. M74HC162DP, T $_a$ = $-40\sim+50^\circ$ C and T $_a$ = $50\sim85^\circ$ C are derated at -5mW/°C.

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85 ^{\circ}\text{C})$

Symbol	Bo		Limits					
Symbol	Pa	rameter	Min	Тур	Max	Unit		
Vcc	Supply voltage	2		6	٧			
V ₁	Input voltage	0		Vcc	·V			
V _o	Output voltage	0.		Vcc	V			
Topr	Operating temperature ra	ange	-40		+85	°C		
		V _{CC} = 2.0V	. 0		1000			
r, tf	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns		
		$V_{CC} = 6.0V$	0		400			

ELECTRICAL CHARACTERISTICS

egogija kimenen i den ekkir en alla

							Limits			
Symbol	Parameter	Test	conditions			25℃		-40~+85℃		Unit
			V _{cc} (V)		Min	Тур	Max	Min	Max	
		$V_{0} = 0.1V, V_{CC}$	0.114	2.0	1.5			1.5		
V _{IH}	High-level input voltage	$ I_0 = 20\mu A$	o0.1 V	4.5	3, 15		1	3.15		v
		1101 == 20µA		6.0	4.2			4.2		
		V _O = 0.1V, V _{CC}	-0.17	2.0			0.5		0.5	
VIL	Low-level input voltage	$ V_0 = 0.1V, V_0 $	5—0.1 V	4.5	1		1.35		1.35	V
	1	1101 - 20AA		6.0]		1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
			$I_{OH} = -20\mu A$	4.5	4.4	ļ	1	4.4		
V_{OH}	High-level output voltage	$V_{i} = V_{iH}, V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		V
	'.		$I_{OH} = -4.0 mA$	4.5	4. 18			4. 13		
			$I_{OH} = -5.2 \text{mA}$	6.0	5. 68			5. 63		
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
			$I_{OL} = 20 \mu A$	4.5			0.1		0.1	
VoL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1	<u> </u>	0. 1	. V
			I _{OL} = 4.0mA	4.5			0.26		0.33	
			$I_{OL} = 5.2 mA$	6.0			0.26		0.33	
I _{IH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μA
I _{IL}	Low-level input current	$V_i = 0V$		6.0			-0.1		-1.0	μA
Icc	Quiescent supply current	VI = VCC, GND	$I_0 = 0\mu A$	6.0			4.0		40.0	μΑ

SWITCHING CHARACTERISTICS ($v_{cc} = 5v$, $\tau_a = 25$ °C)

		T	į	Unit		
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
fmax	Maximum clock frequency		30			MHz
t _{TLH}	Low-level to high-level and high-level to low-level	1			10	ns
t _{THL}	output transition time				10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	1			28	ns
t _{PHL}	output propagation time (CK — Q)	C _L = 15pF (Note 4)			34	ns
t _{PLH}	Low-level to high-level and high-level to low-level				26	ns
t _{PHL}	output propagation time (E _T — RCO)	The second secon			32	ns
t _{PLH}	Low-level to high-level and high-level to low-level				30	ns
t _{PHL}	output propagation time (CK - RCO)				36	ns

SWITCHING CHARACTERISTICS $(v_{cc} = 2\sim6v, \tau_a = -40\sim+85^{\circ}C)$

						Limits			
Symbol	Parameter	Test conditions			25℃		−40 ~	+85℃	Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0	5			4		
fmax	Maximum clock frequency		4.5	27	-		21	:	MHz
			6.0	32			25		
			2.0			75		95	
t _{TLH}	Low-level to high-level and		4.5			15 .		19	ns
	high-level to low-level		6.0			13		16	
	liigh-level to low-level		2.0			75		95	
t _{THL}	output transition time		4.5			15		19	ns
			6.0			13		16	
			2.0		-	170		214	
t _{PLH}	Low-level to high-level and		4.5			34		43	ns
	high-level to low-level		6.0			29		36	
	output propagation time		2.0			205		258	
t _{PHL}	(CK - Q)	C _L = 50pF (Note 4)	4.5			41		52	ns
	<u> </u>	·	6.0			35		44	
	*		2.0			160		202	
t _{PLH}	Low-level to high-level and		4.5			32		40	ns
	high-level to low-level		6.0			27		34	
	output propagation time		2.0			195		246	
t _{PHL}	(E _T — RCO)		4.5			39		49	ns
			6.0			33		42	
			2.0			175		221	
t _{PLH}	Low-level to high-level and		4.5		,	35		- 44	ns
	high-level to low-level		6.0			30		37	
	output propagation time		2.0			215		271	
t _{PHL}	(CK - RCO)		4.5			43		54	ns
			6.0			37	<u> </u>	46	
Cı	Input capacitance					10		10	рF
C _{PD}	Power dissipation capacitance (Note 3)				58				pF

Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.

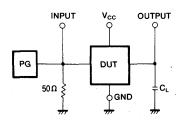
The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$



TIMING REQUIREMENTS ($V_{CC} = 2\sim 6V$, $T_a = -40\sim +85$ °C)

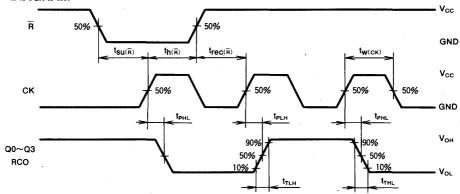
						Limits		,	
Symbol	Parameter	Test conditions			25℃		-40~	+85℃	Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	1
***			2.0	80			101		
tw(ck)	Clock pulse width		4.5	16			20		ns
			6.0	14			17	ļ.	
		•	2.0	150			189		
tsu(P)	P setup time with		4.5	30			38		ns
	respect to CK		6.0	26			32		
	LOAD setup time with		2.0	135			170		
tsu(LOAD)	respect to CK		4.5	- 27	ļ		34		ns
	respect to CK		6.0	23			29]
	R setup time with	•	2.0	160			202		
t _{su(Ä)}	respect to CK		4.5	32	Ì	1	40		ns
	respect to CK		6.0	27			34		
	E _T , E _P setup time with	r	2.0	200			250		
t _{su(E)}	respect to CK		4.5	40			. 50		ns
	respect to CK		6.0	34			43		
	P hold time with		2.0	50			63		
th(P)	respect to CK		4.5	10			13		ns
	respect to OK	•	6.0	9			11		
	LOAD hold time with		2.0	0	·		0		
th(LOAD)	respect to CK		4.5	0	1	1	0		ns
	respect to OK		6.0	0			0		
	R hold time with		2.0	0			0		
th(R)	respect to CK		4. 5	0	ĺ ,		0		ns
	respect to OK		6.0	. 0			0		
	E _T , E _P hold time with		2.0	0			0		
th(E)	respect to CK		4.5	0			0		ns
	respect to OK		6.0	0			0		
	R recovery time with		2.0	125			158		
t _{rec(R)}	respect to CK		4.5	25			32	1	ns
			6. 0	21			27		
	LOAD recovery time with		2.0	125			158		
trec(LOAD)	respect to CK		4.5	25			32		ns
	Topost to oit		6.0	21	L		27		L

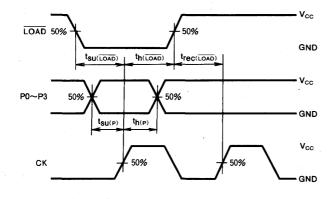
Note 4: Test Circuit

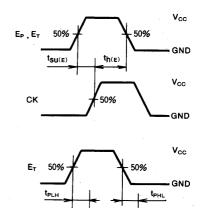


- (1) The pulse generator (PG) has the following characteristics (10%∼90%): t_r = 6ns, t_f = 6ns (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM







50%

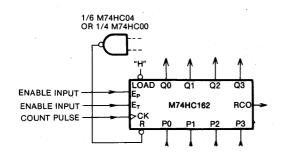
RCO

VoH

50%

APPLICATION EXAMPLE

CONFIGURATION OF A BASE n COUNTER



BASE n COUNTER	PIN CONNECTED TO GATE INPUT
3	Q1
5	Q2
6	Q0, Q2
7	Q1, Q2
9	Q3



M74HC163P/FP/DP

PRESETTABLE 4-BIT BINARY COUNTER WITH SYNCHRONOUS RESET

DESCRIPTION

The M74HC163 is a semiconductor integrated circuit consisting of a presettable synchronous 4-bit binary (hexadecimal) counter with synchronous reset input.

FEATURES

- synchronous reset and preset inputs
- Enable input and ripple-carry output allow cascade connection
- Count frequency: 45MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- Wide operating voltage range: V_{CC}=2∼6V
- Wide operating temperature range: T_a=-40~+85℃

APPLICATION

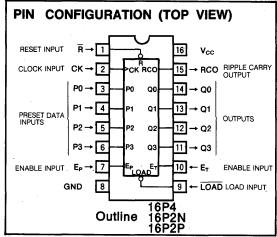
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC163 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS163.

When the count pulse is applied to clock input CK, the number of count pulses will be output at outputs Q0 through Q3 synchronous with the count pulse in 4-bit binary code. Counting takes place when CK changes from low-level to high-level.

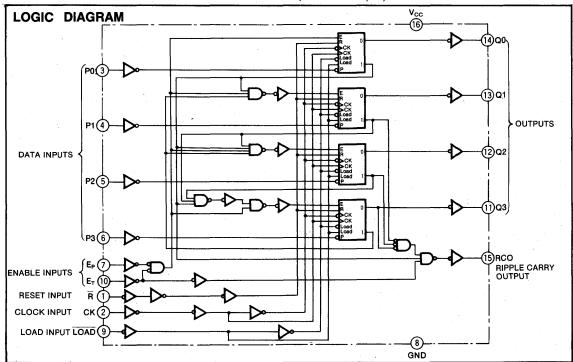
The preset functions synchronously with the count pulse. By



supplying data to PERSET data inputs P0 through P3 and setting load input \overline{LOAD} to low-level, when CK changes from low-level to high-level, the P0 through P3 signals will be output to Q0 through Q3, respectively, irrespective of enable inputs E_P and E_T . This permits persetting of the counter

The reset operates synchronously with the count pules, and by setting reset input \overline{R} to low-level, Q0 through Q3 will become low when CK changes from low-level to high-level.

The ripple carry output RCO will become high only when Q0, Q1, Q2, Q3 and E_T are high. E_P , E_T and RCO are used in cascade connections of the counter in synchronous from when the counter is used as a n-bit counter. (See the Application Example.)



FUNCTION TABLE (Note 1)

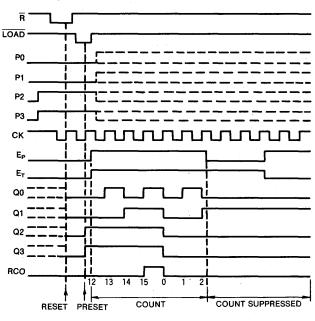
	Inputs						Output	s	
R	LOAD	Eτ	E _P	СК	Q0	Q1	Q2	Q3	RCO
L	X	X	х	†	L	L	L	L	L
Н	L	L	Х	1		P1	P2	Р3	L
Н	L	Н	Х	1	P0	"	P2	Po	L*
Н	Н	Н	Н	1	Cou	nt			L*
Н	Н	L	Х	Х	Count suppressed				L
Н	Н	Н	L	Х	Cou	nt sup	presse	d	L*

Note 1: † : Change from low to high (positive-edge trigger)

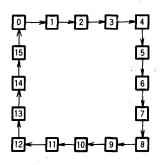
* : RCO is normally low, but will become high when all of Q0, Q1, Q2, Q3 and E_T are high. Accordingly, RCO = Q0 · Q1 · Q2 · Q3 · E_T

X: irrelevant

OPERATION TIMING DIAGRAM



STATE TRANSITION DIAGRAM



ABSOLUTE MAXIMUM RATINGS $(T_a = -40 \sim +85 \degree)$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
V _I	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
		$V_1 < 0\dot{V}$	-20	
lik	Input protection diode current	V _I > V _{CC}	20	mA
		V ₀ < 0V	-20	
lok	Output parasitic diode current	$V_{\rm o} > V_{\rm cc}$	20	mA
lo	Output current per output pin		±25	mA
loc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		-65∼+150	°C

Note 2 : M74HC163FP, T $_{\rm a}=-40\sim+70^{\circ}$ C and T $_{\rm a}=70\sim85^{\circ}$ C are derated at -6mW/°C. M74HC163DP, T $_{\rm a}=-40\sim+50^{\circ}$ C and T $_{\rm a}=50\sim85^{\circ}$ C are derated at -5mW/°C.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85 \degree C)$

Symbol	Parameter			l Imia		
- Symbol	га	ranieter	Min	Тур	Max	Unit
Vcc	Supply voltage		2		6	V
V _I	Input voltage		0		V _{cc}	٧
Vo	Output voltage	Output voltage			Vcc	٧
Topr	Operating temperature ra	ange	-40		+85	r
		$V_{CC} = 2.0V$	0		1000	
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$. 0		500	ns
	$V_{CC} = 6.0V$. 0		400	

ELECTRICAL CHARACTERISTICS

		· · · · · · · · · · · · · · · · · · ·			Limits					
Symbol	Parameter	Test	Test conditions V _{CC} (V)		25℃			-40~+85°C		Unit
					Min	Тур	Max	Min	Max	
		Vo = 0.1V, Voc	0.11/	2.0	1.5			1.5		
VIH	High-level input voltage	$ I_0 = 20\mu A$;u. 1 v	4.5	3.15			3. 15		V
				6.0	4.2			4.2		
		$V_0 = 0.1V, V_{CC}$	0.11/	2.0			0.5		0.5	
VIL	Low-level input voltage	1 -	5—0. 1 V	4.5			1.35		1.35	V
		1101 - 20µA	$ I_0 = 20\mu A$				1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
			$I_{OH} = -20\mu A$	4. 5	4.4			4.4		
V _{OH}	High-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		V
	·		$I_{OH} = -4.0 \text{mA}$	4. 5	4. 18			4. 13		
			$I_{OH} = -5.2 \text{mA}$	6.0	5. 68			5. 63		
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
			$I_{OL} = 20 \mu A$	4.5			0.1		0.1	
VoL	Low-level output voltage	$V_i = V_{iH}, \ V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
	·		I _{OL} = 4.0mA	4.5			0.26		0.33	
			$I_{OL} = 5.2 \text{mA}$	6.0			0.26	1	0.33	
l _{iH}	High-level input current	V ₁ = 6V		6.0			0. 1		1.0	μА
I _{IL}	Low-level input current	V ₁ = 0V	V ₁ == 0V				-0.1		-1.0	μА
Icc	Quiescent pupply current	VI = VCC, GND	$I_0 = 0 \mu A$	6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS $(v_{cc} = 5v, T_a = 25°C)$

	Parameter			Unit		
Symbol	Parameter	Test conditions	Min	Тур	Max	Onit
fmax	Maximum clock frequency		30			MHz
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time		-		10	ns
t _{PLH}	Low-level to high-level and high-level to low-level				28	ns
t _{PHL}	output propagation time (CK - Q)	C _L = 15pF (注4)			34	ns
t _{PLH}	Low-level to high-level and high-level to low-level				26	ns
t _{PHL}	output propagation time (E _T — RCO)			-	32	ns
t _{PLH}	Low-level to high-level and high-level to low-level	7			30	ns
t _{PHL}	output propagation time (CK - RCO)				36	ns

SWITCHING CHARACTERISTICS $(V_{cc} = 2\sim 6V, T_a = -40\sim +85\%)$

						Limits			
Symbol	Parameter	Test conditions		25℃			40~	+85℃	Unit
			V _{CC} (V)	Min	Тур	Max	Min	Max	
			2.0	5			4		
fmax	Maximum clock frequency		4.5	27	İ		21		MHz
			6.0	32			25		
			2.0			75		95	
t _{TLH}	Low-level to high-level and		4.5			15		19	ns
	high-level to low-level		6.0			13		16	<u> </u>
	mgn-level to low-level		2.0			75		95	
t _{THL}	output transition time		4.5			15		19	ns
			6.0			13		16	
			2.0			170		214	
t _{PLH}	Low-level to high-level and		4.5			34		43	ns
	high-level to low-level		6.0			29		36	
	output propagation time		2.0			205		258	
t _{PHL}	(CK - Q)	C _L = 50pF (Note 4)	4.5			41		52	ns
			6.0			35		44	
			2.0			160		202	
t _{PLH}	Low-level to high-level and		4.5			32		40	ns
	high-level to low-level		6.0			27		34	
	output propagation time		2.0			195		246	
t _{PHL}	(E _T - RCO)		4.5			39		49	ns
		·	6.0			33		42	-
,			2.0			175		221	
t _{PLH}	Low-level to high-level and		4.5			35		44	ns
	high-level to low-level		6.0			30		37	
	output propagation time		2.0			215		271	
t _{PHL}	(CK - RCO)		4.5			43		54	ns
			6.0			37		46	
Cı	Input capacitance					10		10	pF
C _{PD}	Power dissipation capacitance (Note 3)				62				pF

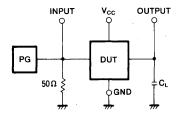
Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula: $P_{D} = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$



TIMING REQUIREMENTS ($V_{cc} = 2\sim 6V$, $T_a = -40\sim +85^{\circ}$)

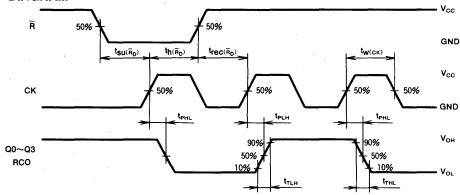
						Limits			
Symbol	Parameter	Test conditions			25℃		-40~	+85°C	Unit
	,		V _{cc} (V)	Min	Тур	Max	Min	Max	1
			2.0	80			101		
t _{w(cK)}	Clock pulse width	• '	4. 5	16			20		ns
			6.0	14			17		
		7	2.0	150			189		
t _{su(P)}	P setup time with		4.5	30		ĺ	38		ns
	respect to CK	•	6.0	26			32		l
	1015		2.0	135			170		
tsu(LOAD)	LOAD setup time with		4.5	27	7		34		ns
	respect to CK		6.0	23			29		
	=		2.0	160			202		
t _{su(≅)}	R setup time with		4.5	32			40		ns
	respect to CK		6.0	27	ļ	ļ	34		
	5 5 1 - 1 1		2.0	200			250		
t _{su(E)}	E _T , E _P setup time with		4.5	40	,		50		ns
	respect to CK		6.0	34	İ		43		
			2.0	50			63		
th(P)	P hold time with		4.5	10			-13		ns
	respect to CK		6.0	9			11		
****	LOAD hold time with		2.0	0			0		
th(LOAD)			4.5	0			0		ns
	respect to CK		6.0	0			0		
			2.0	0			0		-
th(R)	R hold time with		4.5	0			0		ns
	respect to CK	· ·	6.0	0			0		
	F F - 11.0		2.0	0			0		
th(E)	E _T , E _P hold time with		4.5	0			0		ns
	respect to CK		6.0	0			0		
			2.0	125			158		
t _{rec(R)}	R recovery time with		4.5	25			32		ns
	respect to CK		6.0	21			27		
	LOAD		2.0	125			158		
trec(LOAD)	LOAD recovery time with		4.5	25	'		32		ňs
	respect to CK		6.0	21			27		

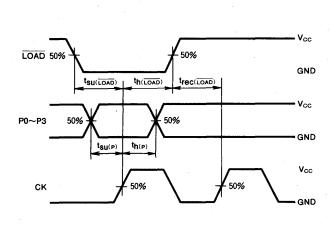
Note 4: Test Circuit

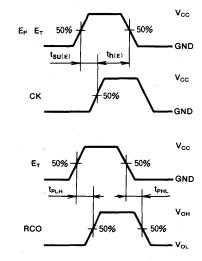


- (1) The pulse generator (PG) has the following characteristics (10%∼90%): t_r = 6ns, t_t = 6ns (2) The capacitance C_L includes stray wiring
- capacitance and the probe input capacitance.



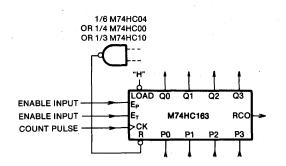






APPLICATION EXAMPLE

CONFIGURATION OF A BASE n COUNTER



BASE	PIN CONNECTED TO GATE INPUT
3	Q1
5	Q2
6	Q0, Q2
7	Q1, Q2
9	Q3
10	Q0, Q3
11	Q1, Q3
12	Q0, Q1, Q3
13	Q2, Q3
14	Q0, Q2, Q3
15	Q1, Q2, Q3

M74HC164P/FP/DP

8-BIT SERIAL-INPUT/PARALLEL-OUTPUT SHIFT REGISTER

DESCRIPTION

The M74HC164 is a semiconductor integrated circuit consisting of an 8-bit serial-input serial/parallel-output shift register with direct reset input.

FEATURES

- High-speed: (Clock frequency) 60MHz typ.
 (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=-40~+85℃

APPLICATION

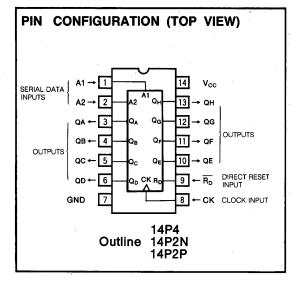
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC164 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS164.

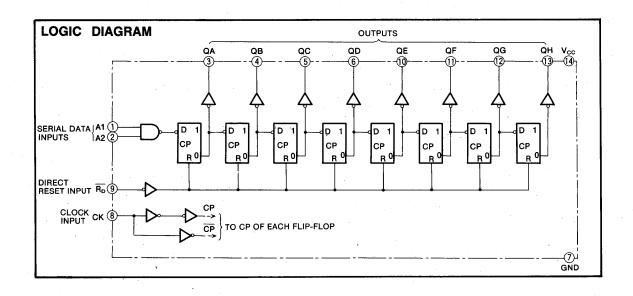
The M74HC164 consists of eight edge-triggered D-type flip-flops. The logical product A1-A2 of the serial data inputs A1 and A2 acts as the shift register input. QA through QH are taken out from the outputs of each flip-flop.

When both A1 and A2 are high, and the clock pulse is applied to clock input CK, the high-level signals will be shifted synchronously with the clock pulse in the order of QA-QH.



When at least one of A1 or A2 is low, the low-level signal will be shifted synchronously with the clock pulse. The shift operation will take place when CK changes from low-level to high-level.

When the direct reset input $\overline{R_D}$ is low, all outputs will be reset to low-level irrespective of other inputs. When used as a shift register, $\overline{R_D}$ should be maintained at high-level.



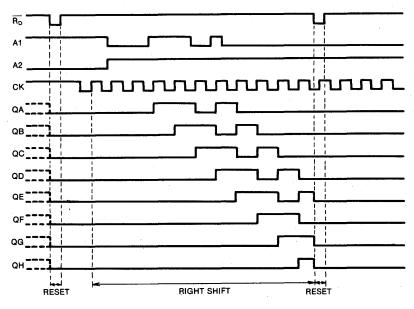
FUNCTION TABLE (Note 1)

Operating		Inp	uts			Outputs							
mode	R₀	СК	A1	A2	QA	QB	QC	QD	QE	QF	QG	QH	
Reset	L	Х	Х	X	L	L	L	L	L	L	L	L	
	Н	†	L	L	L	QA ⁰	QB ⁰	QC°	QDº	QEº	QF ⁰	QGº	
	Н	†	Н	L	L	QA ⁰	QBº	QCº	QDº	QE°	QF ⁰	QGº	
Right shift	Н	Ť	L	Н	L	QA ^o	QBº	QCº	QD°	QE ⁰	QF ⁰	QGº	
	Н	†	Н	н	Н	QAº	QB ⁰	QCº	QD°	QEº	QF ⁰	QGº	
No change	Н	1	Х	х	QAº	QB ⁰	QC°	QDº	QEº	QF ⁰	QGº	QHº	

Note 1: † : Change from low-level to high-level

Change from high-level to low-level Q⁰ : Output state before clock input changed X : Irrelevant

OPERATING TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS $(T_a = -40 \sim +85 ^{\circ}C)$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
V _I	Input voltage		-0.5~V _{cc} +0.5	·V
Vo	Output voltage	•	-0.5~V _{cc} +0.5	٧
		V ₁ < 0V	20	
lik .	Input protection diode current	V _I > V _{CC}	20	mA.
		V ₀ < 0V	20	
lok	Output parasitic diode current	V _o > V _{cc}	20	mA.
lo	Output current per output pin		±25	mA
lcc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		-65~+150	°C

Note 2 : M74HC164FP, $T_a = -40 \sim +70^\circ C$ and $T_a = 70 \sim 85^\circ C$ are derated at -6mW/°C. M74HC164DP, $T_a = -40 \sim +50^\circ C$ and $T_a = 50 \sim 85^\circ C$ are derated at -5mW/°C.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85 \degree C)$

Oh. al	D-1			Limits					
Symbol	Pa	rameter	Min	Тур	Max	Unit			
Vcc	Supply voltage		2		6	V			
V _I	Input voltage		0		Vcc	V			
Vo	Output voltage		. 0		Vcc	V			
Topr	Operating temperature ra	ange	—40		+85	င			
		$V_{CC} = 2.0V$	0		1000				
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns			
	, .,	$V_{CC} = 6.0V$	0	400					

ELECTRICAL CHARACTERISTICS

多婚姻 医二硫氧铅矿矿 海岸部 计经验码对抗原约点

							Limits			
Symbol	Parameter	Test	conditions			25℃		-40~	+85°C	Unit
	· .			V _{CC} (V)	Min	Тур	Max	Min	Max	
		V = 0.1V V	0.114	2.0	1.5			1.5		
V_{IH}	High-level input voltage	$V_0 = 0.1V, V_{CO}$ $ I_0 = 20\mu A$;—0. 1 V	4.5	3. 15			3. 15		٧
		$I_0! = 20\mu\text{A}$	$f_0 = 20\mu A \qquad \qquad 6.0$		4.2			4.2		
		V = 0.1V V	0.114	2.0			0.5		0.5	
VIL	Low-level input voltage	$ V_0 = 0.1V, V_{CC}$ $ I_0 = 20\mu A$	$V_0 = 0.1V, V_{CC} - 0.1V$				1.35		1.35	V
	· · · · · · · · · · · · · · · · · · ·	$ I_0 = 20\mu A$		6.0			1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
			$I_{OH} = -20\mu A$	4.5	4.4			4.4		100
V _{OH}	High-level output voltage	$V_{I} = V_{IH}, V_{IL}$	$I_{OH} = -20\mu A$	6.0	5. 9			5.9		· · · V
			$I_{OH} = -4.0 \text{mA}$	4.5	4. 18			4.13		
			$I_{OH} = -5.2 \text{mA}$	6.0	5. 68		14.1	5.63		1
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
			$I_{OL} = 20 \mu A$	4.5			0.1		0.1	
VoL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	v
			I _{OL} = 4.0mA	4.5			0.26		0.33	
			$I_{OL} = 5.2 mA$	6.0		İ	0.26		0.33	
I _{IH}	High-level input current	$V_1 = 6V$		6.0			0.1		1.0	μА
I _{IL}	Low-level input current	V ₁ = 0V		6.0			-0.1		-1.0	μΑ
I _{CC}	Quiescent supply current	$V_I = V_{CC}$, GND	$I_{0} = 0 \mu A$	6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS ($v_{cc} = 5v$, $T_a = 25^{\circ}C$)

Comphal	Parameter	Task and disional			Unit	
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
fmax	Maximum clock frequency		30			MHz
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time				10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = 15pF (Note 4)			30	ns
t _{PHL}	output propagation time (CK — Q)				30	ns
t _{PHL}	High-level to low-level output propagation time $(\overline{R}_D - Q)$				35	ns

SWITCHING CHARACTERISTICS ($v_{cc} = 2\sim6v$, $T_a = -40\sim+85^{\circ}C$)

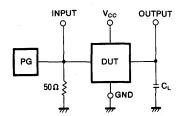
						Limits			
Symbol	Parameter	Test conditions			25℃		-40~	+85℃	Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0	- 5			4		Ĭ
fmax	Maximum clock frequency		4.5	27			21		MHz
		'	6.0	31			24		
			2.0			75		95	
t _{TLH}	Low-level to high-level and	·	4.5			15	}	19	ns
	high favorite lave		√6.0			13		16	
	high-level to low-level		2.0			75		95	
t _{THL}	output transition time		4.5			15		19	ns
		$C_L = 50 pF \text{ (Note 4)}$	6.0		1	13	Ì	16	
		CL — SOPP (Note 4)	2.0			175		218	1
t _{PLH}	Low-level to high-level and		4. 5			35		44	ns
	high-level to low-level		6.0			30		38	
	output propagation time		2.0			175		218	
t _{PHL}	(CK - Q)		4.5		1	35		44	ns
			6.0			30		- 38	
	High-level to low-level		2, 0			205		256	
t _{PHL}	output propagation time		4.5			41		51	ns
	$(\overline{R_D} - Q)$		6.0			35		44	
Cı	Input capacitance					10		10	pF
CPD	Power dissipation capacitance (Note 3)				150				pF

Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS ($v_{cc} = 2\sim 6V$; $T_a = -40\sim +85^{\circ}$)

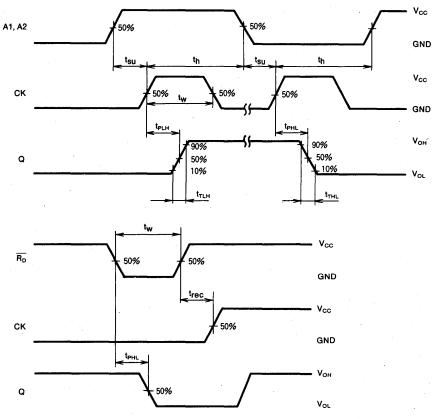
						Limits			
Symbol	Parameter	Test conditions		25℃			-40~	+85°C	Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0	80			100		
tw	CK, RD clock pulse width	•	4.5	16			20		ns
			6.0	14	1		18	ļ	1
			2.0	50			65		
t _{su}	A setup time with	· ·	4.5	10			13	İ	ns
	respect to CK		6.0	9			11		
			2.0	5			5		
th	A hold time with	A TO SERVE AND AN AREA AND AN	4.5	5			5		ns
	respect to CK	·	6.0	5	}		5		
			2.0	5			5		
trec	trec respect to CK		4.5	5			5	1	ns
			6.0	5			5		

Note 4: Test Circuit



- (1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns (2) The capacitance C_L includes stray wiring
- capacitance and the probe input capacitance.

TIMING DIAGRAM





MITSUBISHI HIGH SPEED CMOS

M74HC165P/FP/DP

8-BIT SERIAL-OR PARALLEL-INPUT/SERIAL-OUTPUT SHIFT REGISTER

DESCRIPTION

The M74HC165 is a semiconductor integrated circuit consisting of an 8-bit serial- or parallel-input/serial output shift register.

FEATURES

- High-speed: 40MHz clock frequency typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85°C

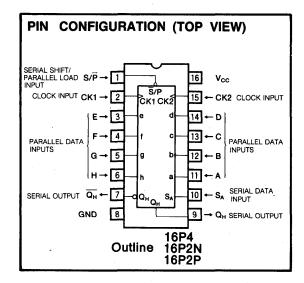
APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

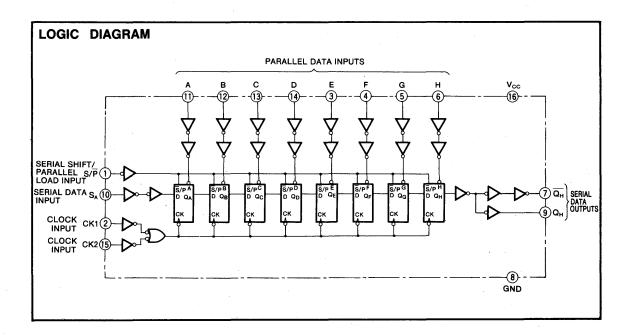
Use of silicon gate technology allows the M74HC165 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS165.

The parallel or serial input mode is selected by serial shift/parallel load input S/\overline{P} signal. When S/\overline{P} is high, serial data input S_A operates and the 8-bit flip flop operates serial shifts with the clock pulse. When S/\overline{P} is low, parallel data inputs $A\sim H$ operate. As $A\sim H$ enter direct set, direct reset



of each flip flop, irrespective of other inputs be read. Serial data transfer is suspended while parallel loading takes place. The load and shift operation takes place when clock input CK1 or CK2 changes from low to high.

For permit use of combination of two clock or use of one prohibition clock input, clock is 2-input NOR gate. When either input is maintained high, the clock operation stops. When it is maintained low, the data transfer is possible.



FUNCTION TABLE (Note 1)

BASSART OF LEADING TO THE BASSACTION

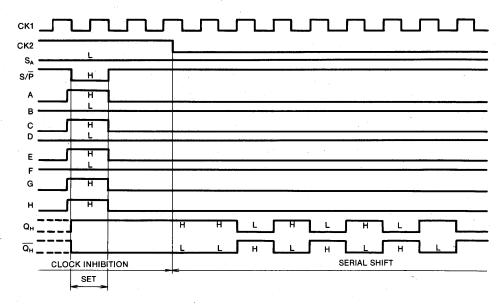
Operating			Inputs			Outputs								
Operating mode	S/P	CK1	СК2		А∼Н		Internal						Q _H	Ια
mode	3/1	CKI	CKZ	SA	А~п	Q ⁴	Qв	Qc	QD	QE	Q_F	Q _G	СZН	ĭ
Load	L	Х	Х	Х	a~h	а	b	С	d ·	е	f	g	h	h
	Н	†	L	L	Х	L	$Q_A{}^0$	Q _B ⁰	Q _C °					Q _G °
	Н	1	L	Н	Х	Н	Q_A^0	Q _B ⁰	Q _C °	Q_D^0				Q _G ⁰
Shift	Н	L	1	L.	х	L	Q _A o	Q _B ⁰	Q _C ⁰	Q_D^0		Q _F ⁰		Q _G ⁰
	Н	L	1	Н	Х	Н	Q _A o	Q _B ^o	Qcº	Q_D^0	Q _E 0	Q _F ⁰	Q _G ⁰	Q _G ⁰
Clock	Н	Н	Х	X.	х	Q_A^0	Q _B ⁰	Qcº	Q₀°	Q _E ⁰	Q _F ⁰		Q _H ⁰	Q _H ⁰
inhibition	Н	Х	Н	Х	Х	Q_A^0	Q _B ⁰	Qcº			Q _F ⁰		Q _H °	Q _H ⁰
No change	Н	· X	Х	Х	Х	Q _A º	Q _B ⁰	Q _C ⁰	Q _D ⁰	Q _E ⁰	Q _F ⁰	Q _G ⁰	QH	Q _H ⁰

Note 1: X : Irrelevant

† : Change from low to high

Qº : Output state before clock input changed

OPERATING TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS $(\tau_a = -40 \sim +85^{\circ}C)$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	and the second second	-0.5~+7.0	V
V _I	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
		V ₁ < 0V	-20	
1 _{IK}	Input protection diode current	V ₁ > V _{CC}	20	mA .
		V ₀ < 0V	-20	
lok	Output parasitic diode current	V _o > V _{cc}	20	⊢ mA
lo	Output current per output pin		±25	mA .
loc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65~+ 150	င

Note 2 : M74HC165FP, T $_{\rm a}=-40\sim+70^{\circ}$ and T $_{\rm a}=70\sim85^{\circ}$ C are derated at -6mW/°C. M74HC165DP, T $_{\rm a}=-40\sim+50^{\circ}$ C and T $_{\rm a}=50\sim85^{\circ}$ C are derated at -5mW/°C.



RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85^{\circ}C)$

Symbol	Do	rameter		Unit		
Зуппон	ra	rameter	Min	Тур	Max	Unit
Vcc	Supply voltage		2		6	٧
V _i	Input voltage	nput voltage			Vcc	٧
Vo	Output voltage	Output voltage			Vcc	٧
Topr	Ambient operating temper	erature	-40		+85	°C
		$V_{CC} = 2.0V$	0		1000	
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns
		$V_{CC} = 6.0V$	0		400	

ELECTRICAL CHARACTERISTICS

							Limits			
Symbol	Parameter	Test	conditions			25℃		-40~	-+85°C	Unit
			•	V _{CC} (V)	Min	Тур	Max	Min	Max	
		V = 0 1V V	0.114	2.0	1.5			1.5		
VIH	High-level input voltage	$V_0 = 0.1V, V_{CO}$ $ I_0 = 20\mu A$		4.5	3. 15			3. 15		V
		$ 1_0\rangle = 20\mu$ A		6.0	4.2			4.2		•
		V =0.1V V	V = 0.1V V = 0.1V				0.5		0.5	
VIL	Low-level input voltage		$V_0 = 0.1V, V_{CC} = 0.1V$ $ I_0 = 20\mu A$		1		1.35		1.35	V
		1101 - 20μΑ			-		1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
			$I_{OH} = -20\mu A$	4.5	4. 4			4.4	1	
V_{OH}	High-level output voltage	$V_i = V_{iH}, \ V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		V
			$I_{OH} = -4.0 \text{mA}$	4.5	4. 18			4.13		
			$I_{OH} = -5.2 \text{mA}$	6.0	5.68			5.63		
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
			$I_{OL} = 20 \mu A$	4.5		ŀ	0.1		0.1	
VoL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
			I _{OL} = 4.0mA	4.5		,	0. 26		0.33	
			$I_{OL} = 5.2 \text{mA}$	6.0			0.26		0.33	
I _{IH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μΑ
l _{IL}	Low-level input current	$V_1 = 0V$		6.0			-0.1		-1.0	μA
Icc	Quiescent supply current	VI = VCC, GND	$l_0 = 0 \mu A$	6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS $(v_{cc} = 5v, T_a = 25^{\circ}C)$

0		T-A		Unit		
Symbol	Parameter	Test conditions	Min	Тур	10 10 25 25 30 30 25	Omit
fmax	Maximum clock frequency		30			MHz
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time				10	ns
t _{PLH}	Low-level to high-level and high-level to low-level				25	ns
t _{PHL}	output propagation time (CK $ Q_H$ or $\overline{Q_H}$)	C _L = 15pF (Note 4)			25	ns
t _{PLH}	Low-level to high-level and high-level to low-level				30	ns
t _{PHL}	output propagation time $(S/\overline{P} - Q_H \text{ or } \overline{Q_H})$				30	ns
t _{PLH}	Low-level to high-level and high-level to low-level				25	ns
t _{PHL}	output propagation time $(H - Q_H \text{ or } \overline{Q_H})$	· ·			25	ns

SWITCHING CHARACTERISTICS $(V_{cc} = 2 \sim 6V, T_a = -40 \sim +85^{\circ}C)$

医乳球形态 化氯酸性钠 医电压的 经额带经验的 二氯酚

				Limits					
Symbol	Parameter	Test conditions		25℃			-40~+85°C		Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max]
			2.0	5			4	1	
fmax	Maximum clock frequency		4.5	27	i		21		MHz
			6.0	32			25		
			2.0			75		95	
t _{TLH}	Low-level to high-level and		4.5			15		19	ns
	1		6.0			13		16	
	high-level to low-level	·	2.0			75		95	
t _{THL}	output transition time		4.5			15		19	ns
			6.0			13.		16	
			2.0			150		189	
t _{PLH}	Low-level to high-level and		4.5			- 30	ļ	38	ns
	high-level to low-level		6.0			26		32	
	output propagation time		2.0			150		189	
t _{PHL}	(Clock - Q _H , Q _H)	C _L = 50pF (Note 4)	4.5			30		38	ns
			6.0			26		32	
			2.0			175		221	
t _{PLH}	Low-level to high-level and		4.5			35		- 44	ns
	high-level to low-level		6.0			30		37	
	output propagation time	÷ .	2.0			175		221	
t _{PHL}	(S/P — Q _H or Q _H)		4.5			35		44	ns
			6.0			30		37	
			2.0			150		189	
t _{PLH}	Low-level to high-level and		4.5		1	30	\	38	ns
	high-level to low-level	e e	6.0			26		32	
	output propagation time		2.0			150		189	
t _{PHL}	$(H - Q_H \text{ or } \overline{Q_H})$		4.5			30		38	ns
			6.0		L	26		32	
Cı	Input capacitance					10		10	pF
C _{PD}	Power dissipation capacitance (Note 3)								pF

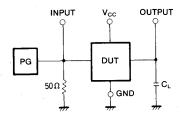
Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot v_{CC}^2 \cdot f_1 + I_{CC} \cdot v_{CC}$



TIMING REQUIREMENTS $(v_{cc} = 2\sim6v, T_a = -40\sim+85^{\circ})$

					Limits					
Symbol	Parameter	Test conditions			25℃		-40~	+85°C	Unit	
			V _{cc} (V)	Min	Тур	Max	Min	Max		
	Clock pulse width		2.0	. 80			101			
tw	Load pulse width		4.5	16			20		ns	
	Load pulse width		6.0	14			17	-		
			2.0	100			126			
	S _A setup time with respect to CK		4.5	20			25		ns	
			6.0	17			21			
			2.0	100			126			
:	S/P setup time with respect to CK		4.5	20			25		ns	
			6.0	17			21			
tsu A∼H setup tim			2.0	100			126			
	A~H setup time with respect to S/P		4.5	20			25	l	ns	
			6.0	17			21			
	CK1 and an Aire with an an Aire CK0		2.0	100			126			
	CK1 setup time with respect to CK2		4.5	20		ļ	25		ns	
	CK2 setup time with respect to CK1		6.0	17			21			
		*	2.0	0			0			
	S _A hold time with respect to CK		4.5	0			0		ns	
			6.0	0			0			
			2.0	0			0			
th	S/P hold time with respect to CK		4.5	0			0 .		ns	
		*	6.0	0			0			
			2.0	0			0			
	A~H hold time with respect to S/P		4.5	0	1	1	0		ns	
			6.0	. 0			0			
-	CK1 recovery time with respect to CK2	4	2.0	100			126			
trec	1		4.5	20			25		ns	
	CK2 recovery time with respect to CK1		6.0	17	1		21			

Note 4: Test Circuit



- (1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_r = 6ns (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM Vcc СК 50% 50% S/P 50% 50% 50% 50% GND GND t_{PLH} t_{PLH} t_{PHL} V_{OH} V_{OH} 90% 90% QH OR QH 50% 50% 50% Q_{H} 50% .10% 10% Vol t_{TLH} Vон Q_H 50% 50% VOL v_{cc} v_{cc} 50% · S/P 50% GND GND tsu th Vcc QH OR QH 50% 50% 50% VoL - GND V_{CC} V_{CC} S/P SA 50% 50% 50% 50% GND GND th tsu tsu V_{CC} V_{CC} СК 50% 50% СК - GND GND V_{CC} CK1 50% 50% 50% GND tsu(CK1) trec(cki) tsu(ck2) trec(CK2 V_{CC} CK2 50% 50% 50% 50% GND

M74HC166P/FP/DP

8-BIT SERIAL-OR
PARALLEL-INPUT/SERIAL-OUTPUT SHIFT REGISTER WITH RESET

DESCRIPTION

The M74HC166 is a semiconductor integrated circuit consisting of an 8-input serial/parallel-input serial-output shift register.

FEATURES

- High-speed: (Clock frequency) 60MHz typ.
 (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max
 (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

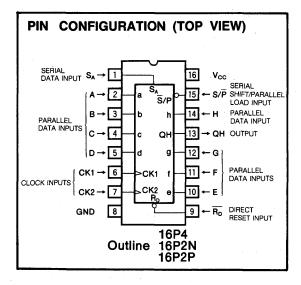
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

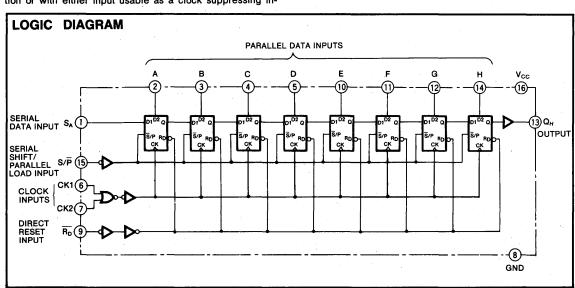
Use of silicon gate technology allows the M74HC166 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS166.

Parallel or serial input modes can be selected by the signal of the serial-shift/parallel-load input S/\overline{P} . When S/\overline{P} is high, serial data input S_A is enabled and 8-bit flip-flop is possible to do serial shift by the clock pulse. When S/\overline{P} is low, parallel data inputs A through H are enabled and the input data is loaded syncrnously with the next clock pulse. During the parallel load, transfer of serial data is suppressed. Shift or load is enabled when clock input CK1 or CK2 changes from low-level to high-level.

The clock employs a 2-input NOR, with usable in combination or with either input usable as a clock suppressing in-



put. When one of the inputs is held at high-level, the clock stops; when held at low-level, data transfer is enabled. When direct reset input $\overline{R_D}$ is low, the shift register is reset irrespective of other inputs.



8-BIT SERIAL-OR PARALUEL-INPUT/SERIAL-OUTPUT SHIFT REGISTER WITH RESET

FUNCTION TABLE (Note 1)

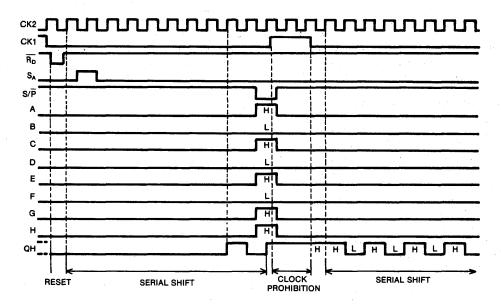
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0======================================			Inp	uts			Outputs			
Operating mode	Rp	c/Ē	01/1	CK2		А~Н	Inte	rnal	_	
mode	ΠD	5/P	CKI	CKZ	SA	A~ n	QA	Qв	QH	
Load	Н	L	X	Х	Х	a~h	а	b	h	
	Н	H	1	L	L	X	L	Q _A º	Q _G ⁰	
01.00	Н	H.	1	٦	Н	Х	Н	Q _A °	O _O	
Shift	Н	Н	L	1	L	Х	٦	QAO	Qgº	
	Н	H	L	1	Н	X,	I	Q _A °	Qg°	
Clock	Н	Н	Н	Х	X	X	Q _A ⁰	Q _B °	Q ₁ o	
prohibition	Н	H	Х	I	Х	Х	Q_A°	Q _B ⁰	Q _H °	
No change	Н	Н	L	L	х	Х	Q _A ⁰	Q _B ⁰	Q _H °	
Reset	L	Х	Х	Х	×	Х	L	L,	L	

Note 1 : X : Irrelevent

† : Change from low-level to high-level Q° : Output state before clock input changed

OPERATING TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS $(\tau_a = -40 \sim +85^{\circ}\text{C}, \text{ unless otherwise noted})$

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
,		V ₁ < 0V	-20	
_l ıκ	Input protection diode current	V _i > V _{CC}	20	mA.
	Outside and a second	V ₀ < 0V	-20	
Іок	Output parasitic diode current	Vo > Vcc	20	mA.
lo	Output current per output pin		±25	mA
loc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		-65~+150	°C

Note 2 : M74HC166FP, T_a = $-40\sim+70^\circ$ C and T_a = $70\sim85^\circ$ C are derated at -6mW/°C. M74HC166DP, T_a = $-40\sim+50^\circ$ C and T_a = $50\sim85^\circ$ C are derated at -5mW/°C.



RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85 \degree c)$

Combal			Limits				
Symbol	Pa	Min	Тур	Max	Unit		
Vcc	Supply voltage	2		6	٧		
V _t	Input voltage	0		Vcc	V		
Vo	Output voltage	0		Vcc	٧		
Topr	Operating temperature ra	inge	40		+85	°C	
	Input risetime, failtime	$V_{CC} = 2.0V$	0		1000		
t _r , t _f		V _{CC} = 4.5V	0		500	ns	
	$V_{CC} = 6.0V$		0		400		

ELECTRICAL CHARACTERISTICS

							Limits			
Symbol	Parameter	Test conditions V _{CC} (V)		25℃			-40~+85°C		Unit	
				Min	Тур	Max	Min	Max		
		$V_{O} = 0.1V, V_{CC} - 0.1V$ 2. 0 4. 5 6. 0		2.0	1.5			1.5		
VIH	High-level input voltage			4.5	3.15	ŀ		3.15		v
				6.0	4. 2			4.2		
	the second second	$V_0 = 0.1V, V_{CC} = 0.1V$		2.0			0.5		0.5	
V _{IL}	Low-level input voltage	1	5—0.1 V	4.5			1.35	}	1.35	v
		$ I_{O} = 20\mu A$		6.0			1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
ŀ	High-level output voltage	$V_i = V_{iH}, \ V_{iL}$	$I_{OH} = -20\mu A$	4.5	4.4		İ	4.4		
Voн			$I_{OH} = -20\mu A$	6.0	5.9			5.9		V
ł			$I_{OH} = -4.0 \text{mA}$	4.5	4. 18			4.13		
			$I_{OH} = -5.2 mA$	6.0	5. 68			5. 63		
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
			$I_{OL} = 20 \mu A$	4.5			0.1	[0.1	
VoL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
			I _{OL} = 4.0mA	4.5			0.26		0.33	
		1	I _{OL} = 5. 2mA	6.0		L	0.26	<u> </u>	0.33	
I _{IH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μА
I _{IL}	Low-level input current	V ₁ = 0V		6.0			-0.1		-1.0	μA
Icc	Quiescent supply current	VI = VCC, GND	$I_0 = 0\mu A$	6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS $(v_{cc} = 5v, \tau_a = 25^{\circ})$

		T		11-14		
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
fmax	Maximum clock frequency		35			MHz
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time				10	ns
tpLH	Low-level to high-level and high-level to low-level	C _L = 15pF (Note 4)			25	ns
t _{PHL}	output propagation time (CK - Q _H)				25	ns
•	High-level to low-level output propagation time				25	ns
t _{PHL}	$(\overline{R}_D - Q_H)$					

SWITCHING CHARACTERISTICS ($V_{cc} = 2\sim 6V$, $T_a = -40\sim +85$ °C)

代表: 化分成物法 海域游戏 计极级数据

						Limits			Ţ
Symbol	Parameter	Test conditions		25℃			-40~+85°C		Unit
			V _{cc} (V)	Mìn	Тур	Max	Min	Max	1
•			2.0	6			5		
fmax	Maximum clock frequency		4.5	31		ļ	25		MHz
			6.0	36	1		29	1	
		· .	2.0			75		95	
t _{TLH}	Low-level to high-level and		4.5			15]	19	ns
	high favol to love town	1 :	6.0			13		16	
	high-level to low-level		2.0			75		95	
t _{THL}	output transition time		4.5		1	15	1	19	ns
		C _L = 50pF (Note 4)	6.0			13		16	ļ .
		CL = 50pr (Note 4)	2. 0			150		190	
t _{PLH}	Low-level to high-level and		4.5		}	30		38	ns
	high-level to low-level		6.0			26		32	1
	output propagation time		2.0			150		190	
t _{PHL}	(CK — Q _H)	1	4.5			30		38	ns
			6.0			26		32	
	High-level to low-level output		2.0			150		190	
t _{PHL}	propagation time $(\overline{R_D} - Q_H)$		4.5		-	30		38	ns
	propagation time (np — QH)		6.0			26	111	32	
Cı	Input capacitance					10		10	pF
CPD	Power dissipation capacitance (Note 3)			2	76		<u> </u>		pF

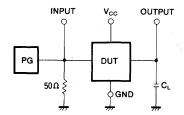
Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$



TIMING REQUIREMENTS $(V_{cc} = 2\sim 6V, T_a = -40\sim +85^{\circ}C)$

	ł				Limits				
Symbol	Parameter	Test conditions		25℃			-40~	+85℃	Unit
		•	V _{cc} (V)	Min	Тур	Max	Min	Max	<u> </u>
			2.0	80			100		
tw(ck)	Clock pulse width		4.5	16			20	1	ns
			6.0	14			17		
			2.0	100			125		
$t_{W(\overline{R_D})}$	Direct reset pulse width		4.5	20			25		ns
_			6.0	17	1		21		
			2.0	80			100		
t _{su(A∼H)}	A∼H setup time with		4.5	16	1		20		ns
respect to CK		6.0	14			17			
			2.0	80			100		
t _{su(s_A)}	S _A setup time with		4.5	16			20		ns
-Su (Og)	respect to CK		6.0	14			17		
			2.0	145			180	 	t -
tsu(s/P)	S/P setup time with		4.5	29			36		ns
respect to CK	1	6.0	25			31			
			2, 0	100	 		125	_	
†	CK1 setup time with		4.5	20			25		ns
t _{SU(CK1)} respect to CK2		6.0	17			21		"	
	·		2.0	100	 		125		
•	CK2 setup time with		4.5	20			25		
tsu(CK2)	respect to CK1		6.0	17			25	1	ns
					<u> </u>	-			ļ
	A~H hold time with		2.0	5			5		
th(A~H)	respect to CK		4.5	5	-		5	1	ns
	,		6.0	5		L	5		
	S _A hold time with		2.0	5			5		ĺ
th(s _A)	respect to CK	·	4.5	5			5	ĺ	ns
			6.0	5	<u> </u>		5		
	S/P hold time with		2.0	.0			0		
th(s/P)	respect to CK		4.5	0			0		ns
			6.0	0			0		
	CK1 recovery time with		2.0	100			125		
trec(ck1)	respect to CK2		4.5	20			25		ns
	respect to GRZ		6.0	17	,		21		
	CK2 recovery time with		2.0	100			125		
trec(ck2)	CK2 recovery time with	**	4.5	20			25		ns
	respect to CK1	,	6.0	17			21	1	
_			2.0	40			50		
trec(RD)	R _D recovery time with		4.5	8			10		ns
.50(1)	respect to CK		6.0	7		1	9	1	1

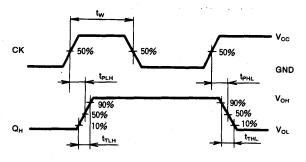
Note 4: Test Circuit



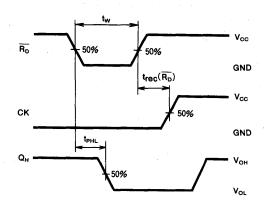
⁽¹⁾ The pulse generator (PG) has the following

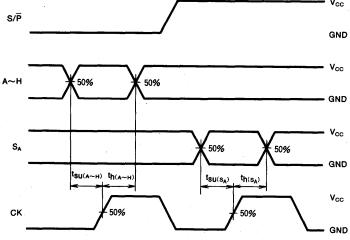
characteristics (10%~90%): t_t = 6ns, t_t = 6ns (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

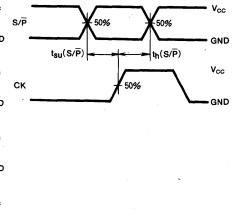
TIMING DIAGRAM

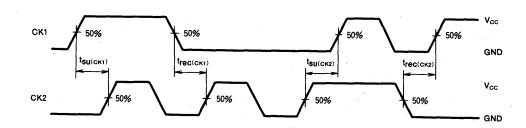


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M74HC173P/FP/DP

QUADRUPLE 3-STATE D-TYPE FLIP-FLOP WITH COMMON CLOCK AND RESET

DESCRIPTION

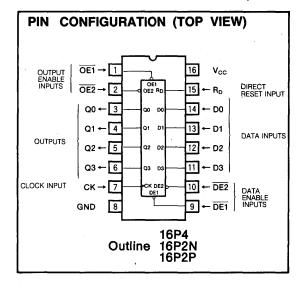
The M74HC173 is a semiconductor integrated circuit consisting of a 4-bit register with 3-state output.

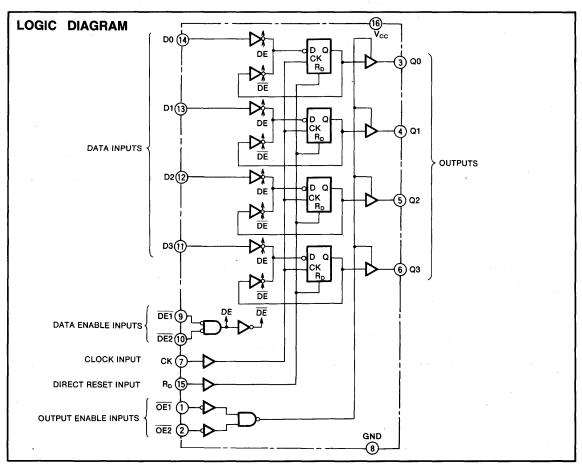
FEATURES

- High-speed: (clock frequency) 60MHz typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC} , min (V_{CC} =4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=-40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.





QUADRUPLE 3-STATE D-TYPE FLIP-FLOP WITH COMMON CLOCK AND RESET

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC173 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS173.

The M74HC173 contains four edge-triggered D-type flip-flops with common direct reset input R_{D} and common clock input CK.

When CK changes from low-level to high-level, the signals just previously input at D appears at outputs Q in accordance with the function table given.

When R_D becomes high while output enable inputs $\overline{OE1}$ and $\overline{OE2}$ are held low, all outputs Q become low-level irrespective of other inputs.

When one of data enable inputs $\overline{DE1}$ or $\overline{DE2}$ is high, while $\overline{OE1}$, $\overline{OE2}$ and R_D are held low, output Q is maintained.

When either $\overline{\text{OE1}}$ or $\overline{\text{OE2}}$ is high, all outputs Q will become the high-impedance state, and the contents of the flip-flop are not affected even when $\overline{\text{OE1}}$ and $\overline{\text{OE2}}$ are changed. When used as a D-type flip-flop, $\overline{\text{OE1}}$, $\overline{\text{OE2}}$, R_D , $\overline{\text{DE1}}$ and $\overline{\text{DE2}}$ should all be maintained at low-level.

FUNCTION TABLE (Note 1)

			Inputs				Output
OE1	OE2	R _D	СК	DE1	DE2	۵	Q
L	L	н	Х	X	Х	X	L
L	L	L	L	X	Х	Х	Q°
L	L	L	Н	X	Х	X	Q°
L	L	L	1	Н	х	Х	Q°
L	L	L	1	X	Н	Х	Qº
L	L	L	Î	L	L	L	L
L	L	L	1	L	L	Н	Н
L	L	L	ļ	X	X	×	Q°
L	Н	Х	X	х	Х	X	Z
Н	L	X	Х	X	Х	X	Z
Н	Н	x	Х	Х	х	х	Z

Note 1 : Z : High impedance

X : Irrelevant

↓ : Change from high to low level
 Q₀ : Output state Q before clock input changed.

ABSOLUTE MAXIMUM RATINGS $(\tau_a = -40 \sim +85 ^{\circ}C)$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V :-
•	Inc. A mark-object diada accessor	V ₁ < 0V	-20	
1 _{IK}	Input protection diode current	$V_1 > V_{CC}$	20	mA
1	Output perceitie diede current	V ₀ < 0V	-20	4
Ток	Output parasitic diode current	V _o > V _{cc}	20	mA
lo	Output current per output pin		±35	mA
Icc	Supply/GND current	V _{CC} , GND	±75	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65~ + 150	င

Note 2 : M74HC173FP, T_a = $-40\sim+70^\circ$ C and T_a = $70\sim85^\circ$ C are derated at -7mW/°C M74HC173DP, T_a = $-40\sim+50^\circ$ C and T_a = $50\sim85^\circ$ C are derated at -5mW/°C

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85 \degree)$

Combal				Limits				
Symbol	Pai	rameter	Min	Тур	Max	Unit		
V _{CC}	Supply voltage	2		6	V			
V _I	Input voltage	0		Vcc	V			
Vo	Output voltage	0		Vcc	V			
Topr	Operating temperature ra	ange	-40		+85	င		
		$V_{CC} = 2.0V$	0		1000	15.1		
t _r , t _f	input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns		
		$V_{CC} = 6.0V$	0		400	1		

M74HC173P/FP/DP

QUADRUPLE 3-STATE D-TYPE FLIP-FLOP WITH COMMON CLOCK AND RESET

ELECTRICAL CHARACTERISTICS

							Limits			
Symbol	Parameter	Test	conditions			25℃		-40~	+85°C	Unit
		1	V _{CC} (V)		Min	Тур	Max	Min	Max	
		V _O ≈ 0.1V, V _O	0.117	2.0	1.5			1.5		
V_{IH}	High-level input voltage	$ V_0 = 0.1V, V_{CO} $ $ I_0 = 20\mu A$		4.5	3. 15	ł		3. 15	ŀ	V
		6.0		4.2			4.2			
		$V_0 = 0.1V$, V_{CC}	0.11/	2.0			0.5		0.5	
V_{1L}	Low-level input voltage	$ V_0 = 0.1V$, V_{CO}	50. TV	4.5			1.35		1: 35	V
		$ 1_0 = 20\mu\text{A}$		6.0			1.8		1.8	
			$I_{OH} = -20 \mu A$	2.0	1.9			1.9		
V _{OH} High-level output voltage	[$I_{OH} = -20\mu A$	4.5	4.4	1		4.4		v
	High-level output voltage	$V_{l} = V_{lH}, V_{lL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		
	,		$I_{OH} = -6.0 \text{mA}$	4.5	4.18			4. 13		
			$I_{OH} = -7.8 mA$	6.0	5.68		į	5. 63		
			$I_{OL} = 20 \mu A$	2.0	_		0.1		0.1	
			$I_{OL} = 20 \mu A$	4.5			0.1	!	0.1	
VOL	Low-level output voltage	$V_{i} = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0		Ì	0.1		0.1	v
			I _{OL} = 6.0mA	4.5			0. 26		0.33	
_			$I_{OL} = 7.8 \text{mA}$	6.0		·	0.26		0.33	
I _{IH}	High-level input current	$V_1 = 6V$		6.0			0.1		1.0	μA
l _{IL}	Low-level input current	V₁ = 0V		6.0			-0.1		-1.0	μА
lozh	Off-state high-level output current	$V_i = V_{iH}, \ V_{iL}, \ V_{iL}$	Vo = Vcc	6.0			0.5		5.0	μA
lozL	Off-state low-level output current	$V_{I} = V_{IH}, V_{IL}, V_{IL}$	Vo = GND	6.0			-0.5		-5.0	μA
Icc	Quiescent supply current	VI = VCC, GND	$I_0 = 0 \mu A$	6.0			4.0		40.0	μΑ

SWITCHING CHARACTERISTICS ($V_{cc} = 5V$, $T_a = 25^{\circ}C$)

Symbol	Parameter	Test conditions	Limits			Unit
Symbol	raianietei	l est conditions	Min	Тур	Max	Unit
fmax	Maximum clock frequency		30			MHz
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time	***			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = 50pF (Note 4)			31	ns
t _{PHL}	output propagation time (CK - Q)				31	ns
t _{PHL}	High-level to low-level output propagation time $(R_D-Q) \label{eq:RD}$				27	ns
t _{PLZ}	Low-level, high-level output disable time	$C_L = 5 \text{pF} (\text{Note 4})$			25	ns
t _{PHZ}	$(\overline{OE} - \mathbf{Q})$	C _L = 5 pr (Note 4)			25 -	ns
t _{PZL}	Low-level, high-level output enable time	$C_1 = 50pF (Note 4)$			28	ns
t _{PZH}	(OE - Q)	C _L = 50pr (Note 4)			28	ns

QUADRUPLE 3-STATE D-TYPE FLIP-FLOP WITH COMMON CLOCK AND RESET

SWITCHING CHARACTERISTICS $(V_{cc} = 2\sim6V, T_a = -40\sim+85\%)$

Burgatan ing ting ting kalaman kalaman di burga si terbah

哪個人種意思的實際生活的人

O b l	5		-		05%	Limits	40	1.05%	1
Symbol	Parameter	Test conditions	[14 (4)		25℃	 		+85℃	Uni
			V _{cc} (V)	Min	Тур	Max	Min	Max	
	Manager at the second	0 = 50=5 (N=++ 4)	2.0	5	,	i l	4.	-	
max	Maxmum clock frequency	$C_L = 50 pF (Note 4)$	4.5	27			21		МН
	<u> </u>	 	6.0	32	 	60	25	75	
	A sur lawel to black found and	,	2.0		-	60		15	
TLH	Low-level to high-level and		4.5 6.0		1	12 10		13	ns
	high-level to low-level	C _L == 50pF (Note 4)	2.0		 	60		75	
	gutnut transition time	ĺ	4.5			12		15	ns
t _{THL}	output transition time		6.0			10		13	118
		 	2.0		 	175		221	
			4.5			35		44	
PLH			6.0		1	30		37	ns
	-	C _L = 50pF (Note 4)	2.0		-	175		221	-
·	Low-level to high-level and		4.5			35		44	ns
PHL	high-level to low-level		6.0			30		37	ns
	output propagation time		2.0		 	225		284	-
PLH	(CK — Q)		4.5			45		57	ns
PLH	(OK Q)		6.0		ł	38		48	118
	\dashv	C _L = 150pF (Note 4)	2.0			225		284	+
)			4.5]	45		57	n
PHL			6.0			38		48	111
		1	2.0		 	150		189	-
	High-level to low-level	C _L = 50pF (Note 4)	4.5			30		38	ns
		OL — SOPI (NOIS 4)	6.0		}	26		32	'"
t _{PHL}	output propagation time		2.0		 	200		252	
	$(R_D - Q)$	C _L = 150pF (Note 4)	4.5			40		50	ns
	(iii)	or apply (Hote 4)	6.0		1	34		43	113
	<u> </u>		2.0			150		189	
t _{PLZ}	Low-level, high-level		4.5			30		38	ns
PLZ	Low lovel, mgm lovel	1	6.0		1	26		32	1 "
	output disable time	$C_L = 50 pF (Note 4)$	2.0		 	150		189	-
t _{PHZ}	$(\overline{OE} - Q)$	1	4.5			30		38	ns
*PHZ	(52 4)		6.0			26		32	'"
			2, 0			150		189	†
t _{PZL}	}		4.5			30		38	n
			6.0			26		32	
	┥	$C_L = 50 pF (Note 4)$	2.0			150		189	1
l _{PZH}	Low-level, high-level		4.5			30		38	n
			6.0		1	26		32	1
	output enable time		2.0		T	200		252	1
PZL	(OE - Q)		4.5			40		50	l n
	1		6.0			34		43	1
	7	$C_L = 150 pF (Note 4)$	2.0			200		252	1
PZH			4.5		1.	40		50	· n
		~ .	6.0		1	34	1	43	
C,	Input capacitance					10		10	pl
Co	Off-state output capacitance	OE = V _{CC}				15		15	pi
CPD	Power dissipation capacitance (Note:				45	1		1	pi

Note 3: C_{DP} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per flip-flop) The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$



QUADRUPLE 3-STATE D-TYPE FLIP-FLOP WITH COMMON CLOCK AND RESET

TIMING REQUIREMENTS ($v_{cc} = 2\sim 6v$, $T_a = -40\sim +85^{\circ}C$)

						Limits			1
Symbol	Parameter	Test conditions	*		25℃		-40~+85℃		Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	
			2. 0	80			101		
tw	CK, R _D Clock pulse width		4.5	16			20	,	ns
			6.0	14			17	[
D DE		2.0	100			126			
tsu	D, DE setup time with		4.5	20	1		25	ļ	ns
	respect to CK		6.0	17			21		
	D, DE hold time with		2.0	0			0		
th			4.5	0			0		ns
	respect to CK		6.0	0			0		
	D		2.0	90			113		
trec	rec R _D recovery time with respect to CK		4.5	18			23		ns
			6.0	15	1		19		1

 ν_{cc}

GND

 V_{OH}

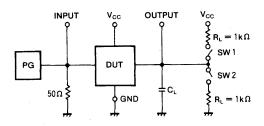
50%

t_{PHL}

90%

50%

Note 4: Test Circuit



Parameter	SW 1	SW 2
t _{TLH} , t _{THL} t _{PLH} , t _{PHL}	Open	Open
t _{PLZ}	Closed	Open
t _{PHZ}	Open	Closed
tezL	Closed	Open
town	Open	Closed

- (1) The pulse generator (PG) has the following characteristics (10%~90%): $t_r = 6ns$, $t_f = 6ns$
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

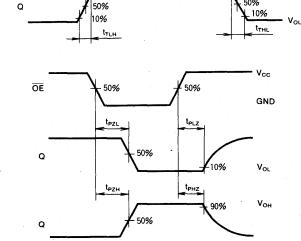
TIMING DIAGRAM

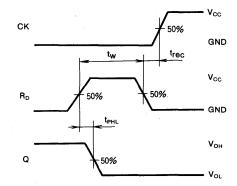
50%

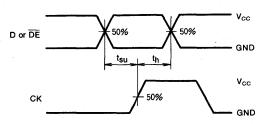
t_{PLH}

90%

СК







M74HC174P/FP/DP

HEX D-TYPE FLIP-FLOP WITH COMMON CLOCK AND RESET

DESCRIPTION

The M74HC174 is a semiconductor integrated circuit consisting of six positive-edge triggered D-type flip flops with common clock and direct reset inputs.

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FEATURES

- High-speed: (clock frequency) 60MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2∼6V
- Wide operating temperature range: Ta=-40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

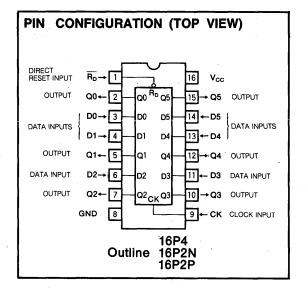
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC174 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS174.

The M74HC174 contains six internal edge-triggered D-type flip-flops with common direct reset input $\overline{R_D}$ and common clock input CK.

When CK changes from low-level to high-level, the signals' just previously input D appears at outputs Q in accordance with the function table given. When $\overline{R_D}$ is low, all outputs Q will become low irrespective of other inputs.

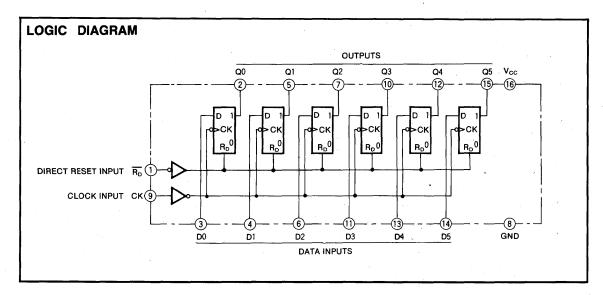
When used as a D-type flip-flop, $\overline{R_{\text{D}}}$ should be maintained at high-level.



FUNCTION TABLE (Note 1)

	Inputs	,	Outputs
R _D	СК	D	Q
Н	1	Н	н
Н	t	L	L
Н	1	X	Q°
L	X	Х	L
Н	L	×	Q°

- Note 1 : X : Irrelevant
 - † : Change from low to high
 - ↓ : Change from high to low
 - Q⁰ : Output state Q before clock input changed



HEX D-TYPE FLIP-FLOP WITH COMMON CLOCK AND RESET

ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85 \degree$ C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit		
Vcc	Supply voltage		-0.5~+7.0	V		
Vi	Input voltage		-0.5~V _{cc} +0.5	V		
Vo	Output voltage		-0.5~V _{cc} +0.5	V		
		V _i < 0V	-20			
lik	Input protection diode current	$V_1 > V_{CC}$	20	mA		
		V ₀ < 0V	-20			
lok	Output parasitic diode current	Vo > Vcc	20	mA		
l _o	Output current per output pin		±25	mA		
Icc	Supply/GND current	V _{CC} , GND	±50	mA		
Pd	Power dissipation	(Note 2)	500	mW		
Tstg	Storage temperature range		-65~+150	°C		

Note 2 : M74HC174FP, T_a = $-40\sim+70^\circ$ C and T_a = $70\sim85^\circ$ C are derated at -6mW/°C. M74HC174DP, T_a = $-40\sim+50^\circ$ C and T_a = $50\sim85^\circ$ C are derated at -5mW/°C.

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85^{\circ}C)$

0				Unit			
Symbol	Pa	rameter	Min	Тур	Max	Unit	
Vcc	Supply voltage	2		6	V		
Vı	Input voltage	0		Vcc	٧		
Vo	Output voltage	0		Vcc	٧		
Topr	Operating temperature ra	ange	-40		+85	°C	
		$V_{CC} = 2.0V$	0		1000		
t _r , t _f	input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns	
		$V_{CC} = 6.0V$			400		

ELECTRICAL CHARACTERISTICS

							Limits			
Symbol	Parameter	Test	conditions		25℃			-40~+85°C		Unit
			V _{cc} (V)		Min	Тур	Max	Min	Max	
		$V_0 = 0.1V, V_{CC}$	_0 1v	2.0	1.5			1.5		
V_{IH}	High-level input voltage	$ I_0 = 20\mu A$;0.1 v	4.5	3.15			3.15		V,
		1101 - 20µA	$ (10) = 20\mu A $ 6.0		4.2		ĺ	4.2		
		$V_0 = 0.1V, V_{CC}$	0.11/	2.0			0.5		0.5	
VIL	Low-level input voltage	$ V_0 = 0.1V, V_{CO}$ $ I_0 = 20\mu A$;0.1 v	4.5			1.35		1.35	V
		Πο = 20μΑ		6.0			1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
		$I_{OH} = -20\mu A$	4.5	4.4			4.4	}		
V_{OH}	High-level output voltage	$V_i = V_{iH}, \ V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		v
			$I_{OH} = -4.0 \text{mA}$	4.5	4.18			4. 13		
			$I_{OH} = -5.2 \text{mA}$	6.0	5. 68			5. 63		
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
			$I_{OL} = 20 \mu A$	4.5			0.1		0.1	l
VOL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1	ļ	0.1	V
	-		I _{OL} = 4.0mA	4. 5			0. 26		0.33	
		$l_{OL} = 5.2 mA$	6.0			0.26		0.33		
I _{iH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μА
I _{IL}	Low-level input current	$V_i = 0V$		6.0			-0.1		-1.0	μА
Icc	Quiescent supply current	VI = VCC, GND	$I_0 = 0\mu A$	6.0			4.0		40.0	μΑ

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SWITCHING CHARACTERISTICS ($v_{cc} = 5v$, $\tau_a = 25^{\circ}$)

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Complete	Parameter	Test conditions		Limits			
Symbol	Parameter	rest conditions	Min	Тур	Max	Unit	
fmax	Maximum clock frequency		30			MHz	
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns	
t _{THL}	output transition time				10	ns	
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = 15pF (Note 4)			30	ns	
t _{PHL}	output propagation time (CK - Q)				30	ns	
t _{PHL}	High-level to low-level output propagation time $(\overline{R}_D - Q)$				30	ns	

SWITCHING CHARACTERISTICS ($V_{cc} = 2\sim 6V$, $T_a = -40\sim +85^{\circ}C$)

						Limits			
Symbol	Parameter	Test conditions			25℃		-40~+85°C		Unit
	İ		V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0	5			4		
fmax	Maximum clock frequency		4.5	27			21		MHz
			6.0	31			24		
			2.0			75		95	
tTLH	Low-level to high-level and		4. 5			15	}	19	ns
	high toyal to love		6.0			13		16	
	high-level to low-level		2.0			75		95	
t _{THL}	output transition time	ļ	4.5	l		15		19	ns
		$C_L = 50 pF \text{ (Note 4)}$	6.0			13	· ·	16	
		C _L = 50pF (Note 4)	2.0			165		206	
t _{PLH}	Low-level to high-level and		4.5	l		33	1	41	ns
	high-level to low-level		6.0			28		35	
	output propagation time		2.0			165		206	
t _{PHL}	(CK - Q)		4.5	1		33	}	41	ns
			6.0			28		35	
	High-level to low-level		2.0			165		206	
t _{PHL}	output propagation time		4.5			33	1	41	ns
	$(\overline{R_D} - Q)$		6.0			28		35	
Cı	Input capacitance					10		10	pF
CPD	Power dissipation capacitance (Note 3)				64				pF

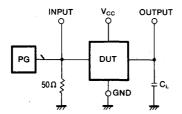
Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS ($V_{cc} = 2\sim 6V$, $T_a = -40\sim +85^{\circ}C$)

						Limits			
Symbol	Parameter	Test conditions		25℃			-40~	+85°C	Unit
			V _{CC} (V)	Min	Тур	Max	Min	Max	
			2.0	80			106		
tw(ck)	Clock pulse width		4.5	16			20	1	ns
	1		6.0	14			18		
			2.0	80			106		
$t_{W(\overline{R_D})}$	Direct reset pulse width		4.5	16			20		ns
-		*	6.0	14			18		
			2.0	100			125		Ī .
tsu	D setup time with		4.5	20			25		ns
	respect to CK		6.0	17			21		
		·	2.0	5			5		
th	D hold time with		4.5	5		1	5		ns
	respect to CK		6.0	5			5		
7	-		2.0	5			5		
trec	R ₀ recovery time with		4.5	5			5		ns
	respect to CK		6.0	5			5		

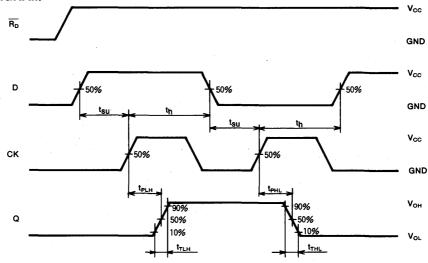
HEX D-TYPE FLIP-FLOP WITH COMMON CLOCK AND RESET

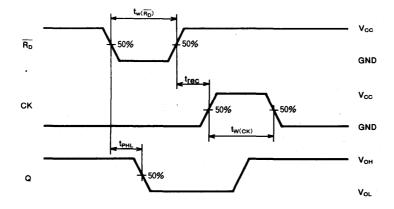
Note 4: Test Circuit



- (1) The pulse generator (PG) has the following characteristics (10%~90%): $t_{\rm f}=6{\rm ns},\,t_{\rm f}=6{\rm ns}$
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





M74HC175P/FP/DP

1999 SQUADRUPLE D-TYPE FLIP-FLOP WITH COMMON CLOCK AND RESET

DESCRIPTION

The M74HC175 is a semiconductor integrated circuit consisting of four positive-edge-triggered D-type flip flops with common clock and direct reset inputs.

FEATURES

- High-speed: (clock frequency) 60MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2∼6V
- Wide operating temperature range: T_a=−40~+85°C

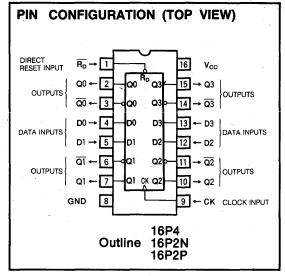
APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC175 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS175.

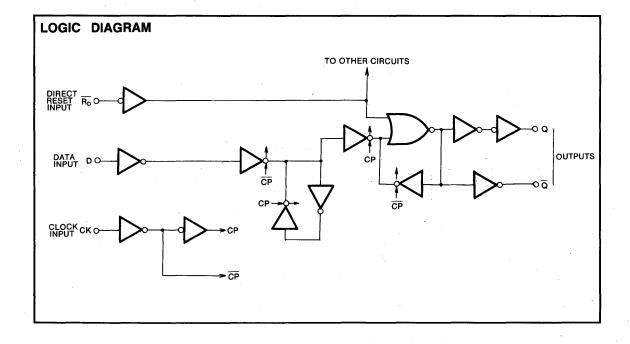
The M74HC175 contains four edge-triggered D-type flip-flops with common direct reset input $\overline{R_D}$ and common clock input CK.



When CK changes from low-level to high-level, the signals just previously input at D appears at outputs Q and \overline{Q} in accordance with the function table given.

When $\overline{R_D}$ is low, output Q and \overline{Q} will become low and high irrespective of other inputs.

When used as a D-type flip flop, $\overline{R_D}$ should be maintained at high-level.





QUADRUPLE D-TYPE FLIP-FLOP WITH COMMON CLOCK AND RESET

FUNCTION TABLE (Note 1)

	Inputs	Outputs			
R _D	СК	D	Q	Q	
Н	Ť	Н	Н	. L	
Н	†	L	L	Н	
Н	↓	×	Q°	Q°	
н	L	Х	Q°	Q°	
L	х	Х	L	н -	

Note 1 : X : Irrelevant

† : Change from low to high

Change from high to low
 Output state Q before clock input changed
 Output state Q before clock input changed

ABSOLUTE MAXIMUM RATINGS $(T_a = -40 \sim +85^{\circ}C)$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V.,
	Input protection diode current	V ₁ < 0V	-20	mA.
l _{IK}	input protection diode current	$V_i > V_{CC}$	20	IIIA
	Output parasitic diode current	V ₀ < 0V	-20	- mA
lok	Output parasitic diode current	Vo > Vcc	20	·ma
lo	Output current per output pin		±25	mA
Icc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		-65~+150	င

Note 2 : M74HC175FP, T $_{\rm a}=-40\sim+70$ °C and T $_{\rm a}=70\sim85$ °C are derated at -6mW/°C. M74HC175DP, T $_{\rm a}=-40\sim+50$ °C and T $_{\rm a}=50\sim85$ °C are derated at -5mW/°C.

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RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85 \%)$

Oursels at			Limits				
Symbol	Pa	Min	Тур	Max	Unit		
Vcc	Supply voltage		2		6	٧	
V,	Input voltage		0		Vcc	V	
Vo	Output voltage		0		Vcc	V	
Topr ·	Operating temperature re	ange	-40		+85	ဗ	
		V _{CC} = 2.0V	0		1000		
t _r , t _f	Input risetime, falitime	$V_{CC} = 4.5V$	0		500	ns	
		V _{CC} = 6.0V	0		400	1	

ELECTRICAL CHARACTERISTICS

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						Limits				
Symbol	Parameter	Test	Test conditions V _{cc} (V)		25℃			-40~+85℃		Unit
					Min	Тур	Max .	Min	Max	:
		V = 0.1V V	$V_0 = 0.1V, V_{CC} = 0.1V$		1.5		1	1.5		
ViH	High-level input voltage	$ I_0 = 20\mu A$			3.15		ľ	3. 15		·V
		1101 — 20µA		6.0	4. 2			4.2		
		V = 0.1V V	_0.11/	2.0			0.5		0.5	
VIL	Low-level input voltage	$ V_0 = 0.1V, V_{CO}$	$V_0 = 0.1V$, $V_{cc} - 0.1V$				1.35		1.35	v
		1101 - 20μΑ		6.0			1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
			$I_{OH} = -20 \mu A$	4.5	4.4			4.4		
V _{OH}	High-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		v
		·	I _{OH} = -4.0mA	4. 5	4.18			4.13		
			I _{OH} = -5. 2mA	6.0	5. 68		,	5.63		
			$I_{OL} = 20 \mu A$	2.0		,	0. 1		0.1	
		•	$I_{OL} = 20 \mu A$	4.5			0. 1		0.1	
VoL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1	Ι,	0.1	·v
			I _{OL} = 4. 0mA	4.5			0.26		0.33	
			I _{OL} = 5. 2mA	6.0			0.26		0.33	
I _{IH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μA
l _{IL}	Low-level input current	V ₁ = 0V		6.0			-0.1		-1.0	μΑ
Icc	Quiescent supply current	VI = VCC, GND	$I_0 = 0\mu A$	6.0			4.0		40.0	μА

SWITCHING CHARACTERISTICS ($v_{cc} = 5v$, $T_a = 25\%$)

Complete	B	Tank and distance		Limits		
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
fmax	Maximum clock frequency		35			MHz
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time				10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = 15pF (Note 4)			25	ns
tpHL	output propagation time (CK-Q, Q)	•			25	ns
t _{PLH}	Low-level to high-level and high-level to low-level				20	ns
t _{PHL}	output propagation time (RD-Q, Q)				20	ns

QUADRUPLE D-TYPE FLIP-FLOP WITH COMMON CLOCK AND RESET

SWITCHING CHARACTERISTICS ($V_{cc} = 2\sim 6V$, $T_a = -40\sim +85^{\circ}C$)

						Limits			
Symbol	Parameter	Test conditions V _{CC} (V)		25℃			-40~+85°C		Unit
				Min	Тур	Max	Min	Max]
3			2.0	6			5		
fmax	Maximum clock frequency		4.5	30			24		MHz
			6.0	35			28		l
			2.0		l	75		95	
t _{TLH}	Low-level to high-level and		4.5			15		19	ns
	high-level to low-level	1.0	6.0			13		16	
	Ingit-level to low-level	[2.0			75		95	
t _{THL}	output transition time		4.5		1	15		19	ns
			6.0			13		16	
		1 .	2.0			150		189	
t _{PLH}	Low-level to high-level and	C _L = 50pF (Note 4)	4. 5			30		38	ns
	high-level to low-level		6. 0			26	1.	32	
	output propagation time		2.0			150		189	
t _{PHL}	(CK - Q, Q)		4.5			30		38	ns
			6.0			26		32	
	1		2.0			125		158	
t _{PLH}	Low-level to high-level and		4.5			25		32	ns
	high-level to low-level		6.0			21		27	
	output propagation time		2. 0			125		158	
t _{PHL}	$(\overline{R_D} - Q, \overline{Q})$		4.5			25		32	ns
			6.0			21		27	
Cı	Input capacitance					10		10	pF
C _{PD}	Power dissipation capacitance (Note 3)		`		52				pF

Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$

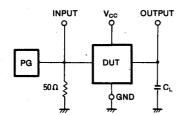
TIMING REQUIREMENTS ($v_{cc} = 2\sim 6V$, $T_a = -40\sim +85^{\circ}C$)

		λ				Limits			
Symbol	Parameter -	Test conditions			25℃		−40 ~	+85℃	Unit
			V _{CC} (V)	Min	Тур	Max	Min	Max	
			2.0	80			101		
tw(ck)	Clock pulse width		4.5	16			20		ns
			6.0	14		-	17		
			2.0	80			101		
$t_{W(\overline{R_D})}$	Direct reset pulse width	·	4.5	. 16			20		ns
.	•		6.0	14			17		
	D and the state of	•	2.0	100	***		126		
tsu	D setup time with		4.5	20			25		ns
	respect to CK		6.0	17			21		
	D hold time with		2.0	5			5		
th			4.5	5			5		ns
	respect to CK	gi	6.0	5	1		5		
			2.0	100			126		
trec	R _D recovery time with	,	4.5	20			25	ĺ	ns
	respect to CK	1	6.0	17			21		

QUADRUPLE D-TYPE FLIP-FLOP WITH COMMON CLOCK AND RESET

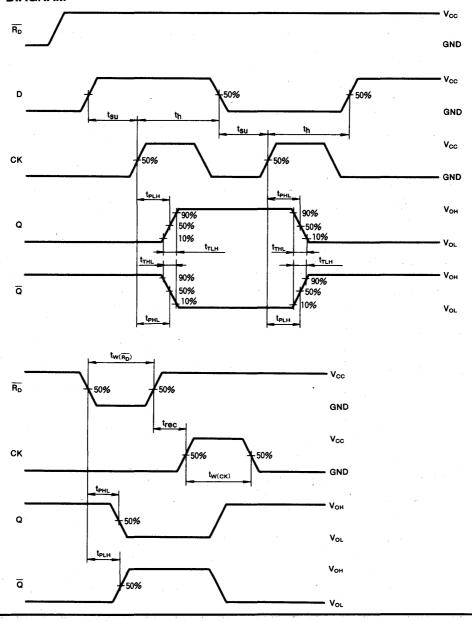
Note 4: Test Circuit

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- (1) The pulse generator (PG) has the following characteristics (10%~90%): t_f = 6ns, t_f = 6ns
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





MITSUBISHI HIGH SPEED CMOS

M74HC190P/FP/DP

PRESETTABLE BCD UP/DOWN COUNTER

DESCRIPTION

The M74HC190 is a semiconductor integrated circuit consisting of a presettable synchronous decimal up/down counter with up/down control input.

FEATURES

- Up/down switching by up/down control input
- High-speed: (clock frequency) 45MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin; 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=-40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

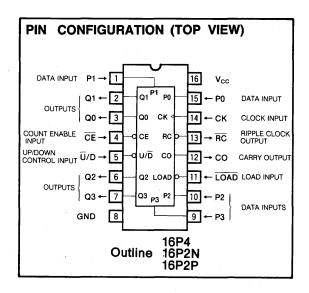
Use of silicon gate technology allows the M74HC190 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS190.

When count enable input \overline{CE} is low and load input \overline{LOAD} is high, and count pulses are applied to clock input CK, the number of count pulses is output at Q0 through Q3 in BCD code in sync with count pulses. The count is incremented when up/down control input \overline{U}/D is low, and decremented when \overline{U}/D is high. The count is enabled when CK changes from low to high.

The preset function operates irrespective of the count pulse. When data is supplied to data inputs P0 through P3 and load input $\overline{\text{LOAD}}$ is low, the signal at P0 through P3 is output at Q0 through Q3 and presets the counter, irrespective of other inputs. When numbers greater than ten are preseted, the counter operates in accordance with the state transition diagram.

The carry output CO becomes high only when 9 appears at Q0 through Q3 during count up and when 0 appears during count down. The ripple clock output \overline{RC} becomes low only when \overline{CE} and CK are both low and when 9 appears at Q0 through Q3 during count up and when 0 appears during count down. \overline{CE} , CO and \overline{RC} are used for a cascade connection.

 $\overline{\text{CE}}$ can be changed from high to low irrespective of CK, but can be changed from low to high only when CK is high. $\overline{\text{U}}/\text{D}$ should be changed only when CK is high.



FUNCTION TABLE (Note 1)

	Inp	outs			Outputs				
LOAD	CE	U/D	CK	Q0	Q1	Q2	Q3		
L	×	Х	Х	P0	P1	P2	P3		
Н	L	L	1	Count	t up				
н	L	Н	†	Count	t down				
н	Н	х	Х	Count	t suppre	ssed			

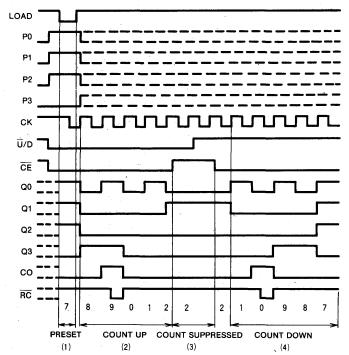
Note 1: † : Change from low to high

X : Irrelevant

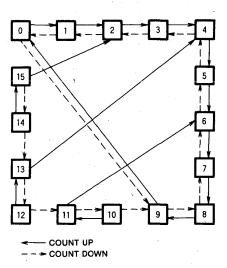
	Inputs							
CE	CO ₍₁₎	СК	RC					
L	Н	L	L					
L	Н	Н	Н					
н	X	Х	Н					
Х	Ľ	Х	Н					

PRESETTABLE BCD UP/DOWN COUNTER

TIMING DIAGRAM



STATE TRANSITION DIAGRAM



The contents of timing diagram

- (1) Preset to 7
- (2) Count up 8, 9, 0, 1, 2
- (3) Count suppressed
- (4) Count down 1, 0, 9, 8, 7



MITSUBISHI HIGH SPEED CMOS

M74HC191P/FP/DP

PRESETTABLE 4-BIT BINARY UP/DOWN COUNTER

DESCRIPTION

The M74HC191 is a semiconductor integrated circuit consisting of a presettable synchronous 4-bit binary (hexadecimal) counter with up/down control input.

FEATURES

- Up/down switching by up/down control input
- Enable input and ripple clock and carry outputs for cascade connection
- Count frequency 40MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

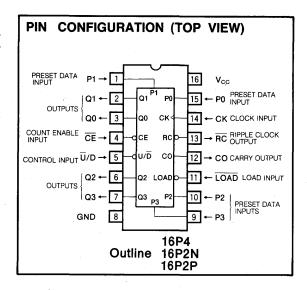
Use of silicon gate technology allows the M74HC191 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS191.

When count enable input \overline{CE} is low and load input \overline{LOAD} is high, and count pulses are applied to clock input CK, the number of count pulses is output at Q0 throgh Q3 in 4-bit binary code in sync with count pulses. The count is incremented when up/down control input \overline{U}/D is low, and decremented when \overline{U}/D is high. The count is enabled when CK changes from low to high.

The preset function operates irrespective of the count pulse. When data is supplied to data inputs P0 through P3 and load input $\overline{\mathsf{LOAD}}$ is set low, the signal at P0 through P3 is output at Q0 through Q3 irrespective of other inputs, and presets the counter.

The carry output CO will become high only when 15_2 appears at Q0 though Q3 during count up and when 0_2 appears duruing count down. The ripple clock output \overline{RC} will becomes low only when \overline{CE} and CK are both low and when 15_2 appears at Q0 through Q3 during count up and when 0_2 appears during count down. \overline{CE} , CO and \overline{RC} are used for a cascade connection.

CE can be changed from high to low irrespective of CK, but can be changed from low to high only when CK is high. \overline{U}/D should be changed only when CK is high.



FUNCTION TABLE (Note 1)

	Inp	outs		Outputs					
LOAD	CE	Ū/D	СК	Q0	Q1	Q2	Q3		
L	Х	X	Х	P0	P1	P2	P3		
н	L	L	†	Coun	t up				
Н	L	н	t	Coun	t down				
н	Н	х	×	Coun	t suppre	ssed	-		

Note 1: † : Change from low to high

X : Irrelevant

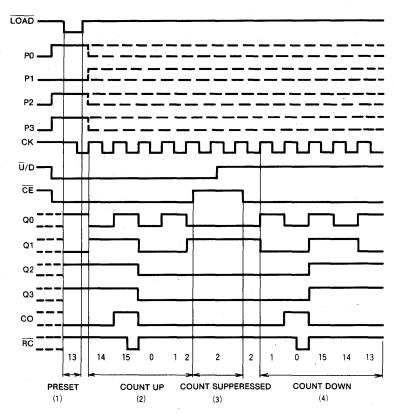
	Inputs		Output	
ČE	CE CO(1) CK			
L	Н	L	L	
L	н	Н	Н	
Н	х	Х	H	
х	L	Х	Н	

(1) Output CO is generated by the following logic equation.

CO=Q0 · Q1 · Q2 · Q3 · (U/D) · · · · · Count up

PRESETTABLE 4-BIT BINARY UP/DOWN COUNTER

TIMING DIAGRAM



The contents of timing diagram

- (1) Preset to 13
- (2) Count up 14, 15, 0, 1, 2
- (3) Count suppressed
- (4) Count down 1, 0, 15, 14, 13



MITSUBISHI HIGH SPEED CMOS

M74HC192P/FP/DP

PRESETTABLE BCD UP/DOWN COUNTER WITH RESET

DESCRIPTION

The M74HC192 is a semiconductor integrated circuit consisting of a synchronous decimal up/down counter with reset and preset inputs.

FEATURES

- High-speed: clock frequency 30MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

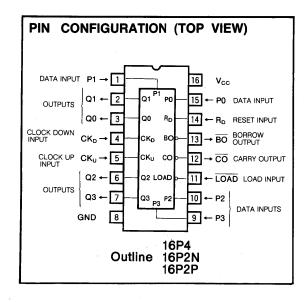
Use of silicon gate technology allows the M74HC192 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS192

The count input consists of independent clock up input CK_U and clock down input CK_D . When load input \overline{LOAD} and CK_D are both high for count up, count pulses are applied to CK_U , and when \overline{LOAD} and CK_U are both high for count down, count pulses are applied to CK_D , and then the number of count pulses is output at Q0 through Q3 in BCD code in sync with the count pulses. The counter is enabled when CK_U or CK_D changes from low to high.

The preset function operates irrespective of the count pulse. When data is pupplied to preset inputs P0 through P3 and load input $\overline{\text{LOAD}}$ is set low, the signal at P0 through P3 is output at Q0 through Q3 and presets the counter, irrespective of CK_{U} and CK_{D} . When the number greater than ten is preset, the counter operates in accordance with the state transition table.

When direct reset input R_{D} is high, the reset function sets Q1 through Q3 low, irrespective of other inputs.

The carry output \overline{CO} will become low only when 9 appears at Q0 through Q3 and CK_U is low during count up. The borrow output \overline{BO} will become low only when 0 appears at Q0 through Q3 and CK_D is low. \overline{CO} and \overline{BO} are connected to CK_U and CK_D in the next state for a cascade connection. (See application examples)



FUNCTION TABLE (Note 1)

			_						
	Inp	uts		Outputs					
RD	LOAD	СКи	CK	QO	Q1	Q2	Q3	co	ВО
Н	х	Х	Х	L	L	L	L	Н	H*
L	L	Х	х	P0	P1	P2	P3	н*	н*
L	Н	Х	Х	Coun	t supp	ressec	ī	н*	н*
L	н	1	Н	Coun	t up			н*	н*
L	Н	Н	1	Coun	t dowr	1		н*	н*

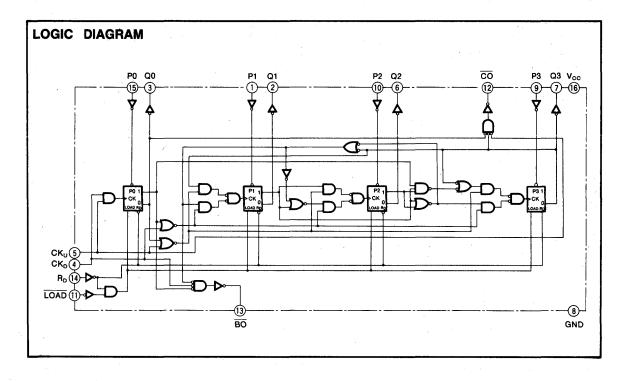
Note 1 : † : Change from low to high

Change from low to high
 Normally set high, but becomes low under the following condition.

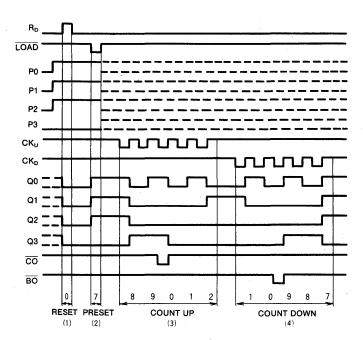
 $\overline{CO} = \overline{Q0 \cdot Q3 \cdot CK_U}$ $\overline{BO} = \overline{Q0 \cdot Q1 \cdot Q2 \cdot Q3 \cdot CK_D}$ Count up $\overline{CO} = \overline{Q0 \cdot Q1 \cdot Q2 \cdot Q3 \cdot CK_D}$ Count down

X : Irrelevant

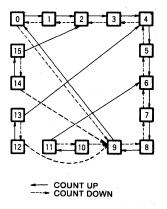
PRESETTABLE BCD UP/DOWN COUNTER WITH RESET



TIMING DIAGRAM



STATE TRANSITION DIAGRAM



PRESETTABLE BCD UP/DOWN COUNTER WITH RESET

ABSOLUTE MAXIMUM RATINGS $(T_a = -40 \sim +85 \degree)$; unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	٧
		V ₁ < 0V	-20	
IIK	Input protection diode current	$V_1 > V_{CC}$	20	mA.
		V ₀ < 0V	20	
Гок	Output parasitic diode current	Vo > Vcc	20	mA mA
l _o	Output current, per output pin		±25	mA
Icc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65~+150	င

Note 2 : M74HC192FP, $T_a=-40\sim+70^\circ\text{C}$ and $T_a=70\sim85^\circ\text{C}$ are derated at -6mW/C. M74HC192DP, $T_a=-40\sim+50^\circ\text{C}$ and $T_a=50\sim85^\circ\text{C}$ are derated at -5mW/C.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85^{\circ}C)$

Oursels at				Limits				
Symbol	Pa	rameter	Min	Тур	Max	Unit		
Vcc	Supply voltage	,	2		6	٧		
V ₁	Input voltage		0		Vcc	٧		
Vo	Output voltage		0		V _{CC}	٧		
Topr	Operating temperature ra	ange	-40		+85	ဗ		
		$V_{CC} = 2.0V$	0		1000			
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns		
		$V_{CC} = 6.0V$	0		400			

ELECTRICAL CHARACTERISTICS

							Limits			
Symbol	Parameter	Test	conditions			25℃		-40~	+85℃	Unit
	<u> </u>		V _{CC} (V)			Тур	Max	Min	Max	1
		V = 0.1V V	0.114	2.0	1.5			1.5		
V_{1H}	High-level input voltage	$V_0 = 0.1V, V_{CC}$;U. I V	4.5	3.15			3.15		V
		1101 - 20µA	$ I_{O} = 20\muA$		4. 2			4.2		
		$V_0 = 0.1V, V_{CC}$	-0.17	2.0			0.5		0.5	
VIL	Low-level input voltage	$ I_0 = 20\mu A$;0.1 v	4. 5			1.35		1.35	V
		1101 — 20µA		6.0			1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
			$I_{OH} = -20\mu A$	4.5	4. 4			4.4		
V_{OH}	high-level output voltage	Vi = ViH, ViL	$I_{OH} = -20\mu A$	6.0	5.9			5.9		ν
		,	$I_{OH} = -4.0 \text{mA}$	4.5	4. 18			4. 13		1
	1		$I_{OH} = -5.2 mA$	6.0	5. 68			5. 63		1
			$I_{OL} = 20 \mu A$	2.0			0. 1		0.1	
			$I_{OL} = 20 \mu A$	4.5			0. 1		0.1	
V_{OL}	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0. 1		0.1	V
			$I_{OL} = 4.0 \text{mA}$	4.5			0.26		0.33]
-			i _{OL} = 5. 2mA	6.0			0.26		0.33	
I _{IH}	High-level input current	V _I = 6V		6.0			0. 1		1.0	μА
I _{IL}	Low-level input current	V ₁ = 0V		6.0			-0.1		-1.0	μA
Icc	Quiescent supply current	$V_1 = V_{CC}$, GND	$I_0 = 0\mu A$	6.0			4.0		40.0	μА

MT4HC192P/FP/DP

PRESETTABLE BCD UP/DOWN COUNTER WITH RESET

SWITCHING CHARACTERISTICS (Voc = 5V, Ta = 25°C)

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Comphal	8	T		Unit		
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
fmax	Maximum clock frequency		20			MHz
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time				10	ns
t _{PLH}	Low-level to high-level and high-level to low-level			* .	26	ns
t _{PHL}	output propagation time (CK _U - CO)				24	ns
t _{PLH}	High-level to low-level output propagation time	0 - 15-5 (Non- 4)			24	ns
t _{PHL}	$(CK_D - \overline{BO})$	C _L = 15pF (Note 4)			24	ns
t _{PLH}	Low-level to high-level and high-level to low-level			1.	- 40	ns
t _{PHL}	output propagation time (CK _U , CK _D — Q0, Q1, Q2, Q3)				52	ns
t _{PLH}	Low-level to high-level and high-level to low-level				42	ns
t _{PHL}	output propagation time (LOAD - Q0, Q1, Q2, Q3)				55	ns
	High-level to low-level output propagation time				47	
t _{PHL}	(R _D - Q0, Q1, Q2, Q3)			1	47	ns

SWITCHING CHARACTERISTICS ($V_{cc} = 2\sim 6V$, $T_a = -40\sim +85^{\circ}C$)

	_					Limits			4
Symbol	Parameter	Test conditions			25℃			+85℃	Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	L
			2.0	3			2.5		
fmax	Maximum clock frequency		4.5	18			14		МН
			6.0	20			16		
			2.0			75		95	
t _{TLH}	Low-level to high-level and		4.5			15		19	ns
	Mak Jairel & January		6.0			13	·	16	
	high-level to low-level		2.0			75		95	
t _{THL}	output transition time		4.5			15		19	ns
		'	6.0			13		16	
		1	2.0			140		175	
t _{PLH}	Low-level to high-level and		4.5			28		35	ns
	high-level to low-level		6.0			24		30	
	output propagation time		2.0		<u> </u>	130		163	
t _{PHL}	(CK _U - CO)	·	4.5			26		33	ns
TENL	()		6.0			22		28	"
		1	2.0			130		163	
t _{PLH}	Low-level to high-level and		4.5			26		33	ns
*PLH	high-level to low-level		6.0			22		28	115
	output propagation time	C _L = 50pF (Note 4)	2.0			130		163	+
	(CK _D — BO)		4.5			26		33	ns
t _{PHL}	(CK) - BO)		6.0			22		28	118
		-	2.0			215		269	-
	Law law law black law at and		1						
t _{PLH}	Low-level to high-level and		4.5			43		54	ns
	high-level to low-level		6.0			37		46	-
_	output propagation time	}	2.0			275		344	
t _{PHL}	(CK _U , CK _D - Q0, Q1, Q2, Q3)	-	4.5			55	-	69	ns
			6.0	,		47		59	1 .
			2.0			230		280	
t _{PLH}	Low-level to high-level and		4.5			46		58	ns
	high-level to low-level		6.0			39		49	<u> </u>
	output propagation time		2.0			290		363	
t _{PHL}	(LOAD — Q0, Q1, Q2, Q3)		4.5	-		58		73	ns
			6.0			49		61	
	High-level to low-level		2.0			265		331	
t _{PHL}	output propagation time		4.5			53		66	ns
	(R _D — Q0, Q1, Q2, Q3)		6.0			45		56	
Cı	Input capacitance				T	10		10	pF
C _{PD}	Power dissipation capacitance (Note 3)								pF

Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$

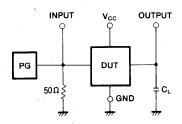


PRESETTABLE BCD UP/DOWN COUNTER WITH RESET

TIMING REQUIREMENTS ($v_{cc} = 2\sim6v$, $\tau_a = -40\sim+85$ °C)

						Limits			
Symbol	Parameter	Test conditions			25℃		−40 ~	+85℃	Unit
	· *	* -	V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0	110			138		
tw(ck)	Clock pulse width		4.5	22		·	28		ns
	•	•	6.0	19			24		
			2.0	100			125		
tw(LOAD)	LOAD pulse width		4.5	20			25		ns
			6.0	17			21		
			2.0	260			325		
t _{W(RD)}	Reset pulse width		4.5	52			65		ns
- -			6.0	45			56		
,			2.0	100			125		
tsu	P setup time with		4.5	20			25		ns
	respect to LOAD		6.0	. 17			22		
	P hold time with		2.0	0			0		
th			4.5	. 0			0	1	ns
	respect to LOAD		6.0	0			0		
	I CAD recovery time with		2.0						
trec(LOAD)	LOAD recovery time with		4.5						ns
	respect to CK		6.0						
	B. racovany time with		2.0	10			10		
trec(RD)	R _D recovery time with		4.5	10			10		ns
-	respect to CK		6.0	10			10		

Note 4: Test Circuit

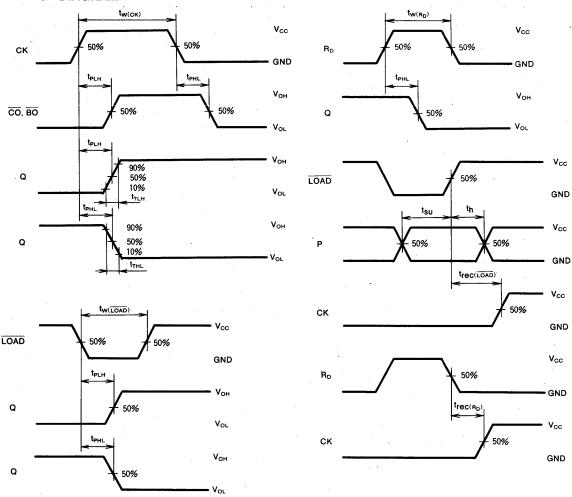


- (1) The pulse generator (PG) has the following characteristics (10%~90%): t_f = 6ns, t_f = 6ns
 (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

PRESETTABLE BCD UP/DOWN COUNTER WITH RESET

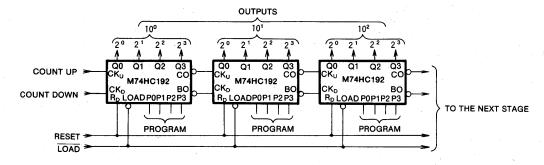
TIMING DIAGRAM

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APPLICATION EXAMPLE

CONFIGURATION OF AN ASYNCHRONOUS BASE 10° COUNTER







MITSUBISHI HIGH SPEED CMOS

M74HC193P/FP/DP

PRESETTABLE 4-BIT BINARY UP/DOWN COUNTER WITH RESET

DESCRIPTION

The M74HC193 is a semiconductor integrated circuit consisting of a synchronous hexadecimal (4-bit binary) up/down counter with reset and preset inputs.

FEATURES

- High-speed: clock frequency 30MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2∼6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC193 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS193.

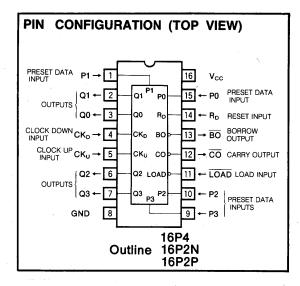
The count input consists of independent clock up input CK_U and clock down input CK_D . When load input \overline{LOAD} and CK_D are both high for count up, count pulses are applied to CK_U , and when \overline{LOAD} and CK_U are both high for count down, count pulses are applied to CK_D , and then the number of count pulses is output at Q0 through Q3 in 4-bit pure binary code in sync with the count pulses. The counter is enabled when CK_U or CK_D changes from low to high.

The preset function operates irrespective of the count pulse. When data is supplied to preset inputs P0 through P3 and load input $\overline{\text{LOAD}}$ is set low, the signal at P0 through P3 is output at Q0 through Q3 and presets the counter, irrespective of CK_U and CK_D.

The reset function sets Q1 through Q3 low, irrespective other inputs when reset input R_{D} is high.

The carry output \overline{CO} will become low only when 15 appears at Q0 through Q3 and CK_U is low during count up. The borrow output \overline{BO} will become low only when 0 appears at Q0 through Q3 and CK_D is low. \overline{CO} and \overline{BO} are connected to CK_U and CK_D in the next stage for a cascade connection.

(See application examples)



FUNCTION TABLE (Note 1)

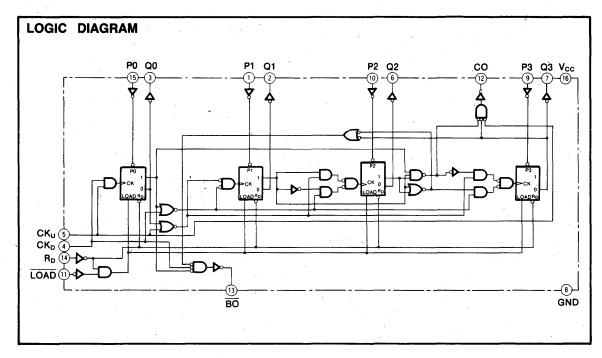
Inputs						Out	puts		
R_D	LOAD	СКи	CK₀	Q	Q1	Q2	Q3	CO	ВО
Н	×	Х	Х	L	L	L	L	Н	н*
L	L	Х	X	P0	P1	P2	P3	H*	Н*
L	Н	Χ.	X	Cou	nt sup	presse	d	Н*	Н*
L	Н	†	Н	Cou	nt up			н*	н*
L	Н	Н	1	Cou	nt dow	'n		н*	н*

Note 1 : † : Change from low to high

* Normally set high, but becomes low under the following condition.

 $\overline{CO} = \underline{Q0 \cdot Q1 \cdot Q2 \cdot Q3 \cdot CK_u} \cdots Count up$ $\overline{BO} = \overline{Q1 \cdot Q1 \cdot Q2 \cdot Q3 \cdot CK_p} \cdots Count down$

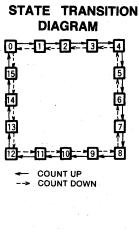
X : Irrelevant



TIMING DIAGRAM LOAD P0 ___ P2 P3 . СКи CK_D Q0 Q1 Q2 _ Q3 \overline{co} BO 15 14 13 15

COUNT UP

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COUNT DOWN

RESET PRESET

ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85 \degree$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	V
V _o	Output voltage	-0.5~V _{cc} +0.5	V	
		V ₁ < 0V	-20	
l _{IK}	Input protection diode current	$V_{l} > V_{CC}$	20	mA
		V ₀ < 0V	-20	
lok	Output parasitic diode current	$V_{o} > V_{cc}$	20	mA
lo	Output current, per output pin		±25	mA
Icc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		-65∼+150	င

Note 2 : M74HC193FP, T $_a=-40\sim+70^\circ$ C and T $_a=70\sim85^\circ$ C are derated at -6mW/°C. M74HC193DP, T $_a=-40\sim+50^\circ$ C and T $_a=50\sim85^\circ$ C are derated at -5mW/°C.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85^{\circ}C)$

Cumbal	Do	rameter		Limits				
Symbol	Pa	rameter	Min	Тур	Max	Unit		
Vcc	Supply voltage		2		6	V		
Vı	Input voltage		0		Vcc	>		
Vo	Output voltage		0		Vcc	· V		
Topr	Operating temperature ra	ange	-40		+85	°C		
		V _{CC} = 2.0V	0	_	1000			
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns		
		$V_{CC} = 6.0V$	0		400			

ELECTRICAL CHARACTERISTICS

					Limits					
Symbol	Parameter	Test	conditions		25℃			-40~+85℃		Unit
-				V _{cc} (V)	Min	Тур	Max	Min	Max	
		$V_0 = 0.1V, V_{C}$	-0.11/	2.0	1.5			1.5		
V _{IH}	High-level input voltage	$ I_0 = 20\mu A$	5-0.1 v	4. 5	3.15			3. 15		V
		1101 - 20AA	6.0		4. 2			4.2		
		$V_0 = 0.1V, V_{CC}$	-0.11/	2.0			0.5		0.5	
VIL	Low-level input voltage	$ V_0 - 0.1V, V_{CO} $ $ I_0 = 20\mu A$		4.5			1.35		1.35	V
		1101 - 20µA	6.0			1.8		1.8		
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
V _{OH}	-		$I_{OH} = -20\mu A$	4. 5	4.4			4.4		
	High-level output voltage	$V_{l} = V_{lH}, V_{lL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		v
			$I_{OH} = -4.0 \text{mA}$	4.5	4.18			4.13		
			$I_{OH} = -5.2 \text{mA}$	6.0	5.68			5.63		
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
			$I_{OL} = 20 \mu A$	4. 5			0. 1		0.1	
VoL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
			I _{OL} = 4.0mA	4.5			0.26		0.33	1
			$I_{OL} = 5.2 mA$	6.0			0.26		0.33	
l _{iH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μΑ
I _{IL}	Low-level input current	V _i = 0V		6.0			-0.1		-1.0	μΑ
lcc.	Quiescent supply current	$V_1 = V_{CC}$, GND, $I_0 = 0\mu A$		6.0			4.0		40.0	μΑ

SWITCHING CHARACTERISTICS $(v_{cc} = 5v, T_a = 25^{\circ}c)$

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Complete	Boundary	Took and distance		Limit		
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
fmax	Maximum clock frequency		20			MHz
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time				10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	7			26	ns
t _{PHL}	output propagation time (CK _U — CO)				24	ns
t _{PLH}	High-level to low-level output propagation time	7			24	ns
t _{PHL}	(CKD - BO)	C _L = 15pF (Note 4)			24	ns
t _{PLH}	Low-level to high-level and high-level to low-level	·.			40	ns
t _{PHL}	output propagation time (CK _U , CK _D — Q0, Q1, Q2, Q3)				52	ns
t _{PLH}	Low-level to high-level and high-level to low-level		-		42	ns
t _{PHL}	output propagation time (LOAD - Q0, Q1, Q2, Q3)				55	ns
	High-level to low-level output propagation time	7			47	ns
t _{PHL}	(R _D - Q0, Q1, Q2, Q3)	· · · · · · · · · · · · · · · · · · ·			٦′.	115

SWITCHING CHARACTERISTICS ($v_{cc} = 2\sim 6v$, $t_a = -40\sim +85$ °C)

	·				'	Limits			Unit
Symbol	Parameter	Test conditions			25℃		-40~	+85℃	
			V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0	3			2.5		
fmax	Maximum clock frequency		4.5	18			14		MHz
	· ·		6.0	20			16		
			2.0			75		95	
t _{TLH}	Low-level to high-level and		4.5	İ		15		19	ns
	Note to a to the town	•	6.0	ļ		13		16	
	high-level to low-level		2.0			75		95	
t _{THL}	output transition time		4.5	ļ		15		19	กร
			6.0			13		16	
			2.0			140		175	
t _{PLH}	Low-level to high-level and		4.5			28		35	ns
	high-level to low-level	ı	6.0	1		24	}	30	
	output propagation time		2.0			130		163	
t _{PHL}	(CK _U - CO)		4.5	}	1	26		33	ns
			6.0			22		- 28	
			2.0		1	130		163	
t _{PLH}	Low-level to high-level and		4.5			26		33	ns
	high-level to low-level	(6.0	1	1	22]	28	Ì
	output propagation time	$C_L = 50pF (Note 4)$	2.0			130		163	
t _{PHL}	(CK _D - BO)		4.5	ì	1	26	Ì	33	ns
			6.0			22	ļ	28	
			2.0			215		269	
t _{PLH}	Low-level to high-level and		4.5			43	l	54	ns
	high-level to low-level		6.0			37		46	
	output propagation time		2.0			275		344	
t _{PHL}	(CKu, CKp - Q0, Q1, Q2, Q3)		4.5			55		69	ns
			6.0			47	1	59	}
			2.0			230		280	
t _{PLH}	Low-level to high-level and		4.5	1	1	46	1	58	ns
	high-level to low-level		6.0			39		49	
	output propagation time	**	2.0	1		290		363	T
t _{PHL}	(LOAD - Q0, Q1, Q2, Q3)		4.5			58		73	ns
		W - C	6.0			49		61	
	High-level to low-level		2. 0			265		331	
t _{PHL}	output propagation time	·	4. 5			53		66	ns
	(R _D - Q0, Q1, Q2, Q3)		6.0			45		56	
C _I	Input capacitance		1.	<u> </u>	1	10		10	pF
C _{PD}	Power dissipation capacitance (Note 3)		+	 			T	· · · ·	pF

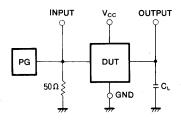
Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$



TIMING REQUIREMENTS ($v_{cc} = 2\sim 6v$, $T_a = -40\sim +85$ °C)

						Limits			
Symbol	Parameter	Test conditions			25℃		-40~	+85°C	Unit
		·	V _{CC} (V)	Min	Тур	Max	Min	Max	İ
			2.0	110			138		
tw(ck)	Clock pulse width		4.5	22			28		ns
			6.0	19			24		
			2.0	100			125		
tw(LOAD)	LOAD pulse width		4.5	20			25	}	ns
		,	6.0	17			21		
			2.0	130			163		
$t_{W(R_D)}$	Reset pulse width		4.5	26			33	1	ns
-			6.0	22			28		
			2.0	100			125		
tsu	P setup time with	· ·	4.5	20			- 25		ns
	respect to LOAD	·	6.0	17			22	1	
	P hold time with		2.0	0			0		
th			4.5	0.			0		ns
	respect to LOAD		6.0	0	· .		0		
	I CAR		2.0						
trec(LOAD)	LOAD recovery time with		4.5		1	-			ns
	respect to CK		6.0						
	B recovery time with	,	2.0	10			10		
trec(RD)	R _D recovery time with		4.5	10			10		ns
•	respect to CK		6.0	10			10		

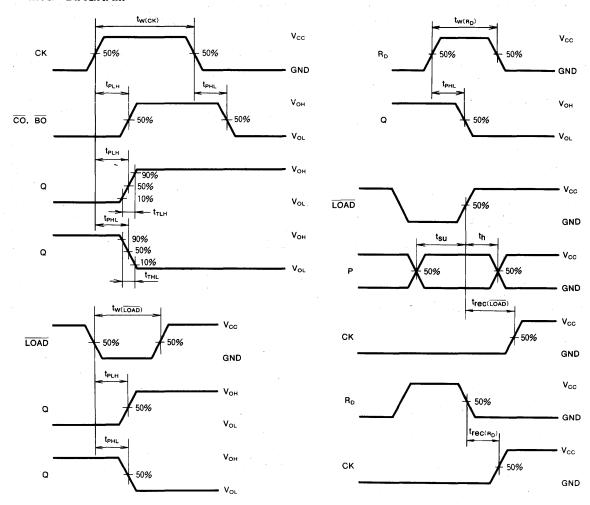
Note 4: Test Circuit

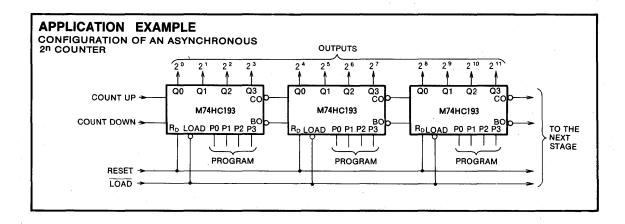


- (1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
 (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM

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MITSUBISHI HIGH SPEED CMOS

M74HC194P/FP/DP

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

DESCRIPTION

The M74HC194 is a semiconductor integrated circuit consisting of a 4-bit bidirectional serial/parallel-input serial/parallel-output shift register with direct reset input.

FEATURES

- High-speed: 50MHz clock frequency typ.
 (C_I=15pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2∼6V
- Wide operating temperature range: T_a=-40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

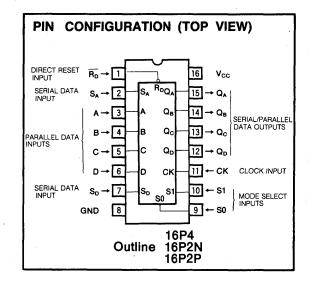
Use of silicon gate technology allows the M74HC194 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS194.

This device is usable as a serial input-serial/parallel output and parallel input-serial/parallel output shift register will the mode select inputs S0 and S1.

When S0 is maintained high and S1 is low, serial data supplied at serial data input S_A will be shifted sequentially to outputs Q_A through Q_D in synchronous with the clock pulse applied at clock input CK. When S0 is maintained low and S1 is high, serial data supplied at serial data input S_D will be shifted sequentially to outputs Q_D through Q_A in synchronous with the clock pulse applied at CK.

When S0 and S1 are both maintained high, parallel data supplied at inputs A through D are simultaneously shifted to Q_A through Q_D by a single clock pulse. When S0 and S1 are both maintained low, none of the flip flops will change state, even if clock pulse is applied at CK.

Left-shift, right-shift and parallel data reading operation take place when the clock pulse changes from low to high. When the direct reset input $\overline{R_D}$ is low, Q_A through Q_D will become low, irrepsective of other inputs.



FUNCTION TABLE (Note 1)

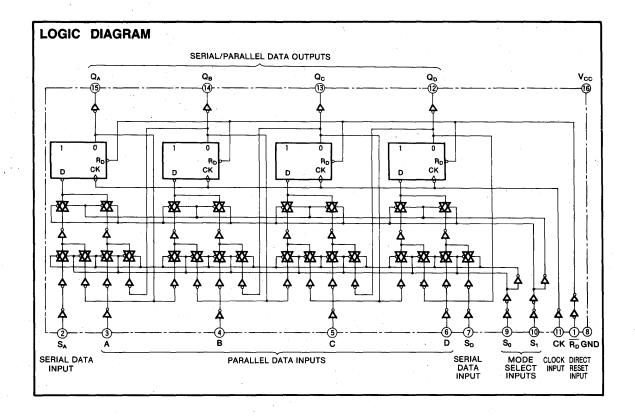
	_			_										
Operating				Input	S			Outputs						
mode	R	S0	S1	СК	SA	SD	A~D	QA	QB	Qc	QD			
Reset	L	Х	х	Х	Х	Х	Х	L	L	L	L			
Right shift	Н	Н	L	†	L	х	х	L	QÃO	Q _B ⁰	Q _C º			
	Н	Н	L	†	Η.	·X	х	Н	Q _A ⁰	QBo	Qcº			
Left-shift	Н	L	Н	1	Х	L	Х	Q _B ⁰	Q _C º	Q _D º				
Leit-Sillit	Н	L	Н	1	Х	Н	Х	Q _B ⁰	Qcº	Q _D ⁰	Н			
Parallel read	Н	Н	Н	†	Х	х	A~D	Α	В	C	D			
Clock inhibit	Н	L	L	Х	Х	Х	х	Q_A^0	Q _B ⁰	Q _C º	å			

Note 1: † : Change from low to high

X : Irrelevant

Q0 : Output state of Q before clock input changed

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER



ABSOLUTE MAXIMUM RATINGS $(\tau_a = -40 \sim +85^{\circ}C)$, unless otherwise noted)

医对动物 医网络海绵属 胸腺 经收益的经济 医抗毒酸

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage		<i>−</i> 0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	. V
	land and add and and a	V ₁ < 0V	-20	
ıĸ	Input protection diode current	$V_{l} > V_{CC}$	20	mA
	Outrant - markle disable - mark	V ₀ < 0V	-20	
lok	Output parasitic diode current	V _o > V _{cc}	20	mA
lo	Output current per output pin		±25	mA
loc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼ +150	℃ .

Note 2 : M74HC194FP, $T_a = -40 \sim +70 ^{\circ} C$ and $T_a = 70 \sim 85 ^{\circ} C$ are derated at $-6 mW/^{\circ} C$. M74HC194DP, $T_a = -40 \sim +50 ^{\circ} C$ and $T_a = 50 \sim 85 ^{\circ} C$ are derated at $-5 mW/^{\circ} C$.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85 \degree C)$

Combal	Do	rameter		Limits					
Symbol	Pa	rameter	Min	Тур	Max	Unit			
Vcc	Supply voltage		2		6	V			
Vı	Input voltage		0		V _{CC}	V			
Vo	Output voltage		0		Vcc	٧			
Topr	Operating temperature ra	ange	-40		+85	ဗ			
		$V_{CC} = 2.0V$	0		1000				
tr, tf	Input risetime, falltime	$V_{CC} = 4.5V$. 0		500	ns			
		$V_{CC} = 6.0V$. 0		400				



M74HC194P/FP/DP

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

ELECTRICAL CHARACTERISTICS

					Limits					
Symbol	Parameter	Test	conditions		25℃			-40~+85°C		Unit
				V _{cc} (V)	Min	Тур	Max	Min	Max	
		$V_0 = 0.1V, V_{00}$	_0 1v	2.0	1.5			1.5		
V _{IH}	High-level input voltage	$ I_0 = 20\mu A$		4.5	3.15			3.15		V .
		1101 - 20µA		6.0	4.2			4.2		
		$V_0 = 0.1V, V_{00}$	_0.11/	2.0			0.5		0.5	
VIL	Low-level input voltage	$ V_0 = 20 \mu A$;—0. 1 V	4.5			1.35		1.35	V
		$ 1_0 = 20\mu\text{A}$		6.0			1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		-
			$i_{OH} = -20\mu A$	4.5	4. 4		ŀ	4.4		
VoH	High-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9	1		5.9		v
,			$I_{OH} = -4.0 \text{mA}$	4.5	4.18			4.13		
			$I_{OH} = -5.2 \text{mA}$	6.0	5. 68	ı		5.63		
			$I_{OL} = 20\mu A$	2.0			0.1		0.1	
			$I_{OL} = 20 \mu A$	4.5		į	0.1	-	0.1	
VoL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
			I _{OL} = 4.0mA	4.5			0.26		0.33	
			I _{OL} = 5. 2mA	6.0			0.26		0.33	
l _{iH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μА
I _{IL}	Low-level input current	$V_1 = 0V$		6.0		5	-0.1		-1.0	μА
Icc	Quiescent supply current	VI = VCC, GND	$I_0 = 0\mu A$	6.0			4. 0		40.0	μΑ

SWITCHING CHARACTERISTICS ($v_{cc} = 2\sim 6V$, $T_a = -40\sim +85$ °C)

Cumbal	Danamatan	Tank and distance		11-14		
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
fmax	Maximum clock frequency		35			MHz
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time	0 = 15-5 (N-1-4)			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = 15pF (Note 4)			24	ns
t _{PHL}	output propagation time (CK - Q)				24	ns
t _{PHL}	High-level to low-level output propagation time $(\overrightarrow{R_D} - Q)$				25	ns

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

SWITCHING CHARACTERISTICS ($V_{cc} = 2\sim6V$, $T_a = -40\sim+85^{\circ}C$)

						Limits			Unit
Symbol	Parameter	Test conditions			25℃		-40~	+85℃	
			V _{cc} (V)	Min	Тур	Max	Min	Max	}
			2.0	6			5		
fmax	Maximum clock frequency		4.5	30	1	1	24	1	MHz
			6.0	35			28		
			2.0			75		95	
tTLH	Low-level to high-level and		4.5		·	15		19	ns
	1	· V	6.0		'	13		16	١.
	high-level to low-level		2.0			75		95	
t _{THL}	output transition time		4.5		1	15	1	19	ns
		0 50.5 (1) (1)	6.0			13		16	
		C _L = 50pF (Note 4)	2.0		-	145		183	
t _{PLH}	Low-level to high-level and		4.5			29		37	ns ns
	high-level to low-level		6.0	_	Ì	25	\ 	31	1
	output propagation time		2, 0			145		183	
t _{PHL}	(CK - Q)	A STATE OF THE STA	4.5			29	1	37	ns
			6.0			25		31	ł
	High-level to low-level	0.89	2.0			150		189	
t _{PHL}	output propagation time		4.5		ĺ	30		38	ns
	$(\overline{R_D} - Q)$		6.0			26)	32	1
Cı	Input capacitance					10		10	pF
CPD	Power dissipation capacitance (Note 3)				127				pF

Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.

The power dissipated during operation under no-load conditions is calculated using the following formula:

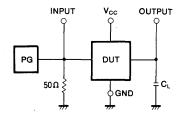
P_D = C_{PD} · V_{CC}² · f₁+I_{CC} · V_{CC}

TIMING REQUIREMENTS ($V_{cc} = 2\sim 6V$, $T_a = -40\sim +85$ °C)

		,				Limits			
Symbol	Parameter	Test conditions			25℃		-40~	+85℃	Unit
			Vcc(V)	Min	Тур	Max	Min	Max	Ì
			2.0	80			101		
tw	CK, RD Clock pulse width		4.5	16	}		20		ns
		·	6.0	14		İ	17		
	A, B, C, D setup time with		2.0	100	}		126		
tsu	respect to CK		4.5	20			25		ns
	respect to CK		6.0	17			21		
	S0, S1, setup time with	*	2.0	100			126		
t _{su}	respect to CK	and the second s	4.5	20	1	1	25	1	ns
	respect to CK		6.0	17			21		
	S _A , S _D setup time with		2.0	100	-		126		
t _{su}	respect to CK		4.5	20	1		25		ns
	respect to CK	**	6.0	17	İ		21		
	A, B, C, D hold time with		2.0	0			0		
th	respect to CK		4.5	0		} .	0		ns
	respect to CK		6.0	0			0		
,	S0, S1 hold time with		2.0	0			0		
th	respect to CK		4.5	-0			0	-	ns
	respect to CK		6.0	0		l	0		
	S _A , S _D hold time with		2.0	0			0		
th	respect to CK	Į.	4.5	.0		[0	1	ns
	respect to CK		6.0	0			0		
	R _D recovery time with		2.0	5			5		
trec	respect to CK		4.5	5	}		5		ns
	respect to CK		6.0	5	1	1	. 5		}

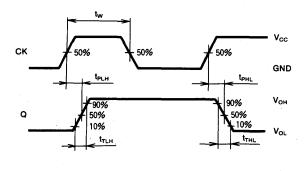
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

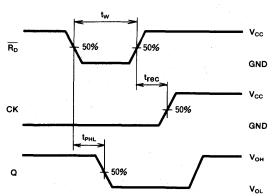
Note 4: Test Circuit

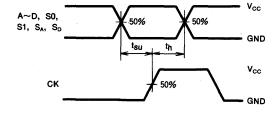


- (1) The pulse generator (PG) has the following characteristics (10% \sim 90%): $t_f = 6ns$, $t_f = 6ns$
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM







MITSUBISHI HIGH SPEED CMOS

M74HC195P/FP/DP

4-BIT UNIVERSAL SHIFT REGISTER

DESCRIPTION

The M74HC195 is a semiconductor integrated circuit consisting of a 4-bit serial/parallel-input serial/parallel-output shift register with direct reset input.

FEATURES

- High-speed: 50MHz clock frequency typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

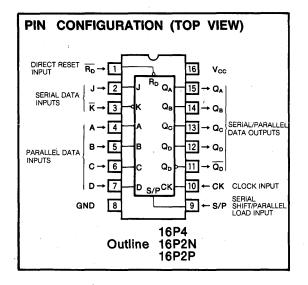
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC195 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS195.

This device is usable as a serial input- serial/parallel output and parallel input- serial/parallel output shift register with the serial shift/parallel load input S/P. When S/P is maintained high, serial data supplied at serial data inputs J and \overline{K} will be shifted sequentially to serial/parallel outputs Q_A through Q_D in synchronous with the clock pulse supplied at clock input CK. The first stage flip flop at J and \overline{K} functions as a J- \overline{K} flip flop. When serial data is supplied from one line, J and \overline{K} are connected and function as a serial input pin. When S/P is maintained low, parallel data supplied at parallel data inputs A through D will be output at Q_A through Q_D by a single clock pules applied at CK. The shift or parallel reading operation take place when CK changes from low to high.

The last-stage flip flop has complementary outputs \mathbf{Q}_D and $\overline{\mathbf{Q}}_D.$

When direct reset input R_D is low, Q_A through Q_D will become low and \overline{Q}_D will become high, irrespective of other inputs.



FUNCTION TABLE (Note 1)

Operating		Inputs						Outputs						
mode	СК	R _D	S/P	J	K	A~D	QA	QB	Qc	Qp	QD			
Reset	Х	L	Х	Х	Х	Х	L	L	L	L	Н			
	t	Н	Н	Н	Н	х	Н	Q _A o	Q _B ⁰	Q _C ⁰	Qc			
Disks skip	t	Н	н	L	L	Х	L	Q _A ⁰	Q _B ⁰	Q _C ⁰	Qc			
Right shift	†	Н	Н	Н	L	Х	Q_A^0	QAO	Q _B ^o	Q _C ⁰	Qc			
	t	Н	Н	L	Н	Х	Q _A ⁰	Q _A o	Q _B ⁰	Qcº	Qc			
Parallel read	1	Н	L	Х	Х	A~D	Α	В	С	D	D			

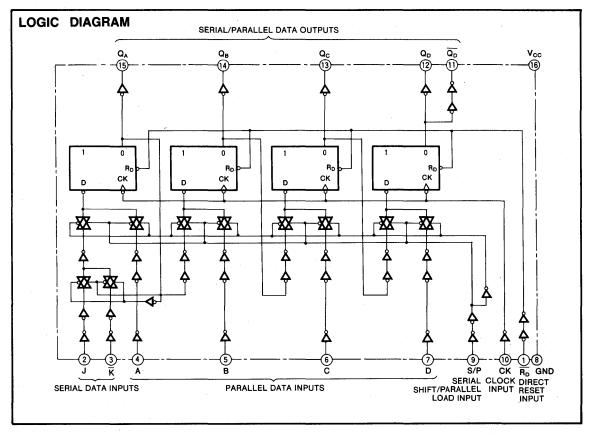
Note 1: † : Change frome low to high

X : Irrelevant

Q0 : Output state of Q before clock input changed

Q0 : Output state of Q before clock input changed

4-BIT UNIVERSAL SHIFT REGISTER



ABSOLUTE MAXIMUM RATINGS $(\tau_a = -40 \sim +85 \degree\text{C}, \text{ unless otherwise noted})$

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
V _I	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
	1	V ₁ < 0V	-20	
lik	Input protection diode current	$V_{i} > V_{CC}$	20	mA
		V ₀ < 0V	-20	
lok	Output parasitic diode current	$V_{\rm o} > V_{\rm cc}$	20	mA
lo	Output current per output pin		±25	mA
Icc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		-65~+150	°C

Note 2 : M74HC195FP, $T_a=-40\sim+70^\circ$ C and $T_a=70\sim85^\circ$ C are derated at -6mW/°C. M74HC195DP, $T_a=-40\sim+50^\circ$ C and $T_a=50\sim85^\circ$ C are derated at -5mW/°C.

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85\%)$

0	B -	Parameter		Limits					
Symbol	Pa	rameter	Min	Тур	Max	Unit			
Vcc	Supply voltage		2		6	٧			
V,	Input voltage	0		Vcc	٧				
V _o	Output voltage	Output voltage			Vcc	٧			
Topr	Operating temperature ra	ange	-40		+85	ဗ			
	,	V _{CC} = 2.0V	0		1000				
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns			
		$V_{CC} = 6.0V$	0		400				

M74HC195P/FP/DP

4-BIT UNIVERSAL SHIFT REGISTER

ELECTRICAL CHARACTERISTICS

李蔚 从 医 位置虚印度 (Jing bi) 1 (4) 中国公安等1566

							Limits			j
Symbol	Parameter	Test	conditions			25℃		-40~	+85°C	Unit
	†			V _{cc} (V)	Min	Тур	Max	Min	Max	1
				2.0	1.5			1.5		
V _{IH}	High-level input voltage	$V_0 = 0.1V$, V_{cc}	c0.1V	4.5	3.15		100	3. 15	İ	- v
		$ I_0 = 20\mu A$		6.0	4.2			4.2	ļ	ĺ
		N - 0 111 11	0.114	2.0			0.5		0.5	
VIL	Low-level input voltage	$V_0 = 0.1V$, V_{cc}		4.5			1.35		1.35	V
		$ I_0 = 20\mu A$		6.0			1.8		1.8	
			$I_{OH} = -20 \mu A$	2.0	1.9			1.9		
			$I_{OH} = -20\mu A$	4.5	4.4			4.4		
VoH	High-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OH} = -20\mu A$	6.0	5. 9			5.9		V
		100	$I_{OH} = -4.0 \text{mA}$	4.5	4.18			4.13		1
			$I_{OH} = -5.2 \text{mA}$	6.0	5.68			5.63		
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
			$I_{OL} = 20 \mu A$	4.5			0.1		0.1	
VoL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
			I _{OL} = 4.0mA	4.5			0.26		0.33	
		-	$I_{OL} = 5.2 \text{mA}$	6.0			0.26	[0.33	
I _{IH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μА
I _{IL}	Low-level input current	V ₁ = 0V	V ₁ = 0V				-0.1		-1.0	μΑ
lcc	Quiescent supply current	VI = VCC, GND	$I_0 = 0\mu A$	6.0			4.0		40.0	μΑ

SWITCHING CHARACTERISTICS $(v_{cc} = 5v, T_a = 25^{\circ})$

O b!		T-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1		Unit		
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
fmax	Maximum clock frequency		35			MHz
t _{TLH}	Low-level to high-level and high-level to low-level	1			10	ns
t _{THL}	output transition time	·			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level				24	ns
t _{PHL}	output propagation time (CK — Q)	C _L = 15pF (Note 4)			24	ns
t _{PLH}	Low-level to high-level and high-level to low-level				24	ns
tpHL	output propagation time (CK — QD)				24	ns
t _{PHL}	High-level to low-level output propagation time $(\overline{R_D} - Q)$				25	ns
t _{PHL}	High-level to low-level output propagation time $(\overline{R_D} - \overline{Q_D})$				25	ns

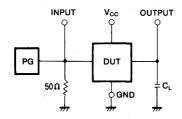
4-BIT UNIVERSAL SHIFT REGISTER

SWITCHING CHARACTERISTICS $(v_{cc} = 2\sim6v, \tau_a = -40\sim+85^{\circ}C)$

						Limits			
Symbol	Parameter	Test conditions			25℃		-40~	+85℃	Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max]
			2.0	. 6			5		
fmax	Maximum clock frequency		4.5	30			24	ŀ	MHz
			6.0	35		ŀ	28		
		1	2.0			75		95	
t _{TLH}	Low-level to high-level and		4.5			15		19	ns
	blab land to land		6.0			13		16	
	high-level to low-level		2.0			75		95	
t _{THL}	output transition time		4.5			15		19	ns
			6.0			13		16	
		1	2.0			145		183	
t _{PLH}	Low-level to high-level and		4.5			29		37	ns
	high-level to low-level		6.0			25		31	
·	output propagation time	·	2.0			145		183	
t _{PHL}	(CK - Q)	C _L = 50pF (Note 4)	4.5			29		37	ns
		200	6.0			25		31	
			2.0			145		183	
t _{PLH}	Low-level to high-level and		4.5			29		37	ns
	high-level to low-level		6.0			25		31	
	output propagation time		2.0			145		183	
t _{PHL}	(CK - QD)		4.5	-		29		37	ns
		-	6.0			25		31	
	High-level to low-level		2.0			150		189	
t _{PHL}	output propagation time		4.5			30		38	ns
	$(\overline{R_D} - Q)$		6.0			26		32	
	High-level to low-level	1	2.0			150		189	
t _{PHL}	output propagation time		4.5	1		30		38	ns
	$(\overline{R_D} - \overline{Q_D})$		6.0			26		32	1
Cı	Input capacitance					10		10	pF
C _{PD}	Power dissipation capacitance (Note 3)				152				pF

Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot v_{CC}^2 \cdot f_i + I_{CC} \cdot v_{CC}$

Note 4: Test Circuit

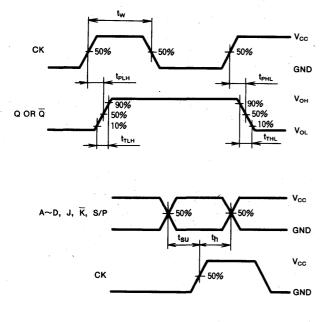


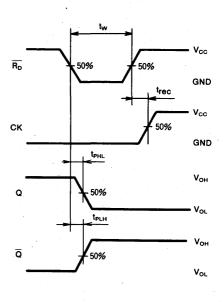
- (1) The pulse generator (PG) has the following characteristics (10%~90%): $\rm t_f=6ns, \ t_f=6ns$
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

4-BIT UNIVERSAL SHIFT REGISTER

TIMING REQUIREMENTS ($v_{cc} = 2\sim 6V$, $T_a = -40\sim +85^{\circ}C$)

		***				Limits			
Symbol	Parameter	Test conditions			25℃		−40~	+85℃	Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	_
			2.0	80			101		
tw	CK, RD clock pulse width		4.5	16			20		ns
			6.0	14			17		
	A, B, C, D setup time with		2.0	100			126		
tsu	1 ' ' ' '		4.5	20		ļ	25		ns
ı	respect to CK		6.0	. 17			21	Ì . ·	
	J, K setup time with		2.0	100			126		
t _{su}			4.5	20			25	}	ns
	respect to CK		6.0	17			21		
	S/P setup time with		2.0	100		-	126		
tsu	respect to CK		4.5	20			. 25		ns
	respect to CK		6.0	17	-		21		
	A, B, C, D hold time with		2. 0	0			0		
th	respect to CK	`	4.5	0	/		0		ns
	respect to CK		6.0	0			0		
	J, K hold time with		2.0	0,			0		
th	respect to CK	1.	4.5	0			0		ns
	respect to CK		6.0	0			0		_
	S/P hold time with		2.0	0			. 0		
th	respect to CK		4.5	0			0		ns
	respect to CK	·	6.0	0			0		
-	R _D recovery time with		2.0	5			5		
trec	respect to CK		4.5	5]	1	5		ns
	leshect to CV	,	6.0	. 5	1		5		1







MITSUBISHI HIGH SPEED CMOS

M74HC221P/FP/DP

DUAL MONOSTABLE MULTIVIBRATOR

DESCRIPTION

The M74HC221 is a semiconductor integrated circuit consisting of two monostable multivibrators with direct reset inputs.

FEATURES

- Direct reset input can interrupt output pulses.
- High-speed: 28ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2∼6V
- Wide operating temperature range: T_a=-40~+85℃

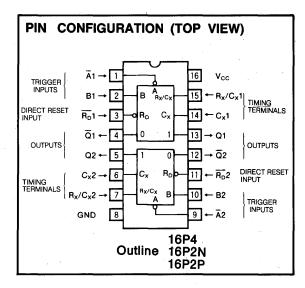
APPLICATION

General purpose, for use in industrial and consumer digital equipment.

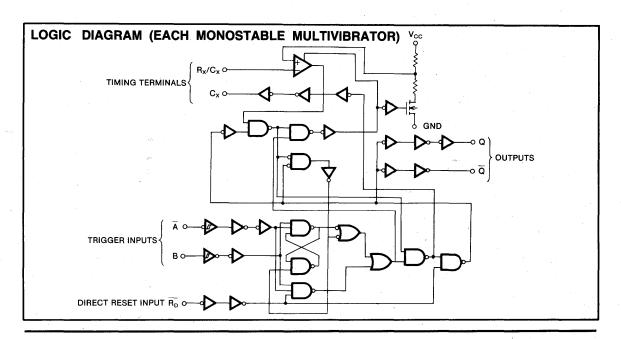
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC221 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS221.

When external resistor R_X and electrostatic capacitor C_X are connected to timing terminals R_X/C_X and C_X as shown in Fig. 1, and trigger pulses are applied at input \overline{A} or B, positive pulses will appear at Q and negative pulses, at \overline{Q} . (Fig.2-(a)) The pulse width t_{WQ} is set by R_X and C_X . The trigger is applied when \overline{A} changes from high-level to low-level or when B changes from low-level to high-level.



When direct reset input $\overline{R_D}$ is low, Q will be reset low and \overline{Q} will be reset high, irrespective of the output state, allowing output pulses to be narrower by $\overline{R_D}$. (Fig.2-(b)). When $\overline{R_D}$ changes from low-level to high-level while \overline{A} is low and B is high, the trigger is applied and Q and \overline{Q} change state.





FUNCTION TABLE (Note 1)

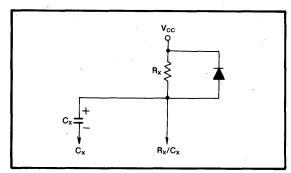
	Inputs	Outputs				
R _D	Ā	В	Q	ā		
L	×	×	L	Η,		
×	н	×	L	Н		
x	X	L	L	Н		
н.	L	f	Л			
Н	.	н	Π	T U		
†	L	Н	Π	11		

- Note 1: † : Change from low to high level
 - 1 : Change from high to low level ☐ : Positive one-shot operation
 -] [: Negative one-shot operation
 - X : Irrelevant

OPERATION

How to use the timing terminals

Resistor R_X and capacitor C_X are connected to timing terminals R_X/C_X and C_X , as shown in Fig. 1. If C_X is polar, the positive lead should be connected to the Rx/Cx side, and the negative lead to the Cx side. A diode is connected to prevent latchup.



Connection of external resistor Rx and Flg.1 capacitor C_X to timing terminals R_X/C_X and C_X

2. Output pulse width two

The output pulse width two is determined as follows: when $C_x > 100000pF$, $R_x \ge 10k\Omega$ $t_{WQ}=0.46C_X \cdot R_X (ns)$ C_X is given in pF, and R_X in $k\Omega$.

Output pulse width control

The output pulse width is controlled in the following two ways.

3-1 Normal use

Fig.2-(a) is the directions as ordinary monostable multivibrator operation and the output pulse width $t_{\text{WQ}}\ \text{can}\ \text{be}\ \text{set}$ by using the formula and figure shown in section 2 above. 3-2 Shortening of the output pulse width with $\overline{R_D}$ signal As shown in Fig.2-(b), the output pulse which has been generated by the trigger'signal can be terminated with the R_D signal and it is possible to shorten its width as required.

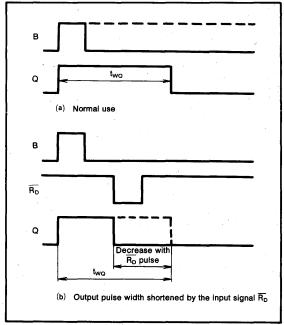


Fig.2 Output pulse width control

4. Precautions for use

- 4-1 The lead lengths of external resistor $R_{\rm X}$ and capacitor Cx should be as short as possible (less than 3cm) to minimize stray wiring capacitance and to prevent misoperation due to noise. Care should also be taken to isolate this circuit from noise sources as far as possible.
- 4-2 Insert a capacitor of $0.01 \sim 0.1 \mu F$ with good highfrequency characteristics between V_{CC} and GND.
- 4-3 Output pulses may be generated when power is switched on.
- 4-4 Capacitor discharge when the power is turned off may cause thermal breakdown or latchup, so a diode should be connected as shown in Fig. 1.

M74HC237P/FP/DP

1-OF-8 DECODER/DEMULTIPLEXER WITH ADDRESS LATCH

DESCRIPTION

The M74HC237 is a semiconductor integrated circuit consisting of a 3-bit binary to 8-line decoder/demultiplexer with address latch.

FEATURES

- Built-in address latch
- High-speed: 18ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=-40~+85℃

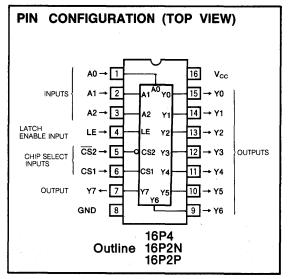
APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC237 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS237.

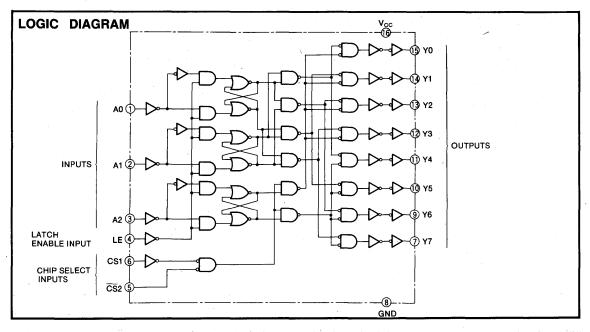
The M74HC237 consists of a 3-bit binary to 8-line decoder/demultiplexer with an address latch to store the signals of inputs A0 through A2. When latch-enable input LE is low, a 3-bit binary code, applied to inputs A0 through A2, goes through the latch and becomes the decoder input signal. In this case, the output Y0 through Y7 corresponding to this value will become high and other outputs will all become



low. When LE is high, the A0 through A2 signals existing immediately prior to the high-level setting will be stored in the latch. In this case, those stored contents will not change even if A0 through A2 are changed.

In this case, chip select inputs CS1 and $\overline{\text{CS2}}$ should be maintained at high and low, respectively. When CS1 and $\overline{\text{CS2}}$ are in conditions other than those given above, all outputs will become low.

When operated as a 1-of-8 demultiplexer, CS1 or $\overline{\text{CS2}}$ is used as a data input and A0 through A2 are used as the selecting inputs.



1-0F-8 DECODER/DEMULTIPLEXER WITH ADDRESS LATCH

FUNCTION TABLE (Note 1)

		Inp	uts						Out	puts			
LE	CS1	CS2	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
×	X	Н	X	Х	X	L	L	L	L	L	L	L	L
Х	L	Х	Х	х	Х	L	L	L	L	L	L.	L	L
L	Н	L	L	L	L	н	L	L	L	L	L	L	Ŀ
L	Н	L	L	L	Н	L	н	L	L	L	L	L	L
L	Н	L	L	Н	L	L	L	Н	L	L	L	L	L
L	Н	L	Ŀ	H	Н	L	L	L .	Н	L	L	L	L
L	Н	L	Н	L	L	L	L	L	L	Н	L	L	L
L	Н	L	. H	L	Н	L	L	L	L	L	Н	L	L
L	Н	L	Н	Н	L	L	L	L	Ĺ	L	L	Н	L
L	Н	L	Н	Н	Н	L	L	L	L	L	L	L	н
Н	Н	L	×	Х	X	Y0º	Y10	Y20	Y30	Y40	Y5°	Y6°	Y7º

Note 1: X: Irrelevant

Yº: Output state Y before LE changed to high

ABSOLUTE MAXIMUM RATINGS $(\tau_a = -40 \sim +85^{\circ}\text{C}, \text{ unless otherwise noted})$

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
V,	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
		V ₁ < 0V	-20	
l _{iK}	Input protection diode current	$v_i > v_{cc}$	20	mA
	0.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1	V ₀ < 0V	-20	
lok	Output parasitic diode current	Vo > Vcc	. 20	mA.
lo	Output current per output pin		±25	mA
Icc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		-65~+150	င

Note 2 : M74HC237FP, $T_a=-40\sim+70^\circ$ C and $T_a=70\sim85^\circ$ C are derated at -6mW/°C. M74HC237DP, $T_a=-40\sim+50^\circ$ C and $T_a=50\sim85^\circ$ C are derated at -5mW/°C.

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85 \degree C)$

	Parameter			Limits		Unit
Symbol	Pai	Min	Тур	Max	Unit	
V _{CC}	Supply voltage		2		6	٧
Vi	Input voltage	. 0		Vcc	V	
Vo	Output voltage	0		Vcc	. V	
Topr	Operating temperature ra	inge	-40		+85	ာ
		V _{CC} = 2.0V	0	-	1000	
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns
	*	$V_{CC} = 6.0V$			400	

1-OF-8 DECODER/DEMULTIPLEXER WITH ADDRESS LATCH

ELECTRICAL CHARACTERISTICS

							Limits			
Symbol	Parameter	Test	conditions		25℃			-40~+85℃		Unit
				V _{cc} (V)	Min	Тур	Max	Min	Max	
		V = 0.1V V	$V_0 = 0.1V, V_{CC} = 0.1V$ $ I_0 = 20\mu A$		1.5			1.5		
V _{IH}	High-level input voltage	1 -			3.15			3.15		٧
		$ 10 = 20\mu\text{A}$		6.0	4. 2		İ	4.2		
	,	V =0.1V V	0.14	2.0			0.5		0.5	
VIL	Low-level input voltage	$V_0 = 0.1V$, V_{CO}		4.5			1. 35		1.35	V
		$ I_0 = 20\mu A$		6.0			1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
			$I_{OH} = -20\mu A$	4.5	4.4			4.4		
V _{OH}	High-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		V
			$I_{OH} = -4.0 \text{mA}$	4.5	4.18			4.13		
			$I_{OH} = -5.2 mA$	6.0	5. 68			5.63		
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
			$I_{OL} = 20 \mu A$	4.5			0.1		0.1	
VoL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1	ľ	0.1	v
			I _{OL} = 4. 0mA	4. 5			0. 26		0.33	
			I _{OL} = 5. 2mA	6.0			0. 26		0.33	
I _{IH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μΑ
l _{IL}	Low-level input current	V ₁ = 0V		6.0			-0.1		-1.0	μΑ
lcc	Quiescent supply current	Vi = VCC, GND	$I_0 = 0 \mu A$	6.0			4.0		40.0	μА

SWITCHING CHARACTERISTICS $(V_{cc} = 5V, T_a = 25^{\circ}C)$

					Unit	
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
truH	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time				10	ns
t _{PLH}	Low-level to high-level and high-level to low-level		,		41	ns
t _{PHL}	output propagation time (A — Y)				32	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = 15pF (Note 4)			35	ns
t _{PHL}	output propagation time (CS2 - Y)	CL = 15pr (Note 4)			25	ns
t _{PLH}	Low-level to high-level and high-level to low-level				35	ns
t _{PHL}	output propagation time (CS1 — Y)				27	ns
t _{PLH}	Low-level to high-level and high-level to low-level				44	ns
t _{PHL}	output propagation time (LE - Y)				33	ns

1-OF-8 DECODER/DEMULTIPLEXER WITH ADDRESS LATCH

SWITCHING CHARACTERISTICS $(v_{cc} = 2\sim6v, \tau_a = -40\sim+85^{\circ}C)$

Symbol	Parameter	Test conditions			25℃	Limits	-40~	+85℃	Unit
Symbol	Falanetei	rest conditions	V _{cc} (V)	Min	Тур	Max	Min	Max	0,,,,
	÷		2.0		1,714	75		95	
t _{TLH}	Low-level to high-level and		4.5			15		19	ns
·ILH			6.0			13		16	
	high-level to low-level		2.0			75		95	
t _{THL}	output transition time		4.5	-		15		19	ns
*180			6.0			13		16	
		†	2.0			235		296	
t _{PLH}	Low-level to high-level and		4.5			47		59	ns
·PLM	high-level to low-level		6.0			40		50	
	output propagation time		2.0			185		233	
t _{PHL}	(A - Y)		4.5			37		47	ns
			6.0			31		40	1
			2.0			200		252	
t _{PLH}	Low-level to high-level and		4.5			40		50	n
	high-level to low-level		6.0			34		43	
	output propagation time	$C_L = 50 pF \text{ (Note 4)}$	2.0			145		183	
t _{PHL}	(CS 2 – Y)		4.5			29		37	ns
			6.0			25		31	
-		1 :	2.0			200		252	
t _{PLH}	Low-level to high-level and		4.5			40		50	n
7	high-level to low-level	· ·	6.0			34		43	
	output propagation time		2.0			160		202	
t _{PHL}	(CS1 - Y)		4.5			32		40	ns
			6.0			27		34	
		1	2.0			250		315	
t _{PLH}	Low-level to high-level and		4.5			50		63	ns
	high-level to low-level		6.0			43		54	
	output propagation time		2.0			190		239	
t _{PHL}	(LE - Y)		4.5			38		· 48	ns
	(12 //	1	6.0			32		41	
Cı	Input capacitance					. 10		. 10	рГ
C _{PD}	Power dissipation capacitance (Note 3)				105				рF

Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.

The power dissipated during operation under no-load conditions is calculated using the following formula:

P_D = C_{PD} • V_{CC}² • f₁+I_{CC} • V_{CC}

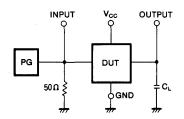
TIMING REQUIREMENTS ($v_{cc} = 2\sim 6v$, $T_a = -40\sim +85^{\circ}C$)

					Limits				
Symbol	Parameter	Test conditions			25℃		-40~+85°C		Unit
			V _{cc} (V)	Min	Тур	Max	Min .	Max	
			2.0	80			101		
tw	Latch enable pulse width		4.5	16			20		ns
			6.0	14			17		
	A A Al] ,	2.0	100			126		
tsu	A setup time with		4.5	20			25		ns
	respect to LE		6.0	17			21		
	A heald sine a suith		2.0	50			63		
th	A hold time with		4.5	10			13		ns
	respect to LE		6.0	9			11		

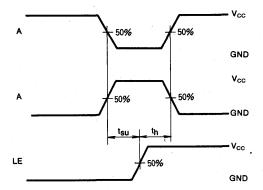


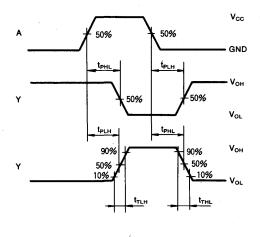
1-OF-8 DECODER/DEMULTIPLEXER WITH ADDRESS LATCH

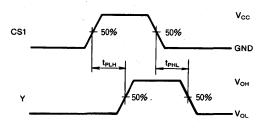
Note 4: Test Circuit

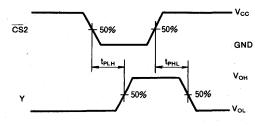


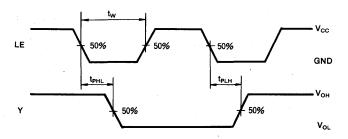
- (1) The pulse generator (PG) has the following characteristics (10% \sim 90%): $t_r = 6$ ns, $t_f = 6$ ns
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.













MITSUBISHI HIGH SPEED CMOS

M74HC238P/FP/DP

1-0F-8 DECODER/DEMULTIPLEXER

DESCRIPTION

The M74HC238 is a semiconductor integrated circuit consisting of a 3-bit binary-to-octal decoder/demultiplexer with chip select inputs.

FEATURES

- Three chip select inputs
- Expandable to 24 outputs without external components
- High-speed: 18ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC238 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS238.

When operated as a decoder, a 3-bit binary code are applied to inputs A0, A1 and A2, one of outputs Y0 through Y7 corresponding to this value will become high and the other outputs will all become low.

In this case, chip select input CS1 should be maintained at high while $\overline{\text{CS2}}$ and $\overline{\text{CS3}}$ should be maintained at low.

When CS1, $\overline{\text{CS2}}$ and $\overline{\text{CS3}}$ are in conditions other than those given above, all outputs will become low irrespective of A0 through A2.

When operated as a 1-of-8 demultiplexer, CS1, $\overline{\text{CS2}}$ or $\overline{\text{CS3}}$ is used as data input and A0 through A2 input are used as selecting input.

PIN CONFIGURATION (TOP VIEW) 16 V_{cc} INPUTS → Y0 A2 14 3 13 CS2 → 4 CS2 Y2 CHIP SELECT CS3 5 CS3 Y3 12 OUTPLITS CS1 11 CS1 → 6 10 OUTPUTS 7 GND 8 16P4 Outline 16P2N 16P2P

FUNCTION TABLE (Note 1)

		Inputs						Out	puts			
CS1	CSX	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6 "	Y7
Х	Н	X	Х	Х	L	L	L	L	L	L	L	L
L	х	Х	X	Х	L	L	L	L	L.	L	L	L
Н	L	L	L	L	. н	L	L	L	L	L	L	١
Н	L	L	L	Н	L	Н	L	L	L	L	L	L
. н	L	L.	Н	L	L	L	H	L	L	L	L	L
Н	L	L	Н	Н	L	L	L	Н	L	: L	L	L
H.	L	Н	L	L	L	L	L	L	н	L	L	L
H.	L	Н	L	Н	L	L	L	L	L	Н	'L	Ĺ
Н	L	Н	Н	L	L	L	L	L	L	L	Н	Ĺ
н	Ļ	Н	Н	н	Ļ	L	L	L	Ŀ	L	L	Н

Note 1: $\overline{CSX} = \overline{CS2} + \overline{CS3}$

X: Irrelevant



MITSUBISHI HIGH SPEED CMOS M74HC240P/FP/DWP

OCTAL 3-STATE INVERTING BUFFER/LINE DRIVER/LINE RECEIVER

DESCRIPTION

The M74HC240 is a semiconductor integrated circuit consisting of two blocks of 3-state non-inverting buffers each with four independent circuits that share a common enable input.

FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 10ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2∼6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC240 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS240.

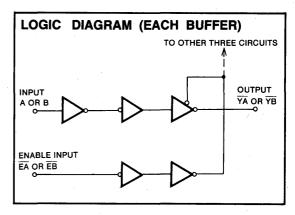
The M74HC240 consists of two independent blocks with each block containing four buffers.

When enable input \overline{E} is low and input A (or B) is low then output \overline{Y} will become high. However, if A (or B) is high then \overline{Y} will become low.

When \overline{E} is high then all outputs within the block will become high-impedance state, irrespective of A (or B).

All eight buffer circuits can be controlled simultaneously by connecting $\overline{\mathsf{EA}}$ and $\overline{\mathsf{EB}}$ of the two blocks.

PIN CONFIGURATION (TOP VIEW) ENABLE INPUT 7 19 ← EB ENABLE INPUT INPUT OUTPUT YB4 ← → YA1 OUTPUT INPUT A2 → 4 17 ← R4 INPLIT OUTPUT YB3 ← 5 16 → YA2 OUTPUT INPUT A3 → 6 15 ← B3 INPUT OUTPUT YB2 ← 7 14 → YA3 OUTPUT A4 → 8 INPUT 13 ← B2 INPUT OUTPUT YB1 ← 9 → YA4 OUTPUT GND ⊷ B1 INPUT 20P4 20P2N Outline 20P2V



FUNCTION TABLE (Note 1)

Inp	outs	Output		
A, B	YA, YB			
L	L	Н		
Н	L	L		
X	Н	Z		

Note 1 : Z : High impedance X : Irrelevant

ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85$ °C, unless otherwise noted)

Carrier Carrier Control Contro

Symbol	Parameter	Conditions	Ratings	Unit
V _{cc}	Supply voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	V "
Vo	Output voltage		-0.5~V _{cc} +0.5	V
		V ₁ < 0V	-20	
lik	Input protection diode current	V _I > V _{CC}	20	mA .
-		V ₀ < 0V	-20	
ок	Output parasitic diode current	V ₀ > V ₀₀	20	mA mA
lo	Output current per output pin		±35	mA
·lcc	Supply/GND current	V _{CC} , GND	±75	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		-65~+150	°

Note 2 : M74HC240FP, T T_a = $-40\sim+75^{\circ}$ C and T T_a = $75\sim85^{\circ}$ C are derated at -7mW/°C. M74HC240DWP, T T_a = $-40\sim+80^{\circ}$ C and T T_a = $80\sim85^{\circ}$ C are derated at -7mW/°C.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85 ^{\circ}C)$

0		Parameter			Limits				
Symbol	Par	ameter	Min	Тур	Max	Unit			
Vcc	Supply voltage		.2		6	٧			
V ₁	Input voltage	0		Vcc	V				
Vo	Output voltage	,	0		Vcc	V			
Topr	Operating temperature ra	inge	40		+85	င			
		V _{CC} = 2.0V	0		1000				
t _r , t _f	Input risetime, falltime	V _{CC} = 4.5V	0		500	ns			
		0		400					

ELECTRICAL CHARACTERISTICS

							Limits			
Symbol	Parameter	Test	conditions		25℃			-40~+85℃		Unit
	· ·			V _{cc} (V)	Min	Тур	Max	Min	Max	
		N - 0 1W		2.0	1.5			1.5		
V _{IH}	High-level input voltage	$V_0 = 0.1V$ $ I_0 = 20\mu A$		4.5	3.15			3. 15		V
		1101 = 20µA	$_{\rm O}$ = $_{\rm ZU}\mu$ A		4.2			4.2	2	
		V =0.1V V	_0 1v	2.0	,		0.5		0. 5	
VIL	Low-level input voltage	$ V_0 = 0.1V, V_{C} $ $ I_0 = 20\mu A$	$V_0 = 0.1 \text{V}, \ V_{CC} - 0.1 \text{V}$				1.35		1.35	V
		1 ₀ = 20μΑ		6.0		-	1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
			$I_{OH} = -20\mu A$	4.5	4.4		* .	4.4		
V _{OH}	High-level output voltage	$V_i = V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		V
	*	,	$I_{OH} = -6.0 \text{mA}$	4.5	4.18			4. 13		
	,		I _{OH} == -7.8mA	6.0	5. 68			5.63		
			$I_{OL} = 20 \mu A$	2, 0			0.1	٠.	0.1	
			$I_{OL} = 20 \mu A$	4.5			0.1	5.	0.1	
VoL	Low-level output voltage	$V_i = V_{iH}, \ V_{iL}$	$I_{OL} = 20 \mu A$	6.0	1		0.1		0.1	V
			$I_{OL} = 6.0 mA$	4.5			0.26		0.33]
			$I_{OL} = 7.8 \text{mA}$	6.0	1 -		0.26	- *	0.33	
I _{IH}	High-level input current	V _i = 6V		6.0			0.1		1.0	μA
I _{IL}	Low-level input current	V _i = 0V		6.0			-0.1		—1.0	μA
lozh	Off-state high-level output current	$V_i = V_{iH}, \ V_{iL},$	$v_o = v_{cc}$	6.0		1.	0.5		5. 0	μA
lozL	Off-state low-level output current	$V_i = V_{iH}, \ V_{iL},$	Vo = GND	6.0			-0.5		-5.0	μA
Icc	Quiescent supply current	Vi = VCC, GNE	$V_i = V_{CC}$, GND, $I_O = 0\mu A$				4.0		40.0	μA

SWITCHING CHARACTERISTICS ($v_{cc} = 2\sim6$ V, $T_a = -40\sim+85$ °C)

Symbol	Parameter	Test conditions		Limits			
Cymbol	Falallicie	Test conditions	Min	Тур	Max	Unit	
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns	
t _{THL}	output transition time	C _L = 50pF (Note 4)			10	ns	
t _{PLH}	Low-level to high-level and high-level to low-level				18	ns	
t _{PHL}	output propagation time $(A - \overline{YA}, B - \overline{YB})$				18	ns	
t _{PLZ}	Output disable time from low-level and high-level	C _L = 5 pF (Note 4)			25	ns	
t _{PHZ}	$(\overline{EA} - \overline{YA}, \overline{EB} - \overline{YB})$	CL = 5 pr (Note 4)			25	ns	
t _{PZL}	Output enable time to low-level and high-level	0 - 50-5 (N-4-4)			28	ns	
t _{PZH}	$(\overline{EA} - \overline{YA}, \overline{EB} - \overline{YB})$	$C_L = 50 pF \text{ (Note 4)}$			28	ns	

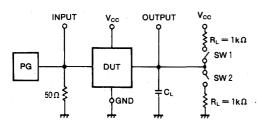
SWITCHING CHARACTERISTICS ($v_{cc} = 2\sim 6V$, $T_a = -40\sim +85^{\circ}C$)

						Limits			
Symbol	Parameter	Test conditions			25℃	,	−40 ~	+85℃	Unit
			V _{CC} (V)	Min	Тур	Max	Min	Max	
			2.0			60		75	
t _{TLH}	Low-level to high-level and		4. 5			12		15	ns
	high-level to low-level	C _L = 50pF (Note 4)	6, 0			10		13	
	Inglitional to low love!	or cobi (trate i)	2.0			60		75	
t _{THL}	output transition time		4.5			12		15	ns
			6.0			10		13	
			2.0			100		126	
t _{PLH}			4.5			20		25	ns
		C _L = 50pF (Note 4)	6.0			17		21	
		CL — SOPE (Note 4)	2.0			100		126	
t _{PHL}	Low-level to high-level and		4. 5			. 20		25	ns
	high-level to low-level		6.0			17		21	
	output propagation time		2.0			150		189	
t _{PLH}	$(A - \overline{YA}, B - \overline{YB})$		4.5			30		38	ns
		0 = 150=5 (N=1=4)	6.0			26		32	
		C _L = 150pF (Note 4)	2. 0			150		189	
t _{PHL}			4. 5			30		38	ns
			6.0			26		32	
			2.0			150		189	
t _{PLZ}	Output disable time from		4.5			30	1	38	ns
		50.5(), ()	6.0			26		32	
	low-level and high-level	C _L = 50pF (Note 4)	2.0			150		189	
t _{PHZ}	$(\overline{EA} - \overline{YA}, \overline{EB} - \overline{YB})$	·	4.5			30		38	ns
			6.0			26		32	
			2.0			150		189	
t _{PZL}			4.5			30		38	ns
			6.0			26		32	
		$C_L = 50pF (Note 4)$	2.0			150		189	
t _{PZH}	Output enable time to low-level		4.5			30		38	ns
		4	6.0			26		32	
	and high-level		2.0			200		252	
t _{PZL}	$(\overline{EA} - \overline{YA}, \overline{EB} - \overline{YB})$		4.5			40		50	ns
			6.0			34		43	
		C _L = 150pF (Note 4)	2.0			200		252	
t _{PZH}			4.5			40	1	50	ns
	z H	*	6.0			34		43	, ,
Cı	Input capacitance					10	†	10	pF
Co	Off-state output capacitance	EA = V _{CC} , EB = V _{CC}	1			15		15	pF
C _{PD}	Power dissipation capacitance (Note 3)	35.			57	† · · ·		 	pF

Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per buffer)
The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$

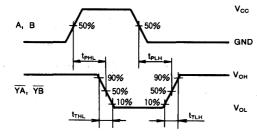


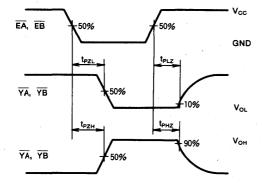
Note 4: Test Circuit



Parameter	SW 1	SW 2
t _{TLH} , t _{THL} t _{PLH} , t _{PHL}	Open	Open
t _{PLZ}	Closed	Open
t _{PHZ}	Open	Closed
t _{PZL}	Closed	Open
t _{PZH}	Open	Closed

- (1) The pulse generator (PG) has the following characteristics (10%~90%): t_f = 6ns, t_f = 6ns
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.





M74HC240-1P/FP/DWP

OCTAL 3-STATE INVERTING BUFFER/LINE DRIVER/LINE RECEIVER

DESCRIPTION

The M74HC240-1 is a semiconductor integrated circuit consisting of two blocks of 3-state inverting buffers each with four independent circuits that share a common enable input.

FEATURES

- High-fanout 3-state output: (I_{OL}=24mA, I_{OH}=-24mA)
- High-speed: 7ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 25µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5, 6V)
- Capable of driving 60 74LSTTL loads
- Wide operating voltage range: V_{CC}=2∼6V
- Wide operating temperature range: T_a=-40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC240-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS240.

The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

The M74HC240-1 consists of two independent blocks with each block containing four buffers.

When enable input \overline{E} is low and input A (or B) is low then output \overline{Y} will become high. However, if A (or B) is high then \overline{Y} will become low.

When \overline{E} is high then all outputs within the block will become high-impedance state, irrespective of A (or B).

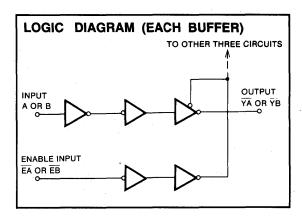
All eight buffer circuits can be controlled simultaneously by connecting $\overline{\sf EA}$ and $\overline{\sf EB}$ of the two blocks.

FUNCTION TABLE (Note 1)

. In	outs	Output
А, В	EA, EB	YA, YB
Ļ	L	н
Н	L	L
х	H	Z

Note 1 : Z : High impedance X : Irrelevant

PIN CONFIGURATION (TOP VIEW) ENABLE INPUT Vice 19 ← EB ENABLE INPUT INPUT OUTPUT YB4 18 → YA1 OUTPUT ← B4 INPUT INPLIT OUTPUT YB3 ← 5 16 → YA2 OUTPUT INPUT A3 → 6 15 ← B3 INPUT → YA3 OUTPUT OUTPUT YB2 ← INPUT A4 → 8 13 ← B2 INPUT 12 → YA4 OUTPUT OUTPUT YB1 ← 9 GND - B1 INPUT 20P4 Outline 20P2N 20P2V



ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85^{\circ}$ C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		−0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	. v
V _o	Output voltage		-0.5~V _{cc} +0.5	V
		V ₁ < 0V	-20	
lik .	Input protection diode current	V _I > V _{CC}	20	mA.
		V ₀ < 0V	-20	
юк	Output parasitic diode current	Vo > Vcc	20	mA
lo :	Output current per output pin		±50	mA
loc	Supply/GND current	V _{CC} , GND	±200	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		-65~+150	င

Note 2 : M74HC240-1FP, $T_a=-40\sim+75^\circ$ C and $T_a=75\sim85^\circ$ C are derated at -7mW/°C. M74HC240-1DWP, $T_a=-40\sim+80^\circ$ C and $T_a=80\sim85^\circ$ C are derated at -7mW/°C.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85 \degree C)$

				Limits	Limits		
Symbol	. Pa	rameter	Min	Тур	Max	Unit	
V _{cc}	Supply voltage		2		6	V	
Vı	Input voltage		0		V _{CC}	٧	
Vo	Output voltage		0		V _{CC}	V	
Topr	Operating temperature ra	ange _	-40		+85	℃ .	
		$V_{CC} = 2.0V$	0		500		
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		50	ns/V	
		$V_{CC} = 6.0V$	0.		30		

ELECTRICAL CHARACTERISTICS

	1						Limits				
Symbol	Parameter	Test	conditions			25℃		−40 ~	+85℃	Unit	
	*			V _{cc} (V)	Min	Тур	Max	Min	Max	· ·	
				2.0	1.5			1.5			
V _{IH}	High-level input voltage	$V_0 = 0.1V$		4.5	3.15			3.15		l v	
·	$ I_0 = 20\mu A$		6.0	4.2			4. 2		v		
-		$V_0 = 0.1V, V_{CC}$	0.11/	2.0		•	0.5		0.5		
VIL	Low-level input voltage	$ V_0 = 0.1V, V_{CO} $ $ I_0 = 20\mu A$	50. T V	4.5			1. 35	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1.35	V	
	1101 - 20µA		6.0			1.8		1.8			
V _{OH} High-level output voltage			$I_{OH} = -20\mu A$	2.0	1.9			1.9		5 V 8 V	
	Migh Javal autout vallage	$V_{l} = V_{lL}$	$I_{OH} = -20\mu A$	4.5	4.4			4. 4	1.1		
	High-level output voltage	VI — VIL	$I_{OH} = -20\mu A$	6.0	5.9			5.9		\ \	
			$I_{OH} = -24mA$	4.5	3. 98			3.84			
			$I_{OL} = 20 \mu A$	2. 0			0.1		0. 1		
Vol.	Low-level output voltage	V; = V;H, V;L	$I_{OL} = 20 \mu A$	4.5			0.1		0.1	١.,	
VOL	Low-level output voltage	VI - VIH, VIL	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	•	
		* *	I _{OL} = 24mA	4.5			0.39		0.5		
l _{IH}	High-level input current	$V_1 = 6V$		6.0			0.1		1.0	μA	
J _{IL}	Low-level input current	V ₁ = 0V		6.0			-0.1		-1.0	μΑ	
lozh	Off-state high-level output current	$V_{i} = V_{iH}, V_{iL}, V_{iL}$	$V_{\rm o} = V_{\rm cc}$	6.0			0.5		5.0	μΑ	
lozL	Off-state low-level output current	$V_{i} = V_{iH}, \ V_{iL},$	o = GND	6.0			-0.5		-5. 0	μА	
loc	Quiescent supply current	VI = VCC, GND	$I_0 = 0\mu A$	6.0			5.0		50.0	μΑ	

SWITCHING CHARACTERISTICS ($V_{cc} = 5V$, $T_a = 25$ °C)

Symbol	Parameter	Test conditions		Limits		Unit
Symbol	Parameter	l est conditions	Min	Тур	Max	Unit
t _{TLH}	TLH Low-level to high-level and high-level to low-level				10	
t _{THL}	output transition time	C _L = 50pF (Note 4)			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	CL — SUPP (Note 4)			14	
t _{PHL}	output propagation time $(A - \overline{YA}, B - \overline{YB})$				14	ns
t _{PLZ}	Output disable time from low-level and high-level	$C_L = 5 pF (Note 4)$			18	
t _{PHZ}	$(\overline{EA} - \overline{YA}, \overline{EB} - \overline{YB})$	C _L = 5 pr (Note 4)			18	ns
t _{PZL}	Output enable time to low-level and high-level	C ₁ = 50pF (Note 4)			21	
t _{PZH}	$(\overline{EA} - \overline{YA}, \overline{EB} - \overline{YB})$	OL — SUPP (NOTE 4)			21	ns

SWITCHING CHARACTERISTICS $(V_{cc} = 2\sim6V, T_a = -40\sim+85^{\circ}C)$

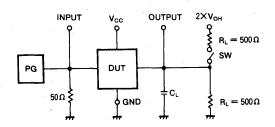
						Limits			
Symbol	Parameter	Test conditions			25℃		-40~	+85°C	ns
			V _{CC} (V)	Min	Тур	Max	Min	Max	
			2, 0			60		75	
t _{TLH}	Low-level to high-level and		4.5		-	12		15	
	high total to level total		6.0			10		13	
	high-level to low-level		2.0			60		75	l lis
t _{THL}	output transition time		4. 5			12		15	
			6.0			10	**	13	
			2.0			75		. 95	
t _{PLH}	Low-level to high-level and		4.5			15		19	
	high-level to low-level		6.0			. 13		16	
	output propagation time		2.0			75		95	ns
t _{PHL}	$(A-\overline{YA}, B-\overline{YB})$	•	4.5			15		19	
		0 = 50=5 (N=1=4)	6.0			13		16	
		$C_L = 50 pF (Note 4)$	2.0			115		145	
t _{PLZ}	Output disable time from		4.5		-	23		29	
	In the standard black to sel		6.0			20		25	
	low-level and high-level		2.0			115		145	ns
t _{PHZ}	$(\overline{EA} - \overline{YA}, \overline{EB} - \overline{YB})$		4.5		Ì	23		29	
•			6.0			20		25	
		,	2.0			115		145	
t _{PZL}	Output enable time to		4.5			23		29	
			6.0			20		25	
	low-level and high-level		2.0			115		145	ns
t _{PZH}	$(\overline{EA} - \overline{YA}, \overline{EB} - \overline{YB})$,	4.5			23		29	
			6.0			20		25	
Cı	Input capacitance					10		10	
Со	Off-state output capacitance	EA = V _{CC} , EB = V _{CC}				15		15	pF
C _{PD}	Power dissipation capacitance (Note 3)				43]

Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per buffer)

The power dissipated during operation under no-load conditions is calculated using the following formula:

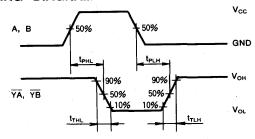
P_D = C_{PD} · V_{CC}² · f₁+I_{CC} · V_{CC}

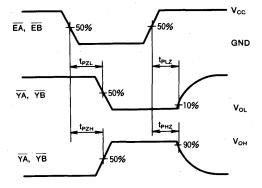
Note 4: Test Circuit



Parameter	sw
t _{TLH} , t _{THL}	Open
t _{PLZ}	Closed
t _{PHZ}	Open
t _{PZL}	Closed
t _{PZH}	Open

- (1) The pulse generator (PG) has the following
- characteristics (10%~90%): t_t = 3ns, t_t = 3ns (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.





M74HCT240P/FP/DWP

OCTAL 3-STATE INVERTING
BUFFER/LINE DRIVER/LINE RECEIVER WITH LSTTL-COMPATIBLE INPUTS

DESCRIPTION

The M74HCT240 is a semiconductor integrated circuit consisting of two blocks of 3-state inverting buffers each with four independent circuits that share a common enable input.

FEATURES

- TTL level input V_{IL} = 0.8V max V_{IH} = 2.0V min
- ◆ High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 12ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- Capable of driving 15 74LSTTL loads
- Wide operating temperature range: T_a=-40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HCT240 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS240.

As the inputs are TTL level, the device can be used as a level converter from LSTTL to high-speed CMOS. In that case, no pull-up resistors are required.

The M74HCT240 consists of two independent blocks with each block containing four buffers.

When enable input \overline{E} is low and input A (or B) is low then output \overline{Y} will become high. However, if A (or B) is high then \overline{Y} will become low.

When \overline{E} is high then all outputs within the block will become high-impedance state, irrespective of A (or B).

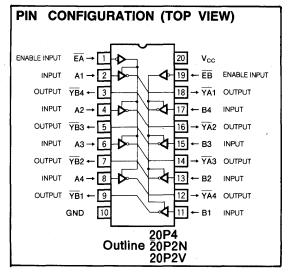
All eight buffer circuits can be controlled simultaneously by connecting $\overline{\text{EA}}$ and $\overline{\text{EB}}$ of the two blocks.

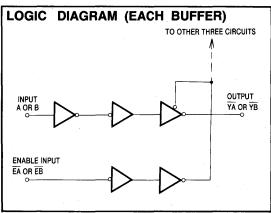
FUNCTION TABLE (Note 1)

Inj	Inputs			
A, B	A, B EA, EB			
L	L	н		
Н	L .	L		
×	х н			

Note 1 : Z : High impedance

X : Irrelevant





OCTAL 3-STATE INVERTING BUFFER/LINE DRIVER/LINE RECEIVER WITH LSTTL-COMPATIBLE INPUTS

ABSOLUTE MAXIMUM RATINGS $(T_a = -40 \sim +85\%$, unless otherwise noted)

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Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
3	Input protection diode current $ \frac{V_{i} < 0V}{V_{i} > V_{CC}} $	V ₁ < 0V	-20	
I _{IK}		20	mA	
	0.1.1	V ₀ < 0V	-20	
Іок	Output parasitic diode current	V _o > V _{cc}	20	mA
lo	Output current, per output pin	: .	±35	mA
Icc	Supply/GND current	V _{CC} , GND	±75	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		-65~+150	င

Note 2 : M74HC240FP, $T_a = -40 \sim +75 ^{\circ} C$ and $T_a = 75 \sim 85 ^{\circ} C$ are derated at -7 mW/C. M74HC240DWP, $T_a = -40 \sim +80 ^{\circ} C$ and $T_a = 80 \sim 85 ^{\circ} C$ are derated at -7 mW/C.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85^{\circ}C)$

Cumahal	Do	rameter		Limits	11-14	
Symbol	Pa	rameter	Min	Тур	Max	V V V C
Vcc	Supply voltage	Supply voltage			5.5	٧
V _i	Input voltage		0		Vcc	٧
Vo	Output voltage		0		Vcc	٧
Topr	Operating temperature ra	ange	-40		+85	Ç
		$V_{CC} = 2.0V$	0		1000	
t _r , t _f	Input risetime, falltime	V _{CC} = 4.5V	0		500	ns
		V _{CC} = 6.0V	.0		400	

ELECTRICAL CHARACTERISTICS ($v_{cc} = 5v \pm 10\%$, unless otherwise noted)

						Limits			
Symbol	Parameter		Test conditions		25℃		-40~	+85°C	Unit V V V μA
				Min	Тур	Max	Min	Max	
V _{IH}	High-level input voltage	$V_O = 0.1V$ $ I_O = 20\mu A$	-				2.0		v
ViL	Low-level input voltage	$V_{CC} = 0.1V, V_{C}$ $ I_{O} = 20\mu A$	_C -0.1V			0.8		0.8	٧
			$I_{OH} = -20\mu A$	V _{cc} -0.1			V _{cc} -0.1		
V _{OH} High-level output voltage	High-level output voltage	$V_i = V_{iL}$	$I_{OH} = -6.0 \text{mA}, V_{CC} = 4.5 \text{V}$	4.18			4. 13		V
			$I_{OH} = -7.2 \text{mA}, V_{CC} = 5.5 \text{V}$	5.18			5.13		
	·		$I_{OL} = 20 \mu A$			0.1		0.1	
VoL	Low-level output voltage	$V_i = V_{iH}, \ V_{iL}$	I _{OL} = 6.0mA, V _{CC} = 4.5V			0.26		0.33	V
			$I_{OL} = 7.2 \text{mA}, V_{CC} = 5.5 \text{V}$			0.26		0.33	
I _{IH}	High-level input current	V ₁ = 5.5V				0.1		1.0	
I _{IL}	High-level input current	$V_i = 0V$				-0.1		-1.0	μΑ
lozh	Off-state high-level output current	$V_i = V_{iH}, V_{iL}, V_{c}$	o = V _{CC}			0.5		5.0	_
I _{OZL}	Off-state low-level output current	$V_i = V_{iH}, V_{iL}, V_0$	= GND			-0.5		-5. 0	μΑ
Icc	Quiescent supply current	VI = VCC, GNE	$I_0 = 0\mu A$			4.0		40.0	μА
Δlcc	Maximum quiescent state supply current	$V_1 = 2.4V, 0.4$	V (Note 3)			2.7		2.9	mA

Note $\,3\,:\,$ Only one input is set at this value and all others are fixed at V_{CC} or GND.

M74HCT240P/FP/DWP

OCTAL 3-STATE INVERTING BUFFER/LINE DRIVER/LINE RECEIVER WITH LSTTL-COMPATIBLE INPUTS

SWITCHING CHARACTERISTICS (Vcc = 5V, Ta = 25°C)

		Task and distance		Limits		Unit ns
Symbol	Parameter	Test conditions	Min	Тур	Max	Onit
t _{TLH}	Low-level to high-level and high-level to low-level				12	
t _{THL}	output transition time	$C_1 = 50pF \text{ (Note 5)}$			12	115
t _{PLH}	Low-level to high-level and high-level to low-level	- C _L = 50pr (Note 5)			23	
t _{PHL}	output propagation time $(A - \overline{YA}, B - \overline{YB})$				23	115
t _{PLZ}	Output disable time from low-level and high-level	C _L = 5 pF (Note 5)			27	ns
t _{PHZ}	$(\overline{EA} - \overline{YA}, \overline{EB} - \overline{YB})$	CL = 5 pr (Note 5)			27	115
t _{PZL}	Output enable time to low-level and high-level	C ₁ = 50pF (Note 5)			32	ns
t _{PZH}	$(\overline{EA} - \overline{YA}, \overline{EB} - \overline{YB})$	OL — SUPP (NOTE 5)			32	115

SWITCHING CHARACTERISTICS ($v_{cc} = 5v \pm 10\%$, $\tau_a = -40 \sim +85$ °C)

					Limits			
Symbol	Parameter	Test conditions		25℃			-40~+85°C	
			Min	Тур	Max	Min	Max	
t _{TLH}	Low-level to high-level and high-level	0 = 50=5 (N=+= 5)			12		15	
t _{THL}	to low-level output transition time	C _L = 50pF (Note 5)			12		15.	ns
t _{PLH}	Low-level to high-level and	O F0 F (N-4 F)			23		29	
t _{PHL}	high-level to low-level	$C_L = 50 pF (Note 5)$			23		29	ns
t _{PLH}	output propagation time	C _L = 150pF (Note 5)			38		48	
t _{PHL}	$(A - \overline{Y}A, B - \overline{Y}\overline{B})$	CL — 150pr (Note 5)			38	48	, ns	
t _{PLZ}	Output disable time from	C = FOrF (Note F)			32		40	
t _{PHZ}	low-level and high-level (EA - YA, EB - YB)	$C_L = 50 pF (Note 5)$			32		40	ns
t _{PZL}	Output applie time to law lovel	$C_1 = 50 pF \text{ (Note 5)}$			32		40	
t _{PZH}	Output enable time to low-level and high-level	CL — 50pr (Note 5)			32		40	
t _{PZL}	(EA - YA, EB - YB)	C _L = 150pF (Note 5)			47		59	ns
t _{PZH}	(EA - TA, EB - TB)	CL — 150pr (Note 5)			47		59	
Cı	Input capacitance				10		10	
Co	Off-sate output capacitance	EA = EB = V _{CC}			15		15	рF
C _{PD}	Power dissipation capacitance (Note 4)			42				

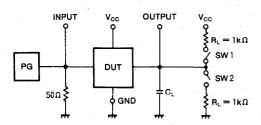
Note 4: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per buffer)

The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$



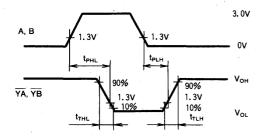
OCTAL 3-STATE INVERTING BUFFER/LINE DRIVER/LINE RECEIVER WITH LSTTL-COMPATIBLE INPUTS

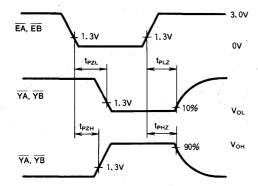
Note 5: Test Circuit



Parameter	SW 1	SW 2
t _{TLH} , t _{THL}	Open	Open
t _{PLZ}	Closed	Open
t _{PHZ}	Open	Closed
t _{PZL}	Closed	Open
t _{PZH}	Open	Closed

- (1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_r = 6ns (2) The capacitance C_L includes stray wiring
- capacitance and the probe input capacitance.







MITSUBISHI HIGH SPEED CMOS

M74HCT240-1P/FP/DWP

OCTAL 3-STATE INVERTING BUFFER/LINE DRIVER/ LINE RECEIVER WITH LSTTL-COMPATIBLE INPUTS

DESCRIPTION

The M74HCT240-1 is a semiconductor integrated circuit consisting of two blocks of 3-state inverting buffers each with four independent circuits that share a common enable input.

FEATURES

- TTL level input V_{IL} = 0.8V max V_{IH} = 2.0V min
- High-fanout 3-state output: (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed: 9ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 25µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- Capable of driving 60 74LSTTL loads
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HCT240-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS240.

The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

As the inputs are TTL level, the device can be used as a level converter from LSTTL to high-speed CMOS. In that case, no pull-up resistors are required.

The M74HCT240-1 consists of two independent blocks with each block containing four buffers.

When enable input \overline{E} is low and input A (or B) is low then output \overline{Y} will become high. However, if A (or B) is high then \overline{Y} will become low.

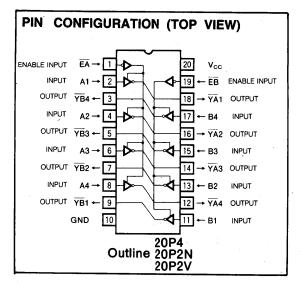
When \overline{E} is high then all outputs within the block will become high-impedance state, irrespective of A (or B).

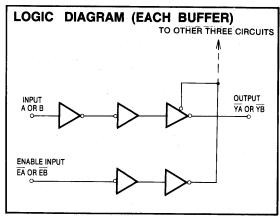
All eight buffer circuits can be controlled simultaneously by connecting $\overline{\mathsf{EA}}$ and $\overline{\mathsf{EB}}$ of the two blocks.

FUNCTION TABLE (Note 1)

Ing	outs	Output
A, B	YA, YB	
L	L	н
Н	L	L
х	Н	Z

Note 1 : Z : High impedance X : Irrelevant





M74HCT240-1P/FP/DWP

OCTAL 3-STATE INVERTING BUFFER/LINE DRIVER/ LINE RECEIVER WITH LSTTL-COMPATIBLE INPUTS

ABSOLUTE MAXIMUM RATINGS $(\tau_a = -40 \sim +85^{\circ}C)$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
V _I	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
		V ₁ < 0V	-20	·
lik	Input protection diode current	V _I > V _{CC}	20	- mA
	Output accepted disease accepted	V ₀ < 0V	-20	
юк	Output parasitic diode current	Vo > Vcc	20	mA
ilo.	Output current, per output pin		±50	mA.
Icc	Supply/GND current	V _{CC} , GND	±200	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65~+150	င

Note 2 : M74HC240-1FP, T $_a=-40\sim+75$ °C and T $_a=75\sim85$ °C are derated at -7mW/°C. M74HC240-1DWP, T $_a=-40\sim+80$ °C and T $_a=80\sim85$ °C are derated at -7mW/°C.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85 \%)$

	Parameter			Limits				
Symbol			Min	Тур	Max	Unit		
Vcc	Supply voltage		4.5		5.5	٧		
Vı	Input voltage		. 0		Vcc	V		
Vo	Output voltage	Output voltage			Vcc	V		
Topr	Ambient operating tempe	erature	40		+85	ဗင		
		V _{CC} = 4.5V	0		25	0		
t _r , t _f	Input risetime, falltime V _{CC} = 5.5V		0		15	ns/\		

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, unless otherwise noted)

			Test conditions		Limits					
Symbol	Parameter				25℃			+85℃	Unit	
	-			Min	Тур	Max	Min	Max		
V _{IH}	High level input veltage	$V_0 = 0.1V$		2.0			2. 0		· v	
VIH	High-level input voltage	I ₀ = 20μA		2.0		1	2.0		· •	
V I am land in the second	I am land in a decay	$V_0 = 0.1V, V_0$	c-0.1V			0.0		0.8	. >	
V _{IL}	Low-level input voltage		$I_0 = 20 \mu A$		0.8			0.8	V	
·	OH High-level output voltage	V - V	$I_{OH} = -20\mu A$	V _{cc} -0.1			V _{cc} -0.1		V	
v он		High-level output voltage $V_i = V_{iL}$	$I_{OH} = -24 \text{mÅ}, \ V_{CC} = 4.5 \text{V}$	3. 98			3.84			
·	1 1 1 1 1 1	W-W W	$I_{OL} = 20\mu A$			0.1		0.1	V	
V _{OL}	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 24 \text{mA}, \ V_{CC} = 4.5 \text{V}$			0.39		0.5		
I _{IH}	High-level input current	$V_i = V_{CC}$				0.1		1.0		
I _{IL}	Low-level input current	V _I = GND				-0.1		-1.0	μA	
l _{ozh}	Off-state high-level output current	$V_i = V_{iH}, \ V_{iL},$	$V_0 = V_{CC}$			0.5		5.0		
lozL	Off-state low-level output current	$V_i = V_{iH}, \ V_{iL},$	$V_{l} = V_{lH}, \ V_{lL}, \ V_{O} = GND$			-0.5		5.0	μF	
Icc	Quiescent supply current	$V_i = V_{CC}$, GNE	$V_i = V_{CC}$, GND, $I_0 = 0\mu A$			5. 0		50.0	μΑ	
△l _{cc}	Maximum quiescent supply current	$V_1 = 2.4V, 0.4$	V (Note 3)			2. 7		2, 9	m/	

Note 3: Only one input is set at this value and all other inputs are fixed at V_{CC} or GND.

MITSUBISHI HIGH SPEED CMOS

M74HCT240-1P/FP/DWP

OCTAL 3-STATE INVERTING BUFFER/LINE DRIVER/LINE RECEIVER WITH LSTTL-COMPATIBLE INPUTS

SWITCHING CHARACTERISTICS ($v_{cc} = 5v$, $T_a = 25^{\circ}C$)

Symbol	Parameter	Test conditions		Unit		
	i arameter	Test contributs	Min	Тур	Max	Unit
t _{TLH}	Low-level to high-level and high-level to low-level				10	
t _{THL}	output transition time	C = FOOF (Note F)			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	$C_L = 50 pF \text{ (Note 5)}$			14	
t _{PHL}	output propagation time $(A - \overline{YA}, B - \overline{YB})$				14	ns
t _{PLZ}	Output disable time from low-level and high-level	0 - 5 - 5 (1) - 5)			18	
t _{PHZ}	(EA — YA, EB — YB)	$C_L = 5 \text{ pF (Note 5)}$		-	18	ns
t _{PZL}	Output enable time to low-level and high-level	0 = 50=5 (N=4=5)	,		21	
t _{PZH}	(EA - YA, EB - YB)	$C_L = 50 pF \text{ (Note 5)}$			21	ns

SWITCHING CHARACTERISTICS $(v_{cc} = 5v \pm 10\%, T_a = -40 \sim +85^{\circ}C)$

				Limits					
Symbol	Parameter	Test conditions		25℃			+85℃	Unit	
			Min	Тур	Max	Min	Max		
t _{TLH}	Low-level to high-level and				12		15		
t _{THL}	high-level to low-level output transition time				12		15	ns	
t _{PLH}	Low-level to high-level and	, , , , , , , , , , , , , , , , , , ,			15		19		
t _{PHL}	output propagation time (A - YA, B - YB)			-	15		19	ns	
THE		C _L = 50pF (Note 5)		_					
t _{PLZ}	Output disable time from	OE SOPI (Note S)		14	23		29		
t _{PHZ}	low-level and high-level				23		29	ns	
t _{PZL}	Output enable time to				23		29		
t _{PZH}	low-level and high-level (EA - YA, EB - YB)				23		29	ns	
Cı	Input capacitance				10		10		
Co	Off-state output capacitance	= V _{CC} , EB = V _{CC}			15		15	pF	
C _{PD}	Power dissipation capacitance (Note 4)								

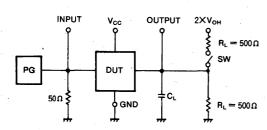
Note 4: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per buffer)
The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$



M74HCT240-1P/FP/DWP

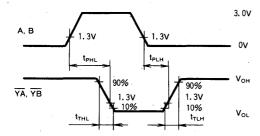
OCTAL 3-STATE INVERTING BUFFER/LINE DRIVER/ LINE RECEIVER WITH LSTTL-COMPATIBLE INPUTS

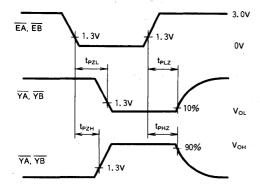
Note 5: Test Circuit



Parameter	sw
t _{TLH} , t _{THL}	Open
t _{PLZ}	Closed
t _{PHZ}	Open
t _{PZL}	Closed
t _{PZH}	Open

- (1) The pulse generator (PG) has the following
- characteristics (10%~90%): t_r = 3ns, t_f = 3ns (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.





M74HC241P/FP/DWP

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER

DESCRIPTION

The M74HC241 is a semiconductor integrated circuit consisting of two blocks of 3-state non-inverting buffers each with four independent circuits that share a common enable input.

FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 10ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2∼6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

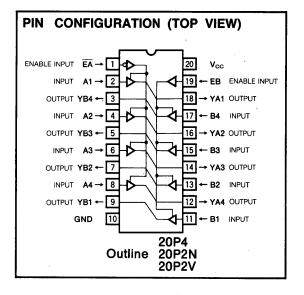
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC241 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS241.

The M74HC241 consists of two independent blocks with each block containing four buffers.

When enable input EA is low and input A is low then output YA will become low. However, if A is high then YA will become high. Inverted in the other block, a high enable input EB signal causes operation the same as that just described with input B signal output at YB.

When EA is high or EB is low then all Y within the block will become high-impedance state, irrespective of A or B.

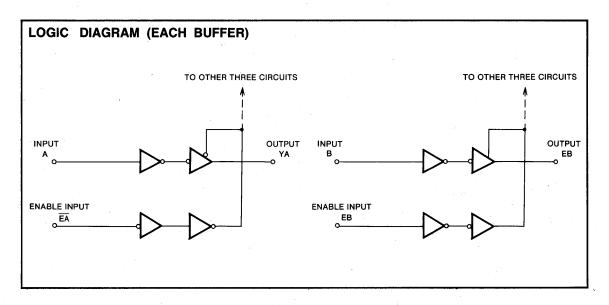


FUNCTION TABLE (Note 1)

Inp	uts	Output
Α	EA	YA
L	L	L
Н	L	Н
Х	н	Z

Note 1 : Z : High impedance

Inp	uts	Output		
В	В ЕВ			
L	н	L		
H	н	н		
х	L	Z		



ABSOLUTE MAXIMUM RATINGS $(\tau_a = -40 \sim +85 \degree)$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
	Input protection diode current	V ₁ < 0V	-20	
I _{IK} Input protection diode current	input protection glode current	V _I > V _{CC}	20	mA.
		V ₀ < 0V	-20	
lok	Output parasitic diode current	$V_0 > V_{CC}$	20	mA mA
lo	Output current per output pin		±35	mA
lcc .	Supply/GND current	V _{CC} , GND	±75	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65~+150	ా

Note 2 : M74HC241FP, $T_a=-40\sim+75^\circ$ C and $T_a=75\sim85^\circ$ C are derated at -7mW/°C. M74HC241DWP, $T_a=-40\sim+80^\circ$ C and $T_a=80\sim85^\circ$ C are derated at -7mW/°C.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85^{\circ}C)$

Complete	Parameter		,	Limits				
Symbol			Min	Тур	Max	Unit		
Vcc	Supply voltage		2		6	٧		
Vi	Input voltage		0		Vcc	V		
Vo	Output voltage		0		Vcc	٧		
Topr	Operating temperature ra	ange	—40		+85	°		
		V _{CC} = 2.0V	0		1000			
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns		
		0		400				

ELECTRICAL CHARACTERISTICS

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							Limits			
Symbol	Parameter	Test	Test conditions		25℃			-40~+85°C		Unit
•				V _{CC} (V)	Min	Тур	Max	Min	Max	
			0.11/	2.0	1.5			1.5		
VIH	High-level input voltage	$V_0 = 0.1V, V_{CC}$;0 . 1 V	4.5	3.15			3.15		٧
	$ \mathbf{I}_{O} = 20\muA$		6.0	4.2			4. 2			
		Vo = 0.1V, Vcc-0.1V		2.0			0.5		0.5	,
VIL	Low-level input voltage	, ,	, , ,	4.5			1.35		1.35	V
	$ 1_0 = 20\mu A$		6.0			1.8		1.8	ľ	
V _{OH} High-level output voltage			$I_{OH} = -20\mu A$	2.0	1.9			1.9		l
	·		$I_{OH} = -20\mu A$	4.5	4. 4			4. 4		l
	High-level output voltage	$V_i = V_{iH}, \ V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9		_	5. 9		١
			$i_{DH} = -6.0 \text{mA}$	4.5	4. 18			4.13		ŀ
			$I_{OH} = -7.8 \text{mA}$	6.0	5.68			5.63		
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	l
			$I_{OL} = 20 \mu A$	4.5			0.1		0.1	1
VoL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	١
		4.	$t_{OL} = 6.0 \text{mA}$	4.5			0.26	l	0.33	
			$I_{OL} = 7.8 \text{mA}$	6.0			0.26		0.33	
I _{IH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μ
l _{IL}	Low-level input current	$V_i = 0V$	$V_1 = 0V$				-0.1		-1.0	μ
I _{OZH}	Off-state high-level output current	$V_i = V_{iH}, \ V_{iL},$	$V_{O} = V_{CC}$	6.0			0.5		5.0	μ
lozL	Off-state low-level output current	$V_i = V_{iH}, \ V_{1L},$	Vo = GND	6.0	L		-0. 5		-5.0	μ
loc	Quiescent supply current	VI = VCC, GNE	$I_0 = 0\mu A$	6.0			4.0		40.0	μ

SWITCHING CHARACTERISTICS ($v_{cc} = 5v$, $\tau_a = 25^{\circ}C$)

Cumahani	Parameter	Test conditions	l	Limits			
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit	
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns	
t _{THL}	output transition time	$C_1 = 50pF (Note 4)$			10	ns	
t _{PLH}	Low-level to high-level and high-level to low-level	CL = Sopr (Note 4)			20	ns	
t _{PHL}	output propagation time (A - YA, B - YB)				20	ns	
t _{PLZ}	Output disable time from low-level and high-level	$C_i = 5 pF (Note 4)$			25	ns	
t _{PHZ}	(EA - YA, EB - YB)	CL = 5 pr (Note 4)			25	ns	
t _{PZL}	Output enable time to low-level and high-level	C ₁ = 50pF (Note 4)			28	ns	
t _{PZH}	(EA - YA, EB - YB)	CL - SOPF (Note 4)			28	ns	

SWITCHING CHARACTERISTICS ($v_{cc} = 2\sim 6v$, $T_a = -40\sim +85^{\circ}C$)

						Limits			
Symbol	Parameter Test condition			25℃		-40~+85°C		Uni	
			V _{CC} (V)	Min	Тур	Max	Min	Max	
			2.0			60		75	
t _{TLH}	Low-level to high-level and		4.5			12		15	ns
	high-level to low-level	C _L = 50pF (Note 4)	6.0	-		10		13	
	mgn-level to low-level	OL — Sopi (Note 4)	2.0			60		75	
t _{THL}	output transition time		4.5			12	i	15	ns
			6.0			10		13	
		_	2. 0			115		145	
t _{PLH}		1	4.5			23		29	ns
		C _L = 50pF (Note 4)	6.0			20	į	25	
		C _L = 50pr (Note 4)	2.0			115		145	
t _{PHL}	Low-level to high-level and		4.5			23		29	ns
	high-level to low-level		6.0			20		25	
	output propagation time		2.0			165		208	
t _{PLH}	(A - YA, B - YB)		4.5			33		42	ns
		150 5 (1)	6.0			28		35	
		C _L = 150pF (Note 4)	2.0			165		208	
t _{PHL}			4.5			33		42	ns
			6.0			28		35	
		`	2.0			150		189	
t _{PLZ}	Output disable time from	1	4.5			30		38	ns
			6.0			26		32	
	low-level and high-level	$C_L = 50pF (Note 4)$	2. 0			150		189	
t _{PHZ}	(EA - YA, EB - YB)		4.5			30	\ \	38	ns
			6.0			26		32	ł
			2. 0			150		189	
t _{PZL}	, '		4.5		1	30		38	ns
	1	1	6.0			26		32	
		$C_L = 50pF (Note 4)$	2. 0			150		189	
t _{PZH}	Output enable time to low-level	·	4.5			30		38	ns
			6.0			26	İ	32	
	and high-level		2.0			200		252	
t _{PZL}	(EA - YA, EB - YB)	1	4.5			40		50	ns
	1		6.0			34		43	
	1	C _L = 150pF (Note 4)	2. 0			200		252	
t _{PZH}			4.5			40		50	ns
-F4H	,		6.0			34		43	,,,5
Cı	Input capacitance		+ 5.5	-	-	10		10	pF
Co	Off-state output capacitance	EA = V _{CC} , EB = GND				15		15	pF
C _{PD}	Power dissipation capacitance (Note 3)	- VCC, LD - GND			59	13		13	pF

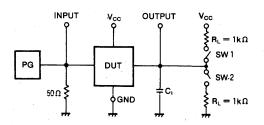
Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per buffer)

The power dissipated during operation under no-load conditions is calculated using the following formula:

P_D = C_{PD} · V_{CC}² · f_I+I_{CC} · V_{CC}

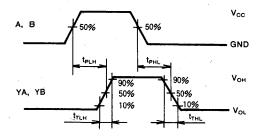


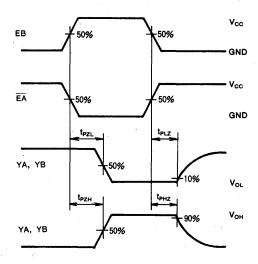
Note 4: Test Circuit



Parameter	SW1	SW 2
t _{TLH} , t _{THL} t _{PLH} , t _{PHL}	Open	Open
t _{PLZ}	Closed	Open
t _{PHZ}	Open	Closed
t _{PZL}	Closed	Open
t _{PZH}	Open	Closed

- (1) The pulse generator (PG) has the following
- characteristics (10%~90%): t_F = 6ns, t_F = 6ns (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.





M74HC241-1P/FP/DWP

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER

DESCRIPTION

The M74HC241-1 is a semiconductor integrated circuit consisting of two blocks of 3-state non-inverting buffers each with four independent circuits that share a common enable input.

FEATURES

- ◆ High-fanout 3-state output: (I_{OL}=24mA, I_{OH}=-24mA)
- High-speed: 8ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 25μW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5, 6V)
- Capable of driving 60 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=-40~+85℃

APPLICATION

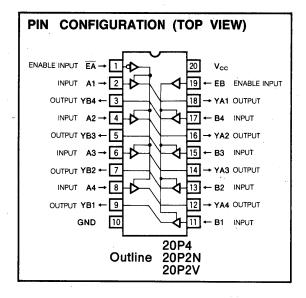
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC241-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS241.

The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

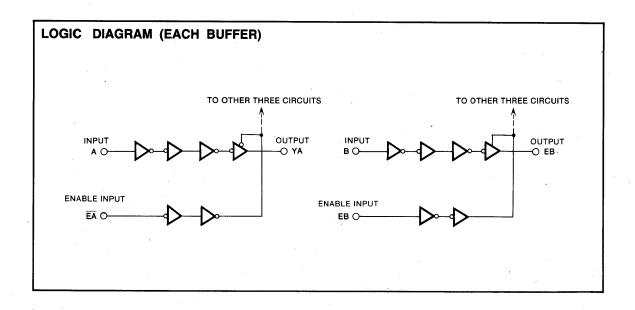
The M74HC241-1 consists of two independent blocks with



each block containing four buffers.

When enable input \overline{EA} is low and input A is low then output YA will become low. However, if A is high then YA will become high. Inverted in the other block, a high enable input EB signal causes operation the same as that just described with input B signal output at YB.

When $\overline{\text{EA}}$ is high or EB is low then all Y within the block will become high-impedance state, irrespective of A or B.



FUNCTION TABLE (Note 1)

Inp	Inputs				
Α	EA	YA			
L	L	L			
Н	L	Н			
X	Н	Z			

Inp	Inputs		
В	EB	YB	
L	н	L	
н.	Н	н	
X	L	Z	

Note 1: Z: High impedance

X : Irrelevant

ABSOLUTE MAXIMUM RATINGS $(T_a = -40 \sim +85\%$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		−0.5~+7.0	V
Vi	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
		V ₁ < 0V	-20	
l _{iK}	Input protection diode current	V _I > V _{CC}	20	mA
	Q 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4	V ₀ < 0V	-20	4
ок	Output parasitic diode current	$V_{o} > V_{cc}$	20	mA mA
lo	Output current per output pin		±50	mA
lcc	Supply/GND current	V _{CC} , GND	±200	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65~+150	င

Note 2 : M74HC241-1FP, T $_a$ = $-40\sim+75$ °C and T $_a$ = $75\sim85$ °C are derated at -7mW/°C. M74HC241-1DWP, T $_a$ = $-40\sim+80$ °C and T $_a$ = $80\sim85$ °C are derated at -7mW/°C.

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85 \degree c)$

Symbol	Parameter			Unit		
Symbol	Parameter			Тур	Max	Unit
Vcc	Supply voltage				6	V
V _i	Input voltage	Input voltage			Vcc	V
Vo	Output voltage		0		Vcc	V
Topr	Ambient operating temper	erature	-40		+85	င
		$V_{CC} = 2.0V$	0		500	
t _r , t _f	Input risetime, falltime	V _{CC} = 4.5V	0		50	ns/V
	$V_{CC} = 6.0V$		0		30]

ELECTRICAL CHARACTERISTICS

							Limits			i
Symbol	Parameter	Test conditions		25℃			-40~+85℃		Unit	
		. •		V _{cc} (V)	Min	Тур	Max	Min	Max	1
		$V_0 = 0.1V, V_{cc}$	-0.11/	2.0	1.5			1.5		
V_{IH}	High-level input voltage	$ I_0 = 20\mu A$	50. TV	4. 5	3.15			3.15		V
		1101 20μΑ		6.0	4.2			4.2		ĺ
		$V_{0} = 0.1V, V_{00}$	_0 1V	2.0			0.5		0.5	
V_{IL}	Low-level input voltage	$ I_0 = 20\mu A$	5—0.1 V	4.5			1.35		1.35	V
		$ 1_0 = 20\mu A$		6.0			1.8		1.8	ĺ
	V_{OH} High-level output voltnge $V_i = V$		$I_{OH} = -20\mu A$	2.0	1.9			1.9		
V.		$V_{i} = V_{iH}, V_{iL}$	$I_{OH} = -20\mu A$	4.5	4.4			4.4		v
• он			$I_{OH} = -20\mu A$	6.0	5.9			5.9		
			$I_{OH} = -24mA$	4.5	3. 98		**	3.84		i
			$I_{OL} = 20 \mu A$	2.0			0. 1		0. 1	
VoL	Low-level output voltage	VI = VIH, VIL	$I_{OL} = 20 \mu A$	4.5			0.1		0.1	v
VOL.	Low-level output voidige	VI — VIH, VIL	$I_{OL} = 20 \mu A$	6.0			0.1	İ	0.1	
			$I_{OL} = 24mA$	4.5			0.39		0.5	İ
I _{IH}	High-level input current	V ₁ = 6V	5	6.0	,		0. 1		1.0	μА
I _{IL}	Low-level input cuuent	V ₁ = 0V		6.0			-0.1		-1.0	μА
lozh	Off-state high-level output cuuent	$V_i = V_{iH}, \ V_{iL}, \ V_{iL}$	$V_0 = V_{CC}$	6.0			0.5		5.0	μΑ
lozL	Off-state low-level output current	$V_i = V_{iH}, \ V_{iL}, \ V_{iL}$	$V_{I} = V_{IH}, V_{IL}, V_{O} = GND $ 6. 0				-0.5		-5. 0	μA
Icc	Quiescent supply current	VI = VCC, GND	$I_{O} = 0\mu A$	6.0			5. 0		50.0	μΑ

SWITCHING CHARACTERISTICS ($v_{cc} = 5v$, $\tau_a = 25$ °C)

Symbol	Parameter	Parameter Test conditions		Unit		
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
t _{TLH}	Low-level to high-level and high-level to low-level				10	
t _{THL}	output transition time	$C_1 = 50 pF (Note 4)$			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	CL = 50pr (Note 4)			16	
t _{PHL}	output propagation time (A — YA, B — YB)				16	ns
t _{PLZ}	Output disable time from low-level and high-level	0 - 5-5(N-1-4)		18		
t _{PHZ}	(EA - YA, EB - YB)	C _L = 5 pF (Note 4)			18	ns
t _{PZL}	Output enable time to low-level and high-level	C = 5005 (Note 4)			21	
t _{PZH}	(EA - YA, EB - YB)	$C_L = 50pF (Note 4)$			21	ns

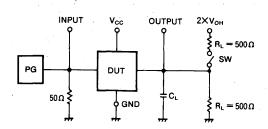
SWITCHING CHARACTERISTICS ($v_{cc} = 2\sim 6V$, $T_a = -40\sim +85^{\circ}C$)

						Limits			
Symbol	Parameter	Test conditions			25℃		−40 ~	+85℃	Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0			60		75	
t _{TLH}	Low-level to high-level and	•	4.5			12		15	ĺ
	high-level to low-level		6.0			10		13	ns
	mign-lever to low-lever		2.0			60		75	115
t _{THL}	output transition time		4.5			12		15	
			6.0			10		13	
			2.0			90		115	
t _{PLH}	Low-level to high-level and		4.5			18		23	
	high-level to low-level		6.0			15	<u> </u>	20	ns
	output propagation time		2.0			90		115	115
t _{PHL}	(A - YA, B - YB)		4.5			18		23	
		C _L = 50pF (Note 4)	6.0			15		25	
		CL — Sopr (Note 4)	2.0			115		145	
t _{PLZ}	Output disable time from		4.5			23	Ì	29	
	low-level and high-level		6.0			20		25	ns
			2.0			115		145	115
t _{PHZ}	(EA - YA, EB - YB)		4.5			23		29	
			6.0			20	-	25	
			2.0			115		145	
t_{PZL}	Output enable time to		4.5			23]	29	ļ
	low-level and high-level	·	6.0			20		25	ns
			2.0			115		145	115
t _{PZH}	(EA - YA, EB - YB)		4.5			23		. 29	
			6.0			20		25	
Cı	Input capacitance					10		10	
Co	Off-state output capacitance	$\overline{EA} = V_{CC}, EB = GND$				15		15	pF
CPD	Power dissipation capacitance (Note 3)				43				

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per buffer)
The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$



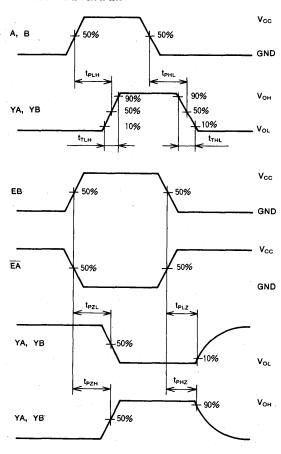
Note 4: Test Circuit



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Parameter	SW
t _{TLH} , t _{THL}	Open
t _{PLZ}	Closed
t _{PHZ}	Open
t _{PZL}	Closed
t _{PZH}	Open

- (1) The pulse generator (PG) has the following characteristics (10%~90%): $t_f=3 n s, \ t_f=3 n s$
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.



M74HCT241P/FP/DWP

OCTAL 3-STATE NONINVERTING
BUFFER/LINE DRIVER/LINE RECEIVER WITH LSTTL-COMPATIBLE INPUTS

DESCRIPTION

The M74HCT241 is a semiconductor integrated circuit consisting of two blocks of 3-state noninverting buffers each with four independent circuits that share a common enable input.

FEATURES

- TTL level input V_{IL}=0.8V max V_{IH}=2.0V min
- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 13ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- Capable of driving 15 74LSTTL loads
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

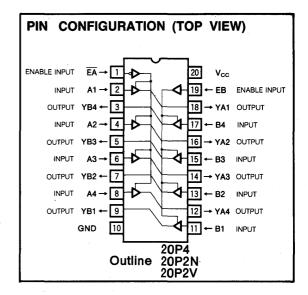
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HCT241 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS241.

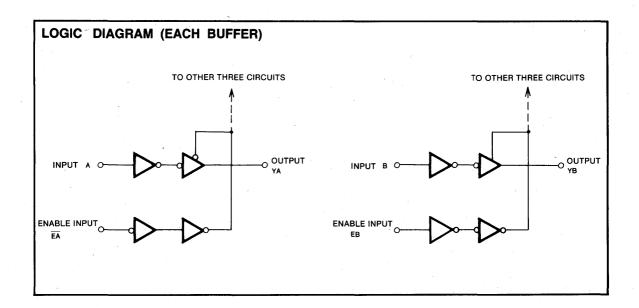
As the inputs are TTL level, the device can be used as a level converter from LSTTL to high-speed CMOS. In that case, no pull-up resistors are required.

The M74HCT241 consists of two independent blocks with each block containing four buffers.



When enable input \overline{EA} is low and input A is low then output YA will become low. However, if A is high then YA will become high. Inverted in the other block, a high enable input EB signal causes operation the same as that just described with input B signal output at YB.

When \overline{EA} is high or EB is low then all Y within the block will become high-impedance state, irrespective of A or B.



FUNCTION TABLE (Note 1)

Inpi	uts	Output
Α	ĒĀ	YA
Ļ	L	L
н	L	н
V	Ц	7

Note 1 : Z : High impedance

X : Irrelevant

ABSOLUTE MAXIMUM RATINGS ($\tau_a = -40 \sim +85$ °C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
I land with still diede augest	V ₁ < 0V	-20		
lik	Input protection diode current	V _I > V _{CC}	20	mA
		V ₀ < 0V	-20	
Іок	Output parasitic diode current	Vo > Vcc	20	mA
lo	Output current per output pin		±35	mA
Icc	Supply/GND current	V _{CC} , GND	土75	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65~ +150	င

Note 2 : M74HCT241FP, T_a = $-40\sim+75^\circ$ C and T_a = $75\sim85^\circ$ C are derated at -7mW/°C. M74HCT241DWP, T_a = $-40\sim+80^\circ$ C and T_a = $80\sim85^\circ$ C are derated at -7mW/°C.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85 ^{\circ}C)$

0	Parameter		Limits				
Symbol		Min	Тур	Max	Unit		
Vcc	Supply voltage	4.5		5.5	V		
Vı	Input voltage	0		Vcc	V		
Vo	Output voltage	0		Vcc	V		
Topr	Operating temperature range	-40		+85	ဇ		
t _r , t _f	Input risetime, falltime	0		500	ns		

ELECTRICAL CHARACTERISTICS ($V_{cc} = 5V \pm 10\%$, unless otherwise noted)

			Limits						
Symbol	Parameter		Test conditions		25℃			+85℃	Unit
				Min	Тур	Max	Min	Max	
V _{IH}	High-level input voltage	$V_0 = 0.1V$, $V_{CC} - 0.1V$ $ I_0 = 20\mu A$		2. 0			2.0		V
VIL	Low-level input voltage	$V_0 = 0.1V$, $V_{CC} = 0.1V$ $ I_0 = 20\mu A$				0.8		0.8	V
			$I_{OH} = -20\mu A$	V _{cc} -0.1			V _{cc} -0.1		
V _{OH}	High-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OH} = -6.0 \text{mA}, V_{CC} = 4.5 \text{V}$	4.18			4.13		V
			$I_{OH} = -7.2 \text{mA}, V_{CC} = 5.5 \text{V}$	5.18			5.13		41
			$I_{OL} = 20\mu A$		· ·	0.1		0.1	
VoL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 6.0 \text{mA}, V_{CC} = 4.5 \text{V}$			0.26		0.33	V
		* .	$I_{OL} = 7.2 \text{mA}, \ V_{CC} = 5.5 \text{V}$			0.26		0.33	
I _{IH}	High-level input current	$V_i = V_{CC}$,		0.1		1.0	μΑ
IIL	Low-level input current	V _I = GND				-0.1		-1.0	μΑ
lozh	Off-state high-level output current	$V_i = V_{iH}, \ V_{iL}, \ V$	$v_0 = V_{CC}$			0.5		5.0	μA
I _{OZL}	Off-state low-level output current	$V_{i} = V_{iH}, \ V_{iL}, \ V$	$V_i = V_{iH}, \ V_{iL}, \ V_O = GND$			-0.5		-5.0	μA
loc	Quiescent supply current	$V_{I} = V_{CC}$, GND.	$I_0 = 0\mu A$			4.0	1	40.0	μΑ
△lcc	Maximum quiescent supply current	$V_1 = 2.4V, 0.4V$	(Note 3), $I_0 = 0 \mu A$			2.7		2. 9	mA

Note 3: Only one input is set at this value and all other inputs are fixed at V_{CC} or GND.



MITSUBISHI HIGH SPEED CMOS M74HCT241P/FP/DWP

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER WITH LSTTL-COMPATIBLE INPUTS

SWITCHING CHARACTERISTICS $(v_{cc} = 5v, T_a = 25^{\circ}C)$

Symbol	Parameter	Tank and diking		Unit		
Symbol		Test conditions	Min	Тур	Max	Unit
t _{TLH}	Low-level to high-level and high-level to low-level				12	ns
t _{THL}	output transition time	C = 50=5 (Note 5)			12	ns
t _{PLH}	Low-level to high-level and high-level to low-level	$C_L = 50 pF \text{ (Note 5)}$			25	ns
t _{PHL}	output propagation time (A — YA, B — YB)				25	ns
t _{PLZ}	Output disable time from low-level and high-level	C _L = 5 pF (Note 5)			27	ns
t _{PHZ}	(EA - YA, EB - YB)	CL = 5 pr (Note 5)			27	ns
t _{PZL}	Output enable time to low-level and high-level	C _L = 50pF (Note 5)			32	ns
t _{PZH}	(EA - YA, EB - YB)	GL — Supr (Note 5)			32	ns

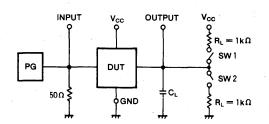
SWITCHING CHARACTERISTICS $(V_{cc} = 2\sim6V, T_a = -40\sim+85^{\circ}C)$

				Limits					
Symbol	Parameter	Test conditions		25℃			-40~+85℃		
			Min	Тур	Max	Min	Max		
t _{TLH}	Low-level to high-level and high-level to low-level	$C_1 = 50pF (Note 5)$			12		15	ns	
t _{THL}	output transition time	CL = 50pr (Note 5)			12		15	ns.	
t _{PLH}	Low-level to high-level and	C = 50=5 (Note 5)			25		32	ns	
t _{PHL}	high-level to low-level	$C_L = 50pF (Note 5)$			25		32	ns	
t _{PLH}	output propagation time	C = 150-5 (Note 5)			40		51	ns	
t _{PHL}	(A - YA, B - YB)	C _L = 150pF (Note 5)			40		51	ns	
t _{PLZ}	Output disable time from	C = 50=5 (Note 5)			32		40	ns	
t _{PHZ}	low-level and high-level (EA — YA, EB — YB)	$C_L = 50 pF \text{ (Note 5)}$			32		40	ns	
t _{PZL}	Custous anable since so love lovel	C _L = 50pF (Note 5)			32		40	ns	
t _{PZH}	Output enable time to low-level	CL = 50pr (Note 5)			32		40	ns	
t _{PZL}	and high-level (EA — YA, EB → YB)	C _L = 150pF (Note 5)			47		59	ns	
t _{PZH}	(EA — TA, EB — TB)	C _L = 150pF (Note 5)	,		47		59	ns	
Cı	Input capacitance				10		10	рF	
Со	Off-state output capacitance	EA = V _{CC} , EB = GND			15		15	рF	
C _{PD} .	Power dissipation capacitance (Note 4)			44				рF	

Note 4: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per buffer)
The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$

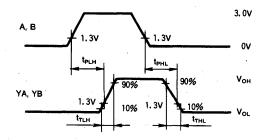


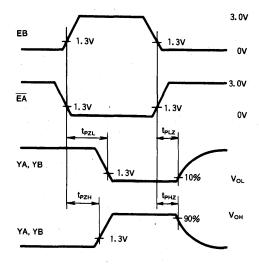
Note 5: Test Circuit



Parameter	SW 1	SW 2
t _{TLH} , t _{THL} t _{PLH} , t _{PHL}	Open	Open
t _{PLZ}	Closed	Open
t _{PHZ}	Open	Closed
tezL	Closed	Open
t _{PZH}	Open	Closed

- (1) The pulse generator (PG) has the following characteristics (10% \sim 90%): t_r = 6ns, t_f = 6ns
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.







MITSUBISHI HIGH SPEED CMOS

M74HCT241-1P/FP/DWP

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER WITH LSTTL-COMPATIBLE INPUTS

DESCRIPTION

The M74HCT241-1 is a semiconductor integrated circuit consisting of two blocks of 3-state noninverting buffers each with four independent circuits that share a common enable input.

FEATURES

- TTL level input V_{IL}=0.8V max V_{IH}=2.0V min
- High-fanout 3-state output: (I_{OL}=24mA, I_{OH}=-24mA)
- High-speed: 10ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 25µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- Capable of driving 60 74LSTTL loads
- Wide operating temperature range: Ta=−40~+85°C

APPLICATION

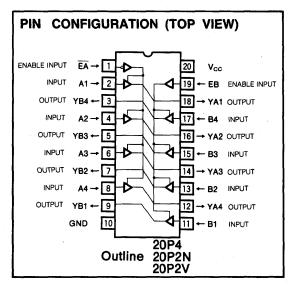
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HCT241-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS241.

The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

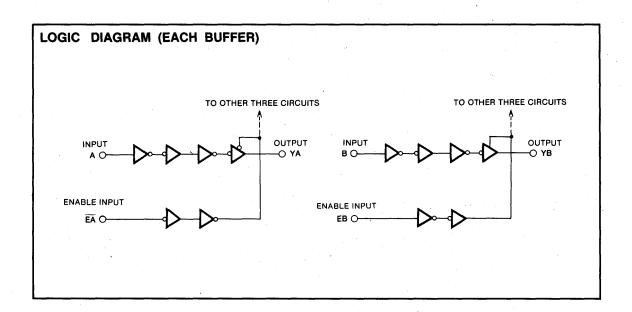
As the inputs are TTL level, the device can be used as a level converter from LSTTL to high-speed CMOS. In that case, no pull-up resistors are required.



The M74HCT241-1 consists of two independent blocks with each block containing four buffers.

When enable input \overline{EA} is low and input A is low then output YA will become low. However, if A is high then YA will become high. Inverted in the other block, a high enable input EB signal causes operation the same as that just described with input B signal output at YB.

When $\overline{\text{EA}}$ is high or EB is low then all Y within the block will become high-impedance state, irrespective of A or B.



M74HCT241-1P/FP/DWP

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER WITH LSTTL-COMPATIBLE INPUTS

FUNCTION TABLE (Note 1)

Inp	uts	Output
Α -	EA	YA
Ŀ	L	L
Η,	L	н
Y	Н	7

Inp	uts	Output	
В	B EB		
L	н	L	
Н	Н	Н	
х	L	Z	

Note 1 : Z : High impedance

X : Irrelevant

ABSOLUTE MAXIMUM RATINGS $(T_a = -40 \sim +85^{\circ}C)$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit	
Vcc	Supply voltage		-0.5~+7.0	. V	
V ₁ .	Input voltage		-0.5~V _{cc} +0.5	V	
Vo	Output voltage		-0.5~V _{cc} +0.5	V	
		V ₁ < 0V	-20		
lικ	Input protection diode current	V _I > V _{CC}	20	mA	
	Outside agentials diads summit	V ₀ < 0V	-20		
юк	Output parasitic diode current	V _o > V _{cc}	20	→ mA	
lo	Output current, per output pin	1	±50	mA	
Icc	Supply/GND current	V _{CC} , GND	±200	mA	
Pd	Power dissipation	(Note 2)	500	mW	
Tstg	Storage temperature range		−65∼+150	°	

Note 2 : M74HCT241-1FP, $T_a=-40\sim+75^\circ$ C and $T_a=75\sim85^\circ$ C are derated at $-7mW/^\circ$ C. M74HCT241-1DWP, $T_a=-40\sim+80^\circ$ C and $T_a=80\sim85^\circ$ C are derated at $-7mW/^\circ$ C.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85 \text{ C})$

Command and	, ba	Parameter		Limits				
Symbol	Pai			Тур	Max	Unit		
Vcc	Supply voltage		4.5		5.5	V		
V _I	Input voltage		0		Vcc	٧		
Vo	Output voltage	, ,	0		Vcc	٧		
Topr	Operating temperature ra	inge	-40		+85	ဗ		
A 4:	Innut via stime falltime	$V_{CC} = 4.5V$	0		25	ns/V		
t _r , t _f	Input risetime, falltime V _{CC} = 5.5V		0		15	ns/V		

ELECTRICAL CHARACTERISTICS ($V_{cc} = 5V \pm 10\%$, unless otherwise noted)

			Limits						
Symbol	Parameter	Test conditions		25℃			-40~+85°C		Unit
	<u>_</u> `			Min	Тур	Max	Min	Max	
V _{IH}	High-level input voltage	$V_0 = 0.1V$, $V_{CC} = 0.1V$ $ I_0 = 20\mu A$		2.0			2.0		٧
VIL	Low-level input voltage	$V_0 = 0.1V, V_0$ $ I_0 = 20\mu A$	$V_0 = 0.1V$, $V_{CC} = 0.1V$ $I_0 = 20\mu A$			0.8		0.8	٧
	High-level output voltage	gh-level output voltage $V_i = V_{iH}, V_{iL}$	$I_{OH} = -20\mu A$	V _{cc} -0.1			V _{cc} -0.1		٠,,
V _{OH}			$I_{OH} = -24 \text{mA}, \ V_{CC} = 4.5 \text{V}$	3. 98			3.84	· v	
.,		v = v	$I_{OL} = 20\mu A$			0.1		0.1	v
Vol	Low-level output voltage	$V_i = V_{iL}$ $I_{OL} =$	$I_{OL} = 24mA$, $V_{CC} = 4.5V$			0.39		0.5	\ \ \
(_{IH}	High-level input current	$V_i = V_{CC}$				0.1		1.0	
I _{IL}	Low-level input current	V _I = GND				-0.1		-1.0	μA
l _{ozh}	Off-state high-level output current	$V_{l} = V_{lH}, \ V_{lL},$	$V_0 = V_{CC}$			0.5		5.0	
lozL	Off-state low-level output current	$V_{l} = V_{lH_{s}} V_{lL}$	$V_i = V_{iHx}$ V_{iL} , $V_O = GND$			-0.5		-5. 0	μA
Icc	Quiescent supply current	VI = VCC, GNI	$0, \ l_0 = 0\mu A$			5.0		50.0	μА
Δlcc	Maximum quiescent supply current	$V_1 = 2.4V, 0.4$	V (Note 3)			2.7		2. 9	mA

Note 3: Only one input is set at this value and all other inputs are fixed at V_{CC} or GND.

SWITCHING CHARACTERISTICS ($v_{cc} = 5v$, $t_a = 25\%$)

Comple ed	Danier dan	Test conditions Limits				Unit
Symbol	Parameter	l'est conditions	Min	Тур	Max	Unit
t _{TLH}	Low-level to high-level and high-level to low-level				10	
tTHL	output transition time	0 - 50-5 (Note 5)			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = 50pF (Note 5)			16	
t _{PHL}	output propagation time (A — YA, B — YB)				16	ns
t _{PLZ}	Output disable time from low-level and high-level	C _L = 5 pF (Note 5)			18	
t _{PHZ}	(EA — YA, EB — YB)	CL = 5 pr (Note 5)			18	ns
t _{PZL}	Output enable time to low-level and high-level	C _L = 50pF (Note 5)			21	
t _{PZH}	(EA - YA, EB - YB)	CL — SOPF (Note 5)			21	ns

SWITCHING CHARACTERISTICS ($v_{cc} = 5v \pm 10\%$, $T_a = -40 \sim +85\%$)

					Limits			
Symbol	Parameter	Test conditions	25℃			-40~+85℃		Unit
			Min	Тур	Max	Min	Max	
t _{TLH}	Low-level to high-level and				12		15	
t _{THL}	high-level to low-level output transition time	•			12		15	ns
t _{PLH}	Low-level to high-level and				18		23	
t _{PHL}	output propagation time (A — YB, B — YB)				18	-	23	ns
t _{PLZ}	Output disable time from	C _L = 50pF (Note 5)			23		29	
t _{PHZ}	low-level and high-level				23		29	ns
t _{PZL}	Output enable time to	,			23		29	
t _{PZH}	low-level and high-level (EA — YA, EB — YB)				23		29	ns
Cı	Input capacitance				10		10	
Со	Off-state output capacitance	$\overline{EA} = V_{CC}, \overline{EB} = V_{CC}$			15		15	pF
C _{PD}	Power dissipation capacitance (Note 4)							, .

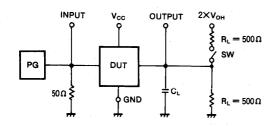
Note 4: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per buffer)

The power dissipated during operation under no-load conditions is calculated using the following formula:

P_D = C_{PD} • V_{CC}² • f₁+I_{CC} • V_{CC}

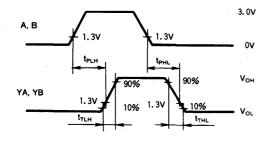


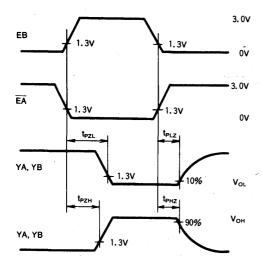
Note 5: Test Circuit



Parameter	sw
t _{TLH} , t _{THL}	Open
t _{PLZ}	Closed
t _{PHZ}	Open
t _{PZL}	Closed
t _{PZH}	Open

(1) The pulse generator (PG) has the following characteristics (10%~90%): t_f = 3ns, t_f = 3ns
 (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.





M74HC242P/FP/DP

QUADRUPLE 3-STATE INVERTING BUS TRANSCEIVER

DESCRIPTION

The M74HC242 is a semiconductor integrated circuit consisting of four bus transceivers with inverted outputs.

FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 10ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

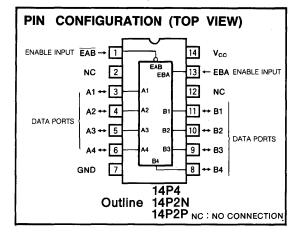
Use of silicon gate technology allows the M74HC242 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS242.

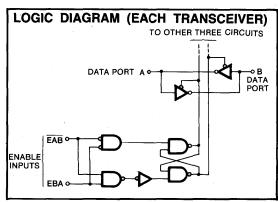
Two buffers with 3-state inverted outputs have their inputs and outputs mutually connected and can be used as buffers in both bidirectional.

The input/output direction is controlled by enable inputs $\overline{\mathsf{EAB}}$ and $\overline{\mathsf{EBA}}$.

When \overline{EAB} and EBA are both low, the data ports A will become input terminals and the data ports B will become output terminals. When \overline{EAB} and EBA are both high, B will become output terminals and A will become output terminals. Whichever the case, the inverted signals of the input terminals.

minals will appear at the output terminals. When EAB is high and EBA is low or when EAB is low and EBA is high, A and B will both become high-impedance state and they will be separated.





FUNCTION TABLE (Note 1)

	Inputs .		puts
EAB	EBA	Α	В
Н	Н	ō	1
L	н	Z	Z
Н	L	Z	Z
L	L	1	ō

Note 1: I : Input terminal

O : Output terminal (inverted outputs)

Z : High impedance

ABSOLUTE MAXIMUM RATINGS $(T_a = -40 \sim +85^{\circ}C)$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit	
Vcc	Supply voltage	,	-0.5~+7.0	V	
Vı	Input voltage		-0.5~V _{cc} +0.5	V	
Vo	Output voltage		-0.5~V _{cc} +0.5	V	
		√ V₁ < 0V	-20		
lik	Input protection diode current	v _I > V _{CC}	$V_{\rm I} > V_{\rm CC}$	20	mA
	0.1.1.1	V _o < 0V	-20	T	
lok	Output parasitic diode current	$v_o > v_{cc}$	20	mA	
lo	Output current per output pin		±35	mA	
Icc	Supply/GND current	V _{CC} , GND	±75	mA	
Pd	Power dissipation	(Note 2)	500	mW	
Tstg	Storage temperature range		-65~+150	င	

Note 2 : M74HC242FP, T $_a$ = $-40\sim$ +60°C and T $_a$ = $60\sim$ 85°C are derated at -6mW/°C. M74HC242DP, T $_a$ = $-40\sim$ +50°C and T $_a$ = $50\sim$ 85°C are derated at -5mW/°C.



QUADRUPLE 3-STATE INVERTING BUS TRANSCEIVER

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85\%)$

0				Limits				
Symbol	Pa	Parameter -		Тур	Max	Unit		
Vcc	Supply voltage	Supply voltage			6	V -		
Vi	Input voltage	Input voltage			Vcc	٧		
Vo	Output voltage	Output voltage			Vcc	V		
Topr	Operating temperature ra	ange	-40	-	+85	°C		
		V _{CC} = 2.0V	0		1000			
t _r , t _f	input risetime, faiitime	V _{CC} = 4.5V	0		500	ns		
	$V_{CC} = 6.0V$		0		400			

ELECTRICAL CHARACTERISTICS

	[Test conditions		Limits					j i	
Symbol	Parameter			25℃			-40~+85°C		Unit	
				V _{cc} (V)	Min	Тур	Max	Min	Max	
			0.111	2, 0	1.5			1.5		
V _{IH}	High-level input voltage	, ,	$_{0} = 0.1V, V_{CC} - 0.1V$		3.15			3.15		V .
	*	$ I_O = 20\mu A$		6.0	4. 2			4.2		
		$V_0 = 0.1V, V_{CC} = 0.1V$		2.0			0.5		0.5	
VIL	Low-level input voltage		o—0.1V	4.5			1.35	ŀ	1.35	v i
		$ I_{O} = 20\mu A$		6.0			1.8		1.8	
	High-level output voltage $V_i = V_{iH}, \ V_{iL}$	$I_{OH} = -20\mu A$	2.0	1.9			1.9			
		$I_{OH} = -20\mu A$	4.5	4.4		İ	4.4			
VoH		$V_i = V_{iH}, V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		· v
			$I_{OH} = -6.0 \text{mA}$	4.5	4. 18			4.13		ĺ
		ľ	$I_{OH} = -7.8 \text{mA}$	6.0	5. 68			5.63		
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
			$I_{OL} = 20 \mu A$	4.5		ľ	0.1		0.1	
VoL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
			$I_{OL} = 6.0 \text{mA}$	4.5			0.26		0.33	
			I _{OL} = 7.8mA	6.0			0. 26		0.33	
I _{IH}	High-level input current	$V_I = 6V$		6.0			0.1		1.0	μΑ
I _{IL}	Low-level input current	$V_i = 0V$		6.0			-0.1		-1.0	μΑ
lozh	Off-state high-level output current	$V_i = V_{iH}, \ V_{iL},$	$V_0 = V_{CC}$	6.0			0.5		5.0	μA
lozL	Off-state low-level output current	$V_i = V_{iH}, \ V_{iL},$	Vo = GND	6.0			-0.5		-5. 0	μΑ
Icc	Quiescent supply current	VI = VCC, GNE	$I_0 = 0 \mu A$	6.0			4.0		40.0	μA

QUADRUPLE 3-STATE INVERTING BUS TRANSCEIVER

SWITCHING CHARACTERISTICS ($v_{cc} = 5v$, $T_a = 25\%$)

Symbol	Parameter	Test conditions		Unit		
Symbol		rest conditions	Min	Тур	Max	Unit
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time	C = 5055 (Note 4)			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = 50pF (Note 4)			18	ns
t _{PHL}	output propagation time $(A - B, B - A)$				18	ns
t _{PLZ}	Output disable time from low-level and high-level	C _L = 5 pF (Note 4)			25	ns
t _{PHZ}	(EAB - A, B, EBA - B, A)	CL = 5 pr (Note 4)			25	ns
t _{PZL}	Output enable time to low-level and high-level	C ₁ = 50pF(Note 4)			28	ns
t _{PZH}	(EAB - A, B, EBA - B, A)	CL — SOPP(Note 4)			28	ns

SWITCHING CHARACTERISTICS ($v_{cc} = 2\sim 6V$, $T_a = -40\sim +85^{\circ}C$)

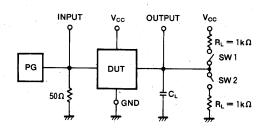
						Limits			
Symbol	Parameter	Test conditions			25℃		−40 ~	+85℃	Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	
	· ·		2.0			60		75	
t _{TLH}	Low-level to high-level and	,	4.5			12		15	ns
	high-level to low-level	C _L = 50pF (Note 4)	6.0	·		10		13	
	ingi level to low level	SE SOPI (Note 1)	2.0			60		75	ĺ
t _{THL}	output transition time		4.5			12		15	ns
			6.0			10		13	
			2.0			100		126	
t _{PLH}			4.5			20		25	ns
		C _L = 50pF (Note 4)	6.0			17		21	
		CL — Sopr (Note 4)	2.0			100		126	
t _{PHL}	Low-level to high-level and		4.5			20		25	ns
	high-level to low-level		6.0			. 17		21	
	output propagation time		2.0			150		189	
t _{PLH}	(A - B, B - A)		4.5			30		38	ns
			6.0			26		32	
		C _L = 150pF (Note 4)	2.0			150		189	
t _{PHL}			4.5			30		38	ns
			6.0			26	:	32	
			2.0			150		189	
t _{PLZ}	Output disable time from		4.5			30		38	ns
			6.0			26		32	"
	low-level and high-level	C _L = 50pF (Note 4)	2, 0			150		189	,
t _{PHZ}	(EAB - A, B, EBA - B, A)		4.5		ļ	30		38	ns
-FHZ		· ·	6.0		l	26		32	
		 	2.0			150		189	
t _{PZL}			4.5			30		38	ns
*PZL	*		6.0		İ	26	İ	32	. 113
	-	C _L = 50pF (Note 4)	2, 0			150		189	
t _{PZH}	Output enable time to low-level		4.5			30		38	ns
чехн	Culput enable lime to low-level	1	6.0			26	ľ	32	113
	and high-level		2.0			200		252	· · · · · · · · · · · · · · · · · · ·
	(EAB - A, B, EBA - B, A)		4.5			40		50	ns
t _{PZL}	(EAB - A, B, EBA - B, A)								กร
	-	C _L = 150pF (Note 4)	6.0			200		43	
		1	2.0			1 1	1	252	
t _{PZH}			4.5			40		50	ns
_	 		6.0			34	<u> </u>	43	<u> </u>
Cı	Input capacitance					10		10	pF
Co	Off-state output capacitance					15		15	pF
CPD	Power dissipation capacitance (Note 3)				58				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per transceiver) The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$



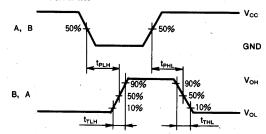
QUADRUPLE 3-STATE INVERTING BUS TRANSCEIVER

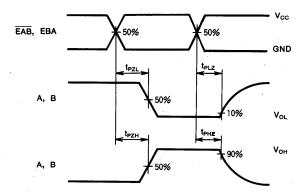
Note 4: Test Circuit



Parameter	SW1	SW 2
t _{TLH} , t _{THL} t _{PLH} , t _{PHL}	Open	Open
t _{PLZ}	Closed	Open
t _{PHZ}	Open	Closed
t _{PZL}	Closed	Open
t _{PZH}	Open	Closed

- (1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
 (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.





M74HC243P/FP/DP

QUADRUPLE 3-STATE NONINVERTING BUS TRANSCEIVER

DESCRIPTION

The M74HC243 is a semiconductor integrated circuit consisting of four bus transceivers with noninverted outputs.

FEATURFEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 12ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_A=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2∼6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

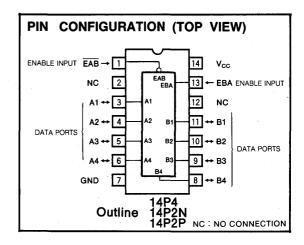
Use of silicon gate technology allows the M74HC243 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS243.

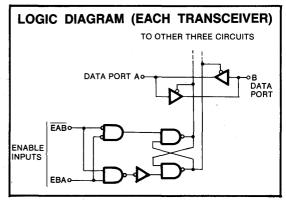
Two buffers with 3-state noninverted outputs have their inputs and outputs mutually connected and can be used as buffers ia both directions.

The input/output direction is controlled by enable inputs $\overline{\text{EAB}}$ and $\overline{\text{EBA}}$.

When \overline{EAB} and EBA are both low, the data prots A will become input terminals and the data ports B will become output terminals. When \overline{EAB} and EBA are both high, B will become input terminals and A will become output terminals.

Whichever the case, the same signals as at the input terminals will appear at the output terminals. When $\overline{\text{EAB}}$ is high and EBA is low or when $\overline{\text{EAB}}$ is low and EBA is high, A and B will both become high-impedance state and they will be separated.





FUNCTION TABLE (Note 1)

	outs	Data ports			
EAB	EBA	Α	В		
Н	н	0	I		
L	Н	Z	z		
н	L	Z	Z		
L	L		0		

Note 1: I : Input terminal

O: Outputs

Z : High impedance

ABSOLUTE MAXIMUM RATINGS $(T_a = -40 \sim +85 ^{\circ}C)$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
V _I	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
	lamina manaka akina dibada a samanak	V ₁ < 0V	-20	
lικ	Input protection diode current	V ₁ > V _{CC}	20	mA
	Output passaids diada assess	V ₀ < 0V	-20	
lok	Output parasitic diode current	$v_o > v_{cc}$	- 20	mA
lo	Output current per output pin		±35	mA
Icc	Supply/GND current	V _{CC} , GND	±75	mA
Pd	Power dissipation	(Note 2)	500	· mW
Tstg	Storage temperature range		-65~+150	°C

Note 2 : M74HC243FP, T $_a$ = $-40\sim+60^\circ$ C and T $_a$ = $60\sim85^\circ$ C are derated at -6mW/°C. M74HC243DP, T $_a$ = $-40\sim+50^\circ$ C and T $_a$ = $50\sim85^\circ$ C are derated at -5mW/°C.



QUADRUPLE 3-STATE NONINVERTING BUS TRANSCEIVER

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85^{\circ}C)$

		Parameter		Limits				
Symbol	Par	rameter	Min	Тур	Max	Unit		
Vcc	Supply voltage		- 2		6	V		
Vı	input voltage		0		Vcc	٧		
V _o	Output voltage		0		Vcc	V		
Topr	Operating temperature ra	inge	-40		+85	င		
		V _{CC} = 2.0V	0		1000			
tr. tf	input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns		
•	,	V _{CC} = 6.0V	0		400	1		

ELECTRICAL CHARACTERISTICS

							Limits	1000	*	100
Symbol	Symbol Parameter		Test conditions			25℃		-40~+85°C		Unit
ļ		V _{cc} (V)		V _{cc} (V)	Min	Тур	Max	Mìn	Max	
		V = 0.1V V	-0.1V	2.0	1.5			1.5		
VIH	High-level input voltage	$ V_0 = 0.1V, V_{CO}$ $ I_0 = 20\mu A$	$_{0} = 0.1V, V_{CC} - 0.1V$		3. 15			3.15		V
		1161 - 20μΑ	<u></u>	6.0	4. 2			4. 2		
		Vo = 0.1V Voo	$V_0 = 0.1V, V_{CC} = 0.1V$		-		0.5		0.5	
V _{IL}	Low-level input voltage	$ I_0 = 20\mu A$	0.14	4.5			1.35		1.35	v
		1101 - 2022		6.0			1.8		1.8	
\			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
		٠.	$t_{OH} = -20\mu A$	4.5	4.4			4.4	İ	
VoH	High-level output voltage	$V_{l} = V_{lH}, V_{lL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		v
1			$I_{OH} = -6.0 \text{mA}$	4.5	4.18			4.13		
			$I_{OH} = -7.8 \text{mA}$	6.0	5. 68			5. 63		
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
		,	$I_{OL} = 20 \mu A$	4.5			0.1		0.1	
VoL	Low-level output voltage	$V_{I} = V_{IH}, V_{IL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
1			$I_{OL} = 6.0 \text{mA}$	4.5		ļ	0.26		0.33	-
			I _{OL} = 7.8mA	6.0			0. 26		0.33	
l _{IH}	High-level input current	V _I = 6V		6.0		<u></u> _	0.1		1.0	μA
I _{IL}	Low-level input current	$V_1 = 0V$		6.0			-0.1		-1.0	. μΑ
I _{OZH}	Off-state high-level output current	$t V_i = V_{iH_1} V_{iL_1} V_O = V_{CC}$		6.0			0.5		5.0	μA
lozL	Off-state low-level output current	$V_i = V_{iH}, \ V_{iL}, \ V_O = GND$		6.0			-0.5		-5. 0	μA
loc	Quiescent supply current	VI = VCC, GND	$I_0 = 0\mu A$	6.0			4.0		40.0	μA

QUADRUPLE 3-STATE NONINVERTING BUS TRANSCEIVER

SWITCHING CHARACTERISTICS $(v_{cc} = 5v, T_a = 25^{\circ}C)$

Symbol	Parameter	Test conditions		Unit		
Cymbol	Palanetei	rest conditions	Min	Тур	Max	Unit
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time	C _L = 50pF (Note 4)			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level				18	ns
t _{PHL}	output propagation time (A - B, B - A)			,	18	ns
t _{PLZ}	Output disable time from low-level and high-level	$C_L = 5 pF (Note 4)$			25	ns
t _{PHZ}	(EAB - A, B, EBA - B, A)	CL — 5 pr (Note 4)			25	ns
t _{PZL}	Output enable time to low-level and high-level	C _L = 50pF (Note 4)			28	ns
t _{PZH}	$(\overline{EAB} - A, B, EBA - B, A)$	CL = 50pr (Note 4)			28	ns

SWITCHING CHARACTERISTICS $(v_{CC} = 2\sim 6V, T_a = -40\sim +85^{\circ}C)$

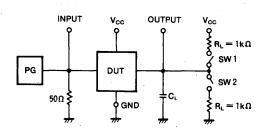
	,					Limits			1
Symbol	Parameter	Test conditions			25℃		-40 ~	+85℃	Unit
			V _{CC} (V)	Min	Тур	Max	Min	Max	<u></u>
			2.0			60		75	į
t _{TLH}	Low-level to high-level and		4.5			12		15	ns
	high lavel to lave towal	$C_L = 50pF (Note 4)$	6.0			10		13	
	high-level to low-level	C _L = 50pr (Note 4)	2.0			60		75	
t _{THL}	output transition time		4.5			12		15	ns
			6.0			10		13	
			2.0			100		126	
t _{PLH}			4.5		[20		25	ns
			6.0			17		21	
	1	$C_L = 50pF (Note 4)$	2.0			100		126	
t _{PHL}	Low-level to high-level and		4.5		l	20		25	ns
	high-level to low-level		6, 0			17		21	
	output propagation time		2.0			150		189	
t _{PLH}	(A - B, B - A)		4.5			30		38	ns
TPLA	, , , , , , , , , , , , , , , , , , , ,	1	6.0			26		32	
		C _L = 150pF (Note 4)	2.0			150		189	
t _{PHL}			4.5			30		38	ns
PHL	·	6.0			26		32		
			2.0			150		189	<u> </u>
t _{PLZ}	Output disable time from		4.5	j		30		38	ns
PLZ	Suput disable time from		6.0	1		26		32	1,13
	low-level and high-level	C _L = 50pF (Note 4)	2, 0			150		189	
t	(EAB - A, B, EBA - B, A)		4.5			30		38	ns
t _{PHZ}	(EAB - A, B, EBA - B, A)		6.0			26		32	115
		 	2.0			150		189	
			4.5			30		38	
t _{PZL}			6.0	ĺ	1	26		32	ns
		C _L = 50pF (Note 4)				+		 	
	Output anable time to low level		2.0 4.5			150 30		189 38	
t _{PZH}	Output enable time to low-level		,		1.			1	ns
	and high-level		6.0		-	26		32	
	1		2.0			200		252	
t _{PZL}	(EAB - A, B, EBA - B, A)		4.5	ļ		40		50	ns
		C _L = 150pF (Note 4)	6.0			34	/ .	43	
			2.0			200		252	
t _{PZH}			4.5		1	40		50	ns
		<u> </u>	6.0			34	ļ	43	
Cı	Input capacitance	ļ				10		. 10	pF
Co	Off-state output capacitance	<u> </u>				15		15	pF
CPD	Power dissipation capacitance (Note 3)		1	l	71	1	}	1	pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per transceiver) The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$



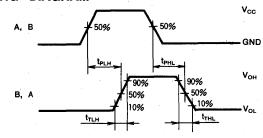
QUADRUPLE 3-STATE NONINVERTING BUS TRANSCEIVER

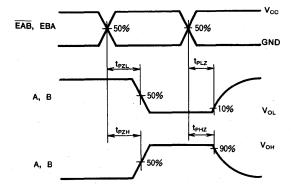
Note 4: Test Circuit



Parameter	SW 1	SW 2
t _{TLH} , t _{THL} t _{PLH} , t _{PHL}	Open	Open
t _{PLZ}	Closed	Open
t _{PHZ}	Open	Closed
t _{PZL}	Closed	Open
t _{PZH}	Open	Closed

- (1) The pulse generator (PG) has the following characteristics (10% \sim 90%): $t_{\rm f}=6$ ns, $t_{\rm f}=6$ ns (2) The capacitance C_L includes stray wiring
- capacitance and the probe input capacitance.





MT4HC244P/FP/DWP

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER

DESCRIPTION

The M74HC244 is a semiconductor integrated circuit consisting of two blocks of 3-state non-inverting buffers each with four independent circuits that share a common enable input.

FEATURES

- High-fanout 3-state output: (I_{OI} =6mA, I_{OH}=−6mA)
- High-speed: 10ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max
 (V_{CC}=5V, T_a=25℃, quiescent state)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2∼6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC244 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS244.

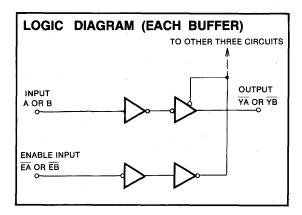
The M74HC244 consists of two independent blocks with each block containing four buffers.

When enable input \overline{E} is low and input A (or B) is low then output Y will become low. However, if A (or B) is high then Y will become high.

When \overline{E} is high then all outputs within the block will become high-impedance state, irrespective of A (or B).

All eight buffer circuits can be controlled simultaneously by connecting $\overline{\mathsf{EA}}$ and $\overline{\mathsf{EB}}$ of the two blocks.

CONFIGURATION (TOP VIEW) ENABLE INPUT EA 20 V_{CC} ← EB ENABLE INPUT 18 → YA1 OUTPUT \overline{A} 17 INPUT A2 -← B4 INPUT OUTPUT YB3 ← → YA2 OUTPUT INPUT A3 → 6 15 ← B3 INPUT OUTPUT YB2 ← → YA3 OUTPUT A4 ← B2 INPUT OUTPUT YB1 -→ YA4 OUTPUT 12 GND 10 ← R1 INPLIT 20P4 Outline 20P2N 20P2V



FUNCTION TABLE (Note 1)

Inj	Inputs		
А, В	EA, EB	YA, YB	
Ļ	Ĺ	L.	
Н	L	Н	
X	х		

Note 1 : Z : High impedance X : Irrelevant

ABSOLUTE MAXIMUM RATINGS $(T_a = -40 \sim +85 \degree$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	٧
Vo	Output voltage		-0.5~V _{cc} +0.5	V
		V ₁ < 0V	-20	
IIK	Input protection diode current	V _I > V _{CC}	20	mA
		V ₀ < 0V	-20	
lok	Output parasitic diode current	Vo > Vcc	20	mA .
lo	Output current per output pin		±35	mA
Icc	Supply/GND current	V _{CC} , GND	±75	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65~+150	ဗ

Note 2 : M74HC244FP, $T_a=-40\sim+75^{\circ}$ C and $T_a=75\sim85^{\circ}$ C are derated at -7mW/°C. M74HC244DWP, $T_a=-40\sim+80^{\circ}$ C and $T_a=80\sim85^{\circ}$ C are derated at -7mW/°C.

RECOMMENDED OPERATING CONDITIONS (Ta = -40~+85℃)

Compleal	Parameter			Limits				
Symbol	, Pa	rameter	Min	Тур	Max	Unit		
Vcc	Supply voltage		2		6	٧		
Vı	Input voltage		. 0		Vcc	٧		
Vo	Output voltage		0		Vcc	V		
Topr	Operating temperature ra	ange	-40		+85	ဗ		
		$V_{CC} = 2.0V$	0		1000			
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns		
		V _{CC} = 6.0V	- 0		400			

ELECTRICAL CHARACTERISTICS

			*				Limits			
Symbol	Symbol Parameter		Test conditions $V_{CC}(V)$			25℃			-40~+85°C	
					Min	Тур	Max	Min	Max	
		$V_0 = V_{CC} - 0.1$,	2.0	1.5			1.5		
VIH	High-level input voltage	$ V_0 - V_{CC} - 0.1V$ $ I_0 = 20\mu A$		4.5	3.15	ĺ		3.15		V
	1	1101 - 20µA	$I = 20\mu$ A		4. 2			4.2		
		$V_0 = 0.1V, V_{00}$	_0.17	2.0			0.5		0.5	
VIL	Low-level input voltage	$ V_0 = 0.1V, V_{CO} $ $ I_0 = 20\mu A$	5—0.1 V	4.5			1.35		1.35	V
	<u> </u>	1101 - 20μΑ	$= 20\mu A$				1.8		1.8	
			$i_{OH} = -20\mu A$	2.0	1.9			1.9		
	y - 1		$I_{OH} = -20\mu A$	4.5	4. 4			4.4		
VoH	High-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		٧
	`.		$I_{OH} = -6.0 \text{mA}$	4.5	4. 18			4.13		
	· · · · · · · · · · · · · · · · · · ·		$I_{OH} = -7.8 \text{mA}$	6.0	5. 68			5.63		
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
]		$I_{OL} = 20 \mu A$	4.5			0.1		0.1	
VoL	Low-level output voltage	$V_I = V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
			I _{OL} = 6.0mA	4.5			0. 26		0.33	
			$I_{OL} = 7.8 \text{mA}$	6.0			0. 26		0.33	
I _{IH}	High-level input current	$V_i = 6V$		6.0			0.1		1.0	μА
I _{IL}	Low-level input current	$V_i = 0V$		6.0			-0.1		-1.0	μA
lozh	Off-state high-level output current	$V_i = V_{iH}, \ V_{iL}, \ V_O = V_{CC}$		6.0			0.5		5.0	μA
lozL	Off-state high-level output current	$V_i = V_{iH}, \ V_{iL}, \ V_O = GND$		6.0			-0.5		-5.0	μA
Icc	Quiescent supply current	$V_1 = V_{CC}$, GND	$I_0 = 0 \mu A$	6.0			4.0		40.0	μΑ

SWITCHING CHARACTERISTICS ($v_{cc} = 5v$, $\tau_a = 25^{\circ}C$)

Comple et	Barrens	T-stditions		Limits			
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit	
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns	
t _{THL}	output transition time	C _L = 50pF (Note 4)			10	ns	
t _{PLH}	Low-level to high-level and high-level to low-level				20	ns	
t _{PHL}	output propagation time (A — YA, B — YB)				20	ns	
t _{PLZ}	Output disable time from low-level and high-level	C = E = E (Note 4)			25	ns	
t _{PHZ}	(EA - YA, EB - YB)	C _L = 5 pF (Note 4)			25	ns	
t _{PZL}	Output enable time to low-level and high-level	C ₁ = 50pF (Note 4)			28	ns	
t _{PZH}	(EA - YA, EB - YB)	CL — SUPP (Note 4)			28	ns	

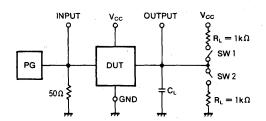
SWITCHING CHARACTERISTICS $(v_{cc} = 2\sim6V, T_a = -40\sim+85^{\circ}C)$

						Limits	,]
Symbol	Parameter	Test conditions			25℃	Ţ	-40~	+85°C	Unit
		·	V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0			60		75	
t _{TLH}	Low-level to high-level and		4. 5			12		15	ns
	high-level to low-level	C _L = 50pF (Note 4)	6.0			10		13	
			2.0			60		. 75	
t _{THL}	output transition time		4.5			12		15	ns
			6.0			10		13	
			2.0			115		145	ĺ
t _{PLH}			4.5			23	1	29	ns
		C _L = 50pF (Note 4)	6.0	,		20		25	
			2.0			115		145	
t _{PHL}	Low-level to high-level and	-	4.5			23		29	ns
	high-level to low-level	,	6.0	-		20	-	25	-
	output propagation time	, i	2.0			165		208	
t _{PLH}	(A - YA, B - YB)		4.5			33		42	ns
		C _L = 150pF (Note 4)	6.0			28		35	
			2.0			165		208	ļ
t _{PHL}	PHL		4.5			33		42	ns
	<u> </u>		6.0			28		35	
			2.0			150		189	1
t _{PLZ}	Output disable time from		4.5			30		38	ns
	low-level and high-level	C _L = 50pF (Note 4)	6.0			26		32	
	$(\overline{EA} - YA, \overline{EB} - YB)$		2.0			150		189	
t _{PHZ}	(EA — YA, EB — YB)	·	4.5			30		38	ns
			6.0		-	26			-
			2.0	ì		150 30		189	
t _{PZL}			4. 5 6. 0			26		38	ns
		C _L = 50pF (Note 4)	2.0			150		189	
•	Output enable time to low-level		4.5			30		38	ns
t _{PZH}	Output enable time to low-level	·	6.0	ŀ	Į	26		32	115
	and high-level		2.0	-		200	 	252	
t _{PZL}	$(\overline{EA} - YA, \overline{EB} - YB)$		4.5		1	40		50	ns
*PZL	10, 10,		6.0			34		43	115
	· ·	C _L = 150pF (Note 4)	2.0	 	-	200	 	252	
t _{PZH}			4.5		1	40		50	ns
*PZH	1	/	6.0			34		43	113
Cı	Input capacitance		- 0.0			10		10	pF
Co	Off-state output capacitance	$\overline{EA} = V_{CC}, \ \overline{EB} = V_{CC}$				15	 	15	pF
C _{PD}	Power dissipation capacitance (Note 3)	vcc, vcc	-		57	13	 	13	pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per buffer) The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$

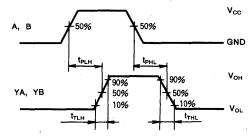


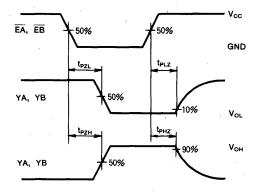
Note 4: Test Circuit



Parameter	SW 1	SW 2
t _{TLH} , t _{THL}	Open	Open
t _{PLZ}	Closed	Open
t _{PHZ}	Open	Closed
t _{PZL}	Closed	Open
t _{PZH}	Open	Closed

- (1) The pulse generator (PG) has the following characteristics (10%~90%): t_f = 6ns, t_f = 6ns
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.





M74HC244-1P/FP/DWP

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER

DESCRIPTION

The M74HC244-1 is a semiconductor integrated circuit consisting of two blocks of 3-state non-inverting buffers each with four independent circuits that share a common enable input.

FEATURES

- High-fanout 3-state output: (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed: 8ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 25µW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 60 74LSTTL loads
- Wide operating voltage range: V_{cc}=2~6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC244-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS244.

The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

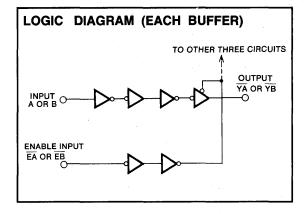
The M74HC244-1 consists of two independent blocks with each block containing four buffers.

When enable input \overline{E} is low and input A (or B) is low then output Y \widetilde{w} ill become low. However, if A (or B) is high then Y will become high.

When \overline{E} is high then all outputs within the block will become high-impedance state, irrespective of A (or B).

All eight buffer circuits can be controlled simultaneously by connecting \overline{EA} and \overline{EB} of the two blocks.

PIN CONFIGURATION (TOP VIEW) ENABLE INPUT EA 20 V_{CC} INPUT A1 19 ← EB ENABLE INPUT OUTPUT YB4 + 18 → YA1 OUTPUT INPUT A2 \rightarrow 4 17 ← **B4** INPUT OUTPUT YB3 + → YA2 OUTPUT INPUT A3 --6 15 ← B3 INPUT OUTPUT YB2 + → YA3 OUTPUT 14 INPUT ← B2 INPUT OUTPUT YB1 + 12 → YA4 OUTPUT 9 GND 11 ← B1 INPUT 20P4 Outline 20P2N 20P2V



FUNCTION TABLE (Note 1)

Inp	uts	output
A, B	YA, YB	
L	L	L
Н	L	Н
х	Н	Z

Note 1 : Z : High impedance X : Irrelevant

ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage		-0.5~+7.0	. V
Vı	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage	·	-0.5~V _{cc} +0.5	V
		V ₁ < 0V	-20	
lıĸ	Input protection diode current	V _I > V _{CC}	20	mA.
		V ₀ < 0V	-20	
lok	Output parasitic diode current	Vo > Vcc	20	mA
l _o	Output current, per output pin		±50	mA
loc	Supply/GND current	V _{CC} , GND	±200	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	°C

Note 2 : M74HC244-1FP, T_a = $-40\sim+75^\circ$ C and T_a = $75\sim85^\circ$ C are derated at -7mW/°C. M74HC244-1DWP, T_a = $-40\sim+80^\circ$ C and T_a = $80\sim85^\circ$ C are derated at -7mW/°C.

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85\%)$

				Limits				
Symbol	Pa	Parameter		Тур	Max	Unit		
Vcc	Supply voltage		2	****	6	V		
V ₁	Input voltage		0		Vcc	V		
V _o	Output voltage	•	0		V _{cc}	V		
Topr	Operating temperature ra	inge	-40		+85	င		
		V _{CC} = 2, 0V	0		500			
tr, tr	Input risetime, falltime	$V_{CC} = 4.5V$	0		50	ns/V		
		V _{CC} = 6 V	0		30]		

ELECTRICAL CHARACTERISTICS

		L		Limits						
Symbol	Parameter Test conditions		conditions		25°C			-40~+85°C		Unit
		V _{cc} (V)		Min	Тур	Max	Min	Max		
		V -V 01V		2.0	1.5			1.5		
VIH	High-level input voltage	$V_0 = V_{CC} - 0.1V$ $ I_0 = 20\mu A$		4.5	3.15			3.15		V
		$ 10 = 20\mu\text{A}$		6.0	4.2		ļ	4.2		
		V =0 1V V	0.11	2.0			0.5		0.5	
VIL	Low-level input voltage	$V_0 = 0.1V, V_{CC}$	U.1 V	4.5			1.35		1.35	V
+ 1	$1101 - 20\mu$	$ I_0 = 20\mu A$		6.0			1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
	I Bak Jawat a Asak watera	$V_i = V_{iH}, V_{iL}$	$I_{OH} = -20\mu A$	4.5	4.4			4.4		v
V _{OH}	High-level output voltage	VI = VIH, VIL	$I_{OH} = -20\mu A$	6.0	5.9			5.9	-	, v
			$I_{OH} = -24mA$	4.5	3. 98			3.84		
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
V	Law lavel autaut veltage		$I_{OL} = 20 \mu A$	4.5			0.1	}	0.1	· v ·
VoL	Low-level output voltage	$V_{l} = V_{lL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	\ \
			I _{OL} = 24mA	4.5			0.39		0.5	
l _{iH}	High-level input current	$V_1 = 6V$		6.0			0.1		1.0	μA
IIL	Low-level input current	$V_i = 0V$		6.0			-0.1		-1.0	μА
lozh	Off-state high-level output current	$V_i = V_{iH}, \ V_{iL}, \ V$	o = Vcc	6.0			0.5		5.0	μA
IozL	Off-state high-level output current	$V_i = V_{iH}, \ V_{iL}, \ V$	o = GND	6.0			-0.5		5.0	μA
Icc	Quiescent supply current	$V_i = V_{CC}$, GND,	$I_0 = 0\mu A$	6.0			5.0		50.0	μA

SWITCHING CHARACTERISTICS ($v_{cc} = 5v$, $t_a = 25$ °C)

Symbol	Bosometor	Test conditions		Limits			
Symbol	Parameter Test conditions	Min	Тур	Max	Unit		
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns	
t _{THL}	output transition time	C _L = 50pF (Note 4)			10	ns	
t _{PLH}	Low-level to high-level and high-level to low-level				16	ns	
t _{PHL}	output propagation time (A — YA, B — YB)				16	ns	
t _{PLZ}	Output disable time from low-level and high-level	C = 5 = 5 (Note 4)			18	ns	
t _{PHZ}	(EA - YA, EB - YB)	C _L = 5 pF (Note 4)			18	ns	
t _{PZL}	Output enable time to low-level and high-level	C _L = 50pF (Note 4)			23	ns	
t _{PZH}	(EA - YA, EB - YB)				23	ns	

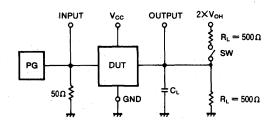
SWITCHING CHARACTERISTICS ($v_{cc} = 2\sim 6V$, $T_a = -40\sim +85^{\circ}C$)

						Limits			
Symbol	Parameter	Test conditions			25℃-		−40~	+85℃	Unit
		· ·	V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0			60		75	
t _{TLH}	Low-level to high-level and		4. 5			12		15	ļ
	high-level to low-level	-	6.0	,		10		13	
*	liigh-level to low-level		2.0			60		75	ns
t _{THL}	output transition time	·	4.5			12		15	
			6.0			10		13	
			2, 0			90		115	
t _{PLH}	Low-level to high-level and		4.5			18		23	ļ
	high-level to low-level		6.0			15		20	
	output propagation time		2. 0			90		115	ns
t _{PHL}	(A - YA, B - YB)	C ₁ = 50pF (Note 4)	4.5			18		23	
			6.0			15		20	
		C _L = 50pr (Note 4)	2.0			115		145	
t_{PLZ}	Output disable time from		4.5		l	23		29	}
	tour lovel and black tours		6.0			20	,	25	
	low-level and high-level		2. 0			115		145	ns
t _{PHZ}	(EA - YA, EB - YB)		4.5			23		29	
			6.0			20		25	ļ
			2. 0			115		145	
t _{PZL}	Output enable time to		4.5			23		29	
	Landard and black based		6.0			20		25	
	low-level and high-level		2.0			115		145	ns
t _{PZH}	(EA — YA, EB — YB)		4.5	,		23		29	
			6.0			20		25	
Cı	Input capacitance					10	-	10	
Со	Off-state output capacitance	EA = V _{CC} , EB = GND				15	-	15	рF
CPD	Power dissipation capacitance (Note 3)				43				

Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per buffer) The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$

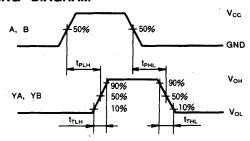


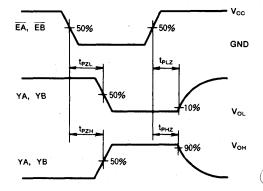
Note 4: Test Circuit



Parameter	SW
t _{TLH} , t _{THL}	Open
t _{PLH} , t _{PHL}	
t _{PLZ}	Closed
t _{PHZ}	Open
t _{PZL}	Closed
t _{PZH}	Open

- (1) The pulse generator (PG) has the following characteristics (10%~90%): $t_{\rm f}=3{\rm ns},\,t_{\rm f}=3{\rm ns}$
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.





MITSUBISHI HIGH SPEED CMOS

M74HCT244P/FP/DWP

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER WITH LSTTL-COMPATIBLE INPUTS

DESCRIPTION

The M74HCT244 is a semiconductor integrated circuit consisting of two blocks of 3-state non-invering buffers each with four independent circuits that share a common enable input.

FEATURES

- TTL level inputs V_{IL}=0.8V max, V_{IH}=2.0V min
- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 13ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2∼6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HCT244 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS244.

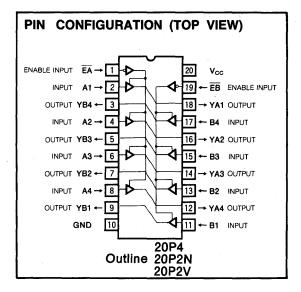
As the inputs are TTL level, the device can be used as a level converter from LSTTL to high-speed COMS. In that case, no pull-up resistros are required.

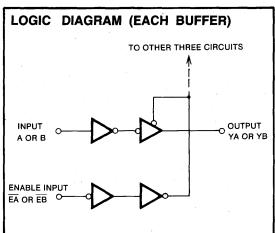
The M74HCT244 consists of two independent blocks with each block containing four buffers.

When enable input \overline{E} is low and input A (or B) is low then output Y will become low. However, if A (or B) is high then Y will become high.

When \overline{E} is high then all outputs within the block will become high-impedance state, irrespective of A (or B).

All eight buffer circuits can be controlled simultaneously by connecting $\overline{\text{EA}}$ and $\overline{\text{EB}}$ of the two blocks.





FUNCTION TABLE (Note 1)

In	puts	Output		
A, B				
L	L	L		
н	L	н		
×	Н	Z		

Note 1 : Z : High impedance X : Irrelevant

ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85$ °C, unless otherwise noted)

新工業等的原理的主義的數計的內容與於1911年

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
· V _I	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{CC} +0.5	V
		V ₁ < 0V	-20	
lıĸ	Input protection diode current	V _I > V _{CC}	20	mA .
		V ₀ < 0V	-20	
юк	Output parasitic diode current	Vo > Vcc	20	mA
lo	Output current per output pin		±35	mA
Icc	Supply/GND current	V _{CC} , GND	±75	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		-65~+150	ဗ

Note 2 : M74HCT244FP, T_a = $-40\sim+75^{\circ}$ C and T_a = $75\sim85^{\circ}$ C are derated at -7mW/°C. M74HCT244DWP, T_a = $-40\sim+80^{\circ}$ C and T_a = $80\sim85^{\circ}$ C are derated at -7mW/°C.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85 \degree C)$

Symbol			Limits				
Symbol	Parameter	Min	Тур	Max	Unit		
V _{cc}	Supply voltage	4.5		5.5	٧		
Vi	Input voltage	0		Voc	V.		
Vo	Output voltage	0		V _{CC}	٧		
Topr	Operating temperature range	-40		+85	ပ		
t _r , t _f	Input risetime, falltime	0		500	ns		

ELECTRICAL CHARACTERISTICS ($v_{cc} = 5v \pm 10\%$, unless otherwise noted)

Symbol	Parameter	,	Test conditions		25℃		-40~+85℃		Unit
			*	Min	Тур	Max	Min	Max	
ViH	High-level input voltage	$V_0 = V_{CC} - 0.1V$ $ I_0 = 20\mu A$	4	2, 0			2.0		٧
V _{IL}	Low-level input voltage	$V_0 = 0.1V, V_{CC}$ $ I_0 = 20\mu A$	-0.1V			0.8		0.8	٧
			$I_{OH} = -20\mu A$	V _{cc} -0.1			V _{cc} -0.1		
V _{OH}	High-level output voltage	$V_i = V_{iH}, \ V_{iL}$	$I_{OH} = -6.0 \text{mA}, V_{CC} = 4.5 \text{V}$	4.18			4.13		V
		,	$I_{OH} = -7.2 \text{mA}, V_{CC} = 5.5 \text{V}$	5.18		1	5.13		
,			$I_{OL} = 20\mu A$			0.1		0.1	
VoL	Low-level output voltage	$V_{I} = V_{IL}$	$I_{OL} = 6.0 \text{mA}, V_{CC} = 4.5 \text{V}$			0. 26		0.33	V
			$I_{OL} = 7.2 \text{mA}, V_{CC} = 5.5 \text{V}$	1 1		0.26		0.33	
1 _{IH}	High-level input current	$V_i = V_{CC}$				0.1		1.0	μA
I _{IL}	Low-level input current	$V_i = GND$				-0.1		-1.0	μA
lozh	Off-state high-level output current	$V_i = V_{iH}, \ V_{iL}, \ V$	o = V _{CC}			0.5		5.0	μА
lozL	Off-state low-level output current	$V_i = V_{iH}, \ V_{iL}, \ V$	o = GND			-0.5	1	-5.0	μA
Icc	Quiescent supply current	$V_i = V_{CC}$, GND,	$I_0 = 0\mu A$			4.0		40.0	μA
ΔI_{CC}	Maximum quiescent supply current	$V_1 = 2.4V, 0.4V$	(Note 3), $I_0 = 0 \mu A$	T		2.7		2.9	mA

Note 3: Only one input is set at this value and all other inputs are fixed at V_{CC} or GND.

MITSUBISHI HIGH SPEED CMOS M74HCT244P/FP/DWP

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER WITH LSTTL-COMPATIBLE INPUTS

SWITCHING CHARACTERISTICS ($V_{cc} = 5V$, $T_a = 25^{\circ}C$)

Symbol	Parameter	Test conditions		Limits			
	raianetei lest condition	rest conditions	Min	Тур	Max	Unit	
t _{TLH}	Low-level to high-level and high-level to low-level				12	ns	
t _{THL}	output transition time	C _L = 50pF (Note 5)			12	ns	
t _{PLH}	Low-level to high-level and high-level to low-level				25	ns	
t _{PHL}	output propagation time (A — YA, B — YB)	·			25	ns	
t _{PLZ}	Output disable time from low-level and high-level	C = 5 = 5 (Note 5)			27	ns	
t _{PHZ}	(EA - YA, EB - YB)	$C_L = 5 pF (Note 5)$			27	ns	
t _{PZL}	Output enable time to low-level and high-level	C _L = 50pF (Note 5)			32	ns	
t _{PZH}	(EA - YA, EB - YB)				32	ns	

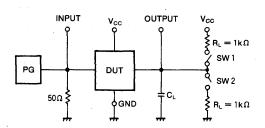
SWITCHING CHARACTERISTICS ($v_{cc} = 5v \pm 10\%$, $\tau_a = -40 \sim +85\%$)

				Limits					
Symbol	Parameter	. Test conditions	25℃			-40~+85℃		Unit	
			Min	Тур	Max	Min	Max		
t _{TLH}	low-level to high-level and	$C_1 = 50pF (Note 5)$.12		15	ns	
t _{THL}	high-level to low-level output transition time	CL = sopr (Note s)			12		15	ns	
t _{PLH}	Low-level to high-level and	C _L = 50pF (Note 5)			25		32	ns	
t _{PHL}	high-level to low-level	C _L = 50pr (Note 5)			25		32	ns	
t _{PLH}	output propagation time	C _L = 150pF(Note 5)			40		51	ns	
t _{PHL}	(A — YA, B — YB)				40		51.	ns	
t _{PLZ}	Output disable time from	O = 50-5 (N-1-5)			32		40	ns	
t _{PHZ}	low-level and high-level (EA — YA, EB — YB)	$C_L = 50 pF (Note 5)$. 32		40	ns	
t _{PZL}	Code de la contra del contra de la contra del contra de la contra del la contra del la contra del la contra del la contra del la contra del la contra del la contra del la contra del la contra del la c	O - 50-5 (Not-5)			32		40	ns	
t _{PZH}	Output enable time to low-level	$C_L = 50 pF \text{ (Note 5)}$			32		40	ns	
t _{PZL}	and high-level (EA - YA, EB - YB)	C ₁ = 150pF (Note 5)			47		59	ns	
t _{PZH}	(EA — YA, EB — YB)	$C_L = 150pr \text{ (Note 5)}$			47		59	ns	
C	Input capacitance				10		10	pF	
Со	Off-state output capacitance	$\overline{EA} = \overline{EB} = V_{CC}$			15		15	pF	
CPD	Power dissipation capacitance (Note 4)			45				pF	

Note 4: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per buffer)
The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$

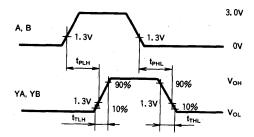


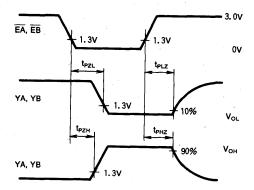
Note 5: Test Circuit



Parameter	SW1	SW 2
t _{TLH} , t _{THL}	Open	Open
t _{PLZ}	Closed	Open
t _{PHZ}	Open	Closed
t _{PZL}	Closed	Open
t _{PZH}	Open	Closed

- (1) The pulse generator (PG) has the following characteristics (10%~90%): t_f = 6ns, t_f = 6ns
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.







MITSUBISHI HIGH SPEED CMOS

M74HCT244-1P/FP/DWP

OCTAL 3-STATE NONINVERTING
BUFFER/LINE DRIVER/LINE RECEIVER WITH LSTTL-COMPATIBLE INPUTS

DESCRIPTION

The M74HCT244-1 is a semiconductor integrated circuit consisting of two blocks of 3-state non-invering buffers each with four independent circuits that share a common enable input.

FEATURES

- TTL level inputs V_{IL}=0.8V max, V_{IH}=2.0V min
- High-fanout 3-state output: (I_{OL}=24mA, I_{OH}=-24mA)
- High-speed: 10ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 25µW/package, max
 (V_{CC}=5V, T_A=25°C, quiescent state)
- Capable of driving 60 74LSTTL loads
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HCT244-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS244.

The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

As the inputs are TTL level, the device can be used as a level converter from LSTTL to high-speed COMS. In that case, no pull-up resistors are required.

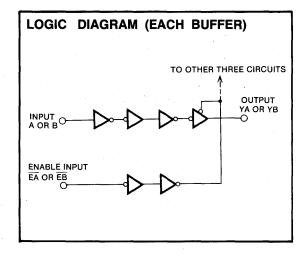
The M74HCT244-1 consists of two independent blocks with each block containing four buffers.

When enable input \overline{E} is low and input A (or B) is low then output Y will become low. However, if A (or B) is high then Y will become high.

When \overline{E} is high then all outputs within the block will become high-impedance state, irrespective of A (or B).

All eight buffer circuits can be controlled simultaneously by connecting \overline{EA} and \overline{EB} of the two blocks.

PIN CONFIGURATION (TOP VIEW) ENABLE INPUT EA 20 Vcc 19 ← EB ENABLE INPUT INPLIT OUTPUT YB4 ← 3 18 → YA1 OUTPUT INPUT A2 → 4 17 ← **B4** INPUT OUTPUT YB3 ← 5 16 → YA2 OUTPUT INPUT A3 → 6 15 ← B3 INPUT OUTPUT YB2 ← 7 → YA3 OUTPUT **→** 8 13 ← B2 INPUT INPLIT OUTPUT YB1 ← 9 → YA4 OUTPUT GND ← R1 INPLIT 20P4 Outline 20P2N 20P2V



FUNCTION TABLE (Note 1)

Int	Inputs		
A, B	A, B EA, EB		
L	L	L	
Н	L	Н	
×	Н	Z	

Note 1 : Z : High impedance X : Irrelevant

ABSOLUTE MAXIMUM RATINGS ($\tau_a = -40 \sim +85 \degree$ C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	V
V _o	Output voltage		-0.5~V _{cc} +0.5	· V
•		v _i < 0v	-20	T
I _{IK} Inpu	Input protection diode current	$v_i > v_{cc}$	20	mA
•	Outside and a second	V ₀ < 0V	-20	
ок	Output parasitic diode current	Vo > Vcc	20	mA
lo	Output current, per output pin		±50	mA
Icc	Supply/GND current	V _{CC} , GND	±200	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		-65~+150	င

Note 2 : M74HCT244-1FP, $T_a=-40\sim+75^\circ$ C and $T_a=75\sim85^\circ$ C are derated at $-7mW/^\circ$ C. M74HCT244-1DWP, $T_a=-40\sim+80^\circ$ C and $T_a=80\sim85^\circ$ C are derated at $-7mW/^\circ$ C.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85 \degree C)$

Symbol	Parameter			Unit		
			Min	Тур	Max	Onit
Vcc	Supply voltage		4.5		5.5	V
V ₁	Input voltage		0		Vcc	٧
Vo	Output voltage	Output voltage			Vcc	٧
Topr	Operating temperature ra	Operating temperature range			+85	c
	In a state of the	V _{CC} = 4.5V	0 :		25	/
t _r , t _f	Input risetime, falltime $V_{CC} = 5.5V$		0		15	ns/

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, unless otherwise noted)

				Limits					
Symbol	Parameter		Test conditions		25℃			+85°C	Unit
				Min	Тур	Max	Min	Max	
VIH	High-level input voltage	$V_0 = 0.1V$ $ I_0 = 20\mu A$		2.0			2.0		· v
VIL	Low-level input voltage	$V_0 = 0.1V, V_0$ $ I_0 = 20\mu A$	_C -0.1V			0.8		0.8	٧
VoH	Mah involved and a M	V – V V	$I_{OH} = -20\mu A$	V _{cc} -0.1			V _{cc} -0.1		>
• он	High-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OH} = -24 \text{mA}, \ V_{CC} = 4.5 \text{V}$	3. 98			3.84		· •
VoL	Low-level output voltage	$V_i = V_{iL}$	$I_{OL} = 20 \mu A$			0.1		0.1	V
VOL	Low-level output voltage	VI VIL	$I_{OL} = 24mA, V_{CC} = 4.5V$			0.39		0.5	•
I _{IH}	High-level input current	$V_i = V_{CC}$				0.1		1.0	
l _{IL}	Low-level input current	$V_I = GND$				-0.1		-1.0	μA
l _{ozh}	Off-state high-level output current	$V_i = V_{iH}, \ V_{iL},$	$V_0 = V_{CC}$			0.5		5.0	
lozL	Off-state low-level output current	$V_i = V_{iH}, \ V_{iL},$	$V_{l} = V_{lH}, V_{lL}, V_{O} = GND$			-0.5		-5.0	μΑ
l _{cc}	Quiescent supply current	VI = VCC, GNE	$0, \ I_0 = 0\mu A$			5.0		50.0	μA
Δlcc	Maximum quiescent supply current	$V_1 = 2.4V, 0.4$	V (Note 3)			2.7		2.9	mA

Note 3 : Only one input is set at this value and all other inputs are fixed at V_{CC} or GND.

MITSUBISHI HIGH SPEED CMOS M74HCT244-1P/FP/DWP

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER WITH LSTTL-COMPATIBLE INPUTS

SWITCHING CHARACTERISTICS (Vcc = 5V, Ta = 25°C)

Complete	Description	To de anadistana	Limits			11-14
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time	C _L = 50pF (Note 5)			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level				16	ns
t _{PHL}	output propagation time (A - YA, B - YB)				16	ns
t _{PLZ}	Output disable time from low-level and high-level	O = E = E (Nisto E)			18	ns
t _{PHZ}	(EA - YA, EB - YB)	$C_L = 5 pF (Note 5)$			18	ns
tpZL	Output enable time to low-level and high-level	0 = 50=5 (N=4=5)	T		23	ns
t _{PZH}	(EA - YA, EB - YB)	C _L = 50pF (Note 5)			23	ns

SWITCHING CHARACTERISTICS ($V_{cc} = 5V \pm 10\%$, $T_a = -40 \sim +85$ °C)

Symbol	Parameter		Limits					T
		Test conditions	25℃			-40~+85°C		Unit
			Min	Тур	Max	Min	Max	i
tTLH	Low-level to high-level and				12		15	
t _{THL}	high-level to low-level output transition time				12		15	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = 50pF (Note 5)			18		23	ns
t _{PHL}	output propagation time (A — YA, B — YB)				18		23	lis
t _{PLZ}	Output disable time from				23		29	
	low-level and high-level						 	ns
t _{PHZ}	(EA - YA, EB - YB)				23		29	
t _{PZL}	Output enable time to	·			23		29	
	low-level and high-level	}		ļ		ļ <u>.</u>		ns
t _{PZH}	(EA - YA, EB - YB)			1	23		29	ĺ
Cı	Input capacitance				10		10	
Со	Off-state output capacitance	$\overline{EA} = V_{CC}, \overline{EB} = V_{CC}$			15		15	pF
C _{PD}	Power dissipation capacitance (Note 4)]

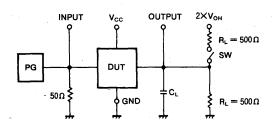
Note 4: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per buffer)

The power dissipated during operation under no-load conditions is calculated using the following formula:

P_D = C_{PD} • V_{CC}² • f₁+I_{CC} • V_{CC}

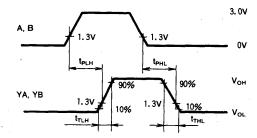


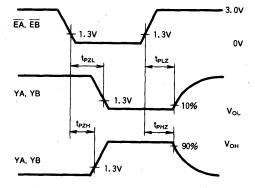
Note 5: Test Circuit



Parameter	SW
t _{TLH} , t _{THL} t _{PLH} , t _{PHL}	Open
t _{PLZ}	Closed
t _{PHZ}	Open
t _{PZL}	Closed
t _{PZH}	Open

- (1) The pulse generator (PG) has the following characteristics (10% \sim 90%): $t_f = 3$ ns, $t_f = 3$ ns
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.





MITSUBISHI HIGH SPEED CMOS

M74HC245P/FP/DWP

OCTAL 3-STATE NONINVERTING BUS TRANSCEIVER

DESCRIPTION

The M74HC245 is a semiconductor integrated circuit consisting of eight transceivers with noninverted outputs.

FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 13ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2∼6V
- Wide operating temperature range: T_a=-40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC245 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS245.

Two buffers with 3-state noninverted outputs have their inputs and outputs mutually connected and can be used as buffers in both directions.

The input/output direction is controlled by direction input DIR.

When DIR is high, the data ports A will become input terminals and the data ports B will become output terminals. When DIR is low, B will become input terminals and A will become output terminals.

When output enable input \overline{OE} is high, A and B will both become a high-impedance state and they will be separated.

FUNCTION TABLE (Note 1)

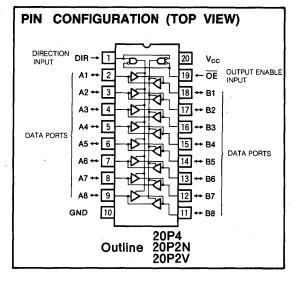
Inputs		Outputs		
OE	DIR	Α	В	
L	L	0	1	
L	Н	ı	0	
Ι	х	Z	Z	

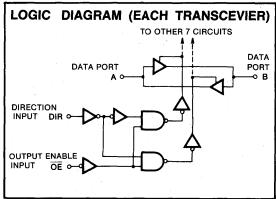
Note 1: |: Input terminal

O: Output terminal (noninverted output)

Z : High impedance (A and B are separated)

X: Irrelevant





OCTAL 3-STATE NONINVERTING BUS TRANSCEIVER

ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85 \, \text{°C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
Input pretection diede current	lanut mustaction dieda suurant	V ₁ < 0V	-20	
I _{IK}	Input protection diode current	$V_{I} > V_{CC}$	20	mA
		V ₀ < 0V	-20	
lok	Output parasitic diode current	Vo > Vcc	20	mA
lo	Output current per output pin		±35	mA
lcc	Supply/GND current	V _{CC} , GND	土75	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		-65∼+150	င

Note 2 : M74HC245FP, $T_a=-40\sim+75^\circ\text{C}$ and $T_a=75\sim85^\circ\text{C}$ are derated at -7mW/°C. M74HC245DWP, $T_a=-40\sim+80^\circ\text{C}$ and $T_a=80\sim85^\circ\text{C}$ are derated at -7mW/°C.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85^{\circ}C)$

Complement	Parameter			Limits				
Symbol			Min	Тур	Max	Unit		
Voc	Supply voltage		2		6	٧		
Vı	Input voltage		0		Vcc	٧		
Vo	Output voltage		0		Vcc	٧		
Topr	Operating temperature re	inge	-40		+85	°C		
	Input risetime, failtime	V _{CC} = 2.0V	0		1000			
t _r , t _f		$V_{CC} = 4.5V$	0		500	ns		
		$V_{CC} = 6.0V$	0		400			

ELECTRICAL CHARACTERISTICS

					•		Limits			
Symbol	Parameter	Test conditions V _{CC} (V)		25°C			-40~+85°C		Unit	
ļ.				V _{cc} (V)	Min	Тур	Max	Min	Max	
		V = 0.1V V	0.11	2.0	1.5			1.5		
VIH	High-level input voltage	$ \cdot \cdot = 20 \text{ m/s}$		4.5	3. 15			3.15		V
				6.0	4.2	·		4. 2	<u> </u>	
		$V_0 = 0.1V, V_{CC} = 0.1V$ 2.0				0.5		0.5		
VIL	Low-level input voltage	$ I_0 = 20\mu A$;0.1 V	4. 5	Ì	Ì	1.35]	1.35	` V
		1101 = 20µA		6.0			1.8	<u> </u>	1.8	
			$I_{OH} = -20\mu A$	2.0	1.9		Ì	1.9	}	
	4.		$I_{OH} = -20\mu A$	4.5	4.4			4.4		
V _{OH}	High-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		V
	·		$I_{OH} = -6.0 \text{mA}$	4.5	4.18			4.13		
			$I_{OH} = -7.8 \text{mA}$	6.0	5.68			5.63		
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
		1	$I_{OL} = 20 \mu A$	4.5			0.1	}	0.1	
VoL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
			$I_{OL} = 6.0 \text{mA}$	4.5			0.26		0.33	-
			I _{OL} = 7.8mA	6.0			0. 26		0.33	
l _{iH}	High-level input current	$V_1 = 6V$		6.0			0.1		1.0	μA
liL	Low-level input current	V _i = 0V		6.0			-0. 1		-1.0	μA
l _{ozh}	Off-state high-level output current	$V_i = V_{iH}, V_{iL}, V_{iL}$	$v_0 = v_{CC}$	6.0			0.5	,	5.0	μA
lozL	Off-state low-level output current	$V_i = V_{iH}, \ V_{iL}, \ V_{iL}$	o = GND	6.0			-0. 5		-5.0	μA
<u>-</u> 6	Quiescent supply current	Vi = Vcc, GND	$I_0 = 0 \mu A$	6.0			4.0		40.0	μA

OCTAL 3-STATE NONINVERTING BUS TRANSCEIVER

SWITCHING CHARACTERISTICS $(V_{cc} = 5V, T_a = 25^{\circ}C)$

Symbol	Parameter	Test conditions		Unit		
	Farameter	rest conditions	Min	Тур	Max	Unit
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time	$C_1 = 50 pF \text{ (Note 4)}$			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	CL — SUPF (Note 4)			21	ns
t _{PHL}	output propagation time (A - B, B - A)				21	ns
t _{PLZ}	Output disable time from low-level and high-level	$C_1 = 5 pF (Note 4)$			42	ns
t _{PHZ}	(OE - A, B)	C _L = 5 pr (Note 4)			42	ns
t _{PZL}	Output enable time to low-level and high-level	C _L = 50pF (Note 4)			42	ns
t _{PZH}	(OE - A, B)	OL — SOPE (NOTE 4)			42	ns

SWITCHING CHARACTERISTICS ($v_{cc} = 2\sim6V$, $T_a = -40\sim+85$ °C)

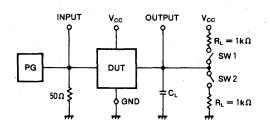
				Limits					
Symbol	Parameter	Test conditions		25°C −40~+85°C				+85℃	Unit
			V _{CC} (V)	Min	Тур	Max	Min	Max	
,			2.0			60		75	
t _{TLH}	Low-level to high-level and		4.5			12		15	ns
	high-level to low-level	C _L = 50pF (Note 4)	6.0			10		13	
	migri-lever to low-lever	CL — SOPP (Note 4)	2.0			60		75	
t _{THL}	output transition time		4.5			12		15	ns
			6.0			10		13	
			2.0			110		140	
t _{PLH}			4.5			22		28	ns
	1 .	C _L = 50pF (Note 4)	6.0		ĺ	19		24	
		$C_L = \text{SUpf (Note 4)}$	2.0			110		140	
t _{PHL}	Low-level to high-level and		4.5			22		28	ns
	high-level to low-level		6.0		· ·	19		24	
	output propagation time		2.0			195		245	
t _{PLH}	(A - B, B - A)		4.5			. 39		49	ns
			6.0			34		43	
t _{PHL}	1	C _L = 150pF (Note 4)	2.0			195		245	
			4.5			39		49	ns
			6.0			34	i	43	ļ
· · · · · ·	`		2.0			172		208	,
t _{PLZ}	Output disable time from		4.5			43		52	ns
			6.0			41		50	
	low-level and high-level	C _L = 50pF (Note 4)	2.0			172		208	
t _{PHZ}	(OE - A, B)		4.5			43	ĺ	52	ns
			6.0			41		50	
			2.0			184		224	
t _{PZL}			4.5			46	ļ	56	ns
	· ·	()	6.0			41	İ	50	
	-	$C_L = 50 pF (Note 4)$	2.0			184		224	
t _{PZH}	Output enable time to low-level		4.5			46		56	ns
			6.0			41		50	
	and high-level		2.0			216		260	
t _{PZL}	(OE - A, B)	*	4.5			54		65	ns
,		0 150 5 (4) 1 1	6.0			47		57	
	1	C _L = 150pF (Note 4)	2.0			216		260	
t _{PZH}			4.5			54		65	ns
-			6.0			47		57	1.1
Cı	Input capacitance					10		10	pF
Co	Off-state output capacitance	OE = V _{CC}				15		15	pF
C _{PD}	Power dissipation capacitance (Note 3)		1		58				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per transceiver). The power dissipation during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$



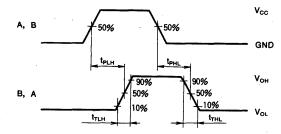
OCTAL 3-STATE NONINVERTING BUS TRANSCEIVER

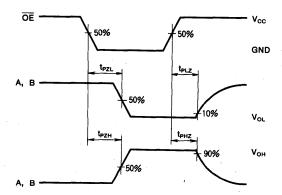
Note 4: Test Circuit



Parameter	SW 1	SW 2
t _{TLH} , t _{THL} t _{PLH} , t _{PHL}	Open	Open
t _{PLZ}	Closed	Open
t _{PHZ}	Open	Closed
t _{PZL}	Closed	Open
t _{PZH}	Open	Closed

- (1) The pulse generator (PG) has the following characteristics (10% \sim 90%): t_r = 6ns, t_f = 6ns (2) The capacitance C_L includes stray wiring
- capacitance and the probe input capacitance.







MITSUBISHI HIGH SPEED CMOS

M74HC245-1P/FP/DWP

OCTAL 3-STATE NONINVERTING BUS TRANSCEIVER

DESCRIPTION

The M74HC245-1 is a semiconductor integrated circuit consisting of eight bus transceivers with noninverted outputs.

FEATURES

- High-fanout 3-state output: (I_{OL}=24mA, I_{OH}=-24mA)
- High-speed: 8ns typ. (C₁=50pF, V_{CC}=5V)
- Low power dissipation: 25μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 60 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=-40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC245-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS245.

The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

Two buffers with 3-state noninverted outputs have their inputs and outputs mutually connected and can be used as buffers in both directions.

The input/output direction is controlled by direction input DIR.

When DIR is high, the data ports A will become input terminals and the data ports B will become output terminals. When DIR is low, B will become input terminals and A will become output terminals.

When output enable input \overline{OE} is high, A and B will both become a high-impedance state and they will be separated.

FUNCTION TABLE (Note 1)

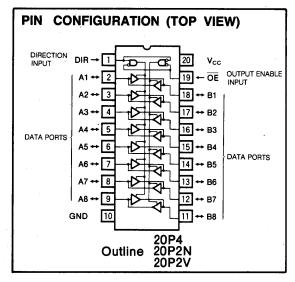
Inp	Inputs		a ports
OE	OE DIR		В
L	L	0	1
L	Н	ŀ	0
Н	X	Z	Z

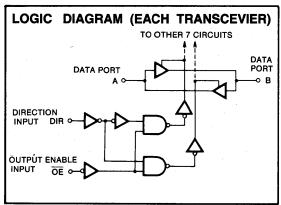
Note 1: I: Input terminal

O: Output terminal (noninverted output)

Z : High impedance (A and B are separated)

X : Irrelevant





OCTAL 3-STATE NONINVERTING BUS TRANSCEIVER

ABSOLUTE MAXIMUM RATINGS $(\tau_a = -40 \sim +85^{\circ}C)$, unless otherwise noted)

Symbol	Parameter	Conditions \	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	٧
Vı	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
	land and all all all all all all all all all al	V ₁ < 0V	-20	
lik .	Input protection diode current	V _I > V _{CC}	20	mΑ
	Cutant assessed all advances	V ₀ < 0V	-20	
ЮК	Output parasitic diode current	Vo > Vcc	20	mΑ
lo	Output current, per output pin		±50	mA
lcc	Supply/GND current	V _{CC} , GND	±200	mΑ
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		-65~+150	°C

Note 2 : M74HC245-1FP, T_a = $-40\sim+75^\circ$ C and T_a = $75\sim85^\circ$ C are derated at -7mW/°C. M74HC245-1DWP, T_a = $-40\sim+80^\circ$ C and T_a = $80\sim85^\circ$ C are derated at -7mW/°C.

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85 ^{\circ}C)$

Symbol	Parameter			Limits				
	Pa	Min	Тур	Max	Unit			
Vcc	Supply voltage		2		6	v		
Vı	Input voltage	•	0		Vcc	V		
Vo	Output voltage		0		Vcc	V		
Topr	Operating temperature ra	inge	-40		+85	င		
		$V_{CC} = 2.0V$	0		500			
t _r , t _f	tr, tf Input risetime, falltime	$V_{CC} = 4.5V$	0		50	ns/V		
		$V_{CC} = 6.0V$	0		30			

ELECTRICAL CHARACTERISTICS

		1		i.			Limits	· · · · · · · · · · · · · · · · · · ·		
Symbol	Parameter	Test	conditions			25℃		−40~	+85℃	Unit
					Min	Тур	Max	Min	Max	1 1
		V =0.1V V		2.0	1.5			1.5		
ViH	High-level input voltage	$V_0 = 0.1V, V_{CO}$ $ I_0 = 20\mu A$	5—0.1 V	4.5	3. 15			3.15		V
	-	$ 10 = 20\mu$ A		6.0	4.2			4.2	-	
		$V_0 = 0.1V, V_{CC}$					0.5		0.5	
VIL	Low-level input voltage	$ V_0 = 0.1V, V_{CO} $ $ I_0 = 20\mu A$	5—0. IV	4.5			1.35		1,35	V
		$ 10 = 20\mu\text{A}$		6.0			1.8		1.8	
	High-level output voltage $V_{l} = V_{lH}, \ V_{lL}$		$I_{OH} = -20\mu A$	2.0	1.9			1.9		
v		V - V V	$I_{OH} = -20\mu A$	4.5	4.4			4.4]	v
V _{OH}		VI - VIH, VIL	$I_{OH} = -20\mu A$	6.0	5.9			5. 9		
		,	$I_{OH} = -24mA$	4. 5	3.98			3.84		
			$I_{OL} = 20 \mu A$	2.0			0.1		0. 1	
VoL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	4. 5			0.1		0.1	v
V OL	Low-level output voltage	VI VIH, VIL	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	•
			I _{OL} = 24mA	4.5			0.39		0.5	
l _{iH}	High-level input current	$V_i = 6V$		6.0			0.1		1.0	μΑ
l _{IL} .	Low-level input current	$V_i = 0V$		6.0			-0.1		-1.0	μA
lozh	Off-state high-level output current	$V_i = V_{iH}, \ V_{iL}, \ V_{iL}$	$V_0 = V_{CC}$	6.0			0.5		5.0	μA
lozL	Off-state low-level output current	$V_{i} = V_{iH}, V_{iL}, V_{iL}$	Vo = GND	6.0			-0.5		-5.0	μA
Icc	Quiescent supply current	VI = VCC, GND	$I_0 = 0\mu A$	6.0			5.0		50.0	μΑ

OCTAL 3-STATE NONINVERTING BUS TRANSCEIVER

SWITCHING CHARACTERISTICS (V_{cc} = 5V, T_a = 25°C)

Symbol	Parameter	Test conditions		Limits			
Symbol	r dramotor	Test conditions	Min	Тур	Max	Unit	
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns	
t _{THL}	output transition time				10	ns	
t _{PLH}	Low-level to high-level and high-level to low-level				15	ns	
t _{PHL}	output propagation time (A - B, B - A)				15	ns	
t _{PLZ}	Output disable time from low-level and high-level	C = E = E (Note 4)			25	ns	
t _{PHZ}	(OE – A, B)	C _L = 5 pF (Note 4)			25	. ns	
t _{PŽL}	Output enable time to low-level and high-level	0 - 50-5 (N-4-4)			28	ns	
t _{PZH}	(OE - A, B)	C _L = 50pF (Note 4)			28	ns	

SWITCHING CHARACTERISTICS $(v_{cc} = 2\sim6v, T_a = -40\sim+85\%)$

	·					Limits			
Symbol	Parameter	Test conditions			25℃		-40~	+85℃	Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	
		·	2.0			60		75	
t _{TLH}	Low-level to high-level and		4.5			12		15	
	Land to the state of		6.0		1	10		13	
	high-level to low-level		2.0			60		75	ns
t _{THL}	output transition time		4.5			12		15	
			6.0			10		13	
			2.0			85		105	
t _{PLH}	Low-level to high-level and		4.5			17		21	
	high-level to low-level		6.0			14		18	
	output propagation time		2.0			85		105	ns
t _{PHL}	(A - B, B - A)		4.5			17		21	
		C _L = 50pF (Note 4)	6.0			14		18	
		CL — Sopr (Note 4)	2.0			150		190	
t _{PLZ}	Output disable time from		4.5	-		30		38	
	low-level and high-level		6.0			26		33	ns
	low-level and high-level		2.0			150		190	l lis
t _{PHZ}	(OE – A, B)	·	4.5			30		38	
			6.0			26		33	
			2.0			150		190	
t _{PZL}	Output enable time to		4.5			30		38	
	low-level and high-level		6.0			26		33	ns
	low-level and night-level		2. 0			150		190	113
t_{PZH}	(OE - A, B)		4.5			30		38	
			6.0			26		33	
Cı	Input capacitance					10		10	
Co	Off-state output capacitance	OE = V _{CC}				15		15	p₽
C _{PD}	Power dissipation capacitance (Note 3)								

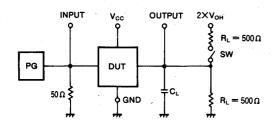
Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per transceiver)

The power dissipation during operation under no-load conditions is calculated using the following formula:

P_D = C_{PD} • V_{CC}² • f₁+I_{CC} • V_{CC}

OCTAL 3-STATE NONINVERTING BUS TRANSCEIVER

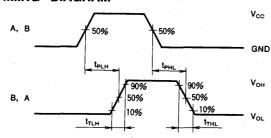
Note 4: Test Circuit

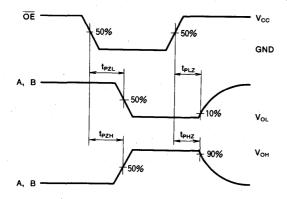


Parameter	sw
t _{TLH} , t _{THL}	Open
t _{PLZ}	Closed
t _{PHZ}	Open
t _{PZL}	Closed
t _{PZH}	Open

- (1) The pulse generator (PG) has the following characteristics (10%~90%): $t_{\rm f}=3{\rm ns},\,t_{\rm f}=3{\rm ns}$
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





OCTAL 3-STATE
NONINVERTING BUS TRANSCEIVER WITH LSTTL-COMPATIBLE INPUTS

DESCRIPTION

The M74HCT245-1 is a semiconductor integrated circuit consisting of eight transceivers with noninverted outputs.

FEATURES

- TTL level inputs V_{IL}=0.8 max, V_{IH}=2.0V min
- High-fanout 3-state output: (I_{OL}=24mA, I_{OH}=-24mA)
- High-speed: 10ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 25µW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- Capable of driving 60 74LSTTL loads
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HCT245-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS245.

The circuit is designed to suppress the increased switching noise that normally occrus at high output currents.

As the inputs are TTL level, the device can be used as a level converter from LSTTL to high-speed CMOS. In that case, no pull-up resistors are required.

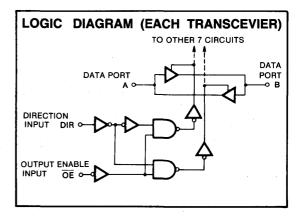
Two buffers with 3-state noninverted outputs have their inputs and outputs mutually connected and can be used as buffers in both directions.

The input/output direction is controlled by direction input DIR.

When DIR is high, the data ports A will become input terminals and the data ports B will become output terminals. When DIR is low, B will become input terminals and A will become output terminals.

When output enable input \overline{OE} is high, A and B will both become a high-impedance state and they will be separated.

PIN CONFIGURATION (TOP VIEW) DIRECTION DIR -Vcc INPUT OUTPUT ENABLE - ŌE 19 A1 -A2 ++ 18 A3 ↔ 4 16 A4 ↔ 5 **↔** B3 DATA PORTS A5 ↔ 6 15 ₩ R4 DATA PORTS A6 ↔ 7 14 **→** B5 → B6 9 **→** R7 A8 ↔ 10 GND **→** R8 20P2N Outline 20P2V



FUNCTION TABLE (Note 1)

Inp	Inputs		puts
- OE	DIR	Α	В
L	L	0	Ī
L	Н	ı	0
Н	Х	Z	Z

Note 1: I : Input terminal

O: Output terminal (noninverted output)

Z : High impedance (A and B are separated)

X : Irrelevant

OCTAL 3-STATE NONINVERTING BUS TRANSCEIVER WITH LSTTL-COMPATIBLE INPUTS

ABSOLUTE MAXIMUM RATINGS ($\tau_a = -40 \sim +85^{\circ}$ C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit	
Vcc	Supply voltage		-0.5~+7.0	V	
Vi	Input voltage		-0.5~V _{cc} +0.5	. V	
V _o	Output voltage		-0.5~V _{cc} +0.5	V	
	Input protection diode current	V ₁ < 0V	—20		
l _{IK}		$v_i > v_{cc}$	20	mA.	
,	Cutant associate diada associat	V ₀ < 0V	-20		
lok	Output parasitic diode current	V _o > V _{cc}	20	⊢ mA	
lo	Output current per output pin		±50	mA	
Icc	Supply/GND current	V _{CC} , GND	±200	mA	
Pd	Power dissipation	(Note 2)	500	mW	
Tstg	Storage temperature range		-65~+150	င	

Note 2 : M74HCT245-1FP, $T_a = -40 \sim +75 ^{\circ} C$ and $T_a = 75 \sim 85 ^{\circ} C$ are derated at -7 mW/C . M74HCT245-1DWP, $T_a = -40 \sim +80 ^{\circ} C$ and $T_a = 80 \sim 85 ^{\circ} C$ are derated at -7 mW/C .

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85 \degree c)$

Symbol	Parameter			Limits				
Symbol	Pa	ameter	Min	Тур	Max	Unit		
Vcc	Supply voltage		4.5		5.5	V		
Vt	Input voltage		0		V _{cc}	V		
Vò	Output voltage		0		Vcc	V		
Topr	Ambient operating temperating	rature	-40		+85	င		
	Innut de câles - fellal	V _{CC} = 4.5V	0		25	//		
t _r , t _f	Input risetime, falltime V _{CC} = 5.5V		0		15	ns/V		

ELECTRICAL CHARACTERISTICS (V_{cc} = 5V±10%, unless otherwise noted)

						Limits			
Symbol	Parameter	Test conditions		25℃			-40~+85°C		Unit
	* '				Тур	Max	Min	Max	
V _{IH}	High-level input voltage	$V_0 = 0.1V, V_0$ $ I_0 = 20\mu A$	$V_0 = 0.1V$, $V_{CC} = 0.1V$ $ I_0 = 20\mu A$				2.0	. •	٧
VIL	Low-level input voltage	$V_0 = 0.1V, V_0$ $ I_0 = 20\mu A$	$V_0 = 0.1 \text{V}, \ V_{CC} = 0.1 \text{V}$ $V_0 = 20 \mu \text{A}$			0.8		0.8	٧
.,		butput voltage $V_{i} = V_{iL} \qquad \frac{I_{OH} = -20\mu A}{I_{OH} = -24mA, \ V_{cC} = 4.5}$	$I_{OH} = -20\mu A$	V _{cc} -0.1			V _{cc} -0.1		v
V _{OH}	High-level output voltage $V_i = V_{iL}$		$I_{OH} = -24mA$, $V_{CC} = 4.5V$	3. 98			3. 84		
V	I am land anti-time	V - V V	$I_{OL} = 20\mu A$			0.1		0.1	v
V _{OL}	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 24 \text{mA}, \ V_{CC} = 4.5 \text{V}$			0.39		0.5	Y
l _{IH}	High-level input current	$V_i = V_{CC}$				0.1		1.0	
I _{IL}	Low-level input current	V ₁ = GND		1		-0.1		-1.0	μA
lozh	Off-state high-level output current	$V_i = V_{iH}, \ V_{iL},$	$V_0 = V_{CC}$	1		0.5		5.0	
lozL	Off-state low-level output current	$V_i = V_{iH}, V_{iL}, V_O = GND$				-0.5		-5.0	μΑ
Icc	Quiescent supply current	VI = VCC, GNE	$D, I_0 = 0\mu A$		*****	5.0		50.0	μA
Δlcc	Maximum quiescent supply current	$V_1 = 2.4V, 0.4$	V (Note 3)			2.7		2.9	- mA

Note 3: Only one input is set at this value and all other inputs are fixed at V_{CC} or GND.

MITSUBISHI HIGH SPEED CMOS M74HCT245-1P/FP/DWP

OCTAL 3-STATE NONINVERTING BUS TRANSCEIVER WITH LSTTL-COMPATIBLE INPUTS

SWITCHING CHARACTERISTICS ($v_{cc} = 5v$, $t_a = 25\%$)

Symbol	Parameter	Test conditions	Limits			Unit
Symbol	Parameter	rest conditions	Min	Тур	Max	O III
t _{TLH}	Low-level to high-level and high-level to low-level	- C _L = 50pF (Note 5)			10	ns
t _{THL}	output transition time				10	ns
t _{PLH}	Low-level to high-level and high-level to low-level				15	ns
t _{PHL}	output propagation time (A - B, B - A)				15	ns
t _{PLZ}	Output disable time from low-level and high-level	$C_1 = 5 pF (Note 5)$			25	ns
t _{PHZ}	(OE - A, B)	$C_L = 5 \text{ pr (Note 5)}$			25	ns
t _{PZL}	Output enable time to low-level and high-level	C _L = 50pF (Note 5)			28	ns
t _{PZH}	(OE - A, B)	OL — SOPE (NOTE S)			28	ns

SWITCHING CHARACTERISTICS ($v_{cc} = 5v \pm 10\%$, $T_a = -40 \sim +85\%$)

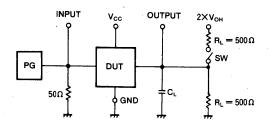
					Unit			
Symbol	Parameter	Test conditions	25℃			-40~+85℃		
	·		Min	Тур	Max	Min	Max	
t⊤∟H	Low-level to high-level and high-level to low-level				12		15	
t _{THL}	output transition time	,			12		15	ns
t _{PLH}	Low-level to high-level and high-level to low-level				17	-	21	ns
t _{PHL}	output propagation time (A — B, B — A)	C = 50sE (Note 5)			17		21	115
t _{PLZ}	Output disable time from	C _L = 50pF (Note 5)			30		38	
t _{PHZ}	low-level and high-level (OE - A, B) Output enable time to				30		38	ns
t _{PZL}					30		38	ns
t _{PZH}	low-level and high-level				30		38	
C	Input capacitance				10		10	
Co	Off-state output capacitance	OE = V _{CC}			15		15	pF
CPD	Power dissipation capacitance (Note 4)							

Note 4: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per transceiver) The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$



OCTAL 3-STATE NONINVERTING BUS TRANSCEIVER WITH LSTTL-COMPATIBLE INPUTS

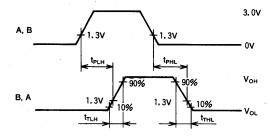
Note 5: Test Circuit

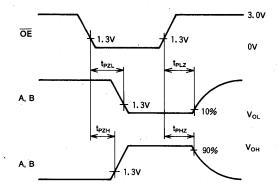


Parameter	sw	
t _{TLH} , t _{THL} t _{PLH} , t _{PHL}	Open	
t _{PLZ}	Closed	
t _{PHZ}	Open	
t _{PZL}	Closed	
t _{PZH}	Open	

- (1) The pulse generator (PG) has the following characteristics (10%~90%): $t_f=3 n s, \, t_f=3 n s$
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





M74HC251P/FP/DP

8-INPUT DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

DESCRIPTION

The M74HC251 is a semiconductor integrated circuit consisting of an 8-line to 1-line data selector/multiplexer with 3-state outputs.

FEATURES

- High-speed: 20ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide supply voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

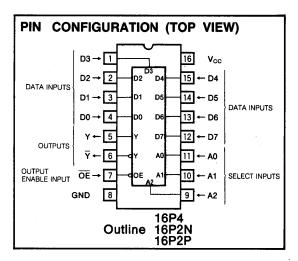
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC251 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS251.

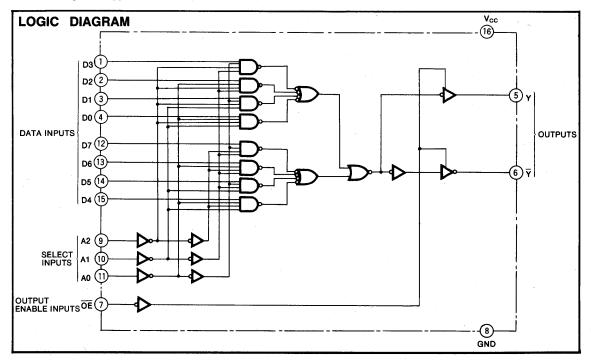
The M74HC251 consists of data selector functions for selecting one of eight input line signals and multiplexer functions for converting 8-bit parallel data into serial data using time-division.

The 8-line signal is applied to data inputs D0 through D7,



and after one of the data inputs has been selected by select inputs A0 through A2, that input signal will be output at Y or an inverted signal will be output at Y. By applying 8-bit parallel data to D0 through D7, and connecting the output of a synchronous octal counter to A0 through A2, D0 through D7 data will be output at Y synchronous with the clock pulse in the order of D0-D7. When output-enable input \overline{OE} is high, all outputs will become a high-impedance state irrespective of other inputs.

M74HC251 has the same functions and pin connections as the M74HC151, but the former has a 3-state output.





FUNCTION TABLE (Note 1)

					Inp	outs						Ou	tput
A2	A1	A0	ŌĒ	D0	D1	. D2	D3	D4	D5	D6	D7	Υ	Ÿ
Х	Х	X	Н	Х	Х	X	Х	Х	Х	Х	X	Z	Z
L	Ĺ	L	L	L	Х	х	Х	х	Х	×	X	L	Н
L	L	L	L	Н	Х	X	Х	Х	Х	х	X	Н	L
L	L	Н	L	х	L	Х	Х	Х	Х	X	Х	L ·	Н
L	L	Н	L	Х	Н	х	Х	Х	Х	х	×	Н	L
L	Н	L	L	Х	х	L	х	х	Х	х	х	L	н
L	н	L	L	X	Х	н	X	Х	Х	×	X	Н	L
L	Н	Н	L	Х	Х	X	L	Х	Х	Х	X	L .	Н
L	Н	Н	L	Х	х	X	Н	Х	X	X	X	Н	L
Н	L	L	L	Х	Χ,	Х	X	L	Х	Х	X	L	Н
Н	L	L	L	Х	х	Х	X	Н	Х	х	X	Н	L
н	L	н	L	Х	Х	х	Х	Х	L	X	X	L	Н
Н	L	Н	L	х	х	х	х	Х	н	х	Х	Н	L
Н	Н	L	L	х	X	х	×	х	Х	L	X	L	Н
Н	Н	L	L	х	X	х	х	х	Х	Н	X .	Н	L
н	Н	н	L	Х	Х	х	х	х	Х	х	L	L	Н
Н	Н	Н	L	Х	Х	X	х	х	Х	X	Н	Н	L

Note 1 : X : Irrelevant

Z : High impedance

ABSOLUTE MAXIMUM RATINGS ($\tau_a = -40 \sim +85 \degree$ C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V _{cc}	Supply voltage		-0.5~+7.0	V
V ₁	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
		V ₁ < 0V	-20	
l _{IK}	input protection diode current	V _I > V _{CC}	20	mA
		V ₀ < 0V	-20	
lok	Output parasitic diode current	V _o > V _{cc}	20	mA.
lo	Output current per output pin		±25	mA
Icc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		-65∼+150	°C

Note 2 : M74HC251FP, $T_a = -40 \sim +70^\circ C$ and $T_a = 70 \sim 85^\circ C$ are derated at -6mW/°C. M74HC251DP, $T_a = -40 \sim +50^\circ C$ and $T_a = 50 \sim 85^\circ C$ are derated at -5mW/°C.

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85 ^{\circ}\text{C})$

0			Limits					
Symbol	Pa	rameter	Min	Тур	Max	Unit		
Vcc	Supply voltage		2		.6	٧		
V _I	Input voltage		0		Vcc	٧		
Vo	Output voltage	Output voltage				٧		
Topr	Operating temperature ra	ange	-40		+85	c		
		$V_{CC} = 2.0V$	0		1000			
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns		
		$V_{CC} = 6.0V$			400			

ELECTRICAL CHARACTERISTICS

					Limits					Unit
Symbol	Parameter	Test conditions V _{CC} (V)		25℃			-40~+85°C			
				Min	Тур	Max	Min	Max		
		$V_{\rm O} = 0.1 V, \ V_{\rm CO}$	- 0.114	2.0	1.5			1.5		
VIH	High-level input voltage	$ V_0 = 0.1V, V_{CO} $ $ I_0 = 20\mu A$	5—0.1 V	4.5	3. 15	·		3.15		V
		11 ₀ 1 = 20μΑ	_	6.0	4.2	Į		4.2)
		V = 0.1V V	0.1V, V _{CC} -0.1V				0.5		0.5	
VIL	Low-level input voltage	$ V_0 = 0.1V, V_{CO} $ $ I_0 = 20\mu A$	5U. T V	4.5			1.35		1.35	V
		11 ₀ = 20μΑ		6.0			1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
	·		$I_{OH} = -20\mu A$	4.5	4. 4			4. 4		[
V _{OH}	High-level output voltage	$V_i = V_{iH}, \ V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		V
			$I_{OH} = -4.0 \text{mA}$	4.5	4.18			4.13		1
			$I_{OH} = -5.2 \text{mA}$	6.0	5.68			5. 63		
			$I_{OL} = 20 \mu A$	2.0			0. 1		0.1	
			$I_{OL} = 20 \mu A$	4.5			0.1		0.1	
VoL	Low-level output voltage	$V_I = V_{IH}, V_{IL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
			I _{OL} = 4.0mA	4.5			0. 26		0.33	
			$I_{OL} = 5.2 mA$	6.0			0.26		0.33	
I _{IH}	High-level input current	$V_i = 6V$		6.0			0. 1	1	1.0	μA
IIL	Low-level input current	$V_1 = 0V$		6.0			-0.1		-1.0	μA
I _{OZH}	Off-state high-level output current	$V_{I} = V_{IH}, \ V_{IL}, \ V_{IL}$	$V_{\rm O} = V_{\rm CC}$	6.0			0.5		5.0	μA
lozL	Off-state low-level output current	$V_i = V_{iH}, \ V_{iL}, \ V_{iL}$	V _O = GND	6.0			-0.5		-5.0	μА
Icc	Quiescent supply current	VI = VCC, GND	$I_0 = 0 \mu A$	6.0			4.0		40.0	μΑ

SWITCHING CHARACTERISTICS $(v_{cc} = 5v, T_a = 25^{\circ}C)$

0	B			Limits		14-11
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time				10	ns
t _{PLH}	Low-level to high-level and high-level to low-level				29	ns
t _{PHL}	output propagation time (D — Y)	- 15.5(0.4)			29	ns
t _{PLH}	Low-level to high-level and high-level to low-level				32	ns
t _{PHL}	output propagation time $(D - \overline{Y})$	C _L = 15pF (Note 4)			32	ns
t _{PLH}	Low-level to high-level and high-level to low-level				35	ns
t _{PHL}	output propagation time (A — Y)				35	ns
t _{PLH}	Low-level to high-level and high-level to low-level				35	ns
t _{PHL}	output propagation time $(A - \overline{Y})$				35	ns
t _{PLZ}	Output disable time from low-level and high-level	C ₁ = 5 pF (Note 4)			35	ns
t _{PHZ}	(OE - Y)	$C_L = 5 \text{ pr (Note 4)}$,	35	ns
t _{PZL}	Output enable time to low-level and high-level	0 - 15-5 (N-t- 4)			26	ns
t _{PZH}	(OE – Y)	C _L = 15pF (Note 4)			26	ns
t _{PLZ}	Output disable time from low-level and high-level	C ₁ = 5 pF (Note 4)			40	ns
t _{PHZ}	$(\overline{OE} - \overline{Y})$	OL — 5 pr (Note 4)			40	ns
t _{PZL}	Output enable time to low-level and high-level	C _L = 15pF (Note 4)			27	ns
t _{PZH}	$(\overline{OE} - \overline{Y})$	CL — TSPF (Note 4)			27	ns

SWITCHING CHARACTERISTICS $(V_{cc} = 2\sim6V, T_a = -40\sim+85\%)$

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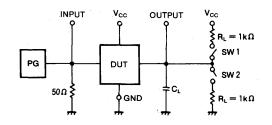
						Limits			ļ
Symbol	Parameter	Test conditions			25℃			+85℃	Uni
	•		V _{cc} (V)	Min	Тур	Max	Min.	Max	
	-		2.0			75		95	
t _{TLH}	Low-level to high-level and		4.5			15 .		19	ns
	high lovel to love lovel		6.0			13		16	
	high-level to low-level		2.0			75		95	
t _{THL}	output transition time	· ·	4.5			15		19	ns
		,	6.0		ĺ	13		16	
			2.0			195		244	
t _{PLH}	Low-level to high-level and		4.5			39		49	n
	high-level to low-level		6.0			33		41	i
	output propagation time	*	2.0			195		244	
t _{PHL}	(D - Y)		4, 5			39		49	n:
PHL	(8 1)		6.0			33		41	
		-	2.0		 	185		231	\vdash
	Law level to high level and		4.5			37		46	n:
t _{PLH}	Low-level to high-level and		6.0			37		40	"
	high-level to low-level								-
	output propagation time		2.0			185		231	١.
t _{PHL}	$(D-\overline{Y})$		4.5			37		46	n
			6.0			32		40	_
		,	2.0			205		256	
t _{PLH}	Low-level to high-level and		4.5			41	-	51	n
	high-level to low-level		6.0			35		44	
	output propagation time		2.0			205		256	
t _{PHL}	(A — Y)		4.5			41		51	n
		C - 50-5 (N-4-4)	6.0		1	35	1	44	
		C _L = 50pF (Note 4)	2, 0			205		256	
t _{PLH}	Low-level to high-level and		4.5			41		51	n
	high-level to low-level		6.0		1	35]	44	
	output propagation time		2.0			205		256	
t _{PHL}	$(A - \overline{Y})$		4.5			41	ļ	51	l n
			6.0			35		44	
-			2. 0			195		244	
t _{PLZ}	Output disable time from		4.5			39	}	49	n
	,		6.0			33		41	"
	low-level and high-level		2.0			195		244	-
	(OE - Y)		4.5			39		49	n
t _{PHZ}	(02 - 1)		6.0			33		41	"
	<u> </u>	-	2, 0			145		181	
	0.4-4		1				1		
t _{PZL}	Output enable time to		4.5			29	l	36	n
	low-level and high-level	*	6.0		ļ	25		31	<u> </u>
	1	-	2.0].		145		181	ĺ
t _{PZH}	(OE – Y)		4.5			29		36	n
			6.0			25	ļ	31	
			2.0		1	220		275	
t _{PLZ}	Output disable time from		4.5			44		55	n
	low-level and high-level		6. Ò			37		46	_
	low-level and mign-level		2.0			220		275	
t _{PHZ}	$(\overline{OE} - \overline{Y})$	*	4.5			44		55	n
			6.0	l	1	37	l	46	(

SWITCHING CHARACTERISTICS $(v_{cc} = 2\sim6v, T_a = -40\sim+85\%)$ (continued)

				Limits					
Symbol	Parameter	Test conditions			25℃		-40~+85°C		Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	1
t _{PZL} Output enable time to			2.0			150		188	
	Output enable time to		4.5			30		38	ns
		50 7/11 1	6.0			26		33	
	low-level and high-level	C _L = 50pF(Note 4)	2.0			150		188	ns
t _{PZH}	$(\overline{OE} - \overline{Y})$		4.5			30	1	38	
			6.0			26		33	
Cı	Input capacitance					10		10	pF
Со	Off-state output capacitance	OE = V _{CC}				15		15	pF
C _{PD}	Power dissipation capacitance (Note 3)				67				pF

Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$

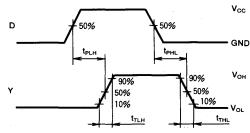
Note 4: Test Circuit

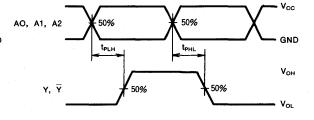


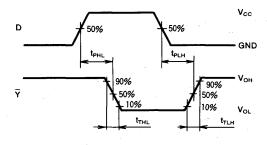
Parameter	SW 1	SW 2
t _{TLH} , t _{THL}	Open	Open
t _{PLZ}	Closed	Open
t _{PHZ}	Open	Closed
t _{PZL}	Closed	Open
t _{PZH}	Open	Closed

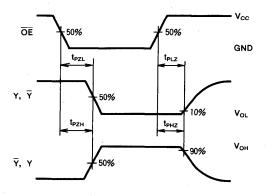
- (1) The pulse generator (PG) has the following characteristics (10% \sim 90%): t_f = 6ns, t_f = 6ns
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM









M74HC253P/FP/DP

DUAL 4-INPUT DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

DESCRIPTION

The M74HC253 is a semiconductor integrated circuit consisting of two 4-line to 1-line data selectors/multiplexrs with 3-state outputs.

等於特別的2000年代,但在2000年期,自由的

医周围变色导致自动

FEATURES

- High-speed: 18ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max
 (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide supply voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

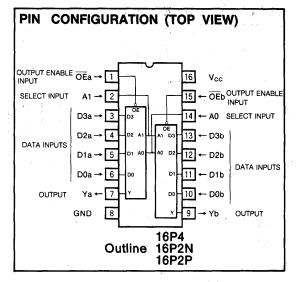
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

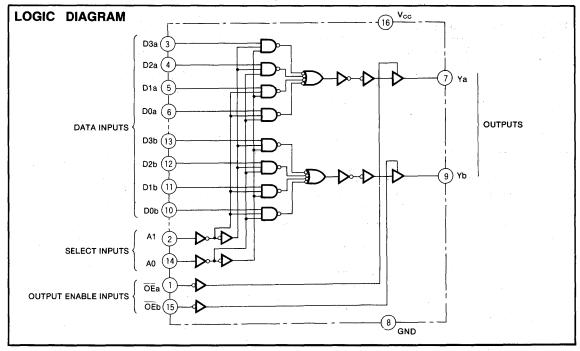
Use of silicon gate technology allows the M74HC253P to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS253.

The M74HC253 consists of data selector functions for selecting one of four input line signals and multiplex functions for converting 4-bit parallel data into serial data using time-division.

The 4-line signal is applied to data inputs D0 through D7, and after one of the data inputs has been selected by



select inputs A0 and A1, that input signal will be output at Y. By applying 4-bit parallel data to D0 through D3, and connecting the output of a synchronous quadruple counter to A0 and A1, D0 through D3 data will be output at Y synchronous with the clock pulse in the order of D0-D3. Slelct inputs A are common to the two circuits while the output-enable inputs $\overline{\text{OE}}$ are independent. When $\overline{\text{OE}}$ is high, Y will become a high-impedance state irrespective of other inputs.





FUNCTION TABLE (Note 1)

			Inputs				Output
A1	AO	D0	D1	D2	D3	ŌE	Y
×	×	х	X	×	×	Н	Z
L	L	L	х	×	×	L	L
L	L	Н	х	х	Х	L	Н
L	н	х	L	х	X	L	L
L	Н	х	Н	х	X	L	Н
Н	L	х	X	L	X	L	L
Н	L	х	х	Н	×	L	Н
Н	н	х	х	х	L	L	L
Н	Н	X	Х	×	Н	L	Н

Note 1 : X : Irrelevant

Z : High impedance

ABSOLUTE MAXIMUM RATINGS $(\tau_a = -40 \sim +85 \%)$

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
V,	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
	land and a diada and	V ₁ < 0V	-20	
l _{IK}	Input protection diode current	V _i > V _{cc}	20	mA
		V ₀ < 0V	-20	
lok	Output parasitic diode current	V _o > V _{cc}	20	⊢ mA
lo	Output current per output pin		±25	mA
loc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65~+150	င

Note 2 : M74HC253FP, T_a = $-40\sim+70^\circ$ C and T_a = $70\sim85^\circ$ C are derated at -6mW/°C. M74HC253DP, T_a = $-40\sim+50^\circ$ C and T_a = $50\sim85^\circ$ C are derated at -5mW/°C.

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85 \circ)$

O	Parameter			Limits				
Symbol			Min	Тур	Max	Unit		
V _{CC}	Supply voltage		2		6	٧		
V _I	Input voltage		0		Vcc			
Vo	Output voltage		. 0		Vcc	٧		
Topr	Operating temperature re	inge	-40		+85	င		
		V _{CC} = 2.0V	0		1000			
t _r , t _f	Input risetime, falltime	V _{CC} = 4.5V	0		500	ns		
	$V_{CC} = 6.0V$		0		400			

M74HC253P/FP/DP

DUAL 4-INPUT DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

ELECTRICAL CHARACTERISTICS

							Limits			<u>.</u>
Symbol	Parameter	Test	conditions			25℃		-40~+85°C		Unit
			V _{cc} (V)		Min	Тур	Max	Min	Max	İ
		V = 0.1V V	0.11/	2.0	1.5			1.5		
V _{IH}	High-level input voltage	$ V_0 = 0.1V, V_{CO} $ $ I_0 = 20\mu A$		4.5	3.15			3.15	(v
		1101 = 20µA		6.0	4.2			4.2		
	$V_0 = 0.1V, V_{CC} = 0.1V$		0.114	2.0			0.5		0.5	
VIL	Low-level input voltage	$ V_0 = 0.1V, V_{CO}$ $ I_0 = 20\mu A$. 1				1.35		1.35	v
		1101 - 20µA		6.0			1.8		1.8	
V _{OH} High-level output voltage		$I_{OH} = -20\mu A$	2.0	1.9			1.9			
		$I_{OH} = -20\mu A$	4.5	4.4			4. 4			
	$V_I = V_{IH}, \ V_{IL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		١ ،	
		$l_{OH} = -4.0 \text{mA}$	4.5	4.18			4.13			
			I _{OH} = -5. 2mA	6.0	5. 68			5.63	ļ ,	ļ
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
			$I_{OL} = 20 \mu A$	4.5			0.1		0, 1	1.
Vol	Low-level output voltage	$V_1 = V_{1H}, V_{1L}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	· · v
1.			I _{OL} = 4.0mA	4.5			0.26		0.33	
			$I_{OL} = 5.2 mA$	6.0			0.26		0.33	
l _{IH}	High-level input current	$V_i = 6V$		6.0			0.1		1.0	μ
կլ	Low-level input current	V ₁ = 0V		6.0			-0.1		-1.0	μ
l _{ozh}	Off-state high-level output current	$V_i = V_{iH}, \ V_{iL}, \ V_{iL}$	vo = Vcc	6.0			0.5		5.0	μ
lozL	Off-state low-level output current	$V_i = V_{iH}, \ V_{iL}, \ V_{iL}$	o = GND	6.0			-0.5		-5.0	μ
lcc	Quiescent supply current	VI = VCC, GND	$I_0 = 0 \mu A$	6.0			4.0		40.0	μ

SWITCHING CHARACTERISTICS ($V_{cc} = 5V$, $T_a = 25^{\circ}C$)

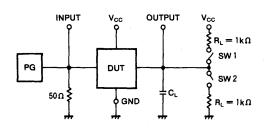
0		Test conditions			Unit	
Symbol	Parameter	Jest conditions	Min	Тур	Max	Onic
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time				10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C ₁ = 15pF (Note 4)			23	ns
t _{PHL}	output propagation time (D - Y)	CL — ISPF (Note 4)		'	23	ns
t _{PLH}	Low-level to high-level and high-level to low-level				30	ns
t _{PHL}	output propagation time (A — Y)	1 - 474			30	กร
t _{PLZ}	Output disable time from low-level and high-level	C = 5 = 5 (Note 4)			27	ns
t _{PHZ}	(OE – Y)	C _L = 5 pF (Note 4)			27	ns
tezL	Output enable time to low-level and high-level	C _L = 15pF (Note 4)			18	ns
t _{PZH}	(OE - Y)	OL — Topr (Note 4)			18	ns

SWITCHING CHARACTERISTICS ($V_{cc} = 2\sim6V$, $T_a = -40\sim+85^{\circ}C$)

O b 1		7		ļ	25°C	Limits	-40~	1.05%	
Symbol	Parameter	Test conditions	F., 63			r		r	Unit
		ļ	V _{cc} (V)	Min	Тур	Max	Min	Max	<u> </u>
			2.0			75		95	
t _{TLH}	Low-level to high-level and		4.5			15		19	ns
	high-level to low-level		6.0			13		16	ļ
	output transition time		2.0		ł	75		95	
t _{THL}	output transition time		4. 5			15		19	ns
		_	6.0	ļ		13		16	
			2.0			126		158	
t _{PLH}	Low-level to high-level and		4.5	1		28		35	ns
	high-level to low-level		6.0			23		29	
	output propagation time		2.0			126		158	ĺ
t _{PHL} .	(D-Y)		4.5			28		35	ns
			6.0			23		29	
	1		2.0			158		198	
t _{PLH}	Low-level to high-level and		4.5			35		44	ns
	high-level to low-level	C _L = 50pF (Note 4)	6.0	<u> </u>		30		38	
	output propagation time	OL - Sopi (Note 4)	2.0			158		198	
t _{PHL}	(A - Y)		4.5		ł	35		44	ns
			6.0			30		38	
	1		2.0	l	1	135		169	
t_{PLZ}	Output disable time from		4.5			30		38	ns
	law lawel and high lawel		6.0			25		31	
	low-level and high-level		2.0			135		169	
t _{PHZ}	(OE - Y)		4.5			30		38	ns
	1.		6.0			25		31	
			2.0			90		113	
t _{PZL}	Output enable time to		4.5	1		20		25	ns
	law laws and black laws		6.0			17		21	
	low-level and high-level		2.0			90		113	
t _{PZH}	(OE - Y)		4.5	_		20		25	ns
	-		6.0			17		21	
Cı	input capacitance				·	10		10	pF
Co	Off-state output capacitance	OE = V _{CC}				15		15	pF
C _{PD}	Power dissipation capacitance (Note 3)				61				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula: $P_{D} = C_{PD} \cdot V_{CC}^2 \cdot f_{|} + I_{CC} \cdot V_{CC}$

Note 4: Test Circuit

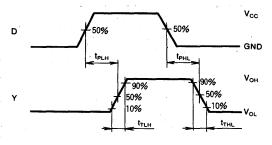


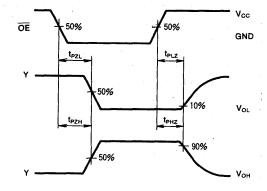
Parameter	SW 1	SW 2
t _{TLH} , t _{THL} t _{PLH} , t _{PHL}	Open	Open
t _{PLZ}	Closed	Open
t _{PHZ}	Open	Closed
tpzL	Closed	Open
t _{PZH}	Open	Closed

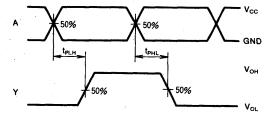
- (1) The pulse generator (PG) has the following characteristics (10% \sim 90%): $t_f=6ns,\,t_f=6ns$
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM

SAME CARREST SECTION PROPERTY







M74HC257P/FP/DP

QUADRUPLE 2-INPUT DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

DESCRIPTION

The M74HC257 is a semiconductor integrated circuit consisting of four 2-line to 1-line data selectors/multiplexers with 3-state outputs.

FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 12ns typ. ($C_L=50pF$, $V_{CC}=5V$)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2∼6V
- Wide operating temperature range: T_a=−40~+85°C

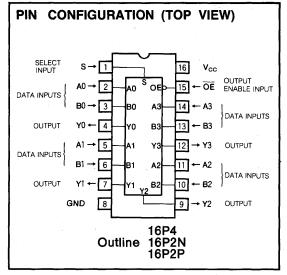
APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

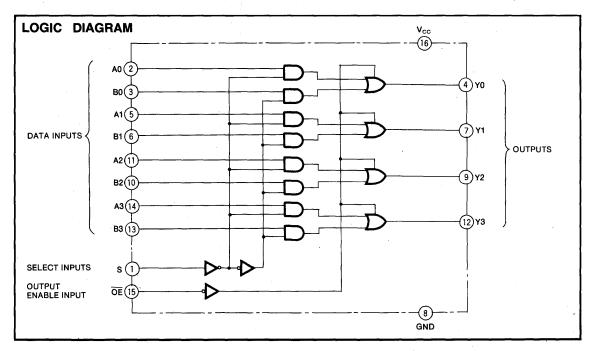
Use of silicon gate technology allows the M74HC257 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS257.

The M74HC257 consists of four circuits each containing date selector functions for selecting one of two input line signals and multiplexer functions for converting 2-bit parallel data into serial data using time-division.



The 2-line signal is applied to data inputs A and B, and after one of the data inputs has been selected by select input S, it is output at pin Y. By applying 2-bit parallel data to A and B, and connecting the output of a binary counter to S, A and B date will be output at Y synchronous with the clock pulse in the order A-B. Both S and output-enable input $\overline{\text{OE}}$ are common to all four circuits.

When $\overline{\text{OE}}$ is high, all outputs Y will become high impedance state irrespective of other inputs.



FUNCTION TABLE (Note 1)

	Inputs					
OE	S	Α	В	Y		
Н	×	X	Х	Z		
L	L	L	X	L		
L.	L	н	Х	Н		
L	Н	X	L	L		
L	н	Х	Н	Н		

Note 1: X: Irrelevant

Z : High impedance

ABSOLUTE MAXIMUM RATINGS $(T_a = -40 \sim +85\%, \text{ unless otherwise noted})$

Symbol	Parameter	Conditions	Ratings	Unit	
Vcc	Supply voltage		-0.5~+7.0	V	
V,	Input voltage		-0.5~V _{cc} +0.5	V	
Vo	Output voltage		-0.5~V _{cc} +0.5	V	
	land and all dansers	V ₁ < 0V	-20		
lıк	Input protection diode current	$V_i > V_{CC}$	20	mA	
	Outside and the disease and	V ₀ < 0V	-20		
lok	Output parasitic diode current	Vo > Vcc	20	mA	
l _o	Output current per output pin		±35	mA	
lcc	Supply/GND current	V _{CC} , GND	±75	mA	
Pd	Power dissipation	(Note 2)	500	mW	
Tstg	Storage temperature range		-65~+150	°C	

Note 2 : M74HC257FP, $T_a = -40 \sim +70 ^\circ C$ and $T_a = 70 \sim 85 ^\circ C$ are derated at $-6 mW/^\circ C$. M74HC257DP, $T_a = -40 \sim +50 ^\circ C$ and $T_a = 50 \sim 85 ^\circ C$ are derated at $-5 mW/^\circ C$.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85 ^{\circ}C)$

Outside al	0-	Parameter		Limits				
Symbol	Pa			Тур	Max	Unit		
Vcc	Supply voltage		2		.6	V		
Vi	Input voltage		0		Vcc	٧		
Vo	Output voltage	Output voltage			Vcc	V		
Topr	Operating temperature ra	ange	40		+85	Ç		
		$V_{CC} = 2.0V$	0		1000			
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns		
		$V_{CC} = 6.0V$	0		400			

M74HC257P/FP/DP

QUADRUPLE 2-INPUT DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

ELECTRICAL CHARACTERISTICS

							Limits			
Symbol	Parameter	Test	conditions			25℃		-40~	+85°C	Unit
				V _{cc} (V)	Min	Тур	Max	Min	Max]
		$V_0 = 0.1V, V_{CC} = 0.1V$		2.0	1.5			1.5		
V _{IH}	High-level input voltage			4.5	3.15	1	ĺ	3.15	1	_ v
		$ I_0 = 20\mu A$ 6.0		6.0	4.2		İ	4.2		
	$V_{\rm O} = 0.1 V, V_{\rm CC} = 0.1 V$		-0.17	2.0			0.5		0.5	
VIL	Low-level input voltage						1.35		1.35	V
		$ I_{O} = 20\mu A$		6.0		l	1.8		1.8	ļ
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
			$I_{OH} = -20\mu A$	4.5	4.4	ł	ļ	4.4]	
V _{OH} High-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		v	
			$I_{OH} = -6.0 \text{mA}$	4.5	4.18			4.13		
			$I_{OH} = -7.8 mA$	6.0	5. 68	1		5. 63		
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
			$I_{OL} = 20 \mu A$	4.5		İ	0.1		0.1	
VoL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0	-		0.1	Ì	0, 1	V
			I _{OL} = 6.0mA	4.5			0.26		0.33	1
			$I_{OL} = 7.8 mA$	6.0			0.26		0.33	
l _{iH}	High-level input current	$V_i = 6V$		6.0			0.1		1,0	μΑ
I _{IL}	Low-level input current	$V_i = 0V$		6.0			-0.1		-1.0	μA
l _{ozh}	Off-state high-level output current	$V_{I} = V_{IH}, \ V_{IL}, \ V_{IL}$	$v_0 = v_{CC}$	6.0			0.5		5.0	μA
lozL	Off-state low-level output current	$V_i = V_{iH}, \ V_{iL}, \ V_O = GND$		6.0			-0.5		-5.0	μA
Icc	Quiescent supply current	VI = VCC, GND	$I_0 = 0\mu A$	6.0			4.0		40.0	μА

SWITCHING CHARACTERISTICS $(V_{cc} = 5V, T_a = 25^{\circ}C)$

0	B	TA			Unit	
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time				10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	O = F0=F (N=+= 4)			18	ns
t _{PHL}	output propagation time (A, B-Y)	$C_L = 50 pF (Note 4)$			18	ns
t _{PLH}	Low-level to high-level and high-level to low-level				29	ns
t _{PHL}	output propagation time (S-Y)	·			29	ns
t _{PLZ}	Output disable time from low-level and high-level	C ₁ = 5 pF (Note 4)			23	ns
t _{PHZ}	(OE-Y)	C _L = 5 pF (Note 4)			23	nş
t _{PZL}	Output enable time to low-level and high-level	C = 50-5 (Note 4)			20	ns
t _{PZH}	(OE-Y)	C _L = 50pF (Note 4)			20	ns

SWITCHING CHARACTERISTICS ($V_{cc} = 2\sim 6V$, $T_a = -40\sim +85\%$)

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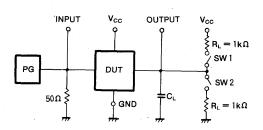
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Symbol	Dava-rates.	Took conditions			25℃	Limits	AD -	+85°C	
Symbol	Parameter	Test conditions	[W (W)	A 41-		14-11			Uni
			V _{cc} (V)	Min	Тур	Max	Min	Max	
,	1		2.0			60		75	
TLH	Low-level to high-level and	•	4.5		l	12	ı	15	ns
	high-level to low-level	C _L = 50pF (Note 4)	6.0			10		13	ļ
			2.0		ļ.	60		75	
THL	output transition time	·	4.5			12		15	n
	 		6.0		-	10		13	
			2.0			100		126	
t _{PLH}			4.5			20		25	n
	_	$C_L = 50 pF (Note 4)$	6.0			17		21	
			2.0			100		126	
t _{PHL}	Low-level to high-level and		4.5			20		25	ns
	high-level to low-level	<u> </u>	6.0			17		21	
	output propagation time		2.0			150		189	
PLH	(A, B-Y)		4.5			30		38	ns
	4	$C_L = 150 pF (Note 4)$	6.0		ļ	26		32	
	PHL		2.0			150		189	İ
t _{PHL}			4.5			30		38	n
			6.0			26		32	
			2.0		j	160		200	
t _{PLH}			4. 5		1 '	32		40	n
		$C_L = 50pF (Note 4)$	6.0			27		34	L
			2. 0		l .	160		200	١.
t _{PHL}			4.5		1	32		40	n:
	high-level to low-level		6.0			27		34	
	output propagation time		2.0			210		265	ĺ
t _{PLH}	(S-Y)		4.5		į.	42		53	n:
	<u> </u>	C _L = 150pF (Note 4)	6.0			36		45	
		OL = 150pi (Note 4)	2.0			210		265	1
t _{PHL}			4.5			42		53	ņ
	·		6.0			36		45	
			2.0			140		175	
t _{PLZ}	Output disable time from		4.5	ļ		.28	4.5 L	35	n
	lew level and bish level	C = 50=5 (NG+= 4)	6.0			24		30	
	low-level and high-level	C _L = 50pF (Note 4)	2.0			140		175	
t _{PHZ}	(OE-Y)	-	4.5			28	·	35	n
			6.0)		24		30	
			2.0			110		140	Ī .
t _{PZL}			4.5			22		28	n
		50.5(0).00	6.0			19	ļ	24	1
	1	$C_L = 50 pF \text{ (Note 4)}$	2.0			110		140	
t _{PZH}	Output enable time to		4.5			22		28	n
			6.0			19		24	
	low-level and high-level		2.0			160		200	
PZL			4.5		1	32		40	l n
			6.0	.		27		34	1
		C _L = 150pF (Note 4)	2.0	<u> </u>		160		200	t
t _{PZH}			4.5			32		40	n
ZIT	PZH		6.0		1	27		34	"
Cı	Input capacitance		- 5 	 	 	10		10	р
C _o	Off-state output capacitace	$\overline{OE} = V_{CC}$			 	15		15	pl
C _{PD}	Power dissipation capacitance (Note					+			p

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipation during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$



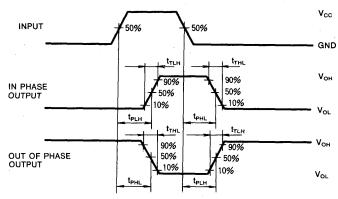
Note 4: Test Circuit

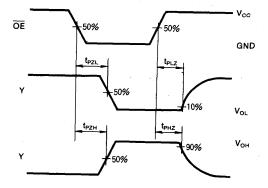


Parameter	SW 1	SW 2
t _{TLH} , t _{THL} t _{PLH} , t _{PHL}	Open	Open
t _{PLZ}	Closed	Open
t _{PHZ}	Open	Closed
t _{PZL}	Closed	Open
t _{PZH}	Open	Closed

- (1) The pulse generator (PG) has the following
- characteristics (10%~90%): t_r = 6ns, t_f = 6ns (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





MITSUBISHI HIGH SPEED CMOS

M74HC258P/FP/DP

QUADRUPLE 2-INPUT DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

DESCRIPTION

The M74HC258 is a semiconductor integrated circuit consisting of four 2-line to 1-line data selectors/multiplexers with 3-state outputs.

FEATURES

- High-fanout 3-state output (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 12ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{cc}=2~6V
- Wide operating temperature range: T_a=-40~+85℃

APPLICATION

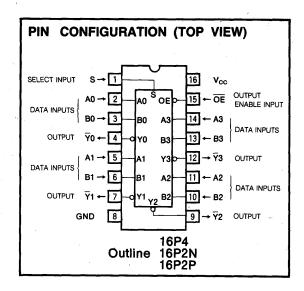
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC258P to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS258.

The M74HC258 consists of four circuits each containing data selector functions for selecting one of two input line signals and multiplexer functions for converting 2-bit parallel data into serial data using time-division.

The 2-line signals are applied to data inputs A and B, and after one of the data inputs has been selected by select input S, it is output at pin \overline{Y} . By applying 2-bit parallel data to A and B, and connecting the output of a binary counter to S, the data at A and B will be inverted and sequentially output



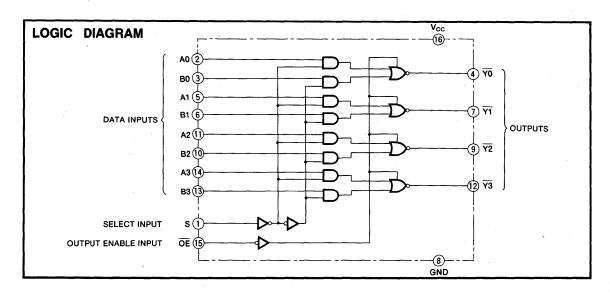
at \overline{Y} in synchronous with the clock pulse in the order A-B. S and output-enable input \overline{OE} are common to all four circuits. When \overline{OE} is high, all outputs Y will become high impedance state irrespective of other inputs.

FUNCTION TABLE (Note 1)

	Inp	Inputs				
ŌĒ	s	Α	В	Output Ÿ		
Н	×	×	х	Z		
L	L	L	Х	Н		
L	L	Н	Х	L		
L	н	X	L	н		
L	Н	Х	н	L		

Note 1 : X : Irrelevant

Z : High impedance



ABSOLUTE MAXIMUM RATINGS ($\tau_a = -40 \sim +85^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
Vi	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
		V ₁ < 0V	-20	
l _{IK}	Input protection diode current	$V_i > V_{CC}$	20	mA
	0.1-11.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1	V ₀ < 0V	-20	
Іок	Output parasitic diode current	Vo > Vcc	20	mA .
lo	Output current per output pin		±35	mA
loc	Supply/GND current	V _{CC} , GND	±75	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	°C

Note 2 : M74HC258FP, T $_a$ = $-40\sim+70^\circ$ C and T $_a$ = $70\sim85^\circ$ C are derated at -6mW/°C. M74HC258DP, T $_a$ = $-40\sim+50^\circ$ C and T $_a$ = $50\sim85^\circ$ C are derated at -5mW/°C.

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85 \%)$

0	D-			Limits						
Symbol	Pa	rameter	Min	Тур	Max	Unit				
Vcc	Supply voltage		2		6	٧				
Vı	Input voltage		0		Vcc	٧				
Vo	Output voltage		0		Vcc	٧				
Topr	Operating temperature range		40		+85	°C				
		V _{CC} = 2.0V	0		1000					
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns				
		$V_{CC} = 6.0V$			400					

ELECTRICAL CHARACTERISTICS

							Limits			
Symbol	Parameter	Test	conditions			25℃		-40~	+85℃	Unit
		l v		V _{cc} (V)	Min	Тур	Max	Min	Max	
		$V_0 = 0.1V, V_{cc}$	0.114	2.0	1.5			1.5		
V _{iH}	High-level input voltage	$ V_0 = 0.1V, V_{CO} $ $ I_0 = 20\mu A$;—0. 1 V	4.5	3.15		1	3.15		v
		$ 1_0 = 20\mu\text{A}$	= 20μΑ		4.2			4.2		
		V = 0.1V V	= 0.1V V = 0.1V			``	0.5		0.5	
VIL	Low-level input voltage	, ,	= 0.1V, V_{CC} -0.1V = 20 μ A				1.35	1	1.35	v
	× .	10 - 20μA					1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
		l _c	$I_{OH} = -20\mu A$	4.5	4.4			4.4		
V _{OH}	High-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		V
-			$I_{OH} = -6.0 mA$	4.5	4. 18			4.13		
			I _{OH} == -7.8mA	6.0	5.68			5.63		
			$i_{OL} = 20 \mu A$	2.0			0.1		0.1	
			$I_{OL} = 20 \mu A$	4.5			0.1		0.1	
VOL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1]	0.1	V
			I _{OL} = 6.0mA	4.5			0. 26		0.33	1
			I _{OL} = 7.8mA	6.0			0. 26		0.33	
I _{IH}	High-level input current	V _i = 6V		6.0			0.1		1.0	μA
I _L	Low-level input current	$V_i = 0V$		6.0			-0.1		-1.0	μA
I _{OZH}	Off-state high-level output current	$V_i = V_{iH}, \ V_{iL}, \ V_{iL}$	/o = Vcc	6.0			0.5		5.0	μA
lozL	Off-state low-level output current	$V_i = V_{iH}, V_{iL}, V_{iL}$	o = GND	6.0			-0.5		5.0	μA
I _C C	Quiescent supply current	VI = VCC, GND	$I_0 = 0\mu A$	6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS $(V_{cc} = 5V, T_a = 25^{\circ}C)$

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Symbol	Parameter	Test conditions		Unit		
Syllibol	raianietei	Test conditions	Min	Тур	Max	Unit
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time				.10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	$C_1 = 50 \text{pF} \text{ (Note 4)}$			18	ns
t _{PHL}	output propagation time (A, $B - \overline{Y}$)	CL = 50pr (Note 4)			18	ns
t _{PLH}	Low-level to high-level and high-level to low-level				18	ns
t _{PHL}	output propagation time $(S - \overline{Y})$	<u> </u>			18	ns
t _{PLZ}	Output disable time from low-level and high-level	$C_1 = 5 pF (Note 4)$			25	ns
t _{PHZ}	$(\overline{OE} - \overline{Y})$	OL — 5 pr (Note 4)			25	ns
t _{PZL}	Output enable time to low-level and high-level	C _L = 50pF (Note 4)			28	ns
t _{PZH}	$(\overline{OE} - \overline{Y})$	OL — SUPP (NOTE 4)			28	ns

SWITCHING CHARACTERISTICS $(v_{cc} = 2\sim6v, T_a = -40\sim+85\%)$

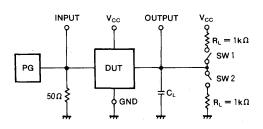
						Limits			
Symbol	Parameter	Test conditions			25℃		-40~	+85℃	Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0			60		75	
t _{TLH}	Low-level to high-level and		4.5			12	'	15	ns
	high-level to low-level	C _L = 50pF (Note 4)	6.0			10		13	
	Iligit-level to low-level	CL — Supr (Note 4)	2.0			60		75	
t _{THL}	output transition time		4.5		-	12		15	ns
			6.0			10		13	
			2.0			100		126	
t _{PLH}			4.5			20	Į	25	ns
]	C _L = 50pF (Note 4)	6.0			17		21	
		CL — Supr (Note 4)	2.0			100		126	
t _{PHL}	Low-level to high-level and	/	4. 5)	20		25	ns
	high-level to low-level		6.0	<u> </u>		17		21	
	output propagation time		2.0			150		189	
t _{PLH}	$(A, B - \overline{Y})$		4. 5	-		30		38	ns
]	C _L = 150pF (Note 4)	6.0		r	26		32 .	
		CL = 130pl (Note 4)	2.0			150		189	1
t _{PHL}	•		4.5	ļ	ļ	30		38	ns
			6.0			26		32	
			2.0			100		126	1
t _{PLH}	1		4.5	Ì		20	1	25	ns
		C _L = 50pF (Note 4)	6.0			17		21	
		CL — SUPP (Note 4)	2.0			100		126	1
t _{PHL}	Low-level to high-level and		4.5			20		25	ns
	high-level to low-level		6.0			17		21	
	output propagation time		2.0			150		189	
t _{PLH}	$(S-\overline{Y})$		4.5		ŀ	30		38	ns
		C ₁ = 150pF (Note 4)	6.0			26		32	
		CL — 130pr (Note 4)	2.0			150		189	
t _{PHL}			4.5		1	30	1	38	ns
			6.0		L	26		32	

SWITCHING CHARACTERISTICS $(v_{cc} = 2\sim 6V, T_a = -40\sim +85\%)$ (Continued)

						Limits			
Symbol	Parameter	Test conditions			25℃		-40~	+85°C	Uni
			V _{cc} (V)	Min Typ		Max	Min Max		
			2.0		-	150		189	
t _{PLZ}	Output disable time from		4. 5	1		30		38	ns
	low-level and high-level	C _L = 50pF (Note 4)	6.0			26		32	
	low-level and night-level	C _L = 50pF (Note 4)	2. 0			150		189	
t _{PHZ}	(OE − Y)		4.5			30		38	ns
			6.0			26		32	ĺ
			2.0			150		189	
t _{PZL}			4.5			30		38	ns
	1	C _L = 50pF (Note 4)	6, 0		1	26		32	
		C _L = 50pF (Note 4)	2.0			150		189	
t _{PZH}	Output eaable time to		4.5			30		38	ņs
	Land to the state of the state		6.0			26		32	
	low-level and high-level	٧.	2.0			200		252	
t _{PZL}	$(\overline{OE} - \overline{Y})$		4.5			40		50	ns
		0 = 150 5 (11.1 4)	6.0			34		43	
		C _L = 150pF (Note 4)	2.0			200		252	
t _{PZH}			4.5			40		50	ns
	·		6.0			34		43	
Cı	Input capacitance					10		10	рF
Со	Off-state output capacitance	OE = V _{CC}				15		15	рF
C _{PD}	Power dissipation capacitance (Note 3)								pF

Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipation during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$

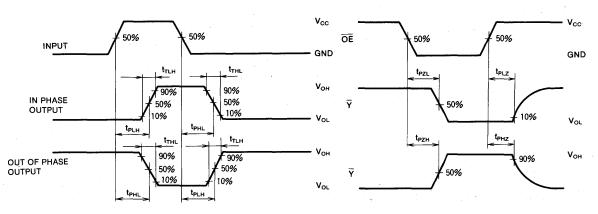
Note 4: Test Circuit



Parameter	SW 1	SW 2
t _{TLH} , t _{THL} t _{PLH} , t _{PHL}	Open	Open
t _{PLZ}	Closed	Open
t _{PHZ}	Open	Closed
t _{PZL}	Closed	Open
t _{PZH}	Open	Closed

- (1) The pulse generator (PG) has the following characteristics (10%~90%): $t_f=6ns,\ t_f=6ns$
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



MITSUBISHI HIGH SPEED CMOS

M74HC259P/FP/DP

8-BIT ADDRESSABLE LATCH/1-OF-8 DECODER

DESCRIPTION

The M74HC259 is a semiconductor integrated circuit consisting of eight latches and a demultiplexer which designates the latches with a 3-bit binary code.

FEATURES

- High-speed: 18ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2∼6V
- Wide operating temperature range: T_a=-40~+85℃

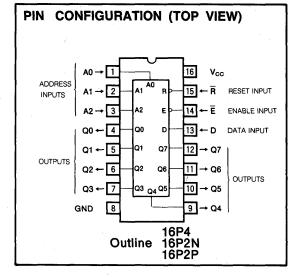
APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

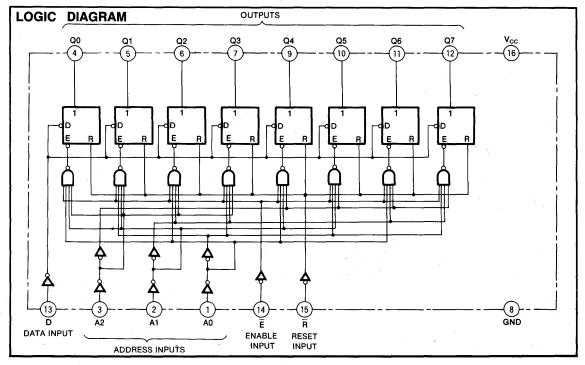
Use of silicon gate technology allows the M74HC259 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS259.

The M74HC259 consists of a 3-bit binary-to-octal demultiplexer and eight latchs. The following operational modes can be selected by combining the enable input $\overline{\rm E}$ and reset input $\overline{\rm R}$.



- (1) 3-bit binary-to-octal decoder/demultiplexer (\overline{E} low, \overline{R} low)
- (2) Addressable latch (E low, R high)
- (3) Data input inhibit (E high, R high)
- (4) Direct reset (E high, R low)

When this device is used as a 3-bit binary-to-octal decoder/demultiplexer, and the select inputs $A0\sim A2$ are designated by a 3-bit binary number, the same signal as the data



8-BIT ADDRESSABLE LATCH/1-OF-8 DECODER

input D will appear in one of the outputs $Q0 \sim Q7$ corresponding to that number and all the other outputs will be low. The latch does not operate in this mode. When used as an addressable latch and inputs $A0 \sim A2$ are designated as above, the corresponding latch will be selected and the same signal as D will appear in the output.

When E changes from low to high (data inhibit mode), the

information from the data input D immediately before the change will be latched. When \overline{E} is low, the signal appearing in Q will be also changed if the signal D is changed. In the data input inhibit mode, Q0 \sim Q7 will not change even if D is changed and the status before \overline{E} is high will be held. In the direct reset mode, all outputs will be reset to low, irrespective of the status of D or A0 \sim A2.

FUNCTION TABLE (Note 1)

0	-		Inp	uts		.,				Out	puts			
Operation mode	R	Ē	D	A0	A1	A2	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
Direct reset	L	Н	X	х	×	х	L	L	L	L	L	L.	L	L
	L	L	L	L	L	L	L	L	L	L	Ļ	L	L	L
	L	L	Н	L	L	L	Н.	L	L	L	L	L	L	L
3-bit binary-to-octal	L	L	L	Н	L	L	L	L	L	L	L	L	L	L
•	L	L	H	Н	L	L	L	Н	L	L	L	L	L	L
decoder/demultiplexer	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	L	L	L	Н	Н	Н	L	L	L	L	L	L	L	L
	L	L	H	Н	Н	Н	L	L	L	L	L	L	L	н
Data input suspension	Н	Н	Х	х	х	х	Q0º	Q1º	. Q2º	Q3º	Q4º	Q5°	Q6º	Q7º
	Н	L	L	L	L	L	L	Q1º	Q2º	Q3º	Q4º	Q5°	Q6º	Q7º
	Н	L	Н	L	L	L	Н	Q1º	Q2º	Q3º	Q4º	Q5º	Q6º	Q7º
	, н	L	L	Н	L	L	Q0°	L	Q2º	Q3º	Q4º	Q5º	Q6º	Q7º
Addressable latch	Н	L	Н	Н	L	L	Q0°	Н	Q2º	Q3º	Q4º	Q5º	Q6 ⁰	Q7º
	:	:	:	:	i	i	:	:	:	:	- i	:	:	:
	Н	L	L	Н	Н	H.	Q0°	Q1º	Q2 ⁰	Q3º	Q4º	Q5 ⁰	Q6º	L
	Н	L	,H	Н	Н	Н	Q0º	Q1º	Q2 ⁰	Q3º	Q4º	Q5 ⁰	Q6º	Н

Note 1: X : Irrelevant

Q0 : Output state Q before enable input changes

ABSOLUTE MAXIMUM RATINGS $(T_a = -40 \sim +85 \degree C$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		−0.5~+7.0	·V
V ₁	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
		V ₁ < 0V	-20	
lik	Input protection diode current	V _i > V _{CC}	20	mA.
	0.4-4	V ₀ < 0V	-20	^
lok	Output parasitic diode current	$V_{o} > V_{cc}$	20	⊢ mA
lo	Output current per output pin		±25	mA
Icc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		-65~+150	ာ

Note 2 : M74HC259FP, $T_a = -40 \sim +70^\circ C$ and $T_a = 70 \sim 85^\circ C$ are derated at -6mW/°C. M74HC259DP, $T_a = -40 \sim +50^\circ C$ and $T_a = 50 \sim 85^\circ C$ are derated at -5mW/°C.

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85 \degree c)$

				Limits					
Symbol	Pai	rameter	Min	Тур	Max	Unit			
V _{CC}	Supply voltage		2		6	٧			
V _I	Input voltage		0		Vcc	V			
Vo	Output voltage	0		V _{CC}	V				
Topr	Operating temperature ra	ange	-40		+85	°C			
		$V_{CC} = 2.0V$	0		1000				
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns			
•		$V_{CC} = 6.0V$			400	1			

8-BIT ADDRESSABLE LATCH/1-OF-8 DECODER

ELECTRICAL CHARACTERISTICS

: : : : : : : : : : : : : : : : : : : :		,					Limits			
Symbol	Parameter	Test	conditions			25℃		40~	+85℃	Unit
			V _{cc} (V)			Тур	Max	Min	Max	
		V = 0.1V V	0.11/	2, 0	1.5			1.5		
VIH	High-level input voltage		$V_0 = 0.1V$, $V_{0C} - 0.1V$ $ I_0 = 20\mu A$		3.15	٠.		3.15		V
		110) = 20µA			4.2			4.2		
		V = 0.1V V	V = 0.1V V = 0.1V				0.5		0.5	
VtL	Low-level input voltage	4 -	$V_{\rm O} = 0.1 \text{V}, V_{\rm CC} - 0.1 \text{V}$ $ I_{\rm O} = 20 \mu \text{A}$			Į	1.35		1.35	V
		1101 = 20μΑ					1.8		1.8	
			$i_{OH} = -20\mu A$	2.0	1.9			1.9		
			$I_{OH} = -20\mu A$	4.5	4. 4			4. 4		
VoH	High-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9	ļ		5.9		V
	· ·		$I_{OH} = -4.0 \text{mA}$	4.5	4. 18			4. 13		
	*		$I_{OH} = -5.2 mA$	6.0	5. 68			5.63		
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
			$I_{OL} = 20 \mu A$	4.5			0.1	1	. 0.1)
Vol	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
			I _{OL} = 4.0mA	4.5			0. 26		0.33	
			$I_{OL} = 5.2 mA$	6.0		ľ	0. 26		0.33	į
I _{IH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	
I _{IL}	Low-level input current	$V_i = 0V$		6.0			-0. 1		-1.0	μА
lcc	Quiescent supply current	VI = VCC, GND	$I_{0} = 0 \mu A$	6.0			4.0		40.0	μА

SWITCHING CHARACTERISTICS ($v_{cc} = 5v$, $T_a = 25$ °C)

Symbol	Parameter	Test conditions	Limits			Unit
Зуньы		l'est conditions	Min	Тур	Max	Unit
t _{TLH}	Low-level to high-level and high-level to low-level				10	
t _{THL}	output transition time				10 .	ns
t _{PLH}	Low-level to high-level and high-level to low-level				32	
t _{PHL}	output propagation time (D - Q)				32	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C ₁ = 15pF (Note 4)			38	ns
t _{PHL}	output propagation time (A - Q)	OL — 19pr (Note 4)			38	115
t _{PLH}	Low-level to high-level and high-level to low-level				35	ns
tpHL	output propagation time (E - Q)				35	115
t _{PHL}	High-level to low-level output propagation time $(\overline{R} + Q)$				27	ns

8-BIT ADDRESSABLE LATCH/1-OF-8 DECODER

SWITCHING CHARACTERISTICS ($v_{cc} = 2\sim6V$, $T_a = -40\sim+85$ °C)

						Limits			
Symbol	Parameter	Test conditions			25℃		-40~	+85℃	Uni
		· · · · · · · · · · · · · · · · · · ·	V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0			75		95	
t _{TLH}	Low-level to high-level and		4.5			15		19	
	high-level to low-level		6.0			13		16	
	nign-level to low-level		2.0		1	75		95	ns
t _{THL}	output transition time	·	4.5			15		19	
			6.0			13		16	
			2.0			180		225	
t _{PLH}	Low-level to high-level and		4.5			37		46	
	high-level to low-level		6.0			32		40	
	output propagation time		2.0			180		225	ns
t _{PHL}	(D - Q)		4.5		-	37		46	
			6.0		ł .	32		40	1
			2.0			220		275	
t _{PLH}	Low-level to high-level and	C _L = 50pF (Note 4)	4.5			43		54	
`	high-level to low-level		6.0			37		46	
	output propagation time		2. 0			220		275	ns
t _{PHL}	(A - Q)		4.5			43		54	
			6.0			37		46	
			2.0			200		250	
t _{PLH}	Low-level to high-level and		4.5			40		50	1
	high-level to low-level		6.0			35		44	l
	output propagation time		2.0			200		250	, na
t _{PHL}	(Ē — Q)	·	4.5			40		50	
			6.0			35		44	
	High-level to low-level		2. 0			150		190	
t _{PHL}	output propagation time		4.5			31		39	n
	(R̄ − Q)		6.0			26		- 32	
Cı	Input capacitance					10		10	pi
C _{PD}	Power dissipation capacitance (Note 3)				27				ρſ

Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.

The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$

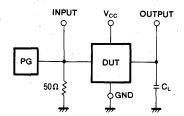
TIMING REQUIREMENTS ($v_{cc} = 2\sim6v$, $t_a = -40\sim+85$ °C)

Symbol	Parameter	Test conditions		25℃			-40~+85℃		Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0	80		-	100		
tw	E, R pulse width		4. 5	16	ĺ		20		ns
			6.0	14	`		18		
			2.0	100			125		
tsu	A, D setup time with		4.5	20		•	25		ns
	respect to E		6.0	15			19		-
		•	2.0	0			0		
th	A, D hold time with		4.5	0		[0		ns
	respect to E		6.0	0			0		

Note 4: Test Circuit

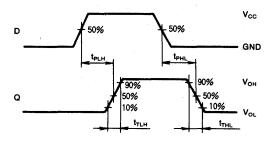
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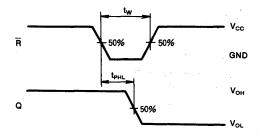
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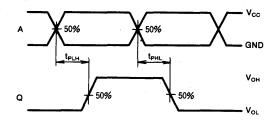


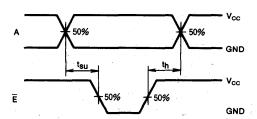
- (1) The pulse generator (PG) has the following characteristics (10% \sim 90%): $t_r = 6ns$, $t_f = 6ns$ (2) The capacitance C_L includes stray wiring
- capacitance and the probe input capacitance.

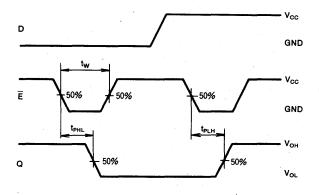
TIMING DIAGRAM

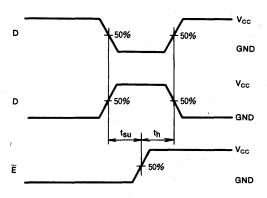














M74HC266P/FP/DP

QUADRUPLE 2-INPUT EXCLUSIVE NOR GATE

DESCRIPTION

The M74HC266 is a semiconductor integrated circuit consisting of four 2-input exclusive NOR gates.

FEATURES

- High-speed: 9ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: Ta=-40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC266 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS266.

Buffered outputs Y improve input-to-output transfer characteristics and reduce to a minimum output impedance variations with respect to input voltage variations.

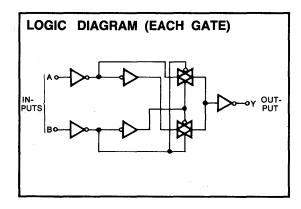
When both inputs A and B are either high or low, the output Y will become high, and when the levels of A and B are opposite, the output Y will become low.

Note that the outputs of M74HC266 and 74LS266 differ in that the outputs of the M74HC266 is not open drain.

This device of some makers is named 74HC7266.

FUNCTION TABLE

Inp	Output	
Α	В	Y
L	L	H
Н	L	L
L	Н	L
Н	Н	I



ABSOLUTE MAXIMUM RATINGS $(T_a = -40 \sim +85 \degree C)$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
	danak anakaskina diada ayanak	V ₁ < 0V	-20	4
lis	Input protection diode current	V _I > V _{CC}	20	mA
	0.4-4	V ₀ < 0V	-20	
юк	Output parasitic diode current	Vo > Vcc	20	mA
lo	Output current per output pin		±25	mA
loc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		-65~+150	င

Note 1 : M74HC266FP, T $_a$ = $-40\sim$ +60°C and T $_a$ = $60\sim$ 85°C are derated at -6mW/°C. M74HC266DP, T $_a$ = $-40\sim$ +50°C and T $_a$ = $50\sim$ 85°C are derated at -5mW/°C.

QUADRUPLE 2-INPUT EXCLUSIVE NOR GATE

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85 \circ c)$

Comple at	Parameter			Limits					
Symbol	Pa	rameter	Min	Тур	Max	Unit			
Vcc	Supply voltage		. 2		6	٧			
V _I	Input voltage		0		Vcc	٧			
Vo	Output voltage		0		Vcc	٧			
Topr	Operating temperature re	ange	40		+85	°C			
		V _{CC} = 2.0V	0		1000				
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns			
	V _{CC} = 6.0V		0		400				

ELECTRICAL CHARACTERISTICS

			Test conditions				Limits			
Symbol	Parameter	Test			25℃			40~+85℃		Unit
				V _{CC} (V)	Min	Тур	Max	Min	Max	
		Vo = 0.1V, Voc	0.11/	2.0	1.5			1.5		-
ViH	High-level input voltage	$ I_0 = 20\mu A$;0.1 v	4.5	3.15			3.15		V.
		1101 - 20µA		6.0	4.2			4.2		
		Vo = 0.1V, Voc	_0.11/	2.0			0. 5		0.5	
VIL	Low-level input voltage	$ I_0 = 20\mu A$	5-0.1 V	4.5			1.35		1.35	V
		1101 - 20μΑ		6.0			1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9	Ī	
ł			$I_{OH} = -20\mu A$	4.5	4.4			4.4		
V _{OH}	High-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		V
			I _{OH} = -4.0mA	4. 5	4. 18			4.13		
			$I_{OH} = -5.2 \text{mA}$	6.0	5. 68			5. 63		
			$I_{OL} = 20 \mu A$	2.0			0.1		0. 1	
			$I_{OL} = 20 \mu A$	4. 5			0.1		0.1	
VoL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
			I _{OL} = 4.0mA	4.5			0.26		0.33	
			I _{OL} = 5. 2mA	6.0			0.26		0.33	
Чин	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μΑ
I _{IL}	Low-level input current	V ₁ = 0V		6.0			-0.1		-1.0	μΑ
loc	Quiescent supply current	VI = VCC, GND	$I_0 = 0 \mu A$	6.0			1.0		10.0	μΑ

QUADRUPLE 2-INPUT EXCLUSIVE NOR GATE

SWITCHING CHARACTERISTICS ($v_{cc} = 5v$, $T_a = 25^{\circ}C$)

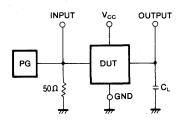
Courselle and	Parameter	Test conditions		Unit		
Symbol		lest conditions	Min	Тур	Max	Unit
t _{TLH}	Low-level to high-level and high-level to low-level	,			10	ns
t _{THL}	output transition time	0 = 15-5 (N-4- 2)			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = 15pF (Note 3)			20	ns
t _{PHL}	output propagation time				20	ns

SWITCHING CHARACTERISTICS $(V_{cc} = 2\sim 6V, T_a = -40\sim +85^{\circ}C)$

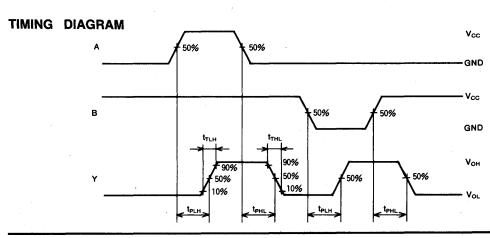
						Limits			
Symbol	Parameter	ter Test conditions		25℃			-40~+85°C		Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0			75		95	
t _{TLH}	Low-level to high-level and		4.5			15		19	ns
			6.0			13		16	
	high-level to low-level		2.0			75		95	
t _{THL}	output transition time		4.5			15		19	ns
		50 5 (11 1 2)	6.0			13		16	•
		$C_L = 50 pF \text{ (Note 3)}$	2.0			120		151	
t _{PLH}	Low-level to high-level and		4.5			24		30	ns
			6.0			20		26	
	high-level to low-level	•	2.0			120		151	
t _{PHL}	output propagation time		4.5			24		30	ns
			6.0			20		26	
Cı	Input capacitance	<u> </u>				10		10	pF
C _{PD}	Power dissipation capacitance (Note 2)				38				pF

Note 2: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per gate) The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$

Note 3: Test Circuit



- (1) The pulse generator (PG) has the following characteristics (10% \sim 90%): $t_r = 6ns$, $t_f = 6ns$ (2) The capacitance C_L includes stray wiring
- capacitance and the probe input capacitance.



M74HC266AP/FP/DP

QUADRUPLE 2-INPUT EXCLUSIVE NOR GATE WITH OPEN-DRAIN OUTPUTS

DESCRIPTION

The M74HC266A is a semiconductor integrated circuit consiting of four 2-input exclusive NOR gates with open-drain outputs.

FEATURES

- Open drain outputs
- High-speed: 8ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2∼6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

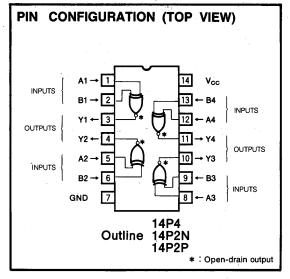
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC266A to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS266.

Open-drain outputs permit a versatile selection of high output impedances by means of externally connected load resistors. This makes "AND ties" a possibility, unlike the case of normal gates.

When both inputs A and B are either high or low, the output Y will become high, and when the levels of A and B are opposite, the output Y will become low.

Note that, unlike 74LS266, voltages higher than V_{CC} must not be applied to the output.

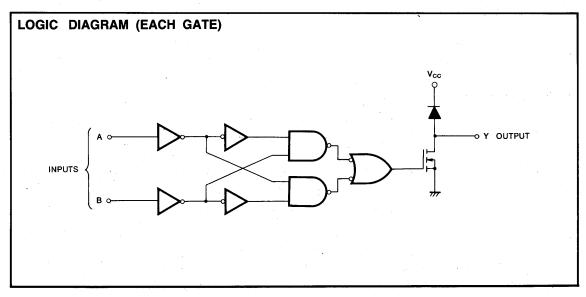


For application requiring normal outputs, another device, the M74HC266 is available with the same functions and pin configuration.

This device of some makers is named 74HC266.

FUNCTION TABLE

` Inp	Output	
Α	В	Y
L	L	Н
н	L	L
L	Н	L
Н	Н	Н



QUADRUPLE 2-INPUT EXCLUSIVE NOR GATE WITH OPEN-DRAIN OUTPUTS

ABSOLUTE MAXIMUM RATINGS $(T_a = -40 \sim +85 ^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		−0.5~+7.0	V
V _I	Input voltage		-0.5~V _{CC} +0.5	٧
Vo	Output voltage		-0.5~V _{cc} +0.5	V
	least seatestics died - somet	V ₁ < 0V	-20	
l _{IK}	Input protection diode current	$V_i > V_{CC}$	20	mA
	Outside and a surrout	V ₀ < 0V	-20	
юк	Output parasitic diode current	V _o > V _{cc}	20	mA mA
Io	Output current per output pin		25	mA.
Icc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		-65~+150	°C

Note 1 : M74HC266AFP, T $_a$ = $-40\sim+60^\circ$ C and T $_a$ = $60\sim85^\circ$ C are derated at -6mW/°C. M74HC266ADP, T $_a$ = $-40\sim+50^\circ$ C and T $_a$ = $50\sim85^\circ$ C are derated at -5mW/°C.

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85^{\circ}C)$

Oursk at	D			Limits		l lait
Symbol	Pal	rameter	Min	Тур	Max	Unit
V _{cc}	Supply voltage		2		6	V
V _I	Input voltage		0		Vcc	V
Vo	Output voltage		0		Vcc	V
Topr	Operating temperature ra	ange	-40	-	+85	Ç
		$V_{CC} = 2.0V$	O´		1000	
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns
		$V_{CC} = 6.0V$	0		400	

ELECTRICAL CHARACTERISTICS

							Limits			
Symbol	Parameter	Test	conditions		25°C			−40 ~	Unit -	
				V _{CC} (V)	Min	Тур	Max	Min	Max	
		$V_{\rm o} = 0.1 V, V_{\rm cc}$	0 11/	2.0	1.5			1.5		
V _{IH}	High-level input voltage	$ V_0 = 0.1V, V_{CC}$ $ I_0 = 20\mu A (No$		4.5	3. 15			3.15		V
		$ 10 = 20\mu A (NO)$	te 3)	6.0	4.2			4.2		
		$V_0 = 0.1V, V_{CC}$	0.11/	2.0			0.5		0.5	
V _{IL}	Low-level input voltage	$ V_0 = 0.1V, V_{CC}$ $ I_0 = 20\mu A (No$		4.5			1.35		1.35	V
		1101 — 20µA (NO	ile 3)	6.0			1.8		1.8	
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
,			$I_{OL} = 20 \mu A$	4.5			0.1		0.1	
VoL	Low-level output voltage	$V_I = V_{IH}, V_{IL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
			I _{OL} = 4.0mA	4.5			0.26		0.33	
			$I_{OL} = 5.2 mA$	6.0			0.26		0.33	
I _{IH}	High-level input current	$V_1 = 6V$		6.0			0.1		1.0	μA
l _{IL}	Low-level input current	$V_1 = 0V$		6.0			-0.1		-1.0	μA
	Maximum output lookaga aurrant	$V_{i} = V_{iH}, V_{iL}, V$	$v_0 = V_{CC}$	6.0			0.5		5.0	μA
Io	Maximum output leakage current	$V_{i} = V_{iH}, \ V_{iL}, \ V$	o = GND	6.0			-0.5		-5. 0	μΑ
Icc	Quiescent supply current	$V_I = V_{CC}$, GND.	$I_0 = 0 \mu A$	6.0			1.0		10.0	μA

SWITCHING CHARACTERISTICS $(v_{cc} = 5v, \tau_a = 25^{\circ}C)$

Cumbal	Dovomator	Took conditions		Unit			
Symbol	Symbol Parameter Test conditions		Min	Тур	Max	01111	
	High-level to low-level output transition time	$R_L = 1 k\Omega$			10		
t _{THL}	nigh-level to low-level output transition time	$C_L = 15pF $ (Note 3)			10	ns	
t _{PLH}	Low-level to high-level and high-level to low-level	$R_L = 1 k\Omega$, $C_L = 5 pF$ (Note 3)	,		23	. ns	
t _{PHL}	output propagation time	$R_L = 1 k\Omega$, $C_L = 15 pF$ (Note 3)			17	ns	

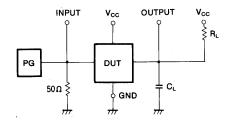
QUADRUPLE 2-INPUT EXCLUSIVE NOR GATE WITH OPEN-DRAIN OUTPUTS

SWITCHING CHARACTERISTICS ($V_{cc} = 2\sim 6V$, $T_a = -40\sim +85^{\circ}C$)

						Limits			
Symbol	Parameter	Test conditions			25℃		-40~	+85℃	Unit
		V _{cc} (V)		Min	Тур	Max	Min -	Max	
	High level to level		2.0			75		95	
t _{THL}	High-level to low-level		4.5			15		19	ns
	output transition time		6.0			13		16	
,		B = 11:0	2.0			125		155	
t _{PLH}	Low-level to high-level and	$R_{L} = 1 k\Omega$ $C_{L} = 50 pF \text{ (Note 3)}$	4.5			25		31	ns
	Atab tanal ta tanal	C _L = 50pr (Note 3)	6.0			23		26	
	high-level to low-level		2.0			100		125	
t _{PHL}	output propagation time		4.5			20		25	ns
		,	6.0			17		. 21	
Cı	Input capacitance					10		10	рF
Co	Output capacitance	A = B = V _{CC} , GND				10		10	pF
C _{PD}	Power dissipation capacitance (Note 2)				16				pF

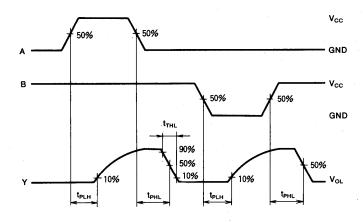
Note 2 : CPD is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per gate) The power dissipation during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$

Note 3: Test Circuit



- (1) The pulse generator (PG) has the following
- characteristics (10%~90%): t_f = 6ns, t_f = 6ns (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



M74HC273P/FP/DWP

OCTAL D-TYPE FLIP-FLOP WITH COMMON CLOCK AND RESET

DESCRIPTION

The M74HC273 is a semiconductor integrated circuit consisting of eight positive-edge triggered D-type flip flops with common clock and direct reset inputs.

FEATURES

- High-speed: (clock frequency) 40MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2∼6V
- Wide operating temperature range: Ta=-40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

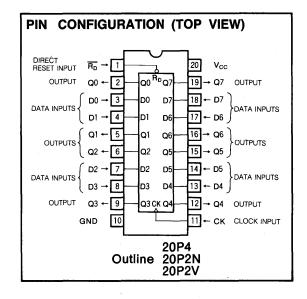
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC273 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74I S273

The M74HC273 contains eight edge-triggered D-type flip flops with common direct reset input $\overline{R_D}$ and common clock input CK.

When CK changes from low-level to high-level, the signals just previously input at D appears at output Q in accordance with the function table given.

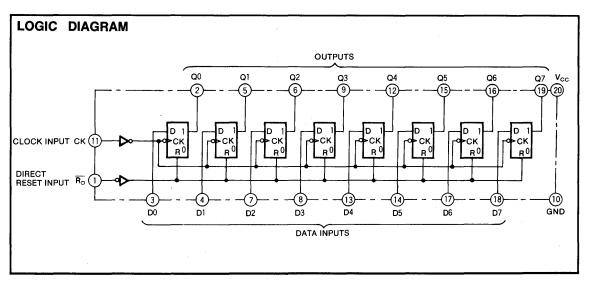
When $\overline{R_D}$ is low, all outputs Q will become low, irrespective of other inputs. When used as a D-type flip flop, $\overline{R_D}$ should be maintained high.



FUNCTION TABLE (Note 1)

	Inputs		Output
R₀	СК	D	. Q
L	x	X	L
Н	t ·	Н	н
н	1	L	L
Н	L	Х	Q°
Н	1	Х	Q°

- Note 1: † : Change from low to high
 - ↓ : Change from high to low
 - Q0 : Output state Q befor clock input changed
 - X : Irrelevant



OCTAL D-TYPE FLIP-FLOP WITH COMMON CLOCK AND RESET

ABSOLUTE MAXIMUM RATINGS $(T_a = -40 \sim +85\%$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
		V ₁ < 0V	-20	
l _{IK}	Input protection diode current	V ₁ > V _{CC}	20	mA .
		V ₀ < 0V	-20	
юк	Output parasitic diode current	V _o > V _{cc}	20	mA mA
lo	Output current per output pin		±25	mA
Icc	Supply/GND current	V _{CC} , GND	±50	mA
Pd .	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		-65~+150	°C

Note 2 : M74HC273FP, $T_a=-40\sim+75^\circ$ C and $T_a=75\sim85^\circ$ C are derated at -7mW/°C. M74HC273DWP, $T_a=-40\sim+80^\circ$ C and $T_a=80\sim85^\circ$ C are derated at -7mW/°C.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85 ^{\circ}C)$

Cumbal	Parameter			Limits				
Symbol	, Pai	raiametei				Unit		
Vcc	Supply voltage		` 2		6	٧		
Vı	Input voltage		0		Vcc	٧		
Vo	Output voltage		. 0		Vcc	V		
Topr	Operating temperature ra	ange	-40		+85	ာ		
		$V_{CC} = 2.0V$	0		1000			
t _r , t _f	Input risetime, failtime	$V_{CC} = 4.5V$	0		500	ns		
		$V_{CC} = 6.0V$	0		400			

ELECTRICAL CHARACTERISTICS

				,			Limits			
Symbol	Parameter	Test	conditions			25℃		-40~	+85℃	Unit
			Vcc		Min	Тур	Max	Min	Max	
		V = 0.1V V	0.114	2.0	1.5			1.5		
VIH	High-level input voltage	$V_0 = 0.1V, V_{CO}$		4.5	3. 15		1	3.15		V
		$ I_0 = 20\mu A$		6.0	4.2			4.2		
		V = 0.1V V	0.114	2.0			0.5		0.5	
VIL	Low-level input voltage	$V_0 = 0.1V, V_{C}$		4.5			1.35		1.35	V
	*	$ I_0 = 20\mu A$		6.0			1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
			$I_{OH} = -20\mu A$	4.5	4.4	ľ		4. 4		
VoH	High-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9			5. 9		V
			$I_{OH} = -4.0 mA$	4.5	4. 18			4.13		
			$I_{OH} = -5.2 mA$	6.0	5. 68	[5.63		
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
			$I_{OL} = 20 \mu A$	4.5			0.1	ļ	0.1	
V_{OL}	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
			$I_{OL} = 4.0 mA$	4.5			0. 26		0.33	
			$I_{OL} = 5.2 \text{mA}$	6.0			0. 26		0.33	
I _{IH}	High-level input current	V _i = 6V		6.0			0.1		1.0	μΑ
I _{IL}	Low-level input current	V ₁ = 0V		6.0			-0.1		-1.0	μA
Icc	Quiescent supply current	VI = VCC, GNE	$I_0 = 0 \mu A$	6.0			4.0		40.0	μA

OCTAL D-TYPE FLIP-FLOP WITH COMMON CLOCK AND RESET

SWITCHING CHARACTERISTICS $(v_{cc} = 5v, T_a = 25\%)$

Symbol	Parameter	Test conditions		Unit		
Symbol	Parameter	rest conditions	Min	Тур	Max	Onit
fmax	Maximum clock frequency		30			MHz
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time				10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = 15pF (Note 4)			27	ns
t _{PHL}	output propagation time (CK - Q)				27	ns
	High-level and high-level to low-level				07	
t _{PHL}	$(\overline{R_D} - Q)$				27	ns

SWITCHING CHARACTERISTICS ($V_{cc} = 2\sim 6V$, $T_a = -40\sim +85\%$)

						Limits			
Symbol	Parameter	Test conditions			25℃		-40~	+85℃	Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0	5			4		
fmax	Maximum clock frequency		4.5	27			21		MHz
			6.0	32			25		
		y .	2.0			75		95	
t _{TLH}	Low-level to high-level and		4.5			15		19	ns
	F1-F 114- 11		6.0			13		16	
	high-level to low-level		2.0			75		95	
t _{THL}	output transition time		4.5		İ	15		19	ns
		0 = 50-5 (N-1-4)	6.0			13		16	1
		C _L = 50pF (Note 4)	2.0			160		202	
t _{PLH}	Low-level to high-level and	•	4.5			32		40	ns
	high-level to low-level		6.0			27		34	
-	output propagation time		2.0			160		202	
t _{PHL}	(CK - Q)		4.5			32		40	ns
	· ·		6.0		İ	27		34	
		1	2.0			160	-	202	
t _{PHL}	High-level to low-level output		4.5			32		40	ns
	propagation time (RD - Q)	·	6.0			27		34	
C ₁	Input capacitance		,			10		10	pF
C _{PD}	Power dissipation capacitance (Note 3)				65				pF

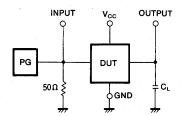
Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per flip-flop) The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS ($v_{cc} = 2\sim 6v$, $T_a = -40\sim +85^{\circ}$ C)

				Limits					
Symbol	Parameter	Test conditions		25℃			-40~+85℃		Unit
	•		V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0	80			101		
t _w	CK, R _D pulse width		4.5	16			20		ns
			6.0	14			17		
			2.0	100			126		
tsu	D setup time with		4.5	20			25		ns
	respect to CK		6.0	17			21		
		1	2. 0	0			0		
th	D hold time with		4.5	0			0	ł	ns
	respect to CK	\$	6.0	0			0		
		- ·	2.0	100			126		
trec	R _D recovery time with		4.5	20			25		ns
	respect to CK		6.0	17			21		

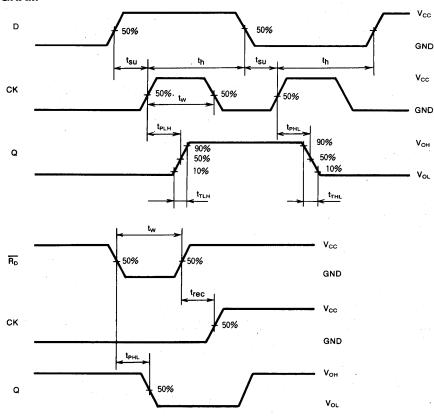
OCTAL D-TYPE FLIP-FLOP WITH COMMON CLOCK AND RESET

Note 4: Test Circuit



- (1) The pulse generator (PG) has the following characteristics (10% \sim 90%): t_f = 6ns, t_f = 6ns
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM







MITSUBISHI HIGH SPEED CMOS

M74HC279P/FP/DP

QUADRUPLE R-S LATCH

DESCRIPTION

The M74HC279 is a semiconductor integrated circuit consisting of four R-S flip flops.

FEATURES

- High speed: 15ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC} , min (V_{CC} =4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC279 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS279.

Two of the 4 circuits have set inputs $\overline{S_1}$ and $\overline{S_2}$ and reset input \overline{R} and the other 2 circuits have set input \overline{S} and reset input \overline{R} .

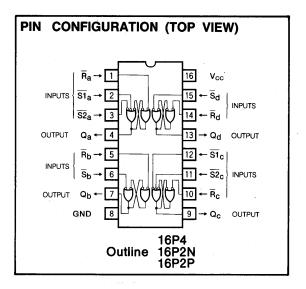
When $\overline{S_1}$ or $\overline{S_2}$ or both are low or \overline{S} is low, the output Q will become high, and when R is low, the output Q will become low. When $\overline{S_1}$ or $\overline{S_2}$ or both are low and \overline{R} is low, the output will become high but when each of the inputs simultaneously become high, the status of Q connot be predetermined.

FUNCTION TABLE (Note 1)

Inp	outs	Output		
s*	S* R			
Н	Н	Q°		
Н	L	L		
. L	Н	Н		
L	ı	н		

Note 1: Q⁰: Output state Q before input conditions are set

When S consists of two inputs, H indicates S₁ and S₂ are both high, L indicates either S₁ or S₂ is low.



M74HC280P/FP/DP

9-BIT ODD/EVEN PARITY GENERATOR/CHECKER

DESCRIPTION

The M74HC280 is a semiconductor integrated circuit consisting of a 9-bit parity generator/checker.

FEATURES

- High-speed: 20ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide supply voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85°C

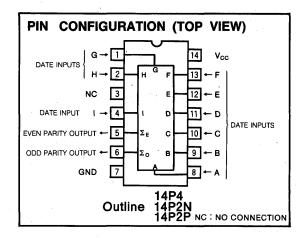
APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC280 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS280.

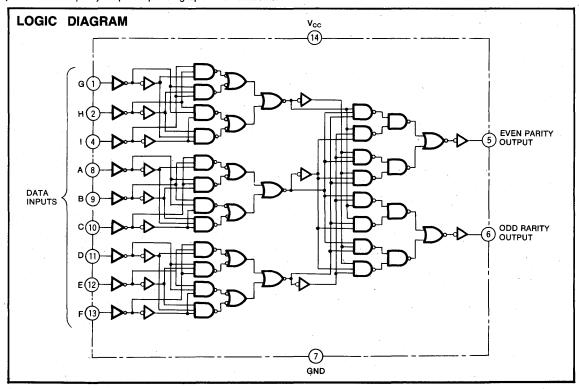
The M74HC280 combines the functions of a 9-bit parity generator and a parity checker. When used as a parity generator, applying 9-bit data to date inputs A through I will result in a generation of parity output to the even parity output or the odd parity output depending upon the number of



high values in the data input. See the Function Table for details. When used as a parity checker, one bit from among the 9 bits of data input is used as an odd or even parity designation and the remaining eight bits are used as date.

FUNCTION TABLE

Number of date input high values	EVEN PARITY	ODD PARITY
Even	H	L
Odd	L	Н





9-BIT ODD/EVEN PARITY GENERATOR/CHECKER

ABSOLUTE MAXIMUM RATINGS $(\tau_a = -40 \sim +85 \degree$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{CC} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
		V ₁ < 0V	-20	^
IIK	Input protection diode current	V _I > V _{CC}	20	mA
	Outside and a surroad	V ₀ < 0V	-20	
ок	Output parasitic diode current	V _o > V _{cc}	20	mA
l _o	Output current per output pin		±25	mA
lcc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		-65∼+150	°C

Note 1 : M74HC280FP, T $_a$ = $-40\sim$ +60°C and T $_a$ = $60\sim$ 85°C are derated at -6mW/°C. M74HC280DP, T $_a$ = $-40\sim$ +50°C and T $_a$ = $50\sim$ 85°C are derated at -5mW/°C.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85^{\circ}C)$

Cumhal	Parameter			Limits				
Symbol	, ra	rameter	Min	Тур	Max	Unit		
Vcc	Supply voltage		2		6	· v		
Vı	Input voltage		0		Vcc	V		
Vo	Output voltage		0		Vcc	٧		
Topr	Operating temperature range		-40		+85	တ္		
		$V_{CC} = 2.0V$	0	-	1000			
t _r , t _f Input rise	Input risetime, falltime	$V_{CC} = 4.5V$. 0		500	ns		
		$V_{CC} = 6.0V$	0		400			

ELECTRICAL CHARACTERISTICS

					Limits					
Symbol	Parameter	Ţest	conditions		25℃			-40~+85°C		Unit
					Min	Тур	Max	Min	Max] !
		V = 0.1V V	- 0.1W	2.0	1.5			1.5		
V _{IH}	High-level input voltage	$ I_0 = 20\mu A$	$V_0 = 0.1V, V_{CC} - 0.1V$		3.15			3.15		V
		$ I_0\rangle = 20\mu$ A	_	6.0	4.2			4. 2		
		V = 0.1V V	$V_0 = 0.1V, V_{CC} - 0.1V$				0.5		0.5	
VIL	Low-level input voltage	$ I_0 = 20\mu A$	-0.1 V	4.5			1.35		1.35	V
	<u> </u>	1101 - 20AA		6.0			1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
		$I_{OH} = -20\mu A$	4.5	4.4		1	4.4			
V _{OH}	High-level output voltage	$V_I = V_{IH}, \ V_{IL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		V
	-		$I_{OH} = -4.0 \text{mA}$	4.5	4.18			4. 13	-	
			$I_{OH} = -5.2 \text{mA}$	6.0	5.68			5. 63	-	
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
			$I_{OL} = 20 \mu A$	4, 5			0.1		0. 1	
VoL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		′0 . 1	V
		· ·	I _{OL} = 4.0mA	4.5			0.26		0.33	
			$I_{OL} = 5.2 \text{mA}$	6.0			0. 26		0.33	
ͺl _{iH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μΑ
l _{IL}	Low-level input current	$V_1 = 0V$		6.0			-0. 1		-1.0	μA
Icc	Quiescent supply current	$V_i = V_{CC}$, GND	$I_0 = 0\mu A$	6.0			4.0		40.0	μA

9-BIT ODD/EVEN PARITY GENERATOR/CHECKER

SWITCHING CHARACTERISTICS ($v_{cc} = 5v$, $t_a = 25^{\circ}C$)

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Symbol	Parameter	Test conditions	Limits			Unit
Symbol		lest conditions	Min	Тур	Max	Unit
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time	0 - 15-5 (Note 2)			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = 15pF (Note 3)	-		35	ns
tenL	output propagation time				35	ns

SWITCHING CHARACTERISTICS ($v_{cc} = 2\sim6v$, $T_a = -40\sim+85^{\circ}C$)

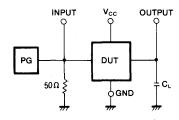
		•			Limits				
Symbol	Parameter	Test conditions			25℃			+85°C	Unit
	LOW-level to high-level and high-level to low-level output transition time		V _{CC} (V)	Min	Тур	Max	Min	Max]
			2.0			75		95	
t _{TLH}	Low-level to high-level and		4.5			15		19	ns
	high lavel to lave be an		6.0			13		16	
	nign-level to low-level		2.0			75		95	
t _{THL}	output transition time		4.5			15		19	ns
		0 50 5 (11.1.2)	6.0		1	13		16	
	I I I I I I	C _L = 50pF (Note 3)	2.0			205		258	
t _{PLH}	Low-level to high-level and		4.5			41		52	ns
	high-level to low-level		6.0			35		44	
	output propagation time		2.0			205		258	
t _{PHL}	A~I- EVEN PARITY	•	4.5			41		52	ns
	ODD PARITY		6.0			35		44	
Cı	Input capacitance	-	7			10		10	рF
C _{PD}	Power dissipation capacitance (Note 2)				92				pF

Note 2: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per gate)

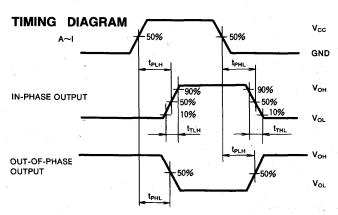
The power dissipated during operation under no-load conditions is calculated using the following formula:

P_D = C_{PD} · V_{CC}² · f_i+I_{CC} · V_{CC}

Note 3: Test Circuit



- (1) The pulse generator (PG) has the following characteristics (10% \sim 90%): $\rm t_f=6ns, \ t_f=6ns$
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.





MITSUBISHI HIGH SPEED CMOS

M74HC283P/FP/DP

4-BIT BINARY FULL ADDER WITH FAST CARRY

DESCRIPTION

The M74HC283 is a semiconductor integrated circuit consisting of a 4-bit full adder.

FEATURES

- High-speed: 30ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2∼6V
- Wide operating temperature range: Ta=-40~+85℃

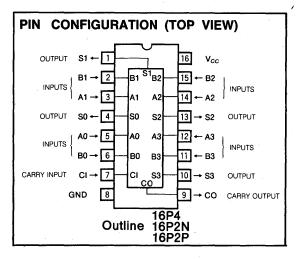
APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC283 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS283.

The M74HC283 is a 4-bit binary full adder. When 4-bit binary values applied inputs A0~A3 and B0~B3, and the carry signal from the previous stage is applied to carry input CI, the corresponding sum output for the respective bits will appear at S0~S3 and the carry output will appear at C0.

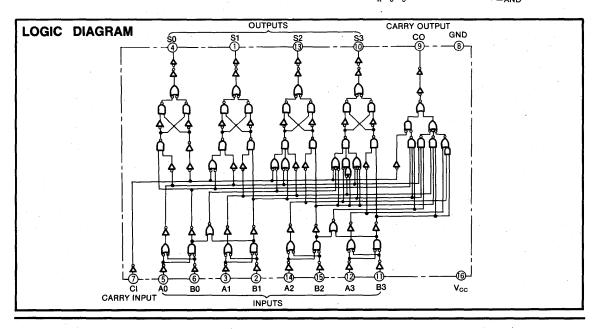


FUNCTION TABLE (Note 1)

	Inputs		Outputs		
C _{K-1}	Aĸ	B _K	Sĸ	Cĸ	
L	L	L	L	L.	
L .	Н	L	Н	L	
L	L	Н	Н	L	
L	Н	н .	L	Н	
Н	L	L	Н	L	
Н	н	L	L	Н	
н	L	н	L	Н	
Н	Н	Н	Н	Н	

Note 1: S_K and C_K are sum and carry outputs generated by the sum of addends A_K and B_K and carry input C_{K-1} . Their values are given by the following logical equations.

$$\begin{array}{lll} S_K \!\!=\! A_K \!\!\oplus\! B_K \!\!\oplus\! C_{K-1} & \oplus \!\!=\! \text{Exclusive OR} \\ C_K \!\!=\! A_K \!\!\cdot\! B_K \!\!+\! (A_K \!\!+\! B_K) \!\!\cdot\! C_{K-1} & + \!\!\!=\! \text{OR} \\ k \!\!=\! 0 \!\!\sim\! 3 & \cdot \!\!\!=\! \text{AND} \end{array}$$



4-BIT BINARY FULL ADDER WITH FAST CARRY

ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85^{\circ}$), unless otherwise noted)

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Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		−0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	٧
	Inc. A contact diagram of the contact of the contac	V ₁ < 0V	-20	T
l _{IK}	Input protection diode current	V ₁ > V _{CC}	20	mA
•	C. A	V ₀ < 0V	-20	
lok	Output parasitic diode current	V _o > V _{cc}	20	mA
lo	Output current per output pin		±25	mA
Icc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		-65~+150	°C.

Note 2 : M74HC283FP, T_a = $-40\sim+70^\circ$ C and T_a = $70\sim85^\circ$ C are derated at -6mW/°C. M74HC283DP, T_a = $-40\sim+50^\circ$ C and T_a = $50\sim85^\circ$ C are derated at -5mW/°C.

RECOMMENDED OPERATING CONDITIONS (Ta = -40~+85°C)

0	Parameter			Limits				
Symbol	Par	rameter	Min	Тур	Max	Unit		
Vcc	Supply voltage		2		6	V		
Vi	Input voltage		0		Vcc	v		
Vo	Output voltage		0		Vcc	٧		
Topr	Ambient operating temperature		-40		+85	င		
		V _{CC} = 2.0V	0		1000			
t _r , t _f	input risetime, falltime	V _{CC} = 4.5V	0		500	ns		
		V _{CC} = 6.0V	0		400			

ELECTRICAL CHARACTERISTICS

				Limits						
Symbol	Parameter Test conditions		25℃			40~+85°C		Unit		
				V _{cc} (V)	Min	Тур	Max	Min	Max]
		$V_0 = 0.1V, V_{CC} = 0.1V$		2.0	1.5			1.5		
V_{iH}	High-level input voltage	$ V_0 = 0.1V, V_{CC}$ $ I_0 = 20\mu A$.—U.1V	4.5	3.15			3. 15	7	V.
		$ 1_{\mathbf{O}} = 20\mu\mathbf{A}$		6.0	4. 2			4.2		
		V = 0.1V V	$V_0 = 0.1V, V_{CC} - 0.1V$				0.5		0.5	
V_{IL}	Low-level input voltage			4.5			1.35		1.35	V
	$ I_0 = 20\mu A$		6.0			1.8		1.8		
		1 1 1	$I_{OH} = -20\mu A$	2.0	1.9			1.9		
		1	$I_{OH} = -20\mu A$	4.5	4. 4			4.4		
VoH	High-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		V
			$I_{OH} = -4.0 \text{mA}$	4.5	4.18		· ·	4.13		
			$I_{OH} = -5.2 \text{mA}$	6.0	5. 68			5.63	Ì	
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
			$I_{OL} = 20 \mu A$	4.5			0.1		0.1	}
VoL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0, 1	V
			I _{OL} = 4.0mA	4.5			0. 26		0. 33]
			I _{OL} = 5. 2mA	6.0			0. 26		0.33	
I _{IH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μΑ
l _{1L}	Low-level input current	V ₁ = 0V		6.0			-0.1		-1.0	μΑ
loc	Quiescent supply current	VI = VCC, GND	$I_0 = 0 \mu A$	6, 0			4.0		40.0	μΑ

4-BIT BINARY FULL ADDER WITH FAST CARRY

SWITCHING CHARACTERISTICS ($v_{cc} = 5v$, $T_a = 25\%$)

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Symbol	Parameter	Test conditions		Limits		
	r aranteter	rest conditions	Min	Тур	Max	Unit
t _{TLH}	Low-level to high-level and high-level to low-level				10	
t _{THL}	output transition time		-		10	ns
t _{PLH}	Low-level to high-level and high-level to low-level				38	
t _{PHL}	output propagation time (CI - SK)				38	ns
t _{PHL}	Low-level to high-level and high-level to low-level	C _L = 15pF (Note 4)			49	ns
*PHL	output propagation time (A _K , B _K - S _K)	OL — ISPI (NOTE 4)	1		49	lis
tpLH	Low-level to high-level and high-level to low-level				31	
t _{PHL}	output propagation time (CI - CO)				31	ns
t _{PLH}	Low-level to high-level and high-level to low-level				41	
t _{PHL}	output propagation time (A _K , B _K — CO)				41	ns

SWITCHING CHARACTERISTICS ($V_{cc} = 2\sim 6V$, $T_a = -40\sim +85^{\circ}$)

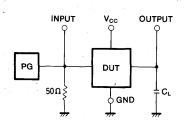
						Limits			1
Symbol	Parameter	Test conditions			25℃		-40~	+85℃	Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0			75		90	
t _{TLH}	Low-level to high-level and		4.5			15		18	ns
	high-level to low-level		6.0			13	ĺ	16	
	nign-level to low-level		2.0	-		- 75		90	
t _{THL}	output transition time		4.5		1.	15	1	18	ns
			6.0			13		16	
			2.0			210		265	
t _{PLH}	Low-level to high-level and		4.5			42		53	ns
	high-level to low-level		6.0			36		45	
	output propagation time		2. 0			210		265	
t _{PHL}	(CI - S _K)		4.5			42		53	ns
			6.0		,	36	1	45	
	high-level to low-level		2.0			270		340	
t _{PHL}	output propagation time	C _L = 50pF (Note 4)	4.5			54		68	ns
	(A _K , B _K - S _K)	'	6.0			46		58	
			2.0			175		220	
t _{PLH}	Low-level to high-level and		4.5			.35		44	ns
	high-level to low-level		6.0			30	, ,	37	
	output propagation time		2.0			175		220	-
t _{PHL}	(CI - CO)		4.5			35		44	ns
		<u> </u>	6.0			30]	37	
,			2.0			225		280	
t _{PLH}	Low-level to high-level and		4.5			45		56	ns
	high-level to low-level	1	6.0		 	38		48	
	output propagation time		2.0			225		280	
t _{PHL}	(A _K , B _K - CO)		4.5			45		56	ns
			6.0			38		. 48	
Cı	Input capacitance					10		10	pF
CPD	Power dissipation capacitance (Note 3)								pF

Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$



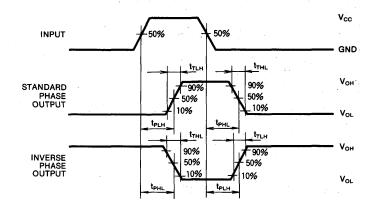
4-BIT BINARY FULL ADDER WITH FAST CARRY

Note 4: Test Circuit



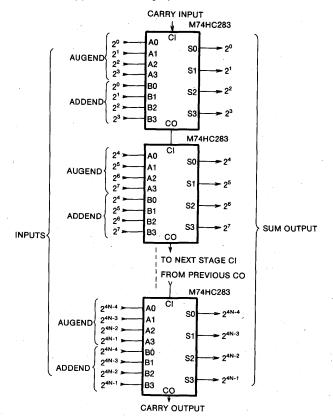
(1).The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
 (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



APPLICATION EXAMPLE

The 4N-bit binary parallel adder using N pieces of the M74HC283 is shown in the following.





MITSUBISHI HIGH SPEED CMOS

M74HC298P/FP/DP

QUADRUPLE 2-INPUT DATA SELECTOR/MULTIPLEXER WITH OUTPUT LATCH

DESCRIPTION

The M74HC298 is a semiconductor integrated circuit consisting of four 2- to 1-line multiplexer with temporary storage and common selector and clock inputs.

FEATURES

- High-speed: 17ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max
 (V_{CC}=5V, T_A=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

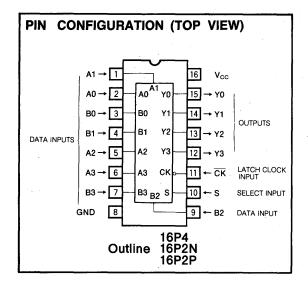
Use of silicon gate technology allows the M74HC298 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS298.

When selector input S is set low, data input B will be selected and when S is set high, data input A will be selected. When latch clock input \overline{CK} changes from high to low level, the selected data will appear at output Y. Since negative-edge trigger D-type flip flops are used for temporary storage, the state of Y is not affected by the state of A or B while \overline{CK} is high or low.

FUNCTION TABLE (Note 1)

	Inputs									
CK	S	В	Α	Y						
+	L	L ·	х	L						
+	L	Н	×	Н						
+ +	Н	×	L	L						
+	Н	Χ.	Н	Н						

Note 1 : ↓ : Change from high to low level (negative-edge trigger)
X : Irrelevant





MITSUBISHI HIGH SPEED CMOS

M74HC299P/FP/DWP

8-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER WITH 3-STATE PARALLEL OUTPUTS

DESCRIPTION

The M74HC299 is a semiconductor integrated circuit consisting of an 8-bit serial/parallel-input, serial/parallel-output shift register with 3-state outputs and a direct reset input.

FEATURES

- High-speed: 40MHz clock frequency typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2∼6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC299 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS299.

Use of mode select inputs S1 and S2 allows the device to operate in the following modes.

- (1) Parallel read S1="H" S2="H"
- (2) Right shift S1="H" S2="L"
- (3) Left shift S1="L" S2="H"
- (4) Clock inhibit S1="L" S2="L"

In the parallel data-read mode, 8-bit parallel data applied at parallel I/O pins $P_A/Q_A \sim P_H/Q_H$ will be stored in the flip flops when clock input CK changes from low-level to high-level.

In the right-shift mode, serial data applied at serial data input S_A will be right-shifted from P_A/Q_A to P_H/Q_H by one bit each time the clock input CK changes from low-level to high-level.

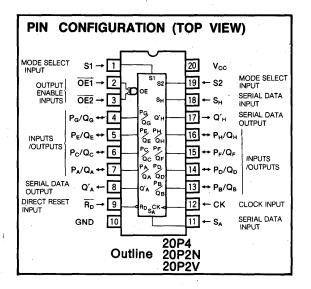
In the left-shift mode, serial data applied at serial data input S_H will be left-shifted from P_H/Q_H to P_A/Q_A by one bit each time the clock input CK changes from low-level to high-level.

In the clock inhibit mode, the clock pulse input is suppressed at each flip flop and the state of flip flop will not change and the previous states of the flip flops will be maintained. When $\overline{\text{OE1}}$ or $\overline{\text{OE2}}$ is high, $P_{\text{A}} \sim P_{\text{H}}$ will become high-impedance state Z. Changing $\overline{\text{OE1}}$ or $\overline{\text{OE2}}$ will not affect the contents of the flip flops.

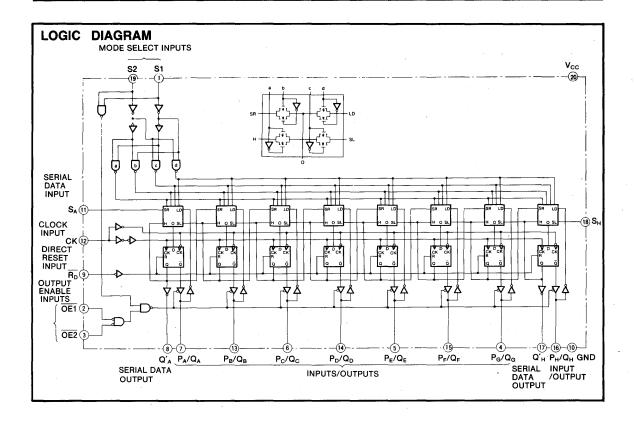
When direct reset input $\overline{R_D}$ is low, each flip flop will be reset low, irrespective of other inputs.

Serial data outputs Q'_{A} and Q'_{H} are used to extend the number of bits.

See Application Example.



8-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER WITH 3-STATE PARALLEL OUTPUTS



FUNCTION TABLE (Note 1)

Operation made				Inp	uts						P	arallel	data I/	O.			Serial dat	ta outputs
Operation mode	R_D	СК	S1	S2	SA	S _H	OE1	OE2	P _A /Q _A	P _B /Q _B	P _C /Q _C	P _D /Q _D	P _E /Q _E	P _F /Q _F	P _G /Q _G	P _H /Q _H	Q′ _A	à
Direct reset	L	Х	L	Х	Х	Х	L	L	L	L	L	L	L	L	L	L	L	L
Direct reset	L	Х	Х	L	Х	Х	L	L	L	L	L	L	L	L	L	L,	L	L
Righ shift	Н	Ť	Н	L	L	Х	L	L	L	Q _A ⁰	Q _B ⁰	Q _C ⁰	Q_D^0	Q _E ⁰	Q _F ⁰	Q_G^0	L	Q_G°
Aigir siiit	Н	<u>†</u>	Н	L	Н	Х	L	L	Н	Q _A ⁰	Q _B ⁰	Qc	Q₀°	Q _E ⁰	Q _F ^o	Q _G ⁰	Н	Q _G ⁰
Left shift	Н	1	L	٠H	Х	L	L	L	Q _B ⁰	Qcº	Q _D o	Q _E ⁰	Q_F^0	Q _G °	Q _H ^o	L	Q _B ^o	L
Leit siiiit	Н	†	L	Н	Х	Н	L	L	Q _B ⁰	Q _c °	Q _D ⁰	Q _E ⁰	Q _F ⁰	Q _G ⁰	QHO	Н	Q _B ^o	Н
Parallel read	Н	1	Н	Н	Х	Х	L	L	P _A	Рв	Pc	Pb	PE	P _F	P _G	Рн	PA	Рн
Clock inhibit	Н	Х	L	L	Х	Х	L	L	Q _A ⁰	Q _B ⁰	Qc°	Q _D o	Q _E ⁰	Q _F ⁰	QGO	Q _H ⁰	Q _A °	Q _H °
Clock innibit	Н	L	Х	Х	Х	Х	L	L	Q _A ⁰	Q _B ⁰	Q _C ⁰	Q _D ⁰	Q _E ⁰	Q _F ⁰	Q _G ⁰	Q _H ⁰	Q _A ⁰	Q _H ⁰
Output disable	X	Х	х	х	X	X	Н	L	Z	Z	Z	Z	Z	Z	Z	Z	Q _A ⁰	Q _H ⁰
(P _A /Q _A ~P _H /Q _H . are the high	Х	Х	х	Х	Х	Х	L	Н	Z	Z	Z	Z	Z	Z	Z	Z	Q _A ⁰	Q _H °
-impedance state.	Х	Х	Х	Х	Х	Х	Н	Н	Z	Z	Z	Z	Z	Z	Z	Z	Q _A ⁰	Q _H ⁰

Note 1: Qn^0 : Output state before input condisions are set.

X : Irrelevant

† : Change from low to high level (positive-edge trigger)

 $P_{\rm H}: P_{\rm A}/Q_{\rm A} \sim P_{\rm H}/Q_{\rm H}$ operate as inputs. $Q_{\rm A}'$ and $Q_{\rm H}'$ are in the same state as $P_{\rm A}$ and $P_{\rm H}$, respectively.

Z : High-impedance state. The flip flops are held in the same state as before P_A/Q_A~P_H/Q_H become the high-impedance state.

8-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER WITH 3-STATE PARALLEL OUTPUTS

ABSOLUTE MAXIMUM RATINGS ($\tau_a = -40 \sim +85 ^{\circ}\text{C}$, unless otherwise noted)

CONTRACTOR OF TAXES WELLIAM OF THE

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	V
Vo .	Output voltage		-0.5~V _{cc} +0.5	V
		V ₁ < 0V	-20	
I _{IK}	Input protection diode current	V _I > V _{CC}	20	→ mA
	G. 4 A	V ₀ < 0V	20	
lok	Output parasitic díode current	V _o > V _{cc}	20	mA.
lo	Output current (Q _A ~Q _H)		±35	mA
lo	Output currents (Q'A~Q'H)		±25	mA
Icc	Supply/GND current	V _{CC} , GND	±75	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		-65∼+150	°c

Note 2 : M74HC299FP, $T_a = -40 \sim +75^{\circ}C$ and $T_a = 75 \sim 85^{\circ}C$ are derated at -6mW/°C. M74HC299DWP, $T_a = -40 \sim +80^{\circ}C$ and $T_a = 80 \sim 85^{\circ}C$ are derated at -7mW/°C.

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85\%)$

O mah al	De.			Unit		
Symbol	Pai	rameter	Min	Тур	Max	Unit
Vcc	Supply voltage		,2		6	٧
Vı	Input voltage		0		Vcc	٧
Vo	Output voltage		0		Vcc	V
Topr	Ambient operating temperating	erature	-40		+85	္
		$V_{CC} = 2.0V$	0		1000	
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns
		$V_{CC} = 6.0V$	0		400	

8-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER WITH 3-STATE PARALLEL OUTPUTS

ELECTRICAL CHARACTERISTICS

							Limits			
Symbol	Parameter	Test	conditions			25℃		-40~	+85°C	Unit
,				V _{cc} (V)	Min	Тур	Max	Min	Max	
V _{IH}	High-level input voltage	$V_0 = 0.1V, V_{CO}$ $ I_0 = 20\mu A$	e−0.1V	2. 0 4. 5 6. 0	1.5 3.15 4.2			1.5 3.15 4.2		٧
V ₁ L	Low-level input voltage	$V_0 = 0.1V, V_{CC}$ $ I_0 = 20\mu A$	-0.1V	2. 0 4. 5 6. 0			0.5 1.35 1.8		0.5 1.35 1.8	٧
	High-level output voltage	$V_i = V_{iH}, \ V_{iL}$	$I_{OH} = -20\mu A$ $I_{OH} = -20\mu A$ $I_{OH} = -20\mu A$	2. 0 4. 5 6. 0	1.9 4.4 5.9	-		1.9 4.4 5.9	-	
V _{OH}	High-level output voltnge (P _A /Q _A ~P _H /Q _H)	$V_{I} = V_{IH}, \ V_{IL}$	$I_{OH} = -6.0 \text{mA}$ $I_{OH} = -7.8 \text{mA}$	4. 5 6. 0	4. 18 5. 68			4. 13 5. 63		V
	high-level output voltnge(Q'A, Q'H)	$V_i = V_{IH}, V_{IL}$	$I_{OH} = -4.0 \text{mA}$ $I_{OH} = -5.2 \text{mA}$	4. 5 6. 0	4. 18 5. 68			4. 13 5. 63		l
	Low-level output voltage	$V_i = V_{iH}, \ V_{iL}$	$I_{OL} = 20\mu A$ $I_{OL} = 20\mu A$ $I_{OL} = 20\mu A$	2. 0 4. 5 6. 0	i		0. 1 0. 1 0. 1		0. 1 0. 1 0. 1	
V _{OL}	Low-level output voltnge (P _A /Q _A ~P _H /Q _H)	$V_i = V_{iH}, \ V_{iL}$	$I_{OL} = 6.0 \text{mA}$ $I_{OL} = 7.8 \text{mA}$	4. 5 6. 0			0. 26 0. 26		0. 33 0. 33	V
	Low-level output voltnge (Q'A, Q'H)	$V_{i} = V_{iH}, \ V_{iL}$	$I_{OL} = 4.0 \text{mA}$ $I_{OL} = 5.2 \text{mA}$	4.5 6.0			0. 26 0. 26		0. 33 0. 33	
l _{iH}	High-level input current	$V_i = 6V$		6.0			0.1		1.0	μΑ
I _{IL}	Low-level input current	V ₁ = 0V	6.0			-0.1		-1.0	μΑ	
lozh	Off-state high-level output current	$V_i = V_{iH}, \ V_{iL}, \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \$	6.0			0.5		5.0	μА	
lozL	Off-state low-level output current	$V_{I} = V_{IH}, \ V_{IL}, \ V_{O} = GND$					-0.5		-5.0	μA
Icc	Quiescent supply current	$V_1 = V_{CC}$, GND; $I_0 = 0\mu A$					4.0		40.0	μΑ

SWITCHING CHARACTERISTICS ($v_{cc} = 5v$, $\tau_a = 25^{\circ}C$)

Complex	Parameter	Test conditions			Unit	
Symbol	rarameter	rest conditions	Min	Тур	Max	Oint
fmax	Maximum clock frequency		25			MHz
tTLH	Low-level to high-level and high-level to low-level]			10	ns
t _{THL}	output transition time				10	ns
t _{PLH}	Low-level to high-level and high-level to low-level				35	ns
t _{PHL}	output propagation time (CK — Q'A, Q'H)]			35	ns
t _{PHL}	High-level to low-level output propagation time $(\overline{R}_D - Q'_A, Q'_H)$	C _L = 50pF (Note 4)			40	ns
t _{PLH}	Low-level to high-level and high-level to low-level				35	ns
t _{PHL}	output propagation time (CK — Q _A ~Q _H)				35	ns
t _{PLH}	High-level to low-level output propagation time $(\overline{R_D} - Q_A \sim Q_H)$				40	ns
t _{PLZ}	Output disable time from low-level and high-level	C ₁ = 5pF (Note 4)			25	ns
t _{PHZ}	(OE - Q _A ~Q _H)	OL — Spr (Note 4)			25	ns
t _{PZL}	Output enable time to low-level and high-level	C ₁ = 50pF (Note 4)			35	ns
t _{PZH}	(OE − Q _A ~Q _H)	OL — SUPP (NOIG 4)			35	ns

8-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER WITH 3-STATE PARALLEL OUTPUTS

SWITCHING CHARACTERISTICS ($V_{cc} = 2\sim 6V$, $T_a = -40\sim +85\%$)

						Limits		1	1
Symbol	Parameter	Test conditions			25℃			+85℃	Unit
			V _{CC} (V)	Min	Тур	Max	Min	Max	<u> </u>
		·	2.0	5	Į.		4		1
max	Maximum clock frequency		4.5	25 ·	1		20	}	МН
			6.0	29			23		
		,	2.0		1	60		75	İ
t _{TÉH}	Low-level to high-level and	•	4.5			12		15	ns
	high-level to low-level		6.0			10		13	1
	nign-level to low-level		2.0			60		75	
t _{THL}	output transition time		4.5			12		15	ns
			6.0			10		13	
			2.0		1	170		210	
t _{PLH}	Low-level to high-level and	•	4.5			38		48	ns
	high-level to low-level		6.0			35		44	1
	output propagation time	C _L = 50pF (Note 4)	2.0		 	170		210	†
t _{PHL}	(CK - Q'A, Q'H)		4.5			38		48	ns
·FILE			6.0			35		44	
	High-level to low-level		2.0		 	200		250	
t _{PHL}	output propagation time		4.5			44		55	ns
PHL	(RD - Q'A, Q'H)		6.0	Į	ļ	38		46	"
	(ND GA, GH)		2.0		 	170		210	+
			4.5			38	ļ	48	ns
t _{PHL}			6.0		1	35		44	113
	-			 	 				+
			2.0			170		210	
t _{PHL}	Low-level to high-level and		4.5	ĺ		38		48	ns
	high-level to low-level		6.0		 	35		44	
	output propagation time		2.0			206		260	
t _{PLH}	(CK - QA~QH)		4.5		Ì	46		57	ns
	_}	C _L = 150pF (Note 4)	6.0		ļ	39		49	ļ
			2.0		1	206]	260	
t _{PHL}			4.5			46	ĺ	57	ns
			6.0	<u> </u>		39		49	
		1	2.0]	1	200		250	1
	High-level to low-level	$C_L = 50 pF (Note 4)$	4.5	1	1	44		55	ns
	output propagation time	·	6.0	l		38		46	
t _{PHL}			2. 0			236		295	
	$(\overline{R_D} - Q_A \sim Q_H)$	C _L = 150pF (Note 4)	4.5	İ	İ	52		65	ns
			6.0	1	1	46	1	57	1
,			2.0			160		200	
t _{PLZ}	Output disable time from		4.5	1	}	32		40	ns
			6.0			28		34	
	low-level and high-level	\	2.0	1		160		200	T
t _{PHZ}	(OE − Q _A ~Q _H)		4.5			33		40	ns
· · · -			6.0	1	}	28	1	34	
		C _L = 50pF (Note 4)	2.0	†	 	160		200	1
t _{PZL}	Output enable time to		4.5			32		40	ns
-F2L			6.0			28		34	'''
	low-level and high-level	·	2.0	-	+	160	 	200	+
t	(OE - QA~QH)	·	4.5	1		32	1	40	ns
t _{PZH}	(OE WATER)		1			1	1	1 .	l us
	1		6.0	l		28		34	.L.



8-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER WITH 3-STATE PARALLEL OUTPUTS

SWITCHING CHARACTERISTICS $(V_{CC} = 2\sim 6V, T_a = -40\sim +85^{\circ}C)$ (Continued)

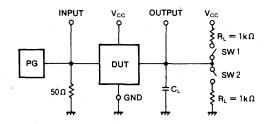
					Limits						
Symbol	Parameter	Test conditions	!		25℃		-40~	+85°C	Unit		
			V _{cc} (V)	Min	Тур	Max	Min	Max			
			2.0			220		275			
t _{PZL}	Output enable time to		4.5			44		55	ns		
	law laws tand bish tawat) — 150-F (N-4- 4)	6.0			37		47	-		
	low-level and high-level	C _L = 150pF (Note 4)	2.0			220		275			
t _{PZH}	(OE - QA, QH)		4.5			44		55	ns		
		·	6.0			37		47			
C,	Input capacitance					10		10	pF		
Co	Off-state output capacitance	OE=V _{CC}							pF		
CPD	Power dissipation capacitance (Note 3)								pF		

Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula: $P_{D} = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS ($V_{cc} = 2\sim6V$, $T_a = -40\sim+85^{\circ}C$)

						Limits			
Symbol	Parameter	Test conditions			25℃		−40 ~	+85℃	Unit
		·	V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0	100			125		
tw	CK, RD pulse width		4.5	20	İ		25		ns
*)		6.0	17		ļ	21		J
	0 0 1 1	1	2.0	100			125		
tsu	S _A , S _H setup time with		4.5	20		·	25		ns
	respect to CK		6.0	17		ŀ	21		
	0.0.1.1.1	7	2.0	5			5		
th	S _A , S _H hold time with		4.5	5			5		ns
	respect to CK		6.0	5			5		
		1	2.0	10			10		
trec	R _D recovery time with		4, 5	10	1		10	1	ns
	respect to CK		6.0	10			10		

Note 4: Test Circuit

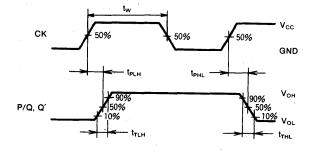


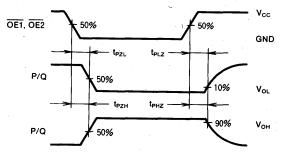
Parameter	SW 1	SW 2
t _{TLH} , t _{THL} t _{PLH} , t _{PHL}	Open	Open
t _{PLZ}	Closed	Open
t _{PHZ}	Open	Closed
t _{PZL}	Closed	Open
t _{PZH}	Open	Closed

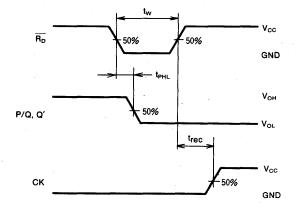
- (1) The pulse generator (PG) has the following characteristics (10% \sim 90%): $t_{\rm f}$ = 6ns, $t_{\rm f}$ = 6ns
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

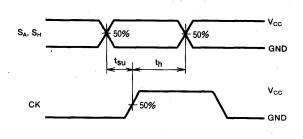
8-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER WITH 3-STATE PARALLEL OUTPUTS

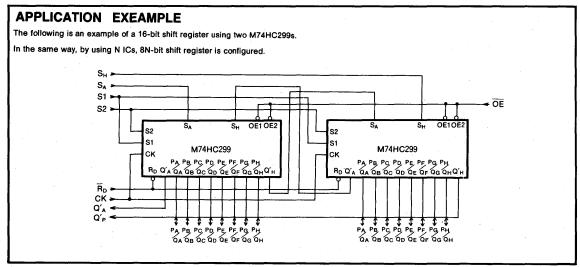
TIMING DIAGRAM











MITSUBISHI HIGH SPEED CMOS

M74HC323P/FP/DWP

8-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER WITH 3-STATE PARALLEL OUTPUTS

DESCRIPTION

The M74HC323 is a semiconductor integrated circuit consisting of an 8-bit serial/parallel-input, serial/parallel-output shift register with 3-state outputs and a synchronous reset input.

FEATURES

- High speed: 40MHz clock frequency typ.
 (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: Ta=-40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC323 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS323.

Use of mode select inputs S1 and S2 allows the device to operate in the following modes.

- (1) Parallel read S1="H" S2="H"
- (2) Right shift S1="H" S2="L"
- (3) Left shift S1="L" S2="H"
- (4) Clock inhibit S1="L" S2="L"

In the parallel data-read mode, 8-bit parallel data applied at parallel data I/O pins $P_A/Q_A \sim P_H/Q_H$ will be stored in the flip flops when the clock input CK changes from low-level to high-level. In the right-shift mode, serial data applied at serial data input S_A will be right-shifted from P_A/Q_A to P_H/Q_A

CONFIGURATION (TOP VIEW) MODE SELECT V_{CC} MODE SELECT - S2 19 OUTPUT INPUT ENABLE INPUTS SERIAL DATA OE2 → 3 18 - S_H SERIAL DATA OUTPUT PG OG → Q′_н $P_G/Q_G \leftrightarrow \boxed{4}$ PE PH 16 ↔ P_H/Q_H GE GF DATA INPUTS OUTPUTS PARALLEL DATA PÇ, ↔ P_F/Q_F ác áf PA PD $P_A/Q_A \leftrightarrow 7$ P_D/Q_D OUTPUTS SERIAL DATA OUTPUT Q'_A ← 8 13 ++ P_B/Q_B Q'A R → 9 12 ← CK CLOCK INPUT RESET INPUT SERIAL DATA 11 ← S_A GND 10 20P4 Outline 20P2N 20P2V

 Q_H by one bit each time the clock input CK changes from low-level to high-level. In the left-shift mode, serial data applied at serial data input S_H will be left-shifted from P_H/Q_H to P_A/Q_A by one bit each time the clock input CK changes from low-level to high-level.

In the clock inhibit mode, the clock pulse input is suppressed at each flip flop and the state of flip flop will not change and the previous states of the flip flops will be maintained. When $\overline{\text{OE1}}$ or $\overline{\text{OE2}}$ is high, $P_A/Q_A \sim P_H/Q_H$ will become the high-impedance state Z. Changing $\overline{\text{OE1}}$ or $\overline{\text{OE2}}$ will not affect the contents of the flip flops.

When reset input \overline{R} is low and CK changes from low-level to high-level, all flip flops will become low.

Serial data output $\mathbf{Q'}_{\mathbf{A}}$ and $\mathbf{Q'}_{\mathbf{H}}$ are used to extend the number of bits.

FUNCTION TABLE (Note 1)

Operation made				Inp	uts						Pa	arallel	data I	0			Serial da	ta outputs
Operation mode	R	СК	S1	S2	SA	S _H	OE1	OE2	P _A /Q _A	P _B /Q _B	P _C /Q _C	P_D/Q_D	P _E /Q _E	P _F /Q _F	P _G /Q _G	P _H /Q _H	Q'A	à
Reset	L	1	L	X	Х	Х	L	L	L	L	L	L	L	L	L	L	L	L
neset	L	†	Х	L	Х	Х	L	٦	L	L	L	L	L	L	L	L	L	٦
Dight shift	Н	†	Н	L	L	Х	L	L	L	Q _A ⁰	Q _B ^o	Qcº	Q₀°	Q _E ⁰	Q _E ⁰	Q _G ⁰	L	Q _G ⁰
Right shift	Н	†	н	L	Н	Х	L	L	H	Q _A ⁰	Q _B °	Q _C ⁰	Qpo	Q _E ⁰	Q _F ⁰	Q _G ⁰	Н	Q _G °
Left shift	Η.	†	L	Н	х	L	L	L	Q _B 0	Qc°	Q _D ⁰	Q _E ⁰	Q _F ⁰	Q _G ⁰	Q _H ⁰	· L	Q _B ⁰	L
Left Shift	Н	†	L	Н	х	٠Н	L	L	Q _B ⁰	Qcº	Q _D °	Q _E ⁰	Q _F ⁰	Q _G ⁰	Q _H ^o	н	Q _B ⁰	Н
Parallel read	Н	1	H	Н	х	х	L	L	PA	Рв	Pc	PD	PE	PF	PG	Рн	PA	Рн
Clock inhibit	Н	Х	L	L	Х	Х	L	L	Q _A ⁰	Q _B ^o	Q _C ⁰	Q_D^0	Q _E ⁰	Q _F ⁰	Q _G °	QHO	Q _A ^O	Q _H ^o
Clock inhibit	Н	L	Х	Х	Х	Х	L	L	Q _A ⁰	Q _B ⁰	Q _C ⁰	Q_D^0	Q _E ⁰	Q _F ⁰	Q _G ⁰	Q _H ⁰	Q _A ⁰	Q _H °
Output disable	Х	Х	х	Х	Х	х	Н	L	z	Z	Z	Z	Z	Z	Z	Z	Q _A ⁰	Q _H ⁰
P _A /Q _A ~P _H /Q _H are the high-	Х	Х	Х	Х	х	. X	L	Н	Z	z	Z	Z	Z	Z	Z	.Z	Q _A ⁰	Q _H °
impedance state.	Х	х	X	Х	Х	Х	н	Н	Z	Z	Z	Z	Z	Z	Z	Z	Q _A ⁰	Q _H °

Note 1: Qnº: Output state before input conditions are set.

X : Irrelevant

† : Change from low to high-level (positive-edge trigger)

Pn : $P_A/Q_A \sim P_H/Q_H$ operate as inputs. Q'_A and Q'_H are in the same state as P_A and P_H .

Z: High-impedance state. The flip flops are held in the same state as before PA/QA-PH/QH become the high-impedance state.



M74HC354P/FP/DWP

8-INPUT DATA SELECTOR/MULTIPLEXER
WITH DATA AND ADDRESS LATCHES AND WITH 3-STATE OUTPUTS

DESCRIPTION

The M74HC354 is a semiconductor integrated circuit consisting of an 8-line to 1-line date selector/multiplexer with 3-state outputs.

FEATURES

- High-speed: 32ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max
 (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85°C
- 3-state outputs

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

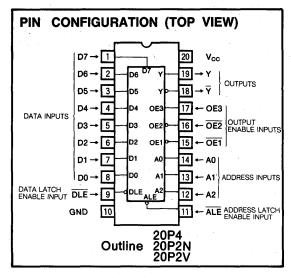
Use of silicon gate technology allows the M74HC354 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS354.

The M74HC354 consists of a circuit containing data selector function for selecting one of eight input line signals and multiplexer function for converting 8-bit parallel date into serial data using time-division.

The 8-line signals are applied to data inputs D0 through D7, and after one of the data inputs has been selected by address input A0, A1 and A2, it is output at pin Y, and the inverted signal is output at pin \overline{Y} .

By applying 8-bit parallel data to D0 through D7, and connecting the output of an octal synchronous counter to A0, A1 and A2, parallel data will be output at Y synchronous with the clock pulse in the order D0 through D7.

When the data latach-eanble input \overline{DLE} is low, the input data is stored in the data latch. When address latch-enable input \overline{ALE} is low, the address data is stored in the address latch. When the output-enable input $\overline{OE1}$, $\overline{OE2}$ is high or OE3 is low, then Y and \overline{Y} will become high impedance state, irrespective of other inputs.



FUNCTION TABLE (Note 1)

			Inputs				Oùt	puts
A2	A1	AO	DLE	OE1	OE2	OE3	Ÿ	Ÿ
X	X	X	X	н	×	×	Z	Z
· x ·	X	×	X.	×	Н.	×	z	z
X	×	×	' X	х	×	L	z	z
L	L	L	н	L	L	н	D0	DO
L	L	н	н	L	L	н	D1	D1
L	н	L	н	L	L	'H	D2	D2
Ĺ	н	н	Н.	L	L	Н .	D3	D3
Н	L	L	н	L	L	Н	D4	D4
H H	L	H.	Н	L	L	Н	D5	D5
Н	н	L	н	L.	L '	н	D6	D6
Н	Н	н	н	L	L	Н	D7	D7
L	L	L	L	L	L	H	D0n	D0n
L	Ŀ	• н	L	L	L	н .	D1n	D1n
L	. н	L	L	L	L	Н	D2n	D2n
L	Н,	н	L	L.	L	н	D3n	D3n
,H	L	L	L	L	L	н	D4n	D4n
н	L	н	L	L	L	Н	D5n	D5n
Н	н	L	L	L	L	н	D6n	D6n
н	н	н	L	L	L	н	D7n	D7n

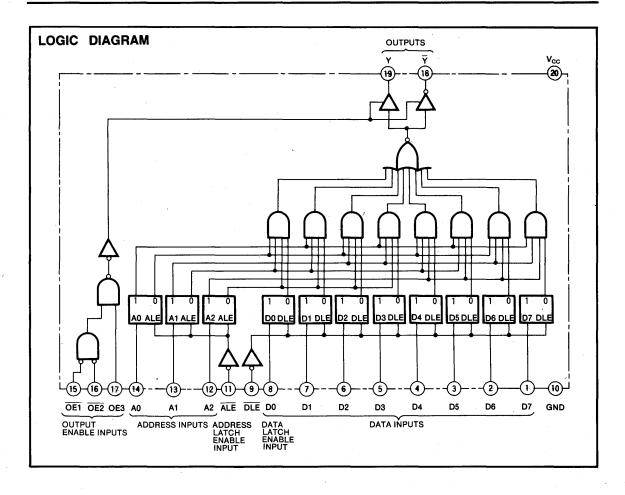
Note 1 : X

Irrelevant

Z : High impedance

D0n~D7n: Data inputs before DLE is changed to low

8-INPUT DATA SELECTOR/MULTIPLEXER WITH DATA AND ADDRESS LATCHES AND WITH 3-STATE OUTPUTS



ABSOLUTE MAXIMUM RATINGS $(\tau_a = -40 \sim +85^{\circ}C)$, unless otherwise noted)

Symbol	Parameter	Test conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	· v
•		V ₁ < 0V	-20	
lik .	Input protection diode current	V _I > V _{CC}	20	mA.
		V ₀ < 0V	-20	
ок	Output parasitic diode current	$V_0 > V_{CC}$	20	mA.
lo	Output current per output pin		±35	mA
Icc	Supply/GND current	V _{CC} , GND	±75	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65~ + 150	ొ

Note 2 : M74HC354FP, T $_a=-40\sim+75^\circ$ C and T $_a=75\sim85^\circ$ C are derated at -7mW/°C. M74HC354DWP, T $_a=-40\sim+80^\circ$ C and T $_a=80\sim85^\circ$ C are derated at -7mW/°C.

8-INPUT DATA SELECTOR/MULTIPLEXER WITH DATA AND ADDRESS LATCHES AND WITH 3-STATE OUTPUTS

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85 \text{ C})$

Symbol	Day		Limits				
Symbol	rai	rameter	Min	Тур	Max	Unit	
Vcc	Supply voltage		2		6	٧	
Vı	input voltage		0		Vcc	٧	
Vo	Output voltage		0		Vcc	٧	
T _{opr}	Operating temperature ra	inge .	-40		+85	Ç	
		$V_{CC} = 2.0V$	0		1000		
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns	
		$V_{CC} = 6.0V$	0		400		

ELECTRICAL CHARACTERISTICS

	*		.)		Limits					
Symbol	Parameter	Test	conditions		25℃			-40~+85°C		Unit
		V _{cc} (V)		Min	Тур	Max	Min	Max	1	
		V = 0.1V V	0.114	2.0	1.5			1.5		
V _{IH}	High-level input voltage	$V_0 = 0.1V, V_{CC}$	$= 0.1 \text{ V}, \text{ V}_{CC} = 0.1 \text{ V}$ = $20 \mu \text{A}$		3. 15	1		3.15		V
		$ 1_0 = 20\mu A$		6.0	4. 2	1		4.2		1
		V = 0.1V V					0.5		0.5	
VIL	Low-level input voltage	$V_0 = 0.1V, V_{CC}$	5U. IV	4. 5			1.35		1.35	V
		$ I_0 = 20\mu A$	$=20\mu$ A				1.8	}	1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
			$I_{OH} = -20\mu A$	4.5	4.4			4.4		
V _{OH}	High-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		V
			$I_{OH} = -6.0 \text{mA}$	4. 5	4. 18			4.13		
			$I_{OH} = -7.8 \text{mA}$	6.0	5. 68			5.63		
			$I_{OL} = 20 \mu A$	2.0			0.1	, .	0.1	
			$I_{OL} = 20 \mu A$	4.5			0.1		0.1	
VoL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0	,		0.1		0.1	V
			$I_{OL} = 6.0 \text{mA}$	4.5			0.26		0.33	{
			I _{OL} = 7.8mA	6.0			0. 26		0.33	
t _{IH}	High-level input current	$V_i = 6V$		6.0			0.1		1.0	μA
l _I L	Low-level input current	V ₁ = 0V		6.0			0.1		-1.0	μA
l _{ozh}	Off-state high-level output current	$V_i = V_{iH}, \ V_{iL},$	$V_0 = V_{CC}$	6.0			0.5		5. 0	μA
lozL	Off-state low-leveloutput current	$V_i = V_{iH}, V_{iL},$	$V_i = V_{iH}, \ V_{iL}, \ V_O = GND$				-0.5		-5.0	μA
Icc	Quiescent supply current	VI = VCC, GND	$I_0 = 0\mu A$	6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS ($V_{cc} = 5V$, $T_a = 25^{\circ}C$)

0	B	TAdistant		Unit		
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time				10	ns
t _{PLH}	Low-level to high-level and high-level to low-level				46	ns
t _{PHL}	output propagation time (D $-$ Y, \overline{Y})				46	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C ₁ = 50pF (Note 4)			53	ns
t _{PHL}	output propagation time (DLE - Y, Y)	CL = 50pr (Note 4)			53	ns
t _{PLH}	Low-level to high-level and high-level to low-level				56	ns
t _{PHL}	output propagation time $(A - Y, \overline{Y})$				56	ns
t _{PLH}	Low-level to high-level and high-level to low-level				58	ns
t _{PHL}	output propagation time (ALE - Y, Y)				58	ns
t _{PLZ}	Output disable time from low-level and high-level	$C_1 = 5 pF (Note 4)$			32	ns
t _{PHZ}	(OE, OE − Y, Y)	OL — 5 pr (Note 4)			32	ns
t _{PZL}	Output enable time to low-level and high-level	C ₁ = 50pF (Note 4)			24	ns
t _{PZH}	$(OE, \overline{OE} - Y, \overline{Y})$	C _L = 50pF (Note 4)			24	ns

MT4HC354P/FP/DWP

8-INPUT DATA SELECTOR/MULTIPLEXER WITH DATA AND ADDRESS LATCHES AND WITH 3-STATE OUTPUTS

SWITCHING CHARACTERISTICS $(V_{cc} = 2\sim6V, T_a = -40\sim+85^{\circ}C)$

						Limits			
Symbol	Parameter	Test conditions			25℃		-40~	+85℃	Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0			60		75	
t _{TLH}	Low-level to high-level and		4.5			12		15	กร
	high tourist tourist	0 = 50=5 (N=4=4)	6.0			10		13	
	high-level to low-level	$C_L = 50 pF \text{ (Note 4)}$	2.0			60		75	
t _{THL}	output transition time		4.5		1	12		15	ns
			6.0			10		13	
			2.0			235		294	
t _{PLH}			4.5			47	ĺ	. 59	ns
TEN			6.0			40		50	
		C _L = 50pF (Note 4)	2.0			235		294	
t _{PHL}	Low-level to high-level and		4.5			47		59	ns
PHL	high-level to low-level		6.0			40		50	
	output propagation time		2.0		-	275		344	
• .	$(D-Y, \overline{Y})$,	4.5			55		68	ns
t _{PLH}	(6 1, 1)				1	46		58	1115
		C _L = 150pF (Note 4)	6.0						-
			2.0	,		275		344	
t _{PHL}			4.5			55		68	ns
			6.0			46		58	
			2.0			270		337	
t _{PLH}			4.5		1	54		68	ns
		C _L = 50pF (Note 4)	6.0			46		58	
		OL = 30pr (Note 4)	2.0			270		337	,
t _{PHL}	Low-level to high-level and	1.	4.5	,		54		68	ns
	high-level to low-level		6.0			46		58 .	
	output propagation time		2.0			310		387	
t _{PLH}	(DLE - Y, Y)		4.5		İ	62		78	ns
			6.0			52		- 66	
		C _L = 150pF (Note 4)	2.0			310		357	
t _{PHL}			4.5			62		78	ns
THE			6.0			52		66	
			2.0			285		356	
+			4.5			57		71	ns
t _{PLH}			6.0			48		60	113
	-	C _L = 50pF (Note 4)						356	
	I am I am I am I am I am I		2.0		1	285		1	
t _{PHL}	Low-level to high-level and		4.5			57		71	ns
	high-level to low-level		6.0			48		60	
	output propagation time		2.0			325		406	
t _{PLH} .	$(A-Y, \overline{Y})$		4.5			65		81	ns
	4	C _L = 150pF (Note 4)	6.0		-	55		69	
			2.0			325		406	
t _{PHL}			4.5		1	65		81	ns
	15		6.0			55		69	
			2. 0			300		375	
t _{PLH}			4.5		1	60		75	ns
		C = 50p5 (Note 4)	6.0			51		64	L
		C _L = 50pF (Note 4)	2.0			300		375	
t _{PHL}	Low-level to high-level and		4.5			60		75	ns
	high-level to low-level		6.0			51		64	
×	output propagation time		2.0			340		425	
t _{PLH}	$(\overline{ALE} - Y, \overline{Y})$		4.5	1		68		85	ns
, e.,			6.0			58		72	,
	1	C _L = 150pF (Note 4)	2.0	-	1	340		425	
+		· ·			1			1	
t _{PHL}	and the second s		4.5			68		85	ns
	<u> L</u>	1	6.0	L	l	58	<u> </u>	72	1

8-INPUT DATA SELECTOR/MULTIPLEXER WITH DATA AND ADDRESS LATCHES AND WITH 3-STATE OUTPUTS

SWITCHING CHARACTERISTICS $(V_{cc} = 2\sim6V, T_a = -40\sim+85\%)$ (Continued)

						Limits]
Symbol	Parameter	Test conditions V _{CC} (V)			25℃			+85℃	Unit
				Min	Тур	Max	Min	Mex]
			2.0			165		206	
t _{PLZ}	Output disable time from		4.5			33		40	ns
	low-level and high-level	C _L = 50pF (Note 4)	6.0]	28		35	l
	low-level and high-level	CL = 50pr (Note 4)	2, 0			165		206	
t _{PHZ}	(OE, OE - Y, Y)	,	4.5	ľ		33		40	ns
			6.0			28		35	
			2.0			125		156	Ī
t _{PZL}	ļ.		4.5			25		31	ns
		0 - 50-5 (N-4-4)	6.0	,	į	21		26	
]	C _L = 50pF (Note 4)	2. 0			125		156	
t _{PZH}	Output enable time to low-level		4.5	1		25		31	ns
	and blab lavel		6.0			21		26	
	and high-level		2.0			165		206	T
t _{PZL}	$(OE, \overline{OE} - Y, \overline{Y})$		4.5	ļ	ĺ	33		41	กร
		0 - 150-5 (N-1-4)	6.0			28		35	
	1 .	C _L = 150pF (Note 4)	2. 0			165		206	
t _{PZH})		4. 5			33		41	ns
			6.0			28		35	
C _i	Input capacitance					10		10	pF
Co	Off-state output capacitance	OE = "H"				15		15	рF
C _{PD}	Power dissipation capacitance (Note 3)					1			pF

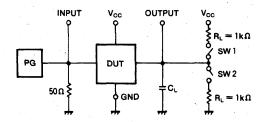
Note 3: CPD is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per flip flop) The power dissipated during operation under no-load conditions is calculated using the following formula:

 $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS ($v_{oc} = 2\sim6v$, $T_a = -40\sim+85$ °C)

	:				_,,-	Limits			
Symbol	Parameter	Test conditions			25℃		-40~	+85℃	Unit
		<u> </u>	V _{cc} (V)	Mìn	Тур	Max	Min	Max	
	Address lately smaller sylve sylvelik		2.0	80			100		
tw	Address latch enable pulse width		4.5	16	1		20		กร
	Data latch enable pulse width		6.0	15			18		
	Daniel March 18th annual Annual SUE		2.0	50	,		60		
t _{su}	D setup time with respect to DLE A setup time with respect to ALE		4.5	10			13	1	ns
ĺ	A setup time with respect to ALE		6.0	10		1	. 13	İ	
	SUE hald down the sub-		2.0	5.			5		
th	DLE hold time with respect to D		4.5	. 5			5		ns
	ALE hold time with respect to A		6.0	5			5		

Note 4: Test Circuit



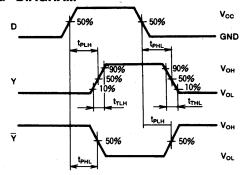
Parameter	SW 1	SW 2
t _{TLH} , t _{THL}	Open	Open
t _{PLZ}	Closed	Open
t _{PHZ}	Open	Closed
t _{PZL}	Closed	Open
t _{PŽH}	Open	Closed

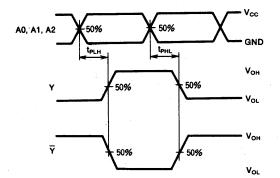
(1) The pulse generator (PG) has the following characteristics (10% \sim 90%): $t_f = 6$ ns, $t_f = 6$ ns (2) The capacitance C_L includes stray wiring

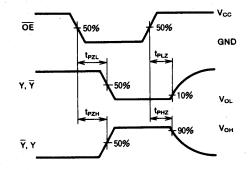
capacitance and the probe input capacitance.

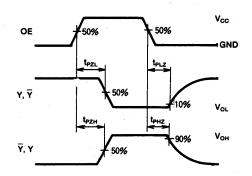
8-INPUT DATA SELECTOR/MULTIPLEXER WITH DATA AND ADDRESS LATCHES AND WITH 3-STATE OUTPUTS

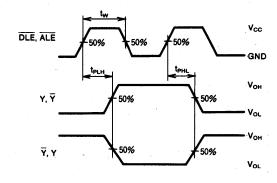
TIMING DIAGRAM

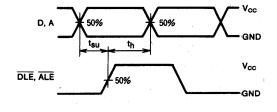












M74HC356P/FP/DWP

PRELIMINAR 8-INPUT DATA SELCTOR/MULTIPLEXER WITH DATA AND ADDRESS LATCHES AND WITH 3-STATE OUTPUTS

DESCRIPTION

The M74HC356 is a semiconductor integrated circuit consisting of an 8-line to 1line data selector/multiplexer with 3state outputs.

FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 35ns typ. ($C_L=50pF$, $V_{CC}=5V$)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2∼6V
- Wide operating temperature range: T_a=−40~+85°C
- 3-state outputs

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

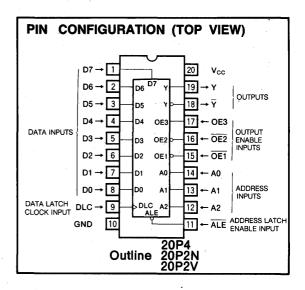
Use of silicon gate technology allows the M74HC356 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS356.

The M74HC356 consists of a circuit containing data selector function for selecting one of eight input line signals and multiplexer function for converting 8-bit parallel data into serial data using time-division.

The 8-line signals are applied to data inputs D0 and D7, and after one of the data inputs has been selected by address input A0, A1 and A2, it is output at pin Y, and the inverted signal is output at pin \overline{Y} .

By applying 8-bit parallel data to D0 through D7, and connecting the output of an octal synchronous counter to A0, A1 and A2, parallel data will be output at Y synchronous with the clock pulse in the order D0 through D7.

D0 through D7 all contain edge-triggered flip flops. Input data is sent to the data latch by the rising edge of data latch clock DLC. The address data is stored in the address latch when the address latch enable input ALE is low. When the output enable input OE1, OE2 is high or OE3 is low then Y and \overline{Y} will become high impedance state irrespective of other inputs.



FUNCTION TABLE (Note 1)

			Inputs				Out	puts
A2	A1	A0	DLC	OE1	OE2	OE3	Y	Y
×	×	X	х	н	Χ.	, X	Z	z
×	· X	х	×	×	н	X	z	Z
×	х	×	X	х	X	L	z	Z
L	L	L	t	L	L	Н	D0n	D0n
L	L	н	t t	L	L.	н	D1n	D1n
L	н	L	1	L	Ł	н	D2n	D2n
L	` н	н	†	L	L	н	D3n	D3n
H	L	L	1 1	L	L	н	D4n	D4n
н	L	н	†	L	L	н	D5n	D5n
н	н	L	1	L	L	н	D6n	D6n
н	H	Н	l t	L	L	н	D7n	D7n
L	L	L	×	L	· L	н	D0p	D0p
L	L,	н	x	L	L	н	D1p	D1p
L	н	L	×	L	L	н	D2p	D2p
L	н	н	×	L	L	н	Ð3p	D3p
н	L	L.	×	L	L	н	D4p	D4p
н	L	н	×	L	L	н	D5p	D5p
н	н	L	x	L L	L	Н	D6p	D6p
• н	н	н	х	L	L	H	D7p	D7p

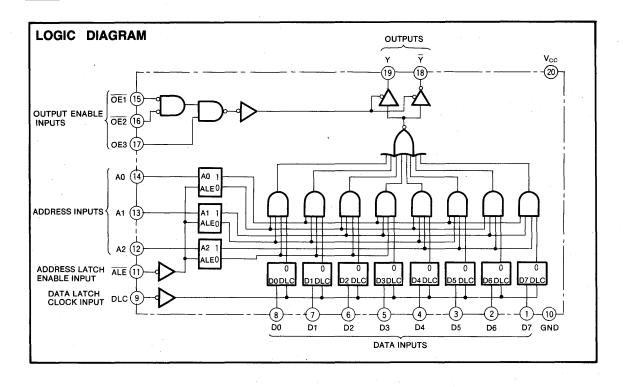
Note 1: : Irrelevant

High impedance

: Each data input D at the rise of DLC

Dp : Each data input D at the rise of previous DLC

8-INPUT DATA SELCTOR/MULTIPLEXER WITH DATA AND ADDRESS LATCHES AND WITH 3-STATE OUTPUTS



ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85$ °C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	. V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
		V ₁ < 0V	-20	
lik	Input protection diode current	V _I > V _{CC}	20	mA.
		V _o < 0V	-20	
Іок	Output parasitic diode current	$V_0 > V_{CC}$	20	mA
lo .	Output current, per output pin		±35	mA
Icc	Supply/GND current	V _{CC} , GND	±75	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65~+150	°C

Note 2 : M74HC356FP, T $_a$ = $-40\sim+75$ °C and T $_a$ = $75\sim85$ °C are derated at -7mW/°C. M74HC356DWP, T $_a$ = $-40\sim+80$ °C and T $_a$ = $80\sim85$ °C are derated at -7mW/°C.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85 ^{\circ}C)$

0 1 1			Unit				
Symbol	Par	ameter	Min	Тур	Max	Oint	
Vcc	Supply voltage		2		6	٧	
Vı	Input voltage		. 0		Vcc	٧	
Vo	Output voltage		0		Vcc	٧	
Topr	Operating temperature ra	inge	-40		+85	Ç	
P-		V _{CC} = 2.0V	0		1000	,	
tr, tf	input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns	
		$V_{CC} = 6.0V$	0		400		

8-INPUT DATA SELCTOR/MULTIPLEXER WITH DATA AND ADDRESS LATCHES AND WITH 3-STATE OUTPUTS

ELECTRICAL CHARACTERISTICS

	;						Limits			
Symbol	Parameter	Test conditions $V_{cc}(V)$		25℃			-40~+85℃		Unit	
				V _{cc} (V)	Min	Тур	Max	Min	Max	
		V = 0.1V V	_0.1V	2.0	1.5			1.5	-	
V _{IH}	High-level input voltage	$V_0 = 0.1V, V_{CC} - 0.1V$ $ I_0 = 20\mu A$		4.5	3. 15			3.15		v
		1161 — 20μΑ		6.0	4.2			4.2		
		V = 0.1V V	_0 tv	2.0			0.5		0.5	
VIL	Low-level input voltage *	$V_0 = 0.1V, V_{CC} - 0.1V$		4.5		l	1.35		1.35	V
		$ I_0 = 20\mu A$		6.0			1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
		$V_i = V_{iH}, \ V_{iL}$	$I_{OH} = -20\mu A$	4.5	.4.4			4.4		v
VoH	High-level output voltage		$I_{OH} = -20\mu A$	6.0	5.9			5.9		
			$I_{OH} = -6.0 \text{mA}$	4.5	4. 18			4.13		
			$I_{OH} = -7.8 mA$	6.0	5. 68			5, 63		
	."		$I_{OL} = 20 \mu A$	2.0	,		0.1		0.1	
			$I_{OL} = 20 \mu A$	4.5		1	0.1		0.1	
VoL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0. 1	V .
			I _{OL} = 6.0mA	4.5			0. 26		0.33	
			$I_{OL} = 7.8 \text{mA}$	6.0			0. 26		0.33	ı
l _{IH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μА
՝ կլ	Low-level input current	$V_i = 0V$		6.0			-0.1		-1.0	μΑ
l _{ozh}	Off-state high-level output current	$V_{i} = V_{iH}, V_{iL}, V_{iL}$	$V_0 = V_{CC}$	6.0			0.5		5.0	μA
l _{ozL}	Off-state low-level output current	$V_i = V_{iH}, \ V_{iL}, \ V_{iL}$	o = GND	6.0			-0.5		-5.0	μΛ
Icc	Quiescent supply current	$V_1 = V_{CC}$, GND	$I_0 = 0\mu A$	6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS ($v_{cc} = 5v$, $T_a = 25^{\circ}C$)

C	B	T-4	Limits			
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time				10′	ns
t _{PLH}	Low-level to high-level and high-level to low-level				50	ns
t _{PHL}	output propagation time (DLC $-Y, \overline{Y}$)	$C_1 = 50 pF \text{ (Note 4)}$			50	ns
t _{PLH}	Low-level to high-level and high-level to low-level	CL — SUPP (Note 4)			56	ns
t _{PHL}	output propagation time $(A - Y, \overline{Y})$				56	ns
t _{PLH}	Low-level to high-level and high-level to low-level				58	ns
t _{PHL}	output propagation time ($\overline{ALE} - Y, \overline{Y}$)				58	ns
t _{PLZ}	Output disable time from low-level and high-level	$C_1 = 5 pF (Note 4)$			32	, ns
t _{PHZ}	$(OE, \overline{OE} - Y, \overline{Y})$	C _L — 5 pr (Note 4)			32	ns
t _{PZL}	Output enable time to low-level and high-level	$C_1 = 50pF (Note 4)$			24	ns
t _{PZH}	$(OE, \overline{OE} - Y, \overline{Y})$	CL — SUPP (NOTE 4)			24	ns

8-INPUT DATA SELCTOR/MULTIPLEXER WITH DATA AND ADDRESS LATCHES AND WITH 3-STATE OUTPUTS

SWITCHING CHARACTERISTICS $(v_{cc} = 2\sim6V, T_a = -40\sim+85^{\circ}C)$

		-		Limits 25°C −40~+85°C					
Symbol	Parameter	Test conditions		25℃					Unit
			V _{CC} (V)	Min	Тур	Max	Min	Max	
			2.0			60		75	1
t _{TLH}	Low-level to high-level and	*	4.5			12		15	ns
	high-level to low-level	C _L = 50pF (Note 4)	6.0			10		13	
		of sob. (moto i)	2.0			60		75	
t _{THL}	output transition time		4.5			12		15	ns
			6.0			10		13	
			2.0			225		318	
t _{PLH}			4.5			51		63	ns
		$C_L = 50pF (Note 4)$	6.0			43		53	
		CL — SOPF (Note 4)	2.0			225		318	-
t _{PHL}	Cultural disable time from		4.5	-		51		63	ns
	Output disable time from		6.0			43		53	
	low-level and high-level		2.0			295		369	
t _{PLH}	$(DLC - Y, \overline{Y})$		4.5			59		73	ns
			6.0			50		63	
	1	C _L = 150pF (Note 4)	2.0			295		369	
t _{PHL}			4.5			59		73	ns
THE			6.0			50		63	
			2.0			285		356	
t _{PLH}			4.5			57		71	ns
'PLH			6.0			48		60	
	1	C _L = 50pF (Note 4)	2.0			235		356	ļ —
•			4.5			57		71	ns
t _{PHL} Output enable time to lov	Output enable time to low-level		6.0			48		60	l iis
	and high-level		2.0			325		406	
	$(A-Y,\overline{Y})$	·	4.5			65		81	
t _{PLH}			1 1			1			ns
	4	C _L = 150pF (Note 4)	6.0			55		69	
			2.0			325		406	
t _{PHL}			4.5			65		81	ns
			6.0			55	-	69	<u> </u>
			2.0			300		375	
t _{PLH}			4.5			60		75	ns
		C _L = 50pF (Note 4)	6.0			51		64	
			2.0			300		375	
t _{PHL}	Low-level to high-level and		4.5			60		75	ns
	high-level to low-level		6.0			51		64	
	output propagation time		2.0			340		425	
t _{PLH}	(ALE - Y, Y)	ř.	4.5	l		68		85	ns
		C _L = 150pF (Note 4)	6.0			58		72	
		OL - 150pr (Note 4)	2.0			340		425	
t _{PHL}	·		4.5	j		68		85	ns
	<u> </u>		6.0			58		72	L .
			2.0			165	11	206	
t _{PLZ}	Output disable time from		4.5			33		41	ns
		*	6.0			28		35	
	low-level and high-level	$C_L = 50 pF (Note 4)$	2.0			165		206	
									t
t _{PHZ}	$(OE, \overline{OE} - Y, \overline{Y})$		4.5			33		41	ns

8-INPUT DATA SELCTOR/MULTIPLEXER WITH DATA AND ADDRESS LATCHES AND WITH 3-STATE OUTPUTS

SWITCHING CHARACTERISTICS $(V_{cc} = 2\sim 6V, T_a = -40\sim +85\%)$ (Continue)

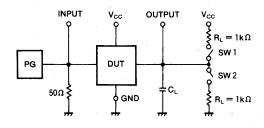
						Limits			
Symbol	Parameter	Test conditions		25℃			-40~+85°C		Ünit
			V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0			125		156	
tezL	1		4.5			25		. 31	ns
		C _L = 50pF (Note 4)	6.0		1	21		26	
]		2.0			125		156	
t _{PZH}	Output enable time to low-level		4.5		ŀ	25		31	ns
			6.0			21		26	
	and high-level	C _L = 150pF (Note 4)	2.0			165		206	
t _{PZL}	(OE, OE - Y, Y)		4.5			33	-	41	ns
			6.0			28		35	
	5 ·		2.0			165		206	
t _{PZH}			4.5			33		41	ns
			6.0			28		35	
Cı	Input capacitance					10		10	pF
Со	Off-state output capacitance	OE = V _{CC}				15		15	pF
C _{PD}	Power dissipation capacitance (Note 3)								рF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per flip flop). The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS ($V_{cc} = 2\sim 6V$, $T_a = -40\sim +85^{\circ}C$)

					Limits				
Symbol	Parameter	Test conditions		25℃			-40~+85℃		Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	
	Address latch anable pulse width		2.0	80			100		
tw	Address latch enable pulse width		4.5	16			20		ns
Data laten clock	Data latch clock pulse width		6.0	15			18		
	Destructions with respect to DLC		2.0	50			50		
t _{su}	tsu D setup time with respect to DLC A setup time with respect to ALE		4.5	10			10		ns
			6.0	10			10		
	DLC hold time with respect to D		2.0	5			5		
th	ALE hold time with respect to A		4.5	5			5		ns
	ALE hold time with respect to A		6.0	5			5		





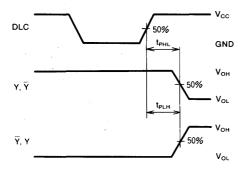
Parameter	SW 1	SW 2
t _{TLH} , t _{THL} t _{PLH} , t _{PHL}	Open	Open
t _{PLZ}	Closed	Open
t _{PHZ}	Open	Closed
t _{PZL}	Closed	Open
t _{PZH}	Open	Closed

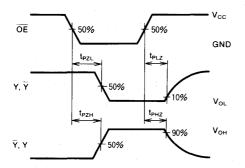
(1) The pulse generator (PG) has the following characteristics (10% \sim 90%): t_f = 6ns, t_f = 6ns

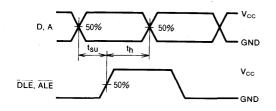
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

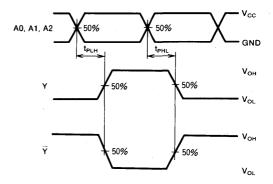
8-INPUT DATA SELCTOR/MULTIPLEXER WITH DATA AND ADDRESS LATCHES AND WITH 3-STATE OUTPUTS

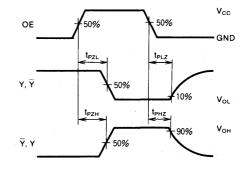
TIMING DIAGRAM

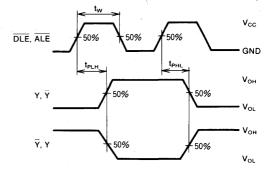












M74HC365P/FP/DP

HEX 3-STATE NONINVERTING BUFFER WITH COMMON ENABLES

DESCRIPTION

The M74HC365 is a semiconductor integrated circuit consisting of six buffers with 3-state noninverted outputs and common enable inputs.

FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 10ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=-40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

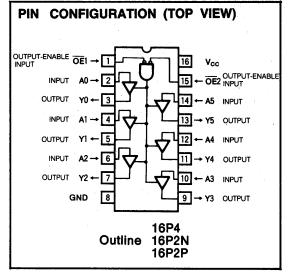
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC365 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS365.

The M74HC365 consists of six 3-state buffers with outputenable inputs common to all circuits.

When output-enable inputs $\overline{OE}1$ and $\overline{OE}2$ are both low, outputs Y will become enable state. If input A is high, a high-level signal will be output to Y and if input A is low, a low-level signale will be output to Y.

When at least one of input $\overline{OE}1$ or $\overline{OE}2$ is high, Y will be-



come high-impedance state.

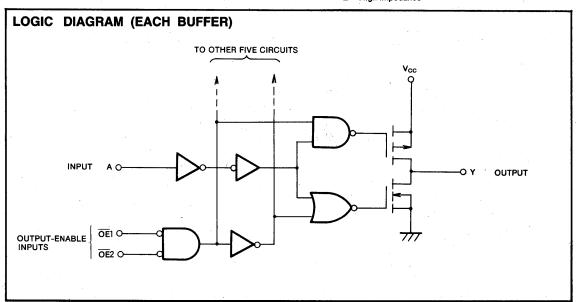
A version of the M74HC356 with an inverted output, the M74HC366 is also available.

FUNCTION TABLE (Note 1)

	Inputs		Output
OE1	OE2	Α	Y
L	L	L	L
L	L	Н	Н
Н	×	X	Z
X	н	X	Z

Note 1: X: Irrelevant

Z : High impedance



HEX 3-STATE NONINVERTING BUFFER WITH COMMON ENABLES

ABSOLUTE MAXIMUM RATINGS ($\tau_a = -40 \sim +85$ °C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage	• • •	-0.5~+7.0	V
V _i	Input voltage	·	-0.5~V _{cc} +0.5	V .
Vo	Output voltage		-0.5~V _{cc} +0.5	V
,	1	V ₁ < 0V	-20	
lik	Input protection diode current	V _I > V _{CC}	20	mA
	0.1.1.1	V ₀ < 0V	-20	
lok	Output parasitic diode current	Vo > Vcc	20	mA
lo	Output cuurent per output pin		±35	mA
Icc	Supply/GND current	V _{CC} , GND	±75	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65~+150	င

Note 2 : M74HC365FP, T $_a$ = $-40\sim+70$ °C and T $_a$ = $70\sim85$ °C are derated at -6mW/°C M74HC365DP, T $_a$ = $-40\sim+50$ °C and T $_a$ = $50\sim85$ °C are derated at -5mW/°C

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85 \degree C)$

0		Parameter		Limits					
Symbol	Pa	rameter	Min	Тур	Max	Unit			
V _{CC}	Supply voltage		2		6				
Vi	Input voltage		0		Vcc	V			
Vo	Output voltage		0		Vcc	V			
Topr	Operating temperature ra	ange	-40		+85	င			
		$V_{CC} = 2.0V$	0		1000				
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns			
	V _{CC} = 6.0V		0		400				

ELECTRICAL CHARACTERISTICS

					,		Limits			
Symbol	Parameter	Test	conditions			25℃		-40~	+85°C	Unit
				V _{cc} (V)	Min	Тур	ax	Min	Max	
ViH	High-level input voltage	$V_0 = V_{CC} - 0.1$ $ I_0 = 20\mu A$			1. 5 3. 15 4. 2			1.5 3.15 4.2		v
V _{IL}	Low-level input voltage	$V_0 = 0.1V, V_0$ $ I_0 = 20\mu A$	e-0.1V	6. 0 2. 0 4. 5 6. 0			0.5 1.35 1.8		0.5 1.35 1.8	v
V _{он}	High-level output voltage	$V_{I} = V_{IH}, \ V_{IL}$	$I_{OH} = -20\mu A$ $I_{OH} = -20\mu A$ $I_{OH} = -20\mu A$ $I_{OH} = -6.0 mA$ $I_{OH} = -7.8 mA$	2. 0 4. 5 6. 0 4. 5 6. 0	1. 9 4. 4 5. 9 4. 18 5. 68	-		1. 9 4. 4 5. 9 4. 13 5. 63		v
V _{OL}	Low-level output voltage	$V_l = V_{lL}$	$I_{OL} = 20 \mu A$ $I_{OL} = 20 \mu A$ $I_{OL} = 20 \mu A$ $I_{OL} = 6.0 mA$ $I_{OL} = 7.8 mA$	2. 0 4. 5 6. 0 4. 5 6. 0			0. 1 0. 1 0. 1 0. 26 0. 26		0. 1 0. 1 0. 1 0. 33 0. 33	v
I _{IH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μΑ
l _{IL}	Low-level input current	$V_1 = 0V$		6.0			-0.1		-1.0	μΑ
огн	Off-state high-level output current	$V_I = V_{IH}, \ V_{iL},$	$V_I = V_{IH}, \ V_{tL}, \ V_O = V_{CC}$				0.5		5.0	μΑ
lozL	Off-state low-level output current	$V_{I} = V_{IH}, V_{IL},$	V _O = GND	6.0			-0.5		-5.0	μΑ
loc	Quiescent supply current	VI = VCC, GNE	$I_0 = 0 \mu A$	6.0			4.0		40.0	μΑ

HEX 3-STATE NONINVERTING BUFFER WITH COMMON ENABLES

SWITCHING CHARACTERISTICS (Voc = 5V, Ta = 25°C)

Symbol	Parameter	Test conditions		Limits				
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit		
tTLH	Low-level to high-level and high-level to low-level				10	ns		
t _{THL}	output transition time	C _L = 50pF (Note 4)			10	ns		
t _{PLH}	Low-level to high-level and high-level to low-level				22	ns		
t _{PHL}	output propagation time (A — Y)				22	ns		
t _{PLZ}	Output disable time from low-level and high-level	C = E = E (Note 4)			36	ns		
t _{PHZ}	(OE - Y)	C _L = 5 pF (Note 4)			36	ns		
t _{PZL}	Output enable time to low-level and high-level	C _L = 50pF (Note 4)			40	ns		
t _{PZH}	(OE – Y)	CL = SUPF (Note 4)			40	ns		

SWITCHING CHARACTERISTICS $(V_{cc} = 2\sim6V, T_a = -40\sim+85C)$

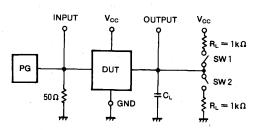
<u>.</u>	_				orto	Limits		1 0510	- I Init
Symbol	Parameter	Test conditions			25℃			+85℃	Unit
		<u> </u>	V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0			60		75	
t _{TLH}	Low-level to high-level and		4.5			12		15	ns
	high-level to low-level	C _L = 50pF (Note 4)	6.0		1	10		13	
	Ingli lovor to low-lovor	or sept (note t)	2.0			60	·	75	
t _{THL}	output transition time		4.5			12		-15	ns
			6.0			10		13	<u> </u>
			2.0			105		130	
t _{PLH}			4.5			24		30	ns
	· ·	C _L = 50pF (Note 4)	6.0	_		19		24	
		CL — Sopr (Note 4)	2.0			105		130	
t _{PHL}	Low-level to high-level and		4.5			24		30	ns
	high-level to low-level		6.0			19		24	
	output propagation time		2.0			135		168	
t _{PLH}	(A — Y)		4.5			29		36	ns
		C _L = 150pF (Note 4)	6.0			24		- 30	
	7	G _L = 150pF (Note 4)	2.0			135		168	
t _{PHL}			4.5			29		36	กร
	İ	6.0		ŀ	24		30	l	
			2.0	-	1	175		218	
t _{PLZ}	Output disable time from		4.5		1	44		55	ns
			6.0			37		46	
	low-level and high-level	C _L = 50pF (Note 4)	2, 0			175		218	
t _{PHZ}	(OE - Y)		4.5			44		55	ns
		, ·	6.0			37		46	
	`		2.0			230		287	
tezu			4.5			44		55	ns
			6.0			35		43	
	1	C _L = 50pF (Note 4)	2.0		· · · · · · · · · · · · · · · · · · ·	230		287	
t _{PZH}	Output enable time to		4.5		1	44		55	ns
			6.0			35		43	
	low-level and high-level		2.0			245		306	
t _{PZL}	(OE - Y)		4.5			53		66	ns
			6.0			41		51	"
	1	C _L = 150pF (Note 4)	2.0			245		306	
t _{PZH}			4.5			53		66	ns
- 40			6.0			41		51	
Cı	Input capacitance	<u> </u>				10		10	pF
Co	Off-state output capacitance	OE = V _{CC}			 	15	 	15	pF
C _{PD}	Power dissipation capacitance (Note 3)				49			1-15	pF

Note 3 : C_{DP} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per buffer)
The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$



HEX 3-STATE NONINVERTING BUFFER WITH COMMON ENABLES

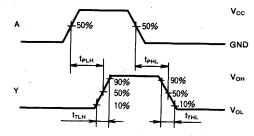
Note 4: Test Circuit

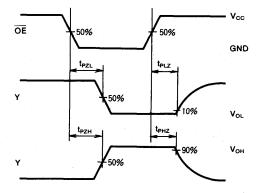


Parameter	SW 1	SW 2
t _{TLH} , t _{THL} t _{PLH} , t _{PHL}	Open	Open
t _{PLZ}	Closed	Open
t _{PHZ}	Open	Closed
t _{PZL}	Closed	Open
t _{PZH}	Open	Closed

(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
 (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





M74HC366P/FP/DP

HEX 3-STATE INVERTING BUFFER WITH COMMON ENABLES

DESCRIPTION

The M74HC366 is a semiconductor integrated circuit consisting of six buffers with 3-state inverted outputs and common enable inputs.

FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=-6mA)
- High-speed: 10ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2∼6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

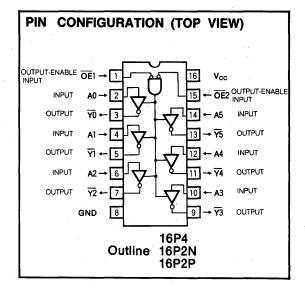
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC366 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS366.

The M74HC366 consists of six 3-state buffers with outputenable inputs common to all circuits.

When output-enable inputs $\overline{OE}1$ and $\overline{OE}2$ are both low, outputs \overline{Y} will become enable state. If input A is high, a low-level signal will be output to \overline{Y} and if input A is low, a high-level signal will be output to \overline{Y} .

When at least one of input $\overline{OE}1$ or $\overline{OE}2$ is high, \overline{Y} will become high-impedance state.



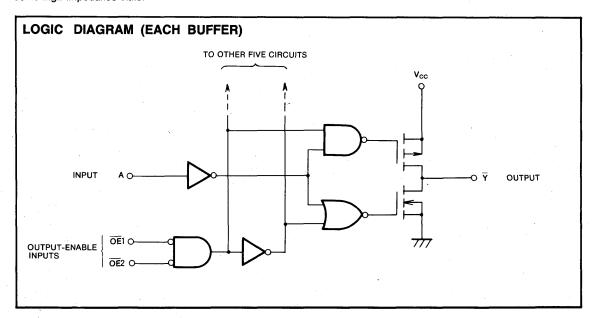
A version of the M74HC366 with a non-inverted output, the M74HC365, is also available.

FUNCTION TABLE (Note 1)

	Inputs		Output
OE1	OE2	Α	Ÿ
L	L	L	Н
L	L	Н	L
Н	×	Х	z
X	Н	X	Z

Note 1 : X : Irrelevant

Z : High impedance



HEX 3-STATE INVERTING BUFFER WITH COMMON ENABLES

ABSOLUTE MAXIMUM RATINGS $(T_a = -40 \sim +85^{\circ}C)$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
V,	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	· V
	Input protection diode current	V ₁ < 0V	-20	
lik		$V_1 > V_{CC}$	20	mA
		V ₀ < 0V	-20	
Ток	Output parasitic diode current	Vo > Vcc	20	mA
lo	Output current per output pin		±35	mA
Icc	Supply/GND current	V _{CC} , GND	±75	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		-65~+150	င

Note 2 : M74HC366FP, T $_a$ = $-40\sim+70^\circ$ C and T $_a$ = $70\sim85^\circ$ C are derated at -6mW/°C. M74HC366DP, T $_a$ = $-40\sim+50^\circ$ C and T $_a$ = $50\sim85^\circ$ C are derated at -5mW/°C.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85 \degree C)$

Ob. ad	0-	Parameter		Limits					
Symbol	Pa	rameter	Min	Тур	Max	Unit			
Vcc	Supply voltage	Supply voltage			6	V			
Vı	Input voltage		0		V _{cc}	V			
Vo	Output voltage		0		Vcc	V			
Topr	Operating temperature ra	inge	-40		+85	°C			
		$V_{CC} = 2.0V$	0	0					
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns			
,		$V_{CC} = 6.0V$	0		400				

ELECTRICAL CHARACTERISTICS

						Limits					
Symbol	Parameter	Test	conditions			25℃			+85°C	Unit	
	1	-		V _{cc} (V)	Min	Тур	Max	Min	Max		
		V = 0.1V		2.0	1.5			1.5			
VIH.	High-level input voltage	$V_O = 0.1V$ $ I_O = 20\mu A$		4.5	3.15			3.15		V	
		$ I_0 = 20\mu A$		6.0	4.2			4.2			
		V = 0.1V V	_0 1v	2.0			0.5		0.5		
V _{IL}	Low-level input voltage	$ V_0 = 0.1V, V_{CO}$ $ I_0 = 20\mu A$	= 0.1V, V _{CC} -0.1V				1.35		1.35	V	
		1 ₀ = 20μΑ		6.0			1.8		1.8		
			$I_{OH} = -20\mu A$	2.0	1.9			1.9			
			$I_{OH} = -20\mu A$	4.5	4.4			4.4			
V _{OH}	/OH High-level output voltage	$V_i = V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9		ĺ	5.9		V	
		 	$I_{OH} = -6.0 \text{mA}$	4.5	4.18			4.13			
			$I_{OH} = -7.8 \text{mA}$	6.0	5. 68			5.63			
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1		
			$I_{OL} = 20 \mu A$	4.5			0.1		0.1		
V _{OL}	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V	
			I _{OL} = 6.0mA	4.5			0. 26		0.33		
			I _{OL} = 7.8mA	6.0			0.26		0.33		
i _{tH}	High-level input current	$V_i = 6V$		6.0			0.1		1.0	μF	
I _{1L}	Low-level input current	$V_1 = 0V$		6.0			-0.1		-1.0	μF	
lozh	Off-state high-level output current	$V_{I} = V_{IH}, \ V_{IL}, \ V_{O} = V_{CC}$		6.0			0.5		5.0	μ	
lozL	Off-state low-level output current	$V_i = V_{iH}, \ V_{iL}, \ V_{iL}$	o = GND	6.0			-0.5		-5.0	μ	
Icc	Quiescent supply current	VI = VCC, GND	$I_0 = 0\mu A$	6.0			4.0		40.0	μ	

HEX 3-STATE INVERTING BUFFER WITH COMMON ENABLES

SWITCHING CHARACTERISTICS (Voc = 5V, Ta = 25°C)

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Symbol	Parameter	Test conditions		Limits			
Sylfibol	Parameter	rest conditions	Min	Typ '	Max	Unit	
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns	
t _{THL}	output transition time	C _L = 50pF (Note 4)			10	ns	
t _{PLH}	Low-level to high-level and high-level to low-level	CL = 50pr (Note 4)			18	ns	
t _{PHL}	output propagation time $(A - \overline{Y})$,		18	ns	
t _{PLZ}	Output disable time from low-level and high-level	$C_L = 5 pF (Note 4)$			36	ns	
t _{PHZ}	$(\overline{OE} - \overline{Y})$	CL = 5 pr (Note 4)			36	ns	
t _{PZL}	Output enable time to low-level and high-level	0 = 50=5 (N=== 4)			40	ns	
t _{PZH}	$(\overline{OE} - \overline{Y})$	C _L = 50pF (Note 4)			40	ns	

SWITCHING CHARACTERISTICS ($v_{cc} = 2\sim 6v$, $\tau_a = -40\sim +85^{\circ}$ C)

						Limits			1
Symbol	Parameter	Test conditions			25℃		-40~	+85℃	Unit
			V _{cc} (v)	Min	Тур	Max	Min	Max	
			2.0			60		75	
t _{TLH}	Low-level to high-level and		4.5	İ	1	12	1	15	ns
	high-level to low-level	C _L = 50pF (Note 4)	6.0			.10		13	
	Ingri-level to low-level	OE = 3001 (Note 4)	2.0		1	60		75	
t _{THL}	output transition time		4.5			12		15	ns
			6.0			10		13	
			2.0			82	ļ	102	
t _{PLH}			4.5			19		24	ns
		C _L = 50pF (Note 4)	6.0			16		20	
-		Se sep (mais),	2.0			82		102	
t _{PHL}	Low-level to high-level and		4.5	}		19	1	24	ns
	high-level to low-level		6.0			16		20	
	output propagation time		2.0	1	1	107		134	
t _{PLH}	$(A - \overline{Y})$		4.5			26		32	ns
		C _L = 150pF (Note 4)	6.0			22		27	<u>L</u>
		Se loop (note ly	2.0			107	l	.134	
t _{PHL}			4.5			26	İ	32	ns
			6.0		<u> </u>	22		27	
			2.0			175		218	l
t _{PLZ}	Output disable time from		4.5			44		55	ns
	low-level and high-level	C _L = 50pF (Note 4)	6.0			37		46	
			2.0	Ì		175		218	
t _{PHZ}	$(\overline{OE} - \overline{Y})$		4.5		į	44		55	ns
			6.0			37		46	ļ
			2.0		-	230		287	
t _{PZL}			4.5			44		55	ns
	4	C _L = 50pF (Note 4)	6.0			. 35		43	<u> </u>
			2.0		Ì	230		287	
t _{PZH}	Output enable time to		4.5			44]	55	ns
	low-level and high-level		6.0	ļ	<u> </u>	35		43	ļ
	**		2.0			245		306	
t _{PZL}	$(\overline{OE} - \overline{Y})$		4.5	-		53		.66	ns
	-	C _L = 150pF (Note 4)	6.0		<u> </u>	41	1	51	
_			2.0			245		306	
t _{PZH}			4.5	1		53	1	66	ns
			6.0		ļ	41		51	<u> </u>
C _i	Input capacitance	<u> </u>		-	-	10	ļ	10	pF
Co	Off-state output capacitance	OE = V _{CC}		-	-	15		15	pF
CPD	Power dissipation capacitance (Note 3)	1		1	46	1	1		pF

Note 3: C_{DP} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per buffer) The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$



M74HC367P/FP/DP

HEX

3-STATE NONINVERTING BUFFER WITH SEPARATE 2-BIT AND 4-BIT SECTIONS

DESCRIPTION

The M74HC367 is a semiconductor integrated circuit consisting of six buffers with 3-state noninverted outputs, the 4-bit and 2-bit sections having common enable inputs.

FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 10ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2∼6V
- Wide operating temperature range: T_a=-40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

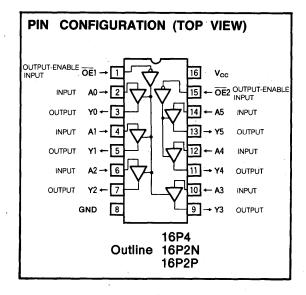
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC367 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS367.

The M74HC367 consists of six 3-state buffers with outputenable inputs common to the 2-bit and 4-bit sections.

When output-enable input \overline{OE} is low, outputs Y will become enable state. If input A is high, a high-level signal will be output to Y and if input A is low, a low-level signale will be output to Y.

When $\overline{\text{OE}}$ is high-level, Y will become high-impedance state

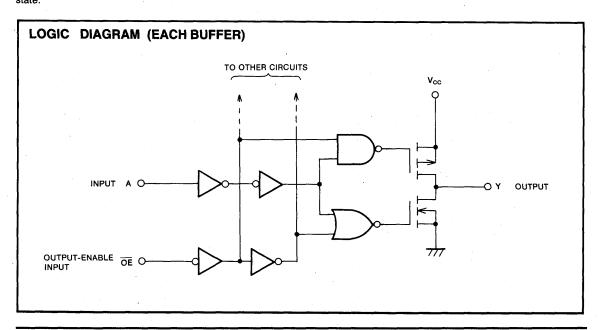


A version of the M74HC367 with an inverted output, the M74HC368, is also available.

FUNCTION TABLE (Note 1)

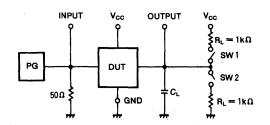
Inputs		Output
OE	Α	Y
L	L	L
L	Н	н
Н	X	Z

Note 1 : X : Irrelevant Z : High impedance



HEX 3-STATE INVERTING BUFFER WITH COMMON ENABLES

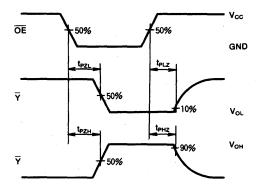
Note 4: Test Circuit



Parameter	SW 1	SW 2
t _{TLH} , t _{THL} t _{PLH} , t _{PHL}	Open	Open
t _{PLZ}	Closed	Open
t _{PH2}	Open	Closed
t _{PZL}	Closed	Open
t _{PZH}	Open	Closed

- (1) The pulse generator (PG) has the following characteristics (10%∼90%): t_r = 6ns, t_r = 6ns (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING	DIAGRAM			
				V _{CC}
^_	50%	50%		GNE
 _		90% 90% - 50% 50%		V _{ОН}
·		10% 10%	t _{TLH}	V _{OL}



HEX

3-STATE NONINVERTING BUFFER WITH SEPARATE 2-BIT AND 4-BIT SECTIONS

ABSOLUTE MAXIMUM RATINGS $(T_a = -40 \sim +85 \degree C)$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
	Innut nest alice diede	V ₁ < 0V	-20	
l _{IK}	Input protection diode current	V _i > V _{CC}	20	mA
	0.4-4	V _o < 0V	-20	
lok	Output parasitic diode current	$V_{o} > V_{cc}$	20	mA
lo	Output current per output pin		±35	mA
Icc	Supply/GND current	V _{CC} , GND	±75	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65 ~ +150	ొ

Note 2 : M74HC367FP, $T_a=-40\sim+70^\circ$ C and $T_a=70\sim85^\circ$ C are derated at -6mW/°C M74HC367DP, $T_a=-40\sim+50^\circ$ C and $T_a=50\sim85^\circ$ C are derated at -5mW/°C

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85^{\circ}C)$

Completed			-	Limits				
Symbol	Pa	Parameter		Тур	Max	Unit		
Vcc	Supply voltage		2		6	V		
V _I	Input voltage		0		Vcc	٧		
Vo	Output voltage		0		V _{cc}	٧		
Topr	Operating temperature ra	Operating temperature range			+85	°C		
		$V_{CC} = 2.0V$	0		1000			
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns		
i		$V_{CC} = 6.0V$	0		400			

ELECTRICAL CHARACTERISTICS

	·						Limits			
Symbol	Parameter	Test	conditions			25℃		−40~	+85℃	Uni
	1			V _{cc} (V)	Min	Тур	Max	Min	Max	
V _{IH}	High-level input voltage	$V_0 = V_{CC} - 0.1$ $ I_0 = 20\mu A$	/	2. 0 4. 5	1.5 3.15			1.5 3.15		٧
				6.0	4.2			4.2		
		$V_{\rm o} = 0.1 V, V_{\rm c}$	_0 1V	2.0			0.5		0.5	
VIL	Low-level input voltage	$ I_0 = 20\mu A$	3—0. TV	4.5			1.35		1.35	V
		1101 — 20μΑ		6.0			1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
		,	$i_{OH} = -20\mu A$	4.5	4.4			4.4		
V _{OH}	High-level output voltage	el output voltage $V_I = V_{IH}, V_{IL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		V
			$I_{OH} = -6.0 \text{mA}$	4.5	4.18			4. 13		
			$I_{OH} = -7.8 mA$	6.0	5. 68		1	5. 63	'	
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
			$I_{OL} = 20 \mu A$	4.5	,		0.1		0.1	
VoL	Low-level output voltage	$V_i = V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
			$I_{OL} = 6.0 \text{mA}$	4.5			0.26		0.33	
			I _{OL} = 7.8mA	6.0			0.26		0.33	
I _{IH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μΙ
l _{iL}	Low-level input current	$V_i = 0V$		6.0			-0.1		-1.0	μ
lozh	Off-state high-level output current	$V_{i} = V_{iH}, \ V_{iL},$	$V_{\rm o} = V_{\rm CC}$	6.0			0.5		5.0	μ
lozL	Off-state low-level output current	$V_i = V_{iH}, \ V_{iL},$	Vo = GND	6.0			-0.5		-5.0	μ
Icc	Quiescent supply current	VI = VCC, GND	$l_0 = 0 \mu A$	6.0			4.0		40.0	μι

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3-STATE NONINVERTING BUFFER WITH SEPARATE 2-BIT AND 4-BIT SECTIONS

SWITCHING CHARACTERISTICS ($V_{cc} = 5V$, $T_a = 25^{\circ}C$)

0	Parameter	7	Limits			1 1-14
Symbol		Test conditions	Min	Тур	Max	Unit
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time	 			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	CL — Supr (Note 4)			22	ns
t _{PHL}	output propagation time (A - Y)				22	ns
t _{PLZ}	Output disable time from low-level and high-level	C - E-F (Note A)			33	ns
t _{PHZ}	(OE – Y)	C _L = 5 pF (Note 4)			33	ns
tpzL	Output enable time to low-level and high-level	C ₁ = 50pF (Note 4)			37	ns
t _{PZH}	(OE – Y)	CL - SUPF (NOIG 4)			37	ns

SWITCHING CHARACTERISTICS ($V_{cc} = 2\sim 6V$, $T_a = -40\sim +85$ °C)

		Parameter Test conditions		Limits				1	
Symbol	Parameter				25℃		-40~	+85℃	Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	
	İ		2.0			60	·	75	
t _{TLH}	Low-level to high-level and		4.5			12		15	ns
	high described from Learning	C _L = 50pF (Note 4)	6.0			10	İ	13	
	high-level to low-level	C _L = 50pr (Note 4)	2.0			60		75	
t _{THL}	output transition time		4.5	ł		12	'	15	ns
			6.0			10		13	
			2.0			105		130	
t _{PLH}			4.5			24		30	ns
			6.0			19	ļ	24	
	1	C _L = 50pF (Note 4)	2.0			105		130	
t _{PHL}	Low-level to high-level and		4.5	:		24		30	ns
'	high-level to low-level		6.0	1		19	Ĭ	24	
	output propagation time		2.0			135		168	
t _{PLH}	(A - Y)		4.5			29		36	ns
			6.0			24		30	
	-	C _L = 150pF (Note 4)	2.0			135		168	
tpHL		•	4.5	Ì		29	1	36	ns
YPHL		·	6.0	1		24		30	,,,,
	-		2.0			117		146	
t _{PLZ}	Output disable time from		4.5			35	l	44	ns
PLZ	Cupit disable time from		6.0			31	l	39	115
	low-level and high-level	C _L == 50pF (Note 4)	2.0		<u> </u>	117		146	
•	(OE - Y)		4.5			35	}	44	ns
t _{PHZ}	(02 1)		6.0	}		31	1	39	115
	 		2.0			172	 	216	
4			4.5	t		38		47	ns
t _{PZL}	·		6.0			35		43	118
	1	C _L = 50pF (Note 4)			ļ.——-				
	Output anable time to		2.0	1		172	1	216	
t _{PZH}	Output enable time to		4.5			38	1.	47	ns
	low-level and high-level		6.0	 	ļ	35	 	43	
١.	(OF W)	:	2.0			187		233	
t _{PZL}	(OE - Y)		4.5			46	1	57	ns
	-	C _L = 150pF (Note 4)	6.0			42	<u> </u>	52	
			2.0			187		233	
t _{PZH}			4.5			46	1	57	ns
<u> </u>			6.0	ļ		42	ļ	52	
Cı	Input capacitance				<u> </u>	10		10	pF
Co	Off-state output capacitance	OE = V _{CC}			<u> </u>	15		15	pF
C _{PD}	Power dissipation capacitance (Note 3)		_1		47	1			pF

Note 3: C_{DP} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per buffer)

The power dissipated during operation under no-load conditions is calculated using the following formula:

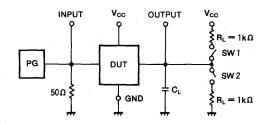
P_D = C_{PD} • V_{CC}² • f₁+I_{CC} • V_{CC}



HEX

3-STATE NONINVERTING BUFFER WITH SEPARATE 2-BIT AND 4-BIT SECTIONS

Note 4: Test Circuit

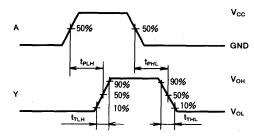


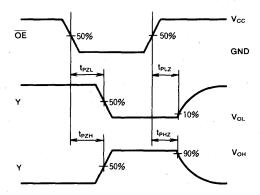
Parameter	SW 1	SW 2
t _{TLH} , t _{THL}	Open	Open
t _{PLZ}	Closed	Open
t _{PHZ}	Open	Closed
t _{PZL}	Closed	Open
t _{PZH}	Open	Closed

(1) The pulse generator (PG) has the following characteristics (10%~90%): $t_{\rm f}=6{\rm ns},\,t_{\rm f}=6{\rm ns}$

(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





M74HC368P/FP/DP

HEX 3-STATE INVERTING BUFFER WITH SEPARATE 2-BIT AND 4-BIT SECTIONS

DESCRIPTION

The M74HC368 is a semiconductor integrated circuit consisting of six buffers with 3-state inverted output, the 4-bit and 2-bit sections having common enable inputs.

FEATURES

- High-fanout 3-state output: (1_{OL}=6mA, 1_{OH}=−6mA)
- High-speed: 10ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=-40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

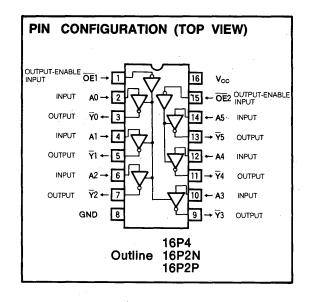
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC368 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS368.

The M74HC368 consists of six 3-state buffers with outputenable inputs common to the 2-bit and 4-bit sections.

When output-enable input \overline{OE} is low, outputs \overline{Y} will become enable state. If input A is high, a low-level signale will be output to \overline{Y} and if input A is low, a high-level signal will be output to \overline{Y} .

When \overline{OE} is high, \overline{Y} will become high-impedance state.



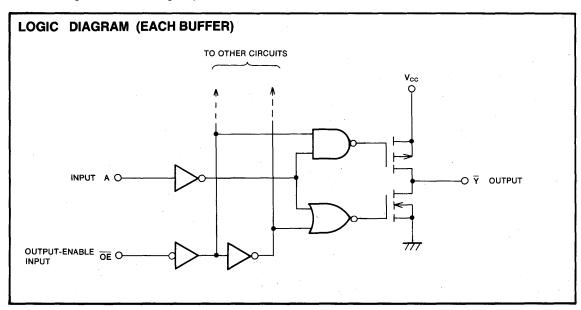
A version of the M74HC368 with a noninverted output, the M74HC367, is also available.

FUNCTION TABLE (Note 1)

Inp	Inputs						
ŌE	Α	Ÿ					
L	Ļ	Н					
L	Н	L					
н	X	· Z					

Note 1 : X : Irrelevant

Z : High impedance



HEX 3-STATE INVERTING BUFFER WITH SEPARATE 2-BIT AND 4-BIT SECTIONS

ABSOLUTE MAXIMUM RATINGS ($\tau_a = -40 \sim +85 \degree$ C, unless otherwise noted)

Symbol	Parameter	Test conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
	Inc. 4 and a size of a surrent	V ₁ < 0V	-20	4
l _{iK}	Input protection diode current	$V_{l} > V_{CC}$	20	mA
	Contract and the state of the s	V ₀ < 0V	-20	
lok	Output parasitic diode current	V _o > V _{cc}	20	mA
lo	Output current per output pin		±35	mA
lcc	Supply/GND current	V _{CC} , GND	±75	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		-65~+150	°C

Note 2 : M74HC368FP, $T_a = -40 \sim +60^\circ$ C and $T_a = 60 \sim 85^\circ$ C are derated at -6mW/°C M74HC368DP, $T_a = -40 \sim +50^\circ$ C and $T_a = 50 \sim 85^\circ$ C are derated at -5mW/°C

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85 \degree c)$

Symbol		ramotor		Limits				
Sylfibol	Parameter		Min	Тур	Max	Unit		
Vcc	Supply voltage		2		6	V		
Vı	Input voltage		0		Vcc	٧		
V _o	Output voltage		0		Vcc	V		
Topr	Operating temperature range		-40		+85	°C		
		V _{CC} = 2.0V	0		1000			
t _r , t _f inpu	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns		
		$V_{CC} = 6.0V$	0		400			

ELECTRICAL CHARACTERISTICS

							Limits			ŀ
Symbol	Parameter	Test	conditions		25℃		-40~	+85℃	Unit	
			V _{cc} (V)		Min Typ	Max	Min	Max		
V _{IH}	High-level input voltage	$V_0 = 0.1V$ $ I_0 = 20\mu A$		2.0 4.5 6.0	1.5 3.15 4.2	•		1.5 3.15 4.2		v
V _{IL}	Low-level input voltage	$V_0 = 0.1V, V_{CO}$ $ I_0 = 20\mu A$	_c —0.1V	2. 0 4. 5 6. 0			0.5 1.35 1.8		0.5 1.35 1.8	v
V _{OH}	High-level output voltage	$V_{l} = V_{lL}$	$I_{OH} = -20\mu A$ $I_{OH} = -20\mu A$ $I_{OH} = -20\mu A$ $I_{OH} = -6.0 \text{mA}$	2. 0 4. 5 6. 0 4. 5	1.9 4.4 5.9 4.18			1.9 4.4 5.9 4.13		V
	<u></u>		$I_{OH} = -7.8 \text{mA}$ $I_{OL} = 20 \mu \text{A}$	6.0	5. 68		0.1	5. 63	0.1	
Vol	Low-level output voltage	$V_{l}=V_{lH},\ V_{lL}$	$I_{OL} = 20\mu A$ $I_{OL} = 20\mu A$ $I_{OL} = 20\mu A$ $I_{OL} = 6.0 mA$ $I_{OL} = 7.8 mA$	4. 5 6. 0 4. 5 6. 0			0. 1 0. 1 0. 26 0. 26		0. 1 0. 1 0. 33 0. 33	v
I _{IH}	High-level input current	$V_i = 6V$		6.0			0.1		1.0	μΑ
I _{IL}	Low-level input current	$V_1 = 0V$		6.0			-0.1		-1.0	μΑ
lozh	Off-state high-level output current	$V_i = V_{iH}, \ V_{iL},$	$V_{\rm o} = V_{\rm cc}$	6.0			0.5		5.0	μА
lozL	Off-state low-level output current	$V_i = V_{iH}, \ V_{iL}, \ $	V _O = GND	6.0			-0.5		-5.0	μΑ
Icc	Quiescent supply current	VI = VCC, GND	$I_0 = 0 \mu A$	6.0			4.0	-	40.0	μΑ

HEX 3-STATE INVERTING BUFFER WITH SEPARATE 2-BIT AND 4-BIT SECTIONS

SWITCHING CHARACTERISTICS $(V_{cc} = 5V, T_a = 25^{\circ}C)$

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Symbol	Parameter	Test conditions		Limits			
Symbol	Parameter	rest conditions	Min	Тур	Max	Unit	
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns	
t _{THL}	output transition time	C ₁ = 50pF (Note 4)			10	ns	
t _{PLH}	Low-level to high-level and high-level to low-level	C _L — 50pr (Note 4)			18	ns	
t _{PHL}	output propagation time $(A - \overline{Y})$				18	ns	
t _{PLZ}	Output disable time from low-level and high-level	0 = 5 = 5 (N=4=4)			33	ņs	
t _{PHZ}	$(\overline{OE} - \overline{Y})$	C _L = 5 pF (Note 4)			33	ns .	
t _{PZL}	Output enable time to low-level and high-level	C ₁ = 50pF (Note 4)			37	ns	
t _{PZH}	$(\overline{OE} - \overline{Y})$	C _L = 50pr (Note 4)			37	ns	

SWITCHING CHARACTERISTICS ($V_{cc} = 2\sim6V$, $T_a = -40\sim+85^{\circ}C$)

						Limits			
Symbol	Parameter	Test conditions			25℃		−40 ~	+85℃	Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	
		-	2.0			60		75	
t _{TLH}	Low-level to high-level and		4.5			12		15	ns
	high level to level	C _L = 50pF (Note 4)	6.0			10		13	
	high-level to low-level	C _L - sopr (Note 4)	2.0			60		75	
t _{THL}	output transition time		4.5			12		15	ns
			6.0			10		13	
			2. 0			82		102	
t _{PLH}			4.5			19	,	24	ns
		C _L = 50pF (Note 4)	6.0			16		20	
		C _L = 50pr (Note 4)	2.0			82		102	
t _{PHL}	Low-level to high-level and		4.5			19		24	ns
	high-level to low-level		6.0			16		20	1
	output propagation time		2.0			107		134	
t _{PLH}	$(A - \overline{Y})$		4.5			26		32	ns
			6.0			22		27	
		C _L = 150pF (Note 4)	2.0			107		134	
t _{PHL}			4.5			26		32	ns
			6.0			22		27	
			2.0			117		146	
t _{PLZ}	Output disable time from		4.5		1	35	l	44	ns
			6.0			31		39	
	low-level and high-level	C _L = 50pF (Note 4)	2.0			117		146	
t _{PHZ}	$(\overline{OE} - \overline{Y})$		4.5			35		44	ns
			6.0			31	1	39	
			2.0			172		216	
tpZL	1		4.5		•	38		47	ns
			6.0			35		43	
-	1	C _L = 50pF (Note 4)	2.0			172		216	
t _{PZH}	Output enable time to		4.5			38		47	ns
	1		6.0			35	-	43	
	low-level and high-level		2.0	-		187		233	
t _{PZL}	$(\overline{OE} - \overline{Y})$		4.5			46		57	ns
			6.0			42		52	
	1	C _L = 150pF (Note 4)	2.0			187		233	
t _{PZH}			4.5	Į	1	46		57	ns
		1	6.0			42		52	
Cı	Input capacitance				1	10		10	pF
Co	Off-state output capacitance	OE = V _{CC}				15		15	pF
C _{PD}	Power dissipation capacitance (Note 3)	1	-		44			1	pF

Note 3 : C_{DP} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per buffer)

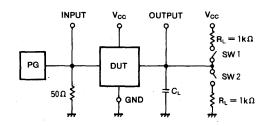
The power dissipated during operation under no-load conditions is calculated using the following formula:

P_D = C_{PD} · V_{CC}² · f₁+I_{CC} · V_{CC}



HEX 3-STATE INVERTING BUFFER WITH SEPARATE 2-BIT AND 4-BIT SECTIONS

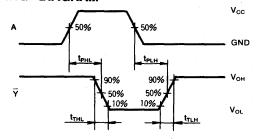
Note 4: Test Circuit

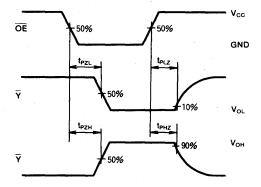


Parameter	SW1	SW 2
t _{TLH} , t _{THL}	Open	Open
t _{PLZ}	Closed	Open
t _{PHZ}	Open	Closed
t _{PZL}	Closed	Open
t _{PZH}	Open	Closed

(1) The pulse generator (PG) has the following characteristics (10%~90%): t_f = 6ns, t_f = 6ns (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





M74HC373P/FP/DWP

OCTAL 3-STATE NONINVERTING D-TYPE TRANSPARENT LATCH

DESCRIPTION

The M74HC373 is a semiconductor integrated circuit consisting of eight 3-state output D-type latches with common latch-enable input and output-enable input.

FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=-6mA)
- High-speed: 13ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=-40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

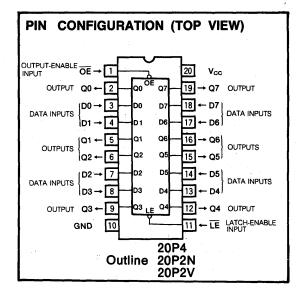
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC373 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS373.

The M74HC373 consists of eight D-type latches with latchenable input $\overline{\text{DE}}$ and output-enable input $\overline{\text{DE}}$ common to all circuits.

When \overline{LE} is high, the data at input D appears at output Q through the latch and the Q state follows changes in the D state. When \overline{LE} changes from high-level to low-level, the data existing immediatry prior to the change at D will be stored in the latch.

Even if other inputs are changed when $\overline{\text{LE}}$ is low, the contents stored in the latch will not be affected.



When $\overline{\text{OE}}$ is high, all outputs Q will become high-impedance state.

A version of the M74HC373 with the same pin connections and an inverted output, the M74HC533, is also available.

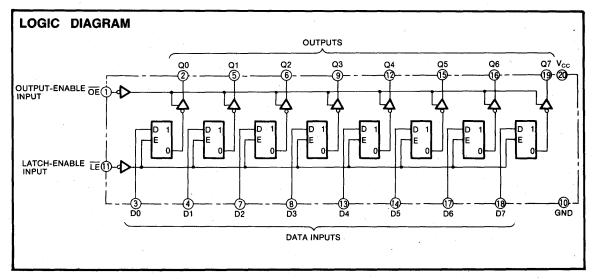
FUNCTION TABLE (Note 1)

	Inputs					
OE	LE	D	Q			
L	Н	Н	Н			
L	н	L	L			
L	L	Х	Q°			
Н	X	X	Z			

Note 1: Qo: Output state Q before LE changed

Z : High impedance

X : Irrelevant



ABSOLUTE MAXIMUM RATINGS ($\tau_a = -40 \sim +85 \degree$ C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	٧
V_i .	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
	Input protection diode current	V ₁ < 0V	-20	
l _{iK}	input protection diode current	$V_i > V_{CC}$	20	mA
		V ₀ < 0V	-20	
Іок	Output parasitic diode current	$v_o > v_{cc}$	20	mA mA
lo	Output current per output pin		±35	mA
lcc	Supply/GND current	V _{CC} , GND	±75	mA
Pd	Power dissipation	(Not 2)	500	mW
Tstg	Storage temperature range		-65~+150	င

Note 2 : M74HC373FP, $T_a=-40\sim+75^\circ\text{C}$ and $T_a=75\sim85^\circ\text{C}$ are derated at $-7\text{mW}/^\circ\text{C}$. M74HC373DWP, $T_a=-40\sim+80^\circ\text{C}$ and $T_a=80\sim85^\circ\text{C}$ are derated at $-7\text{mW}/^\circ\text{C}$.

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85 \degree c)$

0	Do.	Parameter		Limits				
Symbol	Pa	rameter	Min	Тур	Max	Unit		
Vcc	Supply voltage		2		6	٧		
V ₁	Input voltage	Input voltage			Vcc	V		
Vo	Output voltage		0		Vcc	٧		
Topr	Operating temperature ra	ange	-40		+85	ဗ		
		$V_{CC} = 2.0V$	0		1000			
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns		
		$V_{CC} = 6.0V$	0		400			

ELECTRICAL CHARACTERISTICS

							Limits	.,.		
Symbol	Parameter	Test	conditions		25℃			-40~	+85℃	Unit
				V _{cc} (v)	Min	Тур	Max	Min	Max	
		$V_0 = 0.1V, V_{CO}$	-0.17	2.0	1.5			1.5		
VIH	High-level input voltage	$ v_0 = 0.1V$, v_{CO}	-0. IV	4.5	3.15			3. 15		V
		1101 - 20#A		6.0	4.2			4.2		
	-	$V_0 = 0.1V$, V_{cc}	-0.1W W 0.1W				0.5		0.5	
VIL	Low-level input voltage	$ I_0 = 20\mu A$		4.5			1.35		1.35	V
		1101 - 20µA		6.0			1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
			$I_{OH} = -20\mu A$	4.5	4.4			4. 4		
V_{OH}	High-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		v
			$I_{OH} = -6.0 \text{mA}$	4.5	4.18			4.13		
			$I_{OH} = -7.8 \text{mA}$	6.0	5. 68			5.63		·
			$I_{OL} = 20 \mu A$	2.0			0. 1		0.1	
			$I_{OL} = 20 \mu A$	4.5		1	0.1		0.1	
VoL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
			$I_{OL} = 6.0 \text{mA}$	4.5			0.26		0.33	
			$I_{OL} = 7.8 mA$	6.0			0. 26		0.33	
l _{iH}	High-level input current .	$V_i = 6V$		6.0			0.1		1.0	μA
l ₁ _	Low-level input current	V ₁ = 0V		6.0			-0.1		-1.0	μA
l _{ozh}	Off-state high-level output current	$V_i = V_{iH}, \ V_{iL}, \ V_{iL}$	$V_{\rm O} = V_{\rm CC}$	6.0			0.5		5.0	μA
lozL	Off-state low-level output current	$V_i = V_{iH}, \ V_{iL}, \ V_{iL}$	o = GND	6.0			-0.5		-5.0	μA
Icc	Quiescent supply current	VI = VCC, GND	$I_0 = 0\mu A$	6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS ($v_{cc} = 5v$, $\tau_a = 25$ °C)

Symbol	Parameter	Test conditions		Limits				
Symbol	Parameter	rest conditions	Min	Тур	Max	Unit		
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns		
t _{THL}	output transition time				10	ns		
tpLH	Low-level to high-level and high-level to low-level	C _L = 50pF (Note 4)			25	ns		
t _{PHL}	output propagation time (D - Q)		-		25	ns		
t _{PLH}	Low-level to high-level and high-level to low-level				30	ns		
t _{PHL}	output propagation time (LE - Q)				30	ns		
t _{PLZ}	Output disable time from low-level and high-level	0 = 5 = 5 (N - 1 - 1)			25	ns		
t _{PHZ}	(OE - Q)	C _L = 5 pF (Note 4)			25	ns		
t _{PZL}	Output enable time to low-level and high-level	0 = 50-5 (N-4-4)			28	ns		
t _{PZH}	(OE – Q)	C _L = 50pF (Note 4)			28	ns		

SWITCHING CHARACTERISTICS ($V_{cc} = 2\sim6V$, $T_a = -40\sim+85^{\circ}C$)

Cumbal	Do	Took conditions	t		25℃	Limits	40 -	+85°C	Uni
Symbol	Parameter	Test conditions	14 (40)						Uni
			V _{cc} (V)	Min	Тур	Max	Min	Max	├
	1		2.0		1	60		75	ļ
TLH	Low-level to high-level and		4.5		-	12		15	n:
	high-level to low-level	C _L = 50pF (Note 4)	6.0		-	10		13	
			2.0			60		75	
THL	output transition time		4.5			12		15	n
		 	6.0		-	10		13	<u> </u>
	-		2.0	*		150		189	
PLH			4.5			30		38	n
1	4. • • • • • • • • • • •	C _L = 50pF (Note 4)	6.0			26		32	-
		`]	2.0]	150		189	
PHL	Low-level to high-level and		4.5			30		38	n
	high-level to low-level		6.0			26		32	-
	output propagation time		2.0		1	200		252	
PLH	(D-Q)		4.5		1	40		50	n
	4	$C_L = 150 pF (Note 4)$	6.0			34		43	<u> </u>
			2.0			200		252	
PHL			4.5			40		50	n
	·		6.0			34		43	1
			2.0			175		221	
t _{PLH}			4. 5		1	35		44	n
		C _L = 50pF (Note 4)	6.0			30		37	
		SE CODE (NOIS 1)	2.0			175		221	
PHL	Low-level to high-level and		4.5			35		44	n
	high-level to low-level		6.0			30		. 37	
	output propagation time		2.0		1	225		284	
t _{PLH}	(<u>LE</u> — Q)		4.5			45		57	n
		C _L = 150pF (Note 4)	6.0			38		48	
		OL — ISOPI (Note 4)	2.0			225		284	
t _{PHL}		· ·	4.5			45		57	n
			6.0			38		48	
			2.0			150		189	
t _{PLZ}	Output disable time from		4.5			30		. 38	n
	tana lanal and black tanal	0 - 50-5 (Note 4)	6.0			26		32	
	low-level and high-level	C _L = 50pF (Note 4)	2.0			150		189	
PHZ	(OE - Q)		4.5			30		38	n
		, ,	6.0			26		32	
			2.0			150		189	
t _{PZL}			4.5			30		38	n
		0 - 50-5 (N-: 1)	6.0		1	26		32	1
		$C_L = 50 pF \text{ (Note 4)}$	2. 0			150		189	
t _{PZH}	Output enable time to		4.5		1	30		38	n
	1		6.0			26		32	
	low-level and high-level		2.0			200		252	
PZL	(OE – Q)		4. 5			40		50	n
			6.0			34		43	
		$C_L = 150 pF (Note 4)$	2. 0			200		252	
t _{PZH}			4.5			40		50	l n
ZN			6.0		1	34		43	Ι "
C ₁	Input capacitance		"			10		10	р
Co	Output disabled capacitance	OE = V _{CC}			 	15		15	p
- 0				L		'3	<u> </u>	13	p

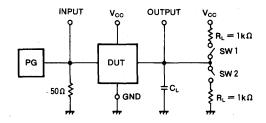
Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per latch)
The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$



TIMING REQUIREMENTS $(v_{cc} = 2\sim6v, T_a = -40\sim+85^{\circ})$

				. Limits					
Symbol	Parameter	Test conditions		25℃			-40~	+85℃	Unit
		·	V _{cc} (V)	Min	Тур	Max	Min	Max	1
			2,0	80			101		
tw	Latch enable pulse width		4.5	16	•		20		ns
		***	6.0	. 14			17		
	D		2.0	75			90		
t _{su}	D setup time with	•	4.5	15			18		ns
	respect to LE		6.0	13			16		
	D b ald dies a suith		2.0	50	-		60		
th	D hold time with		4.5	10		1	12		ns
	respect to LE		6.0	. 9			11		

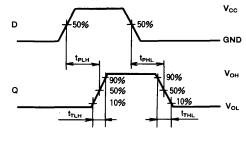
Note 4: Test Circuit

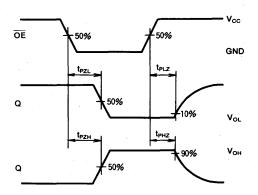


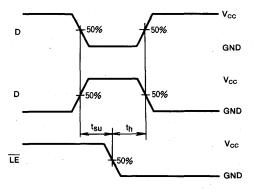
Parameter	SW1	SW 2
t _{TLH} , t _{THL} t _{PLH} , t _{PHL}	Open	Open
t _{PLZ}	Closed	Open
t _{PHZ}	Open	Closed
t _{PZL}	Closed	Open
t _{PZH}	Open	Closed

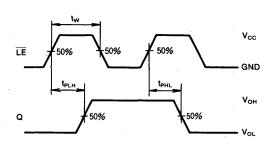
- (1) The pulse generator (PG) has the following characteristics (10% \sim 90%): t_f = 6ns, t_f = 6ns
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM









M74HC373-1P/FP/DWP

OCTAL 3-STATE NONINVERTING D-TYPE TRANSPARENT LATCH

DESCRIPTION

The M74HC373-1 is a semiconductor integrated circuit consisting of eight 3-state output D-type latches with common latch-enable input and output-enable input.

FEATURES

- High-fanout 3-state output: (I_{OL}=24mA, I_{OH}=-24mA)
- High-speed: 9ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 25μW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 60 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

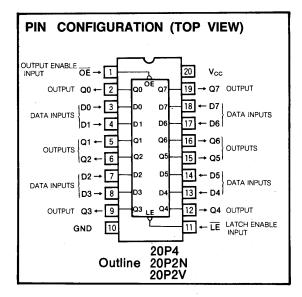
Use of silicon gate technology allows the M74HC373-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS373.

The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

The M74HC373-1 consists of eight D-type latches with latch-enable input $\overline{\text{LE}}$ and output-enable input $\overline{\text{OE}}$ common to all circuits.

When \overline{LE} is high, the data at input D appears at output Q through the latch and the Q state follows changes in the D state. When \overline{LE} changes from high-level to low-level, the data existing immediatry prior to the change at D will be stored in the latch.

Even if other inputs are changed when $\overline{\text{LE}}$ is low, the contents stored in the latch will not be affected .



When $\overline{\text{OE}}$ is high, all outputs Q will become high-impedance state.

A version of the M74HC373-1 with the same pin connections and an inverted output, the M74HC533-1, is also available.

FUNCTION TABLE (Note 1)

	Inputs		Output
ŌE	LE	D	Q
L	Н	Н	Н
L	• Н	L	L`
L	L	х	Q٥
Н	Х	Х	z

Note 1: Qº: Output state Q before LE changed

Z : High impedance X : Irrelevant

LOGIC DIAGRAM OUTPUTS Q2 Q3 Q4 Q5 Q6 Q7 V_{CC} (5) (19-2**9**+ ⊚ (9) OUTPUT ENABLE OE LATCH ENABLE LE **(10)** GND DATA INPUTS

ABSOLUTE MAXIMUM RATINGS $(T_a = -40 \sim +85^{\circ}C, \text{ unless otherwise noted})$

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
	V _I < 0V	-20		
lik .	Input protection diode current	$V_{i} > V_{CC}$	20	mA
		V ₀ < 0V	-20	
lok	Output parasitic diode current	V _o > V _{cc}	20	mA mA
lo	Output current per output pin		±50	mA -
loc	Supply/GND current	V _{CC} , GND	±200	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature		−65∼ +150	°C

Note 2 : M74HC373-1FP , $T_a=-40\sim+75^\circ$ C and $T_a=75\sim85^\circ$ C are derated at -7mW/°C . M74HC373-1DWP, $T_a=-40\sim+80^\circ$ C and $T_a=80\sim85^\circ$ C are derated at -7mW/°C .

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85 \degree C)$

Symbol	Parameter		L .	Limits				
Syllibol	ra	Min	Тур	Max	Unit			
Vcc	Supply voltage		2		6	V		
Vt	Input voltage		0		V _{CC}	٧		
Vo	Output voltage	0		Vcc	V			
Topr	Operating temperature ra	ange	40		+85	င		
		$V_{CC} = 2.0V$	0		500			
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$.0		50	ns/V		
		$V_{CC} = 6.0V$	0		30			

ELECTRICAL CHARACTERISTICS

							Limits			
Symbol	Parameter	Test	conditions			25℃		-40~+85°C		Unit
L		•		V _{CC} (V)	Min	Тур	Max	Min	Max	
		$V_0 = 0.1V, V_{00}$	0.11/	2.0	1.5			1.5		
VIH	High-level input voltnge	$ I_0 = 20\mu A$	5 - 0.1 V	4.5	3.15			3. 15		V
	_	1101 — 20µA		6.0	4.2			4. 2		
		V = 0.1V V	_0.17	2.0			0.5		0.5	
VIL	Low-level input voltage	$ I_0 = 20\mu A$	$V_0 = 0.1V$, $V_{CC} = 0.1V$				1.35		1.35	V
		1101 - 20µA		6.0			1.8		1.8	
	High-level output voltage	High-level output voltage $V_{l} = V_{lL}, V_{lH}$	$I_{OH} = -20\mu A$	2.0	1.9			1.9		100
			$I_{OH} = -20\mu A$	4.5	4.4	}	1	4.4	}	v
V _{OH}			$I_{OH} = -20\mu A$	6.0	5.9			5.9		
			$I_{OH} = -24 \text{mA}$	4.5	3. 98			3.84		
		-	$I_{OL} = 20 \mu A$	2.0			0.1	-	0. 1	
VoL	Low-level output voltnge	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	4.5			0.1	l	0.1	v
VOL	Low-level output voilinge	VI — VIH, VIL	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	
			$I_{OL} = 24mA$	4.5			0.39		0.5	
I _{IH}	High-level inputcurrent	$V_1 = 6V$		6.0			0.1		1.0	
l _{IL}	Low-level input current	$V_i = 0V$		6.0			-0.1		-1.0	μA
I _{OZH}	Off-state high-level output current	$V_i = V_{iH}, V_{iL}, V_{iL}$	Vo = Vcc	6.0			0.5		5.0	μА
lozL	Off-state low-level output current	$V_1 = V_{1H}, V_{1L}, V_{1L}$	o = GND	6.0			-0.5		-5.0	
lcc	Quiescent supply current	$V_{I} = V_{CC}$, GND	$I_0 = 0\mu A$	6.0			5.0		50.0	μA

SWITCHING CHARACTERISTICS ($v_{cc} = 5v$, $\tau_a = 25^{\circ}$)

		T4dist	Limits			Unit
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time				10	115
tpLH	Low-level to high-level and high-level to low-level	C ₁ = 50pF (Note 4)			18	ns
t _{PHL}	output propagation time (D - Q)	C _L = 50pF (Note 4)			18	1113
t _{PLH}	Low-level to high-level and high-level to low-level				21	ns
t _{PHL}	output propagation time (LE - Q)				21	115
t _{PLZ}	Output disable time from low-level and high-level	$C_1 = 5 pF (Note 4)$			20	ns
t _{PHZ}	(OE - Q)	GL = 5 pr (Note 4)			20	110
t _{PZL}	Output enable time to low-level and high-level	$C_1 = 50pF $ (Note 4)			23	
t _{PZH}	(OE - Q)	OL — Sopr (Note 4)			23	

SWITCHING CHARACTERISTICS ($v_{cc} = 2\sim 6V$, $T_a = -40\sim +85\%$)

,						Limits			
Symbol	Parameter	Test conditions			25℃		-40~	+85℃	Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0			60		75	
t _{TLH}	Low-level to high-level and		4.5			12		15	
	1	*	6.0			10		13	
	high-level to low-level		2.0			60		75	ns
tTHL	output transition time		4.5			12		15	
			6.0			10		13	ļ
		7	2.0			100		125	٠.
t _{PLH}	Low-level to high-level and		4.5			20		25	
	high-level to low-level		6.0			17		21	
	output propagation time		2.0			100		125	ns
t _{PHL}	(D - Q)		4.5			20		25	
			6.0			17		21	
			2.0			115		145	
t _{PLH}	Low-level to high-level and		4.5			23		29	
high-level to low-level	50.5(11.4)	6.0			20		25		
,	output propagation time	C _L = 50pF (Note 4)	2.0			115		145	ns
t _{PHL}	(LE - Q)		4.5			23		29	
	·		6.0	ı		20		25	
		1	2.0	*		125		155	
t _{PLZ}	Output disable time from	·	4.5			25		31	
	h	1	6.0			-21		26	
	low-level and high-level		2.0			125		155	ns
t _{PHZ}	(OE - Q)		4.5			25		31	
			6.0			21		. 26	
		¹	2.0			125		155	
t _{PZL}	Output enable time to		4.5			25		31	
	· ·		6.0			21		26	
-	low-level and high-level		2.0			125		155	ns
t _{PZH}	(OE - Q)		4.5			25		31	
			6.0			21		26	
Cı	Input capacitance		1			10		10	
Co	Off-state output capacitance	OE = V _{CC}				15		15	pF
C _{PD}	Power dissipation capacitance (Note 3)	1						 	1 "

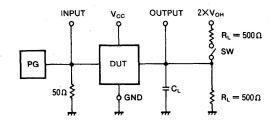
Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$



TIMING REQUIREMENTS ($V_{cc} = 2\sim 6V$, $T_a = -40\sim +85^{\circ}C$)

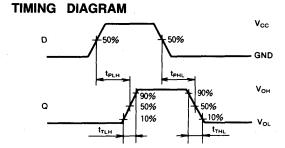
		,		Limits					
Symbol	Parameter	Test conditions	25℃			-40~+85℃		Unit	
			V _{cc} (V)	Min	Тур	Max	Min	Max	
			2,0	60			75		
tw	t _w Latch enable pulse width		4.5	12			15		ns
			6.0	10			13		1
	D to time time		2.0	50			65		
t _{su}	D setup time with		4.5	10		ŀ	13		ns
	respect to LE		6.0	. 9		l	11		
	D h ald time a with		2, 0	25			30		
th	D hold time with		4.5	5			6		ns
	respect to LE		6.0	5		1	6]

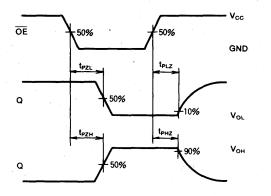
Note 4: Test Circuit

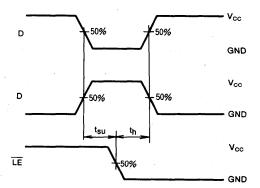


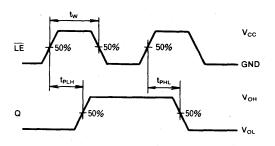
Parameter	sw
t _{TLH} , t _{THL}	Open
t _{PLZ}	Closed
t _{PHZ}	Open
t _{PZL}	Closed
t _{PZH}	Open

- (1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 3ns, t_f = 3ns
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.









M74HCT373-1P/FP/DWP

OCTAL 3-STATE NONINVERTING
D-TYPE TRANSPARENT LATCH WITH LSTTL-COMPATIBLE INPUTS

DESCRIPTION

The M74HCT373-1 is a semiconductor integrated circuit consisting of eight 3-state output D-type latches with common latch-enable input and output-enable input.

FEATURES

- TTL level inputs V_{IL}=0.8V max, V_{IH}=2.0V min
- High-fanout 3-state output: (I_{OL} =24mA, I_{OH} =-24mA)
- High-speed: 11ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 25µW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- Capable of driving 60 74LSTTL loads
- Wide operating temperature range: T_a=-40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

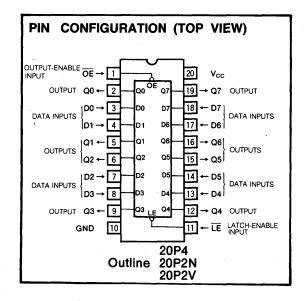
Use of silicon gate technology allows the M74HCT373-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS373.

The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

As the inputs are TTL level, the device can be used as a level converter from LSTTL to high-speed CMOS. In that case, no pull-up resistors are required.

The M74HCT373-1 consists of eight D-type latches with latch-enable input $\overline{\text{OE}}$ and output-enable input $\overline{\text{OE}}$ common to all circuits.

When \overline{LE} is high, the data at input D appears at output Q through the latch and the Q state follows changes in the D state. When \overline{LE} changes from high-level to low-level, the

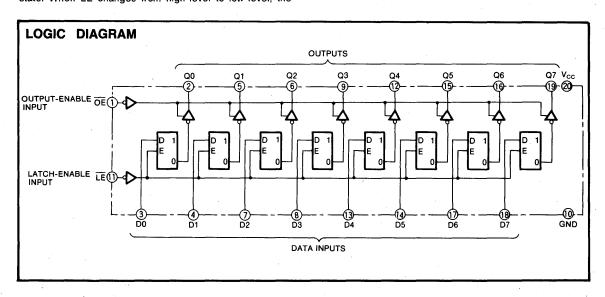


data existing immediatry prior to the change at D will be stored in the latch.

Even if other inputs are changed when $\overline{\text{LE}}$ is low, the contents stored in the latch will not be affected .

When $\overline{\text{OE}}$ is high, all outputs Q will become high-impedance state.

A version of the M74HCT373-1 with the same pin connections and an inverted output, the M74HCT533-1, is also available.



OCTAL 3-STATE NONINVERTING D-TYPE TRANSPARENT LATCH WITH LSTTL-COMPATIBLE INPUTS

FUNCTION TABLE (Note 1)

	Inputs		Output
OE	LE	D	Q
L	н	Н	Н
L	Н	L	L
L	L	Х	Q°
Н	X	Х	Z

Note 1 : Q₀: Output state Q before LE changed Z : High impedance X : Irrelevant

ABSOLUTE NAXIMUM RATINGS ($T_a = -40 \sim +85^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit	
Vcc	Supply voltage		-0.5~+7.0	V	
Vı	Input voltage		-0.5~V _{cc} +0.5	V	
Vo	Output voltage		-0.5~V _{cc} +0.5	V	
	1	V ₁ < 0V	-20		
lік	Input protection diode current	$V_{l} > V_{CC}$	20	mA .	
	O da da a a a a a a a a a a a a a a a a	V ₀ < 0V	-20		
lok	Output parasitic diode current	V _o > V _{cc}	20	mA mA	
Ιο	Output current per output pin		±50	mA	
loc	Supply/GND current	V _{CC} , GND	±200	mA	
Pd	Power dissipation	(Not 2)	500	mW	
Tstg	Storage temperature range		−65~+150	τ	

Note 2 : M74HCT373-1FP, $T_a = -40 \sim +75 ^{\circ} C$ and $T_a = 75 \sim 85 ^{\circ} C$ are derated at $-7 mW/^{\circ} C$. M74HCT373-1DWP, $T_a = -40 \sim +80 ^{\circ} C$ and $T_a = 80 \sim 85 ^{\circ} C$ are derated at $-7 mW/^{\circ} C$.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85 °C)$

		Parameter			Limits				
Symbol	Par	Min	Тур	Max	Unit				
Vcc	Supply voltage		4.5		5. 5	٧			
V _i	Input voltage	0		Vcc	٧				
Vo	Output voltage				Vcc	٧			
Topr	Ambient operating temper	rature	-40		+85	င			
t _r , t _f Input risetime, fallt		V _{CC} = 4.5V	0		25	0			
	Input risetime, failtime	0		15	ns/V				

OCTAL 3-STATE NONINVERTING D-TYPE TRANSPARENT LATCH WITH LSTTL-COMPATIBLE INPUTS

ELECTRICAL CHARACTERISTICS ($v_{c\xi} = 5v \pm 10\%$, unless otherwise noted)

						Limits			
Symbol	Parameter		Test conditions Min		25℃		-40~+85°C		Unit
					Тур	Max	Min	Max	
VIH	High-level input voltage	$V_0 = 0.1V, V_{00}$ $ I_0 = 20\mu A$	$V_0 = 0.1V$, $V_{CC} = 0.1V$ $ I_0 = 20\mu A$				2.0		v
VIL	Low-level input voltage	$V_0 = 0.1V, V_0$ $ I_0 = 20\mu A$	$V_{\rm O} = 0.1 \text{V}, \ V_{\rm CC} - 0.1 \text{V}$ $V_{\rm O} = 20 \mu \text{A}$			0.8		0.8	v
V _{OH}	High-level output voltage	$V_i = V_{iL}$	$I_{OH} = -20\mu A$ $I_{OH} = -24mA, V_{CC} = 4.5V$	V _{cc} -0.1			V _{cc} -0.1		V
VoL	Low-level output voltage	$V_i = V_{iH}, \ V_{iL}$	$I_{OL} = 20 \mu A$ $I_{OL} = 24 mA, V_{CC} = 4.5 V$			0.1		0. 1 0. 5	٧
l _{IH}	High-level input current	$V_i = V_{CC}$				0.1		1.0	
l _{IL}	Low-level input current	V _I = GND				-0.1		-1.0	μA
lozh	Off-state high-level output current	$V_{i} = V_{iH}, \ V_{iL},$	$V_0 = V_{CC}$			0.5		5.0	
IozL	Off-state low-level output current	$V_I = V_{IH}, V_{IL}, V_O = GND$				-0.5		-5.0	μA
Icc	Quiescent supply current	VI = VCC, GND	$V_1 = V_{CC}$, GND, $I_0 = 0\mu A$			5.0		50.0	μА
ΔI_{CC}	Maximum quiescent supply current	$V_1 = 2.4V, 0.4$	V (Note 3)			2.7		2. 9	mA .

Note 3: Only one input is set at this value and all other inputs are fixed at V_{CC} or GND.

SWITCHING CHARACTERISTICS ($v_{cc} = 5v$, $\tau_a = 25^{\circ}C$)

		T . A		Limits			
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit	
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns	
t _{THL}	output transition time		,		10	ns	
t _{PLH}	Low-level to high-level and high-level to low-level	50 5(1) (5)			18	ns	
t _{PHL}	output propagation time (D — Q)	$C_L = 50 pF (Note 5)$			18	ns	
t _{PLH}	Low-level to high-level and high-level to low-level				21	ns	
t _{PHL}	output propagation time (LE - Q)				21	ns	
t _{PLZ}	Output disable time from low-level and high-level	C _L = 5 pF (Note 5)			20	ns	
t _{PHZ}	(OE - Q)	C _L = 5 pr (Note 5)			20	ns	
t _{PZL}	Output enable time to low-level and high-level	0 = 50-5 (N-4-5)			23	ns	
t _{PZH}	(OE - Q)	C _L = 50pF (Note 5)			23	ns	

SWITCHING CHARACTERISTICS ($v_{cc} = 5v \pm 10\%$, $\tau_a = -40 \sim +85\%$)

					Limits			
Symbol	Parameter	Test conditions	25℃			-40~+85℃		Unit
			Min	Тур	Max	Min	Max	}
t _{TLH}	Low-level to high-level and				12		15	
t _{THL}	high-level to low-level output transition time				12		15	ns
t _{PLH}	Low-level to high-level and high-level to low-level				20		25	ns
t _{PHL}	output propagation time (D - Q)				20		25	
t _{PLH}	Low-level to high-level and high-level to low-level	$C_1 = 50 \text{pF} \text{ (Note 5)}$		*	17		21	ns
t _{PHL}	output propagation time (LE - Q)	GE — SUPP (Note 5)			17		21	115
t _{PLZ}	Output disable time from				25		31	
	low-level and high-level						 	ns
t _{PHZ}	(OE - Q)				25		31	
t _{PZL}	Output enable time to				25	·	31	
t _{PZH}	low-level and high-level				25		31	- ns
Cı	Input capacitance				10		10	
Co	Off-state output capacitance	OE = V _{cc}			15		15	pF
C _{PD}	Power dissipation capacitance (Note 4)							1

Note 4: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per latch)
The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$

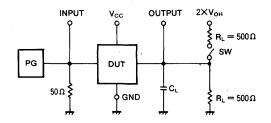


OCTAL 3-STATE NONINVERTING D-TYPE TRANSPARENT LATCH WITH LSTTL-COMPATIBLE INPUTS

TIMING REQUIREMENTS $(v_{cc} = 5v \pm 10\%, T_a = -40 \sim +85\%)$

					Limits			
Symbol	Parameter	Test conditions		25℃		-40~	+85℃	Unit
			Min	Тур	Max	Min	Max	1
t _w	Latch enable pulse with		12			15		ns
tsu	D setup time with respect to LE		10			13		ns
th	D hold time with respect to LE	N	5			6		ns

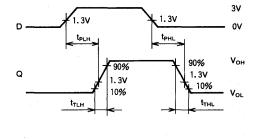
Note 4: Test Circuit

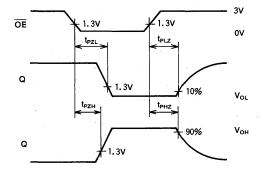


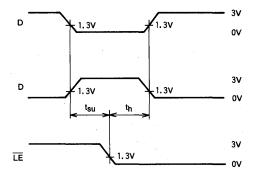
Parameter	sw			
t _{TLH} , t _{THL}	Open			
t _{PLZ}	Closed			
t _{PHZ}	Open			
t _{PZL}	Closed			
t _{PZH}	Open			

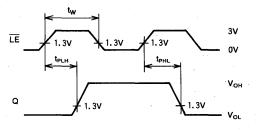
- (1) The pulse generator (PG) has the following characteristics (10%~90%): $\rm t_f=3ns,\,t_f=3ns$
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM









M74HC374P/FP/DWP

OCTAL 3-STATE NONINVERTING D-TYPE FLIP-FLOP

DESCRIPTION

The M74HC374 is a semiconductor integrated circuit consisting of eight positive-edge-triggered 3-state output D-type flip-flops with common clock and output-enable input.

FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: (Clock frequency) 65MHz typ.
 (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

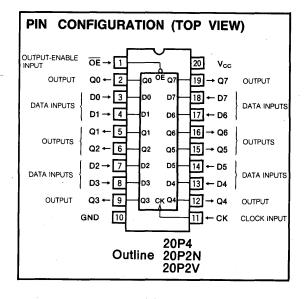
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC374 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS374.

The M74HC374 contains eight edge-triggered D-type flip-flops, sharing common clock input CK and output-enable input $\overline{\text{OE}}$.

When CK changes from low-level to high-level, the signals just previously input at D is stored in the flip-flop.

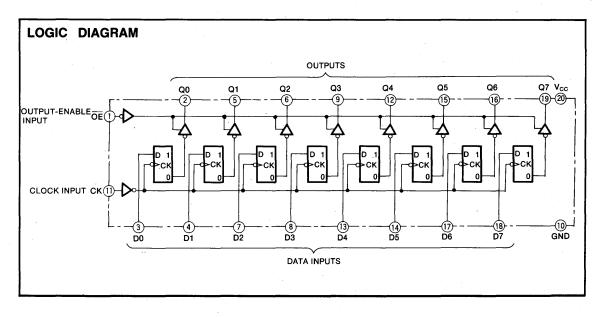
When OE is low, the signal stored in the flip-flop will be



output to Q.

When \overline{OE} is high, all outputs Q will become high-impedance state. The contents stored in the flip-flop will not be affected even if \overline{OE} changes.

A version of the M74HC374 with the same pin connections and an inverted output, the M74HC534, is also available.



OCTAL 3-STATE NONINVERTING D-TYPE FLIP-FLOP

FUNCTION TABLE (Note 1)

	Inputs				
OE	CK	D	Q		
L	†	L	- L		
L	t	Н	Н		
L	L	Х	Q°		
L	H	X	Qº		
L	1	X	Qº		
Н	×	Х	Z		

Note 1: Q^0 : Output state Q before clock input changed

Z : High inmpedance

X : Irrelevant

† : Change from low to high level

↓ : Change from high to low level

ABSOLUTE MAXIMUM RATINGS $(T_a = -40 \sim +85^{\circ}C)$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
	land and and all de annual	V ₁ < 0V	-20	
l _{IK}	Input protection diode current	$V_{\rm I} > V_{\rm CC}$	20	mA.
	0.4-4	V ₀ < 0V	-20	
lok	Output parasitic diode current	Vo > Vcc	20	mA
lo	Output current per output pin		±35	mA
Icc	Supply/GND current	V _{CC} , GND	±75	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65~+150	°C

Note 2 : M74HC374FP, $T_a=-40\sim+75^\circ$ C and $T_a=75\sim85^\circ$ C are derated at -7mW/°C. M74HC374DWP, $T_a=-40\sim+80^\circ$ C and $T_a=80\sim85^\circ$ C are derated at -7mW/°C.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85^{\circ}C)$

Symbol	Da.		<u> </u>	11-14		
Symbol	Pai	Parameter		Тур	Max	Unit
Vcç	Supply voltage		2		6	٧
V _i	Input voltage		0		Vcc	٧
Vo	Output voltage		0		Vcc	٧
Topr	Operating temperature ra	inge	-40		+85	°C-
		$V_{CC} = 2.0V$	0		1000	
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns
	i	$V_{CC} = 6.0V$	0		400	

M74HC374P/FP/DWP

OCTAL 3-STATE NONINVERTING D-TYPE FLIP-FLOP

ELECTRICAL CHARACTERISTICS

							Limits			
Symbol	Parameter	Test	conditions		25℃			-40~+85°C		Unit
				V _{cc} (V)	Min	Тур	Max	Min	Max	
		$V_0 = 0.1V, V_{CO}$	_0.11/	2.0	1.5			1.5		
V _{IH}	High-level input voltage	$ V_0 = 0.1V, V_{CO}$;0. 1 V	4.5	3. 15			3.15		V
		1161 — 20µA		6.0	4.2			4. 2		\
		Vo = 0.1V, Voc	-0.17	2.0			0.5		0.5	
VIL	Low-level input voltage	$ I_0 = 20\mu A$;U.1V	4.5			1. 35	1	1.35	V
		1161 - 20AA		6.0			1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
			$I_{OH} = -20\mu A$	4.5	4.4			4.4		
V _{OH}	High-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9		l	5.9		v
			$I_{OH} = -6.0 \text{mA}$	4.5	4.18			4.13		٠.
			$I_{OH} = -7.8 \text{mA}$	6.0	5. 68			5.63		
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	ļ
			$I_{OL} = 20 \mu A$	4.5			0.1		0.1	
VOL	Low-level output voltage	$V_{i} = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
		-	I _{OL} == 6.0mA	4.5			0. 26	1	0.33	ĺ
			I _{OL} = 7.8mA	6.0			0. 26		0.33	
I _{IH}	High-level input current	$V_i = 6V$		6.0			0.1		1.0	μA
Iլ∟ ′	Low-level input current	$V_l = 0V$		6.0			-0.1		-1.0	μΑ
lozh	Off-state high-level output current	$V_i = V_{iH}, \ V_{iL}, \ V_{iL}$	v _o = v _{cc}	6.0			0.5		5.0	μA
lozL	Off-state low-level output current	$V_i = V_{iH}, \ V_{iL}, \ V_{iL}$	o = GND	6.0			-0.5		-5. 0	μΑ
Icc	Quiescent supply current	VI = VCC, GND	$I_0 = 0 \mu A$	6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (Voc = 5V, Ta = 25°C)

Symbol	Parameter	Test conditions		Limits			
Symbor	Parameter 165t Continues		Min	Тур	Max	Unit	
fmax	Maximum clock frequency		35			MHz	
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns	
t _{THL}	output transition time	C _L = 50pF (Note 4)			10	ns	
t _{PLH}	Low-level to high-level and high-level to low-level				32	ns	
t _{PHL}	output propagation time (CK - Q)				32	ns	
t _{PLZ}	Output disable time from low-level and high-level	C _L = 5 pF (Note 4)			25	ns	
t _{PHZ}	(OE - Q)	CL = 5 pr (Note 4)			25	ns	
t _{PZL}	Output enable time to low-level and high-level	C = 50=5 (N=+= 4)			28	ns	
t _{PZH}	(OE - Q)	$C_L = 50 pF $ (Note 4)			28	ns	

OCTAL 3-STATE NONINVERTING D-TYPE FLIP-FLOP

SWITCHING CHARACTERISTICS $(V_{cc} = 2\sim6V, T_a = -40\sim+85^{\circ}C)$

					0580	Limits	. 40	Lorso	11-22
Symbol	Parameter	Test conditions			25℃	-	-40~		Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0	. 6	1		5		
fmax	Maximum clock frequency	C _L = 50pF (Note 4)	4.5	30			24		МН
			6.0	35	<u> </u>		28		
			2.0			60		75	
t _{TLH}	Low-level to high-level and		4.5			12		15	ns
	high level to leve level	C _L = 50pF (Note 4)	6.0			10		13	L
	high-level to low-level	CL — SOPP (Note 4)	2.0			60		75	
t _{THL}	output transition time		4.5		ĺ	12		15	ns
			6.0			10		13	
			2.0			180		227	
t _{PLH}			4.5			36		45	ns
			6.0			31		39	
	1 .	C _L = 50pF (Note 4)	2.0		 	180		227	
t _{PHL}	Low-level to high-level and		4.5			36		45	ns
'PHL	high-level to low-level		6.0		1	31		39	"
	output propagation time		2,0			230		290	
		· ·	4.5		-	46		58	ns
t _{PLH}	(CK - Q)		- 1		1	39		49	118
	-	C _L = 150pF (Note 4)	6.0		-		<u> </u>		
		· ·	2.0			230	· ·	290	
t _{PHL}			4.5			46		58	ns
<u> </u>			6.0			39		49	-
			2.0		}	150		189	
t _{PLZ}	Output disable time from		4.5			30		38	ns
	low-level and high-level	C _L = 50pF (Note 4)	6.0			26		32	
	1	or sobi (Mate 4)	2.0			150		189	
t _{PHZ}	(OE - Q)		4.5			30		38	ns
			6.0			26		32	
			2.0			150		189	
tezL			4.5			30		38	ns
		50 5 (1)	6.0			26		32	
	1	$C_L = 50pF (Note 4)$	2.0			150		189	
t _{PZH}	Output enable time to		4.5			30		38	ns
			6.0			26		32	1
	low-level and high-level		2.0			200		252	
t _{PZL}	(OE – Q)		4.5			40		50	ns
-F&L			6.0			34		43	'"
	-	C _L = 150pF (Note 4)	2.0		+	200		252	\vdash
t			4.5			40	,	50	ns
t _{PZH}			6.0			34		43	l as
	Land and side and		0.0		-				ļ
C ₁	Input capacitance Off-state output capacitance	OE = V _{CC}		-	· · · · · ·	10 15		10	pF pF
Co									

Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per flip-flop)

The power dissipated during operation under no-load conditions is calculated using the following formula:

P_D = C_{PD} • V_{CC}² • f₁+I_{CC} • V_{CC}

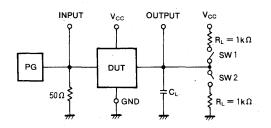


OCTAL 3-STATE NONINVERTING D-TYPE FLIP-FLOP

TIMING REQUIREMENTS ($V_{cc} = 2\sim 6V$, $T_a = -40\sim +85^{\circ}C$)

				Limits						
Symbol	Parameter	Test conditions			25℃		-40~	+85°C	Unit	
			V _{cc} (V)	Min	Тур	Max	Min	Max		
			2.0	80			101			
tw	Clock pluse width		4.5	16			20		ns	
			6.0	14			17	-]	
	D to the		2.0	75			90			
t _{su}	D setup time with		4.5	15			18		ns	
	respect to CK	·	6.0	13			16			
	D 5-14 4ii		2. 0	50			60			
th	D hold time with		4.5	10			12		ns	
	respect to CK		6.0	9			11			

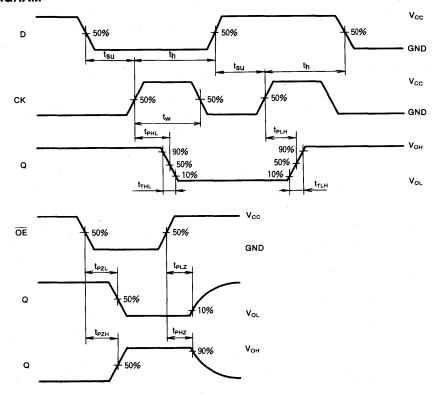
Note 4: Test Circuit



Parameter	SW 1	SW 2
t _{TLH} , t _{THL} t _{PLH} , t _{PHL}	Open	Open
t _{PLZ}	Closed	Open
t _{PHZ}	Open	Closed
t _{PZL}	Closed	Open
t _{PZH}	Open	Closed

- (1) The pulse generator (PG) has the following characteristics (10% \sim 90%): $t_f = 6ns$, $t_f = 6ns$
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





MITSUBISHI HIGH SPEED CMOS

M74HC374-1P/FP/DWP

OCTAL 3-STATE NONINVERTING D-TYPE FLIP-FLOP

DESCRIPTION

The M74HC374-1 is a semiconductor integrated circuit consisting of eight positive-edge-triggered 3-state output D-type flip-flops with common clock and output-enable input.

FEATURES

- High-fanout 3-state output: (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed: (clock frequency) 60MHz typ.
 (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 25μW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 60 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=-40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

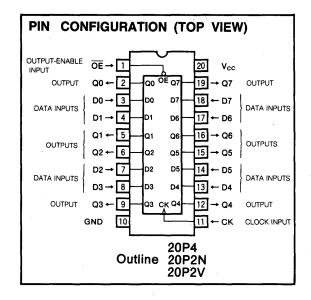
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC374-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series white giving high-speed performance equivalent to the 74LS374.

The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

The M74HC374-1 contains eight edge-triggered D-type flip-flops, sharing common clock input CK and output-enable input $\overline{\text{OE}}$.

When CK changes from low-level to high-level, the signals

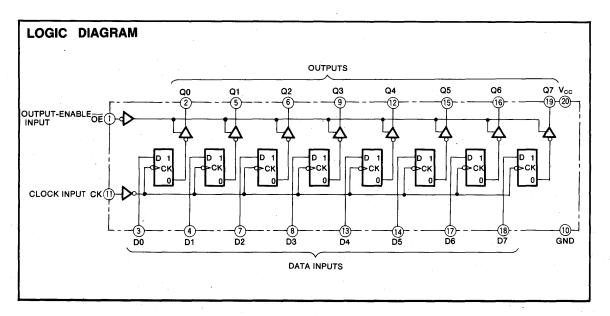


just previously input at D is stored in the flip-flop.

When $\overline{\text{OE}}$ is low, the signal stored in the flip-flop will be output to Q.

When \overline{OE} is high, all outputs Q will become high-impedance state. The contents stored in the flip-flop will not be affected even if \overline{OE} changes.

A version of the M74HC374-1 with the same pin connections and an inverted output, the M74HC534-1, is also available.



OCTAL 3-STATE NONINVERTING D-TYPE FLIP-FLOP

FUNCTION TABLE (Note 1)

	Inputs		
ŌĒ	СК	D	Q
L	. 1	L	L .
L	1	Н	Н
L	L	X	Q°
L	Н	X	Q٥
L	1	Х	Q°
Н	X	Χ.	Z

Note 1: Q0: Output state Q before clock input changed

Z : High inmpedance

X : Irrelevant

† : Change from low to high level ‡ : Change from high to low level

ABSOLUTE MAXIMUM RATINGS $(\tau_a = -40 \sim +85^{\circ}C)$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit	
Vcc	Supply voltage		-0.5~+7.0	V	
V ₁	Input voltage		-0.5~V _{cc} +0.5	V	
Vo	Output voltage		-0.5~V _{cc} +0.5	V	
	land was a state of the same of	V ₁ < 0V	-20		
İıK	Input protection diode current	$V_{i} > V_{CC}$	20	mA	
	0.4-4	V ₀ < 0V	-20		
ок	Output parasitic diode current	$v_o > v_{cc}$	20	mA mA	
lo	Output current per output pin		±50	mA .	
loc	Supply/GND current	V _{CC} , GND	±200	mA	
Pd	Power dissipation	(Note 2)	500	mW	
Tstg	Storage temperature range		−65∼+150	ဗ	

Note 2 : M74HC374-1FP, T_a = $-40\sim+75^{\circ}$ C and T_a = $75\sim85^{\circ}$ C are derated at -7mW/°C. M74HC374-1DWP, T_a = $-40\sim+80^{\circ}$ C and T_a = $80\sim85^{\circ}$ C are derated at -7mW/°C.

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85 \degree \text{C})$

Symbol	Parameter		-	Limits			
	Pa	Min	Тур	Max	Unit		
Vcc	Supply voltage	2		6	V		
V _i	Input voltage	0		V _{CC}	V		
V _o	Output voltage	0		Vcc	V		
Topr	Operating temperature ra	-40		+85	ဗ		
t _r , t _f	Input risetime, falltime	V _{CC} = 2.0V	. 0		500		
		V _{CC} = 4.5V	0		- 50	ns/V	
		$V_{CC} = 6.0V$	0		30]	

OCTAL 3-STATE NONINVERTING D-TYPE FLIP-FLOP

ELECTRICAL CHARACTERISTICS

Symbol	-	Test conditions $V_{CC}(V)$		Limits						
	Parameter			25°C			-40~+85°C		· Unit	
				Min	Тур	Max	Min	Max		
	High-level input voltage	$V_0 = 0.1V, V_{CC} = 0.1V$		2.0	1.5			1.5		v
V _{IH}				4.5	3. 15			3.15		
***				6.0	4.2		i	4. 2		
	Low-level input voltage	$V_0 = 0.1V, V_{CC} = 0.1V$ $ I_0 = 20\mu A$		2.0			0.5		0.5	v
VIL				4.5			1.35		1.35	
				6.0			1.8		1.8	
	High-level output voltage	$V_{l} = V_{lH}, V_{lL}$	$I_{OH} = -20\mu A$	2.0	1.9			1.9		V
			$I_{OH} = -20\mu A$	4.5	4.4			4.4		
V _{OH}			$I_{OH} = -20\mu A$	6.0	5.9			5.9		
			$I_{OH} = -24mA$	4.5	3. 98			3.84		
	Low-level output voltage	$V_{l} = V_{lH}, \ V_{lL}$	$I_{OL} = 20 \mu A$	2.0			0.1		0.1	v
			$I_{OL} = 20 \mu A$	4.5			0.1		0.1	
V _{OL}			$I_{OL} = 20 \mu A$	6.0			0.1	-	0. 1	
			I _{OL} = 24mA	4. 5			0.39		0.5	
I _{IH}	High-level input current	$V_1 = 6V$		6.0			0.1		1.0	μA
I _{IL}	Low-level input current	V ₁ = 0V		6.0			-0.1		-1.0	μΑ
I _{OZH}	Off-state high-level output current	$V_I = V_{IH}, V_{IL}, V_O = V_{CC}$		6.0			0.5		5.0	μΑ
lozL	Off-state low-level output current	$V_I = V_{IH}, \ V_{IL}, \ V_O = GND$		6.0			-0.5		-5. 0	μA
Icc	Quiescent supply current	$V_1 = V_{CC}$, GND, $I_0 = 0\mu A$		6.0			5.0		50.0	μA

SWITCHING CHARACTERISTICS ($v_{cc} = .5v$, $t_a = .25$ °C)

Symbol	Parameter 1	Test conditions	Limits			Linia
	Parameter	rest conditions	Min	Тур	Max	Unit
fmax	Maximum clock frequency		35			MHz
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time	C _L = 50pF (Note 4)			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level				20	ns
t _{PHL}	output propagation time (CK — Q)	· · · · · · · · · · · · · · · · · · ·			20	ns
t _{PLZ}	Output disable time from low-level and high-level	0 - 5 - 5 (N-1-4)			20	ns
t _{PHZ}	(OE – Q)	C _L = 5 pF (Note 4)			20	ns
t _{PZL}	Output enable time to low-level and high-level	0 = 50-5 (N-4-4)			23	ns
t _{PZH}	(OE - Q)	C _L = 50pF (Note 4)			23	ns

OCTAL 3-STATE NONINVERTING D-TYPE FLIP-FLOP

SWITCHING CHARACTERISTICS $(v_{cc} = 2\sim6v, \tau_a = -40\sim+85^{\circ}C)$

	1					Limits			
Symbol	Parameter	Test conditions			25℃		-40~	+85℃	Unit
		•	V _{cc} (V)	Min	Тур	Max	Min	Max]
			2.0	6			5		
fmax	Maximum clock frequency		4.5	32	1	1	26	1	мн
			6.0	38			31		
			2.0			60		75	
t _{TLH}	Low-level to high-level and		4.5		ļ	12		15	
	high lavel to lave lavel	*	6.0			10		13	
	high-level to low-level		2.0			60		75	ns
t _{THL}	output transition time		4.5			12		15	
	1		6.0			10		13	
			2.0			110		140	
t _{PLH}	Low-level to high-level and		4.5			22		28	
	high-level to low-level		6.0			19		24	
	output propagation time		2.0			110		140	ns
t _{PHL}	(CK - Q)	C _L = 50pF (Note 4)	4.5			22		28	
			6.0			19	=	24	
			2. 0			125		155	
t _{PLZ}	Output disable time from		4.5			25		31	
			6.0			21		26	
	low-level and high-level		2.0			125		155	ns
t _{PHZ}	(OE - Q)		4.5			25		31	
-			6.0			21		26	
*		•	2.0			125		155	
t _{PZL}	Output enable time to		4.5			25		31	
			6.0			21		26	
	low-level and high-level		2. 0			125		155	ns
t _{PZH}	(OE – Q)		4.5			25		31	
			6.0			21		26	
Cı	Input capacitance					10		10	
Co	Off-state output capacitance	OE = V _{CC}				15		15	pF
C _{PD}	Power dissipation capacitance (Note 3		<u> </u>			-			1

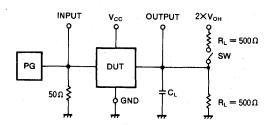
Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per flip-flop) The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS ($V_{cc} = 2\sim 6V$, $T_a = -40\sim +85^{\circ}C$)

						Limits			
Symbol	Parameter	Test conditions		25℃			-40~+85℃		Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max]
			2.0	60	,		75		
tw	Clock pluse width		4.5	12			15		ns
			6.0	10			13		
	D action the a with		2.0	50			65		
t _{su}	D setup time with		4.5	10	ļ		13		ns
*	respect to CK		6.0	9			11		1
			2.0	25			30		
th	D hold time with		4.5	5			6		ns
	respect to CK	•	6.0	5			`6		

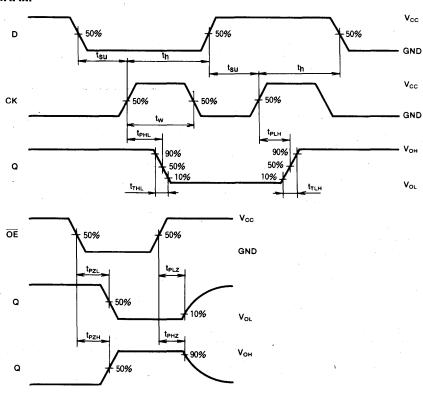
OCTAL 3-STATE NONINVERTING D-TYPE FLIP-FLOP

Note 4: Test Circuit



Parameter	sw
t _{TLH} , t _{THL}	Open
t _{PLZ}	Closed
t _{PHZ}	Open
t _{PZL}	Closed
t _{PZH}	Open

- (1) The pulse generator (PG) has the following characteristics (10% \sim 90%): $t_{\rm f}=3{\rm ns},\,t_{\rm f}=3{\rm ns}$
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.



M74HCT374-1P/FP/DWP

OCTAL 3-STATE
NONINVERTING D-TYPE FLIP-FLOP WITH LSTTL-COMPATIBLE INPUTS

DESCRIPTION

The M74HCT374-1 is a semiconductor integrated circuit consisting of eight positive-edge-triggered 3-state output D-type flip-flops with common clock and output-enable input.

FEATURES

- TTL level inputs V_{IL}=0.8V max, V_{IH}=2.0V mim
- High-fanout 3-state output: (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed: (Clock frequency) 55MHz typ.
 (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 25µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- Capable of driving 60 74LSTTL loads
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

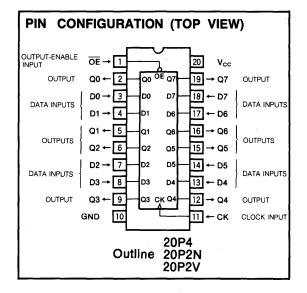
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HCT374-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS374.

The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

As the inputs are TTL level, the device can be used as a level converter from LSTTL to high-speed CMOS. In that case, no pull-up resistors are required.

The M74HCT374-1 contains eight edge-triggered D-type flip-flops, sharing common clock input CK and output-



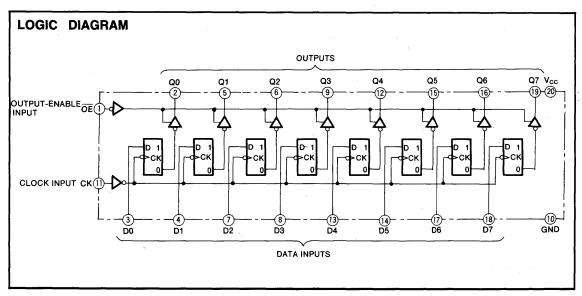
enable input OE.

When CK changes from low-level to high-level, the signals just previously input at D is stored in the flip-flop.

When \overline{OE} is low, the signal stored in the flip-flop will be output to Q.

When \overline{OE} is high, all outputs Q will become high-impedance state. The contents stored in the flip-flop will not be affected even if \overline{OE} changes.

A version of the M74HCT374-1 with the same pin connections and an inverted output, the M74HCT534-1, is also available.



OCTAL 3-STATE NONINVERTING D-TYPE FLIP-FLOP WITH LSTTL-COMPATIBLE INPUTS

FUNCTION TABLE (Note 1)

	Inputs			
ŌĒ	СК	D	Q	
L	1	L	L	
L	†	Н	Н	
L	L	X	Q°	
L	н	×	Q°	
L	1	X	Q°	
Н .	х	×	z	

Note 1 : Q°: Output state Q before clock input changed

Z : High inmpedance

X: Irrelevant

† : Change from low to high level

↓ : Change from high to low level

ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85$ °C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
	Input protection diode current	V ₁ < 0V	-20	
lik .	Input protection glode current V ₁ > V _{CC}		20	mA
	0.4.4	V ₀ < 0V	-20	
lok	Output parasitic diode current	Vo > Vcc	20	mA
l _o	Output current per output pin		±50	mA
loc	Supply/GND current	V _{CC} , GND	±200	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65~+150	င

Note 2 : M74HCT374-1FP, $T_a = -40 \sim +75^{\circ}C$ and $T_a = 75 \sim 85^{\circ}C$ are derated at -7mW/°C. M74HCT374-1DWP, $T_a = -40 \sim +80^{\circ}C$ and $T_a = 80 \sim 85^{\circ}C$ are derated at -7mW/°C.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85 \degree C)$

Symbol	D-		Limits			Unit	
	Pal	rameter	Min	Тур	Max	Unit	
V _{CC}	Supply voltage		4.5		5.5	V	
V _t	Input voltage		0		Vcc	٧	
V _o	Output voltage		0		Vcc	V	
Topr	Ambient operating tempe	erature	-40		+85	င	
t _r , t _f	Innut vinedine dellaine	$V_{CC} = 4.5V$	0	-	25	0	
	Input risetime, falltime Vcc = 5.5V		0		15	ns/V	

OCTAL 3-STATE NONINVERTING D-TYPE FLIP-FLOP WITH LSTTL-COMPATIBLE INPUTS

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, unless otherwise noted)

						Limits			
Symbol	Parameter	Test conditions		25℃			-40~+85°C		Unit
				Min	Тур	Max	Min	Max	
V _{IH}	High-level input voltage	$V_0 = 0.1V, V_0$ $ I_0 = 20\mu A$	$V_0 = 0.1V, \ V_{CC} = 0.1V$ $I_0 = 20\mu A$				2.0		٧
VIL	Low-level input voltage	$V_0 = 0.1V, V_0$ $ I_0 = 20\mu A$	c-0.1V			0.8		0.8	٧
· ·	Illah tarah ada da atau		$I_{OH} = -20\mu A$	V _{cc} -0.1			V _{cc} -0.1		v
V _{OH}	High-level output voltage $V_i = V_{iL}$	$V_i = V_{iL}$	$I_{OH} = -24 \text{mA}, \ V_{CC} = 4.5 \text{V}$	3, 98			3.84		, v
.,			$I_{OL} = 20\mu A$			0.1		0.1	.,
VoL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 24mA, V_{CC} = 4.5V$			0.39		0.5	V
I _{tH}	High-level input current	$V_i = V_{CC}$				0.1		1.0	
I _{IL}	Low-level input current	V _i = GND				0.1		-1.0	μA
I _{OZH}	Off-state high-level output current	$V_i = V_{iH}, \ V_{iL},$	$V_0 = V_{CC}$			0.5		5.0	
lozu	Off-state low-level output current	$V_i = V_{iH}, \ V_{iL},$	Vo = GND			-0.5		-5.0	μA
Icc	Quiescent supply current	VI = VCC, GNE	$0, \ l_0 = 0\mu A$			5.0		50.0	μΑ
Δlcc	Maximum quiescent supply current	$V_1 = 2.4V, 0.4$	V (Note 3)			2.7		2.9	mA

Note 3: Only one input is set at this value and all other inputs are fixed at V_{CC} or GND.

SWITCHING CHARACTERISTICS ($V_{cc} = 5V$, $T_a = 25$ °C)

Symbol	B	To a serial and		Limits		Unit
- Syllibol	Parameter	Test conditions	Min	Тур	Max	Oint
fmax	Maximum clock frequency		35			MHz
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time	C _L = 50pF (Note 5)			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level			,	20	ns
t _{PHL}	output propagation time (CK - Q)				20	ns
t _{PLZ}	Output disable time from low-level and high-level	0 - 5 - 5 (N-4-5)			20	ns
t _{PHZ}	(OE - Q)	$C_L = 5 pF (Note 5)$			20	ns
t _{PZL}	Output enable time to low-level and high-level	0 - 50-5 (N-4-5)			23	ns
t _{PZH}	(OE – Q)	C _L = 50pF (Note 5)			23	ns

SWITCHING CHARACTERISTICS ($V_{cc} = 5 \text{ V} \pm 10\%$, $T_a = -40 \sim +85 ^{\circ}\text{C}$)

			Limits					
Symbol	Parameter	Test conditions		25℃		-40~+85°C		Unit
			Min	Тур	Max	Min	Max	1
fmax	Maximum clock frequency		32			.26		MH
t _{TLH}	Low-level to high-level and	1			12		15	
tTHL	Low-level to high-level and high-level to low-level output transition time				12		15	ns
t _{PLH}	Low-level to high-level and high-level to low-level				22		28	
t _{PHL}	output propagation time (CK — Q)				22		28	ns
t _{PLZ}	Output disable time from	$C_L = 50 pF (Note 5)$		-	25		31	
t _{PHZ}	low-level and high-level				25		31	ns
t _{PZL}	Output enable time to				25		31	
t _{PŽH}	low-level and high-level (OE - Q)				25		31	ns
Cı	Input capacitance				10		10	
Со	Off-state output capacitance	OE = V _{CC}			15		15	рF
C _{PD}	Power dissipation capacitance (Note 4)							

Note 4: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per flip-flop)
The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$

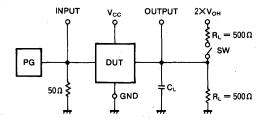


OCTAL 3-STATE NONINVERTING D-TYPE FLIP-FLOP WITH LSTTL-COMPATIBLE INPUTS

TIMING REQUIREMENTS ($V_{cc} = 5V \pm 10\%$, $T_a = -40 \sim +85\%$)

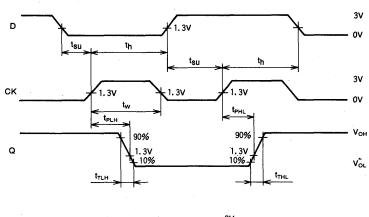
			Limits					
Symbol	Parameter	Test conditions		25℃		-40~	+85°C	Unit
		r .	Min	Тур	Max	Min	Max]
tw	Clock pluse width		12		-	15		ns ,
t _{su}	D setup time with respect to CK		10			13		ns
th	D hold time with respect to CK		5			6		ns

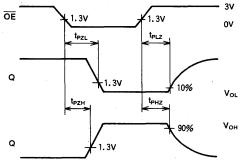
Note 5: Test Circuit



Parameter	SW
t _{TLH} , t _{THL}	Open
t _{PLZ}	Closed
t _{PHZ}	Open
t _{PZL}	Closed
t _{PZH}	Open

- (1) The pulse generator (PG) has the following characteristics (10% \sim 90%): $t_{\rm f}$ = 3ns, $t_{\rm f}$ = 3ns
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.





M74HC375P/FP/DP

DUAL 2-BIT TRANSPARENT LATCH

DESCRIPTION

The M74HC375 is a semiconductor integrated circuit consisting of four bistable latches with outputs Q and \overline{Q} .

FEATURES

- High-speed: 14ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 10µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

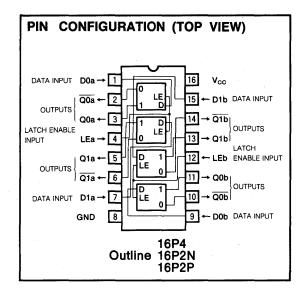
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC375 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS375.

The use of buffered outputs improves the input-to output transfer characteristics and minimizes output impedance variations with respect to input voltage variations.

The M74HC375 has four D-type latches, and is provided with enable inputs LE common to two circuits each. When LE is high, the infromation from the data input D will appear in the outputs Q and \overline{Q} . When the D signal changes, the signal that appears in outputs Q and \overline{Q} also will change. When LE changes from high to low, the status of D immediately before the change will be latched will LE is low, Q and \overline{Q} will not change even if D changes.

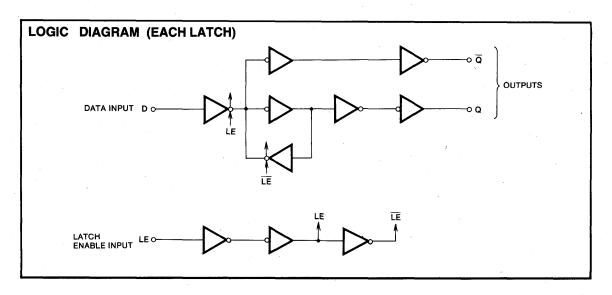
A unit, the M74HC75, having the same functions and electrical characteristics as the M74HC375 is also available.



FUNCTION TABLE (Note 1)

Inp	uts	Out	puts
LE	D	a	Q
Н	н	Н	L
Н	L	L	Н
L	х	Q٥	Q°

Note 1 : Q^0 , \overline{Q}^0 : Output state Q, \overline{Q} before input condition is set



DUAL 2-BIT TRANSPARENT LATCH

ABSOLUTE MAXIMUM RATINGS $(\tau_a = -40 \sim +85 ^{\circ}C, \text{ unless otherwise noted})$

Symbol	Parameter	Conditions	Ratings	Unit
Voc	Supply voltage		-0.5~+7.0	V
Vi	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	-V
		V ₁ < 0V	-20	
lik	Input protection diode current	$V_1 > V_{CC}$	20	mA
		V ₀ < 0V	-20	
ок	Output parasitic diode current	Vo > Vcc	20	mA mA
lo	Output current per output pin		±25	mA
Icc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65~+150	င

Note 2 : M74HC375FP, $T_a=-40\sim+70^\circ\text{C}$ and $T_a=70\sim85^\circ\text{C}$ are derated at -6mW/C. M74HC375DP, $T_a=-40\sim+50^\circ\text{C}$ and $T_a=50\sim85^\circ\text{C}$ are derated at -5mW/C.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85\%)$

Cumbal	Po Po			Unit		
Symbol	Pa	rameter	Min	Тур	Max	Unit
Vcc	Supply voltage		2		6	٧
Vı	Input voltage		0		Vcc	٧
Vo	Output voltage		0		Vcc	٧
Topr	Operating temperature ra	ange	40		+85	°
	Input risetime, falltime	V _{CC} = 2.0V	0		1000	
t _r , t _f		V _{CC} = 4.5V	0		500	ns
	$V_{CC} = 6.0V$		0		400	

ELECTRICAL CHARACTERISTICS

							Limits			
Symbol	Parameter	Test	conditions			25℃		−40 ~	+85℃	Unit
				V _{CC} (V)	Min	Тур	Max	Min	Max	
	/			2.0	1.5			1.5		
V _{IH}	High-level input voltage	$V_0 = 0.1V$, V_{CO}		4.5	3.15	, i		3. 15		v
		$ I_{O} = 20\mu A$		6.0	4.2	ļ		4.2		,
				2.0			0.5		0.5	
VIL	Low-level input voltage	$V_0 = 0.1V$, V_{C}	_0.1 V	4.5			1.35		1.35	.V
		$ 1_0 = 20 \mu A$	$ I_0 = 20\mu A$				1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
	High-level outnput voltage		$I_{OH} = -20\mu A$	4.5	4.4			4.4		
VoH		$V_{l} = V_{lH}, V_{lL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		l v
			$I_{OH} = -4.0 \text{mA}$	4.5	4. 18			4.13		
•			$I_{OH} = -5.2 \text{mA}$	6.0	5.68			5.63		
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
	*		$I_{OL} = 20 \mu A$	4.5			0.1		0.1	
V _{OL}	Low-level outnout voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	v
	•		i _{OL} = 4.0mA	4.5			0. 26		0.33	
			I _{OL} = 5. 2mA	6.0			0.26		0.33	,
l _{iH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μА
I _{IL}	Low-level input current	V₁ = 0V		6.0			-0.1		-1.0	μΑ
lcc	Quiescent supply current	VI = VCC, GNE	$I_0 = 0 \mu A$	6.0			2.0		20.0	μΑ

M74HC375P/FP/DP

DUAL 2-BIT TRANSPARENT LATCH

SWITCHING CHARACTERISTICS ($v_{cc} = 5v$, $\tau_a = 25^{\circ}C$)

Symbol	Parameter	Test conditions		Limits			
Symbol	Parameter	l est conditions	Min	Тур	Max	Unit	
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns	
t _{THL}	output transition time	·			10	ns	
t _{PLH}	Low-level to high-level and high-level to low-level	· ·	,		23	ns	
t _{PHL}	output propagation time (D - Q)				23	ns	
t _{PLH}	Low-level to high-level and high-level to low-level	C ₁ = 15pF (Note 4)			20	ns	
t _{PHL}	output propagation time $(D - \overline{Q})$	C _L = (Spr (Note 4)			20	ns	
t _{PLH}	Low-level to high-level and high-level to low-level				27	ns	
t _{PHL}	output propagation time (LE - Q)				27	ns	
t _{PLH}	Low-level to high-level and high-level to low-level				23	ns	
t _{PHL}	output propagation time (LE $-\overline{\mathbf{Q}}$)				23	ns	

SWITCHING CHARACTERISTICS $(V_{cc} = 2\sim6V, T_a = -40\sim+85^{\circ}C)$

						Limits			
Symbol	Parameter	Test conditions			25℃		-40~	+85℃	Unit
			V _{CC} (V)	Min	Тур	Max	Min	Max	
			2.0			75		95	
t _{TLH}	Low-level to high-level and		4.5			15	i	19	ns
	hist tourist tourist		6.0	1		13	1	16	l
	high-level to low-level		2.0			75		95	
t _{THL}	output transition time	1	4.5			15		19	ns
			6.0			13		16	
			2.0		-	125		156	
t _{PLH}	Low-level to high-level and		4. 5			25	1	32	ns
	high-level to low-level		6.0			21		27	
	output propagation time		2. 0			125		156	,
t _{PHL}	(D - Q)		4.5			25	1	32	ns
			6.0			21	1	27	
		1	2.0			110	1	138	
t _{PLH}	Low-level to high-level and		4.5			22		28	ns
	high-level to low-level	2 52 5 (11 1 1)	6.0			19		24	
	output propagation time	$C_L = 50 pF \text{ (Note 4)}$	2.0			110		138	
t _{PHL}	$(D - \overline{Q})$		4.5			22		28	ns
			6.0			19		24	
			2.0			145		181	
t _{PLH}	Low-level to high-level and		4.5			29		36	ns
	high-level to low-level		6.0			25		31	Í
	output propagation time		2.0			145		181	
t _{PHL}	(LE - Q)		4.5			29		36	ns
			6.0			25		31	
			2.0			125		156	
t _{PLH}	Low-level to high-level and		4.5			25	ĺ	31	ns
	high-level to low-level		6.0			22	1	28	
	output propagation time		2.0	_	1	125		156	
t _{PHL}	(LE - Q)		4. 5			25	1	31	ns
			6.0			22		28	
Cı	Input capacitance					10		10	pF
C _{PD}	Power dissipation capacitance (Note 3)				66				pF

Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per latch) The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$

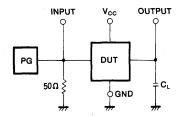


DUAL 2-BIT TRANSPARENT LATCH

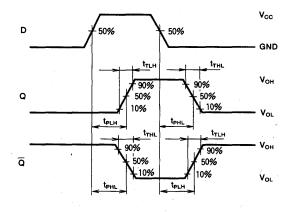
TIMING REQUIREMENTS ($V_{cc} = 2\sim 6V$, $T_a = -40\sim +85^{\circ}C$)

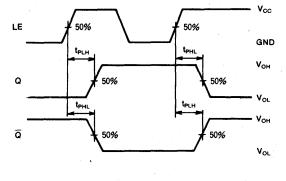
Symbol	Parameter	Test conditions		25°C			-40~+85℃		Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	7
			2.0	. 80			100		
tw	LE pulse width		4.5	16			20		ns
			6.0	14			18		
	Donatus Alexander		2.0	100			125		
tsu	D setup time with		4.5	20		ļ	25		ns
	respect to LE		6.0	17			21		
	D hold time with	1	2.0	5			5		
th			4.5	5		١ '	5		ns
	respect to LE		6.0	5			5		

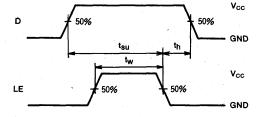
Note 4: Test Circuit



- (1) The pulse generator (PG) has the following characteristics (10%~90%): t_f = 6ns, t_f = 6ns
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.









MITSUBISHI HIGH SPEED CMOS M74HC377P/FP/DWP

OCTAL D-TYPE FLIP-FLOP WITH COMMON CLOCK AND ENABLE

DESCRIPTION

The M74HC377 is a semiconductor integrated circuit consisting of eight positive-edge triggered D-type flip flops with common clock and enable inputs.

FEATURES

- High-speed: (clock frequency)40MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2∼6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

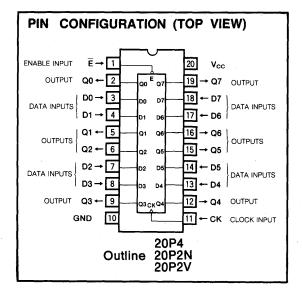
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC377 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS377.

The M74HC377 contains eight D-type flip flops with common clock and enable inputs.

When CK changes from low-level and high-level, the signals just previously input at D appears at outputs Q in accordance with function table given.

When \overline{E} is high, the output does not change, irrespective of other inputs. Changing \overline{E} from high to low, or from low to high does not cause misoperation.



FUNCTION TABLE (Note 1)

	Inputs		Output
E	СК	D	Q
Н	X	Х	Q°
L	1	Н	Н
L	1	L	L
X	L	X	Qº

Note 1: † : Change from low to high

Q0 : Output state Q before input conditions are set

X : Irrelevant

M74HC390P/FP/DP

DUAL 4-STAGE BINARY RIPPLE COUNTER WITH $\div 2$ AND $\div 5$ SECTIONS

DESCRIPTION

The M74HC390 is a semiconductor integrated circuit consisting of two asynchronous decade counters with direct reset input.

FEATURES

- High-speed: (clock frequency) 60MHz typ.
 (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85°C

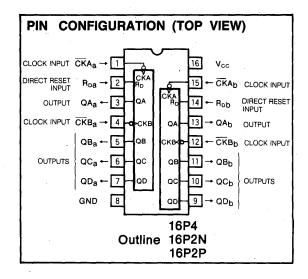
APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC390 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS390.

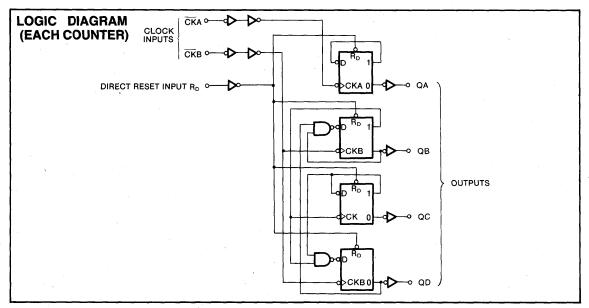
Each decade counter consists of a binary counter and a divide-by-5 counter. When using a binary counter, by applying the count pulse to clock input \overline{CKA} a frequency-demultiplied signal will be output to QA. When using a divide-by-5 counter, by applying the count pulse to clock input \overline{CKB} a frequency-demultiplied signal will be output to QB through QD.



When using the decade counter to output BCD code from QA through QD, connect QA and $\overline{\text{CKB}}$ together and apply the count pulse to $\overline{\text{CKA}}$. When outputting a signal with a 50% duty cycle from QA, connect QD and $\overline{\text{CKA}}$ together and apply the count pulse to $\overline{\text{CKB}}$.

Counting takes place when the clock input changes from high-level to low-level.

When direct reset input R_D is high, QA through QB will become low irrespective of other inputs. Maintain the low-level state when counting.



DUAL 4-STAGE BINARY RIPPLE COUNTER WITH $\div 2$ AND $\div 5$ SECTIONS

FUNCTION TABLE (Note 1)

	puts		Outputs					
СK	R _D	QA	QB	QC	QD			
х	Н	L -	L	L	L			
	L	Count						

Note 1 : ↓ : Change from high to low level

X : Irrelevant

Count number	QA	QB	QC	QD
0	L	L	L	L
1	Н	L	L	L
2	L	Н	L	L
3	Н	Н	L	L
4	L	L	Н	L
5	н	L	Н	L
6	L	Н	Н	L
7	Н	Н	Н	L
8	L	L	L	н
9	Н	L	L	Н

With QA and CKB connected and CKA used as input.

ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85 ^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
V _I _	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
	In a standard and the s	V ₁ < 0V	-20	
l _{iK}	Input protection diode current	V _I > V _{CC}	20	mA
	0.44	V ₀ < 0V	-20	
lok	Output parasitic diode current	Vo > Vcc	20	mA.
l _o	Output current per output pin		±25	mA
Icc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65~+150	°C

Note 2 : M74HC390FP, T $_a$ = $-40\sim+70^\circ$ C and T $_a$ = $70\sim85^\circ$ C are derated at -6mW/°C. M74HC390DP, T $_a$ = $-40\sim+50^\circ$ C and T $_a$ = $50\sim85^\circ$ C are derated at -5mW/°C.

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85 \degree C)$

Complete	Parameter			Limits					
Symbol	Pa	rameter	Min	Тур	Max	Unit			
V _{CC}	Supply voltage	Supply voltage			6	V			
Vı	Input voltage		0		Vcc	V			
Vo	Output voltage		0		V _{cc}	V			
Topr	Operating temperature ra	ange	-40		+85	°C			
		$V_{CC} = 2.0V$. 0		1000				
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns			
		0		400					

DUAL 4-STAGE BINARY RIPPLE COUNTER WITH +2 AND +5 SECTIONS

ELECTRICAL CHARACTERISTICS

							Limits			
Symbol	Parameter	Tes	t conditions			25℃		-40~	+85℃	Unit
				V _{CC} (V)	Min	Тур	Max	Min	Max	
		V = 0.1V V	0.11/	2.0	1.5			1.5		
VIH	High-level input voltage		$V_0 = 0.1V$, $V_{CC} = 0.1V$		3. 15]		3.15	1:	v
	1	$ I_0 = 20\mu A$		6.0	4.2			4.2		
		V = 0.1V V	$V_0 = 0.1V, V_{CC} = 0.1V$				0.5		0.5	
V _{IL}	Low-level input voltage		5—0. (V	4. 5	1	1	1.35		1.35	V
	•	$ I_O = 20\mu A$		6.0	Ì	1	1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
			$I_{OH} = -20\mu A$	4.5	4.4			4.4	l	į
VoH	High-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9	1		5.9	l	v
			$I_{OH} = -4.0 \text{mA}$	4.5	4. 18			4.13		
			$I_{OH} = -5.2 mA$	6.0	5. 68			5.63	l	
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
			$I_{OL} = 20 \mu A$	4.5			0.1	Į	0.1	
VOL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1	Į	0.1	V
	*	,	I _{OL} = 4.0mA	4.5			0.26		0.33	
			$I_{OL} = 5.2 \text{mA}$	6.0			0.26		0.33	
t _{IH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μA
l _{IL}	Low-level input current	V ₁ = 0V		6.0			-0.1		-1.0	μA
loc	Quiescent supply current	VI = VCC, GND	$I_0 = 0 \mu A$	6.0			4.0		40.0	μΑ

SWITCHING CHARACTERISTICS ($V_{cc} = 5V$, $T_a = 25^{\circ}$)

Combal	Parameter	Test conditions	Limits			Unit
Symbol	Parameter	1 est conditions	Min	Тур	Max	Unit
fmax	Maximum clock frequency		30			MHz
t _{TLH}	Low-level to high-level and high-level to low-level	·			10	ns
t _{THL}	output transition time				10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	1			20	ns
t _{PHL}	output propagation time (CKA - QA)				20	ns
t _{PLH}	Low-level to high-level and high-level to low-level output				50	ns
t _{PHL}	propagation time (CKA — QC, with QA and CKB connected)				50	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = 15pF (Note 4)			21	กร
t _{PHL}	output propagation time (CKB - QB)	·			21	ns
t _{PLH}	Low-level to high-level and high-level to low-level				32	ns
t _{PHL}	output propagation time (CKB — QC)				32	ns
t _{PLH}	Low-level to high-level and high-level to low-level	• •			21	ns
t _{PHL}	output propagation time (CKB - QD)				21	ns
	High-level to low-level output propagation time				28	ns
t _{PHL}	(RD - QA, QB, QC, QD)				20	115

DUAL 4-STAGE BINARY RIPPLE COUNTER WITH $\div 2$ AND $\div 5$ SECTIONS

SWITCHING CHARACTERISTICS $(v_{cc} = 2\sim6v, T_a = -40\sim+85\%)$

Symbol	Parameter	Test conditions			25℃		-40~	+85°C	Unit
Cymbo	raiametei	rest conditions	V _{cc} (V)	Min	1	Max	Min	Max	1
	·				Тур	Wax	4	IVIAX	-
_			2.0	5			-		
fmax	Maximum clock frequency		4.5	27			21		МН
			6.0	31			24		
			2.0			75		95	
t _{TLH}	Low-level to high-level and		4.5			15		19	ns
	blab tassalka lassitassal		6.0			13		16	[
	high-level to low-level		2.0			75		95	
t _{THL}	output transition time		4.5		1	15		19	ns
			6.0			13		16	
			2.0			120		150	
	Low-level to high-level and		4.5		1	24		30	ns
t _{PLH}	1				1				115
	high-level to low-level		6.0		ļ	21		26	
	output propagation time	•	2.0		ŀ	120		150	
t _{PHL}	(CKA - QA)	·	4.5			24		30	ns
			6.0			21		26	
			2.0			290		360	
t _{PLH}	Low-level to high-level and		4.5			58		72	ns
	high-level to low-level		6.0		1	50		62	İ
	output propagation time		2.0			290		360	1
t _{PHL}	(CKA - QC, with QA and CKB connected)		4.5		1	58		72	ns
YPHL	(515) 25, 1111 27, 2115 5115 5511150527		6.0			50		62	
			2.0			130		160	
	Law lawel to blab lawel and	C _L = 50pF (Note 4)	4.5		1	26		33	ns
t _{PLH}	Low-level to high-level and								l lis
	high-level to low-level		6.0			22		28	-
	output propagation time		2.0		1	130		160	
t _{PHL}	(CKB — QB)	· ·	4.5		ľ	26		33	ns
			6.0			22		28	
	*		2.0			185		230	
t _{PLH}	Low-level to high-level and	9	4.5			37		46	ns
	high-level to low-level	*	6.0		1	32		40	
	output propagation time	-	2.0			185		230	
t _{PHL}	(CKB - QC)		4.5		}	37		46	ns
-PHL	,	·	6.0		1	32		40	
			2.0			130		160	 -
	1 114- 6/-6 11 1		i i	~		ſ		1	1
t _{PLH}	Low-level to high-level and		4.5			26		33	ns
	high-level to low-level		6.0			22		28	
	output propagation time		2.0			130		160	
t _{PHL}	(CKB — QD)	•	4.5			26		33	ns
			6.0			22		28	1
	High-level to low-level		2.0			165		210	
t _{PHL}	output propagation time		4.5			33		41	ns
	(RD - QA, QB, QC, QD)		6.0		İ	28		35	1
Cı	Input capacitance			-		10		10	pF
<u> </u>	Power dissipation capacitance (Note 3)				46	 10		- ' -	ρF

Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per counter) The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$

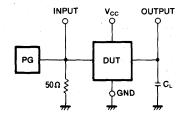


DUAL 4-STAGE BINARY RIPPLE COUNTER WITH $\div 2$ AND $\div 5$ SECTIONS

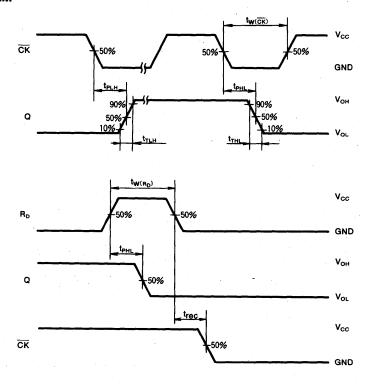
TIMING REQUIREMENTS ($V_{cc} = 2\sim 6V$, $T_a = -40\sim +85^{\circ}C$)

						Limits			
Symbol	Parameter	Test conditions			25℃		-40~	+85℃	Unit
L			V _{cc} (V)	Min	Тур	Max	Min	Max	
}			2.0	80			100		
tw(ok)	Clock pulse width		4.5	16			20	1.0	ns
			6.0	14			18	L]
			2.0	80			100		
t _{W(RD)}	Direct reset pulse width		4.5	16			20		ns
]			6.0	14			18		
	B and a south time with		2.0	50			65		
trec	R _D recovery time with respect to CK		4.5	10		i	13		ns
	respect to CK		6.0	9			11	Ì	<u> </u>

Note 4: Test Circuit



- (1) The pulse generator (PG) has the following
- characteristics $(10\% \sim 90\%)$: $t_r = 6$ ns, $t_f = 6$ ns (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.



MITSUBISHI HIGH SPEED CMOS

M74HC393P/FP/DP

DUAL 4-STAGE BINARY RIPPLE COUNTER

DESCRIPTION

The M74HC393 is a semiconductor integrated circuit consisting of two asynchronous 4-bit binaly (hexadecimal) counters with direct reset input.

FEATURES

- High-speed: (clock frequency) 60MHz typ.
 (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85°C

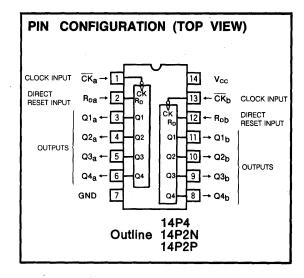
APPLICATION

General purpose, for use in industrial and consumer digital equipment.

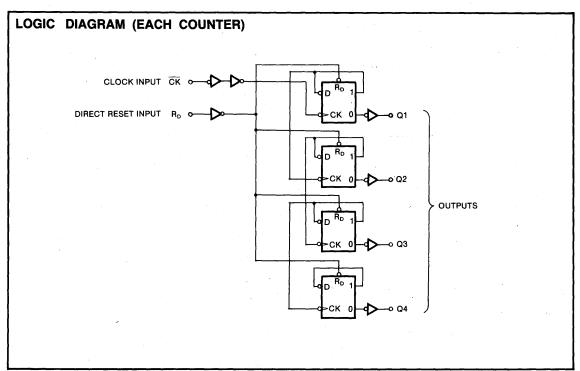
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC393 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS393

When the count pulse is applied to clock input \overline{CK} , a binary code will be output to Q1 through Q4. Counting takes place



when the clock input changes from high-level to low-level. When direct reset input R_D is high, Q1 through Q4 will become low irrespective of other inputs. Maintain the low-level state when counting.





DUAL 4-STAGE BINARY RIPPLE COUNTER

FUNCTION TABLE (Note 1)

Inp	outs	Outputs					
CK	R₀	Q1	Q2	Q3	Q4		
×	Н	L.	L	L	L		
+	L		Co	unt			

Note $1:\downarrow$: Change from high to low level

X : Irrelevant

Count number	Q1	Q2	Q3	Q4
0	L	L	L	L
1	Н	L	L	L
2	L	Н	L	L
3	H	Н	L	L
4	L	L	Ŧ	L
5	Н	L	H	٦
6	L	Н	Н	٦
7	Н	Н	Н	L
8	L	L	L	Н
9	Н	L	L	Н
10	L	Н	L	Н
11	Н	Н	L	Н
12	L	L	H	Н
13	Н	L	н	н
14	L	Н	Н	Н
15	Н	Н	Н	Н

ABSOLUTE MAXIMUM RATINGS $(T_a = -40 \sim \pm 85 \degree C)$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
	land and all all all all all all all all all al	V ₁ < 0V	20	T
I _{IK}	Input protection diode current	$V_1 > V_{CC}$	20	mA
,	Cutant assessment disades assessed	V ₀ < 0V	20	
Ток	Output parasitic diode current	Vo > Vcc	20	mA
lo	Output current per output pin		±25	mA
lcc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		-65~+150	ဗ

Note 2 : M74HC393FP, T $_a$ = $-40\sim$ +60°C and T $_a$ = 60 \sim 85°C are derated at -6mW/°C. M74HC393DP, T $_a$ = $-40\sim$ +50°C and T $_a$ = 50 \sim 85°C are derated at -5mW/°C.

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85 ^{\circ}C)$

Ob. ad	Parameter			Limits				
Symbol	Pai	raiametei			Max	Unit		
Vcc	Supply voltage	2		6	٧			
Vı	Input voltage	0		Vcc	٧			
Vo	Output voltage	0		V _{CC}	٧			
Topr	Operating temperature ra	inge	-40		+85	°C		
		$V_{CC} = 2.0V$	0		1000			
tr, tf	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns		
	$V_{CC} = 6.0V$. 0		400			

M74HC393P/FP/DP

DUAL 4-STAGE BINARY RIPPLE COUNTER

ELECTRICAL CHARACTERISTICS

			-				Limits			
Symbol	Parameter	Test	conditions			25℃		-40~	+85°C	Unit
			V _{cc} (V)		Min	Тур	Max	Min	Max	1
		$V_0 = 0.1V, V_{CC}$	-0.1V	2.0	1.5			1.5		
V_{IH}	High-level input voltage	$ I_0 = 20\mu A$	3-0. TV	4.5	3.15			3.15		V
		Πο1 — 20μΑ		6.0	4.2			4.2		
		$V_0 = 0.1V, V_{C}$	-0 1V	2.0			0.5		0.5	
VIL	Low-level input voltage	$ V_0 = 0.1V$, V_{CI}	c—0.1 V	4.5			1.35	1	1.35	V
		1101 - 20μΑ		6.0			1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
		1	$I_{OH} = -20\mu A$	4.5	4. 4			4. 4	1	
V_{OH}	High-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		V
	-		$I_{OH} = -4.0 \text{mA}$	4.5	4. 18	-		4. 13		
	<u> </u>	_	$I_{OH} = -5.2 \text{mA}$	6.0	5.68			5.63		
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
			$I_{OL} = 20 \mu A$	4.5			0. 1	i	0.1	
VoL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
			I _{OL} = 4.0mA	4.5			0.26		0.33	[
			I _{OL} = 5. 2mA	6.0			0.26		0. 33	
l _{IH}	High-level input current	V _I = 6V		6.0			0.1		1.0	μA
I _{IL}	Low-level input current	$V_1 = 0V$		6.0			<u>-0.1</u>		-1.0	μА
lcc	Quiescent supply current	VI = VCC, GND	$I_0 = 0 \mu A$	6.0			4.0	,	40.0	μА

SWITCHING CHARACTERISTICS $(V_{CC} = 5V, T_a = 25\%)$

O. mark and	Parameter	Test conditions		Unit		
Symbol	Parameter	lest conditions	Min	Ťур	Max	Unit
fmax	Maximum clock frequency		30			MHz
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time	·			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level				20	ns
t _{PHL}	output propagation time (CK-Q1)	·			20	ns
t _{PLH}	Low-level to high-level and high-level to low-level	0 = 15=5 (Note 4)			35	ns
t _{PHL}	output propagation time (CK-Q2)	$C_L = 15pF (Note 4)$			35	ns
t _{PLH}	Low-level to high-level and high-level to low-level] .			42	ns
t _{PHL}	output propagation time (CK-Q3)				42	ns
t _{PLH}	Low-level to high-level and high-level to low-level				50	ns
t _{PHL}	output propagation time (CK-Q4)				50	ns
	High-level to low-level output propagation time	1			20	
t _{PHL}	(R _D -Q1, Q2, Q3, Q4)				28	ns

DUAL 4-STAGE BINARY RIPPLE COUNTER

SWITCHING CHARACTERISTICS ($V_{cc} = 2\sim6V$, $T_a = -40\sim+85^{\circ}C$)

						Limits			1
Symbol	Parameter	Test conditions V _{CC} (V)			25°C			+85℃	Unit
				Min	Тур	Max	Min	Max	1
			2.0	5		-	4		
fmax	Maximum clock frequency		4.5	27]`.		. 21		MHz
	Ì		6.0	31	l		24	1	ì
			2.0			75		95	
t _{TLH}	Low-level to high-level and		4.5			15		19	ns
			6.0]		13		16	İ
	high-level to low-level		2.0			75		95	
t _{THL}	output transition time	·	4.5		į.	15	1	19	ns
	İ		6.0			13		16	
		·	2.0			120		150	
t _{PLH}	Low-level to high-level and	,	4.5		ì	24		30	ns
	high-level to low-level		6.0	1	}	21	}	26	
	output propagation time		2.0			120		150	
t _{PHL}	(CK-Q1)		4.5			24		30	ns
	1		6.0		}	21	1	26	
			2.0			190		240	
t _{PLH}	Low-level to high-level and	·	4.5	l		38		47	ņs
4	high-level to low-level	50 500 0	6.0			32		40	
	output propagation time	C _L = 50pF (Note 4)	2.0			190		240	1
t _{PHL}	(CK-Q2)		4.5	1		38	1	47	ns
			6.0		ļ	32	(40	,
		1	2. 0	7		240		300	
t _{PLH}	Low-level to high-level and		4.5	1		48	1	60	ns
	high-level to low-level		6.0		1	41		51	
	output propagation time		2.0			240	1	300	
t _{PHL}	(CK _Q3)		4. 5		1	. 48		60	ns
	•		6.0]	Ì	41		51	İ
	,	1	2.0	T		290		360	
t _{PLH}	Low-level to high-level and		4.5			58	İ	72	ns
	high-level to low-level		6.0			50		62	
	output propagation time		2.0			290		360	
t _{PHL}	(CK-Q4)		4.5		1	58	1	72	ns
			6.0			50		62	1
	High-level to low-level	1	2.0		Ţ	165		210	T
t _{PHL}	output propagation time	ì	4.5	. :		33	1, 1	41	ns
	(R _D -Q1, Q2, Q3, Q4)		6.0		1	28		35	
Cı	Input capacitance				1.	10		10	pF
C _{PD}	Power dissipation capacitance (Note 3)				41		,	T	pF

Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per counter)

The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$

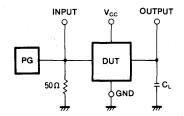


DUAL 4-STAGE BINARY RIPPLE COUNTER

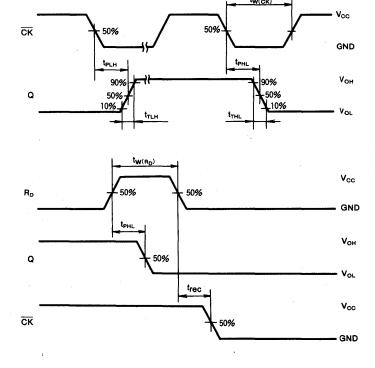
TIMING REQUIREMENTS ($v_{cc} = 2\sim 6v$, $T_a = -40\sim +85^{\circ}C$)

		·				Limits			
Symbol	Parameter	Test conditions			25℃		−40~	+85℃	⊍nit
	· · · · · · · · · · · · · · · · · · ·		V _{cc} (V)	Min	Тур	Max	Min	Max	<u> </u>
			2.0	80			100		
tw(CK)	Clock pulse width		4.5	16			20		ns
			6.0	14	1		18		
			2.0	80			100		
t _{W(RD)}	Direct reset pulse width		4.5	16			20	1	ns
			6.0	14			18		
			2.0	50		-	65		
trec	R _D recovery time with	. *	4.5	10	1		13		ns
	respect to CK		6.0	9			11		

Note 4: Test Circuit



- (1) The pulse generator (PG) has the following characteristics (10%~90%): t_f = 6ns, t_f = 6ns
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.



M74HC533P/FP/DWP

OCTAL 3-STATE INVERTING D-TYPE TRANSPARENT LATCH

DESCRIPTION

The M74HC533 is a semiconductor integrated circuit consisting of eight 3-state output D-type latches with common latch-enable input and output-enable input.

FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=-6mA)
- High-speed: 13ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=-40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

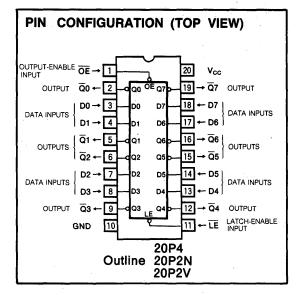
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC533 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS533.

The M74HC533 contains of eight D-type latch with latchenable input $\overline{\text{LE}}$ and output-enable input $\overline{\text{OE}}$ common to all circuits.

When $\overline{\text{LE}}$ is high, the signals of data input D will go through the latch and be output to inverted output \overline{Q} . When the state of D changes, the state of \overline{Q} will also change. When $\overline{\text{LE}}$ changes from high-level to low-level, the data existing immediately prior to the change at D will be stored in the latch.

Even if other inputs are changed when $\overline{\text{LE}}$ is low, the contents stored in the latch will not be affected.



When \overline{OE} is high, all outputs \overline{Q} will become high-impedance state.

A version of the M74HC533 with the same pin connections and a noninverted output, the M74HC373, is also available.

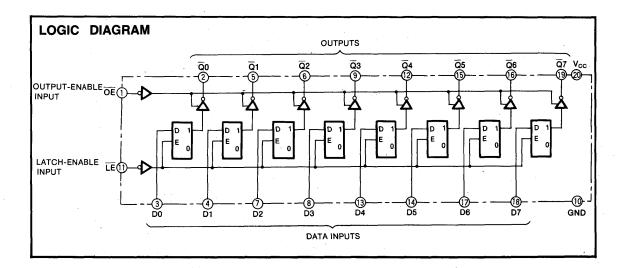
FUNCTION TABLE (Note 1)

	Inputs		Output
OE	LE	D	Q
L	Н	Н	L
L	Н	L	н
L	L	X	Q٥
Н	×	х	Z

Note 1: Q0: Output state Q before LE changed

Z : High impedance

X : Irrelevant



ABSOLUTE MAXIMUM RATINGS $(T_a = -40 \sim +85 \degree$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V.
V _i	Input voltage		-0.5~V _{cc} +0.5	V
Vo .	Output voltage		-0.5~V _{cc} +0.5	V
	Insula must satisfy diads summed	V ₁ < 0V	-20	^
lik	Input protection diode current	V _I > V _{CC}	20	mA
		V ₀ < 0V	-20	
Іок	Output parasitic diode current	Vo > Vcc	20	mA.
lo	Output current per output pin		±35	mA
lcc	Supply/GND current	V _{CC} , GND	±75	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		-65~+150	°C

Note 2 : M74HC533FP, T $_a=-40\sim+75^\circ$ C and T $_a=75\sim85^\circ$ C are derated at -7mW/°C. M74HC533DWP, T $_a=-40\sim+80^\circ$ C and T $_a=80\sim85^\circ$ C are derated at -7mW/°C.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85 ^{\circ}C)$

Cumala al	Parameter			11-14		
Symbol	Pai	rai ai iletei		Тур	Max	Unit
Vcc	Supply voltage	Supply voltage			6	٧
V _I	Input voltage		0		Vcc	· V
Vo	Output voltage		0		Vcc	٧
Topr	Operating temperature ra	inge	-40		+85	ဗ
		$V_{CC} = 2.0V$	0		1000	
t _r , t _f	Input risetime, failtime	$V_{CC} = 4.5V$	0		500	ns
	$V_{CC} = 6.0V$		0		400	

ELECTRICAL CHARACTERISTICS

							Limits			
Symbol	Parameter	Test	conditions			25℃		-40~+85°C		Unit
				V _{cc} (V)	Min	Тур	Max	Min	Max	
		$V_0 = 0.1V, V_{CC}$	0.11/	2.0	1.5			1.5		
ViH	High-level input voltage	$ V_0 - 0.1V, V_{CO} $	5—0.1 V	4.5	3.15			3. 15		V
		1101 - 20µA		6.0	4. 2			4. 2		
	-	V =0.1V V	-0.1V	2.0			0.5		0.5	
VIL	Low-level input voltage	$ V_0 = 0.1V, V_{CO}$ $ I_0 = 20\mu A$	$V_0 = 0.1V, V_{CC} - 0.1V$, -		1.35]	1.35	V
		1161 20µA		6.0			1.8		1.8	
	V_{OH} High-level output voltage $V_i = V_{IH_1} \cdot V_{IL}$		$I_{OH} = -20\mu A$	2.0	1.9			1.9		
		$I_{OH} = -20\mu A$	4.5	4. 4			4.4	ŀ		
V _{OH}		$V_i = V_{iH}, V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		V
			$I_{OH} = -6.0 mA$	4.5	4.18			4.13		
		-	$I_{OH} = -7.8 mA$	6.0	5.68			5.63		
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
	†		$I_{OL} = 20 \mu A$	4.5			0.1		0.1	
VoL	Low-level output voltage	$V_{i} = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
			I _{OL} = 6.0mA	4.5			0. 26		0.33	
			I _{OL} = 7.8mA	6.0			0, 26		0.33	
Ін	High-level input current	$V_1 = 6V$		6.0			0.1		1.0	μA
. I₁∟	Low-level input current	V ₁ = 0V		6.0			-0. 1		-1.0	μA
lozh	Off-state high-level output current	$V_i = V_{iH}, \ V_{iL}, \ V_{iL}$	$v_0 = v_{cc}$	6.0			0.5		5.0	μA
lozL	Off-state low-level output current	$V_i = V_{iH}, \ V_{iL}, \ V_{iL}$	V _O = GND	6.0		ļ	-0.5		-5.0	μA
loc	Quiescent supply current	VI = VCC, GND	$I_0 = 0\mu A$	6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS ($V_{cc} = 5V$, $T_a = 25^{\circ}C$)

Symbol	Parameter	Test conditions		Unit		
Symbol	Farameter	rest conditions	Min	Тур	Max	Unit
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time				10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C ₁ = 50pF (Note 4)			25	ns
t _{PHL}	output propagation time $(D - \overline{Q})$	CL = 50pr (Note 4)			25	ns
t _{PLH}	Low-level to high-level and high-level to low-level				30	ns
t _{PHL}	output propagation time $(\overline{LE} - \overline{Q})$				30	ns
t _{PLZ}	Output disable time from low-level and high-level	C _L = 5 pF (Note 4)			25	ns
t _{PHZ}	$(\overline{OE} - \overline{Q})$	CL — 5 pr (Note 4)			25	ns
t _{PZL}	Output enable time to low-level and high-level	C ₁ = 50pF (Note 4)			28	ns
t _{PZH}	$(\overline{OE} - \overline{Q})$	CL — 50pF (Note 4)			28	ns

SWITCHING CHARACTERISTICS $(v_{cc} = 2\sim6v, \tau_a = -40\sim+85\%)$

Symbol	Paramatas	Tost conditions			25℃	Limits	40	-+85°C	Unit
Symbol	Parameter	Test conditions	14 (14)			 -			- 0"
	<u> </u>		V _{cc} (V)	Min	Тур	Max	Min	Max	-
	1		2.0			60		75	
t _{TLH}	Low-level to high-level and		4.5			12		15	ns
	high-level to low-level	$C_L = 50pF (Note 4)$	6.0			10		13	
			2.0			60		75	
^Ì тн∟	output transition time		4.5			12		15	n:
	-	2	6.0			10		13	
		·	2.0			150		189	
PLH			4.5			30		38	n
		$C_L = 50 pF (Note 4)$	6.0			26		32	<u> </u>
		1 - 1	2, 0		1	150		189	
PHL	Low-level to high-level and		4.5		}	30	-	38	n
	high-level to low-level		6.0			26		32	ļ
	output propagation time		2.0			200		252	
PLH	(D-Q)		4.5			40		50	n
		$C_L = 150 pF (Note 4)$	6.0			34		43	
		OL 13001 (14006 4)	2.0			200		252	
PHL			4.5			40		50	n
			6.0			34		43	l
			2.0			175		221	
PLH			4.5		[35		44	n
		0 - 50-5 (N-1-4)	6.0			30		37	
	1	$C_L \approx 50 \text{pF} \text{ (Note 4)}$	2.0			175		221	
PHL	Low-level to high-level and		4.5			35		44	l n
	high-level to low-level		6.0		Ì	30		37	1
_	output propagation time		2.0			225		284	
PLH	(<u>LE</u> - Q)		4.5			45		57	n
			6.0			38		48	1
	1	C _L = 150pF (Note 4)	2.0			225		284	
PHL			4.5			45		57	n
PHL			6.0			38		48	1. "
			2.0			150		189	+
	Output disable time from		4.5		1	30		38	1
PLZ	Output disable time from	·	6.0			26		32	1 "
	low-level and high-level	$C_L = 50 pF \text{ (Note 4)}$	2, 0		 	150		189	+-
	$(\overline{OE} - \overline{Q})$		4.5		1	30	·	38	
PHZ	(Oz = Q)	1	6.0		}	26		38	n
						150		189	+
			2.0		1 .				_
PZL			4.5			30		38	n
	-	$C_L = 50 pF \text{ (Note 4)}$	6.0			26		32	
		1	2.0			150		189	1
PZH	Output enable time to		4.5			30		38	n
	low-level and high-level		6.0		<u> </u>	26		32	
			2.0			200		252	1
PZL	$(\overline{OE} - \overline{Q})$		4.5		1	40		50	n
		C _L = 150pF (Note 4)	6.0			34		43	<u> </u>
		- 100pi (110to 17)	2.0			200		252	
PZH			4.5			40		50	n
	<u> </u>		6.0			34		43	
) _ı	Input capacitance					10		10	р
٥-	Off-state output capacitance	OE = V _{CC}				15		15	р
PD	Power dissipation capacitance (Note 3				57				P

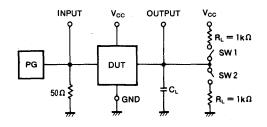
Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per latch) The power dissipated during operation under no-load conditions is calculated using the following formula: $P_{D} = C_{PD} \cdot V_{CC}^2 \cdot f_{1} + I_{CC} \cdot V_{CC}$



TIMING REQUIREMENT ($v_{cc} = 2\sim 6v$, $\tau_a = -40\sim +85^{\circ}$ C)

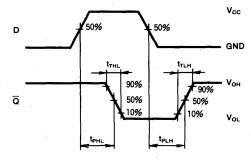
		Test conditions		Limits					
Symbol	Parameter			25℃			-40~+85°C		Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	
1.		,	2.0	80			101		
tw	Latch enable pulse width	le pulse width	4.5	16			20		ns
			6.0	14	1	· ·	17	Ì	'
	D and an Aliman with		2.0	75			90		
tsu	D setup time with respect to LE		4.5	15	}	}	18	1	ns
	respect to LE	· ·	6.0	13			16		
	D hold time with		2.0	50			60		
th	respect to LE		4.5	10			12	Ì	ns
			6.0	9			11		

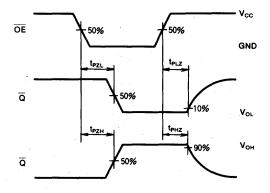
Note 4: Test Circuit

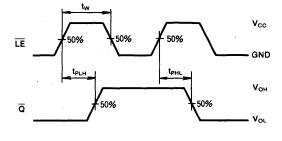


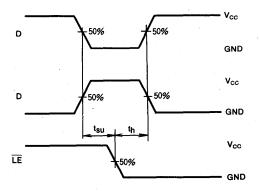
Parameter	SW1	SW 2
t _{TLH} , t _{THL}	Open	Open
t _{PLZ}	Closed	Open
t _{PHZ}	Ореп	Closed
t _{PZL}	Closed	Open
t _{PZH}	Open	Closed

- (1) The pulse generator (PG) has the following
- characteristics (10% \sim 90%): $t_{\rm f}$ = 6ns, $t_{\rm f}$ = 6ns (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.









MITSUBISHI HIGH SPEED CMOS

M74HC533-1P/FP/DWP

OCTAL 3-STATE INVERTING D-TYPE TRANSPARENT LATCH

DESCRIPTION

The M74HC533-1 is a semiconductor integrated circuit consisting of eight 3-state output D-type latches with common latch-enable input and output-enable input.

FEATURES

- High-fanout 3-state output: (I_{OL}=24mA, I_{OH}=-24mA)
- High-speed: 9ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 25µW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 60 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

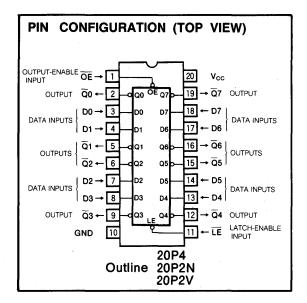
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC533-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS533.

The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

The M74HC533-1 consists of eight D-type latches with latch-enable input $\overline{\text{DE}}$ and output-enable input $\overline{\text{OE}}$ common to all circuits.

When \overline{LE} is high, the signals of data input D will go through the latch and be output to inverted output \overline{Q} . When the state of D changes, the state of \overline{Q} will also change. When

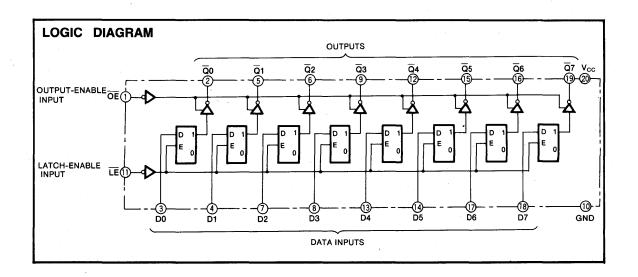


LE changes from high-level to low-level, the data existing immediately prior to the change at D will be stored in the latch.

Even if other inputs are changed when $\overline{\text{LE}}$ is low, the contents stored in the latch will not be affected.

When \overline{OE} is high, all outputs \overline{Q} will become high-impedance state.

A version of the M74HC533-1 with the same pin connections and a noninverted output, the M74HC373-1, is also available.



FUNCTION TABLE (Note 1)

	Inputs		Output
ŌĒ	LÉ	D	Q
L	H :	Н	L
L	Н	L	Н
L	L	Х	Q°
Н	X	X	Z

Note 1 : $\overline{\mathbb{Q}}^0$: Output state $\overline{\mathbb{Q}}$ before $\overline{\mathsf{LE}}$ changed Z : High impedance X : Irrelevant

ABSOLUTE MAXIMUM RATINGS $(T_a = -40 \sim +85 ^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit	
Vcc	Supply voltage		−0.5~+7.0	V	
Vı	Input voltage		-0.5~V _{cc} +0.5	V	
Vo	Output voltage	4	-0.5~V _{cc} +0.5	V	
	Input protection diode current	V ₁ < 0V	-20		
lik .		V _I > V _{CC}	20	mA.	
		V ₀ < 0V	-20		
lok	Output parasitic diode current	$v_o > v_{cc}$	20	mA	
lo	Output current per output pin		±50	mA.	
Icc	Supply/GND current	V _{CC} , GND	±200	- mA	
Pd	Power dissipation	(Note 2)	500	mW	
Tstg	Storage temperature range		-65∼+150	င	

Note 2 : M74HC533-1FP, T_a = $-40\sim+75$ °C and T_a = $75\sim85$ °C are derated at -7mW/°C. M74HC533-1DWP, T_a = $-40\sim+80$ °C and T_a = $80\sim85$ °C are derated at -7mW/°C.

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85 \degree)$

Complete at	Parameter			Limits				
Symbol			Min	Тур	Max	Unit		
Vcc	Supply voltage		2		6	V		
Vı	input voltage		0		Vcc	V		
Vo	Output voltage		0		Vcc	V		
Topr	Operating temperature ra	inge	40		+85	°C		
		$V_{CC} = 2.0V$	0		500			
t _f , tf	input risetime, falltime	$V_{CC} = 4.5V$	0		50	ns/V		
	$V_{CC} = 6.0V$		0		30			

ELECTRICAL CHARACTERISTICS

					Limits					
Symbol	Parameter	Test	conditions	,	25℃			-40~+85°C		Unit
		V _{cc} (V)		Min	Тур	Max	Min	Max		
		$V_0 = 0.1V, V_{CO}$	-0.1V	2.0	1.5		1	1.5		
V _{IH}	High-level input voltage	$ I_0 = 20\mu A$;0. 1 v	4.5	3.15			3.15		V
		1101 - 20µA		6.0	4.2		1	4.2		
		$V_0 = 0.1V, V_{CC} - 0.1V$		2.0			0.5		0.5	
VIL	Low-level input voltage		;U. 1 V	4.5			1.35		1.35	٧
		$ I_{O} = 20\mu A$		6.0			1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		v
	High lavel autout value	$V_{l} = V_{lH}, V_{lL}$	$I_{OH} = -20\mu A$	4.5	4.4			4.4		
V _{OH}	High-level output voltage		$I_{OH} = -20\mu A$	6.0	5.9	*		5.9		
			$I_{OH} = -24mA$	4.5	3. 98			3.84		
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
	I am lamal and and and and and	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	4.5			0.1		0, 1	
Vol	Low-level output voltage	VI - VIH, VIL	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
			I _{OL} = 24mA	4.5			0.39		0.5	
l _{ie}	High-level input current	$V_i = 6V$		6.0			0.1		1.0	μА
l _{IL}	Low-level input current	$V_i = 0V$		6.0			-0.1		-1.0	μА
I _{OZH}	Off-state high-level output current	$V_i = V_{iH}, \ V_{iL}, \ V_{iL}$	$V_{l} = V_{lH}, \ V_{lL}, \ V_{O} = V_{CC}$				0.5		5.0	μΑ
lozL	Off-state low-level output current	$V_i = V_{iH}, \ V_{iL}, \ V_{iL}$	o = GND	6.0			-0.5		-5. 0	μA
Icc	Quiescent supply current	VI = VCC, GND	$V_i = V_{CC}$, GND, $I_O = 0\mu A$				5.0		50.0	μA

SWITCHING CHARACTERISTICS $(V_{cc} = 5V, T_a = 25\%)$

	·			Limits			
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit	
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns	
t _{THL}	output transition time				10	ns	
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = 50pF (Note 4)			18	ns	
t _{PHL}	output propagation time (D \overline{Q})				18	ns	
t _{PLH}	Low-level to high-level and high-level to low-level				21	ns	
t _{PHL}	output propagation time $(\overline{LE} - \overline{Q})$	·			21	ns	
t _{PLZ}	Output disable time from low-level and high-level	C ₁ = 5 pF (Note 4)	-		20	ns	
t _{PHZ}	$(\overline{OE} - \overline{Q})$	CL — 5 pr (Note 4)			20	ns	
t _{PZL}	Output enable time to low-level and high-level	C ₁ = 50pF (Note 4)			23	ns	
t _{PZH}	(OE - Q)	CL — SOPE (NOIE 4)			23	ns	

SWITCHING CHARACTERISTICS ($V_{cc} = 2\sim6V$, $T_a = -40\sim+85$ °C)

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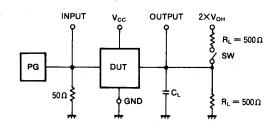
Symbol	Parameter	Test conditions			25℃.	Limits	-40~	+85℃	Unit
Symbol	raianielei	V _{CC} (V)		Min	Тур	Max	Min	Max	01111
·	 		2.0	· · · · · · · · · · · · · · · · · · ·	170	60	- *****	75	
•	Low-level to high-level and		4.5			12	,	15	
t _{TLH}	LOW-level to high-level and	· ·	6.0			10		13	
	high-level to low-level		2.0			60		75	ns
	output transition time		4.5	1 1		12		15	
t _{THL}	output transition time		6.0			10		13	
			2.0			100		125	
	Low-level to high-level and		4.5			20		25	
t _{PLH}	high-level to low-level		6.0			17		25	
	⊣ ~		2, 0			100		125	. ns
. / "	output propagation time $(\mathbf{p} - \overline{\mathbf{Q}})$		4.5			20		25	
t _{PHL}	(D - Q)		6.0			17	,	25 21	
			2.0			115		145	
			4.5			23			
t _{PLH}	Low-level to high-level and		1 .			20		29	
	high-level to low-level	C _L = 50pF (Note 4)	6.0					25	ns
_	output propagation time		2.0			115	ľ	145	
t _{PHL}	(IE - Q)		4.5			23		29	
			6.0			20		25	
		3	2.0			125		155	
t _{PLZ}	Output disable time from		4.5			25		31	
	low-level and high-level		6.0			21		26	ne
		1	2.0			125		155	
t _{PHZ}	$(\overline{OE} - \overline{Q})$		4.5			25		31	
			6.0			21		26	
			2.0			125		155	ļ
t _{PZL}	Output enable time to		4.5			25	ŀ	31	
	low-level and high-level		6.0			21		26	ns
			2.0			125		155	'''
t _{PZH}	$(\overline{OE} - \overline{Q})$	•	4.5			25	1	31	
			6.0			21		26	ļ
Cı	Input capacitance					10		10	1
Со	Off-state output capacitance	OE = V _{CC}	1	-		15		15	pF
CPD	Power dissipation capacitance (Note 3								1

Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per latch)
The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENT ($v_{cc} = 2\sim 6V$, $T_a = -40\sim +85^{\circ}C$)

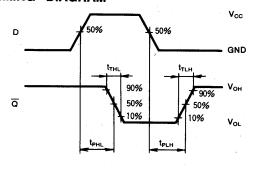
						Limits			
Symbol	bol Parameter Test conditions	Test conditions		25℃			-40~	Unit	
		V _{cc} (V)	Min	Тур	Max	Min	Max		
			2.0	60			75		
tw	Latch enable pulse width		4.5	12			15	ļ	ns
			6.0	10			13	,	1
	D setup time with]	2.0	50			65		
tsu	respect to LE	* * *	4.5	10			13		ns
	respect to LE	,	6.0	9			- 11 .	}	
	D hold time with		2.0	25			30		
th	D hold time with respect to LE		4.5	5			6		ns
	respect to LE		6.0	5			6		

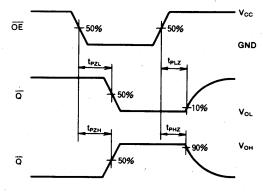
Note 4: Test Circuit

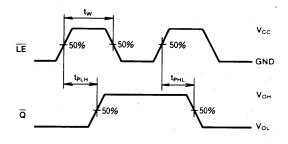


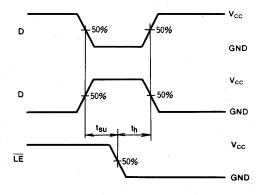
Parameter	sw
t _{TLH} , t _{THL}	Open
t _{PLZ}	Closed
t _{PHZ}	Open
t _{PZL}	Closed
t _{PZH}	Open

- (1) The pulse generator (PG) has the following characteristics (10% \sim 90%): $t_r = 3$ ns, $t_f = 3$ ns (2) The capacitance C_L includes stray wiring
- capacitance and the probe input capacitance.











M74HCT533-1P/FP/DWP

OCTAL 3-STATE INVERTING
D-TYPE TRANSPARENT LATCH WITH LSTTL-COMPATIBLE INPUT

DESCRIPTION

The M74HCT533-1 is a semiconductor integrated circuit consisting of eight 3-state output D-type latches with common latch-enable input and output-enable input.

FEATURES

- TTL level inputs V_{IL}=0.8V max, V_{IH}=2.0V min
- High-fanout 3-state output: (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed: 11ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 25µW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- Capable of driving 60 74LSTTL loads
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

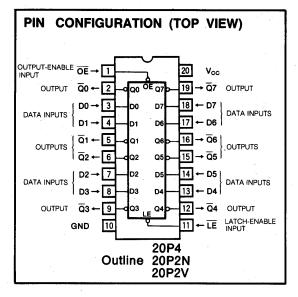
Use of silicon gate technology allows the M74HCT533-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS533.

The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

As the inputs are TTL level, the device can be used as a level converter from LSTTL to high-speed CMOS. In that case, no pull-up resistors are required.

The M74HCT533-1 contains of eight D-type latch with latch-enable input $\overline{\text{LE}}$ and output-enable input $\overline{\text{OE}}$ common to all circuits.

When LE is high, the signals of data input D will go through the latch and be output to inverted output \overline{Q} . When the state of D changes, the state of \overline{Q} will also change. When $\overline{\text{LE}}$ changes from high-level to low-level, the data existing

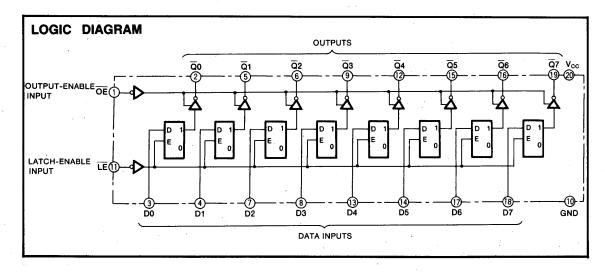


immediately prior to the change at D will be stored in the latch.

Even if other inputs are changed when $\overline{\text{LE}}$ is low, the contents stored in the latch will not be affected.

When \overline{OE} is high, all outputs \overline{Q} will become high-impedance state.

A version of the M74HCT533-1 with the same pin connections and a noninverted output, the M74HCT373-1, is also available.



OCTAL 3-STATE INVERTING D-TYPE TRANSPARENT LATCH WITH LSTTL-COMPATIBLE INPUT

FUNCTION TABLE (Note 1)

	Inputs		Output
ŌĒ	LE	D	Q
Ł	н	Н	L
L	н	L	н
L	L	Х	Q°
Н	×	X	Z

Note 1: Qo: Output state Q before LE changed

Z : High impedance

X : Irrelevant

ABSOLUTE MAXIMUM RATINGS $(\tau_a = -40 \sim +85 \degree\text{C}, \text{ unless otherwise noted})$

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
V ₁	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
		V ₁ < 0V	-20	
ŀк	Input protection diode current	V _I > V _{CC}	20	mA .
,	0	V ₀ < 0V	-20	
lok	Output parasitic diode current	Vo > Vcc	20	mA
lo	Output current per output pin		±50	mA
Icc	Supply/GND current	V _{CC} , GND	±200	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range	,	−65~+150	ొ

Note 2 : M74HCT533-1FP, $T_a=-40\sim+75^\circ$ C and $T_a=75\sim85^\circ$ C are derated at $-7mW/^\circ$ C. M74HCT533-1DWP, $T_a=-40\sim+80^\circ$ C and $T_a=80\sim85^\circ$ C are derated at $-7mW/^\circ$ C.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85 \%)$

				Limits		11-14
Symbol	Pai	rameter	Min	Тур	Max	Unit
V _{CC}	Supply voltage		4.5		5.5	V
Vı	Input voltage		. 0		V _{CC}	V
Vo	Output voltage		0		Vcc	V
Topr	Ambient operating temper	erature	40		+85	င
		$V_{CC} = 4.5V$	0		25	01
t _r , t _f	Input risetime, falltime		0		15	ns/V

OCTAL 3-STATE INVERTING D-TYPE TRANSPARENT LATCH WITH LSTTL-COMPATIBLE INPUT

ELECTRICAL CHARACTERISTICS ($v_{cc} = 5V \pm 10\%$, unless otherwise noted)

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		-				Limits			
Symbol Parameter		Test conditions		25℃			-40~+85℃		Unit
				Min	Тур	Max	Min	Max	ĺ
V _{IH}	High-level input voltage	$V_0 = 0.1V, V_{00}$ $ I_0 = 20\mu A$	$V_{\rm O} = 0.1 \text{V}, \ V_{\rm CC} - 0.1 \text{V}$ $V_{\rm O} = 20 \mu \text{A}$				2.0		V,
ViL	Low-level input voltage	$V_0 = 0.1V, V_0$ $ I_0 = 20\mu A$	_c -0.1V			0.8		0.8	V
		V - V	$I_{OH} = -20\mu A$	V _{cc} -0.1			V _{cc} -0.1		·v
V _{OH}	High-level output voltage	$V_{l} = V_{lL}$	$I_{OH} = -24 \text{mA}, \ V_{CC} = 4.5 \text{V}$	3.98			3.84		
·	Law law lawas and a second	V - V V	$I_{OL} = 20 \mu A$			0.1		0.1	v
Vol	Low-level output voltage	$V_i = V_{iH}, V_{jL}$	I _{OL} = 24mA, V _{CC} = 4.5V			0.39		0.5	, ,
I _{IH}	High-level input current	V _I = V _{CC}				0.1		1.0	
IIL	Low-level input current	V _I = GND				-0.1		-1.0	μA
lozH	Off-state high-level output current	$v_{i} = V_{iH}, \ V_{iL}, \ V_{o} = V_{CC} $ 0.5 5.		5.0					
lozL	Off-state low-level output current	$V_i = V_{iH}, \ V_{iL},$	V _O = GND			-0.5		-5.0	μA
loc	Quiescent supply current	VI = VCC, GNE	$0, I_0 = 0\mu A$			5.0		50.0	μA
Δlcc	Maximum quiescent supply current	$V_1 = 2.4V, 0.4$	V (Note 3)			2.7		2.9	mA

Note 3: Only one input is set at this value and all other inputs are fixed at V_{CC} or GND.

SWITCHING CHARACTERISTICS ($v_{cc} = 5v$, $\tau_a = 25^{\circ}C$)

Combal	Parameter Test conditions			Limits		Unit
Symbol	Parameter	lest conditions	Min	Тур	Max	Unit
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time				10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = 50pF (Note 5)			18	ns
t _{PHL}	output propagation time (D \overline{Q})				18	ns
t _{PLH}	Low-level to high-level and high-level to low-level				21	ns
t _{PHL}	output propagation time $(\overline{LE} - \overline{Q})$				21	ns
t _{PLZ}	Output disable time from low-level and high-level	C _L = 5 pF (Note 5)			20	ns
t _{PHZ}	$(\overline{OE} - \overline{Q})$	CL = 5 pr (Note 5)			20	ns
t _{PZL}	Output enable time to low-level and high-level	C _L = 50pF (Note 5)			23	ns
t _{PZH}	(OE - Q)	OL — Supr (Note 5)			23	กร

SWITCHING CHARACTERISTICS ($v_{cc} = 5v \pm 10\%$, $T_a = -40 \sim +85\%$)

					Limits			
Symbol	Parameter	Test conditions		25℃		-40~+85℃		Unit
			Min	Тур	Max	Min	Max	
t _{TLH}	Low-level to high-level and				12		15	
t _{THL}	high-level to low-level output transition time				12		15	ns
t _{PLH}	Low-level to high-level and high-level to low-level				20		25	
t _{PHL}	output propagation time (D — Q)				20		25	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = 50pF (Note 5)			23		29	ns
t _{PHL}	output propagation time (LE - Q)	CL — SOPP (Note 5)			23		29	lis
t_{PLZ}	Output disable time from				25		31	
t _{PHZ}	low-level and high-level (OE - Q)		1		25		31	ns
t _{PZL}	Output enable time to low-level and high-level				25		31	
t _{PZH}	(OE - Q)			,	25		31	ns
Cı	Input capacitance				10		10	
Со	Off-state output capacitance	OE = V _{CC}			15		15	рF
C _{PD}	Power dissipation capacitance (Note 4)							1

Note 4: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per latch)

The power dissipated during operation under no-load conditions is calculated using the following formula:

P_D = C_{PD} • V_{CC}² • f₁+I_{CC} • V_{CC}

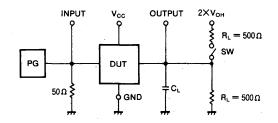


OCTAL 3-STATE INVERTING D-TYPE TRANSPARENT LATCH WITH LSTTL-COMPATIBLE INPUT

TIMING REQUIREMENTS ($v_{cc} = 5v \pm 10\%$, $T_a = -40 \sim +85^{\circ}$)

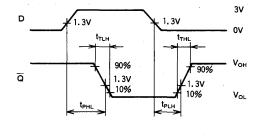
Symbol Parameter		Test conditions		25℃		-40~+85°C		Unit
			Min	Тур	Max	Min	Max	
tw	Latch enable pluse width		12			15		ns
tsu	D setup time with respect to LE		10			13		ns
th	D hold time with respect to LE		5			6		ns

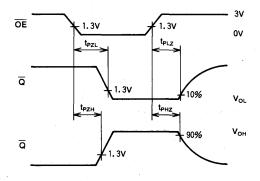
Note 5: Test Circuit

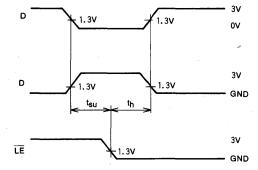


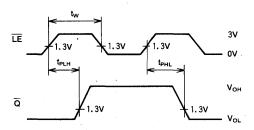
Parameter	sw
t _{TLH} , t _{THL}	Open
t _{PLZ}	Closed
t _{PHZ}	Open
t _{PZL}	Closed
t _{PZH}	Open

- (1) The pulse generator (PG) has the following characteristics (10% \sim 90%): $t_r = 3$ ns, $t_f = 3$ ns (2) The capacitance C_L includes stray wiring
- capacitance and the probe input capacitance.









MITSUBISHI HIGH SPEED CMOS

M74HC534P/FP/DWP

OCTAL 3-STATE INVERTING D-TYPE FLIP-FLOP

DESCRIPTION

The M74HC534 is a semiconductor integrated circuit consisting of eight edge-triggered 3-state output D-type flip-flops with common clock input and output-enable input.

FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 13ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{cc}=2~6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

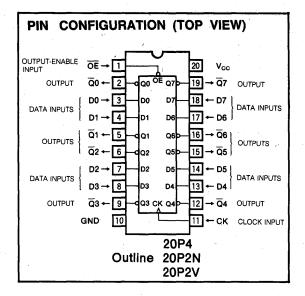
Use of silicon gate technology allows the M74HC534 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS534.

The M74HC534 contains eight edge-triggered D-type flip-flops, sharing common clock input CK and output-enable input $\overline{\text{OE}}$.

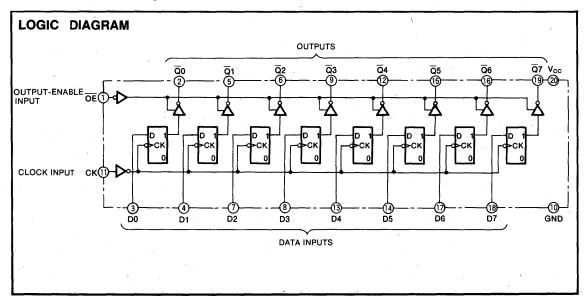
When CK changes from low-level to high-level, the signals just previously input at D is stored in the flip-flop.

When output-enable input \overline{OE} is low, the signals stored in the flip-flop will be output to \overline{Q} .

When OE is high, all outputs \overline{Q} will become high-impedance state. The contents stored in the flip-flop are not affected even if \overline{OE} is changed.



A version of the M74HC534 with the same pin connections and a noninverted output, the M74HC374, is also available.



FUNCTION TABLE (Note 1)

	Inputs		Output
OE	СК	D	Q
L	1	L	Н
L	1	Н	L
L	L	X.	Q°.
L	Н	X	Q٥
L	1	×	Q°
Н	×	X	Z

Note 1 : \overline{Q}^0 : Output state \overline{Q} before clock input changed Z : High impedance

X : Irrelevant

† : Change from low to high level

↓ : Change from high to low level

ABSOLUTE MAXIMUM RATINGS ($\tau_a = -40 \sim +85 \degree$ C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
V _I	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	٧
1	Input protection diode current	—20		
lικ	V _I > V _{CC}		20	mA
	Out to the diade t	V ₀ < 0V	-20	^
lok	$\begin{tabular}{lllllllllllllllllllllllllllllllllll$	20	mA	
lo	Output current, per output pin		±35	mA
Icc	Supply/GND current	V _{CC} , GND	±75	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65~+150	°C

Note 2 : M74HC534FP, $T_a=-40\sim+75^\circ$ C and $T_a=75\sim85^\circ$ C are derated at -7mW/°C. M74HC534DWP, $T_a=-40\sim+80^\circ$ C and $T_a=80\sim85^\circ$ C are derated at -7mW/°C.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85^{\circ}C)$

Symbol	Parameter		ŀ	Limits				
	Pai	Min	Тур	Max	Unit			
V _{CC}	Supply voltage	Supply voltage			6	٧		
V _I	Input voltage	0		Vcc	٧			
Vo	Output voltage	0		Vcc	٧			
Topr	Operating temperature ra	inge	-40		+85	°		
		$V_{CC} = 2.0V$	0		1000			
t _r , t _f Inp	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns		
		0		400				

ELECTRICAL CHARACTERISTICS

						Limits					
Symbol	Parameter	Test	Test conditions $V_{CC}(V)$		25℃			-40~+85℃		Unit	
					Min	Тур	Max	Min	Max		
		V =0.1V V	$V_0 = 0.1V, V_{CC} = 0.1V$ $V_{CC} = 0.1V$		1.5			1.5			
VIH	High-level input voltage				3.15			3.15		·V	
		Πο1 = 20μΑ		6.0	4. 2		-	4.2			
		V =0.1V V	$_{0} = 0.1V, V_{CC} = 0.1V$				0.5		0.5		
VIL	Low-level input voltage	$ V_0 = 0.1V, V_{CO} $					1.35		1.35	V	
				6.0			1.8	ļ	1.8		
	V _{OH} High-level output voltage		$I_{OH} = -20\mu A$	2.0	1.9			1.9			
		-	$I_{OH} = -20\mu A$	4.5	4.4			4.4		×	
V _{OH}		$V_{l} = V_{lH}, V_{lL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9			
			$I_{OH} = -6.0 \text{mA}$	4.5	4.18			4.13			
			$I_{OH} = -7.8 \text{mA}$	6.0	5.68			5. 63			
			$I_{OL} = 20 \mu A$	2.0			0.1		0. 1		
			$I_{OL} = 20 \mu A$	4.5			0.1		0.1		
VOL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0	<u> </u>		0.1		0.1	٧	
			$I_{OL} = 6.0 \text{mA}$	4.5			0. 26		0.33		
<u> </u>			I _{OL} = 7.8mA	6.0			0. 26		0.33		
I _{IH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μA	
I _{IL}	Low-level input current	V ₁ = 0V	V ₁ = 0V				-0.1		-1.0	μA	
lozh	Off-state high-level output current	$V_i = V_{iH}, \ V_{iL}, \ V$	$V_0 = V_{CC}$	6.0			0.5		5.0	μA	
lozL	Off-state low-level output current	$V_i = V_{iH}, V_{iL}, V_{iL}$	o = GND	6.0			-0.5		5.0	μΑ	
lcc	Quiescent supply current	V ₁ = V _{CC} , GND	$I_0 = 0 \mu A$	6.0			4.0		40.0	μA	

SWITCHING CHARACTERISTICS (V_{cc} = 5V, T_a = 25°C)

Symbol	Parameter	Tank and distance		Limits		
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
fmax	Maximum clock frequency		35			MHz
tTLH	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time	C _L = 50pF (Note 4)			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level				32	ns
t _{PHL}	output propagation time (CK $-\overline{Q}$)	*			32	ns
t _{PLZ}	Output disable time from low-level and high-level	0 = 5 : 5 (N + 4)			25	ns
t _{PHZ}	$(\overline{OE} - \overline{Q})$	C _L = 5 pF (Note 4)			25	ns
tezL	Output enable time to low-level and high-level	0 - 50-5 (N-4-4)			28	ns
t _{PZH}	$(\overline{OE} - \overline{Q})$	$C_L = 50pF (Note 4)$			28	ns

SWITCHING CHARACTERISTICS $(v_{cc} = 2\sim6v, \tau_a = -40\sim+85^{\circ}C)$

						Limits			
Symbol	Parameter	Test conditions			25℃		-40~	+85°C	Unit
		<u> </u>	V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0	6			5		
fmax	Maximum clock frequency	C _L = 50pF (Note 4)	4.5	30			24		MHz
			6.0	35			28		
			2.0			60		75	
t _{TLH}	Low-level to high-level and		4.5			12		15	ns
		0 50 5 (Note 4)	6.0			10		13	
	high-level to low-level	$C_L = 50pF (Note 4)$	2.0			60		75	
t _{THL}	output transition time		4.5			12		15	ns
			6.0		1	10		13	
***********		` .	2.0			180		227	
t _{PLH}			4.5			36		45	ns
			6.0			31		39	
		$C_L = 50pF (Note 4)$	2.0			180		227	
tent	Low-level to high-level and		4.5			36		45	ns
	high-level to low-level		6.0			31		39	
	output propagation time		2.0			230		290	
t _{PLH}	(CK - Q)		4.5			46		58	ns
35-211			6.0			39		49	
		C _L = 150pF (Note 4)	2.0			230		290	
t _{PHL}			4.5			46		58	ns
THE			6.0			39		49	
			2.0			150		189	
t_{PLZ}	Output disable time from		4.5			30		38	ns
PLZ	output disable time from		6.0			26		32	"
	low-level and high-level	$C_L = 50pF (Note 4)$	2.0		-	150		189	
t _{PHZ}	$(\overline{OE} - \overline{Q})$		4.5			30		38	ns
PHZ	(02 4)		6.0			26		32	''3
			2.0			150		189	
			4.5		1	30		38	ns
t _{PZL}		•	6.0			26		32	l iis
	-	C _L = 50pF (Note 4)	2.0		-	150	-	189	
	Output anable time to		4.5		100	30		38	ns
t _{PZH}	Output enable time to		6.0			26		38	118
	low-level and high-level		2.0			200		252	
	$(\overline{OE} - \overline{Q})$		4.5			40		50	
t _{PZL}	(02 - 4)		i i						ns
		C _L = 150pF (Note 4)	6.0		<u> </u>	34		43	
			2.0			200		252	
t _{PZH}			4.5			40		50	ns
		<u> </u>	6.0		-	34		43	
C,	Input capacitance	<u> </u>				10		10	pF
Со	Off-state output capacitance	OE = V _{CC}	· .			15		15	pF
CPD	Power dissipation capacitance (Note 3	D			63			<u> </u>	рF

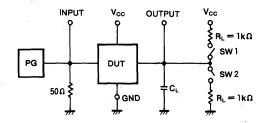
Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per flip-flop) The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$



TIMING REQUIREMENTS ($V_{cc} = 2\sim 6V$, $T_a = -40\sim +85^{\circ}C$)

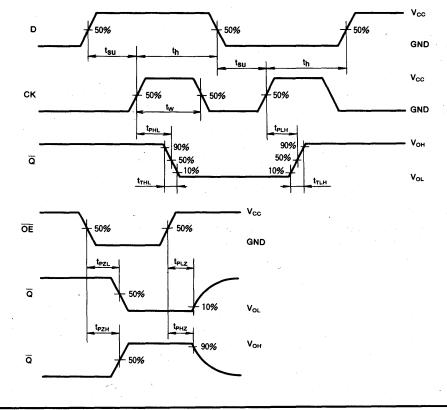
						Limits					
Symbol	Parameter	Test conditions		25℃			-40~+85°C		Unit		
		. 1	V _{cc} (V)	Min	Тур	Max	Min	Max]		
			2.0	80			101				
tw	Clock pulse width		4.5	16		1	20		ns		
			6.0	14			17				
	D setup time with		2.0	75			90				
tsu	respect to CK		4.5	.15			18	·	ns		
l :	respect to CK		6.0	13		1	16				
	D b - () May Mb		2.0	50			60				
th	D hold time with		4.5	10			12		ns		
	respect to CK		6.0	9			11				

Note 4: Test Circuit



Parameter	SW 1	SW 2
t _{TLH} , t _{THL} t _{PLH} , t _{PHL}	Open	Open
t _{PLZ}	Closed	Open
t _{PHZ}	Open	Closed
t _{PZL}	Closed	Open
t _{PZH}	Open	Closed

- (1) The pulse generator (PG) has the following characteristics (10% \sim 90%): $t_r = 6ns$, $t_f = 6ns$ (2) The capacitance C_L includes stray wiring
- capacitance and the probe input capacitance.





MITSUBISHI HIGH SPEED CMOS

M74HC534-1P/FP/DWP

OCTAL 3-STATE INVERTING D-TYPE FLIP-FLOP

DESCRIPTION

The M74HC534-1 is a semiconductor integrated circuit consisting of eight edge-triggered 3-state output D-type flip-flops with common clock input and output-enable input.

FEATURES

- High-fanout 3-state output: (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed: (clock frequency) 60MHz typ.
 (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 25µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 60 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=-40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

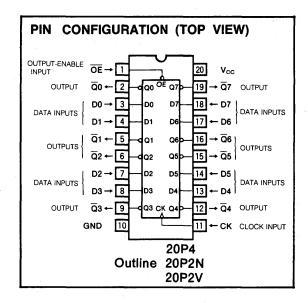
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC534-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS534.

The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

The M74HC534-1 contains eight edge-triggered D-type flip-flops, sharing common clock input CK and output-enable input $\overline{\text{OE}}$.

When CK changes from low-level to high-level, the signals

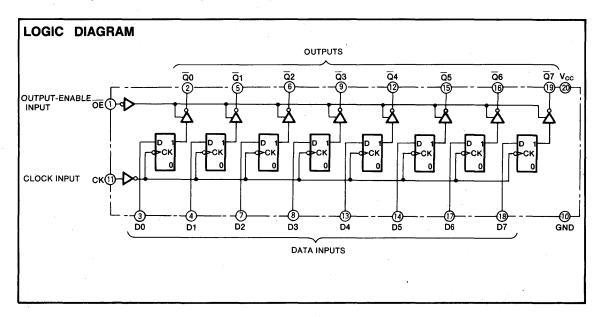


just previously input at D stores in the flip-flop.

When output-enable input \overline{OE} is low, the signals stored in the flip-flop will be output to \overline{Q} .

When \overline{OE} is high, all outputs \overline{Q} will become high-impedance state. The contents stored in the flip-flop will not be affected even if \overline{OE} is changed.

A version of the M74HC534-1 with the same pin connections and a noninverted output, the M74HC374-1, is also available.



FUNCTION TABLE (Note 1)

	Inputs		Output				
OE	CK	D	Q				
* · L	1	, L	Н				
L	1	Н	L				
L	L	Х	Q٥				
L	Н	Х	Q°				
L	1	X	Q٥				
Н	Х	X	Z				

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Note 1 : Qo: Output state Q before clock input changed

Z : High impedance

X : Irrelevant

† : Change from low to high level

↓ : Change from high to low level

ABSOLUTE MAXIMUM RATINGS $(\tau_a = -40 \sim +85\%$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit				
V _{CC}	Supply voltage		-0.5~+7.0	V				
Vı	Input voltage		-0.5~V _{cc} +0.5	V				
Vo	Output voltage		-0.5~V _{cc} +0.5	V				
		V ₁ < 0V	-20	mA				
l _{IK}	Input protection diode current	V _i > V _{cc}	V ₁ > V _{CC} 20					
•	0.1.1.1	V ₀ < 0V	-20					
юк	Output parasitic diode current	V _o > V _{cc}	20	mA				
lo	Output current, per output pin		±50	mA				
loc	Supply/GND current	V _{CC} , GND	±200	mA				
Pd	Power dissipation	(Note 2)	500	mW				
Tstg	Storage temperature range		−65~+150	ဗ				

Note 2 : M74HC534-1FP, Ta = $-40\sim+75$ °C and Ta = $75\sim85$ °C are derated at -7mW/°C. M74HC534-1DWP, Ta = $-40\sim+80$ °C and Ta = $80\sim85$ °C are derated at -7mW/°C.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85 \text{ C})$

Symbol	Dec	Parameter		Limits				
Зуппоот	Fal	ameter	Min	Тур	Max	Unit		
Vcc	Supply voltage		. 2		6	V		
Vı	Input voltage		0		V _{CC}	V		
Vo	Output voltage	0		Vcc	V			
Topr	Operating temperature ra	ange	-40		+85	ဗ		
		V _{CC} = 2.0V	0		500			
t _r , t _f	Input risetime, falltime	V _{CC} = 4.5V	0		50	ns/V		
		0		30	1			

MT4HC534-1P/FP/DWP

OCTAL 3-STATE INVERTING D-TYPE FLIP-FLOP

ELECTRICAL CHARACTERISTICS

	-			Limits						
Symbol	Parameter	Test	Test conditions		25°C			-40~+85°C		Unit
		V _{cc} (V)		Min	Тур	Max	Min	Max	ì	
		$V_0 = 0.1V, V_{CC} = 0.1V$		2.0	1.5			1.5		
VIH	High-level input voltage			4.5	3.15			3. 15		V
		$ I_O = 20\mu A$		6.0	4. 2			4. 2		
	V ₀ = 0		-0.11/	2.0			0.5		0.5	
VIL	Low-level input voltage	$V_0 = 0.1V, V_{CC}$	5—0.1 V	4.5			1.35		1.35	V
	110 = 20µA	$ I_0 = 20\mu A$				1.8	ļ	1.8		
	High level output valtage	$V_i = V_{iH}, \ V_{iL}$	$I_{OH} = -20\mu A$	2.0	1.9			1.9		v
			$I_{OH} = -20 \mu A$	4.5	4. 4			4.4		
V _{OH}	High-level output voltage		$I_{OH} = -20\mu A$	6.0	5.9			5.9		
			$I_{OH} = -24mA$	4.5	3. 98			3.84		
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	v
.,		\ <u></u>	$I_{OL} = 20 \mu A$	4.5			0.1		0.1	
Vol	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0	'		0.1		0.1	
			I _{OL} = 24mA	4.5			0.39		0.5	
I _{IH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μА
I _{IL}	Low-level input current	V ₁ = 0V		6.0			-0.1		-1.0	μΑ
lozh	Off-state high-level output current	$V_i = V_{iH}, \ V_{iL}, \ V_{iL}$	$V_i = V_{iH}, \ V_{iL}, \ V_O = V_{CC}$				0.5		5.0	μА
lozL	Off-state low-level output current	$V_i = V_{iH}, \ V_{iL}, \ V_{iL}$	o = GND	6.0			-0.5		-5.0	μА
Icc	Quiescent supply current	VI = VCC, GND	$I_0 = 0 \mu A$	6.0			5.0		50.0	μА

SWITCHING CHARACTERISTICS $(V_{co} = 5V, T_a = 25^{\circ}C)$

Symbol	Parameter	Test conditions		Limits		
Symbol		rest conditions	Min	уp	Max	Unit
fmax	Maximum clock frequency		35			MHz
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time	C _L = 50pF (Note 4)			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level				20	ns
t _{PHL}	output propagation time (CK — Q)				20	ns
t _{PLZ}	Output disable time from low-level and high-level	0 - 5 - 5 (N-4-4)			20	ns
t _{PHZ}	(OE - Q)	C _L = 5 pF (Note 4)			20	ns
t _{PZL}	Output enable time to low-level and high-level	0 - 50-5 (N-1-4)			23	ns
t _{PZH}	$(\overline{OE} - \overline{Q})$	C _L = 50pF (Note 4)			23	ns

SWITCHING CHARACTERISTICS ($V_{cc} = 2\sim6V$, $T_a = -40\sim+85^{\circ}C$)

						Limits			
Symbol	Parameter	Test conditions	4 <u>-1</u>		25℃		-40~	+85℃	Unit
			V _{CC} (V)	Min	Тур	Max	Min	Max	
			2.0	6		,	5		
fmax	Maximum clock frequency		4.5	32	1	}	26		MHz
			6.0	38			31		
		1	2.0			60		75	
tTLH	Low-level to high-level and	·	4.5		l	12		15	ļ ,
· - · ·			6.0			10		13	· ·
	high-level to low-level		2.0		T	60		75	ns
t _{THL}	output transition time		4.5			12		15	
			6.0			10		13	
		1	2.0			110		140	
t _{PLH}	Low-level to high-level and		4.5			22		28	24 ns
	high-level to low-level		6.0			19		24	
-	output propagation time		2.0	-		110	1	140	
t _{PHL}	(CK - Q)	C _L = 50pF (Note 4)	4.5			22		28	
			6.0			19		24	
		7	2.0			125		155	
t _{PLZ}	Output disable time from		4.5]	100	25		31	
			6.0			21		. 26	
	low-level and high-level		2.0			125		155	ns
t _{PHZ}	$(\overline{OE} - \overline{Q})$		4.5	· ·	ĺ	25		31	\
			6.0			21		26	
			2.0			125		155	
tpZL	Output enable time to		4.5		1	25		31	
			6.0	i	ì	21		26	
	low-level and high-level		2.0			125		155	ns
t_{PZH}	(OE – Q)		4.5			25		31	
			6.0			21		26	<u> </u>
Cı	Input capacitance					10		10	
Со	Off-state output capacitance	OE = V _{CC}				15		15	pF
C _{PD}	Power dissipation capacitance (Note 3)] .

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per flip-flop)

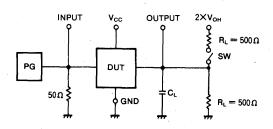
The power dissipated during operation under no-load conditions is calculated using the following formula:

P_D = C_{PD} · V_{CC}² · f₁+I_{CC} · V_{CC}

TIMING REQUIREMENTS ($V_{cc} = 2\sim6V$, $T_a = -40\sim+85^{\circ}C$)

					Limits				
Symbol	Parameter	Test conditions			25℃		-40~+85℃		Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max]
			2.0	60			75		
tw	Clock pulse width		4.5	12			15		ns
			6.0	10			13 \		
	D coting time with		2.0	50			65		
tsu	D setup time with respect to CK	The second secon	4.5	10	-		13		ns
	respect to CK		6.0	9	1		11		1
	D hold time with	• •	2.0	25			30		
th	respect to CK		4.5	5			6		ns
	respect to CK		6.0	5			6		

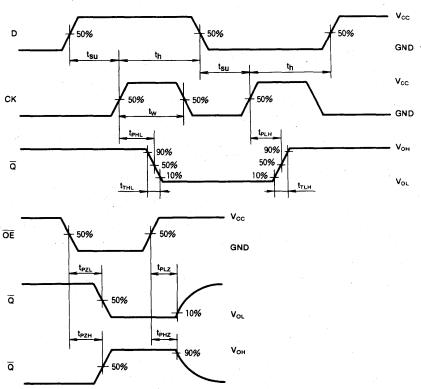
Note 4: Test Circuit



Parameter	sw
t _{TLH} , t _{THL}	Open
t _{PLZ}	Closed
t _{PHZ}	Open
t _{PZL}	Closed
t _{PZH}	Open

- (1) The pulse generator (PG) has the following
- characteristics (10%~90%): t_f = 3ns, t_f = 3ns

 (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.



MITSUBISHI HIGH SPEED CMOS

M74HCT534-1P/FP/DWP

OCTAL 3-STATE
INVERTING D-TYPE FLIP-FLOP WITH LSTTL-COMPATIBLE INPUTS

DESCRIPTION

The M74HCT534-1 is a semiconductor integrated circuit consisting of eight edge-triggered 3-state output D-type flip-flops with common clock input and output-enable input.

FEATURES

- TTL level inputs V_{IL}=0.8V max, V_{IH}=2.0V min
- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: (Clock frequency) 55MHz typ.
 (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 25µW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- Capable of driving 60 74LSTTL loads
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

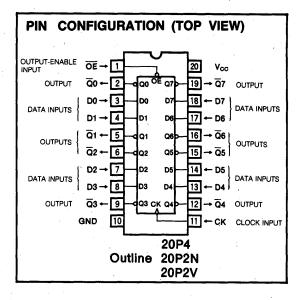
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HCT534-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS534.

The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

As the inputs are TTL level, the device can be used as a level converter from LSTTL to high-speed CMOS. In that case, no pull-up resistors are required.

The M74HCT534-1 contains eight edge-triggered D-type flip-flops, sharing common clock input CK and output-



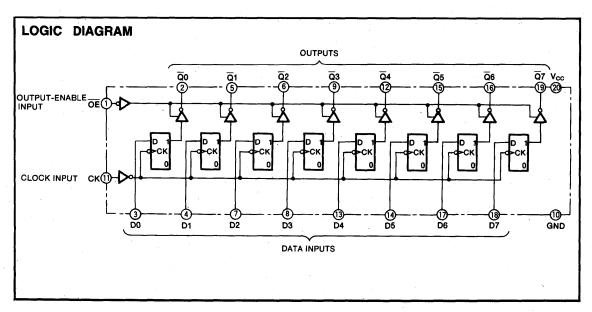
enable input OE.

When CK changes from low-level to high-level, the signals just previously input at D is stored in the flip-flop.

When output-enable input \overline{OE} is low, the signals stored in the flip-flop will be output to \overline{Q} .

When OE is high, all outputs \overline{Q} will become high-impedance state. The contents stored in the flip-flop are not affected even if \overline{OE} is changed.

A version of the M74HCT534-1 with the same pin connections and a noninverted output, the M74HCT374-1, is also available.



OCTAL 3-STATE INVERTING D-TYPE FLIP-FLOP WITH LSTTL-COMPATIBLE INPUTS

FUNCTION TABLE (Note 1)

	Inputs					
OE	OE CK		Q			
L	1	L .	Н			
L	1	Н	L			
L	L	X	Q°			
L	н	Х	Q°			
L	1	Х	Q٥			
Н	X	Х	z			

Note 1: \overline{Q}^0 : Output state \overline{Q} before clock input changed

Z : High impedance

X : Irrelevant

† : Change from low to high level

↓ : Change from high to low level

$\textbf{ABSOLUTE} \quad \textbf{MAXIMUM} \quad \textbf{RATINGS} \ (\textbf{T}_a = -40 \sim +85 ^{\circ} \textbf{C}, \text{ unless otherwise noted})$

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
.V _f	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
	land water died a summe	V ₁ < 0V	-20	
l _{IK}	Input protection diode current	V _I > V _{CC}	20	mA
		V ₀ < 0V	-20	
lok	Output parasitic diode current	V _o > V _{cc}	20	mA
l _o	Output current, per output pin		±50	mA
Icc	Supply/GND current	V _{CC} , GND	±200	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		-65~+150	င

Note 2 : M74HCT534-1FP, $T_a=-40\sim+75^\circ$ C and $T_a=75\sim85^\circ$ C are derated at -7mW/°C. M74HCT534-1DWP, $T_a=-40\sim+80^\circ$ C and $T_a=80\sim85^\circ$ C are derated at -7mW/°C.

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85 \degree c)$

Symbol		Parameter		Limits				
Зупівої	Parameter		Min	Тур	Max	Unit		
V _{cc}	Supply voltage	4.5		5. 5	٧			
V _I	Input voltage		- 0		Vcc	٧		
V _o	Output voltage		0		Vcc	٧		
Topr	Ambient operating temperature		-40		+85	°°		
t _r , t _f		$V_{CC} = 4.5V$	0		25	0		
	Input risetime, falltime V _{CC} = 5.5V		0		15	ns/V		

OCTAL 3-STATE INVERTING D-TYPE FLIP-FLOP WITH LSTTL-COMPATIBLE INPUTS

ELECTRICAL CHARACTERISTICS ($V_{cc} = 5V \pm 10\%$, unless otherwise noted)

				Limits					-
Symbol	Parameter		Test conditions		25℃			+85℃	Unit
		· · · · · · · · · · · · · · · · · · ·		Min.	Тур	Max	Min	Max	
V _{IH}	High-level input voltage	$V_0 = 0.1V, V_{CO}$ $ I_0 = 20\mu A$	$V_0 = 0.1V$, $V_{CC} = 0.1V$ $ I_0 = 20\mu A$				2.0		V
V _{IL}	Low-level input voltage	$V_0 = 0.1V, V_0$ $ I_0 = 20\mu A$	$V_0 = 0.1V$, $V_{CC} = 0.1V$ $I_0 = 20\mu A$			0.8		0.8	V
V High level output veltege	$V_i = V_{ii}$	$I_{OH} = -20\mu A$	V _{cc} -0.1			V _{cc} -0.1		v	
V _{OH}	High-level output voltage	IOH	$I_{OH} = -24mA$, $V_{CC} = 4.5V$	3.98			3.84		
VoL	Level autout videore	V – V V	$I_{OL} = 20 \mu A$			0.1		0.1	v
VOL	Low-level output voltage	AI VIH, VIL	$V_1 = V_{1H}, V_{1L}$ $I_{OL} = 24mA, V_{CC} = 4.5V$			0.39		0.5	
l _{iH}	High-level input current	$V_{I} = V_{CC}$				0.1		1.0	
1 _{IL}	Low-level input current	V _I = GND				-0.1		-1.0	μΑ
lozh	Off-state high-level output current	$V_i = V_{iH}, \ V_{iL},$	$V_0 = V_{CC}$			0.5		5.0	
lozL	Off-state low-level output current	$V_i = V_{iH}, \ V_{iL},$	$V_i = V_{iH}, V_{iL}, V_O = GND$			-0.5		-5.0	μA
Icc	Quiescent supply current	$V_1 = V_{CC}$, GND, $I_0 = 0\mu A$			-	5.0	T	50.0	μА
Δlcc	Maximum quiescent supply current	V _I = 2.4V, 0.4V (Note 3)				2.7		2. 9	mA

Note 3: Only one input is set at this value and all other inputs are fixed at V_{CC} or GND.

SWITCHING CHARACTERISTICS (V_{cc} = 5V, T_a = 25°C)

O b. ed	Parameter	Test conditions		Unit		
Symbol	Parameter	l est conditions	Min	Тур	Max	Unit
fmax	Maximum clock frequency		35			MHz
t _{TLH}	Low-level to high-level and high-level to low-level	7			10	ns
t _{THL}	output transition time	C _L = 50pF (Note 5)			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level				20	ns
t _{PHL}	output propagation time (CK $-\overline{\mathbf{Q}}$)				20	ns
t _{PLZ}	Output disable time from low-level and high-level	0 = 5 = 5 (Note 5)			20	ns
t _{PHZ}	$(\overline{OE} - \overline{Q})$	C _L = 5 pF (Note 5)			20	ns
t _{PZL}	Output enable time to low-level and high-level	0 - 50-5 (Al-a-5)			23	ns
t _{PZH}	$(\overline{OE} - \overline{Q})$	C _L = 50pF (Note 5)			23	ns

SWITCHING CHARACTERISTICS ($V_{cc} = 5V \pm 10\%$, $T_a = -40 \sim +85$ °C)

			Limits						
Symbol	Parameter	Test conditions	25℃			-40~+85℃		Unit	
			Min	Тур	Max	Min	Max	1	
fmax	Maximum clock frequency		32			26		MHz	
t _{TLH}	Low-level to high-level and	,			12		15		
t _{THL}	high-level to low-level output transition time	·			12		15	ns.	
t _{PLH}	Low-level to high-level and high-level to low-level	C _i = 50pF (Note 5)			22		28	ns	
tehL	output <u>pr</u> opagation time (CK — Q)				22		28		
t _{PLZ}	Output disable time from	CL — SUPF (Note 5)			25		31		
	low-level and high-level						 		
t _{PHZ}	(OE - Q)				25	İ	31		
t _{PZL}	Output enable time to				25		31		
t _{PZH}	low-level and high-level (OE - Q)				25		31	ns	
Cı	Input capacitance				10		10		
Co	Off-state output capacitance	OE = V _{CC}			15		15	pF	
C _{PD}	Power dissipation capacitance (Note 4)	·						1	

Note 4: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per flip-flop)

The power dissipated during operation under no-load conditions is calculated using the following formula:

P_D = C_{PD} · V_{CC}² · f₁+I_{CC} · V_{CC}

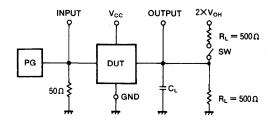


OCTAL 3-STATE INVERTING D-TYPE FLIP-FLOP WITH LSTTL-COMPATIBLE INPUTS

TIMING REQUIREMENTS ($V_{cc} = 5V \pm 10\%$, $T_a = -40 \sim +85^{\circ}C$)

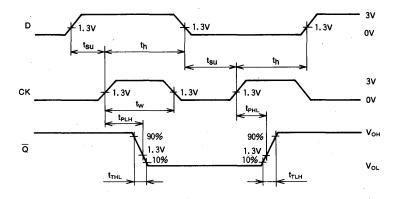
Symbol	Parameter	Test conditions		Limits					
			25°C			-40~+85℃		Unit	
			Min	Тур	Max	Min	Max	1	
t _w	Clock pluse width		12			15		ns	
t _{su}	D setup time with respect to CK		10			13		ns	
th	D hold time with respect to CK	•	- 5			6		ns	

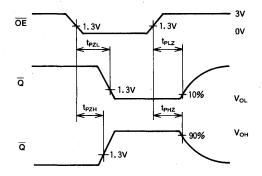
Note 5: Test Circuit



Parameter	SW
t _{TLH} , t _{THL}	Open
t _{PLZ}	Closed
t _{PHZ}	Open
t _{PZL}	Closed
t _{PZH}	Open

- (1) The pulse generator (PG) has the following
- characteristics $(10\% \sim 90\%)$: $t_r = 3ns$, $t_f = 3ns$ (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.





M74HC540P/FP/DWP

OCTAL 3-STATE INVERTING BUFFER/LINE DRIVER/LINE RECEIVER

DESCRIPTION

The M74HC540 is a semiconductor integrated circuit consisting of 3-state inverting buffers each with eight independent circuits that share a common enable inputs.

FEATURES

- High-speed: 12ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2∼6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

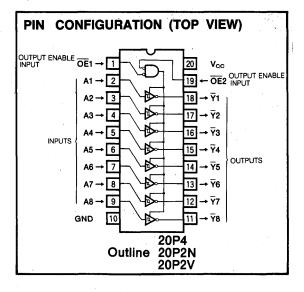
Use of silicon gate technology allows the M74HC540 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS540.

The M74HC540 has hysteresis characteristics in the input circuits and inverting 3-state outputs with a high noise margin.

When the output enable inputs $\overline{OE}1$ and $\overline{OE}2$ are both low, and an input A is low, then the corresponding output \overline{Y} will become high: when A is high, \overline{Y} will become low.

When either $\overline{OE}1$ or $\overline{OE}2$ is high, all outputs will become the high-impedance state, irrespective of A.

The input and output pins are arranged for facilitated board layout (data flow-through pin out).

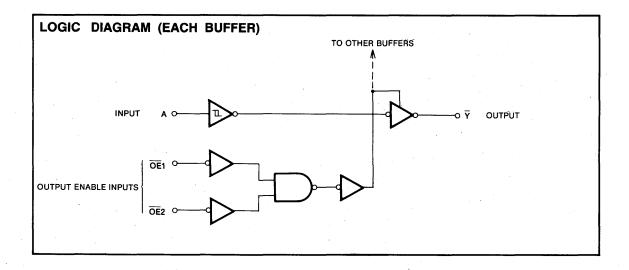


FUNCTION TABLE (Note 1)

	Inputs			
Α	OE1	OE2	Ÿ	
L	. L	L	. Н	
Н	L .	L	L	
' X	L	Н	Z.	
×	Н	L	z	
×	н	Н	Z	

Note 1 : Z : High impedance

X : Irrelevant



OCTAL 3-STATE INVERTING BUFFER/LINE DRIVER/LINE RECEIVER

ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85 \degree$ C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	V
V _O	Output voltage		-0.5~V _{cc} +0.5	V
		V ₁ < 0V	-20	T
l _{IK}	Input protection diode current	V _I > V _{CC}	20	mA
		V _o < 0V	-20	
Іок	Output parasitic diode current	V _o > V _{cc}	20	mA mA
lo	Output current per output pin		±35	mA
Icc	Supply/GND current	V _{CC} , GND	±75	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		-65~+150	င

Note 2 : M74HC540FP, T_a = $-40\sim+75^\circ$ C and T_a = $75\sim85^\circ$ C are derated at -7mW/°C. M74HC540DWP, T_a = $-40\sim+80^\circ$ C and T_a = $80\sim85^\circ$ C are derated at -7mW/°C.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85^{\circ}C)$

Cumbal	mbol Parameter				Unit		
Symbol	Pa	rameter		Min	Тур	Max	Unit
Vcc	Supply voltage	Supply voltage		2		6	V
Vı	Input voltage	nput voltage		0		Vcc	٧
Vo	Output voltage	Output voltage		0		Vcc	V
Topr	Operating temperature ra	ange		-40		+85	ဗ
		$V_{CC} = 2.0V$		0		1000	
t _r , t _f	t _r , t _f Input risetime, falltime	$V_{CC} = 4.5V$		0		500	ns
		$V_{CC} = 6.0V$		0		400	

ELECTRICAL CHARACTERISTICS

							Limits			
Symbol	Parameter	Test	conditions		25℃			-40~+85°C		Unit
	'		V _{cc} (V)		Min	Тур	Max	Min	Max	
V _{IH}	High-level input voltage	$V_0 = 0.1V$ $ I_0 = 20\mu A$		2. 0 4. 5 6. 0	1.5 3.15	-		1.5 3.15		v
		$V_0 = 0.1V, V_{C}$	$V_0 = 0.1V$, $V_{CC} = 0.1V$		4.2		0.5	4.2	0.5	
V _{IL}	Low-level input voltage	$ I_0 = 20\mu A$					1.35 1.8		1.35 1.8	V
			$I_{OH} = -20\mu A$ $I_{OH} = -20\mu A$	2. 0 4. 5	1.9 4.4			1.9 4.4		
V _{OH}	V _{OH} High-level output voltage	$V_i = V_{iL}$	$I_{OH} = -20\mu A$ $I_{OH} = -6.0 \text{mA}$	6. 0 4. 5	5. 9 4. 18			5. 9 4. 13 5. 63		V
			$I_{OH} = -7.8 \text{mA}$ $I_{OL} = 20 \mu \text{A}$ $I_{OL} = 20 \mu \text{A}$	6. 0 2. 0 4. 5	5. 68		0.1	5. 63	0.1	
V _{OL}	Low-level output voltage	$V_{i} = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$ $I_{OL} = 6.0 \text{mA}$ $I_{OL} = 7.8 \text{mA}$	6. 0 4. 5 6. 0			0. 1 0. 26 0. 26		0. 1 0. 33 0. 33	V
I _{IH}	High-level input current	$V_i = 6V$		6.0			0.1		1.0	
I _{IL}	Low-level input current	$V_i = 0V$		6.0			-0.1		-1.0	μF
I _{OZH}	Off-state high-level output current Off-state low-level output current	$V_{I} = V_{IH}, V_{IL}, V_{O} = V_{CC}$ $V_{I} = V_{IH}, V_{IL}, V_{O} = GND$		6.0			0.5		5.0 -5.0	μF
I _{CC}	Quiescent supply current	$V_i = V_{CC}$, GND		6.0			4.0		40.0	μF

OCTAL 3-STATE INVERTING BUFFER/LINE DRIVER/LINE RECEIVER

SWITCHING CHARACTERISTICS ($V_{cc} = 5V$, $T_a = 25$ °C)

Complete	Barrandan	Test conditions		Limits			
Symbol	Parameter	lest conditions	Min	Тур	Max	Unit	
t _{TLH}	Low-level to high-level and high-level to low-level		- ·		10		
t _{THL}	output transition time	C ₁ = 50pF (Note 4)			10	ns	
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = 50pr (Note 4)			18		
t _{PHL}	output propagation time $(A - \overline{Y})$				18	ns	
t _{PLZ}	Output disable time from low-level and high-level	C = 5 = 5 (Note 4)	0 = 5 = 5 (N + + 4)		25		
t _{PHZ}	$(\overline{OE} - \overline{Y})$	$C_L = 5 pF (Note 4)$			25	ns	
t _{PZL}	Output enable time to low-level and high-level	C _L = 50pF (Note 4)		28			
t _{PZH}	(ŌĒ — Ÿ)	OL - SUPP (NOIS 4)			28	ns	

SWITCHING CHARACTERISTICS ($V_{cc} = 2\sim6V$, $T_a = -40\sim+85^{\circ}C$)

						Limits	г		
Symbol	Parameter	Test conditions			25℃		-40~	+85℃	Unit
			V _{CC} (V)	Min	Тур	Max	Min	Max	
			2.0			60		75	
t _{TLH}	Low-level to high-level and		4.5			12		15	
	blab laval to lave lavel	C _L = 50pF (Note 4)	6.0			10		13	ns
	high-level to low-level	C _L = 50pr (Note 4)	2.0			60		75	
t _{THL}	output transition time		4.5			12	1	15	
	į ·	1	6.0			10	1	13	
			2.0			100		126	
t _{PLH}		'	4.5			20	Ì	25	
		50 7 (01) 4)	6.0			17		21	
		C _L = 50pF (Note 4)	2.0			100		126	1
t _{PHL}	Low-level to high-level and		4.5			20		25	
	high-level to low-level	· .	6.0			17	1	21	
	output propagation time		2.0			150		190	ns
t _{PLH}	$(A - \overline{Y})$		4.5		İ	30		38	
			6.0			26		32	
,	1	C _L = 150pF (Note 4)	2.0			150		190	
t _{PHL}			4.5			30		38	
		,	6.0			26		32	
			2.0			150		189	
t _{PLZ}	Output disable time from		4.5			30		38	ns
			6.0			26		32	
	low-level and high-level	C _L = 50pF (Note 4)	2.0			150		189	
t _{PHZ}	$(\overline{OE} - \overline{Y})$		4.5			30		38	
			6.0) ·		26		32	1
			2.0			150		189	
t _{PZL}	· ·		4.5			30		38	
			6.0			26		32	
	1	C _L = 50pF (Note 4)	2.0			150		189	1
t _{PZH}	Output enable time to		4.5			30		38	
			6.0			26		32	
·	low-level and high-level		2.0			200		252	ns
t _{PZL}	$(\overline{OE} - \overline{Y})$		4.5			40		50	
			6.0			34		43	ľ
	1	C _L = 150pF (Note 4)	2.0			200		252	1
t _{PZH}	in the second		4.5			40		50	
			6.0			34		43	
Cı	Input capacitance				<u> </u>	10		10	pF
Co	Off-state output capacitance	OE = V _{CC}	1 -			15	†	15	pF
C _{PD}	Power dissipation capacitance (Note 3)		+		40	1			pF

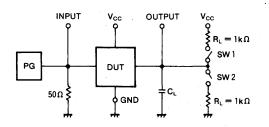
Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per buffer)

The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$



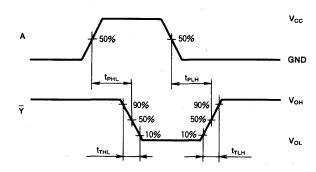
OCTAL 3-STATE INVERTING BUFFER/LINE DRIVER/LINE RECEIVER

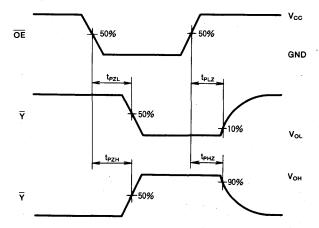
Note 4: Test Circuit



Parameter	SW 1	SW 2
t _{TLH} , t _{THL}	Open	Open
t _{PLZ}	Closed	Open
t _{PHZ}	Open	Closed
t _{PZL}	Closed	Open
t _{PZH}	Open	Closed

- (1) The pulse generator (PG) has the following characteristics (10%~90%): $\rm t_f=6ns,\, t_f=6ns$
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.





M74HC541P/FP/DWP

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER

DESCRIPTION

The M74HC541 is a semiconductor integrated circuit consisting of 3-state non-inverting buffers each with eight independent circuits that share a common enable inputs.

FEATURES

- High-speed: 14ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

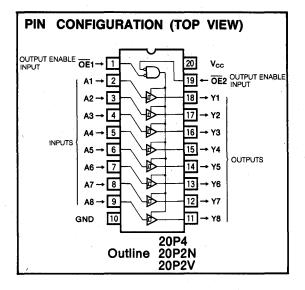
Use of silicon gate technology allows the M74HC541 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS541.

The M74HC541 has hysteresis characteristics in the input circuits and noninverting 3-state outputs with a high noise margin.

When the output enable inputs $\overline{OE}1$ and $\overline{OE}2$ are both low, and an input A is low, then the corresponding output Y will become low; when A is high, Y will become high.

When either $\overline{\text{OE1}}$ or $\overline{\text{OE2}}$ is high, all outputs will become the high-impedance state, irrespective of A.

The input and output pins are arranged for facilitated board layout (data flow-through pin out).

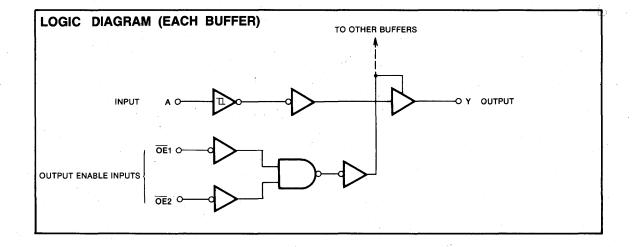


FUNCTION TABLE (Note 1)

	Inputs		Output
Α	OE1	OE2	Y
L	L	L	L
Н	L	L	. н
Х	L	Н	Z
х	н	L	Z
X	н	н	Z

Note 1 : Z : High impedance

X : Irrelevant



OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER

ABSOLUTE MAXIMUM RATINGS ($\tau_a = -40 \sim +85^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit		
Vcc	Supply voltage		-0.5~+7.0	V		
Vi	Input voltage		-0.5~V _{cc} +0.5	V		
V _o	Output voltage		-0.5~V _{cc} +0.5	V		
		V ₁ < 0V	-20			
ık İn	Input protection diode current	V _I > V _{CC}	20	mA.		
		V ₀ < 0V	-20			
Гок	Output parasitic diode current	$V_{o} > V_{cc}$	20	mA		
lo	Output current per output pin		±35	mA		
lcc	Supply/GND current	V _{CC} , GND	±75	mA		
Pd	Power dissipation	(Note 2)	500	mW		
Tstg	Storage temperature range		−65~ + 150	°C		

Note 2 : M74HC541FP, T_a = $-40 \sim +75 \%$ and T_a = $75 \sim 85 \%$ are derated at -7mW/°C. M74HC541DWP, T_a = $-40 \sim +80 \%$ and T_a = $80 \sim 85 \%$ are derated at -7mW/°C.

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85 ^{\circ}C)$

	Parameter			Limits				
Symbol			Min	Тур	Max	Unit		
Vcc	Supply voltage		2		6	٧		
Vı	Input voltage		0		Vcc	V		
Vo	Output voltage		0		Vcc	٧		
Topr	Operating temperature ra	inge	-40		+85	℃		
		$V_{CC} = 2.0V$	0		1000			
t _r , t _f	tr, tf Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns		
		$V_{CC} = 6.0V$	0		400			

ELECTRICAL CHARACTERISTICS

•	·						Limits			
Symbol	Parameter	Test	Test conditions			25℃ ′		-40~+85°C		Unit
				V _{CC} (V)	Min	Тур	Max	Min	Max	
		V - V 0 11		2.0	1.5			1.5		11
ViH	High-level input voltage	$V_0 = V_{CC} - 0.1$	•	4.5	3.15			3. 15		/ v
		$ I_{O} = 20\mu A $ 6. 0		6.0	4.2		1	4.2		
	,	V = 0.1V V	0.11/	2.0			0.5		0.5	
V _{IL}	Low-level input voltage		$_{0} = 0.1V, V_{CC} = 0.1V$				1.35		1.35	V
		$ I_0 = 20\mu A$		6.0			1.8		1.8	
			$1_{OH} = -20 \mu A$	2.0	1.9			1.9		
			$I_{OH} = -20\mu A$	4.5	4.4			4.4		
V _{OH}	High-level output voltage	$V_{l} = V_{lH}, V_{lL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		V
			$I_{OH} = -6.0 \text{mA}$	4.5	4.18			4.13		
			$I_{OH} = -7.8 \text{mA}$	6.0	5.68	1	1	5.63		
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
	*		$I_{OL} = 20 \mu A$	4.5			0.1		Ö. 1	:
VoL	Low-level output voltage	$V_i = V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
			$I_{OL} = 6.0 \text{mA}$	4.5			0.26		0.33	
			$I_{OL} = 7.8 \text{mA}$	6.0			0.26	ì	0.33	
l _{iH}	High-level input current	V₁ == 6V		6.0			0.1		1.0	
l _{IL}	Low-level input current	V, = 0V		6.0			-0.1		-1.0	μA
огн	Off-state high-level output current	$V_i = V_{iH}, \ V_{iL},$	$v_o = v_{cc}$	6.0			0.5		5.0	μ
lozL	Off-state low-level output current	$V_i = V_{iH}, V_{iL},$	V _O = GND	6.0			-0.5		-5.0	μ
Icc	Quiescent supply current	VI = VCC, GND	$I_{O} = 0\mu A$	6.0			4.0		40.0	μ

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER

SWITCHING CHARACTERISTICS (Vcc = 5V, Ta = 25°C)

		T-4diate-		Limits		
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
t _{TLH}	Low-level to high-level and high-level to low-level				10	
t _{THL}	output transition time	C _L = 50pF (Note 4)			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level				20	
t _{PHL}	output propagation time (A — Y)				20	ns
t _{PLZ}	Output disable time from low-level and high-level	C ₁ = 5 pF (Note 4)			25	
t _{PHZ}	(OE - Y)	CL = 5 pr (Note 4)			25	ns
t _{PZL}	Output enable time to low-level and high-level	C = 50=5 (Note 4)			28	
t _{PZH}	(OE – Y)	C _L = 50pF (Note 4)			28	ns

SWITCHING CHARACTERISTICS $(v_{cc} = 2\sim6V, T_a = -40\sim+85^{\circ}C)$

						Limits			
Symbol	Parameter	Test conditions			25℃		-40~	+85°C	Unit
			V _{cc} (v)	Min	Тур	Max	Min	Max	
			2.0		i	60		75	
t _{TLH}	Low-level to high-level and		4.5			12		15	
	high-level to low-level	C _L = 50pF (Note 4)	6.0			10		13	ns
	Iligh-level to low-level	CL — 50PF (14016 4)	2. 0			60		75	1115
t _{THL}	output transition time	· ·	4.5			12		15	
	•		6.0			10		13	
			2, 0			115 -		145	
t _{PLH}			4.5			23		29	
		C _L = 50pF (Note 4)	6.0			20		25	
		C _L = 50pr (Note 4)	2.0			115		145	1
t _{PHL}	Low-level to high-level and		4.5	}		23		29	
	high-level to low-level		6.0			20		25	
	output propagation time		2.0		-	165		208	ns
t _{PLH}	(A — Y)		4.5			33		42	
		0 = 150=5 (N-1=4)	6.0			28		35	
	1	C _L = 150pF (Note 4)	2.0			165		208	1
t _{PHL}			4.5			33		42	
			6.0			28		35	
			2.0			150		189	
t _{PLZ}	Output disable time from		4.5		}	30		38	1
:	1	50 5 (0)	6.0		1	26		32	1
	low-level and high-level	C _L = 50pF (Note 4)	2.0	1		150		189	ns
t _{PHZ}	(OE - Y)		4.5			30		38	
			6.0			26		32	
***************************************			2.0		<u> </u>	150		189	
t _{PZL}			4.5			30		38	
	· ·		6.0			26		- 32	-
	1	C _L = 50pF (Note 4)	2.0			150		189	1
t _{PZH}	Output enable time to		4.5			30		38	
			6.0	-		26		32	
	low-level and high-level		2.0			200	1	252	ns
t _{PZL}	(OE – Y)		4.5	,		40		50	
			6.0			34		43	
	† · ·	C _L = 150pF (Note 4)	2.0		1.	200		252	1
t _{PZH}	;		4.5			40		50	
			6.0		1	34	,	43	
C,	Input capacitance				1.	10		10	pF
Co	Off-state output capacitance	OE = V _{CC}				15		15	pF
C _{PD}	Power dissipation capacitance (Note 3			 	44	T	1		pF

Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per buffer)

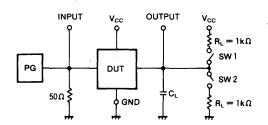
The power dissipated during operation under no-load conditions is calculated using the following formula:

P_D = C_{PD} · V_{CC}² · f₁+I_{CC} · V_{CC}



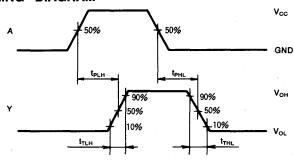
OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER

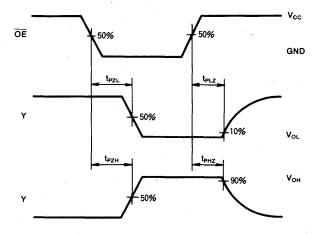
Note 4: Test Circuit



Parameter	SW 1	SW 2
t _{TLH} , t _{THL} t _{PLH} , t _{PHL}	Open	Open
t_{PLZ}	Closed	Open
t _{PHZ}	Open	Closed
t _{PZL}	Closed	Open
t _{PZH}	Opén	Closed

- (1) The pulse generator (PG) has the following characteristics (10% \sim 90%): $t_f = 6$ ns, $t_f = 6$ ns (2) The capacitance C_L includes stray wiring
- capacitance and the probe input capacitance.







MITSUBISHI HIGH SPEED CMOS

M74HC563P/FP/DWP

OCTAL 3-STATE INVERTING D-TYPE TRANSPARENT LATCH

DESCRIPTION

The M74HC563 is a semiconductor integrated circuit consisting of eight three-state-output D-type latches with common latch-enable input and output-enable input.

FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 12ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2∼6V
- Wide operating temperature range: T_a=-40~+85℃

APPLICATION

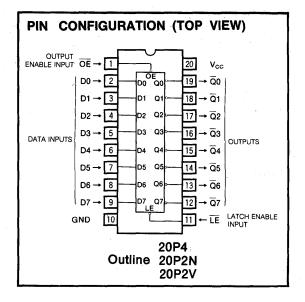
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC563 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS563.

The M74HC563 consists of eight D-type latches with latchenable input $\overline{\text{DE}}$ and output-enable input $\overline{\text{OE}}$ common to all circuits.

When \overline{LE} is high, the signals of data input D will go through the latch and be output to inverted output \overline{Q} . When the state of D changes, the state of \overline{Q} will also change. When

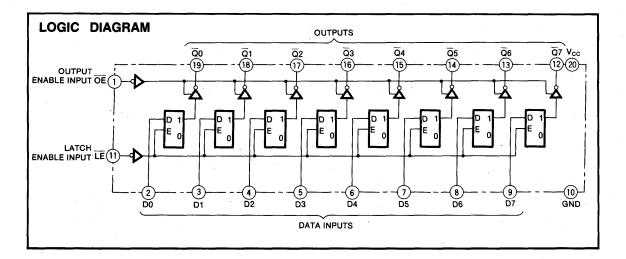


LE changes from high-level to low-level, the data existing immediately prior to the change at D will be stored in the latch.

Even if other inputs are changed when $\overline{\text{LE}}$ is low, the contents stored in the latch will not be affected.

When \overline{OE} is high, all outputs \overline{Q} will become high-impedance state.

A version of the M74HC563 with the same pin connections and a noninverted output, the M74HC573, is also available.



FUNCTION TABLE (Note 1)

	Inputs		Output
ŌĒ	LE	D	Q
L	Н	н	L
L	н	L	н
L	L	X	Q٥
н	Х	×	Z

Note 1: Qo: Output state Q before LE changed

Z : High impedance

X : Irrelevant

ABSOLUTE MAXIMUM RATINGS ($\tau_a = -40 \sim +85 \degree$ C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
	Input protection diode current	V ₁ < 0V	-20	
lik		V _I > V _{CC}	. 20	mA
	C. A. A	V ₀ < 0V	-20	
ок	Output parasitic diode current	Vo > Vcc	20	mA
lo	Output current per output pin		±35	mA
Icc	Supply/GND current	V _{CC} , GND	±75	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65~ +150	ဗ

Note 2 : M74HC563FP, $T_a=-40\sim+75^\circ$ C and $T_a=75\sim85^\circ$ C are derated at -7mW/°C. M74HC563DWP, $T_a=-40\sim+80^\circ$ C and $T_a=80\sim85^\circ$ C are derated at -7mW/°C.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85^{\circ}C)$

Symbol	Parameter			Limits				
Symbol	ra	rameter	Min	Тур	Max	Unit		
Vcc	Supply voltage		2		6	٧		
V _i	Input voltage	Input voltage			Vcc	٧		
Vo	Output voltage		0		Vcc	· >		
Topr	Ambient operating temperating	erature	-40		+85	°		
		V _{CC} == 2.0V	. 0		1000			
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns		
	V _{CC} = 6.0V		0		400			

ELECTRICAL CHARACTERISTICS

							Limits			
Symbol	Parameter	Test	Test conditions V _{CC} (V)		25℃			-40~+85°C		Unit
					Min	Тур	Max	Min	Max	i - I
		$V_0 = 0.1V, V_0$	0.114	2.0	1.5			1.5		
V _{IH}	High-level input voltage	$ V_0 = 0.1V, V_0$ $ V_0 = 20\mu A$	c0.1 V	4.5	3. 15			3.15	ļ	V
		1101 - 20µA		6.0	4.2			4.2		:
		V. = 0.1V. V.	$_{0} = 0.1V, V_{CC} - 0.1V$				0.5	l.	0.5	
ViL	Low-level input voltage	$ I_0 = 20\mu A$	C-0.1V	4.5	1	,	1.35		1.35	V
	<u> </u>	1101 - 20µA		6.0			1.8		1.8	
	IOH =		$I_{OH} = -20\mu A$	2.0	1.9			1.9		
		Іон	$I_{OH} = -20\mu A$	4.5	4.4	Ì	Ì	4.4		
VoH	High-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OH} = -20\mu A$	6.0	5. 9		2.45	5.9		V
			$I_{OH} = -6.0 \text{mA}$	4.5	4. 18			4.13		
		L	$I_{OH} = -7.8 mA$	6.0	5.68	ļ	ļ	5.63		
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
		l .	$I_{OL} = 20 \mu A$	4.5		}	0.1	ì	.0.1	ł
VoL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0	1		0.1		0.1	V
		}	1 _{OL} = 6.0mA	4.5			0.26		0.33	
			I _{OL} = 7.8mA	6.0	l	·	0.26		0, 33	
i _{IH}	High-level input current	V ₁ = 6V		6.0			0. 1		1.0	μA
I _{IL}	Low-level input current	V₁ = 0V		6.0			-0.1		-1.0	μΑ
lozh	Off-state high-level output current	$V_i = V_{iH}, \ V_{iL},$	$v_o = v_{cc}$	6.0			0.5		5.0	μА
lozL	Off-state low-level output current	$V_{l} = V_{lH}, V_{lL},$	V _O = GND	6.0			-0.5		-5.0	μA
Icc	Quiescent supply current	VI = VCC, GNE	$I_0 = 0\mu A$	6.0			4.0		40.0	μΑ

SWITCHING CHARACTERISTICS $(v_{co} = 5v, T_a = 25^{\circ})$

0	D	*		Limits			
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit	
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns	
t _{THL}	output transition time				10	ns	
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = 50pF (Note 4)			25	ns	
t _{PHL}	output propagation time $(D - \overline{Q})$				25	ns	
t _{PLH}	Low-level to high-level and high-level to low-level				30	ns	
t _{PHL}	output propagation time (LE - Q)				30	ns	
t _{PLZ}	Output disable time from low-level and high-level	0 = 5 = 5 (Net- 4)			25	ns	
t _{PHZ}	$(\overline{OE} - \overline{Q})$	C _L = 5 pF (Note 4)			25	ns	
t _{PZL}	Output enable time to low-level and high-level	0 - 50-5 (N-1-4)			28	ns	
t _{PZH}	(OE - Q)	C _L = 50pF (Note 4)			28	ns	

SWITCHING CHARACTERISTICS $(v_{cc} = 2\sim6v, \tau_a = -40\sim+85^{\circ}C)$

		Personator Test conditions				Limits		1.0505	Unit
Symbol	Parameter	Parameter Test conditions			25℃			+85℃	Uni
			V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0			60		75	
t _{TLH}	Low-level to high-level and		4.5		ĺ	12		15	ns
	high level to level	C = 50=5 (Note 4)	6.0			10		. 13	
	high-level to low-level	$C_L = 50 pF (Note 4)$	2.0			60		75	
t _{THL}	output transition time		4.5	,		12		15	ns
		1	6.0			10		13	ĺ
			2.0			150		189	
t _{PLH}			4.5			30		38	n
*PLH			6.0			26		32	
	1	$C_L = 50 pF $ (Note 4)	2.0			150		189	
	Landanial to blob local and		4.5			30		. 38	
t _{PHL}	Low-level to high-level and						-		n
	high-level to low-level		6.0			26		32	
	output propagation time	1	2.0			200		252	ĺ
t _{PLH}	$(D-\overline{Q})$		4.5			40		50	n
		C _L = 150pF (Note 4)	6.0			34		43	
		St - 190bi (140fe 4)	2. 0			200		252	
t _{PHL}			4.5			. 40		50	n
			6.0			34		43	
			2.0			175		221	
t _{PLH}	ч		4.5			35		44	l n
YPLH			6.0			30		37	"
	·	C _L = 50pF (Note 4)	2.0			175		221	
	I ow-level to high-level and		l l		1	35			_
Low-level to high-level and		4.5					44	n	
	high-level to low-level		6.0			30		37	
	output propagation time	·	2.0		[225		284	
t _{PLH}	(LE - Q)		4.5			45		57	n
		C _L = 150pF (Note 4)	6.0			38		48	
		Se resp. (mote t)	2.0			225		284	
t _{PHL}			4.5		ļ	45		57	n
			6.0			38		48	
-			2.0			150		189	
t _{PLZ}	Output disable time from		4.5			30		38	n
			6.0			26		32	
	low-level and high-level	C _L = 50pF (Note 4)	2.0		 	150		189	
taua	$(\overline{OE} - \overline{Q})$		4.5		1	30	}	38	n
t _{PHZ}	(02 (0)		6.0			26		32	"
ď			2.0			150		189	
t _{PZL}			4.5		ł	30		38	n
	<u> </u>	C _L = 50pF (Note 4)	6.0			26		32	
		1 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	2.0			150		189	
t _{PZH}	Output enable time to		4.5			30		38	n
	low lovel and high love!		6.0			26		32	<u> </u>
	low-level and high-level		2.0			200		252	
t _{PZL}	$(\overline{OE} - \overline{Q})$		4.5]	40		50	n
			6.0			34		43	
	1 4	C _L = 150pF (Note 4)	2.0			200		252	
t		1	4.5			40		50	n
t _{PZH}	1	*	6.0			34		43	"
			6.0		ļ				
C _i	Input capacitance					10	ļ	10	р
	Off-state output capacitance	OE = V _{CC}	1	l	1	15	I	15	p

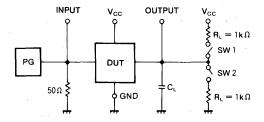
Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot v_{CC}^2 \cdot f_i + I_{CC} \cdot v_{CC}$



TIMING REQUIREMENTS ($v_{cc} = 2\sim6$ V, $T_a = -40\sim+85$ °C)

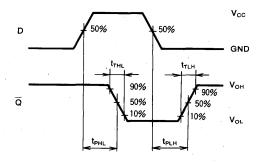
				Limits					
Symbol	Parameter	Test conditions		25℃			-40~+85℃		Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	
		2.0	80			101			
tw	Latch enable pulse width		4.5	16			20		ns
			6.0	14			17	1	
	Donatura kimana unitah		2.0	75			90		
tsu	D setup time with		4.5	15			. 18	ì	ns
	respect to LE		6.0	13			16		
	D hold time with		2.0	50		-	60		
th	th		4.5	10			12		ns
	respect to LE		6.0	9			11		

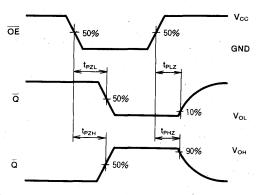
Note 4: Test Circuit

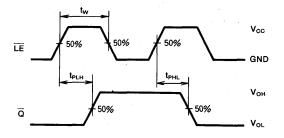


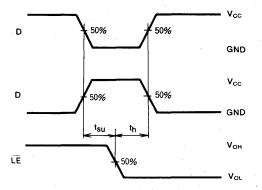
Parameter	SW 1	SW 2
t _{TLH} , t _{THL}	Open	Open
t _{PLZ}	Closed	Open
t _{PHZ}	Open	Closed
t _{PZL}	Closed	Open
t _{PZH}	Open	Closed

- (1) The pulse generator (PG) has the following characteristics (10%~90%): $t_{\rm f}=6{\rm ns},\,t_{\rm f}=6{\rm ns}$
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.











MITSUBISHI HIGH SPEED CMOS

M74HC564P/FP/DWP

OCTAL 3-STATE INVERTING D-TYPE FLIP-FLOP

DESCRIPTION

The M74HC564 is a semiconductor integrated circuit consisting of eight edge-triggered D-type flip-flops with 3-state outputs, common clock input and output-enable input.

FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: (clock frequency) 40MHz typ.
 (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC} , min (V_{CC} =4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2∼6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

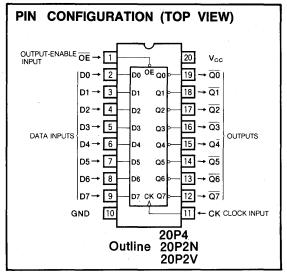
Use of silicon gate technology allows the M74HC564 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS564.

The M74HC564 contains eight edge-triggered D-type flipflops, sharing common clock input CK and output-enable input $\overline{\text{OE}}$.

When CK changes from low-level to high-level, the signals just previously input at D stores in the flip-flop.

When output-enable input \overline{OE} is low, the signals stored in the flip-flop will be inverted and output to \overline{Q} .

When the \overline{OE} is high, all outputs \overline{Q} will become high impedance state. Even if \overline{OE} is changed, the contents stored in the flip-flop will not be affected.



A version of the M74HC564 with the same pin connections and a noninverted output, the M74HC574, is also available.

FUNCTION TABLE (Note 1)

	Inputs			
ŌĒ	CK	D	Output Q	
L	†	L	н	
L	t	Н	L	
L	L	X	Q°	
L	Н	X	Q°	
\ L	1	Х	Q°	
Н	х	×	z	

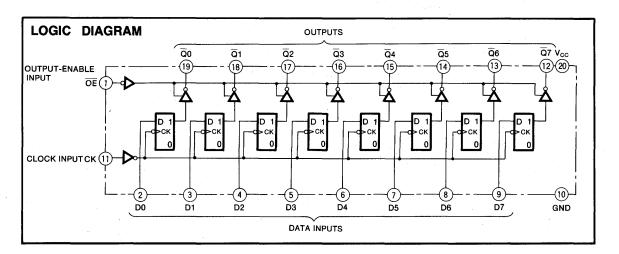
Note 1: Qo: Output state Q before CK changed

Z : High impedance

X : Irrelevant

† : Change from low-level to high-level

↓ : Change from high-level to low-level



ABSOLUTE MAXIMUM RATINGS $(\tau_a = -40 \sim +85 ^{\circ}C)$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
V _t	Input voltage	,	-0.5~V _{cc} +0.5	٧
Vo	Output voltage		-0.5~V _{cc} +0.5	V
	IK Input protection diode current	V ₁ < 0V	-20	
lik		V _I > V _{CC}	20	mA
		V ₀ < 0V	-20	
Іок	Output parasitic diode current	Vo > Vcc	20	mA
l _o	Output current per output pin		±35	mA
lcc	Supply/GND current	Vcc, GND	±75	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65~ + 150	°C

Note 2 : M74HC564FP, $T_a=-40\sim+75^\circ$ C and $T_a=75\sim85^\circ$ C are derated at -7mW/°C. M74HC564DWP, $T_a=-40\sim+80^\circ$ C and $T_a=80\sim85^\circ$ C are derated at -7mW/°C.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85\%)$

Cumb at				Limits					
Symbol	ra	rameter	Min	Тур	Max	Unit			
Vcc	Supply voltage		2		6	٧			
V,	Input voltage		0		Vcc	٧			
Vo	Output voltage		0		V _{cc}	٧			
Topr	Ambient operating temper	erature	-40		+85	င			
		$V_{CC} = 2.0V$	0		1000				
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns			
		$V_{CC} = 6.0V$	0		400	-			

ELECTRICAL CHARACTERISTICS

							Limits			
Symbol	Parameter	Test	conditions			25℃		-40~	+85°C	Unit
		V _{cc} (V		V _{CC} (V)	Min	Тур	Max	Min	Max	
		V = 0 1V V	-0.17	2, 0	1.5			1.5		
V _{IH}	High-level input voltage	$V_0 = 0.1V, V_{CO}$ $ I_0 = 20\mu A$	5—0.1 V	4.5	3.15			3. 15	i	٧.
		1161 — 20µA		6.0	4.2]	4.2]	
		$V_0 = 0.1V, V_{CC}$	_0.17	2.0			0.5		0.5	
VIL	Low-level input voltage	$ V_0 = 0.1V$, V_{CO}	5—0. T V	4.5			1.35		1.35	٧
	<u> </u>	1161 - 20µA		6.0			1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
	. 		$I_{OH} = -20\mu A$	4.5	4. 4			4.4		
V _{OH}	High-level output voltage	$V_i = V_{iH}, V_{iL}$ I_O	$I_{OH} = -20\mu A$	6.0	5.9	ĺ		5.9		V
			$I_{OH} = -6.0 \text{mA}$	4.5	4. 18	1		4.13		
			$I_{OH} = -7.8 \text{mA}$	6.0	5.68			5. 63		
		-	$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
			$I_{OL} = 20 \mu A$	4.5			0.1		0.1	
VoL	Low-level output voltage	$V_{i} = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1	į	0.1	V
	* * * * * * * * * * * * * * * * * * *	† ·	$I_{OL} = 6.0 \text{mA}$	4.5			0. 26		0.33	
		<u> </u>	I _{OL} = 7.8mA	6.0			0.26		0.33	
I _{IH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μA
I _{IL}	Low-level innput current	V ₁ = 0V		6.0			-0.1		-1.0	μΑ
lozh	Off-state high-level output current	$V_{I} = V_{IH}, V_{IL}, V_{IL}$	$V_0 = V_{CC}$	6.0			0.5		5.0	μΑ
lozL	Off-state low-level output current	$V_i = V_{iH}, \ V_{iL}, \ V_{iL}$	Vo = GND	6.0			-0.5		-5.0	μΑ
Icc	Quiescent supply current	VI = VCC, GND	$I_0 = 0 \mu A$	6.0			4.0		40.0	μΑ

SWITCHING CHARACTERISTICS $(V_{cc} = 5V, T_a = 25^{\circ}C)$

Symbol	Parameter	Test conditions		Unit		
Symbol	Farameter	Test conditions	Min	Тур	Max	Unit
fmax	Maximum clock frequency		35			MHz
t _{TLH}	Low-level to high-level and high-level to low-level				10	
t _{THL}	output transition time Low-level to high-level and high-level to low-level	$C_L = 50pF (Note 4)$			10	ns
t _{PLH}					32	
t _{PHL}	output propagation time (CK $-\overline{Q}$)				32	ns
t _{PLZ}	Output disable time from low-level and high-level	0 5 5 (1) (1)			25	
teHZ	$(\overline{OE} - \overline{Q})$	$C_L = 5 pF (Note 4)$			25	ns
tpzL	Output enable time to low-level and high-level	enable time to low-level and high-level			28	
t _{PZH}	$(\overline{OE} - \overline{Q})$	$C_L = 50 pF \text{ (Note 4)}$			28	ns

SWITCHING CHARACTERISTICS $(V_{cc} = 2\sim6V, T_a = -40\sim+85^{\circ}C)$

						Limits			
Symbol	Parameter	Test conditions			25℃		-40~	+85℃	Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0	6			5		
fmax	Maximum clock frequency		4.5	30	1		24	ļ	МН
	•		6. 0	35			28		
			2.0			60		75	
t _{TLH}	Low-level to high-level and	C _L = 50pF (Note 4)	4. 5		ļ	12		15	
	high-level to low-level	• •	6.0			10_		13	ns
	High-level to low-level		2.0			60		. 75	115
t _{THL}	output transition time		4.5			12	l	15	
. 1			6.0			10	Ì	13	
			2.0			180		227	
t _{PLH}			4.5			36		45	
		0 = F0=F (N=: 4)	6.0			31		39	
	1	C _L = 50pF (Note 4)	2.0			180		227	
t _{PHL}	Low-level to high-level and		4.5			36		45	ns
	high-level to low-level	•	6.0			31	Ì	39	
	output propagation time		2.0			230		290	
t _{PLH}	(CK - Q)		4.5			46		58	
			6.0		1	39		49	1
	1 .	$C_L = 150pF (Note 4)$	2.0			230		290	<u> </u>
t _{PHL}			4.5			46		58	
		ļ .	6.0			39		49	
	<u> </u>		2.0			150		189	†
t _{PLZ}	Output disable time from		4.5			30		38	
	•		6.0			26		32	
	low-level and high-level	C _L = 50pF (Note 4)	2.0			150		189	ns
t _{PHZ}	$(\overline{OE} - \overline{Q})$		4.5			30		38	i
·FHZ	(32 4)	,	6.0			26		32	
		1	2.0			150		189	
t _{PZL}			4.5		1	30		38	
*PZL			6.0			26		32	
	†	$C_L = 50 pF (Note 4)$	2.0		-	150	-	189	+
t _{PZH}	Output enable time to		4.5			30		38	
•PZH	Surpar onable time to		6.0			26		32	
	low-level and high-level	· · · · · · · · · · · · · · · · · · ·	2.0		 	200	 	252	ns
t	$(\overline{OE} - \overline{Q})$		4.5			40		50	
t _{PZL}	(OL W)		6.0			34		43	
	1	C _L = 150pF (Note 4)	2.0		-	200		252	+
			4.5			40		50	
t _{PZH}									
			6.0			34	 	43	 —
Cı	Input capacitance					10	-	10	
Co	Off-state output capacitance	OE = V _{CC}				15		15	pF

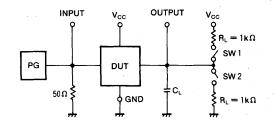
Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per flip flop) The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$



TIMING REQUIREMENTS ($v_{cc} = 2\sim 6V$, $T_a = -40\sim +85^{\circ}C$)

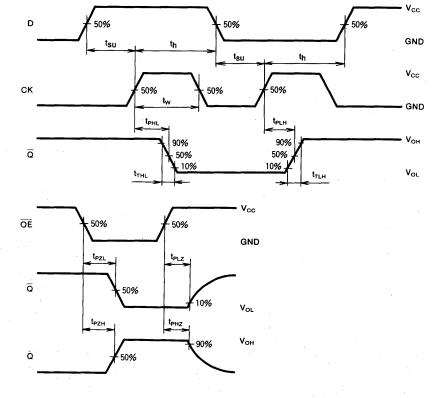
				Limits					
Symbol	Parameter	Test conditions		25°C			-40~+85℃		Unit
	*		V _{cc} (V)	Min	Тур	Max	Min	Max	1
			2.0	80			101		
tw	Clock pulse width		4.5	16	İ		20		ns
	<u> </u>		6.0	14			17		i
	B		2,0	75			90		
tsu	D setup time with		4.5	15	1		18	ł	ns
	respect to CK		6.0	13			16		l
	D hold time with		2.0	50			60	,	ļ
th			4.5	10			12		. ns
	respect to CK		6.0	9			11		

Note 4 : Test Circuit



Parameter	SW1	SW 2
t _{TLH} , t _{THL} t _{PLH} , t _{PHL}	Open	Open
t _{PLZ}	Closed	Open
t _{PHZ}	Open	Closed
t _{PZL}	Closed	Open
t _{PZH}	Open	Closed

- (1) The pulse generator (PG) has the following characteristics (10%~90%): $t_{\rm f}=6{\rm ns},\,t_{\rm f}=6{\rm ns}$
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.



MITSUBISHI HIGH SPEED CMOS

M74HC573P/FP/DWP

OCTAL 3-STATE NONINVERTING D-TYPE TRANSPARENT LATCH

DESCRIPTION

The M74HC573 is a semiconductor integrated circuit consisting of eight 3-state output D-type latches with common enable input and output-enable input.

FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=-6mA)
- High-speed: 12ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

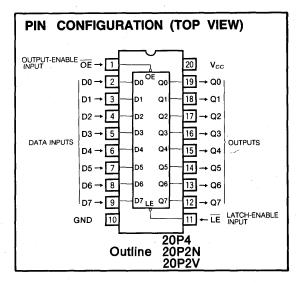
Use of silicon gate technology allows the M74HC573P to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS573.

The M74HC573 cosists of eight D-type latches with latchenable input $\overline{\text{LE}}$ and output-enable input $\overline{\text{OE}}$ common all circuits

When $\overline{\text{LE}}$ is high, the signals of data input D will go through the latch and be output to Q. When the state of D changes, the state of Q will also change. When $\overline{\text{LE}}$ changes from high-level to low-level, the data existing immediatery piror to the change at D will be stored in the latch.

Even if other inputs are changed when $\overline{\text{LE}}$ is low, the contents stored in the latch will not be affected.

When output enable input \overline{OE} is high, all outputs Q will become high impedance state.



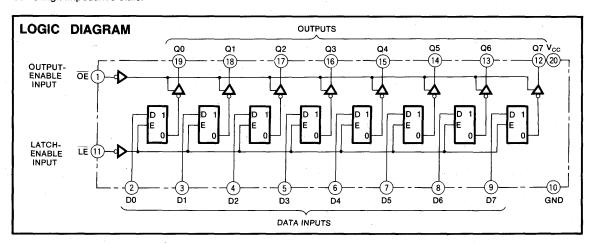
A version of the M74HC573 with the same pin connections and an inverted output, the M74HC563, is also available.

FUNCTION TABLE (Note 1)

	Inputs		Output
ŌĒ	OE LE		Q
L	Н	Н	Н
L	н	Ĺ	L
L	L	х	Q°
Н	X	X	z

Note 1: Q0: Output state Q before LE changed

Z : High impedance



ABSOLUTE MAXIMUM RATINGS $(T_a = -40 \sim +85\%$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{CC} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
L	Input protection diode current	V ₁ < 0V	-20	
lik	input protection diode current	V _I > V _{CC}	20	mA
1	Output parasitic diode current	V ₀ < 0V	-20	T .
Т ОК	Output parasitic diode current	Vo > Vcc	20	mA
lo	Output current, per output pin		±35	mA
loc	Supply/GND current	V _{CC} , GND	±75	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		-65~十150	င

Note 2 : M74HC573FP, $T_a=-40\sim+75^\circ$ C and $T_a=75\sim85^\circ$ C are derated at $-7mW/^\circ$ C. M74HC573DWP, $T_a=-40\sim+80^\circ$ C and $T_a=80\sim85^\circ$ C are derated at $-7mW/^\circ$ C.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85 \text{ C})$

Symbol	Parameter			Limits					
Зупьы	ra	rameter	Min	Тур	Max	Unit			
Vcc	Supply voltage		2		6	V			
Vı	Input voltage		0		V _{cc}	V			
Vo	Output voltage		0		Vcc	٧			
Topr	Operating temperature ra	ange	40		+85	င			
		V _{CC} = 2.0V	0		1000				
t _r , t _f	Input risetime, falltime	V _{CC} = 4.5V	0		500	ns			
		$V_{CC} = 6.0V$	0		400				

ELECTRICAL CHARACTERISTICS

							Limits	-		
Symbol	Parameter	Test	conditions			25℃		-40~	+85℃	Unit
		V _{CC} (V)		Min	Тур	Max	Min	Max		
		V = 0.1V V	0.11/	2.0	1.5			1.5		
VIH	High-level input voltage	$ V_0 = 0.1V, V_{CO} $ $ I_0 = 20\mu A$	5—U. 1 V	4.5	3.15	Į		3. 15		v
		$ 1_0 = 20\mu\text{A}$		6.0	4.2			4.2		
		V = 0.1V V	0.11/	2.0			0.5		0.5	
VIL	Low-level input voltage	$V_0 = 0.1V, V_{cc}$	U. IV	4,5		l	1.35		1.35	V
		$ I_0 = 20\mu A$		6.0			1.8		1.8	
			$I_{OH} = -20 \mu A$	2.0	1.9			1.9		
V _{OH} High-level output voltage			$I_{OH} = -20\mu A$	4.5	4.4			4.4		
	$V_i = V_{iH}, V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		V	
			$I_{OH} = -6.0 \text{mA}$	4.5	4.18			4.13		Ì
	V 1		$I_{OH} = -7.8 \text{mA}$	6.0	5.68			5.63	-	
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
			$I_{OL} = 20 \mu A$	4.5			0.1		0.1	İ
VoL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
			$I_{OL} = 6.0 \text{mA}$	4.5			0. 26		0.33	
	·		I _{OL} = 7.8mA	6.0			0. 26		0.33	
I _{IH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μА
I _{IL}	Low-level input current	$V_i = 0V$		6, 0			-0.1		-1.0	. μΑ
lozh	Off-state high-level output current	$V_i = V_{iH}, \ V_{iL},$	Vo = Vcc	6.0			0.5		5.0	μА
IOZL	Off-state low-level output current	$V_i = V_{iH}, \ V_{iL},$	Vo = GND	6.0			-0.5		-5.0	μΑ
l _{oc}	Quiescent supply current	VI = VCC, GND	$I_0 = 0\mu A$	6.0			4.0		40.0	μA

MT4HC573P/FP/DWP

OCTAL 3-STATE NONINVERTING D-TYPE TRANSPARENT LATCH

SWITCHING CHARACTERISTICS $(v_{cc} = 5v, T_a = 25\%)$

Symbol	Parameter	Test conditions		Limits			
Symbol	Parameter	rest conditions	Min	Тур	Max	Unit	
tTLH	Low-level to high-level and high-level to low-level				10	ns	
t _{THL}	output transition time	utput transition time					
tpLH	Low-level to high-level and high-level to low-level			19			
t _{PHL}	output propagation time (D - Q)	$C_L = 50 pF \text{ (Note 4)}$			19	ns	
t _{PLH}	Low-level to high-level and high-level to low-level				20		
t _{PHL}	output propagation time (LE - Q)				20	ns	
t _{PLZ}	Output disable time from low-level and high-level	0 - 5 - 5 (N-4-4)			20		
t _{PHZ}	(OE - Q)	C _L = 5 pF (Note 4)			20	ns	
tezL	Output enable time to low-level and high-level	0 - 50-5 (N-4-4)			25		
tezn	(OE – Q)	$C_L = 50 pF \text{ (Note 4)}$			25	กร	

SWITCHING CHARACTERISTICS ($v_{cc} = 2\sim 6V$, $T_a = -40\sim +85$ °C)

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Symbol	Parameter	Test conditions			25℃	Limits	-40-	+85℃	Un
Symbol	Parameter	lest conditions	V _{cc} (V)	Adim		May	Min		Un
			2.0	Min	Тур	Max 60	- Mill	75	<u> </u>
	. *							l	ł
TLH	Low-level to high-level and		4.5			12		15	ļ
	high-level to low-level	C _L = 50pF (Note 4)	6.0			10		13	n
	output transition time		2.0			60		75	
t _{THL}	cutput transition time		4.5		١	12		15	
		1	6.0			10		13	
			2.0	,		110		138	
t _{PLH}	· ·		4.5		, i	22		28	l
·		$C_L = 50 pF (Note 4)$	6.0		ļ	19		24	
			2.0		1.	110	Ì	138	
t _{PHL}	Low-level to high-level and		4.5		l	22		28	1
	high-level to low-level		6.0			19		24	n
	output propagation time	1	2.0			150		188	"
t _{PLH}	(D - Q)		4.5			30		38	-
	_	C _L = 150pF (Note 4)	6.0		L	26		33]
		OL - 13001 (14018 4)	2.0			150		188	
t _{PHL}			4.5	}.		30	1	38	1
			6.0			26		33	
			2.0			115		143	
t _{PLH}			4.5			23		29	
		, in F(1) , (1)	6.0	l		20		25	l
	1	$C_L = 50 pF \text{ (Note 4)}$	2.0			115		143	1
t _{PHL}	Low-level to high-level and		4.5		1	23		29	Ì
	high-level to low-level		6.0	1	}	20	}	25	
	output propagation time		2.0			155		194	r
t _{PLH}	(LE - Q)		4.5		Į.	31		47	1
			6.0			27		34	
	7	$C_L = 150 pF $ (Note 4)	2.0		1	155	T	194	
t _{PHL}			4.5			31		47	
			6.0	}		27	1	34	
			2.0			125		156	† –
t _{PLZ}	Outros diserble disers from		4.5	ĺ		25	1	31	1
	Output disable time from	·	6.0			21		27	
	low-level and high-level	C _L = 50pF (Note 4)	2.0	-	†	125		156	- r
t _{PHZ}	(<u>OE</u> – Q)		4.5		1	25	1	31	
*PHZ			6.0	1		21	1	27	
	+	+	2, 0	 	+	140	 	175	+
t _{PZL}			4.5	1	ţ	28		35	-
PZL			6.0		1	24	1	30	
	1	C _L = 50pF (Note 4)	2.0	 	+	140		175	+
			4.5			28	1.	35	1
t _{PZH}	Output enable time to	1	6.0	1		28	1	30	1
	low-level and high-level		2.0		+	180		225	r
	(OE - Q)		1	ļ					1
t _{PZL}	1		4.5		1	36		45	1
	-	C _L = 150pF (Note 4)	6.0	 	+	31	 	39	-
. :	4		2.0			180		225	
t _{PZH}			4.5			36		45	1
	 	1:	6.0	-		31	-	39	↓ _
Cı	Input capacitance					10		10	4
Co	Off-state output capacitance	OE = V _{CC}		1	1	15	1	15	l p

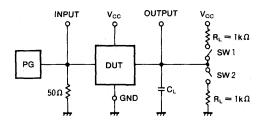
Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per latch)
The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$



TIMING REQUIREMENTS $(V_{cc} = 2\sim6V, T_a = -40\sim+85\%)$

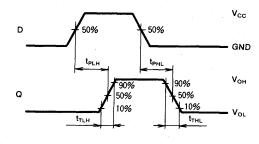
	Parameter	Test conditions		Limits					
Symbol				25℃		-40~+85℃		Unit	
			V _{cc} (V)	Min	Тур	Max	Min	Max	1
t _w	Latch enable pulse width		2.0	80			101		
			4.5	16		ļ	20		ns
			6.0	14			17		
t _{SU}	D setup time with respect to LE	*	2.0	75			95		
			4.5	15			19		ns
			6.0	13	_		16		1
th	D hold time with respect to LE		2.0	25			31		
			4.5	5			6		ns
			6.0	4		l	- 5		1

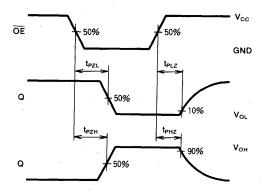
Note 4: Test Circuit

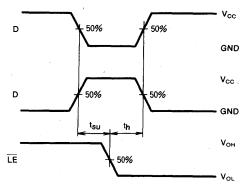


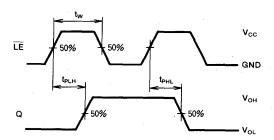
Parameter	SW 1	SW 2		
t _{TLH} , t _{THL}	Open	Open		
t _{PLZ}	Closed	Open		
t _{PHZ}	Open	Closed		
t _{PZL}	Closed	Open		
t _{PZH}	Open	Closed		

- (1) The pulse generator (PG) has the following characteristics (10% \sim 90%): $t_f = 6ns$, $t_f = 6ns$
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.











MITSUBISHI HIGH SPEED CMOS

M74HC574P/FP/DWP

OCTAL 3-STATE NONINVERTING D-TYPE FLIP-FLOP

DESCRIPTION

The M74HC574 is a semiconductor integrated circuit consisting of eight edge-triggered D-type flip-flops with 3-state outputs, common clock input and output-enable input.

FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: (clock frequency) 65MHz typ.
 (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=-40~+85℃

APPLICATION

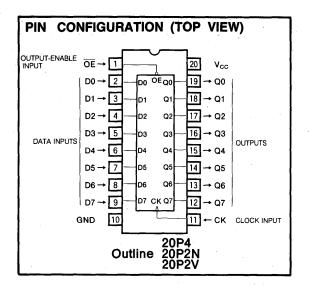
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC574 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS574.

The M74HC574 contains eight edge-triggered D-type flip-flops, sharing common clock input CK and output-enable input \overline{OE}

When CK changes from low-level to high-level, the signals

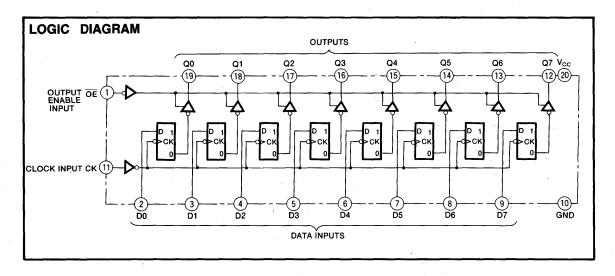


just previously input at D stores in the flip-flop.

When output-enable input \overline{OE} is low, the signals stored in the flip-flop will be output to Q.

When \overline{OE} is high, all outputs Q will become high impedance state. Even if \overline{OE} is changed, the contents stored in the flip-flop will not be affected.

A version of the M74HC574 with the same pin connections and an inverted output, the M74HC564, is also available.



OCTAL 3-STATE NONINVERTING D-TYPE FLIP-FLOP

FUNCTION TABLE (Note 1)

	Inputs		Output
OE	СК	D	Q
L	1	L	L
L	1	Н	н
L	L	Х	Q°
L	Н	Х	Q°
L	1	Х	Q°
н	X	Х	Z

Note 1: Q⁰: Output state Q before CK changed

Z: High impedance
X: Irrelevant

† : Change from low-level to high-level

↓ : Change from high-level to low-level

ABSOLUTE MAXIMUM RATINGS ($\tau_a = -40 \sim +85^{\circ}$ C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
V _I	Input voltage	,	-0.5~V _{cc} +0.5	٧
Vo	Output voltage		-0.5~V _{cc} +0.5	V
1	Input protection diode current	V ₁ < 0V	-20	
l _{IK}	input protection glode current	$V_1 > V_{CC}$	20	mA
	Cutout non-this diada aumant	V ₀ < 0V	-20	
lok	Output parasitic diode current	$V_0 > V_{CC}$	20	mA
lo	Output current per output pin		±35	mA
Icc	Supply/GND current	V _{CC} , GND	土75	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		-65~+150	င

Note 2 : M74HC574FP, $T_a = -40 \sim +75^{\circ}\text{C}$ and $T_a = 75 \sim 85^{\circ}\text{C}$ are derated at $-7\text{mW}/^{\circ}\text{C}$. M74HC574DWP, $T_a = -40 \sim +80^{\circ}\text{C}$ and $T_a = 80 \sim 85^{\circ}\text{C}$ are derated at $-7\text{mW}/^{\circ}\text{C}$.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85^{\circ}C)$

Symbol	Day	rameter		Limits						
Syllibol	Pal	rameter	Min	Тур	Max	Unit				
Vcc	Supply voltage		2		6	٧				
V ₁	Input voltage		0		Vcc	V				
V _o	Output voltage	Output voltage				٧				
Topr	Ambient operating temper	erature	-40		+85	°				
		$V_{CC} = 2.0V$	0		1000					
r, tf Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns					
		$V_{CC} = 6.0V$	0		400					

MT4HC574P/FP/DWP

OCTAL 3-STATE NONINVERTING D-TYPE FLIP-FLOP

ELECTRICAL CHARACTERISTICS

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							Limits			
Symbol	Parameter	Test	conditions			25℃		-40~	+85℃	Unit
					Min	Тур	Max	Min	Max	
		$V_0 = 0.1V, V_{CC}$		2.0	1.5			1.5		
ViH	High-level input voltage		5. O. I V	4.5	3. 15			3.15		V
	<u> </u>	1101 - 20µA	$ I_{O} = 20\mu A$		4.2			4. 2		
		$V_0 = 0.1V, V_{CO}$	-0.17	2.0			0.5		0.5	
V _{IL}	Low-level input voltage	1 -	C-0. 1 V	4.5] .		1.35		1.35	V
		$ I_0 = 20\mu A$		6.0			1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
		İ	$I_{OH} = -20\mu A$	4.5	4.4			4.4		
VoH	V _{OH} High-level output voltage	$V_{l} = V_{lH}, V_{lL}$	$I_{OH} = -20\mu A$	6.0	5.9) .		5.9		v
			$I_{OH} = -6.0 \text{mA}$	4.5	4. 18			4.13		
			$I_{OH} = -7.8 \text{mA}$	6.0	5. 68			5.63		
			$I_{OL} = 20\mu A$	2.0			0.1		0.1	
	1	1	$I_{OL} = 20 \mu A$	4.5	1		0.1]	0.1	
VoL	Low-level output voltage	$V_i = V_{iH}, \ V_{iL}$	$I_{OL} = 20 \mu A$	6.0		l	0.1	<u></u>	0.1	V
	•		$I_{OL} = 6.0 \text{mA}$	4. 5			0.26		0.33	
			I _{OL} = 7.8mA	6.0			0. 26	ł	0.33	
l _{IH}	High-level input current	$V_1 = 6V$	•	6. 0			0.1		1.0	μA
I _{IL}	Low-level input current	V ₁ = 0V		6.0			-0.1		-1.0	μA
l _{ozh}	Off-state high-level output current	$V_i = V_{iH}, \ V_{iL},$	$V_0 = V_{CC}$	6.0			0,5		5.0	μА
lozL	Off-state low-level output current	$V_i = V_{iH}, \ V_{iL},$	$V_i = V_{iH}, \ V_{iL}, \ V_O = GND$				-0.5		-5.0	μA
loc	Quiescent supply current	VI = VCC, GNE	$I_0 = 0\mu A$	6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS $(v_{cc} = 5v, \tau_a = 25^{\circ}c)$

Sumb at	Parameter	Test conditions		Limits		Unit
Symbol	Parameter	lest conditions	Min	Тур	Max	Unit
fmax	Maximum clock frequency		35			MHz
t _{TLH}	Low-level to high-level and high-level to low-level				10	
t _{THL}	output transition time	C _L = 50pF (Note 4)		1	10	ns
t _{PLH}	Low-level to high-level and high-level to low-level				32	
t _{PHL}	output propagation time (CK — Q)				32	ns
t _{PLZ}	Output disable time from low-level and high-level	0 - 5 - 5 (N-4-4)			25	
t _{PHZ}	(OE - Q)	$C_L = 5 pF (Note 4)$			25	ns
t _{PZL}	Output enable time to low-level and high-level	0 - 50-5 (N-4-4)			28	
t _{PZH}	(OE - Q)	C _L = 50pF (Note 4)			- 28	ns

MITSUBISHI HIGH SPEED CMOS M74HC574P/FP/DWP

OCTAL 3-STATE NONINVERTING D-TYPE FLIP-FLOP

SWITCHING CHARACTERISTICS $(v_{cc} = 2\sim 6v, \tau_a = -40\sim +85^{\circ}C)$

Symbol	Parameter	Test conditions			25℃	Limits	-40-	+85℃	Unit
Symbol	Parameter	Test conditions	V (V)	h dia		Man			1 000
			V _{cc} (V)	Min	Тур	Max	Min	Max	
_	1		2.0	6	ļ		5	1	
fmax	Maximum clock frequency		4.5	30			24	1	МН
			6.0	35			28	<u> </u>	├ ─-
		1	2.0		1	60		75	
t _{TLH}	Low-level to high-level and	C _L = 50pF (Note 4)	4.5	*	}	12		15	ns
	high-level to low-level		6.0			10		13	<u> </u>
			2.0			60		75	
t _{THL}	output transition time		4.5			12		15	ns
			6.0			10		13	
`			2.0			180		227	
t _{PLH}			4.5			36	1	45	ns
		C _L = 50pF (Note 4)	6.0			31		39	l
	1	CL — Sopr (Note 4)	2.0			180		227	
t _{PHL}	Low-level to high-level and		4.5			36		45	ns
	high-level to low-level		6.0			31		39	1
	output propagation time		2.0			230		290	
t _{PLH}	(CK - Q)		4.5			46		58	ns
		2 150 5 (1) (1)	6.0			39		49	1
		$C_L = 150 pF \text{ (Note 4)}$	2.0			230		290	
t _{PHL}			4.5		ļ	46		58	ns
		ľ	6.0		l	39		49	1
<u> </u>	-		2.0			150		189	
t _{PLZ}	Output disable time from	*	4.5			30		38	ns
			6.0		l	26		32	
	low-level and high-level	C _L = 50pF (Note 4)	2.0			150		189	
t _{PHZ}	(OE - Q)		4.5		ļ	30		38	ns
-FNZ	1 .55		6.0			26		32	
			2.0			150		189	1-
t _{PZL}	Í		4.5		}	30		38	ns
*PZL			6.0			26		32	"
	+	C _L = 50pF (Note 4)	2.0			150		189	-
•	Output enable time to		4.5			30		38	ns
t _{PZH}	Output enable time to		6.0			26		32	118
	low-level and high-level		2.0			200		252	+
	(<u>o</u> E – o)		1 i			(i	`	1	
t _{PZL}	(ŌĒ — Q)		4.5			40		50	ns
		C _L = 150pF (Note 4)	6.0			34		43	├
			2.0			200		252	
t _{PZH}			4.5			40		50	ns
	<u> </u>		6.0		ļ <u>.</u>	34		43	
Cı	Input capacitance					10		10	pF
C _o	Off-state output capacitance	OE = V _{CC}				15		15	pF
C _{PD}	Power dissipation capacitance (Note 3) [1	1		1	pF

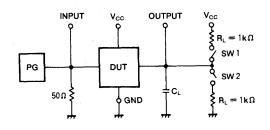
Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per flip flop) The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$

OCTAL 3-STATE NONINVERTING D-TYPE FLIP-FLOP

TIMING REQUIREMENTS ($v_{cc} = 2\sim6v$, $T_a = -40\sim+85^{\circ}C$)

						Limits			
Symbol	Parameter	Test conditions	4	25℃			-40~	+85℃	Unit
	randa da da da da da da da da da da da da d		V _{CC} (V)	Min	Тур	Max	Min	Max] '
			2.0	80			101		
tw	Clock pulse width		4.5	16	i	1	20		ns
			6.0	14			17		İ
			2.0	75			90		
tsu	D setup time with	,	4.5	15			. 18		ns
	respect to CK		6.0	13			16		[
	D bald Name with		2.0	50			60		
th	th D hold time with respect to CK		4.5	10		}	12		ns
			6.0	9		İ	11		

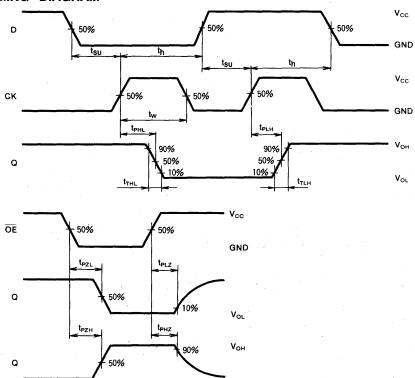
Note 4: Test Circuit



Parameter	SW 1	SW 2
t _{TLH} , t _{THL} t _{PLH} , t _{PHL}	Open	Open
t _{PLZ}	Closed	Open
t _{PHZ}	Open	Closed
t _{PZL}	Closed	Open
t _{PZH}	Open	Closed

- (1) The pulse generator (PG) has the following characteristics (10% \sim 90%): t_r = 6ns, t_f = 6ns
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



MITSUBISHI HIGH SPEED CMOS

M74HC595P/FP/DP

8-BIT SERIAL-INPUT/SERIAL-OR
PARALLEL-OUTPUT SHIFT REGISTER WITH LATCHED 3-STATE OUTPUTS

DESCRIPTION

The M74HC595 is a semiconductor integrated circuit consisting of an 8-bit serial input/parallel output shift register with 3-state output latch.

FEATURES

- High-speed: (clock frequency) 30MHz typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads (Q_A-Q_H)
 10 74LSTTL loads (SQ_H)
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=-40~+85℃

APPLICATION

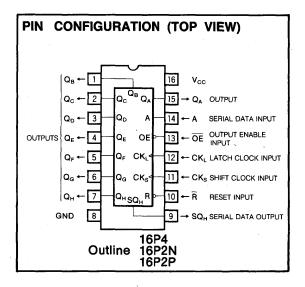
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC595 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS595.

Each bit of shift register consists of two flip flops with independent clocks for shift and latch.

The clock inputs contain independent shift clock input CKs and latch clock input CK_L. Shift and latch operations take place when the inputs change from low-level to high-level. Serial data input A is data input of the first shift register. When A is high and a pulse is applied to CKs, the high-level signal will be shifted in order. When A is low and a pulse is applied to CKs, the low-level signal will be shifted in order.



When a pulse is applied to CK_L , the contents of the shift register existing at that time will be stored in the latch register and appear at outputs Q_A through Q_H . Q_A through Q_H are buffered 3-state outputs.

To extend the number of bits, serial data output $SQ_{\rm H}$ is used to output the eighth bit of the shift register.

By connecting CKs and CK_L, the shift register state delayed by 1 clock cycle is output at Q_A through Q_H .

When reset input \overline{R} is low, shift register and SQ_H will be reset. To reset Q_A through Q_H to low-level, CK_L must be changed from low-level to high-level after the shift register is reset by \overline{R} .

When output-enable input \overline{OE} is high, Q_A through Q_H will becom high impedance state, but SQ_H is not changed. Even if \overline{OE} is changed, shift operation is not affected.

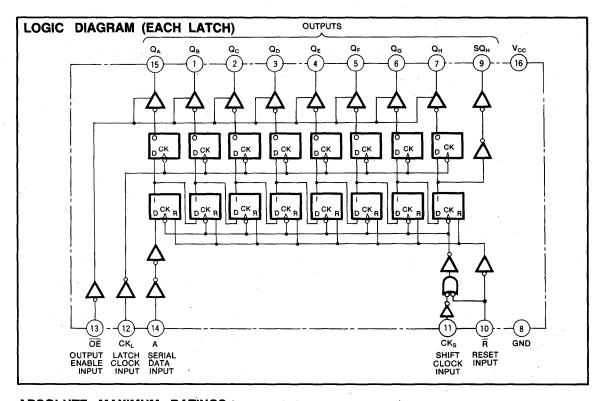
FUNCTION TABLE (Note 1)

0		Inputs			Outputs								Serial data		
Operation	n mode	R	CKs	CKL	Α	OE	QA	QB	Qc	QD	QE	Q _F	QG	Qн	output SQ _H
D4	Shift t ₁	L	х	х	×	L	Q _A ⁰	Q _B ⁰	Q _C ⁰	Q _D °	Q _E ⁰	Q _F ⁰	Q _G ⁰	Q _H ^o	L
Reset	Latch t ₂	х	×	1	. Х	L	L	L	L	L	L	L	L	L	L,
05:44	Shift t ₁	Н	t	х	Н	L	Q _A ⁰	Q _B ⁰	Q _C ⁰	Q _D °	Q _E ⁰	Q _F ⁰	Q _G ⁰	Q _H ⁰	q _G ⁰
Shift	Latch t ₂	Н	X	1	Х	L	Н	q _A o	q _B ⁰	q _c ⁰	q⊳°	q _E ⁰	q _F ⁰	q _G ⁰	q _G ⁰
latch	Shift t ₁	Н	1	х	L	L	Q _A ⁰	Q _B ⁰	Q _c ⁰	Q _D ⁰	Q _E ⁰	Q _F ⁰	Q _G ⁰	Q _H ⁰	q _G ⁰
operation	Latch t ₂	Н	Х	1	×	L	L	Q _A O	Q _B ⁰	q _c ⁰	q _D o	qe⁰	q _F 0	q _g ⁰	q _G ⁰
3 -s	tate	Х	X	Х	X	Н	Z	Z	z	Z	Z	Z	Z	Z	qн

- Note 1. † : Change from low-level to high-level
 - Q⁰: Output state Q before clock input is changed
 - X : Irrelevant
 - q0 : Contents of shift register before clock input changed
 - q : Contents of shift register
 - $t_1, t_2 : t_2$ is set after t_1 is set
 - : High impedance



8-BIT SERIAL-INPUT/SERIAL-OR PARALLEL-OUTPUT SHIFT REGISTER WITH LATCHED 3-STATE OUTPUTS



ABSOLUTE MAXIMUM RATINGS $(T_a = -40 \sim +85\%$, unless otherwise noted)

Symbol	Parameter		Conditions	Ratings	Unit
Vcc	Supply voltage			-0.5~+7.0	V
Vı	Input voltage			-0.5~V _{cc} +0.5	V
Vo	Output voltage			-0.5~V _{cc} +0.5	V
			V ₁ < 0V	-20	
lικ	Input protection diode current		$V_i > V_{CC}$	20	mA
			V _o < 0V	-20	
lok	Output parasitic diode current		$V_{\rm o} > V_{\rm cc}$	20	mA
		Q _A ~Q _H		±35	
lo	Output current per output pin	SQ _H		±25	mA
loc .	Supply/GND current		V _{CC} , GND	土75	mA
Pd	Power dissipation		(Note 2)	500	mW
Tstg	Storage temperature range			-65∼+150	ာင

Note 2 : M74HC595FP, $T_a=-40\sim+70^\circ$ C and $T_a=70\sim85^\circ$ C are derated at -6mW/°C. M74HC595DP, $T_a=-40\sim+50^\circ$ C and $T_a=50\sim85^\circ$ C are derated at -5mW/°C.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85 \%)$

O	D-			Limits		11-4
Symbol	Pa	rameter	Min	Тур	Max	Unit
Vcc	Supply voltage		2		6	V
Vı	Input voltage		0		V _{CC}	٧
Vo	Output voltage	1	0		V _{cc}	· V
Topr	Operating temperature ra	ange	-40		+85	°C
		$V_{CC} = 2.0V$	0		1000	
t _r , t _f	input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns
		0		400		

8-BIT SERIAL-INPUT/SERIAL-OR PARALLEL-OUTPUT SHIFT REGISTER WITH LATCHED 3-STATE OUTPUTS

ELECTRICAL CHARACTERISTICS

								Limits				
Symbol	Param	eter	Test conditions				25℃		-40~	+85℃	Unit	
					V _{CC} (V)	Min	Тур	Max	Min	Max		
			V _o = 0.1V, V _{cc} -0.1V		2.0	1.5			1.5			
V_{IH}	High-level input vo	oltage $ I_0 = 20\mu A $			4.5	3. 15			3.15		V	
			$ 1_0 = 20\mu\text{A}$		6.0	4.2			4.2			
			$V_0 = 0.1V$, V_{CC}	0.114	2.0			0.5		0.5		
V_{IL}	Low-level input vo	ltage	, .	5—0. TV	4.5			1.35		1.35	V	
			$ I_0 = 20\mu A$		6.0			1.8		1.8		
				$I_{OH} = -20 \mu A$	2.0	1.9			1.9	_		
				$I_{OH} = -20\mu A$	4.5	4. 4	1		4. 4		1	
V_{OH}	High-level	Q _A ~Q _H	$V_{I} = V_{IH}, V_{IL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		V	
	output voltage			$I_{OH} = -6.0 \text{mA}$	4.5	4. 18			4.13			
				$I_{OH} = -7.8 mA$	6.0	5. 68			5.63			
				$I_{OL} = 20 \mu A$	2.0			0. 1		0.1		
				$I_{OL} = 20 \mu A$	4.5			0.1		0.1		
VoL	Low-level output voltage	Q _A ~Q _H	Q _A ~Q _H	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
		itput voltage		I _{OL} = 6.0mA	4.5			0.26		0.33		
		.		I _{OL} = 7.8mA	6.0			0.26		0.33		
				$I_{OH} = -20\mu A$	2.0	1.9			1.9			
				$I_{OH} = -20\mu A$	4.5	4.4			4.4			
VoH	High-level	SQ _H	$V_I = V_{IH}, V_{IL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		V	
2	output voltage			$I_{OH} = -4.0 \text{mA}$	4.5	4.18			4.13			
				$I_{OH} = -5.2 \text{mA}$	6.0	5.68			5.63			
				$I_{OL} = 20\mu A$	2.0			0.1		0.1		
	1			$I_{OL} = 20 \mu A$	4.5			0.1		0.1		
VoL	Low-level	SQH	$V_{I} = V_{IH}, V_{IL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V	
	output voltage	ŀ		I _{OL} = 4.0mA	4.5			0.26		0.33		
				$I_{OL} = 5.2 \text{mA}$	6.0			0.26		0.33		
l _{iri}	High-level input co	urrent	$V_i = 6V$		6.0			0.1		1.0		
կը ·	Low-level input cu	rrent	V ₁ = 0V		6.0			-0.1		-1.0	μA	
lozh	Off-state high-leve	output current	$V_i = V_{iH}, \ V_{iL}, \ V_O = V_{CC}$		6.0			0.5		5.0		
I _{OZL}	Off-state low-level	output current	$V_I = V_{IH}, \ V_{IL}, \ V_{IL}$	$V_I = V_{IH}, V_{IL}, V_O = GND$				-0.5		-5.0	μA	
loc	Quiescent supply	current	VI = VCC, GND	$I_0 = 0\mu A$	6.0			4.0		40.0	μA	

SWITCHING CHARACTERISTICS $(v_{cc} = 5v, T_a = 25^{\circ}C)$

0		To ad a condition of		Limits		Unit
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
fmax	Maximum clock frequency	C _L = 50pF (Note 4)	30			MHz
t _{TLH}	Low-level to high-level and high-level to low-level	0 = 15-5 (N-4-4)			10	
t _{THL}	output transition time (SQ _H)	C _L = 15pF (Note 4)			10	ns
t _{TLH}	Low-level to high-level and high-level to low-level	0 = 50=5 (N-+-4)			10	
t _{THL}	output transition time (Q _A — Q _H)	$C_L = 50pF \text{ (Note 4)}$			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level				35	
t _{PHL}	output propagation time (CK _S — SQ _H)	0 = 15=5 (N=4=4)			35	ns
	High-level to low-level output propagation time	C _L = 15pF (Note 4)			30	ns
t _{PHL}	$(\overline{R} - SQ_H)$				30	113
t _{PLH}	Low-level to high-level and high-level to low-level	$C_L = 50 pF \text{ (Note 4)}$			30	ns
t _{PHL}	output propagation time (CK _L — Q _A ~Q _H)	C _L = 50pr (Note 4)			30	115
t _{PLZ}	Output disable time from low-level and high-level	C ₁ = 5 pF (Note 4)			25	ns
t _{PHZ}	(OE − Q _A ~Q _H)	OL — Spr (Note 4)			25	118
t _{PZL}	Output enable time to low-level and high-level	$C_1 = 50pF (Note 4)$			28	
t _{PZH}	(OE - Q _A ~Q _H)	CL = SUPF (NOIE 4)			28	ns

M74HC595P/FP/DP

8-BIT SERIAL-INPUT/SERIAL-OR PARALLEL-OUTPUT SHIFT REGISTER WITH LATCHED 3-STATE OUTPUTS

SWITCHING CHARACTERISTICS ($v_{cc} = 2\sim6V$, $T_a = -40\sim+85^{\circ}C$)

				· · · · ·	05%0	Limits	45	1.05%	
Symbol	Parameter	Test conditions	-		25℃	T		+85℃	Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	<u> </u>
			2.0	5			4		
fmax	Maximum clock frequency		4.5	27	į		21		MH
			.6.0	32			25		
			2.0			75		95	
t _{TLH}	Low-level to high-leveland		4.5			15	1	19	
	high-level to low-level		6.0			13		16	
	output transition time		2. 0			75		95	ns
t _{THL}	(SQ _H)		4.5			. 15		19	
	-	· ·	6.0			13	ĺ	16	
			2.0			60		75	
tTLH	Low-level to high-level and		4.5			12		15	
	high-level to low-level		6.0			10		13	
	output propagation time		2.0			60	<u> </u>	75	ns
t _{THL}	(Q _A ~Q _H)		4.5			12		15	
-184	1 - 11/		6.0		1	10	l	13	İ
		1	2.0			210		265	
t _{PLH}	Low-level to high-level and	C _L = 50pF (Note 4)	4.5			42	l	53	
чРСН	high-level to low-level	O[== 30pr (Note 47)	6.0			36		45	İ
	- -		2.0			210		265	ns
	output propagation time	-	I			1			
t _{PHL}	(CK _S — SQ _H)		4.5			42	ļ	53	
	 	1	6.0			36		45	
	High-level and low-level output		2.0	· ·		175		221	l
t _{PHL}	propagation time		4.5			35		44	ns
	(R - SQ _H)		6.0			30		37	-
			2.0		Ì	175		221	
t _{PLH}		•	4.5			35		44	
	<u> </u>		6.0			30		37	ns
		`	2.0			175		221	"
t _{PHL}	Low-level to high-level and		4.5		1	35		44	
	high-level to low-level		6.0			30		37	
	output propagation time		2.0			225	1	284	1
t _{PLH}	(CK _L - Q _A ~Q _H)		4.5	l	-	45		57	1
		C _L = 150pF (Note 4)	6.0			38		48	
		C _L = 150pr (Note 4)	2.0			225		284	ns
t _{PHL}			4.5	l		45		57	1
			6.0			38		48	
			2.0			150		189	
t _{PLZ}			4.5			30		38	
	Output disable time from	1	6.0			26	l	32	
	low-level and high-level	$C_L = 50 pF \text{ (Note 4)}$	2.0			150	-	189	ns
t _{PHZ}	(OE − Q _A ~Q _H)		4.5			30		38	
-602			6.0	1		26]	32	1

8-BIT SERIAL-INPUT/SERIAL-OR PARALLEL-OUTPUT SHIFT REGISTER WITH LATCHED 3-STATE OUTPUTS

SWITCHING CHARACTERISTICS ($V_{cc} = 2\sim6V$, $T_a = -40\sim+85^{\circ}C$)

						Limits			
Symbol	Parameter	Test conditions		25℃			-40~+85°C		Unit
	· · · · · · · · · · · · · · · · · · ·		V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0			150		189	
t _{PZL}	Output enable time to		4.5		-	30		38	
		0 = 50=5 (N=4= 4)	6.0			26		32	
	low-level and high-level	$C_L = 50 pF \text{ (Note 4)}$	2.0			150		189	ns
t_{PZH} $(\overline{OE} - Q_A \sim Q_H)$		4.5			30		38		
			6.0			26		32	
			2.0			200		252	
t _{PZL}	Output enable time to	,	4.5			40		50	
		C _i = 150pF (Note 4)	6.0			34		43	
	low-level and high-level	C _L = 150pF (Note 4)	2. 0			200		252	ns
t _{PZH}	$(\overline{OE} - Q_A \sim Q_H)$		4.5			40		50	
			6.0			34		43	
Cı	Input capacitance					10		10	рF
Co	Off-state output capacitance (QA~QH)					15		15	pF
C _{PD}	Power dissipation capacitance (Note 3)				287				pF

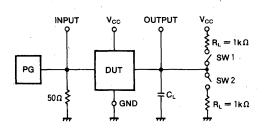
Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot v_{CC}^2 \cdot f_i + I_{CC} \cdot v_{CC}$

TIMING REQUIREMENTS ($v_{cc} = 2\sim6v$, $T_a = -40\sim+85^{\circ}C$)

						Limits			
Symbol	Parameter	Test conditions		25℃		-4		-40~+85°C	
			V _{cc} (V)	Min	Тур	Max	Min	Max	
-			2.0	80			101		
tw(CKS)	Clock pulse width		4.5	16	İ		20		ns
			6.0	14			17		
			2.0	80			101		
tw(CKL)	Clock pulse width		4. 5	16			20		ns
	, [•	6.0	14			17		
			2.0	80			101		
tw(B)	Reset pulse width		4. 5	16			20		ns
			6.0	14			17		
			2.0	100			126		
tsu	A setup time with		4. 5	20			25		ns
	respect to CK _S		6.0	17			21		
	OV		2.0	100			126		
tsu	CK _s setup time with		4.5	20			25		ns
	respect to CK _L		6.0	17			21	ĺ	
			2, 0	5			5		
th	A hold time with		4.5	5			5		ns
	respect to CK _S		6.0	5	1	i	5		
			2.0	50			63		
trec	R recovery time with		4.5	10		1	13		ns
	respect to CK _S		6.0	9			11		

8-BIT SERIAL-INPUT/SERIAL-OR PARALLEL-OUTPUT SHIFT REGISTER WITH LATCHED 3-STATE OUTPUTS

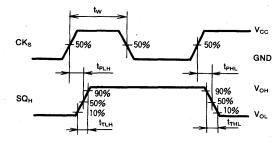
Note 4: Test Circuit

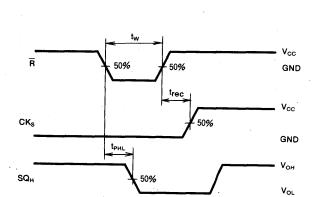


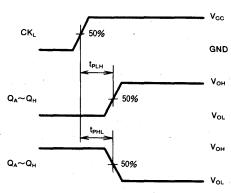
Parameter	SW 1	SW 2
t _{TLH} , t _{THL}	Open	Open
t _{PLZ}	Closed	Open
t _{PHZ}	Open	Closed
t _{PZL}	Closed	Open
t _{PZH}	Open	Closed

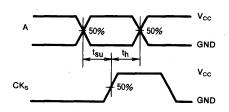
- (1) The pulse generator (PG) has the following characteristics (10% \sim 90%): $\rm t_r=6ns, \, t_f=6ns$
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

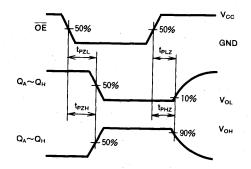
TIMING DIAGRAM

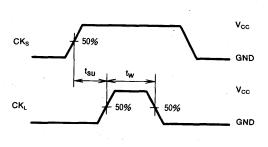












PRELIMINARY PRELIMINARY Notice: This is not a final specification. Some Notice: This is not a final specific to change. 8-B

MITSUBISHI HIGH SPEED CMOS M74HC597P/FP/DP

8-BIT SERIAL-OR PARALLEL
-INPUT/SERIAL-OUTPUT SHIFT REGISTER WITH INPUT LATCH

DESCRIPTION

The M74HC597 is a semiconductor integrated circuit consisting of an 8-bit serial-input/parallel-input with latch, serial-output shift register.

FEATURES

- · Serial-input/parallel-input with latch, serial output
- High-speed: 30MHz clock frequency typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85°C

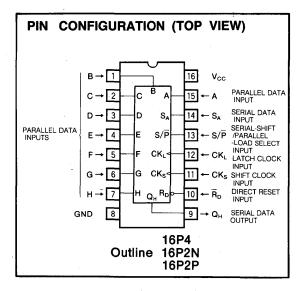
APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC597 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS597.

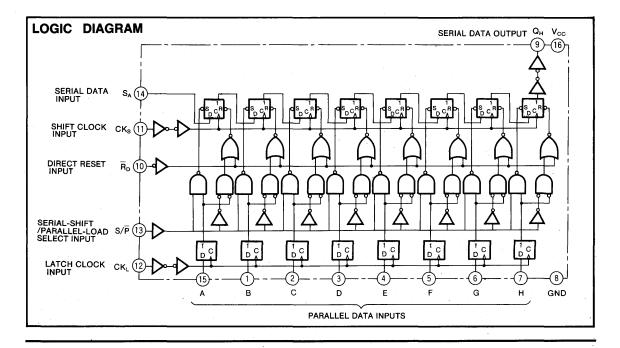
The mode select input S/\overline{P} is used to select either serial or parallel input. When S/\overline{P} is high and serial data input S_A is applied, the data in the 8-bit flip flops will be shifted serially in sync with the clock pulse CK_S . When the latch clock pulse CK_L is applied, parallel data applied at $A\sim H$ will be



stored in the input latch without affecting the contents of the shift register.

Next, S/\overline{P} is low and the parallel data latched at $A\sim H$ will be loaded in sync with the next clock pulse input at CK_L . Serial data transfer is suppressed while parallel data is loaded. Shift or load operations are performed at the rising edge when CK_L changes from low-level to high-level.

When direct reset input $\overline{R_D}$ is low, the shift register will be reset and serial data output Q_H will become low, irrespective of other inputs.



FUNCTION TABLE (Note 1)

		Inp	uts			Output	
R	S/P	CKL	CKs	SA	A~H	Q _H	
L	X	Х	, X	×	X	L	Shift register is reset. Input latch is not affected.
н	н	t	x	×	a-h	no change	Parallel data is stored in the input latch. Shift register is not affected.
Н	L	t	×	×	a-h	h	Parallel data is stored in the input latch and loaded to the shift register.
н	L	×	×	x	×	hL	Parallel data stored in the input latch is loaded in the shift register.
Н	Н	х	1	L	×	Q _{an}	Low-level data is serially shifted into the shift register.
H	• Н	Х	1	Н	X	Qan	High-level data is serially shifted into the shift register.
Н	Н	t	Χ.	L, H	a-h	Q _{an}	Serial data is shifted into the shift register and parallel data is
Н	Н	х	1	L, H	a-h	Q _{gn}	stored in the input latch.

Note 1: † : Change from low to high level

X : Irrelevant

a~h indicate logic level of inputs A~H.

h_L indicates logic level stored in the input latch H.

Q_{GR} indicates logic level of data in the shift register G before shift clock changed.

ABSOLUTE MAXIMUM RATINGS ($\tau_a = -40 \sim +85 ^{\circ}$ C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
		V ₁ < 0V	-20	
lik	Input protection diode current	V _i > V _{CC}	20	mA
	Outros a secretal edited a surrent	V _o < 0V	-20	
Іок	Output parasitic diode current	Vo > Vcc	20	mA
lo	Output current per output pin		±25	mA
loc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature		−65~+150	ე ზ

Note 2 : M74HC597FP, $T_a=-40\sim+70^\circ$ C and $T_a=70\sim85^\circ$ C are derated at -6mW/°C. M74HC597DP, $T_a=-40\sim+50^\circ$ C and $T_a=50\sim85^\circ$ C are derated at -5mW/°C.

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85 \degree c)$

Complete at	D		Limits					
Symbol	Pai	rameter	Min	Тур	Max	Unit		
Vcc	Supply voltage		2		6	٧		
V ₁	Input voltage		0		Vcc	٧		
Vo	Output voltage		0		Vcc	٧		
Topr	Ambient operating temper	rature	-40		+85	Ç		
		$V_{CC} = 2.0V$	0		1000			
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns		
	· '	0		400				

MT4HC597P/FP/DP

8-BIT SERIAL-OR PARALLEL -INPUT/SERIAL-OUTPUT SHIFT REGISTER WITH INPUT LATCH

ELECTRICAL CHARACTERISTICS

	Í				Limits					
Symbol	Parameter	Test	Test conditions V _{CC} (V)		25℃			-40~+85℃		Unit
	2.3				Min	Тур	Max	Min	Max	
		V _O = 0.1V, V _O	_0.11/	2.0	1.5			1.5		
ViH	High-level input voltage	, ,	$ I_0 = 20\mu A$		3.15			3.`15		V
		1101 - 20µA			4.2			4.2		
		$V_0 = 0.1V, V_{C}$	-0.1V	2.0			0.5		0.5	
VIL	Low-level input voltage	$ I_0 = 20\mu A$	5—0. T V	4.5			1. 35		1.35	٧
	1101 20μΑ	$ 1_0 = 20\mu A$				1.8		1.8		
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
		$V_i = V_{iH}, \ V_{iL}$	$I_{OH} = -20\mu A$	4.5	4.4			4.4		
VoH	High-level output voltnge		$I_{OH} = -20\mu A$	6.0	5.9			5.9		V
			$I_{OH} = -4.0 \text{mA}$	4. 5	4.18			4. 13		
			$I_{OH} = -5.2 \text{mA}$	6.0	5.68			5.63		
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
			$I_{OL} = 20 \mu A$	4.5			0.1		0.1	,
VoL	low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
			I _{OL} = 4.0mA	4.5			0. 26		0.33	
	İ		I _{OL} = 5. 2mA	6.0			0. 26		0.33	
l _{iH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μΑ
l ₁ _	Low-level input current	$V_i = 0V$		6.0			—0. 1		-1.0	μΑ
loc	Quiescent supply current	VI = VCC, GNE	$I_0 = 0 \mu A$	6.0			4.0		40.0	μА

SWITCHING CHARACTERISTICS $(V_{cc} = 5V, T_a = 25\%)$

Symbol	Parameter	To at a smallations		Limits		
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
fmax	Maximum clock frequency		30			MHz
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time	,			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level				35	ns
t _{PHL}	output propagation time (CK _L - Q _H)				35	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = 15pF (Note 4)			30	ns
t _{PHL}	output propagation time (CK _S - Q _H)				30	ns
	Low-level to high-level and high-level to low-level				30	T
t _{PHL}	output propagation time $(\overline{R}_D - Q_H)$				30	ns
t _{PLH}	Low-level to high-level and high-level to low-level				30	ns
t _{PHL}	output propagation time (S/P - Q _H)				30	ns

SWITCHING CHARACTERISTICS $(V_{cc} = 2\sim6V, T_a = -40\sim+85^{\circ}C)$

						Limits			
Symbol	Parameter	Test conditions			25℃		−40 ~	+85°C	Unit
	and the second		V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0	5			4		
fmax	Maximum clock frequency		4. 5	27		1	21		MHz
			6.0	32			25		
		· ·	2.0			75		95	
t _{TLH}	Low-level to high-level and		4.5	1.0	ļ	15		19	ns
			6.0			13		16	
	high-level to low-level	·	2.0			75		95	
t _{THL}	output transition time		4.5			15		. 19	ns
			6.0			13		16	
			2, 0			210		265	
teLH	Low-level to high-level and		4.5		,	42		53	ns
	high-level to low-level		6.0		İ	36		45	
	output propagation time		2.0			210		265	
t _{PHL}	(CK _L - Q _H)		4.5			42	1	53	กร
		0 - 50-5 (N-4-4)	6.0			36	1	45	
		C _L = 50pF (Note 4)	2.0			175		221	
t _{PLH}	Low-level to high-level and		4.5			35		44	ns
	high-level to low-level		6.0			30		37	
	output propagation time	_	2.0			175		221	
t _{PHL}	(CK _S - Q _H)		4.5			35		44	ns
		· .	6.0			30		37	
	High-level to low-level	7	2.0			175		221	
t _{PHL}	output propagation time	ì	4.5			35		44	ns
•	$(\overline{R}_D - Q_H)$		6.0			30		37	
			2.0			175		221	
t _{PLH}	Low-level to high-level and		4.5			35		44	ns
	high-level to low-level	,	6.0			30		37	
	output propagation time		2.0			175		221	
t _{PHL}	$(S/\overline{P} - Q_H)$		4.5			35		44	ns
	1		6.0			30	-	37	
Cı	Input capacitance					10		10	pF
C _{PD}	Power dissipation capacitance (Note 3)								pF

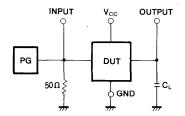
Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$



TIMING REQUIREMENTS ($v_{cc} = 2\sim6v$, $\tau_a = -40\sim+85^{\circ}C$)

		•				Limits]
Symbol	Parameter	Test conditions			25℃		-40~	+85℃	Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	
	Pulse width		2.0	80			101		
tw	(CK _S , CK _L , S/P, RD)		4.5	16			20		ns
	(CRS, CRL, S/P, RD)		6.0	14	İ		17		
	A~H setup time with		2.0	100			126		
tsu(CKL)	respect to CK		4.5	20	1	l	25		ns
	respect to CKL		6.0	17			21		
	C		2.0	100			126		
tsu(CKS)	S _A setup time with		4.5	20			25	1	ns
	respect to CK _S		6.0	17			21		
	0/5		2.0	100			126		
t _{su(cks)}	S/P setup time with	·	4.5	20			25		ns
	respect to CK _S		6.0	17			21	İ	[
	A III hadalara udah		2.0	25			32		
th(CKL)	A∼H hold time with		4.5	5			6		ns
_	respect to CKL		6.0	4			5		
			2.0	5			5		
th(CKS)	S _A hold time with	•	4.5	5			5	İ	ns
•	respect to CK _S		6.0	5			5		
	C/D hald be a with		2.0						
th(cks)	S/P hold time with		4.5		1				ns
•	respect to CK _S		6.0						
	<u></u>		2.0	100			126		
$t_{rec(\overline{R}_D)}$	R _D recovery time with		4.5	20			25		ns
	respect to CKs		6.0	17].		21	1	

Note 4: Test Circuit



- (1) The pulse generator (PG) has the following characteristics $(10\% \sim 90\%)$: $t_r = 6$ ns, $t_f = 6$ ns (2) The capacitance C_L includes stray wiring
- capacitance and the probe input capacitance.

TIMING DIAGRAM 1/f_{max} tw v_{cc} 50% CKL 50% CKs 50% 50% - 50% GND GND t_{PLH} 90% ۷он 90% 50% 50% 50% 10% V_{OL} Q_{H} 50% 10% tw V_{CC} $\overline{\textbf{R}}_{\textbf{D}}$ 50% 50% S/P 50% GND GND V_{OH} V_{OH} Q_{H} 50% 50% 50% Q_H VoL ■ V_{cc} СKs 50% GND v_{cc} V_{CC} 50% 50% SA - 50% 50% - GND GND tsu th th v_{cc} v_{cc} CKs 50% 50% CKL - GND • GND V_{CC} 50% SP • GND tsu th V_{cc} CKs GND

M74HC640P/FP/DWP

OCTAL 3-STATE INVERTING BUS TRANSCEIVER

DESCRIPTION

The M74HC640 is a semiconductor integrated circuit consisting of eight transceivers with inverted outputs.

FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 13 ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC640 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS640.

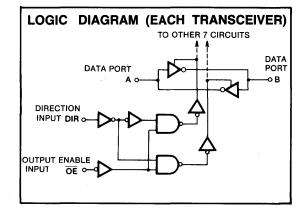
Two buffers with 3-state inverted outputs have their inputs and outputs mutually connected and can be used as buffers in both directions.

The input/output direction is controlled by direction input DIR.

When DIR is high, the data ports A will become input terminals and the data ports B will become output terminals. When DIR is low, B will become input terminals and A will become output terminals.

When output enable input \overline{OE} is high, A and B will both become a high-impedance state and they will be separated.

PIN CONFIGURATION (TOP VIEW) DIRECTION INPUT OE OUTPUT ENABLE 16 + B3 DATA PORTS → R4 DATA PORTS 14 → B5 A8 + GND 20P4 Outline 20P2N 20P2V



FUNCTION TABLE (Note 1)

Inp	outs	Outputs			
ŌĒ	DIR	Α	В		
L	L	ō	- 1		
L	Н	1	ō		
Н	х	Z	Z		

Note 1: I : Input terminal

O : Output terminal (inverted output)

Z : High impedance (A and B are separated)

X : Irrelevant

ABSOLUTE MAXIMUM RATINGS ($\tau_a = -40 \sim +85^{\circ}$ C, unless otherwise noted)

Symbol	Parameter		Conditions	Ratings	Unit
Vcc	Supply voltage			−0.5∼+7.0	V
Vı	Input voltage		,	-0.5~V _{cc} +0.5	٧
Vo	Output voltage			-0.5~V _{cc} +0.5	٧
	lanut avetaction diada averant	V ₁ < 0V		-20	4
lik	Input protection diode current	$v_i > v_{cc}$		20	mA .
	Outrastitte died - coment	V ₀ < 0V		-20	
юк	Output parasitic diode current	$v_o > v_{cc}$		20	mA
lo	Output current per output pin			±35	mA
Icc	Supply/GND current	V _{CC} , GND		±75	mA.
Pd	Power dissipation	(Note 2)		500	mW
Tstg.	Storage temperature range			-65~+150	°C

Note 2 : M74HC640FP, $T_a=-40\sim+75^\circ$ C and $T_a=75\sim85^\circ$ C are derated at -7mW/°C. M74HC640DWP, $T_a=-40\sim+80^\circ$ C and $T_a=80\sim85^\circ$ C are derated at -7mW/°C.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85^{\circ}C)$

	Parameter			Unit		
Symbol	Pa	rameter	Min	Тур	Max	Unit
Vcc	Supply voltage				6	٧
V _I .	Input voltage		. 0		Vcc	V
Vo	Output voitage		0		Vcc	~ V
Topr	Operating temperature ra	ange	-40		+85	င
		$V_{CC} = 2.0V$	0		1000	
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns
		$V_{CC} = 6.0V$	0		400	

ELECTRICAL CHARACTERISTICS

							Limits			
Symbol	Parameter	Test	conditions	_	25℃			-40~+85°C		Unit
				V _{cc} (V)	Min	Тур	Max	Min	Max	
		$V_0 = 0.1V, V_{cc}$	_0.11/	2.0	1.5			1.5		
V _{IH}	High-level input voltage	$ I_0 = 20\mu A$	50. I V	4.5	3. 15		•	3. 15		٧
	<u> </u>	1101 — 20µA	*	6.0	4.2			4. 2	-	
	1	V. = 0.1V. V	o = 0.1V, V _{cc} -0.1V		,		0.5		0.5	
V_{IL}	Low-level input voltage	$ V_0 = 0.1V, V_{CO}$ $ I_0 = 20\mu A$					1.35	·	1.35	٧
	<u> </u>	11 ₀ 1 = 20µA		6.0			1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
			$I_{OH} = -20\mu A$	4.5	4.4			4. 4	·	
V _{OH} High-level output voltage	High-level output voltage	$V_i = V_{iH}, \ V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		· V
			$I_{OH} = -6.0 \text{mA}$	4.5	4.18			4.13		
			$I_{OH} = -7.8 \text{mA}$	6.0	5. 68	_	-	5.63		
			$I_{OL} = 20 \mu A$	2, 0			0.1		0.1	
			$I_{OL} = 20 \mu A$	4.5			0.1		0.1	
VoL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0		}	0.1		0. 1	V
			$I_{OL} = 6.0 \text{mA}$	4. 5			0. 26		0.33	
	·		I _{OL} = 7.8mA	6.0			0. 26		0.33	-
l _{iH}	High-level input current	V _I = 6V		6.0			0.1		1.0	μΑ
I _{IL}	Low-level input current	$V_i = 0V$		6.0			-0.1		-1.0	μΑ
lozh	Off-state high-level output current	$V_i = V_{iH}, \ V_{iL}, \ V_{iL}$	$V_0 = V_{CC}$	6.0			0.5		5.0	μΑ
lozL	Off-state low-level output current	$V_{l} = V_{lH}, \ V_{lL}, \ V_{lL}$	√o = GND	6.0			-0.5		-5.0	μΑ
Icc	Quiescent supply current	VI = VCC, GND	$I_0 = 0\mu A$	6.0			4.0		40.0	μΑ

SWITCHING CHARACTERISTICS ($v_{cc} = 5v$, $t_a = 25^{\circ}C$)

Symbol	Parameter	Test conditions		Unit		
Symbol	Farameter	rest conditions	Min	Тур	Max	Unit
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time	$C_L = 50 pF (Note 4)$			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level				21	ns
t _{PHL}	output propagation time (A - B, B - A)				21	ns
t _{PLZ}	Output disable time from low-level and high-level	C = E = E (Niet = 4)			42	ns
t _{PHZ}	(OE - A, B)	$C_L = 5 pF (Note 4)$			42	ns
t _{PZL}	Output enable time to low-level and high-level	0 - 50-5 (N-4-4)			42	ns
t _{PZH}	(OE - A, B)	C _L = 50pF (Note 4)			42	ns

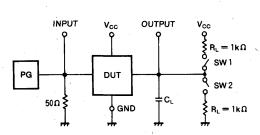
SWITCHING CHARACTERISTICS ($v_{cc} = 2\sim6$ V, $T_a = -40\sim+85$ °C)

	•					Limits			
Symbol	Parameter	Test conditions			25℃		-40~	+85℃	Unit
			V _{CC} (V)	Min	Тур	Max	Min	Max	
			2.0			60		75	
t _{TLH}	Low-level to high-level and		4.5		Ì	12		15	ns
	high-level to low-level	C _L = 50pF (Note 4)	6.0			10		13	
	migh-level to low-level	OL - Sopi (Note 4)	2.0			∞ 60		75	
t _{THL}	output transition time	·	4.5			12		15	ns
			6.0			10		13	
	,		2.0			110		140	
t _{PLH}	,		4.5			22		28	ns
		$C_L = 50 pF \text{ (Note 4)}$	6.0			19		24	
		CL = 30pr (Note 4)	2.0			110		140	
t _{PHL}	Low-level to high-level and		4.5			22		28	ns
	high-level to low-level		6.0			19		24	
	output propagation time		2.0			195		245	
t _{PLH}	(A - B, B - A)		4.5			39	1.	49	ns
		C _L = 150pF (Note 4)	6.0			34		- 43	İ
		$C_L = (50pr (Note 4))$	2.0			195		245	
t _{PHL}	·		4.5			39		49	ns
			6.0			34		43	
			2.0			172		208	
t _{PLZ}	Output disable time from	<u> </u>	4.5			43		52	ns
	1	50 = (11 + 4)	6.0			41		50	
	low-level and high-level	C _L = 50pF (Note 4)	2.0			172		208	
t _{PHZ}	(OE - A, B)	-	4.5			43		52	ns
			6.0			41		50	
			2.0		-	184		224	
t _{PZL}			4.5			46		56	ns
	·		6.0			41		50	
	1	C _L = 50pF (Note 4)	2.0			184		224	
t _{PZH}	Output enable time to low-level		4.5			46		56	ns
			6.0		1	41] .	50	
	and high-level		2.0			216		260	
t _{PZL}	(OE - A, B)		4.5			54		65	ns
			6.0			47		57	
	1	C _L = 150pF (Note 4)	2.0			216		260	
t _{PZH}			4.5		1	54		65	ns
			6.0			47		57	
Cı	Input capacitance					10		10	pF
Co	Off-state output capacitance	OE = V _{CC}	-			15		15	pF
C _{PD}	Power dissipation capacitance (Note 3)				53	1.2		l	pF

Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per transceiver) The power dissipation during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$



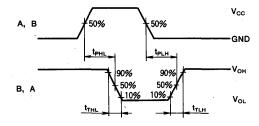
Note 4: Test Circuit

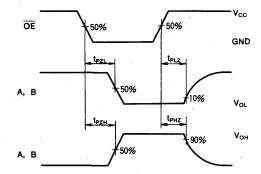


Parameter	SW 1	SW 2
t _{TLH} , t _{THL}	Open	Open
t _{PLZ}	Closed	Open
t _{PHZ}	Open	Closed
t _{PZL}	Closed	Open
t _{PZH}	Open	Closed

- (1) The pulse generator (PG) has the following characteristics (10% \sim 90%): t_r = 6ns, t_t = 6ns (2) The capacitance C_L includes stray wiring
- capacitance and the probe input capacitance.

TIMING DIAGRAM







MITSUBISHI HIGH SPEED CMOS

M74HC640-1P/FP/DWP

OCTAL 3-STATE INVERTING BUS TRANSCEIVER

DESCRIPTION

The M74HC640-1 is a semiconductor integrated circuit consisting of eight bus transceivers with inverted outputs.

FEATURES

- High-fanout 3-state output: (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed: 8 ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 25µW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 60 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC640-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS640.

The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

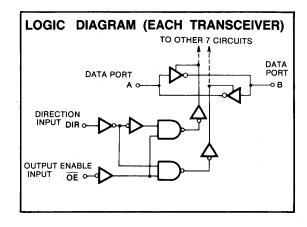
Two buffers with 3-state inverted outputs have their inputs and outputs mutually connected and can be used as buffers in both directions.

The input/output direction is controlled by direction input DIR.

When DIR is high, the data ports A will become input terminals and the data ports B will become output terminals. When DIR is low, B will become input terminals and A will become output terminals.

When output enable input \overline{OE} is high, A and B will both become a high-impedance state and they will be separated.

CONFIGURATION (TOP VIEW) DIRECTION V_{CC} OE OUTPUT ENABLE 19 18 + B1 16 **↔** B3 DATA PORTS 15 **↔** B4 DATA PORTS 14 + B5 13 **↔** B6 A7 ↔ 8 Α8 12 + B7 GND 20P4 Outline 20P2N 20P2V



FUNCTION TABLE (Note 1)

Inp	Inputs		ports
ŌĒ	DIR	Α	В
L	L	ō	1
L	н	1	ō
н	Х	z	Z

Note 1: I : Input terminal

O: Output terminal (inverted output)

Z : High impedance (A and B are separated)

X : Irrelevant

ABSOLUTE MAXIMUM RATINGS $(T_a = -40 \sim +85 \degree)$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	v
Vo	Output voltage		-0.5~V _{cc} +0.5	V
		V ₁ < 0V	-20	
lik	Input protection diode current	V ₁ > V _{CC}	20	mA
		V ₀ < 0V	-20	
lok	Output parasitic diode current	V _o > V _{cc}	20	mA
lo	Output current, per output pin	·	±50	mA
Icc	Supply/GND current	V _{CC} , GND	±200	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65~+150	ာ

Note 2 : M74HC640-1FP, T $_a=-40\sim+75$ °C and T $_a=75\sim85$ °C are derated at -7mW/°C. M74HC640-1DWP, T $_a=-40\sim+80$ °C and T $_a=80\sim85$ °C are derated at -7mW/°C.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85 \degree C)$

Cumbal	Parameter			Limits				
Symbol	Pa	Min	Тур	Max	Unit			
V _{CC}	Supply voltage		2		6	V		
Vı	Input voltage		0		Vcc	V		
Vo	Output voltage		0		Vcc	V		
Topr	Operating temperature ra	ange	-40		+85	င		
		$V_{CC} = 2.0V$	0		500			
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		50	ns/V		
	$V_{\rm CC} = 6.0 \text{V}$		0	-	30	1		

ELECTRICAL CHARACTERISTICS

							Limits			
Symbol	Parameter	Test	conditions		25℃			-40~+85°C		Unit
			V _{CC} (V) Min Typ Max Min Max		Max					
		V = 0 1V V	0.114	2.0	1.5	, , , , ,	-	1.5		-
V _{IH}	High-level input voltage		$_{0} = 0.1 \text{V}, \text{ V}_{CC} = 0.1 \text{V}$		3.15			3. 15		v
		$ I_0 = 20\mu A$		6.0	4.2			4.2		
		V 0 1V V	$V_0 = 0.1V, V_{CC} - 0.1V$				0.5		0.5	
VIL	Low-level input voltage	-					1.35	l	1.35	V
	$ I_0 = 20\mu A$		6.0			1.8		1.8		
	High-level output voltage $V_i = V_{iH}, \ \ V_i$		$I_{OH} = -20\mu A$	2.0	1.9			1.9		
v		$V_I = V_{IH}, \ V_{IL}$	$I_{OH} = -20\mu A$	4.5	4.4			4.4		v
V _{OH}			$I_{OH} = -20\mu A$	6.0	5.9			5.9		
	·	1	$I_{OH} = -24mA$	4.5	3. 98			3.84		Ì
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
v	Law tayat autaut water	$V_{I} = V_{IH}, V_{IL}$	$I_{OL} = 20 \mu A$	4.5	ļ		0.1	ļ	0.1	v
Vol	Low-level output voltage	VI - VIH, VIL	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	'
			I _{OL} = 24mA	4. 5			0.39		0.5	
i _{IH}	High-level input current	$V_1 = 6V$		6.0			0.1		1.0	μA
l _{IL}	Low-level input current	$V_i = 0V$		6.0			—0. 1		-1.0	μA
lozh	Off-state high-level output current	$V_i = V_{iH}, \ V_{iL}, \ V_{iL}$	$V_i = V_{iH}, \ V_{iL}, \ V_O = V_{CC}$				0.5		5.0	μA
lozL	Off-state low-level output current	$V_i = V_{iH}, \ V_{iL}, \ V_{iL}$	/o = GND	6. 0			-0.5		-5.0	μA
loc	Quiescent supply current	VI = VCC, GND	$I_0 = 0\mu A$	6.0			5.0		50.0	μА

SWITCHING CHARACTERISTICS $(v_{cc} = 5v, T_a = 25^{\circ}C)$

Symbol	Parameter	Test conditions		Unit		
Symbol	Parameter	rest conditions	Min	Тур	Max	Unit
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time	C _L = 50pF (Note 4)			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level				15	ns
t _{PHL}	output propagation time (A - B, B - A)				15	ns
t _{PLZ}	Output disable time from low-level and high-level	C _L = 5 pF (Note 4)			25	ns
t _{PHZ}	(OE - A, B)	CL = 5 pr (Note 4)			25	ns
t _{PZL}	Output enable time to low-level and high-level	C ₁ = 50pF (Note 4)			28	ns
t _{PZH}	(OE - A, B)	OL — SOPE (NOTE 4)			28	ns

SWITCHING CHARACTERISTICS $(v_{cc} = 2\sim 6V, T_a = -40\sim +85\%)$

						Limits		٠.	
Symbol	Parameter	Test conditions			25℃		−40 ~	+85°C	Unit
	· ·		V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0			60		75	
t _{TLH}	Low-level to high-level and		4.5			12		15	
	high-level to low-level		6.0			10		13	ns
	riigii-level to low-level		2.0			60		75	115
t _{THL}	output transition time		4.5			12		15	
			6.0			10		13	
			2.0			85		105	
t _{PLH}	Low-level to high-level and	·	4.5			17		21	
	high-level to low-level		6.0			14		18	
	output propagation time		2.0			85		105	ns
t _{PHL}	(A - B, B - A)		4.5			17		21	
		C _L = 50pF (Note 4)	6.0			14		18	
		CL — Supr (Note 4)	2.0			150		190	
t_{PLZ}	Output disable time from		4.5			30		38	
	low-level and high-level		6.0			26		33	ns
	low-lever and high-lever	•	2.0			150		190	115
t _{PHZ}	(OE – A, B)		4.5			. 30		38	
		•	6.0			26		33	
			2.0			150		190	
t _{PZL}	Output enable time to		4.5			30 -		- 38	
	low-level and high-level		6.0			26		33	ns
	low-lever and mign-lever		2.0			150		190	115
t_{PZH}	(OE - A, B)		4.5			30		38	
			6.0			26		33	
C _I	Input capacitance					- 10		10	
Co	Off-state output capacitance	OE = V _{CC}				15		15	рF
CPD	Power dissipation capacitance (Note 3)								

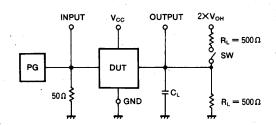
Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per transceiver)

The power dissipation during operation under no-load conditions is calculated using the following formula:

P_D = C_{PD} • V_{CC}² • f₁+I_{CC} • V_{CC}



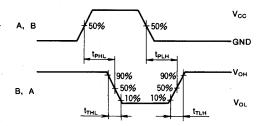
Note 4: Test Circuit

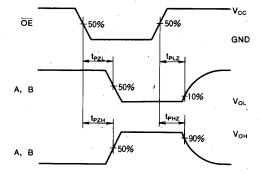


Parameter	sw
t _{TLH} , t _{THL} t _{PLH} , t _{PHL}	Open
t _{PLZ}	Closed
t _{PHZ}	Open
t _{PZL}	Closed
t _{PZH}	Open

- (1) The pulse generator (PG) has the following characteristics (10% \sim 90%): $t_{\rm f}=3$ ns, $t_{\rm f}=3$ ns
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





M74HCT640-1P/FP/DWP

OCTAL 3-STATE
INVERTING BUS TRANSCEIVER WITH LSTTL-COMPATIBLE INPUTS

DESCRIPTION

The M74HCT640-1 is a semiconductor integrated circuit consisting of eight transceivers with inverted outputs.

FEATURES

- TTL level inputs V_{IL}=0.8V max, V_{IH}=2.0V min
- High-fanout 3-state output: (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed: 10 ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 25μW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- Capable of driving 60 74LSTTL loads
- Wide operating temperature range: Ta=-40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HCT640-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS640.

The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

As the inputs are TTL level, the device can be used as a level converter from LSTTL to high-speed CMOS. In that case, no pull-up resistors are required.

Two buffers with 3-state inverted outputs have their inputs and outputs mutually connected and can be used as buffers in both directions

The input/output direction is controlled by direction input DIR.

When DIR is high, the data ports A will become input terminals and the data ports B will become output terminals. When DIR is low, B will become input terminals and A will become output terminals.

When output enable input \overline{OE} is high, A and B will both become a high-impedance state and they will be separated.

come a high-impedance state and the

FUNCTION TABLE (Note 1)

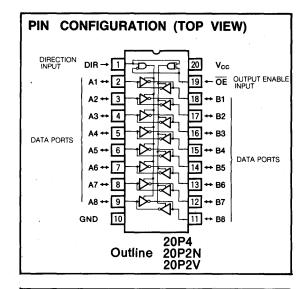
Inputs		Out	puts
OE	DIR	Α	В
٦	L	ō	1 .
Ł	н	1	O
H	х	Z	Z

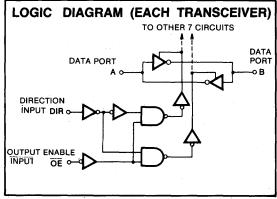
Note 1 : I : Input terminal

O : Output terminal (inverted output)

Z : High impedance (A and B are separated)

X : Irrelevant





MITSUBISHI HIGH SPEED CMOS M74HCT640-1P/FP/DWP

OCTAL 3-STATE INVERTING BUS TRANSCEIVER WITH LSTTL-COMPATIBLE INPUTS

ABSOLUTE MAXIMUM RATINGS ($\tau_a = -40 \sim +85 ^{\circ}$ C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
	Input protection diode current	V ₁ < 0V	-20	
ΊΚ		V _I > V _{CC}	20	mA
	O danak manadaha diada anyarah	V ₀ < 0V	-20	
ок	Output parasitic diode current	Vo > Vcc	20	mA
lo	Output current per output pin		±50	mA
Icc	Supply/GND current	V _{CC} , GND	±200	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		-65~+150	ဗ

Note 2 : M74HCT640-1FP, $T_a = -40 \sim +75^{\circ}C$ and $T_a = 75 \sim 85^{\circ}C$ are derated at -7mW/°C. M74HCT640-1DWP, $T_a = -40 \sim +80^{\circ}C$ and $T_a = 80 \sim 85^{\circ}C$ are derated at -7mW/°C.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85 ^{\circ}C)$

0	Parameter			Limits				
Symbol			Min	Min Typ		Unit		
V _{CC}	Supply voltage		4.5		5.5	V		
Vı	Input voltage		0		Vcc	٧		
Vo	Output voltage	Output voltage			Voc	V		
Topr	Ambient operating temper	Ambient operating temperature			+85	င		
		V _{CC} = 4.5V	0		25	01		
t _r , t _f	Input risetime, falltime V _{CC} = 5.5V		0		15	ns/V		

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, unless otherwise noted)

					Limits				
Symbol Parameter	Parameter	Test conditions		25°C			-40~+85°C		Unit
		ì		Min	Тур	Max	Min	Max	
V _{IH}	High-level input voltage	$V_0 = 0.1V$, $V_{CC} = 0.1V$ $ I_0 = 20\mu A$		2.0			2.0		>
V _{IL}	Low-level input voltage	$V_0 = 0.1V, V_{CC} - 0.1V$ $ I_0 = 20\mu A$				0.8		0.8	· V
	V _{OH} High-level output voltage $V_I = V_{IL}$	$I_{OH} = -20\mu A$	V _{cc} -0.1			V _{CC} -0.1	7	V	
v он		High-level output voltage $V_i = V_{iL}$	V _I = V _{IL}	$I_{OH} = -24mA$, $V_{CC} = 4.5V$	3.98			3.84	
V	1 1 1 1 1		$I_{OL} = 20\mu A$			0.1		0.1	>
VoL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 24 \text{mA}, \ V_{CC} = 4.5 \text{V}$			0.39	-	0.5	٧
l _{iH}	High-level input current	$V_1 = V_{CC}$				0.1		1.0	
I _{IL}	Low-level input current	V _I = GND				-0.1		-1.0	μΑ
l _{ozh}	Off-state high-level output current	$V_i = V_{iH}, \ V_{iL},$	$V_0 = V_{CC}$			0.5		5.0	
lozL	Off-state low-level output current	$V_{l} = V_{lH}, \ V_{lL}, \ V_{O} = GND$				-0.5		-5.0	μΑ
Icc	Quiescent supply current	VI = VCC, GNE	$0, l_0 = 0\mu A$		1 7 7 7	5.0		50.0	μΑ
△lcc	Maximum quiescent supply current	$V_1 = 2.4V, 0.4$	V (Note 3)			2.7		2.9	mA

Note 3: Only one input is set at this value and all other inputs are fixed at V_{CC} or GND.

MITSUBISHI HIGH SPEED CMOS M74HCT640-1P/FP/DWP

OCTAL 3-STATE INVERTING BUS TRANSCEIVER WITH LSTTL-COMPATIBLE INPUTS

SWITCHING CHARACTERISTICS ($v_{cc} = 5v$, $\tau_a = 25\%$)

Cumbal	Daniel de la constant	Took and distance	Limits			Unit
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time	C _L = 50pF (Note 5)			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level				15	ns
t _{PHL}	output propagation time (A — B, B — A)				15	ns
t _{PLZ}	Output disable time from low-level and high-level	C = 5 = 5 (Note 5)			25	ns
t _{PHZ}	(OE - A, B)	$C_L = 5 \text{ pF (Note 5)}$			25	ns
t _{PZL}	Output enable time to low-level and high-level	C _L = 50pF (Note 5)			28	ns
t _{PZH}	(OE - A, B)				28	ns

SWITCHING CHARACTERISTICS $(V_{cc} = 5V \pm 10\%, T_a = -40 \sim +85^{\circ}C)$

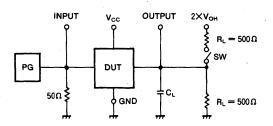
	1		Limits					
Symbol	Parameter -	Test conditions	25℃			-40~+85°C		Unit
			Min	Тур	Max	Min	Max	
t _{TLH}	Low-level to high-level and				12		15	
t _{THL}	high-level to low-level output transition time	C _L = 50pF (Note 5)			12		15	ns
t _{PLH}	Low-level to high-level and high-level to low-level				17		21	ns
t _{PHL}	output propagation time (A — B, B — A)				17		21	lis
t _{PLZ}	Output disable time from				30	_	. 38	
	low-level and high-level							ns
t _{PHZ}	(OE - A, B)				30		38	
t _{PZL}	Output enable time to				30		38	
	low-level and high-level							ns
t _{PZH}	(OE - A, B)		ĺ.		30		38	
Cı	Input capacitance				10		10	
Co	Off-state output capacitance	OE = V _{CC}			15		15	pF
C _{PD}	Power dissipation capacitance (Note 4)							1

Note 4 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per transceiver) The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot v_{CC}^2 \cdot f_1 + I_{CC} \cdot v_{CC}$



OCTAL 3-STATE INVERTING BUS TRANSCEIVER WITH LSTTL-COMPATIBLE INPUTS

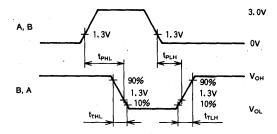
Note 5: Test Circuit

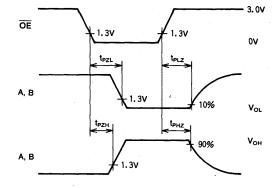


Parameter	SW
t _{TLH} , t _{THL} t _{PLH} , t _{PHL}	Open
t _{PLZ}	Closed
t _{PHZ}	Open
t _{PZL}	Closed
t _{PZH}	Open

- (1) The pulse generator (PG) has the following characteristics (10%~90%): $\rm t_f=3ns,\,t_f=3ns$
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





MITSUBISHI HIGH SPEED CMOS

M74HC643P/FP/DWP

OCTAL 3-STATE INVERTING AND NONINVERTING BUS TRANSCEIVER

DESCRIPTION

The M74HC643 is a semiconductor integrated circuit consisting of eight transceivers with inverted and noninverted outputs.

FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=-6mA)
- High-speed: 13ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max
 (V_{CC}=5V, T_A=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2∼6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC643 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while 'giving high-speed performance equivalent to the 74LS643.

Two buffers with 3-state inverted and noninvertered outputs have their inputs and outputs mutually connected and can be used as buffers in both directions.

The Input/output direction is controlled by direction input DIR.

When DIR is high, the data ports A will become input terminals and the data ports B will become output terminals. When DIR is low, B will become input terminals and A will become output terminals.

When output enable input \overline{OE} is high, A and B will both become a high-impedance state and they will be separated.

FUNCTION TABLE (Note 1)

In	outs	Outputs			
OE	DIR	Α .	В		
L	. L	0	1		
L	Н	1 . 1	ō		
н	×	Z	Z		

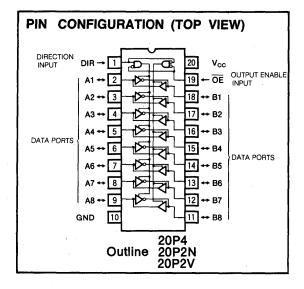
Note 1: I : Input terminal

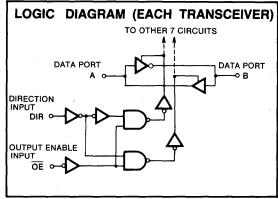
O: Output terminal (noninverted output)

O: Output terminal (inverted output)

Z : High impedance (A and B are separated)

X : irrelevani





ABSOLUTE MAXIMUM RATINGS ($\tau_a = -40 \sim +85$ °C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		−0.5~+7.0	V
V ₁ .	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
I _{IK} Input protection diode current		V ₁ < 0V	-20	
	input protection diode current	V _I > V _{CC}	20	mA
		V ₀ < 0V	-20	
lok	Output parasitic diode current	$v_o > v_{cc}$	20	. mA
lo	Output current per output pin		±35	mA
Icc	Supply/GND current	V _{CC} , GND	±75	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		-65~+150	°C

Note 2 : M74HC643FP, $T_a = -40 \sim +75 ^{\circ} C$ and $T_a = 75 \sim 85 ^{\circ} C$ are derated at $-7 \text{mW/}^{\circ} C$. M74HC643DWP, $T_a = -40 \sim +80 ^{\circ} C$ and $T_a = 80 \sim 85 ^{\circ} C$ are derated at $-7 \text{mW/}^{\circ} C$.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85 \degree C)$

Chambral.	Parameter			Limits				
Symbol			Min	Тур	Max	Unit		
Vcc	Supply voltage		. 2		6	V		
V _i	Input voltage		0		Vcc	٧		
Vo	Output voltage		0		Vcc	٧		
Topr	Operating temperature ra	ange	-40		+85	င		
		$V_{CC} = 2.0V$	0		1000			
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns		
	$V_{CC} = 6.0V$		0		400			

ELECTRICAL CHARACTERISTICS

	-						Limits		·	-
Symbol	Parameter	Parameter Test conditions			25℃			-40~+85°C		Unit
			V _{cc} (V)		Min	Тур	Max	Min	Max	
		$V_0 = 0.1V, V_{CO}$	-0.1V	2.0	1.5			1.5		
V _{IH}	High-level input voltage	$ I_0 = 20\mu A$	5- 0.1 V	4.5	3.15			3. 15		V
		1161 - 20μΑ		6.0	4.2			4.2		
		$V_0 = 0.1V, V_{cc}$	-0.1V	2.0			0.5		0.5	
VIL	Low-level input voltage	$ I_0 = 20\mu A$	5- 0.1 V	4.5			1.35		1.35	V
		1101 — 20µA		6.0			1.8		1.8	1
		-	$I_{OH} = -20\mu A$	2.0	1.9			1.9		
	· .		$I_{OH} = -20\mu A$	4.5	4. 4			4.4		
VoH	High-level output voltage	$V_{l} = V_{lH}, V_{lL}$	$I_{OH} = -20\mu A$	6.0	5.9	1		5.9		· V
		-	$I_{OH} = -6.0 \text{mA}$	4. 5	4.18			4. 13		
		<u> </u>	$I_{OH} = -7.8 \text{mA}$	6.0	5.68			5.63		
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
			$I_{OL} = 20 \mu A$	4.5	ļ		0.1		0.1	
VoL	Low-level output voltage	$V_I = V_{IH}, V_{IL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
			$I_{OL} = 6.0 mA$	4.5	1	1	0.26	1	0.33	1
			I _{OL} = 7.8mA	6.0			0. 26		0.33	
l _{IH}	High-level input current	$V_1 = 6V$		6.0		,	0.1		1.0	μA
l _{IL}	Low-level input current	$V_i = 0V$		6.0			-0.1		-1.0	μA
l _{ozh}	Off-state high-level output current	$V_i = V_{iH}, \ V_{iL}, \ $	$V_0 = V_{CC}$	6.0	ļ		0.5		5.0	μA
lozL	Off-state low-level output current	$V_{i} = V_{iH}, \ V_{iL}, \ $	√o = GND	6.0			-0.5		-5. 0	μA
Icc	Quiescent supply current	VI = VCC, GND	$l_0 = 0\mu A$	6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS $(v_{cc} = 5v, \tau_a = 25^{\circ}C)$

Cumahaal	Parameter	Test conditions		Limits			
Symbol	rarameter	rest conditions	Min	Тур	Max	Unit	
trun	Low-level to high-level and high-level to low-level				10	ns	
tTHL	output transition time	C ₁ = 50pF (Note 4)			10	ns	
t _{PLH}	Low-level to high-level and high-level to low-level	CL — SUPP (Note 4)			21	ns	
t _{PHL}	output propagation time (A - B, B - A)				21	ns	
t _{PLZ}	Output disable time from low-level and high-level	C ₁ = 5 pF (Note 4)			42	ns	
t _{PHZ}	(OE - A, B)	C _L — 5 pr (Note 4)			42	ns	
t _{PZL}	Output enable time to low-level and high-level	C _L = 50pF (Note 4)			42	ns	
t _{PZH}	(OE – A, B)	CL — Supr (Note 4)			42	ns	

SWITCHING CHARACTERISTICS ($V_{cc} = 2\sim 6V$, $T_a = -40\sim +85^{\circ}C$)

,		·				Limits			1
Symbol	Parameter	Test conditions			25℃		−40 ~	+85℃	Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0			60		75	
t⊤∟∺	Low-level to high-level and		4.5			12		15	ns
	high-level to low-level	C _L = 50pF (Note 4)	6.0			10		13	
	Ingli-level to low-level	SE SSPI (Note 1)	2.0			60		75	
t _{THL}	output transition time		4.5		,	12		15	ns
			6.0			10		13	
			2.0			110		140	
t _{PLH}	-		4.5			22		28	ns
		C _t = 50pF (Note 4)	6.0			19		24	
	·	SE SSE (Mais 1)	2.0			110		140	
t _{PHL}	Low-level to high-level and		4.5			22		28	ns
	high-level to low-level		6.0			19		24	
	output propagation time		2.0			195		245	
t _{PLH}	(A - B, B - A)	-	4.5			39		49	ns
		C _L = 150pF (Note 4)	6.0			34		43	
		O[- 130p1 (Note 4)	2.0			195	ĺ	245	
t _{PHL}			4.5			39	İ	49	ns
			6.0			34		43	
			2.0			172		208	
t _{PLZ}	Output disable time from		4.5			43	}	52	ns
	low-level and high-level	C _L = 50pF (Note 4)	6.0	<u> </u>		41		50	
	_	SE SEP. (HOLD I)	2.0			172	1	208	
t _{PHZ}	(OE - A, B)		4.5			43	!	52	ns
			6.0			41		50	
			2.0			184		224	
t _{PZL}	·		4.5			46	ļ .	56	ns.
		C _L = 50pF (Note 4)	6.0			41		50	
			2.0			184		224	
t _{PZH}	Output enable time to low-level		4.5			46		56	ns
	and high-level		6, 0			41		50	
	_		2.0			216		260	
t _{PZL}	(OE - A, B)		4.5			54		65	ns
		C _L = 150pF (Note 4)	6. 0			47	-	57	
			2.0			216		260	
t _{PZH}		1	4.5			54		65	ns
			6.0			47	ļ	57	
C,	Input capacitance					10		10	pF
Со	Off-state output capacitance	OE = V _{CC}				15		15	pF
C _{PD}	Power dissipation capacitance (Note 3)				55		L		pF

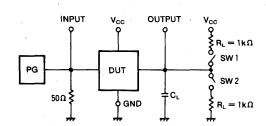
Note 3: CPD is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per transceiver)



The lower dissipation during operation under no-load conditions is calculated using the following formula:

PD CPD • Vcc² • f₁+f₁cc • Vcc

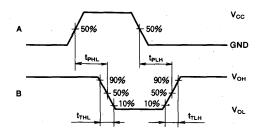
Note 4: Test Circuit

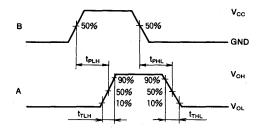


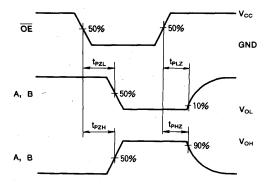
Parameter	SW1	SW 2
t _{TLH} , t _{THL}	Open	Open
t _{PLZ}	Closed	Open
t _{PHZ}	Open	Closed
t _{PZL}	Closed	Open
t _{PZH}	Open	Closed

- (1) The pulse generator (PG) has the following characteristics (10% \sim 90%): $t_r = 6ns$, $t_f = 6ns$
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM









MITSUBISHI HIGH SPEED CMOS

M74HC643-1P/FP/DWP

OCTAL 3-STATE INVERTING AND NONINVERTING BUS TRANSCEIVER

DESCRIPTION

The M74HC643-1 is a semiconductor integrated circuit consisting of eight bus transceivers with inverted and noninverted outputs.

FEATURES

- High-fanout 3-state output: (I_{OL}=24mA, I_{OH}=-24mA)
- High-speed: 8ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 25 µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 60 74LSTTL loads
- Wide operating voltage range: $V_{CC}=2\sim6V$
- Wide operating temperature range: Ta=-40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC643-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS643.

The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

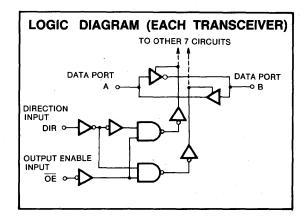
Two buffers with 3-state inverted and noninvertered outputs have their inputs and outputs mutually connected and can be used as buffers in both directions.

The Input/output direction is controlled by direction input

When DIR is high, the data ports A will become input terminals and the data ports B will become output terminals. When DIR is low, B will become input terminals and A will become output terminals.

When output enable input OE is high, A and B will both become a high-impedance state and they will be separated.

PIN CONFIGURATION (TOP VIEW) DIRECTION DIR 20 Vcc INPUT OUTPUT ENABLE 19 OE INPUT 18 **↔** B1 A2 ++ A3 ↔ 4 17 ↔ B2 16 DATA PORTS 15 A5 ↔ 6 **↔** B4 DATA PORTS 14 ↔ B5 A6 ↔ 7 A7 ↔ 8 12 **↔** B7 A8 ++ 9 11 GND 10 **↔** B8 20P4 20P2N Outline 20P2V



FUNCTION TABLE (Note 1)

inp	outs	Data	ports
OE	OE DIR		В
L	L	0	ı
L	н	ı	ō
Н	х	Z	Z

- Note 1: I: Input terminal
 - O: Output terminal (noninverted output)
 - O: Output terminal (inverted output)
 - Z: High impedance (A and B are separated)
 - X : Irrelevant

ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
V _I	Input voltage		-0.5~V _{cc} +0.5	V
V _o	Output voltage		-0.5~V _{cc} +0.5	V
	Insula medicables diada assessa	V ₁ < 0V	-20	T
l _{IK}	Input protection diode current	V _I > V _{CC}	20	mA
	Q. 44	V ₀ < 0V	-20	
lok	Output parasitic diode current	Vo > Vcc	20	mA
l _o	Output current per output pin		±50	mA
Icc	Supply/GND current	V _{CC} , GND	±200	mA.
Pd	Power dissipation	(Note 2)	500	mW.
Tstg	Storage temperature range		-65~+150	င

Note 2 : M74HC643-1FP, T_a = $-40\sim+75^\circ$ C and T_a = $75\sim85^\circ$ C are derated at -7mW/°C. M74HC643-1DWP, T_a = $-40\sim+80^\circ$ C and T_a = $80\sim85^\circ$ C are derated at -7mW/°C.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85^{\circ}C)$

	B			Limits				
Symbol	Pa	Parameter			Max	Unit		
Vcc	Supply voltage		2		6	V		
Vı	Input voltage		0		Vcc	V		
Vo	Output voltage	, , , , , , , , , , , , , , , , , , , ,	0		Vcc	V		
Topr	Operating temperature ra	ange	-40		+85	°C .		
		V _{CC} = 2.0V	0		500			
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		50	ns/V		
		$V_{CC} = 5.5V$	0		30	1		

ELECTRICAL CHARACTERISTICS

							Limits			
Symbol	Parameter	Test	Test conditions		25°C			-40~+85°C		Unit
			V _{cc} (V)		Min	Тур	Max	Min	Max	
		$V_0 = 0.1V, V_{CC}$	0.11/	2.0	1.5			1.5		
ViH	High-level input voltage	$ V_0 = 0.1V, V_{CC} $ $ I_0 = 20\mu A$		4.5	3. 15	Ì	:	3.15] -	v
	<u>i</u>	1161 — 20µA		6.0	4.2		L	4.2		
		$V_0 = 0.1V, V_{CC}$	_0.10	2.0			0.5		0.5	
VIL	Low-level input voltage	$ V_0 = 0.1V, V_{CC} $ $ I_0 = 20\mu A$		4.5			1.35	/	1.35	v
		1161 — 20μΑ		6.0			1.8		1.8	l
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
V	High-level output voltage	$V_{l} = V_{lH}, V_{lL}$	$I_{OH} = -20\mu A$	4.5	4.4	ļ		4.4	1	v
V _{OH}	nigh-lever output voltage	VI - VIH, VIL	$I_{OH} = -20\mu A$	6.0	5.9			5.9	<u></u>	. V
	1		$I_{OH} = -24mA$	4.5	3. 98			3. 84		
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
Vol	Low-level output voltage	$V_{l} = V_{lH}, V_{lL}$	$I_{OL} = 20 \mu A$	4.5		\	0.1		0.1	l v
VOL	Low-level output voltage	VI — VIH, VIL	$I_{OL} = 20 \mu A$	6.0		[0.1		0.1	
	1		I _{OL} = 24mA	4.5			0.39		0.5	
I _{IH}	High-level input current	$V_i = 6V$		6.0			0.1		1.0	μA
I _{IL}	Low-level input current	$V_1 = 0V$		6.0			-0.1		-1.0	μA
lozh	Off-state high-level output current	$V_{i} = V_{iH}, \ V_{iL}, \ V$	$v_0 = v_{cc}$	6.0			0.5		5.0	μA
IOZL	Off-state low-level output current	$V_{I} = V_{IH}, V_{IL}, V$	$V_I = V_{IH}, \ V_{IL}, \ V_O = GND$				-0.5		-5. 0	μA
lcc ·	Quiescent supply current	VI = VCC, GND	$I_{0} = 0 \mu A$	6.0			5.0		50.0	μA

SWITCHING CHARACTERISTICS $(v_{cc} = 5v, T_a = 25^{\circ})$

Ob. ad	Parameter	Test conditions		Unit		
Symbol	Parameter	lest conditions	Min	Тур	Max	Offic
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time	$C_1 = 50pF (Note 4)$			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	CL — SUPP (Note 4)			15	ns
t _{PHL}	output propagation time (A - B, B - A)				15	ns
t _{PLZ}	Output disable time from low-level and high-level	$C_1 = 5 pF (Note 4)$			25	ns
t _{PHZ}	(OE - A, B)	CL — 5 pr (Note 4)			25	ns
t _{PZL}	Output enable time to low-level and high-level	C _L = 50pF (Note 4)			28	ns
t _{PZH}	(OE - A, B)	CL — 50pr (Note 4)			28	ns

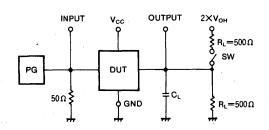
SWITCHING CHARACTERISTICS ($v_{cc} = 2\sim 6v$, $\tau_a = -40\sim +85\%$)

						Limits			
Symbol	Parameter Test conditions			25℃			-40~+85°C		Unit
		V _{cc} (V)		Min	Тур	Max	Min	Max	
			2.0		1	60		75	
t _{TLH}	Low-level to high-level and		4.5		1	12	1	15	1
	high-level to low-level		6.0			10		13	ns
	migh-level to low-level		2.0			60		75	115
t _{THL}	output transition time		4.5			12	ر ا	15	
			6.0			10		13	
			2.0			85		105	
t _{PLH}	Low-level to high-level and		4.5			17		21	
	high-level to low-level		6.0			14		18	
	output propagation time		2.0			85		105	ns
t _{PHL}	(A-B, B-A)		4.5			17		21	
		C _L = 50pF (Note 4)	6.0			14		18	
		GL — Sopr (Note 4)	2.0			150		190	
t _{PLZ}	Output disable time from		4. 5		1	30	ł	38	, .
	low-level and high-level		6.0		-	26		33	ns
-	low-lever and mgn-lever		2.0			150		190	115
t _{PHZ}	(OE - A, B)		4.5	-		30		38	ľ
			6.0			26		33	
			2.0			150	,	190	
t _{PZL}	Output enable time to	· ·	4.5			30		38	
	low-level and high-level		6.0			26	<u> </u>	33	
	low-lever and migh-lever		2.0			150		190	ns
t _{PZH}	(OE - A, B)		4.5			30	l	38	
_			6.0			26		33	
Cı	Input capacitance					10		10	pF
Со	Off-state output capacitance	OE = V _{CC}				15		15	pF
C _{PD}	Power dissipation capacitance (Note 3)								pF

Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per transceiver) The power dissipation during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$



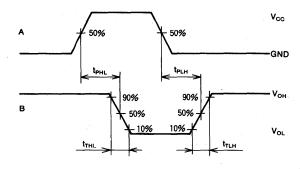
Note 4: Test Circuit

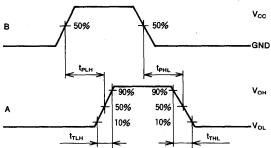


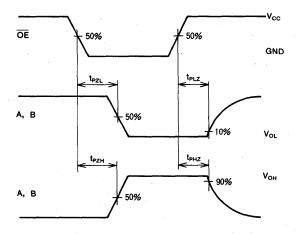
Parameter	sw
t _{TLH} , t _{THL} t _{PLH} , t _{PHL}	Open
t _{PLZ}	Closed
t _{PHZ}	Open
tpZL	Closed
t _{PZH}	Open

- (1) The pulse generator (PG) has the following characteristics (10% \sim 90%): $t_f=3ns,\,t_f=3ns$
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM









M74HCT643-1P/FP/DWP

OCTAL 3-STATE INVERTING
AND NONINVERTING BUS TRANSCEIVER WITH LSTTL-COMPATIBLE INPUTS

DESCRIPTION

The M74HCT643-1 is a semiconductor integrated circuit consisting of eight transceivers with inverted and noninverted outputs.

FEATURES

- TTL level inputs V_{IL}=0.8V max, V_{IH}=2.0V min
- High-fanout 3-state output: (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed: 10ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 25µW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- Capable of driving 60 74LSTTL loads
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HCT643-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS643.

The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

As the inputs are TTL level, the device can be used as a level converter from LSTTL to high-speed CMOS. In that case, no pull-up resistors are required.

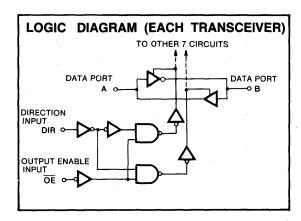
Two buffers with 3-state inverted and noninvertered outputs have their inputs and outputs mutually connected and can be used as buffers in both directions.

The Input/output direction is controlled by direction input

When DIR is high, the data ports A will become input terminals and the data ports B will become output terminals. When DIR is low, B will become input terminals and A will become output terminals.

When output enable input \overline{OE} is high, A and B will both become a high-impedance state and they will be separated.

PIN CONFIGURATION (TOP VIEW) DIRECTION DIR → 1 Vcc OUTPUT ENABLE - ŌE 19 A1 A3 ↔ 4 - B2 16 ++ B3 DATA PORTS A5 ↔ 6 15 + R4 DATA PORTS A6 ↔ 7 14 → B5 A7 ↔ 8 13 → B6 Ά8 - 9 R7 GND + B8 20P4 Outline 20P2N 20P2V



FUNCTION TABLE (Note 1)

	outs	Out	puts
OE	OE DIR		В
L	L L		ŀ
L	L H		ō
Н	х	Z	Z

Note 1: I : Input terminal

O: Output terminal (noninverted output)

O: Output terminal (inverted output)

Z : High impedance (A and B are separated)

X : Irrelevant

MITSUBISHI HIGH SPEED CMOS M74HCT643-1P/FP/DWP

OCTAL 3-STATE INVERTING AND NONINVERTING BUS TRANSCEIVER WITH LSTTL-COMPATIBLE INPUTS

ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85$ °C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	v
Vı	Input voltage		-0.5~V _{cc} +0.5	٧
Vo ·	Output voltage		-0.5~V _{cc} +0.5	V
1	land protection diade convert	V ₁ < 0V	-20	
lik	Input protection diode current	$V_{i} > V_{CC}$	20	mA
	Outrot accepted died accept	V _o < 0V	-20	
Іок	Output parasitic diode current	Vo > Vcc	20	mA
lo	Output current per output pin		±50	mA
lcc	Supply/GND current	V _{CC} , GND	±200	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65~+150	°C

Note 2 : M74HCT643-1FP, $T_a = -40 \sim +75 ^{\circ} C$ and $T_a = 75 \sim 85 ^{\circ} C$ are derated at $-7 mW/^{\circ} C$. M74HCT643-1DWP, $T_a = -40 \sim +80 ^{\circ} C$ and $T_a = 80 \sim 85 ^{\circ} C$ are derated at $-7 mW/^{\circ} C$.

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85 \degree c)$

0		Parameter		Limits				
Symbol	Pai	Min	Тур	Max	Unit			
Vcc	Supply voltage		4.5		5.5	V		
V _I	Input voltage		0		Vcc	V		
Vo	Output voltage	Output voltage			Vcc	V		
Topr	Ambient operating temper	erature	-40		+85	°C		
		V _{CC} = 4.5V	0		25	- 04		
t _r , t _f	Input risetime, falltime V _{CC} = 5.5V		0		15	ns/V		

ELECTRICAL CHARACTERISTICS ($V_{cc} = 5V \pm 10\%$, unless otherwise noted)

						Limits		_	,
Symbol	Parameter	Test conditions		25℃			-40~+85℃		Unit
				Min	Тур	Max	Min	Max	`
V _{IH}	High-level input voltage	$V_0 = 0.1V$, $V_{CC} = 0.1V$ $ I_0 = 20\mu A$		2.0			2.0	,	v
VIL	Low-level input voltage	$V_0 = 0.1V$, $V_{CC} = 0.1V$ $ I_0 = 20\mu A$				0.8	. 1	0.8	v
			$I_{OH} = -20\mu A$	V _{cc} -0.1			V _{cc} -0.1		V
V _{он}	High-level output voltage	$V_i = V_{iL}$	$I_{OH} = -24 \text{mA}, \ V_{CC} = 4.5 \text{V}$	3. 98			3. 84		\ \ \
			$I_{OL} = 20\mu A$			0.1		0.1	v
Vol	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	I _{OL} = 24mA, V _{CC} = 4.5V			0.39		0.5	\ \
l _{iH}	High-level input current	$V_{I} = V_{CC}$				0.1		1.0	
l _{IL}	Low-level input current	VI = GND				-0.1		-1.0	μΑ
lozh	Off-state high-level output current	$V_{l} = V_{lH}, \ V_{lL},$	$V_0 = V_{CC}$			0.5		5.0	
lozL	Off-state low-level output current	$V_{i} = V_{iH}, \ V_{iL},$	V _O = GND			-0.5		-5. 0	μA
Icc	Quiescent supply current	VI = VCC, GNE	$0, l_0 = 0\mu A$			5.0		50.0	μA
△lcc	Maximum quiescent supply current	$V_1 = 2.4V, 0.4$	V (Note 3)			2.7		2. 9	mA

Note 3: Only one input is set at this value and all other inputs are fixed at V_{CC} or GND.

MITSUBISHI HIGH SPEED CMOS M74HCT643-1P/FP/DWP

OCTAL 3-STATE INVERTING AND NONINVERTING BUS TRANSCEIVER WITH LSTTL-COMPATIBLE INPUTS

SWITCHING CHARACTERISTICS ($V_{cc} = 5V$, $T_a = 25^{\circ}C$)

Symbol	Parameter	Test conditions	Limits			Unit
Symbol	Parameter	1 est conditions	Min	Тур	Max] Onk
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time	C ₁ = 50pF (Note 5)			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	$C_{L} = 50pF (Note 5)$			15	ns
t _{PHL}	output propagation time (A - B, B - A)	· · · · · · · · · · · · · · · · · · ·			15	ns
t _{PLZ}	Output disable time from low-level and high-level	C = E = E (Note E)			25	ns
t _{PHZ}	(OE – A, B)	$C_L = 5 pF (Note 5)$			25	ns
t _{PZL}	Output enable time to low-level and high-level	C ₁ = 50pF (Note 5)			28	ns
t _{PZH}	(OE – A, B)	OL — Sopr (Note 5)			28	ns

SWITCHING CHARACTERISTICS ($V_{cc} = 5V \pm 10\%$, $T_a = -40 \sim +85$ °C)

					Limits			
Symbol	Parameter	Test conditions		25℃			-40~+85℃	
			Min	Тур	Max	Min	Max]
t _{TLH} .	Low-level to high-level and				12		15	
t _{THL}	high-level to low-level output transition time				- 12		15	ns
t _{PLH}	Low-level to high-level and high-level to low-level				17		21	ns
t _{PHL}	output propagation time (A - B, B - A)				17		21	115
t _{PLZ}	Output disable time from	C _L = 50pF (Note 5)			30		38	
7.22	low-level and high-level				-			ns
t _{PHZ}	(OE - A, B)	,			30	_	38	
t _{PZL}	Output enable time to				30		38	
	low-level and high-level	•			-			ns
t _{PZH}	(OE - A, B)			1	30		38	
Cı	Input capacitance				10		10	
Co	Off-state output capacitance	OE = V _{CC}			15		15	pF
C _{PD}	Power dissipation capacitance (Note 4)							

Note 4: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per transceiver)

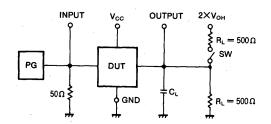
The power dissipated during operation under no-load conditions is calculated using the following formula:

P_D = C_{PD} • V_{CC}² • f₁+I_{CC} • V_{CC}



OCTAL 3-STATE INVERTING AND NONINVERTING BUS TRANSCEIVER WITH LSTTL-COMPATIBLE INPUTS

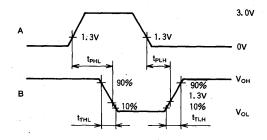
Note 5 : Test Circuit

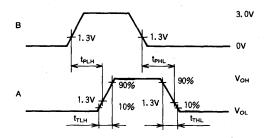


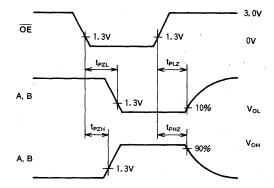
Parameter	SW
t _{TLH} , t _{THL}	Open
t _{PLZ}	Closed
t _{PHZ}	Open
tezL	Closed
t _{PZH}	Open

- (1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 3ns, t_f = 3ns (2) The capacitance C_L includes stray wiring
- capacitance and the probe input capacitance.

TIMING DIAGRAM







M74HC645P/FP/DWP

OCTAL 3-STATE NONINVERTING BUS TRANSCEIVER

DESCRIPTION

The M74HC645 is a semiconductor integrated circuit consisting of eight transceivers with noninverted outputs.

FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=-6mA)
- High-speed: 13ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: Ta=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC645 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS645.

Two buffers with 3-state noninverted outputs have their inputs and outputs mutually connected and can be used as buffers in both directions.

The input/output direction is controlled by direction input DIR.

When DIR is high, the data ports A will become input terminals and the data ports B will become output terminals. When DIR is low, B will become input terminals and A will become output terminals.

When output enable input \overline{OE} is high, A and B will both become a high-impedance state and they will be separated.

FUNCTION TABLE (Note 1)

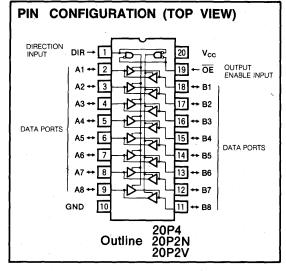
In	puts	Out	puts
OE	DIR	Α	В
L	L	0	1
L	н	1	0
Н	х '	Z	Z

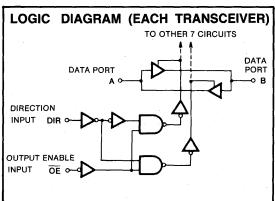
Note 1: I : Input terminal

O: Output terminal (noninverted output)

Z : High impedance (A and B are separated)

X : Irrelevant





ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{CC} +0.5	V
L	Input protection diode current	V ₁ < 0V	-20	T .
lik .	mput protection diode current	$V_{I} > V_{CC}$	20	. mA
l	Output parasitic diode current	V ₀ < 0V	-20	1
lok	Culput parasitic diode current	Vo > Vcc	20	mA
lo	Output current per output pin		±35	mA
lcc ·	Supply/GND current	V _{CC} , GND	±75	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		-65~+150	င

Note 2 : M74HC645FP, $T_a=-40\sim+75^\circ$ C and $T_a=75\sim85^\circ$ C are derated at $-7mW/^\circ$ C. M74HC645DWP, $T_a=-40\sim+80^\circ$ C and $T_a=80\sim85^\circ$ C are derated at $-7mW/^\circ$ C.

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85\%)$

Cumbal	Parameter			Unit		
Symbol	Pa	rameter	Min	Тур	Max	Unit
Vcc	Supply voltage				6	V
V _I	Input voltage		0		Vcc	٧
V _o	Output voltage		0		Vcc	٧
Topr	Operating temperature ra	ange	-40		+85	°
		$V_{CC} = 2.0V$	0		1000	
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns
		$V_{CC} = 6.0V$	0		400	

ELECTRICAL CHARACTERISTICS

							Limits			i
Symbol	Parameter	Test	conditions		25℃			-40~	+85°C	Unit
	-	V _{cc} (v)		Min	Тур	Max	Min	Max		
		$V_0 = 0.1V, V_{CC}$	0.11/	2.0	1.5			1.5	, ,	4
ViH	High-level input voltage	$ V_0 = 0.1V, V_{CO}$ $ I_0 = 20\mu A$			3.15			3.15		V
		$ 1_0 = 20\mu\text{A}$		6.0	4.2			4. 2		
		$V_{\rm O} = 0.1 V, V_{\rm CO}$	0.114.140.114				0.5		0.5	
VIL	Low-level input voltage	$ V_0 = 0.1V, V_{CO}$ $ I_0 = 20\mu A$	50-1 V	4.5			1.35		1.35	٧
	10 = 20µA			6.0			1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
			$I_{OH} = -20\mu A$	4.5	4.4			4.4		
V_{OH}	High-level output voltage	$V_{i} = V_{iH}, V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9	i		5.9		l v
	-		$I_{OH} = -6.0 \text{mA}$	4.5	4.18			4.13		
			$I_{OH} = -7.8 mA$	6.0	5. 68			5.63		
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
			$I_{OL} = 20 \mu A$	4.5			0.1		0.1	
VoL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1	1.5	0.1	V
			$I_{OL} = 6.0 \text{mA}$	4.5			0. 26		0.33	
			I _{OL} = 7.8mA	6.0			0. 26	l _	0.33	
l _{iH}	High-level input current	$V_1 = 6V$		6.0			0. 1		1.0	μΑ
l _{IL}	Low-level input current	$V_I = 0V$		6.0			-0.1		-1.0	μP
lozh	Off-state high-level output current	$V_i = V_{iH}, \ V_{iL},$	$V_{\rm o} = V_{\rm cc}$	6.0			0.5		5.0	μΑ
lozL	Off-state low-level output current	$V_{I} = V_{IH}, V_{IL},$	Vo = GND	6.0			-0.5		-5.0	μP
Icc	Quiescent supply current	VI = VCC, GNE	$I_0 = 0 \mu A$	6.0			4.0		40.0	μА

SWITCHING CHARACTERISTICS $(V_{cc} = 5V, T_a = 25^{\circ}C)$

Symbol	Parameter	Test conditions		Limits		
- Cyllibol	Falanetei	Test conditions	Min	Тур	Max	Unit
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time	C _L = 50pF (Note 4)			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level				21	ns
t _{PHL}	output propagation time $(A - B, B - A)$				21	ns
t _{PLZ}	Output disable time from low-level and high-level	C _L = 5 pF (Note 4)			42	ns
t _{PHZ}	(OE - A, B)	CL = 5 pr (Note 4)			42	ns
t _{PZL}	Output enable time to low-level and high-level	$C_1 = 50 pF \text{ (Note 4)}$			42	ns
t _{PZH}	(OE - A, B)	CL — SUPF (Note 4)			42	ns

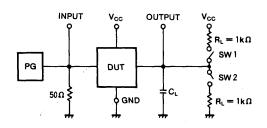
SWITCHING CHARACTERISTICS $(V_{cc} = 2\sim6V, T_a = -40\sim+85^{\circ}C)$

						Limits			
Symbol	Parameter	Test conditions			25℃		-40~	+85℃	Unit
			V _{CC} (V)	Min	Тур	Max	Min	Max	
		1	2.0]		60	1	75	
t _{TLH}	Low-level to high-level and		4.5	!		12	[15	ns
	high-level to low-level	C _L = 50pF (Note 4)	6.0			10		13	
	mign-lever to low-lever	CL — SOPP (Note 4)	2.0			60		75	
t _{THL}	output transition time		4. 5			12		15	ns
			6.0			10		13	
			2.0			110		140	
t _{PLH}			4.5			22		28	ns
		C _L = 50pF (Note 4)	6.0			19	[24	
		C _L = 50pr (Note 4)	2.0			110		140	
t _{PHL}	Low-level to high-level and		4.5	ł		22		28	ns
	high-level to low-level		6.0		}	19		24	
	output propagation time		2.0			195		245	
t _{PLH}	(A - B, B - A)		4.5		į	39	1	49	ns
	-	0 - 150-5 (N-4-4)	6.0			34		43	l
		$C_L = 150 pF (Note 4)$	2.0			195		245	
t _{PHL}			4.5			39		49	ns
			6.0	43					
			2.0			172		208	
t_{PLZ}	Output disable time from		4.5		İ	43		52	ns
		0 - 50-5 (N-4- 4)	6.0	1		` 41	1	50	ł
-	low-level and high-level	$C_L = 50 pF \text{ (Note 4)}$	2.0			172		208	
t _{PHZ}	(OE - A, B)		4.5			43		52	ns
			6.0		ļ	41]	50	
			2.0			184		224	
t _{PZL}			4.5			46	ľ	56	ns
		0 50-5 (N-+- 4)	6.0			41		50	
	1	$C_L = 50 pF (Note 4)$	2.0			184		224	
t _{PZH}	Output enable time to low-level		4.5			46		56	ns
			6.0			41	1	50	
	and high-level		2.0			216		260	
t _{PZL}	(OE - A, B)	1.	4.5			54		65	ns
-		150 5 (1)	6.0	1	1	47		57	1
	1	C _L = 150pF (Note 4)	2.0		1	216		260	
t _{PZH}			4.5	1		54		65	ns
		<u> </u> -	6.0			47		57	
Çı	Input capacitance					10		10	рF
Co	Off-state output capacitance	OE = V _{CC}				15	1	15	pF
C _{PD}	Power dissipation capacitance (Note 3)				- 58				pF

Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per transceiver) The power dissipation during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$



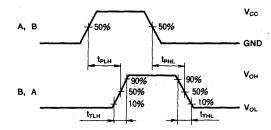
Note 4: Test Circuit

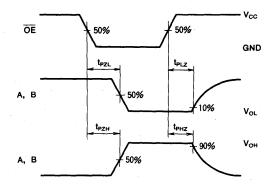


Parameter	SW1	SW 2
t _{TLH} , t _{THL} t _{PLH} , t _{PHL}	Open	Open
t _{PLZ}	Closed	Open
t _{PHZ}	Open	Closed
t _{PZL}	Closed	Open
t _{PZH}	Open	Closed

- (1) The pulse generator (PG) has the following
- characteristics $(10\% \sim 90\%)$: $t_f = 6$ ns, $t_f = 6$ ns (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM







M74HC645-1P/FP/DWP

OCTAL 3-STATE NONINVERTING BUS TRANSCEIVER

DESCRIPTION

The M74HC645-1 is a semiconductor integrated circuit consisting of eight bus transceivers with noninverted outputs.

FEATURES

- High-fanout 3-state output: (I_{OL}=24mA, I_{OH}=-24mA)
- High-speed: 8ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 25µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 60 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC645-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS645.

The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

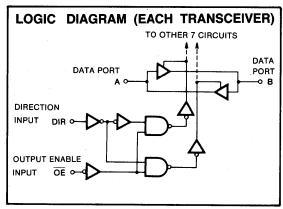
Two buffers with 3-state noninverted outputs have their inputs and outputs mutually connected and can be used as buffers in both directions.

The input/output direction is controlled by direction input DIR.

When DIR is high, the data ports A will become input terminals and the data ports B will become output terminals. When DIR is low, B will become input terminals and A will become output terminals.

When output enable input \overline{OE} is high, A and B will both become a high-impedance state and they will be separated.

PIN CONFIGURATION (TOP VIEW) DIRECTION DIR v_{cc} INPUT OUTPUT 19 ← ŌE ENABLE INPUT 18 16 → B3 DATA PORTS 15 + B4 DATA PORTS 14 13 12 **GND** 20P4 Outline 20P2N



FUNCTION TABLE (Note 1)

Inp	Inputs		ports
OE	DIR .	Α	В
L	L	0	ı
L	н	1	0.
н	X	Z	Z

Note 1: I : Input terminal

O: Output terminal (noninverted output)

Z : High impedance (A and B are separated)

X : Irrelevant

ABSOLUTE MAXIMUM RATINGS $(T_a = -40 \sim +85\%$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	· V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
,		V ₁ < 0V	-20	'A
1 _{IK}	Input protection diode current	V ₁ > V _{CC}	. 20	mA
		V ₀ < 0V	-20	
ок	Output parasitic diode current	V _o > V _{cc}	20	mA mA
lo	Output current per output pin		±50	mA
Icc	Supply/GND current	V _{CC} , GND	±200	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		-65~+150	င

Note 2 : M74HC645-1FP, T_a = $-40\sim+75^\circ$ C and T_a = $75\sim85^\circ$ C are derated at -7mW/°C. M74HC645-1DWP, T_a = $-40\sim+80^\circ$ C and T_a = $80\sim85^\circ$ C are derated at -7mW/°C.

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85^{\circ}\text{C})$

Committee and				Limits		Unit
Symbol	Pai	rameter	Min	Тур	Max	Unit
Vcc	Supply voltage		2		6	V.
Vi	Input voltage		0		Vcc	V
Vo	Output voltage		0		V _{CC}	٧
Topr	Operating temperature ra	inge	-40		+85	င
	* *	$V_{CC} = 2.0V$	0	,	500	
t _r , t _f	input risetime, falltime	$V_{CC} = 4.5V$	0		50	ns/V
	*	$V_{CC} = 6.0V$	0		30]

ELECTRICAL CHARACTERISTICS

		· ·								
Symbol	Parameter	Test	Test conditions		25℃			-40~+85℃		Unit
				V _{cc} (V)	Min	Тур	Max	Min	Max	
		V = 0 1V V	0.1V, V _{CC} -0.1V		1.5			1.5		
V _{IH}	High-level input voltage	$ V_0 - 0.1V, V_{CO} $ $ I_0 = 20\mu A$;0. T V	4.5	3.15			3, 15		V
	1101 - 20µA		6.0	4.2			4.2	`		
		$V_0 = 0.1V, V_{00}$	_0.1V	2.0			0.5		0.5	,
VIL	Low-level input voltage	$ V_0 - 0.1V, V_{CC} $	5—0. I V	4.5			1.35		1.35	V
	, 1101	$ 10 = 20\mu A$		6.0			1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9	-		1.9		
	V - V V	$I_{OH} = -20\mu A$	4. 5	4.4			4.4		v	
V _{OH}	High-level output voltage	$V_{l} = V_{lH}, V_{lL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		•
			$I_{OH} = -24mA$	4.5	3. 98			3.84		
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
VoL	Low-level output voltage	$V_{l} = V_{lH}, V_{lL}$	$I_{OL} = 20 \mu A$	4.5			0.1		0.1	v
VOL	Low-rever output voltage	VI - VIH, VIL	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	*
			I _{OL} = 24mA	4.5			0.39		0.5	
I _{IH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μΑ
I _{IL}	Low-level input current	V ₁ = 0V		6.0			-0.1		-1.0	μA
lozh	Off-state high-level output current	$V_i = V_{iH}, V_{iL}, V_{iL}$	$V_0 = V_{CC}$	6.0			0.5		5.0	μΑ
lozL	Off-state low-level output current	$V_i = V_{iH}, \ V_{iL}, \ V_{iL}$	o = GND	6.0		l	-0.5		-5.0	μA
lcc	Quiescent supply current	VI = VCC, GND	$I_0 = 0\mu A$	6.0			5.0		50.0	μA

MITSUBISHI HIGH SPEED CMOS M74HC645-1P/FP/DWP

OCTAL 3-STATE NONINVERTING BUS TRANSCEIVER

SWITCHING CHARACTERISTICS $(v_{cc} = 5v, \tau_a = 25\%)$

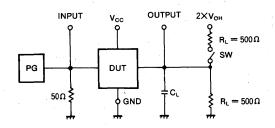
Symbol	Parameter	Test conditions		Limits		
Зупівої	Parameter	l est conditions	Min	Тур	Max	Unit
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time	C ₁ = 50pF (Note 4)			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = 50pr (Note 4)			15	ns
t _{PHL}	output propagation time (A - B, B - A)				15	ns
t _{PLZ}	Output disable time from low-level and high-level	O = 5 = F (N)=+= 4)			25	ns
t _{PHZ}	(OE - A, B)	C _L = 5 pF (Note 4)			25	ns
t _{PZL}	Output enable time to low-level and high-level	C = 50=5 (Note 4)			28	ns
t _{PZH}	(OE - A, B)	C _L = 50pF (Note 4)			28	ns

SWITCHING CHARACTERISTICS ($v_{cc} = 2\sim6$ V, $T_a = -40\sim+85$ °C)

		·				Limits			
Symbol	Parameter	Test conditions			25℃		-40 ~	+85°C	Unit
		<u> </u>	V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0			60		75	
t _{TLH}	Low-level to high-level and		4.5			12		15	
	high-level to low-level		6.0		-	10		13	ns
	Inight-level to low-level		2.0			60		75	118
t _{THL}	output transition time		4.5		ļ	12		15	
			6.0			10		13	
		1	2.0			85		105	
t _{PLH}	Low-level to high-level and		4.5			17		21	
4	high-level to low-level		6.0			14		18	ns
	output propagation time		2.0			85		105	115
t _{PHL}	(A - B, B - A)		4.5			17		21	
		C _L = 50pF (Note 4)	6.0			14		18	
		OL — Supr (Note 4)	2.0			150		190	
t _{PLZ}	Output disable time from		4.5		j	30		38	
	low-level and high-level		6.0			26		33	ns
			2.0			150		190	''3
t _{PHZ}	(OE - A, B)		4.5			30		38	
			6.0			26		33	
			2.0			150		190	
t _{PZL}	Output enable time to		4.5			30		38	
	low-level and high-level		6.0			26		33	ns
		-	2.0			150		190	'''
t _{PZH}	(OE - A, B)	*	4.5			30		38	
			6.0			26		33	
Cı	Input capacitance					10		10	
Co	Off-state output capacitance	ŌE = V _{CC}				15		15	рF
CPD	Power dissipation capacitance (Note 3)								1

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per transceiver) The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$

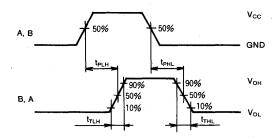
Note 4: Test Circuit

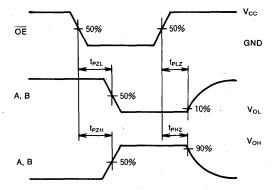


Parameter	sw
t _{TLH} , t _{THL} t _{PLH} , t _{PHL}	Open
t _{PLZ}	Closed
t _{PHZ}	Open
t _{PZL}	Closed
t _{PZH}	Open

- (1) The pulse generator (PG) has the following characteristics (10%~90%): t_f = 3ns, t_f = 3ns
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM







M74HCT645-1P/FP/DWP

NONINVERTING BUS TRANSCEIVER WITH LSTTL-COMPATIBLE INPUTS

DESCRIPTION

The M74HCT645-1 is a semiconductor integrated circuit consisting of eight three-state noninverted bus transceivers.

FEATURES

- TTL level input V_{IL}=0.8V max V_{IH}=2.0V min
- High-fanout 3-state output: (I_{OL}=24mA, I_{OH}=-24mA)
- High-speed: 10ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 25µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- Capable of driving 60 74LSTTL loads
- Wide operating temperature range: T_a=-40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HCT645-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS645.

The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

As the inputs are TTL level, the device can be used as a level converter from LSTTL to high-speed CMOS. In that case, no pull-up resistors are required.

Two buffers with 3-state noninverted outputs have their inputs and outputs mutually connected and can be used as buffers in both directions.

The input/output direction is controlled by direction input DIR.

When DIR is high, the data ports A will become input terminals and the data ports B will become output terminals. When DIR is low, B will become input terminals and A will become output terminals.

When output enable input \overline{OE} is high, A and B will both become a high-impedance state and they will be separated.

FUNCTION TABLE (Note 1)

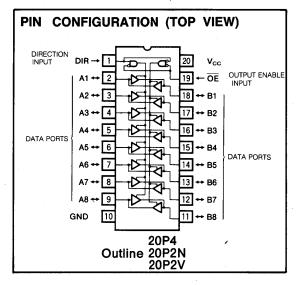
Inj	outs	Data ports		
OE	DIR	Α	В	
L	L	0	1	
L	н	1	O	
Н	х	Z	Z	

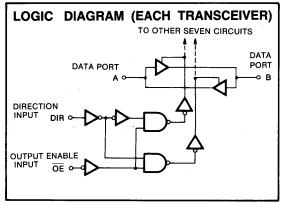
Note 1: I:Input

O: Output (noninverting output)

Z : High impedance (A and B are isolated)

X : Irrelevant





OCTAL 3-STATE NONINVERTING BUS TRANSCEIVER WITH LSTTL-COMPATIBLE INPUTS

ABSOLUTE MAXIMUM RATINGS $(T_a = -40 \sim +85 \degree$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	·	−0.5~+7.0	V
V _I	Input voltage		-0.5~V _{cc} +0.5	V.
Vo	Output voltage		-0.5~V _{cc} +0.5	V
	In a section died a second	V ₁ < 0V	-20	
lik .	Input protection diode current	V _i > V _{cc}	20	mA.
	Cutant associate diada sumant	V _o < 0V	20	
Іок	Output parasitic diode current	$v_o > v_{cc}$	20	mA.
lo	Output current per output pin		±50	mA
loc	Supply/GND current	V _{CC} , GND	±200	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature		-65~+150	ొ

Note 2 : M74HCT645-1FP , $T_a=-40\sim+75^\circ\mathrm{C}$ and $T_a=75\sim85^\circ\mathrm{C}$ are derated at $-7\mathrm{mW/C}$. M74HCT645-1DWP, $T_a=-40\sim+80^\circ\mathrm{C}$ and $T_a=80\sim85^\circ\mathrm{C}$ are derated at $-7\mathrm{mW/C}$.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85^{\circ}C)$

0	D.	Parameter		Limits				
Symbol	Pai	rameter	Min	Тур	Max	Unit		
V _{CC}	Supply voltage		4. 5		5.5	V		
Vı	Input voltage		0		V _{CC}	V		
Vo	Output voltage		. 0		V _{cc}	٧		
Topr	Operating temperature ra	ange	-40	-	+85	င		
	In	V _{CC} = 4.5V	0	-	25	01		
t _r , t _f Input risetime, falltime	Input risetime, falltime V _{CC} = 5.5V	. 0		15	ns/V			

ELECTRICAL CHARACTERISTICS

						Limits			
Symbol	Parameter		Test conditions		25℃		-40~	+85℃	Unit
•				Min	Тур	Max	Min	Max	
V _{IH}	High-level input voltage	$V_0 = 0.1V, V_{C}$ $ I_0 = 20\mu A$	c - 0.1V	2.0			2.0		V
VIL	Low-level input voltage	$V_0 = 0.1V, V_0$ $ I_0 = 20\mu A$	_c -0.1V			0.8		0.8	>
.,			$I_{OH} = -20\mu A$	V _{cc} -0.1			V _{cc} -0.1		V
V _{OH} .	high-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OH} = -24 \text{mA}, \ V_{CC} = 4.5 \text{V}$	3.98			3.84		٧
.,		.,, .,	$I_{OL} = 20\mu A$			0.1		0. 1	>
VoL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 24 \text{mA}, \ V_{CC} = 4.5 \text{V}$			0, 39		0.5	٧
I _{IH}	high-level input current	$V_i = V_{CC}$				0.1		. 1.0	
l _{IL}	Low-level input current	V _I = GND				-0.1		-1.0	μA
lozh	Off-state high-level output current	$V_{l} = V_{lH}, \ V_{lL},$	$V_0 = V_{CC}$			0.5		5.0	
lozL	Off-state low-level output current	$V_{I} = V_{IH}, \ V_{IL},$	V _o = GND			-0.5		-5.0	μA
Icc	Quiescent supply current	VI = VCC, GNE	$0, \ I_0 = 0\mu A$			5.0		50.0	μА
△lcc	Maximum quiescent supply current	$V_1 = 2.4V, 0.4$	V (Note 3)			2.7		2. 9	mA

Note 3: Only one input is set at this value and all other inputs are fixed at V_{CC} or GND.

OCTAL 3-STATE NONINVERTING BUS TRANSCEIVER WITH LSTTL-COMPATIBLE INPUTS

SWITCHING CHARACTERISTICS $(V_{cc} = 5V, T_a = 25^{\circ}C)$

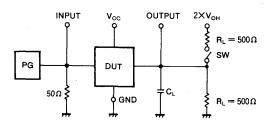
Symbol	Parameter	TA		Limits		Unit
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
t _{TLH}	Low-level to high-level and high-level to low-level		-		10	
t _{THL}	output transition time	$C_1 = 50 \text{pF} (\text{Note 5})$			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	$C_L = \text{supp (Note 5)}$			15	
t _{PHL}	output propagation time $(A - B, B - A)$				15	ns
t _{PLZ}	Output disable time from low-level and high-level	$C_L = 5 pF (Note 5)$	T.		25	
t _{PHZ}	(OE - A, B)	GL = 5 pr (Note 5)			25	ns
t _{PZL}	Output enable time to low-level and high-level	C _L = 50pF (Note 5)			28	
t _{PZH}	(OE - A, B)	OL — Sope (Note 5)			28	ns

SWITCHING CHARACTERISTICS ($v_{cc} = 5v \pm 10\%$, $T_a = -40 \sim +85\%$)

			-		Limits			
Symbol	Parameter	Test conditions		25℃		-40~	+85℃	Unit
			Min	Тур	Max	Min	Max	
t _{TLH}	Low-level to high-level and	,			12		15	ns
tTHL	high-level to low-level output transition time				12		15	118
t _{PLH}	Low-level to high-level and				17	· ·	21	
	high-level to low-level output			<u> </u>				ns
t _{PHL}	propagation time $(A - B, B - A)$				17		21	
t _{PLZ}	Output disable time from	C _L = 50pF (Note 5)	1		30		38	
	low-level and high-level					-		ns
t _{PHZ}	(OE - A, B)				30		38	
t _{PZL}	Output enable time to				30		38	
	low-level and high-level							ns
t _{PZH}	(OE - A, B)				30		38	
Cı	Input capacitance				10		10	
Co	Off-state output capacitance	ÖE = V _{CC}			15		15	pF.
C _{PD}	Power disipation capacitance (Note 4)							

Note 4: CPD is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per transceiver) The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$

Note 5: Test Circuit

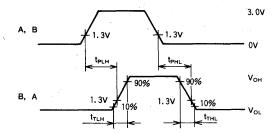


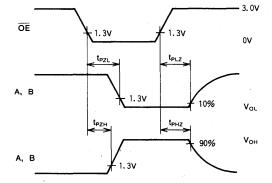
Parameter	SW
t _{TLH} , t _{THL} t _{PLH} , t _{PHL}	Open
t _{PLZ}	Closed
t _{PHZ}	Open
t _{PZL}	Closed
t _{PZH}	Open

- (1) The pulse generator (PG) has the following
- characteristics (10% \sim 90%): $t_r = 3$ ns, $t_f = 3$ ns (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

OCTAL 3-STATE NONINVERTING BUS TRANSCEIVER WITH LSTTL-COMPATIBLE INPUTS

TIMING DIAGRAM







M74HC646P/FP/DWP

OCTAL 3-STATE NONINVERTING BUS TRANSCEIVER AND D-TYPE FLIP-FLOP

DESCRIPTION

The M74HC646 is a semiconductor integrated circuit consisting of eight bus transceivers with noninverted outputs.

FEATURES

- High-fanout 3-state outputs (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 70MHz clock frequency typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=-40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC646 to maintain of the low power dissipation and high noise margin the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS646.

The M74HC646 consists of eight bidirectional buffers by interconnecting the I/O buffers of two D-type flip flops with 3-state noninverted outputs. The I/O direction is controlled by output-enable input $\overline{\text{OE}}$ and direction input DIR. The signals are routed from input to output or from the flip flop to output by source select inputs S_{AB} and S_{BA} .

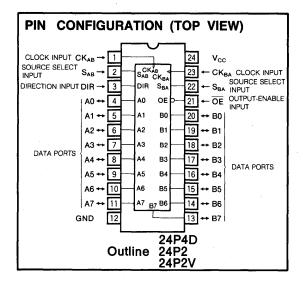
None of the signals are inverted.

When \overline{OE} is low and DIR is high, the data ports A will become input terminals and the data ports B will become output terminals. When S_{AB} goes low, the signal A, which was stored in flip frop (A) as Q_A when S_{AB} was high, appears at B. When S_{AB} is held low and when clock input CK_{AB} changes from low to high, the signal present at A is stored in flip flop (A). When S_{AB} is held high and when CK_{AB} changes from low to high, the signal present at A is inverted and stored in flip flop (A). At the same time, the signal Q_A which was stored in flip frop (A), appears at B.

When $\overline{\text{OE}}$ and DIR are both low, the I/O direction is reversed: B will become input terminals and A will become output terminals. When S_{BA} goes low, the signal B, Which was stored in flip flop (B) as Q_B when S_{BA} was high, appears at A. When S_{BA} is held low and clock input CK_{BA} changes from low to high, the signal present at B is stored in flip flop (B).

When S_{BA} is held high and CK_{BA} changes from low to high, the signal present at B is stored in flip flop (B). At the same time, the signal Q_B which was stored in flip flop (B), appears at A.

When $\overline{\text{OE}}$ is high, both A and B will become high impedance state and they will be separated. When CK_{AB}



changes from low to high, the signal present at A is stored in flip flop (A). When CK_{BA} changes from low to high, the signal present at B is stored in flip flop (B).

FUNCTION TABLE (Note 1)

	-	Contro	inputs	3			Data	port	s	Flip	flop	
ŌĒ	DIR	CKAB	СКва	SAB	SBA		Α		В	QA	Qв	Operational description
Н	Х	Х	Х	Х	X		. X		Х	QAO	Q _B ⁰	The output of data ports A and B are disabled.
Н	X	1	Х	Х	X		L		Х	Q _A ^o	Х	Data ports A and B are stroed by the flip flops at the rising edge of
Н	X	1	X	X	X	ı	Н	1	X	Q _A º	X	CK _{AB} and CK _{BA} . The output of data ports A and B is disabled.
Н	X	X	1	X	X	1	X		L	X	QBO	
Н	X	X	1	X	X		X		H	X	Q _B ⁰	
L	н	×	x*	L	x		L		L	$\overline{Q_A}^0$	Q _B o	The output of data port B is enabled. (Note 2) 1) When S _{AB} is low, data port A appears at data port B. The state of
L	н	×	x*	L	×		н		н	Q _A °	Q _B ⁰	the flip flop (A) is unchanged.
L	Н	×	x*	н	×		×		Q _A o	QÃO	Q _B º	2) When S _{AB} is high, the output of flip flop (A) appears at data port B.
L	Н	t	x*	L	х	'	L	0	L	Q _A ⁰	Q _B ⁰	3) When S _{AB} is low, the data port A appears at data port B and is
L	н	1	х*	L.	х		Н		н	Q _A o	Q _B °	stored in flip flop (A) at the rising edge of CK _{AB} .
L	Н	t	x*	н	х		L		Q _A ⁰	Q _A o	Q _B ⁰	4) When S _{AB} is high, the data port A is stored in flip flop (A) at the ris-
L	н	1	x*	Н	х		Н		Q _A ⁰	Q _A o	Q _B ⁰	ing edge of CK _{AB} , and the output of flip flop (A) appears at data port B.
L	L	x*	х	х	L		L		L	Q _A o	Q _B ⁰	The output of data port A is enabled. (Note 3) 1) When S _{RA} is low, the data port B appears at data port A. The state
 	,	x*	x		<u> </u>				ļ	Q _A °	Q _B 0	of flip flop (B) is unchanged.
L	L	^	^_	×	L		Н		H	Ų _A .	Ų _B -	
L	L	x*	×	×	н		Q _B ⁰		×	Q _A o	Q _B o	2) When S _{BA} is high, the output of flip flop (B) appears at data port A.
L	L	x*	t	x	L	0	L	'	L	$\overline{Q_A}^o$	Q _B ⁰	3) When S _{BA} is low, the data port B appears at data port A and is
L	L	x*	t	х	L		н		Н	Q _A °	Q _B °	stored is flip flop (B) at the rising edge of CK _{AB} .
L	L	x*	t	х	н		Q _B ó		L	$\overline{Q_A}^0$	Q _B ⁰	When S _{BA} is high, the data port B is stored in flip flop (B) and the output of flip flop (B) appears at data port A.
L	L	x*	Ť	х	н		Q _B ⁰		Н	$\overline{Q_A}^0$	Q _B ⁰	output of trip from (B) appears at trata port A.

Note 1: X

: Change from low to high

Q_A⁰, Q_B⁰: Output state of flip flops before the rise of CK_{AB} and CK_{BA}.

: Input terminal of data port

0 Output terminal of data port

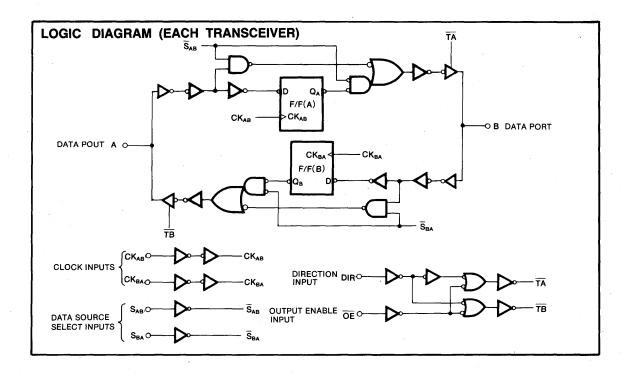
: As CKAB and CKBA are not selected by the I/O directional signal, data from data ports A and B can be stored in the corresponding

flip flops at the rising edge of CKAB or CEBA.

Note 2: The output at port B is given by:

 $B = (A \cdot \overline{S_{AB}}) + (Q_A \cdot S_{AB})$

Note 3: The output at port B is given by: $A = (B \cdot \overline{S_{BA}}) + (Q_B \cdot S_{BA})$



ABSOLUTE MAXIMUM RATINGS $(T_a = -40 \sim +85^{\circ}C)$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V _{cc}	Supply voltage		-0.5~+7.0	.V
Vı	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
		V ₁ < 0V	-20	
lik	Input protection diode current	V _I > V _{CC}	20	mA
	Outside services	V ₀ < 0V	-20	
lok	Output parasitic diode current	$V_0 > V_{CC}$	20	⊢ mA
lo	Output current per output pin		±35	mA
Icc	Supply/GND current	V _{CC} , GND	±75	mA
Pd	Power dissipation	(Note 4)	500	mW
Tstg	Storage temperature range		-65~+150	°C

Note 4 : M74HC646FP, $T_a=-40\sim+80^\circ\text{C}$ and $T_a=80\sim85^\circ\text{C}$ are derated at $-7\text{mW}/^\circ\text{C}$. M74HC646DWP, $T_a=-40\sim+80^\circ\text{C}$ and $T_a=80\sim85^\circ\text{C}$ are derated at $-7\text{mW}/^\circ\text{C}$.

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85 ^{\circ}C)$

Cumahad				Limits		Link
Symbol	Pa	rameter	Min	Тур	Max	Unit
Vcc	Supply voltage	· · · · · · · · · · · · · · · · · · ·	2		6	٧
Vı	input voltage		. 0		Vcc	٧
v _o	Output voltage		0		Vcc	V
Topr	Operating temperature ra	ange	-40		+85	ဗင
		$V_{CC} = 2.0V$	0		1000	
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns
	,	$V_{CC} = 6.0V$	0		400	

ELECTRICAL CHARACTERISTICS

	, ,						Limits		,	
Symbol	Parameter	Test	conditions			25℃		40~	+85℃	Unit
				V _{cc} (V)	Min	Тур	Max	Min	Max	
		$V_0 = 0.1V, V_{CC}$	_0.1V	2.0	1.5			1.5		
VIH	High-level input voltage	$ \mathbf{l}_0 = 20\mu \mathbf{A}$	3 0.14	4.5	3.15		ł	3.15		٧
		1101 - 20µA		6.0	4.2			4.2		
		$V_0 = 0.1V, V_{CC}$	-0.17	2.0			0.5		0.5	
VIL	Low-level input voltage	$ V_0 = 0.1V, V_{CO}$ $ I_0 = 20\mu A$		4.5			1.35		1.35	V
		1101 — 20μA		6.0			1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
			$I_{OH} = -20\mu A$	4.5	4.4		}	4. 4		
V _{OH}	High-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		٧.
			$I_{OH} = -6.0 \text{mA}$	4. 5	4. 18			4.13		
			$I_{OH} = -7.8 \text{mA}$	6.0	5. 68			5.63		
			$I_{OL} = 20 \mu A$	2.0			0.1		0. 1	
	}	\	$I_{OL} = 20 \mu A$	4.5		1	0.1	ì	0.1	
VOL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0		l	0.1		0.1	V
			I _{OL} = 6.0mA	4.5			0.26		0.33	
			I _{OL} = 7.8mA	6.0			0.26		0.33	
I _{IH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μA
l _{IL}	Low-level input current	$V_1 = 0V$		6.0			-0.1		-1.0	μА
lozh	Off-state high-level output current	$V_i = V_{iH}, V_{iL}, V_{iL}$	$v_0 = v_{cc}$	6.0			0.5		5.0	μΑ
lozL	Off-state low-level output current	$V_i = V_{iH}, V_{iL}, V_{iL}$	Vo = GND	6.0			-0.5		-5. 0	μA
loc	Quiescent supply current	VI = VCC, GND	$I_0 = 0 \mu A$	6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS ($v_{cc} = 5v$, $\tau_a = 25\%$)

0	B	T-st distant		Limits		Unit
Symbol	Parameter	Test conditions	Min	Тур	Max	Onit
fmax	Maximum clock frequency	C _L = 50pF (Note 6)	30			MHz
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time				10	ns
t _{PLH}	Low-level to high-level and high-level to low-level				30	ns
t _{PHL}	output propagation time (A - B, B - A)	C = 50=5 (Note 6)			30	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = 50pF (Note 6)			40	ns
t _{PHL}	output propagation time (CK _{AB} - B, CK _{BA} - A)				40	ns
t _{PLH}	Low-level to high-level and high-level to low-level				30	ns
t _{PHL}	output propagation time (SAB - B, SBA - A)	'			30	ns
t _{PLZ}	Output disable time from low-level and high-level	$C_1 = 5pF (Not 6)$			30	ns
t _{PHZ}	(DIR - A, B)	CL — Spr (Not 6)			30	ns
t _{PZL}	Output enable time to low-level and high-level	$C_1 = 50 pF (Note 6)$			33	ns
t _{PZH}	(DIR - A, B)	GL = Supr (Note 6)			33	ns
t _{PLZ}	Output disable time from low-level and high-level	O = 5-5 (N-4-6)			- 30	ns
t _{PHZ}	(OE - A, B)	C _L = 5pF (Note 6)			30	ns
t _{PZL}	Output enable time to low-level and high-level	0 - 50-5 (N-4-6)			33	ns
t _{PZH}	(OE - A, B)	C _L = 50pF (Note 6)			33	ns

MT4HC646P/FP/DWP

OCTAL 3-STATE NONINVERTING BUS TRANSCEIVER AND D-TYPE FLIP-FLOP

SWITCHING CHARACTERISTICS ($v_{cc} = 2\sim6V$, $T_a = -40\sim+85$ °C)

Symbol	Parameter	Test conditions			25℃	Limits	40-	+85°C	Unit
Symbol	Parameter	rest conditions	V _{CC} (V)	Min	Тур	Max	Min	Max	Unit
	· · · · · · · · · · · · · · · · · · ·		2.0	5	Typ	IVIAX	4	IVIAX	
	Maximum alack fraguency		4.5	27			21		MH
fmax	Maximum clock frequency		1	l	i		1		MIL
			6.0	32			25		└
			2.0			60		75	
t _{TLH}	Low-level to high-level and		4.5			12	1	15	ns
	high-level to low-level		6.0			10		13	
	ingi iotorio ioni iotor		2, 0			60	1	75	
t _{THL}	output transition time	C _L = 50pF (Note 6)	4.5			12		15	ns
	1		6.0			10		13	
			2.0			170		214	
t _{PLH}			4.5		ļ	34		43	ns
			6.0			29		36	
-	1		2.0			170		214	
t _{PHL}	Low-level to high-level and		4.5			34	1	43	ns
-PIIL	high-level to low-level		6.0			29		36	
	output propagation time		2.0		 	220	 	277	-
	(A - B, B - A)	,	4.5		ļ	44		55	
t _{PLH}	(A - B, B - A)		1	1		37	1	1	ns
	4	C _L = 150pF (Note 6)	6.0		-			47	<u> </u>
	1		2.0			220		277	1
t _{PHL}			4.5			44	[55	ns
			6.0			37		47	
			2.0	ĺ	1	220	1	277	1
t _{PLH}	*		4.5			44		55	ns
		C _L = 50pF (Note 6)	6.0		<u> - </u>	37		47	1
	1	CL — Sopr (Note 6)	2.0			220		277	
t _{PHL}	Low-level to high-level and		4.5		1	44		55	ns
	high-level to low-level		6.0			37		47	
	output propagation time		2.0			270		340	
t _{PLH}	(CKAB - B, CKBA - A)		4.5		1	54		68	ns
	() ()		6.0			46		58	
	•	C _L = 150pF (Note 6)	2.0			270	l	340	
•			4.5			54		68	ns
t _{PHL}	1		1		1	46	1	58	113
	<u> </u>		6.0					+	
	1		2.0	1	1	170		214	
t _{PLH}			4.5			34		43	ns
		C _L = 50pF (Note 6)	6.0	ļ		29		36	
			2.0		1 1	170		214	
t _{PHL}	Low-level to high-level and		4.5			34	'	43	ns
	high-level to low-level		6.0		<u> </u>	29		36	
	output propagation time		2.0			220		277	
t _{PLH}	(SAB - B, SBA - A)		4.5		1	44		55	ns
		0 = 150-5 (N-1-0)	6.0			37		47	
		$C_L = 150 pF (Note 6)$	2.0		1	220		277	
t _{PHL}			4.5			44		55	ns
	1		6.0]	1	37		47	
		<u> </u>	2.0		<u> </u>	175	 	221	
	Output disable time from		4.5			35		44	ns
t _{PLZ}	Output disable time from			1	1	30		37	ns
	low-level and high-level	C _L = 50pF (Note 6)	6.0		 				
			2.0		1	175		221	
t _{PHZ}	(DIR - A, B)		4.5			35		44	ns
	1		6.0			30		37	

SWITCHING CHARACTERISTICS ($V_{cc} = 2\sim 6V$, $T_a = -40\sim +85^{\circ}C$)

Karata Historia (n. 1904)

Symbol	Parameter	Test conditions			25℃	Limits	-40~	+85℃	Uni
Cymbol	raramoter	Tool conditions	V _{cc} (V)	Min	Тур	Max	Min	Max	0
			2.0		-34	175		221	
I _{PZL}			4.5		l	35		44	ns
			6.0		ĺ	30		37	
	1	C _L = 50pF (Note 6)	2.0			175		221	
PZH	Output enable time to low-level		4,5			35		44	ns
			6.0			30		37	
	and high-level		2.0			225		284	-
PZL	(DIR - A, B)		4.5			45		57	n:
			6.0		1	38		48	
	1 .	C _L = 150pF (Note 6)	2.0			225		284	-
t _{PZH}			4.5			45		57	n:
			6.0	,	} .	38		48	
			2.0			175		221	
PLZ	Output disable time from		4.5			35		44	n
			6.0			30		37	1
	low-level and high-level		2.0			175		221	
PHZ	(OE - A, B)		4.5)	35		44	n
	,	50 5 (1) (0)	6.0		ļ	30		37	
		$C_L = 50 pF (Note 6)$	2. 0			175		221	
PZL	I.		4.5			35		44	n:
			6.0			30		37	ļ
	1		2.0			175		221	
t _{PZH}	Output enable time to low-level		4.5		-	35		44	n
===			6.0			30		37	
	and high-level		2.0			225		284	
PZL	(OE - A, B)		4.5		(45		57	- n
		0 = 150 = 5'(N + + 0)	6.0			38		48	
	1	C _L = 150pF (Note 6)	2.0			225		284	
PZH			4.5			45		57	n:
			6.0]	1	38		48	
C ₁	Input capacitance		-			10		10	pl
Co	Off-state output capacitance	OE = V _{CC}				15		15	pl
C _{PD}	Power dissipation capacitance (Note 5)			I					pl

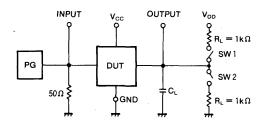
Note 5 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per flip flop)

The power dissipation during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS ($v_{cc} = 2\sim6v$, $T_a = -40\sim+85$ °C)

						Limits			
Symbol	Parameter	Test conditions			25℃		-40~	+85℃	Unit
		· ·	V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0	80			101		
tw	CK _{AB} , CK _{BA} pulse width		4.5	16	N.		20		ns
			6.0	14			17		
			2.0	100			125		
tsu	A, B setup time with		4.5	20		l	25		ns
	respect to CK _{AB} , CK _{BA}		6.0	17	i		21		
		1	2.0	0			0		
th	A, B hold time with		4.5	0			0		ns
	respect to CKAB, CKBA		6.0	0			0		

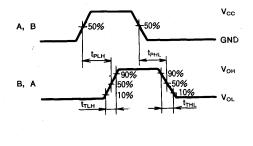
Note 6: Test Circuit

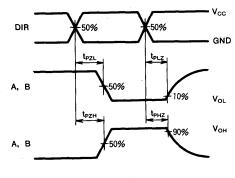


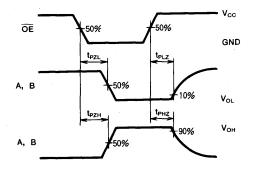
Parameter	SW 1	SW 2
t _{TLH} , t _{THL}	Open	Open
t _{PLZ}	Closed	Open
t _{PHZ}	Open	Closed
t _{PZL}	Closed	Open
t _{PZH}	Open	Closed

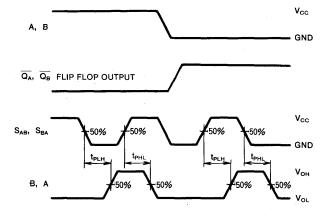
- (1) The pulse generator (PG) has the following characteristics (10%~90%): $t_{\rm f}=6{\rm ns},\,t_{\rm f}=6{\rm ns}$
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

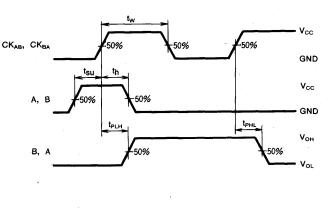
TIMING DIAGRAM













M74HC648P/FP/DWP

OCTAL 3-STATE INVERTING BUS TRANSCEIVER AND D-TYPE FLIP-FLOP

DESCRIPTION

The M74HC648 is a semiconductor integrated circuit consisting of eight bus transceivers with inverted outputs.

FEATURES

- High fon-out 3-state outputs (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 70MHz clock frequency typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC648 to maintain the low power dissipation and high noise margin of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS648.

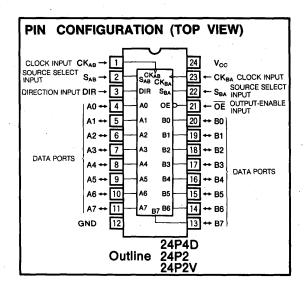
The M74HC648 consists of eight bidirectional buffers by interconnecting the I/O buffers of two D-type flip flops with 3-state inverted outputs. The I/O direction is controlled by output-enable input $\overline{\text{OE}}$ and direction input DIR. The signals are routed from input to output or from the flip flop to output by source select inputs S_{AB} and S_{BA} . The input signals are inverted when they appear at the output.

When \overline{OE} is low and DIR is high, the data ports A will become input terminals and the data ports B will become output terminals. When S_{AB} goes low, the inverted signal A, which was stored in flip flop (A) as Q_A when S_{AB} was high, appears at B. When SAB is held low and when clock input CK_{AB} changes from low to high, the signal present at A is stored in flip flop (A). When S_{AB} is held high and when CK_{AB} changes from low to high, the signal present at A is inverted and stored in flip flop (A). At the same time, the inverted signal $\overline{Q_A}$ which was stored in flip flop (A), appears at B.

When \overline{OE} and DIR are both low, the I/O direction is reversed: B will become input terminals and A will become output terminals. When S_{BA} goes low, and the inverted signal B, which was stored in flip flop (B) as Q_B when S_{BA} was high, appears at A. When S_{BA} is held low and clock input CK_{BA} changes from low to high, the signal present at B is stored in flip flop (B).

When S_{BA} is held high and CK_{BA} changes from low to high, the signal present at B is stored in flip flop (B). At the same time, the inverted signal $\overline{Q_B}$ which was stored in flip flop (B), appears at A.

When OE is high, both A and B will become high impe-



dance state and they will be separated. When CK_{AB} changes from low to high, the signal present at A is stored in flip flop (A). When CK_{BA} changes from low to high, the signal present at B is stored in flip flop (B).



FUNCTION TABLE (Note 1)

		Contro	inputs	5			Data	port	s	Flip	Flop	Operational description
OE	DIR	CKAB	CKBA	SAB	SBA		A	Ĺ	В	Q _A	Qв	Operational description
.H	Х	Х	Х	Х	Х		X		Х	Q _A ⁰	Q _B ⁰	The output of data ports A and B are disabled.
Н	Х	1	Х	Х	Х		L		X	Q _A ⁰	X	Data ports A and B are stored by the flip flops at the rising edge of
I	Х	1	X	X	X	ı	Н	1	_ X	Q _A ⁰	Х	CK _{AB} and CK _{BA} . The output of data ports A and B is disabled.
Н	Х	X	1	Х	Х	ļ	Х		L	X	Q _B ⁰	
Н	X	X	1	X	Х		X	<u> </u>	Н	X	Q _B ⁰	
L	Н	x	х*	L	x		L		н	Q _A ⁰	Q _B ⁰	The output of data port B is enabled. (Note 2) 1) When SAB is low, the data port A appears at data port B. The state
L	н	x	x*	L	×		Н		L	Q _A ^o	Q _B o	of the flip flop (A) is unchanged.
L	н	x	x*	н	×		×		Q _A °	Q _A ⁰	Q _B ⁰	2) When S _{AB} is high, the output of flip flop (A) appears at data port B.
L	Н	t	x*	L	х	1	L	0	н	Q _A ⁰	Q _B ⁰	3) When S _{AB} is low, the data port A appears at data port B and is
L	Н	1	х*	L	х		Н		L	Q _A ⁰	о _в	stored in flip flop (A) at the rising edge of CK _{AB} .
L	н	1	x*	Н	х		L		Q _A 0	Q _A ⁰	Q _B ⁰	 When S_{AB} is high, the data port A is stored in flip flop (A) at the rising edge of CK_{AB}, and the output of flip flop (A) appears at data port
L	Н	1	x*	н	×		н		Q _A 0	Q _A ⁰	Q _B °	B.
L	L	x*	x	x	L		н		L.	Q _A ⁰	Q _B ⁰	The output of data port A is enabled. (Note 3) 1) When S _{BA} is low, the data port B appears at data port A. The state
L	L	x*	х	x	L		L		н	Q _A ⁰	Q _B ⁰	of flip flop (B) is unchanged.
L	L	x*	x	×	н		Q _B o		×	Q _A º	Q _B ⁰	2) When S _{BA} is high, the output of flip flop (B) appears at data port A.
L	L	x*	t	Х	L	0	н	'	L	Q _A o	Q _B ⁰	3) When S _{BA} is low, the data port B appears at data port A and is
٦	L	x*	†	X	L.		L		н	Q _A ⁰	Q _B ⁰	stored in flip flop (B) at the rising edge of CK _{AB} .
L	L	х*	1	х	Н		Q _B ⁰		L	Q _A o	Q _B °	When S _{BA} is high, the data port B is stored in flip flop (B) and the output of flip flop (B) appears at data pout A.
L	L	х*	†	х	Н		Q _B °		Н	Q _A ⁰	Q _B ⁰	output of hip hop (b) appears at data pout A.

Note 1 : X

: Irrelevant

: Change from low to high

Q_A°, Q_B°: Output state of flip flops before the rising edge of CK_{AB} and CK_{BA}.

: Input terminal of data port

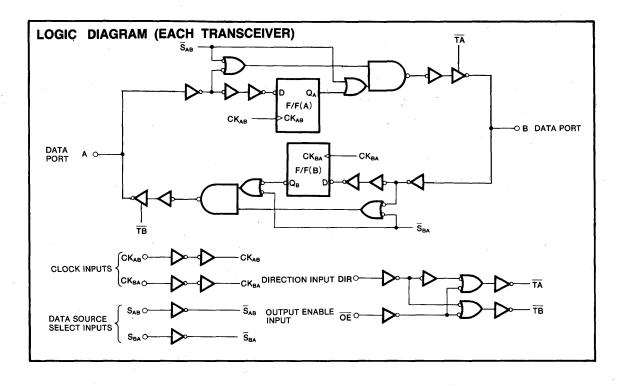
: Output terminal data port : As CKAB and CKBA are not selected by the I/O direction signal, data from data ports A and B can be stored in the corresponding

flip flops at the rising edge of CKAB or CKBA.

Note 2: The outnput at data port B is given by: $B = (\overline{A} \cdot \overline{S_{AB}}) + (\overline{Q_A} \cdot \overline{S_{AB}})$

Note 3: The output at data port B is given by:

 $A = (\overline{B} \cdot \overline{S_{BA}}) + (\overline{Q_B} \cdot S_{BA})$



ABSOLUTE MAXIMUM RATINGS $(T_a = -40 \sim +85 ^{\circ}C)$, unless otherwise noted)

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Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
	Innut protection died a curve t	V ₁ < 0V	-20	
lik	Input protection diode current	V _I > V _{CC}	20	mA
	0	V ₀ < 0V	-20	
lok	Output parasitic diode current	Vo > Vcc	20	mA
lo	Output current per output pin		±35	mA
Icc	Supply/GND current	V _{CC} , GND	±75	mA
Pd	Power dissipation	(Note 4)	500	mW
Tstg	Storage temperature range		−65~+150	°C

Note 4 : M74HC648FP, $T_a=-40\sim+80^\circ\text{C}$ and $T_a=80\sim85^\circ\text{C}$ are derated at -7mW/°C. M74HC648DWP, $T_a=-40\sim+80^\circ\text{C}$ and $T_a=80\sim85^\circ\text{C}$ are derated at -7mW/°C.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85 \degree C)$

Cumbal	Do			Limits					
Symbol	Pa	rameter	Min	Тур	Max	Unit			
Vcc	Supply voltage		2		6	٧			
V,	Input voltage		0		Vcc	٧			
Vo	Output voltage		0		Vcc	٧			
Topr	Operating temperature ra	ange	-40		+85	Ç			
		$V_{CC} = 2.0V$	0		1000				
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns			
		$V_{CC} = 6.0V$	0		400				



ELECTRICAL CHARACTERISTICS

							Limits			-
Symbol	Parameter	Test	conditions			25℃		-40~	+85℃	Unit
		V _{cc} (V)		Min	Тур	Max	Min	Max	'	
		$V_0 = 0.1V, V_{00}$	_0 1V	2.0	1.5			1.5		
VIH	High-level input voltage	$ V_0 = 0.1V, V_{CO} $;0.1 V	4.5	3. 15			3.15		V
·		1101 - 20μΑ	$I_0 \mid = 20\mu A$					4.2		
		V = 0.1V V	$V_0 = 0.1V, V_{CC} = 0.1V$				0.5		0.5	
VIL	Low-level input voltage	$ I_0 = 20\mu A$;-0.14	4.5			1.35		1.35	٧
		1101 - 20μΑ		6.0			1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
		**	$I_{OH} = -20\mu A$	4.5	4.4			4.4		
VoH	High-level output voltage	$V_{i} = V_{iH}, V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9			5. 9		V
		·	$I_{OH} = -6.0 \text{mA}$	4.5	4. 18			4.13		
			$I_{OH} = -7.8 \text{mA}$	6.0	5. 68			5.63		
			$I_{OL} = 20 \mu A$	2.0			0. 1		0.1	
			$I_{OL} = 20 \mu A$	4.5			0.1		0.1	
VoL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
			$I_{OL} = 6.0 \text{mA}$	4.5			0.26		0.33	
			I _{OL} = 7.8mA	6.0			0. 26		0.33	
l _{IH}	High-level input current	V _I = 6V		6.0			0.1		1.0	μA
I _{IL}	Low-level input current	V ₁ = 0V		6.0			-0.1		-1.0	μA
I _{OZH}	Off-state high-level output current	$V_i = V_{IH}, \ V_{IL}, \ V_O = V_{CC}$		6.0			0.5		5.0	μA
lozL	Off-state low-level output current	$V_i = V_{iH}, V_{iL}, V_{iL}$	6.0			-0.5		-5.0	μA	
Icc	Quiescent supply current	$V_{i} = V_{CC}$, GND	$I_0 = 0\mu A$	6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS $(v_{cc} = 5v, \tau_a = 25\%)$

Symbol	Parameter	Test conditions		Limits			
Symbol	raiameter	rest conditions	Min	Тур	Max	Unit	
fmax	Maximum clock frequency	C _L = 50pF (Note 6)	30			MHz	
t _{TLH}	Low-level to high-level and high-level to low-level			4	10	ns	
t _{THL}	output transition time				10	ns	
t _{PLH}	Low-level to high-level and high-level to low-level				30	ns	
t _{PHL}	output propagation time (A - B, B - A)	$C_1 = 50 \text{pF} \text{ (Note 6)}$			30	ns	
t _{PLH}	Low-level to high-level and high-level to low-level	CL = SUPF (Note 6)			40	ns	
t _{PHL}	output propagation time (CK _{AB} - B, CK _{BA} - A)				40	ns	
t _{PLH}	Low-level to high-level and high-level to low-level				30	ns	
t _{PHL}	output propagation time (S _{AB} - B, S _{BA} - A)				30	ns	
t _{PLZ}	Output disable time from low-level and high-level	C = F=F(N=4= C)			30	ns	
t _{PHZ}	(DIR - A, B)	$C_L = 5pF (Note 6)$			30	ns	
t _{PZL}	Output enable time to low-level and high-level	0 - 50-5 (N-4-0)			33	ns	
t _{PZH}	(DIR - A, B)	$C_L = 50 pF \text{ (Note 6)}$			33	ns	
t _{PLZ}	Output disable time from low-level and high-level	0 -5 5(0 . 0)			30	ns	
t _{PHZ}	(OE - A, B)	$C_L = 5pF (Note 6)$			30	ns	
t _{PZL}	Output enable time to low-level and high-level	0 50 5 (44 + 0)			33	ns	
t _{PZH}	(OE – A, B)	C _L = 50pF (Note 6)			33	ns	

SWITCHING CHARACTERISTICS $(V_{cc} = 2\sim6V, T_a = -40\sim+85^{\circ}C)$

क्ष्म रक्षेत्र होता वह तिहासको अने स्कूछका । अने होता हो स्कूछ । स्कूछका स्कूछका अने स्कूछका । अने होता होता होता होता होता होता है ।

Symbol	Parameter	Test conditions			25℃	Limits	-40~	-+85°C	Unit
Cymbol	T di dinotoi	rost containons	V _{cc} (V)	Min	Тур	Max	Min	Max	-
	 		2.0	5	.,,,,	····ux	4	IVIUA	
f _{max}	Maximum clock frequency		4.5	27			21		мна
·IIIax	material order (requeste)		6.0	32			25		''''
		2.0				60		75	
t _{TLH}	Low-level to high-level and	The state of the s	4.5			12	1	15	ns
TLH	Low-lover to high-lover and		6.0			10		13	113
	high-level to low-level		2.0			60	-	75	
t	output transition time	$C_L = 50 pF (Note 6)$	4.5			12		15	ns
t _{THL}	Calpat transition time	OE = SOPI (Note o)	6.0			10		13	110
			2.0	,		170	-	214	<u> </u>
			4.5			34		43	
t _{PLH}			6.0	İ		29	ł	36	ns
	-			<u> </u>					ļ
			2.0			170	1	214	
t _{PHL}	Low-level to high-level and		4.5			34		43	ns
	high-level to low-level		6.0			29	ļ.,	36	_
_	output propagation time		2.0			220		277	
t _{PLH}	(A-B, B-A)	·	4.5	ļ		44	ļ	55	ns
	_	C _L = 150pF (Note 6)	6.0			37		47	
			2.0	i		220		277	ł
t _{PHL}		[4.5	1	-	44		55	ns
			6.0			37		47	
			2.0			220		277	
t _{PLH}			4.5			44		55	ns
		C _L = 50pF (Note 6)	6.0			37		47	
		CL — SUPP (Note 6)	2.0			220		277	
t _{PHL}	Low-level to high-level and	· ·	4.5			44		55	ns
	high-level to low-level	•	6.0		i	37	İ	47	
	output propagation time		2.0			270		340	
t _{PLH}	(CKAB - B, CKBA - A)	*	4.5	1	}	54		68	ns
			6.0			46		58	
		C _L = 150pF (Note 6)	2.0			270		340	
t _{PHL}			4.5			54		68	ns
			6.0			46		58	
		· †	2.0			170	1	214	-
t _{PLH} .			4.5	1		34		43	ns
YPLH -			6.0			29		36	"
		C _L = 50pF (Note 6)	2.0	t	 	170	t	214	—
t _{PHL}	Low-level to high-level and		4.5			34		43	ns
PHL	high-level to low-level		6.0			29		36	"
	output propagation time	*	2.0			220	 	277	
			1			1			l
t _{PLH}	$(S_{AB}-B, S_{BA}-A)$		4.5			44		55	ns
	- ·	C _L = 150pF (Note 6)	6.0	 		37		47	ļ.
			2.0			220		277	
t _{PHL}			4.5			44	1 1	55	ns
			6.0	-	-	37	}	47	
			2.0			175		221	
t _{PLZ}	Output disable time from		4.5			35		44	ns
	low-level and high-level	C _L = 50pF (Note 6)	6.0			30		37	
•	IOTOI UIIU IIIGII-IOTOI	JE OOD (Hote O)	2.0			175		221	
t _{PHZ}	(DIR - A, B)		4.5			35		44	ns
			6.0			30		37	1.

SWITCHING CHARACTERISTICS ($v_{cc} = 2\sim6V$, $T_a = -40\sim+85^{\circ}C$)

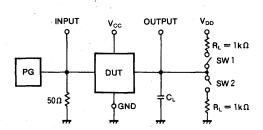
Symbol	Parameter	Test conditions			25℃	Limits	-40~	+85℃	Unit
Cymbol	T dramoter	Tool conditions	V _{CC} (V)	Min	Тур	Max	Min	Max	1
			2.0			175		221	
t _{PZL}			4.5			35		44	ns
TZL			6.0			30		37	
		$C_L = 50 pF (Note 6)$	2.0			175		221	
t _{PZH}	Output enable time to low-level		4.5			35		44	ns
72			6.0			30		37	
	and high-level		2.0			225		284	ļ. —
t _{PZL}	(DIR - A, B)		4.5			45		57	ns
			6.0			38		48	
	7	$C_L = 150 pF (Note 6)$	2. 0			225		284	
t _{PZH}		·	4.5			45		. 57	ns
		•	6.0			38		48	
			2.0			175		221	
tPLZ	Output disable time from		4.5		İ	35		44	ns
	at the state of th		6.0			30		37	
	low-level and high-level	-	2.0			175		221	
t _{PHZ}	(OE - A, B)		4.5			35		44	ns
		50 5 (1)	6.0		ļ	30		37	1
		$C_L = 50 pF (Note 6)$	2.0			175		221	
t _{PZL}			4.5			35		44	ns
			6.0			30	,	37	
		•	2.0			175		221	
t _{PZH}	Output enable time to low-level		4.5			35		44	ns
	1		6.0			30		37	Ì .
	and high-level		2.0			225		284	
t _{PZL}	(OE – A, B)		4. 5		,	. 45		57	ns
		0 = 150=5 (N-4= 6)	6.0			38		48	
	1	C _L = 150pF (Note 6)	2.0	,		225		284	
t _{PZH}			4. 5			45		57	ns
			6.0			38		48	
Cı	Input capacitance					10		10	pF
Co	Off-state output capacitance	ŌE = V _{CC}				15		15	рF
C _{PD}	Power dissipation capacitance (Note 5)								pF

Note 5 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per flip flop) The power dissipation during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS ($V_{cc} = 2\sim 6V$, $T_a = -40\sim +85$ °C)

						Limits			
Symbol	Parameter	Test conditions			25℃		-40~	+85℃	Unit
1.			V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0	80			101		
tw	CKAB, CKBA pulse width		4.5	16			20	}	ns
			6.0	14			17		
	A D - A - A - A - A - A - A - A - A - A		2.0	100			125		
t _{su}	A, B setup time with		4.5	20			25		ns
	respect to CK _{AB} , CK _{BA}		6.0	17		-	21		
	A D blad time a with		2.0	0			0		
th	A, B hlod time with		4.5	. 0			0		ns
	respect to CK _{AB} , CK _{BA}	· ·	6.0	0_			0		

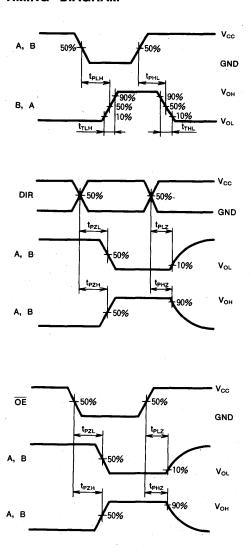
Note 6: Test Circuit

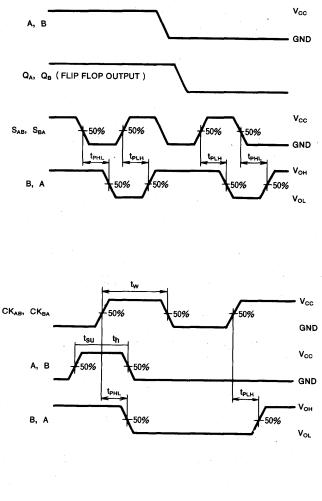


Parameter	SW1	SW 2
t _{TLH} , t _{THL}	Open	Open
t _{PLZ}	Closed	Open
t _{PHZ}	Open	Closed
t _{PZL}	Closed	Open
t _{PZH}	Open	Closed

(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
 (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM









M74HC669P/FP/DP

PRESETTABLE 4-BIT BINARY UP/DOWN COUNTER

DESCRIPTION

The M74HC669 is a semiconductor integrated circuit consisting of a 4-bit binary synchronous counter with up/down control and synchronous preset inputs.

FEATURES

- Up/down control and synchronous preset inputs
- Enable input and ripple-carry output allow cascade connection
- High-speed: 45 MHz clock frequency typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2∼6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

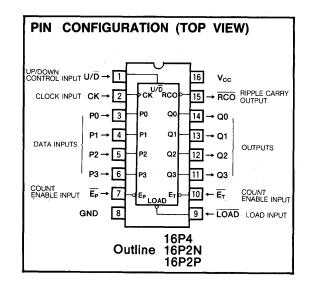
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC699 to maintain the low power dissipation and high noise margin of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS699.

The preset function, up/down control and enable function operate in synchronous with the rising edge of the clock. To preset the counter to a specific value, Load input $\overline{\text{LOAD}}$ is set to low-level and the corresponding data is applied to data inputs P0 through P3, the new count appears at outputs Q0 throgh Q3 in synchronous with the rising edge of the next clock input at CK.

Up/down control is possible when $\overline{\mathsf{LOAD}}$ is high-level and count enable inputs $\overline{\mathsf{E}_\mathsf{P}}$ and $\overline{\mathsf{E}_\mathsf{T}}$ are both low-level. The count increases when control input $\mathsf{U}/\overline{\mathsf{D}}$ is high-level, and



decreases when U/D is low-level.

The ripple carry output \overline{RCO} will become low when the count reaches 15 (1111₂) going up or 0 (0000₂) going down. $\overline{E_P}$, $\overline{E_T}$ and \overline{RCO} are used in cascade connections of the counter in synchronous from when the counter is used as a 2^n counter.

Counting is inhibited when \overline{LOAD} is high-level, and when either $\overline{E_P}$ or $\overline{E_T}$ is high-level.

FUNCTION TABLE (Note 1)

		Inputs			Outputs				
LOAD	Eρ	Ēτ	U/D	СК	Q0	Q1	Q2	Q3	RCO*
L	×	x	×	1	P0	P1	P2	P3	Н
Н	L	L	Н	1	Count up				Н
н	L	L	L	1		Count	down		. н
Н	н .	x	х	×		0			
Н	Х	н	Х	X		Count sp	peressed		Н

Note 1: † : Change from low to high

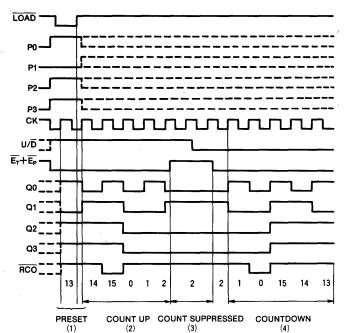
X : Irrelevant

*: RCO is normally high, but when $\overline{E_T}$ is low, the count is increasing, and Q0, Q1, Q2 and Q3 are high, then RCO will become low. It also will become low when the count is decreasing and Q0, Q1, Q2 and Q3 are low.

 $\frac{\overline{RCO} = \underline{Q0} \cdot \underline{Q1} \cdot \underline{Q2} \cdot \underline{Q3} \cdot (\underline{U/\overline{D}}) \cdot \overline{\underline{E_T}}}{\overline{RCO} = \underline{Q0} \cdot \underline{Q1} \cdot \underline{Q1} \cdot \underline{Q2} \cdot \underline{Q3} \cdot (\underline{U/\overline{D}}) \cdot \overline{\underline{E_T}}$

PRESETTABLE 4-BIT BINARY UP/DOWN COUNTER

TIMING DIAGRAM



TIMING DIAGRAM

- (1) Preset to 13(2) The count up sequence is 14, 15, 0, 1, 2
- (3) Count suppressed
- (4) The count down sequences is 1, 0, 15, 14, 13.



M74HC670P/FP/DP

4-BY-4 REGISTER FILE WITH 3-STATE OUTPUTS

DESCRIPTION

The M74HC670 is a semiconductor integrated circuit consisting of a 4-word by 4-bit register file with 3-state outputs.

FEATURES

- Independent inputs for read and write addresses allow simultaneous reading and writing.
- · Read-enable and output-control inputs
- High-speed: 21 ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=-40~+85℃
- 3-state outputs

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC670 to maintain the low power dissipation and high noise margin the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS670.

The M74HC670 has sixteen flip flops for storage and has discrete enable, address and output-enable inputs for both reading and writing. One word can be read while another is written enabling high-speed data transfer. The use of 3-state outputs enables "AND" ties.

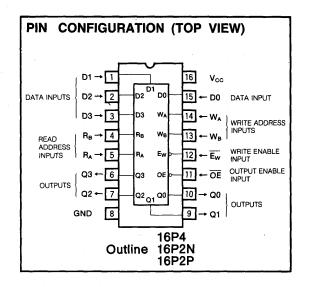
Writing method

By selecting a word using write address input WA and WB and applying date to the date inputs D0, D1, D2 and D3, writing into each bit is performed.

For writing the write-enable input \overline{EW} must be held low. When \overline{EW} is high, no date will be written.

Reading method

When a word is selected by read address inputs RA and RB, the contents of each bit appear at the outputs Q0, Q1, Q2 and Q3. For reading the output-enable input $\overline{\text{OE}}$ must be held low. When $\overline{\text{OE}}$ is high, all outputs will become high-impedance state irrespective of other inputs.



FUNCTION TABLE (Note 1) WRITTING FUNCTION

	Inputs			Outputs							
		=		Word							
WA	W _B	Ew	0	1	2	3					
×	Х	Н	Q°	Q°	Qº	Q°					
L	- L	L	Q=D	Qº	Q°	Q°					
Н	L	L	Q°	Q=D	Q٥	Q°					
L	Н	L	Q°	Qº	Q=D	Q°					
Н	Н	L	Qº	Q°	Qº	Q=D					

READING FUNCTION

	Inputs		Outputs					
RA	R _B	OE	Q0	Q1	Q2	Q3		
Х	Х	Н	Z	Z	Z	Z		
L	L	L	W ₀ B ₀	W ₀ B ₁	W ₀ B ₂	W ₀ B ₃		
н	L	L	W ₁ B ₀	W ₁ B ₁	W ₁ B ₂	W ₁ B ₃		
L	Н	L	W ₂ B ₀	W ₂ B ₁	W ₂ B ₂	W ₂ B ₃		
Н	Н	L	W ₃ B ₀	W ₃ B ₁	W ₃ B ₂	W ₃ B ₃		

ote 1: Q⁰: The contents of the word do not change.

Q=D : The input data is written to the specified word.

W_XB_Y : Word X bit Y X : Irrelevant Z : High impedance

M74HC688P/FP/DWP

8-BIT EQUALITY COMPARATOR

DESCRIPTION

The M74HC688 is a semiconductor integrated circuit consisting of an 8-bit digital comparator with a cascade input.

FEATURES

- High-speed: 28ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC},min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2∼6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

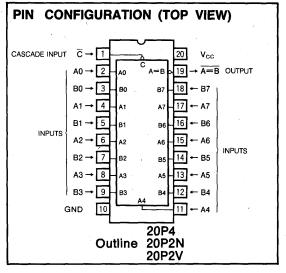
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC688 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS688.

When cascade input \overline{C} is low and two 8-bit binary A and B are applied to comparison inputs A0 \sim A7 and B0 \sim B7, the output $\overline{A=B}$ will become low when A=B and the output will become high when A>B or A<B.

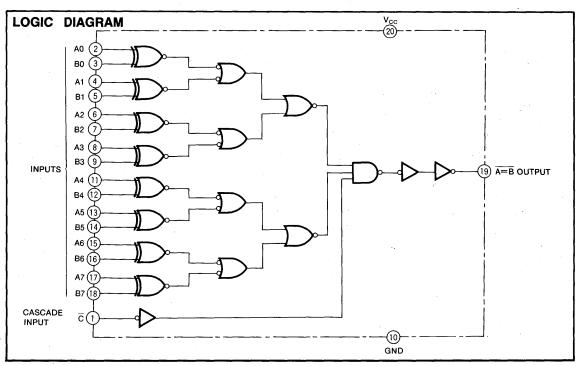
When \overline{C} is high, $\overline{A=B}$ will become high irrespective of A0 \sim A7 or B0 \sim B7.



FUNCTION TABLE (Note 1)

inp	Output		
A, B	A=B		
A=B	L	L	
A>B	A>B L		
A <b< td=""><td>L</td><td>Н</td></b<>	L	Н	
X	Н	Н	

Note 1: X: Irrelevant





MT4HC688P/FP/DWP

8-BIT EQUALITY COMPARATOR

ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85 \degree$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
	land and a single distance of	V ₁ < 0V	—20	
l _{IK}	Input protection diode current	$V_i > V_{CC}$	20	mA
	Output parasitic diode current	V ₀ < 0 V	-20	
lok		Vo > Vcc	20	mA
lo	Output current, per output pin		±25	mA
Icc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		-65~+150	°C

Note 2 : M74HC688FP, $T_a = -40 \sim +75 ^{\circ} C$ and $T_a = 75 \sim 80 ^{\circ} C$ are derated at -7 mW/C. M74HC688DWP, $T_a = -40 \sim +80 ^{\circ} C$ and $T_a = 80 \sim 85 ^{\circ} C$ are derated at -7 mW/C.

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85 \degree c)$

Symbol	Parameter		l	Unit		
	Pai	Min	Тур	Max	Unit	
Vcc	Supply voltage	2		6	٧	
V _I	Input voltage	0		V _{CC}	٧	
Vo	Output voltage	. 0		Vcc	V	
Topr	Operating temperature ra	-40		+85	°C	
	Input risetime, falltime	$V_{CC} = 2.0V$	0		1000	
t _r , t _f		$V_{CC} = 4.5V$	0		500	ns
	$V_{CC} = 6.0V$		0		400	

ELECTRICAL CHARACTERISTICS

			Test conditions $V_{\rm cc}(V)$		Limits					
Symbol	Parameter	Test			25℃			-40~+85°C		Unit
					Min	Тур	Max	Min	Max	ĺ
V _{IH} High-I		V = 0.1V V	$V_0 = 0.1V, V_{CC} = 0.1V$		1.5			1.5		
	High-level input voltage	$ I_0 = 20\mu A$;0.1 v	4.5	3.15			3, 15		V
		1101 - 20μΑ	$ I_0 = 20\mu A \qquad \qquad 6.0$		4.2			4. 2		
V _{IL} L	Low-level input voltage	V - 0 1V V	_0.1v	2.0			0.5		0.5	
			$V_0 = 0.1V, V_{CC} = 0.1V$ $ I_0 = 20\mu A$				1.35		1.35	: V
		1101 - 20μΑ					1.8		1.8	
	High-level output voltage	-	$I_{OH} = -20\mu A$	2.0	1.9			1.9		v
			$I_{OH} = -20\mu A$	4.5	4.4			4.4	1	
V _{OH}		$V_i = V_{iH}, V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		
			$I_{OH} = -4.0 \text{mA}$	4.5	4.18			4.13		
			$I_{OH} = -5.2 \text{mA}$	6. 0	5.68			5, 63		
-			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
	-	-	$i_{OL} = 20 \mu A$	4.5			0.1		0.1	
VoL	Low-level output voltage	$V_{l} = V_{lH}, V_{lL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
			$I_{OL} = 4.0 \text{mA}$	4.5			0.26		0.33	
			$I_{OL} = 5.2 \text{mA}$	6.0			0.26		0.33	ľ
J _{IH}	High-level input current	V ₁ = 6V	V ₁ = 6V				0.1		1.0	
l _{IL}	Low-level input current	$V_1 = 0V$	$V_1 = 0V$				-0.1		-1.0	μА
loc	Quiescent supply current	V = VCC, GND	$I_0 = 0 \mu A$	6.0			4.0		40.0	μΑ

8-BIT EQUALITY COMPARATOR

SWITCHING CHARACTERISTICS $(v_{cc} = 5v, \tau_a = 25^{\circ}C)$

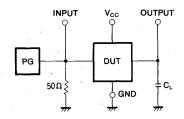
Symbol		7.4		Limits			
	Parameter	Test conditions	Min	Тур	Max	Unit	
tTLH	Low-level to high-level and high-level to low-level				10		
t _{THL}	output transition time		,		10	ns	
t _{PLH}	Low-level to high-level and high-level to low-level	C ₁ = 15pF (Note 4)			38		
t _{PHL}	output propagation time (A, B $-\overline{A=B}$)	C _L = 15pr (Note 4)			- 38	ns_	
t _{PLH}	Low-level to high-level and high-level to low-level	1			22	ns	
t _{PHL}	output propagation time (C - A=B)				22	118	

SWITCHING CHARACTERISTICS ($V_{cc} = 2\sim6V$, $T_a = -40\sim+85^{\circ}C$)

		Test conditions V _{CC} (V)		Limits					
Symbol	Parameter			25℃			-40~+85°C		Unit
				Min	Тур	Max	Min	Max	
			2.0			75		95	
1	Low-level to high-level and		4.5			15		19	
			6.0			-13	1	16	
	high-level to low-level		2.0	1		75		95	ns
t _{THL}	output transition time		4.5			15		19	Ì
			6.0			13		16	
		· ·	2.0			210		265	
t _{PLH}	Low-level to high-level and		4.5			42		53	
	high-level to low-level	0 50 5 (11 4 4)	6.0]		36		45	1
	output propagation time	C _L = 50pF (Note 4)	2.0			210		265	ns
t _{PHL}	(A, B — A=B)		4.5			42	1	53	
	1		6.0			36		45	
			2.0			120		151	
t _{PLH}	Low-level to high-level and		4.5			- 24		30	
	high-level to low-level		6.0			20		26	
	output propagation time		2.0		-	120		151	ns
t _{PHL}	$(\overline{C} - \overline{A = B})$	1	4.5			24	1	30	
		•	6.0			20	100	26	
Cı	Input capacitance					10		10	pF
CPD	Power dissipation capacitance (Note 3)				32				pF

Note 3 : CPD is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$

Note 4: Test Circuit

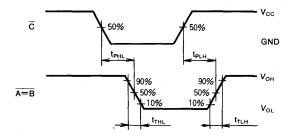


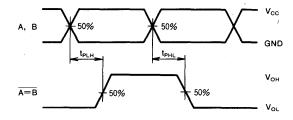
⁽¹⁾ The pulse generator (PG) has the following characteristics (10% \sim 90%): $t_r = 6ns$, $t_f = 6ns$ (2) The capacitance C_L includes stray wiring

capacitance and the probe input capacitance.

MT4HC688P/FP/DWP

8-BIT EQUALITY COMPARATOR





MITSUBISHI HIGH SPEED CMOS

M74HC4002P/FP/DP

DUAL 4-INPUT POSITIVE NOR GATE

DESCRIPTION

The M74HC4002 is a semiconductor integrated circuit consisting of two 4-input positive-logic NOR gates, usable as negative-logic NAND gates.

FEATURES

- High-speed: 10ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC4002 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the LSTTL.

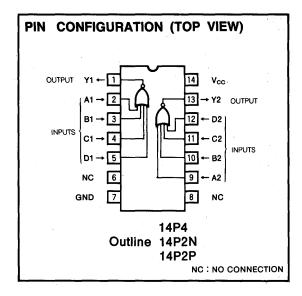
Buffered outputs Y improve input-to -output transfer characteristics and reduce to a minimum output impedance variations with respect to input voltage variations.

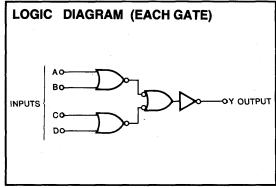
When all inputs A, B, C and D are low, the output Y will become high, and when at least one of the inputs is high, the output Y will become low.

FUNCTION TABLE

Inp	uts	Output
Α	N	Υ
L	L L	Н
Н	L	L
L	Н	L
Н	Н	L

N = B + C + D





ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85^{\circ}$ C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
	Input protection diode current	V ₁ < 0V	-20	
lικ		V _I > V _{CC}	20	mA
	0.44	V ₀ < 0V	-20	
Ток	Output parasitic diode current	$V_0 > V_{CC}$	20	mA
lo	Output current per output pin		±25	mA
Icc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65 ~ +150	င

Note 1 : M74HC4002FP, $T_a = -40 \sim +60 ^\circ$ and $T_a = 60 \sim 85 ^\circ$ are derated at $-6 mW/^\circ$ C. M74HC4002DP, $T_a = -40 \sim +50 ^\circ$ and $T_a = 50 \sim 85 ^\circ$ C are derated at $-5 mW/^\circ$ C.



M74HC4002P/FP/DP

DUAL 4-INPUT POSITIVE NOR GATE

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85^{\circ}C)$

Symbol		rameter		Unit		
Symbol	Fa	rameter	Min	Тур	Max	Unit
Vcc	Supply voltage	2		6	٧	
Vı	Input voltage		0		V _{CC}	V
V _o	Qutput voltage		0		Vcc	٧
Topr	Operating temperature ra	ange	-40		+85	°C
		$V_{CC} = 2.0V$	0		1000	
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns
	$V_{CC} = 6.0V$		0		400	1

ELECTRICAL CHARACTERISTICS

							Limits			
Symbol	Parameter	Test	conditions		25℃			-40~+85℃		Unit
	· ·		V _{cc} (V)		Min	Тур	Max	Min	Max	
		$V_0 = 0.1V$		2.0	1.5			1.5		
V _{IH}	High-level input voltage	1 -		4.5	3.15			3.15		V
		$ 1_0 = 20\mu\text{A}$	$ I_0 = 20\mu A$		4.2			4.2		
		V - 0 1V V	0.11/	2.0			0.5		0.5	
VIL	Low-level input voltage	$V_0 = 0.1V, V_{CC}$	5—0.1 V	4.5			1.35		1.35	V
		$ I_0 = 20\mu A$		6.0			1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
			$I_{OH} = -20\mu A$	4.5	4.4			4.4		
VoH	High-level output voltage	$V_I = V_{IL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		V
	1		$I_{OH} = -4.0 \text{mA}$	4.5	4.18			4.13		
			$I_{OH} = -5.2 \text{mA}$	6.0	5.68		-	5. 63		
			$I_{OL} = 20\mu A$	2.0			0.1		0.1	
		. [$I_{OL} = 20 \mu A$	4.5			0.1		0.1	
VoL	Low-level output voltage	$V_{l} = V_{lH}, V_{lL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
			I _{OL} = 4.0mA	4.5			0.26		0.33	
			$I_{OL} = 5.2 \text{mA}$	6.0			0.26		0.33	1
I _{IH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μA
IIL	Low-level input current	V _I = 0V		6.0	-		-0.1	-	-1.0	μΑ
loc	Quiescent supply current	Vi = Vcc, GND	$I_0 = 0 \mu A$	6.0			1.0		10.0	μА

DUAL 4-INPUT POSITIVE NOR GATE

SWITCHING CHARACTERISTICS (Voc = 5V, Ta = 25°C)

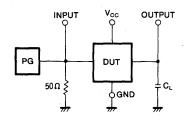
Symbol	Paramata.	Test conditions		Limits		Unit
Symbol	Parameter	rest conditions	Min	Тур	Max	Unit
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
tTHL	output transition time	0 - 15-5 (N-1-2)			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = 15pF (Note 3)			20	ns
t _{PHL}	output propagation time				20	ns

SWITCHING CHARACTERISTICS ($V_{cc} = 2\sim 6V$, $T_a = -40\sim +85^{\circ}C$)

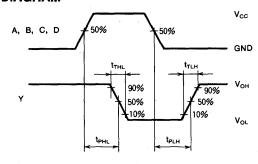
						Limits				
Symbol	Parameter	Test conditions			25℃		-40~	+85°C	Unit	
				Min	Тур	Max	Min	Max		
			2.0			75		95		
t _{TLH}	Low-level to high-level and		4.5			15	1	19	ns	
			`6.0			13		16		
	high-level to low-level		2.0			75		95		
t _{THL}	output transition time		4.5			15		19	ns	
		50 7 (01 + 0)	6.0			13	,	- 16		
		C _L = 50pF (Note 3)	2.0			120		151		
t _{PLH}	Low-level to high-level and		4.5			24		30	ns	
			6.0			20	1	26		
	high-level to low-level		2.0			120		151		
t _{PHL}	output propagation time		4.5			24		30	ns	
			6.0	'		20		26	!	
Cı	Input capacitance			•		10		10	ρF	
C _{PD}	Power disipation capacitance (Note 2)				31				pF	

Note 2: C_{PD} is the internal capacitance of the IC calculated from the operation supply current under no-load conditions. (per gate) The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$

Note 3: Test Circuit



- (1) The pulse generator (PG) has the following characteristics (10%~90%): $t_r = 6$ ns, $t_f = 6$ ns
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.





MITSUBISHI HIGH SPEED CMOS

M74HC4017P/FP/DP

DECADE COUNTER/DIVIDER

DESCRIPTION

The M74HC4017 is a semiconductor integrated circuit consisting of a decimal counter with direct reset input and decode output.

FEATURES

- High-speed: (clock frequency)40MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2∼6V
- Wide operating temperature range: T_a=-40~+85℃

APPLICATION

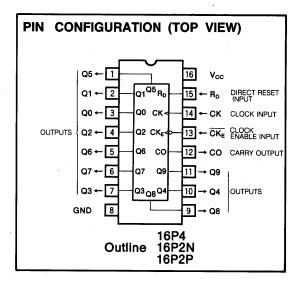
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC4017 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS4017.

The M74HC4017 is a decade Johnson counter with decoded outputs, in which only one output is high at any time, the other outputs remaining at low.

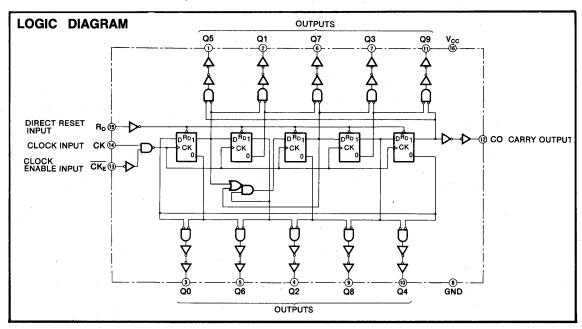
When clock enable input $\overline{CK_E}$ and direct reset input R_D are both held low, a pulse is applied to clock input CK, one output of Q0 through Q9 which corresponds to the number of counting pulses will become high. Counting takes place when CK changes from low-level to high-level.



When R_D is held low and CK is high, a clock pulse is applied to $\overline{CK_E}$, one output of Q0 through Q9 which corresponds to number of counting pulses will become high. Counting take place when $\overline{CK_E}$ changes from high-level to low-level

When $R_{\rm D}$ is high, Q0 and carry-output CO both will become high, and Q1 through Q9 will become low, irrespective of other inputs.

When Q0 through Q4 are high, CO will become high, and when Q5 through Q9 are high, CO will become low, providing an output wavefrom with a 50% duty cycle.



FUNCTION TABLE (Note 1)

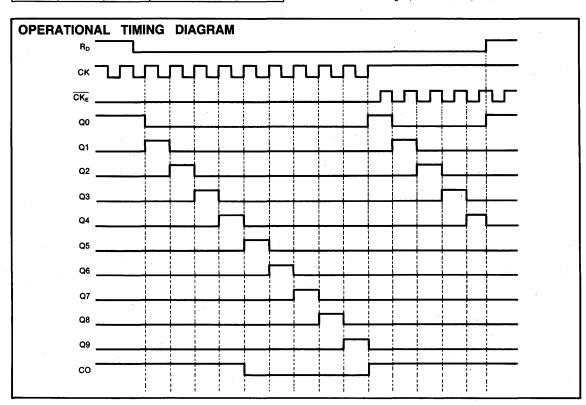
, II	nputs		List lavel systems win
	CKE	R _D	High-level output pin
	Х	Н	Q0
	Н	L	0-
	X	L	Qn
	L	L	Qn+1 (Counter operation)
	Н	L	
	Х	L]
	Ť	L	Qn
	ţ	L	
	1	L	Qn+1 (Counter operation)

Note 1 : X : Irrelevant

Qn: Indicates output pin which is high before the input con-

dition is set.

n : 0 through 9, but when n is 9, Qn+1 becomes Q0.



ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85 ^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
		V ₁ < 0V	-20	
I _{IK}	Input protection diode current	$V_{I} > V_{CC}$	20	mA
	Output acresitie diede current	V ₀ < 0V	-20	
lok	Output parasitic diode current	V _o > V _{cc}	20	mA
lo	Output current per output pin		±25	mA
l _{cc}	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65 ~ +150	င

Note 2 : M74HC4017FP, $T_a = -40 \sim +70 ^\circ$ and $T_a = 70 \sim 85 ^\circ$ are derated at $-6 mW/^\circ$. M74HC4017DP, $T_a = -40 \sim +50 ^\circ$ and $T_a = 50 \sim 85 ^\circ$ are derated at $-5 mW/^\circ$.



RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85\%)$

Symbol	Do	Parameter		Limits				
Symbol	га	rameter	Min	Тур	Max	Unit		
Vcc	Supply voltage	Supply voltage			6	V		
Vı	input voltage		0	_	Vcc	V		
Vo	Output voltage	0		Vcc	V			
Topr	Operating temperature ra	ange	-40		+85	ဗ		
		$V_{CC} = 2.0V$	0		1000			
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns		
		$V_{CC} = 6.0V$	0		400			

ELECTRICAL CHARACTERISTICS

							Limits			
Symbol	Parameter	Test	conditions	*	25℃			-40~+85℃		Unit
			V _{CC} (V)		Min	Тур	Max	Min	Max]
1		V = 0.1V V	0.11/	2.0	1.5			1.5		
VIH	High-level input voltage	1 2 7 2	$V_0 = 0.1V$, $V_{CC} - 0.1V$ $ I_0 = 20\mu A$		3.15			3.15		V
	1	1101 - 20µA		6.0	4.2			4.2		
		$V_{O} = 0.1V, V_{CO}$	_0.11/	2.0			0.5		0.5	
VIL	Low-level input voltage	$ V_0 = 0.1V, V_{CO} $ $ I_0 = 20\mu A$		4.5			1.35		1.35	V
	$ 1_0 = 20\mu A$	$ 10 = 20\mu A$				1.8		1.8		
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
		$I_{OH} = -20\mu A$	4.5	4. 4			4.4			
V _{OH}	High-level output voltage	$V_{I} = V_{IH}, V_{IL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		v
			$I_{OH} = -4.0 \text{mA}$	4.5	4.18			4.13		
			$I_{OH} = -5.2 \text{mA}$	6.0	5. 68			5. 63		
			$I_{OL} = 20 \mu A$	2.0			0.1		0. 1	
			$I_{OL} = 20 \mu A$	4.5			0.1		0.1	
VoL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
			I _{OL} = 4.0mA	4.5			0.26		0.33	· ·
			$I_{OL} = 5.2 \text{mA}$	6.0			0.26		0.33	
I _{IH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μА
I _{IL}	Low-level input current	$V_i = 0V$		6.0			0.1		-1.0	μA
Icc	Quiescent supply current	VI = VCC, GND	$I_0 = 0 \mu A$	6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS $(V_{cc} = 5V, T_a = 25^{\circ}C)$

Sumbol	Parameter	Tost conditions		11-14		
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
fmax	Maximum clock frequency		30			MHz
t⊤∟H	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time				10	ns
t _{PLH}	Low-level to high-level and high-level to low-level				40	ns
t _{PHL}	output propagation time (CK - Q)				40	ns
t _{PLH}	Low-level to high-level and high-level to low-level				40	ns
t _{PHL}	output propagation time (CK - CO)				40	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = 15pF (Note 4)			40	ns
t _{PHL}	output propagation time (R _D - Q)				40	ns
t _{PLH}	Low-level to high-level output propagation time (R _D - CO)				40	ns
t _{PLH}	Low-level to high-level and high-level to low-level				44	ns
t _{PHL}	output propagation time ($\overline{CK_E}$ — Q)				44	ns
t _{PLH}	Low-level to high-level and high-level to low-level	7			44	ns
t _{PHL}	output propagation time (CK _E - CO)				44	ns

SWITCHING CHARACTERISTICS ($v_{cc} = 2\sim6v$, $\tau_a = -40\sim+85$ °C)

						Limits	г		4
Symbol	Parameter	Test conditions			25℃		-40~	+85°C	Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0	4			3		
fmax	Maximum clock frequency		4.5	20			16		МН
			6.0	24			- 19		
		1 .	2.0			75		95	
t _{TLH}	Low-level to high-level and		4.5			15		19	ns
·ILH	Low lover to mgn lover and		6.0			13		16	"
	high-level to low-level		2.0			75		95	
	autout transition time		4.5		1	15		19	
t _{THL}	output transition time		1			1			ns
	<u> </u>		6.0			13	ļ	16	1
			2.0			230		290	
t _{PLH}	Low-level to high-level and		4.5			46		58	ns
	high-level to low-level		6.0			39		49	<u> </u>
	output propagation time		2.0			230		290	
t _{PHL}	(CK - Q)		4.5			46		58	ns
			6.0			39		49	
		1	2.0			230		290	
t _{PLH}	Low-level to high-level and		4.5			46		58	ns
4FER	high-level to low-level		6.0		1	39		49	
	output propagation time		2.0			230		290	1
	(CK - CO)		4.5			46		58	
t _{PHL}	(CK = CO)	· ·	1			1			ns
		C _L = 50pF (Note 4)	6.0			39		49	ļ
			2.0			230		290	1
t _{PLH}	Low-level to high-level and		4.5			46	'	58	ns
·	high-level to low-level		6.0			39		49	
	output propagation time		2.0			230		290	
t _{PHL}	$(R_D - Q)$		4.5			46		58	ns
			6.0			39		49	
	Low-level to high-level	· ·	2.0	-		230		290	
t _{PLH}	output propagation time		4.5			46		58	ns
	(R _D - CO)		6.0			39		49	
		† .	2.0			250		315	1
t _{PLH}	Low-level to high-level and		4.5			50		63	ns
-PLN	high-level to low-level		6.0			43		54	"
	output propagation time		2.0			250		315	
			4.5			50		63	
t _{PHL}	(CKE - Q)								ns
		4	6.0			43		54	
			2.0			250		315	
t _{PLH}	Low-level to high-level and		4.5			50		63	ns
	high-level to low-level		6.0			43		54	
	output propagation time		2.0		1	250		315	
t _{PHL}	(CK _E - CO)		4.5		-	50		63	ns
			6.0			43		54	1
Cı	Input capacitance		-			10		10	ρF
C _{PD}	Power dissipation capacitance (Note 3)		1			1	†	 	pF

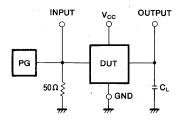
Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipation during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$



TIMING	REQUIREMENTS ($V_{cc} = 2\sim 6V$, $T_a = -40\sim +85^{\circ}$ C)
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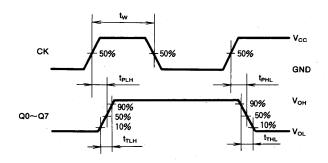
				Limits					
Symbol	Parameter	Test conditions		25℃			-40~+85℃		Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0	80			101		
tw	CK, CK _E , R _D pulse width		4.5	16			20		ns
			6.0	14			17		
	CK _E setup time with		2.0	50			63		
tsu	respect to CK		4.5	10			13		ns
	respect to CK		6.0	9			11		
	CK setup time with		2. 0	50			63		
t _{su}	respect to CK _E		4.5	10			13		ns
	respect to CKE		6.0	9			11		l
	CK _E hold time with		2.0	50			63		
· t _h	respect to CK		4.5	10			13		ns
	respect to CK		6.0	9	1		11		
	CK hold time with		2.0	50			63		
th	respect to CK _E	•	4.5	10			.13		ns
	respect to CKE		6.0	9			11		
	D. recovery time with		2.0	100			126		
trec	R _D recovery time with respect to CK		4.5	20			25		ns
	respect to CK		6.0	17			21		
	R _D recovery time with		2.0	100			126		
trec	respect to CK _E		4.5	20			25		ns
	Lesbect to CVE		6.0	17			21		

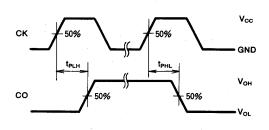
Note 4: Test Circuit



- (1) The pulse generator (PG) has the following
- characteristics (10%~90%): t_f = 6ns, t_f = 6ns

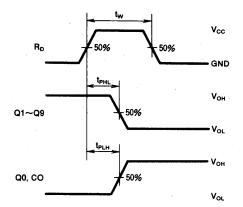
 (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

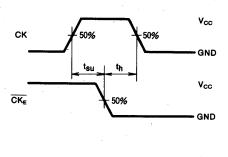


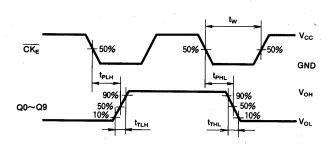


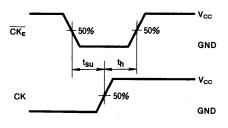
M74HC4017P/FP/DP

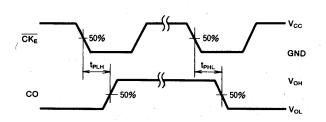
DECADE COUNTER/DIVIDER

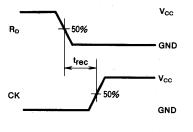


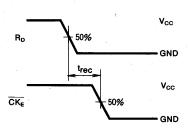














MITSUBISHI HIGH SPEED CMOS

M74HC4020P/FP/DP

14-STAGE BINARY RIPPLE COUNTER

DESCRIPTION

The M74HC4020 is a semiconductor integrated circuit consisting of an asynchronous 14-stage binary counter with a direct reset input.

FEATURES

- High-speed: (clock-frequency) 40MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2∼6V
- Wide operating temperature range: T_a=−40~+85°C

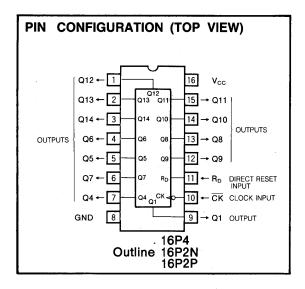
APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC4020 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to LSTTL. The M74HC4020 contains a 14-stage master-slave flip-flop with independent outputs Q1 and Q4~Q14 at each flip-flop. When operated as a counter, the direct reset input R_D should be held low and a clock pulse applied at clock input $\overline{\text{CK}}$.

Counting takes place when $\overline{\text{CK}}$ changes from high-level to low-level. When R_D is set high, all flip-flops will be cleared



and all outputs Q1 and Q4 \sim Q14 will become low irrespective of $\overline{\text{CK}}$.

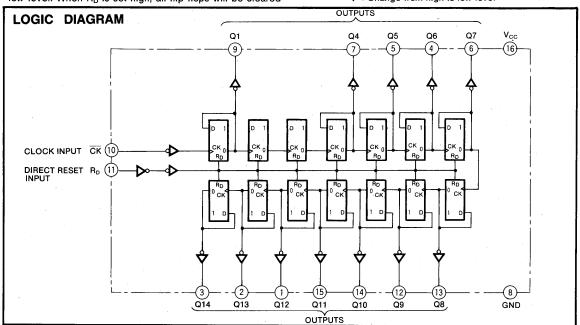
FUNCTION TABLE (Note 1)

Inp	uts	0.45.4
CK	R _D	Output state
×	Н	All outputs are low-level
Ť	L	No change
1	L	Advance counter

Note 1: X: Irrelevant

† : Change from low to high level

† : Change from high to low level



ABSOLUTE MAXIMUM RATINGS ($\tau_a = -40 \sim +85^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
	Input protection diede current	V ₁ < 0V	-20	
lik	Input protection diode current $V_i > V_{CC}$	V _I > V _{CC}	20	mA
	Contract and a second s	V ₀ < 0V	-20	
Іок	Output parasitic diode current	Vo > Voc	20	mA
lo	Output current per output pin		±25	mA
Icc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	°C

Note 2 : M74HC4020FP, $T_a = -40 \sim +70^{\circ}\text{C}$ and $T_a = 70 \sim 85^{\circ}\text{C}$ are derated at -6mW/C. M74HC4020DP, $T_a = -40 \sim +50^{\circ}\text{C}$ and $T_a = 50 \sim 85^{\circ}\text{C}$ are derated at -5mW/C.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85^{\circ}C)$

0	Parameter			Limits				
Symbol			Min	Тур	Max	Unit		
Vcc	Supply voltage		2		6	V		
V _I	Input voltage		0		Vcc	٧		
Vo	Output voltage		0		V _{CC}	٧		
Topr	Operating temperature ra	ange	—40		+85	င		
		V _{CC} = 2.0V	0		1000			
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns		
	$V_{CC} = 6.0V$		0		400			

ELECTRICAL CHARACTERISTICS

		1 .			Limits					Unit
Symbol	Parameter	Test	Test conditions $V_{CC}(V)$		25°C			-40~+85℃		
					Min	Тур	Max	Min	Max	1
		V = 0.1V V	0.11/	2.0	1.5			1.5		
V _{IH}	High-level input voltage		$V_0 = 0.1V, V_{CC} - 0.1V$ $ I_0 = 20\mu A$		3. 15			3. 15		v
		$ 1_0 = 20\mu\text{A}$			4.2			4.2		
		V = 0.1V V	0.11/	2.0			0.5		0.5	
VIL	Low-level input voltage	$ V_0 = 0.1V, V_{C} $ $ I_0 = 20\mu A$	C-0. 1 V	4.5			1.35		1.35	v
		$ I_0 = 20\mu A$		6.0			1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
		$I_{OH} = -20\mu A$	4.5	4.4			4.4			
V _{OH}	High-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		l v
			$I_{OH} = -4.0 \text{mA}$	4.5	4.18			4.13		
	1		$i_{OH} = -5.2 \text{mA}$	6.0	5. 68	-		5.63		
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
			$I_{OL} = 20 \mu A$	4.5			0.1		0.1	
VoL	Low-level output voltage	$V_{I} = V_{IH}, V_{IL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
			I _{OL} = 4.0mA	4.5			0.26		0.33	
		$I_{OL} = 5.2 \text{mA}$	6.0			0.26		0.33		
l _{iH}	High-level input current	V _I = 6V		6.0			0.1		1.0	μA
l _{IL}	Low-level input current	V ₁ = 0V		6.0			-0.1		-1.0	μF
Icc	Quiescent supply current	VI = VCC, GNE	$I_0 = 0\mu A$	6.0			4.0		40.0	μΑ

SWITCHING CHARACTERISTICS ($v_{cc} = 5v$, $T_a = 25^{\circ}C$)

O	D	T4 dist	Limits			Unit
Symbol	Parameter	Test conditions	Min	Тур	Max	UIII
fmax	Maximum clock frequency		30			MHz
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time	·			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = 15pF (Note 4)			35	ns
t _{PHL}	output propagation time (CK - Q1)				35	ns
	High-level to low-level output propagation time				40	
t _{PHL}	(R _D - Q1, Q4~Q14)				40 .	ns

SWITCHING CHARACTERISTICS ($V_{cc} = 2\sim6V$, $T_a = -40\sim+85$ °C)

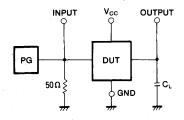
,	1	Parameter Test conditions							
Symbol	Parameter			25℃			-40~+85℃		Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	l
			2.0	4			3		
fmax	Maximum clock frequency		4.5	20			16		MHz
			6.0	24			19		
,			2.0			75		95	
t _{TLH}	Low-level to high-level and	· ·	4.5			15		19	ns
	high lavel to lave lavel		6.0			13		16	
	high-level to low-level		2.0			75		95	
t _{THL}	output transition time		4.5			15		19	ns
		C _L = 50pF (Note 4)	6.0			13		16	
		CL — SUPP (Note 4)	2.0			210		265	
t _{PLH}	Low-level to high-level and		4.5			. 42		. 53	ns
	high-level to low-level		6.0			36		45	
	output propagation time		2.0			210		265	
t _{PHL}	(CK – Q1)		4.5			42		53	ns
		·	6.0			36		45	
	High-level to low-level		2.0			240		302	1
t _{PHL}	output propagation time		4.5			48		60	ns
	(R _D — Q1, Q4~Q14)		6.0			41		51	
Ci	Input capacitance				1.5	10		10	pF
C _{PD}	Power dissipation capacitance (Note 3)								pF

Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot v_{CC}^2 \cdot f_i + I_{CC} \cdot v_{CC}$

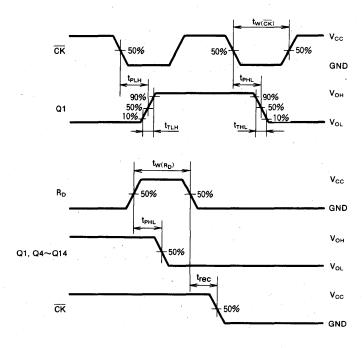
TIMING REQUIREMENTS ($v_{cc} = 2\sim 6V$, $T_a = -40\sim +85^{\circ}C$)

			,		Limits				
Symbol	Symbol Parameter	Test conditions		25℃			-40~+85°C		Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	
		2.0	80			101			
tw	CK, R _D pulse width		4.5	16			20		ns
			6.0	14			17		
			2.0	100			126		
trec	R _D recovery time with		4.5	20			25		ns
	respect to CK	,	6.0	17			21		

Note 4: Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%∼90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.







MITSUBISHI HIGH SPEED CMOS

M74HC4022P/FP/DP

OCTAL COUNTER/DIVIDER

DESCRIPTION

The M74HC4022 is a semiconductor integrated circuit consisting of an octal counter with reset input and decode output.

FEATURES

- High-speed: (clock frequency)40MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: Ta=−40~+85°C

APPLICATION

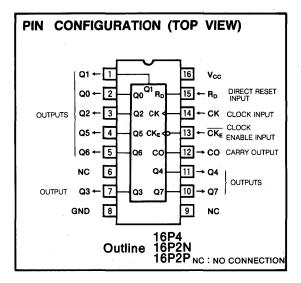
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC4022 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS4022.

The M74HC4022 is an octal Johnson counter with a decodered outputs, in which only one output in high at any time, the other outputs remaining at low.

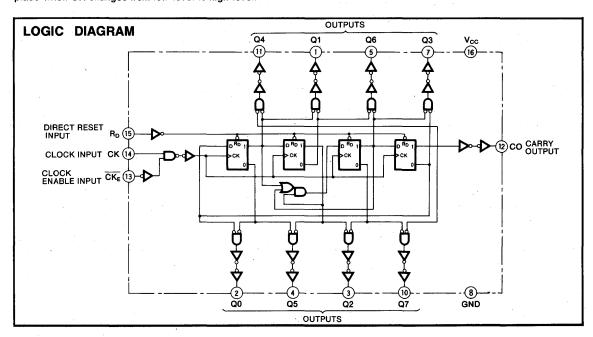
When clock enable input $\overline{CK_E}$ and direct reset input R_D are both held low, a clock pulse is applied to clock input CK, one output of Q0 through Q7 which corresponds to the number of counting pulses will become high. Counting takes place when CK changes from low-level to high-level.



When R_D is held low and CK is high, a clock pulse is applied to $\overline{CK_E}$, one output of Q0 though Q7 which corresponds to the number of counting pulses will become high. Counting takes place when $\overline{CK_E}$ changes from high-level to low-level.

When R_{D} is high, Q0 and carry-output CO will become high, and Q1 through Q7 will become low, irrespective of other inputs.

When Q0 through Q3 are high, CO will become high, and when Q4 through Q7 are high, CO will become low, providing an output wavefrom with a 50% duty cycle.



OCTAL COUNTER/DIVIDER

FUNCTION TABLE (Note 1)

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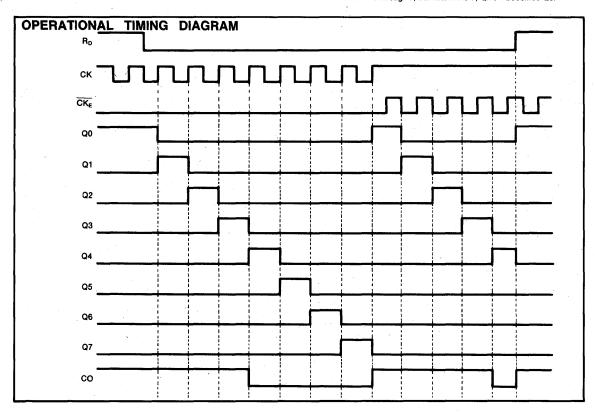
	Inputs		Allah Jawal autout nin
СК	CKE	R₀	High-level output pin
Х	Х	Н	Q0
×	Н	L	0-
L	Χ.	L	Qn
†	L	L	Qn+1 (Counter operation)
†	H	L	
↓	L	Ĺ	1
Х	<u>†</u>	L	Qn
L	Į.	L]
Н	1	L	Qn+1 (Counter operation)

Note 1: X : Irrelevant

† : Change from low to high : Change from high to low

Qn: Indicates output pin which is high before the input condition is set.

n : 0 through 7, but when n is 7, Qn+1 becomes Q0.



ABSOLUTE MAXIMUM RATINGS $(T_a = -40 \sim +85 ^{\circ}C)$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
	Input protection diode current	V₁ < 0V	-20	
l _{IK}		$V_1 > V_{CC}$	20	mA
		v _o < 0v	-20	
Гок	Output parasitic diode current	$V_{o} > V_{cc}$	20	mA
lo	Output current per output pin		±25	mA
loc T	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		-65~+150	°C

Note 2 : M74HC4022FP, $T_a=-40\sim+70^\circ\text{C}$ and $T_a=70\sim85^\circ\text{C}$ are derated at $-6\text{mW}/^\circ\text{C}$. M74HC4022DP, $T_a=-40\sim+50^\circ\text{C}$ and $T_a=50\sim85^\circ\text{C}$ are derated at $-5\text{mW}/^\circ\text{C}$.



OCTAL COUNTER/DIVIDER

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85 \degree c)$

Cumbal	Parameter			11-14		
Symbol	, Pa	Min	Тур	Max	Unit	
V _{CC}	Supply voltage		2		6	V
V _i	Input voltage		0		Vcc	٧
Vo	Output voltage		0		Vcc	V
Topr	Operating temperature ra	ange	-40		+85	င
	Input risetime, falltime	V _{CC} = 2.0V	0		1000	ns
t _r , t _f		$V_{CC} = 4.5V$	0		500	
	$V_{CC} = 6.0V$		0		400	

ELECTRICAL CHARACTERISTICS

							Limits			
Symbol	Parameter	Test	conditions			25℃		-40~	+85℃	Unit
			V _{cc} (v)		Min	Тур	Max	Min	Max	
		$V_0 = 0.1V, V_{CC}$	0.11/	2.0	1.5			1.5		
V _{IH}	High-level input voltage	$ I_0 = 20\mu A$	5—0.1 V	4.5	3.15			3. 15		V
•		1101 20μΑ		6.0	4.2			4.2		
		$V_{\rm O} = 0.1 V, V_{\rm CO}$	-0.11/	2.0			0. 5		0.5	
VIL	Low-level input voltage	$ I_0 = 20\mu A$		4.5			1.35		1.35	V
		1101 — 20µA		6.0			1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
		'	$I_{OH} = -20\mu A$	4.5	4. 4			4. 4		
VoH	High-level output voltage	$V_{i} = V_{iH}, V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		V
			$t_{OH} = -4.0 \text{mA}$	4.5	4. 18			4.13		
			$I_{OH} = -5.2 \text{mA}$	6.0	5. 68			5.63		
			$I_{OL} = 20 \mu A$	2.0			0. 1		0.1	
			$I_{OL} = 20 \mu A$	4.5			0.1		0.1	
VoL	Low-level output voltage	$V_I = V_{IH}, V_{IL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
	,		I _{OL} = 4.0mA	4.5			0.26		0.33	
	1		$I_{OL} = 5.2 mA$	6.0			0.26	l	0. 33	
I _{IH}	High-level input current	V ₁ = 6V		6.0			0. 1		1.0	μA
I _{IL}	Low-level input current	V ₁ = 0V		6.0			-0. 1		-1.0	μA
Icc	Quiescent supply current	$V_i = V_{CC}$, GND	$I_0 = 0 \mu A$	6.0			4. 0		40.0	μA

SWITCHING CHARACTERISTICS $(v_{cc} = 5v, T_a = 25\%)$

		+		Limits		Unit
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
fmax	Maximum clock frequency		30			MHz
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time				10	115
t _{PLH}	Low-level to high-level and high-level to low-level				40	ns
t _{PHL}	output propagation time (CK — Q)				40	115
t _{PLH}	Low-level to high-level and high-level to low-level				40	
t _{PHL}	output propagation time (CK — CQ)				40	ns
tplH	Low-level to high-level and high-level to low-level	C _L = 15pF (Note 4)			40	
t _{PHL}	output propagation time (R _D — Q)				40	ns
t _{PLH}	Low-level to high-level output propagation time (R _D - CO)				40	ns
t _{PLH}	Low-level to high-level and high-level to low-level				44	
t _{PHL}	output propagation time ($\overline{CK_E} - Q$)		,		44	ns
t _{PLH}	Low-level to high-level and high-level to low-level	7			44	ns
t _{PHL}	output propagation time (CK _E — CO)				44	118

M74HC4022P/FP/DP

OCTAL COUNTER/DIVIDER

SWITCHING CHARACTERISTICS ($V_{cc} = 2\sim 6V$, $T_a = -40\sim +85\%$)

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						Limits		1.0=00	·
Symbol	Parameter	Test conditions	· .		25℃			+85℃	Unit
			V _{CC} (V)	Min	Тур	Max	Min	Max	
	1		2.0	4			3		
fmax	Maximum clock frequency	*.	4.5	20		(16		MH:
			6.0	24			19		
		,	2.0			75		95	
t _{TLH}	Low-level to high-level and	·	4.5	N		15		19	ns
· I LH	Low to to thigh to to and		6.0			13		16	
	high-level to low-level		2. 0		 	75		95	-
			1			1			
t _{THL}	output transition time		4.5			15		19	ns
	<u> </u>	4	6.0			13	 	16	
			2.0			230		290	
t _{PLH}	Low-level to high-level and		4.5			46		58	ns
	high-level to low-level	·	6.0			39		49	1
	output propagation time		2.0			230		290	
tpHL	(CK - Q)	la contraction of the contractio	4.5		Ì	46	Ì	58	ns
			6.0		ł	39		49	
		1	2.0			230		290	
	Low-level to high-level and		4.5			46	ĺ	58	ļ
t _{PLH}	-	1.		*	}	1		1	ns
	high-level to low-level		6.0	L	 	39	<u> </u>	49	<u> </u>
	output propagation time		2.0		İ	230		290	1
t _{PHL}	(CK - CO)		4.5		\ .	46	1	58	กร
		C _L = 50pF (Note 4)	6.0			39		49	
		CL — Sopi (Note 4)	2.0			230		290	
t _{PLH}	Low-level to high-level and	· ·	4.5] .	46		58	ns
	high-level to low-level		6.0	,		39		49	
	output propagation time		2.0			230		290	
t _{PHL}	$(R_D - Q)$		4.5		1	46		58	ns
VPHL:	(11)		6.0			39		49	113
	I am I amal As bish I amal	-							
	Low-level to high-level		2.0			230		290	
t _{PLH}	output propagation time		4.5		1	46	}	58	ns
	(R _D - CO)	<u>.</u>	6.0			39		49	
			2.0		1	250		315	Į.
t _{PLH}	Low-level to high-level and	1	4.5			50		63	ns
	high-level to low-level		6.0		1	43		54	
	output propagation time	1	2.0			250		315	
t _{PHL}	(CKE - Q)		4.5		1	50		63	ns
	1		6.0			43	1	54	
	 	1	2.0		+	250	 	315	+
	Law lavel to blob lovel and		I .		1		"		-
t _{PLH}	Low-level to high-level and		4.5		1	50		63	ns
	high-level to low-level		6.0	ļ	_	43	<u> </u>	54	4
	output propagation time		2.0			250		315	1
tpHL	(CKE - CO)		4.5		1	50		63	ns
	_1:		6.0			43		54	
Cı	Input capacitance					10		10	pF
СРО	Power dissipation capacitance (Note 3)				1			1	pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipation during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$



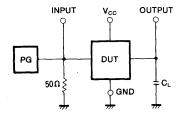
MITSUBISHI HIGH SPEED CMOS M74HC4022P/FP/DP

OCTAL COUNTER/DIVIDER

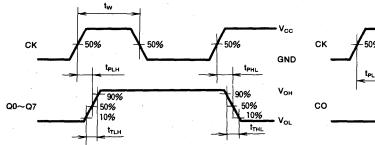
TIMING	REQUIREMENTS	$(v_{cc} = 2\sim 6V, T_a = -40\sim +85^{\circ}C)$
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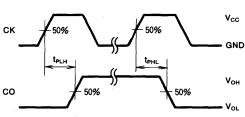
	T					Limits			
Symbol	Parameter	Test conditions			25℃		-40~	+85°C	Unit
			V _{CC} (V)	Min	Тур	Max	Min	Max	1
			2.0	80			101		
tw	CK, CK _E , R _D pulse width		4.5	16		l	20	ļ	ns
	<u> </u>		6.0	14		l	17		
	CK _E setup time with	-	2.0	50			63		
tsu	respect to CK		4. 5	10		1	13	ļ.	ns
	respect to CK		6.0	9			11	L	1
	CK setup time with		2.0	50			63	l	
t _{su}	respect to CKE		4.5	10)	13		ns
	respect to CRE		6.0	9			11		
	CK _E hold time with		2.0	50			63		
th	respect to CK		4.5	10			13	ł	ns
	respect to CK		6.0	9			- 11		
	CK hold time with		2.0	50		,	63		
th	respect to CKE		4.5	10			13		ns
	respect to CKE		6.0	9		İ	11		
	R _D recovery time with		2.0	100			126		
trec	respect to CK		4.5	20			25		ns
	respect to CK	_	6.0	17	L		21		
	R _D recovery time with		2, 0	100			126		
trec	respect to CKE		4.5	20			25	1	ns
	respect to CVE		6.0	17	1		21	L	ł

Note 4: Test Circuit



- (1) The pulse generator (PG) has the following
- characteristics (10%~90%): t_r = 6ns, t_f = 6ns (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.





MITSUBISHI HIGH SPEED CMOS M74HC4022P/FP/DP

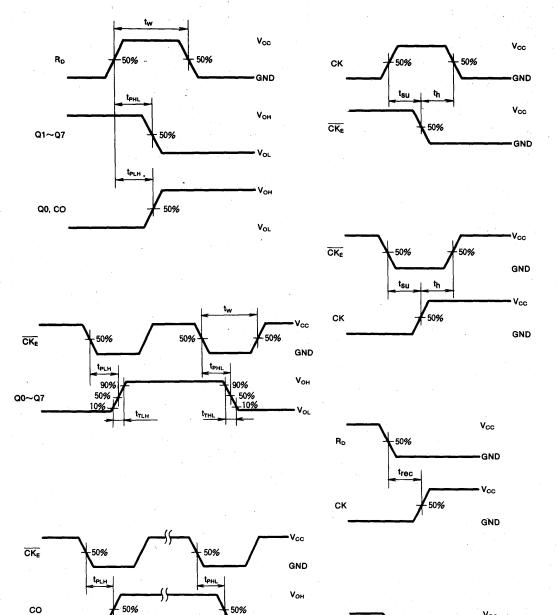
OCTAL COUNTER/DIVIDER

 v_{cc}

GND

Vcc

GND



Vol

Ro

CKE

50%

trec

50%

MITSUBISHI HIGH SPEED CMOS

M74HC4024P/FP/DP

7-STAGE BINARY RIPPLE COUNTER

DESCRIPTION

The M74HC4024 is a semiconductor integrated circuit consisting of an asynchronous 7-stage binary counter with direct reset input.

FEATURES

- High-speed: (clock frequency) 70MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: Ta=-40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

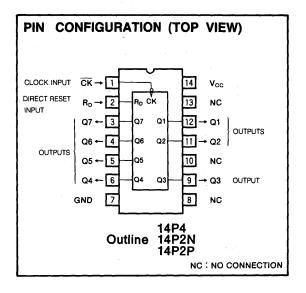
Use of silicon gate technology allows the M74HC4024 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the LSTTL.

The M74HC4024 consists of a 7-stage master-slave flip-flop with independent output signals at each flip-flop.

When used as a counter, the direct reset input R_D is maintained low and the clock pulse applied at clock input \overline{CK} .

The counter operates when $\overline{\text{CK}}$ changes from high-level to low-level, and pure binary codes will appear at each output Q.

When direct reset input R_D is high, all flip-flop will be cleared and Q1 through Q7 all will become low irrespective of \overline{CK} .

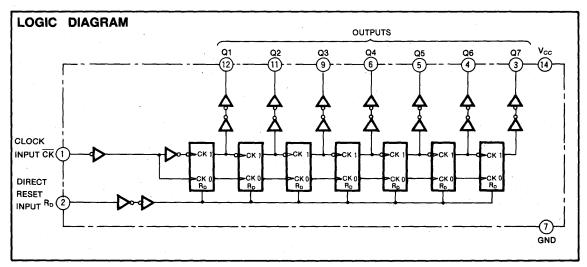


FUNCTION TABLE (Note 1)

inp	uts	
CK	R _D	Output state
Х Н		All outputs are low-level
1	L	No change
1	L	Proceed to next state (counter operation)

Note 1 : X : Irrelevant

- † : Change from low-level to high-level
- ↓ : Change from high-level to low-level



ABSOLUTE MAXIMUM RATINGS $(T_a = -40 \sim +85 \degree)$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
	Input protection diade arrest	V ₁ < 0V	20	
l _{IK}	Input protection diode current	V ₁ > V _{CC}	20	mA
	Outrot and a secretary display a support	V ₀ < 0V	-20	
ок	Output parasitic diode current	$V_{o} > V_{cc}$	20	mA
10	Output current per output pin		±25	mA
Icc	Supply/GND current	V _{CC} , GND	±50	mA.
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		-65~+150	°C

Note 2 : M74HC4024FP, $T_a = -40 \sim +60 ^{\circ}\text{C}$ and $T_a = 60 \sim 85 ^{\circ}\text{C}$ are derated at -6mW/C. M74HC4024DP, $T_a = -40 \sim +50 ^{\circ}\text{C}$ and $T_a = 50 \sim 85 ^{\circ}\text{C}$ are derated at -5mW/C.

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85 \degree c)$

0			Limits					
Symbol	Pal	ameter	Min	Тур	Max	Unit		
Vcc	Supply voltage		2		6	V		
V ₁	Input voltage		0		Vcc	٧		
ν _o	Output voltage	0		Vcc	٧			
Topr	Operating temperature ra	inge	-40		+85	°		
		$V_{CC} = 2.0V$	0		1000			
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns		
Ι		$V_{\rm CC} = 6.0 \text{V}$			400			

ELECTRICAL CHARACTERISTICS

							Limits			
Symbol	Parameter	Test	conditions		25℃			-40~+85°C		Unit
		V _{CC} (V)		Min	Тур	Max	Min	Max		
		$V_0 = 0.1V, V_{co}$	_0 1V	2.0	1.5			1.5		
VIH	High-level input voltage	$ 1_0 = 20\mu A$;0.1 V	4.5	3.15		1	3.15		V
		1101 - 20µA		6.0	4.2		1	4.2		
		$V_0 = 0.1V, V_{co}$	_0.17	2.0			0.5		0.5	
V _{1∟}	Low-level input voltage	$ V_0 = 0.1V, V_{CO}$	0.10	4.5		j	1.35		1.35	v
		1101 - 2000		6.0			1.8		1.8	l
ļ			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
			$I_{OH} = -20\mu A$	4.5	4, 4	1		4. 4	1	
V _{OH}	High-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9			5. 9	L	V
			$I_{OH} = -4.0 \text{mA}$	4.5	4. 18			4. 13		
			$I_{OH} = -5.2 \text{mA}$	6.0	5. 68			5.63		
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
			$I_{OL} = 20 \mu A$	4.5	1	1	0.1	1	0.1	(
VoL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
ļ.	\$		$I_{OL} = 4.0 \text{mA}$	4.5			0.26		0.33	
			$I_{OL} = 5.2 \text{mA}$	6.0			0.26		0.33	
l _{IH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μА
l _{IL}	Low-level input current	$V_1 = 0V$		6.0			-0.1		-1.0	μА
loc	Quiescent supply current	VI = VCC, GND	$I_0 = 0 \mu A$	6.0			4.0		40.0	μА

M74HC4024P/FP/DP

7-STAGE BINARY RIPPLE COUNTER

SWITCHING CHARACTERISTICS ($V_{cc} = 5V$, $T_a = 25\%$)

Symbol	Parameter	Test conditions		Unit		
Symbol	rarameter	L	Min .	Тур	Max	J J
fmax	Maximum clock frequency		30			MHz
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time				10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = 15pF (Note 4)	,		35	ns
t _{PHL}	output propagation time (CK — Q1)	·	,		35	ns
	High-level to low-level output propagation time				25	
t _{PHL}	(R _D - Q1~Q7)		1		35	ns

SWITCHING CHARACTERISTICS ($V_{cc} = 2\sim6V$, $T_a = -40\sim+85^{\circ}C$)

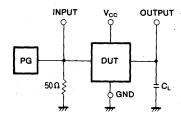
						Limits			1
Symbol	Parameter	Test conditions			25℃		-40~	+85℃	Unit
	1		V _{cc} (V)	Min	Тур	Max	Min	Max]
			2.0	5			4		
fmax	Maximum clock frequency		4.5	27		ł	21		MHz
	1		6.0	32			25	l	l
			2.0			75		95	
t _{TLH}	Low-level to high-level and		4.5			15		19	ns
	high-level to low-level		6.0			13		16	
	liigh-level to low-level		2.0			75		95	
t _{THL}	output transition time		4.5			15		19	ns
		C _L = 50pF (Note 4)	6.0	!		13		16	
		CL = 50pr (Note 4)	2.0			210		265	
t _{PLH}	Low-level to high-level and		4.5		ĺ	42	ľ	53	ns
	high-level to low-level		6.0			36		45	
	output propagation time		2.0			210		265	
t _{PHL}	(CK – Q1)		4.5			42		53	ns
			6.0	[-		36		45	
	High-level to low-level		2.0			210		265	
t _{PHL}	output propagation time	·	4.5		\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	42	i	53	ns
	(R _D - Q1~Q7)		6.0	 		36		45	
Cı	Input capacitance					10		10	pF
C _{PD}	Power dissipation capacitance (Note 3)				60				pF

Note 3 : C_{DP} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load condition is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$

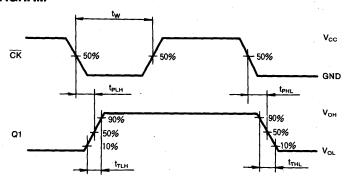
TIMING REQUIREMENT ($v_{cc} = 2\sim 6v$, $T_a = -40\sim +85$ °C)

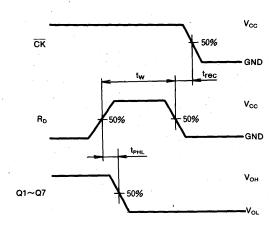
]				
Symbol	Parameter	Test conditions			25℃		-40~	+85℃	Unit .
1			V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0	80			101		
tw	CK, Rp clock pulse width	· .	4.5	16		i	20		ns
			6.0	14			17		
			2.0	100			126		
trec	R _D recovery time with	1	4.5	20		l	25	}	ns
	respect to CK		6.0	17			21		

Note 4: Test Circuit



- (1) The pulse generator (PG) has the following characteristics (10%~90%): $t_{\rm f}$ = 6ns, $t_{\rm f}$ = 6ns
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.







MITSUBISHI HIGH SPEED CMOS

M74HC4040P/FP/DP

12-STAGE BINARY RIPPLE COUNTER

DESCRIPTION

The M74HC4040 is a semiconductor integrated circuit consisting of an asynchronous 12-stage binary counter with a direct reset input.

FEATURES

- High-speed: (clock frequency) 40MHz typ.
 - $(C_L=15pF, V_{CC}=5V)$
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=-40~+85℃

APPLICATION

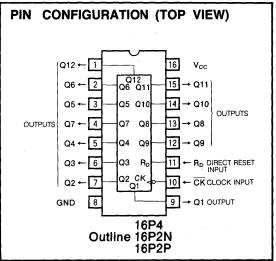
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC4040 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to LSTTL. The M74HC4040 contains a 12-state master-slave flip-flop with independent outputs Q1~Q12 at each flip-flop.

When operated as a counter, the direct reset input R_D should be held low and a clock pulse applied at clock input \overline{CK} .

Counting takes place when $\overline{\text{CK}}$ changes from high-level to low-level, and pure binary code outputs appear at each



outputs Q1~Q12.

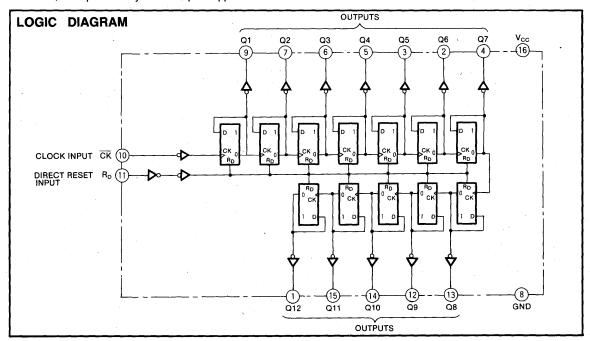
When R_D is set high, all flip-flops will be cleared and all outputs Q1 \sim Q12 will become low irrespective of \overline{CK} .

FUNCTION TABLE (Note 1)

11	nputs	Output state
CK	R₀	Output state
×	Н	All outputs are low-level
†	L	No change
1	L	Advance counter

Note 1: X: Irrelevant

↑ : Change from low to high level ↓ : Change from high to low level



ABSOLUTE MAXIMUM RATINGS ($\tau_a = -40 \sim +85 ^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit		
Vcc	Supply voltage		-0.5~+7.0	V		
Vı	Input voltage		-0.5~V _{cc} +0.5	V		
Vo ·	Output voltage		-0.5~V _{cc} +0.5	V		
		V ₁ < 0V	-20	1		
lik .	Input protection diode current	V _I > V _{CC}	20	mA mA		
	Out-A-servite died-	V _o < 0V	20			
Іок	Output parasitic diode current	Vo > Vcc	20	mA		
lo	Output current per output pin		±25	mA		
loc	Supply/GND current	Vcc, GND	±50	mA		
Pd	Power dissipation	(Note 2)	500	mW		
Tstg	Storage temperature range		−65~+150	င		

Note 2 : M74HC4040FP, $T_a = -40 \sim +70^\circ C$ and $T_a = 70 \sim 85^\circ C$ are derated at -6mW/°C. M74HC4040DP, $T_a = -40 \sim +50^\circ C$ and $T_a = 50 \sim 85^\circ C$ are derated at -5mW/°C.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85^{\circ}C)$

Ć b. al		Parameter		Limits				
Symbol	Pa	rameter	Min	Тур	Max	Unit		
Vcc	Supply voltage	2		6	V			
Vı	Input voltage	0		Vcc	V			
Vo	Output voltage	0		Vcc	V			
Topr	Operating temperature ra	ange	-40		+85	°C		
		$V_{CC} = 2.0V$	0		1000			
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns		
		$V_{CC} = 6.0V$	0		400			

ELECTRICAL CHARACTERISTICS

							Limits			
Symbol	Parameter	Test	conditions	25℃			−40 ~	+85℃	Unit	
					Min	Тур	Max	Min	Max	
		V = 0.1V V	$V_0 = 0.1V, V_{CC} - 0.1V$ $ I_0 = 20\mu A$		1.5			1.5	,	
VIH	High-level input voltage				3. 15			3.15		V
		1101 = 20µA			4.2			4.2		
		V = 0.1V V	$V_0 = 0.1V, V_{CC} = 0.1V$				0.5		0.5	
VIL	Low-level input voltage	$ I_0 = 20\mu A$					1.35		1.35	V -
	1161 - 20μΑ			6.0			1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
	1		$I_{OH} = -20\mu A$	4.5	4.4	1	1	4. 4		
V _{OH}	High-level output voltage	$V_l = V_{lH}, V_{lL}$	$I_{OH} = -20\mu A$	6.0	5.9	1		5.9		V
· · · .			$I_{OH} = -4.0 \text{mA}$	4.5	4.18	1		4.13		
			$I_{OH} = -5.2 \text{mA}$	6.0	5. 68		1	5.63		
			$I_{OL} = 20 \mu A$	2.0			0.1		0. 1	
			$I_{OL} = 20 \mu A$	4.5		1	0.1		0.1	
VoL	Low-level output voltage	$V_i = V_{iH}, \ V_{iL}$	$I_{OL} = 20 \mu A$	6.0		`	0.1		0.1	V
		1	$I_{OL} = 4.0 mA$	4.5			0. 26		0.33	
	1		I _{OL} = 5. 2mA	6.0			0.26		0.33	
l _{iH}	High-level input current	V _I = 6V		6.0			0.1		1.0	μA
l _{IL}	Low-level input current	$V_i = 0V$		6.0			一0.1		-1.0	μA
Icc	Quiescent supply current	$V_l = V_{CC}$, GND	$I_0 = 0\mu A$	6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS $(V_{CC} = 5V, T_a = 25^{\circ}C)$

Symbol	Parameter	Test conditions		Unit		
Symbol	Faranietei	l est conditions	Min	Тур	Max	Onic
fmax	Maximum clock frequency		30			MHz
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time				10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = 15pF (Note 4)			35	ns
t _{PHL}	output propagation time (CK - Q1)				35	ns
	High-level to low-level output propagation time				40	
t _{PHL}	(R _D - Q1~Q12)				40	ns

SWITCHING CHARACTERISTICS $(v_{cc} = 2\sim 6V, T_a = -40\sim +85^{\circ}C)$

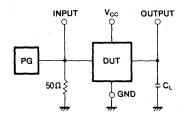
		,				Limits			
Symbol	Parameter	Test conditions			25℃		-40~+85°C		Unit
	}	V _{cc} (V)		Min	Тур	Max	Min	Max	
			2.0	4			3		
fmax	Maximum clock frequency		4.5	20	[[16		MHz
	1		6.0	24			19		
			2.0			75		95	
t _{TLH}	Low-level to high-level and		4.5		ł	15		19	ns
	http://www.houstoneri	,	6.0		1	- 13		16	1
	high-level to low-level		2.0			75		95	
t _{THL}	output transition time		4.5]	15		19	ns
		0 = 50=5 (N===4)	6.0		ł	13		16	
		$C_L = 50 pF $ (Note 4)	2.0			210		265	1
t _{PLH}	Low-level to high-level and		4.5		1	42		53	ns
	high-level to low-level		6.0		[36		45	1
	output propagation time		2.0			210		265	
t _{PHL}	(CK – Q1)		4.5		l	42	-	53	ns
	\		6.0			36		45	1
	High-level to low-level		2.0,			240		302	
t _{PHL}	output propagation time		4.5			48		60	ns
	(R _D - Q1~Q12)		6.0			41		51	1
C,	Input capacitance					10		10	pF
CPD	Power dissipation capacitance (Note 3)								pF

Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot v_{CC}^2 \cdot f_1 + I_{CC} \cdot v_{CC}$

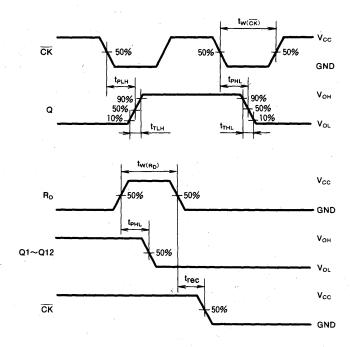
TIMING REQUIREMENTS ($v_{cc} = 2\sim 6V$, $T_a = -40\sim +85^{\circ}C$)

1									
Symbol	Parameter	Test conditions			25℃		−40~	+85℃	Unit
1			V _{cc} (V)	Min	Тур	Max	Min	Max	
· · · · · · · · · · · · · · · · · · ·		2.0	80			101			
tw	t _W CK, R _D pulse width		4.5	16	l		20		ns
L			6.0	14	1		17		
	Ro recovery time with respect to CK		2.0	100			126		
trec			4.5	20			25		ns.
		<u> </u>	6.0	17			21		

Note 4: Test Circuit



- (1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
 (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.



M74HC4049BP/FP/DP

HEX INVERTING BUFFER/LOGIC-LEVEL DOWN CONVERTER

DESCRIPTION

The M74HC4049B is a semiconductor integrated circuit consisting of 6 built-in buffer/converter circuits with inverting outputs.

FEATURES

- High-speed: 12ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 5µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2∼6V
- Wide operating temperature range: Ta=-40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

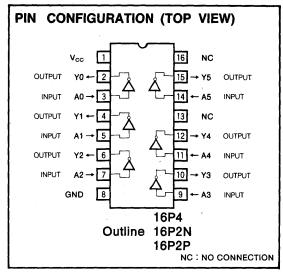
Use of silicon gate technology allows the M74HC4049B to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the LSTTL.

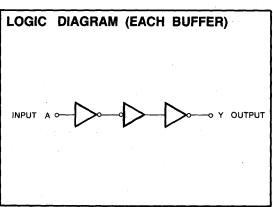
Unlike ordinary input protection circuits, inputs can be applied up to GND+15V, irrespective of $V_{\rm CC},$ allowing the circuit to be used as logic-level converter from CMOS to high-speed CMOS/LSTTL logic circuits.

When input A is high, the output Y will become low, and when input A is low, the output Y will become high.

FUNCTION TABLE

Input	Output
Α	Υ
L	H
Н	L





ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
V _t	Input voltage		-0.5~+18	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
lik	Input protection diode current	V ₁ < 0V	-20	mA
		V ₀ < 0V	-20	
lok	Output parasitic diode current	Vo > Vcc	20	mA
lo	Output current per output pin		±35	mA
loc	Supply/GND current	V _{CC} , GND	土75	mA
Pd	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65~+150	°C

Note 1 : M74HC4049BFP, $T_a = -40 \sim +70 ^\circ C$ and $T_a = 70 \sim 85 ^\circ C$ are derated at $-6 mW/^\circ C$ M74HC4049BDP, $T_a = -40 \sim +50 ^\circ C$ and $T_a = 50 \sim 85 ^\circ C$ are derated at $-5 mW/^\circ C$

HEX INVERTING BUFFER/LOGIC-LEVEL DOWN CONVERTER

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85 ^{\circ}C)$

. 0		Parameter			Limits				
Symbol	Pi	rameter	Min	Тур	Max	Unit			
Vcc	Supply voltage	Supply voltage			6	>			
Vı	Input voltage	0		15	٧				
Vo	Output voltage	0		Vcc	V				
Topr	Operating temperature	ange	-40		+85	ဗ			
		$V_{CC} = 2.0V$	0		1000				
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns			
	$V_{\rm CC} = 6.0V$		0		400	ĺ			

ELECTRICAL CHARACTERISTICS

							Limits			
Symbol	Parameter	Test o	conditions			25℃		-40~	+85℃	Unit
	,	V _C		V _{CC} (V)	Min	Тур	Max	Min	Max	
		V = 0.1V		2.0	1.5			1.5		
`V _{IH}	High-level input voltage	$V_0 = 0.1V$ $ V_0 = 20\mu A$	·		3.15	ļ	ļ	3.15		V
		(IO) = 20µA	51 — 20µA		4.2	ļ		4.2		
		V - V 0 1V	$v = V_{CC} - 0.1V$				0.5		0.5	
V _{IL}	Low-level input voltage	$ V_0 - V_{CC} - 0.1V $ $ I_0 = 20\mu A$		4.5		l	1.35		1.35	V
l	11 ₀ 1 = 20µA			6.0		{	1.8		1.8	
		,	$I_{OH} = -20\mu A$	2.0	1.9			1.9		
Ì		$V_I = V_{IL}$	I _{OH} = -20µA	4.5	4.4		}	4.4		v
VoH	V _{OH} High-level output voltage		$I_{OH} = -20\mu A$	6.0	5.9			5. 9		
		1	$i_{OH} = -6.0 mA$	4.5	4.18			4. 13		
ł		1	$I_{OH} = -7.8 \text{mA}$	6.0	5. 68]	1	5. 63		
			$I_{OL} = 20 \mu A$	2.0			0, 1		0.1	
			$I_{OL} = 20 \mu A$	4.5	Į.		0.1	,	0.1	
VoL	Low-level output voltage	$V_{I} = V_{IH}$	I _{OL} = 20μA	6,0		(0.1	!	0.1	V
	·	1	I _{OL} = 6. 0mA	4.5			0.26		0.33	
		Į.	I _{OL} = 7.8mA	6.0	}		0.26		0.33	
	Mich level input current	V ₁ = 6V		6.0			0.1		1.0	
I _{IH}	High-level input current	$V_1 = 15V$	V ₁ = 15V				0.5		5.0	μΑ
I _{IL}	Low-level input current	V ₁ = 0V		6.0			-0.1		-1.0	μA
_lcc	Quiescent supply current	$V_1 = 15V$, GND,	$I_0 = 0 \mu A$	6.0			1.0		10.0	μA

SWITCHING CHARACTERISTICS (V_{cc} = 5V, T_a = 25°C)

Symbol	Parameter	Test conditions	Limits			Unit
- Cymbol	r arameter	rest conditions :	Min	Тур	Max	01111
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time	C = 50=5 (N=== 3)			10	ńs
t _{PLH}	Low-level to high-level and high-level to low-level	$C_L = 50 pF \text{ (Note 3)}$			15	ns
t _{PHL}	output propagation time				15	ns

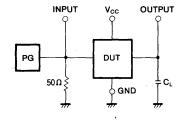
HEX INVERTING BUFFER/LOGIC-LEVEL DOWN CONVERTER

SWITCHING CHARACTERISTICS $(v_{cc} = 2\sim6v, T_a = -40\sim+85^{\circ}c)$

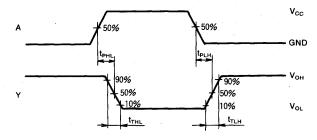
	1			Limits					
Symbol	Parameter	Test conditions V _{CC} (V)		25℃			-40~	+85°C	Unit
				Min	Тур	Max	Min	Max]
			2.0			60		75	
tTLH	Low-level to high-level and		4.5			12		15	ns
		(6.0			10		13	į .
	high-level to low-level	C _L = 50pF (Note 3)	2. 0			60		75	ļ
t _{THL}	output transition time		4.5			12		15	ns
	ł		6.0			10		13	1
			2.0			85		100	
t _{PLH}	PLH .		4.5			17		20	ns
,		1 4	6.0			15	i	18	i
		$C_L = 50 pF (Note 3)$	2.0			75		95	
t _{PHL}	Low-level to high-level and	-	4.5			15		19	ns
			6.0		1	13		16	1
	high-level to low-level		2.0		1	127		150	†
t _{PLH}	output propagation time		4.5			25		30	ns
	1		6.0			22		27	
	†	C _L = 50pF (Note 3)	2.0			112		142	
t _{PHL}		4.5			22		28	ns	
	1		6.0			19		24	
Cı	Input capacitance					10		10	pF
C _{PD}	Power dissipation capacitance (Note 2)				34				pF

Note 2 : CPD is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per buffer) The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$

Note 3: Test Circuit



- (1) The pulse generator (PG) has the following
- characteristics $(10\% \sim 90\%)$: $t_f = 6ns$, $t_f = 6ns$ (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.



M74HC4050BP/FP/DP

HEX NONINVERTING BUFFER/LOGIC-LEVEL DOWN CONVERTER

DESCRIPTION

The M74HC4050B is a semiconductor integrated circuit consisting of 6 built-in buffer/converter circuits with noninverting outputs.

FEATURES

- High-speed: 12ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 5μW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

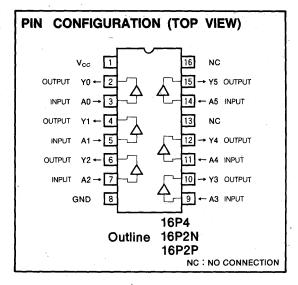
Use of silicon gate technology allows the M74HC4050B to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the LSTTL.

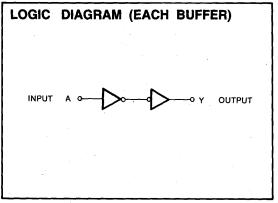
Unlike ordinary input protection circuits, inputs can be applied up to GND+15V, irrespective of $V_{\rm CC}$, allowing the circuit to be used as logic-level converter from CMOS to high-speed CMOS/LSTTL logic circuits.

When input A is high, the output Y will become high, and when input A is low, the output Y will become low.

FUNCTION TABLE

Input	Output
Α	Υ
L	L
Н	Н





ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	. Unit
V _{CC} ,	Supply voltage		-0.5~+7.0	ν
V _t	Input voltage		−0.5~+18	ν
Vo	Output voltage		-0.5~V _{cc} +0.5	ν
lik	Input protection diode current	V ₁ < 0V	-20	mA
	Outside acceptate died accept	V ₀ < 0V	20	
lok	Output parasitic diode current	Vo > Vcc	20	mA
lo	Output current per output pin		±35	mA
Icc	Supply/GND current	V _{CC} , GND	±75	mA
Pd	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65~ +150	°C

Note 1 : M74HC4050BFP, $T_a=-40\sim+70^\circ$ C and $T_a=70\sim85^\circ$ C are derated at -6mW/°C. M74HC4050BDP, $T_a=-40\sim+50^\circ$ C and $T_a=50\sim85^\circ$ C are derated at -5mW/°C.



MT4HC4050BP/FP/DP

HEX NONINVERTING BUFFER/LOGIC-LEVEL DOWN CONVERTER

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85 \text{°C})$

Symbol	D.		Limits				
- Gymboi		arameter	Min	Тур	Max	Unit	
Vcc	Supply voltage	Supply voltage			6	V	
Vı	Input voltage	0		15	٧		
٧o	Output voltage	Output voltage			Vcc	٧	
Topr	Operating temperature	range	-40		+85	°C	
		$V_{CC} = 2.0V$	0		1000		
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns	
		0		400	ĺ		

ELECTRICAL CHARACTERISTICS

					Limits					
Symbol	Parameter Test condition		conditions		25℃			-40~+85°C		Unit
			V _{CC} (V)		Min	Тур	Max	Min	Max	
		$V_0 = V_{CC} - 0.1$,	2.0	1.5			1.5		
V _{IH}	High-level input voltage	$ V_0 - V_{CC} - 0.1$ $ I_0 = 20\mu A$		4.5	3.15		[3.15		V
		1101 - 20µA		6.0	4.2			4.2		
		$V_0 = 0.1V$		2.0			0.5		0.5	
V _{IL}	Low-level input voltage	$ I_0 = 20\mu A$		4.5			1.35		1.35	V
	1101 - 20μΑ		6.0			1.8		1.8	Ĺ	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
)		$I_{OH} = -20\mu A$	4.5	4.4			4.4		
V _{OH}	High-level output voltage	$V_i = V_{iH}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		V
	\		$I_{OH} = -6.0 \text{mA}$	4.5	4.18	•		4.13		
			$I_{OH} = -7.8 \text{mA}$	6.0	5. 68			5.63		
			$I_{OL} = 20 \mu A$	2.0			0.1	1	0.1	
	1	*	$I_{OL} = 20 \mu A$	4.5	!		0.1	ł	0.1	}
VoL	Low-level output voltage	$V_i = V_{iL}$	$I_{OL} = 20 \mu A$	6.0			0.1		0.1	V
			$I_{OL} = 6.0 \text{mA}$	4.5			0. 26		0.33	}
			I _{OL} = 7.8mA	6.0			0. 26	·	0.33	
	High level input ourrent	V _I = 6V		6.0			0.1		1.0	
I _{IH}	High-level input current $V_i = 15V$			6.0			0.5		5.0	μA
I _{IL}	Low-level input current	$V_1 = 0V$		6.0			-0.1		-1.0	μA
Icc	Quiescent supply current	V ₁ = 15V, GND	$I_0 = 0\mu A$	6.0			1.0		10.0	μA

SWITCHING CHARACTERISTICS ($v_{cc} = 5v$, $T_a = 25^{\circ}C$)

Symbol	Parameter	Test conditions		Limits		Unit
Symbol	Farameter	l'est conditions	Min	Тур	Max	Unit
t _{TLH}	Low-level to high-level and high-level to low-level				10	
tTHL	output transition time	C _L = 50pF (Note 3)			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = 50pr (Note 5)			15	
t _{PHL}	output propagation time	·			15	ns

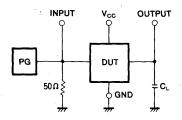
HEX NONINVERTING BUFFER/LOGIC-LEVEL DOWN CONVERTER

SWITCHING CHARACTERISTICS ($v_{cc} = 2\sim6$ V, $T_a = -40\sim+85$ °C)

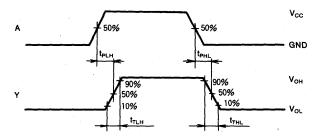
						Limits			
Symbol	Parameter	Test conditions			25°C		−40~	+85℃	Unit
		V _{cc} (V)		Min Typ		Max	Min Max		
			2.0			60		75	
t _{TLH}	Low-level to high-level and		4.5			-12		15	ns
	-	$C_L = 50 pF $ (Note 3)	6.0			10		13	
	high-level to low-level	CL = SOPF (Note 3)	2.0	,		60		75	
t _{THL}	output transition time		4.5			12		15	ns
			6.0			10		13	
			2.0			85		100	
tplH			4.5			17		20	ns
-		C _L = 50pF (Note 3)	6.0	_ : _		15		18	
		CL - SOPF (Note 3)	2.0			75		95	
t _{PHL}	Low-level to high-level and		4.5	į		15		19	ns
	,		6.0			13		16	
	high-level to low-level		2.0			127		150	
tpLH	output propagation time		4.5			25		30	ns
		O = 50=5 (N=== 3)	6.0		ŀ	22	İ	27	1
		C _L = 50pF (Note 3)	2.0			112		142	
tpHL			4.5			22	l	28	ns
			6.0			19		24	
Cı	Input capacitance					10		10	рF
CPD	Power dissipation capacitance (Note 2)				32				pF

Note 2 : CPD is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per buffer) The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$

Note 3: Test Circuit



- (1) The pulse generator (PG) has the following
- characteristics (10% \sim 90%): $t_r = 6ns$, $t_f = 6ns$ (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.







MITSUBISHI HIGH SPEED CMOS

M74HC4051P/FP/DP

8-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

DESCRIPTION

The M74HC4051 is a semiconductor integrated circuit consisting of a multiplexer/demultiplexer which is capable of selecting between 8 analog switches with 3-input digital signal.

FEATURES

- Low on-state resistance
- High off-state resistance: more than 10⁹Ω, typ.
- Excellent conductance linearity. Distortion 0.05% typ.
- Enable input
- High-speed: 18ns typ. (C_L = 50pF, V_{CC} = 4.5V, V_{EE} = GND)
- Low power dissipation: 20μW/package, max
 (V_{CC}=5V, V_{EE}=GND, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Wide operating voltage range: V_{CC}-V_{EE}=2~12V
 V_{CC}-GND=2~6V
- Wide operating temperature range: T_a=−40~+85°C

PIN CONFIGURATION (TOP VIEW) 16 CHANNEL INPUTS/OUTPUTS x6 X4 15 COMMON PIN CHANNEL INPUTS/OUTPUTS 13 CHANNEL INPUTS/OUTPUTS 12 ENABLE INPUT 6 11 10 CONTROL INPUTS 7 GND 9 16P4 Outline 16P2N 16P2P

APPLICATION

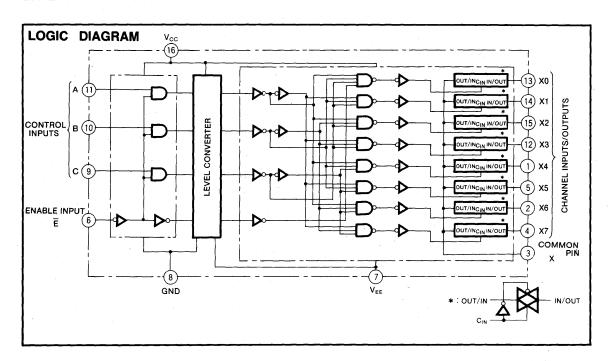
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC4051 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the LSTTL.

When a three-bit binary code is applied at control inputs A, B and C, the impedance between the common pin X and the selected channel X0 through X7 will become low-impedance state, and the other channels will become high-impedance state. In this case, when enable input \overline{E} is high, all channels X0 through X7 will become high-impedance state, irrespective of other inputs.

Analog signals of amplitude V_{CC} - V_{EE} greater than logic amplitude V_{CC} -GND at A, B and C can be switched.



8-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

FUNCTION TABLE (Note 1)

Enable input		Control inputs		Switch between channel input/output and common pin							
Ē	С	В	Α	Х0	X1	X2	Х3	X4	X5	Х6	X7
L	L	L	L	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
L	L	L	Н	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF
L	L	Н	L	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF
L	L	Н	Н	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF
L	Н	L	L	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF
L	Н	L	Н	OFF.	OFF	OFF	OFF	OFF	ON	OFF	OFF
L	Н	Н	L	OFF	OFF.	OFF	OFF	OFF	OFF	ON	OFF
L	Н	Н	Н	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
Н	Х	Х	Х	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

Note 1 : X : Irrelevant

ON : Impedance between Xn and X is low. (n: $0\sim7$)
OFF : Impedance between Xn and X is high. (n: $0\sim7$)

ABSOLUTE MAXIMUM RATINGS ($\tau_a = -40 \sim +85^{\circ}$ C, unless otherwise noted)

Symbol	Parameter	Test conditions	Ratings	Unit
Vcc	Construction -		-0.5~+7.0	٧
VEE	Supply voltage		-7.0∼+0.5	V
,	Innut valtage	Control inputs, enable input	-0.5~V _{cc} +0.5	V
Vı	input voltage	I/O channels, common pin	V _{EE} -0.5~V _{CC} +0.5]
V _{1/0}	Input to output voltage		±0.5	V
Vo	Output voltage	-	VEE-0.5~Vcc+0.5	V
	lanut protection diede current	V ₁ < 0V	-20	- ma
l _{IK}	Input protection diode current	V _i > V _{CC}	20	mA
lo	Output current per gate		±25	mA
Icc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature		−65∼+150	င

Note 2 : M74HC4051FP, $T_a = -40 \sim +70^{\circ}\text{C}$ and $T_a = 70 \sim 85^{\circ}\text{C}$ are derated at -6mW/C. M74HC4051DP, $T_a = -40 \sim +50^{\circ}\text{C}$ and $T_a = 50 \sim 85^{\circ}\text{C}$ are derated at -5mW/C.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85 \%)$

				-1	Unit		
Symbol	,	Parameter			Тур	Max	Unit
Vcc				2.0		6.0	٧
VEE	Supply volta	ge	-	0		-6.0	٧
	Control inp		ut, enable input	0.		Vcc	- V
Vı	Input voltage	Channel input/output, common pin				Vcc	٧
Vo	Output volta	ge		VEE		Vcc	٧
Topr	Ambient ope	rating tempe	erature	-40		+85	౮
	T	$V_{CC} = 2.0V$		0		1000	
	Input risetim	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns
	}		$V_{CC} = 6.0V$	0		400	

MITSUBISHI HIGH SPEED CMOS M74HC4051P/FP/DP

8-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

ELECTRICAL CHARACTERISTICS

							Limits				
Symbol	Parameter	Test conditions				25℃		-40~	+85℃	Unit	
			V _{EE} (V)	V _{cc} (V)	Min	Тур	Max	Min	Max		
	Mah Jawal			2.0	1.5			1.5	i		
VIH	High-level	Refer to Ron specification	-	4.5	3. 15		l	3. 15		ν	
	input voltage		_	6.0	4.2			4.2			
			_	2.0			0.5		0.5		
VIL	Low-level	Refer to Ron specification		4.5			1.35		1.35	V	
	input voltage		_	6.0			1.8		1.8		
		$V_i = V_{iH} V_{iL}, I_S = 0.1 mA$	GND	4.5			170		215		
	∤ s.	VIS = GND~VCC	-4.5	4.5		j .	85		106	Ω	
		(Test circuit 1)	-6.0	6.0			50		63		
Ron	On-state resistance	$V_i = V_{iH} V_{iL}, I_S = 0.1 \text{mA}$	GND	2.0							
			GND	4.5			85		106	_	
		V _{IS} = GND, V _{CC} (Test circuit 1)	-4.5	4.5		ĺ	63		78	Ω	
		(Test circuit 1)	-6.0	6.0			37		47		
	On-state resistance varia-	$V_{i} = V_{iH}, V_{iL}$	GND	4.5							
ΔR_{ON}	tion (switch-to-switch in	VIS = GND~VCC	-4.5	4.5					}	Ω	
	the same package)	· · · · · · · · · · · · · · · · · · ·	-6.0	6.0							
	Switch-off	VI = VIH, VIL, VIS = GND, VCC	GND	6.0			±0.1		±1.0		
IZ(OFF)	leakage current	Vos = Vcc, GND	-6.0	6.0			±0.2		±2.0	μΑ	
,	Switch-on	$V_{\rm I} = V_{\rm IH}, V_{\rm IL}, V_{\rm IS} = GND, V_{\rm CC}$	GND	6.0			±0.2		±2.0	Α	
Iz(ON)	leakage current	·	一6.0	6.0			±0.4		±4.0	μ μ	
he	High-level input current	$V_i = 6V$	_	6.0			0. 1		1.0	μΑ	
l _{IL}	Low-level input current	$V_i = 0V$	_	6.0			-0.1		-1.0	μΑ	
	Quiescent power		GND	6.0		}	4. 0	-	40.0		
loc	dissipation	$V_1 = V_{CC}$, GND, $I_0 = 0\mu A$		6.0			8.0		80.0	μ	

SWITCHING CHARACTERISTICS ($V_{cc} = 2\sim 6V$, $T_a = -40\sim +85^{\circ}C$)

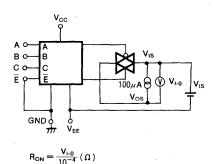
•	_				•		05%	Limits	10	Lor%	ł ,
Symbol	Parame	eter	Test conditions	[N (N)	14 (14)		25℃	-40~-l			Unit
	Navious pagagatio	n fraguency	C = 50=5	V _{EE} (V)	V _{cc} (V)	Min	Тур	Max	Min	Max	├
fmax	Maximum propagation $R_L = 1 k\Omega$, $V_{iS} = 1.6$		C _L = 50pF (Test circuit 2)	-4.5	4.5						MHz
				GND	2.0			. 60		75	
+			Ì	GND	4.5			- 12		15	ns
t _{PLH}	Low-level to high-lev	vel and	D = 160	-4.5	4.5]				113
	high-level to low-leve	el .	$R_L = 1k\Omega$	-6.0	6.0			Ì.	;		,
	output propagation ti	me	$C_L = 50 pF$	GND	2.0			60		75	
	$(x_0 \sim x_7 - x, x - x_0)$	0~X7)	(Test circuit 3)	GND	4.5		1	12	1	15	
t _{PHL}			L :	-4.5	4.5		}	ì	1	1	ns
			,	-6.0	6.0			1	ì	1	
				GND	2.0	•		370		465	
			Į	GND	4.5			74		93	
t _{PLH}	Low-level to high-lev	vel and	D = 11.0	-4.5	4.5				ł		ns
	high-level to low-leve	el	$R_L = 1k\Omega$	-6.0	6.0					-	-
	output propagation ti	me	$C_L = 50 pF$	GND	2.0			370		465	
	(A, B, C - X)		(Test circuit 8)	GND	4.5		l	74	ļ	93	
tpHL				-4.5	4.5		, ,		ļ	1	ns
				-6.0	6.0				(Į.	
				GND	2.0			290		365	
	ľ			GND	4.5			58		73	
t _{PLZ}	Low-level and high-l	evel		-4.5	4.5	-					ns
	output disable time		1	-6.0	6.0						
	/A, B, C - X0~X7	,	1	GND	2.0			290		365	
	$\begin{pmatrix} A, B, C - X0 \sim X7 \\ \overline{E} - X, X0 \sim X7 \end{pmatrix}$			GND	4.5			58		73	
t _{PHZ}				-4.5	4.5			1	-		ns
			$R_L = 1k\Omega$	-6.0	6.0				l	1	1
			$C_L = 50 pF$	GND	2.0			345		435	
			(Test circuit 4)	GND	4.5		1	69		87	
t _{PZL}	Low-level and high-l	evel		-4.5	4.5				}		ns
	output enable time			-6.0	6.0		1	1			1
	(A, B, C - X0~X7)	١		GND	2.0			345		435	
	\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\		Į.	GND	4.5	1		69		87	
t _{PZH}				-4.5	4.5	ļ					ns
		•	İ	-6.0	6.0						1
	0:		V _{IS} = 1.6VRMS								
	Sine wave propagati	OII	$R_L = 10k\Omega$	-4.5	4.5					1	%
	dissipation		(Test circuit 5)				l				
			V _{IS} = 1.6VRMS								
	Feedthrough		$R_L = 10k\Omega$	4.5	4.5						
	(switch off)		$C_L = 50pF$	-4.5	4.5						MH:
			(Test circuit 2)	1]		1.			
	Crosstalk		$R_L = 10k\Omega$								
	Crosstalk (control input,		$R_i = 1 \kappa \Omega$	-4.5	4,5]					mV _P .
	I .	ab autaut\	$C_L = 50pF$	-4.5	4.5						IIIV P.
	enable input-to-switch	on output)	(Test circuit 6)			<u> </u>					
	Crosstalk		$R_L = 1k\Omega$, $C_L = 50pF$	-4.5	4.5		,				мн
	(switch-to-switch)		(Test circuit 7)			ļ			 		
	Input -	ol input	1	-				10	ļ	10	-
Cı	capacitance Chann	nel input/output	<u> </u>	1	1			1	ļ		pF
	Comn	non pin	<u>.</u>		<u> </u>						
Cı	Feedthrough capacit				-		<u> </u>				pF
CPD	Power dissipation capac	itance (Note 3)						1		L	pF

Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$

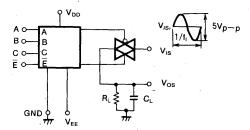


Test Circuit

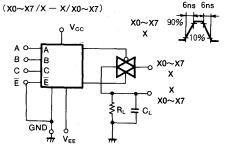
1. On-state resistance



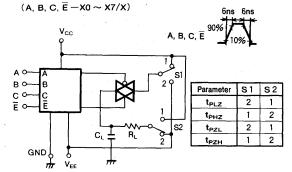
2. Maximum propagation frequency, fledthrough (switch off)



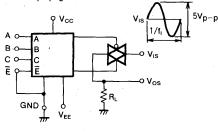
3. Low-level to high-level and high-level to low-level propagation time



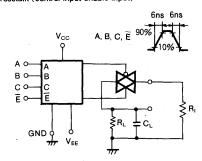
4. Low-level to high-level and high-level to low-level output propagation time, output enable, disable time



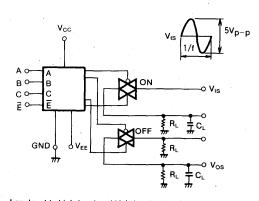
5. Sine wave propagation distortion



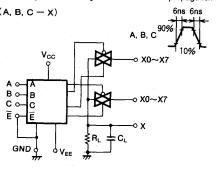
6. Crosstalk (control input enable input)

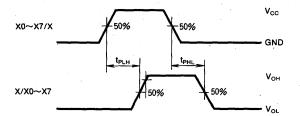


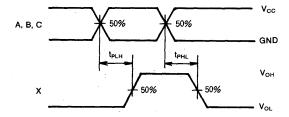
7. Crosstalk (switch-to-switch)

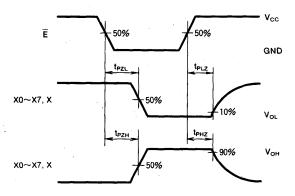


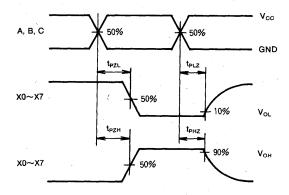
8. Low-level to high-level and high-level to low-level propagation time (A, B, C - X) fins 6ns











MITSUBISHI HIGH SPEED CMOS

M74HC4052P/FP/DP

DUAL 4-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

DESCRIPTION

The M74HC4052 is a semiconductor integrated circuit consisting of two multiplexer/demultiplexers capable of selecting between 4 analog switches with 2-input digital signal.

FEATURES

- Low on-state registance
- High off-state resistance: more than 10⁹Ω, typ.
- Excellent conductance linearity
- Enable input
- High-speed: 28ns typ. (C_L = 50pF, V_{CC} = 4.5V, V_{EE} = GND)
- Low power dissipation: 20µW/package, max
 (V_{GC}=5V, V_{FF}=GND, T_B=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Wide operating voltage range: V_{CC}−V_{EE}=2~12V
 V_{CC}−GND=2~12V
- Wide operating temperature range: T_a=−40~+85°C

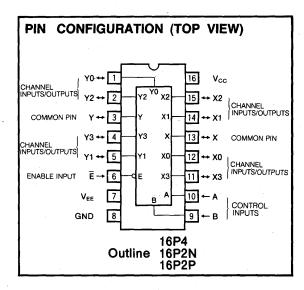
APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC4052 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the LSTTL.

When a two-bit binary code is applied at control inputs A and B, the impedance between common pin X and the selected channel X0 through X3 will become low, and the other channels will become high-impedance state. The impedance between common pin Y and channels Y0 through Y3 is controlled in the same way. In this case, when enable input \overline{E} is high, all channels X0 through X3 and Y0 through Y3 will become high-impedance state, irrespective of other inputs.



Analog signals of amplitude $V_{\text{CC}} - V_{\text{EE}}$ greater than logic amplitude $V_{\text{CC}} - \text{GND}$ at A and B can be switched.

FUNCTION TABLE (Note 1)

Enable	Col	ntrol	Sw	Switch between channel						
input	inp	outs	input	input/output and common pin						
E	В	Α	X0, Y0	X1, Y1	X2, Y2	X3, Y3				
L	L	L	ØN	OFF	OFF	OFF				
L	L	Н	OFF	ON	OFF	OFF				
L	Η	L	OFF	OFF	ON	OFF				
L	н н		OFF	OFF	OFF	ON				
Н	X X		OFF	OFF	OFF	OFF				

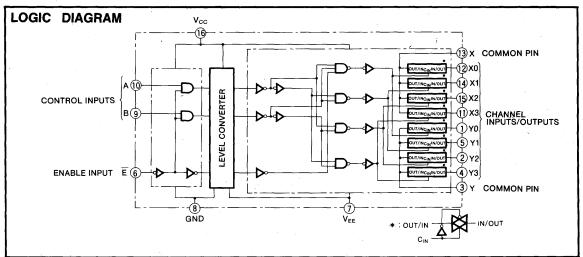
Note 1 : X : Irrelevant

ON : Impedance between Xn and X, and between Yn and

Y is low. (n:0~3)

OFF: Impedance between Xn and X, and btween Yn and Y

is high. (n:0~3)



DUAL 4-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

ABSOLUTE MAXIMUM RATINGS ($\tau_a = -40 \sim +85^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	0		-0.5~+7.0	~
VEE	Supply voltage		−7.0~+0.5	V
	In the section of	Control inputs, enable inputs	-0.5~V _{cc} +0.5	V
V ₁	Input voltage	I/O channels, common pins	V _{EE} -0.5~V _{CC} +0.5	V
V _{I/O}	Input to output voltage		±0.5	V
Vo	Output voltage		V _{EE} -0.5~V _{CC} +0.5	V
	beautiful diede ausent	V ₁ < 0V	-20	
1 _{IK}	Input protection diode current	V _I > V _{CC}	20	mA
· Io	Output current per gate		±25	mA
loc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature		−65 ~ +150	င

Note 2 : M74HC4052FP, $T_a=-40\sim+70^\circ$ C and $T_a=70\sim85^\circ$ C are derated at -6mW/°C. M74HC4052DP, $T_a=-40\sim+50^\circ$ C and $T_a=50\sim85^\circ$ C are derated at -5mW/°C.

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85 ^{\circ}\text{C})$

0			rameter		Limits		Unit
Symbol	ļ	Pai	rameter	Min	Тур	Max	Unit
Vcc	0 1			2.0		6.0	٧
VEE	Supply voltage	ge		0		-6.0	٧
	In a state of a	Control input, enable input Channel input/output, common pin		. 0		-6.0 V _{CC} V _{CC}	
Vı	Input voltage			VEE		V _{CC}	٧
Vo	Output voltag	ge		VEE		Vcc	٧
Topr	Ambient ope	rating tempe	erature	-40		+85	ဗ
			$V_{CC} = 2.0V$	0		1000	
t _r , t _f	Input risetim	e, falltime	$V_{CC} = 4.5V$	0		500	ns
	1		$V_{CC} = 6.0V$	0		400	

ELECTRICAL CHARACTERISTICS

		• *			L		Limits			
Symbol	Parameter	Test conditions				25℃		−40 ~	+85℃	Unit
	L		V _{EE} (V)	V _{cc} (V)	Min	Тур	Max	Min	Max	
	I Park day at	,	_	2.0	1.5			1.5		
V _{IH}	High-level	Refer to R _{ON} specification		4.5	3.15	ļ		3.15	ļ	٧
	input voltage		· -	6.0	4.2	ļ	ţ	4.2	!	
	Low-level		T -	2.0			0.5		0.5	
VIL	1	Refer to Ron specification	_	4.5			1.35	1	1.35	٧
	input voltage		_	6.0	ļ	}	1.8		1.8	
		$V_I = V_{IH} V_{IL}, I_S = 0.1 \text{mA}$	GND	4.5			170		215	
		VIS = GND~VCC	-4.5	4.5	}		85	}	106	Ω
		(Test circuit 1)	-6.0	6.0	1	l	50		63	
R _{ON} On-state resistance	$V_i = V_{iH} V_{iL}$, $I_S = 0.1 \text{mA}$	GND	2.0							
			GND	4.5	1		85		106	
		V _{IS} = GND, V _{CC}	-4.5	4.5		}	63		78	Ω
		(Test circuit 1)	-6.0	6.0	1	}	37		47	
	On-state resistance varia-	$V_{i} = V_{iH}, V_{iL}$	GND	4.5						
ΔR_{ON}	tion (switch-to-switch in	VIS = GND~VCC	-4.5	4.5					Į.	Ω
	the same package)		-6.0	6.0	1	ì				
	Switch-off	VI = VIH, VIL, VIS = GND, VCC	GND	6.0			±0.1		±1.0	
I _{IZ} (OFF)	leakage current	Vos = Vcc, GND	-6.0	6.0		Ì	±0.2		±2.0	μΑ
1	Switch-on	$V_{\rm I} = V_{\rm IH}, V_{\rm IL}, V_{\rm IS} = {\rm GND}, V_{\rm CC}$	GND	6.0			±0.2		±2.0	
IZ(ON)	leakage current		-6.0	6.0			±0.4		±4.0	μA
l _{iH}	High-level input current	$V_1 = 6V$	_	6.0			0.1		1.0	μA
I _{IL}	Low-level input current	$V_1 = 0V$		6.0			-0.1		-1.0	μA
-	Quiescent power	V = V CND 1 = 0	GND	6.0			4.0		40.0	
lcc	dissipation	$V_1 = V_{CC}$, GND, $I_0 = 0\mu A$	-6.0	6.0	l		8.0	· ·	80.0	μΑ

DUAL 4-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

SWITCHING CHARACTERISTICS ($V_{cc} = 2\sim6V$, $T_a = -40\sim+85^{\circ}C$)

Symbol		Parameter	Test conditions				25℃	Limits	-40~	+85°C	Unit
		· diamotor	100t conditions	V _{EE} (V)	V _{cc} (V)	Min	Тур	Max	Min	Max	1
f _{max}	Maximum pro $R_L \approx 1 k \Omega$, V_R	pagation frequency	C _L = 50pF (Test circuit 2)	-4.5	4.5		- 7,				МН
	1			GND	2.0			60		75	
				GND	4.5			12		15	
t _{PLH}		high-level and		-4.5	4.5						ns
	high-level to		$R_L = 1 k\Omega$	-6.0	6.0						[
	output propag		$C_L = 50pF$	GND	2.0			60		75	
		x-x0~x3	(Test circuit 3)	GND	4.5			12		15	
t _{PHL}	(Y0~Y3-Y,	Y-Y0~Y3)		-4.5	4.5						ns
	1			-6.0	6.0					1	
			1	GND	2.0			370		465	
	İ			GND	4.5			74		93	
t _{PLH}	Low-level to I	high-level and		-4.5	4.5		ĺ				ns
	high-level to	low-level	$R_L = 1k\Omega$	-6.0	6.0						
	output propag		$C_L = 50pF$	GND	2.0			370		465	
	(A, B-X,		(Test circuit 8)	GND	4.5			74		93	
t _{PHL}				-4.5	4.5						ns
				-6.0	6.0						
				GND	2.0			290		365	
				GND	4.5			58		73	
tPLZ	Low-level and	d high-level		-4.5	4.5						ns
		Low-level and high-level output disable time		-6.0	6.0		ľ	1		}	
	⊣ . '			GND	2.0			290		365	
	$\begin{pmatrix} A, B-X0\sim X3,Y0\sim Y3\\ \overline{E}-X, X0\sim X3, Y, Y0\sim Y3 \end{pmatrix}$		GND	4.5			58		1		
t _{PHZ}	(= 1,1,1	,		-4.5	4.5		ĺ				ns
			$R_L = 1k\Omega$	-6.0	6.0		1	1		73	١.
			$C_L = 50pF$	GND	2.0			345		435	
			(Test circuit 4)	GND	4.5			69		87	
t _{PZL}	Low-level and	d high-level		-4.5	4.5		Ì	-	ĺ		ns
	output enable	•		-6.0	6.0						1
	(A, B−X0~			GND	2.0			345		435	
		x3, Y, Y0~Y3)		GND	4.5		l	69		87	ĺ
t _{PZH}	(= ,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	, .,		-4.5	4.5				ł	}	ns
				-6.0	6.0]		}		1
	 		Vis = 1.6VRMS	+	3.0						
	Sine wave pr	opagation	$R_L = 10k\Omega$	-4.5	4.5			-	ĺ	1	%
	distortion		(Test circuit 5)							1	"
	1		V _{IS} = 1.6VRMS	+						 	
	Feedthrough		$R_L = 10k\Omega$				ŀ		l		
	(switch off)		C _L ≈ 50pF	-4.5	4.5		i		ĺ	1	МН
	(Giriton Gir)		(Test circuit 2)	1			1			1	
	 		$R_L = 10k\Omega$	+	 			-			
	Crosstalk		$R_i = 1 k \Omega$								
	(control input		C _L ≈ 50pF	-4.5	4.5				1	1	mV₅
	enable input	t-to-switch outputs)	(Test circuit 6)						1		
	Crosstalk		$R_L = 1k\Omega$, $C_L = 50pF$	+	 				 	+	-
	(switch-to-sw	vitch)	(Test circuit 7)	-4.5	4.5						МН
	(577.577 10754)	Control input	,	+				10	 	10	1
C,	Input	Channel input/output	†					 		1	pF
-1	capacitance	Common pin	†				<u> </u>	1			ן "'
C _i	Feedthrough	<u> </u>	1 .			<u> </u>	 	 		<u> </u>	pF
C _{PD}		on capacitance (Note 2)		+			 	 	1	+	pF

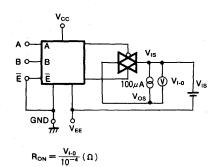
Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot v_{CC}^2 \cdot f_i + I_{CC} \cdot v_{CC}$



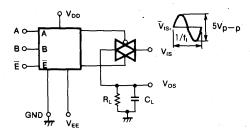
DUAL 4-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

Test Circuit

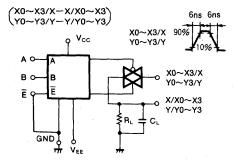
1. On-state resistance



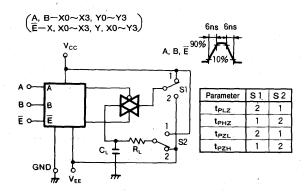
2. Maximum propagation frequency, fieldthrough (switch off)



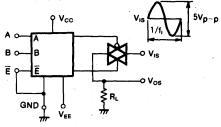
3. Low-level to high-level and high-level to low-level propagation time



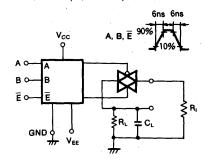
 Low-level to high-level and high-level to low-level output propagation time, output enable, disable time



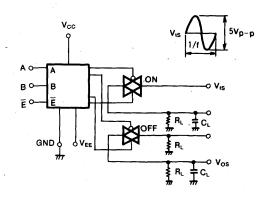
5. Sine wave propagation distortion



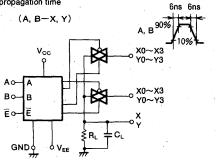
6. Crosstalk (control input, enable input)



7. Crosstalk (switch-to-switch)

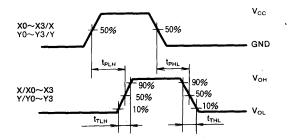


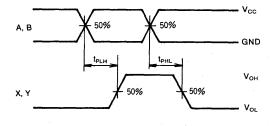
Low-level to high-level and high-level to low-level propagation time

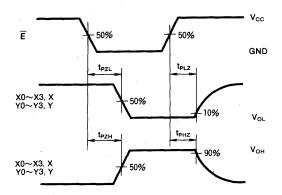


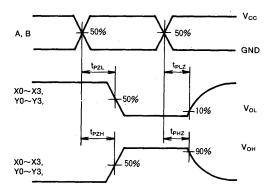
M74HC4052P/FP/DP

DUAL 4-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER









MITSUBISHI HIGH SPEED CMOS

M74HC4053P/FP/DP

TRIPLE 2-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

DESCRIPTION

The M74HC4053 is a semiconductor integrated circuit consisting of three multiplexers/demultiplexers capable of selecting between 2 analog switches.

FEATURES

- Low on-state resistance
- High off-state resistance: more than $10^9 \Omega$, typ.
- Excellent conductance linearity
- Enable input
- High-speed: 28ns typ. ($C_L = 50pF$, $V_{CC} = 4.5V$, $V_{EE} = GND$)
- Low power dissipation: 20μW/package, max
 (V_{CC}=5V, V_{EE}=GND, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Wide operating voltage range: V_{CC}−V_{EE}=2~6V
 - V_{CC} -GND=2~6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

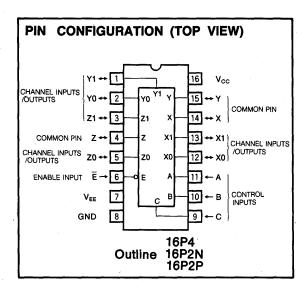
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC4053 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS4053.

When a one-bit binaly code is applied at control inputs A, B and C, the impedance between the common pin and the selected channel will become low, and the other channels will become high-impedance state.

In this case, when enable input \overline{E} is high, all channels will become high-impedance state, irrespective of other inputs.



Analog signals of amplitude V_{CC} - V_{EE} greater than logic amplitude V_{CC} -GND at A, B and C can be switched.

FUNCTION TABLE (Note 1)

Enable input	Control inputs	Switches be	tween chanel and common pin
E	A, B, C	X0, Y0, Z0	X1, Y1, Z1
L	L	ON	OFF
L	Н	OFF	ON
H	х	OFF	OFF

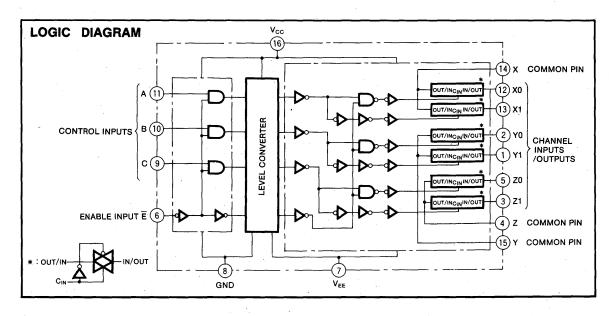
Note 1 : X : Irrelevant

ON: Impedance between Xn and X, Yn and Zn and Z is

low (n:0,1)

OFF: Impedance between Xn and X, Yn and Y, and Zn and

Z is high (n:0,1)



ABSOLUTE MAXIMUM RATINGS $(\tau_a = -40 \sim +85 \degree\text{C}, \text{ unless otherwise noted})$

Symbol	Parameter	Conditions	Ratings	Unit
V _{cc}	0		-0.5~+7.0	V
VEE	Supply voltage		-7.0~+0.5	V
	Input voltage	Control input, enable input	-0.5~V _{CC} +0.5	V
V _I	input voitage	Channel input/output, common pin	V _{EE} -0.5~V _{CC} +0.5	V
V _{I/O}	Input to output voltage		±0.5	V
Vo	Output voltage		V _{EE} -0.5~V _{CC} +0.5	V
	Input protection diode current	V ₁ < 0V	-20	mA
I _{IK}	input protection alode current	V _I > V _{CC}	20	T ITIA
lo	Output current per gate		±25	mA
Icc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature		−65~+150	°C

Note 2 : M74HC4053FP, $T_a = -40 \sim +70^{\circ}\text{C}$ and $T_a = 70 \sim 85^{\circ}\text{C}$ are derated at -6mW/C. M74HC4053DP, $T_a = -40 \sim +50^{\circ}\text{C}$ and $T_a = 50 \sim 85^{\circ}\text{C}$ are derated at -5mW/C.

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85 \degree c)$

Symbol		. Do	rameter		Limits		11-14
Symbol		га	rameter	Min	Тур	Max	Unit
Vcc	C	_:		2.0		6.0	V
VEE	Supply volta	ge 		0		-6.0	٧
V,	Input voltage		ut, enable input	0		Vcc	ν
V ₁	input voitage	Channel in	put/output, common pin	VEE		Vcc	V
Vo	Output volta	ge	·	VEE		Vcc	V
Topr	Ambient ope	erating tempe	erature	-40		+85	°C
			$V_{CC} = 2.0V$	0		1000	
tr, tr	Input risetim	e, falltime	$V_{CC} = 4.5V$	0		500	ns
	$V_{CC} = 6.0V$			0		400	

ELECTRICAL CHARACTERISTICS

		4					Limits			
V _{IL}	Parameter	Test conditions				25℃		-40~	+85℃	Unit
			V _{EE} (V)	V _{cc} (V)	Min	Тур	Max	Min	Max	1
	High-level		- '	2.0	1.5			1.5		
V _{IH}	input voltage	Refer to R _{ON} specification	-	4.5	3.15			3.15		v
	input voltage	·	_	6.0	4. 2			4.2		ì
	Low-level		_	2.0			0.5		0.5	
VIL	input voltage	Refer to R _{ON} specification	_	4.5]	1.35	!	1.35	V
	input voitage			6.0	-		1.8		1.8	ĺ
		$V_{I} = V_{IH} V_{IL}, I_{S} = 0.1 \text{mA}$	GND	4.5			170		215	
		Vis = GND~Vcc	-4.5	4.5	į		85		106	Ω
		(Test circuit 1)	-6.0	6.0			50		63	
RON	On-state resistance	$V_i = V_{iH} V_{iL}, I_S = 0.1 \text{mA}$	GND	2.0						
		$V_{IS} = GND, V_{CC}$	GND	4.5		1	85		106	
		(Test circuit 1)	-4.5	4.5		j	63		78	Ω
		(Test circuit 1)	-6. 0	6.0			37		47	
	On-state resistance varia-	$V_i = V_{iH}, V_{iL}$	GND	4.5						
ΔRON	tion (switch-to-switch in	V _{IS} = GND~V _{CC}	-4.5	4.5		-	l	}		Ω
	the same package)	k	-6.0	6.0		J				
I _{IZ(OFF)}	Switch-off	$V_{I} = V_{IH}, V_{IL}, V_{IS} = GND, V_{CC}$	GND	6.0			±0.1		±1.0	
'IZ(OFF)	leakage current	Vos = Vcc, GND	-6.0	6.0			±0.2		±2.0	μA
I _{IZ(ON)}	Switch-on	$V_{l} = V_{lH}, V_{lL}, V_{lS} = GND, V_{CC}$	GND	6.0			±0.2		±2.0	
IZ(ON)	leakage current		-6.0	6.0			±0.4		±4.0	μA
I _{IH}	High-level input current	$V_1 = 6V$	-	6.0			0.1		1.0	μА
l _{IL}	Low-level input current	$V_i = 0V$	_	6.0			-0.1		-1.0	μА
L	Quiescent power	V - V CND I - O.A	GND	6.0			4.0		40.0	
I _{CC}	dissipation	$V_i = V_{CC}$, GND, $I_O = 0\mu A$	-6.0	6.0			8.0		80.0	μA

SWITCHING CHARACTERISTICS ($V_{cc} = 2\sim6V$, $T_a = -40\sim+85$ °C)

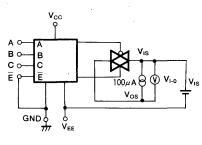
Symbol		Parameter	Test conditions				25℃	Limits	-40~	LOESC	Unit
Symbol		rarameter	rest conditions	V _{EE} (V)	V _{cc} (V)	Min	Typ	Max	Min	Max	Unit
	Maximum proj	pagation frequency	$C_L = 50pF$				1,50	Wax	141111		<u> </u>
fmax	$R_L = 1k\Omega, V_{is}$	s = 1.6VRMS	(Test circuit 2)	-4.5	4.5		Ì]			MHz
				GND	2.0			60		75	
•	Low-level to h	nigh-level and		GND	4.5			12		15	ns
t _{PLH}	high-level to I	ow-level	$R_L = 1 k\Omega$	-4.5	4.5			Į			118
	output propag	ation time	$C_L = 50 pF$	-6.0	6.0						
	/X0, X1-X/X		(Test circuit 3)	GND	2.0			60		75	
t _{PHL}	Y0, Y1-Y/Y	Y—Y0, Y1	(Test circuit 5)	GND	4.5		1	12		15	ns
PHL	\Z0, Z1-Z/2	Z—Z0, Z1/		-4. 5	4.5			l	ļ		',5
				6.0	6, 0						
{				GND	2.0		Ì	370		465	
tpLH	Low-level to h	nigh-level and	,	GND	4.5		1	74		93	ns
PLH	high-level to I	ow-level	$R_L = 1 k\Omega$	-4.5	4.5		l	ļ			""
	output propag	ation time	C _L = 50pF	-6.0	6.0						
	(A-X)		(Test circuit 8)	GND	2.0]	370		465	
t _{PHL}	B-Y		(100t Girodit G)	GND	4.5			74		93	ns
THE.	\c-z/			-4. 5	4.5						"
				-6.0	6.0				· .		<u> </u>
				GND	2.0].	290	İ	365	
t _{PLZ}	Low-level and	i high-level		GND	4.5		1	58	1	73	ns
	output disable	•		-4.5	4.5			l	ļ		113
		Ē—X, X0, X1\		-6.0	6.0						
		Ē-Y, Y0, Y1		GND	2.0			290	}	365	
t _{PHZ}	1	E-z, zo, zı	-	GND	4.5			58	1	73	ns
TPHZ	(0 20, 217	2, 20, 217	$R_L = 1k\Omega$	-4. 5	4.5			ļ	1		""
			$C_L = 50 pF$	-6.0	6.0						
			(Test circuit 4)	GND	2.0			345		435	
	Low-level and	t high lavel	(Test Choulty)	GND	4.5		1	69	1	87	
	output enable	-		-4.5	4.5				1		ns
	· ·	ĒX, X0, X1∖		-6.0	6.0						
	1	Ē-Y, Y0, Y1		GND	2.0			345		435	
t _{PZH}	1	Ē-Z, ZO, Z1		GND	4.5		}	69		87	ns
чегн	. (0 20, 217	L 2, 20, 21/		-4.5	4.5		1				"
				-6.0	6.0						
	Sine wave pro	opogation	V _{IS} = 1.6VRMS								
ľ	dissipation	opagation	$R_L = 10k\Omega$	-4.5	4.5		ì	ì			%
			(Test circuit 5)				<u> </u>		L		<u> </u>
. 1			V _{IS} = 1.6VRMS					ļ	ļ		1
}.	Feedthrough		$R_L = 10k\Omega$	-4.5	4.5						мн
.	(switch off)		$C_L = 50pF$	7.3	4.5		1) -			1
			(Test circuit 2)					<u> </u>			
	Crosstalk		$R_L = 10k\Omega$								
1	(control input		$R_i = 1 k\Omega$	-4.5	4.5		i				mV _P
Į.			C _L = 50pF	4.3	4.5						""*
L	Chable input	to-switch output)	(Test circuit 6)				ļ	1			<u> </u>
.	Crosstalk		$R_L = 1k\Omega$, $C_L = 50pF$	-4.5	4.5						мн
	(switch-to-sw	ritch)	(Test circuit 7)	7.5	7.5						14.11
	Input	Control input]					10		10	1
C ₁	capacitance	Channel input/output	1								pF
		Common pin	_								1
Cí	Feedthrough	capacitance									pF
CPD	Power dissipation	on capacitance (Note 2)		1)]	1			1	pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$



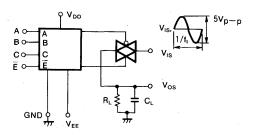
Test Circuit

1. On-state resistance

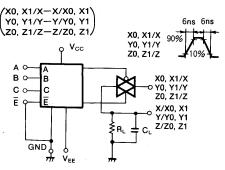


$$R_{ON} = \frac{V_{I\text{-}0}}{10^{-4}} \left(\Omega \right)$$

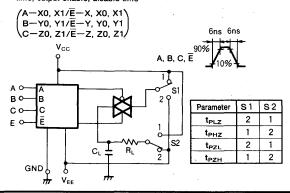
2. Maximum propagation frequency, fieldthrough (switch off)



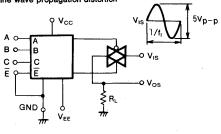
3. Low-level to high-level and high-level to low-level propagation time



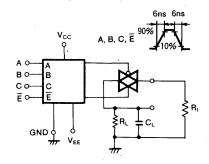
 Low-level to high-level and high-level to low-level output propagation time, output enable, disable time



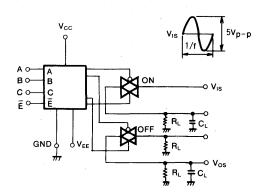
5. Sine wave propagation distortion



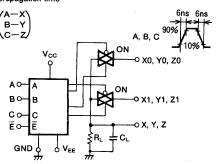
6. Crosstalk (control input, enable input)

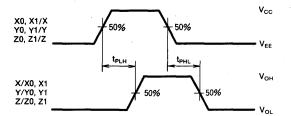


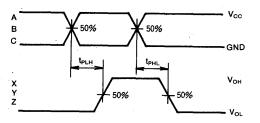
7. Crosstalk (switch-to-switch)

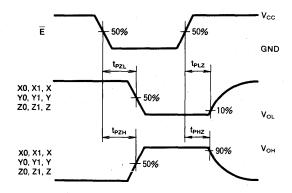


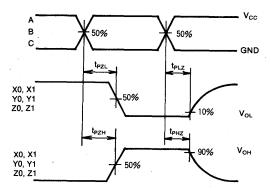
Low-level to high-level and high-level to low-level propagation time











M74HC4066P/FP/DP

QUADRUPLE ANALOG SWITCH/MULTIPLEXER/DEMULTIPLEXER
WITH ENHANCED ON-RESISTANCE LINEARITY

DESCRIPTION

The M74HC4066 is a semiconductor integrated circuit consisting of four independent bidirectional analog switches.

FEATURES

- Low on-state resistance 60 Ω typ. (V_{CC}=6V)
- High off-state resistance: more than $10^9 \Omega$, typ.
- Excellent conductance linearity: Variation 0.05% typ.
- High speed: 12ns typ. (C_L=50pF, V_{CC}=6V)
- Low power dissipation: 5µW/package, max (V_{CC}=5V, T_A=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

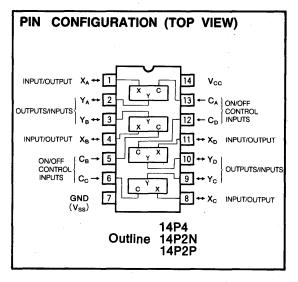
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC4066 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the LSTTL.

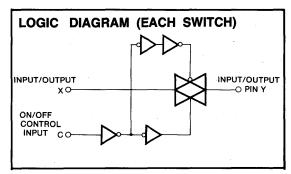
On/off control inputs C_A , C_B , C_C and C_D change the impedance between the switch inputs/outputs X_A - Y_A , X_B - Y_B , X_C - Y_C , and X_D - Y_D .

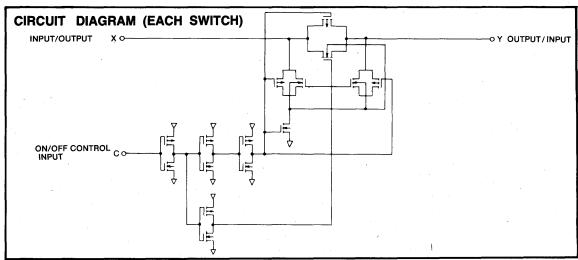
When control input C_A , C_B , C_C , and C_D are high, the impedance between the corresponding switch inputs/outputs will become low, and when C_A , C_B , C, and C_D are low, the impedance will become high.



FUNCTION TABLE (Note 1)

Inputs	Input/output-to-output/input impedance
С	(V _{CC} = 4.5, 6V)
Н	60~100Ω
L	$>10^9\Omega$ (typ.)





QUADRUPLE ANALOG SWITCH/MULTIPLEXER/DEMULTIPLEXER WITH ENHANCED ON-RESISTANCE LINEARITY

ABSOLUTE MAXIMUM RATINGS $(T_a = -40 \sim +85 \degree)$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		−0.5~+7.0	V ·
Vı	Input voltage		-0.5~V _{cc} +0.5	V
V _{1/O}	Input to output voltage		±0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
•		V ₁ < 0V	-20	
lik .	Input protection diode current	$V_1 > V_{CC}$	20	mA
lo	Output current per gate	10	±25	mA
lcc .	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature		-65∼+150	ဗ

Note 2 : M74HO4066FP, $T_a = -40 \sim +60 ^{\circ} C$ and $T_a = 60 \sim 85 ^{\circ} C$ are derated at $-6mW/^{\circ} C$. M74HC4066DP, $T_a = -40 \sim +50 ^{\circ} C$ and $T_a = 50 \sim 85 ^{\circ} C$ are derated at $-5mW/^{\circ} C$.

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85 ^{\circ}C)$

0		Parameter		Limits				
Symbol	Pal	Falanielei			Max	Unit		
Vcc	Supply voltage		2		6	٧		
V ₁	Input voltage		0		Vcc	V		
Vo	Output voltage		0		Vcc	٧		
Topr	Ambient operating temperating	erature	-40		+85	ဗ		
		V _{CC} = 2.0V	0	-	1000			
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns		
	$V_{CC} = 6.0V$		0		400			

ELECTRICAL CHARACTERISTICS

						Limits			
Symbol	Parameter	Test conditions			25℃		−40 ~	+85℃	Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	
,			2.0	1.5			1.5		
Viii I	High-level input	Refer to Ron specification	4, 5	3.15			3.15		V
	voltage (control)		6.0	4.2	1		4.2		
	1 11		2.0			0.5		0.5	
VIL	Low-level input	$ I_{OFF} \leq 1.0 \mu A$	4.5			1.35		1.35	V
voltage (control)	voitage (control)		6.0			1.8		1.8	
R _{ON} On-state		V _{CTL} = V _{IH}	2.0		1000				
	On-state resistance	V _{IS} = 0~V _{CC} (Test circuit 1)	4.5		100	170		215	Ω
		I _S =100μA	6.0		70	140		180	
	On-state resistance varia-	$V_{CTL} = V_{IH}$	2.0		50				
ΔR_{ON}	tion (switch-to-switch in	$I_S = 100 \mu A$	4.5		3	1			Ω
	the same pacage)	Switch-to-switch	6.0		2				
	Switch-off	V _{CTL} = V _{IL}							
I _{IZ(OFF)}	leakage current	$V_{iS} = 6V, V_{OS} = 0V$	6.0			±0.1	ł	±1.0	μA
	leakage current	$V_{is} = 0V$, $V_{OS} = 6V$							
	Switch-on	$V_{CTL} = V_{IH}$							
I _{IZ(ON)}	leakage current	V _{IS} = 0V~6V	6.0			±0.1		±1.0	μΑ
	leakage current	Vos = OPEN							
I _{IH}	High-level input		6.0			0.1		1.0	μΑ
чн	current (control)		0.0			0.1		1.0	μΑ
l _{iL}	Low-level input		6.0			-0.1		-1.0	μА
'1L	current (control)		0.0					-1.0	μΑ
Icc	Quiescent power dissipation	V _{CTL} = V _{CC} , GND	6.0			1.0		10.0	μΑ

MT4HC4066P/FP/DP

QUADRUPLE ANALOG SWITCH/MULTIPLEXER/DEMULTIPLEXER WITH ENHANCED ON-RESISTANCE LINEARITY

SWITCHING CHARACTERISTICS $(v_{cc} = 2\sim 6V, T_a = -40\sim +85°C)$

0	Parameter	T 4	}		0510	Limits	40	+85°C	·
Symbol	Parameter	Test conditions	1 (11)		25°C				Uni
		$V_{SS} = -2.5V$	V _{cc} (V)	Min	Тур	Max	Mín	Max	
	the second second second					ŀ			
		V _{IS} = 0.88V RMS							
max(I/O)	Maximum prapagation frequency	$R_L = 1k\Omega$ (Test circuit 2)	2.5		30				МН
		C _L = 50pF						1	
		$20\log_{10}V_{\rm O}/V_{\rm i} = -3dB$							
		$R_L = 1k\Omega$	2.0		29			İ	1
fmax(c)	Maximum control frequency	C _L = 15pF (Test circuit 3)	4.5		30				MH
		$V_{OS} = 1/2V_{CC}$	6.0		35				
			2.0		14	50		65	
t _{PLH}	Low-level to high-level and	$R_L=10k\Omega$	4.5		5	10		13	ns
	high-level to low-level	C _L =50pF	6.0		4	9		11	
	output propagation time	(Test circuit 4)	2.0		11	50		65	ĺ
t _{PHL}	(X-Y, Y-X)	(Test circuit 4)	4.5		5	10		13	กร
			6.0		4	9		11	<u>l</u> .
			2.0	,	16	115		145	
PLZ .			4.5		11	23		29	ns
	Low-level and high-level	$R_L = 1k\Omega$	6.0		10	20		25	
	output disable time	C _L = 50pF	2.0		21	115		145	
t _{PHZ}	(C-X, C-Y)	(Test circuit 5)	4.5		13	23		29	ns
			6.0		12	20		25	
			2.0		29	115		145	
t _{PZL}			4.5		10	23		29	ne
'	Low-level and high-level	$R_L = 1k\Omega$	6. Q		8	20		25	'''
	output enable time	$C_L = 50pF$	2.0		27	115		145	
t _{PZH}	(C-X, C-Y)	(Test circuit 5)	4.5		10	23		29	ns
PZH			6.0		8	20		25	'"
		V _{SS} =-2.5V	0.0		-	- 20		25	
	Sine ways propagation	V _{IS} = 0.88V RMS							
	Sine wave propagation	1	2.5		0.02				96
	distortion	$R_L = 10k\Omega$	1 1					1	1
		f _i = 1kHz (Test circuit 6)							
	·	$V_{SS} = -2.5V$							
	Feedthrough	$V_{IS} = 0.88V \text{ RMS}$	_						
	(switch off)	$R_L = 1 k\Omega$ (Test circuit 2)	2.5		1.0				MF
		$C_L = 50pF$	- -						
		$20\log_{10}V_{OS}/V_{IS} = -50dB$							<u> </u>
	Crosstalk	$R_i = 1k\Omega$	2.0		10				
	(control input-to-switch outputs)	$R_L = 10k\Omega$ (Test circuit 7)	4.5		20				m'
	(control input-to-switch curputs)	$C_L = 50pF$	6.0		25				
		$V_{SS} = -2.5V$							
	Crosstalk	VIS = 0.88V RMS			1				1
	1	$R_L = 1k\Omega$ (Test circuit 8)	2.5		1.5				MH
	(switch-to-switch)	(switch-to-switch) $C_L = 50pF$						}	
		$20\log_{10}V_{OS}/V_{IS} = -50dB$	1 1		1				1
C _{I(C)}		Control input			4	10		10	pl
C _{I(X,Y)}	Input capacitance	Input/output, output/input (Test ci	rcuit 9)		T			 	pl
C _{X-Y,Y-X}	Feedthrough capacitance	(Test ci			t			 	pl
- A-1,1-A	Power dissipation capacitance (Note 2)	(,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,			9				pl

Note 2: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$

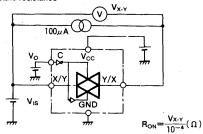


M74HC4066P/FP/DP

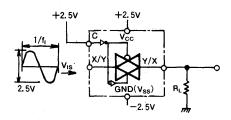
QUADRUPLE ANALOG SWITCH/MULTIPLEXER/DEMULTIPLEXER WITH ENHANCED ON-RESISTANCE LINEARITY

Test Circuit

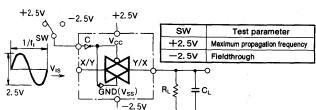
1. On-state resistance



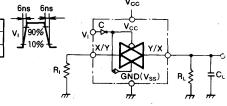
6. Sine wave propagation distortion



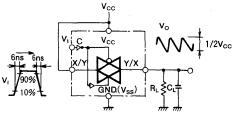
2. Maximum propagation frequency, fieldthrough (switch off)



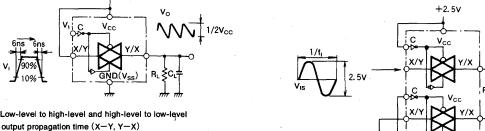
7. Crosstalk (control input-to-switch-input)



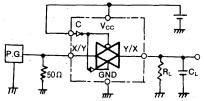
3. Maximum control frequency



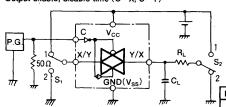
8. Crosstalk (switch-to-switch)



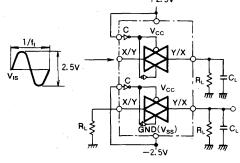
4. Low-level to high-level and high-level to low-level



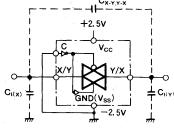
- (1) The pulse generator (PG) has the following characteristics ($10\%\sim90\%$) : tr=6ns, tr=6ns
- The capacitance C_L includes stray wiring capacitance and the probe input capacitance.
- 5. Output enable, disable time (C-X, C-Y)



- (1) The pulse generator (PG) has the following characteristics (10%~90%): t_f=6ns, t_f=6ns
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.



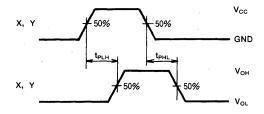
9. Input capacitance, fieldthrough capacitance



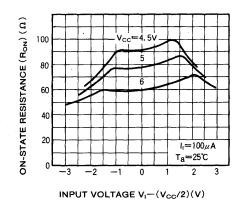
Parameter	S1	S2
t _{PLZ}	2	1
t _{PHZ}	1	2
t _{PZL}	2	1
t _{PZH}	1	2

M74HC4066P/FP/DP

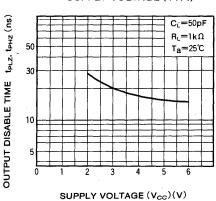
QUADRUPLE ANALOG SWITCH/MULTIPLEXER/DEMULTIPLEXER WITH ENHANCED ON-RESISTANCE LINEARITY

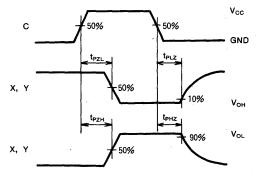


ON-STATE RESISTANCE
— INPUT VOLTAGE (TYP.)

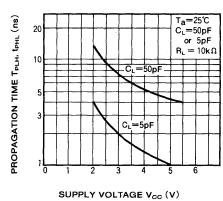


OUTPUT DISABLE TIME - SUPPLY VOLTAGE (TYP.)

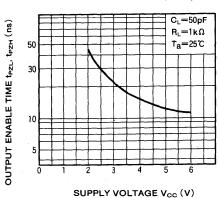




PROPAGATION TIME - SUPPLY VOLTAGE (TYP.)



OUTPUT ENABLE TIME — SUPPLY VOLTAGE (TYP.)





M74HC4075P/FP/DP

TRIPLE 3-INPUT OR GATE

DESCRIPTION

The M74HC4075 is a semiconductor integrated circuit consisting of three 3-input positive-logic OR gates, usable as negative-logic AND gates.

FEATURES

- High-speed: 10ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC4075 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the LSTTL.

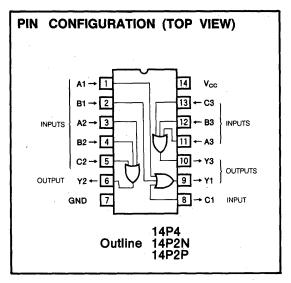
Buffered outputs Y improve input-to-output transfer characteristics and reduce to a minimum output impedance variations with respect to input voltage variations.

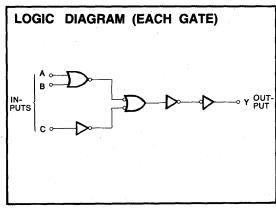
When all inputs A, B and C are low, the output Y will become low, and when at least one of the inputs is high, the output Y will become high.

FUNCTION TABLE

Inp	uts	Output
Α	N	Υ
L	L	L
Н	. L	H
L	н	H
Н	н	н

N = B + C





ABSOLUTE MAXIMUM RATINGS ($\tau_a = -40 \sim +85^{\circ}$ C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
V ₁	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
		V ₁ < 0V	-20	
lik.	Input protection diode current	V _I > V _{CC}	20	mA
	2	V ₀ < 0V	. —20	
ок	Output parasitic diode current	$V_{o} > V_{cc}$	20	mA
lo	Output current per output pin		±25	mA
Icc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		-65~+150	°C

Note 1: M74HC4075FP, $T_a = -40 \sim +60^\circ C$ and $T_a = 60 \sim 85^\circ C$ are derated at -6mW/°C. M74HC4075DP, $T_a = -40 \sim +50^\circ C$ and $T_a = 50 \sim 85^\circ C$ are derated at -5mW/°C.



M74HC4075P/FP/DP

TRIPLE 3-INPUT OR GATE

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85^{\circ}C)$

0		Parameter		Limits			
Symbol	Pa	Parameter				Unit	
Vcc	Supply voltage		2		6	V	
V,	Input voltage	. 0		Vcc	٧		
Vo	Output voltage		0		Vcc	v	
Topr	Operating temperature re	ange	-40		+85	င	
		V _{CC} = 2.0V	0		1000		
tr, tr	Input risetime, falltime	V _{CC} = 4.5V	0		500	ns	
	$V_{\rm cc} = 6.0 V$		0		400		

ELECTRICAL CHARACTERISTICS

					Limits					
Symbol	Parameter	Test	est conditions		25℃			-40~+85°C		Unit
				$V_{CC}(V)$	Min	Тур	Max	Min	Max	
	,	$V_0 = V_{cc} - 0.1$,	2.0	1.5			1.5		
ViH	High-level input voltage	$ I_0 = 20\mu A$		4. 5	3. 15		}	3.15	ļ	V
		1101 - 20µA		6.0	4.2			4.2		
	:	$V_{0} = 0.1V, V_{00}$	_0.11/	2.0			0.5		0.5	
VIL	Low-level input voltage	$ I_0 = 20\mu A$	5—0. I V	4. 5			1. 35		1.35	V
	<u> </u>	1101 - 20μΑ		6.0			1.8	·	1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
	High-level output voltage		$I_{OH} \approx -20\mu A$	4. 5	4.4			4.4	}	v
VoH		$V_i = V_{iH}, V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		
			$I_{OH} = -4.0 \text{mA}$	4.5	4.18			4.13		
			I _{OH} = −5. 2mA	6.0	5. 68			5. 63		
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
	!		$I_{OL} = 20 \mu A$. 4. 5			0.1		0.1	
VOL	Low-level output voltage	$V_i = V_{iL}$	$I_{OL} \approx 20 \mu A$	6.0			0.1	Ì	0.1	v
	İ		I _{OL} = 4.0mA	4.5			0. 26		0.33	
			I _{OL} = 5. 2mA	6.0			0. 26	ĺ	0. 33	1
l _{iH}	High-level input current	V ₁ = 6V	V ₁ = 6V				0.1		1.0	
I _{IL}	Low-level input current	V ₁ = 0V		6.0			-0.1		-1.0	μА
loc	Quiescent supply current	VI = VCC, GND	$I_0 = 0\mu A$	6.0	•		1.0		10.0	μA

TRIPLE 3-INPUT OR GATE

SWITCHING CHARACTERISTICS ($v_{cc} = 2\sim6v$, $T_a = -40\sim+85^{\circ}C$)

Sumb at	Parameter	Test conditions		l lait		
Symbol	Parameter	1 est conditions	Min	Тур	Max	Unit
t _{TLH}	Low-level to high-level and high-level to low-level				10	
t _{THL}	output transition time	O = 15-5 (Note 2)		,	10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = 15pF (Note 3)			20	
tehl	output propagation time				20	ns

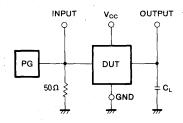
SWITCHING CHARACTERISTICS $(V_{cc} = 2\sim6V, T_a = -40\sim+85^{\circ}C)$

						Limits			
Symbol	Parameter	Test conditions			25℃		-40~	+85°C	Unit
İ.,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,			V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0			75		95	
t _{TLH}	Low-level to high-level and		4.5			15		19	i
1	high level to level		6.0			13		16	
	high-level to low-level		2.0			75		95	ns
t _{THL}	output transition time		4. 5			15		19	
İ		0 = 50-5 (N-1-2)	6.0			13		16	
		C _L = 50pF (Note 3)	2.0			115		145	
t _{PLH}	Low-level to high-level and		4.5			23		29	
	high (sup) to love lavel		6.0			20		25	
	high-level to low-level		2.0			115		145	ns
t _{PHL}	output propagation time		4.5			23	1	29	
			6.0	,		20		25	
Cı	Input capacitance					10		10	рF
C _{PD}	Power dissipation capatitance (Note 2)	×			31				pF

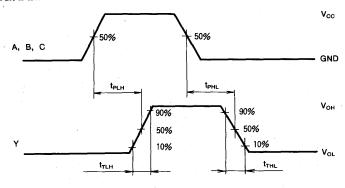
Note 2: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per gate)
The power dissipation during operation under no-load conditions is calculated using the following formula:

 $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$

Note 3: Test Circuit



- (1) The pulse generator (PG) has the following characteristics (10%~90%): $t_r=6$ ns, $t_f=6$ ns
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.



MITSUBISHI HIGH SPEED CMOS

M74HC4078P/FP/DP

8-INPUT POSITIVE NOR/OR GATE

DESCRIPTION

The M74HC4078 is a semiconductor integrated circuit consisting of an 8-input positive-logic NOR/OR gates, usable as a negative-logic NAND/AND gate.

FEATURES

- High-speed: 16ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC4078 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the LSTTL.

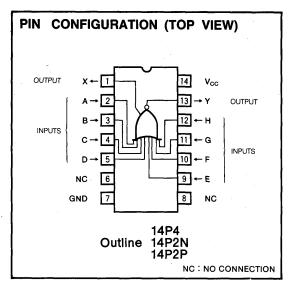
Buffered outputs Y and X improve input-to-output transfer characteristics and reduce to a minimum output impedance variations with respect to input voltage variations.

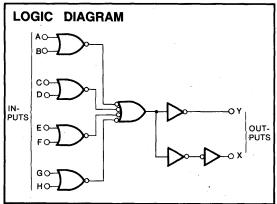
When all inputs A through H are low, output Y will become high and output X will become low. When at least one of the inputs is high, output Y will become low and output X will become high.

FUNCTION TABLE

Int	outs	Out	puts
A	N	Y	X
L	L	Н	L
Н	L	L	Н
L	Н	L	н
н	н	L	Н

N = B + C + D + E + F + G + H





ABSOLUTE MAXIMUM RATINGS $(T_a = -40 \sim +85\%$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	٧
Vi	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
	land and all designs	V ₁ < 0V	-20	4
lικ	Input protection diode current	V _I > V _{CC}	20	mA
		V _o < 0V	-20	
lok	Output parasitic diode current	$v_o > v_{cc}$	20	mA
lo	Output current per output pin		±25	mA
I _{CC}	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		-65~+150	°C

Note 1: M74HC4078FP, $T_a = -40 \sim +60^\circ$ C and $T_a = 60 \sim 85^\circ$ C are derated at -6mW/°C. M74HC4078DP, $T_a = -40 \sim +50^\circ$ C and $T_a = 50 \sim 85^\circ$ C are derated at -5mW/°C.



8-INPUT POSITIVE NOR/OR GATE

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85 \degree C)$

	_			Limits		11-14
Symbol	Pai	ameter	Min	Тур	Max	Unit
Vcc	Supply voltage		2		6	٧
Vi	Input voltage		0		Vcc	V
Vo	Output voltage	0		Vcc	٧	
Topr	Operating temperature ra	inge	-40		+85	ဗ
		$V_{CC} = 2.0V$	0		1000	
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns
		$V_{CC} = 6.0V$	0		400	

ELECTRICAL CHARACTERISTICS

							Limits			
Symbol	Parameter	Test	conditions			25°C		-40~	+85°C	Unit
<u> </u>				V _{cc} (V)	Min	Тур	Max	Min	Max	
		$V_0 = 0.1V, V_{CC}$	- 0.11/	2.0	1.5			1.5		
V _{IH}	High-level input voltage	$ V_0 - 0.1V, V_{CC} $ $ I_0 = 20\mu A$	-0.1 V	4.5	3.15	1	}	3. 15		V
		1101 - 20µA		6.0	4.2	Į	l	4.2	i	
		V = 0.1V V	V- = 0.1V V= 0.1V				0.5		0.5	
V _{IL}	Low-level input voltage	$ V_0 = 0.1V, V_{CO}$ $ I_0 = 20\mu A$	$V_0 = 0.1V, V_{CC} - 0.1V$			ì	1.35		1.35	V
		$ I_0 = 20\mu A$		6.0			1.8		1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
			$I_{OH} = -20\mu A$	4.5	4.4	1	1	4.4		
VoH	High-level output voltage	$V_i = V_{iL}, V_{iH}$	$I_{OH} = -20\mu A$	6.0	5.9	l		5.9		.V
			$I_{OH} = -4.0 \text{mA}$	4.5	4. 18			4.13		
			$I_{OH} = -5.2 mA$	6.0	5.68			5.63	· ·	,
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
			$I_{OL} = 20 \mu A$	4.5			0.1		0.1	
Vol	Low-level output voltage	$V_i = V_{iH}, \ V_{iL}$	$I_{OL} = 20 \mu A$	6.0]	0.1		0.1	V ·
			I _{OL} = 4.0mA	4.5			0.26		0.33	
			$I_{OL} = 5.2 \text{mA}$	6.0			0.26	′	0.33	
t _{iH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μА
I _{IL}	Low-level input current	V ₁ = 0V		6.0			-0.1		-1.0	μA
Icc	Quiescent supply current	VI = VCC, GND	$I_0 = 0 \mu A$	6.0			1.0		10.0	μΑ

8-INPUT POSITIVE NOR/OR GATE

SWITCHING CHARACTERISTICS $(v_{cc} = 5v, T_a = 25^{\circ}C)$

O	B	T		Limits				
Symbol	Parameter	Test conditions	Min	10				
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns		
t _{THL}	output transition time				10	ns		
t _{PLH}	Low-level to high-level and high-level to low-level	C ₁ = 15pF (Note 3)			22	ns		
t _{PHL}	output propagation time (A~H — Y)	C _L = 15pr (Note 3)			22	ns		
t _{PLH}	Low-level to high-level and high-level to low-level	1			24	ns		
t _{PHL}	output propagation time (A~H - X)	•			24	ns		

SWITCHING CHARACTERISTICS $(V_{cc} = 2\sim6V, T_a = -40\sim+85^{\circ}C)$

							Limits			
Symbol	Parameter	Test condi	tions			25℃		-40~	+85°C	Unit
				V _{cc} (V)	Min	Тур	Max	Min	Max	
				2.0			75		95	
t _{TLH}	Low-level to high-level and			4.5			15		19	ns
				6.0			13		16	
	high-level to low-level			2.0			75		95	
t _{THL}	output transition time			4.5		-	15		19	ns
				6.0			13		16	
			`	2.0			130		165	
t _{PLH}	Low-level to high-level and			4.5			26		33	ns
	high-level to low-level	0 50 5 (11 1 0)		6.0			22		28	
	output propagation time	$C_L = 50 pF (Note 3)$		2.0			130		165	
t _{PHL}	(A~H − Y)			4.5			26		33	ns
				6.0			22		28	
				2.0			140		175	
t _{PLH}	Low-level to high-level and			4.5		1	28		35	ns
	high-level to low-level			6.0			24		30	
	output propagation time			2.0			140		175	
t _{PHL}	(A~H − X)			4.5		1	28		35	ns
				6.0			24		30	
Cı	Input capacitance						10		10	pF
C _{PD}	Power dissipation capacitance (Note 2)					75				pF

Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.

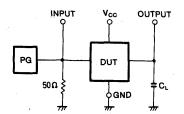
The power dissipated during operation under no-load condition is calculated using the following formula:

P_D = C_{PD} • V_{CC}² • f₁+I_{CC} • V_{CC}

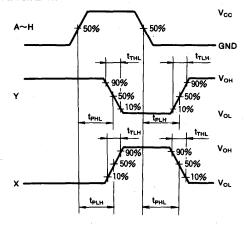


8-INPUT POSITIVE NOR/OR GATE

Note 3: Test Circuit



- (1) The pulse generator (PG) has the following characteristics (10% \sim 90%): t_r = 6ns, t_t = 6ns (2) The capacitance C_L includes stray wiring
- capacitance and the probe input capacitance.



MITSUBISHI HIGH SPEED CMOS

M74HC4511P/FP/DP

BCD-TO SEVEN-SEGMENT LATCH/DECODER/DISPLAY DRIVER

DESCRIPTION

The M74HC4511 is a semiconductor integrated circuit consisting of a BCD seven-segment decoder/driver.

FEATURES

- Contained latch for BCD input
- Blanking input
- High-speed: 55ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC4511 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the LSTTL.

When BCD code is applied to BCD (binary coded decimal) inputs A through D, the corresponding segment outputs a through g will become high. When each output is connected to a seven-segment display device, numeric characters are displayed as shown in the displayed character

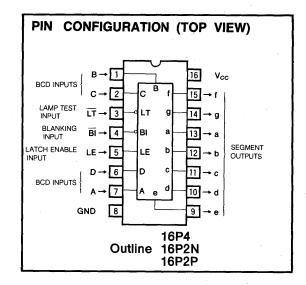
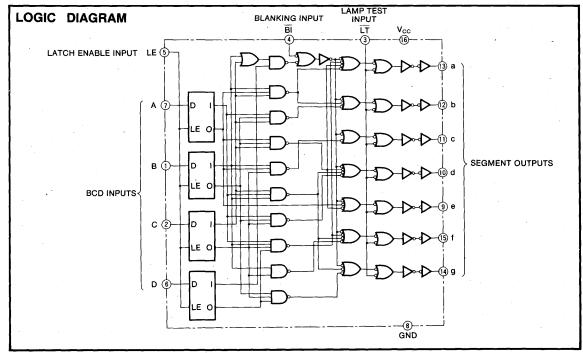


table.

When latch enable input LE changes from low-level to high-level, the signals existing immediately prior to the change at A through D will be stored in the latch. When the blanking input $\overline{B1}$ is low, a through g will become low, and display will be put out, irrespective of A through D.

When lamp test input \overline{LT} is low, a through g will become high irrespective of other inputs, and all display segments will be lighted for visual inspection.



FUNCTION TABLE (Note 1)

in the light and the first start of

				Inputs							Outputs			
Decimal value or function	LE	5	B	D	С	В	A.	а	b	C	d	Ф	1	g
0	L	Н	Н	L	L	L	L	Н	Н	Н	Н	Н	Н	L
1	L	Н	Ħ	L	L	L	Ŧ	L	I	Η	٦	١	٦	L
2	٦.	Н	Н	Ł	L	н	L	Н	Н	٦	Н	Н	Ļ	Н
3	L	н	Н	L	L	Н	Н	H	Н	H	Н	L	L	H
4	L	Н	Н	L	Н	L	L	L	Н	H	L	L	H	Н
5	L	Н	Н	L	Н	L	н	Н	L	Н	Н	L	Н	н
6	L	Н	Н	L	Н	н	L	L	L	H	H	Н	Н	H
7	L	H	Н	L	Н	H	Н	н	н	I	L	L	٦	L
8	L	Н	Н	Н	L	L	L	Н	Н	H	н	Н	Н	Ŧ
9	L	Н	Н	н	L	L	Н	Н	н	Н	L	L	H	н
10	L	Н	Н	Н	L	Н	L	L	L	L	L	L	L	L
11	L	Н	н	Н	L	Н	Н	L	L	L	L	L	L	L
12	L	н	Н	Н	Н	L	L	L	L	L	L	L	, L	L
13	L	Н	Н	H	Н	L	Н	L	L	L	٦	L	L	L
14	L	н	Н	н	н	н	L	L	L	L	L	L	L	L
15	L	н	Н	Н	. н	H	н	L	L	L	L	L	L	L
Latch	t	н	н	X	×	X	х	a ^o	þo	co	ď°	e°	f ⁰	g ^o
Blanking	×	Н	L	X	X	X	х	L	L	L	L	L	L	Ĺ
Lamp test	Х	L	X.	X	X	X	х	н	н	Н	н	Н	н	Н

Note 1 : X : Irrelevant

† : Change from low to high

 $a^0 \sim g^0$: Output state of a \sim g when latch enable pulse is applied.

Definition of character segments



DISPLAYED CHARACTERS

Decimal number	0	1	2	3 .	4	5	6	7	8	9	10	11	12	13	14	15
Displayed character	\mathbb{C}		0	3	L	Ŋ	O	7	8	ŋ		-				

ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85 \degree$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
V _I	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
	4	V ₁ < 0V	-20	
lik	Input protection diode current	V _I > V _{CC}	20	mA
		V ₀ < 0V	-20	
lok	Output parasitic diode current	Vo > Vcc	20	mA.
	0	When output is high	-35	
lo	Output current per output pin	When output is low	25	mA
	0 -1 (0)10	V _{cc}	150	
Icc	Supply/GND current	GND	-50	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		-65~+150	°C

Note 2 : M74HC4511FP, $T_a=-40\sim+70^\circ$ C and $T_a=70\sim85^\circ$ C are derated at -6mW/°C. M74HC4511DP, $T_a=-40\sim+50^\circ$ C and $T_a=50\sim85^\circ$ C are derated at -5mW/°C.



RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85 \degree C)$

				Limits		Unit
Symbol	Pai	rameter	Min	Тур	Max	Unit
Vcc	Supply voltage		2		6	>
Vı	Input voltage		0		V _{CC}	٧
Vo	Output voltage		0		Vcc	٧
Topr	Operating temperature re	ange	-40		+85	္င
		V _{CC} = 2.0V	0		1000	
t _r , t _f	Input risetime, falltime	V _{CC} = 4.5V	0		500	ns
		0		400		

ELECTRICAL CHARACTERISTICS

]			
Symbol	Parameter	Test	conditions			25℃		-40~	+85℃	Unit
)		V _{cc} (V)	Min	Тур	Max	Min	Max	}
		$V_0 = 0.1V, V_{CC}$	-0.114	2.0	1.5			1.5		
VIH	High-level input voltage			4.5	3.15			3.15	1	v
		$ I_0 = 20\mu A$		6.0	4.2			4.2	ļ	} .
		V - 0 1V V	$V_0 = 0.1V$, $V_{CC} = 0.1V$				0.5		0.5	
VIL	Low-level input voltage	, , ,	o—0.1 V	4.5			1.35		1.35	V
		$ I_0 = 20\mu A$		6.0			1.8		1.8	Ì
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
		. ' }	$I_{OH} = -20\mu A$	4.5	4.4	1		4. 4		}
VoH	High-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9	!		5.9)	V
			$I_{OH} = -6.0 \text{mA}$	4.5	4. 18			4.13]
		1	$I_{OH} = -7.8 mA$	6.0	5. 68)	5. 63		1
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
	1	1.	$I_{OL} = 20 \mu A$	4.5			0.1		0.1	{
VoL	Low-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	6.0		}	0.1		0.1	V
			I _{OL} = 4. 0mA	4.5			0.26		0.33	1
	-		I _{OL} == 5. 2mA	6.0		[0.26		0.33	Ì
I _{IH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	7 μA
I _{IL}	Low-level input current	V ₁ = 0V	V ₁ = 0V				-0.1		-1.0	μА
loc	Quiescent supply current	VI = VCC, GND	$I_0 = 0\mu A$	6.0			4.0		40.0	μΑ

SWITCHING CHARACTERISTICS ($v_{cc} = 5v$, $T_a = 25$ °C)

Symbol	Parameter	Test conditions		Unit		
Symbol	Parameter	1 est conditions	Min	Тур	Max	Unit
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time	· .			10	ns
t _{PLH}	Low-level to high-level and high-level to low-level				100	ns
tpHL	output propagation time (A~D — a~g)				100	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C _i = 15pF (Note 4)			100	ns
t _{PHL}	output propagation time (LE - a~g)	CL — 13pr (Note 4)			100	ns
t _{PLH}	Low-level to high-level and high-level to low-level			_	100	ns
t _{PHL}	output propagation time (BI — a~g)				100	ns
t _{PLH}	Low-level to high-level and high-level to low-level				100	ns
t _{PHL}	output propagation time (TT − a~g)				100	ns

SWITCHING CHARACTERISTICS $(V_{cc} = 2\sim 6V, T_a = -40\sim +85\%)$

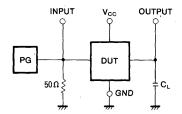
						Limits			
Symbol	Parameter	Test conditions			25℃		-40~	+85℃	Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	
			2,0			75		95	
tTLH	Low-level to high-level and	l .	4.5			- 15	· '	19	ns
	high lavel to lavel		6.0			13		16	
	high-level to low-level		2.0			75		95	
t _{THL}	output transition time		4.5			15		19	ns
	}	A Company of the Comp	6.0			. 13	į	16	
		,	2.0			600		756	
t _{PLH}	Low-level to high-level and		4.5			120	}	151	ns
	high-level to low-level		6.0			102		129	
	output propagation time		2.0			600		756	
tenL	(A~D − a~g)		4.5			120	1	151	ns
	** * *		6.0			102	1	129	
		1	2.0			600		756	
t _{PLH}	Low-level to high-level and	1	4.5	Į		120	1	151	ns
	high-level to low-level	C _L = 50pF (Note 4)	6.0			102		129	
	output propagation time	C _L = 50pr (Note 4)	2.0			600		756	
t _{PHL}	(LE — a∼g)		4.5			120	}	151	ns
			6.0			102		129	
			2.0			600		756	
t _{PLH}	Low-level to high-level and		4.5			120		151	ns
	high-level to low-level	1	6.0			102		129	
	output propagation time	l e	2.0			600		756	
t _{PHL}	(Bi — a∼g)		4.5			120		151	ns
	1		6.0	{		102		129)
		1	2.0			600		756	
t _{PLH}	Low-level to high-level and	•	4.5			120	1	151	ns
	high-level to low-level	1	6.0			102		129	
	output propagation time		2.0			600		756	
t _{PHL}	(<u>L</u> T − a~g)		4.5	[120	1	151	ns
.	1		6.0	1		102	1:	129	
Cı	Input capacitance					10		10	pF
C _{PD}	Power dissipation capacitance (Note 3)		7						- pF

Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula: $P_{D} = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$

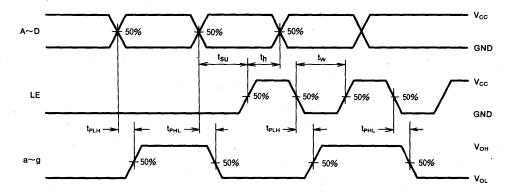
TIMING REQUIREMENTS ($v_{cc} = 2\sim6v$, $\tau_a = -40\sim+85$ °C)

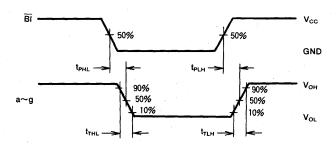
Symbol	Parameter	Test conditions			25℃		-40~	+85℃	Unit
1			V _{CC} (V)	Min	Тур	Max	Min	Max	
			2.0	80		1	101		
tw	LE pulse width		4.5	16			20	1.0	ns
]		·	6.0	14			17	•	
			2.0	100		2.0	126		
tsu	A~D setup time with	• • • •	4.5	20		100	25		ns
<u> </u>	respect to LE		6.0	17			21		
			2.0	0			0		
t _h	A~D hold time with		4.5	0			0		ns
	respect to LE	4.0	6.0	0			0		

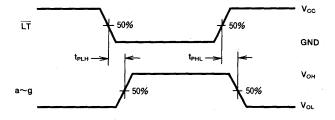
Note 4: Test Circuit



- (1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns (2) The capacitance C_i includes stray wiring
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.







MITSUBISHI HIGH SPEED CMOS

M74HC4514P/FP/DWP

1-OF-16 DECODER/DEMULTIPLEXER WITH ADDRESS LATCH("H" LEVEL OUTPUT)

DESCRIPTION

The M74HC4514 is a semiconductor integrated circuit consisting of a 4-bit binary to 16-line decoder/demultiplexer with address latch.

FEATURES

- High-speed: 24ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2∼6V
- Wide operating temperature range: Ta=-40~+85℃

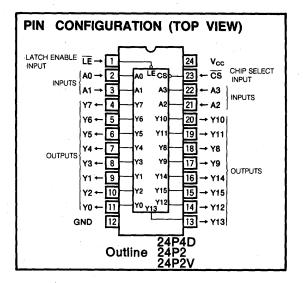
APPLICATION

General purpose, for use in industrial and consumer digital equipment. $^{\prime}$

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC4514 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the LSTTL.

The M74HC4514 consists of a 4-bit binary to 16-line decoder/demultiplexer with an address latch to store the signals of inputs A0 through A3. When latch-enable input $\overline{\text{LE}}$ is high, a 4-bit binary code, applied to inputs A0 through A3, goes through the latch and will become a decoder input signal, the corresponding output Y0 through Y15 will be-



come high, and all the other outputs will become low. When $\overline{\text{LE}}$ is low, the signals existing immdiately prior to the change at A0 through A3 will be stored in the latch, and the latch contents do not change even if A0 through A3 are changed. In this case, chip select input $\overline{\text{CS}}$ is maintained low. When $\overline{\text{CS}}$ is high, Y0 through Y15 all will become low. When operated as a 1-of-16 demultiplexer, $\overline{\text{CS}}$ is used as the data input and A0 through A3 are used as the select inputs.

FUNCTION TABLE (Note 1)

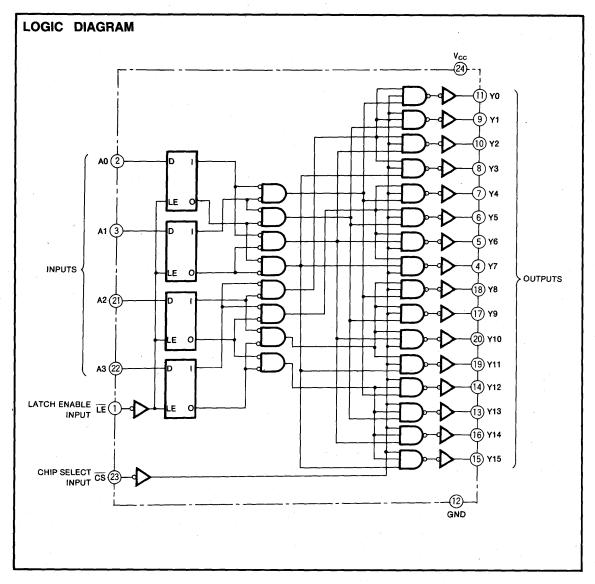
		Inp	uts										Out	puts							
LE	S	A3	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8	Y9	Y10	Y11	Y12	Y13	Y14	Y15
Н	با	اد	Ц	L	٦	Н	L	٦	u	٦	ŗ	L	L	L	<u>.</u>	L	L	L	L	L	L
Н	L	L	L	L	Н	L	н	L	L	L	L	L	L	L	الـ	L	L	L	L	L	L
Н	٦	L	١	Н	L	L	L	Τ	٦	L	L	L	L	L	Ļ	L	L	L	L	L	L
Н	L	L	L	Н	Н	L	L	L	H	L	L	L	L	L	٦	L	L	L	L	L	L
Н	اد	L	Ι	L	٦	L	L	ب	١	Ĥ	۲	L	٦	L	اد	L	L	L	٦	L	L
H	L	٦	Н	L	н	L	L	L	L	L	Н	L	L	L	٦	L	L	L	L	L	L.
Н	L	L	Н	Н	L	L	L	L	٦	L	L	н	L	L	L	L	L	L	L	L	L
Н	L	L	Н	Н	Н	L	L	L	٦	L	٦	L	Н	L	٦	L	L	L	L	L	L_
Н	٦	Ι	اد	L	٦	L	L	L	۲	, L	L	L	L	Н	١	L	L	L	L	L	L
Н	L	Ι	١	L	Η	L	L	L	٦	L	٦	L	٦	L	Η	L	L	L	L	L	L
Н	L	H	٦	Н	L	L	L	L	يا	L	L	L	L	L	L	Н	L	L	L	L	L
Н	L	Τ	L	н	Н	L	Ĺ	L	L	L	L	L	L	L	L	L	Н	L	L	L	L
н	L	I	Ι	L	٤	٦	L	L	٦	L	L	L	٦	L	٦	L	L	Н	L.	L	L
Н	L	I	I	L	Η	١	L	L	٦	L	٦	L	٦	L	L	L	L	L	Н	L	L
Н	L	Τ	I	Н	ب	L	L	L	٦	L	L	L	L	L	L	L	L	L	L	Н	L
Н	L.	Н	Н	Н	Н	L	L	L	L	L	L	L	L	L	.L	L	L	L	L	L	Н
х	н	X	Х	X	Х	L	L	Ĺ	Ĺ	L	L	L	L	L	L	· L′	L	L	L	L	L
L	L	X	X	Х	Х	Y0º	Y10	Y20	Y30	Y4 ⁰	Y5 ⁰	Y60	Y70	Y8°	Y9°	Y10 ⁰	Y110	Y120	Y130	Y140	Y15°

Note 1 : X : Irrelevant

Yº : Output state Y before LE change to low-level



1-OF-16 DECODER/DEMULTIPLEXER WITH ADDRESS LATCH("H" LEVEL OUTPUT)



ABSOLUTE MAXIMUM RATINGS ($\tau_a = -40 \sim +85^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
V ₁	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
•		V ₁ < 0V	-20	T
(IK	Input protection diode current	V _I > V _{CC}	20	mA
		V ₀ < 0V	-20	
юк	Output parasitic diode current	$V_{o} > V_{cc}$	20	mA
lo	Output current per output pin		±25	mA
Icc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		-65~+150	င

Note 2 : M74HC4514FP, T_a = $-40\sim+80^\circ$ C and T_a = $80\sim85^\circ$ C are derated at -7mW/°C. M74HC4514DWP, T_a = $-40\sim+80^\circ$ C and T_a = $80\sim85^\circ$ C are derated at -7mW/°C.



1-OF-16 DECODER/DEMULTIPLEXER WITH ADDRESS LATCH("H" LEVEL OUTPUT)

RECOMMENDED OPERATING CONDITIONS $(T_a = -40 \sim +85^{\circ}C)$

Symbol			Limits					
Symbol	Pai	rameter	Min	Тур	Max	Unit		
Vcc	Supply voltage		2		6	V		
Vı	Input voltage	0		Vcc	V			
Vo	Output voltage	0		Vcc	V			
Topr	Operating temperature ra	inge	-40		+85	°C		
	Input risetime, falltime	$V_{CC} = 2.0V$	0	1	1000			
t _r , t _f		$V_{CC} = 4.5V$	0	0		ns		
		$V_{CC} = 6.0V$	0					

ELECTRICAL CHARACTERISTICS

					Limits					
Symbol	Parameter	Test	Test conditions $V_{CC}(V)$			25°C		-40~+85℃		Unit
						Тур	Max	Min	Тур	
		V =0.1V V	$V_0 = 0.1V, V_{CC} = 0.1V$					1.5		
V_{IH}	High-level input voltage	$ I_0 = 20\mu A$;0.1 v	4.5	3.15			3.15		V
		1101 - 20μΑ	$ 1_0 = 20\mu\text{A}$				1	4.2	!	
		$V_{0} = 0.1V, V_{00}$	0.11/	2.0			0.5		0.5	
V_{IL}	Low-level input voltage $ I_0 = 20\mu A$	1	5-0.1 V	4.5			1.35		1.35	V
		1101 = 20µA	1101 — 20μΑ				1.8	1	1.8	
	High-level output voltage		$I_{OH} = -20\mu A$	2.0	1.9			1.9		
			$I_{OH} = -20\mu A$	4. 5	4. 4			4.4	1	
V_{OH}		$V_{i} = V_{iH}, V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9			5.9		V
			$I_{OH} = -4.0 \text{mA}$	4.5	4. 18		,	4. 13		ĺ
			$I_{OH} = -5.2 \text{mA}$	6.0	5.68			5.63		}
-			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
	1		$I_{OL} = 20 \mu A$	4.5			0.1		0.1	
VOL	Low-level output voltage	$V_I = V_{IH}, V_{IL}$	$I_{OL} = 20 \mu A$	6.0		,	0.1	j	0.1	V
			I _{OL} = 4.0mA	4.5			0.26		0.33	}
		*	I _{OL} = 5. 2mA	6.0			0. 26		0.33	
Цн	high-level input current	V ₁ = 6V		6.0			0.1		1.0	
l _{IL}	Low-level input current	V ₁ = 0V	$V_1 = 0V$				-0.1		-1.0	μА
Icc	Quiescent supply current	VI = VCC, GND	$l_0 = 0 \mu A$	6.0			4.0		40.0	μΑ

SWITCHING CHARACTERISTICS $(v_{cc} = 5v, T_a = 25^{\circ})$

		T-Adist		Unit		
Symbol	Parameter	Test conditions	Min	Тур	Max	Offic
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time				10	ns
t _{PLH}	Low-level to high-level and high-level to low-level				30	ns
t _{PHL}	output propagation time (CS - Y)	C _L = 15pF (Note 4)			30	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C[= 15pr (Note 4)			40	ns
t _{PHL}	output propagation time (A — Y)				30	ns
t _{PLH}	Low-level to high-level and high-level to low-level				40	ns
t _{PHL}	output propagation time (LE - Y)				30	ns

1-OF-16 DECODER/DEMULTIPLEXER WITH ADDRESS LATCH("H" LEVEL OUTPUT)

SWITCHING CHARACTERISTICS ($V_{cc} = 2\sim 6V$, $T_a = -40\sim +85\%$)

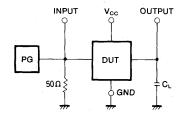
						Limits			
Symbol	Parameter	Test conditions			25℃		−40 ~	+85°C	Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	L
			2.0			75		95	
t _{TLH}	Low-level to high-level and		4.5			15		19	ns
	high-level to low-level		6.0			13		16	
	nigh-level to low-level		2.0			75		95	
t _{THL}	output transition time		4.5			15		19	ns
			6.0			13		16	
]	2.0			175		221	
t _{PLH}	Low-level to high-level and		4.5			35		44	ns
	high-level to low-level		6.0			30		37	
	output propagation time		2.0			175		221	
t _{PHL}	(CS - Y)		4.5	ļ.	1	35		44	ns
		0 = 50=5 (N=4=4)	6.0		-	30		37	
		$C_L = 50 pF \text{ (Note 4)}$	2.0			230		290	
tPLH	Low-level to high-level and		4.5	İ		46		58	ns
	high-level to low-level		6.0	ĺ	1	39		49	
	output propagation time		2.0			175		221	
t _{PHL}	(A - Y)		4.5			35	}	44	ns
		•	6.0			30	,	37	
		1	2.0			230		290	
t _{PLH}	Low-level to high-level and		4.5			46		58	ns
	high-level to low-level		6.0			39		49	
	output propagation time		2.0			175		221	
t _{PHL}	(LE - Y)		4.5		1	35		44	ns
			6.0	}		30		37	
Cı	Input capacitance					10		10	pF
C _{PD}	Power dissipation capacitance (Note 3)								pF

Note 3 : CPD is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS ($v_{cc} = 2\sim6v$, $T_a = -40\sim+85^{\circ}C$)

Symbol	Parameter	Test conditions			25°C		-40~	+85℃	Unit
Ì			V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0	80			101	-	
tw	LE pulse width		4.5	16	}		20	1	ns
ļ.			6.0	14	}		17		
			2.0	100			126		
tsu	A setup time with respect to LE		4.5	20			25		ns
ļ	respect to LE		6.0	17			21	1	
	A b -1 d A		2.0	5			5		
th	A hold time with		4.5	. 5	1		5	1	ns
	respect to LE		6.0	5			5 .		

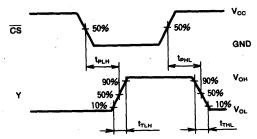
Note 4: Test Circuit

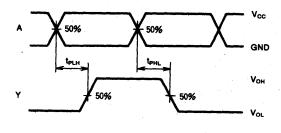


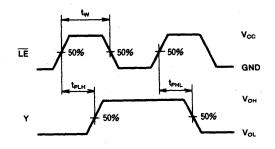
- (1) The pulse generator (PG) has the following
- characteristics (10%~90%): t_f = 6ns, t_f = 6ns (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

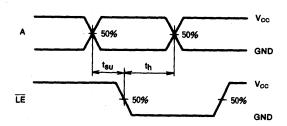
MT4HC4514P/FP/DWP

1-OF-16 DECODER/DEMULTIPLEXER WITH ADDRESS LATCH("H" LEVEL OUTPUT)











MITSUBISHI HIGH SPEED CMOS

M74HC4515P/FP/DWP

1-OF-16 DECODER/DEMULTIPLEXER WITH ADDRESS LATCH("L" LEVEL OUTPUT)

DESCRIPTION

The M74HC4515 is a semiconductor integrated circuit consisting of a 4-bit binary to 16-line decoder/demultiplexer with address latch.

FEATURES

- High-speed: 24ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=-40~+85℃

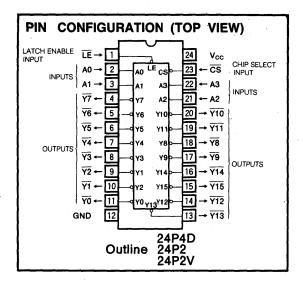
APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC4515 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the LSTTL.

The M74HC4515 consists of a 4-bit binary to 16-line decoder/demultiplexer with an address latch to store the signals of inputs A0 through A3. When latch enable input $\overline{\text{LE}}$ is high, a 4-bit binary code, applied to inputs A0 through A3, goes through the latch and will become a decoder input signal, the corresponding output $\overline{\text{Y0}}$ through $\overline{\text{Y15}}$ will become low and all the other outputs will become high. When $\overline{\text{LE}}$ is high, the signals existing immediately prior to the change at A0 through A3 will be stored in the latch, and the



latch contents do not change even if A0 through A3 are changed. In this case, chip select input $\overline{\text{CS}}$ is maintained low.

When \overline{CS} is high, $\overline{Y0}$ through $\overline{Y15}$ all will become high. When operated as a 1-of-16 demultiplexer, \overline{CS} is used as the data input and A0 through A3 are used as the select inputs.

FUNCTION TABLE (Note 1)

		Inp	uts										Out	puts						-	
LE	CS	А3	A2	A1	A0	YO	Y1	Y2	Y3	Y4	Y5	Y6	¥7	Y8	Y9	Y10	Y11	Y12	Y13	Y14	Y15
Н	7	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	_Н_
н	٦	L	L	L	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
Н	٦	L	L	Н	L	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	н	Н	H	н	н
Н	٦	Ļ	L	Н	Н	Н	Н	н	L	Н	Н	Н	Н	H	Н	Н	Н	Н	Н	Н	Н
Н	۲	4	Н	L	L	Н	I	Н	Н	L	Н	Н	Н	H	Н	Н	Н	Н	Н	Н	Н
Н	۲	٦	Н	L	н	Н	I	н	Н	Н	· L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
Н	٦	4	H	Н	L	Н	Ι	Н	Н	Ι	Н	L	Н	Н	Н	Н	н	Н	Н	Н	Н
Н	٤	L	Н	Н	Н	Н	I	н	Н	Н	Н	н	L	Η	Н	Н	Н	Н	Н	Н	Н
H	L	I	L	L	L	Н	Н	н	Н	Н	Н	Н	Н	L	Н	н	Н	Н	Н	Н	Н
Н	L	I	L	L	Н	Н	Ŧ	Н	Н	Н	Н	Η.	Н	Н	L	Н	н	Н	Н	Н	Н
Н	L	I	L	Н	L	Н	H	Н	Н	Н	Н	Н	Н	Ή	Н	L	Н	Н	Н	Н	Н
Н	٦	I	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	Н	Н	Н
Н	L	I	Н	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	Н	Н
Н	L	I	H	L	Н	Н	Η	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	H
Н	L	Н	Н	Н	L	H.	Н	Н	Н	н	Н	Н	Н	Η.	Н	Н	Н	Н	Н	L	Н
Н	L	I	Н	Н	· H	Н	Ι	Н	Н	Ι	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L
Х	н	X	X	Х	Х	Н	Ξ	Н	Н	Н	Н	Н	Н	H	Н	Н	Н	Н	н	Н	Н
L	L	Х	Х	X	X	Y0°	Y10	Y20	Y30	Y40	Y50	Y60	Y70	Y80	Y90	Y10°	Y110	Y120	Y130	Y140	Y150

Note 1 : X : Irrelevant

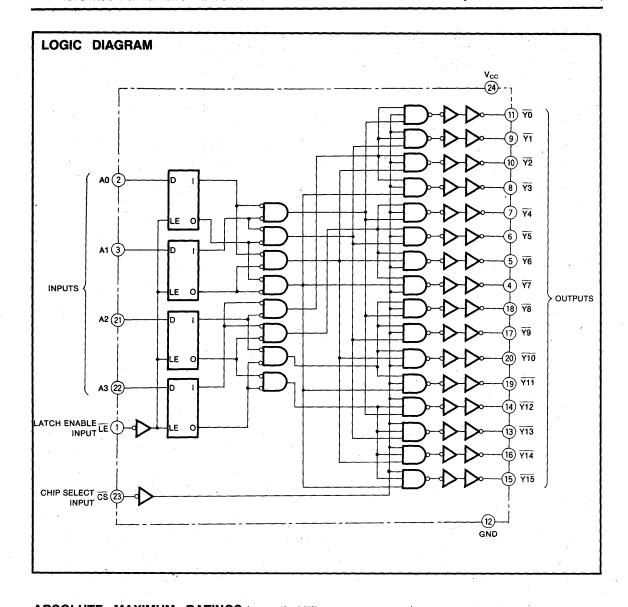
Yo : Output state Y before LE changed to low-level

M74HC4515P/FP/DWP

1:0F-16 DECODER/DEMULTIPLEXER WITH ADDRESS LATCH("L" LEVEL OUTPUT)

可能的效益。影響實際的學術與影響。 不能不能被發展的

公司的政策等 经济建筑的特别



ABSOLUTE MAXIMUM RATINGS ($\tau_a = -40 \sim +85$ °C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V _{cc}	Supply voltage		-0.5~+7.0	V
Vı	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
	h	V ₁ < 0V	20	
l _{IK}	Input protection diode current	V _I > V _{CC}	20	mA
		V ₀ < 0V	-20	
lok	Output parasitic diode current	V _o > V _{cc}	20	mA
lo	Output current per output pin		±25	mA
Icc	Supply/GND current	V _{CC} , GND	±50	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		-65~ + 150	°C

Note 2 : M74HC4515FP, T_a = $-40\sim+80$ °C and T_a = $80\sim85$ °C are derated at -7mW/°C. M74HC4515DWP, T_a = $-40\sim+80$ °C and T_a = $80\sim85$ °C are derated at -7mW/°C.



1-OF-16 DECODER/DEMULTIPLEXER WITH ADDRESS LATCH("L" LEVEL OUTPUT)

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85\%)$

Cumbal	De				11-14	
Symbol	Pal	rameter	Min	Тур	Max	Unit
Vcc	Supply voltage		2		6	V
Vı	Input voltage		0		Vcc	V
Vo	Output voltage		0		Vcc	V
Topr	Operating temperature ra	ange	-40		+85	င
		$V_{CC} = 2.0V$	0		1000	
tr, tr	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns
		$V_{CC} = 6.0V$. 0		400	

ELECTRICAL CHARACTERISTICS

					,		Limits		, , , , , , , , , , , , , , , , , , , ,	
Symbol	Parameter	Test	conditions			25°C		-40~	+85℃	Unit
				V _{cc} (V)	Min	Тур	Max	Min	Max	
		$V_0 = 0.1V, V_{CC}$	_0 1v	2.0	1.5			1.5		
VIH	High-level input voltage	$ V_0 = 0.1V$, V_{CO}	;0.1 V	4.5	3.15			3, 15		v
		1101 - 20µA		6.0	4.2			4.2		
		$V_0 = 0.1V, V_{cc}$	0.11/	2.0			0.5		0.5	
VIL	Low-level input voltage	$ V_0 = 0.1V$, V_{CO}	;—0. 1 V	4.5]	1.35		1.35	V
		1101 - 20µA		6.0			1.8	1	1.8	
			$I_{OH} = -20\mu A$	2.0	1.9			1.9		
		1	$I_{OH} = -20\mu A$	4.5	4.4	İ		4.4		
V _{OH}	High-level output voltage	$V_i = V_{iH}, V_{iL}$	$I_{OH} = -20\mu A$	6.0	5.9	1		5.9		v
		1	$i_{OH} = -4.0 \text{mA}$	4.5	4. 18			4. 13		
	1		$I_{OH} = -5.2 mA$	6.0	5. 68	1		5, 63		
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
	\		$I_{OL} = 20 \mu A$	4.5			0, 1		0.1	
V _{OL}	Low-level output voltage	$V_{I} = V_{IH}, V_{IL}$	$I_{OL} = 20 \mu A$	6.0			0.1	i	0.1	V
		1	I _{OL} = 4.0mA	4.5			0.26		0.33	1
			I _{OL} = 5. 2mA	6.0			0. 26		0.33	
I _{ін}	High-level input current	V ₁ = 6V		6.0		/	0.1		1.0	μA
I _I L	Low-level input current	V ₁ = 0V		6.0			-0.1		-1.0	μA
lcc	Quiescent supply current	VI = VCC, GND	$I_0 = 0 \mu A$	6.0			4.0		40.0	μА

SWITCHING CHARACTERISTICS $(v_{cc} = 5v, T_a = 25^{\circ}C)$

		T4		Limits		Unit
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
tTHL	output transition time				10	ns
t _{PLH}	Low-level to high-level and high-level to low-level	,			30	ns
t _{PHL}	output propagation time $(\overline{CS} - \overline{Y})$	C ₁ = 15pF (Note 4)			30	ns
t _{PLH}	Low-level to high-level and high-level to low-level	CL — 15pF (Note 4)			40	ns
t _{PHL}	output propagation time $(A - \overline{Y})$				30	ns
t _{PLH}	Low-level to high-level and high-level to low-level		,		40	ns
t _{PHL}	output propagation time $(\overline{LE} - \overline{Y})$				30	ns

1-OF-16 DECODER/DEMULTIPLEXER WITH ADDRESS LATCH("L" LEVEL OUTPUT)

SWITCHING CHARACTERISTICS ($V_{cc} = 2\sim 6V$, $T_a = -40\sim +85^{\circ}C$)

5.1 (1840.2) 整数数字字 (如::\$P\$ (1945) (1945)

教学(44) 2. 意识(1.00) 48(1.1)

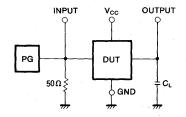
		1				Limits			}
Symbol	Parameter	Test conditions			25℃		40~	+85℃	Unit
			V _{CC} (V)	Min	Тур	Max	Min	Max	
			2.0			75		95	
t _{TLH}	Low-level to high-level and	the second	4.5	. !		15	l	19	ns
	high level to leve level		6.0			13		- 16	
	high-level to low-level		2.0			75		95	
t _{THL}	output transition time	1	4.5			15		19	ns
			6.0			13	1	16	
			2.0			175		221	
t _{PLH}	Low-level to high-level and		4.5		!	35		44	ns
	high-level to low-level		6.0			30		37	
	output propagation time		2.0			175		221	
t _{PHL}	$(\overline{CS} - \overline{Y})$		4.5			35		44	ns
		C _L = 50pF (Note 4)	6.0			30		37 ·	
		- C _L = 50pr (Note 4)	2.0			230		290	
t _{PLH}	Low-level to high-level and		4.5			46		58	ns
	high-level to low-level	(contraction of the contraction	6.0			39	11.5	49	
	output propagation time	\	2.0			175		221	
t _{PHL}	$(A-\overline{Y})$	1	4.5			35		44	ns
		1	6.0		Ì	30		37	
		1	2. 0			230		290	
t _{PLH}	Low-level to high-level and	\	4.5			46		58	ns
	high-level to low-level		6.0			39		49	
	output propagation time	1	2.0		·	175		221	
t _{PHL}	$(\overline{LE} - \overline{Y})$	1	4.5			35	ŀ	44	ns
		1	6.0			30		37	
Cı	Input capacitance		1			10		10	pF
CPD	Powerdissipation capacitance (Note 3)								pF

Note 3 : CPD is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS ($v_{cc} = 2\sim 6V$, $T_a = -40\sim +85^{\circ}C$)

						Limits			
Symbol	Parameter	Test conditions			25℃		−40~	+85℃	Unit
			V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0	. 80			101		
tw	LE pulse width	i e	4.5	16			20		ns
		•	6.0	14			17		
,	A cotor time visits		2.0	100			126		
t _{su}	A setup time with		4.5	20			25		ns
	respect to LE	· · · · · · · · · · · · · · · · · · ·	6.0	17			21		
	A b and Aires a solution		2.0	5			5		1
t _h	A hold time with	" ·	4.5	. 5			5		ns
	respect to LE		6.0	5			- 5		

Note 4: Test Circuit



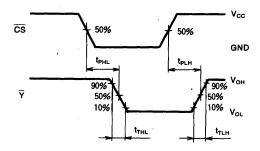
⁽¹⁾ The pulse generator (PG) has the following characteristics (10% \sim 90%): $t_{\rm f}=6{\rm ns},\,t_{\rm f}=6{\rm ns}$ (2) The capacitance C_L includes stray wiring

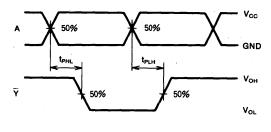
capacitance and the probe input capacitance.

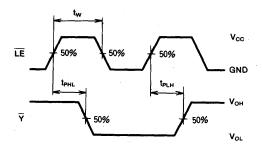
MT4HC4515P/FP/DWP

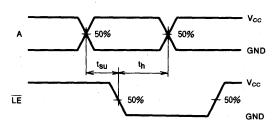
1-OF-16 DECODER/DEMULTIPLEXER WITH ADDRESS LATCH("L" LEVEL OUTPUT)

TIMING DIAGRAM











MITSUBISHI HIGH SPEED CMOS

M74HC4538P/FP/DP

DUAL PRECISION MONOSTABLE MULTIVIBRATOR (RETRIGGERABLE RESETTABLE)

DESCRIPTION

The M74HC4538 is a semiconductor integrated circuit, consisting of two retriggerable monostable multivibrators with direct reset inputs.

FEATURES

- Retriggerable multivibrator can generate wide output pulses.
- Direct reset input can interrupt output pulses.
- High speed: 30ns typ. (C₁=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{cc}=2~6V
- Wide operating temperature range: Ta=−40~+85°C

APPLICATION

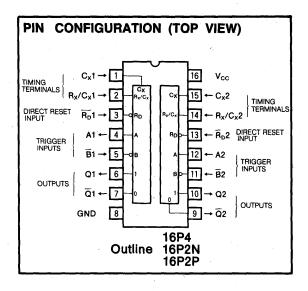
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC4538 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the LSTTL.

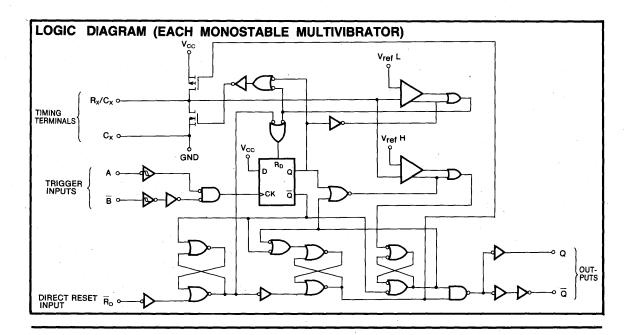
Trigger input with built-in Schmitt trigger circuit prevents the occurrence of incorrect oscillations even when input signals having slow rise and fall times are applied.

When external resistor R_X and electrostatic capacitor C_X are connected to timing terminals R_X/C_X and C_X as shown



in Fig. 1, and trigger pulses are applied at input A or \overline{B} , positive pulses will appear at Q and negative pulses, at \overline{Q} . (Fig.2-(a)) The pulse width t_{WQ} is set by R_X and C_X . The trigger is applied when A changes from low-level to highlevel or when \overline{B} changes from high-level to low-level. The retrigger function is used to obtain longer pulse width and output pulses can be extended by retriggering at A or \overline{B} before the output pulse is completed. (Fig.2-(b)).

When direct reset input $\overline{R_D}$ is low, Q will be reset low and \overline{Q} will be reset high, irrespective of the output state, allowing output pulses to be narrower by R_D . (Fig.2-(c)).





DUAL PRECISION MONOSTABLE MULTIVIBRATOR (RETRIGGERABLE RESETTABLE)

FUNCTION TABLE (Note 1)

	Inputs		Out	puts
_ A	B	R _D	Q	Q
†	Н	Н	Л	П
х	L ·	Н	L	Н
н	×	н	L	Н
L	1	Н	Л	L
×	X	L	L	Н

Note 1: X: Irrelevant

Change from low to high level

☐: Negative one-shot operation

OPERATION

1. How to use the timing terminals

Resistor R_X and capacitor C_X are connected to timing terminals R_X/C_X and C_X , as shown in Fig. 1. If C_X is polar, the positive lead should be connected to the R_X/C_X side, and the negative lead to the C_X side. A diode is connected to prevent latchup.

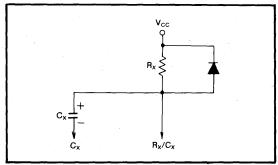


Fig.1 Connection of external resistor R_X and capacitor C_X to timing terminals C_X and R_X/C_X

2. Output pulse width two

The output pulse width t_{WQ} is determined as follows: When $C_X>100000pF$, $R_X\geqq10k\Omega$ $t_{WQ}=0.72$ $C_X{}^{\bullet}R_X$ (ns)

 C_x is givin in pF, and R_x in $k\Omega$.

3. Output pulse width control

The output pulse width can be controlled in the following three ways.

3-1 Normal use

Fig.2-(a) is the directions as ordinary monostable multi-vibrator operation and the output pulse width t_{WQ} can be set by using the formula and figure shown in section 2 above.

3-2 Extention of the output pulse width with retrigger function

As shown in Fig.2-(b), the output pulse width can be extended at will by applying additional trigger pulses before the output pulse is completed.

3–3 Shortening of the output pulse width with $\overline{R_D}$ signal As shown in Fig.2-(c), the output pulse which has been generated by the trigger signal can be terminated with the $\overline{R_D}$ signal and it is possible to shorten its width as required.

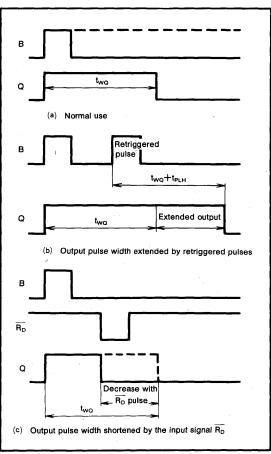


Fig.2 Output pulse width contorl

MT4HC4538P/FP/DP

DUAL PRECISION MONOSTABLE MULTIVIBRATOR (RETRIGGERABLE RESETTABLE)

4. Precautions for use

- 4-1 Additional trigger pulses must be applied at least t_{fr} later after the previous trigger pulse has been applied. The retrigger pulse during this period is ineffective.
- 4-2 The lead lengths of external resistor R_X and capacitor C_X should be as short as possible (less than 3cm) to minimize stray wiring capacitance and to prevent misoperation due to noise. Care should also be taken to isolate this circuit from noise sources as far as possible.
- 4-3 Insert a capacitor of $0.01\sim0.1\mu F$ with good high-frequency characteristics between V_{CC} and GND.
- 4-4 Output pulses may be generated when power is switched on.
- 4-5 Capacitor discharge when the power is turned off may cause thermal breakdown or latchup, so a diode should be connected as shown in Fig. 1.





M74HC4543P/FP/DP

PRELIMINAR **BCD-TO SEVEN-SEGMENT** LATCH/DECODER/DISPLAY DRIVER FOR LIQUID-CRYSTAL DISPLAYS

DESCRIPTION

The M74HC4543 is a semiconductor integrated circuit consisting of a seven-segment BCD decoder/driver, enable to drive liquid-crystal displays.

FEATURES

- Contained latch for BCD input
- Blanking input
- High-speed: 45ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20µW/package, max (V_{CC}=5V, T_a=25°C, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: Ta=-40~+85℃

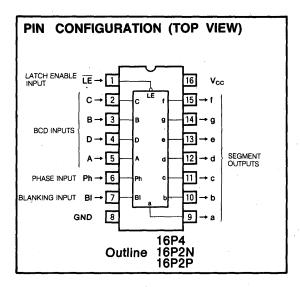
APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

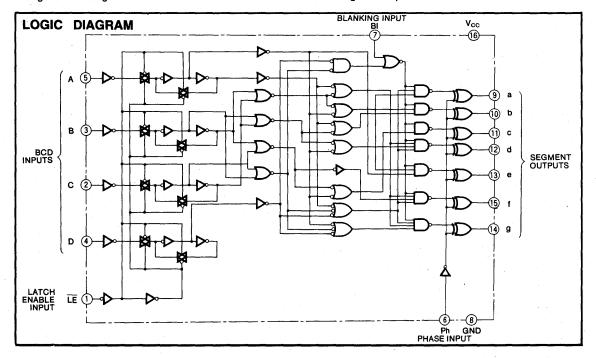
When BCD code is applied to BCD (binary coded decimal) inputs A through D, the corresponding segment outputs a through g will become high. When each output is connected to a seven-segment display device, numeric characters are displayed as shown in the displayed character

When latch enable input LE changes from high-level to low-level, the signals existing immediately prior to the change at A through D will be stored in the latch. When



blanking input B1 is high, a~g will become low irrespective of A through D, and display will be put out.

When phase input Ph is high, outputs a through g will be changed. To drive a liquid-crystal display device, the common square wave signal must be applied to Ph and the common backplane of display device. (See Application Example.) To drive other display devices, Ph must be set to low or high, and additional components must be connected to the segment outputs to increase the drive current.



BCD-TO SEVEN-SEGMENT LATCH/DECODER/DISPLAY DRIVER FOR LIQUID-CRYSTAL DISPLAYS

FUNCTION TABLE (Note 1)

				Inputs							Outputs			
Decimal value or function	LE	Ph	ВІ	D	С	В	Α	а	b	С	d	е	f	g
0	н.	Ŀ	L	L	Ŀ	L	L	Н	Н	Н	Н	н	н	L
1	н	L	L	L	L	L	Н	L	Н	Н	L	L	L	L
2	Н	L	L	L	L	Н	L	Н	н	L	Н	Н	L	н
3	Н	L	L	L	L	H.	Н	Н	Н	Н	Н	L	L	н
4	H.	L	L	L	Н	L	L	L	Н	Н	L	Ŀ	н	Н
5	Н	L	L	L	Н	L	Н	н	L	Н	Н	L	н	Н
6	н	L	L	L	Н	Н	L	Н	L	Н	Н	н	I	н
7	Н	L	L	L	Н	н	H,	н	Н	Н	L	L	L	L
8	Н	L	L	Н	L	L	L	Н	Н	Н	Н	Н	Н	н
9	Fi	L	L	Н	L	L:	Н	Н	Н	н	Н	L	н	Н
10	Н	L	L	Н	L	Н	L	L	L	L	L	L	L	L
11	Н	L	L	Н	L	Н	Н	L	L	L	L	L	L	L
12	Н	L	L	Н	Н	L	L	L	L	L	L	L	L	L
13	Н	L	L	Н	Н	L	Н	L	L	L	L	L	L	L
1.4	Н	L	L	Н	Н	Н	L	L	L	L	L	L	L	L
15	Н	L	L	Н	Н	н	Н	L	L	L	L	L	L	L
Latch	L	L	L	х	X	х	х	a ^o	þ°	c ⁰	ď	e ⁰	f ⁰	g ^o
Blanking	Х	L	Н	х	х	Х	х	L	L	L	L	L	L	L
DITTO	†	Н	†			†		The ou	tput leve	ls show	above	are inve	ted.	

Note 1: X : Irrelevant

a⁰~g⁰ : Output state of a~g when latch enable pulse is applied.

† : Same combination as above

Definitions of character segments



DISPLAYED CHARACTERS

Decimal value	0	1	2	3	4	5	6	7	.8	9	10	11	12	13	14	15
Displayed character		1	5	3	7	U)	O	7	8	٩						

ABSOLUTE MAXIMUM RATINGS $(T_a = -40 \sim +85 \degree)$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5~+7.0	V
V ₁	Input voltage		-0.5~V _{cc} +0.5	V
Vo	Output voltage		-0.5~V _{cc} +0.5	V
		V ₁ < 0V	-20	
l _{IK}	Input protection diode current	V _I > V _{CC}	20	mA
		V ₀ < 0V	-20	
ок	Output parasitic diode current	$V_0 > V_{CC}$	20	mA
10	Output current per output pin		±25	mA
Icc	Supply/GND current	V _{CC} , GND	±50	·mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		-65~+150	౮

Note 2 : M74HC4543FP, $T_a=-40\sim+70^\circ\text{C}$ and $T_a=70\sim85^\circ\text{C}$ are derated at -6mW/°C. M74HC4543DP, $T_a=-40\sim+50^\circ\text{C}$ and $T_a=50\sim85^\circ\text{C}$ are derated at -5mW/°C.

BCD-TO SEVEN-SEGMENT LATCH/DECODER/DISPLAY DRIVER FOR LIQUID-CRYSTAL DISPLAYS

RECOMMENDED OPERATING CONDITIONS $(\tau_a = -40 \sim +85 ^{\circ}C)$

0				Limits		Unit
Symbol	Pa	rameter	Min	Тур	Max	Unit
V _{CC}	Supply voltage		2	- /	6	٧
V,	Input voltage		0	,	Vcc	V
v _o	Output voltage		0		Vcc	٧
Topr	Operating temperature ra	ange	-40		+85	°C
		$V_{CC} = 2.0V$	0		1000	
t _r , t _f	Input risetime, falltime	$V_{CC} = 4.5V$	0		500	ns
		$V_{CC} = 6.0V$	0		400	

ELECTRICAL CHARACTERISTICS

					Limits					Unit
Symbol	Parameter	Test conditions V _{CC} (V)		25°C			-40~+85℃			
				V _{cc} (V)	Min	Тур	Max	Min	Max	
V _{IH}	High-level input voltage	$V_0 = 0.1V, V_{CC} = 0.1V$ $ I_0 = 20\mu A$		2.0	1.5			1.5		
				4.5	3. 15			3. 15	!	٧
				6.0	4. 2			4.2		
VIL	Low-level input voltage	$V_0 = 0.1V, V_{CC} - 0.1V$ $ I_0 = 20\mu A$		2.0			0.5		0.5	
				4.5			1. 35		1.35	V
				6.0			1.8		1.8	
	High-level output voltage	$V_{l} = V_{lH}, \ V_{lL}$	$I_{OH} = -20\mu A$	2.0	1.9			1.9		
			$I_{OH} = -20\mu A$	4.5	4.4			4.4		v
VoH			$I_{OH} = -20 \mu A$	6.0	5.9			5.9		
			$I_{OH} = -0.4 \text{mA}$	4.5	3. 98		′	3. 84		
	-		$I_{OH} = -0.52 \text{mA}$	6.0	5. 48			5. 34		
			$I_{OL} = 20 \mu A$	2.0			0.1		0.1	
V _{OL}		$V_i = V_{iH}, V_{iL}$	$I_{OL} = 20 \mu A$	4.5			0.1		0.1	
	Low-level output voltage		$i_{OL} = 20 \mu A$	6.0			0.1		0.1	V
			I _{OL} = 0.4mA	4.5			0. 26		0.33	
			$I_{OL} = 0.52 \text{mA}$	6.0			0.26		0.33	
I _{IH}	High-level input current	V ₁ = 6V		6.0			0.1		1.0	μΑ
I _{IL}	Low-level input current	$V_i = 0V$		6.0			-0.1		-1.0	μA
Icc	Quiescent supply current	$V_i = V_{CC}$, GND	$I_{0} = 0 \mu A$	6.0			4.0		40.0	μΑ

SWITCHING CHARACTERISTICS $(V_{CC} = 5V, T_a = 25^{\circ}C)$

Symbol	Parameter	Test conditions		Limits		
	r ai dilletei	rest conditions	Min	Тур	Max	Unit
t _{TLH}	Low-level to high-level and high-level to low-level				10	ns
t _{THL}	output transition time				10	ns
t _{PLH}	Low-level to high-level and high-level to low-level]			66	ns
t _{PHL}	output propagation time $(A\sim D-a\sim g)$	*			66	ns
t _{PLH}	Low-level to high-level and high-level to low-level	C _L = 15pF (Note 4)			66	ns
t _{PHL}	output propagation time (LE - a~g)				66	ns
t _{PLH}	Low-level to high-level and high-level to low-level	1			41	ns
t _{PHL}	output propagation time (BI — a~g)				41	ns
t _{PLH}	Low-level to high-level and high-level to low-level	1			30	ns
t _{PHL}	output propagation time (Ph — a∼g)				30	ns

BCD-TO SEVEN-SEGMENT LATCH/DECODER/DISPLAY DRIVER FOR LIQUID-CRYSTAL DISPLAYS

SWITCHING CHARACTERISTICS ($v_{cc} = 2\sim6V$, $T_a = -40\sim+85^{\circ}C$)

Symbol				Limits					
	Parameter	Test conditions	-		25°C			-40~+85°C	
	<u> </u>		V _{cc} (V)	Min	Тур	Max	Min	Max	<u> </u>
			2.0		ĺ	75		95	
t _{TLH}	Low-level to high-level and	,	4.5			15		_ 19	n
_	high lavel to Jave lavel	1	6.0			13		16	
	high-level to low-level output transition time		2.0			75		95	
t _{THL}			4.5			15		19	ns
		1	6.0)	. 13		16	1
		1	2.0			385		480	
t _{PLH}	Low-level to high-level and		4.5			77		96	n
	high-level to low-level		6.0			66		82	
	output propagation time		2.0			385		480	
tpHL	(A~D − a~g)	. The state of th	4.5			77		96	r
			6.0			66		82	l
		$C_L = 50 pF (Note 4)$	2. 0			385		480	
t _{PLH}	Low-level to high-level and	l e	4.5	1	}	77		96	r
	high-level to low-level		6.0		ļ	66	 -	82	1
	output propagation time		2.0			385		480	
t _{PHL}	(<u>LE</u> − a~q)		4.5	İ]	77		96	r
THE .	, , , , , , , , , , , , , , , , , , , ,	1	6.0			66		82	1
		1	2.0			240	-	300	
t _{PLH}	Low-level to high-level and		4.5			48		60	r
*PLH	high-level to low-level		6.0			41		51	'
	output propagation time		2.0			240		300	1-
tpHL	(BI — a∼g)		4.5		1	48	ļ	60	
TPIL	,		6.0			41		51	'
		†	2.0			175		220	
t _{PLH}	Low-level to high-level and		4.5			35		44	r
-ru	high-level to low-level		6.0	l	l	30		37	'
	output propagation time		2.0		<u> </u>	175		220	+-
t _{PHL}	(Ph — a~g)		4.5		1	35]	44	r
THE	4 g /	1	6.0			30		37	'
Cı	Input capacitance	 		 		10		10	p
CPD	Power dissipation capacitance (Note 3)					<u> </u>		† · · ·	p

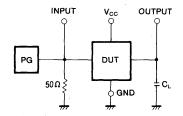
Note 3: C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS ($V_{cc} = 2 \sim 6V$, $T_a = -40 \sim +85^{\circ}$ C)

Symbol	Parameter	Test conditions			25℃		-40~	+85℃	Unit
l			V _{cc} (V)	Min	Тур	Max	Min	Max	
			2.0	75			95		
tw	LE pulse width		4.5	15	1		19		ns
		·	6.0	13			. 16		
	A~D setup time with respect to LE		2.0	75			95		
t _{su}			4.5	15		i i	19.		ns
			6.0	13			16		
	A~D hold time with respect to LE		2.0	0			0		
th			4.5	0			0		ns
			6.0	0			0		

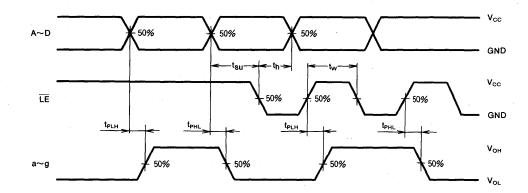
BCD-TO SEVEN-SEGMENT LATCH/DECODER/DISPLAY DRIVER FOR LIQUID-CRYSTAL DISPLAYS

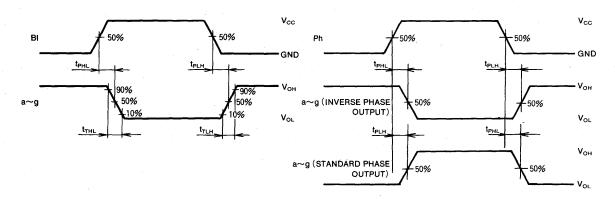
Note 4: Test Circuit



- (1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

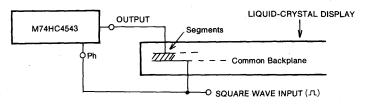
TIMING DIAGRAM





APPLICATION EXAMPLE

LIQUID-CRYSTAL DISPLAY DRIVER







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