MITSUBISHI SEMICONDUCTORS 1986

HIGH SPEED CMOS LOGIC

DATA BOOK

MITSUBISHI ELECTRIC

1986 MITSUBISHI HIGH SPEED CMOS LOGIC SEMICONDUCTORS
MITSUBISHI ELECTRIC

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GUIDANCE 1

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INDEX BY FUNCTION (★ : under development)

Conditions (V_{CC}=4.5V, T_a=−40∼+85℃, switching characteristics are at C_L=50pF)

INVERTERS

Type	Circuit function	Electrical characteristics				Package outlines	Page
		High-level output current (mA)	Low-level output current (mA)	Output propagation time (L to H) (ns)	Output propagation time (H to L) (ns)		
M74HCU04P	Hex Unbuffered Inverter	−4	4	21	21	14P4	2−15
M74HCU04DP ★	Hex Unbuffered Inverter	−4	4	21	21	14P2P	2−15
M74HC04P	Hex Inverter	−4	4	24	24	14P4	2−12
M74HC04DP ★	Hex Inverter	−4	4	24	24	14P2P	2−12
M74HCT04P ★	Hex Inverter with LSTTL-Compatible Inputs	—	—	—	—	14P4	—
M74HC05P ★	Hex Inverter with Open-Drain Outputs	—	—	—	—	14P4	—
M74HC05DP ★	Hex Inverter with Open-Drain Outputs	—	—	—	—	14P2P	—

NAND GATES

M74HC00P	Quadruple 2-Input Positive NAND Gate	−4	4	23	23	14P4	2−3
M74HC00DP ★	Quadruple 2-Input Positive NAND Gate	−4	4	23	23	14P2P	2−3
M74HCT00P ★	Quadruple 2-Input Positive NAND Gate with LSTTL-Compatible Inputs	—	—	—	—	14P4	—
M74HC03P	Quadruple 2-Input Positive NAND Gate with Open-Drain Outputs	—	4	32	32	14P4	2−9
M74HC10P	Triple 3-Input Positive NAND Gate	−4	4	24	24	14P4	2−21
M74HC10DP ★	Triple 3-Input Positive NAND Gate	−4	4	24	24	14P2P	2−21
M74HC20P	Dual 4-Input Positive NAND Gate	−4	4	23	23	14P4	2−30
M74HC20DP ★	Dual 4-Input Positive NAND Gate	−4	4	23	23	14P2P	2−30
M74HC30P ★	8-Input Positive NAND Gate	—	—	—	—	14P4	—
M74HC30DP ★	8-Input Positive NAND Gate	—	—	—	—	14P2P	—
M74HC133P ★	13-Input Positive NAND Gate	—	—	—	—	16P4	—

AND GATES

M74HC08P	Quadruple 2-Input Positive AND Gate	−4	4	30	30	14P4	2−18
M74HC08DP ★	Quadruple 2-Input Positive AND Gate	−4	4	30	30	14P2P	2−18
M74HC09P ★	Quadruple 2-Input Positive AND Gate with Open-Drain Outputs	—	—	—	—	14P4	—
M74HC11P	Triple 3-Input Positive AND Gate	−4	4	31	31	14P4	2−24
M74HC11DP ★	Triple 3-Input Positive AND Gate	−4	4	31	31	14P2P	2−24
M74HC21P ★	Dual 4-Input Positive AND Gate	—	—	—	—	14P4	—

NOR GATES

M74HC02P	Quadruple 2-Input Positive NOR Gate	−4	4	23	23	14P4	2−6
M74HC02DP ★	Quadruple 2-Input Positive NOR Gate	−4	4	23	23	14P2P	2−6
M74HC27P	Triple 3-Input Positive NOR Gate	−4	4	23	23	14P4	2−33
M74HC27DP ★	Triple 3-Input Positive NOR Gate	−4	4	23	23	14P2P	2−33
M74HC4002P	Dual 4-Input Positive NOR Gate	−4	4	30	30	14P4	2−243
M74HC4078P	8-Input Positive NOR/OR Gate	−4	4	33	33	14P4	2−246

OR GATES

M74HC32P	Quadruple 2-Input Positive OR Gate	−4	4	25	25	14P4	2−36
M74HC32DP ★	Quadruple 2-Input Positive OR Gate	−4	4	25	25	14P2P	2−36
M74HC4075P ★	Triple 3-Input OR Gate	—	—	—	—	14P4	—
M74HC4078P	8-Input Positive NOR/OR Gate	−4	4	33	33	14P4	2−246

EXCLUSIVE OR GATE

M74HC86P	Quadruple 2-Input Exclusive OR Gate	−4	4	30	30	14P4	2−58
M74HC86DP ★	Quadruple 2-Input Exclusive OR Gate	−4	4	30	30	14P2P	2−58

INDEX BY FUNCTION

EXCLUSIVE NOR GATE

Type	Circuit function	Electrical characteristics				Package outlines	Page
		High-level output current (mA)	Low-level output current (mA)	Output propagation time (L to H) (ns)	Output propagation time (H to L) (ns)		
M74HC266P	Quadruple 2-Input Exclusive NOR Gate	−4	4	30	30	14P4	2 −187
M74HC266AP★	Quadruple 2-Input Exclusive NOR Gate with Open-Drain Outputs	—	—	—	—	14P4	—

AND-OR-INVERTER GATE

M74HC51P ★	2-Wide, 2-Input/2-Wide, 3-Input AND-OR-INVERT Gates	—	—	—	—	14P4	—
M74HC51DP ★	2-Wide, 2-Input/2-Wide, 3-Input AND-OR-INVERT Gates	—	—	—	—	14P2P	—

BUFFERS/LINE DRIVERS

Type	Circuit function	Output		Electrical characteristics				Package outlines	Page
		2 state	3 state	High-level output current (mA)	Low-level output current (mA)	Output propagation time (L to H) (ns)	Output propagation time (H to L) (ns)		
M74HC125P ★	Quadruple 3-State Noninverting Buffer		NI	—	—	—	—	14P4	—
M74HC126P ★	Quadruple 3-State Noninverting Buffer		NI	—	—	—	—	14P4	—
M74HC240P	Octal 3-State Inverting Buffer/Line Driver /Line Receiver		I	−6	6	25	25	20P4	2 −156
M74HC240DWP ★	Octal 3-State Inverting Buffer/Line Driver /Line Receiver		I	−6	6	25	25	20P2V	2 −156
M74HCT240P★	Octal 3-State Inverting Buffer/Line Driver /Line Receiver with LSTTL-Compatible Inputs		I	—	—	—	—	20P4	—
M74HC241P	Octal 3-State Noninverting Buffer/Line Driver /Line Receiver		NI	−6	6	29	29	20P4	2 −160
M74HC241DWP ★	Octal 3-State Noninverting Buffer/Line Driver /Line Receiver		NI	−6	6	29	29	20P2V	2 −160
M74HCT241P★	Octal 3-State Noninverting Buffer/Line Driver /Line Receiver with LSTTL-Compatible Inputs		NI	—	—	—	—	20P4	—
M74HC244P	Octal 3-State Noninverting Buffer/Line Driver /Line Receiver		NI	−6	6	29	29	20P4	2 −173
M74HC244DWP ★	Octal 3-State Noninverting Buffer/Line Driver /Line Receiver		NI	−6	6	29	29	20P2V	2 −173
M74HCT244P★	Octal 3-State Noninverting Buffer/Line Driver /Line Receiver with LSTTL-Compatible Inputs		NI	—	—	—	—	20P4	—
M74HC365P	Hex 3-State Noninverting Buffer with Common Enables		NI	−6	6	30	30	16P4	2 −197
M74HC365DP★	Hex 3-State Noninverting Buffer with Common Enables		NI	−6	6	30	30	16P2P	2 −197
M74HC366P	Hex 3-State Inverter Buffer with Common Enables		I	−6	6	24	24	16P4	2 −201
M74HC367P	Hex 3-State Noninverting Buffer with Separate 2-Bit and 4-Bit Sections		NI	−6	6	24	24	16P4	2 −205
M74HC367DP★	Hex 3-State Noninverting Buffer with Separate 2-Bit and 4-Bit Sections		NI	−6	6	24	24	16P2P	2 −205
M74HC368P	Hex 3-State Inverting Buffer with Separate 2-Bit and 4-Bit Sections		I	−6	6	24	24	16P4	2 −209
M74HC368DP★	Hex 3-State Inverting Buffer with Separate 2-Bit and 4-Bit Sections		I	−6	6	24	24	16P2P	2 −209
M74HC540P ★	Octal 3-State Inverting Buffer/Line Driver /Line Receiver		I	—	—	—	—	20P4	—
M74HC541P ★	Octal 3-State Noninverting Buffer/Line Driver /Line Receiver		NI	—	—	—	—	20P4	—
M74HC4049BP ★	Hex Inverting Buffer/Logic-Level Down Converter	I		—	—	—	—	16P4	—
M74HC4050BP ★	Hex Noninverting Buffer/Logic-Level Down Converter	NI		—	—	—	—	16P4	—

I : Invert output NI : Non-inverted output

INDEX BY FUNCTION

BUS TRANSCEIVERS

Type	Circuit function	Output		Electrical characteristics				Package outlines	Page
		2 state	3 state	High-level output current (mA)	Low-level output current (mA)	Output propagation time (L to H) (ns)	Output propagation time (H to L) (ns)		
M74HC242P	Quadruple 3-State Inverting Bus Transceiver		I	−6	6	25	25	20P4	2 −165
M74HC243P	Quadruple 3-State Noninverting Bus Transceiver		NI	−6	6	25	25	20P4	2 −169
M74HC245P ★	Octal 3-State Noninverting Bus Transceiver		NI	—	—	—	—	20P4	—
M74HC245DWP ★	Octal 3-State Noninverting Bus Transceiver		NI	—	—	—	—	20P2V	—
M74HC640P ★	Octal 3-State Inverting Bus Transceiver		I	—	—	—	—	20P4	—
M74HC643P ★	Octal 3-State Inverting and Noninverting Bus Transceiver		NI, I	—	—	—	—	20P4	—
M74HC645P ★	Octal 3-State Noninverting Bus Transceiver		NI	—	—	—	—	20P4	—
M74HC646P ★	Octal 3-State Noninverting Bus Transceiver and D-Type Flip-Flop		NI	—	—	—	—	24P4D	—
M74HC648P ★	Octal 3-State Inverting Bus Transceiver and D-Type Flip-Flop		I	—	—	—	—	24P4D	—

I : Invert output NI : Non-inverted output

SCHMITT TRIGGERS

Type	Circuit function	Electrical characteristics				Package outlines	Page
		Positive-going threshold voltage (V)	Negative-going threshold voltage (V)	Output propagation time (L to H) (ns)	Output propagation time (H to L) (ns)		
M74HC14P	Hex Schmitt-Trigger Inverter	−4	4	31	31	14P4	2 −27
M74HC14DP ★	Hex Schmitt-Trigger Inverter	−4	4	31	31	14P2P	2 −27
M74HC132P ★	Quadruple 2-Input Schmitt-Trigger Positive NAND Gate	—	—	—	—	14P4	—

J-K FLIP FLOPS

Type	Circuit function	Electrical characteristics			Trigger	Set	Reset	Package outlines	Page
		Operation frequency (MHz)	Setup time (ns)	Hold time (ns)					
M74HC73P	Dual J-K Flip-Flop with Reset	21	25	0	↓	—	⊔	14P4	2 −43
M74HC76P	Dual J-K Flip-Flop with Set and Reset	21	25	0	↓	⊔	⊔	16P4	2 −53
M74HC107P ★	Dual J-K Flip-Flop with Reset	21	25	0	↓	—	⊔	14P4	2 −61
M74HC109P	Dual J-$\overline{K}$ Flip-Flop with Set and Reset	25	25	5	↑	⊔	⊔	16P4	2 −66
M74HC112P	Dual J-K Flip-Flop with Set and Reset	25	25	0	↓	⊔	⊔	16P4	2 −71
M74HC113P ★	Dual J-K Flip-Flop with Set	21	25	0	↓	⊔	—	14P4	2 −76
M74HC114P	Dual J-K Flip-Flop with Set and Common Reset	21	25	0	↓	⊔	⊔	14P4	2 −81

↑ : Positive-going edge ↓ : Negative-going edge ⊔ : Active low-level

INDEX BY FUNCTION

D-TYPE FLIP FLOPS

Type	Circuit function	Electrical characteristics			Trigger	Set	Reset	Package outlines	Page
		Operation frequency (MHz)	Setup time (ns)	Hold time (ns)					
M74HC74P	Dual D-Type Flip-Flop with Set and Reset	21	25	0	↑	⌊	⌊	14P4	2—48
M74HC74DP ★	Dual D-Type Flip-Flop with Set and Reset	21	25	0	↑	⌊	⌊	14P2P	2—48
M74HC173P ★	Quadruple 3-State D-Type Flip-Flop with Common Clock and Reset	—	—	—	↑	—	—	16P4	—
M74HC174P	Hex D-Type Flip-Flop with Common Clock and Reset	21	25	5	↑	—	⌊	16P4	2—142
M74HC174DP★	Hex D-Type Flip-Flop with Common Clock and Reset	21	25	5	↑	—	⌊	16P2P	2—142
M74HC175P	Quadruple D-Type Flip-Flop with Common Clock and Reset	24	25	5	↑	—	⌊	16P4	2—146
M74HC175DP★	Quadruple D-Type Flip-Flop with Common Clock and Reset	24	25	5	↑	—	⌊	16P2P	2—146
M74HC273P	Octal D-Type Flip-Flop with Common Clock and Reset	21	25	0	↑	—	⌊	20P4	2—190
M74HC273DWP ★	Octal D-Type Flip-Flop with Common Clock and Reset	21	25	0	↑	—	⌊	20P2V	2—190
M74HC374P	Octal 3-State Noninverting D-Type Flip-Flop	24	18	12	↑	—	—	20P4	2—218
M74HC374DWP ★	Octal 3-State Noninverting D-Type Flip-Flop	24	18	12	↑	—	—	20P2V	2—218
M74HC377P ★	Octal D-Type Flip-Flop with Common Clock and Enable	—	—	—	↑	—	—	20P4	—
M74HC534P	Octal 3-State Inverting D-Type Flip-Flop	24	18	12	↑	—	—	20P4	2—238
M74HC564P ★	Octal 3-State Inverting D-Type Flip-Flop	—	—	—	↑	—	—	20P4	—
M74HC574P ★	Octal 3-State Noninverting D-Type Flip-Flop	—	—	—	↑	—	—	20P4	
M74HC646P ★	Octal 3-State Noninverting Bus Transceiver and D-Type Flip-Flop	—	—	—	↑	—	—	24P4D	—
M74HC648P ★	Octal 3-State Inverting Bus Transceiver and D-Type Flip-Flop	—	—	—	↑	—	—	24P4D	—

↑ : Positive-going edge ⌊ : Active low-level

SYNCHRONOUS BINARY COUNTERS

Type	Circuit function	Electrical characteristics	Trigger	Preset	Reset	Package outlines	Page
		Count frequency (MHz)					
M74HC161P	Presettable 4-Bit Binary Counter with Asynchronous Reset	21	↑	Ⓢ	⌊Ⓐ	16P4	2—119
M74HC161DP★	Presettable 4-Bit Binary Counter with Asynchronous Reset	21	↑	Ⓢ	⌊Ⓐ	16P2P	2—119
M74HC163P	Presettable 4-Bit Binary Counter with Synchronous Reset	21	↑	Ⓢ	⌊Ⓢ	16P4	2—131
M74HC163DP★	Presettable 4-Bit Binary Counter with Synchronous Reset	21	↑	Ⓢ	⌊Ⓢ	16P2P	2—131
M74HC191P ★	Presettable 4-Bit Binary Up/Down Counter	—	↑	Ⓐ	—	16P4	—
M74HC193P ★	Presettable 4-Bit Binary Up/Down Counter with Reset	—	↑	Ⓐ	⎍Ⓐ	16P4	—
M74HC669P ★	Presettable 4-Bit Binary Up/Down Counter	—	↑	Ⓢ	—	16P4	—

↑ : Positive-going edge ⎍ : Active high-level ⌊ : Active low-level Ⓐ : Asynchronous Ⓢ : Synchronous

SYNCHRONOUS DECADE COUNTERS

M74HC160P	Presettable BCD Counter with Asynchronous Reset	21	↑	Ⓢ	⌊Ⓐ	16P4	2—113
M74HC162P	Presettable BCD Counter with Synchronous Reset	21	↑	Ⓢ	⌊Ⓢ	16P4	2—125
M74HC190P ★	Presettable BCD Up/Down Counter	—	↑	Ⓐ	—	16P4	—
M74HC192P ★	Presettable BCD Up/Down Counter with Reset	—	↑	Ⓐ	⎍Ⓐ	16P4	—
M74HC4017P ★	Decade Counter/Divider	—	Note	—	⎍Ⓐ	16P4	—

↑ : Positive-going edge ⎍ : Active high-level ⌊ : Active low-level Ⓐ : Asynchronous Ⓢ : Synchronous

Note : Positive-going edge↓, ($\overline{CE}$ is low-level), when the CLOCK pin is used. Negative-going edge↓, (CP is high-level), when the $\overline{CLOCK\ ENABLE}$ pin is used.

INDEX BY FUNCTION

OCTAL COUNTER/DIVIDER

Type	Circuit function	Electrical characteristics: Count frequency (MHz)	Trigger	Preset	Reset	Package outlines	Page
M74HC4022P ★	Octal Counter/Divider	—	Note	—	⎍	16P4	—

⎍ : Active high-level

Note : Positive-going edge, ↑ ($\overline{CE}$ is low-level), when the CLOCK pin is used. Negative-going edge, ↓ (CP is high-level), when the CLOCK ENABLE pin is used.

MONOSTABLE MULTIVIBRATORS

Type	Circuit function	Electrical characteristics: External timing resistor/capacitor for setting output pulse width	Retrigger	Reset	Package outlines	Page
M74HC123P ★	Dual Retriggerable Monostable Multivibrator	1~1MΩ/no restriction	○	○	16P4	—
M74HC221P ★	Dual Monostable Multivibrator	1~1MΩ/no restriction	○	○	16P4	—
M74HC4538P ★	Dual Precision Monostable Multivibrator (Retriggerable, Resettable)	1~1MΩ/no restriction	○	○	16P4	—

LATCHES

Type	Circuit function	Electrical characteristics: Output propagation time (L to H) (ns)	Output propagation time (H to L) (ns)	Setup time (ns)	Hold time (ns)	Enable	Reset	Package outlines	Page
M74HC75P ★	Dual 2-Bit Transparent Latch	—	—	—	—	⎍	—	16P4	—
M74HC259P ★	8-Bit Addressable Latch/1-of-8 Decoder	—	—	—	—	⎍	⎍	16P4	—
M74HC279P ★	Quadruple R-S Latch	—	—	—	—	—	—	16P4	—
M74HC373P	Octal 3-State Noninverting D-Type Transparent Latch	38	38	18	12	⎍	—	20P4	2—213
M74HC373DWP ★	Octal 3-State Noninverting D-Type Transparent Latch	38	38	18	12	⎍	—	20P2V	2—213
M74HC375P ★	Dual 2-Bit Transparent Latch	—	—	—	—	⎍	—	16P4	—
M74HC533P	Octal 3-State Inverting D-Type Transparent Latch	38	38	18	12	⎍	—	20P4	2—233
M74HC563P ★	Octal 3-State Inverting D-Type Transparent Latch	—	—	—	—	⎍	—	20P4	—
M74HC573P ★	Octal 3-State Noninverting D-Type Transparent Latch	—	—	—	—	⎍	—	20P4	—

⎍ : Active high-level ⎍ : Active low-level

SHIFT REGISTERS

Type	Circuit function	Electrical characteristics: Shift frequency (MHz)	Trigger	Operating modes: Right shift	Left shift	Parallel load	Reset	Package outlines	Page
M74HC164P	8-Bit Serial-Input/Parallel-Output Shift Register	21	↑	○	—	—	⎍	14P4	2—137
M74HC165P ★	8-Bit Serial-or Parallel-Input/Serial-Output Shift Register	—	↑	○	—	○	—	16P4	—
M74HC166P ★	8-Bit Serial-or Parallel-Input/Serial-Output Shift Register with Reset	—	↑	○	—	○	⎍	16P4	—
M74HC194P ★	4-Bit Bidirectional Universal Shift Register	—	↑	○	○	○	⎍	16P4	—
M74HC195P ★	4-Bit Universal Shift Register	—	↑	○	—	○	⎍	16P4	—
M74HC299P ★	8-Bit Bidirectional Universal Shift Register with 3-State Parallel Outputs	—	↑	○	○	○	⎍	20P4	—
M74HC323P ★	8-Bit Bidirectional Universal Shift Register with 3-State Parallel Outputs	—	↑	○	○	○	⎍	20P4	—
M74HC595P ★	8-Bit Serial-Input/Serial-or Parallel-Output Shift Register with Latched 3-State Outputs	—	↑	○	—	—	⎍	16P4	—
M74HC597P ★	8-Bit Serial-or Parallel-Input/Serial-Output Shift Register with Input Latch	—	↑	○	—	○	○	16P4	—

↑ : Positive-going edge ⎍ : Active low-level

INDEX BY FUNCTION

BINARY RIPPLE COUNTERS

Type	Circuit function	Electrical characteristics: Count frequency (MHz)	Trigger	Reset	Package outlines	Page
M74HC393P	Dual 4-Stage Binary Ripple Counter	21	↓	⎍	14P4	2—228
M74HC4020P ★	14-Stage Binary Ripple Counter	—	↓	⎍	16P4	—
M74HC4024P ★	7-Stage Binary Ripple Counter	—	↓	⎍	14P4	—
M74HC4040P ★	12-Stage Binary Ripple Counter	—	↓	⎍	16P4	—

↓ : Negative-going edge ⎍ : Active high-level

ASYNCHRONOUS DECADE COUNTER

M74HC390P	Dual 4-Stage Binary Ripple Counter with ÷2 and ÷5 Sections	21	↓	⎍	16P4	2—223

↓ : Negative-going edge ⎍ : Active high-level

ANALOG SWITCHES/MULTIPLEXERS

Type	Circuit function	Electrical characteristics: ON resistance V_I=2.5V (Ω)	Propagation time(ns): Data input to output	Propagation time(ns): Control (inhibit) input to output	Package outlines	Page
M74HC4051P ★	8-Channel Analog Multiplexer/Demultiplexer	—	—	—	16P4	—
M74HC4052P ★	Dual 4-Channel Analog Multiplexer/Demultiplexer	—	—	—	16P4	—
M74HC4053P ★	Triple 2-Channel Analog Multiplexer/Demultiplexer	—	—	—	16P4	—
M74HC4066P ★	Quad Analog Switch/Multiplexer/Demultiplexer with Enhanced ON-Resistance Linearity	—	—	—	14P4	—

DATA SELECTORS/DIGITAL MULTIPLEXERS

Type	Circuit function	Output	Electrical characteristics: Propagation time(ns): Strobe (inhibit) to output	Propagation time(ns): Select input to output	Propagation time(ns): Data input to output	Package outlines	Page
M74HC151P	8-Input Data Selector/Multiplexer	NI, I	35	63	49	16P4	2—100
M74HC153P ★	Dual 4-Input Data Selector/Multiplexer	NI	—	—	—	16P4	—
M74HC157P	Quadruple 2-Input Noninverting Data Selector/Multiplexer	NI	29	32	32	16P4	2—105
M74HC157DP★	Quadruple 2-Input Noninverting Data Selector/Multiplexer	NI	29	32	32	16P2P	2—105
M74HC158P	Quadruple 2-Input Inverting Data Selector/Multiplexer	I	29	32	32	16P4	2—109
M74HC251P	8-Input Data Selector/Multiplexer with 3-State Outputs	3S, NI, I	55	51	49	16P4	2—177
M74HC253P ★	Dual 4-Input Data Selector/Multiplexer with 3-State Outputs	3S, NI	—	—	—	16P4	—
M74HC257P ★	Quadruple 2-Input Data Selector/Multiplexer with 3-State Outputs	3S, NI	38	25	25	16P4	2—182
M74HC258P ★	Quadruple 2-Input Data Selector/Multiplexer with 3-State Outputs	3S, NI	—	—	—	16P4	—
M74HC298P ★	Quadruple 2-Input Data Selector/Multiplexer with Output Latch	NI	—	—	—	16P4	—
M74HC354P ★	8-Input Data Selector/Multiplexer with Data and Address Latches and with 3-State Outputs	3S, NI, I	—	—	—	20P4	—
M74HC356P ★	8-Input Data Selector/Multiplexer with Data and Address Latches and with 3-State Outputs	3S, NI, I	—	—	—	20P4	—

I : Invert output NI : Non inverted output 3S : 3-State output

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DECODERS

Type	Circuit function	Electrical characteristics: Output propagation time (L to H) (ns)	Electrical characteristics: Output propagation time (H to L) (ns)	Package outlines	Page
M74HC42P	1-of-10 Decoder	38	38	16P4	2—39
M74HC137P	1-of-8 Decoder/Demultiplexer with Address Latch	43	60	16P4	2—86
M74HC138P	1-of-8 Decoder/Demultiplexer	38	50	16P4	2—91
M74HC138DP★	1-of-8 Decoder/Demultiplexer	38	50	16P2P	2—91
M74HCT138P	1-of-8 Decoder/Demultiplexer with LSTTL-Compatible Inputs	—	—	16P4	—
M74HC139P	Dual 1-of-4 Decoder/Demultiplexer	55	55	16P4	2—96
M74HC139DP★	Dual 1-of-4 Decoder/Demultiplexer	55	55	16P2P	2—96
M74HC154P ★	1-of-16 Decoder/Demultiplexer	—	—	24P4D	—
M74HC155P ★	Dual 1-of-4 Decoder/Demultiplexer	—	—	16P4	—
M74HC237P	1-of-8 Decoder/Demultiplexer with Address Latch	59	47	16P4	2—151
M74HC238P ★	1-of-8 Decoder/Demultiplexer	—	—	16P4	—
M74HC259P ★	8-Bit Addressable Latch/1-of-8 Decoder	—	—	16P4	—
M74HC4511P★	BCD-to-Seven-Segment Latch/Decoder/Display Driver	—	—	16P4	—
M74HC4514P★	1-of-16 Decoder/Demultiplexer with Address Latch ("H" Level Output)	—	—	24P4D	—
M74HC4515P★	1-of-16 Decoder/Demultiplexer with Address Latch ("L" Level Output)	—	—	24P4D	—
M74HC4543P★	BCD-to-Seven-Segment Latch/Decoder/Display Driver for Liquid-Crystal Displays	—	—	16P4	—

Segment Identification of M74HC4511P, M74HC4543P

Decimal number	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Character	0	1	2	3	4	5	6	7	8	9						

ENCODERS

Type	Circuit function	Electrical characteristics: Output propagation time (L to H) (ns)	Electrical characteristics: Output propagation time (H to L) (ns)	Package outlines	Page
M74HC147P ★	Decimal-to-BCD Priority Encoder	—	—	16P4	—
M74HC148P ★	Octal-to-BCD Priority Encoder	—	—	16P4	—

COMPARATORS

M74HC85P ★	4-Bit Magnitude Comparator	—	—	16P4	—
M74HC688P ★	8-Bit Equality Comparator	—	—	20P4	—

FULL ADDER

M74HC283P ★	4-Bit Binary Full Adder with Fast Carry	—	—	16P4	—

PARITY GENERATOR/CHECKER

M74HC280P	9-Bit Odd/Even Parity Generator/Checker	52	52	14P4	2—194

REGISTER FILES

M74HC670P ★	4-By-4 Register File with 3-State Outputs	—	—	16P4	—

SYMBOLOGY

Symbol	Descriptions	
C_I	Input capacitance	
C_L	Load capacitance	Extenally connected load capacitance
C_O	Off-state output capacitance	The output capacitance when the output is disabled
C_{PD}	Power dissipation capacitance	Internal capacitance of the IC calculated from operation supply current.
C_X	External timing capacitance	Externally connected capacitance used to set the output pulse width of a monostable multivibrator.
f_I	Input frequency	The sine wave frequency applied to the input terminal
f_{max}	Maximum repetition frequency	Maximum input repetition frequency for normal IC operation.
GND	Ground	
H	Indicates the high logic level	Used in voltage and current suffixes to indicate the high potential level.
I	Indicates current or input	Currents flowing into ICs are taken to be positive and those flowing out as negative.
I_{CC}	Supply current	The current flowing into the V_{CC} supply terminal.
I_{DD}	Supply current	The current flowing into the V_{DD} supply terminal.
I_I	Input current	Input current flowing into an input terminal when a voltage is applied.
I_{IH}	High-level input current	The current flowing into an input when a specified high voltage is applied.
I_{IL}	Low-level input current	The current flowing into an input when a specified low voltage is applied.
I_O	Output current	Output currents flowing into ICs are taken to be positive and those flowing out as negative
I_{OFF}	Off-state leakage current	The current flowing between the input and output of an analog switch is in the off state.
I_{OH}	High-level output curent	The current flowing out of an output which is in the high state.
I_{OL}	Low-level output current	The current flowing out of an output which is in the low state
I_{OZH}	Off-state high-level output current	The current flowing out of the off state output with a specified high output voltage applied.
I_{OZL}	Off-state low-level output current	The current flowing out of the off state output with a specified low output voltage applied.
L	Indicates the low logic level	Used in voltage and current suffixes to indicate the low potential level.
O	Indicates output	
P_d	Power dissipation	Product of the supply voltage and the supply current.
R_I	Input resistance	Externally connected intput resistance.
R_L	Load resistance	Externally connected load resistance.
R_{OFF}	OFF resistance	The DC resistance between the input and output of an analog switch is in the off state.
R_{ON}	ON resistance	The DC resistance between the input and output of an analog switch is in the on state.
R_X	External connected timing resistor	Externally connected resistor used to set the output pulse width of a monostable multivibrator.
T_a	Operating free-air temperature	The temperature of the environment surrounding an IC.
t_f	Fall time	Amount of time for the clock pulse to change from high to low.
t_h	Hold time	Amount of time that the input conditions must be held after related inputs are changed.
T_{opr}	Operating temperatuer	The ambient temperature range for normal IC operation.
t_{pd}	Propagation delay time	Amount of time required from a change of input signal until the corresponding change in output, expressed as the average propagation time.
t_{PHL}	High-level to low-level output propagation time	Amount of time required from a change of input signal until the output changes from high-level to low-level.
t_{PHZ}	Output disable time from high-level	Amount of time required from a change of input signal until the output changes from high-level to high-impedance.
t_{PLH}	Low-level to high-level output propagation time	Amount of time required from a change of input signal until the ourtput changes from low-level to high-level
t_{PLZ}	Output disable time from low-level	Amount of time required from a change of input signal until the output changes from low-level to high-impedance.
t_{PZH}	Output enable time to high-level	Amount of time required from a change of input signal until the output changes from high-impedance to high-level
t_{PZL}	Output enable time to low-level	Amount of time required from a change of input signal until the output changes from high-impedance to low-level.
t_r	Rise time	Amount of time for the clock pulse to change from low to high
t_{rec}	Recovery time	Time from the point at which the input states are cancelled until the next clock pulse may be applied.
T_{stg}	Storage temperature	The range of surrounding storage temperature for an IC
t_{SU}	Setup time	Amount of time that the input conditions must be held before related inputs are changed.

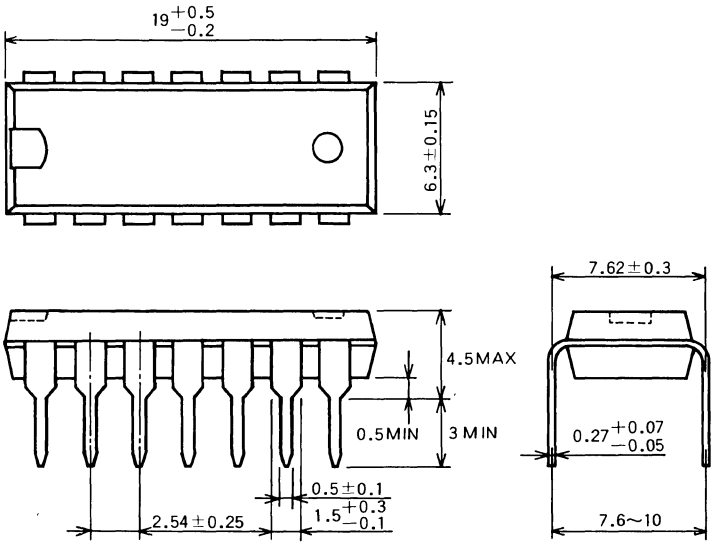
SYMBOLOGY

Symbol	Descriptions	
t_{THL}	High-level to low-level output transition time	The time required for the output waveform voltage value to change from the 90% point to the 10% point
t_{TLH}	Low-level to high-level output transition time	The time required for the output waveform voltage value to change from the 10% point to the 90% point
t_W	Pulse width	The time required for a pulse to change from one specified level to another
t_{WQ}	Output pulse width	The width of the pulse appearing in the output of a monostable multivibrator
V_{CC}	V_{CC} supply voltage	
V_{DD}	V_{DD} supply voltage	
V_{EE}	V_{EE} supply voltage	
V_H	Hysteresis voltage	This voltage is the difference between the positive-going threshold and the negative-going threshold voltages of the Schmitt trigger circuit
V_I	Input voltage	Voltage applied to an input
V_{IH}	High-level input voltage	The range of input voltages that represents a logic high in the system
V_{IL}	Low-level input voltage	The range of input voltages that represents a logic low in the system
V_O	Output voltage	Voltage applied to or appearing at an ouptut
V_{OH}	High-level output voltage	Voltage at an ouptut in the high state
V_{OL}	Low-level output voltage	Voltage at an output in the low state
V_{SS}	V_{SS} supply voltage	
V_T	Threshold voltage	The input voltage beyond at which the output changes
V_{T+}	Positive-going threshold voltage	The threshold voltage at which the output changes when the input is changing from low to high
V_{T-}	Negative-going threshold voltage	The threshold voltage at which the output changes when the input is changing from high to low
Z	Indicates the Off-state	Indicates that the output is in the high-impedance state

PACKAGE OUTLINES

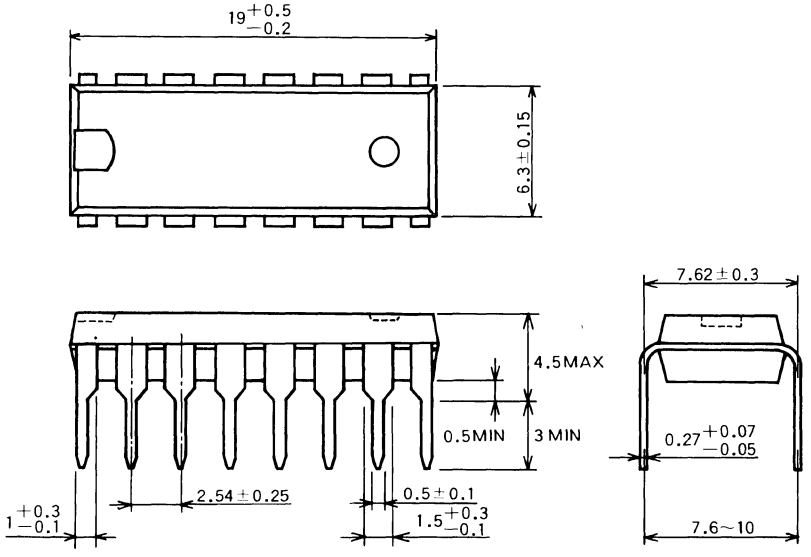
TYPE 14P4 14-PIN MOLDED PLASTIC DIP

Dimension in mm



TYPE 16P4 16-PIN MOLDED PLASTIC DIP

Dimension in mm

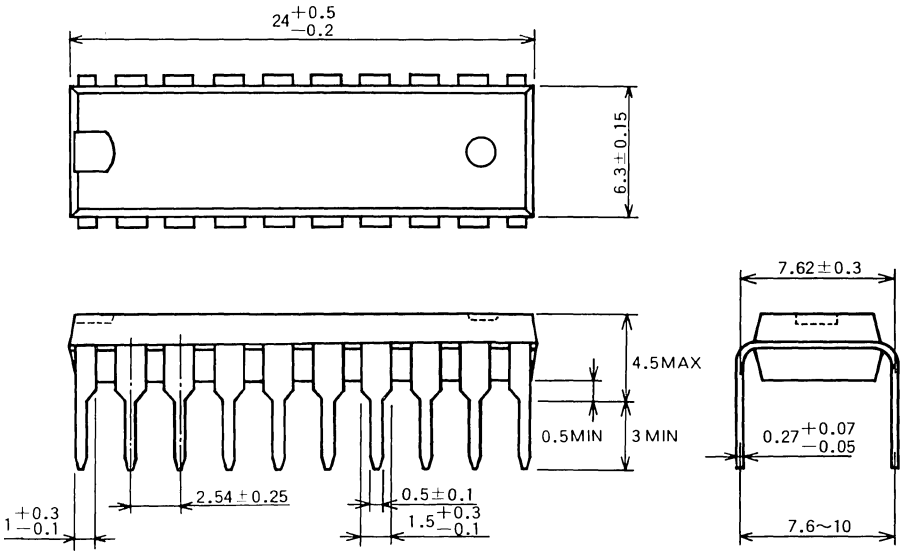


MITSUBISHI ELECTRIC

PACKAGE OUTLINES

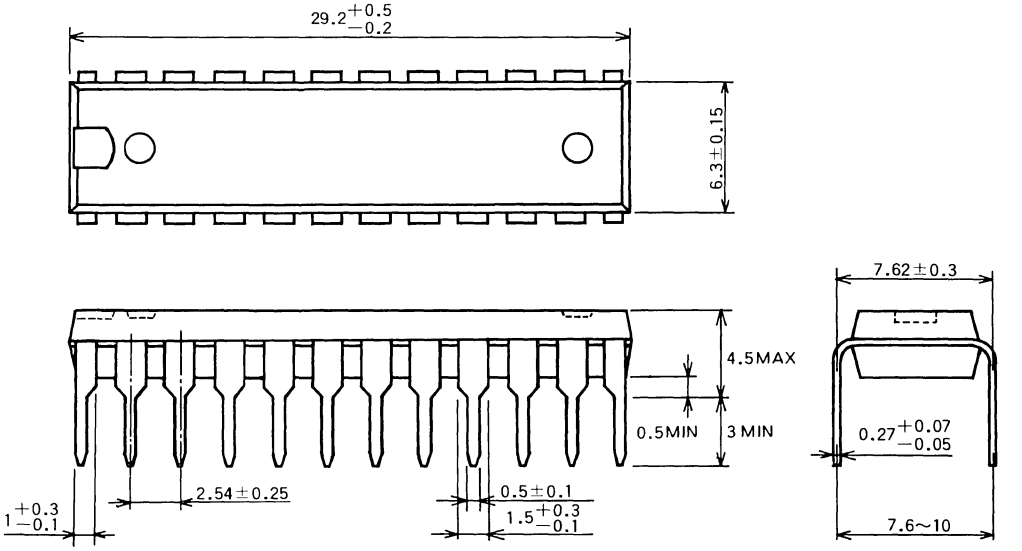
TYPE 20P4 20-PIN MOLDED PLASTIC DIP

Dimension in mm



TYPE 24P4D 24-PIN MOLDED PLASTIC DIP

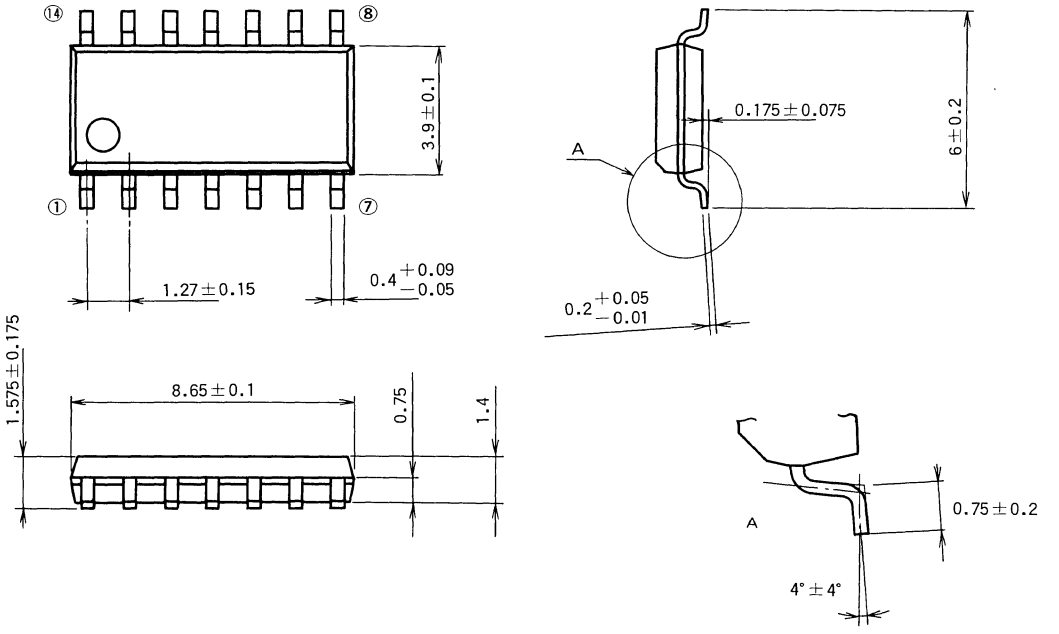
Dimension in mm



PACKAGE OUTLINES

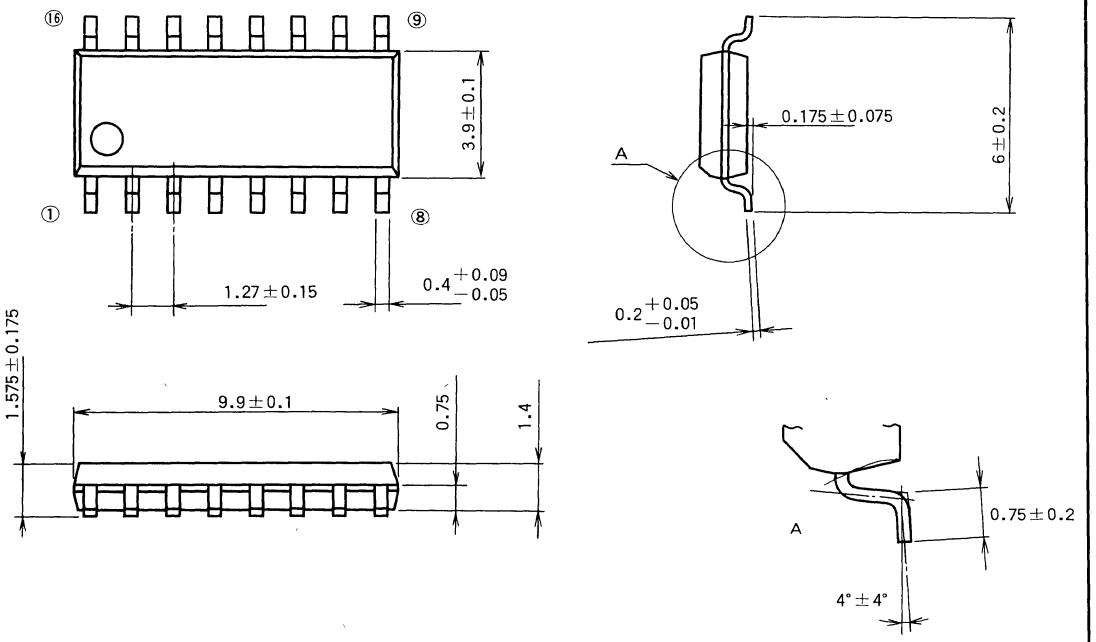
TYPE 14P2P 14-PIN MOLDED PLASTIC SOP(JEDEC 150mil body)

Dimension in mm



TYPE 16P2P 16-PIN MOLDED PLASTIC SOP(JEDEC 150mil body)

Dimension in mm

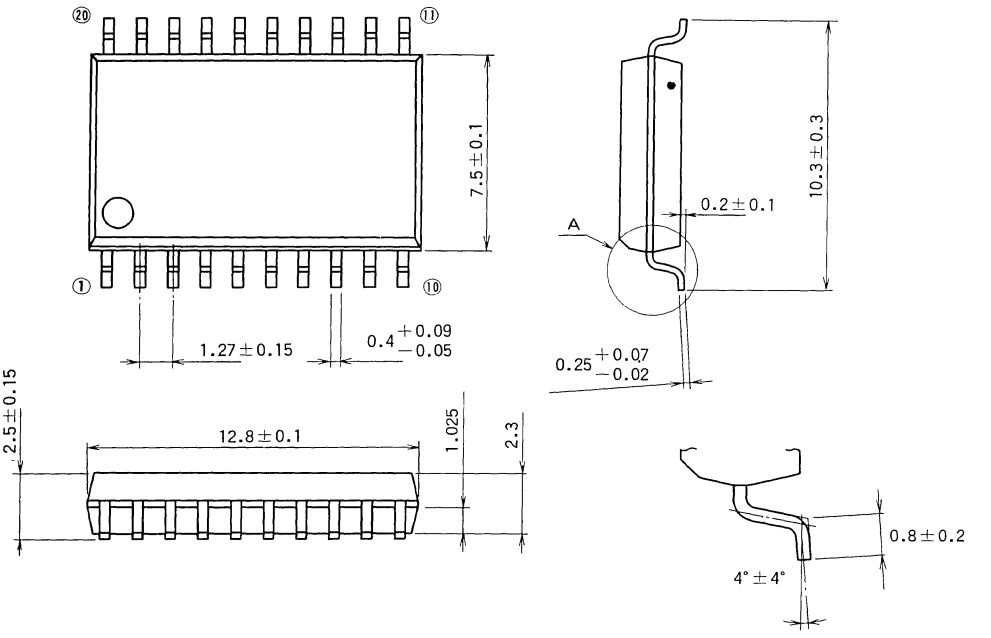


MITSUBISHI ELECTRIC

PACKAGE OUTLINES

TYPE 20P2V 20-PIN MOLDED PLASTIC SOP(JEDEC 300mil body)

Dimension in mm



DATA SHEETS

2

M74HC00P
M74HC00DP

QUADRUPLE 2-INPUT POSITIVE NAND GATE

DESCRIPTION

The M74HC00 is a semiconductor integrated circuit consisting of four 2-input positive-logic NAND, usable as negative-logic NOR gates.

FEATURES

- High-speed: 8ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC00 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS00.

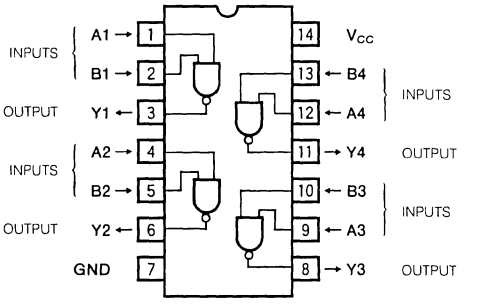
Buffered outputs Y improve input-to-output transfer characteristics and reduce to a minimum output impedance variations with respect to input voltage variations.

When both inputs A and B are high, the output Y will become low, and when at least one of the inputs is low, the output Y will become high.

FUNCTION TABLE

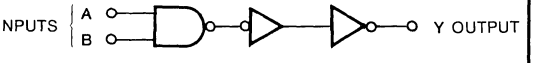
Inputs		Output
A	B	Y
L	L	H
H	L	H
L	H	H
H	H	L

PIN CONFIGURATION (TOP VIEW)



Outline 14P4
14P2P

LOGIC DIAGRAM (EACH GATE)



ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 1 : M74HC00DP, T_a = −40~+50℃ and T_a = 50~85℃ are derated at −5mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits						Unit
				25℃			−40∼+85℃			
				V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			1.0		10.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

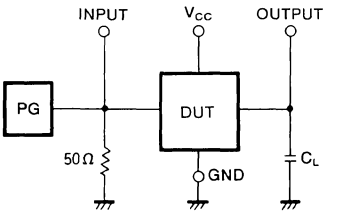
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 3)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time				15	ns
t_{PHL}					15	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40~+85℃		
		V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0		75		95	ns
			4.5		15		19	
			6.0		13		16	
t_{THL}			2.0		75		95	
			4.5		15		19	
			6.0		13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time		2.0		90		113	ns
			4.5		18		23	
			6.0		15		19	
t_{PHL}			2.0		90		113	
			4.5		18		23	
			6.0		15		19	
C_I	Input capacitance				10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)			25				pF

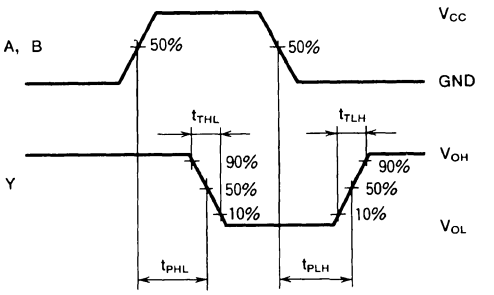
Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per gate)
The power dissipated during operation under no-load conditions is calculated using the following formula
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 3 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%) t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM



M74HC02P
M74HC02DP

QUADRUPLE 2-INPUT POSITIVE NOR GATE

DESCRIPTION

The M74HC02 is a semiconductor integrated circuit consisting of four 2-input positive-logic NOR, usable as negative-logic NAND gates.

FEATURES

- High-speed: 8ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC02 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS02.

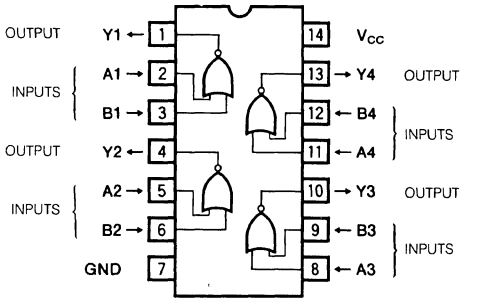
Buffered outputs Y improve input-to-output transfer characteristics and reduce to a minimum output impedance variations with respect to input voltage variations.

When both inputs A and B are low, the output Y will become high, and when at least one of the inputs is high, the output Y will become low.

FUNCTION TABLE

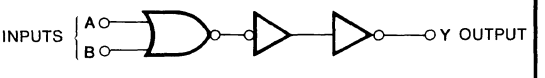
Inputs		Output
A	B	Y
L	L	H
H	L	L
L	H	L
H	H	L

PIN CONFIGURATION (TOP VIEW)



Outline 14P4
14P2P

LOGIC DIAGRAM (EACH GATE)



ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 1 : M74HC02DP, T_a = −40~+50℃ and T_a = 50~85℃ are derated at −5mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V, $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IL}, I_{OH} = −20μA	2.0	1.9			1.9		V
		I_{OH} = −20μA	4.5	4.4			4.4		
		I_{OH} = −20μA	6.0	5.9			5.9		
		I_{OH} = −4.0mA	4.5	4.18			4.13		
		I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}, I_{OL} = 20μA	2.0			0.1		0.1	V
		I_{OL} = 20μA	4.5			0.1		0.1	
		I_{OL} = 20μA	6.0			0.1		0.1	
		I_{OL} = 4.0mA	4.5			0.26		0.33	
		I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V	6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V	6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA	6.0			1.0		10.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

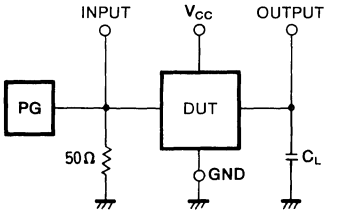
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 3)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time				15	ns
t_{PHL}					15	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time		2.0			90		113	ns
			4.5			18		23	
			6.0			15		19	
t_{PHL}			2.0			90		113	
			4.5			18		23	
			6.0			15		19	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				31				pF

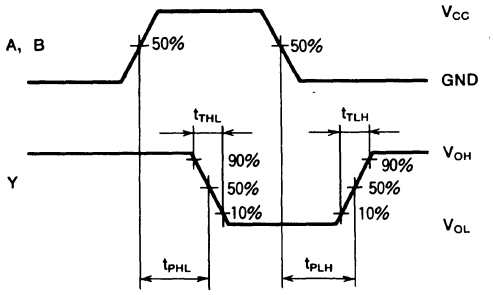
Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per gate)
The power dissipated during operation under no-load conditions is calculated using the following formula.
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 3 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%) · t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM



M74HC03P

QUADRUPLE 2-INPUT POSITIVE NAND GATE WITH OPEN-DRAIN OUTPUTS

DESCRIPTION

The M74HC03 is a semiconductor integrated circuit consisting of four 2-input positive-logic NAND usable as negative-logic NOR gates, with open-drain outputs.

FEATURES

- Open-drain outputs
- High-speed: 10ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC03 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS03.

Open-drain outputs permit a versatile selection of high output impedances by means of externally connected load resistors. This makes "AND ties" a possibility, unlike the case of normal gates.

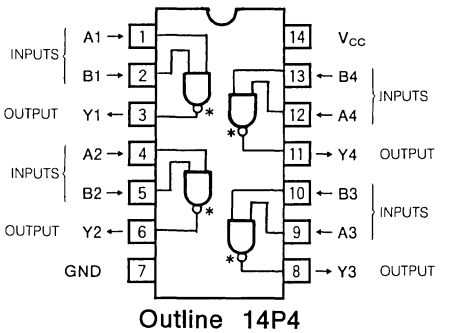
When both inputs A and B are high, the output Y will become low, and when at least one of the inputs is low, the output Y will become high.

Note that this IC differs from the 74LS03 and a voltage higher than V_{CC} can not be applied to the output.

FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

PIN CONFIGURATION (TOP VIEW)



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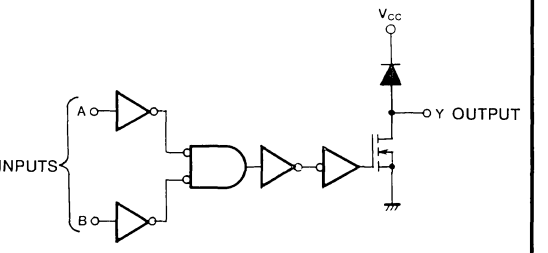
* Open-drain outputs

LOGIC DIAGRAM (EACH GATE)



QUADRUPLE 2-INPUT POSITIVE NAND GATE WITH OPEN-DRAIN OUTPUTS

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation		500	mW
Tstg	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA (Note 2)	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = V_{CC}−0.1V $\|I_O\|$ = 20μA (Note 2)	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OL}	Low-level output voltage	V_I = V_{IH}, I_{OL} = 20μA	2.0			0.1		0.1	V
			4.5			0.1		0.1	
			6.0			0.1		0.1	
		V_I = V_{IH}, I_{OL} = 4.0mA	4.5			0.26		0.33	
		V_I = V_{IH}, I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V	6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V	6.0			−0.1		−1.0	μA
I_O	Maximum output leakage current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}	6.0			0.5		5.0	μA
		V_I = V_{IH}, V_{IL}, V_O = GND	6.0			−0.5		−5.0	
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA	6.0			1.0		10.0	μA

QUADRUPLE 2-INPUT POSITIVE NAND GATE WITH OPEN-DRAIN OUTPUTS

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

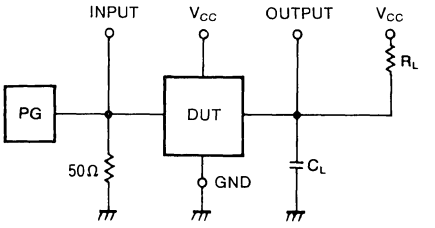
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{THL}	High-level to low-level output transition time	R_L = 1KΩ C_L = 15pF (Note 2)			10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time	R_L = 1KΩ, C_L = 5pF (Note 2)			20	ns
t_{PHL}		R_L = 1KΩ, C_L = 15pF (Note 2)			20	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	yp	Max	Min	Max	
t_{THL}	high-level to low-level output transition time	R_L = 1KΩ C_L = 50pF (Note 2)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time		2.0			125		158	ns
			4.5			25		32	
			6.0			21		27	
t_{PHL}			2.0			125		158	
			4.5			25		32	
			6.0			21		27	
C_I	Input capacitance					10		10	pF
C_O	Output capacitance	A or B = GND				10		10	pF
C_{PD}	Power dissipation capacitance (Note 1)				11				pF

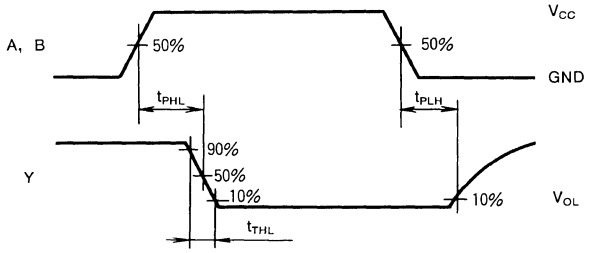
Note 1 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per gate)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 2 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%) t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM



M74HC04P
M74HC04DP

HEX INVERTER

DESCRIPTION

The M74HC04 is a semiconductor integrated circuit consisting of six inverters.

FEATURES

- High-speed: 10ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

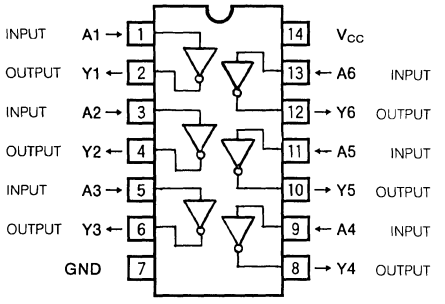
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC04 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS04.

Buffered outputs Y improve input-to-output transfer characteristics and reduce to a minimum output impedance variations with respect to input voltage variations.

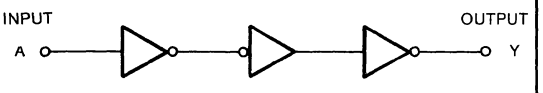
When input A is high, the output Y is low, and when input A is low, the output Y will become high.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4
14P2P

LOGIC DIAGRAM (EACH INVERTER)



FUNCTION TABLE

Input	Output
A	Y
L	H
H	L

ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 1 : M74HC04DP, T_a = −40~+50℃ and T_a = 50~85℃ are derated at −5mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits						Unit
				25℃			−40∼+85℃			
				V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V $\|I_O\|$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			1.0		10.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

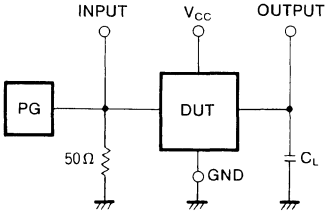
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 3)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time				17	ns
t_{PHL}					17	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time		2.0			86		108	ns
			4.5			19		24	
			6.0			16		20	
t_{PHL}			2.0			86		108	
			4.5			19		24	
			6.0			16		20	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				26				pF

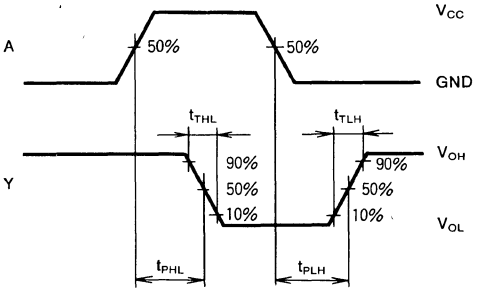
Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per inverter)
The power dissipated during operation under no-load conditions is calculated using the following formula·
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 3 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%). t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM



MITSUBISHI ELECTRIC

M74HCU04P
M74HCU04DP

HEX UNBUFFERED INVERTER

DESCRIPTION

The M74HCU04 is a semiconductor integrated circuit consisting of six unbuffered inverters.

FEATURES

- High-speed· 7ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HCU04 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS04.

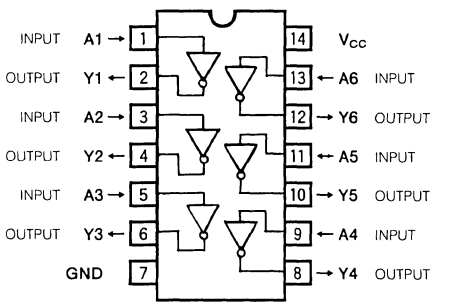
Unbuffered outputs Y make this device suitable for linear circuit applications such as oscillators and amplifier circuits as well as logic system applications. However, consideration must be given in linear circuit applications dissipated power is much greater than of the 4000B series.

When input A is high, the output Y will become low, and when input A is low, the output Y will become high.

FUNCTION TABLE

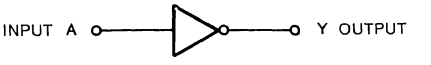
Input	Output
A	Y
L	H
H	L

PIN CONFIGURATION (TOP VIEW)



Outline 14P4
14P2P

LOGIC DIAGRAM (EACH INVERTER)



ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 1 : M74HCU04DP, T_a = −40~+50℃ and T_a = 50~85℃ are derated at −5mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40~+85℃)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	2		6	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
T_{opr}	Operating temperature range	−40		+85	℃
t_r, t_f	Input risetime, falltime	No Limit			ns

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.2V, $\|I_O\|$ = 20μA	2.0	1.7			1.7		V
		V_O = 0.5V, $\|I_O\|$ = 20μA	4.5	3.6			3.6		
		V_O = 0.5V, $\|I_O\|$ = 20μA	6.0	4.8			4.8		
V_{IL}	Low-level input voltage	V_O = V_{CC}−0.2V, $\|I_O\|$ = 20μA	2.0			0.3		0.3	V
		V_O = V_{CC}−0.5V, $\|I_O\|$ = 20μA	4.5			0.8		0.8	
		V_O = V_{CC}−0.5V, $\|I_O\|$ = 20μA	6.0			1.1		1.1	
V_{OH}	High-level output voltage	V_I = V_{IL}, I_{OH} = −20μA	2.0	1.8			1.8		V
			4.5	4.0			4.0		
			6.0	5.5			5.5		
		V_I = GND, I_{OH} = −4.0mA	4.5	3.98			3.84		
		V_I = GND, I_{OH} = −5.2mA	6.0	5.48			5.34		
V_{OL}	Low-level output voltage	V_I = V_{IH}, I_{OL} = 20μA	2.0			0.2		0.2	V
			4.5			0.5		0.5	
			6.0			0.5		0.5	
		V_I = V_{CC}, I_{OL} = 4.0mA	4.5			0.26		0.33	
		V_I = V_{CC}, I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V	6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V	6.0			−0.1		−1.0	
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA	6.0			1.0		10.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

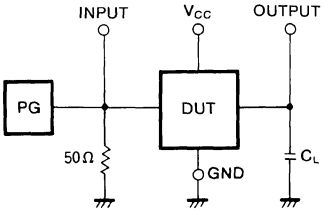
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level	C_L = 15pF (Note 3)			10	ns
t_{THL}	output transition time				10	
t_{PLH}	Low-level to high-level and high-level to low-level				13	ns
t_{PHL}	output propagation time				13	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time		2.0			82		103	ns
			4.5			16		21	
			6.0			14		18	
t_{PHL}			2.0			82		103	
			4.5			16		21	
			6.0			14		18	
C_I	Input capacitance					15		15	pF
C_{PD}	Power dissipation capacitance (Note 2)				25				pF

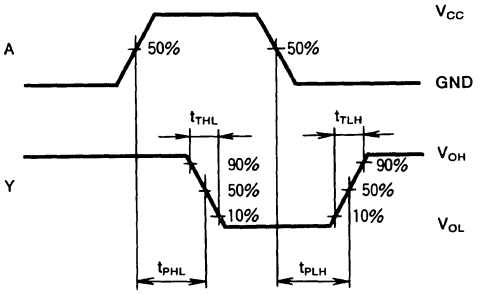
Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per inverter)
The power dissipated during operation under no-load conditions is calculated using the following formula
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 3 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%) t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM



M74HC08P
M74HC08DP

QUADRUPLE 2-INPUT POSITIVE AND GATE

DESCRIPTION

The M74HC08 is a semiconductor integrated circuit consisting of four 2-input positive-logic AND, usable as negative-logic OR gates.

FEATURES

- High-speed: 9.5ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

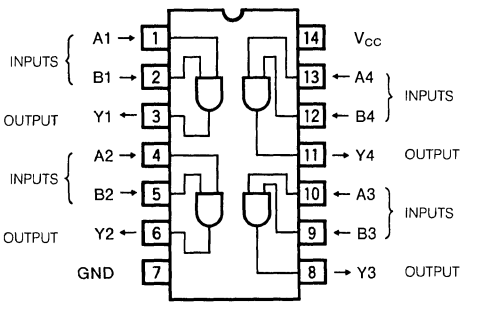
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC08 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS08.

Buffered outputs Y improve input-to-output transfer characteristics and reduce to a minimum output impedance variations with respect to input voltage variations.

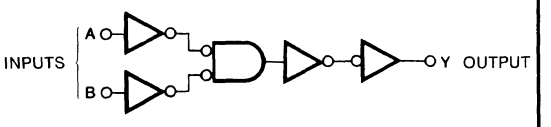
When both inputs A and B are high, the output Y will become high, and when at least one of the inputs is low, the output Y will become low.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4
14P2P

LOGIC DIAGRAM (EACH GATE)



FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	L
H	L	L
L	H	L
H	H	H

ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 1 : M74HC08DP, T_a = −40~+50℃ and T_a = 50~85℃ are derated at −5mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		V_{CC}(V)	Limits					Unit
					25℃			−40∼+85℃		
					Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V $\|I_O\|$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			1.0		10.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

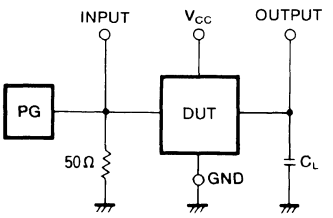
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 3)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time				15	ns
t_{PHL}					20	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time		2.0			121		151	ns
			4.5			24		30	
			6.0			20		25	
t_{PHL}			2.0			121		151	
			4.5			24		30	
			6.0			20		25	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				40				pF

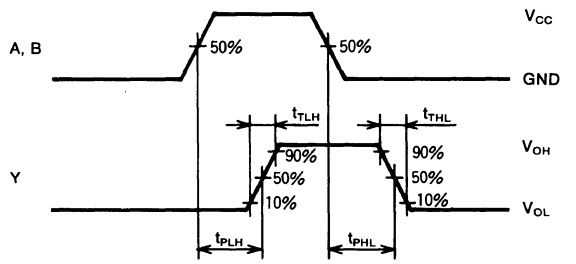
Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per gate)
The power dissipated during operation under no-load conditions is calculated using the following formula·
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 3 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%) t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM



M74HC10P
M74HC10DP

TRIPLE 3-INPUT POSITIVE NAND GATE

DESCRIPTION

The M74HC10 is a semiconductor integrated circuit consisting of three 3-input positive-logic NAND, usable as negative-logic NOR gates.

FEATURES

- High-speed: 10ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC10 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS10.

Buffered outputs Y improve input-to-output transfer characteristics and reduce to a minimum output impedance variations with respect to input voltage variations.

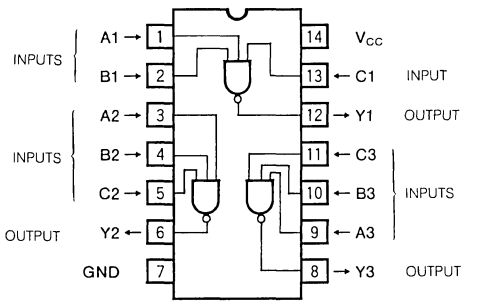
When all inputs A, B and C are high, the output Y will become low, and when at least one of the inputs is low, the output Y will become high.

FUNCTION TABLE

Inputs		Output
A	N	Y
L	L	H
H	L	H
L	H	H
H	H	L

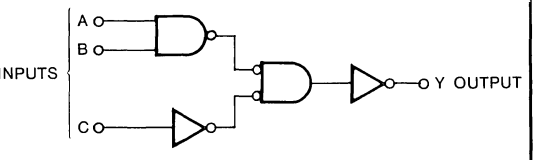
N = B C

PIN CONFIGURATION (TOP VIEW)



Outline 14P4
14P2P

LOGIC DIAGRAM (EACH GATE)



ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 1 : M74HC10DP, T_a = −40~+50℃ and T_a = 50~85℃ are derated at −5mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			1.0		10.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

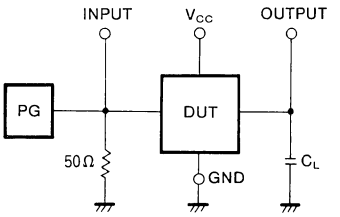
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 3)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time				15	ns
t_{PHL}					15	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time		2.0			95		120	ns
			4.5			19		24	
			6.0			16		20	
t_{PHL}			2.0			95		120	
			4.5			19		24	
			6.0			16		20	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				36				pF

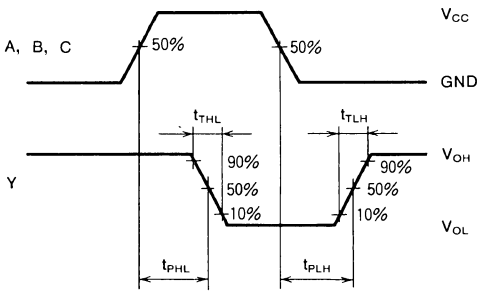
Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per gate)
The power dissipated during operation under no-load conditions is calculated using the following formula
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$

Note 3 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%) t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM



M74HC11P
M74HC11DP

TRIPLE 3-INPUT POSITIVE AND GATE

DESCRIPTION

The M74HC11 is a semiconductor integrated circuit consisting of three 3-input positive-logic AND, usable as negative-logic OR gates.

FEATURES

- High-speed: 12ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC11 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS11.

Buffered outputs Y improve the input-to-output transfer characteristics and reduce to a minimum output impedance variations with respect to input voltage variations.

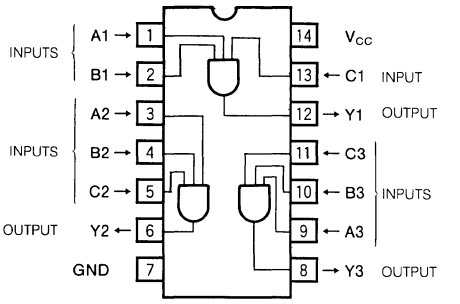
When all inputs A, B and C are high, the output Y will become high, and when at least one of the inputs is low, the output Y will become low.

FUNCTION TABLE

Inputs		Output
A	N	Y
L	L	L
H	L	L
L	H	L
H	H	H

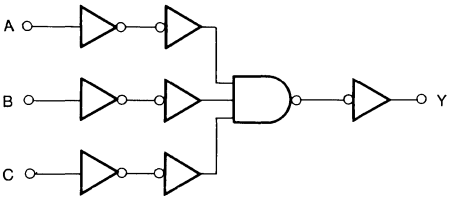
N = B·C

PIN CONFIGURATION (TOP VIEW)



Outline 14P4, 14P2P

LOGIC DIAGRAM (EACH GATE)



ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 1 : M74HC11DP, T_a = −40~+50℃ and T_a = 50~85℃ are derated at −5mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		V_{CC}(V)	Limits 25℃ Min	Limits 25℃ Typ	Limits 25℃ Max	Limits −40∼+85℃ Min	Limits −40∼+85℃ Max	Unit
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V $\|I_O\|$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			1.0		10.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

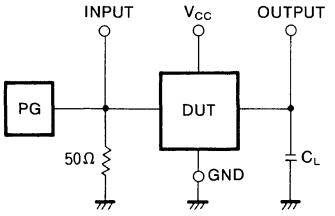
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 3)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time				20	ns
t_{PHL}					20	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time		2.0			125		156	ns
			4.5			25		31	
			6.0			21		27	
t_{PHL}			2.0			125		156	
			4.5			25		31	
			6.0			21		27	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				34				pF

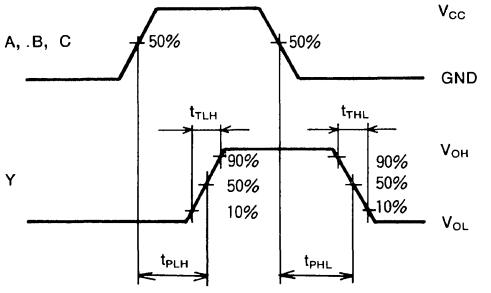
Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per gate)
The power dissipated during operation under no-load conditions is calculated using the following formula
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 3 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%) t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM



M74HC14P
M74HC14DP

HEX SCHMITT-TRIGGER INVERTER

DESCRIPTION

The M74HC14 is a semiconductor integrated circuit consisting of six Schmitt-trigger inverters.

FEATURES

- High-speed: 12ns typ. (C_L=15pF, V_{CC}=5V)
- Wide hysteresis voltage width: 0.8V (V_{CC} = 5V, typ)
- Low power dissipation: 5μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

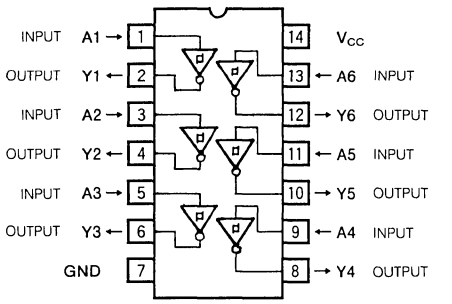
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC14 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS14.

Built-in Schmitt-trigger circuits prevent the occurrence of incorrect oscillations even when input signals having slow rise and fall times are applied. The Schmitt triggers ensure a signal of restored waveshape will appear at the output

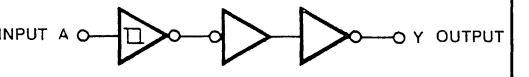
When input A is high, the output Y will become low, and when input A is low, the output Y will become high.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4
14P2P

LOGIC DIAGRAM (EACH SCHMITT-TRIGGER)



FUNCTION TABLE

Input	Output
A	Y
L	H
H	L

ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 1 : M74HC14DP, T_a = −40~+50℃ and T_a = 50~85℃ are derated at −5mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	2		6	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
T_{opr}	Operating temperature range	−40		+85	℃
t_r, t_f	Input risetime, falltime	no restriction			

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
					25℃			−40∼+85℃	
				V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{T+}	Postive-going threshold voltage	V_O = 0.1V $\|I_O\|$ = 20μA		2.0	0.7		1.5	0.7	1.5	V
				4.5	1.55		3.15	1.55	3.15	
				6.0	2.1		4.2	2.1	4.2	
V_{T-}	Negative-going threshold voltage	V_O = V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0	0.3		1.0	0.3	1.0	V
				4.5	0.9		2.45	0.9	2.45	
				6.0	1.2		3.2	1.2	3.2	
V_H	Hysteresis voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0	0.2		1.2	0.2	1.2	V
				4.5	0.4		2.1	0.4	2.1	
				6.0	0.5		2.5	0.5	2.5	
V_{OH}	High-level output voltage	V_I = V_{T-}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{T+}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			1.0		10.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

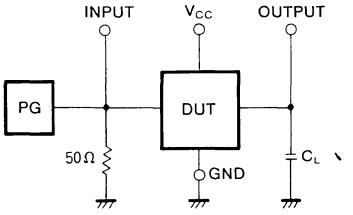
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 3)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time				22	ns
t_{PHL}					22	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time		2.0			125		156	ns
			4.5			25		31	
			6.0			21		26	
t_{PHL}			2.0			125		156	
			4.5			25		31	
			6.0			21		26	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				29				pF

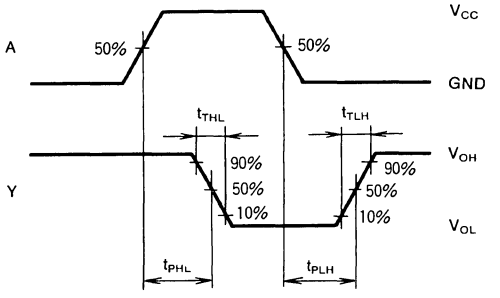
Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per inverter)
The power dissipated during operation under no-load conditions is calculated using the following formula·
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 3 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%) t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM



M74HC20P
M74HC20DP

DUAL 4-INPUT POSITIVE NAND GATE

DESCRIPTION

The M74HC20 is a semiconductor integrated circuit consisting of two 4-input positive-logic NAND, usable as negative-logic NOR gates.

FEATURES

- High-speed: 8ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

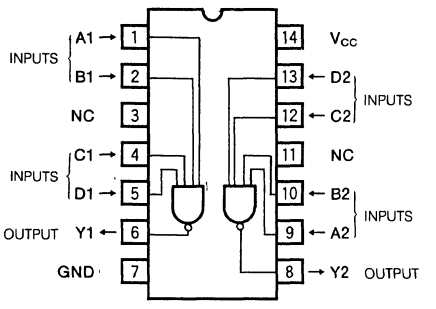
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC20 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS20.

Buffered output Y improve input-to-output transfer characteristics and reduce to a minimum output impedance variations with respect to input voltage variations.

When all inputs A, B, C and D are high, the output Y will become low, and when at least one of the inputs is low, the output Y will become high.

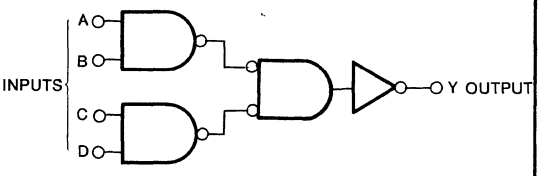
PIN CONFIGURATION (TOP VIEW)



Outline 14P4
14P2P

NC : No connection

LOGIC DIAGRAM (EACH GATE)



FUNCTION TABLE

Inputs		Output
A	N	Y
L	L	H
H	L	H
L	H	H
H	H	L

N = B·C·D

ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 1 : M74HC20DP, T_a = −40~+50℃ and T_a = 50~85℃ are derated at −5mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			1.0		10.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

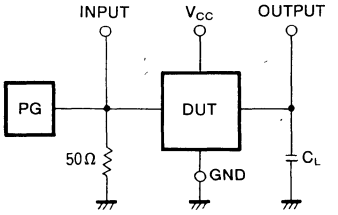
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 3)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time				15	ns
t_{PHL}					15	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time		2.0			90		113	ns
			4.5			18		23	
			6.0			15		19	
t_{PHL}			2.0			90		113	
			4.5			18		23	
			6.0			15		19	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				34				pF

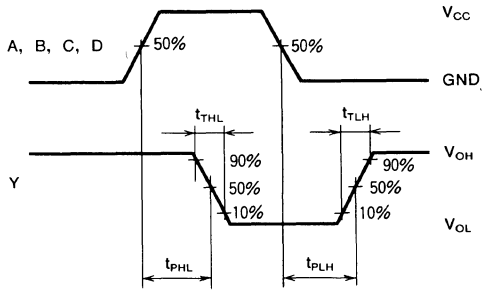
Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per gate)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 3 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%) t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM



M74HC27P
M74HC27DP

TRIPLE 3-INPUT POSITIVE NOR GATE

DESCRIPTION

The M74HC27 is a semiconductor integrated circuit consisting of three 3-input positive-logic NOR, usable as negative-logic NAND gates.

FEATURES

- High-speed: 8ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC27 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS27.

Buffered outputs Y improve input-to-output transfer characteristics and reduce to a minimum output impedance variations with respect to input voltage variations.

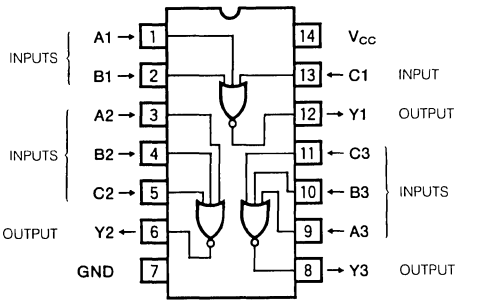
When all inputs A, B and C are low, the output Y will become high, and when at least one of the inputs is high, the output Y will become low.

FUNCTION TABLE

Inputs		Output
A	N	Y
L	L	H
H	L	L
L	H	L
H	H	L

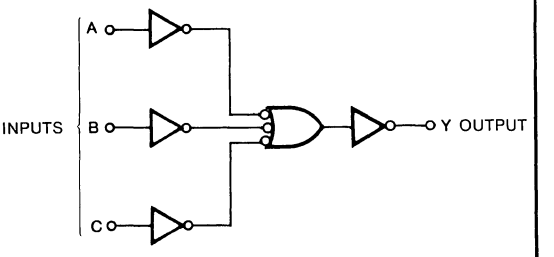
N = B + C

PIN CONFIGURATION (TOP VIEW)



Outline 14P4
14P2P

LOGIC DIAGRAM (EACH GATE)



ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 1 : M74HC27DP, T_a = −40~+50℃ and T_a = 50~85℃ are derated at −5mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits						Unit
				25℃			−40∼+85℃			
				V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, $\|I_O\|$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V, $\|I_O\|$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			1.0		10.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

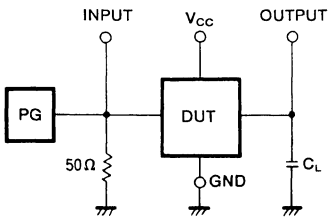
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 3)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time				15	ns
t_{PHL}					15	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time		2.0			90		113	ns
			4.5			18		23	
			6.0			15		19	
t_{PHL}			2.0			90		113	
			4.5			18		23	
			6.0			15		19	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				34				pF

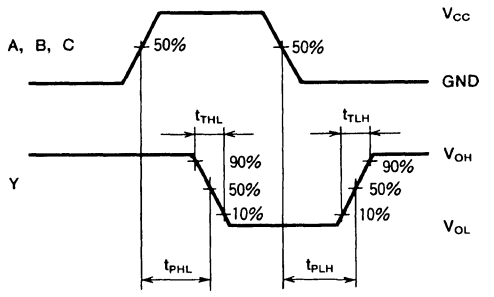
Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per gate)
The power dissipated during operation under no-load conditions is calculated using the following formula·
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 3 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



M74HC32P
M74HC32DP

QUADRUPLE 2-INPUT POSITIVE OR GATE

DESCRIPTION

The M74HC32 is a semiconductor integrated circuit consisting of four 2-input positive-logic OR, usable as negative-logic AND gates.

FEATURES

- High-speed: 10ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

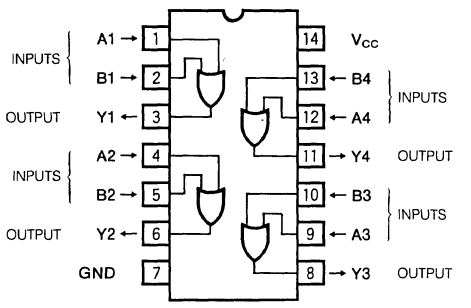
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC32 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS32.

Buffered outputs Y improve input-to-output transfer characteristics and reduce to a minimum output impedance variations with respect to input voltage variations.

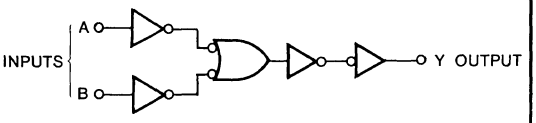
When both inputs A and B are low, the output Y is low, and when at least one of the inputs is high, the output Y is high.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4
14P2P

LOGIC DIAGRAM (EACH GATE)



FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	L
H	L	H
L	H	H
H	H	H

ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 1 : M74HC32DP, T_a = −40~+50℃ and T_a = 50~85℃ are derated at −5mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = V_{CC}−0.1V, $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V, $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			1.0		10.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

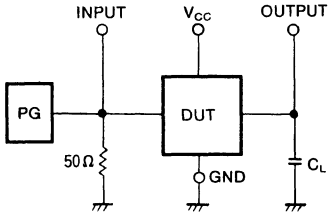
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 3)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time				18	ns
t_{PHL}					18	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time		2.0			100		125	ns
			4.5			20		25	
			6.0			17		21	
t_{PHL}			2.0			100		125	
			4.5			20		25	
			6.0			17		21	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				30				pF

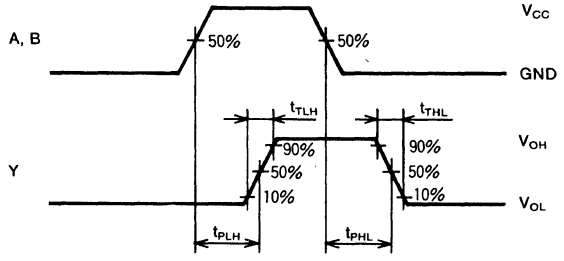
Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per gate)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 3 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



M74HC42P

1-OF-10 DECODER

DESCRIPTION

The M74HC42 is a semiconductor integrated circuit consisting of a BCD to decimal decoder.

FEATURES

- Active-low output
- High speed: 17ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

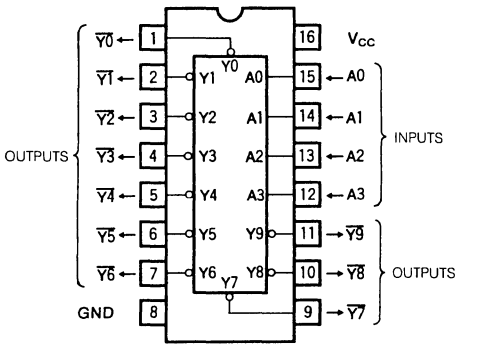
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC42 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS42.

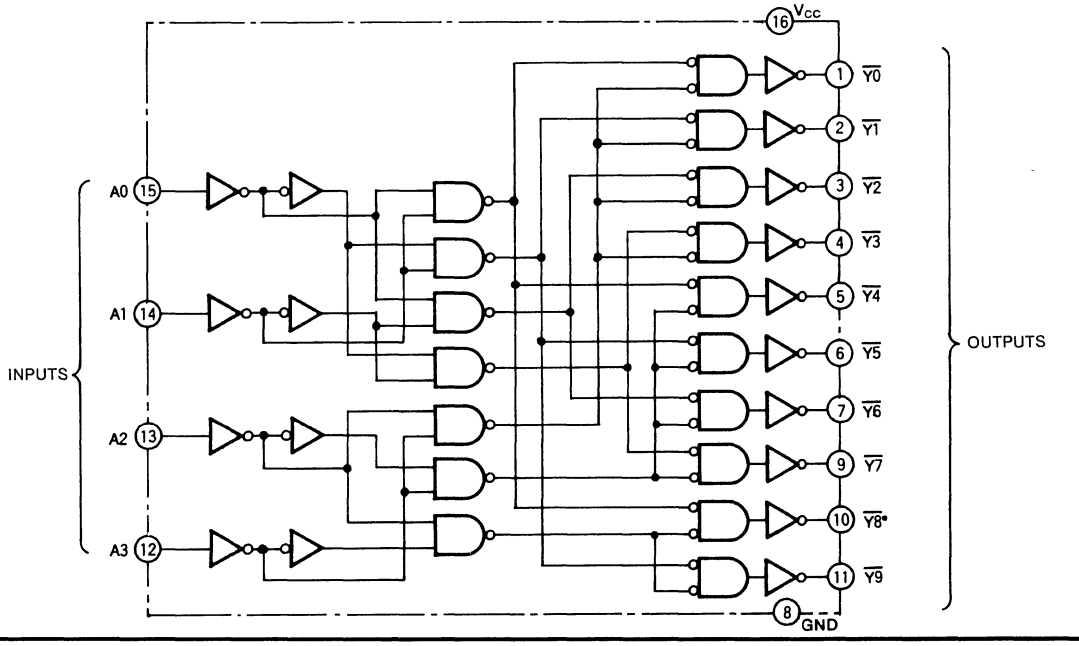
When a BCD code is applied to inputs A0, A1, A2 and A3, one of outputs $\overline{Y0}$ through $\overline{Y9}$ corresponding to this value will become low and all others will become high. Use A0 for the least significant bit and A3 for the most significant bit. If a value of ten or greater is applied to the inputs (A0 through A3), all outputs will become high.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

LOGIC DIAGRAM



FUNCTION TABLE

Decimal number	Inputs				Outputs									
	A3	A2	A1	A0	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$	$\overline{Y8}$	$\overline{Y9}$
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
10	H	L	H	L	H	H	H	H	H	H	H	H	H	H
11	H	L	H	H	H	H	H	H	H	H	H	H	H	H
12	H	H	L	L	H	H	H	H	H	H	H	H	H	H
13	H	H	L	H	H	H	H	H	H	H	H	H	H	H
14	H	H	H	L	H	H	H	H	H	H	H	H	H	H
15	H	H	H	H	H	H	H	H	H	H	H	H	H	H

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation		500	mW
Tstg	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

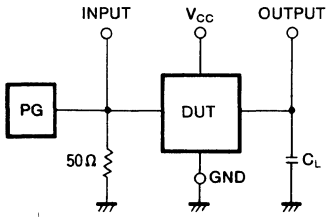
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 2)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time				25	ns
t_{PHL}					25	

SWITCHING CHARACTERISTICS (V_{CC} = 2～6V, T_a = −40～+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40～+85℃		
		V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 2)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time		2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHL}			2.0			150		189	
			4.5			30		38	
			6.0			26		32	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 1)				86				pF

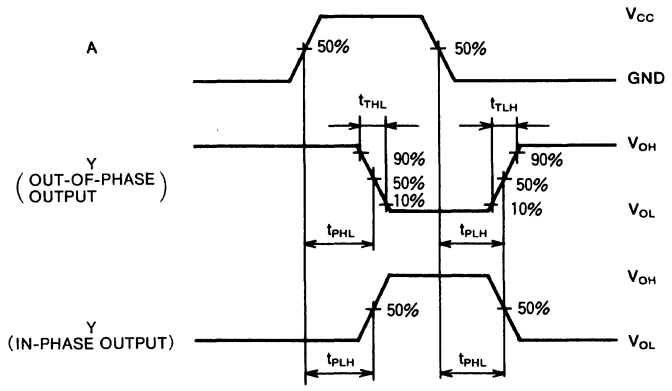
Note 1 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$

Note 2 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM



MITSUBISHI ELECTRIC

M74HC73P

DUAL J-K FLIP-FLOP WITH RESET

DESCRIPTION

The M74HC73 is a semiconductor integrated circuit consisting of two negative-edge triggered J-K flip flops with independent control inputs.

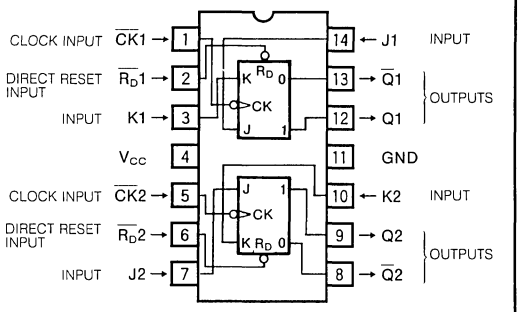
FEATURES

- High-speed: (clock frequency) 50MHz typ. (C_L=15pF V_{CC}=5V)
- Low power dissipation: 10μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

FUNCTIONAL DESCRIPTION

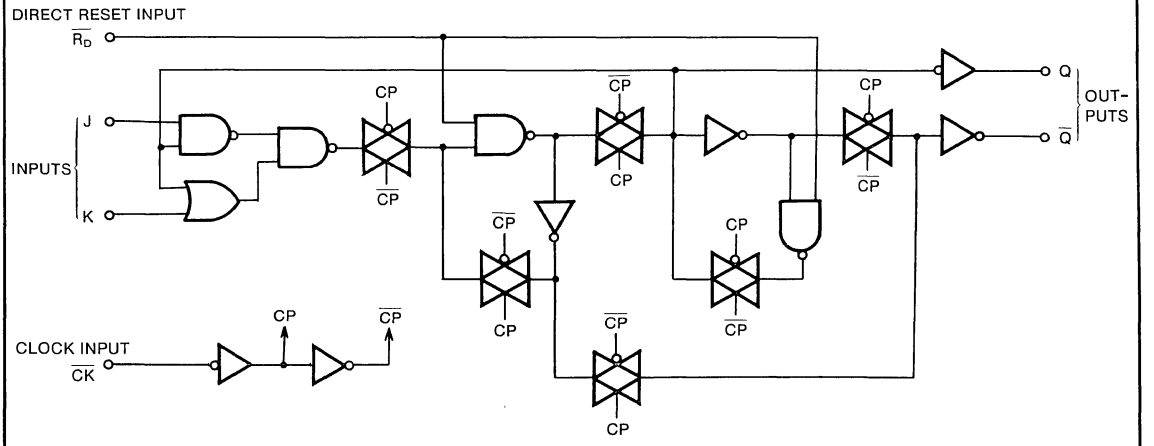
Use of silicon gate technology allows the M74HC73 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS73.

The M74HC73 contains two edge-triggered J-K flip flops, each circuit with independent clock input $\overline{CK}$, direct reset input $\overline{R_D}$, and both inputs J and K.

When $\overline{CK}$ changes from high-level to low-level, the signals just previously input at J and K appear at outputs Q and $\overline{Q}$ in accordance with the function table given. When $\overline{R_D}$ is low, Q and $\overline{Q}$ will become low and high respectively, irrespective of other inputs. When used as a J-K flip flop, $\overline{R_D}$ should be maintained at high.

A unit, the M74HC107, having the same functions and electrical characteristics as the M74HC73 is also available. This offers easy mounting with pins 7 and 14 being GND and V_{CC} respectively.

LOGIC DIAGRAM (EACH FLIP FLOP)



FUNCTION TABLE (Note 1)

Inputs				Outputs	
$\overline{R_D}$	$\overline{CK}$	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q^0	$\overline{Q}^0$
H	↓	L	H	L	H
H	↓	H	L	H	L
H	↓	H	H	Toggle	
H	L	X	X	Q^0	$\overline{Q}^0$
H	H	X	X	Q^0	$\overline{Q}^0$
H	↑	X	X	Q^0	$\overline{Q}^0$

Note 1 : ↑ : Change from low to high level
↓ : Change from high to low level
X : Irrelevant
Q^0 : Output state Q before clock input changed
$\overline{Q}^0$: Output state $\overline{Q}$ before clock input changed.
Toggle : Inverted state before clock input changed

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation		500	mW
Tstg	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
				V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			2.0		20.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 3)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level output transition time				10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$ – Q, $\overline{Q}$)				28	ns
t_{PHL}					28	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{R_D}$ – Q, $\overline{Q}$)				34	ns
t_{PHL}					34	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

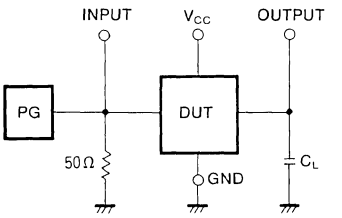
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 3)	2.0	5			4		MHz
			4.5	27			21		
			6.0	31			24		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$ – Q, $\overline{Q}$)		2.0			160		195	ns
			4.5			32		39	
			6.0			28		34	
t_{PHL}			2.0			160		195	
			4.5			32		39	
			6.0			28		34	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{R_D}$ – Q, $\overline{Q}$)		2.0			195		235	ns
			4.5			39		47	
			6.0			34		40	
t_{PHL}			2.0			195		235	
			4.5			39		47	
			6.0			34		40	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				109				pF

Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per flip flop)
The power dissipated during operation under no-load conditions is calculated using the following formula
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

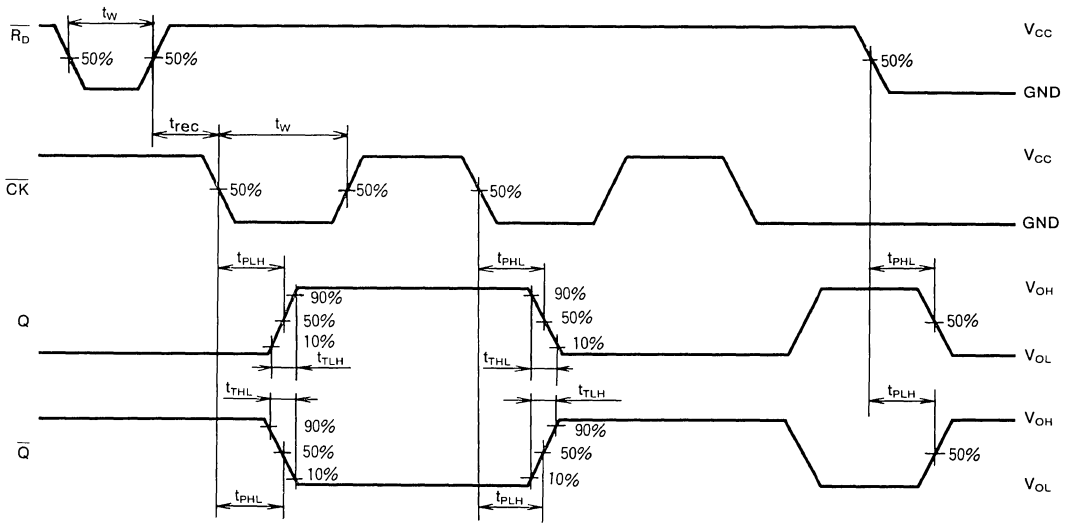
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	$\overline{CK}$, $\overline{R_D}$ pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
t_{su}	J, K setup time with respect to $\overline{CK}$		2.0	100			125		ns
			4.5	20			25		
			6.0	17			21		
t_h	J, K hold time with respect to $\overline{CK}$		2.0	0			0		ns
			4.5	0			0		
			6.0	0			0		
t_{rec}	$\overline{R_D}$ recovery time with respect to $\overline{CK}$		2.0	100			125		ns
			4.5	20			25		
			6.0	17			21		

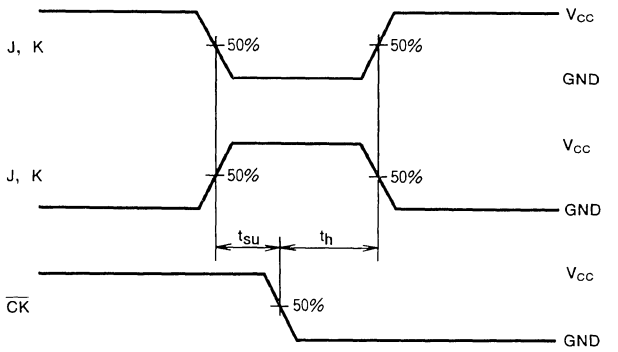
Note 3 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%) t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM





M74HC74P
M74HC74DP

DUAL D-TYPE FLIP-FLOP WITH SET AND RESET

DESCRIPTION

The M74HC74 is a semiconductor integrated circuit consisting of two positive-edge triggered D-types flip flops with independent clock, data, and direct set and reset inputs.

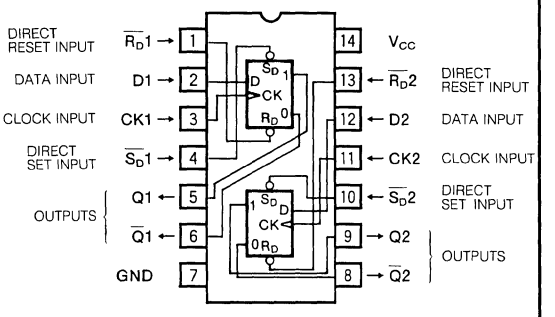
FEATURES

- High-speed: (clock frequency) 40MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 10μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4
14P2P

FUNCTIONAL DESCRIPTION

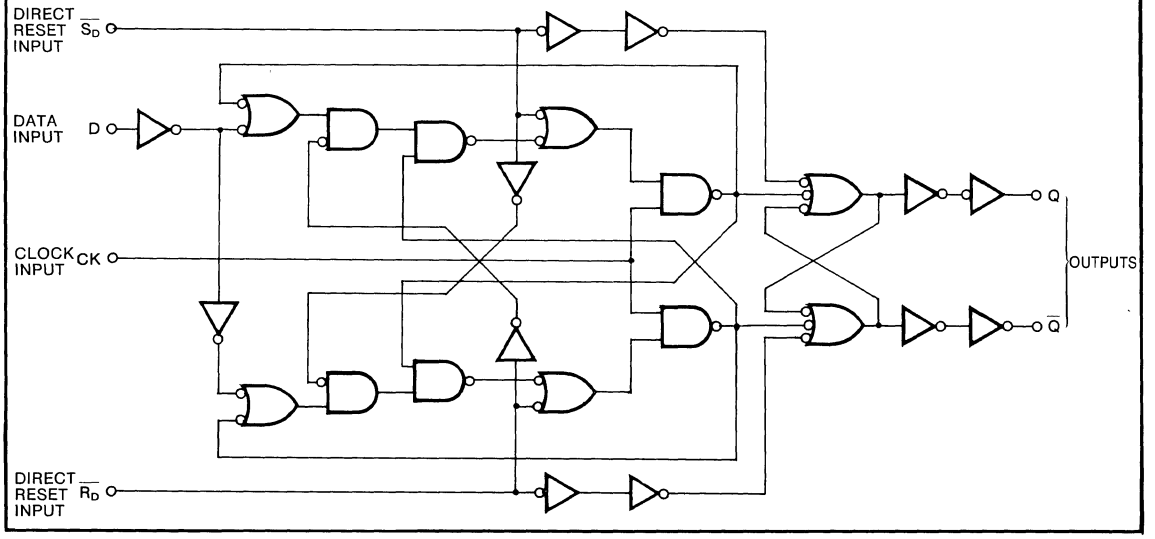
Use of silicon gate technology allows the M74HC74 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS74.

The M74HC74 contains two independent D-type flip flops, each circuit with independent clock input CK, direct set input $\overline{S_D}$, and direct reset input $\overline{R_D}$.

When used as a D-type flip flop, $\overline{S_D}$ and $\overline{R_D}$ should be maintained at high-level. When CK changes from low-level to high-level, the signals just previously input at D appears at outputs Q and $\overline{Q}$ in accordance with the function table given.

Use of $\overline{S_D}$ and $\overline{R_D}$ permits direct R-S flip flop operation. When $\overline{S_D}$ and $\overline{R_D}$ are low, Q and $\overline{Q}$ will both become high but when $\overline{S_D}$ and $\overline{R_D}$ simultaneously become high, the condition of Q and $\overline{Q}$ cannot be predetermined.

LOGIC DIAGRAM (EACH FLIP FLOP)



MITSUBISHI ELECTRIC

FUNCTION TABLE (Note 1)

Inputs				Outputs	
$\overline{S_D}$	$\overline{R_D}$	CK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	L	X	Q^0	$\overline{Q}^0$
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	H	X	Q^0	$\overline{Q}^0$
H	H	↓	X	Q^0	$\overline{Q}^0$

Note 1 : X : Irrelevant
↑ : Change from low to high level
↓ : Change from high to low level
Q^0 : Output state Q before clock input changed
$\overline{Q}^0$: Output state $\overline{Q}$ before clock input changed
* : When $\overline{S_D}$ and $\overline{R_D}$ are low, Q and $\overline{Q}$ will become both high-level but when $\overline{S_D}$ and $\overline{R_D}$ simultaneously become high, the condition of Q and $\overline{Q}$ cannot be predetermined

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC74DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			2.0		20.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

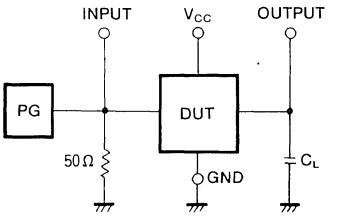
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 4)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level output transition time				10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q, $\overline{Q}$)				30	ns
t_{PHL}					30	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{S_D}$, $\overline{R_D}$ − Q, $\overline{Q}$)				40	ns
t_{PHL}					40	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	2.0	5			4		MHz
			4.5	27			21		
			6.0	32			25		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q, $\overline{Q}$)		2.0			175		220	ns
			4.5			35		44	
			6.0			30		37	
t_{PHL}			2.0			175		220	
			4.5			35		44	
			6.0			30		37	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{S_D}$, $\overline{R_D}$ − Q, $\overline{Q}$)		2.0			230		290	ns
			4.5			46		58	
			6.0			39		49	
t_{PHL}			2.0			230		290	
			4.5			46		58	
			6.0			39		49	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)				47				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per flip flop)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 4 : Test Circuit

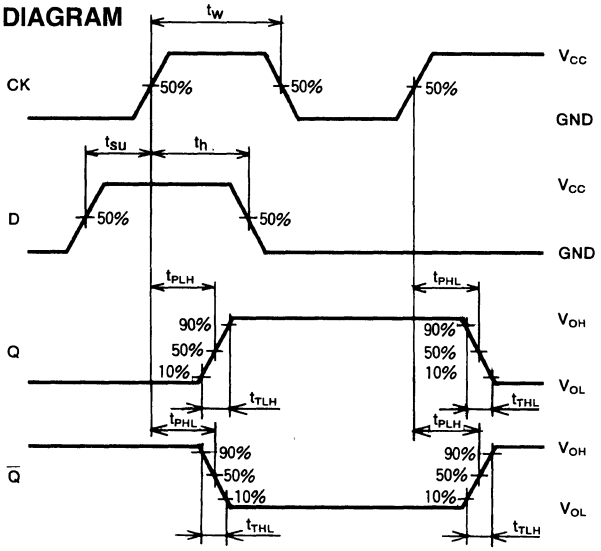


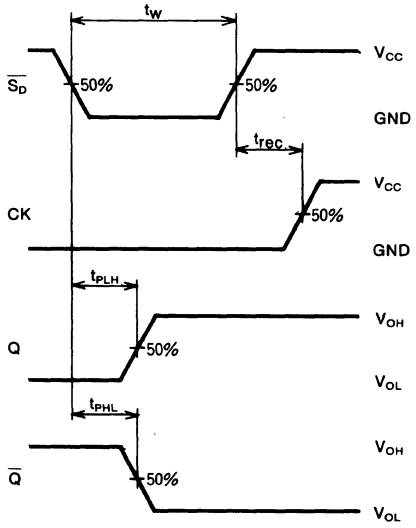
(1) The pulse generator (PG) has the following characteristics (10%~90%) t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

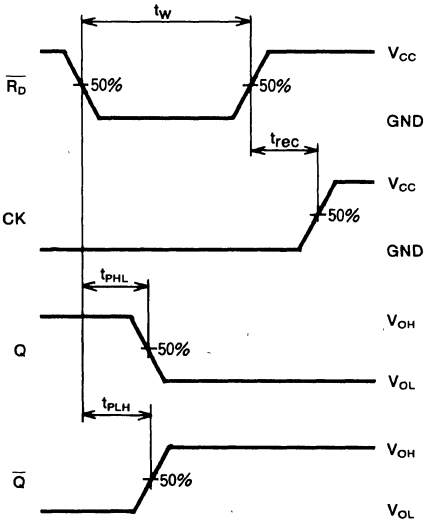
TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	CK, $\overline{S_D}$, $\overline{R_D}$ pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
t_{su}	D setup time with respect to CK		2.0	100			126		ns
			4.5	20			25		
			6.0	17			21		
t_h	D hold time with respect to CK		2.0	0			0		ns
			4.5	0			0		
			6.0	0			0		
t_{rec}	$\overline{S_D}$, $\overline{R_D}$ recovery time with respect to CK		2.0	5			5		ns
			4.5	5			5		
			6.0	5			5		

TIMING DIAGRAM







MITSUBISHI ELECTRIC

M74HC76P

DUAL J-K FLIP-FLOP WITH SET AND RESET

DESCRIPTION

The M74HC76 is a semiconductor integrated circuit consisting of two negative-edge triggered J-K flip flops with independent control inputs.

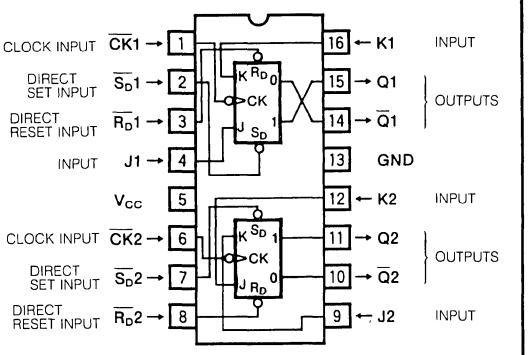
FEATURES

- High-speed: (clock frequency) 50MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 10μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

FUNCTIONAL DESCRIPTION

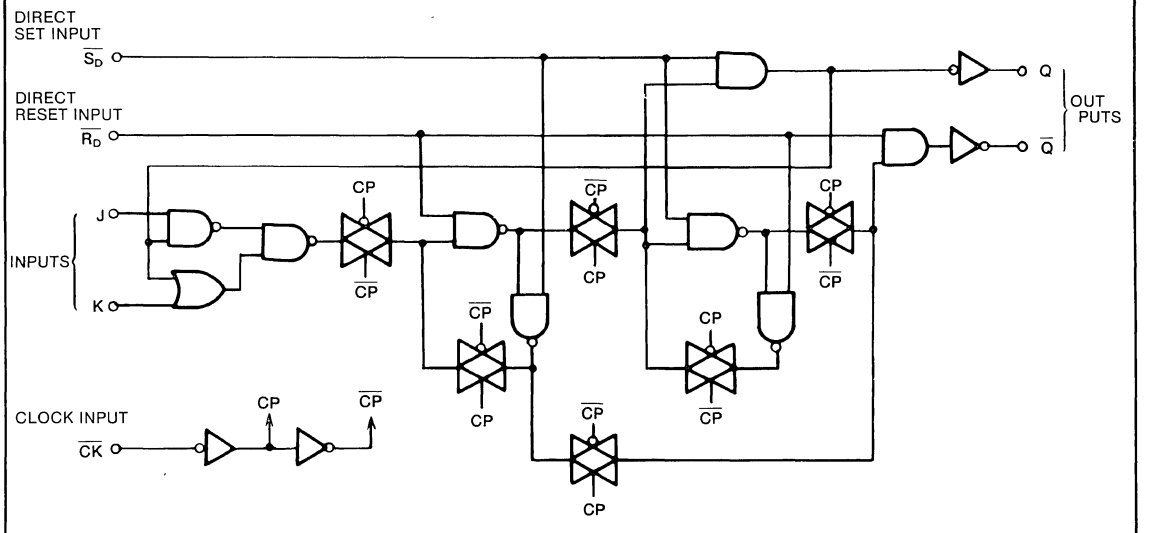
Use of silicon gate technology allows the M74HC76 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS76.

The M74HC76 contains two edge-triggered J-K flip flops, each circuit with independent clock input $\overline{CK}$, direct set input $\overline{S_D}$ and direct reset input $\overline{R_D}$, and both inputs J and K.

When $\overline{CK}$ changes from high-level to low-level, the signal just previously input at J and K appear at outputs Q and $\overline{Q}$ in accordance with the function table given. Use of $\overline{S_D}$ and $\overline{R_D}$ permits direct R-S flip flop operation. When $\overline{S_D}$ and $\overline{R_D}$ are low, Q and $\overline{Q}$ will both become high but when $\overline{S_D}$ and $\overline{R_D}$ simultaneously become high, the condition of Q and $\overline{Q}$ cannot be predetermined. When used as a J-K flip flop, $\overline{S_D}$ and $\overline{R_D}$ should be maintained at high-level.

A unit, the M74HC112, having the same functions and electrical characteristics as the M74HC76 is also avaiable. This offers easy mounting with pin 8 and 16 being GND and V_{CC} respectively.

LOGIC DIAGRAM (EACH FLIP FLOP)



FUNCTION TABLE (Note 1)

Inputs					Outputs	
$\overline{S_D}$	$\overline{R_D}$	$\overline{CK}$	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q^0	$\overline{Q}^0$
H	H	↓	L	H	L	H
H	H	↓	H	L	H	L
H	H	↓	H	H	Toggle	
H	H	L	X	X	Q^0	$\overline{Q}^0$
H	H	H	X	X	Q^0	$\overline{Q}^0$
H	H	↑	X	X	Q^0	$\overline{Q}^0$

Note 1 : ↑ : Change from low to high level
↓ : Change from high to low level
X : Irrelevant
Q^0 : Output state Q before clock input changed.
$\overline{Q}^0$: Output state $\overline{Q}$ before clock input changed
Toggle : Inverted state before clock input changed
* : When $\overline{S_D}$ and $\overline{R_D}$ are low, Q and $\overline{Q}$ will become both high-lvel but when $\overline{S_D}$ and $\overline{R_D}$ simultaneously become high, the condition of Q and $\overline{Q}$ cannot be predetermined.

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
Pd	Power dissipation		500	mW
Tstg	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40~+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			2.0		20.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 3)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level				10	ns
t_{THL}	output transition time				10	
t_{PLH}	Low-level to high-level and high-level to low-level				26	ns
t_{PHL}	output propagation time ($\overline{CK}$ − Q, $\overline{Q}$)				26	
t_{PLH}	Low-level to high-level and high-level to low-level				33	ns
t_{PHL}	output propagation time ($\overline{R_D}$ − Q, $\overline{Q}$)				33	
t_{PLH}	Low-level to high-level and high-level to low-level				33	ns
t_{PHL}	output propagation time ($\overline{S_D}$ − Q, $\overline{Q}$)				33	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

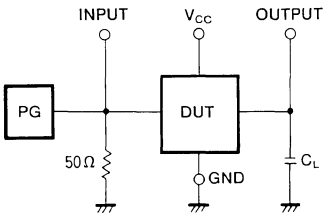
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 3)	2.0	5			4		MHz
			4.5	27			21		
			6.0	31			24		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$ − Q, $\overline{Q}$)		2.0			150		180	ns
			4.5			30		36	
			6.0			26		32	
t_{PHL}			2.0			150		180	
			4.5			30		36	
			6.0			26		32	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{R_D}$ − Q, $\overline{Q}$)		2.0			190		230	ns
			4.5			38		46	
			6.0			33		40	
t_{PHL}			2.0			190		230	
			4.5			38		46	
			6.0			33		40	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{S_D}$ − Q, $\overline{Q}$)		2.0			190		230	ns
			4.5			38		46	
			6.0			33		40	
t_{PHL}			2.0			190		230	
			4.5			38		46	
			6.0			33		40	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				86				pF

Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per flip flop)
The power dissipated during operation under no-load conditions is calculated using the following formula.
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

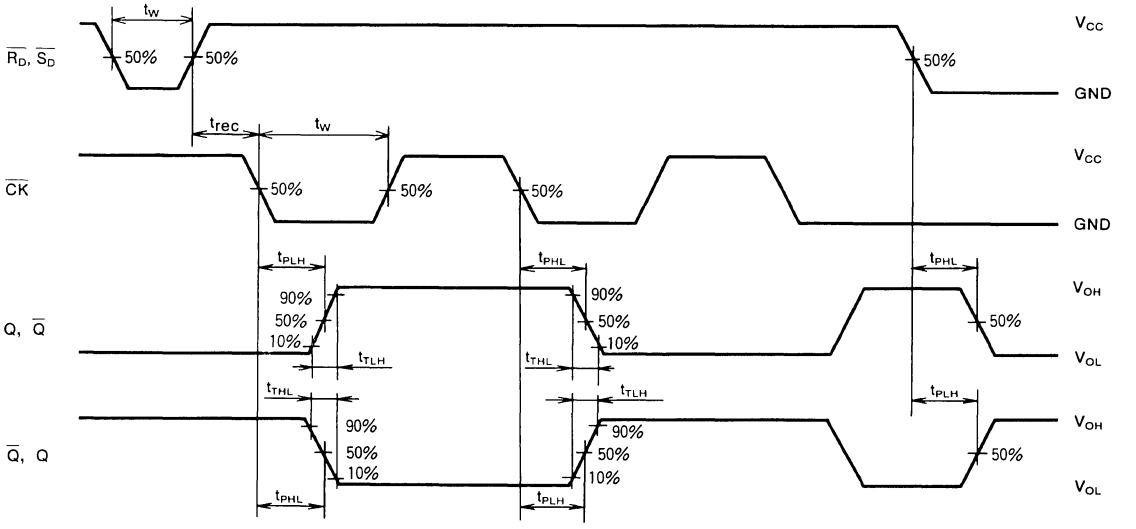
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	$\overline{CK}$, $\overline{S_D}$, $\overline{R_D}$ pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
t_{su}	J, K setup time with respect to $\overline{CK}$		2.0	100			125		ns
			4.5	20			25		
			6.0	17			21		
t_h	J, K hold time with respect to $\overline{CK}$		2.0	0			0		ns
			4.5	0			0		
			6.0	0			0		
t_{rec}	$\overline{S_D}$, $\overline{R_D}$ recovery time with respect to $\overline{CK}$		2.0	100			125		ns
			4.5	20			25		
			6.0	17			21		

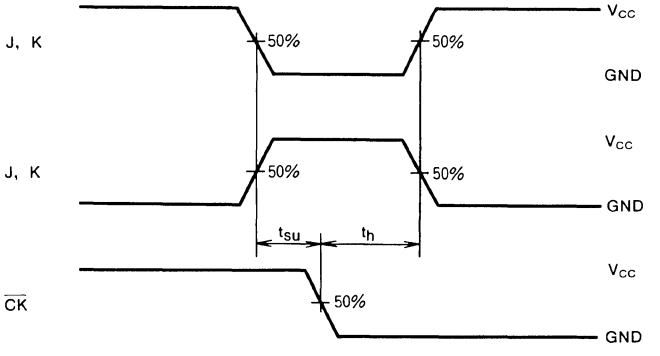
Note 3 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM





M74HC86P
M74HC86DP

QUADRUPLE 2-INPUT EXCLUSIVE OR GATE

DESCRIPTION

The M74HC86 is a semiconductor integrated circuit consisting of four 2-input exclusive OR gates.

FEATURES

- High-speed: 9ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

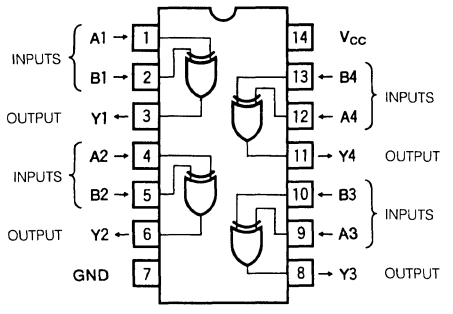
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC86 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS86.

Buffered outputs Y improve input-to-output transfer characteristics and reduce to a minimum output impedance variations with respect to input voltage variations.

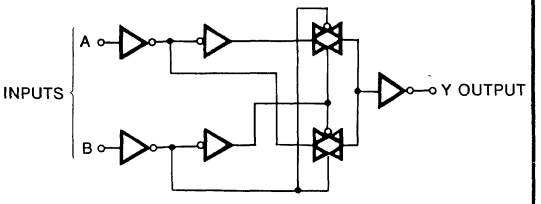
When both inputs A and B are either high or low, the output Y will become low, and when the levels of A and B are opposite, the output Y will become high.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4
14P2P

LOGIC DIAGRAM (EACH GATE)



FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	L
H	L	H
L	H	H
H	H	L

ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 1)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 1 : M74HC86DP, T_a = −40~+50℃ and T_a = 50~85℃ are derated at −5mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			1.0		10.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

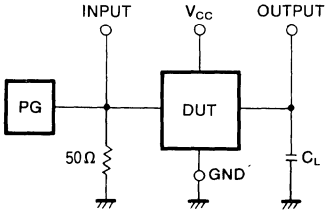
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 3)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time				20	ns
t_{PHL}					20	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time		2.0			120		151	ns
			4.5			24		30	
			6.0			20		26	
t_{PHL}			2.0			120		151	
			4.5			24		30	
			6.0			20		26	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				41				pF

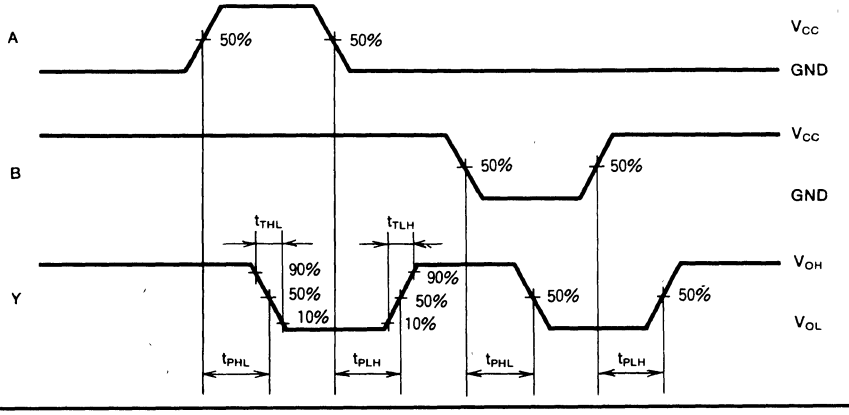
Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per gate)
The power dissipated during operation under no-load conditions is calculated using the following formula
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 3 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM



MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HC107P

DUAL J-K FLIP-FLOP WITH RESET

DESCRIPTION

The M74HC107 is a semiconductor integrated circuit consisting of two negative-edge triggered J-K flip flops with independent control inputs.

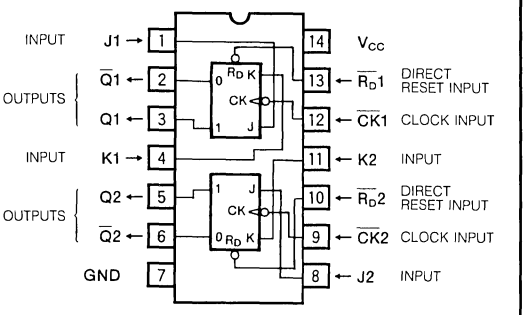
FEATURES

- High-speed: (clock frequency) 50MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 10μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

FUNCTIONAL DESCRIPTION

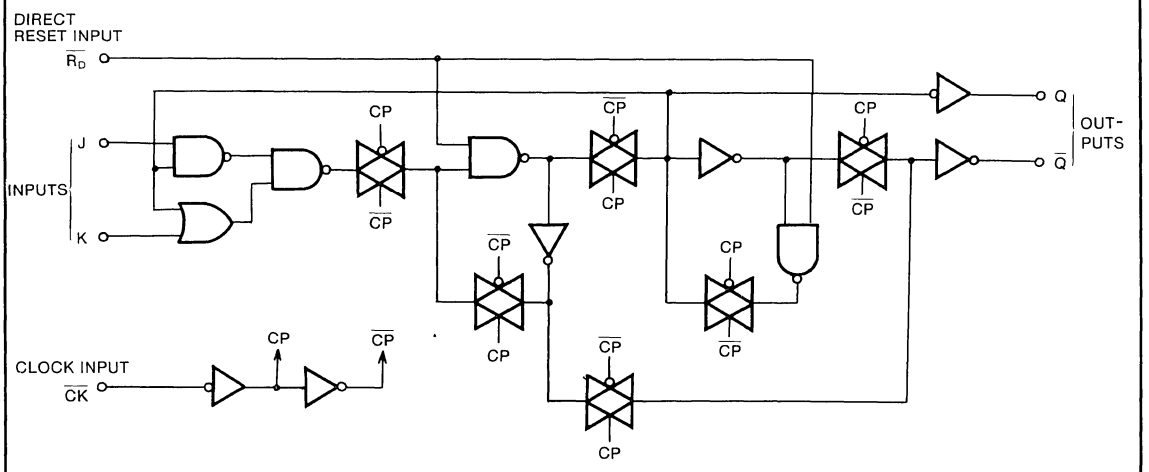
Use of silicon gate technology allows the M74HC107 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS107.

The M74HC107 contains two edge-triggered J-K flip flops, each circuit with independent clock input $\overline{CK}$, direct reset input $\overline{R_D}$, and both inputs J and K.

When $\overline{CK}$ changes from high-level to low-level, the signals just previously input at J and K appear at output Q and $\overline{Q}$ in accordance with the function table given. When $\overline{R_D}$ is low, Q and $\overline{Q}$ will become low and high respectively, irrespective of other inputs. When used as a J-K flip flop, $\overline{R_D}$ should be maintained at high-level.

M74HC107 is the same functions and electrical characteristics as M74HC73P, differing only pin connections.

LOGIC DIAGRAM (EACH FLIP FLOP)



FUNCTION TABLE (Note 1)

Inputs				Outputs	
$\overline{R_D}$	CK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q^0	$\overline{Q}^0$
H	↓	L	H	L	H
H	↓	H	L	H	L
H	↓	H	H	Toggle	
H	L	X	X	Q^0	$\overline{Q}^0$
H	H	X	X	Q^0	$\overline{Q}^0$
H	↑	X	X	Q^0	$\overline{Q}^0$

Note 1 : ↑ : Change from low to high level
↓ : Change from high to low level
X : Irrelevant
Q^0 : Output state Q before clock input changed
$\overline{Q}^0$: Output state $\overline{Q}$ before clock input changed
Toggle : Inverted state before clock input changed

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation		500	mW
Tstg	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			2.0		20.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 3)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level output transition time				10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$ − Q, $\overline{Q}$)				21	ns
t_{PHL}					21	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{R_D}$ − Q, $\overline{Q}$)				26	ns
t_{PHL}					26	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

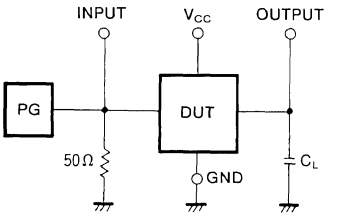
Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40~+85℃		
		V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 3)	2.0	5			4		MHz
			4.5	27			21		
			6.0	31			24		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$ − Q, $\overline{Q}$)		2.0			126		160	ns
			4.5			25		32	
			6.0			21		27	
t_{PHL}			2.0			126		160	
			4.5			25		32	
			6.0			21		27	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{R_D}$ − Q, $\overline{Q}$)		2.0			155		194	ns
			4.5			31		39	
			6.0			26		32	
t_{PHL}			2.0			155		194	
			4.5			31		39	
			6.0			26		32	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)								pF

Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per flip flop)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

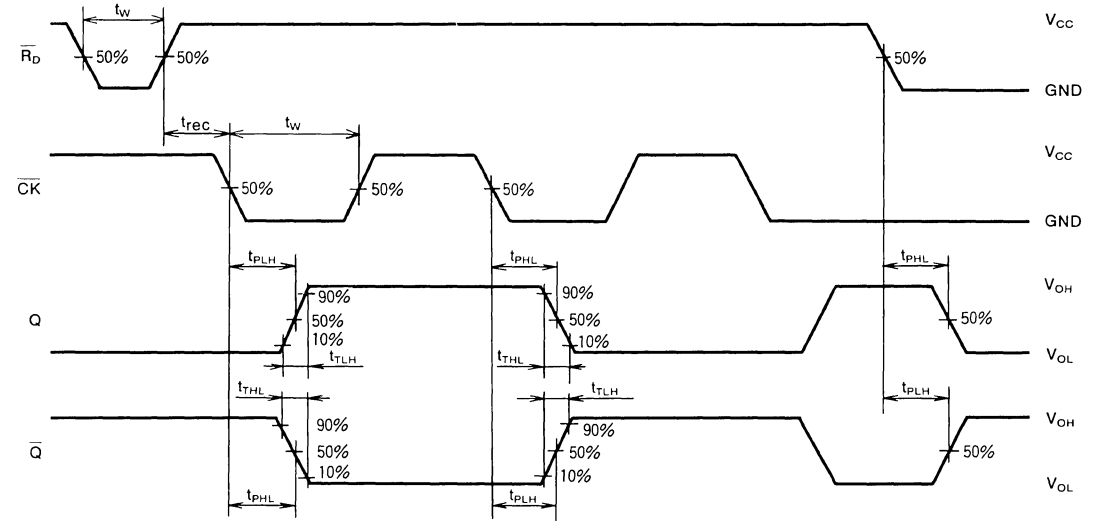
Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40~+85℃		
		V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	$\overline{CK}$, $\overline{R_D}$ pulse width	2.0	80			101		ns
		4.5	16			20		
		6.0	14			17		
t_{su}	J and K setup time with respect to $\overline{CK}$	2.0	100			125		ns
		4.5	20			25		
		6.0	17			21		
t_h	J and K hold time with respect to $\overline{CK}$	2.0	0			0		ns
		4.5	0			0		
		6.0	0			0		
t_{rec}	$\overline{R_D}$ recovery time with respect to $\overline{CK}$	2.0	100			125		ns
		4.5	20			25		
		6.0	17			21		

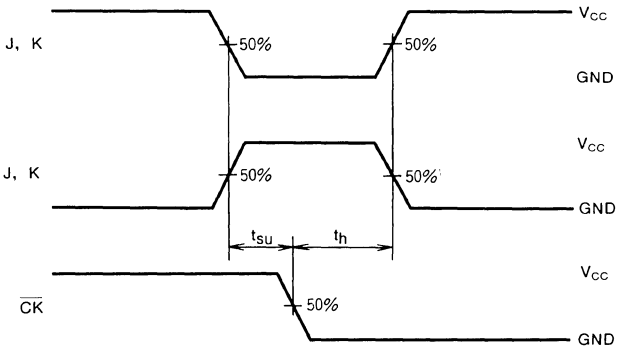
Note 3 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%) $t_r = 6ns$, $t_f = 6ns$
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM





M74HC109P

DUAL J-$\overline{K}$ FLIP-FLOP WITH SET AND RESET

DESCRIPTION

The M74HC109 is a semiconductor integrated circuit consisting of two positive-edge triggered J-$\overline{K}$ flip-flops with independent control inputs.

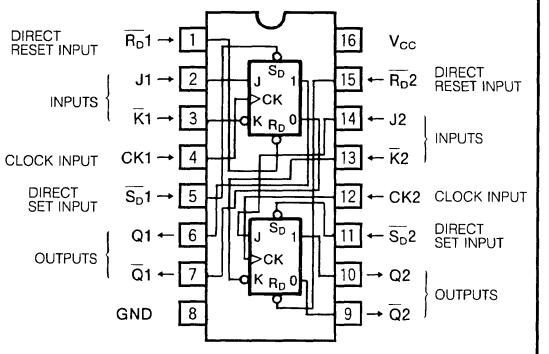
FEATURES

- High-speed: (clock frequency) 50MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 10μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

FUNCTIONAL DESCRIPTION

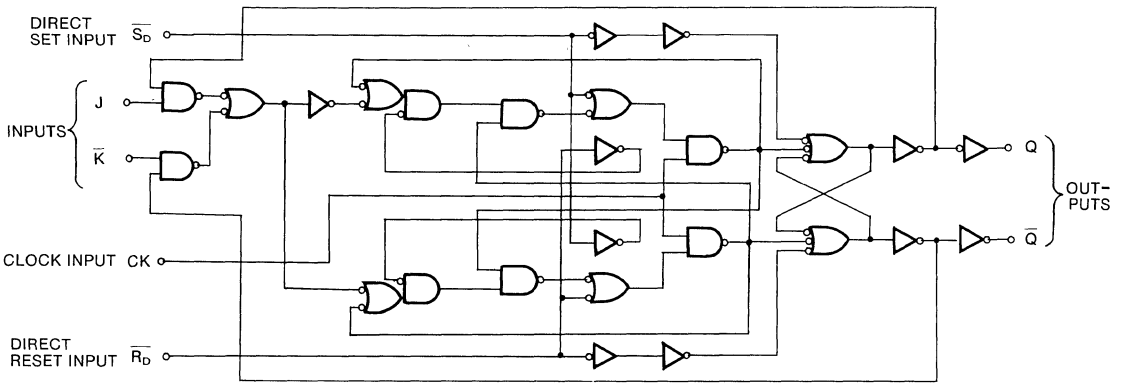
Use of silicon gate technology allows the M74HC109 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS109.

The M74HC109 contains two edge-triggered J-$\overline{K}$ flip flops, each circuit with independent clock input CK, direct set input $\overline{S_D}$, direct reset input $\overline{R_D}$ and both inputs J and $\overline{K}$.

When CK changes from low-level to high-level, the signals just previously input at J and $\overline{K}$ appear at outputs Q and $\overline{Q}$ in accordance with the function table given. Use of $\overline{S_D}$ and $\overline{R_D}$ permits direct R-S flip flop operation. When $\overline{S_D}$ and $\overline{R_D}$ are low, Q and $\overline{Q}$ will both become high but when $\overline{S_D}$ and $\overline{R_D}$ simultaneously become high, the condition of Q and $\overline{Q}$ cannot be predetermined. When used as a J-$\overline{K}$ flip flop, $\overline{S_D}$ and $\overline{R_D}$ should be maintained at high-level.

Connecting J and $\overline{K}$ will permit the M74HC109 to be used as a D-type flip flop.

LOGIC DIAGRAM (EACH FLIP FLOP)



MITSUBISHI ELECTRIC

FUNCTION TABLE (Note 1)

Inputs					Outputs	
$\overline{S_D}$	$\overline{R_D}$	CK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	Toggle	
H	H	↑	L	H	Q^0	$\overline{Q}^0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q^0	$\overline{Q}^0$

Note 1 : ↑ : Change from low to high level
X : Irrelevant
Q^0 : Output state Q before clock input changed
$\overline{Q}^0$: Output state $\overline{Q}$ before clock input changed
Toggle : Inverted state before clock input changed
* : When $\overline{S_D}$ and $\overline{R_D}$ are low, Q and $\overline{Q}$ will both become high but when $\overline{S_D}$ and $\overline{R_D}$ simultaneously become high, the condition of Q and $\overline{Q}$ cannot be predetermined

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation		500	mW
Tstg	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			2.0		20.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 3)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level output transition time				10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$ − Q, $\overline{Q}$)				30	ns
t_{PHL}					30	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{S_D}$, $\overline{R_D}$ − Q, $\overline{Q}$)				40	ns
t_{PHL}					40	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

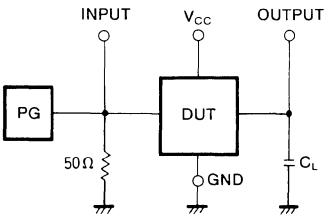
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 3)	2.0	5			4		MHz
			4.5	27			21		
			6.0	31			24		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q, $\overline{Q}$)		2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PHL}			2.0			175		221	
			4.5			35		44	
			6.0			30		37	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{S_D}$, $\overline{R_D}$ − Q, $\overline{Q}$)		2.0			230		290	ns
			4.5			46		58	
			6.0			39		49	
t_{PHL}			2.0			230		290	
			4.5			46		58	
			6.0			39		49	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				45				pF

Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per flip flop)
The power dissipated during operation under no-load conditions is calculated using the following formula
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

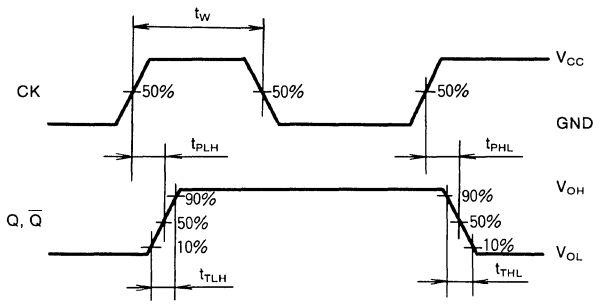
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	CK, $\overline{S_D}$, $\overline{R_D}$ pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
t_{su}	J, $\overline{K}$ setup time with respect to $\overline{CK}$		2.0	100			126		ns
			4.5	20			25		
			6.0	17			21		
t_h	J, $\overline{K}$ hold time with respect to $\overline{CK}$		2.0	5			5		ns
			4.5	5			5		
			6.0	5			5		
t_{rec}	$\overline{S_D}$, $\overline{R_D}$ recovery time with respect to $\overline{CK}$		2.0	5			5		ns
			4.5	5			5		
			6.0	5			5		

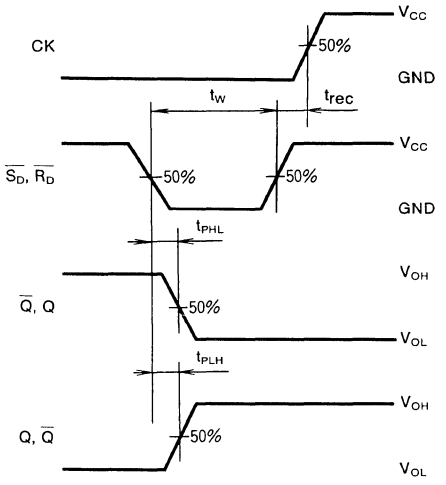
Note 3 : Test Circuit

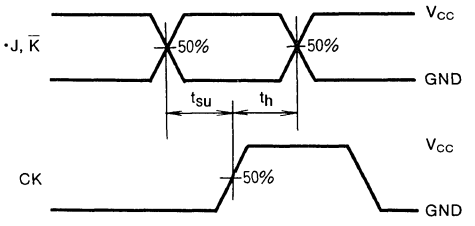


(1) The pulse generator (PG) has the following characteristics (10%~90%) t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM







MITSUBISHI ELECTRIC

M74HC112P

DUAL J-K FLIP-FLOP WITH SET AND RESET

DESCRIPTION

The M74HC112 is a semiconductor integrated circuit consisting of two negative-edge triggered J-K flip flops with independent control inputs.

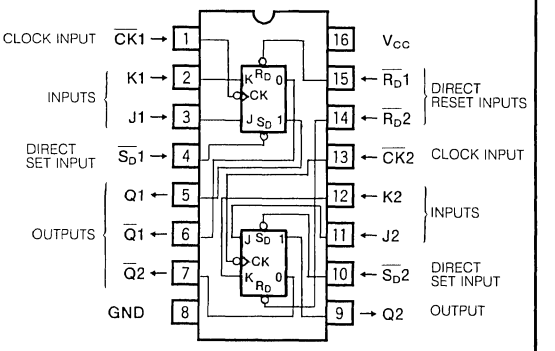
FEATURES

- High-speed: (clock frequency) 50MHz typ (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 10μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

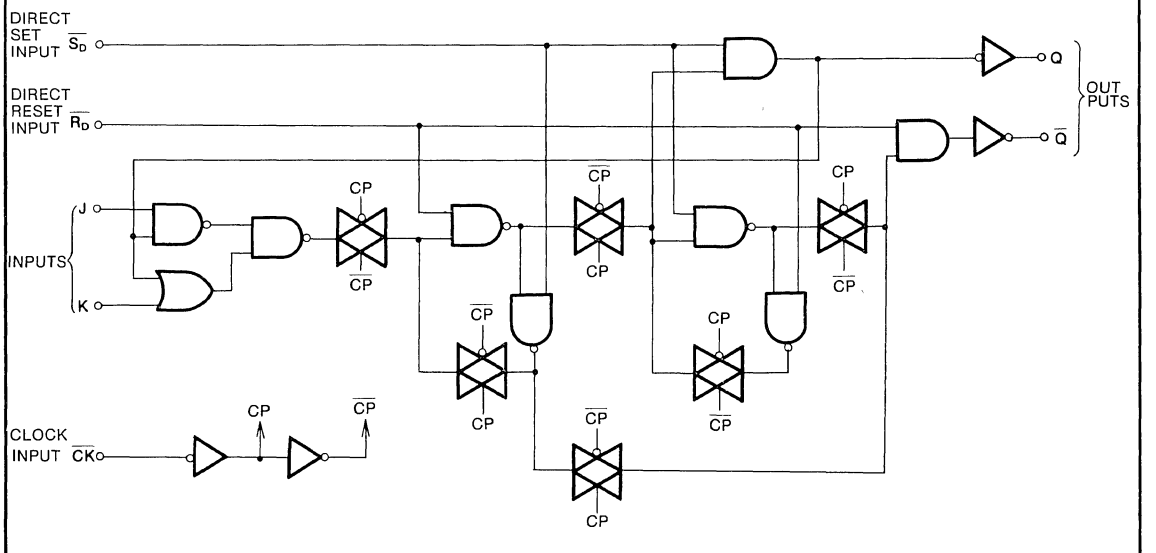
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC112 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS112.

The M74HC112 contains two edge-triggered J-K flip flops, each circuit with independent clock input $\overline{CK}$, direct set input $\overline{S_D}$ and direct reset input $\overline{R_D}$, and both inputs J and K.

When $\overline{CK}$ is high-level, the J and K signals can be read. When $\overline{CK}$ changes from high-level to low-level, the signals just previously input at J and K appear at outputs Q and $\overline{Q}$ in accordance with the function table given. Use of $\overline{S_D}$ and $\overline{R_D}$ permits direct R-S flip flop operation. When $\overline{S_D}$ and $\overline{R_D}$ are low, Q and $\overline{Q}$ will both become high but when $\overline{S_D}$ and $\overline{R_D}$ simultaneously become high, the condition of Q and $\overline{Q}$ cannot be predetermined. When used as a J-K flip flop, $\overline{S_D}$ and $\overline{R_D}$ should be maintained at high-level.

LOGIC DIAGRAM (EACH FLIP FLOP)



FUNCTION TABLE (Note 1)

Inputs					Outputs	
$\overline{S_D}$	$\overline{R_D}$	$\overline{CK}$	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q^0	$\overline{Q}^0$
H	H	↓	L	H	L	H
H	H	↓	H	L	H	L
H	H	↓	H	H	Toggle	
H	H	L	X	X	Q^0	$\overline{Q}^0$
H	H	H	X	X	Q^0	$\overline{Q}^0$
H	H	↑	X	X	Q^0	$\overline{Q}^0$

Note 1 : ↑ : Change from low to high level
↓ : Change from high to low level
X : Irrelevant
Q^0 : Output state Q before clock input changed
$\overline{Q}^0$: Output state $\overline{Q}$ before clock input changed
Toggle : Inverted state before clock input changed
* : When $\overline{S_D}$ and $\overline{R_D}$ are low, Q and $\overline{Q}$ will both become high but when $\overline{S_D}$ and $\overline{R_D}$ simultaneously become high the condition of Q and $\overline{Q}$ cannot be predetermined

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
Pd	Power dissipation		500	mW
Tstg	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			2.0		20.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 3)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level				10	ns
t_{THL}	output transition time				10	
t_{PLH}	Low-level to high-level and high-level to low-level				26	ns
t_{PHL}	output propagation time ($\overline{CK}$ − Q, $\overline{Q}$)				26	
t_{PLH}	Low-level to high-level and high-level to low-level				31	ns
t_{PHL}	output propagation time ($\overline{R_D}$ − Q, $\overline{Q}$)				31	
t_{PLH}	Low-level to high-level and high-level to low-level				31	ns
t_{PHL}	output propagation time ($\overline{S_D}$ − Q, $\overline{Q}$)				31	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

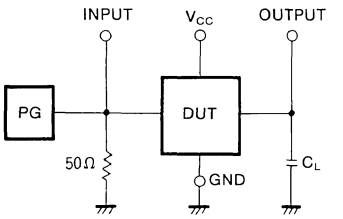
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 3)	2.0	5			4		MHz
			4.5	27			21		
			6.0	31			24		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$ − Q, $\overline{Q}$)		2.0			150		190	ns
			4.5			30		38	
			6.0			26		33	
t_{PHL}			2.0			150		190	
			4.5			30		38	
			6.0			26		33	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{R_D}$ − Q, $\overline{Q}$)		2.0			180		225	ns
			4.5			36		45	
			6.0			31		38	
t_{PHL}			2.0			180		225	
			4.5			36		45	
			6.0			31		38	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{S_D}$ − Q, $\overline{Q}$)		2.0			180		225	ns
			4.5			36		45	
			6.0			31		38	
t_{PHL}			2.0			180		225	
			4.5			36		45	
			6.0			31		38	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				75				pF

Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per flip flop)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

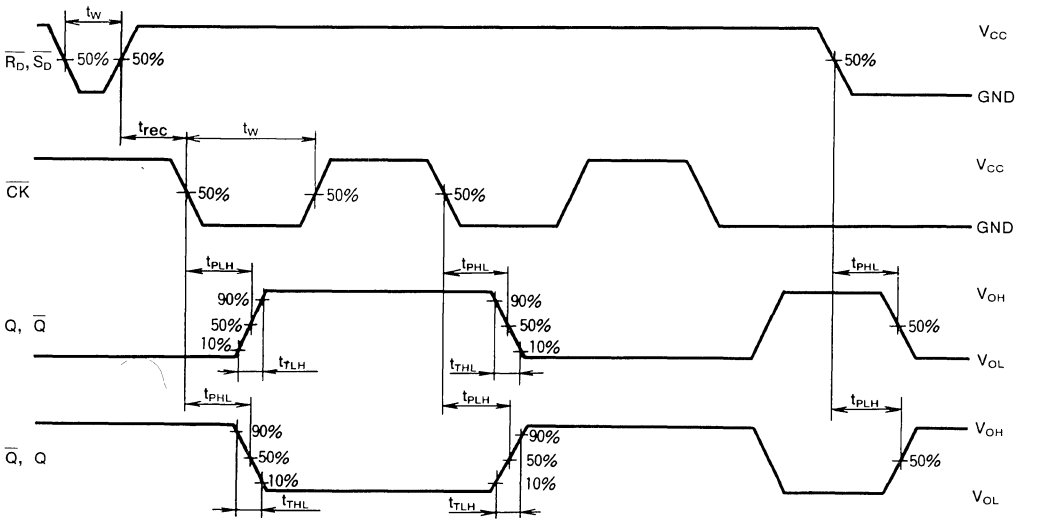
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	$\overline{CK}$, $\overline{S_D}$, $\overline{R_D}$ pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
t_{su}	J, K setup time with respect to $\overline{CK}$		2.0	100			125		ns
			4.5	20			25		
			6.0	17			21		
t_h	J, K hold time with respect to $\overline{CK}$		2.0	0			0		ns
			4.5	0			0		
			6.0	0			0		
t_{rec}	$\overline{R_D}$, $\overline{S_D}$ recovery time with respect to $\overline{CK}$		2.0	100			125		ns
			4.5	20			25		
			6.0	17			21		

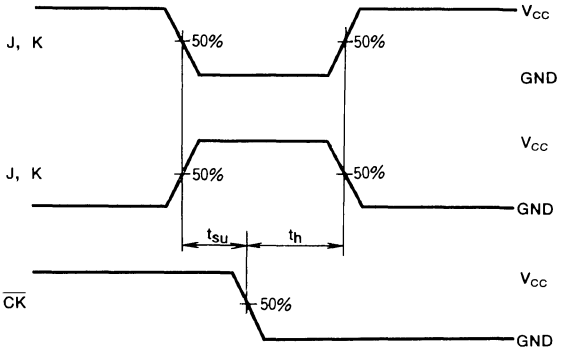
Note 3 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%) t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM





PRELIMINARY
Notice This is not a final specification Some parametric limits are Subject to change

MITSUBISHI HIGH SPEED CMOS

M74HC113P

DUAL J-K FLIP-FLOP WITH SET

DESCRIPTION

The M74HC113 is a semiconductor integrated circuit consisting of two negative-edge triggered J-K flip flops with independent control inputs.

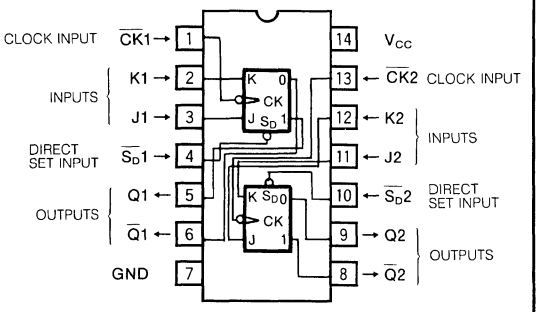
FEATURES

- High-speed: (clock frequency) 50MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 10μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

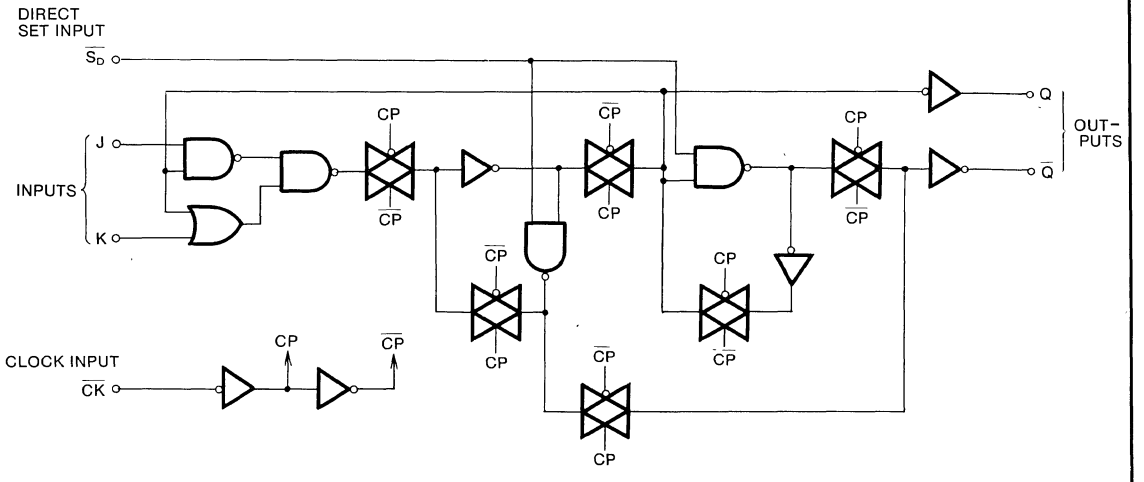
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC113 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS113.

The M74HC113 contains two edge-triggered J-K flip flops, each circuit with independent clock input $\overline{CK}$, direct set input $\overline{S_D}$, and both inputs J and K.

When $\overline{CK}$ changes from high-level to low-level, the signals just previously input at J and K appear at outputs Q and $\overline{Q}$ in accordance with the function table given. When $\overline{S_D}$ is high, Q and $\overline{Q}$ will become high and low respectively, irrespective of other inputs. When used as a J-K flip flop, $\overline{S_D}$ should be maintained at high-level.

LOGIC DIAGRAM (EACH FLIP FLOP)



MITSUBISHI ELECTRIC

FUNCTION TABLE (Note 1)

Inputs				Outputs	
$\overline{S_D}$	$\overline{CK}$	J	K	Q	$\overline{Q}$
L	X	X	X	H	L
H	↓	L	L	Q^0	$\overline{Q}^0$
H	↓	L	H	L	H
H	↓	H	L	H	L
H	↓	H	H	Toggle	
H	L	X	X	Q^0	$\overline{Q}^0$
H	H	X	X	Q^0	$\overline{Q}^0$
H	↑	X	X	Q^0	$\overline{Q}^0$

Note 1 : ↑ : Change from low to high level
↓ : Change from high to low level
X : Irrelevant
Q^0 : Output state Q before clock input changed
$\overline{Q}^0$: Output state $\overline{Q}$ before clock input changed
Toggle : Inverted state before clock input changed

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation		500	mW
Tstg	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			2.0		20.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 3)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level				10	ns
t_{THL}	output transition time				10	
t_{PLH}	Low-level to high-level and high-level to low-level				21	ns
t_{PHL}	output propagation time ($\overline{CK}$ − Q, $\overline{Q}$)				21	
t_{PLH}	Low-level to high-level and high-level to low-level				26	ns
t_{PHL}	output propagation time ($\overline{S_D}$ − Q, $\overline{Q}$)				26	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

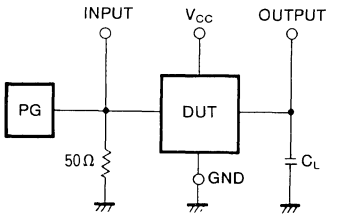
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 3)	2.0	5			4		MHz
			4.5	27			21		
			6.0	31			24		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$ − Q, $\overline{Q}$)		2.0			126		160	ns
			4.5			25		32	
			6.0			21		27	
t_{PHL}			2.0			126		160	
			4.5			25		32	
			6.0			21		27	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{S_D}$ − Q, $\overline{Q}$)		2.0			165		210	ns
			4.5			33		41	
			6.0			28		35	
t_{PHL}			2.0			165		210	
			4.5			33		41	
			6.0			28		35	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)								pF

Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per flip flop)
The power dissipated during operation under no-load conditions is calculated using the following formula
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

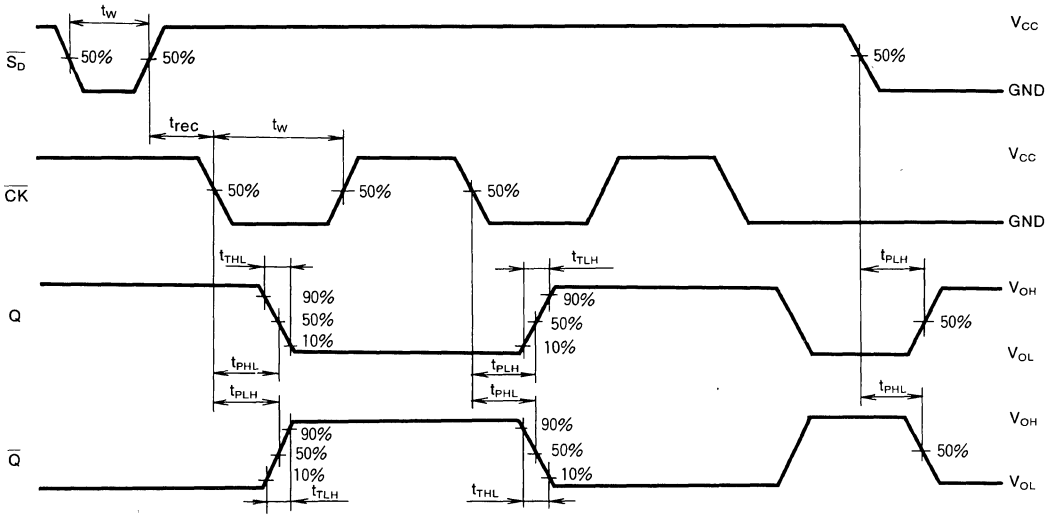
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	$\overline{CK}$, $\overline{S_D}$ pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
t_{su}	J, K setup time with respect to $\overline{CK}$		2.0	100			125		ns
			4.5	20			25		
			6.0	17			21		
t_h	J, K hold time with respect to $\overline{CK}$		2.0	0			0		ns
			4.5	0			0		
			6.0	0			0		
t_{rec}	$\overline{S_D}$ recovery time with respect to $\overline{CK}$		2.0	100			125		ns
			4.5	20			25		
			6.0	17			21		

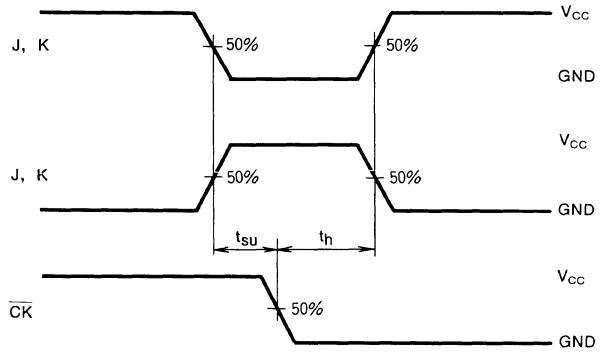
Note 3 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%) t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM





MITSUBISHI ELECTRIC

M74HC114P

DUAL J-K FLIP-FLOP WITH SET AND COMMON RESET

DESCRIPTION

The M74HC114 is a semiconductor integrated circuit consisting of two negative-edge triggered J-K flip flops with independent control inputs.

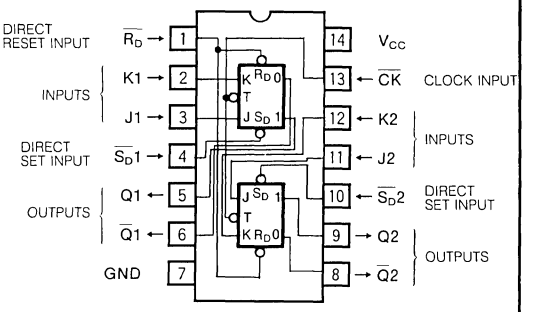
FEATURES

- High-speed (clock frequency) 50MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation 10μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment

PIN CONFIGURATION (TOP VIEW)



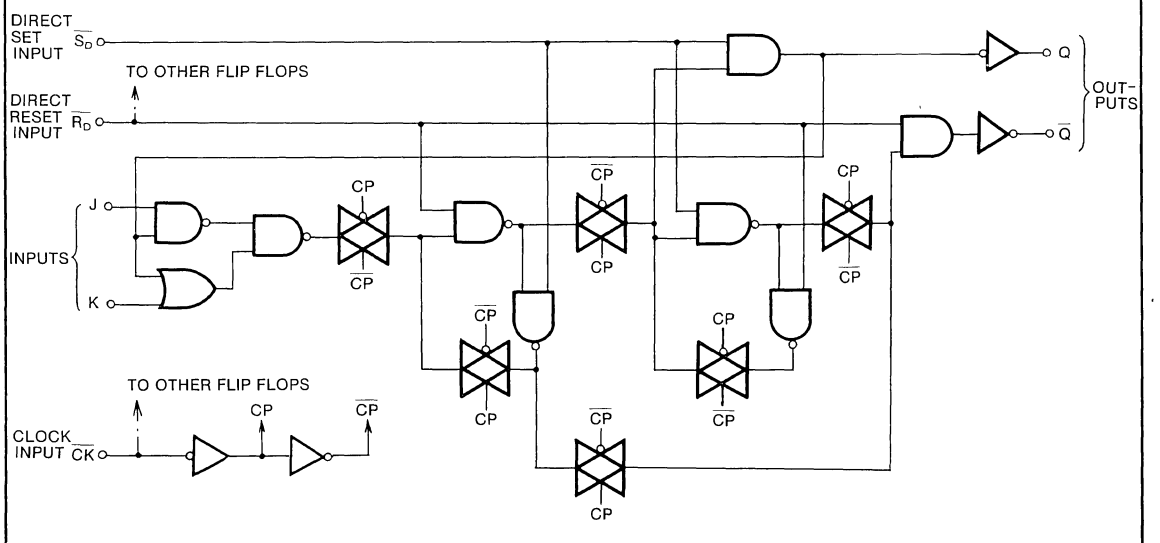
Outline 14P4

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC114 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS114.

The M74HC114 contains two edge-triggered J-K flip flops, each circuit with independent direct set input $\overline{S_D}$, inputs J and K, common clock input $\overline{CK}$, and direct reset input $\overline{R_D}$. When $\overline{CK}$ is high, the J and K signals can be read. When $\overline{CK}$ changes from high-level to low-level, the signals just previously input at J and K appear at outputs Q and $\overline{Q}$ in accordance with the function table given Use of $\overline{S_D}$ and $\overline{R_D}$ permits direct R-S flip flop operation. When $\overline{S_D}$ and $\overline{R_D}$ are low, Q and $\overline{Q}$ will both become high but when $\overline{S_D}$ and $\overline{R_D}$ simultaneously become high the condition of Q and $\overline{Q}$ cannot be predetermined. When used as a J-K flip flop, $\overline{S_D}$ and $\overline{R_D}$ should be maintained at high.

LOGIC DIAGRAM (EACH FLIP FLOP)



FUNCTION TABLE (Note 1)

Inputs					Outputs	
$\overline{S_D}$	$\overline{R_D}$	$\overline{CK}$	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q^0	$\overline{Q}^0$
H	H	↓	L	H	L	H
H	H	↓	H	L	H	L
H	H	↓	H	H	Toggle	
H	H	L	X	X	Q^0	$\overline{Q}^0$
H	H	H	X	X	Q^0	$\overline{Q}^0$
H	H	↑	X	X	Q^0	$\overline{Q}^0$

Note 1 : ↑ : Change from low to high level
↓ : Change from high to low level
X : Irrelevant
Q^0 : Output state Q before clock input changed
$\overline{Q}^0$: Output state $\overline{Q}$ before clock input changed
Toggle : Inverted state before clock input changed
* : When $\overline{S_D}$ and $\overline{R_D}$ are low, Q and $\overline{Q}$ will both become high but when $\overline{S_D}$ and $\overline{R_D}$ simultaneously become high, the condition of Q and $\overline{Q}$ cannot be predetermined.

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
Pd	Power dissipation		500	mW
Tstg	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0		0.1		0.1	V
			I_{OL} = 20μA	4.5		0.1		0.1	
			I_{OL} = 20μA	6.0		0.1		0.1	
			I_{OL} = 4.0mA	4.5		0.26		0.33	
			I_{OL} = 5.2mA	6.0		0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			2.0		20.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 3)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level				10	ns
t_{THL}	output transition time				10	
t_{PLH}	Low-level to high-level and high-level to low-level				26	ns
t_{PHL}	output propagation time ($\overline{CK}$ − Q, $\overline{Q}$)				26	
t_{PLH}	Low-level to high-level and high-level to low-level				31	ns
t_{PHL}	output propagation time ($\overline{R_D}$ − Q, $\overline{Q}$)				31	
t_{PLH}	Low-level to high-level and high-level to low-level				31	ns
t_{PHL}	output propagation time ($\overline{S_D}$ − Q, $\overline{Q}$)				31	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

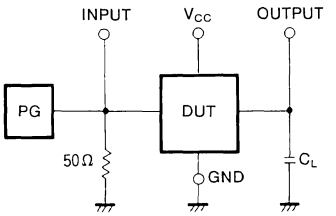
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 3)	2.0	5			4		MHz
			4.5	27			21		
			6.0	31			24		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$ − Q, $\overline{Q}$)		2.0			150		190	ns
			4.5			30		38	
			6.0			26		33	
t_{PHL}			2.0			150		190	
			4.5			30		38	
			6.0			26		33	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{R_D}$ − Q, $\overline{Q}$)		2.0			180		225	ns
			4.5			36		45	
			6.0			31		38	
t_{PHL}			2.0			180		225	
			4.5			36		45	
			6.0			31		38	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{S_D}$ − Q, $\overline{Q}$)		2.0			180		225	ns
			4.5			36		45	
			6.0			31		38	
t_{PHL}			2.0			180		225	
			4.5			36		45	
			6.0			31		38	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)								pF

Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per flip flop)
The power dissipated during operation under no-load conditions is calculated using the following formula.
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

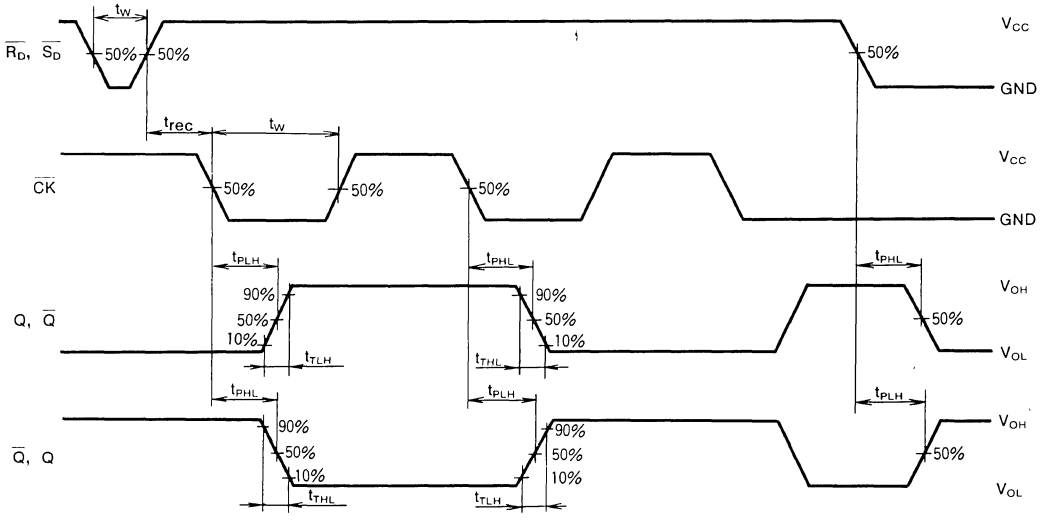
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	$\overline{CK}$, $\overline{S_D}$, $\overline{R_D}$ pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
t_{su}	J, K setup time with respect to $\overline{CK}$		2.0	100			125		ns
			4.5	20			25		
			6.0	17			21		
t_h	J, K hold time with respect to $\overline{CK}$		2.0	0			0		ns
			4.5	0			0		
			6.0	0			0		
t_{rec}	$\overline{R_D}$, $\overline{S_D}$ recovery time with respect to $\overline{CK}$		2.0	100			125		ns
			4.5	20			25		
			6.0	17			21		

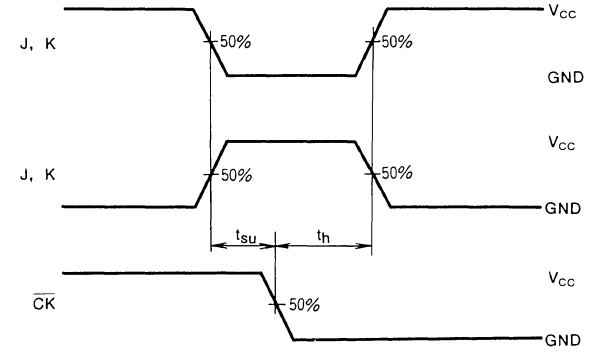
Note 3 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%) t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM





M74HC137P

1-OF-8 DECODER/DEMULTIPLEXER WITH ADDRESS LATCH

DESCRIPTION

The M74HC137 is a semiconductor integrated circuit consisting of a 3-bit binary to 8-line decoder/demultiplexer with address latch provided.

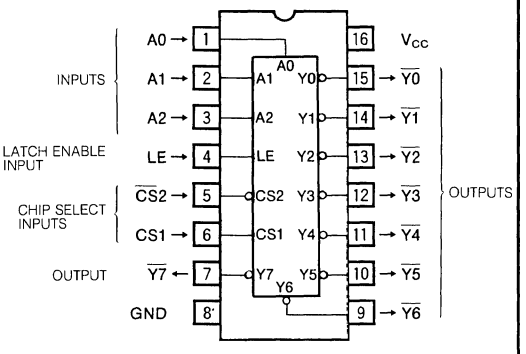
FEATURES

- Built-in address latch
- High-speed: 17ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

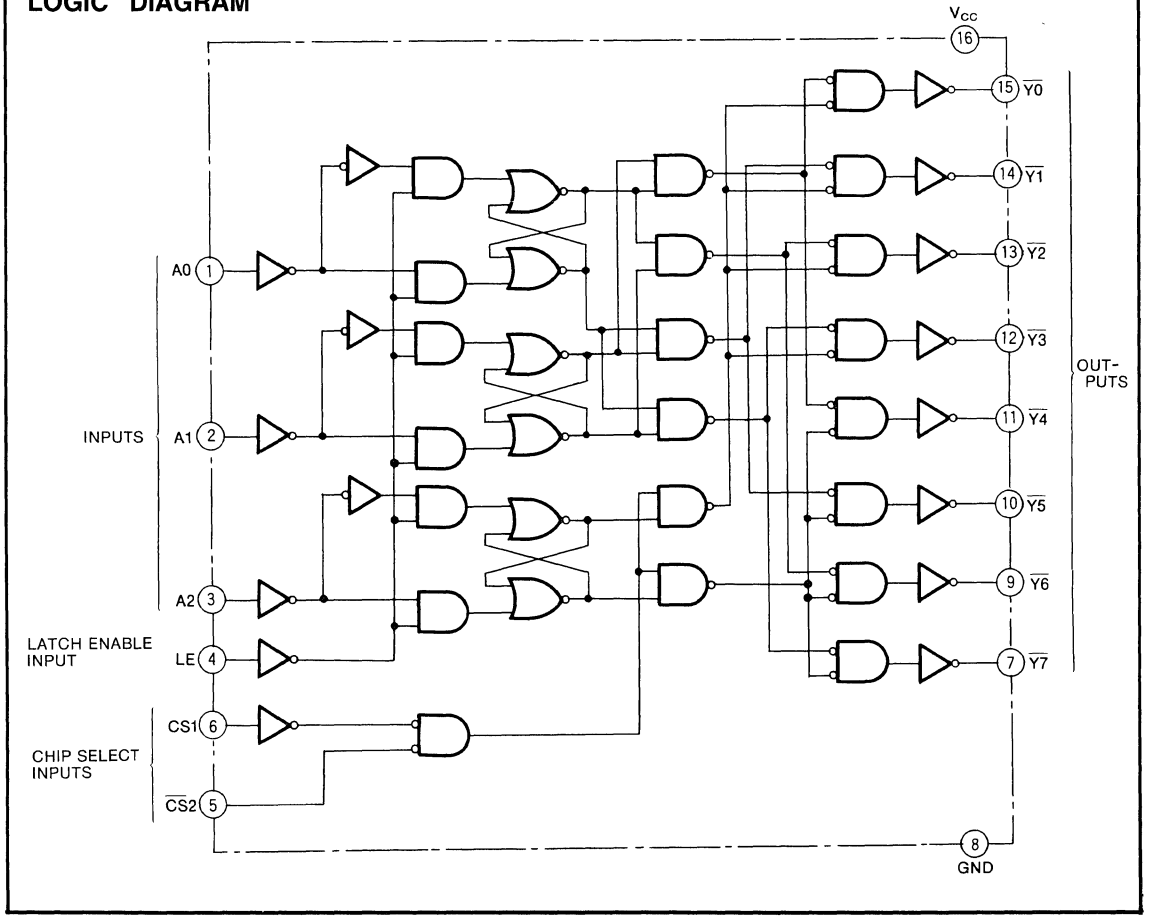
General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

LOGIC DIAGRAM



MITSUBISHI ELECTRIC

1-OF-8 DECODER/DEMULTIPLEXER WITH ADDRESS LATCH

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC137 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while providing high-speed performance equivalent to the 74LS137.

The M74HC137 consists of a 3-bit binary to 8-line decoder/demultiplexer with an address latch to store the signals of inputs A0 through A2. When latch-enable input LE is low, a 3-bit binaly code is applied to inputs A0 through A2 goes through the latch and becomes a code input signal. In this case, one of outputs $\overline{Y0}$ through $\overline{Y7}$ corresponding to this value will become low and the other outputs will all become high. In this case, chip select inputs CS1 and $\overline{CS2}$ should be maintained at high and low, respectively. When CS1 and $\overline{CS2}$ are in conditions other than those given above, all outputs will become high.

When LE is high, the A0 through A2 signals existing immediately prior to the high-level setting will be stored in the latch. In this case, those stored contents will not change even if A0 through A2 are changed.

When operated as a 1-of-8 demultiplexer, CS1 or $\overline{CS2}$ is used as a data input and A0 through A2 are used as selecting inputs.

FUNCTION TABLE (Note 1)

Inputs						Outputs							
LE	CS1	$\overline{CS2}$	A2	A1	A0	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	$\overline{Y0}^0$	$\overline{Y1}^0$	$\overline{Y2}^0$	$\overline{Y3}^0$	$\overline{Y4}^0$	$\overline{Y5}^0$	$\overline{Y6}^0$	$\overline{Y7}^0$

Note 1 : X : Irrelevant
$\overline{Y}^0$: Output state $\overline{Y}$ before LE chaged to high level

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
Pd	Power dissipation		500	mW
Tstg	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level	C_L = 15pF (Note 3)			10	ns
t_{THL}	output transition time				10	
t_{PLH}	Low-level to high-level and high-level to low-level				29	ns
t_{PHL}	output propagation time (A − $\overline{Y}$)				42	
t_{PLH}	Low-level to high-level and high-level to low-level				22	ns
t_{PHL}	output propagation time ($\overline{CS2}$ − $\overline{Y}$)				34	
t_{PLH}	Low-level to high-level and high-level to low-level				25	ns
t_{PHL}	output propagation time (CS1 − $\overline{Y}$)				34	
t_{PLH}	Low-level to high-level and high-level to low-level				30	ns
t_{PHL}	output propagation time (LE − $\overline{Y}$)				44	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

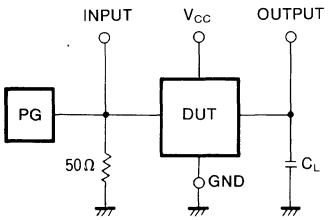
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − $\overline{Y}$)		2.0			170		214	ns
			4.5			34		43	
			6.0			29		36	
t_{PHL}			2.0			240		302	
			4.5			48		60	
			6.0			41		51	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CS2}$ − $\overline{Y}$)		2.0			130		164	ns
			4.5			26		33	
			6.0			22		28	
t_{PHL}			2.0			195		246	
			4.5			39		49	
			6.0			33		42	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CS1 − $\overline{Y}$)		2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHL}			2.0			195		246	
			4.5			39		49	
			6.0			33		42	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (LE − $\overline{Y}$)		2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PHL}			2.0			250		315	
			4.5			50		63	
			6.0			43		54	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				108				pF

Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

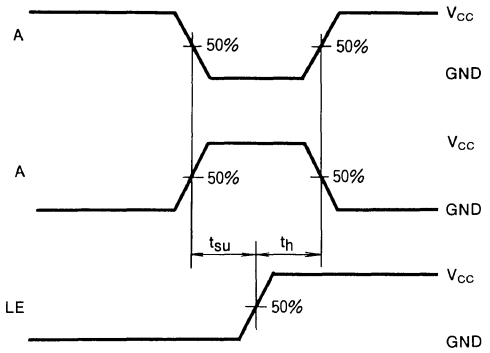
TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_W	LE pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
t_{SU}	A setup time with respect to LE		2.0	100			126		ns
			4.5	20			25		
			6.0	17			21		
t_h	A hold time with respect to LE		2.0	50			63		ns
			4.5	10			13		
			6.0	9			11		

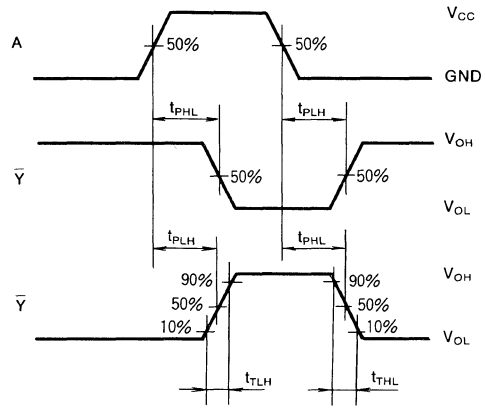
Note 3 : Test Circuit

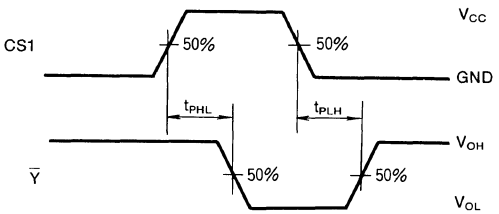


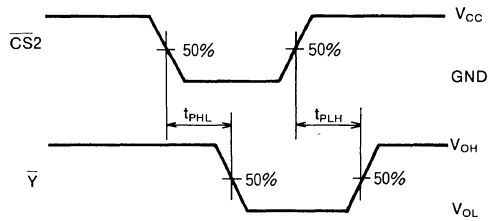
(1) The pulse generator (PG) has the following characteristics (10%~90%) $t_r = 6ns$, $t_f = 6ns$
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

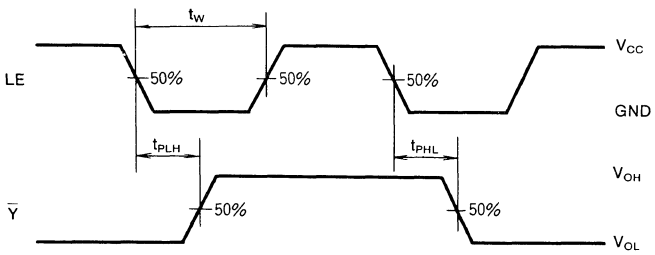


TIMING DIAGRAM









M74HC138P
M74HC138DP

1-OF-8 DECODER/DEMULTIPLEXER

DESCRIPTION

The M74HC138 is a semiconductor integrated circuit consisting of a 3-bit binary to 8-line decoder/demultiplexer with chip-select inputs.

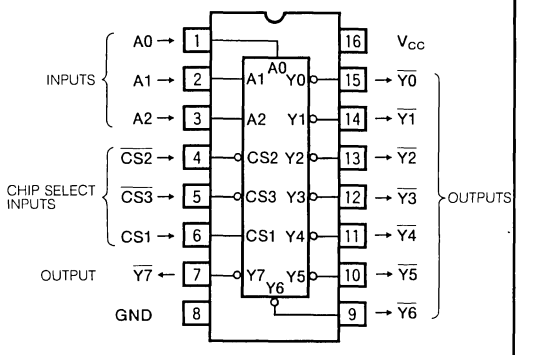
FEATURES

- Selection of three types of chip inputs
- Expansion up to 24 outputs possible with externally connection.
- High-speed: 17ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4
16P2P

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC138 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS138.

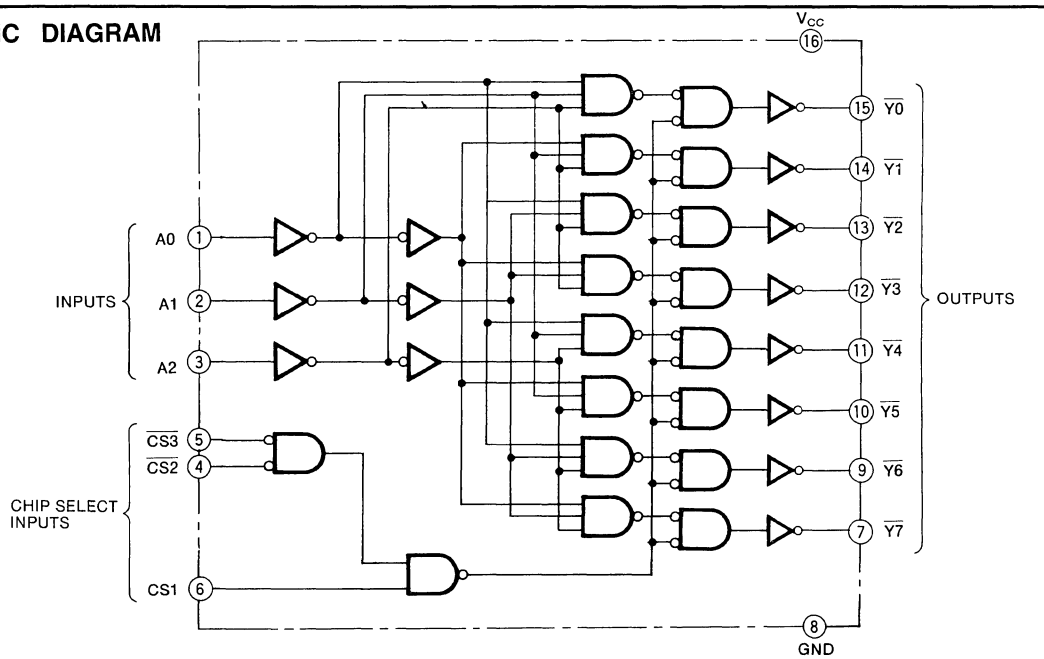
When operated as a decoder, a 3-bit binary code are applied to inputs A0, A1 and A2, one of outputs $\overline{Y0}$ through $\overline{Y7}$ corresponding to this value will become low and the other outputs will all become high.

In this case, chip select input CS1 should be maintained at high while $\overline{CS2}$ and $\overline{CS3}$ should be maintained at low.

When CS1, $\overline{CS2}$ and $\overline{CS3}$ are in conditions other than those given above, all outputs will become high irrespective of A0 through A2.

When operated as a 1-of-8 demultiplexer, CS1, $\overline{CS2}$ or $\overline{CS3}$ is used as data input and A0 through A2 input are used as slecting input.

LOGIC DIAGRAM



FUNCTION TABLE (Note 1)

Inputs					Outputs							
CS1	$\overline{CSX}$	A2	A1	A0	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

Note 1 : $\overline{CSX} = \overline{CS2} + \overline{CS3}$
X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC138DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0		0.1		0.1	V
			I_{OL} = 20μA	4.5		0.1		0.1	
			I_{OL} = 20μA	6.0		0.1		0.1	
			I_{OL} = 4.0mA	4.5		0.26		0.33	
			I_{OL} = 5.2mA	6.0		0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

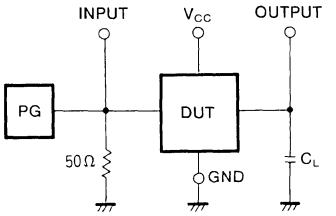
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level	C_L = 15pF (Note 4)			10	ns
t_{THL}	output transition time				10	
t_{PLH}	Low-level to high-level and high-level to low-level				25	ns
t_{PHL}	output propagation time (A − $\overline{Y}$)				35	
t_{PLH}	Low-level to high-level and high-level to low-level				25	ns
t_{PHL}	output propagation time (CS1 − $\overline{Y}$)				25	
t_{PLH}	Low-level to high-level and high-level to low-level				25	ns
t_{PHL}	output propagation time ($\overline{CS2}$, $\overline{CS3}$ − $\overline{Y}$)				30	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − $\overline{Y}$)		2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHL}			2.0			200		252	
			4.5			40		50	
			6.0			34		43	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CS1 − $\overline{Y}$)		2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHL}			2.0			150		189	
			4.5			30		38	
			6.0			26		32	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CS2}$, $\overline{CS3}$ − $\overline{Y}$)		2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHL}			2.0			175		221	
			4.5			35		44	
			6.0			30		37	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)				82				pF

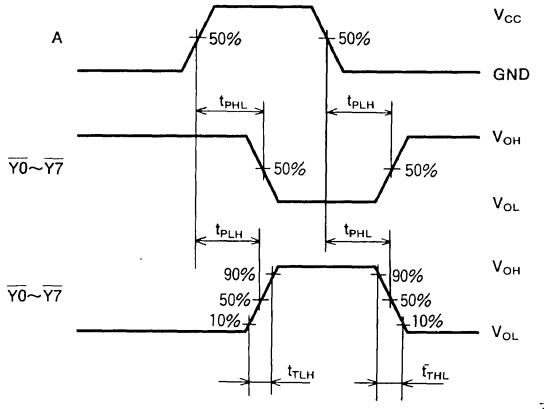
Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

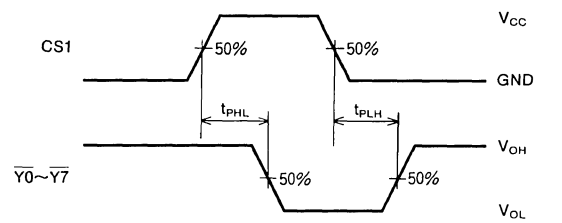
Note 4 : Test Circuit

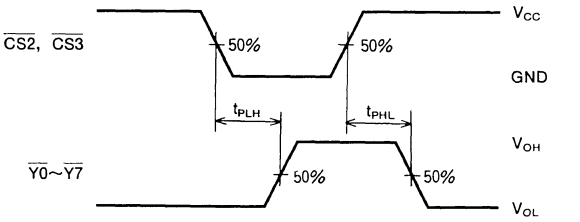


(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM







M74HC139P
M74HC139DP

DUAL 1-OF-4 DECODER/DEMULTIPLEXER

DESCRIPTION

The M74HC139 is a semiconductor integrated circuit consisting of a 2-bit binary to divide-by-4 decoder/demultiplexer circuits with chip select inputs.

FEATURES

- Chip select inputs
- High-speed: 19ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

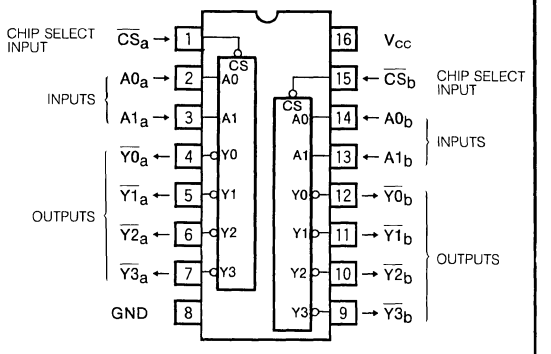
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC139 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS139.

When operated as a decoder, a 2-bit binary code are applied to inputs A0 and A1, one of outputs $\overline{Y0}$ through $\overline{Y3}$ corresponding to this value will become low and the other outputs will all become high. In this case, chip select input $\overline{CS}$ should be maintained at low. When $\overline{CS}$ is high, all outputs will become high irrespective of A0 and A1.

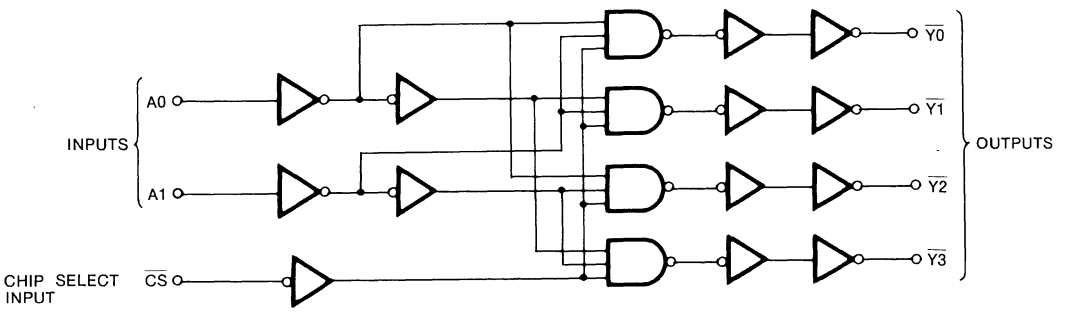
PIN CONFIGURATION (TOP VIEW)



Outline 16P4
16P2P

When operated as a 1-of-4 demultiplexer, $\overline{CS}$ is used as a data input and A0 and A1 are used as slecting inputs.

LOGIC DIAGRAM (EACH DECODER/DEMULTIPLEXER)



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FUNCTION TABLE (Note 1)

Inputs			Outputs			
$\overline{CS}$	A1	A0	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L
H	X	X	H	H	H	H

Note 1 : X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC139DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
					25℃			−40∼+85℃	
				V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

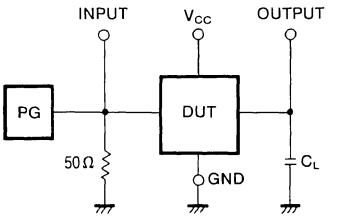
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 4)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CS}$ − $\overline{Y}$)				30	ns
t_{PHL}					30	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − $\overline{Y}$)	Number of delay gate stages 4			30	ns
t_{PHL}					30	
t_{PLH}		Number of delay gate stages 5			38	ns
t_{PHL}					38	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CS}$ − $\overline{Y}$)		2.0			175		219	ns
			4.5			35		44	
			6.0			30		38	
t_{PHL}			2.0			175		219	
			4.5			35		44	
			6.0			30		38	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − $\overline{Y}$)	Number of delay gate stages 4	2.0			175		219	ns
			4.5			35		44	
			6.0			30		38	
t_{PHL}			2.0			175		219	
			4.5			35		44	
			6.0			30		38	
t_{PLH}		Number of delay gate stages 5	2.0			220		275	ns
			4.5			44		55	
			6.0			38		47	
t_{PHL}			2.0			220		275	
			4.5			44		55	
			6.0			38		47	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)				62				pF

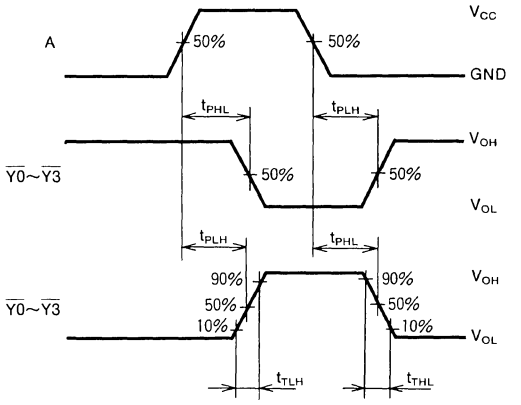
Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per decoder)
The power dissipated during operation under no-load conditions is calculated using the following formula
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

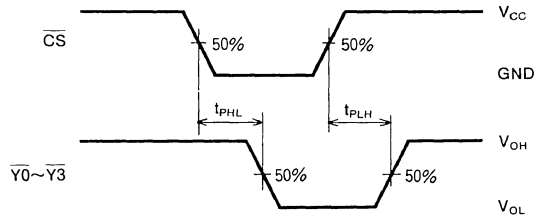
Note 4 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM





M74HC151P

8-INPUT DATA SELECTOR/MULTIPLEXER

DESCRIPTION

The M74HC151 is a semiconductor integrated circuit consisting of an 8-line to 1-line data selector/multiplexer.

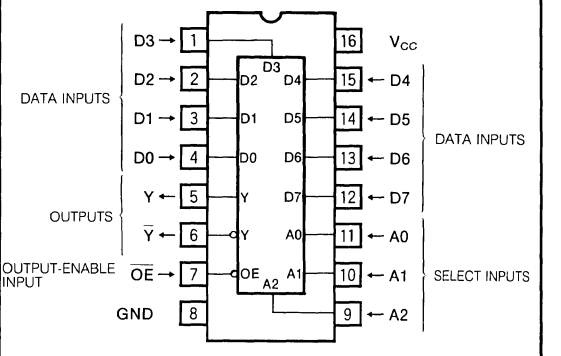
FEATURES

- High-speed: 22ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

FUNCTIONAL DESCRIPTION

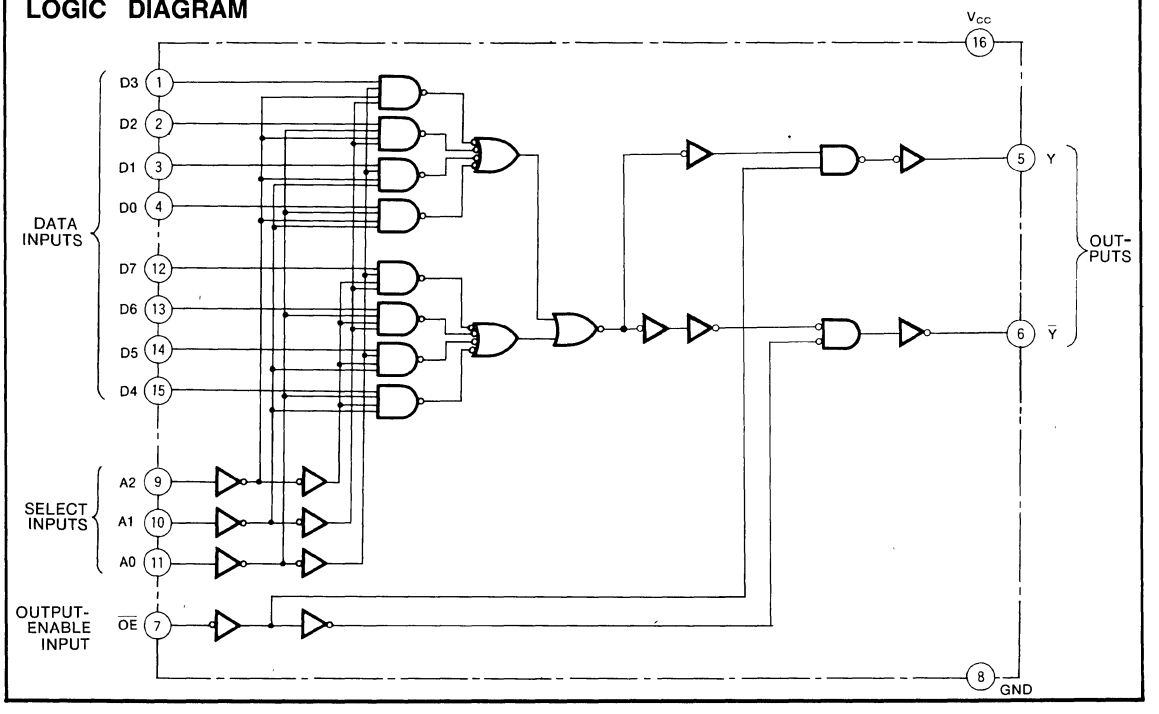
Use of silicon gate technology allows the M74HC151 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS151.

The M74HC151 consists of data selector functions for selecting one of eight input line signals and multiplexer functions for converting 8-bit parallel data into serial data using time-division.

The 8-line signal is applied to data inputs D0 through D7, and after one of the data inputs has been selected by select inputs A0 through A2, that input signal is output at Y or an inverted signal is output at $\overline{Y}$. By applying 8-bit parallel data to D0 through D7, and connecting the output of a synchronous octal counter to A0 through A2, D0 through D7 data will be output at Y synchronous with the clock pulse in the order of D0 - D7. When output-enable input $\overline{OE}$ is high, Y will become low and $\overline{Y}$ will become high irrespective of other inputs.

M74HC151 has the same functions and pin connections as the M74HC251, but the latter has a 3-state output.

LOGIC DIAGRAM



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FUNCTION TABLE (Note 1)

Inputs												Outputs	
A2	A1	A0	$\overline{OE}$	D0	D1	D2	D3	D4	D5	D6	D7	Y	$\overline{Y}$
X	X	X	H	X	X	X	X	X	X	X	X	L	H
L	L	L	L	L	X	X	X	X	X	X	X	L	H
L	L	L	L	H	X	X	X	X	X	X	X	H	L
L	L	H	L	X	L	X	X	X	X	X	X	L	H
L	L	H	L	X	H	X	X	X	X	X	X	H	L
L	H	L	L	X	X	L	X	X	X	X	X	L	H
L	H	L	L	X	X	H	X	X	X	X	X	H	L
L	H	H	L	X	X	X	L	X	X	X	X	L	H
L	H	H	L	X	X	X	H	X	X	X	X	H	L
H	L	L	L	X	X	X	X	L	X	X	X	L	H
H	L	L	L	X	X	X	X	H	X	X	X	H	L
H	L	H	L	X	X	X	X	X	L	X	X	L	H
H	L	H	L	X	X	X	X	X	H	X	X	H	L
H	H	L	L	X	X	X	X	X	X	L	X	L	H
H	H	L	L	X	X	X	X	X	X	H	X	H	L
H	H	H	L	X	X	X	X	X	X	X	L	L	H
H	H	H	L	X	X	X	X	X	X	X	H	H	L

Note 1 : X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation		500	mW
Tstg	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

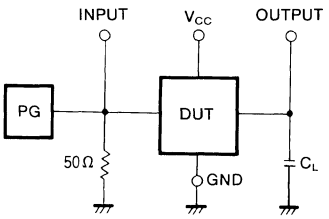
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 3)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (D − Y)				29	ns
t_{PHL}					29	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (D − $\overline{Y}$)				32	ns
t_{PHL}					32	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − Y)				43	ns
t_{PHL}					43	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − $\overline{Y}$)				35	ns
t_{PHL}					35	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{OE}$ − Y)				23	ns
t_{PHL}					23	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{OE}$ − $\overline{Y}$)				21	ns
t_{PHL}					21	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (D − Y)		2.0			195		244	ns
			4.5			39		49	
			6.0			33		41	
t_{PHL}			2.0			195		244	
			4.5			39		49	
			6.0			33		41	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (D − $\overline{Y}$)		2.0			185		231	ns
			4.5			37		46	
			6.0			32		40	
t_{PHL}			2.0			185		231	
			4.5			37		46	
			6.0			32		40	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − Y)		2.0			250		312	ns
			4.5			50		63	
			6.0			43		54	
t_{PHL}			2.0			250		312	
			4.5			50		63	
			6.0			43		54	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − $\overline{Y}$)		2.0			205		256	ns
			4.5			41		51	
			6.0			35		44	
t_{PHL}			2.0			205		256	
			4.5			41		51	
			6.0			35		44	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{OE}$ − Y)		2.0			140		175	ns
			4.5			28		35	
			6.0			24		30	
t_{PHL}			2.0			140		175	
			4.5			28		35	
			6.0			24		30	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{OE}$ − $\overline{Y}$)		2.0			127		159	ns
			4.5			25		32	
			6.0			22		28	
t_{PHL}			2.0			127		159	
			4.5			25		32	
			6.0			22		28	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				70				pF

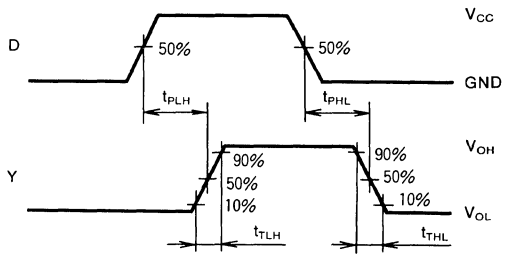
Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions
The power dissipated during operation under no-load conditions is calculated using the following formula
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

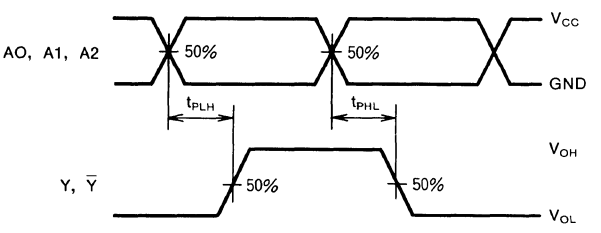
Note 3 : Test Circuit

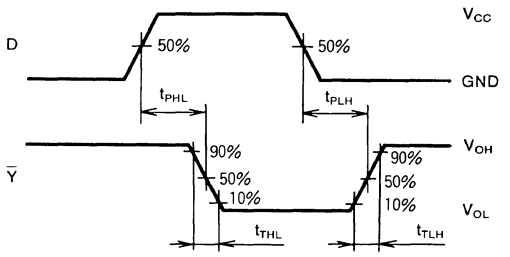


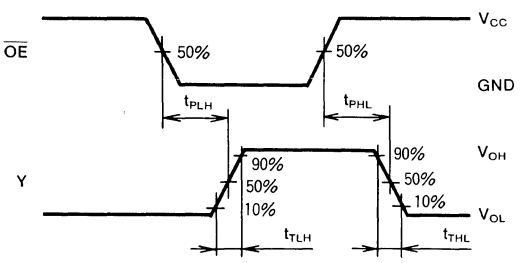
(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

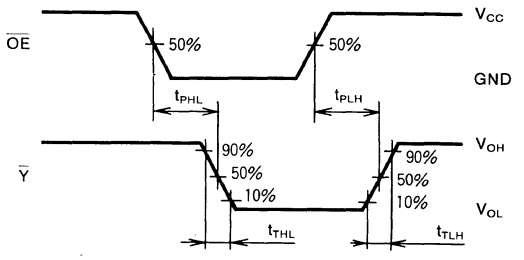
TIMING DIAGRAM











M74HC157P
M74HC157DP

QUADRUPLE 2-INPUT NONINVERTING DATA SELECTOR/MULTIPLEXER

DESCRIPTION

The M74HC157 is a semiconductor integrated circuit consisting of four 2-line to 1-line data selectors/multiplexers.

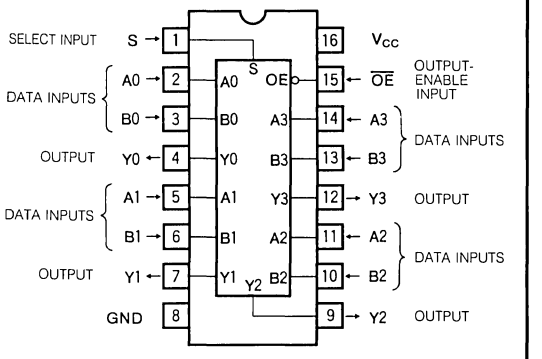
FEATURES

- High-speed: 12ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4
16P2P

FUNCTIONAL DESCRIPTION

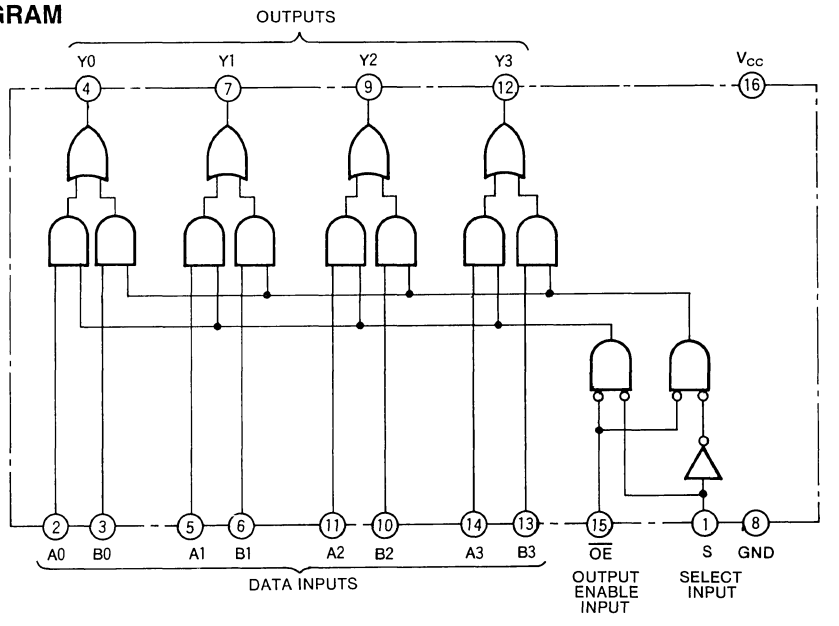
Use of silicon gate technology allows the M74HC157 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS157.

The M74HC157 consists of four circuits each containing data selector functions for selecting one of two input line signals and multiplexer functions for converting 2-bit parallel data into serial data using time-division.

The 2-line signals are applied to data inputs A and B, and after one of the data inputs has been selected by select input S, it is output at pin Y. By applying 2-bit parallel data to A and B, and connecting the output of a binary counter to S, A and B data will be output at Y synchronous with the clock pulse in the order A-B. Both S and ouput-enable input $\overline{OE}$ are common to all four circuits. When $\overline{OE}$ is high, all outputs, Y will become low irrespective of other inputs.

M74HC157 is the same functions and pin connections as M74HC257, differing in that the output of M74HC257 is 3-state.

LOGIC DIAGRAM



FUNCTION TABLE (Note 1)

Inputs				Output
$\overline{OE}$	S	A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

Note 1 : X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC157DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25°C			−40～+85°C		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9			V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25°C)

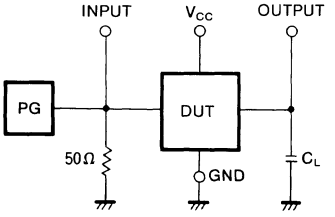
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level	C_L = 15pF (Note 4)			10	ns
t_{THL}	output transition time				10	
t_{PLH}	Low-level to high-level and high-level to low-level				20	ns
t_{PHL}	output propagation time (A, B − Y)				20	
t_{PLH}	Low-level to high-level and high-level to low-level				20	ns
t_{PHL}	output propagation time (S − Y)				20	
t_{PLH}	Low-level to high-level and high-level to low-level				18	ns
t_{PHL}	output propagation time ($\overline{OE}$ − Y)				18	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A, B − Y)		2.0			125		158	ns
			4.5			25		32	
			6.0			21		27	
t_{PHL}			2.0			125		158	
			4.5			25		32	
			6.0			21		27	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (S − Y)		2.0			125		158	ns
			4.5			25		32	
			6.0			21		27	
t_{PHL}			2.0			125		158	
			4.5			25		32	
			6.0			21		27	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{OE}$ − Y)		2.0			115		145	ns
			4.5			23		29	
			6.0			20		25	
t_{PHL}			2.0			115		145	
			4.5			23		29	
			6.0			20		25	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)				51				pF

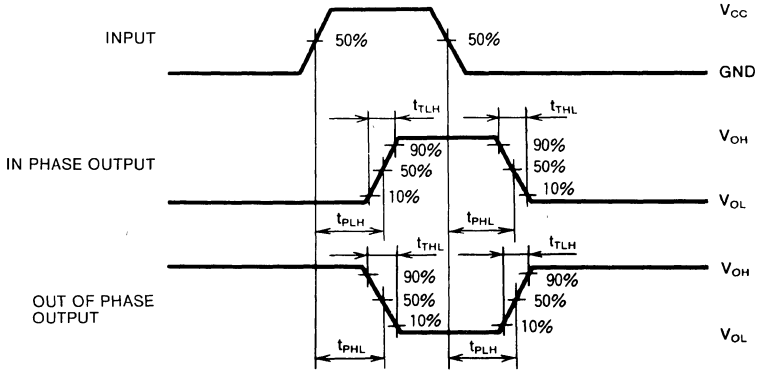
Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions
The power dissipated during operation under no-load conditions is calculated using the following formula
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 4 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%) · t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM



M74HC158P

QUADRUPLE 2-INPUT INVERTING DATA SELECTOR/MULTIPLEXER

DESCRIPTION

The M74HC158 is a semiconductor integrated circuit consisting of four 2-line to 1-line data selectors/multiplexers.

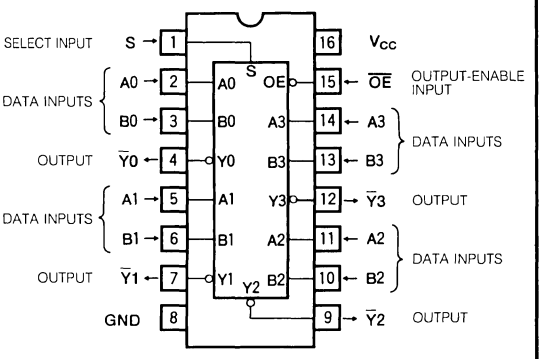
FEATURES

- High-speed: 12ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

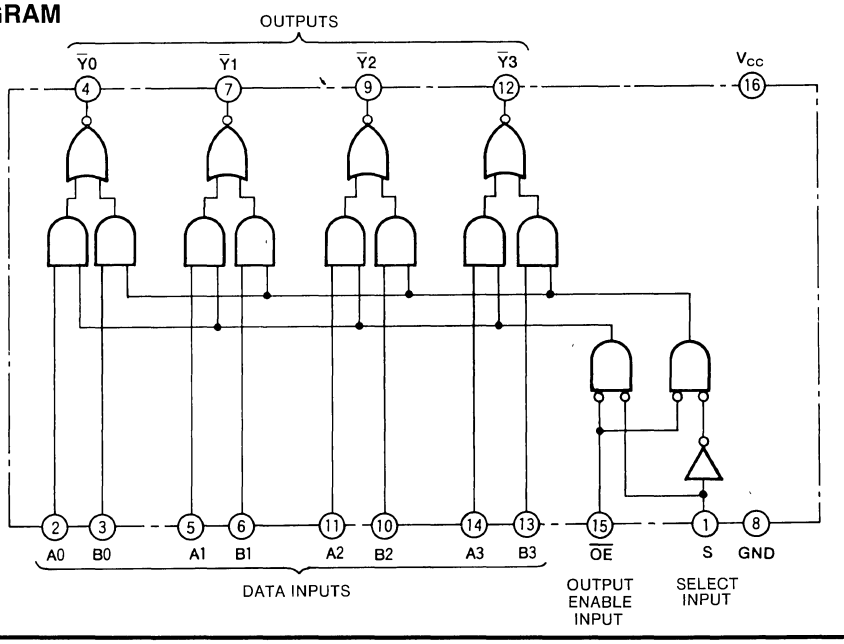
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC158 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS158.

The M74HC158 consists of four circuits each containing data selector functions for selecting one of two input line signals and multiplexer functions for converting 2-bit parallel data into serial data using time-division.

The 2-line signal is applied to data inputs A and B, and after one of the data inputs has been selected by select input S, it is inverted and output at pin $\overline{Y}$. By applying 2-bit parallel data to A and B, and connecting the output of a binary counter to S, the inverted A and B data will be output at $\overline{Y}$ synchronous with the clock pulse in the order A-B. Both S and ouput-enable input $\overline{OE}$ are common to all four circuits. When $\overline{OE}$ is high, all the outputs, $\overline{Y}$0 through $\overline{Y}$3, will become high irrespective of input level signals.

LOGIC DIAGRAM



FUNCTION TABLE (Note 1)

Inputs				Output
$\overline{OE}$	S	A	B	$\overline{Y}$
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

Note 1 : X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation		500	mW
Tstg	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0		0.1		0.1	V
			I_{OL} = 20μA	4.5		0.1		0.1	
			I_{OL} = 20μA	6.0		0.1		0.1	
			I_{OL} = 4.0mA	4.5		0.26		0.33	
			I_{OL} = 5.2mA	6.0		0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

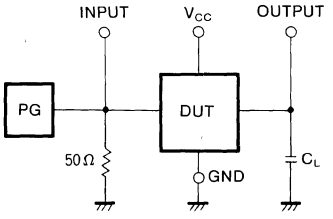
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level	C_L = 15pF (Note 3)			10	ns
t_{THL}	output transition time				10	
t_{PLH}	Low-level to high-level and high-level to low-level				20	ns
t_{PHL}	output propagation time (A, B − $\overline{Y}$)				20	
t_{PLH}	Low-level to high-level and high-level to low-level				20	ns
t_{PHL}	output propagation time (S − $\overline{Y}$)				20	
t_{PLH}	Low-level to high-level and high-level to low-level				18	ns
t_{PHL}	output propagation time ($\overline{OE}$ − $\overline{Y}$)				18	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A, B − $\overline{Y}$)		2.0			125		158	ns
			4.5			25		32	
			6.0			21		27	
t_{PHL}			2.0			125		158	
			4.5			25		32	
			6.0			21		27	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (S − $\overline{Y}$)		2.0			125		158	ns
			4.5			25		32	
			6.0			21		27	
t_{PHL}			2.0			125		158	
			4.5			25		32	
			6.0			21		27	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{OE}$ − $\overline{Y}$)		2.0			115		145	ns
			4.5			23		29	
			6.0			20		25	
t_{PHL}			2.0			115		145	
			4.5			23		29	
			6.0			20		25	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				82				pF

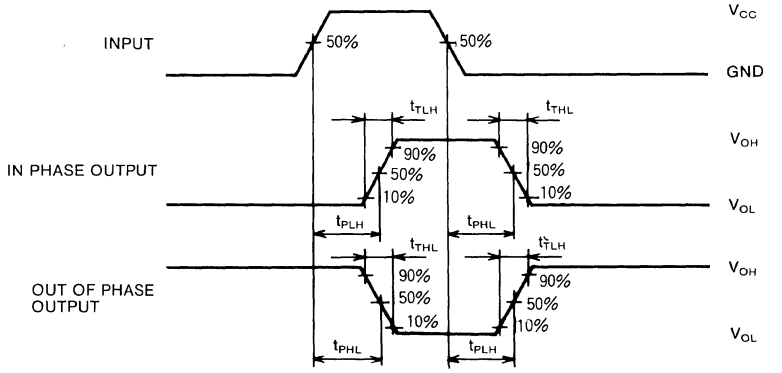
Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions
The power dissipated during operation under no-load conditions is calculated using the following formula
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 3 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%) t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM



MITSUBISHI ELECTRIC

M74HC160P

PRESETTABLE BCD COUNTER WITH ASYNCHRONOUS RESET

DESCRIPTION

The M74HC160 is a semiconductor integrated circuit consisting of a presettable synchronous BCD counter with direct reset input.

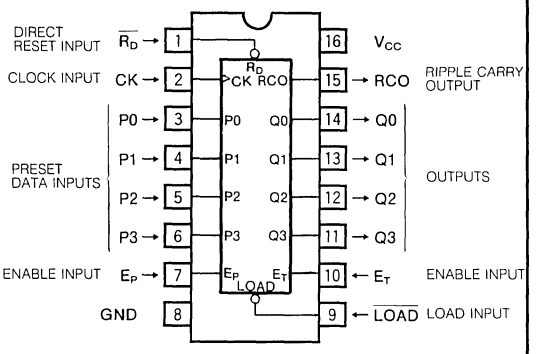
FEATURES

- Direct reset and synchronous preset inputs
- Enable input and ripple carry output for cascade connection
- High-speed: (clock frequency) 45MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

FUNCTIONAL DESCRIPTION

When the count pulse is applied to clock input CK, the number of count pulses will be output at outputs Q0 through Q3 synchronous with the count pulse in BCD code. Counting takes place when CK changes from low-level to high-level.

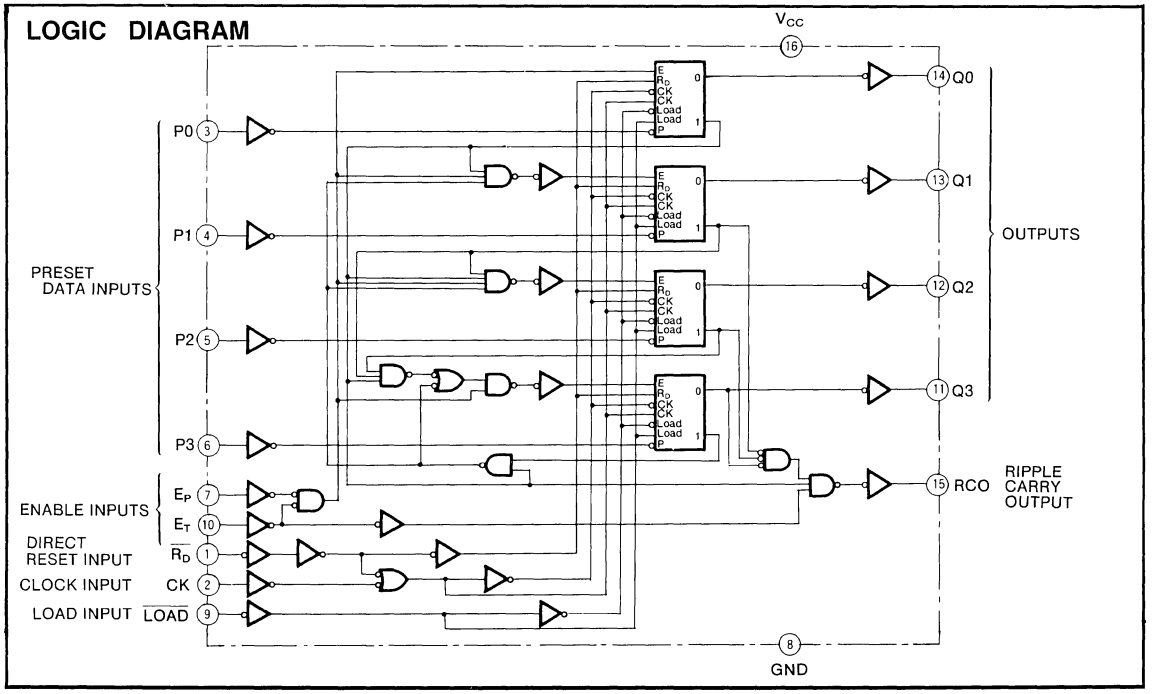
The preset functions synchronously with the count pulse. By supplying data to preset data inputs P0 through P3 and setting load input $\overline{LOAD}$ to low-level, when CK changes from low-level to high-level, the P0 through P3 signals will be output to Q0 through Q3, respectively, irrespective of enable inputs E_P and E_T. This permits presetting of the counter.

When values greater than 10 are preset, the count advances as shown in the State Transition Diagram.

The reset operates asynchronously, and by setting direct reset input $\overline{R_D}$ to low-level, Q0 through Q3 will become low irrespective of other inputs.

The ripple carry output RCO will become high only when Q0 is high, Q1 is low, Q2 is low, Q3 is high, and E_T is high. E_P, E_T and RCO are used in cascade connections of the counter in synchronous form when the counter is set up in a 10n arrangement. (See the Application Example.)

LOGIC DIAGRAM



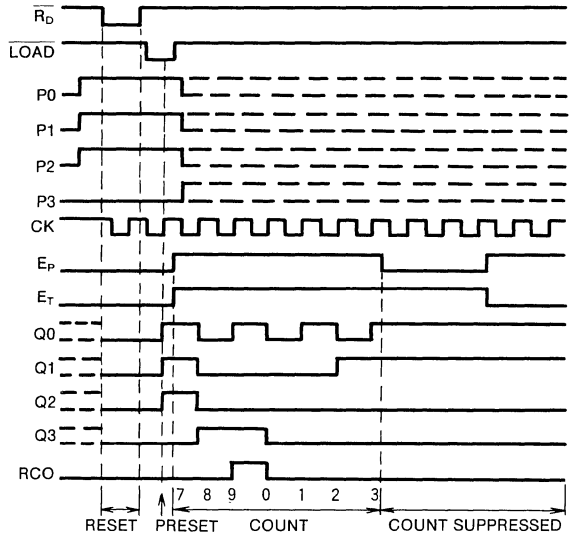
PRESETTABLE BCD COUNTER WITH ASYNCHRONOUS RESET

FUNCTION TABLE (Note 1)

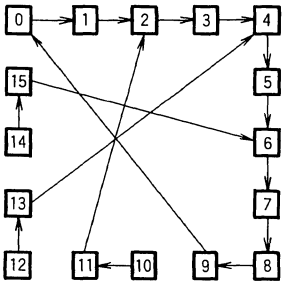
Inputs					Outputs				
$\overline{R_D}$	LOAD	E_T	E_P	CK	Q0	Q1	Q2	Q3	RCO
L	X	X	X	X	L	L	L	L	L
H	L	L	X	↑	P0	P1	P2	P3	L
H	L	H	X	↑					L*
H	H	H	H	↑	Count				L*
H	H	L	X	X	Count suppressed				L
H	H	H	L	X	Count suppressed				L*

Note 1 : ↑ : Change from low to high level
* : RCO is normally low, but becomes high when Q0 is high, Q1 is low, Q2 is low, Q3 is high, and E_T is high. Accordingly, RCO=Q0 · $\overline{Q1}$ · $\overline{Q2}$ · Q3 · E_T
: X : Irrelevant

OPERATION TIMING DIAGRAM



STATE TRANSITION DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
Pd	Power dissipation		500	mW
Tstg	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

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ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

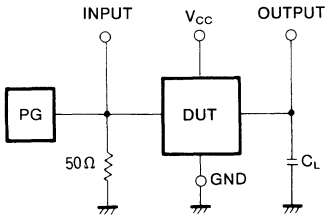
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 3)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level				10	ns
t_{THL}	output transition time				10	
t_{PLH}	Low-level to high-level and high-level to low-level				28	ns
t_{PHL}	output propagation time (CK−Q)				34	
t_{PHL}	High-level to low-level output propagation time ($\overline{R_D}$ − Q)				36	ns
t_{PLH}	Low-level to high-level and high-level to low-level				26	ns
t_{PHL}	output propagation time (E_T − RCO)				32	
t_{PLH}	Low-level to high-level and high-level to low-level				30	ns
t_{PHL}	output propagation time (CK − RCO)				36	
t_{PHL}	High-level to low-level output propagation time ($\overline{R_D}$ − RCO)				38	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 3)	2.0	5			4		MHz
			4.5	27			21		
			6.0	32			25		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q)		2.0			170		214	s
			4.5			34		43	
			6.0			29		36	
t_{PHL}			2.0			205		258	
			4.5			41		52	
			6.0			35		44	
t_{PHL}	High-level to low-level output propagation time ($\overline{R_D}$ − Q)		2.0			210		265	ns
			4.5			42		53	
			6.0			36		45	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (E_T − RCO)		2.0			160		202	ns
			4.5			32		40	
			6.0			27		34	
t_{PHL}			2.0			195		246	
			4.5			39		49	
			6.0			33		42	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − RCO)		2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PHL}			2.0			215		271	
			4.5			43		54	
			6.0			37		46	
t_{PHL}	High-level to low-level output propagation time ($\overline{R_D}$ − RCO)		2.0			220		277	ns
			4.5			44		55	
			6.0			37		47	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				57				pF

Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions
The power dissipated during operation under no-load conditions is calculated using the following formula
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 3 : Test Circuit



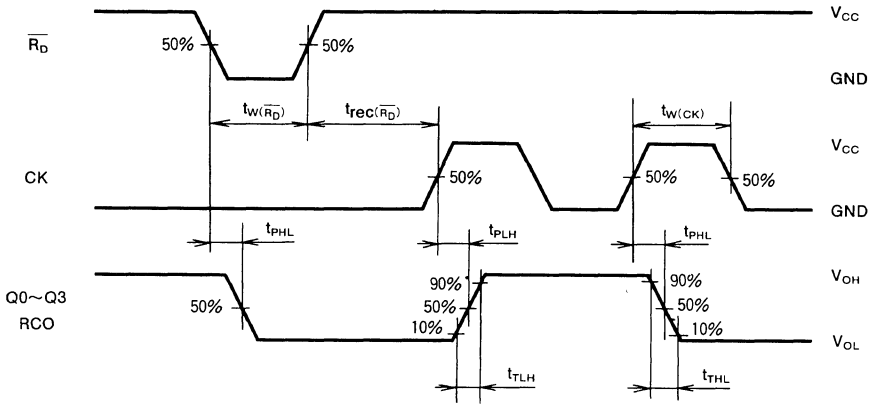
(1) The pulse generator (PG) has the following characteristics (10%~90%) t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

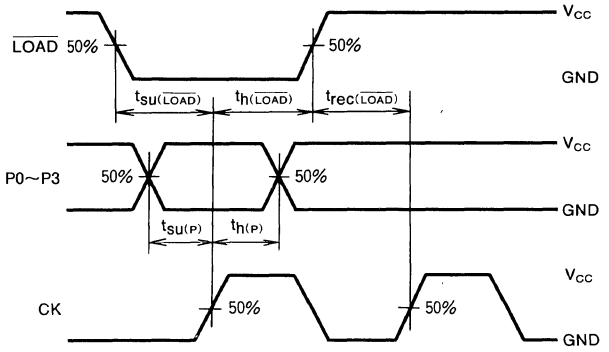
MITSUBISHI ELECTRIC

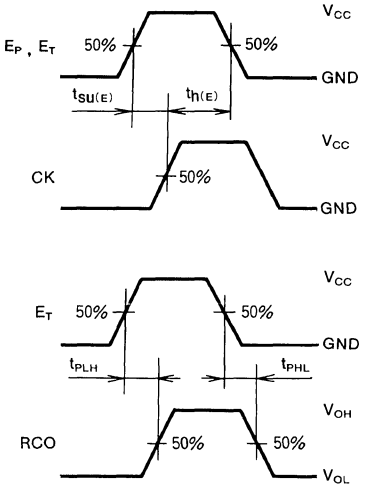
TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
$t_{w(CK)}$	Clock pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
$t_{w(\overline{R_D})}$	Direct reset pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
$t_{su(P)}$	P setup time with respect to CK		2.0	150			189		ns
			4.5	30			38		
			6.0	26			32		
$t_{su(\overline{LOAD})}$	$\overline{LOAD}$ setup time with respect to CK		2.0	135			170		ns
			4.5	27			34		
			6.0	23			29		
$t_{su(E)}$	E_T, E_P setup time with respect to CK		2.0	200			250		ns
			4.5	40			50		
			6.0	34			43		
$t_{h(P)}$	P hold time with respect to CK		2.0	50			63		ns
			4.5	10			13		
			6.0	9			11		
$t_{h(\overline{LOAD})}$	$\overline{LOAD}$ hold time with respect to CK		2.0	0			0		ns
			4.5	0			0		
			6.0	0			0		
$t_{h(E)}$	E_T, E_P hold time with respect to CK		2.0	0			0		ns
			4.5	0			0		
			6.0	0			0		
$t_{rec(\overline{R_D})}$	$\overline{R_D}$ recovery time with respect to CK		2.0	125			158		ns
			4.5	25			32		
			6.0	21			27		
$t_{rec(\overline{LOAD})}$	$\overline{LOAD}$ recovery time with respect to CK		2.0	125			158		ns
			4.5	25			32		
			6.0	21			27		

TIMING DIAGRAM

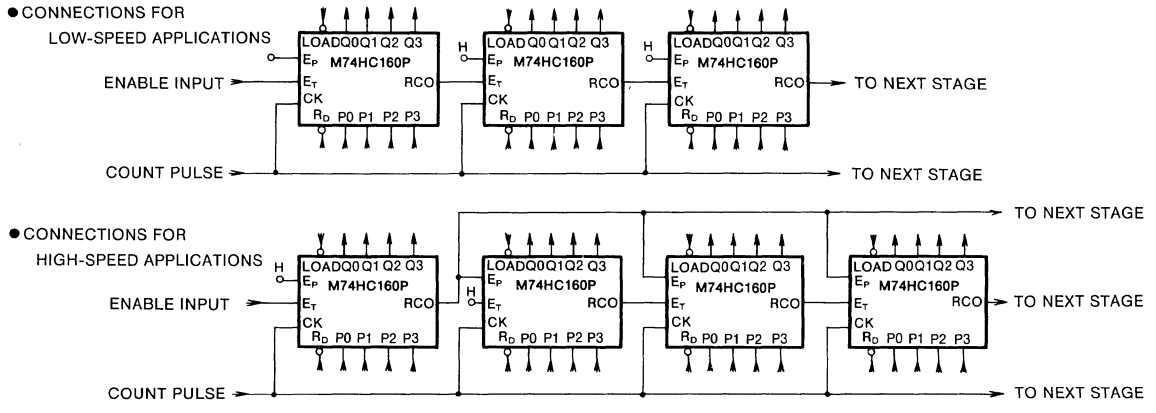






APPLICATION EXAMPLE

10^n COUNTER USING CASCADE CONNECTION



MITSUBISHI ELECTRIC

M74HC161P
M74HC161DP

PRESETTABLE 4-BIT BINARY COUNTER WITH ASYNCHRONOUS RESET

DESCRIPTION

The M74HC161 is a semiconductor integrated circuit consisting of a presettable synchronous 4-bit binary (hexadecimal) counter with direct reset input.

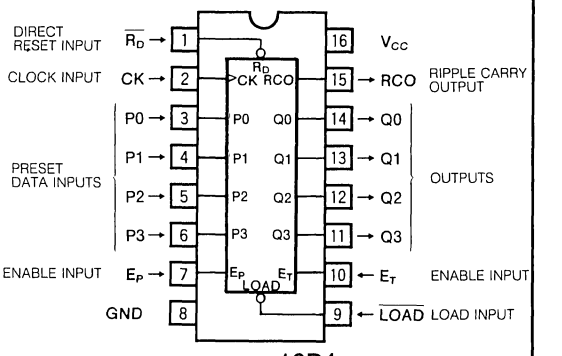
FEATURES

- Direct reset and synchronous preset inputs
- Enable input and ripple carry output for cascade connection
- High-speed: (clock-frequency) 45MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4
16P2P

FUNCTIONAL DESCRIPTION

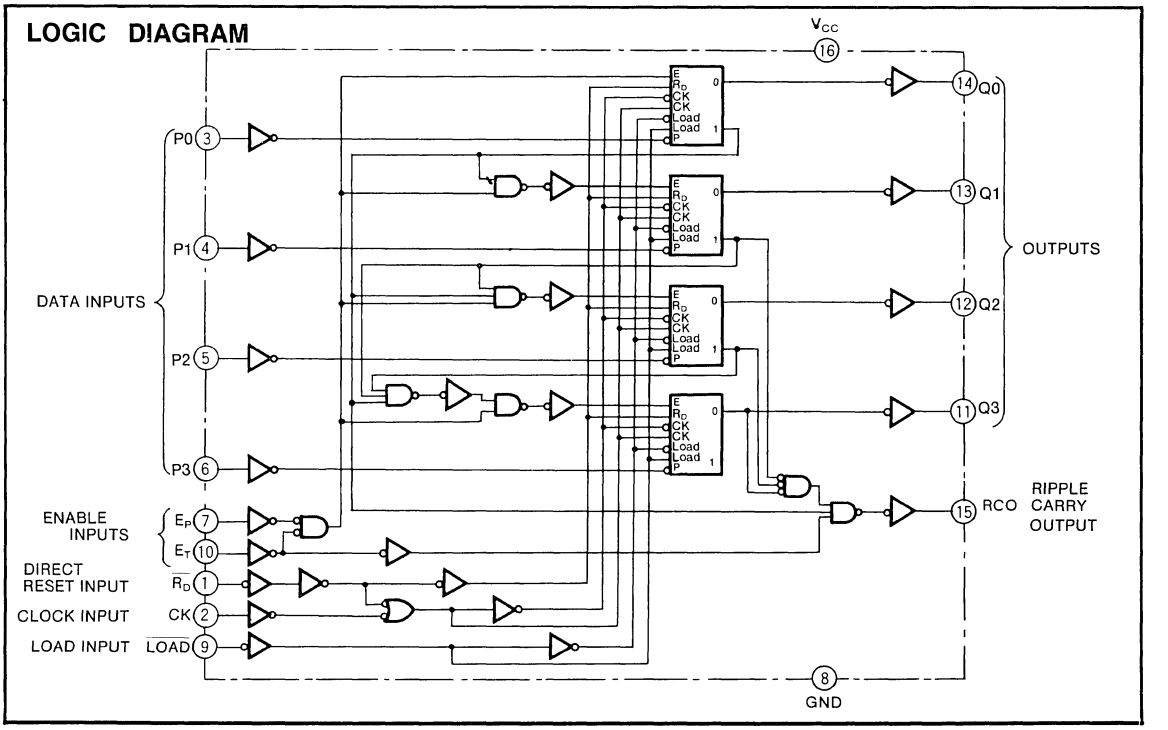
When the count pulse is applied to clock input CK, the number of count pulses will be output at outputs Q0 through Q3 synchronous with the count pulse in 4-bit binary code. Counting takes place when CK changes from low-level to high-level.

The preset functions synchronously with the count pulse. By supplying data to data inputs P0 through P3 and setting load input $\overline{LOAD}$ to low-level, when CK changes from low-level to high-level, the P0 through P3 signals will be output to Q0 through Q3, respectively, irrespective of enable inputs E_P and E_T. This permits presetting of the counter.

The reset operates asynchronously, and by setting direct reset input $\overline{R_D}$ to low-level, Q0 through Q3 will become low, irrespective of other inputs.

The ripple carry output RCO will become high only when all of Q0, Q1, Q2, Q3 and E_T are high. E_P, E_T and RCO are used in cascade connections of the counter in synchronous form when the counter is set up in a 10^n arrangement. (See the Application Example.)

LOGIC DIAGRAM



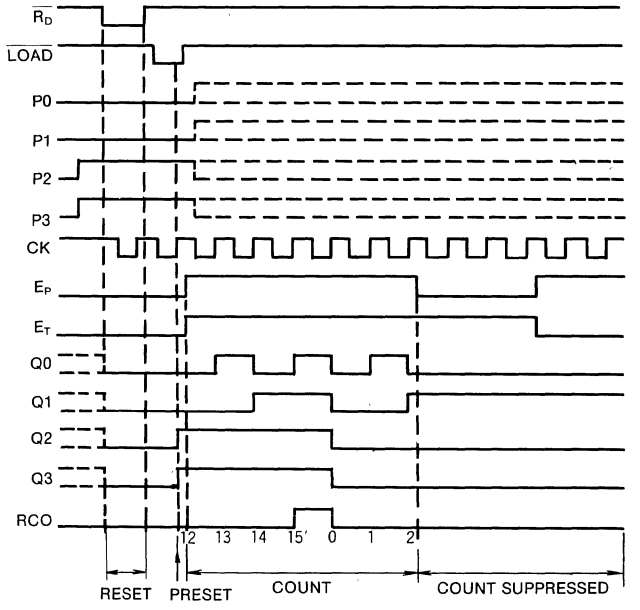
PRESETTABLE 4-BIT BINARY COUNTER WITH ASYNCHRONOUS RESET

FUNCTION TABLE (Note 1)

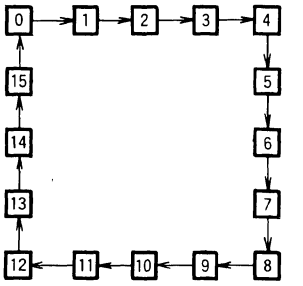
Inputs					Outputs				
$\overline{R_D}$	LOAD	E_T	E_P	CK	Q0	Q1	Q2	Q3	RCO
L	X	X	X	X	L	L	L	L	L
H	L	L	X	↑	P0	P1	P2	P3	L
H	L	H	X	↑					L*
H	H	H	H	↑	Count				L*
H	H	L	X	X	Count suppressed				L
H	H	H	L	X	Count suppressed				L*

Note 1 : ↑ : Change from low to high level
* : RCO is normally low, but becomes high when all of Q0, Q1, $\overline{Q2}$, Q3 and E_T are high Accordingly, RCO = Q0 · Q1 · $\overline{Q2}$ · Q3 · E_T
X : Irrelevant

OPERATION TIMING DIAGRAM



STATE TRANSITION DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC161DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃

PRESETTABLE 4-BIT BINARY COUNTER WITH ASYNCHRONOUS RESET

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

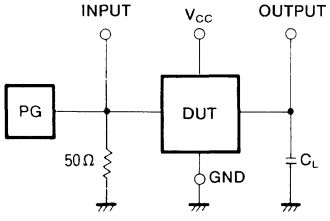
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 4)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level				10	ns
t_{THL}	output transition time				10	
t_{PLH}	Low-level to high-level and high-level to low-level				28	ns
t_{PHL}	output propagation time (CK −Q)				34	
t_{PHL}	High-level to low-level output propagation time ($\overline{R_D}$ − Q)				36	ns
t_{PLH}	Low-level to high-level and high-level to low-level				26	ns
t_{PHL}	output propagation time (E_T − RCO)				32	
t_{PLH}	Low-level to high-level and high-level to low-level				30	ns
t_{PHL}	output propagation time (CK − RCO)				36	
t_{PHL}	High-level to low-level output propagation time ($\overline{R_D}$ − RCO)				38	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	2.0	5			4		MHz
			4.5	27			21		
			6.0	32			25		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q)		2.0			170		214	ns
			4.5			34		43	
			6.0			29		36	
t_{PHL}			2.0			205		258	
			4.5			41		52	
			6.0			35		44	
t_{PHL}	High-level to low-level output propagation time ($\overline{R_D}$ − Q)		2.0			210		265	ns
			4.5			42		53	
			6.0			36		45	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (E_T − RCO)		2.0			160		202	ns
			4.5			32		40	
			6.0			27		34	
t_{PHL}			2.0			195		246	
			4.5			39		49	
			6.0			33		42	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − RCO)		2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PHL}			2.0			215		271	
			4.5			43		54	
			6.0			37		46	
t_{PHL}	High-level to low-level output propagation time ($\overline{R_D}$ − RCO)		2.0			220		277	ns
			4.5			44		55	
			6.0			37		47	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)				57				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula.
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 4 : Test Circuit

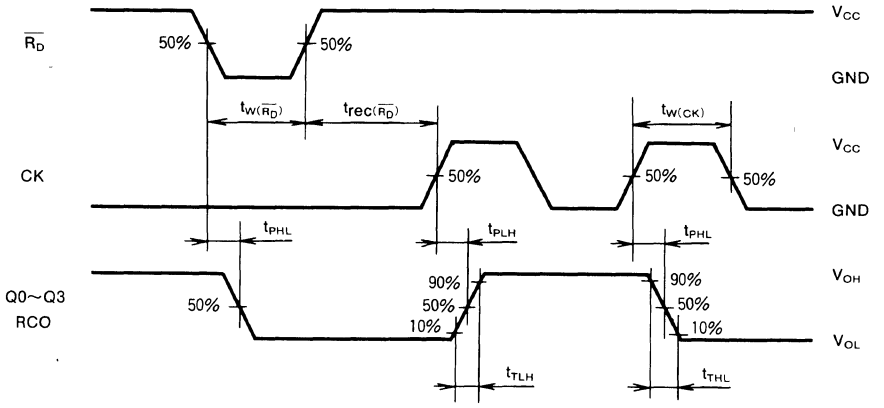


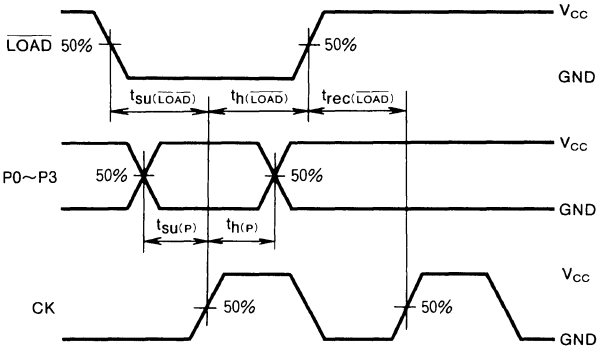
(1) The pulse generator (PG) has the following characteristics (10%~90%). t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

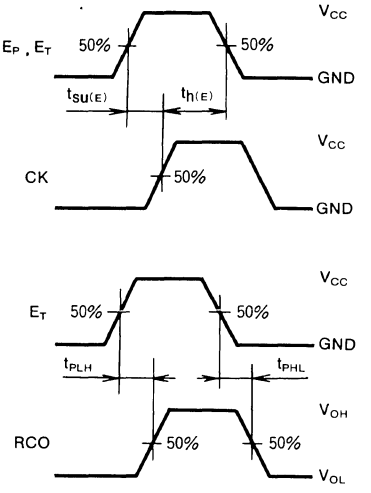
TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
$t_{w(CK)}$	Clock pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
$t_{w(\overline{R_D})}$	Direct reset pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
$t_{su(P)}$	P setup time with respect to CK		2.0	150			189		ns
			4.5	30			38		
			6.0	26			32		
$t_{su(\overline{LOAD})}$	$\overline{LOAD}$ setup time with respect to CK		2.0	135			170		ns
			4.5	27			34		
			6.0	23			29		
$t_{su(E)}$	E_T, E_P setup time with respect to CK		2.0	200			250		ns
			4.5	40			50		
			6.0	34			43		
$t_{h(P)}$	P hold time with respect to CK		2.0	50			63		ns
			4.5	10			13		
			6.0	9			11		
$t_{h(\overline{LOAD})}$	$\overline{LOAD}$ hold time with respect to CK		2.0	0			0		ns
			4.5	0			0		
			6.0	0			0		
$t_{h(E)}$	E_T, E_P hold time with respect to CK		2.0	0			0		ns
			4.5	0			0		
			6.0	0			0		
$t_{rec(\overline{R_D})}$	$\overline{R_D}$ recovery time with respect to CK		2.0	125			158		ns
			4.5	25			32		
			6.0	21			27		
$t_{rec(\overline{LOAD})}$	$\overline{LOAD}$ recovery time with respect to CK		2.0	125			158		ns
			4.5	25			32		
			6.0	21			27		

TIMING DIAGRAM

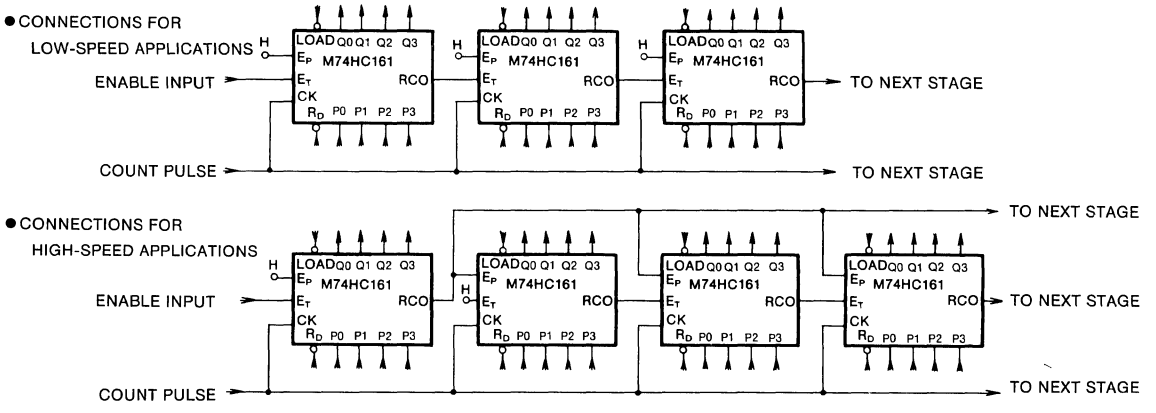






APPLICATION EXAMPLE

10^n COUNTER USING CASCADE CONNECTION



M74HC162P

PRESETTABLE BCD COUNTER WITH SYNCHRONOUS RESET

DESCRIPTION

The M74HC162 is a semiconductor integrated circuit consisting of a presettable synchronous BCD counter with synchronous reset input.

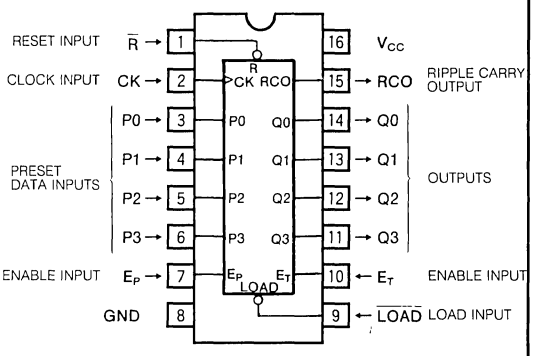
FEATURES

- Synchronous reset and synchronous preset inputs
- Enable input and ripple carry output for cascade connection
- High-speed: (clock frequency) 45MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package (max) (V_{CC}=5V, T_a=25°C, quiescent state)
- Wide operating voltage range. V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

FUNCTIONAL DESCRIPTION

When the count pulse is applied to clock input CK, the number of count pulses will be output at outputs Q0 through Q3 synchronous with the count pulse in BCD code. Counting takes place when CK changes from low-level to high-level.

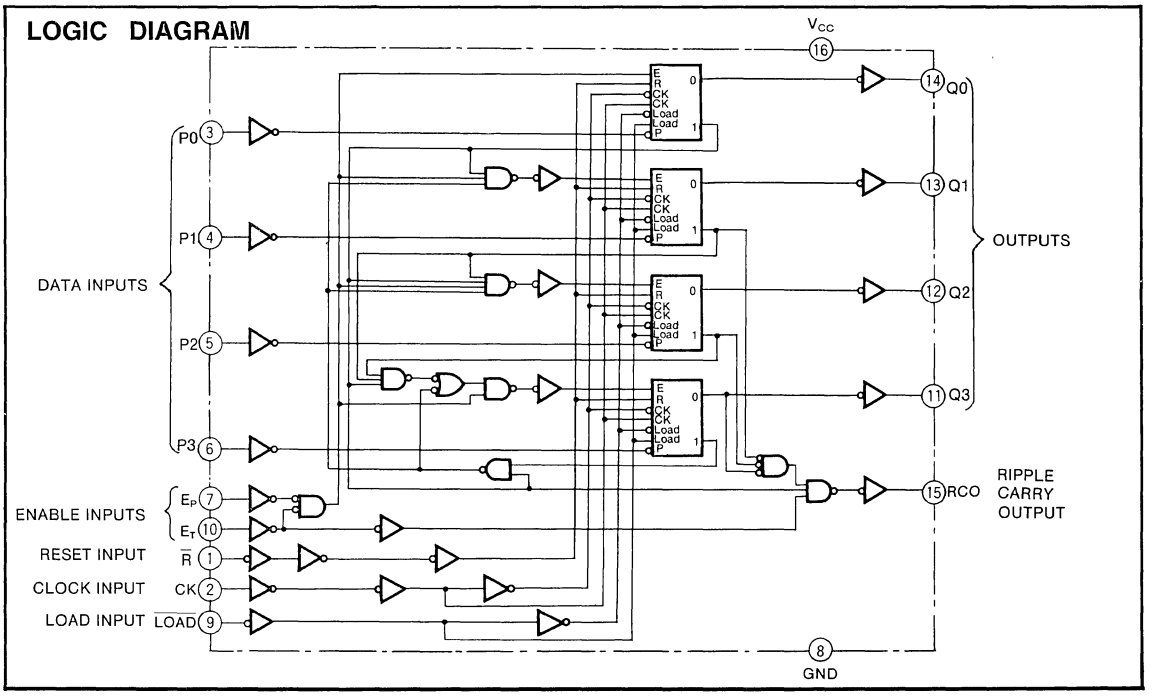
The preset functions synchronously with the count pulse. By supplying data to data inputs P0 through P3 and setting load input $\overline{LOAD}$ to low-level, when CK changes from low-level to high-level, the P0 through P3 signals will be output to Q0 through Q3, respectively, irrespective of enable inputs E_P and E_T. This permits presetting of the counter.

When values greater than 10 are preset, the count advances as shown in the State Transition Diagram.

The reset operates synchronously with the count pulse, and by setting reset input $\overline{R}$ to low-level, Q0 through Q3 will become low when CK changes from low-level to high-level.

The ripple carry output RCO will become high only when Q0 is high, Q1 is low, Q2 is low, Q3 is high, and E_T is high. E_P, E_T and RCO are used in cascade connections of the counter in synchronous form when the counter is set up in a 10^n arrangement. (See the Application Example.)

LOGIC DIAGRAM



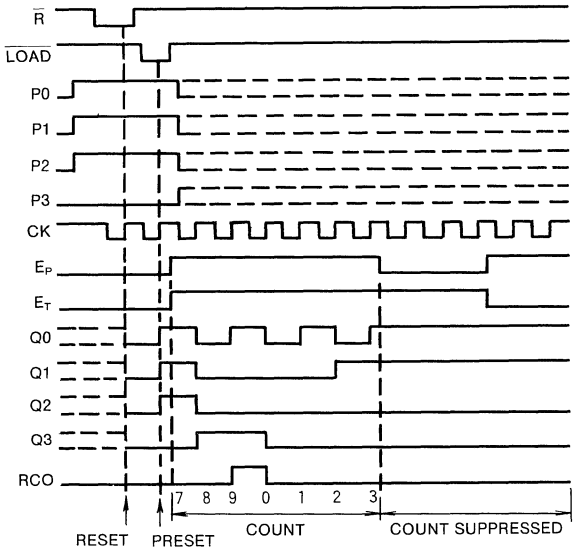
PRESETTABLE BCD COUNTER WITH SYNCHRONOUS RESET

FUNCTION TABLE (Note 1)

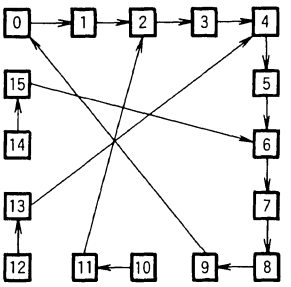
Inputs					Outputs				
$\overline{R}$	$\overline{LOAD}$	E_T	E_P	CK	Q0	Q1	Q2	Q3	RCO
L	X	X	X	↑	L	L	L	L	L
H	L	L	X	↑	P0	P1	P2	P3	L
H	L	H	X	↑					L*
H	H	H	H	↑	Count				L*
H	H	L	X	X	Count suppressed				L
H	H	H	L	X	Count suppressed				L*

Note 1 : ↑ : Change from low to high level
∗ : RCO is normally low, but becomes high when Q0 is high, Q1 is low, Q2 is low, Q3 is high and E_T is high. Accordingly, RCO=Q0 · $\overline{Q1}$ · $\overline{Q2}$ · Q3 · E_T
X : Irrelevant

OPERATION TIMING DIAGRAM



STATE TRANSITION DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation		500	mW
Tstg	Storage temperature range		−65~+150	℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40~+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

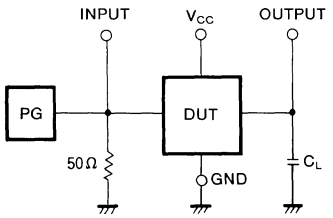
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
fmax	Maximum clock frequency	C_L = 15pF (Note 3)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level				10	ns
t_{THL}	output transition time				10	
t_{PLH}	Low-level to high-level and high-level to low-level				28	ns
t_{PHL}	output propagation time (CK −Q)				34	
t_{PLH}	Low-level to high-level and high-level to low-level				26	ns
t_{PHL}	output propagation time (E_T − RCO)				32	
t_{PLH}	Low-level to high-level and high-level to low-level				30	ns
t_{PHL}	output propagation time (CK − RCO)				36	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	V_{CC}(V)	Limits 25℃ Min	Typ	Max	Limits −40~+85℃ Min	Max	Unit
f_{max}	Maximum clock frequency	C_L = 50pF (Note 3)	2.0	5			4		MHz
			4.5	27			21		
			6.0	32			25		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q)		2.0			170		214	ns
			4.5			34		43	
			6.0			29		36	
t_{PHL}			2.0			205		258	
			4.5			41		52	
			6.0			35		44	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (E_T − RCO)		2.0			160		202	ns
			4.5			32		40	
			6.0			27		34	
t_{PHL}			2.0			195		246	
			4.5			39		49	
			6.0			33		42	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − RCO)		2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PHL}			2.0			215		271	
			4.5			43		54	
			6.0			37		46	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				58				pF

Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions
The power dissipated during operation under no-load conditions is calculated using the following formula
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 3 : Test Circuit

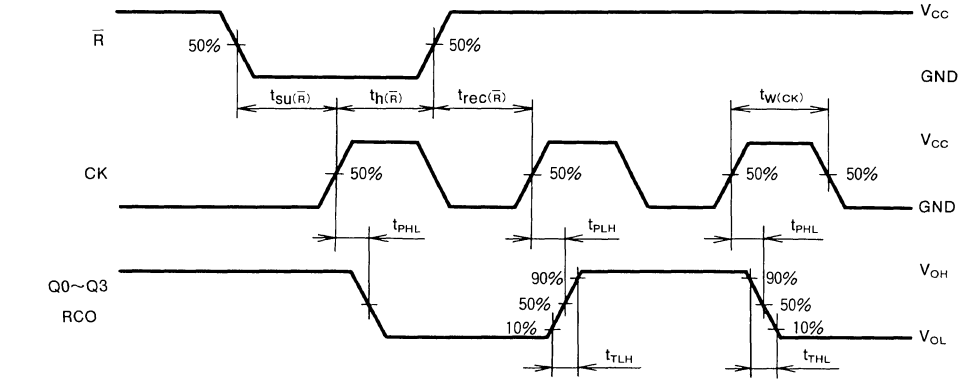


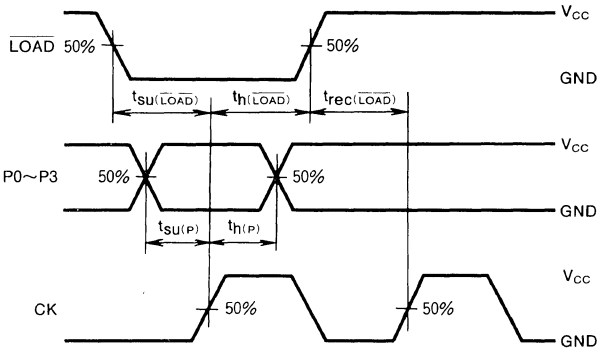
(1) The pulse generator (PG) has the following characteristics (10%~90%) t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

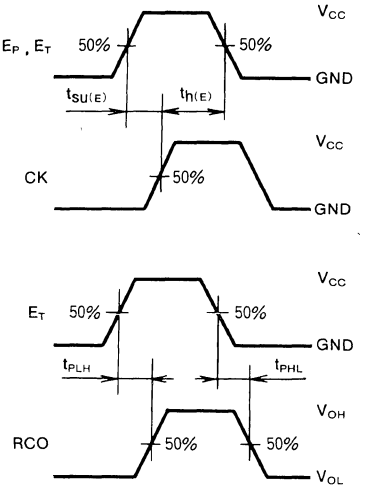
TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40~+85℃		
		V_{CC}(V)	Min	Typ	Max	Min	Max	
$t_{w(CK)}$	Clock pulse width	2.0	80			101		ns
		4.5	16			20		
		6.0	14			17		
$t_{su(P)}$	P setup time with respect to CK	2.0	150			189		ns
		4.5	30			38		
		6.0	26			32		
$t_{su(\overline{LOAD})}$	$\overline{LOAD}$ setup time with respect to CK	2.0	135			170		ns
		4.5	27			34		
		6.0	23			29		
$t_{su(\overline{R})}$	$\overline{R}$ setup time with respect to CK	2.0	160			202		ns
		4.5	32			40		
		6.0	27			34		
$t_{su(E)}$	E_T, E_P setup time with respect to CK	2.0	200			250		ns
		4.5	40			50		
		6.0	34			43		
$t_{h(P)}$	P hold time with respect to CK	2.0	50			63		ns
		4.5	10			13		
		6.0	9			11		
$t_{h(\overline{LOAD})}$	$\overline{LOAD}$ hold time with respect to CK	2.0	0			0		ns
		4.5	0			0		
		6.0	0			0		
$t_{h(\overline{R})}$	$\overline{R}$ hold time with respect to CK	2.0	0			0		ns
		4.5	0			0		
		6.0	0			0		
$t_{h(E)}$	E_T, E_P hold time with respect to CK	2.0	0			0		ns
		4.5	0			0		
		6.0	0			0		
$t_{rec(\overline{R})}$	$\overline{R}$ recovery time with respect to CK	2.0	125			158		ns
		4.5	25			32		
		6.0	21			27		
$t_{rec(\overline{LOAD})}$	$\overline{LOAD}$ recovery time with respect to CK	2.0	125			158		ns
		4.5	25			32		
		6.0	21			27		

TIMING DIAGRAM

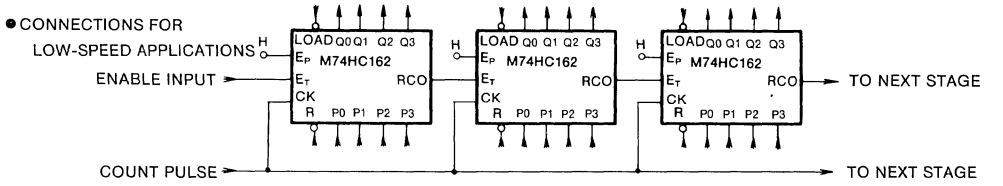


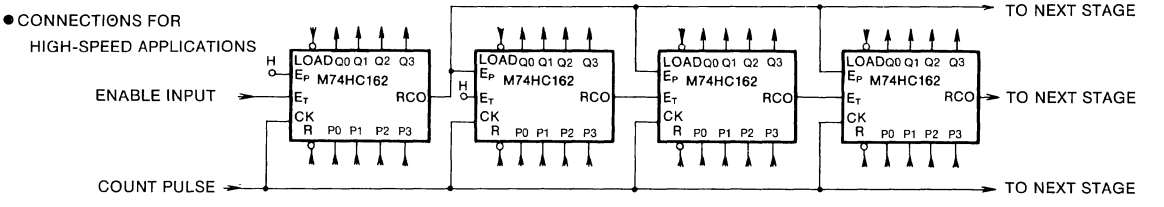




APPLICATION EXAMPLE

10^n COUNTER USING CASCADE CONNECTION





M74HC163P
M74HC163DP

PRESETTABLE 4-BIT BINARY COUNTER WITH SYNCHRONOUS RESET

DESCRIPTION

The M74HC163 is a semiconductor integrated circuit consisting of a presettable synchronous 4-bit binary (hexadecimal) counter with synchronous reset input

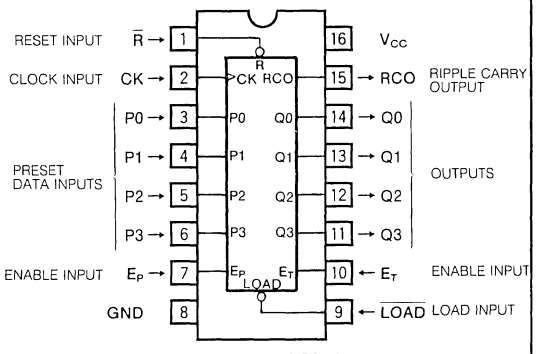
FEATURES

- Synchronous reset and synchronous preset inputs
- Enable input and ripple carry output for cascade connection
- High-speed: (clock frequency) 45MHz typ (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package (max) (V_{CC}=5V, T_a=25°C, quiescent state)
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85°C

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4 16P2P

FUNCTIONAL DESCRIPTION

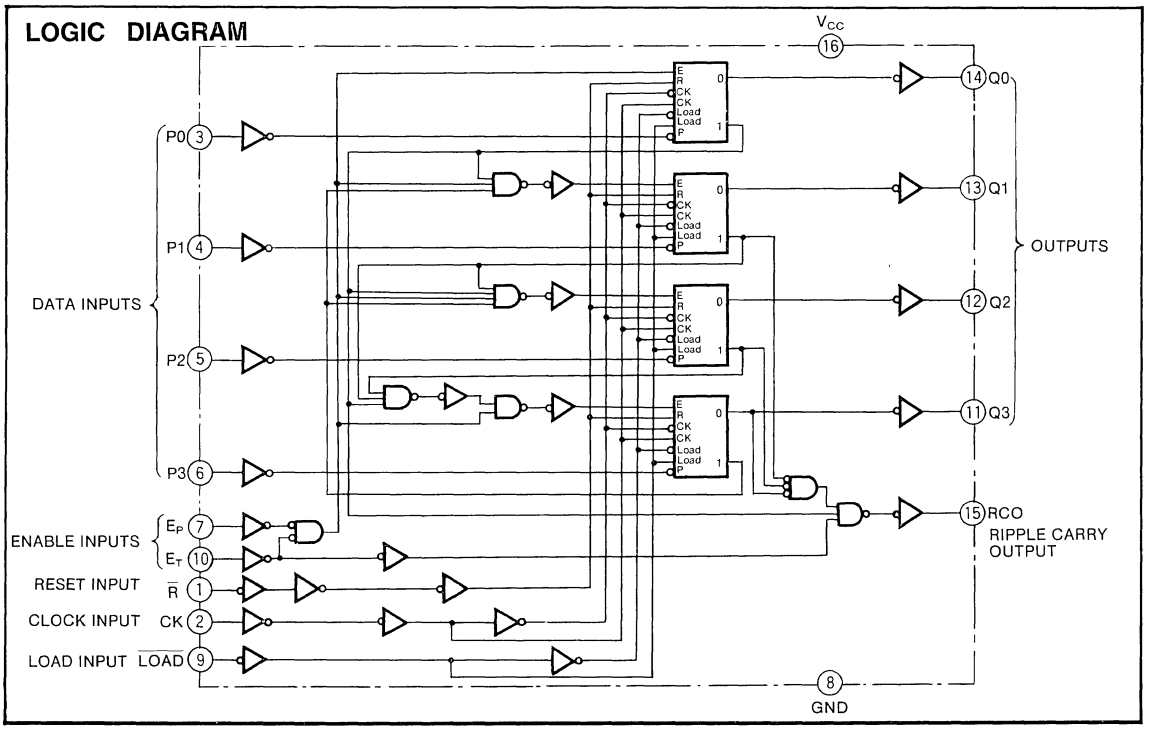
When the count pulse is applied to clock input CK, the number of count pulses will be output at outputs Q0 through Q3 synchronous with the count pulse in 4-bit binary code. Counting takes place when CK changes from low-level to high-level.

The preset functions synchronously with the count pulse. By supplying data to data inputs P0 through P3 and setting load input $\overline{LOAD}$ to low-level, when CK changes from low-level to high-level, the P0 through P3 signals will be output to Q0 through Q3, respectively, irrespective of enable inputs E_P and E_T. This permits presetting of the counter.

The reset operates synchronously with the count pulse, and by setting reset input $\overline{R}$ to low-level, Q0 through Q3 will become low when CK changes from low-level to high-level

The ripple carry output RCO will become high only when Q0, Q1, Q2, Q3 and E_T are high. E_P, E_T and RCO are used in cascade connections of the counter in synchronous form when the counter is set up in a 10^n arrangement. (See the Application Example.)

LOGIC DIAGRAM



M74HC163P
M74HC163DP

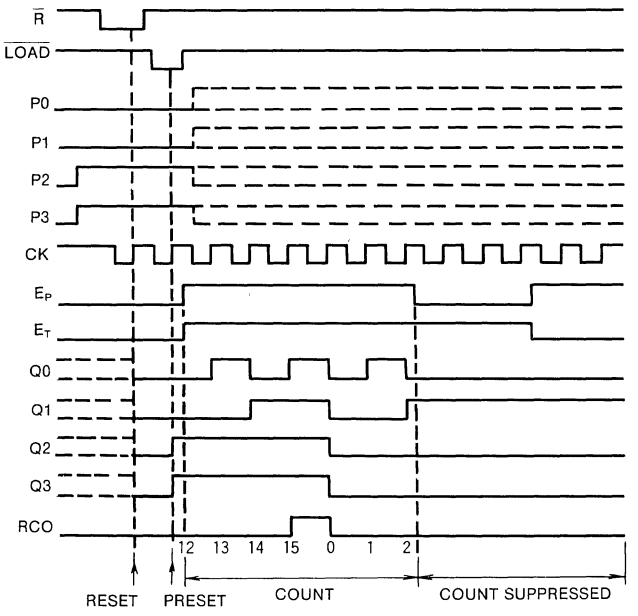
PRESETTABLE 4-BIT BINARY COUNTER WITH SYNCHRONOUS RESET

FUNCTION TABLE (Note 1)

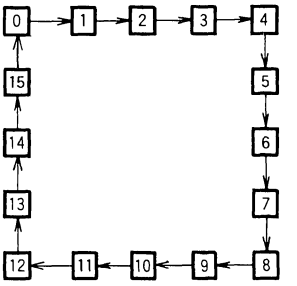
Inputs					Outputs				
$\overline{R}$	$\overline{LOAD}$	E_T	E_P	CK	Q0	Q1	Q2	Q3	RCO
L	X	X	X	↑	L	L	L	L	L
H	L	L	X	↑	P0	P1	P2	P3	L
H	L	H	X	↑					L*
H	H	H	H	↑	Count				L*
H	H	L	X	X	Count suppressed				L
H	H	H	L	X	Count suppressed				L*

Note 1 : ↑ : Change from low to high level
* : RCO is normally low, but becomes high when all Q0, Q1, Q2, Q3 and E_T are high Accordingly, RCO = Q0 · $\overline{Q1}$ · $\overline{Q2}$ · Q3 · E_T
X : Irrelevant

OPERATION TIMING DIAGRAM



STATE TRANSITION DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC163DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃

PRESETTABLE 4-BIT BINARY COUNTER WITH SYNCHRONOUS RESET

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

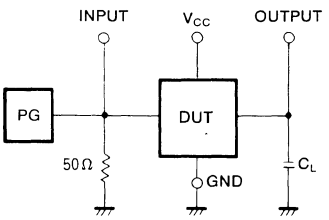
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 4)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level				10	ns
t_{THL}	output transition time				10	
t_{PLH}	Low-level to high-level and high-level to low-level				28	ns
t_{PHL}	output propagation time (CK − Q)				34	
t_{PLH}	Low-level to high-level and high-level to low-level				26	ns
t_{PHL}	output propagation time (E_T − RCO)				32	
t_{PLH}	Low-level to high-level and high-level to low-level				30	ns
t_{PHL}	output propagation time (CK − RCO)				36	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	2.0	5			4		MHz
			4.5	27			21		
			6.0	32			25		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q)		2.0			170		214	ns
			4.5			34		43	
			6.0			29		36	
t_{PHL}			2.0			205		258	
			4.5			41		52	
			6.0			35		44	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (E_T − RCO)		2.0			160		202	ns
			4.5			32		40	
			6.0			27		34	
t_{PHL}			2.0			195		246	
			4.5			39		49	
			6.0			33		42	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − RCO)		2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PHL}			2.0			215		271	
			4.5			43		54	
			6.0			37		46	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)				62				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 4 : Test Circuit

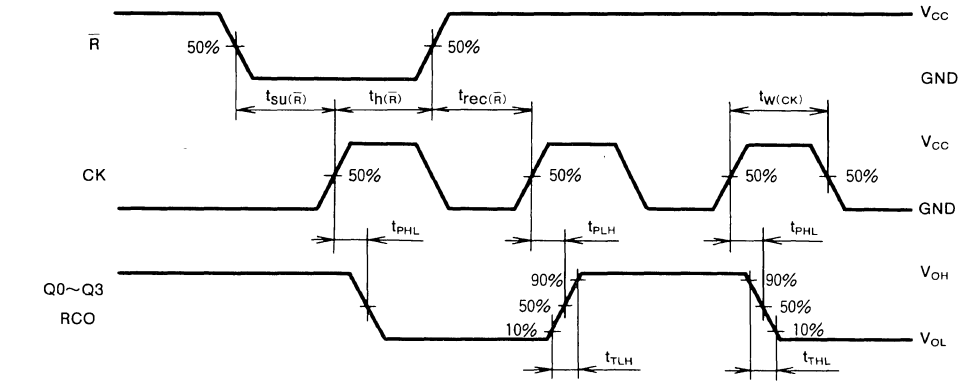


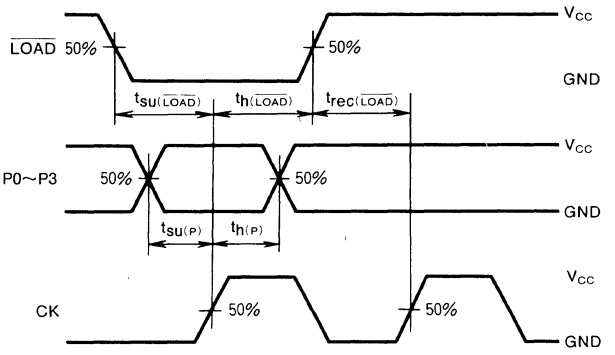
(1) The pulse generator (PG) has the following characteristics (10%~90%). t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

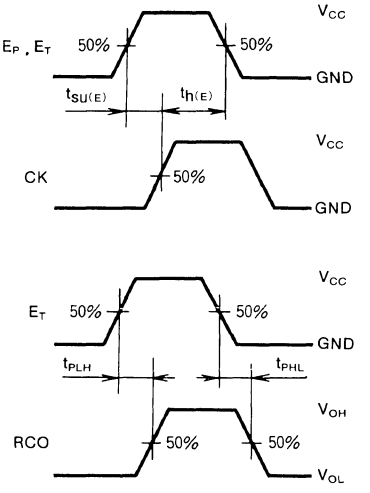
TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
$t_{w(CK)}$	Clock pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
$t_{su(P)}$	P setup time with respect to CK		2.0	150			189		ns
			4.5	30			38		
			6.0	26			32		
$t_{su(\overline{LOAD})}$	$\overline{LOAD}$ setup time with respect to CK		2.0	135			170		ns
			4.5	27			34		
			6.0	23			29		
$t_{su(\overline{R})}$	$\overline{R}$ setup time with respect to CK		2.0	160			202		ns
			4.5	32			40		
			6.0	27			34		
$t_{su(E)}$	E_T, E_P setup time with respect to CK		2.0	200			250		ns
			4.5	40			50		
			6.0	34			43		
$t_{h(P)}$	P hold time with respect to CK		2.0	50			63		ns
			4.5	10			13		
			6.0	9			11		
$t_{h(\overline{LOAD})}$	$\overline{LOAD}$ hold time with respect to CK		2.0	0			0		ns
			4.5	0			0		
			6.0	0			0		
$t_{h(\overline{R})}$	$\overline{R}$ hold time with respect to CK		2.0	0			0		ns
			4.5	0			0		
			6.0	0			0		
$t_{h(E)}$	E_T, E_P hold time with respect to CK		2.0	0			0		ns
			4.5	0			0		
			6.0	0			0		
$t_{rec(\overline{R})}$	$\overline{R}$ recovery time with respect to CK		2.0	125			158		ns
			4.5	25			32		
			6.0	21			27		
$t_{rec(\overline{LOAD})}$	$\overline{LOAD}$ recovery time with respect to CK		2.0	125			158		ns
			4.5	25			32		
			6.0	21			27		

TIMING DIAGRAM

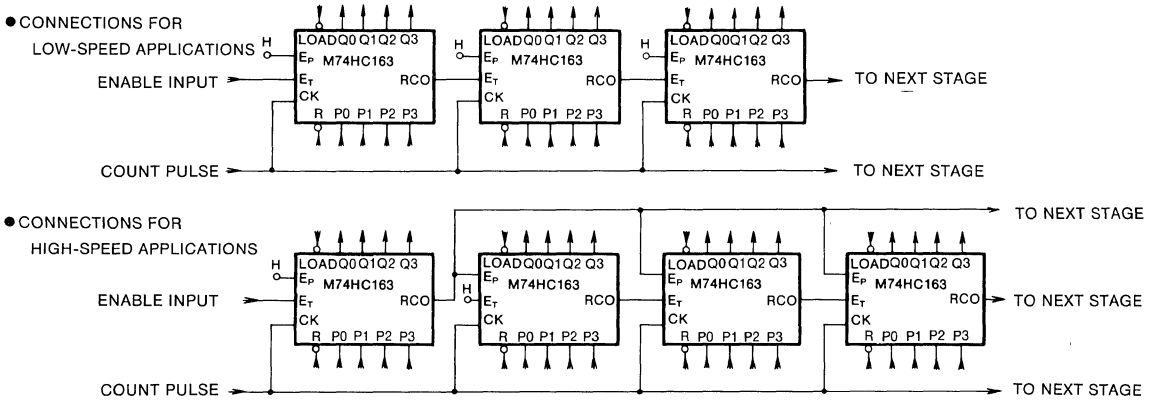






APPLICATION EXAMPLE

10^n COUNTER USING CASCADE CONNECTION



MITSUBISHI ELECTRIC

M74HC164P

8-BIT SERIAL-INPUT PARALLEL-OUTPUT SHIFT REGISTER

DESCRIPTION

The M74HC164 is a semiconductor integrated circuit consisting of an 8-bit serial-input serial/parallel-output shift register with direct reset input.

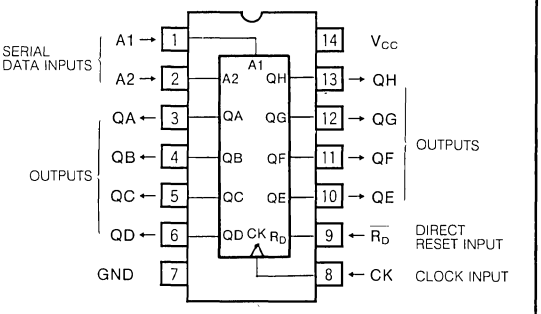
FEATURES

- High-speed (clock frequency) 60MHz typ (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC164 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS164

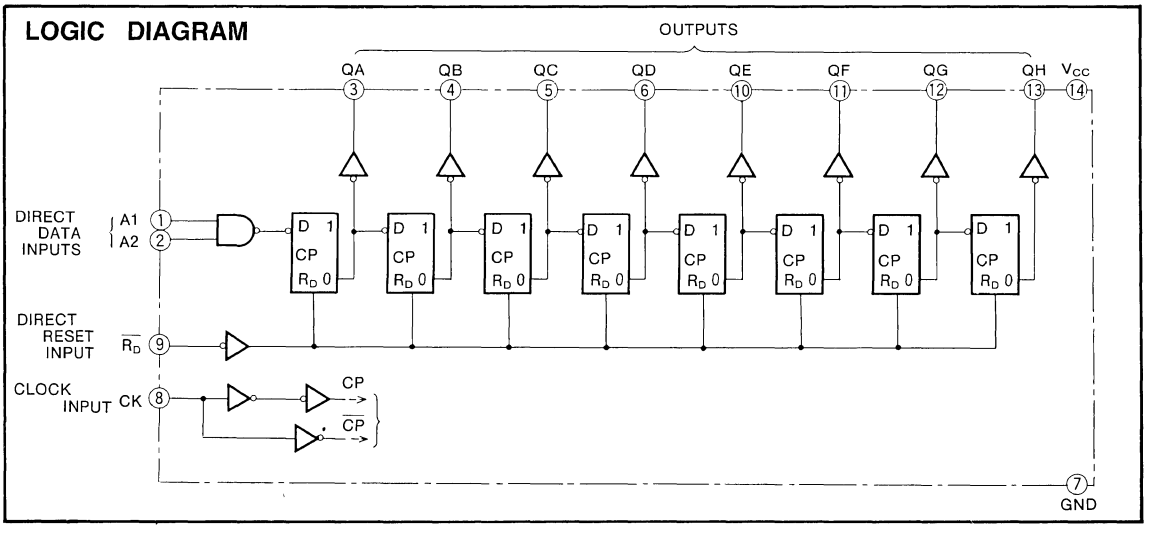
The M74HC164 contains eight edge-triggered D-type flip-flops. The logical product A1 • A2 of the serial data inputs A1 and A2 acts as the input of the shift registers. Outputs QA through QH are taken out from the outputs of each flip-flop.

When both A1 and A2 are high, by applying the clock pulse to clock input CK, the high-level signals will be shifted synchronously with the clock pulse in the order of QA-QH.

When at least one of A1 or A2 is low, a low-level signal will be shifted synchronously with the clock pulse. The shift operation will take place when CK changes from low-level to high-level.

When direct reset input $\overline{R_D}$ is low, all outputs will be reset to low-level irrespective of other inputs. When used as a shift register, $\overline{R_D}$ should be maintained at high-level.

LOGIC DIAGRAM

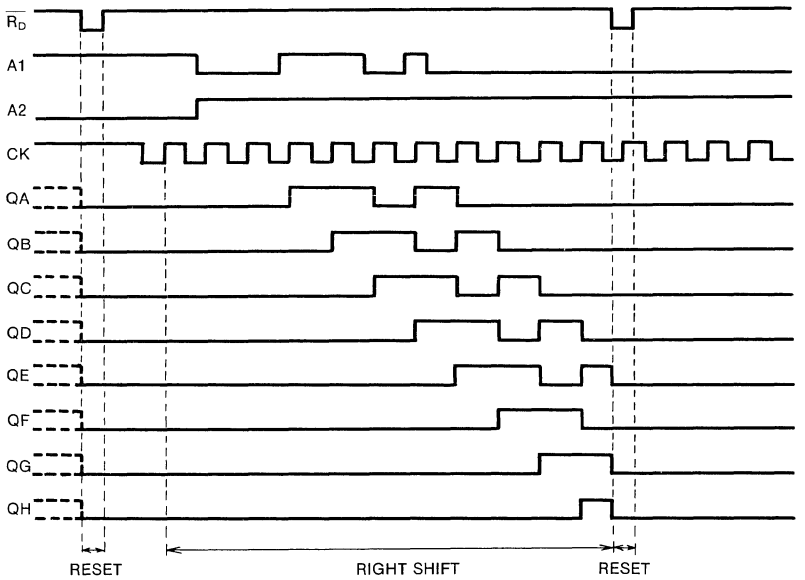


FUNCTION TABLE (Note 1)

Operation mode	Inputs				Outputs							
	$\overline{R_D}$	CK	A1	A2	QA	QB	QC	QD	QE	QF	QG	QH
Reset	L	X	X	X	L	L	L	L	L	L	L	L
Right shift	H	↑	L	L	L	QA^0	QB^0	QC^0	QD^0	QE^0	QF^0	QG^0
	H	↑	H	L	L	QA^0	QB^0	QC^0	QD^0	QE^0	QF^0	QG^0
	H	↑	L	H	L	QA^0	QB^0	QC^0	QD^0	QE^0	QF^0	QG^0
	H	↑	H	H	H	QA^0	QB^0	QC^0	QD^0	QE^0	QF^0	QG^0
No change	H	↓	X	X	QA^0	QB^0	QC^0	QD^0	QE^0	QF^0	QG^0	QH^0

Note 1 : ↑ : Change from low to high level
↓ : Change from high to low level
Q^0 : Output state Q before clock input changed
X : Irrelevant

OPERATION TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation		500	mW
Tstg	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 3)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level output transition time				10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q)				30	ns
t_{PHL}					30	
t_{PHL}	High-level to low-level output propagation time ($\overline{R_D}$ − Q)				35	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

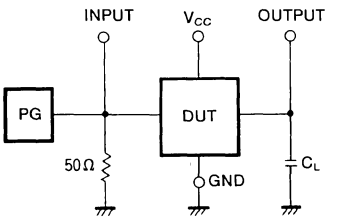
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 3)	2.0	5			4		MHz
			4.5	27			21		
			6.0	31			24		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q)		2.0			175		218	ns
			4.5			35		44	
			6.0			30		38	
t_{PHL}			2.0			175		218	
			4.5			35		44	
			6.0			30		38	
t_{PHL}	High-level to low-level output propagation time ($\overline{R_D}$ − Q)		2.0			205		256	ns
			4.5			41		51	
			6.0			35		44	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				150				pF

Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

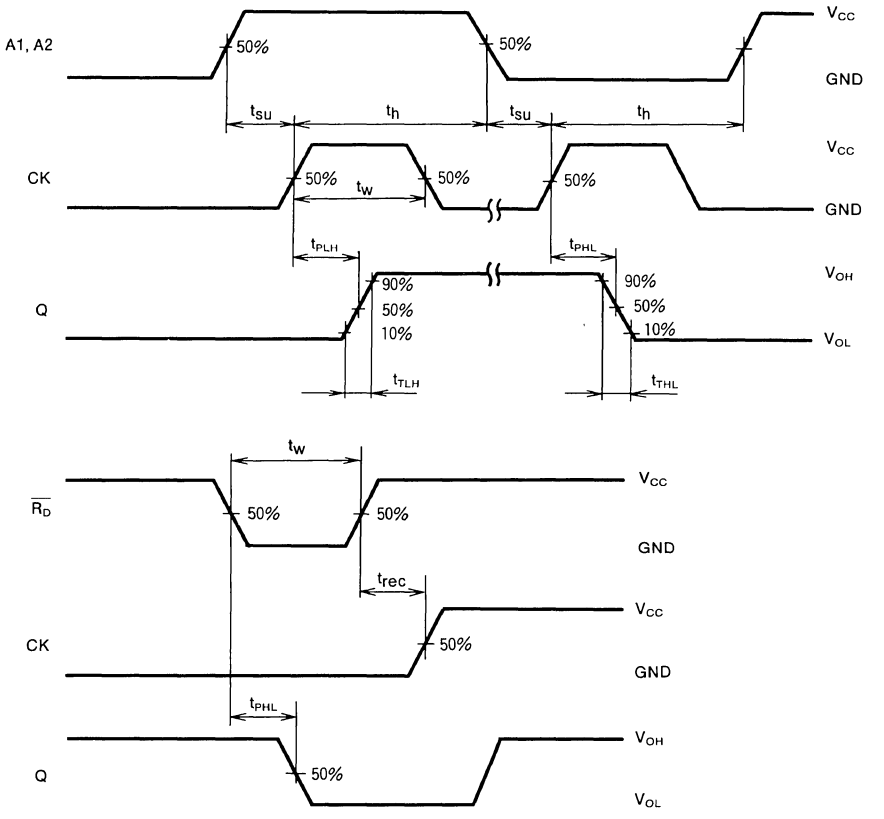
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	CK, $\overline{R_D}$ pulse width		2.0	80			100		ns
			4.5	16			20		
			6.0	14			18		
t_{su}	D setup time with respect to CK		2.0	50			65		ns
			4.5	10			13		
			6.0	9			11		
t_h	D hold time with respect to CK		2.0	5			5		ns
			4.5	5			5		
			6.0	5			5		
t_{rec}	$\overline{R_D}$ recovery time with respect to CK		2.0	5			5		ns
			4.5	5			5		
			6.0	5			5		

Note 3 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM



M74HC174P
M74HC174DP

HEX D-TYPE FLIP-FLOP WITH COMMON CLOCK AND RESET

DESCRIPTION

The M74HC174 is a semiconductor integrated circuit consisting of six positive-edge triggered D-type flip flops with common clock and direct reset inputs, and independent data input.

FEATURES

- High-speed: (clock frequency) 60MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

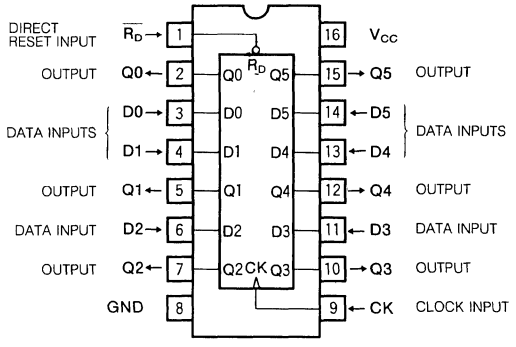
Use of silicon gate technology allows the M74HC174 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS174.

The M74HC174 contains six edge-triggered D-type flip flops, sharing common clock input CK, and direct reset input $\overline{R_D}$.

When CK changes from low-level to high-level, the signals just previously input at D appears at outputs Q in accordance with the function table given.

When $\overline{R_D}$ is low, all the outputs Q will become low irrespective of other inputs. When used as a D-type flip flop, $\overline{R_D}$ should be maintained at high-level.

PIN CONFIGURATION (TOP VIEW)



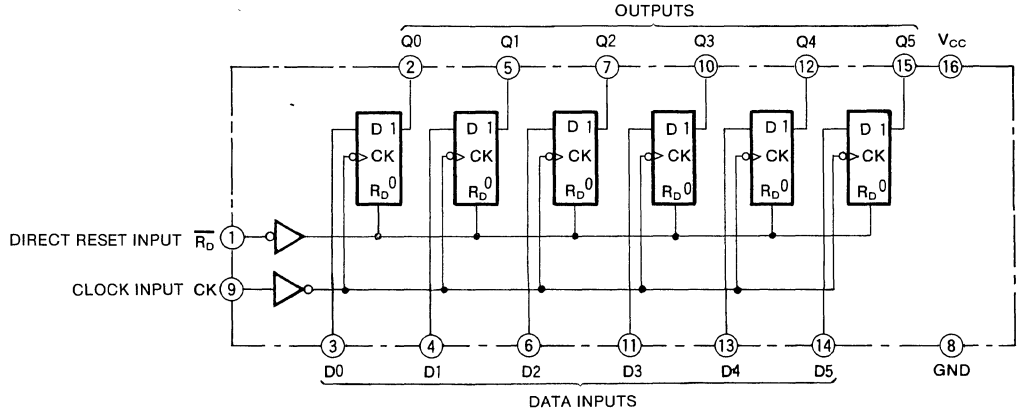
Outline 16P4
16P2P

FUNCTION TABLE (Note 1)

Inputs			Output
$\overline{R_D}$	CK	D	Q
H	↑	H	H
H	↑	L	L
H	↓	X	Q^0
L	X	X	L
H	L	X	Q^0

Note 1 : X : Irrelevant
↑ : Change from low to high level
↓ : Change from high to low level
Q^0 : Output state Q before clock input changed

LOGIC DIAGRAM



MITSUBISHI ELECTRIC

M74HC174P
M74HC174DP

HEX D-TYPE FLIP-FLOP WITH COMMON CLOCK AND RESET

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC174DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		V_{CC}(V)	Limits 25℃ Min	Limits 25℃ Typ	Limits 25℃ Max	Limits −40∼+85℃ Min	Limits −40∼+85℃ Max	Unit
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 4)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level output transition time				10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q)				30	ns
t_{PHL}					30	
t_{PHL}	High-level to low-level output propagation time ($\overline{R_D}$ − Q)				30	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

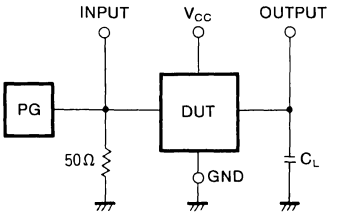
Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40~+85℃		
		V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	2.0	5			4		MHz
			4.5	27			21		
			6.0	31			24		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q)		2.0			165		206	ns
			4.5			33		41	
			6.0			28		35	
t_{PHL}			2.0			165		206	
			4.5			33		41	
			6.0			28		35	
t_{PHL}	High-level to low-level output propagation time ($\overline{R_D}$ − Q)		2.0			165		206	ns
			4.5			33		41	
			6.0			28		35	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)				64				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions
The power dissipated during operation under no-load conditions is calculated using the following formula
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

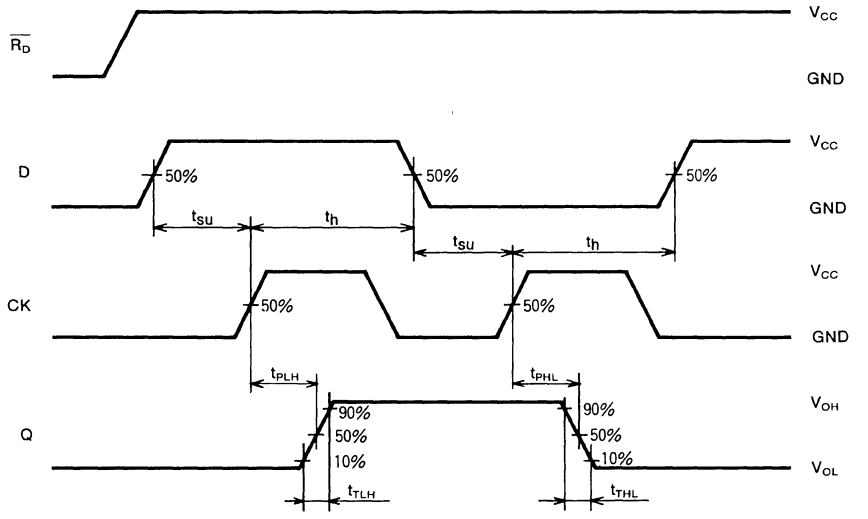
Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40~+85℃		
		V_{CC}(V)	Min	Typ	Max	Min	Max	
$t_{W(CK)}$	Clock pulse width		2.0	80			106		ns
			4.5	16			20		
			6.0	14			18		
$t_{W(\overline{R_D})}$	Direct reset pulse width		2.0	80			106		ns
			4.5	16			20		
			6.0	14			18		
t_{su}	D setup time with respect to CK		2.0	100			125		ns
			4.5	20			25		
			6.0	17			21		
t_h	D hold time with respect to CK		2.0	5			5		ns
			4.5	5			5		
			6.0	5			5		
t_{rec}	$\overline{R_D}$ recovery time with respect to CK		2.0	5			5		ns
			4.5	5			5		
			6.0	5			5		

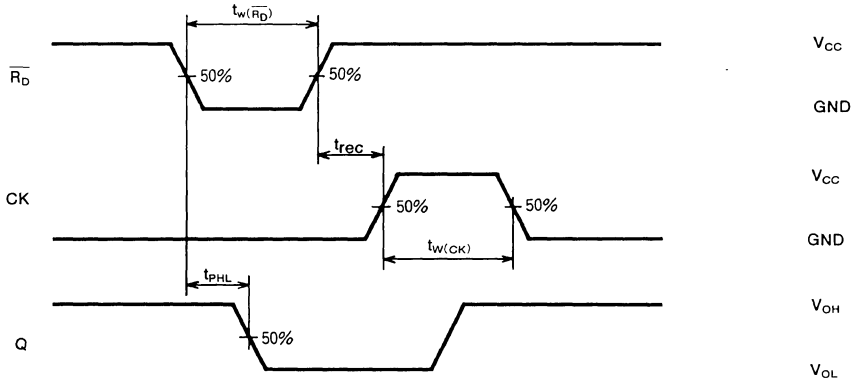
Note 4 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%). t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





M74HC175P
M74HC175DP

QUADRUPLE D-TYPE FLIP-FLOP WITH COMMON CLOCK AND RESET

DESCRIPTION

The M74HC175 is a semiconductor integrated circuit consisting of four positive-edge triggered D-type flip-flops with common clock input and direct reset input.

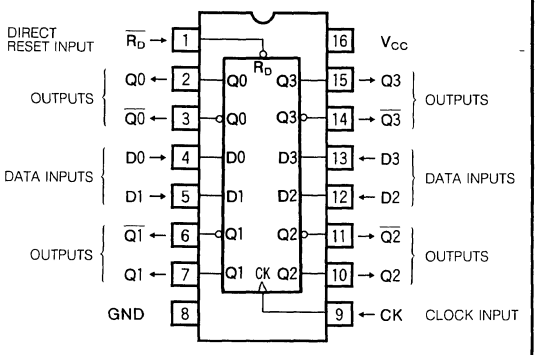
FEATURES

- High-speed: (clock frequency) 60MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4
16P2P

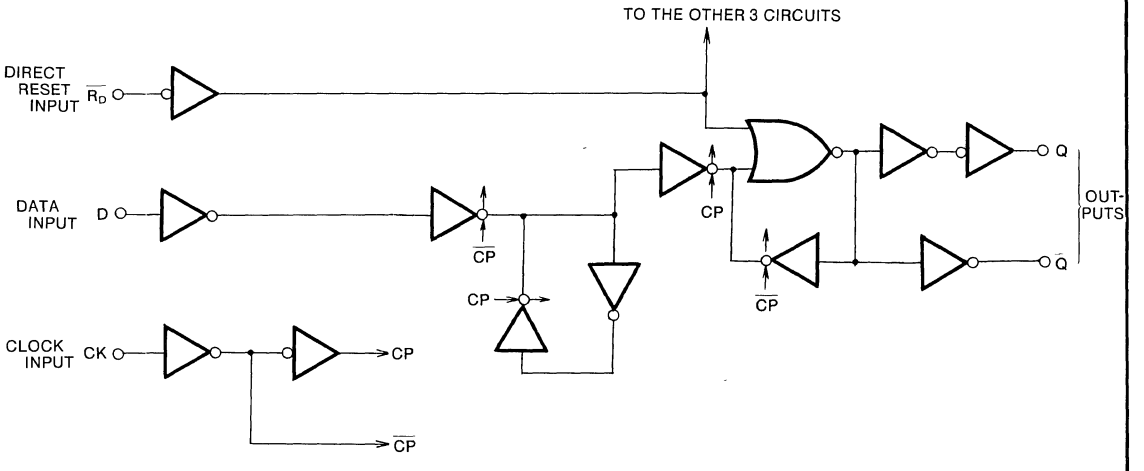
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC175 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS175.

The M74HC175 contains four edgetriggered D-type flip-flops, sharing common clock input CK and direct reset input $\overline{R_D}$.

When CK changes from low-level to high-level, the signals just previously input at D appears at outputs Q and $\overline{Q}$ in accordance with the function table given. When $\overline{R_D}$ is low, Q and $\overline{Q}$ will become low and high, irrespective of other inputs. When used as a D-type flip flop, $\overline{R_D}$ should be maintained at high-level.

LOGIC DIAGRAM (EACH FLIP-FLOP)



MITSUBISHI ELECTRIC

QUADRUPLE D-TYPE FLIP-FLOP WITH COMMON CLOCK AND RESET

FUNCTION TABLE (Note 1)

Inputs			Outputs	
$\overline{R_D}$	CK	D	Q	$\overline{Q}$
H	↑	H	H	L
H	↑	L	L	H
H	↓	X	Q^0	$\overline{Q^0}$
H	L	X	Q^0	$\overline{Q^0}$
L	X	X	L	H

Note 1 : X : Irrelevant
↑ : Change from low to high level
↓ : Change from high to low level
Q^0 : Output state Q before clock input changed
$\overline{Q^0}$: Output state $\overline{Q}$ before clock input changed

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC175DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits						Unit
				25℃			−40∼+85℃			
			V_{CC}(V)	Min	Typ	Max	Min	Max		
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5			V
			4.5	3.15			3.15			
			6.0	4.2			4.2			
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5		V
			4.5			1.35		1.35		
			6.0			1.8		1.8		
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9			V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 4)	35			MHz
t_{TLH}	Low-level to high-level and high-level to low-level				10	ns
t_{THL}	output transition time				10	
t_{PLH}	Low-level to high-level and high-level to low-level				25	ns
t_{PHL}	output propagation time (CK − Q, $\overline{Q}$)				25	
t_{PLH}	Low-level to high-level and high-level to low-level				20	ns
t_{PHL}	output propagation time ($\overline{R_D}$ − Q, $\overline{Q}$)				20	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

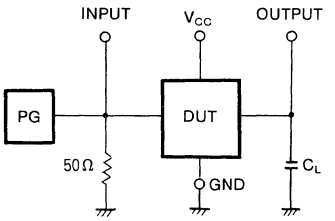
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	2.0	6			5		MHz
			4.5	30			24		
			6.0	35			28		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q, $\overline{Q}$)		2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHL}			2.0			150		189	
			4.5			30		38	
			6.0			26		32	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{R_D}$ − Q, $\overline{Q}$)		2.0			125		158	ns
			4.5			25		32	
			6.0			21		27	
t_{PHL}			2.0			125		158	
			4.5			25		32	
			6.0			21		27	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)				52				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

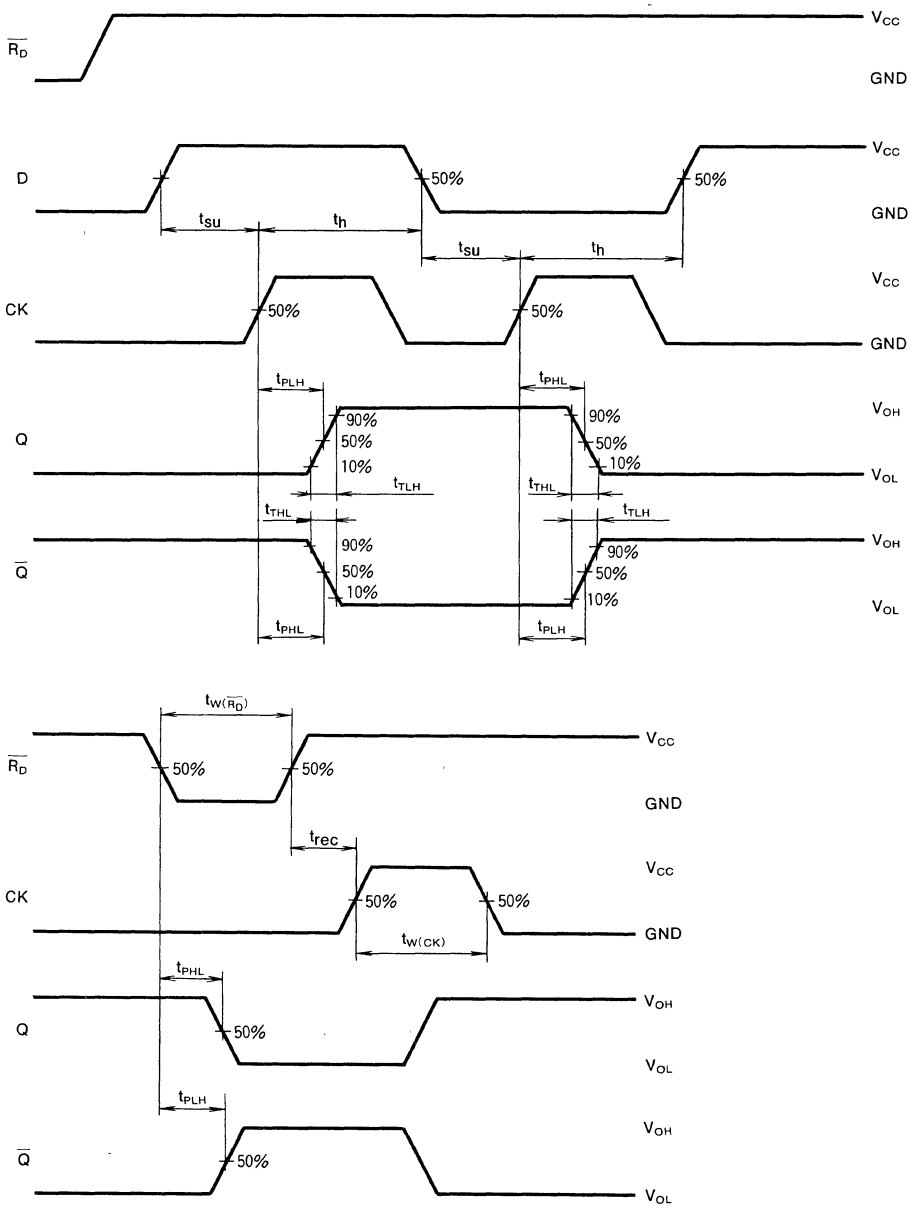
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
$t_{W(CK)}$	Clock pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
$t_{W(\overline{R_D})}$	Direct reset pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
t_{su}	D setup time with respect to CK		2.0	100			126		ns
			4.5	20			25		
			6.0	17			21		
t_h	D hold time with respect to CK		2.0	5			5		ns
			4.5	5			5		
			6.0	5			5		
t_{rec}	$\overline{R_D}$ recovery time with respect to CK		2.0	100			126		ns
			4.5	20			25		
			6.0	17			21		

Note 4 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%). t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



MITSUBISHI ELECTRIC

M74HC237P

1-OF-8 DECODER/DEMULTIPLEXER WITH ADDRESS LATCH

DESCRIPTION

The M74HC237 is a semiconductor integrated circuit consisting of a 3-bit binary to 8-line decoder/demultiplexer with address latch.

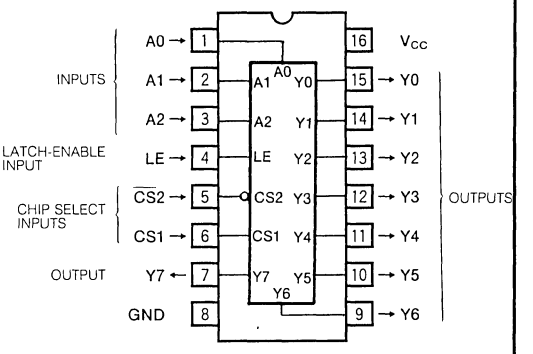
FEATURES

- Built-in address latch
- High-speed: 18ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

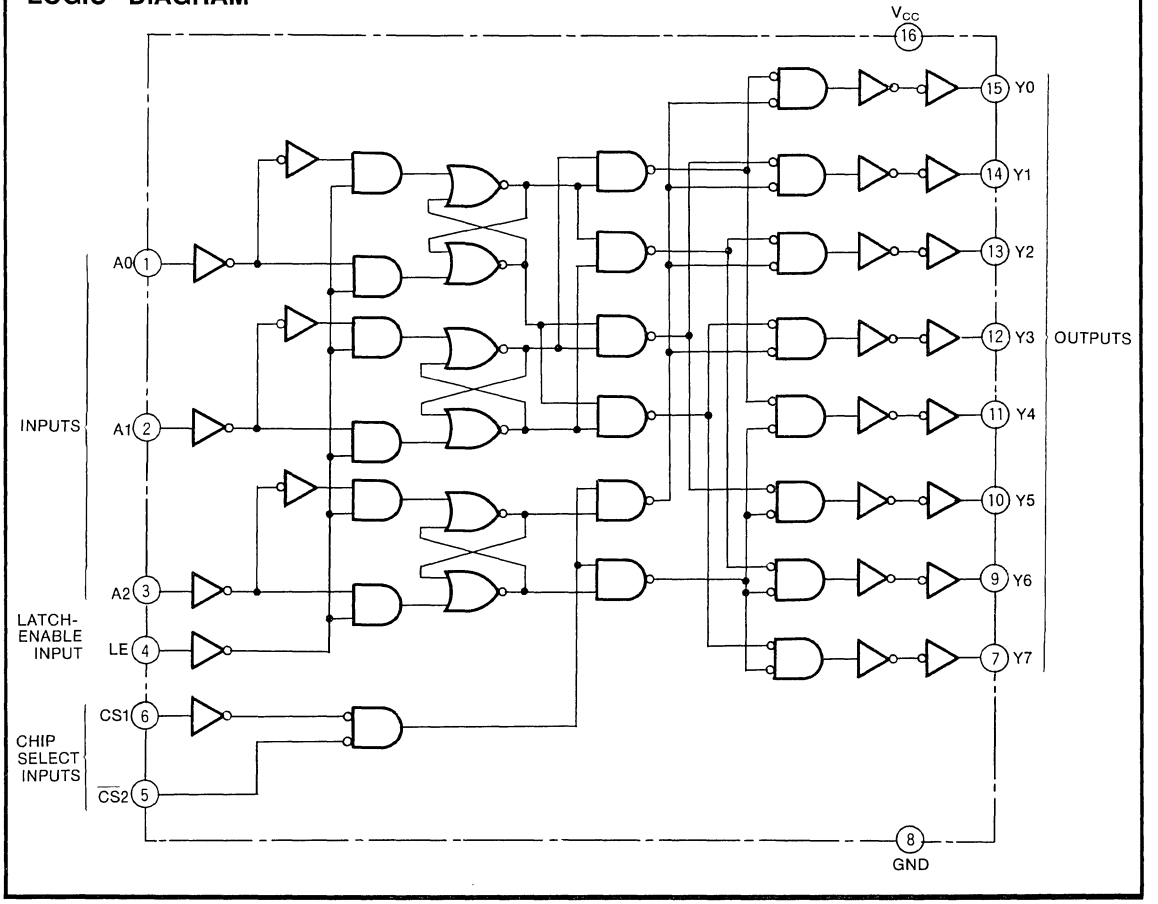
General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC237 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS237.

The M74HC237 consists of a 3-bit binaly to 8-line decoder/demultiplexer with an address latch to store the signals of inputs A0 through A2. When latch-enable input LE is low, a 3-bit binary code is applied to inputs A0 through A2 goes through the latch and becomes a code input signal. In this case, one of outputs Y0 through Y7 corresponding to this value will become high and the other outputs will all become low. When LE is high, the A0 through A2 signals existing immediately prior to the high-level setting will be stored in the latch. In this case, those stored contents will not change even if A0 through A2 are changed.

In this case, chip select inputs CS1 and $\overline{CS2}$ should be maintained at high and low, respectively. When CS1 and $\overline{CS2}$ are in conditions other than those given above, all outputs will become low.

When operated as a 1-of-8 demultiplexer, CS1 or $\overline{CS2}$ is used as a data input and A0 through A2 are used as selecting inputs.

FUNCTION TABLE (Note 1)

Inputs						Outputs							
LE	CS1	$\overline{CS2}$	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	L	L	L	L	L	L	L	L
X	L	X	X	X	X	L	L	L	L	L	L	L	L
L	H	L	L	L	L	H	L	L	L	L	L	L	L
L	H	L	L	L	H	L	H	L	L	L	L	L	L
L	H	L	L	H	L	L	L	H	L	L	L	L	L
L	H	L	L	H	H	L	L	L	H	L	L	L	L
L	H	L	H	L	L	L	L	L	L	H	L	L	L
L	H	L	H	L	H	L	L	L	L	L	H	L	L
L	H	L	H	H	L	L	L	L	L	L	L	H	L
L	H	L	H	H	H	L	L	L	L	L	L	L	H
H	H	L	X	X	X	$Y0^0$	$Y1^0$	$Y2^0$	$Y3^0$	$Y4^0$	$Y5^0$	$Y6^0$	$Y7^0$

Note 1 : X : Irrelevant
Y^0 : Output state Y before LE changed to high level

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation		500	mW
Tstg	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − Y)				41	ns
t_{PHL}					32	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CS2}$ − Y)				35	ns
t_{PHL}					25	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CS1 − Y)				35	ns
t_{PHL}					27	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (LE − Y)				44	ns
t_{PHL}					33	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

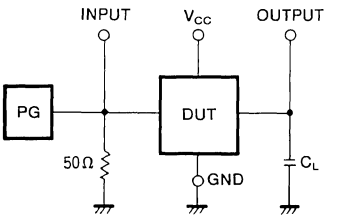
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − Y)		2.0			235		296	ns
			4.5			47		59	
			6.0			40		50	
t_{PHL}			2.0			185		233	
			4.5			37		47	
			6.0			31		40	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CS2}$ − Y)		2.0			200		252	ns
			4.5			40		50	
			6.0			34		43	
t_{PHL}			2.0			145		183	
			4.5			29		37	
			6.0			25		31	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CS1 − Y)		2.0			200		252	ns
			4.5			40		50	
			6.0			34		43	
t_{PHL}			2.0			160		202	
			4.5			32		40	
			6.0			27		34	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (LE − Y)		2.0			250		315	ns
			4.5			50		63	
			6.0			43		54	
t_{PHL}			2.0			190		239	
			4.5			38		48	
			6.0			32		41	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				105				pF

Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions
The power dissipated during operation under no-load conditions is calculated using the following formula.
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

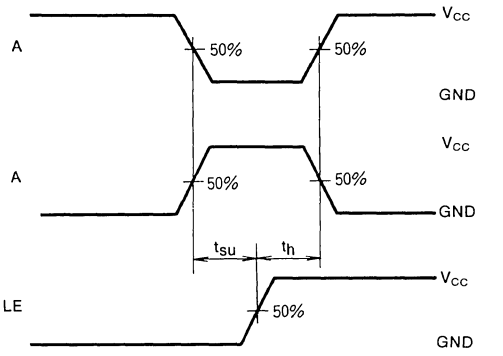
TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	Limits						Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_W	LE pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
t_{su}	A setup time with respect to LE		2.0	100			126		ns
			4.5	20			25		
			6.0	17			21		
t_h	A hold time with respect to LE		2.0	50			63		ns
			4.5	10			13		
			6.0	9			11		

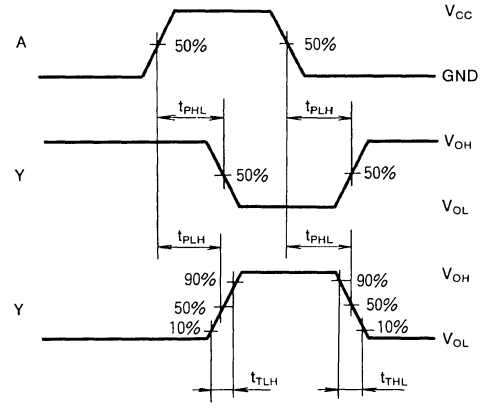
Note 3 : Test Circuit

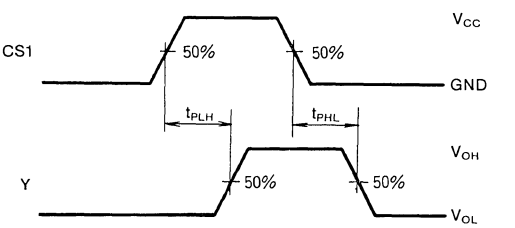


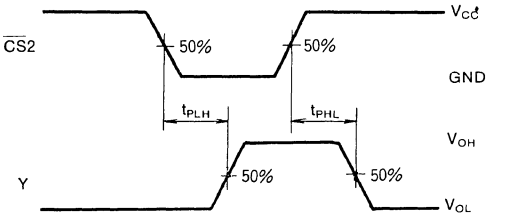
(1) The pulse generator (PG) has the following characteristics (10%~90%) $t_r = 6ns$, $t_f = 6ns$
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

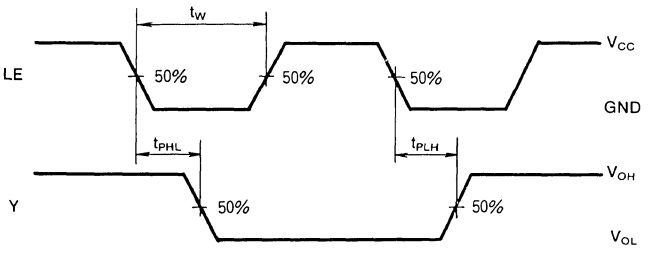


TIMING DIAGRAM









M74HC240P
M74HC240DWP

OCTAL 3-STATE INVERTING BUFFER/LINE DRIVER/LINE RECEIVER

DESCRIPTION

The M74HC240 is a semiconductor integrated circuit consisting of two blocks of 3-state inverting buffers each with four independent circuits that share a common enable input.

FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 10ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC240 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS240.

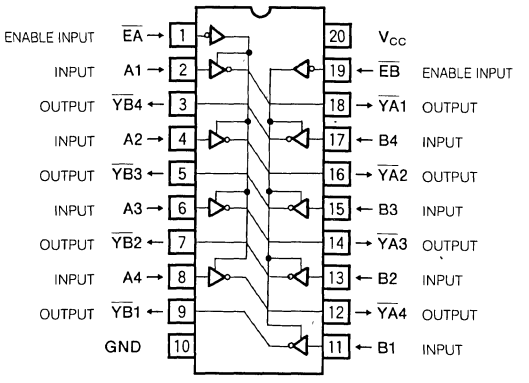
The M74HC240 consists of two independent blocks with each block containing four buffers.

When enable input $\overline{E}$ is low and input A (or B) is low then output $\overline{Y}$ will become high. However, if A (or B) is high then $\overline{Y}$ will become low.

When $\overline{E}$ is high then all outputs within the block will become high-impedance state, irrespective of A (or B).

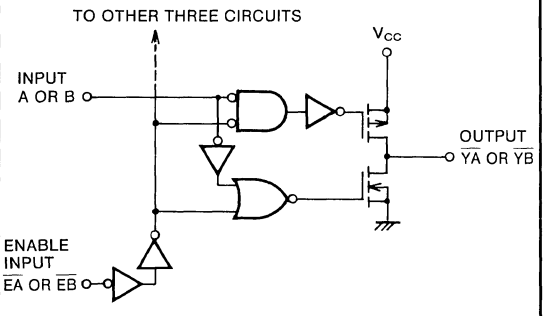
All eight buffer circuits can be controlled simultaneously by connecting $\overline{EA}$ and $\overline{EB}$ of the two blocks.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4
20P2V

LOGIC DIAGRAM (EACH BUFFER)



FUNCTION TABLE (Note 1)

Inputs		Outputs
A, B	$\overline{EA}$, $\overline{EB}$	$\overline{YA}$, $\overline{YB}$
L	L	H
H	L	L
X	H	Z

Note 1 : Z : High impedance
X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 2 : M74HC240DWP, T_a = −40~+80℃ and T_a = 80~85℃ are derated at −7mW/℃

MITSUBISHI ELECTRIC

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V, $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IL}, I_{OH} = −20μA	2.0	1.9			1.9		V
			4.5	4.4			4.4		
			6.0	5.9			5.9		
		I_{OH} = −6.0mA	4.5	4.18			4.13		
		I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}, I_{OL} = 20μA	2.0			0.1		0.1	V
			4.5			0.1		0.1	
			6.0			0.1		0.1	
		I_{OL} = 6.0mA	4.5			0.26		0.33	
		I_{OL} = 7.8mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V	6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V	6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}	6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND	6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA	6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

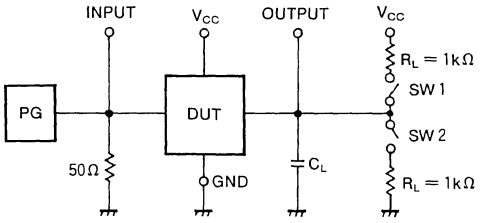
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − $\overline{YA}$, B − $\overline{YB}$)				18	ns
t_{PHL}					18	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{EA}$ − $\overline{YA}$, $\overline{EB}$ − $\overline{YB}$)	C_L = 5 pF (Note 4)			25	ns
t_{PHZ}					25	
t_{PZL}	Output enable time to low-level and high-level ($\overline{EA}$ − $\overline{YA}$, $\overline{EB}$ − $\overline{YB}$)	C_L = 50pF (Note 4)			28	ns
t_{PZH}					28	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − $\overline{YA}$, B − $\overline{YB}$)	C_L = 50pF (Note 4)	2.0			100		126	ns
			4.5			20		25	
			6.0			17		21	
t_{PHL}			2.0			100		126	
			4.5			20		25	
			6.0			17		21	
t_{PLH}		C_L = 150pF (Note 4)	2.0			150		189	
			4.5			30		38	
			6.0			26		32	
t_{PHL}			2.0			150		189	
			4.5			30		38	
			6.0			26		32	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{EA}$ − $\overline{YA}$, $\overline{EB}$ − $\overline{YB}$)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHZ}			2.0			150		189	
			4.5			30		38	
			6.0			26		32	
t_{PZL}	Output enable time to low-level and high-level ($\overline{EA}$ − $\overline{YA}$, $\overline{EB}$ − $\overline{YB}$)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZH}			2.0			150		189	
			4.5			30		38	
			6.0			26		32	
t_{PZL}		C_L = 150pF (Note 4)	2.0			200		252	
			4.5			40		50	
			6.0			34		43	
t_{PZH}			2.0			200		252	
			4.5			40		50	
			6.0			34		43	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{EA}$ = V_{CC}, $\overline{EB}$ = V_{CC}				15		15	
C_{PD}	Power dissipation capacitance (Note 3)				57				

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per buffer)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

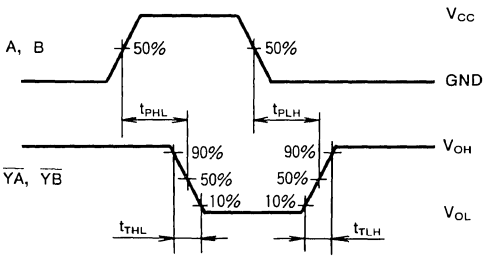
Note 4 : Test Circuit

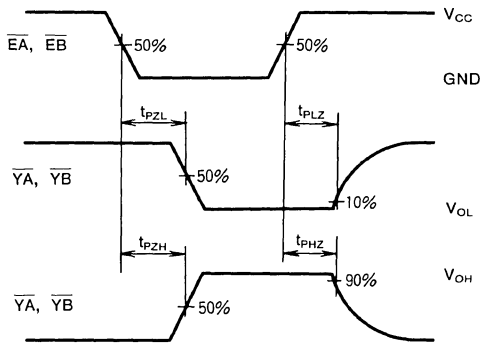


Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

(1) The pulse generator (PG) has the following characteristics (10%~90%) $t_r = 6ns$, $t_f = 6ns$
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM





M74HC241P
M74HC241DWP

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER

DESCRIPTION

The M74HC241 is a semiconductor integrated circuit consisting of two blocks of 3-state non-inverting buffers each with four independent circuits that share a common enable input.

FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 10ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

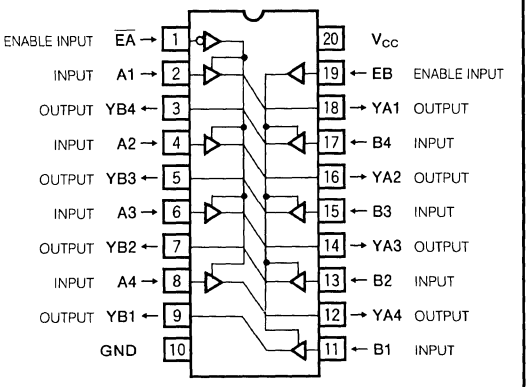
Use of silicon gate technology allows the M74HC241 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS241.

The M74HC241 consists of two independent blocks with each block containing four buffers.

When enable input $\overline{EA}$ is low and input A is low then output YA will become low. However, if A is high then YA will become high. Inverted in the other block, a high enable input EB signal causes operation the same as that just described with input B signal output at YB.

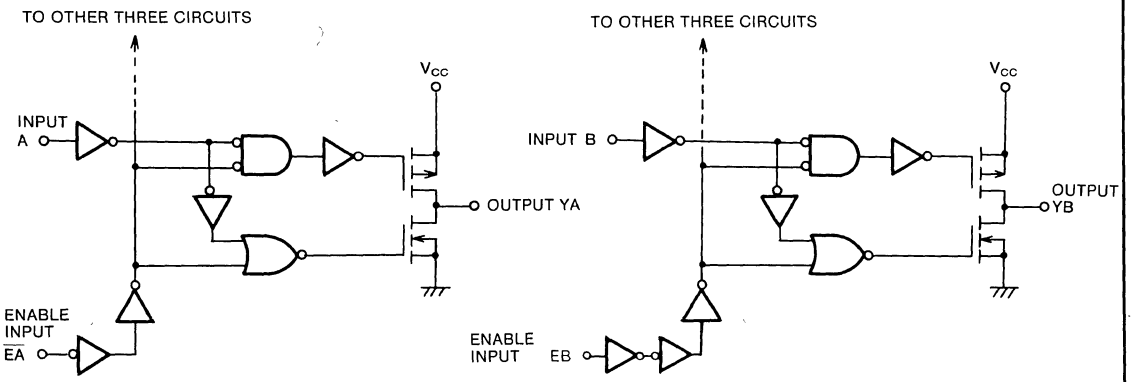
When $\overline{EA}$ is high or EB is low then all Y within the block will become high-impedance state, irrespective of A or B.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4
20P2V

LOGIC DIAGRAM (EACH BUFFER)



MITSUBISHI ELECTRIC

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER

FUNCTION TABLE (Note 1)

Inputs		Output
A	$\overline{EA}$	YA
L	L	L
H	L	H
X	H	Z

Inputs		Output
B	EB	YB
L	H	L
H	H	H
X	L	Z

Note 1 : Z : High impedance
X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC241DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits						Unit
					25℃			−40∼+85℃		
				V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −6.0mA	4.5	4.18			4.13		
			I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 6.0mA	4.5			0.26		0.33	
			I_{OL} = 7.8mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

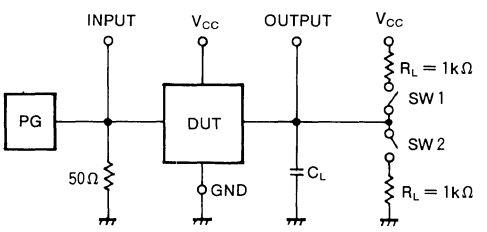
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level	C_L = 50pF (Note 4)			10	ns
t_{THL}	output transition time				10	
t_{PLH}	Low-level to high-level and high-level to low-level				20	ns
t_{PHL}	output propagation time (A − YA, B − YB)				20	
t_{PLZ}	Output disable time from low-level and high-level	C_L = 5 pF (Note 4)			25	ns
t_{PHZ}	($\overline{EA}$ − YA, EB − YB)				25	
t_{PZL}	Output enable time to low-level and high-level	C_L = 50pF (Note 4)			28	ns
t_{PZH}	($\overline{EA}$ − YA, EB − YB)				28	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − YA, B − YB)	C_L = 50pF (Note 4)	2.0			115		145	ns
			4.5			23		29	
			6.0			20		25	
t_{PHL}			2.0			115		145	
			4.5			23		29	
			6.0			20		25	
t_{PLH}		C_L = 150pF (Note 4)	2.0			165		208	
			4.5			33		42	
			6.0			28		35	
t_{PHL}			2.0			165		208	
			4.5			33		42	
			6.0			28		35	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{EA}$ − YA, EB − YB)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHZ}			2.0			150		189	
			4.5			30		38	
			6.0			26		32	
t_{PZL}	Output enable time to low-level and high-level ($\overline{EA}$ − YA, EB − YB)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZH}			2.0			150		189	
			4.5			30		38	
			6.0			26		32	
t_{PZL}		C_L = 150pF (Note 4)	2.0			200		252	
			4.5			40		50	
			6.0			34		43	
t_{PZH}			2.0			200		252	
			4.5			40		50	
			6.0			34		43	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{EA}$ = V_{CC}, EB = GND				15		15	
C_{PD}	Power dissipation capacitance (Note 3)				59				

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per buffer)
The power dissipated during operation under no-load conditions is calculated using the following formula
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

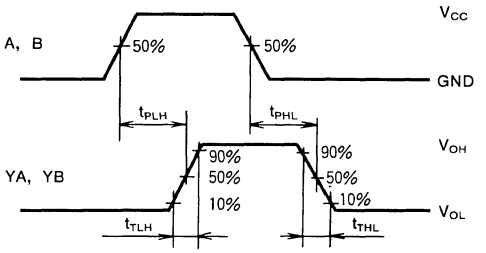
Note 4 : Test Circuit

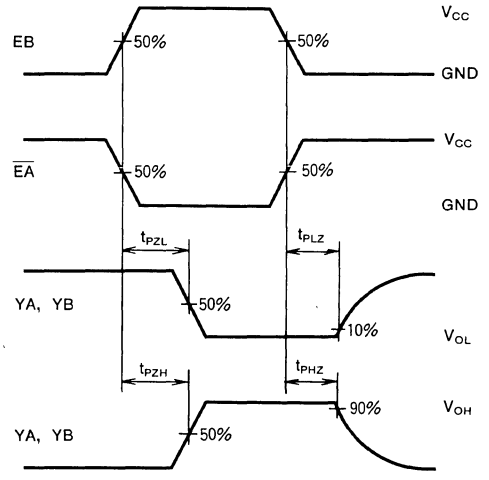


Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Close	Open
t_{PHZ}	Open	Close
t_{PZL}	Close	Open
t_{PZH}	Open	Close

(1) The pulse generator (PG) has the following characteristics (10%~90%): $t_r = 6ns$, $t_f = 6ns$
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM





M74HC242P

QUADRUPLE 3-STATE INVERTING BUS TRANSCEIVER

DESCRIPTION

The M74HC242 is a semiconductor integrated circuit consisting of four transceivers with inverted outputs.

FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 10ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

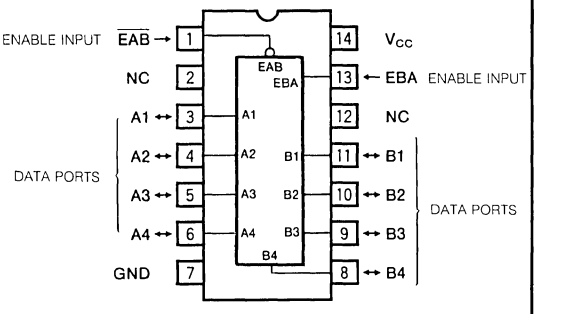
Use of silicon gate technology allows the M74HC242 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS242.

Two buffers with 3-state inverted outputs have their inputs and outputs mutually connected and can be used as buffers in both directions.

The input/output direction is controlled by enable inputs $\overline{EAB}$ and EBA.

When $\overline{EAB}$ and EBA are both low, the data ports A will become input terminals and the data ports B will become output terminals. When $\overline{EAB}$ and EBA are both high, B will become input terminals and A will become output terminals. Whichever the case, the inverted signals of the input terminals will appear at the output terminals. When $\overline{EAB}$ is high and EBA is low or when $\overline{EAB}$ is low and EBA is high, A and B will both become a high-impedance state and they will be separated.

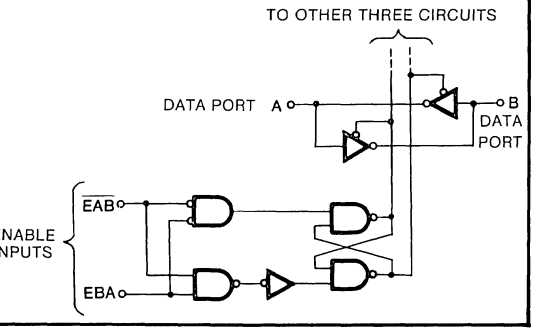
PIN CONFIGURATION (TOP VIEW)



Outline 14P4

NC : NO CONNECTION

LOGIC DIAGRAM (EACH TRANSCEIVER)



FUNCTION TABLE (Note 1)

Inputs		Outputs	
$\overline{EAB}$	EBA	A	B
H	H	$\overline{O}$	I
L	H	Z	Z
H	L	Z	Z
L	L	I	$\overline{O}$

Note 1 : I : Input terminal
$\overline{O}$: Output terminal (inverted output)
Z : High impedance

ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation		500	mW
Tstg	Storage temperature range		−65~+150	℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −6.0mA	4.5	4.18			4.13		
			I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 6.0mA	4.5			0.26		0.33	
			I_{OL} = 7.8mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

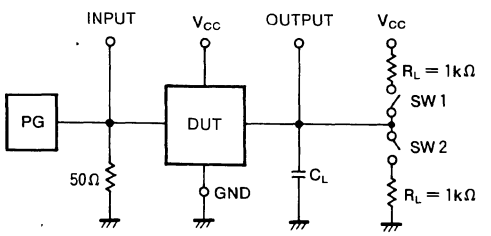
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level	C_L = 50pF (Note 3)			10	ns
t_{THL}	output transition time				10	
t_{PLH}	Low-level to high-level and high-level to low-level				18	ns
t_{PHL}	output propagation time (A − B, B − A)				18	
t_{PLZ}	Output disable time from low-level and high-level	C_L = 5 pF (Note 3)			25	ns
t_{PHZ}	($\overline{EAB}$ − A, B, EBA − B, A)				25	
t_{PZL}	Output enable time to low-level and high-level	C_L = 50pF (Note 3)			28	ns
t_{PZH}	($\overline{EAB}$ − A, B, EBA − B, A)				28	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − B, B − A)	C_L = 50pF (Note 3)	2.0			100		126	ns
			4.5			20		25	
			6.0			17		21	
t_{PHL}			2.0			100		126	
			4.5			20		25	
			6.0			17		21	
t_{PLH}		C_L = 150pF (Note 3)	2.0			150		189	
			4.5			30		38	
			6.0			26		32	
t_{PHL}			2.0			150		189	
			4.5			30		38	
			6.0			26		32	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{EAB}$ − A, B, EBA − B, A)	C_L = 50pF (Note 3)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHZ}			2.0			150		189	
			4.5			30		38	
			6.0			26		32	
t_{PZL}	Output enable time to low-level and high-level ($\overline{EAB}$ − A, B, EBA − B, A)	C_L = 50pF (Note 3)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZH}			2.0			150		189	
			4.5			30		38	
			6.0			26		32	
t_{PZL}		C_L = 150pF (Note 3)	2.0			200		252	
			4.5			40		50	
			6.0			34		43	
t_{PZH}			2.0			200		252	
			4.5			40		50	
			6.0			34		43	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance					15		15	
C_{PD}	Power dissipation capacitance (Note 2)				58				

Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per transceiver)
The power dissipated during operation under no-load conditions is calculated using the following formula
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

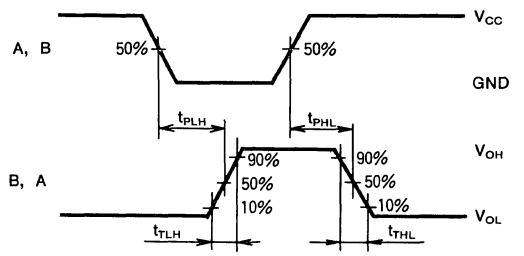
Note 3 : Test Circuit

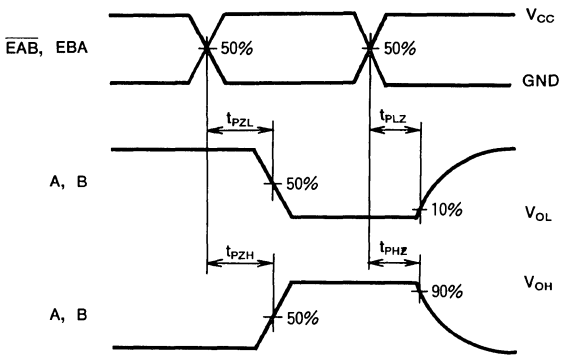


Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

(1) The pulse generator (PG) has the following characteristics (10%~90%) t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM





M74HC243P

QUADRUPLE 3-STATE NONINVERTING BUS TRANSCEIVER

DESCRIPTION

The M74HC243 is a semiconductor integrated circuit consisting of four bus transceivers with noninverted outputs.

FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 12ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

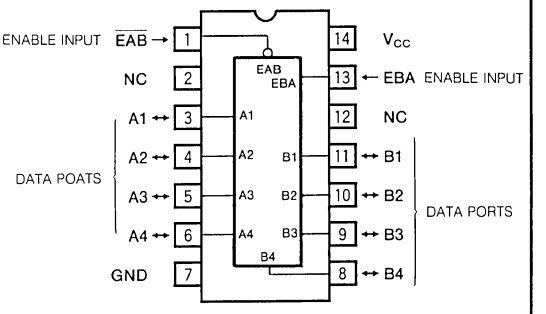
Use of silicon gate technology allows the M74HC243 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS243.

Two buffers with 3-state noninverted outputs have their inputs and outputs mutually connected and can be used as buffers in both directions.

The input/output direction is controlled by enable inputs $\overline{EAB}$ and EBA.

When $\overline{EAB}$ and EBA are both low, the data ports A will become input terminals and the data ports B will become output terminals. When $\overline{EAB}$ and EBA are both high, B will become input terminals and A will become output terminals. Whichever the case, the same signals as at the input terminals will appear at the output terminals. When $\overline{EAB}$ is high and EBA is low or when $\overline{EAB}$ is low and EBA is high, A and B will both become a high-impedance state and they will be separated.

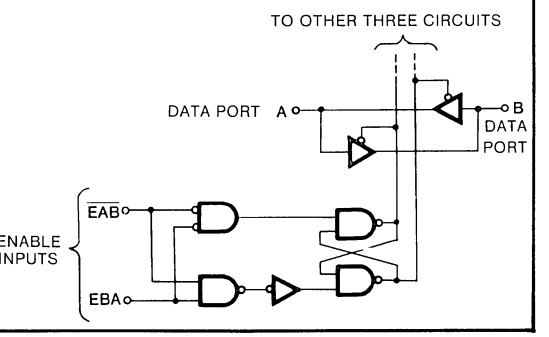
PIN CONFIGURATION (TOP VIEW)



Outline 14P4

NC : NO CONNECTION

LOGIC DIAGRAM (EACH TRANSCEIVER)



FUNCTION TABLE (Note 1)

Inputs		Outputs	
$\overline{EAB}$	EBA	A	B
H	H	O	I
L	H	Z	Z
H	L	Z	Z
L	L	I	O

Note 1 : I : Input terminal
O : Output terminal
Z : High impedance

ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation		500	mW
Tstg	Storage temperature range		−65~+150	℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −6.0mA	4.5	4.18			4.13		
			I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 6.0mA	4.5			0.26		0.33	
			I_{OL} = 7.8mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

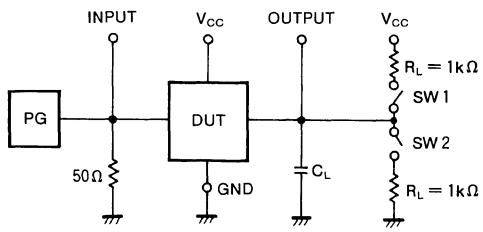
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − B, B − A)				18	ns
t_{PHL}					18	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{EAB}$ − A, B, EBA − B, A)	C_L = 5 pF (Note 3)			25	ns
t_{PHZ}					25	
t_{PZL}	Output enable time to low-level and high-level ($\overline{EAB}$ − A, B, EBA − B, A)	C_L = 50pF (Note 3)			28	ns
t_{PZH}					28	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − B, B − A)	C_L = 50pF (Note 3)	2.0			100		126	ns
			4.5			20		25	
			6.0			17		21	
t_{PHL}			2.0			100		126	
			4.5			20		25	
			6.0			17		21	
t_{PLH}		C_L = 150pF (Note 3)	2.0			150		189	
			4.5			30		38	
			6.0			26		32	
t_{PHL}			2.0			150		189	
			4.5			30		38	
			6.0			26		32	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{EAB}$ − A, B, EBA − B, A)	C_L = 50pF (Note 3)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHZ}			2.0			150		189	
			4.5			30		38	
			6.0			26		32	
t_{PZL}	Output enable time to low-level and high-level ($\overline{EAB}$ − A, B, EBA − B, A)	C_L = 50pF (Note 3)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZH}			2.0			150		189	
			4.5			30		38	
			6.0			26		32	
t_{PZL}		C_L = 150pF (Note 3)	2.0			200		252	
			4.5			40		50	
			6.0			34		43	
t_{PZH}			2.0			200		252	
			4.5			40		50	
			6.0			34		43	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance					15		15	
C_{PD}	Power dissipation capacitance (Note 2)				71				

Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per transceiver)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

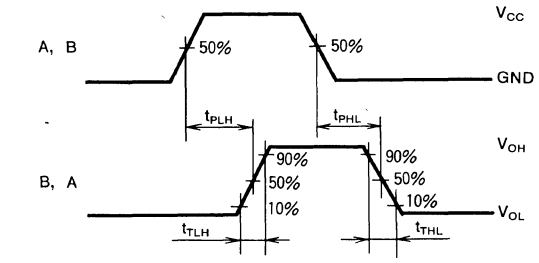
Note 3 : Test Circuit

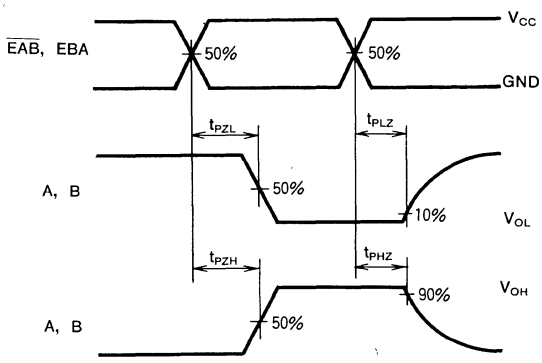


Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

(1) The pulse generator (PG) has the following characteristics (10%~90%) $t_r = 6ns$, $t_f = 6ns$
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM





M74HC244P
M74HC244DWP

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER

DESCRIPTION

The M74HC244 is a semiconductor integrated circuit consisting of two blocks of 3-state non-inverting buffers each with four independent circuits that share a common enable input.

FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 10ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC244 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS244.

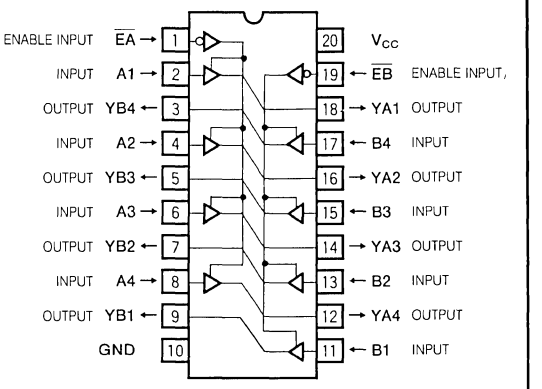
The M74HC244 consists of two independent blocks with each block containing four buffers.

When enable input $\overline{E}$ is low and input A (or B) is low then output Y will become low. However, if A (or B) is high then Y will become high.

When $\overline{E}$ is high then all outputs within the block will become high-impedance state, irrespective of A (or B).

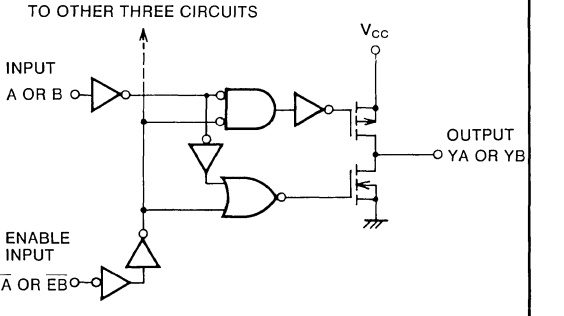
All eight buffer circuits can be controlled simultaneously by connecting $\overline{EA}$ and $\overline{EB}$ of the two blocks.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4
20P2V

LOGIC DIAGRAM (EACH BUFFER)



FUNCTION TABLE (Note 1)

Inputs		Outputs
A, B	$\overline{EA}$, $\overline{EB}$	YA, YB
L	L	L
H	L	H
X	H	Z

Note 1 : Z : High impedance
X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 2 : M74HC244DWP, T_a = −40~+80℃ and T_a = 80~85℃ are derated at −7mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits						Unit
					25℃			−40∼+85℃		
				V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −6.0mA	4.5	4.18			4.13		
			I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 6.0mA	4.5			0.26		0.33	
			I_{OL} = 7.8mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

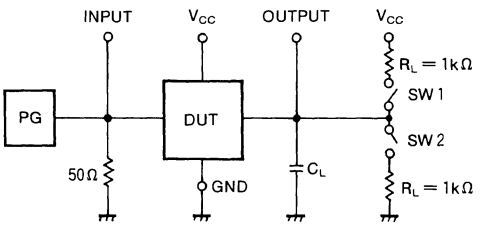
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − YA, B − YB)				20	ns
t_{PHL}					20	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{EA}$ − YA, $\overline{EB}$ − YB)	C_L = 5 pF (Note 4)			25	ns
t_{PHZ}					25	
t_{PZL}	Output enable time to low-level and high-level ($\overline{EA}$ − YA, $\overline{EB}$ − YB)	C_L = 50pF (Note 4)			28	ns
t_{PZH}					28	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − YA, B − YB)	C_L = 50pF (Note 4)	2.0			115		145	ns
			4.5			23		29	
			6.0			20		25	
t_{PHL}			2.0			115		145	
			4.5			23		29	
			6.0			20		25	
t_{PLH}		C_L = 150pF (Note 4)	2.0			165		208	
			4.5			33		42	
			6.0			28		35	
t_{PHL}			2.0			165		208	
			4.5			33		42	
			6.0			28		35	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{EA}$ − YA, $\overline{EB}$ − YB)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHZ}			2.0			150		189	
			4.5			30		38	
			6.0			26		32	
t_{PZL}	Output enable time to low-level and high-level ($\overline{EA}$ − YA, $\overline{EB}$ − YB)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZH}			2.0			150		189	
			4.5			30		38	
			6.0			26		32	
t_{PZL}		C_L = 150pF (Note 4)	2.0			200		252	
			4.5			40		50	
			6.0			34		43	
t_{PZH}			2.0			200		252	
			4.5			40		50	
			6.0			34		43	
C_I	Input capacitance					10		10	pF
C_O	Three-state output capacitance	$\overline{EA}$ = V_{CC}, $\overline{EB}$ = V_{CC}				15		15	
C_{PD}	Power dissipation capacitance (Note 3)				57				

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per buffer)
The power dissipated during operation under no-load conditions is calculated using the following formula
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

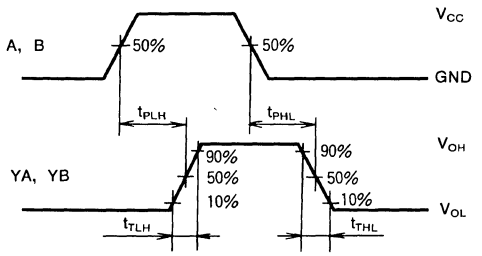
Note 4 : Test Circuit

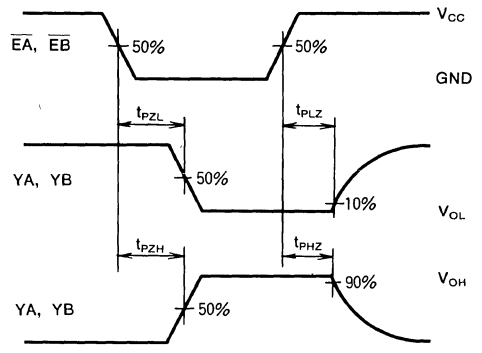


Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Close	Open
t_{PHZ}	Open	Close
t_{PZL}	Close	Open
t_{PZH}	Open	Close

(1) The pulse generator (PG) has the following characteristics (10%~90%): $t_r = 6ns$, $t_f = 6ns$
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM





M74HC251P

8-INPUT DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

DESCRIPTION

The M74HC251 is a semiconductor integrated circuit consisting of an 8-line to 1-line data selector/multiplexer with 3-state outputs.

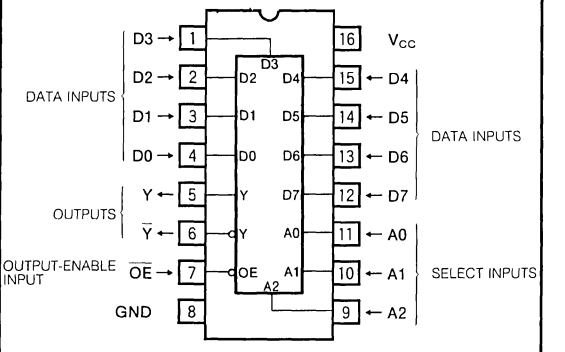
FEATURES

- High-speed: 20ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃
- 3-state outputs

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

FUNCTIONAL DESCRIPTION

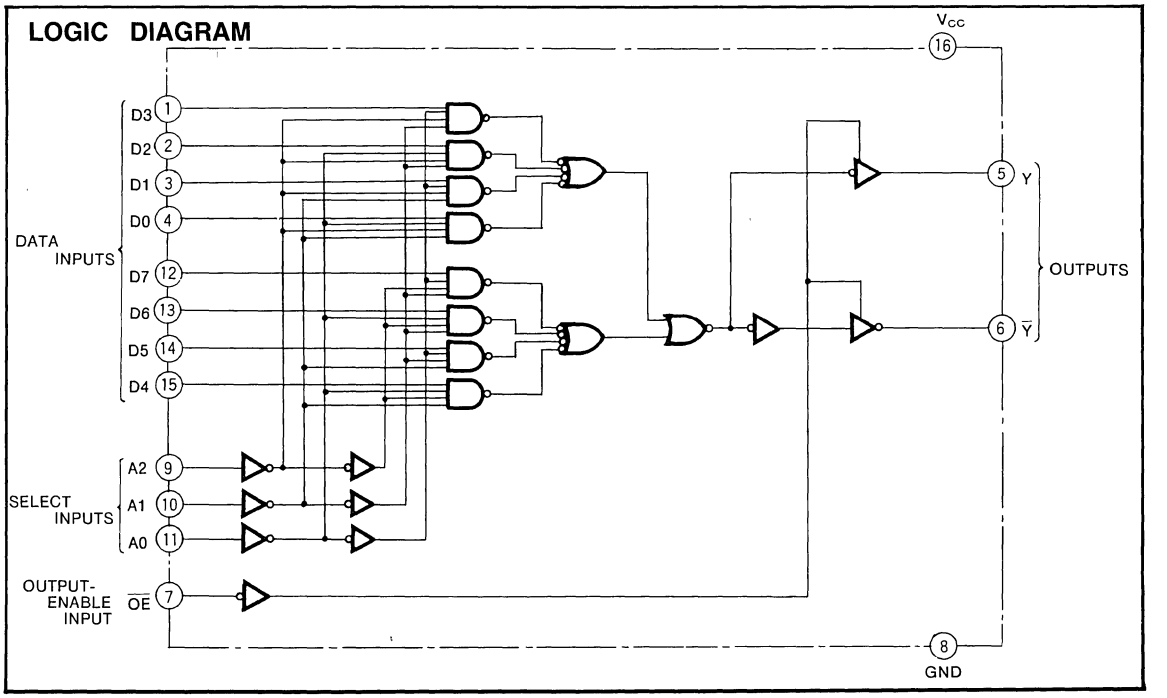
Use of silicon gate technology allows the M74HC251 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS251.

The M74HC251 consists of data selector functions for selecting one of eight input line signals and multiplexer functions for converting 8-bit parallel data into serial data using time-division.

The 8-line signal is applied to data inputs D0 through D7, and after one of the data inputs has been selected by select inputs A0 through A2, that input signal is output at Y or an inverted signal is output at $\overline{Y}$. By applying 8-bit parallel data to D0 through D7, and connecting the output of a synchronous octal counter to A0 through A2, D0 through D7 data will be output at Y synchronous with the clock pulse in the order of D0 - D7. When output-enable input $\overline{OE}$ is high, all outputs will become a high-impedance state irrespective of other inputs.

M74HC251 has the same functions and pin connections as the M74HC151, but the former has a 3-state output.

LOGIC DIAGRAM



FUNCTION TABLE (Note 1)

Inputs												Outputs	
A2	A1	A0	$\overline{OE}$	D0	D1	D2	D3	D4	D5	D6	D7	Y	$\overline{Y}$
X	X	X	H	X	X	X	X	X	X	X	X	Z	Z
L	L	L	L	L	X	X	X	X	X	X	X	L	H
L	L	L	L	H	X	X	X	X	X	X	X	H	L
L	L	H	L	X	L	X	X	X	X	X	X	L	H
L	L	H	L	X	H	X	X	X	X	X	X	H	L
L	H	L	L	X	X	L	X	X	X	X	X	L	H
L	H	L	L	X	X	H	X	X	X	X	X	H	L
L	H	H	L	X	X	X	L	X	X	X	X	L	H
L	H	H	L	X	X	X	H	X	X	X	X	H	L
H	L	L	L	X	X	X	X	L	X	X	X	L	H
H	L	L	L	X	X	X	X	H	X	X	X	H	L
H	L	H	L	X	X	X	X	X	L	X	X	L	H
H	L	H	L	X	X	X	X	X	H	X	X	H	L
H	H	L	L	X	X	X	X	X	X	L	X	L	H
H	H	L	L	X	X	X	X	X	X	H	X	H	L
H	H	H	L	X	X	X	X	X	X	X	L	L	H
H	H	H	L	X	X	X	X	X	X	X	H	H	L

Note 1 : X : Irrelevant
Z : High impedance

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation		500	mW
Tstg	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

MITSUBISHI ELECTRIC

8-INPUT DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level	C_L = 15pF (Note 3)			10	ns
t_{THL}	output transition time				10	
t_{PLH}	Low-level to high-level and high-level to low-level				29	ns
t_{PHL}	output propagation time (D − Y)				29	
t_{PLH}	Low-level to high-level and high-level to low-level				32	ns
t_{PHL}	output propagation time (D − $\overline{Y}$)				32	
t_{PLH}	Low-level to high-level and high-level to low-level				35	ns
t_{PHL}	output propagation time (A − Y)				35	
t_{PLH}	Low-level to high-level and high-level to low-level				35	ns
t_{PHL}	output propagation time (A − $\overline{Y}$)				35	
t_{PLZ}	Output disable time from low-level and high-level	C_L = 5 pF (Note 3)			35	ns
t_{PHZ}	($\overline{OE}$ − Y)				35	
t_{PZL}	Output enable time to low-level and high-level	C_L = 15pF (Note 3)			26	ns
t_{PZH}	($\overline{OE}$ − Y)				26	
t_{PLZ}	Output disable time from low-level and high-level	C_L = 5 pF (Note 3)			40	ns
t_{PHZ}	($\overline{OE}$ − $\overline{Y}$)				40	
t_{PZL}	Output enable time to low-level and high-level	C_L = 15pF (Note 3)			27	ns
t_{PZH}	($\overline{OE}$ − $\overline{Y}$)				27	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

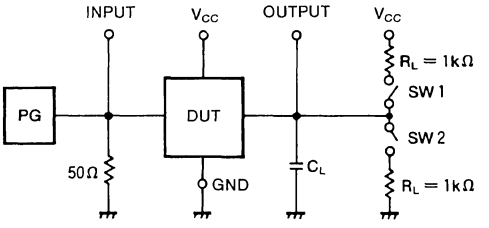
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (D − Y)		2.0			195		244	ns
			4.5			39		49	
			6.0			33		41	
t_{PHL}			2.0			195		244	
			4.5			39		49	
			6.0			33		41	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (D − $\overline{Y}$)		2.0			185		231	ns
			4.5			37		46	
			6.0			32		40	
t_{PHL}			2.0			185		231	
			4.5			37		46	
			6.0			32		40	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − Y)		2.0			205		256	ns
			4.5			41		51	
			6.0			35		44	
t_{PHL}			2.0			205		256	
			4.5			41		51	
			6.0			35		44	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − $\overline{Y}$)		2.0			205		256	ns
			4.5			41		51	
			6.0			35		44	
t_{PHL}			2.0			205		256	
			4.5			41		51	
			6.0			35		44	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − Y)		2.0			195		244	ns
			4.5			39		49	
			6.0			33		41	
t_{PHZ}			2.0			195		244	
			4.5			39		49	
			6.0			33		41	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − Y)		2.0			145		181	ns
			4.5			29		36	
			6.0			25		31	
t_{PZH}			2.0			145		181	
			4.5			29		36	
			6.0			25		31	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − $\overline{Y}$)		2.0			220		275	ns
			4.5			44		55	
			6.0			37		46	
t_{PHZ}			2.0			220		275	
			4.5			44		55	
			6.0			37		46	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{PZL}	Output enable time to high-level and low-level ($\overline{OE}$ − $\overline{Y}$)	C_L = 50pF (Note 3)	2.0			150		188	ns
			4.5			30		38	
			6.0			26		33	
t_{PZH}			2.0			150		188	
			4.5			30		38	
			6.0			26		33	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}				15		15	pF
C_{PD}	Power dissipation capacitance (Note 2)				67				pF

Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions
The power dissipated during operation under no-load conditions is calculated using the following formula
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

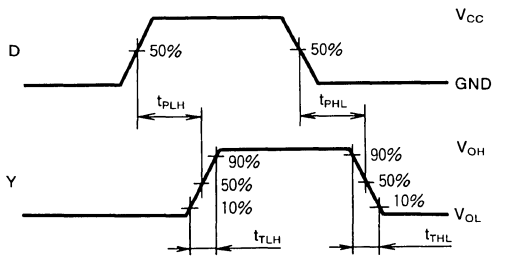
Note 3 : Test Circuit

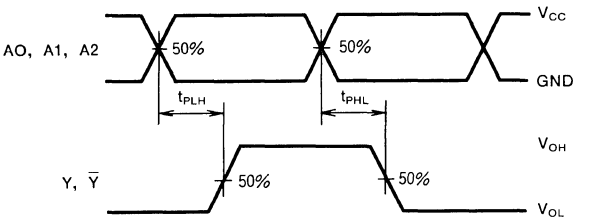


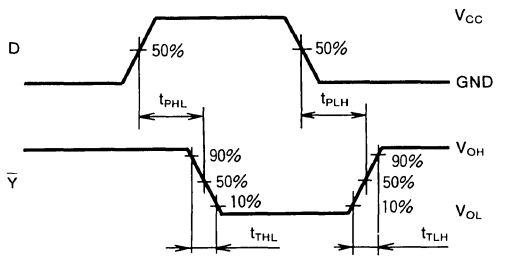
Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

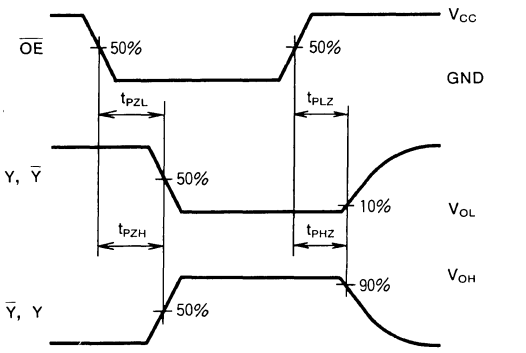
(1) The pulse generator (PG) has the following characteristics (10%~90%) t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM









PRELIMINARY
Notice This is not a final specification Some parametric limits are Subject to change

MITSUBISHI HIGH SPEED CMOS

M74HC257P

QUADRUPLE 2-INPUT DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

DESCRIPTION

The M74HC257 is a semiconductor integrated circuit consisting of four 2-line to 1-line data selectors/multiplexrs with 3-state outputs.

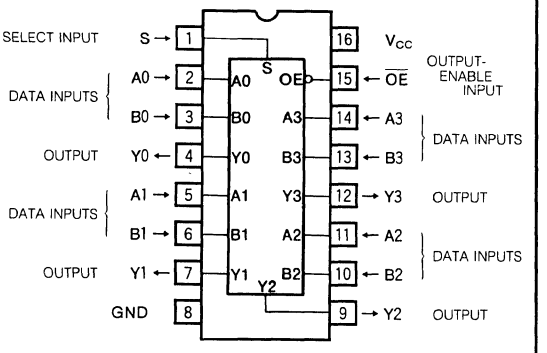
FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 12ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

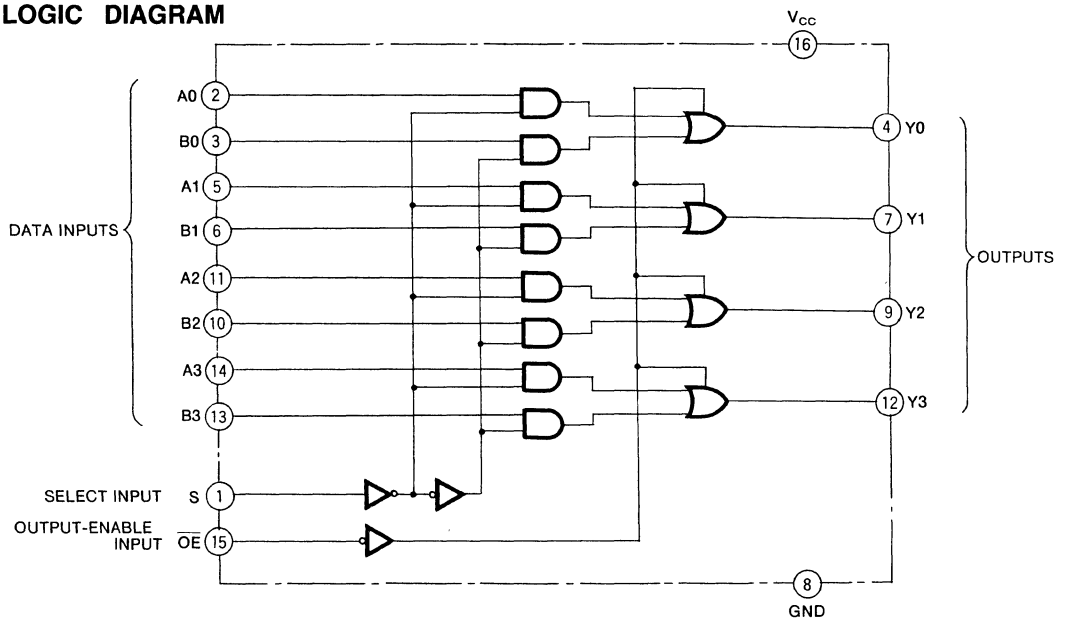
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC257 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS257.

The M74HC257 consists of four circuits each containing data selector functions for selecting one of two input line signals and multiplexer functions for converting 2-bit parallel data into serial data using time-division.

The 2-line signals are applied to data inputs A and B, and after one of the data inputs has been selected by select input S, it is output at pin Y. By applying 2-bit parallel data to A and B, and connecting the output of a binary counter to S, A and B data will be output at Y synchronous with the clock pulse in the order A → B. Both S and output-enable input $\overline{OE}$ are common to all four circuits. When $\overline{OE}$ is high, all outputs will become a high-impedance state irrespective of other inputs.

LOGIC DIAGRAM



MITSUBISHI ELECTRIC

QUADRUPLE 2-INPUT DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

FUNCTION TABLE (Note 1)

Inputs				Output
$\overline{OE}$	S	A	B	Y
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

Note 1 : X : Irrelevant
Z : High impedance

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation		500	mW
Tstg	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

QUADRUPLE 2-INPUT DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −6.0mA	4.5	4.18			4.13		
			I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 6.0mA	4.5			0.26		0.33	
			I_{OL} = 7.8mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A, B − Y)				18	ns
t_{PHL}					18	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (S − Y)				18	ns
t_{PHL}					18	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − Y)	C_L = 5 pF (Note 3)			25	ns
t_{PHZ}					25	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − Y)	C_L = 50pF (Note 3)			28	ns
t_{PZH}					28	

QUADRUPLE 2-INPUT DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

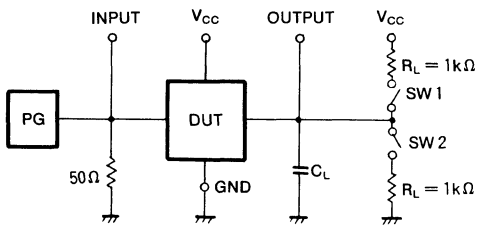
SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A, B − Y)	C_L = 50pF (Note 3)	2.0			100		126	ns
			4.5			20		25	
			6.0			17		21	
t_{PHL}			2.0			100		126	
			4.5			20		25	
			6.0			17		21	
t_{PLH}		C_L = 150pF (Note 3)	2.0			150		189	
			4.5			30		38	
			6.0			26		32	
t_{PHL}			2.0			150		189	
			4.5			30		38	
			6.0			26		32	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (S − Y)	C_L = 50pF (Note 3)	2.0			100		126	ns
			4.5			20		25	
			6.0			17		21	
t_{PHL}			2.0			100		126	
			4.5			20		25	
			6.0			17		21	
t_{PLH}		C_L = 150pF (Note 3)	2.0			150		189	
			4.5			30		38	
			6.0			26		32	
t_{PHL}			2.0			150		189	
			4.5			30		38	
			6.0			26		32	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − Y)	C_L = 50pF (Note 3)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHZ}			2.0			150		189	
			4.5			30		38	
			6.0			26		32	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − Y)	C_L = 50pF (Note 3)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZH}			2.0			150		189	
			4.5			30		38	
			6.0			26		32	
t_{PZL}		C_L = 150pF (Note 3)	2.0			200		252	
			4.5			40		50	
			6.0			34		43	
t_{PZH}			2.0			200		252	
			4.5			40		50	
			6.0			34		43	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}				15		15	
C_{PD}	Power dissipation capacitance (Note 2)								

Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

QUADRUPLE 2-INPUT DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

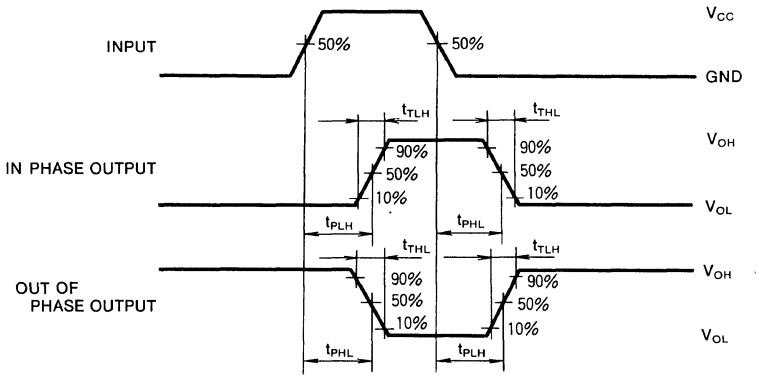
Note 3 : Test Circuit

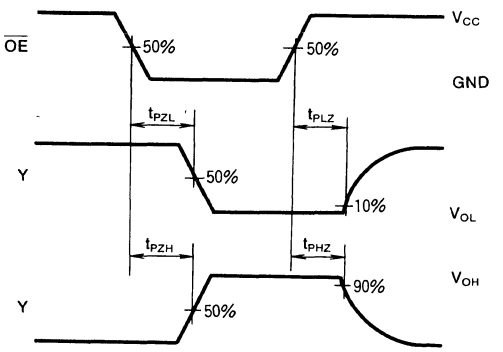


Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

(1) The pulse generator (PG) has the following characteristics (10%~90%). t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM





MITSUBISHI ELECTRIC

M74HC266P

QUADRUPLE 2-INPUT EXCLUSIVE NOR GATE

DESCRIPTION

The M74HC266 is a semiconductor integrated circuit consisting of four 2-input exclusive NOR gates.

FEATURES

- High-speed: 9ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

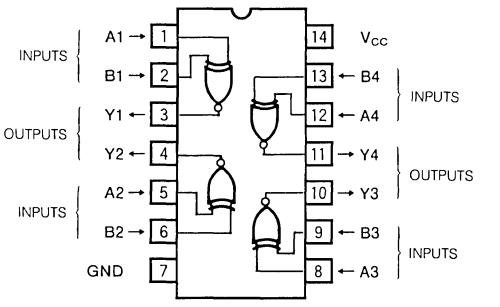
Use of silicon gate technology allows the M74HC266 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS266.

Buffered outputs Y improve input-to-output transfer characteristics and reduce to a minimum output impedance variations with respect to input voltage variations.

When both inputs A and B are either high or low, the output Y will become high, and when the levels of A and B are opposite, the output Y will become low.

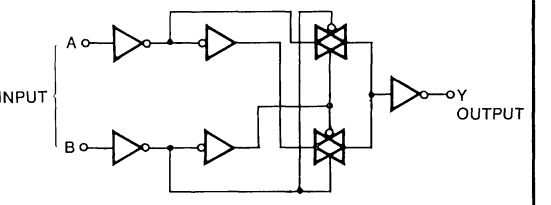
Note that the output of M74HC266 and 74LS266 differ in that the output of the M74HC266 is not open drain.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

LOGIC DIAGRAM (EACH GATE)



FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	H
H	L	L
L	H	L
H	H	H

ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation		500	mW
Tstg	Storage temperature range		−65~+150	℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			1.0		10.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

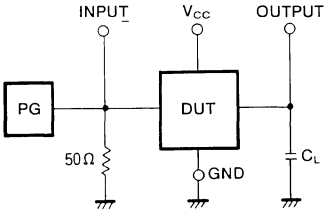
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 2)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time				20	ns
t_{PHL}					20	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 2)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time		2.0			120		151	ns
			4.5			24		30	
			6.0			20		26	
t_{PHL}			2.0			120		151	
			4.5			24		30	
			6.0			20		26	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 1)				38				pF

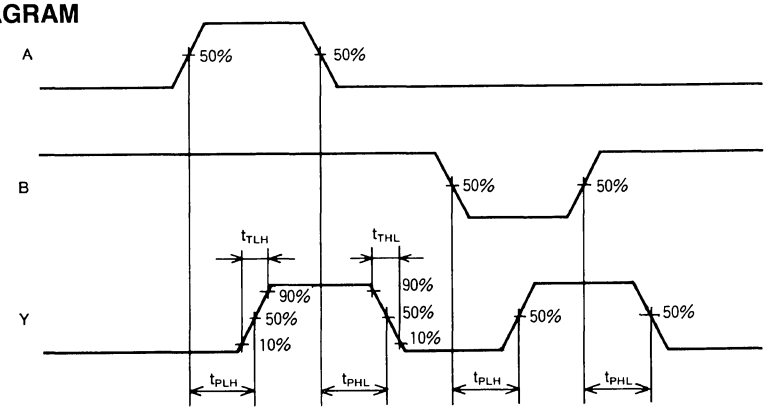
Note 1 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per gate)
The power dissipated during operation under no-load conditions is calculated using the following formula
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 2 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%) · t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM



M74HC273P
M74HC273DWP

OCTAL D-TYPE FLIP-FLOP WITH COMMON CLOCK AND RESET

DESCRIPTION

The M74HC273 is a semiconductor integrated circuit consisting of eight positive-edge triggered D-type flip flops with common clock and direct reset inputs.

FEATURES

- High-speed: (clock frequency) 40MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

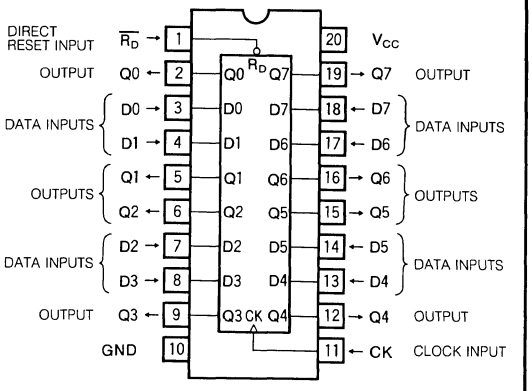
Use of silicon gate technology allows the M74HC273 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS273.

The M74HC273 contains eight edge-triggered D-type flip flops, sharing common clock input CK and direct reset input $\overline{R_D}$.

When CK changes from low-level to high-level, the signals just previously input at D appears at output Q in accordance with the function table given.

When $\overline{R_D}$ is low, all outputs Q will become low, irrespective of the state of other inputs. When used as a D-type flip flop, $\overline{R_D}$ should be maintained at high.

PIN CONFIGURATION (TOP VIEW)



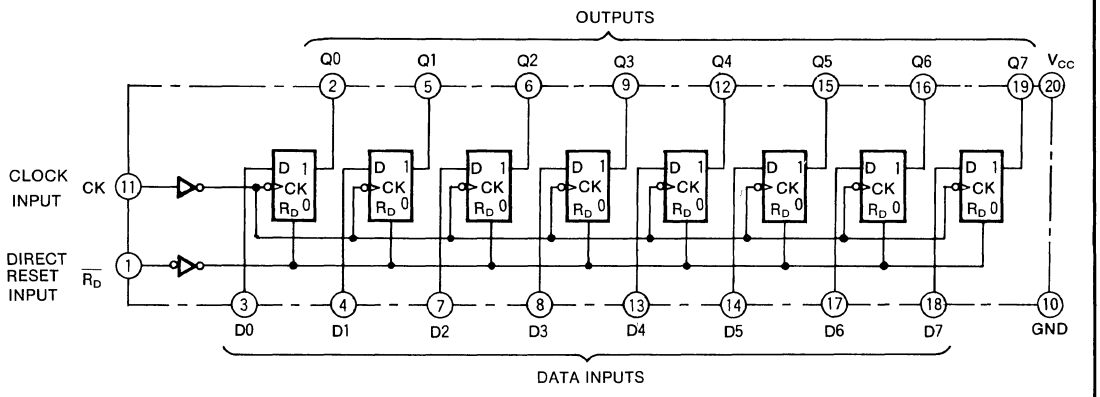
Outline 20P4
20P2V

FUNCTION TABLE (Note 1)

Inputs			Output
$\overline{R_D}$	CK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q^0
H	↓	X	Q^0

Note 1 : ↑ : Change from low to high level
↓ : Change from high to low level
Q^0 : Output state Q before clock input changed
X : Irrelevant

LOGIC DIAGRAM



MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC273DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL} ; I_{OH} = −20μA	2.0	1.9			1.9		V
		V_I = V_{IH}, V_{IL} ; I_{OH} = −20μA	4.5	4.4			4.4		
		V_I = V_{IH}, V_{IL} ; I_{OH} = −20μA	6.0	5.9			5.9		
		V_I = V_{IH}, V_{IL} ; I_{OH} = −4.0mA	4.5	4.18			4.13		
		V_I = V_{IH}, V_{IL} ; I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL} ; I_{OL} = 20μA	2.0			0.1		0.1	V
		V_I = V_{IH}, V_{IL} ; I_{OL} = 20μA	4.5			0.1		0.1	
		V_I = V_{IH}, V_{IL} ; I_{OL} = 20μA	6.0			0.1		0.1	
		V_I = V_{IH}, V_{IL} ; I_{OL} = 4.0mA	4.5			0.26		0.33	
		V_I = V_{IH}, V_{IL} ; I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V	6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V	6.0			−0.1		−1.0	
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA	6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 4)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level output transition time				10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q)				27	ns
t_{PHL}					27	
t_{PHL}	High-level to low-level output propagation time ($\overline{R_D}$ − Q)				27	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

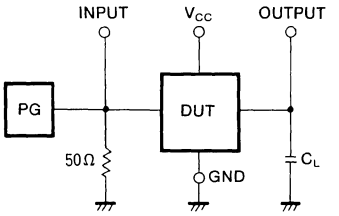
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	2.0	5			4		MHz
			4.5	27			21		
			6.0	32			25		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q)		2.0			160		202	ns
			4.5			32		40	
			6.0			27		34	
t_{PHL}			2.0			160		202	
			4.5			32		40	
			6.0			27		34	
t_{PHL}	High-level to low-level output propagation time ($\overline{R_D}$ − Q)		2.0			160		202	ns
			4.5			32		40	
			6.0			27		34	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)				65				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per flip frop)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

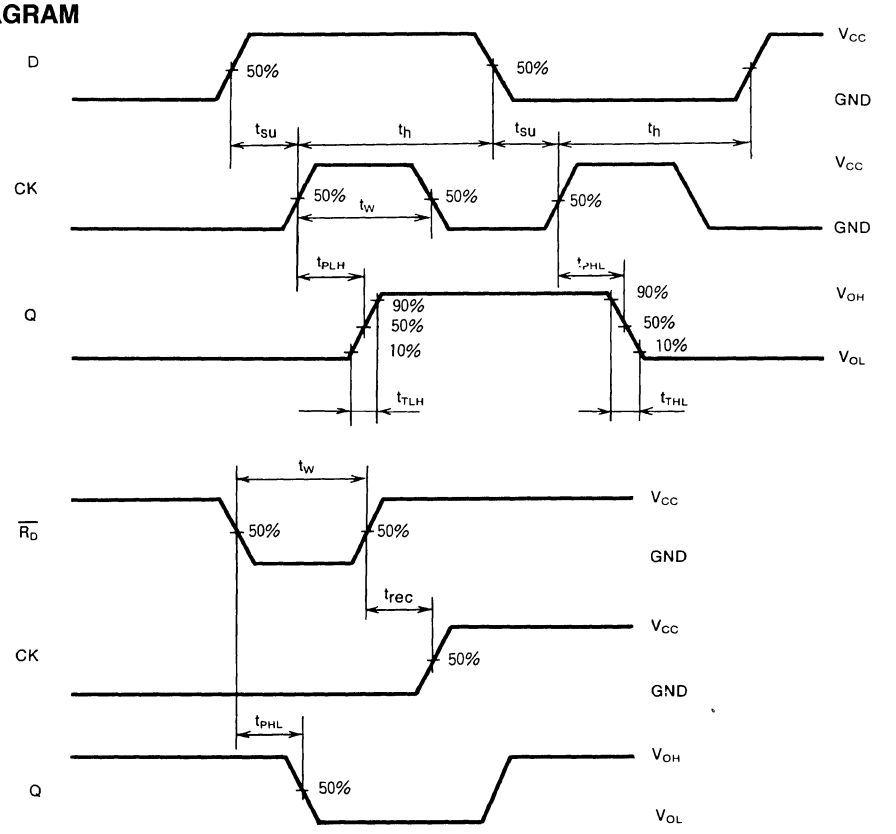
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	CK, $\overline{R_D}$ pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
t_{su}	D setup time with respect to CK		2.0	100			126		ns
			4.5	20			25		
			6.0	17			21		
t_h	D hold time with respect to CK		2.0	0			0		ns
			4.5	0			0		
			6.0	0			0		
t_{rec}	$\overline{R_D}$ recovery time with respect to CK		2.0	100			126		ns
			4.5	20			25		
			6.0	17			21		

Note 4 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM



M74HC280P

9-BIT ODD/EVEN PARITY GENERATOR/CHECKER

DESCRIPTION

The M74HC280 is a semiconductor integrated circuit consisting of a 9-bit parity generator/checker.

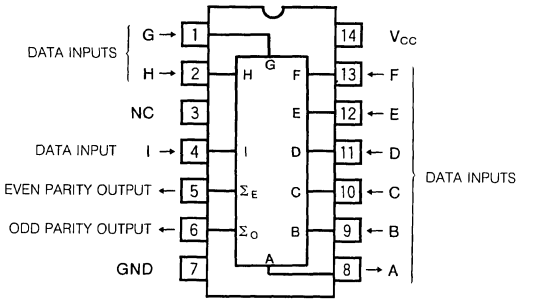
FEATURES

- High-speed: 20ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

NC : NO CONNECTION

FUNCTIONAL DESCRIPTION

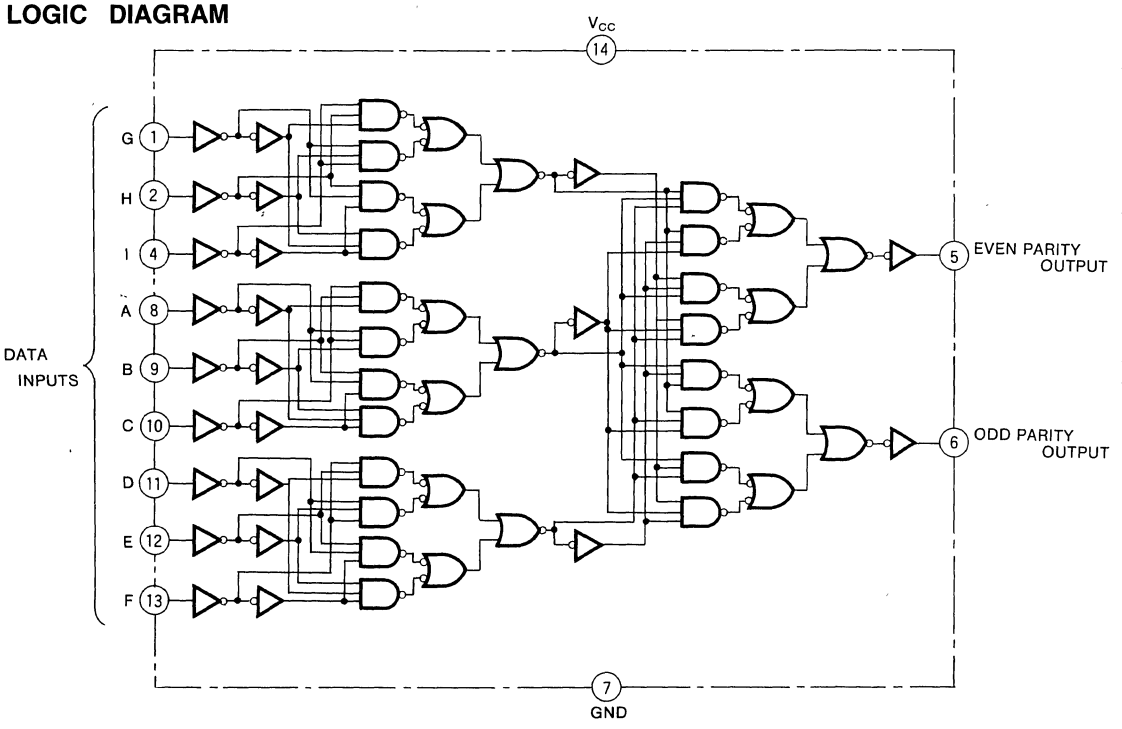
Use of silicon gate technology allows the M74HC280 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS280.

The M74HC280 combines the functions of a 9-bit parity generator and a parity checker. When used as a parity generator, applying 9-bit data to data inputs A through I will result in a generation of parity output to the even parity output or the odd parity output depending upon the number of high values in the data input. See the Function Table for details. When used as a parity checker, one bit from among the 9 bits of data input is used as an odd or even parity designation and the remaining eight bits are used as data.

FUNCTION TABLE

Number of data input high values	EVEN PARITY	ODD PARITY
Even	H	L
Odd	L	H

LOGIC DIAGRAM



MITSUBISHI ELECTRIC

9-BIT ODD/EVEN PARITY GENERATOR/CHECKER

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation		500	mW
Tstg	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL} ; I_{OH} = −20μA	2.0	1.9			1.9		V
			4.5	4.4			4.4		
			6.0	5.9			5.9		
		I_{OH} = −4.0mA	4.5	4.18			4.13		
		I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL} ; I_{OL} = 20μA	2.0			0.1		0.1	V
			4.5			0.1		0.1	
			6.0			0.1		0.1	
		I_{OL} = 4.0mA	4.5			0.26		0.33	
		I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V	6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V	6.0			−0.1		−1.0	
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA	6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

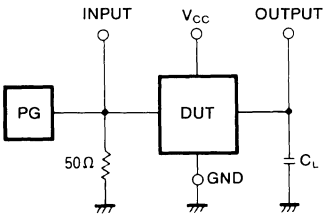
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 2)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time				35	ns
t_{PHL}					35	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 2)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time		2.0			205		258	ns
			4.5			41		52	
			6.0			35		44	
t_{PHL}	A ~ I — EVEN PARITY / ODD PARITY		2.0			205		258	
			4.5			41		52	
			6.0			35		44	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 1)				92				pF

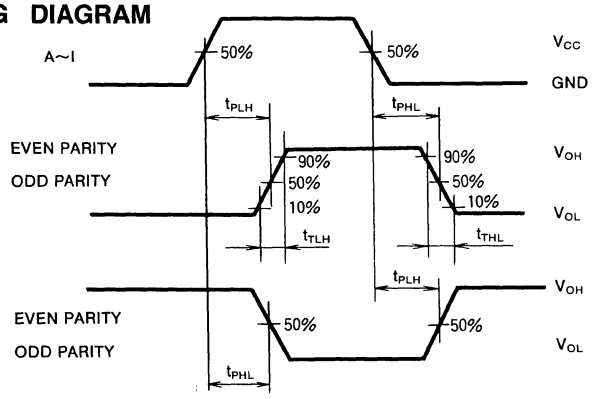
Note 1 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 2 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%). t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM



MITSUBISHI ELECTRIC

M74HC365P
M74HC365DP

HEX 3-STATE NONINVERTING BUFFER WITH COMMON ENABLES

DESCRIPTION

The M74HC365 is a semiconductor integrated circuit consisting of six buffers with 3-state noninverted outputs and common enable inputs.

FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 10ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

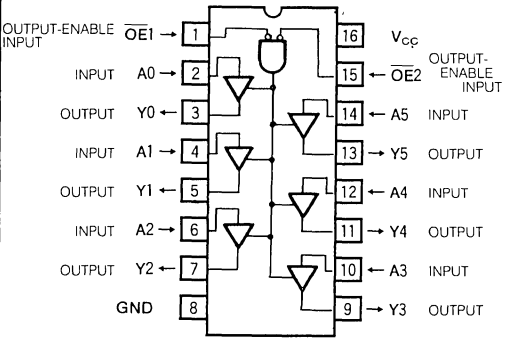
Use of silicon gate technology allows the M74HC365 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS365.

The M74HC365 consists of six 3-state buffers with output-enable inputs common to all circuits.

When output-enable inputs $\overline{OE1}$ and $\overline{OE2}$ are both low, outputs Y will become enable state. If input A is high, a high-level signal will be output to Y and if input A is low, a low-level signal will be output to Y.

When at least one of input $\overline{OE1}$ or $\overline{OE2}$ is high, Y will become high-impedance state.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4
16P2P

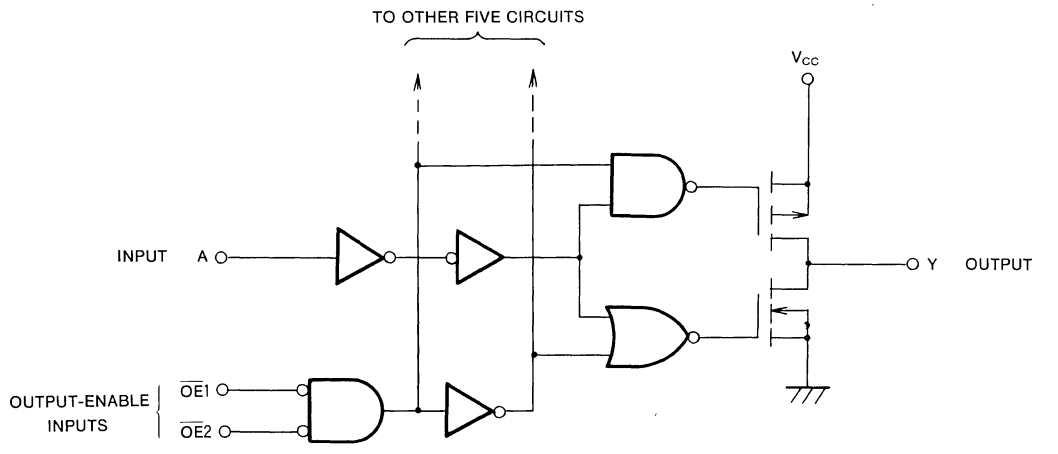
A version of the M74HC365 with an inverted output, the M74HC366, is also available.

FUNCTION TABLE (Note 1)

Inputs			Output
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

Note 1 : X : Irrelevant
Z : High impedance state

LOGIC DIAGRAM (EACH BUFFER)



ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC365DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
				V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = V_{CC}−0.1V, |I_O| = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V, |I_O| = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −6.0mA	4.5	4.18			4.13		
			I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 6.0mA	4.5			0.26		0.33	
			I_{OL} = 7.8mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

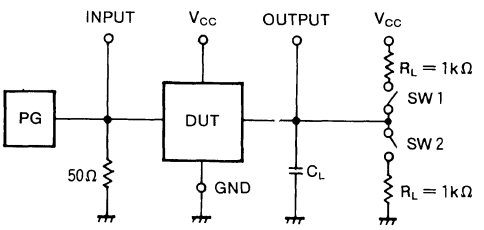
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level	C_L = 50pF (Note 4)			10	ns
t_{THL}	output transition time				10	
t_{PLH}	Low-level to high-level and high-level to low-level				22	ns
t_{PHL}	output propagation time (A − Y)				22	
t_{PLZ}	Output disable time from low-level and high-level	C_L = 5 pF (Note 4)			36	ns
t_{PHZ}	($\overline{OE}$ − Y)				36	
t_{PZL}	Output enable time to low-level and high-level	C_L = 50pF (Note 4)			40	ns
t_{PZH}	($\overline{OE}$ − Y)				40	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − Y)	C_L = 50pF (Note 4)	2.0			105		130	ns
			4.5			24		30	
			6.0			19		24	
t_{PHL}			2.0			105		130	
			4.5			24		30	
			6.0			19		24	
t_{PLH}		C_L = 150pF (Note 4)	2.0			135		168	
			4.5			29		36	
			6.0			24		30	
t_{PHL}			2.0			135		168	
			4.5			29		36	
			6.0			24		30	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − Y)	C_L = 50pF (Note 4)	2.0			175		218	ns
			4.5			44		55	
			6.0			37		46	
t_{PHZ}			2.0			175		218	
			4.5			44		55	
			6.0			37		46	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − Y)	C_L = 50pF (Note 4)	2.0			230		287	ns
			4.5			44		55	
			6.0			35		43	
t_{PZH}			2.0			230		287	
			4.5			44		55	
			6.0			35		43	
t_{PZL}		C_L = 150pF (Note 4)	2.0			245		306	
			4.5			53		66	
			6.0			41		51	
t_{PZH}			2.0			245		306	
			4.5			53		66	
			6.0			41		51	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}				15		15	
C_{PD}	Power dissipation capacitance (Note 3)				49				

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per buffer)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

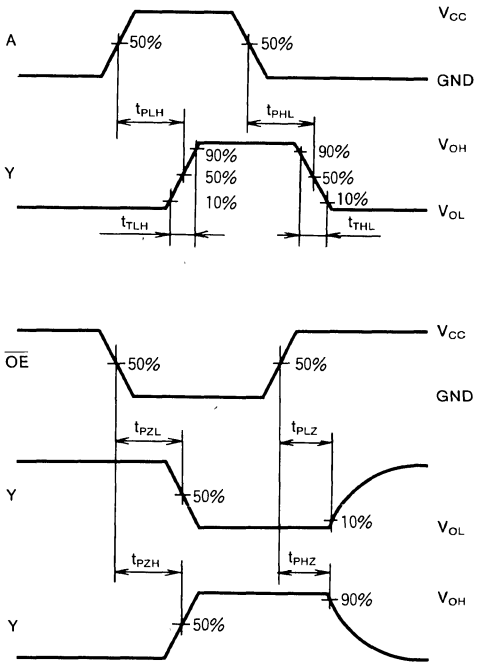
Note 4 : Test Circuit



Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

(1) The pulse generator (PG) has the following characteristics (10%~90%): $t_r = 6ns$, $t_f = 6ns$
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



M74HC366P

HEX 3-STATE INVERTING BUFFER WITH COMMON ENABLES

DESCRIPTION

The M74HC366 is a semiconductor integrated circuit consisting of six buffers with 3-state inverted outputs and common enable inputs.

FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 10ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

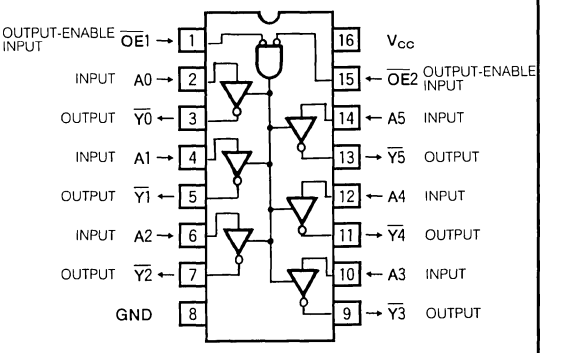
Use of silicon gate technology allows the M74HC366 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS366.

The M74HC366 consists of six 3-state buffers with output-enable inputs common to all circuits.

When output-enable inputs $\overline{OE1}$ and $\overline{OE2}$ are both low, outputs $\overline{Y}$ will become enable state. If input A is high, a low-level signal will be output to $\overline{Y}$ and if input A is low, a high-level signal will be output to $\overline{Y}$.

When at least one of the $\overline{OE1}$ or $\overline{OE2}$ is high, $\overline{Y}$ will become high-impedance state.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

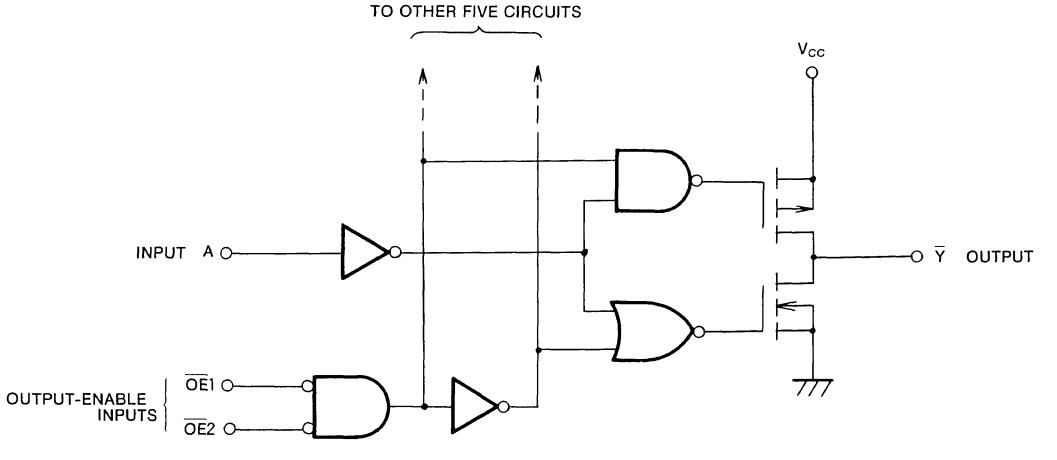
A version of the M74HC366 with a noninverted output, the M74HC365, is also available.

FUNCTION TABLE (Note 1)

Inputs			Output
$\overline{OE1}$	$\overline{OE2}$	A	$\overline{Y}$
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

Note 1 : X : Irrelevant
Z : High impedance

LOGIC DIAGRAM (EACH BUFFER)



ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation		500	mW
Tstg	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, |I_O| = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V, |I_O| = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −6.0mA	4.5	4.18			4.13		
			I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 6.0mA	4.5			0.26		0.33	
			I_{OL} = 7.8mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

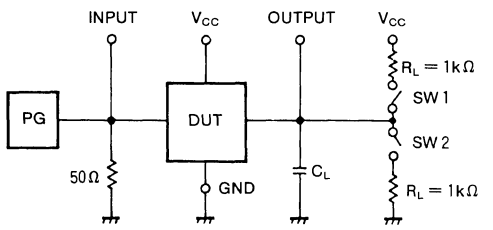
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − $\overline{Y}$)				18	ns
t_{PHL}					18	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − $\overline{Y}$)	C_L = 5 pF (Note 3)			36	ns
t_{PHZ}					36	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − $\overline{Y}$)	C_L = 50pF (Note 3)			40	ns
t_{PZH}					40	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Tip	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − $\overline{Y}$)	C_L = 50pF (Note 3)	2.0			82		102	ns
			4.5			19		24	
			6.0			16		20	
t_{PHL}			2.0			82		102	
			4.5			19		24	
			6.0			16		20	
t_{PLH}		C_L = 150pF (Note 3)	2.0			107		134	
			4.5			26		32	
			6.0			22		27	
t_{PHL}			2.0			107		134	
			4.5			26		32	
			6.0			22		27	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − $\overline{Y}$)	C_L = 50pF (Note 3)	2.0			175		218	ns
			4.5			44		55	
			6.0			37		46	
t_{PHZ}			2.0			175		218	
			4.5			44		55	
			6.0			37		46	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − $\overline{Y}$)	C_L = 50pF (Note 3)	2.0			230		287	ns
			4.5			44		55	
			6.0			35		43	
t_{PZH}			2.0			230		287	
			4.5			44		55	
			6.0			35		43	
t_{PZL}		C_L = 150pF (Note 3)	2.0			245		306	
			4.5			53		66	
			6.0			41		51	
t_{PZH}			2.0			245		306	
			4.5			53		66	
			6.0			41		51	
C_I	Input capacitance					10		10	pF
C_O	Output disabled capacitance	$\overline{OE}$ = V_{CC}				15		15	
C_{PD}	Power dissipation capacitance (Note 2)				46				

Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per buffer)
The power dissipated during operation under no-load conditions is calculated using the following formula
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

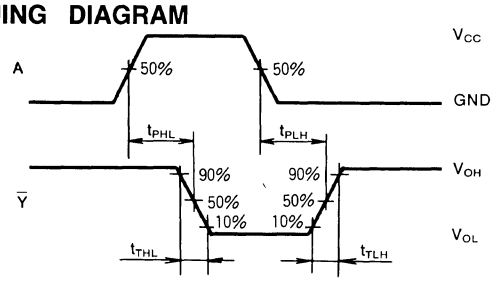
Note 3 : Test Circuit

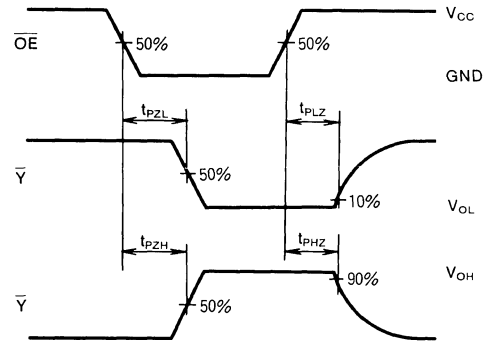


Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

(1) The pulse generator (PG) has the following characteristics (10%~90%) $t_r = 6ns$, $t_f = 6ns$
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM





M74HC367P
M74HC367DP

HEX 3-STATE NONINVERTING BUFFER WITH SEPARATE 2-BIT AND 4-BIT SECTIONS

DESCRIPTION

The M74HC367 is a semiconductor integrated circuit consisting of six buffers with 3-state noninverted outputs, the 4-bit and 2-bit sections having common enable inputs.

FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 10ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation. 20μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC367 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS367.

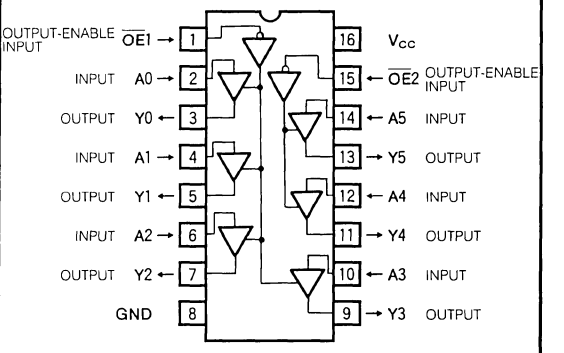
The M74HC367 consists of six 3-state buffers with output-enable inputs common to the 2-bit and 4-bit sections.

When output-enable input $\overline{OE}$ is low, outputs Y will become enable state. If inputs A are high, a high-level signal will be output to Y and if A are low, a low-level signal will be output to Y.

When $\overline{OE}$ is high, Y will become high-impedance state

A version of the M74HC367 with an inverted output, the M74HC368, is also available.

PIN CONFIGURATION (TOP VIEW)



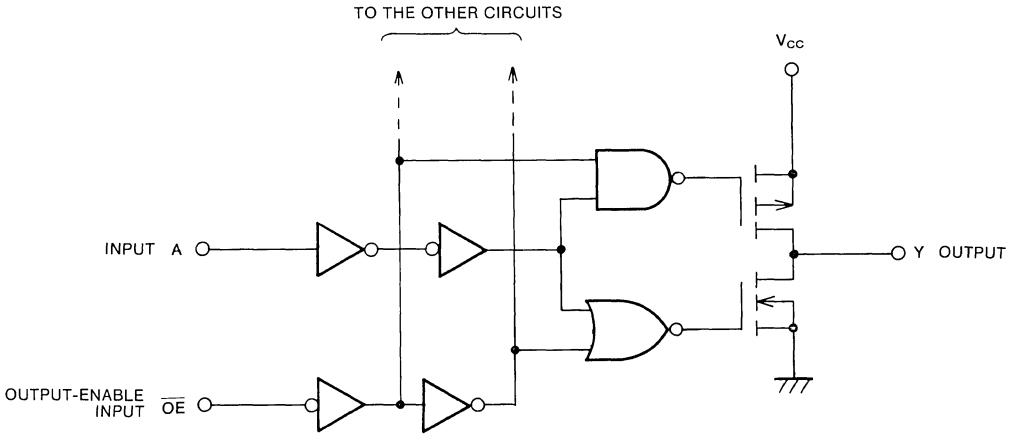
Outline 16P4, 16P2P

FUNCTION TABLE (Note 1)

Inputs		Output
$\overline{OE}$	A	Y
L	L	L
L	H	H
H	X	Z

Note 1 : X : Irrelevant
Z : High impedance

LOGIC DIAGRAM (EACH BUFFER)



HEX 3-STATE NONINVERTING BUFFER WITH SEPARATE 2-BIT AND 4-BIT SECTIONS

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC367DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = V_{CC}−0.1V, $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V, $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −6.0mA	4.5	4.18			4.13		
			I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 6.0mA	4.5			0.26		0.33	
			I_{OL} = 7.8mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

HEX 3-STATE NONINVERTING BUFFER WITH SEPARATE 2-BIT AND 4-BIT SECTIONS

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25°C)

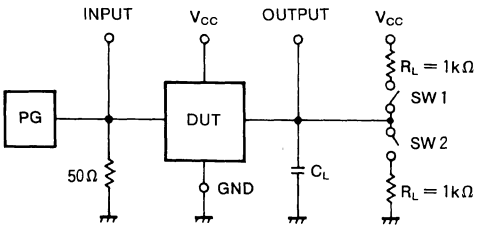
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − Y)				22	ns
t_{PHL}					22	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − Y)	C_L = 5 pF (Note 4)			33	ns
t_{PHZ}					33	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − Y)	C_L = 50pF (Note 4)			37	ns
t_{PZH}					37	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85°C)

Symbol	Parameter	Test conditions		Limits					Unit
				25°C			−40~+85°C		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − Y)	C_L = 50pF (Note 4)	2.0			105		130	ns
			4.5			24		30	
			6.0			19		24	
t_{PHL}			2.0			105		130	
			4.5			24		30	
			6.0			19		24	
t_{PLH}		C_L = 150pF (Note 4)	2.0			135		168	
			4.5			29		36	
			6.0			24		30	
t_{PHL}			2.0			135		168	
			4.5			29		36	
			6.0			24		30	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − Y)	C_L = 50pF (Note 4)	2.0			117		146	ns
			4.5			35		44	
			6.0			31		39	
t_{PHZ}			2.0			117		146	
			4.5			35		44	
			6.0			31		39	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − Y)	C_L = 50pF (Note 4)	2.0			172		216	ns
			4.5			38		47	
			6.0			35		43	
t_{PZH}			2.0			172		216	
			4.5			38		47	
			6.0			35		43	
t_{PZL}		C_L = 150pF (Note 4)	2.0			187		233	
			4.5			46		57	
			6.0			42		52	
t_{PZH}			2.0			187		233	
			4.5			46		57	
			6.0			42		52	
C_I	Input capacitance					10		10	pF
C_O	Output disabled capacitance	$\overline{OE}$ = V_{CC}				15		15	
C_{PD}	Power dissipation capacitance (Note 3)				47				

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per buffer)
The power dissipated during operation under no-load conditions is calculated using the following formula
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

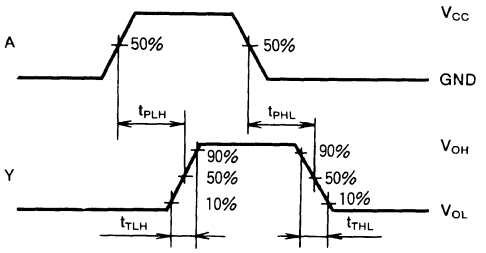
Note 4 : Test Circuit

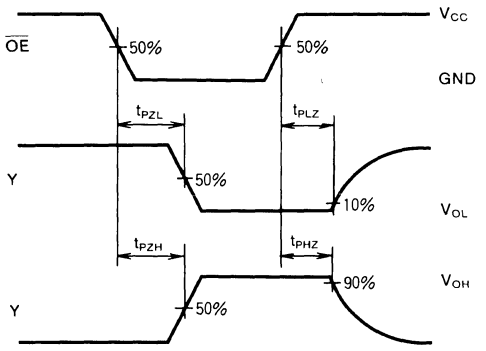


Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

(1) The pulse generator (PG) has the following characteristics (10%~90%) $t_r = 6ns$, $t_f = 6ns$
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM





M74HC368P
M74HC368DP

HEX 3-STATE INVERTING BUFFER WITH SEPARATE 2-BIT AND 4-BIT SECTIONS

DESCRIPTION

The M74HC368 is a semiconductor integrated circuit consisting of six buffers with 3-state inverted outputs, the 4-bit and 2-bit sections having common enable input.

FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 10ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC368 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS368

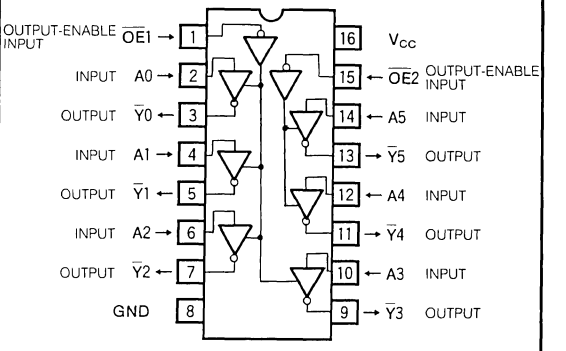
The M74HC368 consists of six 3-state buffers with output-enable inputs common to the 2-bit and 4-bit sections.

When output-enable input $\overline{OE}$ is low, outputs $\overline{Y}$ will become enable state. If input A is high, a low-level signal will be output to $\overline{Y}$ and if input A is low, a high-level signal will be output to $\overline{Y}$.

When $\overline{OE}$ is high, $\overline{Y}$ will become high-impedance state.

A version of the M74HC368 with a noninverted output, the M74HC367, is also available.

PIN CONFIGURATION (TOP VIEW)



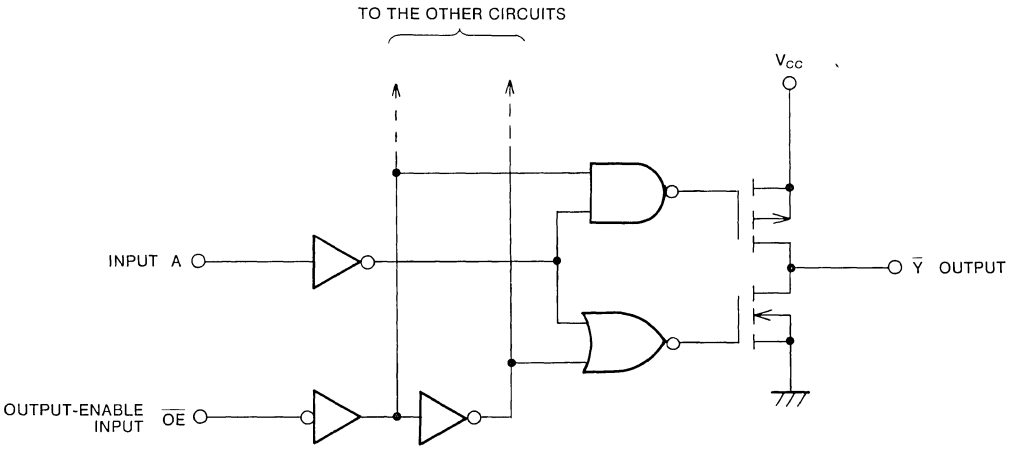
Outline 16P4
16P2P

FUNCTION TABLE (Note 1)

Inputs		Output
$\overline{OE}$	A	$\overline{Y}$
L	L	H
L	H	L
H	X	Z

Note 1 : X : Irrelevant
Z : High impedance

LOGIC DIAGRAM (EACH BUFFER)



M74HC368P
M74HC368DP

HEX 3-STATE INVERTING BUFFER WITH SEPARATE 2-BIT AND 4-BIT SECTIONS

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC368DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
				V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, |I_O| = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V, |I_O| = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −6.0mA	4.5	4.18			4.13		
			I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 6.0mA	4.5			0.26		0.33	
			I_{OL} = 7.8mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

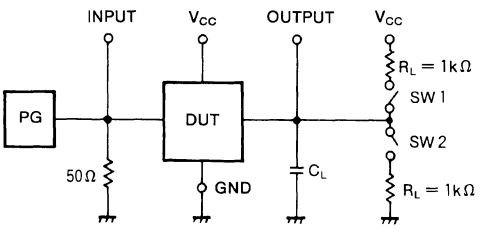
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − $\overline{Y}$)				18	ns
t_{PHL}					18	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − $\overline{Y}$)	C_L = 5 pF (Note 4)			33	ns
t_{PHZ}					33	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − $\overline{Y}$)	C_L = 50pF (Note 4)			37	ns
t_{PZH}					37	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − $\overline{Y}$)	C_L = 50pF (Note 4)	2.0			82		102	ns
			4.5			19		24	
			6.0			16		20	
t_{PHL}			2.0			82		102	
			4.5			19		24	
			6.0			16		20	
t_{PLH}		C_L = 150pF (Note 4)	2.0			107		134	
			4.5			26		32	
			6.0			22		27	
t_{PHL}			2.0			107		134	
			4.5			26		32	
			6.0			22		27	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − $\overline{Y}$)	C_L = 50pF (Note 4)	2.0			117		146	ns
			4.5			35		44	
			6.0			31		39	
t_{PHZ}			2.0			117		146	
			4.5			35		44	
			6.0			31		39	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − $\overline{Y}$)	C_L = 50pF (Note 4)	2.0			172		216	ns
			4.5			38		47	
			6.0			35		43	
t_{PZH}			2.0			172		216	
			4.5			38		47	
			6.0			35		43	
t_{PZL}		C_L = 150pF (Note 4)	2.0			187		233	
			4.5			46		57	
			6.0			42		52	
t_{PZH}			2.0			187		233	
			4.5			46		57	
			6.0			42		52	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}				15		15	
C_{PD}	Power dissipation capacitance (Note 3)				44				

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per buffer)
The power dissipated during operation under no-load conditions is calculated using the following formula
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

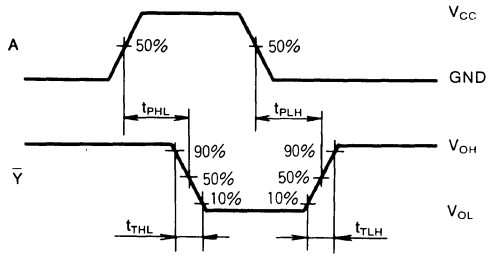
Note 4 : Test Circuit

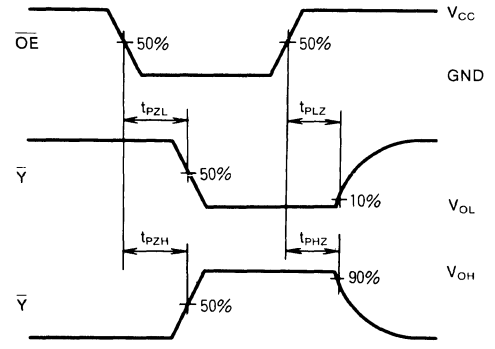


Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

(1) The pulse generator (PG) has the following characteristics (10%~90%). t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM





M74HC373P
M74HC373DWP

OCTAL 3-STATE NONINVERTING D-TYPE TRANSPARENT LATCH

DESCRIPTION

The M74HC373 is a semiconductor integrated circuit consisting of eight D-type latches with 3-state outputs, common latch-enable input and output-enable input.

FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 13ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC373 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS373.

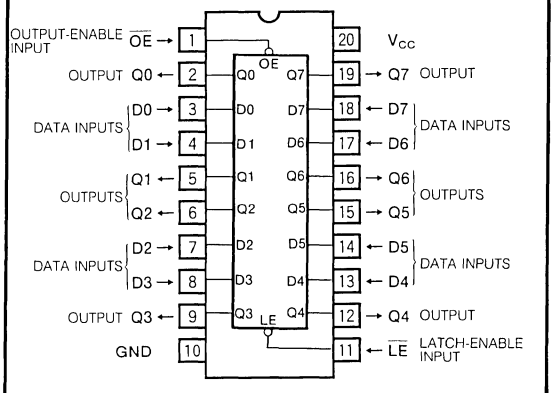
The M74HC373 consists of eight D-type latches with latch-enable input $\overline{LE}$ and output-enable input $\overline{OE}$ common to all circuits.

When $\overline{LE}$ is high, the signals of data input D will go through the latch and be output to Q. When the state of D changes, the state of Q will also change. When $\overline{LE}$ changes from high-level to low-level, the data existing immediatery prior to the change at D will be stored in the latch.

Even if other inputs are changed when $\overline{LE}$ is low, the contents stored in the latch will not be affected.

When $\overline{OE}$ is high, all outputs Q will become high-impedance state.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4
20P2V

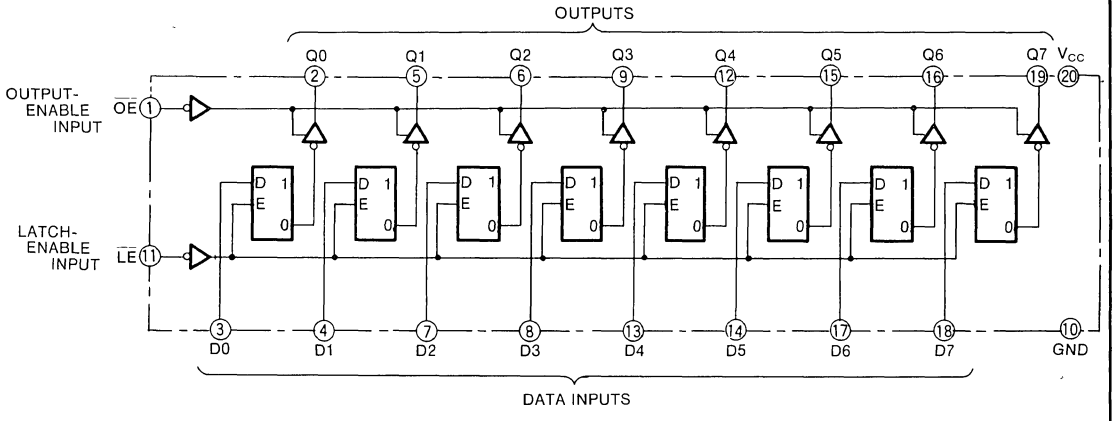
A version of the M74HC373 with the same pin connections and an inverted output, the M74HC533, is also available.

FUNCTION TABLE (Note 1)

Inputs			Output
$\overline{OE}$	$\overline{LE}$	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q^0
H	X	X	Z

Note 1 : Q^0 : Output state Q before $\overline{LE}$ changed
Z : High impedance
X : Irrelevant

LOGIC DIAGRAM



OCTAL 3-STATE NONINVERTING D-TYPE TRANSPARENT LATCH

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC373DWP, T_a = −40∼+80℃ and 80∼85℃ are derated at −7mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −6.0mA	4.5	4.18			4.13		
			I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 6.0mA	4.5			0.26		0.33	
			I_{OL} = 7.8mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O=V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V=GND		6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25°C)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (D − Q)				25	ns
t_{PHL}					25	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{LE}$ − Q)				30	ns
t_{PHL}					30	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − Q)	C_L = 5 pF (Note 4)			25	ns
t_{PHZ}					25	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − Q)	C_L = 50pF (Note 4)			28	ns
t_{PZH}					28	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

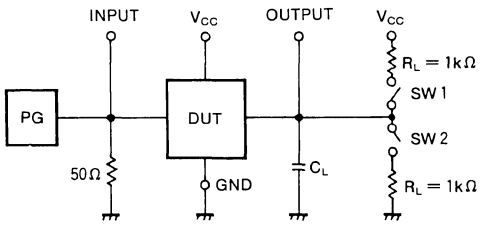
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (D − Q)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHL}			2.0			150		189	
			4.5			30		38	
			6.0			26		32	
t_{PLH}		C_L = 150pF (Note 4)	2.0			200		252	
			4.5			40		50	
			6.0			34		43	
t_{PHL}			2.0			200		252	
			4.5			40		50	
			6.0			34		43	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{LE}$ − Q)	C_L = 50pF (Note 4)	2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PHL}			2.0			175		221	
			4.5			35		44	
			6.0			30		37	
t_{PLH}		C_L = 150pF (Note 4)	2.0			225		284	
			4.5			45		57	
			6.0			38		48	
t_{PHL}			2.0			225		284	
			4.5			45		57	
			6.0			38		48	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − Q)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHZ}			2.0			150		189	
			4.5			30		38	
			6.0			26		32	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − Q)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZH}			2.0			150		189	
			4.5			30		38	
			6.0			26		32	
t_{PZL}		C_L = 150pF (Note 4)	2.0			200		252	
			4.5			40		50	
			6.0			34		43	
t_{PZH}			2.0			200		252	
			4.5			40		50	
			6.0			34		43	
C_I	Input capacitance					10		10	pF
C_O	Output disabled capacitance	$\overline{OE}$ = V_{CC}				15		15	
C_{PD}	Power dissipation capacitance (Note 3)				57				

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per latch)
The power dissipated during operation under no-load conditions is calculated using the following formula
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	Latch enable pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
t_{su}	D setup time with respect to $\overline{LE}$		2.0	75			90		ns
			4.5	15			18		
			6.0	13			16		
t_h	D hold time with respect to $\overline{LE}$		2.0	50			60		ns
			4.5	10			12		
			6.0	9			11		

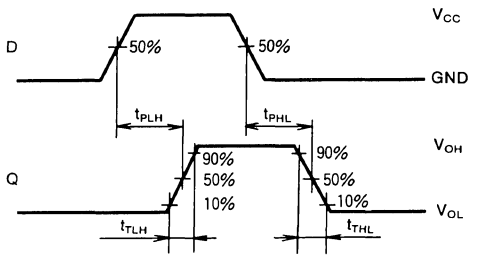
Note 4 : Test Circuit

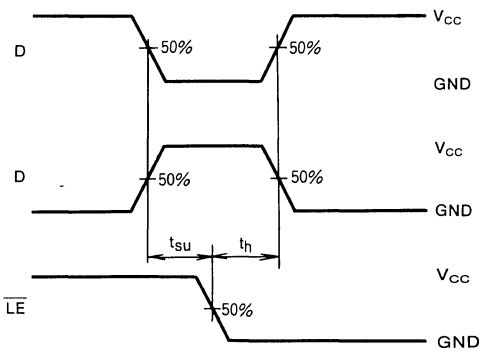


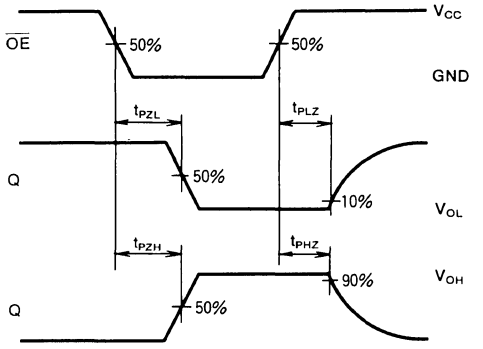
Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open ,
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

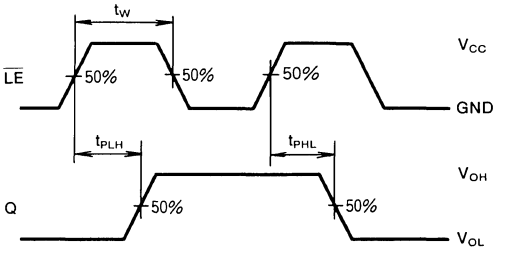
(1) The pulse generator (PG) has the following characteristics (10%~90%) t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM









M74HC374P
M74HC374DWP

OCTAL 3-STATE NONINVERTING D-TYPE FLIP-FLOP

DESCRIPTION

The M74HC374 is a semiconductor integrated circuit consisting of eight positive-edge triggered D-type flip-flops with 3-state outputs, common clock and output-enable inputs.

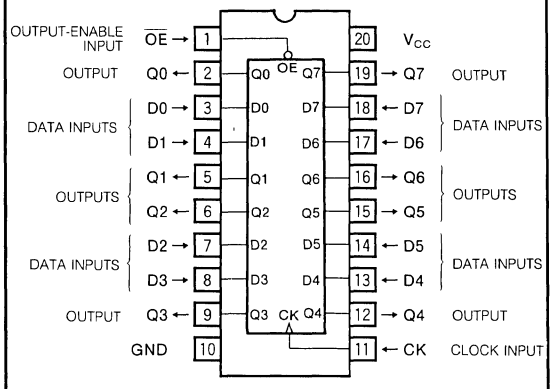
FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 15ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4
20P2V

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC374 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS374.

The M74HC374 contains eight edge-triggered D-type flip-flops, sharing common clock input CK and output enable input $\overline{OE}$.

When CK changes from low-level to high-level, the signals just previously input at D stores in the flip-flop.

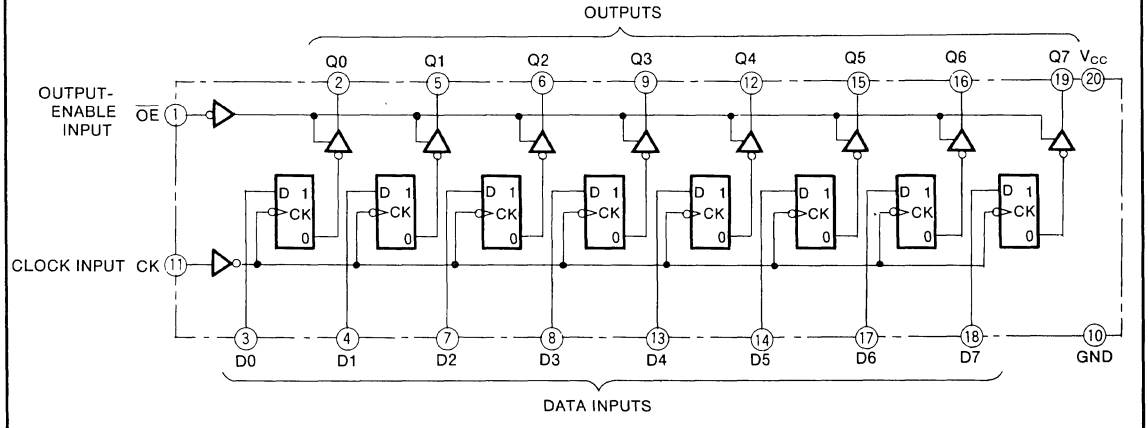
When $\overline{OE}$ is low, the signals stored in the flip-flop will be output to Q.

When $\overline{OE}$ is high, all outputs Q will become high-impedance state.

Even if $\overline{OE}$ is changed, the contents stored in the flip-flop will not be affected.

A version of the M74HC374 with the same pin connections and an inverted output, the M74HC534, is also available.

LOGIC DIAGRAM



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FUNCTION TABLE (Note 1)

Inputs			Output
$\overline{OE}$	CK	D	Q
L	↑	L	L
L	↑	H	H
L	L	X	Q^0
L	H	X	Q^0
L	↓	X	Q^0
H	X	X	Z

Note 1 : Q^0 : Output state Q before clock input changed
Z : High impedance
X : Irrelevant
↑ : Change from low to high level
↓ : Change from high to low level

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC374DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −6.0mA	4.5	4.18			4.13		
			I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 6.0mA	4.5			0.26		0.33	
			I_{OL} = 7.8mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	35			MHz
t_{TLH}	Low-level to high-level and high-level to low-level				10	ns
t_{THL}	output transition time				10	
t_{PLH}	Low-level to high-level and high-level to low-level				32	ns
t_{PHL}	output propagation time (CK − Q)				32	
t_{PLZ}	Output disable time from low-level and high-level	C_L = 5 pF (Note 4)			25	ns
t_{PHZ}	($\overline{OE}$ − Q)				25	
t_{PZL}	Output enable time to low-level and high-level	C_L = 50pF (Note 4)			28	ns
t_{PZH}	($\overline{OE}$ − Q)				28	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

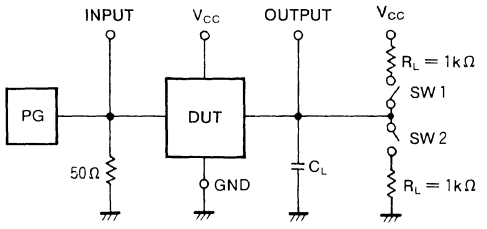
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	2.0	6			5		MHz
			4.5	30			24		
			6.0	35			28		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q)	C_L = 50pF (Note 4)	2.0			180		227	ns
			4.5			36		45	
			6.0			31		39	
t_{PHL}			2.0			180		227	
			4.5			36		45	
			6.0			31		39	
t_{PLH}		C_L = 150pF (Note 4)	2.0			230		290	
			4.5			46		58	
			6.0			39		49	
t_{PHL}			2.0			230		290	
			4.5			46		58	
			6.0			39		49	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − Q)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHZ}			2.0			150		189	
			4.5			30		38	
			6.0			26		32	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − Q)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZH}			2.0			150		189	
			4.5			30		38	
			6.0			26		32	
t_{PZL}		C_L = 150pF (Note 4)	2.0			200		252	
			4.5			40		50	
			6.0			34		43	
t_{PZH}			2.0			200		252	
			4.5			40		50	
			6.0			34		43	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}				15		15	
C_{PD}	Power dissipation capacitance (Note 3)				63				

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per flip-flop)
The power dissipated during operation under no-load conditions is calculated using the following formula
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	Clock pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
t_{su}	D setup time with respect to CK		2.0	75			90		ns
			4.5	15			18		
			6.0	13			16		
t_h	D hold time with respect to CK		2.0	50			60		ns
			4.5	10			12		
			6.0	9			11		

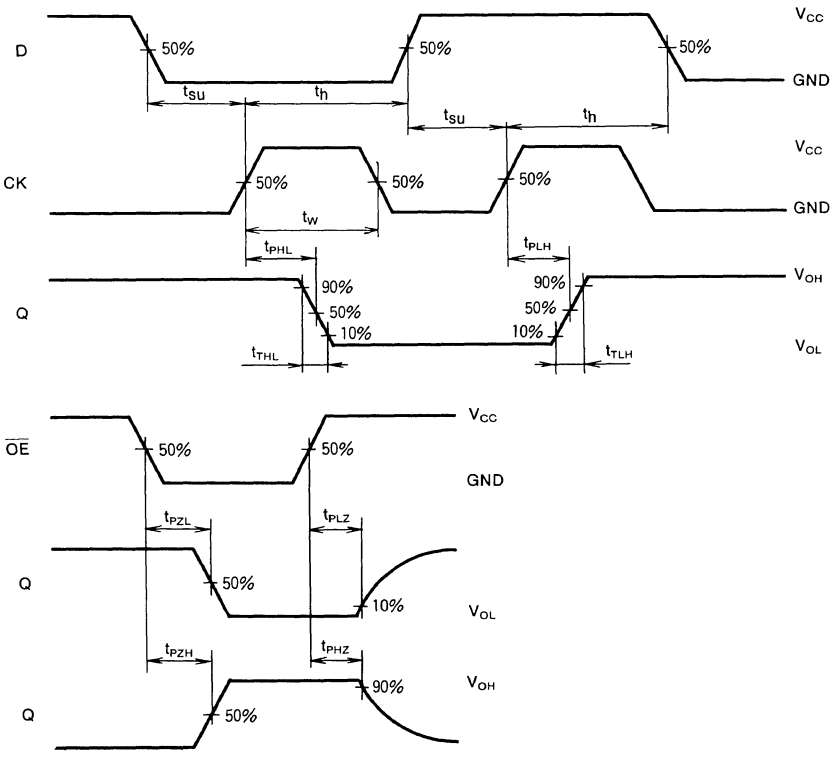
Note 4 : Test Circuit



Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Close	Open
t_{PHZ}	Open	Close
t_{PZL}	Close	Open
t_{PZH}	Open	Close

(1) The pulse generator (PG) has the following characteristics (10%~90%) t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM



M74HC390P

DUAL 4-STAGE BINARY RIPPLE COUNTER WITH ÷2 AND ÷5 SECTIONS

DESCRIPTION

The M74HC390 is a semiconductor integrated circuit consisting of two asynchronous decade counters with direct reset input.

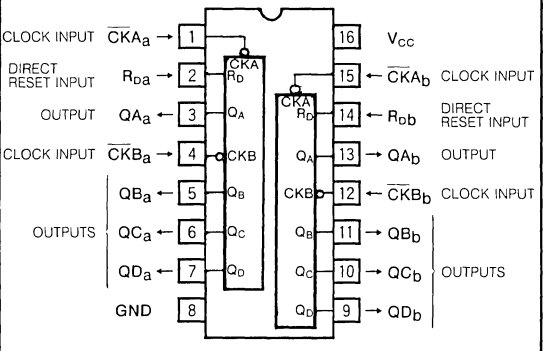
FEATURES

- High-speed: (clock frequency) 60MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC390 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS390.

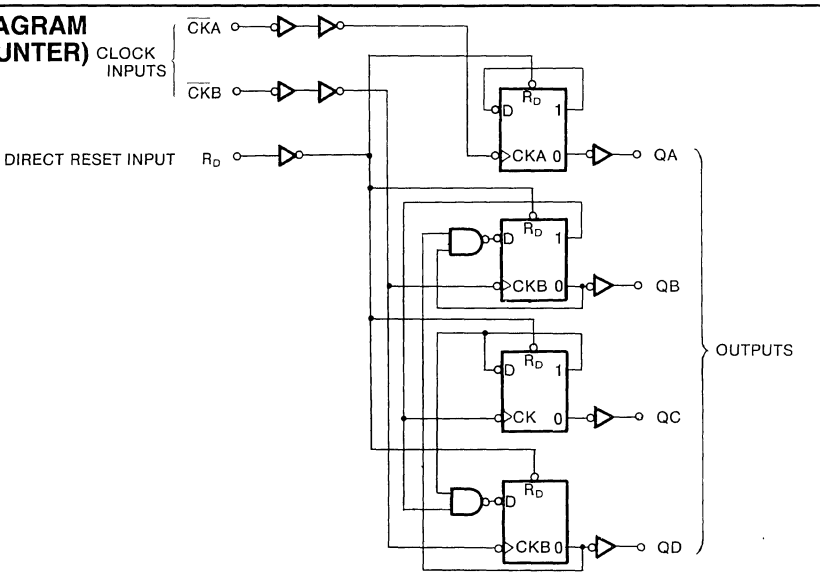
Each decade counter consists of a binary counter and a divide-by-5 counter. When using a binary counter,by applying the count pulse to clock input $\overline{CK}A$ a frequency-demultiplied signal will be output to QA. When using a divide-by-5 counter, by applying the count pulse to clock input $\overline{CK}B$ a frequency-demultiplied signal will be output to QB through QD.

When using the decade counter to output BCD code from QA through QD, connect QA and $\overline{CK}B$ together and apply the count pulse to $\overline{CK}A$ When outputting a signal with a 50% duty cycle from QA, connect QD and $\overline{CK}A$ together and apply the count pulse to $\overline{CK}B$

Counting takes place when the clock input changes from high-level to low-level.

When direct reset input R_D is high, QA through QB will become low irrespective of other inputs. Maintain the low-level state when counting.

LOGIC DIAGRAM (EACH COUNTER)



DUAL 4-STAGE BINARY RIPPLE COUNTER WITH ÷2 AND ÷5 SECTIONS

FUNCTION TABLE (Note 1)

Inputs		Outputs			
$\overline{CK}$	R_D	QA	QB	QC	QD
X	H	L	L	L	L
↓	L	Count			

Note 1 : ↓ : Change from high to low level
X : Irrelevant

Count	QA	QB	QC	QD
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

With QA and $\overline{CKB}$ connected and $\overline{CKA}$ used as input

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation		500	mW
Tstg	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

DUAL 4-STAGE BINARY RIPPLE COUNTER WITH ÷2 AND ÷5 SECTIONS

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0		0.1		0.1	V
			I_{OL} = 20μA	4.5		0.1		0.1	
			I_{OL} = 20μA	6.0		0.1		0.1	
			I_{OL} = 4.0mA	4.5		0.26		0.33	
			I_{OL} = 5.2mA	6.0		0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0		0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0		−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0		4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 3)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level output transition time				10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}A - QA$)				20	ns
t_{PHL}					20	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}A - QC$, with QA and $\overline{CK}B$ connected)				50	ns
t_{PHL}					50	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}B - QB$)				21	ns
t_{PHL}					21	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}B - QC$)				32	ns
t_{PHL}					32	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}B - QD$)				21	ns
t_{PHL}					21	
t_{PHL}	High-level to low-level output propagation time ($R_D - QA$, QB, QC, QD)				28	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

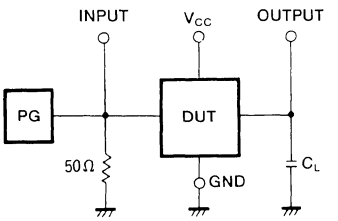
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 3)	2.0	5			4		MHz
			4.5	27			21		
			6.0	31			24		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$A − QA)		2.0			120		150	ns
			4.5			24		30	
			6.0			21		26	
t_{PHL}			2.0			120		150	
			4.5			24		30	
			6.0			21		26	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$A − QC, with QA and $\overline{CK}$B connected)		2.0			290		360	ns
			4.5			58		72	
			6.0			50		62	
t_{PHL}			2.0			290		360	
			4.5			58		72	
			6.0			50		62	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$B − QB)		2.0			130		160	ns
			4.5			26		33	
			6.0			22		28	
t_{PHL}			2.0			130		160	
			4.5			26		33	
			6.0			22		28	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$B − QC)		2.0			185		230	ns
			4.5			37		46	
			6.0			32		40	
t_{PHL}			2.0			185		230	
			4.5			37		46	
			6.0			32		40	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$B − QD)		2.0			130		160	ns
			4.5			26		33	
			6.0			22		28	
t_{PHL}			2.0			130		160	
			4.5			26		33	
			6.0			22		28	
t_{PHL}	High-level to low-level output propagation time (R_D − QA, QB, QC, QD)		2.0			165		210	ns
			4.5			33		41	
			6.0			28		35	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				46				pF

Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per counter)
The power dissipated during operation under no-load conditions is calculated using the following formula
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

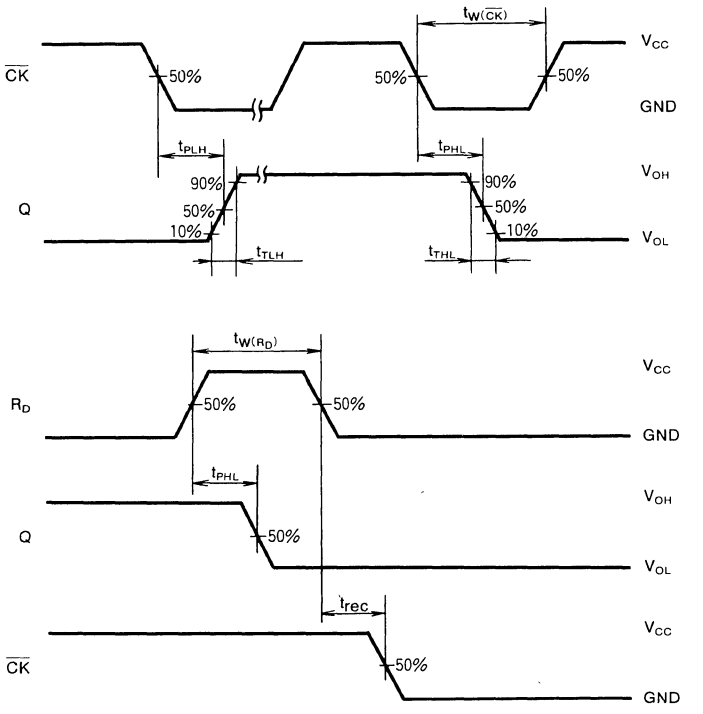
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
$t_{W(\overline{CK})}$	Clock pulse width		2.0	80			100		ns
			4.5	16			20		
			6.0	14			18		
$t_{W(R_D)}$	Direct reset pulse width		2.0	80			100		ns
			4.5	16			20		
			6.0	14			18		
t_{rec}	R_D recovery time with respect to $\overline{CK}$		2.0	50			65		ns
			4.5	10			13		
			6.0	9			11		

Note 3 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%) t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM



M74HC393P

DUAL 4-STAGE BINARY RIPPLE COUNTER

DESCRIPTION

The M74HC393 is a semiconductor integrated circuit consisting of two asynchronous 4-bit binary (hexadecilmal) counters with direct reset input.

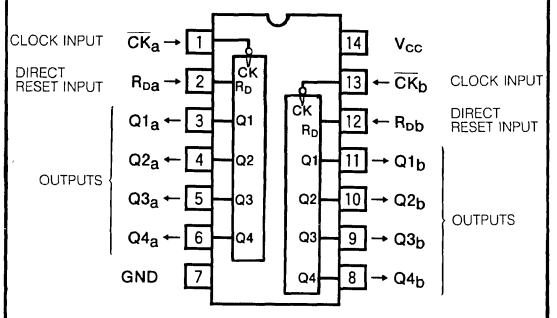
FEATURES

- High-speed: (clock frequency) 60MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



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FUNCTIONAL DESCRIPTION

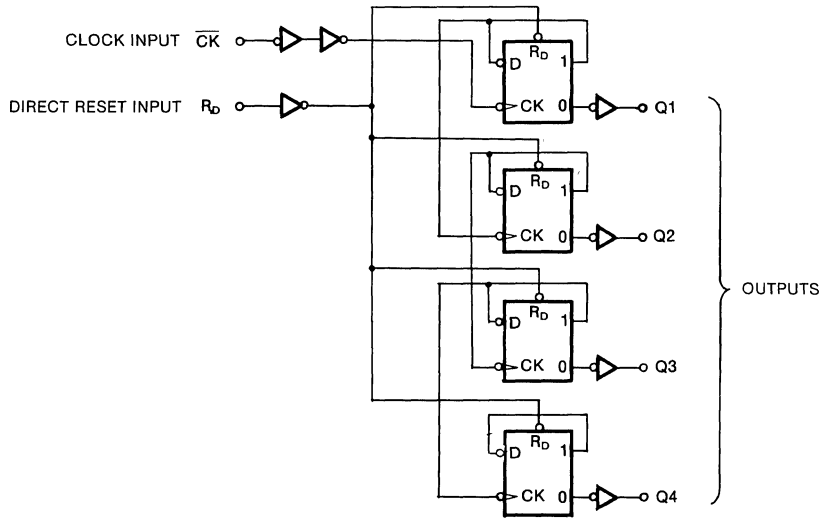
Use of silicon gate technology allows the M74HC393 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS393.

When the count pulse is applied to clock input $\overline{CK}$, a binary code will be output to Q1 through Q4.

Counting takes place when the clock input changes from high-level to low-level.

When direct reset input R_D is high, Q1 through Q4 will become low irrespective of other inputs. Maintain the low-level state when counting.

LOGIC DIAGRAM (EACH CIRCUIT)



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DUAL 4-STAGE BINARY RIPPLE COUNTER

FUNCTION TABLE (Note 1)

Inputs		Outputs			
$\overline{CK}$	R_D	Q1	Q2	Q3	Q4
X	H	L	L	L	L
↓	L	Count			

Note 1 : ↓ : Change from high-level to low-level
X : Irrelevant

Count	Q1	Q2	Q3	Q4
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation		500	mW
Tstg	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		4.4		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 3)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level output transition time				10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$ − Q1)				20	ns
t_{PHL}					20	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$ − Q2)				35	ns
t_{PHL}					35	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$ − Q3)				42	ns
t_{PHL}					42	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$ − Q4)				50	ns
t_{PHL}					50	
t_{PHL}	High-level to low-level output propagation time (R_D − Q1, Q2, Q3, Q4)				28	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

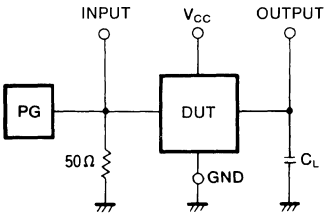
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 3)	2.0	5			4		MHz
			4.5	27			21		
			6.0	31			24		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$ − Q1)		2.0			120		150	ns
			4.5			24		30	
			6.0			21		26	
t_{PHL}			2.0			120		150	
			4.5			24		30	
			6.0			21		26	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$ − Q2)		2.0			190		240	ns
			4.5			38		47	
			6.0			32		40	
t_{PHL}			2.0			190		240	
			4.5			38		47	
			6.0			32		40	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$ − Q3)		2.0			240		300	ns
			4.5			48		60	
			6.0			41		51	
t_{PHL}			2.0			240		300	
			4.5			48		60	
			6.0			41		51	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$ − Q4)		2.0			290		360	ns
			4.5			58		72	
			6.0			50		62	
t_{PHL}			2.0			290		360	
			4.5			58		72	
			6.0			50		62	
t_{PHL}	High-level to low-level output propagation time (R_D − Q1, Q2, Q3, Q4)		2.0			165		210	ns
			4.5			33		41	
			6.0			28		35	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				41				pF

Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per counter)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85°C)

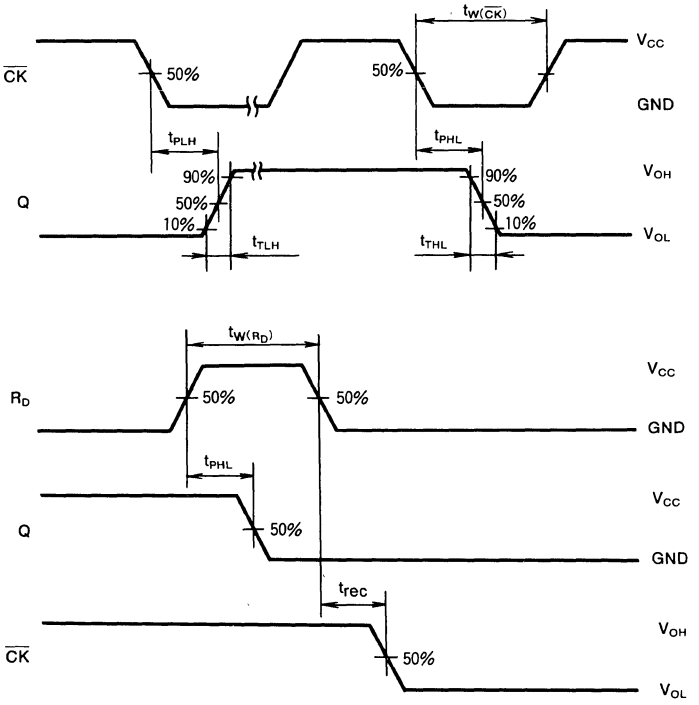
Symbol	Parameter	Test conditions		Limits					Unit
				25°C			−40~+85°C		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
$t_{w(\overline{CK})}$	Clock pulse width		2.0	80			100		ns
			4.5	16			20		
			6.0	14			18		
$t_{w(R_D)}$	Direct reset pulse width		2.0	80			100		ns
			4.5	16			20		
			6.0	14			18		
t_{rec}	R_D recovery time with respect to $\overline{CK}$		2.0	50			65		ns
			4.5	10			13		
			6.0	9			11		

Note 3 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%) t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM



MITSUBISHI ELECTRIC

M74HC533P

OCTAL 3-STATE INVERTING D-TYPE TRANSPARENT LATCH

DESCRIPTION

The M74HC533 is a semiconductor integrated circuit consisting of eight D-type latches with 3-state outputs, common latch-enable input and output-enable input.

FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 13ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC533 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS533.

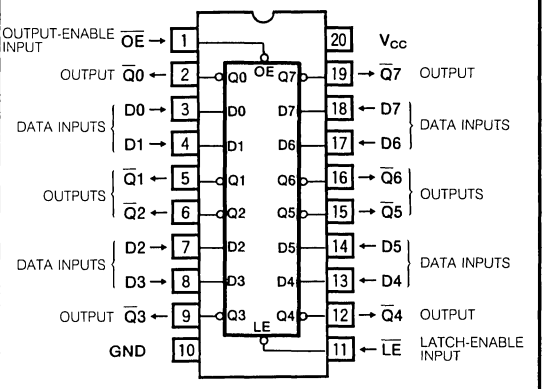
The M74HC533 consists of eight D-type latches with latch-enable input $\overline{LE}$ and output-enable input $\overline{OE}$ common to all circuits

When $\overline{LE}$ is high, the signals of data input D will go through the latch and be output to inverted output $\overline{Q}$. When the state of D changes, the state of $\overline{Q}$ will also change. When $\overline{LE}$ changes from high-level to low-level, the data existing immediately prior to the change at D will be stored in the latch .

Even if other inputs are changed when $\overline{LE}$ is low, the contents stored in the latch will not be affected.

When $\overline{OE}$ is high, all outputs $\overline{Q}$ will become high-impedance state.

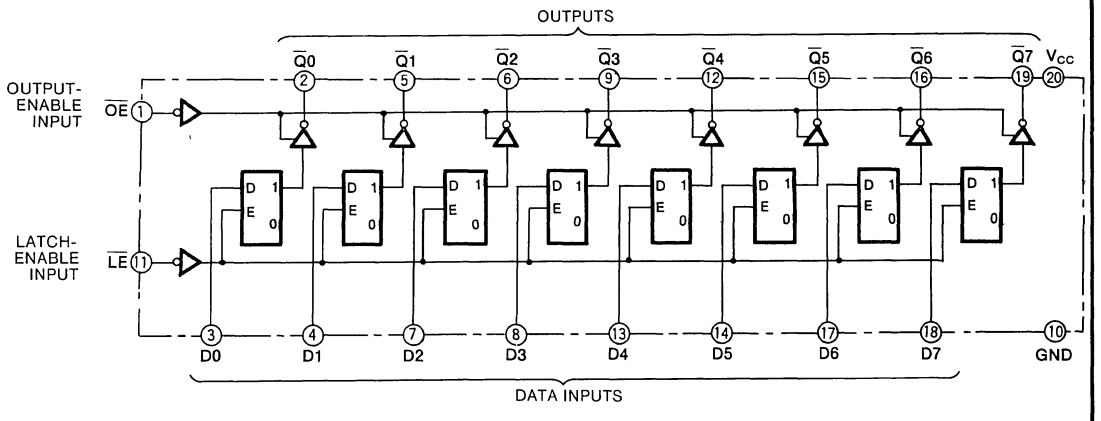
PIN CONFIGURATION (TOP VIEW)



Outline 20P4

A version of the M74HC533 with the same pin connections and a noninverted output, the M74HC373, is also available.

LOGIC DIAGRAM



OCTAL 3-STATE INVERTING D-TYPE TRANSPARENT LATCH

FUNCTION TABLE (Note 1)

Inputs			Output
$\overline{OE}$	$\overline{LE}$	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}^0$
H	X	X	Z

Note 1 : Q^0 : Output state $\overline{Q}$ before $\overline{LE}$ changed.
Z : High impedance
X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation		500	mW
Tstg	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −6.0mA	4.5	4.18			4.13		
			I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0		0.1		0.1	V
			I_{OL} = 20μA	4.5		0.1		0.1	
			I_{OL} = 20μA	6.0		0.1		0.1	
			I_{OL} = 6.0mA	4.5		0.26		0.33	
			I_{OL} = 7.8mA	6.0		0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (D − $\overline{Q}$)				25	ns
t_{PHL}					25	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{LE}$ − $\overline{Q}$)				30	ns
t_{PHL}					30	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − $\overline{Q}$)	C_L = 5 pF (Note 3)			25	ns
t_{PHZ}					25	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − $\overline{Q}$)	C_L = 50pF (Note 3)			28	ns
t_{PZH}					28	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

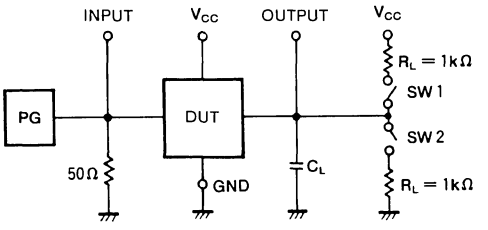
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (D − $\overline{Q}$)	C_L = 50pF (Note 3)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHL}			2.0			150		189	
			4.5			30		38	
			6.0			26		32	
t_{PLH}		C_L = 150pF (Note 3)	2.0			200		252	
			4.5			40		50	
			6.0			34		43	
t_{PHL}			2.0			200		252	
			4.5			40		50	
			6.0			34		43	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{LE}$ − $\overline{Q}$)	C_L = 50pF (Note 3)	2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PHL}			2.0			175		221	
			4.5			35		44	
			6.0			30		37	
t_{PLH}		C_L = 150pF (Note 3)	2.0			225		284	
			4.5			45		57	
			6.0			38		48	
t_{PHL}			2.0			225		284	
			4.5			45		57	
			6.0			38		48	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − Q)	C_L = 50pF (Note 3)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHZ}			2.0			150		189	
			4.5			30		38	
			6.0			26		32	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − $\overline{Q}$)	C_L = 50pF (Note 3)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZH}			2.0			150		189	
			4.5			30		38	
			6.0			26		32	
t_{PZL}		C_L = 150pF (Note 3)	2.0			200		252	
			4.5			40		50	
			6.0			34		43	
t_{PZH}			2.0			200		252	
			4.5			40		50	
			6.0			34		43	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}				15		15	
C_{PD}	Power dissipation capacitance (Note 2)				57				

Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per latch)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40~+85℃		
		V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	Latch enable pulse width	2.0	80			101		ns
		4.5	16			20		
		6.0	14			17		
t_{su}	D setup time with respect to $\overline{LE}$	2.0	75			90		ns
		4.5	15			18		
		6.0	13			16		
t_h	D hold time with respect to $\overline{LE}$	2.0	50			60		ns
		4.5	10			12		
		6.0	9			11		

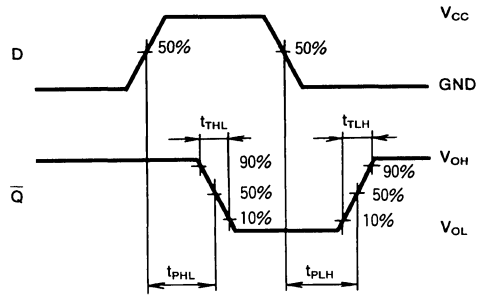
Note 3 : Test Circuit

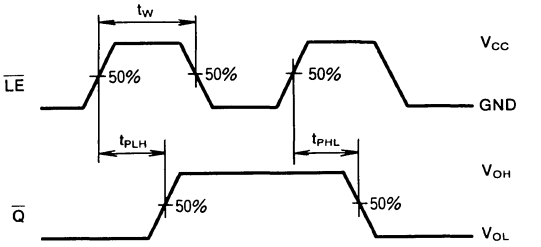


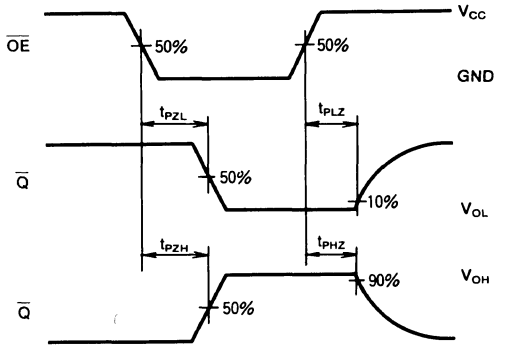
Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

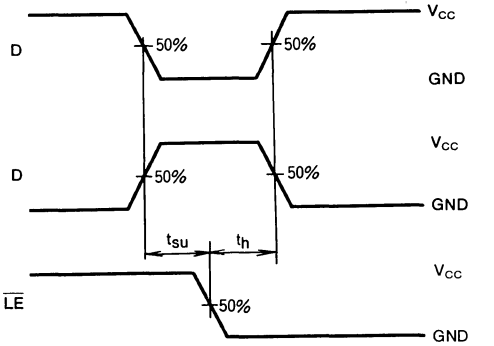
(1) The pulse generator (PG) has the following characteristics (10%~90%) t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM









M74HC534P

OCTAL 3-STATE INVERTING D-TYPE FLIP-FLOP

DESCRIPTION

The M74HC534 is a semiconductor integrated circuit consisting of eight positive edge triggered D-type flip-flops with 3-state outputs, common clock input and output-enable input.

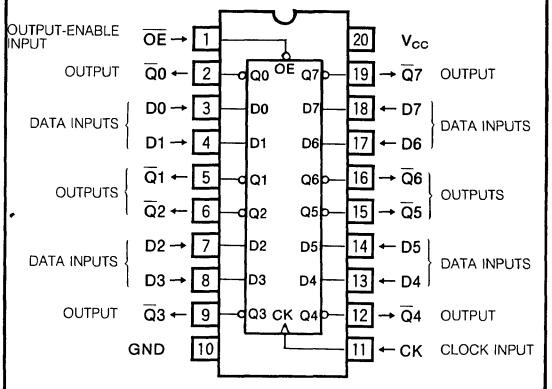
FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 13ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC534 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS534.

The M74HC534 contains eight edge triggered D-type flip-flops, sharing common clock input CK and output-enable input $\overline{OE}$.

When CK changes from low-level to high-level, the signals just previously input at D stores in the flip-flop.

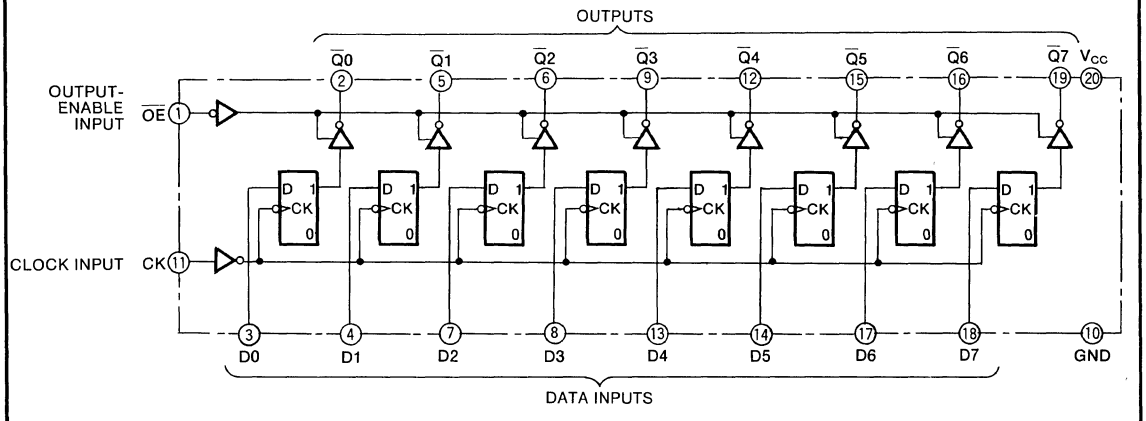
When output-enable input $\overline{OE}$ is low, the signals stored in the flip-flop will be output to $\overline{Q}$.

When $\overline{OE}$ is high, all outputs $\overline{Q}$ will become high-impedance state.

Even if $\overline{OE}$ is changed, the contents stored in the flip-flop will not be affected.

A version of the M74HC534 with the same pin connections and a noninverted output, the M74HC374, is also available.

LOGIC DIAGRAM



MITSUBISHI ELECTRIC

OCTAL 3-STATE INVERTING D-TYPE FLIP-FLOP

FUNCTION TABLE (Note 1)

Inputs			Output
$\overline{OE}$	CK	D	$\overline{Q}$
L	↑	L	H
L	↑	H	L
L	L	X	$\overline{Q}^0$
L	H	X	$\overline{Q}^0$
L	↓	X	$\overline{Q}^0$
H	X	X	Z

Note 1 : $\overline{Q}^0$: Output state $\overline{Q}$ before clock input changed
Z : High impedance
X : Irrelevant
↑ : Change from low to high level
↓ : Change from high to low level

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation		500	mW
Tstg	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −6.0mA	4.5	4.18			4.13		
			I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 6.0mA	4.5			0.26		0.33	
			I_{OL} = 7.8mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 3)	35			MHz
t_{TLH}	Low-level to high-level and high-level to low-level output transition time				10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − $\overline{Q}$)				32	ns
t_{PHL}					32	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − $\overline{Q}$)	C_L = 5 pF (Note 3)			25	ns
t_{PHZ}					25	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − $\overline{Q}$)	C_L = 50pF (Note 3)			28	ns
t_{PZH}					28	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

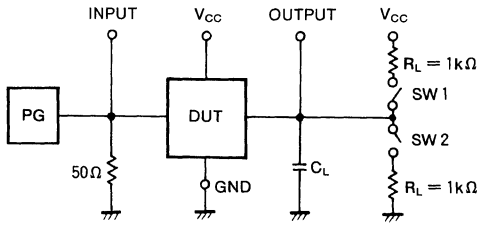
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 3)	2.0	6			5		MHz
			4.5	30			24		
			6.0	35			28		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 3)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − $\overline{Q}$)	C_L = 50pF (Note 3)	2.0			180		227	ns
			4.5			36		45	
			6.0			31		39	
t_{PHL}			2.0			180		227	
			4.5			36		45	
			6.0			31		39	
t_{PLH}		C_L = 150pF (Note 3)	2.0			230		290	
			4.5			46		58	
			6.0			39		49	
t_{PHL}			2.0			230		290	
			4.5			46		58	
			6.0			39		49	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − $\overline{Q}$)	C_L = 50pF (Note 3)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHZ}			2.0			150		189	
			4.5			30		38	
			6.0			26		32	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − $\overline{Q}$)	C_L = 50pF (Note 3)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZH}			2.0			150		189	
			4.5			30		38	
			6.0			26		32	
t_{PZL}		C_L = 150pF (Note 3)	2.0			200		252	
			4.5			40		50	
			6.0			34		43	
t_{PZH}			2.0			200		252	
			4.5			40		50	
			6.0			34		43	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}				15		15	
C_{PD}	Power dissipation capacitance (Note 2)				63				

Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per flip flop)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symboi	Parameter	Test condition		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	Clock pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
t_{su}	D setup time with respect to CK		2.0	75			90		ns
			4.5	15			18		
			6.0	13			16		
t_h	D hold time with respect to CK		2.0	50			60		ns
			4.5	10			12		
			6.0	9			11		

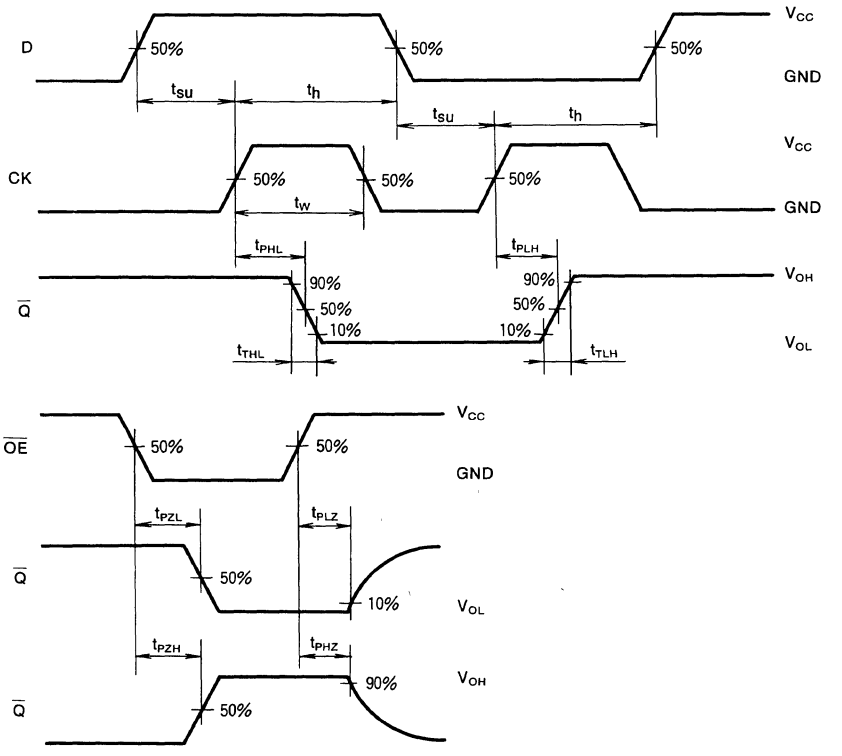
Note 3 : Test Circuit



Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

(1) The pulse generator (PG) has the following characteristics (10%~90%). t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



MITSUBISHI ELECTRIC

M74HC4002P

DUAL 4-INPUT POSITIVE NOR GATE

DESCRIPTION

The M74HC4002 is a semiconductor integrated circuit consisting of two 4-input positive-logic NOR, usable as negative-logic NAND gates.

FEATURES

- High-speed: 10ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

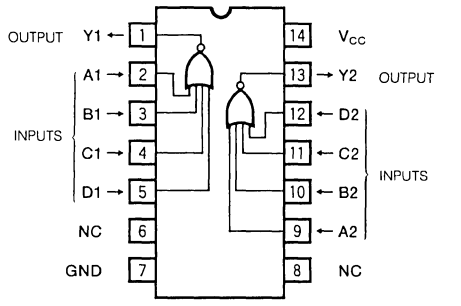
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC4002 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the LSTTLs.

Buffered outputs Y improve input-to-output transfer characteristics and reduce to a minimum output impedance variations with respect to input voltage variations.

When inputs A, B, C, and D are low, output Y is high, and when at least one of the inputs is high, output Y is low.

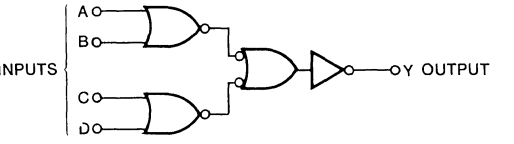
PIN CONFIGURATION (TOP VIEW)



Outline 14P4

NC : NO CONNECTION

LOGIC DIAGRAM (EACH GATE)



FUNCTION TABLE

Inputs		Output
A	N	Y
L	L	H
H	L	L
L	H	L
H	H	L

N = B + C + D

ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation		500	mW
Tstg	Storage temperature range		−65~+150	℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits						Unit
					25℃			−40∼+85℃		
				V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, $\|I_O\|$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V, $\|I_O\|$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			1.0		10.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

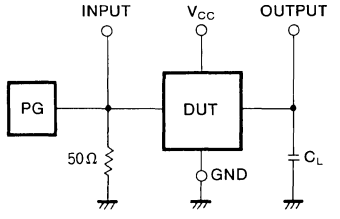
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 2)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time				20	ns
t_{PHL}					20	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 2)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time		2.0			120		151	ns
			4.5			24		30	
			6.0			20		26	
t_{PHL}			2.0			120		151	
			4.5			24		30	
			6.0			20		26	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 1)				31				pF

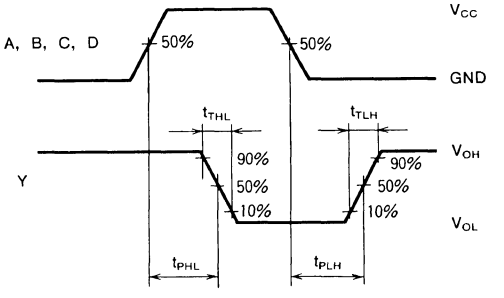
Note 1 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per gate)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 2 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%) t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM



M74HC4078P

8-INPUT POSITIVE NOR/OR GATE

DESCRIPTION

The M74HC4078 is a semiconductor integrated circuit consisting of an 8-input positive-logic NOR/OR, usable as a negative-logic NAND/AND gate.

FEATURES

- High-speed: 16ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 5μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

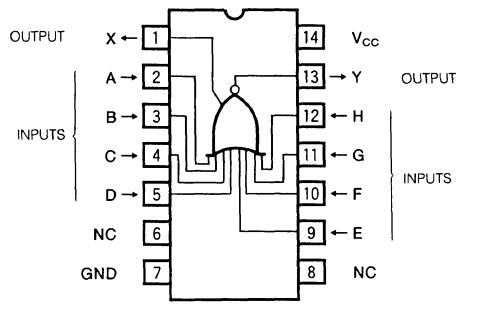
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC4078 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the LSTTL.

Buffered outputs Y and X improve input-to-output transfer characteristics and reduce to a minimum output impedance variations with respect to input voltage variations.

When all inputs A through H are low, output Y will become high and output X will become low. When at least one of the inputs is high, the output Y will become low and the output X will become high.

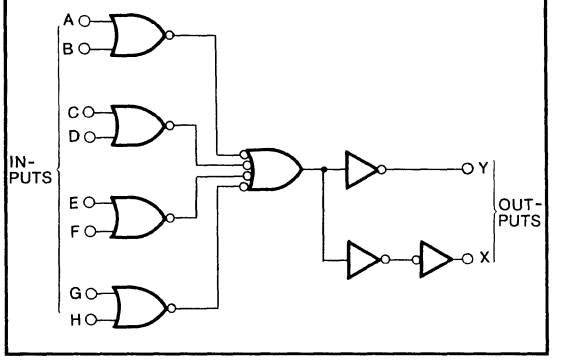
PIN CONFIGURATION (TOP VIEW)



Outline 14P4

NC : NO CONNECTION

LOGIC DIAGRAM



FUNCTION TABLE

Inputs		Outputs	
A	N	Y	X
L	L	H	L
H	L	L	H
L	H	L	H
H	H	L	H

N = B + C + D + E + F + G + H

ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation		500	mW
Tstg	Storage temperature range		−65~+150	℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r,	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IL}, V_{IH}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			1.0		10.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 2)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A ~ H − Y)				22	ns
t_{PHL}					22	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A ~ H − X)				24	ns
t_{PHL}					24	

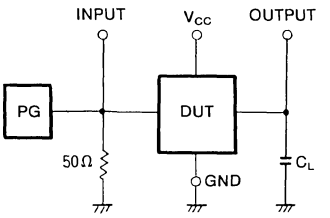
SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 2)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A ~ H − Y)		2.0			130		165	ns
			4.5			26		33	
			6.0			22		28	
t_{PHL}			2.0			130		165	
			4.5			26		33	
			6.0			22		28	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A ~ H − X)		2.0			140		175	ns
			4.5			28		35	
			6.0			24		30	
t_{PHL}			2.0			140		175	
			4.5			28		35	
			6.0			24		30	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 1)				75				pF

Note 1 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula

$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 2 : Test Circuit



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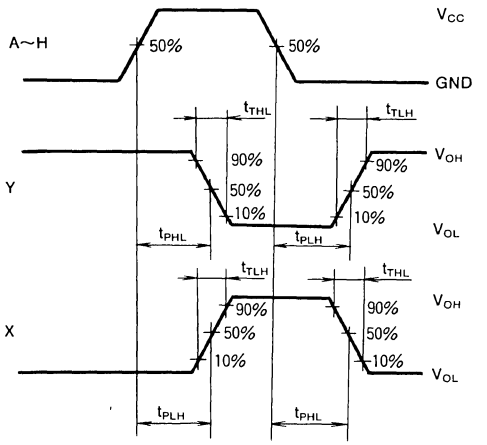
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM



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