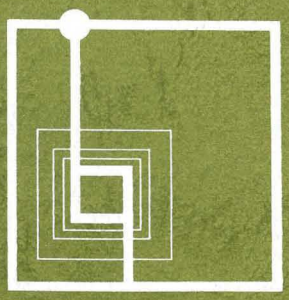
MITSUBISHI DATA BOOK 1982

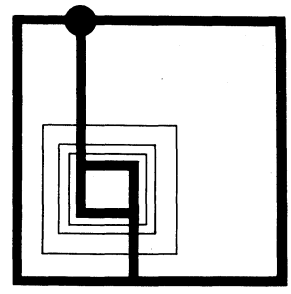
VIDEO



MITSUBISHI ELECTRIC

MITSUBISHI DATA BOOK 1982

VIDEO



MITSUBISHI ELECTRIC

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INDEX & GENERAL INFORMATION

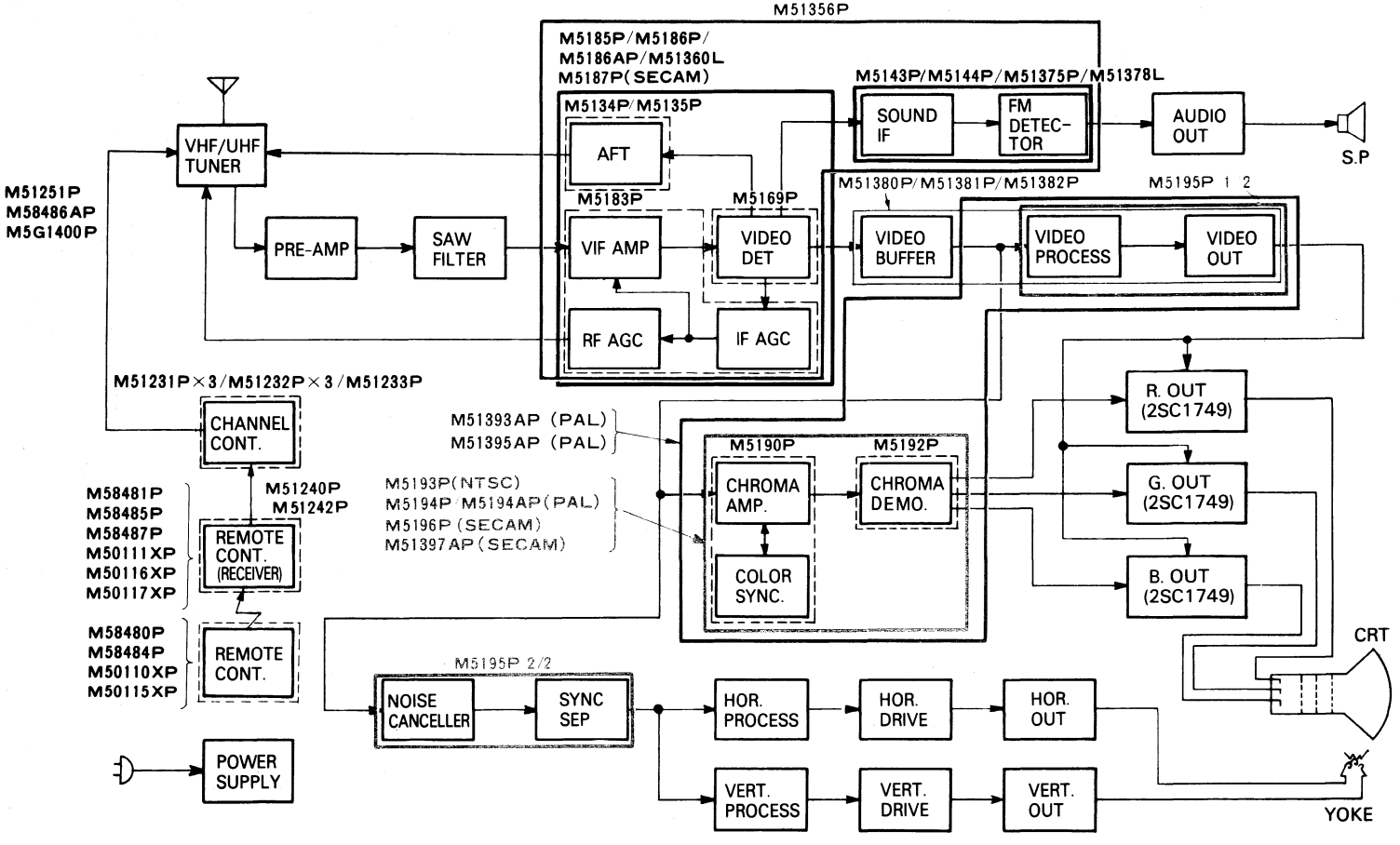
1

TYPE DESIGNATION TABLE

CIRCUIT FUNCTIONS

TYPE No. \ FUNCTION		VIF AMP	IF AGC	AGC FW RF	AGC RV RF	VIDEO DET.	SIF DET.	AFT.	NOISE CAN.	SYNC. SEP.	VIDEO BUFF.	PIX CONTROL	CONTRAST CONTROL	BRIGHTNESS CONTROL	PEDESTAL CLAMP	BLANKING	ABL	VIDEO OUT	CHROMA SIG. PROCESSOR	CHROMA SYNC.	CHROMA DEMOD.	SIF/DET	AF POWER	CHANNEL SELECTOR	REMOTE CONTROL
M5134P	14							■																	
M5135P	14							■																	
M5183P	14	■	■	■																					
M5169P	8					■																			
M5185P	28	■	■	■	■	■	■	■																	
M5186P/AP	22	■	■	■	■	■	■	■																	
M5187P	22	■	■		■	■		■																	
M51360L	16	■	■		■	■																			
M51356P	30	■	■		■	■	■	■														■			
M5195P	16								■	■			■	■	■	■	■	■							
M51380P	16										■	■	■	■	■	■	■	■							
M51381P	14										■	■	■	■	■	■	■	■							
M51382P	14										■	■	■	■	■	■	■	■							
M5190P	14																		■	■					
M5192P	14																				■				
M5193P	22																		■	■	■				
M5194P/AP	22																		■	■	■				
M5196P	28																		■	■	■				
M51393P	30											■	■	■	■	■	■	■	■	■	■				
M51395P	30											■	■	■	■	■	■	■	■	■	■				
M51397P	30																		■	■	■				
M5143P	14																					■			
M5144P	14																					■			
M51375P	14																					■			
M51378L	8																					■			
M51231P	16																							■	
M51232P	16																							■	
M51233P	22																							■	
M51240P	16																								■
M51242P	16																								■

●IC APPLICATION FOR COLOR TV SET



ORDERING INFORMATION

For Second Source Products

Example: **M 5 1 99 A Y**

M: Indicates the product is a Mitsubishi Electric integrated circuit.

5: Industrial/consumer
(Operating ambient temperature range is −20 to 75°C, standard)

9: High-reliability type

0: CMOS

1: Linear circuit

3: TTL

10~19: Linear circuit

32~33: TTL (equivalent to the TI SN74 family)

41~47: TTL, others

48~49: I^2L

84: CMOS

85: p-channel silicon gate MOS

86: p-channel aluminum gate MOS

87: n-channel silicon gate MOS

88: p-channel aluminum gate EDMOS

89: CMOS

S0~S2: Shottky TTL
(equivalent to the TI SN74S family)

This group consists of a two-digit serial number to indicate the type of circuit within the series.

Consists of a single letter which indicates the difference of outer appearance or some part of the device specifications as listed below.

(1) For linear circuits, this is one letter of the alphabet, chosen in alphabetical order but not including I or O, which is used to flag devices for which parts of the specifications differ.

(2) For devices with identical specifications having only pin bending direction differences, an R is assigned to this group.

(3) When this group designation is not required, the next group is shifted to the left to follow the group (4) immediately.

B: Resin sealed ceramic-type package

K: Low melting point glass sealed ceramic-type package

L: Plastic molded SIL (single in-line) package

P: Plastic molded DIL (dual in-line) package

S: Cermet package

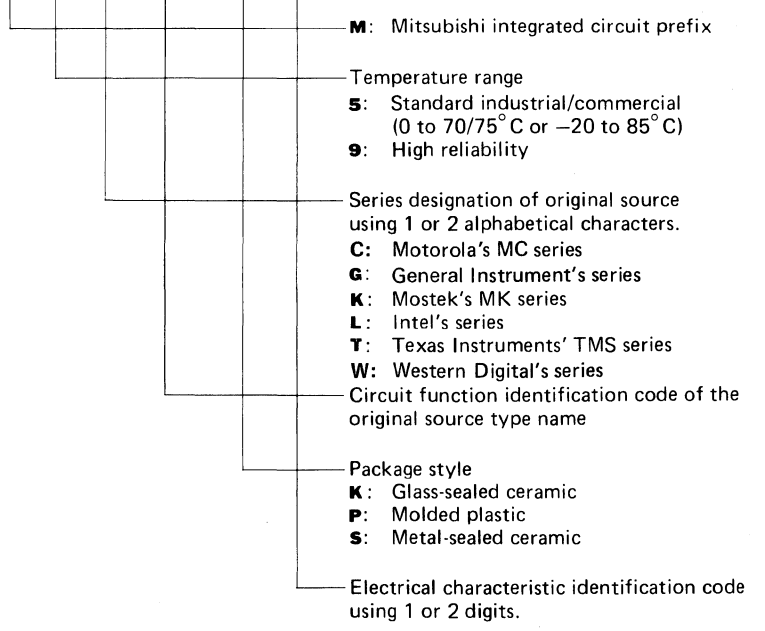
T: Can sealed glass-metal package
(similar to the TO-5 package)

Y: Can sealed glass-metal package
(similar to the TO-3 package)

ORDERING INFORMATION

For Second Source Products

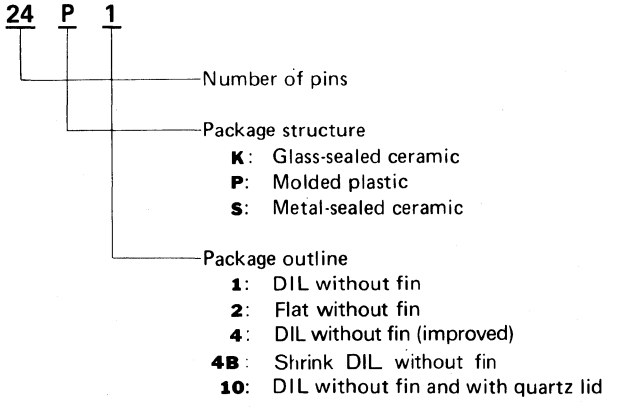
Example: M 5 K 4116 S – 2



PACKAGE CODE

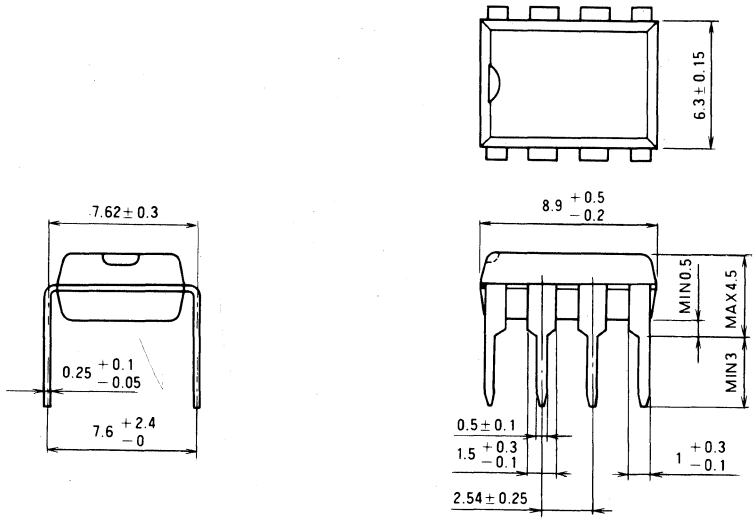
Package style may be specified by using the following simplified alphanumeric code.

Example: 24 P 1



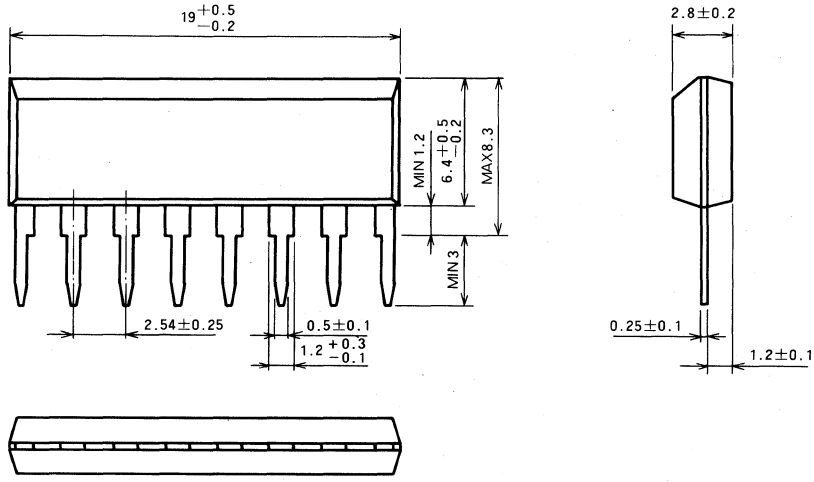
TYPE 8P4 8-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 8P5 8-PIN MOLDED PLASTIC SIL

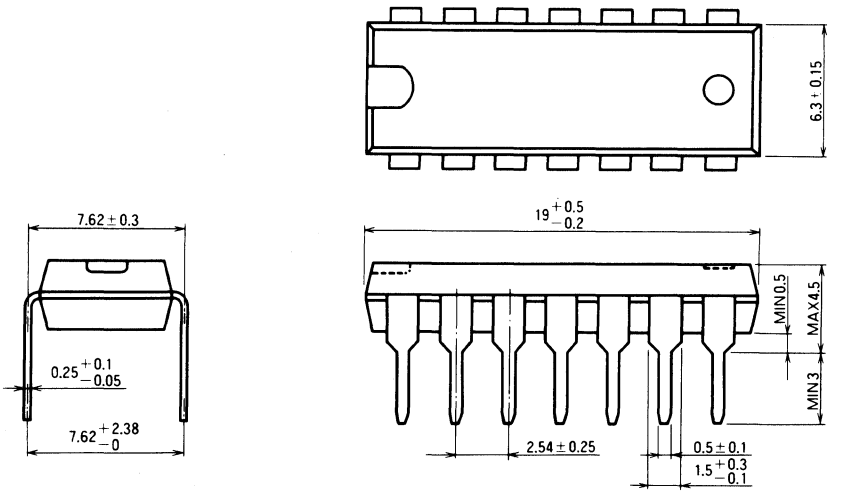
Dimension in mm



PACKAGE OUTLINES

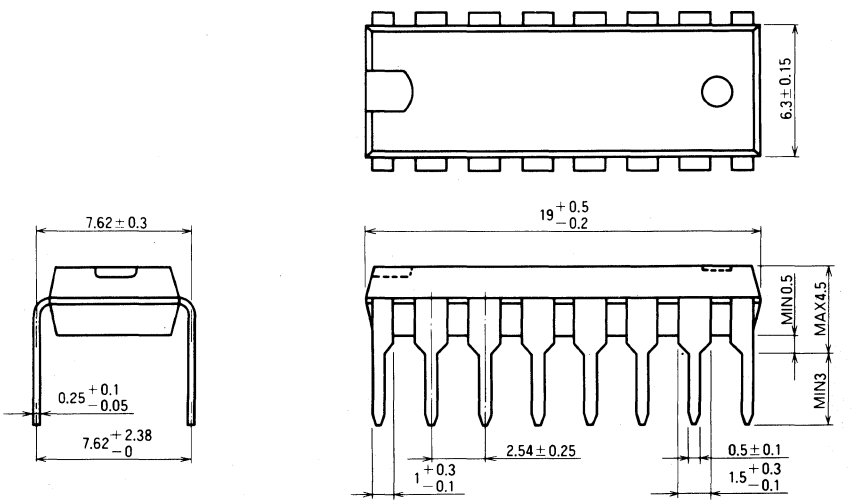
TYPE 14P4 14-PIN MOLDED PLASTIC DIL

Dimension in mm



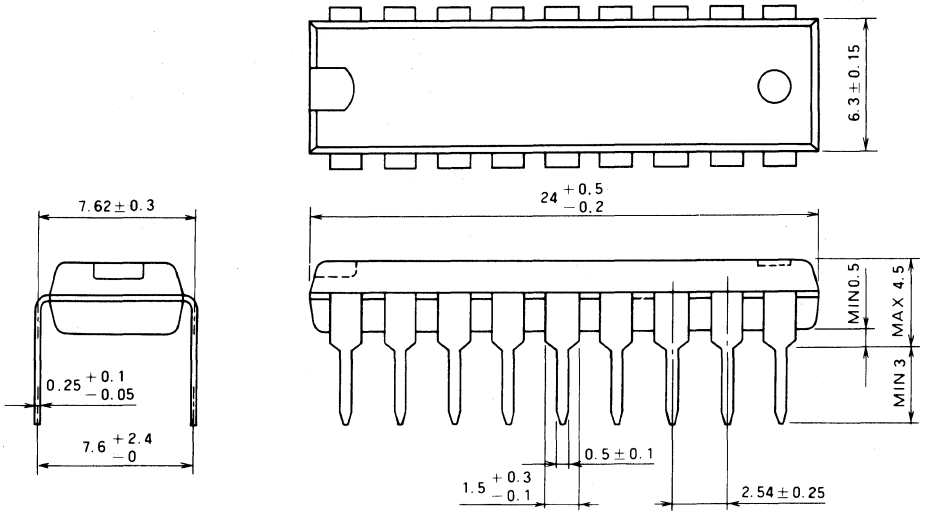
TYPE 16P4 16-PIN MOLDED PLASTIC DIL

Dimension in mm



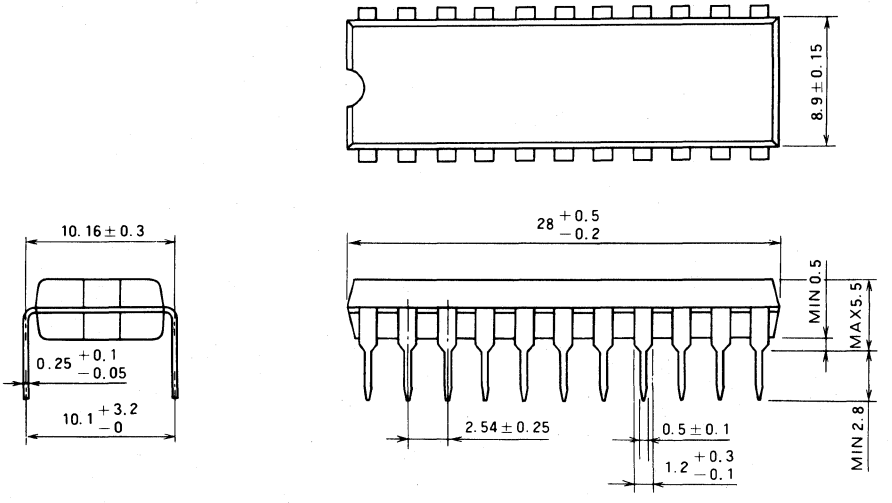
TYPE 18P4 18-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 22P1 22-PIN MOLDED PLASTIC DIL

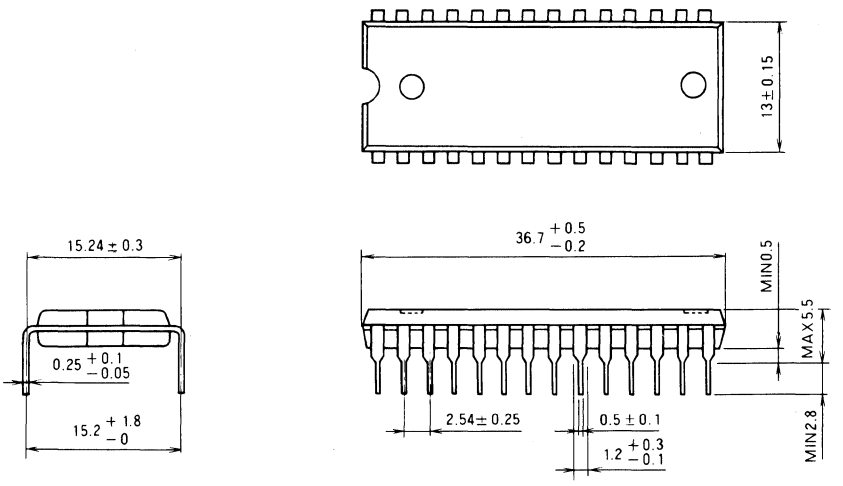
Dimension in mm



PACKAGE OUTLINES

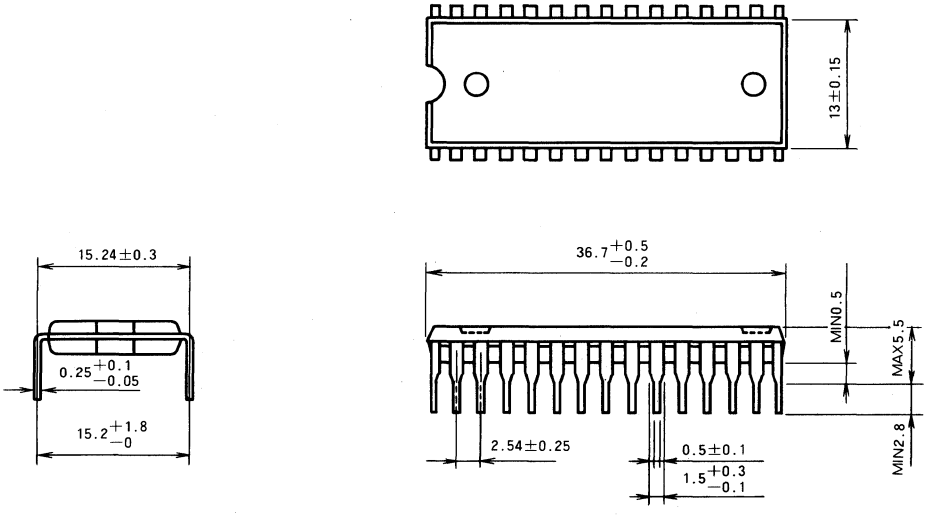
TYPE 28P4 28-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 30P4 30-PIN MOLDED PLASTIC DIL

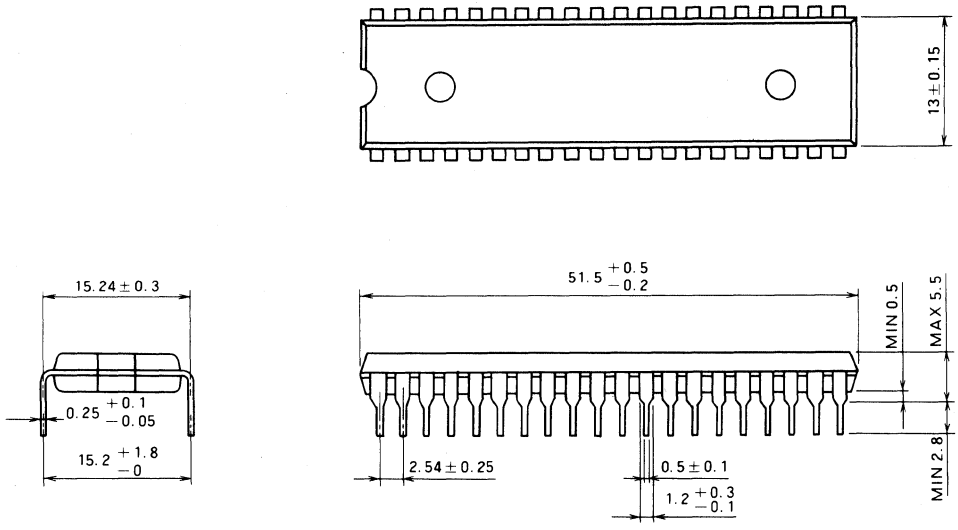
Dimension in mm



PACKAGE OUTLINES

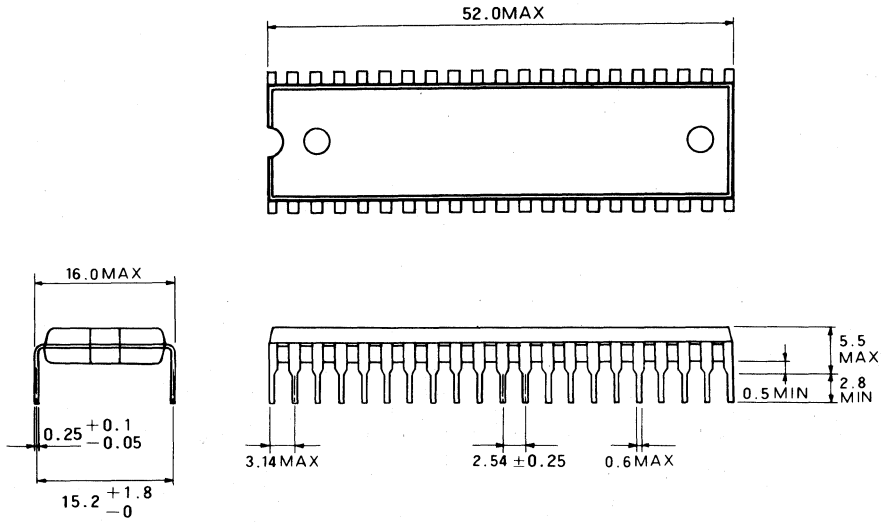
TYPE 40P1 40-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 42P1 42-PIN MOLDED PLASTIC DIL

Dimension in mm



MITSUBISHI ELECTRIC

QUALITY ASSURANCE AND RELIABILITY TESTING

1. INTRODUCTION

Recent years have seen rapid advancements in semiconductor integrated circuits in the areas of level of integration, speed, and other performance factors. Increasingly complex systems requiring higher reliability and the need to simplify assembly processes has resulted in a rapidly increasing demand for semiconductor integrated circuits. Accompanying this increased demand is the very serious problem of supplying customers with devices that operate with uniform quality. Mitsubishi Electric has developed the system of quality assurance described below as well as a system for controlling reliability, enabling the supply of highly reliable devices to customers. This system and the results of reliability testing will be described below in addition to an overview of the problems that face us in the future for the support of high semiconductor reliability.

2. QUALITY ASSURANCE SYSTEM

This system consists of a combination of design reliability and product quality and is summarized in Fig. 1, along with the procedures for evaluation of reliability.

2.1 Design Quality Assurance

This part of the quality assurance system is implemented by the following two methods.

(1) Investigations are performed of required device characteristics and quality by means of breadboarding with standardly available components.

(2) CAD technology is used to design the device according to established design standards.

2.2 Product Quality Assurance

Product quality assurance is implemented with the following controls and inspections.

(1) Environmental control

(2) Periodic inspection and preventative maintenance on equipment and measurement instruments used in design.

(3) Purchasing control

(4) Manufacturing process control

(5) Intermediate inspections: Wafer process and assembly

(6) Final inspections: Inspections of the finished product for outward appearance, dimensions, structure, and electrical characteristics to determine the device's pass or fail status.

(7) Quality assurance inspections: These inspections are performed from the standpoint of the end user to provide an overall verification of quality to judge whether the device will be placed in stock. The following groups of categories are used in this type of inspection:

Group A: Tests of outward appearance, markings and electrical characteristics

Group B: Tests of environmental mechanical life.

Group C: Reliability tests of samples made from lots that have passed the Group A and Group B tests. Testing is performed to determine life and includes environmental and mechanical testing and is performed every several months.

Table 1 Integrated Circuit Reliability Testing Categories and Conditions (examples)

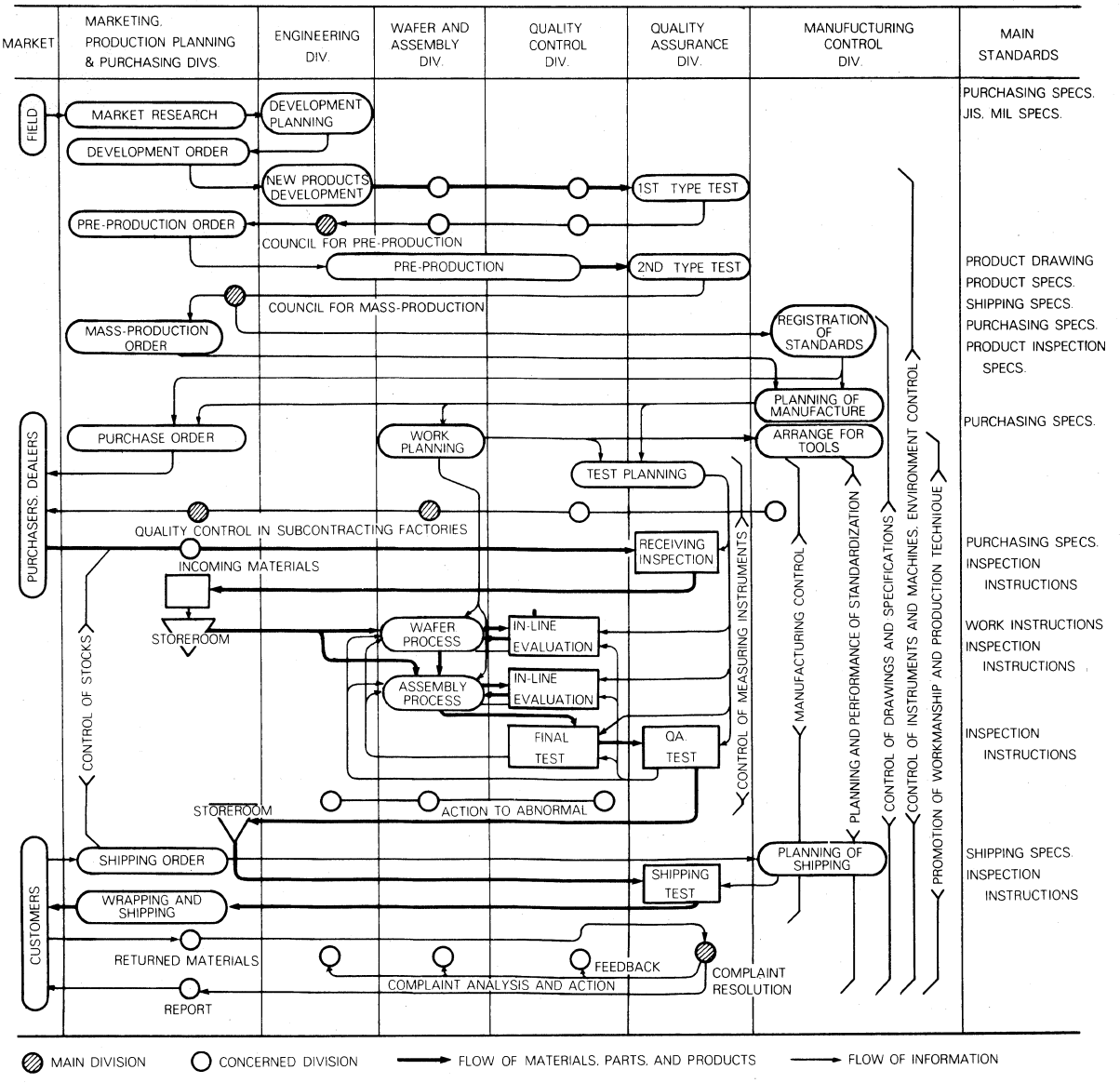
Group	Test category	Test conditions
1	Continuous operation	Maximum operating temperature for 1000h
	High-temperature storage	Maximum storage temperature for 1000h
	Resistance to humidity (storage)	65°C、95%RH、 500Hrs
2	Resistance to soldering heat	260°C、10Sec
	Thermal shock	0~100°C, 15 cycles, 10min/cycle
	Temperature cycling	Minimum – Maximum storage temperature, 10 cycles 1h/cycle
3	Solderability	230°C, 5s, using rosin flux
	Lead strength	Pulling: 340g, 30s Bending:225g, ±30°, 3 times
	Vibration	20G in X,Y, and Z directions, every 4 times, 100~2000Hz, 4min/cycle
	Shock	75cm, 3 times, on a wooden board, Y_1 direction
	Constant acceleration	20000G, Y_1 direction, 1min

Table 2 Integrated Circuit Failure Analysis Procedures

Step	Description
(1) External inspection	• Inspection of the condition of the leads, plating, soldering and bonding • Package material, sealing, and marking inspection • Inspection of other specified external features • Inspections using stereo and metallurgical microscopes, X-ray fluoroscopy, and fine leakage or gross leakage inspections are performed as required.
(2) Electrical inspection	• Determination of shorts, opens, and deteriorization in parameters by measurement of electrical parameters. • Observation of characteristics by means of oscilloscope and curves tracers, including physical characteristics observed indirectly by means of electrical characteristics. • If required, perform stress testing such as environmental and life testing.
(3) Internal inspection	• Open the package lid and optically inspect the device internally. • Observation of the surface of the silicon chip • When applicable, measurement of electrical characteristics using a probe. • If required, the application of SEM, XMA, or IR microscanning
(4) Chip analysis	• Metallurgical inspection and analysis to supplement the internal inspection analysis • Cross-sectioning of the chip • Analysis of flaws in the oxide layer • Analysis of flaws in the diffusion layer

QUALITY ASSURANCE AND RELIABILITY TESTING

Fig. 1 Quality assurance system



2.3 Reliability Evaluation Testing Used from the Development Prototype Phase through the Mass Production Phase

To verify the quality as described in sections 2.1 and 2.2 above, reliability evaluation is performed at three different stages of a product's life, development prototype, preproduction, and mass production.

In the development prototype stage, after a product has passed primary tests it advances to the preproduction stage at which some quantity of product is produced, after which secondary testing is performed to verify that the quality and reliability observed in the prototype has been maintained. In the mass production stage, a verification of quality and reliability is again performed, using the above described quality assurance testing procedures.

3. RELIABILITY CONTROL

3.1 Reliability Testing

Reliability certification is controlled on a worldwide basis by the IEC and locally in Japan by the Reliability Center of Japan (RCJ), operating in accordance with JIS standards to certify quality.

At Mitsubishi Electric, reliability testing is performed in accordance with such standards as MIL-STD-883 and EIAJ-IC-121 and is summarized in Table 1.

3.2 Failure Analysis

To improve the reliability of integrated circuits, the causes of failures encountered in reliability and accelerated testing are sought to provide feedback information for the improvement of process technology and the manufacturing function. Such failure analysis procedures are summarized in Table 2.

4. EXAMPLES OF RELIABILITY TEST AND FAILURE ANALYSIS RESULTS

4.1 Reliability Test Results

Linear ICs are widely used in audio and TV equipment and have been used with high reliability in these applications. Table 3 shows an example of the results of life testing of such linear ICs.

4.2 Example of Failure Analysis Results

Accelerated testing under conditions more severe than those encountered in normal operation is used to observe failures caused by moisture, wire bonding failures, and those caused when surge voltages cause damage or failures of vapor-deposited aluminum conductors. Typical results are shown below.

(1) Failures Caused by Moisture

An example of the results of steam pressure testing performed to evaluate moisture resistance of a plastic molded package is shown in Fig. 2. The vapor-deposited aluminum conductor was dissolved by moisture which penetrated the package.

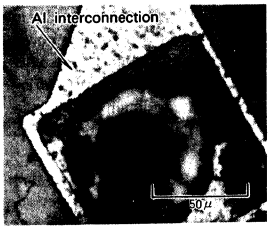


Fig. 2 Example of corrosion of an aluminum vapor-deposited conductor (analyzed using a metallurgical microscope)

Table 3 Examples of Linear IC Endurance Test Results

Application	Type No.	Package	Test category and conditions		Number of samples	Component hours	Number of failures	Type of failure
Audio	M51011P	14-pin plastic molded DIL	Operating life	75℃	45	45,000	0	
			High-temperature storage	125℃	45	45,000	0	
	M51521L	8-pin plastic molded SIL	Operating life	75℃	22	22,000	0	
			High-temperature storage	125℃	22	22,000	0	
	M51530L	16-pin plastic molded ZIL	Operating life	75℃	22	22,000	0	
			High-temperature storage	125℃	22	22,000	0	
	M51516L	9-pin plastic molded SIL	Operating life	75℃	48	48,000	0	
			High-temperature storage	125℃	50	50,000	0	
TV	M5186P	22-pin plastic molded DIL	Operating life	75℃	22	22,000	0	
			High-temperature storage	125℃	22	22,000	0	
	M5193P	22-pin plastic molded DIL	Operating life	75℃	22	22,000	0	
			High-temperature storage	125℃	22	22,000	0	
	M5195P	16-pin plastic molded DIL	Operating life	75℃	22	22,000	0	
			High-temperature storage	125℃	22	22,000	0	
Others	M51903L	8-pin plastic molded SIL	Operating life	75℃	22	22,000	0	
			High-temperature storage	125℃	22	22,000	0	
	M51202L	5-pin plastic molded SIL	Operating life	75℃	22	22,000	0	
			High-temperature storage	125℃	22	22,000	0	
	M51231P	16-pin plastic molded DIL	Operating life	75℃	45	45,000	0	
	M51848P	8-pin plastic molded DIL	Operating life	75℃	22	22,000	0	
			High-temperature storage	125℃	22	22,000	0	

(2) Wire Bonding Failures

Fig. 3 shows an example of a failure occuring during the operational temperature cycling testing for evaluating the reliability of the wire bonding of the ICs inner leads. The cause of this failure is thought to be the opening of an internal lead bond due to the difference in thermal expansion coefficients of metal and resin, resulting in stress being applied to the inner lead.

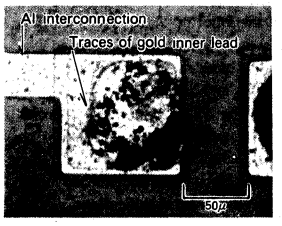


Fig. 3 Lift off of gold inner lead (analyzed using a metallurgical microscope)

Fig. 4 Surge destruction example (analyzed using a metallurgical microscope)

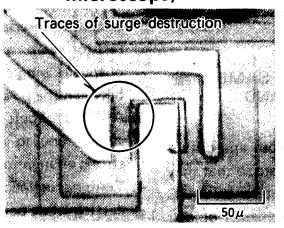


Fig. 5 Enlarged view of Fig. 4 aluminum bridge (analyzed using XAM-A1Kα)

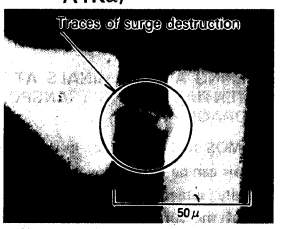


Fig. 6 Hot spot at the bonding head (analyzed using an infrared microscanner)

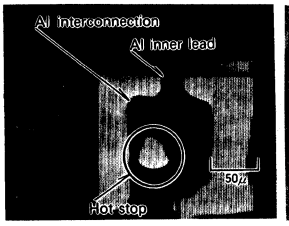
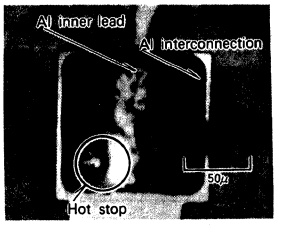


Fig. 7 The junction of Fig. 6 after removal of aluminum (analyzed using a metallurgical microscope)



(3) Failures Due to Surge Voltages

Many integrated circuits fail in the field due to the application of surge voltages. Surge voltage margin tests have been performed to reproduce this type of failure to allow analysis of this type of destruction and development of suitable protection.

Examples of failures occuring during such tests are shown in Fig. 4~7. In Fig. 4 and 5, the presence of a bridge was verified by means of an X-ray microscanner, while the hot spot shown in Fig. 6 and 7 was verified using an infrared microscanner.

(4) Failures of Aluminum Vapor-Deposited Interconnections

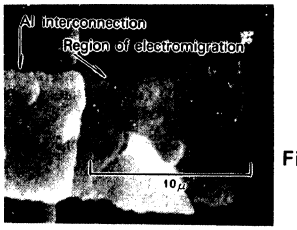


Fig. 8 Electromigration of an aluminum interconnection (analyzed using an SEM)

Fig. 8 shows an open circuit vapor-deposited aluminum interconnection, in a high current density region, caused by the operating life test. This test is performed as a step stress test to investigate IC deteriorization and failure caused by temperature and voltage stresses. This phenomenon is due to aluminum electromigration, which is observed when high-current loads are applied to a vapor-deposited aluminum interconnection.

5. SUMMARY

We have discussed the concepts of the Mitsubishi Electric quality assurance system and reliability control methods. The demands for high reliability integrated circuits will be increasing in the future. To anticipate and meet these new, more severe demands, as a manufacturer of integrated circuits, Mitsubishi Electric is making efforts in the following areas:

(1) Cooperation with device users in establishing quality levels, including those for reliability.
(2) The establishment of thorough reliability testing centered on evaluation of wafer and assembly and the feedback of information gained in such testing to create design standards and product standards.
(3) Facilitation of the achievement of reliability by means of improvements in failure analysis and accelerated life testing methods.
(4) Establishment of a system of collecting data on failures in the field and the use of this data in improving reliability.

To improve IC reliability even further, Mitsubishi Electric is continuing to make efforts with the cooperation of its users in system design, setting of quality levels, performing of incoming inspections, controlling the assembly and adjustment phase of IC equipment production and in the collection of field data essential to the improvement of device reliability.

LINEAR ICs for VIDEO SYSTEMS

2

M51231P

TOUCH-TYPE ELECTRONIC CHANNEL SELECTOR

DESCRIPTION

The M51231P is a semiconductor integrated circuit consisting of a touch-type selection control circuit. It is designed for use in color and black-and-white TV tuners and includes a touch amplifier, channel memory, display drive circuit, and up/down control circuit for each of four channels. In addition to use in TV circuits, it has applications in other consumer and industrial equipment for touch switch control.

FEATURES

- High breakdown voltage output circuit ..... 45V (Rated)
- Can be cascaded to increase number of channels
- Built-in up/down shifting function
- Usable for remote control

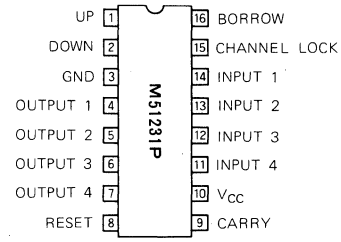
APPLICATION

Color and black-and-white TV, VTR, stereo and other radio receivers

RECOMMENDED OPERATING CONDITIONS

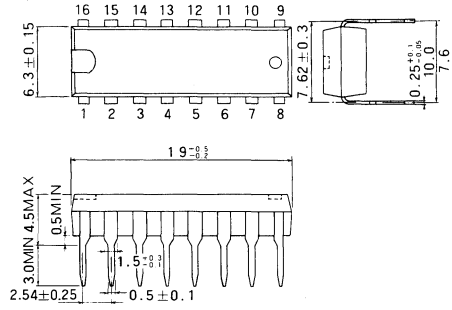
Supply voltage range ..... 5~7V
Rated supply voltage 5V

PIN CONFIGURATION (TOP VIEW)



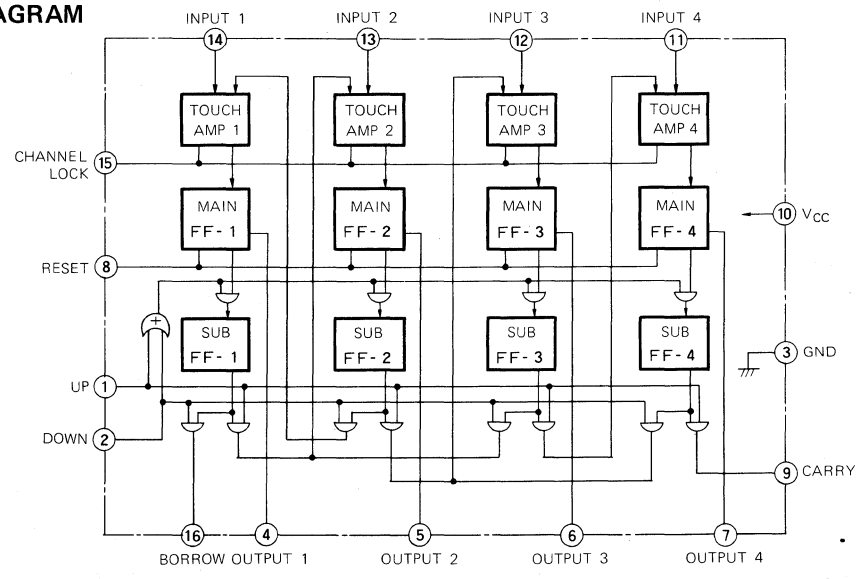
PACKAGE OUTLINE

Dimensions in mm



16-pin plastic DIL package

BLOCK DIAGRAM



TOUCH-TYPE ELECTRONIC CHANNEL SELECTOR

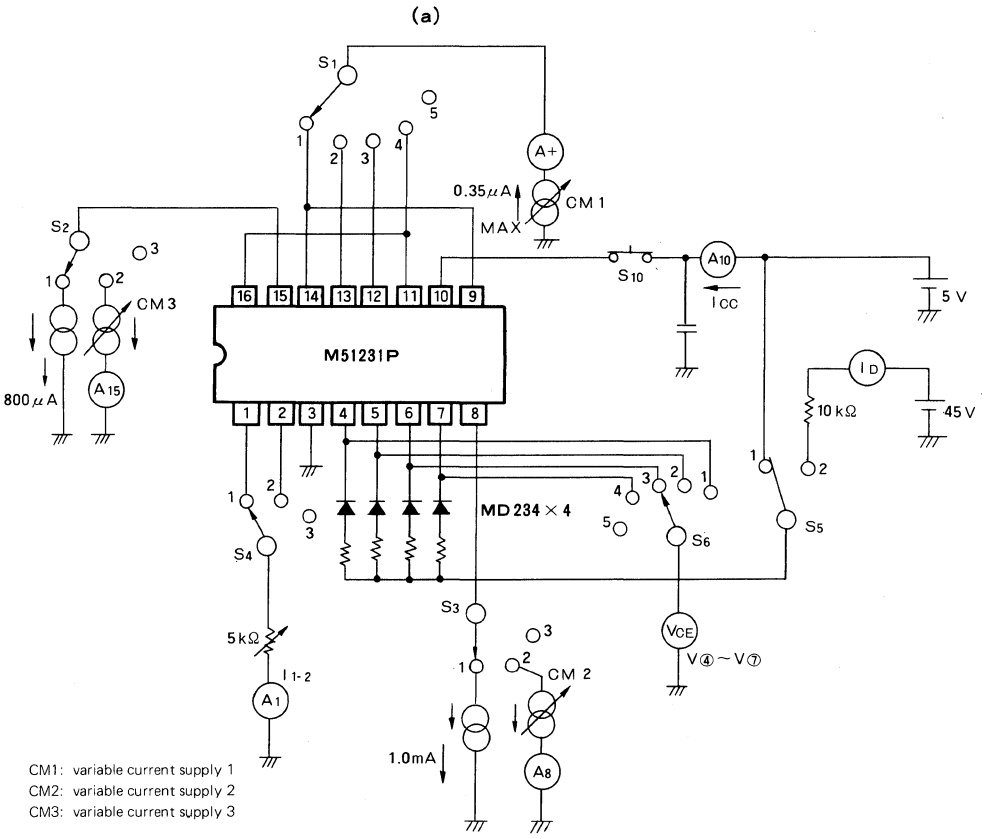
ABSOLUTE MAXIMUM RATINGS (Ta=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		10	V
V_O	Output terminal breakdown voltage	Pins ④⑤⑥⑦	45	V
I_O	Output load current	Pins ④⑤⑥⑦	50	mA
Pd	Power dissipation		700	mW
K_θ	Derating	Ta≧25°C	7	mW/°C
Topr	Operating temperature		−20～+75	°C
Tstg	Storage temperature		−40～+125	°C

ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{CC}=5V)

Symbol	Parameter	Test conditions	Test Circuit	Limits			Unit
				Min	Typ	Max	
$I_{⑩}$-OFF	Circuit current	All channels off	(a)	1.3	2.5	3.7	mA
$I_{⑩}$-ON	Circuit current	Only 1 channel on	(a)	3.7	6.7	10	mA
I_I	Input current (pins⑪, ⑫, ⑬, ⑭)	Input amplifier not saturated	(a)			0.35	μA
$I_⑧$	Reset terminal (trigger current)		(a)	0.55	0.74	0.95	mA
$I_⑮$	Channel lock terminal (trigger current)		(a)	0.43	0.60	0.72	mA
V_{CE}	Output saturation voltage (pins④,⑤,⑥,⑦)		(a)			120	mV
I_D	Output leakage current (pins④, ⑤, ⑥, ⑦)		(a)			5	μA
I_S	Shift trigger current (pins①, ②)		(a)	0.37	0.57	0.77	mA
$V_⑩$	Operating supply voltage			4.5	5	8	V
$\partial V_{CE}/\partial T$	Output voltage temperature coefficient	I_C=5mA				0.3	mV/°C

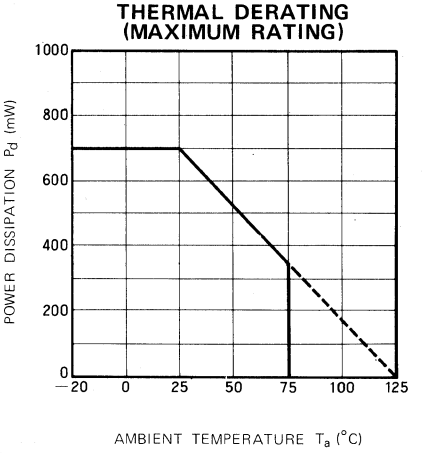
TEST CIRCUIT



TEST METHODS

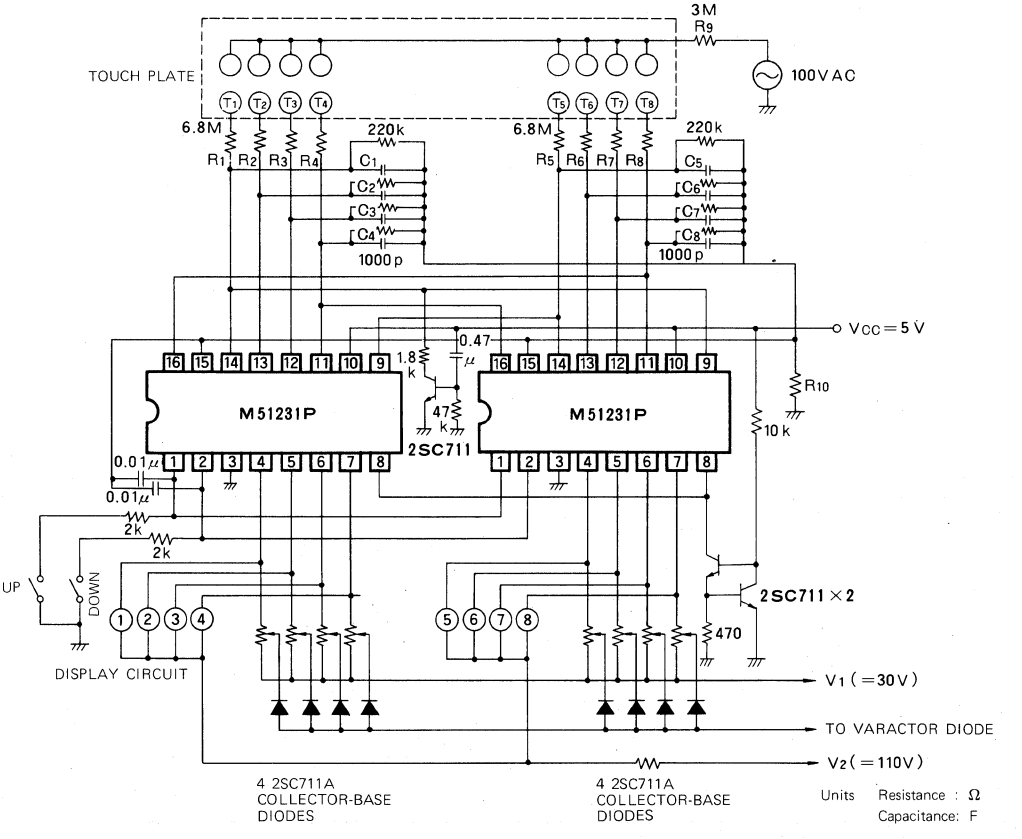
Sequence	Symbol	S_1	S_2	S_3	S_4	S_5	S_6	Test instrument
1	$I_{⑩\text{-OFF}}$	5	3	1	3	1	5	A_{10}
2	$I_{⑩\text{-ON}}$	1~4 *	1	1	3	1	5	A_{10}
3	I_I	1~4 *	1	1	3	1	5	A_+
4	$I_⑧$	1~4 *	1	2	3	1	5	A_8
5	$I_⑮$	1~4 *	2	1	3	1	5	A_{15}
6	V_{CE}	1~4 *	1	1	3	1	1~4 *	V_{CE}
7	I_D	5	1	3	3	2	5	I_D
8	I_{S1}	1~4 *	1	1	1	1	5	A_1
9	I_{S2}	1~4 *	1	1	2	1	5	A_1

* S_1 through S_6 are switched and all channels 1, 2, 3, 4 tested.



APPLICATION EXAMPLE

8-channel touch selector circuit



M51232P

TOUCH-TYPE ELECTRONIC CHANNEL SELECTOR

DESCRIPTION

The M51232P is a semiconductor integrated circuit consisting of a touch-type electronic channel selector designed for use in electronic tuners for color and black-and-white TV sets.

The M51232P consists of touch amplifiers, channel memories, display drivers and up/down shift circuits for each of 4 channels. It can also be used in various other types of consumer and industrial equipment.

FEATURES

- Incorporates a high sensitivity PNP input circuit.
- The output circuit has a high breakdown voltage.
  ····· 45V (max rated)
- The number of controllable channels can be increased by cascading multiple M51232Ps.
- Incorporates an up/down shift function.
- Compatible with remote control applications.

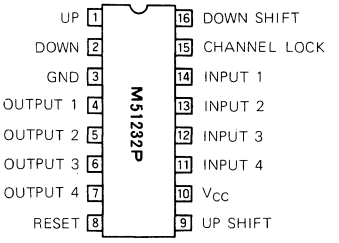
APPLICATION

Color TVs, VTRs, radios, stereos, etc.

RECOMMENDED OPERATING CONDITIONS

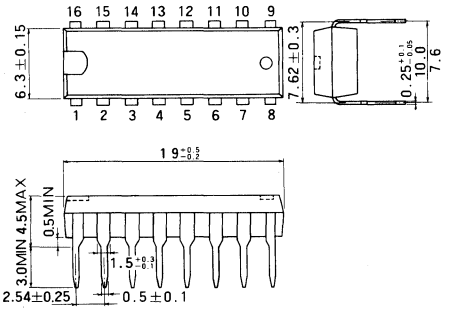
Supply voltage range ..... 13 ~ 17V
Rated supply voltage 15V

PIN CONFIGURATION (TOP VIEW)



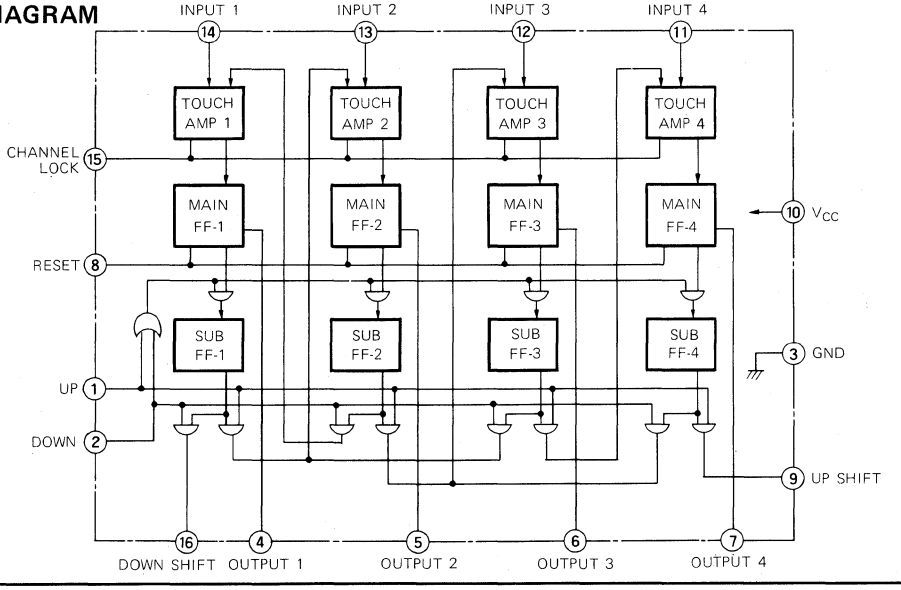
PACKAGE OUTLINE

Dimensions in mm



16-pin plastic DIL package

BLOCK DIAGRAM



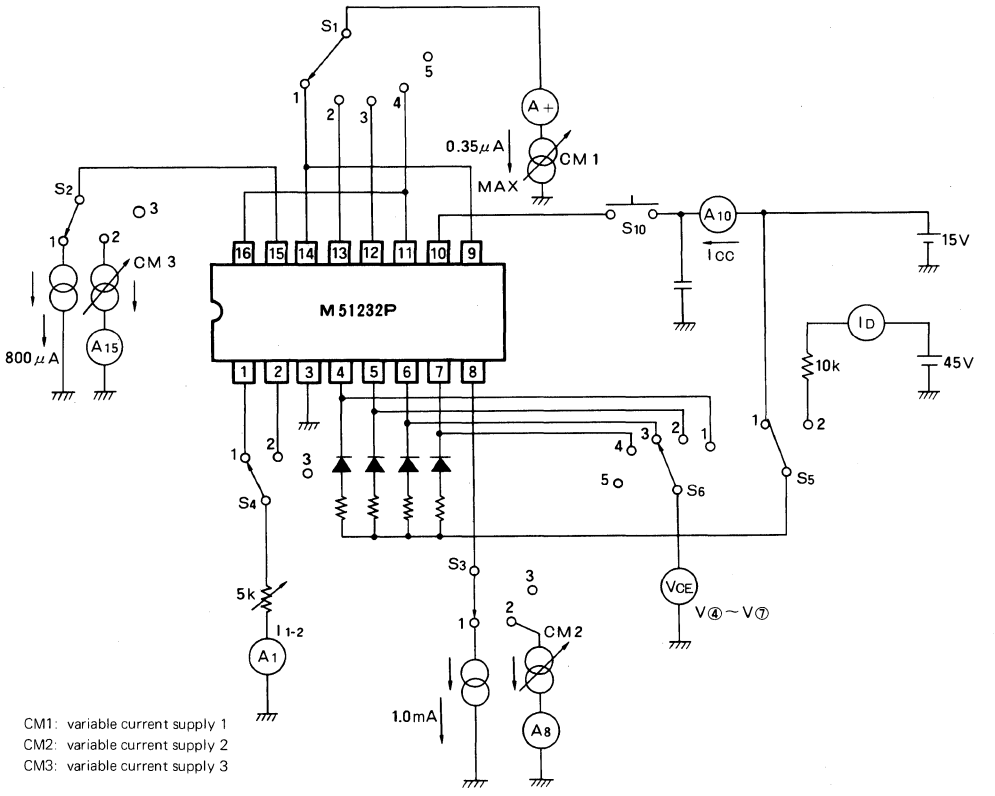
ABSOLUTE MAXIMUM RATINGS (Ta=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		18	V
V_O	Output terminal breakdown voltage	Pins ④⑤⑥⑦	45	V
I_O	Output load current	Pins ④⑤⑥⑦	50	mA
Pd	Power dissipation		700	mW
K_θ	Derating	Ta≧25°C	7	mW/°C
Topr	Operating temperature		−20～+75	°C
Tstg	Storage temperature		−40～+125	°C

ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{CC}=15V)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I⑩-OFF	Circuit current	All channels off	3.5	5.5	8.50	mA
I⑩-ON	Circuit current	Only 1 channel on	6.4	10.5	17.0	mA
I_I	Input current (pins ⑪, ⑫, ⑬, ⑭)	Input amplifier not saturated			0.35	μA
I⑧	Reset terminal (trigger current)		0.55	0.74	0.95	mA
I⑮	Channel lock terminal (trigger current)		0.43	0.60	0.72	mA
V_{CE}	Output saturation voltage (pins ④, ⑤, ⑥, ⑦)	Load current = 5 mA			120	mV
I_D	Output leak current (pins ④, ⑤, ⑥, ⑦)				5	μA
I_S	Shift trigger current (pins ①, ②)		0.37	0.57	1.00	mA
V⑩	Operating supply voltage		12.0	15.0	18.0	V
$\partial V_{CE}/\partial T$	Output voltage temperature coefficient	Load current = 5 mA			0.3	mV/°C

TEST CIRCUIT



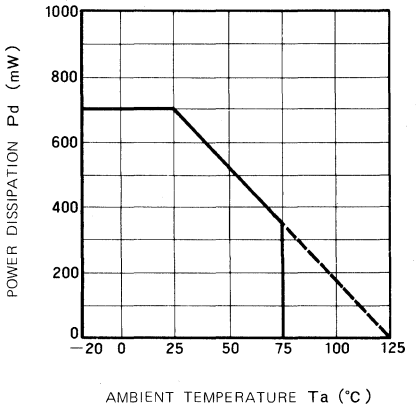
CM1: variable current supply 1
CM2: variable current supply 2
CM3: variable current supply 3

TEST METHODS

Sequence	Symbol	S_1	S_2	S_3	S_4	S_5	S_6	Test instrument
1	I⑩-OFF	5	3	1	3	1	5	A_{10}
2	I⑩-ON	1~4 *	1	1	3	1	5	A_{10}
3	I_I	1~4 *	1	1	3	1	5	A_+
4	I⑧	1~4 *	1	2	3	1	5	A_8
5	I⑮	1~4 *	2	1	3	1	5	A_{15}
6	V_{CE}	1~4 *	1	1	3	1	1~4 *	V_{CE}
7	I_D	5	1	3	3	2	5	I_D
8	I_{S1}	1~4 *	1	1	1	1	5	A_1
9	I_{S2}	1~4 *	1	1	2	1	5	A_1

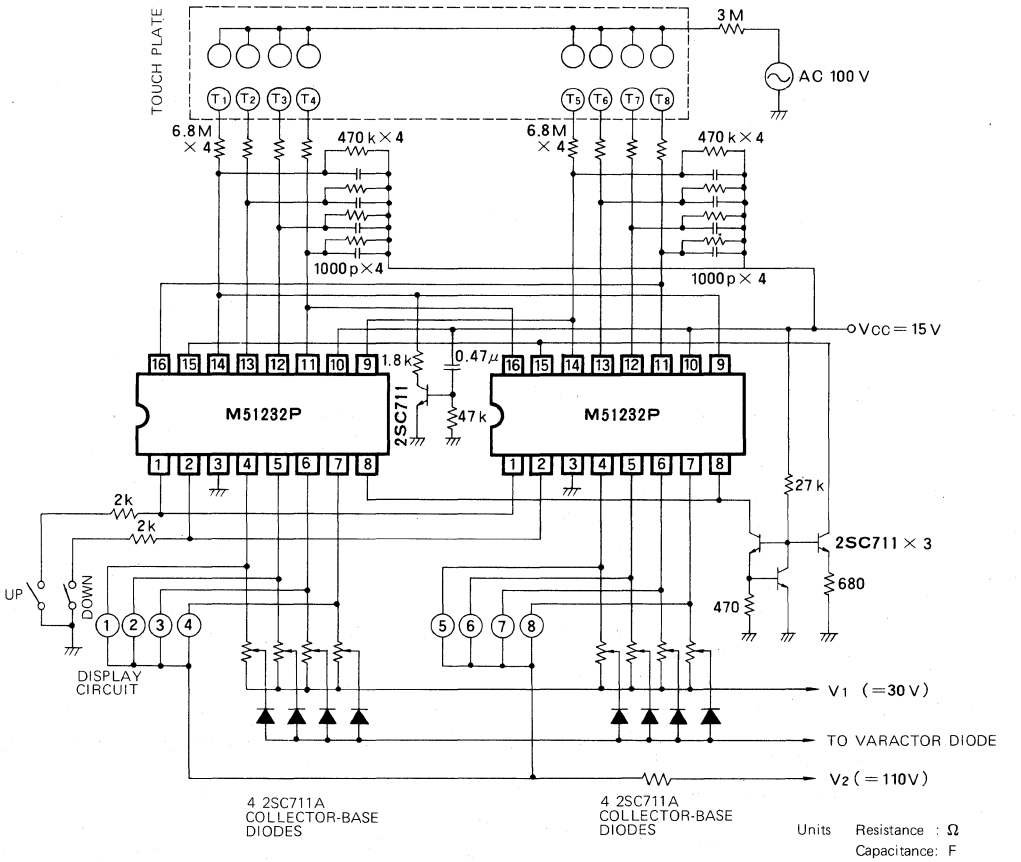
* S_1 through S_6 are switched and all channels 1, 2, 3, 4 tested.

THERMAL DERATING
(MAXIMUM RATING)



APPLICATION EXAMPLE

8-channel touch selector circuit



MITSUBISHI ELECTRIC

M51233P

SOFT-TYPE ELECTRONIC CHANNEL SELECTOR

DESCRIPTION

The M51233P is a semiconductor integrated circuit consisting of a soft-type electroric channel selector. It is designed for use in color TV and radio receiver electronic tuners for selection of up to 12 channels. The circuit is housed in a 22-pin plastic DIL package.

FEATURES

- Built-in Zener diode voltage regulation ..... 5.5V (typ
- Low power consumption ..... I_{CC}=20mA, typical (including 10mA Zener current)
- Up/down shifting
- Built-in channel shift oscillator
- Built-in initialization circuit
- Built-in AFT defeat pulse driver (open collector output)
- Common input/output pins

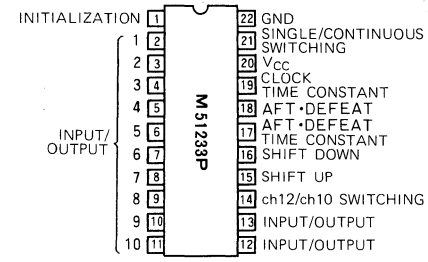
APPLICATION

TV and audio equipment

RECOMMENDED OPERATING CONDITIONS

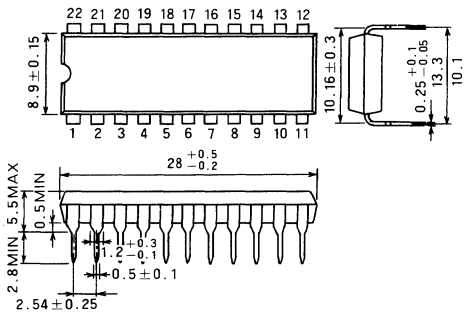
Rated supply voltage ..... I_{CC}=30mA

PIN CONFIGURATION (TOP VIEW)



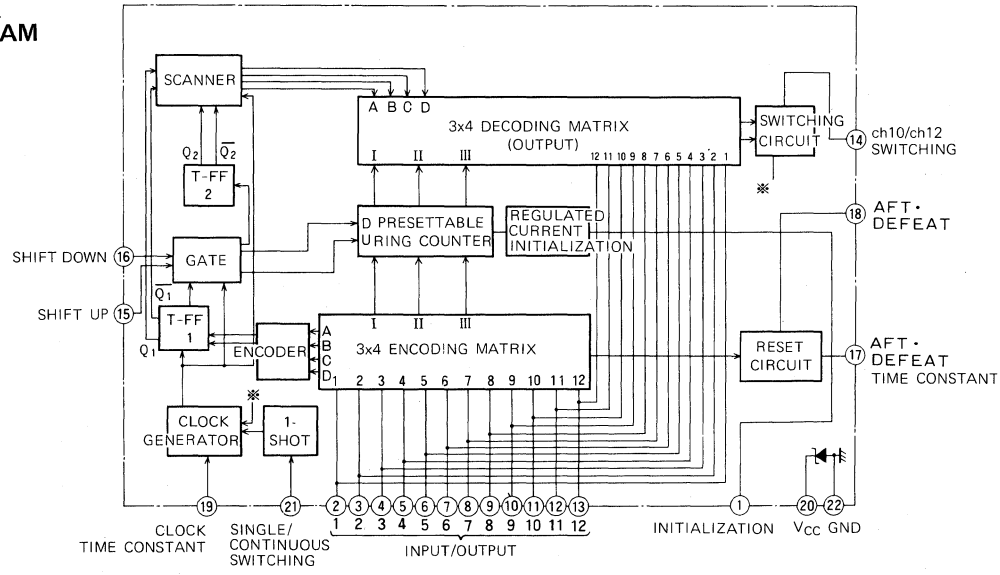
PACKAGE OUTLINE

Dimensions in mm



22-pin plastic DIL package

BLOCK DIAGRAM



SOFT-TYPE ELECTRONIC CHANNEL SELECTOR

ABSOLUTE MAXIMUM RATINGS (Ta=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
I_{CC}	Circuit current		70	mA
$V_{D①}$	Pin ① reverse DC voltage		45	V
$V_{D①}$	Input/output pin reverse DC voltage	Pin ⓘ (i=2~13)	45	V
$V_{D⑱}$	Pin ⑱ reverse DC voltage		30	V
$V_{P①}$	Pin ① reverse pulse voltage	Pulse width 5μs	60	V
$V_{P①}$	Input/output pin reverse pulse voltage	Pulse width 5μs, pin ⓘ (i=2~13)	60	V
$I_{D①}$	Input/output pin DC current	Pin ⓘ (i=2~13)	50	mA
$I_{D⑱}$	Pin ⑱ DC current		10	mA
$V_{D⑭}$	Pin ⑭ DC voltage		$V_{⑳}$	V
$V_{D⑮}$	Pin ⑮ DC voltage		$V_{⑳}$	V
$V_{D⑯}$	Pin ⑯ DC voltage		$V_{⑳}$	V
$V_{D⑰}$	Pin ⑰ DC voltage	1kΩ between applied voltage and pin ⑰	$V_{⑳}$	V
$V_{D⑲}$	Pin ⑲ DC voltage	1kΩ between applied voltage and pin ⑲	$V_{⑳}$	V
$V_{D㉑}$	Pin ㉑ DC voltage		$V_{⑳}$	V
$I_{D①}$	Pin ① DC current		10	mA
Pd	Power dissipation		1.4	W
K_θ	Derating	Ta≧25°C	14	mW/°C
Topr	Operating temperature		−20~+75	°C
Tstg	Storage temperature		−40~+125	°C

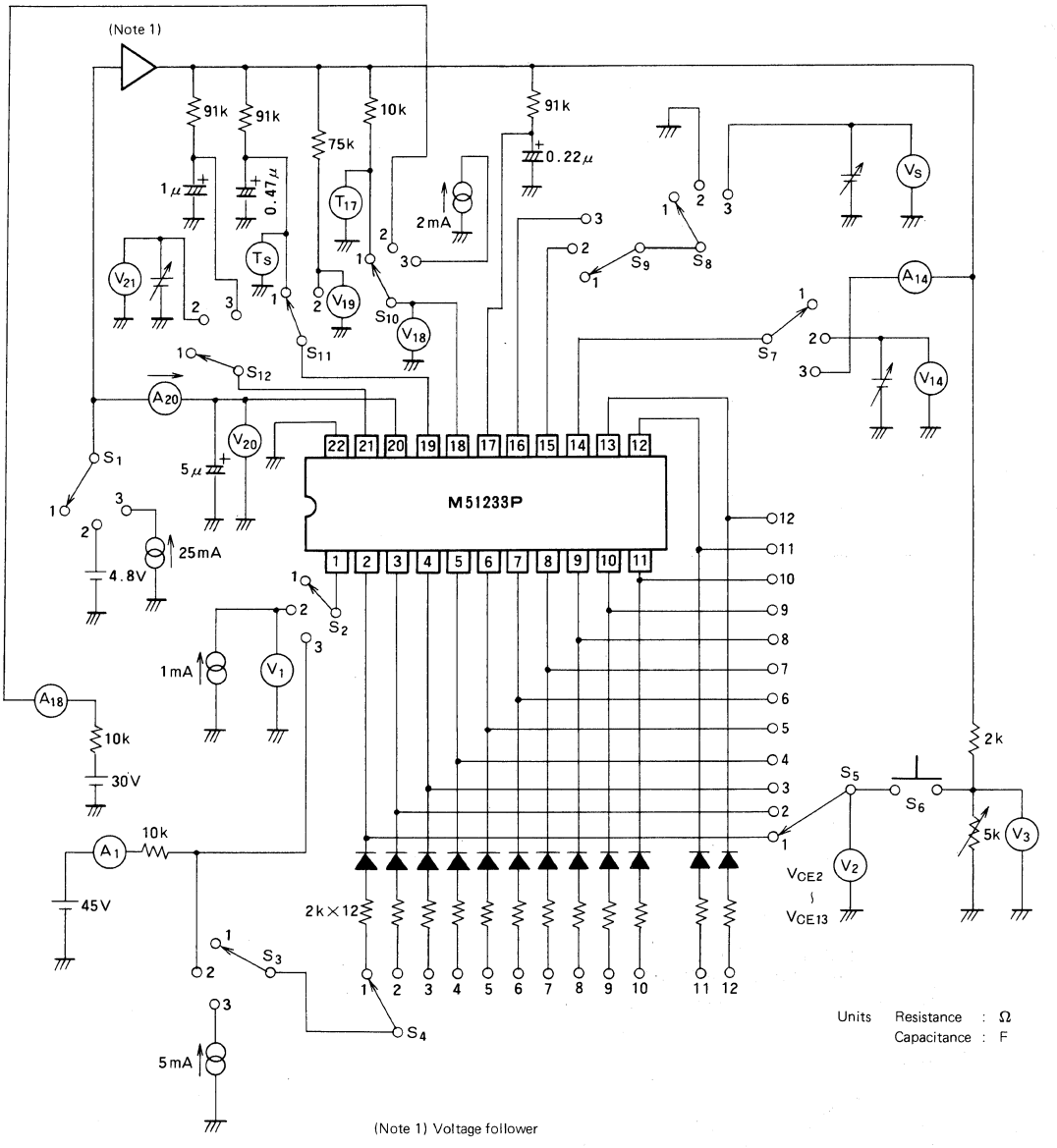
Note. $V_{⑳}$ is the voltage at pin ⑳

ELECTRICAL CHARACTERSTICS (Ta=25°C, Vcc=4.8V)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$I_{⑳}$ OFF	Circuit current (off)		3.0	6.5	13.0	mA
$I_{⑳}$ ON	Circuit current (on)		4.5	9.7	20.0	mA
$V_{CE①}$	Pin ① saturation voltage				700	mV
$V_②$	Pin ② trigger voltage		0.3		2.5	V
$V_③$	Pin ③ trigger voltage		0.3		2.5	V
$V_④$	Pin ④ trigger voltage		0.3		2.5	V
$V_⑤$	Pin ⑤ trigger voltage		0.3		2.5	V
$V_⑥$	Pin ⑥ trigger voltage		0.3		2.5	V
$V_⑦$	Pin ⑦ trigger voltage		0.3		2.5	V
$V_⑧$	Pin ⑧ trigger voltage		0.3		2.5	V
$V_⑨$	Pin ⑨ trigger voltage		0.3		2.5	V
$V_⑩$	Pin ⑩ trigger voltage		0.3		2.5	V
$V_⑪$	Pin ⑪ trigger voltage		0.3		2.5	V
$V_⑫$	Pin ⑫ trigger voltage		0.3		2.5	V
$V_⑬$	Pin ⑬ trigger voltage		0.3		2.5	V
$V_⑮$	Shift trigger voltage — Pin ⑮ voltage		0.5		2.0	V
$V_⑯$	Shift trigger voltage — Pin ⑯ voltage		0.5		2.0	V
$V_⑳$	Pin ⑳ Zener voltage		5.0	5.5	6.0	V
$V_㉑$	Pin ㉑ trigger voltage		2.1		4.2	V

MITSUBISHI ELECTRIC

TEST CIRCUIT

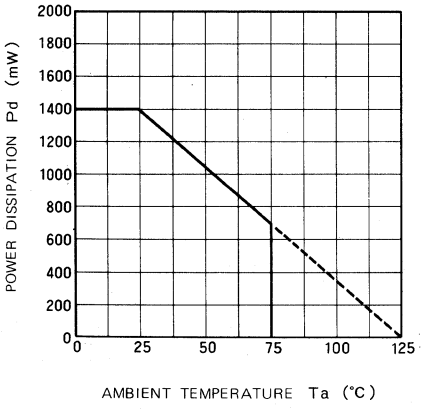


(Note 1) Voltage follower

TEST METHODS

Symbol	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}	Test instrument
$I_{⑳}$ (OFF)	2	1	1	—	—	OFF	1	1	—	1	1	1	A_{20}
$I_{⑳}$ (ON)	2	1	1	1～12	1～12	ON	1	1	—	1	1	1	A_{20}
$V_{CE①}$	1→3	2	1	—	—	OFF	1	1	—	1	1	1	V_1
$V_{②}$	3	1	3	2→1	2→1	ON	1	1	—	1	1	1	V_3
$V_{③}$	3	1	3	1→2	1→2	ON	1	1	—	1	1	1	V_3
$V_{④}$	3	1	3	2→3	2→3	ON	1	1	—	1	1	1	V_3
$V_{⑤}$	3	1	3	3→4	3→4	ON	1	1	—	1	1	1	V_3
$V_{⑥}$	3	1	3	6→5	6→5	ON	1	1	—	1	1	1	V_3
$V_{⑦}$	3	1	3	5→6	5→6	ON	1	1	—	1	1	1	V_3
$V_{⑧}$	3	1	3	6→7	6→7	ON	1	1	—	1	1	1	V_3
$V_{⑨}$	3	1	3	7→8	7→8	ON	1	1	—	1	1	1	V_3
$V_{⑩}$	3	1	3	10→9	10→9	ON	1	1	—	1	1	1	V_3
$V_{⑪}$	3	1	3	9→10	9→10	ON	1	1	—	1	1	1	V_3
$V_{⑫}$	3	1	3	10→11	10→11	ON	1	1	—	1	1	1	V_3
$V_{⑬}$	3	1	3	11→12	11→12	ON	1	1	—	1	1	1	V_3
$V_{⑮}$	3	1	3	1～12	1→12	ON	1	1→3	2	1	1	3	V_S
$V_{⑯}$	3	1	3	12～1	12～1	ON	1	1→3	3	1	1	3	V_S
$V_{⑳}$	3	1	1	—	—	OFF	1	1	—	1	1	1	V_{20}
$V_{㉑}$	3	1	1	—	—	OFF	1	2	2	1	2	2	V_{21}

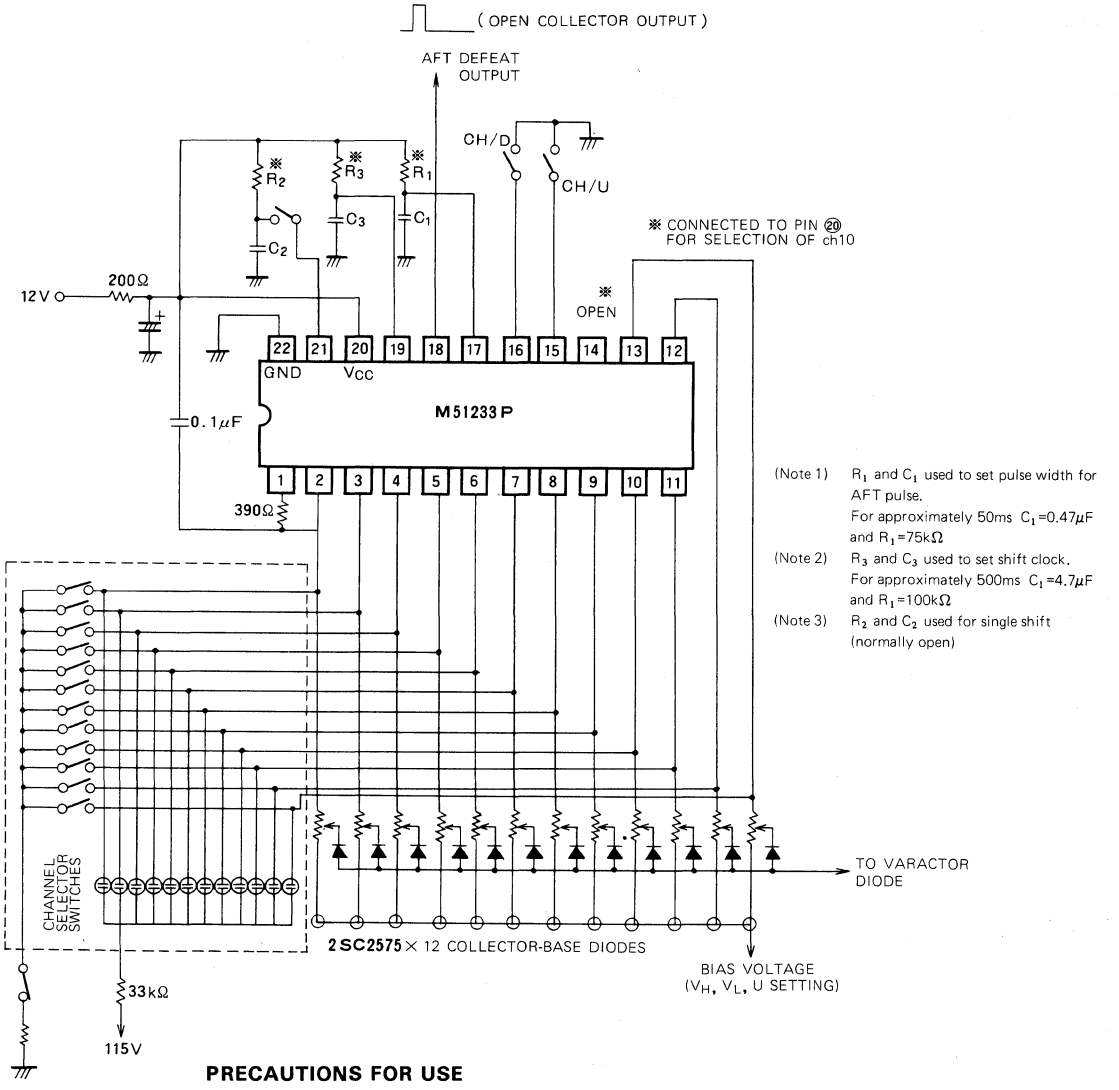
THERMAL DERATING (MAXIMUM RATING)



SOFT-TYPE ELECTRONIC CHANNEL SELECTOR

APPLICATION EXAMPLE

SOFT-TYPE SWITCH 12 CHANNEL SELECTOR CIRCUIT



(Note 1) R_1 and C_1 used to set pulse width for AFT pulse.
For approximately 50ms C_1=0.47μF and R_1=75kΩ

(Note 2) R_3 and C_3 used to set shift clock.
For approximately 500ms C_1=4.7μF and R_1=100kΩ

(Note 3) R_2 and C_2 used for single shift (normally open)

PRECAUTIONS FOR USE

Pin ⑳ should not be subjected to voltage over 5V.
For use of voltages over 5V, a dropping resistance must be used.

M51240P

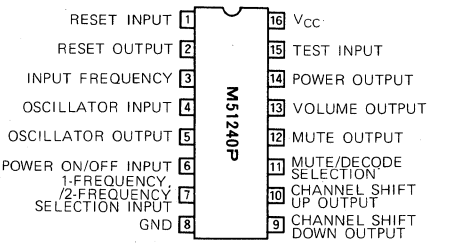
6-FUNCTION REMOTE CONTROL RECEIVER

DESCRIPTION

The M51240P is a semiconductor integrated circuit consisting of a circuit designed to provide 6 function remote control for color TVs and audio equipment. The circuit digitally detects 6 signal frequencies and provides 6 different outputs according to the input frequency. This frequency detection method is used to control power on/off, channel shift up, channel shift down, volume up, volume down and muting functions.

A digital low-pass filter is used to eliminate the effects of noise and provide stable operation.

PIN CONFIGURATION (TOP VIEW)



FEATURES

- 2-frequency control upon power on
- Volume is set at 50% upon powering up
- 64-step volume control
- Reference frequency signal is sinewave with low spurious emissions
- Built-in mute/decode switching
- Built-in Zener diode regulation
- 16-pin DIL package

APPLICATIONS

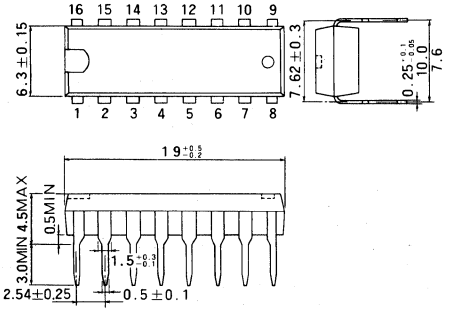
Color TVs, audio equipment, air conditioning equipment

RECOMMENDED OPERATING CONDITIONS

Rated supply voltage ..... I_{CC}=60mA

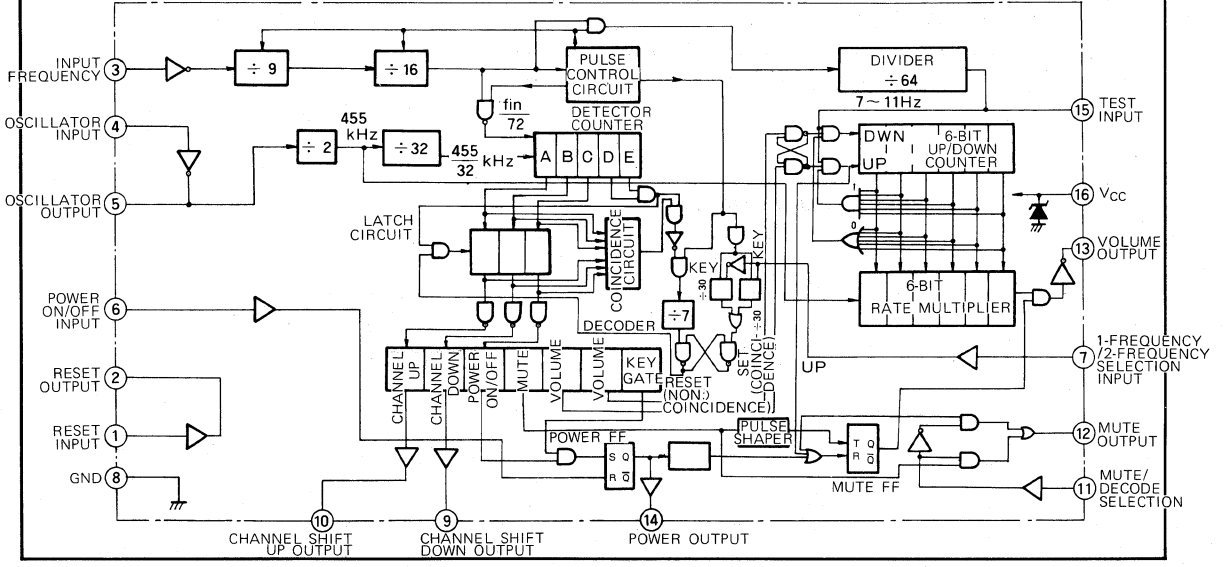
PACKAGE OUTLINE

Dimensions in mm



16-pin plastic DIL package

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

6-FUNCTION REMOTE CONTROL RECEIVER

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

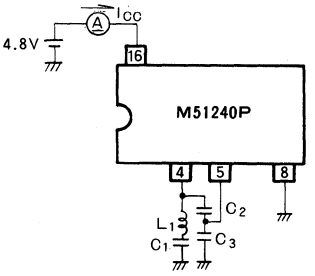
Symbol	Parameter	Conditions	Limits	Unit
I_{CC}	Circuit current		70	mA
Pd	Power dissipation		800	mW
$K\theta$	Derating	Ta ≧ 25℃	8	mW/℃
Topr	Operating temperature		−10 ~ +75	℃
Tstg	Storage temperature		−40 ~ +125	℃

ELECTRICAL CHARACTERISTICS (Ta = 25℃, V_{CC} = 4.8V, unless otherwise noted)

Symbol	Parameter	Test conditions	Test circuit	Limits			Unit
				Min	Typ	Max	
I_{CC}	Circuit current		(a)	10	20	50	mA
f_{ref}	Reference frequency range		(b)	899	910	926	kHz
v_{ref}	Reference frequency voltage		(b)	0.5	1.0	4.0	V_{P-P}
f_1	Operating frequnecy range (ch/dwn)		(c)	33.2	33.58	33.8	kHz
f_2	Operating frequency range (ch/up)		(c)	34.3	34.71	35.1	kHz
f_3	Operating frequency range (mute)		(c)	35.5	35.93	36.2	kHz
f_4	Operating frequency range (power)		(c)	36.7	37.24	37.6	kHz
f_5	Operating frequency range (vol/u)		(c)	38.1	38.64	39.0	kHz
f_6	Operating frequency range (vol/d)		(c)	39.6	40.16	40.6	kHz
f_7	Operating frequency range (key)		(c)	41.2	41.78	42.1	kHz
I_{D9}	Pin ⑨ leakage current		(d)			5	μA
I_{D10}	Pin ⑩ leakage current		(d)			5	μA
I_{D12}	Pin ⑫ leakage current		(d)			5	μA
I_{D13}	Pin ⑬ leakage current		(d)			5	μA
I_{D14}	Pin ⑭ leakage current		(d)			5	μA
V_{CE9}	Pin ⑨ saturation voltage		(d)	0.4	0.8	1.3	V
V_{CE10}	Pin ⑩ saturation voltage		(d)	0.4	0.8	1.3	V
V_{CE12}	Pin ⑫ saturation voltage		(d)	0.3	0.6	1.1	V
V_{CE13}	Pin ⑬ saturation voltage		(d)	0.3	0.6	1.1	V
V_{CE14}	Pin ⑭ saturation voltage		(d)	0.3	0.6	1.1	V
V_{Z16}	Pin ⑯ Zener voltage		(b)	5.0	5.5	6.0	V
	Volume function	Table 1	(e), (f)		Table 1		
	Power supply function	Table 2	(g)		Table 2		
	Muting function	Table 3	(h)		Table 3		

TEST CIRCUITS

(a) Icc

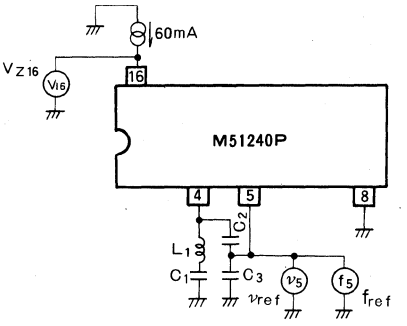


OSCILLATOR EXTERNAL CONSTANTS

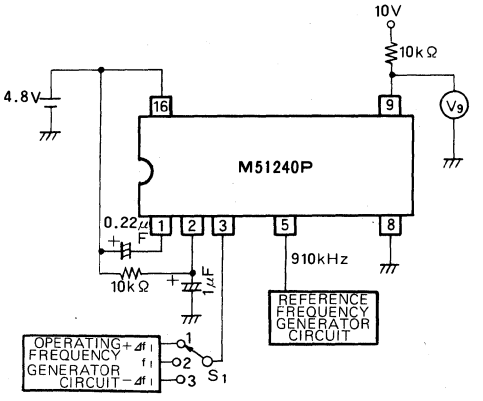
$L_1 \simeq 350\,\mu H$
$C_1 = 330\,pF$
$C_2 = 330\,pF$
$C_3 = 500\,pF$

THE CONSTANTS LISTED TO THE LEFT APPLY TO THE OTHER TEST CIRCUITS AS WELL

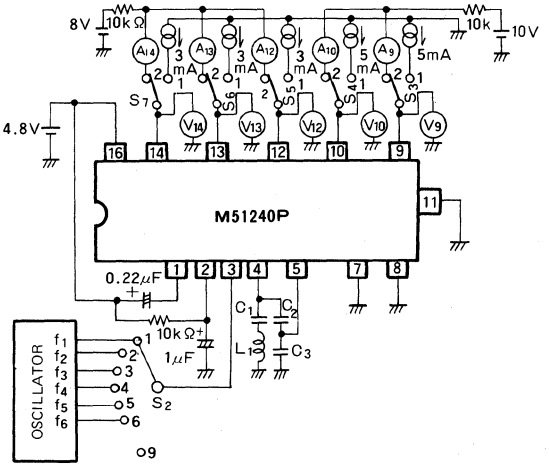
(b) V_{Z16}, fref, νref



(c) Operating frequency range



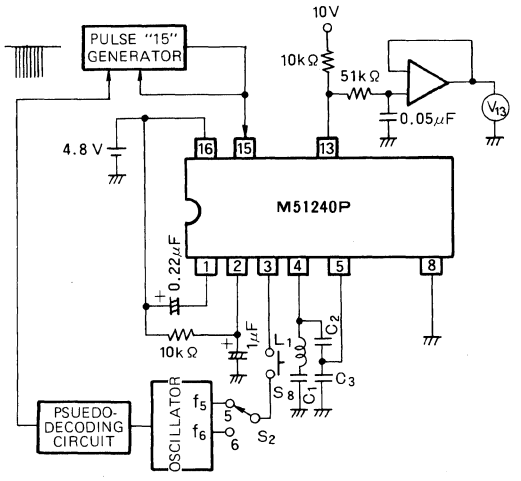
(d) V_{CE9}, I_{D9}, V_{CE10}, I_{D10}, V_{CE12}, I_{D12}, V_{CE13}, I_{D13}, V_{CE14}, I_{D14}



TEST METHODS

Symbol	Parameter	S_2	S_3	S_4	S_5	S_6	S_7	Test instrument	Method
V_{CE9}	Pin ⑨ saturation voltage	1	1					V_9	Measurement made 70ms after setting S_7
I_{D9}	Pin ⑨ leakage current	9	2					A_9	
V_{CE10}	Pin ⑩ saturation voltage	2		1				V_{10}	
I_{D10}	Pin ⑩ leakage current	9		2				A_{10}	
V_{CE12}	Pin ⑫ saturation voltage	3			1			V_{12}	
I_{D12}	Pin ⑫ leakage current	9			2			A_{12}	
V_{CE13}	Pin ⑬ saturation voltage	3				1		V_{13}	
I_{D13}	Pin ⑬ leakage current	5				2		A_{13}	
V_{CE14}	Pin ⑭ saturation voltage	9					1	V_{14}	
I_{D14}	Pin ⑭ leakage current	4					2	A_{14}	

(e) Volume test circuit



(f) Volume timing chart

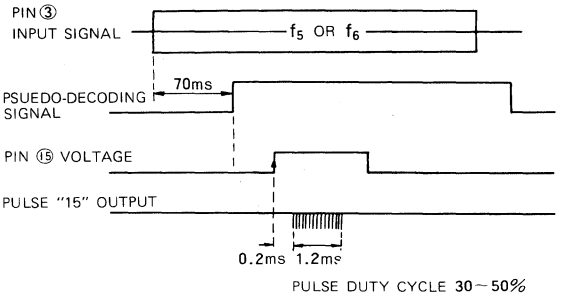
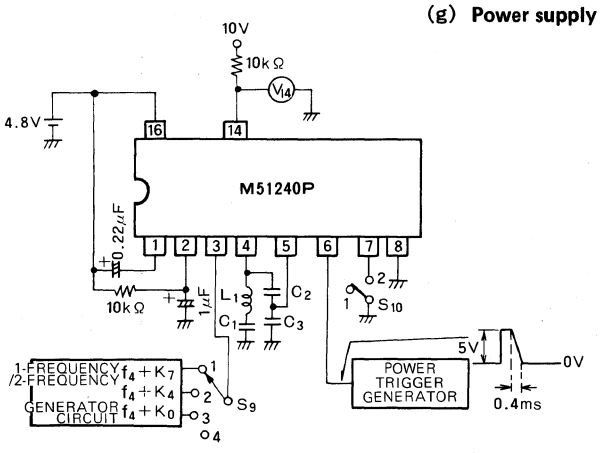


Table 1

Symbol	Parameter	S_2	S_8	Test instrument	Limits			Unit
					Min	Typ	Max	
V_{S50} (1)	Pin ⑬ voltage		OFF	V_{13}	5.0	5.63	6.2	V
V_{SD25}	Pin ⑬ voltage	6	OFF→ON	V_{13}	2.5	2.81	3.1	V
V_{SD0}	Pin ⑬ voltage	6	OFF→ON	V_{13}		0.1	0.5	V
V_{SU25}	Pin ⑬ voltage	5	OFF→ON	V_{13}'	2.5	2.81	3.1	V
V_{SU50}	Pin ⑬ voltage	5	OFF→ON	V_{13}	5.0	5.63	6.2	V
V_{SU75}	Pin ⑬ voltage	5	OFF→ON	V_{13}	6.8	7.63	8.4	V
V_{SU100}	Pin ⑬ voltage	5	OFF→ON	V_{13}	9.6	9.9		V
V_{SD75}	Pin ⑬ voltage	6	OFF→ON	V_{13}	6.9	7.63	8.4	V
V_{SD50} (1)	Pin ⑬ voltage	6	OFF→ON	V_{13}	4.8	5.33	5.9	V

Note (1): Upon applying power, volume is automatically initialized at 50%. The volume-up function increases the volume after a slight decrease.

(g) Power supply function



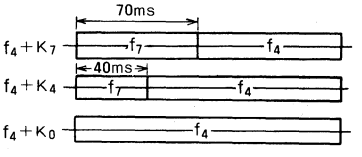


Table 2

Symbol	Parameter	S_9	S_{10}	Test circuit	Output mode	Remarks
V_{14}	Pin ⑭ voltage	4	1	V_{14}	L	
$V_{14\text{-}T7}$	Pin ⑭ voltage	4	1	V_{14}	H	Power trigger generator output applied to pin ⑥
$V_{14\text{-}T7}$	Pin ⑭ voltage	4	1	V_{14}	L	Power trigger generator output applied to pin ⑥
$V_{14\text{-}K7}$	Pin ⑭ voltage	1	1	V_{14}	H	
$V_{14\text{-}K4}$	Pin ⑭ voltage	2	1	V_{14}	H	
$V_{14\text{-}K7}$	Pin ⑭ voltage	1	1	V_{14}	L	
$V_{14\text{-}K4}$	Pin ⑭ voltage	2	1	V_{14}	L	
$V_{14\text{-}K0}$	Pin ⑭ voltage	3	2	V_{14}	H	
$V_{14\text{-}K0}$	Pin ⑭ voltage	3	2	V_{14}	L	

(h) Muting function

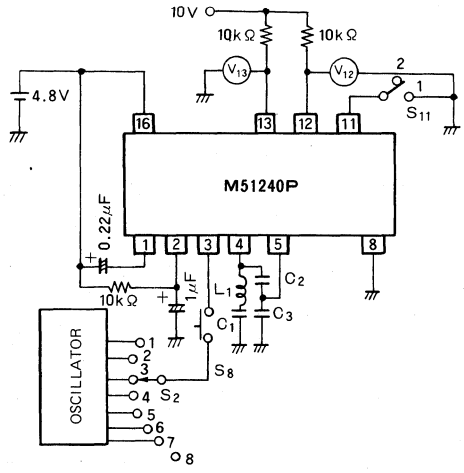
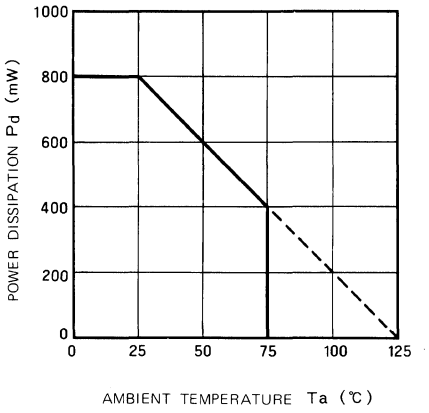


Table 3

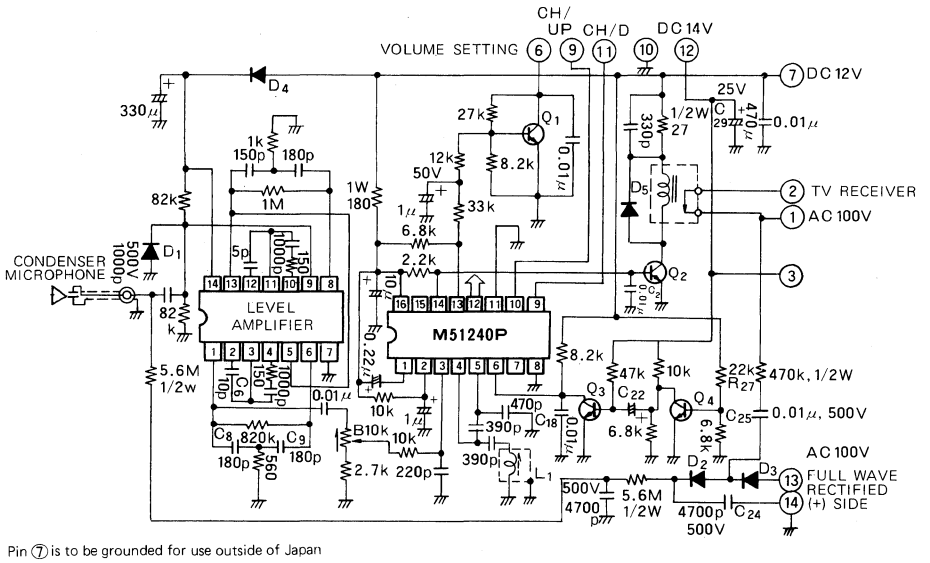
Symbol	Parameter	S_2	S_8	S_{11}	Test circuit	Output mode	Remarks
V_{MI}	Pin ⑬ voltage	8	OFF→ON	2	V_{13}	$\frac{Vcc}{2}$	Initial power output off
	Pin ⑬ voltage	3	OFF→ON	2	V_{13}	L	
V_{MM}	Pin ⑬ voltage	3	OFF→ON	2	V_{13}	$\frac{Vcc}{2}$	
	Pin ⑬ voltage	3	OFF→ON	2	V_{13}	L	
V_{MP}	Pin ⑬ voltage	4	OFF→ON	2	V_{13}	$\frac{Vcc}{2}$	Acts as subsequent power output on latch
	Pin ⑬ voltage	3	OFF→ON	2	V_{13}	L	
V_{MD}	Pin ⑬ voltage	5	OFF→ON	2	V_{13}	$\frac{Vcc}{2}$	
	Pin ⑬ voltage	3	OFF→ON	2	V_{13}	L	
V_{MU}	Pin ⑬ voltage	6	OFF→ON	2	V_{13}	$\frac{Vcc}{2}$	
	Pin ⑫ voltage	3	OFF→ON	2	V_{12}	H	
	Pin ⑫ voltage	3	OFF→ON	2	V_{12}	L	
	Pin ⑫ voltage	4	OFF→ON	2	V_{12}	H	Power output off
	Pin ⑫ voltage	4	OFF→ON	2	V_{12}	L	Power output on
	Pin ⑫ voltage	3	OFF→ON	2	V_{12}	H	
	Pin ⑫ voltage	5	OFF→ON	2	V_{12}	L	
	Pin ⑫ voltage	3	OFF→ON	2	V_{12}	H	
	Pin ⑫ voltage	6	OFF→ON	2	V_{12}	L	
	Pin ⑫ voltage	3	OFF→ON	1	V_{12}	L	
	Pin ⑬ voltage	3	OFF→ON	1	V_{13}	$\frac{Vcc}{2}$	

THERMAL DERATING
(MAXIMUM RATING)



APPLICATION EXAMPLE

6-Function color TV remote circuit



★M51240P Pin ⑦ is to be grounded for use outside of Japan

D1……MC301
D2……SRIFM-8
D3……SRIFM-8
D4……SRIFM-2
D5……SRIFM-4

Q1……2SC711A-F
Q2……2SC620-D, E
Q3……2SC711A-E, F
Q4……2SC711 A-E, F

Units Resistance; Ω (unless otherwise noted 1/4W)
Capacitance; F

PRECAUTION FOR USE

Do not apply more than 5V between pin ⑯ and pin ⑧. If more than 5V is applied, use a dropping resistor.

M51242P

3-FUNCTION REMOTE CONTROL RECEIVER

DESCRIPTION

The M51242P is a semiconductor integrated circuit consisting of a remote control demodulator which can be used to select functions in consumer and industrial equipment such as color TVs.

FEATURES

- Zener diode for power stability
- 3 selectable functions
- Stable frequency standard (314kHz Clapp oscillator)
- Low-distortion frequency standard (no cross-modulation from higher harmonics)
- Open collector output

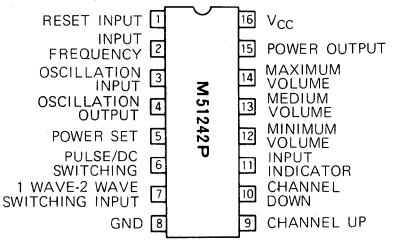
APPLICATIONS

Television, audio equipment, etc.

RECOMMENDED OPERATING CONDITIONS

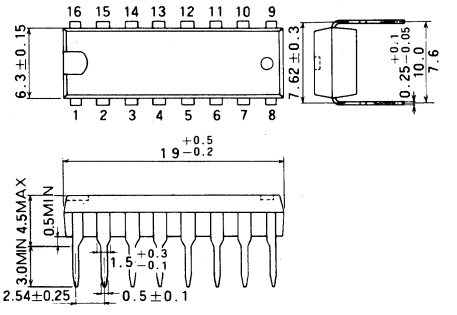
Rated supply voltage ..... I_{CC}=30mA

PIN CONFIGURATION (TOP VIEW)



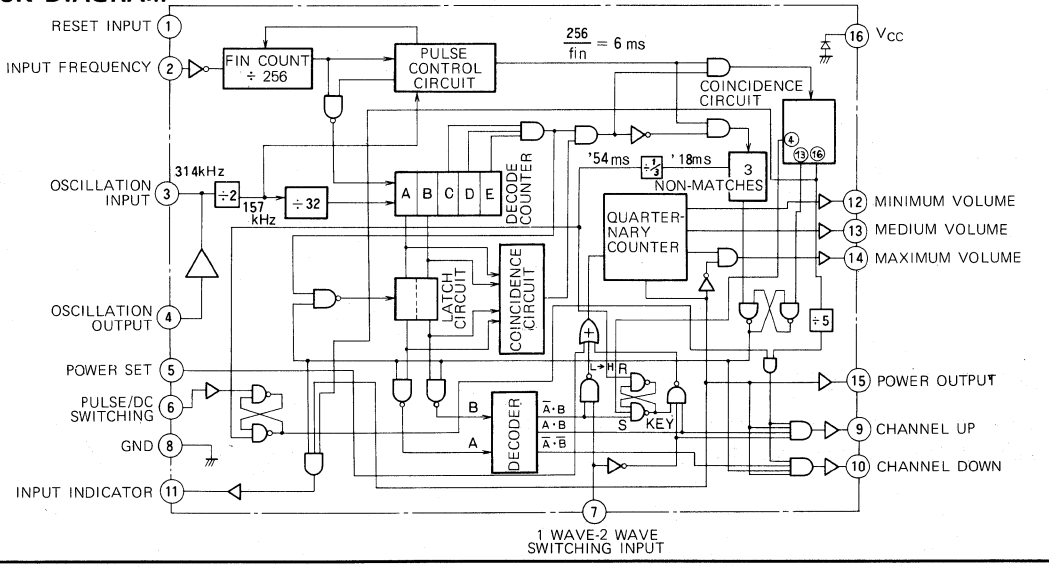
PACKAGE OUTLINE

Dimensions in mm



16-pin plastic DIL package

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS (Ta=25°C, unless otherwise noted)

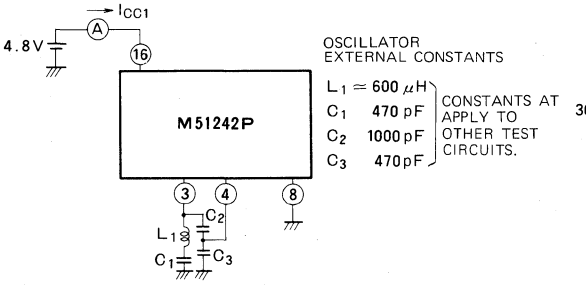
Symbol	Parameter	Conditions	Limits	Unit
I_{CC}	Circuit current		50	mA
I_P	Pin ⓘ current input	Pin ⓘ (i=1~3, 5~7, 12~15)	5	mA
$I_{④P}$	Pin ④ current input		5	mA
$I_{④N}$	Pin ④ current output		−5	mA
$I_⑨$	Pin ⑨ current input		10	mA
$I_⑩$	Pin ⑩ current input		10	mA
$I_⑪$	Pin ⑪ current input		7	mA
$I_⑯$	Pin ⑯ current input		50	mA
$V_⑨$	Pin ⑨ reverse DC breakdown voltage		10	V
$V_⑩$	Pin ⑩ reverse DC breakdown voltage		10	V
V_B	Pin ⓘ reverse DC breakdown voltage	Pin ⓘ (i=11~15)	8	V
Pd	Power dissipation		700	mW
K_θ	Derating	Ta≧25°C	7	mW/°C
Topr	Operating temperature		−10~+75	°C
Tstg	Storage temperature		−40~+125	°C

ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{CC}=4.8V)

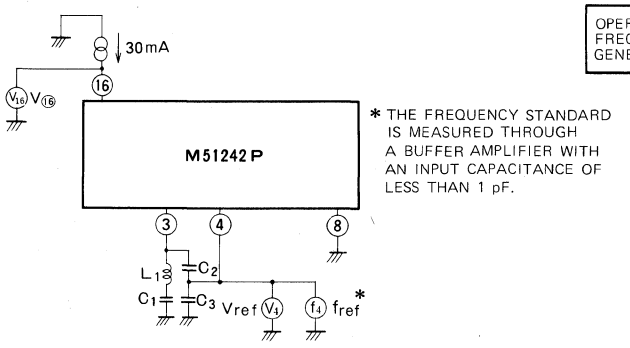
Symbol	Parameter	Test conditions	Test circuit	Limits Min	Limits Typ	Limits Max	Unit
I_{CC1}	Circuit current		(a)	7	12	22	mA
fref	Frequency standard range		(b)	309	314	319	kHz
Vref	Frequency standard voltage		(b)	0.5	2.5	5.0	V
f_1	Operating frequency range (POWER)		(c)	40.6	41.1	41.6	kHz
f_2	Operating frequency range (CH/UP)		(c)	42.0	42.5	43.1	kHz
f_3	Operating frequency range (CH/DWN)		(c)	43.4	44.0	44.6	kHz
$ID_⑨$	Pin ⑨ leakage current		(d)		—	5	μA
$ID_⑩$	Pin ⑩ leakage current		(d)		—	5	μA
$ID_⑪$	Pin ⑪ leakage current		(d)		—	5	μA
$ID_⑫$	Pin ⑫ leakage current		(d)		—	5	μA
$ID_⑬$	Pin ⑬ leakage current		(d)	—	—	5	μA
$ID_⑭$	Pin ⑭ leakage current		(d)	—	—	5	μA
$ID_⑮$	Pin ⑮ leakage current		(d)	—	—	5	μA
$V_{CE⑨}$	Pin ⑨ saturation voltage		(d)	80	160	350	mV
$V_{CE⑩}$	Pin ⑩ saturation voltage		(d)	80	160	350	mV
$V_{CE⑪}$	Pin ⑪ saturation voltage		(d)	200	400	700	mV
$V_{CE⑫}$	Pin ⑫ saturation voltage		(d)	150	300	600	mV
$V_{CE⑬}$	Pin ⑬ saturation voltage		(d)	150	300	600	mV
$V_{CE⑭}$	Pin ⑭ saturation voltage		(d)	150	300	600	mV
$V_{CE⑮}$	Pin ⑮ saturation voltage		(d)	150	300	600	mV
$V_⑯$	Pin ⑯ Zener diode voltage		(b)	5.0	5.5	6.0	V

TEST CIRCUITS

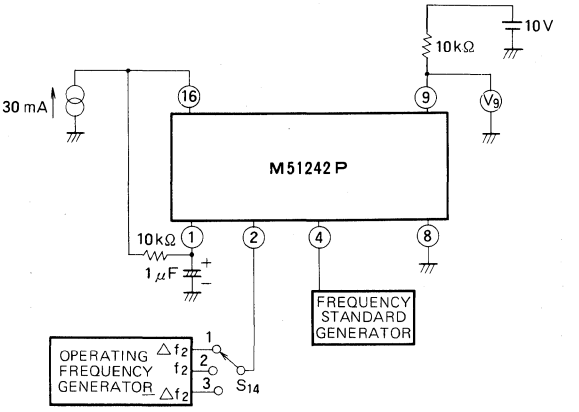
(a) I_{CC1}



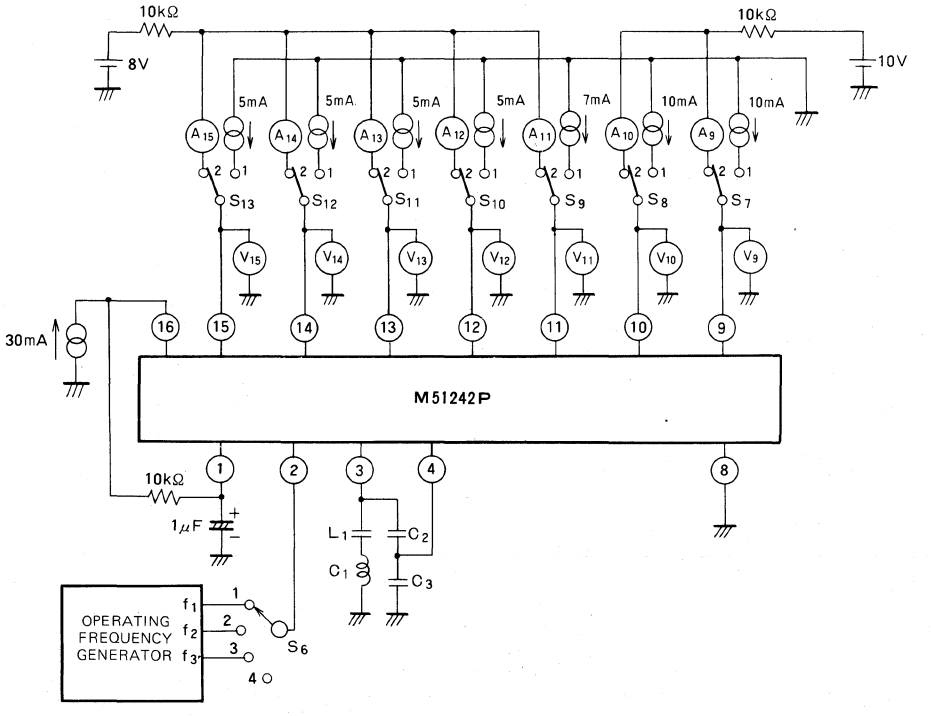
(b) $V_{⑯}$, f_{ref} V_{ref}



(c) Operating frequency range (typified by f_2 test)



(d) $V_{CE⑨}$, $I_{D⑨}$, $V_{CE⑩}$, $I_{D⑩}$, $V_{CE⑪}$, $I_{D⑪}$, $V_{CE⑫}$, $I_{D⑫}$
$V_{CE⑬}$, $I_{D⑬}$, $V_{CE⑭}$, $I_{D⑭}$, $V_{CE⑮}$, $I_{D⑮}$



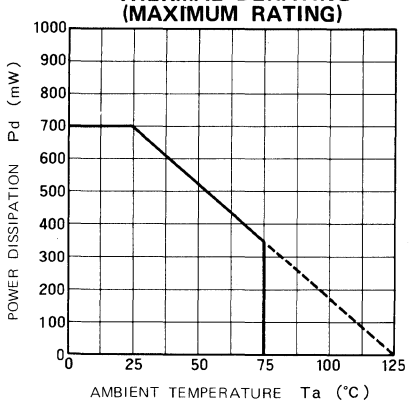
MITSUBISHI ELECTRIC

TEST METHODS

Symbol	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}	S_{13}	Test meter	Method
$V_{CE⑨}$	2	1							V_9	Test 280 ms after setting S_7
$ID_{⑨}$	3	2							A_9	
$V_{CE⑩}$	3		1						V_{10}	Test 280ms after setting S_7
$ID_{⑩}$	1(Note)		2						A_{10}	
$V_{CE⑪}$	1(Note)			1					V_{11}	Test 80 ms after setting S_7
$ID_{⑪}$	4			2					A_{11}	〃
$V_{CE⑫}$	4				1				V_{12}	〃
$ID_{⑫}$	4→1				2				A_{12}	〃
$V_{CE⑬}$	4					1			V_{13}	〃
$ID_{⑬}$	4→1					2			A_{13}	〃
$V_{CE⑭}$	4						1		V_{14}	〃
$ID_{⑭}$	4→1						2		A_{14}	〃
$V_{CE⑮}$	4							1	V_{15}	〃
$ID_{⑮}$	4→1							2	A_{15}	〃

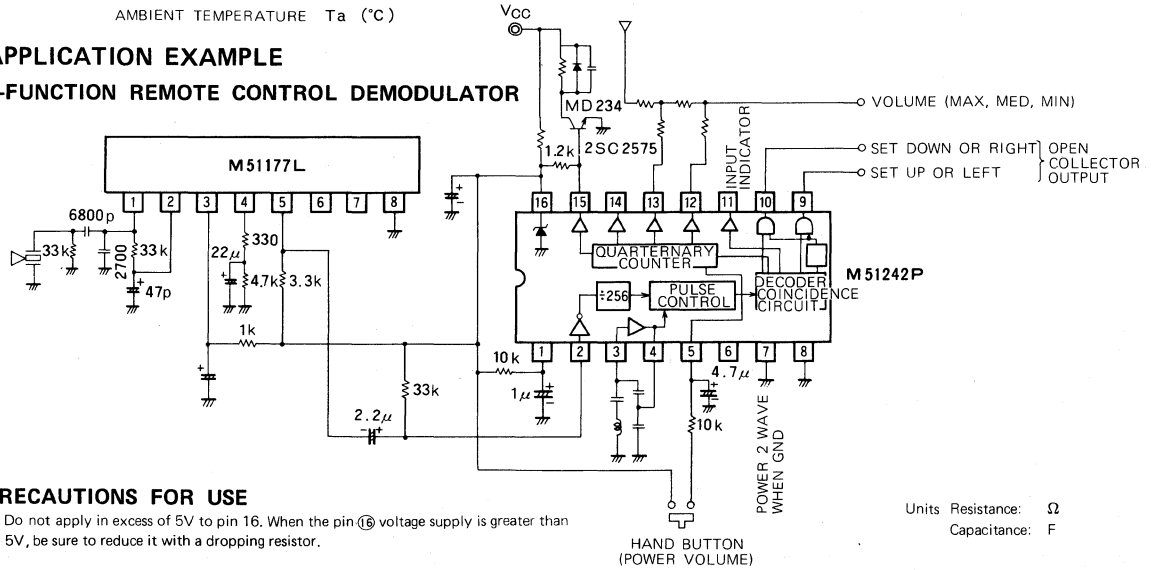
Note: Leave S_6 set to 1 between tests of $IC_{⑩}$ and $V_{CE⑪}$

THERMAL DERATING (MAXIMUM RATING)



APPLICATION EXAMPLE

3-FUNCTION REMOTE CONTROL DEMODULATOR



PRECAUTIONS FOR USE

1. Do not apply in excess of 5V to pin 16. When the pin ⑯ voltage supply is greater than 5V, be sure to reduce it with a dropping resistor.

Units Resistance: Ω
Capacitance: F

M51251P

TV VOLTAGE SYNTHESIZER

DESCRIPTION

The M51251P is a semiconductor integrated circuit consisting of a TV voltage synthesizer.

Functions include AFT signal processing, TV video carrier detection, D/A conversion and buffer amplification.

FEATURES

- AFT output without the need for a varicap
- AFT on/off switching input
- CRT display is possible of the tuned frequency (channel)

APPLICATIONS

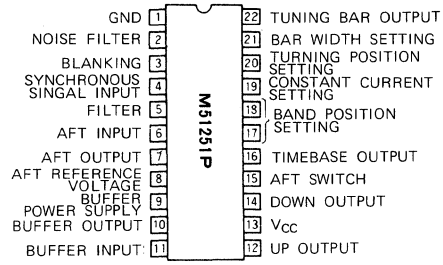
Voltage synthesizers for color TVs and VTR tuners

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... 11~13V

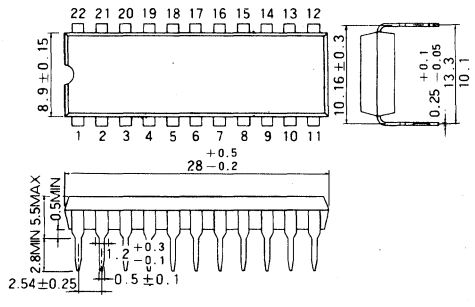
Rated supply voltage 12V

PIN CONFIGURATION (TOP VIEW)



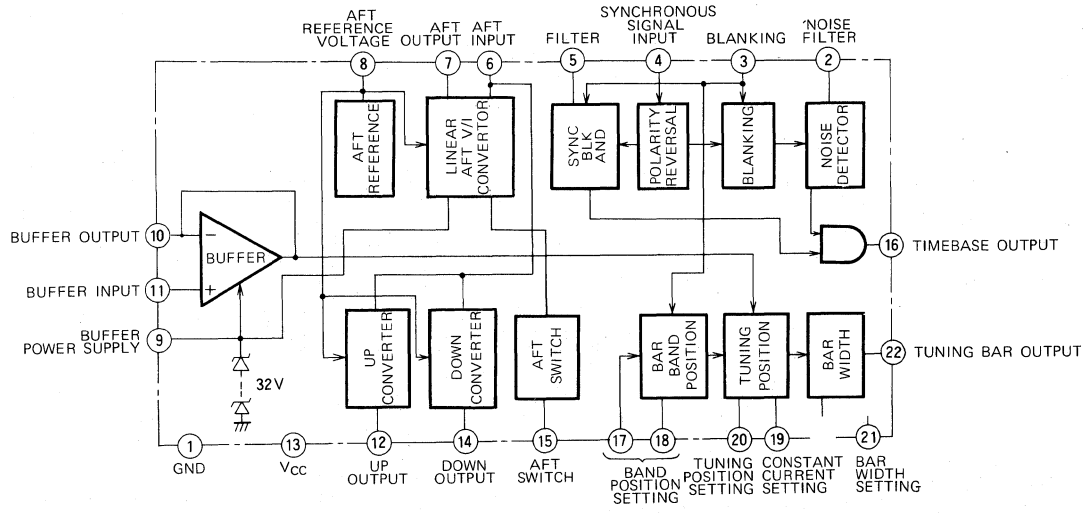
PACKAGE OUTLINE

Dimensions in mm



22-pin plastic DIL package

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS (Ta=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		16	V
P_d	Power dissipation		1.4	W
T_{opr}	Operating temperature		−20 ~ +75	°C
T_{stg}	Storage temperature		−40 ~ +125	°C
I_9	Pin 9 current		8	mA

ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{CC}=12V, unless otherwise noted)

Symbol	Parameter	Test circuit	Test conditions									Test point	Limits			Unit
			▽a	SW_1	SW_2	SW_3	SW_4	SW_5	SW_6	SW_7	SW_8		Min	Typ	Max	
I_{CC}	Circuit current	1	10V	2		2	1	1	1	2	2	a	17	27	37	mA
V_{BH}	Buffer output voltage range	1				3	1	2	2	1	2	10 • 11		29		V
V_{BL}										3				0.6		
V_Z	Zener voltage	1				3	1	2	2	2	2	9	29	31.7	33.5	V
I_{BIAS}	Buffer bias current	1				3	1	2	2	2	2	b			0.6	μA
V_{6-8U}	AFT converter threshold voltage	1	Variable	2	3				1		2	6,8 12	+150	+200	+270	mV
V_{6-8D}					2							6,8 14	−240	−190	−120	
g_m	AFT mutual conductance	1	Variable			1			1	2	2	6,8 C		0.65		mΩ
I_{AFTH}	AFT maximum output current	1	8V			1			1	2	2	C	+200	+290	+400	μA
I_{AFTL}			4V										−400	−290	−200	
I_{OFF}	AFT off current	1	8V			3			1	2	2	C	−5	0	+5	μA
V_{REF}	AFT reference voltage	1							2		2	8		6.0		V
V_{2H}	Pin 2 voltage	1					1	1			2	2		9.4		V
V_{2L}							2	1							0.2	
V_{5H}	Pin 5 voltage	1					2	2	2		2	5		10		V
V_{5L}							2	1						0.2		
V_{UH}	Up output voltage	1	8V	3	3				1		2	12	9.35	10	10.65	V
V_{UL}			4V	1											1.2	
V_{DH}	Down output voltage	1	4V	3	2				1		2	14	9.35	10	10.65	V
V_{DL}			8V	1											1.2	
V_{TH}	Timebase output voltage	1		3	1	]	2	1			2	16	9.35	10	10.65	V
V_{TL}				1			1								1.2	
V_{2TH}	Pin 2 threshold voltage	1	Variable	2			2	1	2		1	2, 16		7.0		V
V_{5TH}	Pin 5 threshold voltage		Variable	2				2	2		3	5, 16		5.5		V

Symbol	Parameter	Test circuit	Test conditions				Limits			Unit
			SW_9	SW_{10}	SW_{11}	Test point	Min	Typ	Max	
V_{ZZ}	Pin 22 voltage	2	1	2	2	A		0.2		V
B_W	Bar width	2	2	1	3	A		1.2		μs
B_L	Bar lower limit	2	2	1	3	A		12		μs
B_H	Bar upper limit	2	2	2	1	A		43		μs

Note 1. Buffer Output Voltage Range

Units are considered good when the voltage difference V_{10}-V_{11} (V_{10-11}) is smaller than 29mV for setting of SW_1 to 29V and 0.6V.

Note 2. AFT Comparator Threshold Voltage

Varying V_a the voltage difference V_6-V_8 when the voltage on pin 12 goes from to high or high to low is taken as the reference for V_{6-8U}. The same is true for pin 14 and the V_{6-8D} reference.

Note 3. AFT Mutual Conductance

Varying V_a and letting I_{a1} (μA) be the AFT output current (pin 7) with a V_{6-8} of 300mV and I_{a2} (μA) be the AFT output current (pin 7) for a V_{6-8} of −300mV, then gm is given by the expression which follows.

$$gm = \frac{Ia_1 - Ia_2}{300 - (-300)} \quad (gm)$$

Note 4. Pin 2 Threshold Voltage

The pin 2 threshold voltage V_{2TH} is the voltage V_a at which the pin 16 voltage V_{16} goes from high to low or low to high.

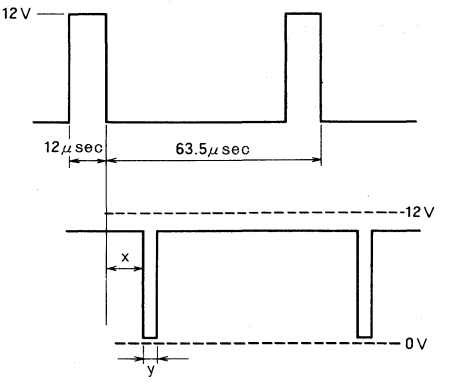
Note 5. Pin 5 Threshold Voltage

The pin 5 threshold voltage V_{5TH} is the voltage V_a at which the pin 16 voltage V_{16} goes from high to low or from low to high.

Note 6. Bar Width and Bar Lower Limit

Inputing a signal from a signal generator as shown in Figure (a), at point a the bar width is as shown in Figure (b) as y (μs).

The bar lower limit is the period shown in Figure (a) as X(μs) starting from the trailing edge of Figure (a) waveform to the leading edge of the Figure (b) waveform.

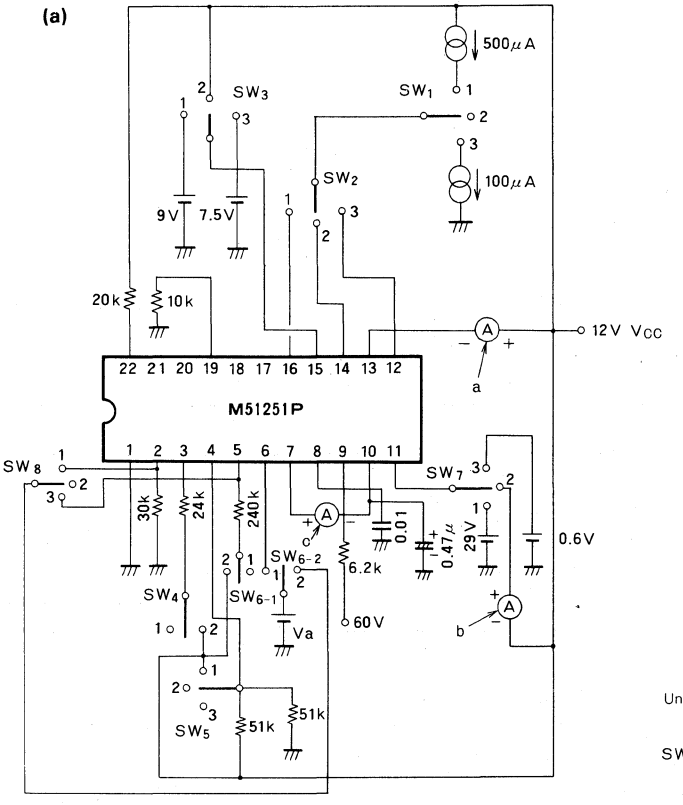


Note 7. Bar Upper Limit

Switching SW_{10} and SW_{11} the upper limit is again the time from the falling edge of the Figure (a) waveform to the falling edge of the Figure (b) waveform.

TEST CIRCUITS

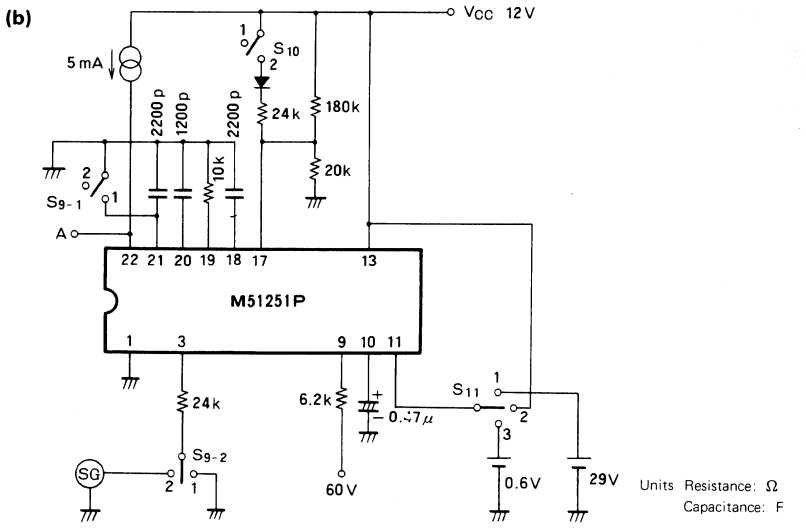
(a)

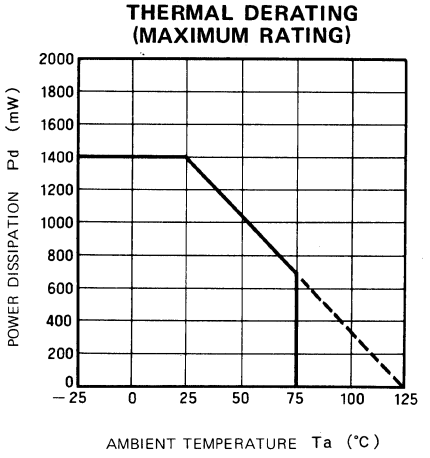


Units Resistance: Ω
Capacitance: F

SW_{6-1}, SW_{6-2} are linked

MITSUBISHI ELECTRIC





FUNCTION

(1) AFT signal processor

The AFT signal processor is normally part of the AFT loop and operates during automatic selection as well.

As shown in Figure 1, when the AFT voltage is greater than or less than the central value by more than 200mV the up or down digital signal is output respectively. When the tuning voltage is lower the up signal is high (12V) and when it is high the down signal is high. These two signals are used to provide digital AFT control. The AFT loop is formed by outputing a current as shown in Figure 2 in response to the

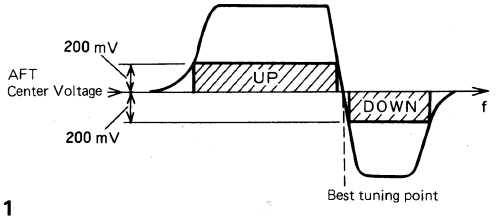


Fig. 1

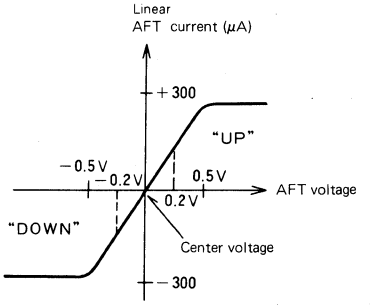


Fig. 2

AFT output voltage. This current flows through a load resistance to form a voltage signal which is impressed upon the AFT voltage. Linear AFT operation is controlled by the AFT switch.

(2) TV Video Carrier Detector

This detector is used to detect the video carrier by two methods ANDing them to form a digital output. The output is high (12V) for a detected video carrier.

The first detection method checks if the blanking signal and the separated sink signal coincide (coincidence detection).

The other method relies on detection of the quantity of noise in the above syne signal during the horizontal scan. (Noise detection)

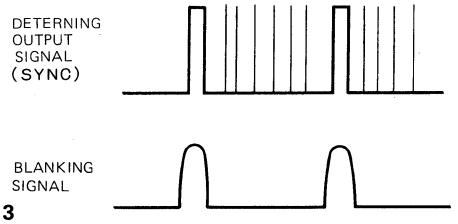


Fig. 3

(3) D/A Buffer Amplifier

The output tuning voltage from the controller is a pulse train of pulses two μs wide and 12Vp-p in amplitude, varying in duty cycle. These pulses are amplified by an inverting amplifier with zener diode temperature compensation and then filtered with an RC low pass filter to remove the ripple components. The voltage is then amplified by a buffer amplifier of gain one which also lowers the impedance. The signal is then applied to the linear AFT load resistance and applied as well to the varicap as the tuning voltage. An active filter is formed by feeding back the output voltage to the capacitor of the first stage of the low pass filter so that the time constant may be lowered.

(4) Tuning Display

The tuning display consists of a vertical bar of green, red or blue on the TV screen, the position of the bar indicating the channel selected.

As shown in Fig. 4, the screen is divided vertically into three sections; V_L, V_H and U. For each band a tuning voltage of 0V corresponds to the position to the far left of the horizontal region and as the voltage is increased the bar moves to the right. At the highest tuning voltage value the bar is at the right of the band. The width of the band is controllable by an external capacitance. However, the widths of the bands may not be varied independently for each band.

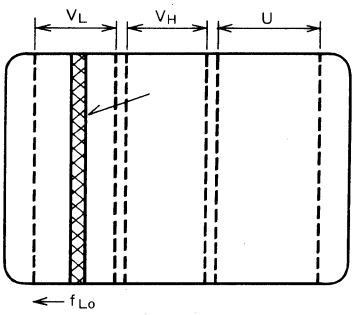


Fig. 4

The beginning of the band may be determined by an external DC voltage independent of the other bands. Therefore, as shown in Fig. 5, each band can be made to take up the entire screen width.

The bar width may also be controlled by an external capacitance which if removed causes the bar to disappear completely. While the channel spacing is adjusted to be approximately equal, the adjustment is different for VHF and UHF band as shown in Fig. 4. For the case of Fig. 5, the band adjustment does not differ.

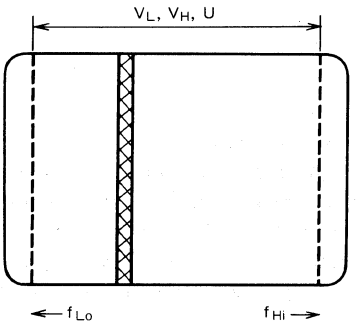
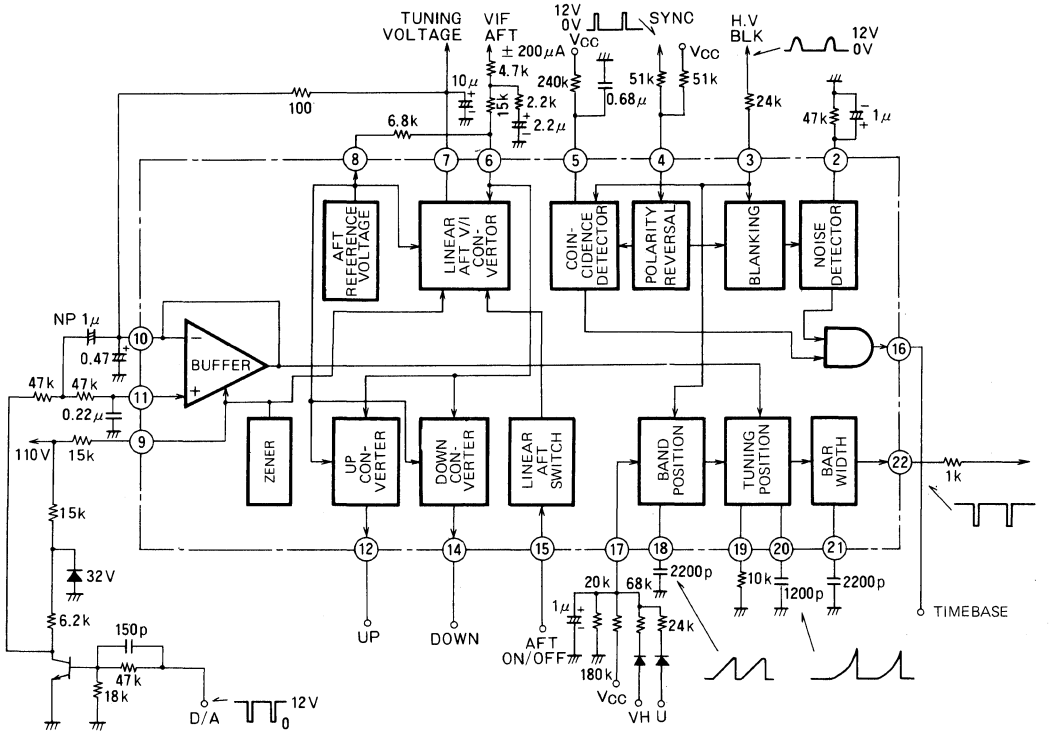


Fig. 5

APPLICATION EXAMPLE



M5134P

TV AFT CIRCUIT

DESCRIPTION

The M5134P is a semiconductor integrated circuit consisting of an AFT circuit designed for applications in TV tuner automatic frequency control. It includes an RF amplifier/limiter, phase detector, differential DC amplifier, bias stabilizer circuit and a voltage regulated circuit formed around a zener diode.

FEATURES

- Regulated power supply with zener diode included
- Built-in differential input amplifier and limiter
- Full-wave bridge detection using diode
- Differential output available

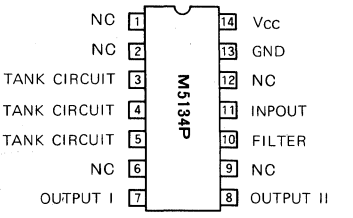
APPLICATION

TV AFT circuits

RECOMMENDED OPERATING CONDITIONS

Rated supply voltage ..... 18V (with R_s = 270Ω)

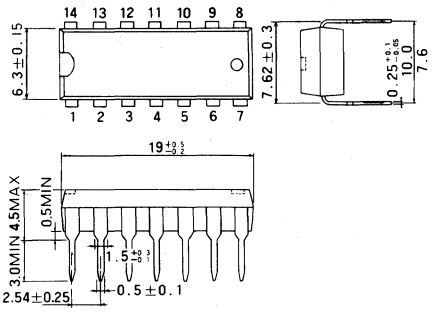
PIN CONFIGURATION (TOP VIEW)



NC: NO CONNECTION

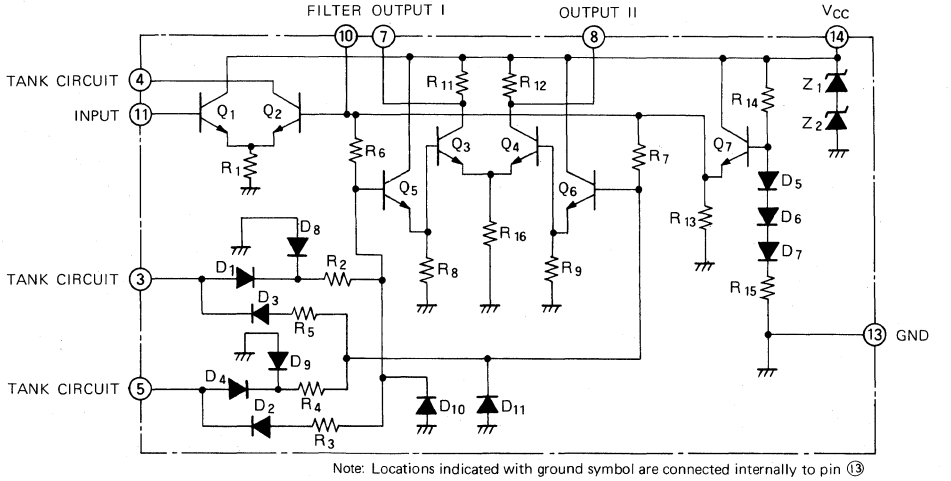
PACKAGE OUTLINE

Dimensions in mm



14-pin plastic DIL package

EQUIVALENT CIRCUIT



Note: Locations indicated with ground symbol are connected internally to pin ⑬

MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS (Ta=25°C, unless otherwise noted)

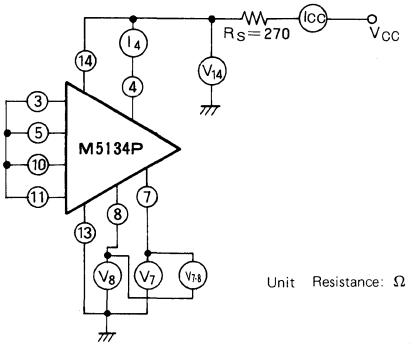
Symbol	Parameter	Conditions	Limits	Unit
I_{CC}	Circuit current		60	mA
Pd	Power dissipation		700	mW
K_θ	Thermal derating	Ta≧25°C	7	mW/°C
Topr	Operating temperature		−20～+75	°C
Tstg	Storage temperature		−40～+125	°C

ELECTRICAL CHARACTERISTICS (Ta=25°C)

Symbol	Parameter	Test conditions		Test circuit	Limits			Unit
					Min	Typ	Max	
Pd	Power dissipation	V_{CC}=18.0V, Rs=270Ω		(a)	190	270	360	mW
I_{CC}	Circuit current (V_{CC}=9V)	$V_{⑭}$=9V		(a)	4.3	6.3	9.5	mA
$V_{⑭}$	Pin ⑭ voltage	V_{CC}=18.0V, Rs=270Ω		(a)	10.3	11.2	11.9	V
$I_{④}$	Pin ④ current				1.0	2.1	4.3	mA
$V_{⑦}$	Pin ⑦ voltage				5.0	6.5	8.0	V
$V_{⑦-⑧}$	Voltage difference across pins ⑦ and ⑧				−1.0	0	1.0	V
V_i(lim)	Input limiting voltage	f=58.75MHz		(b)		100		mVrms
Δf_1	Control voltage characteristics I	V_i=200mVrms	$V_{⑦,⑧}$=3～10V	(c)		50	100	kHz
Δf_2	Control voltage characterisitcs 2		$V_{⑦,⑧}$=3～10V	(c)	2.5			MHz

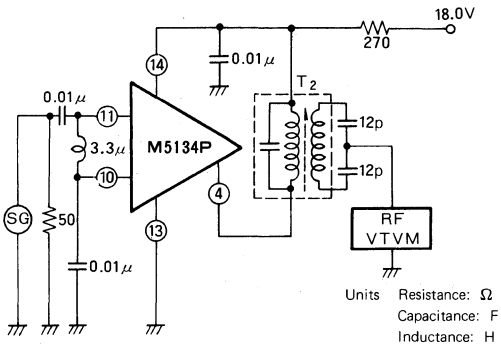
TEST CIRCUIT

(a) Power dissipation, sink current, pin voltage



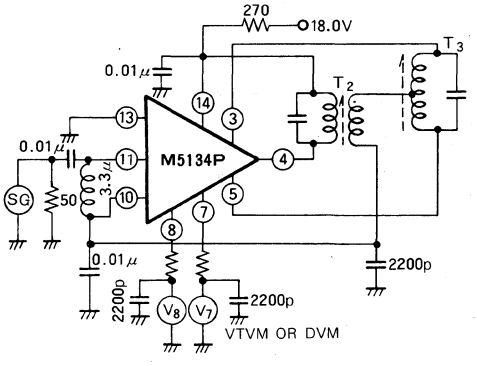
Unit Resistance: Ω

(b) Input limiting voltage



Units Resistance: Ω
Capacitance: F
Inductance: H

(c) Control voltage characteristics



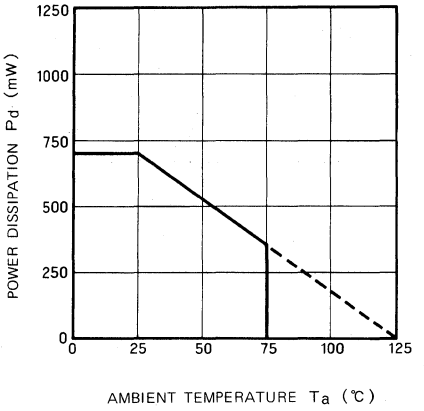
Units Resistance: Ω
Capacitance: F
Inductance: H

Test method:
Increase the input level until the output level is saturated and then turn down the SG attenuator until the RF DVM indication value is reduced by 3dB. The input signal voltage will now be $V_{i(lim)}$.
RF DVM: RF digital voltmeter
SG: Signal generator

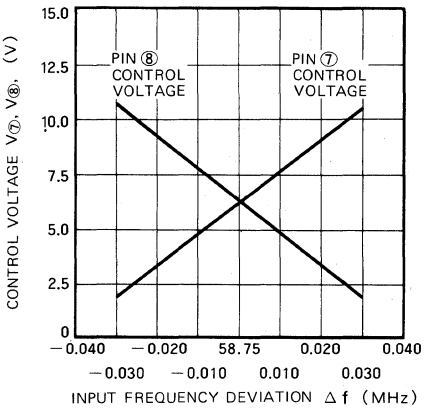
Testing precautions:
Refer to Table 1 for the specifications of T2 and T3. Attach all the parts except the IC socket to the copper foil side of the PCB.
DVM: Digital voltmeter

TYPICAL CHARACTERISTICS (Ta = 25°C, unless otherwise noted)

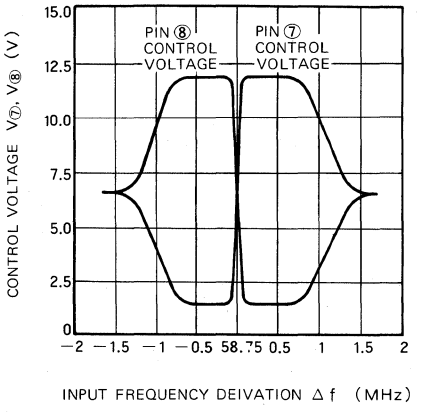
THERMAL DERATING (MAXIMUM RATING)



CONTROL VOTAGE VS INPUT FREQUENCY DEVIATION



CONTROL VOLTAGE VS INPUT FREQUENCY DEVIATION



APPLICATION EXAMPLE

Color TV AFT circuit

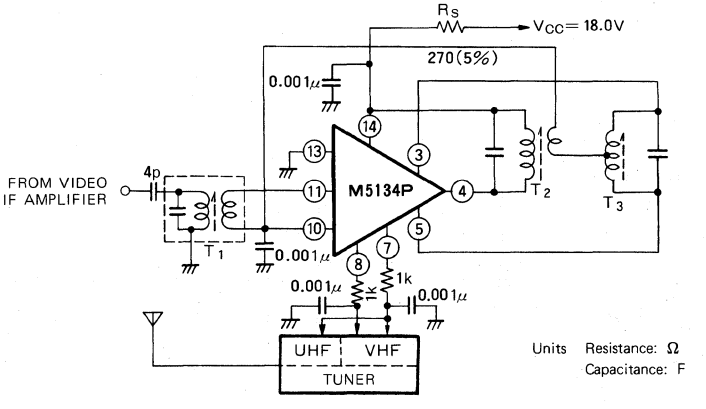
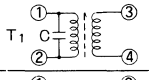
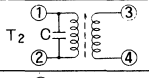
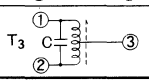


Table 1 Transformer specifications

Transformer	Connections	Pins	Coil material and turns	Capacitance C(pF)	Qo
T_1		①—②	φ0.8mm formarwire 6¾ turns	47	100
		③—④	φ0.8mm formarwire, 4¾ turns		
T_2		①—②	φ0.8mm formarwire 3¼ turns	56	130
		③—④	φ0.8mm formarwire, 3¼ turns		
T_3		①—②	φ0.8mm tin-plated wire 4¾ turns, space winding ③はCT	68	150

Note: Core material: E 1 screw core φ3.5mm×6.5mm

PRECAUTIONS FOR USE

1. The M5134P has a built-in zener diode and so the drop resistance R_s should be chosen with the voltage supply conforming to the supply voltage V_{CC} so that the allowable power consumption of the IC is not exceeded with variations in the V_{CC} and zener diode voltage V_z. The standard operating conditions are a supply voltage of 18.0V ±10% and a drop resistance of 270Ω ±5%. Refer to Table 2 when setting the drop resistance.
2. When using only one of the M5134P's differential outputs (pin ⑦ or ⑧) for the tuner AFT circuit, connect the unconnected pin to the V_{CC} pin((pin ⑭) for use.

Table 2 Supply voltage regulation (K%) and drop resistance

K	Vcc	Rs
5%	16V min.	Vcc=18V→Rs=270Ω
10%	20V min.	Vcc=24V→Rs=620Ω
15%	29V min.	Vcc=30V→Rs=800Ω

M51342P

TV GAME MODULATOR

DESCRIPTION

The M51342P is a semiconductor integrated circuit consiting of a modulator designed for NTSC TV games and includes a color signal modulator, 3.58MHz oscillator, 4.5MHz oscillator, RF oscillator and RF modulator. Its output serves to receive the TV antenna input signal.

The standard supply voltage is 9V in consideration of dry battery operation.

FEATURES

- Controller allows digital signals to be sent to M51342P.
- 3.58MHz signal is used as clock signal of controller IC.
- Controller IC block and modulator block including the M51342P and its peripheral circuits can be configured separately.
- RF outputs for two channels.
- Selectable color signal step and number

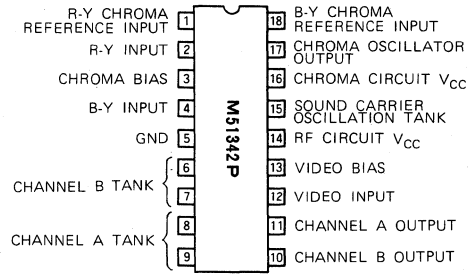
APPLICATION

TV displays for color TV games

RECOMMENDED OPERATING CONDITIONS

Supply volrage range ..... 7.0~11.0V
Rated supply voltage 9.0V

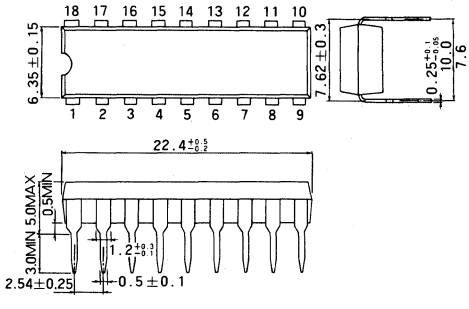
PIN CONFIGURATION (TOP VIEW)



NC: NO CONNECTION

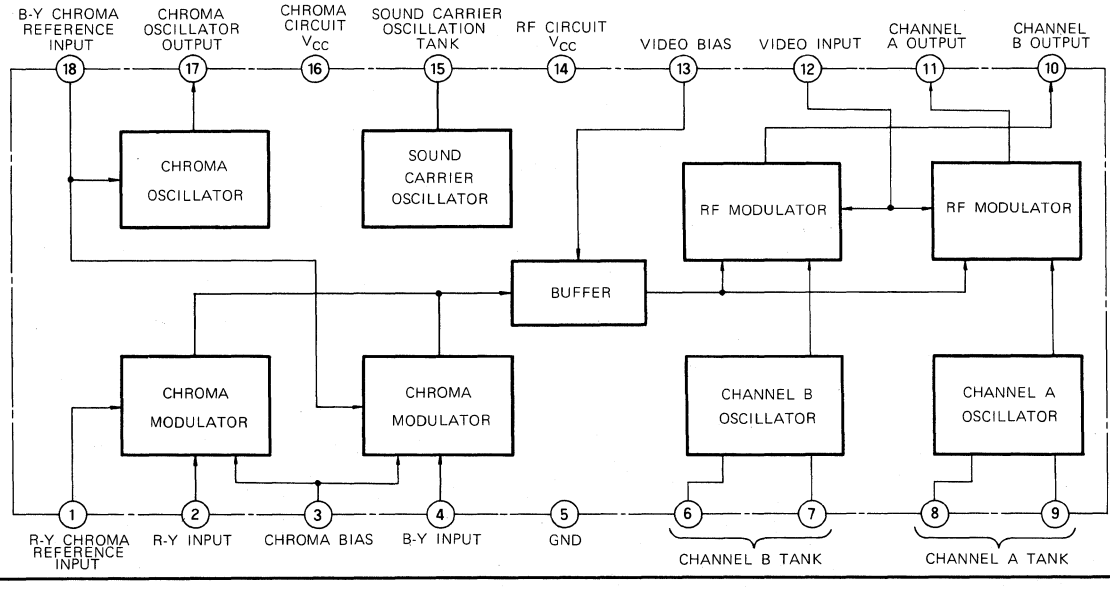
PACKAGE OUTLINE

Dimensions in mm



18-pin plastic DIL package

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

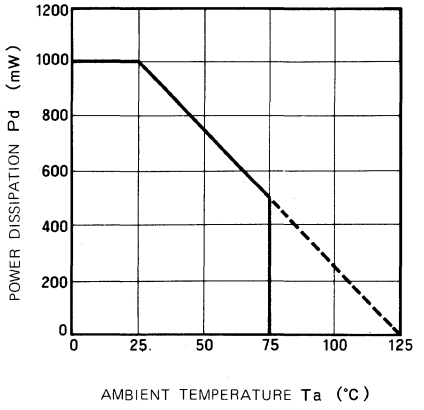
ABSOLUTE MAXIMUM RATINGS (Ta=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		13.5	V
$V_{②-⑤}$	Circuit voltage (pins ②~⑤)		V_{CC}	V
$V_{③-⑤}$	Circuit voltage (pins ③~⑤)		V_{CC}	V
$V_{④-⑤}$	Circuit voltage (pins ④~⑤)		V_{CC}	V
$V_{⑫-⑤}$	Circuit voltage (pins ⑫~⑤)		V_{CC}	V
$V_{⑬-⑤}$	Circuit voltage (pins ⑬~⑤)		V_{CC}	V
$I_{⑰}$	Circuit current		5	mA
Pd	Power dissipation		1000	mW
K_θ	Derating	Ta≧25°C	10	mW/°C
Topr	Operating temperature		−20~+75	°C
Tstg	Storage temperature		−40~+125	°C

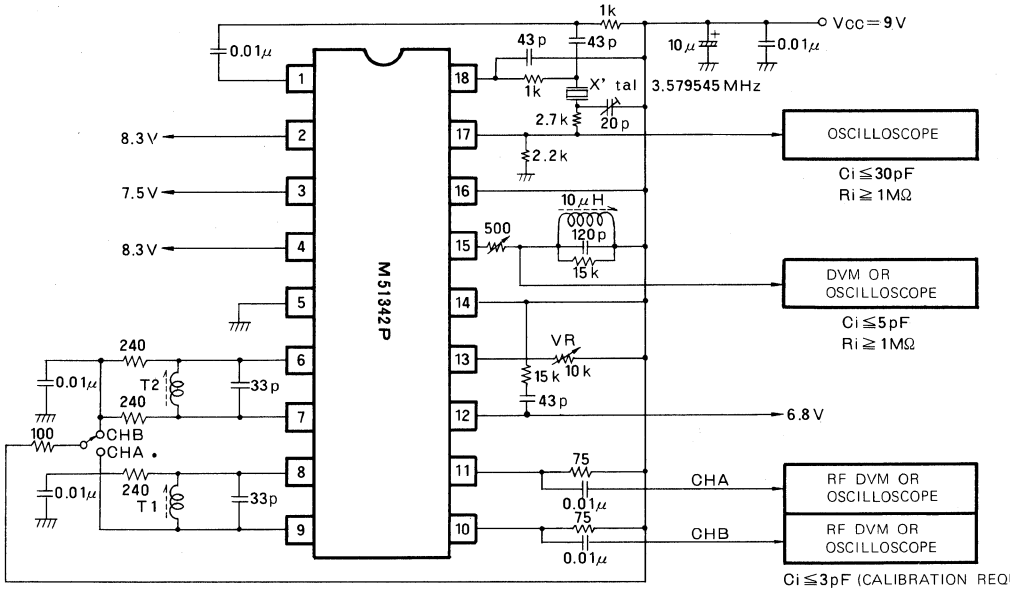
ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{CC}=9V)

Symbol	Parameter	Test conditions	Test circuit	Limits			Unit
				Min	Typ	Max	
I_{CC}	Total circuit current		(a)	25	36	47	mA
$v_{⑰}$	Chroma oscillator output		(a)	1.1	1.6	2.0	V_{P-P}
$v_{⑬}$	Modulated chroma output		(a)		0.2		V_{P-P}
$v_{⑪}$	Channel A output	f=91.25MHz or 97.25MHz	(a)	10	30	100	mV_{P-P}
$v_{⑩}$	Channel B output	f=91.25MHz or 97.25MHz	(a)	10	30	100	mV_{P-P}
$v_{⑮}$	Sound carrier oscillation output	f=4.5MHz	(a)	1.0	1.7	2.5	V_{P-P}
$v_{③}$	Chroma bias			7.0	7.5	8.0	V
$\lvert v_{④-③}\rvert$	B-Y input			0.70	0.75	0.80	V_{P-P}
$\lvert v_{②-③}\rvert$	R-Y input			0.70	0.75	0.80	V_{P-P}
$C_{①}$	Pin ① input capacitance	f=3.58MHz			4		pF
$R_{①}$	Pin ① input resistance	f=3.58MHz			8.2		kΩ
$C_{⑱}$	Pin ⑱ input capacitance	f=3.58MHz			4		pF
$R_{⑱}$	Pin ⑱ input resistance	f=3.58MHz			8.2		kΩ

THERMAL DERATING (MAXIMUM RATING)

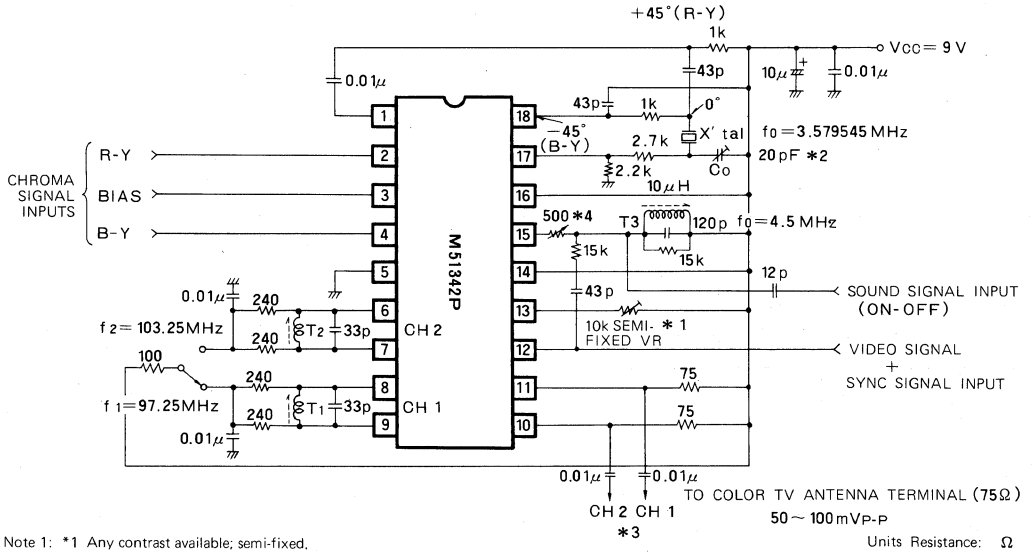


TEST CIRCUIT

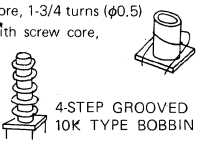


Note: T 1, T2 : Bobbins with screw core, 1¾ TURN (φ0.5)

APPLICATION EXAMPLE



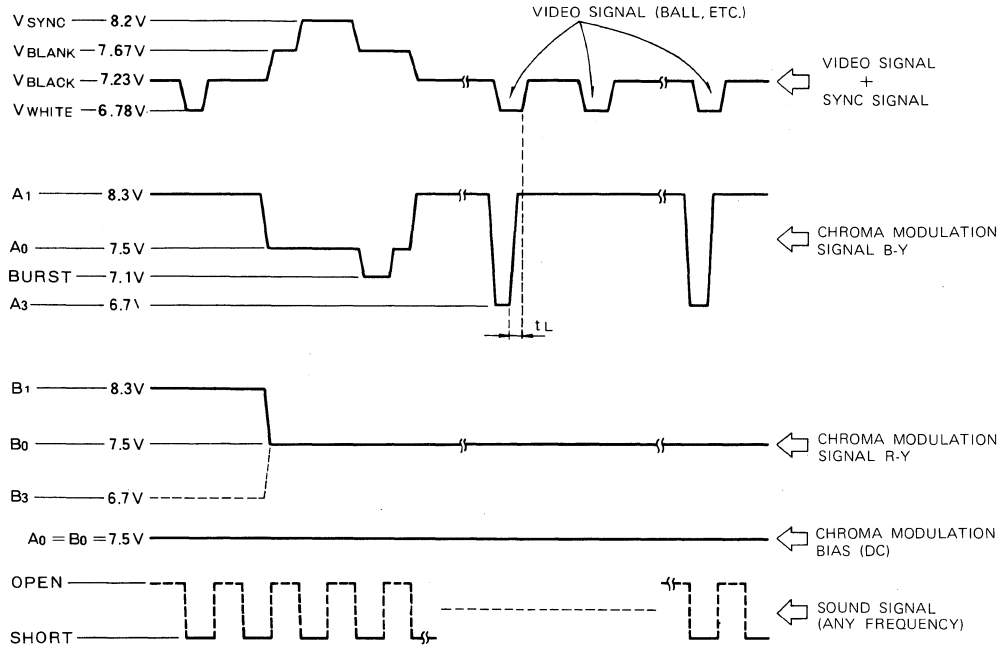
Note 1: *1 Any contrast available; semi-fixed.
*2 C_o is for phase shifting; 20pF is typ capacitance.
*3 Sideband filter and spurious noise suppressor filter may be connected if required.
2: Transformer specifications
T_1, T_2 : Bobbins with screw core, 1-3/4 turns (φ0.5)
T_3 : 10K type bobbin with screw core, pot core, approx. 30 turns (φ0.1)



Note 3: *4 Resistor for 4.5MHz oscillation adjustment.
4: Adjust 43pF and 1k parts to yield 90° relative angle between color subcarrier B-Y and R-Y signal and also identical amplitude.

PRECAUTIONS FOR USE

M51342P standard input signal (V_{CC} = 9V)



Note 1: Set the level of the V_{BLACK} and V_{WHITE} video signals so that there is no suppression of black or white on the screen.

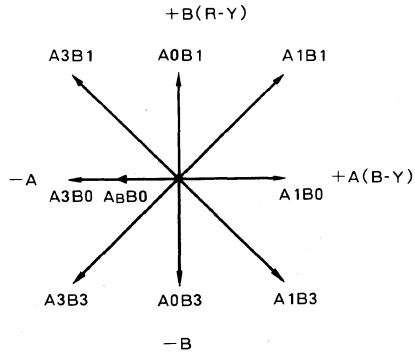
2: If the positions of the video and chroma signals should deviate, shift the phase of these signals only during the terminal period of the signals (pictures of ball, line, etc.)

Note 3: The chroma modulation signal has a standard ±0.8V deviation from the 7.5V (typ) bias although ±10% is allowable after the screen has been checked.

Any type of color may be chosen in accordance with the chroma modulation signals B-Y and R-Y level ratio and the absolute level. The figure below shows the color vectors under the standard operating state.

4: Use V_{cc} or GND to short the sound signal.

Relationship of chroma modulation signals with chroma bias and approximate colors



Color modulation signal level (7.5V reference)		Approximate color
Chroma A (B-Y)	Chroma B (R-Y)	
A0 = 0 V	B0 = 0 V	Light gray
A0 = 0 V	B1 = +0.8V	Red
A0 = 0 V	B3 = −0.8V	Cyan
A1 = +0.8V	B0 = 0V	Blue
A1 = +0.8V	B1 = +0.8V	Magenta
A1 = +0.8V	B3 = −0.8V	Blue cyan
A3 = −0.8V	B0 = 0 V	Yellow
A3 = −0.8V	B1 = +0.8V	Orange
A3 = −0.8V	B3 = −0.8V	Green
$A_{B\,(BURST)}$ = −0.4V	B0 = 0 V	Burst

M5135P

TV AFT CIRCUIT

DESCRIPTION

The M5135P is a semiconductor integrated circuit consisting of an AFT circuit designed for applications in TV tuner automatic frequency control. It includes an RF amplifier/limiter, phase detector, differential DC amplifier, bias regulator circuit and a voltage regulator using a zener diode. It has the same functions and pin connections as the M5134P, and it requires virtually the same external circuit. However, it is characterized by an input sensitivity which has been improved by 20dB.

FEATURES

- High input sensitivity ..... $V_{i(lim)}$ = 18mVrms (typ)
- Built-in regulated power supply with zener diode
- Differential input amplifier and limiter provided
- Differential output available

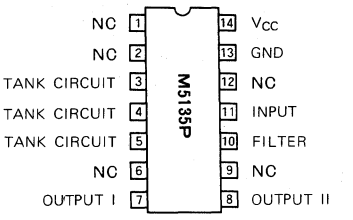
APPLICATION

TV AFT circuits

RECOMMENDED OPERATING CONDITIONS

Rated supply voltage ..... 18V (with R_s = 510Ω)

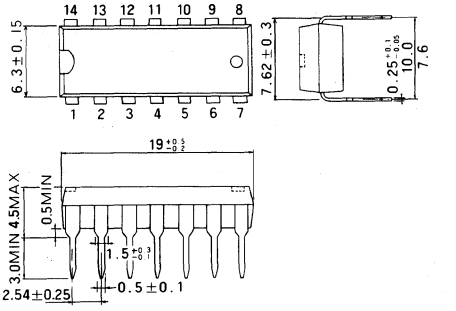
PIN CONFIGURATION (TOP VIEW)



NC : NO CONNECTION

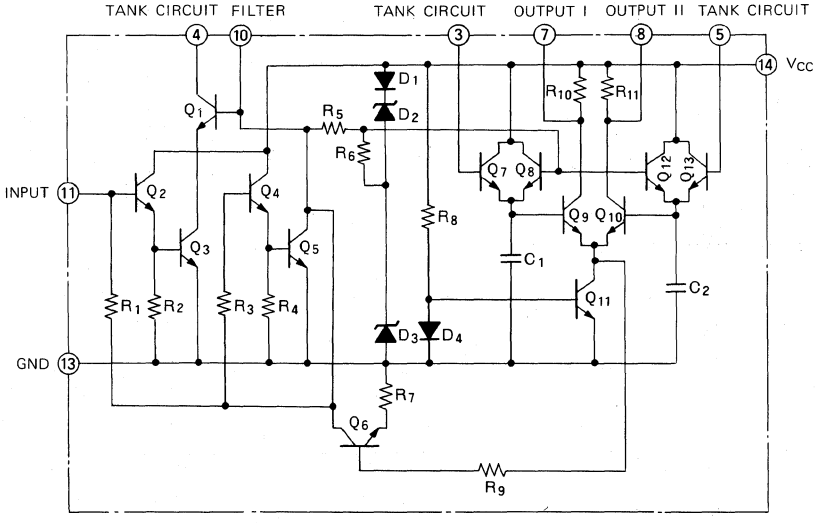
PACKAGE OUTLINE

Dimensions in mm



14-pin plastic DIL package

EQUIVALENT CIRCUIT



MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS (Ta=25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
I_{CC}	Circuit current (pin ⑭)		50	mA
P_d	Power dissipation		700	mW
K_θ	Derating	Ta≧25℃	7.0	mW/℃
Topr	Operating temperature		−20～+75	℃
Tstg	Storage temperature		−40～+125	℃

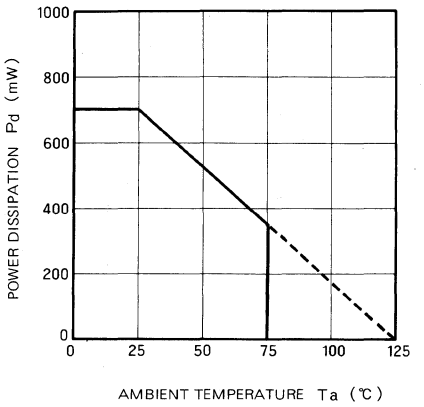
ELECTRICAL CHARACTERISTICS (Ta=25℃)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
P_d	Power dissipation	V_{CC}=18.0V, R_S=510Ω		130	140	150	mW
I_{CC}	Circuit current	$V_{⑭}$=10.5V		4.0	6.5	9.5	mA
$V_{⑭}$	Zener voltage	V_{CC}=18.0V R_S=510Ω		10.9	11.8	12.8	V
$I_{④}$	Pin ④ sink current			1	2	4	mA
$V_{⑦}$	Pin ⑦ output voltage			5.0	6.9	8.0	V
$V_{⑧}$	Pin ⑧ output voltage			5.0	6.9	8.0	V
$V_{⑦,⑧}$	Pins ⑦, ⑧ offset voltage			−1.0	0	1.0	V
$V_{i(lim)}$	Input limiting voltage				18		mVrms
Δf_1	Pins ⑦, ⑧ control voltage characteristics	V_{CC}=18.0V R_S=510Ω V_i=18mVrms	$V_{⑦,⑧}$=3～10V		60	100	kHz
Δf_2			$V_{⑦,⑧}$=3～10V	1.8	3.0	4.0	MHz

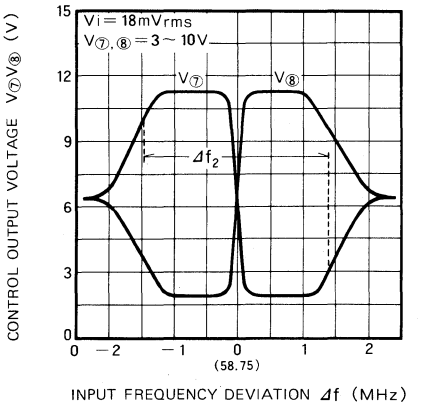
TYPICAL CHARACTERISTICS

(Ta=25℃, V_{CC}=18.0V, R_S=510Ω, unless otherwise noted)

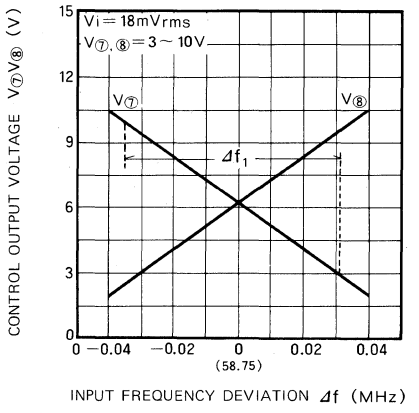
THERMAL DERATING (MAXIMUM RATING)



CONTROL OUTPUT VOLTAGE VS INPUT FREQUENCY DEVIATION

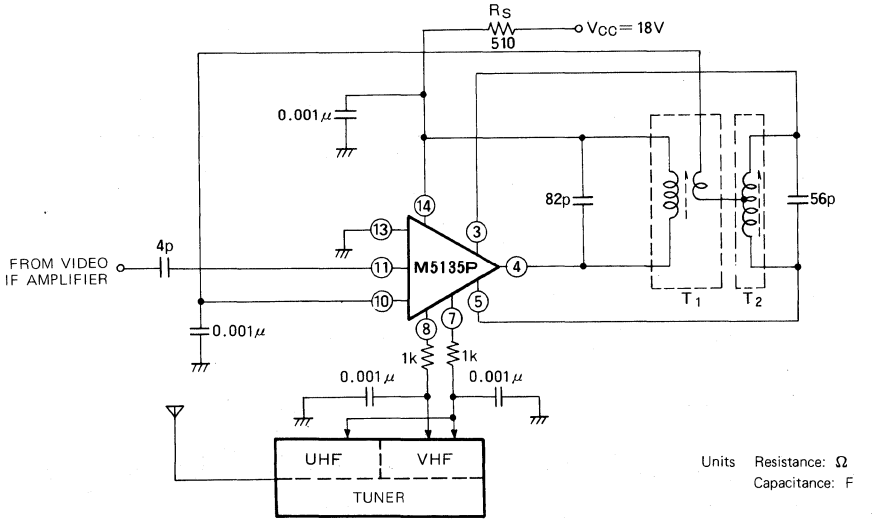


CONTROL OUTPUT VOLTAGE VS INPUT FREQUENCY DEVIATION



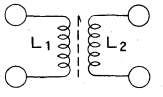
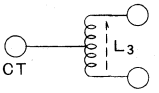
APPLICATION EXAMPLE

Color TV AFT circuit



Units Resistance: Ω
Capacitance: F

Coil specifications (Core material: for T_1, T_2 TDK's M5 ϕ3.3mm×6.5mm screw core or equivalent)

Transformer	Connections		Coil material and turns	Q_O
T_1		L_1	ϕ0.7mm, formar wire, $3\frac{1}{4}$ turns, tightly wound	130
		L_2	ϕ0.7mm, formar wire, $3\frac{1}{4}$ turns, tightly wound	
T_2		L_3	ϕ0.7mm, tin-plated wire, $4\frac{3}{4}$ turns, space wound	150

T_1 : M-6025 (Toko) or equivalent
T_2 : M-6026 (Toko) or equivalent

MITSUBISHI ELECTRIC

M51356P

TV IF SYSTEM

DESCRIPTION

The M51356P is a semiconductor integrated circuit consisting of a VIF amplifier, video detector, sound IF detector, IF/RF AGC, AFT, sound IF limiter amplifier, FM demodulator, electronic attenuator, and audio driver circuit. It provides in a single chip all color TV IF functions including video IF and audio IF.

The M51356P is an effective means of providing high reliability and performance in a small package.

FEATURES

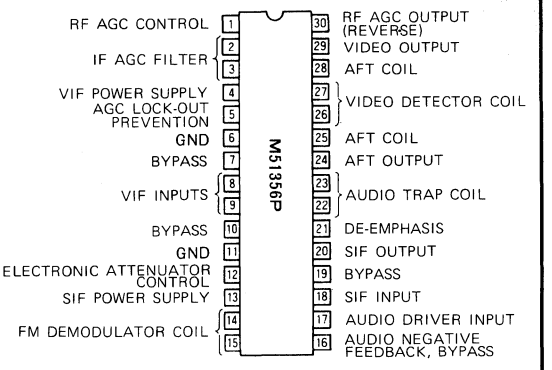
- High density packaging includes VIF, SIF, and audio driver circuits in one chip
- High S/N ratio ..... 57dB, typ. (for high input levels)
- A built-in white spot and black spot noise inverter improves picture quality and stability
- Good AGC characteristics combine with a noise inverter to provide stable synchronization even in the presence of noise
- Negative feedback is used in the audio driver stage for reduced distortion

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... 10~14.5V

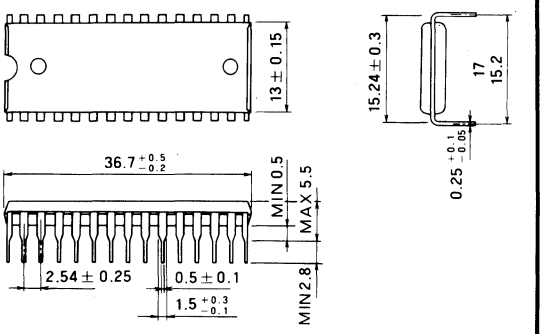
Rated supply voltage 12V

PIN CONFIGURATION (TOP VIEW)



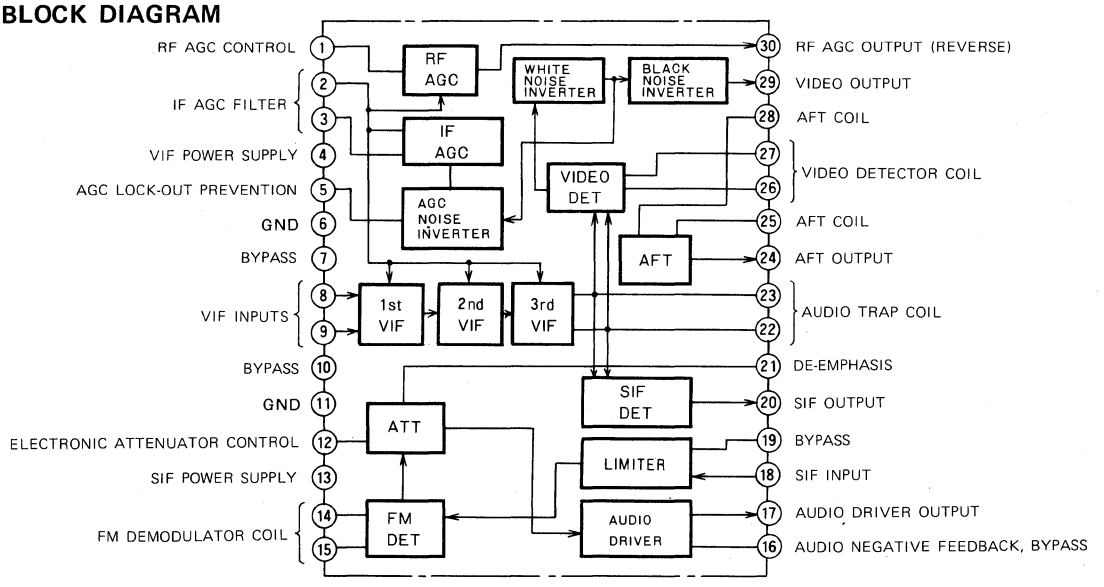
PACKAGE OUTLINT

Dimension in mm



30-pin plastic molded DIL package

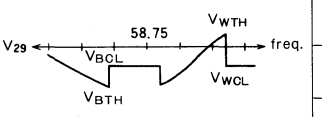
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta=25°C, unless otherwise noted)

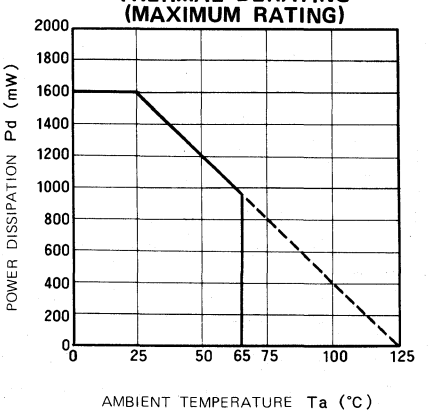
Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		14.4	V
Pd	Power dissipation		1.6	W
Topr	Operating temperature		−20 ~ +65	°C
Tstg	Storage temperature		−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

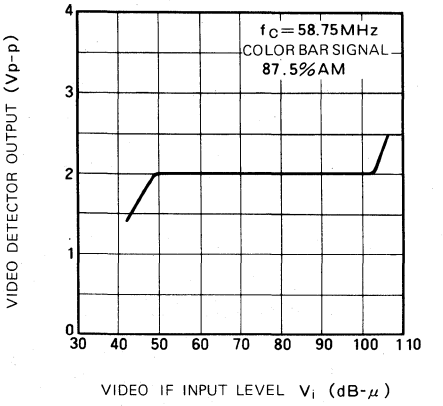
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CC}	Circuit current	V_{CC}=12V	40	60	82	mA
Vin min	Input sensitivity	fp=58.75MHz CW Input level for 0.6V increase in V_{29}		48	54	dBμ
Vin max	Maximum allowable input	fp=58.75MHz CW Input level for 0.6V decrease in V_{29}	100	105		dBμ
GR	AGC range	Vin max − Vin min	48	57		dB
Vodet	Video detector output	fp=58.75MHz, AM74% fm=20kHz	1.75	2.15	2.55	V_{P-P}
BW	Video frequency response	fp=58.75MHz, CW90dBμ, f_B=40~ 58MHz sweep 90dBμ (external AGC B_2 = 0V)	8	12		MHz
V_{30H}	RF AGC maximum voltage	fp=58.75MHz, CW, 50dBμ V_1=4V	9.4	9.8		V
V_{30L}	RF AGC minimum voltage	fp=58.75MHz, CW, 105dBμ V_i=5.0V		0	1.0	V
μ	AFT detector sensitivity	For 100kΩ + 100kΩ load resistance	40	60	85	mV/kHz
$V_{OAF\ max}$	AF maximum output	fp=58.75MHz, CW, 80dBμ V_{12}=10V f_S=54.25MHz, FM7.5kHzdev fm=	800	1200	1600	mVrms
LTM	Limiting sensitivity	f_S=4.5MHz, FM 7.5kHzdev. fm= 400Hz Applied to pin 18		49	53	dBμ
AMR	AMR	f_S=4.5MHz, AM 30%, fm=1kHz, 90dBμ Applied to pin 18	38	43		dB
V_{BTH}	Black spot inverter threshold level	f_C=58.75±5MHz sweep 80dBμ External AGC, V_2=5.8V	2.3	2.7	3.25	V
V_{BCL}	Black spot inverter clamp level		3.7	4.2	4.7	V
V_{WCL}	White spot inverter threshold level		6.6	7.0	7.4	V
V_{WOL}	White spot inverter clamp level		3.9	4.4	4.9	V

TYPICAL CHARACTERISTICS

THERMAL DERATING (MAXIMUM RATING)



AGC CHARACTERISTICS



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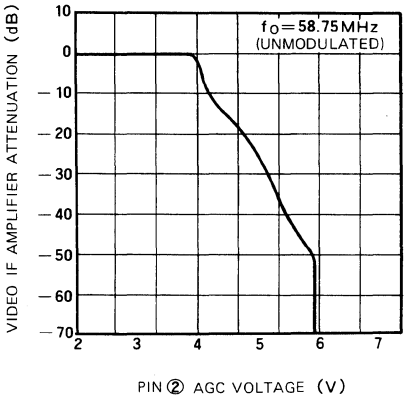
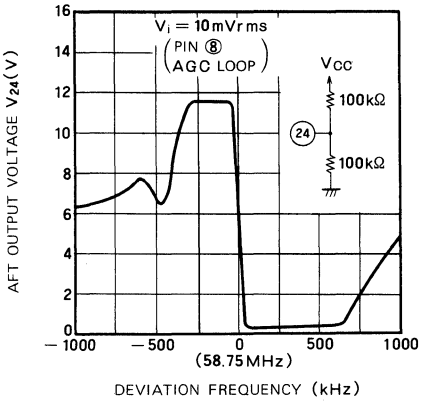
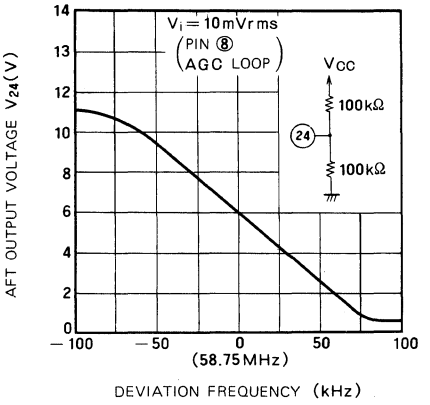
AGC CHARACTERISTICS



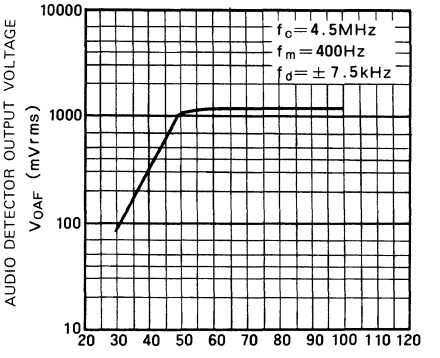
AFT WIDEBAND CHARACTERISTICS



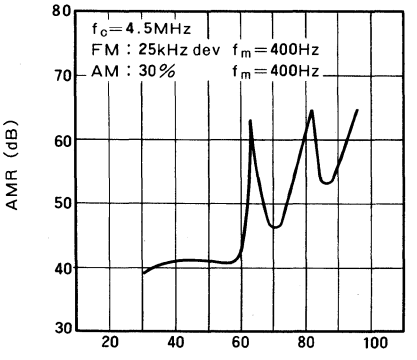
AFT NARROWBAND CHARACTERISTICS



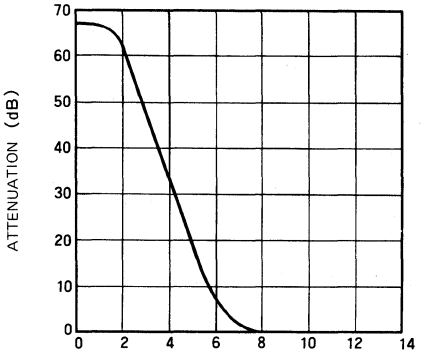
SIF DETECTOR OUTPUT LIMITING



SIF SECTION AMR CHARACTERISTICS



ELECTRONIC VOLUME CONTROL CHARACTERISTICS



Pin①RF AGC Delay Control

By means of a variable resistance the voltage on this pin can be adjusted to allow changes in the threshold voltage at which the RF AGC output (pin ㉚) begins to change. The capacitor C_1 connected to this pin is a high frequency bypass capacitor.

Pin②IF AGC Filter

The time constant is determined by R_1, C_2 and C_3. The internal IC impedance is approximately 2.2kΩ. This filter further smooths the output of the IF AGC filter (pin③), making use of a two-stage circuit.

Pin③IF AGC Filter

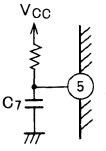
C_4 is charged with a time constant of approximately 10ms during the asynchronous signal period, and discharged with a time constant of approximately 50μs. L_1 is used to prevent ringing.

Pin④Supply Voltage 1 (V_{CC})

Supply voltage pin for the VIF, AGC, LLD, and video amplifier sections. The decoupling capacitors C_5 and C_6 are applied as close as possible to the IC pin, with the ground sides connected as close as possible to pin ⑥.

Pin⑤AGC Lock-Out Prevention

This pin normally has a 0.1~0.45μF capacitor connected to it. The larger the capacitance, the greater the AGC noise cancelling effect is. However, smaller values prevent AGC lock-out so that this capacitance value should be chosen to balance these two effects. If AGC lock-out occurs, a resistance of several hundreds of kilohms is effective when connected between the capacitor and the power supply.



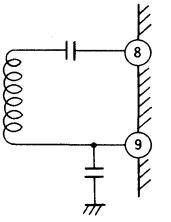
Pin ⑥ Ground 1

Ground pin for the VIF, AGC, LLD, and video amplifier sections. It acts as a quard in the VIF amplifier pin area, preventing feedback from output pins with high-level signals so that further care is required when laying out the PC board (refer to the PC board layout example).

Pins⑦and ⑩ Negative Feedback Bypass

These pins are used to provide DC feedback bypass between the output and input of the VIF amplifier to insure bias stability. Capacitors C_8 and C_{11} provide AC feedback bypass from the output. To improve amplifier stability, capacitors with good high-frequency characteristics should be chosen for C_8 and C_{11} and they should be mounted as close as possible to the IC pins. C_{10} should also have good high-frequency characteristics.

Pins ⑧ and ⑨ VIF Input



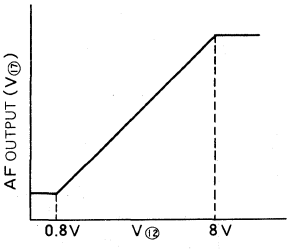
Pin⑧has the same polarity as the VIF output, pin ㉒, and pin⑨has the same polarity as the output pin ㉒. As shown in the application circuit, a transformer coupling through C_9 provides a balanced input configuration. As shown in the circuit at the right, by bypassing one side, a single ended input can be achieved. Gain is reduced, however, and for large input signals, the possibility exists that a difference in output amplitude will arise (pin ㉒ and pin ㉓) so that care is required in this regard. Transformer T_1 acts as an impedance matching device for the IC, and is effective in reducing noise outside of the video IF passband, yielding an improvement in S/N ratio for weak signals. The primary to secondary turns ratio is determined by the matching impedance and gain. The sensitivity of the M51356P at full gain being approximately 48dBμV means that for a tuner with a gain of 30dB the maximum sensitivity is approximately 18μV. If an SAW filter is used after the tuner, in general the SAW filter loss being large, for example 20dB requires that the preamplifier formed by Q_1, R_2~R_5 and C_{12}~C_{14} be used to compensate for this loss (gain 16~20dB). If a low-loss SAW filter (less than 10dB) is used, this preamplifier is not required (T_1 is still required for noise reduction).

Pin ⑪ Ground 2

This is the SIF section ground. To improve stability and prevent interferance to the VIF from the SIF, special care is required in the laying out of the PC board as was explained in the case of Pin ⑥.

Pin ⑫ Electronic Attenuator Control

As shown in the figure at the right, the demodulated AF output is controlled in accordance with the voltage on this pin. Approximately 0.8V provides minimum output while approximately 8V provides maximum output. C_{15} is a high-frequency bypass capacitor.



MITSUBISHI ELECTRIC

Pin ⑬ Power Supply 2 (V_{CC})

This is the power supply for the SIF section. To prevent interferance to the VIF from the SIF harmonics, capacitors C_{16} and C_{17} are connected as close as possible to the IC pin. In addition, to prevent interference via this power supply, the high-frequency choke L_3 is effective. R_{16} is effective in eliminating power supply ripple from the audio stages.

Pins ⑭ and ⑮ SIF Phase Circuit

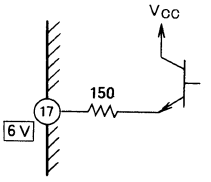
L_4, C_{18}, and C_9 form a peak differential-type FM demodulator circuit. For 4.5MHz, an inductance value of L=18 H with a Q of 60 is appropriate. Since no surge absorbing diode has been used, care should be taken that surge voltages are not applied to pins 14 and 15.

Pin ⑯ Audio Negative Feedback

The gain of the M51356P can be reduced by providing external negative feedback from the output stage, resulting in a reduction in distortion and improvement in gain stability. For the application example, the gain up to the externally connected transistors collector is $1+R_8/R_6$, the gain up to the internal IC pin 17 (audio stage gain) being approximately 18dB (R_C= 1.5kΩ).

Pin ⑰ Audio Driver Output

The output is an emitter follower circuit as shown at the right, the bias voltage being approximately 6V. As shown in the application example, the output transistor can be connected directly to this pin. C_{22} prevents the self oscillation and R_7 is used for internal transistor biasing. An output coupling capacitor may be used to block DC components from the output pin.



Pin ⑱ SIF Input

This is the input for the limiter stage, the input limiting sensitivity being approximately 49dBμV. The input bias resistance is connected to pin ⑲. To prevent interference from the SIF stages to the VIF input, the input to pin ⑱ should be approximately 30mV.

Pin ⑲ SIF Input Bias

C_{23} is a high frequency bypass capacitor. The input stage bias resistor R_9 should be below 10kΩ for amplifier stability. In the application example to achieve ceramic resonator impedance matching a value of 1kΩ is used.

Pin ⑳ Audio Detector Output

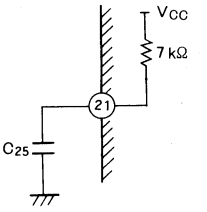
This is the output pin for the audio detector (transistor detector). Normally 90dBμV output is obtainable. The output is connected to a ceramic filter through coupling capacitor C_{24}. For applications in which S/N ratio or buzz noise is a problem, a tuned transformer circuit may be inserted between the ceramic resonator.

Pin ㉑ De-Emphasis

De-emphasis implemented by the combination of the ICs internal resistance (7kΩ, typ.) and C_{25}.

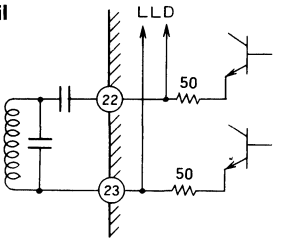
$$t = \frac{1}{2\pi f C_{25} \times 7k\Omega} = 75\mu s$$

The above expression determines the de-emphasis, with a value of 0.01μF being normal.



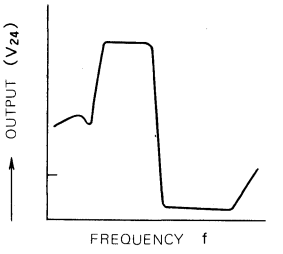
Pins ㉒ and ㉓ Audio Trap Coil

As shown at the Fig. at the right, a shunt-type audio trap is placed between the VIF outputs to lower the audio impedance and attenuate the LLD audio component.



Pin ㉔ AFT Output

The S-curve sloping off to the right as shown at the right is obtained. The voltage at pin 24 (V_{24}) is nearly entirely determined by the divider R_{10}/R_{11}. C_{28} is a high frequency bypass capacitor.

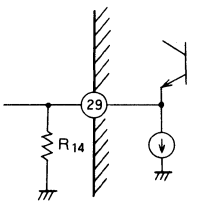


Pins ㉕, ㉖, ㉗, and ㉘ LLD Coil and AFT Coil

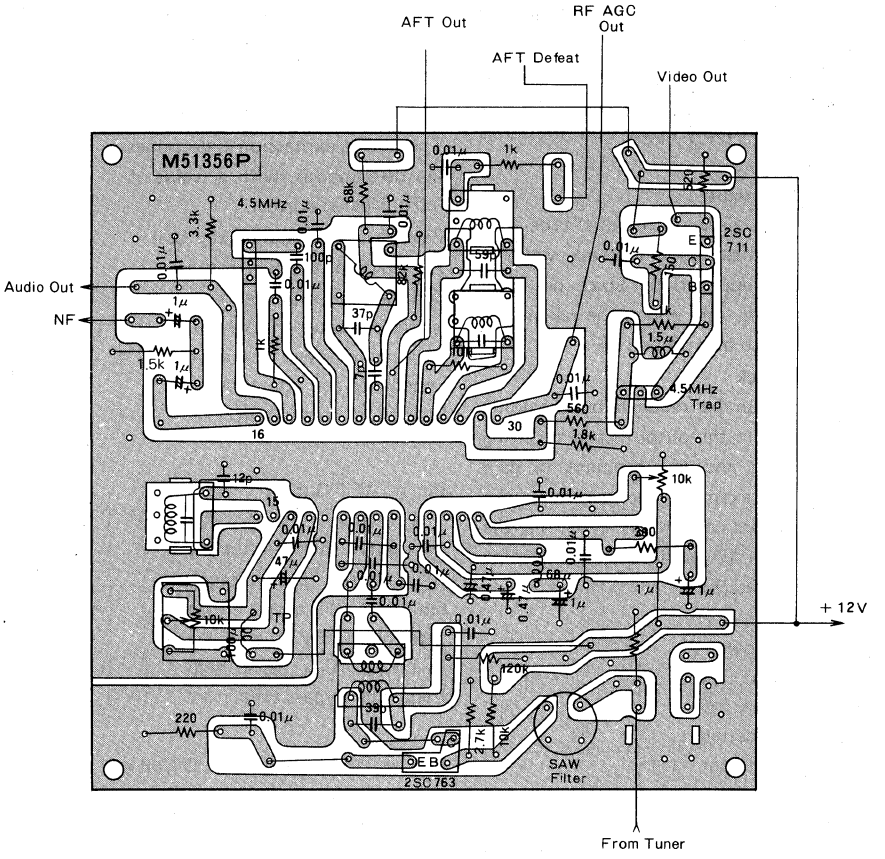
L_6, C_{29}, and R_{12} form the LLD tuning circuit with L_7 and C_{29} forming the AFT tuning circuit. The LLD to AFT coupling is formed by the stray capacitance of the terminal pairs ㉕/㉖ and ㉗/㉘ (comprised of the IC pin capacitance of approximately 1pF and the PC board capacitance), a value of 2pF being ideal. The value of the LLD damping resistance R_{12} should be chosen to match the demodulator output linearity from a value of several kilohms to several tens of kilohms. AFT defeat when channel switching is performed by leaving open or grounding through R_{12} the centertap of L_7. C_{31} is a high-frequency bypass capacitor.

Pin ㉙ Video Output

The internal connection is to an emitter follower output. R_{14} is the emitter follower bias resister (1kΩ or greater should be used) and R_{15} is used to impedance match the audio trap ceramic filter. L_8 is a high-frequency choke and Q_2 is used for bias regulation. With the lower level video sync output, the DC bias for no input is 6V while for signal conditions the edge is 3.5B.



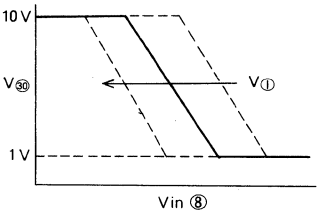
PRINTED CIRCUIT BOARD LAYOUT



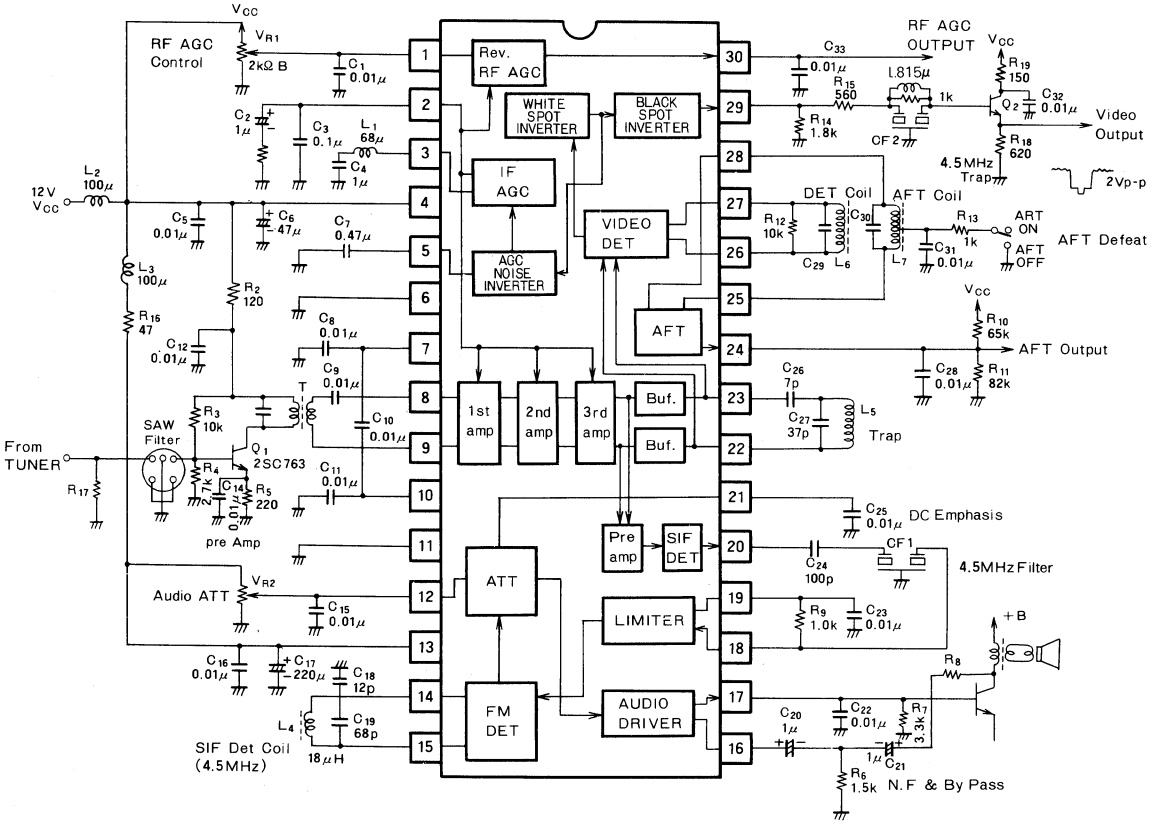
MITSUBISHI ELECTRIC

Pin ㉚ RF AGC Output

A reverse AGC output polarity is obtained with 10V for weak fields and approximately 1V for strong fields, which provides AGC for the tuner. In accordance with the pin ① control voltage V_1, the output changeover point shifts as shown in the figure at the right so that the M51356P can accommodate the tuner characteristics such that the inputs (pins ⑧ and ⑨) never exceed the maximum allowable input.



APPLICATION EXAMPLE



Units Resistance: Ω
Capacitance: F
Inductance: H

M51360L

TV VIDEO IF SYSTEM

DESCRIPTION

The M51360L is a semiconductor integrated circuit consisting of a TV video IF system including a video detector, video amplifier, IF AGC and RF AGC circuits. It makes use of a power-saving design for portable TVs.

FEATURES

- Low voltage operation ..... 4.5V (typ)
- Low power consumption
  ..... 11mA (typ) power supply current
  (at maximum video sensitivity)
- Wideband or narrow band video IF amplifier characteristics may be selected
- Housed in a compact 16-pin ZIL package

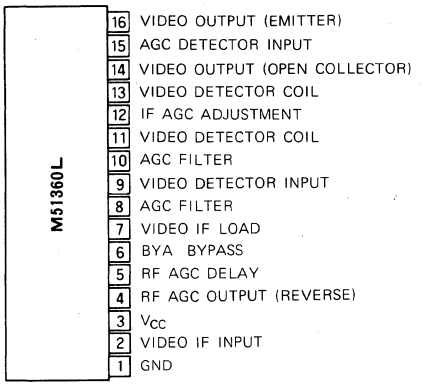
APPLICATION

B/W portable TVs

RECOMMENDED OPERATING CONDITIONS

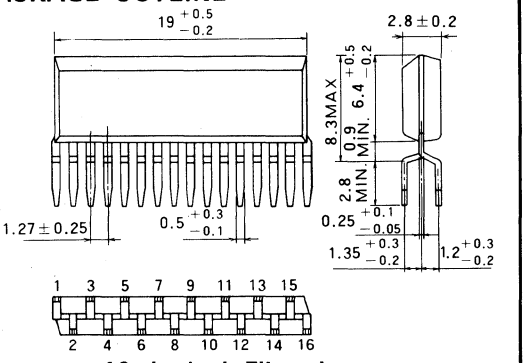
Supply voltage range ..... 3.5~7.5V
Rated supply voltage 4.5V

PIN CONFIGURATION (TOP VIEW)



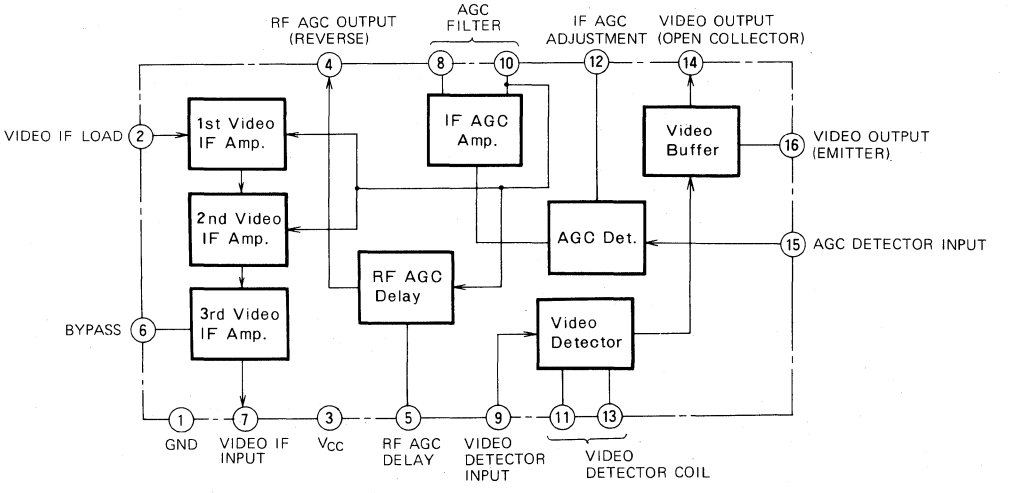
PACKAGE OUTLINE

Dimensions in mm



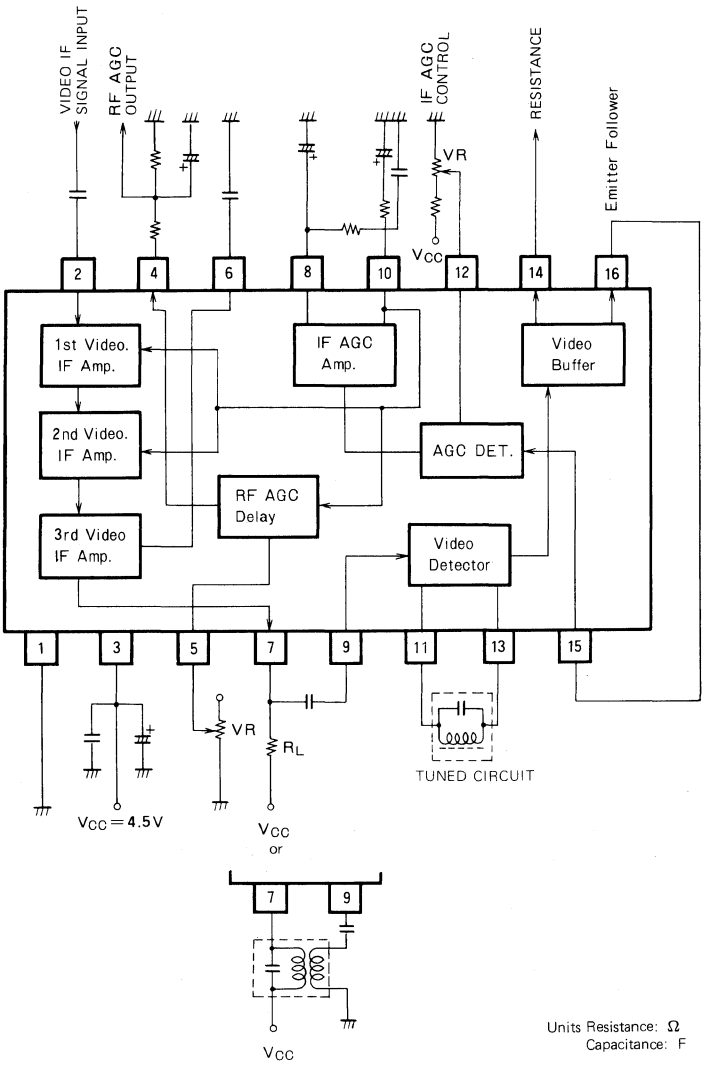
16-pin plastic ZIL package

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

APPLICATION EXAMPLE



M51375P

TV SOUND IF DEMODULATOR

DESCRIPTION

The M51375P is a semiconductor integrated circuir consisting of a TV sound IF circuit including an IF amplifier, FM detector, DC volume control, AF driver, regulated power supply, muting circuit, and DC volume characteristic switching functions. It is housed in a 14-pin molded epoxy resin DIL package.

FEATURES

- Reduced power supply ripple
- Regulated power supply
- Switching of the DC volume characteristics is possible
- Built-in muting circuit
- Excellent AM Rejection ratio

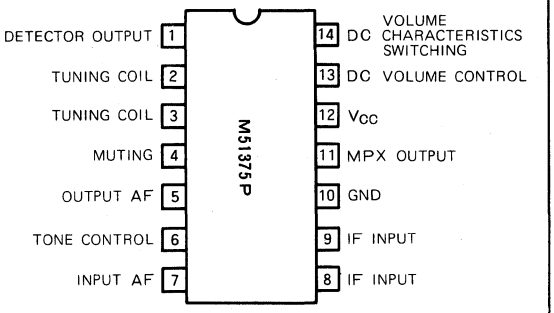
APPLICATION

TV sound IF demodulation

RECOMMENDED OPERATING CONDITIONS

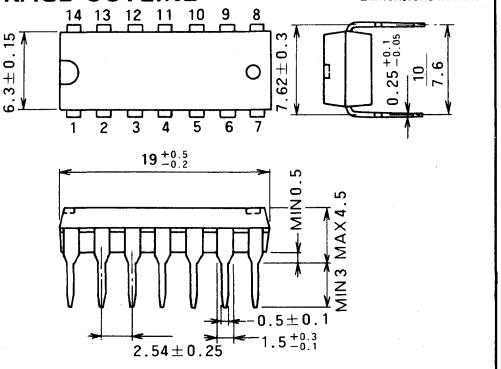
Supply voltage range ..... 11~13V
Rated supply voltage 12V

PIN CONFIGURATION (TOP VIEW)



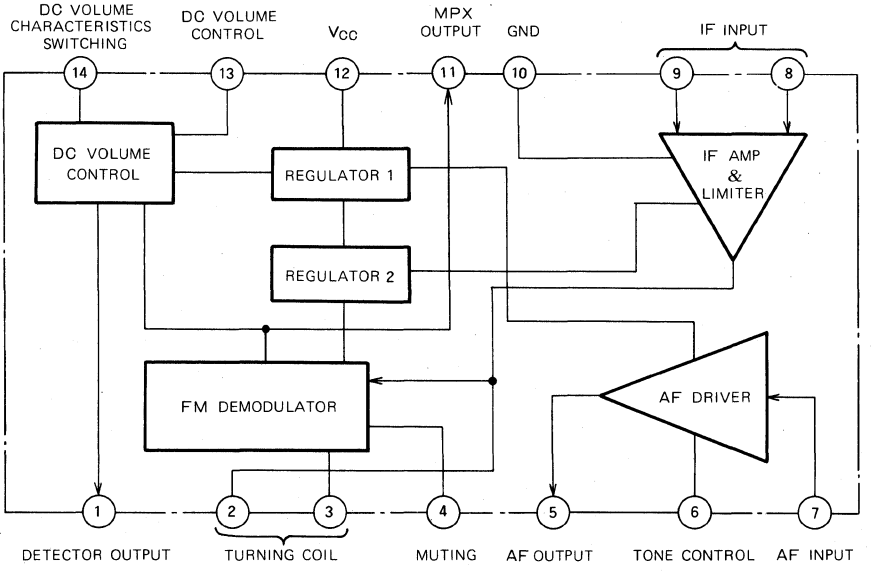
PACKAGE OUTLINE

Dimensions in mm



14-pin plastic DIL package

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

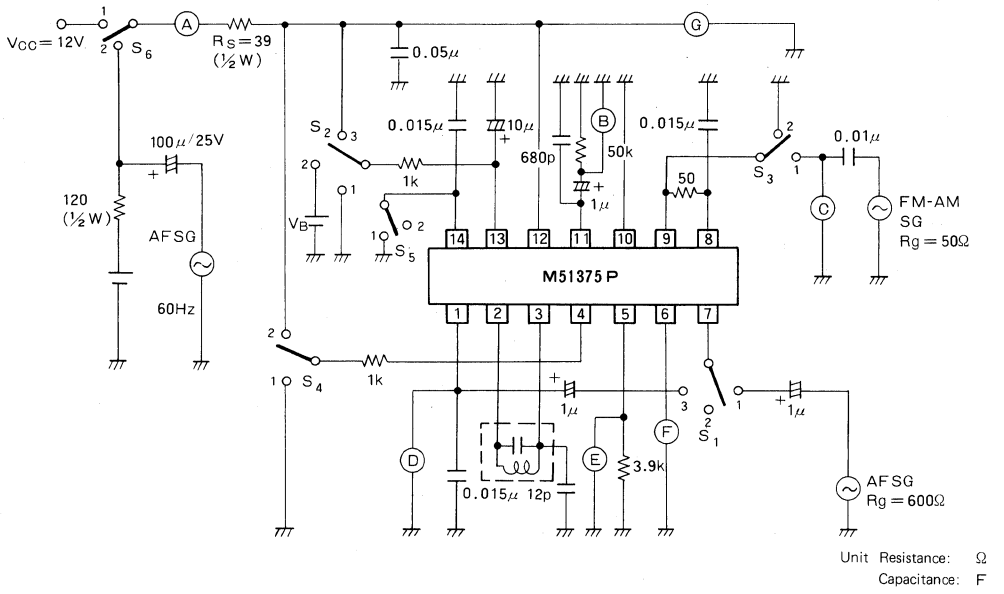
ABSOLUTE MAXIMUM RATINGS (Ta=25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		16	V
$V_{i(IF)}$	Input voltage		± 3	V
P_D	Power dissipation		1.2	W
I_D	Supply current		60	mA
Topr	Operating temperature		−10～+60	℃
Tstg	Storage temperature		−50～+125	℃

ELECTRICAL CHARACTERISTICS (Ta=25℃, V_{CC}=12V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{12}	Circuit voltage characteristics	V_{CC}=12V, R_S=39Ω	10.3	10.5	11.0	V
I_D	Supply current	V_{CC}=12V, R_S=39Ω	30	35	41	mA
$V_{R(ATT)}$	Power supply ripple suppression	V_{CC}=12V±100mVp-p	8			dB
$V_{O(DET)}$	Detector output	Vin=100dBμ, fm=1kHz f=4.5MHz, f_{DEV}=±25kHz	0.30	0.45	0.60	Vrms
$THD_{(DET)}$	Detector output distortion	Vin=100dBμ, fm=1kHz f=4.5MHz, f_{DEV}=±50kHz			5	%
$V_{i(LIM)}$	Input limiting voltage	f=4.5MHz, fm=1kHz f_{DEV}=±25kHz		46	52	dBμ
AMR	AM Rejection ratio	Vin=100dBμ, f=4.5MHz	45			dB
$V_{O(ATT1)}$	DC Volume maximum attenuation	V_B=0	73	75		dB
$V_{O(ATT2)}$	DC Volume attenuation characteristic 1	V_B=1.9V	−25	−22	−19	dB
$V_{O(ATT3)}$	DC Volume attenuation characteristic 2	V_B=5V	−10	−7.5	−5	dB
$V_{O(ATT4)}$	DC Volume attenuation characteristic 3	V_B=5V, V_{14}=0V	−24	−21	−18	dB
$G_{V(AF)}$	AF Driver voltage gain	V_i=100mVrms, f=1kHz	17.5	20	23	dB
$V_{O(AF)MAX}$	Undistorted AF driver output	THD=5%	2.0	2.5		Vrms
$V_{O(ATT5)}$	Muting characteristics				−60	dB
$V_{N(AF)}$	AF Noise	Rg=0Ω			0.5	mVrms
V_6	Pin 6 voltage		2.6	5.5	7.0	V
$V_{N(IF)}$	IF Noise	V_C=100dBμ, f=4.5MHz C.W.			1.0	mVrms

TEST CIRCUIT

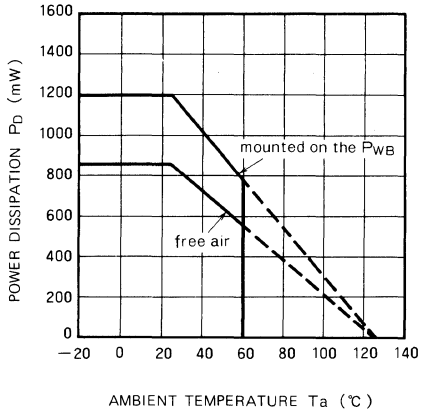


TEST METHODS

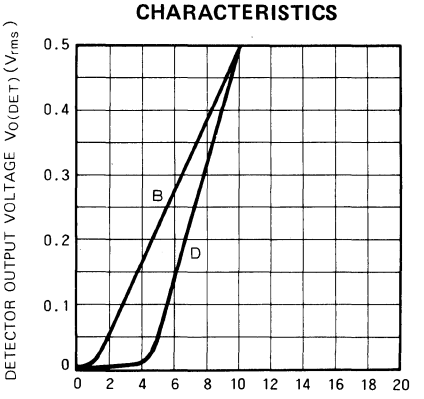
Symbol	S_1	S_2	S_3	S_4	S_5	S_6	Test point	Method
V_{12}	2	3	1	1	1	1	G	V_{CC} = 12V, R_S = 39Ω Read voltmeter
I_D	2	3	1	1	1	1	A	V_{CC} = 12V, R_S = 39Ω Read ammeter
$V_{R(ATT)}$	2	3	1	1	1	2	G	With V_{CC} = 12V ± 100mVp-p applied, and V_O as the output (mVp-p) at point G, $V_{R(ATT)}$ = log 200/V_O
$V_{O(DET)}$	2	3	1	1	1	1	B	V_{in} = 100dBμ, f = 4.5MHz f = 1kHz, f_{DEV} = ±25kHz } Read voltmeter
$THD_{(DET)}$	2	3	1	1	1	1	D	Vin = 100dBμ, f = 4.5MHz fm = 1kHz, f_{DEV} = ±50kHz } Read distortion meter
$V_{I(LIM)}$	2	3	1	1	1	1	C	Read input level when the detector output is 3dB lower than $V_{O(DET)}$
AMR	2	3	1	1	1	1	D	FM : fm = 1kHz, f_{DEV} = ±25kHz → $V_{O(DET)FM}$ AM : fm = 1kHz, 30% → $V_{O(DET)AM}$ $AMR = 20\log\frac{V_{O(DET)FM}}{V_{O(DET)AM}}$
$V_{O(ATT1)}$	2	1	1	1	1	1	D	With $V_{O(DET)1}$ as the detector output with V_B = 0, $V_{O(ATT1)} = 20\log V_{O(DET)}/V_{O(DET)1}$
$V_{O(ATT2)}$	2	2	1	1	1	1	D	With $V_{O(DET)2}$ as the detector output with V_B = 1.9V, $V_{O(ATT2)} = 20\log V_{O(DET)2}/V_{O(DET)}$
$V_{O(ATT3)}$	2	2	1	1	1	1	D	With $V_{O(DET)3}$ as the detector output with V_B = 5V, $V_{O(ATT3)} = 20\log V_{O(DET)3}/V_{O(DET)}$
$V_{O(ATT4)}$	2	2	1	1	2	1	D	With $V_{O(DET)4}$ as the detector output with V_B = 5V and V_{14} = 0V, $V_{O(ATT4)} = 20\log V_{O(DET)4}/V_{O(DET)}$
$G_{U(AF)}$	1	1	—	—	—	1	E	With $V_{O(AF)(mVrms)}$ as the AF output with f = 1kHz, Vi = 100mVrms, $G_V = 20\log V_{O(AF1)}/100$
$V_{O(AF)MAX}$	1	1	—	—	—	1	E	Read the AF output level with f = 1kHz, THD = 5%
$V_{O(ATT5)}$	2	3	1	2	—	1	D	With Vin = 100dBμ, f = 4.5MHz fm = 1kHz, f_{DEV} = ±25kHz, and muting applied, if $V_{O(DET)5}$ is the detector output, $V_{O(ATT5)} = 20\log V_{O(DET)5}/V_{O(DET)}$
$V_{N(AF)}$	3	1	2	1	—	1	E	Read voltmeter with no input
V_6	2	—	—	2	1	1	F	Read voltmeter with no input
$V_{N(IF)}$	2	3	1	1	1	1	D	Read voltmeter with f = 4.5MHz C.W.

TYPICAL CHARACTERISTICS

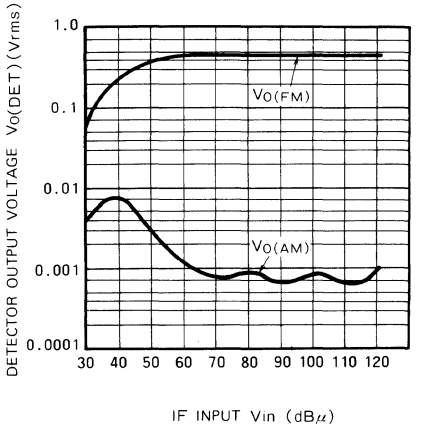
THERMAL DERATING



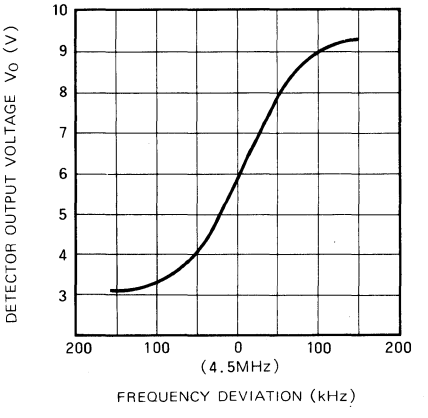
DC VOLUME ATTENUATION CHARACTERISTICS



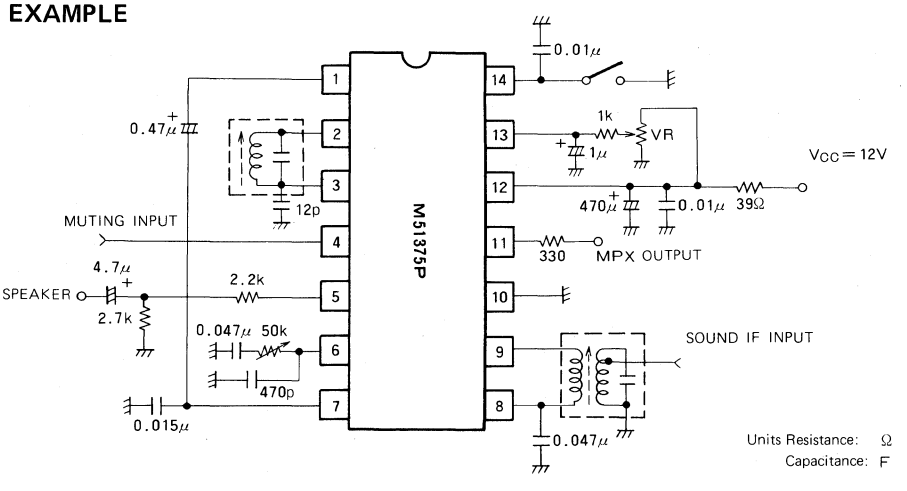
AM REJECTION RATIO CHARACTERISTICS



S-CURVE CHARACTERISTICS



APPLICATION EXAMPLE



M51378L

TV AUDIO IF DEMODULATOR

DESCRIPTION

The M51378L is a semiconductor integrated circuit consisting of an audio IF demodulator circuit designed for use in small portable TV receivers.

The circuit includes an audio IF amplifier, limiter and differential peak-type FM detector.

FEATURES

- Low-voltage, low-current operation for low power consumption ..... V_{cc} = 4.5V(TYP), I_{cco} = 5mA(TYP)
- Wide operating supply voltage range ..... V_{cc} = 3.2 ~ 7.5V
- Small 8-pin SIL package

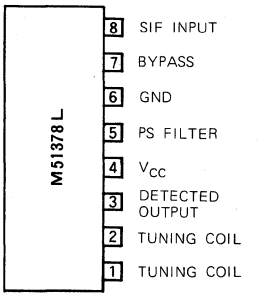
APPLICATION

Small portable TV audio IF demodulator circuits

RECOMMENDED OPERATING CONDITIONS

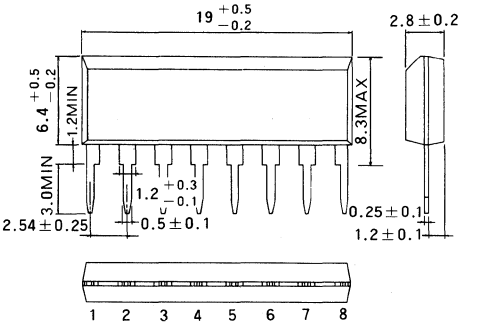
Supply voltage range ..... 3.2 ~ 7.5V
Rated supply voltage 4.5V

PIN CONFIGURATION (TOP VIEW)



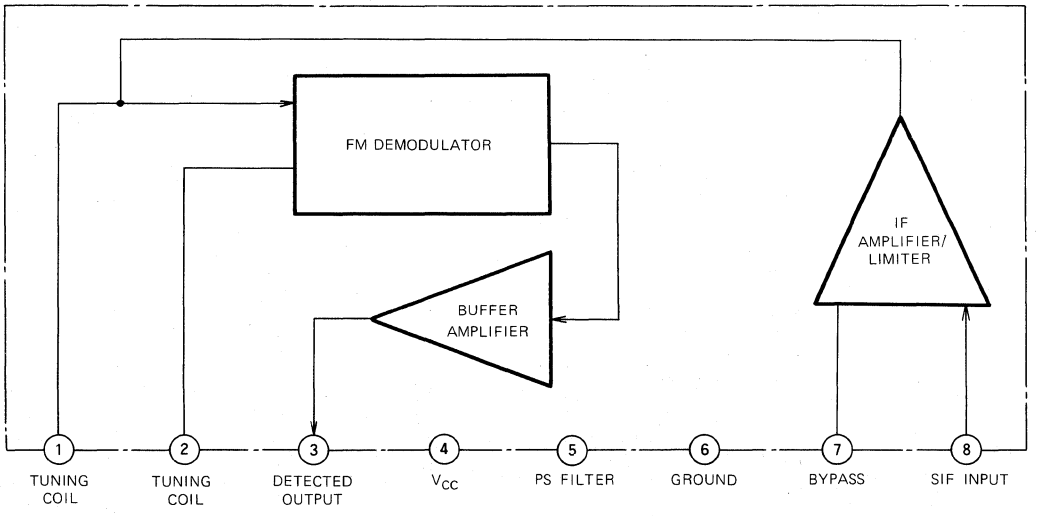
PACKAGE OUTLINE

Dimensions in mm



8-pin plastic SIL package

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

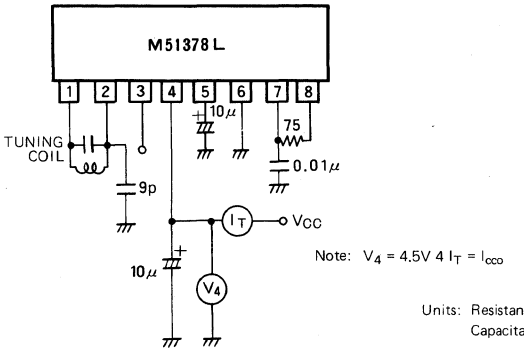
Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		7.5	V
$V_{i(IF)}$	Input signal voltage (between pins ⑦ and ⑧)		±3	V
I_{CC}	Circuit current		15	mA
Pd	Power dissipation		500	mW
K_θ	Derating	Ta ≧ 25℃	5	mW/℃
Topr	Operating temperature		−20 ~ +75	℃
Tstg	Storage temperature		−40 ~ +125	℃

ELECTRICAL CHARACTERISTICS (Ta = 25℃, V_{CC} = 4.5V, unless otherwise noted)

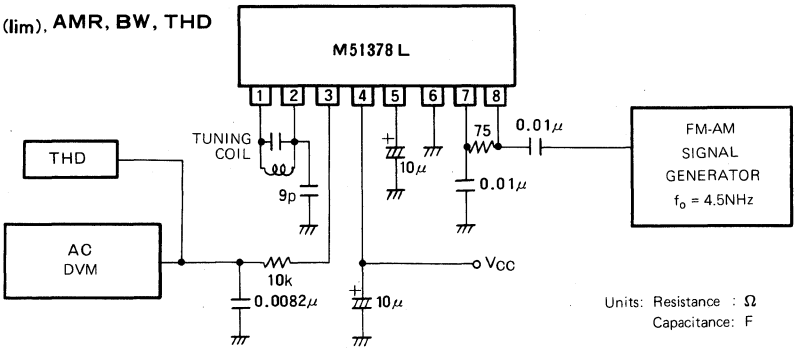
Symbol	Parameter	Test conditions	Test circuit	Limits			Unit
				Min	Typ	Max	
I_{CCO}	Quiescent circuit current	Zero signal condition	(a)		5.0	6.0	mA
$V_{i(lim)}$	Input limiting voltage	fo = 4.5MHz, fm = 400Hz fd = ±7.5kHz	(b)		46	50	dBμ
$V_{o(af)}$	Detector output voltage	fo = 4.5MHz, fm = 400Hz fd = ±7.5kHz, Vi = 100dBμ	(b)	41	58	82	mVrms
AMR	AM rejection ratio	FM : fd = ±25kHz, Vi = 100dBμ AM : 400Hz, 30%Mod.	(b)	35	40		dB
BW	Bandwidth	fm = 400Hz fd = ±7.5kHz	(b)		150		kHz
$V_{CC(op)}$	Supply voltage range	Required for operation		3.2	4.5	7.5	V
THD	Total harmonic distortion	fo = 4.5MHz, fm = 400Hz fd = ±7.5kHz, Vi = 100dBμ	(b)		0.3	1.0	%

TEST CIRCUITS

(a) I_{CCO}

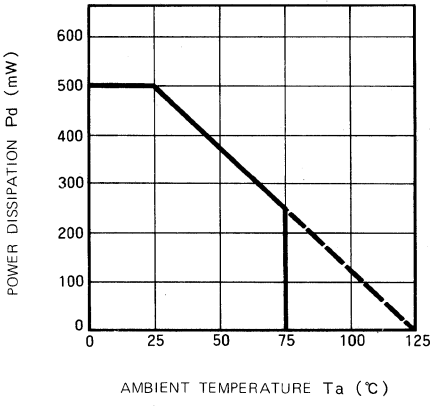


(b) $V_{o(af)}$, $V_{i(lim)}$, AMR, BW, THD

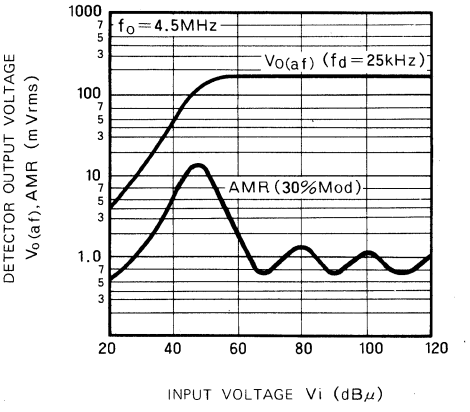


TYPICAL CHARACTERISTICS (Ta = 25℃, V_{CC} = 4.5V, Unless otherwise noted)

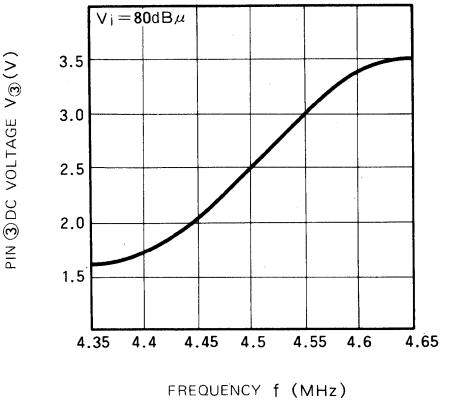
THERMAL DERATING (MAXIMUM RATING)



DETECTOR OUTPUT LIMITING

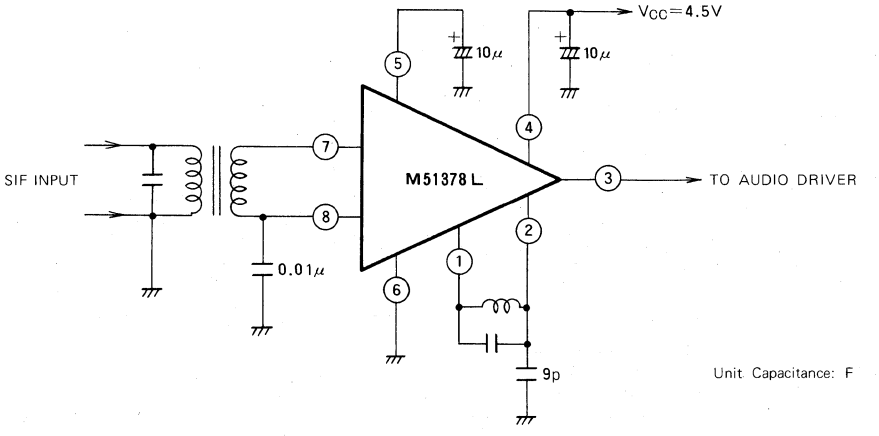


S-CURVE CHARACTERISTICS



APPLICATION EXAMPLE

Small portable TV audio IF demodulator circuit



M51380P/M51381P

TV VIDEO SIGNAL PROCESSOR

DESCRIPTION

The M51380P is a semiconductor integrated circuit consisting of a circuit designed for use as a TV video signal processing circuit with video tone control, brightness control, contrast control, pedestal clamping (variable DC regeneration ratio) and video drive functions. It is housed in a 16-pin package.

Apart from the variable DC regeneration ratio function, the M51381P has all the functions of the M51380P and is housed in a 14-pin package. The corresponding pins of the two units are given at the end of the section.

FEATURES

- Video tone, brightness and contrast adjustment with DC voltage control
- Two-level differentiation for video tone adjustment; external peaking pin allows overshooting and preshooting to be set as desired
- Variable DC regeneration ratio (M51380P only)
- Color signal output transistor can be driven directly.
- Built-in peak limiter circuit

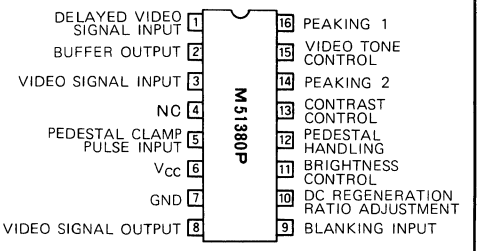
APPLICATION

TV video signal processing

RECOMMENDED OPERATING CONDITIONS

Supply voltage ..... 11.0 ~ 13.0V
Rated supply voltage 12.0V

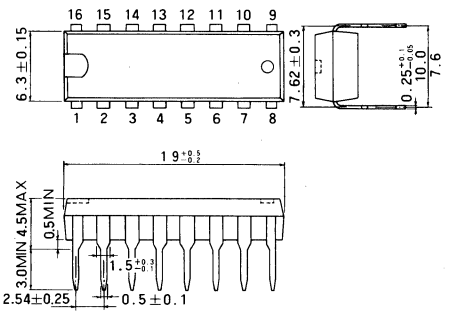
PIN CONFIGURATION (TOP VIEW)



NC: NO CONNECTION

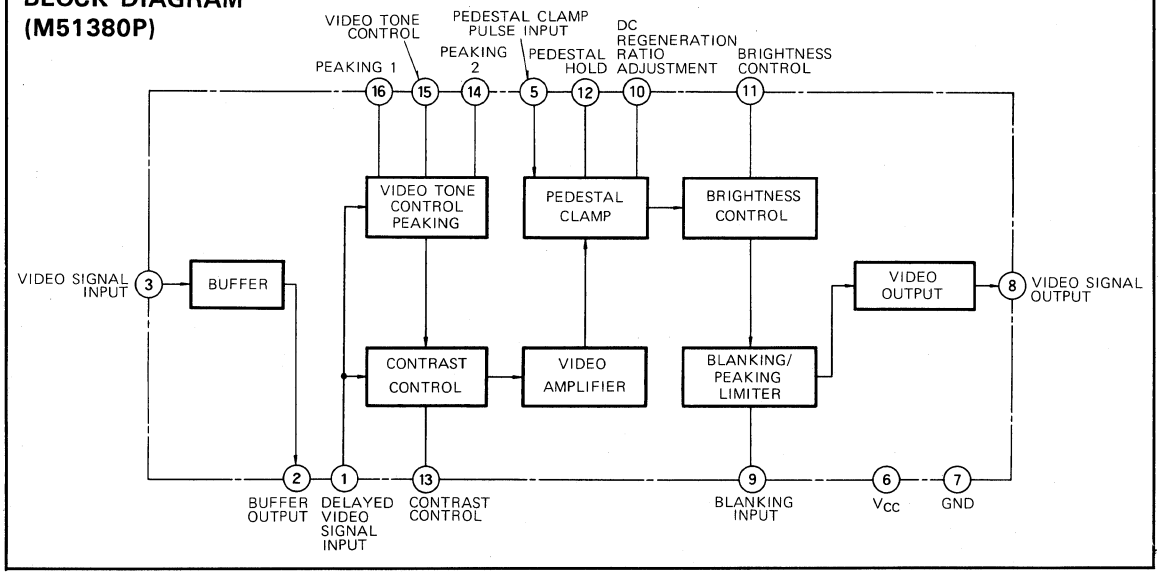
PACKAGE OUTLINE

Dimensions in mm



16-pin plastic DIL package

BLOCK DIAGRAM (M51380P)



ABSOLUTE MAXIMUM RATINGS (Ta=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		16.0	V
Pd	Power dissipation		700	mW
K_θ	Derating	Ta≧25°C	7	mW/°C
Topr	Operating temperature		−20～+75	°C
Tstg	Storage temperature		−40～+125	°C

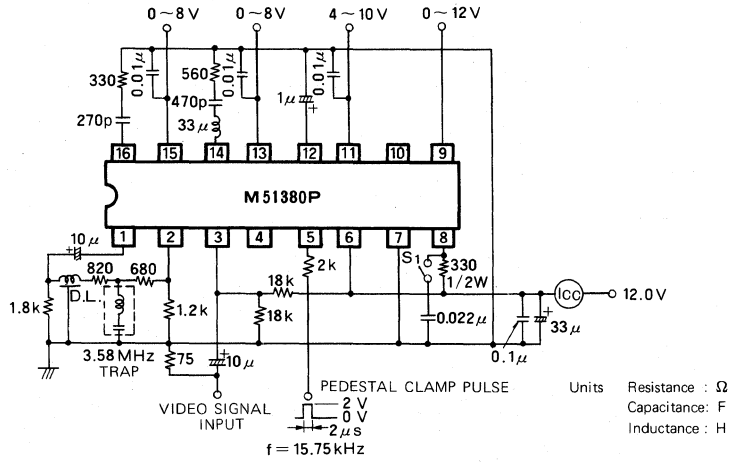
ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{CC}=12.0V, unless otherwise noted)

Symbol	Parameter	Test conditions					Limits			Unit
		Video signal Note:	Pin ⑨ (V)	Pin ⑪ (V)	Pin ⑬ (V)	Pin ⑮ (V)	Min.	Typ	Max.	
I_{CC1}	Circuit current 1	OFF	0	7.0	6.0	0	29	37	44	mA
I_{CC2}	Circuit current 2	OFF	12.0	7.0	6.0	0	20	25	30	mA
Vo max	Maximum video output	II	0	7.0	8.0	0	7.0	8.0		V_{P-P}
$G_V$max	Maximum video voltage gain	I	0	7.0	8.0	0	8.5	12.0	15.5	dB
Vplim	Peak limiter operating voltage	OFF	5.0	4.0	6.0	0	3.9	4.2	4.5	V_{O-P}
V_{BLK}	Blanking operating voltage	OFF	5～6	4.0	6.0	0	5.0	5.4	5.7	V_{O-P}
f_B	Frequency band response	I, IV	0	7.0	6.0	0	−8	−6	−4	dB
Gp max	Maximum video peaking	II, III	0	7.0	6.0	8.0	13.5	16	20.5	dB
$\delta V_{ODC}/\delta Ta$	Video output pin voltage temperature dependence	OFF	0	7.0	6.0	0	0	2	4	mV/°C

Note: Video signal

	Signal content
I	200mVp-p, 100kHz sine wave
II	3.0Vp-p, 100kHz sine wave
III	200mVp-p, 2.0MHz sine wave
IV	200mVp-p, 4.0MHz sine wave

TEST CIRCUIT



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TEST METHODS

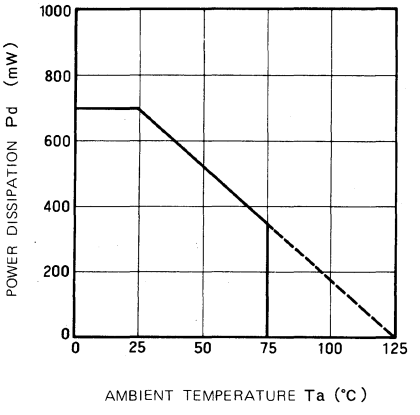
Symbol	Method
Vplim	DC voltage of pin⑧ scanning period. Set S_1 to ON.
V_{BLK}	Voltage of pin ⑨ when pin ⑧ voltage changes suddenly.
f_B	Output ratio at pin ⑧ with signals I and IV is expressed in decibels.
G_{pmax}	Output ratio at pin ⑧ with signals II and III is expressed in decibels.

CORRESPONDING PINS OF M51380P and M51381P

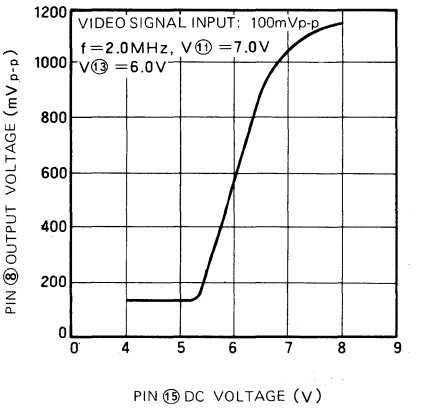
M51380P pin no.	①	②	③	④	⑤	⑥	⑦	⑧	⑨	⑩	⑪	⑫	⑬	⑭	⑮	⑯
M51381P pin no.	①	②	③	—	④	⑤	⑥	⑦	⑧	—	⑨	⑩	⑪	⑫	⑬	⑭

TYPICAL CHARACTERISTICS (Ta=25°C, Vcc=12.0V, unless otherwise noted)

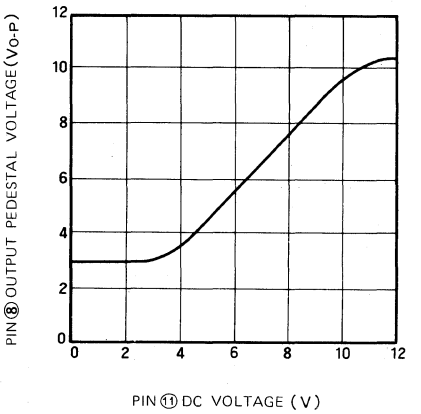
THERMAL DERATING (MAXIMUM RATING)



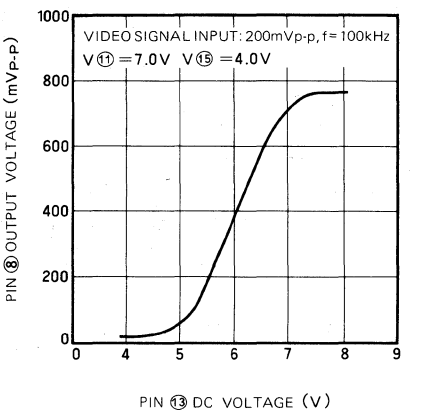
PICTURE QUALITY CONTROL



BRIGHTNESS CONTROL



CONTRAST CONTROL



M51382P

TV VIDEO SIGNAL PROCESSOR

DESCRIPTION

The M51382P is a semiconductor integrated circuit consisting of a TV video signal processing circuit which includes a brightness control, contrast control, pedestal clamping and video drive functions.

FEATURES

- DC control of brightness and contrast
- Can directly drive chroma output transistors
- Peak limiter circuit
- Color tracking circuit

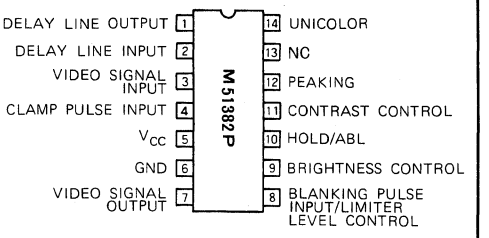
APPLICATION

TV video signal processing

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... 11~13V
Rated supply voltage 12V

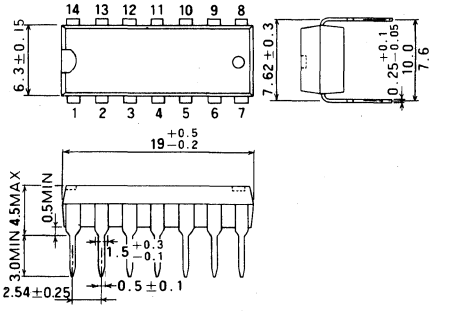
PIN CONFIGURATION (TOP VIEW)



NC: NO CONNECTION

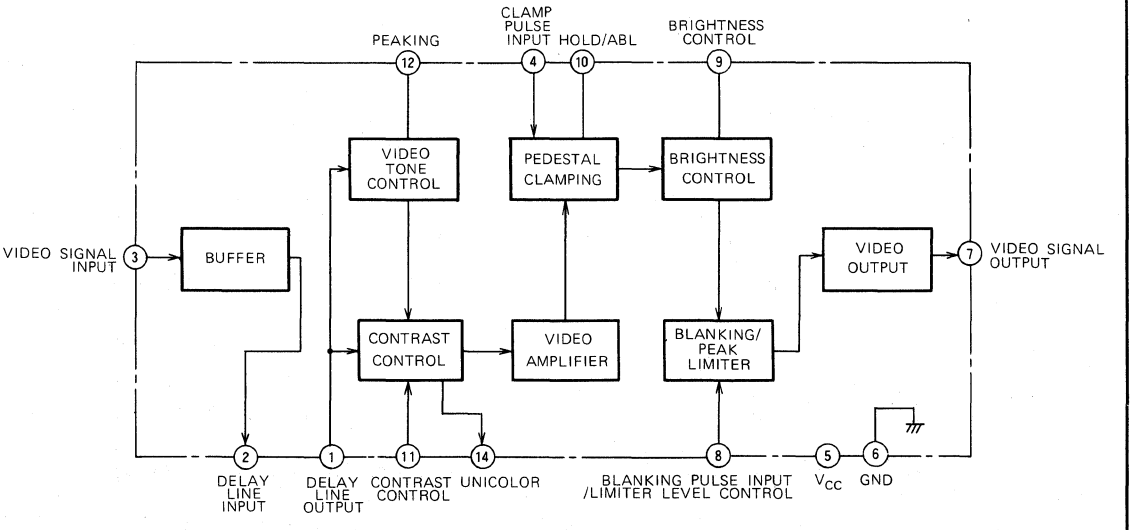
PACKAGE OUTLINE

Dimensions in mm



14-pin plastic DIL package

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS (Ta=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		16	V
Pd	Power dissipation		700	mW
K_θ	Derating	Ta≧25°C	7	mW/°C
Topr	Operating temperature		−20～+75	°C
Tstg	Storage temperature		−40～+125	°C

ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{CC}=12V)

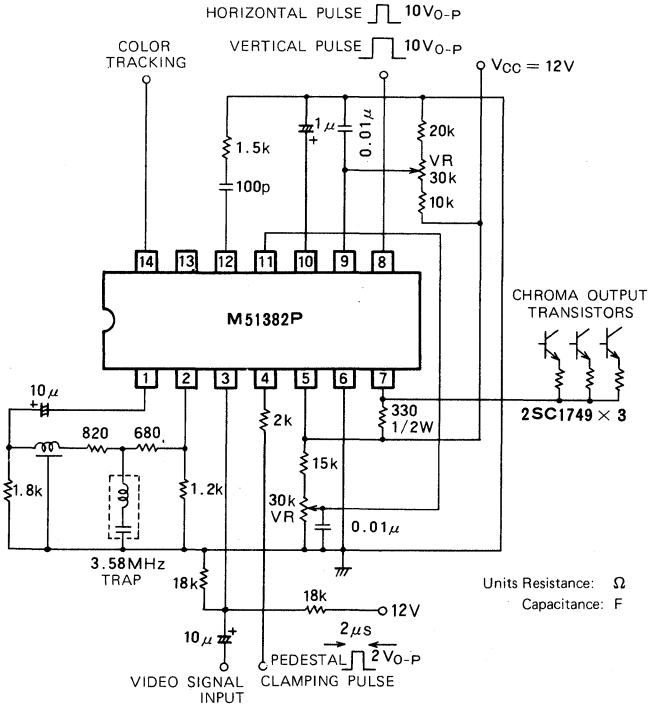
Symbol	Parameter	Test conditions				Limits			Unit
		Video signal Note	Pin ⑧ (V)	Pin ⑨ (V)	Pin ⑪ (V)	Min	Typ	Max	
I_{CC1}	Circuit current (1)	OFF	0	7.0	6.0	28	37	44	mA
I_{CC2}	Circuit current (2)	OFF	12.0	7.0	6.0	17	26	32	mA
$V_O$max	Maximum video output	II	0	7.0	8.0	7.0	8.0		V_{P-P}
$G_V$max	Maximum video voltage gain	I	0	7.0	8.0	8.5	12.0	15.5	dB
$V_P$lim	Peak limiter operating voltage	OFF	5.0	4.0	6.0	3.9	4.2	4.5	V_{O-P}
V_{BLK}	Blanking operating voltage	OFF	12.0	4.0	6.0	10.0			V_{O-P}
f_B	Frequency band characteristics	I, III	0	7.0	6.0	−8.0	−6.0	−4.0	dB
$\delta V_{ODC}/\delta Ta$	Video output voltage temperature dependence	OFF	0	7.0	6.0	0	2	4	mV/°C

Note Video signal

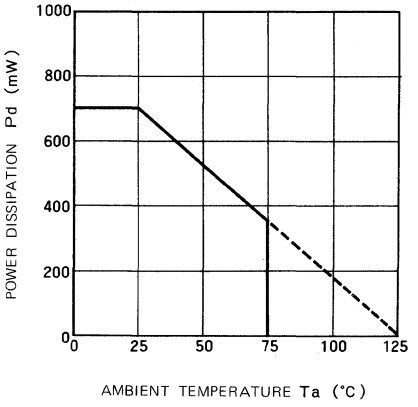
	Signal content
I	200mVp-p, 100kHz sine wave
II	3.0Vp-p, 100kHz sine wave
III	200mVp-p, 4.0MHz sine wave

APPLICATION EXAMPLE

TV Video Signal Processing Circuit



THERMAL DERATING (MAXIMUM RATING)



M51393AP

PAL VIDEO CHROMA SYSTEM

DESCRIPTION

The M51393AP is a semiconductor integrated circuit consisting of a PAL system color TV video chroma system, housed in a 30-pin molded DIL package.

Functions include video tone control, contrast control, and brightness control. The device includes a video output transistor, chroma signal processing and chroma demodulator circuits.

FEATURES

- Double differentiation is used for video tone control and high frequency component suppression control is continuous
- Pedestal clamp system with variable DC regeneration
- Linked contrast and color saturation control
- Peak limiting
- Built-in a video output transistor
- High sensitivity killer ..... –43dB level (typ)

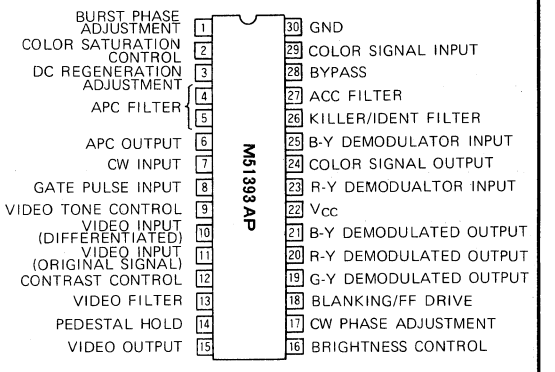
APPLICATION

PAL system color TV (video chroma circuits)

RECOMMENDED OPERATING CONDITIONS

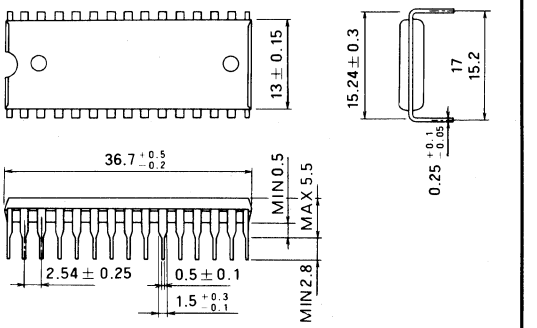
Supply voltage range ..... 11~13V
Rated supply voltage 12V

PIN CONFIGURATION (TOP VIEW)



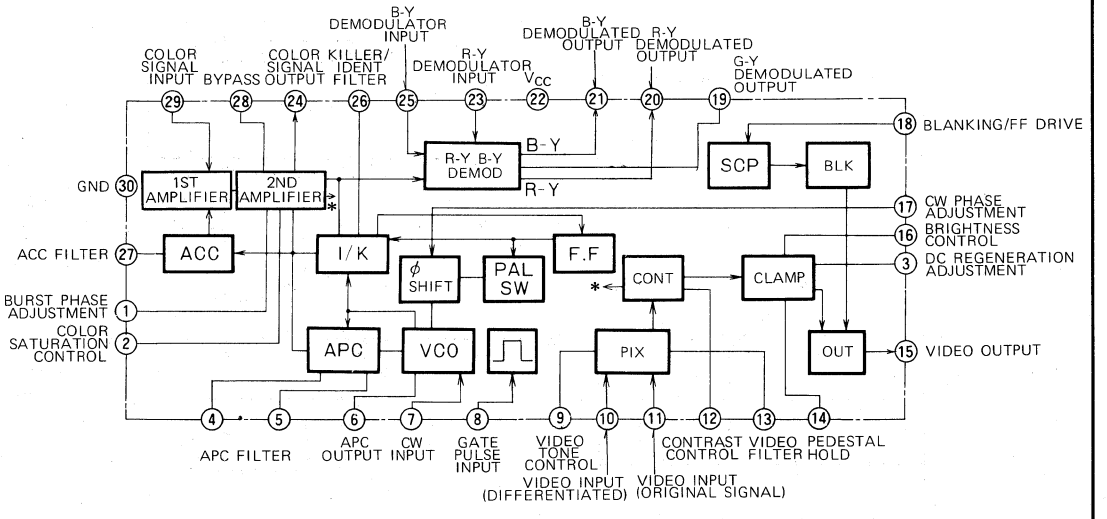
PACKAGE OUTLINE

Dimensions in mm



30-pin plastic molded DIL package

BLOCK DIAGRAM



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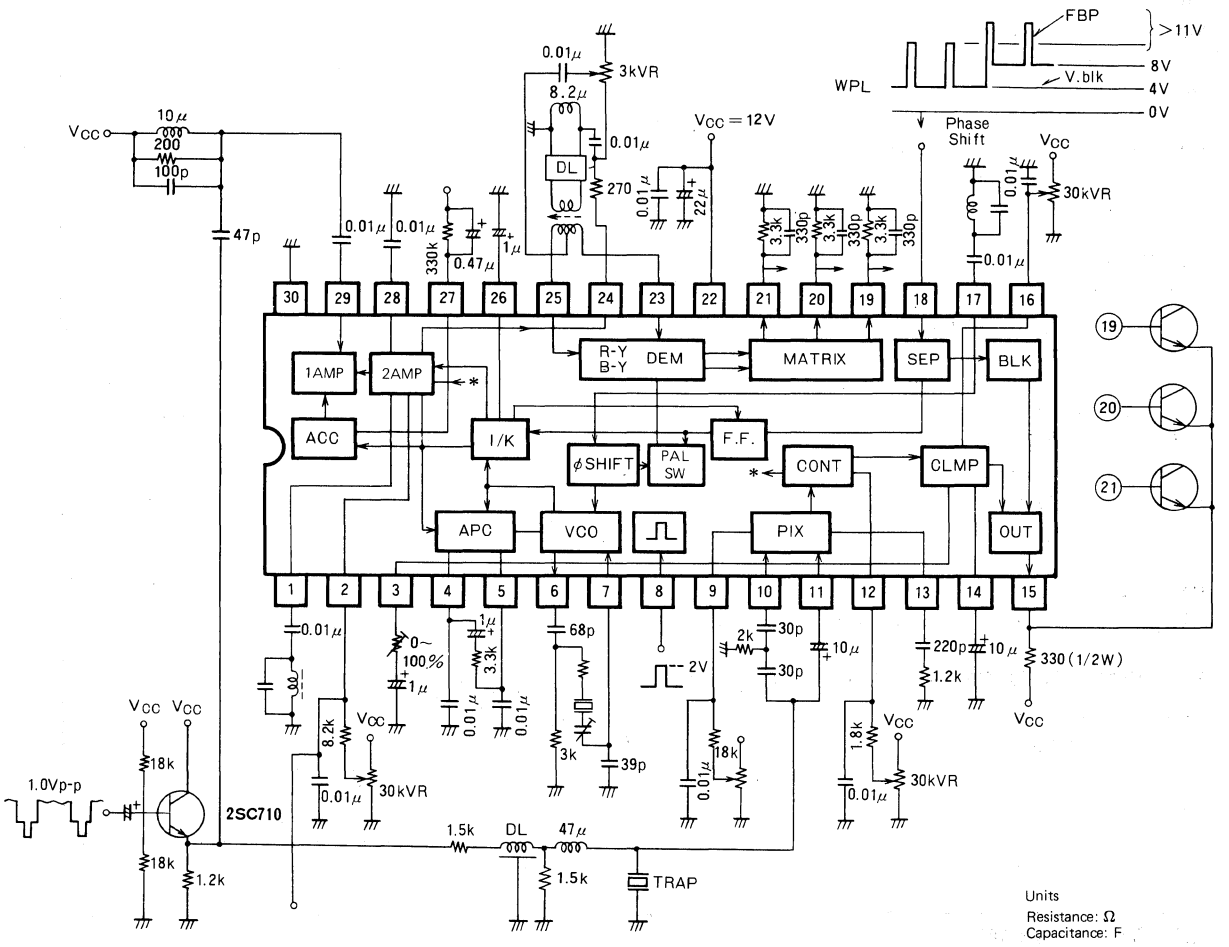
APPLICATION EXAMPLE



M51395AP

PAL VIDEO CHROMA SYSTEM

DESCRIPTION

The M51395AP is a semiconductor integrated circuit consisting of a system PAL video chroma system capable of handling PAL and SECAM dual systems, and housed in a 30-pin molded DIL package.

Its functions include video tone control, contrast control, brightness control, and the device includes video output transistor, a chroma signal processing circuit, and a chroma demodulator.

FEATURES

- The video tone control uses double differential and has continuous high frequency component suppression
- Pedestal clamp system with variable DC regeneration
- A contrast control voltage output is available for use with the M51397AP SECAM IC color saturation adjustment
- Peak-limiting is possible
- Built-in video output transistor
- High-sensitivity killer ..... −43dB level, typ

APPLICATION

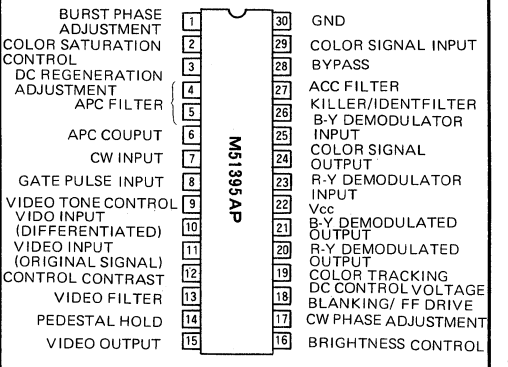
PAL and SECAM dual systems, PAL video chroma circuits

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... 11~13V

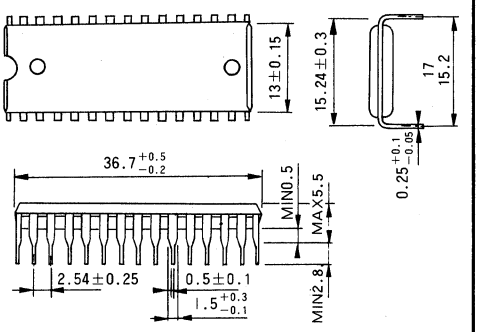
Rated supply voltage 12V

PIN CONFIGURATION (TOP VIEW)



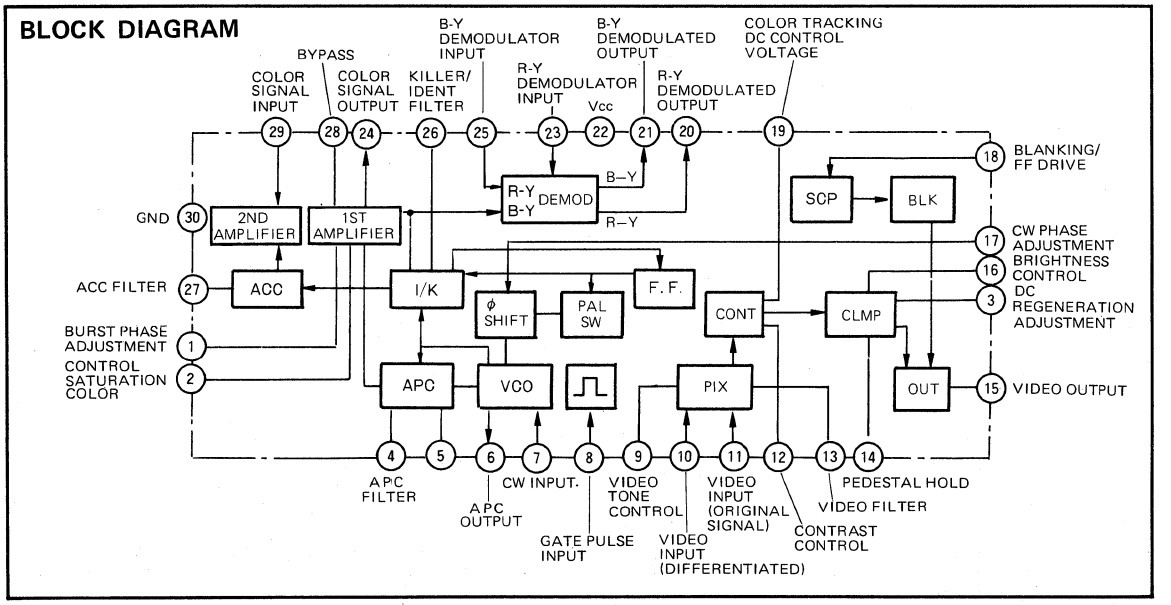
PACKAGE OUTLINE

Dimensions in mm



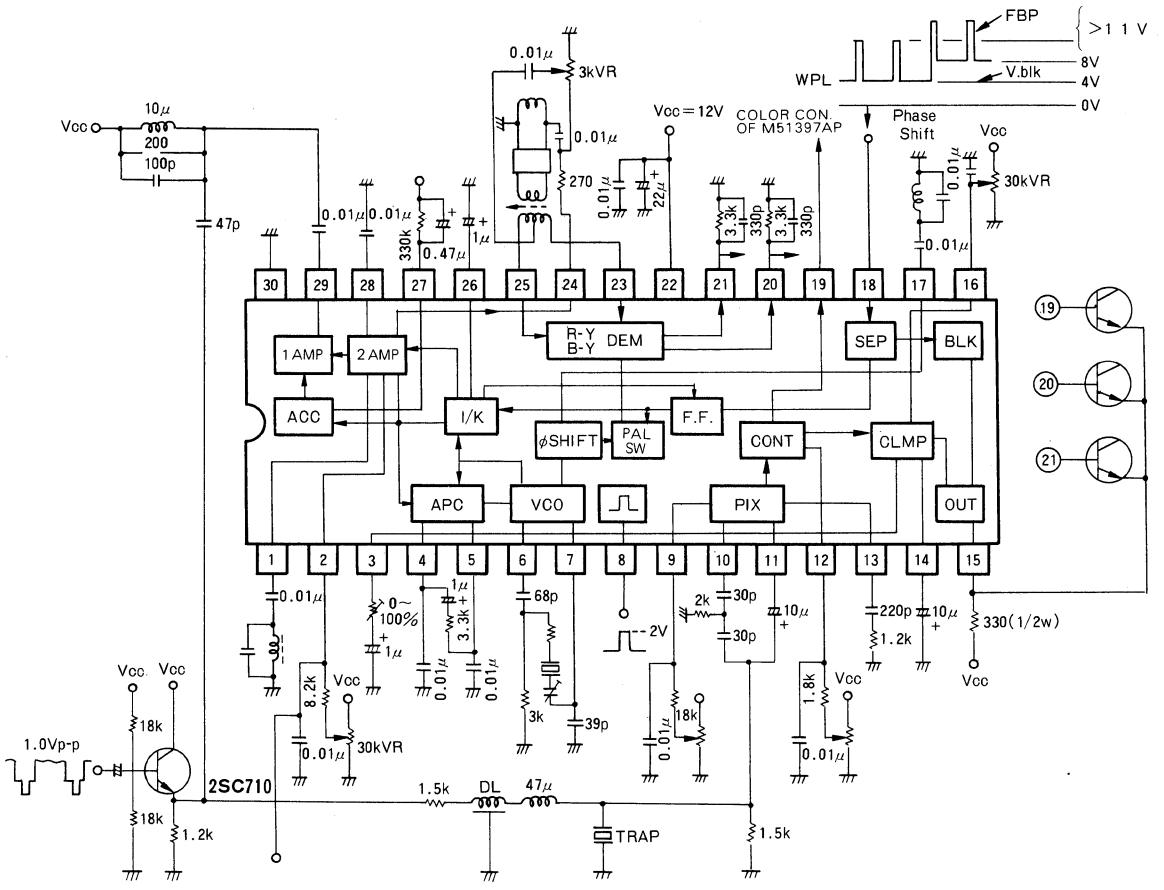
30-pin plastic molded DIL package

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

APPLICATION EXAMPLE



Units
Resistance: Ω
Capacitance: F

M51397AP

PAL VIDEO CHROMA SYSTEM

DESCRIPTION

The M51397AP is a semiconductor integrated circuit consisting of a limiter amplifier, SECAM switch, ident discriminator (ident B-Y and R-Y signals), color killer, color saturation control, matrix, system switch (PAL/SECAM) and DC regenerations circuit. It is intended for use in SECAM system color TV signal processing and demodulation including regeneration in one chip.

FEATURES

- Horizontal and vertical ident signals are possible
- Built-in ident error compensation
- High-gain limiter amplifier
- A system switch allows selection of either PAL or SECAM automatically
- Built-in DC regeneration circuit
- Low crosstalk

APPLICATION

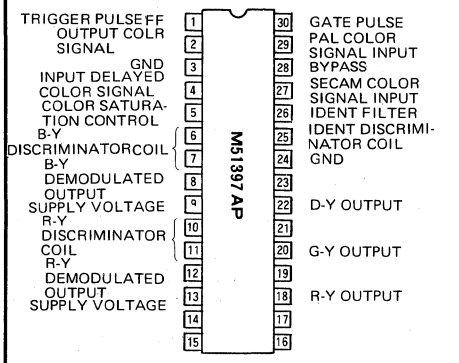
SECAM system color TV, color disgnal processors

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... 11～13V

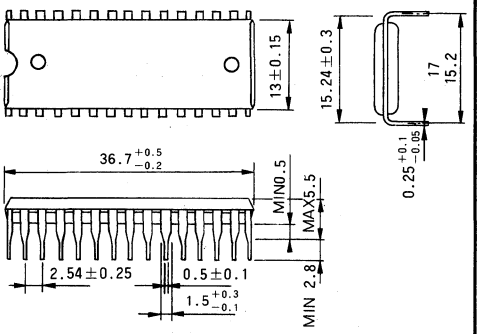
Rated supply voltage 12V

PIN CONFIGURATION (TOP VIEW)



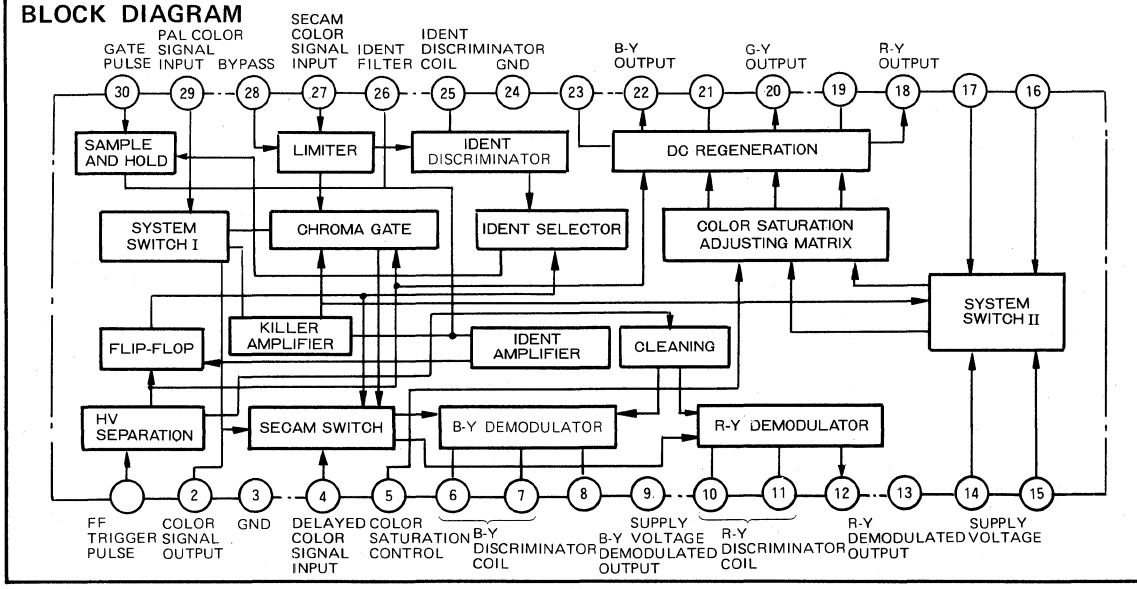
PACKAGE OUTLINE

Dimensions in mm



30-pin plastic molded DIL package

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

M51401P

VTR SERVO CONTROL CIRCUIT

DESCRIPTION

The M51401P is a semiconductor integrated circuit consisting of a VTR servo control circuit for use in home VTR equipment (1/2" and 3/4"). The circuit includes a reference pulse signal amplifier and delay circuit, pulse amplifiers to process the signals detected at the controlled circuits, the associated delay circuit, trapezoid waveform generator, sample and hold circuit and buffer amplifier.

FEATURES

- Wide dynamic range . . . . . 0.5~10V (typ)
- Low ripple . . . . . 80mV (max)
- Good linearity . . . . . 5% (max)
- Trapezoid waveform generator provides two slopes which can be selected
- Built-in time delay for the reference signal and detected pulse signals.

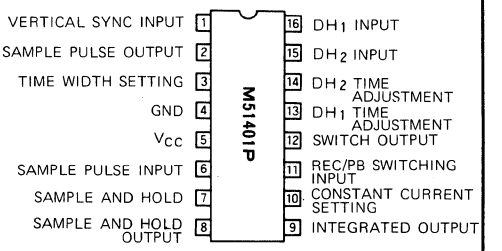
APPLICATIONS

VTR servocontrollers, general purpose DC servocontroller circuits

RECOMMENDED OPERATING CONDITIONS

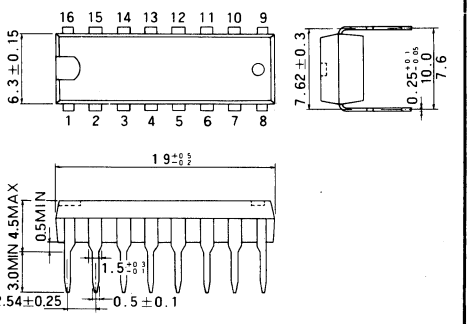
Supply voltage range . . . . . 8.5~13V
Rated supply voltage 12V

PIN CONFIGURATION (TOP VIEW)



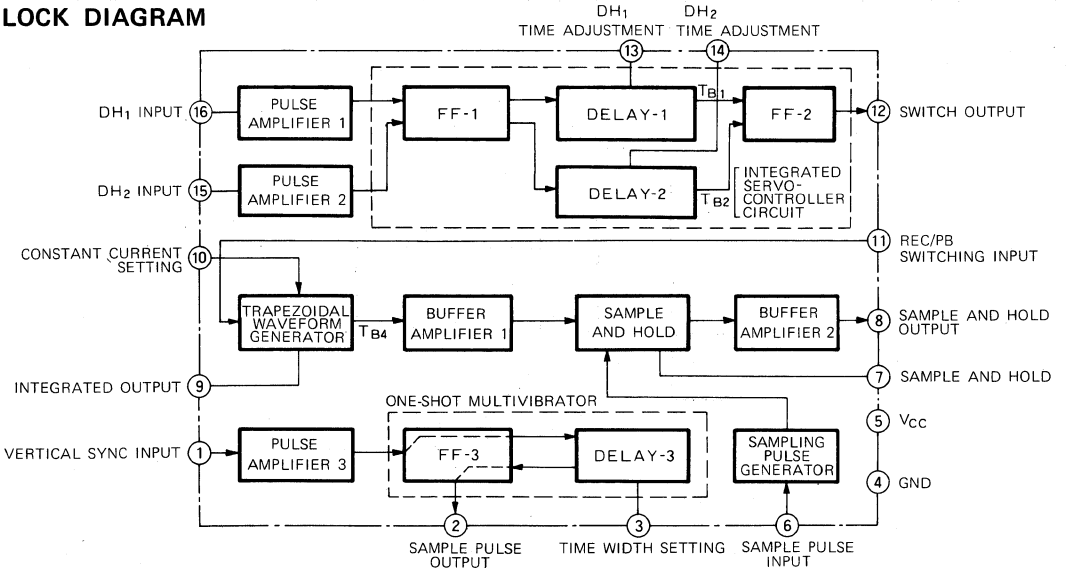
PACKAGE OUTLINE

Dimensions in mm



16-pin plastic DIL package

BLOCK DIAGRAM



VTR SERVO CONTROL CIRCUIT

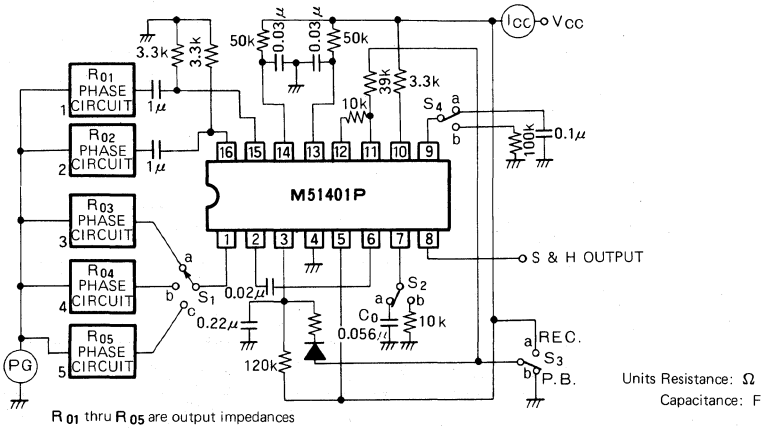
ABSOLUTE MAXIMUM RATINGS (T_a = 25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		15.6	V
I_{CC}	Circuit current		64	mA
P_d	Power dissipation		610	mW
V_{IN}	Input signal voltage (pins ⑮ and ⑯)		±3	V
T_{opr}	Operating temperature		−20 ~ + 70	℃
T_{stg}	Storage temperature		−40 ~ + 150	℃

ELECTRICAL CHARACTERISTICS (T_a = 25℃, V_{CC} = 12V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		8.5		13	V
I_{CC}	Circuit current		30	42	52	mA
ΔV_{16}	Input level	Phase circuit-1 R_{01} = 200Ω	40			mV_{O-P}
ΔV_{15}	Input level	Phase circuit-2 R_{02} = 200Ω	40			mV_{O-P}
ΔV_1	Input level	Phase circuit-3 R_{03} = 200Ω	200			mV_{O-P}
$T_{rape-LY}$	Trapezoid linearity				5	%
$\angle 9$(PB)	Trapezoid slope (PB)		3.55	4.15	5.15	V/ms
$\angle 9$(REC)	Trapezoid slope (REC)		1.72	1.85	1.97	V/ms
$V_{8(max)}$	S & H maximum output voltage				700	mV
$V_{8(min)}$	S & H minimum output voltage		9.5	10	11.5	V
$V_{8(rip)}$	S & H ripple voltage				80	mV
$\tau_{7(P)}$	Sampling pulse width		100	130	160	μs
T_{D-15}	Delay time		0.7	1.2	1.7	ms
T_{D-16}	Delay time		0.7	1.2	1.7	ms
T_{3-PB}	Pulse delay (PB)		21	25	29	ms
T_{3-REC}	Pulse delay (REC)		2.5	3.0	3.5	ms
$V_{8(TRS)}$	Output transient response	Refer to section on typical characteristics for details				

TEST CIRCUIT



R_{01} thru R_{05} are output impedances

Note 1. The phase circuits are used to adjust the pin ⑮ and pin ⑯ input signals and pin ⑥ sample pulse phase relationships to that shown in the section on typical characteristics.

TEST METHODS

Parameter	S_1	S_2	S_3	S_4	Measurement point	Method
I_{CC}	b	a	a	a		
ΔV_{16}				a	Pin ⑫	Monitor the rectangular waveform
ΔV_{15}				a	Pin ⑫	
ΔV_1		b		a	Pin ⑦	Monitor the sample pulse
Trape-LY	c		b	a	Pin ⑨	Use a meter with an input impedance of 10MΩ or above
∠9(PB)			b	a	Pin ⑨	
∠9(REC)	a		b	a	Pin ⑨	
$V_{8(max)}$	b		a	a	Pin ⑧	
$V_{8(min)}$	c		a	a	Pin ⑧	
$V_{8(rip)}$				a	Pin ⑧	
$\tau_{7(p)}$		b		a	Pin ⑦	
T_{D-16}				a	Pin ⑯, ⑫	
T_{D-15}				a	Pin ⑮, ⑫	
T_{3-PB}				a	Pin ①, ⑦	Phase comparison of the pulse leading edges
T_{3-REC}				a	Pin ①, ⑦	
$V_{8(TRS)}$	※	a		b	Pin ⑧	* S_1 as in output transient response curves Fig. 2

TYPICAL CHARACTERISTICS (Ta=25℃, unless otherwise noted)

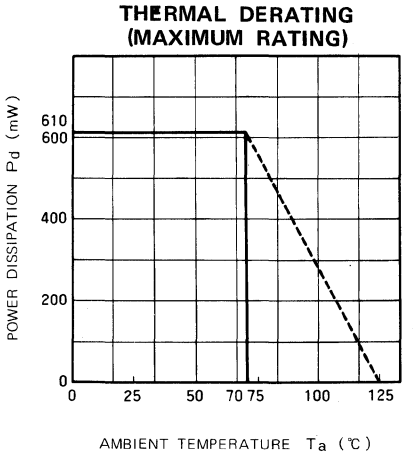
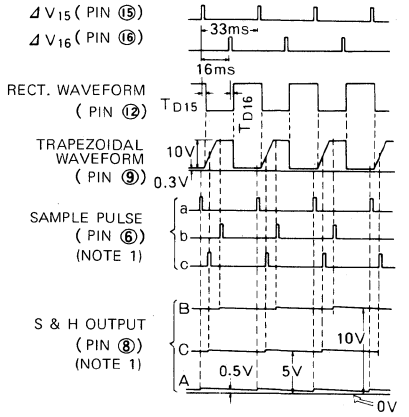
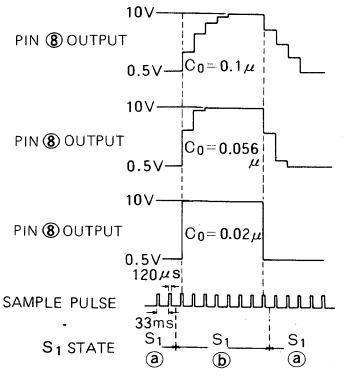


Fig. 1 Signal level and timing relationships



Note 1. The S & H output phases a, b, and c refer to the S & H A, B and C outputs.

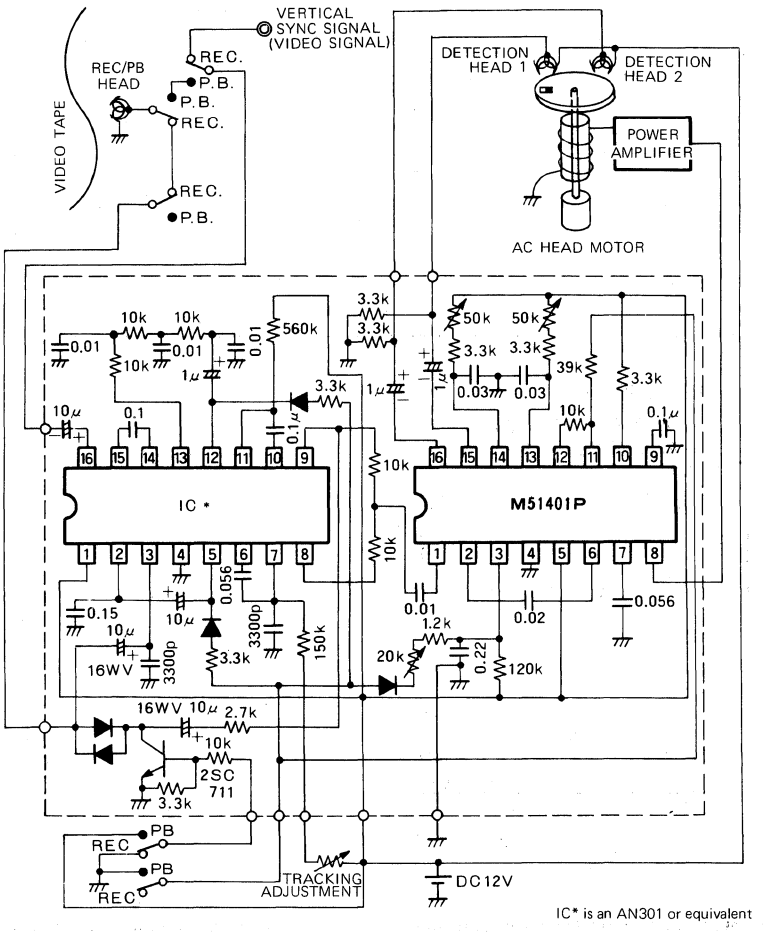
Fig. 2 Sample output transient response



Units Resistance: Ω
Capacitance: F

APPLICATION EXAMPLE

Home VTR Servocontroller Circuit



IC* is an AN301 or equivalent

Units Resistance: Ω
Capacitance: F
Diode: MD234

MITSUBISHI ELECTRIC

M5143P

TV SOUND IF DEMODULATOR

DESCRIPTION

The M5143P is a semiconductor integrated circuit consisting of the sound circuits required for use in TV sets. It includes a sound IF amplifier, limiter, differential peak detector, electronic volume control, audio driver and regulated power supply.

FEATURES

- Electronic volume control allowing control with DC
- Single coil with differential peak detection
- Minimal number of external parts, high stability
- High limiting sensitivity ..... 200μV (typ)
- Excellent AMR ..... 50dB (typ)
- High audio drive output ..... 6mAp-p (max)

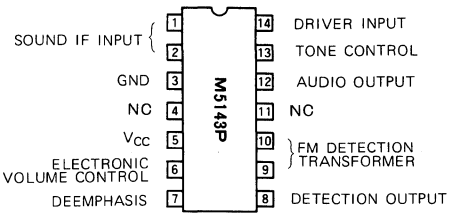
APPLICATION

TV sound IF demodulation

RECOMMENDED OPERATING CONDITIONS

Rated supply voltage ..... 18.0V (with R_s = 220Ω)

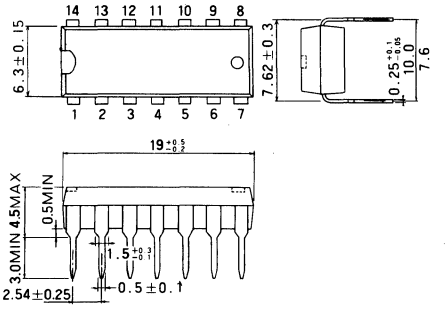
PIN CONFIGURATION (TOP VIEW)



NC : NO CONNECTION

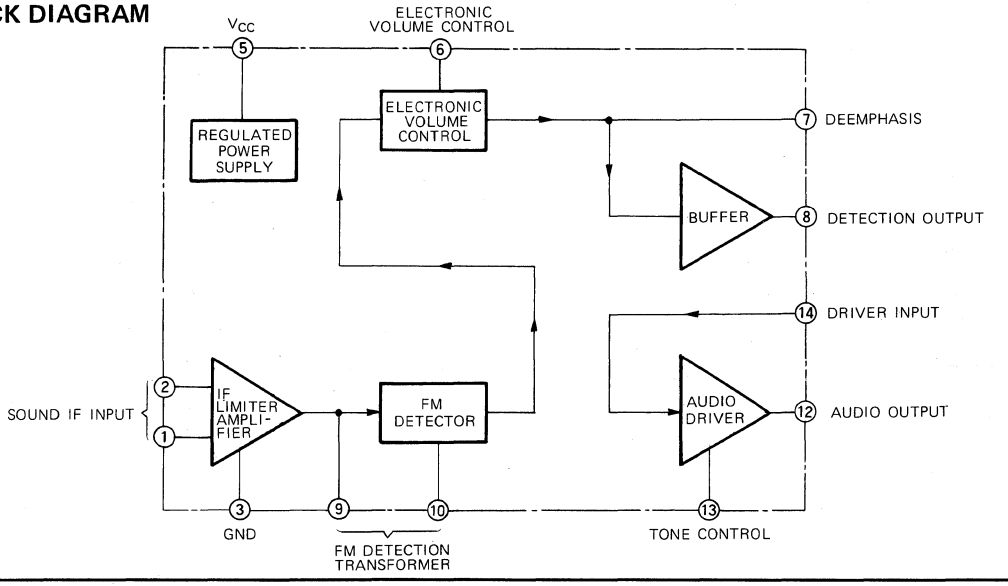
PACKAGE OUTLINE

Dimensions in mm



14-pin plastic DIL package

BLOCK DIAGRAM



TV SOUND IF DEMODULATOR

ABSOLUTE MAXIMUM RATINGS (Ta=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
I_{CC}	Circuit current*		50	mA
V_{in}	Input signal voltage (pins ①—②)		±3	V
P_d	Power dissipation		650	mW
K_θ	Thermal derating	Ta≧25°C	6.5	mW/°C
Topr	Operating temperature		−20～+70	°C
Tstg	Storage temperature		−40～+125	°C

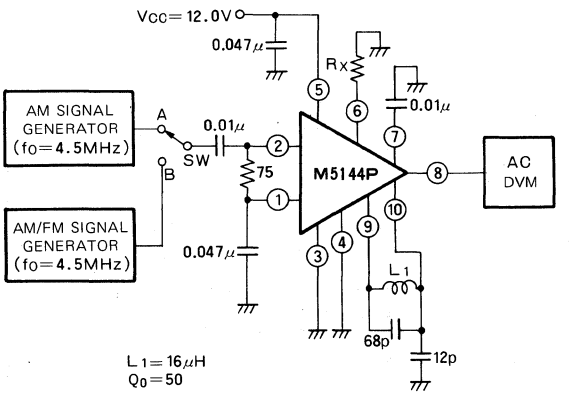
*Current capable of flowing into pin ⑤

ELECTRICAL CHARACTERISTICS (Ta=25°C, Vcc=12.0V,)

Symbol	Parameter	Test conditions	Test circuit	Limits			Unit
				Min	Typ	Max	
P_d	Power dissipation			264	316	360	mW
V_z	Zener voltage	I_{CC}=28mA		10.3	11.2	12.2	mA
$V_{i(lim)}$	Input limiting voltage	f_o=4.5MHz, R_X=0	(a)		46	52	dBμ
AMR	AM rejection ratio	f_{AM}=30%, f_d=25kHz, f_o=4.5MHz, R_X=0	(a)	40	50		dB
$V_{o(af)}$	Detection output voltage	f_d=25kHz, f_m=400Hz f_o=4.5MHz, V_{in}=100dBμ, R_X=0	(a)	500	750		mV
ATT(max)	Maximum electronic volume control attenuation	R_X=∞	(a)	60	80		dB
$G_{v(af)}$	Audio driver voltage gain	f=400Hz, V_{in}=0.1V	(b)	17.5	20		dB

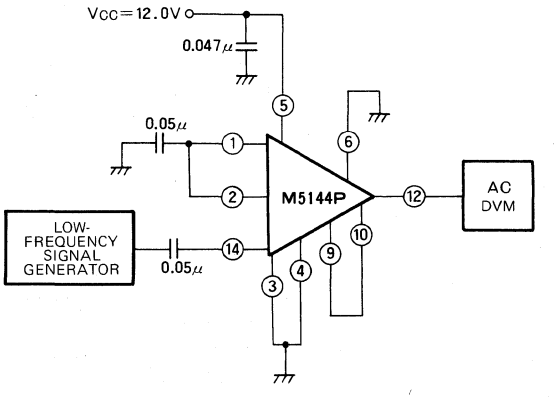
TEST CIRCUITS

(a) $V_{o(af)}$, $V_{i(lim)}$, AMR ATT(max)



Units Resistance: Ω
Capacitance: F

(b) $G_{v(af)}$

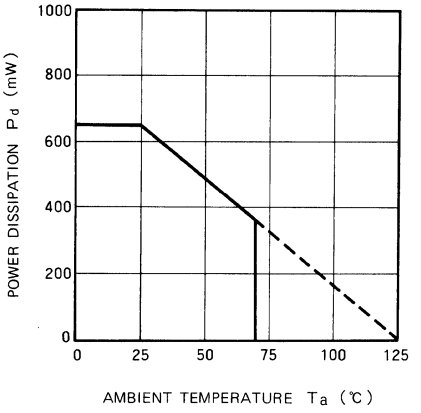


Units Resistance: Ω
Capacitance: F

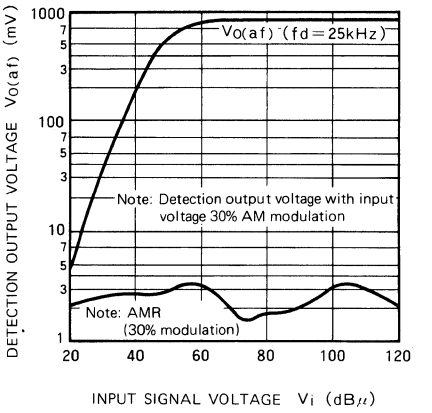
MITSUBISHI ELECTRIC

TYPICAL CHARACTERISTICS (Ta=25°C, unless otherwise noted)

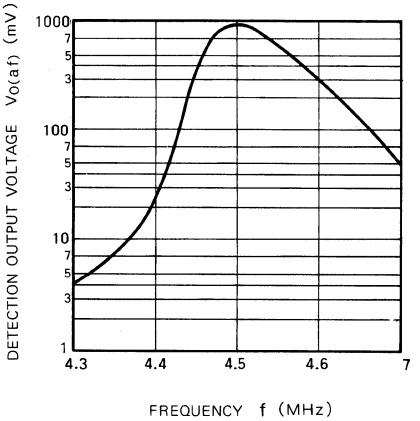
THERMAL DERATING (MAXIMUM RATINGS)



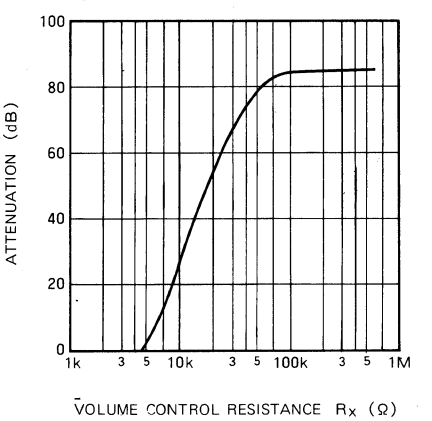
DETECTION OUTPUT LIMITING CHARACTERISTICS (fo=4.5MHz)



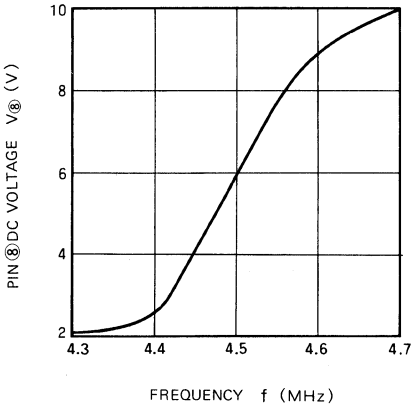
DETECTION OUTPUT VOLTAGE FREQUENCY RESPONSE



ELECTRONIC VOLUME CONTROL CHARACTERISTICS

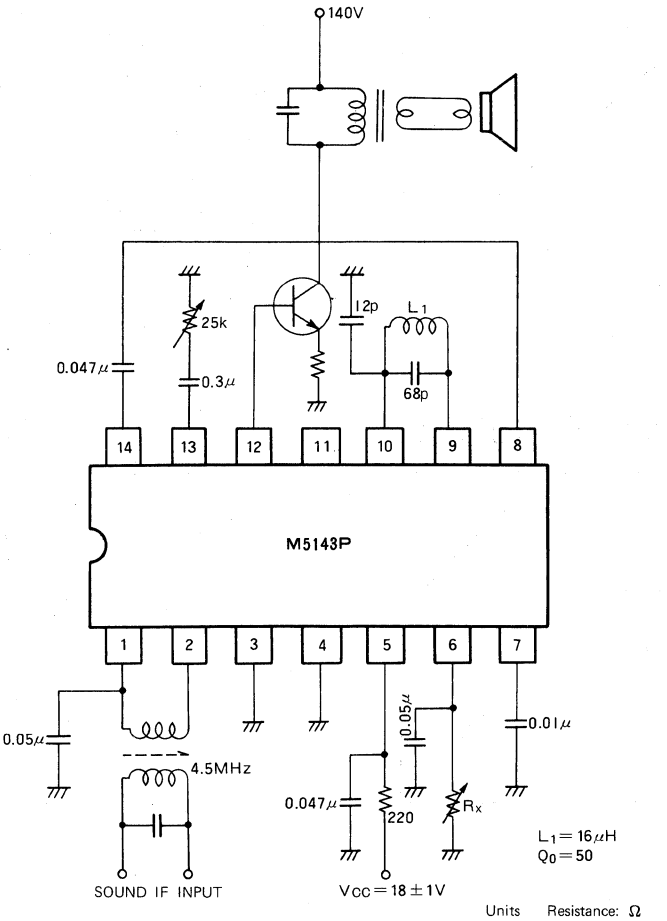


S-CURVE RESPONSE



APPLICATION EXAMPLE

TV sound circuit



Units Resistance: Ω
Capacitance: F

MITSUBISHI ELECTRIC

M5144P

TV SOUND IF DEMODULATOR

DESCRIPTION

The M5144P is a semiconductor integrated circuit consisting of in the sound circuits required for use in TV sets. It includes a sound IF amplifier, limiter, differential peak detector, electronic volume control and audio driver and, apart from the zener diode used in the regulated power supply, it is completely identical to the M5143P.

FEATURES

- Electronic volume control allowing DC control
- Single coil with differential peak detection
- Minimal number of external parts, high stability
- High limiting sensitivity ..... 200μV (typ)
- Excellent AMR ..... 50dB (typ)
- High sound drive output ..... 6mAp-p (max)

APPLICATION

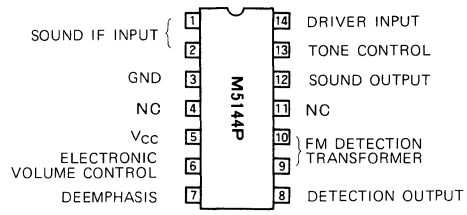
TV sound IF demodulation

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... 12 ±10%

Rated supply voltage 12V

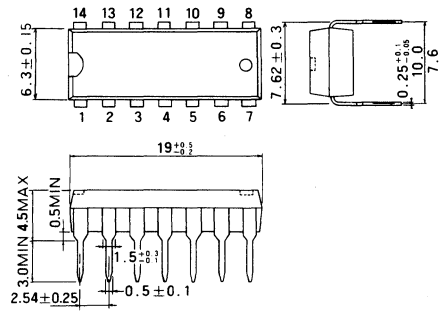
PIN CONFIGURATION (TOP VIEW)



NC : NO CONNECTION

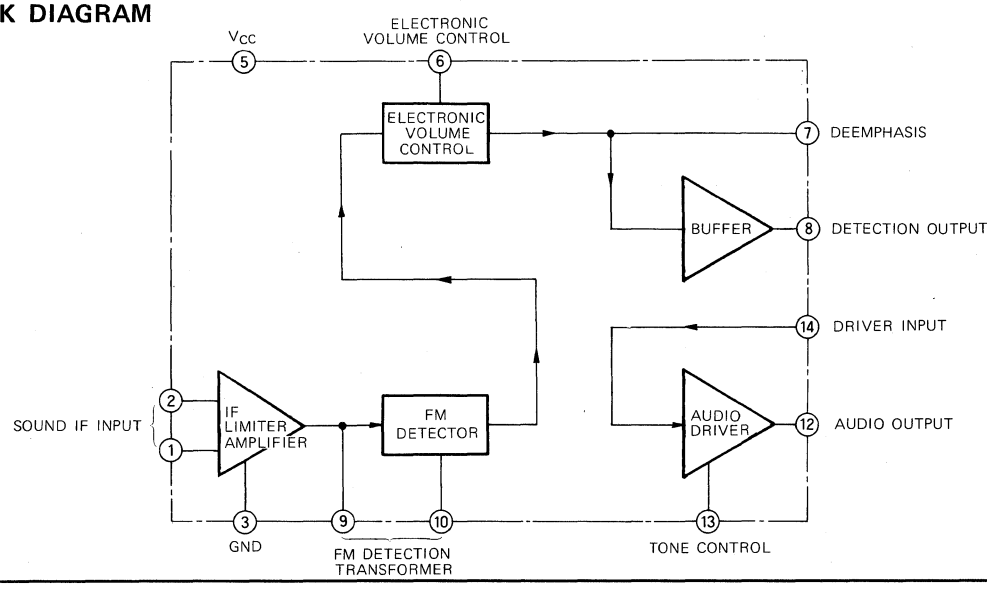
PACKAGE OUTLINE

Dimensions in mm



14-pin plastic DIL package

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta=25°C, unless otherwise noted)

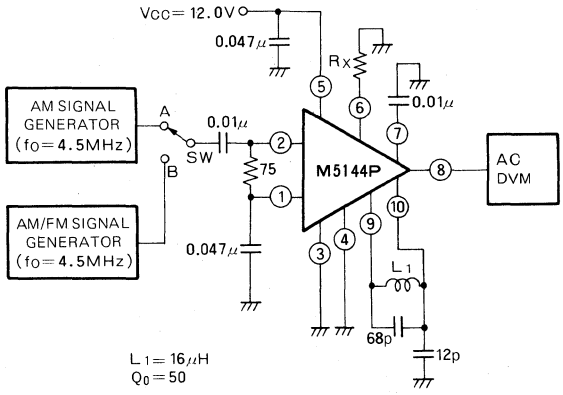
Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		18	V
V_{in}	Input singal voltage (pins ①−②)		±3	V
P_d	Power dissipation		650	mW
K_θ	Thermal derating	Ta≧25°C	6.5	mW/°C
Topr	Operating temperature		−20～+70	°C
Tstg	Storage temperature		−40～+125	°C

ELECTRICAL CHARACTERISTICS (Ta=25°C, Vcc=12.0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Test circuit	Limits			Unit
				Min	Typ	Max	
P_d	Power dissipation			264	316	360	mW
I_{CC}	Circuit current			18	22.5	27	mA
$V_{i(lim)}$	Input limiting voltage	f_0=4.5MHz, R_X=0	(a)		46	52	dBμ
AMR	AM rejection ratio	f_{AM}=30%, f_d=25kHz, f_0=4.5MHz, R_X=0	(a)	40	50		dB
$V_{o(af)}$	Detection output voltage	f_d=25kHz, f_m=400Hz f_0=4.5MHz, V_{in}=100dBμ, R_X=0	(a)	500	750		mV
ATT(max)	Maximum electronic volume attenuation	R_X=∞	(a)	60	80		dB
$G_{V(af)}$	Sound driver voltage gain	f=400Hz, V_{in}=0.1V	(b)	17.5	20		dB

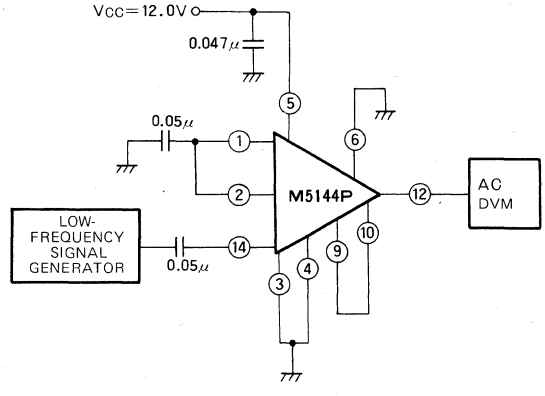
TEST CIRCUITS

(a) $V_{o(af)}$, $V_{i(lim)}$, AMR ATT(max)



Units Resistance: Ω
Capacitance: F

(b) $G_{V(af)}$

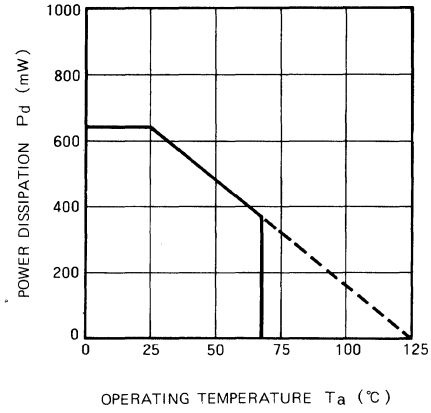


Units
Capacitance: F

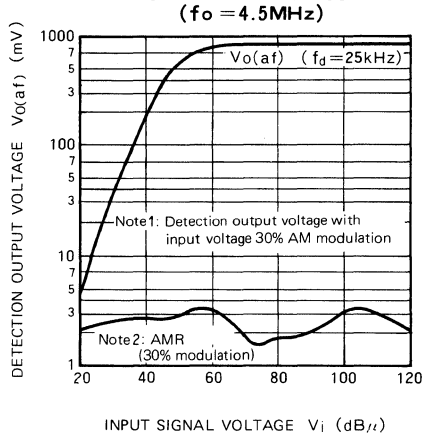
MITSUBISHI ELECTRIC

TYPICAL CHARACTERISTICS (Ta=25°C, unless otherwise noted)

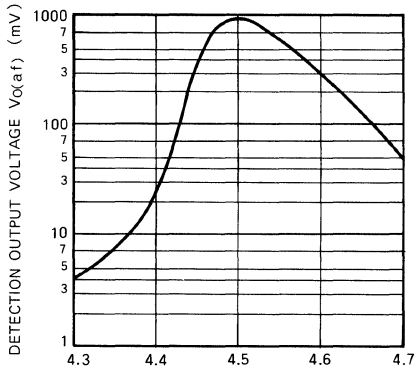
THERMAL DERATING (MAXIMUM RATING)



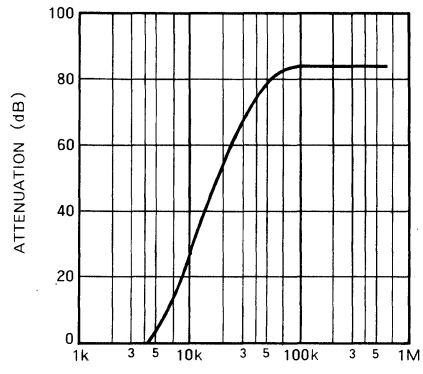
DETECTION OUTPUT LIMITING CHARACTERISTICS (fo=4.5MHz)



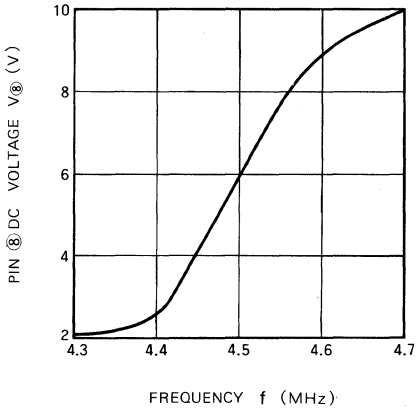
DETECTION OUTPUT VOLTAGE FREQUENCY RESPONSE



ELECTRONIC VOLUME CONTROL CHARACTERISTICS

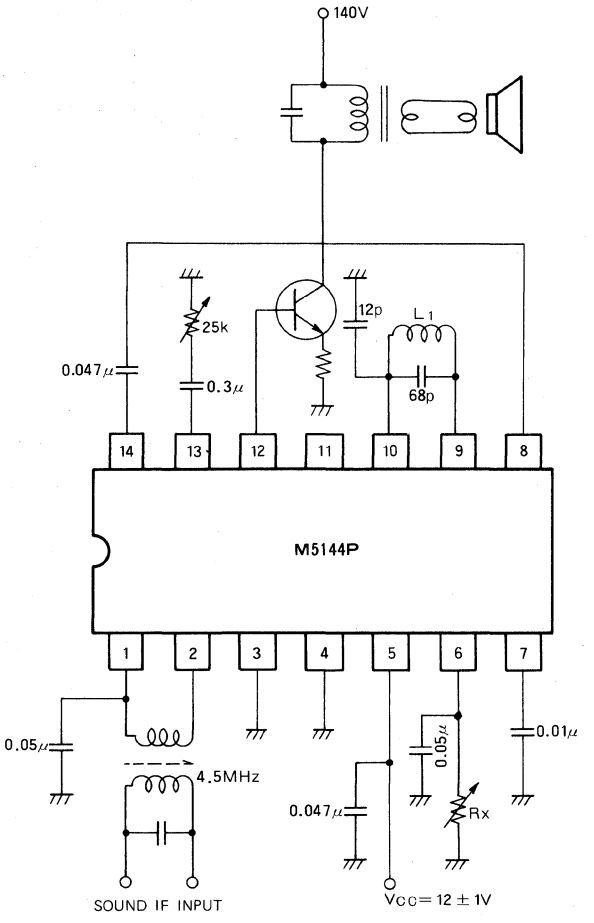


S-CURVE RESPONSE



APPLICATION EXAMPLE

TV sound circuit



Units Resistance: Ω
Capacitance: F

MITSUBISHI ELECTRIC

M5169P

TV VIDEO DETECTOR

DESCRIPTION

The M5169P is a semiconductor integrated circuit consisting of a video detection circuit for use in TV picture detection applications. The circuit consists of an AM detector circuit and a level shift circuit.

FEATURES

- Quasi-synchronous detection system
- Extraction of both positive and negative outputs
- Drive with low inputs (200mVp-p typ, with V_{in} = 5mVrms, AM 30% modulation)
- Excellent carrier suppression characteristics

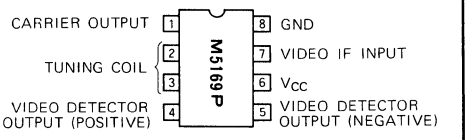
APPLICATIONS

TV video detection.

RECOMMENDED OPERATING CONDITIONS

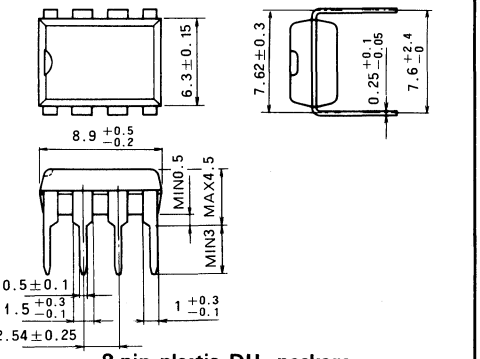
Supply voltage range ..... 12~24V
Rated supply voltage 20V

PIN CONFIGURATION (TOP VIEW)



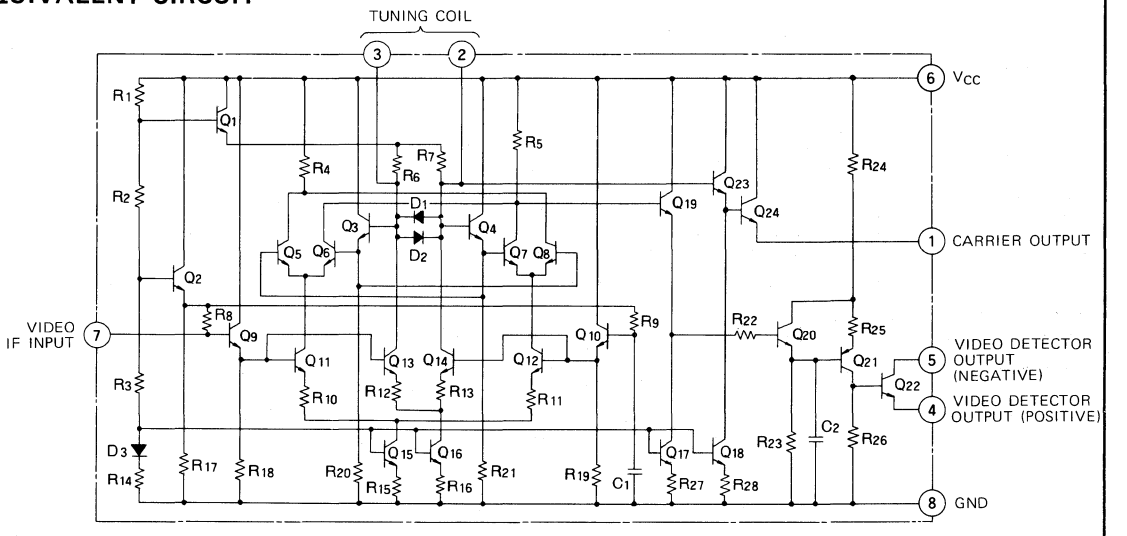
PACKAGE OUTLINE

Dimensions in mm



8-pin plastic DIL package

EQUIVALENT CIRCUIT



TV VIDEO DETECTOR

ABSOLUTE MAXIMUM RATINGS (Ta=25°C, unless otherwise noted)

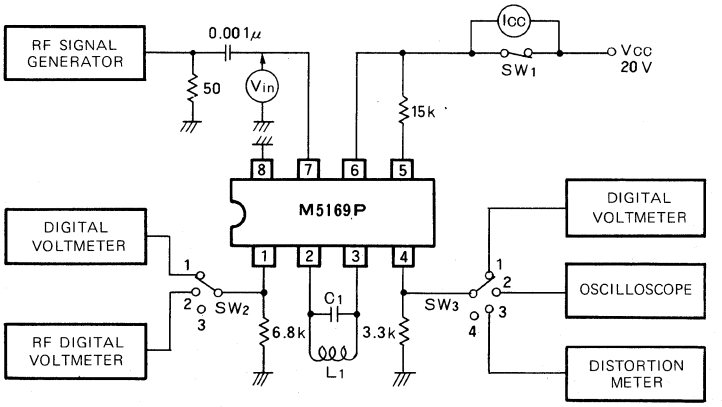
Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		24	V
Vin	Signal input voltage		1.0	Vrms
I_{CC}	Circuit current		26	mA
Pd	Power dissipation		625	mW
K_θ	Derating	Ta≧25°C	6.25	mW/°C
Topr	Operating temperature		−20～+75	°C
Tstg	Storage tmperature		−40～+125	°C

ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{CC}=20.0V)

Symbol	Parameter	Test conditions	Test circuit	Limits			Unit
				Min	Typ	Max	
I_{CC}	Circuit current		(a)		15	20	mA
$V_④$	Pin ④ quiescent DC voltage		(a)	7.5	8.3	9.0	V
$V_④$min	Minimum video detection output voltage	f=58.75MHz unmodulated, Vin varied	(a)		0	0.5	V
Vin	Input signal voltage	fo=58.75MHz, fm=1kHz AM=30%, $V_{O④}$=200mV$_{P-P}$	(a)	2.5	5.0	10.0	mVrms
$V_{O\,(AFT)}$	AFT output voltage	f=58.75MHz unmodulated	(a)	130	150		mVrms
$V_①$	AFT output DC voltage		(a)	7.0	8.2	9.5	V
$THD_{(DET)}$	Total harmonic detection of detector output	fo=58.76MHz, fm=1kHz AM=80%, $V_{O④}$=1.5V$_{P-P}$	(a)		4	9	%
Vlim	Diode limiting characteristics	I_D=200μA	(b)	0.30	0.48	0.55	V

TEST CIRCUITS

(a)



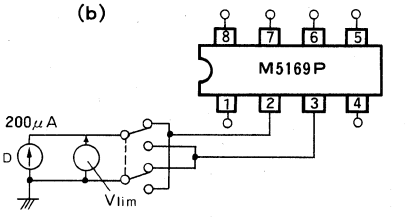
Units Resistance: Ω
Capacitance: F

TEST METHODS

($SW_{1,2,3}$ setting conditions)

Symbol	SW_1	SW_2	SW_3
I_{CC}	OFF	3	4
$V_④$	ON	3	1
$V_④$min	ON	3	1
Vin	ON	2	2
$V_{O\,(AFT)}$	ON	2	2
$V_①$	ON	1	4
$THD_{(DET)}$	ON	3	2 & 3

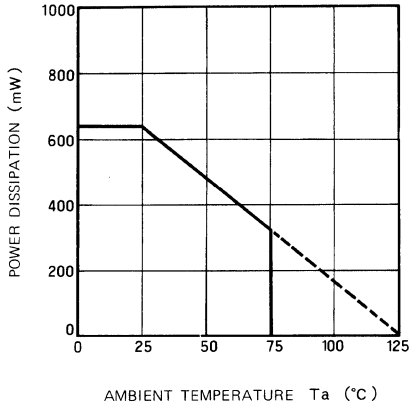
(b)



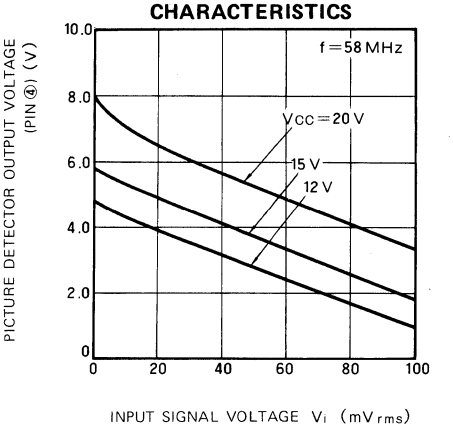
MITSUBISHI ELECTRIC

TYPICAL CHARACTERISTICS (Ta=25°C, unless otherwise noted)

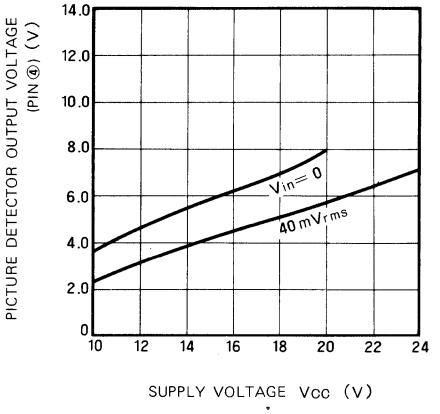
THERMAL DERATING (MAXIMUM RATING)



PICTURE DETECTOR OUTPUT VOLTAGE VS INPUT SIGNAL VOLTAGE CHARACTERISTICS

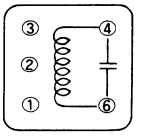


PICTURE DETECTOR OUTPUT VOLTAGE VS SUPPLY VOLTAGE CHARACTERISTICS



TUNING COIL L_1, C_1 SPECIFICATIONS

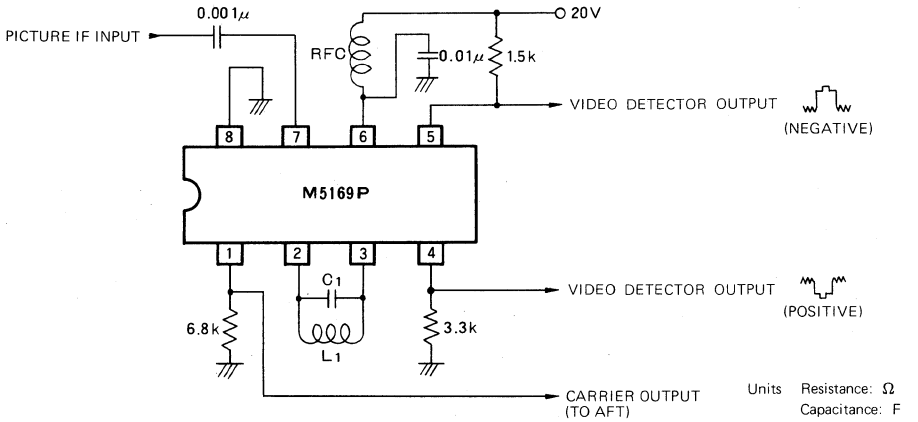
Type : made by Toko Inc., equivalent to 10k bobbin with shield
Number of turns : 5 (pins ④−⑥)
Wire material : 0.12φ, 0 VEW
Q_0 = 90 ± 20%
Internal capacitance = 33 pF



(BOTTOM VIEW)

APPLICATION EXAMPLE

TV video detector circuit



M5183P

TV VIDEO IF AMPLIFIER

DESCRIPTION

The M5183P is a semiconductor integrated circuit designed for use as a TV video IF amplifier circuit and it includes a two-stage IF amplifier circuit, a keyed AGC circuit and an AGC amplifier circuit.

FEATURES

- High power gain ..... 48dB typ (f=58MHz)
- Excellent and wide-range AGC response ..... 68dB (typ)
- Minimum output variations caused by 60dB IF input variations
- Minimum changes in input/output admittance across entire AGC spectrum
- Both positive and negative high-gain keyed AGC system

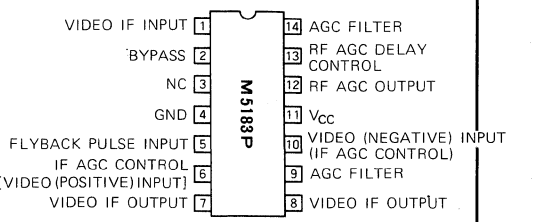
APPLICATION

TV video IF amplification

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... 10~18V
Rated supply voltage 12V

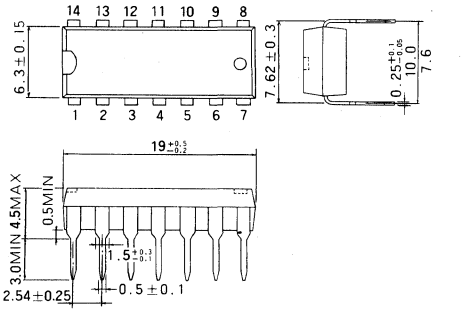
PIN CONFIGURATION (TOP VIEW)



NC: NO CONNECTION

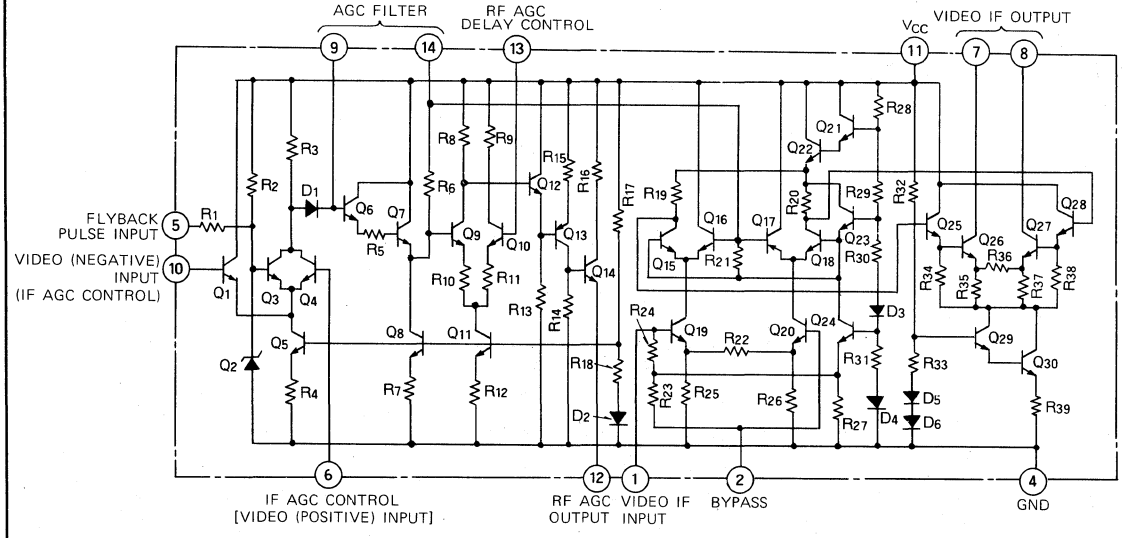
PACKAGE OUTLINE

Dimensions in mm



14-pin plastic DIL package

EQUIVALENT CIRCUIT



MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C, unless otherwise noted)

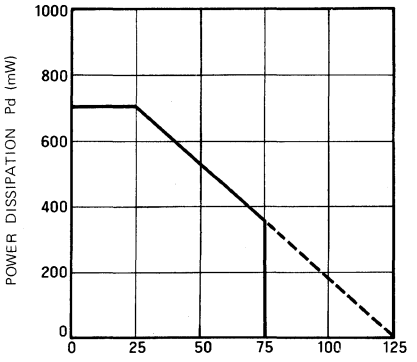
Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage (pin ⑪)		18	V
$V_⑦$, $V_⑧$	Output stage breakdown voltage (pins ⑦, ⑧)		18	V
$V_{①-②}$	Input voltage (pins ① ~ ②)		10	V_{P-P}
$V_{⑥-⑩}$	AGC voltage (pins ⑥ ~ ⑩)		6	V
$V_⑤$	Gating voltage (pin ⑤)		10, −20	V
Pd	Power dissipation		700	mW
K_θ	Derating	Ta≧25°C	7	mW/°C
Topr	Operating temperature		−20 ~ +75	°C
Tstg	Storage temperature		−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS (T_a = 25°C, V_{CC} = 12.0V)

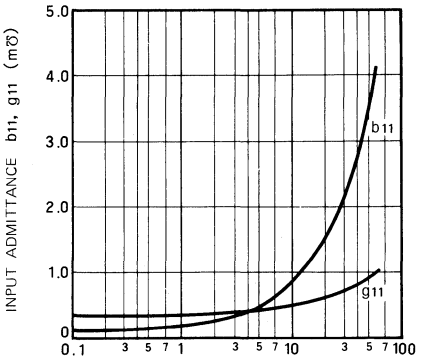
Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
Pd	Power dissipation				325	370	mW
I_O	Output current		$I_⑦ + I_⑧$		5.7		mA
I_{CC}	Circuit current		$I_⑦ + I_⑧ + I_⑪$		27	31	mA
AGC	AGC range				68		dB
G_P	Power gain		f=58MHz	44	48		dB
NF	Noise figure		f=60MHz, Rg=50Ω		8.5		dB
$V_⑫$	RF AGC voltage range	Max		6.5	7.0		V_{DC}
		Min		0	0.2	0.6	
V_O	Maximum voltage swing for differential output	0 dB AGC	Across pins ⑦ ~ ⑧		16.8		V_{P-P}
		−30dB AGC			8.4		
	Output variations		IF signal variation: 60dB		0.3		dB
	IF gain variation		Variation across total RF AGC range		10		dB

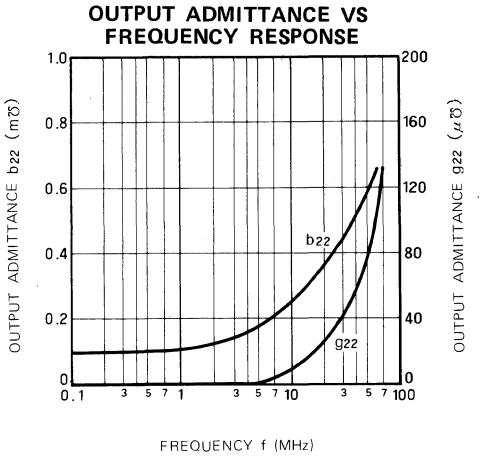
TYPICAL CHARACTERISTICS

THERMAL DERATING (MAXIMUM RATING)



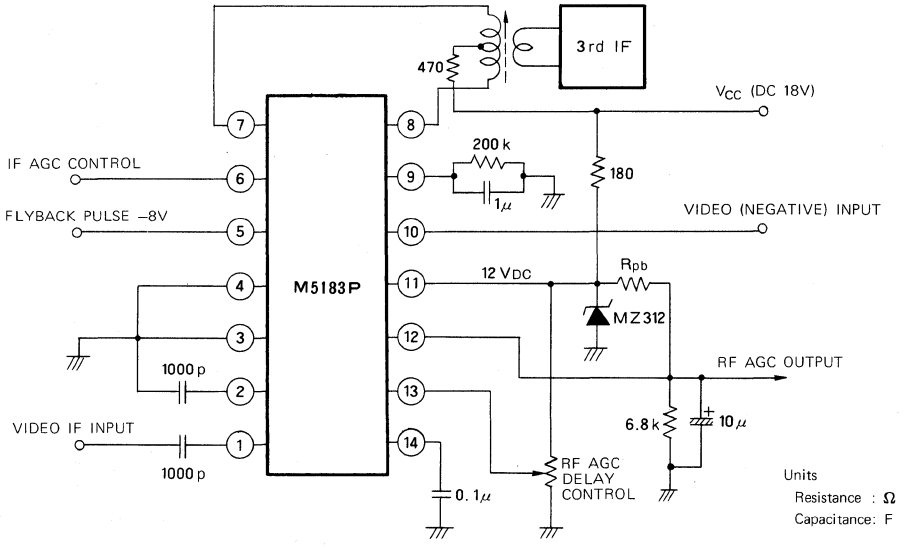
INPUT ADMITTANCE VS FREQUENCY RESPONSE





APPLICATION EXAMPLE

TV video IF amplifier circuit



MITSUBISHI ELECTRIC

M5185P

TV VIDEO IF SIGNAL PROCESSOR

DESCRIPTION

The M5185P is a semiconductor integrated circuit consisting of a video IF amplifier, video detector circuit, video amplifier circuit, sound IF detector circuit, AFT circuit, AFT switching circuit, AGC noise eliminator circuit, peak-type IF AGC circuit, and RF AGC circuit. It is designed for use in TV video IF signal processing.

FEATURES

- The sound IF detector and video detector circuit are separated
- The video detector circuit uses synchronous detection, and the sound IF detector circuit uses a transistor detecting method
- Fixed or variable IF AGC level is possible
- Positive/negative RF AGC output

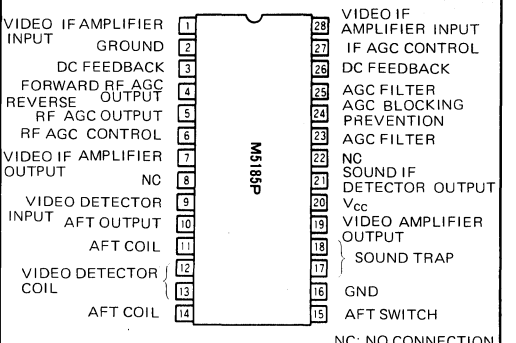
APPLICATION

TV video IF signal processing circuits

RECOMMENDED OPERATING CONDITIONS

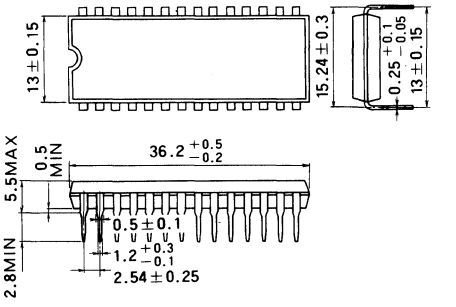
Supply voltage range ..... 11～13V
Rated supply voltage 12.0V

PIN CONFIGURATION (TOP VIEW)



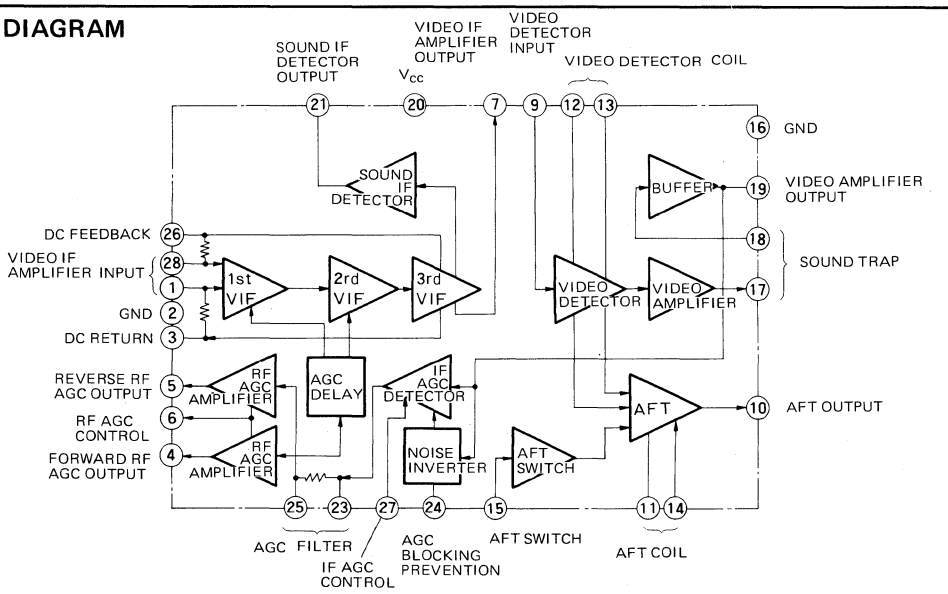
PACKAGE OUTLINE

Dimensions in mm



28-pin plastic DIL package

BLOCK DIAGRAM



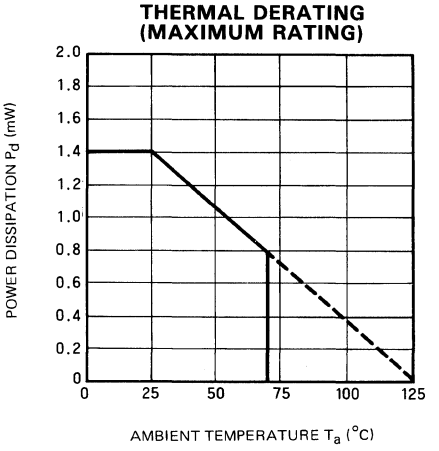
ABSOLUTE MAXIMUM RATINGS (Ta=25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		14.4	V
Pd	Power dissipation		1.4	W
K_θ	Derating	Ta≧25℃	14	mW/℃
Topr	Operating temperature		−20～+70	℃
Tstg	Storage temperature		−40～+125	℃

ELECTRICAL CHARACTERISTICS (Ta=25℃, V_{CC}=12V, unless otherwise noted)

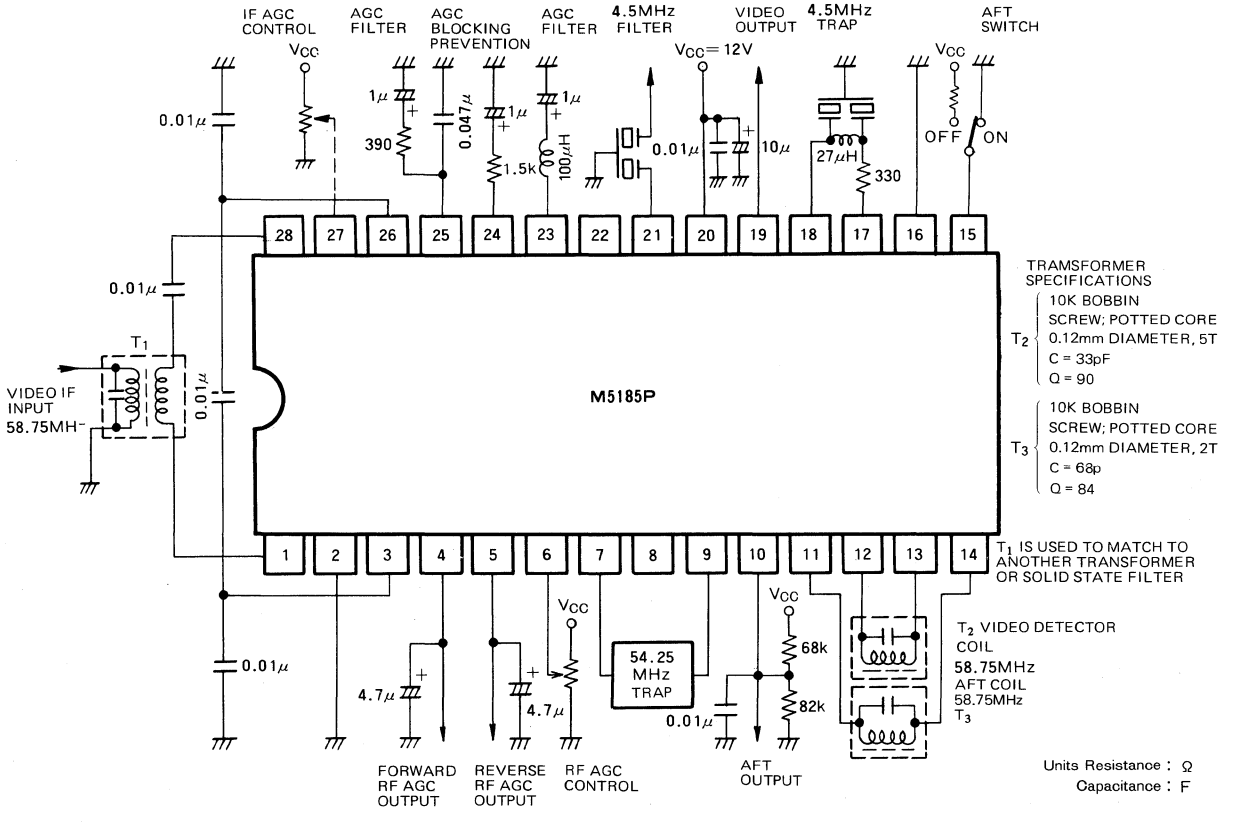
Symbol	Parameter	Test conditions		Limits			Unit
		f (MHz)		Min	Typ	Max	
I_{CCO}	Quiescent circuit current			35	50	66	mA
G_V	Video IF voltage gain	58.75	Vi=1mVrms	38	41	44	dB
G_R	Video IF AGC control range	58.75	Vi=100mVrms	49	52		dB
Rin(VIF)	Video IF input resistance	58.75			1.1		kΩ
Cin(VIF)	Video IF input capacitance	58.75			2.9		pF
Ro	Video IF output resistance	58.75			280		Ω
G_C	Video detector conversion gain	58.75	Vi=120mV$_{P-P}$, f_m=400Hz, 74%AM	27	30	33	dB
Vo max	Maximum video output	58.75	f_m=400Hz, 74%AM	3.6	4.0		V_{P-P}
DG	Video detector differentiation gain	58.75	f_m=3.58MHz, step waveform	0	5	10	%
DP	Video detector differentiation phase	58.75	f_m=3.58MHz, step waveform	0	3	7	%
$V_{⑰}$	Video amplifier output DC voltage		Zero signal condition	4.8	5.8	6.8	V
BW	Video amplifier band width	58.75	Vi=20mVrms, f_m= sweep, 40%AM	6	11		MHz
Rin(VD)	Video detector input resistance	58.75			6.2		kΩ
Cin(VD)	Video detector input capacitance	58.75			3.3		pF
μ	AFT detector sensitivity	58.75	Sweep signal, $V_{⑩}$=5.3～7.5V	44	58	72	mV/kHz
$V_{⑩}$	AFT output DC voltage		Zero signal condition	4.9	5.7	7.0	V
$V_{AFT(ON)}$	AFT switch on voltage	58.75	Sweep signal, $V_{⑮}$ varied	0	1.2	1.3	V
$V_{AFT(OFF)}$	AFT switch off voltage	58.75	Sweep signal, $V_{⑮}$ varied	1.3	1.5	1.6	V
V_{RRH}	RF AGC maximum voltage			9.5	10.8	11.5	V
V_{RRL}	RF AGC minimum voltage			0	0.2	0.5	V
S/N	Overall signal to noise ratio	58.75	Vi=80dBμ		56		dB
R_{AGC}	Overall AGC range	58.75	Vi varied		56		dB
$V_{O(SIF)}$	Sound IF detector output signal voltage	58.75	80dBμ, f_S=54.25MHz, 60dBμ	89	93	97	dBμ

TYPICAL CHARACTERISTICS

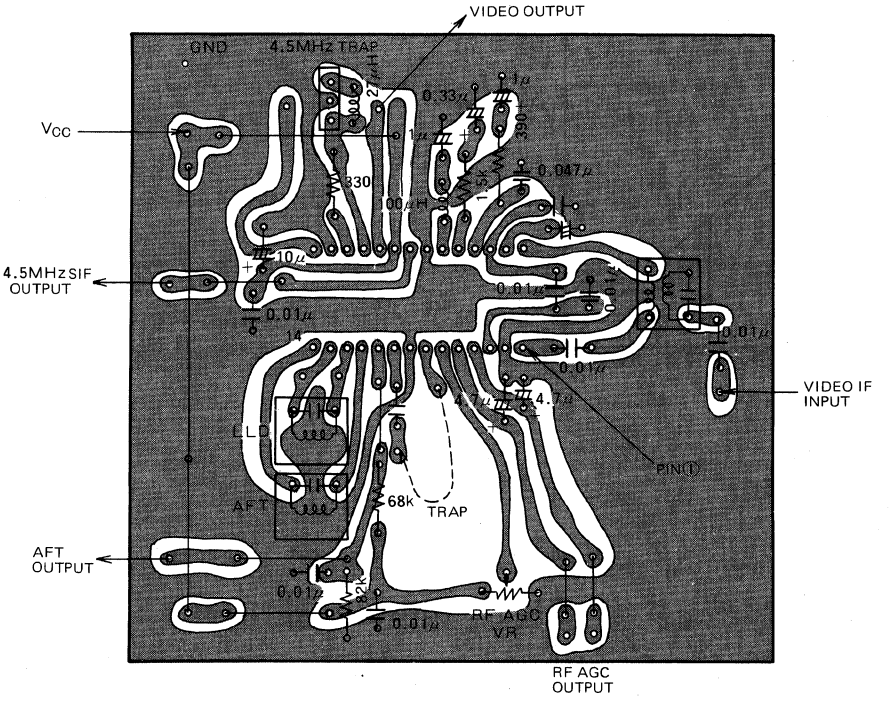


APPLICATION EXAMPLE

TV Video IF signal processing circuit



PRINTED CIRCUIT BOARD LAYOUT (copper clad side, full size)



MITSUBISHI ELECTRIC

M5186P/AP

TV VIDEO IF SIGNAL PROCESSOR

DESCRIPTION

The M5186P/AP is a semiconductor integrated circuit designed to serve as a TV video IF signal processing circuit. The circuit consists of a video IF amplifier, video detector, video amplifier, audio IF detector, AFT circuit, AFT switching circuit, IF AGC circuit (peak-type) and RF AGC circuits. These circuits are housed in a 22-pin plastic DIL package.

FEATURES

- Audio IF detector circuits and video detector circuits are separated
- Forward, reverse and RF AGC outputs are availables.
- Synchronous video and audio detection system
- Quadrature detection type AFT circuit
- Excellent AGC characteristics with broad control range
- Peak-type AGC circuit

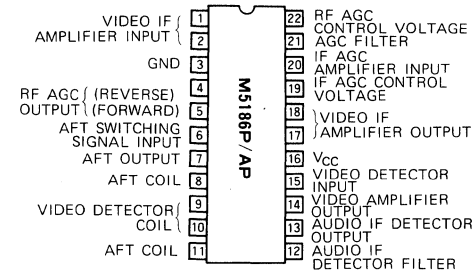
APPLICATION

TV video IF signal processing

RECOMMENDED OPERATING CONDITIONS

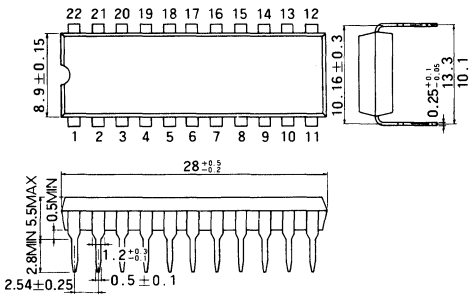
Supply voltage ..... 11~13V
Rated supply voltage 12.0V

PIN CONFIGURATION (TOP VIEW)



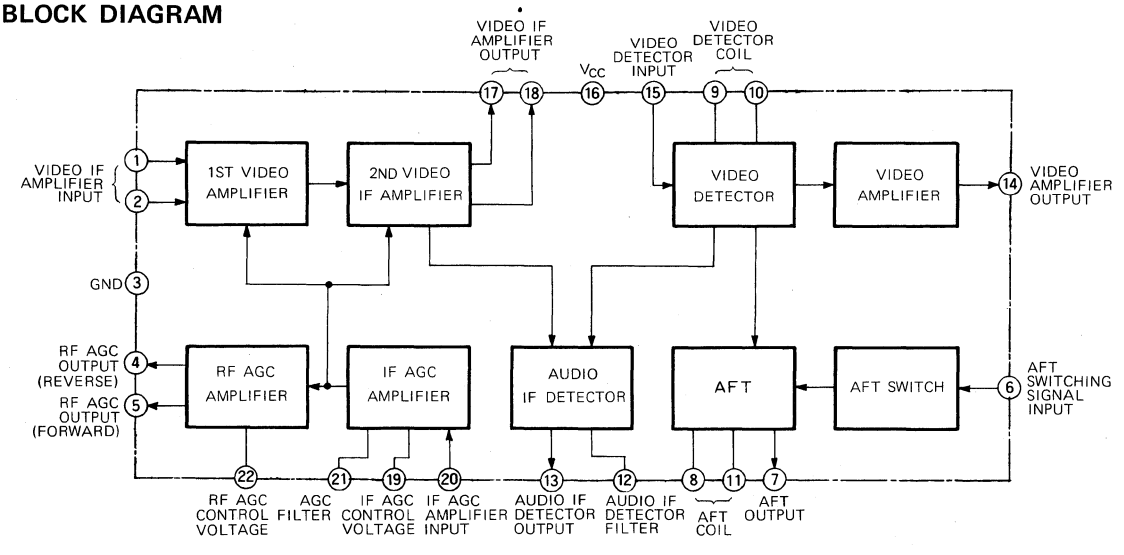
PACKAGE OUTLINE

Dimensions in mm



22-pin plastic DIL package

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta=25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		16.0	V
Pd	Power dissipation		1.4	W
K_θ	Derating	Ta≧25℃	14	mW/℃
Topr	Operating temperature		−20～+75	℃
Tstg	Storage temperature		−40～+125	℃

ELECTRICAL CHARACTERISTICS (Ta=25℃, V_{CC}=12.0V)

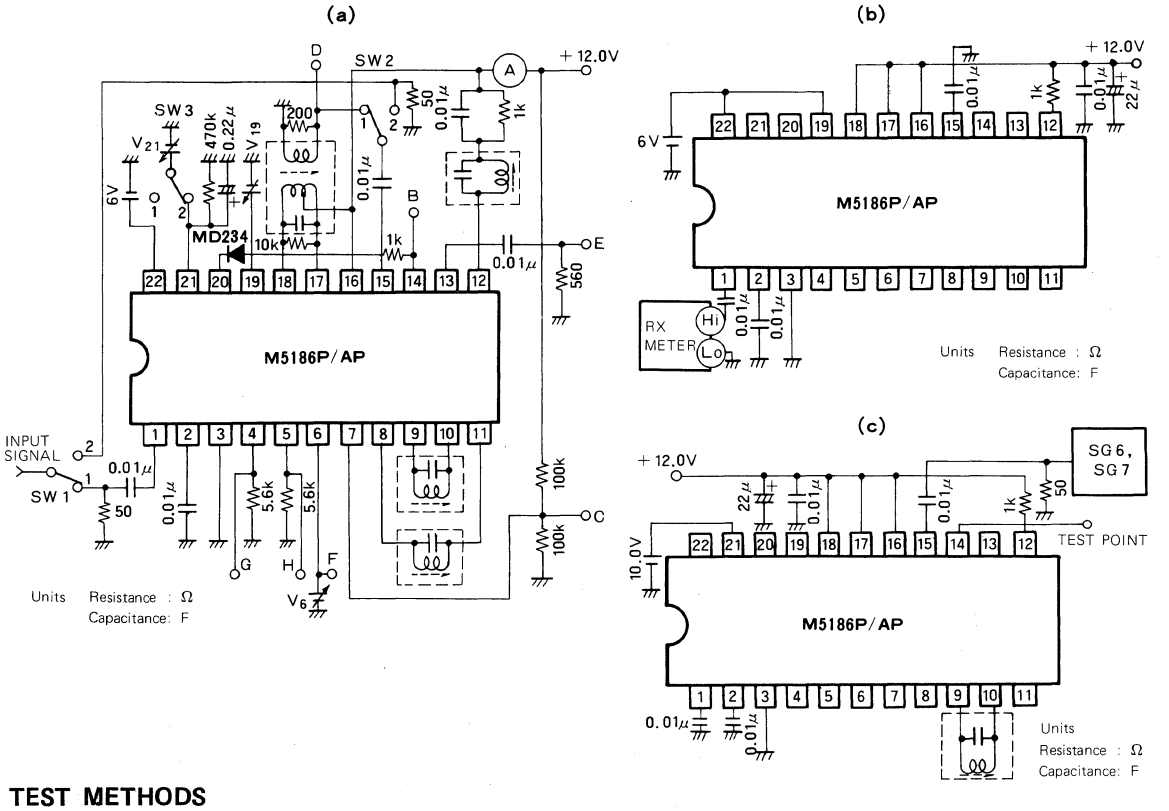
Symbol	Parameter	Test conditions	Test circuit	Limits			Unit
				Min	Typ	Max	
I_{CC}	Circuit current		(a)	36	50	70	mA
$V_{⑭}$	Video amplifier output DC voltage		(a)	4.8	6.0	7.2	V
$V_{⑦}$	AFT output DC voltage		(a)	4.3	5.5	7.0	V
$G_{V(IF)}$	Video IF amplifier maximum voltage gain		(a)	36	41	46	dB
GR	IF AGC control range		(a)	58			dB
$V_{O(DET)}$	Video amplifier output signal voltage		(a)	250	350	500	mVrms
$THD_{(DET)}$	Video amplifier output distortion		(a)			6	%
$V_{O(SIF)}$	Audio IF detector output signal voltage		(a)	30	70	120	mVrms
Δf	AFT detector sensitivity	$V_{⑦}$=3～10V	(a)		130	180	kHz
V_L	AFT switch control range		(a)	1.5	1.8	2.1	V
V_H			(a)	6.2	6.6	7.0	
$V_{④}$-L	RF AGC control range		(a)			0.5	V
$V_{④}$-H			(a)	9.5			
$V_{⑤}$-L			(a)			0.5	
$V_{⑤}$-H			(a)	9.5			
Rin	Video IF amplifier input resistance		(b)		1		kΩ
Cin	Video IF amplifier input capacitance		(b)		7		pF
DG	Video detector differentiation gain response		(c)			7	%
DP	Video detector differentiation phase response		(c)			7	°
f_C	Video amplifier frequency response		(c)		7		MHz

INPUT SIGNALS (levels measured into 50Ω terminations)

SG 1	f_O=58.75MHz, V_i=1mVrms, unmodulated
SG 2	f_O=58.75MHz, V_i=100mVrms, unmodulated
SG 3	f_C=58.75MHz, V_i=20mVrms, f_m=1kHz, 40% AM modulated
SG 4	f_1=58.75MHz, V_i=20mVrms, / f_2=54.25MHz, V_i=2 mVrms, } signals added
SG 5	f = 58.75MHz ± 5MHz sweep signal, V_i = 20mVrms
SG 6	f_c = 58.75MHz / f_m = 3.58MHz overlayed stepped waveform } modulated signal, V_i=variable
SG 7	f_1 = 58.75MHz, V_i = 20mVrms, / f_2 = 58.75MHz − 10MHz sweep signal, V_i = 2mVrms } Signals added

TV VIDEO IF SIGNAL PROCESSING CIRCUIT

TEST CIRCUITS

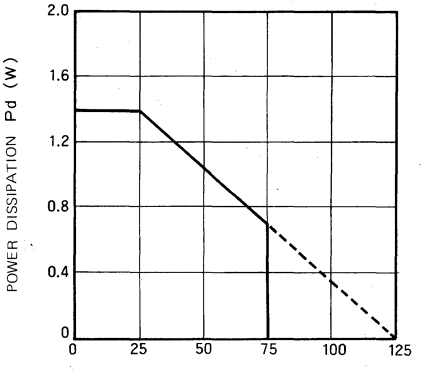


TEST METHODS

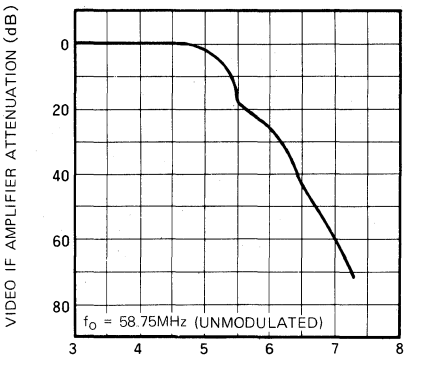
Symbol	Input signal	V⑤(V)	V⑲(V)	V㉑(V)	SW1	SW2	SW3	Test point
I_{CC}	OFF	5.0	10.0		1	1	1	A
V⑭								B
V⑦								C
$G_{V(IF)}$	SG1	5.0	10.0	4.0	1	2	2	D
GR	SG2			10.0				
$V_{O(DET)}$	SG3	5.0	10.0	10.0	2	2	2	B
$THD_{(DET)}$								
$V_{O(SIF)}$	SG4	5.0	4.0		1	1	1	E
Δf	SG5	5.0	10.0	10.0	2	2	2	C
V_L	SG5	Variable	10.0	10.0	2	2	2	F
V_H								
V④-L	OFF	5.0	10.0	10.0	1	1	2	G
V④-H				4.0				
V⑤-L				4.0				H
V⑤-H				10.0				
Rin			6.0					
Cin								
DG	SG6			10.0				
DP								
f_C	SG7			10.0				

TYPICAL CHARACTERISTICS (T_a = 25℃, V_{CC} = 12.0V, unless otherwise noted)

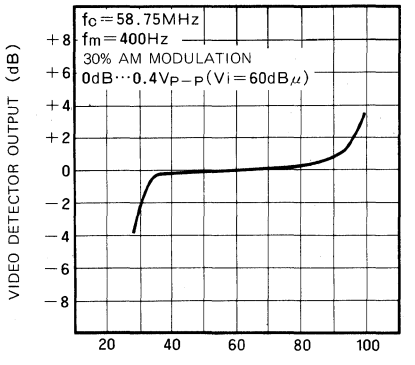
THERMAL DERATING (MAXIMUM RATING)



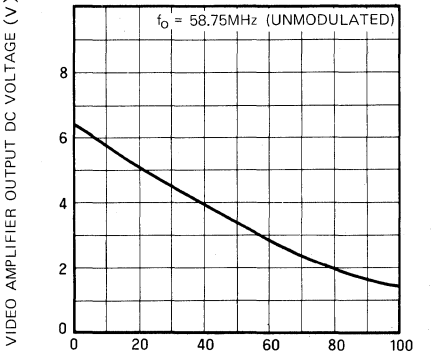
AGC CHARACTERISTICS



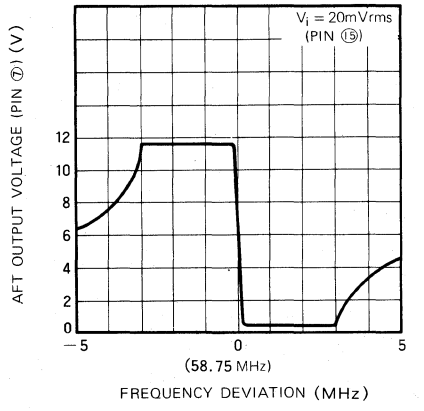
AGC CHARACTERISTICS



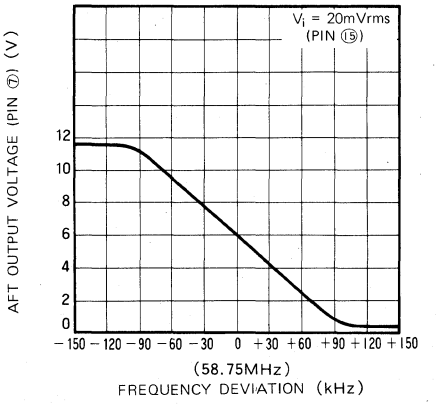
VIDEO DETECTOR LINEARITY



AFT WIDEBAND CHARACTERISTICS



AFT NARROWBAND CHARACTERISTICS



M5187P

SECAM TV VIF SIGNAL PROCESSOR

DESCRIPTION

The M5187P is a semiconductor integrated circuit consisting of a SECAN TV video IF signal processing circuit. It includes a video IF amplifier, video detector, video amplifier, AFT circuit, AFT switching circuit, keyed IF AGC circuits. All these circuits are housed in a 22-pin plastic DIL package.

FEATURES

- Built-in AFT switching circuit
- Synchronous video detection system
- Quadrature detection type AFT circuit
- Excellent AGC characteristics with wide control range
- Keyed AGC system

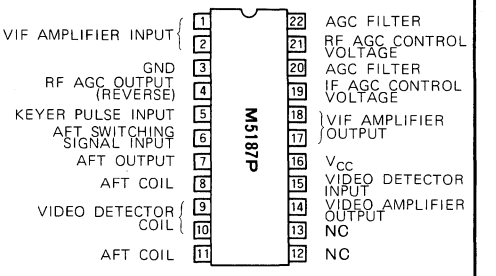
APPLICATION

SECAM TV VIF signal processing

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... 11 ~ 13V
Rated supply voltage 12V

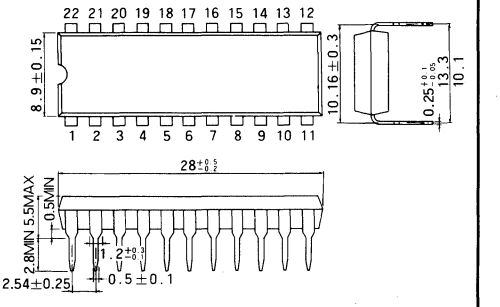
PIN CONFIGURATION (TOP VIEW)



NC: NO CONNECTION

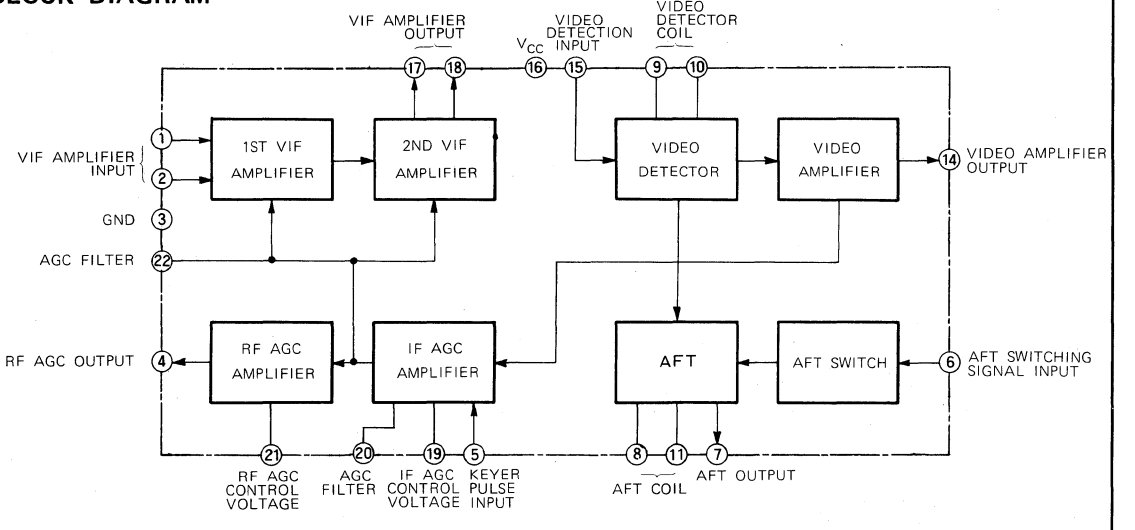
PACKAGE OUTLINE

Dimensions in mm



22-pin plastic DIL package

BLOCK DIAGRAM



SECAM TV VIF SIGNAL PROCESSOR

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		16	V
P_d	Power dissipation		1.4	W
K_θ	Derating	Ta ≧ 25℃	14	mW/℃
Topr	Operating temperature		−20 ~ + 75	℃
Tstg	Storage temperature		−40 ~ + 125	℃

ELECTRICAL CHARACTERISTICS (Ta = 25℃, V_{CC} = 12.0V)

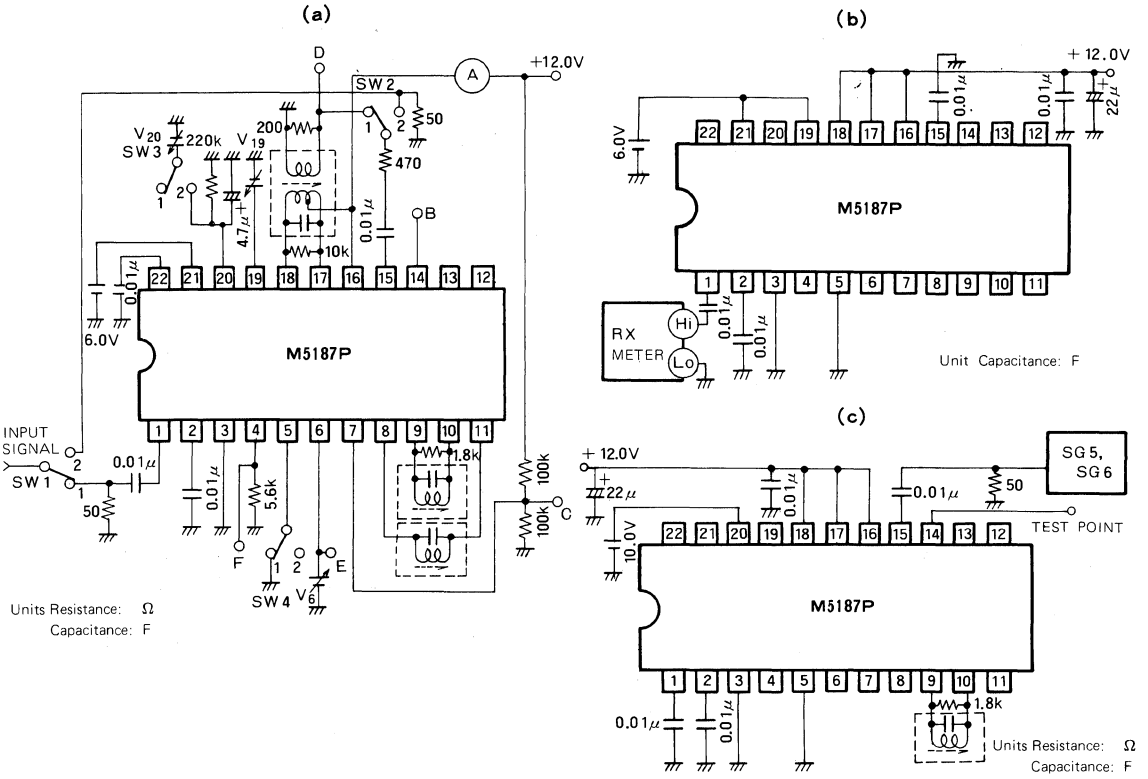
Symbol	Parameter	Test conditions	Test circuit	Limits			Unit
				Min	Typ	Max	
I_{CC}	Circuit current		(a)	33	46	65	mA
$V_{⑭}$	Video amplifier output DC voltage		(a)	5.8	7.0	8.2	V
$V_{⑦}$	AFT output DC voltage		(a)	4.3	5.7	7.2	V
$GV_{(IF)}$	VIF amplifier maximum voltage gain		(a)	38	43	48	dB
GR	IF AGC control range		(a)	58			dB
$V_{O(DET)}$	Video amplifier output signal voltage		(a)	250	350	500	mVrms
$THD_{(DET)}$	Video amplifier output distortion		(a)			6	%
Δf	AFT detector sensitivity	$V_{⑦}$ = 3 ~ 10V	(a)		120	180	kHz
V_L	AFT switch control range		(a)	1.5	1.8	2.1	V
V_H			(a)	6.2	6.6	7.0	
$V_{④-L}$	RF AGC control range		(a)			0.5	V
$V_{④-H}$			(a)	9.5			
R_{in}	VIF amplifier input resistance		(b)		1		kΩ
C_{in}	VIF amplifier input capacitance		(b)		7		pF
DG	Video detector differential gain response		(c)			7	%
DP	Video detector differential phase response		(c)			7	
f_C	Video amplifier frequency response		(c)		7		MHz
Keyed	Keyed AGC control response	$V_{⑭}$ difference between when pin ⑤ is grounded and when left open.	(a)	0.4			V

INPUT SIGNALS (levels measured into 50Ω termination)

SG 1	f_O = 32.7MHz, V_i = 1mVrms, unmodulated
SG 2	f_O = 32.7MHz, V_i = 100mVrms, unmodulated
SG 3	f_C = 32.7MHz, V_i = 20mVrms, f_m = 1kHz, AM40% modulated
SG 4	f = 32.7MHz ± 5MHz signal, V_i = 20mVrms
SG 5	f_C = 32.7MHz f_m = 4.25MHz stepped multiplex waveform } modulated signal, V_i = variable
SG 6	f_1 = 32.7MHz, V_i = 15mVrms f_2 = 32.7MHz + 15MHz sweep signal, V_i = 1.5mVrms } signals added
SG 7	f_O = 32.7MHz, V_i = 20mVrms, unmodulated

MITSUBISHI ELECTRIC

TEST CIRCUITS

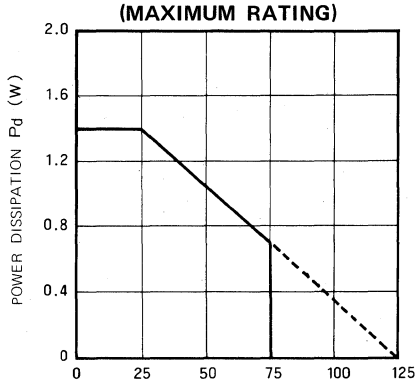


TEST METHODS

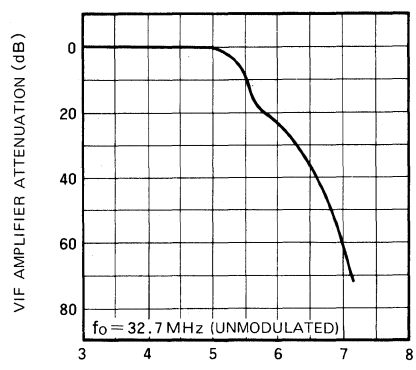
Symbol	Input signal	$V_{⑥}$(V)	$V_{⑲}$(V)	$V_{⑳}$(V)	SW1	SW2	SW3	SW4	Test point
I_{CC}	OFF	5.0	10.0		1	1	1	1	A
$V_{⑭}$									B
$V_{⑦}$									C
$GV_{(IF)}$	SG1	5.0	10.0	4.0	1	2	2	1	D
GR	SG2			10.0					
$V_{O(DET)}$	SG3	5.0	10.0	10.0	2	2	2	1	B
$THD_{(DET)}$									
Δf	SG4	5.0	10.0	10.0	2	2	2	1	C
V_L	SG4	Variable	10.0	10.0	2	2	2	1	E
V_H									
$V_{④-L}$	OFF	5.0	10.0	10.0	1	1	2	1	F
$V_{④-H}$				4.0					
R_{in}			6.0						
C_{in}									
DG	SG5			10.0					
DP									
f_C	SG6			10.0					
Keyed	SG7	5.0	4.7		1	1	1	1	B
								2	

TYPICAL CHARACTERISTICS (Ta = 25℃, V_{CC} = 12.0V, unless otherwise noted)

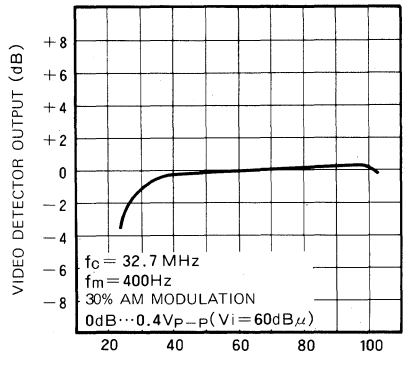
THERMAL DERATING (MAXIMUM RATING)



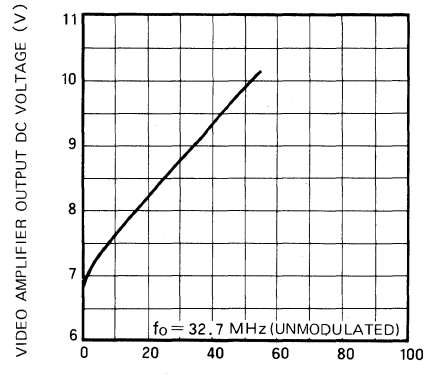
AGC CHARACTERISTICS



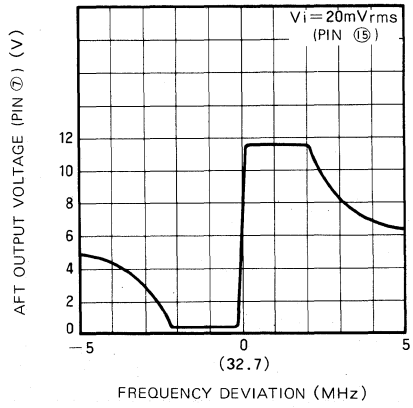
AGC CHARACTERISTICS



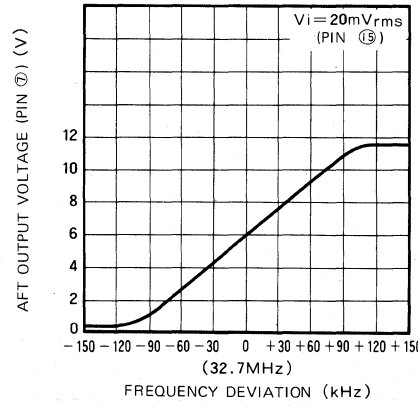
VIDEO DETECTOR LINEARITY



AFT WIDEBAND CHARACTERISTICS



AFT NARROWBAND CHARACTERISTICS



M5190P

NTSC SYSTEM COLOR TV COLOR SIGNAL PROCESSOR

DESCRIPTION

The M5190P is a semiconductor integrated circuit consisting of an NTSC color signal processor for color TV sets. The use of an injection lock system for color synchronization reduces the number of externally mounted parts and DC for color saturation and color phase control facilitates circuit interconnection.

FEATURES

- Low number of externally mounted parts
- DC for color saturation and color phase control
- 3.58MHz color subcarrier oscillator based on an injection lock system
- Built-in color killer circuit using a Schmitt trigger
- ACC circuit provided
- Highly sensitive synchronized oscillation.
- Built-in voltage regulator

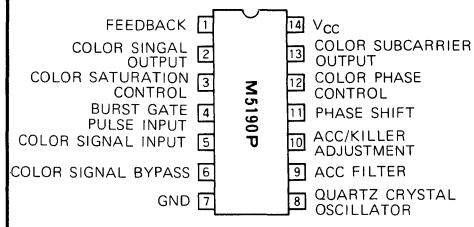
APPLICATION

NTSC system color TV color signal processing

RECOMMENDED OPERATING CONDITIONS

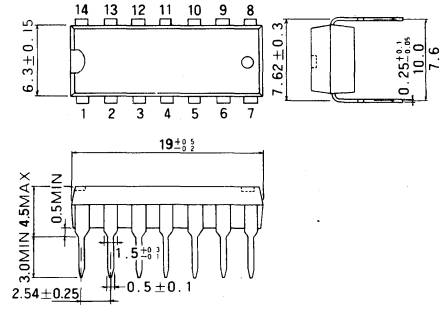
Rated supply voltage ..... 20V (R_S=390Ω)

PIN CONFIGURATION (TOP VIEW)



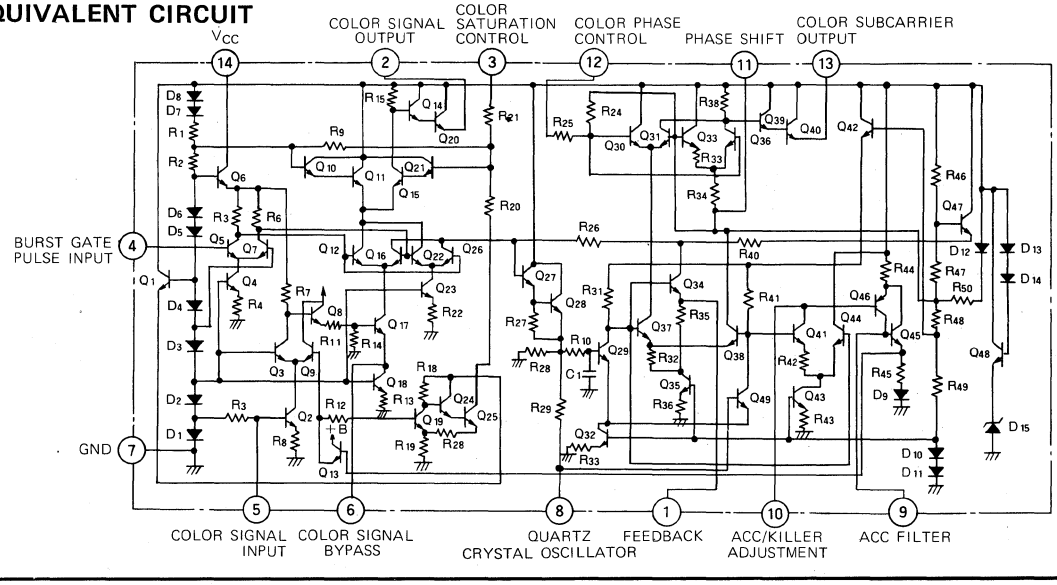
PACKAGE OUTLINE

Dimensions in mm



14-pin plastic DIL package

EQUIVALENT CIRCUIT



NTSC SYSTEM COLOR TV COLOR SIGNAL PROCESSOR

ABSOLUTE MAXIMUM RATINGS (Ta=25°C, unless otherwise noted)

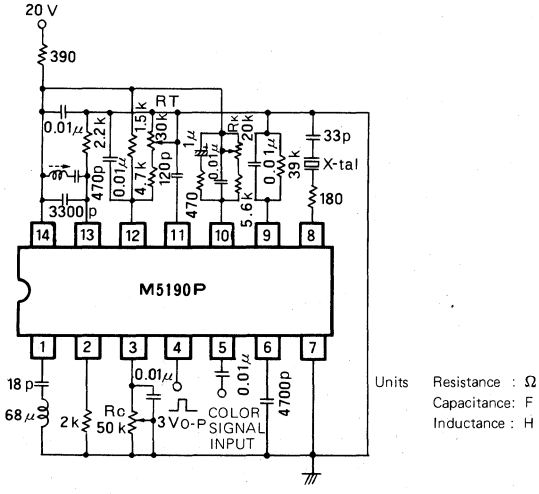
Symbol	Parameter	Conditions	Limits	Unit
I_{CC}	Circuit current		32	mA
$I_{⑭}$	Horizontal pulse input current		250	μApeak
Pd	Power dissipation		700	mW
K_θ	Derating	Ta≧25°C	7.0	mW/°C
Topr	Operating temperature		−20～+75	°C
Tstg	Storage temperature		−40～+125	°C

ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{CC}=20V, Rs=390Ω)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$V_{⑭}$	Pin ⑭ voltage	Input OFF, R_C = 7.5Ω, R_T = 4.5kΩ	8.6	9.2	10	V
Vcmax	Color signal maximum output	Input 0dB, R_C 50kΩ, R_T = 4.5kΩ	2.0	2.9		V_{P-P}
G_C	Color signal maximum gain	Input -20dB, R_C = 50kΩ, R_T = 4.5kΩ	34	40		dB
R_K	Killer operating resistance		1	8	16	kΩ
R_{ACC}	ACC control range	Input +6dB～-10dB	5	15	30	%
V_{CW}	Color subcarrier output		0.55	0.75	1.0	V_{P-P}
C	Color saturation variation	R_C=0～50kΩ	40			dB
T	Color phase variation	R_T=0～30kΩ		126		deg

Input 0dB = 60mVp-p (frequency: 3.579545MHz)

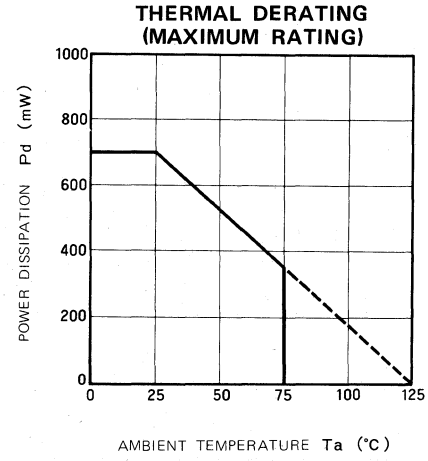
TEST CIRCUIT



Units Resistance : Ω
Capacitance: F
Inductance : H

TYPICAL CHARACTERISTICS

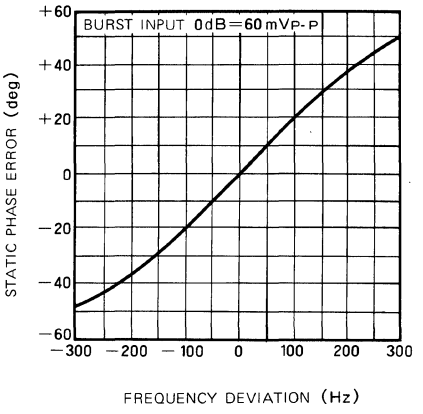
(Ta=25°C, V_{CC}=20V, Rs=390Ω, unless otherwise noted)



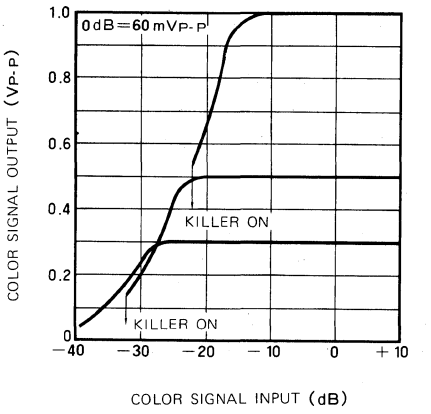
MITSUBISHI ELECTRIC

NTSC SYSTEM COLOR TV COLOR SIGNAL PROCESSOR

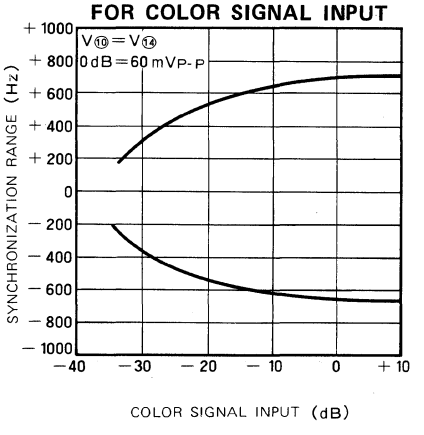
STATIC PHASE ERROR



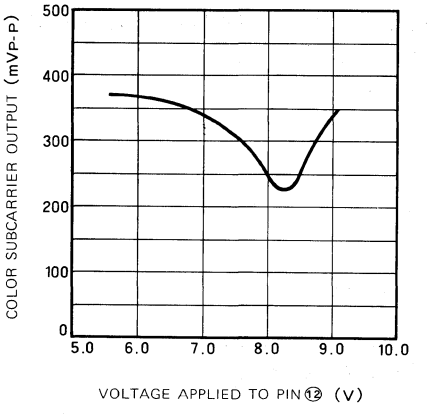
ACC CHARACTERISTICS



PULL-IN RANGE ON SYNCHRONIZATION FOR COLOR SIGNAL INPUT

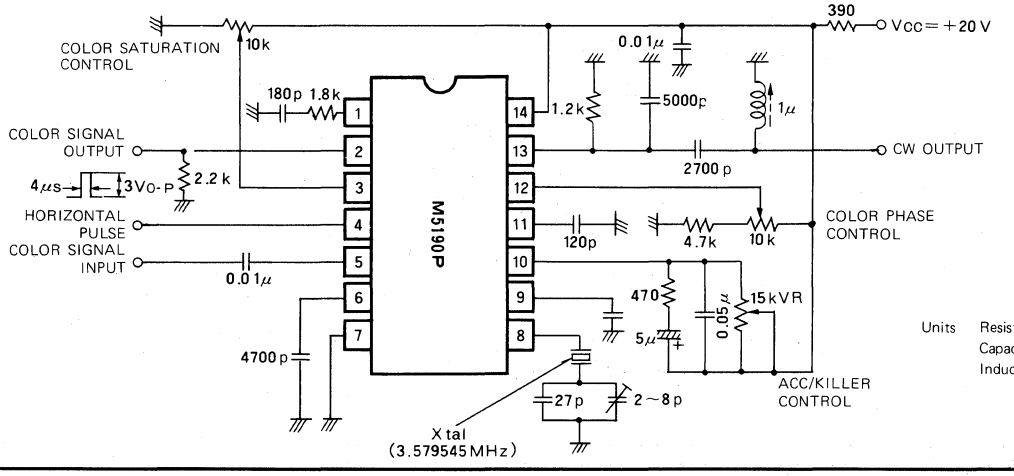


COLOR PHASE CONTROL-BASED COLOR SUBCARRIER OUTPUT



APPLICATION EXAMPLE

NTSC Color Signal Processor



M5192P

NTSC SYSTEM COLOR TV COLOR SIGNAL DEMODULATOR

DESCRIPTION

The M5192P is a semiconductor integrated circuit consisting of an NTSC system color TV color demodulation and includes a vector demodulator and matrix circuit. It not only features excellent temperature characteristics for the DC output offset voltage for each axis and DC output level for each axis as well as minimal offset but is also provided with a luminance signal adder circuit, thereby enabling RGB direct-coupled drive.

FEATURES

- Double balanced demodulator circuit
- Excellent balance between 3 outputs
- Low temperature coefficient for DC output offset voltage
- Low DC output offset voltage across all axes
- Low temperature coefficient of DC output offset voltage across all axes
- Low unbalanced output

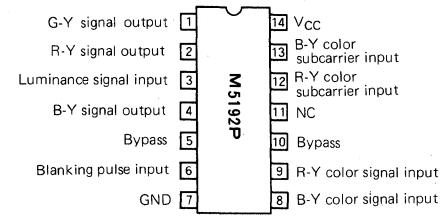
APPLICATION

NTSC system color TV sets

RECOMMENDED OPERATING CONDITIONS

Supply voltage ..... 16 ~ 26V
Rated supply voltage 24V

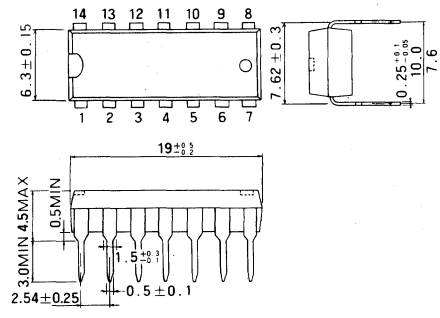
PIN CONFIGURATION (TOP VIEW)



NC: NO CONNECTION

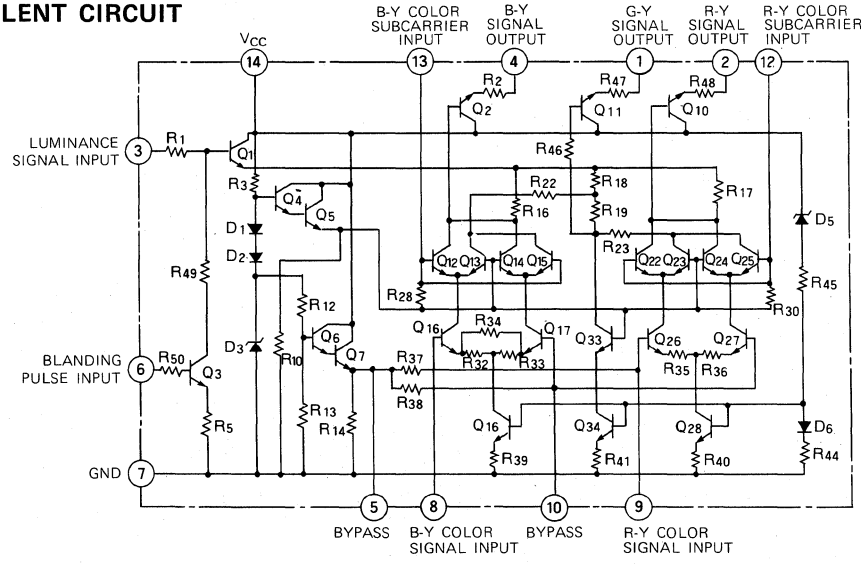
PACKAGE OUTLINE

Dimensions in mm



14-pin plastic DIL package

EQUIVALENT CIRCUIT



MITSUBISHI ELECTRIC

NTSC SYSTEM COLOR TV COLOR SIGNAL DEMODULATOR

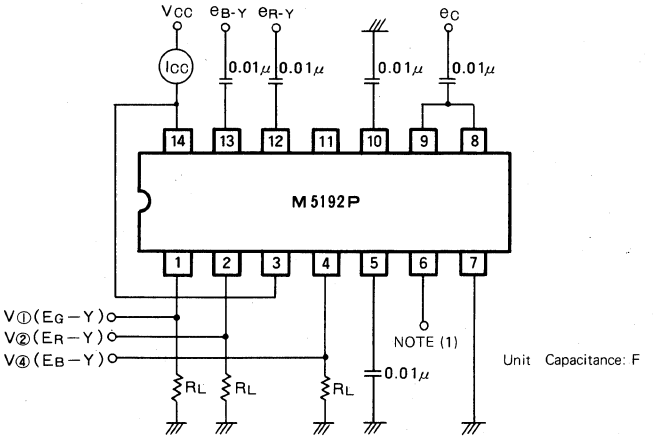
ABSOLUTE MAXIMUM RATINGS (Ta=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		28	V
R_L	Load resistnace		3 (min)	kΩ
e_{B-Y} e_{R-Y}	Color subcarrier input voltage		5	V_{P-P}
e_C	Color signal input voltage		5	V_{P-P}
e_Y	Luminance signal input voltage		$V_{CC}-5 \leqq e_C \leqq V_{CC}$	V_{P-P}
V_{BLK}	Blanking pulse input voltage		5	V_{P-P}
Pd	Power dissipation		700	mW
K_θ	Derating	Ta≧25°C	7.0	mW/°C
Topr	Operating temperature		−20～+75	°C
Tstg	Storage temperature		−40～+125	°C

ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{CC}=24V, unless otherwise noted)

Symbol	Parameter	Test conditions				Limits			Unit
		e_C (V_{P-P})	e_{B-Y} (V_{P-P})	e_{R-Y} (V_{P-P})		Min	Typ	Max	
I_{CC}	Circuit current	0	0	0	R_L=1MΩ	5	9	14	mA
		0	0	0		16	22	27	mA
V①, V②, V④	Output voltage	0	0	0	R_L=3.3kΩ	13.5	14.5	15.5	V
ΔV	Output offset voltage	0	0	0	V③=V_{CC}		0	0.45	V
$\varkappa$	Output potential temperature coefficient	0	0	0			0	4	mV/°C
e_C	B-Y input voltage		0.4	0.4	R_L=3.3kΩ		0.4	0.7	V_{P-P}
E_{R-Y}	R-Y output voltage		0.4	0.4	V③=V_{CC}		3.8		V_{P-P}
E_{G-Y}	G-Y output voltage		0.4	0.4	E_{B-Y}=5V_{P-P}		1.0		V_{P-P}
θ_{B-R}	Relative demodulation angle						106		deg.
θ_{B-G}							256		
E_U	Unbalanced output	0	2	2	R_L=3.3kΩ V③=V_{CC}		0.2		V_{P-P}
ΔV_{BLK}	Blanking voltage drop				V⑥=4V	0.8	1.5	3.0	V

TEST CIRCUIT

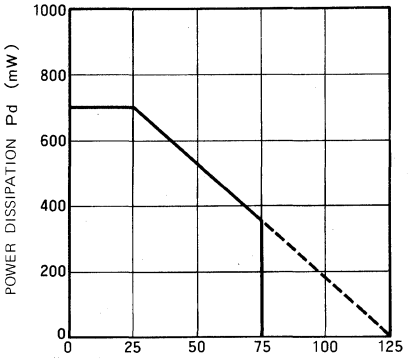


Note : Apply 4V only when measuring ΔV_{BLK}

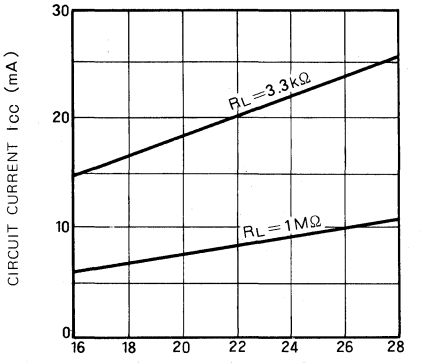
NTSC SYSTEM COLOR TV COLOR SIGNAL DEMODULATOR

TYPICAL CHARACTERISTICS (Ta=25°C, unless otherwise noted)

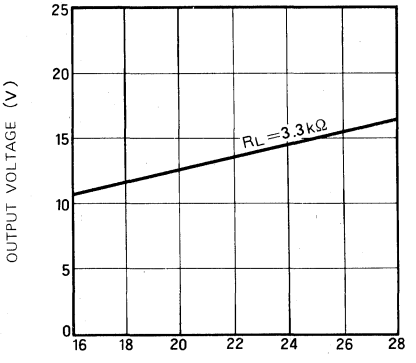
THERMAL DERATING (MAXIMUM RATING)



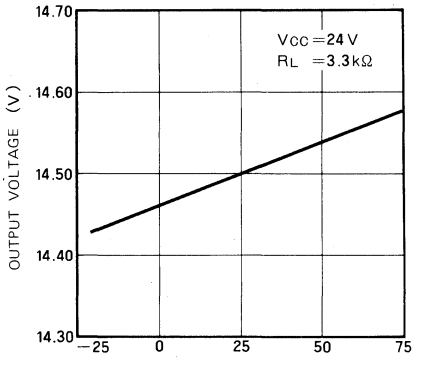
CIRCUIT CURRENT VS SUPPLY VOLTAGE



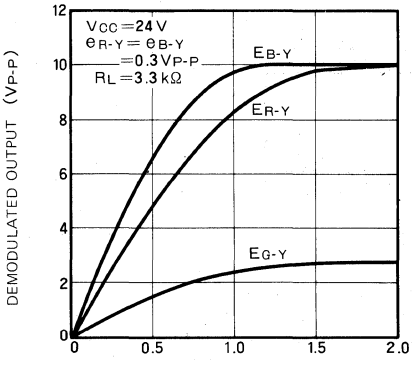
OUTPUT VOLTAGE VS SUPPLY VOLTAGE



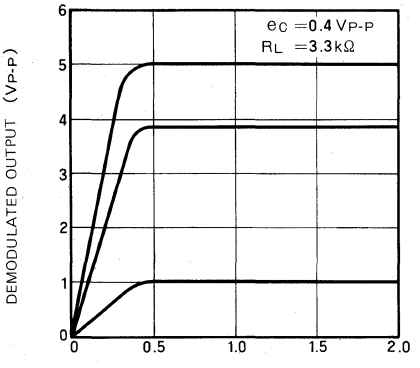
OUTPUT VOLTAGE VS TEMPERATURE CHARACTERISTICS



DEMODULATION LINEARITY

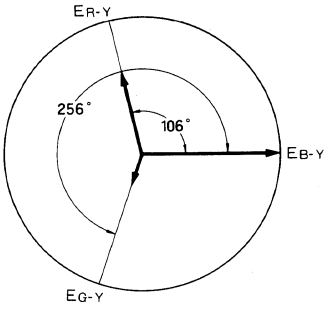


DEMODULATED OUTPUT VS COLOR SUBCARRIER INPUT VOLTAGE



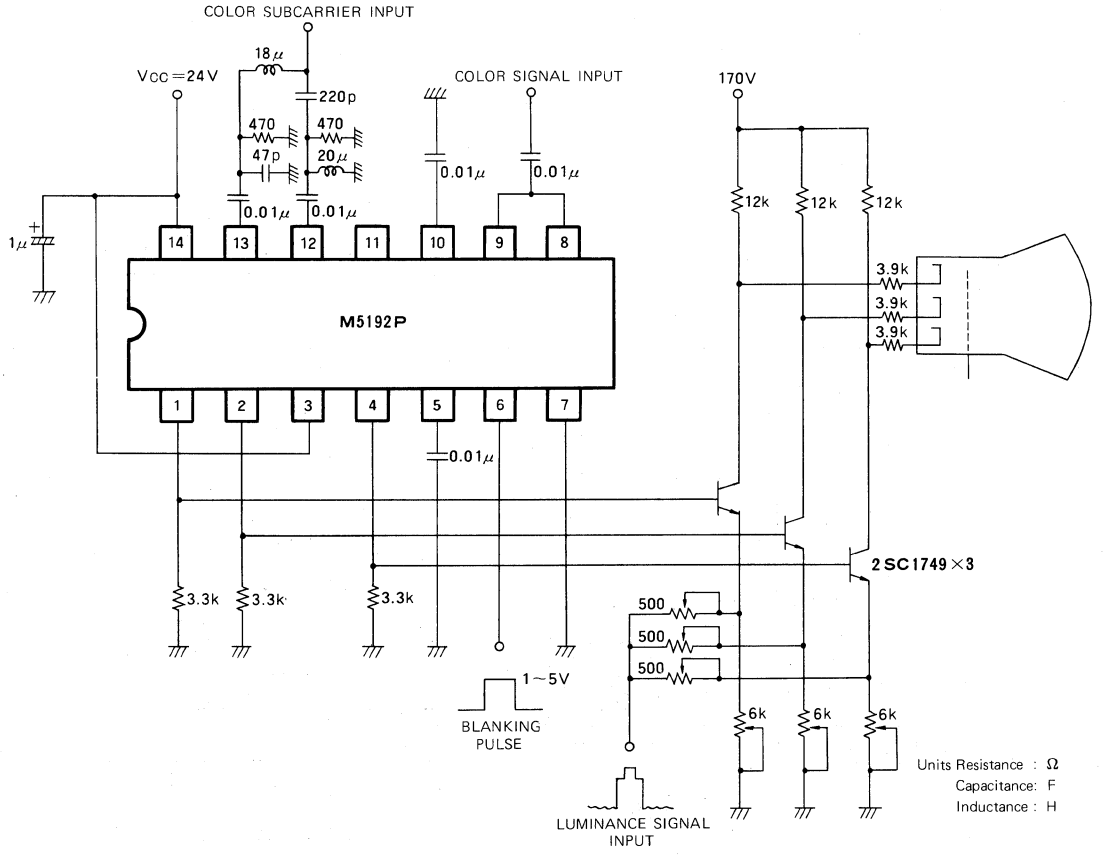
NTSC SYSTEM COLOR TV COLOR SIGNAL DEMODULATOR

RELATIVE DEMODULATION ANGLES



APPLICATION EXAMPLE

NTSC system color TV color signal demodulator



M5193P

NTSC SYSTEM COLOR TV COLOR SIGNAL PROCESSOR

DESCRIPTION

The M5193P is a semiconductor integrated circuit consisting of an NTSC color signal processor and demodulator circuit. APC color synchronization is used and DC color-phase control is employed to ensure stability.

FEATURES

- Peak-type ACC detector
- Internal setting of ACC and color killer levels
- APC system uses sample and hold for color synchronization
- Detector circuit has excellent output temperature characteristics
- 22-pin DIL package

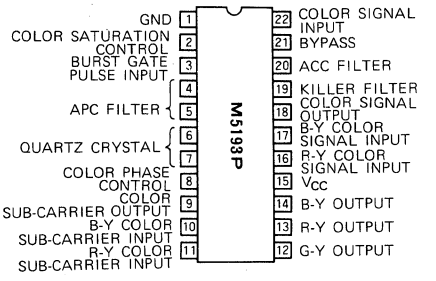
APPLICATION

NTSC color TV color signal processing

RECOMMENDED OPERATING CONDITIONS

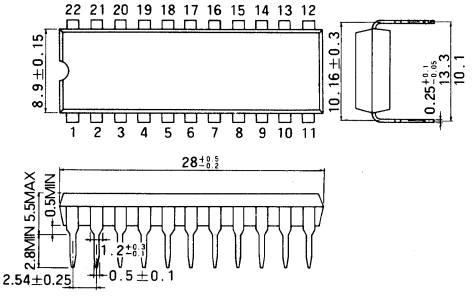
Supply supply voltage range ..... 11~13V
Rated supply voltage 12V

PIN CONFIGURATION (TOP VIEW)



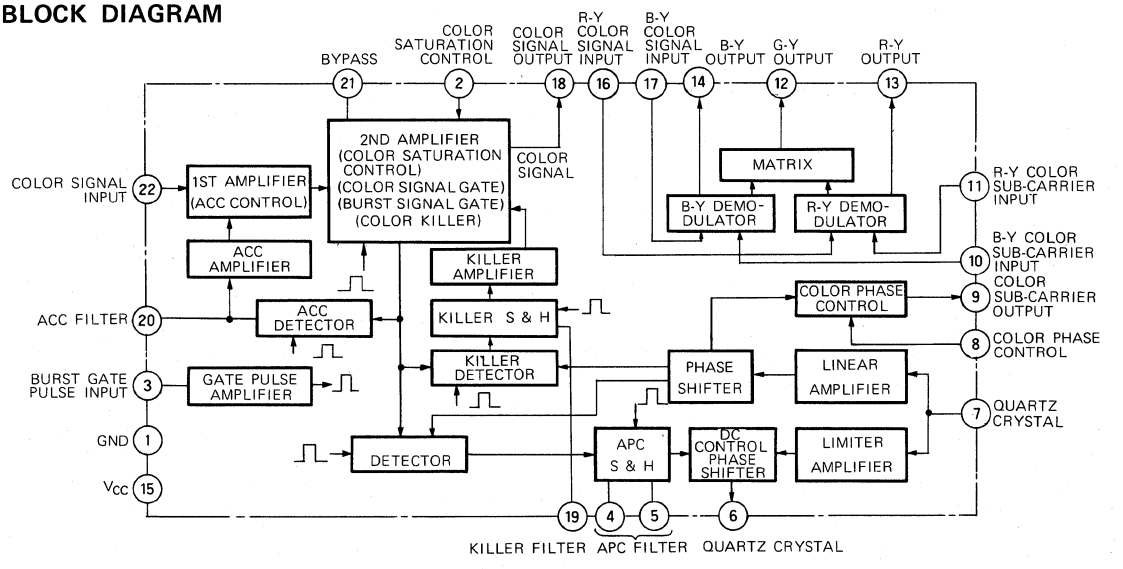
PACKAGE OUTLINE

Dimensions in mm



22-pin plastic DIL package

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

NTSC SYSTEM COLOR TV COLOR SIGNAL PROCESSOR

ABSOLUTE MAXIMUM RATINGS (Ta=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		16.0	V
Pd	Power dissipation		1.4	W
K_θ	Derating	Ta≧25°C	14	mW/°C
Topr	Operating temperature		−20～+75	°C
Tstg	Storage temperature		−40～+125	°C

ELECTRICAL CHARACTERISTICS (Ta=25°C, Vcc=12V, unless otherwise noted)

Symbol	Parameter	Test conditions				Limits			Unit
		Color signal input (dB)	Pin②voltage (V)	Pin⑧voltage (V)		Min	Typ	Max	
I_{CC}	Circuit current	OFF	6	6		27	38	49	mA
G_C	Color signal maximum gain	−22	8	6		36	42	47	dB
Vcmax	Color signal maximum output	0	8	6		0.9	1.25	1.6	V_{P-P}
R_{ACC}	ACC control range		6	6	Note (1)	−18			dB
$V_{i\,(K)}$	Killer operational input level		6	6		−46	−37	−28	dB
C	Color saturation characteristics	0	4～8	6		40			dB
T	Color phase characteristics	0	5.5	4～8			90		deg.
F_P	APC pull-in range	0	6	6		±400			Hz
E_{ODC}	Output voltage	OFF	6	6		6.6	7.0	7.4	V
ΔE_{ODC}	Output offset voltage	OFF	6	6				0.3	V
$\delta E_{ODC}/\delta T$	Output voltage temperature coefficient	OFF	6	6		−2	0	2	mV/°C
E_{Omax}	Maximum demodulated output voltage	0	8	6	Note (2)	4.0			V_{P-P}
E_{CO}	B-Y demodulation sensitivity	0		6	Note (2), (3)	3.0	4.0	5.0	V_{P-P}
$E_{O(R-Y)}/E_{O(B-Y)}$	Demodulated output voltage ratio	0		6	Note (2), (4)		0.81		
$E_{O(G-Y)}/E_{O(B-Y)}$		0		6	Note (2), (4)		0.32		
θ_{R-Y}	Demodulated phase angle	0	5.5	6			106		deg.
θ_{B-Y}		0	5.5	6			259		deg.

● Color input signal consists of 50mVp-p burst portion and 100mVp-p color portion, treated as 0dB levels (frequency=3.579545MHz±5Hz)

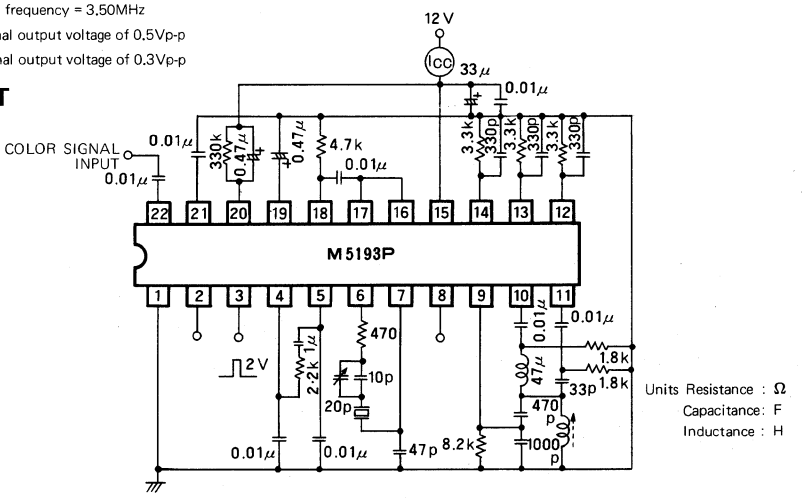
Note (1) ACC control range is the input level when color output voltage decreased by 3dB compared with color output voltage which occurs with a 0 dB color input signal

Note (2) Color portion frequency = 3.50MHz

Note (3) For color signal output voltage of 0.5Vp-p

Note (4) For color signal output voltage of 0.3Vp-p

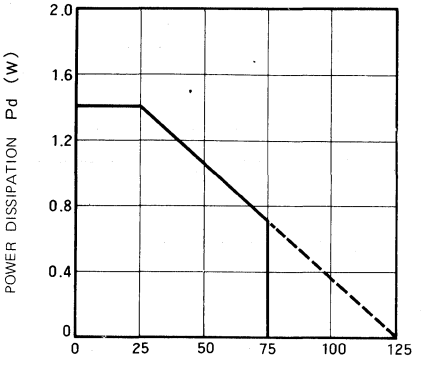
TEST CIRCUIT



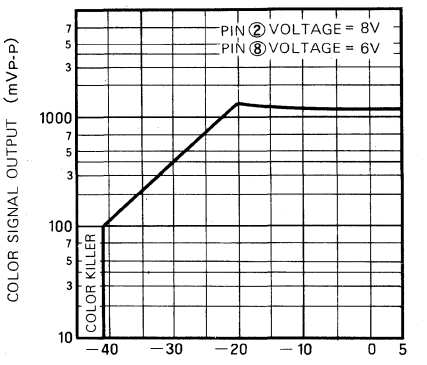
NTSC SYSTEM COLOR TV COLOR SIGNAL PROCESSOR

TYPICAL CHARACTERISTICS (Ta=25°C, Vcc=12V, unless otherwise noted)

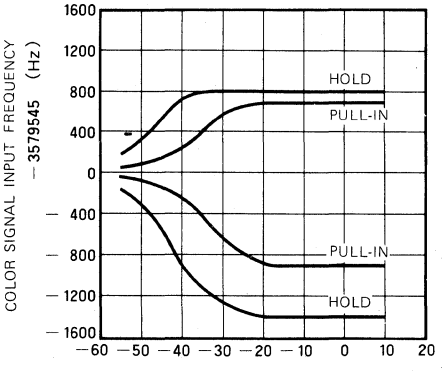
THERMAL DERATING (MAXIMUM RATING)



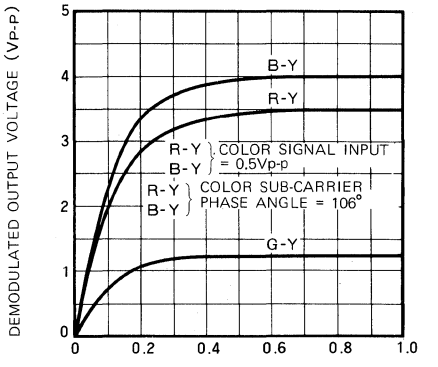
ACC CHARACTERISTICS



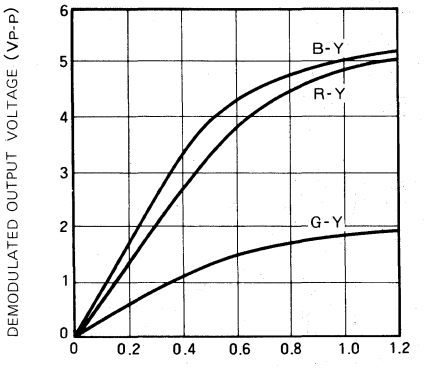
APC PULL-IN/HOLD CHARACTERISTICS



DEMODULATED OUTPUT VOLTAGE VS COLOR SUB-CARRIER INPUT



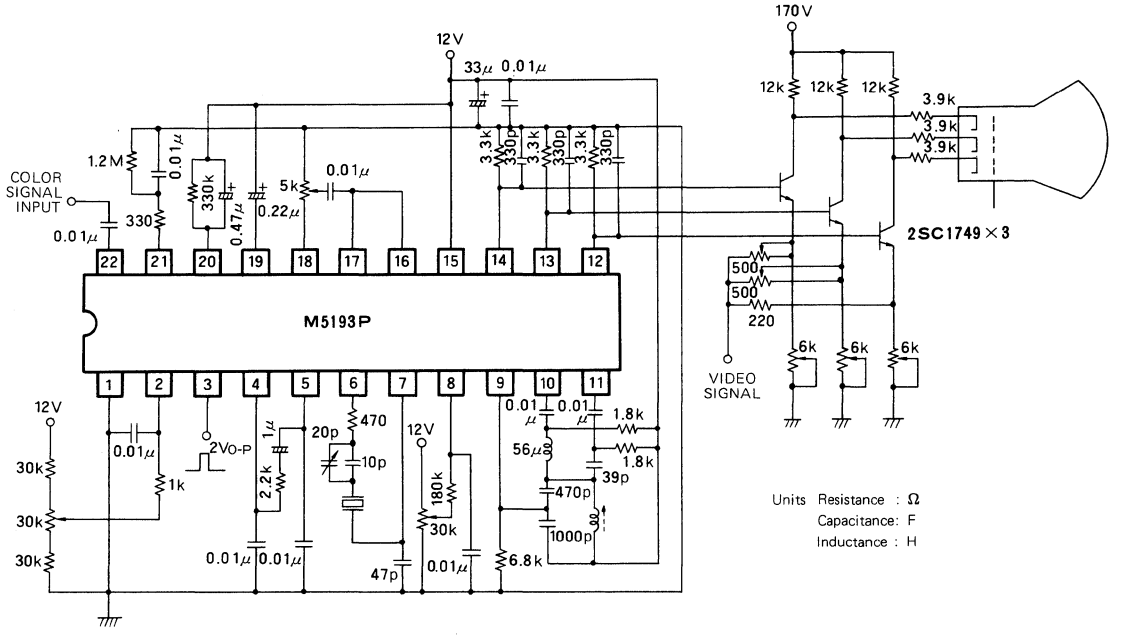
DEMODULATED OUTPUT VOLTAGE VS B-Y, R-Y COLOR SIGNAL INPUT



NTSC SYSTEM COLOR TV COLOR SIGNAL PROCESSOR

APPLICATION EXAMPLE

NTSC color TV color signal processing circuit



M5194P/AP

PAL SYSTEM COLOR TV SIGNAL PROCESSOR

DESCRIPTION

The M5194P/AP is a semiconductor integrated circuit consisting of a PAL system color TV signal processing circuit including the circuitry required to process and demodulate a PAL system color TV signal. An APC-type color sync circuit is used and DC control is used for color saturation control to ensure stability.

FEATURES

- Peak-type ACC detector
- Internal setting of ACC and color killer levels
- An APC-type sample and hold circuit is used for color synchronization
- Highly temperature-stable demodulator circuit
- Housed in a 22-pin DIL package

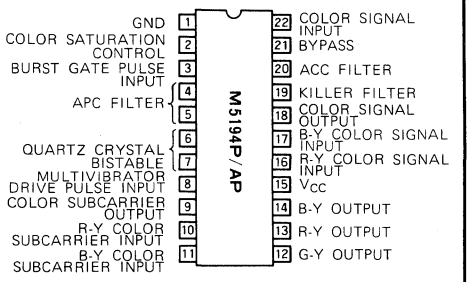
APPLICATION

PAL system color TV signal processing

RECOMMENDED OPERATING CONDITIONS

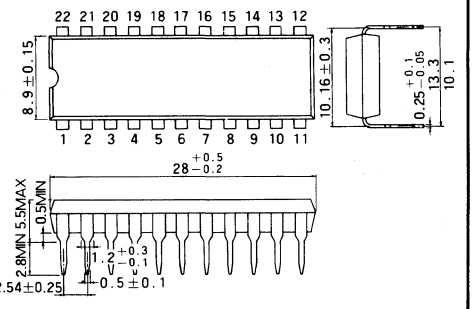
Supply voltage range . . . . . 11~13V
Rated supply voltage 12V

PIN CONFIGURATION (TOP VIEW)



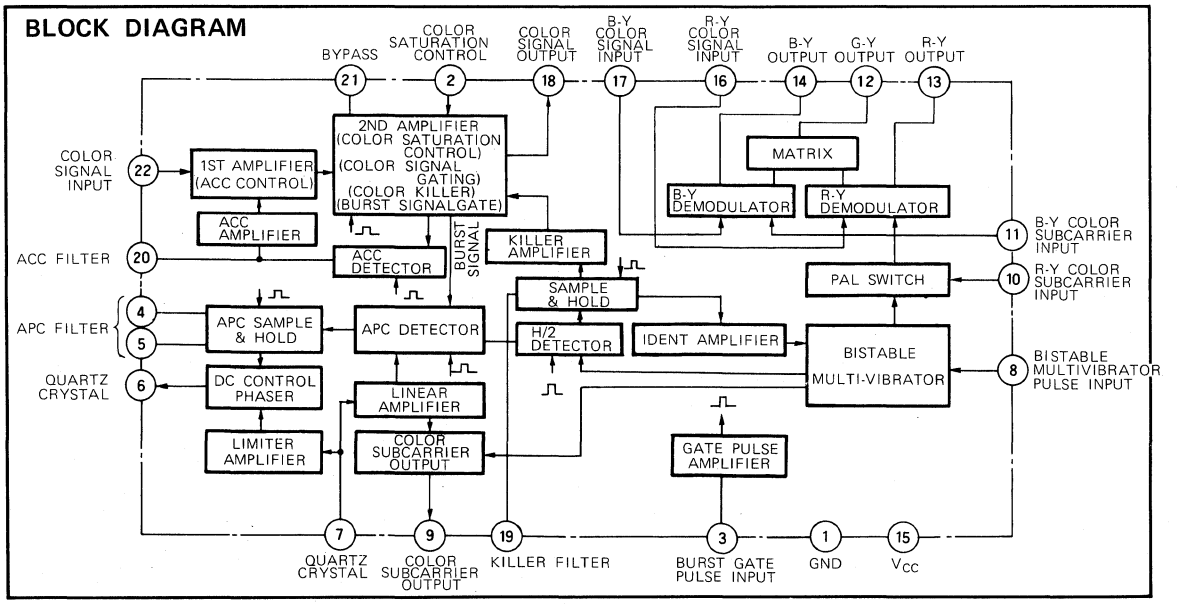
PACKAGE OUTLINE

Dimensions in mm



22-pin plastic DIL package

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

PAL SYSTEM COLOR TV SIGNAL PROCESSOR

ABSOLUTE MAXIMUM RATINGS (Ta=25°C, unless otherwise noted)

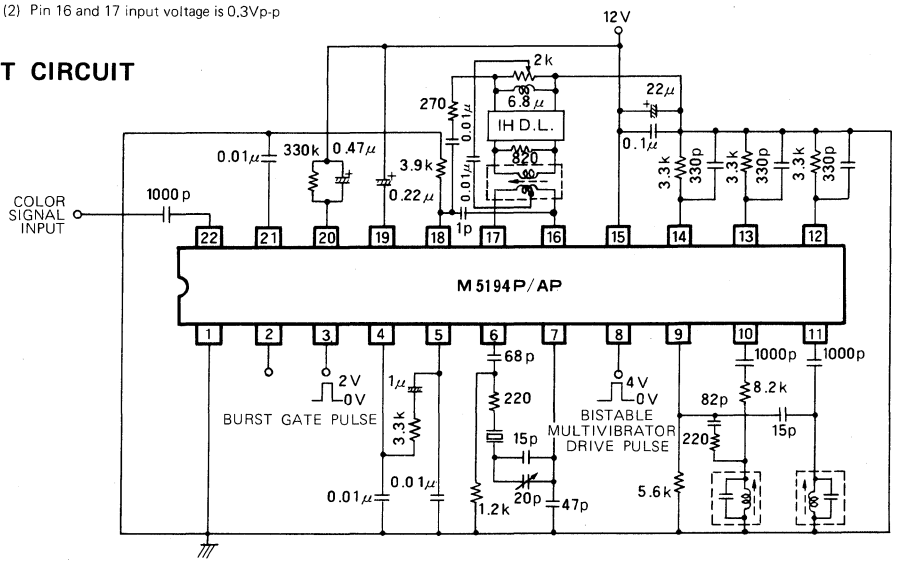
Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		16.0	V
Pd	Power dissipation		1.4	W
K_θ	Derating	Ta≧25°C	14	mW/°C
Topr	Operating temperature		−20～+75	°C
Tstg	Storage temperature		−40～+125	°C

ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{CC}=12V, unless otherwise noted)

Symbol	Parameter	Test conditions			Limits			Unit
		Color signal input (dB)	Pin ② voltage (V)		Min	Typ	Max	
I_{CC}	Circuit current	OFF	6		25	34	43	mA
G_C	Maximum color signal gain	−22	8		37	42	47	dB
Vcmax	Maximum color signal output	0	8		1.0	1.50	2.0	V_{P-P}
R_{ACC}	ACC control range		6		−16			dB
$V_{i(K)}$	Killer operating input level		6	M5194P	−45	−35	−30	dB
				M5194AP	−48	−38	−30	
$V_{i(I)}$	Indent operating input level		6				$V_{i(K)}$	dB
C	Color saturation variation	0	4～8		40			dB
F_P	APC pull-in range	0	6		±400			Hz
E_{ODC}	Output voltage	OFF	6	M5194P	6.6	7.0	7.4	V
				M5194AP	6.8	7.2	7.6	
ΔE_{ODC}	Output offset voltage	OFF	6				0.3	mV/°C
$\delta E_{ODC}/\delta T$	Output voltage temperature coefficient	OFF	6		−2	0	2	mV/°C
Eomax	Demodulated output voltage	0	8	Note (1)	4.0			V_{P-P}
Eco	B-Y demodulation sensitivity	0		Note (1) Note (2)	3.0	4.0	5.0	V_{P-P}
$E_{O(R-Y)}/E_{O(B-Y)}$	Demodulated output voltage ratio	0		Note (1) Note (2)		0.61		
$E_{O(G-Y)}/E_{O(B-Y)}$		0		Note (1) Note (2)		0.36		

● Input Signals are 50mVp-p color burst signal, and 100mVp-p color signal taken as 0dB (frequency = 4.433619MHz ±5Hz)
Note (1) Color section frequency is 4.424MHz
Note (2) Pin 16 and 17 input voltage is 0.3Vp-p

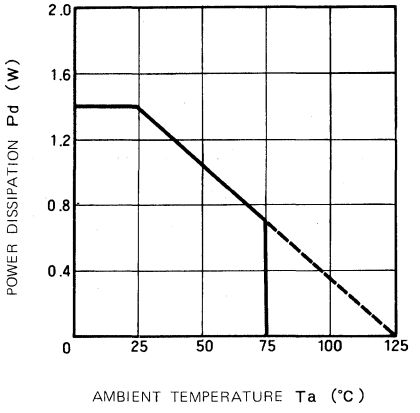
TEST CIRCUIT



Units Resistance: Ω
Capacitance: F
Inductance: H

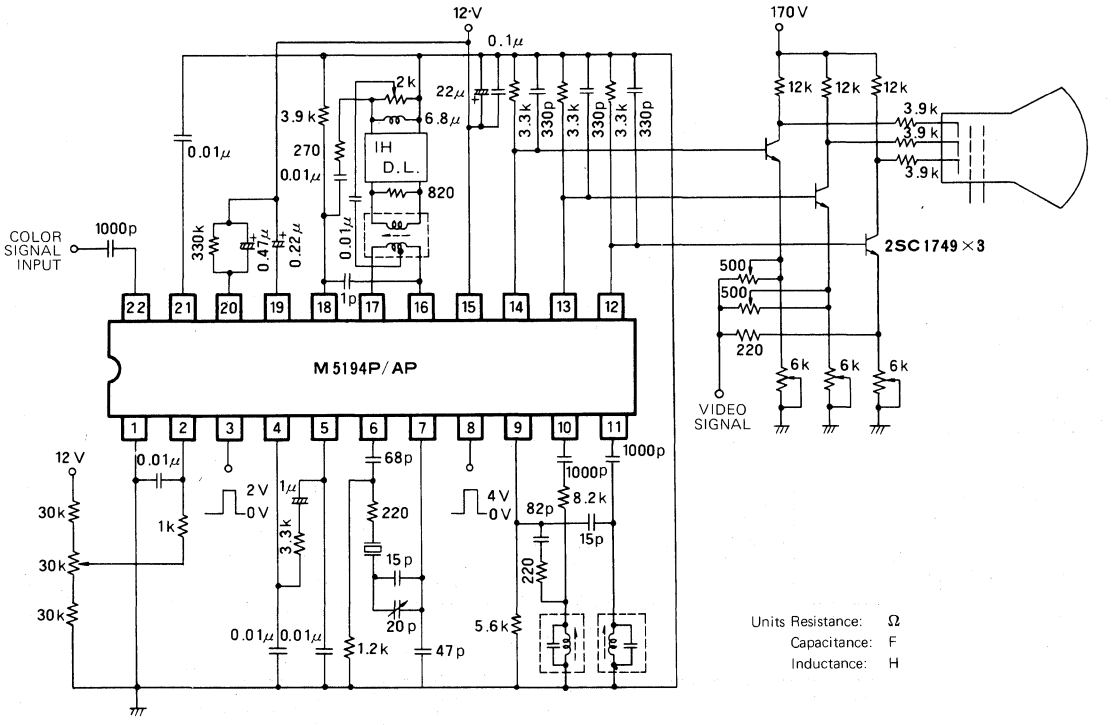
TYPICAL CHARACTERISTICS (Ta=25°C, unless otherwise noted)

THERMAL DERATING
(MAXIMUM RATING)



APPLICATION EXAMPLE

PAL system color TV signal processing circuit



MITSUBISHI ELECTRIC

M5195P

TV VIDEO SIGNAL PROCESSOR & SYNC SEPARATOR

DESCRIPTION

The M5195P is a semiconductor integrated circuit consisting of a video signal processor and sync separator. It is designed for TV video signal processing and sync separation, and its functions include video tone control, brightness control, contrast control, pedestal clamping, video output, noise cancelling and sync separation.

FEATURES

- DC voltage control of video tone, brightness and contrast.
- Video tone control uses a double differentiation system and since peaking pins are accessible, the overshoot and preshoot can be set optionally.
- Variable DC regeneration ratio
- Direct drive of color signal output transistors is possible
- Pedestal clamp pulse not required
- Built-in peak limiter circuit
- Built-in blanking circuit

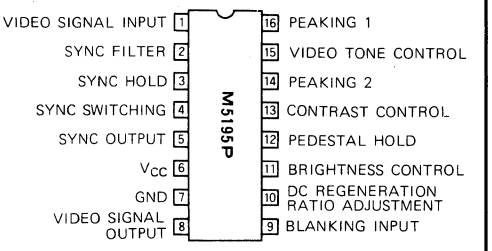
APPLICATION

TV video signal processing and sync separation

RECOMMENDED OPERATING CONDITIONS

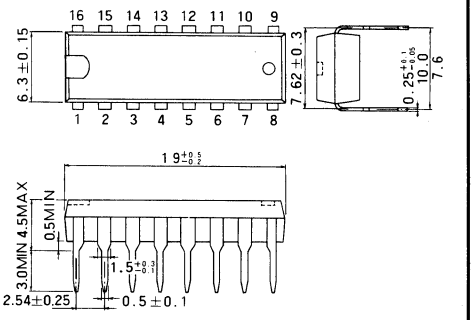
Supply voltage range ..... 11.0~13.0V
Rated supply voltage 12.0V

PIN CONFIGURATION (TOP VIEW)



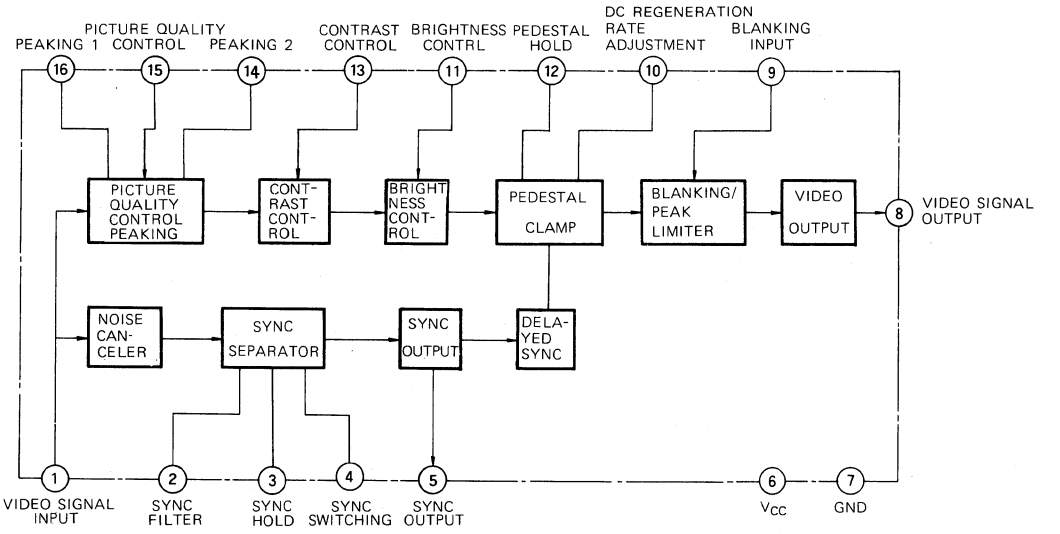
PACKAGE OUTLINE

Dimensions in mm



16-pin plastic DIL package

BLOCK DIAGRAM



TV VIDEO SIGNAL PROCESSOR & SYNC SEPARATOR

ABSOLUTE MAXIMUM RATINGS (Ta=25°C, unless otherwise noted)

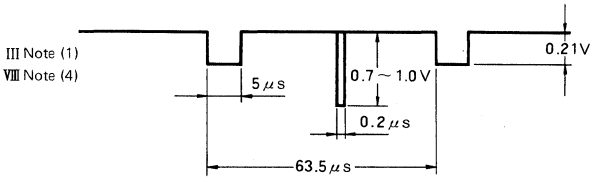
Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		16.0	V
Pd	Power dissipation		700	mW
K_θ	Derating	Ta≧25°C	7	mW/°C
Topr	Operating temperatue		−20～+75	°C
Tstg	Storage temperature		−40～+125	°C

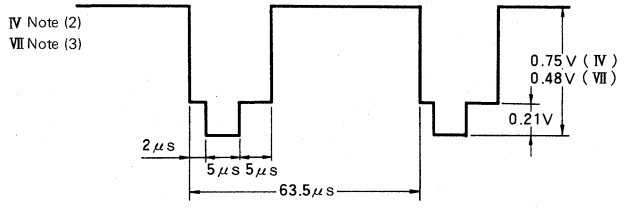
ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{CC}=12.0V, unless otherwise noted)

Symbol	Parameter	Test conditions				Test circuit	Limits			Unit
		Video signal (Note)	SW1	SW2	SW3		Min	Typ	Max	
I_{CC1}	Circuit current 1	Ⅶ	①	①	②		30	38	46	mA
I_{CC2}	Circuit current 2	Ⅶ	①	①	②		18	25	34	mA
Vomax	Maximum video output	II	①	②	②		7.0	8.0		V_{P-P}
Gvmax	Maximum video voltage gain	I	①	②	②		14.5	17.5	21.5	dB
Vplim	Peak limiter operating voltage	Ⅳ	①	①	①		3.8	4.2	4.6	V_{O-P}
V_{BLK}	Blanking operating voltage	Ⅳ	①	①	①		5.0	5.4	5.7	V
f_B	Frequency band response	I, V	①	②	②		−2	0	+1	dB
Gpmax	Maximum video peaking	I, Ⅵ	②	②	②		13.5	16	20.5	dB
V_{NC}	Noise cancelation level	Ⅷ	①	①	①			0.7	1.0	V_{P-P}
W_S	Sync output pulse width	III	①	①	①		3.3	3.9	4.2	μs
V_{OS}	Sync output pulse amplitude	III	①	①	①		10.0	10.5		V_{P-P}
$\delta V_{ODC}/\delta Ta$	Video output pin voltage temperature dependability	Ⅶ	①	②	①		0	2	4	mV/°C

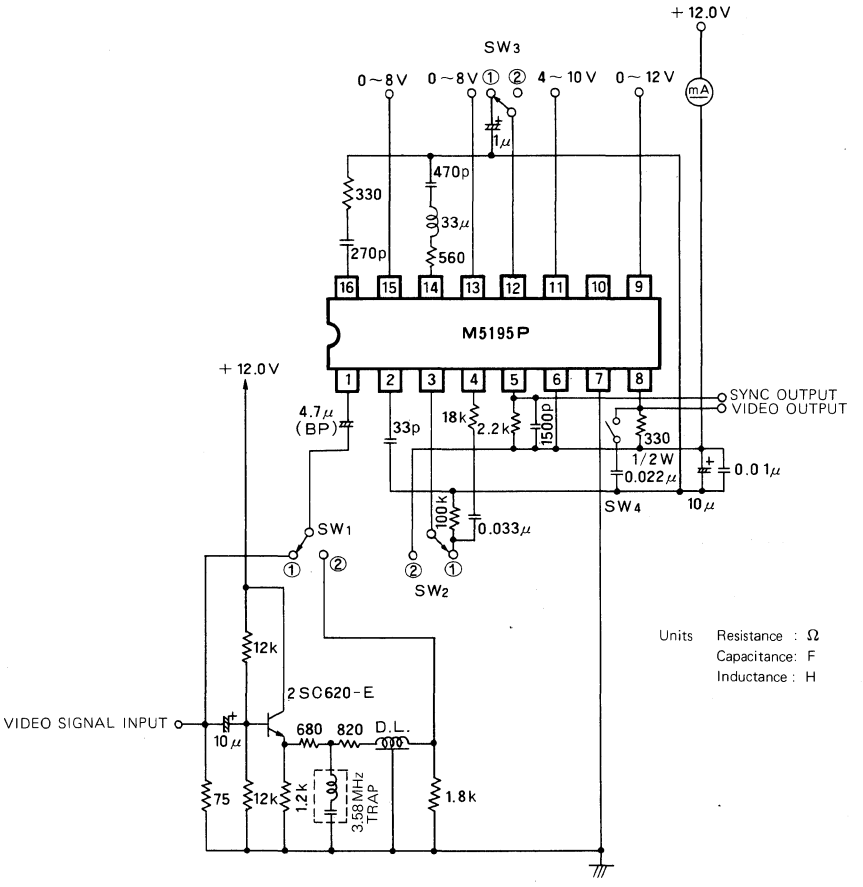
(Note) Video signals

	Contents
I	100mVp-p, 100kHz sine wave
II	1.5Vp-p, 100kHz sine wave
III	Reference sync signal [Note (1)]
Ⅳ	APL 100% reference signal [Note (2)]
Ⅴ	100mVp-p, 4.0MHz sine wave
Ⅵ	100mVp-p, 2.0MHz sine wave
Ⅶ	APL 50% reference signal [Note (3)]
Ⅷ	Pulse (0.2μs) overlayed sync signal [Note (4)]





TEST CIRCUIT



TEST METHODS

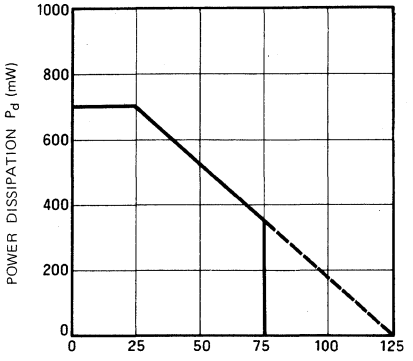
Symbol	Method
I_{CC1}	
I_{CC2}	Pin ⑨ = 12.0V
Vomax	Pin ⑬ = 8.0V
Gvmax	Pin ⑬ = 8.0V
Vplim	DC voltage of pin ⑧ scanning interval when pin ⑨ = 5.0V; SW_4 is set to ON
V_{BLK}	Pin ⑨ voltage when pin ⑧ voltage varies suddenly with pin ⑨ voltage varied from 4.0V to 5.0V
f_B	Output ratio is expressed in decibels at pin ⑧ with signals I and V
Gpmax	Output ratio is expressed in decibels at pin ⑧ with signals I and VI and pin ⑮ = 8.0V
V_{NC}	Difference between sync pulse and noise pulse peaks when noise canceler starts operating is read out at pin ①
W_S	Output pulse width at pin ⑤
V_{DS}	Output pulse width at pin ⑤
δV_{ODC} δTa	Temperature dependency of pin ⑧ DC voltage

Note (1) Unless otherwise noted, pin ⑨ = 0V, pin ⑪ = 7.0V, pin ⑬ = 6.0V and pin ⑮ = 0V

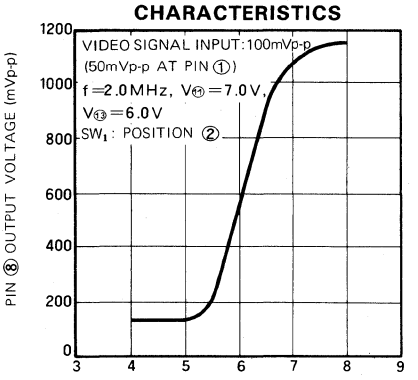
(2) Set pin ⑫ DC voltage so that DC voltage of pin ⑧ scanning interval is 6V when SW_3 = ②

TYPICAL CHARACTERISTICS (T_a = 25°C, V_{CC} = 12.0V, unless otherwise noted)

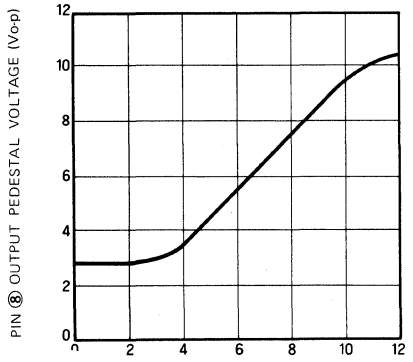
THERMAL DERATING (MAXIMUM RATING)



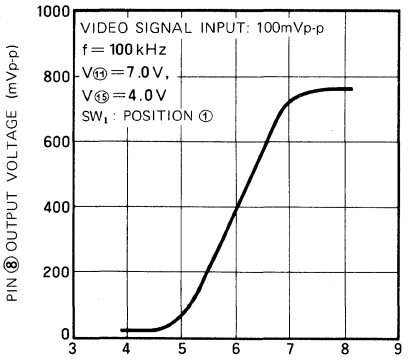
VIDEO TONE CONTROL CHARACTERISTICS



BRIGHTNESS CONTROL CHARACTERISTICS



CONTRAST CONTROL CHARACTERISTICS



M5196P

SECAM CHROMA SYSTEM

DESCRIPTION

The M5196P is a semiconductor integrated circuit designed for use as an SECAM system color TV color signal processing and demodulation circuit. It consists of a limiter amplifier, SECAM switch, discriminator (ident, B-Y, R-Y), color killer, saturation controller, and matrix circuit.

FEATURES

- Horizontal/vertical ident
- Built-in ident error correction
- High-gain limiter amplifier
- Low crosstalk

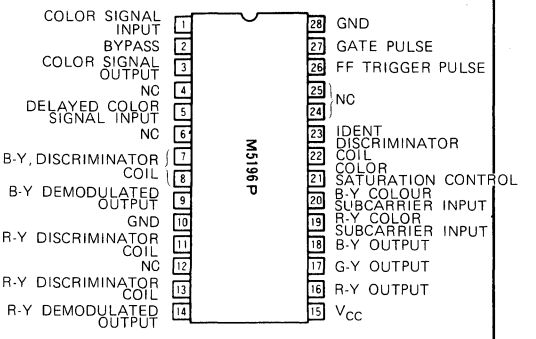
APPLICATION

SECAM system CTV, color signal processing circuit

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... 11 ~ 13V
Rated supply voltage 12V

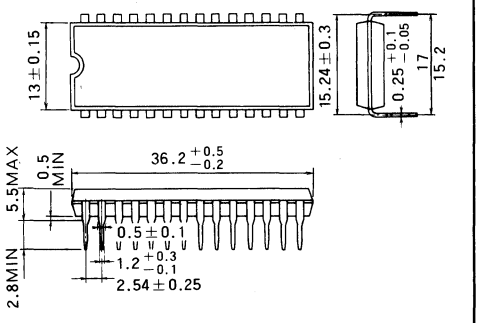
PIN CONFIGURATION (TOP VIEW)



NC: NO CONNECTION

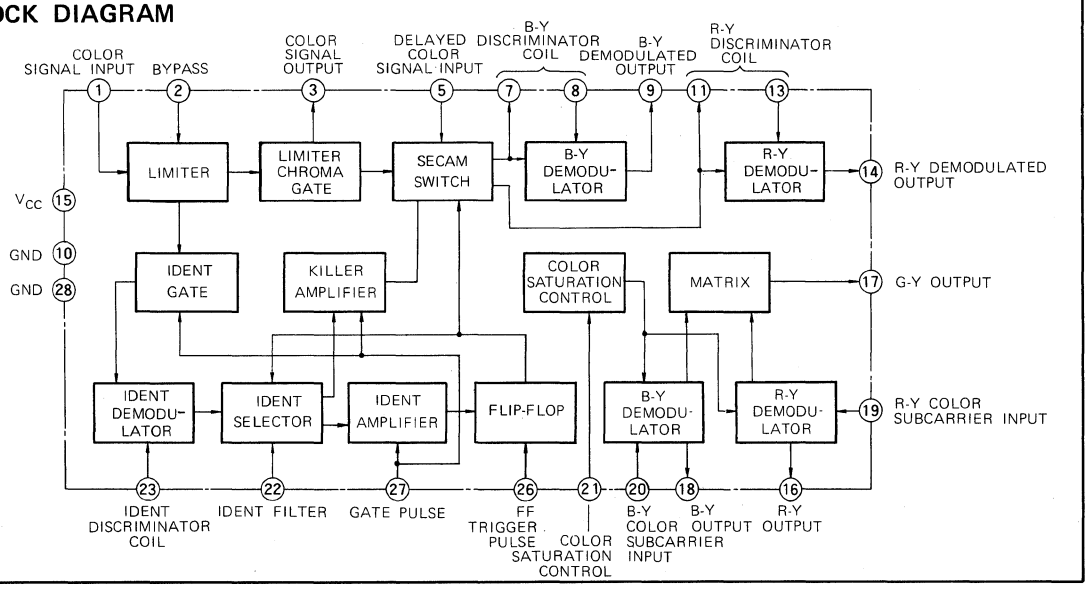
PACKAGE OUTLINE

Dimension in mm



28-pin plastic DIL package

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta=25℃, unless otherwise noted)

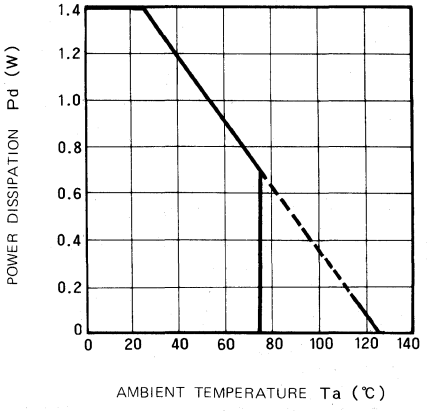
Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		16	V
Pd	Power dissipation		1.4	W
K_θ	Derating		14	mW/℃
Topr	Operating temperature		−20～+75	℃
Tstg	Storage temperature		−40～+125	℃

ELECTRICAL CHARACTERISTICS (Ta=25℃, V_{CC}=12V)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CCO}	Quiescent circuit current		43	55	67	mA
G_L	Limiter voltage gain	−3dB lowered	16	22	30	dB
G_{SW}	SECAM SW limiter voltage gain	−3dB lowered	10	18	26	dB
$V_{i(K)}$	Killer operating input level		−66	−58	−50	dB
Rc	Color signal voltage gain control range	$V_{⑳}$=2～4V	26			dB
AMR	AM rejection ratio			−30	−25	dB
$E_{O(R-Y)}/E_{O(B-Y)}$	Demodulated output voltage ratio			0.79		
$E_{O(G-Y)}/E_{O(B-Y)}$				0.47		
$E_{Omax(B-Y)}$	Maximum demodulated output voltage		4	5	6	V_{P-P}
$E_{Omax(R-Y)}$			3	4	5	V_{P-P}
$E_{Omax(G-Y)}$			2	2.5	3	V_{P-P}
Vcr	Overall crosstalk		0	30	60	mV_{P-P}

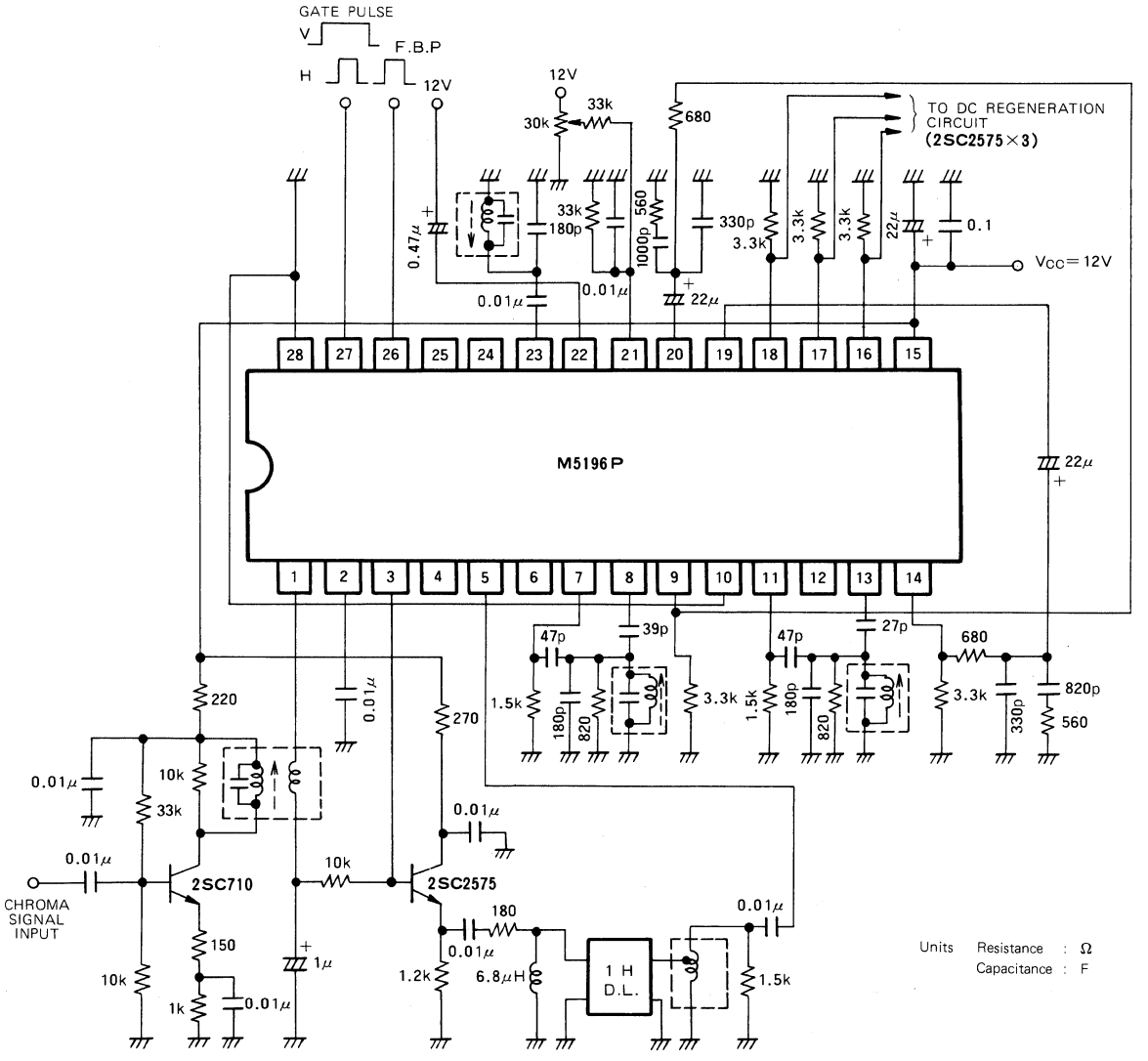
TYPICAL CHARACTERISTICS

THERMAL DERATING (MAXIMUM RATING)



APPLICATION EXAMPLE

SECAM system Color TV, color signal processing circuit



DIGITAL ICs for VIDEO SYSTEMS

3

M50110XP, M50115XP

30～120-FUNCTION REMOTE-CONTROL TRANSMITTERS

DESCRIPTION

The M50110XP and M50115XP are remote-control transmitter circuits manufactured by aluminum-gate CMOS technology for use in television receivers, audio equipment and other devices using infrared for transmission. The M50110-XP conveys 30 different commands on the basis of a 10-bit PCM code, while the M50115XP conveys 120 different commands. These transmitters are intended to be used in conjunction with an M50111XP, M50116XP or M50117-XP receiver. The X in each type corresponds to blank, A, B or C, which are respectively used for audio equipment, TV and VTR, air conditioners and other applications, or video-disk equipment.

FEATURES

Type	Remote-control function
M50110XP	30
M50115XP	120

- Single power supply
- Wide supply voltage range: 2.2V~8V
- Low power dissipation:
  Idle state (V_{DD}=3V): 3mW (typ)
  3μW (max)
- Has many functions and various uses
- Low-cost LC or ceramic oscillator used for reference frequency
- Low external component count
- Low transmitter duty cycle for minimal power consumption
- High-speed transmission

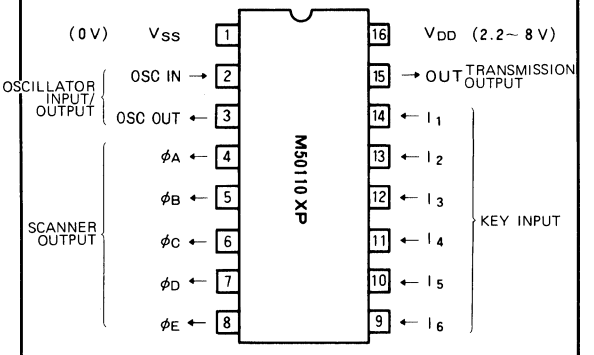
APPLICATION

- Remote-control transmitter for audio equipment, TV, VTR, air conditioners and video-disk equipment

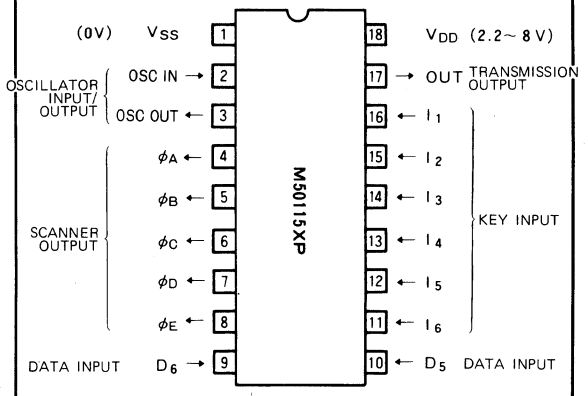
FUNCTION

The M50110XP and M50115XP transmitter circuits for infrared remote-control systems consist of an oscillator, a timing generator, a scanner, a key-in encoder, an instruction decoder, a code modulator and an output buffer. In M50110XP with a 6x5 keyboard matrix 30 commands can be transmitted by 10-bit PCM codes. In M50115XP, with a 6x5 keyboard matrix and two data inputs 120 commands can be transmitted. Oscillation is stopped when none of the keys are depressed in order to minimize power consumption.

PIN CONFIGURATIONS (TOP VIEW)



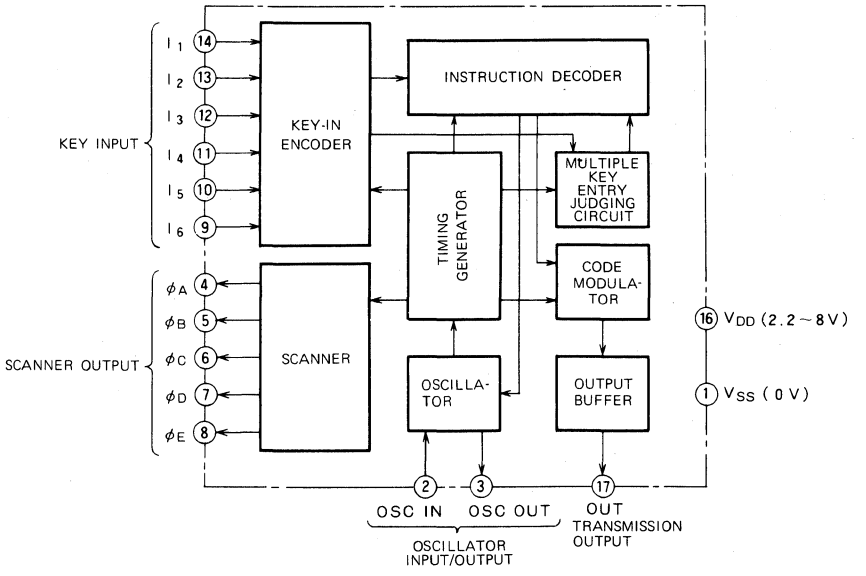
Outline 16P4



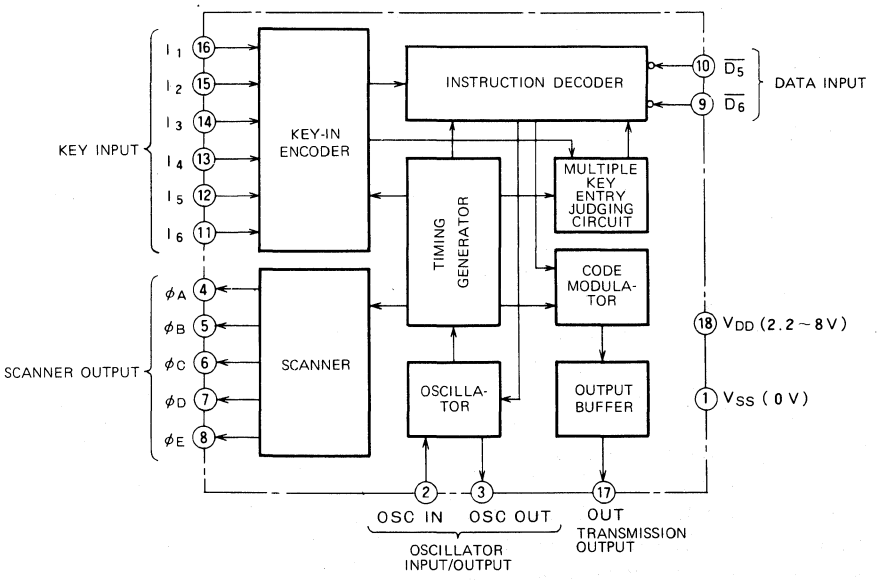
Outline 18P4

BLOCK DIAGRAM

M50110XP



M50115XP



FUNCTION

Oscillator

As the oscillator is on chip, oscillation frequency is easily obtained by connecting an external LC network or ceramic resonator between the OSC IN and OSC OUT terminals. Fig. 1 and Fig. 2 show examples of typical oscillation circuits.

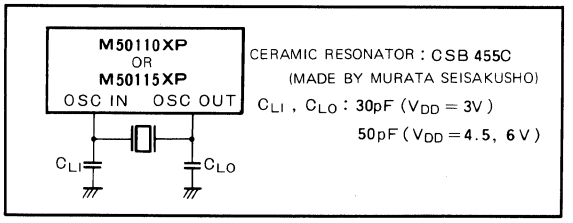


Fig. 1 An example of an oscillator (using a ceramic resonator)

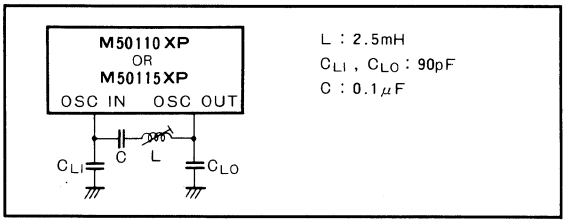


Fig. 2 An example of an oscillator (using an LC network)

Setting the oscillation frequency to 480kHz (or 455kHz) will also set the signal transmission carrier wave to 400kHz (or 38kHz).

Power consumption is minimized by stopping oscillation in the oscillator when none of the keys is depressed.

Key input and data input

In the M50110XP, 30 different commands can be sent through a 6x5 keyboard matrix, consisting of inputs I_1～I_6 and scanner outputs I_A～I_E. In the M50115XP, 120 different commands can be sent because two data inputs, $\overline{D_5}$ and $\overline{D_6}$, are also used.

Table 2 shows the relationship between the keyboard matrix and the transmission code.

Table 1 Key code, type number and use

Key code			Type number	Use
K_0	K_1	K_2		
0	0	0	M50110P M50115P	Remote control for audio equipment
1	0	0	M50110AP M50115AP	Remote control for TV and VTR
0	1	0	M50110BP M50115BP	Remote control for air conditioners and other application
0	0	1	M50110CP M50115CP	Remote control for video-disk equipment

Table 2 Relation between the keyboard matrix and the transmission code names

	ϕ_A	ϕ_B	ϕ_C	ϕ_D	ϕ_E
I_6	A－1	A－2	A－3	A－4	A－5
I_5	A－6	A－7	A－8	A－9	A－10
I_4	A－11	A－12	A－13	A－14	A－15
I_3	B－0	B－1	B－2	B－3	B－4
I_2	B－5	B－6	B－7	B－8	B－9
I_1	B－10	B－11	B－12	B－13	B－14

Table 3 Relation between the transmission code names and the transmission codes

Transmission code name	Transmission				
	D_0	D_1	D_2	D_3	D_4
A－1	1	0	0	0	0
A－2	0	1	0	0	0
A－3	1	1	0	0	0
A－4	0	0	1	0	0
A－5	1	0	1	0	0
A－6	0	1	1	0	0
A－7	1	1	1	0	0
A－8	0	0	0	1	0
A－9	1	0	0	1	0
A－10	0	1	0	1	0
A－11	1	1	0	1	0
A－12	0	0	1	1	0
A－13	1	0	1	1	0
A－14	0	1	1	1	0
A－15	1	1	1	1	0
B－0	0	0	0	0	1
B－1	1	0	0	0	1
B－2	0	1	0	0	1
B－3	1	1	0	0	1
B－4	0	0	1	0	1
B－5	1	0	1	0	1
B－6	0	1	1	0	1
B－7	1	1	1	0	1
B－8	0	0	0	1	1
B－9	1	0	0	1	1
B－10	0	1	0	1	1
B－11	1	1	0	1	1
B－12	0	0	1	1	1
B－13	1	0	1	1	1
B－14	0	1	1	1	1

Transmission Commands

In the M50110XP, 30 commands can be transmitted by 10-bit PCM codes (K_0~K_2, D_0~D_6), and in the M50115XP, 120 commands can be transmitted. The first three bits K_0~K_2, which are key codes between transmitters and receivers, correspond to type numbers and uses. Relation between key codes, type numbers and uses of remote control systems is shown in Table 1.

The next five bits D_0~D_4 correspond to the 6x5 keyboard matrix. Relation between transmission codes and their name is shown in Table 2.

The last two bits, D_5 and D_6, are controlled by the data inputs D_5 and D_6. When terminal D_5 or D_6 is open or high level, data code D_5 or D_6 becomes "0", and when terminal D_5 or D_6 is low level, code data D_5 or D_6 becomes "1".

In the M50110XP, the data bits D_5 and D_6 are fixed in "0." To prevent spurious operation, the codes are designed so that there is no transmission code whose data bits D_0~D_6 are all "0" or "1."

Transmission Coding

When oscillation frequency f_{osc} is 480kHz, transmission of data code is executed as follows: when f_{osc} is other than 480kHz, the period is multiplied by 480kHz/f_{osc} and its frequency by f_{osc}/480kHz.

A single pulse is amplitude-modulated by a carrier of 40kHz, and the pulse width is 0.25ms. Therefore a single pulse consists of 10 clock pulses of 40kHz (see Fig. 3).

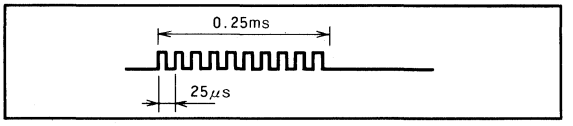


Fig. 3 A single pulse modulated onto carrier (40kHz)

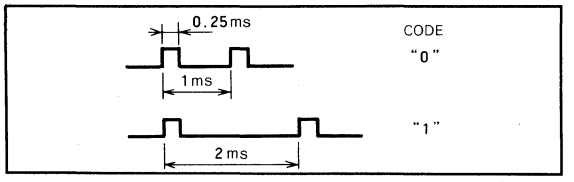


Fig. 4 Distinction between the bits "1" and "0"

The distinction between "0" and "1" bits is made by the pulse interval between two pulses, with an 1ms interval corresponding to "0", and a 2ms interval representing "1" (see Fig. 4).

One command word is composed of 10 bits, that is, of 11 pulses, and it is transmitted in the 24ms cycle while a matrix switch is depressed (see Fig. 5).

As mentioned above, adopting of this code means that the period during which output is high level (i.e. signal emitting LED is lit) is shorter than in continuous wave transmission. Indeed the LED is on for only half of the 11-pulse period or 1.375ms, which is 5.7% of the 24ms entire cycle. This not only saves in total power consumption, but it also improves LED reliability. That is to say, emission can be increased on the same power consumption.

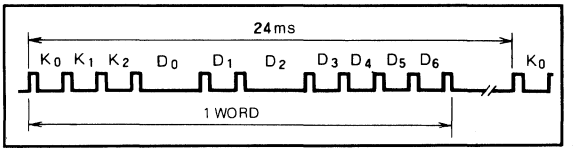


Fig. 5 Synthesis of one word (the code below shows 0001010000)

MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{DD}	Supply voltage	With respect to GND	−0.3～9	V
V_I	Input voltage		$V_{SS} \leqq V_I \leqq V_{DD}$	V
V_O	Output voltage		$V_{SS} \leqq V_O \leqq V_{DD}$	V
Pd	Maximum power dissipation	Ta＝25°C	300	mW
Topr	Operating free-air temperature range		−30～70	°C
Tstg	Storage temperature range		−40～125	°C

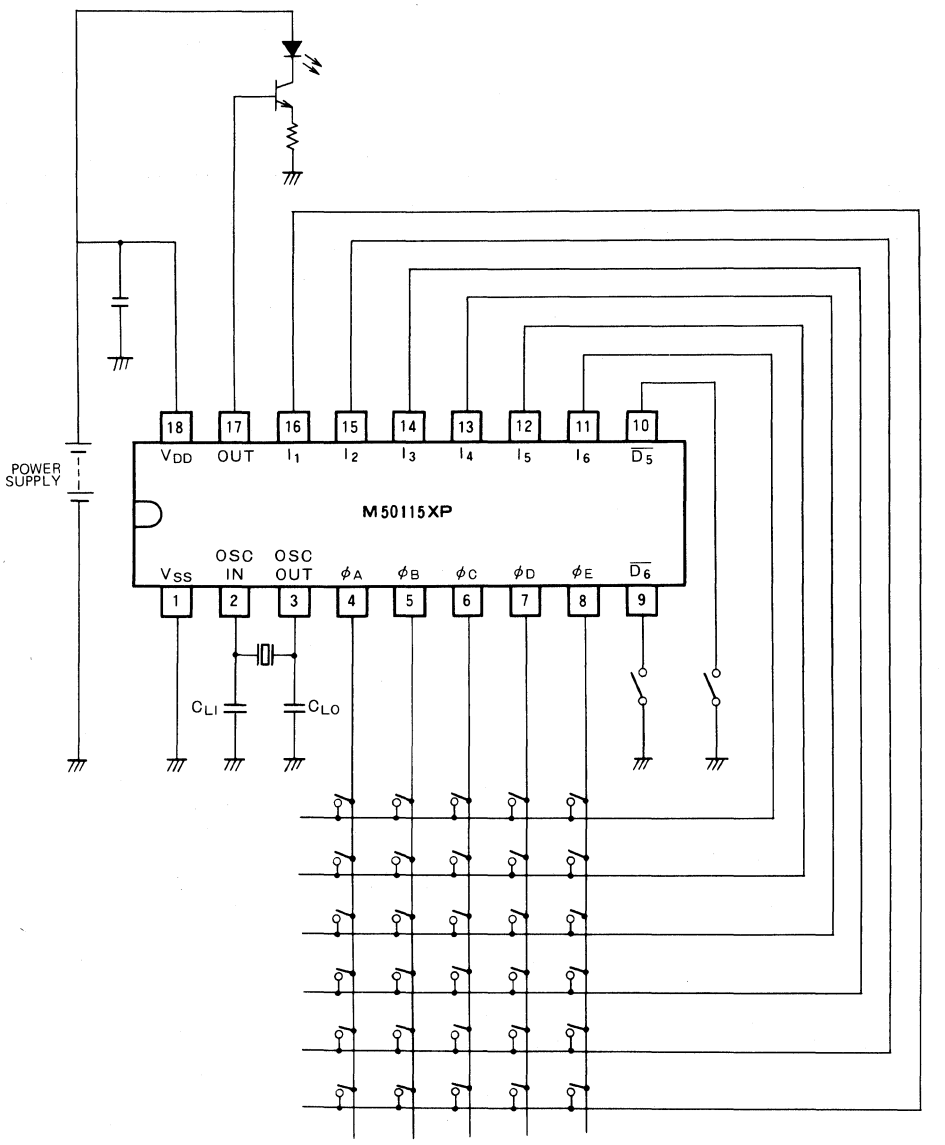
RECOMMENDED OPERATING CONDITIONS (Ta＝−30～70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{DD}	Supply voltage	2.2		8	V
V_{IH}	High-level input voltage	$0.7 \times V_{DD}$		V_{DD}	V
V_{IL}	Low-level input voltage	0		$0.3 \times V_{DD}$	V
f_{OSC}	Oscillation frequency		455		kHz
			480		kHz

ELECTRICAL CHARACTERISTICS (Ta＝25°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
V_{DD}	Operational supply voltage	Ta＝−30～70°C, f_{OSC}＝455kHz		2.2		8	V
I_{DD}	Supply voltage during operation	f_{OSC}＝455kHz	V_{DD}＝3V		0.1	0.5	mA
			V_{DD}＝6V		0.5	2	mA
I_{DD}	Supply voltage during non-operation	V_{DD}＝3V				1	μA
		V_{DD}＝8V				5	μA
R_I	Pull-up resistances, I_1～I_6				20		kΩ
I_{OL}	Low-level output currents, ϕ_A～ϕ_E	V_{DD}＝3V, V_{OL}＝0.9V		0.18	0.6		mA
		V_{DD}＝6V, V_{OL}＝1.8V		0.7	3		mA
I_{OH}	High-level output current, OUT	V_{DD}＝3V, V_{OH}＝2V		−2	−5		mA
		V_{DD}＝6V, V_{OH}＝4V		−8	−16		mA

APPLICATION EXAMPLE (M50115XP)



M50111XP, M50116XP, M50117XP

30~120-FUNCTION REMOTE-CONTROL RECEIVER

DESCRIPTION

The M50111XP, M50116XP and M50117XP are remote control receiver circuits manufactured by aluminum-gate CMOS technology for use in television receivers, audio equipment and other applications using infrared transmission. The systems can receive 30~120 different 10-bit PCM code commands by remote control.

The M50111XP, M50116XP and M50117XP are designed for use with an M50110XP or M50115XP transmitter. The X in each type number corresponds to blank, A, B or C, which are respectively used for audio equipment, TV and VTR, air conditioner and other applications, or video-disk equipment.

FEATURES

Type	Remote-control function		Parallel outputs
	Serial data	Parallel data	
M50111XP	120	30	D_0~D_3, $\overline{STA}$, $\overline{STB}$
M50116XP	120	60	D_0~D_3, $\overline{STA}$~$\overline{STD}$
M50117XP	120	120	D_0~D_7, FF

- Single power supply
- Wide power supply voltage range: 4.5V~8V
- Low power dissipation
- Low-cost LC or ceramic oscillator used for frequency reference
- Information is transmitted by pulse code modulation
- High speed reception
- Superior noise immunity — instructions are not executed unless the same code is received two or more times in succession
- Single transmission frequency (40kHz or 38kHz) for carrier wave
- Many functions and various uses
- Large tolerance in operating frequency between the transmitter and the receiver
- Can be simply connected to a microcomputer

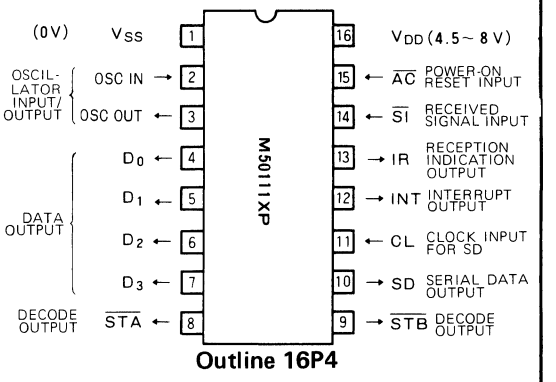
APPLICATION

- Remote control receivers for audio equipment, TV, VTR, air conditioners, video-disk equipment and similar devices

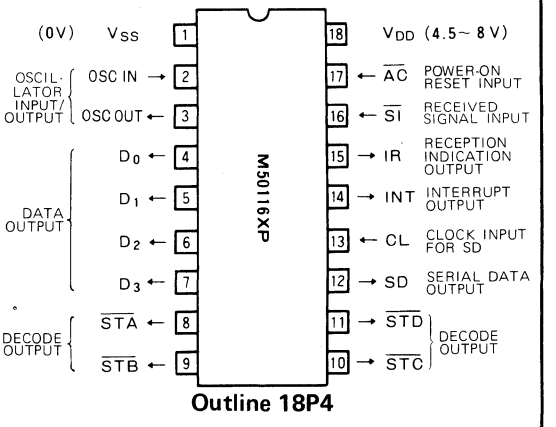
FUNCTION

The M50111XP, M50116XP and M50117XP receivers for infrared remote control systems consist of an oscillator, a timing generator, a demodulator, an error prevention circuit, a reception state decision circuit, a serial data processor, a shift register, a received signal input circuit, power-on reset circuit and other circuits. The M50111XP, M50116XP and M50117XP are designed to decode and execute instructions after 2 successive receptions of the identical instruction code. This provides positive assurance that noise will not be executed as instructions.

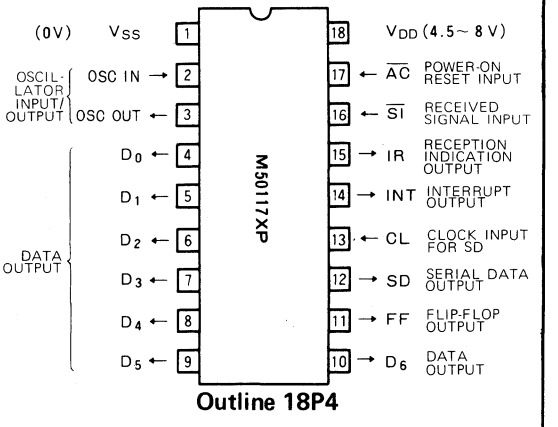
PIN CONFIGURATIONS (TOP VIEW)



Outline 16P4



Outline 18P4



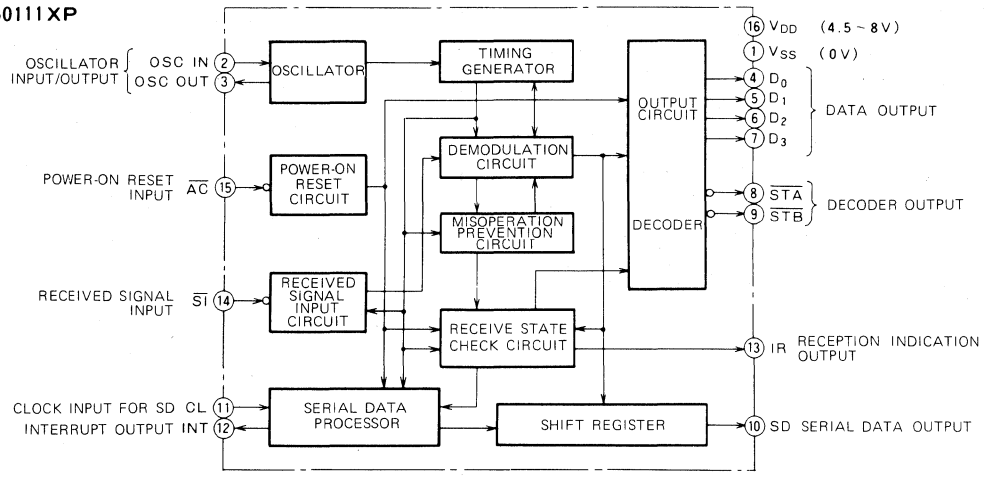
Outline 18P4

With the data outputs D_0~D_6 and the decode outputs $\overline{STA}$~$\overline{STD}$, M50111XP can process 30 different instructions, the M50116XP can process 60 different instructions and the M50117XP can process 120 different instructions. With a serial data output SD, 120 different instructions can be processed by any of the receivers.

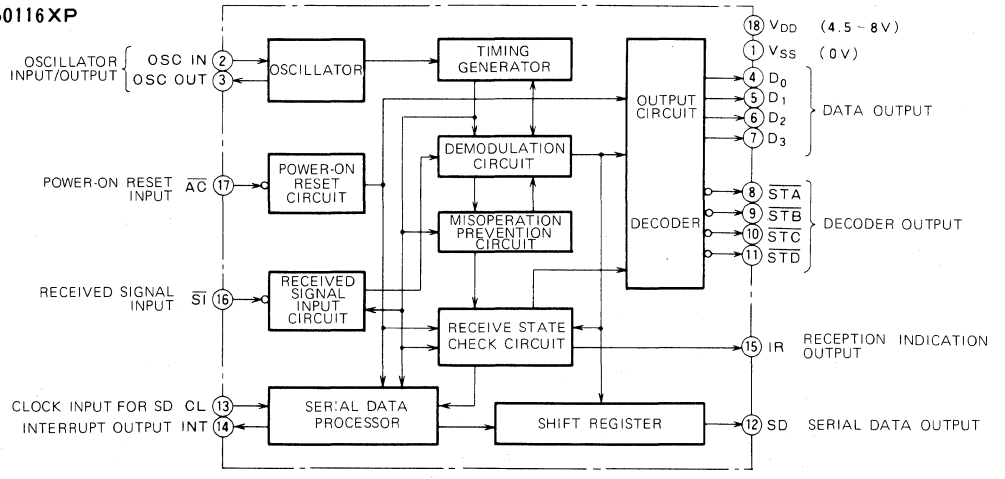
30~120-FUNCTION REMOTE-CONTROL RECEIVER

BLOCK DIAGRAM

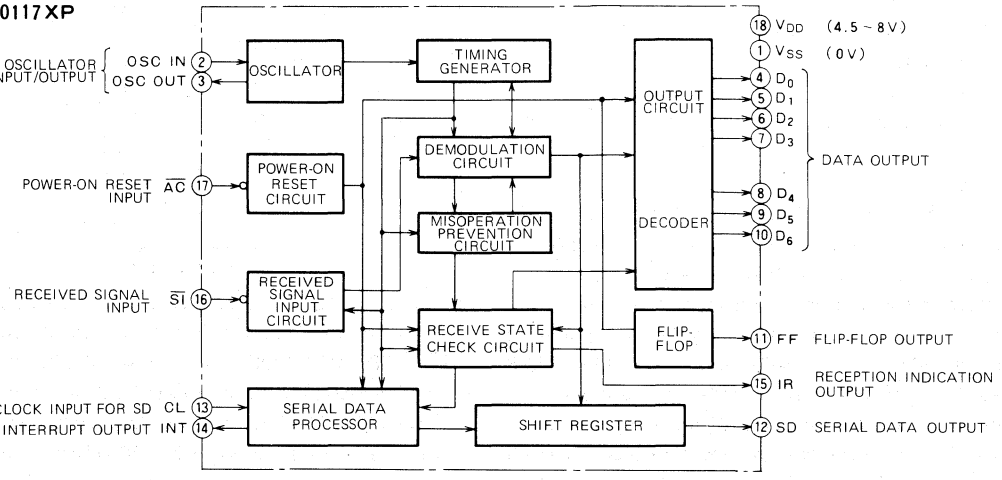
M50111XP



M50116XP



M50117XP



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FUNCTION

Oscillator

As the oscillator is on chip, oscillation frequency is easily obtained by connecting an external LC network or ceramic resonator between the OSC IN and OSC OUT terminals. Fig. 1 and Fig. 2 show examples of typical oscillation circuit.

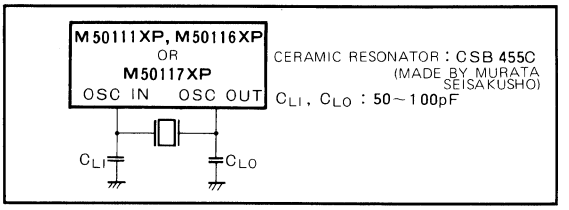


Fig. 1 An example of an oscillator (using a ceramic resonator)

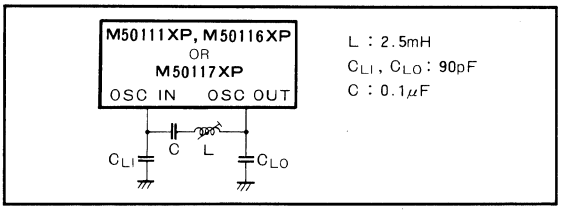


Fig. 2 An example of an oscillator (using an LC network)

When oscillation frequency f_{osc} is 480kHz, execution is as follows:

Received Signal Input Circuit and Demodulation Circuit

The received signal, sensed by the photo detector, is amplified and an integrated signal is supplied through $\overline{SI}$ to be processed by the received signal input circuit, and then it is sent to the demodulation circuit. In the demodulation circuit, the pulse interval of the signal is analyzed and then converted to a digital code. Fig. 3 shows the relationship between the $\overline{SI}$ input wave form, codes and data.

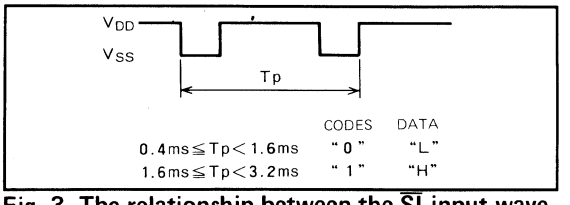


Fig. 3 The relationship between the $\overline{SI}$ input wave form, code and data

When the input pulse interval to the $\overline{SI}$ input is 3.2 ms or longer, it will be assumed to be the end of a word, but if the interval is finally 50 ms or longer it will be accepted as the end of the command transmission and the device will be put in the idle state. In the idle state, the data outputs D_0～D_6 and the reception indication output IR goes to low-level and the decoder outputs $\overline{STA}$～$\overline{STD}$ go to high-level.

Misoperation Prevention Circuit

Any signal whose low-level interval at $\overline{SI}$ input is less than 50～100 μs is not accepted as a transmission signal.

When a pulse interval T_p is less than 0.4 ms, the misoperation prevention circuit resets to idle state to prevent an error. When all data codes D_0～D_4 are supplied as 0 or 1, it resets to idle state.

Receive State Check Circuit

The reception indication output IR becomes high-level after receiving the same transmission code 2 or more times in succession. Therefore reception states of an instruction from the transmitter can be indicated by an LED connected to the output IR.

Reception Code, Data Output, Decode Output and Flip-flop Output

Data outputs D_0～D_6 correspond to D_0～D_6 of the transmission codes. When a code is 0, the data output will be low-level, and when a code is 1, the data output will be high-level, while decode outputs $\overline{STA}$～$\overline{STD}$ correspond to transmission codes D_4, D_5 as shown in Table 1. When the transmission codes D_0～D_6 are 1010000, the flip-flop output FF will go to high-level, and when the codes are 0101000, the output FF will go to low-level.

Table 2 shows the relationship between key codes and type numbers, and examples of their use.

Table 1 The relationship between the decode outputs and the transmission codes D_4, D_5

Transmission code		Decode output			
D_4	D_5	$\overline{STA}$	$\overline{STB}$	$\overline{STC}$	$\overline{STD}$
0	0	L	H	H	H
1	0	H	L	H	H
0	1	H	H	L	H
1	1	H	H	H	L

Table 2 The relationship between be key codes, types numbers examples of their use

Key code			Type number	Use
K_0	K_1	K_2		
0	0	0	M50111P M50116P M50117P	Remote control for audio equipment
1	0	0	M50111AP M50116AP M50117AP	Remote control for TV, VTR
0	1	0	M50111BP M50116BP M50117BP	Remote control for air conditioners and others
0	0	1	M50111CP M50116CP M50117CP	Remote control for video-disk equipment

Serial Data Processor

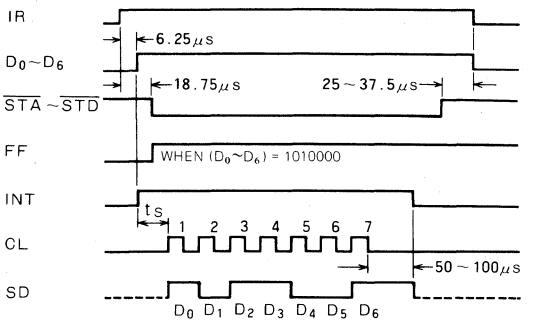
When an identical code is received twice, the reception indication output IR is turned from low-level to high-level and then after 6.25μs delay the interrupt output INT is turned from low-level to high-level (see the timing diagram). When pulses are supplied to the clock input CL for SD while the INT output is high-level, the received data are sent from the serial data output SD. These data are synchronized with the rising edge of the CL input pulses. Thus the contents of the transmission code can be read, if the SD output is decided at the falling edge of the CL input pulses.

The SD output is a three-state output, which is usually in the disabled state (high impedance). After an interrupt output INT goes to high-level, the disabled state is absolved at the first low-to-high transmission of a CL input pulses. And then the data D_0~D_6 is serially sent, and after 50~100μs from the seventh high-to-low transmission of CL input pulses, the SD output is again put in the disabled state and at the same time the INT output goes to low-level.

Power-on Reset Circuit

Attaching a capacitor to the terminal $\overline{AC}$, the power-on reset function can be activated when power supply is applied to the IC. When the $\overline{AC}$ input is turned to low-level, the data outputs D_0~D_6, the reception indication output IR, the interrupt output INT and the flip-flop output FF go to low-level, the decode outputs $\overline{STA}$~$\overline{STD}$ go to high-level and the serial data output SD is put in disabled state.

Timing Diagram



After the INT output becomes high-level, when the received code is not identical to the previously received code before the first fall of the CL input, the INT output is returned to low-level; at the same time the $\overline{STA}$~$\overline{STD}$ outputs become high level and the SD output become a disabled state. After the INT output goes to high-level, when received codes are not identical after the first fall of the CL input, the data D_0~D_6 are sent and then the INT output goes to low-level after 50~100μs from the seventh fall of CL input pulses and the SD output is put in the disabled state.

The time t_s from the rising edge of the INT output to the rising edge of the CL input must be at least 6.25μs.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{DD}	Supply voltage	With respect to V_{SS}	−0.3～9	V
V_I	Input voltage		$V_{SS} \leqq V_I \leqq V_{DD}$	V
V_O	Output voltage		$V_{SS} \leqq V_O \leqq V_{DD}$	V
Pd	Maximum power dissipation	Ta＝25°C	300	mW
Topr	Operating free-air temperature range		−30～70	°C
Tstg	Storage temperature range		−40～125	°C

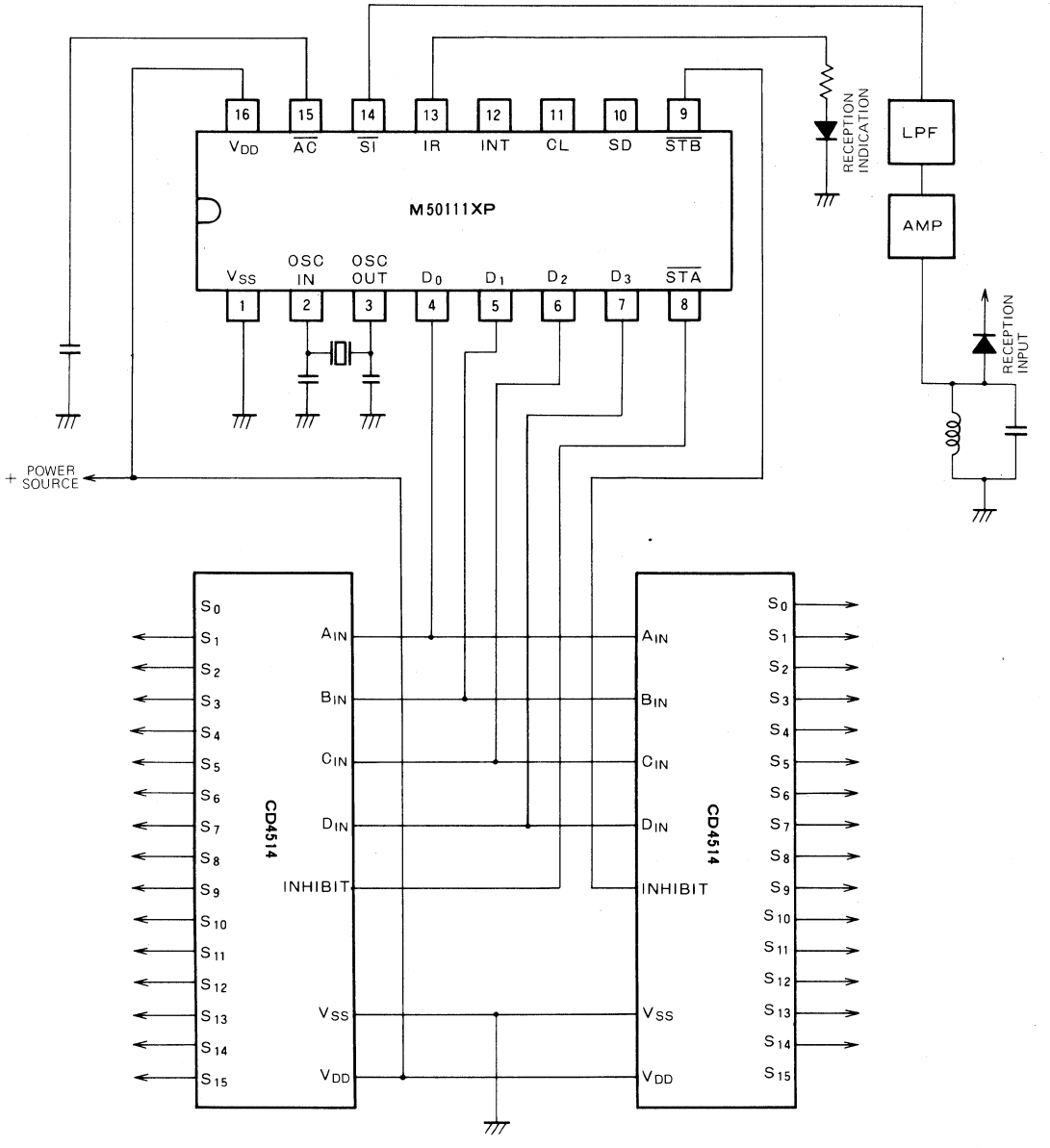
RECOMMENDED OPERATING CONDITIONS (Ta＝−30～70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{DD}	Supply voltage	4.5		8	V
V_{IH}	High-level input voltage	$0.7 \times V_{DD}$		V_{DD}	V
V_{IL}	Low-level input voltage	0		$0.3 \times V_{DD}$	V
f_{OSC}	Oscillation frequency		455		kHz
			480		kHz

ELECTRICAL CHARACTERISTICS (Ta＝25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{DD}	Operational supply voltage	Ta＝−30～70°C, f_{OSC}＝455kHz	4.5		8	V
I_{DD}	Supply current from V_{DD}	V_{DD}＝5V, f_{OSC}＝455kHz		0.3	1.0	mA
I_{OH}	High-level output current, SD	V_{DD}＝4.5V, V_{OH}＝2.4V	−2	−6		mA
I_{OH}	High-level output current, INT, IR	V_{DD}＝4.5V, V_{OH}＝2.4V	−1	−3		mA
I_{OH}	High-level output current, D_0～D_6, $\overline{STA}$～$\overline{STD}$, FF	V_{DD}＝4.5V, V_{OH}＝2.4V	−0.5	−1.5		mA
I_{OL}	Low-level output current, D_0～D_6, $\overline{STA}$～$\overline{STD}$, FF, SD, INT, IR	V_{DD}＝4.5V, V_{OL}＝0.4V	1.6	3.2		mA
R_I	Pull-up resistance, $\overline{SI}$			20		kΩ
R_I	Pull-up resistance, $\overline{AC}$			48		kΩ
R_I	Pull-down resistance, CL			63		kΩ

APPLICATION EXAMPLE (M50111XP)



MITSUBISHI ELECTRIC

VOLTAGE SYNTHESIZER

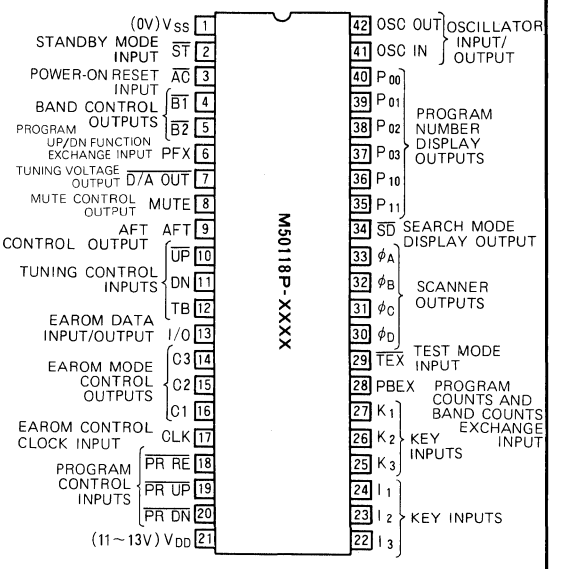
DESCRIPTION

The M50118P is a voltage synthesizer circuit manufactured by aluminum-gate CMOS technology. It has a fully automatic search function of storing in an EAROM the tuning voltages corresponding to all suitable stations with only one key depressed, a sequentially automatic up/down search function of presetting of any arbitary station. It can be used in conjunction with the M5G1400P EAROM to obtain a completely electronic tuning sytem for TVs, VTRs and so on.

FEATURES

- Fully automatic search and sequentially automatic up/down search
- 12 programs selected directly with one key depressed
- 30 programs selected directly with two keys depressed or sequentially
- 30 programs selected directly or sequentially from a remote control receiver IC (for example, M50120P)
- Exchange function of program counts: 30, 20, 12 or 10 programs
- Exchange function of band counts: Band 1 ~ Band 3, Band 1 ~ Band 4 or Band 3
- AFT on/off and Mute on/off memory for each program
- Program number outputs with BCD code

PIN CONFIGURATION (TOP VIEW)

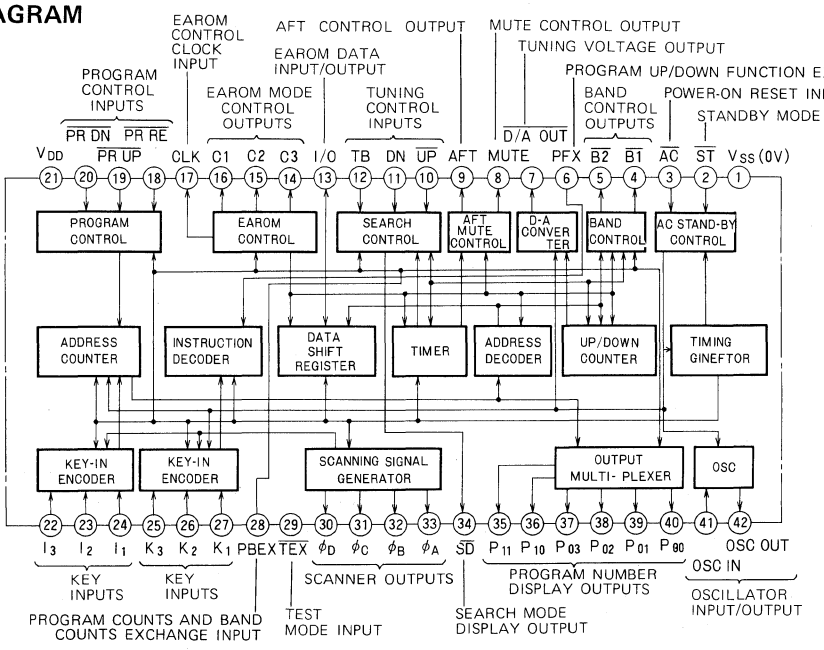


Outline 42P1

APPLICATIONS

Electronic tuning systems for TVs, VTRs and other devices requiring similar program selection functions.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{DD}	Supply voltage		−0.3～+15.0	V
V_I	Input voltage		$V_{SS} \leqq V_I \leqq V_{DD}$	—
V_O	Output voltage		$V_{SS} \leqq V_I \leqq V_{DD}$	—
Topr	Operating free-air ambient temperature range		−30～+70	°C
Tstg	Storage temperature range		−40～+125	°C
Pd	Maximum power dissipation		300	mV

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{DD}	Supply voltage	11	12	13	V
f_{OSC}	Oscillator frequency		1.8		MHz
V_{IH}	High-level input voltage	$V_{DD}-3V$		V_{DD}	—
V_{IL}	Low-level input voltage	V_{SS}		$V_{SS}+3V$	—

ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{DD}=12V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{DD}	Supply voltage	Ta=−30～+70°C, f_{OSC}=1.8MHz	11	12	13	V
I_{DD}	Supply current	f_{OSC}=1.8MHz		2	7	mA
R_I	Pull-up resistance, ($\overline{PR\ RE}$, $\overline{PR\ UP}$, $\overline{PR\ DN}$, $\overline{UP}$, DN, TB, $\overline{TEX}$)			50		kΩ
R_I	Pull-up resistance ($\overline{AC}$)			100		kΩ
R_I	Pull-down resistance, ($\overline{ST}$, PFX, I_1～I_3, K_1～K_3, PBEX)			50		kΩ
I_{OH}	High-level output current ($\overline{B1}$, $\overline{B2}$)	V_O=10V	2			mA
I_{OL}	Low-level output current ($\overline{B1}$, $\overline{B2}$)	V_O=2V	3			mA
I_{OH}	High-level output current ($\overline{D/A\ OUT}$)	V_O=10V	3			mA
I_{OL}	Low-level output current ($\overline{D/A\ OUT}$)	V_O=2V	5			mA
I_{OH}	High-level output current (AFT, MUTE)	V_O=10V	3			mA
I_{OL}	Low-level output current (AFT, MUTE)	V_O=2V	4			mA
I_{OZH}	Off-state output current (AFT, MUTE)	V_O=12V			1	μA
I_{OZL}		V_O=0V			1	μA
V_{OH}	High-level output voltage (CLK, C1～C3, I/O)	I_O=0.5mA	11			V
V_{OL}	Low-level output voltage (CLK, C1～C3, I/O)	I_O=1mA			2	V
I_{OZH}	Off-state output current (I/O)	V_O=12V			1	μA
I_{OZL}		V_O=0V			1	μA
I_{OH}	High-level output current (ϕ_A～ϕ_D)	V_O=10V	6			mA
I_{OL}	Low-level output current ($\overline{SD}$, P_{00}～P_{11})	V_O=0.4V	1.6			mA
I_{OZH}	Off-state output current ($\overline{SD}$, P_{00}～P_{11})	V_O=10V			1	μA
I_{OL}	Low-level output current ($\overline{SD}$)	V_O=3V	10			mA

FUNCTIONAL DESCRIPTION

The M50118P is a voltage synthesizer IC and consists of a completely electronic tuning system when used in conjunction with the M5G1400P EAROM that is capable of operation without the use of any mechanical components.

The major functions include fully automatic search, sequentially automatic up and down search, direction or sequential selection of up to 30 programs, exchange function of program counts (30, 20, 12 or 10 channels), digital AFT (automatic fine tuning), automatic bandswitching, fine tuning, and AFT on/off and MUTE on/off memory for each program separately, and program number display output with BCD code.

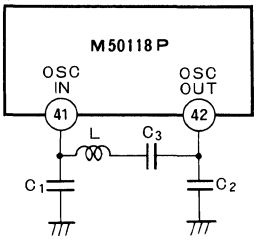
In addition, by using a remote control unit, direct or sequential selection of up to 30 channels is possible.

FUNCTION

(1) Oscillator Circuit

The M50118P includes an CMOS inverter and high-impedence feed-back resistance so that the only components required for external connection to configure the oscillatór circuit consist of the LC circuit of three capacitors and one inductor as shown in Fig. 1.

Fig. 1 Connections of external oscillator components



Examples of component values (for f_{osc}=1.8MHz)

$L = 180\,\mu H$
$C_1 = C_2 = 87\,pF$
$C_3 = 0.1\,\mu F$
($f_{OSC} = 1.8MHz$)

Table 1 Keyboard matrix I

I \ φ	ϕ_A	ϕ_B	ϕ_C	ϕ_D
I_1	Pr 1	Pr 2	Pr 3	Pr 4
I_2	Pr 5	Pr 6	Pr 7	Pr 8
I_3	Pr 9	Pr 10	Pr 11	Pr 0

Table 2 Keyboard matrix II

K \ φ	ϕ_A	ϕ_B	ϕ_C	ϕ_D
K_1	FAS	FT (+)	CLEAR	10—19
K_2	AS (+)	FT (−)	AFT ON	20—29
K_3	AS (−)	PR UP	PR UP	PRL

(2) Keyboard Matrix

The combination of the $\phi_A \sim \phi_D$ scanner outputs and the $I_1 \sim I_3$ and $K_1 \sim K_3$ key inputs form a matrix of 4 x 3, enabling the input of 24 commands.

When two or more keys are pressed simultaneously, neither key input is accepted, the last key being released having effect. Note however that PRL is independent from the other keys and can be input simultaneously with other keys.

Table 1 and 2 show the relationship between the matrix and the corresponding commands.

As shown in Table 1, when program counts are 10 or 12, single action program selection is possible (when the program counts are 10, Pr1 ~ Pr9 and Pr0 are used).

When program counts are 20 or 30, program selection is made using two actions, for which the Pr1 ~ Pr9 and Pr0 of Table 1 are required. For example, if the Pr17 selection is to be made, the 10 — 19 key is first pressed, followed by the Pr7 key. If after the 10 — 19 or 20 — 29 key more than approximately 6.5 seconds elapses before a key in the range Pr0 to Pr9 is pressed, the key input sequence is cancelled.

(3) Program Counts and Band Counts Exchange Input (PBEX)

By inputing the scan outputs $\phi_A \sim \phi_D$ at the PBEX input, selection of program counts and band counts can be achieved. These relationships are summarized in Tables 3 and 4.

Table 3 Channel Number Selection

Program counts \ PBEX	ϕ_A	ϕ_B
30	—	—
20	0	—
12	—	0
10	0	0

Table 4 Bandswitching

Band \ PBEX	ϕ_C	ϕ_D
Band 1 ~ Band 3	—	—
Band 1 ~ Band 4	0	—
Band 3	—	0

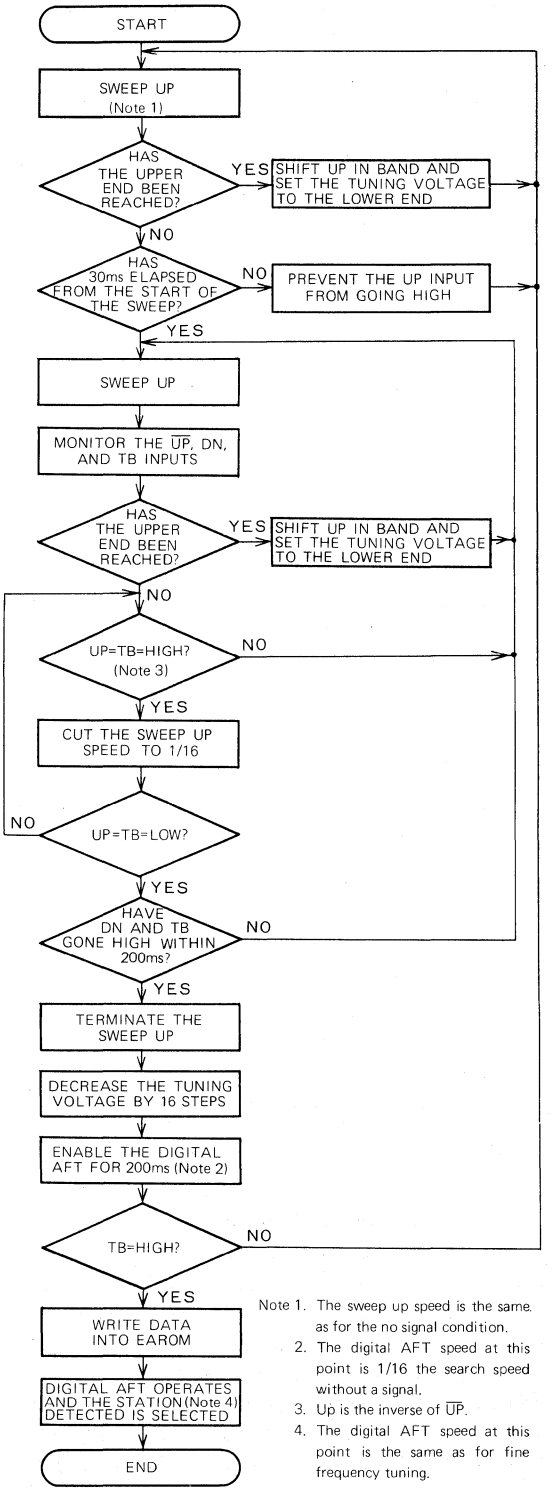
(4) Search

The search functions consist of the sequentially automatic and the fully automatic search functions.

(i) Auto Search

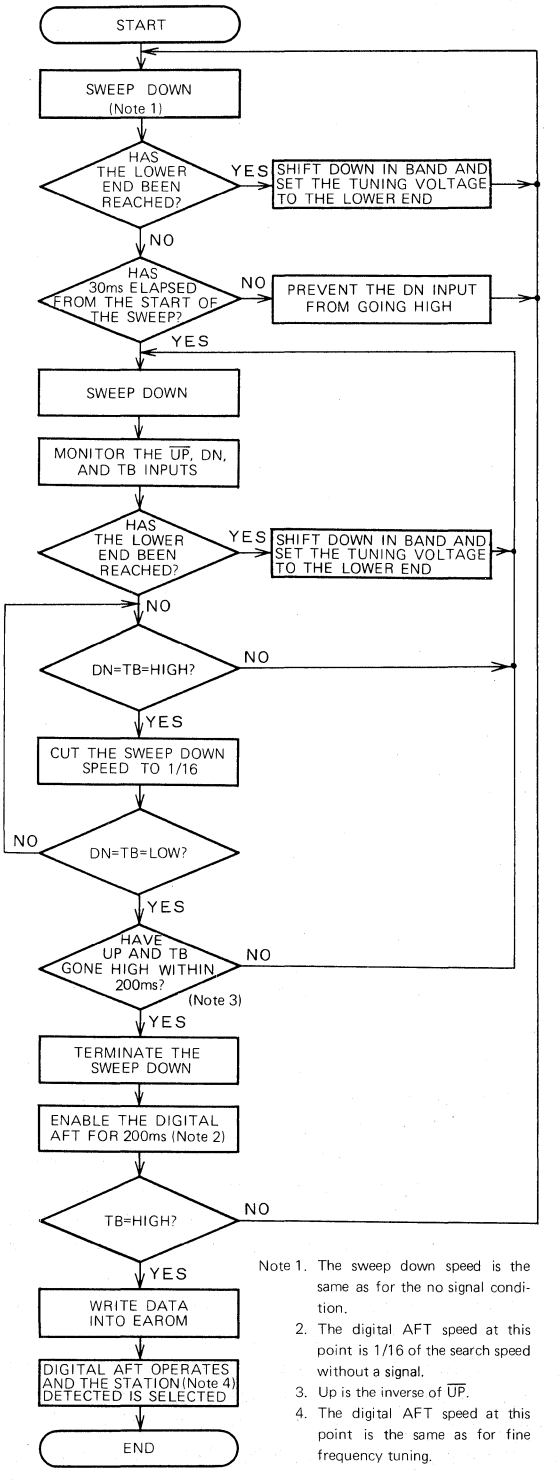
When the AS(+) or AS(−) keys are input, the search mode causes the muting function to be enabled and the sweep up (or down) from the current position. For 30ms after the sweep begins the UP (or DN) input is prevented from going high. After this 30ms has elapsed, the $\overline{UP}$, DN and TB inputs are monitored and when UP = TB = high (or DN = TB = high), the sweep speed is cut to 1/16. When UP and TB (or DN and TB) go from high to low, a timer starts to operate to sense if DN and TB (or UP and TB) go to high within 200ms or not. In this period the sweep speed is 1/16 of the sweep speed without a signal and this is maintained until this sensing of DN and TB (or UP and TB) is completed. If within 200ms DN and TB (or UP and TB) don't change to high, the sweep continues. If they change to high during this period, the sweep is terminated when this state change occurs. The tuning voltage at this point is lowered by 16 steps (approx. 32mV) (for the case of AS(−) this is not done). Next, the digital AFT operates for 200ms. Digital

Fig. 2 Flowchart of sequentially automatic up search (the case when the AS(+) key has been pressed)



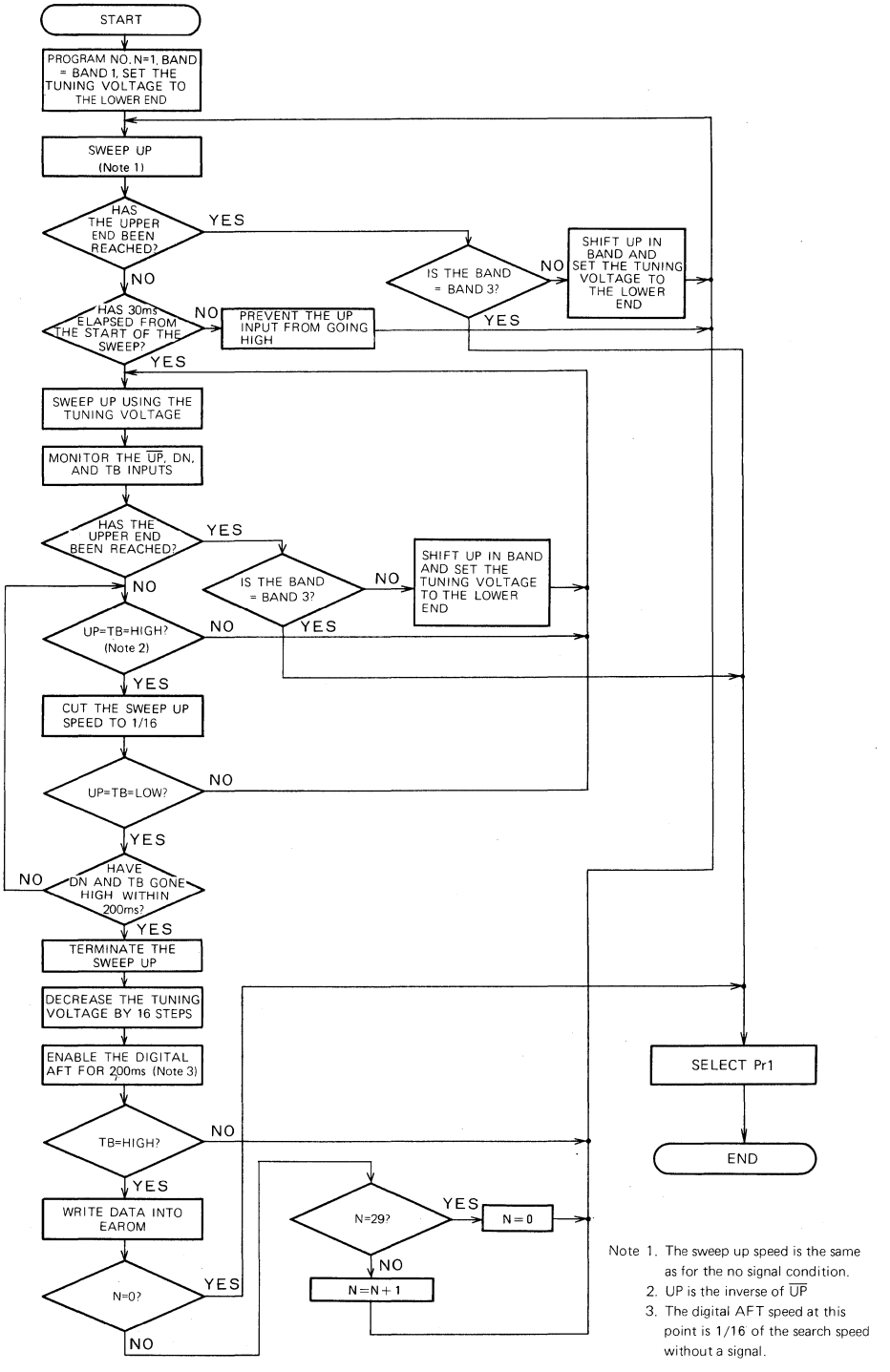
Note 1. The sweep up speed is the same as for the no signal condition.
2. The digital AFT speed at this point is 1/16 the search speed without a signal.
3. Up is the inverse of $\overline{UP}$.
4. The digital AFT speed at this point is the same as for fine frequency tuning.

Fig. 3 Flowchart of sequentially automatic down search (the case when the AS(−) key has been pressed)



Note 1. The sweep down speed is the same as for the no signal condition.
2. The digital AFT speed at this point is 1/16 of the search speed without a signal.
3. Up is the inverse of $\overline{UP}$.
4. The digital AFT speed at this point is the same as for fine frequency tuning.

Fig. 4 Flowchart of fully automatic search
(the case when the FAS key has been pressed, with the program counts 30 and the band between 1 and 4)



AFT is controlled by the $\overline{UP}$ and DN inputs. When the $\overline{UP}$ input is low, the tuning voltage is increased, and when the DN input is high, the tuning voltage is decreased. When 200ms has elapsed, the TB input is sensed. If TB is low at this time, it is judged that a normal station is not being received and the sweep is restarted, the operation from this point being similar to that described above. If the TB input is high, however, a normally received station is judged to have been encountered and the following data is written into the EAROM:

Tuning voltage:	14 bits	18 bits
Band:	2 bits	
AFT on/off:	1 bit	
MUTE on/off:	1 bit	

When the write operation has been completed, the search mode is cancelled and the digital AFT operates, the AFT output going high with the mute mode being cancelled as well. The digital AFT speed at this time is the same as for fine tuning.

In the search mode when the sweep up (or down) reaches the upper (or lower) end of a band, automatic bandswitching is performed and the new tuning voltage output is that of the lower (or upper) end of the new band.

The flowchart for the automatic search operation is shown in Fig. 2 and 3.

Sequentially automatic up (or down) sequencing search operation changes to down (or up) search when the AS(−) (or AS(+)) key is pressed respectively during a sequentially automatic up (or down) search operation.

(ii) Fully Automatic Search

When the FAS key is input, the search mode is enabled and MUTE is turned on. At the same time, the program number 1 is selected and the tuning voltage is set at the lower end of Band 1 (Band 3 if this is the only band). Next, the sweep begins and this operation is the same as the sequentially automatic up search. When a station has been captured, data is written into EAROM, after which the program number is incremented by 1 and the next search is initiated. When in this manner, all program numbers are searched or all bands are exhausted, the search ends with the selection of Pr1.

The sequence of program numbers for searching is shown in Table 5.

Table 5 Full Auto Search Sequence

The number of programs	Search sequence
10	Pr 1 ⟶ Pr 10
12	Pr 1 ⟶ Pr 12
20	Pr 1 ⟶ Pr 19 ⟶ Pr 0
30	Pr 1 ⟶ Pr 29 ⟶ Pr 0

The flowchart for fully automatic search is shown in Fig. 4. During the fully automatic search operation, the Mute control output is at a high level.

For either the fully or sequentially search modes, if a station is selected during the search process the search mode is cancelled. The data written as a result of the search is AFT on and MUTE off.

(iii) Search Speed

The search speed is switched for every band. Table 6 shows the search speeds for each band in the no signal condition.

Table 6 Search Time for Zero-Signal Condition

Band	Search time
Band 1	2.33s
Band 2	4.66s
Band 3, Band 4	9.32s

In the following cases the search speed will be 1/16 of the no signal condition speed:

FAS, AS(+) . . . From the time TB goes high and $\overline{UP}$ goes low until DN goes high.

AS(-) . . . . . From the time TB and DN go high until $\overline{UP}$ goes low.

(iv) Bandswitching in Search Mode

Automatic bandswitching is accomplished in the search modes as shown in Table 7.

Table 7 Bandswitching Sequence for the Search Modes

Band	Bandswitching sequence
Band 1—Band 3	Band 1 ⟷ Band 2 ⟷ Band 3
Band 1—Band 4	Band 1 ⟷ Band 2 ⟷ Band 4 ⟷ Band 3
Band 3	Band 3

(v) Search Mode Display

During execution of the search mode, a 50% duty cycle clock of period 0.3s is available at the search mode display output $\overline{SD}$. By using this output the search mode can be displayed during the search operation.

For modes other than search mode, this output is left floating.

(5) Program Selection

(i) Direct Program Selection Using Key Input

For 10 or 12 programs, direct selection of a program is possible by using only one action. For 20 or 30 programs, 2 key operations are required. Note that the Pr10 and Pr11 keys are when 12 programs.

For two-action program serection, when the 0 — 19 or 20 — 29 key is pressed the lower order digit of the program

number display disappears ($P_{00} \sim P_{03}$ are floating). The upper order digit is 1 and 2 for 10 – 19 and 20 – 29 respectively, and the display is flashing at this point. If a key in the range Pr0 to Pr9 is not pressed within approximately 6.5 seconds, the flashing of the display stops and original program number is restored, the key input for the 10 – 19 or 20 – 29 key being ignored.

(ii) Sequential Selection Using Key Input

The PR UP and PR DN key input functions are switched by the PFX input.

If the PFX input is left open or set to low, these keys cause sequential selection. If, however, the PFX input is high, the program number display changes in sequence but the reading of EAROM data is not executed, the received program remaining unchanged.

(iii) Remote Control Interface

The $\overline{\text{PR RE}}$, $\overline{\text{PR UP}}$, and $\overline{\text{PR DN}}$ inputs are provided with internal pull-up resistors, allowing the direct selection of up to 30 programs from a remote control receiver (e.g., M50120P).

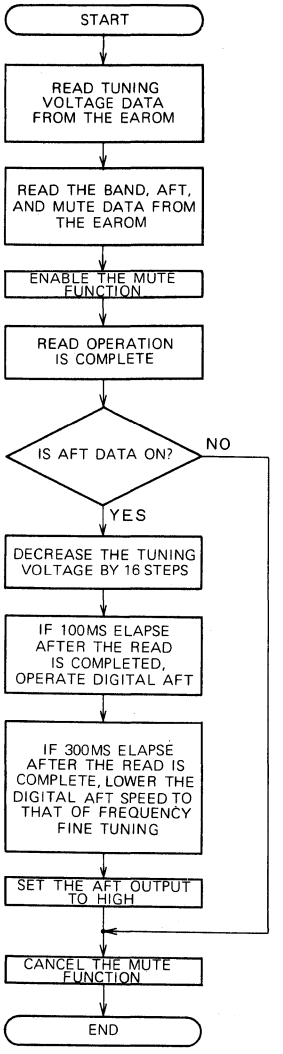
When a program selection is performed by either the key matrix or a remote control receiver the tuning voltage data which corresponds to the select channel is read out of EAROM. The read sequence is: 14-bit tuning voltage data, and then 4 bits of data on the band, AFT and muting modes. When the read operation is complete muting is turned on, and the AFT data is sensed for AFT on or off condition. If the AFT data is off, after 300ms elapses the mute function is cancelled and the MUTE data in memory takes priority. If AFT is on when this data is examined, the tuning voltage read out of memory is lowered by 16 steps (approx. 32mV). Then, after 100ms have elapsed, digital AFT is enabled. The digital AFT speed at this point is the same as the digital AFT speed in the search mode, that is, equal to 1/16 of the no signal condition search speed. When another 200ms has elapsed, the digital AFT speed becomes that of frequency fine tuning and the AFT output goes to high. Simultaneously with this the mute function is cancelled and the mute function is controlled by the MUTE data read from memory, the mute output being floating for MUTE on and low for MUTE off.

Fig. 5 shows the flowchart of program selection.

(6) Band Control Outputs ($\overline{\text{B1}}$, $\overline{\text{B2}}$)

The data indicating the currently selected band is available at the $\overline{\text{B1}}$ and $\overline{\text{B2}}$ outputs with binary code. These outputs are summarized in Table 8.

Fig. 5 Flowchart of the Program Selection



Note: At this point the digital AFT is the same as the digital AFT speed in the search mode.

Table 8 Relationship between Band Outputs and 4 Bands

$\overline{\text{B1}}$	$\overline{\text{B2}}$	Band
H	H	Band 1
L	H	Band 2
H	L	Band 3
L	L	Band 4

(7) CLEAR Key Input

When the CLEAR key is input, the tuning voltage changes to 0V and the band to Band 1. Note that the band will be Band 3 if this is the only band. AFT is turned off and the muting function is turned on, this data being written into EAROM.

This allows the system to be re-initialized during a search operation and allows the muting function to be turned on after program selection without generating any noise.

(8) Frequency Fine Tuning

When the FT(+) or FT(−) keys are input, the digital AFT function is turned off and the AFT output is left floating. The frequency is slowly shifted. The speed of this shift is given in Table 9.

While the FT(+) or FT(−) is being depressed, the frequency shifts and when the key is released, the data corresponding to the tuned frequency as well as AFT off data are written into EAROM automatically.

Table 9 Sweep Speeds of Frequency Fine Tuning

Band	Time required to sweep the entire band
Band 1	300 s (110 mV/s)
Band 2	600 s (55 mV/s)
Band 3, Band 4	1200 s (27.5 mV/s)

Note that the range of the tuning voltage is 0 ~ 33V.

(9) AFT ON key Input

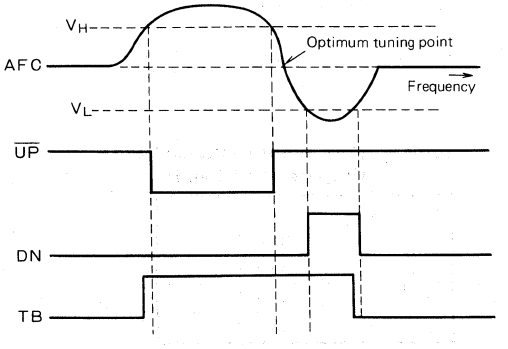
After AFT has been turned off using frequency fine tuning or the CLEAR key, if the AFT ON key is pressed the AFT function is restored and AFT ON data is written into EAROM automatically.

(10) Tunining Control Inputs ($\overline{UP}$, DN, and TB)

The $\overline{UP}$, DN and TB inputs control the search mode. The relationship to the AFC signal is shown in Fig. 6. It is possible to determine the existence of a video signal by examining the TB input.

Digital AFT is controlled by the $\overline{UP}$ and DN inputs.

Fig. 6 AFT Signal and Search Control Input Relationships



(11) Tuning Voltage Output ($\overline{D/A\ OUT}$)

As shown in Fig. 7, a pulse modulated waveform is output at $\overline{D/A\ OUT}$ in accordance with a 14-bit digital value.

The period T_0 (approx. 110Hz) is broken into 64 subperiods of width Ts = 142 μs (approx. 7kHz). This is further divided into 256 minimum periods of pulse width t_0 = 555 ns (1.8F MHz period).

The low period for each of the 64 subperiods, that is, Tm (m = 1 ~ 64) is determined as follows.

The 14-bits data word is divided into a 6-bits lower data and an 8-bits upper data. For example, if the lower data are 000000 and the upper data are 00110000, then $T_1 \sim T_{64} = 12t_0$. In this relationship one step means that the lower data would become 100000 making $T_{32} = 13t_0$, an increase in length of just t_0, with the other periods T_m remaining $12t_0$. If we step up once more the lower data become 010000, $T_{16} = T_{48} = 13t_0$, that is, two periods have now become equal to $13t_0$ with the remaining periods T_m at $12t_0$. In this manner, stepping continues until the entire lower 6-bits data are ones, that is 111111. At this point $T_1 \sim T_{63} = 13t_0$ and $T_{64} = 12t_0$. If we proceed one step further, the upper data is now affected, becoming 10110000, such that with the lower data of 000000, $T_1 \sim T_{64}$ are all $13t_0$. Therefore, we see that the lengths of the periods $T_1 \sim T_{64}$ are either all the same or have a difference of t_0, with this sequence of changing periods repeating at a rate of 7kHz.

Table 9 shows the relationship between the lower 6-bits data and the relative lengths of the periods T_m.

Fig. 7 $\overline{D/A\ OUT}$ Output Waveform

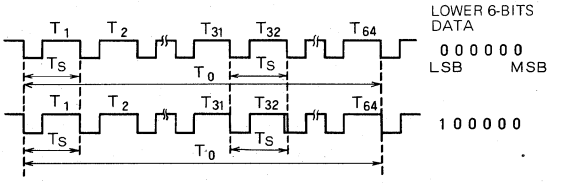
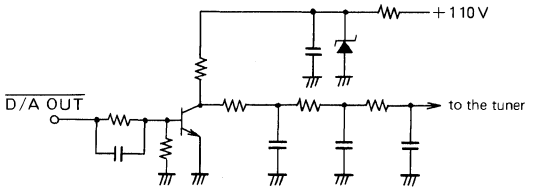


Table 10 Relationship of the Lower 6-bits Data and the Periods T_m

Lower 6-bit byte of data	Subperiods that are longer than the periods T_m (where m=1~64) by t_0
1 0 0 0 0 0	m = 32
0 1 0 0 0 0	m = 16, 48
0 0 1 0 0 0	m = 8, 24, 40, 56
0 0 0 1 0 0	m = 4, 12, 20, 28, 36, 44, 52, 60
0 0 0 0 1 0	m = 2, 6, 10, ·····58, 62
0 0 0 0 0 1	m = 1, 3, 5, ·····61, 63

Fig. 8 Low-pass Filter Circuit Example



(12) Program No. Display Output ($P_{00} \sim P_{03}$, $P_{10} \sim P_{11}$)

The outputs $P_{00} \sim P_{03}$ and $P_{10} \sim P_{11}$ are program number display outputs and are n-channel open drain outputs.

$P_{00} \sim P_{03}$ indicate lower order digit of the program number and $P_{10} \sim P_{11}$ indicate higher order digit of the program number, expressed in static BCD form.

An example of the use of this display output is shown in Fig. 9.

Fig. 9 An Example of Program Number Display Circuit

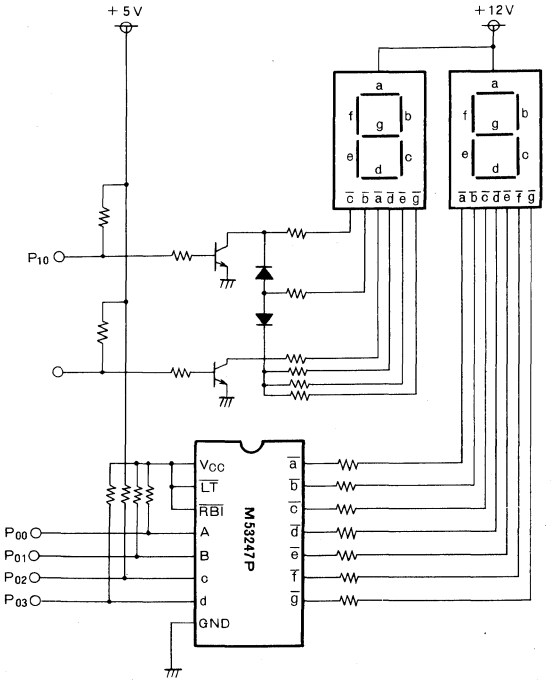


Table 11 shows the relationship between the program number and the corresponding program number display outputs. The output for Pr0 will depend upon the program counts.

Note that for the outputs listed in Table 11, a 1 indicates a floating output while a 0 indicates a low-level output.

Table 11 Output Data for $P_{00} \sim P_{11}$

Pr NO.	1's Digit				10's digit		Remarks
	P_{00}	P_{01}	P_{02}	P_{03}	P_{10}	P_{11}	
1	1	0	0	0	0	0	
2	0	1	0	0	0	0	
3	1	1	0	0	0	0	
4	0	0	1	0	0	0	
5	1	0	1	0	0	0	
6	0	1	1	0	0	0	
7	1	1	1	0	0	0	
8	0	0	0	1	0	0	
9	1	0	0	1	0	0	
10	0	0	0	0	1	0	
11	1	0	0	0	1	0	
12	0	1	0	0	1	0	
13	1	1	0	0	1	0	
14	0	0	1	0	1	0	
15	1	0	1	0	1	0	
16	0	1	1	0	1	0	
17	1	1	1	0	1	0	
18	0	0	0	1	1	0	
19	1	0	0	1	1	0	
20	0	0	0	0	0	1	
22	1	0	0	0	0	1	
22	0	1	0	0	0	1	
23	1	1	0	0	0	1	
24	0	0	1	0	0	1	
25	1	0	1	0	0	1	
26	0	1	1	0	0	1	
27	1	1	1	0	0	1	
28	0	0	0	1	0	1	
29	1	0	0	1	0	1	
0	0	0	0	0	0	0	For 20 or 30 programs
	0	0	0	0	1	0	For 10 programs
	0	1	0	0	1	0	For 12 programs
Standby mode	1	1	1	1	0	0	

(13) Standby Input ($\overline{ST}$)

When the $\overline{ST}$ input is low, the M50118P functions are inhibited and the oscillator circuit is halted. Thus the scanner output disappears and the program number display extinguishes. Since, however, the program number is held in the address counter, when the $\overline{ST}$ input is restored to high, the program number selected before the input went low is reselected. This feature is called the last program memory function.

When the $\overline{ST}$ input is low the output levels are as shown in Table 12.

Table 12 Output Levels with $\overline{ST}$ Low

Output pin name	Output level
$\overline{B1}$. $\overline{B2}$	L
$\overline{D/A\ OUT}$	L
MUTE	Open
AFT	Open
I/O	Open
CLK, C1, C2, C3	H
ϕ_A	H
ϕ_B, ϕ_C, ϕ_D	L
$\overline{SD}$	Open
P_{00}, P_{01} P_{02}, P_{03}	Open
P_{10} P_{11}	L
OSC OUT	H

(14) Power-on Reset Input ($\overline{AC}$)

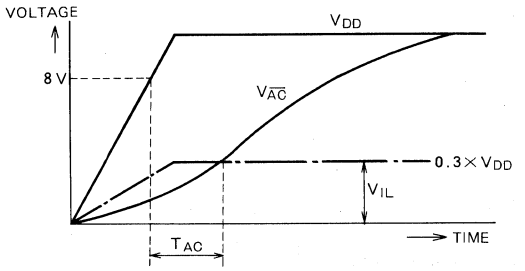
By connecting a capacitor between the $\overline{AC}$ pin and the V_{SS} pin, a power-on reset function can be implemented.

The power-on reset function is enabled to provide the clear function at the time power is applied to the device, Pr1 being automatically selected.

After both $\overline{ST}$ and $\overline{AC}$ inputs are low, when both go high Pr1 is first selected.

To assure that the power-on reset function operates reliably, after the V_{DD} supply is greater than 8V, the amount of time that the voltage $V_{\overline{AC}}$ at the pin AC is below or equal to 0.3 x V_{DD} is 1ms minimum (period T_{AC} in Fig. 10).

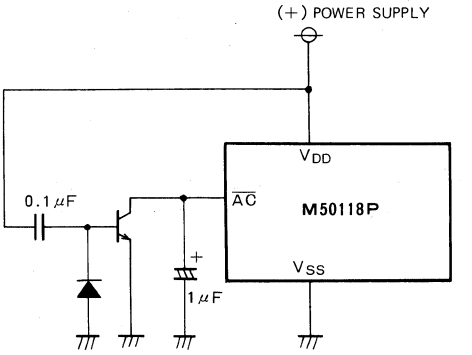
Fig. 10 Power on Reset Timing Requirements



Also, since in this system the contents of the M5G1400P EAROM for Pr1 are read upon power on, for the condition $V_{\overline{AC}} \geqq 0.3 \times V_{DD}$, the M5G1400P power supply must be at least 92% of the 35V level, i.e. at 32.2V.

When the power supply is turned off and then reapplied, the capacitor may not discharge sufficiently to ensure reliable power-on reset upon reapplying the power. For this cases the additional circuit of Fig. 11 can be used. Note, however, that the external capacitor value must be chosen such that the period $T_{AC} \geqq$ 1ms condition is met as well. (The value shown in Fig. 11 are for reference only).

Fig. 11 External Components to Ensure Reliable Power-on Reset Function



(15) Program Lock Key Input (PRL)

When the PRL key is input program selection from the keyboard the Pr0 ~ Pr11, 10 – 19 and 20 – 29 keys, as well as the PR UP and PR DN functions are locked out, that is, prohibited.

Note however, that in this mode, program selection using $\overline{PR\ UP}$, $\overline{PR\ DN}$, and $\overline{PR\ RE}$ from the remote control receiver is not prohibited.

(16) AFT Output

The AFT pin controls the on/off switching of the linear AFT function. When the AFT output is high, linear AFT is operating. When it is low or high-impedance (floating), linear AFT is not operating.

Table 13 summarizes the AFT modes of operation.

Table 13 AFT Output Logic Levels

Mode	AFT output logic level
Search mode (during sweep)	L
Search mode (during the 200ms that digital AFT is operating)	Z
Program select mode (with linear AFT on)	H
Program select mode (with linear AFT off)	Z

(17) Mute Output

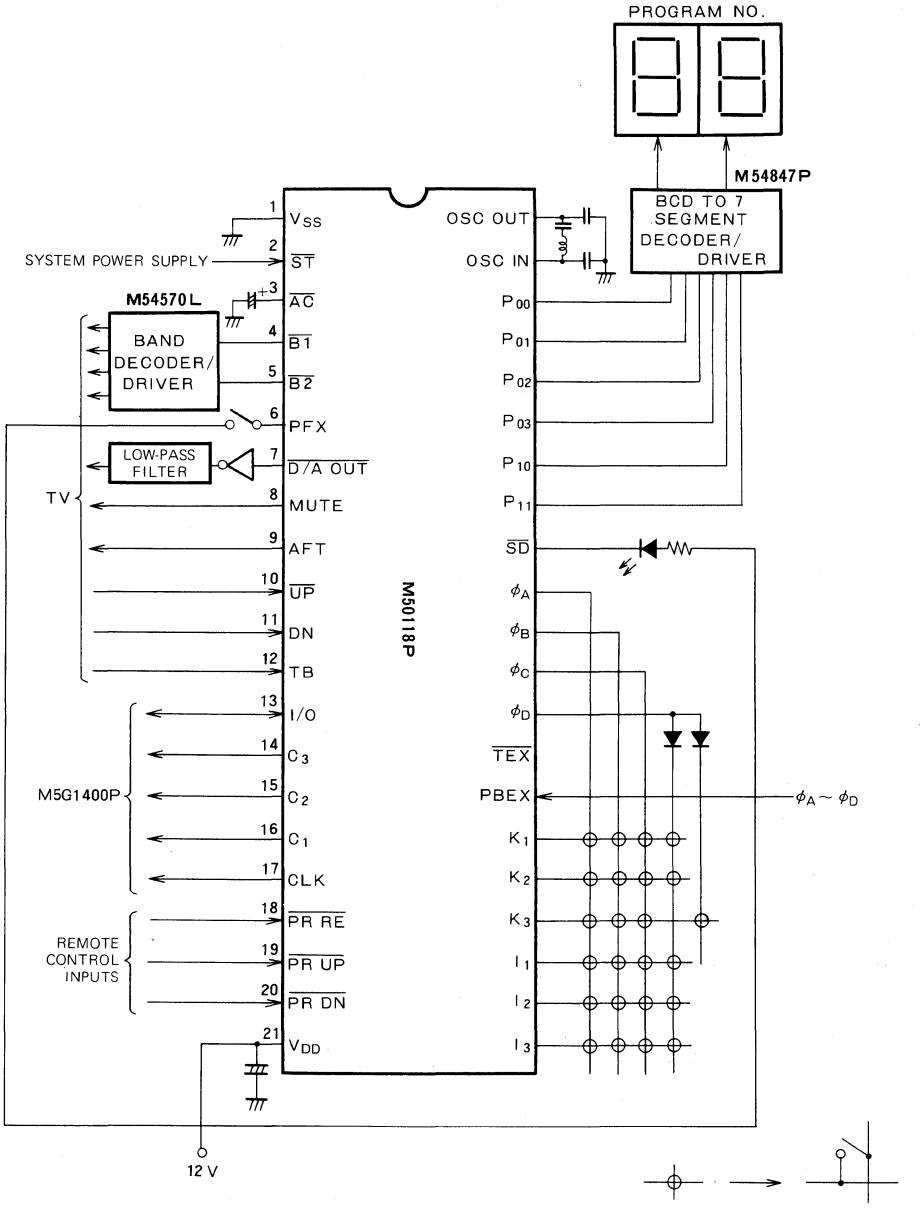
The MUTE pin controls the MUTE on/off switching. In the fully automatic search mode this can be sensed using this output. When the MUTE output is high or high-impedance (floating), muting is on. When it is low, muting is off. Table 14 summarizes the Mute modes of operation.

Table 14 Mute Output Logic Levels

Mode	Mute output logic level
Fully automatic search	H
Other modes with muting on	Z
Muting off	L

Note the Z indicates a floating output.

APPLICATION EXAMPLE



M50119P

REMOTE CONTROL TRANSMITTER FOR TV RECEIVERS EQUIPPED WITH TELETEXT AND VIEWDATA SYSTEMS

DESCRIPTION

The M50119P is an aluminum-gate CMOS integrated circuit consisting of a infrared control circuit for controlling TV receivers equipped with Teletext and Viewdata systems. By means of a 10-bit code, it is capable of transmitting 36 commands.

The M50119P can be used in combination with the M50120P receiver IC.

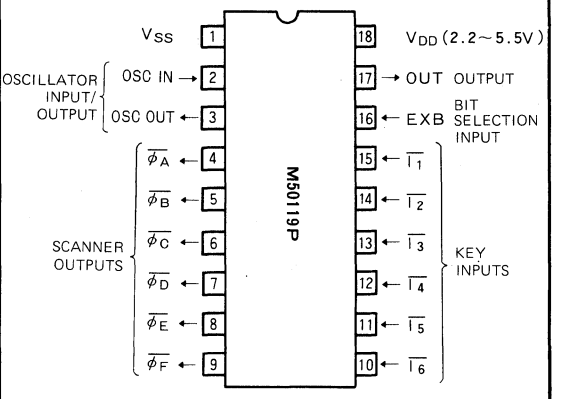
FEATURES

- Single power supply
- Wide supply voltage range ..... 2.2 ~ 5.5V
- Low power consumption when not operating
  (V_{DD}= 3V) ..... 3nW (typ)
  3μW (max)
- Built-in oscillator makes use of a ceramic resonator or LC circuit
- The power consumption of the LED during transmission of a command is low, resulting in high reliability for the LED
- Low number of external components

FUNCTION

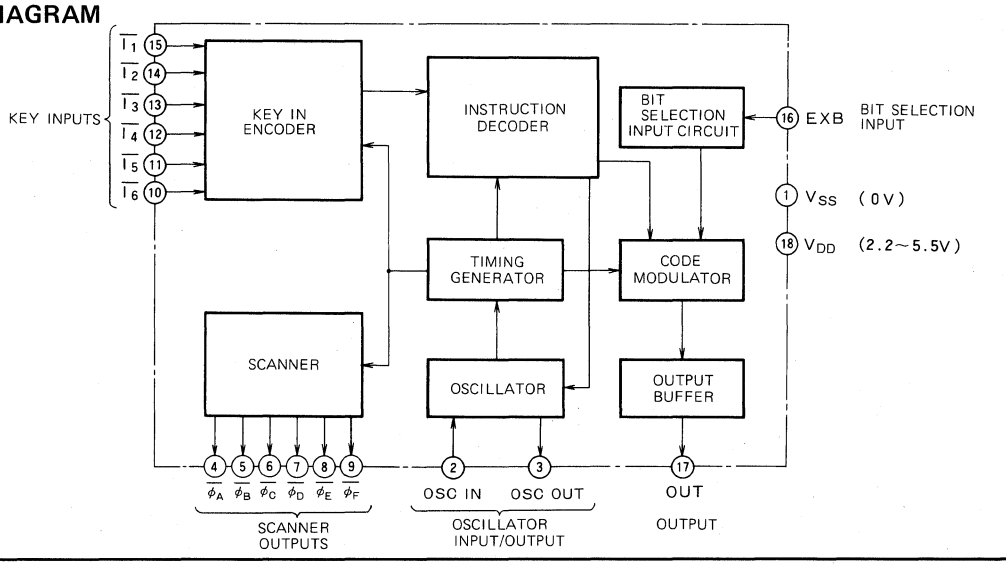
The M50119P infrared TV remote control transmitter consists of an oscillator, timing generator, scanner signal generator, key input encoder, command decoder, code modulation circuit, bit selection input circuit and an output buffer. It has a 6 x 6 keyboard matrix input and encodes the key inputs in 10-bit PCM code to enable transmission of 36 commands. When key input is not being performed, the oscillator is stopped to reduce power consumption to as low a level as possible.

PIN CONFIGURATION (TOP VIEW)



Outline 18P4

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

REMOTE CONTROL TRANSMITTER FOR TV RECEIVERS EQUIPPED WITH TELETEXT AND VIEWDATA SYSTEMS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{DD}	Supply voltage	With respect to the V_{SS} pin	−0.3∼6	V
V_I	Input voltage		$V_{SS}-0.3 \leqq V_I \leqq V_{DD}+0.3$	V
V_O	Output voltage		$V_{SS} \leqq V_O \leqq V_{SS}$	V
Pd	Maximum power dissipation	Ta=25°C	300	mW
Topr	Operating free-air temperature range		−30∼70	°C
Tstg	Storage temperature range		−40∼125	°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{DD}	Supply voltage	2.2		5.5	V
f_{OSC}	Oscillation frequency		455		kHz
			480		
V_{IH}	High-level input voltage	$0.7\times V_{DD}$	V_{DD}	V_{DD}	V
V_{IL}	Low-level input voltage	0	0	$0.3\times V_{DD}$	V
$C_{I-\phi}$	Inter-pin capacitance, between $\overline{T}_1\sim\overline{T}_6$ and $\overline{\phi_A}\sim\overline{\phi_F}$ pins			100	pF

ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{DD}=3V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{DD}	Supply voltage	Ta=−30∼70°C	2.2	3.0	5.5	V
I_{DD}	Supply current, operating	f_{OSC}=455kHz		0.1	0.3	mA
I_{DD}	Supply current, non-operating				1	μA
R_I	Pull-up resistance, $\overline{T}_1\sim\overline{T}_6$	V_{DD}=2.2∼5.5V	30	50	70	kΩ
I_{OL}	Low-level output current $\overline{\phi_A}\sim\overline{\phi_F}$	V_{OL}=0.9V	0.1	0.5		mA
I_{OH}	High-level output current, OUT	V_{OH}=2V	5	10		mA
R_I	Pull-up resistance, EXB	V_{DD}=2.2∼5.5V	15	25		kΩ

FUNCTIONAL DESCRIPTION

(1) Oscillator Circuit

Since a built-in oscillator circuit has been provided, all that need be provided externally is either a ceramic resonator or LC circuit to obtain the reference signal. The circuits for ceramic resonator and LC circuits are shown in Fig. 1 and 2 respectively.

By setting the reference frequency to 480kHz or 455kHz, the transmitted frequency will be 40kHz or 38kHz respectively.

When key input is not being performed, the oscillator is shut off to minimize power consumption.

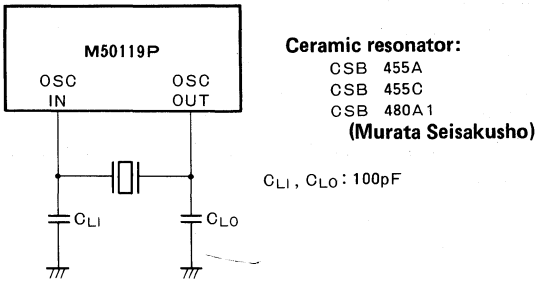


Fig. 1 Example of oscillator using a ceramic resonator

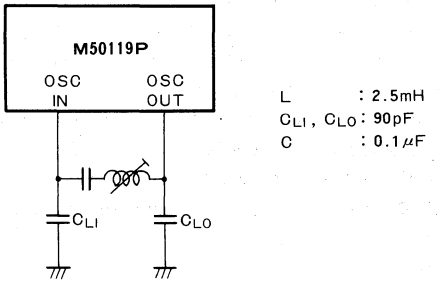


Fig. 2 Example of oscillator circuit using an LC circuit

REMOTE CONTROL TRANSMITTER FOR TV RECEIVERS EQUIPPED WITH TELETEXT AND VIEWDATA SYSTEMS

(2) Key Input

A 6 x 6 keyboard matrix is formed by the $\overline{I_1} \sim \overline{I_6}$ inputs and $\overline{\phi_A} \sim \overline{\phi_F}$ scan outputs, enabling the input of 36 commands.

If two or more keys are pressed simultaneously, no keys will have any effect.

Table 1 shows the relationship between the key matrix and the transmitted commands.

Table 1 Keyboard Matrix and Transmission Codes

Scan output / Key input	$\overline{\phi_A}$	$\overline{\phi_B}$	$\overline{\phi_C}$	$\overline{\phi_D}$	$\overline{\phi_E}$	$\overline{\phi_F}$
$\overline{I_1}$	Pr 1	Pr 2	Pr 3	10 – 19	TV mode	Mute
	No 1	No 2	No 3	———	TV mode	Mute
	No 1	No 2	No 3	———	TV mode	Mute
	D	E	F	———	TV mode	Mute
$\overline{I_2}$	Pr 4	Pr 5	Pr 6	20 – 29	Text mode	POW ON/OFF
	No 4	No 5	No 6	———	Text mode	POW ON/OFF
	No 4	No 5	No 6	———	Text mode	POW ON/OFF
	G	H	I	———	Text mode	POW ON/OFF
$\overline{I_3}$	Pr 7	Pr 8	Pr 9	CALL 2	View mode	(Pr 10)
	No 7	No 8	No 9	Top	View mode	———
	No 7	No 8	No 9	Top	View mode	———
	J	K	L	O	View mode	———
$\overline{I_4}$	Pr 0	CT DN	CT UP	CALL 1	RSV mode	(Pr 11)
	No 0	Timed page on	Timed page off	Full page	RSV mode	———
	No 0	#	*	Full page	RSV mode	———
	M	CT DN	CT UP	N	RSV mode	———
$\overline{I_5}$	CS UP	BR UP	VO UP	Pr UP	Time	———
	———	BR UP	VO UP	Hold	Text concel	Bottom
	Tape Rec.	BR UP	VO UP	Ring off	Picture	Bottom
	CS UP	BR UP	VO UP	A	C	P
$\overline{I_6}$	CS DN	BR DN	VO DN	Pr DN	Norm	Mix
	———	BR DN	VO DN	Reveal	Norm	Mix
	Tape play	BR DN	VO DN	Reveal	Norm	Mix
	DS DN	BR DN	VO DN	B	Norm	Q

Equal key commands in the matrix always result in the same transmitted code being output. While in Table 1 the same key is shown in 4 different positions, this results in different operations as determined by the function of the M50120P receiver IC. The operating modes are, from the top, TV, Text, Viewdata, and RSV.

In the 12 prog. type of operation, Pr0 ~ Pr11 will result, in a single action, in the channel being selected. For this operation the 10–19 and 20–29 keys are not required.

For 20 channel use, the Pr10, Pr19 keys are selectable with a single action, with Pr10 through Pr19 requiring two actions. For example, to select Pr15 the 10–19 key is first pressed followed by the 5 key to complete the selection. If however more than approximately 6.5 seconds elapses after pressing the 10–19 key before the 5 key is pressed, the M50120P will not accept the direct sleection command for the channel range Pr10 ~ Pr19.

By using the 10–19 and 20–29 keys, direct selection of up to 30 channels can be made. The method of selection for the range 20 to 29 is much the same as for the range 10 to 19, with the 20–29 key replacing the 10–19 key in the key-in sequence to allow direct sleection of the range Pr20 to Pr29.

For 20 channel or 30 channel operation, the Pr10 and Pr11 keys are not required.

(3) Transmitted Commands

As shown in Fig. 3, the transmitted commands are coded in a 10-bit format. The first 3 bits, K_0, K_1, and K_2 are the key code. For Teletext control the M50119P sets these to the code 101. Bit D_6 is a user's bit which is 0 when the bit selection input EXB is set to high or left open. When this input is low, the user's bit is 1.

When D_6 is 0, the M50120P receiver IC may be operated. (when it is 1, the M50120P does not operate).

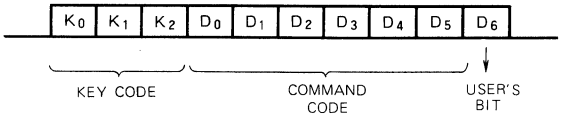


Fig. 3 Transmitted code format

Table 2 Relationships of command functions and transmitted codes

	D_6	D_5	D_4	D_3	D_2	D_1	D_0	TV mode	Text mode	View date mode	RSV mode (Note 1)	(Note 2)
1	0	0	0	0	0	0	0	Norm.	Norm.	Norm.	Norm.	O
2	0	0	0	0	0	0	1	Mute	Mute	Mute	Mute	O
3	0	0	0	0	0	1	0	POW ON/OFF	POW ON/OFF	POW ON/OF F	POW ON/OFF	O
4	0	0	0	0	0	1	1	TV mode	TV mode	TV mode	TV mode	O
5	0	0	0	0	1	0	0	RSV mode	RSV mode	RSV mode	RSV mode	O
6	0	0	0	0	1	0	1	PR UP	Hold	Ring off	A	R
7	0	0	0	0	1	1	0	PR DN	Reveal	Reveal	B	R
8	0	0	0	0	1	1	1	Time	Text cancel	Picture display	C	R
9	0	0	0	1	0	0	0	VO UP	VO UP	VO UP	VO UP	R
10	0	0	0	1	0	0	1	VO DN	VO DN	VO DN	VO DN	R
11	0	0	0	1	0	1	0	BR UP	BR UP	BR UP	BR UP	R
12	0	0	0	1	0	1	1	BR DN	BR DN	BR DN	BR DN	R
13	0	0	0	1	1	0	0	CS UP	———	Tape Rec.	CS UP	R
14	0	0	0	1	1	0	1	CS DN	———	Tape play	CS DN	R
15	0	0	0	1	1	1	0	CT UP	Timed page off	*	CT UP	R
16	0	0	0	1	1	1	1	CT DN	Timed page on	#	CT DN	R
17	0	1	1	0	0	0	0	Pr 1	Number 1	Number 1	D	O
18	0	1	1	0	0	0	1	2	2	2	E	O
19	0	1	1	0	0	1	0	3	3	3	F	O
20	0	1	1	0	0	1	1	4	4	4	G	O
21	0	1	1	0	1	0	0	5	5	5	H	O
22	0	1	1	0	1	0	1	6	6	6	I	O
23	0	1	1	0	1	1	0	7	7	7	J	O
24	0	1	1	0	1	1	1	8	8	8	K	O
25	0	1	1	1	0	0	0	9	9	9	L	O
26	0	1	1	1	0	0	1	0	0	0	M	O
27	0	0	1	1	0	1	0	CALL 1	Full page	Full page	N	O
28	0	0	1	1	0	1	1	CALL 2	Top	Top	O	R
29	0	0	1	1	1	0	0	———	Bottom	Bottom	P	R
30	0	0	1	1	1	0	1	Viewdata mode	Viewdata mode	Viewdata mode	Viewdata mode	O
31	0	0	1	1	1	1	0	Mix	Mix	Mix	Q	O
32	0	0	1	1	1	1	1	Text mode	Text mode	Text mode	Text mode	O
33	0	1	1	1	0	1	0	Pr10	———	———	———	O
34	0	1	1	1	0	1	1	Pr11	———	———	———	O
35	0	0	1	0	0	0	0	10 – 19	———	———	———	O
36	0	0	1	0	0	0	1	20 – 29	———	———	———	O

Note 1. For codes marked "O" only 5 words are transmitted. Those marked "R" are transmitted continuously with a period of 28ms (for f_{osc} = 480kHz)

2. The RSV mode is reserved for future expanded systems.

(4) Transmission Coding Method

The following description will be made for an oscillation frequency of 480kHz. If another frequency is used, the periods and frequencies mentioned will have to be multiplied by 480kHz/f_{osc} and f_{osc}/480kHz respectively.

A single pulse is amplitude modulated by a 40kHz, the pulse width being 0.5ms. With this timing relationship, there are 20 clocks of 40kHz in one pulse (refer to Fig. 4).

Distinction between 1 and 0 in the transmitted signal is made by changing the pulse spacing. As is shown in Fig. 5, for the code 0 the pulse spacing is 1ms while for the code 1 it is 2ms.

One transmitted word consists of 10 bits and therefore 11 pulses which are transmitted with a period of 28ms as long as the associated key is being depressed.

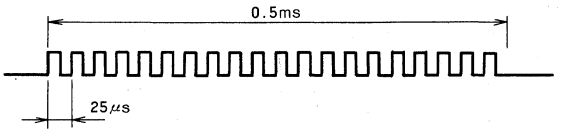


Fig. 4 A single pulse, modulated with a 40kHz signal

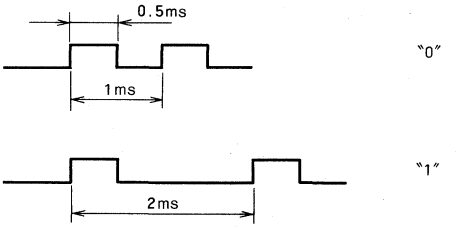


Fig. 5 The distinction between the 0 and 1 codes

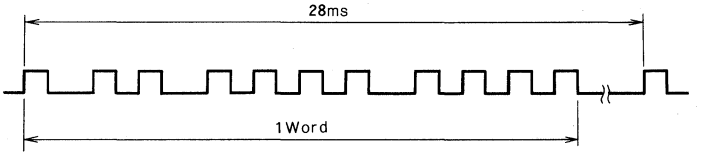
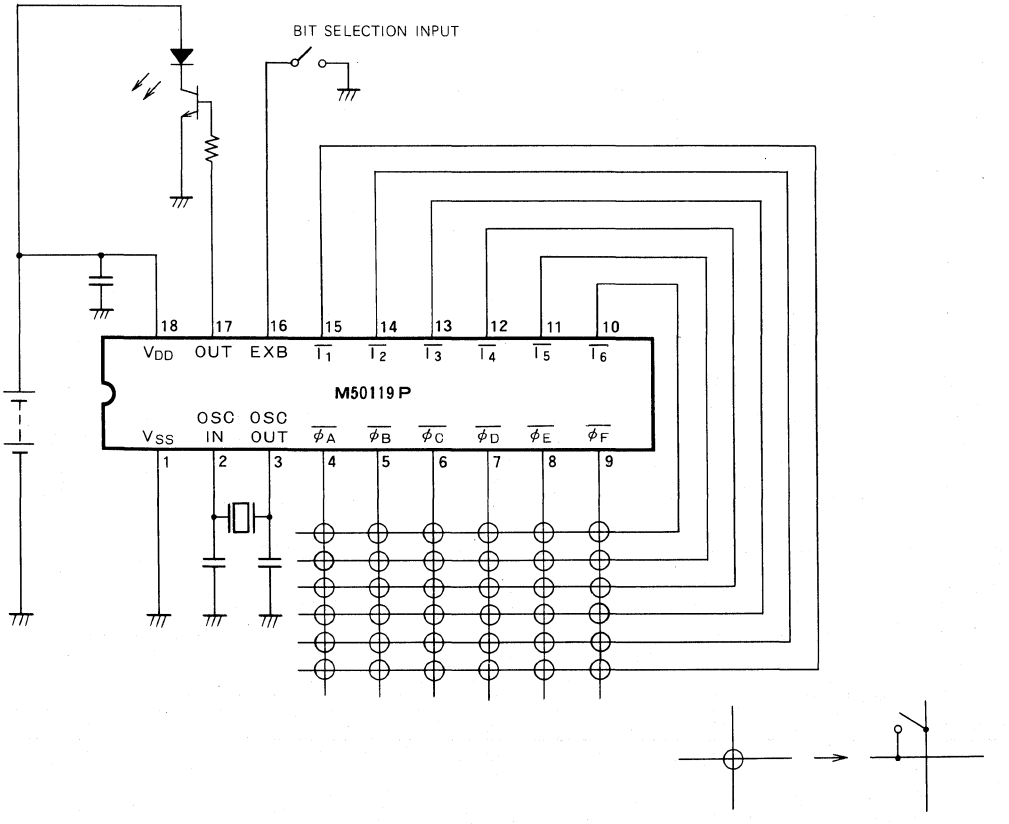


Fig. 6 Single-word format (the code shown is 1010001000)

APPLICATION EXAMPLE



MITSUBISHI ELECTRIC

M50120P

REMOTE CONTROL RECEIVER IC FOR THE TELETEXT AND VIEWDATA SYSTEMS

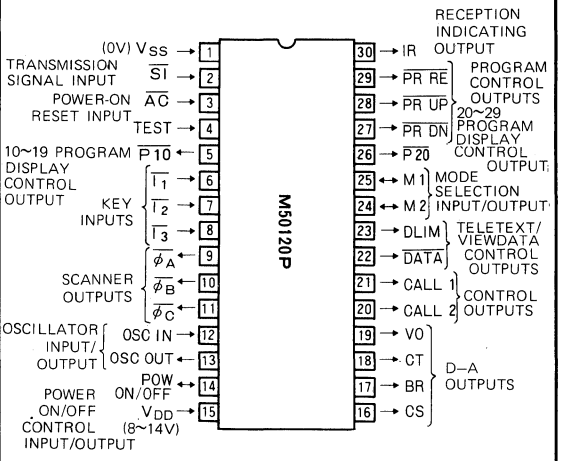
DESCRIPTION

The M50120P is an aluminum-gate CMOS integrated circuit consisting of a circuit capable of controlling Teletext and Viewdata equipped TV receivers using an infrared remote control system. The circuit can receive 36 commands and has 9 direct key functions as well.

FEATURES

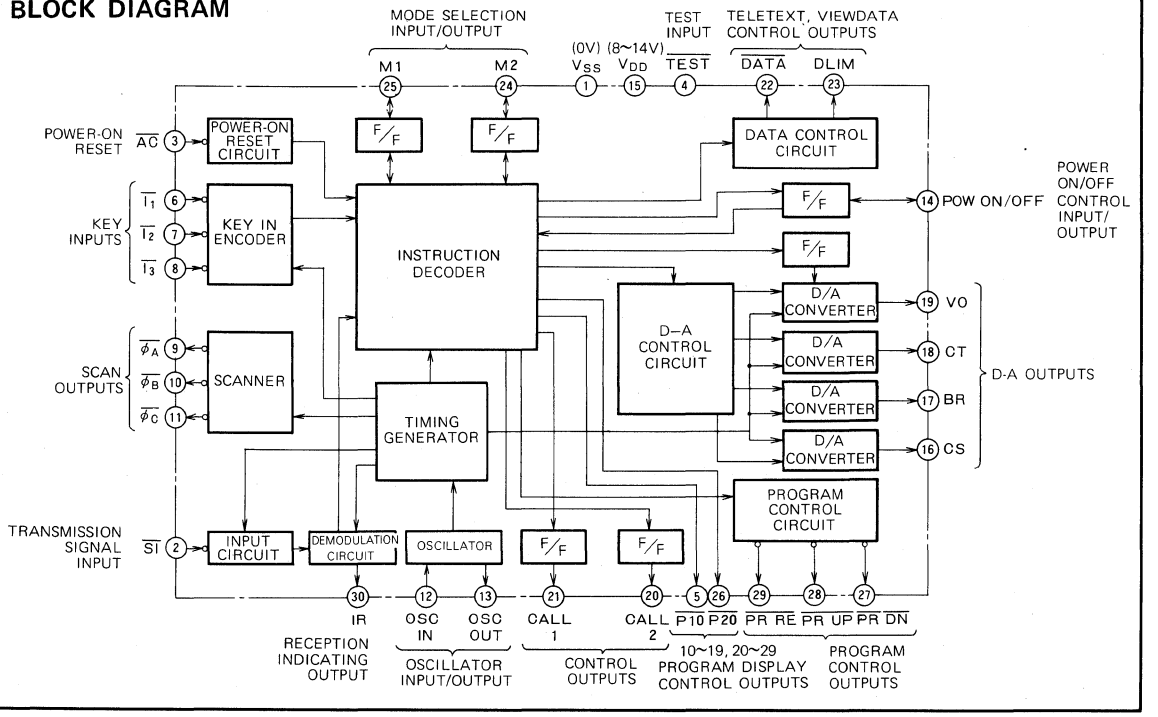
- Single supply voltage and operation over a wide supply voltage range ..... 8~14V
- Low power dissipation
- Built-in oscillator makes use of a ceramic resonator or LC circuit
- The transmitted signal is PCM coded for immunity to interference
- Simple, single frequency receiving system
- Direct selection of 30 programs (channels)
- 4 analog functions controllable with 64 discrete levels using four 6-bit D-A converters
- The receiver can accept 9 control commands
- Large tolerances for the transmit and receive frequencies
- Can be used in conjunction with an M51231P (or equivalent) touch-control electronic channel selector IC
- Can be used in conjunction with an M58486AP or M50118P tuning IC's

PIN CONFIGURATION (TOP VIEW)



Outline 30P4

BLOCK DIAGRAM



REMOTE CONTROL RECEIVER IC FOR THE TELETEXT AND VIEWDATA SYSTEMS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{DD}	Supply voltage	With respect to V_{SS}	−0.3～15	V
V_I	Input voltage		$V_{SS}-0.3 \leqq V_I \leqq V_{DD}+0.3$	V
V_O	Output voltage		$V_{SS} \leqq V_O \leqq V_{DD}$	V
Pd	Maximum power dissipation	Ta = 25°C	300	mW
Topr	Operating free-air temperature range		−30～70	°C
Tstg	Storage temperature range		−40～125	°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{DD}	Supply voltage	8	12	14	V
f_{OSC}	Oscillation frequency		455		kHz
			480		
V_{IH}	High-level input voltage, $\overline{I_1}$～$\overline{I_3}$, POW on/off, M1, M2, $\overline{AC}$	$0.7 \times V_{DD}$	V_{DD}	V_{DD}	V
V_{IL}	Low-level input voltage, $\overline{I_1}$～$\overline{I_3}$, POW on/off, M1, M2, $\overline{AC}$	0	0	$0.3 \times V_{DD}$	V
V_{IL}	High-level input voltage, $\overline{SI}$	$0.9 \times V_{DD}$	V_{DD}	V_{DD}	V
V_{IL}	Low-level input voltage, $\overline{SI}$	0	0	$0.1 V_{DD}$	V
$C_{I-\phi}$	Inter-pin capacitance, between $\overline{I_1}$～$\overline{I_3}$ and $\overline{\phi_A}$～$\overline{\phi_C}$ pins			100	pF

ELECTRICAL CHARACTERISTICS (Ta = 25°C, V_{DD} = 12V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{DD}	Supply voltage	Ta = −30°C～+70°C	8	12	14	V
I_{DD}	Supply current	f_{OSC} = 455kHz			5	mA
V_{OL}	Low-level output voltage, $\overline{\phi_A}$～$\overline{\phi_C}$	I_{OL} = 200μA			1	V
I_{OL}	Low-level output currents, $\overline{PR\ RE}$, $\overline{PR\ UP}$, $\overline{PR\ DN}$	V_{OL} = 0.4V	3.5			mA
I_{OZH}	Off-state output currents, $\overline{PR\ RE}$, $\overline{PR\ UP}$, $\overline{PR\ DN}$	V_{OH} = 12V			1	μA
I_{OH}	High-level output currents, VO, BR, CS, CT	V_{OH} = 10V	4			mA
I_{OL}	Low-level output currents, VO, BR, CS, CT	V_{OL} = 2V	10			mA
I_{OH}	High-level output current, POW on/off	V_{OH} = 10V	11			mA
I_{OL}	Low-level output current, POW on/off	V_{OL} = 2V	6.5			mA
I_{OZH}	Off-state output current, POW on/off	V_{OH} = 12V			1	μA
I_{OH}	High-level output currents, CALL 1, CALL 2	V_{OH} = 10V	11			mA
I_{OL}	Low-level output currents, CALL 1, CALL 2	V_{OL} = 2V	5			mA
I_{OL}	Low-level output currents, M1, M2	V_{OL} = 0.4V	3.5			mA
I_{OZH}	Off-state output currents, M1, M2	V_{OH} = 12V			1	μA
V_{OH}	High-level output voltage, $\overline{DATA}$, DLIM	I_{OH} = 1mA	10			V
V_{OL}	Low-level output voltage, $\overline{DATA}$, DLIM	I_{OL} = 1mA			0.3	V
I_{OH}	High-level output current, IR	V_{OH} = 10V	7			mA
I_{OL}	Low-level output current, IR	V_{OH} = 12V	5			mA
I_{OZH}	Off-state output current, IR	V_{OH} = 12V			1	μA
I_{OL}	Low-level output currents, $\overline{P10}$, $\overline{P20}$	V_{OL} = 2V	1.8			mA
I_{OH}	High-level output currents, $\overline{P10}$, $\overline{P20}$	V_{OH} = 10V	0.2			mA
R_I	Pull-up resistance, $\overline{I_1}$～$\overline{I_3}$	V_{DD} = 8～14V		30		kΩ
R_I	Pull-up resistance, $\overline{AC}$	V_{DD} = 8～14V		55		kΩ

REMOTE CONTROL RECEIVER IC FOR THE TELETEXT AND VIEWDATA SYSTEMS

FUNCTION

The M50120P infrared TV remote control receiver IC, when it receives the same transmitted signal from the transmitter three times, executes the associated command, enabling a remote control system that is resistant to interferance.

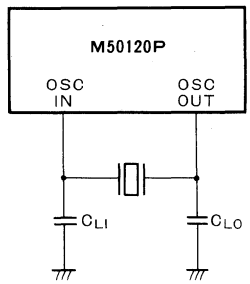
The M50120P has four modes, TV, Teletext, Viewdata, and RSV. Its control functions for reception of the same transmitted signal depend on which mode has been set (refer to Table 1 for details).

In addition, nine control functions can be input at the receiver.

FUNCTIONAL DESCRIPTION

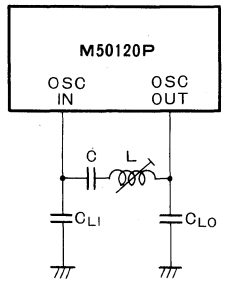
(1) Oscillator Circuit

Since a built-in oscillator circuit has been provided, all that need be provided externally is either a ceramic resonator or LC circuit to obtain the reference signal. The circuits for ceramic resonator and LC circuits are shown in Fig. 1 and 2 respectively.



CSB 455A
CSB 455C
CSB $480A_1$
C_{LI}, C_{LO} 50~150pF

Fig. 1 Example of oscillator circuit using ceramic resonator



L : 2.5mH
C_{LI}, C_{LO} : 90pF
C : 0.1μF

Fig. 2 Example of an oscillator circuit using an LC circuit

In the description below frequencies and periods are given for the case of a 480kHz reference frequency.

(2) Received Frequency Input Circuits and Demodulation Circuit

The amplified and integrated signal captured by the photodetector is applied to the $\overline{SI}$ input. The signal applied to this input is processed by the input circuit and sent to the demodulator circuit. In the demodulator circuit the pulse spacing of this pulse signal is determined and the signal is converted to a digital code. Fig. 3 shows the relationship between the $\overline{SI}$ signal input waveform and the coded data (a schmitt trigger is provided at the SI input to prevent spurious operation caused by noise.)

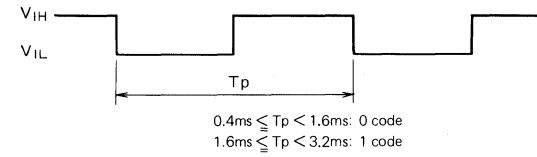


Fig. 3 $\overline{SI}$ Input waveform and code relationship

If the pulse spacing of the signal input at the $\overline{SI}$ input is greater than 3.2ms, the input circuit judges that a word has ended. Approximately 60ms after this, the transmitted command is assumed to have ended.

(3) Error Prevention Circuit

Signals shorter than 100μs at the $\overline{SI}$ input are not recognized as transmitted codes. Also, if the pulse spacing Tp is less than 0.4ms, the current word is not used as a valid word.

Command words will be decoded only when the key code (K_0, K_1, K_2) is 101 (the D_6 bit set at 0).

(4) Receiving Status Determination and Receiver Display Output (IR)

When the same transmitted code is received three times, a pulse of approximatley 4.9Hz is output at the receiver display output IR. By using an externally connected LED, therefore, the reception of a signal from the transmitter can be indicated by a flashing display.

The IR output uses a CMOS circuit and is in the off state (high-impedance) when waiting for a signal and in a CMOS output state while the LED is flashing.

(5) Command Decoder

When the same transmitted code is received three times, the command decoder executes the command corresponding to the transmitted code.

Table 1 Relationship of Commands and Transmitted Codes.

No.	Data code								M2	M1			M2	M1			M2	M1			M2	M1
									D_8	D_7			D_8	D_7			D_8	D_7			D_8	D_7
	D_6	D_5	D_4	D_3	D_2	D_1	D_0	TV mode		0	0	Text mode		1	0	Viewdate mode		1	1	RSV mode		0	1
1	0	0	0	0	0	0	0	Norm.	S	0	0	Norm.	S	0	0	Norm.	S	0	0	Norm.	NT	–	–
2	0	0	0	0	0	0	1	Mute	S	0	0	Mute	S	1	0	Mute	S	1	1	Mute	S	0	1
3	0	0	0	0	0	1	0	POW ON/OFF	S	0	0	POW ON/OFF	S	1	0	POW ON/OFF	S	1	1	POW ON/OFF	S	0	1
4	0	0	0	0	0	1	1	TV mode	S	0	0	TV mode	S	0	0	TV mode	S	0	0	TV mode	S	0	0
5	0	0	0	0	1	0	0	RSV mode	S	0	1	RSV mode	S	0	1	RSV mode	S	0	1	RSV mode	S	0	1
6	0	0	0	0	1	0	1	PR UP	NT	0	0	Hold	S	1	0	Ring off	S	1	1	A	S	0	1
7	0	0	0	0	1	1	0	PR DN	NT	0	0	Reveal	R	1	0	Reveal	R100	1	1	B	S	0	1
8	0	0	0	0	1	1	1	Time	S	0	0	Text camcel	R	1	0	Picture	R100	1	1	C	S	0	1
9	0	0	0	1	0	0	0	VO UP	NT	–	–	VO UP	NT	–	–	VO UP	NT	–	–	VO UP	NT	–	–
10	0	0	0	1	0	0	1	VO DN	NT	–	–	VO DN	NT	–	–	VO DN	NT	–	–	VO DN	NT	–	–
11	0	0	0	1	0	1	0	BR UP	NT	–	–	BR UP	NT	–	–	BR UP	NT	–	–	BR UP	NT	–	–
12	0	0	0	1	0	1	1	BR DN	NT	–	–	BR DN	NT	–	–	BR DN	NT	–	–	BR DN	NT	–	–
13	0	0	0	1	1	0	0	CS UP	NT	–	–	——	S	1	0	Tape Rec.	S	1	1	CS UP	NT	–	–
14	0	0	0	1	1	0	1	CS DN	NT	–	–	——	S	1	0	Tape play	S	1	1	CS DN	NT	–	–
15	0	0	0	1	1	1	0	CT UP	NT	–	–	TP off	S	1	0	*	S	1	1	CT UP	NT	–	–
16	0	0	0	1	1	1	1	CT DN	NT	–	–	TP on	S	1	0	#	S	1	1	CT DN	NT	–	–
17	0	1	1	0	0	0	0	Pr 1	NT	–	–	No. 1	S	1	0	No. 1	S	1	1	D	S	0	1
18	0	1	1	0	0	0	1	2	NT	–	–	2	S	1	0	2	S	1	1	E	S	0	1
19	0	1	1	0	0	1	0	3	NT	–	–	3	S	1	0	3	S	1	1	F	S	0	1
20	0	1	1	0	0	1	1	4	NT	–	–	4	S	1	0	4	S	1	1	G	S	0	1
21	0	1	1	0	1	0	0	5	NT	–	–	5	S	1	0	5	S	1	1	H	S	0	1
22	0	1	1	0	1	0	1	6	NT	–	–	6	S	1	0	6	S	1	1	I	S	0	1
23	0	1	1	0	1	1	0	7	NT	–	–	7	S	1	0	7	S	1	1	J	S	0	1
24	0	1	1	0	1	1	1	8	NT	–	–	8	S	1	0	8	S	1	1	K	S	0	1
25	0	1	1	1	0	0	0	9	NT	–	–	9	S	1	0	9	S	1	1	L	S	0	1
26	0	1	1	1	0	0	1	0	NT	–	–	0	S	1	0	0	S	1	1	M	S	0	1
27	0	0	1	1	0	1	0	CALL 1	NT	–	–	Full page	S	1	0	Full page	S	1	1	N	S	0	1
28	0	0	1	1	0	1	1	CALL 2	NT	–	–	Top	S	1	0	Top	S	1	1	O	S	0	1
29	0	0	1	1	1	0	0	——	NT	–	–	Bottom	S	1	0	Bottom	S	1	1	P	S	0	1
30	0	0	1	1	1	0	1	View mode (Note 2)	S	1	1	View mode	S	1	1	View mode	S	1	1	View mode	S	1	1
31	0	0	1	1	1	1	0	Mix (Note 2)	S	1	0	Mix	S	1	0	Mix	S	1	0	Q	S	0	1
32	0	0	1	1	1	1	1	Text mode (Note 2)	S	1	0	Text mode	S	1	0	Text mode	S	1	0	Text mode	S	1	0
33	0	1	1	1	0	1	0	Pr 10	NT	–	–	——	NT	–	–	——	NT	–	–	——	NT	–	–
34	0	1	1	1	0	1	1	Pr 11	NT	–	–	——	NT	–	–	——	NT	–	–	——	NT	–	–
35	0	0	1	0	0	0	0	10 – 19	NT	–	–	——	NT	–	–	——	NT	–	–	——	NT	–	–
36	0	0	1	0	0	0	1	20 – 29	NT	–	–	——	NT	–	–	——	NT	–	–	——	NT	–	–

Note 1. NT: No data output
S: One word of output only
R: Data output with a repetition period of 102ms
2. When the M2 pin is grounded, data output D_7=0

(6) Key Input

The inputs $\overline{I_1}$~$\overline{I_3}$ and the scan outputs $\overline{\phi_A}$ ~ $\overline{\phi_C}$ forming 3x3 keyboard Matrix allowing the input of 9 functions. If two keys are pressed simultaneously, neither will have any effect.

Transmission of signals while the keys are being pressed is inhibited.

Table 2 shows the relationship between the keyboard matrix and the command functions

Table 2 Relationships Between the Keyboard Matrix and Commands

Scanner output / Key input	$\overline{\phi_A}$	$\overline{\phi_B}$	$\overline{\phi_C}$
$\overline{I_1}$	VO UP	BR UP	CS UP
$\overline{I_2}$	VO DN	BR DN	CS DN
$\overline{I_3}$	CT UP	CT DN	CALL 1

Note. Analog up/on operate upon key input regardless of the mode.

(7) Analog Outputs (VO, BR, CS, CT)

The M50120P includes four 6-bit D-A converters which produce four independent analog signals of 64-level resolution for control functions. The output repetition frequency is 1.25kHz (with f_{osc} = 480kHz) and the minimum pulse width is 12.5μs forming a type of pulse width modulated output.

With either remote control or keyboard input, the analog quantities are stepped at approximately 1 step/0.1s either up or down. Thus, to slew from the minimum to the maximum analog value requires approximately 6.6s (with f_{osc}= 480kHz).

Using the remote control Norm command, BR, CS and CT can be set to 1/2 of the maximum value. Note, however, that for this operation VO does not change.

(8) Muting

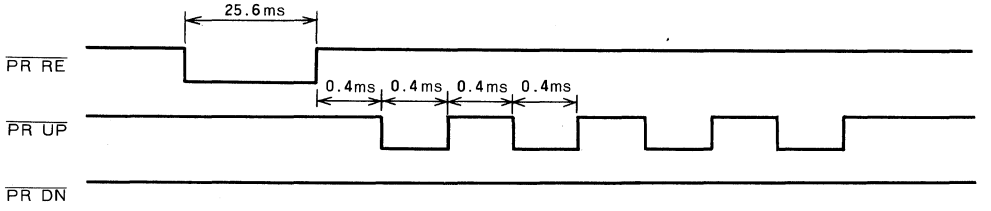
Muting on/off control can be accomplished remotely. When muting is on, the VO output is its minimum value L. In this state remote control or keyboard input can be used to either increase the VO output or decrease it, thereby canceling the muted condition. Note that when muting is canceled in this manner, the slew up or down starts from the level set prior to setting the muted condition.

(9) Program Control

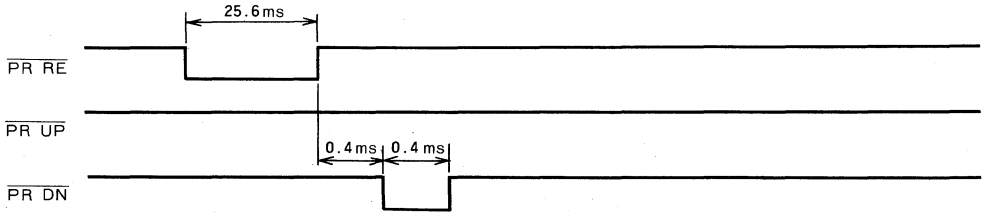
For direct channel selection, selection of Pr1 ~ Pr29 begins with a single pulse appearing at the $\overline{\text{PR RE}}$ output next, a number of pulse appears at the $\overline{\text{PR UP}}$ output equal to the selected channel number minus 1.

Fig. 4(a) shows the $\overline{\text{PR RE}}$ and $\overline{\text{PR UP}}$ output timing relationship.

As shown in Fig. 4(b), for the selection of Pr0, a single pulse appears at the $\overline{\text{PR RE}}$ output after which a single pulse appears at the $\overline{\text{PR-DN}}$ output.



(a) Example for Selection of Pr5



(b) Example for Selection of Pr0

Fig. 4 Program control output timing

For 12 Prog. operation, direct channel selection can be made using the keyboard Matrix range Pr0 ~ Pr11 with the M50119P transmitter IC. For this operation the 10 ~ 19 and 20 ~ 29 keys are not required. For 20 Prog. operation, Pr0 ~ Pr9 can be directly selected using only one key action and Pr10 ~ Pr19 with two key actions. For example, to select Pr15, first the 10 ~ 19 key is pressed followed by the 5 key to complete the selection. If, however, more than approximately 6.5 seconds elapses after receiving the 10 ~ 19 transmitted code before the 5 key code is received, the M50120P will not accept the direct selection command for the channel range Pr10 ~ Pr19.

By using the 10 ~ 19 and 20 ~ 29 keys, direct selection of up to 30 channels can be made. The method of selection for the range Pr20 ~ Pr29 is much the same as for the range Pr10 ~ Pr19, with the 20 ~29 key replacing the 10 ~ 19 key in the key-in sequence to allow direct selection of the range Pr20 ~ Pr29.

For 20 channel or 30 channel operation, the Pr10 and Pr11 keys are not required.

For sequential channel selection, when the remote control $\overline{\text{PR UP}}$ or $\overline{\text{PR DN}}$ command is received, one pulse appears in the $\overline{\text{PR UP}}$ or $\overline{\text{PR DN}}$ output respectively.

When the $\overline{\text{PR UP}}$ or $\overline{\text{PR DN}}$ commands are received repetitively, pulses appear at the corresponding $\overline{\text{PR UP}}$ or $\overline{\text{PR DN}}$ outputs at a period of 0.8s. The pulse width is 0.4ms, the same as with direct channel selection.

For both direct and sequential channel selection, the VO output changes to low level automatically for approximately 100ms.

The $\overline{\text{PR UP}}$, $\overline{\text{PR DN}}$, and $\overline{\text{PR RE}}$ outputs are n-channel open-drain outputs.

(10) $\overline{\text{P10}}$ and $\overline{\text{P20}}$ Outputs

When the $\overline{10 \sim 19}$ command is received, the $\overline{\text{P10}}$ output goes low for approximately 64 ~ 120ms. When this signal is applied to the M50118P voltage synthesizer IC key input, the program number lower order digits are dropped from the M50118P display output and the upper order digit flashes as 1.

When the $\overline{20 \sim 29}$ command is received, in the same manner as for the $\overline{10 \sim 19}$ command, the $\overline{\text{P20}}$ output goes low for approximately 64 ~ 120ms and the M50118P program number display output upper digit flashes as 2.

Fig. 5 shows the timing diagram for $\overline{\text{P10}}$ and $\overline{\text{P20}}$ outputs. Fig. 6 shows the interconnections with the M50118P.

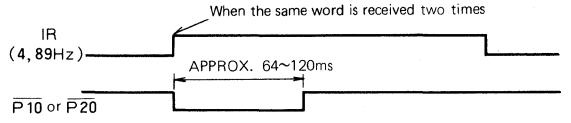


Fig. 5 $\overline{\text{P10}}$ and $\overline{\text{P20}}$ output timing diagram

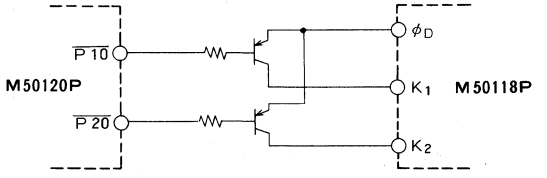


Fig. 6 $\overline{\text{P10}}$ and $\overline{\text{P20}}$ output connections to the M50118P

(11) Power Supply On/Off

The POW on/off input/output pin can be changed from low to high or high to low by means of the remote control input.

When the input/output pin is low and receives a high level externally, the pin remains high and the power on condition is maintained even if the external signal is removed.

When the POW on/off input/output pin is low, except for POW on/off commands, the remote control function and key input commands are all inhibited.

In addition, when the POW on/off output goes from low to high, the TV mode is always enabled.

Note that for approximately 25.6ms after the POW on/off input/output pin goes from high to low, tthe POW on input will not accept a high signal.

The POW on/off input/output is a P-channel transistor, open drain circuit.

(12) CALL 1 Output

The CALL 1 output can be changed from low to high or high to low using the remote control or keyboard input. Note, however, that this operates only in the TV mode.

(13) CALL 2 Output

When the CALL 2 command is input by means of the remote control function the CALL 2 output goes from low to control function, the CALL 2 output goes from low to high, remaining high only while the CALL 2 command is input. Note that this operates only in the TV mode.

Table 3 Modes and Output Status Relationships

Pin / Mode	M1(D_7)	M2(D_8)	Mode modification commands
T V	0	0	Norm, TV mode
Teletext	0	1	Text mode, Mix (Note)
Viewdata	1	1	View mode
RSV	1	0	RSV mode

Note. The mix command is not valid in the RSV mode.
The Norm. command cannot be used to change from the RSV mode to the TV mode. Note that BR, CS, and CT analog outputs change to 1/2 of their normal values.

(14) Mode Selection inputs/outputs (M1, M2)

These pins indicate the mode of the M50120P as shown in Table 3.

M1 and M2 are input/output pins. Grounding M1 inhibits the Viewdata and RSV modes while grounding M2 inhibits the Teletext and Viewdata modes. Grounding both M1 and M2 inhibits all modes except the TV mode.

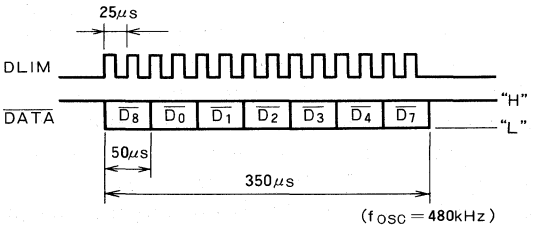


Fig. 7 $\overline{\text{DATA}}$ and DLIM output timing diagram

(15) Teletext and Viewdata Control Outputs ($\overline{DATA}$, DLIM)

The $\overline{DATA}$ output is a serial output consisting of the command byte of 5 bits ($D_0 \sim D_4$) and the mode status 2-bit byte ($D_7 \sim D_8$) of the transmitted 10-bit code. The $\overline{DATA}$ output for remote control is shown in Table 1.

The DLIM output is a clock output of period 25μs which is active while output is available at $\overline{DATA}$.

The timing relationships for the $\overline{DATA}$ and DLIM outputs are shown in Fig. 5.

(16) Power-on Reset

By connecting a capacitor to the $\overline{AC}$ pin, a power-on reset function can be provided for the M50120P.

When this power-on reset function operates, the VO, BR, CS and CT outputs are set to 1/2 of the maximum values, the CALL 1 and CALL 2 outputs are set to low, both mode selection outputs M1 and M2 are set to low (TV mode), the channel control outputs $\overline{PR\ RE}$, $\overline{PR\ UP}$, $\overline{PR\ DN}$, are all set to off, the $\overline{DATA}$ output is set to high, and the DLIM output to low.

To assure that the power-on reset function operates properly at the time of power-on, as shown in Fig. 8, for a supply voltage (V_{DD}) greater than 8V, the voltage at the $\overline{AC}$ pin ($V_{\overline{AC}}$) must remain below $0.3 \times V_{DD}$ for more than 1ms.

If the power supply is shut off and reapplied before the voltage on pin $\overline{AC}$ has dropped sufficiently, the T_{AC} time minimum of 1ms may not be satisfied. In this case, by using the additional circuitry shown in Fig. 9 connected to input pin $\overline{AC}$, the power-on reset function can be reliably implemented. Care should be taken in chosing the external capacitor such that $T_{AC} \geqq 1$ms (the value shown in Fig. 9 is an example only).

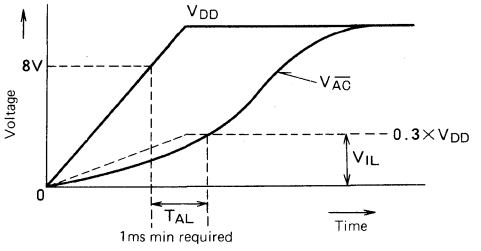


Fig. 8 Relationship of power supply rise (V_{DD}) and pin $\overline{AC}$ voltage ($V_{\overline{AC}}$)

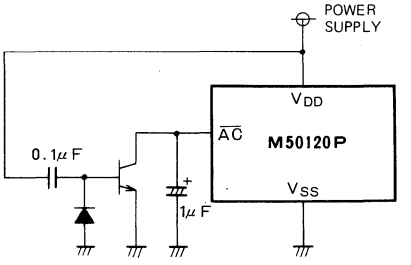


Fig. 9 External circuitry required for reliable power-on reset functioning

Power Supply On/Off

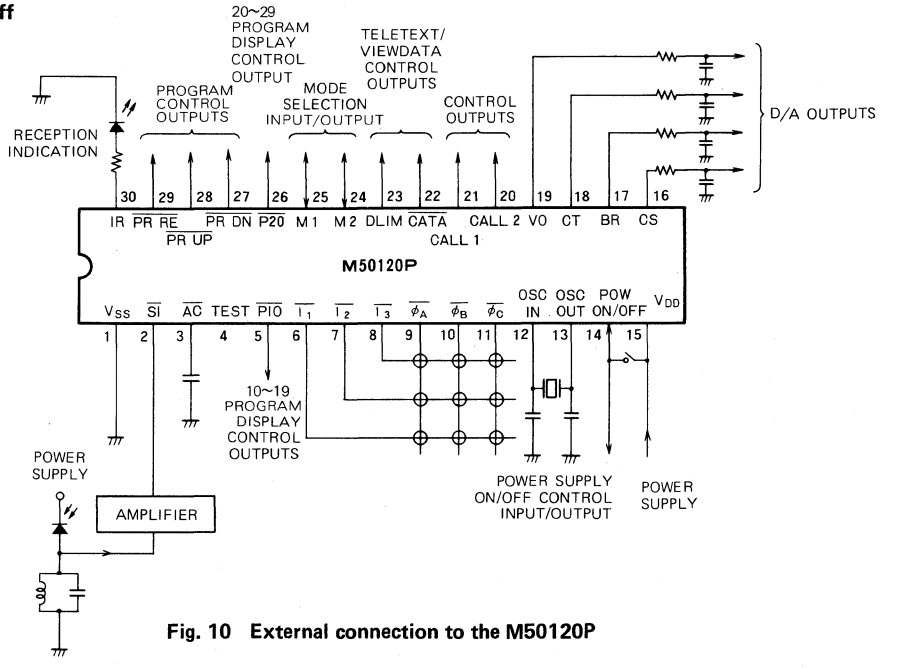


Fig. 10 External connection to the M50120P

M54452P

1/64 HIGH-SPEED DIVIDER WITH TTL OUTPUT

DESCRIPTION

The M54452P is a semiconductor integrated circuit consisting of a 1/64 high-speed frequency divider with an ECL circuit configuration.

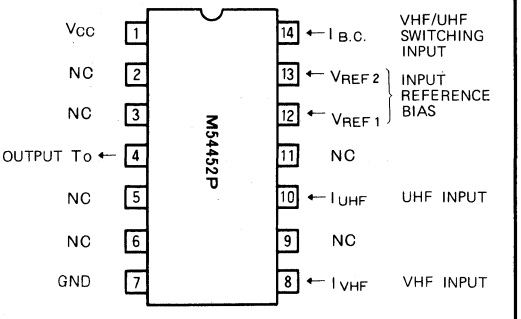
FEATURES

- Ultra-high-speed operation (f_{max} = 1.2 GHz)
- Operation at low input amplitude (300mV_{P-P} minimum input amplitude)
- TTL level output
- Two inputs (UHF and VHF)
- TTL level compatible band switching input

APPLICATIONS

Prescalers for PLL synthesizer TV tuners; digital equipment for consumer and industrial applications

PIN CONFIGURATION (TOP VIEW)



NC: NO CONNECTED

Package Outline 14P4

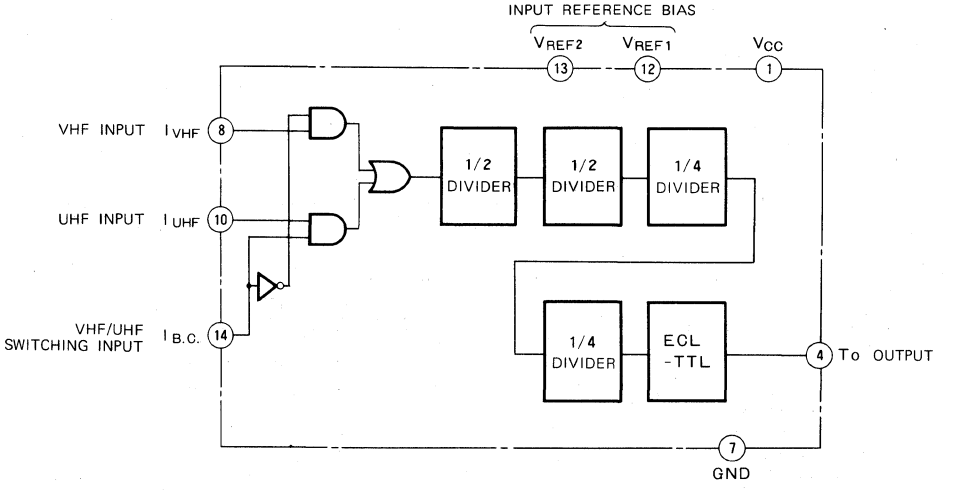
FUNCTION

This 1/64 frequency divider is based on an ECL circuit configuration. When a frequency between 450MHz and 950MHz is applied to the UHF input (I_{UHF}) pin, a 1/64-divided frequency output is obtained. The same output is obtained when a frequency between 80MHz and 350MHz is applied to the VHF input (I_{VHF}) pin. The output (T_O) conforms to the TTL level.

A wide-band operating system should be used when the UHF input pin is supplied with frequencies ranging from 80MHz to 950MHz.

When the band switching input ($I_{B.C.}$) pin is high or open, the UHF input (I_{UHF}) pin can be used and when it is low the VHF input (I_{VHF}) pin can be used. Do not supply signals simultaneously to the UHF input (I_{UHF}) and VHF input (I_{VHF}) pins.

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

1/64 HIGH-SPEED DIVIDER WITH TTL OUTPUT

ABSOLUTE MAXIMUM RATINGS (Ta = −10 ~ +75°C , unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		9	V
V_I	Input voltage		2.5	V_{P-P}
$V_{B,C}$	Band switching input voltage		−0.5 ~ +7.2	V
I_O	Output current		−30 ~ +30	mA
Topr	Operating temperature		−10 ~ +75	°C
Tstg	Storage temperature		−55 ~ +125	°C

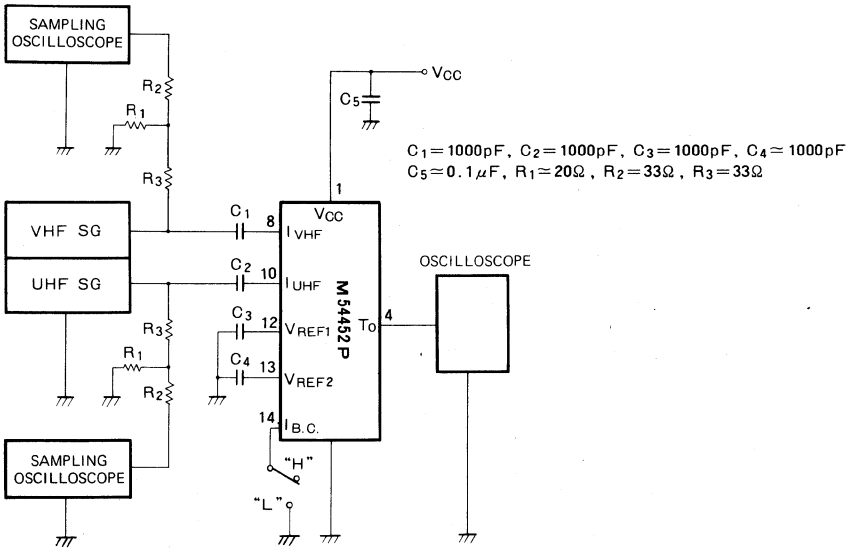
RECOMMENDED OPERATING CONDITIONS (Ta = −10 ~ +75°C , unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	6.1	6.8	7.5	V
I_{OL}	"L" Output current			5	mA

ELECTRICAL CHARACTERISTICS (Ta = −10 ~ +75°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Limits			Unit
			Min	Typ	Max	
I_{CC}	Circuit current	V_{CC}=6.8V		68		mA
V_{OH}	High-level output voltage	V_{CC}=6.8V, I_{OH}=−0.2mA	2.5	3.5		V
V_{OL}	Low-level output voltage	V_{CC}=6.8V, I_{OL}=5mA			0.4	V
V_{BCH}	High-level band switching input voltage		2.5			V
V_{BCL}	Low-level band switching input voltage				0.4	V
V_S	VHF Input sensitivity	V_{CC}=6.8V, Ta=25°C f_{IN}=80~350MHz			300	mV_{P-P}
U_{S1}	UHF Input sensitivity 1	V_{CC}=6.8V, Ta=25°C f_{IN}=450~950MHz			300	mV_{P-P}
U_{S2}	UHF Input sensitivity 2	V_{CC}=6.8V, Ta=25°C f_{IN}=80~350MHz			300	mV_{P-P}
Vmax	VHF Maximum input level	f_{IN}=80~350MHz	1			V_{P-P}
Umax	UHF Maximum input level	f_{IN}=450~950MHz	1			V_{P-P}

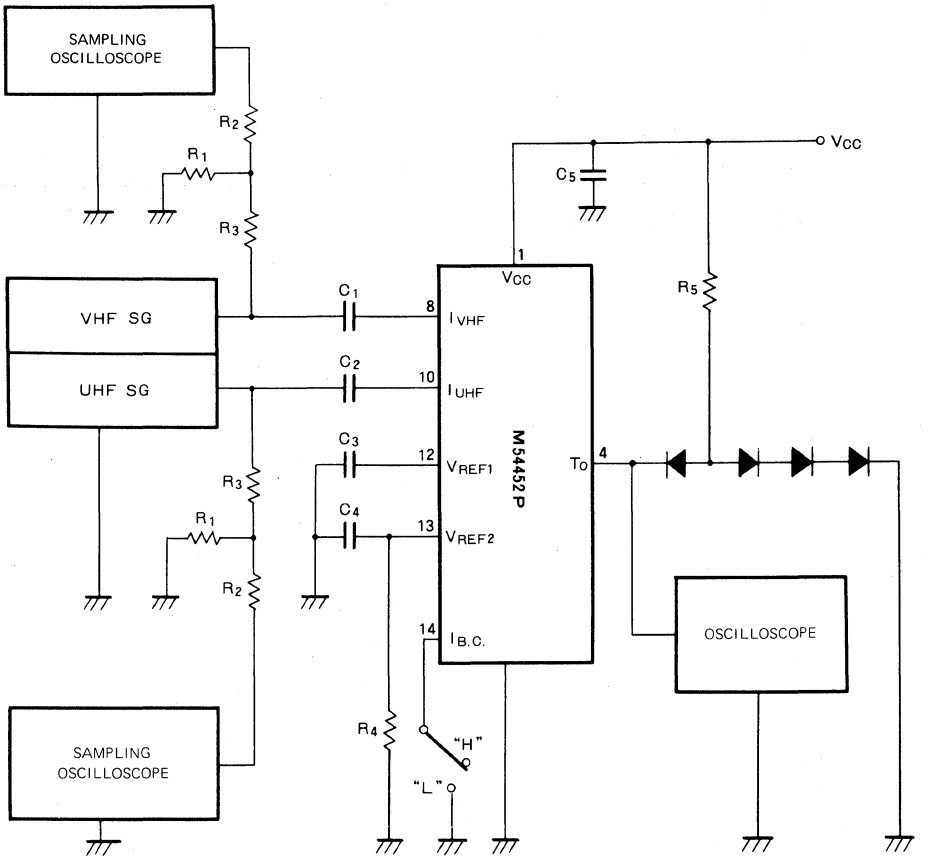
f_{max} TEST CIRCUIT



1/64 HIGH-SPEED DIVIDER WITH TTL OUTPUT

APPLICATION EXAMPLE

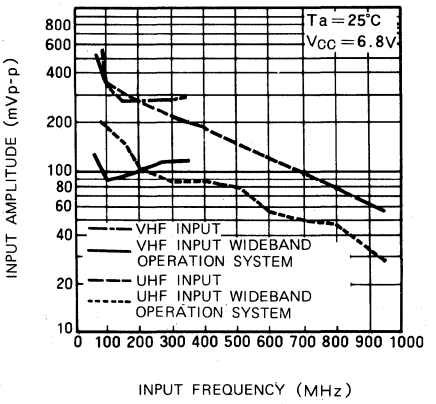
For wide-band operation



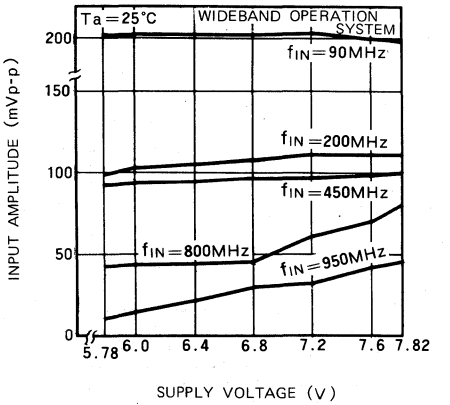
Operation across an even wider frequency range is enabled for the UHF input by setting R_4 between V_{REF2} and GND with C_1 = 1000pF, C_2 = 1000pF, C_3 = 1000pF, C_4 = 1000pF, C_5 = 0.1μF, R_1 = 20Ω, R_2 = 33Ω, R_3 = 33Ω, R_4 = 36kΩ, R_5 = 1kΩ.

TYPICAL CHARACTERISTICS

MINIMUM INPUT AMPLITUDE VS INPUT FREQUENCY



MINIMUM INPUT AMPLITUDE VS SUPPLY VOLTAGE



MITSUBISHI ELECTRIC

M54454P

1/256 HIGH-SPEED DIVIDER WITH TTL OUTPUT

DESCRIPTION

The M54454P is a semiconductor integrated circuit consisting of a built-in 1/256 high-speed frequency divider in an ECL circuit configuration.

FEATURES

- Ultra-high-speed operation (f_{max} = 1.2GHz)
- Operation at low input amplitude (300mV_{P-P} minimum input amplitude)
- TTL level output
- Two inputs (UHF and VHF)
- TTL level compatible bandswitching input

APPLICATIONS

Prescalers for PLL synthesizer TV tuners; digital equipment for consumer and industrial application

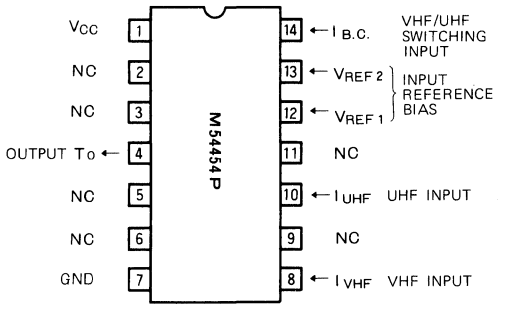
FUNCTION

This 1/256 frequency divider is based on an ECL circuit configuration. When a frequency between 450MHz and 950MHz is applied to the UHF input (I_{UHF}) pin, a 1/256-divided frequency output is obtained. The same output is obtained when a frequency between 80MHz and 350MHz is applied to the VHF input (I_{VHF}) pin. The output (T_O) conforms to the TTL level.

A wideband operating system should be used when the UHF input pin is supplied with frequencies ranging from 80MHz to 950MHz.

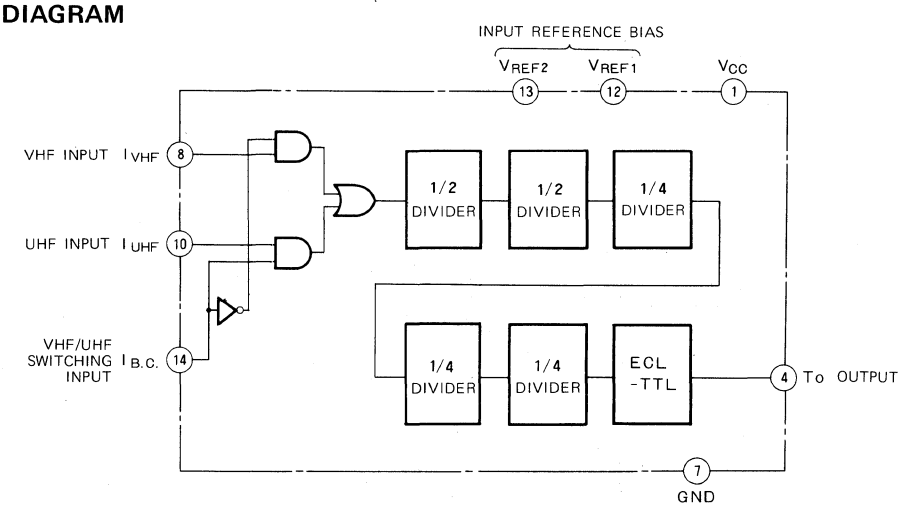
When the bandswitching input ($I_{B.C.}$) pin is high or open, the UHF input (I_{UHF}) pin can be used and when it is low, the VHF input (I_{VHF}) pin can be used. Do not supply signals simultaneously to the UHF input (I_{UHF}) and VHF input (I_{VHF}) pins.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4 NC: NO CONNECTION

BLOCK DIAGRAM



1/256 HIGH-SPEED DIVIDER WITH TTL OUTPUT

ABSOLUTE MAXIMUM RATINGS (Ta = −10 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		9	V
V_I	Input voltage		2.5	V_{P-P}
$V_{B,C}$	Band switching input voltage		−0.5 ~ +7.2	V
I_O	Output current		−30 ~ +30	mA
Topr	Operating temperature		−10 ~ +75	°C
Tstg	Storage temperature		−55 ~ +125	°C

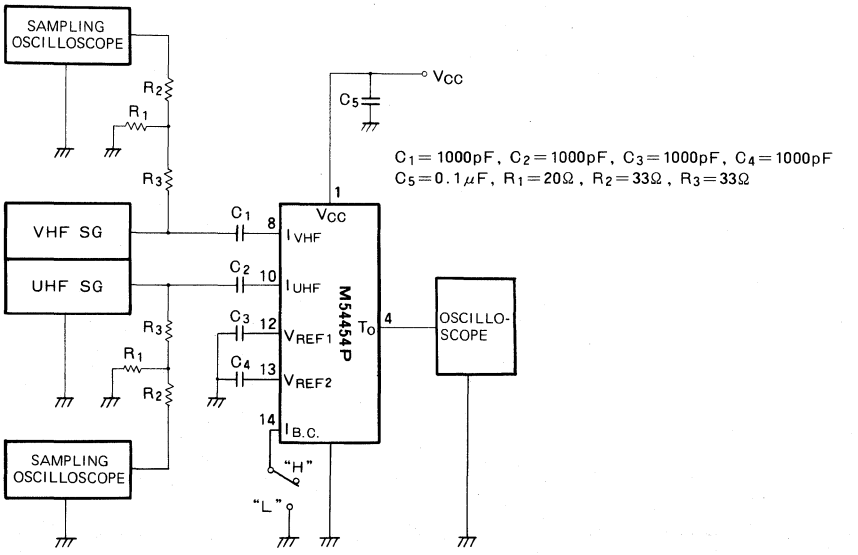
RECOMMENDED OPERATING CONDITIONS (Ta = −10 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	6.1	6.8	7.5	V
I_{OL}	Low-level output current			5	mA

ELECTRICAL CHARACTERISTICS (Ta = −10 ~ +75°C unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CC}	Circuit current	V_{CC} = 6.8V		68		mA
V_{OH}	High-level output voltage	V_{CC} = 6.8V, I_{OH} = −0.2mA	2.5	3.5		V
V_{OL}	Low-level output voltage	V_{CC} = 6.8V, I_{OL} = 5mA			0.4	V
V_{BCH}	High-level bandswitching input voltage		2.5			V
V_{BCL}	Low-level bandswitching input voltage				0.4	V
V_S	VHF input sensitivity	V_{CC} = 6.8V, Ta = 25°C f_{IN} = 80 ~ 350MHz			300	mV_{P-P}
U_{S1}	UHF input sensitivity 1	V_{CC} = 6.8V, Ta = 25°C f_{IN} = 450 ~ 950MHz			300	mV_{P-P}
U_{S2}	UHF input sensitivity 2	V_{CC} = 6.8V, Ta = 25°C f_{IN} = 80 ~ 350MHz			300	mV_{P-P}
Vmax	VHF maximum input level	f_{IN} = 80 ~ 350MHz	1			V_{P-P}
Umax	UHF maximum input level	f_{IN} = 450 ~ 950MHz	1			V_{P-P}

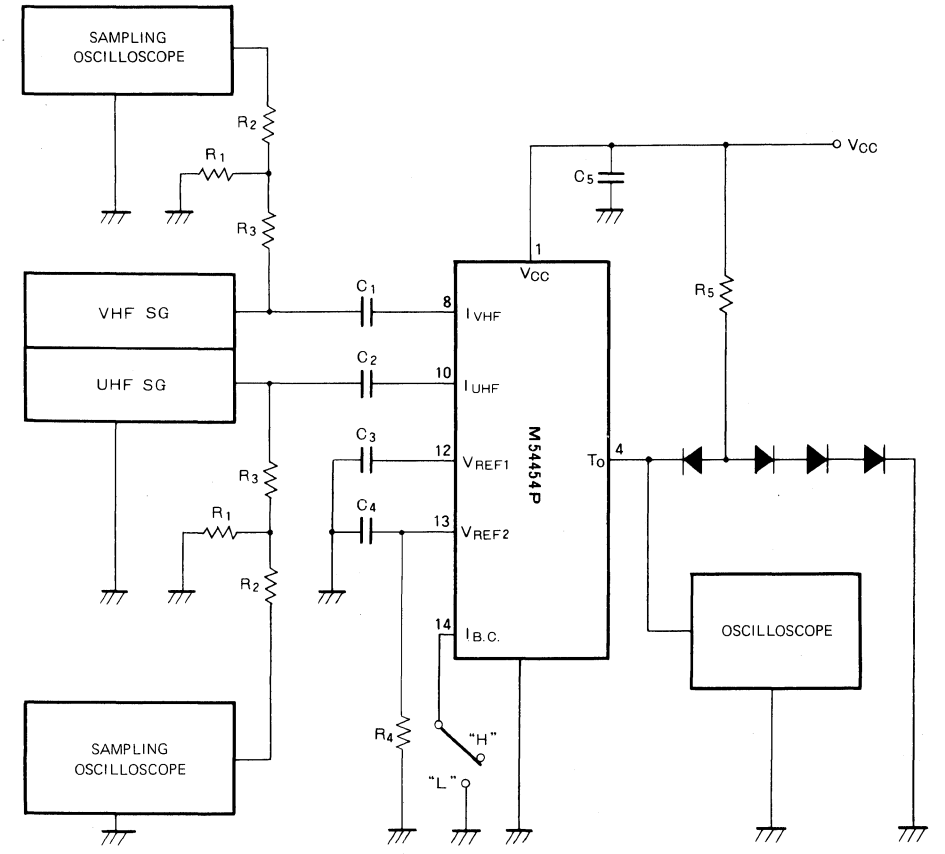
f_{max} TEST CIRCUIT



MITSUBISHI ELECTRIC

APPLICATION EXAMPLE

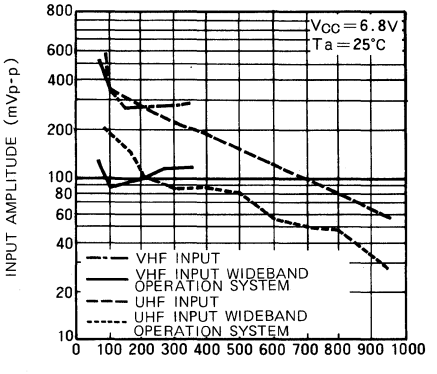
For wide-band operation



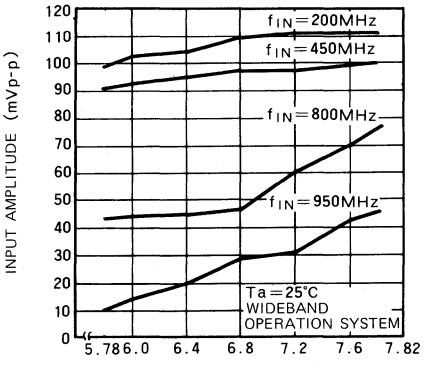
Operation across an even wider frequency range is enabled for the UHF input by setting R_4 between V_{REF2} and GND with $C_1 = 1000pF$, $C_2 = 1000pF$, $C_3 = 1000pF$, $C_4 = 1000pF$, $C_5 \simeq 0.1\mu F$, $C_6 = 0.1\mu F$, $R_1 = 20\Omega$, $R_2 = 33\Omega$, $R_3 = 33\Omega$, $R_4 = 36k\Omega$

TYPICAL CHARACTERISTICS

MINIMUM INPUT AMPLITUDE VS INPUT FREQUENCY RESPONSE



MINIMUM INPUT AMPLITUDE VS SUPPLY VOLTAGE



M54456P

1/64 HIGH SPEED DIVIDER WITH ECL OUTPUT

DESCRIPTION

The M54456P is a semiconductor integrated circuit consisting of a built-in 1/64 high-speed frequency divider with an ECL circuit configuration.

FEATURES

- Ultra-high-speed operation (f_{max} = 1.2GHz)
- Operation at low input amplitude (300mV_{P-P} minimum input amplitude)
- ECL level output
- Two inputs (UHF and VHF)
- TTL level compatible band switching input

APPLICATIONS

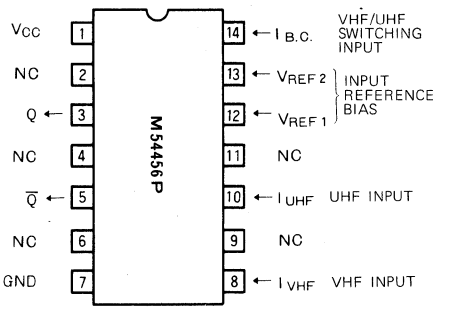
Prescalers for PLL synthesizer TV tuners; digital equipment for consumer and industrial applications

FUNCTION

This 1/64 frequency divider is based on an ECL circuit configuration. When a frequency between 450MHz and 950MHz is applied to the UHF input (I_{UHF}) pin, a 1/64-divided frequency output is obtained. The same output is obtained when a frequency between 80MHz and 350MHz is applied to the VHF input (I_{VHF}) pin. The outputs (Q, $\overline{Q}$) conform to ECL levels.

A wide-band operating system should be used when the UHF input pin is supplied with frequencies ranging from 80MHz to 950MHz.

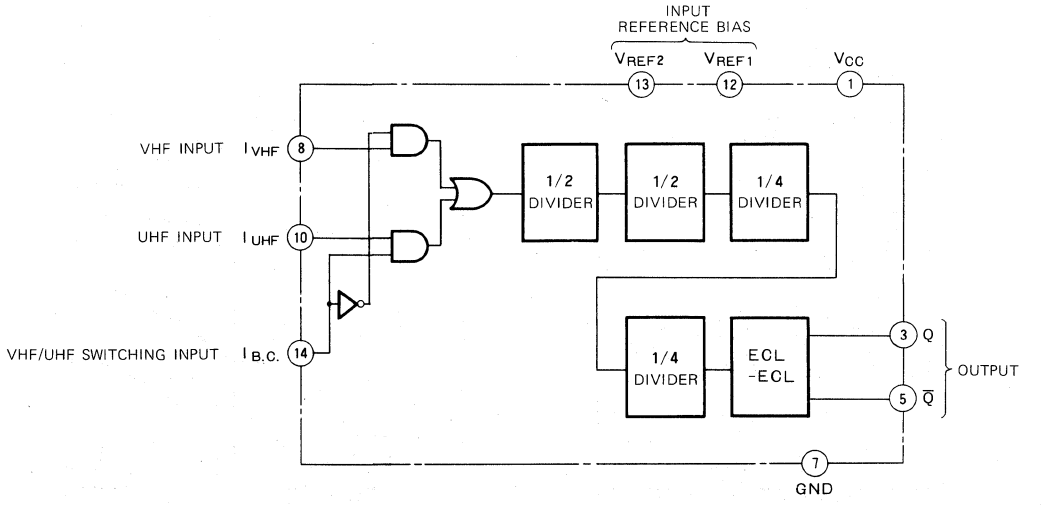
PIN CONFIGURATION



Outline 14P4 NC: NO CONNECTION

When the band switching input ($I_{B.C.}$) pin is high or open, the UHF input (I_{UHF}) pin can be used and when it is low the VHF input (I_{VHF}) pin can be used. Do not supply signals simultaneously to the UHF input (I_{UHF}) and VHF input (I_{VHF}) pins.

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

1/64 HIGH SPEED DIVIDER WITH ECL OUTPUT

ABSOLUTE MAXIMUM RATINGS (Ta = −10 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Condition	Limits	Unit
V_{CC}	Supply voltage		9	V
V_I	Input voltage		2.5	V_{P-P}
$V_{B.C}$	Band switching input voltage		−0.5 ~ +7.2	V
I_O	Output current		−30 ~ +30	mA
Topr	Operating temperature		−10 ~ +75	°C
Tstg	Storage temperature		−55 ~ +125	°C

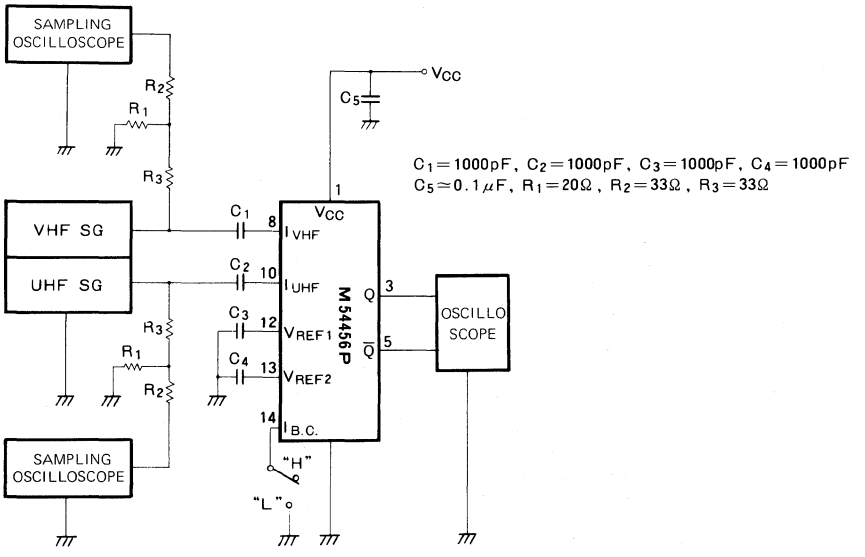
RECOMMENDED OPERATING CONDITIONS (Ta = −10 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	6.1	6.8	7.5	V
I_{OL}	Low-level output current			5	mA

ELECTRICAL CHARACTERISTICS (Ta = −10 ~ +75°C unless otherwise noted)

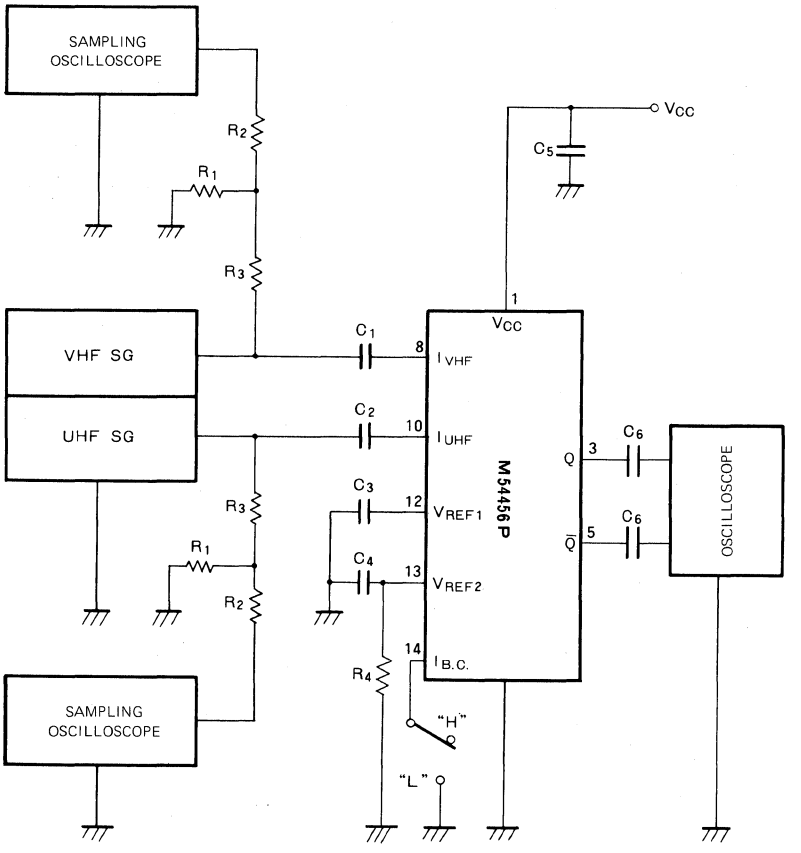
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CC}	Circuit current	V_{CC}=6.8V		68		mA
V_O	Output voltage	V_{CC}=6.8V		0.8		V_{P-P}
V_{BCH}	High-level band switching 2 input voltage		2.5			V
V_{BCL}	Low-level band switching 2 input voltage				0.4	V
V_S	VHF input sensitivity	V_{CC}=6.8V, Ta=25°C f_{IN}=80~350MHz			300	mV_{P-P}
U_{S1}	UHF input sensitivity 1	V_{CC}=6.8V, Ta=25°C f_{IN}=450~950MHz			300	mV_{P-P}
U_{S2}	UHF input sensitivity 2	V_{CC}=6.8V, Ta=25°C f_{IN}=80~350MHz			300	mV_{P-P}
Vmax	VHF maximum input level	f_{IN}=80~350MHz	1			V_{P-P}
Umax	UHF maximum input level	f_{IN}=450~950MHz	1			V_{P-P}

f_{max} TEST CIRCUIT



APPLICATION EXAMPLE

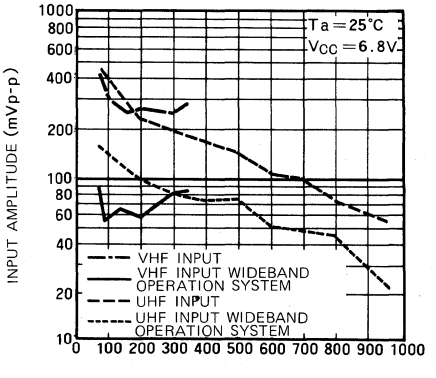
For wide-band operation



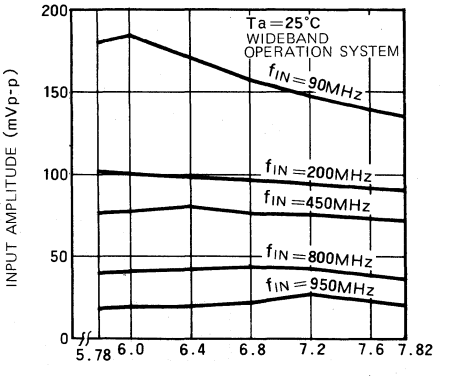
Operation across an even wider frequency range is enabled for the UHF input by setting R_4 between V_{REF2} and GND with $C_1=1000pF$, $C_2=1000pF$, $C_3=1000pF$, $C_4=1000pF$, $C_5=0.1\mu F$, $C_6=0.1\mu F$, $R_1=20\Omega$, $R_2=33\Omega$, $R_3=33\Omega$, $R_4=36k\Omega$

TYPICAL CHARACTERISTICS

MINIMUM INPUT AMPLITUDE VS INPUT FREQUENCY



MINIMUM INPUT AMPLITUDE VS SUPPLY VOLTAGE



MITSUBISHI ELECTRIC

M54457P

1/256 HIGH-SPEED DIVIDER WITH ECL OUTPUT

DESCRIPTION

The M54457P is a semiconductor integrated circuit consisting of a built-in 1/256 high-speed frequency divider with an ECL circuit configuration.

FEATURES

- Extremely high-speed operation (f_{max} = 1.0GHz)
- Operation at low input amplitude (300mVp-p minimum input amplitude)
- ECL level output
- Two inputs (UHF and VHF)
- TTL level compatible bandswitching input

APPLICATIONS

Prescalers for PLL synthesizer TV tuners; digital equipment for consumer and industrial applications.

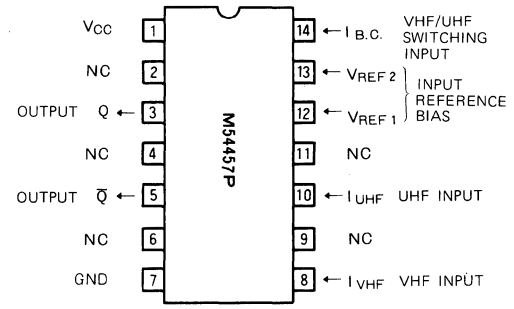
FUNCTION

This divider is based on an ECL circuit configuration. When a frequency between 450MHz and 950MHz is applied to the UHF input (I_{UHF}) pin, a 1/256-divided frequency output is obtained. The same output is obtained when a frequency between 80MHz and 350MHz is applied to the VHF input (I_{VHF}) pin. The outputs (Q, $\overline{Q}$) conform to the ECL level.

A wideband operating system should be used when the UHF input pin is supplied with frequencies ranging from 80MHz to 950MHz.

When the bandswitching input ($I_{B.C}$) pin is high or open, the UHF input (I_{UHF}) pin can be used and when it is a low the VHF input (I_{VHF}) pin can be used. Do not supply signals simultaneously to the UHF input (I_{UHF}) and VHF input (I_{VHF}) pins.

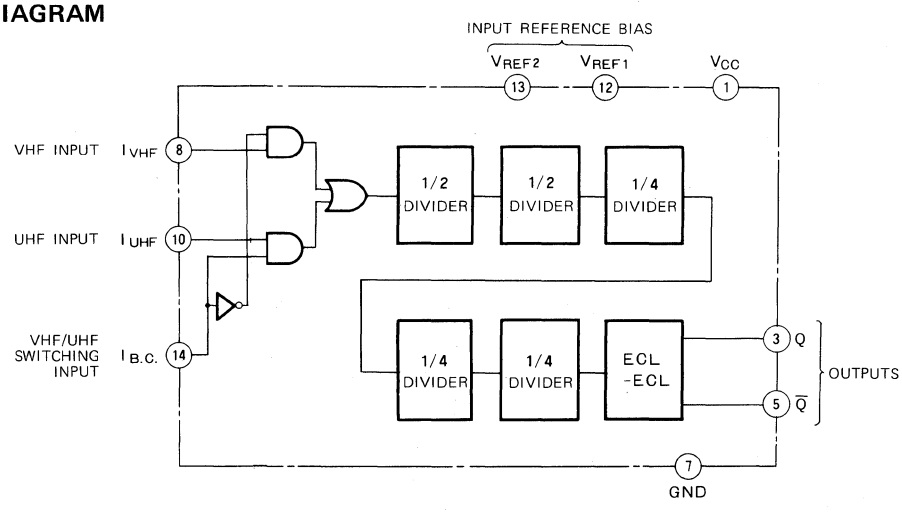
PIN CONFIGURATION (TOP VIEW)



NC: NO CONNECTION

Package Outline 14P4

BLOCK DIAGRAM



1/256 HIGH-SPEED DIVIDER WITH ECL OUTPUT

ABSOLUTE MAXIMUM RATINGS (Ta = −10 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		9	V
V_I	Input voltage		2.5	V_{P-P}
$V_{B,C}$	Band switching input voltage		−0.5 ~ +7.2	V
I_O	Output current		−30 ~ +30	mA
Topr	Operating temperature		−10 ~ +75	°C
Tstg	Storage temperature		−55 ~ +125	°C

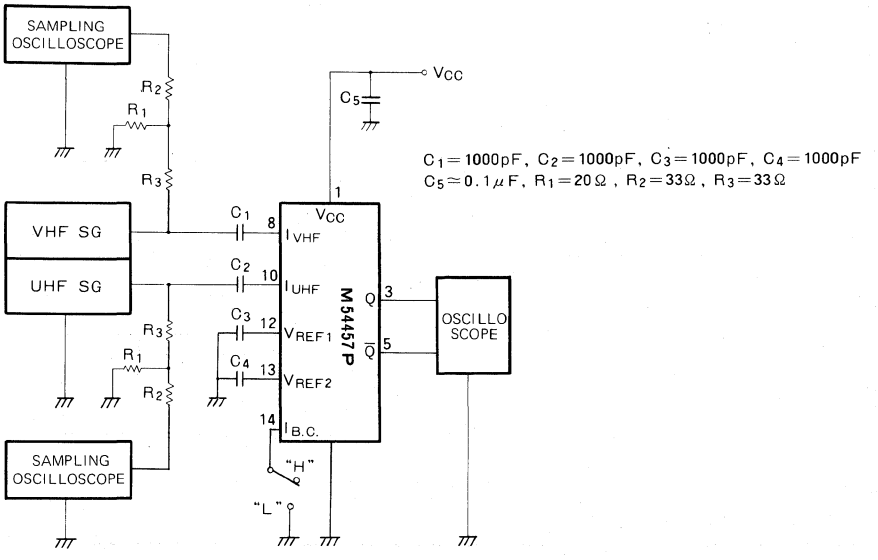
RECOMMENDED OPERATING CONDITIONS (Ta = −10 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	6.1	6.8	7.5	V
I_{OL}	Low-level output current			5	mA

ELECTRICAL CHARACTERISTICS (Ta = −10 ~ +75°C unlews otherwise noted)

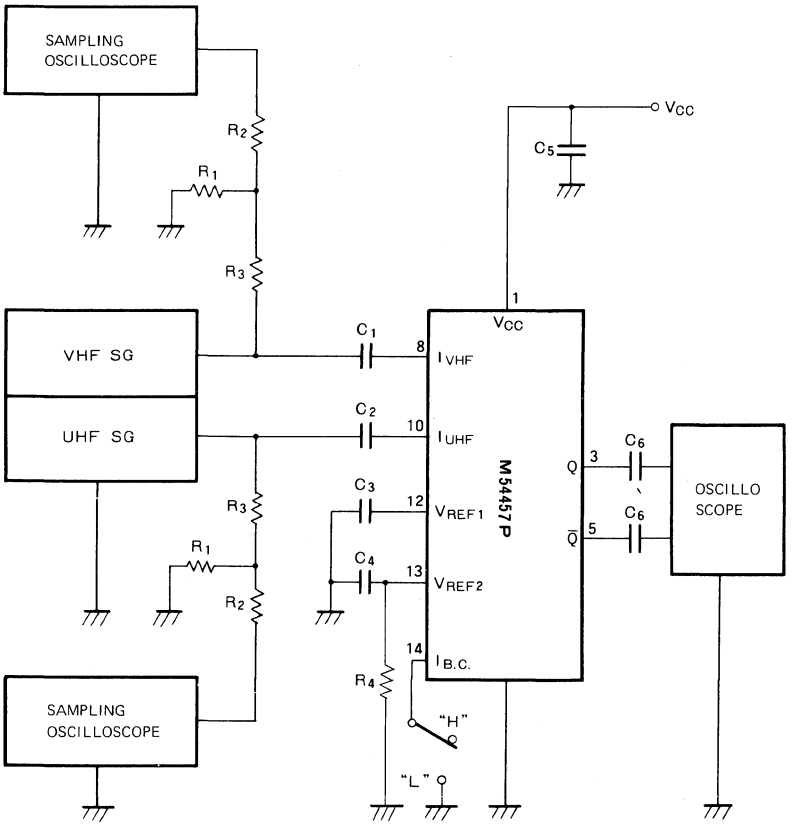
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CC}	Circuit current	V_{CC} = 6.8V		68		mA
V_O	Output voltage	V_{CC} = 6.8V		0.8		V
V_{BCH}	High-level bandswitching input voltage		2.5			V
V_{BCL}	Low level bandswitching input voltage				0.4	V
V_S	VHF input sensitivity	V_{CC} = 6.8V, Ta = 25°C, f_{IN} = 80 ~ 350MHz			300	mV_{P-P}
U_{S1}	UHF input sensitivity 1	V_{CC} = 6.8V, Ta = 25°C, f_{IN} = 450 ~ 950MHz			300	mV_{P-P}
U_{S2}	UHF input sensitivity 2	V_{CC} = 6.8V, Ta = 25°C, f_{IN} = 80 ~ 350MHz			300	mV_{P-P}
Vmax	VHF maximum input level	f_{IN} = 80 ~ 350MHz	1			V_{P-P}
Umax	UHF maximum input level	f_{IN} = 450 ~ 950MHz	1			V_{P-P}

f_{max} TEST CIRCUIT



APPLICATION EXAMPLE

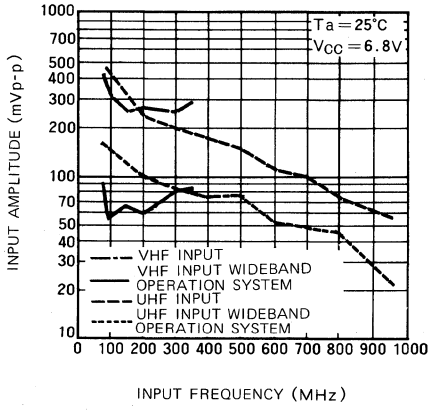
For wide-band operation



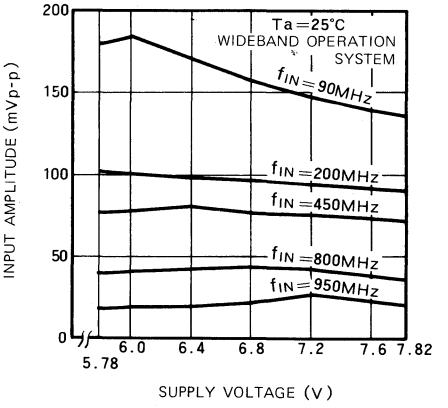
Operation across an even wider frequency range is enabled for the UHF input by setting R_4 between V_{REF2} and GND with $C_1 = 1000pF$, $C_2 = 1000pF$, $C_3 = 1000pF$, $C_4 = 1000pF$, $C_5 = 0.1\mu F$, $R_1 = 20\Omega$, $R_2 = 33\Omega$, $R_3 = 33\Omega$, $R_4 = 36k\Omega$, $R_5 = 1k\Omega$

TYPICAL CHARACTERISTICS

MINIMUM INPUT AMPLITUDE VS INPUT FREQUENCY



MINIMUM INPUT AMPLITUDE VS SUPPLY VOLTAGE



M54462P

1/64, 1/256 HIGH-SPEED DIVIDER

DESCRIPTION

The M54462P is semiconductor integrated circuit consisting of a 1/64, 1/256 high-speed divider using ECL circuit configuration.

FEATURES

- Extremely high-speed operation (f_{max} = 1.0GHz)
- Operates at low input amplitude (100mV p-p minimum input amplitude)
- TTL output level

APPLICATIONS

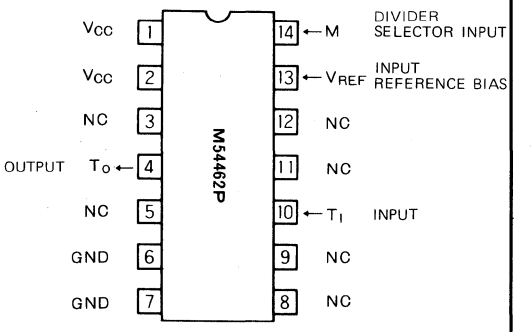
Prescaler for PLL synthesizer type TV tuners. For general use in commercial and industrial digital equipment.

FUNCTION

This divider is bared on an ECL circuit configuration. When a frequency between 80MHz and 950MHz is applied to the input terminal (T_1), this ECL type divider gives division by 1/256 when the selector input M is at low level, and division by 1/64 when the selector input M is high level.

Output T_0 is the TTL output.

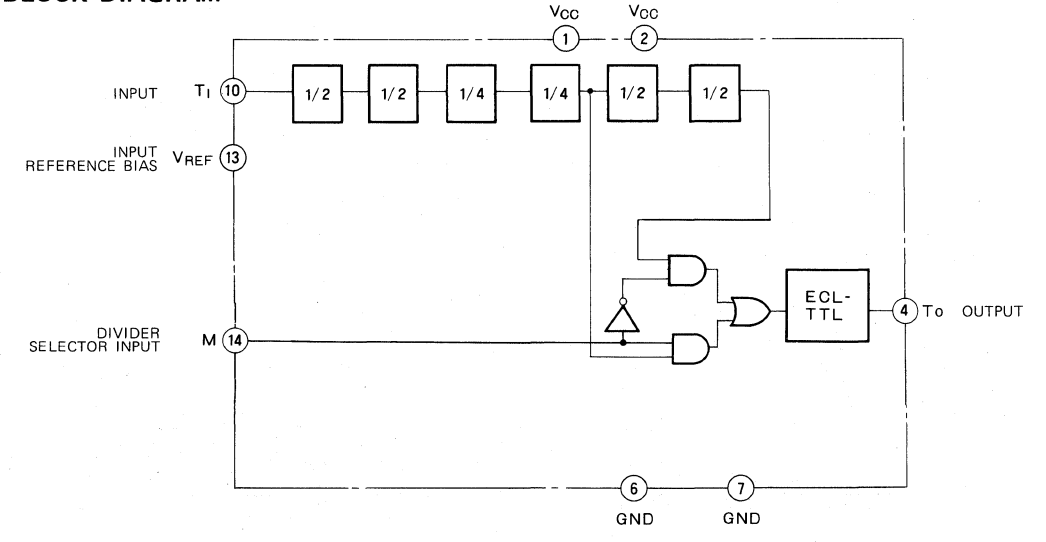
PIN CONFIGURATION (TOP VIEW)



NC : NO CONNECTION

Package Outline 14P4

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS (Ta = −10 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		7	V
V_I	Input voltage		2.5	V_{P-P}
Pc	Power dissipation	Ta = 25°C	1.35	W
Topr	Operating temperature		−10 ~ +75	°C
Tstg	Storage temperature		−55 ~ +125	°C

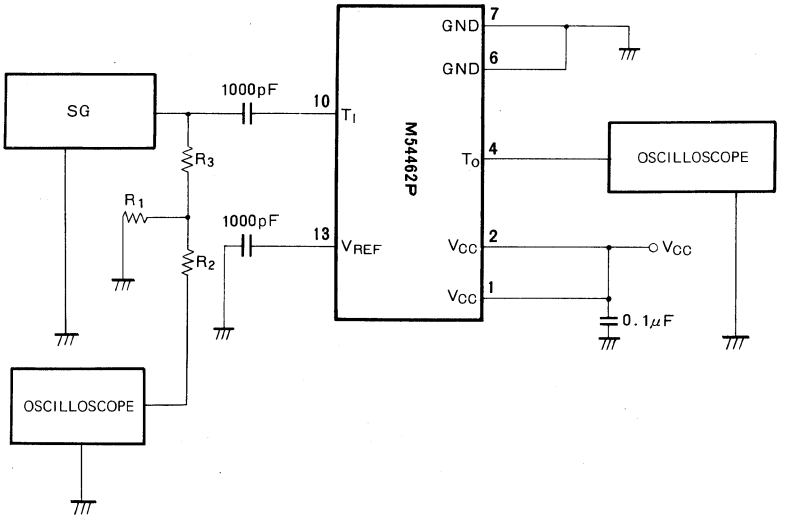
RECOMMENDED OPERATING CONDITIONS (Ta = −10 ~ +75°C, unless otherwise indicated)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.75	5	5.5	V
V_{IN}	Input voltage			600	mV_{P-P}
V_{IH}	High-level input voltage to terminal M			V_{CC}−0.3	V
V_{IL}	Low-level input voltage to terminal M			0.5	V

ELECTRICAL CHARACTERISTICS (Ta = −10 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CC}	Supply current	V_{CC} = 5V	30	50	80	mA
S_I	Input sensitivity	V_{CC} = 5V, Ta = 25°C f_{IN} = 80MHz ~ 950MHz			100	mV_{P-P}
V_{OH}	High-level voltage	V_{CC} = 5V, I_{OH} = −1mA	2.4	3.8		V
V_{OL}	Low-level voltage	V_{CC} = 5V, I_{OL} = 2mA			0.45	V

f_{max} TEST CIRCUIT



M54463P

1/128 HIGH-SPEED DIVIDER WITH ECL OUTPUT

DESCRIPTION

The M54463P is a semiconductor integrated circuit consisting of a high-speed 1/128 divider with ECL output.

FEATURES

- High-speed operation (f_{max} = 1.25GHz)
- Operates with low input amplitudes (300mV_{P-P} minimum input amplitude)
- ECL output levels
- Two inputs (UHF and VHF)
- The band change-over input is TTL compatible

APPLICATIONS

Prescalers for PLL synthesizer type television tuners, general commercial and industrial digital equipment.

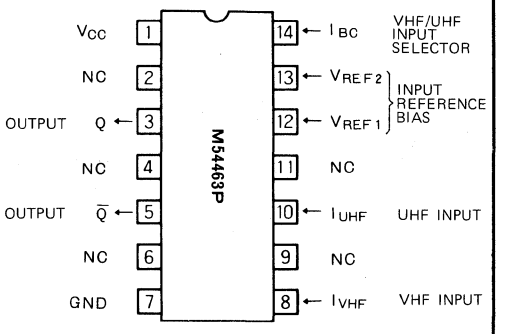
FUNCTION

When a frequency of 450 ~ 950MHz is applied to the UHF input (I_{UHI}), this ECL-type divider outputs a frequency which is divided by 1/128. The outputs Q, $\overline{Q}$, are ECL levels.

When the band change-over input (I_{BC}) is high or open, UHF input, please use wideband operation.

When the bandchange-over input (I_{BC}) is high or open, the UHF input (I_{UHF}) is available, and similarly when I_{BC} is low, the VHF input is available. Note that inputs should not be applied simultaneously to the UHF input (I_{UHF}) and the VHF input (I_{VHF}).

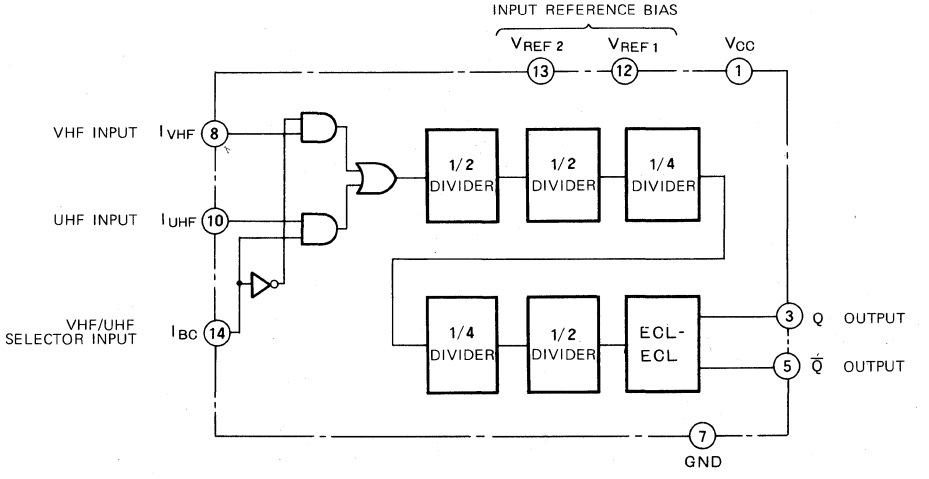
PIN CONFIGURATION (TOP VIEW)



NC : NO CONNECTOIN

Package Outline 14P4

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

1/128 HIGH-SPEED DIVIDER WITH ECL OUTPUT

ABSOLUTE MAXIMUM RATINGS (Ta = −10 ~ +75°C unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		9	V
V_I	Input voltage		2.5	V_{P-P}
V_{BC}	Band change-over input voltage		−0.5 ~ +7.2	V
I_O	Output current		−30 ~ +30	mA
Topr	Operating temperature		−10 ~ +75	°C
Tstg	Storage temperature		−55 ~ +125	°C

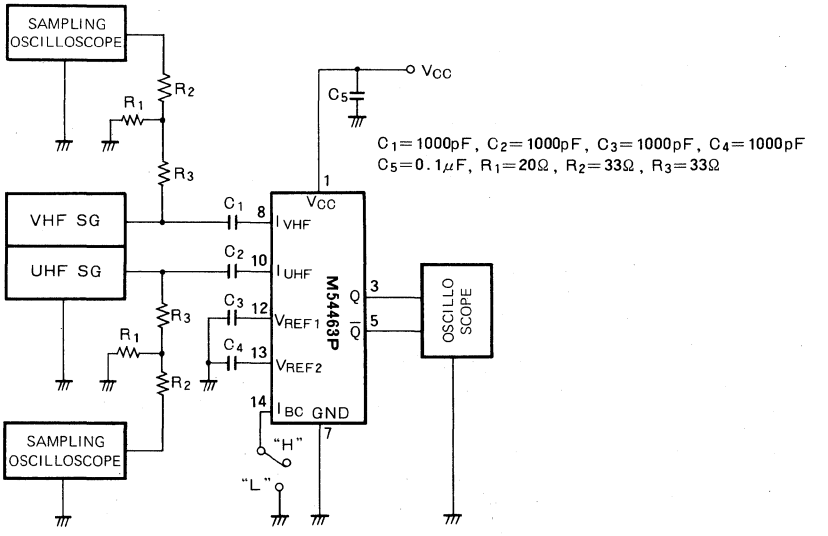
RECOMMENDED OPERATING CONDITIONS (Ta = −10 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	6.1	6.8	7.5	V
I_O	Input voltage			5	mA

ELECTRICAL CHARACTERISTICS (Ta = −10 ~ +75°C, unless otherwise noted)

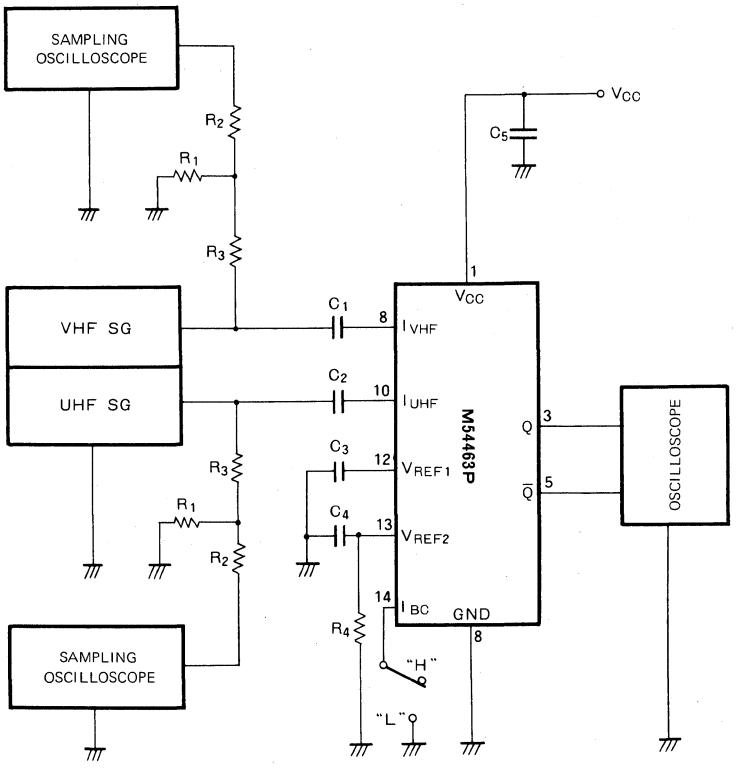
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CC}	Circuit current	V_{CC}=6.8V		68		mA
V_O	Output amplitude	V_{CC}=6.8V		0.8		V
V_{BCH}	Band change-over high-level voltage		2.5			V
V_{BCL}	Band change-over low-level voltage				0.4	V
V_S	VHF input sensitivity				300	mV_{P-P}
U_{S1}	UHF input sensitivity 1				300	mV_{P-P}
U_{S2}	UHF input sensitivity 2				300	mV_{P-P}
Vmax	Maximum VHF input level	f_{IN}=80 ~ 350MHz	1			V_{P-P}
Umax	Maximum UHF input level	f_{IN}=450 ~ 950MHz	1			V_{P-P}

f_{max} TEST CIRCUIT



APPLICATION EXAMPLE

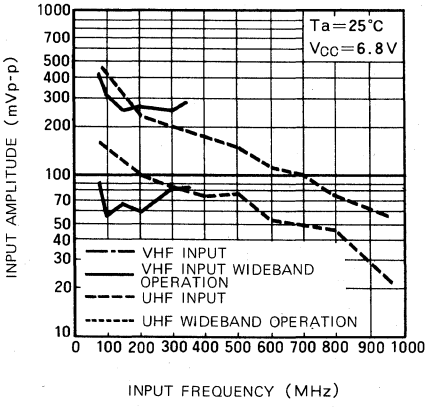
Wideband operation



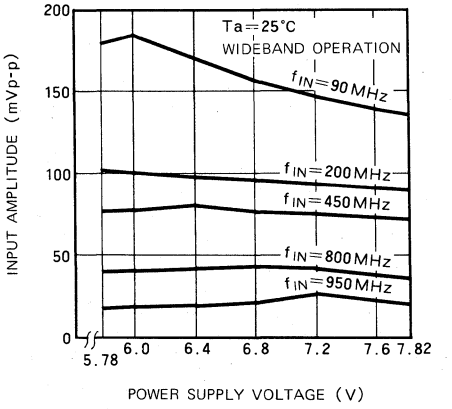
With C_1= 1000pF, C_2= 1000pF, C_3= 1000pF, C_4= 1000pF, C_5=0.1μF, R_1=20Ω, R_2=33Ω R_3=33Ω, R_4=36kΩ, R_5= 1kΩ, the insertion of R_4 between V_{REF2} and ground enables the UHF input to be used over a much wider frequency range for wideband operation.

TYPICAL CHARACTERISTICS

MINIMUM INPUT AMPLITUDE VS INPUT FREQUENCY



MINIMUM INPUT AMPLITUDE VS POWER SUPPLY VOLTAGE



M54817P

VTR SYNCHRONOUS SIGNAL GENERATOR

DESCRIPTION

The M54817P is an I^2L semiconductor integrated circuit consisting of a video synchronous signal generator. It includes a quartz oscillator and divider circuits.

FEATURES

- Built-in quartz oscillator (reference frequency 3.58MHz)
- Four outputs; horizontal sync, vertical sync, frame sync signals and 2MHz.
- Individual reset for horizontal sync, vertical sync, and frame sync signals
- Built-in regulated power supply

APPLICATION

VTR, Video cameras

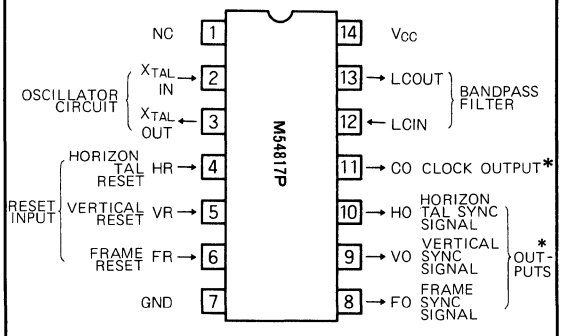
FUNCTION

The M54817P is designed for use in Video equipment as a vertical and horizontal sync signal generator. It includes a 3.58MHz crystal oscillator which used in conjunction with an external bandpass filter and internal dividers provides a 2.04545MHz clock signal, a 15.734kHz horizontal sync signal, a 59.94Hz vertical sync signal, and 29.97Hz frame synchronous signal outputs.

All outputs are open collector and are capable of syncing 1.6mA current. The horizontal, vertical, and frame sync signals have individual resets.

An internal regulated power supply is provided, making the M54817P usable over a wide range of supply voltages for stable, accuracy sync signal generation.

PIN CONFIGURATION (TOP VIEW)

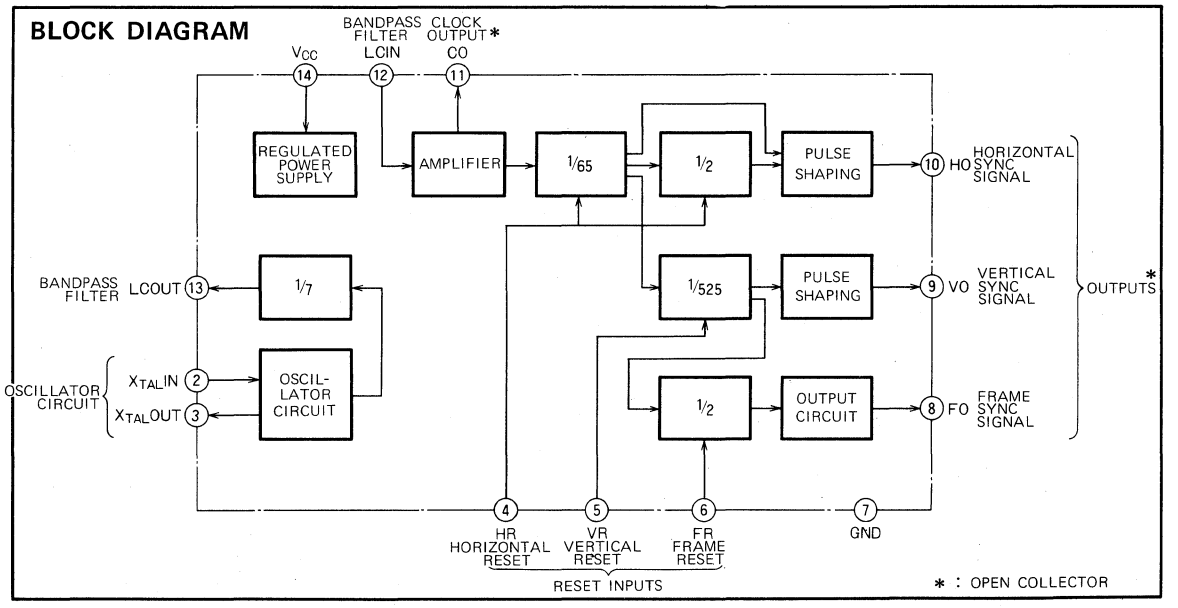


NC : NO CONNECTION
* : OPEN COLLECTOR OUTPUT

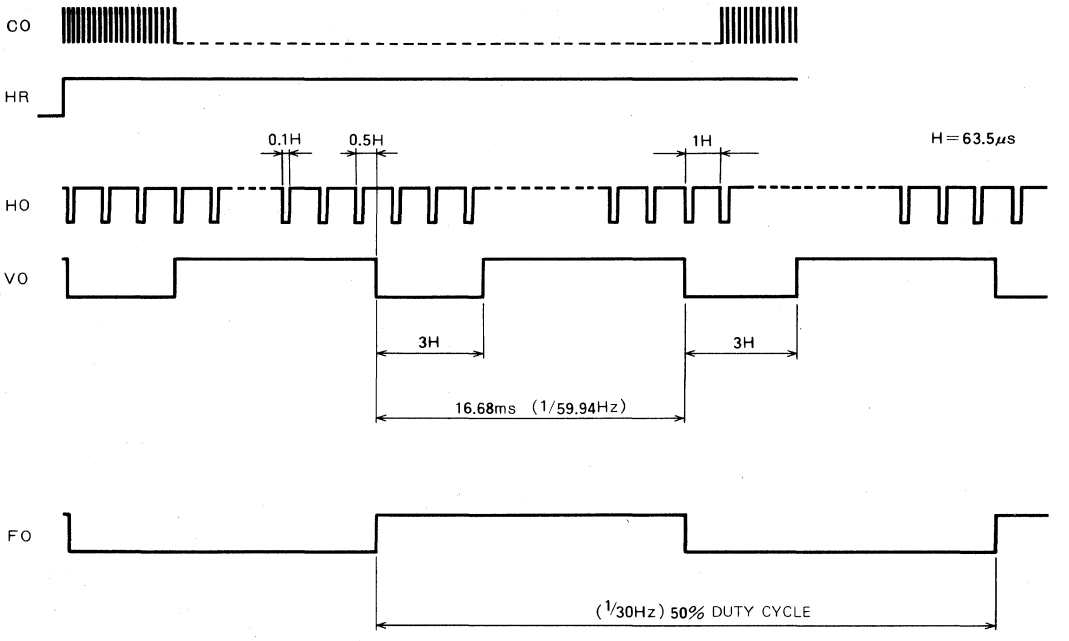
Package Outline 14P4

The external bandpass filter, requiring five capacitors and two inductors is used to provide fourth harmonic output with no amplitude variations. Amplifiers and dividers are then used to provide a 3.58MHz chroma signal, a horizontal synchronous signal at 3.58 x (2/455) MHz and a vertical synchronous signal at 3.58 x (2/455)x (2/525) MHz.

BLOCK DIAGRAM



TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Condition	Limits	Unit
V_{CC}	Supply voltage		7	V
V_I	Input voltage		5.5	V
V_O	Output voltage		5.5	V
T_{opr}	Operating temperature		−20∼+75	℃
T_{stg}	Storage temperature		−55∼+125	℃

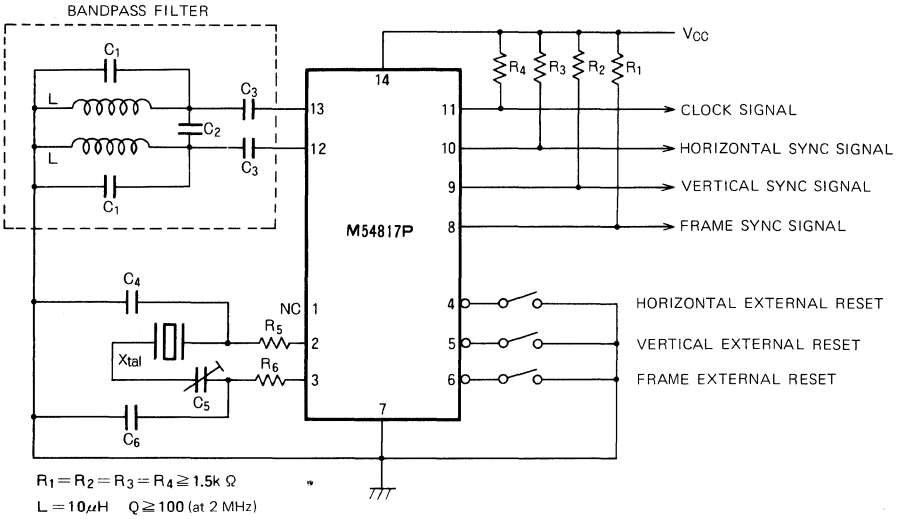
RECOMMENDED OPERATING CONDITIONS (Ta=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4	5	6	V
I_{OL}	Circuit current			1.6	mA

ELECTRICAL CHARACTERISTICS (Ta=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage (reset input)					V
I_{IL}	Low-level input current (reset input)	V_{CC}=6V, V_I=0.2V			−0.3	mA
I_{OH}	High-level output current	V_{CC}=4V, V_O=5.5			25	μA
V_{OL}	Low-level output voltage	V_{CC}=6V, I_{OL}=1.6mA			0.4	V
t_{PW}	Reset pulse width		300			ns
t_{PLH}	Low to high output transition time, from input reset to output	V_{CC}=6V			500	ns
I_{CC}	Circuit current	V_{CC}=6V		17	25	mA

APPLICATION EXAMPLE



$R_1 = R_2 = R_3 = R_4 \geqq 1.5k\,\Omega$

$L = 10\mu H$ $Q \geqq 100$ (at 2 MHz)

$C_1 = 560pF$ $C_2 = 15pF$ $C_3 = 30pF$

$1/2\pi\sqrt{LC_1} = 2.05MHz$

$C_4 = 220pF$ $C_5 = 150pF$ $C_6 = 47pF$

$R_5 = 220\,\Omega$ $R_6 = 330\,\Omega$

Crystal specifications

Resonant frequency 3.579545MHz
Effective resistance 100Ω, max.
Load capacitance 16pF

M54818L

1/59718 VTR DIVIDER

DESCRIPTION

The M54818L is an I^2L semiconductor integrated circuit consisting of a frequency divider used to derive the vertical synchronous signal from the TV chroma signal.

FEATURES

- Built-in high input sensitivity amplifier
- Divided outputs (three outputs)
  Vertical sync signal
  output ..... Division ratio: 1/59718 (59.94Hz)
  Frame sync signal output 29.97Hz
  Tuner output (with pulse shaping circuit)..... 3.58MHz
- Setting function

APPLICATIONS

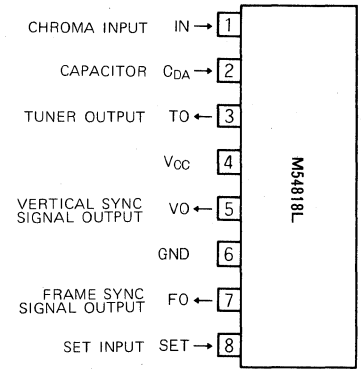
VTR, Video cameras

FUNCTION

The M54818L is intended for use as a VTR vertical synchronous signal generator. It consists of an amplifier and 17 stages of divider circuits. The input circuit makes use of a differential amplifier which operates on signals as low as 150mVp-p. The output is derived by dividing the 3.58MHz chroma input signal using 17 stages of division to obtain a 59.94Hz vertical synchronous signal. In addition, the chroma input is pulse shaped to provide a 3.58MHz tuner output signal and a 30Hz frame synchronous signal output.

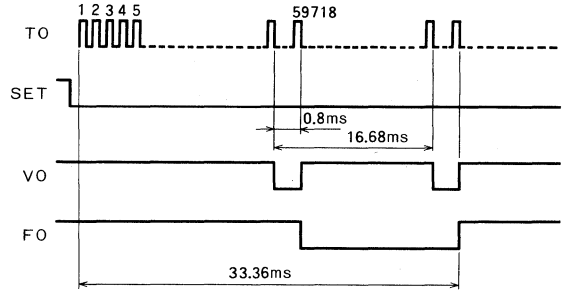
All outputs are totem pole type capable of sourcing or sinking up to 2mA. An input is provided for direct syncing of the vertical sync output and the frame sync output. When the set input transits from low-level to high-level both outputs are set to high-level.

PIN CONFIGURATION (TOP VIEW)

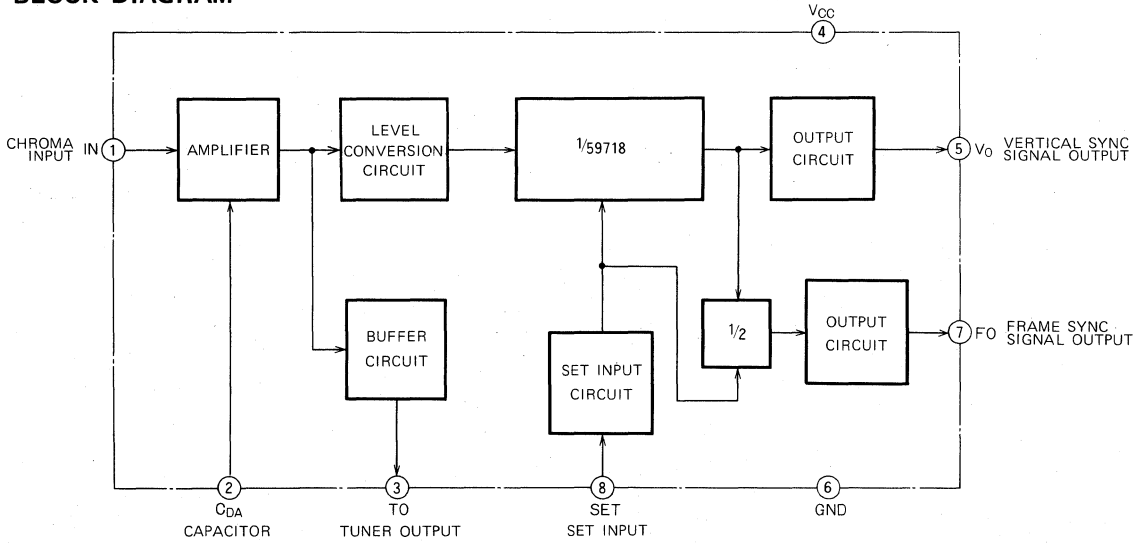


Package Outline 8P5

TIMING DIAGRAM



BLOCK DIAGRAM



MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS (Ta= 0 ~75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		8	V
V_I	Input voltage (IN input pin)		6	V
V_O	Output voltage		V_{CC}	V
T_{opr}	Operating temperature		0 ~75	℃
T_{stg}	Storage temperature		−55~ +125	℃

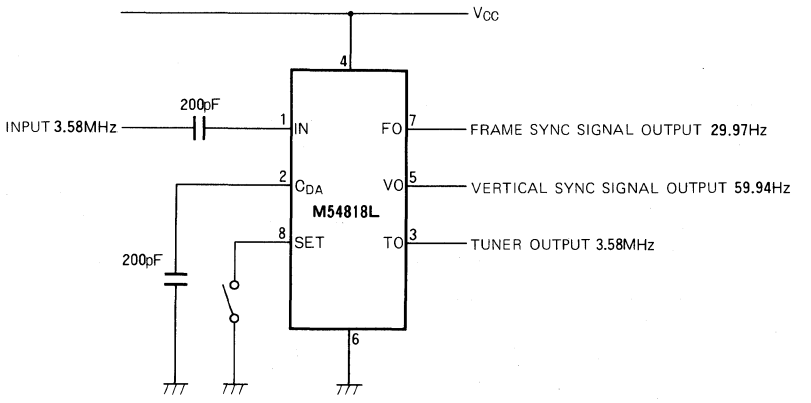
RECOMMENDED OPERATING CONDITIONS (Ta=25℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	6	6.5	7	V
V_I	Input voltage	0.15			V_{P-P}
I_{OL}	Low-level output current			2	mA
$f_{(IN)}$	Input frequency		3.58		MHz

ELECTRICAL CHARACTERISTICS (Ta=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_I	Input voltage (IN input)	V_{CC}=6.5V, $f_{(IN)}$=3.58MHz	0.15		1	V
I_{IL}	Low-level input current (SET input)	V_{CC}=6.5V, V_{IL}=0.2V			−100	μA
I_{IH}	High-level input current (SET input)	V_{CC}=6.5V, V_{IH}=6.5V			10	μA
V_{OH}	High-level output voltage	V_{CC}=6V, V_{IH}=6V, I_{OH}=−0.4mA	2.4			V
I_{OH}	High-level output current	V_{CC}=6V, V_{IH}=6V, V_O=0.85V	−1.6			mA
V_{OL}	Low-level output voltage	V_{CC}=6V, I_{OL}=2mA			0.2	V
$t_{PW(S)}$	Set pulse width			280		ns
t_{PLH}	Output propagation time from low to high-level (from input set to output VO-FO)	V_{CC}=6.5V		500		ns
I_{CC}	Circuit current	V_{CC}=6.5V, $V_{I(IN)}$=0.3V_{P-P} $f_{(IN)}$=3.58MHz		15	22	mA

APPLICATION EXAMPLE



M54819L

PRESETTABLE DIVIDER

DESCRIPTION

The M54819L is an I^2L semiconductor integrated circuit consisting of a divider circuit which provides seven types of frequency divide ratios.

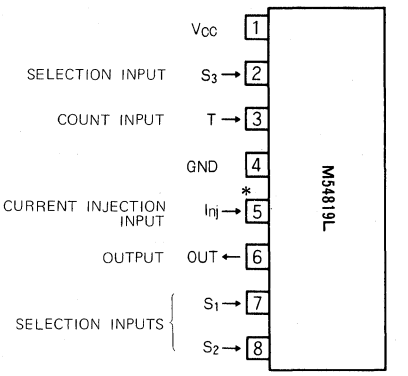
FEATURES

- Built-in regulated power supply
- Maximum operating frequency f_{max} = 3.0MHz
- Reset function
- Selectable divide ratio
  1/2, 1/4, 1/6, 1/8, 1/10, 1/12, or 1/16
- Wide supply voltage range (V_{CC} = 4.0 ~ 14.5V)
- Low power consumption (I_{CC} = 3mA for V_{CC} = 14.5V)

APPLICATIONS

General consumer equipment, frequency dividers

PIN CONFIGURATION (TOP VIEW)



Package Outline 8P5

FUNCTION

The M54819L is designed for use as a general purpose frequency divider and consists of a regulated power supply, and dividers with divide ratios of 1/3, 1/5, and 1/16.

The output frequency division ratio is selectable and determined by a 3-input binary coded division ratio input. This allows the selection of one out of seven division ratios (1/2, 1/4, 1/6, 1/8, 1/10, 1/12, or 1/16). The output is a current source/sink type output capable of sourcing 100μA and sinking 1.6mA.

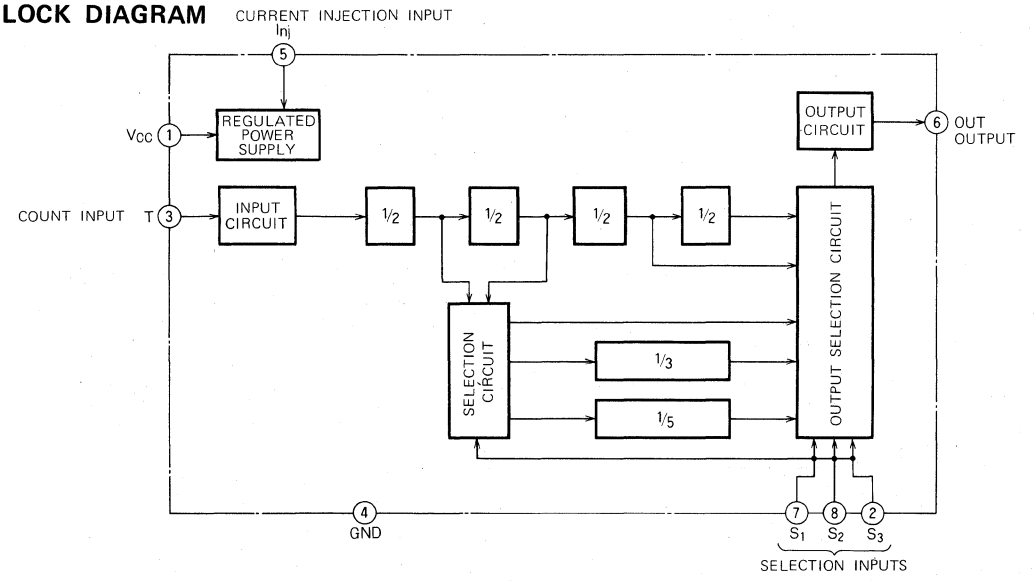
The built-in regulated power supply operates over a wide voltage range from 4.0 to 14.5V. A current injection input is provided to increase operating speed. By supplying this pin with current, the input count frequency can be raised to a maximum of 3MHz.

Resetting is accomplished by setting all the division ratio inputs to high-level, whereupon the internal divider circuits are cleared, the output going to low-level.

PRESETTABLE FUNCTION TABLE

Selection inputs	S_1	H	H	H	L	L	L	H	L
	S_2	H	L	H	H	H	L	L	L
	S_3	H	H	L	H	L	H	L	L
Output divide ratio		Reset	1/2	1/4	1/6	1/8	1/10	1/12	1/16

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Conditions	Limits	Unit
V_{CC}	Supply voltage			15	V
V_I	Input voltage	Count input T		4	V
		Selection inputs S_1, S_2, S_3		15	V
V_O	Output voltage			6	V
T_{opr}	Operating temperature			−20 ~ +75	℃
T_{stg}	Storage temperature			−55 ~ +125	℃

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75℃, unless otherwise noted)

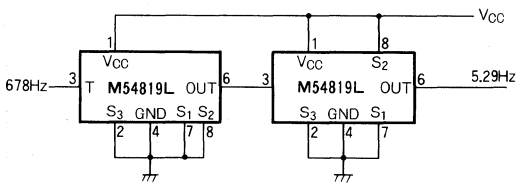
Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4		14.5	V
I_{OL}	Low-level output current			1.6	mA

ELECTRICAL CHARACTERISTICS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{IH}	High-level input voltage	Count input T		0.9			V
		Selection inputs S_1, S_2, S_3		2			V
V_{IL}	Low-level input voltage	Count input T				0.3	V
		Selection inputs S_1, S_2, S_3				0.6	V
V_{OH}	High-level output voltage		V_{CC}=7V, I_{OH}=−0.1mA	2.4			V
			V_{CC}=4V, I_{OH}=−0.1mA	0.8			V
V_{OL}	Low-level output voltage		V_{CC}=7V, I_{OL}=1.6mA			0.4	V
I_{IH}	High-level input current	Count input T	V_{CC}=14.5V, V_I=1V			1.5	mA
		Selection inputs S_1, S_2, S_3	V_{CC}=14.5V, V_I=14.5V			100	μA
I_{IL}	Low-level input current	Count input T	V_{CC}=14.5V, V_I=0.2V			−10	μA
		Selection inputs S_1, S_2, S_3	V_{CC}=14.5V, V_I=0V			−100	μA
I_{OS}	Output short-circuit current		V_{CC}=14.5V, V_O=0V	−0.1		−1	mA
I_{CC}	Circuit current		V_{CC}=14.5V, V_I=V_{CC} (pins 2, 7, 8)		3	5	mA

APPLICATION EXAMPLE

Capstan motor control application (1/128 divider)



M58478P,M50121P,M50122P

17-STAGE OSCILLATOR/DIVIDER

DESCRIPTION

The M58478P, M50121P and M50122P are semiconductor integrated circuits which use aluminum-gate CMOS technology. The M58478P produces a frequency of 1/59719 or 1/88672, the M50121P produces a frequency of 1/58239 or 1/61425, and the M50122P produces a frequency of 1/86118 or 1/92077 of the input frequency.

FEATURES

- Usable as a crystal oscillator circuit
- Capable of handling small-amplitude input signals as low as $0.3V_{PP}$
- Frequency-dividing ratio selected through pin N
- Reset function
- Produces a shaped-waveform output of the same frequency as the input signal or oscillation output
- Derives a vertical scanning frequency from TV color subcarrier

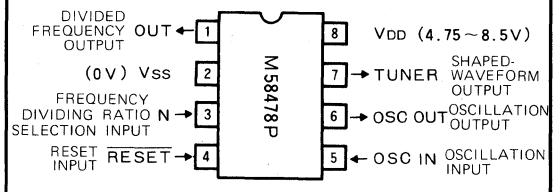
APPLICATION

Frequency divider for VTR equipment

FUNCTION

The M58478P, M50121P and M50122P have a programmable counter consisting of a 17-stage binary frequency divider which provides one of two frequency-dividing ratios as selected by the state of the N input.

PIN CONFIGURATION (TOP VIEW)

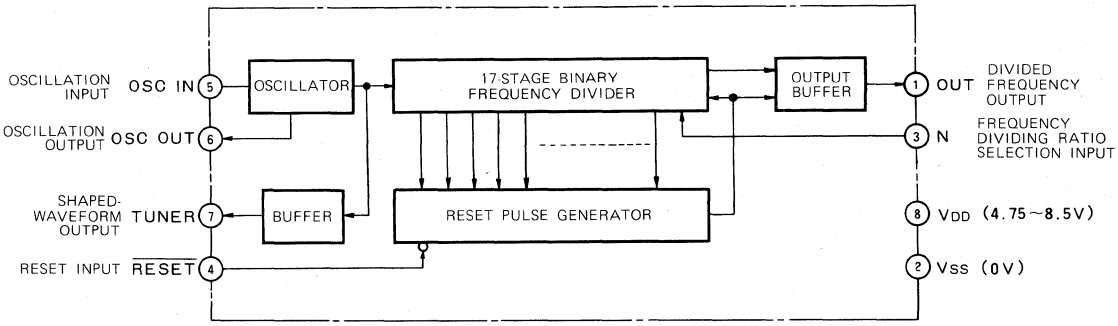


Outline 8P4 (M58478P)
(M50121P)
(M50122P)

Table 1 Input versus output frequencies

Type	Input frequency (MHz)	State of the N input	Output frequency (Hz)
M58478P	3.579545	H(open)	59.94
	4.433618	L	50.00
M50121P	3.579545	H(open)	61.46
		L	58.28
M50122P	4.433618	H(open)	51.48
		L	48.15

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

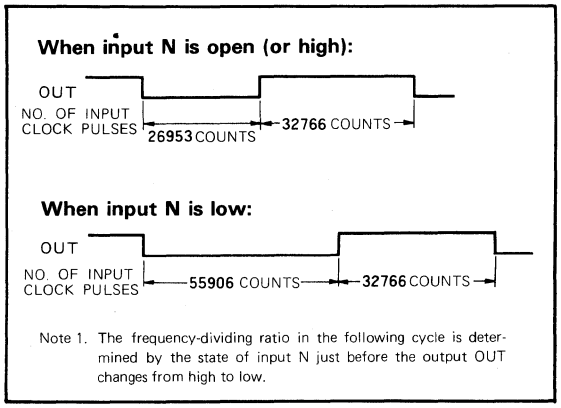
FUNCTIONAL DESCRIPTION

Crystal Oscillator

A crystal oscillator is obtained by connecting a quartz resonator element between pins OSC IN and OSC OUT, and capacitances C_{LI} and C_{LO} between the two pins and V_{SS} (the feedback resistor is contained on-chip). A built-in amplifier at the OSC IN pin enables even small amplitude signals to be input through a coupling capacitor C_C.

Output Frequency

The frequency dividing ratio depends on the state of the N input. Table 2 summarizes the frequency dividing ratios and duty cycles as they are related to this N input. An example of a divided frequency output waveform is shown in Fig. 1.



Note 1. The frequency-dividing ratio in the following cycle is determined by the state of input N just before the output OUT changes from high to low.

Fig. 1 Waveforms of divided-frequency output (In the case of M58478P)

A shaped-waveform output of the same frequency as the input signal or oscillation frequency is available at the TUNER output.

Reset Function

When the $\overline{\text{RESET}}$ input is changed from high to low (edge triggered, active low input), the output OUT changes to low.

Pull-up Resistance

Pull-up resistors are provided at inputs N and $\overline{\text{RESET}}$, eliminating the need for external resistors. The standard resistance of the pull-up resistor is 20KΩ.

Frequency Dividing Ratio

The frequency-dividing ratio is determined by the data input of the programmable counter consisting of a 17-stage binary divider.

Special Frequency Dividing Ratios

It is possible to modify the frequency dividing ratios on special order. By changing one of the manufacturing processes, the data input of the programmable counter consisting of a 17-stage binary divider can be changed to enable any frequency-dividing ratio from 5 to 131071 ($=2^{17}-1$).

Table 2 Frequency-dividing ratios

Type	State of the N input	Frequency-dividing ratio	Divided frequency output low-level period	Divided frequency output high-level period
M58478P	H	59719	26953	32766
	L	88672	55906	32766
M50121P	H	58239	25473	32766
	L	61425	28659	32766
M50122P	H	86118	53352	32766
	L	92077	59311	32766

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{DD}	Supply voltage	When respect to V_{SS}	−0.3 ~ 9	V
V_I	Input voltage		$V_{SS} \leqq V_I \leqq V_{DD}$	V
Pd	Maximum power dissipation	Ta = 25°C	250	mW
Topr	Operating temperature		−30 ~ 70	°C
Tstg	Storage temperature		−40 ~ 125	°C

RECOMMENDED OPERATING CONDITIONS (Ta = −30 ~ 70°C, unless otherwise noted)

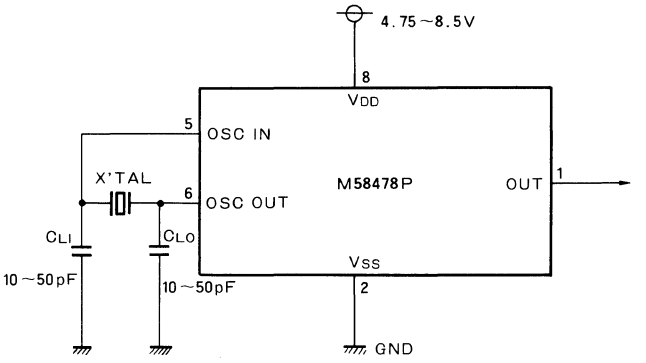
Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{DD}	Supply voltage	4.75		8.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	V_{DD}-0.5			V
V_{IL}	Low-level input voltage			0.5	V
V_I	Oscillation input amplitude voltage	0.3			V_{PP}
f	Input frequency with input N high		3.58	5.5	MHz
	Input frequency with input N low		4.43	5.5	MHz

ELECTRICAL CHARACTERISTICS (Ta = 25°C, V_{DD} = 6.5V, V_{SS} = 0V, f_{IN} = 4.5MHz, unless otherwise noted)

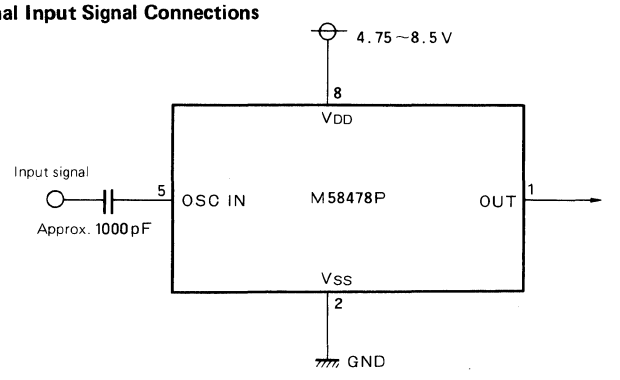
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{DD}	Supply voltage	Ta = −30 ~ 70°C	4.75		8.5	V
I_{DD}	Supply current	N and $\overline{RESET}$ inputs and outputs open			5	mA
V_{IH}	High-level input voltage		V_{DD}-0.5			V
V_{IL}	Low-level input voltage				0.5	V
V_{OH}	High-level output voltage		V_{DD}-0.5			V
V_{OL}	Low-level output voltage				0.5	V
I_{OH}	High-level output current	$V_O = V_{SS}$	−2			mA
I_{OL}	Low-level output current	$V_O = V_{DD}$	2			mA
R_I	Pull-up resistance, N and $\overline{RESET}$ inputs			20		kΩ
VI	Oscillation input amplitude voltage	V_{DD} = 4.75V	0.3			V_{PP}
f_{MAX}	Maximum operating frequency	V_{DD} = 4.75V	5.5			MHz

APPLICATION EXAMPLES

(1) Crystal Oscillator (with built-in feedback resistance)



(2) External Input Signal Connections



M58479P, M58482P

CMOS COUNTER/TIMERS

DESCRIPTION

The M58479P and M58482P are electronic timer ICs developed by aluminum-gate CMOS technology. Use of these ICs makes possible timer devices without mechanical elements, which have reduced power dissipation, superior reliability, and higher noise immunity. The M58479P is specifically designed for high noise immunity while the M58482P particularly features low power dissipation.

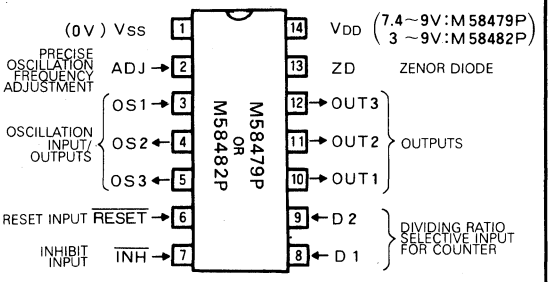
FEATURES

- Low power dissipation
  M58479P: 2mW (typ), 7.5mW (max)
  M58482P: 200μW (typ), 750μW (max)
- Superior noise immunity
- Single power supply with a zenor diode
- Internal RC oscillator
- Precise oscillation frequency regulating capability
- Extremely broad time-delay range (50ms~4800h)
- Time-delay settable to 10, 60, or 600 times fundamental time (1024 times oscillation period)
- M58479P has automatic-reset function during power engagement
- Built-in reset and inhibit functions
- Residual time display possible by adding Mitsubishi's M53290P and M53242P IC

APPLICATIONS

- Electronic timer or counter with broad time-delay range (50ms~4800h)

PIN CONFIGURATION (TOP VIEW)



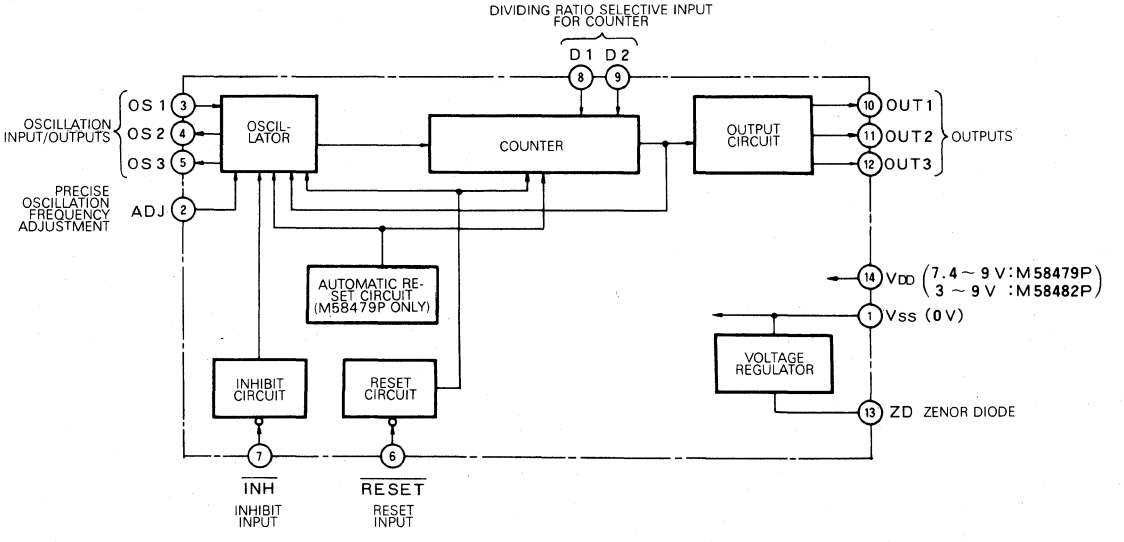
Outline 14P4

FUNCTION

These devices make possible extremely long clock performance, by counting pulse signals from the RC oscillator. It has precise oscillation frequency adjustment, automatic-reset, reset, and inhibit functions.

There are three outputs. When the time duration is up, OUT1 turns from low to high and OUT2 from high to low. OUT3 can be connected to M53290P and M53242P TTLs for residual time display.

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

FUNCTIONAL DESCRIPTION

Voltage Regulator

A zenor diode is on-chip, making it easy to obtain a constant voltage regulator circuit. Since the zenor diode terminal (ZD) is independent of the power terminal (V_{DD}), it can be used as a constant voltage power supply for the total system.

Oscillator

Oscillation is obtained by connecting an external resistor (feedback resistor R_{FC}) between terminals OS1 and OS3 and an external capacitor (oscillation capacitor C_{FC}) between terminals OS1 and OS2. The values of the external resistor and capacitor can then be changed to vary the oscillation period and thus change the time delay. Oscillation period T_0 is obtained by the following equation:

$$T_0 = -R_{FC} \cdot C_{FC} \left\{ \ln \frac{V_{TR}}{V_{DD}+V_{BE}} + \ln \frac{V_{DD}-V_{TR}}{V_{DD}+V_{BE}} \right\} \cdots (1)$$

Where,

- R_{FC} : Resistance of external resistor
- C_{FC} : Capacitance of external capacitor
- V_{TR} : Transition voltage of the first inverter in the oscillation circuit
- V_{DD} : Supply voltage
- V_{BE} : Forward rising voltage of the diode in terminal OS1 (0.3~0.7V)

Automatic-Reset Function

The M58479P has a power-supply voltage-detection circuit on-chip, so that the counter is automatically reset by the rising edge of the supply voltage when power is turned on. The reset is then released, making the oscillator ready to function and the counter ready to start counting.

The M58482P can also be provided with the same automatic-reset function by connecting capacitor between terminals $\overline{RESET}$ and V_{SS}.

Reset Function

When the $\overline{RESET}$ input turns low (V_{SS}), oscillation of the oscillator can be stopped and the counter reset.

Inhibit Function

When terminal $\overline{INH}$ turns low (V_{SS}) while the timer is in action, the oscillation halts. When input $\overline{INH}$ is turned high or returned to OPEN afterwards, it starts to count residual time.

Counter

This counter consists of an 11-stage 1/2 frequency divider, a 2-stage 1/10 frequency divider and a 1-stage 1/6 frequency divider. As shown in the table below, timer duration can be changed by varying the number of pulses counted according to the combination of the input levels on terminals D1 and D2.

D1	D2	Number of pulses counted	Time delay	Typical time delay applied
H	H	1024	T_1	1 min
L	H	1024×10	$T_1 \times 10$	10 min
H	L	$1024 \times 10 \times 6$	$T_1 \times 10 \times 6$	1h
L	L	$1024 \times 10 \times 6 \times 10$	$T_1 \times 10 \times 6 \times 10$	10h

Where, $T_1 = T_0 \times 1024$

T_0 is the value obtained from equation (1)

Output Circuits

The chips have three outputs: OUT1 changes from low to high and OUT2 from high to low as soon as the time duration is up. Either can be used to drive a transistor by connecting it to the transistor base. OUT1 can drive a thyristor when connected to the thyristor gate.

OUT3 is an open-drain output with period 1/8 of the time delay, and can be used to drive a TTL in a separate (5V) power supply line. Thus, if a M53290P counter and a M53242P binary-to-decimal decoder are connected to OUT3, with their output connected to a light-emitting diode, residual time will be displayed on the LED. When not in use, OUT3 should be connected to V_{SS}.

Fine Adjustment of Oscillation Period

A variable resistor can be connected between terminals ADJ and V_{SS}, enabling precise adjustment of the period of the oscillator. However, when not used for fine adjustment, ADJ should be connected to V_{SS}.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{DD}	Supply voltage	With respect to V_{SS}	−0.3～9.5	V
V_I	Input voltage		$V_{SS} \leqq V_I \leqq V_{DD}$	V
Pd	Maximum power dissipation	Ta=25°C	250	mW
Topr	Operating free-air temperature range		−30～75	°C
Tstg	Storage temperature range		−40～125	°C

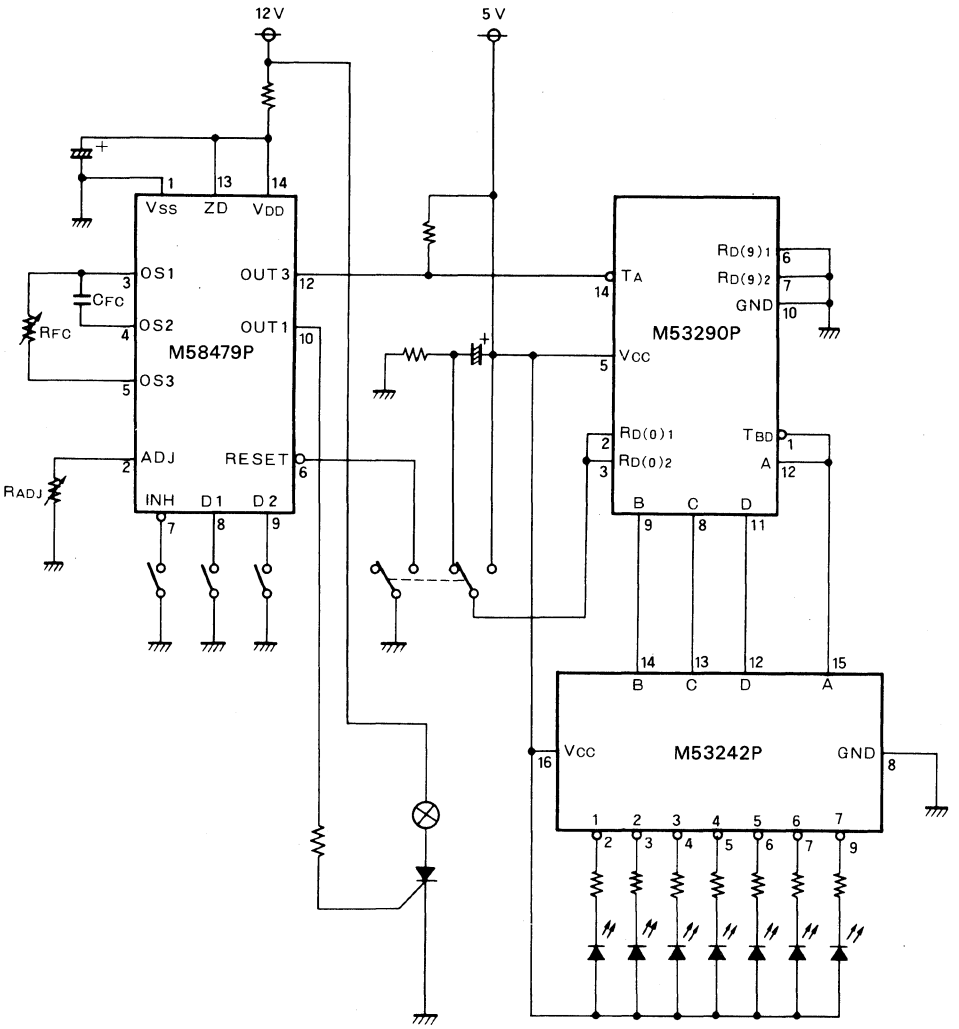
RECOMMENDED OPERATING CONDITIONS (Ta = −30～75°C, unless otherwise noted.)

Symbol	Parameter		Limits			Unit
			Min	Nom	Max	
V_{DD}	Supply voltage	M58479P	7.4		9	V
		M58482P	3		9	V
I_{ZD}	Zenor current				10	mA
R_{FC}	Feedback resistance		0.005		10	MΩ
C_{FC}	Oscillation capacitance		0.001		1	μF
R_{FC}	Resistance for fine-adjustment of oscillation frequency		0		100	kΩ
V_{IH}	High-level input voltage, $\overline{RESET}$, $\overline{INH}$, D_1, D_2		$0.7 \times V_{DD}$	V_{DD}	V_{DD}	V
V_{IL}	Low-level input voltage, $\overline{RESET}$, $\overline{INH}$, D_1, D_2		0	0	$0.3 \times V_{DD}$	V

ELECTRICAL CHARACTERISTICS (Ta=25°C, unless otherwise noted.)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{ZD}	Zenor voltage		I_{ZD}=2mA	7.4	8.2	9	V
			I_{ZD}=10mA	7.5	8.2	9	V
I_{DD}	Supply current	M58479P	V_{DD}=7.5V, C_{FC}=0.01μF, R_{FC}=1MΩ, R_{ADJ}=0Ω, Input/output open		0.25	1	mA
		M58482P	V_{DD}=7.5V, C_{FC}=0.01μF, R_{FC}=1MΩ, R_{ADJ}=0Ω, Input/output open		25	100	μA
V_{RE}	Supply voltage at the time of automatic-reset release	M58479P		3.1		5.4	V
V_{TR}	Transition voltage of first inverter in the oscillator		V_{DD}=7.5V, R_{ADJ}=0Ω	2.9		4.8	V
R_I	Pull-up resistance: $\overline{RESET}$, $\overline{INH}$, D1, D2 inputs	M58479P		10	20	30	kΩ
		M58482P		25	50	75	kΩ
I_{OH}	High-level output current, OUT1 and OUT2 outputs		V_{DD}=7.5V, V_O=0V	5	10		mA
I_{OL}	Low-level output current, OUT1, OUT2, and OUT3 outputs		V_{DD}=7.5V, V_O=7.5V	10	20		mA
I_{OZH}	Off-state output current, OUT3 output		V_{DD}=7.5V, V_O=7.5V			1	μA
I_{OL}	Low-level output current; OUT1, OUT2, and OUT3 outputs		V_{DD}=7.5V, V_O=0.4V	1.6			mA
I_{OL}	Low-level output current; OUT1, OUT2, and OUT3 outputs	M58482P	V_{DD}=4.5V, V_O=0.4V	1.6			mA
V_{OL}	Low-level output voltage; OUT1, OUT2, and OUT3 outputs		V_{DD}=7.5V			0.1	V

APPLICATION EXAMPLE



M58480P, M58484P

30-FUNCTION REMOTE-CONTROL TRANSMITTERS

DESCRIPTION

The M58480P and M58484P are 30-function remote-control transmitter circuits manufactured by aluminum-gate CMOS technology for use with in television receivers, audio equipment and the like, using infrared for transmission. They convey 30 different commands on the basis of a 6-bit PCM code. In the M58480P, entry priority is given to the first key pushed, while in the M58484P each key has an assigned priority. These transmitters are intended to be used in conjunction with an M58481, M58485P or M58487P receiver.

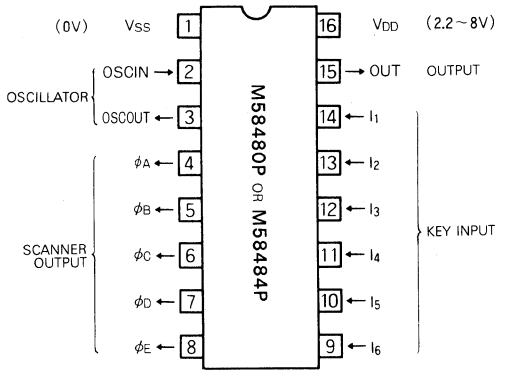
FEATURES

- Single power supply
- Wide supply voltage range: 2.2V 8V
- Low power dissipation:
  Non-operating condition (V_{DD} = 3V) : ..... 3nW (typ)
  : ..... 3μW (max)
- On-chip oscillator
- Low-cost LC/L or ceramic oscillator used in determining reference frequency (480 kHz or 455 kHz)
- Low external component count
- Low transmitter duty cycle (3.6%) for minimal power consumption

APPLICATIONS

- Remote-control transmitters for TV and other applications

PIN CONFIGURATION (TOP VIEW)

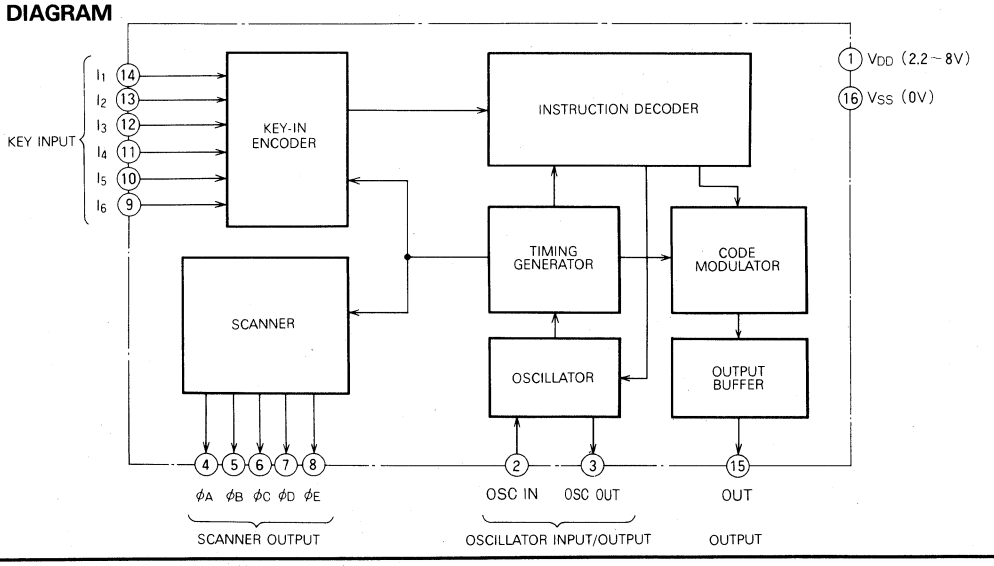


Outline 16P4

FUNCTION

The M58480P and M58484P transmitter circuits for infrared remote-control systems consist of an oscillator, a timing generator, a scanner, a key-in encoder, an instruction decoder, a code modulator, and an output buffer. With a 6 x 5 keyboard matrix, 30 commands can be transmitted by 6-bit PCM code. Oscillation is stopped when none of the keys are depressed, to minimize power consumption.

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

FUNCTIONAL DESCRIPTION

Oscillator

As the oscillator is on chip, oscillation frequency is easily obtained by connecting an external LC network or ceramic resonator between the OSC IN and OSC OUT terminals. Figs. 1 and 2 show typical oscillators.

Fig. 1 An example of an oscillator (using a ceramic resonator)

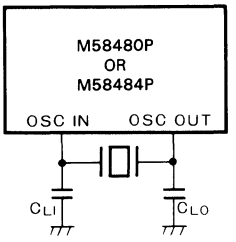
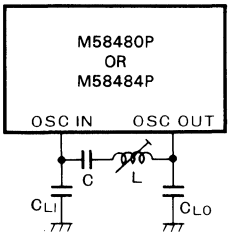


Fig. 2 An example of an oscillator (using an LC network)



Setting the oscillation frequency to 480 kHz (or 455 kHz) will also set the signal transmission carrier wave to 40 kHz (or 38 kHz).

Power consumption is minimized by stopping oscillation in the oscillator when none of the keys are depressed.

Key Input

Thirty different commands can be input by a 6 x 5 keyboard matrix consisting of inputs $I_1 \sim I_6$ and scanner outputs $\phi A \sim \phi E$.

In the M58480P, key with first-key entry is given priority, and next-key entry is not allowed unless all keys are released.

In the M58484P, with assigned priority, simultaneous depression of more than two keys makes the key with higher priority effective. Order of key priority for scanner outputs is ϕA, ϕB, ϕC, ϕD, and ϕE, and in the same scanner output, I_1, I_2, I_3, I_4, I_5, and I_6.

When more than two keys are depressed at the same time, however, commands may not function due to short-circuiting among scanner outputs.

Table 1 shows the relationship between the keyboard matrix and the transmission commands.

Table 1 Relation between the keyboard matrix and the transmission commands

Key input \ Scanner output	ϕE	ϕD	ϕC	ϕB	ϕA
I_1	CH1	CH2	CH3	CH4	POWER ON/OFF
I_2	CH5	CH6	CH7	CH8	CH UP
I_3	CH9	CH10	CH11	CH12	CH DOWN
I_4	CH13	CH14	CH15	CH16	VO UP
I_5	BR UP	BR DOWN	BR 1/2	MUTE	VO DOWN
I_6	CS UP	CS DOWN	CS 1/2	CALL	VO 1/3

Transmission Commands

Table 2 shows the 30 commands that can be transmitted by 6-bit PCM codes ($D_1 \sim D_6$).

The code 000000 is not assigned for preventing error operations.

Table 2 Relation between the commands and the transmission codes

Transmission code						Function	Remarks
D_1	D_2	D_3	D_4	D_5	D_6		
1	0	0	0	0	0	CH UP	Analog control
0	1	0	0	0	0	CH DOWN	
1	1	0	0	0	0	VO UP	
0	0	1	0	0	0	VO DOWN	
1	0	1	0	0	0	BR UP	
0	1	1	0	0	0	BR DOWN	
1	1	1	0	0	0	CS UP	
0	0	0	1	0	0	CS DOWN	
1	0	0	1	0	0	MUTE	
0	1	0	1	0	0	VO(1/3)	Normalization of analog
1	1	0	1	0	0	BR(1/2)	
0	0	1	1	0	0	CS(1/2)	
1	0	1	1	0	0	CALL	
0	1	1	1	0	0	POWER ON/OFF	
0	0	0	0	1	0	CH 1	Channels selected directly
1	0	0	0	1	0	CH 2	
0	1	0	0	1	0	CH 3	
1	1	0	0	1	0	CH 4	
0	0	1	0	1	0	CH 5	
1	0	1	0	1	0	CH 6	
0	1	1	0	1	0	CH 7	
1	1	1	0	1	0	CH 8	
0	0	0	1	1	0	CH 9	
1	0	0	1	1	0	CH 10	
0	1	0	1	1	0	CH 11	
1	1	0	1	1	0	CH 12	
0	0	1	1	1	0	CH 13	
1	0	1	1	1	0	CH 14	
0	1	1	1	1	0	CH 15	
1	1	1	1	1	0	CH 16	

Transmission Coding

When oscillation frequency f_{OSC} is 480kHz, transmission of data code is executed as follows: when f_{OSC} is other than 480 kHz, period is multiplied by 480 kHz/f_{OSC} and its frequency by f_{OSC}/480 kHz.

A single pulse is amplitude-modulated by a carrier of 40 kHz, and the pulse width is 0.5ms. Therefore a single pulse consists of 20 clock pulses of 40kHz (see Fig. 3).

The distinction between "0" and "1" bits is made by the pulse interval between pulses, with a 2msec interval corresponding to "0", and a 4msec interval representing "1" (Fig. 4).

One command word is composed of 6 bits, that is, of 7 pulses, and it is transmitted in the 48ms cycle while a matrix switch is depressed.

As mentioned above, adoption of this code means that the period during which output is high (i.e. signal emitting LED is lit) is shorter than in continuous wave transmission. Indeed the LED is on for only half the 7-pulse period or 1.75ms, which is 3.6% of the 48ms entire cycle. This not only saves in total power consumption, but it also improves LED reliability. Put another way, emission can be increased on the same power consumption.

Fig. 3 A single pulse modulated onto carrier (40kHz)

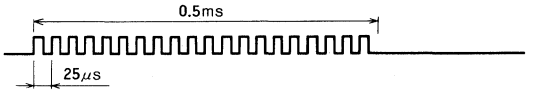


Fig. 4 Distinction between the bits "1" and "0"

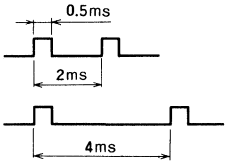
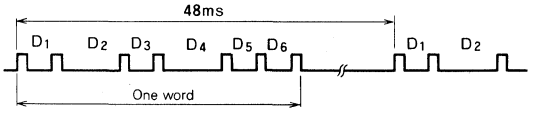
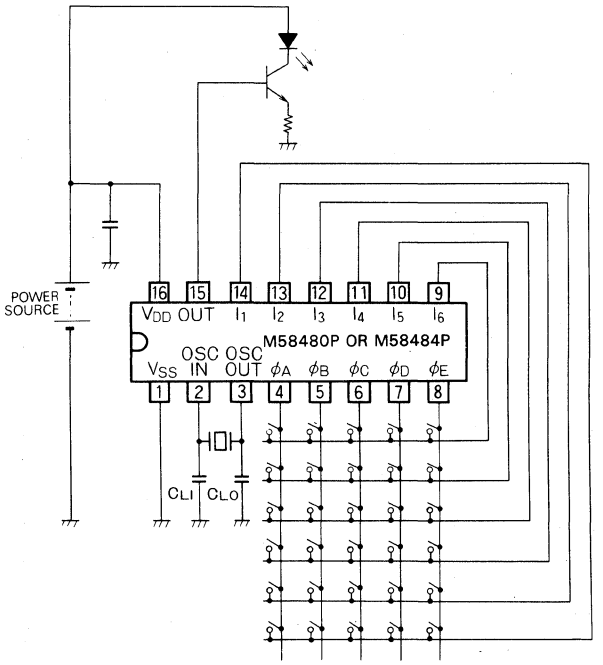


Fig. 5 Synthesis of one word (the code below shows 010100)



APPLICATION EXAMPLE



MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{DD}	Supply voltage	With respect to V_{SS}	−0.3 ~ 9	V
V_I	Input voltage		$V_{SS} \leqq V_I \leqq V_{DD}$	V
V_O	Output voltage		$V_{SS} \leqq V_O \leqq V_{DD}$	V
P_d	Maximum power dissipation	Ta = 25℃	300	mW
T_{opr}	Operating free-air temperature range		−30 ~ 70	℃
T_{stg}	Storage temperature range		−40 ~ 125	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{DD}	Supply voltage	2.2		8	V
f_{OSC}	Oscillation frequency		455		kHz
			480		kHz
V_{IH}	High-level input voltage, $I_1 \sim I_6$	$0.7 \times V_{DD}$	V_{DD}	V_{DD}	V
V_{IL}	Low-level input voltage, $I_1 \sim I_6$	0	0	$0.3 \times V_{DD}$	V

ELECTRICAL CHARACTERISTICS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
V_{DD}	Operational supply voltage	Ta = −30 ~ 70℃, f_{OSC} = 455kHz		2.2		8	V
I_{DD}	Supply voltage during operation	f_{OSC} = 455kHz	V_{DD} = 3 V		0.1	0.5	mA
			V_{DD} = 6 V		0.5	2	mA
I_{DD}	Supply voltage during non-operation	V_{DD} = 3 V				1	μA
		V_{DD} = 8 V				5	μA
R_I	Pull-up resistances, $I_1 \sim I_6$				20		kΩ
I_{OL}	Low-level output currents, $\phi_A \sim \phi_E$	V_{DD} = 3 V, V_O = 3 V		0.2	0.5		mA
		V_{DD} = 6 V, V_O = 6 V		1	2		mA
I_{OH}	High-level output current, OUT	V_{DD} = 3 V, V_O = 0 V		−5	−10		mA
		V_{DD} = 6 V, V_O = 0 V		−15	−30		mA

30 FUNCTION REMOTE-CONTROL RECEIVERS

DESCRIPTION

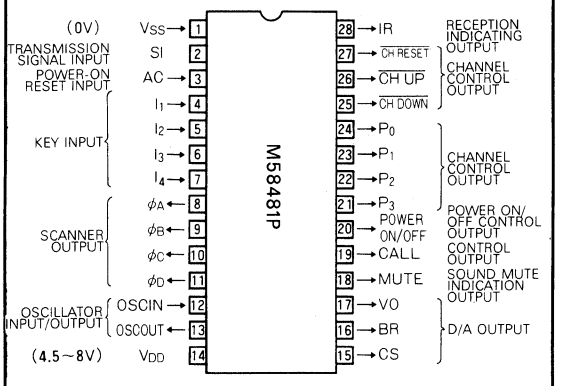
The M58481P is a 30-function remote-control receiver circuit manufactured by aluminum-gate CMOS technology for use in television receivers, audio equipment, and the like using infrared for transmission. It enables direct control of 16 functions at the receiver.

The M58481P is intended for use with an M58480P or M58484P transmitter.

FEATURES

- Single power supply
- Wide supply voltage range: 4.5V~8V
- Low power dissipation
- On-chip oscillator
- Low-cost LC or ceramic oscillator used in determining reference frequency (480 kHz or 455 kHz)
- Information is transmitted by pulse code modulation
- Good noise immunity—instructions are not executed unless same code is received three or more times in succession
- Single transmission frequency (40 kHz or 38 kHz) for carrier wave
- 16 TV channels selected directly
- Three analog functions—volume, brightness and color saturation—are independently controlled to 64 stages by three 6-bit D/A converters.
- 16 commands are controlled at the M58481P receiver as well
- Has large tolerance in operating frequency between the transmitter and the receiver
- Can be connected with an M51231P or equivalent touch-control channel selector.

PIN CONFIGURATION (TOP VIEW)



Outline 28P4

APPLICATION

- Remote-control receiver for TV or other applications

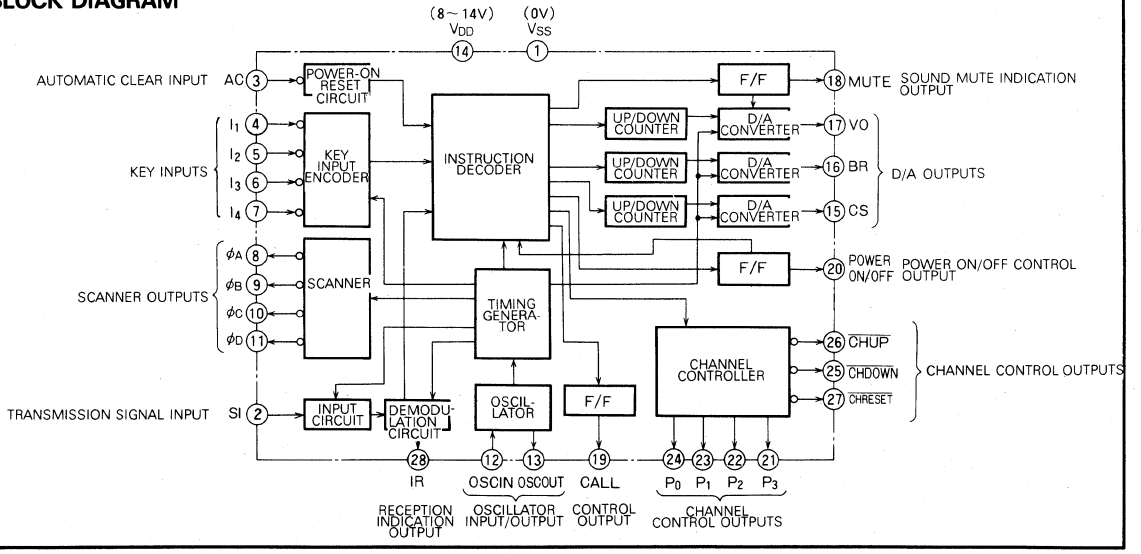
FUNCTION

The M58481P is designed to decode and execute instructions after three successive receptions of the identical instruction code, providing a good noise immunity.

Instructions comprise direct selection of 16 channels, channel position high and low, volume high and low, brightness high and low, color saturation high and low, normalization of volume, brightness and color saturation, sound mute on and off, TV main power on and off, and output CALL on and off.

In addition, 16 functional instructions can be entered from the receiver.

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

FUNCTIONAL DESCRIPTION

Oscillator

As the oscillator is on-chip, oscillation frequency is easily obtained by connecting an external LC network or ceramic resonator between the OSC IN and OSC OUT terminals. Figs. 1 and 2 show typical oscillators.

Fig. 1 An example of an oscillator (using ceramic resonator)

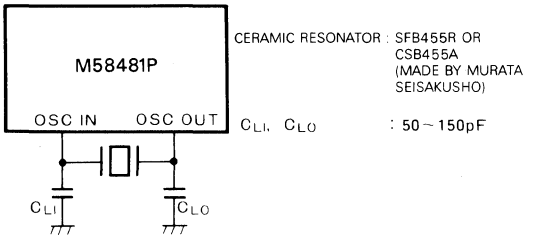
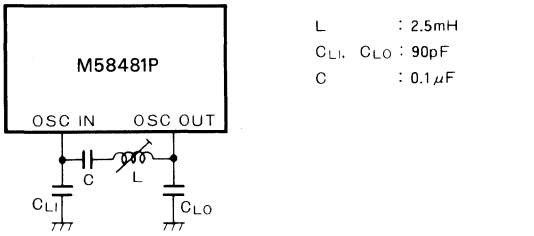


Fig. 2 An example of an oscillator (using LC network)



Reception Signal Input Circuit and Demodulation Circuit

The reception signal caught by the photo detector is amplified in the amplifier and added to the SI, where it is converted into a pulse signal in the input circuit to be sent to the demodulation circuit. In the demodulation circuit, the pulse interval of the pulse signal is judged and then converted into the digital code to be sent to the instruction decoder.

SI is applied as amplified, either through a capacitor coupling (Fig. 3) or directly as a pulse signal (Figs. 4 and 5). A Schmitt trigger circuit is provided in the SI input circuit for preventing spurious operation due to noise.

Fig. 3 SI input waveform (when applied through a capacitor coupling)

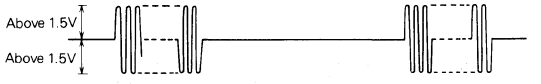


Fig. 4 SI input waveform (when applied directly)

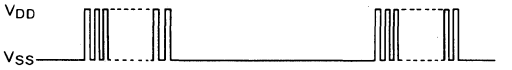
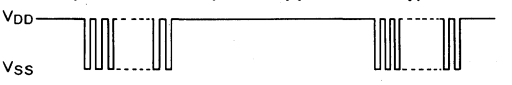


Fig. 5 SI input waveform (when applied directly)



Instruction Decoder

The instruction decoder starts to function after receiving the same instruction code three or more times in succession from the demodulation circuit.

Table 1 shows the relations between the reception code and instruction function. To prevent spurious operation, there is no code 000000.

Table 1 Relations between reception codes and instructions

Reception code						Function	Remarks
D_1	D_2	D_3	D_4	D_5	D_6		
1	0	0	0	0	0	CH UP	Channel up
0	1	0	0	0	0	CH DOWN	Channel down
1	1	0	0	0	0	VO UP	Analog control
0	0	1	0	0	0	VO DOWN	
1	0	1	0	0	0	BR UP	
0	1	1	0	0	0	BR DOWN	
1	1	1	0	0	0	CS UP	
0	0	0	1	0	0	CS DOWN	
1	0	0	1	0	0	MUTE	Sound mute on/off
0	1	0	1	0	0	VO(1/3)	Normalization of analog control
1	1	0	1	0	0	BR(1/2)	
0	0	1	1	0	0	CS(1/2)	
1	0	1	1	0	0	CALL	Output CALL on/off
0	1	1	1	0	0	POWER ON/OFF	Power on/off
0	0	0	0	1	0	CH 1	Channels selected directly
1	0	0	0	1	0	CH 2	
0	1	0	0	1	0	CH 3	
1	1	0	0	1	0	CH 4	
0	0	1	0	1	0	CH 5	
1	0	1	0	1	0	CH 6	
0	1	1	0	1	0	CH 7	
1	1	1	0	1	0	CH 8	
0	0	0	1	1	0	CH 9	
1	0	0	1	1	0	CH 10	
0	1	0	1	1	0	CH 11	
1	1	0	1	1	0	CH 12	
0	0	1	1	1	0	CH 13	
1	0	1	1	1	0	CH 14	
0	1	1	1	1	0	CH 15	
1	1	1	1	1	0	CH 16	

Key Inputs

16 different instructions can be input by a 4 x 4 keyboard matrix consisting of inputs $I_1 \sim I_6$ and scanner outputs $\phi A \sim \phi E$. Protection is also available against chattering within 10ms.

Entry priority is given to the first key depressed, and subsequent key entry is not allowed unless all keys are released. When two or more keys are depressed at the same time, scanner outputs may short-circuit, disabling all functions.

While one of the keys is depressed, instructions from the transmitter are ignored.

Table 2 Relations between keyboard matrix and instructions

Scanner output / Key input	ϕD	ϕC	ϕB	ϕA
I_1	CH RESET	CH DOWN	CH UP	POWER ON/OFF
I_2	MUTE	VO DOWN	VO UP	VO(1/3)
I_3	VO(1/3) BR(1/2) CS(1/2)	BR DOWN	BR UP	BR(1/2)
I_4	CALL	CS DOWN	CS UP	CS(1/2)

Indication of Reception

As soon as an identical code is received three times, output IR turns from low-level to high-level. Thus reception of an instruction from the transmitter can be indicated by an LED connected to output IR. Table 2 shows the relations between the keyboard matrix and the instructions.

Analog Outputs (VO, BR, CS)

As three 6-bit D/A converters are contained internally, three kinds of analog values can be controlled to 64 stages independently. The D/A converters are pulse-width modulator, the repetition frequency is 1.25 kHz (when f_{OSC}= 480 kHz) and minimum pulse width is 12.5μs.

Analog values can be incremented/decremented at a rate of about 1 step/0.1sec through the remote control or key input. The time required for increasing the analog value from the minimum to the maximum is about 6.6 seconds (when f_{OSC}=480 kHz).

It is also possible to set the analog values to 1/3 (VO), 1/2 (BR, CS) of these maximum values by means of the remote control or the key input (normalization).

Sound Mute

Sound mute on/off is controlled through the remote control or the key input. When sound mute is on, output VO goes low, and output MUTE goes high.

Sound mute is automatically released from ON when VO is either incremented or decremented by remote control or the key input.

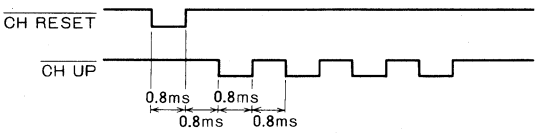
Channel Control

It is possible to employ either of two channel-control methods: parallel control by outputs $P_0 \sim P_3$, and serial control by outputs $\overline{\text{CH UP}}$, $\overline{\text{CH DOWN}}$, and $\overline{\text{CH RESET}}$.

In parallel control, a 4-bit address corresponding to a selected channel number appears at output $P_0 \sim P_3$. Table 3 shows the relation between channel numbers and outputs $P_0 \sim P_3$.

In serial control, a single pulse appears on the output $\overline{\text{CH RESET}}$ first, and then the pulses whose number is deducted by one from the selected channel number appear on the output $\overline{\text{CH UP}}$, as shown in Fig. 6. Up and down

Fig. 6 Timing chart of serially controlled channel selection (when fosc =480kHz)



channel switching, is controlled by a single pulse appearing at output $\overline{\text{CH UP}}$ or $\overline{\text{CH DOWN}}$, allowing connection to the M51231P or equivalent touch-control channel selector IC.

During direct channel selection or up-down channel switching, output VO goes low for 25~50ms.

Table 3 Relations between channel number and address output $P_0 \sim P_3$.

Channel number	Address outputs			
	P_0	P_1	P_2	P_3
1	0	0	0	0
2	1	0	0	0
3	0	1	0	0
4	1	1	0	0
5	0	0	1	0
6	1	0	1	0
7	0	1	1	0
8	1	1	1	0
9	0	0	0	1
10	1	0	0	1
11	0	1	0	1
12	1	1	0	1
13	0	0	1	1
14	1	0	1	1
15	0	1	1	1
16	1	1	1	1

Power On/Off

The remote control or the key input makes it possible to turn the POWER ON/OFF output from low to high or vice versa, effecting on/off control of the TV set.

While POWER ON/OFF is low, all channel and analog controls through the remote control are disabled, as are all through the keyboard, except CH RESET ($\phi D \sim I_1$), VO (1/3), BR (1/2), and CS (1/2) ($\phi D \sim I_3$).

Output CALL

The output CALL is turned high or low by remote control or the key input. This output effects on/off control of channel number indication or change of receiving modes of multi-channel broadcasting.

Power-on Reset

Attaching a capacitor to terminal AC activates the power-on reset function when power is on to the M58481P.

Activation of the power-on reset function sets outputs VO, BR, and CS to 1/3, 1/2, and 1/2, respectively, of their maximum value, turns POWER ON/OFF and CALL outputs low, and turns outputs $P_0 \sim P_3$ to 0000.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{DD}	Supply voltage	With respect to V_{SS}	−0.3～9	V
V_I	Input voltage		$V_{SS} \leqq V_I \leqq V_{DD}$	—
V_O	Output voltage		$V_{SS} \leqq V_O \leqq V_{DD}$	—
P_d	Maximum power dissipation	Ta＝25℃	300	mW
T_{opr}	Operating free-air temperature range		−30～70	℃
T_{stg}	Storage temperature range		−40～126	℃

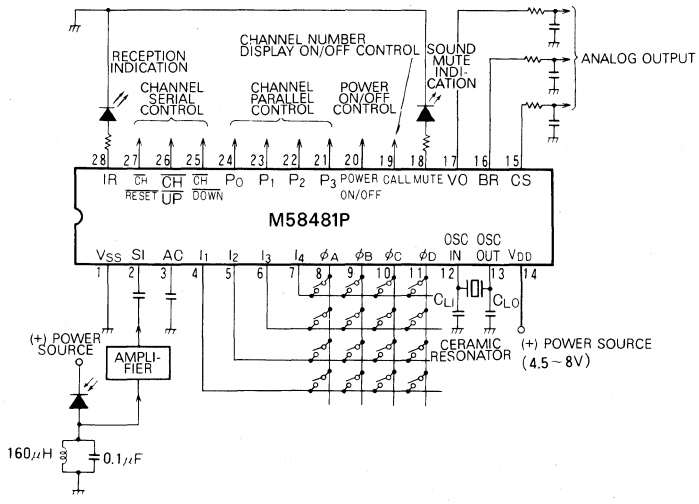
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{DD}	Supply voltage	4.5		8	V
f_{OSC}	Oscillation frequency		455		kHz
			480		kHz
V_I	Input voltage, SI	3			V_{P-P}
V_{IH}	High-level input voltage, I_1～I_4	0.7×V_{DD}	V_{DD}	V_{DD}	V
V_{IL}	Low-level input voltage, I_1～I_4	0	0	0.3×V_{DD}	V

ELECTRICAL CHARACTERISTICS (T_a＝25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{DD}	Operating supply voltage	Ta＝−30～70℃, f_{OSC}＝455kHz	4.5		8	V
I_{DD}	Supply current	V_{DD}＝5V, f_{OSC}＝455kHz		0.4	1	mA
		V_{DD}＝8V, f_{OSC}＝455kHz		1.5	3	mA
R_I	Pull-up resistors, I_1～I_4			20		kΩ
I_{OL}	Low-level output currents, ϕ_A～ϕ_D	V_{DD}＝8V, V_O＝8V	3			mA
I_{OL}	Low-level output currents, $\overline{CH\ UP}$, $\overline{CH\ DOWN}$, $\overline{CH\ RESET}$	V_{DD}＝8V, V_O＝8V	15			mA
I_{OZH}	Off-state output currents, $\overline{CH\ UP}$, $\overline{CH\ DOWN}$, $\overline{CH\ RESET}$	V_{DD}＝8V, V_O＝8V			1	μA
I_{OH}	High-level output currents, P_0～P_3	V_{DD}＝8V, V_O＝0V	−0.5			mA
I_{OL}	Low-level output currents, P_0～P_3	V_{DD}＝8V, V_O＝8V	15			mA
I_{OH}	High-level output currents, VO, BR, CS	V_{DD}＝8V, V_O＝0V	−5			mA
I_{OL}	Low-level output currents, VO, BR, CS	V_{DD}＝8V, V_O＝8V	10			mA
I_{OH}	High-level output currents, POWER ON/OFF, CALL, MUTE	V_{DD}＝8V, V_O＝0V	−15			mA
I_{OL}	Low-level output currents, POWER ON/OFF, CALL, MUTE	V_{DD}＝8V, V_O＝8V	3			mA
I_{OH}	High-level output current, IR	V_{DD}＝8V, V_O＝0V	−10			mA
I_{OL}	Low-level output current, IR	V_{DD}＝8V, V_O＝8V	3			mA

APPLICATION EXAMPLE



29-FUNCTION REMOTE-CONTROL RECEIVERS

DESCRIPTION

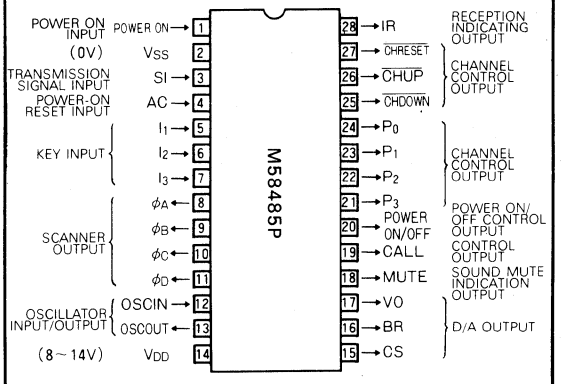
The M58485P is a 29-function remote-control receiver circuit manufactured by aluminum-gate CMOS technology for use in television receivers, audio equipment, and the like using infrared for transmission. It enables direct control of 12 functions at the receiver.

The M58485P is intended for use with an M58480P or M58484P transmitter.

FEATURES

- Single power supply
- Wide supply voltage range: 8V~14V
- Low power dissipation
- On-chip oscillator
- Low-cost LC or ceramic oscillator used in determining reference frequency (480 kHz or 455 kHz)
- Information is transmitted by pulse code modulation
- Good noise immunity—instructions are not executed unless the same code is received three or more times in succession
- Single transmission frequency (40 kHz or 38 kHz) for carrier wave
- 16 TV channels selected directly
- Three analog functions—volume, brightness, and color saturation—are independently controlled to 64 stages by three 6-bit D/A converters.
- 12 instructions are controlled at the M58485P receiver, as well.
- Has large tolerance in operating frequency between the transmitter and the receiver
- Can be connected with an M51231P or equivalent touch-control channel selector

PIN CONFIGURATION (TOP VIEW)



Outline 28P4

APPLICATION

- Remote-control receiver for TV or other applications

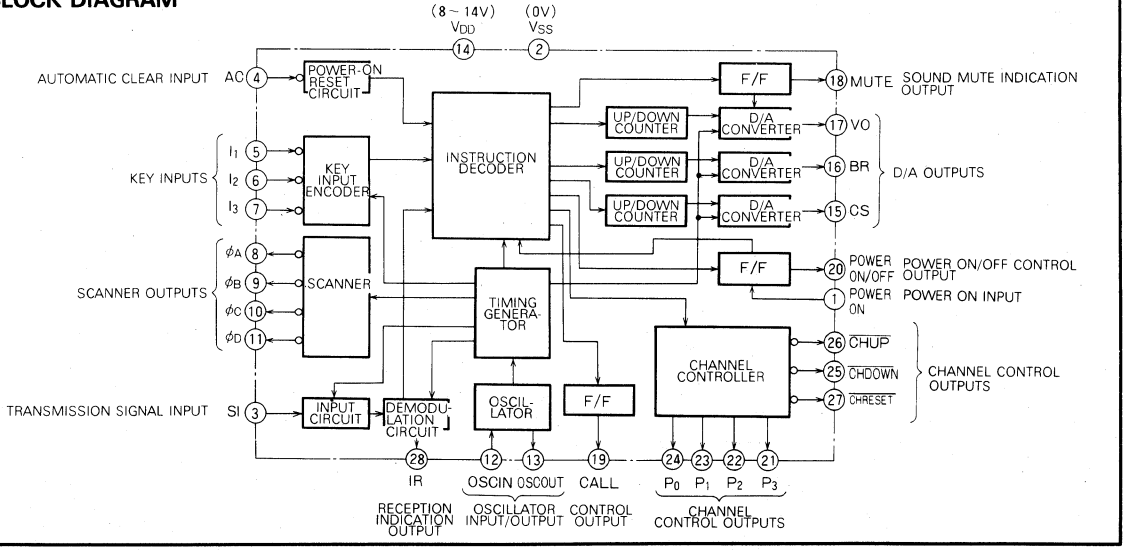
FUNCTION

The M58485P is designed to decode and execute instructions after three successive receptions of the identical instruction code, providing a good noise immunity.

Instructions comprise direction selection of 16 channels, channel position high and low, volume high and low, brightness high and low, color saturation high and low, normalization of volume, brightness and color saturation, sound mute on and off, TV main power on and off, and output CALL on and off.

In addition, 12 functional instructions can be entered from the receiver.

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

FUNCTIONAL DESCRIPTION

Oscillator

As the oscillator is on-chip, oscillation frequency is easily obtained by connecting an external LC network or a ceramic resonator between the OSC IN and OSC OUT terminals. Figs. 1 and 2 show typical oscillators.

Fig. 1 An example of an oscillator (using ceramic resonator)

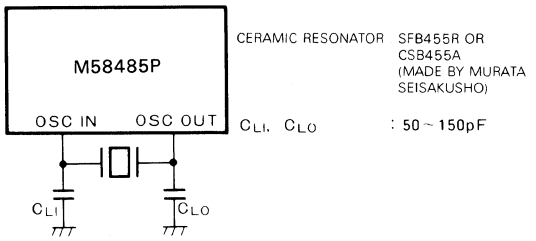
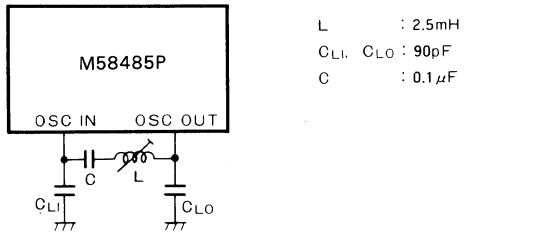


Fig. 2 An example of an oscillator (using LC network)



Reception Signal Input Circuit and Demodulation Circuit

The reception signal caught by the photo detector is amplified in the amplifier and added to the SI, where it is converted into a pulse signal in the input circuit to be sent to the demodulation circuit. In the demodulation circuit, the pulse interval of the pulse signal is judged and then converted into the digital code to be sent to the instruction decoder.

SI is applied as amplified either through a capacitor coupling (Fig. 3) or directly as a pulse signal (Figs. 4 and 5). A Schmitt trigger circuit is provided in the SI input circuit for preventing spurious operation due to noise.

Fig. 3 SI input waveform (when applied through a capacitor coupling)

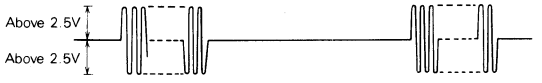
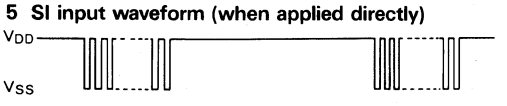


Fig. 4 SI input waveform (when applied directly)

Fig. 5 SI input waveform (when applied directly)



Instruction Decoder

The instruction decoder starts to function after receiving the same instruction code three or more times in succession from the demodulation circuit.

Table 1 shows the relations between the reception code and instruction function. To prevent spurious operation, there is no code 000000.

Table 1 Relations between reception codes and instructions

Reception code						Function	Remarks
D_1	D_2	D_3	D_4	D_5	D_6		
1	0	0	0	0	0	CH UP	Channel up
0	1	0	0	0	0	CH DOWN	Channel down
1	1	0	0	0	0	VO UP	Analog control
0	0	1	0	0	0	VO DOWN	
1	0	1	0	0	0	BR UP	
0	1	1	0	0	0	BR DOWN	
1	1	1	0	0	0	CS UP	
0	0	0	1	0	0	CS DOWN	
1	0	0	1	0	0	MUTE	Sound mute on/off
0	1	0	1	0	0	VO(1/3)	Normalization of analog control
1	1	0	1	0	0	BR(1/2), CS(1/2)	
1	0	1	1	0	0	CALL	Output CALL on/off
0	1	1	1	0	0	POWER ON/OFF	Power on/off
0	0	0	0	1	0	CH 1	Channels selected directly
1	0	0	0	1	0	CH 2	
0	1	0	0	1	0	CH 3	
1	1	0	0	1	0	CH 4	
0	0	1	0	1	0	CH 5	
1	0	1	0	1	0	CH 6	
0	1	1	0	1	0	CH 7	
1	1	1	0	1	0	CH 8	
0	0	0	1	1	0	CH 9	
1	0	0	1	1	0	CH 10	
0	1	0	1	1	0	CH 11	
1	1	0	1	1	0	CH 12	
0	0	1	1	1	0	CH 13	
1	0	1	1	1	0	CH 14	
0	1	1	1	1	0	CH 15	
1	1	1	1	1	0	CH 16	

Key Inputs

It is possible to input 12 different instructions by the 3 x 4 keyboard matrix consisting of inputs $I_0 \sim I_3$ and scanner outputs $\phi A \sim \phi D$. Protection is also available against chattering within 10ms.

As entry priority is given to each key, depression of more than two keys at the same time makes the key with higher priority effective. For the scanner output, priority is given in the order of ϕA, ϕB, ϕC, and ϕD, and in the order of I_1, I_2, and I_3 if scanner output is the same. When two or more keys are depressed at the same time, scanner outputs may short-circuit, disabling all functions.

While one of the keys is depressed, instructions from the transmitter are ignored.

Table 2 shows the relations between the keyboard matrix and the commands.

Table 2 Relations between keyboard matrix and instructions

Scanner output / Key input	ϕ_D	ϕ_C	ϕ_B	ϕ_A
I_1	CH UP	VO UP	BR UP	CS UP
I_2	CH DOWN	VO DOWN	BR DOWN	CS DOWN
I_3	POWER ON/OFF	MUTE	VO(1/3) BR(1/2) CS(1/2)	CALL

Indication of Reception

As soon as an identical code is received three times, the output IR turns from low-level to high-level. Thus reception of a command from the transmitter can be indicated by an LED connected to output IR.

Analog Outputs (CO, BR, CS)

As three 6-bit D/A converters are contained internally, three kinds of analog values can be controlled to 64 stages independently. The D/A converters are pulse-width modulator, and the repetition frequency is 1.25 kHz (when f_{OSC}= 480 kHz) and minimum pulse width is 12.5μs.

Analog values can be incremented/decremented at a rate of about 1 step/0.1 sec through the remote control or the key input. The time required for increasing the analog value from the minimum to the maximum is about 6.6 seconds (when f_{OSC}=480 kHz).

It is also possible to set the analog values to 1/3 (VO), 1/2 (BR, CS) of these maximum values by means of the remote control or the key input (normalization).

Sound Mute

Sound mute on/off is controlled through the remote control or the key input. When sound mute is on, output VO goes low, and output MUTE goes high.

Sound mute is automatically released from ON when VO is either incremented or decremented by remote control or the key input.

Channel Control

It is possible to employ either of two channel control methods: parallel control by outputs $P_0 \sim P_3$, and serial control by outputs $\overline{\text{CH UP}}$, $\overline{\text{CH DOWN}}$, and $\overline{\text{CH RESET}}$.

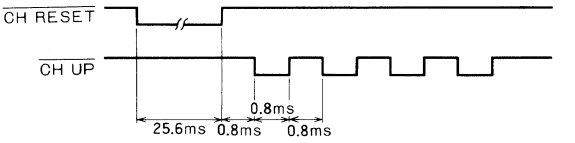
In parallel control, a 4-bit address corresponding to a selected channel number appears at output $P_0 \sim P_3$. Table 3 shows the relations between channel numbers and outputs $P_0 \sim P_3$.

In serial control, a single pulse appears on the output $\overline{\text{CH RESET}}$ first, and then the pulses whose number is deducted by one from the selected channel number appear on the output $\overline{\text{CH UP}}$, as shown in Fig. 6. Up and down channel switching is controlled by a single pulse appearing at output $\overline{\text{CH UP}}$ or $\overline{\text{CH DOWN}}$, allowing connection to the M51231P or equivalent touch-control channel selector IC.

Table 3 Relations between channel number and address output $P_0 \sim P_3$.

Channel number	Address outputs			
	P_0	P_1	P_2	P_3
1	0	0	0	0
2	1	0	0	0
3	0	1	0	0
4	1	1	0	0
5	0	0	1	0
6	1	0	1	0
7	0	1	1	0
8	1	1	1	1
9	0	0	0	1
10	1	0	0	1
11	0	1	0	1
12	1	1	0	1
13	0	0	1	1
14	1	0	1	1
15	0	1	1	1
16	1	1	1	1

Fig. 6 Timing chart of serially controlled channel selection (when fosc =480kHz)



During direct channel selection or up-down channel switching, output VO goes low for 25~50ms.

Outputs, $\overline{\text{CH UP}}$, $\overline{\text{CH DOWN}}$, $\overline{\text{CH RESET}}$, and $P_0 \sim P_3$, are the open-drain type of N-channel transistor.

Power on/off

The remote control or the key input makes it possible to turn the POWER ON/OFF output from low to high or vice versa, and it is possible to change the POWER ON/OFF output from low to high by means of the POWER ON input.

While POWER ON/OFF is low, all channel and analog controls through the remote control are disabled, as are all through the keyboard.

Output CALL

The output CALL is turned high or low by remote control or the key input. This output effects on/off control of channel number indication or change of receiving modes of multi-channel broadcasting.

Power-on Reset

Attaching a capacitor to terminal AC activates the power-on reset function when power is on to the M58485P.

Activation of the power-on reset function sets outputs VO, BR, and CS to 1/3, 1/2, and 1/2, respectively, of their maximum value, turns POWER ON/OFF and CALL outputs low and turns outputs $P_0 \sim P_3$ to 0000.

29-FUNCTION REMOTE-CONTROL RECEIVERS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{DD}	Supply voltage	With respect to V_{SS}	−0.3～15	V
V_I	Input voltage		$V_{SS} \leqq V_I \leqq V_{DD}$	—
V_O	Output voltage		$V_{SS} \leqq V_O \leqq V_{DD}$	—
Pd	Maximum power dissipation	Ta＝25℃	300	mW
Topr	Operating free-air temperature range		−30～70	℃
Tstg	Storage temperature range		−40～125	℃

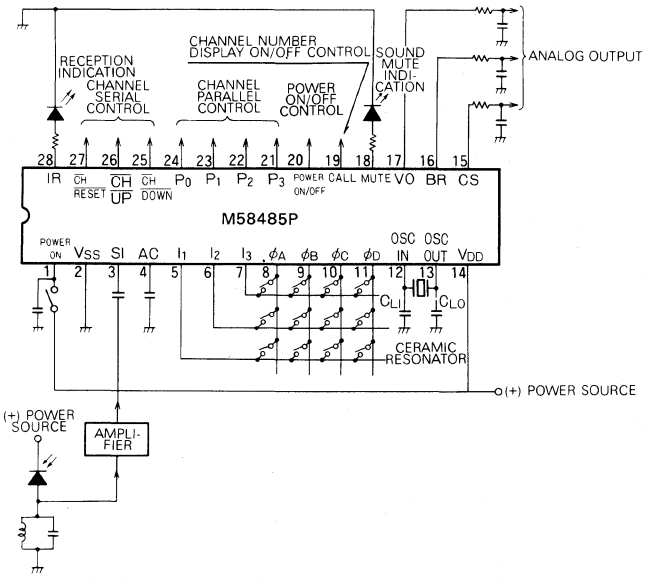
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{DD}	Supply voltage	8	12	14	V
fosc	Oscillation frequency		455		kHz
			480		kHz
V_I	Input voltage	5			V_{P-P}
V_{IH}	High-level input voltage, I_1～I_3	$0.7 \times V_{DD}$	V_{DD}	V_{DD}	V
V_{IL}	Low-level input voltage, I_1～I_3	0	0	$0.3 \times V_{DD}$	V

ELECTRICAL CHARACTERISTICS (Ta＝25℃, V_{DD}＝12V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{DD}	Supply voltage	Ta＝−30～70℃, fosc＝455kHz	8	12	14	V
I_{DD}	Supply current	fosc＝455kHz		2	5	mA
R_I	Pull-up resistance, I_1～I_3			20		kΩ
I_{OL}	Low-level output currents, ϕ_A～ϕ_D	V_O＝12V	5			mA
I_{OL}	Low-level output currents, $\overline{\text{CH UP}}$, $\overline{\text{CH DOWN}}$, $\overline{\text{CH RESET}}$	V_O＝12V	20			mA
I_{OZH}	Off-state output currents, $\overline{\text{CH UP}}$, $\overline{\text{CH DOWN}}$, $\overline{\text{CH RESET}}$	V_O＝12V			1	μA
I_{OL}	Low-level output currents, P_0～P_3	V_O＝12V	20			mA
I_{OZH}	Off-state output currents, P_0～P_3	V_O＝12V			1	μA
I_{OH}	High-level output currents, VO, BR, CS	V_O＝0 V	−7			mA
I_{OL}	Low-level output currents, VO, BR, CS	V_O＝12V	7			mA
I_{OH}	High-level output currents, POWER ON/OFF, CALL, MUTE	V_O＝0 V	−20			mA
I_{OL}	Low-level output currents, POWER ON/OFF, CALL, MUTE	V_O＝12V	5			mA
I_{OH}	High-level output current, IR	V_O＝0 V	−15			mA
I_{OL}	Low-level output current, IR	V_O＝12V	5			mA

APPLICATION EXAMPLE



M58486AP

VOLTAGE SYNTHESIZER

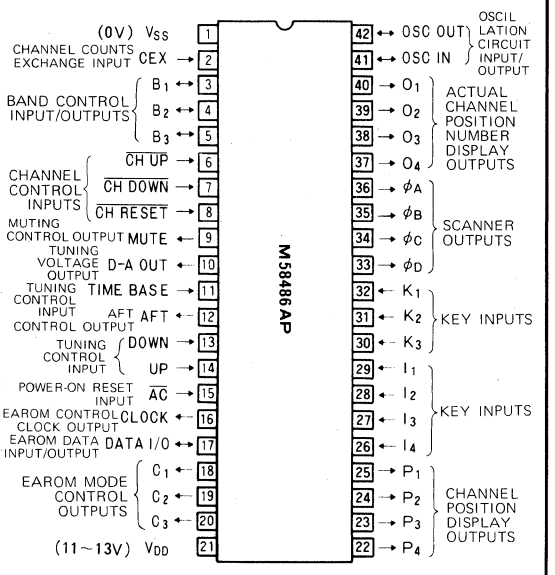
DESCRIPTION

The M58486AP is an aluminum gate CMOS integrated circuit. It has a fully automatic search function capable of writing into an EAROM the tuning voltages corresponding to all receivable stations and a sequentially automatic search function which presets any arbitrary channel. Used in conjunction with the M51251P linear sensor and M5G1400P EAROM, it is possible to configure a fully electronic tuning system for use in TVs or VTR equipment.

FEATURES

- Fully automatic search and sequentially automatic search functions
- The channel display provides channel position tab display, channel position number display, and actual channel number display
- Automatic bandswitching
- Band skip function
- Digital AFT (Automatic Fine Tuning) function
- Frequency fine adjustment function
- AFT on/off data is memorized in EAROM for each channel position
- Direct connection with a remote controller LSI such as the M58485P or M58487AP
- Direct 16 (or 12) channel selection
- Last channel memory function

PIN CONFIGURATION (TOP VIEW)

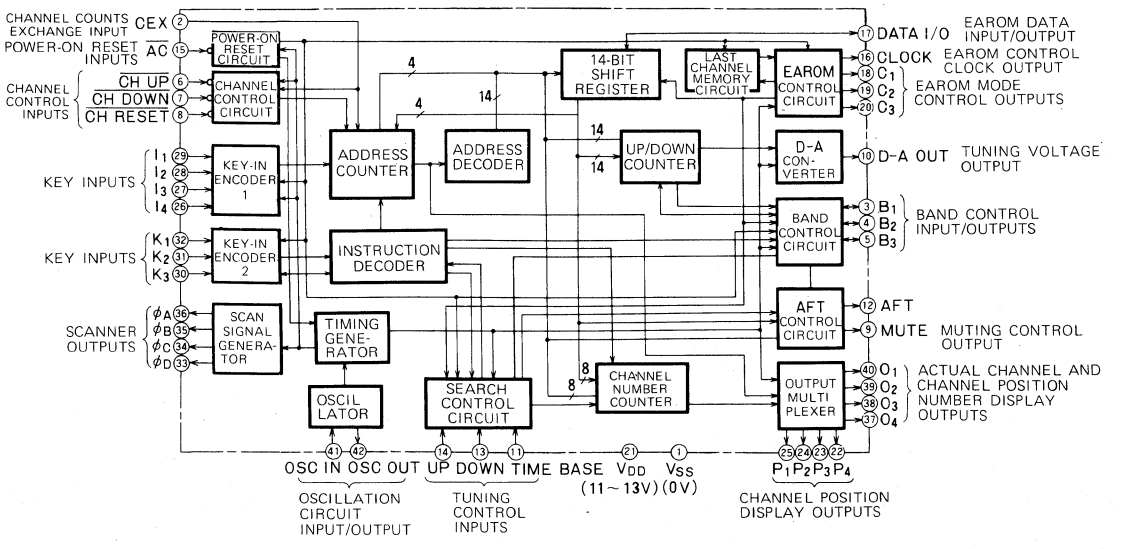


Outline 42P1

APPLICATIONS

Electronic tuning systems for TVs, VTRs, and other electronic equipment.

BLOCK DIAGRAM



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FUNCTION

The M58486AP voltage synthesizer, when used in conjunction with the M51251P linear sensor and M5G1400P EAROM, enables the configuration of a completely electronic tuning system without the use of any mechanical parts.

The main functions include fully automatic search, sequentially automatic search, direct selection of either 12 or 16 channels, automatic bandswitching, a band skip function, digital AFT (Automatic Fine Tuning), fine tuning, last channel memory, channel position tab display, channel position number display, and actual channel number display functions.

In addition, direct and sequential channel selection from a remote controller as possible.

FUNCTIONAL DESCRIPTION

Oscillator Circuit

As the oscillator is on-chip, an oscillator frequency is easily obtained by connecting an external LC network or ceramic resonator between the OSC IN and OSC OUT terminals. Fig. 1 and 2 show typical examples.

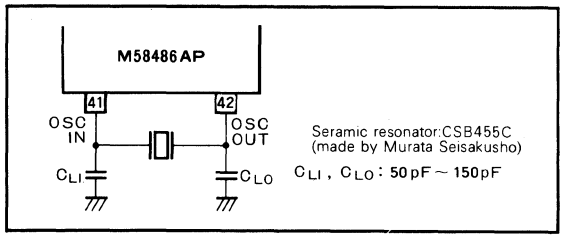

Fig. 1 An example of an oscillator (using a ceramic resonator)

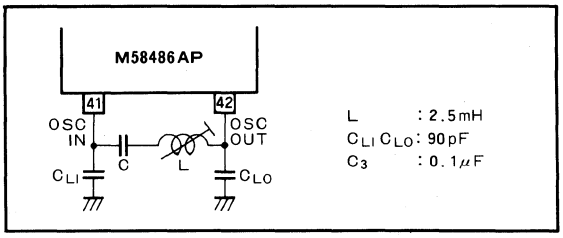

Fig. 2 An example of an oscillator (using an LC network)

Key Inputs

The M58486AP is provided with scanner outputs $\phi_A \sim \phi_D$, key inputs $I_1 \sim I_4$ and $K_1 \sim K_3$. 16-channel position selection can be achieved by using the 4x4 matrix formed by $\phi_A \sim \phi_D$ and $I_1 \sim I_4$. In addition, the 4x3 matrix formed by $\phi_A \sim \phi_D$ and $K_1 \sim K_3$ enables the input of 12 commands.

If two or more of the keys are depressed simultaneously, no commands will be input. However, it is possible to input FAM or CH LOCK in combination with another key.

Table 1 shows the relationships between these matrices and the command functions.

Table 1 Matrix and Command Functions

I \ φ	ϕ_A	ϕ_B	ϕ_C	ϕ_D
I_1	CHP 1	CHP 5	CHP 9	CHP 13
I_2	CHP 2	CHP 6	CHP 10	CHP 14
I_3	CHP 3	CHP 7	CHP 11	CHP 15
I_4	CHP 4	CHP 8	CHP 12	CHP 16

K \ φ	ϕ_A	ϕ_B	ϕ_C	ϕ_D
K_1	U-SEARCH	D/A UP	CHN 10	CHP-UP
K_2	V-SEARCH	D/A DOWN	CHN 1	CHP-DOWN
K_3	SEARCH	CH LOCK	FAM	STORE

Tuning Voltage Output (D/A OUT)

As a 14-bit D-A converter is built into the M58486AP, tuning voltage can be controlled to 16384 stages. The D-A converter is a pulse-width modulator, and the repetition frequency is 28Hz and the minimum pulse width is 2.2 μs.

By applying this output signal to the electronic tuner through an RC network, the desired tuning frequency can be achieved.

Tuning Control Inputs (UP, DOWN, TIME BASE)

These inputs are required for tuning in the search mode or channel selection mode and are supplied by the M51251P.

As shown in Fig. 3, UP and DOWN inputs are controlled by the AFC signal. The UP input is changed to a high level when the AFC signal exceeds a threshold voltage (V_H) and the DOWN input is changed to a high level when the AFC signal falls below a threshold voltage (V_L).

The TIME BASE input is high when a normal video signal is captured.

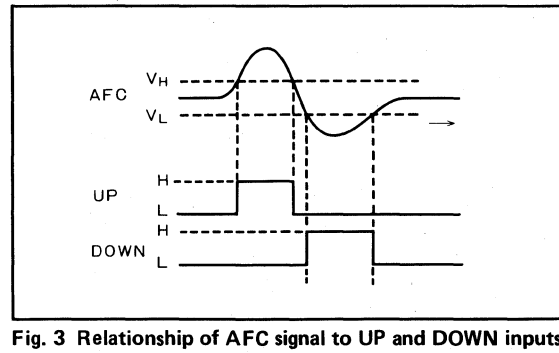

Fig. 3 Relationship of AFC signal to UP and DOWN inputs

Band Input/Outputs (B1 ~ B3)

The M58486AP system is provided with three bands. An electronic tuner is controlled by these three band inputs/outputs and D-A OUT.

As shown in Table 2, these bands correspond to the TV broadcast frequency bands.

Band	Broadcast frequency band
B1	VHF low band
B2	VHF high band
B3	UHF

Three band inputs (B1 ~ B3) are provided on the M58486AP, the output corresponding to the currently selected band being high, with all other band outputs low. Thus, by connecting transistor and LED with currents to these outputs a display of the selected band can be implemented.

If a particular band pin is shorted to V_{SS} that band will be skipped during the search (band skip function).

Search Modes

The search is the function searching automatically the video signal and writing of the required data into the EAROM.

The search function is controlled by the UP, DOWN, and TIME BASE tuning control inputs. Search functions will be described using Fig. 3, 4, and 5.

When search is begun, as up signal is applied to the 14-bit up/down counter, and the analog output of the D-A converter increases (sweeps).

As shown in Fig. 3 and 4, when the signal reaches a certain point, the UP input changes to high. Next, if the DOWN input goes high within 50ms after the UP input goes low, the sweep is ended and the digital AFT is enabled. If DOWN doesn't go high within 50ms, this is taken as an indication that the signal was not a video signal, and the sweep is continued.

Digital AFT is controlled by both the UP and DOWN inputs. When UP is high, the up signal is applied to the up/down counter and the analog output of the D-A converter increases. When DOWN is high, the down signal is applied to the up/down couner and the analog output of the D-A converter decreases. The up/down speed of digital AFT is 1/16 of the up sweep speed.

Digital AFT is ended after 200ms, after which the TIME BASE input is examined. If TIME BASE is low, it is taken as an indication that the signal is not a video signal and the sweep operation is restarted. If TIME BASE is high, the signal is taken as a video signal and the required data is written into the EAROM at the specified address. For this operation, the EAROM address is determined by the channel position and the data written is as follows.

Note, however, that for automatic writing of data into EAROM in the search mode, AFT deta is on.

14-bit up/down counter data	14 bits
2-digit BCD data of channel number counter	8 bits
Band control binary data	2 bits
AFT on/off control data	1 bit

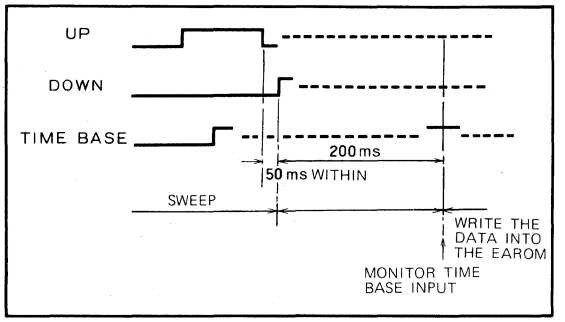

Fig. 4 UP, DOWN, TIME BASE inputs in the search mode

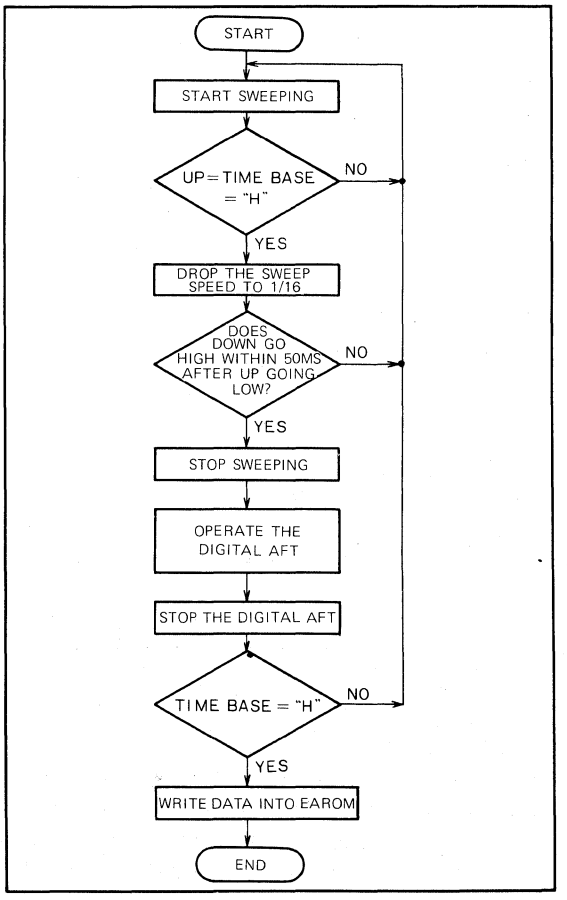

Fig. 5 A flowchart of the search method

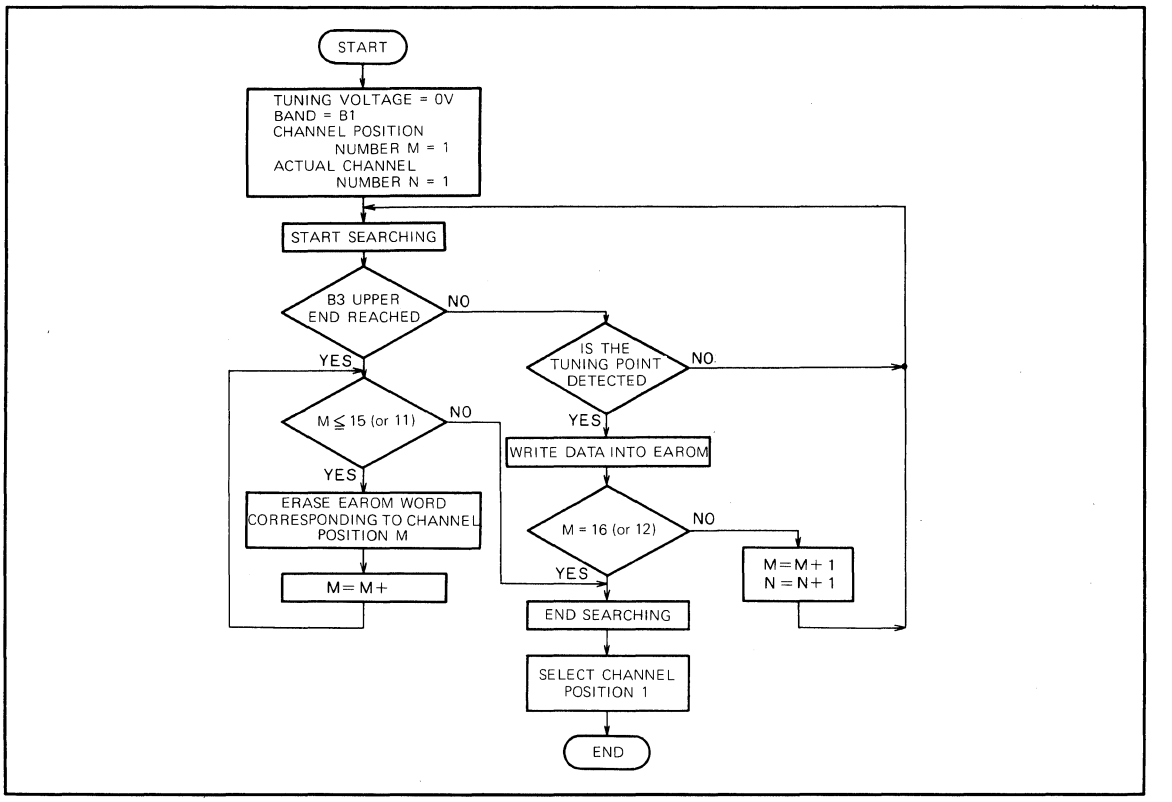

Fig. 6 A flowchart of fully automatic search (SEARCH or V-SEARCH)

Fully Automatic Search

Fig. 6 shows the flowchart of the fully automatic search.

When SEARCH or V-SEARH key is input, the D-A converter analog output is set to the lower end of B1 and the channel position number and actual channel number are both initialized to 1.

After initialization, search begins and when a video signal is captured, the required data is automatically written into the EAROM, the channel position number and actual channel number being incremented by 1, after which the search is restarted.

In this manner, when tuning voltage goes to the upper end of band B3 or when all 16 (or 12) channel positions are written, the EAROM data corresponding to channel position number 1 (channel position 1 is selected) is read, and the fully automatic search operation is completed. If the upper end of band B3 is reached before all 16 (or 12) channels have been searched, the data at the EAROM addresses corresponding to reset channel position is erased. If these erased channel positions are selected, the D-A converter analog output is set to the lower end of band B1, the actual channel number is set to 0, and the AFT function is turned off.

When U-SEARCH key is input, the operation is exactly the same as the above described SEARCH or V-SEARCH except that initialization to the lower end of band B3 is performed and the search ends at the upper edge band B2.

Also, during fully automatic search, no key command can be input.

Sequentially Automatic Search

For sequentially automatic search, the channel position and actual channel number are the currently selected channel position.

When V-SEARCH key is input, search begins from the current position if the current band is B1 or B2, and from the lower end of band B1 if the current band is B3.

The search begins and when a video signal has been captured, the required data is automatically written into the EAROM, the search mode is cancelled, and the search is completed. When the upper end of the B2 band is reached, the tuning voltage output returns to the lower end of the B1 band and search continues.

When U-SEARCH key is input, search begins at the present location if the current band is B3. If it is B1 or B2, it begins at the lower end of band B3. The search method is exactly the same as for the above described V-SEARCH

except that when the upper end of band B3 is reached, the tuning voltage returns to the lower end of band B3.

When SEARCH key is input, search begins from the current location. For SEARCH, when the upper end of band B3 is reached, the tuning voltage returns to the lower end of band B1.

During sequentially automatic search, pressing channel selector keys cancels the search mode, ending the search and resulting in input of the channel selection command.

Search Speed

The tuning voltage rate of change varies between bands and within bands such that the search speed with respect to frequency is virtually constant over the entire range.

Because of the time constant associated with the integration circuit connected to the D/A OUT output, time delays occurs during the sweep. However, to compensate for this when UP and TIME BASE inputs are both high, the search speed is dropped to 1/16 of the sweep speed.

Table 3 shows the search speed for all bands without this reduced speed mode.

Table 3 Search Speed for Each Band

Band / Tuning voltage	B1	B2	B3, B4
0 ~ 1/4	1.16s	2.31s	9.22s
1/4 ~ 1/2	0.58	1.16	
1/2 ~ 1	0.58	1.16	4.61
Total	2.32	4.63	13.83

Note 1. The reference oscillator frequency is 455kHz.
2. The tuning voltage is given normalized to a value of 1.

Switching between fully automatic search and sequentially automatic search is accomplished by the FAM command as shown in Table 1. By using a switch, connecting the ϕ_C pin, with the K_3 pin results in fully automatic search while opening this connection results in switching to sequencially automatic search.

If the FAM command is attempted during a search, the command will not immediately be executed. After the search mode has been cancelled it will be input and the appropriate search mode, either fully automatic or automatic sequencial search, will be selected.

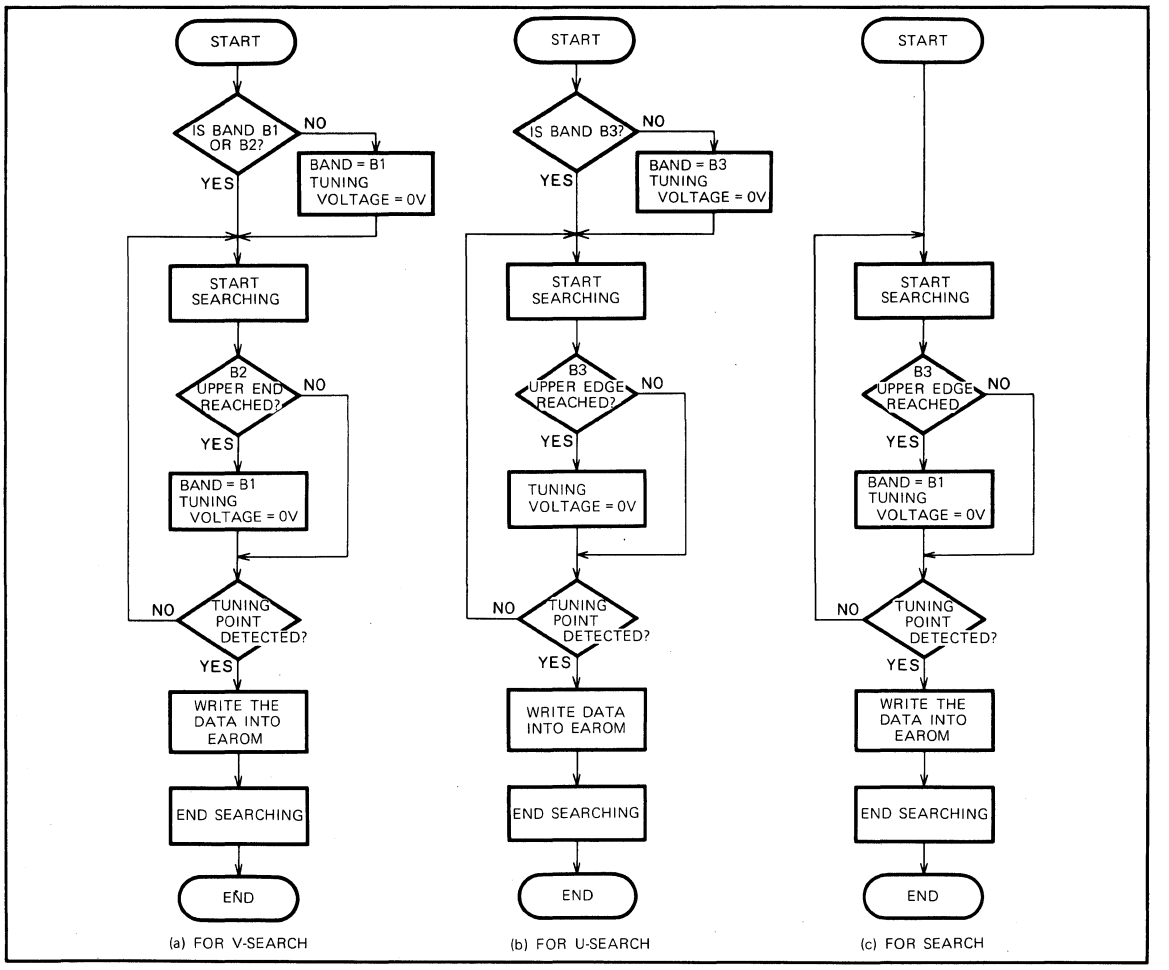

Fig. 7 Shows the flowchart of sequentially of search

Channel Selection Mode

When either a channel selection key is depressed or a channel selection command is input from a remote control receiver (described below), the data at the EAROM address corresponding to the selected channel position is read.

After the read data is set in the up/down counter, if the AFT control data read is on, 16 down pulses are applied, causing the up/down counter to count down and cause a corresponding output from the D-A converter. This is to enable pull-in at the optimum position of the video signal, using the digital AFT and linear AFT to be descfibed next.

If the AFT control data read is on, after 100 ms digital AFT is enabled. In addition, when 100ms has elapsed, the AFT output goes high and linear AFT is enabled. When the AFT control data is off, both digital and linear AFT functions are disabled.

Tuning Voltage Fine Adjustment (D-A UP, D-A DOWN)

By pressing the D-A UP and D-A DOWN key, it is possible to adjust the D-A converter analog output (that is the tuning voltage).

After channel selection, pressing the D-A UP or D-A DOWN keys turns AFT off and disables both digital and linear AFT functions. After this, the up or down signals are applied to the up/down counter and the D-A converter analog output changes. The rate of this change is 1/128 of the sweep speed, allowing sufficient fine adjustment.

When the key is released writing into the EAROM begins. At this time, the AFT on/off data is written as off.

EAROM Input/Output (CLOCK, C_1, C_2, C_3, DATA I/O)

This system makes use of an M5G1400P as an EAROM.

To control the M5G1400P, the M58486AP is provided with a reference clock (~14kHz) output clock, outputs C_1, C_2, and C_3 used to specify the mode, and a data input/output DATA I/O.

These inputs and outputs are controlled by the EAROM control circuit. The clock output is fixed at the V_{DD} level at all times except during memory read and write operations.

AFT Output

The AFT pin is connected to the AFT on/off pin (pin 15) of the M51251P, and is used to on/off control linear AFT. When the AFT output is high, linear AFT is enabled. When it is low or high impedance (open) linear AFT is disabled. Table 4 summarizes the AFT output for the various states.

Table 4 AFT Outputs for the Various Modes

Mode	AFT output level
Search mode (during sweep)	L
Search mode (during the 200ms that digital AFT is enabled)	Z
Channel selection mode (with linear AFT on)	H
Channel selection mode (with linear AFT off)	Z

Note 1. 'Z' indicates high-impedance (open)

Last Channel Memory

In this system when the power supply is applied, a last channel memory function selects the last channel position that was selected before the power supply was last removed.

This function is controlled by the last channel memory circuit such that when a channel is selected the data for the selected channel position is written into a specified address in the EAROM. Each time a channel is selected the data contents are updated so that the last channel selected before power is removed is always stored. When the power is applied, this data is read from the EAROM and used as the initial channel position selected.

Channel Position Display (P_1 ~ P_4)

By connecting transistors and LEDs to the 4x4 matrix formed by the P_1 ~ P_4 and ϕ_A ~ ϕ_D outputs, a 16-channel position display can be configured.

The display repetition frequency is 45Hz and the duty cycle is 23.5%. Fig. 8 gives an example of output timings. Note that when not used pins should be connected to V_{DD}.

Channel Number Display (O_1 ~ O_2)

The output O_1 ~ O_4 provide a two-digit (0 ~ 99) BCD output of the actual channel number. The upper and lower digits are output under the control of the ϕ_D and ϕ_B scan signals. Thus, by using a BCD seven-segment decoder (for example, the M53247P or equivalent), it is possible to display the actual channel number using a two-digit seven-segment display. Fig. 9 shows an example of timing for the outputs 0_1 ~ 0_4 used to display the actual channel number.

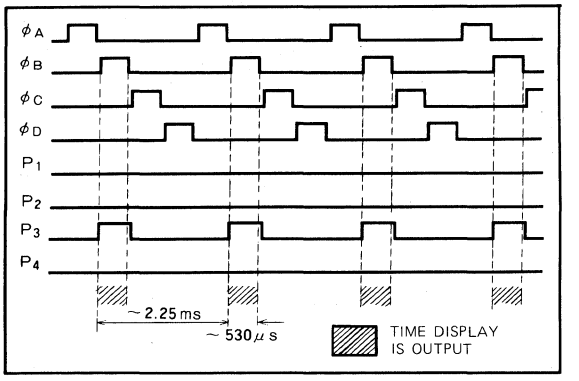

Fig. 8 Timing example for outputs P_1~P_4 and ϕ_A~ϕ_D (channel position = 7)

When the O_1 ~ O_4 outputs are used to display the channel position number in binary form the ϕ_A and ϕ_C scan signals are used for timing of the otuputs. For the channel positions 1 ~ 16, the O_1 ~ O_4 outputs are 0 ~ 15. Therefore, the channel position number can be displayed using seven-segment display elements. Fig. 9 shows a timing example of the outputs O_1 ~ O_4 used to display the channel position number. The outputs O_1 through O_4 use N-channel transistors in open drain configuration. When not used they should be connected to the V_{SS} pin.

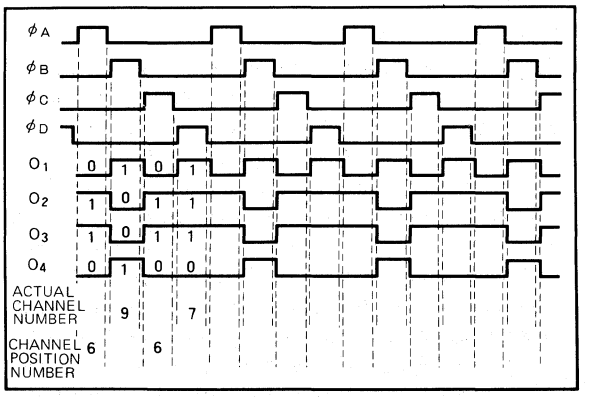

Fig. 9 Timing example for outputs 0_1~0_4 and ϕ_A~ϕ_D (Actual channel number setting line 79 Channel position number 7)

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Actual Channel Number Control Inputs (CHN 10, CHN 1)
When CHN 10 key is input, the upper digit of the actual channel number is incremented by 1, cycling back to 0 after reaching 9. In the same manner, when CHN 1 key is input, the lower digit is incremented by 1. Therefore, by using these inputs, the actual channel number can be changed with respect to the channel position, and by using the STORE command described below, the proper corresponding channel numbers can be selected.

Channel Position Control Inputs (CHP-UP, CHP-DOWN)
When either CHP-UP or CHP-DOWN key is input, the contents of the address counter are incremented or decremented by1, the channel position display changing accordingly. But data is not read from the EAROM, so the D-A converted analog output, band, AFT output and actual channel do not change.

When these commands are input, the channel position is changed, and the STORE command described below is input, data is written into the EAROM at the address corresponding to the displayed channel position. This enables, for example, such copying operations as writing the same data in position 3 as stored in position 1.

EAROM Write Command (STORE)
When the STORE command is input, data is written into the EAROM at the address corresponding to the currently displayed channel position. This STORE command is used to change the actual channel number and to perform memory copying operations.

Audio Control Output (MUTE)
In the search mode or channel selection mode, the MUTE output changes to a high level, enabling the muting function which lowers the sound level to the minimum level. This output is normally low.

Power-on reset ($\overline{AC}$)
By connecting a capacitor between the $\overline{AC}$ pin and the V_{SS} pin, the power-on reset function is enabled upon applying power to the M58486AP.

When the power-on reset operates, the last channel memory function is enable the channel position selected before the power was removed, is selected.

Remote Control Inputs ($\overline{CH\ UP}$, $\overline{CH\ DOWN}$, $\overline{CH\ RESET}$)
If the $\overline{CH\ UP}$, $\overline{CH\ DOWN}$, and $\overline{CH\ RESET}$ inputs are connected to the corresponding pins on, for example, a remote control receiver device such as the M58485P or M58487AP, direct remote control of channel selection, channel up, and channel down functions is possible.

Channel Lock Input (CH LOCK)
By using the input combination of the key input K3 and the scan signal ϕ_B, the CH LOCK command is input. This command prohibits the CHP1 ~ CHP16, CHP-UP, AND CHP-DOWN keys commands as well as the remote control $\overline{CH\text{-}UP}$, $\overline{CH\text{-}DOWN}$, and $\overline{CH\text{-}RESET}$. This command is independent of any other key commands and can be input simultaneously input with any command except the channel selection commands CHP1~CHP16.

Number of Channels Selection Input (CEX)
The CEX input is provided with a built-in pull-up resistance and when at the high level (or open), the M58486AP for 16 channels. When it is at the low level the M58486AP accommodates 12 channels.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{DD}	Supply voltage	With respect to V_{SS}	−0.3～15	V
V_I	Input voltage		$V_{SS} \leqq V_I \leqq V_{DD}$	V
V_O	Output voltage		$V_{SS} \leqq V_O \leqq V_{DD}$	V
Pd	Power dissipation	Ta=25°C	300	mW
Topr	Operating temperature		−30～70	°C
Tstg	Storage temperature		−40～125	°C

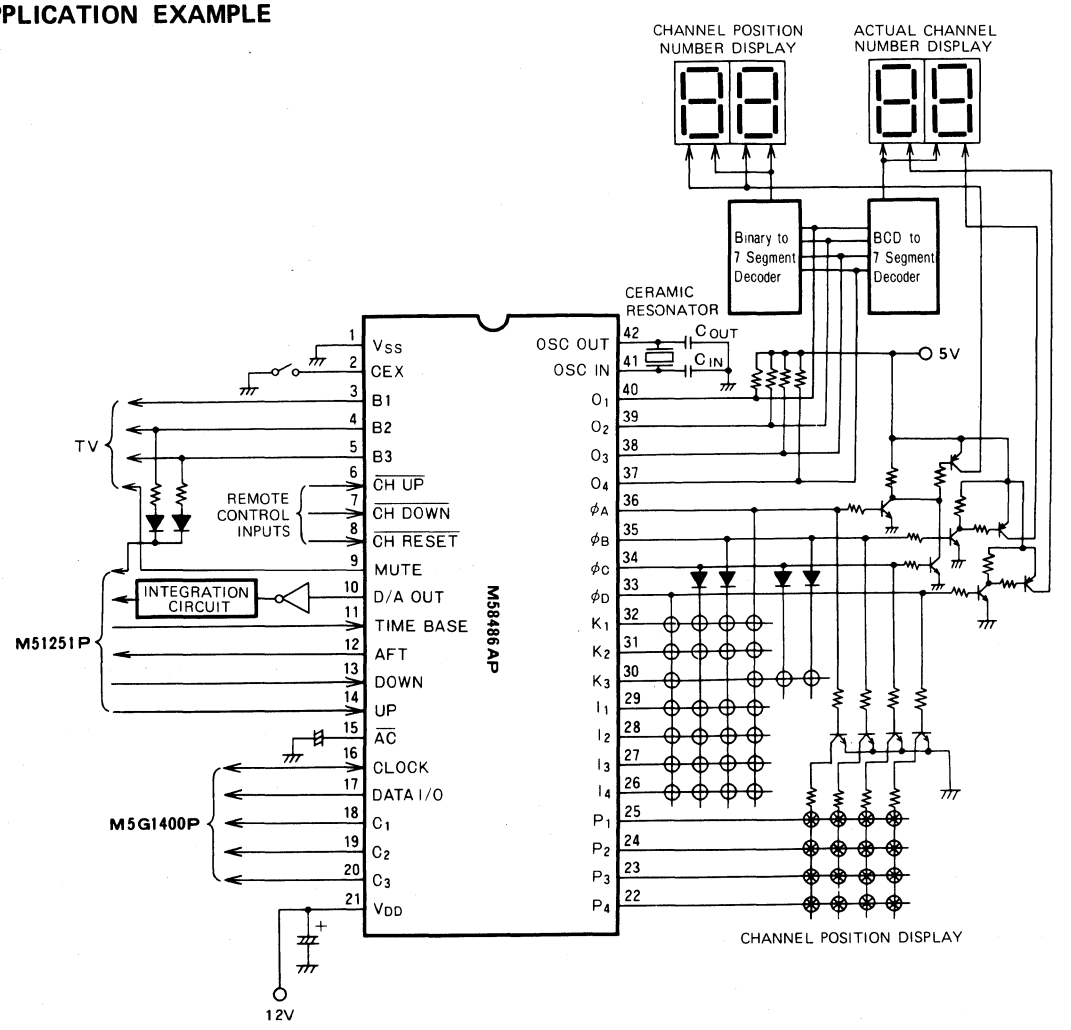
RECOMMENDED OPERATING CONDITIONS

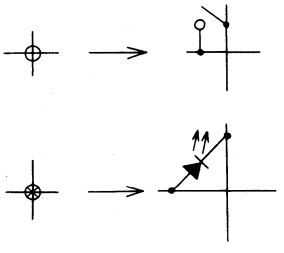
Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{DD}	Supply voltage	11	12	13	V
V_{IH}	High-level input voltage	$V_{DD}-3$	V_{DD}	V_{DD}	V
V_{IL}	Low-level input voltage	0	0	3	V
f_{OSC}	Oscillation frequency		455		kHz
			480		kHz

ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{DD}=12V, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{DD}	Operational supply voltage	Ta=−30～70°C, f_{OSC}=455kHz	11	12	13	V
I_{DD}	Supply current	f_{OSC}=455kHz		0.5	6	mA
R_I	Pull-up resistance, $\overline{\text{CH UP}}$, $\overline{\text{CH DOWN}}$, $\overline{\text{CH RESET}}$, UP, DOWN, TIME BASE, CEX			50		kΩ
R_I	Pull-up resistance, $\overline{\text{AC}}$			100		kΩ
R_I	Pull-down resistance, I_1～I_4, K_1～K_3			50		kΩ
I_{OH}	High-level output current, ϕ_A～ϕ_D	V_O=10V	−5			mA
I_{OH}	High-level output current, B1～B3, MUTE	V_O=10V	−1			mA
I_{OL}	Low-level output current, B1～B3, MUTE	V_O=2V	2			mA
I_{OH}	High-level output current, AFT, D/A OUT	V_O=10V	−1.5			mA
I_{OL}	Low-level output current, AFT	V_O=2V	1			mA
I_{OL}	Low-level output current, D/A OUT	V_O=2V	1.5			mA
I_{OZH}	Off-state output current, AFT	V_O=12V			1	μA
I_{OZL}	Off-state output current, AFT	V_O=0V			−1	μA
V_{OH}	High-level output voltage, CLOCK, C1～C3	I_{OH}=−0.5mA	11			V
V_{OL}	Low-level output voltage, CLOCK, C1～C3	I_{OL}=1mA			2	V
V_{OH}	High-level output voltage, DATA I/O	I_{OH}=−0.2mA	11			V
V_{OL}	Low-level output voltage, DATA I/O	I_{OL}=0.5mA			2	V
I_{OZH}	Off-state output current, DATA I/O	V_O=12V			1	μA
I_{OZL}	Off-state output current, DATA I/O	V_O=0V			−1	μA
V_{OH}	High-level output voltage, P_1～P_4	I_{OH}=−40mA	10			V
I_{OZL}	Off-state output current, P_1～P_4	V_O=2V			10	μA
I_{OL}	Low-level output current, O_1～O_4	V_O=0.4V	1.6			mA
I_{OZH}	Off-state output current, O_1～O_4	V_O=10V			1	μA

APPLICATION EXAMPLE





22-FUNCTION REMOTE CONTROL RECEIVERS

DESCRIPTION

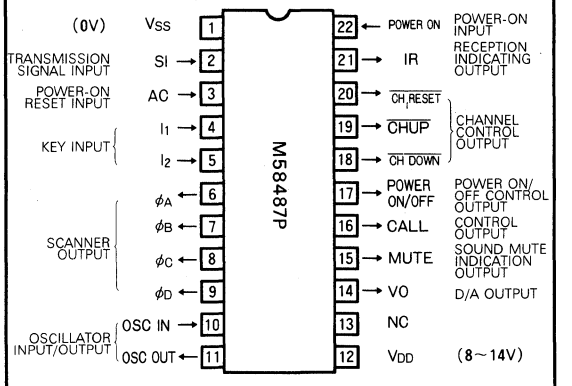
The M58487P is a 22-function remote-control receiver circuit manufactured by aluminum-gate CMOS technology for use in television receivers, audio equipment, and the like, using infrared for transmission. It enables direct control of 8 functions at the receiver.

The M58487P is intended for use with an M58480P or M58484P transmitter.

FEATURES

- Single power supply
- Wide supply voltage range: 8V~14V
- Low power dissipation
- On-chip oscillator
- Low-cost LC or ceramic oscillator used in determining the reference frequency (480kHz or 455kHz)
- Information is transmitted by means of pulse code modulation
- Good noise immunity—instructions are not executed unless same code is received three or more times in succession.
- Single transmission frequency (40kHz or 38kHz) for carrier wave
- 16 TV channels selected directly
- Three analog functions—volume, brightness, and color saturation—are independently controlled to 64 stages by three 6-bit D/A converters
- 8 commands are controlled at the M58487P receiver
- Has large tolerance in operating frequency between the transmitter and the receiver
- Can be connected with an M51231P or equivalent touch control channel selector IC

PIN CONFIGURATION (TOP VIEW)



Outline 22P1

NC : NO CONNECTION

APPLICATIONS

- Remote-control receiver for TV or other applications

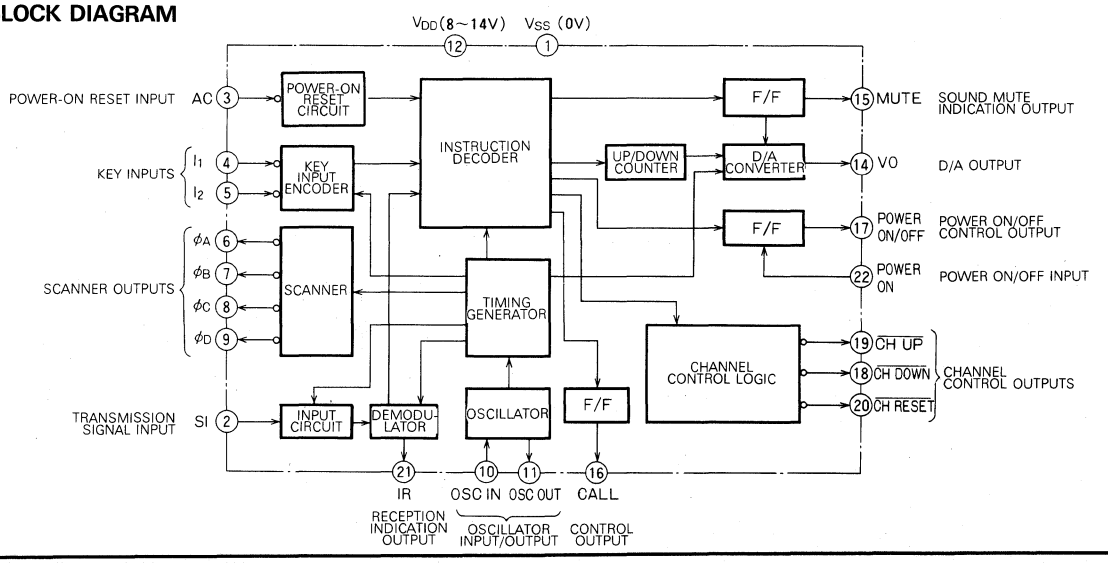
FUNCTIONS

The M58487P is designed to decode and execute instructions after three successive receptions of the identical instruction code, providing a good noise immunity.

Instructions comprise direct selection of 16 channels, channel position up and down, volume up and down, brightness up and down, color saturation up and down, normalization of volume, brightness and color saturation, sound mute on and off, TV main power on and off, and output CALL on and off.

In addition, 8 functional instructions can be entered from the receiver side.

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

FUNCTION DESCRIPTION

Oscillator

As the oscillator is on-chip, oscillation frequency is easily obtained by connecting an external LC network or ceramic resonator between the OSC IN and OSC OUT terminals. Figs. 1 and 2 show typical oscillators.

Fig. 1 An example of an oscillator (when a ceramic resonator is used)

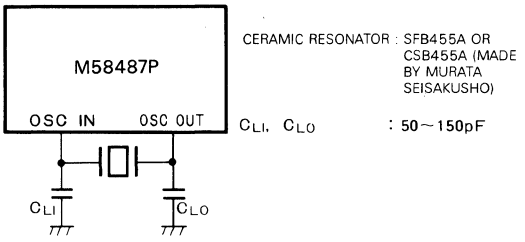
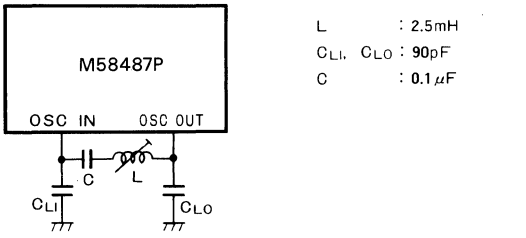


Fig. 2 An example of an oscillator (when a LC network is used)



Reception Signal Input Circuit and Demodulation Circuit

The reception signal caught by the photo detector is amplified in the amplifier and added to the SI, where it is converted into a pulse signal in the input circuit to be sent to the demodulation circuit. In the demodulation circuit, the pulse interval of the pulse signal is judged and then converted into the digital code to be sent to the instruction decoder.

SI is applied as amplified, either through a capacitor coupling (Fig. 3) or directly as a pulse signal (Figs. 4 and 5). A Schmitt trigger circuit is provided in the SI input circuit for preventing spurious operation due to noise.

Fig. 3 SI input waveform (when applied through a capacitor coupling)

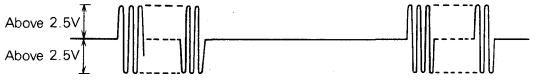


Fig. 4 SI input waveform (when applied directly)

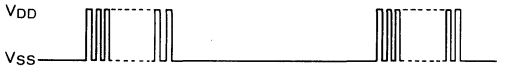
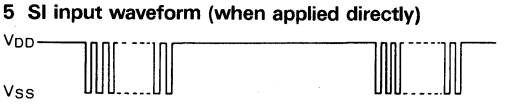


Fig. 5 SI input waveform (when applied directly)



Instruction Decoder

The instruction decoder starts to function after receiving the same instruction code three or more times in succession from the demodulation circuit.

Table 1 shows the relations between the reception code and instruction function. To prevent spurious operation, there is no code 000000.

Table 1 Relations between reception codes and instructions

Reception code						Function	Remarks
D_1	D_2	D_3	D_4	D_5	D_6		
1	1	0	0	0	0	VO UP	Volume up
0	0	1	0	0	0	VO DOWN	Volume down
1	0	0	1	0	0	MUTE	Sound mute on/off
0	1	0	1	0	0	VO(1/3)	Normalization of volume
1	0	1	1	0	0	CALL	Output CALL on/off
0	1	1	1	0	0	POWER ON/OFF	Power on/off
0	0	0	0	1	0	CH 1	Direct channel selection (Direct access)
1	0	0	0	1	0	CH 2	
0	1	0	0	1	0	CH 3	
1	1	0	0	1	0	CH 4	
0	0	1	0	1	0	CH 5	
1	0	1	0	1	0	CH 6	
0	1	1	0	1	0	CH 7	
1	1	1	0	1	0	CH 8	
0	0	0	1	1	0	CH 9	
1	0	0	1	1	0	CH 10	
0	1	0	1	1	0	CH 11	
1	1	0	1	1	0	CH 12	
0	0	1	1	1	0	CH 13	
1	0	1	1	1	0	CH 14	
0	1	1	1	1	0	CH 15	
1	1	1	1	1	0	CH 16	

Key Inputs

8 different instructions are input by a 2X4 keyboard matrix consisting of inputs I_1~I_2 and scanner outputs ϕA~ϕD. Protection is also available against chattering within 10ms.

As entry priority is given to each key, depression of more than two keys at the same time makes the key with higher priority effective. For the scanner output, priority is given in the order of ϕA, ϕB, ϕC, and ϕD, and I_1 takes precedence over I_2 if the scan output is the same. When two or more keys are depressed at the same time, scanner outputs may short-circuit, disabling all functions.

While one of the keys is depressed, instructions from the transmitter are ignored.

Table 2 shows the relations between the keyboard matrix and the instructions.

Table 2 Relations between keyboard matrix and instructions

Key input \ Scanner output	ϕD	ϕC	ϕB	ϕA
I_1	POWER ON/OFF	VO UP	MUTE	CH UP
I_2	CALL	VO DOWN	VO(1/3)	CH DOWN

Indication of Reception

As soon as an identical code is received three times, output IR turns from low-level to high-level. Thus reception of an instruction from the transmitter can be indicated by an LED connected to the output IR.

Output VO

As the 6-bit D/A converter is contained internally, analog value can be controlled to 64 stages independently. The D/A converter is pulse-width modulator, the reception frequency is 1.25kHz (when f_{OSC} = 480kHz) and minimum pulse width is 12.5μs.

Analog value can be incremented/decremented at a rate of about 1 step/0.1 second through the remote control or the key input. The time required for increasing the analog value from the minimum to the maximum is about 6.6 seconds (when f_{OSC} = 480kHz).

It is also possible to set the analog value to 1/3 of its maximum value by means of the remote control or the key input (normalization).

Sound Mute

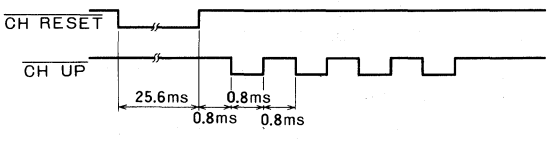
Sound mute on/off is controlled through the remote control or the key input. When sound mute is on, output VO goes low, and output MUTE goes high.

Sound mute is automatically released from ON when the output VO is either incremented or decremented by remote control or the key input.

Channel Control

Channel control is attained through outputs $\overline{\text{CH UP}}$, $\overline{\text{CH DOWN}}$ and $\overline{\text{CH RESET}}$. With respect to direct channel selection by the remote-control operation, a single pulse appears on output $\overline{\text{CH RESET}}$ first, and then the pulses whose number is deducted by one from the selected channel appear on the output $\overline{\text{CH UP}}$. Up and down channel switching is controlled by presenting a single pulse on the output $\overline{\text{CH UP}}$ or $\overline{\text{CH DOWN}}$. Thus it can be connected with an M51231P or equivalent touch-control channel selector IC.

Fig. 6 Timing chart of channel control (when fosc = 480kHz)



During direct channel selection, up or down, output VO goes low for 50~100ms.

Outputs, $\overline{\text{CH UP}}$, $\overline{\text{CH DOWN}}$, and $\overline{\text{CH RESET}}$ are the open-drain type of N-channel transistor.

Power On/Off

The remote control or the key input makes it possible to turn the POWER ON/OFF output from low to high or vice versa. While the POWER ON/OFF output is low, all channel and analog controls through the remote control are disabled, as are all through the keyboard.

Output CALL

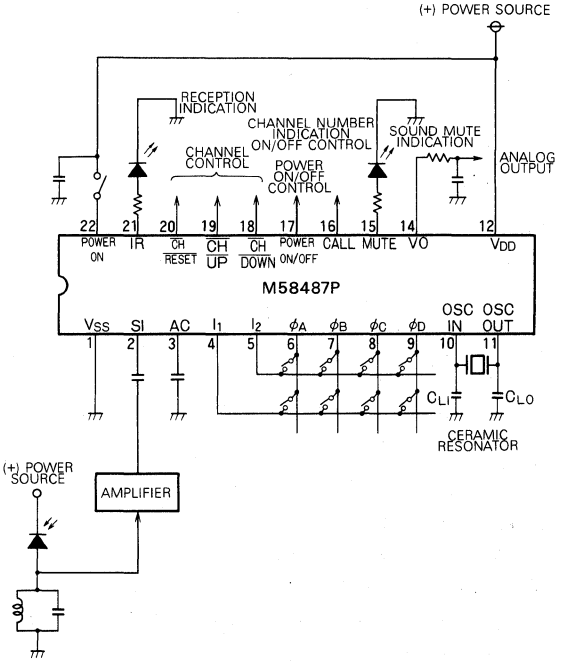
The output CALL is turned high or low by remote control or the key input. This output effects on/off control of channel number indication or change of receiving modes of multi-channel broadcasting.

Power-on Reset

Attaching a capacitor to terminal AC activates the power-on reset when power is on to the M58487P.

Activation of the power-on reset function sets output VO to 1/3 of its maximum value and turns the POWER ON/OFF and CALL outputs to low-level.

An Example of an Application Circuit



MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{DD}	Supply voltage	With respect to V_{SS}	−0.3～15	V
V_I	Input voltage		$V_{SS} \leqq V_I \leqq V_{DD}$	V
V_O	Output voltage		$V_{SS} \leqq V_O \leqq V_{DD}$	V
P_d	Maximum power dissipation	Ta=25℃	300	mW
T_{opr}	Operating free-air temperature range		−30～70	℃
T_{stg}	Storage temperature range		−40～125	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{DD}	Supply voltage	8	12	14	V
f_{OSC}	Oscillation frequency		455		kHz
			480		kHz
V_I	Input voltage, SI	5			V_{P-P}

ELECTRICAL CHARACTERISTICS (Ta=25℃, V_{DD}=12V, unless otherwise noted.)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{DD}	Operating supply voltage	Ta=−30～70℃, f_{OSC}=455kHz	8	12	14	V
I_{DD}	Supply current	f_{OSC}=455kHz		2	5	mA
R_I	Pull-up resistances, I_1, I_2			20		kΩ
I_{OL}	Low-level output currents, ϕ_A～ϕ_D	V_O=12V	5			mA
I_{OL}	Low-level output currents, $\overline{\text{CH RESET}}$, $\overline{\text{CH UP}}$, $\overline{\text{CH DOWN}}$	V_O=12V	20			mA
I_{OZH}	Off-state output currents, $\overline{\text{CH RESET}}$, $\overline{\text{CH UP}}$, $\overline{\text{CH DOWN}}$	V_O=12V			1	μA
I_{OH}	High-level output current, VO	V_O= 0 V	−7			mA
I_{OL}	Low-level output current, VO	V_O=12V	7			mA
I_{OH}	High-level output currents, POWER ON/OFF, CALL, MUTE	V_O= 0 V	−20			mA
I_{OL}	Low-level output currents, POWER ON/OFF, CALL, MUTE	V_O=12V	5			mA
I_{OH}	High-level output current, IR	V_O= 0 V	−15			mA
I_{OL}	Low-level output current, IR	V_O=12V	5			mA

M58487AP

24-FUNCTION REMOTE-CONTROL RECEIVERS

DESCRIPTION

The M58487AP is a 24-function remote-control receiver circuit manufactured by aluminum-gate CMOS technology for use in television receivers, audio equipment, and the like, using infrared for transmission. It enables direct control of 8 functions at the receiver.

The M58487AP is intended for use with an M58480P or M58484P transmitter.

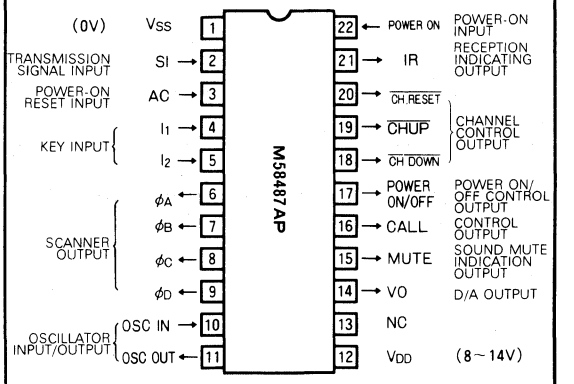
FEATURES

- Wide supply voltage range: 8V~14V
- Single power supply
- Low power dissipation
- On-chip oscillator
- Low-cost LC or ceramic oscillator used in determining the reference frequency (480kHz or 455kHz)
- Information is transmitted by means of pulse code modulation
- Good noise immunity—instructions are not executed unless same code is received three or more times in succession.
- Single transmission frequency (40kHz or 38kHz) for carrier wave
- 16 TV channels selected directly
- Three analog functions—volume, brightness, and color situration—are independently controlled to 64 stages by three 6-bit D/A converters
- 8 commands are controlled at the M58487AP receiver
- Has large tolerance in operating frequency between the transmitter and the receiver.
- Can be connected with an M51231P or equivalent touch control channel selector IC

APPLICATION

- Remote-control receiver for TV or other applications

PIN CONFIGURATION (TOP VIEW)



Outline 22P1

NC NO CONNECTION

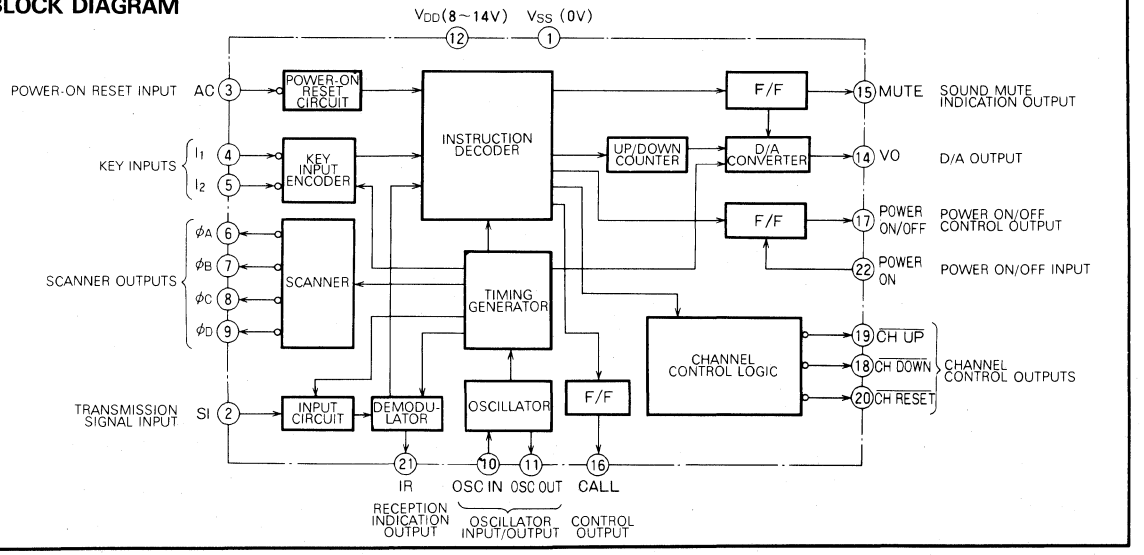
FUNCTION

The M58487AP is designed to decode and execute instructions after three successive receptions of the identical instruction code, providing a good noise immunity.

Instructions comprise direct selection of 16 channels, channel position up and down, volume up and down, brightness up and down, color saturation up and down, normalization of volume, brightness and color saturation, sound mute on and off, TV main power on and off, and output CALL on and off.

In addition, 8 functional instructions can be entered from the receiver side.

BLOCK DIAGRAM



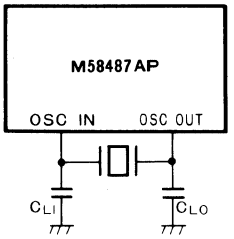
MITSUBISHI ELECTRIC

FUNCTIONAL DESCRIPTION

Oscillator

As the oscillator is on-chip, oscillation frequency is easily obtained by connecting an external LC network or ceramic resonator between the OSC IN and OSC OUT terminals. Figs. 1 and 2 show typical oscillators.

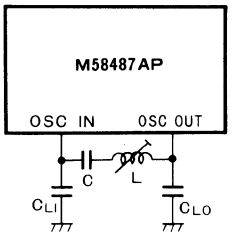
Fig. 1 An example of an oscillator (when a ceramic resonator is used)



CERAMIC RESONATOR : SFB455A OR CSB455A (MADE BY MURATA SEISAKUSHO)

C_{LI}, C_{LO} : 50~150pF

Fig. 2 An example of an oscillator (when a LC network is used)



L : 2.5mH

C_{LI}, C_{LO} : 90pF

C : 0.1μF

Reception Signal Input Circuit and Demodulation Circuit

The reception signal caught by the photo detector is amplified in the amplifier and added to the SI, where it is converted into a pulse signal in the input circuit to be sent to the demodulation circuit. In the demodulation circuit, the pulse interval of the pulse signal is judged and then converted into the digital code to be sent to the instruction decoder.

SI is applied as amplified, either through a capacitor coupling (Fig. 3) or directly as a pulse signal (Figs. 4 and 5). A Schmitt trigger circuit is provided in the SI input circuit for preventing spurious operation due to noise.

Fig. 3 SI input waveform (when applied through a capacitor coupling)

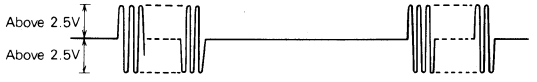


Fig. 4 SI input waveform (when applied directly)

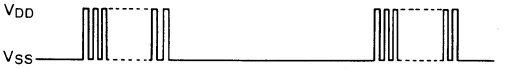
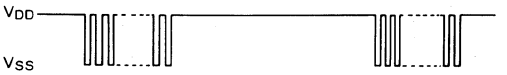


Fig. 5 SI input waveform (when applied directly)



Instruction Decoder

The instruction decoder starts to function after receiving the same instruction code three or more times in succession from the demodulation circuit.

Table 1 shows the relations between the reception code and instruction function. To prevent spurious operation, there is no code 000000.

Table 1 Relations between reception codes and instructions

Reception code						Function	Remarks
D_1	D_2	D_3	D_4	D_5	D_6		
1	0	0	0	0	0	CH UP	Channel up
0	1	0	0	0	0	CH DOWN	Channel down
1	1	0	0	0	0	VO UP	Volume up
0	0	1	0	0	0	VO DOWN	Volume down
1	0	0	1	0	0	MUTE	Sound mute on/off
0	1	0	1	0	0	VO(1/3)	Normalization of volume
1	0	1	1	0	0	CALL	Output CALL on/off
0	1	1	1	0	0	POWER ON/OFF	Power on/off
0	0	0	0	1	0	CH 1	Direct channel selection (Direct access)
1	0	0	0	1	0	CH 2	
0	1	0	0	1	0	CH 3	
1	1	0	0	1	0	CH 4	
0	0	1	0	1	0	CH 5	
1	0	1	0	1	0	CH 6	
0	1	1	0	1	0	CH 7	
1	1	1	0	1	0	CH 8	
0	0	0	1	1	0	CH 9	
1	0	0	1	1	0	CH 10	
0	1	0	1	1	0	CH 11	
1	1	0	1	1	0	CH 12	
0	0	1	1	1	0	CH 13	
1	0	1	1	1	0	CH 14	
0	1	1	1	1	0	CH 15	
1	1	1	1	1	0	CH 16	

Key Inputs

8 different instructions are input by a 2 x 4 keyboard matrix consisting of inputs I_1 ~ I_2 and scanner outputs ϕA ~ ϕD, Protection is also available against chattering within 10ms.

As entry priority is given to each key, depression of more than two keys at the same time makes the key with higher priority effective. For the scanner output, priority is given in the order of ϕA, ϕB, ϕC, and ϕD, and I_1 takes precedence over I_2 if the scan output is the same. When two or more keys are depressed at the same time, scanner outputs may short-circuit, disabling all functions.

While one of the keys is depressed, instructions from the transmitter are ignored.

Table 2 shows the relations between the keyboard matrix and the instructions.

Table 2 Relations between keyboard matrix and instructions

Key input \ Scanner output	ϕD	ϕC	ϕB	ϕA
I_1	POWER ON/OFF	VO UP	MUTE	CH UP
I_2	CALL	VO DOWN	VO(1/3)	CH DOWN

Indication of Reception

As soon as an identical code is received three times, output IR turns from low-level to high-level. Thus reception of an instruction from the transmitter can be indicated by an LED connected to the output IR.

Output VO

As the 6-bit D/A converter is contained internally, analog value can be controlled to 64 stages independently. The D/A converter is pulse-width modulator, the reception frequency is 1.25kHz (when f_{OSC} = 480kHz) and minimum pulse width is 12.5μs.

Analog value can be incremented/decremented at a rate of about 1 step/0.1 second through the remote control or the key input. The time required for increasing the analog value from the minimum to the maximum is about 6.6 seconds (when f_{OSC} = 480kHz).

It is also possible to set the analog value to 1/3 of its maximum value by means of the remote control or the key input (normalization).

Sound Mute

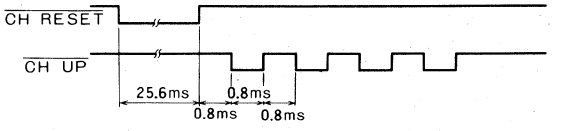
Sound mute on/off is controlled through the remote control or the key input. When sound mute is on, output VO goes low, and output MUTE goes high.

Sound mute is automatically released from ON when the output VO is either incremented or decremented by remote control or the key input.

Channel Control

Channel control is attained through outputs $\overline{\text{CH UP}}$, $\overline{\text{CH DOWN}}$ and $\overline{\text{CH RESET}}$. With respect to direct channel selection by the remote-control operation, a single pulse appears on output $\overline{\text{CH RESET}}$ first, and then the pulses whose number is deducted by one from the selected channel appear on the output $\overline{\text{CH UP}}$. Up and down channel switching is controlled by presenting a single pulse on the output $\overline{\text{CH UP}}$ or $\overline{\text{CH DOWN}}$. Thus it can be connected with an M51231P or equivalent touch-control channel selector IC.

Fig. 6 Timing chart of channel control (when f_{OSC} = 480kHz)



During direct channel selection, up or down, output VO goes low for 50~100ms.

Outputs, $\overline{\text{CH UP}}$, $\overline{\text{CH DOWN}}$, and $\overline{\text{CH RESET}}$ are the open-drain type of N-channel transistor.

Power On/Off

The remote control or the key input makes it possible to turn the POWER ON/OFF output from low to high or vice versa. While the POWER ON/OFF output is low, all channel and analog controls through the remote control are disabled, as are all through the keyboard.

Output CALL

The output CALL is turned high or low by remote control or the key input. This output effects on/off control of channel number indication or change of receiving modes of multi-channel broadcasting.

Power-on Reset

Attaching a capacitor to terminal AC activates the power-on reset when power is on to the M58487AP.

Activation of the power-on reset function sets output VO to 1/3 of its maximum value and turns the POWER ON/OFF and CALL outputs to low-level.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{DD}	Supply voltage	With respect to V_{SS}	−0.3 ~ 15	V
V_I	Input voltage		$V_{SS} \leqq V_I \leqq V_{DD}$	V
V_O	Output voltage		$V_{SS} \leqq V_O \leqq V_{DD}$	V
Pd	Maximum power dissipation	Ta = 25℃	300	mW
Topr	Operating temperature		−30 ~ 70	℃
Tstg	Storage temperature		−40 ~ 125	℃

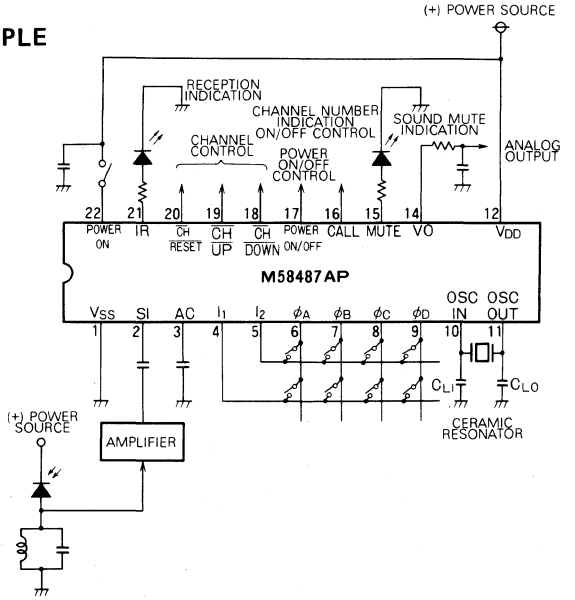
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{DD}	Supply voltage	8	12	14	V
f_{OSC}	Oscillation frequency		455		kHz
			480		kHz
V_I	Input voltage, SI	5			Vp-p
V_{IH}	High-level input voltages, I_1, I_2	$0.7 \times V_{DD}$	V_{DD}	V_{DD}	V
V_{IL}	Low-level input voltages, I_1, I_2	0	0	$0.3 \times V_{DD}$	V

ELECTRICAL CHARACTERISTICS (Ta = 25℃, V_{DD} = 12V, unless otherwise noted.)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{DD}	Operating supply voltage	Ta = −30 ~ 70℃, f_{OSC} = 455kHz	8	12	14	V
I_{DD}	Supply current	f_{OSC} = 455kHz		2	5	mA
R_I	Pull-up resistances, I_1, I_2			20		kΩ
I_{OL}	Low-level output currents, ϕ_A ~ ϕ_D	V_O = 12V	5			mA
I_{OL}	Low-level output currents, $\overline{\text{CH RESET}}$, $\overline{\text{CH UP}}$, $\overline{\text{CH DOWN}}$	V_O = 12V	20			mA
I_{OZH}	Off-state output currents, $\overline{\text{CH RESET}}$, $\overline{\text{CH UP}}$, $\overline{\text{CH DOWN}}$	V_O = 12V			1	μA
I_{OH}	High-level output current, VO	V_O = 0 V	−7			mA
I_{OL}	Low-level output current, VO	V_O = 12V	7			mA
I_{OH}	High-level output currents, POWER ON/OFF, CALL, MUTE	V_O = 0 V	−20			mA
I_{OL}	Low-level output currents, POWER ON/OFF, CALL, MUTE	V_O = 12V	5			mA
I_{OH}	High-level output current, IR	V_O = 0 V	−15			mA
I_{OL}	Low-level output current, IR	V_O = 12V	5			mA

APPLICATION EXAMPLE



VIDEO DISPLAY GENERATOR

DESCRIPTION

The M5C6847P-1 is a color or monochrome television interface device, fabricated using N-channel silicon gate ED-MOS technology. The M5C6847P-1 has a 64-character (6-bit ASCII code) generator and memory interface.

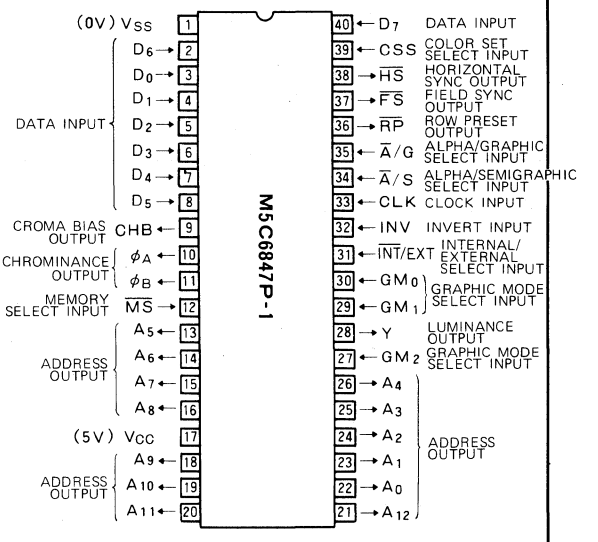
FEATURES

- Can be easily connected to the MELPS 85 series 8-bit CPUs.
- Alphanumeric display: 4 modes
- Graphic display: 8 modes
- Can connect directly with the M51342P RF modulator
- Alphanumeric display: 32 characters per line by 16 lines
- Character generator for 64 ASCII characters
- Can be used with an external character generator
- Generates composite video signals
- Generates intensity signal Y, color signal R-Y (ϕA) and B-Y (ϕB)
- Display RAM capacity (depends on mode): 512~6K bytes
- Single 5V power supply
- Interchangeable with the Motorola's MC6847P in pin configuration

APPLICATION

- Microcomputer system or terminals using a color or monochrome CRT.

PIN CONFIGURATION (TOP VIEW)

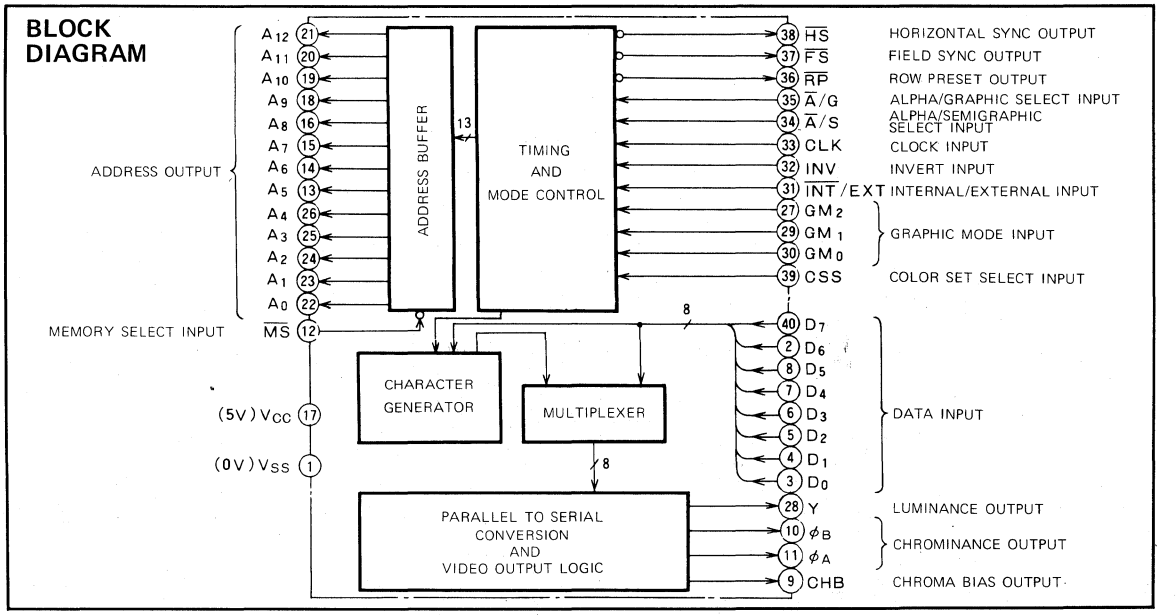


Outline 40P1

FUNCTION

The picture on the television set is composed of the synchronization signals such as horizontal synchronization signal, vertical synchronization signal and color burst signal, and syncronizing serial data. M5C6847P-1 can generate these signals. The information or data to be shown on the screen is written in the display memory by the CPU. (When the picture is to be composed on a CRT) the data for one screen in the display memory is read in the order of th scan cycles and synchronization signals are added. This

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

serial is sent to the RF modulator. The M5C6847P-1 performs these functions by reading the display memory in the order of the CRT scan, adding the required synchronization signals such as luminance signal, color signal and then transferring the data stream serially to the RF modulator.

OPERATION

Address Outputs (A_{12}~A_0)

Thirteen address lines are used by the M5C6847P-1 to access the display memory (refresh memory). The starting address of the display memory is located at the upper-left corner of the display screen. As the television sweeps from the left to right and top to bottom, the VDG increments the RAM display address. The address lines are TTL-compatible and may be forced in a high-impedance state when input $\overline{MS}$ goes low.

Data Input (D_7~D_0)

Eight TTL-compatible data lines are used to input data from the display memory to be processed by the M5C-6847P-1. The data is interpreted and transformed into video analog level signals.

Video Output (Y, ϕ_A, ϕ_B, CHB)

These video outputs are used to transfer luminance and color information of pictures displayed on television with standard NTSC systems. These outputs can be directly connected to the RF modulator M51342P.

Luminance Output (Y)

The luminance output is a 6-level analog output. The six level analog outputs contain composite, blank, and four levels of video intensity.

Chrominance Output (ϕ_A)

The chrominance output ϕ_A is a 3-level analog output. The signal is used in combination with ϕ_B and Y to specify one of eight colors.

Chrominance Output (ϕ_B)

The chrominance output ϕ_B is a 4-level analog output. These levels of the signal are used in combination with ϕ_A and Y to specify one of eight colors. The other level is used to specify the time of the color burst reference signal.

Chroma Bias Output (CHB)

The chroma bias output is a single level analog output that provides the DC reference for chrominance outputs.

Synchronization Input ($\overline{MS}$, CLK)

Memory Select Input ($\overline{MS}$)

This is a TTL compatible input. When it goes low-level, address outputs (A_{12}~A_0) are forced in high-impedance state. When other devices such as the CPU access the display memory, it must be kept at low-level to prevent interference.

Clock input (CLK)

The clock input requires a 3.579545 MHz clock with a duty cycle of 50±5%. The M51342P RF modulator may be used to supply the 3.579545 MHz clock.

Synchronization output ($\overline{FS}$, $\overline{HS}$, $\overline{RP}$)

The synchronization outputs $\overline{FS}$, $\overline{HS}$ and $\overline{RP}$ are TTL-compatible and provide circuits, exterior to the M5C6847P-1 states.

Table 1 Operation modes

$\overline{A}/G$	$\overline{A}/S$	$\overline{INT}/EXT$	INV	GM_2	GM_1	GM_0	Mode
0	0	0	0	X	X	X	Internal alphanumerics
0	0	0	1	X	X	X	Internal alphanumerics inverted
0	0	1	0	X	X	X	External alphanumerics
0	0	1	1	X	X	X	External alphanumerics inverted
0	1	0	X	X	X	X	Semigraphics 4
0	1	1	X	X	X	X	Semigraphics 6
1	X	X	X	0	0	0	64× 64 Color graphics
1	X	X	X	0	0	1	128× 64 Graphics
1	X	X	X	0	1	0	128× 64 Color graphics
1	X	X	X	0	1	1	128× 96 Graphics
1	X	X	X	1	0	0	128× 96 Color graphics
1	X	X	X	1	0	1	128×192 Graphics
1	X	X	X	1	1	0	128×192 Color graphics
1	X	X	X	1	1	1	256×192 Graphics

Note 1: X is "don't care" bit

Table 2 Alphanumeric mode display memory, color and display element

Mode	Memory capacity (bits)	Color	Display elements
Internal alphanumerics	512×8	2	8 dots, 12 dots; Character is 5 x 7 dots
External alphanumerics	512×8	2	8 dots, 12 dots
Semigraphics 4	512×8	8	Elements 64×32
Semigraphics 6	512×8	4	Elements 64×48

Table 3 Graphic mode display memory, color and display element

Mode	Memory capacity (bits)	Color	Display elements
64× 64 Color graphics	1K×8	4	64×64
128× 64 Graphics	1K×8	2	128×64
128× 64 Color graphics	2K×8	4	
128× 96 Graphics	2K×8	2	128×96
128× 96 Color graphics	3K×8	4	
128×192 Graphics	3K×8	2	128×192
128×192 Color graphics	6K×8	4	
256×192 Graphics	6K×8	2	256×192

Field synchronization output ($\overline{FS}$)

The high to low transition of the $\overline{FS}$ output coincides with the end of active display area. The low to high transition of $\overline{FS}$ coincides with the trailing edge of the vertical synchronization pulse. The CPU should not access display memory while $\overline{FS}$ is at low-level to avoid undesired flicker on the screen.

Horizontal synchronization output ($\overline{HS}$)

This signal is used for horizontal synchronization on the CRT. A fall from high-level to low-level indicates the leading edge of the horizontal synchronization signal.

Row preset output ($\overline{RP}$)

This signal can be used when an external character generator ROM that is used with the VDG. An external 4-bit binary counter must also be added to supply row selection.

The counter is clocked by the $\overline{HS}$ signal and cleared by the $\overline{RP}$ signal. See Table 4 ② for details.

Mode Control Inputs ($\overline{A}$/G, $\overline{A}$/S, $\overline{INT}$/EXT, GM_2, GM_1, GM_0, CSS and INV)

These eight TTL-compatible input signals are used to determine and control the operational modes of the M5C6847P-1. Outline and details of the operational modes are shown in Table 1~3.

Alphanumeric mode

A screen in the alphanumeric mode is composed of 32 characters x 16 lines. Each character occupies space equivalent to an 8 x 12 dot matrix. The internal character generator can generate 64 characters (6-bit ASCII). Each character is formed by a 5 x 7 dot matrix. The low-order 6 bits of the 8-bit data input are used to select 1 of 64 characters and the remaining 2 bits can be used to implement the CSS and INV signal inputs. Operation in this mode requires a display memory of a least 512 bytes.

Semigraphic 4 mode

A screen in the semigraphics 4 mode is composed of 64 x 32 display elements. A display element is a 4 x 6 dot matrix; that is to say, each 8 x 12 character dot matrix is split into 4 display elements, each display element being a 4 x 6 dot matrix. The low-order 4 bits of the 8-bit data input correspond to the 4 display elements of a character. Three data bits of the remaining 4 bits may be used to select one of eight colors for the entire character box. The extra bit is available to switch the operation mode. Operation in this mode requires a display memory of at least 512 bytes.

Semigraphics 6 mode

A screen in the semigraphics 6 mode is composed of 64 x 48 display elements. A display element is a 4 x 4 dot matrix; that is to say, each 8 x 12 character dot matrix is split into 6 display elements, each display element being a 4 x 4 dot matrix. The low-order 6 bits of the 8-bit data input to the 6 display elements of a character and the remaining 2 bits are used to determine color. Operation in this mode requires a display memory of at least 512 bytes.

Full Graphic Modes

There are 8 full graphic modes. The border color (green or white) is selected by the level of the CSS signal. The CSS pin selects one of two sets of four colors in the four color graphic modes.

Color Graphic Mode 64 x 64

A screen in the 64 x 64 color graphic mode is composed of 64 x 64 display elements. Each display element can be 1 of 4 colors. Operation in this mode requires a display memory of at least 1024 bytes.

Graphic mode 128 x 64

A screen in the 128 x 64 graphic mode is composed of 128 x 64 display elements. Each display element can be green or white depending on the level of the CSS signal. Operation in this mode requires a display memory of at least 1024 bytes.

Color graphic mode 128 x 64

A screen in the 128 x 64 color graphic mode is composed of 128 x 64 display elements. Each display element can be 1 of 4 colors. Operation in this mode requires a display memory of at least 2048 bytes.

Graphic mode 128 x 96

A screen in the 128 x 96 graphic mode is composed of 128 x 96 picture elements. Each display element can be geeen or white depending on the level of the CSS signal. Operation in this mode requires a display memory of at least 2048 bytes.

Color graphic mode 128 x 96

A screen in the 128 x 96 color graphic mode is composed of 128 x 96 display elements. Each display element can be 1 of 4 colors. Operation in this mode requires a display memory of at least 3072 bytes.

Graphic mode 128 x 192

A screen in the 128 x 192 graphic mode is composed of 128 x 192 display elements. Each display element can be green or white depending on the level of the CSS signal. Operation in this mode requires a display memory of at least 3072 bytes.

Color graphic mode 128 x 192

A screen in the 128 x 192 color graphic mode is composed of 128 x 192 display elements. Each picture element can be 1 of 4 colors. Operation in this mode requires a display memory of at least 6144 bytes.

Graphic mode 256 x 192

A screen in the 256 x 192 graphic mode is composed of 256 x 192 display elements. Each display element can be green or white depending on the level of the CSS signal. Operation in this mode requires a display memory of at least 6144 bytes.

Details of the 8 graphic modes are shown in Table 4 which gives more information in an easy to understand form.

Table 4 Operational characteristics in the various graphic modes

	Input Pin									Color			TV Screen (1 screen is composed of 256×192 dots)		Data Bus	Display Mode
	$\overline{MS}$	$\overline{A}$/G	$\overline{A}$/S	$\overline{INT}$/EXT	GM_2	GM_1	GM_0	CSS	INV	Character Color	Background	Border	Mode	Display Elements		
①	1	0	0	0	X	X	X	0	0	green	black	black	16 lines of 32 characters	5x7 Dots 1 Character	D_7 6 5 4 3 2 1 0 / ASCII Code	Alphanumeric mode
									1	black	green					
								1	0	orange	black	black				
									1	black	orange					
②	1	0	0	1	X	X	X	0	0	green	black	black	16 lines of 32 characters	8x12 Dots 1 Character	External ROM Code	Alphanumeric mode
									1	black	green					
								1	0	orange	black	black				
									1	black	orange					
③	1	0	1	0	X	X	X	X	X	$D_{0\sim3}$ D_6 D_5 D_4 0 X X X black 1 0 0 0 green 1 0 0 1 yellow 1 0 1 0 blue 1 0 1 1 red 1 1 0 0 white 1 1 0 1 cyan 1 1 1 0 magenta 1 1 1 1 orange		black	64×32 display elements	4 Dots; D_3 D_2 } 6 Dots; D_1 D_0 All 4 picture elements of the character group are the same color. The color intensity is 0 (black) or 1 (full color)	Color Luminance	Semigraphics 4 mode
④	1	0	1	1	X	X	X	0	X	$D_{0\sim5}$ D_7 D_6 0 X X black 1 0 0 green 1 0 1 yellow 1 1 0 blue 1 1 1 red		black	64×48 display elements	4 Dots; D_5 D_4 } 4 Dots; D_3 D_2; D_1 D_0 All 6 picture elements of the character group are the same color. The color intensity is 0 (black) or 1 (full color).	Color Luminance	Semigraphics 6 mode
								1		0 X X black 1 0 0 white 1 0 1 cyan 1 1 0 magenta 1 1 1 orange						
⑤	1	1	X	X	0	0	0	0	X	D_7 D_6 (D_5, D_4, D_3, D_2, D_1, D_0) 0 0 green 0 1 yellow 1 0 blue 1 1 red		green	64×64 display elements	2 Dots; E_3 E_2 E_1 E_0 } 3 Dots	Color E_3 E_2 E_1 E_0	Color graphic mode 64x64
								1		0 0 white 0 1 cyan 1 0 magenta 1 1 orange		white				
⑥	1	1	X	X	0	0	1	0	X	D_7 (D_6, D_5, D_4, D_3, D_2, D_1, D_0) 0 black 1 green		green	128×64 display elements	2 Dots; 7 6 5 4 3 2 1 0 } 3 Dots	Luminance	Graphic mode 128x64
								1		0 black 1 white		white				
⑦	1	1	X	X	0	1	0	0	X	The same as ⑤		green	128×64 display elements	2 Dots; E_3 E_2 E_1 E_0 } 3 Dots	Color E_3 E_2 E_1 E_0	Graphic mode 128x64
								1				white				
⑧	1	1	X	X	0	1	1	0	X	The same as ⑥		green	128×96 display elements	2 Dots; 7 6 5 4 3 2 1 0 } 2 Dots	Luminance	Graphic mode 128x96
								1				white				
⑨	1	1	X	X	1	0	0	0	X	The same as ⑤		green	128×96 display elements	2 Dots; E_3 E_2 E_1 E_0 } 2 Dots	Color E_3 E_2 E_1 E_0	Color graphic mode 128x96
								1				white				
⑩	1	1	X	X	1	0	1	0	X	The same as ⑥		green	128×192 display elements	2 Dots; 7 6 5 4 3 2 1 0 } 1 Dot	Luminance	Graphic mode 128x192
								1				white				
⑪	1	1	X	X	1	1	0	0	X	The same as ⑤		green	128×192 display elements	2 Dots; E_3 E_2 E_1 E_0 } 1 Dot	Color E_3 E_2 E_1 E_0	Color graphic mode 128x192
								1				white				
⑫	1	1	X	X	1	1	1	0	X	The same as ⑥		green	256×192 display elements	1 Dot; 7 6 5 4 3 2 1 0 } 1 Dot	Luminance	Graphic mode 256x192
								1				white				

Internal Character Generator

The M5C6847P-1 generates the 64 standard ASCII characters in a 5 x 7 dot matrix form. It generates the 64 standard ASCII characters according to a 6-bit code. The code for each character is showed in Table 5.

Table 5 M5C6847P-1 character set

Code						Character
D_5	D_4	D_3	D_2	D_1	D_0	
0	0	0	0	0	0	@
0	0	0	0	0	1	A
0	0	0	0	1	0	B
0	0	0	0	1	1	C
0	0	0	1	0	0	D
0	0	0	1	0	1	E
0	0	0	1	1	0	F
0	0	0	1	1	1	G
0	0	1	0	0	0	H
0	0	1	0	0	1	I
0	0	1	0	1	0	J
0	0	1	0	1	1	K
0	0	1	1	0	0	L
0	0	1	1	0	1	M
0	0	1	1	1	0	N
0	0	1	1	1	1	O
0	1	0	0	0	0	P
0	1	0	0	0	1	Q
0	1	0	0	1	0	R
0	1	0	0	1	1	S
0	1	0	1	0	0	T
0	1	0	1	0	1	U
0	1	0	1	1	0	V
0	1	0	1	1	1	W
0	1	1	0	0	0	X
0	1	1	0	0	1	Y
0	1	1	0	1	0	Z
0	1	1	0	1	1	[
0	1	1	1	0	0	\
0	1	1	1	0	1	]
0	1	1	1	1	0	↑
0	1	1	1	1	1	←

Code						Character
D_5	D_4	D_3	D_2	D_1	D_0	
1	0	0	0	0	0	SP
1	0	0	0	0	1	!
1	0	0	0	1	0	"
1	0	0	0	1	1	#
1	0	0	1	0	0	$
1	0	0	1	0	1	%
1	0	0	1	1	0	&
1	0	0	1	1	1	'
1	0	1	0	0	0	(
1	0	1	0	0	1	)
1	0	1	0	1	0	*
1	0	1	0	1	1	+
1	0	1	1	0	0	,
1	0	1	1	0	1	−
1	0	1	1	1	0	.
1	0	1	1	1	1	/
1	1	0	0	0	0	0
1	1	0	0	0	1	1
1	1	0	0	1	0	2
1	1	0	0	1	1	3
1	1	0	1	0	0	4
1	1	0	1	0	1	5
1	1	0	1	1	0	6
1	1	0	1	1	1	7
1	1	1	0	0	0	8
1	1	1	0	0	1	9
1	1	1	0	1	0	:
1	1	1	0	1	1	;
1	1	1	1	0	0	<
1	1	1	1	0	1	=
1	1	1	1	1	0	>
1	1	1	1	1	1	?

EXAMPLE OF DISPLAY ON CRT

The M5C6847P-1 can be used to generate characters for display on a video screen. An example of a display is shown in Fig. 1.

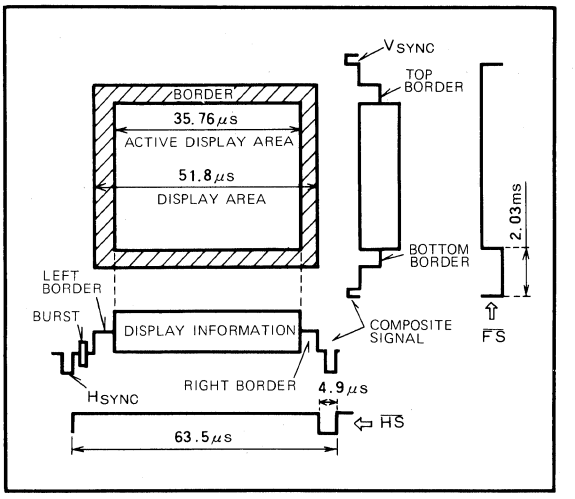


Fig. 1 Example of a display by a M5C6847P-1

APPLICATION EXAMPLE

One example of interfacing a M5C6847P-1 with a television set for home use is shown in Fig. 2. A M5L8085AP is used as the CPU in the example shown. The CPU executes the programs to control display and write the information for one screen into display memory. The M5C6847P-1 performs the main functions of interfacing with the CRT such as synchronizing scan, reading the display information from the display memory while adding necessary synchronization signals and sending to the RF modulator.

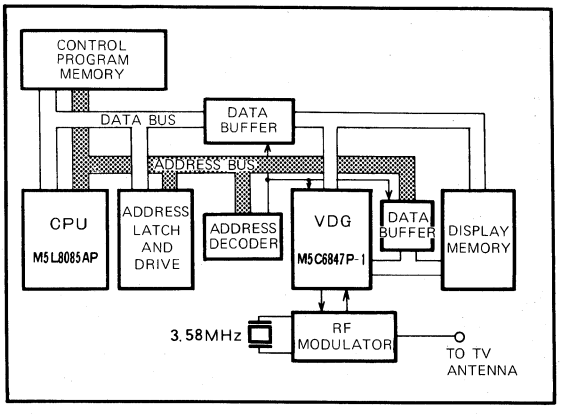


Fig. 2 Application example using the M5C6847P-1

A schematic for using the M5C6847P-1 with the M51342P RF modulator is shown in Fig. 3. M51342 requires ±5V power supplies. The video signal and chroma signal from the M5C6847P-1 can be modulated with the sound signal to form a RF signal that appears the same as the television antenna input signal. The video amp circuit to enable direct connection to a M5C6847P-1 is shown in Fig. 4. This can be connected to the monochrome video monitor. In this case, the inpedance is 75Ω.

Four levels of brightness (black, low, medium and high) can display a clear picture.

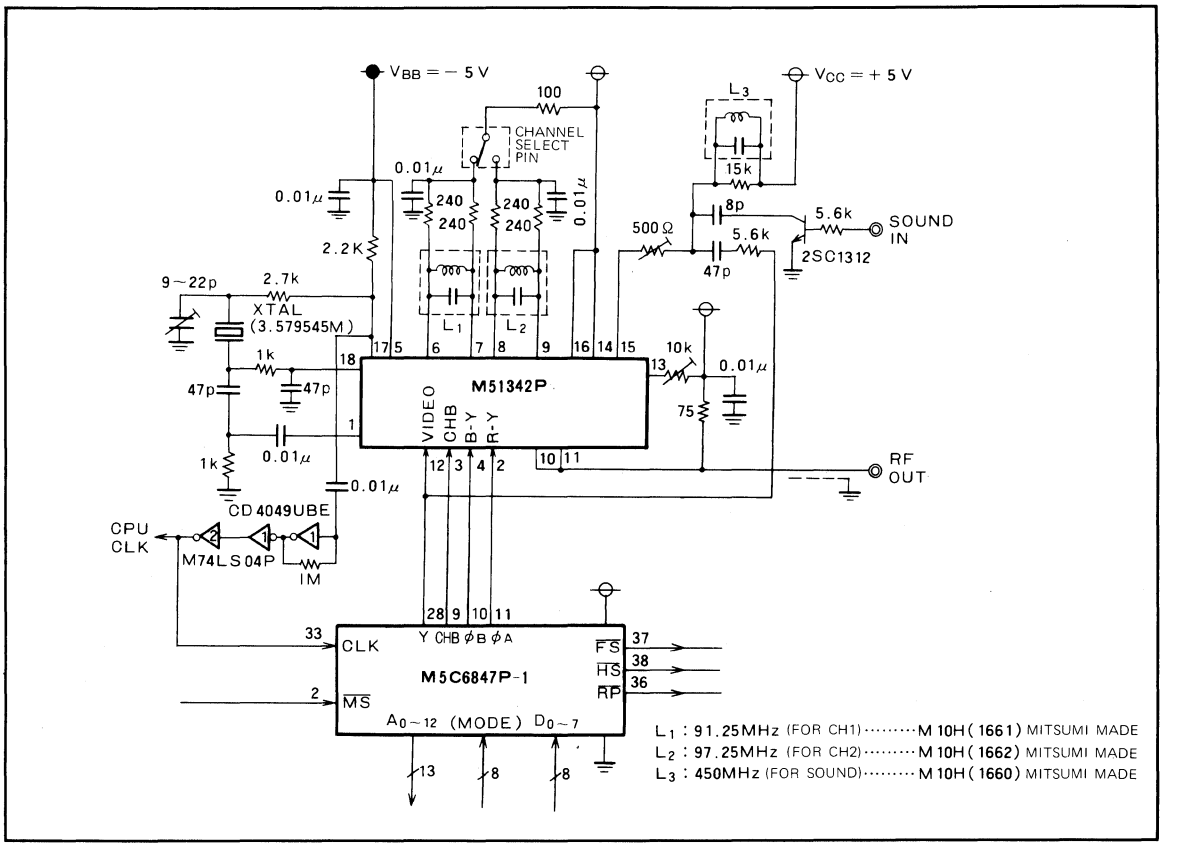


Fig. 3 Schematic for using the M51342P (RF modulator) with the M5C6847P-1

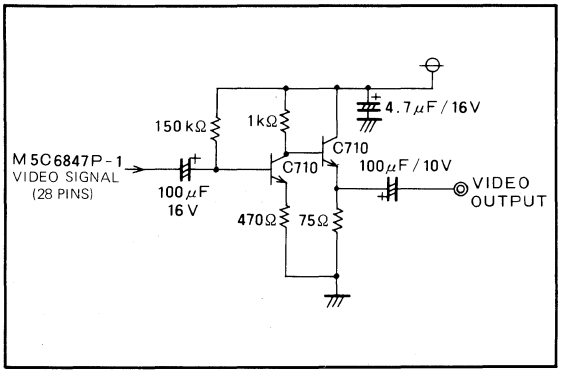
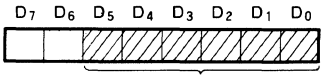
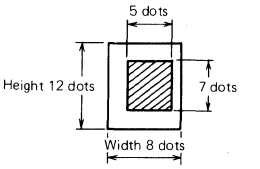
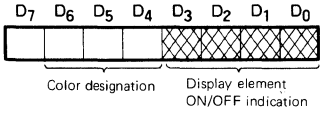
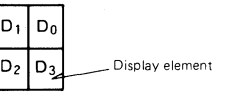
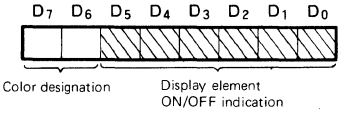
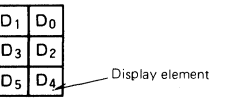
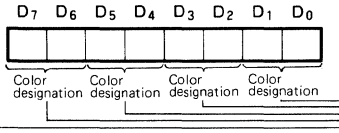
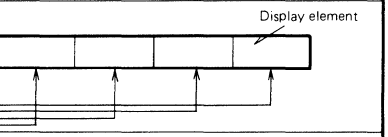
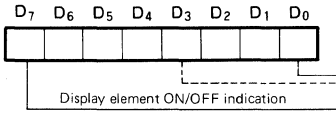
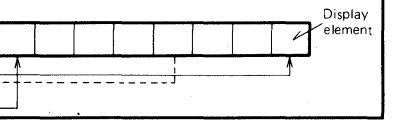


Fig. 4 Video amp circuit

Data and Display Relation

The relation between data and 5 display modes is shown in Table 6.

Table 6 Data and display relation

Mode	Data	Display
Character		
Semigraphic 4		
Semigraphic 6		
Color-graphic (4 colors)		
Graphic (2 colors)		

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.3～7	V
V_I	Input voltage	With respect to V_{SS}	−0.3～7	V
V_O	Output voltage		−0.3～7	V
Pd	Power dissipation	Ta＝25°C	1000	mW
Topr	Operating free-air temperature range		0～70	°C
Tstg	Storage temperature range		−65～150	°C

RECOMMENDED OPERATING CONDITIONS (Ta＝0～70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{SS}	Supply voltage		0		V
$V_{IH(\phi)}$	High-level input voltage, clock	2.4		V_{CC}	V
V_{IH}	High-level input voltage	2		V_{CC}	V
$V_{IL(\phi)}$	Low-level input voltage, clock	−0.3		0.4	V
V_{IL}	Low-level input voltage	−0.3		0.8	V

ELECTRICAL CHARACTERISTICS (Ta＝0～70°C, V_{CC}＝5V±5%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OH}	High-level output voltage, except for ϕ_A, ϕ_B, Y, and CHB output	V_{SS}＝0V, I_{OH}＝−100μA, C_L＝30pF	2.4			V
V_{OL}	Low-level output voltage, except for ϕ_A, ϕ_B, Y and CHB output	V_{SS}＝0V, I_{OL}＝1.6mA, C_L＝30pF			0.4	V
I_{IH}	High-level input current	V_{SS}＝0V, V_I＝5.25V	−10		10	μA
I_{IL}	Low-level output current	V_{SS}＝0V, V_I＝0V	−10		10	μA
I_{OZ}	Output floating leak current	V_{SS}＝0V, V_I＝0.4V, MS＝0.4V	−10		10	μA
I_{CC}	Supply current from V_{CC}	V_{SS}＝0V			150	mA
Ci	Input capacitance	V_I＝0V, f＝1MHz, Ta＝25°C			10	pF
C_O	Output capacitance				20	pF
V_{CHB}	Chroma bias voltage	V_{SS}＝0V, C_L＝20pF, R_L＝200kΩ		0.6V_{CC}		V
$V_{\phi A,H}$	ϕ_A chrominance high-level output voltage			V_{CHB}+0.16V_{CC}		V
$V_{\phi A,M}$	ϕ_A chrominance medium-level output voltage			V_{CHB}		V
$V_{\phi A,L}$	ϕ_A chrominance low-level output voltage			V_{CHB}−0.16V_{CC}		V
$V_{\phi B,H}$	ϕ_B chrominance high-level output voltage			V_{CHB}+0.16V_{CC}		V
$V_{\phi B,M}$	ϕ_B chrominance medium-level output voltage			V_{CHB}		V
$V_{\phi B,B}$	ϕ_B chrominance burst-level output voltage			V_{CHB}−0.08V_{CC}		V
$V_{\phi B,L}$	ϕ_B chrominance low-level output voltage			V_{CHB}−0.16V_{CC}		V
V_{YSYNC}	Luminance sync output voltage			0.74V_{CC}		V
V_{YBLANK}	Luminance blank output voltage			0.85 V_{YSYNC}		V
V_{YBLACK}	Luminance black output voltage			0.81 V_{YSYNC}		V
$V_{YW(H)}$	White luminance high-level output voltage			0.62 V_{YSYNC}		V
$V_{YW(M)}$	White luminance medium-level output voltage			0.69 V_{YSYNC}		V
$V_{YW(L)}$	White luminance low-level output voltage			0.77 V_{YSYNC}		V

TIMING REQUIREMENTS (Ta=0~70°C, V_{CC}=5V±5%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$f_{C(\phi)}$	Clock frequency		3.579535	3.579545	3.579555	MHz
f_{DUTY}	Clock duty ratio		45	50	55	%
$t_{r(\phi)}$	Clock rise time				10	ns
$t_{f(\phi)}$	Clock fall time				10	ns
$t_{a(A-D)I}$	Address access time of display memory	Internal character mode			900	ns
$t_{a(A-D)E}$	Address access time of display memory + Address access time of external character ROM	External character mode			900	ns

SWITCHING CHARACTERISTICS

Composite video and chroma (Ta=0~70°C, V_{CC}=5V±5%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(YSYNC)}$	Luminance output synchronization signal pulse width			4.89		μs
$t_{W(YFP)}$	Luminance output front pot signal pulse width			1.96		μs
$t_{W(YHBLANK)}$	Luminance output horizontal blank signal pulse width			11.73		μs
$t_{r(YHSYNC)}$	Luminance output horizontal synchronization signal rise time				250	ns
$t_{f(YHSYNC)}$	Luminance output horizontal synchronization signal fall time				250	ns
$t_{r(YHBLANK)}$	Luminance output horizontal blank signal rise time				340	ns
$t_{f(YHBLANK)}$	Luminance output horizontal blank signal fall time				340	ns

CHROMA

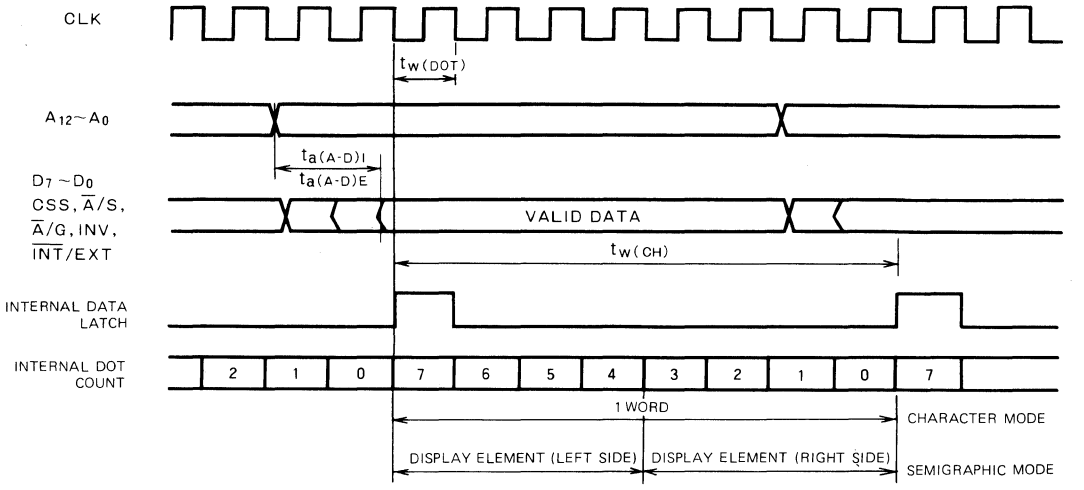
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{r(\phi A)}$	ϕ_A chrominance output rise time			60		ns
$t_{f(\phi A)}$	ϕ_A chrominance output fall time			60		ns
$t_{r(\phi B)}$	ϕ_B chrominance output rise time			60		ns
$t_{f(\phi B)}$	ϕ_B chrominance output fall time			60		ns
$t_{PHL(SYNC-BURST)}$	ϕ_B chrominance output propagation time after luminance syncronization signal output			980		ns
$t_{W(BURST)}$	ϕ_B chrominance output burst signal pulse width			2.93		μs
$t_{r(BURST)}$	ϕ_B chrominance output burst signal rise time			60		ns
$t_{f(BURST)}$	ϕ_B chrominance output burst signal fall time			60		ns
$t_{PHL(Y-CH)}$	Chrominance propagation time after luminance output			0		ns
$t_{PLH(Y-CH)}$						

MISCELLANEOUS

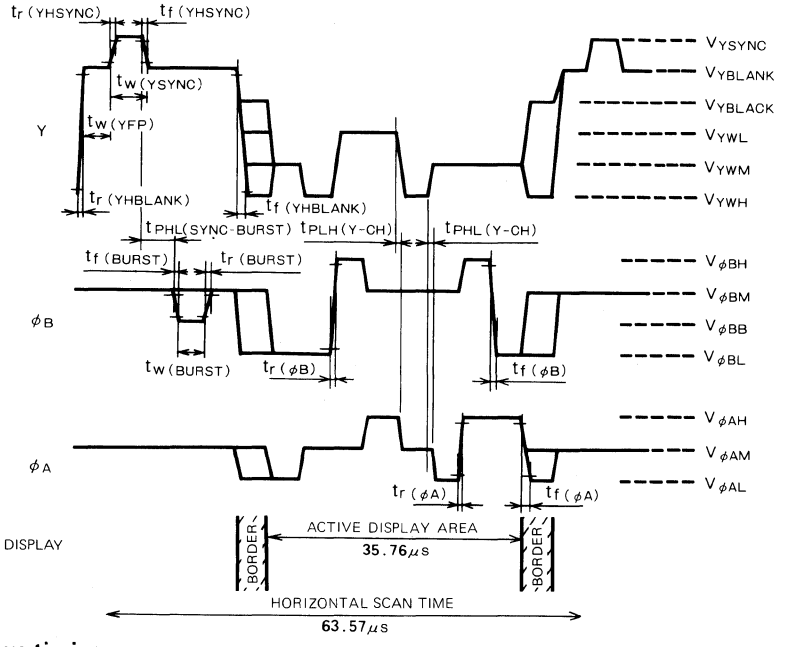
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(FS)}$	Field syncronization pulse width			2.03		ms
$t_{W(RP)}$	Row preset pulse width			980		ns
$t_{PHL(HS-RP)}$	$\overline{RP}$ propagation time after $\overline{HS}$			980		ns
$t_{W(HS)}$	Horizontal syncronization pulse width			4.9		μs
$t_{W(CH)}$	Character width			1.12		μs
$t_{W(DOT)}$	Dot width			140		ns

TIMING DIAGRAM

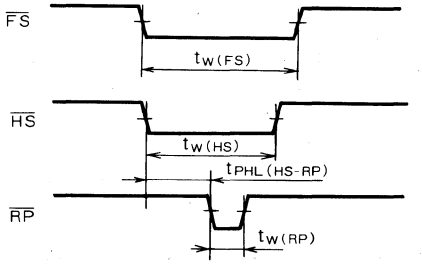
Display memory access



Composite video and chroma



Miscellaneous timing



M5G 1400P

1400-BIT (100-WORD BY 14-BIT) ELECTRICALLY ALTERABLE ROM

DESCRIPTION

The M5G1400P is a serial input/output 1400-bit electrically erasable and reprogrammable ROM organized as 100 words of 14 bits, and fabricated using MNOS technology. Data and addresses are transferred serially via a one-bit bidirectional bus.

FEATURES

- Word-by-word electrically alterable
- Non-volatile data storage: ..... 10 years (min)
- Write/erase time: 20ms/word
- Single 35V power supply
- Number of erase-write cycles: ..... 10^5 times (min)
- Number of read access unrefreshed:.... 10^6 times (min)
- Interchangeable with GI's ER1400 in pin configuration and electrical characteristics

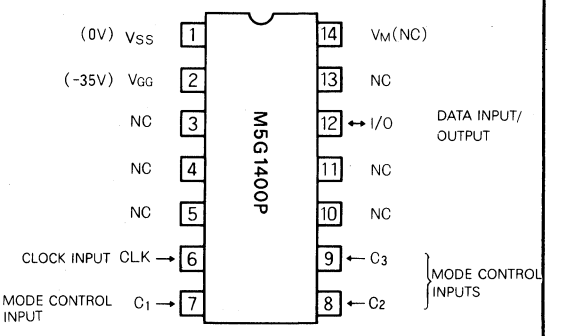
APPLICATION

- Non-volatile channel memories for electronic tuning systems and field-reprogrammable read-only memory systems

FUNCTION

The address is designated by two consecutive one-of-ten-coded digits. Seven modes—accept address, accept data, shift data output, erase, write, read, and standby—are all selected by a 3-bit code applied to C_1, C_2, and C_3. Data is stored by internal negative writing pulses that selectively tunnel charges into the SiO_2—Si_3N_4 interface of the gate insulators of the MNOS memory transistors.

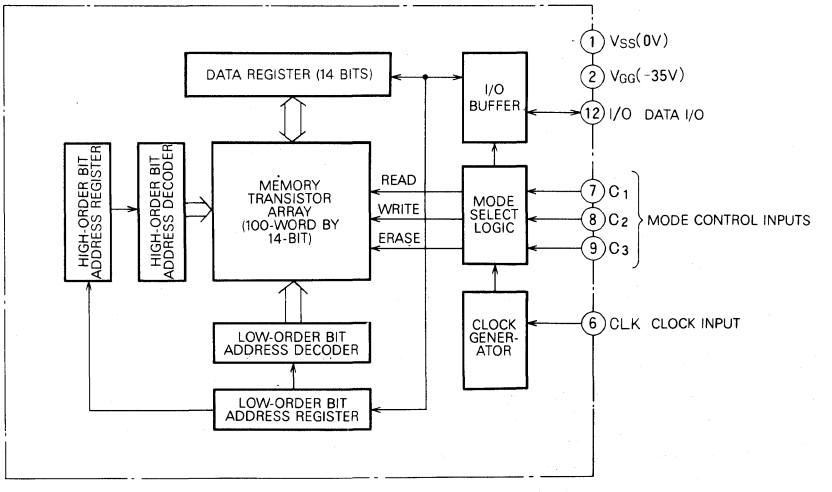
PIN CONFIGURATION (TOP VIEW)



Outline 14P4

NC: NO CONNECTION

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

1400-BIT (100-WORD BY 14-BIT) ELECTRICALLY ALTERABLE ROM

PIN DESCRIPTION

Pin	Name	Functions
I/O	I/O	In the accept address and accept data modes, used for input. In the shift data output mode, used for output. In the standby, read, erase and write modes, this pin is in a floating state.
V_M	Test	Used for testing purposes only. It should be left unconnected during normal operation.
V_{SS}	Chip substrate voltage	Normally connected to ground.
V_{GG}	Power supply voltage	Normally connected to −35V.
CLK	Clock input	14kHz timing reference. Required for all operating modes. High-level input is possible during standby mode.
$C_1 \sim C_3$	Mode control input	Used to select the operation mode.

OPERATION MODES

C_1	C_2	C_3	Functions
H	H	H	Standby mode: The contents of the address registers and the data register remain unchanged. The output buffer is held in the floating state.
H	H	L	Not used.
H	L	H	Erase mode: The word stored at the addressed location is erased. The data bits after erasing are all low-level.
H	L	L	Accept address mode: Data presented at the I/O pin is shifted into the address registers one bit with each clock pulse. The address is designated by two one-of-ten-coded digits.
L	H	H	Read mode: The addressed word is read from the memory into the data register.
L	H	L	Shift data output mode: The output driver is enabled and the contents of the data register are shifted to the I/O pin one bit with each clock pulse.
L	L	H	Write mode: The data contained in the data register is written into the location designated by the address registers.
L	L	L	Accept data mode: The data register accepts serial data from the I/O pin one bit with each clock pulse. The address registers remain unchanged.

1400-BIT (100-WORD BY 14-BIT) ELECTRICALLY ALTERABLE ROM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{GG}	Supply voltage	With respect to V_{SS}	0.3～−40	V
V_I	Input voltage		0.3～−20	V
V_O	Output voltage		0.3～−20	V
T_{stg}	Storage temperature range		−65～150	℃
T_{opr}	Operating free-air temperature range		−10～70	℃

RECOMMENDED OPERATING CONDITIONS (Ta = −10～70℃, unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{GG}	Supply voltage	−32.2	−35	−37.8	V
V_{SS}	Supply voltage (GND)		0		V
V_{IH}	High-level input voltage	$V_{SS}-1$		$V_{SS}+0.3$	V
V_{IL}	Low-level input voltage	$V_{SS}-15$		$V_{SS}-8$	V

Note 1:
The order of V_{SS} V_{GG} with on or off.
With on, V_{GG} is turned on after V_{SS} is done.
With off, V_{SS} is turned off after V_{GG} is done.

ELECTRICAL CHARACTERISTICS (Ta = −10～70℃, V_{GG} = −35V ± 8%, unless otherwise noted.)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		$V_{SS}-1$		$V_{SS}+0.3$	V
V_{IL}	Low-level input voltage		$V_{SS}-15$		$V_{SS}-8$	V
I_{IL}	Low-level input current	V_I = −15V			±10	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_O = −15V			±10	μA
V_{OH}	High-level output voltage	I_{OH} = −200μA	$V_{SS}-1$			V
V_{OL}	Low-level output voltage	I_{OL} = 10μA			$V_{SS}-12$	V
I_{GG}	Supply current from V_{GG}	I_O = 0μA		5.5	8.8	mA

Note 2: Typical values are at Ta=25°C and nominal supply voltage.

TIMING REQUIREMENTS (Ta = −10～70℃, V_{GG} = −35V ± 8%, unless otherwise noted.)

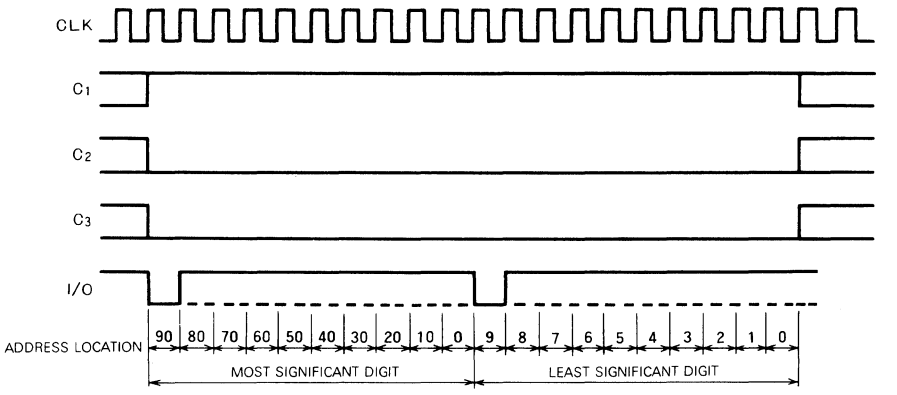
Symbol	Parameter	Alternative symbols	Test conditions	Limits			Unit
				Min	Typ	Max	
f(φ)	Clock frequency	fφ		11.2	14	16.8	kHz
D(φ)	Clock duty cycle	Dφ		30	50	55	%
tw(W)	Write time	tw		16	20	24	ms
tw(E)	Erase time	te		16	20	24	ms
tr, tf	Risetime, falltime	tr, tf				1	μs
tsu(c−φ)	Control setup time before the fall of the clock pulse	t_{CS}		0			ns
th(φ−c)	Control hold time after the rise of the clock pulse	t_{CH}		0			ns

SWITCHING CHARACTERISTICS (Ta = −10～70℃, V_{GG} = −35V ± 8%, unless otherwise noted.)

Symbol	Parameter	Alternative symbols	Test conditions	Limits			Unit
				Min	Typ	Max	
ta(c)	Read access time	t_{PW}	C_L = 50pF, $V_{OH}=V_{SS}-2V$, $V_{OL}=V_{SS}-8V$			20	μs
ts	Unpowered nonvolatile data retention time	T_S	$N_{EW}=10^4$, tw(W) = 20ms, tw(E) = 20ms	10			Year
		T_S	$N_{EW}=10^5$, tw(W) = 20ms, tw(E) = 20ms	1			Year
N_{EW}	Number of erase/write cycles	N_W		10^5			Times
N_{RA}	Number of read access unrefreshed	N_{RA}		10^6	10^9		Times
tdv	Data valid time	t_{PW}				20	μs

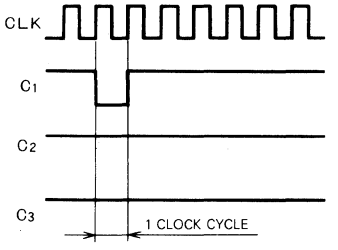
TIMING DIAGRAM

Accept Data Mode

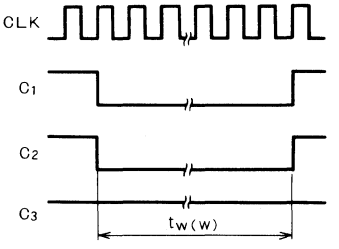


Note 3: The address is designated by two one-of-ten-coded digits. The figure shows designation of the address 99.

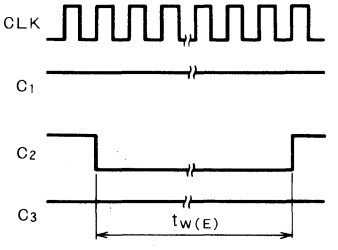
Read Mode



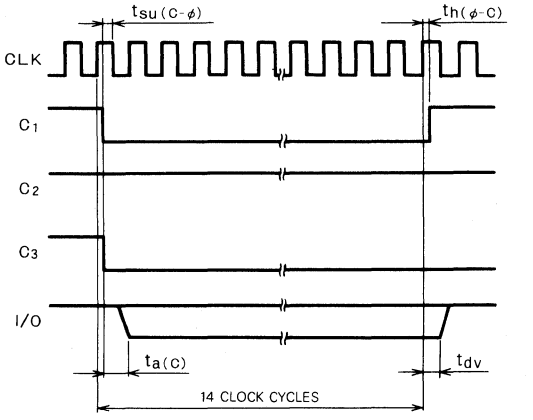
Write Mode



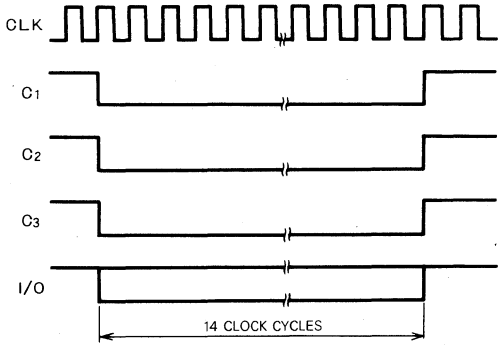
Erase Mode



Shift Data Output Mode



Accept Data Mode



M5L 8279P-5

PROGRAMMABLE KEYBOARD/DISPLAY INTERFACE

DESCRIPTION

The M5L8279P-5 is a programmable keyboard and display interface device that is designed to be used in combination with an 8-bit microprocessor such as the Mitsubishi MELPS 8 CPUs. This device is fabricated with N-channel silicon-gate technology and is packed in a 40-pin DIL package. It needs only single 5V power supply.

FEATURES

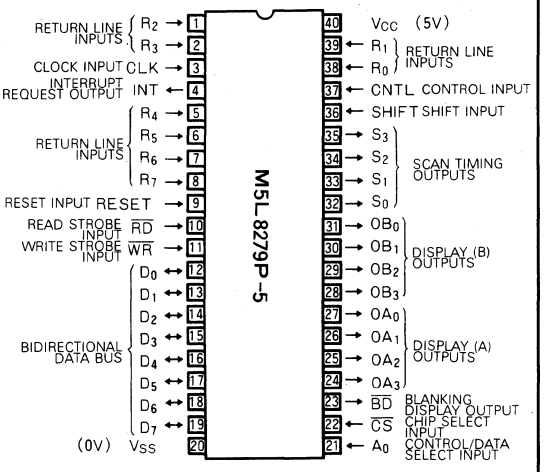
Parameter	M5L 8279P-5
Output enable time after read (max)	200ns
Output enable time after address (max)	250ns
Clock cycle time (min)	320ns

- Single 5V power supply
- Keyboard mode
- Sensor mode
- Strobed entry mode
- Internally provided key bounce protection circuit
- Programmable debounce time
- 2-key/N-key rollover
- 8-character keyboard FIFO
- Internally contained 16 × 8-bit display RAM
- Programmable right and left entry
- Interchangeable with Intel's 8279/8279-5 in pin configuration and electrical characteristics

APPLICATIONS

- Microcomputer I/O device
- 64 contact key input device for such items as electronic cash registers
- Dual 8- or single 16-alphanumeric display

PIN CONFIGURATION (TOP VIEW)



Outline 40P1

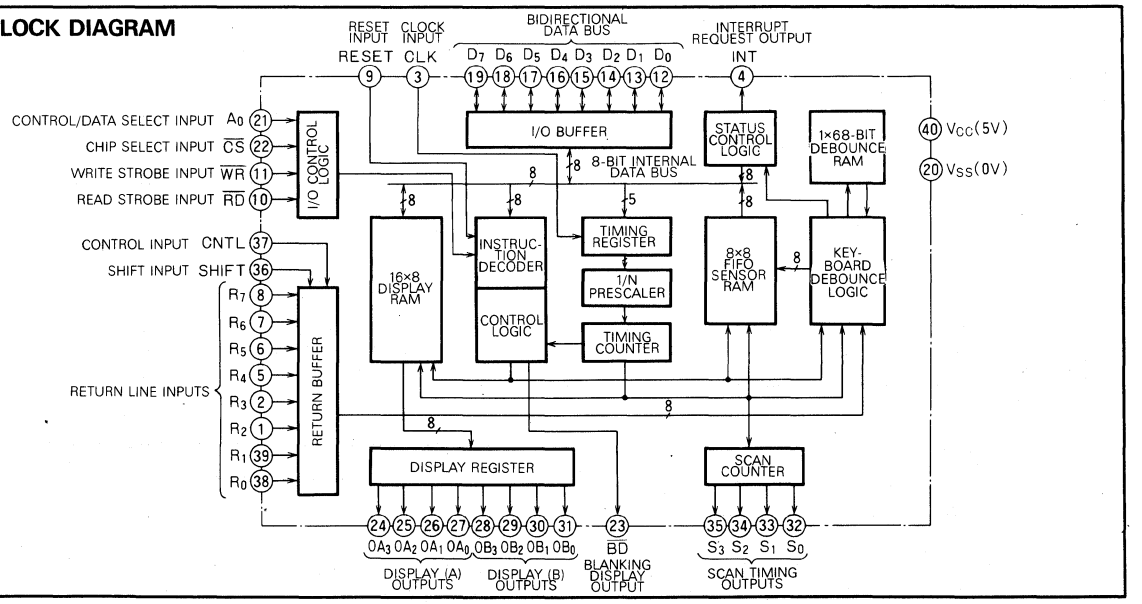
FUNCTION

The total chip, consisting of a keyboard interface and a display interface, can be programmed by eight 8-bit commands.

The keyboard portion is provided with a 64-bit key debounce buffer and an 8 × 8-bit FIFO. It operates in any one of the scanned keyboard mode, scanned sensor mode or strobed entry mode.

The display portion is provided with a 16 × 8-bit display RAM that can be organized into a dual 16 × 4 configuration. Also, an 8-digit display configuration is possible by means of programming.

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

PIN DISCRIPTON

Pin	Name	Input or output	Functions
D_0~D_7	Bidirectional data bus	In/out	All data and commands between the CPU and the chip are transferred through these lines.
CLK	Clock input	In	Clock signal from the system which is used to generate internal timing.
RESET	Reset input	In	Resets the chip when this signal is high. After the reset it assumes 8-digit, left-entry, encode display, and 2-key rollover mode, and the prescale value of the clock becomes 31. The display RAM, however, is not cleared.
$\overline{CS}$	Chip select input	In	Chip select is enabled when this signal is low.
A_0	Control/data select input	In	When this signal is high, it indicates that the signals in and out are either command (in) or status (out). When low, it indicates they are data (in/out).
$\overline{RD}$	Read strobe input	In	Functions to control data transfer to the data bus.
$\overline{WR}$	Write strobe input	In	Functions to control command/data transfer from the data bus.
INT	Interrupt request output	Out	When there is any data in the FIFO during the keyboard mode or the strobed mode, this signal turns high-level so as to request interrupt to the CPU. It turns low each time data is read, but if any data remains in the FIFO it will turn high again and request interrupt to the CPU.
S_0~S_3	Scan timing outputs	Out	These signals are used to scan the key switch, the sensor matrix, or the display digit. They can be either decoded or encoded, but it requres an external decoder in the encode mode. Signals S_0~S_3 are all turned to low-level when RESET is high.
R_0~R_7	Return line inputs	In	These are the return lines which are connected with the scan lines through the keys or sensor switches, and are used for 8-bit input in the strobed entry mode. They are provided with internal pullups to maintain them high until a switch closure pulls one low. They become active at low-level.
SHIFT	Shift input	In	In the keyboard mode, the shift input becomes the second highest bit of the key input information and is stored in the FIFO. This input is ignored in the other modes. It is constantly kept at high-level by an internal pull resistor.
CNTL	Control input	In	In the keyboard mode, the control input becomes the most significant bit of the key input information and is stored in the FIFO. The signal is active at high-level. In the strobed entry mode, it becomes the strobe signal and stores the return input data in the FIFO at the rising edge of the input. It affects nothing internal in the sensor mode. It is constantly kept at high-level by an internal pullup resistor.
OA_0~OA_3 OB_0~OB_3	Display (A) and (B) outputs	Out	These output ports can be used either as a dual 4-bit port or a single 8-bit port depending on an application, and the contents of the display RAM are output synchronizing with the scan timing signals. These two 4-bit ports may be blanked independently. Blanking may be activated with either high- or low-level signal by means of clear command.
$\overline{BD}$	Blanking display output	Out	This signal is used in preventing overlapped display during digit switching. It also may be brought to low-level by display blanking command.

OPERATION

Of the three operating modes, the keyboard mode is the most common, and allows programmed 2-key lockout and N-key rollover. Encoded timing signals corresponding with key input are stored in the FIFO through the key-debounce logic, and the debouncing time of the key is also programmable. In the sensor mode, the contents of the 8 × 8 key contacts are constantly stored in the FIFO/sensor RAM, generating an interrupt signal to the CPU each time there is a change in the contents. In the strobed entry mode, the CNTL input signal is used as a strobe for storing the 8 return line inputs to the FIFO/sensor RAM.

The display portion is provided with a 16 × 8-bit display RAM that can be organized into a dual 16 × 4-bit configuration. Also, an 8-digit display configuration is possible by means of programming. Input to the register can be performed by either left or right entry modes. In the auto increment mode, read and write can be carried out after designating the starting address only.

Both the keyboard and display sections are scanned by common scan timing signals that are derived from the basic clock pulse. This frequency-dividing ratio is changeable by means of programming. There are decode and encode modes for the scanning mode; timing signals that are decoded from the lower 2 bits of the scan counter are output in the decode mode, while the 4-bit binary output from the scan counter is decoded externally in the encode mode.

COMMAND DESCRIPTION

There are eight commands provided for programming the operating modes of the M5L8279P. These commands are sent on the data bus with the signal $\overline{CS}$ in low-level and the signal A_0 in high-level and are stored in the M5L 8279P at the rising edge of the signal $\overline{WR}$.

1. Mode Set Command

	MSB							LSB
Code :	0	0	0	D	D	K	K	K

DD (Display mode set command)

0 0 8—8-bit character display—left entry
0 1 16—8-bit character display—left entry[1]
1 0 8—8-bit character display—right entry
1 1 16—8-bit character display—right entry

KKK (Keyboard mode set command)

0 0 0 Encoded display keyboard mode — 2-key lockout[1]
0 0 1 Decoded display keyboard mode — 2-key lockout
0 1 0 Encoded display keyboard mode — N-key rollover
0 1 1 Decoded display keyboard mode — N-key rollover
1 0 0 Encoded display, sensor mode
1 0 1 Decoded display, sensor mode
1 1 0 Encoded display, strobed entry mode
1 1 1 Decoded display, strobed entry mode

Note 1 : Default after reset.

2. Program Clock Command

	MSB							LSB
Code :	0	0	1	P	P	P	P	P

The external clock is divided by the prescaler value PPPPP designated by this command to obtain the basic internal frequency.

When the internal clock is set to 100kHz, it will give a 5.1ms keyboard scan time and a 10.3ms debounce time. The prescale value that can be specified by PPPPP is from 2 to 31. In case PPPPP is 00000 or 00001, the prescale is set to 2. Default after a reset pulse is 31, but the prescale value is not cleared by the clear command.

3. Read FIFO Command

	MSB							LSB	
Code :	0	1	0	AI	X	A	A	A	X=Don't care

This command is used to specify that the following data readout ($CS \cdot \overline{A_0} \cdot RD$) is from the FIFO. As long as data is to be read from the FIFO, no additional commands are necessary.

AI and AAA are used only in the sensor mode. AAA designates the address of the FIFO to be read, and AI is the auto-increment flag. Turning AI to "1" makes the address automatically incremented after the second read operation. This auto-increment bit does not affect the auto-increment of the display RAM.

4. Read Display RAM Command

	MSB							LSB
Code :	0	1	1	AI	A	A	A	A

This command is used to specify that the following data readout ($CS \cdot \overline{A_0} \cdot RD$) is from the display RAM. As long as data is to be read from the display RAM, no additional commands are necessary.

The data AAAA is the value with which the display RAM read/write counter is set, and it specifies the address of the display RAM to be read or written next.

AI is the auto-increment flag. Turning AI to "1" makes the address automatically incremented after the second read/write operation. This auto-increment bit does not affect the auto-increment of FIFO readout in the sensor mode.

5. Write Display RAM Command

	MSB							LSB
Code :	1	0	0	AI	A	A	A	A

With this command, following display RAM read/write addressing is achieved without changing the data readout source (FIFO or display RAM). Meaning of AI and AAAA are identical with read display RAM command.

6. Display Write Inhibit/Blanking Command

	MSB							LSB	
Code :	1	0	1	X	IW	IW	BL	BL	X=Don't care
					A	B	A	B	

The IW is a write inhibit bit to the display RAM that corresponds with the output A or B. Inhibit is activated by turning the IW "1".

The BL is used in blanking the out A or B. Blanking is activated by turning the BL "1". Setting both BL flags makes the signal $\overline{BD}$ low so that it can be used in 8-bit display mode.

Resetting the flags makes all IW and BL turn "0".

7. Clear command

	MBS							LSB
Code :	1	1	0	C_D	C_D	C_D	C_F	C_A

C_D: Clears the display RAM.

C_D	C_D	C_D	
0	X	X	No specific performance
1	0	X	Entire contents of the display RAM are turned "0".
1	1	0	The contents of the display RAM are turned 20H (00100000 = $0A_3 0A_2 0A_1 0A_0$ $0B_3 0B_2 0B_1 0B_0$).
1	1	1	Entire contents of the display RAM are turned "1".

C_F : Clears the status word and resets the interrupt signal (INT).

C_A : Clears the display RAM and the status word and resets the interrupt signal (INT).

Clearing condition of the display RAM is determined by the lower 2 bits of the C_D.

Clearing the display RAM needs a whole display scan cycle and causes the display-unavailable status (DU) in the status word to be "1". The display RAM is not accessible for the duration of a scan cycle (scan time for 16 digits), even if the display mode was in 8-digit display mode or a decoded mode.

As both C_F and C_A function to reset the internal key-debounce counter, the key input under counting is ignored, and the internal FIFO counter is reset to make the interrupt signal low-level.

C_A resets the internal timing counter, forcing $S_0 \sim S_3$ to start from $S_3S_2S_1S_0$ = 0000 after the execution of the command.

8. End Interrupt/Error Mode Set Command

MSB LSB

Code:	1	1	1	E	X	X	X	X

X=Don't care

In the sensor matrix mode, an interrupt signal is generated at the beginning of the next key scan time to inhibit further writing to the FIFO when there is a change in the sensor switch, but execution of this command makes the interrupt signal released so as to allow writing to the FIFO.

When E is kept in "0", depression of any sensor makes the second highest bit of the status word "1". When E is kept in "1", the status is kept "0" all the time.

When E is programmed to "1" in the N-key rollover mode, the execution of this command makes the chip operate in special error mode, during which time depression of more than two keys in a key scan time causes an error and sets the second highest bit of the status word "1".

Status word

MSB LSB

DU	S/E	0	U	F	N	N	N

NNN: Indicates the number of characters in the FIFO during the keyboard and strobed entry modes.

F: Indicates that the FIFO is filled up with 8 characters.
The number of characters existing in the FIFO (0~8 characters) can be known by means of the bits NNN and F (FNNN = 0000~FNNN = 1000).

U: Underrun error flag
This flag is set when a master CPU tries to read an empty FIFO.

O: Overrun error flag
This flag is set when another character is strobed into a full FIFO.
The bits U and O cannot be cleared by status read. They will be cleared by the clear command.

S/E: Sensor closure/multiple error flag
When "111EXXXX" is executed by turning E = 0, the bit S/E in the status word is set when there is at least one sensor closure.
When "111EXXXX" is executed by turning E = 1 (special error mode), the bit S/E is set when there are more than two key depressions made in a key scan time.

DU: Display unavailable
This flag is set during a whole display scan cycle when a clear display command is executed, and announces that the display RAM is not accessible.

Note: It is necessary to execute the clear command (C_F=1) to reset the underrun, overrun, and special error flags.

CPU INTERFACE

1. Command Write

A command is written on the rising edge of the signal $\overline{WR}$ with $\overline{CS}$ low and A_0 high.

2. Data Write

Data is written to the display RAM on the rising edge of the signal $\overline{WR}$ with $\overline{CS}$ and A_0 low.

The address of the display RAM is also incremented on the rising edge of the signal WR if AI is set for the display RAM.

3. Status Read

The status word is read when $\overline{CS}$ and $\overline{RD}$ are low and A_0 is high. The status word appears on the data bus as long as the signal $\overline{RD}$ is low.

4. Data Read

Data is read from either the FIFO or the display RAM with $\overline{CS} = \overline{RD} = 0$ and $A_0 = 1$. The source of the data (FIFO or display RAM) is decided by the latest command (read display or read FIFO). The data read appears on the data bus as long as the signal $\overline{RD}$ is low.

The trailing edge of the signal $\overline{RD}$ increments the address of the FIFO or the display RAM when AI is set. After the reset, data will be read from the FIFO, however.

$\overline{CS}$	A_0	$\overline{RD}$	$\overline{WR}$	Operation
0	1	1	0	Command write
0	0	1	0	Data write
0	1	0	1	Status read
0	0	0	1	Data read
1	X	X	X	No operation

KEYBOARD INTERFACE

Keyboard interface is done by the scan timing signals (S_0~S_3), the return line inputs (R_0~R_7), the SHIFT and the CNTRL inputs.

In the decoded mode, the low order of two bits of the internal scan counter are decoded and come out on the timing pins (S_0~S_3). In the encoded mode, the four binary bits of the scan counter are directly output on the timing pins, thus a 3-to-8 decoder must be employed to generate keyboard scan timing.

The return line inputs (R_0~R_7), the SHIFT and the CNTL inputs are pulled up high by internal pullup transistors until a switch closure pulls one low.

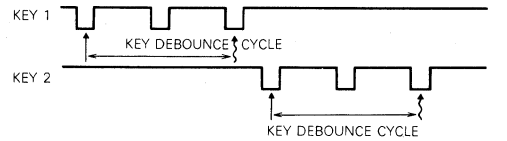
The internal key debounce logic works for a 64-key matrix that is obtained by combining the return line inputs with the scan timing.

For the keyboard interface, M5L8279P-5 has four distinctive modes that allow various kinds of applications. In the following explanation, a "key scan cycle" is the time needed to scan a 64-key matrix, and a "key debounce cycle" needs a duration of two "key scan" cycles. (In the decoded mode 32 keys, unlike 64 keys in the encoded mode, can be employed for a maximum key matrix due to the limit of timing signals. However, both the key scan cycle and the key debounce cycle are the same as in the encoded mode.)

1. 2-Key Lockout (Scanned Keyboard mode)

The detection of a new key closure resets the internal debounce counter and starts counting. At the end of a key debounce cycle, the key is checked and entered into the FIFO if it is still down. An entry in the FIFO sets the IRQ output high. If any other keys are depressed in a key debounce cycle, the internal key debounce counter is reset each time it encounters a new key. Thus only a single-key depression within a key debounce duration is accepted, but all keys are ignored when more than two keys are depressed at the same time.

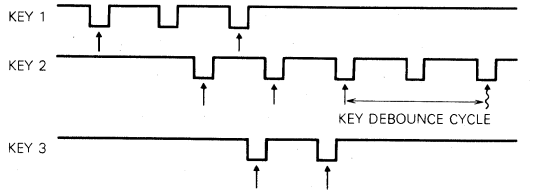
Example 1: Accepting two successive key depressions



Note 2 : ↑ : Debounce counter reset

↕ : Key input

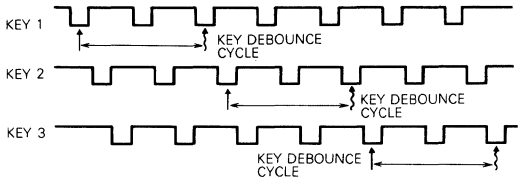
Example 2: Overlapped depression of three keys



Note 3 : Only key 2 is acceptable.

2. N-Key Rollover (Scanned Keyboard Mode)

Each key depression is treated independently from all others so as to allow overlapped key depression. Detection of a new key depression makes the internal key debounce counter reset and start to count in a same manner as in the case of 2-key rollover. But, in N-key rollover, other key closures are entirely ignored within a key debounce cycle so that depression of any other keys would not reset the key debounce counter. In this way, overlapped key depression is allowed so as to enable the following key input:

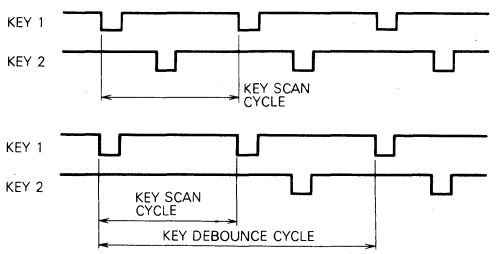


The scanned key input signal does not always reflect the actual key depressing action, as the key matrix is scanned by the timing signal.

With N-key rollover, there is a mode provided with which error is caused when there are more than two key inputs in a key scan cycle, which can be programmed by using the end interrupt/error mode set command. In this mode (special error mode), recognition of the above error sets the IRQ signal to "1" and sets the bit S/E in the status word.

In case two key entries are made separately in more than a debounce cycle, there would be no problem, as key depression is clearly identified. And no problem exists for 2-key lockout, as the both keys are recognized invalid.

Example of error



3. Sensor Matrix Mode

The key debounce logic is disabled in this mode. As the image of the sensor switch is kept in the FIFO, any change in this status is reported to the CPU by means of the interrupt signal INT. Although a debounce circuit is not used in this mode, it has an advantage in that the CPU is able to know how long and when the sensor was depressed.

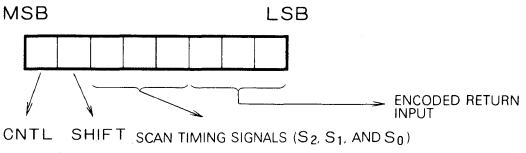
In the sensor matrix mode with the bit E = 0 of the end interrupt/error mode set command, the second most significant bit of the status word (S/E bit) is set to "1" when any sensor switch is depressed.

4. Strobe Mode

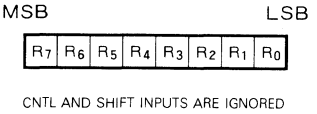
The data is entered into the FIFO from the return lines (R_0~R_7) at the rising edge of a CNTL pulse. The INT goes high while any data exists in the FIFO, in the same manner as in the keyboard mode. The key debounce circuit will not operate.

Formats of data entered into the FIFO in each of the above modes are described in the following:

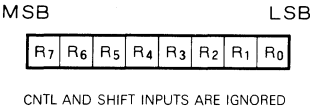
Keyboard matrix



Sensor matrix mode



Strobe mode



DISPLAY INTERFACE

The display interface is done by eight display outputs (OA_0~OA_3, OB_0~OB_3), a blanking signal ($\overline{BD}$), and scan timing outputs (S_0~S_3).

The relation between the data bus and the display outputs is as shown below:

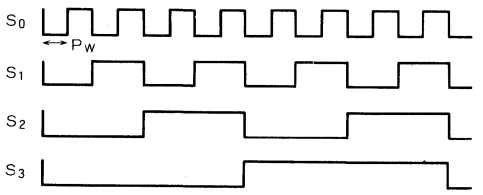
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
↓	↓	↓	↓	↓	↓	↓	↓
OA_3	OA_2	OA_1	OA_0	OB_3	OB_2	OB_1	OB_0

Clearing the display RAM is achieved by the reset signal (9-pin) but requires the execution of the clear command.

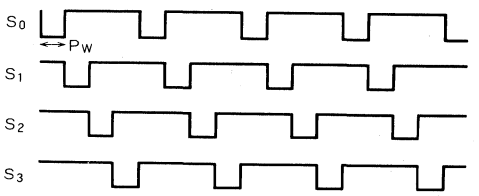
The timing diagrams for both the encoded and decoded modes are shown below.

For the encoded mode, a 3-to-8 or 4-to-16 decoder is required, according to whether eight or sixteen digit display used.

(1) Encoded mode

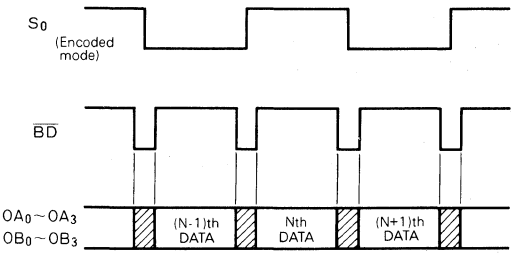


(2) Decoded mode



Note 4 : Here P_W is 640μs if the internal clock frequency is set to 100kHz.

Timing relations of S, $\overline{BD}$, and display outputs (OA_0~OA_3, OB_0~OB_3) are shown below:

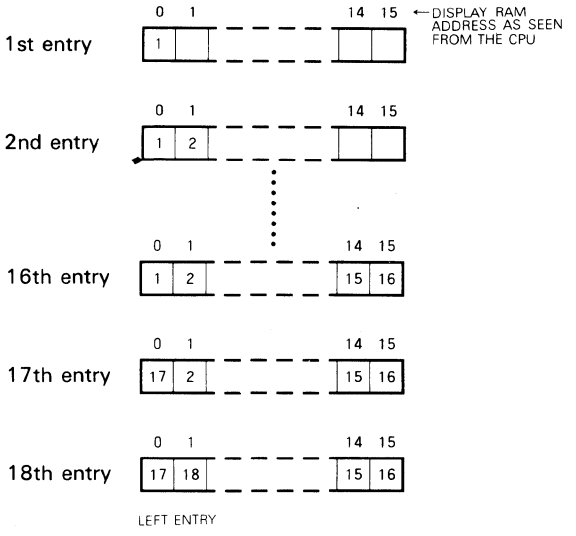


Note 5 : Values of the output data shown in the slantd line areas are decided upon the clear command executed last to become the value of the display RAM after the reset. The values in the slanted areas after reset will go low. In the same manner, the values OA_0~OA_3, OB_0~OB_3 are dependent on the clear command executed last. When the both A and B are blanked, the signal $\overline{BD}$ will be in low-level.

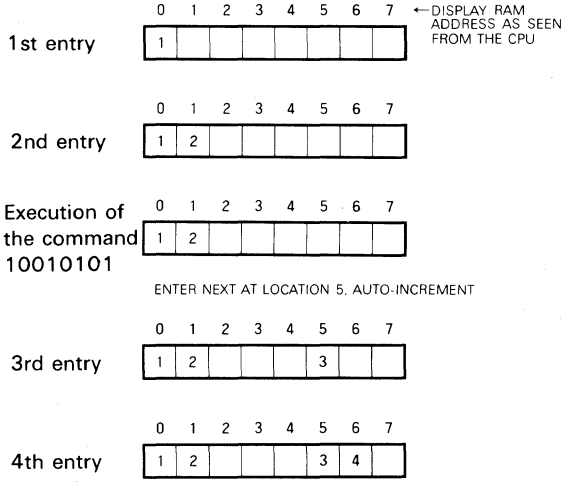
KEY ENTRY METHODS

1. Left Entry

Address 0 in the display RAM corresponds to the leftmost position ($S_3S_2S_1S_0$ = 0000) of a display and address 15 (or address 7 in 8-character display) to the rightmost position ($S_3S_2S_1S_0$ = 111 or $S_2S_1S_0$ = 111). The 17th (9th) character is entered back into the leftmost position.

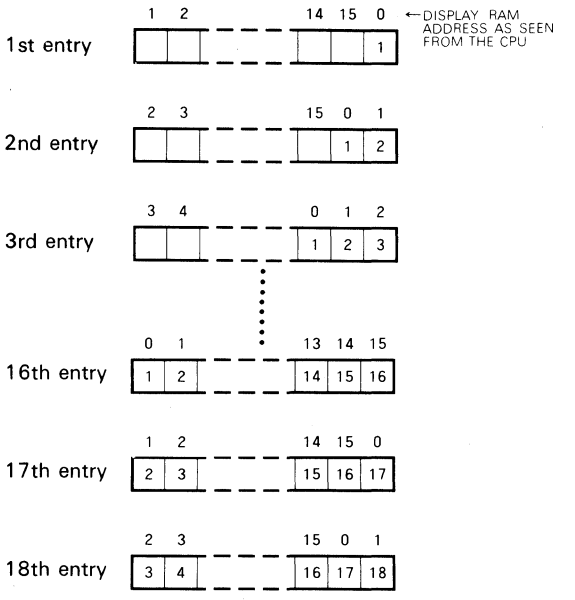


Auto-increment mode

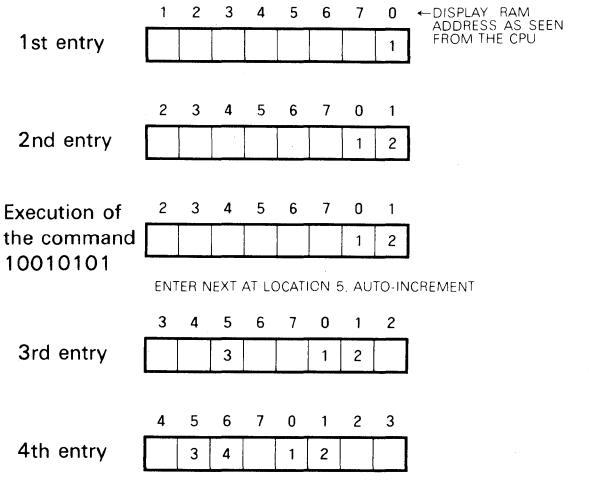


2. Right Entry

The first data is entered in the rightmost position ($S_3S_2S_1S_0$ = 0000 in 16-character display) of a display. From the next entry, the display is shifted left one character and the new data is placed in the rightmost position. A display position and a register address as viewed from the CPU change each each time and do not correspond.



Auto-increment mode



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−0.5～7	V
V_I	Input voltage		−0.5～7	V
V_O	Output voltage		−0.5～7	V
P_d	Maximum power dissipation	T_a=25℃	1000	mW
T_{opr}	Operating free-air temperature range		0～70	℃
T_{stg}	Storage temperature range		−60～150	℃

RECOMMENDED OPERATING CONDITIONS (T_a=0～70℃, unless otherwise noted.)

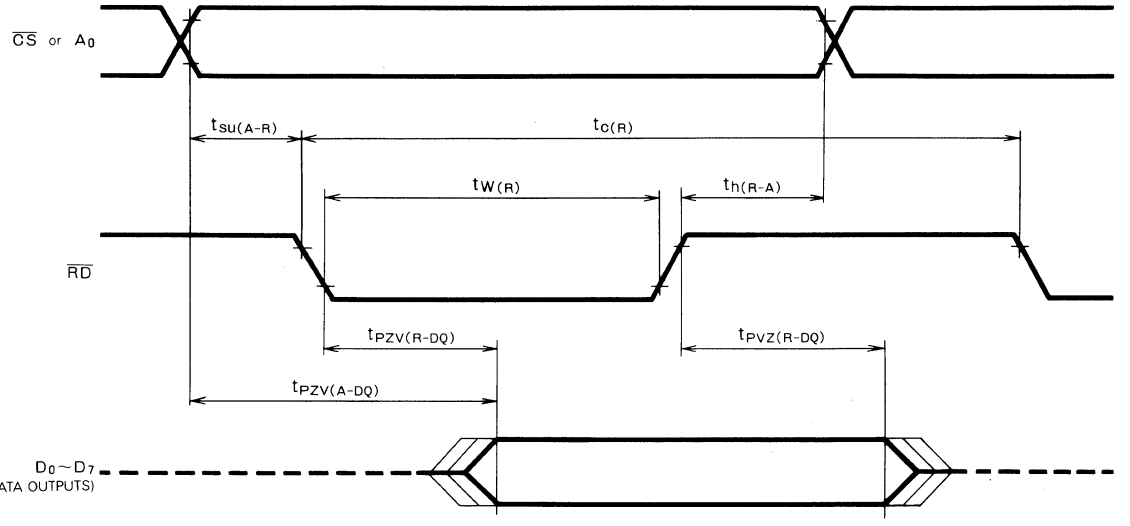
Symbol	Parameter	Limits			Unit
		Min.	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
$V_{IH(RL)}$	High-level input voltage, for return line inputs	2.2			V
V_{IH}	High-level input voltage, all others	2			V
$V_{IL(RL)}$	Low-level input voltage, for return line inputs	V_{SS}−0.5		1.4	V
V_{IL}	Low-level input voltage, all others	V_{SS}−0.5		0.8	V

ELECTRICAL CHARACTERISTICS (T_a=0～70℃ V_{CC} = (Note 6), V_{SS}=0V, unless otherwise noted.)

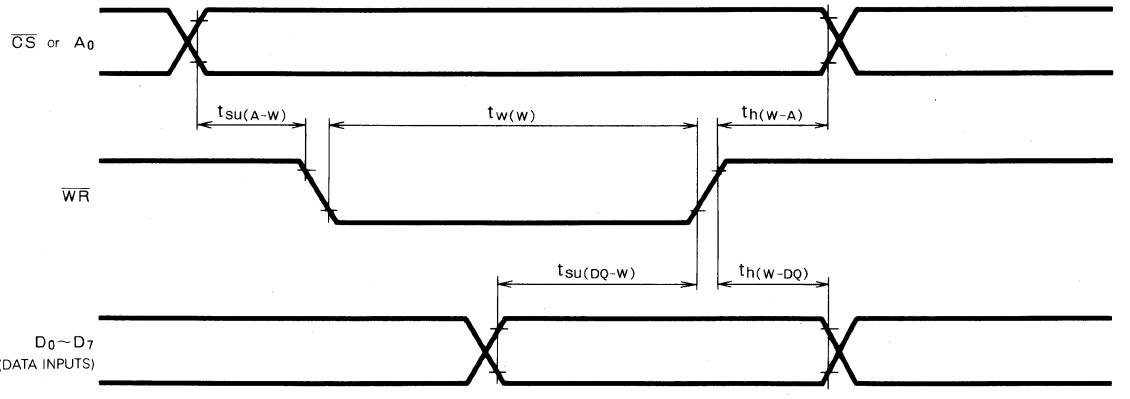
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OH}	High-level output voltage	I_{OH}=−400μA	2.4			V
$V_{OH(INT)}$	Low-level output voltage, interrupt request output	I_{OH}=−300μA	3.5			V
V_{OL}	Low-level output voltage	I_{OL}=2.2mA			0.45	V
I_{CC}	Supply current from V_{CC}				120	mA
$I_{I(RL)}$	Input current, return line inputs, shift input and control input	V_I=V_{CC}			10	μA
		V_I=0V	−100			μA
I_I	Input current, all others	V_I=V_{CC}～0V	−10		10	μA
I_{OZ}	Off-state output current	V_I=V_{CC}～0V	−10		10	μA
C_i	Input capacitance	V_I=V_{CC}	5		10	pF
C_O	Output capacitance	V_O=V_{CC}	10		20	pF

TIMING DIAGRAM

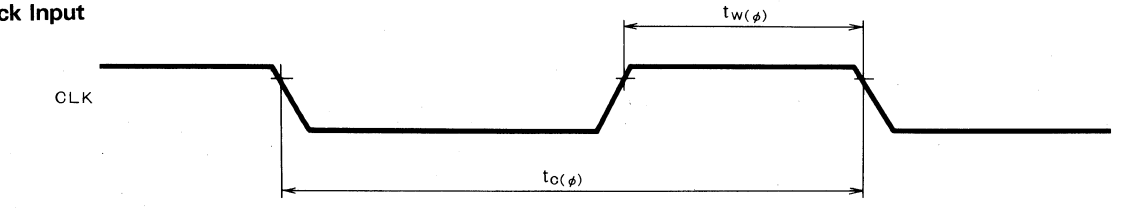
Read Mode



Write Mode



Clock Input



TIMING REQUIREMENTS (T_a=0~70℃, V_{CC}=(Note 6), V_{SS}=0V, unless otherwise noted.)

Read Cycle

Symbol	Parameter	Alternative symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{C(R)}$	Read cycle time	t_{RCY}	(Note 6)	1000			ns
$t_{W(R)}$	Read pulse width	t_{RR}		250			ns
$t_{su(A-R)}$	Address setup time before RD	t_{AR}		0			ns
$t_{h(R-A)}$	Address setup time after RD	t_{RA}		0			ns

Write Cycle

Symbol	Parameter	Alternative symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{W(W)}$	Write pulse width	t_{WW}	(Note 6)	250			ns
$t_{su(A-W)}$	Address setup time before WR	t_{AW}		0			ns
$t_{h(W-A)}$	Address hold time after WR	t_{WA}		0			ns
$t_{su(DQ-W)}$	Data input setup time before WR	t_{DW}		150			ns
$t_{h(W-DQ)}$	Data input hold time after WR	t_{WD}		0			ns

Other Timings

Symbol	Parameter	Alternative symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{C(\phi)}$	Clock cycle time	t_{CY}	(Note 6)	320			ns
$t_{W(\phi)}$	Clock pulse width	$t_{\phi W}$		120			ns

For an internal clock frequency of 100kHz

- Key scan cycle time: ~ 5.1ms
- Key debounce cycle time: ~ 10.3ms
- Single-key scan time: 80μs
- Display scan time: ~ 10.3ms
- Single digit display time: 490μs
- Blanking time: 150μs
- Internal clock cycle: 10μs

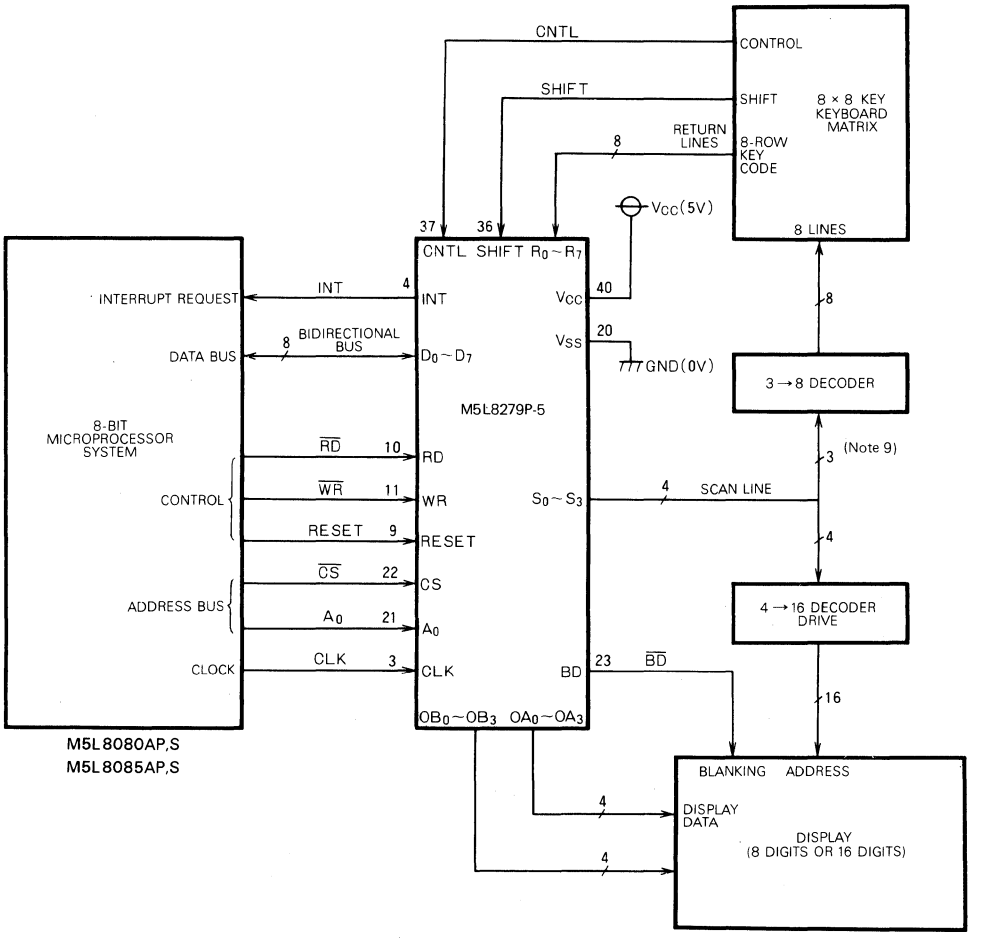
Note 6 : Test conditions:
Input pulse level: 0.45~2.4V
Input pulse rise time: 20ns
Input pulse fall time: 20ns
High-level input reference level: 2V
Low-level input reference level: 0.8V
C_L=150pF

SWITCHING CHARACTERISTICS (T_a=0~70℃, V_{CC}=(Note 1), V_{SS}=0V, unless otherwise noted.)

Symbol	Parameter	Alternative symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{PZV(R-DQ)}$	Output enable time after read	t_{RD}	(Note 7)			200	ns
$t_{PZV(A-DQ)}$	Output enable time after address	t_{AD}				250	ns
$t_{PVZ(R-DQ)}$	Output disable time after read	t_{DF}		10		100	ns

Note 7 : Test conditions
Input pulse level: 0.45~2.4V
Input pulse rise time: 20ns
Input pulse fall time: 20ns
High-level input reference voltage: 2V
Low-level input reference voltage: 0.8V
High-level output reference voltage: 2V
Low-level output reference voltage : 0.8V
C_L=150pF

APPLICATION EXAMPLE



Note 8 When using an 8-bit character display of more than 9 digits for the decoder display, it is necessary to provide a separate decoder (for example 4→10 decoder, 4→16 decoder) and key scan 3→8 decoder. Only S_0, S_1 and S_2 may be used as inputs to the key scan 3→8 decoder.

9. Don't drive the keyboard decoder with the MSB of the scan line.

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