Synario
Getting Started

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Data I/O Corporation
10525 Willows Road N.E., P.O. Box 97046
Redmond, Washington 98073-9746 USA
(206) 881-6444

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Before You Begin

This manual takes you step-by-step through design entry, simulation and implementation of a variety of designs in the Synario FPGA Design System. Among other topics, it discusses how to

- Install and enable the Synario software.
- Enter designs using schematics, ABEL-HDL modules, and combinations of the two.
- Perform functional (pre-route) simulation independent of a target device.

Installation

Installing a Synario product involves the following steps:

1. Connecting the Synario Security Device (or verifying that it is connected).
2. Installing the Synario software.
3. Creating a Registration and Enable Code Request form.
4. Sending the Registration and Enable Code Request form to Data I/O.
5. Entering permanent Enable Codes after receiving them from Data I/O.

These steps are explained in more detail below.

Connecting the Synario Security Device

Synario products are licensed by a single Security Device that attaches to your computer’s parallel port. The Security Device is delivered as part of the Synario Design Entry product and contains a unique identifier for your installation. Each Synario product is individually licensed through an Enable Code that allows a product to run only on computers that have the appropriate Security Device attached.

To connect the Synario Security Device, you need

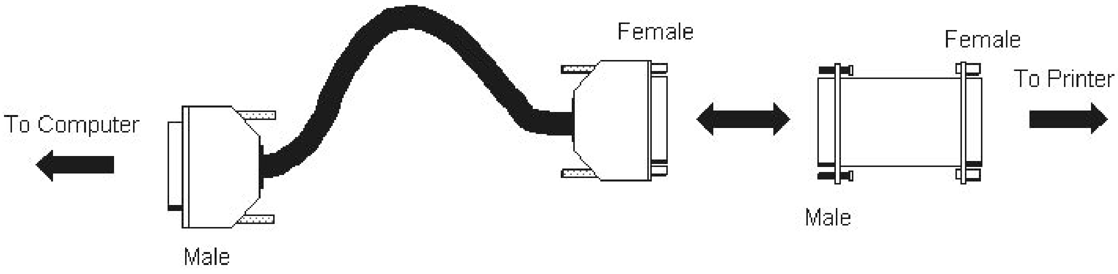
- Security Device and cable (included with Synario Design Entry product)
- Parallel port with DB-25 connector

Before connecting the Security Device, note the number (you may need to refer to it later).

To connect the Security Device:

1. Locate the parallel port on your computer. Refer to your computer system documentation.
2. Locate the Security Device and interconnection cable provided with Synario. The interconnection cable has a male DB-25 connector at one end and a female DB-25 connector at the other. The Security Device also has a male and female connector.

Note: *The interconnection cable is not required. It is provided for easier access to the Security Device.*



3. Connect the male connector of the Security Device to the female connector of the interconnection cable. Secure the connection.

Note: *If you have other Data I/O software products, you may already have one or more security devices. If so, add the Security Device to the other security devices.*

If you have the LCA Device Kit, its Security Device must be the farthest security device from the computer for proper operation.

If you have the MAX/FLEX Device Kit or the MAX+plus II software, the MAX+plus II Software Guard must be installed closest to the computer.

4. Connect the male connector of the interconnection cable to the parallel port of your computer. Secure the cable to the parallel port connector.
5. If you disconnected a printer from the parallel port, reconnect the printer to the female connector of the Security Device, using the cable that was previously connected directly to the computer.

Note: *To ensure proper operation, you may need to turn on the printer that you have connected to the Security Device. If this is necessary, power must remain on during program operation.*

Installing the Synario Software

Use the instructions below to install the software:

1. Insert Disk 1 of the Synario product into your disk drive.
2. From the Windows Program Manager, select Run from the File menu.
3. Enter

   ```
   drive:\SETUP
   ```

   where *drive* is the disk drive letter where you inserted the installation disk.
4. Follow the instructions on the screen. (They vary depending on which product is being installed.)

Note: *In general, you do NOT need to reboot your computer after installation. The installation program for the option tells you if you need to reboot.*

User Notes and Comment Forms

Important information about the product is placed in the installation directory during installation. These files are in Microsoft Write format (.WRI) and are in the README subdirectory of the installation directory.

The Synario readme file is installed as an icon in the Synario program group. This file contains last-minute release information and describes other files installed in the readme directory.

Creating a Registration and Enable Code Request Form

You need to register your Synario products with Data I/O to obtain Enable Codes that permanently license your software. Use the Data I/O Registration Editor to register Synario products and enable a 30 day license while you wait for your permanent license codes. The Data I/O Registration Editor is installed as an icon labeled "Data I/O Registration" in the Synario program group.

You can install all of your Synario products before registering them.

To register your Synario product:

1. Confirm that the Synario Security Device is attached to the computer.
2. Select the "Data I/O Registration" icon from the Synario program group.
3. The Customer Information dialog box appears. Select the Security Device Number that you want to use. (Usually there is only one number, unless you have multiple Data I/O Security Devices connected to your computer.)
4. Fill out the Customer Information dialog box. All fields not marked *Optional* must be filled out. If you do not have a facsimile machine, type the word "none" in the Fax Number field.

The information you enter allows Data I/O to create the Enable Codes to permanently activate Synario products for your Security Device, and to support you better in the future -- through better product support, timelier product information and up-to-date information about new releases and upgrades.

Note: *If your Shipping Address is different from your Mailing Address, be sure to enter it to ensure timely delivery of updates and upgrades.*

Note: *You may want to double-check the information. If Data I/O needs to contact you for additional information, delivery of your permanent Enable Codes may be delayed.*

5. When all required information has been entered, click on the Licensing button. (If the button is not enabled, there is some required information missing). The Product Information dialog box appears. This screen provides an inventory of the Synario products installed.

Note: *If the installation directory is on a network and the directory is shared, then you might see products that you have not purchased. However, without a Serial Number (described later) you will not be able to obtain a permanent Enable Code. You can evaluate the additional products by using a 30 Day license; however, the product will be unavailable after the license expires.*

6. Select the product to register. The fields in the Serial Number Card section change to match the Licensed Software title that appears on your Serial Number Card for that product.
7. Double-click on the product line or click the Enable button.
8. The License Information dialog box appears. Fill in the Serial Number field from the Serial Number Card included in your product documentation. This number is required by Data I/O to identify and verify the product that you purchased.
9. If you want to access your software immediately, select the 30 Day License from the License Type section and click the OK button.

Note: *You are allowed only one 30 Day License per product per Security Device.*

10. Repeat steps 6 through 9 until all Serial Numbers have been entered.
11. Some Synario products require additional licensing information. When those products are selected from the product list, the Extended button is enabled. See the documentation for those products for instructions on the Extended License Information dialog box.
12. After registering all software, click the Close button to return to the Customer Information dialog box.
13. Click the Print button to print the Registration and Enable Code Request form. This form will print to the default printer. For information on setting up your default printer, see your Windows documentation.
14. Click the Close button to exit the Registration Editor.

Sending the Registration Form to Data I/O for Processing

The Registration and Enable Code Request form printed out contains all the information you entered in the Registration Editor. You must send this form to Data I/O to obtain your enable codes. Use one of the following methods (listed in order of response time, from fastest to slowest):

1. Send by facsimile (fax) machine to the number at the top of the form. Data I/O returns your permanent Enable Codes to the fax number given in the Customer Information section.
2. Call the telephone number at the top of the form during the hours listed. Data I/O will take the registration information over the phone and return your call with your permanent Enable Codes.

3. Send the form by mail to the address at the top of the form. Data I/O will process the form and return the permanent Enable Codes by return mail to your Mailing Address.

Entering Permanent Enable Codes

Once you receive your Enable Codes from Data I/O, enter them as follows:

1. Confirm that the Synario Security Device is attached to the computer.
2. Run Data I/O Registration Editor from the Synario program group.
3. Click the Licensing button to display the Product Information dialog box.
4. Select a product to enable and either double-click on the product line or select the Enable button to display the License Information dialog box.
5. If not already chosen, select the License Type labeled "Permanent License."
6. Enter the Enable Code for the selected product into the Enable Code field.
7. Click the OK button to exit the License Information dialog box and return to the Product Information dialog box.

Note: *If the Enable Code entered does not match the other information regarding the license, then clicking the OK button will result in a message box stating that the Enable Code is invalid. Return to the License Information dialog box and carefully check that the Enable Code was entered correctly and for the correct product.*

8. Repeat steps 4 through 7 until all Enable Codes have been entered. The Enable Code Status in the product list will change to Permanent. After all codes have been entered, select the Close button to return to the Customer Information dialog box.
9. Select the Close button to exit the Registration Editor.

Tutorial Prerequisites

Some of the procedures in the tutorials require specific device kits and the Verilog Simulator to function exactly as described. If you do not have the required device kit or the Verilog Simulator, you can still follow parts of all of the tutorials. The tutorials list which device kits they use.

All of the files for these tutorials are available in the examples\tutorial directory.

Design Methods

Each of the example circuits has a specific set of goals, and the design entry methods described for each tutorial are intended to help you learn specific functions of the product. However, since Synario can be used in many different ways, the same designs could be entered, simulated and implemented using whatever design entry method and ordering of tasks that is most comfortable for you. Your *User Manual* explains these methods and tasks in detail, and provides a higher-level view of Synario's capabilities.

How to Use this Guide

This guide contains the following sections:

- Tutorial 1: Examining an Existing Project
- Tutorial 2: Entering and Simulating a Schematic-based Design
- Tutorial 3: Using ABEL-HDL in Synario

Tutorial 1
Examining an Existing Project

By examining an existing project, you can learn the basics of creating and testing designs with Synario. The example design in this project is one of the Programmable Electronics Performance Corporation (PREP) benchmark circuits.

This tutorial shows you how to:

- Start Synario and open an existing project.
- Identify various project sources by their icon.
- Observe processes defined for each project source.
- Access online help.
- Use source editors and the Hierarchy Navigator.
- Use the Verilog Simulator (if you have this option).

Opening an Existing Project

Designs entered using Synario can contain a number of files that describe and verify the design, including the following:

- Schematics
- ABEL-HDL modules
- VHDL modules
- Verilog test fixtures
- VHDL test benches
- Text files or any other files related to the design, such as design specifications.

To help you manage a large design containing many files, Synario collects all of the files into a *project*. When you open an existing design, or create a new one, you are opening or creating a Synario project.

This tutorial uses the PREP benchmark circuit number 2.

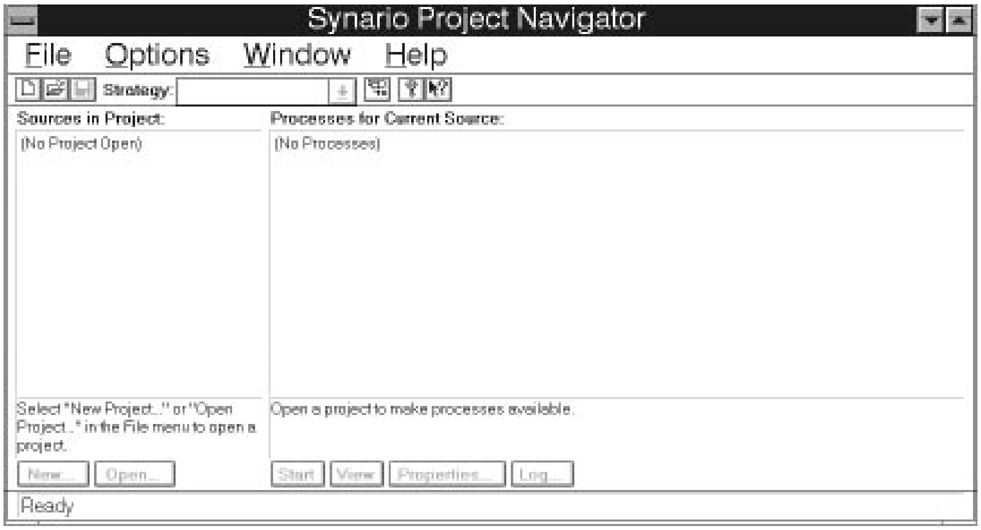
To open the existing project:

1. Start Synario by double-clicking on the Synario icon.

   When Synario initializes, it loads the last used project, so if someone has previously opened a project, Synario loads that project on startup.

   If you have not opened a project already (or if you have disabled the Open Previous Project option), you will see a blank Synario project like the one shown in Figure 1-1.

Figure 1-1
Synario Project Navigator



(No Project Open)

(No Processes)

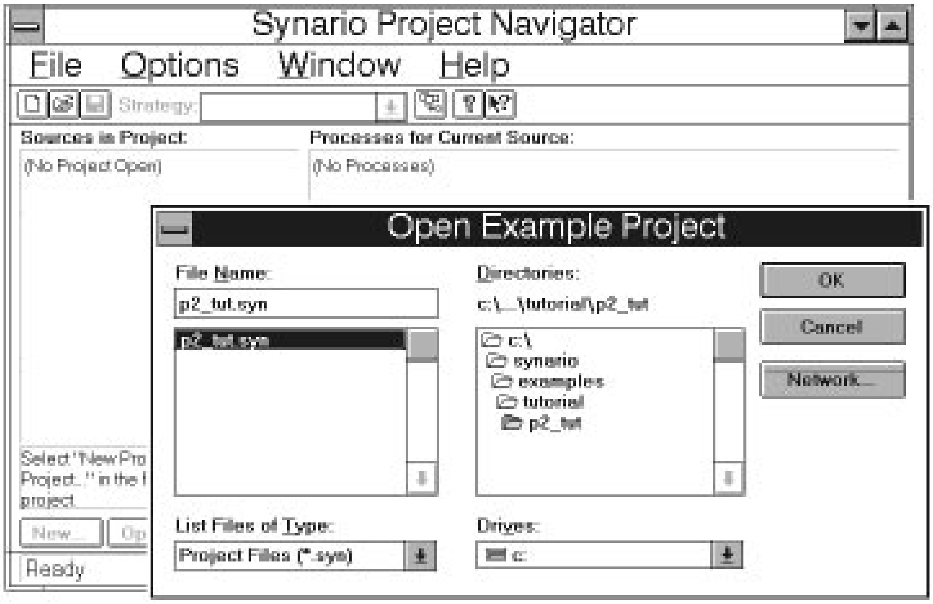
Select "New Project..." or "Open Project..." in the File menu to open a project.

Open a project to make processes available.

Ready

2. To open the PREP benchmark 2 circuit, select Open Example from the File menu. Navigate through the example directories until you are in the synario\examples\tutorial\p2_tut directory as shown in Figure 1-2.
3. Highlight the Synario project, p2_tut.syn, and click OK or press Enter to exit the dialog box. There is a pause while Synario loads the project. When the project is open, the display should look similar to Figure 1-3.

Figure 1-2
Opening an Example: Open Example Dialog Box



Sources in Project: (No Project Open)

Processes for Current Source: (No Processes)

Select "New Pro
Project..." in the
project.

New... Op

Ready

File Name: p2_tut.syn

p2_tut.syn

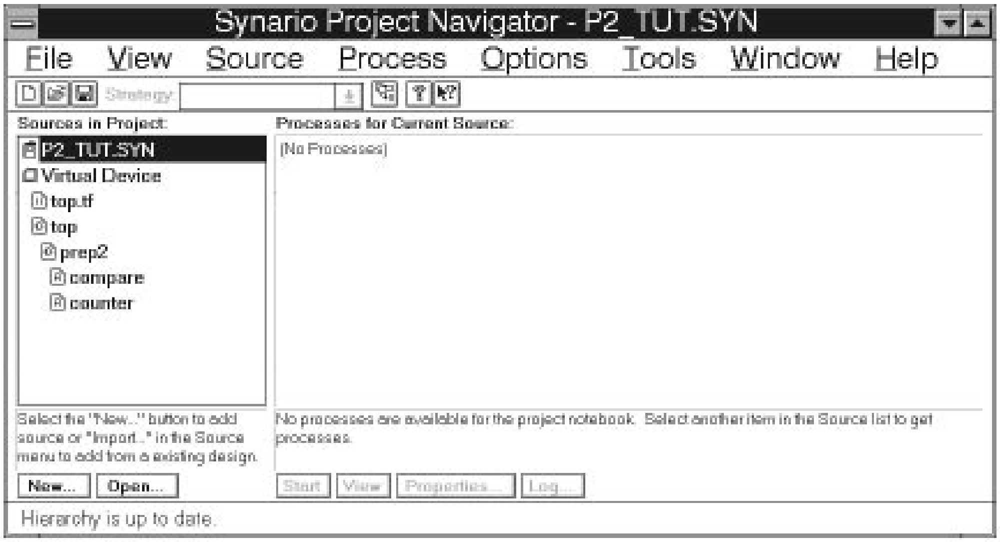
Directories: c:\...\tutorial\p2_tut

c:\
synario
examples
tutorial
p2_tut

List Files of Type: Project Files (*.syn)

Drives: c:

Figure 1-3
PREP2 Project Loaded into Synario



Select the "New..." button to add source or "Import..." in the Source menu to add from a existing design.

No processes are available for the project notebook. Select another item in the Source list to get processes.

Hierarchy is up to date.

Project Sources

A Synario project is composed of one or more items called sources. Sources include files such as schematics, HDL source files, and test stimulus files. Each type of source is identified by an icon and name in the *Sources in Project* window. The *Sources in Project* window is the large scrollable window on the left side of the Synario Project Navigator display. The *Sources in Project* window for the prep2 project lists all of the sources that are a part of this design.

In addition to the sources that describe the function of the design, every Synario project contains at least two special types of sources: the project notebook and the device.

Project Notebook

The project notebook is where you enter the title and name of the project. The project notebook can also be used to keep track of external files (such as document files) that are related to your project. You'll learn how to use the project notebook in a later tutorial.

Device

The device is a source that includes information about the currently-selected device. This design has been entered without a device specified, so the device shown is "Virtual Device."

The remaining sources listed in the prep2 project are:

A top-level schematic (top)

A behavioral simulation Verilog test fixture (top.tf)

Two lower-level ABEL-HDL modules (compare and counter)

A lower-level schematic (prep2)

These sources define the logic of the design (in the form of a mixed hierarchy of ABEL-HDL and schematic design files) and the Verilog test fixtures for performing behavioral and timing simulation.

Project Processes

Synario has two primary windows that display information about your design. The *Sources in Project* window described above contains all of the sources in your design. Some sources have a unique set of tasks (processes) that must be performed to complete the design for simulation or implementation. When you select a source, the Synario *Processes for Current Source* window reflects the processing required for that source.

To see the processes change:

Use the mouse to highlight each of the sources in the *Sources in Project* window, and see the processes defined for each type of source.

In the tutorials that follow, you will learn about these different processes, and see how they are used to process a design for simulation and implementation in a device.

See Also

For detailed information about each of these processes, refer to the online help.

Online Help

Use Synario's online help to guide you through the design entry process. The help contains task-oriented as well as reference information.

Browsing Online Help

Click on the help icon and spend a few minutes browsing through the Synario Help Map.

Getting Context-sensitive Help

Click on the context help icon, then move the help cursor to a part of the screen you'd like to see help on, such as the Processes for Current Source window, and click the left mouse button. Synario displays help about the area of the screen you select.

Examining the Project Sources

Using the Source Editors

The prep2 project consists of a top-level schematic, and lower-level schematic and ABEL-HDL module sources. To view or edit a source file, double-click on it in the *Sources in Project* window. Synario runs the appropriate source editor (schematic or text) and loads the selected source.

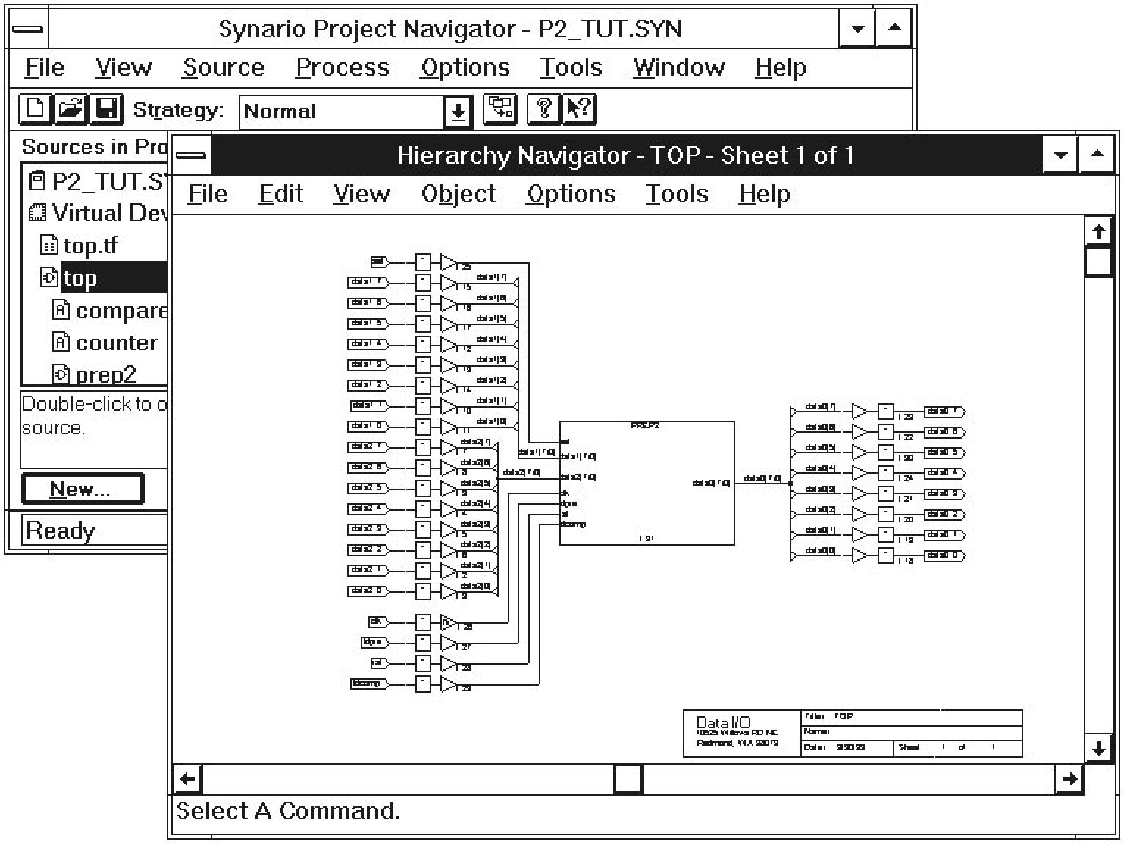
Try double-clicking on each of the project sources (“top,” “compare,” “counter” and “prep2”). To exit the source editors (schematic, text or other), choose Exit from the File menu.

Viewing Sources with the Hierarchy Navigator

If your design is hierarchical and has a top-level schematic, you can use an alternate method to examine the source files that make up the design:

1. In the prep2 project, highlight the schematic source **top** (do not double-click).
2. Double-click on Navigate Hierarchy in the *Processes for Current Source* window. Synario rebuilds the hierarchy and displays the top-level source, as shown in Figure 1-4.
3. In the Hierarchy Navigator, select Push / Pop from the View menu. The Hierarchy Navigator allows you to move up and down (“push” and “pop”) to navigate through the sources in your design hierarchy as shown in the following steps.
4. To “push” into a lower-level module in the design, click on the block symbol in the center of the hierarchy display. The Hierarchy Navigator moves down to the next level in the hierarchy and displays the lower-level block diagram of the circuit (Figure 1-5).
5. Move the cursor over the compare block and click the mouse button. The Hierarchy Navigator displays the Text Editor, loaded with a lower level in the hierarchy: the ABEL-HDL source file that describes the function of the compare block.
6. With the Text Editor still open, move the cursor over the counter block in the schematic and click the mouse button. The Text Editor loads another lower level in the hierarchy: the ABEL-HDL source file that describes the function of the counter block. Move between the two ABEL-HDL sources by clicking on the window of each.

Figure 1-4
Using the Hierarchy Navigator


Synario Project Navigator - P2_TUT.SYN
File View Source Process Options Tools Window Help
Sources in Pro
P2_TUT.S
Virtual Dev
top.tf
top
compare
counter
prep2
New...
Hierarchy Navigator - TOP - Sheet 1 of 1
File Edit View Object Options Tools Help
PREP2
Data I/O
File: TOP
Name:
Sheet 1 of 1

Strategy: Normal

Double-click to o
source.

Ready

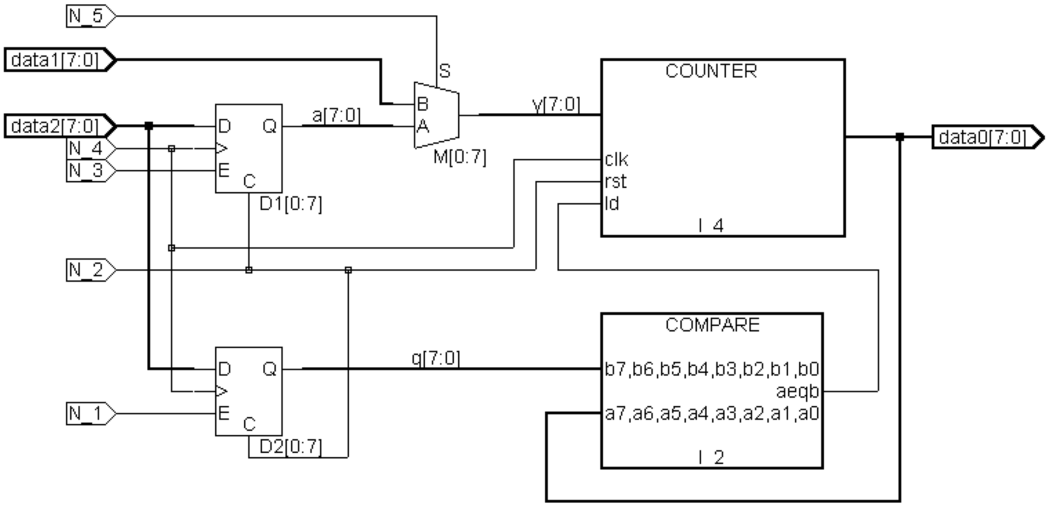
Select A Command.

7. Close the Text Editor. Back in the block diagram, you can move further up the hierarchy by moving the cursor to an empty area of the schematic and clicking the mouse button.

8. Spend a few minutes experimenting with the Hierarchy Navigator. Push and pop up and down the hierarchy, and try using the zoom features (select Zoom In from the View menu) of the Hierarchy Navigator to get a closer view of the schematic portions of the design.

Note: *The Hierarchy Navigator is a view-only mode of the Schematic Editor that gives you a graphical view of the Schematic Editor's connectivity database. Some items (like certain attributes) can be changed in the Hierarchy Navigator, but most other items cannot be changed.*

Figure 1-5
PREP Benchmark Circuit #2 Block Diagram Schematic



9. Select Exit from the File menu to exit from the Hierarchy Navigator. (If you have made any changes, answer “No” when Synario asks if you want to save the changes.)

Viewing Test Stimulus Sources

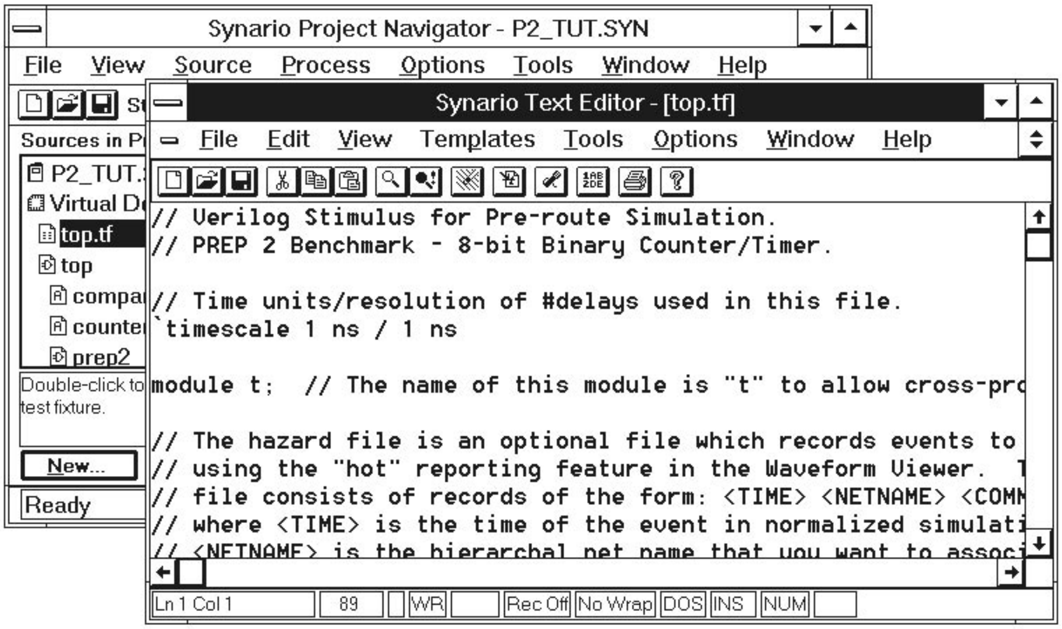
In addition to the schematic and ABEL-HDL sources that define the logic of this design, there is an additional source, called a Verilog test fixture, that defines the test stimulus for simulation. Test fixtures describe how the design is to be exercised during simulation.

In the *Sources in Project* window, find the test fixture (.tf) source, a test fixture **top.tf**. To view the test fixture file, double-click on top.tf in the *Sources in Project* window. The Text Editor displays the Verilog file describing the functional test stimulus for this project (see Figure 1-6).

Later tutorials describe how Verilog test fixtures are entered and used, and documentation included with the Verilog Simulator describes how you can quickly get started using Verilog.

After you have finished examining the test fixture, exit the Text Editor and return to the Synario Project Navigator (the main window).

Figure 1-6
Verilog Test Fixture for PREP Benchmark Circuit #2


Synario Project Navigator - P2_TUT.SYN
File View Source Process Options Tools Window Help
St
Sources in P
P2_TUT.
Virtual D
top.tf
top
compa
counte
prep2
Double-click to
test fixture.
New...
Ready
Synario Text Editor - [top.tf]
File Edit View Templates Tools Options Window Help
Ln 1 Col 1
89
WR
Rec Off
No Wrap
DOS
INS
NUM

```
// Verilog Stimulus for Pre-route Simulation.
// PREP 2 Benchmark - 8-bit Binary Counter/Timer.

// Time units/resolution of #delays used in this file.
`timescale 1 ns / 1 ns

module t;  // The name of this module is "t" to allow cross-pro

// The hazard file is an optional file which records events to
// using the "hot" reporting feature in the Waveform Viewer.  T
// file consists of records of the form: <TIME> <NETNAME> <COMM
// where <TIME> is the time of the event in normalized simulati
// <NETNAME> is the hierarchal net name that you want to associ
```

Using the Verilog Simulator

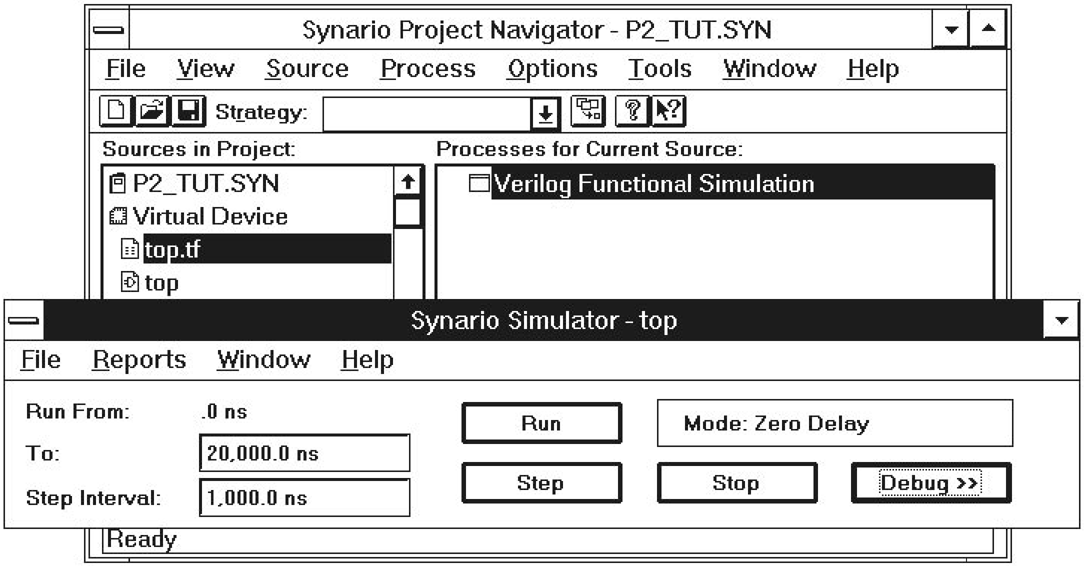
Note: *If you do not have the Verilog Simulator, go to Tutorial 2.*

To start the Verilog Simulator:

1. Highlight the test fixture source named top (do not double-click.)
2. Select the Verilog Functional Simulation process in the *Processes for Current Source* window.
3. To start the process, double-click on the process name (Verilog Functional Simulation).

The Verilog Simulator starts as shown in Figure 1-7. (There is a pause while the Simulator initializes, builds the simulation model for the design and reads the test fixture file.)

Figure 1-7
The Verilog Simulator Control Panel


Synario Project Navigator - P2_TUT.SYN
File View Source Process Options Tools Window Help
Strategy:
Sources in Project:
P2_TUT.SYN
Virtual Device
top.tf
top
Processes for Current Source:
Verilog Functional Simulation
Synario Simulator - top
File Reports Window Help
Run
Step
Stop
Debug >>
Ready

Run From: .0 ns
To: 20,000.0 ns
Step Interval: 1,000.0 ns
Mode: Zero Delay

Before you can run a simulation, Synario may need to update other processes. Synario keeps track of which processes have been run, so if you modify one part of the design, the other parts are not reprocessed.

The following processes may be updated when you start the Simulator:

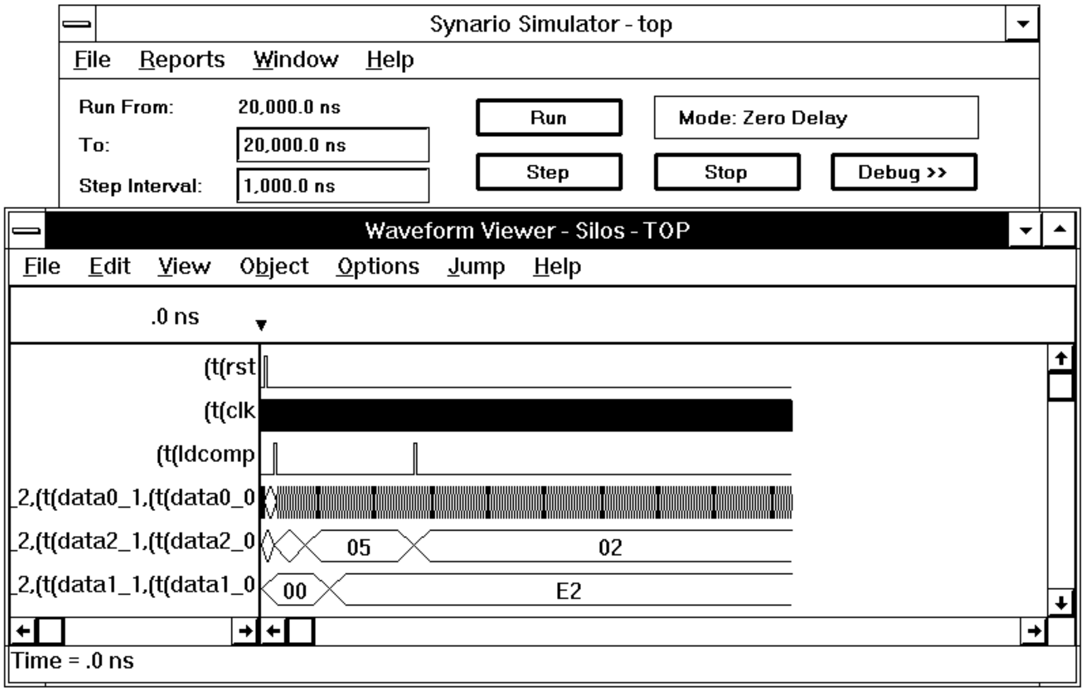
- Translate all of the design-related sources in the project (the schematics and ABEL-HDL files) into simulation models.
- Read and process the test fixture file (in this case, “top.tf”).

When the required processes are updated, the Simulator Control Panel displays the default simulation times.

To run a simulation and view the results:

1. Click the Run button. The simulation of the circuit is very fast, so you might not notice any pause.
2. When simulation is complete, select Waveform Viewer from the Window menu in the Simulator Control Panel. The Waveform Viewer displays the simulation results (see Figure 1-8).

Figure 1-8
Simulation Waveform Viewer



Synario Simulator - top

Run From: 20,000.0 ns
To: 20,000.0 ns
Step Interval: 1,000.0 ns
Mode: Zero Delay

Waveform Viewer - Silos - TOP

Time = .0 ns

3. Spend a few minutes becoming familiar with the features of the Waveform Viewer:

- Try the View: Zoom feature to zoom in on part of the waveform.
- Experiment with adding and deleting signals from the waveform display (select Show from the Edit menu).

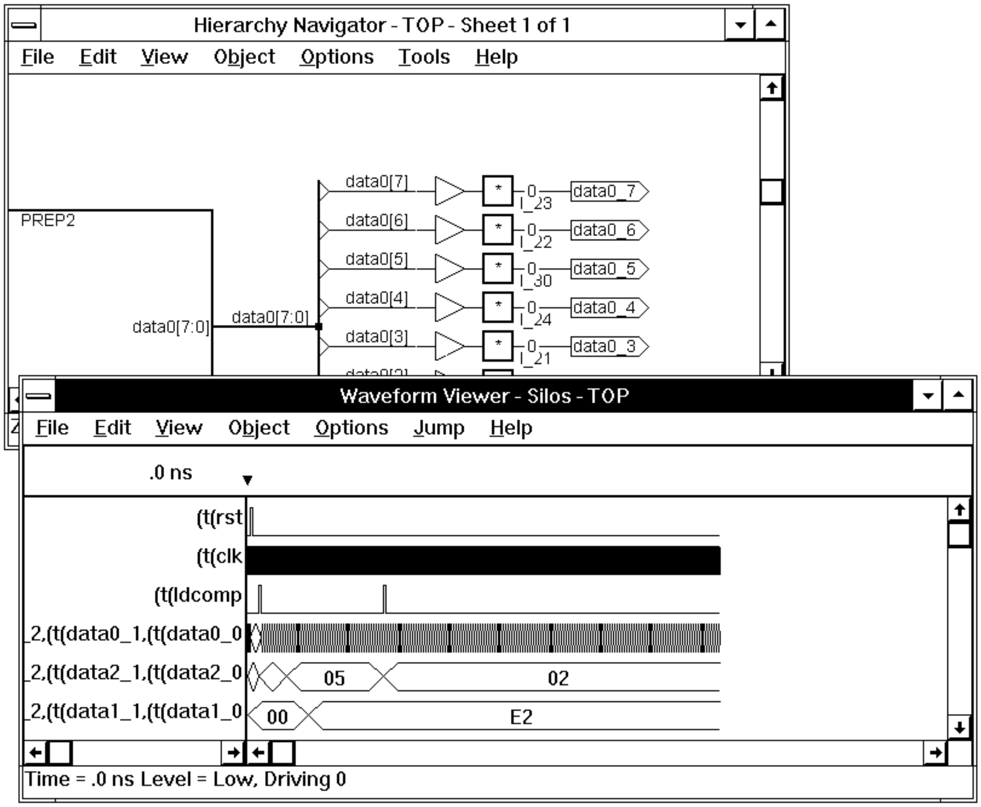
To view simulation results on the schematic:

Viewing simulation results on the schematic is called *cross-probing,* and is accessed from the Hierarchy Navigator.

1. Keep the simulation Waveform Viewer open (do not exit or close the Waveform Viewer).
2. In the *Sources in Project* window, highlight the top-level schematic (top).
3. In the *Processes for Current Source* window, double-click on Navigate Hierarchy.

   The Hierarchy Navigator displays the design. Just as before, you can move up and down in the hierarchy, but now you see actual simulation values attached to the inputs and outputs of the circuit.
4. Arrange the waveform and Hierarchy Navigator windows so that both are visible as shown in Figure 1-9.
5. In the Waveform Viewer, use the mouse to select different time positions and watch the Hierarchy Navigator. The values shown on the schematics change to reflect the values at the selected times.

Figure 1-9
Cross-probing Between a Schematic and the Waveform Viewer



Time = .0 ns Level = Low, Driving 0

Where To Go Next

This completes the Examining an Existing Project tutorial. All of the features that are in this introduction have been related to design entry and simulation. The tutorials that follow lead you through specific aspects of the design entry process, and describe how designs are implemented.

Tutorial 2

Entering and Simulating a Schematic-based Design

This tutorial describes how to:

- Use the Schematic Editor to enter a simple circuit.
- Use the Text Editor to create a Verilog test fixture for simulation.
- Run a behavioral simulation of the circuit (if you have the Verilog Simulator).

The circuit consists of one AND gate feeding a D flip-flop, entered with the Schematic Editor. In the next tutorial you will learn how to enter and simulate a design that is described using ABEL-HDL.

Entering the Circuit

Entering a new schematic-design circuit in Synario entails the following basic steps:

- Setting up a new project
- Adding a new schematic to the project
- Creating the schematic

These steps are detailed below.

Setting Up a New Project

Before you start entering a circuit, you need to start Synario and set up a new project.

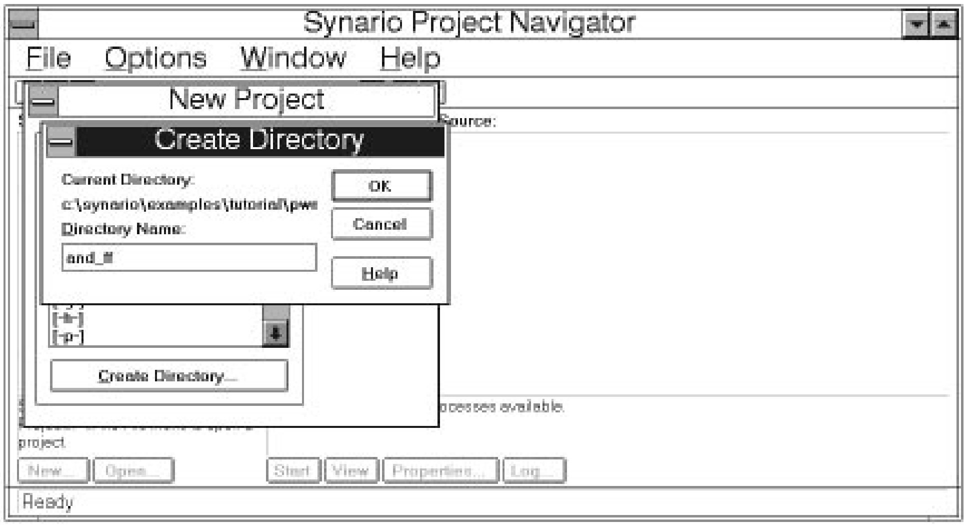
To set up a new project:

1. Start Synario and select New Project from the File menu. Synario prompts you for the working directory for your new project.

2. Navigate to the location where you wish to create a new directory (for example, **\examples\tutorial**). Then, select Create Directory, and enter a name for a new project directory. All projects should be kept in separate directories.

   This tutorial refers to the **\and_ff** directory as shown in Figure 2-1. (You can use your own directory and substitute its name wherever the **\and_ff** directory is indicated.)

Figure 2-1
New Project: Create Directory Dialog Box



Current Directory:
c:\synario\examples\tutorial\pwr
Directory Name:
and_ff

3. Click OK to exit the Create Directory dialog box, then click OK to exit the New Project dialog box.

   Synario resets the selected device to the default (Virtual Device) and re-configures to the default state. (The first time you enter Synario, it is in the default state.)

4. Change the project name by double-clicking on the project Notebook (“Untitled”) icon at the top of the *Sources in Project* window.

5. Enter the project name AND_FF.SYN (In most cases, the project name does not have to have the same name as the directory you created), and click OK.

6. Save the project by selecting Save As from the File menu. Enter **and_ff.syn** in the File Name text box.

7. Click OK to exit the Save Project As dialog box.

Adding a New Schematic to the Project

Once you have a new project set up, you can add a schematic source.

To add a new schematic:

1. Click the New button below the *Sources in Project* window.
   Synario prompts you for the type of source you wish to create.
2. Select Schematic from the list of source types, and click OK.
   The Schematic Editor runs, and a dialog box prompts you for a name for the new schematic.
3. Enter **andff** in the File Name text box and click OK (or press Enter).

   The Schematic Editor now displays a blank schematic named andff.

Creating the Schematic

The next step is to add the appropriate symbols and interconnecting wires to the schematic. In the Schematic Editor, you add symbols by selecting Symbol from the Add menu.

Using the Add Symbol Command

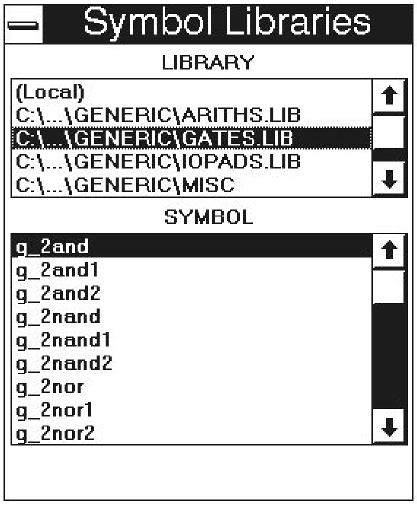
When you select Add: Symbol (or press F2), the prompt line at the bottom of the schematic window prompts you to select a symbol name from the list shown in the Symbol Libraries dialog box. You can select a symbol in two ways:

♦ Type the symbol name on the prompt line and press Enter.

OR ♦ Click on a symbol library in the Symbol Libraries dialog box shown in Figure 2-2, then click on a symbol in the Symbol list box.

The symbols shown in the Symbol Libraries dialog box are organized by type, and vary according to the device selected. Since you have not selected a device for this design, the symbols listed are from the Generic Library. The symbols in the Generic Library are not specific to any device, so you can use them in schematics targeted to any device kit that supports schematic entry. See the *SCS Reference* for more information.

Figure 2-2
Symbol List



(Local)
C:\...\GENERIC\ARITHS.LIB
C:\...\GENERIC\GATES.LIB
C:\...\GENERIC\IOPADS.LIB
C:\...\GENERIC\MISC

g_2and
g_2and1
g_2and2
g_2nand
g_2nand1
g_2nand2
g_2nor
g_2nor1
g_2nor2

Adding Symbols and Wires to the Schematic

This tutorial uses two symbols from the Generic Library:

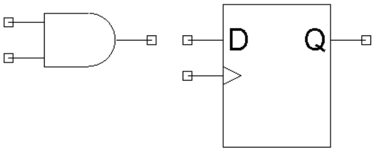
- a 2-input AND gate
- a D flip-flop

To add the symbols:

1. List the gate symbols by selecting ..\GENERIC\GATES.LIB in the Library list box.
2. Select g_2and (a 2-input AND gate) in the Symbol list box.
3. Move the cursor onto the schematic. An outline of the symbol is attached to the cursor.
4. Click the left mouse button to place the symbol on the schematic
5. Return to the Symbol Libraries dialog box, and select the REGS Library, then the g_d symbol (a D flip-flop).
6. Place the D flip-flop to the right of the AND gate, with the D input of the flip-flop vertically aligned with the output of the AND gate. (Leave some space between the two symbols as shown in Figure 2-3. The space between the symbols is important during simulation of the design later in this tutorial.)

Your schematic should be similar to Figure 2-3.

Figure 2-3
Adding an AND Gate to the Schematic



To connect the symbols with wires:

1. Select Wire from the Add menu.
2. To connect the output of the AND gate to the D input of the flip-flop, click the left mouse button once on the output stub of the AND gate, and once on the input stub of the D flip-flop.

Identifying Schematic Inputs and Outputs

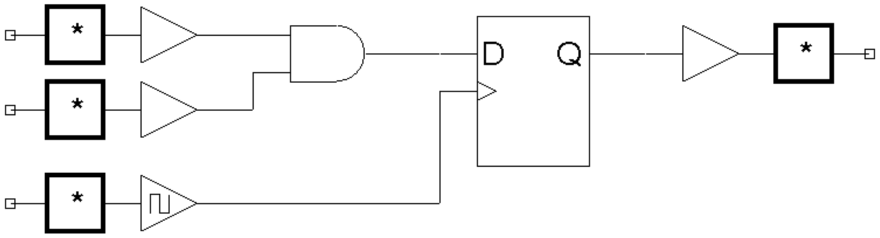
For simulation and device mapping, the input buffers, output buffers, clock buffers, named nets and I/O markers in your schematic need to be identified. Input, output and clock buffers are identified by adding the appropriate symbols from the IOS symbol library.

To identify the buffers in your schematic:

1. Use Add: Symbol to place two input buffers (g_input) in front of the AND gate.
2. Place a clock buffer (g_clkbuf) in front of the clock input to the flip-flop.
3. Place an output buffer (g_output) after the output of the flip-flop.
4. Connect the symbols with Add: Wire so your drawing looks similar to Figure 2-4.

Next, you must name the input and output signals (nets) of your schematic for reference during simulation.

Figure 2-4
Adding a Input, Output and Clock Buffers to the Schematic



To create input and output signals:

1. Choose Net Name from the Add menu. The schematic editor prompts you for net names on the prompt line.
2. Type in a net name (input_1) and press Enter.
3. Click on the top, left pin stub, and drag horizontally to the left.

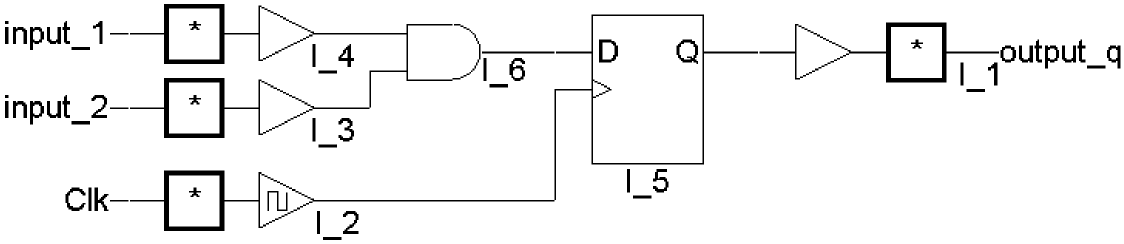
   The schematic editor creates and names the net with the name you chose in step 1.
4. Repeat steps 2 and 3 to name the other two input wires **input_2** and **Clk**, as shown in Figure 2-5, except that for these two wires, you do not need to drag the mouse; simply click on the pin stub.

   The schematic editor remembers the last wire length you created and repeats it whenever you click on a pin stub.
5. Name the output wire **output_q** by repeating steps 2 and 3, except that you should drag horizontally to the right from the output pin stub. Clicking on the pin stub will position the name incorrectly.

Note: *If you make a mistake while creating a schematic, you can undo it by choosing Undo from the Edit menu. You can undo as far back as you like.*

The last step is to mark the signals as inputs and outputs.

Figure 2-5
Schematic with Named Wires

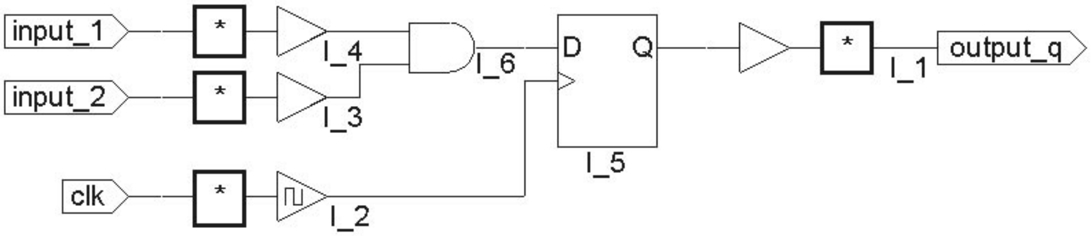


To mark the signals as inputs and outputs:

1. Choose I/O Marker from the Add menu.
2. In the I/O Markers dialog box, click Input. Then, drag a box around the three circuit inputs to add an input marker symbol around each of the input net names.
3. In the I/O Markers dialog box, click Output, then click on the output_q net to create an output I/O marker.

The schematic should be similar to Figure 2-6.

Figure 2-6
Complete Schematic



Saving the Schematic and Exiting

To save the schematic:

Choose Save from the File menu.

To exit the Schematic Editor:

Double-click on the close box

OR Choose Exit from the File menu.

When you exit the Schematic Editor, Synario updates the *Sources in Project* window to include the new schematic source.

Creating a Test Fixture

To perform Verilog simulation on a design in Synario, you must create circuit stimuli using a subset of the Verilog language.

Note: *In addition to Verilog simulation, you may also perform Equation or JEDEC simulation. For Equation or JEDEC simulation, you create test vectors rather than Verilog test fixtures (See the example in Tutorial 3).*

To perform Verilog simulation, you must have the Verilog Simulator licensed and installed.

For this simple circuit, you can create a Verilog stimulus file that sets up the clock and applies a few combinations of input stimulus to the AND gates. When you simulate the design in the next section, you will see how the stimulus you create results in values appearing on the circuit outputs.

There are two basic parts to a Verilog stimulus file:

- Circuit declarations
- Test stimulus

Creating a Test Fixture File

To create the test fixture and associate it with the device:

1. Create a new text fixture file for your design by clicking the New button below the *Sources in Project* window, then clicking on Verilog Test Fixture in the New Source dialog box. Then click OK.

The Associate Test Fixture dialog box prompts for whether you want the test fixture to be associated with the Virtual Device or with the **andff** source.

2. Choose Virtual Device, and click OK.
3. In the New File dialog box, enter **andff** and click OK.

Associating Test Fixtures

You can write test fixtures for your entire design, or for individual sources of a design (such as lower-level schematics or ABEL-HDL modules).

Test Fixtures for Lower-level Sources

If you associate a test fixture with a lower-level source,

- You can simulate portions of the design before the entire design is complete.
- You cannot do post-route (timing) simulation, since this type of simulation can be performed only on the entire design, after fitting to a device.

Test Fixtures for the Device

If you associate a test fixture with a device (or with the top-level source in a hierarchical design):

- You can simulate the design as a whole.
- If Synario supports post-route (timing) simulation for the selected device, you can perform accurate timing simulation of the circuit.

Creating Test Stimulus

Use the Text Editor to create the Verilog test stimulus shown below. The Verilog statements are explained in the following paragraphs.

When you have entered the statements shown, save the file by choosing Save from the Text Editor File menu, then exit the Text Editor. The test fixture file, andff.tf, is added to the project.

```
‘timescale 1 ns / 1 ns
module t;
‘ include “andff.tfi”
    initial begin
        #0  Clk = 0;
            input_1 = 0;
            input_2 = 0;

        #20 Clk = 1;
        #20 Clk = 0;

        #10 input_1 = 0;
            input_2 = 1;

        #10 Clk = 1;
        #20 Clk = 0;

        #10 input_1 = 1;
            input_2 = 1;

        #10 Clk = 1;
        #20 Clk = 0;
    end
endmodule
```

The stimulus is written using simple Verilog statements:

‘ timescale 1 ns / 1 ns — Defines the time scale and resolution as one nanosecond.

‘ include “andff.tfi” — Includes the andff.tfi file in the current stimulus file (andff.tf).

module t;
... endmodule — Defines a module name for the test fixture. (The name "t" is required to allow schematic cross-probing.)

initial begin
... end — Encloses a block of circuit stimulus statements. Statements within this block specify values for the clock (Clk), and for the inputs (input_1 and input_2) using relative times.

#0 Clk = 0;
...
#20 Clk = 0; — Define the actual circuit stimulus. The #n prefixes define the amount of time that is to elapse before the next statement is executed.

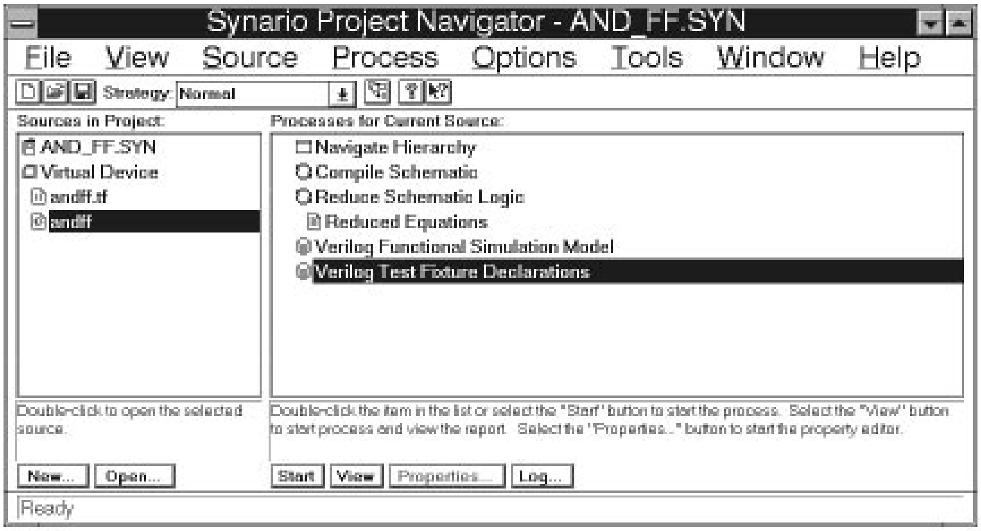
Circuit Declarations

The first part of a Verilog stimulus file contains declarations about the circuit being simulated. These declarations include a list of ports (inputs and outputs of the circuit) as well as any simulation initialization information (such as powerup information). In most cases, the declaration information can be generated automatically by Synario.

To create the declarations part of a Verilog test stimulus:

1. Highlight the top-level schematic (in this case, **andff**) in the *Sources in Project* window.
2. Double-click on Verilog Test Fixture Declarations in the *Processes for Current Source* window as shown in Figure 2-7.

Figure 2-7
Creating the Verilog Test Fixture Declarations



Strategy: Normal

Sources in Project:
AND_FF.SYN
Virtual Device
andff.tf
andff

Processes for Current Source:
Navigate Hierarchy
Compile Schematic
Reduce Schematic Logic
Reduced Equations
Verilog Functional Simulation Model
Verilog Test Fixture Declarations

Double-click to open the selected source.

Double-click the item in the list or select the "Start" button to start the process. Select the "View" button to start process and view the report. Select the "Properties..." button to start the property editor.

Ready

The Verilog Test Fixture Declarations process creates a template file that you can use as a basis for your test fixture. The template file is created with a .TFI file name extension.

The template file can be included in your .TF test fixture file (with a Verilog **‘ include** statement). If you later change your design (to add new I/Os, for example) and regenerate the template, the changes are immediately reflected in your simulation test fixture. (Although you can rename the .TFI to .TF and add stimulus, you would then have to modify the file to include the updated declarations every time the circuit changed.)

For this design, the automatically-generated Verilog test fixture declarations are similar to the file shown below:

```
// SCH2TF 0.1 - Synario 2.7
// andff.tfi - 9/26/94 1:39:02 PM
// NOTE: Don’t edit this file.
// Auto generated everytime SCH2TF if run.
‘ ifdef use_proj_name
    ‘ define TOPNAME AND_FF
‘ else
    ‘ define TOPNAME andff
‘ endif
reg Clk, input_1, input_2;
wire output_q;
‘ ifdef post_map
wire cLK=Clk, INPUT_1=input_1, INPUT_2=input_2;
‘ TOPNAME d ( .clk(cLK), .input_1(INPUT_1), .input_2(INPUT_2),
.output_q(output_q));
‘ else
    ‘ ifdef map_upper_case
    ‘ TOPNAME d ( .CLK(Clk), .INPUT_1(input_1),
.INPUT_2(input_2), .OUTPUT_Q(output_q));
    ‘ else
    ‘ TOPNAME d ( .Clk(Clk), .input_1(input_1),
.input_2(input_2), .output_q(output_q));
    ‘ endif
‘ endif
‘ ifdef auto_init
    initial begin
        Clk = 0;
        input_1 = 0;
        input_2 = 0;
    end
‘ endif
‘ ifdef use_sdf
    initial begin
        $sdf_annotate("and_ff.sdf",t.d);
    end
‘ endif
```

This file contains a commented out module declaration that you can uncomment if you are going to use the file as a basis for your test fixture file. The module name of "t" is required if you use cross-probing in the Hierarchy Navigator.

After the top-level module declaration, one instance of the circuit andff is declared. (For cross-probing, the circuit to be tested must be instantiated in the test fixture with the name "d.")

Circuit Initialization Section

The .TFI file may also contain an optional section for circuit initialization. The initialization section is enclosed in Verilog **‘ ifdef** statement so that it can be included or excluded by defining a constant in the higher-level test fixture file just prior to the ‘ include statement.

Simulating the Design

You are now ready to simulate the design.

To simulate this design:

1. Highlight the test fixture file (andff.tf) in the *Sources in Project* window.
2. The *Processes for Current Source* window has a single process listed. Double-click on the Verilog Functional Simulation process.

   Synario builds the simulation model for the circuit, and then displays the Verilog Simulator.

Note: *To view system-related messages generated during the processing of the test fixture file, click the Log button below the Processes for Current Source window. Most errors during functional simulation are syntax errors in the test fixture file (such as signal case not being the same as on the schematic), which can be viewed by selecting Simulator Transcript from the Simulator Window menu. Scroll to the bottom of the report to view the latest messages.*

   In the Verilog Simulator, you can specify the duration of simulation, and the interval to be used for single-stepping during debugging. Set the simulation duration (the "To:" field) to 200 ns.

3. Click Run in the Verilog Simulator to run the simulation. (If the Run button is grayed out, either the simulator has not finished reading in the simulation model and test fixture file, or there was an error during Simulator startup.)

When you select Run, the Simulator applies the stimulus to the simulation model of the circuit and stores the results. The simulation is usually close to instantaneous.

4. To display the simulation results, select Waveform Viewer from the Simulator's Window menu.

   The Waveform Viewer initially displays no signals, so you must add the signals you wish to observe. Two ways to add signals to the Waveform Viewer are described below. Selecting signals from the Waveform Viewer menus is shown first; adding signals using the schematic source is shown later.

5. Select Show from the Waveform Viewer Edit menu. The Show dialog box appears.

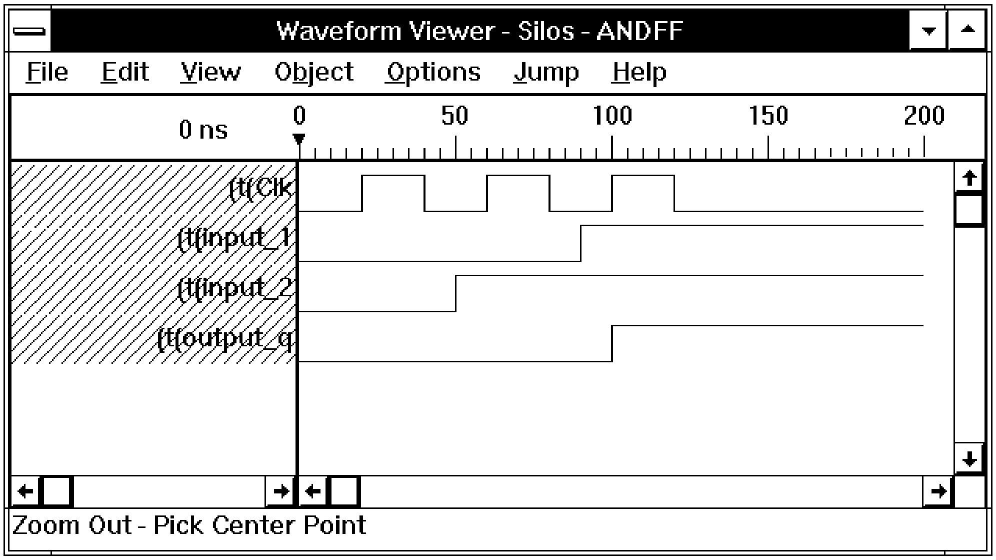
6. Double-click on the module "t" listed on the left side of the Show dialog box.

   a. Select one or more signals to display in the waveform. For this example, select signals input_1, input_2, Clk and output_q. You can select all four signals at once by holding the mouse button down and dragging over the four names.

   b. Click Add Wave to add the selected signals to the waveform display.

      When you add the signals, the Waveform Viewer displays a waveform like the one shown in Figure 2-8.

Figure 2-8
Waveform Viewer With Four Signals


Waveform Viewer - Silos - ANDFF
File Edit View Object Options Jump Help
0 ns
0
50
100
150
200
{t{Clk
{t{input_1
{t{input_2
{t{output_q
Zoom Out - Pick Center Point

Using the Zoom In Feature

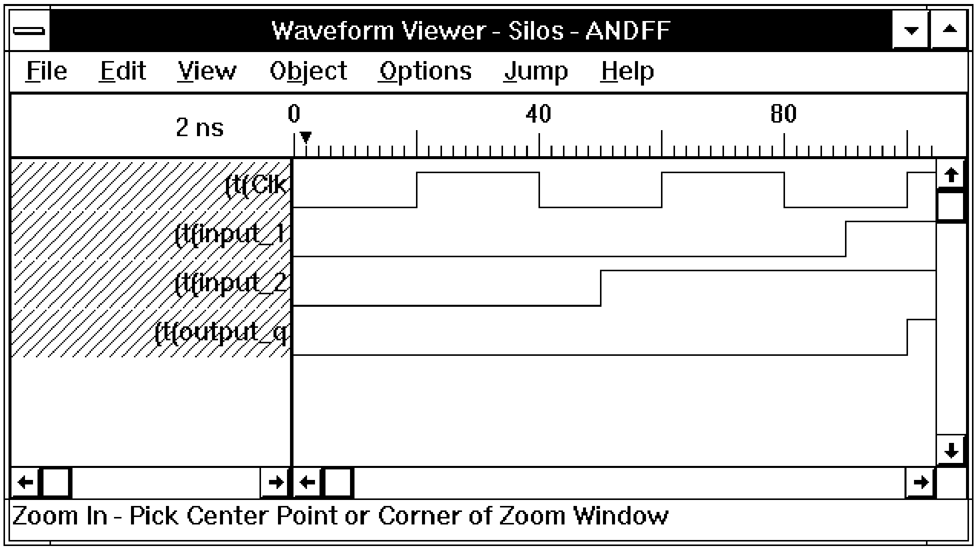
You can use the Waveform Viewer’s Zoom feature to view parts of the design in greater detail.

To zoom in with the Waveform Viewer:

1. Select Zoom In from the View menu.
2. Place the zoom cursor at the beginning of the waveform, hold the left mouse button down, and select a zoom region of about 150 ns. The Waveform Viewer zooms in on the selected waveform so you can see the circuit stimulus more clearly, as shown in Figure 2-9.
3. Press the right mouse button to exit zoom mode when you have zoomed in the desired amount.

   The waveform has the three inputs (input_1, input_2 and Clk) and the output (output_q).

Figure 2-9
Waveform Zoomed In


Waveform Viewer - Silos - ANDFF
File Edit View Object Options Jump Help
2 ns
0
40
80
(t(Clk
(t(input_1
(t(input_2
(t(output_q
Zoom In - Pick Center Point or Corner of Zoom Window

Viewing Simulation Results on a Schematic Source

You can also view simulation results directly on the schematic using the Hierarchy Navigator:

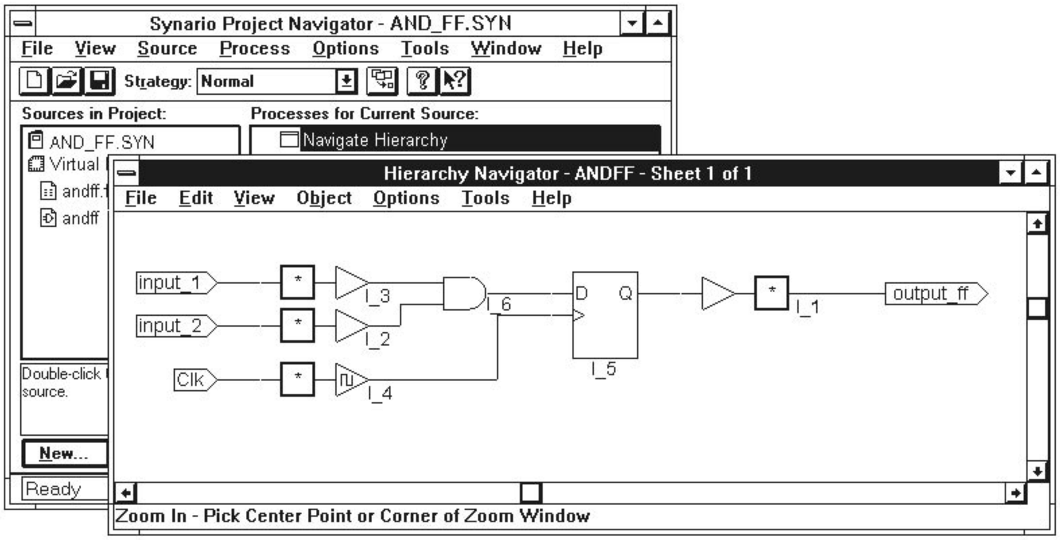
To view simulation results:

1. Leave the Simulator Waveform Viewer window up (do not minimize or close it; just click outside the window).
2. Go to the Synario Project Navigator, and highlight the schematic (andff.sch) in the *Sources in Project* window. (Do not double-click.)
3. In the *Processes for Current Source window, double-click on Navigate Hierarchy to run the Hierarchy Navigator. The Hierarchy Navigator displays the schematic, with the back-annotated simulation results shown directly on the schematic.*

Note: *The Hierarchy Navigator looks very similar to the Schematic Editor, but its function is different. You cannot edit the schematic in the Hierarchy Navigator.*

4. Choose Zoom In from the Hierarchy Navigator View menu, and zoom in until your display is similar to Figure 2-10 (the actual values displayed depend on the location of the waveform cursor in the Waveform Viewer).

Figure 2-10
Hierarchy Navigator


Synario Project Navigator - AND_FF.SYN
File View Source Process Options Tools Window Help
Sources in Project:
Processes for Current Source:
Navigate Hierarchy
AND_FF.SYN
Virtual
andff.t
andff
New...
Hierarchy Navigator - ANDFF - Sheet 1 of 1
File Edit View Object Options Tools Help
input_1
input_2
Clk
*
I_3
I_2
I_4
I_6
D
Q
I_5
I_1
output_ff

Strategy: Normal

Double-click
source.

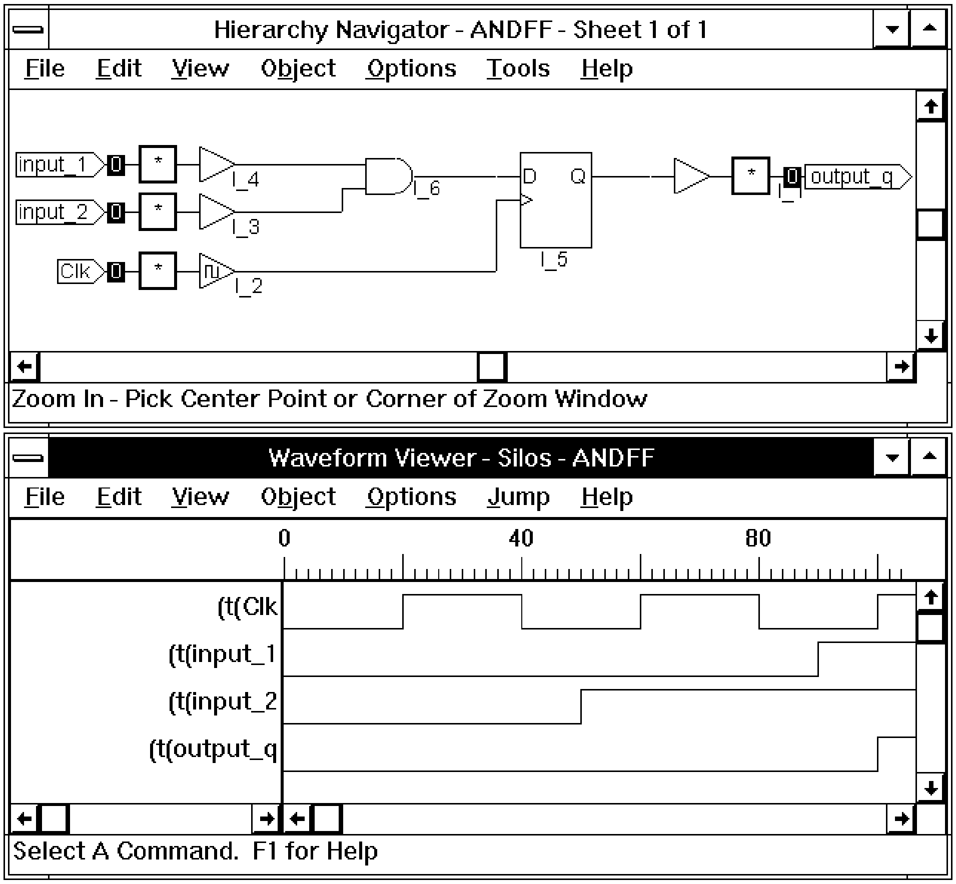
Ready

Zoom In - Pick Center Point or Corner of Zoom Window

5. To see how the Hierarchy Navigator and the Waveform Viewer communicate, arrange the two windows so that both are visible as shown in Figure 2-11.

6. Select various locations in the Waveform Viewer window. The values on the schematic change as you select different states of the simulation.

Figure 2-11
Waveform and Hierarchy Navigator Windows


Hierarchy Navigator - ANDFF - Sheet 1 of 1
File Edit View Object Options Tools Help
input_1
input_2
Clk
0
*
I_4
I_3
I_2
I_6
D
Q
I_5
I_
output_q
Waveform Viewer - Silos - ANDFF
File Edit View Object Options Jump Help
0
40
80
(t(Clk
(t(input_1
(t(input_2
(t(output_q

Zoom In - Pick Center Point or Corner of Zoom Window

Select A Command. F1 for Help

Adding an unnamed wire

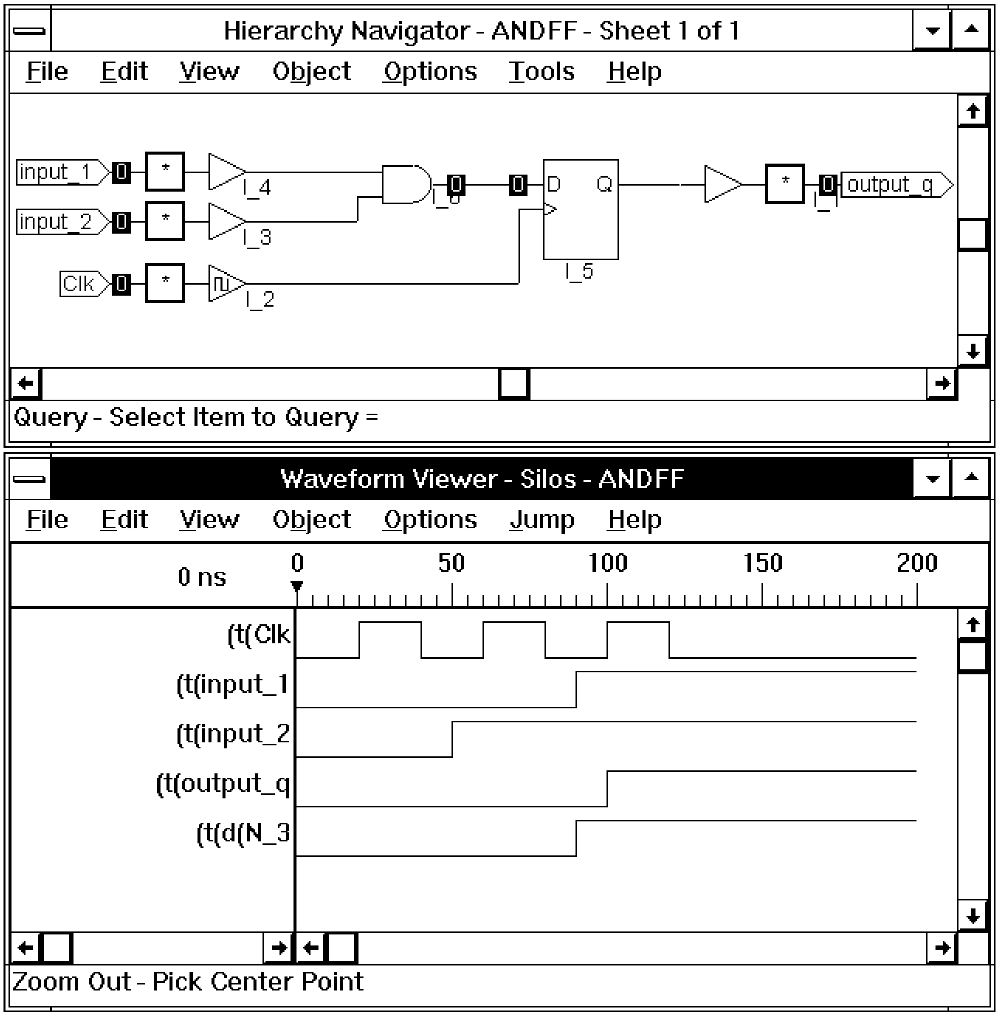
The Hierarchy Navigator can also be used to select wires (nets) for viewing during simulation. This is particularly useful if you are not sure of the name of a wire.

To add the unnamed wire to the simulation Waveform Viewer:

1. In the Hierarchy Navigator, select Probe Item from the Tools menu.
2. Place the cursor over the wire connecting the output of the AND gate with the D input of the flip-flop and press the left mouse button.

The wire is added to the Waveform Viewer, and the value of the wire appears on the schematic as shown in Figure 2-12.

Figure 2-12
Cross-probing for an Unnamed Wire



Hierarchy Navigator - ANDFF - Sheet 1 of 1

Query - Select Item to Query =

Waveform Viewer - Silos - ANDFF

Zoom Out - Pick Center Point

Tutorial 3
Using ABEL-HDL in Synario

This tutorial describes how to:

- Enter an ABEL-HDL design description.
- Process the ABEL-HDL design.
- Use properties and strategies.
- Simulate the ABEL-HDL design with Verilog test fixtures.
- Simulate the ABEL-HDL design with test vectors and the Simulate Equations process.

This tutorial uses the same circuit as Tutorial 2: a simple AND gate with a flip-flop. Instead of using a schematic for the design, this tutorial shows how to use ABEL-HDL to describe the circuit behaviorally.

Creating a new ABEL-HDL Source

Creating a new ABEL-HDL source in Synario entails the following basic steps:

- Setting up a new project
- Adding a new ABEL-HDL source to the project
- Describing the circuit using ABEL-HDL

These steps are detailed below.

Setting Up a New Project

Before you start entering a circuit, you need to start Synario and set up a new project.

To set up a new project:

1. Start Synario and select New Project from the File menu. Synario prompts you for the working directory for your new project.

2. Navigate to the location where you wish to create a new directory (for example, **\examples\tutorial**). Then, select Create Directory, and enter a name for a new project directory. (All projects should be kept in separate directories.)

   This tutorial refers to the **\and_ff2** directory. (You can use your own directory and substitute its name wherever the **\and_ff2** directory is indicated.)

3. Click OK to exit the Create Directory dialog box, then click OK to exit the New Project dialog box.

   Synario resets the selected device to the default (Virtual Device) and re-configures to the default state. (The first time you enter Synario, it is in the default state.)

4. Change the project name by double-clicking on the project Notebook ("Untitled") icon at the top of the *Sources in Project* window.

5. Enter the project name AND_FF2.SYN (In most cases, the project name does not have to have the same name as the directory you created), and click OK.

6. Save the project by selecting Save As from the File menu. Enter **and_ff2.syn** in the File Name text box.

7. Click OK to exit the Save Project As dialog box.

Adding a new ABEL-HDL source

Once you have a new project set up, you can add an ABEL-HDL source.

To add an ABEL-HDL source to the project:

1. Click the New button below the *Sources in Project* window.
   Synario prompts you for the type of source you wish to create.

2. Select ABEL-HDL Module from the list of source types, and click OK.
   The Text Editor runs, and a dialog box prompts you for a module name, filename, and title.

3. For the module name, type **andff**.

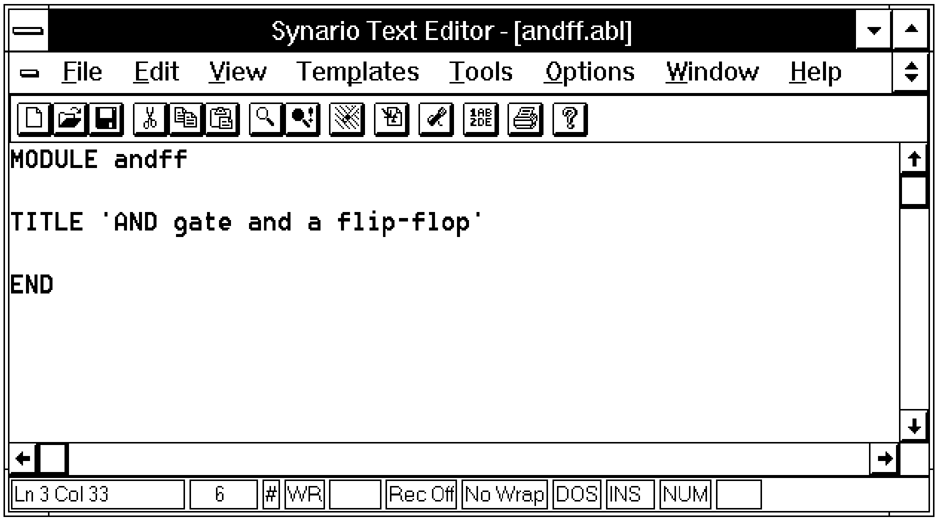
4. For the filename, type **andff**. (You do not need to type the file extension; Synario appends it automatically.)

5. If you like, type a descriptive title in the Title text box.

6. When you have finished entering the information, click OK (or press Enter).

The Text Editor now displays a template ABEL-HDL source file as shown in Figure 3-1.

Figure 3-1
Synario Text Editor with ABEL-HDL Template


Synario Text Editor - [andff.abl]
File Edit View Templates Tools Options Window Help
Ln 3 Col 33
6
#
WR
Rec Off
No Wrap
DOS
INS
NUM

```
MODULE andff

TITLE 'AND gate and a flip-flop'

END
```

Describing the circuit using ABEL-HDL

Now you need to describe the behavior of the design.

To describe the circuit:

1. Add declarations for the three inputs (the AND gate inputs and the clock) and the output by entering the following statements in the ABEL-HDL source file (after the TITLE statement, if there is one in the template file):

```
input_1, input_2, Clk      pin;
output_q                 pin istype ’reg’;
```

These two statements declare four signals (input_1, input_2, Clk, and output_q. These declarations are similar to the assignment of net names in the schematic that are entered in Tutorial 2.

Note: *ABEL-HDL does not have an explicit declaration for inputs and outputs; whether a given signal is an input or an output depends on how it is used in the design description that follows. The signal output_q is declared to be of type 'reg', which implies that it is a registered output pin. The actual behavior of output_q, however, is specified using one or more equations.*

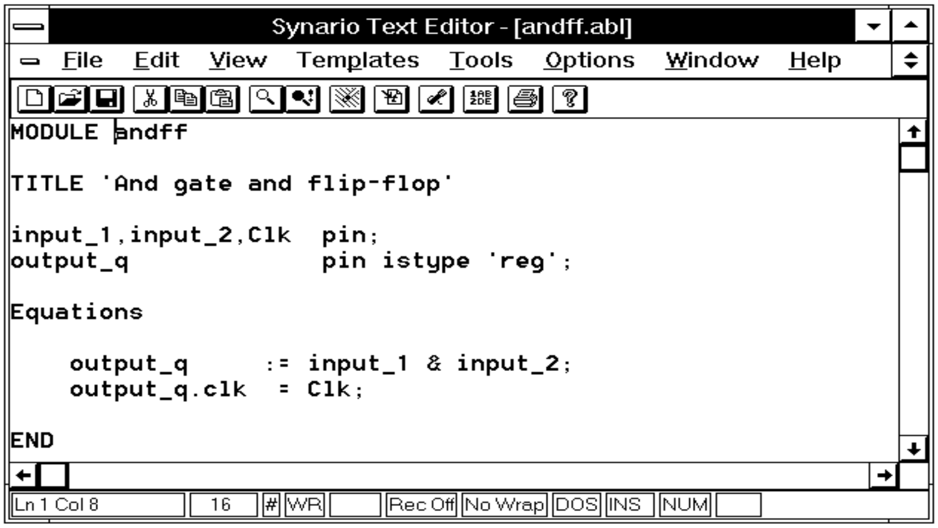
2. To describe the actual behavior of this circuit, enter two equations as follows:

   ```
   Equations

       output_q        := input_1 & input_2;
       output_q.clk    = Clk;
   ```

   These two equations define the data to be loaded on the registered output, and define the clocking function for the output: the same function as the schematic drawn in the previous example. Figure 3-2 shows the complete ABEL-HDL source file describing the circuit.

Figure 3-2
ABEL-HDL Source File for AND Gate and Flip-flop Circuit



```
MODULE andff

TITLE 'And gate and flip-flop'

input_1,input_2,Clk  pin;
output_q             pin istype 'reg';

Equations

    output_q     := input_1 & input_2;
    output_q.clk  = Clk;

END
```

Hint: *You can get help with ABEL-HDL language structure and syntax by selecting the Help menu or pressing F1 while working with an ABEL-HDL file in the Text Editor. For help on a particular ABEL-HDL keyword, highlight the word in the Text Editor and press F1.*

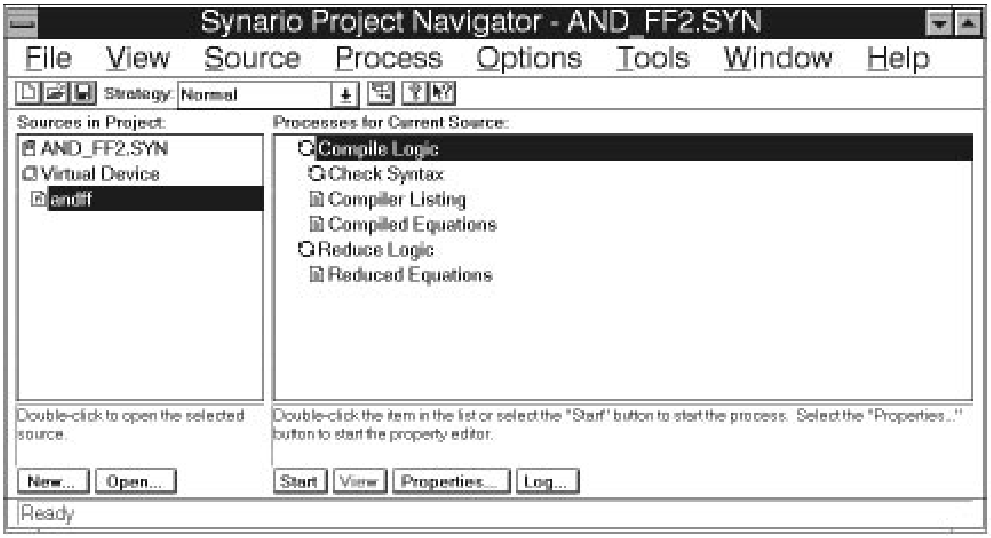
3. To save the ABEL-HDL source file and exit from the Text Editor, select Save and then Exit from the Text Editor's File menu.

   Synario updates the *Sources in Project* window to include the new ABEL-HDL source (notice the ABEL-HDL source icon) and also updates the *Processes for Current Source* window to reflect the steps necessary to process this source file.

Hint: *You can run the Text Editor with an ABEL-HDL source loaded by double-clicking on the source in the Sources in Project window.*

In the previous tutorial, Synario updated the *Sources in Project* and *Processes for Current Source* windows after you created the schematic. The difference this time is that the processes are different for ABEL-HDL sources. Figure 3-3 shows the *Processes for Current Source* window for this ABEL-HDL source file.

Figure 3-3
Process Window When an ABEL-HDL Source Is Selected



Double-click to open the selected source.

Double-click the item in the list or select the "Start" button to start the process. Select the "Properties..." button to start the property editor.

Keeping Track of Processes: Auto-update

There are more processes required for an ABEL-HDL source file than for a schematic because the ABEL-HDL source file requires compilation and optimization before a simulation model can be created. But because Synario knows what processes are required to generate a simulation model from an ABEL-HDL source, you can double-click on the end process you want (for example, Verilog Functional Simulation Model). Synario's auto-update feature automatically runs any processes required to complete the process you request.

Device-related processes such as mapping the selected ABEL-HDL source file to a JEDEC file or XNF file are available in the *Processes for Current Source* window when you select a device for this design.

Compiling an ABEL-HDL Source File

Synario's auto-update feature reprocesses sources as needed to accomplish the process you request, so you do not need to worry about when to recompile ABEL-HDL source files.

However, you can compile an individual source file by highlighting the file in the *Sources in Project* window and double-clicking on Compile Logic in the *Processes for Current Source* window. Alternatively, you can double-click on a report in the *Processes for Current Source* window, and compilation is run automatically.

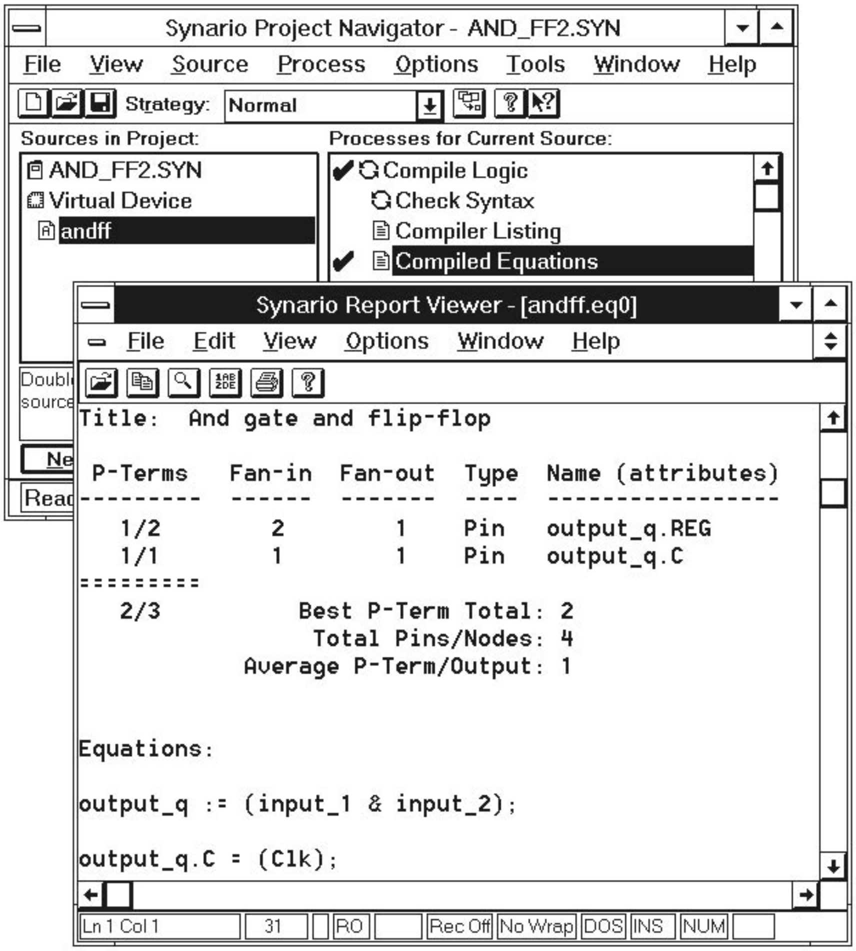
To compile an ABEL-HDL file and view the report:

1. Highlight the ABEL-HDL source file (andff.abl) in the *Sources in Project* window.
2. Double-click on Compiled Equations in the *Processes for Current Source* window.

   The source file is compiled and the resulting compiled equations are displayed in the Synario Report Viewer as shown in Figure 3-4. (If the ABEL-HDL file contained syntax errors, then the errors are displayed in a view window, and an error indication appears in the *Processes for Current Source* window.)

In this example, the compiled equations are identical to the equations that you entered into the ABEL-HDL source file. This is because the equations were simple Boolean equations that did not require any advanced synthesis in order to be processed.

Figure 3-4
Compiled Equations for AND Gate and Flip-flop


Synario Project Navigator - AND_FF2.SYN
File View Source Process Options Tools Window Help
Sources in Project:
AND_FF2.SYN
Virtual Device
andff
Processes for Current Source:
Compile Logic
Check Syntax
Compiler Listing
Compiled Equations
Doubl
source
Ne
Read
Synario Report Viewer - [andff.eq0]
File Edit View Options Window Help
Ln 1 Col 1
31
RO
Rec Off
No Wrap
DOS
INS
NUM

Strategy: Normal

```
Title:  And gate and flip-flop

 P-Terms   Fan-in  Fan-out  Type  Name (attributes)
---------  ------  -------  ----  -----------------
   1/2        2        1    Pin   output_q.REG
   1/1        1        1    Pin   output_q.C
=========
   2/3          Best P-Term Total: 2
                 Total Pins/Nodes: 4
             Average P-Term/Output: 1


Equations:

output_q := (input_1 & input_2);

output_q.C = (Clk);
```

Using Properties and Strategies

For many Synario processes (such as the compiling and optimizing steps seen above) there are processing options you can specify. These options include compiler options, such as custom arguments or processing changes, and optimization options, such as node collapsing. These options are specified using *properties*.

Properties

The properties available at any given time are dependent on

- The type of source file selected in the *Sources in Project* window (for example, ABEL-HDL, VHDL, schematic or test fixture)
- The process that is selected in the *Processes for Current Source* window
- The device selected for the project

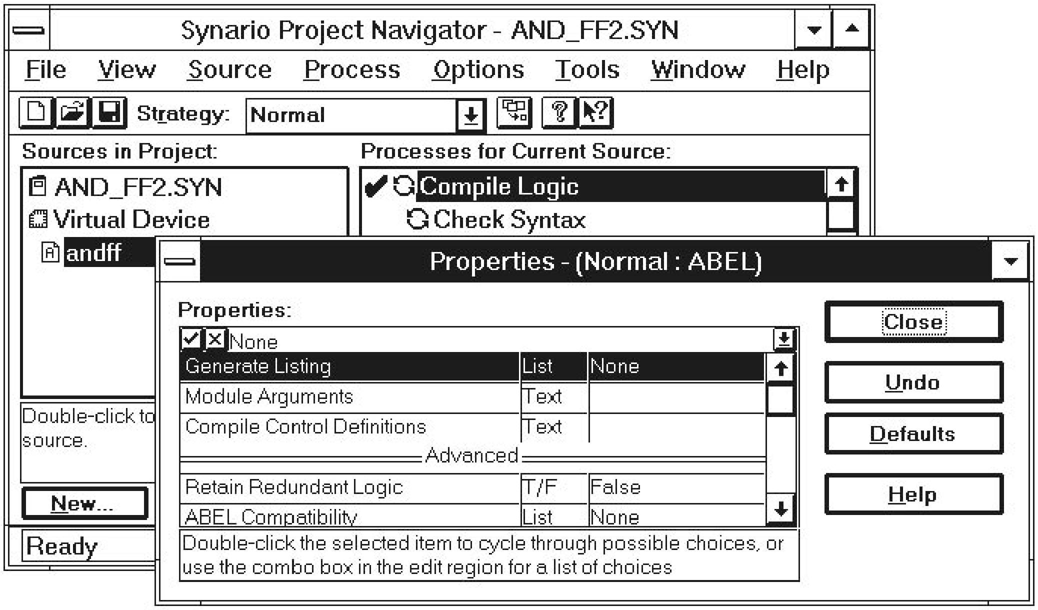
You can see how properties are set by changing the type of listing file that is generated for all ABEL-HDL sources in the current project.

To change properties:

1. Highlight the ABEL-HDL source file in the *Sources in Project* window (by clicking on the andff ABEL-HDL source).
2. Highlight (do not double-click) Compile Logic in the *Processes for Current Source* window.
3. Click the Properties button below the *Processes for Current Source* window.

   The Properties dialog box appears with a list of options, as shown in Figure 3-5. This list is specific to the Compile Logic process for ABEL-HDL sources.
4. In the Properties dialog box, select the Generate Listing property.
5. Click on the arrow to the right of the text box (at the top of the properties menu), and select Expanded.
6. Click on the Close button to exit the Properties dialog box.

Figure 3-5
Properties for Compile Logic Process



Strategy: Normal

Properties:

☑ ☒ None

Generate Listing	List	None
Module Arguments	Text	
Compile Control Definitions	Text	
Advanced		
Retain Redundant Logic	T/F	False
ABEL Compatibility	List	None

Double-click the selected item to cycle through possible choices, or use the combo box in the edit region for a list of choices

Strategies

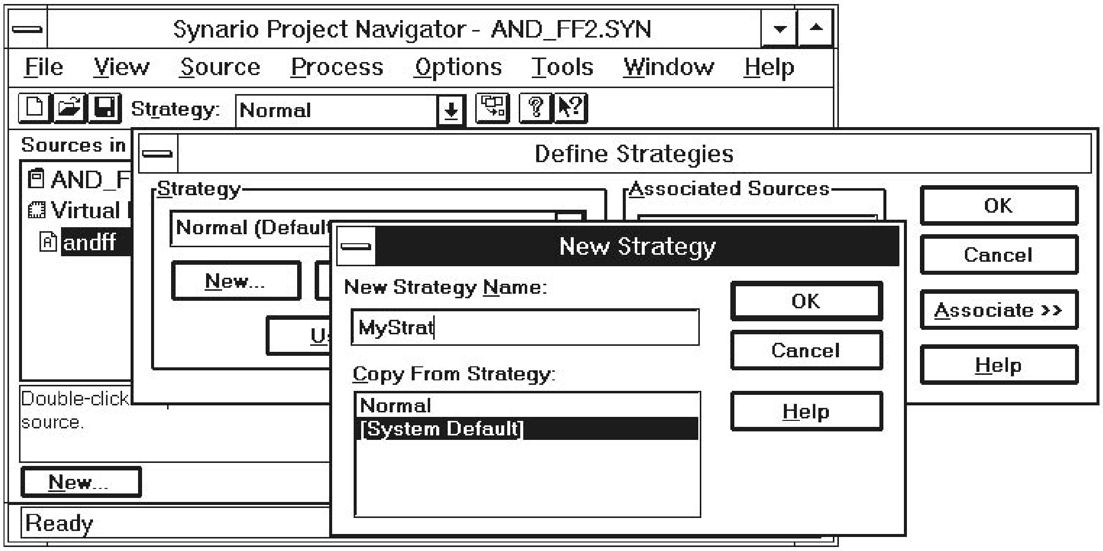
Another way to set options in your project is to use *strategies*. A strategy is a set of properties (processing options) that you have specified for some or all of the sources in your project. Strategies can be useful if you have processing requirements that change depending on factors such as the size and speed tradeoffs in synthesis, or whether the design is being processed for simulation or for final implementation.

With strategies, you do not have to modify the properties for every source in the design to change the processing options. Strategies allow you to set up the properties once, then associate the strategy with the sources you want the properties applied to. You can create new strategies that reflect different properties for the entire project, and then associate one or more custom strategies with the sources in your project.

To see how strategies work:

1. Select Strategy from the Source menu.
2. In the Define Strategies dialog box, click New to create and name a new strategy, as shown in Figure 3-6.

Figure 3-6
Creating and Naming a New Strategy



Strategy: Normal

Strategy: Normal (Default

New Strategy Name: MyStrat

Copy From Strategy:
Normal
[System Default]

3. Enter a name for the strategy, and click OK. The new strategy appears in the Strategy drop-down list box.

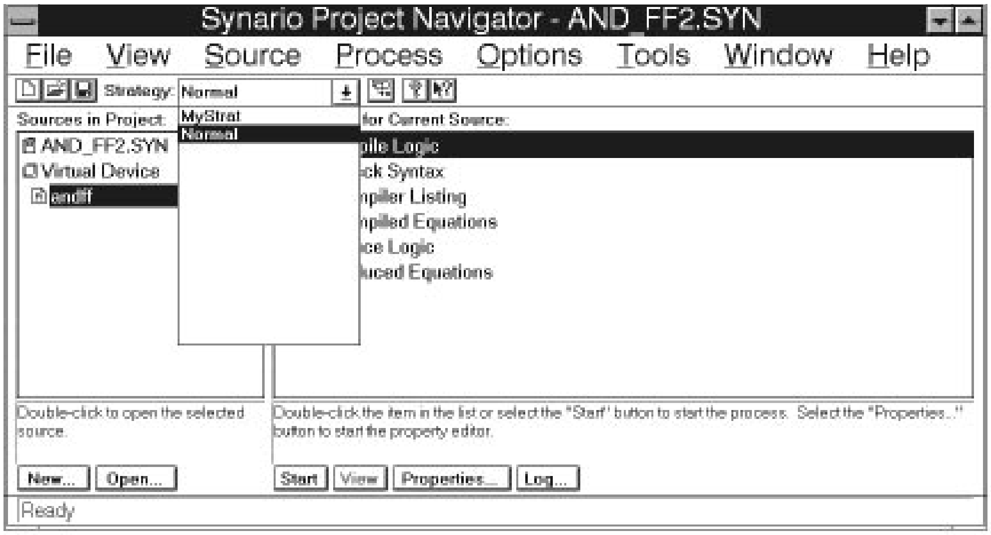
To associate a source with a new strategy:

1. Click the Associate button in the Define Strategies dialog box.
2. Highlight the ABEL-HDL source (andff) in the Source to Associate with Strategy list box.
3. Click the Associate with Strategy button.

   The andff source appears in the Associated Sources list box.

Hint: *A shortcut for associating a source with a strategy is to do so from the Project Navigator. Highlight a source and use the Strategy drop-down list box to associate an existing strategy with the selected source. This is shown in Figure 3-7.*

Figure 3-7
Associating a Strategy With a Source



Synario Project Navigator - AND_FF2.SYN

Strategy: Normal

Double-click to open the selected source.

Double-click the item in the list or select the "Start" button to start the process. Select the "Properties..." button to start the property editor.

Ready

Simulating the Design

Since no device is specified for this project (the device is Virtual Device), simulation will be functional simulation of the design rather than a timing simulation of the whole circuit. Synario supports the following methods of simulation:

- Verilog
- Equations
- JEDEC

Verilog and Equations simulation are discussed below.

Performing Verilog Simulation

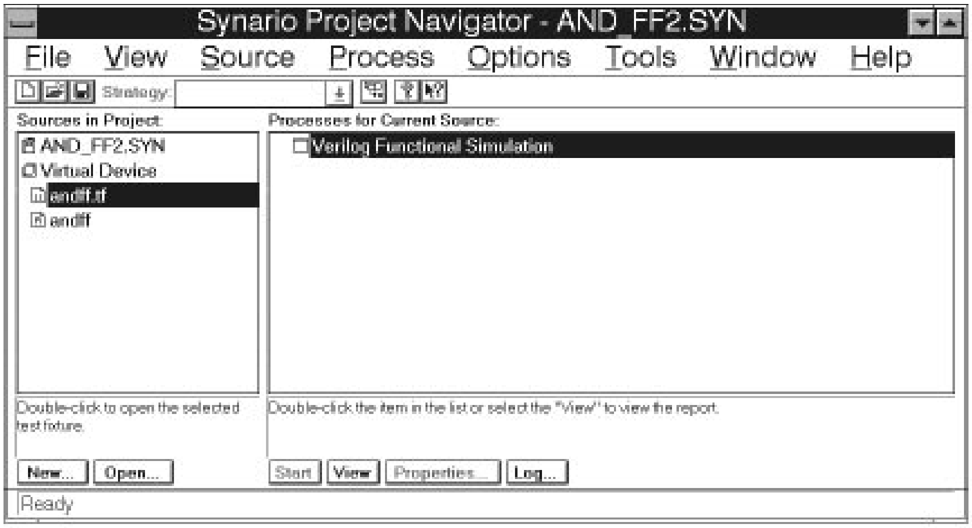
Performing a Verilog simulation of this version of the design is, in most respects, the same as simulating the schematic version of the design created in the previous tutorial. The major difference is that when you enter a design (or portion of a design) using ABEL-HDL, you cannot cross-probe from the simulation Waveform Viewer to the original ABEL-HDL source file.

To import the test fixture:

1. Use the Windows File Manager to copy the test fixture file from the previous tutorial (andff.tf) from the **\and_ff** directory to the **\and_ff2** directory. You can now import the test fixture and use it for this project.
2. Select Import from the Source menu.
3. Select the file **andff.tf** and click OK.
4. Synario prompts you for whether the test fixture file should be associated with the Virtual Device source or with the **andff** source.
5. Choose Virtual Device, and click OK.

   The test fixture file is included in the *Sources in Project* window, as shown in Figure 3-8.

Figure 3-8
Project with ABEL-HDL and Test Stimulus Source


Synario Project Navigator - AND_FF2.SYN
File View Source Process Options Tools Window Help
Strategy:
Sources in Project:
AND_FF2.SYN
Virtual Device
andff.tf
andff
Processes for Current Source:
Verilog Functional Simulation
New...
Open...
Start
View
Properties...
Log...
Ready

Double-click to open the selected test fixture.

Double-click the item in the list or select the "View" to view the report.

To simulate the project:

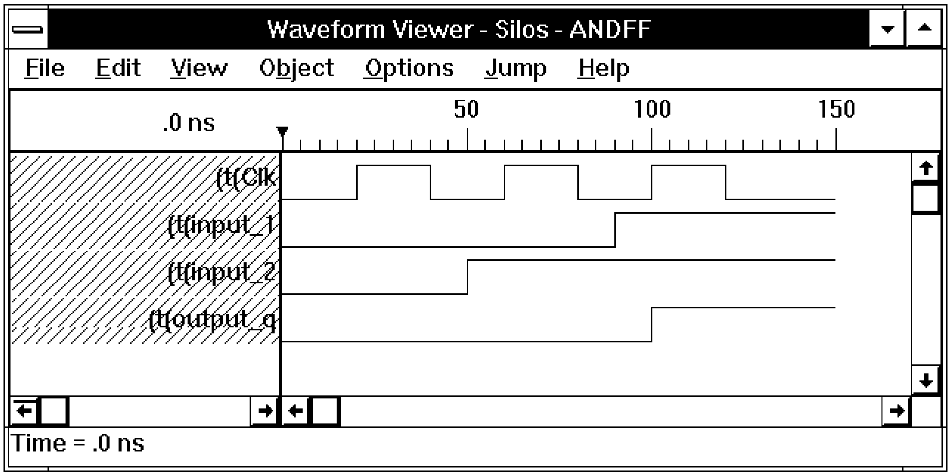
1. Highlight the test fixture file (andff.tf) in the *Sources in Project* window.
2. In the *Processes for Current Source* window, double-click on Verilog Functional Simulation (the only process listed) to start the Verilog Simulator.

   Synario does the following:

   - Builds a simulation model for the circuit. If necessary, Synario recompiles the ABEL-HDL source file, runs the optimizer, and then generates the simulation model from the optimized logic.
   - Opens the Simulator Control Panel.
   - Regenerates the test fixture declarations file (andff.tfi) referenced in your test fixture file.
3. Set the To field to 150 ns before running the Simulator.
4. Select Run to start the simulation.
5. Select Waveform Viewer from the Simulator Window menu to display the simulation results.
6. Select Show from the Edit window and use the cursor to select the signals to display in the waveform.

The Waveform Viewer displays a waveform similar to the one displayed in the previous tutorial. The waveform is shown in Figure 3-9.

Figure 3-9
Post-route Simulation



Using the Simulate Equations Process

Another method for testing ABEL-HDL designs is to use Simulate Equations process. To use this process, you must create test vectors for the ABEL-HDL source.

Test vectors are sets of input stimulus values and corresponding expected outputs that can be used with both Equation and JEDEC simulators. Test vectors can be specified in two ways:

- in the ABEL-HDL source
- in an external Test Vector file (ABV).

When you specify the test vectors in the ABEL-HDL source, the system creates a "dummy" vector file that points to the ABEL-HDL source containing the vectors. This file is necessary because a test vector file is required in order to have access to the Equation and JEDEC simulation processes.

To Add test vectors to the source file:

1. Double-click on the ABEL-HDL source (andff.abl) in the *Sources in Project* window.

   The Text Editor runs with andff.abl loaded.

2. Before the END statement, add the test vectors, as shown below:

```
Test_vectors
([Clk, input_1 , input_2] -> output_q)
 [ 0 ,    0    ,   0    ] ->    0;
 [.C.,    0    ,   0    ] ->    0;
 [.C.,    0    ,   1    ] ->    0;
 [.C.,    1    ,   1    ] ->    1;
```

3. Select Save and then Exit from the Text Editor's File menu to save the source file and exit from the Text Editor.

   Synario updates the *Sources in Project* window by adding the test vector file, andff-vectors, to the project.

You can now simulate the design, using the test vectors.

To simulate the design:

1. Highlight the test vector file (andff-vectors) in the *Sources in Project* window.
2. Double-click on the Simulate Equations process in the Process window.

   The Project Navigator builds all of the files needed to simulate the circuit and then runs the Equation Simulator.

To display the simulation results:

1. Double-click on the Equation Simulation Report process to display the simulation report file for **and_ff2**. The simulation report file is shown below.

```
Simulate ABEL 6.00  Date Tue Jun  28 14:36:01 1994
Fuse file: ’and_ff2.bl2’  Vector file: ’andff.tmv’ Part: ’Pla’
AND gate and a flip-flop

            o
       i i  u
       n n  t
       p p  p
       u u  u
     C t t  t
     l _ _  _
     k 1 2  q


V0001  0 0 0   L
V0002  C 0 0   L
       C 0 0   L
V0003  C 0 1   L
       C 0 1   L
       C 0 1   L
V0004  C 1 1   L
       C 1 1   H
       C 1 1   H

4 out of 4 vectors passed.
```

2. Select Equation Simulation Waveform to enter the Waveform Viewer and display the simulation waveforms.

   The Waveform Viewer initially displays no signals, so you must add the signals you wish to observe by selecting signals from the Waveform Viewer menus.

   Select signals, using Show from the Edit menu, in the following manner:

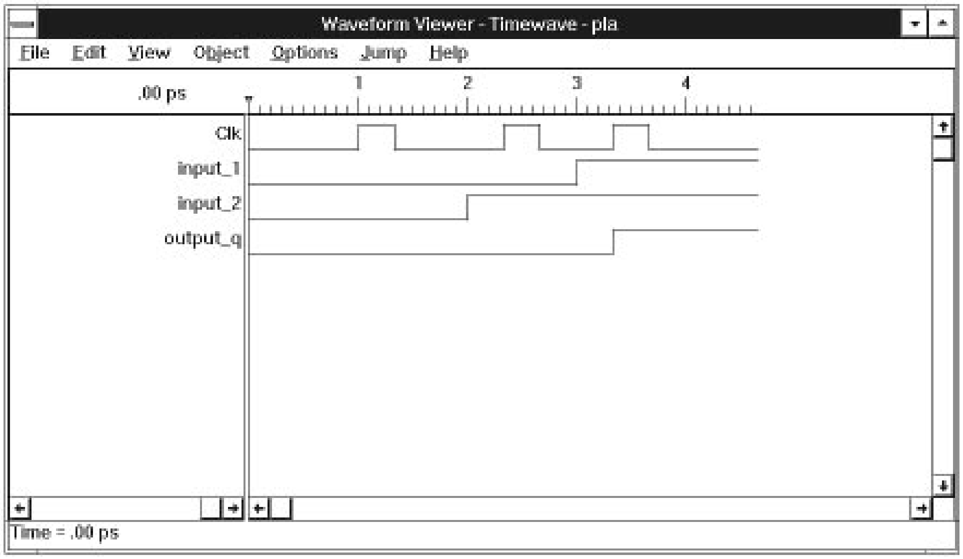
   a. Select Show from the Waveform Viewer Edit menu.

   b. Select one or more signals to display in the waveform. For our example, select signals input_1, input_2, Clk, and output_q. You can select all four signals at once by holding the left mouse button down and dragging over the four names.

   c. Click Add Wave to add the selected signals to the waveform display.

When you add the signals, the Waveform Viewer displays a waveform like the one shown in Figure 3-10.

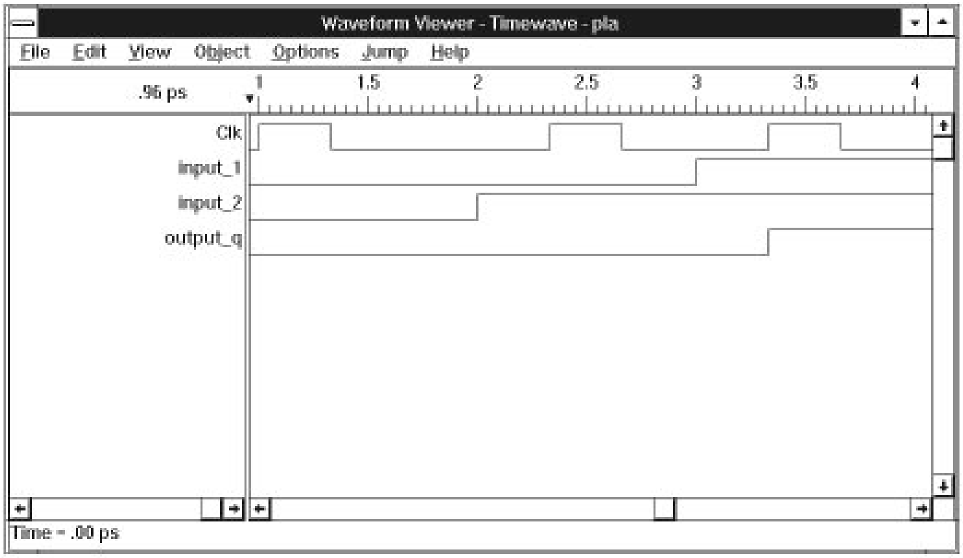
Figure 3-10
Waveform Viewer



To use Zoom In in the Waveform Viewer:

1. Select Zoom In from the View menu.
2. Place the zoom cursor at the beginning of the waveform, hold down the left mouse button and select a zoom region of about 150 ns. The Waveform Viewer zooms in on the selected waveform so you can see the circuit stimulus more clearly, as shown in Figure 3-11.

Figure 3-11
Zoom In in the Waveform Viewer



3. Press the right mouse button to exit zoom mode when you have zoomed in the desired amount.

   The waveform has the three inputs (input_1, input_2, and Clk) and the output (output_q).