PRELIMINARY

iAPX 43204 iAPX 43205
FAULT TOLERANT
BUS INTERFACE AND MEMORY CONTROL UNITS

- **Software Transparent Detection And Recovery From Any Single Point Failure**
- **Supports Up To 31 Processors For A Large Performance Range**
- **Configure From 1 To 8 Buses For High Bandwidth And Fault Tolerance**
- **Single, Dual, and Quad Redundant Configurations Tailor System Designs to Meet A Spectrum of Fault Tolerance And Cost Objectives**
- **VLSI System Simplifies Design With Low TTL Count**
- **Dynamic RAM Refresh with Error Correction and Scrubbing**

The 43204 Bus Interface Unit (BIU) and 43205 Memory Control Unit (MCU) are two VLSI devices that support the construction of fault tolerant, multiple processor 432 systems. Together they support: multiprocessor arbitration, dynamic RAM control, and ECC with a minimal amount of TTL. Fault tolerant systems can be built that tolerate the failure of any single component or bus. The BIU and MCU detect the failure and automatically switch to a redundant processor, bus, or memory. Hardware failures are completely masked from application software.

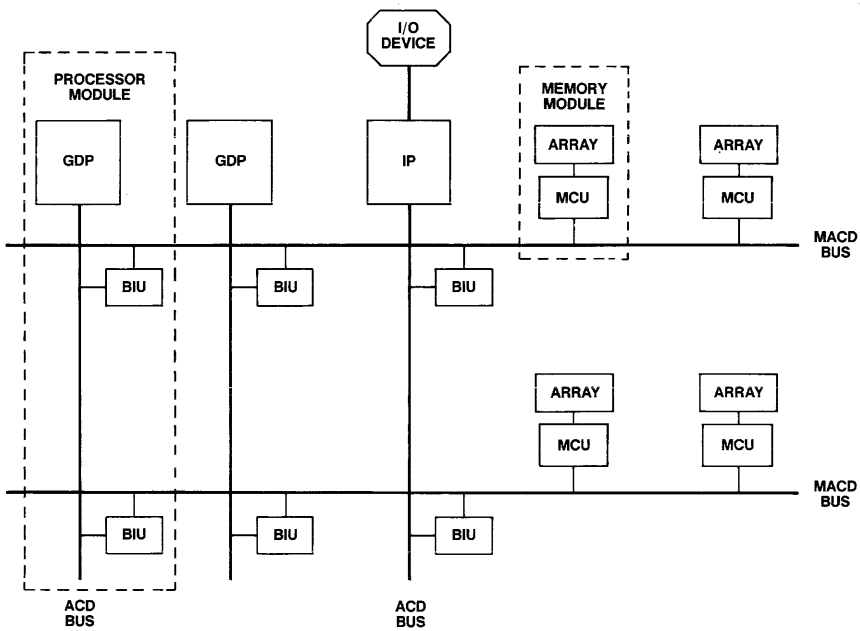

Figure 1. A 2 Bus System with 2 General Data Processors and 1 I/O Subsystem.

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INTRODUCTION

The first phase of the iAPX 432 program introduced two processor types: the General Data Processor (GDP) and the Interface Processor (IP). The GDP was implemented with two VLSI components: iAPX 43201 and iAPX 43202. The IP was implemented as a single VLSI component: the iAPX 43203. These three VLSI components implement the *processor architecture* for the iAPX 432. System builders have constructed multiple processor systems by surrounding the VLSI processors with discrete logic, which provided the interface to shared memory and the interprocessor communication paths. The method for interconnecting iAPX 432 processors and memories was unique for each system, since no standard had been defined.

This data sheet describes a pair of VLSI components: the iAPX 43204 Bus Interface Unit (BIU) and the iAPX 43205 Memory Control Unit (MCU) that form a unifying *interconnect architecture* for building iAPX 432 systems. Together, these components form the basis for constructing multiple-processor fault-tolerant iAPX 432 systems.

The iAPX 432 together with the BIU/MCU interconnect architecture provide:

- *Integrated fault tolerance.* The VLSI interconnect components (BIU/MCU) integrate all the detection and recovery logic required to build a system that can tolerate any single component failure.
- *Software transparent fault tolerance.* Hardware performs all fault detection and recovery functions transparent to application software. The architecture never dies.
- *Configurability.* The BIU and MCU support a range of fault tolerance and performance options to meet a diverse set of cost, performance, and reliability needs.
- *Standard VLSI solution.* Very little external logic is required.
- *Reliable software.* The iAPX 432 system's "need to know" (capability) addressing confines errors, protecting the system from errant software.

The object-based architecture of the iAPX 432 provides a robust and flexible environment for cooperating, concurrent software systems. The iAPX 432 processors use a cooperating, self-dispatching mechanism to automatically share the workload between the available processors. The number of processors available in the system is transparent to software.

The BIU and the MCU extend the logical flexibility and robustness of the iAPX 432 processors into the physical implementation of iAPX 432 systems. The BIU and MCU allow the iAPX 432 hardware to modularly and transparently extend the processing power (from 1 to 63 modules of processors or memories), bus bandwidth (1 to 8 backplane buses), and fault-tolerant capabilities of the system. Figure 1 shows an example of a two bus three processor (2 GDPs + 1 IP) system.

As Figure 2 shows, an iAPX 432 system based on the interconnect architecture may be expanded gracefully. A system with one processor and one memory may be built with a single memory bus. Transparent multiprocessing may be achieved by simply adding processor modules. When additional memory is required, memory modules may be added onto the single memory bus. When more memory bandwidth is required, an additional memory bus(es) can be added. None of these alternative systems require any change to application software.

In an iAPX 432 system, each processor is unaware of the manner in which the memory address space is actually implemented. Hardware located in the BIUs determines how processor addresses are mapped to buses and memory systems.

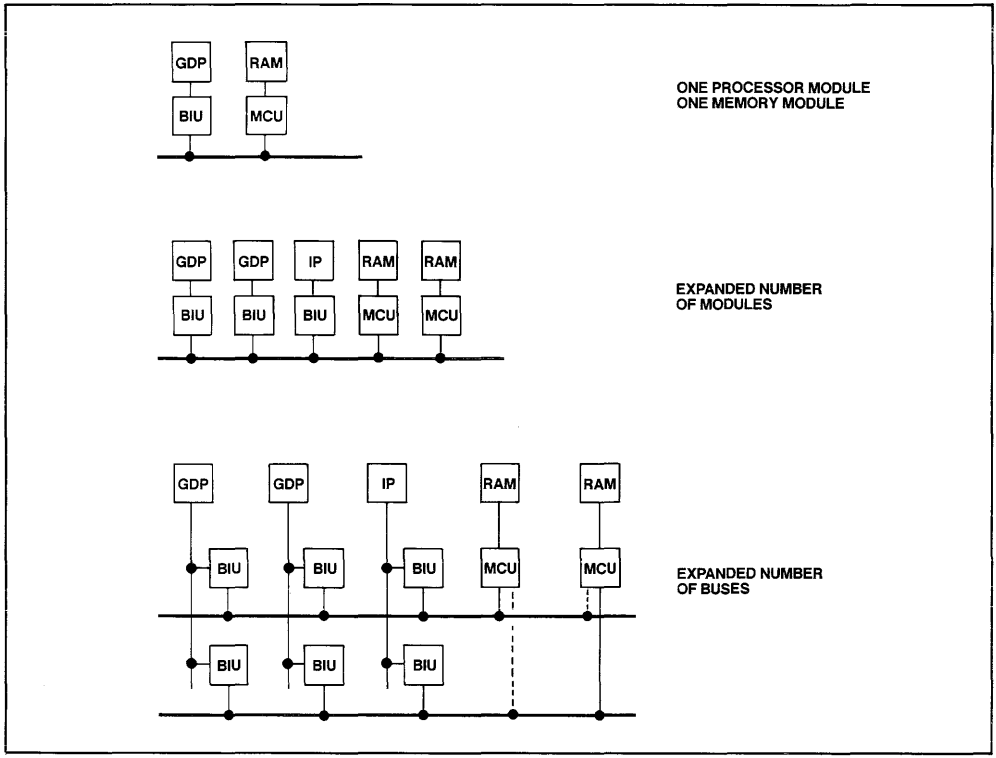


Figure 2. Modular Expansion

BUS INTERFACE UNIT

The Bus Interface Unit or BIU provides the switching function of the IAPX 432 interconnect system. That is, it accepts access requests from an iAPX 432 processor and, based on the physical address, it decides which memory bus(es) will be used to perform the access. The BIU is also responsible for arbitrating the usage of the memory bus. Finally, the BIU is responsible for propagating error information throughout the sytem.

MEMORY CONTROL UNIT

The Memory Control Unit or MCU interfaces memory storage arrays to the memory bus. The storage arrays will typically be constructed with high-density dynamic RAM (DRAM) components. All types of DRAMs are supported: 16K, 64K, 256K, even partially good components. The MCU manages the storage array as a logical collection of 32 data bits, 7 bits of error correcting code (ECC), and an optional spare bit. The MCU can automatically *refresh* the dynamic storage array. In addition, the MCU can *scrub* single-bit errors from the storage array as a background task. Scrubbing is accomplished by periodically reading the storage array, correcting all single-bit errors, and detecting and reporting all double-bit errors. The MCU accepts variable length data requests from the memory bus and performs the necessary access sequencing to read or write the data into the storage array. A modest amount of external logic is required to interface the MCU to the storage array RAMs — for simple configurations, as few as 12 external TTL packages are required.

MEMORY BUS

The memory bus (sometimes referred to as the MACD bus) provides the principal communication path, carrying all memory access requests and interprocessor communication. The memory bus connects BIUs to MCUs. Each node in the interconnect system tracks each operation on the memory bus to which it is attached. Thus, unlike most bus protocols, each BIU and MCU keeps track of all outstanding requests on the bus — not just the ones made by the BIU or MCU itself. Control for the bus in fully distributed; there is no centralized bus controller.

INTEGRATED FAULT TOLERANCE

BIUs and MCUs also form the basis for building *fault-tolerant* iAPX 432 systems. *Functional Redundancy Checking (FRC)* provides the low-level hardware support on which hardware fault-tolerant modules are constructed. In Figure 3, notice that a redundant processor module is formed by *replication* of the VLSI GDP and BIUs. A redundant memory module is formed by duplicating the VLSI MCU. The unshaded GDPs, BIUs, and MCUs act as *masters*. The shaded components act as *checkers*, which observe their master and report any disagreement they detect in the values the master produced.

When any error occurs, a special *error reporting network* notifies all nodes in the system of the discrepancy. Figure 4 illustrates the flow of error information in the interconnect system. In phase 1, an error is detected at a node in the interconnect system. The example illustrates an error detected at BIU(2,1); i.e., the BIU on memory bus 2 in processor

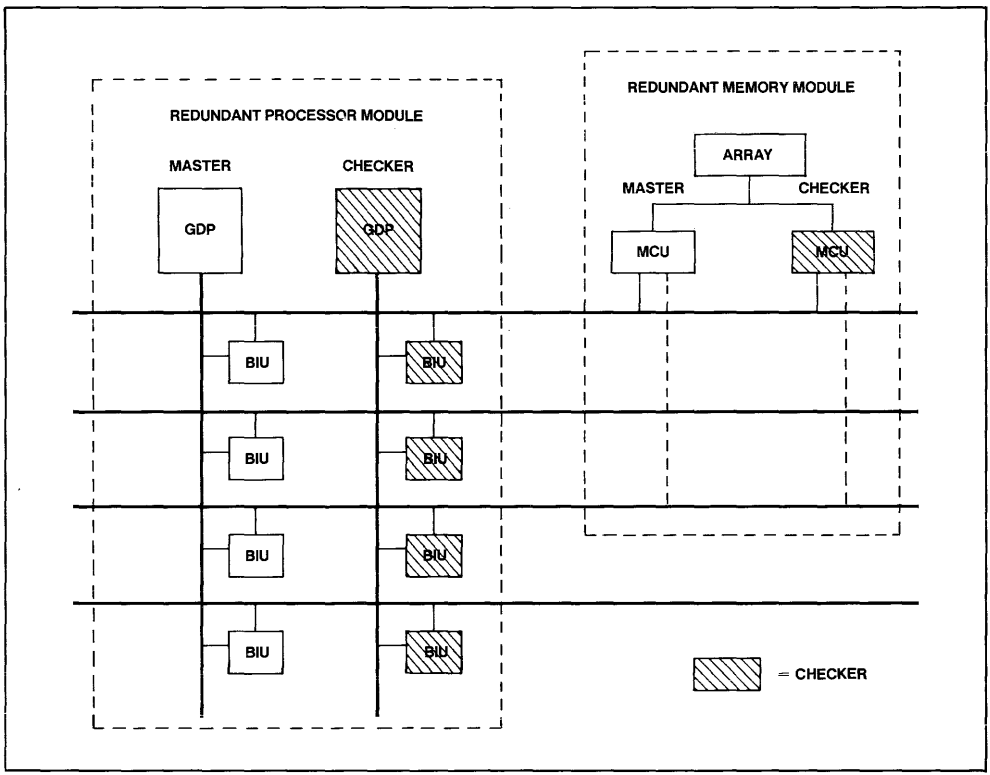


Figure 3. FRC Configuration Pairing

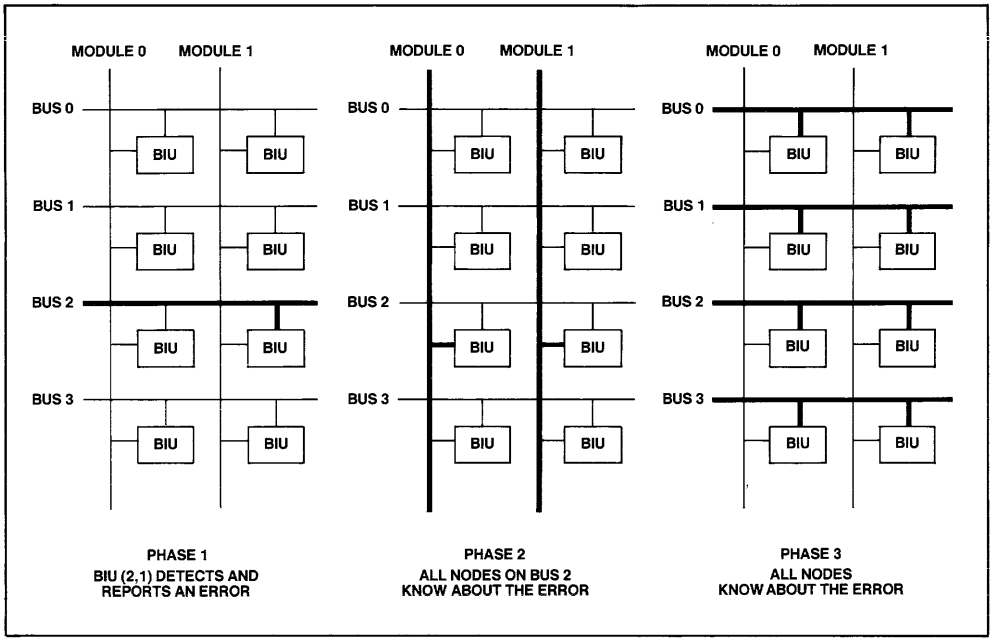


Figure 4. Three Phase Error Reporting Mechanism

module 1. The detecting component reports the error to all components attached to the same bus (a bold line indicates an active error reporting path). At this point, if all error reporting nodes are intact, all nodes have received the error message. In phase 2, all components that received the phase 1 error message *rebroadcast* the message along their module paths. Finally, in phase 3, each component that has received an error message rebroadcasts the message along its bus path. This second rebroadcast ensures that all nodes receive the error message even if a single module or bus error report line has failed. At the end of phase 3, all interconnect components in the system have been informed of the error. The actual error reporting paths are separate from, but run parallel to, the MACD and ACD busses so that error reports may propagate even if a bus is inoperative. In addition, the reporting paths may be duplicated to remove any single-point dependency in delivering an error report.

RECOVERY

The recovery process begins after an error report message has been broadcast around the system. Recovery is a distributed operation — each node in the system reads the error report message and decides what recovery actions need to be taken.

For recovery to be successful, there must be redundant resources available in the system. There are three redundancy mechanisms in the BIU and MCU: *bus retry buffers, ECC, and module shadowing.* The first two are useful in recovering from transient errors, while module shadowing allows recovery from permanent errors.

Figure 5 illustrates how every module in the system may be paired with another self-checking module of the same type. This pair of self-checking modules operates in lock step and provides a complete and current backup for all state information in the module. This mechanism is known as *module shadowing* because a shadow is ready to fill in if the primary fails, or vice versa. Fault detection and recovery is performed totally transparent to both application and system software. When the recovery is complete, system software is notified that a failure occurred. Figure 6 shows sample module failures and automatic hardware recovery.

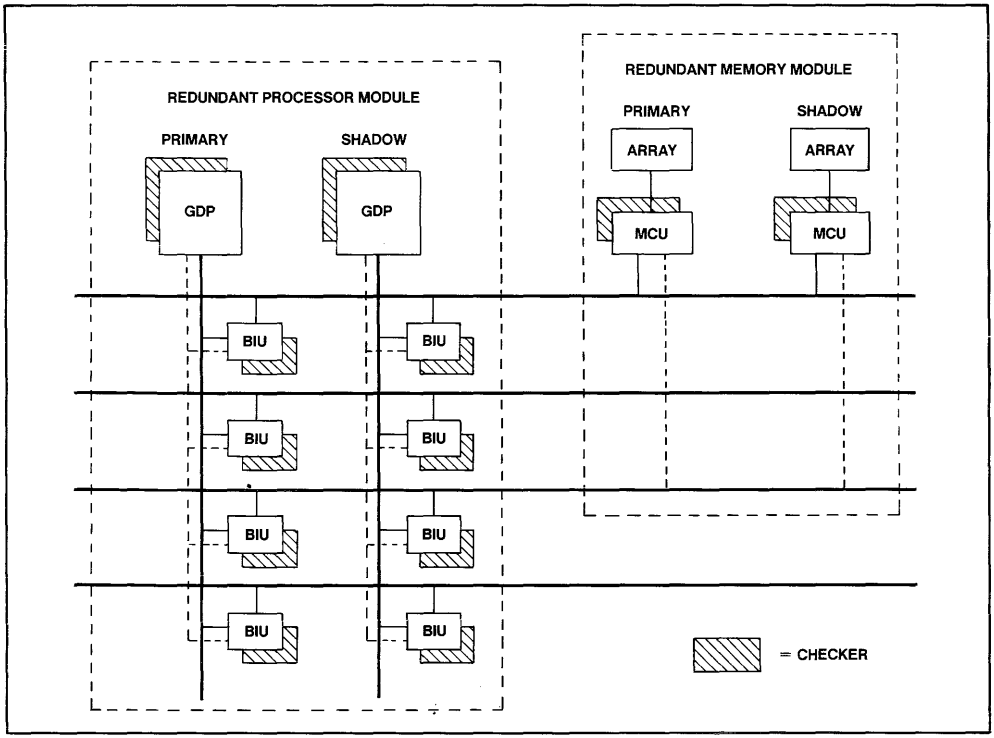


Figure 5. QMR Configuration Pairing

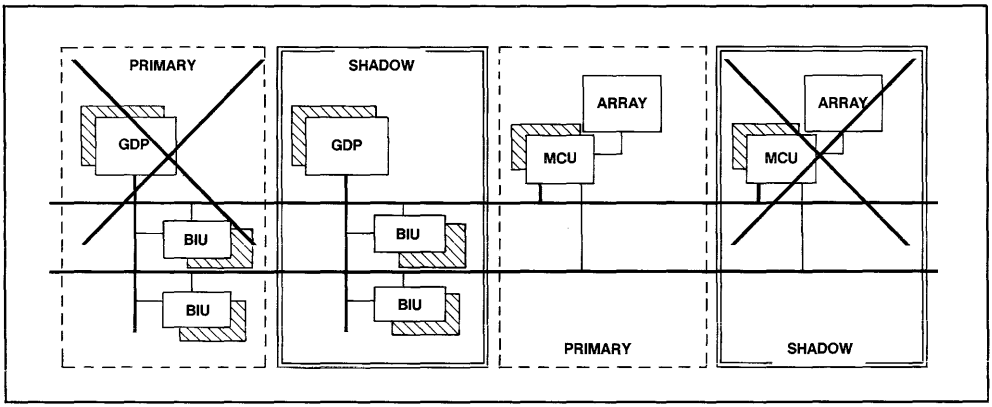


Figure 6A. Module Failures Are Detected

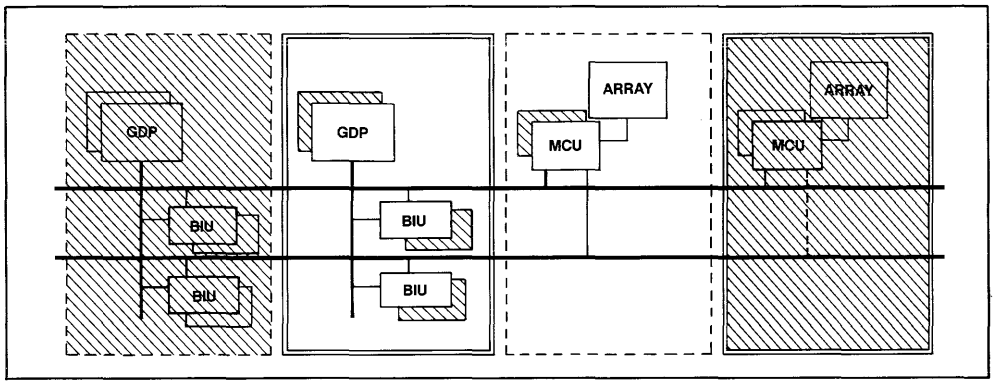


Figure 6B. Failed Modules Are Disabled

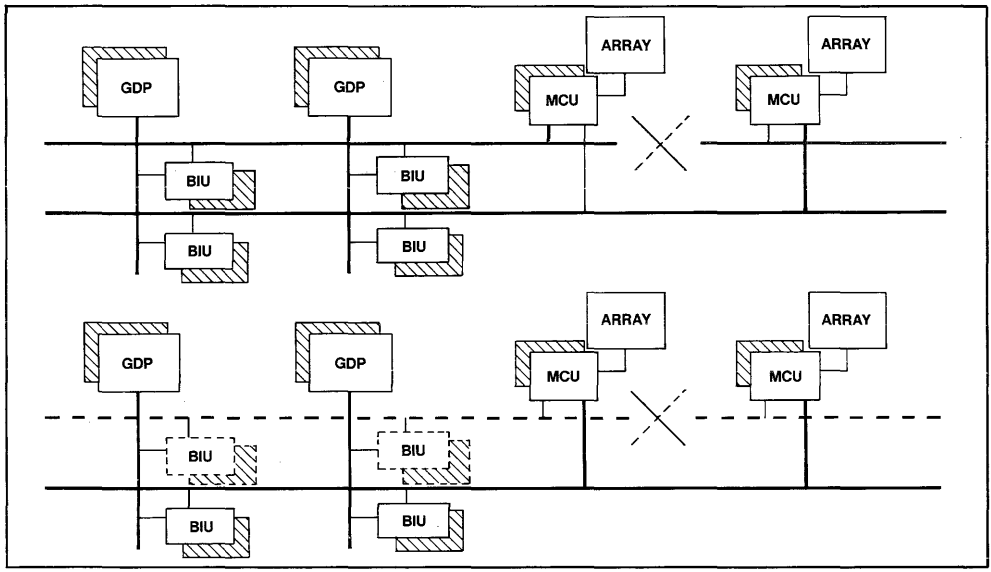


Figure 7. Bus Reconfiguration

A fault-tolerant module is also called a QMR module (Quad Modular Redundant) because most components (except memory) are replicated four times. There are two self-checking modules and each of these has a master and a checker.

Each memory bus in the system may be paired with another memory bus. Memory modules are physically connected to both buses although logically they are attached to only one bus at a time. During normal operation the buses run independently. Both contribute to the total memory bandwidth available in the system. If a bus fails, the memory modules attached to that bus will automatically switch to the other bus which is still operating. Figure 7 illustrates how the BIU and MCU reconfigure the system when a bus fails.

CONFIGURABLE FAULT TOLERANCE

Figure 8 illustrates the range of alternatives available to system designers when they build iAPX 432 systems. The most fault-tolerant systems are built from a QMR configuration of processors that can tolerate any single component failure without crashing the system. BIUs and MCUs provide full hardware error detection and recovery transparent to software.

The lowest cost configurations can be built using basic processor modules without FRC or QMR. This type of configuration will crash if a component fails, but can be made "self-healing" by adding intelligent software to the I/O subsystem. Unlike QMR, self-healing does not protect against system crashes, but it does allow the system to recover from a failure in a short period of time. The "healing" takes place in 3 steps. First, a watchdog timer in an I/O subsystem alerts I/O subsystem software that the central system has failed. Second, the I/O subsystem checks BIU/MCU error logging registers and runs diagnostics to identify which resource (e.g., processor, bus or memory) has failed. Third, the I/O subsystem reinitializes the system using the configuration control within the BIU and MCU to configure out the failed resource. The system is up and running without human intervention after only a short period of down time.

The basic configuration is the lowest cost alternative, but for some applications it is desirable to have a very high degree of confidence that calculations are performed correctly. A QMR system will do this since all components have a checker that alerts the system whenever a mistake is made. However, a QMR configuration may be overkill for some applications that can tolerate an occasional system failure, as long as the computations are correct when they do complete. FRC configurations offer an alternative in between the basic and QMR approaches. Adding a second set of checker components to each module improves the error detection capabilities of the system providing "high confidence" computing. No single hardware failure will go undetected and corrupt the results of a critical computation. FRC insures that any error is caught before it can propagate to another module in the system. FRC alone does not provide automatic hardware recovery like a QMR system, but it does detect errors as soon as they occur so that the system does not become corrupted. It is then the responsibility of system software to implement a "self-healing" strategy where the faulty resource is disabled and the system reinitialized.

The software configurability of a BIU/MCU system allows a system to use a combination of the above strategies. For example, software can configure a system as a full QMR system in the morning for critical applications, and then switch to an FRC only system in the afternoon. This doubles the system throughput (twice as many processors are working in parallel) without making any hardware changes.

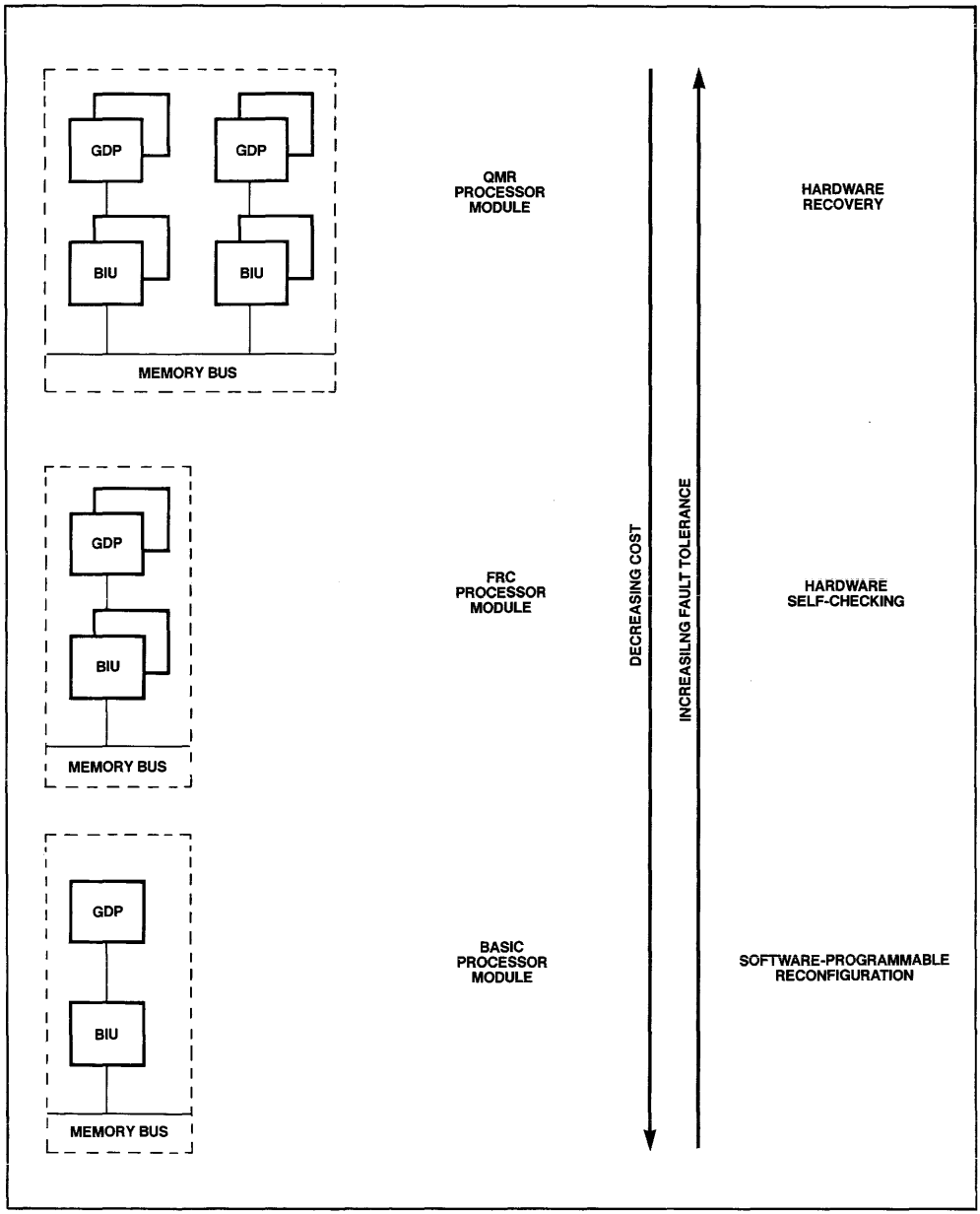


Figure 8. Fault-Tolerant Alternatives

FAULT-TOLERANT SYSTEM DESIGN RESPONSIBILITIES

The interconnect architecture and the VLSI components provide a stable base for developing fault-tolerant iAPX 432 systems. The iAPX 432 interconnect components address the issues concerning fault tolerance which are encountered when constructing the iAPX 432 central system. *A number of system-wide issues remain the responsibility of the iAPX 432 system designer.* These issues include:

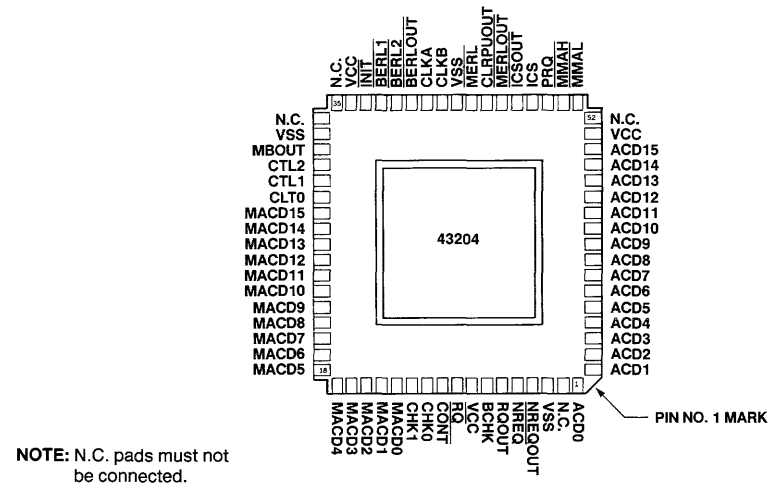
- A fault-tolerant I/O system
- Fault-tolerant power supplies and distribution method
- A fault-tolerant method for clock generation and distribution
- The electrical and physical provisions for on-line repair

SUMMARY

The iAPX 432 interconnect architecture provides a standard VLSI method for constructing multiple processor VLSI computer systems. The iAPX 432 interconnect architecture is implemented by a pair of VLSI components, the Bus Interface Unit (BIU) and the Memory Control Unit (MCU). Together with iAPX 432 processors, these components permit the construction of modular, extensible, multiprocessor computer systems. The components are designed to support the construction of fully fault-tolerant iAPX 432 systems. However, there is no penalty in performance or in cost for those applications that do not require fault tolerance.

The 432 fault-tolerant mechanisms are designed to provide a flexible and complete solution to the problems of fault-tolerant hardware. For basic systems (those without checkers for error detection or QMR for recovery), a user may decide to use only a few detection mechanisms and provide recovery only for transient errors. This functionality comes at no additional cost in the VLSI interconnect system. To reduce maintenance cost and increase system availability, a system may use all of the detection mechanisms (i.e. may add checker components) but may not add any extra recovery capability (i.e. may not marry self-checking modules into a fault-tolerant QMR module). Continuous operation is available to the user who adds the extra recovery capabilities.

None of the fault-tolerant mechanisms reduce system performance. Systems that do not require the highest level of fault tolerance are not penalized in any way (cost, size, or performance) for the unused fault-tolerant capabilities. Increased levels of fault tolerance are achieved by replicating the iAPX 432 VLSI components. The hardware fault tolerance in the iAPX 432 is transparent to application software. The system's fault-tolerant capabilities may be changed without any changes to the application software system.



NOTE: N.C. pads must not be connected.

Figure 9. 43204 Pin Configuration

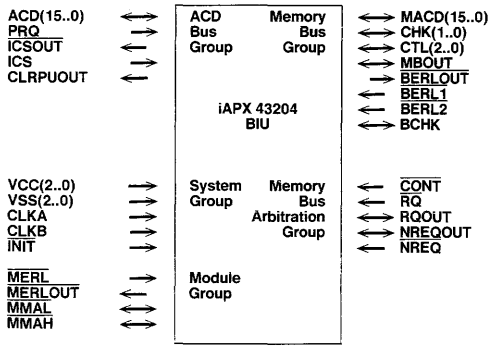


Figure 10. iAPX 43204 BIU Logic Symbol

Table 1. iAPX 43204 BIU Pin Description

Symbol	Type	Name and Function
Memory Bus Group		
MACD15 . . MACD0	I/O*	These 16 bidirectional signals carry physical memory addresses, control information (access length and type), and data to and from the memory bus.
CHK1..CHK0	I/O*	These 2 bidirectional signals carry parity bit check information which detects errors in transfers on MACD15 . . MACD0 and CTL2 . . CTL0. The 2 parity check bits are computed to satisfy the following equations (X = Exclusive OR): MACD15 X MACD13 X MACD11 X MACD9 X MACD7 X MACD5 X MACD3 X MACD1 X CTL1 X CHK1 = 0 MACD14 X MACD12 X MACD10 X MACD8 X MACD6 X MACD4 X MACD2 X MACD0 X CTL2 X CTL0 X CHK0 = 1 The BIU and MCU generate and check even parity (an even number of ones) across the 10 odd-numbered MACD, CTL, and CHK signals, and odd parity (an odd number of ones) across the 11 even-numbered MACD, CTL, and CHK signals.
CTL2..CTL0	I/O*	The 3 MACD bus control signals carry a code that controls the sequencing of the memory bus.
MBOUT	I/O**	MBOUT controls the direction of external buffers for the MACD, CHK, and CTL signals. When MBOUT is asserted, it indicates that the buffers must be directed to carry information outbound from the component to the memory bus.
$\overline{\text{BERLOUT}}$	0	$\overline{\text{BERLOUT}}$ supplies bit-serial bus error messages when the component detects a memory bus error, a storage array error, or a memory module error.
$\overline{\text{BERL1}}$, $\overline{\text{BERL2}}$,	I I	$\overline{\text{BERL1}}$ and $\overline{\text{BERL2}}$ are duplicate paths on which the component receives bit-serial bus error messages from the memory bus. When duplicated paths are not required, these two pins must be supplied with the same bus error report information.
BCHK	I/O*	BCHK provides a mechanism which checks that external buffers are operating. BCHK is toggled once each clock cycle by the component that is driving it. In an FRC pair, the master component drives BCHK. The checker component in the FRC pair receives BCHK. Routing BCHK from the master component, through one buffer in each external buffer package, and to the checker component, forms a serial network. If the oscillating BCHK signal fails to traverse the external buffer network, the buffer path is suspect and a bus error will be signalled. Buffer checking can be disabled by interconnect register programming.

Table 1. iAPX 43204 BIU Pin Description (Continued)

Symbol	Type	Name and Function
Memory Bus Arbitration Group		
$\overline{CONT}$	I	The $\overline{CONT}$ input indicates if the external arbitration network has detected that two or more simultaneous requests have been made for the use of the memory bus. When contention is indicated, all contending components will perform a binary arbitration sequence (based on each component's unique 6-bit module ID) to decide which component will be granted first use of the memory bus.
$\overline{RQ}$	I	The $\overline{RQ}$ input indicates if any agent is requesting the use of the memory bus. There are three valid combinations for $\overline{RQ}$ and $\overline{CONT}$: **$\overline{RQ}$ $\overline{CONT}$ Interpretation** 1 1 No request 0 1 One BIU is making a request 0 0 Two or more BIUs are making a request The MCU does not generate any memory bus requests. The MCU tracks the action of $\overline{RQ}$ and $\overline{CONT}$, and the CTL(2 . . 0) signals to determine when it is allowable to use the memory bus to reply to a request.
RQOUT	I/O**	When asserted, RQOUT signals that the component requires the use of the memory bus. RQOUT is intended to drive an external open-collector inverter which is wire-ORed to form a combined $\overline{RQ}$ line. The RQOUT signal from all BIUs attached to a memory bus must be logically combined to form a contention signal. (Contention occurs when two or more BIUs issue RQOUT simultaneously). The logic to detect contention among BIUs must be supplied by the customer.
NREQOUT	I/O*	The NREQOUT signal indicates that the component has received a new request from its associated processor. NREQOUT is intended to drive an external open-collector inverter, which is wire-ORed (with the same signal from other BIUs on the memory bus) to form $\overline{NREQ}$.
$\overline{NREQ}$	I	$\overline{NREQ}$ is an input that signals the beginning of a new time-ordered request cycle in which a request from one or more processors must be managed.

Table 1. iAPX 43204 BIU Pin Description (Continued)

Symbol	Type	Name and Function
Module Group		
$\overline{\text{MERL}}$	I	The $\overline{\text{MERL}}$ input accepts bit-serial module error messages. See the $\overline{\text{BERLOUT}}$ pin description for the format of the serial error messages.
$\overline{\text{MERLOUT}}$	O	The $\overline{\text{MERLOUT}}$ output broadcasts bit-serial module error messages to all BIUs contained within the same module (attached to the same processor).
$\overline{\text{MMAL}}$	I/O+	$\overline{\text{MMAL}}$ operates in the same manner as $\overline{\text{MMAH}}$ except that when $\overline{\text{MMAL}}$ is asserted it indicates that the lower addressed portion of a multiple module access is in progress on the memory bus. The two BIUs that are cooperating in a multiple module access observe both $\overline{\text{MMAH}}$ and $\overline{\text{MMAL}}$. Both signals are deasserted after each BIU has completed its portion of the access on the memory bus to which it is connected. In read accesses, after both signals are deasserted, the BIU with the lower addressed portion of the access presents data to the processor first. The BIU with the higher addressed portion of the access tracks the other BIU by counting the number of bytes returned to the processor (noting ICS, Interconnect Status, see below). When the BIU with the lower-addressed portion of the access completes its transfer, the next BIU begins automatically. Multiple module read accesses which begin at an odd addressed byte boundary cause the two cooperating BIUs to simultaneously return data to the processor. At the address boundary for which they share access responsibility, the low BIU returns its last byte on ACD7 . . ACD0, and the high BIU returns its first byte on ACD15 . . ACD8. After $\overline{\text{MMAH}}$ and $\overline{\text{MMAL}}$ have been deasserted, one (or both) of the BIUs may reassert the signals, each to indicate that its portion of the multiple module access encountered an error. This indication will be returned to the processor during error significance time for ICS.
$\overline{\text{MMAH}}$	I/O+	When asserted, $\overline{\text{MMAH}}$ indicates that one of the BIUs in a module is performing the high order address part of a multiple module access. A multiple module access occurs when a processor request spans an address range such that two memory buses, each connected via a different BIU, much be engaged. When it is deasserted, $\overline{\text{MMAH}}$ indicates that the high portion of the access has been completed on the memory bus.

Table 1. iAPX 43204 BIU Pin Description (Continued)

Symbol	Type	Name and Function
ACD Bus Group		The ACD Bus Group contains the set of signals with which a compatible iAPX 432 processor connects to the BIU. See the iAPX 43201/43202 General Data Processor Data Sheet (Order Number 590125) and the iAPX 43203 Interface Processor Data Sheet (Order Number 590130) for information about compatible iAPX 432 processors.
ACD15 . . ACD0	I/O	These 16 signals form the processor-to-BIU communication path that carries all memory and interconnect accesses.
PRQ	I	PRQ indicates the start of a processor request to the BIU.
$\overline{\text{ICSOUT}}$	O	$\overline{\text{ICSOUT}}$ is intended to drive an external open-collector inverter to form ICS. All BIUs in a processor module contribute to the wired-OR ICS signal.
ICS	I	ICS supplies interconnect status to both the BIU and its associated iAPX 432 processor. ICS carries information on errors, data synchronization, and interprocessor communication to the processor. It is also monitored by each BIU for coordinating multiple module accesses.
CLRPUOUT	O	CLRPUOUT is intended to drive an open collector inverter and form a wired-OR $\overline{\text{CLR}}$ signal to the associated iAPX 432 processor. All BIUs in a processor module contribute to the wired-OR $\overline{\text{CLR}}$ signal. Using CLRPUOUT, a BIU can synchronize the FRC master and checker processor components.
System Group		
VCC2..VCC0		Three VCC pins supply 5-volt power to the BIU/MCU. All three pins must be connected. The three VCC pins are not connected together inside the component.
VSS2..VSS0		Three VSS pins provide ground to the BIU/MCU. All three pins must be connected. The three VSS pins are not connected together inside the component.
CLKA	I	CLKA is a square-wave clock for the BIU/MCU. CLKA must operate continuously to preserve the operating state of the component.
CLKB	I	CLKB is a square-wave clock for the BIU/MCU. CLKB is the same frequency as CLKA but lags CLKA by 90 degrees. CLKB must operate continuously to preserve the operating state of the component.
$\overline{\text{INIT}}$	I	$\overline{\text{INIT}}$ is a signal that causes the BIU/MCU to initialize. In addition, $\overline{\text{INIT}}$ is used to enable external logic which provides configuration information to the component.

Legend:
I = Input signal
O = Output signal
I/O = Input/Output signal
* = FRC errors cause module error
** = FRC errors cause bus error
$\underline{+}$ = External passive pullup required (10K Ohms)
$\overline{}$ = Asserted low

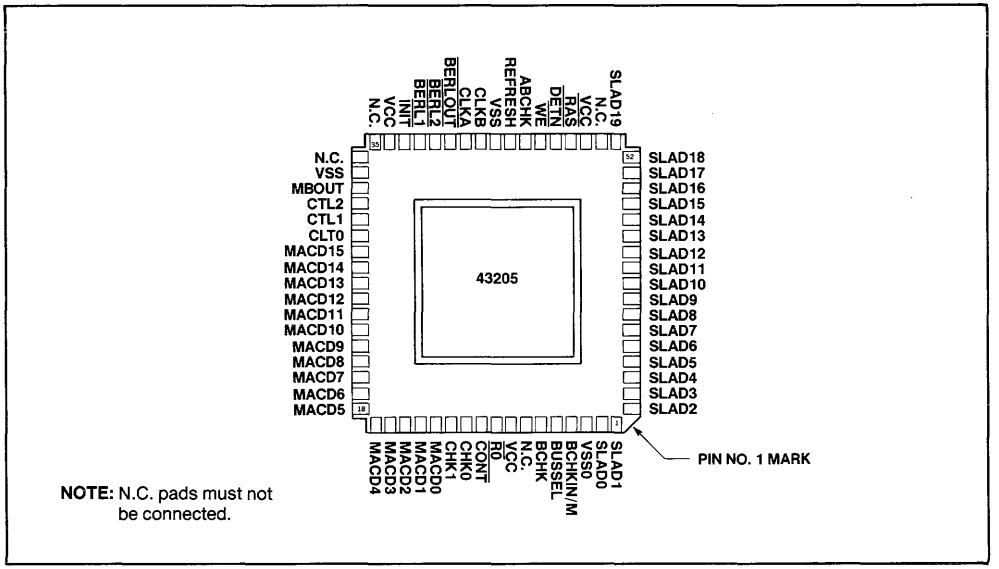


Figure 11. 43205 Pin Configuration

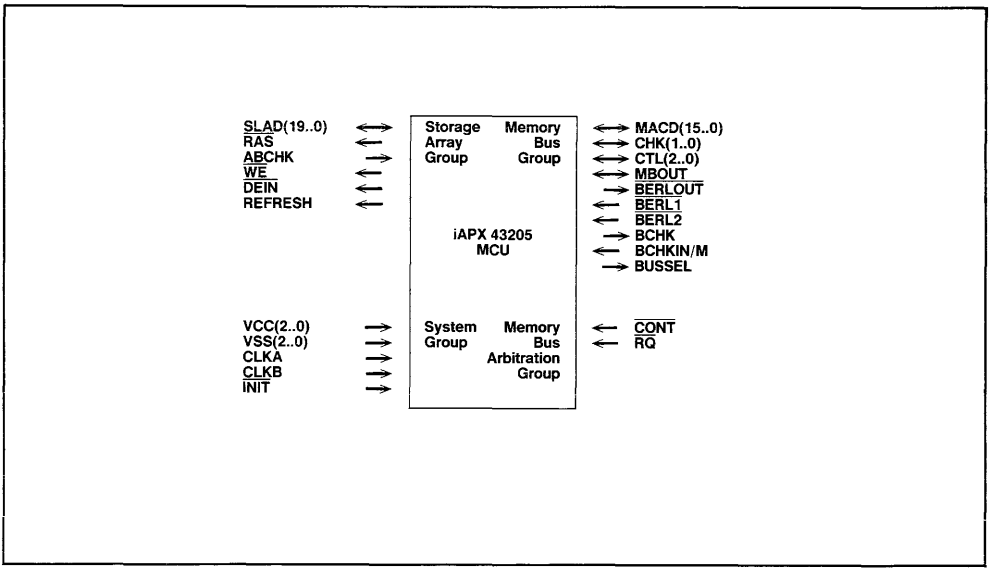


Figure 12. iAPX 43205 MCU Logic Symbol

Table 2. iAPX 43205 MCU Pin Description

Symbol	Type	Name and Function
Memory Bus Group		
MACD15 . . MACD0	I/O*	These 16 bidirectional signals carry physical memory addresses, control information (access length and type), and data to and from the memory bus.
CHK1..CHK0	I/O*	These 2 bidirectional signals carry parity bit check information which detects errors in transfers on MACD15 . . MACD0 and CTL2 . . CTL0. The 2 parity check bits are computed to satisfy the following equations (X = Exclusive OR): MACD15 X MACD13 X MACD11 X MACD9 X MACD7 X MACD5 X MACD3 X MACD1 X CTL1 X CHK1 = 0 MACD14 X MACD12 X MACD10 X MACD8 X MACD6 X MACD4 X MACD2 X MACD0 X CTL2 X CTL0 X CHK0 = 1 The BIU and MCU generate and check even parity (an even number of ones) across the 10 odd-numbered MACD, CTL, and CHK signals, and odd parity (an odd number of ones) across the 11 even-numbered MACD, CTL, and CHK signals.
CTL2..CTL0	I/O*	The 3 MACD bus control signals carry a code that controls the sequencing of the memory bus.
MBOUT	I/O**	MBOUT controls the direction of external buffers for the MACD, CHK, and CTL signals. When MBOUT is asserted, it indicates that the buffers must be directed to carry information outbound from the component to the memory bus.
$\overline{\text{BERLOUT}}$	O	$\overline{\text{BERLOUT}}$ supplies bit-serial bus error messages when the component detects a memory bus error, a storage array error, or a memory module error.
$\overline{\text{BERL1}}$ $\overline{\text{BERL2}}$	I I	$\overline{\text{BERL1}}$ and $\overline{\text{BERL2}}$ are duplicate paths on which the component receives bit-serial bus error messages from the memory bus. When duplicated paths are not required, these two pins must be supplied with the same bus error report information.
BCHK	O*	BCHK provides a mechanism which checks that external buffers are operating. BCHK is toggled once each clock cycle by the component. By routing BCHK through one buffer in each external buffer package to BCHKIN/M, a serial network is formed. If the oscillating BCHK signal fails to traverse the external buffer network, BCHKIN/M will detect the error and signal a bus error. The BCHK signal does not toggle when the component is being initialized by either the $\overline{\text{INIT}}$ signal or an internal initialization request. Buffer checking can be disabled by a parameter acquired by the MCU during initialization. The MCU will disable buffer checking after it detects a permanent module error.
BCHKIN/M	I	BCHKIN/M checks the oscillating BCHK signal after it has been routed through each of the external buffers for the memory bus. If any errors are detected, a module error will be signalled. During initialization, the BCHKIN/M pin accepts the MASTER information. If it is high during initialization, then the component will become the master of an FRC pair of components; otherwise it will become a checker.

Table 2. iAPX 43205 MCU Pin Description (Continued)

Symbol	Type	Name and Function
Memory Bus Group		
BUSSEL	O	BUSSEL controls which of two memory buses (normal or backup) the MCU is to use. The middle bit of an internal 3-bit normal bus identifier (ID) is logically combined with an internal bus state code to produce BUSSEL. The bus state code records the state and health of both the normal and backup buses. When the component switches to an alternate bus (changes the bus state code), BUSSEL is changed accordingly.
Memory Bus Arbitration Group		
$\overline{CONT}$	I	The $\overline{CONT}$ input indicates if the external arbitration network has detected that two or more simultaneous requests have been made for the use of the memory bus. When contention is indicated, all contending components will perform a binary arbitration sequence (based on each component's unique 6-bit module ID) to decide which component will be granted first use of the memory bus.
$\overline{RQ}$	I	The $\overline{RQ}$ input indicates if any agent is requesting the use of the memory bus. There are three valid combinations for $\overline{RQ}$ and $\overline{CONT}$: **$\overline{RQ}$ $\overline{CONT}$ Interpretation** 1 1 No request 0 1 One BIU is making a request 0 0 Two or more BIUs are making a request The MCU does not generate any memory bus requests. The MCU tracks the action of $\overline{RQ}$ and $\overline{CONT}$, and the CTL(2 . . 0) signals to determine when it is allowable to use the memory bus to reply to a request.
Storage Array Group		
SLAD19. . SLAD0	I/O*	The 20 SLAD signals form the communication path between the MCU and its associated storage array. The SLAD bus multiplexes addresses to the storage array with data (32 bits) and ECC (7 bits) which are to be read from or written to the array.
$\overline{RAS}$	O*	When $\overline{RAS}$ is asserted, it indicates the start of a storage array cycle. $\overline{RAS}$ may combine with external sequencing logic to control the operation of the storage array.
ABCHK	I	ABCHK is an input used to verify operation of the external buffers associated with the storage array. ABCHK is analogous to the BCHKIN input in the memory bus group. To check the control signals to the storage array, the signals $\overline{WE}$ and $\overline{CAS}$ (generated by the external array sequencing logic) are used to generate a signal that is routed serially through all of the external buffers. To check the buffers to the storage array the oscillating BCHK signal, buffer control signals, and an external decoder PROM can be used to produce the ABCHK signal. An alternative method of checking the storage array buffers is to use buffer packages with no more than four buffers so that the special ECC protection in the MCU may detect buffer failures.
$\overline{WE}$	O*	When $\overline{WE}$ is asserted, the MCU indicates that a write operation is to be performed in the storage array.

Table 2. iAPX 43205 MCU Pin Description (Continued)

Symbol	Type	Name and Function
Memory Bus Arbitration Group		
$\overline{\text{DEIN}}$	O*	When $\overline{\text{DEIN}}$ is asserted, the MCU indicates that the SLAD19 . . SLAD0 signals are ready to accept information from the storage array into the MCU.
REFRESH	O*	When REFRESH is asserted the MCU indicates that the storage array cycle is a refresh cycle. In systems with multiple bank dynamic RAM storage arrays, the REFRESH signal may be used to command the storage array sequencing logic to perform an appropriate cycle (e.g., RAS-only refresh for all banks). In a storage array with a single bank of dynamic RAMs the REFRESH signal need not be used.
System Group		
VCC2..VCC0		Three VCC pins supply 5-volt power to the BIU/MCU. All three pins must be connected. The three VCC pins are not connected together inside the component.
VSS2..VSS0		Three VSS pins provide ground to the BIU/MCU. All three pins must be connected. The three VSS pins are not connected together inside the component.
CLKA	I	CLKA is a square-wave clock for the BIU/MCU. CLKA must operate continuously to preserve the operating state of the component.
CLKB	I	CLKB is a square-wave clock for the BIU/MCU. CLKB is the same frequency as CLKA but lags CLKA by 90 degrees. CLKB must operate continuously to preserve the operating state of the component.
$\overline{\text{INIT}}$	I	$\overline{\text{INIT}}$ is a signal that causes the BIU/MCU to initialize. In addition, $\overline{\text{INIT}}$ is used to enable external logic which provides configuration information to the component.

Legend: I = Input signal
O = Output signal
I/O = Input/Output signal
* = FRC errors cause module error
$\underline{**}$ = FRC errors cause bus error
$\overline{}$ = Asserted low

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Range ..... 0°C to 70°C
Storage Temperature .....−65°C to +150°C
Voltage on Any Pin with
Respect to Ground ..... −1.0V to +7V
Power Dissipation ..... 2.2 Watt

**NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

iAPX 43204 DC Characteristics

Symbol	Description	Min	Max	Units
Vilc	Clock input low voltage	−0.5	+0.8	V.
Vihc	Clock input high voltage	3.2	Vcc+0.5	V.
Vil	Input low voltage	−0.5	+0.8	V.
Vih	Input high voltage	2.0	VCC+0.5	V.
Vol	Output low voltage	—	0.45	V.
Voh	Output high voltage	2.4	VCC	V.
Ili	Input leakage current (measured at Vin=VCC)	—	±10	μA.
Ilo	Output leakage current (measured at 0.45 V. ≤ Vout ≤ VCC)	—	±10	μA.
Ioh	Output high current (measured at 2.6 V.)	−2	—	mA.
Iol	Output low current (measured at 0.45 V.)	4	—	mA.
Icc	Power supply current (sum of VCC0, VCC1, VCC2)	—	400	mA.

All DC parameters are guaranteed over the following conditions:

VSS2..VSS0 = 0 Volts
VCC2..VCC0 = 5.0 Volts ±10%
The absolute value of the differential DC voltage between any of the VCC pins (VCC2..VCC0) must be less than 0.1 Volts. This is normally guaranteed by connecting the three VCC pins to the same printed circuit power trace.

iAPX 43204 AC Characteristics

Ambient temperatrue range of 0°C to 70°C

Symbol	Description	8 MHz		Unit
		Min	Max	
tr, tf	Clock rise and fall times	0	10	nsec.
t1, t2, t3, t4	Clock pulse width	24	250	nsec.
tcy	Clock cycle time	125	1000	nsec.
tcd	Clock to signal delay time	—	55	nsec.
tdh	Clock to signal hold time	15	—	nsec.
ten	Clock to signal output enable time	15	—	nsec.
tdf	Clock to signal data float time	—	40	nsec.
tdc	Signal to clock setup time	5	—	nsec.
tie	Initialization period	20	100	tcy

All AC parameters are guaranteed over the following conditions:

VSS2..VSS0 = 0 Volts
VCC2..VCC0 = 5.0 Volts ±10%

100 picoFarad external load capacitor on all output pins

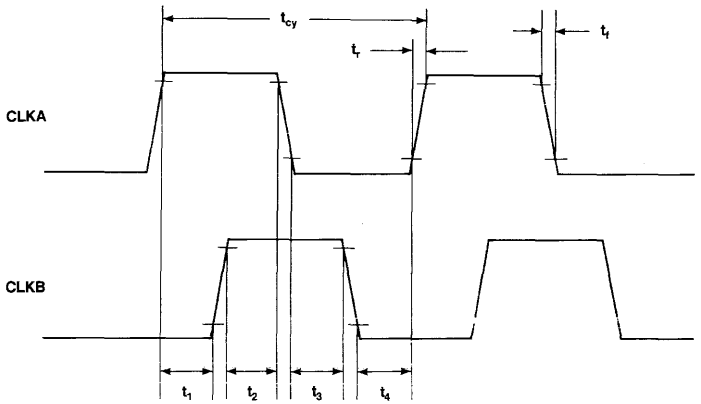
iAPX 43204 Capacitance Data

Conditions: Ta = 25°C
VCC = 5.0 Volts, GND = 0.0 Volts
f(test) = 1.0 MHz
Inputs held at 0.0 Volts
All outputs in high impedance state
All input/output pins are classified as outputs

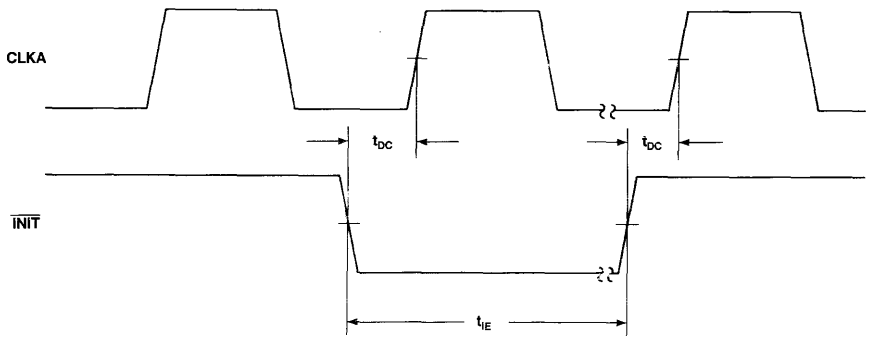
Symbol	Description	Max	Units
Cin	Input Capacitance	6	pF
Cout	Output Capacitance	12	pF

WAVEFORMS

iAPX 43204 Clock Input Specification

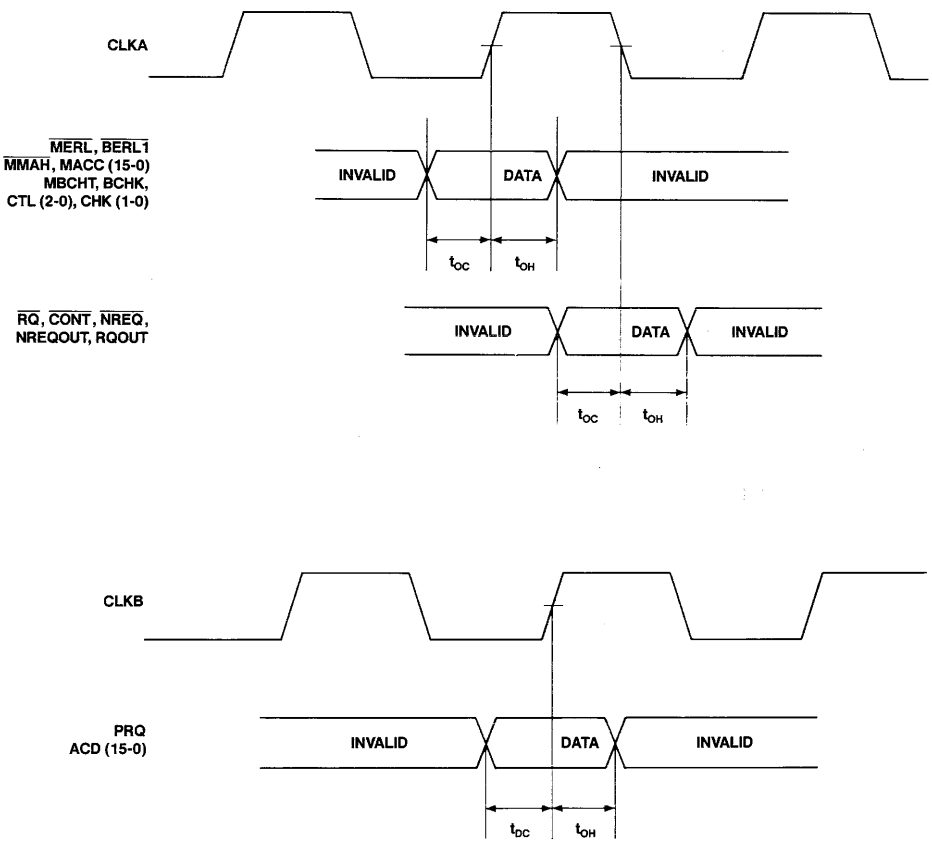


iAPX 43204 Initialization Timing



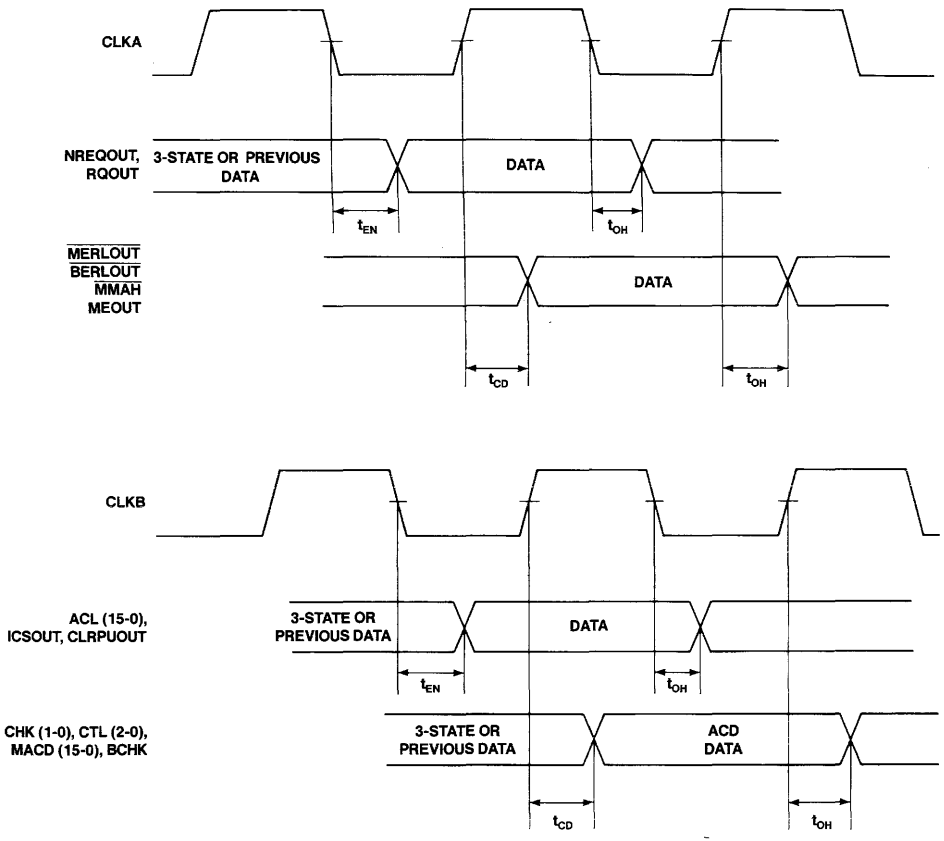
WAVEFORMS (Continued)

iAPX 43204 Input Timing Specification



WAVEFORMS (Continued)

iAPX 43204 Output Timing Specification



ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Range ..... 0°C to 70°C
Storage Temperature .....−65°C to +150°C
Voltage on Any Pin with
Respect to Ground ..... −1.0V to +7V
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Vil	Input low voltage	−0.5	+0.8	V.
Vih	Input high voltage	2.0	VCC+0.5	V.
Vol	Output low voltage	—	0.45	V.
Voh	Output high voltage SLAD19..0 Other outputs	 2.6 2.4	 VCC VCC	 V. V.
Ili	Input leakage current (measured at Vin=VCC Volts)	—	±10	μA.
Ilo	Output leakage current (measured at 0.45 Volts ≤ Vout ≤ VCC Volts)	—	±10	μA.
Ioh	Output high current (measured at Vout=2.6 V.)	−2	—	mA.
Iol	Output low current (measured at Vout=0.45 V.)	4	—	mA.
Icc	Power supply current (sum of VCC0, VCC1, VCC2)	—	450	mA.

All DC parameters are guaranteed over the following conditions:

VSS2..VSS0 = 0 Volts
VCC2..VCC0 = 5.0 Volts ±10%
The absolute value of the differential DC voltage between any of the VCC pins (VCC2..VCC0) must be less than 0.1 Volts. This is normally guaranteed by connecting the three VCC pins to the same printed circuit power trace.

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tdh	Clock to signal hold time	15	—	nsec.
ten	Clock to signal output enable time	15	—	nsec.
tdf	Clock to signal data float time	—	40	nsec.
tdc	Signal to clock setup time	15	—	nsec.
tmc	MACD input setup time	24	—	nsec.
tie	Initialization period	40	100	tcy

All AC parameters are guaranteed over the following conditions:

VSS2..VSS0 = 0 Volts
VCC2..VCC0 = 5.0 Volts ±10%

100 picoFarad external load capacitor on all output pins

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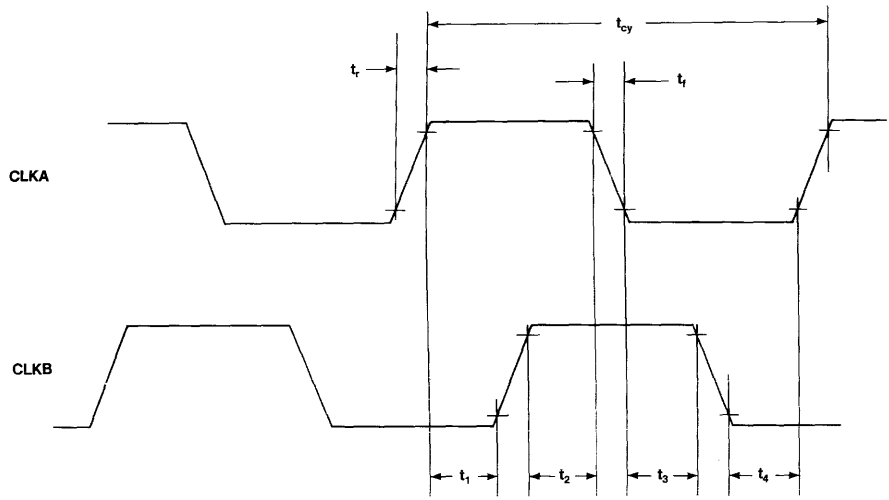
Conditions: Ta = 25°C
VCC = 5.0 Volts, GND = 0.0 Volts
f(test) = 1.0 MHz
Inputs held at 0.0 Volts
All outputs in high impedance state
All input/output pins are classified as outputs

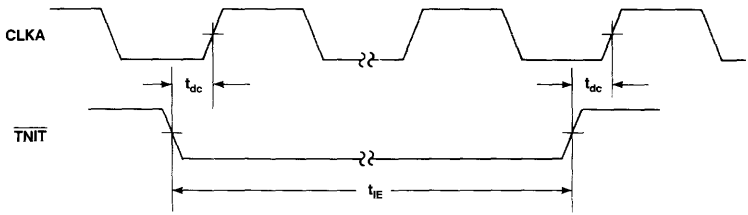
Symbol	Description	Max	Units
Cin	Input Capacitance	6	pF
Cout	Output Capacitance	12	pF

WAVEFORMS

Clock Input Timing Specification

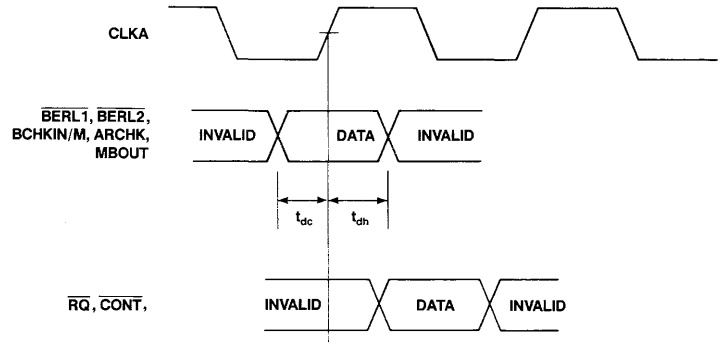


Initialization Timing Specification

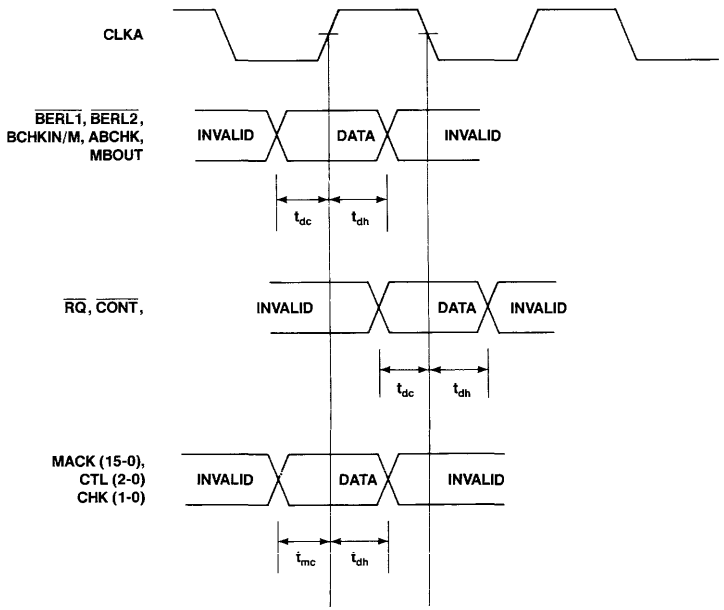


WAVEFORMS (Continued)

Input Timing Specification

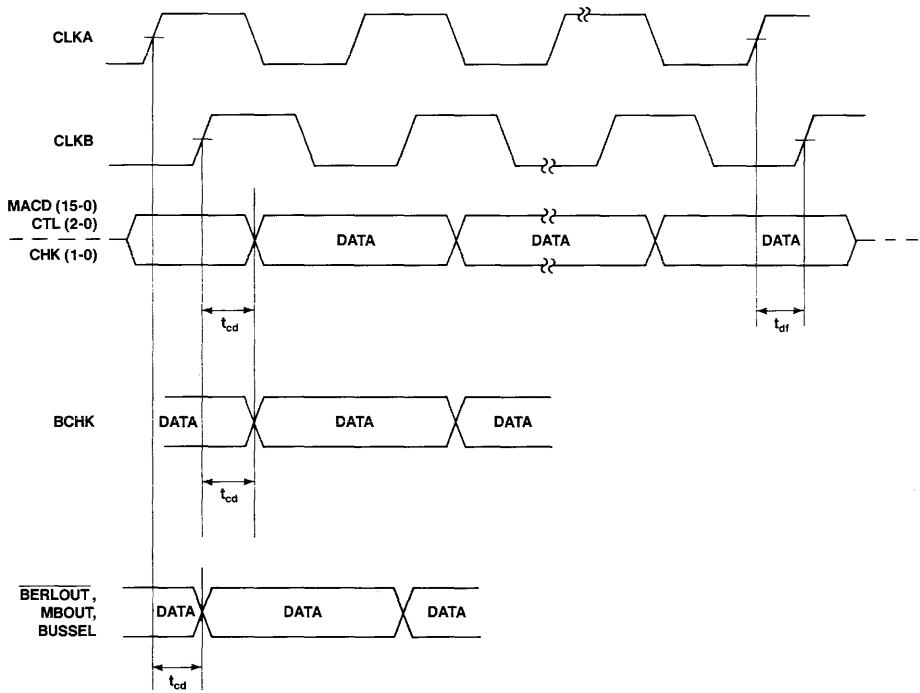


Memory Bus Input Timing Specification



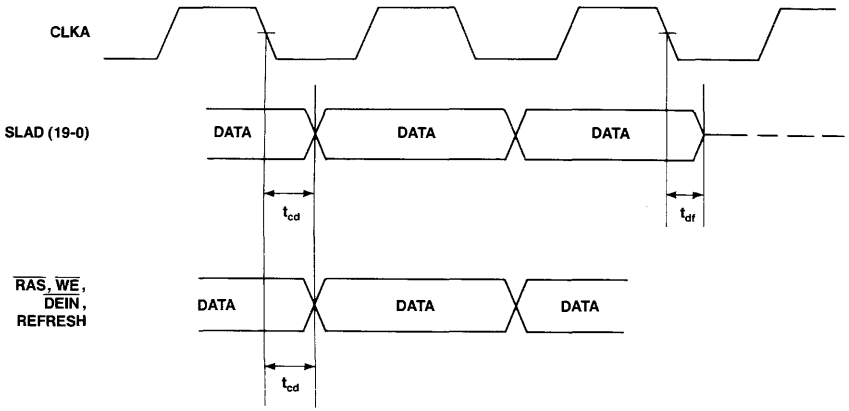
WAVEFORMS (Continued)

Memory Bus Output Timing Specification

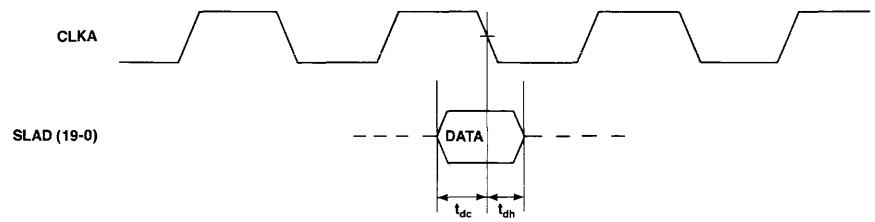


WAVEFORMS (Continued)

Storage Array Bus Output Timing Specification



Storage Array Bus Input Timing Specification



PACKAGE

The 43204 and 43205 are packaged in 68-pin, leadless JEDEC type A hermetic chip carriers. Figure 13 illustrates the package, and Figures 9 and 11 show the pinouts.

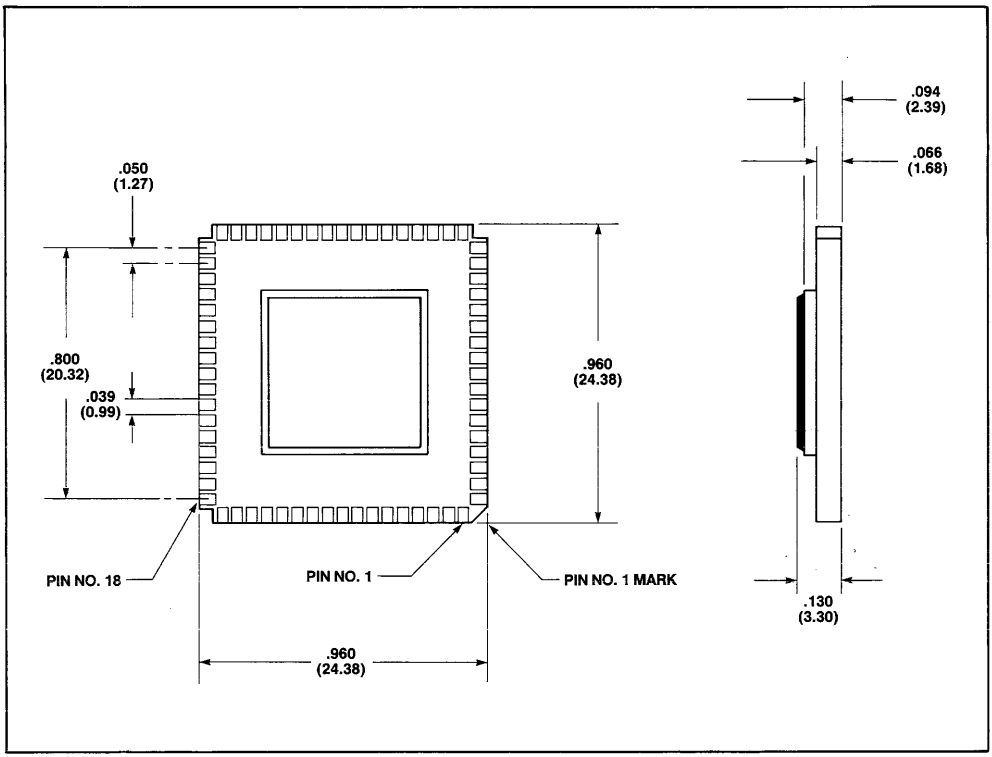


Figure 13. 43204 and 43205 JEDEC Type A Package

ADDITIONAL INFORMATION

More information about the interconnect system is available in :

- *iAPX 43204/43205 Electrical Specification* (Order Number 172867)
- *iAPX 432 Interconnect Architecture Reference Manual* (Order Number 172487)
- Chapter 18: A Design Methodology for High Reliability Systems: The Intel 432, *The Theory and Practice of Reliable System Design*, Sieworik and Swartz, Digital Press, 1982.

For more information about overall iAPX 432 system operation, refer to:

- *General Data Processor Architecture Reference* (Order Number 171860)
- *iAPX 432 Interface Processor Architecture Reference Manual* (Order Number 171863)

For more information about iAPX 432 processor components that utilize the interconnect system, refer to:

- *iAPX 43201/43202 General Data Processor Data Sheet* (Order Number 590125)
- *iAPX 43203 Interface Processor Data Sheet* (Order Number 590130)

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