μP

CMOS Microprocessor

CMOS Peripherals

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

Volume 1

VOLUME I
PRICE $2.95

Harris CMOS Microprocessor Data Book

μP

Harris Semiconductor Microprocessor Products represent state-of-the-art in density and high speed performance. Harris' expertise in design and processing offers the user the most reliable product available in a wide choice of formats, options, and package types. With continuing research and development and the introduction of new products, Harris will provide its customers with the most advanced technology.

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NOTE: *Available as separate data sheets.

Data Sheet Classifications

CLASSIFICATION	PRODUCT STAGE	DISCLAIMERS
Preview DATA SHEET	Formative or Design	This document contains the design specifications for product under development. Specifications may be changed in any manner without notice.
Advance Information DATA SHEET	Sampling or Pre-Production	This is advanced information, and specifications are subject to change without notice.
Preliminary DATA SHEET	First Production	Supplementary data maybe published at a later date. Harris reserves the right to make changes anytime without notice, in order to improve design and supply the best product possible.

CMOS Microprocessor Products

GENERAL DESCRIPTION

The 6100 CMOS Microprocessor Family offers all CMOS components, enabling the designer to build low power PDP-8 based microcomputer systems. Obvious advantages of this architecture are readily available software, a variety of development and operating systems and a familiar instruction set that is easy to program. The low power, single voltage CMOS circuitry and LSI design of each component within the 6100 microcomputer system will result in cost effective systems that minimize power and packaging costs. For example, the operating power drain for a system consisting of 256 words of RAM, an interval timer, two latched I/O ports, an I/O controller, and 1024 words of ROM is typically less than 100mW. Minimum package, high density configurations allow this all CMOS microcomputer to be incorporated on small printed circuit boards (approximately 4" by 5"), suggesting interesting possibilities for portable, self-contained equipment designs. Here are a few of the benefits derived from the 6100 microcomputer system.

- Battery operation
- Data retention during power outages
- Data acquisition at remote sites
- On-site data reduction
- Portable systems
- Remote instrumentation
- Small size, low cost

The microprocessor family components include a 12-bit CPU, various I/O controllers and a wide variety of CMOS memory and bus driver devices. Using just a few of these LSI components, a minimum yet very powerful microcomputer, as shown in Figure 1, can be built having the following features.

- ROM – 1024 x 12
- RAM – 64 x 12
- Vectored or polled I/O interrupts
- Four programmable outputs
- Control for two I/O ports

The complete 6100 microprocessor product line is tabulated in Tables 1, 2, 3, and 4. For parametric data consult the appropriate product data sheet.

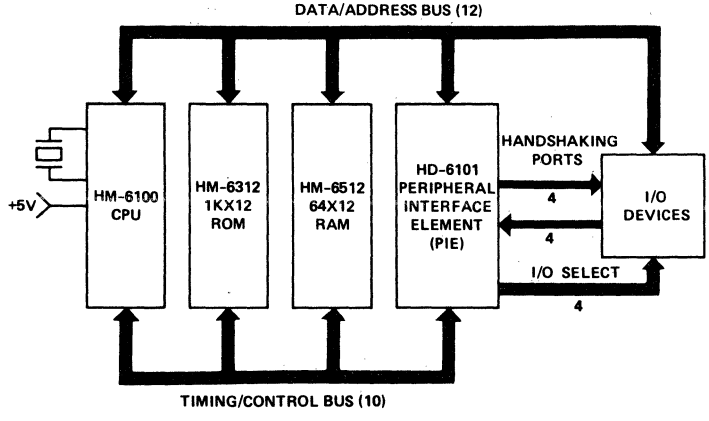

Figure 1 – Minimum CMOS Microcomputer

Table 1 — CMOS Microprocessor Products

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Bus Driver Group		
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* Digital Equipment Corporation Trademark

System Architecture

Figure 2 shows the architecture of an HM-6100 system. Note that the Register Page and Auto Increment Registers which are an integral part of the processor architecture are located in memory rather than "on-chip". This permits a larger number of registers to be made available (128 per field) and they can be operated on by all Memory Reference Instructions rather than a separate group of "register operation" instructions.

The registers on the register page are true general purpose registers in that they can be accessed with a single word instruction from anywhere in the instruction field, and can be used as stack pointers, program vectors, or as memory locations.

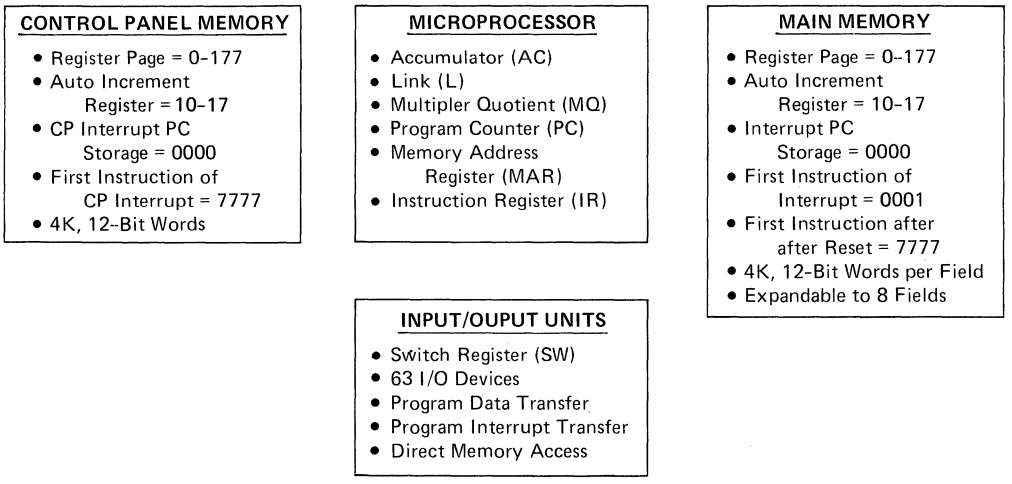

Figure 2 – HM-6100 System Architecture

Microprocessor Features

Since the HM-6100 bridges the gap between the microprocessor and minicomputer worlds, it has some features not found in most 8-bit microprocessors. These are explained more fully in the HM-6100 data sheet, but briefly they are:

Memory Reference Instructions (MRIs) – Combine the operation and the address of the operand in a single memory word. This eliminates the requirement for "immediate" instructions, shortens programs significantly, and speeds execution.

Memory Fields and Pages – The 32K memory space is conceptually divided into 4K word fields which are subdivided into 128 word pages. The memory reference instruction addresses are always specified relative to the beginning of a specific page, thus making software "page relocatable".

General Purpose Registers Located in Memory – The first 128 words of each memory field (page 0, or the Register Page) can be used as general purpose registers. Since they are located in memory, the MRIs are used to manipulate them rather than a separate set of "register instructions".

Auto Increment Registers – When locations $10\text{-}17_8$ of the register page are used as operand addresses they are automatically incremented prior to each use.

IOTs – There is an entire class of Input/Output transfer instructions. Hardware interfacing of the CPU to the various peripherals is simple and straight forward.

Microcode – Accumulator operations can be microcoded to tailor the instruction set to a particular application.

Execution Times – Since the HM-6100 is a static device which can be operated at clock frequencies from 0 to 8MHz, the number of states required to execute each instruction is given.

Control Panel Memory – This has been included in the HM-6100 to simplify implementation of the control panel function in microcomputer systems. Its use is not, however, limited to that function in that the control panel interrupt request is a true non-maskable interrupt which accesses a program stored in Control Panel (CP) memory. As such, CP memory is valuable for functions such as system debug, system diagnostic programs, non-maskable interrupt routines, resident storage of frequently used for software, etc. It is in no way limited to "Control Panel Functions". The HM-6100 will execute programs in Control Panel Memory or Main Memory or a combination of both.

NOTE: In HM-6100 literature bit 0 refers to the MSB, bit 11 refers to the LSB. Data is represented in Two's Complement Integer notation. In this system, the negative of a number is formed by complementing each bit in the data word and adding "1" to the complemented number. The sign is indicated by the most significant bit. In the 12-bit word used by the HM-6100, when bit 0 is a "0", it denotes a positive number and when bit 0 is a "1", it denotes a negative number. The maximum number ranges for this system are 3777_8 (+2047) and 4000_8 (-2048).

System Flexibility

Using the HM-6100 family, the designer has access to a comprehensive product line dedicated to satisfy his particular system requirements. He also has a very low cost reproduction of the PDP-8/E minicomputer whose existence is justified by a large product market base and a wealth of existing software. The wide range of CMOS memory products enable partitioning of the memory system in blocks from 64 to 4096 words of RAM and from 256 to 1024 words of ROM or PROM.

DEVELOPMENT SUPPORT

The 6100 CPU family is supported by the Harris, single-board, CMOS MICRO-12 microcomputer and by existing PDP-8 minicomputers and their low cost operating systems.

CMOS Microprocessor Family

μP

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2

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-6100
CMOS 12 BIT MICROPROCESSOR (CPU)

Features

- LOW POWER - TYP.<5.0μW STANDBY
- SINGLE SUPPLY 4-11 VOLT
- FULL TEMPERATURE RANGE -55°C TO +125°C
- STATIC OPERATION
- SINGLE PHASE CLOCK, ON CHIP CRYSTAL OSC.
- SOFTWARE COMPATIBLE WITH PDP-8/E
- 12-BIT DATA WORD
- OVER 90 SINGLE WORD INSTRUCTIONS
- RELOCATABLE MEMORY ORGANIZATION
- BASIC ADDRESSING TO 4K 12 BIT WORDS
- PROVISION FOR DEDICATED CONTROL PANEL
- 128 GENERAL PURPOSE REGISTERS
- 8 AUTOINDEXING REGISTERS
- FLEXIBLE PROGRAMMED I/O TRANSFERS
- VECTORED INTERRUPT CAPABILITY

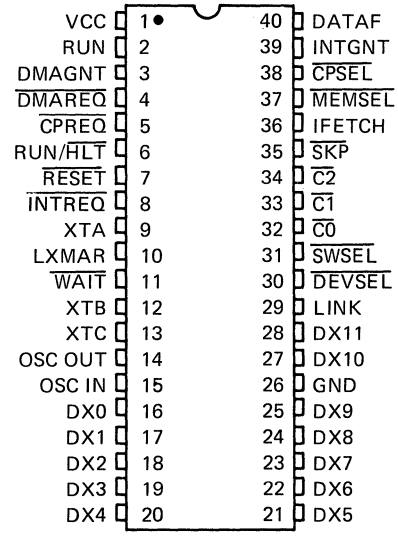
2

Description

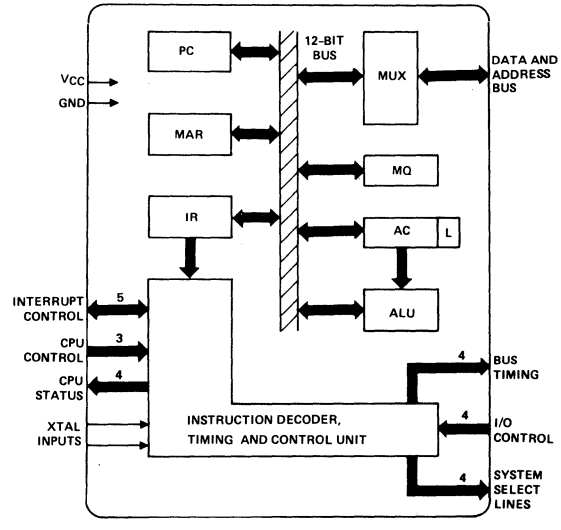
The HM-6100 is a single address, fixed word length, parallel transfer microprocessor using 12-bit two's complement arithmetic. It is a general purpose processor which recognizes the instruction set of Digital Equipment Corporation's PDP-8/E Minicomputer.

Standard features include indirect addressing and facilities for instruction skipping, program interrupts as a function of input/output device conditions, and auto-restart. Five 12-bit registers are used to control microprocessor operations, address memory, perform arithmetic or logical operations, and store data. The device design is optimized to minimize the number of external components required for interfacing with standard memory and peripheral devices.

Pinout



Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+12.0V
Input or Output Voltage Applied	Gnd -0.3V to VCC +0.3V
Storage Temperature Range	-65°C to 150°C
Operating Temperature Range	
Industrial HM-6100A-9	-40°C to +85°C
Military HM-6100A-2	-55°C to +125°C

ELECTRICAL CHARACTERISTICS

VCC = 10.0 ± 0.5 Volts, T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
VIH	Logical "1" Input Voltage	70% VCC			V	
VIHC	Logical "1" Osc. Input Voltage	VCC-.5			V	
VIL	Logical "0" Input Voltage			20% VCC	V	
VILC	Logical "0" Osc. Input Voltage			GND +.5	V	
IIL	Input Leakage (1)	-1.0		+1.0	μA	$0V \leq VIN \leq VCC$
VOH	Logical "1" Output Volt. (2)	VCC-2.0			V	IOH = -0.2mA
VOL	Logical "0" Output Volt. (2)			0.45	V	IOL = 2.0
IO	Output Leakage	-1.0		1.0	μA	$0V \leq VO \leq VCC$
ICC1	Supply Current (Static)			800	μA	VIN =VCC, Freq. = 0
ICC2	Supply Current (Operating)		1.0	10.0	mA	VCC=10.5V, Freq=2.0MHz
CI	Input Capacitance (3)		5	7	pF	
CO	Output Capacitance (3)		8	10	pF	
CIO	Input/Output Capacitance (3)		8	10	pF	
COSC	Oscillator IN/OUT CAP. (3)		30		pF	

Notes: (1) Except pin 14 and 15
(2) Except pin 14
(3) Guaranteed and sampled, but not 100% tested.

A.C.

		TA = 25°C VCC = 10.0V (1)		TA = Indust. VCC = 10 ± 0.5V		TA = Military VCC = 10 ± 0.5V			
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	TEST CONDITIONS
fMAX	Max Operating Frequency		8.0		5.71		5.0	MHz	CL = 50pF
TS	Major State Time	250		350		400		ns	See Timing Diagram
TLX	LXMAR Pulse Width	110		150		170		ns	
TAS	Address Setup Time	30		55		70		ns	
TAH	Address Hold Time	75		60		70		ns	
TAL	Access Time from LXMAR	225		295		340		ns	
TEN	Output Enable (Memory)	125		185		220		ns	
TEND	Output Enable (I/O)	150		250		290		ns	
TWP	Write Pulse Width	110		140		160		ns	
TDS	Data Setup (Memory)	80		115		140		ns	
TDSD	Data Setup (I/O)	85		110		140		ns	
TDH	Data Hold Time	50		60		70		ns	
TST	Status Signals Valid		150		200		250	ns	
TRS	Request Inputs Setup	0		0		0		ns	
TRH	Request Inputs Hold	100		150		200		ns	
TWS	Wait Setup Time	0		25		25		ns	
TWH	Wait Hold Time	50		50		80		ns	
TRHS	Run Halt Setup Time	0		30		30		ns	
TRHP	Run Halt Pulse Width	60		60		80		ns	

NOTE 1: All devices guaranteed at worst case limits. Room temperature, 10V data provided for information - not guaranteed.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	Gnd -0.3V to VCC +0.3V
Storage Temperature Range	-65°C to 150°C
Operating Temperature Range	
Industrial HM-6100-9	-40°C to +85°C
Military HM-6100-2	-55°C to +125°C

ELECTRICAL CHARACTERISTICS

VCC = 5.0 ± 10% Volts, T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
VIH	Logical "1" Input Voltage	70% VCC			V	
VIHC	Logical "1" Osc. Input Voltage	VCC-.5			V	
VIL	Logical "0" Input Voltage			20% VCC	V	
VILC	Logical "0" Osc. Input Voltage			GND +.5	V	
IIL	Input Leakage (1)	-1.0		+1.0	μA	$0V \leq VIN \leq VCC$
VOH	Logical "1" Output Volt. (2)	2.4			V	IOH = -0.2mA
VOL	Logical "0" Output Volt. (2)			0.45	V	IOL = 2.0mA
IO	Output Leakage	-1.0		+1.0	μA	$0V \leq VO \leq VCC$
ICC1	Supply Current (Static)			400	μA	VIN = VCC, Freq. = 0
ICC2	Supply Current (Operating)			2.5	mA	VCC=5.5V, Freq=2.0MHz
CI	Input Capacitance (3)		5	7	pF	
CO	Output Capacitance (3)		8	10	pF	
CIO	Input/Output Capacitance (3)		8	10	pF	
COSC	Oscillator IN/OUT CAP. (3)		30		pF	

Notes: (1) Except pin 14 and 15
(2) Except pin 14
(3) Guaranteed and sampled, but not 100% tested.

A.C.

		TA = 25°C VCC = 5.0V (1)		TA = Indust. VCC = 5.0 ± 10%V		TA = Military VCC = 5.0 ± 10%V			
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	TEST CONDITIONS
fMAX	Max Operating Frequency		4.0		3.33		2.5	MHz	CL = 50pF
TS	Major State Time	500		600		800		ns	See Timing Diagram
TLX	LXMAR Pulse Width	220		230		355		ns	
TAS	Address Setup Time	80		85		200		ns	
TAH	Address Hold Time	150		125		175		ns	
TAL	Access Time from LXMAR	450		520		745		ns	
TEN	Output Enable (Memory)	250		300		470		ns	
TEND	Output Enable (I/O)	300		470		655		ns	
TWP	Write Pulse Width	200		235		330		ns	
TDS	Data Setup (Memory)	160		135		250		ns	
TDSD	Data Setup (I/O)	185		225		350		ns	
TDH	Data Hold Time	125		125		170		ns	
TST	Status Signals Valid		250		300		325	ns	
TRS	Request Inputs Setup	0		0		0		ns	
TRH	Request Inputs Hold	200		250		300		ns	
TWS	Wait Setup Time	0		50		50		ns	
TWH	Wait Hold Time	100		100		150		ns	
TRHS	Run Halt Setup Time	0		50		50		ns	
TRHP	Run Halt Pulse Width	100		100		150		ns	

NOTE 1: All devices guaranteed at worst case limits. Room temperature, 5V data provided for information - not guaranteed.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	8.0V
Input or Output Voltage Applied	Gnd -0.3V to VCC +0.3V
Storage Temperature Range	-65°C to 150°C
Operating Temperature Range	
Industrial HM-6100C-9	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

VCC = 5.0 ± 5% Volts, T_A = Industrial

D.C.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
VIH	Logical "1" Input Voltage	70% VCC			V	
VIHC	Logical "1" Osc. Input Voltage	VCC-.5			V	
VIL	Logical "0" Input Voltage			.8	V	
VILC	Logical "0" Osc. Input Voltage			GND +.5	V	
IIL	Input Leakage (1)	-10		+10	μA	$0V \leq VIN \leq VCC$
VOH	Logical "1" Output Volt. (2)	2.4			V	IOH = -0.2mA
VOL	Logical "0" Output Volt. (2)			0.45	V	IOL = 1.6mA
IO	Output Leakage	-10		+10	μA	$0V \leq VO \leq VCC$
ICC1	Supply Current (Static)			600	μA	VIN = VCC, Freq. = 0
ICC2	Supply Current (Operating)			5.0	mA	VCC=5.5V, Freq=2.0MHz
CI	Input Capacitance (3)		5	7	pF	
CO	Output Capacitance (3)		8	10	pF	
CIO	Input/Output Capacitance (3)		8	10	pF	
COSC	Oscillator IN/OUT CAP. (3)		30		pF	

Notes: (1) Except pin 14 and 15
(2) Except pin 14
(3) Guaranteed and sampled, but not 100% tested.

A.C.

		TA = 25°C VCC=5.0V(1)		TA = Indust. VCC = 5.0 ± 5%			
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNIT	TEST CONDITION
fMAX	Max operating Freq.		3.33		2.5	MHz	CL = 50pF
TS	Major State Time	600		800		ns	See Timing Diagram
TLX	LXMAR Pulse Width	270		335		ns	
TAS	Address Setup Time	100		120		ns	
TAH	Address Hold Time	150		175		ns	
TAL	Access Time from LXMAR	500		650		ns	
TEN	Output Enable (Memory)	300		400		ns	
TEND	Output Enable (I/O)	350		575		ns	
TWP	Write Pulse Width	250		320		ns	
TDS	Data Setup (Memory)	180		240		ns	
TDSD	Data Setup (I/O)	200		275		ns	
TDH	Data Hold Time	130		175		ns	
TST	Status Signals Valid		300		350	ns	
TRS	Request Inputs Setup	0		0		ns	
TRH	Request Inputs Hold	100		130		ns	
TWS	Wait Setup Time	0		0		ns	
TWH	Wait Hold Time	100		130		ns	
TRHS	Run Halt Setup Time	0		70		ns	
TRHP	Run Halt Pulse Width	100		130		ns	

Note 1: All devices guaranteed at worst case limits. Room temperature, 5V data provided for information - not guaranteed.

Timing and State Control

The HM-6100 generates all the timing and state signals internally. A crystal is used to control the CPU operating frequency. The CPU divides the crystal frequency by two. With a 4MHz crystal, the internal states will be of 500ns duration. The major timing states are described in Figure 1.

T1 For memory reference instructions, a 12-bit address is sent on the DataX, DX, lines. The Load External Address Register, LXMAR, is used to clock an external register to store the address information externally, if required. When executing an Input-Output I/O instruction, the instruction being executed is sent on the DX lines to be stored externally. The external address register then contains the device address and control information.

Various CPU request lines are priority sampled if the next cycle is an Instruction Fetch cycle. Current state of the CPU is available externally.

T2 Memory/Peripheral data is read for an input transfer (READ). $\overline{\text{WAIT}}$ controls the transfer duration. If $\overline{\text{WAIT}}$ is active during input transfers, the CPU waits in the T2 state. The wait duration is an integral multiple of the crystal frequency - 250ns for 4MHz.

For Memory reference instructions, the Memory Select, $\overline{\text{MEMSEL}}$, lines are active. For I/O instruction the $\overline{\text{DEVSEL}}$, line is active. Control lines, therefore, distinguish the contents of the external register as memory or device address.

External device sense lines $\overline{\text{C0}}$, $\overline{\text{C1}}$, $\overline{\text{C2}}$, and SKP are sampled if the instruction being executed is an I/O instruction.

Control Panel Memory Select, $\overline{\text{CPSEL}}$, and Switch Register Select, $\overline{\text{SWSEL}}$, become active low for data transfers between the HM-6100 and Control Panel Memory and the Switch Register, respectively.

T3, T4, T5
ALU operation and internal register transfers.

T6 This state is entered for an output transfer (WRITE). The address is defined during T1. $\overline{\text{WAIT}}$ controls the time for which the WRITE data must be maintained.

The following illustrates the timing of the CPU when its operating frequency is low enough that propagation delays can be ignored. It effectively shows the timing of the CPU when it is single clocked.

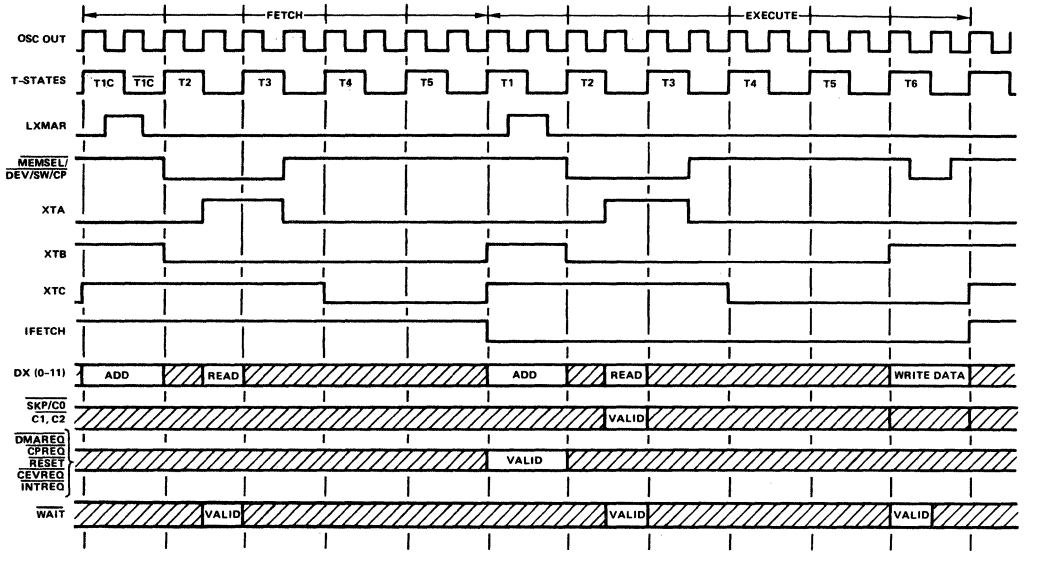


FIGURE 1 – Static Timing

The dynamic or high frequency timing illustrates the propagation delays at specified operating frequencies. (Refer to specifications) It defines the interface requirements for memory and I/O devices on the bus.

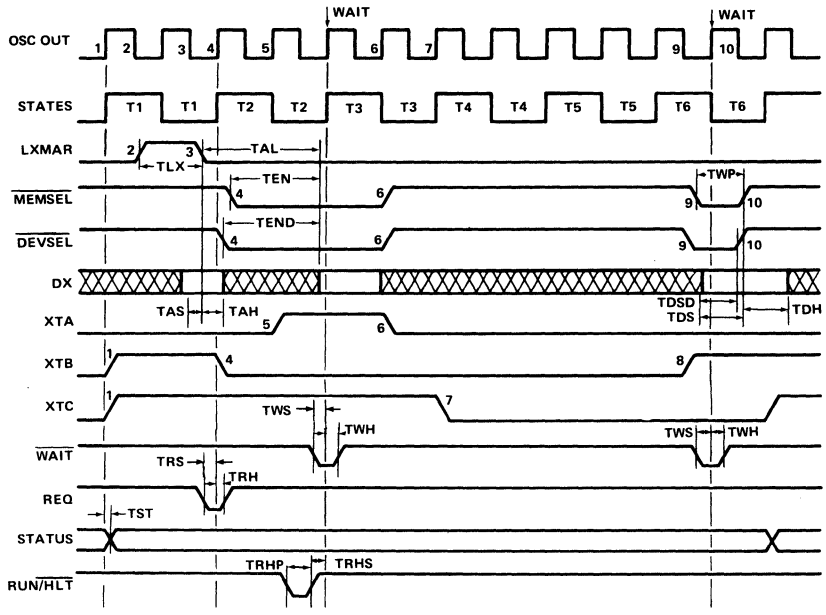


FIGURE 2 – Dynamic Timing

Microprocessor Architecture

The block diagram of the CPU architecture, shown on the front page, consists of the following major functional segments:

- CPU Registers
- Arithmetic and Logic Unit
- Dx-Bus Multiplexer
- Timing and Control Unit

Each one is briefly described below.

CPU REGISTERS

The CPU consists of five, 12-bit registers, of which three are user programmable; 1) Accumulator (AC), 2) Program Counter (PC), and 3) Multiply Quotient (MQ). The remaining two registers are the Instruction Register (IR) and the Memory Address Register (MAR) which are used exclusively for internal operations. The CPU registers are defined as follows.

ACCUMULATOR AND LINK (AC/L)

All arithmetic and logical operations are performed in the AC. For any arithmetic operation, the AC data and memory data are combined in the ALU and the result is temporarily stored in the AC. Under software control, the AC can be cleared, set, complemented, incremented, tested or rotated. Using the Operate Microinstructions, a variety of register operate instructions can be derived.

The link is a one-bit extension of the AC. It can be complemented with a carry out of the ALU or cleared, set, complemented, tested and rotated along with the rest of the AC. It also serves as the carry output for two's complement arithmetic.

MULTIPLY QUOTIENT (MQ)

The MQ register can be used as a temporary storage for the AC. The MQ may be OR'ed with the AC and the result stored in the AC or the contents of the AC and MQ may be swapped. The MQ is used in conjunction with the AC to perform multiplication, division, and double-precision operations.

PROGRAM COUNTER (PC)

The PC supports both memory and input-output device operations. For memory operations, the PC is controlled exclusively by internal logic and instructions fetched from memory. During an instruction fetch cycle the contents of the PC are transferred to the memory address register (MAR) while the current instruction is being decoded. The PC is then loaded with a new address or simply incremented for the next instruction depending upon the type of instruction. The next instruction obtained from memory is then loaded into the Instruction Register. For example, if the instruction is a JMP X, then the branch address X is loaded into the PC for program controlled branching.

Branching can also be controlled by an external device during input-output operations. This feature allows I/O controlled vectored interrupts.

MEMORY ADDRESS REGISTER (MAR)

The MAR contains the address of the memory location that is currently selected for memory or I/O read-write operations. It is also used for microprogram control during data transfers to and from memory and peripherals.

INSTRUCTION REGISTER (IR)

The instruction fetched from memory is held in the IR while being interpreted by the Instruction Decoder. The IR specifies the initial step of the microprogram sequence for each instruction and is also used to store temporary data for microprogram control.

ARITHMETIC AND LOGIC UNIT (ALU)

2

The ALU performs 12-bit arithmetic, logical and rotate operations. Its input is derived from the AC and any one of the other CPU registers. The type of operations performed by the ALU include:

ADD	Left-right shifts and rotates
Logical AND	Increment
Logical OR	Complement
Test AC	Set/Clear

DX-BUS MULTIPLEXER

To keep the CPU pin count to a reasonable 40 and still maintain a 12-bit word structure, the address and data paths are multiplexed by the DX-Bus Multiplexer. It handles data, address and instruction transfers between the CPU and memory or peripheral devices on a time-multiplexed basis.

TIMING AND CONTROL UNIT

The Timing and Control Unit generates the state and cycle timing signals from a single-phase clock and maintains the proper sequences of events required for any processing task. It also decodes the instruction obtained from the IR and combines the result with various timing signals and external control inputs to provide control and gating signals required by other functional units (both internal and external to the CPU).

Memory Organization

The HM-6100 has a basic addressing capacity of 4096 12-bit words. The addressing capacity may be extended to 32K words by Extended Memory Control hardware. Every location has a unique 4 digit octal (12 bit binary) address, 0000_8 to 7777_8 (0000_{10} to 4095_{10}). The Memory is subdivided into 32 PAGES of 128 words each. Memory Pages are numbered sequentially from Page 00_8, containing addresses 0000-0177_8, to Page 37_8, containing addresses 7600_8-7777_8. The first 5 bits of a 12-bit MEMORY ADDRESS denote the PAGE NUMBER and the low order 7 bits specify the PAGE ADDRESS of the memory location within the given Page.

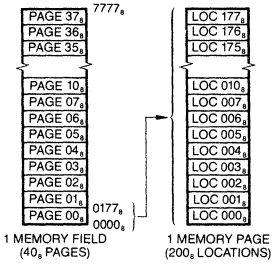


FIGURE 3 – Memory Organization

The HM-6100 instructions are 12-bit words stored in memory. The HM-6100 makes no distinction between instruction and data; it can manipulate instructions as stored variables or execute data as instructions. There are three general classes of HM-6100 instructions. They are Memory Reference Instructions (MRI), Operate Instructions (OPR), and Input/Output Transfer Instructions (IOT).

During an instruction fetch cycle, the HM-6100 fetches the instruction pointed to by the PC. The contents of the PC are transferred to the MAR. The PC is incremented by 1. The PC now contains the address of the "current" instruction which must be fetched from memory. Bits 0-4 of the MAR identify the CURRENT PAGE, that is, the Page from which instructions are currently being fetched and bits 5-11 of the MAR identify the location within the Current Page. (PAGE ZERO (0), 0000_8-0177_8, by definition, denotes the first 128 words of memory and is called the Register Page.)

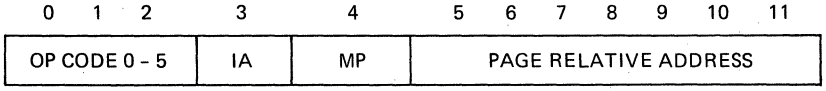
Since the HM-6100 is a static design it can operate at any crystal frequency from 0 to 8MHz. State times required for execution are given for each instruction. Execution time can be calculated from the equation:

$$T = N*(2*(1/F))$$

where N is the number of state times and F is the crystal or input clock frequency.

MEMORY REFERENCE INSTRUCTIONS (MRI)

The Memory Reference Instructions operate on the contents of a memory location or use the contents of a memory location to operate on the AC or the PC. The first 3 bits of a Memory Reference Instruction specify the operation code, or OPCODE, and the low order 9 bits, the OPERAND address, as shown in Figure 4.



IA: Indirect Addressing 0 = Direct; 1 = Indirect
MP: Memory Page 0 = Register Page; 1 = Current Page

FIGURE 4 – Memory Reference Instruction Format

Bits 5 through 11, the PAGE ADDRESS, identify the location of the OPERAND on a given page, but they do not identify the page itself. The page is specified by bit 4, called the CURRENT PAGE OR REGISTER PAGE BIT. If bit 4 is a 0, the page address is interpreted as a location on the Register Page. If bit 4 is a 1, the page address specified is interpreted to be on the Current Page.

By this Method, 256 locations may be directly addressed, 128 on the REGISTER PAGE and 128 on the CURRENT PAGE. Other locations are addressed by using bit 3. When bit 3 is a 0, the operand address is a DIRECT ADDRESS. An INDIRECT ADDRESS (pointer address) identifies the location that contains the desired address (effective address). To address a location that is not directly addressable, not in the REGISTER PAGE or in the CURRENT PAGE, the absolute address of the desired location is stored in one of the 256 directly addressable locations (pointer address). Upon execution, the MRI will operate on the contents of the location identified by the address contained in the pointer location. Note that locations 0010_8-0017_8 in the Register Page are AUTOINDEXED. When these locations are used for index registers their contents are incremented by 1 and restored before they are used as the operand address. These locations are therefore convenient for indexing applications.

Combinations of mode and page bits yield four (4) addressing modes:

- Current Page, Direct
- Current Page, Indirect
- Register Page, Direct
- Register Page, Indirect

A fifth addressing mode results from use of the AUTOINDEX registers:

- Register Page, Autoindexed

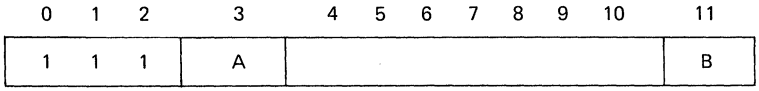
TABLE 1

MNE-MONIC	OP CODE	NUMBER OF STATES			OPERATION
		DIRECT	INDIRECT	AUTO-INDEXED	
AND	0XXX	10	15	16	LOGICAL AND: Causes a bit-by-bit boolean AND between the contents of the Accumulator and the contents of the effective address (XXX) specified by the instruction. The result is left in the AC and the data word in the referenced location is not altered.
TAD	1XXX	10	15	16	TWO'S COMPLEMENT ADD: Performs a binary two's complement addition between the specified data word and the contents of the AC; the result is left in the AC. If a carry out occurs, the state of the Link is complemented. If the AC is initially cleared, this instruction acts as a LOAD from memory.
ISZ	2XXX	16	21	22	INCREMENT AND SKIP IF ZERO: The contents of the effective address are incremented by 1 and restored. If the result is zero, the next sequential instruction is skipped.
DCA	3XXX	11	16	17	DEPOSIT AND CLEAR THE ACCUMULATOR: The contents of the AC are stored in the effective address and the AC is cleared.
JMS	4XXX	11	16	17	JUMP TO SUBROUTINE: The contents of the PC are stored in the effective address and the effective address + 1 is stored in the PC. The link, AC, and MQ are unchanged.
JMP	5XXX	10	15	16	JUMP: The effective address is loaded into the PC thus causing program execution to branch to a new location.
IOT	6XXX	17			INPUT/OUTPUT TRANSFER: Used to initiate the operation of peripheral devices and to transfer data between the peripherals and the CPU.
OPI	7XXX				OPERATE Instructions: Used to perform logical operations on the contents of the major registers.
		10			2 - Cycle OPERATE
		15			3 - Cycle OPERATE

Operate Instructions

The Operate Instructions, which have an OPCODE of 7_8(111), consist of 3 groups of microinstructions. Group 1 microinstructions, which are identified by the presence of a 0 in bit 3, are used to perform logical operations on the contents of the accumulator and link. Group 2 micro instructions, which are identified by the presence of a 1 in bit 3 and a 0 in bit 11, are used primarily to test the contents of the accumulator and then conditionally skip the next sequential instruction. Group 3 microinstructions have a 1 in bit 3 and a 1 in bit 11 and are used to perform logical operations on the contents of the AC and MQ.

The basic OPR instruction format is shown in Figure 5. Operate microinstructions from any group may be microprogrammed with other operate microinstructions of the same group. The actual code for a microprogrammed combination of two, or more, microinstructions is the bitwise logical OR of the octal codes for the individual microinstructions. When more than one operation is microprogrammed into a single instruction, the operations are performed in a prescribed sequence, with logical sequence number 1 microinstructions performed first, logical sequence number 2 microinstructions performed second, logical sequence number 3 microinstructions performed third, and so on. Two operations with the same logical sequence number, within a given group of microinstructions, are performed simultaneously.

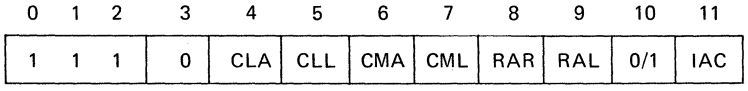


MICROINSTRUCTION	A	B
Group 1	0	0/1
Group 2	1	0
Group 3	1	1

FIGURE 5 – Basic OPR Instruction Format

GROUP 1 MICROINSTRUCTIONS

Figure 6 shows the instruction format of a group 1 microinstruction. Any one of bits 4 to 11 may be set, loaded with a binary 1, to indicate a specific group 1 microinstruction. If more than one of these bits is set, the instruction is a microprogrammed combination of group 1 microinstructions, which will be executed according to the logical sequence shown in Figure 6.



Logical Sequences:
1- CLA CLL
2 - CMA CML
3 - IAC
4 - RAR RAL RTR RTL BSW

BIT 8	BIT 9	BIT 10	FUNCTION
0	0	1	BSW
0	1	0	RAL
0	1	1	RTL
1	0	0	RAR
1	0	1	RTR

FIGURE 6 – Group 1 Microinstruction Format

Table 2-1 lists commonly used group 1 microinstructions, their assigned mnemonics, octal number, instruction format, logical sequence, the operation they perform, and the number of states. The same format is followed in Table 3 and 4 which corresponds to group 2 and 3 microinstructions, respectively.

There are several commonly used microprogrammed combinations of group 1 microinstructions. These are listed in Table 2-2. When writing programs it is necessary to load various constants into the AC for such purposes as initiallizing counters and to provide comparisons. Table 2-3 lists those constants which can be loaded directly via microprogrammed combinations of group 1 instructions.

TABLE 2 - 1

MNE-MONIC	OCTAL CODE	LOGICAL SEQUENCE	NUMBER OF STATES	OPERATION
NOP	7000	1	10	NO OPERATION - This instruction causes a 10 state delay in program execution, without affecting the state of the HM-6100. It may be used for timing synchronization or as a convenient means of deleting an instruction from a program.
CLA	7200	1	10	CLEAR ACCUMULATOR - The accumulator is loaded with binary 0's.

FIGURE 2 - 1 Continued

MNE-MONIC	OCTAL CODE	LOGICAL SEQUENCE	NUMBER OF STATES	OPERATION
CLL	7100	1	10	CLEAR LINK - The link is loaded with a binary 0.
CMA	7040	2	10	COMPLEMENT ACCUMULATOR - The content of each bit of the AC is complemented. This has the effect of replacing the contents of the AC with its one's complement.
CML	7020	2	10	COMPLEMENT LINK - The content of the link is complemented.
IAC	7001	3	10	INCREMENT ACCUMULATOR - The content of the AC is incremented by one (1) and the carry out componments the Link (L).
BSW	7002	4	15	BYTE SWAP - The right six (6) bits of the AC are exchanged or SWAPPED with the left six bits. AC(0) is swapped with AC(6), AC(1) with AC(7), etc. The link is not affected.
RAL	7004	4	15	ROTATE ACCUMULATOR LEFT - The content of the AC and L are rotated one binary position to the left. AC(0) is shifted to L and L is shifted to AC(11). The ROTATE instructions use what is commonly called a circular shift, meaning that any bit rotated off one end of the accumulator will reappear at the other end.
RTL	7006	4	15	ROTATE TWO LEFT - The contents of the AC and L are rotated two binary positions to the left. AC(1) is shifted to L and L is shifted to AC(10).
RAR	7010	4	15	ROTATE ACCUMULATOR RIGHT - The contents of the AC and L are rotated one binary position to the right. AC(11) is shifted to L and L is shifted to AC(0).
RTR	7012	4	15	ROTATE TWO RIGHT - The contents of the AC and L are rotated two binary positions to the right. AC(10) is shifted to L and L is shifted to AC(1).

2

TABLE 2 - 2

MNE-MONIC	OCTAL CODE	LOGICAL SEQUENCE	NUMBER OF STATES	OPERATION
CLA CLL	7300	1	10	CLEAR ACCUMULATOR - CLEAR LINK
CIA	7041	2, 3	10	COMPLEMENT AND INCREMENT ACCUMULATOR - The content of the AC is replaced with its two's complement. The carry out complements the link. This is a microprogrammed combination of CMA and IAC.
STL	7120	1, 2	10	SET THE LINK - The LINK is loaded with a binary 1 corresponding with a microprogrammed combination of CLL and CML.
STA	7240	1, 2	10	SET THE ACCUMULATOR - Each bit of the AC is set to 1 corresponding to a microprogrammed combination of CLA and CMA.
CLA IAC	7201	1, 3	10	Sets the accumulator to a 1.

TABLE 2 - 2 Continued

MNE-MONIC	OCTAL CODE	LOGICAL SEQUENCE	NUMBER OF STATES	OPERATION
GLK	7204	1, 4	15	GET LINK - The AC is cleared and the content of the link is shifted into AC(11) while a 0 is shifted into the link. This is a microprogrammed combination of CLA and RAL.
CLL RAL	7104	1, 4	15	CLEAR LINK - ROTATE ACCUMULATOR LEFT
CLL RTL	7106	1, 4	15	CLEAR LINK - ROTATE TWO LEFT
CLL RAR	7110	1, 4	15	CLEAR LINK - ROTATE ACCUMULATOR RIGHT
CLL RTR	7112	1, 4	15	CLEAR LINK - ROTATE TWO RIGHT

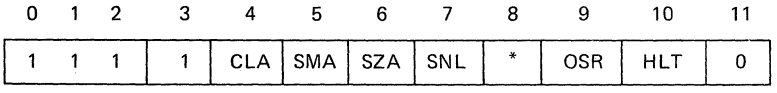
TABLE 2 - 3

MNEMONIC	OCTAL CODE	LOGICAL SEQUENCE	NUMBER OF STATES	DECIMAL CONSTANT	INSTRUCTIONS COMBINED
NL0000	7300	1	10	0	CLA CLL
NL0001	7301	1, 3	10	1	CLA CLL IAC
NL0002	7305	1, 3, 4	15	2	CLA CLL IAC RAL
NL0003	7325	1, 2, 3, 4	15	3	CLA CLL CML IAC RAL
NL0004	7307	1, 3, 4	15	4	CLA CLL IAC RTL
NL0006	7327	1, 2, 3, 4	15	6	CLA CLL CML IAC RTL
NL0100	7303	1, 3, 4	15	64	CLA CLL BSW
NL2000	7332	1, 2, 4	15	1024	CLA CLL CML RTR
NL3777	7350	1, 2, 4	15	2047	CLA CLL CMA RAR
NL4000	7330	1, 2, 4	15	-0	CLA CLL CML RAR
NL5777	7352	1, 2, 4	15	-1025	CLA CLL CMA RTL
NL6000	7333	1, 2, 3, 4	15	-1024	CLA CLL CML IAC RTL
NL7775	7346	1, 2, 4	15	-3	CLA CLL CMA RTL
NL7776	7344	1, 2, 4	15	-2	CLA CLL CMA RAL
NL7777	7340	1, 2	10	-1	CLA CLL CMA

2

GROUP 2 MICROINSTRUCTIONS

Figure 7 shows the instruction format of group 2 microinstructions, Bits 4 - 10 may be set to indicate a specific group 2 microinstruction. If more than one of bits 4 - 7 or 9 - 10 is set, the instruction is a microprogrammed combination group 2 microinstructions, which will be executed according to the logical sequence shown in Figure 7.



Logical Sequences:
1 (BIT 8 = 0) -SMA or SZA or SNL
(BIT 8 = 1) -SPA or SNA or SZL
2 -CLA
3 -OSR, HLT

* Reverse sensing BIT:
Unconditional SKIP when
BITS 5, 6, & 7 are 0's

FIGURE 7 — Group 2 Microinstruction Format

Skip microinstructions may be microprogrammed with CLA, OSR, or HLT microinstructions. Skip microinstructions which have a 0 in bit 8, however, may not be microprogrammed with skip microinstructions which have a 1 in bit 8. When two or more skip microinstructions are microprogrammed into a single instruction, the resulting condition on which the decision will be based is the logical OR of the individual conditions when bit 8 is 0, or when bit 8 is 1, the decision will be based on the logical AND.

TABLE 3 -1

MNE-MONIC	OCTAL CODE	LOGICAL SEQUENCE	NUMBER OF STATES	OPERATION
NOP	7400	1	10	NO OPERATION - See Group 1 microinstructions.
CLA	7600	2	10	CLEAR ACCUMULATOR - The accumulator is loaded with binary O's.
HLT	7402	3	10	HALT - Program stops at the conclusion of the current machine cycle. If HLT is combined with others in OPR 2, the other operations are completed before the end of the cycle.
SKP	7410	1	10	SKIP - The content of the PC is incremented by 1, to skip the next instruction.
SNL	7420	1	10	SKIP ON NON-ZERO LINK - The content of L is sampled; the next sequential instruction is skipped if L contains a 1. If L contains a 0, the next instruction is executed.
SZL	7430	1	10	SKIP ON ZERO LINK - The instruction is skipped if the link contains a 0.
SZA	7440	1	10	SKIP ON ZERO ACCUMULATOR - The content of the AC is sampled; the next sequential instruction is skipped if all AC bits are 0. If any bit in the AC is a 1, the next instruction is executed.
SNA	7450	1	10	SKIP ON NON-ZERO ACCUMULATOR - The next instruction is skipped if any one bit of the AC contains a 1. If every bit in the AC is 0, the next instruction is executed.
SMA	7500	1	10	SKIP ON MINUS ACCUMULATOR - If the content of AC(0) contains a negative two's complement number, the next sequential instruction is skipped. If AC(0) contains a 0, the next instruction is executed.
SPA	7510	1	10	SKIP ON POSITIVE ACCUMULATOR - If the content of AC(0) contains a 0, indicating a positive two's complement number, the next sequential instruction is skipped.
OSR	7404	3	15	OR WITH SWITCH REGISTER - The content of the Switch Register is inclusively OR'ed with the content of the AC and the result stored in the AC. The HM-6100 sequences the OSR instruction through a 2-cycle execute phase referred to as OPR 2A and OPR 2B. This instruction provides the simplest way to input data to the HM-6100 from peripherals.
LAS	7604	1, 3	15	LOAD ACCUMULATOR WITH SWITCH REGISTER - The content of the AC is loaded with the content of the SR, bit for bit. This is equivalent to a microprogrammed combination of CLA and OSR.

Table 3 - 2 lists every legal combination of skip microinstructions, along with the resulting condition upon which the decision to skip or execute the next sequential instruction is based. When these combinations include a CLA, the accumulator is cleared after the decision is made. This is a useful trick to save code when a new value will be TAD'ed into the AC.

TABLE 3 - 2

MNEMONIC	OCTAL CODE	LOGICAL SEQUENCE	NUMBER OF STATES	OPERATION
SZA SNL	7460	1	10	Skip if AC = 0 or L = 1 or both.
SNA SZL	7470	1	10	Skip if AC ≠ 0 and L = 0.
SMA SNL	7520	1	10	Skip if AC < 0 or L = 1 or both.
SPA SZL	7530	1	10	Skip if AC ≥ 0 and L = 0
SMA SZA	7540	1	10	Skip if AC ≤ 0.
SPA SNA	7550	1	10	Skip if AC > 0.
SMA SZA SNL	7560	1	10	Skip if AC ≤ 0 or L = 1 or both.
SPA SNA SZL	7570	1	10	Skip if AC > 0 and L = 0.

When writing an actual program, it is useful to think in terms of the FORTRAN relational operators - .LT., .EQ., etc.- when trying to compare numbers. The following method along with Table 3 - 3 will provide this.

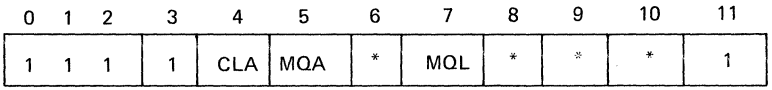
```
CLA CLL                 /Initialize AC and LInk
TAD B                   /Fetch 2nd number
CML CMA IAC             /Create "-B" (AC & L act like a 13 bit accumulator)
TAD A                   /Fetch 1st number
Test <CLA>              /Use instructions from Table 3 - 3 to provide test
                        /The CLA is optional to provide a clear AC after test
JMP FAIL                /Branch to FAIL routine if test failed
. . .                   /Test passed, continue with program
. . .
```

TABLE 3 - 3

SKIP IF	UNSIGNED COMPARE	SIGNED COMPARE
A .NE. B	SNA	SNA
A .LT. B	SNL	SMA
A .LE. B	SNL SZA	SMA SZA
A .EQ. B	SZA	SZA
A .GE. B	SZL	SPA
A .GT. B	SZL SNA	SPA SNA

GROUP 3 MICROINSTRUCTIONS

Figure 8 shows the instruction format of group 3 microinstructions which requires bits 3 and 11 to contain a 1. Bits 4, 5 or 7 may be set to indicate a specific group 3 microinstruction. If more than one of the bits is set, the instruction is a microprogrammed combination of group 3 microinstructions following the logical sequence listed in Figure 8.



Logical Sequences:
1 - CLA
2 - MQA, MQL
3 - NOP

* Don't care

FIGURE 8 — Group 3 Microinstruction Format

TABLE 4

MNE-MONIC	OCTAL CODE	LOGICAL SEQUENCE	NUMBER OF STATES	OPERATION
NOP	7401	3	10	NO OPERATION - See group 1 microinstructions.
CLA	7600	1	10	CLEAR ACCUMULATOR
MQA	7501	2	10	MQ REGISTER INTO ACCUMULATOR - The content of the MQ is logical OR'ed with the content of the AC and the result is loaded into the AC. The original content of the AC is lost but the original content of the MQ is retained. This instruction provides the programmer with an inclusive OR operation.
MQL	7421	2	10	MQ REGISTER LOAD - The content of the aAC is loaded into the MQ, the AC is cleared and the original content of the MQ is lost. This is similar to a DCA instruction.
ACL	7701	1, 2	10	CLEAR ACCUMULATOR AND LOAD MQ REGISTER INTO ACCUMULATOR - This is equivalent to a microprogrammed combination of CLA and MQA. It is similar to the two instruction combination of CLA and TAD.
CAM	7621	1, 2	10	CLEAR ACCUMULATOR AND MQ REGISTER - The content of the AC and MQ are loaded with binary 0's. This is equivalent to a microprogram combination of CLA and MQL.
SWP	7521	2	10	SWAP ACCUMULATOR AND MQ REGISTER - The content of the AC and MQ are interchanged by accomplishing a microprogrammed combination of MQA and MQL.
CLA SWP	7721	1, 2	10	CLEAR ACCUMULATOR AND SWAP ACCUMULATOR AND MQ REGISTER - The content of the AC is cleared. The content of the MQ is loaded into the AC and the MQ is cleared.

2

Input Output Transfer Instructions (IOT)

The input/output transfer instructions, which have an OPCODE of 6_8 are used to initiate the operation of peripheral devices and to transfer data between peripherals and the HM-6100. Three types of data transfer may be used to receive or transmit information between the HM-6100 and one or more peripheral I/O devices. PROGRAMMED DATA TRANSFER provides a straightforward means of communicating with relatively slow I/O devices, such as Teletypes, cassettes, card readers and CRT displays. INTERRUPT TRANSFERS use the interrupt system to service several peripheral devices simultaneously, on an intermittent basis, permitting computational operations to be performed concurrently with the data I/O operations. Both Programmed Data Transfers and Program Interrupt Transfers use the accumulator as a buffer, or storage area, for all data transfers. Since data may be transferred only between the accumulator and the peripheral, only one 12 bit word at a time may be transferred. DIRECT MEMORY ACCESS, DMA, Transfers variable-size blocks of data between high-speed peripherals and the memory with minimum of program control required by the HM-6100.

IOT INSTRUCTION FORMAT

The Input/Output Transfer instruction format is represented in Figure 9.

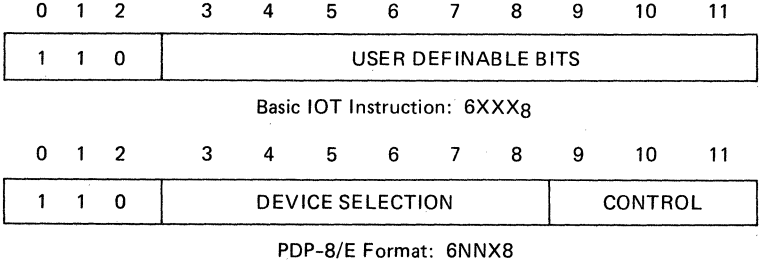


FIGURE 9 — IOT Instruction Format

The first three bits, 0 - 2, are always set to 6$_8$ (110) to specify an IOT instruction. The next 9 bits, 3 - 11, are user definable and can provide a minimal implementation when each bit controls one operation. When following PDP-8/E format, the next six bits, 3 - 8, contain the device selection code that determines the specific I/O device for which the IOT instruction is intended and, therefore, permit interface with up to 64 I/O devices. The last three bits, 9 - 11, contain the operation specification code that determines the specific operation to be performed. The nature of this operation for any given IOT instruction depends entirely upon the circuitry designed into the I/O device interface.

PROGRAMMED DATA TRANSFER

Programmed Data Transfer is the easiest, simplest, most convenient and most common means of performing data I/O. For microprocessor applications, it may also be the most cost effective approach. The data transfer begins when the HM-6100 fetches an instruction from the memory and recognizes that the current instruction is an IOT (2). This is referred to an IFETCH and consists of five (5) internal states. The HM-6100 sequences the IOT instruction through a 2-cycle execute phase referred to as IOTA and IOTB. Bits 0 - 11 of the IOT instruction are available on DX0 - 11 at IOTA ∧ LXMAR (3). These bits must be latched in an external address register. $\overline{\text{DEVSEL}}$ is active low to enalbe data transfers between the HM-6100 and the peripheral device (4) & (5). Input-Output Instruction Timing is shown in Figure 10. The selected peripheral device communicates with the HM-6100 through 4 control lines - $\overline{\text{C0}}$, $\overline{\text{C1}}$, $\overline{\text{C2}}$ and $\overline{\text{SKP}}$. In the HM-6100 the type of data transfer, during an IOT instruction, is specified by the peripheral device(s) by asserting the control lines as shown in Tables 5-1 and 5-2.

The control line $\overline{\text{SKP}}$, when low during an IOT, causes the HM-6100 to skip the next sequential instruction. This feature is used to sense the status of various signals in the device interface. The C0, C1, and C2 lines are treated independently of the $\overline{\text{SKP}}$ line. In the case of a RELATIVE or ABSOLUTE JUMP, the skip operation is performed after the jump. The input signals to the HM-6100, DX0 - 11, $\overline{\text{C0}}$, $\overline{\text{C1}}$, $\overline{\text{C2}}$ and $\overline{\text{SKP}}$, are sampled during IOTA on the rising edge of time state 3 (4). The data from the HM-6100 is available to the device during $\overline{\text{DEVSEL}}$ ∧ $\overline{\text{XTC}}$ (5). The IOTB cycle is internal to the HM-6100 to perform the operations requested during IOTA. Both IOTA and IOTB consists of six (6) internal states.

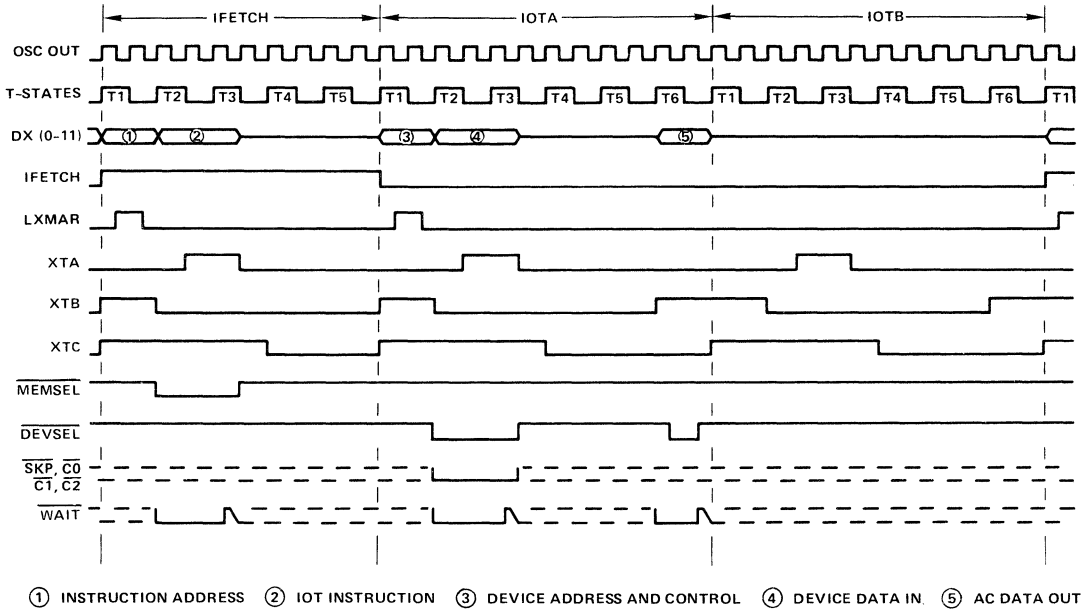


FIGURE 10 – Input-output instruction timing

TABLE 5 - 1
AC DATA TRANSFERS

CONTROL LINES				OPERATION	DESCRIPTION
$\overline{SKP}$	$\overline{C0}$	$\overline{C1}$	$\overline{C2}$		
H	H	H	H	DEV ← AC	The content of the AC is sent to the device.
H	L	H	H	DEV ← AC; CLA	The content of the AC is sent to a device and then the AC is cleared.
H	H	L	H	AC ← AC V DEV; DEV ← AC	Data is received from a device OR'ed with the data in the AC and the result is stored in the AC. The new AC content is sent to the device.
H	L	L	H	AC ← DEV; DEV ← AC	Data is received from a device and loaded into the AC. The new AC content is sent to the device.
L	H	H	H	DEV ← AC; PC ← PC + 1	The content of the AC is sent to the device and the microprocessor skips the next sequential instruction.
L	L	H	H	DEV ← AC; CLA; PC ← PC + 1	The content of the AC is sent to a device, the AC is cleared, and the microprocessor skips the next sequential instruction.
L	H	L	H	AC ← AC V DEV; DEV ← AC; PC ← PC + 1	Data is OR'ed into the AC, the new AC sent to the device, and the microprocessor skips the next sequential instruction.
L	L	L	H	AC ← DEV; DEV ← AC PC ← PC + 1	Data is loaded into the AC, the new AC contents sent to the device, and the next sequential instruction skipped.

TABLE 5 - 2
PC VECTOR TRANSFERS

CONTROL LINES				OPERATION	DESCRIPTION
$\overline{SKP}$	$\overline{C0}$	$\overline{C1}$	$\overline{C2}$		
H	*	H	L	PC ← PC + DEV	Data from the device is added to the contents of the PC. This is referred to as a RELATIVE JUMP.
H	*	L	L	PC ← DEV	Data is received from a device and loaded into the PC. This is referred to as an ABSOLUTE JUMP.
L	*	H	L	PC ← PC + DEV; PC ← PC + 1	The RELATIVE JUMP is performed and then the microprocessor skips the next sequential instruction.
L	*	L	L	PC ← DEV; PC ← PC + 1	The ABSOLUTE JUMP is executed and then the next sequential instruction is skipped.

* Don't Care

PROGRAM INTERRUPT TRANSFERS

The program interrupt system may be used to initiate programmed data transfers in such a way that the time spent waiting for device status is greatly reduced or eliminated altogether. It also provides a means of performing concurrent programmed data transfers between the HM-6100 and the peripheral devices. This is accomplished by isolating the I/O handling routines from the mainline program and using the interrupt system to ensure that these routines are entered only when an I/O device status is set, indicating that the device is actually ready to perform the next data transfer, or that is requires some sort of intervention from the running program.

TABLE 6
PROCESSOR IOT INSTRUCTIONS

MNE-MONIC	OCTAL CODE	OPERATION
SKON	6000	SKIP IF INTERRUPT ON - If Interrupt system is enabled, the next sequential instruction is skipped. The Interrupt system is disabled.
ION	6001	INTERRUPT TURN ON - The internal interrupt acknowledge system is enabled. The interrupt system is enabled after the CPU executes the next sequential instruction.
IOF	6002	INTERRUPT TURN OFF - The interrupt system is disabled. Note that the interrupt system is automatically disabled when the CPU acknowledges an INT request.
SRQ	6003	SKIP IF INT REQUEST - The next sequential instruction is skipped if the INT request bus is low.
GTF	6004	GET FLAGS - The following machines states are read into the indicated bits of AC. bit 0 - Link bit 1 - Greater than flag* bit 2 - INT request bus bit 3 - Interrupt Inhibit FF* bit 4 - Interrupt Enable FF* bit 5 - User flag* bit 6 - 11 - Save Field Register* * These bits are modified by external devices driving the DX bus and the $\overline{C}$-lines ($\overline{C0}$ = L, $\overline{C1}$ = L). For example, bits 1 and 6 - 11 are part of the Extended Memory Control.
RTF	6005	RETURN FLAGS - Link is restored from AC (0). Interrupt system is enabled after the next sequential instruction is executed. All AC bits are available externally to restore external states. (ex. Extended memory control). ($\overline{C0}$ = H, $\overline{C1}$ = H)
SGT	6006	SKIP ON GREATER THAN FLAG - Operation is determined by external devices, if any. This flag is external and must control the skip line.
CAF	6007	CLEAR ALL FLAGS - AC and link are cleared. Interrupt system is disabled.

The interrupt system allows certain external conditions to interrupt the computer program by driving the $\overline{\text{INTREQ}}$ input to the HM-6100 low. If no higher priority requests are outstanding and the interrupt system is enabled, the HM-6100 grants the device interrupt at the end of the current instruction. After an interrupt has been granted, the Interrupt Enable Flip-Flop in the HM-6100 is reset so that no more interrupts are acknowledged until the interrupt system is re-enabled under program control.

The current content of the Program Counter, PC, is deposited in location 0000_8 of the memory and the program fetches the instruction from location 0001_8. The return address is available in location 0000_8. This address must be saved, possibly in a software stack, if nested interrupts are permitted. The INTGNT signal is activated by the HM-6100 when a device interrupt is acknowledged. This signal is reset by executing any IOT instruction. The INTGNT is also useful in implementing an External Vectored Priority Interrupt network.

The user program controls the interrupt mechanism of the HM-6100 by executing the processor IOT instructions listed in Table 6. Several of these interrupt IOT instructions are also used if the memory is extended beyond 4K words.

DIRECT MEMORY ACCESS (DMA)

Direct Memory Access, sometimes called data break, is the perferred form of data transfer for use with high-speed storage devices such as magnetic disk or tape units. The DMA mechanism transfers data directly between memory and peripheral devices. The HM-6100 is involved only is setting up the transfer; the transfers take place with no processor intervention on a "cycle stealing" basis. The DMA transfer rate is limited only by the bandwidth of the memory and the data transfer characteristics of the device.

The device generates a DMA Request when it is ready to transfer data. The HM-6100 grants the $\overline{\text{DMAREQ}}$ by activating the DMAGNT signal at the end of the current instruction. The HM-6100 suspends any further instruction fetches until the $\overline{\text{DMAREQ}}$ line is released. The DX lines are tri-stated, all SEL lines are high, and the external timing signals XTA, XTB, and XTC are active. The device which generated the $\overline{\text{DMAREQ}}$ must provide the address and necessary control signals to the memory for data transfers. The $\overline{\text{DMAREQ}}$ line can also be used as a level sensitive "pause" line.

Control Panel Interrupt Transfer

The HM-6100 CPU provides a unique Control Panel (CP) feature through its $\overline{\text{CPREQ}}$ input and $\overline{\text{CPSEL}}$ output lines. After acknowledging the control panel request, the CPU generates the necessary timing to execute program code in CP memory while also providing the capability to transfer data between CP memory and the user memory using the AC as a buffer. This allows the user memory to be examined and/or modified by the CP software. The CPU will output the $\overline{\text{MEMSEL}}$ signal for all user memory references while the $\overline{\text{CPSEL}}$ signal is generated for CP memory references as shown in Figure 11.

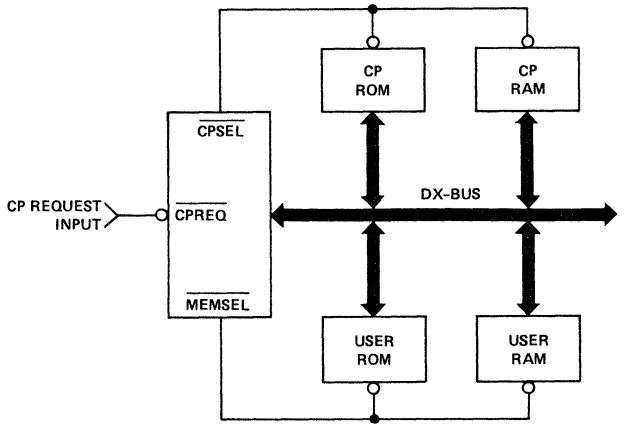


FIGURE 11 – Control Panel Block Diagram

The designer can make use of the control panel features to implement various functions that will be "transparent" to the user's (main) memory. Some of the more common functions include:

- Binary Loader and Punch
- Register Examination and Modification
- Single Cycle
- Octal Debug with Breakpoints
- Octal listing
- Auto Bootstrap

When a $\overline{\text{CPREQ}}$ is granted the PC is stored in location 0000 of Panel Memory and the HM-6100 resumes operation at location 7777 of the Panel Memory. The $\overline{\text{CPREQ}}$ bypasses the interrupt enable system and the processor IOT instruction, ION and IOF, are ignored while the HM-6100 is in the Control Panel Mode. Once a $\overline{\text{CPREQ}}$ is granted, the HM-6100 will not recognize any $\overline{\text{DMAREQ}}$ or $\overline{\text{INTREQ}}$ until the CPREQ has been fully serviced.

During Control Panel program execution access to the user memory is gained through use of indirect TAD, AND, DCA and ISZ instructions. The CPU will transfer control from $\overline{\text{CPSEL}}$ to $\overline{\text{MEMSEL}}$ during the execute phase of these instructions. The instructions are always fetched from control panel memory.

Exiting from the control panel routine is achieved by executing the following sequence:

- ION
- JMP I 0000 /Exit via location 0000 in Panel Memory

Location 0000 contains either the original return address deposited by the HM-6100 when the CP routine was entered, or it may be a new starting address defined by the CP routine.

Internal Priority Structure

After an instruction is completely sequenced, the major state generator scans the internal priority network as shown in in Figure 12. The state of the priority network decides the next sequence of the HM-6100.

The CPU samples the $\overline{\text{RESET}}$ line, the request lines $\overline{\text{CPREQ}}$, $\overline{\text{DMAREQ}}$, and $\overline{\text{INTREQ}}$, and the state of its internal RUN flip-flop during the last execute cycle of each instruction. The worst case response time of the HM-6100 to an external request is, therefore the time required to execute the longest instruction preceded by any 6-state execution cycle. For the HM-6100, this is an autoindexed ISZ, 22 states, preceded by any 6-state execution cycle instruction. The worst case response time is, therefore, 28 states, 14 μs at 4MHz clock frequency.

When the HM-6100 is initially powered up, the state of the timing generator is undefined. The generator is automatically initialized with a maximum of 34 clock pulses. The request inputs, as the HM-6100 is powered on, must span at least 58 clock pulses to be recognized, 34 clocks for the counter to initialize and a maximum of two HM-6100 cycles (20 to 24 clocks) for the state generator to sample the request lines. A positive transition of RUN/$\overline{\text{HLT}}$ should occur at least 10 clock pulses after $\overline{\text{RESET}}$ to be recognized.

The priority hierarchy is:

- $\overline{\text{RESET}}$ - If the $\overline{\text{RESET}}$ line is asserted at the sample time, the processor immediately sets its program counter to 7777, clears the Accumulator and Link, and puts the processor in the $\overline{\text{HALT}}$ state. While halted, the processor continues to cycle and generate the timing signals XTA, XTB, and XTC. During reset the DX line is tri-stated and the SEL lines are high.
- $\overline{\text{CPREQ}}$ - If the $\overline{\text{RESET}}$ line is not found to be asserted, but the $\overline{\text{CPREQ}}$ line is, the processor grants the control panel interrupt request at the end of the current cycle.
- RUN/$\overline{\text{HLT}}$ - If neither of the foregoing lines are asserted, but the processor finds its internal RUN FF in the halt state, it enters the HALT cycle at the end of the last execute cycle. Pulsing the RUN/$\overline{\text{HLT}}$ line low causes the HM-6100 to alternately run and halt. The internal RUN FF changes state on the rising edge of the RUN/$\overline{\text{HLT}}$ line. While halted the processor continues to generate the timing signals XTA, XTB, and XTC.
- $\overline{\text{DMAREQ}}$ - DMA requests are granted at the end of the current cycle only if none of the above actions are pending.
- $\overline{\text{INTREQ}}$ - An interrupt request is granted at the end of the current cycle only if none of the higher priority lines preempts it.
- IFETCH - If none of the above actions are indicated, the processor will fetch the next sequential instruction in the next cycle.

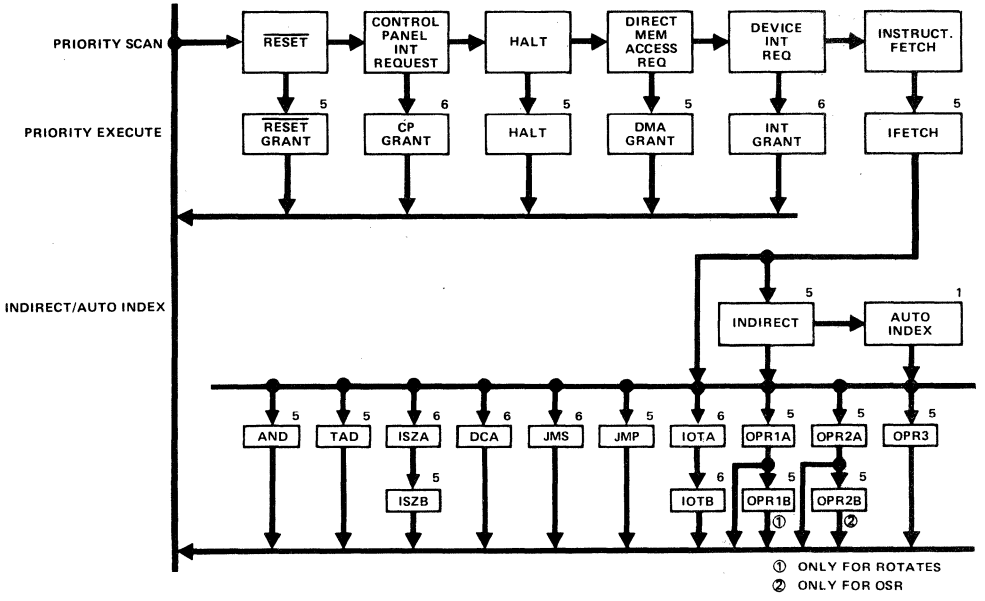


FIGURE 12 – Major processor states and number of clock cycles in each state.

Use of Wait Input

The HM-6100 samples the $\overline{\text{WAIT}}$ line during input-output data transfers. The $\overline{\text{WAIT}}$ line, if active low, controls the transfer duration. If $\overline{\text{WAIT}}$ is active during input transfers (READ), the CPU waits in the T2 state. For an output transfer (WRITE), $\overline{\text{WAIT}}$ controls the time for which the write data is maintained on the DX lines by extending the T6 state. When operating at the max frequency, the internal delay of the HM-6100 causes the falling edge select lines to be past the $\overline{\text{WAIT}}$ setup time for WRITE. The rising edge of the select line for READ can be used to activate $\overline{\text{WAIT}}$ for a WRITE. The wait duration is an integral multiple of the oscillator time period (Figure 13).

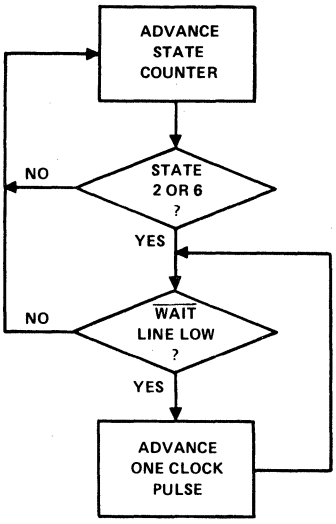


FIGURE 13 – WAIT sequencing steps.

HM-6100 Oscillator Requirements

USING AN EXTERNAL CRYSTAL

An inexpensive crystal can be used thereby eliminating the need for a clock generator. The crystal operates at parallel resonance, and thus is looks inductive in the circuit. An "AT" cut crystal should be used because it has a low temperature coefficient and can be used over a wide temperature range. The Feedback resistor and shunt capacitance are included internally. The crystal parameters needed are:

- Frequency
- Mod of Resonance - Parallel (anti-resonant)
- Maximum Power level - 1 milliwatt
- Load Capacitance - 32pF
- Series Resistance (max) - 250Ω

For precise frequency determination the effect of the stray circuit capacitance and internal 30pF capacitance must be taken into account.

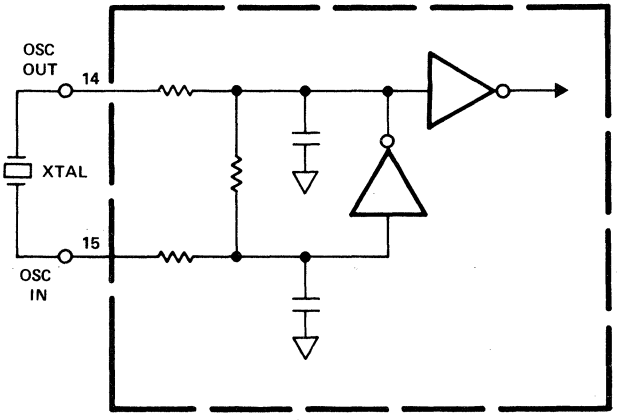


FIGURE 14 – Oscillator input schematic

USING AN EXTERNAL CLOCK GENERATOR

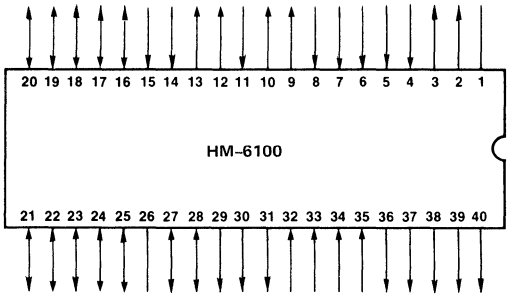
When a system clock is needed, eg. for a baud rate generator for UARTs, the HM-6100 can be externally clocked, thus eliminating the need for separate crystals. The external clock can be connected to the oscillator output pin while grounding oscillator input. This has the effect of over driving the small internal oscillator inverter causing an increase in supply current.

Duty cycle - 50/50
T_{rise}, T_{fall} - 20ns

PIN DEFINITIONS

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
1	VCC		Supply voltage.
2	RUN	H	The signal indicates the run state of the CPU and may be used to power down the external circuitry
3	DMAGNT	H	Direct Memory Access Grant—DX lines are three-state.
4	$\overline{\text{DMAREQ}}$	L	Direct Memory Access Request—DMA is granted at the end of the current instruction. Upon DMA grant, the CPU suspends program execution until the $\overline{\text{DMAREQ}}$ line is released.
5	$\overline{\text{CPREQ}}$	L	Control Panel Request—a dedicated interrupt which bypasses the normal device interrupt request structure.
6	RUN/$\overline{\text{HLT}}$	L	Pulsing the Run/Halt line causes the CPU to alternately run and halt by changing the state of the internal RUN/$\overline{\text{HLT}}$ flip flop.
7	$\overline{\text{RESET}}$	L	Clears the AC and loads 7777_8 into the PC. CPU is halted.
8	$\overline{\text{INTREQ}}$	L	Peripheral device interrupt request.
9	XTA	H	External coded minor cycle timing—signifies input transfers to the HM-6100.

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
10	LXMAR	H	The Load External Address Register is used to store memory and peripheral address externally.
11	$\overline{\text{WAIT}}$	L	Indicates that peripherals or external memory is not ready to transfer data. The CPU state gets extended as long as $\overline{\text{WAIT}}$ is active. The CPU is in the lowest power state with clocks running.
12	XTB	H	External coded minor cycle timing—signifies output transfers from the HM-6100.
13	XTC	H	External coded minor cycle timing—used in conjunction with the Select Lines to specify read or write operations.
14	OSC OUT		Crystal input to generate the internal timing (also external clock input).
15	OSC IN		See Pin 14—OSC OUT (also external clock ground)
16	DX0		DataX—multiplexed data in, data out and address lines.
17	DX1		See Pin 16—DX0.
18	DX2		See Pin 16—DX0.
19	DX3		See Pin 16—DX0.
20	DX4		See Pin 16—DX0.



PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
21	DX5		See Pin 16—DX0.
22	DX6		See Pin 16—DX0.
23	DX7		See Pin 16—DX0.
24	DX8		See Pin 16—DX0.
25	DX9		See Pin 16—DX0.
26	GND		Ground
27	DX10		See Pin 16—DX0.
28	DX11		See Pin 16—DX0.
29	LINK	H	Link flip flop.
30	$\overline{\text{DEVSEL}}$	L	Device Select for I/O transfers.
31	$\overline{\text{SWSEL}}$	L	Switch Register Select for the OR THE SWITCH REGISTER INSTRUCTION (OSR). OSR is a Group 2 Operate Instruction which reads a 12 bit external switch register and OR's it with the contents of the AC.
32	$\overline{\text{C0}}$	L	Control line inputs from the peripheral device during an I/O transfer (Table 5).

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
33	$\overline{\text{C1}}$	L	See Pin 32—C0.
34	$\overline{\text{C2}}$	L	See Pin 32—C0.
35	$\overline{\text{SKP}}$	L	Skips the next sequential instruction if active during an I/O instruction. (Table 5)
36	IFETCH	H	Instruction Fetch Cycle
37	$\overline{\text{MEMSEL}}$	L	Memory Select for memory transfers.
38	$\overline{\text{CPSEL}}$	L	The Control Panel Memory Select becomes active, instead of the $\overline{\text{MEMSEL}}$, for control panel routines. Signal may be used to distinguish between control panel and main memories.
39	INTGNT	H	Peripheral device Interrupt Grant
40	DATAF	H	Data Field pin indicates the execute phase of indirectly addressed AND, TAD, ISZ and DCA instructions so that the data transfers are controlled by the Data Field, DF, and not the Instruction Field, IF, if Extended Memory Control hardware is used to extend the addressing space from 4K to 32K words.

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HD-6101
CMOS PARALLEL INTERFACE ELEMENT (PIE)

Features

- HM-6100 COMPATIBLE
- LOW POWER TYP. $<5.0\mu W$ STANDBY
- SINGLE SUPPLY 4–11 VOLTS
- FULL TEMPERATURE RANGE −55°C TO +125°C
- STATIC OPERATION
- 4 PROGRAMMABLE OUTPUTS (FLAGS)
- 4 PROGRAMMABLE SENSE INPUTS
- CONTROL FOR TWO 12 BIT INPUT PORTS
- CONTROL FOR TWO 12 BIT OUTPUT PORTS
- PRIORITY VECTORED INTERRUPTS
- UP TO 31 PIE'S PER SYSTEM
- 16 INSTRUCTIONS FOR PIE CONTROL

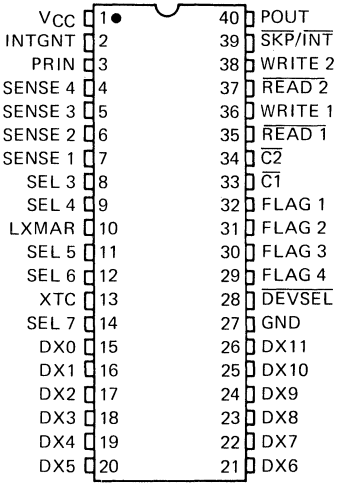
2

Description

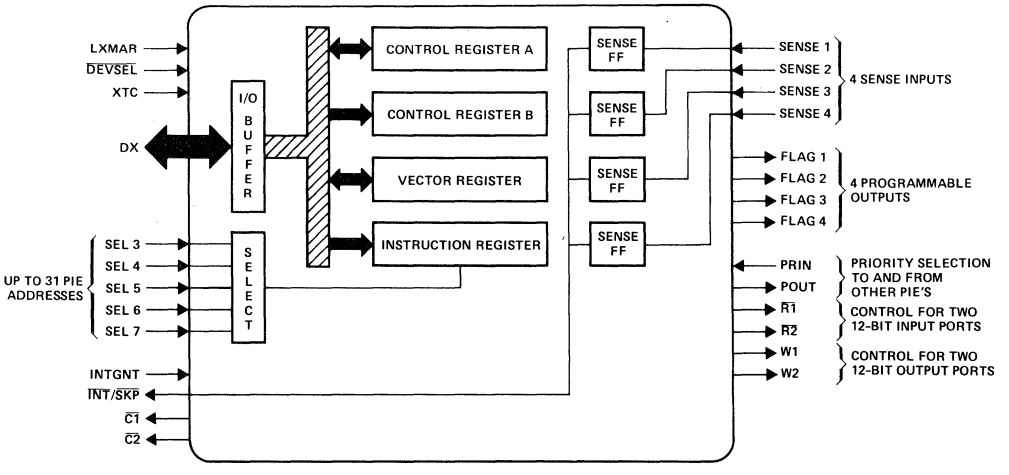
The HD-6101 Parallel Interface Elements (PIE) are high speed, low power, silicon gate CMOS general purpose devices which provide addressing interrupt and control for a variety of peripheral functions, such as UARTs, FIFOs, Keyboards, etc. Data transfers between the HM-6100 CMOS Microprocessor and the HD-6101 are via Input-Output Transfer (IOT) instructions, control lines and DX bus.

Data transfers between peripheral devices and the DX bus are controlled by the PIE via 2 read, 2 write, 4 sense and 4 flag functions. Internal PIE registers are programmed under software control for write polarities, sense levels or edges, flag values and interrupt enables. Another software controlled register stores the address for vectored interrupt operation.

Pinout



Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+12.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6101A-9	-40°C to +85°C
Military HD-6101A-2	-55°C to +125°C

ELECTRICAL CHARACTERISTICS

V_{CC} = 10.0 ±0.5 Volts; T_A = Industrial or Military

	SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	TEST CONDITIONS
D.C.	V_{IH}	Logical "1" Input Voltage	70% V_{CC}			V	
	V_{IL}	Logical "0" Input Voltage			20% V_{CC}	V	
	I_{IL}	Input Leakage	-1.0		+1.0	μA	$0V \leqslant V_{IN} \leqslant V_{CC}$
	V_{OH}	Logical "1" Output Voltage(1)	V_{CC} -2.0			V	I_{OH} = -0.2mA
	V_{OL}	Logical "0" Output Voltage			0.45	V	I_{OL} = 2.0mA
	I_O	Output Leakage	-1.0		+1.0	μA	$0V \leqslant V_O \leqslant V_{CC}$
	I_{CC}	Supply Current (Static)		1.0	800	μA	V_{IN} = V_{CC}, Freq. = 0
	C_I	Input Capacitance(2)		5	7	pF	
	C_O	Output Capacitance(2)		8	10	pF	
	C_{IO}	Input/Output Capacitance(2)		8	10	pF	

NOTES: (1) Except pins 33, 34, 39
(2) Guaranteed and sampled, but not 100% tested.

			T_A = 25°C V_{CC} = 10.0V(1)		T_A = INDUSTRIAL V_{CC} = 10 ±0.5V		T_A = MILITARY V_{CC} = 10 ±0.5V			
	SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	TEST CONDITIONS
A.C.	t_{DR}	Delay: $\overline{DEVSEL}$ to $\overline{READ}$		100		150		165	ns	C_L = 50pF
	t_{DW}	Delay: $\overline{DEVSEL}$ to WRITE	50	110	50	150	50	165	ns	See Timing
	t_{DF}	Delay: $\overline{DEVSEL}$ to FLAG		100		200		220	ns	Diagram
	t_{DC}	Delay: $\overline{DEVSEL}$ to $\overline{C1}$, $\overline{C2}$		105		215		240	ns	
	t_{DI}	Delay: $\overline{DEVSEL}$ to $\overline{SKP}/\overline{INT}$		105		215		240	ns	
	t_{DA}	Delay: $\overline{DEVSEL}$ to DX		175		215		240	ns	
	t_{LX}	LXMAR Pulse Width	100		120		135		ns	
	t_{AS}	Address Set-Up Time	30		40		45		ns	
	t_{AH}	Address Hold Time	50		50		55		ns	
	t_{DS}	Data Set-Up Time	40		65		70		ns	
	t_{DH}	Data Hold Time	50		50		55		ns	

NOTE (1): All devices guaranteed at worst case limits. Room temperature, 10V data provided for information — not guaranteed.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6101-9	-40°C to +85°C
Military HD-6101-2	-55°C to +125°C

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%; T_A = Industrial or Military

2

D.C.

SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}			V	
V_{IL}	Logical "0" Input Voltage			20% V_{CC}	V	
I_{IL}	Input Leakage	-1.0		+1.0	μA	$0V \leqslant V_{IN} \leqslant V_{CC}$
V_{OH}	Logical "1" Output Voltage(1)	2.4			V	I_{OH} = -0.2mA
V_{OL}	Logical "0" Output Voltage			0.45	V	I_{OL} = 2.0mA
I_O	Output Leakage	-1.0		+1.0	μA	$0V \leqslant V_O \leqslant V_{CC}$
I_{CC}	Supply Current (Static)		1.0	100	μA	$V_{IN} = V_{CC}$, Freq. = 0
C_I	Input Capacitance(2)		5	7	pF	
C_O	Output Capacitance(2)		8	10	pF	
C_{IO}	Input/Output Capacitance(2)		8	10	pF	

NOTE: (1) Except pins 33, 34, 39
(2) Guaranteed and sampled, but not 100% tested.

A.C.

		T_A = 25°C V_{CC} = 5.0V(1)		T_A = INDUSTRIAL V_{CC} = 5V ±10%		T_A = MILITARY V_{CC} = 5V ±10%			
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	TEST CONDITIONS
tDR	Delay: $\overline{DEVSEL}$ to $\overline{READ}$		200		300	330		ns	C_L = 50pF
tDW	Delay: $\overline{DEVSEL}$ to WRITE	100	220	140	300	150	330	ns	See Timing
tDF	Delay: $\overline{DEVSEL}$ to FLAG		200		375		415	ns	Diagram
tDC	Delay: $\overline{DEVSEL}$ to $\overline{C1}$, $\overline{C2}$		160		460		510	ns	
tDI	Delay: $\overline{DEVSEL}$ to $\overline{SKP}/\overline{INT}$		210		460		510	ns	
tDA	Delay: $\overline{DEVSEL}$ to DX		350		460		510	ns	
tLX	LXMAR Pulse Width	200		240		265		ns	
tAS	Address Set-Up Time	60		80		90		ns	
tAH	Address Hold Time	100		125		140		ns	
tDS	Data Set-Up Time	50		80		80		ns	
tDH	Data Hold Time	100		100		110		ns	

NOTE (1): All devices guaranteed at worst case limits. Room temperature, 5V data provided for information – not guaranteed.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6101C-9	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±5%; T_A = Industrial

D.C.

SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}			V	
V_{IL}	Logical "0" Input Voltage			.8	V	
I_{IL}	Input Leakage	-10		+10	µA	$0V \leqslant V_{IN} \leqslant V_{CC}$
V_{OH}	Logical "1" Output Voltage(1)	2.4			V	I_{OH} = -0.2mA
V_{OL}	Logical "0" Output Voltage			0.45	V	I_{OL} = 1.6mA
I_O	Output Leakage	-10		+10	µA	$0V \leqslant V_O \leqslant V_{CC}$
I_{CC}	Supply Current (Static)		1.0	800	µA	$V_{IN} = V_{CC}$, Freq. = 0
C_I	Input Capacitance(2)		5	7	pF	
C_O	Output Capacitance(2)		8	10	pF	
C_{IO}	Input/Output Capacitance(2)		8	10	pF	

NOTES: (1) Except pins 33, 34, 39
(2) Guaranteed and sampled, but not 100% tested.

A.C.

		T_A = 25°C V_{CC} = 5.0V(1)		T_A = INDUSTRIAL V_{CC} = 5V ±5%			
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS	TEST CONDITIONS
tDR	Delay: $\overline{DEVSEL}$ to $\overline{READ}$		230		375	ns	C_L = 50pF
tDW	Delay: $\overline{DEVSEL}$ to WRITE	100	240	125	375	ns	See Timing
tDF	Delay: $\overline{DEVSEL}$ to FLAG		230		475	ns	Diagram
tDC	Delay: $\overline{DEVSEL}$ to $\overline{C1}$, $\overline{C2}$		190		560	ns	
tDI	Delay: $\overline{DEVSEL}$ to $\overline{SKP}/\overline{INT}$		250		560	ns	
tDA	Delay: $\overline{DEVSEL}$ to DX		400		560	ns	
tLX	LXMAR Pulse Width	230		300		ns	
tAS	Address Set-Up Time	80		100		ns	
tAH	Address Hold Time	120		150		ns	
tDS	Data Set-Up Time	60		90		ns	
tDH	Data Hold Time	120		150		ns	

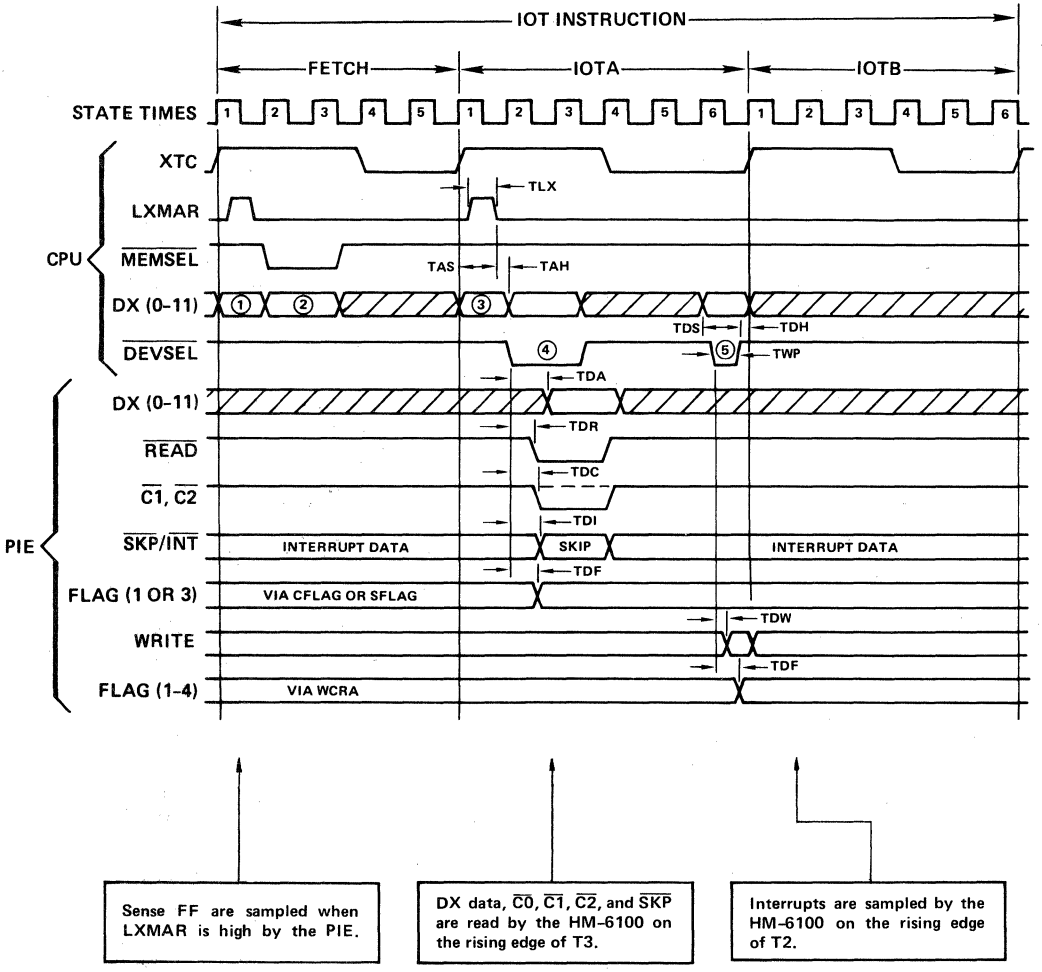
NOTE (1): All devices guaranteed at worst case limits. Room temperature, 5V data provided for information — not guaranteed.

Timing Diagram

Timing for a typical transfer is shown below. During an instruction fetch the processor places the contents of the PC on the bus (1) and obtains from memory an IOT instruction of the form 6XXX (2). During IOTA of the execute phase the processor places that instruction back on the DX lines (3) and pulses LXMAR transferring address and control information for the IOT transfer to all peripheral devices. A low going pulse on $\overline{\text{DEVSEL}}$ while XTC is high (4) is used by the addressed PIE along with the decoded control information to generate CPU control signals $\overline{\text{C1}}$, $\overline{\text{C2}}$, and $\overline{\text{SKP}}$. Also at this time either the Control Register A or the Interrupt Vector Register are outputed on the DX lines, or control outputs $\overline{\text{READ1}}$ and $\overline{\text{READ2}}$ are generated to gate peripheral data to the DX lines. A low going pulse on $\overline{\text{DEVSEL}}$ while XTC is low (5) is used to generate WRITE 1 and WRITE 2 controls. These signals are used to latch accumulator data into peripheral devices.

All PIE timing is generated from HM-6100 signals LXMAR, $\overline{\text{DEVSEL}}$, and XTC. No additional timing signals, clocks, or one shots are required.

Propagation delays, pulse width, data setup and hold times are specified for direct interfacing with the HM-6100.

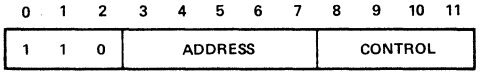


Pie Address and Instructions

The HM-6100 communicates with the PIE and with peripherals through the PIE via IOT commands. During the IOTA cycle an instruction of the form 6XXX is loaded into all PIE instruction registers. The bits are interpreted as shown below.

The 5 address bits (3-7) are compared with the pin programmable select inputs SEL3, SEL4, SEL5, SEL6, SEL7 to address 1 of 31 possible PIEs. Address zero is reserved for IOT's internal to the HM-6100. The four control bits are decoded by the PIE to select one of 16 instructions which are described below.

PIE INSTRUCTION FORMAT



CONTROL	MNEMONICS	ACTION
0000 1000	READ1 READ2	The READ instructions generate a pulse on the appropriate read outputs. This signal is used by the peripheral device to gate onto the DX bus to be "OR'ed" with the HM-6100 accumulator data. The HM-6100 accumulator is cleared prior to reading peripheral data when $\overline{CO}$ is asserted low.
0001 1001	WRITE1 WRITE2	The WRITE instructions generate a pulse on the appropriate write output. This signal is used by peripherals to load the HM-6100 accumulator data on the DX lines into peripheral data registers. The HM-6100 AC is cleared after the write operation when the $\overline{CO}$ input is asserted low.
0010 0011 1010 1011	SKIP1 SKIP2 SKIP3 SKIP4	The SKIP instructions test the state of the sense flip flops. If the input conditions have set the sense flip flop, the PIE will assert the $\overline{SKP}/\overline{INT}$ output causing the HM-6100 to skip the next program instruction. The sense flip flop is then cleared. If the sense flip flop is not set, the PIE does not assert the $\overline{SKP}/\overline{INT}$ output and the HM-6100 will execute the next instruction.
0110	RCRA	The Read Control Register A instruction gates the contents of CRA onto the DX lines during time ④ to be "OR" transferred to the HM-6100 AC.
0101 1101 1100	WCRA WCRB WVR	The Write Control Register A, Write Control Register B and Write Vector Register instructions transfer HM-6100 AC data on the DX lines during time ⑤ of IOTA into the appropriate register.
0100 1110	SFLAG1 SFLAG3	The SET FLAG instructions set the bits FL1 and FL3 in control register A to a high level. PIE outputs FLAG1 and FLAG3 follow the data stored in bits FL1 and FL3 of CRA.
0111 1111	CFLAG1 CFLAG3	The CLEAR FLAG instructions clear the bits FL1 and FL3 in control register A to a low level.
$(6007)_8$	CAF	HM-6100 internal IOT instruction CLEAR ALL FLAGS clears the interrupt requests by clearing the sense flip flops.

Programmable Outputs

FLAGs (1-4) – The FLAGs are general purpose outputs that can be set and cleared under program control. FLAG1 follows bit FL1 in Control Register A and etc. FLAGs can be changed by loading new data into CRA via the WCRA commands. In addition, FLAG1 and FLAG3 can be set and cleared directly by the commands SFLAG1, CFLAG1, SFLAG3 and CFLAG3.

Programmable Sense Inputs

The sense inputs are used to set sense flip flops (SENSE FF) inside the PIE. For each sense input there are two FF's, one for skip and one for interrupt. Conditions for setting each SENSE FF, levels or edges and positive or negative polarities, are set by control bits SL and SP in CRB.

The SENSE FF's are sampled when LXMAR is high. Interrupt requests are generated only when the sense flip flops are set by an edge and interrupts are enabled by writing to control reg A. Sense flip flops are reset on the following conditions.

CONDITION	SENSE FLIP FLOPS	
	SKIP FF	INTERRUPT FF
CAF Instruction (6007₈)	Clears All	Clears All
SKIP Instruction	Clears Corresponding FF	Clears Corresponding FF
Vectored Interrupt	Not Cleared	Clears Highest Priority FF on Selected PIE After Vectoring
Interrupt Disabled (IE = "0")	Not Cleared	Disables Interrupt by Holding Corresponding FF in Reset State

2

Controls for Input and Output Ports

READ (1-2) – The $\overline{\text{READ}}$ outputs are activated by the read instructions and are used by peripheral devices to get data onto the DX lines for transfer to the HM-6100. Read lines are active low.

WRITE (1-2) – The WRITE outputs are activated by the write instructions and are used by peripheral devices to load HM-6100 AC data from the DX lines into peripheral data registers. Output polarity is controlled by the WRITE POLARITY bits of CRA. A logic one causes pulses to be positive while a logic zero causes pulses to be negative.

I/O CONTROL LINES – There are three I/O control lines from the PIE to the microprocessor – $\overline{C1}$, $\overline{C2}$, and $\overline{INT}/\overline{SKP}$. The type of data transfer, during an IOT instruction, is specified by the PIE's assertion of the $\overline{C1}$ and $\overline{C2}$ control lines as shown below.

Interrupt and skip information are time multiplexed on the same line ($\overline{SKP}/\overline{INT}$). Since the HM-6100 samples skip and interrupt data at separate times there is no degradation in system performance. The PIE samples the sense flip flops and generates an interrupt request for enabled bits (IE1-4) when LXMAR is high. Interrupt requests are asserted by the PIE driving the $\overline{INT}/\overline{SKP}$ line low. During IOTA of SKIP instructions the $\overline{INT}/\overline{SKP}$ reflects the SENSE FF data when $\overline{DEVSEL}$ is low and XTC is high. If the SENSE flip flop is set, the $\overline{INT}/\overline{SKP}$ line is driven low to cause the HM-6100 to skip the next instruction. All these outputs are open drain.

CONTROL LINES				OPERATION	DESCRIPTION
$\overline{SKP}$	$\overline{C0}$*	$\overline{C1}$	$\overline{C2}$		
H	H	H	H	PIE ← AC	The contents of the AC is sent to the PIE.
H	H	L	H	AC ← AC V PIE	Data is received from the PIE, OR'ed with the data in the AC and the result stored in the AC.
H	H	L	L	PC ← Vector Address	Vector address received from PIE and loaded into PC. This is referred to as an absolute jump.
L	H	H	H	PC ← PC + 1	Forces Microprocessor to skip next sequential instruction.

NOTE: *The $\overline{C0}$ line must be connected to V_{CC} using a pull-up resistor.

CONTROL REGISTER A (CRA)

The CRA can be read and written by the HM-6100 via the RCRA and WCRA commands.

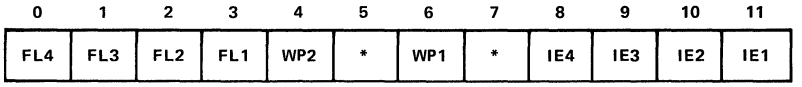
The format and meaning of control bits are shown below.

FL (1-4) – Data on FLAG outputs corresponds to data in FL (1-4). Changing the FL bits under software control changes the corresponding FLAG outputs.

IE (1-4) – A high level on INTERRUPT ENABLE enables interrupts for the SENSE inputs.

Otherwise these inputs provide conditional skip testing as defined by the SKIP1-4 instructions.

WP (1-2) – A high level on WRITE POLARITY bits causes positive pulses at the WRITE outputs.



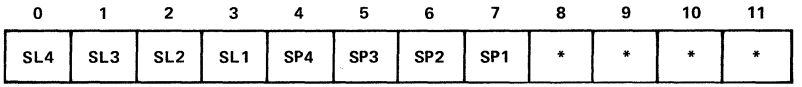
* = Don't Care

CONTROL REGISTER B (CRB)

The CRB can be written by the HM-6100 via the WCRB instruction. It has no read back capability. The format and meaning of control bits are shown.

SL (1-4) – A high level on the SENSE LEVEL bits causes the SENSE inputs to be level sensitive. A low level in the SL bits causes the SENSE inputs to be edge sensitive. An interrupt request is generated only if a sense line is set up to be edge sensitive and interrupts are enabled via the IE bits of CRA.

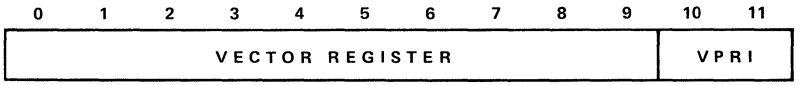
SP (1-4) – A high level on the SENSE POLARITY bits causes the flip flop to be set by high level or positive going edge. A low level causes the flip flop to be set by a low level or negative going edge.



* = Don't Care

VECTOR REGISTER

A hardware priority network uniquely selects a PIE to provide a vectored address. The first IOT command of any type, after the HM-6100 signal INTERRUPT GRANT goes high, resets the INTGNT line to a low level. The INTGNT signal is used to freeze the priority network and enable vector generation. The highest priority PIE has PIN tied to V_{CC}. The lowest priority PIE is the last one on the chain. Within the PIE, SENSE1 has the highest priority and SENSE 4 has the lowest. The vector address generated by the PIE consists of 10 bits from the vector register and two bits that indicate the sense input within the highest priority PIE that generated the interrupt. If PIN is tied to GND, then the PIE will respond as a non-vectored interrupt device.

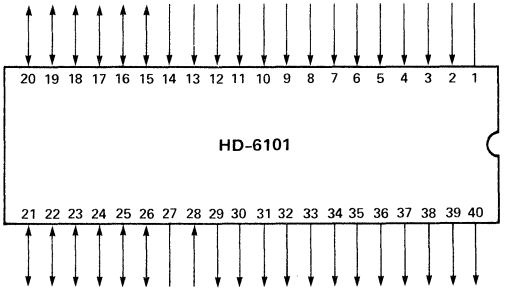


VPRI	CONDITIONS
00	SENSE 1
01	SENSE 2
10	SENSE 3
11	SENSE 4

Pin Definitions

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
1	V_{CC}		Positive voltage
2	INTGNT	H	A high level on INTERRUPT GRANT inhibits recognition of new interrupt requests and allows the priority chain time to uniquely specify a PIE.
3	PRIN	H	A high level ON PRIORITY IN and an interrupt request will select a PIE for vectored interrupt.
4	SENSE 4	PROG	The SENSE input is controlled by the SL (sense level) and SP (sense polarity) bits of control register B. A high SL level will cause the sense flip flop to be set by a level while a low SL level causes then sense flip flop to be set by an edge. A high SP level will cause the sense flip flop to be set by a positive going edge or high level. A high IE (interrupt enable) level generates an interrupt request whenever the sense flip flop is set by an edge.
5	SENSE 3	PROG	See pin 4 – SENSE 4
6	SENSE 2	PROG	See pin 4 – SENSE 4
7	SENSE 1	PROG	See pin 4 – SENSE 4

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
8	SEL 3	TRUE	Matching SELECT(3-7) inputs with PIE addressing on DX(3-7) during IOTA selects a PIE for programmed input output transfers.
9	SEL 4	TRUE	See Pin 8 – SEL 3
10	LXMAR	H	A positive pulse on LOAD EXTERNAL ADDRESS REGISTER loads address and control data from DX(3-11) into the address register.
11	SEL 5	TRUE	See Pin 8 – SEL 3
12	SEL 6	TRUE	See Pin 8 – SEL 3
13	XTC	H	The XTC input is a timing signal produced by the microprocessor. When XTC is high a low going pulse on $\overline{DEVSEL}$ initiates a "read" operation. When XTC is low, a low going pulse on $\overline{DEVSEL}$ initiates a write operation.
14	SEL 7	TRUE	See Pin 8 – SEL 3
15	DX 0	TRUE	Data transfers between the microprocessor and PIE take place via these input/output pins.
16	DX 1	TRUE	See Pin 15 – DX 0
17	DX 2	TRUE	See Pin 15 – DX 0
18	DX 3	TRUE	See Pin 15 – DX 0
19	DX 4	TRUE	See Pin 15 – DX 0
20	DX 5	TRUE	See Pin 15 – DX 0



PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
21	DX 6	TRUE	See Pin 15 – DX 0
22	DX 7	TRUE	See Pin 15 – DX 0
23	DX 8	TRUE	See Pin 15 – DX 0
24	DX 9	TRUE	See Pin 15 – DX 0
25	DX 10	TRUE	See Pin 15 – DX 0
26	DX 11	TRUE	See Pin 15 – DX 0
27	GND		
28	$\overline{DEVSEL}$	L	The $\overline{DEVSEL}$ input is a timing signal produced by the microprocessor during IOT instructions. It is used by the PIE to generate timing for controlling PIE registers and "read" and "write" operations.
29	FLAG 4	PROG	The FLAG outputs reflect the data stored in control register A. Flags (1-4) can be set or reset by changing data in CRA via a WRA (write control register A) command. FLAG1 and FLAG3 can be controlled directly by PIE commands SFLAG1, CFLAG1, SFLAG3 and CFLAG3.
30	FLAG 3	PROG	See Pin 29 – FLAG 4
31	FLAG 2	PROG	See Pin 29 – FLAG 4
32	FLAG 1	PROG	See Pin 29 – FLAG 4
33	$\overline{C1}$	L	The PIE decodes address, control and priority information and asserts outputs $\overline{C1}$ and $\overline{C2}$ during the IOTA cycle to control the type of data transfer. These outputs are open drain for bussing and require a pullup register to V_{CC}. $\overline{C1}$(L), $\overline{C2}$(L) - vectored interrupt $\overline{C1}$(L), $\overline{C2}$(H) - $\overline{READ1}$, $\overline{READ2}$ or RRA commands $\overline{C1}$(H), $\overline{C2}$(H) - all other instructions

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
34	$\overline{C2}$	L	See Pin 33 – $\overline{C1}$
35	$\overline{READ1}$	PROG	Outputs $\overline{READ1}$ and $\overline{READ2}$ are used to gate data from peripheral devices onto the DX bus for input to the **HM-6100** Note the data does not pass through the PIE.
36	WRITE1	PROG	Outputs WRITE1 and WRITE2 are used to gate data from the **HM-6100** DX bus into peripheral devices. Data does not pass through the PIE.
37	$\overline{READ2}$	PROG	See Pin 35 – $\overline{READ1}$
38	WRITE2	PROG	See Pin 36 – WRITE1
39	$\overline{SKP/INT}$	L	The PIE asserts this line low to generate interrupt requests and to signal the **HM-6100** when sense flip flops are set during SKIP instructions. This output is open drain.
40	POUT	H	A high level on priority out indicates no higher priority PIE interrupt requests are outstanding. This output is tied to the PIN input of the next lower priority PIE in the chain.

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HD-6102

MEMORY EXTENSION/DMA/ INTERVAL TIMER/CONTROLLER (MEDIC)

Advance Information

Features

- HM-6100 COMPATIBLE
- LOW POWER – TYP. < 5.0μW STANDBY
- SINGLE SUPPLY 4 – 11 VOLTS
- FULL TEMPERATURE RANGE -55°C TO +125°C
- STATIC OPERATION
- SINGLE PHASE CLOCK, ON CHIP CRYSTAL OSC.
- SOFTWARE COMPATIBLE WITH PDP-8/E
- PROVIDES ADDRESSING UP TO 32 WORDS
- PROVIDES SIMULTANEOUS DMA
- DMA CHANNEL CAN BE USED FOR DYNAMIC RAM
- 12-BIT PROGRAMMABLE INTERVAL TIMER
- HARDWARE RESET
- PRIORITY VECTORED INTERRUPTS
- 28 DIFFERENT I/O INSTRUCTIONS

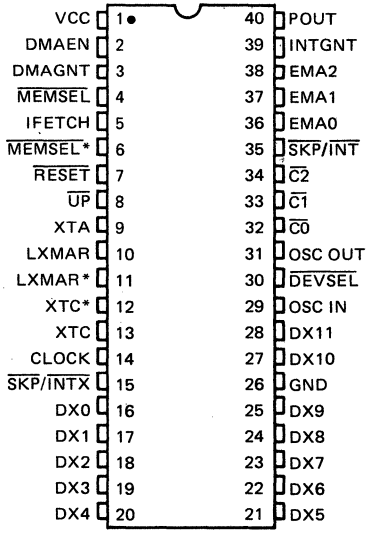
Description

The HD-6102 is a multi-function peripheral controller circuit incorporating such functions as memory extension, direct memory access control, and a programmable real time clock.

The HD-6102 provides the necessary control to address up to 32K words of memory, and its DMA channel can be used with Dynamic RAM Components for "transparent refresh". The programmable real time clock is 12-bits long, and its output frequency can be programmed for 5 decades.

It features a high degree of system integration, putting into one chip all the functions which are normally available in three or more LSI circuits. As a result of this large integration, the user can design and produce a compact microcomputer with minicomputer performance.

Pinout



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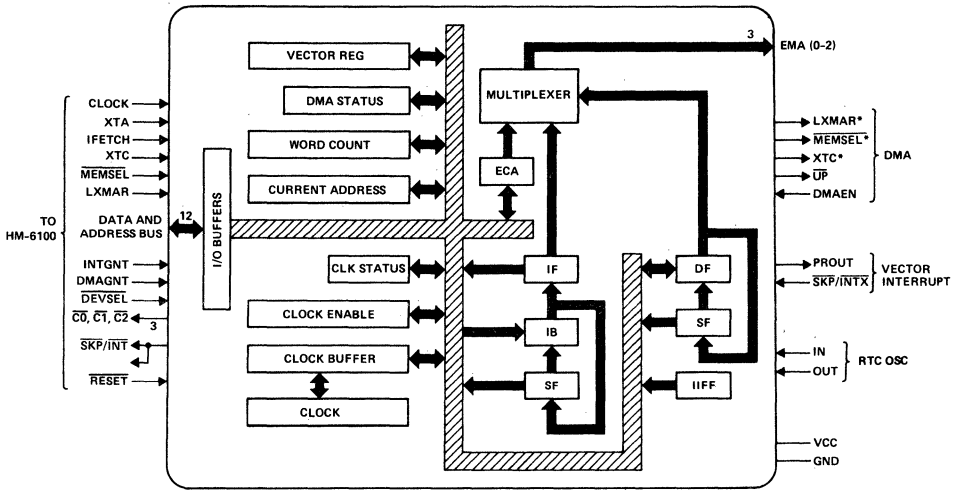
Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+12.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6102A-9	-40°C to +85°C
Military HD-6102A-2	-55°C to +125°C

ELECTRICAL CHARACTERISTICS VCC = 10.0 ±0.5 Volts TA = Industrial or Military

D.C.

SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	TEST CONDITIONS
VIH	Logical "1" Input Voltage	70% VCC			V	
VIHC	Logical "1" Osc. Input Voltage	VCC -.5			V	
VIL	Logical "0" Input Voltage			20% VCC	V	
VILC	Logical "0" Osc. Input Voltage			GND +.5	V	
IIL	Input Leakage(1)	1.0		1.0	μA	0V ≤ VIN ≤ VCC
VOH	Logical "1" Output Voltage(2)	VCC -2.0			V	IOH = -0.2mA
VOL	Logical "0" Output Voltage(3)			0.45	V	IOL = 2.0mA
IO	Output Leakage	-1.0		1.0	μA	0V ≤ VO ≤ VCC
ICC1	Supply Current (Static)			900	μA	VIN = VCC, Freq. = 0
ICC2	Supply Current (Operating) (HD-6102A-9)			4.0	mA	VCC = 10.0V Freq. = 5.7MHz
ICC2	Supply Current (Operating) (HD-6102A-2)			4.0	mA	VCC = 10.0V Freq. = 5.0MHz
CI	Input Capacitance(4)		7	8	pF	
CO	Output Capacitance(4)		8	10	pF	
CIO	Input/Output Capacitance(4)		8	10	pF	
COSC	Oscillator IN/OUT Capacitance(4)		30		pF	

NOTES: (1) Except pins 15, 29, 31. (2) Except pins 31, 32, 33, 34. (3) Except pin 31.
(4) Guaranteed and sampled, but not 100% tested.

A.C.

		TA = 25°C VCC = 10V (1)		TA = INDUSTRIAL VCC = 10 ±0.5V Fc = 5.7MHz		TA = MILITARY VCC = 10 ±0.5V Fc = 5.0MHz			
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	TEST CONDITIONS
tLXIN	LXMAR Pulse Width IN			125		135		ns	CL = 50pF
tAIS	Address Set-Up Time IN			50		60		ns	See Timing
tAIH	Address Hold Time IN			50		60		ns	Diagram
tDA	Delay: $\overline{DEVSEL}$ to DX				240		260	ns	
tDC	Delay: $\overline{DEVSEL}$ to $\overline{C1}$, $\overline{C2}$				240		260	ns	
tDI	Delay: $\overline{DEVSEL}$ to $\overline{SKP/INT}$				240		260	ns	
tDIS	Data Input Set-Up Time			50		60		ns	
tDIH	Data Input Hold Time			50		60		ns	
tRST	$\overline{RESET}$ Input Pulse Width			250		250		ns	
tSID	Delay: $\overline{SKP/INTX}$ to $\overline{SKP/INT}$				100		120	ns	
tDMLX	Delay: XTC to XTC*, $\overline{MEMSEL}$ to $\overline{MEMSEL}$*, LXMAR to LXMAR*				100		120	ns	
tDEM	Enable/Disable Time: DMAGNT to EMA Lines				50		60	ns	
tMDR	$\overline{MEMSEL}$* Pulse Width READ			300		375		ns	
tMDW	$\overline{MEMSEL}$* Pulse Width WRITE			380		475		ns	
tMDWR	$\overline{MEMSEL}$* Pulse Width WRITE/REFRESH			240		275		ns	
tLD	LXMAR* Pulse Width			150		175		ns	
tDRAT	DMA READ Access Time: LXMAR to $\overline{UP}$			300		375		ns	
tDXAS	DX & EMA Address Setup Time Wrt LXMAR*			150		70		ns	
tDXAH	DX & EMA Address Hold Time Wrt LXMAR*			55		70		ns	
tDREN	DMA READ Enable Time: $\overline{MEMSEL}$* to $\overline{UP}$			210		275		ns	
tRUP	$\overline{UP}$ Pulse Width DMA READ			150		175		ns	
tDWAT	DMA WRITE Access Time: LXMAR* to $\overline{MEMSEL}$*			300		375		ns	
tDWEN	DMA WRITE Enable Time: $\overline{UP}$ to $\overline{MEMSEL}$*			210		275		ns	
tMWS	$\overline{MEMSEL}$* Setup Time DMA Write: $\overline{MEMSEL}$* to LXMAR*			50		50		ns	
tDMS	DMAEN Setup Time Write			50		50		ns	
tDMH	DMAEN Hold Time Write			50		50		ns	
tWUP	$\overline{UP}$ Pulse Width DMA WRITE			300		375		ns	

NOTE 1: All devices guaranteed at worst case limits. Room temperature, 10V data provided for information — not guaranteed.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6102-9	-40°C to +85°C
Military HD-6102-2	-55°C to +125°C

ELECTRICAL CHARACTERISTICS VCC = 5.0 ±10% Volts TA = Industrial or Military

D.C.

SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	TEST CONDITIONS
VIH	Logical "1" Input Voltage	70% VCC			V	
VIHC	Logical "1" Osc. Input Voltage	VCC -.5			V	
VIL	Logical "0" Input Voltage			20% VCC	V	
VILC	Logical "0" Osc. Input Voltage			GND +.5	V	
IIL	Input Leakage(1)	-1.0		1.0	µA	0V ≤ VIN ≤ VCC
VOH	Logical "1" Output Voltage(2)	2.4			V	IOH = -0.2mA
VOL	Logical "0" Output Voltage(3)			0.45	V	IOL = 2.0mA
IO	Output Leakage	-1.0		1.0	µA	0V ≤ VO ≤ VCC
ICC1	Supply Current (Static)			800	µA	VIN = VCC, Freq. = 0
ICC2	Supply Current (Operating) (HD-6102-9)			2.0	mA	VCC = 5.0V Freq. = 3.33MHz
ICC2	Supply Current (Operating) (HD-6102-2)			2.0	mA	VCC = 5.0V Freq. = 2.5MHz
CI	Input Capacitance(4)		7	8	pF	
CO	Output Capacitance(4)		8	10	pF	
CIO	Input/Output Capacitance(4)		8	10	pF	
COSC	Oscillator IN/OUT Capacitance(4)		30		pF	

NOTES: (1) Except pins 15, 29, 31. (2) Except pins 31, 32, 33, 34. (3) Except pin 31.
(4) Guaranteed and sampled, but not 100% tested.

A.C.

		TA = 25°C VCC=5.0V (1)		TA = INDUSTRIAL VCC=5V ±10% Fc = 3.33MHz		TA = MILITARY VCC=5V ±10% Fc = 2.5MHz			
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	TEST CONDITIONS
tLXIN	LXMAR Pulse Width IN			250		300		ns	CL = 50pF
tAIS	Address Set-Up Time IN			70		80		ns	See Timing
tAIH	Address Hold Time IN			100		120		ns	Diagram
tDA	Delay: $\overline{DEVSEL}$ to DX				350		400	ns	
tDC	Delay: $\overline{DEVSEL}$ to $\overline{C1}$, $\overline{C2}$				350		400	ns	
tDI	Delay: $\overline{DEVSEL}$ to $\overline{SKP}/\overline{INT}$				350		400	ns	
tDIS	Data Input Set-Up Time			100		100		ns	
tDIH	Data Input Hold Time			100		100		ns	
tRST	$\overline{RESET}$ Input Pulse Width			500		500		ns	
tSID	Delay: $\overline{SKP}/\overline{INTX}$ to $\overline{SKP}/\overline{INT}$				120		130	ns	
tDMLX	Delay: XTC to XTC*, $\overline{MEMSEL}$ to $\overline{MEMSEL}$*, LXMAR to LXMAR*				120		130	ns	
tDEM	Enable/Disable Time: DMAGNT to EMA Lines				80		100	ns	
tMDR	$\overline{MEMSEL}$* Pulse Width READ			550		750		ns	
tMDW	$\overline{MEMSEL}$* Pulse Width WRITE			700		950		ns	
tMDWR	$\overline{MEMSEL}$* Pulse Width WRITE/REFRESH			400		550		ns	
tLD	LXMAR* Pulse Width			260		350		ns	
tDRAT	DMA READ Access Time: LXMAR to $\overline{UP}$			85		750		ns	
tDXAS	DX & EMA Address Setup Time Wrt LXMAR*			125		120		ns	
tDXAH	DX & EMA Address Hold Time Wrt LXMAR*			125		175		ns	
tDREN	DMA READ Enable Time: $\overline{MEMSEL}$* to $\overline{UP}$			400		550		ns	
tRUP	$\overline{UP}$ Pulse Width DMA READ			260		350		ns	
tDWAT	DMA WRITE Access Time: LXMAR* to $\overline{MEMSEL}$*			550		750		ns	
tDWEN	DMA WRITE Enable Time: $\overline{UP}$ to $\overline{MEMSEL}$*			400		550		ns	
tMWS	$\overline{MEMSEL}$* Setup Time DMA Write: $\overline{MEMSEL}$* to LXMAR*			100		100		ns	
tDMS	DMAEN Setup Time Write			100		100		ns	
tDMH	DMAEN Hold Time Write			100		100		ns	
tWUP	$\overline{UP}$ Pulse Width DMA WRITE			550		750		ns	

NOTE 1: All devices guaranteed at worst case limits. Room temperature, 5V data provided for information — not guaranteed.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6102C-9	-40°C to +85°C

ELECTRICAL CHARACTERISTICS VCC = 5.0 ±5% Volts TA = Industrial

D.C.

SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	TEST CONDITIONS
VIH	Logical "1" Input Voltage	70% VCC			V	
VIHC	Logical "1" Osc. Input Voltage	VCC -.5			V	
VIL	Logical "0" Input Voltage			.8	V	
VILC	Logical "0" Osc. Input Voltage			GND +.5	V	
IIL	Input Leakage(1)	-10		+10	μA	0V ≤ VIN ≤ VCC
VOH	Logical "1" Output Voltage(2)	2.4			V	IOH = -0.2mA
VOL	Logical "0" Output Voltage(3)			0.45	V	IOL = 1.6mA
IO	Output Leakage	-10		+10	μA	0V ≤ VO ≤ VCC
ICC1	Supply Current (Static)			900	μA	VIN = VCC, Freq. = 0
ICC2	Supply Current (Operating)			1.8	mA	VCC = 5.0V Freq. = 2.5MHz
CI	Input Capacitance(4)		7	8	pF	
CO	Output Capacitance(4)		8	10	pF	
CIO	Input/Output Capacitance(4)		8	10	pF	
COSC	Oscillator IN/OUT Capacitance(4)		30		pF	

NOTES: (1) Except pins 15, 29, 31. (2) Except pins 31, 32, 33, 34. (3) Except pin 31.
(4) Guaranteed and sampled, but not 100% tested.

A.C.

		TA = 25°C VCC=5.0V (1)		TA = INDUSTRIAL VCC=5V ±5% Fc = 2.5MHz			
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS	TEST CONDITIONS
tLXIN	LXMAR Pulse Width IN			300		ns	CL = 50pF
tAIS	Address Set-Up Time IN			80		ns	See Timing
tAIH	Address Hold Time IN			120		ns	Diagram
tDA	Delay: $\overline{DEVSEL}$ to DX				400	ns	
tDC	Delay: $\overline{DEVSEL}$ to $\overline{C1}$, $\overline{C2}$				400	ns	
tDI	Delay: $\overline{DEVSEL}$ to $\overline{SKP/INT}$				400	ns	
tDIS	Data Input Set-Up Time			100		ns	
tDIH	Data Input Hold Time			100		ns	
tRST	$\overline{RESET}$ Input Pulse Width			500		ns	
tSID	Delay: $\overline{SKP/INTX}$ to $\overline{SKP/INT}$				150	ns	
tDMLX	Delay: XTC to XTC*, $\overline{MEMSEL}$ to $\overline{MEMSEL}$*, LXMAR to LXMAR*				150	ns	
tDEM	Enable/Disable Time: $\overline{DMAGNT}$ to EMA Lines				100	ns	
tMDR	$\overline{MEMSEL}$* Pulse Width READ			750		ns	
tMDW	$\overline{MEMSEL}$* Pulse Width WRITE			950		ns	
tMDWR	$\overline{MEMSEL}$* Pulse Width WRITE/REFRESH			550		ns	
tLD	LXMAR* Pulse Width			350		ns	
tDRAT	DMA READ Access Time: LXMAR to $\overline{UP}$			750		ns	
tDXAS	DX & EMA Address Setup Time Wrt LXMAR*			120		ns	
tDXAH	DX & EMA Address Hold Time Wrt LXMAR*			175		ns	
tDREN	DMA READ Enable Time: $\overline{MEMSEL}$* to $\overline{UP}$			550		ns	
tRUP	$\overline{UP}$ Pulse Width DMA READ			350		ns	
tDWAT	DMA WRITE Access Time: LXMAR* to $\overline{MEMSEL}$*			750		ns	
tDWEN	DMA WRITE Enable Time: $\overline{UP}$ to $\overline{MEMSEL}$*			550		ns	
tMWS	$\overline{MEMSEL}$* Setup Time DMA Write: $\overline{MEMSEL}$* to LXMAR*			100		ns	
tDMS	DMAEN Setup Time Write			100		ns	
tDMH	DMAEN Hold Time Write			100		ns	
tWUP	$\overline{UP}$ Pulse Width DMA WRITE			750		ns	

NOTE 1: All devices guaranteed at worst case limits. Room temperature, 5V data provided for information — not guaranteed.

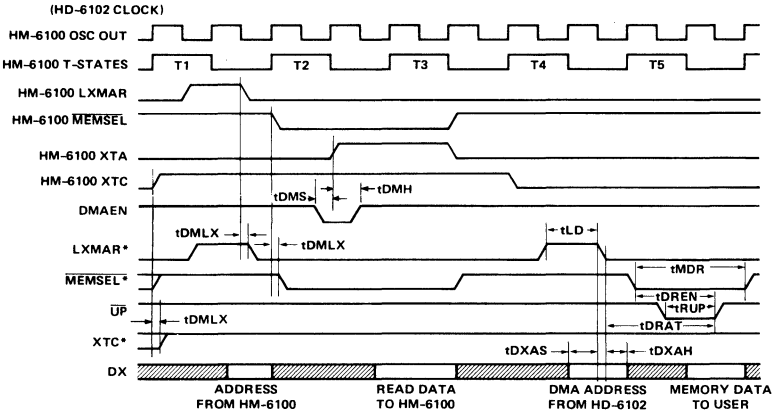


FIGURE 1-1 – DMA Read

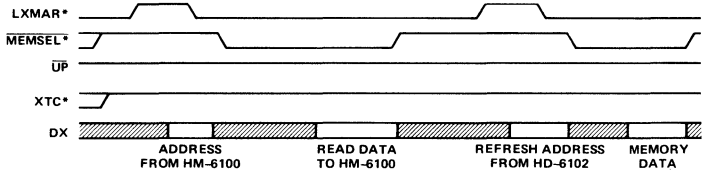


FIGURE 1-2 – DMA Read/Refresh

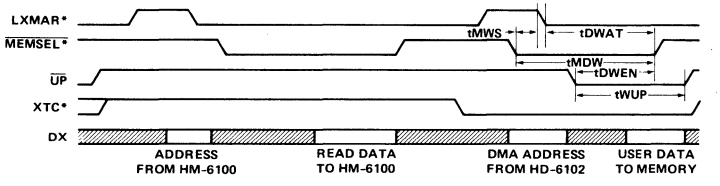


FIGURE 1-3 – DMA Write

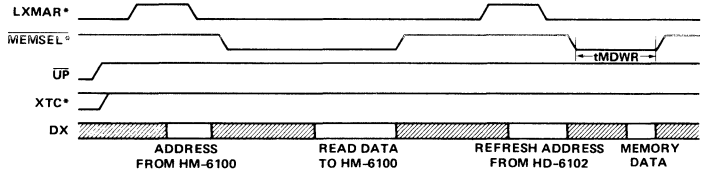


FIGURE 1-4 – DMA Write/Refresh

HD-6102 System Timing

The three-state bi-directional 12-bit DX bus is used to transfer data and control information between the HD-6102 and the HM-6100 microprocessor. The HM-6100 transmits the device address and control information on the DX bus during the 'execute' phase of an Input-Output Transfer (IOT) instruction. The HD-6102 accepts this information on the falling edge of the LXMAR (Address Latch Enable) Signal.

The device selection bits (3-8) are compared within the HD-6102 and if these are 00, 13, or 2X, the MEDIC decodes the control bits (9-11) for execution. $\overline{\text{DEVSEL}}$ goes low, during the first half of an IOT execute machine cycle for a read operation and it goes low again in the second half for a write operation.

The HD-6102 responds to a 'read' instruction by putting data on the DX bus when $\overline{\text{DEVSEL}}$ is low. During the write operation, the MEDIC accepts data from the HM-6100 Accumulator on the rising edge of the $\overline{\text{DEVSEL}}$.

$\overline{\text{SKP/INT}}$ line goes low during the 'read' $\overline{\text{DEVSEL}}$ if the HD-6102 is responding to a 'skip' instruction, and the 'skip' condition is met, therefore causing the HM-6100 to skip the next sequential instruction. $\overline{\text{SKP/INT}}$ line reflects the interrupt request status of the HM-6100 at all times except during the 'read' $\overline{\text{DEVSEL}}$. The $\overline{\text{SKP/INT}}$ line goes low if an active interrupt request is pending. During read $\overline{\text{DEVSEL}}$ mode, the $\overline{\text{SKP/INT}}$ indicates the current skip condition.

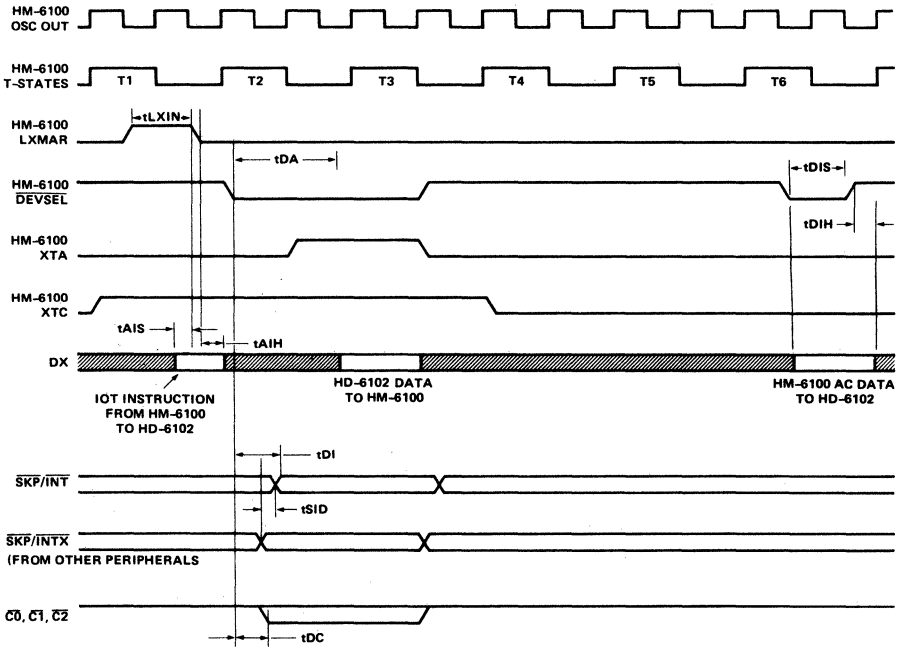


FIGURE 2 – HD-6102 System Timing Diagram

Architecture

The HD-6102 is composed of three distinct functions:

(A) A DMA port that uses the bus during the second half of a cycle to read, write, or refresh memory. The DMA port logic includes a word count register WC, a current address register CA, an extended current address register ECA, and a DMA status register.

(B) An extended memory address controller that augments the 12-bit addresses generated by the HM-6100 microprocessor by supplying a 3-bit address field that may be decoded to select one of eight 4096 word memory fields. The memory extension controller logic consists of an instruction field register IF, a data field register DF, an instruction buffer register IB, and a save field register SF.

(C) A realtime clock whose mode and time base rate may be programmed by the user. The clock logic includes a clock enable register CE, a clock buffer register CB, a clock counter register CC, and a time base multiplexer.

The SDMA registers are summarized as follows:

CURRENT ADDRESS (CA) REGISTER

This register is a 12-bit presettable binary counter. At the beginning of a SDMA transfer, the current address must be set to the first location to be accessed. The content of the CA register is incremented by 1 after a SDMA transfer, and the incremented value is used as the address of the memory location with which the next transfer will be performed.

EXTENDED CURRENT ADDRESS (ECA) REGISTER

This is a 3-bit presettable binary counter and if the carry enable bit of the DMA status register is set, the 12-bit CA register and the 3 ECA bits are treated as one 15-bit register with the ECA bits most significant. If memory field 7 (all 3 bits at logic one) is selected, the ECA cannot increment, but will wrap around infield 7 and an F7 error (F7E) will occur. The Interrupt Enable bit IE in SR11 must be set to enable F7E interrupts. If enabled, the F7E will request an interrupt. If the carry enable bit CE in SR9 is not set, the ECA is not incremented when CA goes from 7777_8 to 0000_8.

WORD COUNT (WC) REGISTER

A 12-bit presettable binary counter is used as a word counter. At the beginning of a SDMA transfer, the two's complement of the number of 12-bit words to be transferred must be loaded into the WC. If enabled, this will initiate the SDMA operation. The WC register is incremented by 1 after a SDMA transfer. If this value becomes zero, word count overflow has occurred and if the IE bit in SR11 is set, interrupts are enabled and an interrupt is requested. Unless instructed to be in the continuous run mode, a WC overflow inhibits further transfers. The WOF is set when the MSB of the WC register makes a "1" to "0" transition.

DMA STATUS REGISTER

This register consists of 5 control bits and 2 flag bits for the SDMA feature. For a description, refer to the register bit assignments.

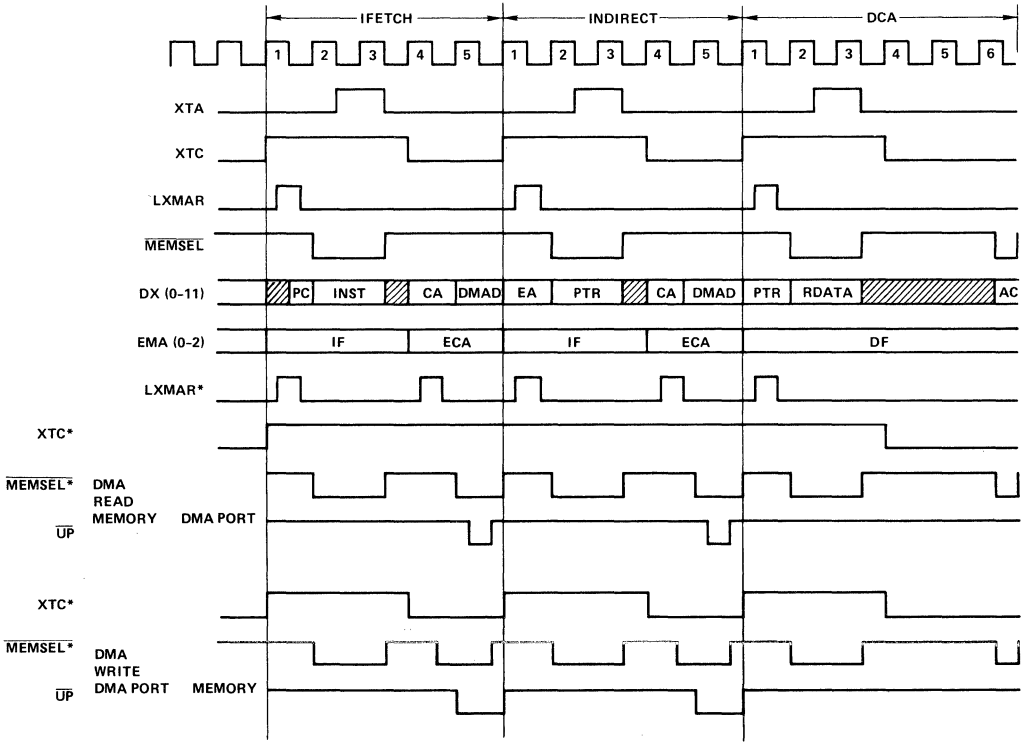


FIGURE 3 – MEDIC Timing for DCA I

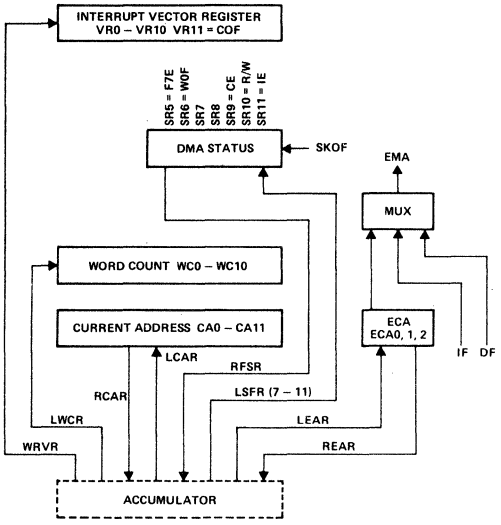


FIGURE 4 – SDMA Registers

TABLE 1 – SDMA Instructions

MNEMONIC	OCTAL CODE	OPERATION
LCAR	62058	LOAD CURRENT ADDRESS REGISTER (CA). Description: The contents of the AC replace the contents of the CA and the AC is cleared. DMA sequencing is stopped.
RCAR	62158	READ CURRENT ADDRESS REGISTER. Description: Contents of CA transferred to AC.
LWCR	62258	LOAD WORD COUNT REGISTER (WC). Description: Contents of AC is cleared WORD COUNT OVERFLOW (WOF) is cleared and DMA operation started.
LEAR	62N68	LOAD IMMEDIATE TO EXTENDED CURRENT ADDRESS REGISTER (ECA). Description: Field N of the IOT instruction is transferred to the Extended current address register.
REAR	62358	READ EXTENDED CA. Description: Extended Current Address register contents OR'd into bits 6, 7, 8, of AC.
LSFR	62458	LOAD DMA FLAGS and STATUS REGISTER. Description: AC bits 7-11 are transferred to the DMA STATUS REGISTER and the AC is cleared.
RFSR	62558	READ DMA FLAGS and STATUS REGISTER. Description: DMA Flags and Status Register bits are OR transferred into AC bits 5-11 and Field 7 wraparound error (F7E) is cleared.
SKOF	62658	SKIP ON OVERFLOW INTERRUPT. Description: The PC is incremented by 1 if a Word Count register overflow interrupt condition is present causing next instruction to be skipped.
WVWR	62758	WRITE VECTOR REGISTER. Description: AC bits 0-10 are transferred to the Vector Register and the AC is cleared.
CAF	60078	CLEAR ALL FLAGS. Description: Clears F7E and WOF (and also COF), clock enable and clock buffer. The DMA process is initiated if the Status Register is not set to the "stop" mode.

TABLE 2 – DMA Flags and Status Register Bit Assignments

0	1	2	3	4	5	6	7	8	9	10	11
*	*	*	*	*	F7E	WOF	SR7	SR8	CE	R/W	IE

where* – don't care for write and zero for read.

F7E Field 7 wrap around carry error; Cleared by CAF, RFSR and RESET.

WOF Logic one indicates word counter overflow; clear by CAF, LWCR and RESET.

CE Carry enable from CA (0-11) to ECA; cleared by RESET.

R/W Logic one indicates DMA write (Port to Memory transfer). Cleared (DMA Read) by RESET.

SR7, 8
- 00 Refresh mode; WC is frozen no UP, DMAEN is don't care.
- 01 Normal mode; DMAEN (H) freezes WC, CA and no UP if WC has not overflowed; Stop if WC overflows.
- 10 Burst mode; DMAEN (H) freezes WC, CA and no UP if WC has not overflowed; refresh condition if WC overflows.
- 11 Stops DMA.

OPERATION

The HD-6102 SDMA channel augments the throughput of the HM-6100 during DMA operations by transferring data between memory and peripheral devices simultaneously with normal processor bus usage. In other words, no memory cycles are "stolen" from the processor; but the DMA address and data are transferred on the bus during periods that the DX bus is inactive.

DMA MODES

SR7 = SR8 = 0 REFRESH MODE

This is the mode to which the 6102 reverts on RESET. The word count register clock input is disabled, the user pulse (DMA data strobe) is suppressed and the DMAEN input is ignored. However, provided valid DMA transfer conditions are met in a particular memory cycle, the DMA sequencer will be started, appropriate timing signals will be generated and the current address register will be clocked. Thus DMA read accesses will be performed continually with an essentially free-running current address register. Read accessess will refresh dynamic memory. No WOF is possible but an F7E is possible if bit SR9 is set, enabling a carry from the current address register to the extended current address register.

SR7 = 0; SR8F = 1 NORMAL MODE

This mode is used for normal SDMA operations with static memory. The following instruction sequence can be used:

```
CLA      /Clear AC
TAD CA   /Get starting address
LCAR     /Load into current address register and clear
          AC
TAD SR   /Get value for DMA status register
LFSR     /Change status (from refresh to normal for
          example)
TAD WC   /Get two's complement of block length
LWCR     /Load word count register and start DMA
          transfers
```

Note that LWCR will start the sequencer so it should be the last instruction in the initialization sequence. The ECA register and vector register could also have been initialized in this sequence.

The SDMA sequencer samples DMAEN on the rising edge of every XTA and latches the condition of the enable line. If DMAEN is low, the sequencer is enabled, external timing signals XTC*, MEMSEL*, UP, LXMAR* are generated, the WC and CA registers are clocked. If DMAEN is high, at XTA (↓) time, the signal is sampled and latched and if the WC has not overflowed, the WC and CA registers are frozen, UP is suppressed. If the WOF condition comes up, the SDMA operation stops, regardless of DMAEN level.

The DMAEN and UP signals provide a simple interlocked handshaking method for transferring data one or more characters at a time (entire blocks) concurrently with processor operations on the bus. Of course, at all times, independent of DMAEN, the SDMA sequencer can proceed only if other bus usage conditions for DMA operations are met (not IOTA, IAUTOI, DCA, JMS, IJMS, ISZ, DMAGNT, or access of location $X0000_8$).

NOTE: IAUTOI is an indirect cycle of any autoindexed instruction; IJMS is indirect cycle of JMS. An autoindexed JMP instruction may not be executed when the DMA mode is active.

SR7 = 1; SR8 = 1 BURST MODE

This mode is the same as the normal mode except when the word count register overflows. When this happens, the SDMA sequencer will set the WOF flag and revert to the refresh mode (ignoring DMAEN, freezing WC and suppressing UP). This mode is used when SDMA operations and dynamic memory refresh must be concurrently performed. The system designer must control the block lengths to be transferred, the refresh interval, and memory system design according to the application and performance desired.

SR7 = 1; SR8 = 1 STOP MODE

In this mode, no SDMA operations will take place. Naturally, cycle stealing DMA is still possible, and indeed may be used in any of the modes but the designer must be aware that cycle stealing may adversely affect dynamic memory refresh intervals. LWCR and LFSR may be executed in either order to change mode and start DMA.

The EMA function of the HD-6102 is program compatible with the DEC PDP-8/E KM8-E Memory Extension option. The purpose of the EMA function is to extend the effective addressing space of the system from 4K to 32K words. To perform this function, the EXTENDED MEMORY CONTROLLER maintains a 3-bit extended address which is decoded by the memory modules to select 1 of 8 memory fields each containing 4096 words of storage. These 4K fields start with FIELD 0 and progress to FIELD 7 when 32K of memory is used. All software communication with the controller is via programmed IOT instructions.

The figure below shows two 3-bit field registers: the Instruction Field, which acts as an extension to the Instruction and directly obtained operand addresses and the Data Field, which augments indirectly obtained operand addresses. The program can, therefore, use one field for instructions and address pointers and another field for data. The selection between Instruction and Data Fields is signalled by the DATAF signal generated by the HM-6100. A discussion of the various registers follows.

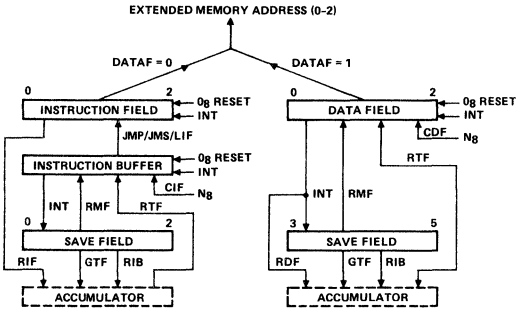


FIGURE 5 – EMA Registers

INSTRUCTION FIELD REGISTER (IF)

The IF is a 3-bit register that serves as an extension of the Program Counter (PC). The IF, however, is not incremented when the PC goes from 7777$_8$ to 0000$_8$. The contents of the IF determine the field from which all instructions are taken. Operands for all directly addressed memory reference instructions also come from the Instruction Field. The indirect pointer for all indirectly addressed memory reference instructions reside in the Instruction Field. The IF is cleared to 0$_8$ and the HM-6100 Program Counter is set to 7777$_8$ by $\overline{\text{RESET}}$.

DATA FIELD REGISTER (DF)

The DF is a 3-bit register which determines the memory field from which operands are fetched in indirectly addressed AND, TAD, ISZ, or DCA instructions. However, the branch address for indirectly addressed JMS or JMP instructions is obtained from the Instruction Field. The Data Field register may be modified under program control. The DF is set to 0$_8$, on reset.

INSTRUCTION BUFFER REGISTER (IB)

The IB is a 3-bit register which serves as an input buffer for the Instruction Field (IF) register. All programmed modifications of the IF register are made through the IB register. The transfer from IB to IF takes place at the beginning of the execute phase of the "next" JMP or JMS instruction or immediately upon execution of an LIF instruction. Using this feature, a program segment can execute an instruction to modify the IF and "exit" the program segment before the actual modification of the IF takes place. If instructions could change the IF directly, it would be impossible to execute the "next" sequential instruction, followed by a Change IF instruction. The IB to IF transfer is inhibited if the JMP/JMS instruction is fetched from control panel memory, which is restricted to 4K, but the LIF instruction is used here to provide the ability to load the IF register from the IB register. This allows the control panel routines to be executed transparently while the IB and IF differ and also yields a method for the panel to extract or alter the status of the primary EMA registers. The IB is set to 0$_8$, on reset. The IB to IF transfer takes place during the second cycle of a JMP/JMS instruction when XTC makes a falling ($\downarrow$) transition.

SAVE FIELD REGISTER (SF)

The SF is a 6-bit register in which the IB and DF registers are saved during an Interrupt Grant. When an Interrupt occurs, the contents of IB and DF are automatically stored in SF (0-2) and SF (3-5), respectively, and the IF, IB and DF registers are cleared. The INTGNT (Interrupt Grant) cycle stores the "current" Program Counter (PC) in location 0000$_8$ of Memory Field 0$_8$ and the CPU resumes operation in location 0001$_8$ of Memory Field 0$_8$. The Instruction Field and Data Field of the program segment being executed by the CPU before the interrupt was acknowledged are available in the SF register.

INTERRUPT INHIBIT FLIP-FLOP

The $\overline{\text{INTREQ}}$ (Interrupt Request) line to the HM-6100 must be "gated" by the Interrupt Inhibit Flip-Flop so that, when the Instruction Field is changed under program control, all interrupts are disabled until a JMP, JMS or LIF instruction is executed. Since the actual modification of the Instruction Field takes place only after the "next" JMP/JMS/LIF, this inhibition of the $\overline{\text{INTREQ}}$'s ensures that the program sequence resumes operation in the "new" memory field before an Interrupt Request is granted.

Since Interrupt Requests are asynchronous in nature, a situation may arise in which an $\overline{\text{INTREQ}}$ is generated when the IF and IB bits are different. The Interrupt Inhibit FF guarantees the structural integrity of the program segment. The IF is cleared on reset.

TABLE 3 – EMA Instructions

MNEMONIC	OCTAL CODE	OPERATION
GTF	6004$_8$	GET FLAGS Operation: AC (0)←LINK AC (2)←INTREQ Line AC (3)←INT INHIBIT FF AC (4)←INT ENABLE FF AC (6-11)←SF (0-5) Description: LINK, INTREQ and INT ENABLE FF are internal to the CPU. The INT INHIBIT FF and SF are in the MEDIC.
RTF	6005$_8$	RETURN FLAGS Operation: LINK←AC (0) IB←AC (6-8) DF←AC (9-11) Description: LINK is restored. All AC bits are available externally during T6 of IOTA to restore other flag bits. The internal Interrupt System is enabled. However, the Interrupt Inhibit FF is set until the "next" JMS/JMP/LIF. The IB is transferred to IF after the "next" JMS/JMP/LIF.
CDF	62N1$_8$	CHANGE DATA FIELD Operation: DF←N$_8$ Description: Change DF register to N (0$_8$-7$_8$).
CIF	62N2$_8$	CHANGE INSTRUCTION FIELD Operation: IB←N$_8$ Description: Change IB to N (0$_8$-7$_8$). Transfer IB to IF after the "next" JMP/JMS/LIF. The Interrupt Inhibit FF is set until the "next" JMP/JMS/LIF.
CDF, CIF	62N3$_8$	CHANGE DF, IF Operation: DF←N$_8$ IB←N$_8$ Description: Combination of CDF and CIF.
RDF	6214$_8$	READ DATA FIELD Operation: AC (6-8)←AC (6-8) + DF Description: OR's the contents of DF into bits 6-8 of the AC. All other bits are unaffected.
RIF	6224$_8$	READ INSTRUCTION FIELD Operation: AC (6-8)←AC (6-8) + IF Description: OR's the contents of IF into bits 6-8 of the AC. All other bits of the AC are unaffected.
RIB	6234$_8$	READ INTERRUPT BUFFER READ SAVE FIELD Operation: AC (6-22)←AC (6-11) + SF Description: OR's the contents of SF into bits 6-11 of the AC. All other bits are unaffected.
RMF	6244$_8$	RESTORE MEMORY FIELD Operation: IB←SF (0-2) DF←SF (3-5) Description: The SF register saves the contents of the IB and DF when an interrupt occurs. This command is used to restore IB and DF when "exiting" from the interrupt service routing in another field. Transfer IB to IF after the next JMP/JMS/LIF. The Interrupt Inhibit Flip-Flop is set until the next JMP/JMS/LIF.
LIF	6254$_8$	LOAD INSTRUCTION FIELD Operation: IF←IB Description: Transfer IB to IF and clear the Interrupt Inhibit FF.

+ "OR"
∧ "AND"
← "IS REPLACED BY"

OPERAND FETCHING

Instructions are accessed from the currently assigned Instruction Field. For indirect AND, TAD, ISZ or DCA instructions, the operand address refers first to the Instruction Field to obtain an Effective Address which in turn refers to a location in the currently addressed Data Field. All instructions and operands are obtained from the field designated by the IF, except for indirectly addressed operands, which are specified by the DF. Thus, DF is active only in the Execute phase of an AND, TAD, ISZ or DCA when it is directly preceded by an Indirect phase.

ADDRESS MODE	IF	DF	AND, TAD, ISZ or DCA
Direct	m	n	Operand in field m.
Indirect	m	n	Absolute address of operand in field m; operand in field n.

Each field of extended memory contains eight auto-index registers in addresses 10 through 17. For example, assume that a program in field 2 is running (IF = 2) and using operands in field 1 (DF = 1) when the instruction TAD I 10 is fetched. The indirect autoindex cycle is entered, and the contents of location 10 in field 2 are read, incremented, and rewritten. If address 10 in field 2 originally contained 0546, it now contains 0547. In the execute cycle, the operand is fetched from location 0547 of field 1.

Program control is transferred between memory fields by the CIF instruction. The instruction does not change the instruction field directly, as this would make it impossible to execute the next sequential instruction; instead, it loads the new instruction field in the IB for automatic transfer into the IF when either a JMP or JMS instruction is executed. The DF is unaffected by the JMP and JMS instructions.

The 12-bit program counter is set in the normal manner and, because the IF is an extension on the most significant end of the PC, the program sequence resumes in the new memory field following a JMP or JMS. Entry into a program interrupt is inhibited after the CIF instruction until a JMP or JMS is executed.

NOTE: The IF is not incremented if the PC goes from 7777_8 to 0000_8. This feature protects the user from accidentally entering a nonexistent field.

To call a subroutine that is out of the current field, the data field register is set to indicate the field of the calling JMS, which establishes the location of the operands as well as the identity of the return field. The instruction field is set to the field of the starting address of the subroutine. The following sequence returns program control to the main program from a subroutine that is out of the current field.

```
/PROGRAM OPERATIONS IN MEMORY FIELD 2
/INSTRUCTION FIELD = 2; DATA FIELD = 2
/CALL A SUBROUTINE IN MEMORY FIELD 1
/INDICATE CALLING FIELD LOCATION BY THE
/CONTENTS OF THE DATA FIELD

        CIF 10          /CHANGE TO INSTRUCTION
                        /FIELD 1 = 6212
        JMS I SUBRP     /SUBRP = ENTRY ADDRESS
        CDF 20          /RESTORE DATA FIELD
          .
          .
          .
SUBRP,  SUBR            /POINTER
                                        FIELD 2
                                        FIELD 1

                        /CALLED SUBROUTINE,
                        /LOCATION IN FIELD 1
SUBR,   0               /RETURN ADDRESS
                        /STORED HERE
        CLA
        RDF             /READ DATA FIELD INTO AC
        TAD RETURN      /CONTENTS OF THE AC =
                        /6202 + DATA FIELD BITS
        DCA EXIT        /STORE CIF N INSTRUCTION
          .             /NOW CHANGE DATA FIELD
          .             /IF DESIRED
          .
EXIT,   0               /A CIF INSTRUCTION
        JMP I SUBR      /RETURN TO CALLING
                        /PROGRAM
RETURN, CIF             /USED TO FORM CIF N
                        /INSTRUCTION
```

When a program interrupt occurs, the current instruction and data field numbers are automatically stored in the 6-bit save field register, then the IF and DF are cleared. The 12-bit program counter is stored in location 0000_8 of field 0_8 and program control advances to location 0001_8 of field 0_8. At the end of the program interrupt subroutine, the RMF instruction restores the IF and DF from the contents of the SF. Alternatively, the GTF and RTF instructions may be used to handle the Save Field and Link information. The following instruction sequence at the end of the program interrupt subroutine continues the interrupted program after the interrupt has been processed.

```
          .
          .
          .
        CLA
        TAD AC          /RESTORE AC
        RMF             /LOAD IB AND DF FROM SF
        ION             /TURN ON INTERRUPT
                        /SYSTEM
        JMP I 0         /RESTORE PC WITH
                        /CONTENTS OF LOCATION
                        /0000₈ AND LOAD
                        /IF FROM IB
```

HM-6100 control panel memory programs, if used must be careful in the manner that EMA register data is manipulated. Control panel interrupt requests bypass the device interrupt enable flip flop, and indeed, are granted even by a halted CPU. The interrups from a control panel may occur at any time, and in particular when the IB and IF registers do not contain the same data. The EMA logic inhibits IB to IF transfers in control panel memory so that panel routines may execute transparently (in particular, JMP/JMS instructions). The panel routines may alter the IF by executing the LIF instructions.

Users should also note that the GTF and RIB instructions read the SF register, and only the RIF instruction reads the IF register. Note also that the SF saves the IB register rather than the IF during an interrupt. However, interrupts are inhibited until the IF and IB registers are the same.

The memory extension controller that we have discussed

in this section shows three important design considerations involved in extending memory addressing space. The first is the concept of having separate instructions and data fields for program flexibility. The second is the importance of double buffering the instruction field register to maintain structural integrity of programs and the third is the provision for saving the current field status upon interrupts and disabling interrupts until a change of instruction field has been completely executed.

C. Programmable Real Time Clock

The programmable real time clock offers the HM-6102 user a number of ways to accurately measure and count intervals in order to implement real time data acquisition and data processing systems. It is similar in functionality to the DEC PDP-8/E DK8-EP Programmable Real Time Clock option.

The crystal used should have the following characteristics:

RS $\leqslant$ 150 ohms
CM = 3-30mpF (10^{-15}F)
CO = 10-15pF

Static capacitance should be around 5pF; for the greatest stability, CO should be around 12pF and the oscillator is parallel resonant.

TABLE 4 – Clock Enable Register Bit Assignments

0	1	2	3	4	5	6	7	8	9	10	11
EN0	*	EN2	EN3	EN4	EN5	*	EN7	*	*	*	*

*Don't care for write and zero for read.

Where EN0 When set to 1, enables clock overflow (COF flag) to cause an interrupt. Cleared by $\overline{\text{RESET}}$, CAF.

EN2 When reset to a 0-counter runs at selected rate. Overflow occurs every 4096 (2^{12}) counts. COF flag remains set until cleared by either IOT 6135 (CLSA), or CAF, or $\overline{\text{RESET}}$.

When set to a 1-counter runs at selected rate. If the COF flag is cleared, overflow causes clock buffer to be transferred to the clock counter which continues to run. COF flag remains set until cleared with IOT 6135 (CLSA). Also cleared by $\overline{\text{RESET}}$, CAF.

EN3, 4, 5 Assuming a 2MHz crystal oscillator cleared by $\overline{\text{RESET}}$, CAF.

EN3	EN4	EN5	Octal	Interval Between Pulses	Frequency
0	0	0	0	Stop	0
0	0	1	1	Stop	0
0	1	0	2	20msec	50Hz
0	1	1	3	2msec	500Hz
1	0	0	4	200μsec	5kHz
1	0	1	5	20μsec	50kHz
1	1	0	6	2μsec	500kHz
1	1	1	7	Stop	0

EN7 Inhibits clock prescaler when set to 1; cleared by $\overline{\text{RESET}}$ or CAF. EN3-5 and EN7 should not be changed simultaneously.

A discussion of the Real Time Clock registers as shown in Figure 6 follows:

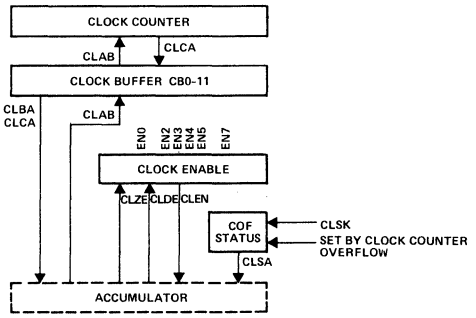


FIGURE 6 – RTC Registers

CLOCK ENABLE REGISTER

This register controls the mode of counting, whether clock interrupts are allowed, and the rate of the time base of the clock. For a description, refer to the register bit assignment.

CLOCK BUFFER REGISTER (CB)

This 12-bit register stores data being transferred from the AC to the clock counter, or from the clock counter to the AC. It also permits presetting of the clock counter.

CLOCK COUNTER REGISTER (CC)

This register is a 12-bit binary counter that may load the clock buffer or be loaded from it. It is driven by a 2MHz crystal oscillator with the proper predivision set by the time base selection. When an overflow occurs and if bit 0 of the clock enable register is a logic one, an interrupt is requested. If bit 2 is also 1, overflow causes the clock buffer to be transferred automatically into the clock counter.

TIME BASE MULTIPLEXER

The multiplexer provides count pulses to the clock counter according to the rate set by the clock enable register. Use of other than a 2MHz crystal for the clock will result in proportionately different time bases.

CLOCK OVERFLOW FLAG

This flag is set by a clock counter overflow. It is cleared by CAF, CLSA and $\overline{\text{RESET}}$. Its complement provides LSB (VR11) of interrupt vector. If EN0 of clock enable counter is set, COF can cause an interrupt request. The COF is set when the MSB of the counter makes a "1" to "0" transition.

TABLE 5 – RTC Instructions

MNEMONIC	OCTAL CODE	OPERATION
CLZE	6130$_8$	CLEAR ENABLE REGISTER PER AC Description: Clears the bits in the clock enable register corresponding to those bits set in the AC. The AC is not changed.
CLSK	6131$_8$	SKIP ON CLOCK INTERRUPT Description: Causes the program counter to be incremented by one if clock interrupt conditions exists, so that the next sequential instruction is skipped.
CLOE	6132$_8$	SET ENABLE REGISTER PER AC Description: Sets the bits in the clock enable register corresponding to those bits set in the AC. The AC is not changed.
CLAB	6133$_8$	TRANSFER AC TO CLOCK BUFFER Description: Causes the contents of the AC to be transferred to the Clock Buffer, then causes the contents of the Clock Buffer to be transferred to the Clock Counter. The AC is not changed.
CLEN	6134$_8$	READ CLOCK ENABLE REGISTER Description: Causes contents of the Clock Enable Register to be transferred into the AC.
CLSA	6135$_8$	READ CLOCK STATUS Description: Interrogates the clock overflow status flip flop by clearing AC, then transferring clock status into AC bit 0. COF is cleared.
CLBA	6136$_8$	READ CLOCK BUFFER Description: Clears the AC, then transfers the contents of the Clock Buffer into the AC.
CLCA	6137$_8$	READ CLOCK COUNTER Description: Clears the AC, transfers the contents of the Clock Counter to the Clock Buffer, then transfers the contents of the Clock Buffer into the AC. If EN7 is set to 1 (clock prescaler is inhibited), the CLCA instruction increments the prescaler input by one. If the clock is in the "stop" mode but EN7 is not inhibited, the prescaler will not be clocked by the CLCA instruction.
CAF	6007$_8$	CLEAR ALL FLAGS Description: Clears COF flag (and also F7E, WOF flags), clock enable and clock buffer registers.

System Considerations

The HD-6102 is the highest priority device in a priority interrupt scheme. It provides an active low signal on pin 40, POUT, to signal the next lower priority device in the chain (thus, a high level on POUT indicates that the 6102 is not requesting an interrupt) via its "priority-in", PRIN, input.

The HD-6102 when requesting an interrupt activates the $\overline{\text{SKP/INT}}$ line low on pin 35 and the POUT line low on pin 40 if its interrupt inhibit flip-flop is not set.

The IOT instructions used by the HD-6102 preclude the use of certain device addresses when the system uses HD-6101 PIEs. The addresses that may not be used are those given by bits 3 through 7 of the IOT instructions that are used with the HD-6102. These addresses are 00101, 01000, 01001, 01010, 01011 corresponding to IOT instructions 612X, 613X, 620X, 621X, 622X, 623X, 624X, 625X, 626X and 627X.

The HD-6102 does not generate $\overline{\text{DMAREQ}}$ signals to the 6100 because of its simultaneous use of the DX bus. It monitors the DMAGNT signal in order to place the EMA0, 1, 2 lines on pins 36, 37, 38 in a high impedance state while DMAGNT is high.

If the application requires other peripherals requiring direct memory access on a cycle stealing basis, for example, bus contention problems will be resolved by the HD-6102 as it monitors the DMAGNT line and gets off the bus (by placing all lines in the high impedance state) when DMAGNT is active.

If interrupts are enabled and a request is pending, during the first INTGNT cycle, the HD-6102 will detect the referencing of location 0000$_8$ by the HM-6100 in order to save the PC and will suspend simultaneous DMA during that cycle. The logic will in fact suspend simultaneous DMA in any cycle that location 0000$_8$ is referenced, either in main memory or control panel memory.

This makes it possible to disable automatic interrupt vectoring by grounding the INTGNT line to the HD-6102. This will not affect the generation of $\overline{\text{INTREQ}}$ so the HM-6100 will have to poll peripheral devices (skip on flag instructions) to determine the interrupting source.

Grounding INTGNT is not possible in extended memory applications since the INTGNT signal is used to save the Instruction Buffer and Data Field Register and clear the IF, IB and DF registers. (All peripheral device interrupt service routines have their entry point at location 0001$_8$ of Memory Field 0$_8$.)

If no interrupt requests are pending in the 6102 (COF, F7E or WOF) from the DMA or RTC functions, the HD-6102 interrupt request flip-flop is clear and POUT, the priority out signal, is high, enabling interrupt requests downstream in the priority chain. In the event that interrupts are enabled (DMA status bit SR11 is set and/or clock enable bit EN0 is set) and an interrupting condition occurs (F7E, WOF, COF), the POUT signal goes low asynchronously disabling interrupt vectors downstream.

If the Interrupt Inhibit Flip-Flop is not set, the $\overline{SKP}/\overline{INT}$ line is driven low by the interrupt request. If the IIFF is set, the $\overline{SKP}/\overline{INT}$ line stays high until the IIFF is cleared (by $\overline{RESET}$ or an IB to IF transfer) at which time $\overline{SKP}/\overline{INT}$ may be driven low. Skip requests will always propagate independently of IIFF during IOTA $\wedge$ $\overline{DEVSEL}$ $\wedge$ XTC.

Interrupt request from devices downstream of the HD-6102 must also be channeled via the HD-6102 in order that the IIFF may condition the request timing. The HD-6102 provides a built in pull-up on the $\overline{SKP}/\overline{INTX}$ line coming in from devices downstream in the priority chain. At 5V, the pull-up looks like a 10K resistor; at 10V, it looks like 5K.

The execution of any IOT instruction will reset INTGNT to a low level at the end of IOTA time. This IOT instruction will be the first instruction in the interrupt service routine after saving status. If hardware vectoring is being used, any IOT instruction when INTGNT is high will cause the HD-6102 to place a vector address on the bus if it requested an interrupt and pull the $\overline{C1}$ and $\overline{C2}$ lines low, thus placing the vector in PC and forcing a branch to the service routine. If the $\overline{C2}$ line is left unconnected, the vector address will not be forced into the PC, but will be OR'ed into the AC. The interrupt service routine would have to execute a CLA after its first IOT instruction in order to clear the AC. Note that the LSB of the vector address is determined by the complement of the COF flag and that a DMA interrupt service routine must distinguish between the two possible interrupting conditions, a word count overlfow or a field 7 wrap-around error. The programmer may read the DMA status register with an RFSR instruction and also test the WOF flag with a skip instruction, SKOF. The COF flag may also be tested with the CLSK skip instruction. The flag may be read (and cleared) with the CLSA instruction. The skip instructions cause the $\overline{SKP}/\overline{INT}$ line to go low during IOTA $\wedge$ XTC time if the flag being tested is set. At all other times, the $\overline{SKP}/\overline{INT}$ line carries interrupt requests as modified by the HD-6102 interrupt inhibit logic. The flags must always be explicitly cleared by the interrupt service routine.

The DMA transfer rate depends on the program. The minimum rate would be obtained if the processor was executing an autoindexed DCA or an indirect JMS (even if non-autoindexed, DMA is suppressed during indirect phase of JMS). Continuously executing these instructions would cause DMA transfers to occur only every third memory cycle (IFETCH). The maximum rate could be obtained by executing a "JMP ." loop (JMP to itself); data would be transferred on every cycle and the interrupt routine entered when word count overflows could bump the return address out of the loop.

In dynamic memory systems it should be noted that the $\overline{MEMSEL}$* signal narrows when the mode changes from write to refresh (burst mode). $\overline{RESET}$ signals may need to be limited in duration to prevent loss of memory data in dynamic memory systems.

The accuracy of the clock counter in the programmable real time clock section of the HD-6102 is as follows:

CASE 1 Counter running; CC loaded from AC via CB using instruction CLAB (IOT 6133) accuracy is 0 to +11 count.

CASE 2: CC loaded from CB automatically on overflow; the accuracy of counting is then only dependent on accuracy of oscillator.

HD-6102 users who do not need all the capabilities of the device may improve systems performance by not using some of the features. To do this properly, certain pins on the device will become unused. The following table summarizes what may be done with certain pins when using only part of the HD-6102 functions. All unlisted pins must be used when implementing any of the three basic features.

PIN NUMBER	PIN NAME	RTC ONLY	SDMA ONLY	EMC ONLY	EMC & DYNAMIC REFRESH
2	DMAEN	GND	USED	GND	GND
3	DMAGNT	USED	USED	USED	USED
6	$\overline{MEMSEL}$*	N/C	USED	N/C	USED
8	$\overline{UP}$	N/C	USED	N/C	N/C
11	LXMAR*	N/C	USED	N/C	USED
12	XTC*	N/C	USED	N/C	USED
15	$\overline{SKP}/\overline{INTX}$	VCC	VCC	USED	USED
29	OSCIN	USED	GND	GND	GND
31	OSC OUT	USED	N/C	N/C	N/C
34	C2	USED	USED	N/C	N/C
36	EMA0	N/C	N/C	USED	USED
37	EMA1	N/C	N/C	USED	USED
38	EMA2	N/C	N/C	USED	USED
40	PROUT	USED	USED	N/C	N/C

MNEMONIC	OCTAL CODE	I/O CONTROL LINES				OPERATION
		$\overline{SKP}$	$\overline{C0}$	$\overline{C1}$	$\overline{C2}$	
GTF	6004	1	0	0	1	(1) Get Flags
IOF	6002	1	1	0	0	(2) Interrupt Off
RTF	6005	1	1	1	1	(3) Restore Flags
CAF	6007	1	1	1	1	(4) Clear All Flags
CDF	62N1	1	1	1	1	Change Data Field
CIF	62N2	1	1	1	1	Change Instruction Field
CDF CIF	62N3	1	1	1	1	Combination of CDF & CIF
RDF	6214	1	1	0	1	Read Data Field
RIF	6224	1	1	0	1	Read Instruction Field
RIB	6234	1	1	0	1	Read Interrupt Buffer
RMF	6244	1	1	1	1	Restore Memory Field
LIF	6254	1	1	1	1	Load Instruction Field
CLZE	6130	1	1	1	1	Clear Clock Enable Register per AC
CLSK	6131	0	1	1	1	Skip on Clock Overflow Interrupt
CLOE	6132	1	1	1	1	Set Clock Enable Register per AC
CLAB	6133	1	1	1	1	AC to Clock Buffer
CLEN	6134	1	0	0	1	Load Clock Enable Register into AC
CLSA	6135	1	0	0	1	Clock Status to AC
CLBA	6136	1	0	0	1	Clock Buffer to AC
CLCA	6137	1	0	0	1	Clock Counter to AC
LCAR	6205	1	0	1	1	Load Current Address Register
RCAR	6215	1	0	0	1	Read Current Address Register
LWCR	6225	1	0	1	1	Load Word Count Register
LEAR	62N6	1	1	1	1	Load Extended Current Address Register
REAR	6235	1	1	0	1	Read Extended Current Address Register
LFSR	6245	1	0	1	1	Load DMA Flags and Status Register
RFSR	6255	1	1	0	1	Read DMA Flags and Status Register
SKOF	6265	0	1	1	1	Skip on Word Count Overflow
WRVR	6275	1	0	1	1	Write Vector Register

NOTES:

(1) The internal flags of the HM-6100 are defined as follows: LINK → AC(0); INTREQ → AC(2); and INTERRUPT ENABLE FF → AC(4)

(2) The IOF instruction is used in conjunction with the vector interrupt operation. (See System Considerations.)

(3) When RTF is executed, the LINK is restored from AC(0) and the Interrupt System is enabled after the next sequential instruction is executed. The Interrupt Inhibit FF is set preventing interrupts until the next JMP, JMS, or LIF instruction is executed.

(4) A hardware $\overline{RESET}$ clears F7E, WOF, IIFF, and COF. The IF and DF are cleared to 0$_8$. The DMA status register, the Clock Enable register, and the Counter/Buffer are cleared.

Summary of HD-6102 Bit Assignments

	DX0	DX1	DX2	DX3	DX4	DX5	DX6	DX7	DX8	DX9	DX10	DX11
Current Address	CA0	CA1	CA2	CS3	CA4	CA5	CA6	CA7	CA8	CA9	CA10	CA11
Extended Current Address							ECA0	ECA1	ECA2			
Word Count	WC0	WC1	WC2	WC3	WC4	WC5	WC6	WC7	WC8	WC9	WC10	WC11
DMA Status (1)						SR5	SR6	SR7	SR8	SR9	SR10	SR11
Interrupt Vector (2)	VR0	VR1	VR2	VR3	VR4	VR5	VR6	VR7	VR8	VR9	VR10	VR11
RIF Instruction (3)							IF0	IF1	IF2			
RTF, CIF Instruction							IB0	IB1	IB2			
GTF, RIB Instruction				IIFF(4)			SF0	SF1	SF2	SF3	SF4	SF5
CDF, RDF Instruction							DF0	DF1	DF2			
RTF Instruction										DF0	DF1	DF2
Clock Enable (5)	EN0		EN2	EN3	EN4	EN5		EN7				
Clock Buffer	CB0	CB1	CB2	CB3	CB4	CB5	CB6	CB7	CB8	CB9	CB10	CB11
Clock Overflow (6)	COF											

(1) DMA STATUS

SR5 Set if Field 7 wraparound carry error – F7E; cleared by CAF, RFSR (at IOTA∧XTC time), $\overline{\text{RESET}}$.

SR6 Set if DMA Word Counter Overflow – WOF; Cleared by CAF, LWCR, $\overline{\text{RESET}}$.

(READ ONLY BITS)

SR7 Mode Bit 7

SR8 Mode Bit 8

;cleared by $\overline{\text{RESET}}$ (REFRESH MODE). See below.

SR9 Carry enable from CA0-11 to ECA2 if set – CE.

SR10 DMA Write if set.

SR11 Enable F7E or WOF interrupt if set – IE.

(2) VR0-10 Loaded from AC. VR11 is equivalent to COF.

(3) IF Instruction Field; cleared to 0_8 by $\overline{\text{RESET}}$ and INTGNT.

(4) IIFF Interrupt Inhibit Flip Flop; set whenever IB ≠ IF; (CIF, CDF/CIF, RMF, RTF) cleared by $\overline{\text{RESET}}$ and IB ⟶ IF transfer.

(5) EN0 Enable Clock Overflow (COF) interrupt; cleared (interrupt disable) by $\overline{\text{RESET}}$, CAF.

EN2 When set causes clock buffer to be transferred to clock counter on COF. Counter runs at selected rate; COF remains set until cleared with CLSA. When cleared to 0, counter runs at selected rate, overflow occurs every 2^{12} counts and COF remains set. EN2 is cleared by $\overline{\text{RESET}}$, CAF.

EN3,4,5 Select interval between pulses. Cleared to 000 by $\overline{\text{RESET}}$ (counter disabled), CAF see below.

EN7 Inhibits clock prescaler when set. Cleared by $\overline{\text{RESET}}$, CAF.

(6) COF Clock Overflow status bit; cleared by CAF, $\overline{\text{RESET}}$ and CLSA; complement provides LSB of interrupt vector.

SR7,8
- 00 Refresh mode; WC is frozen, no $\overline{\text{UP}}$, DMAEN don't care.
- 01 Normal mode; DMAEN (H) freezes WC, CA and no $\overline{\text{UP}}$ if WC has not overflowed; stop if WC overflows.
- 10 Burst mode; DMAEN (H) freezes WC, CA and no $\overline{\text{UP}}$ if WC has not overflowed; reverts to refresh mode if WC overflows.
- 11 Stops SDMA

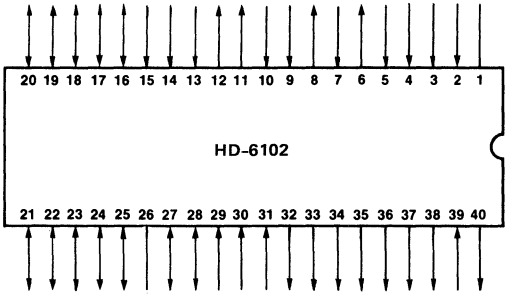
EN3,4,5 with 2MHz clock
- 000 STOP
- 001 STOP
- 010 20ms interval
- 011 2ms interval
- 100 200μs interval
- 101 20μs interval
- 110 2μs interval
- 111 STOP

NOTES:
1. Bits SR7 and 8 do not change when the DMA controller stops or reverts to refresh mode as a result of WC overflow.
2. The "overflow" status is defined as set when the most significant bit of a counter makes a "1" to "0" transition.

HD-6102 Functional Pin Description

PIN	SYMBOL	INPUT/ OUTPUT	DESCRIPTION
1	VCC		Supply voltage
2	DMAEN	I	Enable the HM-6102 DMA channel to transfer data
3	DMAGNT	I	Direct memory access grant from CPU
4	$\overline{\text{MEMSEL}}$	I	Memory select for read or write from CPU
5	IFETCH	I	CPU flag indicating instruction fetch cycle
6	$\overline{\text{MEMSEL}}$*	O	Memory select generated by the HM-6102
7	$\overline{\text{RESET}}$	I	Asynchronous reset will clear Instruction Field to 08, disable all interrupts, initialize DMA port to READ/REFRESH, initialize timer to "stop", "divide by 2^{12} mode" and "enable divide counters"
8	$\overline{\text{UP}}$	O	User pulse (read or write)
9	XTA	I	CPU external minor cycle timing signal

PIN	SYMBOL	INPUT/ OUTPUT	DESCRIPTION
10	LXMAR	I	A falling edge of LXMAR pulse from CPU will load external memory address register
11	LXMAR*	O	LXMAR generated by the HM-6102
12	XTC*	O	XTC generated by the HM-6102
13	XTC	I	CPU external minor cycle timing signal.
14	CLOCK	I	Oscillator OUT pulses from CPU for timing the HM-6102 DMA transfers
15	$\overline{\text{SKP}}/\overline{\text{INTX}}$	I	Multiplexed $\overline{\text{SKP}}/\overline{\text{INT}}$ line from lower priority devices
16	DX0	I/O	Most significant bit of the 12-bit multiplexed address and data I/O bus
17	DX1	I/O	See pin 16-DX0
18	DX2	I/O	See pin 16-DX0
19	DX3	I/O	See pin 16-DX0
20	DX4	I/O	See pin 16-DX0



PIN	SYMBOL	INPUT/ OUTPUT	DESCRIPTION
21	DX5	I/O	See pin 16-DX0
22	DX6	I/O	See pin 16-DX0
23	DX7	I/O	See pin 16-DX0
24	DX8	I/O	See pin 16-DX0
25	DX9	I/O	See pin 16-DX0
26	GND	I/O	Power supply
27	DX10	I/O	See pin 16-DX0
28	DX11	I/O	See pin 16-DX0
29	OSCIN	I	Crystal input for timer oscillator
30	$\overline{\text{DEVSEL}}$	I	Device select for read or write from CPU
31	OSC OUT	O	See pin 29

PIN	SYMBOL	INPUT/ OUTPUT	DESCRIPTION
32	$\overline{\text{C0}}$	O	Control lines to CPU determining type of peripheral data transfer
33	$\overline{\text{C1}}$	O	See pin 32-$\overline{\text{C0}}$
34	$\overline{\text{C2}}$	O	See pin 32-$\overline{\text{C0}}$
35	$\overline{\text{SKP}}/\overline{\text{INT}}$	O	Multiplexed $\overline{\text{SKP}}/\overline{\text{INT}}$ input to the CPU
36	EMA0	O	Extended memory address field (most significant bit)
37	EMA1	O	Extended memory address field
38	EMA2	O	Extended memory address field
39	INTGNT	I	CPU interrupt grant
40	POUT	O	Priority out for vectored interrupt

NOTE: All DX lines are bi-directional with three-state outputs: Pins 4, 8, 11, 12, 35, 40 have active pullups; pins 32, 33, 34 have open drain outputs; pin 15 has a resistive input pullup; all inputs and outputs protected with resistors and clamp diodes.

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

Advance Information

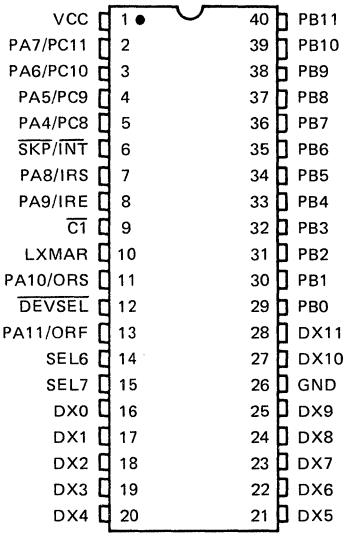
HD-6103

CMOS PARALLEL INPUT/OUTPUT PORT (PIO)

Features

- HM-6100 COMPATIBLE
- LOW POWER - TYP. < 5.0μW STANDBY
- SINGLE SUPPLY 4-11 VOLT
- FULL TEMPERATURE RANGE -55°C TO +125°C
- STATIC OPERATION
- IDEAL FOR MINIMUM SYSTEMS
- 20 PROGRAMMABLE BI-DIRECTIONAL I/O PINS
- THREE MODES OF OPERATION
- SOFTWARE POLLED INTERRUPTS
- UP TO 4 PIO'S PER SYSTEM
- 16 INSTRUCTIONS FOR PIO CONTROL

Pinout

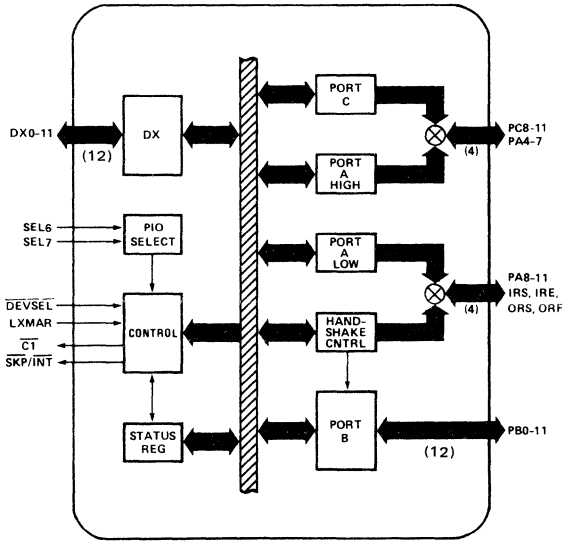


Description

The HD-6103 Parallel Input/Output Port (PIO) is a high speed, low power, silicon gate CMOS general purpose device which provides parallel data transfers and interrupt control for a variety of peripheral functions, such as displays, keyboards, A/D converters, etc. Data transfers between the HD-6103 are via Input/Output Transfer (IOT) instructions, control lines and DX bus. The PIO is ideal for minimum system configurations.

The HD-6103 has 20 I/O pins that are programmable in groups of 4, 8, or 12 bits via three modes of operation. In one mode, 4 of the pins are utilized as handshake control lines.

Functional Diagram



2

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+12.0V
Input or Output Voltage Applied	Gnd. -0.3V to VCC +0.3V
Storage Temperature Range	-65°C to 150°C
Operating Temperature Range	
Industrial HD-6103A-9	-40°C to +85°C
Military HD-6103A-2	-55°C to +125°C

ELECTRICAL CHARACTERISTICS

VCC = 10.0 ± 0.5% Volts, TA = Industrial or Military

2 D.C.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
VIH	Logical "1" Input Voltage	70% VCC			V	
VIL	Logical "0" Input Voltage			20% VCC	V	
IIL	Input Leakage	1.0		1.0	μA	$0V \leq VIN \leq VCC$
VOH	Logical "1" Output Volt.(1)	VCC-2.0			V	IOH = -0.2mA
VOL	Logical "0" Output Voltage			0.45	V	IOL = 2.0mA
IO	Output Leakage	-1.0		1.0	μA	$0V \leq VO \leq VCC$
ICC	Supply Current (static)		1.0	800	μA	VIN = VCC, Freq. = 0
CI	Input Capacitance (2)		5	7	pF	
CO	Output Capacitance (2)		8	10	pF	
CIO	Input/Output Capacitance (2)		8	10	pF	

Notes: (1) Except pins 6, 9
(2) Guaranteed and sampled, but not 100% tested.

A.C.

		TA = 25°C VCC = 10V			
SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
tLX	LXMAR Pulse Width	100		ns	CL = 50pF
tAS	Address Set-Up Time	20		ns	See Timing Diagram
tAH	Address Hold Time	40		ns	
tDC	Delay: $\overline{DEVSEL}$ to $\overline{C1}$		80	ns	
tDI	Delay: $\overline{DEVSEL}$ to $\overline{SKP}/\overline{INT}$		90	ns	
tDA	Delay: $\overline{DEVSEL}$ to DX		100	ns	
tDS	Data Setup Time	10		ns	
tDH	Data Hold Time	50		ns	
tDPO	Delay: $\overline{DEVSEL}$ to Port Data		10	ns	
tPSLX	Port Data Setup LXMAR	10		ns	
tPHLX	Port Data Hold LXMAR	50		ns	
tPSIR	Port Data Setup IRS	5		ns	
tPHIR	Port Data Hold IRS	50		ns	
tPEN	Port B Enable Time		75	ns	
tPDIS	Port B Disable Time		75	ns	
tDR	Delay: IRS to IRE				
	ORS to ORF				
	$\overline{DEVSEL}$ to IRE				
	$\overline{DEVSEL}$ to ORF		150	ns	

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	Gnd. -0.3V to VCC +0.3V
Storage Temperature Range	-65°C to 150°C
Operating Temperature Range	
Industrial HD-6103-9	-40°C to +85°C
Military HD-6103-2	-55°C to +125°C

ELECTRICAL CHARACTERISTICS

VCC = 5.0 ± 10% Volts, TA = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
VIH	Logical "1" Input Voltage	70% VCC			V	
VIL	Logical "0" Input Voltage			20% VCC	V	
IIL	Input Leakage	-1.0		1.0	μA	$0V \leq VIN \leq VCC$
VOH	Logical "1" Output Volt.(1)	2.4			V	IOH = -0.2mA
VOL	Logical "0" Output Voltage			0.45	V	IOL = 2.0mA
IO	Output Leakage	-1.0		1.0	μA	$0V \leq VO \leq VCC$
ICC	Supply Current (static)		1.0	100	μA	VIN = VCC, Freq. = 0
CI	Input Capacitance (2)		5	7	pF	
CO	Output Capacitance (2)		8	10	pF	
CIO	Input/Output Capacitance (2)		8	10	pF	

Notes: (1) Except pins 6, 9
(2) Guaranteed and sampled, but not 100% tested.

A.C.

		TA = 25°C VCC = 5.0V			
SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
tLX	LXMAR Pulse Width	200		ns	CL = 50pF
tAS	Address Setup Time	40		ns	See Timing Diagram
tAH	Address Hold Time	80		ns	
tDC	Delay: $\overline{DEVSEL}$ to $\overline{C1}$ $\overline{C2}$		160	ns	
tDI	Delay: $\overline{DEVSEL}$ to $\overline{SKP}/\overline{INT}$		180	ns	
tDA	Delay: $\overline{DEVSEL}$ to DX		200	ns	
tDS	Data Setup Time	20		ns	
tDH	Data Hold Time	100		ns	
tDPO	Delay: $\overline{DEVSEL}$ to Port Data		20	ns	
tPSLX	Port Data Setup LXMAR	20		ns	
tPHLX	Port Data Hold LXMAR	100		ns	
tPSIR	Port Data Setup IRS	10		ns	
tPHIR	Port Data Hold IRS	100		ns	
tPEN	Port B Enable Time		150	ns	
tPDIS	Port B Disable Time		150	ns	
tDR	Delay: IRS to IRE				
	ORS to ORF				
	$\overline{DEVSEL}$ to IRE				
	$\overline{DEVSEL}$ to ORF		300	ns	

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	Gnd. -0.3V to VCC +0.3V
Storage Temperature Range	-65°C to 150°C
Operating Temperature Range	
Industrial HD-6103C-9	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

VCC = 5.0 ± 5% Volts, TA = Industrial

2 D.C.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
VIH	Logical "1" Input Voltage	70% VCC			V	
VIL	Logical "0" Input Voltage			.8	V	
IIL	Input Leakage	-10		+10	μA	$0V \leq VIN \leq VCC$
VOH	Logical "1" Output Volt. (1)	2.4			V	IOH = -0.2mA
VOL	Logical "0" Output Voltage			0.45	V	IOL = 1.6mA
IO	Output Leakage	-10		+10	μA	$0V \leq VO \leq VCC$
ICC	Supply Current (static)		1.0	500	μA	VIN = VCC, Freq. = 0
CI	Input Capacitance (2)		5	7	pF	
CO	Output Capacitance (2)		8	10	pF	
CIO	Input/Output Capacitance (2)		8	10	pF	

Notes: (1) Except pins 6, 9
(2) Guaranteed and sampled, but not 100% tested.

A.C.

		TA = 25°C VCC = 5.0V			
SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
tLX	LXMAR Pulse Width	230		ns	CL = 50pF
tAS	Address Setup Time	80		ns	See Timing Diagram
tAH	Address Hold Time	120		ns	
tDC	Delay: $\overline{DEVSEL}$ to $\overline{C1}$ $\overline{C2}$		190	ns	
tDI	Delay: $\overline{DEVSEL}$ to $\overline{SKP/INT}$		210	ns	
tDA	Delay: $\overline{DEVSEL}$ to DX		250	ns	
tDS	Data Setup Time	30		ns	
tDH	Data Hold Time	120		ns	
tDPO	Delay: $\overline{DEVSEL}$ to Port Data		40	ns	
tPSLX	Port Data Setup LXMAR	30		ns	
tPHLX	Port Data Hold LXMAR	120		ns	
tPSIR	Port Data Setup IRS	20		ns	
tPHIR	Port Data Hold IRS	120		ns	
tPEN	Port B Enable Time		175	ns	
tPDIS	Port B Disable Time		175	ns	
tDR	Delay: IRS to IRE				
	ORS to ORF				
	$\overline{DEVSEL}$ to IRE				
	$\overline{DEVSEL}$ to ORF		340	ns	

Timing Diagram

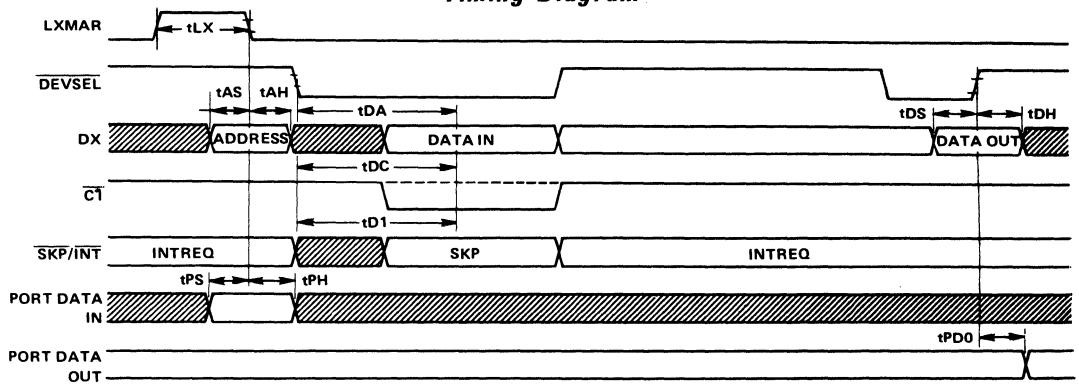


FIGURE 1-1 – HD-6103 PIO Timing Diagram

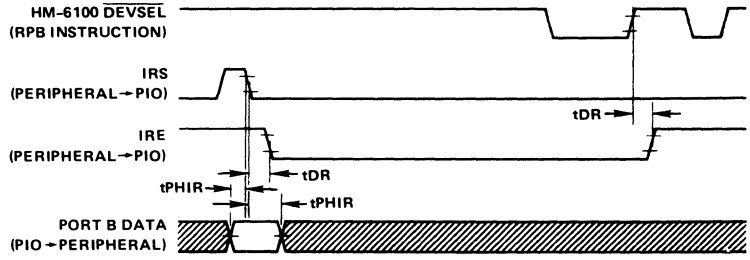


FIGURE 1-2 – Input Data Transfer (Peripheral device to PIO)

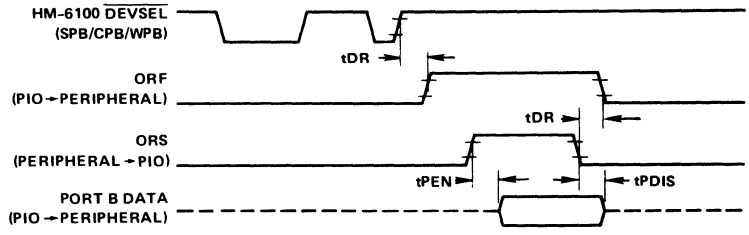


FIGURE 1-3 – Output Data Transfer (PIO to Peripheral device)

HD-6103 System Timing

The three-state bi-directional 12-bit DX bus is used to transfer data and control information (Fig. 3) between the HD-6103 and the HM-6100 microprocessor. The HM-6100 transmits the device address and control information on the DX bus during the 'execute' phase of an Input-Out put Transfer (IOT) instruction. The HD-6103 accepts this information on the falling edge of the LXMAR (Address Latch Enable) Signal.

The address bits (6-7) are compared with the chip select inputs (SEL6 and SEL7) to address 1 of 4 PIO's. The IOT address bits (3-5) are programmed internally to respond to the bit pattern 011. The SEL6 and SEL7 inputs should be externally hard-wired to match the DX6 and DX7 chip select bits. As shown in Fig. 3, $\overline{\text{DEVSEL}}$ goes low, during the first half of an IOT execute machine cycle for a read operation and it goes low again in the second half for a write operation. The HD-6103 responds to a 'read' instruction by putting data on the DX bus and $\overline{\text{C1}}$ output (of HM-6100) low when $\overline{\text{DEVSEL}}$ (from HM-6100) input is low. $\overline{\text{C1}}$ line goes low to indicate an input transfer cycle to the HM-6100. All PIO data transfers to the HM-6100 Accumulator (AC) is an 'OR' transfer, (i.e., PIO data is OR'ed into the contents of the AC).

During the write operation into PIO, the PIO accepts data from the HM-6100 Accumulator on the rising edge of the $\overline{\text{DEVSEL}}$. During and after the PIO write, the contents of the accumulator are not cleared.

$\overline{\text{SKP/INT}}$ line goes low during the 'read' $\overline{\text{DEVSEL}}$ if the HD-6103 is responding to a 'skip' instruction, and the 'skip' condition is met, therefore causing the HM-6100 to skip the next sequential instruction. $\overline{\text{SKP/INT}}$ line reflects the interrupt request status of the HM-6100 at all times except during the 'read' $\overline{\text{DEVSEL}}$. The $\overline{\text{SKP/INT}}$ line goes low if an active interrupt request is pending. During read $\overline{\text{DEVSEL}}$ mode, the $\overline{\text{SKP/INT}}$ indicates the current skip condition. The bits are interpretted as shown below:

Note: Both $\overline{\text{CI}}$ and $\overline{\text{SKP/INT}}$ are open drain outputs which are wire OR'd with outputs from other HM-6100 peripheral controllers.

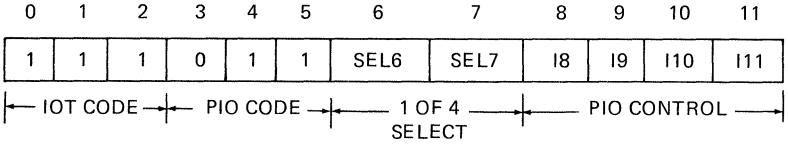


FIGURE 2 – PIO Instruction Format

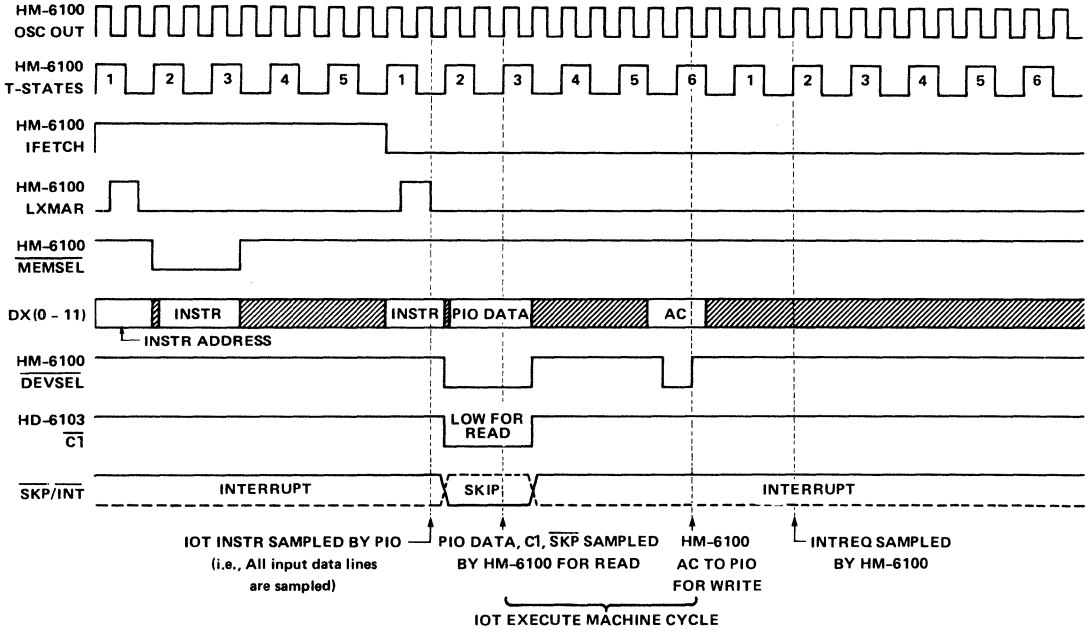


FIGURE 3 – HD-6103 System Timing Diagram

Operation of Port Buffers

The HD-6103 has 20 I/O pins which can be individually programmed in groups of 4, 8 or 12 bits in three different modes of operation.

In mode 11, the 20 I/O lines are divided into three ports:

- Port A with 4 bits (PA8 - PA11)
- Port B with 12 bits (PB0 - PB11)
- Port C with 4 bits (PC8 - PC11)

In mode 10, the 20 I/O lines are grouped into 2 ports:

- Port A with 8 bits (PA4 - PA11)
- Port B with 12 bits (PB0 - PB11)

The four I/O lines associated with Port C in Mode 11 (PC8 - PC11) are allocated to Port A as PA4 - PA7.

In mode 0X, there are two ports - Port B with 12 bits and Port C with 4 bits and four lines for handshake control logic. Four lines of Port A in Mode 11 (PA8 - PA11) are reassigned as handshake control lines. They are:

- Input Register Strobe (IRS)
- Input Register Empty (IRE)
- Output Register Strobe (ORS)
- Output Register Empty (ORE)

The handshake logic controls the data transfer for the Port B. Port C operation remains the same as in Mode 11.

For an 'input' transfer in 0X Mode, the input register empty (IRE) output goes high to indicate to the peripheral device that the input register is empty (as shown in Fig. 4).

The peripheral device may then strobe in the new data into Port B with Input Register Strobe (IRS). At this time, IRE goes low to indicate to the peripheral device that the input buffer is full, and remains low until Port B has been read by the HM-6100 microprocessor. IRE then goes high after the HM-6100 executes a Read Port B (RPB) instruction to initiate another input sequence. The data into Port B should be valid only for a short duration before and after IRS makes the 1 to 0 transition.

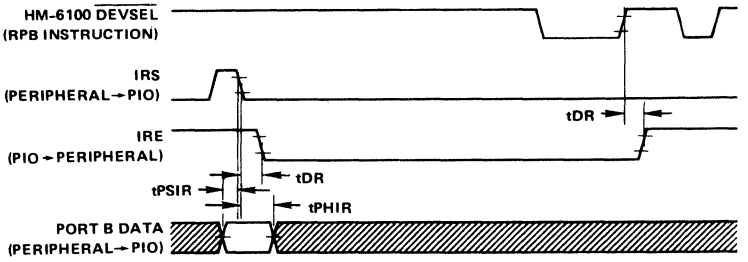


FIGURE 4 – Input Data Transfer (Peripheral device to PIO)

For an 'output' transfer in 0X mode, the HM–6100 microprocessor writes the data into Port B and its timing is shown in Fig. 5. ORF line from the PIO goes high, signaling the peripheral device that the output register is full. The peripheral device may then strobe in the new data from Port B with ORS. Port B stays in the high impedance mode until ORS is activated by the peripheral device. ORF line goes low and remains low until Port B has been written into by the HM-6100 microprocessor. ORF then goes high, initiating another output sequence.

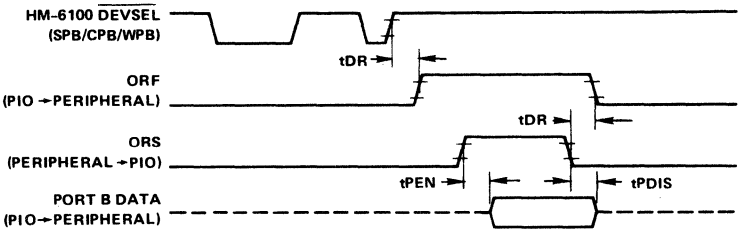


FIGURE 5 – Output Data Transfer (PIO to peripheral device)

The HM-6100 monitors the status of ORF (Output Register Full). If it is low (i.e., output register is empty), HM-6100 may load data into Port B output buffer with SPB/CPB/WPB instruction. ORF goes high a delay time after the rising edge of the 'write' $\overline{\text{DEVSEL}}$, signaling the peripheral device that output buffer has new data. During this time, Port B output buffers remain three-stated. The peripheral device may then enable and read out Port B output latches by activating ORS (Output Register Strobe) high. The falling edge of ORS (from high to low) signals the PIO that the peripheral device no longer needs the valid current information. Port B is three-stated and ORF then goes low, thereafter, to indicate another output sequence.

ORF should be set to 0 and IRE to 1 with a 'write' command in Mode 0X, to initiate the handshaking sequence.

The HM-6100 microprocessor should not write into Port B until ORF is low for an 'output' transfer and should not read Port B until IRE is low for an 'input' transfer. The peripheral device reads Port B if ORF is high and writes into Port B if IRE is high.

The PIO may be programmed to generate an $\overline{\text{INTREQ}}$ (Interrupt Request) to the microprocessor when ORF or IRE goes low by setting the respective Interrupt enable bits, OREN and IREN.

The HM-6100 may poll the status of ORF or IRE by executing the respective skip instructions SKPOR and SKPIR, by reading the status register or by reading "Port A".

In Mode 11 and 10, when handshaking control is not in effect, the execution of SKPOR and SKPIR Instructions depend on the state of the Port A lines PA11 and PA9, respectively. The Interrupt feature is available only in Mode 0X.

The mode of operation - 11, 10 or 0X, is selected by programming the Status Register (SR).

All ports are bi-directional. The execution of a 'write' instruction caused a port to be automatically programmed to be an 'output'. The output data may be changed by using the 'set', 'clear' or 'write' instructions. The output remains valid until the port bit lines are reset to be inputs.

Execution of a 'read' instruction causes a port to be automatically set as an 'input' port - i.e., it presents a very high impedance to the I/O lines. Data appearing on the I/O lines will be sampled into the port input latch at every LXMAR pulse and may be read by the HM-6100 microprocessor by the 'read' instruction.

In Mode 0X, Port B acts as a three-state bi-directional buffer which is controlled by an external peripheral device. ORF and IRE lines are outputs and ORS and IRS lines are inputs.

At power-on, all ports are defined to be input ports and the PIO is initialized to be in Mode 10. With 20 I/O lines partitioned into the 8/12 (i.e., Port A = 8 bits, Port B = 12 bits) format.

PIO Instructions

PIO CONTROL	MNEMONICS	DESCRIPTION
0000	SETPA	Set PA(i) to 1 if AC(i) is 1. AC is not cleared. Mode 11: PA(i) ← PA(i) + AC(i), $8 \leq i \leq 11$ Mode 10: PA(i) ← PA(i) + AC(i), $4 \leq i \leq 11$ Mode 0X: IREN ← IREN + AC(8) IRE ← IRE + AC(9) OREN ← OREN + AC(10) ORF ← ORF + AC(11)
0001	CLRPA	Clear Port A. Clear PA(i) to 0 if AC(i) is 1. AC is not cleared. Mode 11: PA(i) ← PA(i) ^ $\overline{AC(i)}$, $8 \leq 1 \leq 11$ Mode 10: PA(i) ← PA(i) ^ $\overline{AC(i)}$, $4 \leq i \leq 11$ Mode 0X: IREN ← IREN ^ $\overline{AC(8)}$ IRE ← IRE ^ $\overline{AC(9)}$ OREN ← IREN ^ $\overline{AC(10)}$ ORF ← ORF ^ $\overline{AC(11)}$
0010	WPA	Write Port A. Set PA(i) = AC(i). AC is not cleared. Mode 11: PA(i) ← AC(i), $8 \leq i \leq 11$ Mode 10: PA(i) ← AC(i), $4 \leq i \leq 11$ Mode 0X: IREN ← AC(8) IRE ← AC(9) OREN ← AC(10) ORF ← AC(11)
0011	RPA	Read Port A. 'OR' transfer PA to AC. Mode 11: AC(i) ← AC(i) + PA(i), $8 \leq i \leq 11$ AC(i) ← AC(i), $0 \leq i \leq 7$ Mode 10: AC(i) ← AC(i) + PA(i), $4 \leq i \leq 11$ AC(i) ← AC(i), $0 \leq i \leq 3$ Mode 0X: AC(8) ← AC(8) + IRS AC(9) ← AC(9) + IRE AC(10) ← AC(10) + ORS AC(11) ← AC(11) + ORF AC(i) ← AC(i), $0 \leq i \leq 7$
0100	SETPB	Set Port B. Set PB(i) to 1 if AC(i) is 1. AC is not cleared. PB(i) ← PB(i) + AC(i), $0 \leq i \leq 11$
0101	CLRPB	Clear Port B. Clear PB(i) to 0 if AC(i) is 1. AC is not cleared. PB(i) ← PB(i) ^ $\overline{AC(i)}$, $0 \leq i \leq 11$
0110	WPB	Write Port B. Set PB(i) = AC(i). AC is not cleared PB(i) ← AC(i), $0 \leq i \leq 11$
0111	RPB	Read Port B. 'OR' transfer PB to AC. AC(i) AC(i) + PB(i), $0 \leq i \leq 11$

PIO CONTROL	MNEMONICS	DESCRIPTION
1000	SETPC	Set Port C. Set PC(i) to 1 if AC(i) is 1. AC is not cleared. Mode 11 and 0X: PC(i) ← PC(i) + AC(i) $8 \leq i \leq 11$ Mode 10: No operation
1001	CLRPC	Clear Port C. Clear PC(i) to 0 if AC(i) is 1. AC is cleared. Mode 11 and 0X: PC(i) ← PC(i) ^ $\overline{AC(i)}$ $8 \leq i \leq 11$ Mode 10: No operation.
1010	WPC	Write Port C. Set PC(i)=AC(i). AC is not cleared Mode 11 and 0X: PC(i) ← AC(i) $8 \leq i \leq 11$ Mode 10: No operation.
1011	RPC	Read Port C. 'OR' transfer PC to AC. Mode 11 and 0X: AC(i) ← AC(i) + PC(i) $8 \leq i \leq 11$ Mode 10: No operation.
1100	SKPOR	Skip the next sequential instruction if PA(11))/ ORF is low. Mode 11 and 10: Skip if PA(11) is low. Mode 0X: Skip if ORF is low.
1101	SKPIR	Skip the next sequential instruction if PA(9)/ ORF is low. Mode 11 and 10: Skip if PA(9) is low. Mode 0X: Skip if IRE is low.
1110	WSR	Write status Register. AC is not cleared. M(8) ← AC(8) M(9) ← AC(9)
1111	RSR	Read Status Register. 'OR' transfer Status Register to AC. AC(i) ← AC(i), $0 \leq i \leq 7$ AC(8) ← AC(8) + M(8) AC(9) ← AC(9) + M(9) Mode 11 and 10: AC(10) ← AC(10) + PA(11) AC(11) ← AC(11) + PA(9) Mode 0X: AC(10) ← AC(10) + ORINT AC(11) ← AC(11) + IRINT

Symbol definition:
^ "and"
+ "or"
← "is replaced by"

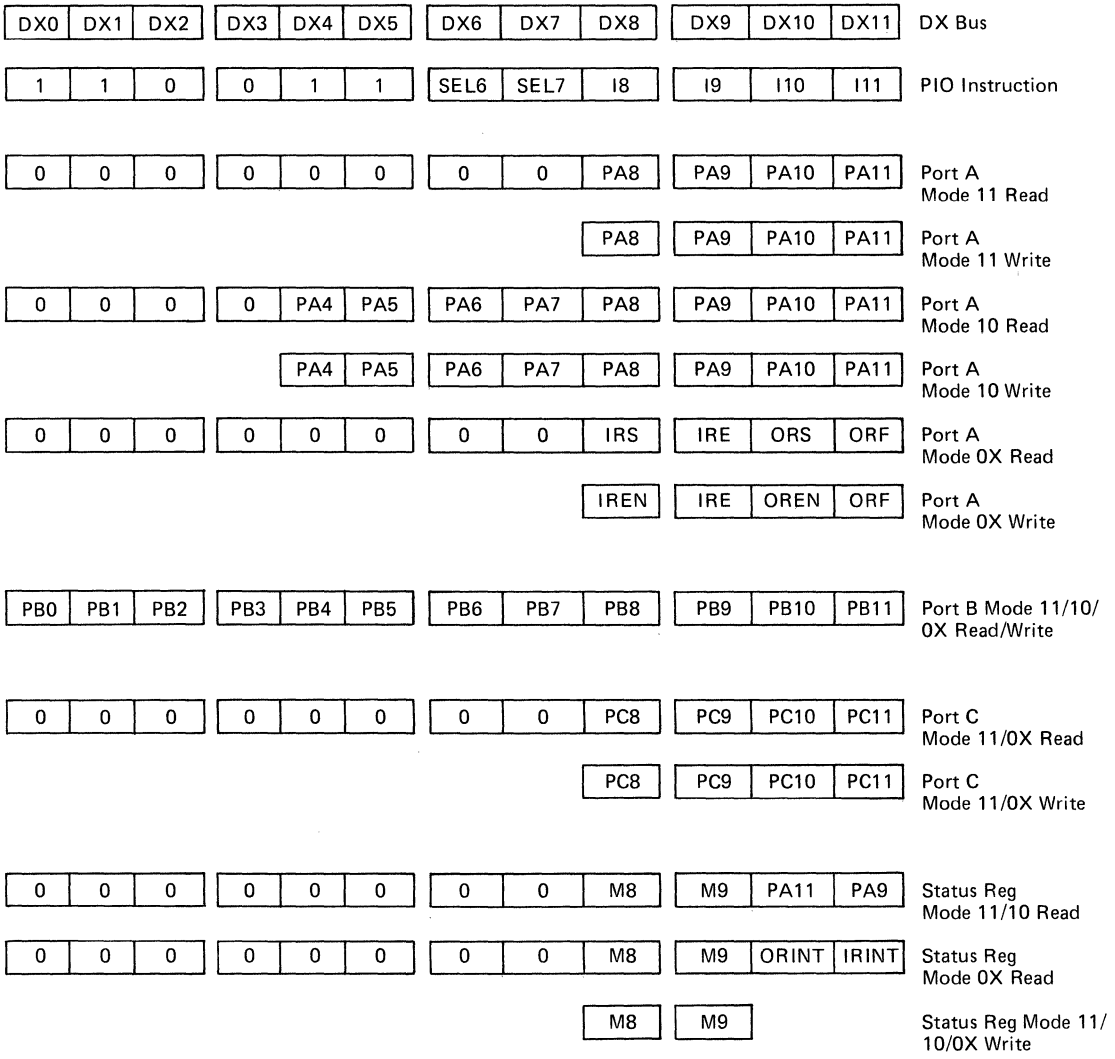


FIGURE 6 – HD-6103 PIO Register Bit Assignments

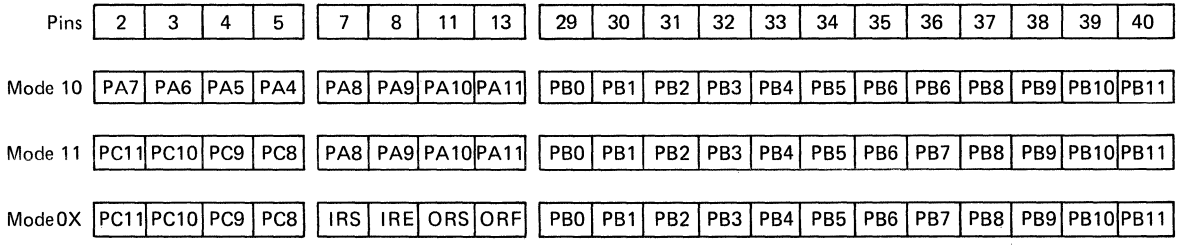


FIGURE 7 – HD-6103 PIO Port Pin Assignments

STATUS REGISTER

The Status Register (SR) has 2 mode bits, M8 and M9 which can be modified by the WSR (Write Status Register) instruction. These two bits define the mode of operation for the HD-6103 as shown in Figure 8.

M8	M9	MODE	PORT OPERATION
0	*	Mode 0X	PB(0)-(11), PC(8)-(11), IRS, IRE, ORS, ORF
1	0	Mode 10	PB(0)-(11), PA(4)-(11)
1	1	Mode 11	PB(0)-(11), PC(8)-(11), PA(8)-(11)

FIGURE 8 – Mode Bit Assignments

The Mode and Interrupt status bits, ORINT (Output Register empty Interrupt) and IRINT (Input Register empty Interrupt), may be read with the RSR (Read Status Register) instruction. The interrupt status bits are set to 0 if the corresponding flag is requesting an interrupt.

In Mode 11/10 the current value of PA11 and PA9 can be interrogated. In this mode, Port A can be either an input or an output. M(8) and M(9) are initialized to '11' at power-on.

MODE	COND-ITION	BIT ASSIGNMENTS			
		DX8	DX9	DX10	DX11
0X	READ	M8	M9	ORINT	IRINT
11/10	READ	M8	M9	PA11	PA9
11/10/0X	WRITE	M8	M9		

FIGURE 9 – Status Register Bit Assignments

SKIP OPERATION

The HM-6100 may poll the status of ORF or IRE in Mode 0X, by executing a skip instruction, SKPOR or SKPIR. The HD-6103 will assert the $\overline{SKP}/\overline{INT}$ line low if the corresponding status line (ORF or IRE) is low, causing the next sequential instruction to be skipped. During this cycle, ORF and IRE remain unchanged.

In Mode 11/10, SKPOR and SKPIR instruction executions depend on the state of PA11 and PA9, respectively. Port A may be an input or output port.

If ORF is reset to 0 be executing a CLRPA or WPA instruction to initiate the handshaking sequence, the next SKPOR instruction will cause the next sequential instruction to be skipped.

INTERRUPT OPERATION

The HD-6103 may be programmed to generate an interrupt request input ($\overline{INTREQ}$) when ORF or IRE goes low, by setting the corresponding interrupt enable bits, OREN or IREN, to 1. If the HM-6100 interrupt system has been previously enabled, the microprocessor will acknowledge the $\overline{INTREQ}$ input. If the HM-6100 microprocessor does not see the higher priority $\overline{INTREQ}$'s, inputs from other peripheral controllers such as HD-6102 Memory Extender/Direct Memory Access/Internal Timer Controller (MEDIC) or HD-6101 Parallel Interface Elements (PIE) in the system, the interrupt service routine should initiate a software poll of the PIO's in the system to identify the particular PIO that generated the $\overline{INTREQ}$. In Mode 0X, the interrupt request status of ORF and IRE may be identified by reading the Status Register. ORINT or IRINT will be set to 0 if ORF (being low) or IRE (being low) is generating an $\overline{INTREQ}$. Note that HD-6102 MEDIC and HD-6101 PIE provide an automatic priority vectoring.

The interrupt feature of HD-6103 is available only in Mode 0X. An ORF $\overline{INTREQ}$ may be removed by one of the following methods:

- Executing an SPB/CPB/WPB Instruction (ORF goes high if Port B is written into), or
- Setting ORF to 1 with SPA/WPA Instruction, or
- By resetting OREN to 0 with a CPA/WPA Instruction, or
- By changing to Mode 11/10.

An IRE $\overline{INTREQ}$ may be removed by:

- Executing a RPB Instruction (IRE goes higher after Port B is read), or
- Setting IRE to 1 with SPA/WPA Instruction, or
- Resetting IREN to 0 with a CPA/WPA Instruction, or
- Changing to Mode 11/10.

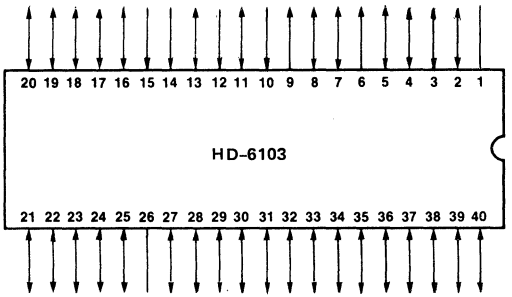
PIO may be software programmed to generate an $\overline{INTREQ}$ to the HM-6100 by resetting ORF or IRE to 0 with a CPA/WPA Instruction and by setting the corresponding enable bit, OREN or IREN, with a SPA/WPA Instruction in Mode 0X.

PIN DEFINITIONS

PIN NO.	SYMBOL	INPUT/ OUTPUT	DESCRIPTION
1	VCC		Positive Power Supply
2	PA7	I/O	Port A I/O Line (7)
	PC11	I/O	Port C I/O Line (11) in Mode 11/0X
3~5	PA6~PA4	I/O	Port A6~A4 (Mode 10).
	PC10~PC8	I/O	Port C10~C8 (Mode 11/0X).
6	$\overline{SKP}/\overline{INT}$	O	Time Multiplexed $\overline{SKP}$ and $\overline{INTREQ}$ lines to the HM-6100 Microprocessor – Active Low. This output is open drain.
7	PA8	I/O	Port A I/O Line in Mode 11/10 – Most Significant Bit of Port A in Mode 11.
	IRS	O	Input Register Strobe to clock data into Port B in Handshake Mode (Mode 0X). Port B Latches in the data on the falling edge of IRS (IRS↓).
8	PA9	I/O	Port A9 (Mode 11/10).

PIN NO.	SYMBOL	INPUT/ OUTPUT	DESCRIPTION
8 Cont'd	IRE	O	Input Register Empty output goes high when Port B input buffer has been read by the HM-6100 Microprocessor. It goes low when Port B input buffers are strobed in by IRS↓. (Mode 0X). PIO may be programmed to generate an $\overline{INTREQ}$ on IRE↓.
9	$\overline{C1}$	O	C1 output goes low upon completion of PIO Port data transfer to the HM-6100 Accumulator (AC). This output is an open-drain output to be wire-OR'd with $\overline{C1}$ Lines from other HM-6100 peripheral controllers
10	LXMAR	I	Address Latch enable signal from the HM-6100. PIO clocks in address and control information from the HM-6100 on the falling edge of LXMAR (LXMAR↓). All Port inputs are sampled at LXMAR↓.

2



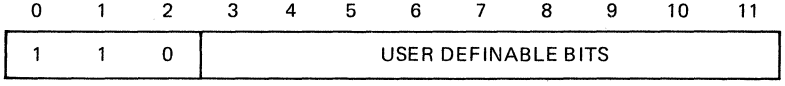
PIN NO.	SYMBOL	INPUT/ OUTPUT	DESCRIPTION
11	PA10	I/O	Port A10 (Mode 11/10).
	ORS	I	Output Register Strobe input to Enable Port B output buffers in Mode 0X. Port B is three-stated when ORS is low.
12	$\overline{DEVSEL}$	I	Input-Output Device Select control line from the HM-6100. It performs both the read and write function. The first negative transition after LXMAR↓, enables the DX output buffer of the selected PIO for a read operation. When $\overline{DEVSEL}$ returns high, the 'read' operation is terminated. The second negative-going pulse on $\overline{DEVSEL}$ serves as a 'write' pulse to the selected PIO and the HM-6100 AC data is written into the selected PIO register or port on the rising edge.
13	PA11	I/O	Port A11 (Mode 11/10)-Least Significant bit of Port A.

PIN NO.	SYMBOL	INPUT/ OUTPUT	DESCRIPTION
13 Cont'd	ORF	O	Output Register Full output goes high when the HM-6100 writes into Port B in a handshake mode. It goes low when the peripheral device reads Port B by enabling ORS high. The PIO may be programmed to generate an $\overline{INTREQ}$ on ORF↓ (Mode 0X).
14	SEL6	I	A Chip Select Input. PIO has 2 chip selects, SEL6 and SEL7, thereby enabling up to 4 PIO chips in a system.
15	SEL7	I	A Chip Select Input.
16~25	DX0~DX9	I/O	The HM-6100 System bus (Data and Address).
26	GND		Ground
27~28	DX10~DX11	I/O	HM-6100 System bus (Data and Address).
29~40	PB0~PB11	I/O	I/O Port Pin. PB0 is the most Significant bit, and PB11 is the Least Significant bit.

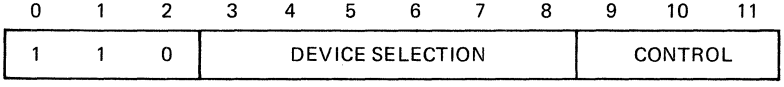
IOT Considerations

The HM-6100 communicates with peripherals via input/output transfers (IOT) instructions. The first three bits, 0-2 are always set to 6_8 (110) to specify an IOT instruction. The next 9 bits, 3-11, are user definable and can provide a minimal implementation when each bit controls one operation. When following PDP-8/E format, the next six bits, 3-8, contain the device selection code that determines the specific I/O device for which the IOT instruction is intended and, therefore, permits interfaces with up to 63 I/O devices. The last three bits, 9-11, contain the operation specification code that determines the specific operation to be performed. The HD-6102 MEDIC utilizes the PDP-8/E format. When using the HD-6101 PIE and the HD-6103 PIO, bits 3-7 perform the device selection function and bits 8-11 provide the operation specification code.

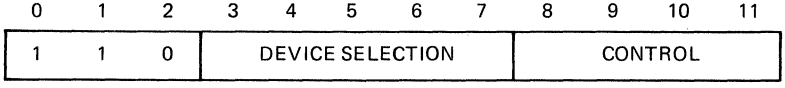
IOT INSTRUCTION FORMAT



Basic IOT Instruction: $6XXX_8$



PDP-8/E Format: $6NNX_8$



PIE and PIO Format

Care must be taken when building a system which uses all three peripheral interface devices from Harris to avoid conflicts with the device selection codes. Care also must be used when utilizing DEC compatible teletype and high speed reader interfaces in a system which includes PIE's and PIO's. The following table will assist in the assignment of device selection codes.

DEVICE SELECTION		DEVICE TYPE
PDP-8/E ①	PIE & PIO ②	
00	000 00	Internal IOT's
01	000 00	DEC High Speed Reader
02	000 01	DEC High Speed Punch
03	000 01	DEC Teletype Keyboard/Reader
04	000 10	DEC Teletype Printer/Punch
05	000 10	User Definable (DEC PDP-8/E Format Only)
06, 07	000 11	User Definable
10, 11	001 00	User Definable
12	001 01	User Definable (DEC PDP-8/E Format Only)
13	001 01	MEDIC Real Time Clock
14, 15	001 10	User Definable
16, 17	001 11	User Definable
20, 21	010 00	MEDIC Extended Memory Control and DMA
22, 23	010 01	MEDIC Extended Memory Control and DMA
24, 25	010 10	MEDIC Extended Memory Control and DMA
26, 27	010 11	MEDIC Extended Memory Control and DMA
30, 31	011 00	HD-6103 PIO No. One
32, 33	011 01	HD-6103 PIO No. Two
34, 35	011 10	HD-6103 PIO No. Three
36, 37	011 11	HD-6103 PIO No. Four
40, 41	100 00	User Definable
42, 43	100 01	
44, 45	100 10	
46, 47	100 11	
50, 51	101 00	
52, 53	101 01	
54, 55	101 10	
56, 57	101 11	
60, 61	110 00	
62, 63	110 01	
64, 65	110 10	
66, 67	110 11	(DEC Line Printer = 66)
70, 71	111 00	
72, 73	111 01	
74, 75	111 10	(DEC Floppy Disk Drive = 75)
76, 77	111 11	User Definable

NOTES:

① PDP-8/E device selection in octal.

② PIE & PIO device selection in binary.

CMOS Memory Family

μP

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CMOS ROM	
HM-6312 1024 x 12	3—4
CMOS RAMS	
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HM-6518 1024 x 1	3—20
HM-6533 1024 x 4	3—25
HM-6543 4096 x 1	3—31

3

Symbols and Abbreviations

This data sheet utilizes a new set of specification nomenclature. This new format is an IEEE and JEDEC supported standard for semiconductor memories. It is intended to clarify the symbols, abbreviations and definitions, and to make all memory data sheets consistent. We believe that, once acclimated, you will find this standardized format easy to read and use.

ELECTRICAL PARAMETER ABBREVIATIONS

All abbreviations use upper case letters with no subscripts. The initial symbol is one of these four characters:

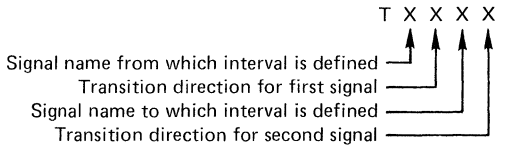
V (Voltage)
I (Current)
P (Power)
C (Capacitance)

The second letter specifies input (I) or output (O), and the third letter indicates the high (H), low (L) or off (Z) state of the pin during measurements. Examples:

VIL — Input Low Voltage
IOZ — Output Leakage Current

TIMING PARAMETER ABBREVIATIONS

All timing abbreviations use upper case characters with no subscripts. The initial character is always T and is followed by four descriptors. These characters specify two signal points arranged in a "from-to" sequence that define a timing interval. The two descriptors for each signal point specify the signal name and the signal transitions. Thus the format is:



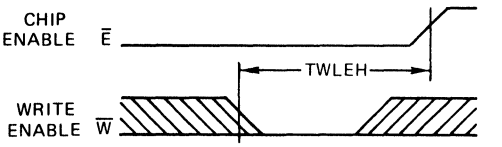
Signal Definitions:

A = Address
D = Data In
Q = Data Out
W = Write Enable
E = Chip Enable
S = Chip Select
G = Output Enable

Transition Definitions:

H = Transition to High
L = Transition to Low
V = Transition to Valid
X = Transition to Invalid or Don't Care
Z = Transition to Off (High Impedance)

EXAMPLE:



The example shows Write pulse setup time defined as TWLEH-Time from Write enable Low to chip Enable High.

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address set-up time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WAVEFORMS

WAVEFORM SYMBOL	INPUT	OUTPUT
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	—	HIGH IMPEDANCE

Battery Backup Applications

The Harris CMOS Memories are especially well suited for use in battery backup systems. Data retention supply voltage and supply current are guaranteed over the full temperature range.

When designing the backup system, the following suggestions should be considered:

1. As RAM VCC drops, the input logical one voltages should follow so as not to exceed VCC +0.3. It is suggested to use CMOS drivers, operating at CMOS VCC, such as the HD-6495, HD-6432, and HD-6433. Another approach is the use of open collector or open drain buffers pulled up to CMOS VCC.
2. $\overline{E}$ must be held high at CMOS VCC and $\overline{S}$, $\overline{G}$ high or G low. $\overline{W}$, $\overline{G}$, address, and data inputs should be held at either GND or CMOS VCC.
3. When exiting from the battery backup mode, VCC should ramp without ring or discontinuities.
4. The RAM can begin operation one TEHEL after VCC reaches the minimum operating voltage (4.5 or 4.75V).

A very simple battery backup system is shown in Figure 1. When system power is available, diode D1 is forward biased and supplies current to the CMOS devices. Upon loss of system power, diode D1 is reversed biased and only CMOS devices are consuming battery power. A disadvantage to this method is that CMOS VCC is one diode drop .7V, below TTL VCC. There is a possibility that a TTL output signal could rise higher than CMOS VCC and cause possible latch problems. This possibility can be reduced by incorporating a system similar to that shown in Figure 2. Other alternatives include using a germanuin diode yielding a VF $\approx$ .2V or adding diode D2 in the TTL supply and raising VCC to account for the drop. A PNP transistor is substituted for the diode in Figure 2. The saturation drop of the transistor, 0.2V, is less than the 0.7V drop of the diode giving more margin against latch-up. A power fail output signal is available to disable the $\overline{E}$ circuitry. Open collector TTL with pullups to CMOS VCC or LS type TTL should be used as memory drivers. This will insure that the CMOS inputs are not floating during the backup period. When system power is restored, operation continues as normal and the NI-CAD battery pack is trickle charged through RC.

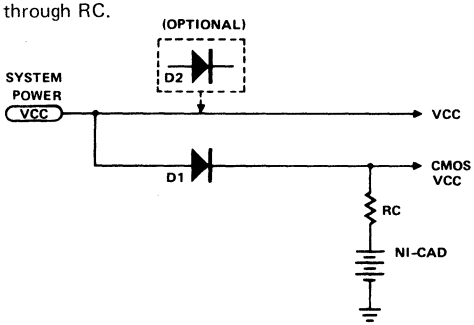


FIGURE 1

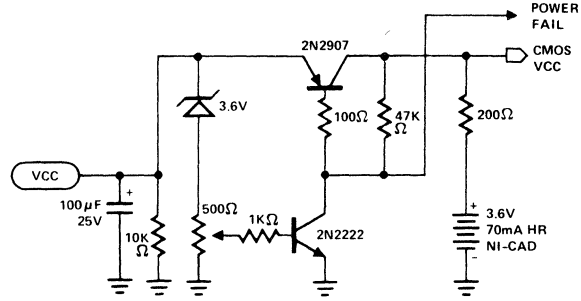
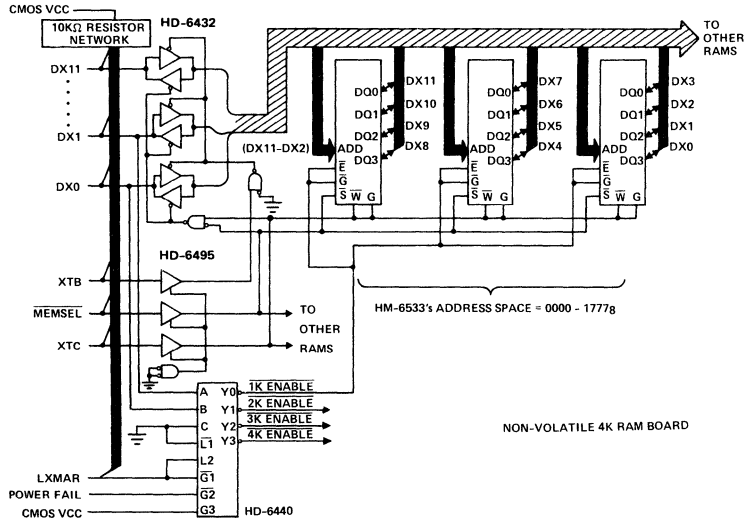


FIGURE 2



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HM-6312/6312A

CMOS ROM
1024 Word x 12 Bit

Features

- HM-6100 COMPATIBLE
- LOW POWER - TYPICAL < 5.0μW STANDBY
- 4 - 11 VOLT VCC OPERATION
- HIGH SPEED
- STATIC OPERATION

Description

The HM-6312 and HM-6312A are high speed, low power, silicon gate CMOS static ROM's, organized 1024 words by 12 bits. In all static states these units exhibit the microwatt power requirements typical of CMOS. The basic part operates at 4 - 7 volts with a typical 5 volt 25°C access time of 350ns. Higher operating voltages, 4 - 11 volts, are available with the A version. Signal polarities and functions are specified for interfacing with the HM-6100 Microprocessor.

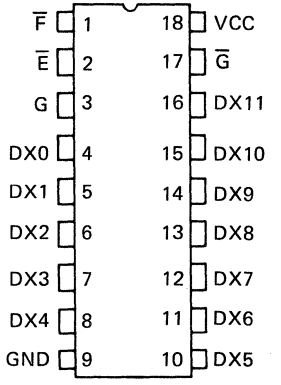
3

Operation

Addresses and data out are multiplexed on 12 lines, DX0 - DX11. Addresses are loading into an on chip register by falling edge of $\overline{E}$. Data out, corresponding to the latched address, is enabled when $\overline{E}$, $\overline{G}$ and G are true. The $\overline{F}$ output defines an area in the 4096 word addressing space dedicated to RAM. It can be programmed by DX0, DX1, DX2 and DX3. This output eliminates a four bit register and decoder for the high order address bits to select RAM.

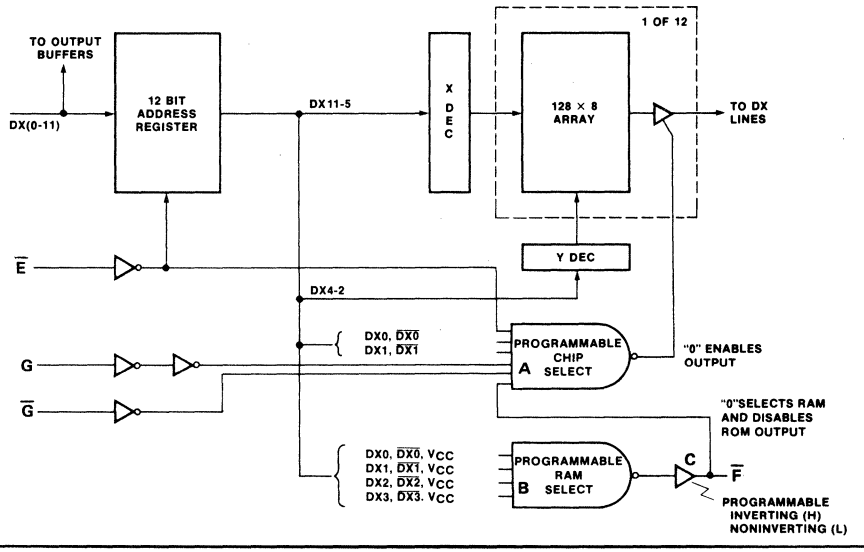
Pinout

TOP VIEW – DIP



DX - Address Input and Data Out
$\overline{E}$ - Chip Enable
G - Output Enable
$\overline{G}$ - Output Enable
$\overline{F}$ - RAM Field Select

Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+12.0V
Applied Input or Output Voltage	GND -0.3V to VCC + 0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial-9	-40°C to +85°C
Military-2	-55°C to +125°C

ELECTRICAL CHARACTERISTICS VCC = 10 ± 5%

D.C.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
VIH	Logical "1" Input Voltage	70% VCC			V	
VIL	Logical "0" Input Voltage			20% VCC	V	
IIL	Input Leakage	-1.0		+1.0	μA	$0V \leq VIN \leq VCC$
VOH	Logical "1" Output Voltage	VCC -0.1			V	IOUT = 0
VOL	Logical "0" Output Voltage			GND + 0.1	V	IOUT = 0
IO	Output Leakage	-1.0		1.0	μA	$0V \leq VO \leq VCC$
ICCSB	Standby Supply Current			800	μA	VIN = 0 or VCC
ICCOP	Operating Current ①		7	10	mA	f = 1MHz, IO = 0
CI	Input Capacitance ②		5.0	7.0	pF	VI = VCC or GND
CIO	I/O Capacitance ②		6.0	10.0	pF	

See Switching Waveforms page 3-8

A.C.

		INDUSTRIAL		MILITARY			
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS	TEST CONDITIONS ③
TELQV	Access Time From $\overline{E}$		200		220	ns	VCC = 10 ± 5%
TGHQV	Output Enable Time		160		175	ns	
TGLQZ	Output Disable Time		160		175	ns	
TEHEL	Strobe Pos. Pulse Width	125		140		ns	
TELEL	Cycle Time	325		360		ns	
TAVEL	Address Set-Up Time	30		35		ns	
TELAX	Address Hold Time	55		60		ns	
TELFV	Propagation to $\overline{F}$		100		110	ns	

NOTES: ① Operating Supply Current (ICCOP) is proportional to operating frequency, example typical ICCOP = 7mA/MHz.
② Capacitance sampled and guaranteed - not 100% tested.
③ A.C. test conditions: Inputs - TRise = TFall = 20ns; Outputs - 1TTL Load and 50pF.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8 .0V
Applied Input or Output Voltage	GND -0.3V to VCC + 0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial-9	-40°C to +85°C
Military-2	-55°C to +125°C

ELECTRICAL CHARACTERISTICS VCC = 5 ± 10%

D.C.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
VIH	Logical "1" Input Voltage	70% VCC			V	
VIL	Logical "0" Input Voltage			20% VCC	V	
IIL	Input Leakage	-1.0		+1.0	μA	0V ≤ VIN ≤ VCC
VOH	Logical "1" Output Voltage	VCC -0.1			V	IOUT = 0
VOL	Logical "0" Output Voltage			GND + 0.1	V	IOUT = 0
IO	Output Leakage	-1.0		1.0	μA	0V ≤ VO ≤ VCC
ICCSB	Standby Supply Current			100	μA	VI = 0 or VCC
ICCOP	Operating Current ①		3	5	mA	f = 1MHz, IO = 0
CI	Input Capacitance ②		5.0	7.0	pF	VI = VCC or GND
CIO	I/O Capacitance ②		6.0	10.0	pF	

See Switching Waveforms page 3-8

A.C.

		INDUSTRIAL		MILITARY			
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS	TEST CONDITIONS ③
TELQV	Access Time From $\overline{E}$		510		560	ns	VCC = 5 ± 10%
TGHQV	Output Enable Time		290		320	ns	
TGLQZ	Output Disable Time		290		320	ns	
TEHEL	Strobe Pos. Pulse Width	260		285		ns	
TELEL	Cycle Time	770		845		ns	
TAVEL	Address Set-Up Time	75		85		ns	
TELAX	Address Hold Time	120		135		ns	
TELFV	Propagation to $\overline{F}$		220		240	ns	

NOTES: ① Operating Supply Current (ICCOP) is proportional to operating frequency, example typical ICCOP = 3mA/MHz.
② Capacitance sampled and guaranteed - not 100% tested.
③ A.C. test conditions: Inputs - TRise = TFall = 20ns; Outputs -1TTL Load and 50pF.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8 .0V
Applied Input or Output Voltage	GND -0.3V to VCC + 0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

VCC = 5 ± 10%

D.C.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
VIH	Logical "1" Input Voltage	70% VCC			V	
VIL	Logical "0" Input Voltage			20% VCC	V	
IIL	Input Leakage	-10		+10	μA	0V ≤ VIN ≤ VCC
VOH	Logical "1" Output Voltage	VCC -.01			V	IOUT = 0
VOL	Logical "0" Output Voltage			GND + 0.1	V	IOUT = 0
IO	Output Leakage	-10		+10	μA	0V ≤ VO ≤ VCC
ICCSB	Standby Supply Current			500	μA	VI = 0 or VCC
ICCOP	Operating Current ①		3	5	mA	f = 1MHz, IO = 0
CI	Input Capacitance ②		5.0	7.0	pF	VI = VCC or GND
CIO	I/O Capacitance ②		6.0	10.0	pF	

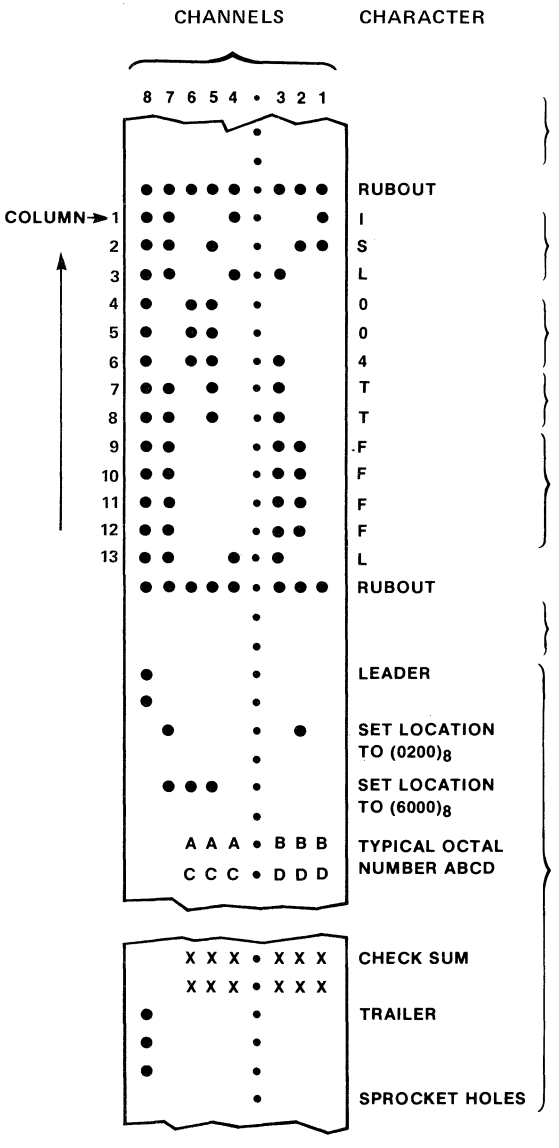
See Switching Waveforms page 3-8

A.C.

		INDUSTRIAL			
SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS ③
TELQV	Access Time From $\overline{E}$		640	ns	VCC = 5 ± 10%
TGHQV	Output Enable Time		390	ns	
TGLQZ	Output Disable Time		390	ns	
TEHEL	Strobe Pos. Pulse Width	300		ns	
TELEL	Cycle Time	940		ns	
TAVEL	Address Set-Up Time	75		ns	
TELAX	Address Hold Time	140		ns	
TELFV	Propagation to $\overline{F}$		250	ns	

NOTES: ① Operating Supply Current (ICCOP) is proportional to operating frequency, example typical ICCOP = 3mA/MHz.
② Capacitance sampled and guaranteed - not 100% tested.
③ A.C. test conditions: Inputs - TRise = TFall = 20ns; Outputs - 1TTL Load and 50pF.

HM-6312/6312A programming information is generated from the PAL III Symbolic Assembler as a "second pass" binary tape. A separate tape is required for each 1024 word ROM pattern, i.e. a separate symbolic should be generated for each 1024 word block of memory used, (0000-1777)8, (2000-3777)8, (4000-5777)8 and (6000-7777)8. A header is added to the front of each tape giving customer ID, chip select and $\overline{F}$ programming information. The header consists of 15 ASCII characters generated from a standard teletype. Channel 8 is always punched. The header begins with a rubout followed by 6 alphanumeric characters identifying the customer and the pattern number. Next are 2 characters designating true or false for inputs DX0 and DX1 to chips select gate A (see Functional Diagram), and 4 characters designating true, false, don't care for inputs DX0, DX1, DX2 and DX3 to the RAM select gate B (see Functional Diagram). Next is one character (H or L) designating $\overline{F}$ as active high or active low. The $\overline{F}$ function is inhibited when all $\overline{F}$ inputs are VCC or don't care (V) and $\overline{F}$ is active high. The header ends with a rubout.



PAL III Symbolic Assembler "second pass" output is of this form. Channel 8 only– punches indicate leader or trailer. An address is designated by a punch in channel 7. 12 bits of data are represented by two adjacent columns. DX0 - DX5 are represented by channels (6 - 1) in the first column. DX6 - 11 are represented by channels (6 - 1) in the second column.

The set location to $(0200)_8$ is an output of the PAL III Symbolic Assembler, not otherwise needed.

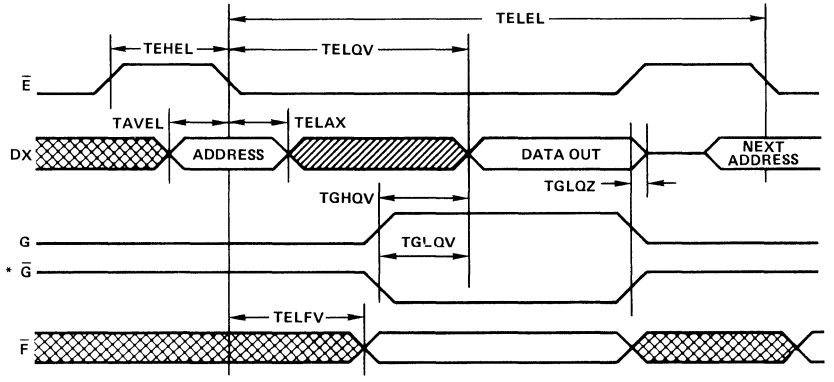
The example shown above has a customer ID and pattern ISL 004. Chip selects are programmed to recognize addresses $(6000\text{-}7777)_8$ or $(3072\text{-}4095)_{10}$. RAM select is active low for addresses $(0000\text{-}0377)_8$ or $(0000\text{-}0255)_{10}$. For programs using less than 1024 words the unused locations are automatically programmed to a logic one.

$\overline{F}$ PROGRAMMING

Defining the address block for which $\overline{F}$ is active is accomplished through programming the inputs to gate B. (See Functional Diagram). The sense of $\overline{F}$ is defined by programming gate C for inverting or noninverting. These conditions are specified in the header portion of the tape, columns 9 thru 13.

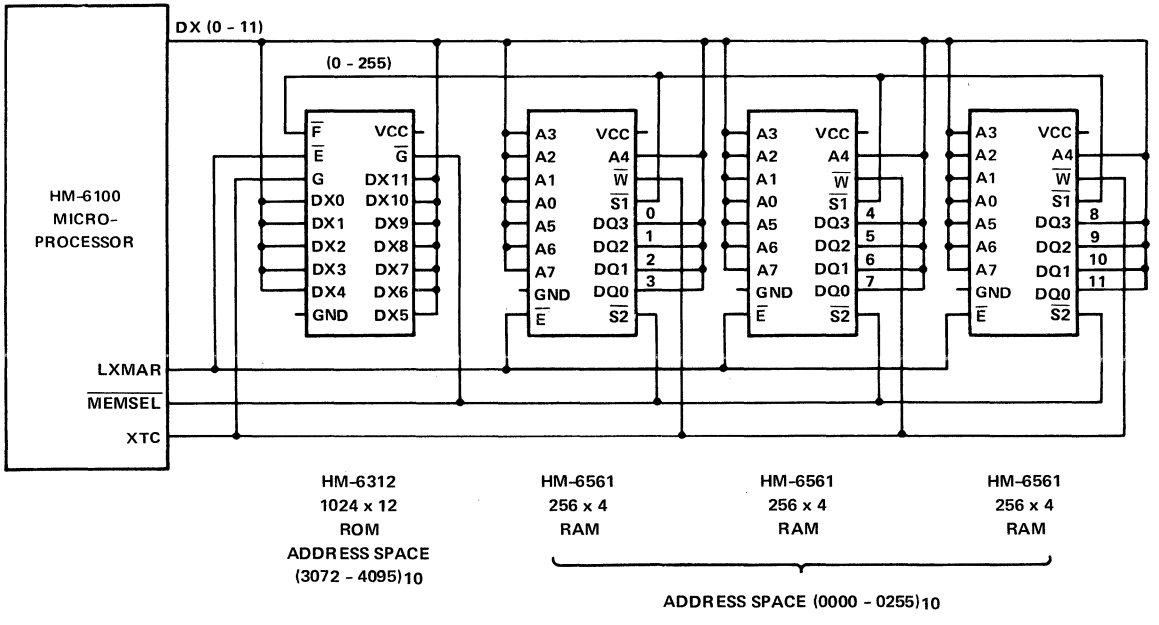
Particular care is required in specifying the sense of $\overline{F}$. Careful examination of the Functional Diagram reveals that $\overline{F}$ actually serves two functions, 1). $\overline{F}$ is anded with the inputs of gate A to enable the HM-6312 output buffers. 2). The output of $\overline{F}$ is used to select RAM or other external devices, this function is always a low true.

Switching Waveforms



* $\overline{G}$ has the same timing as G and is inverted.

A Typical Microprocessor System



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PRODUCTS DIVISION
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HM-6512

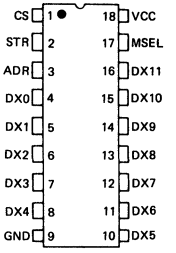
64 x 12 CMOS RAM

Features

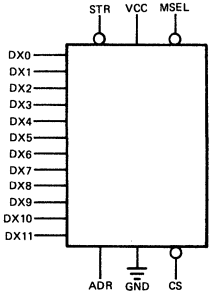
- HM-6100 COMPATIBLE
- LOW POWER STANDBY . . . . . 1mW MAX.
- LOW POWER OPERATION. . . . . .22mW/MHz MAX.
- DATA RETENTION . . . . . @ 2.0V MIN.
- TTL COMPATIBLE INPUT/OUTPUT
- TWO HM-6512's CAN BE USED WITH HM-6100 AND HM-6312 WITHOUT ADDITIONAL COMPONENTS
- THREE STATE OUTPUTS
- FAST ACCESS TIME . . . . . .250nsec MAX.
- MILITARY AND INDUSTRIAL TEMPERATURE RANGE
- 18 PIN PACKAGE FOR HIGH DENSITY
- ON CHIP ADDRESS REGISTER

Pinout

TOP VIEW



Logic Symbol



CS – Chip Select
STR – Chip Enable
MSEL – Enable and R/W Decode
ADR – Address Decode
DX – Address Input and Data I/O

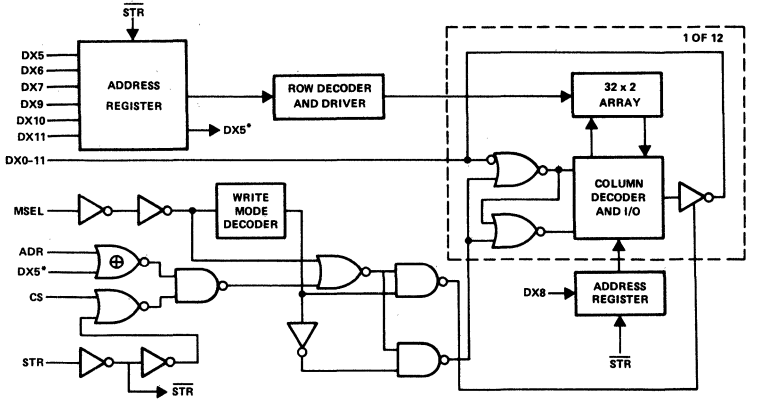
Description

The HM-6512 is a high speed, low power, silicon gate CMOS 768 bit static RAM organized 64 words by 12 bits. In all static states these units exhibit the microwatt power requirements typical of CMOS. Inputs and three state outputs are TTL compatible. The basic part operates at 4-7 volts with a typical 5 volt, 25°C access time of 150ns.

Signal polarities and functions are specified for direct interfacing with the HM-6100 microprocessor. The device is ideally suited for minimum system all CMOS applications where low power, minimum cost, or non-volatility is required.

3

Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	8.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HM-6512-9	-40°C to +85°C
Military HM-6512-2	-55°C to +125°C

ELECTRICAL CHARACTERISTICS VCC = 5.0V ±10%, TA = Industrial or Military

	SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	TEST CONDITIONS
D.C.	VIH	Logical "1" Input Voltage	VCC -2.0			V	
	VIL	Logical "0" Input Voltage			0.8	V	
	IIL	Input Leakage	-1.0		+1.0	µA	0V ≤ VIN ≤ VCC
	VOH	Logical "1" Output Voltage	2.4			V	IOH = -0.2mA
	VOL	Logical "0" Output Voltage			0.45	V	IOL = 2.0mA
	IO	Output Leakage	-1.0		+1.0	µA	0V ≤ VO ≤ VCC
	ICCSB	Supply Current Standby		1.0	100	µA	STR = VCC = 5.5V VIN = VCC or GND
	ICCDR	Supply Current Data Retention		0.1	50	µA	STR = VCC = 3.0V VIN = VCC or GND
	CI*	Input Capacitance		5.0	7.0	pF	
	CIO*	Input/Output Capacitance		6.0	10.0	pF	
A.C.	TAC	Access Time from STR			250	ns	CL = 50pF See Figures 1 & 2
	TEN	Output Enable Time			200	ns	
	TDIS	Output Disable Time			200	ns	
	TSTR	STR Pulse Width (Positive)	200			ns	
	$\overline{TSTR}$	STR Pulse Width (Negative)	250			ns	
	TC	Cycle Time	450			ns	
	TWP	Write Pulse Width (Negative)	130			ns	
	TAS	Address Setup Time	30			ns	
	TAH	Address Hold Time	50			ns	
	TDS	Data Setup Time	130			ns	
	TDH	Data Hold Time	0			ns	
	TPS	MSEL Pulse Separation	150			ns	
	TMS	MSEL Setup Time	50			ns	
	TMH	MSEL Hold Time	50			ns	

*Guaranteed but not 100% tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	7.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HM-6512C-9	-40°C to +85°C

ELECTRICAL CHARACTERISTICS VCC = 5.0V ±5%, TA = Industrial

	SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	TEST CONDITIONS
D.C.	VIH	Logical "1" Input Voltage	VCC -1.5			V	
	VIL	Logical "0" Input Voltage			0.8	V	
	IIL	Input Leakage	-5.0		+5.0	μA	0V ≤ VIN ≤ VCC
	VOH	Logical "1" Output Voltage	2.4			V	IOH = -0.2mA
	VOL	Logical "0" Output Voltage			0.45	V	IOL = 1.6mA
	IO	Output Leakage	-5.0		+5.0	μA	0V ≤ VO ≤ VCC
	ICCSB	Supply Current Standby			800	μA	STR = VCC = 5.25V VIN = VCC or GND
	CIN*	Input Capacitance		5.0	7.0	pF	
	CIO*	Input/Output Capacitance		6.0	10.0	pF	
A.C.	TAC	Access Time from STR			400	ns	CL = 50pF See Figures 1 & 2
	TEN	Output Enable Time			300	ns	
	TDIS	Output Disable Time			300	ns	
	TSTR	STR Pulse Width (Positive)	250			ns	
	$\overline{TSTR}$	STR Pulse Width (Negative)	400			ns	
	TC	Cycle Time	650			ns	
	TWP	Write Pulse Width (Negative)	200			ns	
	TAS	Address Setup Time	60			ns	
	TAH	Address Hold Time	100			ns	
	TDS	Data Setup Time	200			ns	
	TDH	Data Hold Time	0			ns	
	TPS	MSEL Pulse Separation	150			ns	
	TMS	MSEL Setup Time	100			ns	
	TMH	MSEL Hold Time	100			ns	

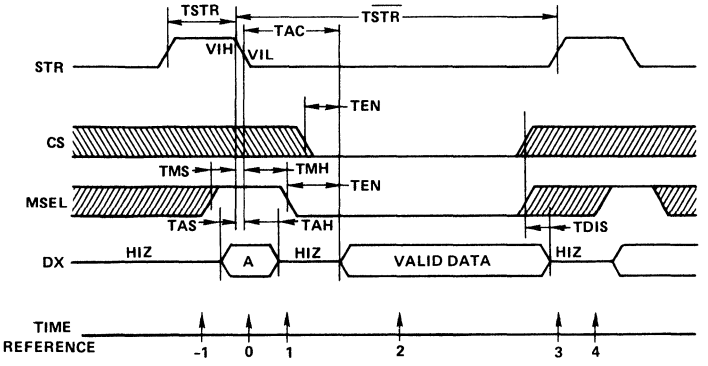
*Guaranteed but not 100% tested.

Functional Description

MSEL – The MSEL pin functions as a second chip enable and a write enable pin. If MSEL is low during the address strobe time the chip is placed in the write mode immediately. If MSEL is high during address strobe the chip performs a read operation during the first MSEL pulse and a write operation during the second MSEL pulse. In the event that a read only operation is desired the second MSEL pulse would be omitted.

ADR – The ADR pin provides the user with a method for using two HM-6512 chips in a HM-6100, HM-6312 ROM based system without any further decoding. The data on this pin is compared internally with address on DX5. If the two match, the chip will respond to MSEL and CS, otherwise the outputs remain high impedance and the stored data is unchanged. Using the HM-6312 with RSEL pin programmed for an active low for address $0\text{-}377_8$ and one or two HM-6512 RAMs provides for a 64 or 128 word scratch pad memory on page 0.

Read Cycle



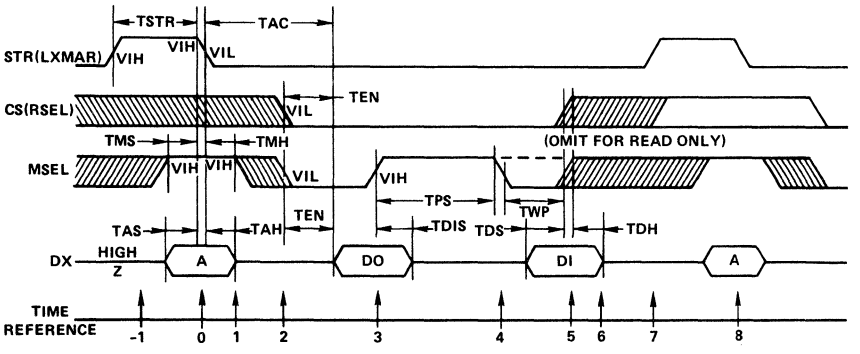
TRUTH TABLE

TIME REFERENCE	INPUTS STR	MSEL	DX	FUNCTION
-1	H	X	Z	Memory Disabled
0	↘	X	V*	Valid, Address Latched In
1	L	↘	X	End of Address Time
2	L	L	V	Valid, Data on Output
3	↗	H	Z	End of Read Cycle
4	H	X	Z	Begin New Cycle, Same as -1

*Address valid during this time.

FIGURE 1

Read Modify Write Cycle



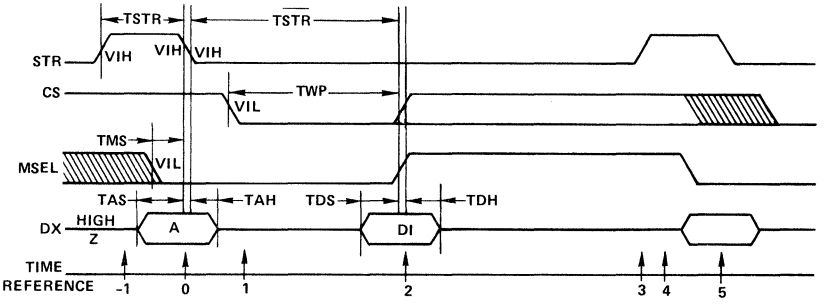
TRUTH TABLE

TIME REFERENCE	INPUTS STR	MSEL	DX	FUNCTION
-1	H	X	Z	Memory Disabled
0	↘	H	V*	Cycle Begins, Address Latched In
1	L	↘	Z	End of Address Time
2	L	L	X	Begin Read Time
3	L	↗	V	End of Read Time
4	L	↘	Z	Begin Write Time
5	L	↗	V	Data Written In
6	L	H	Z	End of Write Time
7	H	X	Z	End of Cycle, Memory Disabled
8	↘	H	V*	Begin New Cycle, New Address Latched In

*Address valid during this time.

FIGURE 2

Write Cycle



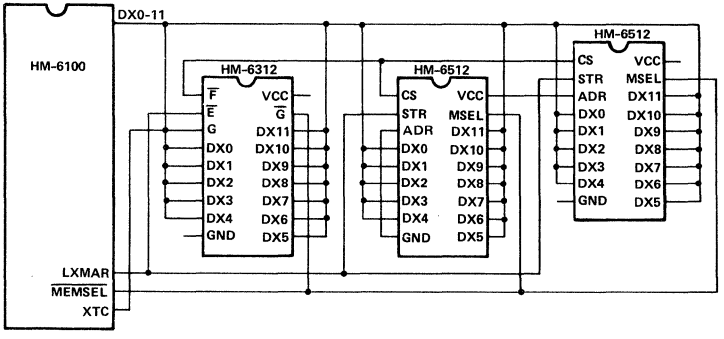
TRUTH TABLE

TIME REFERENCE	INPUTS STR	MSEL	DX	FUNCTION
-1	H	X	Z	Memory Disabled
0	↘	X	V*	Cycle Begins, Addresses are Latched
1	L	L	Z	Write Period Begins
2	L	↗	V	Data In is Written
3	↗	H	Z	Write Completed
4	H	X	Z	Prepare for Next Cycle
5	↘	X	V*	Cycle Ends, Next Cycle Begins

*Address valid during this time.

FIGURE 3

Typical Microprocessor System



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HM-6561

256 x 4 CMOS RAM

Features

- HM-6100 COMPATIBLE
- LOW STANDBY POWER . . . . . 55μW MAX
- LOW OPERATING POWER. . . . . 22mW/MHz MAX
- FAST ACCESS TIME . . . . . 220nsec MAX
- DATA RETENTION VOLTAGE . . . . . 2.0 VOLTS MIN
- TTL COMPATIBLE IN/OUT
- HIGH OUTPUT DRIVE – 2 TTL LOADS
- ON CHIP ADDRESS REGISTERS
- COMMON DATA IN/OUT
- THREE STATE OUTPUTS
- EASY MICROPROCESSOR INTERFACING
- MILITARY TEMPERATURE RANGE
- INDUSTRIAL TEMPERATURE RANGE

Description

The HM-6561 is a 256 by 4 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

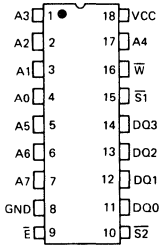
On chip latches are provided for address and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays. The data inputs and outputs are multiplexed internally for common I/O bus compatibility.

The HM-6561 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

The HM-6561 is pin for pin replaceable with the HM-6661, a 256 x 4 CMOS PROM. This allows a single memory board design with any organization of RAM and PROMs.

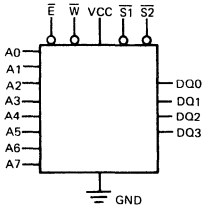
Pinout

TOP VIEW



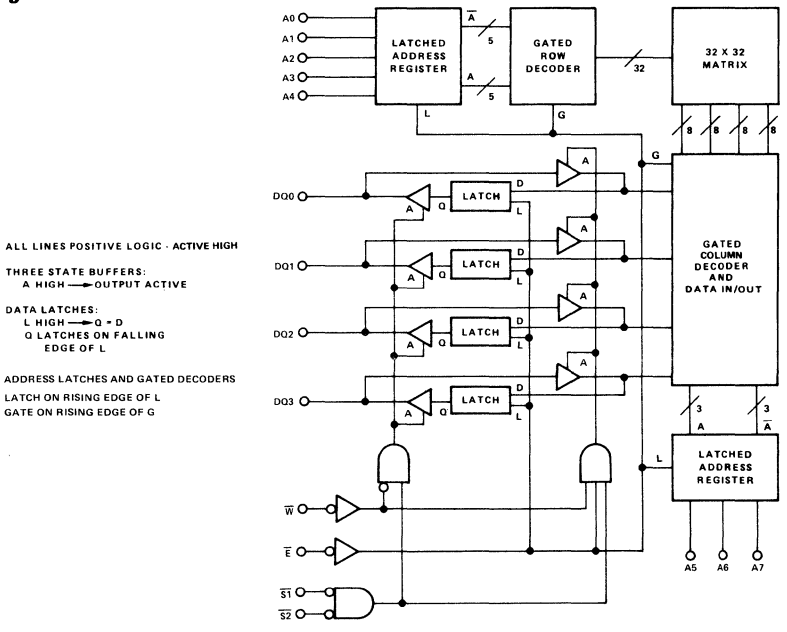
A – Address Input
$\overline{E}$ – Chip Enable
$\overline{S}$ – Chip Select
$\overline{W}$ – Write Enable
DQ – Data In/Out

Logic Symbol



3

Functional Diagram



ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage -VCC	+8.0V	Operating Supply Voltage -VCC	
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V	Military (-2)	4.5V to 5.5V
Storage Temperature	-65°C to +150°C	Industrial (-9)	4.5V to 5.5V
		Operating Temperature	
		Military (-2)	-55°C to +125°C
		Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

3 D.C.

SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE		TEMP. = 25°C ① VCC = 5.0V			UNITS	TEST CONDITIONS
		MIN	MAX	MIN	TYP	MAX		
ICCSB	Standby Supply Current		10 1(+25°C)		1.0	1	μA	IO = 0 VI = VCC or GND
ICCOP	Operating Supply Current ②		4		1.5	2.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
ICCDR	Data Retention Supply Current		10		0.1	1	μA	VCC = 3.0, IO = 0 VI = VCC or GND
VCCDR	Data Retention Supply Voltage	2.0		2.0	1.4		V	
II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VI ≤ VCC
IIOZ	Input/Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VO ≤ VCC
VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 3.2mA
VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -0.4mA
CI	Input Capacitance ③		6		4	6	pF	VI = VCC or GND f = 1MHz
CIO	Input/Output Capacitance ③		10		6	10	pF	VO= VCC or GND f = 1MHz

A.C.

TELQV	Chip Enable Access Time		300		160	240	ns	④
TAVQV	Address Access Time		300		150	240	ns	④
TSLQX	Chip Select Output Enable Time		150		60	120	ns	④
TWLQZ	Write Enable Output Disable Time		150		60	120	ns	④
TSHQZ	Chip Select Output Disable Time		150		60	120	ns	④
TELEH	Chip Enable Pulse Negative Width	300		240	160		ns	④
TEHEL	Chip Enable Pulse Positive Width	100		70	50		ns	④
TAVEL	Address Setup Time	0		0	-10		ns	④
TELAX	Address Hold Time	50		40	30		ns	④
TDVWH	Data Setup Time	150		120	100		ns	④
TWHDX	Data Hold Time	0		0	0		ns	④
TWLDV	Write Data Delay Time	150		120	60		ns	④
TWLSH	Chip Select Write Pulse Setup Time	300		240	160		ns	④
TWLEH	Chip Enable Write Pulse Setup Time	300		240	160		ns	④
TSLWH	Chip Select Write Pulse Hold Time	300		240	160		ns	④
TELWH	Chip Enable Write Pulse Hold Time	300		240	160		ns	④
TWLWH	Write Enable Pulse Width	300		240	160		ns	④
TWLSL	Early Output High Z Time	0		0	-10		ns	④
TSHWH	Late Output High Z Time	0		0	-10		ns	④
TELEL	Read or Write Cycle Time	400		310	210		ns	④

NOTES:
① All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
② Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
③ Capacitance sampled and guaranteed — not 100% tested.
④ AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — 1 TTL load and 50pF. All timing measurements at 1/2 VCC.

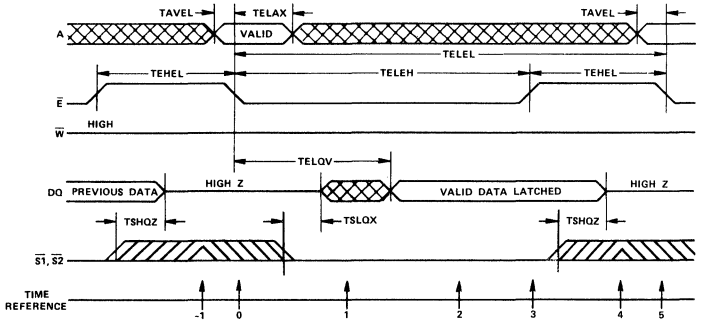
ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage -VCC	+8.0V	Operating Supply Voltage -VCC Commercial	4.5V to 5.5V
Applied Input or Output Voltage	GND -0.3V VCC +0.3V		
Storage Temperature	-65°C to +150°C	Operating Temperature Commercial	0°C to 75°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MIN	TEMP. = 25°C ① VCC = 5.0V TYP	TEMP. = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		100		10	100	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4		1.5	2.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		2.0			V	
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 1.6mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -0.2mA
	CI	Input Capacitance ③		6		4	6	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance ③		10		6	10	pF	VO= VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		350		200	300	ns	④
	TAVQV	Address Access Time		360		200	310	ns	④
	TSLQX	Chip Select Output Enable Time		180		80	160	ns	④
	TWLQZ	Write Enable Output Disable Time		180		80	160	ns	④
	TSHQZ	Chip Select Output Disable Time		180		80	160	ns	④
	TELEH	Chip Enable Pulse Negative Width	350		300	200		ns	④
	TEHEL	Chip Enable Pulse Positive Width	150		130	90		ns	④
	TAVEL	Address Setup Time	10		10	0		ns	④
	TELAX	Address Hold Time	70		50	40		ns	④
	TDVWH	Data Setup Time	170		140	120		ns	④
	TWHDX	Data Hold Time	0		0	0		ns	④
	TWLDV	Write Data Delay Time	200		170	60		ns	④
	TWLSH	Chip Select Write Pulse Setup Time	350		300	200		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	350		300	200		ns	④
	TSLWH	Chip Select Write Pulse Hold Time	350		300	200		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	350		300	200		ns	④
	TWLWH	Write Enable Pulse Width	350		300	200		ns	④
	TWLSL	Early Output High Z Time	0		0	-10		ns	④
	TSHWH	Late Output High Z Time	0		0	-10		ns	④
	TELEL	Read or Write Cycle Time	500		430	290		ns	④

NOTES:
① All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
② Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
③ Capacitance sampled and guaranteed — not 100% tested.
④ AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — 1 TTL load and 50pF. All timing measurements at 1/2 VCC.

Read Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS E	S1	W	A	OUTPUT DQ	FUNCTION
-1	H	H	X	X	Z	MEMORY DISABLED
0	↘	X	H	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	L	H	X	X	OUTPUT ENABLED
2	L	L	H	X	V	OUTPUT VALID
3	↗	L	H	X	V	OUTPUT LATCHED
4	H	H	X	X	Z	DEVICE DISABLED, PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	X	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

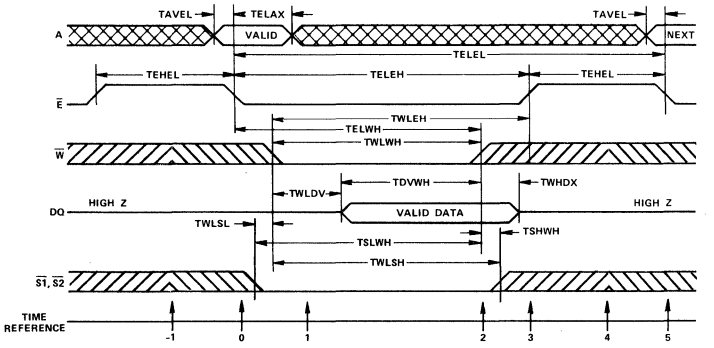
NOTES: 1) Device selected only if both $\overline{S1}$ and $\overline{S2}$ are low, and deselected if either $\overline{S1}$ or $\overline{S2}$ are high.

3

The HM-6561 Read Cycle is initiated on the falling edge of $\overline{E}$. This signal latches the input address word into on chip registers. Minimum address setup and hold times must be met. After the required hold time, the address lines may change state without affecting device operation. In order to read the output data $\overline{E}$, $\overline{S1}$ and $\overline{S2}$ must be low and $\overline{W}$ must be high. The output data will be valid at access time (TELQV).

The HM-6561 has output data latches that are controlled by $\overline{E}$. On the rising edge of $\overline{E}$ the present data is latched and remains latched until $\overline{E}$ falls. Either or both $\overline{S1}$ or $\overline{S2}$ may be used to force the output buffers into a high impedance state.

Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS E	S1	W	A	DQ	FUNCTION
-1	H	H	X	X	Z	MEMORY DISABLED
0	↘	X	X	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	L	L	X	Z	WRITE PERIOD BEGINS
2	L	L	↗	X	V	DATA IN IS WRITTEN
3	↗	X	H	X	Z	WRITE IS COMPLETED
4	H	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	X	X	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

NOTES: 1) Device selected only if both $\overline{S1}$ and $\overline{S2}$ are low, and deselected if either $\overline{S1}$ or $\overline{S2}$ are high.

In the Write Cycle the falling edge of $\overline{E}$ latches the addresses into on chip registers. The write portion of the cycle is defined as $\overline{E}$, $\overline{W}$, $\overline{S1}$, and $\overline{S2}$ being low simultaneously. $\overline{W}$ may go low anytime during the cycle provided that the write enable pulse setup times (TWLEH and TWLSH) are met. The write portion of the cycle is terminated by the first rising edge of $\overline{E}$, $\overline{W}$, $\overline{S1}$ or $\overline{S2}$. Data setup and hold times must be referenced to the terminating signal.

If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may remain low until all desired locations have been written. When this method is used, data setup and hold times must be referenced to the first rising edge of $\overline{E}$, $\overline{S1}$, or $\overline{S2}$. By positioning the write pulse at different times within the $\overline{E}$ low time (TELEH), various types of write cycles may be performed.

If the $\overline{E}$ low time (TELEH) is greater than the $\overline{W}$ pulse (TWLWH) plus an output enable time (TWHQX), a combination read-write cycle is executed.

Data may be modified an indefinite number of times during any single write cycle (TELEH).

Data multiplexing is done internal to the chip and is controlled by $\overline{W}$. When $\overline{W}$ goes low, the output buffers are forced to a high impedance state. After one output disable time (TWLQZ) input data may be applied to the bus. If it is desired that the output buffers not become active during the write cycle, $\overline{W}$ should go low with or before $\overline{S1}$, or $\overline{S2}$ (TWLSL). It should also change to a high state after $\overline{S1}$ or S2 goes high (TSHWH). Thus, TWLSL and TSHWH may be ignored unless the system design requires that the data outputs never become active during a write cycle. If the specified TWLSL time is met, the TWLDV time may be ignored. Data may then be applied to the bus whenever convenient since the output is guaranteed not to become active.

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HM-6518

1024 x 1 CMOS RAM

Features

- HM-6100 COMPATIBLE
- LOW STANDBY POWER . . . . . 55μW MAX
- LOW OPERATING POWER . . . . . 22mW/MHz MAX
- FAST ACCESS TIME . . . . . 180nsec MAX
- DATA RETENTION VOLTAGE . . . . . 2.0 VOLTS MIN
- TTL COMPATIBLE IN/OUT
- HIGH OUTPUT DRIVE - 2 TTL LOADS
- HIGH NOISE IMMUNITY
- ON CHIP ADDRESS REGISTER
- TWO CHIP SELECTS FOR EASY ARRAY EXPANSION
- THREE STATE OUTPUTS
- MILITARY TEMPERATURE RANGE
- INDUSTRIAL TEMPERATURE RANGE

Description

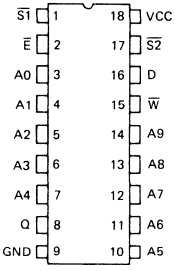
The HM-6518 is a 1024 by 1 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

On chip latches are provided for address and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

The HM-6518 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

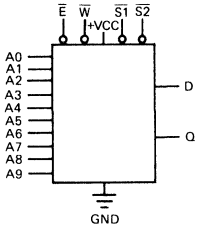
Pinout

TOP VIEW

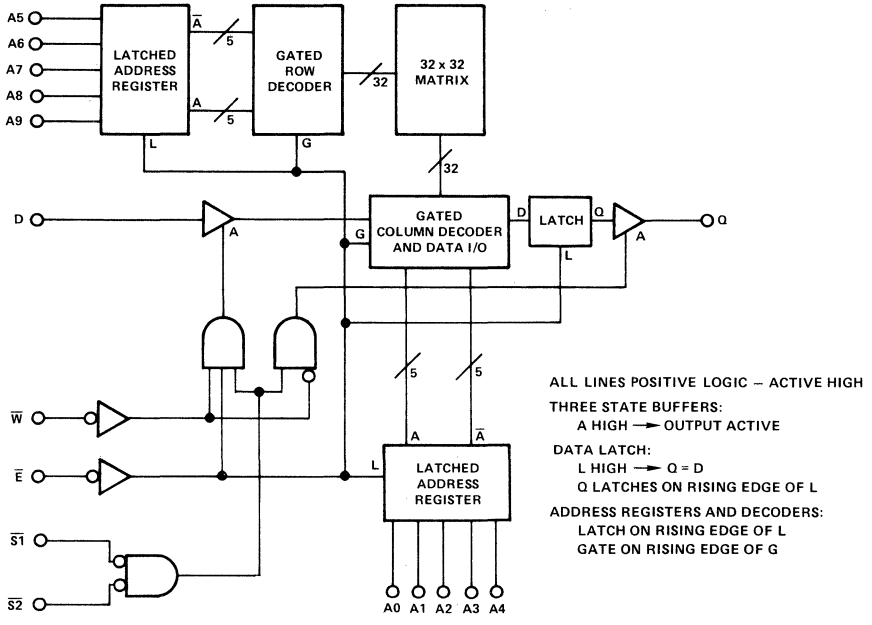


A - ADDRESS INPUT
E - CHIP ENABLE
S - CHIP SELECT
W - WRITE ENABLE
D - DATA INPUT
Q - DATA OUTPUT

Logic Symbol



Functional Diagram



ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage -VCC	+8.0V	Operating Supply Voltage -VCC	
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V	Military (-2)	4.5V to 5.5V
Storage Temperature	-65°C to +150°C	Industrial (-9)	4.5V to 5.5V
		Operating Temperature	
		Military (-2)	-55°C to +125°C
		Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MIN	TEMP. = 25°C ① VCC = 5.0V TYP	TEMP. = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		10 1(+25°C)		1.0	1	µA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4		1.5	2.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		10		0.1	1	µA	VCC = 3.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		2.0	1.4		V	
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	µA	GND ⩽ VI ⩽ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	µA	GND ⩽ VO ⩽ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 3.2mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -0.4mA
	CI	Input Capacitance ③		6		4	6	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10		6	10	pF	VO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		250		110	200	ns	④
	TAVQV	Address Access Time		250		100	200	ns	④
	TSLQX	Chip Select Output Enable Time		160		60	130	ns	④
	TWLQX	Write Enable Output Disable Time		160		60	130	ns	④
	TSHQX	Chip Select Output Disable Time		160		60	130	ns	④
	TELEH	Chip Enable Pulse Negative Width	250		200	110		ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		80	50		ns	④
	TAVEL	Address Setup Time	0		0	-10		ns	④
	TELAX	Address Hold Time	50		40	30		ns	④
	TDVWH	Data Setup Time	110		80	50		ns	④
	TWHDX	Data Hold Time	0		0	0		ns	④
	TWLSH	Chip Select Write Pulse Setup Time	130		100	60		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	130		100	60		ns	④
	TSLWH	Chip Select Write Pulse Hold Time	130		100	60		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	130		100	60		ns	④
	TWLWH	Write Enable Pulse Width	130		100	60		ns	④
	TELEL	Read or Write Cycle Time	350		280	160		ns	④

NOTES:
① All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed.
② Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
③ Capacitance sampled and guaranteed – not 100% tested.
④ AC Test Conditions: Inputs – TRISE = TFALL = 20nsec; Outputs – 1 TTL load and 50pF. All timing measurements at 1/2 VCC.

ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage -VCC	+8.0V	Operating Supply Voltage -VCC Commercial	4.5V to 5.5V
Input or Output Voltage Applied	GND -0.3V VCC +0.3V		
Storage Temperature	-65°C to +150°C	Operating Temperature Commercial	0°C to 75°C

ELECTRICAL CHARACTERISTICS

3 D.C.

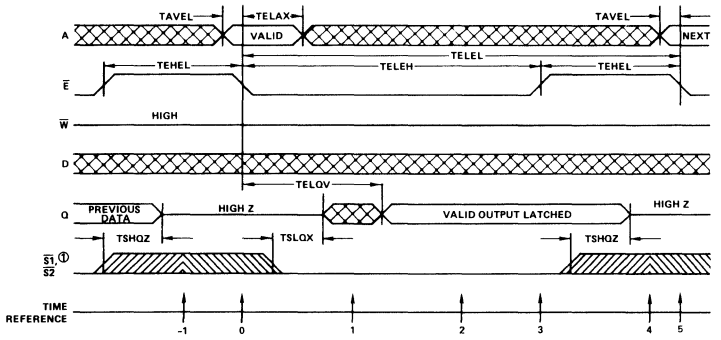
SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MIN	TEMP. = 25°C ① VCC = 5.0V TYP	TEMP. = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current		100		10	100	μA	IO = 0 VI = VCC or GND
ICCOP	Operating Supply Current ②		4		1.5	2.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
VCCDR	Data Retention Supply Voltage	2.0		2.0			V	
II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ⩽ VI ⩽ VCC
IOZ	Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ⩽ VO ⩽ VCC
VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 1.6mA
VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -0.2mA
CI	Input Capacitance ③		6		4	6	pF	VI = VCC or GND f = 1MHz
CO	Output Capacitance ③		10		6	10	pF	VO= VCC or GND f = 1MHz

A.C.

TELQV	Chip Enable Access Time		300		160	250	ns	④
TAVQV	Address Access Time		310		160	260	ns	④
TSLQX	Chip Select Output Enable Time		200		60	170	ns	④
TWLQX	Write Enable Output Disable Time		200		60	170	ns	④
TSHQX	Chip Select Output Disable Time		200		60	170	ns	④
TELEH	Chip Enable Pulse Negative Width	300		250	160		ns	④
TEHEL	Chip Enable Pulse Positive Width	150		130	90		ns	④
TAVEL	Address Setup Time	10		10	0		ns	④
TELAX	Address Hold Time	50		50	30		ns	④
TDVWH	Data Setup Time	130		100	80		ns	④
TWHDX	Data Hold Time	0		0	0		ns	④
TWLSH	Chip Select Write Pulse Setup Time	160		130	100		ns	④
TWLEH	Chip Enable Write Pulse Setup Time	160		130	100		ns	④
TSLWH	Chip Select Write Pulse Hold Time	160		130	100		ns	④
TELWH	Chip Enable Write Pulse Hold Time	160		130	100		ns	④
TWLWH	Write Enable Pulse Width	160		130	100		ns	④
TELEL	Read or Write Cycle Time	450		380	250		ns	④

NOTES:
① All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
② Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
③ Capacitance sampled and guaranteed — not 100% tested.
④ AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — 1 TTL load and 50pF. All timing measurements at 1/2 VCC.

Read Cycle



TRUTH TABLE

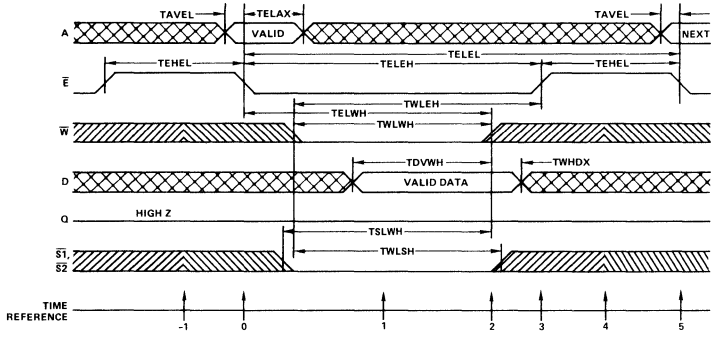
TIME REFERENCE	INPUTS Ē	S̄①	W̄	A	D	OUTPUT Q	FUNCTION
-1	H	H	X	X	X	Z	MEMORY DISABLED
0	↘	X	H	V	X	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	L	H	X	X	X	OUTPUT ENABLED
2	L	L	H	X	X	V	OUTPUT VALID
3	↗	L	H	X	X	V	OUTPUT LATCHED
4	H	H	X	X	X	Z	DEVICE DISABLED, PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	X	H	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

NOTES: ① Device selected only if both $\overline{S1}$ and $\overline{S2}$ are low, and deselected if either $\overline{S1}$ or $\overline{S2}$ are high.

In the HM-6518 read cycle the address information is latched into the on chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address setup and hold time requirements must be met. After the required hold time the addresses may change state without affecting device operation. In order for the output to be read $\overline{S1}$, $\overline{S2}$, and $\overline{E}$ must be low, $\overline{W}$ must be high. When $\overline{E}$ goes high the output data is latched into an on chip register. Taking either or both $\overline{S1}$ or $\overline{S2}$ high forces the output buffer to a high impedance state. The output data may be re-enabled at any time by taking $\overline{S1}$ and $\overline{S2}$ low. On the falling edge of $\overline{E}$ the data will be unlatched.

3

Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS Ē	W̄	S̄①	A	D	OUTPUT Q	FUNCTION
-1	H	X	X	X	X	Z	MEMORY DISABLED
0	↘	X	X	V	X	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	L	L	X	V	Z	WRITE MODE HAS BEGUN
2	L	↗	L	X	V	Z	DATA IS WRITTEN
3	↗	X	X	X	X	Z	WRITE COMPLETED
4	H	X	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	X	X	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

NOTES: ① Device selected only if both $\overline{S1}$ and $\overline{S2}$ are low, and deselected if either $\overline{S1}$ or $\overline{S2}$ are high.

The write cycle is initiated by the falling edge of $\overline{E}$ which latches the address information into the on chip registers. The write portion of the cycle is defined as $\overline{E}$, $\overline{W}$, $\overline{S1}$, and $\overline{S2}$ being low simultaneously. $\overline{W}$ may go low anytime during the cycle provided that the write enable pulse set-up time (TWLEH) is met. The write portion of the cycle is terminated by the first rising edge of either $\overline{E}$, $\overline{W}$, $\overline{S1}$ or $\overline{S2}$. Data setup and hold times must be referenced to the terminating signal.

If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may remain low until all desired locations have been written. When this method is used data setup and hold times must be referenced to the rising edge of $\overline{E}$. By positioning the $\overline{W}$ pulse at different times within the $\overline{E}$ low time (TELEH), various types of write cycles may be performed.

If the $\overline{E}$ low time (TELEH) is greater than the $\overline{W}$ pulse (TWLWH) plus an output enable time (TSLQX), a combination read-write cycle is executed. Data may be modified an indefinite number of times during any write cycle (TELEH).

The data input and data output pins may be tied together for use with a common I/O data bus structure. When using the RAM in this method allow a minimum of one output disable time (TWLQZ) after $\overline{W}$ goes low before applying input data to the bus. This will insure that the output buffers are not active.

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-6533

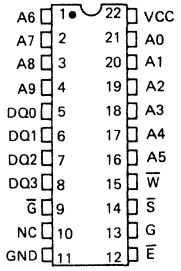
1024 x 4 CMOS RAM

Features

- HM-6100 COMPATIBLE
- LOW POWER STANDBY 1mW
- LOW POWER OPERATION. . . . . 35mW/MHz MAX
- DATA RETENTION @ 2.0 VOLTS.
- TTL COMPATIBLE INPUT/OUTPUT.
- "THREE STATE" OUTPUT.
- SEPARATE CHIP SELECT FOR EASE OF MEMORY EXPANSION.
- FULL MILITARY AND INDUSTRIAL TEMPERATURE RANGES.
- ON CHIP ADDRESS REGISTER.

Pinout

TOP VIEW



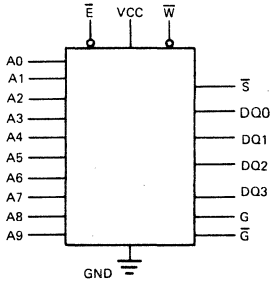
Description

The HM-6533 is a 1024 x 4 clocked static CMOS RAM designed specifically to interface with the HM-6100 Microprocessor. The device is manufactured utilizing self-aligned silicon gate technology. Extremely low power drain makes the HM-6533 an ideal candidate for battery powered systems.

On chip latching address registers and "Three State" I/O buffers enable the HM-6533 to operate in a multiplexed bus system with a minimum of support circuitry. Separate chip select and output disable pins allow for easy expansion. The output buffers can be disabled by the G, $\overline{G}$, or S pins (see Truth Table).

Wide supply voltage range and high noise immunity offer the system designer a large degree of flexability. Data retention is guaranteed down to 2.0V VCC making non-volitile memory systems simple to implement.

Logic Symbol



PIN NAMES

A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
DQ	Data In/Out
S	Chip Select
G	Output Enable

Functional Diagram

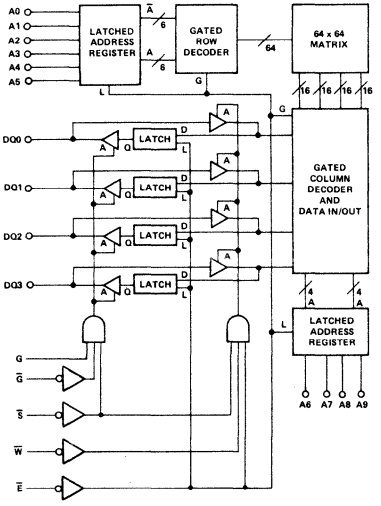
ALL LINES POSITIVE LOGIC ACTIVE HIGH

THREE STATE BUFFERS:
A HIGH → OUTPUT ACTIVE

DATA LATCHES:
L HIGH → Q = D
Q LATCHES ON FALLING EDGE OF L

ADDRESS LATCHES AND GATED DECODERS

LATCH ON RISING EDGE OF L
GATE ON RISING EDGE OF G



ABSOLUTE MAXIMUM RATINGS

Supply Voltage-VCC	+8.0V
Applied Input or Output Voltage	GND-0.3V VCC+0.3V
Storage Temperature Range	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage-VCC	4.5V to 5.5V
Operating Temperature Range	
Military (-2)	-55°C to +125°C
Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

			VCC & TEMP = OPERATING RANGE		TEMP = 25°C VCC = 5.0V (1)				
	SYMBOL	PARAMETER	MIN	MAX	MIN	TYP	MAX	UNIT	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		100		0.1	1.0	µA	IO = 0, VI = VCC or GND
	ICCOP	Operating Current ②		8		6	7	mA	F = 1MHz, IO = 0
	ICCDR	Data Retention Supply Current		50		1.0	5.0	µA	VCC = 3.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage		2.0		2.0	1.4	V	
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	µA	GND < VI < VCC
	IOZ	Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	µA	GND < VO < VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 2.0mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -2.0mA
	CI	Input Capacitance ③		6		4	6	pF	VI, VIO=VCC or GND F = 1MHz
	CIO	Output Capacitance ③		10		6	10	pF	VI, VIO=VCC or GND F = 1MHz
A.C.	TELQV	Chip Enable Access Time		400		300	350	ns	④
	TSLQX	Chip Select Output Enable Time		200		110	150	ns	④
	TSHQZ	Chip Select Output Disable Time		200		110	150	ns	④
	TGLQX	Output Enable Time		200		110	150	ns	④
	TGHQX	Output Disable Time		200		110	150	ns	④
	TELEL	Read or Write Cycle Time		600		475	550	ns	④
	TEHEL	Chip Enable Positive Pulse Width	200		200	175		ns	④
	TELEH	Chip Enable Negative Pulse Width	400		350	300		ns	④
	TAVEL	Address Setup Time	25		25	10		ns	④
	TELAX	Address Hold Time	75		75	60		ns	④
	TWLWH	Write Enable Pulse Width	220		130	110		ns	④
	TWLEH	Write Enable Pulse Setup Time	220		130	110		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	220		130	110		ns	④
	TWLSH	Chip Select Write Pulse Setup Time	220		130	110		ns	④
	TSLWH	Chip Select Write Pulse Hold Time	220		130	110		ns	④
	TDVWH	Data Setup Time	130		100	70		ns	④
	TWHDX	Data Hold Time	50		50	40		ns	④
	TDVSH	Data to Chip Select Setup Time	130		100	70		ns	④
	TSHDX	Data to Chip Select Hold Time	50		50	40		ns	④
	TSLSH	Chip Select Write Setup Time	220		130	100		ns	④

NOTES:
① All devices tested at worst case limits. Room temperature, 5V data provided for information - not guaranteed.
② Operating supply current (ICCOP) is proportional to operating frequency. Example: Typical ICCOP = 6mA/MHz.
③ Capacitance sampled and guaranteed - not 100% tested.
④ AC test conditions: Inputs – Trise = Tfall = 20ns.
Outputs – 1 TTL Load and 50pF.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage-VCC	+8.0V
Applied Input or Output Voltage	GND-0.3V VCC+0.3V
Storage Temperature Range	-65°C to +150°C

OPERATING RANGE

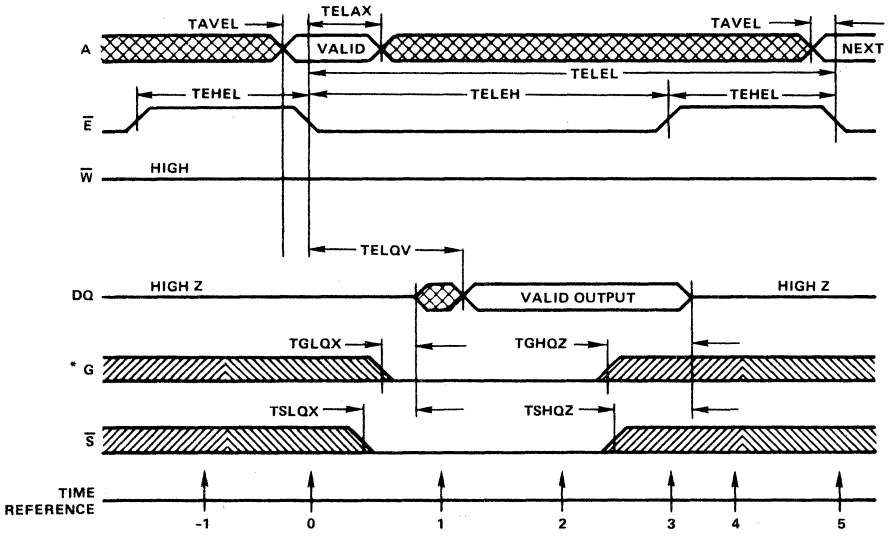
Operating Supply Voltage-VCC	4.5V to 5.5V
Operating Temperature Range	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

			VCC & TEMP = OPERATING RANGE		TEMP = 25°C VCC = 5.0V (1)				
	SYMBOL	PARAMETER	MIN	MAX	MIN	TYP	MAX	UNIT	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		1.0		0.1	1.0	mA	IO = 0, VI = VCC or GND
	ICCOP	Operating Current ②		8		6	+7	mA	F = 1MHz, IO = 0
	II	Input Leakage Current	-10	+10		±0.5	+7	µA	GND<VI<VCC
	IOZ	Output Leakage Current	-10	+10	-7	± 0.5	+7	µA	GND<VO< VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 1.6mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = --1.6mA
	CI	Input Capacitance ③		6		4	6	pF	VI, VIO=VCC or GND F = 1MHz
	CIO	Output Capacitance ③		10		6	10	pF	VI, VIO=VCC or GND F = 1MHz
A.C.	TELQV	Chip Enable Access Time		450		350	400	ns	④
	TSLQX	Chip Select Output Enable Time		300		130	180	ns	④
	TSHQZ	Chip Select Output Disable Time		300		130	180	ns	④
	TGLQX	Output Enable Time		250		130	180	ns	④
	TGHQX	Output Disable Time		250		130	180	ns	④
	TELEL	Read or Write Cycle Time	700		650	560		ns	④
	TEHEL	Chip Enable Positive Pulse Width	250		250	210		ns	④
	TELEH	Chip Enable Negative Pulse Width	450		400	350		ns	④
	TAVEL	Address Setup Time	50		50	30		ns	④
	TELAX	Address Hold Time	100		100	75		ns	④
	TWLWH	Write Enable Pulse Width	300		200	175		ns	④
	TWLEH	Write Enable Pulse Setup Time	300		200	175		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	300		200	175		ns	④
	TWLSH	Chip Select Write Pulse Setup Time	300		200	175		ns	④
	TSLWH	Chip Select Write Pulse Hold Time	300		200	175		ns	④
	TDVWH	Data Setup Time	200		150	120		ns	④
	TWHDX	Data Hold Time	75		50	25		ns	④
	TDVSH	Data to Chip Select Setup Time	220		150	120		ns	④
	TSHDX	Data to Chip Select Hold Time	75		50	25		ns	④
	TSLSH	Chip Select Write Setup Time	300		200	175		ns	④

NOTES: ① All devices tested at worst case limits. Room temperature, 5V data provided for information - not guaranteed.
② Operating supply current (ICCOP) is proportional to operating frequency. Example: Typical ICCOP = 6mA/MHz.
③ Capacitance sampled and guaranteed - not 100% tested.
④ AC test conditions: Inputs – Trise = Tfall = 20ns.
Outputs – 1 TTL Load and 50pF.

Read Cycle



*G has same timing as $\overline{G}$ except signal is inverted.

3

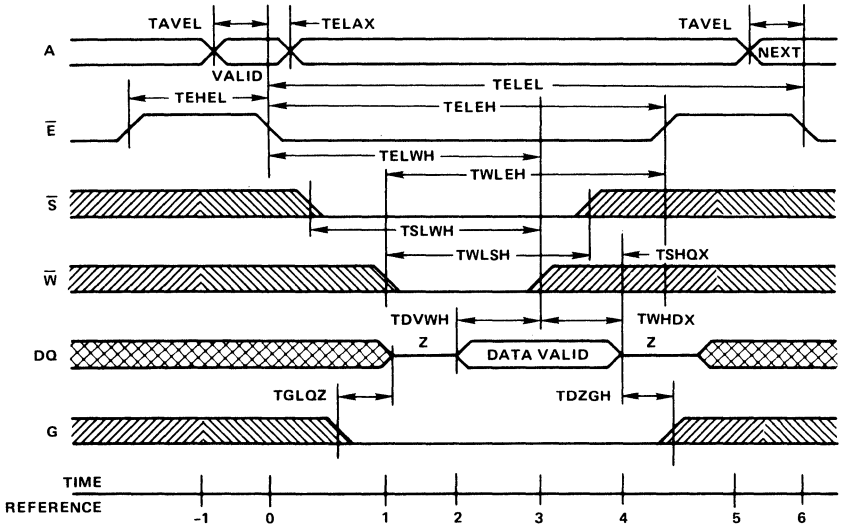
TIME REFERENCE	INPUTS $\overline{E}$	$\overline{S}$	$\overline{G}$	$\overline{W}$	A	OUTPUT DQ	FUNCTION
-1	H	H	H	X	X	Z	Memory Disabled
0	↘	H	H	H	V	Z	Cycle begins, Addresses are Latched
1	L	L	L	H	X	X	Output Enabled
2	L	L	L	H	X	V	Output Valid
3	↗	L	L	H	X	V	Output Latched
4	H	H	H	X	X	Z	Device Disabled, Prepare for next cycle (Same as -1)
5	↘	H	H	H	V	Z	Cycle ends, next cycle begins (Same as 0)

The read cycle is initiated by the falling edge of $\overline{E}$. This signal latches the input address word into on chip registers providing that minimum address setup and hold times are met. After the required hold time, the address inputs may change state without affecting device operation. For the output to be read, $\overline{G}$ and $\overline{E}$ and $\overline{S}$ must be low; $\overline{W}$ must be high. The output data will be valid at access time (TELQV) or at one output enable time (TSHQX or TGLQX), whichever is the latter occuring signal.

G and $\overline{G}$ are complementary signals which simplify the external logic required for decoding in expanded memory arrays. Either or both of these signals may be used to disable the outputs when tying several memories in an array. The HM-6533 has output data latches that are controlled by $\overline{E}$.

When $\overline{E}$ goes high the outputs are latched to contain the present data. The output buffers can be forced to a high impedance state by either $\overline{G}$ or $\overline{S}$ but the latches will only unlatch on the falling edge of $\overline{E}$.

Write Cycle



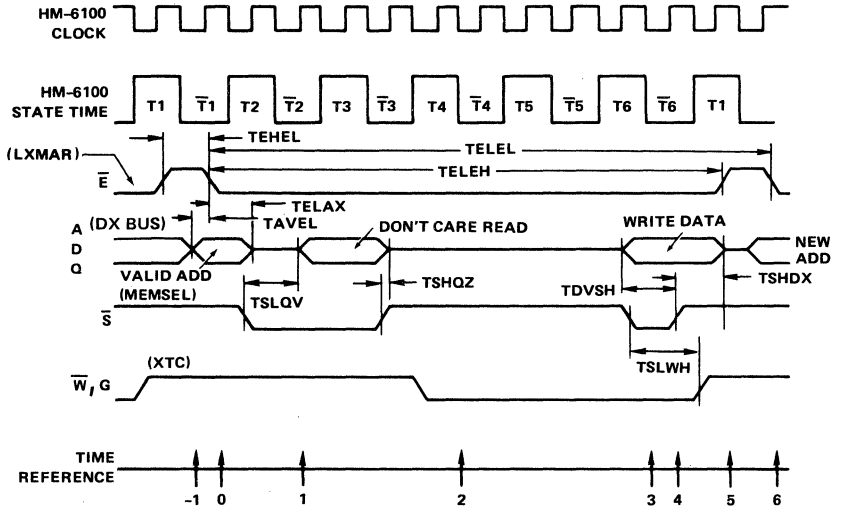
TIME REFERENCE	INPUTS Ē	S̄	G	W̄	A	I/O DQ	FUNCTION
-1	H	H	X	X	X	Z	Memory Disabled
0	↓	H	X	X	V	Z	Cycle begins, Addresses are Latched
1	L	L	L	↓	X	Z	Begin Write Operation, Output Disabled
2	L	L	L	L	X	V	Input Data Valid
3	L	L	L	↑	X	V	Data In is Written
4	L	H	L	H	X	Z	Input Data Gated Off
5	H	X	X	X	X	X	Memory Disabled (Same as -1)
6	↓	H	X	X	V	X	New Cycle begins (Same as 0)

As in the read mode, the write cycle is initiated by the falling edge of $\overline{E}$ which latches the addresses. The write portion of the cycle is defined as E and $\overline{W}$ being low simultaneously with $\overline{S}$ low. Since the inputs and outputs are tied together, G must be low. The write portion of the cycle is terminated on the first rising edge of $\overline{E}$, W, or $\overline{S}$. Data setup and hold times must be referenced to the terminating signal.

If a series of consecutive write cycles are to be performed, the W line may remain low until all desired locations have been written. When this method is used, data setup and hold times must be referenced to the rising edge of $\overline{E}$ or $\overline{S}$, whichever occurs first. By positioning the W pulse at different times within the $\overline{E}$ low time (TELEH) various types of write cycles may be performed.

If the $\overline{E}$ low time (TELEH) is greater than the W pulse (TWLWH) plus an output enable time (TSHQX or TGHQX) a combination read-write cycle is executed. Data may be modified an indefinite number of times during any write cycle (TELEH).

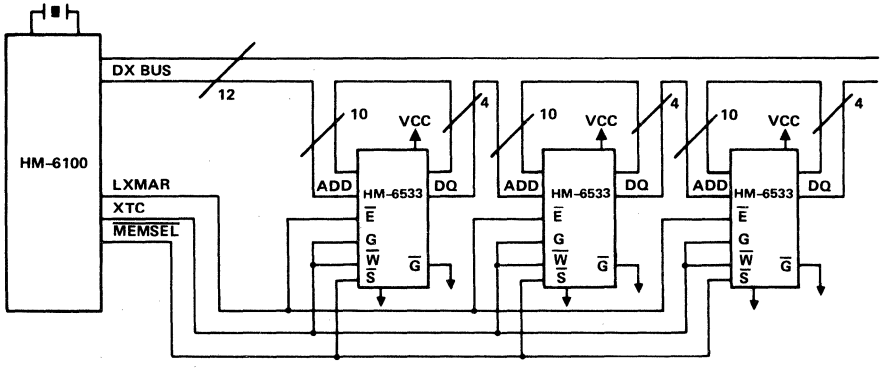
HM-6100 COMPATIBLE READ WRITE CYCLE



TRUTH TABLE

TIME REFERENCE	INPUTS						DATA I/O	FUNCTION
	$\overline{E}$	$\overline{S}$	$\overline{W}$	G	$\overline{G}$	A	DQ	
-1	H	H	H	H	L	X	Z	Memory Disabled
0	↓	H	H	H	L	V	Z	Cycle begins Addresses are Latched
1	L	L	H	H	L	X	V	Memory Output Enabled
2	L	H	H	H	L	X	Z	Memory Output Disabled
3	L	L	L	L	L	X	V	Valid Input Data present preparing to Write
4	L	↑	L	L	L	X	V	New Data Written In
5	↑	H	H	H	L	X	Z	Prepare for next cycle (Same as -1)
6	↓	H	H	H	L	V	Z	Cycle ends, next cycle begins (Same as 0)

HM-6100 1K x 12 MEMORY SYSTEM USING 3 HM-6533 RAMS



HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-6543

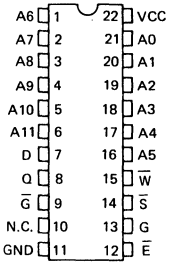
4096 x 1 CMOS RAM

Features

- HM-6100 COMPATIBLE
- LOW POWER STANDBY . . . . . 1mW MAX
- LOW POWER OPERATION. . . . . 35mW/MHz MAX
- DATA RETENTION . . . . . @ 2.0 VOLTS
- TTL COMPATIBLE INPUT/OUTPUT
- THREE STATE OUTPUT
- SEPARATE CHIP SELECT FOR EASE OF MEMORY EXPANSION
- FULL MILITARY AND INDUSTRIAL TEMPERATURE RANGE
- ON CHIP ADDRESS REGISTER

Pinout

TOP VIEW



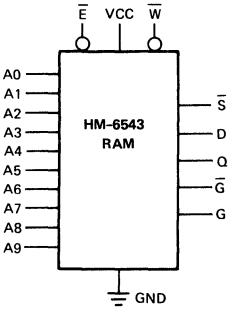
Description

The HM-6543 is a 4096 x 1 static CMOS RAM fabricated with self-aligned silicon gate technology. The device is designed to interface directly with the HM-6100, 12 bit Microprocessor.

On chip latches are provided for addresses and output data. The chip provides a three state output buffer for ease of use on a common bus.

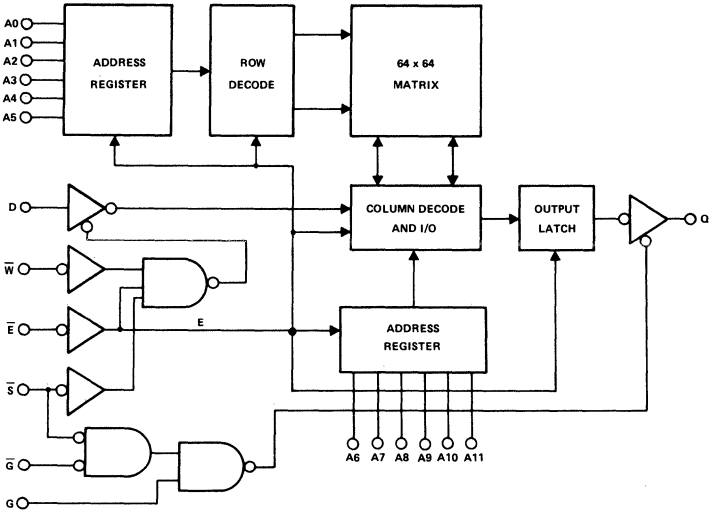
The HM-6543 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention, supply voltage and supply current are guaranteed over temperature.

Logic Symbol



A – Address Input
$\overline{E}$ – Chip Enable
$\overline{W}$ – Write Enable
$\overline{G}$ – Output Enable
$\overline{S}$ – Chip Select
D – Data Input
Q – Data Output
G – Output Enable

Functional Diagram



3

ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage -VCC	+8.0V	Operating Supply Voltage -VCC	4.5V to 5.5V
Applied Input or Output Voltage	GND -0.3V to VCC +0.3V	Operating Temperature	
		Military (-2)	-55°C to +125°C
Storage Temperature	-65°C to +150°C	Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MIN	TEMP. = 25°C ① VCC = 5.0V TYP	TEMP. = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
	ICCSB	Standby Supply Current		100		2	10	µA	IO = 0 VI = VCC or GND
	ICCOP	Operating Current ②		8		6	7	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		50		1	5	µA	VCC = 3.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage		2.0		2.0	1.4	V	
D.C.	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	µA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	µA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 2.0mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -2.0mA
	CI	Input Capacitance ③		6		4	6	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10		6	10	pF	VO= VCC or GND f = 1MHz
	TELQV	Chip Enable Access Time		400		300	350	ns	④
	TSLQX	Chip Select Output Enable Time		200		110	150	ns	④
	TSHQZ	Chip Select Output Disable Time		200		110	150	ns	④
	TGLQX	Output Enable Time		200		110	150	ns	④
	TGHQZ	Output Disable Time		200		110	150	ns	④
	TELEL	Read or Write Cycle Time		600		475	550	ns	④
	TEHEL	Chip Enable Positive Pulse Width	200		200	175		ns	④
	TELEH	Chip Enable Negative Pulse Width	400		350	300		ns	④
A.C.	TAVEL	Address Setup Time	25		25	10		ns	④
	TELAX	Address Hold Time	75		75	60		ns	④
	TWLWH	Write Enable Pulse Width	220		130	110		ns	④
	TWLEH	Write Enable Pulse Setup Time	220		130	110		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	220		130	110		ns	④
	TWLSH	Chip Select Write Pulse Setup Time	220		130	110		ns	④
	TSWLH	Chip Select Write Pulse Hold Time	220		130	110		ns	④
	TDVWH	Data Setup Time	130		100	70		ns	④
	TWHDX	Data Hold Time	50		50	40		ns	④
	TDVSH	Data to Chip Select Setup Time	130		100	70		ns	④
	TSHDX	Data to Chip Select Hold Time	50		50	40		ns	④
	TSLSH	Chip Select Write Setup Time	220		130	100		ns	④

NOTES:
① All devices tested at worst case limits. Room temp., 5 volt data provided — not guaranteed.
② Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example Typical ICCOP = 6mA/MHz.
③ Capacitance sampled and guaranteed — not 100% tested.
④ A.C. Test Conditions: Inputs — TRISE = TFALL = 20ns; Outputs — 1TTL load and 50pF.

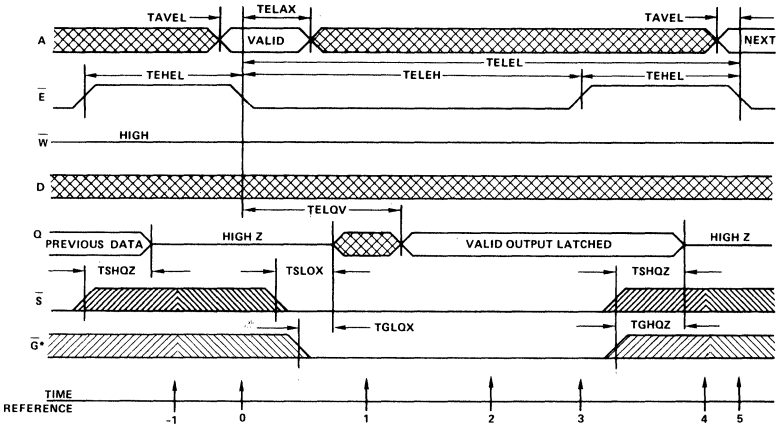
ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage -VCC	+8.0V	Operating Supply Voltage -VCC	4.5V to 5.5V
Applied Input or Output Voltage	GND -0.3V to VCC +0.3V	Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C		

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MIN	TEMP. = 25°C ① VCC = 5.0V TYP	TEMP. = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		1.0		0.1	1.0	mA	IO = 0 VI = VCC or GND
	ICCOP	Operating Current ②		8		6	7	mA	f = 1MHz, IO = 0 VI = VCC or GND
	II	Input Leakage Current	-10	+10		±0.5	+7	μA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-10	+10	-7	±0.5	+7	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +3.0	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 2.0mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -2.0mA
	CI	Input Capacitance ③		6		4	6	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10		6	10	pF	VO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		450		350	400	ns	④
	TSLQX	Chip Select Output Enable Time		300		130	180	ns	④
	TSHQZ	Chip Select Output Disable Time		300		130	180	ns	④
	TGLQX	Output Enable Time		250		130	180	ns	④
	TGHQZ	Output Disable Time		250		130	180	ns	④
	TELEL	Read or Write Cycle Time	700		560	650		ns	④
	TEHEL	Chip Enable Positive Pulse Width	250		210	250		ns	④
	TELEH	Chip Enable Negative Pulse Width	450		350	400		ns	④
	TAVEL	Address Setup Time	50		30	50		ns	④
	TELAX	Address Hold Time	100		75	100		ns	④
	TWLWH	Write Enable Pulse Width	300		175	200		ns	④
	TWLEH	Write Enable Pulse Setup Time	300		175	200		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	300		175	200		ns	④
	TWLSH	Chip Select Write Pulse Setup Time	300		175	200		ns	④
	TSLWH	Chip Select Write Pulse Hold Time	300		175	200		ns	④
	TDVWH	Data Setup Time	200		120	150		ns	④
	TWHDX	Data Hold Time	75		25	50		ns	④
	TDVSH	Data To Chip Select Setup Time	220		120	150		ns	④
	TSHDX	Data to Chip Select Hold Time	75		25	50		ns	④
	TSLSH	Chip Select Write Setup Time	300		175	200		ns	④

NOTES:
① All devices tested at worst case limits. Room temp., 5 volt data provided — not guaranteed.
② Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example Typical ICCOP = 6mA/MHz.
③ Capacitance sampled and guaranteed — not 100% tested.
④ A.C. Test Conditions: Inputs — TRISE = TFALL = 20ns; Outputs — 1TTL load and 50pF.

Read Cycle



*G Has same timing as $\overline{G}$ except signal is inverted

TRUTH TABLE

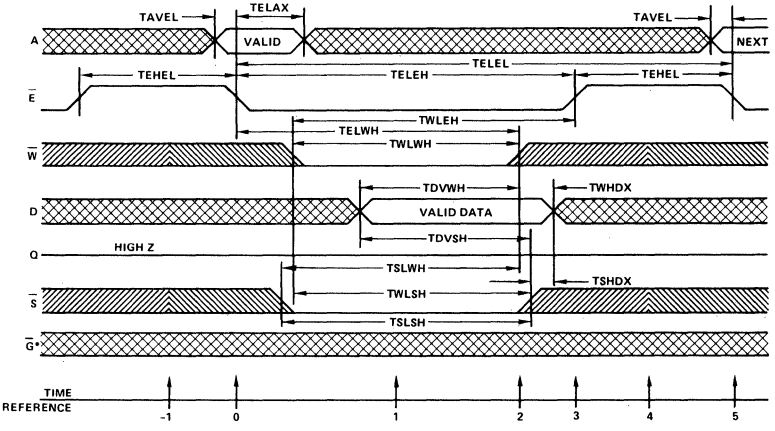
TIME REFERENCE	INPUTS $\overline{E}$	$\overline{S}$	$\overline{G}$*	$\overline{W}$	A	D	OUTPUT Q	FUNCTION
-1	H	H	H	X	X	X	Z	MEMORY DISABLED
0	↘	H	H	H	V	X	Z	CYCLE BEGINS, ADDRESS ARE LATCHED
1	L	L	L	H	X	X	X	OUTPUT ENABLED
2	L	L	L	H	X	X	V	OUTPUT VALID
3	↗	L	L	H	X	X	V	OUPUT LATCHED
4	H	H	H	X	X	X	Z	DEVICE DISABLED, PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	H	H	H	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The read cycle is initiated by the falling edge of $\overline{E}$. This signal latches the input address word into on chip registers providing that minimum address setup and hold times are met. After the required hold time, the address inputs may change state without affecting device operation. For the output to be read, $\overline{G}$ and $\overline{E}$ and $\overline{S}$ must be low; $\overline{W}$ must be high. The output data will be valid at access time (TELQV) or at one output enable time (TSLQX or TGLQX), whichever is the later occuring signal.

G and $\overline{G}$ are complementary signals which simplify the external logic required for decoding in expanded memory arrays. Either or both of these signals may be used to disable the outputs when or-tying several memories in an array. The HM-6543 has an output data latch that is controlled by $\overline{E}$.

When $\overline{E}$ goes high the outputs are latched to contain the present data. The output buffers can be forced to a high impedance state by either $\overline{G}$ or $\overline{S}$ but the latch will only unlatch on the falling edge of $\overline{E}$.

Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS						OUTPUT	FUNCTION
	$\overline{E}$	$\overline{S}$	$\overline{G}$	$\overline{W}$	A	D	Q	
-1	H	H	X	X	X	X	Z	MEMORY DISABLED
0	↘	X	X	X	V	X	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	L	X	↘	X	X	Z	WRITE PERIOD BEGINS
2	L	L	X	↗	X	V	Z	DATA IN IS WRITTEN
3	↗	X	X	H	X	X	Z	WRITE IS COMPLETED
4	H	H	X	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	X	X	X	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

As in the read mode, the write cycle is initiated by the falling edge of $\overline{E}$ which latches the addresses. The write portion of the cycle is defined as $\overline{E}$ and $\overline{W}$ being low simultaneously with $\overline{S}$ low.

The write portion of the cycle is terminated on the first rising edge of $\overline{E}$, $\overline{W}$, or $\overline{S}$. Data setup and hold times must be referenced to the terminating signal.

If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may remain low until all desired locations have been written. When this method is used, data setup and hold times must be referenced to the rising edge of $\overline{E}$ or $\overline{S}$, whichever occurs first. By positioning the $\overline{W}$ pulse at different times within the $\overline{E}$ low time (TELEH) various types of write cycles may be performed.

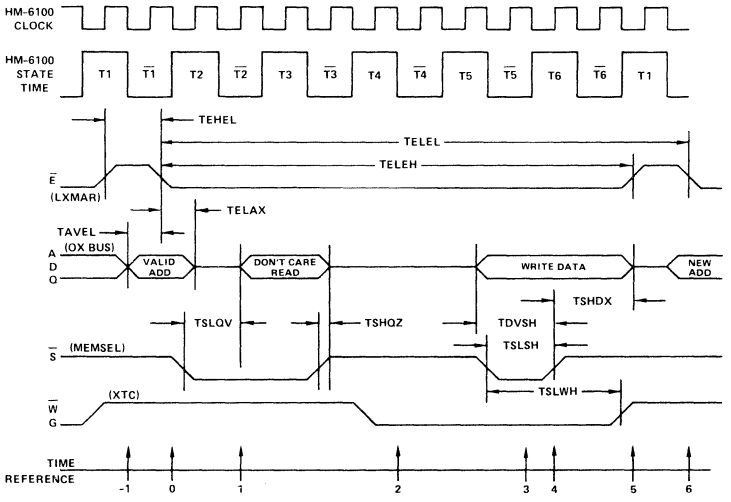
If the $\overline{E}$ low time (TELEH) is greater than the $\overline{W}$ pulse (TWLWH) plus an output enable time (TSLQX or TGLQX) a combination read-write cycle is executed. Data may be modified an indefinite number of times during any write cycle (TELEH).

COMMON I/O OPERATION

The HM-6543 is readily adaptable for use in a common I/O bus oriented system. In this mode of operation the G or $\overline{G}$ pins are used to disable the output before the input data is presented on the bus. When the chip is deselected ($\overline{S}$ high) the output is forced to the high impedance state thereby leaving the bus free to be driven from another source.

3

HM-6100 Compatible Read Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS							OUTPUT	FUNCTION
	$\overline{E}$	$\overline{S}$	$\overline{W}$	G	$\overline{G}$	A	D	Q	
-1	H	H	H	H	L	X	X	Z	MEMORY DISABLED
0	↘	H	H	H	L	V	X	Z	CYCLE BEGINS, ADDRESSES LATCHED
1	L	L	H	H	L	X	X	X	MEMORY OUTPUT ENABLED
2	L	H	H	H	L	X	X	Z	MEMORY OUTPUT DISABLED
3	L	L	L	L	L	X	V	Z	VALID INPUT DATA PRESENT PREPARING TO WRITE
4	L	↗	L	L	L	X	V	Z	NEW DATA WRITTEN IN
5	↗	H	H	H	L	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
6	↘	H	H	H	L	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

CMOS Interface Family

μP

CMOS Bus Driver Family Pinouts 4—2

Serial Interface

HD-4702/6405 Programmable Bit Rate Generator 4—4

HD-6402 Universal Asynchronous Receiver/Transmitter (UART) 4—10

HD-6408 Asynchronous Serial Manchester Adapter (ASMA) 4—15

CMOS Bus Drivers

HD-6431 Hex Latched Bus Driver 4—20

HD-6432 Hex Bi-Directional Bus Driver 4—24

HD-6433 Quad Bus Separator/ Driver 4—28

HD-6434 Octal Resettable Latched Bus Driver 4—32

HD-6435 Hex Resettable Latched Bus Driver 4—35

HD-6436 Octal Bus Buffer/ Driver 4—38

HD-6440 One-of-Eight Latched Decoder/Driver 4—41

HD-6495 Hex Bus Buffer/Driver 4—45

4

CMOS Bus Driver Family

HD-6431 CMOS HEX LATCHING BUS DRIVER

FEATURES

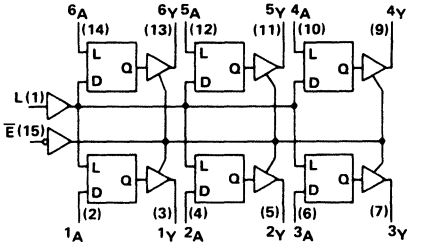
- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY 300pF
- SOURCE CURRENT 4mA
- SINK CURRENT 6mA
- PROPAGATION DELAY: 65nsec @ 5V

TRUTH TABLE

CONTROL INPUTS		DATA PORT STATUS	
$\overline{E}$	L	A	Y
H	L	X	HI-Z*
H	H	X	HI-Z
L	↓	X	*
L	H	L	L
L	H	H	H

* Data is latched to the value of the last input
X = Don't Care
HI-Z = High Impedance
↓ = Transition from High to Low Level

FUNCTIONAL DIAGRAM



HD-6432 CMOS HEX BI-DIRECTIONAL BUS DRIVER

FEATURES

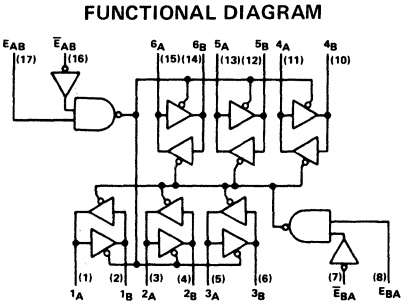
- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY 300pF
- SOURCE CURRENT 4mA
- SINK CURRENT 6mA
- PROPAGATION DELAY: 45nsec @ 5V

TRUTH TABLE

CONTROL INPUTS				DATA PORT STATUS	
E_{AB}	$\overline{E}_{AB}$	E_{BA}	$\overline{E}_{BA}$	A	B
L	X	H	L	O	I
X	H	H	L	O	I
H	L	X	H	I	O
H	L	L	X	I	O
L	X	L	X	ISOLATED	
X	H	X	H	ISOLATED	
L	X	X	H	ISOLATED	
X	H	L	X	ISOLATED	
H	L	H	L	NOT ALLOWED	

I = Input, O = Output, X = Don't Care

FUNCTIONAL DIAGRAM



HD-6433 CMOS QUAD BUS SEPARATOR/DRIVER

FEATURES

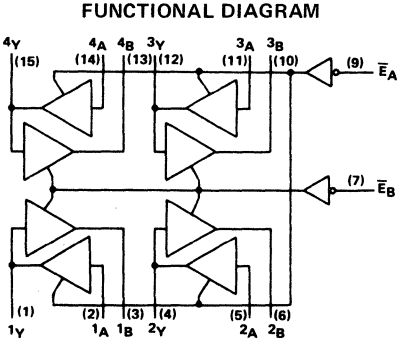
- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY 300pF
- SOURCE CURRENT 4mA
- SINK CURRENT 6mA
- PROPAGATION DELAY: 40nsec @ 5V

TRUTH TABLE

CONTROL INPUTS		FUNCTION		
$\overline{E}_A$	$\overline{E}_B$	A	B	Y
L	L	I	O	O
L	H	I	D	O
H	L	D	O	I
H	H	ISOLATED		

I = Input, O = Output,
D = Disconnected

FUNCTIONAL DIAGRAM



HD-6434 CMOS OCTAL RESETTABLE LATCHED BUS DRIVER

FEATURES

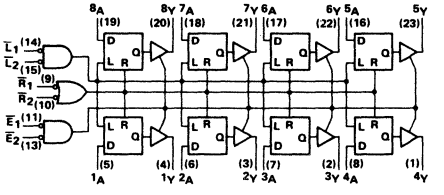
- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY 300pF
- SOURCE CURRENT 6mA
- SINK CURRENT 9mA
- PROPAGATION DELAY: 45nsec @ 5V

TRUTH TABLE

CONTROL INPUTS						DATA	
$\overline{R}_1$	$\overline{R}_2$	$\overline{E}_1$	$\overline{E}_2$	$\overline{L}_1$	$\overline{L}_2$	A	Y
X	X	H	X	X	X	X	HI-Z
X	X	X	H	X	X	X	HI-Z
L	X	L	L	X	X	X	L
X	L	L	L	X	X	X	L
H	H	L	L	L	L	L	L
H	H	L	L	L	L	H	H
H	H	L	L	↑	L	X	*
H	H	L	L	L	↑	X	*

X = Don't Care HI-Z = High Impedance
L = Low H = High
* Data is latched to the valve of the last input
↑ = Transition from a Low to High level

FUNCTIONAL DIAGRAM



HD-6435 CMOS HEX RESETTABLE LATCHED BUS DRIVER

FEATURES

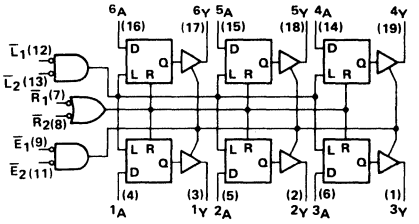
- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY 300pF
- SOURCE CURRENT 6mA
- SINK CURRENT 9mA
- PROPAGATION DELAY: 45nsec @ 5V

TRUTH TABLE

CONTROL INPUTS						DATA	
$\overline{R}_1$	$\overline{R}_2$	$\overline{E}_1$	$\overline{E}_2$	$\overline{L}_1$	$\overline{L}_2$	A	Y
X	X	H	X	X	X	X	HI-Z
X	X	X	H	X	X	X	HI-Z
L	X	L	L	X	X	X	L
X	L	L	L	X	X	X	L
H	H	L	L	L	L	L	L
H	H	L	L	L	L	H	H
H	H	L	L	↑	L	X	*
H	H	L	L	L	↑	X	*

X = Don't Care HI-Z = High Impedance
L = Low H = High
* Data is latched to the valve of the last input
↑ = Transition from a Low to High level

FUNCTIONAL DIAGRAM



HD-6436 CMOS OCTAL BUS BUFFER/DRIVER

FEATURES

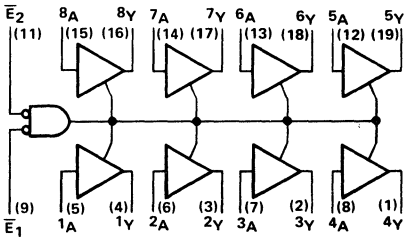
- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY 300pF
- SOURCE CURRENT 6mA
- SINK CURRENT 9mA
- PROPAGATION DELAY: 45nsec @ 5V

TRUTH TABLE

CONTROL		INPUT	OUTPUT
$\overline{E}_1$	$\overline{E}_2$	A	Y
L	L	L	L
L	L	H	H
L	H	X	HI-Z
H	L	X	HI-Z
H	H	X	HI-Z

L = Low, H = High X = Don't Care
HI-Z = High Impedance

FUNCTIONAL DIAGRAM



HD-6440 CMOS LATCHED 3 TO 8 LINE DECODER-DRIVER

FEATURES

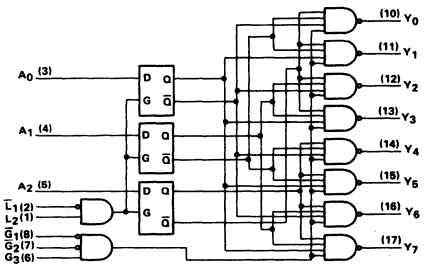
- HIGH SPEED DECODING FOR MEMORY ARRAYS
- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY 200pF
- SOURCE CURRENT .... 2 mA
- SINK CURRENT ..... 2.4 mA
- PROPAGATION DELAY . 65nsec @ 5V

TRUTH TABLE

INPUTS				OUTPUTS	
ENABLE		ADDRESS			
$\overline{G}_1\overline{G}_2G_3$	$\overline{L}_1L_2$	$A_2A_1A_0$	$Y_0Y_1Y_2Y_3Y_4Y_5Y_6Y_7$	FUNCTION
X X L	X X	X X X	H H H H H H H H	DISABLE
X H X	X X	X X X	H H H H H H H H	
H X X	X X	X X X	H H H H H H H H	
L L H	L H	L L L	L H H H H H H H	DECODE
L L H	L H	L L H	H L H H H H H H	
L L H	L H	L H L	H H L H H H H H	
L L H	L H	L H H	H H H L H H H H	
L L H	L H	H L L	H H H H L H H H	
L L H	L H	H L H	H H H H H L H H	
L L H	L H	H H L	H H H H H H L H	
L L H	L H	H H H	H H H H H H H L	
L L H	X L	X X X	$Y_0Y_1Y_2Y_3Y_4Y_5Y_6Y_7$	LATCHED
L L H	H X	X X X	$Y_0Y_1Y_2Y_3Y_4Y_5Y_6Y_7$	

L = Low, H = High, X = Don't Care
Y_n = Data is latched to the valve of the last input

FUNCTIONAL DIAGRAM



HD-6495 CMOS HEX BUS DRIVER

FEATURES

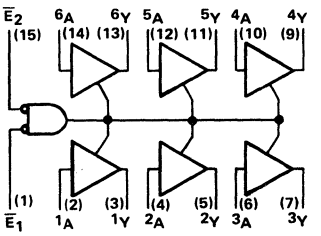
- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY 300pF
- SOURCE CURRENT 4mA
- SINK CURRENT 6mA
- PROPAGATION DELAY: 35nsec @ 5V

TRUTH TABLE

CONTROL		INPUT	OUTPUT
$\overline{E}_1$	$\overline{E}_2$	A	Y
L	L	L	L
L	L	H	H
L	H	X	HI-Z
H	L	X	HI-Z
H	H	X	HI-Z

X = Don't Care HI-Z = High Impedance

FUNCTIONAL DIAGRAM



4

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HD-4702/6405

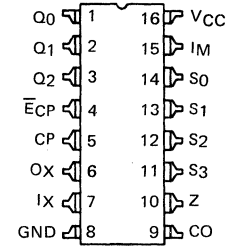
CMOS PROGRAMMABLE BIT RATE GENERATOR

Features

- HD-4702 – PROVIDES 13 COMMONLY USED BIT RATES
- HD-6405 – PROVIDES 15 COMMONLY USED BIT RATES
- USES A 2.4576MHz CRYSTAL/INPUT FOR STANDARD FREQUENCY OUTPUT (16 TIMES BIT RATE)
- TTL COMPATIBLE – OUTPUT WILL SINK 1.6mA
- LOW POWER DISSIPATION HD-6405 4.0mW TYP. @ 2.4576MHz
  HD-4702 4.5mW TYP. @ 2.4576MHz
- CONFORMS TO EIA RS-404
- ONE HD-4702 OR HD-6405 CONTROLS UP TO EIGHT TRANSMISSION CHANNELS
- INITIALIZATION CIRCUIT FACILITATES DIAGNOSTIC FAULT ISOLATION
- ON-CHIP INPUT PULL-UP CIRCUIT – HD-4702 ONLY

Pinout

TOP VIEW



PIN NAMES

$\overline{CP}$	External Clock Input
$\overline{E}_{CP}$	External Clock Enable Input (Active Low)
I_X	Crystal Input
I_M	Multiplexed Input
$S_0 - S_3$	Rate Select Inputs
CO	Clock Output
O_X	Crystal Drive Output
$Q_0 - Q_2$	Scan Counter Outputs
Z	Bit Rate Output

Description

The HD-4702/6405 Bit Rate Generator provides the necessary clock signals for digital data transmission systems, such as UART. It generates 13(HD-4702) or 15(HD-6405) commonly used bit rates using an on-chip crystal oscillator or an external input. For conventional operation generating 16 output clock pulses per bit period, the input clock frequency must be 2.4576MHz (i.e. 9600 Baud x 16 x 16, since there is an internal ÷16 prescaler). A lower input frequency will result in a proportionally lower output frequency.

The HD-4702/6405 can provide multi-channel operation with a minimum of external logic by having the clock frequency CO and the ÷8 prescaler outputs Q_0, Q_1, Q_2 available externally. All signals have a 50% duty cycle except 1800 Baud and 2000 Baud which has less than 0.39% distortion and 3600 Baud which has less than 0.78% distortion.

The four rate select inputs (S_0-S_3) select which bit rate is at the output (Z). The table lists select code and output bit rate. Two of the 16 for the HD-4702 and one of the 16 for the HD-6405 do not select an internally generated frequency, but select an input into which the user can feed either a different frequency, or a static level (High or Low) to generate "ZERO BAUD".

The bit rate most commonly used in modern data terminals (110, 150, 300, 1200, 2400 Baud) require that no more than one input be grounded for the HD-4702, which is easily achieved with a single, 5-position switch.

The HD-4702/6405 has an initialization circuit which generates a common master reset for all flip-flops. This signal is derived from a digital differentiator that senses the first high level on the CP input after the $\overline{E}_{CP}$ input goes low. When $\overline{E}_{CP}$ is high, selecting the crystal input, CP must be low. A high level on CP would apply a continuous reset.

For the HD-4702, all inputs except I_X have on-chip pull-up circuits which provide TTL compatibility and eliminate the need to tie a permanently high input to V_{CC}.

Truth Tables

TABLE 1
CLOCK MODES AND INITIALIZATION

I_X	E_{CP}	CP	OPERATION
⎍⎍	H	L	Clocked from I_X
X	L	⎍⎍	Clocked from CP
X	H	H	Continuous Reset
X	L	⎍	Reset During 1st CP = HIGH Time

NOTE: Actual output frequency is 16 times the indicated Output Rate, assuming a clock frequency of 2.4576MHz.

H = HIGH Level
L = LOW Level
X = Don't care
⎍ = 1st HIGH Level Clock Pulse after E_{CP} goes LOW
⎍⎍ = Clock Pulse

TABLE 2
TRUTH TABLE FOR RATE SELECT INPUTS

S_3 S_2 S_1 S_0	OUTPUT RATE (Z) HD-4702	OUTPUT RATE (Z) HD-6405
L L L L	MUX INPUT (I_M) ①	MUX INPUT (I_M) ①
L L L H	MUX INPUT (I_M)	2000 BAUD
L L H L	50 BAUD	50 BAUD
L L H H	75 BAUD	75 BAUD
L H L L	134.5 BAUD	134.5 BAUD
L H L H	200 BAUD	200 BAUD
L H H L	600 BAUD	600 BAUD
L H H H	2400 BAUD	3600 BAUD
H L L L	9600 BAUD	9600 BAUD
H L L H	4800 BAUD	4800 BAUD
H L H L	1800 BAUD	1800 BAUD
H L H H	1200 BAUD	1200 BAUD
H H L L	2400 BAUD	2400 BAUD
H H L H	300 BAUD	300 BAUD
H H H L	150 BAUD	150 BAUD
H H H H	110 BAUD	110 BAUD

NOTE:
① 19200 BAUD by connecting Q_2 to I_M.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+12.0V
Input or Output Voltage Applied	GND -0.3 to V_{CC} +0.3
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-4702A-9/6405A-9	-40°C to +85°C
Military HD-4702A-2/6405A-2	-55°C to +125°C
Operating Voltage Range	+4V to +11V

ELECTRICAL CHARACTERISTICS

D.C.: V_{CC} = 10V ± 10%; T_A = Industrial or Military.
A.C.: V_{CC} = 10V; T_A = 25°C.

	SYMBOL	PARAMETER	HD-4702A-2/ 6405A-2 MIN	TYP	MAX	HD-4702A-9/ 6405A-9 MIN	TYP	MAX	UNITS	TEST CONDITIONS
D.C.	V_{IH}	Input High Voltage	70% V_{CC}			70% V_{CC}			V	
	V_{IL}	Input Low Voltage			20% V_{CC}			20% V_{CC}	V	
	V_{OH1}	Output High Voltage	V_{CC} -0.1			V_{CC} -0.1			V	$I_{OH} \leq -1\mu A$
	V_{OL1}	Output Low Voltage	GND +0.1			GND +0.1			V	$I_{OL} \leq +1\mu A$
	I_{IH}	Input High Current	-1		+1	-1		+1	μA	$V_I = V_{CC}$, All other pins = 0V
	I_{IL}	INPUT ① HD-4702 (all other inputs) LOW		-110	-170		-110	-170	μA	
	I_{ILX}	CURRENT (IX inputs)	-1		+1	-1		+1	μA	V_I = 0, All other pins = V_{CC}
	I_{IL}	HD-6405 - All pins	-1		10	-1		10	μA	
	I_{OHX}	OUTPUT (OX) HIGH	0.2			0.2			mA	V_{OUT} = 9.5 Input at 0 or V_{CC} per Logic Function
	I_{OH}	CURRENT (all other outputs)	0.6			0.6			mA	V_{OUT} = 9.5 or Truth Table
	I_{OLX}	OUTPUT (OX) LOW	0.2			0.2			mA	V_{OUT} = .5V
	I_{OL}	CURRENT (all other outputs)	3.2			3.2			mA	V_{OUT} = .5V
		SUPPLY ① HD-4702A			1000			3000	μA	$\overline{E}_{CP}$ = V_{CC}, CP = 0, All other inputs = GND
		CURRENT HD-4702A			500			1000	μA	$\overline{E}_{CP}$ = V_{CC}, CP = 0, All other inputs = V_{CC}
		(STATIC) HD-6405A			500			500	μA	$\overline{E}_{CP}$ = V_{CC}, CP = 0, All other inputs = V_{CC} or GND
A.C.	t_{PLH} t_{PHL}	Propagation Delay, IX to CO			150 125			150 125	ns ns	$C_L \leq$ 7pF on OX ②
	t_{PLH} t_{PHL}	Propagation Delay, CP to CO			110 100			110 100	ns ns	C_L = 15pF Input Transition Times ≤ 20ns
	t_{PLH} t_{PHL}	Propagation Delay, CO to Q_n			⑤			⑤	ns ns	
	t_{PLH} t_{PHL}	Propagation Delay, CO to Z			40 35			40 35	ns ns	
	t_{TLH} t_{THL}	Output Transition Time (except OX)			40 20			40 20	ns ns	
	t_{PLH} t_{PHL}	Propagation Delay, IX to CO			175 140			175 140	ns ns	$C_L \leq$ 7pF on OX ②
	t_{PLH} t_{PHL}	Propagation Delay, CP to CO			130 110			130 110	ns ns	C_L = 50pF Input Transition Times ≤ 20ns
	t_{PLH} t_{PHL}	Propagation Delay, CO to Q_n			⑤			⑤	ns ns	
	t_{PLH} t_{PHL}	Propagation Delay, CO to Z			45 40			45 40	ns ns	
	t_{TLH} t_{THL}	Output Transition Time (except OX)			80 40			80 40	ns ns	
	t_s t_h	Set-Up Time, Select to CO Hold Time, Select to CO	175 0			175 0			ns ns	$C_L \leq$ 7pF on OX ②
	t_s t_h	Set-Up Time, IM to CO Hold Time, IM to CO	175 20			175 20			ns ns	C_L = 15pF Input Transition Times ≤ 20ns
	$t_{WCP(L)}$ $t_{WCP(H)}$	Minimum Clock Pulse-Width Low and High ③ ④	60 60			60 60			ns ns	
	$t_{WCP(L)}$ $t_{WCP(H)}$	Minimum IX Pulse Width, Low and High ④	80 80			80 80			ns ns	

NOTES:

① Input Current and Quiescent Power Supply Current are relatively higher for this device because of active pull-up circuits on all inputs except IX. This is done for TTL compatibility.
② Propagation Delays (t_{PLH} and t_{PHL}) and Output Transistion Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-Up Times (t_s), Hold Times (t_h), and Mininum Pulse Widths (t_W) do not vary with load capacitance.
③ The first High Level Clock Pulse after $\overline{E}_{CP}$ goes Low and must be at least 200ns long to guarantee reset of all Counters.
④ It is recommended that input rise and fall times to the Clock Inputs (CP, IX) be less than 4μs.
⑤ For multichannel operation, Propagation Delay (CO to Q_n) plus Set-Up Time, Select to CO, is guaranteed to be ≤ 190ns.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage		+8.0V
Input or Output Voltage Applied		GND -0.3V to V_{CC} +0.3V
Storage Temperature Range		-65°C to +150°C
Operating Temperature Range		
Industrial	HD-4702-9/6405-9	-40°C to +85°C
Military	HD-4702-2/6405-2	-55°C to +125°C
Operating Voltage Range		+4 to +7V

ELECTRICAL CHARACTERISTICS

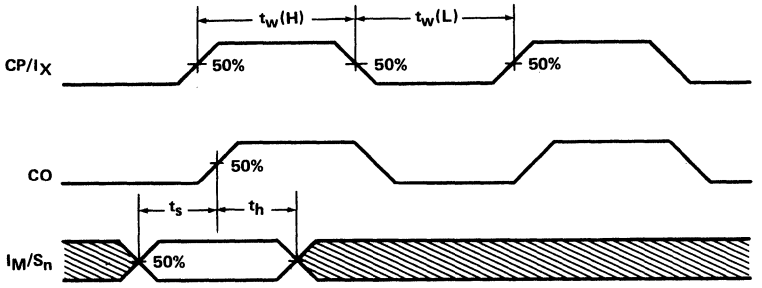
D.C.: V_{CC} = 5V ± 10%; T_A = Industrial or Military.
A.C.: V_{CC} = 5V; T_A = 25°C.

	SYMBOL	PARAMETER	HD-4702-2/ 6405-2 MIN	TYP	MAX	HD-4702-9/ 6405-9 MIN	TYP	MAX	UNITS	TEST CONDITIONS
D.C.	V_{IH}	Input High Voltage	V_{CC} -1.5			V_{CC} -1.5			V	
	V_{IL}	Input Low Voltage			1.5			1.5	V	
	V_{OH1}	Output High Voltage	V_{CC} -.05			V_{CC} -.05			V	$I_{OH} \leq -1\mu A$
	V_{OL1}	Output Low Voltage			0.05			0.05	V	$I_{OL} \leq +1\mu A$
	I_{IH}	Input High Current	-1		+1	-1		+1	μA	$V_I = V_{CC}$, All other pins = 0V
	I_{IL}	INPUT HD-4702 ① (all other inputs) LOW		-30	-50		-30	-50	μA	
	I_{ILX}	CURRENT (I_X inputs)	-1		+1	-1		+1	μA	V_I = 0, All other pins = V_{CC}
	I_{IL}	HD-6405 - All pins	-1		+1	-1		+1	μA	
	I_{OHX}	OUTPUT (O_X)	-0.1			-0.1			mA	$V_{OUT} = V_{CC}$ -.5
	I_{OH1}	HIGH (all other outputs)	-1.0			-1.0			mA	V_{OUT} = 2.5V
	I_{OH2}	CURRENT (all other outputs)	-0.3			-0.3			mA	$V_{OUT} = V_{CC}$ -.5
	I_{OLX}	OUTPUT (O_X) LOW	0.1			0.1			mA	V_{OUT} = .4V
	I_{OL}	CURRENT (all other outputs)	1.6			1.6			mA	V_{OUT} = .4V
	ICC	SUPPLY ① HD-4702 CURRENT HD-4702 (STATIC) HD-6405			500 150 150			1500 1000 150	μA μA μA	$\overline{E}_{CP} = V_{CC}$, CP = 0, All other inputs = GND $\overline{E}_{CP} = V_{CC}$, CP = 0, All other inputs = V_{CC} $\overline{E}_{CP} = V_{CC}$, CP = 0, All other inputs = V_{CC} or GND
A.C.	t_{PLH} t_{PHL}	Propagation Delay, I_X to CO			300 250			300 250	ns ns	$C_L \leq 7$pF on O_X ②
	t_{PLH} t_{PHL}	Propagation Delay, CP to CO			215 195			215 195	ns ns	C_L = 15pF Input Transition Times ≤ 20ns
	t_{PLH} t_{PHL}	Propagation Delay, CO to Q_n			⑤			⑤	ns ns	
	t_{PLH} t_{PHL}	Propagation Delay, C_O to Z			75 65			75 65	ns ns	
	t_{TLH} t_{THL}	Output Transition Time (except O_X)			80 40			80 40	ns ns	
	t_{PLH} t_{PHL}	Propagation Delay, I_X to CO			350 275			350 275	ns ns	$C_L \leq 7$pF on O_X ②
	t_{PLH} t_{PHL}	Propagation Delay, CP to CO			260 220			260 220	ns ns	C_L = 50pF Input Transition Times ≤ 20ns
	t_{PLH} t_{PHL}	Propagation Delay, CO to Q_n			⑤			⑤	ns ns	
	t_{PLH} t_{PHL}	Propagation Delay, CO to Z			85 75			85 75	ns ns	
	t_{TLH} t_{THL}	Output Transition Time (except O_X)			160 75			160 75	ns ns	
	t_s t_h	Set-Up Time, Select to CO Hold Time, Select to CO	350 0			350 0			ns ns	$C_L \leq 7$pF on O_X ②
	t_s t_h	Set-Up Time, I_M to CO Hold Time, I_M to CO	350 0			350 0			ns ns	C_L = 15pF Input Transition Times ≤ 20ns
	$t_{WCP(L)}$ $t_{WCP(H)}$	Minimum Clock Pulse-Width Low and High ③ ④	120 120			120 120			ns ns	
	$t_{WCP(L)}$ $t_{WCP(H)}$	Minimum I_X Pulse Width, Low and High ④	160 160			160 160			ns ns	

NOTES:

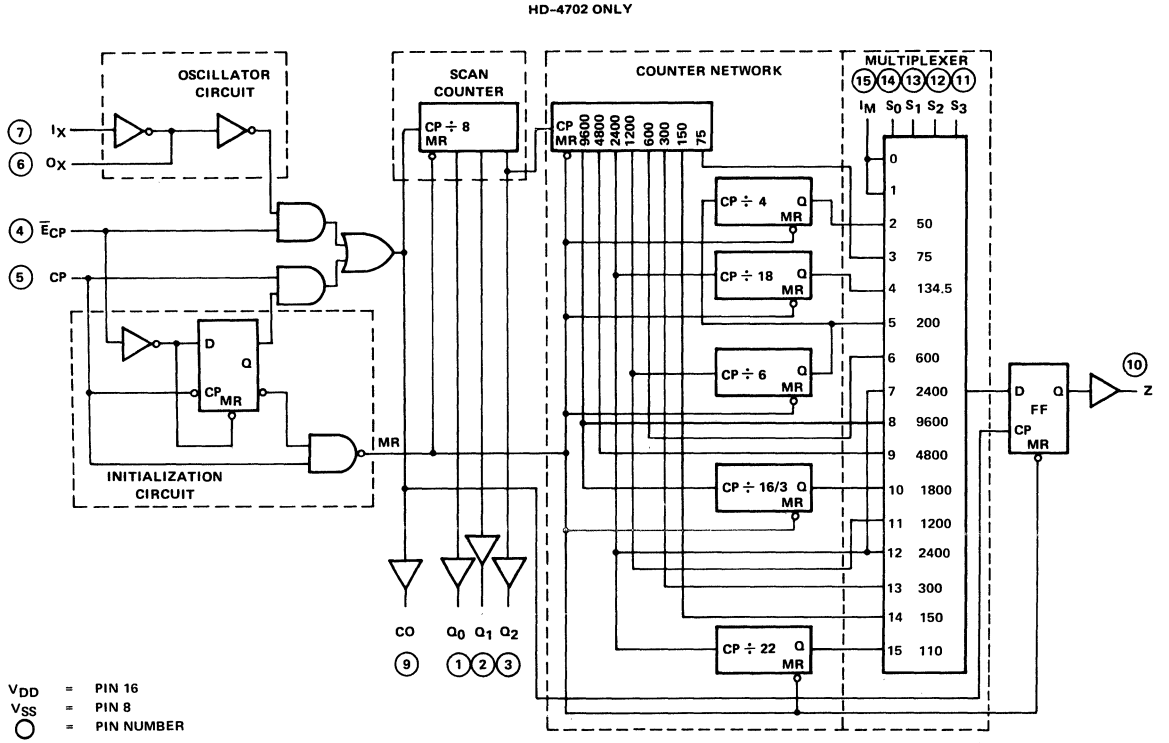
① Input Current and Quiescent Power Supply Current are relatively higher for this device because of active pull-up circuits on all inputs except I_X. This is done for TTL compatibility.
② Propagation Delays (t_{PLH} and t_{PHL}) and Output Transistion Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-Up Times (t_s), Hold Times (t_h), and Mininum Pulse Widths (t_W) do not vary with load capacitance.
③ The first High Level Clock Pulse after $\overline{E}_{CP}$ goes Low and must be at least 350ns long to guarantee reset of all Counters.
④ It is recommended that input rise and fall times to the Clock Inputs (CP, I_X) be less than 15μs.
⑤ For multichannel operation, Propagation Delay (CO to Q_n) plus Set-Up Time, Select to CO, is guaranteed to be ≤ 367ns.

Switching Waveforms



NOTE: Set-Up and Hold Times are shown as positive values but may be specified as negative values.

Block Diagram



SINGLE CHANNEL BIT RATE GENERATOR

Figure 1 shows the simplest application of the HD-4702/6405. This circuit generates one of five possible bit rates as determined by the setting of a single pole, 5-position switch. The Bit Rate Output (Z) drives one standard TTL load or four low power Schottky loads over the full temperature range. The possible output frequencies correspond to 110, 150, 300, 1200, and 2400 or 3600 Baud. For many low cost terminals, these five bit rates are adequate.

SIMULTANEOUS GENERATION OF SEVERAL BIT RATES

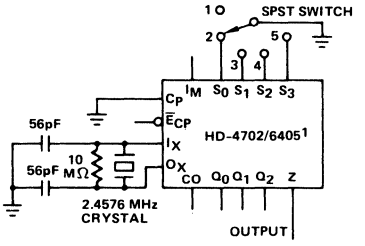
Figure 2 shows a simple scheme that generates eight bit rates on eight output lines, using one HD-4702/6405 and one 93L34 Bit Addressable Latch. This and the following applications take advantage of the built-in scan counter (prescaler) outputs, As shown in the block diagram, these outputs (Q_0 to Q_2) go through a complete sequence of eight states for every half-period of the highest output frequency (9600 Baud). Feeding these Scan Counter Outputs back to the Select Inputs of the multiplexer causes the HD-4702/6405 to interrogate sequentially the state of eight different frequency signals. The 93L34 8 Bit Addressable Latch, addressed by the same Scan Counter Outputs, re-converts the multiplexed single Output (Z) of the HD-4702/6405 into eight parallel output frequency signals. In the simple scheme of Figure 2, input S_3 is left open (HIGH) and the following bit rates are generated:

Q_0: 110 Baud Q_1: 9600 Baud Q_2: 4800 Baud
Q_3: 1800 Baud Q_4: 1200 Baud Q_5: 2400 Baud
Q_6: 300 Baud Q_7: 150 Baud

Other bit rate combinations can be generated by changing the Scan Counter to Selector interconnection or by inserting logic gates into this path.

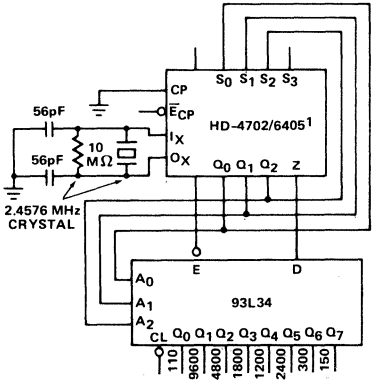
19200 BAUD OPERATION

Though a 19200 Buad signal is not internally routed to the multiplexer, the HD-4702/6405 can be used to generate this bit rate by connecting the Q_2 output to the I_M input and applying select code. An additional 2-input NOR gate can be used to retain the "Zero Baud" feature on select code 1 for the HD-4702 (See Figure 3).



SWITCH POSITION	HD-4702 BIT RATE	HD-6405 BIT RATE
1	110 Baud	110 Baud
2	150 Baud	150 Baud
3	300 Baud	300 Baud
4	1200 Baud	1200 Baud
5	2400 Baud	3600 Baud

FIGURE 1
Switch selectable bit rate generator configuration providing five bit rates.



NOTE 1: Need to add pull-up resistor on all inputs for the HD-6405.

FIGURE 2
Bit rate generator configuration with eight simultaneous frequencies

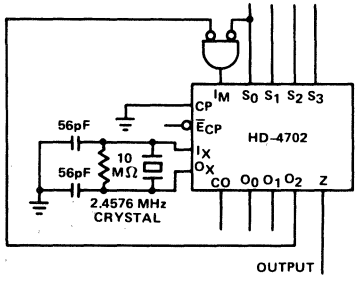


FIGURE 3
19200 Baud Operation

TABLE 3
CRYSTAL SPECIFICATIONS

PARAMETERS	TYPICAL CRYSTAL SPEC
Frequency	2.4576 MHz "AT" Cut
Series Resistance (Max)	250
Unwanted Modes	-6.0dB (Min)
Type of Operation	Parallel
Load Capacitance	32pF +0.5

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HD-6402

CMOS/LSI Universal Asynchronous Receiver Transmitter (UART)

Features

- OPERATION FROM D.C. TO 4.0MHz @10.0 VOLTS
- LOW POWER-TYP. 10mW @ 2.0MHz AND 5.0 VOLTS
- 4 TO 11 VOLT OPERATION
- PROGRAMMABLE WORD LENGTH, STOP BITS AND PARITY
- AUTOMATIC DATA FORMATTING AND STATUS GENERATION
- COMPATIBLE WITH INDUSTRY STANDARD UART'S
- SINGLE POWER SUPPLY

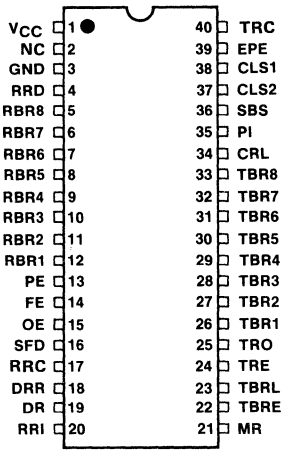
Description

The HD-6402 is a CMOS/LSI subsystem for interfacing computers or microprocessors to an asynchronous serial data channel. The receiver converts serial start, data, parity and stop bits to parallel data verifying proper code transmission, parity, and stop bits. The transmitter converts parallel data into serial form and automatically adds start, parity, and stop bits. The data word length can be 5, 6, 7 or 8 bits. Parity may be odd or even. Parity checking and generation can be inhibited. The stop bits may be one or two or one and one-half when transmitting 5 bit code.

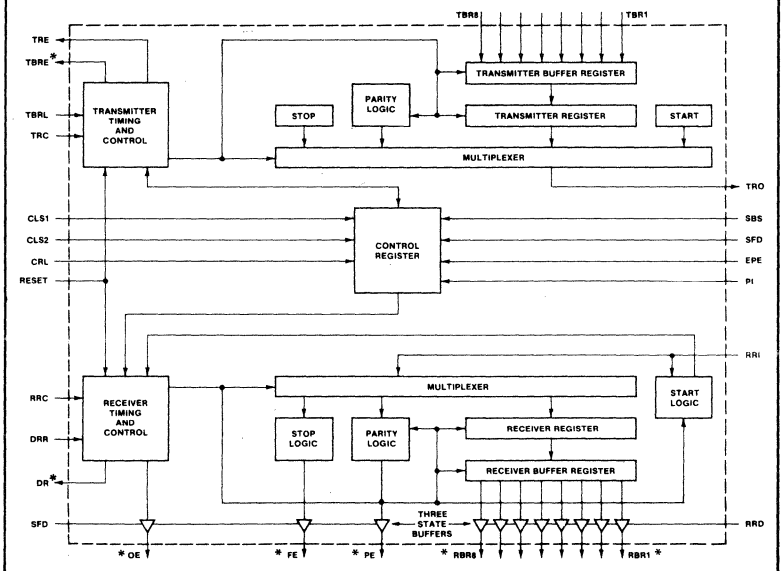
The HD-6402 can be used in a wide range of applications including modems, printers, peripherals and remote data aquisition systems. CMOS/LSI technology permits operation clock frequencies up to 4.0MHz (250K Baud) an improvement of 10 to 1 over previous PMOS UART designs. Power requirements, by comparison, are reduced from 300mW to 10mW. Status logic increases flexibility and simplifies the user interface.

Pinout

TOP VIEW



Functional Diagram



* These outputs are three state

Control Definition

CONTROL WORD						CHARACTER FORMAT			
CLS2	CLS1	PI	PE	SB		START BIT	DATA BITS	PARITY BIT	STOP BITS
0	0	0	0	0		1	5	ODD	1
0	0	0	0	1		1	5	ODD	1.5
0	0	0	1	0		1	5	EVEN	1
0	0	0	1	1		1	5	EVEN	1.5
0	0	1	X	0		1	5	NONE	1
0	0	1	X	1		1	5	NONE	1.5
0	1	0	0	0		1	6	ODD	1
0	1	0	0	1		1	6	ODD	2
0	1	0	1	0		1	6	EVEN	1
0	1	0	1	1		1	6	EVEN	2
0	1	1	X	0		1	6	NONE	1
0	1	1	X	1		1	6	NONE	2
1	0	0	0	0		1	7	ODD	1
1	0	0	0	1		1	7	ODD	2
1	0	0	1	0		1	7	EVEN	1
1	0	0	1	1		1	7	EVEN	2
1	0	1	X	0		1	7	NONE	1
1	0	1	X	1		1	7	NONE	2
1	1	0	0	0		1	8	ODD	1
1	1	0	0	1		1	8	ODD	2
1	1	0	1	0		1	8	EVEN	1
1	1	0	1	1		1	8	EVEN	2
1	1	1	X	0		1	8	NONE	1
1	1	1	X	1		1	8	NONE	2

4

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+12.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature Range	-65°C to 150°C
Operating Temperature Range	
Industrial HD-6402A-9	-40°C to +85°C
Military HD-6402A-2	-55°C to +125°C

ELECTRICAL CHARACTERISTICS

VCC = 10.0V ± 0.5V, TA = Industrial or Military

D.C.

SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% VCC			V	
V_{IL}	Logical "0" Input Voltage			20% VCC	V	
I_{IL}	Input Leakage	-1.0		1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage*	VCC -0.01			V	$I_{OUT} = 0$
V_{OL}	Logical "0" Output Voltage*			GND +0.01	V	$I_{OUT} = 0$
I_O	Output Leakage	-1.0		1.0	μA	$0V \leq V_O \leq V_{CC}$
I_{CC}	Supply Current		5.0	500	μA	$V_{CC} = 10.5V$, $V_{IN} = V_{CC}$ or GND
C_{IN}	Input Capacitance*		7.0	8.0	pF	
C_O	Output Capacitance*		6.0	10.0	pF	

*Guaranteed but not 100% tested.

A.C.

		VCC = 10.0V ① TA = 25°C			VCC = 10V ± 0.5V TA = Industrial or Military				
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS	CONDITIONS
f_{clock}	Clock Frequency	D.C.		6.0	D.C.		4.0	MHz	
t_{pw}	Pulse Widths CRL, DRR, TBRL	75			100			ns	C_L = 50pF
t_{MP}	Pulse Width MR	350			400			ns	See Switching Time
t_{SET}	Input Data Setup Time	40			40			ns	Waveforms 1, 2, 3
t_{HOLD}	Input Data Hold Time	30			30			ns	
t_{EN}	Output Enable Time			50			70	ns	

NOTE ①: All devices guaranteed at worst case limits. Room temperature, 10V data provided for information-not guaranteed.

Switching Waveforms

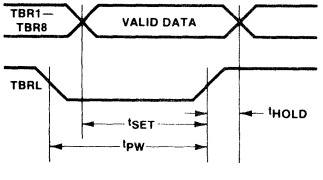


FIGURE 1
Data Input Cycle

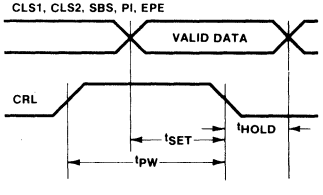


FIGURE 2
Control Register Load Cycle

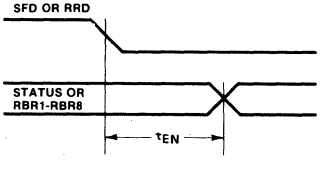


FIGURE 3
Status Flag Output Enable Time or Data Output Enable Time

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6402-9	-40°C to +85°C
Military HD-6402-2	-55°C to +125°C

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%. T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}			V	
V_{IL}	Logical "0" Input Voltage			20% V_{CC}	V	
I_{IL}	Input Leakage	-1.0		1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	2.4			V	$I_{OH} = -0.2mA$
V_{OL}	Logical "0" Output Voltage			0.45	V	$I_{OL} = 2.0mA$
I_O	Output Leakage	-1.0		1.0	μA	$0V \leq V_O \leq V_{CC}$
I_{CC}	Supply Current		1.0	100	μA	V_{IN} = GND or V_{CC}; V_{CC} = 5.5V, Output Open
C_{IN}	Input Capacitance*		7.0	8.0	pF	
C_O	Output Capacitance*		8.0	10.0	pF	

*Guaranteed but not 100% tested

A.C.

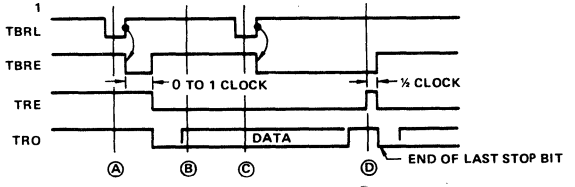
		V_{CC} = 5.0V ① T_A = 25°C			V_{CC} = 5.0V ± 10% T_A = Indust. or Mil.				
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS	CONDITIONS
f_{clock}	Clock Frequency	D.C.		3.0	D.C.		2.0	MHz	
t_{pw}	Pulse Widths CRL, DRR, TBRL	150			150			ns	C_L = 50pF
t_{MR}	Pulse Width MR	350			400			ns	See Switching Time
t_{SET}	Input Data Setup Time	50			50			ns	Waveforms 1, 2, 3
t_{HOLD}	Input Data Hold Time	60			60			ns	
t_{EN}	Output Enable Time			125			160	ns	

NOTE ① All devices guaranteed at worst case limits. Room temperature, 5V data provided for information-not guaranteed.

4

Transmitter Operation

The transmitter section accepts parallel data, formats it and transmits it in serial form on the TROutput terminal. Ⓐ Data is loaded into the transmitter buffer register from the inputs TR1 through TR8 by a logic low on the TBRLoad input. Valid data must be present at least t_{SET} prior to and t_{HOLD} following the rising edge of TBRL. If words less than 8 bits are used, only the least significant bits are used. The character is right justified into the least significant bit, TR1. Ⓑ The rising edge of TBRL clears TBREmpty. 0 to 1 clock cycles later, data is transferred to the transmitter register; TREmpty is cleared; TBREmpty is set high; and serial data transmission is started. Output data is clocked by TRClock. The clock rate is 16 times the data rate. Ⓒ A second pulse on TBRLoad loads data into the transmitter buffer register. Data transfer to the transmitter register is delayed until transmission of the current character is complete. Ⓓ Data is automatically transferred to the transmitter register and transmission of that character begins one clock cycle later.



TRANSMITTER TIMING (NOT TO SCALE)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range (Industrial -9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS $V_{CC} = 5.0V \pm 5\%$. T_A = Industrial

	SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	CONDITIONS
D.C.	V_{IH}	Logical "1" Input Voltage	V_{CC} -2.0			V	
	V_{IL}	Logical "0" Input Voltage			0.8	V	
	I_{IL}	Input Leakage	-10.0		+10.0	μA	$0V \leq V_{IN} \leq V_{CC}$
	V_{OH}	Logical "1" Output Voltage	2.4			V	I_{OH} = -0.2mA
	V_{OL}	Logical "0" Output Voltage			0.45	V	I_{OL} = 2.0mA
	I_O	Output Leakage	-10.0		+10.0	μA	$0V \leq V_O \leq V_{CC}$
	I_{CC}	Supply Current		1.0	800	μA	V_{IN} = GND or V_{CC}, V_{CC} = 5.25V, Output Open
	C_{IN}	Input Capacitance*		7.0	8.0	pF	
	C_O	Output Capacitance*		8.0	10.0	pF	

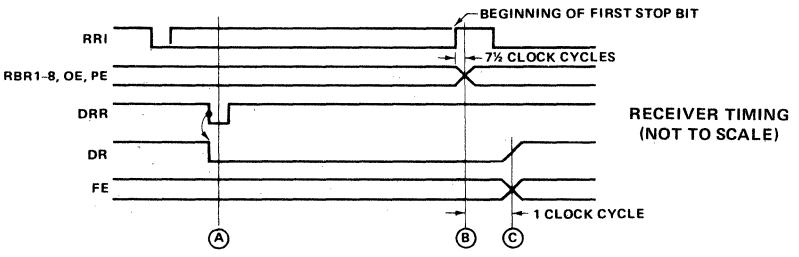
*Guaranteed but not 100% tested.

			$V_{CC} = 5.0V$ ① $T_A = 25°C$			$V_{CC} = 5.0V \pm 5\%$ T_A = Industrial				
	SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS	CONDITIONS
A.C.	f_{clock}	Clock Frequency	D.C.		2.0	D.C.		1.0	MHz	
	t_{pw}	Pulse Widths CRL, DRR, TBRL	200			225			ns	C_L = 50pF
	t_{MR}	Pulse Width MR	500			600			ns	See Switching Time
	t_{SET}	Input Data Setup Time	60			75			ns	Waveforms 1, 2, 3
	t_{HOLD}	Input Data Hold Time	75			90			ns	
	t_{EN}	Output Enable Time			150			190	ns	

NOTE ①: All devices guaranteed at worst case limits. Room temperature, 5V data provided for information-not guaranteed.

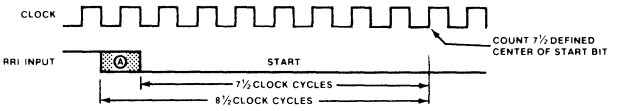
Receiver Operation

Data is received in serial form at the RInput. When no data is being received, RInput must remain high. The data is clocked through the RRClock. The clock rate is 16 times the data rate. Ⓐ A low level on DRReset clears the DReady line. Ⓑ During the first stop bit data is transferred from the receiver register to the RBRegister. If the word is less than 8 bits, the unused most significant bits will be a logic low. The output character is right justified to the least significant bit RBR1. A logic high on OError indicates overruns. An overrun occurs when DReady has not been cleared before the present character was transferred to the RBRegister. Ⓒ 1 clock cycle later DReady is reset to a logic high, and FError is evaluated. A logic high on FError indicates an invalid stop bit was received, a framing error. A logic high on PError indicates a parity error.



Start Bit Detection

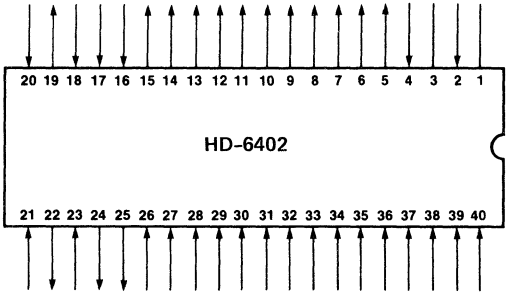
The receiver uses a 16X clock for timing. Ⓐ The start bit could have occurred as much as one clock cycle before it was detected, as indicated by the shaded portion. The center of the start bit is defined as clock count 7½. If the receiver clock is a symetrical square wave, the center of the start bit will be located within ±½ clock cycle, $\pm\frac{1}{32}$ bit or 3.125% giving a receiver margin of 46.875%. The receiver begins searching for the next start bit at the center of the first stop bit.



Pin Assignment And Functions

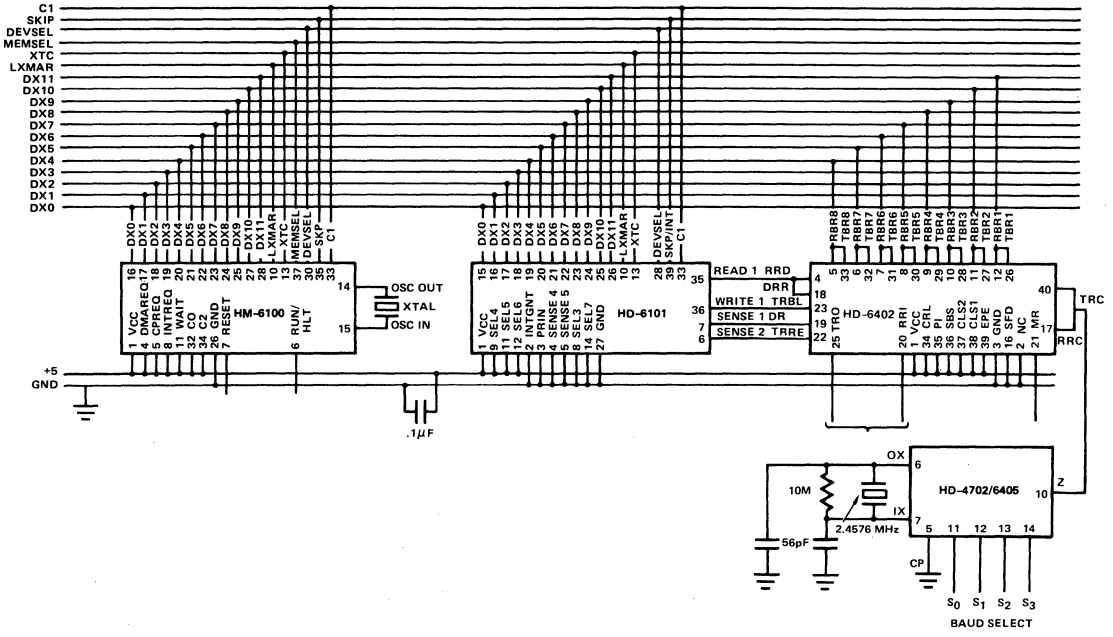
PIN	SYMBOL	DESCRIPTION
1	V_{CC}	Positive Voltage Supply
2	NC	No Connection
3	GND	Ground
4	RRD	A high level on RECEIVER REGISTER DISABLE forces the receiver holding outputs RBR1-RBR8 to a high impedance state.
5	RBR8	The contents of the RECEIVER BUFFER REGISTER appear on these three-state outputs. Word formats less than 8 characters are right justified to RBR1.
6	RBR7	See Pin 5 - RBR8
7	RBR6	See Pin 5 - RBR8
8	RBR5	See Pin 5 - RBR8
9	RBR4	See Pin 5 - RBR8
10	RBR3	See Pin 5 - RBR8
11	RBR2	See Pin 5 - RBR8
12	RBR1	See Pin 5 - RBR8
13	PE	A high level on PARITY ERROR indicates received parity does not match parity programmed by control bits. When parity is inhibited this output is low.

PIN	SYMBOL	DESCRIPTION
14	FE	A high level on FRAMING ERROR indicates the first stop bit was invalid.
15	OE	A high level on OVERRUN ERROR indicates the data received flag was not cleared before the last character was transferred to the received buffer register.
16	SFD	A high level on STATUS FLAGS DISABLE forces the outputs PE, FE, OE, DR, TBRE to a high impedance state.
17	RRC	The RECEIVER REGISTER CLOCK is 16X the receiver data rate.
18	DRR	A low level on DATA RECEIVED RESET clears the data received output DR to a low level.
19	DR	A high level on DATA RECEIVED indicates a character has been received and transferred to the receiver buffer register.
20	RRI	Serial data on RECEIVER REGISTER INPUT is clocked into the receiver register.
21	MR	A high level on MASTER RESET clears PE, FE, OE, and DR to a low level and sets the transmitter output to a high level after 18 clock cycles. MR does not clear the receiver buffer register.

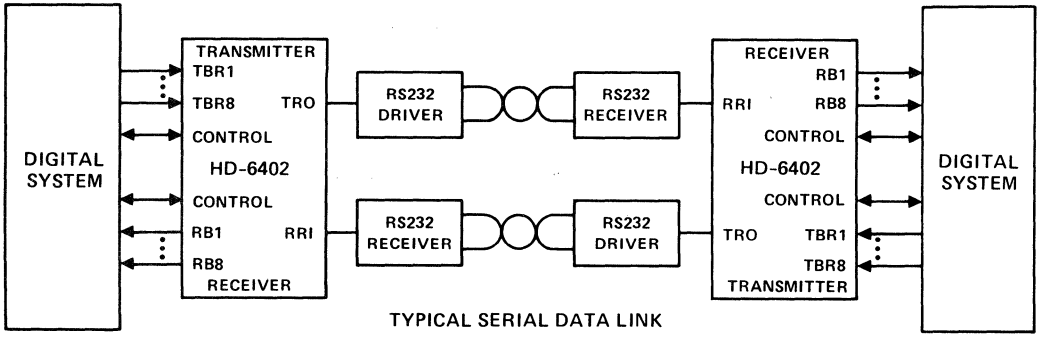


PIN	SYMBOL	DESCRIPTION
22	TBRE	A high level on TRANMITTER BUFFER REGISTER EMPTY indicates the transmitter buffer register has transferred its data to the transmitter register and is ready for new data.
23	TBRL	A low level on TRANSMITTER BUFFER REGISTER LOAD transfers data from inputs TBR1-TBR8 into the transmitter buffer register. A low to high transition on TBRL indicates data transfer to the transmitter register is busy, transfer is automatically delayed so that the two characters are transmitted end to end.
24	TRE	A high level on TRANSMITTER REGISTER EMPTY indicates completed transmission of a character including stop bits.
25	TRO	Character data, start data and stop bits appear serially at the TRANSMITTER REGISTER OUTPUT.
26	TBR1	Character data is loaded into the TRANSMITTER BUFFER REGISTER via inputs TBR1-TBR8. For character formats less than 8 bits the TBR8, 7, and 6 inputs are ignored corresponding to the programmed word length.
27	TBR2	See Pin 26 - TBR1
28	TBR3	See Pin 26 - TBR1

PIN	SYMBOL	DESCRIPTION
29	TBR4	See Pin 26 - TBR1
30	TBR5	See Pin 26 - TBR1
31	TBR6	See Pin 26 - TBR1
32	TBR7	See Pin 26 - TBR1
33	TBR8	See Pin 26 - TBR1
34	CRL	A high level on CONTROL REGISTER LOAD loads the control register.
35	PI	A high level on PARITY INHIBIT inhibits parity generation. Parity checking and forces PE output low.
36	SBS	A high level on STOP BIT SELECT selects 1.5 stop bits for 5 character format and 2 stop bits for other lengths.
37	CLS2	These inputs program the CHARACTER LENGTH SELECTED (CLS1 low CLS2 low 5 bits) (CLS1 high CLS2 low 6 bits) (CLS1 low CLS2 high 7 bits) (CLS1 high CLS2 high 8 bits)
38	CLS1	See Pin 37 - CLS2
39	EPE	When PI is low, a high level on EVEN PARITY ENABLE generates and checks even parity. A low level selects odd parity.
40	TRC	The TRANSMITTER REGISTER CLOCK is 16X the transmit data rate.



The bit rate generator is shown supplying the transmit and receive clocks for the UART.



TYPICAL SERIAL DATA LINK

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HD-6408

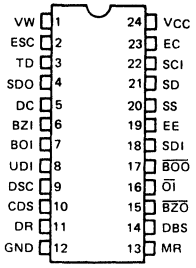
CMOS Asynchronous Serial Manchester Adapter (ASMA)

Features

- LOW BIT ERROR RATE
- ONE MEGABIT/SEC DATA RATE
- SYNC IDENTIFICATION AND LOCK-IN
- CLOCK RECOVERY
- MANCHESTER II ENCODE, DECODE
- SEPARATE ENCODE AND DECODE
- LOW OPERATING POWER: 50mW AT 5 VOLTS
- SINGLE POWER SUPPLY
- 24 PIN PACKAGE

Pinout

TOP VIEW



Description

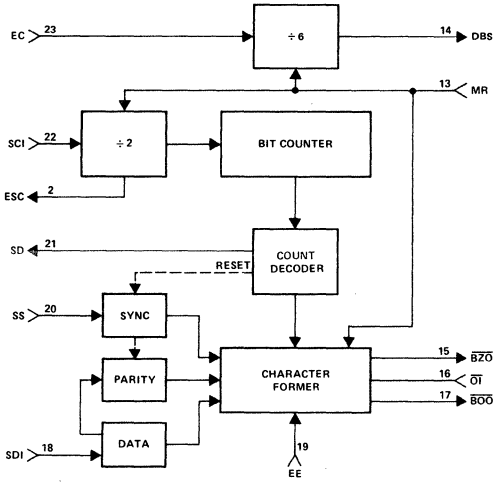
The HD-6408 is a CMOS/LSI Manchester Encoder/Decoder for creating a very high speed asynchronous serial data bus. The Encoder converts serial NRZ data (typically from a shift register) to Manchester II encoded data adding a sync pulse and parity bit. The Decoder recognizes this sync pulse and identifies it as a Command Sync or a Data Sync. The data is then decoded and shifted out in the NRZ code (typically into a shift register). Finally, the parity bit is checked. If there were no Manchester or parity errors the Decoder responds with a valid word signal. This Decoder puts the Manchester code to full use to provide clock recovery and excellent noise immunity at these very high speeds.

The HD-6408 can be used in many commercial applications such as, security systems, environmental control systems, serial data links and many others. It utilizes a single 12X clock and achieves data rates of up to one million bits per second with a very minimum overhead of only 4 bits out of 20, leaving 16 bits for data.

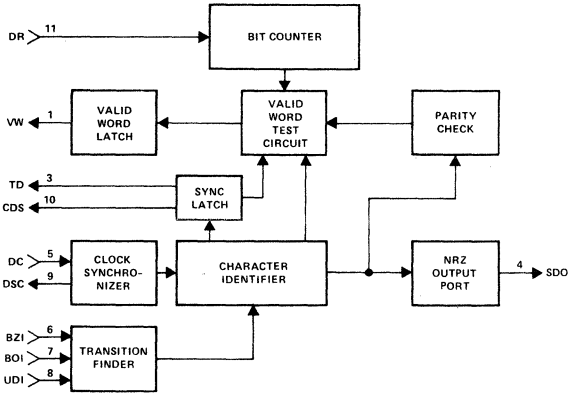
4

Block Diagrams

ENCODER



DECODER



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+7.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-40°C to +85°C

ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ±5% T_A = -40°C to +85°C

	SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	TEST CONDITIONS
D.C.	V_{IH}	Logical "1" Input Voltage	70% V_{CC}			V	
	V_{IL}	Logical "0" Input Voltage			20% V_{CC}	V	
	V_{IHC}	Logical "1" Input Voltage (Clock)	V_{CC} -0.5			V	
	V_{ILC}	Logical "0" Input Voltage (Clock)			GND +0.5	V	
	I_{IL}	Input Leakage	-1.0		+1.0	µA	$0V \leqslant V_{IN} \leqslant V_{CC}$
	V_{OH}	Logical "1" Output Voltage	2.4			V	I_{OH} = -3mA
	V_{OL}	Logical "0" Output Voltage			0.4	V	I_{OL} = 1.8mA
	I_{CCSB}	Supply Current Standby		0.5	2	mA	$V_{IN} = V_{CC} = 5.25V$ Outputs Open
	I_{CCOP}	Supply Current Operating*		8.0	10.0	mA	V_{CC} = 5.25V, f = 1MHz
	C_{IN}	Input Capacitance*		5.0	7.0	pF	
	C_O	Output Capacitance*		8.0	10.0	pF	
		*Guaranteed and sampled but not 100% tested.					
ENCODER TIMING V_{CC} = 5.0V ±5% T_A = -40°C to +85°C							
A.C.	F_{EC}	Encoder Clock Frequency			12	MHz	C_L = 50pF
	F_{ESC}	Send Clock Frequency			2.0	MHz	
	T_{ECR}	Encoder Clock Rise Time			8	ns	
	T_{ECF}	Encoder Clock Fall Time			8	ns	
	F_{ED}	Data Rate			1.0	MHz	
	T_{MR}	Master Reset Pulse Width	150			ns	
	T_{E1}	Shift Clock Delay			125	ns	
	T_{E2}	Serial Data Setup	75			ns	
	T_{E3}	Serial Data Hold	75			ns	
	T_{E4}	Enable Setup	90			ns	
	T_{E5}	Enable Pulse Width	80			ns	
	T_{E6}	Sync Setup	55			ns	
	T_{E7}	Sync Pulse Width	150			ns	
	T_{E8}	Send Data Delay			50	ns	
	T_{E9}	Bipolar Output Delay			130	ns	
DECODER TIMING V_{CC} = 5.0V ±5% T_A = -40°C to +85°C							
A.C.	F_{DC}	Decoder Clock Frequency			12	MHz	C_L = 50pF
	T_{DCR}	Decoder Clock Rise Time			8	ns	
	T_{DCF}	Decoder Clock Fall Time			8	ns	
	F_{DD}	Data Rate			1.0	MHz	
	T_{DR}	Decoder Reset Pulse Width	150			ns	
	T_{DRS}	Decoder Reset Setup Time	75			ns	
	T_{MR}	Master Reset Pulse Width	150			ns	
	T_{D1}	Bipolar Data Pulse Width	T_{DC} +10			ns	①
	T_{D2}	Sync Transition Span		18T_{DC}		ns	①
	T_{D3}	One Zero Overlap			T_{DC} -10	ns	①
	T_{D4}	Short Data Transition Span		6T_{DC}		ns	①
	T_{D5}	Long Data Transition Span		12T_{DC}		ns	①
	T_{D6}	Sync Delay (ON)		40	110	ns	
	T_{D7}	Take Data Delay (ON)		50	110	ns	
	T_{D8}	Serial Data Out Delay		70	80	ns	
	T_{D9}	Sync Delay (OFF)		90	110	ns	
	T_{D10}	Take Data Delay (OFF)		90	110	ns	
	T_{D11}	Valid Word Delay		90	110	ns	

NOTE ①: $15T_{DC}$ +10 = [15 (Decoder Clock Period)] +10ns T_{DC} = Decoder Clock Period = $\frac{1}{F_{DC}}$
These parameters are guaranteed but not 100% tested.

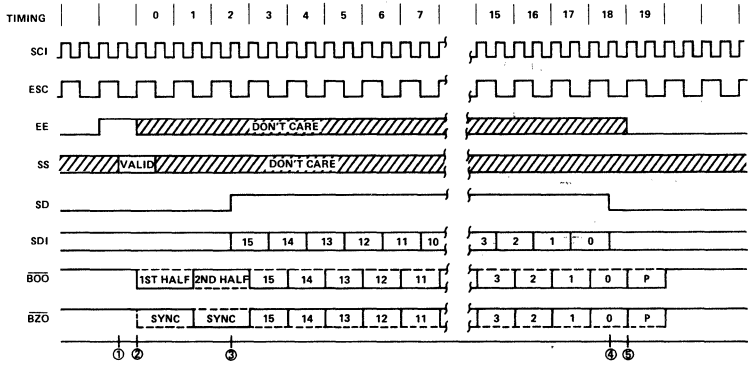
Encoder Operation

The Encoder requires a single clock with a frequency of twice the desired data rate applied at the SClock input. An auxiliary divide by six counter is provided on chip which can be utilized to produce the SClock by dividing the DClock.

The Encoder's cycle begins when EE is high during a falling edge of ESC ①. This cycle lasts for one word length or twenty ESC periods. At the next low-to-high transition of the ESC, a high at SS input actuates a Command sync or a low will produce a Data sync for that word ②. When the Encoder is ready to accept data, the SD output will go high and remain high for sixteen ESC periods ③ – ④.

During these sixteen periods the data should be clocked into the SDInput with every high-to-low transition of the ESC ③ – ④. After the sync and Manchester II encoded data are transmitted through the $\overline{BOO}$ and $\overline{BZO}$ outputs, the Encoder adds on an additional bit which is the (odd) parity for that word ⑤. At any time a low on $\overline{OI}$ will force both bipolar outputs to a high state but will not affect the Encoder in any other way.

To abort the Encoder transmission a positive pulse must be applied at MR. Any time after or during this pulse, a low-to-high transition on SC clears the internal counters an initializes the Encoder for a new word.



Decoder Operation

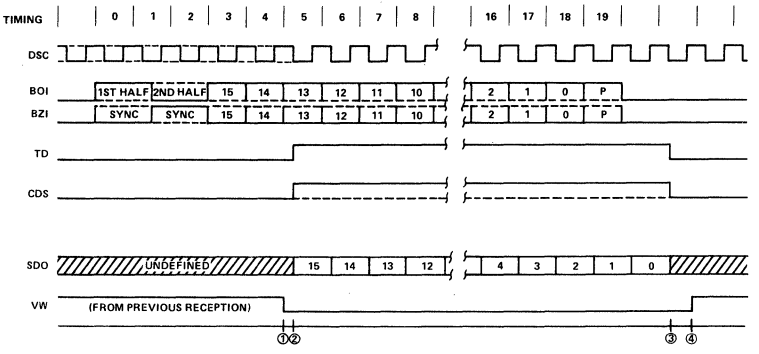
The Decoder requires a single clock with a frequency of 12 times the desired data rate applied at the DClock input. The Manchester II coded data can be presented to the Decoder in one of two ways. The BOI and BZI inputs will accept data from a differential output comparator. The UDI input can only accept noninverted Manchester II coded data (e.g. from $\overline{BZO}$ of an Encoder).

The Decoder is free running and continuously monitors its data input lines for a valid sync character and two valid Manchester data bits to start an output cycle. When a valid sync is recognized ①, the type of sync is indicated by the CDS output. If the sync character was a command, this output will go high ② and remain high for sixteen DSC periods ③, otherwise it will remain low. The TD output will go high and remain high ② – ③ while the Decoder is transmitting the decoded data through SDO.

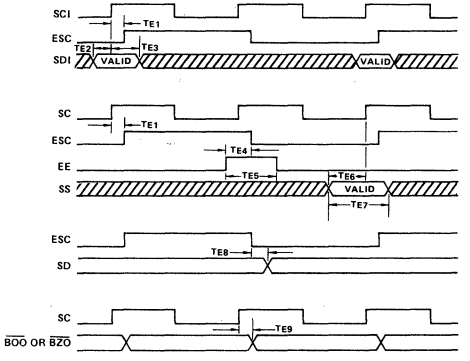
The decoded data available at SDO is in a NRZ format. The DSC is provided so that the decoded bits can get shifted into an external register on every low-to-high transition for this clock ② – ③.

After all sixteen decoded bits have been transmitted ③ the data is checked for odd parity. A high on VW output ④ indicates a successful reception of a word without any Manchester or parity errors. At this time the Decoder is looking for a new sync character to start another output sequence.

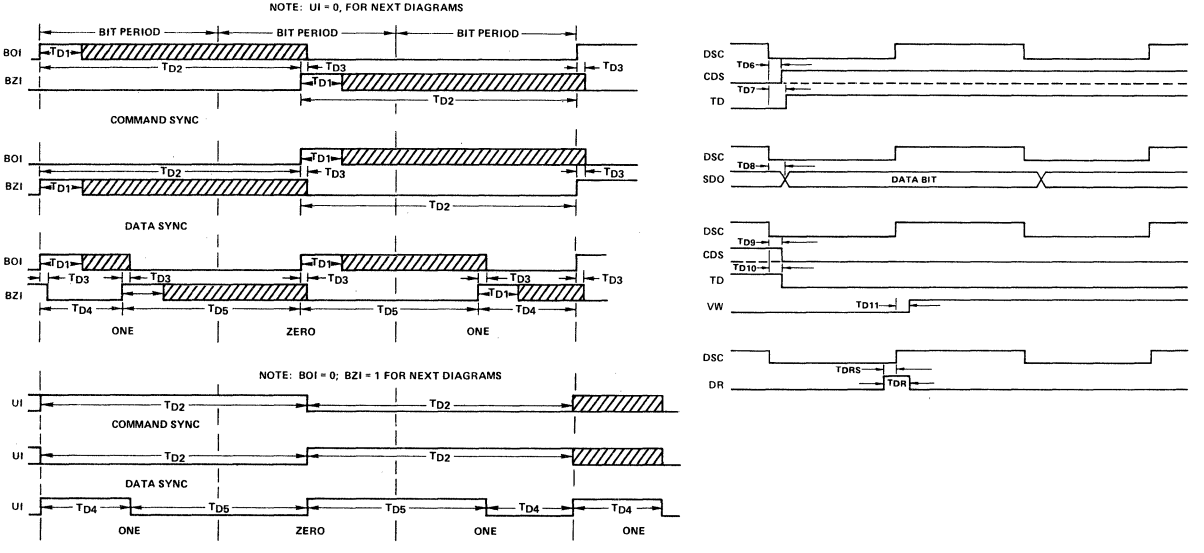
At any time in the above sequence a high input on DR during a low-to-high transition of DSC will abort transmission and initialize the Decoder to start looking for a new sync character.



Encoder Timing

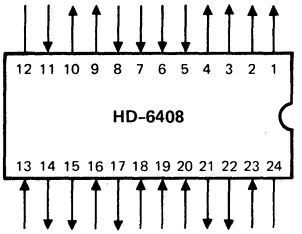


Decoder Timing



Pin Assignment and Functions

PIN	SYMBOL	SECTION	DESCRIPTION
1	VW	Decoder	Output high indicates receipt of a VALID WORD.
2	ESC	Encoder	ENCODER SHIFT CLOCK is an output for shifting data into the Encoder. This clock shifts data on a low-to-high transition.
3	TD	Decoder	TAKE DATA output is high during receipt of data after identification of a sync pulse.
4	SDO	Decoder	SERIAL DATA OUT delivers received data in correct NRZ format.
5	DC	Decoder	DECODER CLOCK input drives the transition finder, and the synchronizer which in turn supplies the clock to the balance of the Decoder.
6	BZI	Decoder	A high input should be applied to BIPOLAR ZERO IN when the bus is in its negative state. This pin must be held high when the Unipolar input is used.
7	BOI	Decoder	A high input should be applied to BIPOLAR ONE IN when the bus is in its positive state, this pin must be held low when the Unipolar input is used.
8	UDI	Decoder	With pin 6 high and pin 7 low, this pin enters UNIPOLAR DATA IN to the transition finder circuit. If not used this input must be held low.
9	DSC	Decoder	DECODER SHIFT CLOCK output delivers a frequency (DECODER CLOCK ÷ 12), synchronized by the recovered serial data stream.
10	CDS	Decoder	COMMAND/DATA SYNC output high occurs during output of decoded data which was preceded by a Command synchronizing character. A low output indicates a Data synchronizing character.
11	DR	Decoder	A high input to DECODER RESET during a rising edge of DECODER SHIFT CLOCK resets the decoder bit counting logic to a condition ready for a new word.
12	GND	Both	GROUND supply pin.



PIN	SYMBOL	SECTION	DESCRIPTION
13	MR	Both	A high on MASTER RESET clears the 2:1 counters in both the encoder and decoder.
14	DBS	Encoder	DIVIDE BY SIX is an output from 6:1 divider which is driven by the ENCODER CLOCK.
15	$\overline{BZO}$	Encoder	$\overline{BIPOLAR\ ZERO\ OUT}$ is an active low output designed to drive the zero or negative sense of a bipolar line driver.
16	$\overline{OI}$	Encoder	A low on $\overline{OUTPUT\ INHIBIT}$ forces pin 15 and 17 high, their inactive states.
17	$\overline{BOO}$	Encoder	$\overline{BIPOLAR\ ONE\ OUT}$ is an active low output designed to drive the one or positive sense of a bipolar line driver.
18	SDI	Encoder	SERIAL DATA IN accepts a serial data stream at a data rate equal to ENCODER SHIFT CLOCK.
19	EE	Encoder	A high on ENCODER ENABLE initiates the encode cycle. (Subject to the preceding cycle being complete.)
20	SS	Encoder	SYNC SELECT actuates a Command sync for an input high and Data sync for an input low.
21	SD	Encoder	SEND DATA is an active high output which enables the external source of serial data.
22	SCI	Encoder	SEND CLOCK IN is 2X the Encoder data rate.
23	EC	Encoder	ENCODER CLOCK is the input to the 6:1 divider.
24	VCC	Both	Positive supply pin.

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

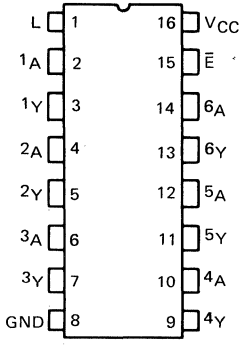
HD-6431
CMOS HEX LATCHING BUS DRIVER

Features

- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY. 300pF
- SOURCE CURRENT. 4mA
- SINK CURRENT 6mA
- PROPAGATION DELAY . . . . . 65nsec @ 5V

Pinout

TOP VIEW



Description

The HD-6431 is a self-aligned silicon gate CMOS Latching Three-State Bus Driver. This circuit consists of 6 non-inverting latching drivers with separate input and output. A high on the strobe line L allows data to go through the latches and a transition to low latches the data. A high on the Three-State control $\overline{E}$ forces the buffers to the high impedance mode without disturbing the latched data. New data may be latched in while the buffers are in the high impedance mode.

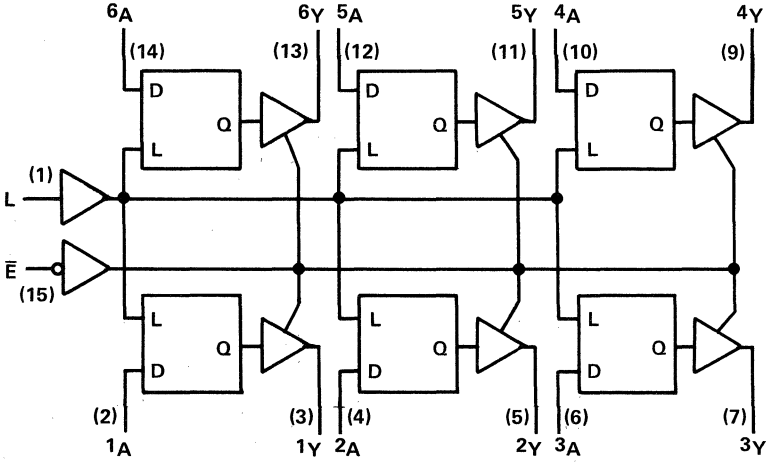
Outputs guaranteed valid at VCC 2.0V for Battery Backup Applications.

Truth Table

CONTROL INPUTS		DATA PORT STATUS	
$\overline{E}$	L	A	Y
H	L	X	HI-Z*
H	H	X	HI-Z
L	↓	X	*
L	H	L	L
L	H	H	H

* Data is latched to the value of the last input
X = Don't Care
HI-Z = High Impedance
↓ = Transition from High to Low level

Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+12.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6431A-9	-40°C to +85°C
Military HD-6431A-2	-55°C to +125°C
Operating Voltage Range	+4 to +11V

ELECTRICAL CHARACTERISTICS

V_{CC} = 10V ± 10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-10	10	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} -0.4		V	I_{OH} = -8.0mA, $\overline{E}$ = Low
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 12mA $\overline{E}$ = Low
I_O	Output Leakage	-10	10	μA	$0V \leq V_O \leq V_{CC}$, $\overline{E}$ = High
I_{CC}	Supply Current		100	μA	$V_{IN} = V_{CC}$ or GND, V_{CC} = 11V
C_{IN}	Input Capacitance*		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
C_O	Output Capacitance*		15	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

* Guaranteed and sampled, but not 100% tested.

C_L = 300pF

A.C.

		V_{CC} = 10.0V ① 25°C		V_{CC} = 10.0V ± 10% T_A = Indust. or Mil.		
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
t_{PD}	Propagation Delay		35		45	ns
t_{EN}	Enable Time		35		45	ns
t_{DIS}	Disable Time		35		45	ns
t_{SET}	Input Set Up Time	10		10		ns
t_{HOLD}	Input Hold Time	10		10		ns
t_{PW}	Pulse Width	15		20		ns
t_R	Output Rise Time		30		40	ns
t_F	Output Fall Time		20		30	ns

NOTE ① All devices guaranteed at worst case limits. Room temperature, 10V data provided for information-not guaranteed.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6431-9	-40°C to +85°C
Military HD-6431-2	-55°C to +125°C
Operating Voltage Range	+4 to +7V

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-1.0	1.0	µA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} -0.4		V	I_{OH} = -4.0mA, $\overline{E}$ = Low
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 6.0mA $\overline{E}$ = Low
I_O	Output Leakage	-1.0	1.0	µA	$0V \leq V_O \leq V_{CC}$, $\overline{E}$ = High
I_{CC}	Supply Current		10	µA	V_{IN} = V_{CC} or GND, V_{CC} = 5.5V
C_{IN}	Input Capacitance*		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
C_O	Output Capacitance*		15	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

* Guaranteed and sampled, but not 100% tested.

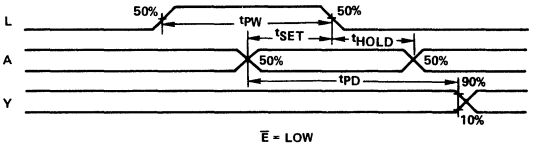
C_L = 300pF

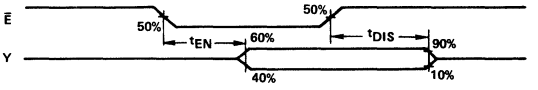
A.C.

		V_{CC} = 5.0V ① 25°C		V_{CC} = 5.0V ± 10% T_A = Indus. or Mil.		
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
t_{PD}	Propagation Delay		65		75	ns
t_{EN}	Enable Time		80		90	ns
t_{DIS}	Disable Time		80		90	ns
t_{SET}	Input Setup Time	15		15		ns
t_{HOLD}	Input Hold Time	15		15		ns
t_{PW}	Pulse Width	25		30		ns
t_R	Output Rise Time		80		90	ns
t_F	Output Fall Time		70		80	ns

NOTE ① All devices guaranteed at worst case limits. Room temperature, 5V data provided for information-not guaranteed.

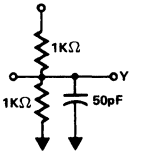
Switching Waveforms





All inputs have t_R, $t_F \leq$ 20ns.

OUTPUT TEST CIRCUIT
FOR PROPAGATION DELAYS



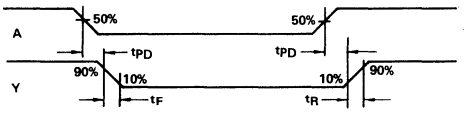
OUTPUT TEST CIRCUIT
FOR THREE-STATE DELAYS

DECOUPLING CAPACITORS

The transient current required to charge the load capacitance is given by $I_T = C\frac{dv}{dt}$. Assuming that all outputs may change state at the same time and that $\frac{dv}{dt}$ is constant; $I_T = \left(\Sigma C_L\right)\left(\frac{V_{CC} \times 80\%}{t_R \text{ or } t_F}\right)$ eg. $\left[t_R = 80ns, V_{CC} = 5.0V, \text{each } C_L = 300pF, I_T = (4)\left(300 \times 10^{-12}\right)\frac{5.0 \times 0.8}{80 \times 10^{-9}} = 90mA.\right]$ This current spike may cause a large negative voltage spike on V_{CC}, which if it becomes a diode drop less than any input, may cause the device to latch up. It is recommended that a 0.1 μF ceramic disk decoupling capacitor be placed between V_{CC} and GND at each device to filter out this noise.

4

PROPAGATION DELAYS



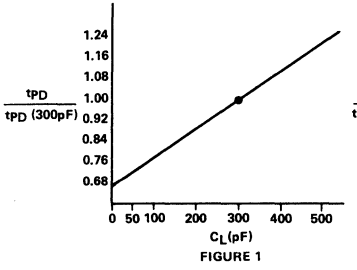


FIGURE 1

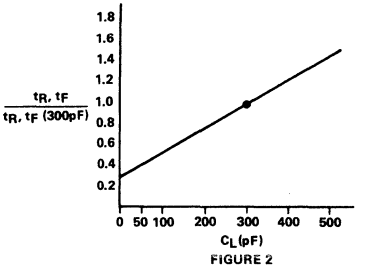


FIGURE 2

The above example will illustrate the calculation of a more useful propagation delay. The system on this example uses a 5 volt supply with a tolerance of ± 10%, an ambient temperature of as high as 125°C, and a calculated load capacitance of 150pF. This application requires the HD-6431-2. The table of A.C. specs shows the t_{PD} at 4.5V and 125°C is 75nsec. Use the graph in Figure 1 to get the degradation multiple for 150pF. The number shown is 0.84. The adjusted propagation delay, to the 10% or 90% point, is therefore 75 x 0.84 or 63nsec. To obtain the rise and fall times check the A.C. specs for the rise and fall times at 4.5V and 125°C to obtain a worst case rise time of 90nsec. Use Figure 2 to find it's degradation multiple to be 0.65. The adjusted rise time is, therefore, 90 x 0.65 or 58nsec. To obtain the standard 50% to 50% propagation delay, add the adjusted propagation delay to half of the adjusted rise time to get a propagation delay of 92nsec. The rise time was used here because it is always the worst case.

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HD-6432

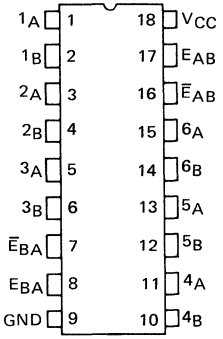
CMOS HEX BI-DIRECTIONAL BUS DRIVER

Features

- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY. 300pF
- SOURCE CURRENT. 4mA
- SINK CURRENT 6mA
- PROPAGATION DELAY . . . . . 45nsec @ 5V

Pinout

TOP VIEW



Description

The HD-6432 is a self-aligned silicon gate CMOS bi-directional bus driver. This circuit consists of 12 drivers organized as 6 bi-directional pairs. Four enable lines select drive direction or Three-State mode.

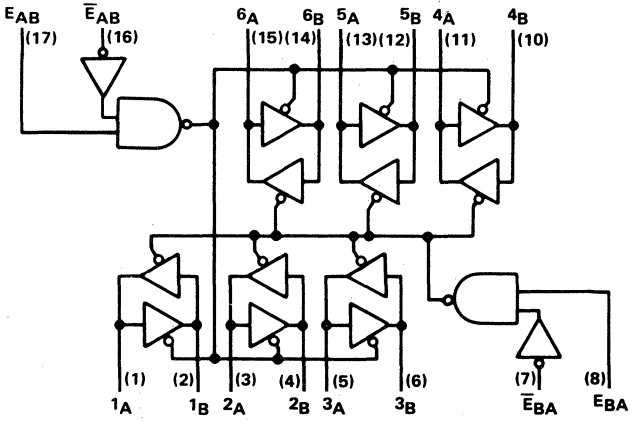
Outputs guaranteed valid at VCC 2.0V for Battery Backup Applications.

Truth Table

CONTROL INPUTS				DATA PORT STATUS	
E_{AB}	$\overline{E}_{AB}$	E_{BA}	$\overline{E}_{BA}$	A	B
L	X	H	L	O	I
X	H	H	L	O	I
H	L	X	H	I	O
H	L	L	X	I	O
L	X	L	X	ISOLATED	
X	H	X	H	ISOLATED	
L	X	X	H	ISOLATED	
X	H	L	X	ISOLATED	
H	L	H	L	NOT ALLOWED	

I = Input, O = Output, X = Don't Care

Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+12.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6432A-9	-40°C to +85°C
Military HD-6432A-2	-55°C to +125°C
Operating Voltage Range	+4 to +11V

ELECTRICAL CHARACTERISTICS

V_{CC} = 10V ±10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-10	10	µA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} -0.4		V	I_{OH} = -8.0mA,
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 12mA
I_O	Output Leakage	-10	10	µA	$0V \leq V_O \leq V_{CC}$, $E_{AB} = E_{BA}$ = Low
I_{CC}	Supply Current		100	µA	$V_{IN} = V_{CC}$ or GND, V_{CC} = 11V
C_{IN}	Input Capacitance*		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
$C_{I/O}$	I/O Capacitance*		20	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

* Guaranteed and sampled, but not 100% tested.

C_L = 300pF

A.C.

		V_{CC} = 10.0V ① 25°C		V_{CC} = 10.0V ±10% T_A = Indust. or Mil.		
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
t_{PD}	Propagation Delay		35		45	ns
t_{EN}	Enable Time		40		50	ns
t_{DIS}	Disable Time		75		85	ns
t_R	Output Rise Time		40		50	ns
t_F	Output Fall Time		35		45	ns

NOTE ①: All devices guaranteed at worst case limits. Room temperature, 10V data provided for information–not guaranteed.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6432-9	-40°C to +85°C
Military HD-6432-2	-55°C to +125°C
Operating Voltage Range	+4 to +7V

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-1.0	1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} -0.4		V	I_{OH} = -4.0mA
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 6.0mA
I_O	Output Leakage	-1.0	1.0	μA	$0V \leq V_O \leq V_{CC}$, $E_{AB} = E_{BA}$ = Low
I_{CC}	Supply Current		10	μA	$V_{IN} = V_{CC}$ or GND, V_{CC} = 5.5V
C_{IN}	Input Capacitance*		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
$C_{I/O}$	I/O Capacitance*		20	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

* Guaranteed and sampled, but not 100% tested.

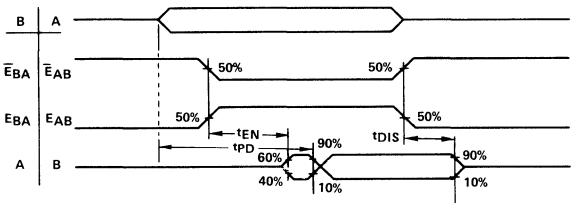
C_L = 300pF

A.C.

		V_{CC} = 5.0V ① 25°C		V_{CC} = 5.0V ± 10% T_A = Indus. or Mil.		
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
t_{PD}	Propagation Delay		45		55	ns
t_{EN}	Enable Time		65		75	ns
t_{DIS}	Disable Time		100		110	ns
t_R	Output Rise Time		100		110	ns
t_F	Output Fall Time		70		80	ns

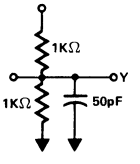
NOTE ①: All devices guaranteed at worst case limits. Room temperature, 5V data provided for information-not guaranteed.

Switching Waveforms



All inputs have t_R, $t_F \leq 20$ns.

OUTPUT TEST CIRCUIT
FOR PROPAGATION DELAYS



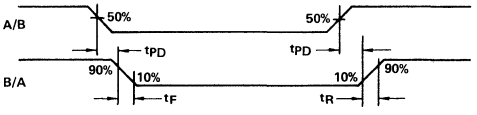
OUTPUT TEST CIRCUIT
FOR THREE-STATE DELAYS

DECOUPLING CAPACITORS

The Transient current required to charge the load capacitance is given by $I_T = C \frac{dv}{dt}$. Assuming that all outputs may change state at the same time and that $\frac{dv}{dt}$ is constant; $I_T = (\Sigma C_L)\left(\frac{V_{CC} \times 80\%}{t_R \text{ or } t_F}\right)$ eg. $\left[t_R = 100\text{ns} \quad V_{CC} = 5.0\text{V} \quad \text{each } C_L = 300\text{pF} \quad I_T = (6)\ (300 \times 10^{-12})\frac{5.0 \times 0.8}{100 \times 10^{-9}} = 72\text{mA.}\right]$ This current spike may cause a large negative voltage spike on V_{CC}, which if it becomes a diode drop less than any input, may cause the device to latch up. It is recommended that a 0.1 μF ceramic disk decoupling capacitor be placed between V_{CC} and GND at each device to filter out this noise.

4

PROPAGATION DELAYS



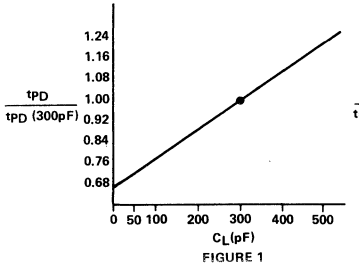


FIGURE 1

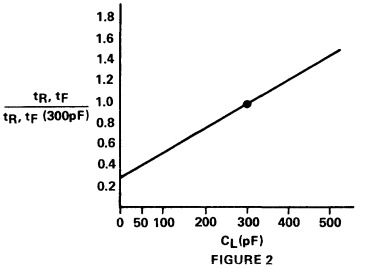


FIGURE 2

The above example will illustrate the calculation of a more useful propagation delay. The system on this example uses a 5 volt supply with a tolerance of ± 10%, an ambient temperature of as high as 125°C, and a calculated load capacitance of 150pF. This application requires the HD-6432-2. The table of A.C. specs shows the t_{PD} at 4.5V and 125°C is 55nsec. Use the graph in Figure 1 to get the degradation multiple for 150pF. The number shown is 0.84. The adjusted propagation delay, to the 10% or 90% point, is therefore 55 x 0.84 or 46nsec. To obtain the rise and fall times check the A.C. specs for the rise and fall times at 4.5V and 125°C to obtain a worst case rise time of 110nsec. Use Figure 2 to find it's degradation multiple to be 0.65. The adjusted rise time is, therefore, 110 x 0.65 or 72nsec. To obtain the standard 50% to 50% propagation delay, add the adjusted propagation delay to half of the adjusted rise time to get a propagation delay of 82nsec. The rise time was used here because it is always the worst case.

HD-6433

CMOS QUAD BUS SEPARATOR/DRIVER

Features

- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY. 300pF
- SOURCE CURRENT. 4mA
- SINK CURRENT 6mA
- PROPAGATION DELAY . . . . . 40nsec @ 5V

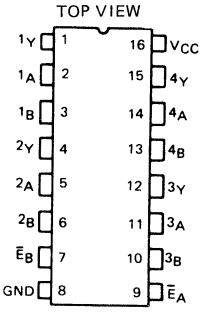
Description

The HD-6433 is a self-aligned silicon gate CMOS bus separator/driver. This circuit consists of 8 drivers organized as 4 pairs of bus separators which allow a unidirectional input bus and a unidirectional output bus to be interfaced with a bi-directional bus.

Outputs guaranteed valid at VCC 2.0V for Battery Backup Applications.

Pinout

TOP VIEW

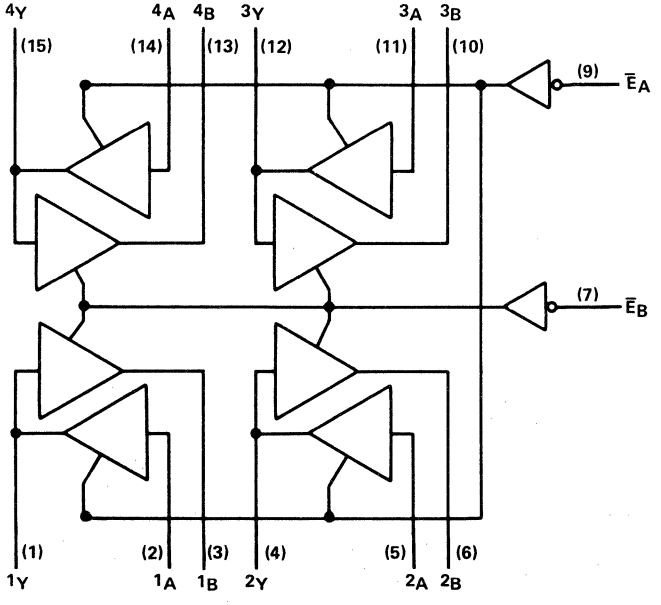


Truth Table

CONTROL INPUTS		FUNCTION		
$\bar{E}_A$	$\bar{E}_B$	A	B	Y
L	L	I	O	O
L	H	I	D	O
H	L	D	O	I
H	H	ISOLATED		

I = Input, O = Output,
D = Disconnected

Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+12.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6433A-9	-40°C to +85°C
Military HD-6433A-2	-55°C to +125°C
Operating Voltage Range	+4 to +11V

ELECTRICAL CHARACTERISTICS

V_{CC} = 10V ±10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-10	10	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} -0.4		V	I_{OH} = -8.0mA
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 12mA
I_O	Output Leakage	-10	10	μA	$0V \leq V_O \leq V_{CC}$, $\overline{E}_A = \overline{E}_B$ = High
I_{CC}	Supply Current		100	μA	$V_{IN} = V_{CC}$ or GND, V_{CC} = 11V
C_{IN}	Input Capacitance*		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
$C_{I/O}$	I/O Capacitance *		20	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
C_O	Output Capacitance*		15	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

* Guaranteed and sampled, but not 100% tested.

C_L = 300pF

A.C.

		V_{CC} = 10.0V ① 25°C		V_{CC} = 10.0V ±10% T_A = Indust. or Mil.		
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
t_{PD}	Propagation Delay		20		30	ns
t_{EN}	Enable Time		45		55	ns
t_{DIS}	Disable Time		45		55	ns
t_R	Output Rise Time		65		75	ns
t_F	Output Fall Time		55		65	ns

NOTE ① All devices guaranteed at worst case limits. Room temperature, 10V data provided for information-not guaranteed.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6433-9	-40°C to +85°C
Military HD-6433-2	-55°C to +125°C
Operating Voltage Range	+4 to +7V

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-1.0	1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} -0.4		V	I_{OH} = -4.0mA
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 6.0mA
I_O	Output Leakage	-1.0	1.0	μA	$0V \leq V_O \leq V_{CC}$ $\overline{E}_A = \overline{E}_B$ = High
I_{CC}	Supply Current		10	μA	$V_{IN} = V_{CC}$ or GND, V_{CC} = 5.5V
C_{IN}	Input Capacitance*		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
$C_{I/O}$	I/O Capacitance*		20	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
C_O	Output Capacitance*		15	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

* Guaranteed and sampled, but not 100% tested.

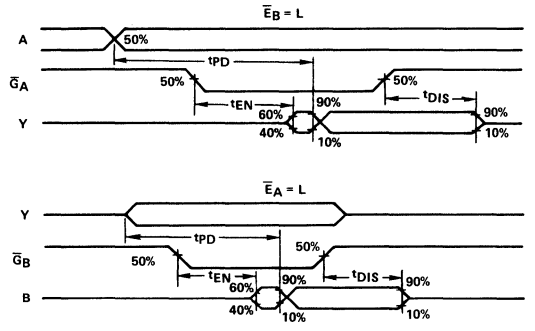
C_L = 300pF

A.C.

		V_{CC} = 5.0V ① 25°C		V_{CC} = 5.0V ± 10% TA = Indust. or Mil.		
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
t_{PD}	Propagation Delay		40		50	ns
t_{EN}	Enable Time		60		70	ns
t_{DIS}	Disable Time		90		100	ns
t_R	Output Rise Time		85		95	ns
t_F	Output Fall Time		70		80	ns

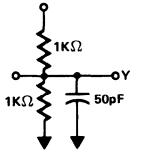
NOTE ① All devices guaranteed at worst case limits. Room temperature, 5V data provided for information-not guaranteed.

Switching Waveforms



All inputs have t_R, $t_F \leq$ 20ns.

OUTPUT TEST CIRCUIT
FOR PROPAGATION DELAYS



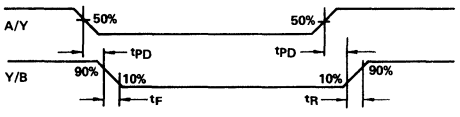
OUTPUT TEST CIRCUIT
FOR THREE-STATE DELAYS

DECOUPLING CAPACITORS

The transient current required to charge the load capacitance is given by $I_T = C\frac{dv}{dt}$. Assuming that all outputs may change state at the same time and that $\frac{dv}{dt}$ is constant; $I_T = \left(\Sigma C_L\right)\left(\frac{V_{CC} \times 80\%}{t_R \text{ or } t_F}\right)$ eg. $\left[t_R = 85\text{ns}, V_{CC} = 5.0\text{V}, \text{each } C_L = 300\text{pF}, I_T = (4)\left(300 \times 10^{-12}\right)\frac{5.0 \times 0.8}{85 \times 10^{-9}} = 56.5\text{mA}.\right]$ This current spike may cause a large negative voltage spike on V_{CC}, which if it becomes a diode drop less than any input, may cause the device to latch up. It is recommended that a 0.1 μF ceramic disk decoupling capacitor be placed between V_{CC} and GND at each device to filter out this noise.

4

PROPAGATION DELAYS



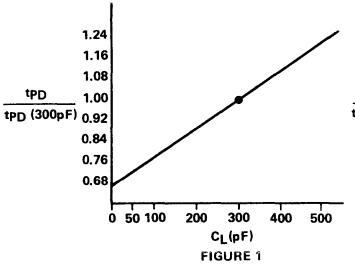


FIGURE 1

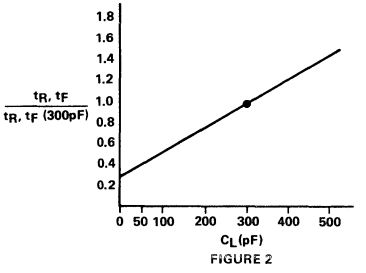


FIGURE 2

The above example will illustrate the calculation of a more useful propagation delay. The system on this example uses a 5 volt supply with a tolerance of ± 10%, an ambient temperature of as high as 125°C, and a calculated load capacitance of 150pF. This application requires the HD-6433-2. The table of A.C. specs shows the t_{PD} at 4.5V and 125°C is 50nsec. Use the graph in Figure 1 to get the degradation multiple for 150pF. The number shown is 0.84. The adjusted propagation delay, to the 10% or 90% point, is therefore 50 x 0.84 or 42nsec. To obtain the rise and fall times check the A.C. specs for the rise and fall times at 4.5V and 125°C to obtain a worst case rise time of 95nsec. Use Figure 2 to find it's degradation multiple to be 0.65. The adjusted rise time is, therefore, 95 x 0.65 or 62nsec. To obtain the standard 50% to 50% propagation delay, add the adjusted propagation delay to half of the adjusted rise time to get a propagation delay of 73nsec. The rise time was used here because it is always the worst case.

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HD-6434

CMOS OCTAL RESETTABLE LATCHED BUS DRIVER

Advance Information

Features

- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY 300pF
- SOURCE CURRENT 6mA
- SINK CURRENT 9mA
- PROPAGATION DELAY . . . . . 45nsec @ 5V

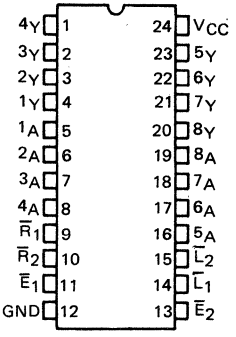
Description

The HD-6434 is a self-aligned silicon gate CMOS latching Three State bus driver. This circuit consists of 8 non-inverting latching drivers with separate input and output. A low on both strobe lines ($\overline{L}$) allows data to go through the latches and a transition to high latches the data. A high on either Three State control ($\overline{E}$) forces the buffers to the high impedance mode without disturbing the latched data. A low on either reset line ($\overline{R}$) forces each of the latches to a low level. New data may be latched in while the buffers are in the high impedance mode.

Outputs guaranteed valid at VCC 2.0V for Battery Backup Applications.

Pinout

TOP VIEW

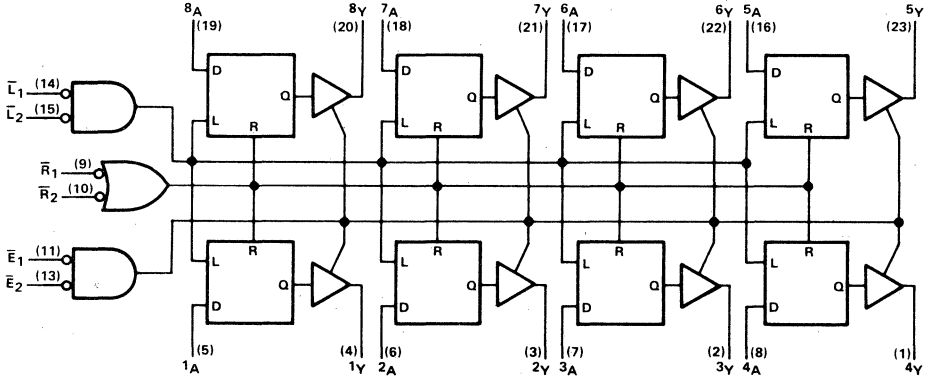


Truth Table

CONTROL INPUTS						DATA	
$\overline{R}_1$	$\overline{R}_2$	$\overline{E}_1$	$\overline{E}_2$	$\overline{L}_1$	$\overline{L}_2$	A	Y
X	X	H	X	X	X	X	Hi-Z
X	X	X	H	X	X	X	Hi-Z
L	X	L	L	X	X	X	L
X	L	L	L	X	X	X	L
H	H	L	L	L	L	L	L
H	H	L	L	L	L	H	H
H	H	L	L	↑	L	X	*
H	H	L	L	L	↑	X	*

X = Don't Care Hi-Z = High Impedance L = Low
H = High * = Data is latched to the valve of the last input
↑ = Transition from a Low to High level

Functional Diagram



4

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6434-9	-40°C to +85°C
Military HD-6434-2	-55°C to +125°C
Operating Voltage Range	+4V to +7V

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-1.0	1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} -0.4		V	I_{OH} = -6.0mA, $\overline{E}_1 = \overline{E}_2$ = Low
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 9.0mA $\overline{E}_1 = \overline{E}_2$ = Low
I_O	Output Leakage	-10	10	μA	$0V \leq V_O \leq V_{CC}$, $\overline{E}_1 = \overline{E}_2$ = High
I_{CC}	Supply Current		10	μA	$V_{IN} = V_{CC}$ or GND, V_{CC} = 5.5V
C_{IN}	Input Capacitance*		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
C_O	Output Capacitance*		15	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

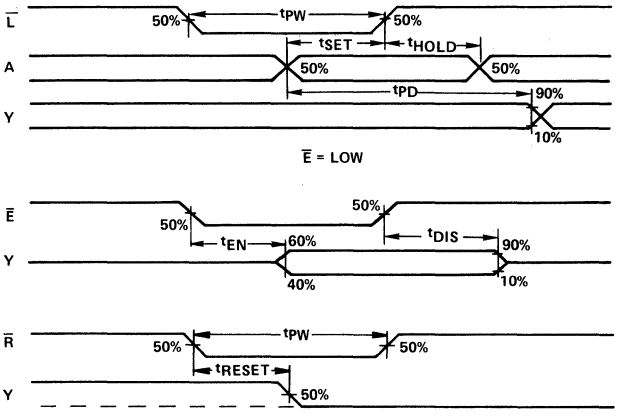
* Guaranteed and sampled, but not 100% tested.

A.C.

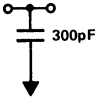
C_L = 300pF

SYMBOL	PARAMETER	V_{CC} = 5.0V TEMP. = 25°C MIN	MAX	UNITS
t_{PD}	Propagation Delay		45	ns
t_{EN}	Enable Time		40	ns
t_{DIS}	Disable Time		40	ns
t_{SET}	Input Setup Time	25		ns
t_{HOLD}	Input Hold Time	25		ns
t_{PW}	Pulse Width	50		ns
t_R	Output Rise Time		40	ns
t_F	Output Fall Time		35	ns
t_{RESET}	Reset Delay Time		40	ns

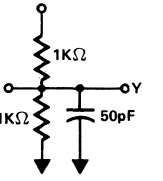
Switching Waveforms



All inputs have t_R, $t_F \leq$ 20ns.



OUTPUT TEST CIRCUIT
FOR PROPAGATION DELAYS



OUTPUT TEST CIRCUIT
FOR THREE-STATE DELAYS

4

DECOUPLING CAPACITORS

The instantaneous current required to switch a large capacitance load may cause a voltage spike on V_{CC}, which if it becomes a diode drop less than any input, may cause the device to latch up. It is recommended that a 0.1μF ceramic disk decoupling capacitor be placed between V_{CC} and GND at each device to filter out this noise.

PROPAGATION DELAYS

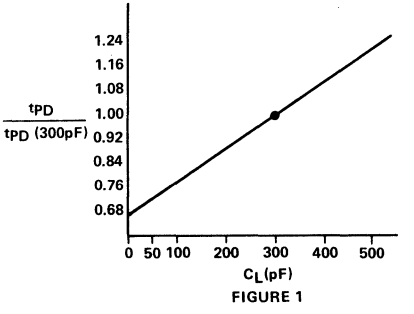


FIGURE 1

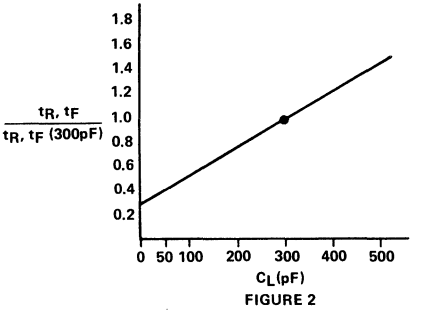


FIGURE 2

TYPICAL CURVES

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HD-6435

CMOS HEX RESETTABLE LATCHED BUS DRIVER

Advance Information

Features

- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY 300pF
- SOURCE CURRENT 6mA
- SINK CURRENT 9mA
- PROPAGATION DELAY . . . . . 45nsec @ 5V

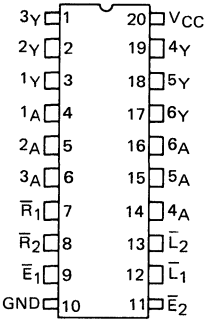
Description

The HD-6435 is a self-aligned silicon gate CMOS latching Three State bus driver. This circuit consists of 6 non-inverting latching drivers with separate input and output. A low on both strobe lines ($\overline{L}$) allows data to go through the latches and a transition to high latches the data. A high on either Three State control ($\overline{E}$) forces the buffers to the high impedance mode without disturbing the latched data. A low on either reset line ($\overline{R}$) forces each of the latches to a low level. New data may be latched in while the buffers are in the high impedance mode.

Outputs guaranteed valid at VCC 2.0V for Battery Backup Applications.

Pinout

TOP VIEW

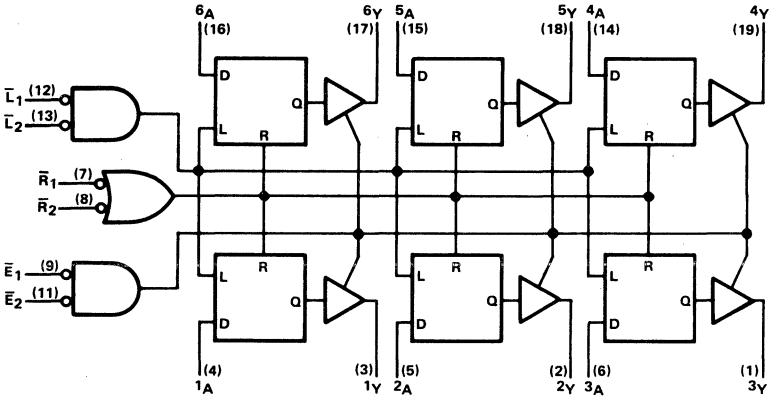


Truth Table

CONTROL INPUTS						DATA	
$\overline{R}_1$	$\overline{R}_2$	$\overline{E}_1$	$\overline{E}_2$	$\overline{L}_1$	$\overline{L}_2$	A	Y
X	X	H	X	X	X	X	Hi-Z
X	X	X	H	X	X	X	Hi-Z
L	X	L	L	X	X	X	L
X	L	L	L	X	X	X	L
H	H	L	L	L	L	L	L
H	H	L	L	L	L	H	H
H	H	L	L	↑	L	X	*
H	H	L	L	L	↑	X	*

X = Don't Care Hi-Z = High Impedance L = Low
H = High * = Data is latched to the valve of the last input
↑ = Transition from a Low to High level

Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6435-9	-40°C to +85°C
Military HD-6435-2	-55°C to +125°C
Operating Voltage Range	+4V to +7V

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-1.0	1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} -0.4		V	I_{OH} = -6.0mA, $\overline{E}_1 = \overline{E}_2$ = Low
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 9.0mA $\overline{E}_1 = \overline{E}_2$ = Low
I_O	Output Leakage	-10	10	μA	$0V \leq V_O \leq V_{CC}$, $\overline{E}_1 = \overline{E}_2$ = High
I_{CC}	Supply Current		10	μA	$V_{IN} = V_{CC}$ or GND, V_{CC} = 5.5V
C_{IN}	Input Capacitance*		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
C_O	Output Capacitance*		15	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

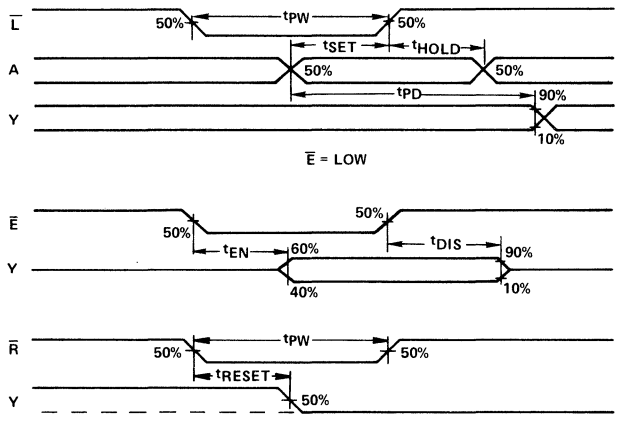
* Guaranteed and sampled, but not 100% tested.

A.C.

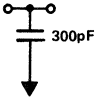
C_L = 300pF

		V_{CC} = 5.0V TEMP. = 25°C		
SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{PD}	Propagation Delay		45	ns
t_{EN}	Enable Time		40	ns
t_{DIS}	Disable Time		40	ns
t_{SET}	Input Setup Time	25		ns
t_{HOLD}	Input Hold Time	25		ns
t_{PW}	Pulse Width	50		ns
t_R	Output Rise Time		40	ns
t_F	Output Fall Time		35	ns
t_{RESET}	Reset Delay Time		40	ns

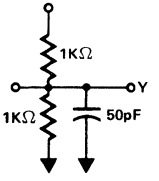
Switching Waveforms



All inputs have t_R, $t_F \leq 20$ns.



OUTPUT TEST CIRCUIT
FOR PROPAGATION DELAYS



OUTPUT TEST CIRCUIT
FOR THREE-STATE DELAYS

4

DECOUPLING CAPACITORS

The instantaneous current required to switch a large capacitance load may cause a voltage spike on V_{CC}, which if it becomes a diode drop less than any input, may cause the device to latch up. It is recommended that a 0.1μF ceramic disk decoupling capacitor be placed between V_{CC} and GND at each device to filter out this noise.

PROPAGATION DELAYS

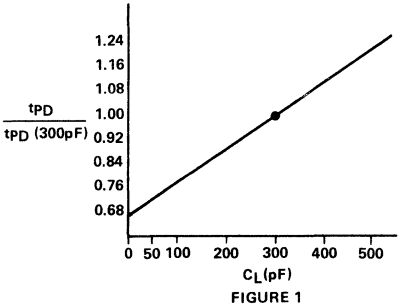


FIGURE 1

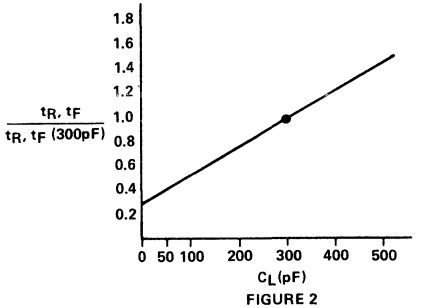


FIGURE 2

TYPICAL CURVES

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HD-6436

CMOS OCTAL BUS BUFFER/DRIVER

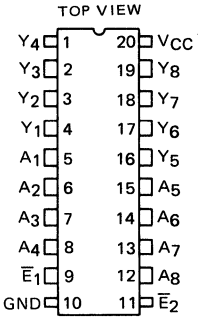
Advance Information

Features

- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY 300pF
- SOURCE CURRENT 6mA
- SINK CURRENT 9mA
- PROPAGATION DELAY . . . . . 45nsec @ 5V

Pinout

TOP VIEW



Description

The HD-6436 is a self-aligned silicon gate CMOS Three State buffer driver. The circuit consists of 8 non-inverting buffers with separate inputs and outputs which permit this driver to be used for bi-directional or uni-directional busing. A high on either Three State control line $\overline{E}_1$ or $\overline{E}_2$ will force the drivers to the high impedance mode.

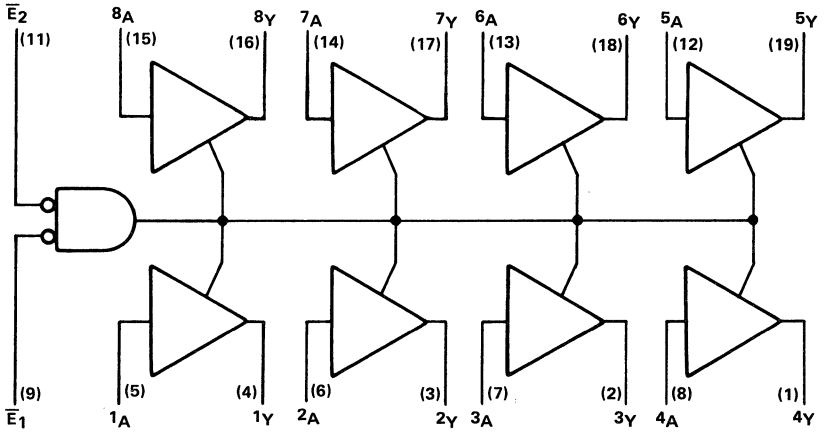
Outputs guaranteed valid at VCC 2.0V for Battery Backup Applications.

Truth Table

CONTROL INPUTS		INPUT	OUTPUT
$\overline{E}_1$	$\overline{E}_2$	A	Y
L	L	L	L
L	L	H	H
L	H	X	Hi-Z
H	L	X	Hi-Z
H	H	X	Hi-Z

L = Low, H = High
X = Don't Care
Hi-Z = High Impedance

Functional Diagram



4

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6436-9	-40°C to +85°C
Military HD-6436-2	-55°C to +125°C
Operating Voltage Range	+4V to +7V

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-1.0	1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} -0.4		V	I_{OH} = -6.0mA, $\overline{E}_1 = \overline{E}_2$ = Low
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 9.0mA $\overline{E}_1 = \overline{E}_2$ = Low
I_O	Output Leakage	-10	10	μA	$0V \leq V_O \leq V_{CC}$, $\overline{E}_1 = \overline{E}_2$ = High
I_{CC}	Supply Current		10	μA	$V_{IN} = V_{CC}$ or GND, V_{CC} = 5.5V
C_{IN}	Input Capacitance*		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
C_O	Output Capacitance*		15	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

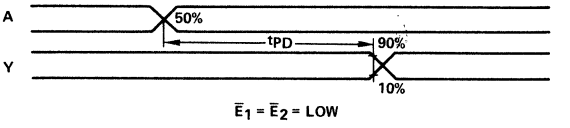
* Guaranteed and sampled, but not 100% tested.

A.C.

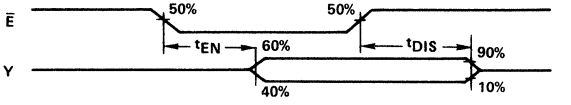
C_L = 300pF

SYMBOL	PARAMETER	V_{CC} = 5.0V TEMP. = 25°C MAX	UNITS
t_{PD}	Propagation Delay	45	ns
t_{EN}	Enable Time	40	ns
t_{DIS}	Disable Time	40	ns
t_R	Output Rise Time	40	ns
t_F	Output Fall Time	35	ns

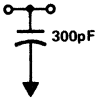
Switching Waveforms



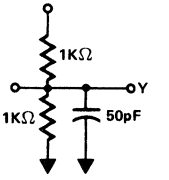
$\overline{E}_1 = \overline{E}_2$ = LOW



All inputs have t_R, $t_F \leq 20$ns.



OUTPUT TEST CIRCUIT
FOR PROPAGATION DELAYS



OUTPUT TEST CIRCUIT
FOR THREE-STATE DELAYS

4

DECOUPLING CAPACITORS

The instantaneous current required to switch a large capacitance load may cause a voltage spike on V_{CC}, which if it becomes a diode drop less than any input, may cause the device to latch up. It is recommended that a 0.1μF ceramic disk decoupling capacitor be placed between V_{CC} and GND at each device to filter out this noise.

PROPAGATION DELAYS

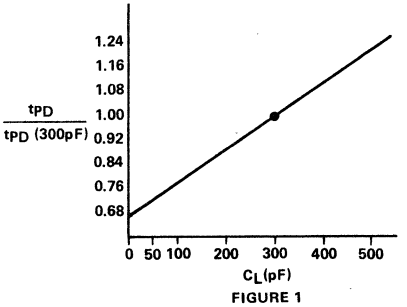


FIGURE 1

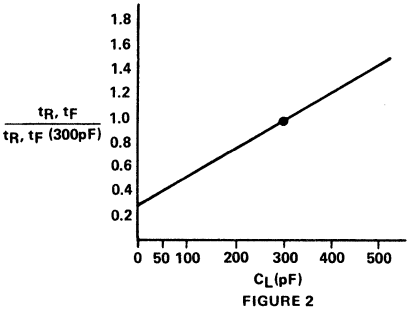


FIGURE 2

TYPICAL CURVES

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HD-6440

CMOS LATCHED 3 TO 8 LINE DECODER-DRIVER

Features

- HIGH SPEED DECODING FOR MEMORY ARRAYS
- INCORPORATES 3 ENABLE INPUTS TO SIMPLIFY EXPANSION
- LOW POWER . . . . . TYPICALLY<50 μ W @ 5V STANBDY
- HIGH NOISE IMMUNITY
- AVAILABLE IN BOTH MILITARY AND INDUSTRIAL TEMPERATURE RANGE
- HIGH CAPACITANCE DRIVE 200pF
- HIGH OUTPUT DRIVE . . . . . I_{OH} = -2mA, I_{OL} = 2.4mA
- SINGLE POWER SUPPLY

Description

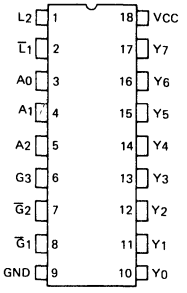
The HD-6440 is a self aligned silicon gate latched decoder. One of 8 output lines is decoded, and brought to a low state, from the 3 input lines. There are two latch enables ($\overline{L_1}$, L_2), one complemented and one not, to eliminate the need for external gates. The output is enabled by three different output enables ($\overline{G_1}$, $\overline{G_2}$, G_3), two of them complemented and one not. Each output remains in a high state until it is selected, at which time it will go low.

When using high speed CMOS memories, the delay time of the HD-6440 and the enable time of the memory is usually less than the access time of the memory. This assures that memory access time will not be lengthened by the use of the HD-6440 latched decoder driver. The latch is useful for memory mapping or for systems which use a multiplexed bus.

Outputs guaranteed valid at VCC 2.0V for Battery Backup Applications.

Pinout

TOP VIEW



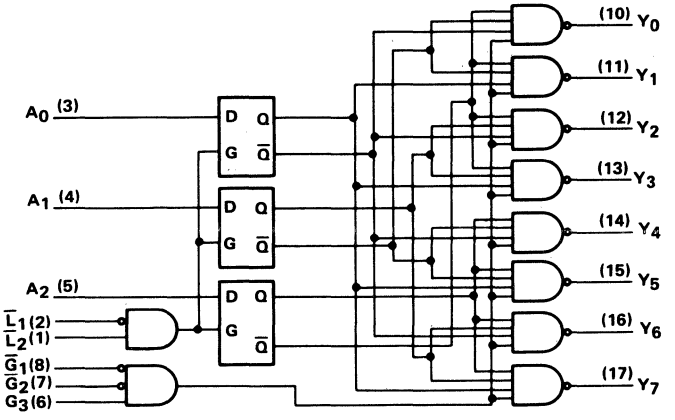
Truth Table

INPUTS				OUTPUTS								
ENABLE			ADDRESS									
$\overline{G_1}$	$\overline{G_2}$	G_3	$\overline{L_1}$ L_2	A_2	A_1	A_0	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	FUNCTION
X	X	L	X X	X	X	X	H	H	H	H	H	H	H	H	DISABLE
X	H	X	X X	X	X	X	H	H	H	H	H	H	H	H	
H	X	X	X X	X	X	X	H	H	H	H	H	H	H	H	
L	L	H	L H	L	L	L	L	H	H	H	H	H	H	H	DECODE
L	L	H	L H	L	L	H	H	L	H	H	H	H	H	H	
L	L	H	L H	L	H	L	H	H	L	H	H	H	H	H	
L	L	H	L H	L	H	H	H	H	H	L	H	H	H	H	
L	L	H	L H	H	L	L	H	H	H	H	L	H	H	H	
L	L	H	L H	H	L	H	H	H	H	H	H	L	H	H	
L	L	H	L H	H	H	L	H	H	H	H	H	H	L	H	
L	L	H	L H	H	H	H	H	H	H	H	H	H	H	L	
L	L	H	X L	X	X	X	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	LATCHED
L	L	H	H X	X	X	X	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	

L = Low, H = High, X = Don't Care

Y_n = Data is latched to the valve of the last input

Functional Diagram



4

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	12.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6440A-9	-40°C to +85°C
Military HD-6440A-2	-55°C to +125°C
Operating Voltage Range	+4 to +11V

ELECTRICAL CHARACTERISTICS

V_{CC} = 10V ± 10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-10	10	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} - 0.4		V	I_{OH} = -5.0mA
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 5.0mA
I_{CC}	Supply Current		100	μA	V_{CC} = 11V
C_{IN}	Input Capacitance*		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
C_O	Output Capacitance*		15	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

* Guaranteed and sampled, but not 100% tested..

A.C.

C_L = 200pF

		V_{CC} = 10.0V ① 25°C		V_{CC} = 10.0V ± 10% T_A = Indus. or Mil.		
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
t_{SET}	Input Setup Time	15		15		ns
t_{HOLD}	Input Hold Time	15		15		ns
t_{PD}	Propagation Delay		40		60	ns
t_{EN}	Enable Time		35		50	ns
t_{DIS}	Disable Time		35		50	ns
t_{PW}	Pulse Width	15		25		ns
t_R	Output Rise Time		45		60	ns
t_F	Output Fall Time		45		60	ns

NOTE:

① All devices guaranteed at worse case limits. Room temperature, 10V data provided for information - not guaranteed.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6440A-9	-40°C to +85°C
Military HD-6440A-2	-55°C to +125°C
Operating Voltage Range	+4 to +7V

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-1.0	1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} - 0.4		V	I_{OH} = -2.4mA
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 2.4mA
I_{CC}	Supply Current		10	μA	V_{CC} = 5.5V
C_{IN}	Input Capacitance*		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
C_O	Output Capacitance*		15	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

*Guaranteed and sampled, but not 100% tested.

4

CL = 200pF

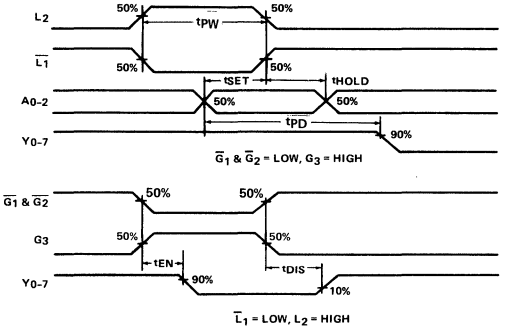
A.C.

		V_{CC} = 5.0V ① 25°C		V_{CC} = 5.0V ± 10% T_A = Indust. or Mil.		
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
t_{SET}	Input Setup Time	20		20		ns
t_{HOLD}	Input Hold Time	20		20		ns
t_{PD}	Propagation Delay		65		100	ns
t_{EN}	Enable Time		50		80	ns
t_{DIS}	Disable Time		50		90	ns
t_{PW}	Pulse Width	30		30		ns
t_R	Output Rise Time		60		90	ns
t_F	Output Fall Time		50		80	ns

NOTE:

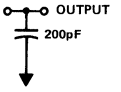
① All devices guaranteed at worse case limits. Room temperature, 10V data provided for information - not guaranteed.

Switching Waveforms



All Inputs have t_R, $t_F \leq 20$ns

OUTPUT TEST CIRCUIT FOR PROPAGATION DELAYS

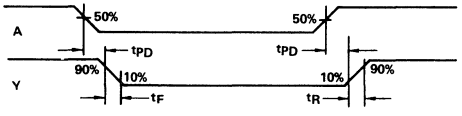


DECOUPLING CAPACITORS

The Transient current required to charge the load capacitance is given by $I_T = C\frac{dv}{dt}$. Assuming that all outputs may change state at the same time and that $\frac{dv}{dt}$ is constant; $I_T = \left(\Sigma C_L\right)\left(\frac{V_{CC} \times 80\%}{t_R \text{ or } t_F}\right)$ eg. [t_R = 60ns, V_{CC} = 5.0V, each C_L = 200pF, $I_T = (2)(200 \times 10^{-12})\frac{5.0 \times 0.8}{60 \times 10^{-9}} = 26.7$mA.] This current spike may cause a large negative voltage spike on V_{CC}, which if it becomes a diode drop less than any input, may cause the device to latch up. It is recommended that a 0.1μF ceramic disk decoupling capacitor be placed between V_{CC} and GND at each device to filter out this noise.

4

PROPAGATION DELAY



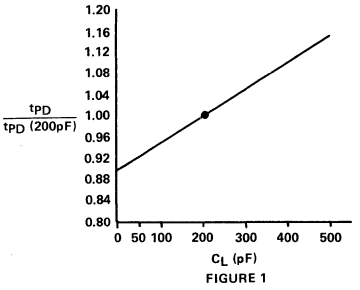


FIGURE 1

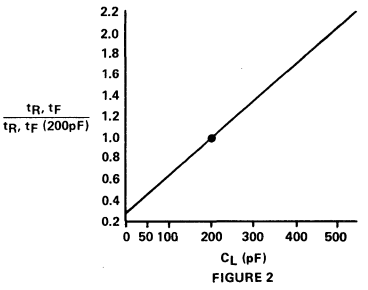


FIGURE 2

The above example will illustrate the calculation of a more useful propagation delay. The system on this example uses a 5 volt supply with a tolerance of ± 10%, an ambient temperature of as high as 125°C, and a calculated load capacitance of 150pF. This application requires the HD-6440-2. The table of A.C. specs shows the t_{PD} at 4.5V and 125°C is 100nsec. Use the graph in Figure 1 to get the degradation multiple for 150pF. The number shown is 0.97. The adjusted propagation delay, to the 10% or 90% point, is therefore 100 x 0.97 or 97nsec. To obtain the rise and fall times check the A.C. specs for the rise and fall times at 4.5V and 125°C to obtain a worst case rise time of 90nsec. Use Figure 2 to find it's degradation multiple to be 0.85. The adjusted rise time is, therefore, 90 x 0.85 or 76.5nsec. To obtain the standard 50% to 50% propagation delay, add the adjusted propagation delay to half of the adjusted rise time to get a propagation delay of 135nsec. The rise time was used here because it is always the worst case.

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HD-6495
CMOS HEX BUS DRIVER

Features

- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY. 300pF
- SOURCE CURRENT. 4mA
- SINK CURRENT 6mA
- PROPAGATION DELAY . . . . . 35nsec @ 5V

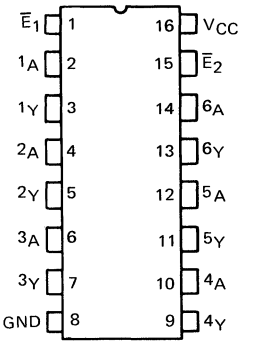
Description

The HD-6495 is a self aligned silicon gate CMOS Three-State buffer driver. The circuit consists of 6 non-inverting buffers with separate inputs and outputs which permit this driver to be used for bi-directional or uni-directional busing. A high on either Three-State control line $\overline{E}_1$ or $\overline{E}_2$ will force the drivers to the high impedance mode.

Outputs guaranteed valid at VCC 2.0V for Battery Backup Applications.

Pinout

TOP VIEW



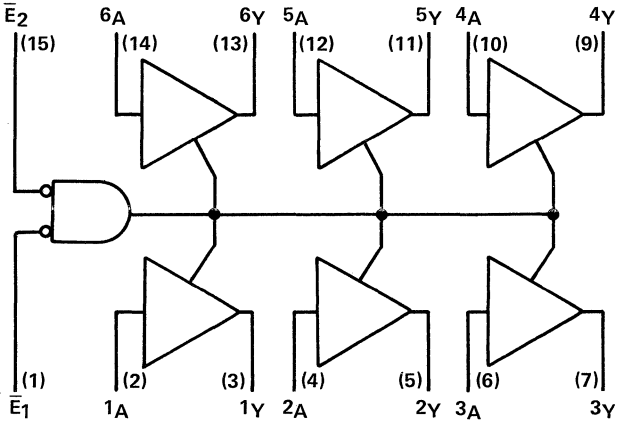
Truth Table

CONTROL INPUTS		INPUT	OUTPUT
$\overline{E}_1$	$\overline{E}_2$	A	Y
L	L	L	L
L	L	H	H
L	H	X	HI-Z
H	L	X	HI-Z
H	H	X	HI-Z

X = DON'T CARE
HI-Z = HIGH IMPEDANCE

4

Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+12.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6495A-9	-40°C to +85°C
Military HD-6495A-2	-55°C to +125°C
Operating Voltage Range	+4 to +11V

ELECTRICAL CHARACTERISTICS

V_{CC} = 10V ± 10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-10	10	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} -0.4		V	I_{OH} = -8.0mA, $\overline{E}_1 = \overline{E}_2$ = Low
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 12mA $\overline{E}_1 = \overline{E}_2$ = Low
I_O	Output Leakage	-10	10	μA	$0V \leq V_O \leq V_{CC}$, $\overline{E}_1 = \overline{E}_2$ = High
I_{CC}	Supply Current		100	μA	$V_{IN} = V_{CC}$ or GND, V_{CC} = 11V
C_{IN}	Input Capacitance*		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
C_O	Output Capacitance*		15	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

* Guaranteed and sampled, but not 100% tested.

C_L = 300pF

A.C.

		V_{CC} = 10.0V ① 25°C		V_{CC} = 10.0V ± 10% T_A = Indust. or Mil.		
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
t_{PD}	Propagation Delay		30		40	ns
t_{EN}	Enable Time		60		70	ns
t_{DIS}	Disable Time		60		70	ns
t_R	Output Rise Time		65		75	ns
t_F	Output Fall Time		65		75	ns

NOTE ①: All devices guaranteed at worst case limits. Room temperature, 10V data provided for information-not guaranteed.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6495-9	-40°C to +85°C
Military HD-6495-2	-55°C to +125°C
Operating Voltage Range	+4 to +7V

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-1.0	1.0	µA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} -0.4		V	I_{OH} = -4.0mA, $\overline{E}_1 = \overline{E}_2$ = Low
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 6.0mA $\overline{E}_1 = \overline{E}_2$ = Low
I_O	Output Leakage	-1.0	1.0	µA	$0V \leq V_O \leq V_{CC}$, $\overline{E}_1 = \overline{E}_2$ = High
I_{CC}	Supply Current		10	µA	$V_{IN} = V_{CC}$ or GND, V_{CC} = 5.5V
C_{IN}	Input Capacitance*		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
C_O	Output Capacitance*		15	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

* Guaranteed and sampled, but not 100% tested.

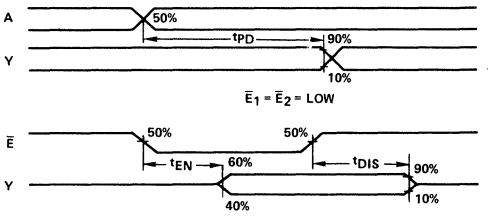
C_L = 300pF

A.C.

		V_{CC} = 5.0V ① 25°C		V_{CC} = 5.0V ± 10% T_A = Indus. or Mil.		
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
t_{PD}	Propagation Delay		35		45	ns
t_{EN}	Enable Time		90		100	ns
t_{DIS}	Disable Time		90		100	ns
t_R	Output Rise Time		85		95	ns
t_F	Output Fall Time		65		75	ns

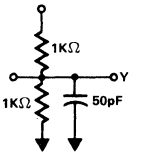
NOTE ① All devices guaranteed at worst case limits. Room temperature, 5V data provided for information–not guaranteed.

Switching Waveforms



All inputs have t_R, $t_F \leq$ 20ns.

OUTPUT TEST CIRCUIT
FOR PROPAGATION DELAYS



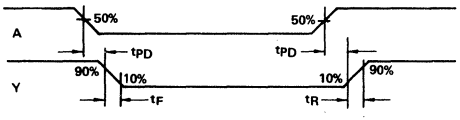
OUTPUT TEST CIRCUIT
FOR THREE-STATE DELAYS

DECOUPLING CAPACITORS

The transient current required to charge the load capacitance is given by $I_T = C\frac{dv}{dt}$. Assuming that all outputs may change state at the same time and that $\frac{dv}{dt}$ is constant; $I_T = \left(\Sigma C_L\right)\left(\frac{V_{CC} \times 80\%}{t_R \text{ or } t_F}\right)$ eg. $\left[t_R = 85\text{ns}, V_{CC} = 5.0\text{V}, \text{each } C_L = 300\text{pF}, I_T = (6)\left(300 \times 10^{-12}\right)\frac{5.0 \times 0.8}{85 \times 10^{-9}} = 84.7\text{mA}.\right]$ This current spike may cause a large negative voltage spike on V_{CC}, which if it becomes a diode drop less than any input, may cause the device to latch up. It is recommended that a 0.1 μF ceramic disk decoupling capacitor be placed between V_{CC} and GND at each device to filter out this noise.

4

PROPAGATION DELAYS



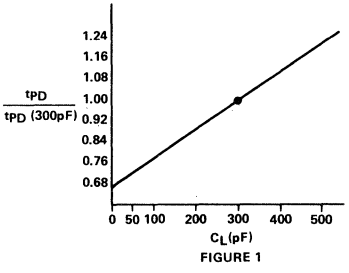


FIGURE 1

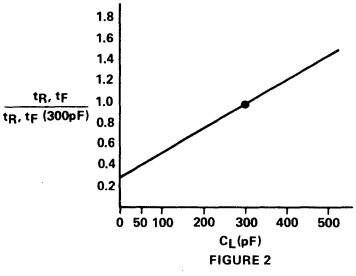


FIGURE 2

The above example will illustrate the calculation of a more useful propagation delay. The system on this example uses a 5 volt supply with a tolerance of ± 10%, an ambient temperature of as high as 125°C, and a calculated load capacitance of 150pF. This application requires the HD-6495-2. The table of A.C. specs shows the t_{PD} at 4.5V and 125°C is 45nsec. Use the graph in Figure 1 to get the degradation multiple for 150pF. The number shown is 0.84. The adjusted propagation delay, to the 10% or 90% point, is therefore 45 x 0.84 or 38nsec. To obtain the rise and fall times check the A.C. specs for the rise and fall times at 4.5V and 125°C to obtain a worst case rise time of 95nsec. Use Figure 2 to find it's degradation multiple to be 0.65. The adjusted rise time is, therefore, 95 x 0.65 or 62nsec. To obtain the standard 50% to 50% propagation delay, add the adjusted propagation delay to half of the adjusted rise time to get a propagation delay of 69nsec. The rise time was used here because it is always the worst case.

Microprocessor Support Systems

μP

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HB-61001 4K x 12 Memory Board	5—8
DECstation-78	5—13
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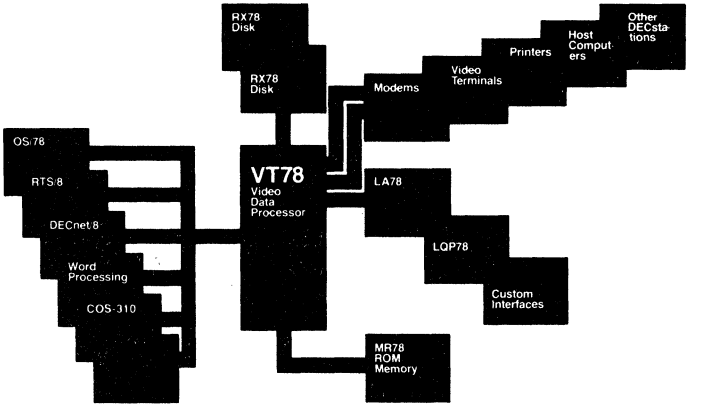
5

Support Overview

Harris provides the foundation tools needed for system development including a prototyping board and thorough documentation. For software development needs, Harris recommends the use of DIGITAL Equipment Corporation's DECstation-78 because it provides flexibility and versatility for many functions.

The MICRO-12 is an all CMOS, single-board system that can be obtained either fully assembled or in kit form. To complement the MICRO-12, a 4K CMOS RAM board is also available. Both the MICRO-12 and the RAM board have wire-wrap areas available for prototyping specialized interfaces such as A/D converters.

The DECstation-78 is a "packaged" computer system that in its basic configuarations comprise an LSI version of the 16K PDP-8 minicomputer, a video display terminal, one or two RX78 Dual Floppy Disk drive(s), an easy-to-use interface system, and a versatile operating software system OS/78. Unlike other systems which must be configured from individually selected system components, DECstation-78's components are carefully matched and tested as a system by DIGITAL to ensure hassle-free startup. Harris offers application software to link the DECstation-78 to the MICRO-12 and to a Data I/O Model 9 PROM Programmer.



The DECstation-78 can be easily programmed to perform in a wide range of data processing enviromnents — everything from personal computing and software development to real-time, multitasking operations and networking. The Operating System OS/78 supports the popular high-level programming languages BASIC and FORTRAN IV and is an excellent tool for general purpose program development in the single user environment.

Installation is simple. There is only one cable between the processor and each peripheral. Fewer complicated electronic and mechanical parts and interconnection cables mean fewer maintenance problems and easier installation. In fact, system interconnection has been so streamlined and simplified that DECstation-78 can be installed by the user in something less than an hour — without special tools. The interconnections are through external plug-in ports which allow the user to adapt or reconfigure DECstation-78 to handle new processing needs as they occur. The I/O connection panel on the back of the processor contains five ports. Two serial EIA RS-232C asynchronous interface ports are suitable for interfacing with terminals and other devices that operate from 50 to 19,200 baud. One port is equipped for modem control. A parallel I/O port for printers and custom interfacing provides bi-directional 12-bit transfers at rates up to 15K words per second. A disk interface port allows connection to RX78 Floppy Disks.

The OS/78 operating system is a complete software development operating system designed to run on DECstation 78. OS/78 is supplied as part of the basic system. In addition to OS/78, a multitasking real-time operating system RTS/8 is optionally available. RTS/8, assembly language based, allows multiple tasks to run concurrently while competing for resources on a fixed priority basis. For small business applications, the COS-310 commercial operating system can be added. Word processing software, WPS-8, can also be added to help with your documentation requirements.

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HB-61000
MICRO-12

Features

- COMPLETE SINGLE BOARD CMOS MICROCOMPUTER SYSTEM
- INCLUDES CPU, MEMORY, UART AND I/O
- HIGH PERFORMANCE CMOS 12 BIT CPU
- WIDELY USED PDP-8* INSTRUCTION SET
- INTERFACES DIRECTLY WITH TTY/CRT TERMINAL/ TAPE CASSETTE
- INTERACTIVE KEYBOARD & DISPLAY
- USER WIREWRAP AREA
- EXTENSIVE CONTROL PANEL MONITOR IN ROM
- LARGE USER SOFTWARE LIBRARY AVAILABLE
- SMALL 5V POWER SUPPLY INCLUDED.

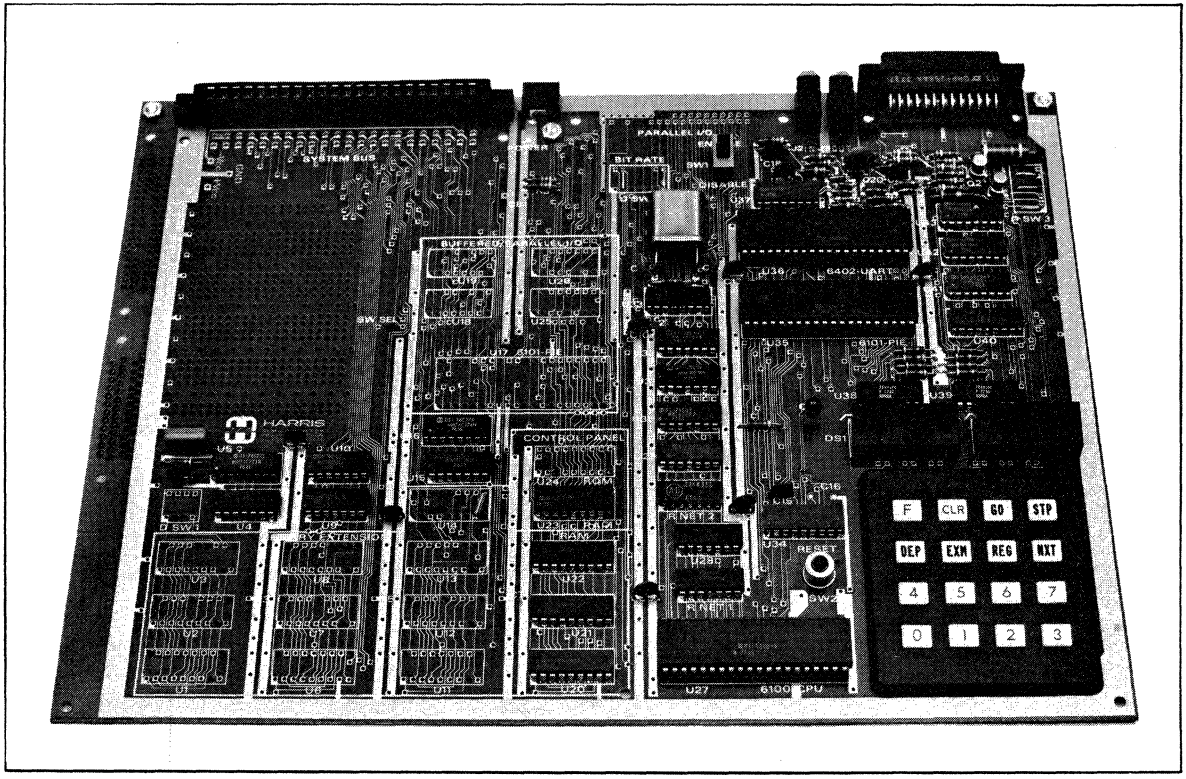
* Trademark of Digital Equipment Corp., Maynard, Ma.

Description

The Harris MICRO-12 is a fully assembled and tested single board CMOS 12 bit microprocessor system. A preprogrammed ROM provides a system monitor, keyboard and display utilities and system diagnostic capabilities.

The MICRO-12 includes an 8 digit LED display and 16 key-keyboard which allows direct program insertion, execution and examination.

The ROM system monitor also provides a Binary Loader and List capability from a TTY. A Kansas City Standard Tape Cassette interface (300 Baud) provides the user with a simple means of loading and storing programs.



5

The MICRO-12 is a fully assembled and tested 12 bit CMOS microprocessor system. It is compact (8.4" x 11.6") and provides a full compliment of CMOS system components. A system monitor ROM (1K x 12) allows the user to enter his program manually with a 16 key keyboard or through a TTY or tape cassette by using the Binary Loader feature. A standard program memory of 256 words x 12 bit RAM is provided with optional socket space for a full 1K x 12 program memory. The monitor does not use any of the user program memory.

The system monitor provides the user with four (4) independent breakpoints for program debug. An 8 digit display allows inspection of the address, memory and register data.

A special function key allows the user program to be listed on either an external TTY or CRT. Another special function key allows the user to punch a program tape on the TTY. The Binary Punch feature may also be used to load an external tape cassette from program memory. A 300 baud Kansas City Standard interface is provided for this purpose. Communications rate of 50 to 9600 baud are jumper selectable on the Bit Rate Generator through the Universal Asynchronous Receiver Transmitter (UART).

KEYBOARD MONITOR COMMANDS:

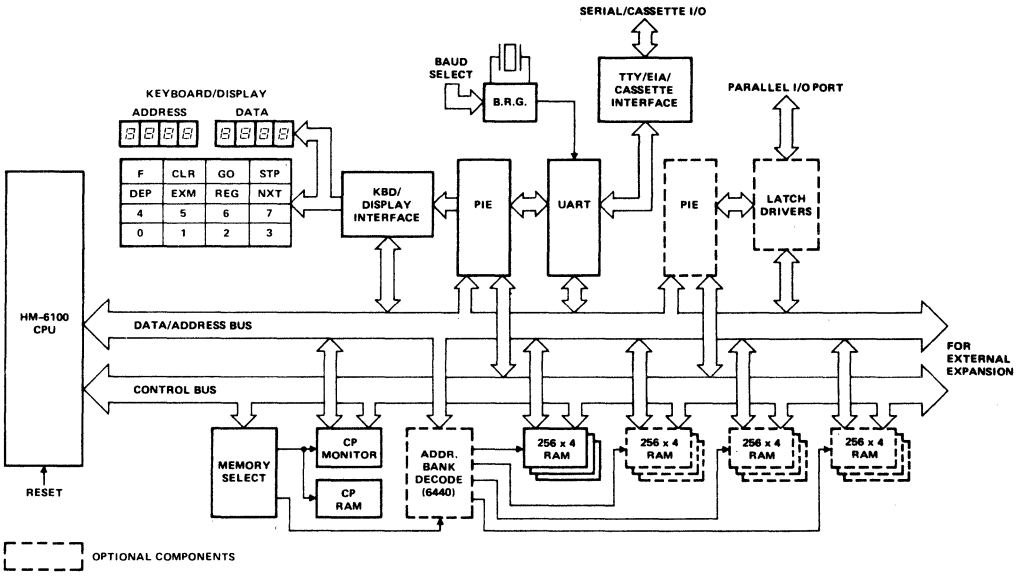
- **EXAMINE** – Allow user to inspect memory data at keyed in address.
- **DEPOSIT** – Alters data at data address.
- **REGISTER EXAMINE** – Allows the user to examine PC, AC, MQ & LINK.
- **NEXT (INSTRUCTION)** – Increments present address.
- **EXECUTE** – Allows the user program to be executed.
- **SINGLE CYCLE** – Allows program to execute single instruction at a time.
- **FUNCTION** – Causes entry to be second function routines.
- **CLEAR** – Clears accumulator, MQ registers, LINK, and Breakpoints (P.C. address is set to 7777).

FUNCTION COMMANDS:

- **BINARY LOAD** – Allows TTY reader or cassette entry of user program.
- **BINARY PUNCH** – Allows TTY punching or cassette loading of users program.
- **OCTAL LISTING** – Allows TTY printing of user program.
- **BREAKPOINT SET** – Examine/alter any of four software breakpoints.

Documentation package includes detailed information on using the control panel, how the system operates and users manual which contains circuit diagrams and a listing of the control panel program. Several hardware and software examples are included. The Micro-12 User Manual can be ordered from Harris for more detailed information.

Functional Block Diagram



HM-6100 Microprocessor

The HM-6100 CMOS Microprocessor is a single address, fixed word length, parallel transfer 12 bit microprocessor. It is a member of a broad based CMOS product line which comprises 6100 peripheral devices, RAMs, PROMs, ROMS and a full logic family. The processor recognizes the PDP-8* instruction set and utilizes two's complement arithmetic logic. The device is completely static and may be operated from DC to its rated frequency. No external clock generators or controllers are required.

The support chips, Peripheral Interface Element (PIE), Universal Asynchronous Receiver Transmitter (UART), Bit Rate Generator, Read Only Memories (ROM), Random Access Memories (RAM) and Programmable Read Only Memories (PROM) are completely compatible with the microprocessor. All devices are available in either an industrial or a military temperature range.

* Trademark of Digital Equipment Corp., Maynard Ma.

Table of Instruction Set

BASIC INSTRUCTIONS

MNEMONIC	OCTAL CODE	OPERATION
AND	0XXX	Logical AND
TAD	1XXX	Binary ADD
ISZ	2XXX	Increment, and skip if zero
DCA	3XXX	Deposit and clear AC
JMS	4XXX	Jump to subroutine
JMP	5XXX	Jump
IOT	6XXX	In/out transfer
OPR	7XXX	Operate

GROUP 1 OPERATE MICROINSTRUCTIONS

MNEMONIC	OCTAL CODE	OPERATION	LOG SEQ
NOP	7000	No operation	1
IAC	7001	Increment accumulator	3
RAL	7004	Rotate accumulator left	4
RTL	7006	Rotate two left	4
RAR	7010	Rotate accumulator right	4
RTR	7012	Rotate two right	4
BSW	7002	Byte swap	4
CML	7020	Complement link	2
CMA	7040	Complement accumulator	2
CIA	7041	Complement and increment accum.	2,3
CLL	7100	Clear link	1
CLL RAL	7104	Clear link–rotate accum. left	1,4
CLL RTL	7106	Clear link–rotate two left	1,4
CLL RAR	7110	Clear link–rotate accum. right	1,4
CLL RTR	7112	Clear link–rotate two right	1,4
STL	7120	Set the link	1,2
CLA	7200	Clear accumulator	1
CLA IAC	7201	Clear accum. –increment accum.	1,3
GLK	7204	Get the link	1,4
CLA CLL	7300	Clear accumulator–clear link	1
STA	7240	Set the accumulator	1,2

GROUP 2 OPERATE MICROINSTRUCTIONS

MNEMONIC	OCTAL CODE	OPERATION	LOG SEQ
NOP	7400	No operation	1
HLT	7402	Halt	3
OSR	7404	Or with switch register	3
SKP	7410	Skip	1
SNL	7420	Skip on non-zero link	1
SZL	7430	Skp on zero link	1
SZA	7440	Skip on zero accumulator	1
SNA	7450	Skip on non-zero accumulator	1
SZA SNL	7460	Skip on zero accum, or skip on non-zero link, or both	1
SNA SZL	7470	Skip on non-zero accum. and skip on zero link	1
SMA	7500	Skip on minus accumulator	1
SPA	7510	Skip on positive accumulator	1
SMA SNL	7520	Skip on minus accum. or skip on non-zero link or both	1
SPA SZL	7530	Skip on positive accum. and skip on zero link	1
SMA SZA	7540	Skip on minus accum. or skip on zero accum. or both	1
SPA SNA	7550	Skip on positive accum. and skip on non-zero accum.	1
SMA SZA SNL	7560	Skip on minus accum. or skip on zero accum. or skip on non-zero link or all	1
SPA SNA SZL	7570	Skip on positive accum. and skip on non-zero accum. and skip on zero link	1
CLA	7600	Clear accumulator	2
LAS	7604	Load accum. with switch register	1,3
SZA CLA	7640	Skip on zero accum. then clear accum.	1,2
SNA CLA	7650	Skip on non-zero accum. then clear accum.	1,2
SMA CLA	7700	Skip on minus accum. then clear accum.	1,2
SPA CLA	7710	Skip on positive accum. then clear accum.	1,2

GROUP 3 OPERATE MICROINSTRUCTIONS

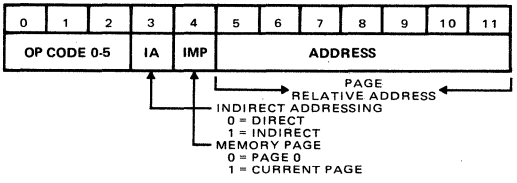
MNEMONIC	OCTAL CODE	OPERATION	LOG SEQ
NOP	7401	No operation	3
MQL	7421	MQ register load	2
MQA	7501	MQ register into accumulator	2
SWP	7521	Swap accum. and MQ register	3
CLA	7601	Clear accumulator	1
CAM	7621	Clear accum. and MQ register	3
ACL	7701	Clear accum. and load MQ register into accumulator	3
CLA SWP	7721	Clear accum. and swap accum. and MQ register	3

PROCESSOR IOT INSTRUCTIONS

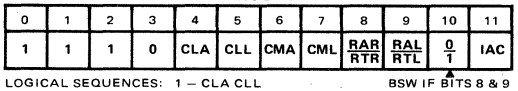
MNEMONIC	OCTAL CODE	OPERATION
SKON	6000	Skip if interruption on
ION	6001	Interrupt turn on
IOF	6002	Interrupt turn off
SRQ	6003	Skip if INT request
GTF	6004	Get flags
RTF	6005	Return flags
SGT	6006	Operation is determined by external devices, if any
CAF	6007	Clear all flags

Bit Assignments

MEMORY REFERENCE INSTRUCTION FORMAT



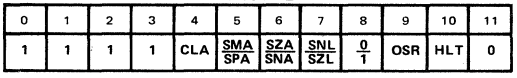
GROUP 1



LOGICAL SEQUENCES: 1 – CLA CLL
2 – CMA CML
3 – IAC
4 – RAR RAL RTR RTL BSW

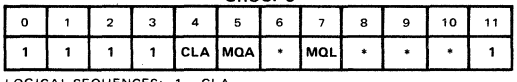
BSW IF BITS 8 & 9 ARE 0 AND BIT 10 IS 1

GROUP 2



LOGICAL SEQUENCES: 1 (Bit 8 is Zero) – SMA or SZA or SNL
(Bit 8 is One) – SPA and SNA and SZL
2 – CLA
3 – OSR HLT

GROUP 3



LOGICAL SEQUENCES: 1 – CLA
2 – MQA MQL
3 – ALL OTHERS

* DON'T CARE

Specifications

CENTRAL PROCESSOR

HM-6100

- Crystal Controlled 2.45MHz
- Single Power Supply . . . . . +5 Volts
- CMOS . . . . . TTL Compatible

MEMORY

ROM – 1K x 12 Bits Monitor (Resident in control panel memory does not use user address space.)

RAM – 256 x 12 Bits (Expandable to 1K words.)

INTERFACES

SERIAL I/O:	20mA Current Loop TTY RS-232 (Jumper Selectable) Baud Rate 50 thru 9600 (Jumper Selectable)
BUS:	CMOS Compatible (Dual 22 Pin Connector Provided)
PARALLEL I/O:	12 Bit Input (Optional) 12 Bit Output (Optional) Large User Wirewrap Area Provided for Additional I/O

SOFTWARE

System monitor provided in ROM with resident keyboard, display and serial output control. Allows user to load, dump and display programs.

LITERATURE (Provided with Micro-12)

- Micro-12 User Manual
- Microprocessor Systems Design Manual
- Introduction to Programming
- Assembly Language Reference Card
- Introduction to DECUS

PHYSICAL CHARACTERISTICS

- Height . . . . . 8.4 Inches
- Width . . . . . 11.6 Inches
- Depth . . . . . 0.75 Inches
- Weight . . . . . 14 Oz.

ELECTRICAL CHARACTERISTICS

- V_{CC} = ...(+)5 Volts ±10%
- V_{TTY} = ...(-)12 Volts ±20%, 30mA (Req. only if TTY is connected.)
- I_{CC} = ...40mA (System), 160mA (Display)

OPTIONS:

- 1K Memory
- 4K Memory
- Parallel I/O
- Downloader Software

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HB-61001
CMOS MEMORY BOARD

Features

- SINGLE SUPPLY, 5V
- ALL CMOS SYSTEM, HIGH NOISE IMMUNITY
- LOW POWER, < 12mW MAXIMUM STANDBY
- DATA RETENTION @ 2 VOLTS
- BUS COMPATIBLE WITH HB-61000 MICROCOMPUTER BOARD
- 4096 x 12 RAM
- 2048 x 12 OPTION – ADDRESS SELECTABLE

Description

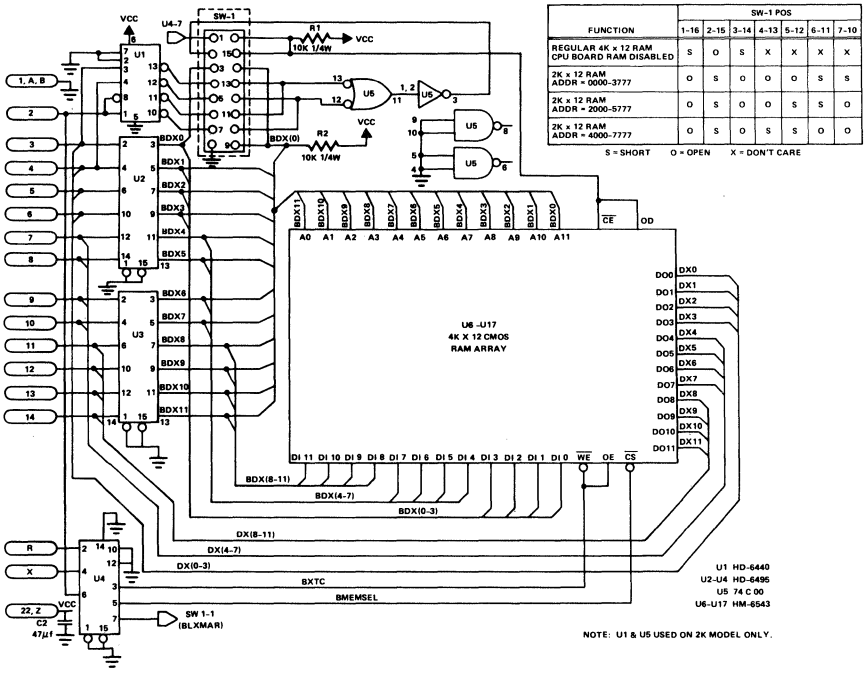
The HB-61001 is a fully assembled and tested all-CMOS memory board, designed to interface directly with the HB-61000 (MICRO-12) single board computer.

The board uses Harris' high performance HM-6543 fully static CMOS RAM's. The HB-61001 comes with either 4K x 12 or 2K x 12 organizations with address selectable by jumper options.

Interfacing the board to other systems is extremely easy, only three (3) control signals and a 12-bit multiplexed address/data bus are needed. See bus signals definition for details. There is no field control logic for extended memory.

A wire wrap area (1.7 x 4"2) with .1" center holes are provided on the board for custom interface circuitrys, battery back-up circuitry, etc.

Functional Block Diagram



FUNCTION	SW-1 POS 1-16	2-15	3-14	4-13	5-12	6-11	7-10
REGULAR 4K x 12 RAM CPU BOARD RAM DISABLED	S	O	S	X	X	X	X
2K x 12 RAM ADDR = 0000-3777	O	S	O	O	O	S	S
2K x 12 RAM ADDR = 2000-5777	O	S	O	O	S	S	O
2K x 12 RAM ADDR = 4000-7777	O	S	O	S	S	O	O

S = SHORT O = OPEN X = DON'T CARE

ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage	+8.0V	Operating Supply Voltage	VCC 4.5V to 5.5V
Applied Input or Output Voltage	GND -0.3V VCC to +0.3V	Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +100°C	Physical Characteristics	4.5" x 7.0" x .6" Weight: 5 oz.

ELECTRICAL CHARACTERISTICS

VCC = 5V ±10% TA = Operating Range

	SYMBOL	PARAMETER	HB-61001-1 MIN	HB-61001-1 MAX	HB-61001-2 MIN	HB-61001-2 MAX	UNIT	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		1.0		1.0	mA	VI = VCC or GND IO = HIZ
	ICCOP	Operating Supply Current ①		15		15	mA	f = 125kHz
	VCCDR	Data Retention Supply Voltage	2.0		2.0		V	
	ICCDR	Data Retention Supply Current		1.0		1.0	mA	VCC = 3.0 VI = VCC or GND
	VIH	Input High Voltage	70% VCC	VCC +0.3	70% VCC	VCC +0.3	V	
	VIL	Input Low Voltage	GND -0.3	20% VCC	GND -0.3	20% VCC	V	
	VOH	Output High Voltage	2.4		2.4		V	IOH = -2.0mA
	VOL	Output Low Voltage		0.4		0.4	V	IOL = 2.0mA
	II	Input Leakage Current	-1.0	+1.0	-1.0	+1.0	μA	GND ≤ VI ≥ VCC
	IOZ	Output Leakage Current	-20	+20	-20	+20	μA	GND ≤ VO ≥ VCC
	CI	Input Capacitance ②		15		15	pF	f = 1MHz I/O = HIZ
	CI/O	Input/Output Capacitance ②		30		30	pF	
A.C.	TAS	Address Set Up Time	25		25		ns	③
	TAH	Address Hold Time	75		165		ns	
	TLX	LXMAR Pulse Width (Positive)	200		200		ns	
	$\overline{TLX}$	LXMAR Pulse Width (Negative)	450		575		ns	
	TAL	Access Time from LXMAR		450		575	ns	
	TCY	Read or Write Cycle Time	650		775		ns	
	TEN	Output Enable Time		250		250	ns	
	TDIS	Output Disable Time		150		150	ns	
	TDS	Write Data Set Up Time	130		130		ns	
	TDH	Write Data Hold Time	50		50		ns	
	TWP	Write Pulse Width	220		220		ns	

NOTES:

① Operating current (ICCOP) is proportional to operating frequency. Example: Typical ICCOP 80mA/MHz.

② Capacitance sampled and guaranteed but not 100% tested.

③ AC test conditions: Inputs TRISE = TFALL ≤ 100ns; Outputs — 1 TTL load and 100pF.

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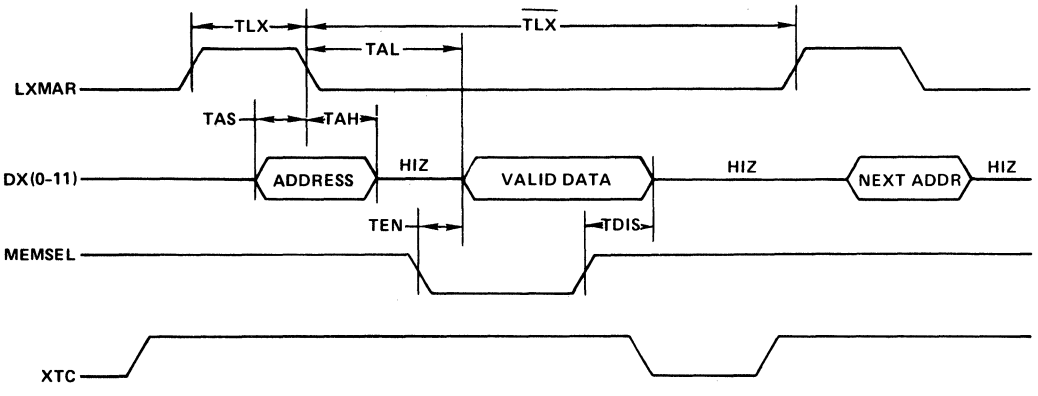


FIGURE 1-1 -- Read Cycle Timing

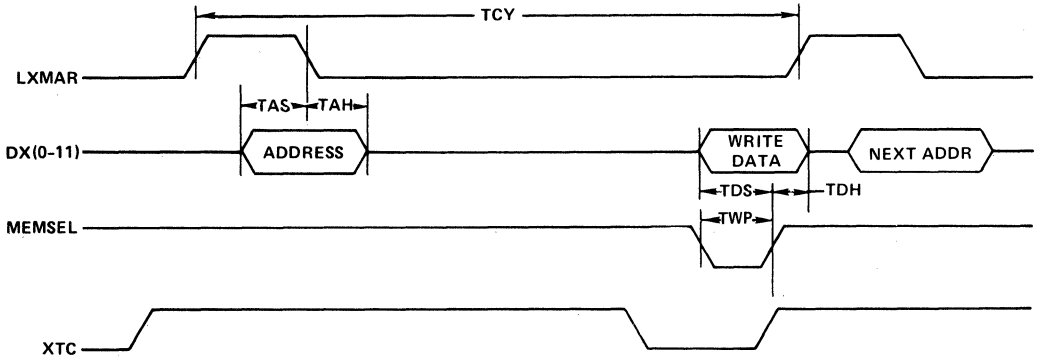


FIGURE 1-2 – Write Cycle Timing

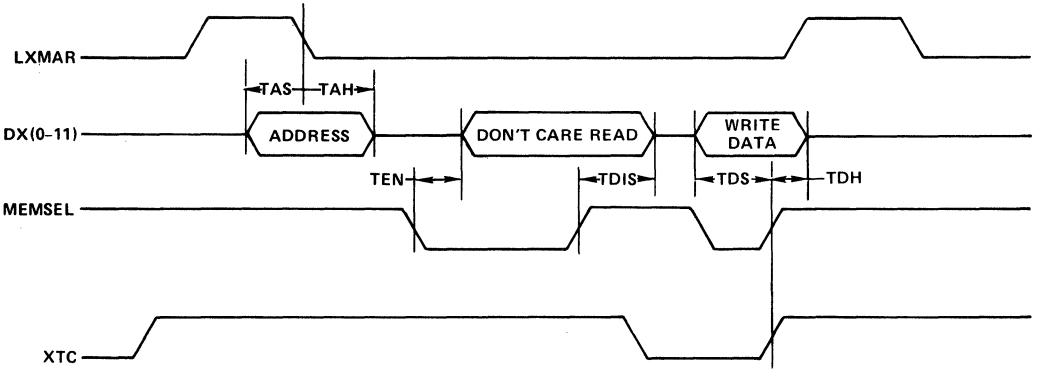


FIGURE 1-3 – MICRO-12 Compatible Timing Read Modify Write Cycle

BASIC INSTALLATION

To install the HB-61001 memory board in the MICRO-12, first determine the amount of RAM that exists on the CPU board.

If there are 256 words of onboard RAM, and no HD-6440 in U14, installing the HB-61001 is accomplished by removing the jumper from pin 8 to 10 of U14 on the MICRO-12 and replacing it with a jumper from pin 10 to pin 6 of U14. Next plug the memory board into the edge connector with the components facing the keypad.

If there are more than 256 words of RAM and a HD-6440 in U14 on the MICRO-12 replace the jumper from pin 2 to 7 of DSW-1 on the MICRO-12 with one from pin 8 to ground of DSW-1 and plug in the memory board.

SPECIAL HINTS FOR 2K VERSION USERS

It is possible for users of the 2K version (HB-61001-2) to actually have up to 3K of useable read write memory. This is accomplished by utilizing both the MICRO-12 onboard memory and the external memory board. Setting the HB-61001 memory board to reside at locations 2000-5777 octal and leaving the MICRO-12 memory enabled allows the use of all available memory. See the truth table on the first page for details on setting the address of the HB-61001-2. Refer to the MICRO-12 manual, page A-61 for details of the onboard memory circuits.

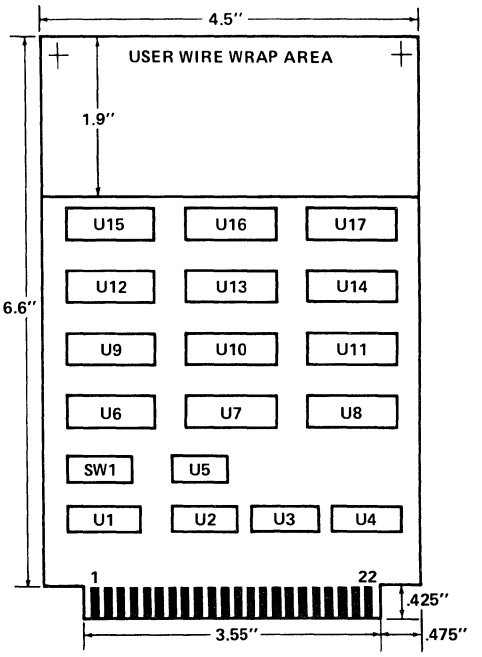


FIGURE 2 – HB-61001 Dimensions

Battery Back-Up

In many applications it is desireable to provide for data retention during power interruptions. The circuit shown in Figure 3 will provide power to the memory during power outages and doubles as a battery charging circuit during normal operation.

In addition to providing a standby supply, the user must take precautions to guarantee that none of the CMOS inputs are left floating during the power outage. The easiest way to accomplish this, is to add 10K pull-up resistors from all board inputs to CMOS VCC.

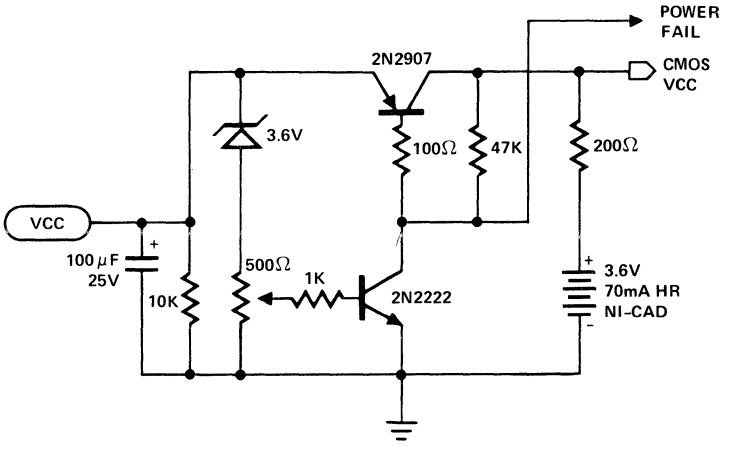


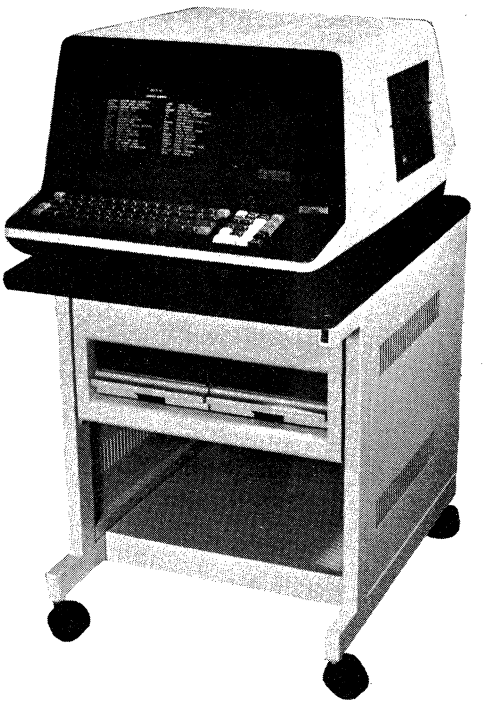
FIGURE 3 – A Typical Battery Back-Up Circuit

(Connector Type: Dual 22 Pin .156" spacing)

PIN #	SIGNAL	DESCRIPTION
1, A, B	GND	Ground
2	LXMAR	Chip enable signal; the negative going edge latches address in RAM and initializes a memory cycle.
3	DX0	Multiplexed address/data bus, most significant bit.
4	DX1	
5	DX2	
6	DX3	
7	DX4	
8	DX5	
9	DX6	
10	DX7	
11	DX8	
12	DX9	
13	DX10	
14	DX11	Multiplexed address/data bus, least significant bit.
R	XTC	READ/$\overline{\text{WRITE}}$ control signal (READ = High, WRITE = Low)
X	MEMSEL	Memory select, active low.
Z, 22	V_{CC}	+5V ($\pm$ 10%) Supply

DECstation-78 Technical Description

In DECstation-78 the computer and terminal are a single compact unit, designated as a VT78 Video Data Processor. The processor and display are interconnected over a high-speed serial line with the processor physically located inside the video display's case. A single START switch activates the entire system. At system power-up, the display and keyboard are automatically tested.



VIDEO DISPLAY AND KEYBOARD

The keyboard/video display is basically a DECscope in origin but has some added features to tailor it to DECstation-78. The same clarity of displayed characters, adjustability of screen intensity, and glare-free screen popular in DECscope products are carried over in DECstation-78. The display system includes a 24-line by 80 character screen format, the complete ASCII upper and lower character set, 33 special symbols, and nineteen user-defined special function keys.

The keyboard is standard typewriter (ANSII) and produces a key-stroke click for audible feedback of key operation. Three-key rollover protection eliminates fast typing errors. Should three keys be depressed simultaneously, transmission will still be correct if one of the first two key typed is released before the third. Note that striking a key does not directly cause a display result. All instructions are fed to the processor which then controls the displayed characters or cursor movements. This is equvalent to a DECscope-Host computer configuration where the instructions are echoed back from the host.

An auxiliary keypad extends the keyboard's capabilities. The keypad has 19 keys. There are two modes in which the keypad can operate, Normal and Alternate. When in the Normal Mode, the ten numeral keys and the decimal point key, respond like the numeral keys and decimal point key on the main keyboard. The ENTER key responds like the RETURN key. The Alternate Mode is established by an escape sequence (ESC =) to enter the mode and (ESC >) to exit the mode. When in the Alternate Mode, the ten numeral keys, the decimal point key, and the ENTER key transmit unique escape codes for custom assignment by the user. In either mode, there are also three blank unassigned keypad keys for user definition. Cursor control keys complete the keypad's function.

PROCESSOR

The overall organization of DECstation-78 is shown in the Figure below. An LSI (large scale integration) version of the powerful PDP-8 minicomputer contained on a 15 3/4" x 11 7/8" printed circuit board is mounted inside of DECstation-78's video display unit. This is the processor for the system. It includes a 12-bit CPU with memory extension control, 16,384 words (32 bytes) of Random Access Memory, complete peripheral interfacing, internal bootstrap facilities, and a 100Hz real-time clock. The CPU has the same powerful instruction set as the PDP-8A. Cycle time is approximately 3.6 microseconds.

Three general purpose processor registers are provided:

- PC. The 12-bit program counter points to the location from which the next instruction will be fetched.
- AC, L. The 12-bit accumulator and its 1-bit carry extension, the Link, form the register where all arithemtic calculations take place.
- MQ. The 12-bit Multiplier Quotient register serves as a temporary storage register.

Memory

Main memory is 12-bits by 16K words of Random Access NMOS Memory organized as 4 fields of 4K words each. Each field consists of 32 pages of 128 words.

An on-board ROM permits several important features to be included. These are:

- Automatic self-test procedure.
  Processor status display.
- Terminal emulation mode, which alllows DECstation-78 to be used as a stand alone computer terminal without independent processing capability.
- Internal disk bootstrap.
  Preselection of baud rates on primary communications port.

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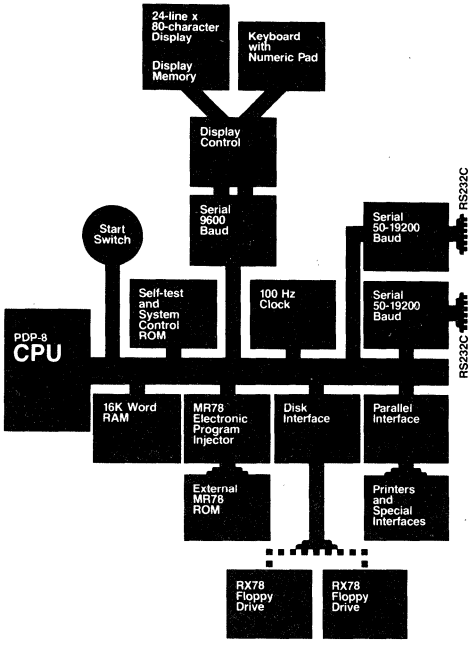


Instructions

There are two basic groups of instructions: memory reference and microinstructions. Memory reference instructions require an operand; microinstructions do not. The DECstation-78 processor features indirect addressing capability up to 4K and 8 auto-index registers. Three groups of operate microinstructions perform a variety of program operations without any need for reference to memory location. Groups 1 and 2 allow the programmer to manipulate and/or test the data that is located in the accumulator or link. Group 3 operate instructions allow the programmer to manipulate the MQ register. Many of these operate microinstructions may be combined by the experienced programmer in order to use the DECstation-78 processor more efficiently.

Input/Output (IOT) instructions are used to control the operation of the computer's interrupt system and clock and to make all exchanges of data to the system display, keyboard, and externally connected peripherals.

Interface Ports

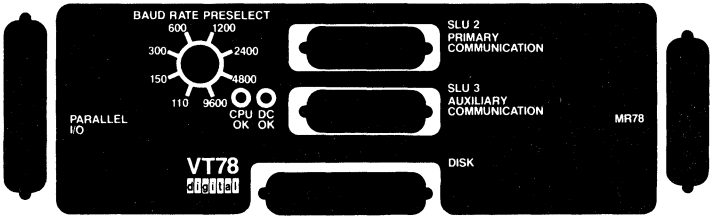
There are six interface ports for DECstation-78: a parallel port, a disk interface port, a electronic program injection port and three asynchronous serial ports.

Parallel I/O Port – is for printers and custom interfacing. It provides bi-directional 12-bit transfers at rates up to 15K words per second.

Serial Line Unit-1 (SLU-1) – connects the central processor to the display subsystem internally and is not externally accessible. The two other asynchronous serial EIA RS-232C interface ports are suitable for primary and secondary communications applications, terminals, and the attachment of a variety of devices. These ports (SLU-2 and SLU-3) features 16 program selectable baud rates ranging from 50 to 19,200 baud and programmable loopback for maintenance. One port, SLU-3, provides programmable parity generation and overrun detection, variable width stop-bit selection and programmable character length. The other port, SLU-2, is equipped for full modem control.

Disk Interface Port – allows connection between the DECstation-78 processor and two independent dual drive disk units (RX78). It provides both 8- and 12-bit data formats for maximum flexibility.

MR78 Electronic Program Injection Port – allows the mounting of an external Read Only Memory program capsule. The MR78 provides high speed loading under control of a preprogrammed ROM unit. Loading is automatically initiated when the DECstation-78 START button is pressed.



RX78 FLOPPY DISK DRIVE

The RX78 Floppy Disk System is an inexpensive mass storage subsystem, I/O and random access file device characterized by speed and reliability. Either one or two compact, self-contained units may be interfaced with the processor via a high-speed data port on the external connector panel.

Track-to-track moves require six milliseconds for the move plus twenty milliseconds for settling time if the head is loaded for a read or write. The rotational speed of the diskette is 360-rpm, with an average latency time of 83 milliseconds. The total average access time is only 263 milliseconds.

The RX78 Floppy Disk System uses IBM-standard diskettes — thin, flexible oxide-coated disks about the size of a 45-rpm phonograph record. The disk is recorded only on one side and is permanently contained in an 8-inch square flexible protective envelope. The diskette contains 77 tracks with 26 sectors per track. Each sector can store 256 8-bit bytes or 128 12-bit words for a total formatted capacity of 512,512 bytes or 256,256 words. The diskette is a portable, convenient storage, interchange and software distribution medium which allows DECstation-78 users to store large amounts of data in a small space.

PRINTERS

For local on-site output, the LA78 DECprinter-1 180-cps line printer is recommended. This printer interfaces via a parallel port on DECstation-78. For word processing applications, the LQP78 letter quality printer is available.

Support Software

Harris supports its microprocessor-based systems through an extensive variety of proven PDP-8 software. For the DECstation-78, there are three major operating system packages available. These are: the OS/78 operating system that is included in the price of the basic DECstation-78 package; an optional commercial operating system, COS-310, for small business applications; and a word processing system, WPS-8, for documentation and other text editing needs. For real-time multitasking, RTS/8 can also be added.

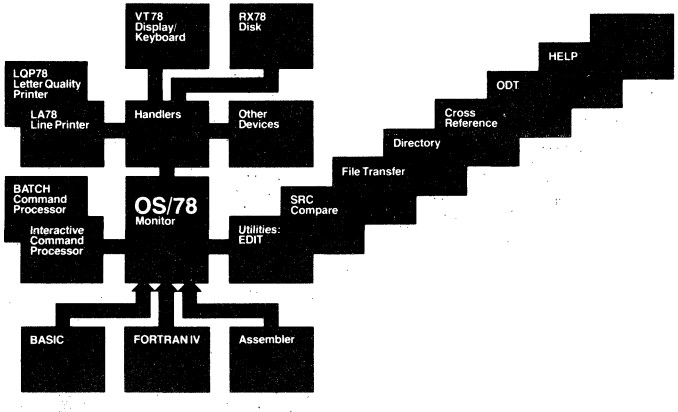
In addition to these basic software support packages, Harris can provide the user application software for linking the DECstation-78 to a hardware development system, such as the MICRO-12. Harris also has a software package to link the DECstation-78 to a Data I/O Model 9 PROM Programmer. PAL-8 based cross assemblers for the popular 8-bit microprocessors can be obtained from various sources, thus increasing the functionality of the DECstation-78. The user also has access to the extensive DECUS library of PDP-8 programs which in many cases can reduce development efforts.

MULTILANGUAGE OPERATING SYSTEM OS/78

OS/78 provides DECstation-78 users with power and flexibility in both interactive and batch programming environments. OS/78 is based on DIGITAL's proven OS/8 and offers many features previously available only on larger computer systems. OS/78 maximizes utilization of DECstation-78 main memory because the resident portion of the operating system requires only 256 words of memory. Non-resident portions of the system are swapped into memory from the RX78 floppy disk automatically as required.

OS/78 is easy to use and provides the development programmer with a complete, logical interface to program and file structures. All data files and executable programs are stored in one or more floppy disks where they may be accessed for loading, modification or execution by simple keyboard commands.

OS/78 incorporates Commercial BASIC and FORTRAN IV and provides a comprehensive set of software tools and utility programs that help make DECstation-78 an excellent program development and calculations tool in the single-user environment. These include EDIT, PAL8, CREF, ODT and BATCH PROCESSING, among others.



EDIT – is a line-oriented text editor that allows the user to enter and modify ASCII files. It supports commands to list, insert, delete, change and move text as well as to search for character strings.

PAL 8 – is a two-pass language assembler that provides the programmer with the capability of coding directly in machine-oriented symbolic instructions. Its features include: 1) conditional assembly which enables a single source file to produce different binaries for different purposes; 2) paginated listings, page headings and page numbering to improve program documentation; and 3) a symbol table which lists all program labels and their memory location or value.

CREF (Cross-Reference Utility Program) – aids the programmer in writing, debugging and maintaining assembly language programs by providing the ability to pinpoint all references to a particular symbol. CREF provides an alphabetical cross-reference table for PAL8 assembly listings and numbers each line in the listing. Program symbols and literals are printed alphabetically along with the numbers of the lines that reference to them. Optional two-pass operations doubles the number of symbols that can be accommodated in a program.

BITMAP – is an OS/78 utility used to construct a table, or map, showing the memory locations used by a given binary file. BITMAP will accept any absolute binary file as input and route its output to any supported I/O device.

ODT (Octal Debugging Technique) – is invisibly co-resident with the user program so that there is no need to allocate more than 3 words in each 4K field for a debugging package during development. Breakpoints can be set anywhere in a program to allow the programmer to trace the execution of his program. Whenever program execution is suspended, ODT provides the capability to examine and optionally modify memory locations or registers. Specified areas of memory may be searched by means of ODT's binary memory search mechanism.

OS/78's Batch Processing utility – allows lengthy sequences of commands or frequently used programs to be run automatically on DECstation-78.

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OS/78 BASIC – is high level, easily learned programming language compatible with Dartmouth BASIC. It uses simple English words, abbreviations and familar mathematical symbols to specify operations. BASIC can be used for executing large data processing tasks as well as performing quick, one-time calculations.

BASIC consists of an editor, compiler, and a runtime system, all three supporting BASIC's dual functions as an interactive program development tool and a system for interactive and batch execution. The BASIC instruction set includes powerful, yet simply learned commands which allow novices to do useful programming in a relatively short time. Extended operations and functions, such as program chaining and string operations, allow the more experienced programmer to perform intricate manipulations or express a problem efficiently and concisely.

REAL-TIME MULTITASKING RTS/8

RTS/8 allows DECstation-78 to handle many tasks simultaneously by making use of the otherwise idle processor cycles that occur periodically during a programs execution. A user-defined priority list allows the most important jobs to be processed first. As a result, programs in execution can, if necessary, be temporarily suspended and removed from memory (swapped out) to make room for a higher priority job.

By using RTS/8, the programmer is able to take advantage of a set of software modules that will interface with his hardware, thereby freeing him to concentrate on his own programs and greatly reduce development time. Note: RTS/8 must have OS/78 software as the operating system.

WORD PROCESSING SOFTWARE WPS-8

Word Station 78 is a complete word processing and visual text editing package for use in both stand alone and shared-logic environments. It can be added to the DECstation-78 and includes proven turnkey word processing software. Options include the LQP 78 letter quality printer and a Communications/Optical Character Reader interface which permits the word station to communicate over various grades of communications facilities with host computers or other word stations.

WS78 is powerful yet inexpensive enough to be used as a free-standing word processing system with its own processing capability, local storage and printers. The software is conveniently stored on the system floppy disk. Additonal space on the system floppy disk is reserved for a boilerplate library and a shorthand dictionary. "Shorthand" expressions might be names, addresses, titles, technical words or other standard short units of text that an organization uses repeatedly. These expressions may be stored on floppy disk, recalled with a few keystrokes and automatically inserted into the current text, thereby saving hours of retyping and increasing operator productivity. More than one hundred full pages of typing in as many as 200 separate files may be stored on a document diskette.

Because all the "programming" is in the software, DIGITAL word stations can be used by anyone for productive work after only a day's familiarization with the equipment. A typical stand-alone application, for example, might involve the use a a Word Station 78 in a development facility for the production of reports, documents and correspondence.

Word Station 78 Features:

Software Features:

- "Cue card" prompting of commands via visual display.
- Prestored rulers for margin, printer spacing and tabbing control.
- Format information stored with each document.
- Variety of printer output for mailing labels, envelopes, letterhead, technical manuals, etc.
- Simultaneous printing and editing.
- Justified margins.
- Underlined and overstruck printout.
- Time and date indexing of documents.
- Mailing list generation.
- Form letter merge.
- Insertion of boilerplate material.

Full Editing Features:

- Bi-directional search capabilities.
- Block move ("cut and paste").
- Editing done by grammatical entities – character, word, tab, column, sentence, line, paragraph, or page.
- Decimal point alignment.
- Swap of transposed characters.
- Manual or automatic pagination.

COMMERCIAL OPERATING SYSTEM COS-310

System Software

DIGITAL's Commercial Operating System (COS-310) is a self-contained, disk-resident operating system for small to medium-sized commercial applications. System features include:

- A comprehensive business programming language, DIGITAL's Business-Oriented Language (DIBOL).
- Numerous utilities to simplify program development and create, update, sort/merge and back-up data files.
- Sequential or random file accessing from disk storage.
- User file directories.
- A large system message library.
- Multivolume file support.
- Batch and interactive data processing.

Applications Flexibility

One of the most important characteristics designed and built into DEC COS-310 is flexibility — flexibility that lets 310 tackle a wide range of data processing problems and produce solutions quickly, efficiently, and economically. COS-310's flexibility is shown in its many uses:

- A stand-alone computer system.
- A remote job entry station.
- A "brilliant" terminal functioning as a satellite to a central computer system but having its own totally independent power.

COS-310 also services a wide range of users. Small companies can use COS-310 as their total processing system to perform payroll and other necessary accounting functions. Larger companies can use several DECstation-78's with COS-310 to decentralize their data processing by placing a DECstation-78 at each branch office to handle remote job entry while providing complete formatting and batch processing capabilities on a local level. Banks, insurance companies, manufacturers, warehousing operations — these are just a few of the many users who can profit from the cost-effective performance of COS-310. Standard applications programs are available from DEC as well as from numerous software firms.

The System for Small Companies

In small companies, COS-310 can be used in many applications areas — from order entry and inventory control to accounts payable, accounts receivable, and payroll. It can maintain credit files and information on outstanding orders, accept order entry information keyed in at the video terminal, print the packing tickets, update the inventory file, and generate invoices. COS-310 can also be used to report on back orders and future orders, to describe the company's overall sales picture, to keep track of salesmen's commissions, and to perform sales analysis and related processing tasks.

COS-310 can provide small companies with immediate information when it is needed, not sometime later when the "crisis" has passed. Customers are happier because their orders can be filled faster and more accurately. They receive up-to-date billing information and account statements with no delays — a benefit that means a good cash flow back from customers who want to maintain their credit ratings and/or discounts. Special discounts are easily handled by the system with each customer's account reflecting information that is unique to that company. Customer orders for the future can be entered into COS-310 and automatically processed at the exact time they were requested.

Support Literature

① HARRIS DATA BOOKS

CMOS Microprocessor Data Book

Bipolar and CMOS Memory Data Book

Analog Data Book

② HARRIS MANUALS

Harris Microprocessor Systems Design Manual

MICRO-12 User's Manual

② DEC MANUAL

Introduction to Programming

③ DEC SYSTEM MANUALS

DECstation User's Guide

DECstation Technical Manual

OS/78 User's Manual

RTS-8 User's Manual

Word Processing System Reference Manual

COS-310 System Reference Manual

NOTES:

① Data Books are available from Harris sales representatives and distributors.

② Manuals can be purchased from Harris Semiconductor, Melbourne, Fla. (see order form in back of this Data Book.

③ DEC Systems Manuals are available from DIGITAL Equipment Corporation.

Introduction to DECUS™

OVERVIEW

Since the HM-6100 microprocessor was designed to recognize the instruction set of the Digital Equipment Corporation (DIGITAL) ™ PDP-8/E ™ minicomputer, most programs written for the PDP-8 family are also usable with the HM-6100. The Digital Equipment Computer Users Society (DECUS) provides the vehicle through which HM-6100 and PDP-8 users can exchange ideas, information and user written programs. Harris Semiconductor supports the HM-6100 through participation in the 12-Bit Special Interest Group of DECUS.

HISTORY

DECUS was established in 1961 to " . . . advance the effcient use of DIGITAL computers. It is a voluntary, not-for-profit users group, supported in part by Digital Equipment Corporation."[1]

ACTIVITIES

Symposia

The symposia, which are held throughout the year, provide a forum for users to meet with each other and with DIGITAL management. The papers and presentations are published as DECUS Proceedings shortly after each symposium and provide a permanent record of the meetings activities.

Special Interest Groups (SIGs)

The SIGs promote the interchange of specialized information through the pubilication of newsletters and the coordination of symposia sessions. At the symposiums they sponser business meetings, tutorials, and workshops which fulfill the two-fold purpose of fostering communication among users and between users and DIGITAL. User submitted articles, minutes of local meetings, and letters comprise the major portion of the newseltters. Suggestions, hints, bug fixes, program plans, or questions of a non-commercial nature are suitable material for SIG newsletters.

The 12-Bit Special Interest Group is the vehicle through which users interested in 12-Bit hardware and software can share their ideas. Focus on user interest in HM-6100 related material (such as the DECstation-78) is provided by the MICRO-8 Working Group within the 12-Bit SIG. Various application notes, and hardware and software suggestions are covered in the MICRO-8 section of the 12-Bit SIG newsletter and at the symposia.

Program Library

One of the services performed by DECUS is the maintainence of a large library of programs for DIGITAL computers. The DECUS PDP-8 Program Library Catalog lists over 1200 assembly language and FOCAL ™ programs organized into 17 categories. Included are text editors, assemblers, debuggers, high-level languages (BASIC, FOCAL, ALGOL, SNOBOL, LISP, etc.), operating systems, input/output device handlers, mathematical packages, and various other types of application software.

MEMBERSHIP

Associate

An individual who wishes to join DECUS is eligible for an Associate (non-voting) membership if he has " . . . a bonifide interest in DECUS . . ."[1]. Associate Members receive DECUSCOPE, the Society's Newsletter, automatically. They may receive other DECUS material, such as the 12-Bit SIG Newsletter and the PDP-8 Library Catalog, on request.

Installation

An organization, institution, or individual that has purchased, leased, or has on order a computer manufactured by Digital Equipment Corporation (such as a DECstation-78) is elgible for Installation Membership in DECUS.

TM Trademark Digital Equipment Corporation, Maynard, Ma. 01784

1 DECUS Membership Brochure

Harris Reliability & Quality

µP

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Harris Reliability & Quality

Introduction

The Product Assurance Department at Harris Semiconductor Products Division is responsible for assuring that the quality and reliability of all products shipped to customers meets their requirements. During all phases of product fabrication, there are many independent visual and electrical checks performed by Product Assurance personnel.

Prior to shipment, a final inspection is performed at Quality Assurance Plant Clearance to insure that all requirements of the purchase order and customer specifications are met.

The following military documents provide the foundation for Harris Product Assurance Program.

MIL-M-38510D	"General Specification of Microcircuits"
MIL-Q-9858A	"Quality Program Requirements"
MIL-STD-883B	"Test Methods and Procedures for Microelectronics"
NASA Publication 200-3	"Inspection System Provisions"
MIL-C-45662A	"Calibration System Requirements"
MIL-I-4508A	"Inspection System Requirements"

The Harris Semiconductor Reliability and Quality Manual, which is available upon request, describes the total function and policies of the organization to assure product reliability and quality. All customers are encouraged to visit the Harris Semiconductor facilities and survey the deployment of the Product Assurance function.

Quality Control

All critical processing steps for digital products are subject to rigid process control monitoring.

For example, to insure process stability of CMOS fabrication, frequent qualification of diffusion furnaces, metallization and passivation equipment by C-V plotting techniques is performed. The C-V plot method provides a very sensitive monitor of the amount of ionic contamination present in the processing equipment, and assures clean process with built-in reliability. Process controls of this kind are one reason Harris products have an excellent reliability record.

Another example, in the case of bipolar memory circuits, is the nichrome fusible link process. This process is rigorously controlled by frequent measurements of parameters such as resistivity and dimensions. Consistent and controlled execution of this process has led to very reliable PROMs of high programmability.

The above are only a few of the many process controls instituted to ensure high quality and reliable products. Some other examples are listed below:

- In-line SEM inspection
- Continuous environmental monitoring for particle count, temperature and humidity
- Oxide and metallization thickness measurements
- Doping concentration and profiles
- Pre and post etch inspections
- Prescribed interval calibration and preventative maintenance of processing equipment
- Total documation of specifications and change control procedures

The Product Assurance department also maintains a well equipped Analytical Services Department. This area is equipped with a complete electron microscopy laboratory, including Scanning Electron microscopes with energy dispersive x-ray analysis capability, electron microprobe, a Scanning Auger microscope with ESCA attachment, and all sample preparation equipment. The Analytical Services Department also has a complete physical chemistry

laboratory utilized for analyzing the products and process materials for LSI circuits. Equipment in this section includes atomic absorption flame emission spectrometry, arc emission spectrography, gas chromatography, a research grade talystep, an ultraviolet spectrophotometer and an infrared spectrophotometer. This section also contains a complete wet chemical analysis laboratory.

Further, to ensure high quality metal deposition, critical die areas are monitored via in-process SEM.

Reliability

The reliability approach at Harris Semiconductor is based on designing in reliability rather than testing for reliability only. The latter is applied to confirm that sound design with quality and reliability ground rules are obsreved and correctly executed in a new product design.

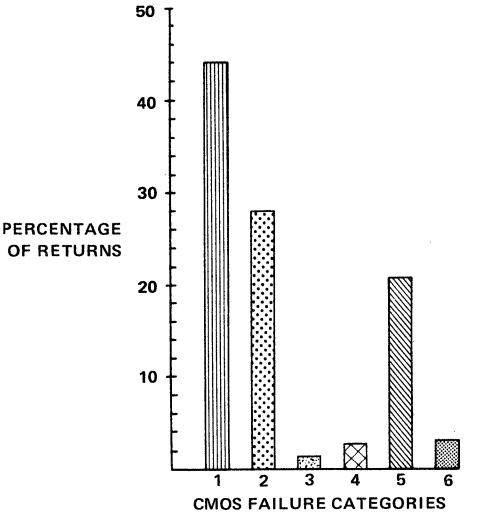
Reliability engineering becomes involved as early as concept review of a new product and continues to remain involved through design and layout reviews. At these critical development points of a new design, basic reliability layout guidelines are invoked to insure an all-around reliable design. This concept is reflected by the Harris reliability procedures which encompass mandatory first run product evaluation. This is done at not only the circuit level, but also at the process and package level. Reliability engineering approval is required before new product designs are released to manufacturing.

Both maximum rated and accelerated stress conditions are performed. Acceleration is important to determine how and at what stress level a new design would fail. From this information, necessary design changes can be implemented to insure a wider and safer margin between the maximum rated stress condition and the device's stress limitation.

The notably low failure rates for all the Harris Semiconductor product lines are a direct result of the application of this reliability concept. Conservatively derating to a typical system condition of +50°C gives a failure rate of 0.020%/1K hrs. for programmed 76XX Bipolar PROMs, a value of 0.013%/1K hrs. for the 65XX CMOS Memory products, and for the CMOS Microprocessor products the rate is 0.015%/1K hrs. The process and layout ground rules are compatible for the Memory and Microprocessor products CMOS lines thus resulting in the expected equivalently low failure rates.

The excellent reliability performance is further exemplified by our customers. Analysis of parts returned to Harris indicates the following results. For the CMOS Microprocessor products and CMOS Memory products, the returns constitute only 0.2% of the total volume shipped.

The accompanying chart illustrates the distribution of categories for why devices are returned. Note that 60-70% of these returned are devices that were not defective as shipped. These units failed due to electrostatic damage (ESD), electrical overstress (EOS), or were good devices which were incorrectly identified as board or system level failures. The latter category is defined as invalid returns and represents 30-40% of the total number of returned units.



CUSTOMER INDUCED PROBLEMS: 73.5% OF RETURNED UNITS

1. INVALID RETURNS 44%
2. ELECTROSTATIC DAMAGE 28%
3. EOS, V_{CC} SPIKES 1.5%

OBSERVED FAILURE MODES 26.5%:

4. ASSEMBLY 2.5%
5. PROCESSING FLAWS 21%
6. TEST ESCAPES 3%

RETURNED UNITS EQUAL ≃0.2% OF TOTAL PARTS SHIPPED

SUMMARY BASED ON RESULTS OBTAINED DURING THE INTERVAL 8/'77 – 3/'78

Section 1. CMOS Reliability/Quality Enhancement

To ensure a totally reliable product and system, the design engineer needs to understand the capabilities and limitations of the CMOS product. In addition, a clear understanding of the techniques employed to improve reliability is essential for High Reliability system goals. The following describes the necessary tools to enhance CMOS reliability.

DESIGNING OUT FAILURE MODES

Static Charge

Since the introduction of MOS, manufacturers have searched for effective and safe ways of handling this sensitive device. High input impedance of CMOS, coupled with gate-oxide breakdown characteristics, result in susceptibility to electrostatic charge damage.

Figure 1 shows a cross-section of silicon gate MOS structure. Note the very thin oxide layer ($\approx$ 1000Å)* present under the gate material. Actual breakdown voltage for this insulating layer ranges from 70 to 100V.

Handling equipment and personnel, by simply moving, can generate in excess of 10kV of static potential in a low humidity environment. Thus, static voltages, in magnitudes sufficient to damage delicate MOS input gate structures, are generated in most handling environments.

A failure occurs when a voltage of sufficient magnitude is applied across the gate oxide causing it to breakdown and destruct. Molten material then flows into the void creating a short from the gate to the underlying silicon. Such shorts occur either at a discontinuity in doping concentration, or at a defect site in the thin oxide. If no problems appear in the oxide, breakdown would most likely occur at gate/source, or gate/drain intersection coincidence due to the doping concentration gradient.

Noncatastrophic degradation may result due to overstressing a CMOS input. Sometimes an input may be damaged, but not shorted. Most of these failures relate to damage of the protection network, not the gate, and show up as increased input leakage.

*1Å (Angstrom = 10^{-8}cm)

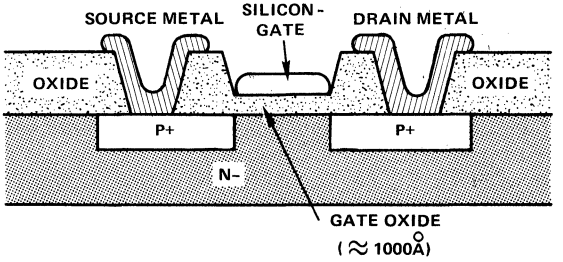


FIGURE 1 — Silicon-gate PFET structure cross-section shows the heavily doped source and drain regions. They are separated by a narrow gap over which lies a thin-gate oxide and gate material.

Voltage Limiting Input Protection

During the evolution of monolithic MOS, manufacturers developed various protection mechanisms that are an integral part of the circuit. However, several of these earlier techniques have been replaced by improved methods now in use. The object of most of these schemes is to prevent damage to input-gate structures by limiting applied voltages.

Recent CMOS designs employ a dual-diode concept in their input protection networks. Figure 2 illustrates such a protection circuit.

One characteristic of junction-isolated CMOS protection circuits is the $\approx 200\Omega$ current limiting resistor. Cross sectional area of the metallization leading to the resistor, and the area of the resistor are, therefore, designed to absorb discharge energy without sustaining permanent damage. This dual-diode protection has proved very effective and is the most commonly used method in production today.

HARRIS INPUT GATE PROTECTION

To protect input device gates against destructive overstress by static electricity accumulating during handling and insertion of CMOS products, Harris provides a protection circuit on all inputs. The general configuration of this protection circuit is shown in Figure 2.

Both diodes to the V_{DD} and V_{SS} lines have breakdown voltages averaging between 35 and 40 volts. Excessive static charge accumulated on the input pin is thus effectively discharged through these diodes which limit the voltage applied from gate to drain and source. The 200 ohm resistor provides current limiting during discharge. Depending on the polarity of the input static charge and on which of the supply pins is grounded, the protective diodes may either conduct in the forward direction or breakdown in the reverse direction.

In order to test this concept, step stress tests have been performed at Harris using an approximate equivalent circuit to simulate the static charge encountered in handling operations. The equivalent circuit consists of a 100pF capacitor in series with a 1.5K ohm resistor and is considered the rough equivalent of a human body. Step stressing takes the form of charging the capacitor to a given voltage and then discharging it into an input pin of the CMOS device under test according to the sequence given in MIL-STD-38510.

Stress Voltage	Cumulative Failures
500	0
700	0
1000	0
1500	1
1700	3
1800	4

These results indicate that the input protection used for Harris CMOS products provides adequate protection against static electricity based on the limits specified in MIL-STD-38510.

There are two trade-offs to consider when fabricating an input protection scheme. Effectiveness of the overvoltage protection, and performance of the overall circuit. It is obvious that increasing series resistance and capacitance at an input limits current. This, in turn, increases the input protection's ability to absorb the shock of a static discharge. However, such an approach to protection can have a significant effect on circuit speed and input leakage. The input protection selected must provide a useful performance level and adequate static-charge protection.

Commonly used MOS-input protection circuits all have basic characteristics that limit their effectiveness. The zener diodes, or forward-biased pn-junctions, employed have finite turn-on times too long to be effective for fast rise-time conditions. A static discharge of 1.5kV into a MOS input may bring the gate past its breakdown level before the protection diodes or zener becomes conductive.

Actual turn-on times of zeners and pn-diodes are difficult to determine. It is estimated that they are a few nanoseconds and a few tens of picoseconds, respectively. A low-impedance static source can easily produce rise times equal to or faster than these turn-on times. Obviously the input time constant required to delay buildup of voltage at the gate must be much higher for zener, or other schemes having longer turn-on times.

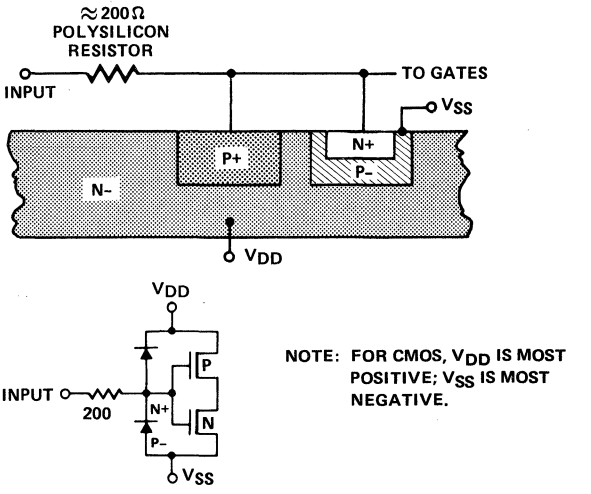


FIGURE 2 – Junction isolated dual-diode protection networks are most commonly used in today's CMOS circuits.

Consider an example. Figure 3 shows a test circuit that simulates the discharge of a 1.5kV static charge into a CMOS input. Body capacitance and resistance of the average worker is represented by a 100pF capacitor through 1.5kΩ. Switch A is initially closed, charging 100pF to 1.5kV with switch B open. Switch A is opened, then B is closed, starting the discharge. With the 1.5KΩ x 5pF time constant to limit the charge rate at the DUT input, it would take approximately 350psec to charge to 70V above V_{DD}. Diode turn-on time is much shorter than 350psec, hence the gate node would be clamped before any damage could be sustained.

There is no completely foolproof system of chip-input protection presently in production. If static discharge is of high enough magnitude, or sufficiently short rise-time, some damage or degradation may occur. It is evident, therefore, that proper handling procedures should be adopted.

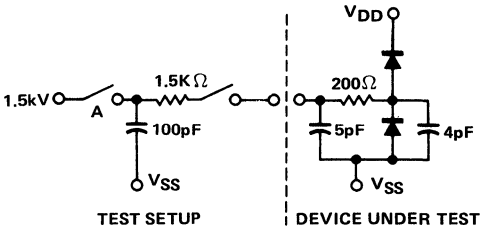


FIGURE 3 – Input protection network test setup illustrates how diode clamping prevents excessive voltages from damaging the CMOS device.

HANDLING RULES

Elimination or reduction of static charge can be accomplished as follows:

- Use conductive work stations. Metallic or conductive plastic* tops on work benches connected to ground help eliminate static build-up.
- Ground all handling equipment.
- Ground all handling personnel with a conductive bracelet through 1MΩ to ground. The 1MΩ resistor will prevent injury.
- Smocks, clothing, and especially shoes of certain insulating materials (notably nylon) should not be worn in areas where devices are handled. These materials, highly dielectric in nature, will hold or aid in the generation of a static charge.
- Control relative humidity to as high a level as practical. A higher level of humidity helps bleed away any static charge as it collects.
- Ionized air blowers reduce charge build-up in areas where grounding is not possible or deisrable.
- Devices should be in conductive carrriers during all phases of transport. Leads may be shorted by tubular metallic carriers, conductive foam or foil.
- In automated handling equipment, the belts, chutes, or other surfaces the leads contact should be of a conducting nature. If this is not possible, ionized air blowers may be a good alternative.

THE FORWARD-BIAS PHENOMENON

Monolithic CMOS integrated circuits employ a single-crystal silicon wafer into which FET sources and drains are implanted. For complex functions many thousands of transistors may be required and each must be electrically isolated for proper operation.

Junction techniques are commonly used to provide the required isolation – each switching node operating reverse-biased to its respective substrate material. Additionally, as previously mentioned, protection diodes are provided to prevent static-charge related damage where inputs interface to package pins. Forward-biasing any of these junctions with or without power applied may result in malfunction, parametric degradation, or damage to the circuit.

*Supplier: 3M Company "Velostat".

Before proceeding, it should be pointed out that junction isolation, in the classical sense, is not implemented in the CMOS structure. Although commonly called junction isolation, the CMOS technique varies substantially from that used in bipolar TTL (Figure 4).

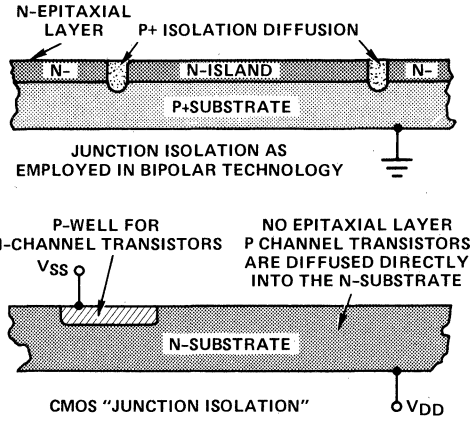


FIGURE 4 — Junction isolation for bipolar and CMOS differ considerably. CMOS utilizes a simpler technique that takes advantage of its less complex processing.

ELECTROMIGRATION AND FUSING

An aluminum metallization system is used for on-chip interconnect and wire bonding of most CMOS integrated circuits. On-chip metallization means a very pure grade of aluminum deposited on the surface of a silicon wafer. A subsequent metal etch defines the interconnect pattern.

This on-chip metallization can be subject to two primary current-density related failure modes, electromigration and fusing.

6

Electromigration results from displacement of metal atoms due to high current densities. Displacement of atoms creates physical holes in the metal structure that enlarge with time, eventually causing an open circuit. Under extreme circumstances, displacement can be sufficient to short to an adjacent line. Current density levels for which circuit life is not impaired are subjects of considerable debate. One figure, generally considered to be ultra-safe, is $10^5 A/cm^2$.

Considerably higher current densities, on the order of $10^6 - 10^8 A/cm^2$, are required to cause fusing. For a 0.3 mil wide, 40 μ inch thick aluminum line and a fuse current density of $10^7 A/cm^2$, 775mA will cause fusing. Current levels of this magnitude are not generated during normal CMOS operation.

Could a high-energy static discharge into a CMOS input or output cause fusing ? Yes, but such a failure would most likely occur due to heavily forward-biasing an input or output through a low impedance.

High currents resulting from an excessive forward-bias can cause severe overheating localized to the area of a junction. Damage to the silicon, overlying oxide and metallization can result.

BIPOLAR PARASITICS

Care must always be exercised not to forward-bias junctions from input or output pads.

A complex and potential defect phenomenon is the interaction of a npn/pnp combination a la SCR (Figure 5). Forward-biasing the base-emitter junction of either bipolar component can cause the pair to latch-up if βnpn x βpnp ≥ 1. The resultant low impedance between supply pins can cause fusing of metallization or over-dissipation of the chip.

Figure 5 shows how an SCR might be formed. The p+ diffusion labeled INPUT is connected to aluminum metallization and bonded to a package pin. Biasing this point positive with respect to V_{DD} supplies base drive to the pnp through $R2$. Although gain of these lateral devices is normally very low, sufficient collector current may be generated to forward-bias and supply substantial base current to the vertical npn parasitic. Once the pair has been activated, each member provides the base current required to sustain the other. A latched condition will be maintained until power is removed or circuit damage disables further operation.

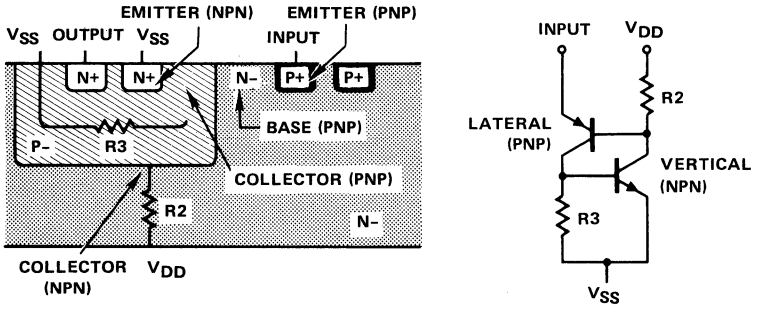


FIGURE 5 — Improper biasing can latch-up this SCR configuration. A p+ guard ring is commonly used to kill lateral pnp action. This ring is diffused into the surface at the junction of p- and n- silicon.

DESIGN RULES EQUALLY IMPORTANT AS HANDLING RULES

A system using CMOS must have reliability designed in. No amount of testing can guarantee long term reliability when poor design practices are evident.

- Never apply signals to a CMOS circuit before power has been turned on.
- Supply filter capacitance should be distributed such that some filtering is in close proximity to supply pins of each package. Testing has shown 0.01 μF/package to be effective in filtering noise generated by most CMOS functions.
- CMOS signal lines are terminated at the driving end by a relatively high impedance when operating at the low end of the supply voltage range. This high-impedance termination results in vulnerability to high-energy or high-frequency noise generated by bipolar or other non-CMOS components. Such noise must be held to manageable levels on both CMOS power and signal lines.
- Where CMOS must interface between logic frames or between different equipments, ground differences must be controlled in order to maintain operation within absolute maximum ratings.

- Capacitance on a CMOS input or output will result in a forward-bias condition when power is turned off. This capacitance must discharge through forward-biased input or output to substrate junctions as the bus voltage collapses. Excessive capacitance (thousands of pF) should be avoided as discharging the stored energy may generate excessive current densities during power-down.
- Where forward-biasing is inevitable, current limiting should be provided. Current should not be permitted to exceed 1mA on any package pin excluding supply pins.

All CMOS is susceptible to damage due to electrical overstress. It is the user's responsibility to follow a few simple rules in order to minimize device losses.

He should first select a source for the CMOS device that employs an effective input protection scheme. This will allow a greater margin of safety at all levels of device handling since the devices will not be quite so prone to static charge damage. Next, he should apply a sound set of handling and design rules. At minimum, this will eliminate electrical stressing or hold it to manageable levels.

With an effective on-chip protection scheme, good handling procedures and sound design, users should not lose any CMOS devices to electrical overstress.

Section 2. Reliability Screening Programs

Reliability Screening Programs

Facility Qualification

Harris is closely attuned to the requirements of military quality and reliability manufacturing programs. Our facilities and its quality plan is well accepted at all major companies. In addition, we have JAN qualification in the Bipolar Memory area and have JAN qualifications in process on CMOS Memory and Linear products.

MIL-STD-883 Class B (Dash 8)

As a special service to users of high rel products Harris makes instantly available high reliability on many of our product lines. Simply by adding its postscript -8 to appropriate Harris part numbers "off the shelf" delivery can be obtained of products screened to MIL-STD-883 Method 5004 Class B.

To meet our commitment to CMOS growth, Harris has introduced the Hi-Rel Dash 8 program. This program is designed to meet the needs of the customer seeking enhanced quality and reliability by additional screening steps.

This program is designed for:

- Customers using a current reliability add-on program.
- For the individual seeking a trade-off between additional cost and improved reliability and quality through screening — Harris gives a broad selection from Class B flow to burn-in only.

The Harris Hi-Rel Program is a comprehensive program aimed at serving the various needs of many customers. With the increasing need for improved IC systems mean time to failure performance, the Hi-Rel program assures high quality and reliability of CMOS circuits.

Harris CMOS devices have been produced for over 6 years in modern state of the art manufacturing facilities. Our implemented second and third generation mask designs with the experience of well-controlled processes, results in standard products with built-in reliability. Coupling Harris CMOS with a Hi-Rel program will result in an enhanced combination for quality and reliability.

User Benefits

- Eliminates user screening programs
- Provides uncomplicated incoming inspection
- Reduces infant mortality and board rework
- Reduces field failures and unnecessary maintenance costs

Quality

In theory, parts tested 100 percent should upon receipt at the user's site be 100 percent good. Due to mass production there may exist a small percentage of parts which escape 100 percent tests. The AQL or LTPD outgoing sampling plans at Harris have been very successful in stopping the DOA's (Dead on Arrival). For the user with complex systems using large quantities of products, a quality enhancement can be tailored into your specific Hi-Rel program by choosing tightened sampling plans. The tightened quality test plan ensures close maintenance of the improved quality level through careful product segregation and retesting.

Reliability

Experience and perfected process controls have built reliability into a standard Harris CMOS product. Reliability cannot be tested into a part. Quality level may be improved by retesting and tighter sampling plans. However, reliability is improved by proper design and observance of sound ground rules, controlled processes and finally by stress testing to confirm claimed reliability performance. The Hi-Rel program offers a varied mix of stress tests to compress time and weed out devices subject to infant mortality. The equivalent early life failures are removed by the various screens such as temperature cycling, stabilization bake, burn-in and high temperature functional testing. Some or all of these stress tests will remove early failures and thus improve overall system reliability.

INTRODUCTION

Statement of Scope

This section establishes the detail requirements for Harris' circuits screened and tested under the Product Assurance Program.

The Harris DASH 8 Devices pass the screening requirements of the latest issue of MIL-STD-883, Method 5004, Class B, and the requirements as specified in this document. Included in this section are the quality standards and screening methods for commercial parts which must perform reliably in the field.

Applicable Documents

The following Military documents form a part of this section to the extent referenced herein and provide the foundation for Harris Products Assurance Program.

MIL-M-38510	"General Specification for Microcircuits"
MIL-Q-9858A	"Quality Program Requirements"
MIL-STD-883	"Test Methods and Procedures for Microelectronics"
NASA Publication 200-3	"Inspection System Provisions"

Harris maintains a Product Assurance Program (PAP) using MIL-M-38510 as a guide. Harris Product Assurance Program assures compliance with the requirements and quality standards of control drawings and the requirements of this specification.

The DASH 8 Program will also be found useful by those Harris customers who must generate their own procurement specifications. Use of the enclosed Harris Standard Test Tables, Test Parameters, and Burn-In Circuits will aid in reducing specification negotiation time.

PRODUCT ASSURANCE AT HARRIS

Our Product Assurance Department strives to assure that the quality and reliability of products shipped to customers is of a high quality level and consistent with customer requirements. During product processing, there are several independent visual and electrical checks performed by Quality Assurance personnel.

Prior to shipment, a final inspection is performed at Quality Assurance Plant Clearance to insure that all requirements of the purchase order and customer specifications are met. The system and procedures used and implemented are in accordance with MIL-M-38510, MIL-Q-9858A, MIL-STD-883A, MIL-C-45662 and MIL-I-45208.

The Harris Semiconductor Reliability and Quality Manual which is available upon request, describes the total function and policies of the organization to assure product reliability and quality.

HARRIS SEMICONDUCTOR DASH 8 PRODUCT FLOW
MIL-M-38510/MIL-STD-883, METHOD 5004 CLASS B

100% SCREENING PROCEDURE

	SCREEN	MIL-STD-883 METHOD/COND.
1	Internal Visual	2010 Cond. B.
2	Stabilization Bake	1008 Cond. C (24 hrs. minimum)
3	Temperature Cycling	1010 Cond. C
4	Constant Acceleration	2001 Cond. E; Y1 plane 40 Pin Cerdip, Cond. C; Y1 plane
5	Seal: (A) Fine (B) Gross	1014 Cond. A or B 1014 Cond. C2
6	Initial Electrical	Harris Specifications
7	Burn-In Test	1015, 160 hrs. @ 125°C (or equivalent) (Burn-In circuits enclosed)
8	Final Electrical 100% go-no-go	Tested at Worst Case Operating Conditions
9	External Visual	2009 Sample Inspection
10	Lot Acceptance	Table I, Group A Elect. Tests

Note:

Traceability: All devices are assigned date code identification that provides traceability back to the inspection lot.

Branding: All devices are branded with the HX-XXXX-8 and EIA date code.

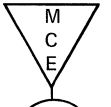
Aged Products: Product that has been held for more than 24 months will be reinspected prior to shipment to group A inspection requirements.

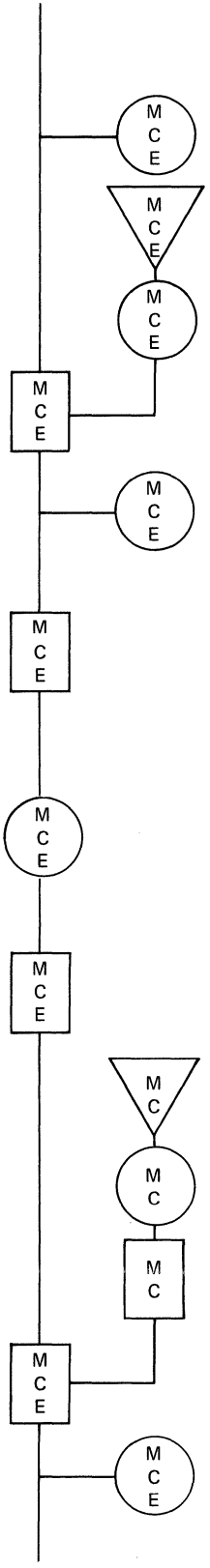
Additional Requirements: Attributes data will be supplied on Group A Lot Acceptance upon request.

Generic data from Harris' Reliability Add-On Program is available upon request. The objective of Harris Reliability Add-On Program is to provide a continuous life and environmental monitor for all products families in manufacturing. This program provides life test performance results to fullfill reliability data requirements and to verify package integrity. The Reliability Add-On Program is supplemental to customer funded Lot Qualification.

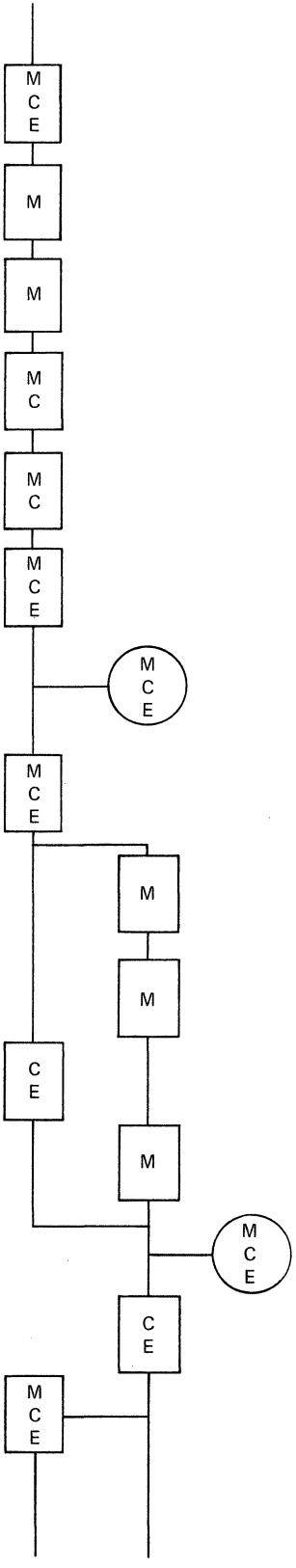
For customers desiring Lot Qualification, Harris Semiconductor will perform Group A, B, C and D inspections to MIL-STD-883, Method 5005 as defined herein for an additional charge.

STANDARD PRODUCTS SCREENING AND INSPECTION PROCEDURE

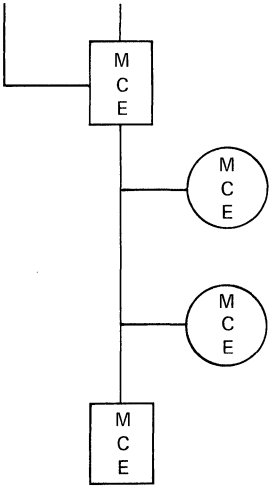
OPER. SEQ.	OPER. DESCRIPTION	PRODUCT CATEGORIES		
		MIL (M)	COMM (C)	EPOXY (E)
	Incoming Material Silicon and Chemical Procurement.	X	X	X
	Q.C. Incoming Inspection. Materials are Inspected for Conformance to Specified Requirements.	X	X	X
	Manufacturing Wafer Fabrication	X	X	X
	QC • DIH_2O & Gas Monitor • SEM Process Control • Wafer Process Control	X	X	X
	Manufacturing, Wafer Electrical Probe (100%)	X	X	X
	Manufacturing, Wafer Scribe, Break (100%)	X	X	X
	Manufacturing Dice Screen (100%)	X	X	X
	QA Dice Inspection Control	X	X	X
	Preform Procurement Package Procurement Leadframe Procurement Epoxy Compound Procurement	X X	X X	N/A N/A X X
	Q.C. Preform Inspection Q.C. Package Inspection Q.C. Leadframe Inspection	X X	X X	N/A N/A X
	Manufacturing Package Clean	X	X	N/A
	Manufacturing Die Mounting	X	X	X



QA Die Mount Control (continuous sampling) • Visual Die Inspection	X	X	X
Bond Wire Procurement	X	X	X
Q.C. Wire Inspection (receiving)	X	X	X
Manufacturing Wire Bonding	X Al	X Al	X Au
QA Bond Control (continuous sampling) • Visual Die & Bond Inspection • Wire and Pull Test	X	X	X
Manufacturing Pre-Seal Screen (100%)	MS883 Method 2010 Cond. A or B	MS883 Method 2010 HS Mod. Cond. B	MS883 Method 2010 HS Mod. Cond. B
QA Pre-Seal Inspection Lot Acceptance	MS883 Method 2010 Cond. A or B	MS883 Method 2010 HS Mod. Cond. B	MS883 Method 2010 HS Mod. Cond. B
Preseal Bake Per MS-883, Method 1008, Cond. C	8 hr.	4 hr.	4 hr.
Package Lid Procurement	X	X	N/A
Package Lid Inspection	X	X	N/A
Package Lid Clean	X	X	N/A
Package Seal/Encapsulation	X	X	X
QA Package Seal/Encapsulated Control (continuous sampling)	X	X	X



Stabilization Bake MS-883, Method 1008, Cond. C.	24 hr.	8 hr.	8 hr.
Temperature Cycle, MS-883, Method 1010, Cond. C,	X	X	N/A
Centrifuge, MS-883, Method 1010, (Y1) Plane 30 KG's min. 40 Pin Cerdip Package 5H 15 KG's min.	100%	X	N/A
Fine Leak, MS-883, Method 1014	100%	X	N/A
Gross Leak, MS-883, Method 1014 Condition C2	100%	X	N/A
Frame Removal & Loading Units In Carriers/Sticks	X	X	X
Final QA Lot Inspection, MS-883 Method 1014 • Fine & Gross Leak • Visual/Mechanical Inspection	X	X	X
Group A Initial Tests 1.	X	X	X
Brand Device Type/Date Code Serialize, If Applicable	X	N/A	N/A
Burn-In (100%), MS-883, Method 1015	Classes A/B Products	N/A	N/A
Group A Final Test (100%) (Worst Case Oper. Cond.)	X	N/A	N/A
QA Acceptance Elec. Testing • Visual/Mechanical Method 2009 Lot Sampling	X	X	X
Brand Devices Type/Date Code	N/A	X	X
Controlled Inventory	X	X	X



Package for Shipment	X	X	X
Quality Conformance Inspection Group B/C/D Testing, MS-883, Method 5005, Periodically or by Customer P.O. Request	X	X	X
QA Plant Clearance • Final Visual of Marking and Physical Quantity, Conformation of Product by Inspection or Sample Test	X	X	X
Ship to Customer	X	X	X

NOTE: 1. Group A – Table 1, Subgroup 2 & 10 for CMOS.

HARRIS COMMERCIAL GRADE PRODUCTS

This product is processed on the same wafer fabrication lines, to the same thorough specification and rigid controls as HI-Rel parts. At wafer electrical probe the product may be categorized for electrical performance, such as temperature range of operation or maximum output (see specific product data sheet for grading details) by utilizing multiple colored inks. Defective die are inked with red ink, but, for example, die meeting the commercial temperature range electrical specifications may be inked with green ink.

The die are then visually inspected and sorted after die separation to a modified Class B visual criteria. They are then assembled in packages on a controlled assembly line. The ink used to categorize product performance, such as the green ink, might not be removed from the commercial grade die. This ink has been chemically characterized as inert and reliability verification confirms there is no effect on performance or operating life of the parts.

Harris invites any interested customer to review our assembly flow and facilities for information, quality survey, or certification.

TABLE I – GROUP A ELECTRICAL TESTS [1]

SUBGROUP[2]	CLASSES S & B LTPD	CLASS C LTPD
Subgroup 1 Static Tests at 25°C	5	5
Subgroup 2 Static Tests at Maximum Rated Operating Temperature	7	10
Subgroup 3 Static Tests at Minimum Rated Operating Temperature	7	10
Subgroup 7 Functional Tests at 25°C	5	5
Subgroup 8 Functional Tests at Maximum and Minimum Rated Operating Temperatures	10	15
Subgroup 9 Switching Tests at 25°C	7	10
Subgroup 10 Switching Tests at Maximum Rated Operating Temperature	10	15
Subgroup 11 Switching Tests at Minimum Rated Operating Temperature	10	15

1. The specific parameters to be included for tests in each subgroup shall be as specified in the applicable procurement document. Where no parameters have been identified in a particular subgroup or test within a subgroup, no group A testing is required for that subgroup or test to satisfy group A requirements.

2. A single sample may be used for all subgroup testing. Where the required size exceeds the lot size, 100% inspection shall be allowed (see 30.2.5 of Appendix B of MIL-M-38510).

TABLE II – GROUP B TESTS (LOT RELATED) [1.]

TEST	MIL-STD-883 METHOD	MIL-STD-883 CONDITION	LTPD*
Subgroup 1			
Physical Dimensions	2016		2 Devices (No Failures)
Subgroup 2			
a. Resistance to Solvents	2015		3 Devices (No Failures)
b. Internal Visual and Mechanical	2014	Failure Criteria from Design and Construction Requirements of Applicable Procurement Document.	1 Device (No Failures)
c. Bond Strength [2.]			
(1) Thermocompression	2011	(1) Test Condition C or D	15
(2) Ultrasonic or Wedge		(2) Test Condition C or D	
(3) Beam Lead		(3) Test Condition H	
Subgroup 3			
Solderability [3.]	2003	Soldering Temperature of 260 ±10°C	15

NOTES:

1. Electrical reject devices from the same inspection lot may be used for all subgroups when end point measurements are not required.
2. Test samples for bond strength may, at the manufacturer's option unless otherwise specified be randomly selected immediately following internal visual (precap) inspection specified in method 5004, prior to sealing.
3. All devices submitted for solderability test must have been through the temperature/time exposure specified for burn-in. The LTPD for solderability test applies to the number of leads inspected except in no case shall less than 3 devices be used to provide the number of leads required.
4. Generic data from Harris Reliability Add-On Program in the form of Reliability Bulletins are available upon request.

* Reference Note – Table 1*

TABLE III – GROUP C (DIE-RELATED TESTS)

TEST	MIL-STD-883 METHOD	MIL-STD-883 CONDITION	LTPD*
Subgroup 1			
Operating Life Test	1005	Test Condition to be specified (1000 Hrs)	5
End Point Electrical Parameters		Table I – Subgroup 1	
Subgroup 2			
Temperature Cycling	1010	Test Condition C	15
Constant Acceleration	2001	Test Condition E, 40 Pin Cerdip, Cond. C Y_1 Axis	
Seal	1014	As Applicable	
(a) Fine			
(b) Gross 2.			
Visual Examination	1.		
End Point Electrical Parameters		Table I – Subgroup 1	

6

NOTES:

1. Visual examination shall be in accordance with method 1010.
2. When fluorocarbon gross leak testing is utilized, test condition C_2 shall apply as minimum.
3. Generic data from Harris Reliability Add-On Program in the form of Reliability Bulletins are available upon request.

* Reference Note - Table 1 *

TABLE IV – GROUP D (PACKAGE RELATED TESTS)

TEST	MIL-STD-883 METHOD	MIL-STD-883 CONDITION	LTPD*
Subgroup 1			
Physical Dimensions	2016		15
Subgroup 2 [4.]			
Lead Integrity	2004	Test Condition B2 (Lead Fatigue)	15
Seal	1014	As Applicable	
(a) Fine			
(b) Gross [6.]			
Subgroup 3 [1.]			
Thermal Shock	1011	Test Condition B as a Minimum, 15 Cycles Minimum.	15
Temperature Cycling	1010	Test Condition C, 10 Cycles Minimum	
Moisture Resistance	1004	Omit Initial/Conditioning and Vibration	
Seal	1014	As Applicable	
(a) Fine			
(b) Gross [6.]			
Visual Examination	2.		
End Point Electrical Parameters		Table I – Subgroup 1	
Subgroup 4 [1.]			
Mechanical Shock	2002	Test Condition B	15
Vibration Variable Frequency	2007	Test Condition A	
Constant Acceleration	2001	Test Condition E, 40 Pin Cerdip, Cond. C	
Seal	1014	As Applicable	
(a) Fine			
(b) Gross [6.]			
Visual Examination	3.		
End Point Electrical Parameters		Table I – Subgroup 1	
Subgroup 5 [4.]			
Salt Atmosphere	1009	Test Condition A	15
Visual Examination	5.		

NOTES:

1. Devices used in subgroup 3, "Thermal and Moisture Resistance" may be used in subgroup 4, "Mechanical".
2. Visual examination shall be in accordance with method 1010 or 1011 at a magnification of 5X to 10X.
3. Visual examination shall be performed in accordance with method 2007 for evidence of defects or damage to case, leads, or seals resulting from testing (not fixturing). Such damages shall constitute a failure.
4. Electrical reject devices from that same inspection lot may be used for samples.
5. Visual examination shall be in accordance with paragraph 3.3.1 for method 1009.
6. When fluorocarbon gross leak testing is utilized, test condition C_2 shall apply as minimum.
7. Generic data from Harris Reliability Add-On Program in the form of Reliability Bulletins are available upon request.

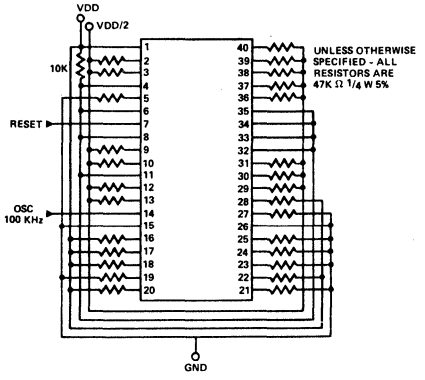
* Reference Note - Table 1 *

Section 3. Burn-In Circuits

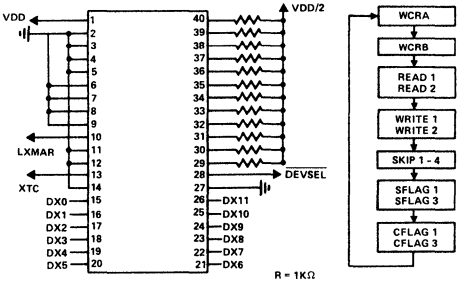
Burn-In Circuit Index

		Drawing No.
MICROPROCESSOR FAMILY		
HM-6100	CMOS 12 Bit Microprocessor (CPU)	1
HD-6101	CMOS Parallel Interface Element (PIE)	2
HD-6102 (Advance)	Memory Extension/DMA/Interval Timer/Controller (MEDIC)	
HD-6103 (Advance)	CMOS Parallel Input/Output Port (PIO)	
MEMORY FAMILY		
HM-6312	CMOS ROM 1024 Word x 12 Bit	3
HM-6512	64 x 12 CMOS RAM	4
HM-6561	256 x 4 CMOS RAM	5
HM-6518	1024 x 1 CMOS RAM	6
HM-6533	1024 x 4 CMOS RAM	7
HM-6543	4096 x 1 CMOS RAM	8
INTERFACE FAMILY		
HD-4702	CMOS Programmable Bit Rate Generator	9
HD-6402	CMOS/LSI Universal Asynchronous Receiver Transmitter (UART)	10
HD-6405	CMOS Programmable Bit Rate Generator	9
HD-6408	CMOS Asynchronous Serial Manchester Adapter (ASMA)	11
HD-6431	CMOS Hex Latched Bus Driver	12
HD-6432	CMOS Hex Bi-directional Bus Driver	13
HD-6433	CMOS Quad Bus Transceiver	14
HD-6434 (Advance)	CMOS Octal Resettable Latched Bus Driver	15
HD-6435 (Advance)	CMOS Hex Resettable Latched Bus Driver	16
HD-6436 (Advance)	CMOS Octal Bus Buffer Driver	17
HD-6440	CMOS Latched 3 to 8 Line Decoder Driver	18
HD-6495	CMOS Hex Bus Driver	19

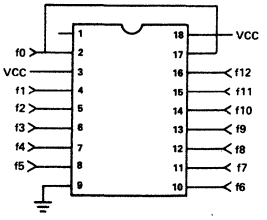
1 HM-6100



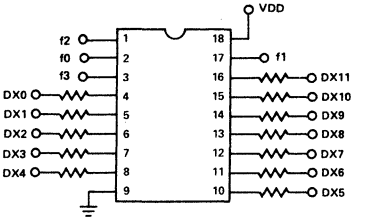
2 HD-6101



3 HM-6312

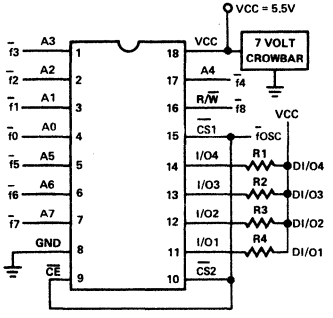


4 HM-6512



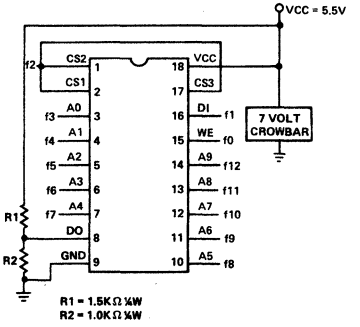
ALL RESISTORS ARE 47KΩ ,¼ WATT, ±10%

5 HM-6561



R1, R2, R3, R4 = 10KΩ ¼W

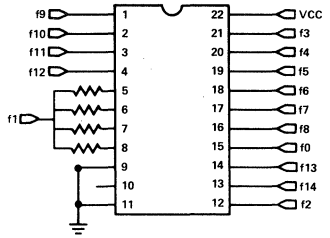
6 HM-6518



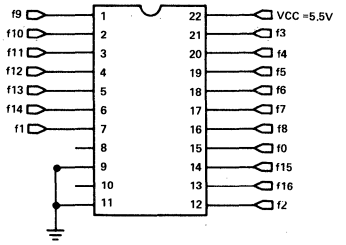
R1 = 1.5KΩ ¼W
R2 = 1.0KΩ ¼W

6

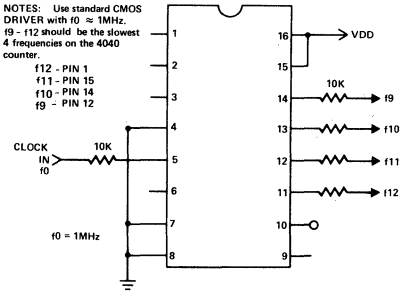
7 HM-6533



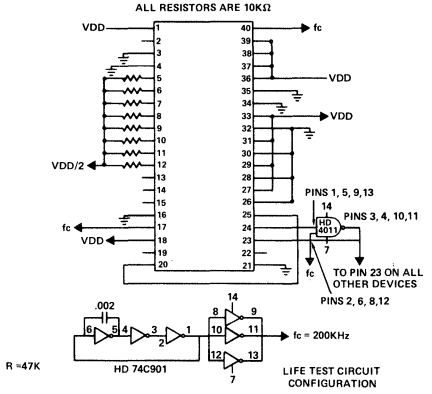
8 HM-6543



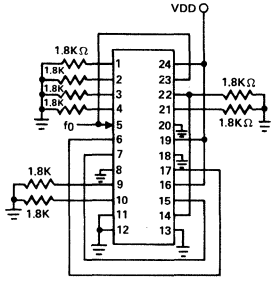
9 HD-4702 HD-6405



10 HD-6402

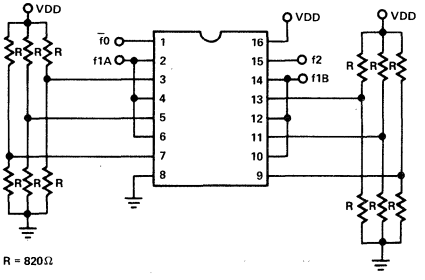


11 HD-6408

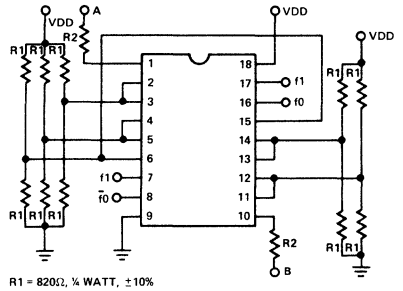


All load resistors on the HD-6408 are 1.8KΩ 20% 1/4 watt.

12 HD-6431

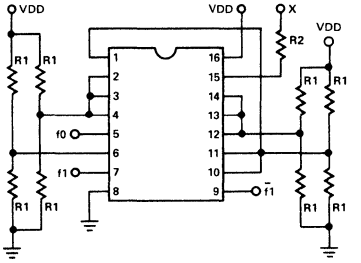


13 HD-6432



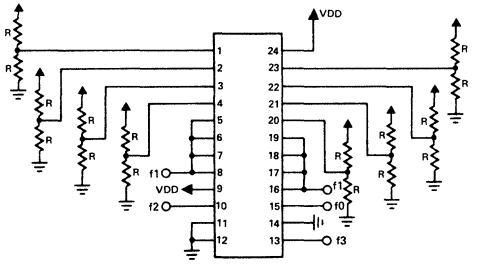
R1 = 820Ω, ¼ WATT, ±10%
R2 = 910Ω, ¼ WATT, ±10%

14 HD-6433

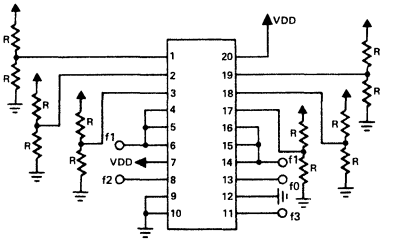


R1 = 820Ω, ¼ WATT, ±10%
R2 = 910Ω, ¼ WATT, ±10%

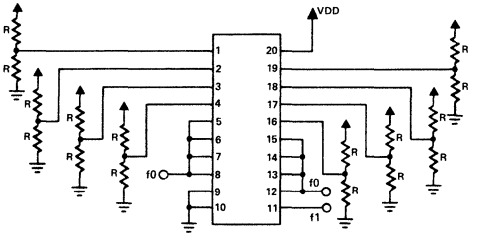
15 HD-6434 (ADVANCE)



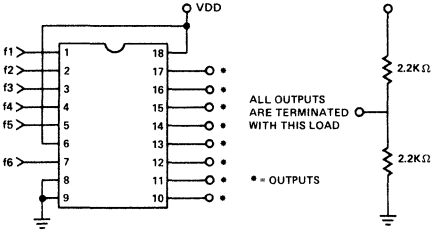
16 HD-6435 (ADVANCE)



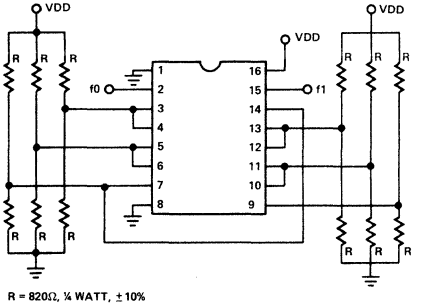
17 HD-6436 (ADVANCE)



18 HD-6440



19 HD-6495



R = 820Ω, ¼ WATT, ±10%

6

Ordering & Packaging

µP

Component Ordering Information	7—2
System Ordering Information	7—2
Package Selection Guide	7—3
Package Dimensions	7—4

Component Ordering Information

H M 1 - 6100 A - 2

PREFIX:
H - Harris

FAMILY:
A - Analog
C - Communications
D - Digital
I - Interface
M - Memory

PACKAGE CODE:
0 - Chip Form
1 - Ceramic
3 - Epoxy
4 - Leadless Carrier
9 - Flatpack

PART NUMBER:
0XXX - Diode Matrices
61XX - Microprocessor
63XX - CMOS ROMs
64XX - CMOS Interface
65XX - CMOS RAMs
66XX - CMOS PROMs
76XX - Bipolar PROMs

VERSION:
A - 10.0V Nominal
C - Relax 5.0V Nominal
Blank - 5.0V Nominal

TEMPERATURE:
2 - -55°C to +125°C
5 - 0°C to +75°C
6 - 100% 25°C Probe
8 - Dash 8 Program Mil. Std. 883B
9 - -40°C to +85°C

System Ordering Information

H B 0 - 61000 - 1

PREFIX:
H - Harris

FAMILY:
B - Board & Systems
Z - Documentation

PACKAGE CODE:
0 - Systems

PART NUMBER:
61XXX - Systems

OPTION:
61000-1 - Basic system with 256 words memory
61000-4 - Basic system with 1024 words memory & parallel I/O port
61000-5 - Basic system with 256 words memory & parallel I/O port in kit form
61001-1 - 4096 word CMOS memory
61001-2 - 2048 word CMOS memory

7

HARRIS DASH 8 PROGRAM

As a service to users of High Rel products, Harris makes readily available via the high reliability DASH 8 program many products from our product lines. Parts screened to MIL-STD-883 Method 5004 Class B are simply branded with the postscript "-8" to the appropriate Harris part numbers, in effect, offering "off the shelf" delivery. For details concerning this special Harris program for High Rel users, see the Dash 8 section of this Data Book.

SPECIAL ORDERS

For best availability and price, it is urged that standard "Product Code" devices be specified, which are available worldwide from authorized distributors. Where enhanced reliability is needed, note standard "Dash 8" screening described in the Data Book. Harris application engineers may be consulted for advice about suitability of a part for a given application.

If additional electrical parameter guarantees or reliability screening are absolutely required, a Request for Quotation and Source Control Drawing should be submitted through the local Harris Sales Office or Sales Representative. Since many electrical parameters may be economically assured through design analysis, characterization, or correlation with other parameters should be labeled "Vendor will guarantee, but not necessarily test".

Harris reserves the right to decline to quote or to request modification to special screening requirements.

Package Selection Guide

	1*	3*	4*	9*	9*
PRODUCT	CERDIP	EPOXY	LEADLESS	FLATPACK †	CERPACK †
Microprocessor Family					
HM-6100	4J (5H)**	3H	LG	9X	8P
HD-6101	4J (5H)**	3J	LG	9X	8P
HD-6102 (Advance)	4J (5H)**	3J			
HD-6103 (Advance)	4J (5H)**	3J			
Memory Family					
HM-6312	4G	3D	LA	9D	8C
HM-6512	4N	3D	LA	9D	8C
HM-6561	4N	3D	LA	9D	8C
HM-6518	4N	3D	LA	9D	8C
HM-6533	4M	3E	LC	9E	8K
HM-6543	4M	3E	LC	9E	8K
Interface Family					
HD-4702	4Z	3L	LA	9B	8B
HD-6402	4J (5H)**	3J	LG	9X	8P
HD-6405	4Z	3L	LA	9B	8B
HD-6408	4K	3F			
HD-6431	4Z	3L	LA	9B	8B
HD-6432	4N	3D	LA	9D	8C
HD-6433	4Z	3L	LA	9B	8B
HD-6434 (Advance)	4K	3F			
HD-6435 (Advance)	4L	3N			
HD-6436 (Advance)	4L	3N			
HD-6440	4N	3D	LA	9D	8C
HD-6495	4Z	3L	LA	9B	8B

* These package numbers to be used in product ordering. Other numbers shown in Selection Guide and drawings are internal numbers.

** Harris is making a transition from the 4J to the 5H package. Check with your local rep before placing an order to determine the current package type.

† Harris is making a transition from flatpacks to cer-packs. Check with your local rep before placing an order to determine the current package type.

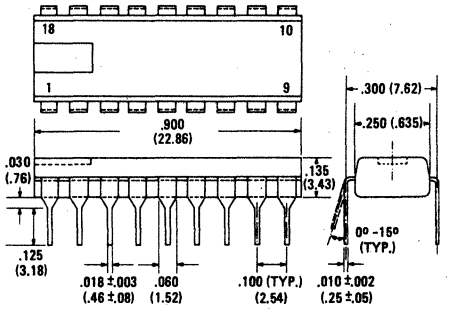
NOTE FOR PACKAGE DRAWINGS ON FOLLOWING PAGES:

1. All dimensions in inches; millimeters are shown in parenthesis.
2. All dimensions ± .010 (± 0.25mm) unless otherwise shown.
3. Internal package codes are shown in black squares.

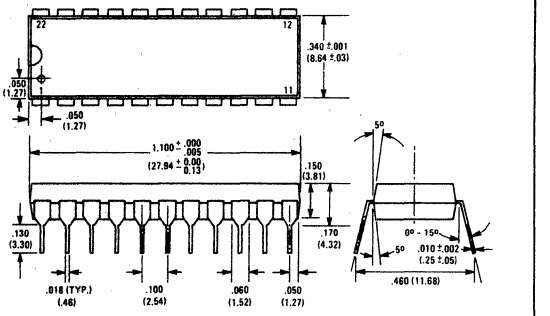
7

Package Dimensions

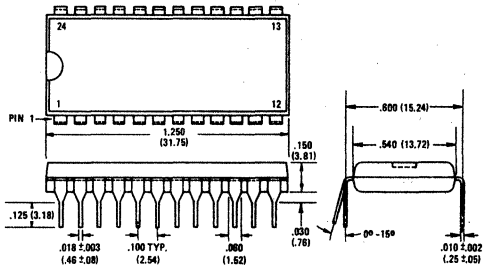
3D — 18 LEAD D.I.P. EPOXY



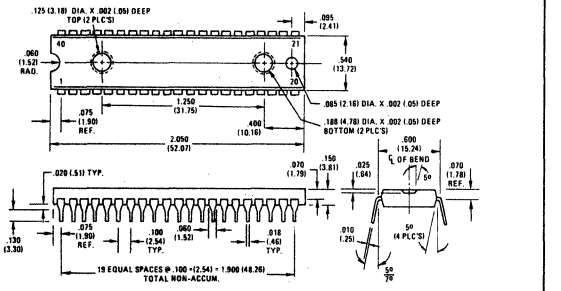
3E — 22 LEAD D.I.P. EPOXY



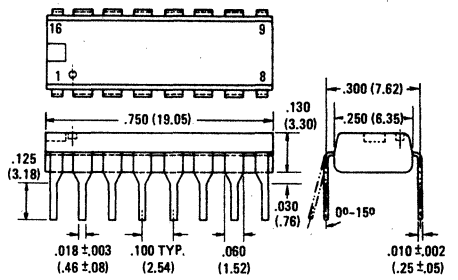
3F — 24 LEAD D.I.P. EPOXY



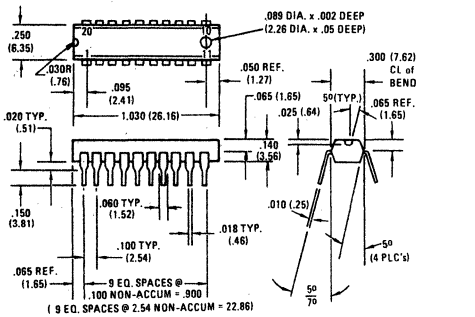
3H 3J — 40 LEAD D.I.P. EPOXY



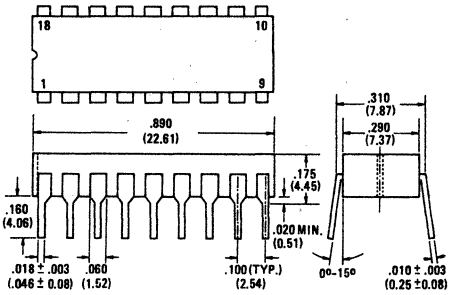
3L — 16 LEAD D.I.P. EPOXY



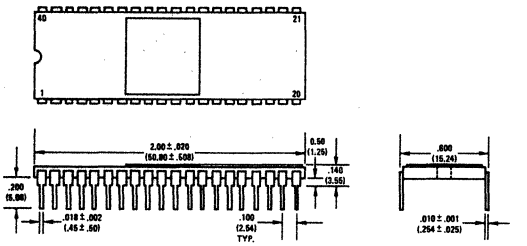
3N — 20 LEAD D.I.P. EPOXY



4G 4N — 18 LEAD CERAMIC D.I.P.

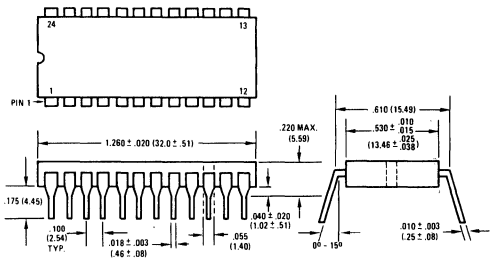


4J — 40 LEAD SIDE BRAZED D.I.P.

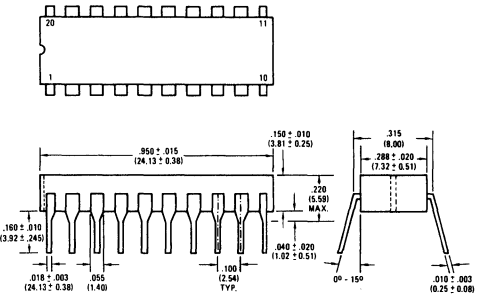


7

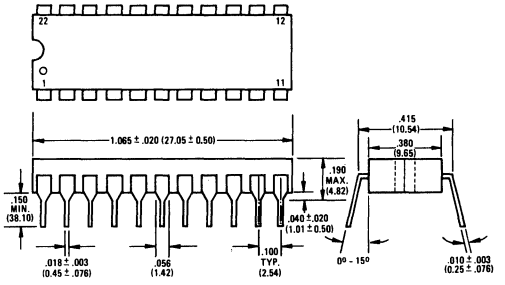
4K 24 LEAD CERAMIC D.I.P.



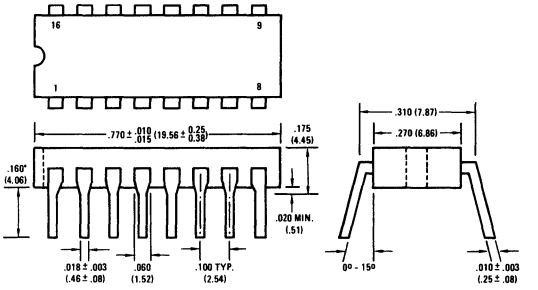
4L 20 LEAD CERAMIC D.I.P.



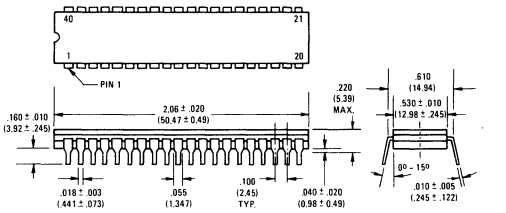
4M 22 LEAD CERAMIC D.I.P.



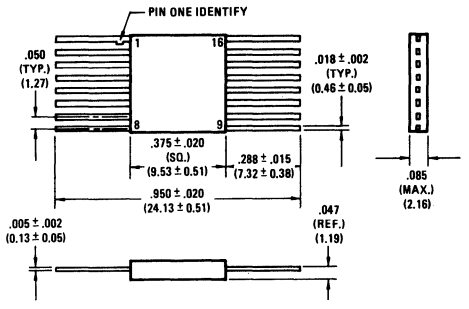
4Z 16 LEAD CERAMIC D.I.P.



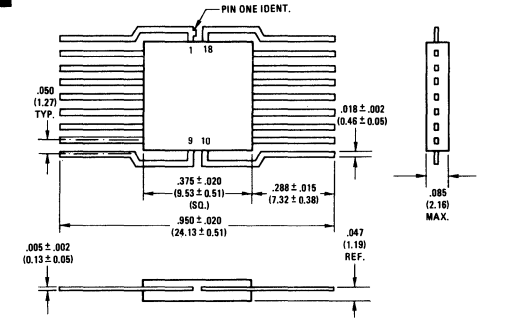
5H 40 LEAD CERAMIC D.I.P.



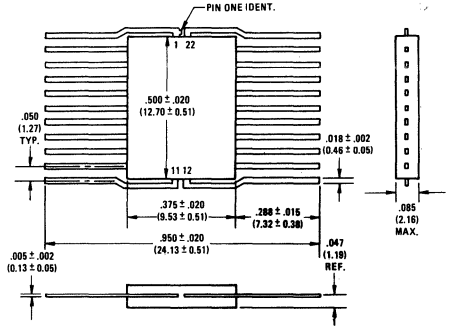
8B 16 LEAD CER-PAK



8C 18 LEAD CER-PAK

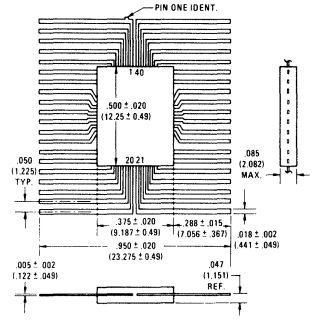


8K 22 LEAD CER-PAK

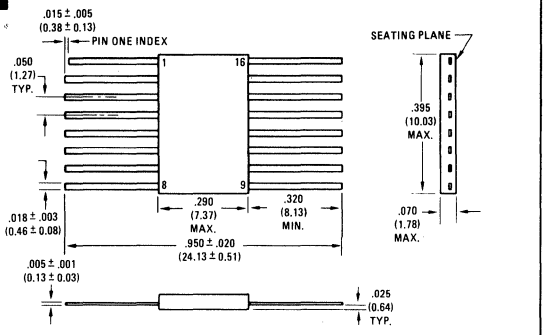


7

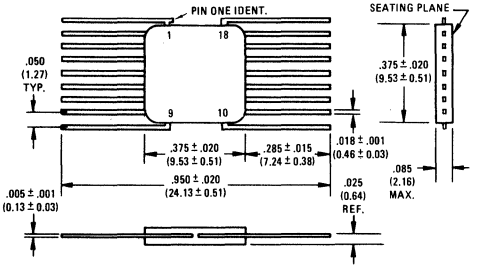
8P 40 LEAD CER-PAK



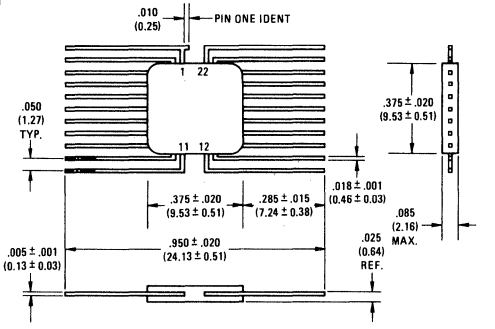
9B 16 LEAD FLATPACK



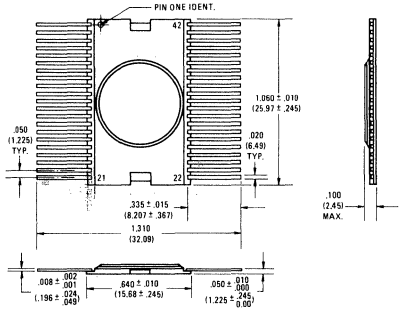
9D 18 LEAD FLATPACK



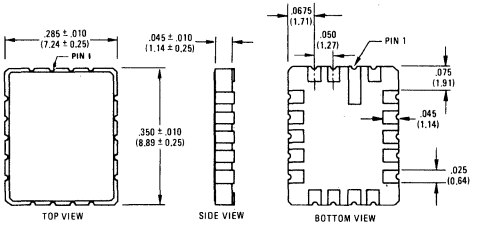
9E 22 LEAD FLATPACK



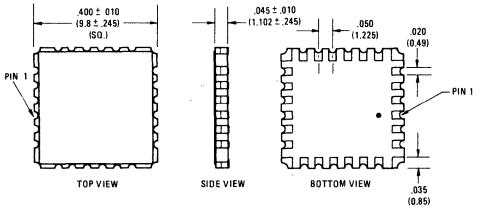
9X 42 LEAD FLATPACK



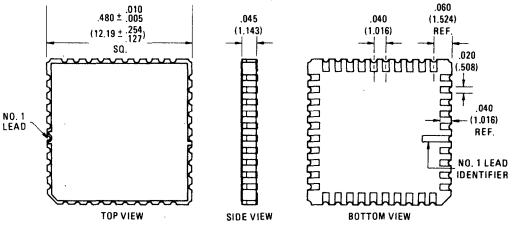
LA 18 PIN LEADLESS CARRIER



LC 28 PIN LEADLESS CARRIER



LG 40 PIN LEADLESS CARRIER



7

Dice Information

μP

Dice Ordering Information	8—2
Dice Geometry Index	8—3
Dice Geometries & Dimensions	8—4

Dice Ordering Information

GENERAL INFORMATION

Harris Microprocessor Products are available in chip form to the hybrid micro circuit designer. The standard chips are DC electrically tested at 25°C to the data sheet limits for the commercial device and are 100% visually inspected to MIL-STD-883, Method 2010, condition B criteria. Packaging for shipment consists of waffle pack carriers plus an anti-static cushioning strip for extra protection.

The hybrid industry has rapidly become more diversified and stringent in its requirements for integrated circuits. To meet these demands Harris has several options additonal to standard chip processing available upon request at extra cost. For more information consult your nearest Harris Sales Office.

CHIP ORDERING INFORMATION

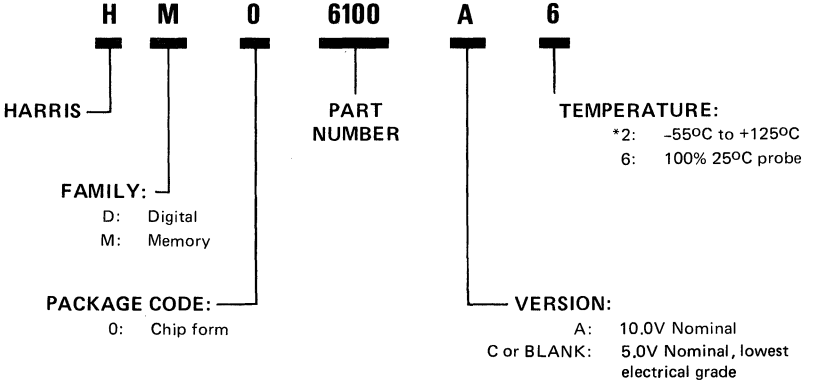
Standard and special chip sales are direct factory order only. The minimum order on all sales is $250.00 per line item. Contact the local Harris Sales Office for pricing and delivery on special chip requirements.

MECHANICAL INFORMATION

Dimensions: All chip dimensions nominal with a tolerance of ± .003".
Maximum chip thickness is .012".

Bonding pads: Minimum bonding pad size is .004" x .004" unless otherwise specified.

PRODUCT CODE EXAMPLE



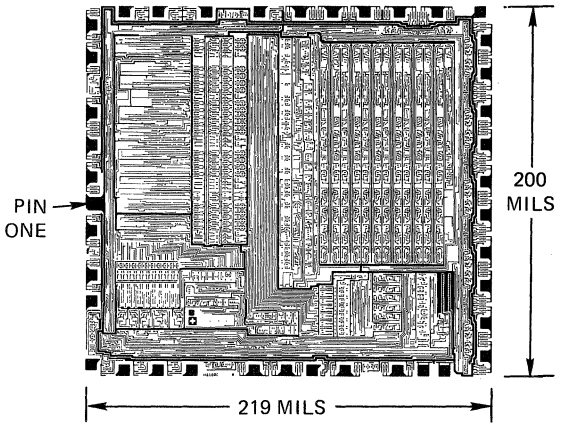
* Contact Harris for Availability

NOTE: All Harris Digital Microprocessor Products have biased substrates. Persons wishing to utilize products in dice form should contact the Harris factory for specific product information regarding proper connection of the substrate.

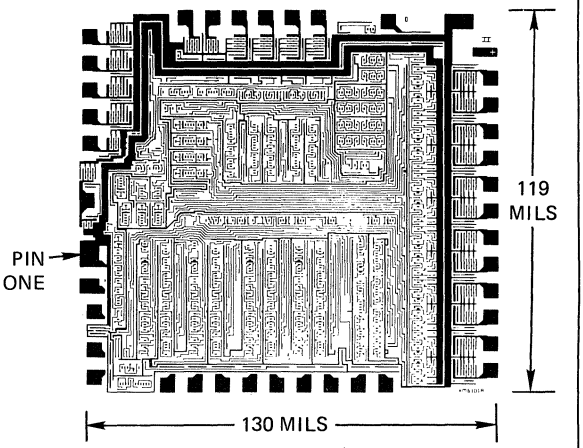
Dice Geometry Index

Product		Drawing No.
MICROPROCESSOR FAMILY		
HM-6100	CMOS 12 Bit Microprocessor (CPU)	1
HD-6101	CMOS Parallel Interface Element (PIE)	2
HD-6102 (Advance)	Memory Extension/DMA/Interval Timer/Controller (MEDIC)	
HD-6103 (Advance)	CMOS Parallel Input/Output Port (PIO)	
MEMORY FAMILY		
HM-6312	CMOS ROM 1024 Word x 12 Bit	3
HM-6512	64 x 12 CMOS RAM	4
HM-6561	256 x 4 CMOS RAM	5
HM-6518	1024 x 1 CMOS RAM	6
HM-6533	1024 x 4 CMOS RAM	7
HM-6543	4096 x 1 CMOS RAM	8
INTERFACE FAMILY		
HD-4702	CMOS Programmable Bit Rate Generator	9
HD-6402	CMOS/LSI Universal Asynchronous Receiver Transmitter (UART)	10
HD-6405	CMOS Programmable Bit Rate Generator	11
HD-6408	CMOS Asynchronous Serial Manchester Adapter (ASMA)	12
HD-6431	CMOS Hex Latched Bus Driver	13
HD-6432	CMOS Hex Bi-directional Bus Driver	14
HD-6433	CMOS Quad Bus Transceiver	13
HD-6434 (Advance)	CMOS Octal Resettable Latched Bus Driver	15
HD-6435 (Advance)	CMOS Hex Resettable Latched Bus Driver	16
HD-6436 (Advance)	CMOS Octal Bus Buffer Driver	17
HD-6440	CMOS Latched 3 to 8 Line Decoder Driver	18
HD-6495	CMOS Hex Bus Driver	13

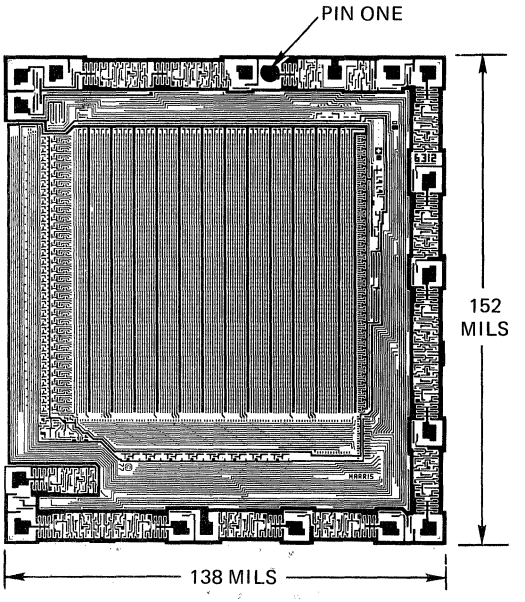
1 HM-6100



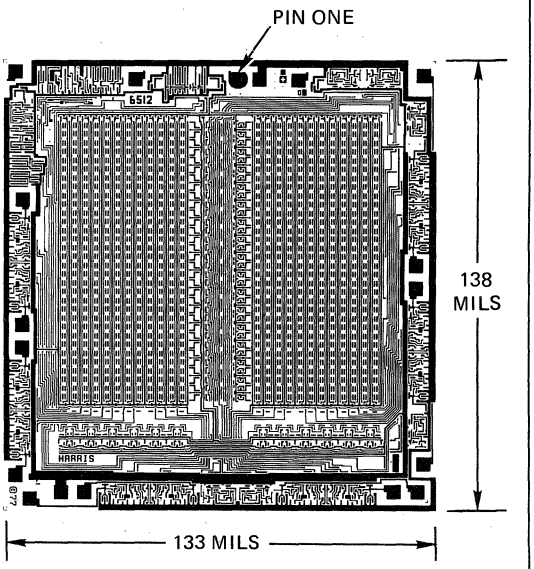
2 HD-6101



3 HM-6312

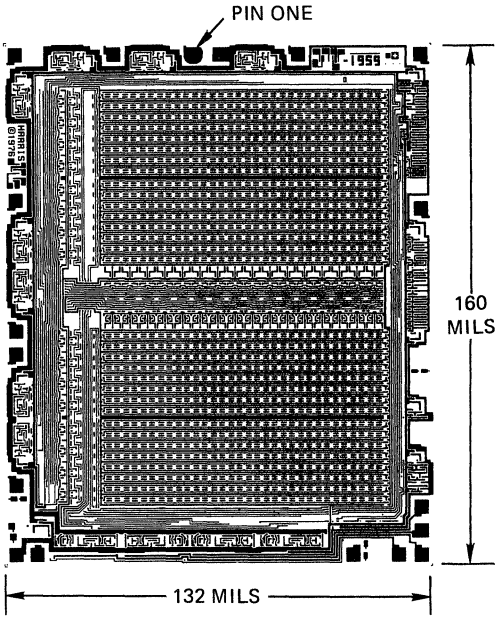


4 HM-6512

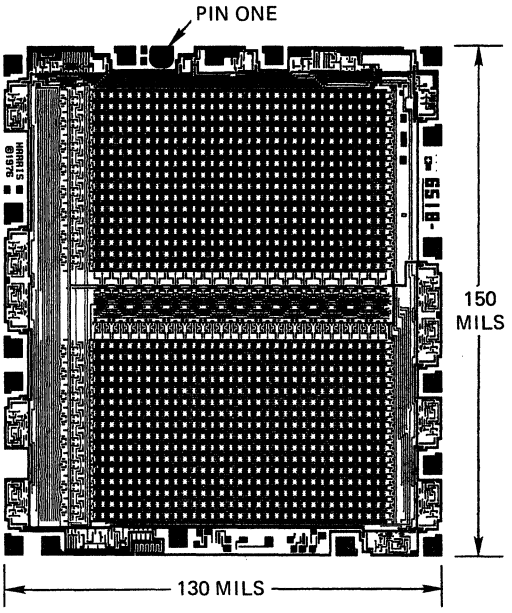


8

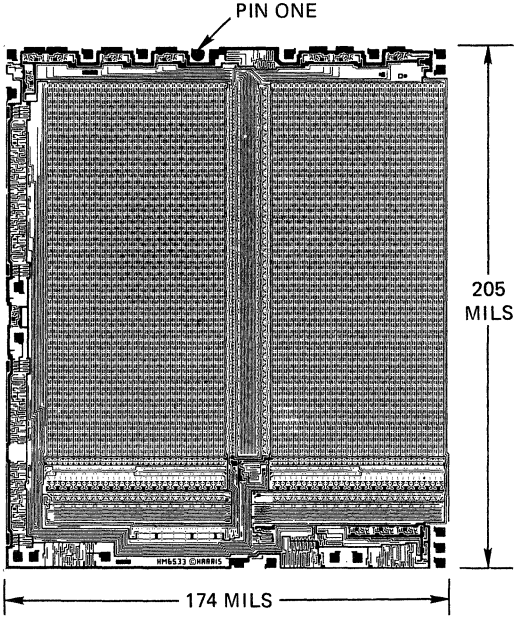
5 HM-6561



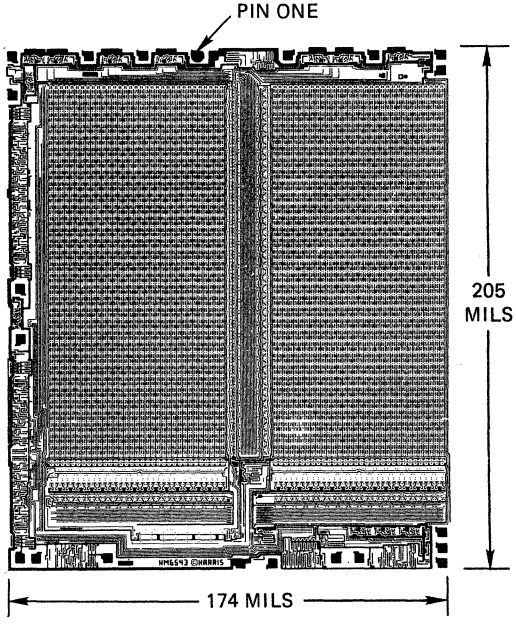
6 HM-6518



7 HM-6533

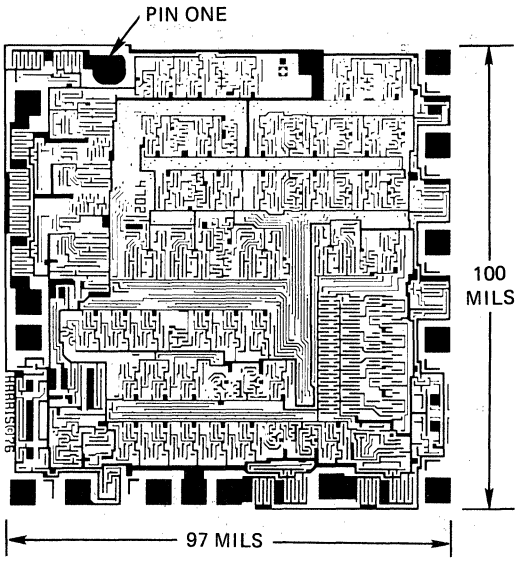


8 HM-6543

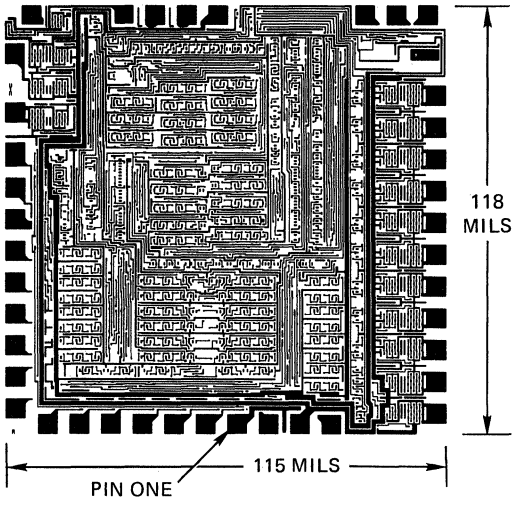


8

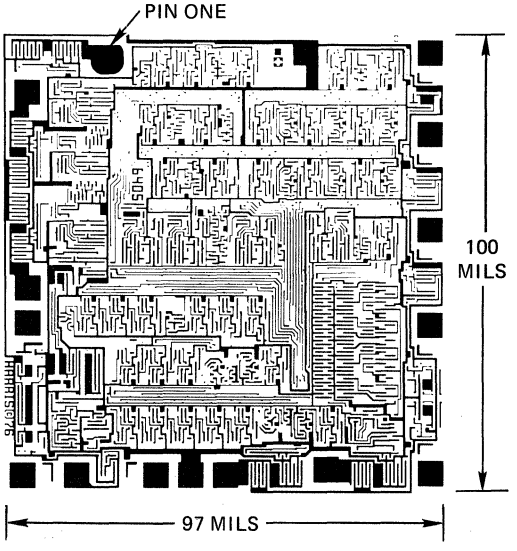
9 HD-4702



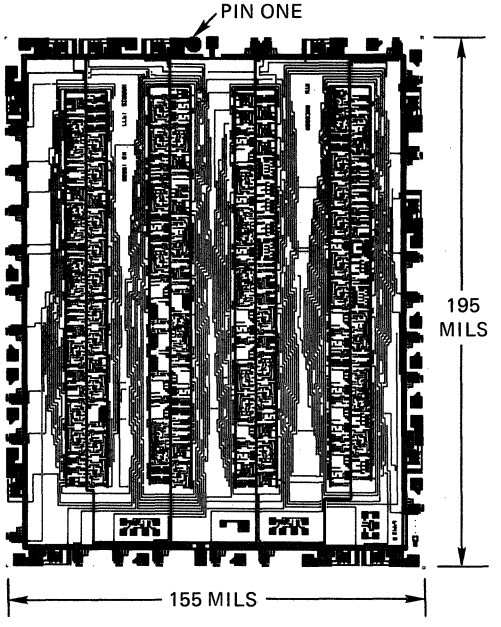
10 HD-6402



11 HD-6405

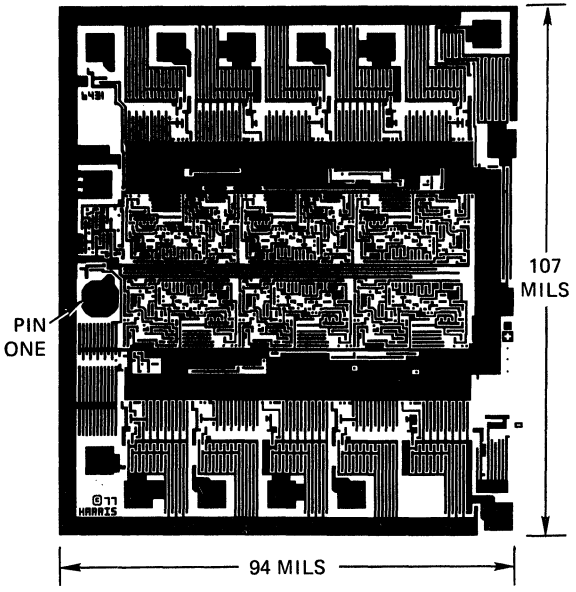


12 HD-6408

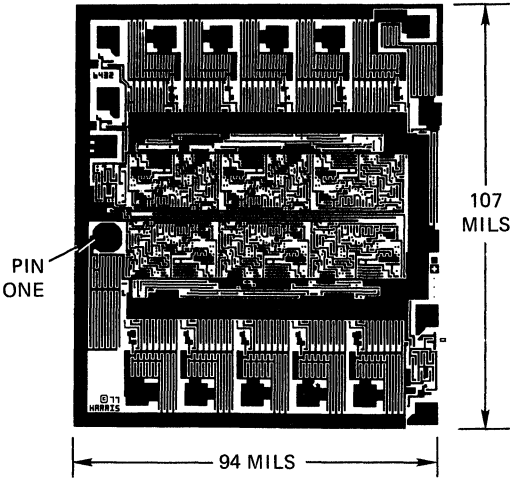


8

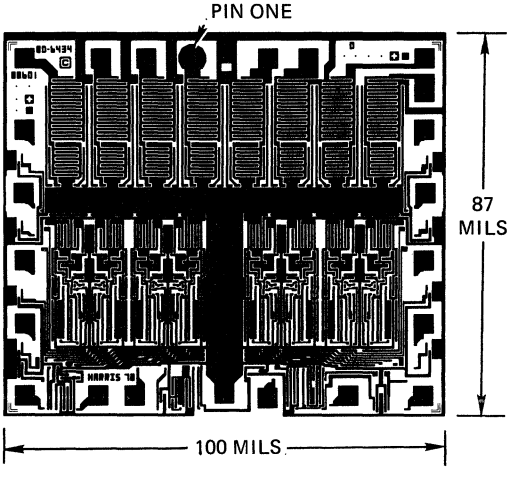
13 HD-6431, HD-6433, HD-6495



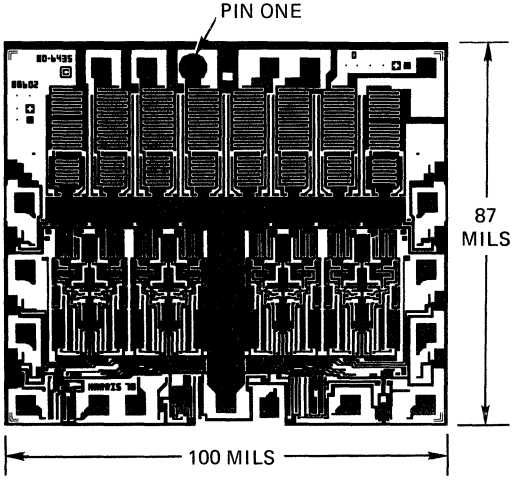
14 HD-6432



15 HD-6434

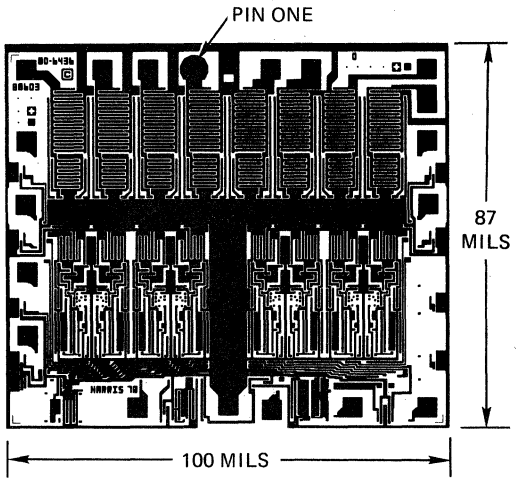


16 HD-6435

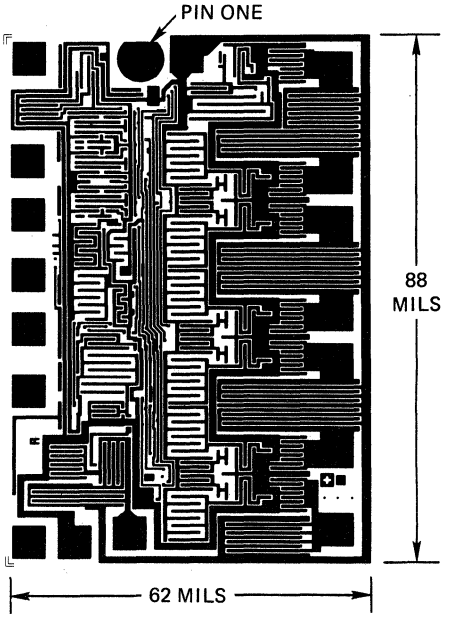


8

17 HD-6436



18 HD-6440



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Harris Sales Locations

OEM Sales

NORTHEASTERN REGION

Suite 301
177 Worcester Street
Wellesley Hills, MA 02181
(617) 237-5430

535 Broadhollow Road
Melville, L.I., NY 11747
(516) 249-4500

SOUTHEASTERN REGION

Suite 115
2020 W. McNab Road
Ft. Lauderdale, FL 33309
(305) 971-3200

Suite 325
650 Swedesford Road
Wayne, PA 19087
(215) 687-6680

CENTRAL REGION

16001 Dallas Parkway
Mail Stop 47
Dallas, TX 75240
(214) 386-2090

Suite 206
5250 Far Hills Avenue
Kettering, OH 45429
(513) 433-5770

Suite 508
2355 S. Arlington Heights Road
Arlington Heights, IL 60005
(312) 437-4712

WESTERN REGION

Suite 227
21243 Ventura Boulevard
Woodland Hills, CA 91364
(213) 992-0686

2016 Quail Street
Newport Beach, CA 92660
(714) 540-2176

Suite 300
625 Ellis Street
Mountain View, CA 94043
(415) 964-6443

International Sales

Europe

OEM SALES OFFICES

ENGLAND

Harris Systems Ltd.
Harris Semiconductor Div.
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