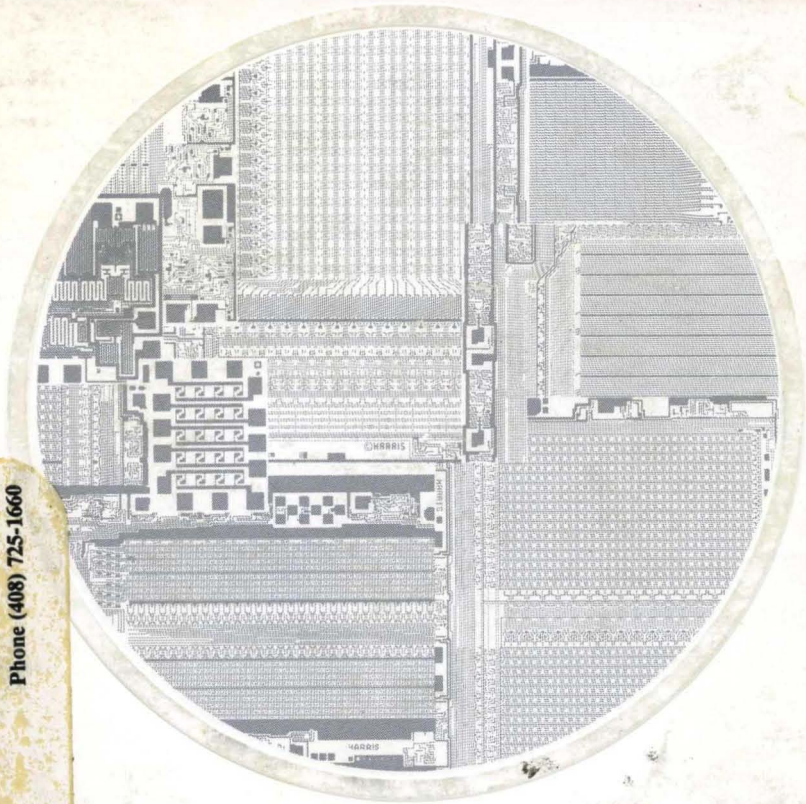
MEMORY

BIPOLAR

CMOS



HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

Volume 1

Volume 1
$2.95

Harris Bipolar & CMOS Memory Data Book

Harris Semiconductor Memory Products represent state-of-the-art in density and high speed performance. Harris' expertise in design and processing offers the user the most reliable product available in a wide choice of formats, options, and package types. With continuing research and development and the introduction of new products, Harris will provide its customers with the most advanced technology.

This book describes Harris Semiconductor Products Division's complete line of memory products and includes a complete set of product specifications and data sheets. Also included are sections on reliability, programming, and packaging.

Please fill out the registration card at the back of this book and return it to us so we may keep you informed of our latest new product developments over the next year.

If you need more information on these and other Harris products, please contact the nearest Harris sales office listed in the back of this data book.

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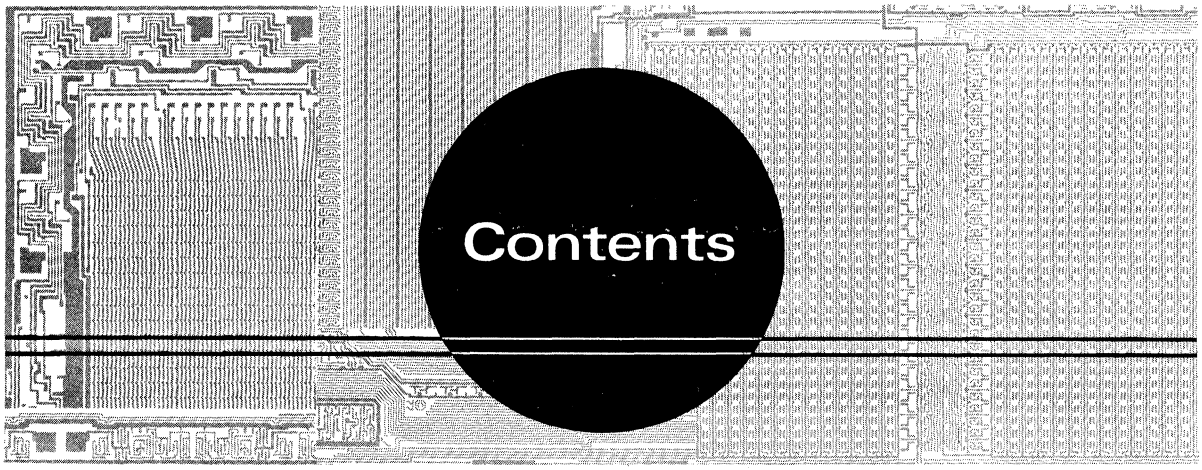

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HA-911	Low Noise Operational Amplifier
HA-2050	High Slew Rate F.E.T. Input Operational Amplifier
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HA-2055	High Slew Rate F.E.T. Input Operational Amplifier
HA-2055A	High Slew Rate F.E.T. Input Operational Amplifier
HA-2060	Wide Band F.E.T. Input Operational Amplifier
HA-2060A	Wide Band F.E.T. Input Operational Amplifier
HA-2065	Wide Band F.E.T. Input Operational Amplifier
HA-2065A	Wide Band F.E.T. Input Operational Amplifier
HA-2400	PRAM, Four Channel Operational Amplifier
HA-2404	PRAM, Four Channel Operational Amplifier
HA-2405	PRAM, Four Channel Operational Amplifier
HA-2420	Sample and Hold
HA-2425	Sample and Hold
HA-2500	Precision High Slew Rate Operational Amplifier
HA-2502	Precision High Slew Rate Operational Amplifier
HA-2510	High Slew Rate Operational Amplifier
HA-2512	High Slew Rate Operational Amplifier
HA-2515	High Slew Rate Operational Amplifier
HA-2520	High Slew Rate, Uncompensated Operational Amplifier
HA-2522	High Slew Rate, Uncompensated Operational Amplifier
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HA-2622	Very Wide Band, Uncompensated Operational Amplifier
HA-2625	Very Wide Band, Uncompensated Operational Amplifier
HA-2630	High Performance Current Booster
HA-2635	High Performance Current Booster
HA-2640	High Voltage Operational Amplifier
HA-2645	High Voltage Operational Amplifier
HA-2650	Dual High Performance Operational Amplifier
HA-2655	Dual High Performance Operational Amplifier
HA-2700	Low Power, High Performance Operational Amplifier
HA-2704	Low Power, High Performance Operational Amplifier
HA-2705	Low Power, High Performance Operational Amplifier
HA-2720	Low Power, Current Programmable Operational Amplifier
HA-2725	Low Power, Current Programmable Operational Amplifier
HA-2730	Dual Low Power, Current Programmable Operational Amplifier
HA-2735	Dual Low Power, Current Programmable Operational Amplifier
HA-2900	Chopper Stabilized Operational Amplifier
HA-2904	Chopper Stabilized Operational Amplifier
HA-2905	Chopper Stabilized Operational Amplifier
HA-4602	Quad High Performance Operational Amplifier
HA-4605	Quad High Performance Operational Amplifier
HA-4622	Wide Band, High Performance Quad Operational Amplifier
HA-4625	Wide Band, High Performance Quad Operational Amplifier
HA-4741	Quad Operational Amplifier
HA-4900	Quad Precision Comparator
HA-4905	Quad Precision Comparator
HC-55516	Delta Modulator (CVSD)
HC-55532	Delta Modulator (CVSD)

HD-1065	Keyboard Encoder
HD-245	Triple Line Transmitter
HD-246	Triple Line Receiver
HD-248	Triple Party Line Receiver
HD-249	Triple Line Receiver
HD-4702	CMOS Bit Rate Generator
HD-6101	CMOS Parallel Interface Element
HD-6102	CMOS Memory Extension/DMA/Interval Timer/Controller
HD-6103	CMOS Parallel Input-Output Port
HD-6402	CMOS Universal Assynchronous Receiver-Transmitter
HD-6405	CMOS Bit Rate Generator
HD-6431	CMOS Three State Latching Bus Driver
HD-6432	CMOS Bi-Directional Bus Driver
HD-6433	CMOS Bus Separator Driver
HD-6440	CMOS 1 of 8 Latched Decoder Driver
HD-6495	CMOS Three State Buffer Driver
HD-6600	Quad PROM Power Strobe
HD-15530	CMOS Manchester Encoder/Decoder (24 Pin)
HD-15531	CMOS Manchester Encoder/Decoder (40 Pin)
HI-200	Dual SPST Switch
HI-201	Quad SPST Switch
HI-506	16/Dual 8 Channel Multiplexer
HI-506A	Overvoltage Protected 16/Dual 8 Channel Multiplexer
HI-507	16/Dual 8 Channel Multiplexer
HI-507A	Overvoltage Protected 16/Dual 8 Channel Multiplexer
HI-508A	Overvoltage Protected 8/Dual 4 Channel Multiplexer
HI-509A	Overvoltage Protected 8/Dual 4 Channel Multiplexer
HI-562	12 Bit High Speed, Precision Digital to Analog Converter
HI-1080	8 Bit Precision Digital to Analog Converter
HI-1085	8 Bit Precision Digital to Analog Converter
HI-1800A	Dual DPDT Low Leakage Switch
HI-1818A	8/Dual 4 Channel Multiplexer
HI-1828A	8/Dual 4 Channel Multiplexer
HI-1840	Fail-Safe 16 Channel Multiplexer
HI-5040	Low Resistance SPST Switch
HI-5041	Low Resistance Dual SPST Switch
HI-5042	Low Resistance SPST Switch
HI-5043	Low Resistance Dual SPDT Switch
HI-5044	Low Resistance DPST Switch
HI-5046	Low Resistance DPDT Switch
HI-5046A	Low Resistance DPDT Switch
HI-5047	Low Resistance 4 PST Switch
HI-5047A	Low Resistance 4 PST Switch
HI-5048	Low Resistance Dual SPST Switch
HI-5049	Low Resistance Dual DPST Switch
HI-5050	Low Resistance SPDT Switch
HI-5051	Low Resistance Dual SPDT Switch
HI-5610	10 Bit High Speed Precision D to A Converter
HI-5612	12 Bit Very High Speed Precision D to A Converter
HM-0104	10 x 4 Diode Matrix
HM-0110	4 x 10 Diode Matrix
HM-0168	6 x 8 Diode Matrix
HM-0186	8 x 6 Diode Matrix
HM-0198	9 x 8 Diode Matrix
HM-0410	4 x 10 Diode Matrix
HM-6100	CMOS 12 Bit Microprocessor
HM-6312	1024 x 12 CMOS ROM
HM-6388	8192 x 8 CMOS ROM
HM-6389	8192 x 8 CMOS ROM
HM-6501	256 x 4 CMOS RAM
HM-6503	2048 x 1 CMOS RAM

HM-6504	4096 x 1 CMOS RAM
HM-6508	1024 x 1 CMOS RAM
HM-6511	64 x 12 CMOS RAM
HM-6512	64 x 12 CMOS RAM
HM-6513	512 x 4 CMOS RAM
HM-6514	1024 x 4 CMOS RAM
HM-6518	1024 x 1 CMOS RAM
HM-6533	1024 x 4 CMOS RAM
HM-6543	4096 x 1 CMOS RAM
HM-6551	256 x 4 CMOS RAM
HM-6561	256 x 4 CMOS RAM
HM-6562	256 x 4 CMOS RAM
HM-6611	256 x 4 CMOS PROM
HM-6661	256 x 4 CMOS PROM
HM-7602	32 x 8 Bipolar PROM – Open Collector
HM-7603	32 x 8 Bipolar PROM – Three State
HM-76LS03	32 x 8 Bipolar PROM – Three State
HM-7608	1024 x 8 Bipolar PROM – Open Collector
HM-7610	256 x 4 Bipolar PROM – Open Collector
HM-7610A	256 x 4 Bipolar PROM – Open Collector
HM-7611	256 x 4 Bipolar PROM – Three State
HM-7611A	256 x 4 Bipolar PROM – Three State
HM-7616	2048 x 8 Bipolar PROM – Three State
HM-76160	2048 x 8 Bipolar PROM – Open Collector
HM-76161	2048 x 8 Bipolar PROM – Three State
HM-7620	512 x 4 Bipolar PROM – Open Collector
HM-7620A	512 x 4 Bipolar PROM – Open Collector
HM-7621	512 x 4 Bipolar PROM – Three State
HM-7621A	512 x 4 Bipolar PROM – Three State
HM-7625R	256 x 8 Bipolar PROM – Three State
HM-7629	256 x 8 Bipolar PROM – Three State
HM-7640	512 x 8 Bipolar PROM – Open Collector
HM-7640A	512 x 8 Bipolar PROM – Open Collector
HM-7640AR	512 x 8 Bipolar PROM – Open Collector
HM-7641	512 x 8 Bipolar PROM – Three State
HM-7641A	512 x 8 Bipolar PROM – Three State
HM-7641AR	512 x 8 Bipolar PROM – Three State
HM-7642	1024 x 4 Bipolar PROM – Open Collector
HM-7642A	1024 x 4 Bipolar PROM – Open Collector
HM-7642P	1024 x 4 Bipolar PROM – Open Collector
HM-7643	1024 x 4 Bipolar PROM – Three State
HM-7643A	1024 x 4 Bipolar PROM – Three State
HM-7643P	1024 x 4 Bipolar PROM – Three State
HM-7644	1024 x 4 Bipolar PROM
HM-7644A	1024 x 4 Bipolar PROM
HM-7645	1024 x 4 Bipolar PROM – Three State
HM-7645P	1024 x 4 Bipolar PROM – Three State
HM-7647R	512 x 8 Bipolar PROM – Three State
HM-7648	512 x 8 Bipolar PROM – Open Collector
HM-7649	512 x 8 Bipolar PROM – Three State
HM-7680	1024 x 8 Bipolar PROM – Open Collector
HM-7680R	1024 x 8 Bipolar PROM – Open Collector
HM-7680P	1024 x 8 Bipolar PROM – Open Collector
HM-7680RP	1024 x 8 Bipolar PROM – Open Collector
HM-7681	1024 x 8 Bipolar PROM – Three State
HM-7681R	1024 x 8 Bipolar PROM – Three State
HM-7681P	1024 x 8 Bipolar PROM – Three State
HM-7681RP	1024 x 8 Bipolar PROM – Three State
HM-7683	1024 x 8 Bipolar PROM
HM-7684	2048 x 4 Bipolar PROM – Open Collector

HM-7684P	2048 x 4 Bipolar PROM – Open Collector
HM-7685	2048 x 4 Bipolar PROM – Three State
HM-7685P	2048 x 4 Bipolar PROM – Three State
HM-7686	2048 x 4 Bipolar PROM – Open Collector
HM-7686R	2048 x 4 Bipolar PROM – Open Collector
HM-7686P	2048 x 4 Bipolar PROM – Open Collector
HM-7686RP	2048 x 4 Bipolar PROM – Open Collector
HM-7687	2048 x 4 Bipolar PROM – Three State
HM-7687R	2048 x 4 Bipolar PROM – Three State
HM-7687P	2048 x 4 Bipolar PROM – Three State
HM-7687RP	2048 x 4 Bipolar PROM – Three State
JAN-0512	JAN Qualified PROM

Devices by Families

BIPOLAR PROMS (Section 2)

JAN 0512
HM-76XX
- HM-7602/03
- HM-7610/11
- HM-7620/21
- HM-7640/41
- HM-7642/43/44

HM-76LS03
HM-7608
HM-7610A/11A
HM-7616
HM-76160/161
HM-7620A/21A
HM-7625R
HM-7629
HM-7640A/41A
HM-7640AR/41AR
HM-7642A/43A
HM-7642P/43P
HM-7644A
HM-7645
HM-7645P
HM-7647R
HM-7648/49
HM-7680/81
HM-7680R/81R
HM-7680P/81P
HM-7680RP/81RP
HM-7683
HM-7684/85
HM-7684P/85P
HM-7686/87
HM-7686/R/87R
HM-7686P/87P
HM-7686RP/87RP

CMOS BUS DRIVERS (Section 4)

HD-6431
HD-6432
HD-6433
HD-6440
HD-6440A
HD-6495

CMOS INTERFACE (Section 4)

HD-4702
HD-6402
HD-6405

CMOS PROMS (Section 3)

HM-6611
HM-6611A
HM-6661
HM-6661A

CMOS RAMS (Section 3)

HM-6501
HM-6503
HM-6504
HM-6508
HM-6511
HM-6512
HM-6513
HM-6514
HM-6518
HM-6533
HM-6543
HM-6551
HM-6561
HM-6562

CMOS ROMS (Section 3)

HM-6312
HM-6388
HM-6389

DIODE MATRICES (Section 4)

HM-0104
HM-0168
HM-0186
HM-0198
HM-0410

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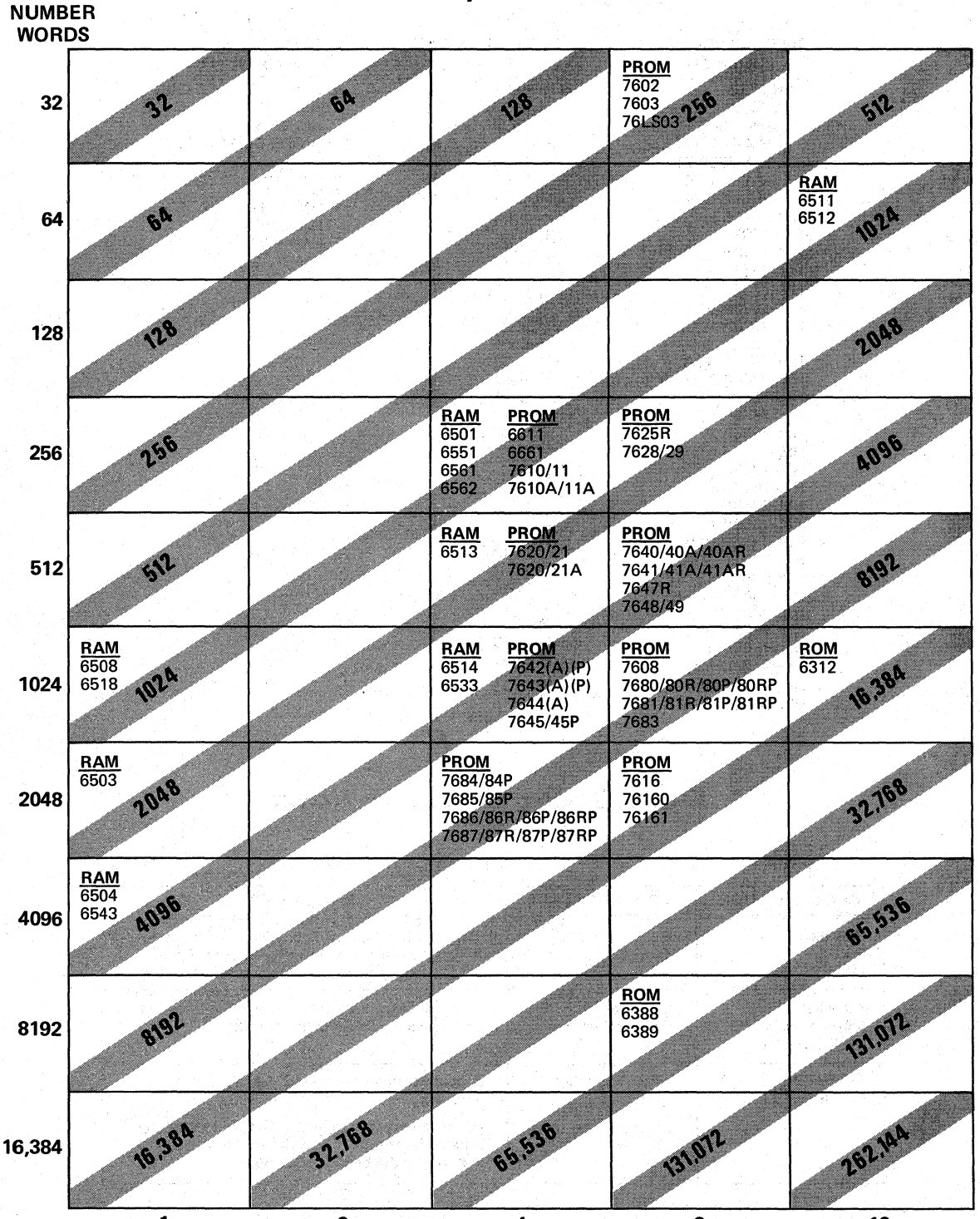
Data Sheet Classifications

CLASSIFICATION	PRODUCT STAGE	DISCLAIMERS
Preview DATA SHEET	Formative or Design	This document contains the design specifications for product under development. Specifications may be changed in any manner without notice.
Advance Information DATA SHEET	Sampling or Pre-Production	This is advanced information, and specifications are subject to change without notice.
Preliminary DATA SHEET	First Production	Supplementary data maybe published at a later date. Harris reserves the right to make changes at any-time without notice, in order to improve design and supply the best product possible.

Harris Memory Selection Guide



Bipolar PROM Cross Reference

AMD	HARRIS
AM 27LS08 AM 27S08 AM 29750 AM 27S18	7602
AM 27LS09 AM 27S09 AM 29751 AM 27S19	7603
AM 27LS100 AM 27S10 AM 29760 AM 27LS20	7610/10A
AM 27LS11 AM 27S11 AM 29761 AM 27LS21	7611/11A
AM 27S12 AM 29770	7620/20A
AM 27S13 AM 29771	7621/21A

INTEL	HARRIS
3601	7610/10A
3621	7611/11A
3602/02A	7620/20A
3622/22A	7621/21A
3604/04A 3604L	7640/41A
3624/24A	7641/41A
3605	7642
3625	7643
3608	7680
3628	7681

MOTOROLA	HARRIS
MCM5303A	JAN 38510/201
MCM7640	7640/40A
MCM7641	7641/41A
MCM7642	7642
MCM7643	7643
MCM2708	7608

RAYTHEON	HARRIS
29660 29662	7610/10A
29661 29663	7611/11A
29611 29613	7620/20A
29620 29622	7648
29624 29625	7640/40A
29621 29623	7649
29625 29627	7641/41A
29630 29632	7680
29631 29633	7681
29634 29635 29636 29637	7608

FAIRCHILD	HARRIS
93417	7610/10A
93427	7611/11A
93436	7620/20A
93446	7620/21A
93438	7640/40A
93448	7641/41A
93452	7642
93453	7643
93450	7680
93451	7681

INTERSIL	HARRIS
5600	7602
5610	7603
5603	7610/10A
5623	7611/11A
5604	7620/20A
5624	7621/21A
5605	7640/40A
5625	7641/41A
56506	7642
56526	7643

NATIONAL	HARRIS
DM8577 DM74S188	7602
DM8578 DM74S288	7603/LS03
DM74S387	7610/10A
DM74S287	7611/11A
DM74S473	7648
DM87S295	7640/40A
DM74S472	7649
DM87S296	7641/41A
DM74S572	7642
DM74S573	7643
DM87S229	7680
DM87S228	7681
DM74S672	7684
DM74S673	7685
DM27LS08	7608

SIGNETICS	HARRIS
82S23	7602
82S123	7603
82S27 82S126	7610/10A
82S129	7611/11A
82S131	7620/20A
82S146	7648
82S140	7640/40A
82S147	7649
82S141	7641/41A
82S136	7642
82S137	7643
82S180	7680
82S181	7681
82S2708	7608
82S184	7684
82S185	7685
82S114	7625R
82S190	76160
82S191	76161

FUJITSU	HARRIS
MB7056	7602
MB7051	7603
MB7057	7610/10A
MB7052	7611/11A
MB7058	7620/20A
MB7053	7620/21A
MB7059	7642
MB7054	7643
MB7060	7680
MB7055	7681

MMI	HARRIS
6330	7602
6331	7603
6300	7610/10A
6301	7611/11A
6305	7620/20A
6306	7621/21A
6348	7648
6340	7640/40A
6349	7649
6341	7641/41A
6352	7642
6353	7643
6380	7680
6381	7681
6385	7608
63100	7684
63101	7685
6336	7629

NEC	HARRIS
μPB403	7610/10A
μPB405	7640/40A
μPB425	7641/41A
μPB406	7642
μPB426	7643
μPB408	7680
μPB428	7681
μPB427	7608

TEXAS INST.	HARRIS
74S188/188A	7602
74S288	7603
74186	JAN 38510/201
74S387	7610/10A
74S287	7611/11A
74S473	7648
74S475	7640/40A
74S472	7649
74S474	7641/41A
74S477	7642
74S476	7643

CMOS Memory Cross Reference

AMD	HARRIS	
9111	6561	B2
9101	6501	A1
9102	6508	C1
9112	6562	A1
9130	6533	A3
9140	6543	A3

AMI	HARRIS	
2114	6514	A1
2147		
4025		
5101	6501	A1
6508	6508	A3

EA	HARRIS	
2101	6501	A1
2111	6561	A1
2112	6562	A1

FAIRCHILD	HARRIS	
2101	6508	C1

GI	HARRIS	
RA3-4256		
4801		
4804		
2114	6514	A1

EMM	HARRIS	
2114	6514	A1

HITACHI	HARRIS	
35101	6501	A1

INTERSIL	HARRIS	
6504	6504	A3
6508	6508	A3
6512	6512	A3
6518	6518	A3
6551	6551	A3
6561	6561	A3
7101		
7111		
7112		
7114		
7141		
7552		

INTEL	HARRIS	
2101	6501	A1
2102	6508	C1
2111	6561	A1
2112	6562	A1
2113	6513	A1
2114	6514	A1
2147		
5101	6501	A1

MOSTEK	HARRIS	
4102	6508	C1
4103		
4104	6504	A2
4404	6514	C2
4451	6514	C2

MOTOROLA	HARRIS	
2114	6514	A1
7001		

NATIONAL	HARRIS	
2101	6501	A1
2102	6508	C1
2111	6561	A1
2114	6561	A1
5257	6504	A1
5269		
74C920	6551	A3
74C921	6561	A3
74C929	6508	A3
74C930	6518	A3

NEC	HARRIS	
2101	6501	A1
2102	6508	C1
2111	6561	A1
2112	6562	A1
4PD415		
5101	6501	A1
6508	6508	A3

RCA	HARRIS	
4101	6501	A1
4111	6561	B1
4112	6562	A1
5001	6508	A1
5040	6501	A1
5501	6508	A1
5540	6501	A1
5114	6514	A1

SIGNETICS	HARRIS	
2101	6501	A1
2102	6508	C1
2111	6561	A1
2601		
2606	6562	C2
2613	6504	A2
2614	6514	A2

SYNERTEK	HARRIS	
2101	6501	A1
2102	6508	C1
2111	6561	A1
2112	6562	A1
2114	6514	A1
5101	6501	A1
5102	6508	C1
5111		
5112		

TI	HARRIS	
2101	6501	A1
2102	6508	C1
2112	6562	A1
2114	6514	A1
4033	6508	C1
4039	6501	A1
4042	6561	A1
4043	6562	A1
4044	6504	A1
4045	6514	A1
5101	6501	A1
6508	6508	A3

TOSHIBA	HARRIS	
5504	6504	A3
5501	6501	A3
5508	6508	A3
5047	6514	C3
54104	6504	C3

ZILOG	HARRIS	
4104	6504	A2
6104	6504	A2

A — Pin for Pin Replacement
B — Minor Pinout Differences
C — Not Pin Compatible

1 — Synchronous-Asynchronous Differences
2 — NMOS Rather Than CMOS but Similar
3 — Similar Electrical Characteristics

User's Guide to Static RAM's

SIZE & ORGANIZATION	TYPE	PINS	HARRIS	AMD	AMI	EA	FAIRCHILD	GI/EMM	HITACHI	INTERSIL	INTEL	MOSTEK	MOTOROLA	NATIONAL	NEC	RCA	SIGNETICS	SYNERTEK	TI	TOSHIBA	ZILOG
768 BIT 64 x 12	CMOS	18	6512						6512												
		18	6511																		
1K BIT 1024 x 1	CMOS	16	6508		6508 4025				6508			7001	74C929	6508	5001 5501		5102	6508	5508		
		18	6518						6518				74C930								
	NMOS	16		9102			2102		7552	2102	4102		2102	4PD415 2102		2102	2102	2102 4033			
256 x 4	CMOS	16	6562														5112				
		18	6561						6561				74C921				5111				
		22	6551						6551				74C920								
		22	6501		5101			35101		5101				5101	5040 5540		5101	5101	5501		
	NMOS	16		9112		2112			7112	2112				2112	4112	2606	2112	2112 4043			
		18		9111		2111			7111	2111			2111	2111	4111	2111	2111	4042			
		22		9101		2101		RA3-4256	7101	2101			2101 5269	2101	4101	2101 2601	2101	2101 4039			
2K BIT 2K x 1	CMOS	18	6503																		
	NMOS	18									4103										
2K BIT 512 x 4	CMOS	18	6513																		
	NMOS	18								2113											
4K BIT 4K x 1	CMOS	18	6504						6504											54104	
		22	6540																	5504	
		22	6543																		
	NMOS	18		9145 2147	2147			4801 4804		7141	2147	4104 4451		5257			2613		4044		4104
		22		9140																	
4K BIT 1K x 4	CMOS	18	6514						6514							5114				5047	
		22	6530																		
		22	6533																		
	NMOS	18		9135	2114			2114		7114	2114	4404	2114	2114			2614	2114	4045 2114		
		22		9130																	

Bipolar Memory

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Product Index

Harris Generic Programmable Read Only Memories

In 1970, Harris offered the industry's first Bipolar programmable read only memory, and has been a leader in the field of Bipolar PROMs from 1970 to date. Harris PROMs are manufactured using the Bipolar Junction Isolation process with reliability proven nickel chromium fusible links. Harris has had experience with nichrome since 1964 when it was first used for high reliability military circuits because of its high stability characteristics. Harris has been manufacturing nichrome fuse links since 1970 when the first PROM was manufactured, and has become the industry's most extensive programmable read only memory concept. This history has been a factor in giving Harris PROMs the industry's highest programming yield and a proven level of quality and reliability.

We now employ a shallow diffused self-aligned emitter aperture process conbined with two-level aluminum interconnect. This state of the art process technology has been deployed to produce large format devices with the high speed and versatility required by the industry.

Today Harris offers a family of programmable read only memories which we call the Generic PROMs or GPROMs. They have the following characteristics:

- Coherent part numbering scheme, the 76xxx series.
- Identical programming procedure for all GPROMs.
- All parameters are guaranteed over full temperature and voltage.
- The GPROM family comprises a complete range of formats.

JAN QUALIFIED PROMS

The Harris Semiconductor Bipolar manufacturing line has received certification for processing JAN product. The Harris JAN 0512 is a QPL I JAN qualified PROM. Four additional Harris PROMs have been granted QPL II listing pending QPL I approval and may be shipped as JAN qualified product. Additional Harris PROMs are at various stages of qualification and the status of each at press time is listed below. As the status of these products will change rapidly, we suggest that you contact the nearest Harris Representative or Harris Sales Office for current status.

HARRIS PART #	SLASH SHEET	STATUS
JAN 0512	MIL-M-38510/20101 BJB	QPL I
HM1-7610	MIL-M-38510/20301 BEB	QPL II
HM1-7611	MIL-M-38510/20302 BEB	QPL II
HM1-7620	MIL-M-38510/20401 BEB	QPL II
HM1-7621	MIL-M-38510/20402 BEB	QPL II
HM1-7642	MIL-M-38510/20601 BVB	Pending QPL II
HM1-7643	MIL-M-38510/20602 BVB	Pending QPL II
HM1-7644	MIL-M-38510/20603 BEB	Pending QPL II
HM1-7602	MIL-M-38510/207	Pending Slash Sheets
HM1-7603	MIL-M-38510/207	Pending Slash Sheets
HM1-7640	MIL-M-38510/208	Pending Slash Sheets
HM1-7641	MIL-M-38510/208	Pending Slash Sheets

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

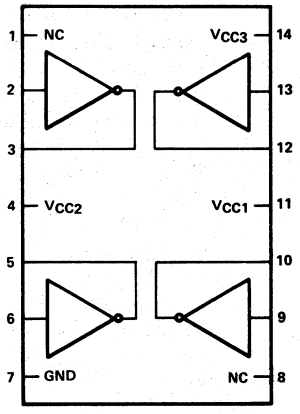
HD-6600
QUAD POWER STROBE

FEBRUARY 1978

Features

- HIGH DRIVE CURRENT–200mA
- HIGH SPEED 50ns TYPICAL
- TTL COMPATIBLE INPUTS
- DIELECTRIC ISOLATION
- QUAD MONOLITHIC CONSTRUCTION
- POWER SUPPLY FLEXIBILITY
- LOW POWER:
  STANDBY–30mW/CIRCUIT
  ACTIVE–95mW/CIRCUIT

Logic Diagram

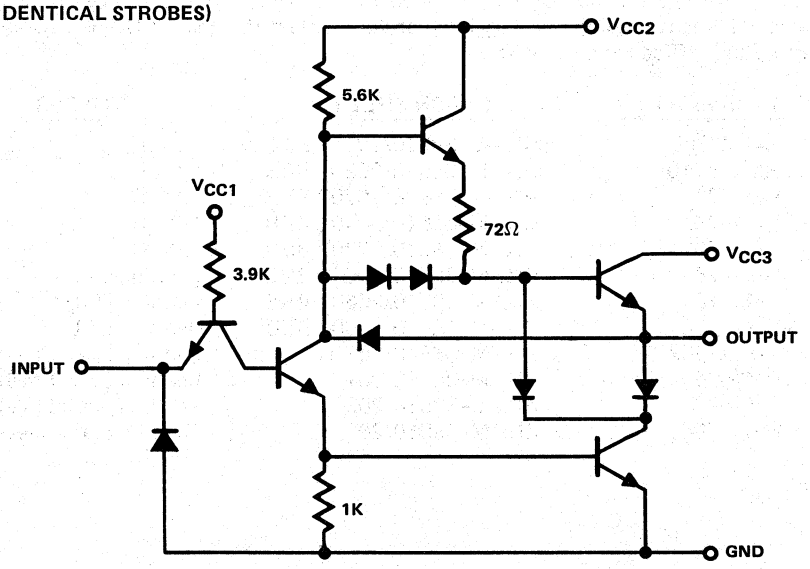


Description

The HD-6600 Quad Power Strobe is constructed with Harris Dielectric Isolation Bipolar Monolithic Process. The design incorporates power supply flexibility with TTL compatible inputs and high current outputs. This circuit is intended for use in power switched PROM arrays.

Circuit Diagram

(ONE OF FOUR IDENTICAL STROBES)



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	V_{CC1}	+8 VDC
	V_{CC2}	+18 VDC
	V_{CC3}	+18 VDC
Input Voltage V_{IN}		-0.5 VDC to +5.5 VDC
Storage Temperature T_{STG}		-65°C to +150°C
Output Current I_L		-200mA
Power Dissipation at 25°C		1000mW
		(Derate 9mW/°C Above 60°C)

RECOMMENDED OPERATING CONDITIONS

Power Supplies:	V_{CC1}	5 VDC ± 10%
	V_{CC2}	12 VDC ± 15%
	V_{CC3}	5 VDC ± 20%

ELECTRICAL CHARACTERISTICS

T_A = -55°C to +125°C HD1-6600-2 V_{CC2} = 12.0 VDC
T_A = 0°C to +75°C HD1-6600-5 V_{CC3} = 5.0 VDC

D.C.

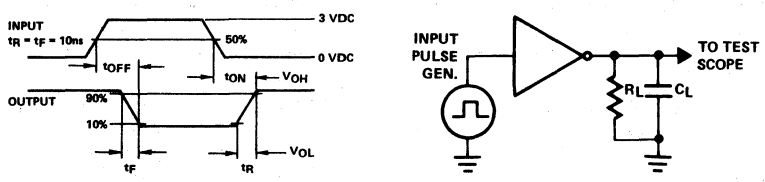
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
I_{IR} I_{IF}	Input Current			60 -1.6	µA mA	V_{IN} = 2.4 VDC V_{IN} = 0.4 VDC V_{CC1} = 5.5 VDC
V_{IH} V_{IL}	Input Threshold Voltage	2.0		0.8	V V	V_{CC1} = 4.5 VDC
V_{OH}	Output Voltage (Note 1)	4.75	4.85		V	V_{CC1} = 5.0 VDC V_{IN} = 0.4 VDC I_L = -150mA DC
V_{OL}				1.0	V	V_{CC1} = 5.0 VDC I_L = 500µA DC
I_{CC1}	Supply Current (Note 2)		4	6.0	mA	V_{CC1} = 5.5 VDC V_{IN} = 2.4 VDC
I_{CC2}			40	70	mA	V_{CC1} = 5.5 VDC V_{IN} = 0.4 VDC I_L = -150mA DC
I_{CC2}			8	15	mA	V_{CC1} = 5.5 VDC V_{IN} = 2.4 VDC I_L = 0

A.C.

SYMBOL	PARAMETER	TYP.	MAX.	UNITS	CONDITIONS T_A = 25°C
tON	Turn On Delay	50	75	ns	V_{CC1} = 5.0 VDC
tOFF	Turn Off Delay	50	75	ns	V_{CC2} = 12 VDC
					V_{CC3} = 5.0 VDC
tR	Rise Time	40	65	ns	R_L = 33Ω
tF	Fall Time	40	65	ns	C_L = 620 pF

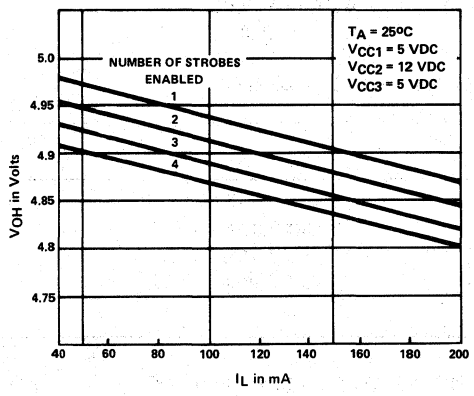
NOTES (1) One strobe enabled. (2) All strobes enabled.

Switching Time Definitions

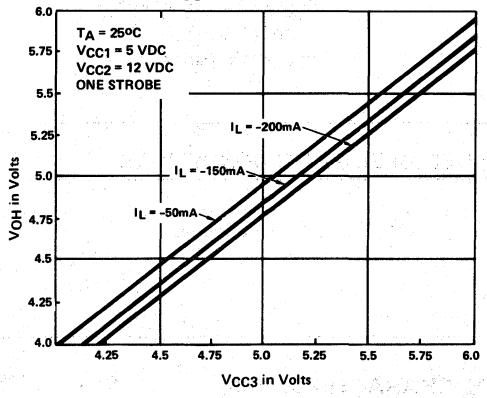


Typical Characteristics

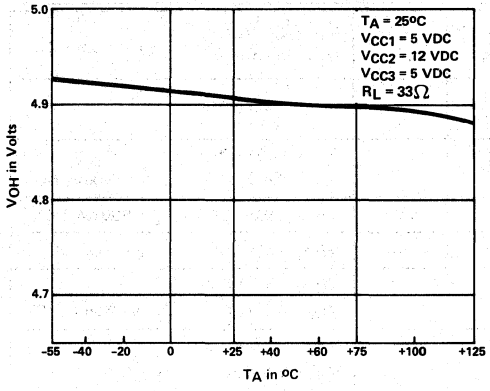
TYPICAL OUTPUT VOLTAGE vs.
LOAD CURRENT AND NUMBER OF STROBES ENABLED



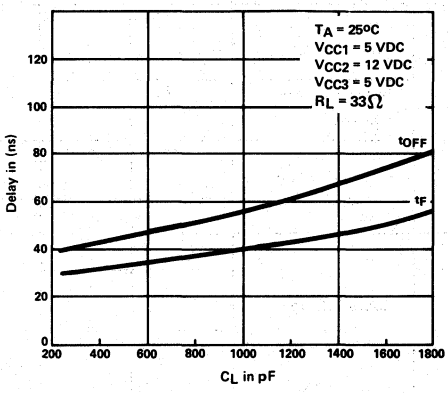
TYPICAL OUTPUT VOLTAGE vs.
V_{CC3} SUPPLY VOLTAGE



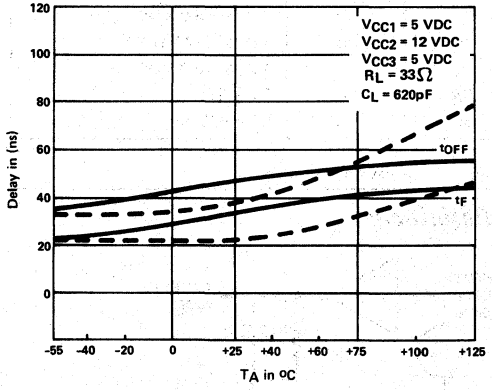
TYPICAL OUTPUT VOLTAGE vs.
AMBIENT TEMPERATURE



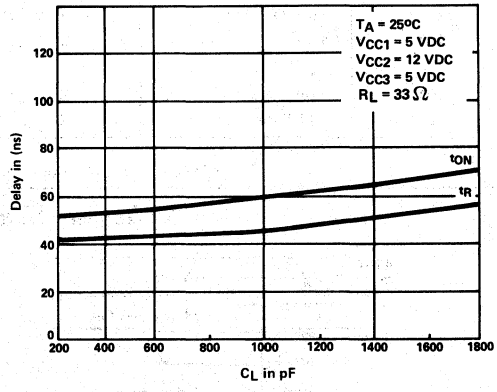
TYPICAL DELAY t_{OFF} AND t_F vs.
LOAD CAPACITANCE



TYPICAL DELAY vs.
AMBIENT TEMPERATURE



TYPICAL DELAY t_{ON} AND t_R vs.
LOAD CAPACITANCE



HM-76XX

GENERIC PROM FAMILY

JANUARY 1978

Features

- COMMON D.C. ELECTRICAL CHARACTERISTICS AND PROGRAMMING PROCEDURE
- SIMPLE, HIGH SPEED PROGRAMMING PROCEDURE, ONE PULSE/BIT
- EXPANDABLE - "OPEN COLLECTOR" OR "THREE STATE" OUTPUTS AND CHIP ENABLE INPUTS
- INPUTS AND OUTPUTS TTL COMPATIBLE
  - LOW INPUT CURRENT – 250μA LOGIC "0", 40μA LOGIC "1"
  - FULL OUTPUT DRIVE – 16 mA SINK, 2mA SOURCE
- FAST ACCESS TIME – GUARANTEED FOR WORST CASE N^2 SEQUENCING, OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES
- PIN COMPATIBLE WITH INDUSTRY STANDARD PROMs AND ROMs

Organizations

PART NUMBER	*OUTPUT	TOTAL BITS	WORDS x BITS/WORD
HM-7602 HM-7603	OC TS	256	32 x 8
HM-7610 HM-7611	OC TS	1024	256 x 4
HM-7620 HM-7621	OC TS	2048	512 x 4
HM-7640 HM-7641	OC TS	4096	512 x 8
HM-7642 HM-7643 HM-7644	OC TS APU	4096	1024 x 4

*OC – Open Collector
*TS – "Three State"
*APU – Active Pull-Up

Description

The HM-76XX Generic PROMs comprise a completely compatible family having common D.C. electrical characteristics and identical programming requirements. They are fully decoded, high speed, field programmable ROMs and are available in all commonly used organizations, with both open-collector and "Three State" outputs. All bits are manufactured storing a logical "1" (outputs high), and can be selectively programmed for a logical "0" (outputs low).

The nichrome fuse technology is the same as is used in the JAN approved MIL-STD-38510/201 PROM and in all other Harris PROMs.

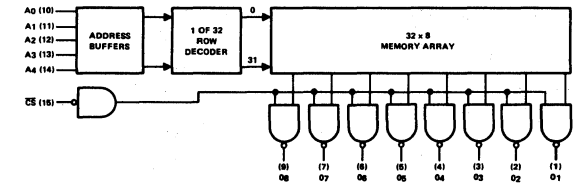
The field programmable PROM can be custom programmed to any pattern using a simple programming procedure. Schottky Bipolar circuitry provides fast access time, and features temperature and voltage compensation to minimize access time variation.

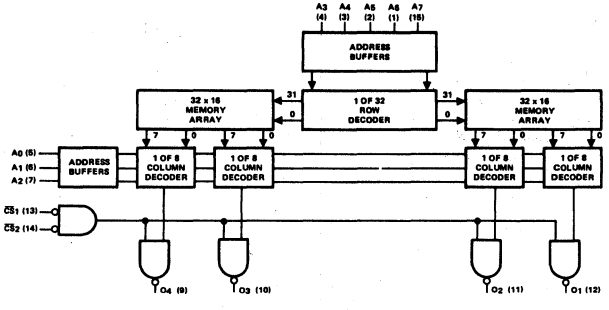
All pinouts are compatible to industry standard PROMs and ROMs.

In addition to the conventional storage array, extra test rows and columns are included to assure high programmability, and guarantee parametric and A.C. performance. Fuses in these test rows and columns are blown prior to shipment.

2

Block Diagrams

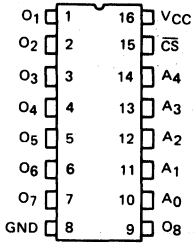




Pinouts

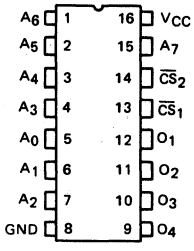
HM-7602/03
32 x 8

TOP VIEW

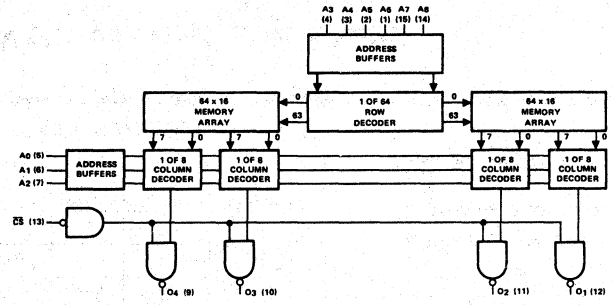


HM-7610/11
256 x 4

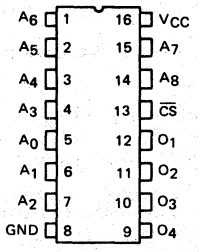
TOP VIEW



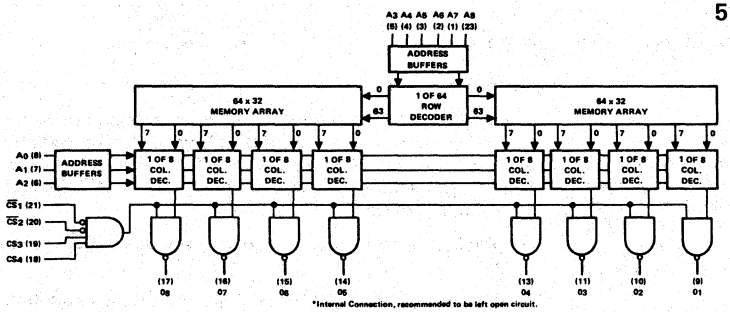
HM-7620/21
512 x 4



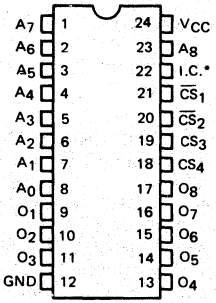
TOP VIEW



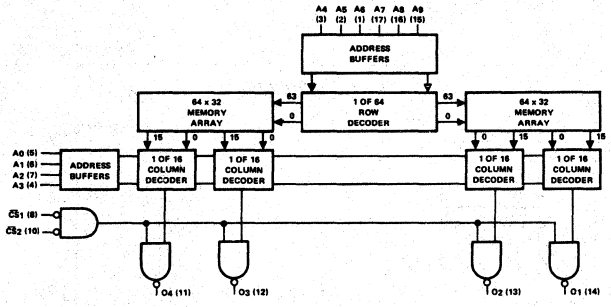
HM-7640/41
512 x 8



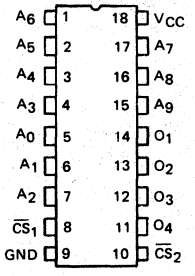
TOP VIEW



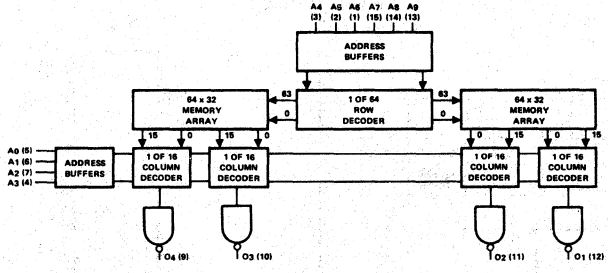
HM-7642/43
1024 x 4



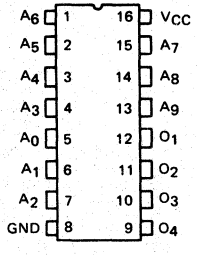
TOP VIEW



HM-7644
1024 x 4



TOP VIEW



ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-76XX-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-76XX-2, HM-76XX-8 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical Measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	OPEN COLLECTOR OUTPUT MIN	OPEN COLLECTOR OUTPUT TYP	OPEN COLLECTOR OUTPUT MAX	THREE STATE OUTPUT MIN	THREE STATE OUTPUT TYP	THREE STATE OUTPUT MAX	UNITS	TEST CONDITIONS
I_{IH}	Address/Enable "1"	–		40	–		40	µA	V_{IH} = V_{CC} Max.
I_{IL}	Input Current (1) "0"	–	-50.0	-250	–	-50.0	-250	µA	V_{IL} = 0.45V
V_{IH}	Input Threshold "1"	2.0	–		2.0	–		V	V_{CC} = V_{CC} Min.
V_{IL}	Voltage "0"		–	0.8		–	0.8	V	V_{CC} = V_{CC} Max.
V_{OH}	Output Voltage "1"	N/A			2.4	3.4		V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min.
V_{OL}	"0"		0.35	0.45		0.35	0.45	V	I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE}	Output Disabled "1"	–	–	100	–	–	100	µA	V_{OH}, V_{CC} = V_{CC} Max.
I_{OLE}	Current (2) "0"	–	–	N/A	–	–	-100	µA	V_{OL} = +0.3V, V_{CC} = V_{CC} Max.
I_{OH}	Output Leakage (1) "1"	–	–	100	–	–	N/A	µA	V_{OH}, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	N/A	–	N/A	-15	–	-100	mA	V_{OUT} = 0.0V One Output Only for a Max. of 1 sec.
I_{CC}	Power Supply Current HM-7602/7603	–	90	105	–	90	105	mA	V_{CC} = V_{CC} Max. All Inputs Grounded
	HM-7610/7611 HM-7620/7621	–	90	130	–	90	130	mA	
	HM-7640/7641	–	125	170	–	125	170	mA	
	HM-7642/7643/7644	–	100	140	–	100	140	mA	

NOTE: (1) Enable current measured using only one enable input to disable the device.
(2) N/A for HM-7644, Active Pull-Up Output.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

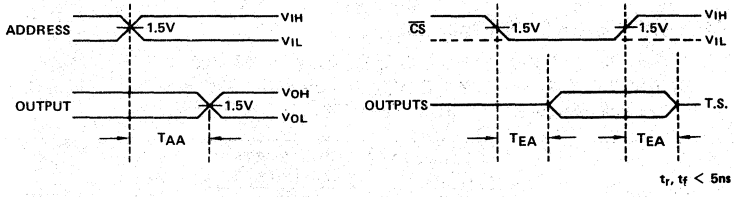
SYMBOL	PARAMETER	HM-76XX-5 V_{CC} – 5V ±5% T_A – 0° to +75°C TYPICAL	HM-76XX-5 V_{CC} – 5V ±5% T_A – 0° to +75°C MAXIMUM	HM-76XX-2 HM-76XX-8 V_{CC} – 5V ±10% T_A – -55°C to +125°C TYPICAL	HM-76XX-2 HM-76XX-8 V_{CC} – 5V ±10% T_A – -55°C to +125°C MAXIMUM	UNITS
T_{AA}	HM-7602/7603	30	40	30	50	ns
T_{EA}		20	30	20	40	ns
T_{AA}	HM-7610/7611	40	60	40	75	ns
T_{EA}		15	25	15	30	ns
T_{AA}	HM-7620/7621	45	70	45	85	ns
T_{EA}		15	25	15	30	ns
T_{AA}	HM-7640/7641	45	70	45	85	ns
T_{EA}		30	40	30	50	ns
T_{AA}	HM-7642/7643	45	60	45	85	ns
T_{EA}	HM-7644	15	25	15	30	ns

T_{AA} – Address to Output Access Time
T_{EA} – Chip Enable Access Time (N/A HM-7644)
A.C. Limits Guaranteed for Worst Case N^2 Sequencing

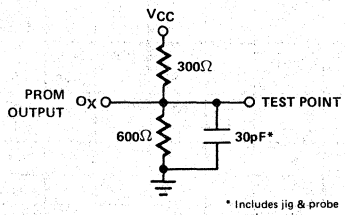
CAPACITANCE: $T_A = 25^oC$

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
CINA, CINCS	Input Capacitance	12	pF	VCC = 5V, VIN = 2.0V, f = 1MHz
COUT	Output Capacitance	12	pF	VCC = 5V, VOUT = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS



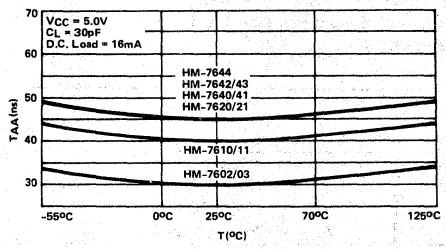
A.C. TEST LOAD



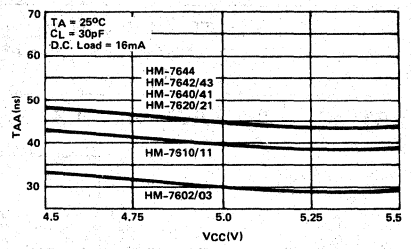
* Includes jig & probe total capacitance

TYPICAL A.C. CHARACTERISTICS

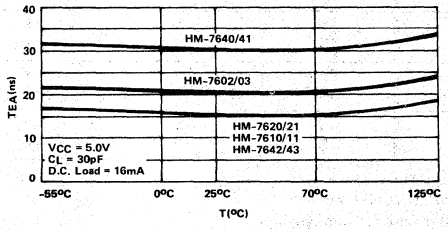
ADDRESS TO OUTPUT DELAY VS. TEMPERATURE



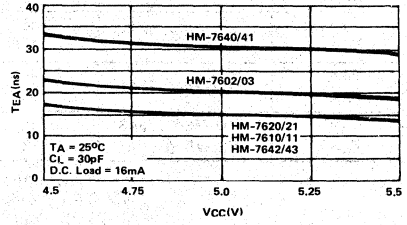
ADDRESS TO OUTPUT DELAY VS. SUPPLY VOLTAGE



CHIP SELECT TO OUTPUT DELAY VS. TEMPERATURE



CHIP SELECT TO OUTPUT DELAY VS. SUPPLY VOLTAGE



HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-76LS03

32 x 8 PROM
"Three State" Outputs

MAY 1978 ***Preliminary***

Features

- ULTRA LOW POWER - 60mW TYPICAL
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE - ONE PULSE/BIT TYPICAL, ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD.
- PIN COMPATIBLE WITH THE STANDARD 7603 PINOUT.

Description

The HM-76LS03 is an ultra low power version of the standard 7603 PROM, designed to be MOS compatible with it's low ICC specification. The HM-76LS03 is a fully decoded high speed Schottky TTL 256-Bit Field Programmable ROM in a 32 word by 8 bit/word format with "Three State" outputs. This PROM is available in a 16 pin DIP (ceramic or epoxy).

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

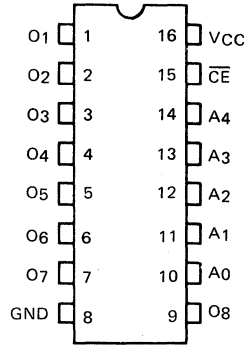
Nichrome fuse technology is used on this and all other Harris Bipolar PROMs.

The HM-76LS03 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

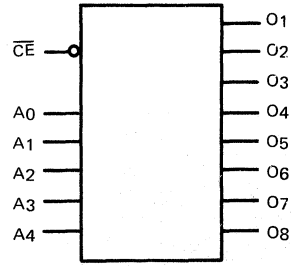
There is a Chip Enable on the HM-76LS03, $\overline{CE}$ low enables the device.

Pinout

TOP VIEW—DIP



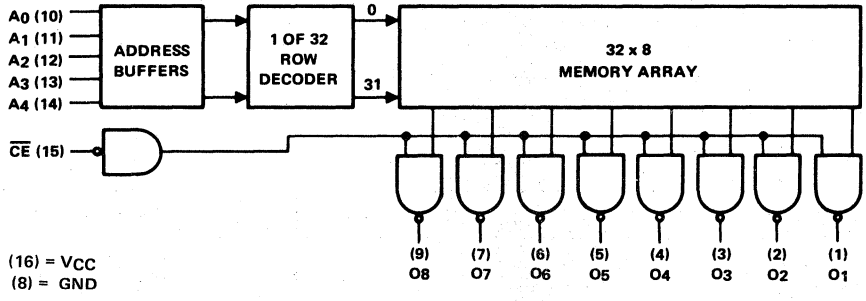
Logic Symbol



PIN NAMES

A0 - A4	Address Inputs
O1 - O8	Data Outputs
$\overline{CE}$	Chip Enable Input

Functional Diagram



(16) = VCC
(8) = GND

ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage Ratings (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	+5.5V	Operating Temperature (Ambient)	0°C to +75°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-76LS03-5 (V_{CC} = 5.0V ± 5%, T_A = 0°C to +75°C)

SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable Input Current	"1" "0"	— —	— —	+40 -50	uA uA	V_{IH} = V_{CC} max V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold Voltage	"1" "0"	2.0 —	1.5 1.5	— 0.80	V V	V_{CC} = V_{CC} min V_{CC} = V_{CC} max
V_{OH} V_{OL}	Output Voltage	"1" "0"	2.4 —	3.4 0.34	— 0.45	V V	I_{OH} = -0.20mA V_{CC} = V_{CC} min. I_{OL} = +1.0mA V_{CC} = V_{CC} min.
I_{OHE} I_{OLE}	Output Disable Current	"1" "0"	— —	— —	+100 -100	uA uA	V_{OH}, V_{CC} = V_{CC} max V_{OL} = +0.3V V_{CC} = V_{CC} max
V_{CL}	Input Clamp Voltage		—	—	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current		-2	—	-20	mA	V_{OUT} = 0.0V one output only for a max of one second.
I_{CC}	Power Supply Current		—	12	25	mA	V_{CC} = V_{CC} max all inputs grounded

Typical measurements are at T_A = 25°C, V_{CC} = +5V
NOTE: Positive current defined as into the device terminals.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

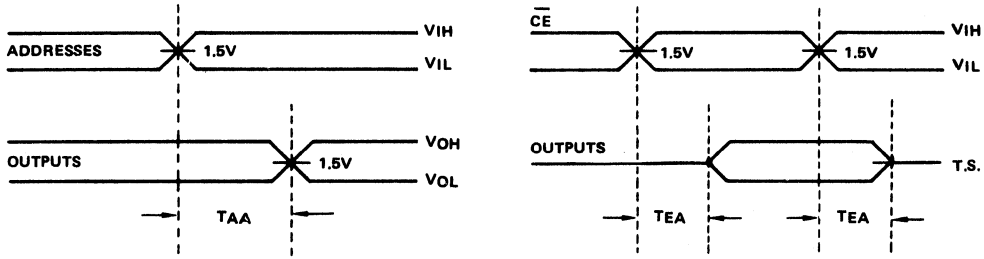
		HM-76LS03-5 5V ± 5% 0°C to +75°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
TAA TEA	Address Access Time Chip Enable Access Time	— —	300 300	500 500	ns ns

A.C. limits guaranteed for worst case N^2 sequencing.

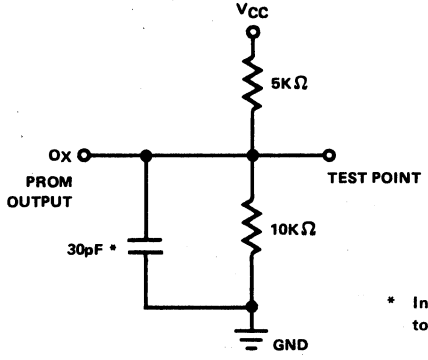
CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	MAX	UNIT	TEST CONDITIONS
C_{INA}, C_{INCE} C_{OUT}	Input Capacitance Output Capacitance	12 12	pF pF	V_{CC} = 5V, V_{IN} = 2.0, f = 1MHz V_{CC} = 5V, V_{OUT} = 2.0, f = 1MHz

SWITCHING TIME DEFINITIONS



A.C. TEST LOAD



2

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-7608

1K x 8 PROM

APRIL 1978 *Preliminary*

Features

- 60ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OUTPUTS WITH A CHIP ENABLE INPUT
- SIMPLE, HIGH SPEED PROGRAMMING PROCEDURE – ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME – GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD
- PIN COMPATIBLE WITH THE 2708 WITH:
  - ONLY ONE 5 VOLT SUPPLY
  - SUPERIOR ACCESS TIME
  - FASTER PROGRAMMING TIME

Description

The HM-7608 is a fully decoded high speed Schottky TTL 8192-Bit Field Programmable ROM in a 1K word by 8 bit/word format and is available in a 24 pin D.I.P. (ceramic or epoxy) and a 24 pin flat pack.

All bits are manufactured storing a logical "1" (Positive Logic) and can be selectively programmed for a logical "0" in any bit position, the HM-7608 has "Three State" outputs.

Nichrome fuse technology is used on this and all other Harris Bipolar PROM's.

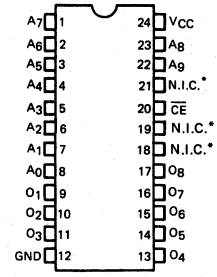
The HM-7608 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

This PROM is a plug in replacement for the 2708 where the V_{SS} pin on the 2708 becomes GND on the HM-7608. The V_{BB}, V_{DD}, and program pins on the 2708 are all N.C. on the HM-7608.

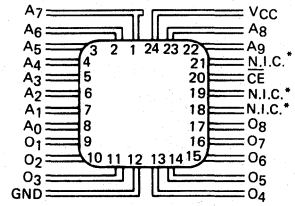
There is a chip enable input on the HM-7608 where $\overline{CE}$ low enables the device.

Pinouts

TOP VIEW – DIP



TOP VIEW – FLATPACK

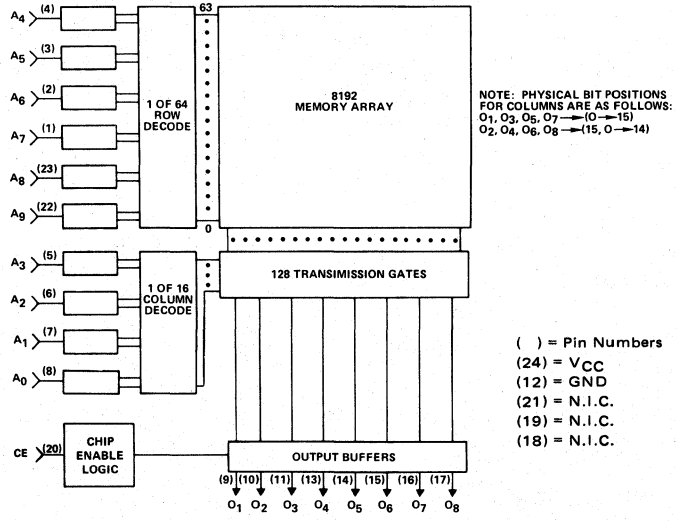


PIN NAMES

$A_0 - A_9$	Address Inputs
$O_1 - O_8$	Data Outputs
$\overline{CE}$	Chip Enable Input

*No Internal Connect

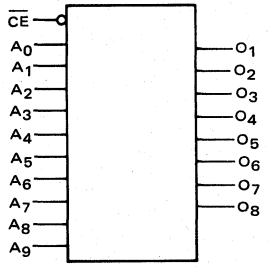
Functional Diagram



NOTE: PHYSICAL BIT POSITIONS FOR COLUMNS ARE AS FOLLOWS:
$O_1, O_3, O_5, O_7 \rightarrow (0 \rightarrow 15)$
$O_2, O_4, O_6, O_8 \rightarrow (15, 0 \rightarrow 14)$

( ) = Pin Numbers
(24) = V_{CC}
(12) = GND
(21) = N.I.C.
(19) = N.I.C.
(18) = N.I.C.

Logic Symbol



ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7608-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7608-2 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/enable "1" Input Current "0"	– –	– -50.0	+40 -100	µA µA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	1.5 1.5	– 0.8	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4 –	3.2 0.35	– 0.45	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40 -40	µA µA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output S.C. Current	-15	–	-100	mA	V_{OUT} = 0.0V One Output Only for a Max. of 1 Second
I_{CC}	Power Supply Current	–	130	170	mA	V_{CC} = V_{CC} Max. All Inputs Grounded

NOTE: Positive current defined as into device terminals.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

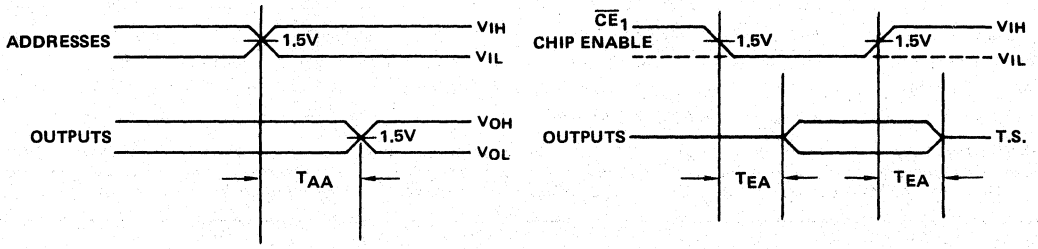
		HM-7608-5 5V ±5% 0°C to + 75°C			HM-7608-2 5V ±10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	–	45	60	–	–	80	ns
T_{EA}	Chip Enable Access Time	–	30	40	–	–	50	ns

A.C. limits guaranteed for worst case N^2 sequencing.

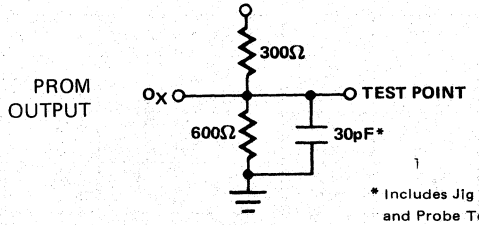
CAPACITANCE : T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
CINA, CINCE	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
COUT	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS



A.C. TEST LOAD



2

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-7610A/11A

256 x 4 PROM

HM-7610A - Open Collector Outputs
HM-7611A - "Three State" Outputs

DECEMBER 1977

Features

- 40ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS
- SIMPLE, HIGH SPEED PROGRAMMING PROCEDURE USING SINGLE PULSES, ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY
- INPUTS AND OUTPUTS TTL COMPATIBLE
- FAST ACCESS TIME – GUARANTEED FOR WORST CAST N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD
- PIN COMPATIBLE WITH INDUSTRY STANDARD PROM's AND ROM's

Description

The HM-7610A/11A are fully decoded high speed Schottky TTL 1024-Bit Field Programmable ROMs in a 256 word by 4 bit/word format with open collector (HM-7610A) or "three state" (HM-7611A) outputs. These PROMs are available in 16 pin D.I.P. (ceramic or epoxy) and a 16 pin flatpack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

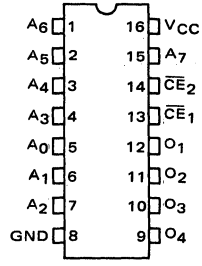
The HM-7610A/11A contain test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

This PROM is intended for use in state of the art ultra high speed logic systems.

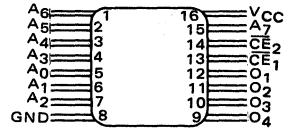
Nichrome fuse technology is used on these and all other Harris Bipolar PROM's.

Pinouts

TOP VIEW–DIP



TOP VIEW–FLAT PACK

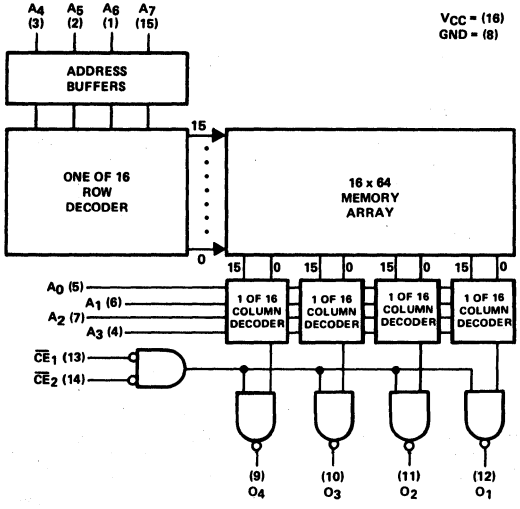


PIN NAMES

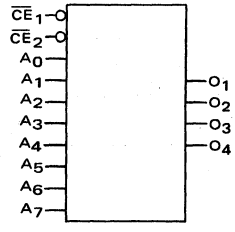
$A_0 - A_7$	Address Inputs
$O_1 - O_4$	Data Outputs
$\overline{CE}_1, \overline{CE}_2$	Chip Enable Inputs

2

Functional Diagram



Logic Symbol



ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7610A/11A-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7610A/11A-2 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	– –	– -50.0	+40 -250	µA µA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	1.5 1.5	– 0.8	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4* –	3.2* 0.35	– 0.45	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40 -40*	µA µA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output S.C. Current *	-15*	–	-100*	mA	V_{OUT} = 0.0V One Output Only for a Max. of 1 Second
I_{CC}	Power Supply Current	–	–	130	mA	V_{CC} = V_{CC} Max. All Inputs Grounded

*Not applicable to open collector.
NOTE: Positive current defined as into device terminals.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

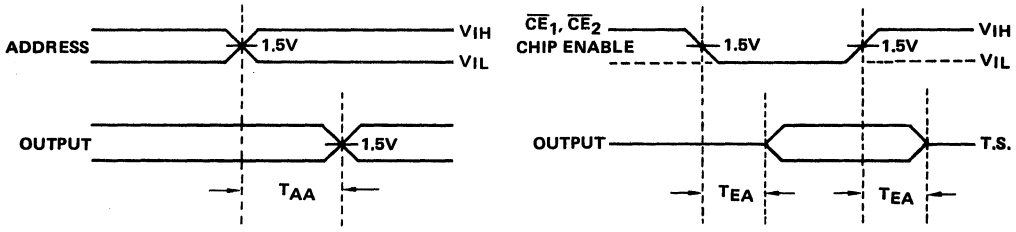
		HM-7610A/11A-5 5V ±5% 0°C to + 75°C			HM-7610A/11A-2 5V ±10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	–	–	40	–	–	60	ns
T_{EA}	Chip Enable Access Time	–	–	25	–	–	40	ns

A.C. limits guaranteed for worst case N^2 sequencing.

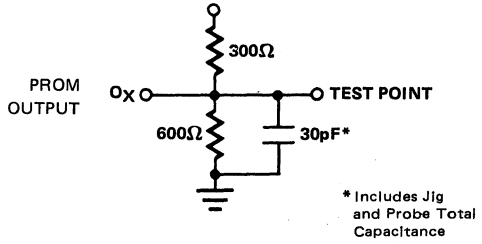
CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS



A.C. TEST LOAD



2

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-7616
2K x 8 PROM

MARCH 1978 ***Preview***

Features

- 60ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OUTPUTS AND A CHIP ENABLE INPUT
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE – ONE PULSE/BIT TYPICAL
- FAST ACCESS TIME – GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES
- INDUSTRY'S HIGHEST PROGRAMMING YIELD
- PIN COMPATIBLE WITH THE 2716

Description

HM-7616 is a fully decoded high speed Schottky TTL, 16,384 bit Field Programmable ROM in a 2K word by 8 bit/word format with "Three State" outputs. This PROM is available in a 24 pin DIP.

All bits are manufactured storing a logical "1" (Positive Logic) and can be selectively programmed for a logical "0" in any bit position.

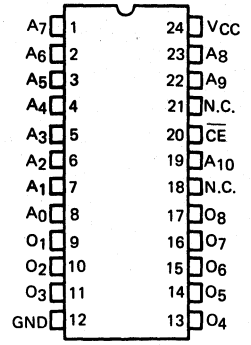
The nichrome fuse technology used is the same as all other Harris Bipolar PROMs and the JAN approved MIL-M-38510/201 PROM.

The HM-7616 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

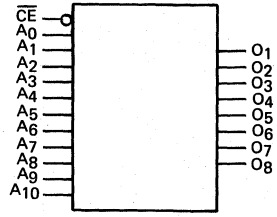
There is a chip enable input on the HM-7616. $\overline{CE}$ low enables the device.

Pinout

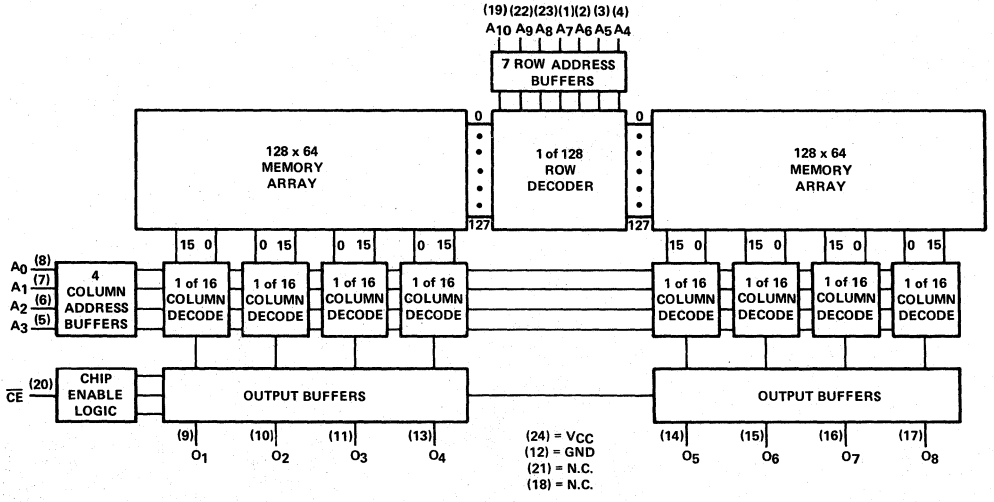
TOP VIEW - D I P



Logic Symbol



Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7616-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7616-2 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical Measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH}	Address/Enable "1"	–	–	+40	μA	V_{IH} = V_{CC} Max.
I_{IL}	Input Current "0"	–	-50.0	-250	μA	V_{IL} = 0.45V
V_{IH}	Input Threshold "1"	2.0	1.5	–	V	V_{CC} = V_{CC} Min.
V_{IL}	Voltage "0"	–	1.5	0.8	V	V_{CC} = V_{CC} Max.
V_{OH}	Output "1"	2.4*	3.2	–	V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min.
V_{OL}	Voltage "0"	–	0.35	0.50	V	I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE}	Output Disable "1"	–	–	+40	μA	V_{OH}, V_{CC} = V_{CC} Max.
I_{OLE}	Current "0"	–	–	-40*	μA	V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15	–	-100	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	–	180	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

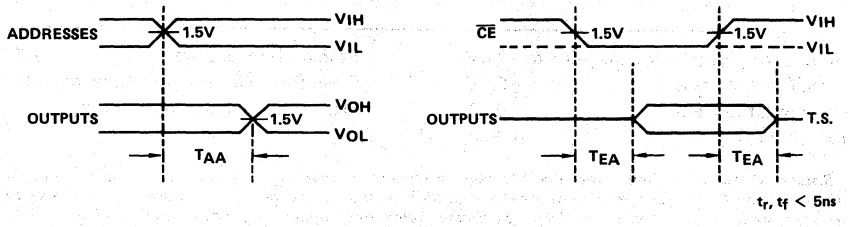
		HM-7616-5 5V ±5% 0°C to +75°C			HM-7616-2 5V ±10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	–	45	60	–	–	80	ns
T_{EA}	Chip Enable Access Time	–	30	40	–	–	50	ns

A.C. limits guaranteed for worst case N^2 sequencing.

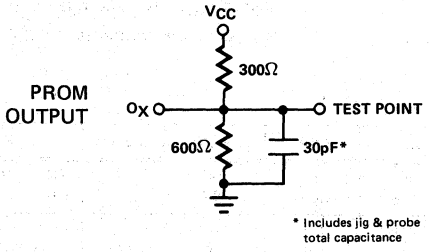
CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS



A.C. TEST LOAD



2

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

MARCH 1978 **Preview**

HM-76160/161

2K x 8 PROMS

HM-76161 — "Three State" Outputs
HM-76160 — Open Collector Outputs

Features

- 60ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND THREE CHIP
- ENABLE INPUTS
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE – ONE PULSE/BIT TYPICAL
- FAST ACCESS TIME – GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES
- INDUSTRY'S HIGHEST PROGRAMMING YIELD

Description

The HM-76160/161 are fully decoded high speed Schottky TTL 16,384 bit Field Programmable ROMs in a 2K word by 8 bit/word format with open collector (HM-76160) or "Three State" (HM-76161) outputs. These PROMs are available in a 24 pin DIP.

All bits are manufactured storing a logical "1" (Positive Logic) and can be selectively programmed for a logical "0" in any bit position.

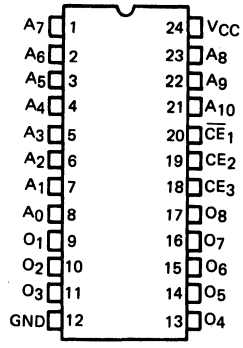
The nichrome fuse technology used is the same as all other Harris Bipolar PROMs and the JAN approved MIL-M-38510/201 PROM.

The HM-76160/161 contain test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

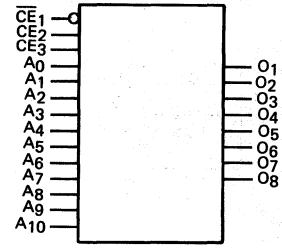
There are three chip enable inputs on the HM-76160/161. $\overline{CE}_1$ low, CE_2 high, and CE_3 high enables the device.

Pinout

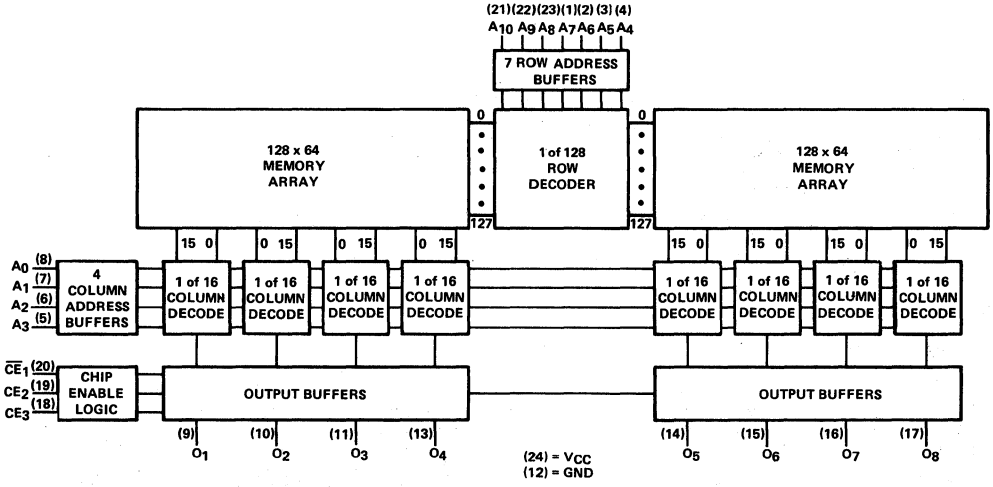
TOP VIEW - D I P



Logic Symbol



Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-76160/161-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-76160/161-2 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical Measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH}	Address/Enable "1"	–	–	+40	µA	V_{IH} = V_{CC} Max.
I_{IL}	Input Current "0"	–	-50.0	-250	µA	V_{IL} = 0.45V
V_{IH}	Input Threshold "1"	2.0	1.5	–	V	V_{CC} = V_{CC} Min.
V_{IL}	Voltage "0"	–	1.5	0.8	V	V_{CC} = V_{CC} Max.
V_{OH}	Output "1"	2.4*	3.2*	–	V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min.
V_{OL}	Voltage "0"	–	0.35	0.50	V	I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE}	Output Disable "1"	–	–	+40	µA	V_{OH}, V_{CC} = V_{CC} Max.
I_{OLE}	Current "0"	–	–	-40*	µA	V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15*	–	-100*	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	–	180	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.
*"Three State" only

A.C. ELECTRICAL CHARACTERISTICS (Operating)

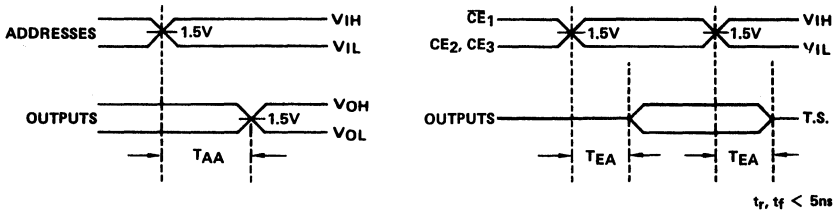
		HM-76160/161-5 5V ±5% 0°C to +75°C			HM-76160/161-2 5V ±10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	–	45	60	–	–	80	ns
T_{EA}	Chip Enable Access Time	–	30	40	–	–	50	ns

A.C. limits guaranteed for worst case N^2 sequencing.

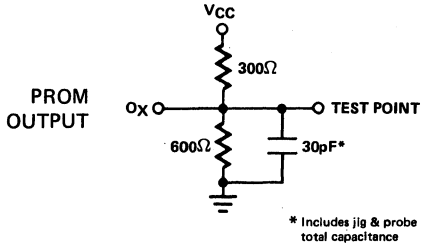
CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS



A.C. TEST LOAD



2

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-7620A/21A

512 x 4 PROM

HM-7620A - Open Collector Outputs
HM-7621A - "Three State" Outputs

DECEMBER 1977

Features

- 45ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS
- SIMPLE, HIGH SPEED PROGRAMMING PROCEDURE USING SINGLE PULSES, ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- INPUTS AND OUTPUTS TTL COMPATIBLE
- FAST ACCESS TIME – GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD
- PIN COMPATIBLE WITH INDUSTRY STANDARD PROM's AND ROM's.

Description

The HM-7620A/21A are fully decoded high speed Schottky TTL 2048-Bit Field Programmable ROM's in a 512 word by 4 bit/word format with open collector (HM-7620A) or "three state" (HM-7621A) outputs. These PROMs are available in 16 pin D.I.P. (ceramic or epoxy) and a 16 pin flatpack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

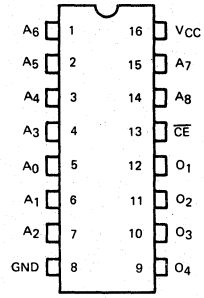
The HM-7620A/21A contain test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

This PROM is intended for use in state of the art ultra high speed logic systems.

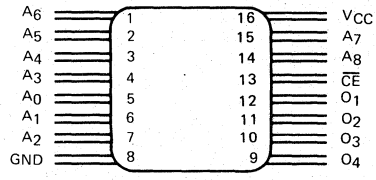
Nichrome fuse technology is used on these and all other Harris Bipolar PROM's.

Pinouts

TOP VIEW - DIP



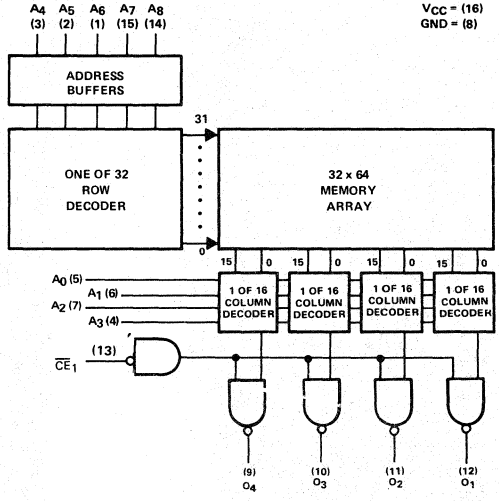
TOP VIEW – FLATPACK



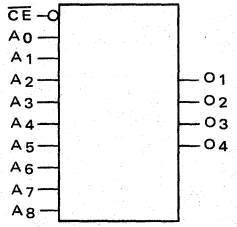
PIN NAMES

$A_0 - A_8$	Address Inputs
$\overline{CE}$	Chip Enable Input
$O_1 - O_4$	Data Outputs

Functional Diagram



Logic Symbol



ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7620A/21A-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7620A/21A-2 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/enable "1" Input Current "0"	– –	– -50,0	+40 -250	µA µA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	1.5 1.5	– 0.8	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4* –	3.2* 0.35	– 0.45	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40 -40*	µA µA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output S.C. Current	-15*	–	-100*	mA	V_{OUT} = 0.0V One Output Only for a Max. of 1 Second
I_{CC}	Power Supply Current	–	90	130	mA	V_{CC} = V_{CC} Max. All Inputs Grounded

*"Three State" only
NOTE: Positive current defined as into device terminals.

2

A.C. ELECTRICAL CHARACTERISTICS (Operating)

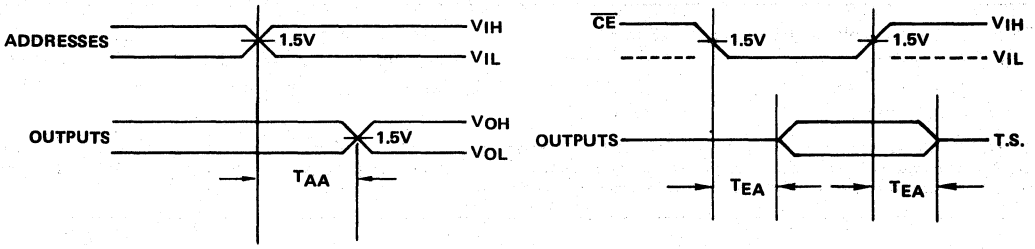
		HM-7620A/21A - 5 5V ±5% 0°C to + 75°C			HM-7620A/21A -2 5V ±10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	–	–	45	–	–	60	ns
T_{EA}	Chip Enable Access Time	–	–	25	–	–	40	ns

A.C. limits guaranteed for worst case N^2 sequencing.

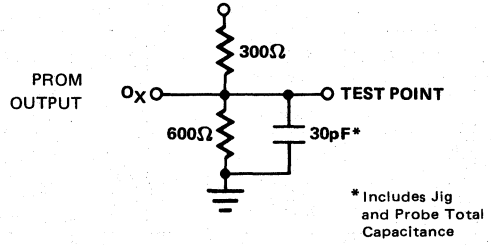
CAPICITANCE: T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS



A.C. TEST LOAD



2

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-7625R

256 x 8 PROM

"Three State" Outputs

MAY 1978

Features

- 60ns MAXIMUM ADDRESS ACCESS TIME.
- "THREE STATE" OUTPUTS WITH TWO CHIP ENABLE INPUTS.
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE-ONE PULSE/BIT TYPICAL. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME - GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD.

Description

The HM-7625R is a fully decoded high speed Schottky TTL 2048-Bit Field Programmable ROM in a 256 word by 8 bit/word format and is available in a 24 pin DIP (ceramic or epoxy).

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

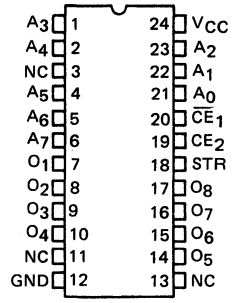
Nichrome fuse technology is used on this and all other Harris Bipolar PROMs.

The HM-7625R contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

There are two chip enables on the HM-7625R. $\overline{CE}_1$ low and CE_2 high enables the chip.

Pinout

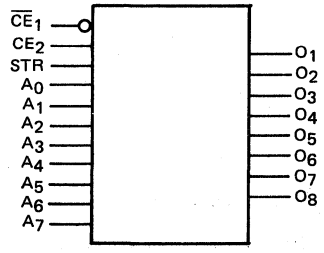
TOP VIEW – DIP



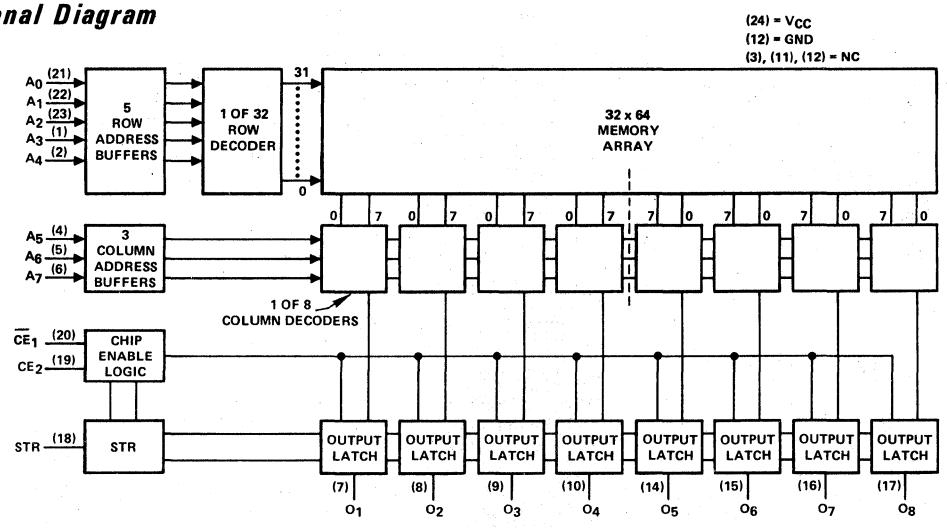
PIN NAMES

$A_0 - A_7$	Address Inputs
$O_1 - O_8$	Data Outputs
CE_1', CE_2	Chip Enable Inputs
STR	Strobe Input

Logic Symbol



Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7625R-5 (V_{CC} = 5.0V ± 5%, T_A = 0°C to +75°C)
HM-7625R-2 (V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH}	Address/Enable "1"	–	–	+25	μA	V_{IH} = V_{CC} Max.
I_{IL}	Input Current "0"	–	-50.0	-100(1)	μA	V_{IL} = 0.45V
V_{IH}	Input Threshold "1"	2.0	1.5	–	V	V_{CC} = V_{CC} Min.
V_{IL}	Voltage "0"	–	1.5	0.85	V	V_{CC} = V_{CC} Max.
V_{OH}	Output "1"	2.7(2)	3.3	–	V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min.
V_{OL}	Voltage "0"	–	0.35	0.50	V	I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE}	Output Disable "1"	–	–	+40	μA	V_{OH}, V_{CC} = V_{CC} Max.
I_{OLE}	Current "0"	–	–	-40	μA	V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-20	–	-70	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	135	185	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.
NOTE(1): I_{IL} = -150μA for -2
NOTE(2): V_{OH} = 2.4V for -2

A.C. ELECTRICAL CHARACTERISTICS (Operating)

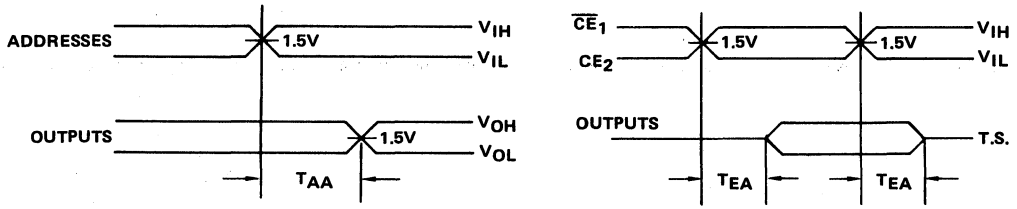
		HM-7625R-5 5V ±5% 0°C to +75°C			HM-7625R-2 5V ±10% -55°C to +125°C				
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS	TEST CONDIT.
T_{AA}	Address Access Time	–	40	60	–	50	80	ns	Latched or
T_{EA}	Chip Enable Access Time	–	30	40	–	40	50	ns	Transparent
T_{ADH}	Address Hold Time	0	-10	–	0	-10	–	ns	Latched Only
T_{CDH}	Chip Enable Hold Time	10	0	–	10	0	–	ns	
T_{SW}	Strobe Pulse Width	30	15	–	40	15	–	ns	
T_{SL}	Strobe Latch Time	60	35	–	80	45	–	ns	
T_{DL}	Strobe Delatch Time	–	–	40	–	–	50	ns	
T_{CDS}	Chip Enable Set-Up Time	40	–	–	50	–	–	ns	

A.C. limits guaranteed for worst case N^2 sequencing.

CAPACITANCE (1): T_A = 25°C

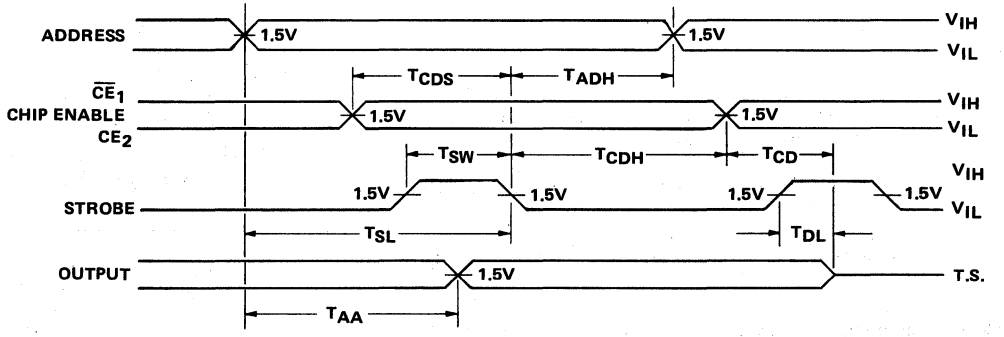
SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS (Transparent Mode)

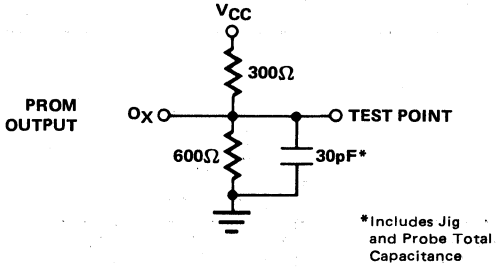


NOTE: Strobe input must remain high throughout read cycle while in the transparent mode.

SWITCHING TIME DEFINITIONS (Latched Mode)



A.C. TEST LOAD



HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-7629

256 x 8 PROM

"Three State" Outputs

MAY 1978

Features

- 70ns MAXIMUM ADDRESS ACCESS TIME.
- "THREE STATE" OUTPUTS WITH FOUR CHIP ENABLE INPUTS.
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE - ONE PULSE/BIT TYPICAL. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME - GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD.

Description

The HM-7629 is a fully decoded high speed Schottky TTL 2048-Bit Field Programmable ROM in a 256 word by 8 bit/word format and is available in a 24 pin DIP (ceramic or epoxy).

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

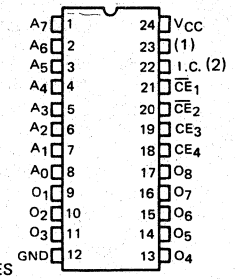
Nichrome fuse technology is used on this and all other Harris Bipolar PROMs.

The HM-7629 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

There are four chip enables on the HM-7629. $\overline{CE}_1$ low, $\overline{CE}_2$ low, CE_3 high , and CE_4 high enables the chip.

Pinout

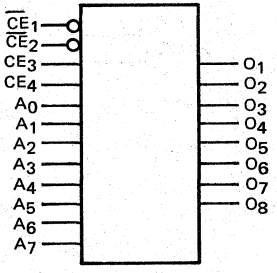
TOP VIEW – DIP



PIN NAMES

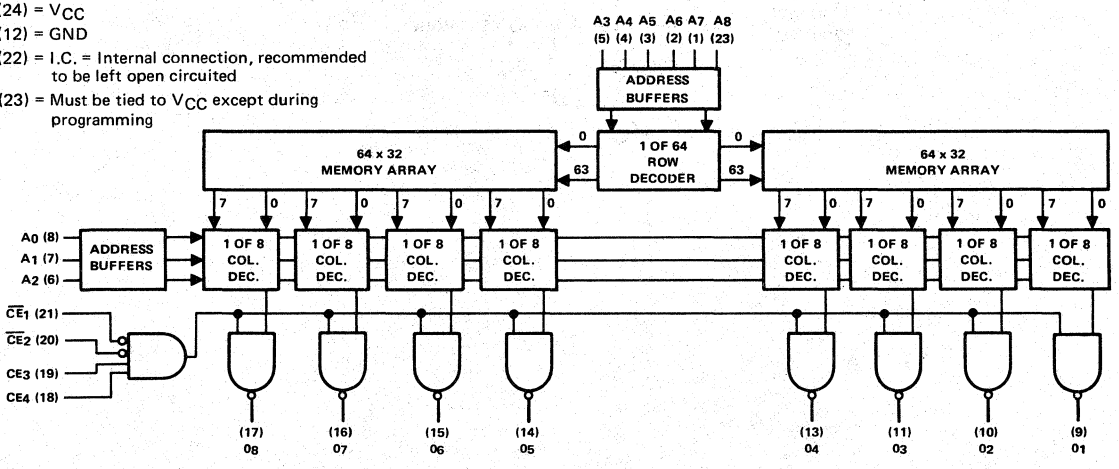
$A_0 - A_7$ Address Inputs
$O_1 - O_8$ Data Outputs
$\overline{CE}_1$, $\overline{CE}_2$, CE_3, CE_4 Chip Enable Inputs
(1) Pin 23 must be tied to V_{CC} except during programming
(2) Internal Connection

Logic Symbol



Functional Diagram

(24) = V_{CC}
(12) = GND
(22) = I.C. = Internal connection, recommended to be left open circuited
(23) = Must be tied to V_{CC} except during programming



ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	0°C to +75C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7629-5 (V_{CC} = 5.0V + 5%, T_A = 0°C to +75°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable*"1" Input Current "0"	– –	– -50.0	+40 -250	µA µA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	1.5 1.5	– 0.80	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4 –	3.4 0.35	– 0.45	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+100 -100	µA µA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15	–	-100	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	125	170	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.
*Enable current measured using only one enable input at a time to disable the device.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

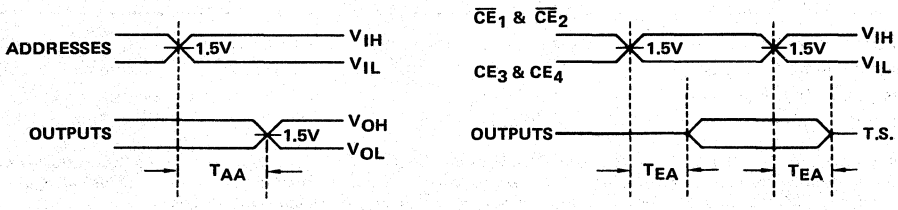
		HM-7629-5 5V ± 5% 0°C to +75°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	–	45	70	ns
T_{EA}	Chip Enable Access Time	–	30	40	ns

A.C. limits guaranteed for worst case N^2 sequencing.

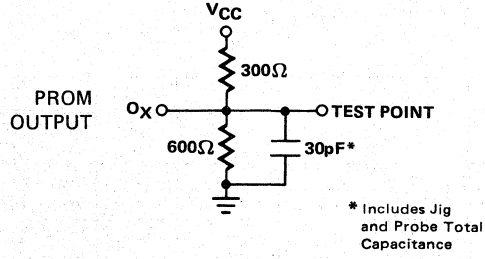
CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	12	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	12	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS



A.C. TEST LOAD



HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-7640A/41A

512 x 8 PROM

HM-7640A - Open Collector Outputs
HM-7641A - "Three State" Outputs

APRIL 1978

Features

- 50ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND FOUR CHIPS ENABLE INPUTS.
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE — ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME – GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD
- LOW INPUT LOADING

Description

The HM-7640A/41A are fully decoded high speed Schottky TTL 4096-Bit Field Programmable ROMs in a 512 word by 8 bit/word format and are available in a 24 pin DIP (ceramic or epoxy) and a 24 pin flatpack.

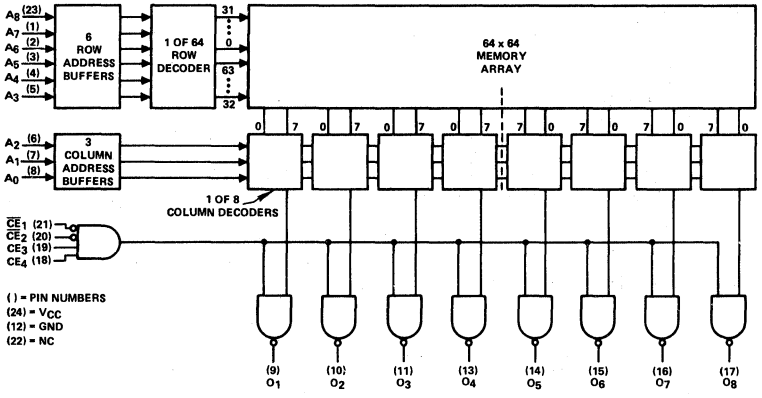
All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

Nichrome fuse technology is used on this and all other Harris Bipolar PROM's.

The HM-7640A/41A contain test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

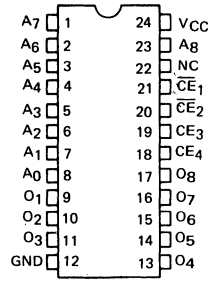
There are four chip enable inputs on the HM-7640A/41A where $\overline{CE}_1$, and $\overline{CE}_2$ low and CE_3 and CE_4 high enables the chip.

Functional Diagram

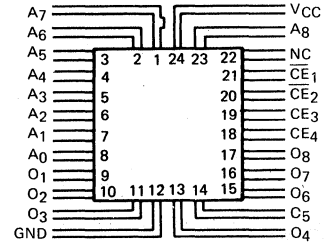


Pinouts

TOP VIEW – DIP



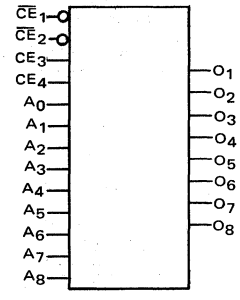
TOP VIEW – FLATPACK



PIN NAMES

$A_0 - A_8$	Address Inputs
$O_1 - O_8$	Data Outputs
$\overline{CE}_1, \overline{CE}_2, CE_3, CE_4$	Chip Enable Inputs

Logic Symbol



ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7640A/41A-5 (V_{CC} = 5.0V ± 5%, T_A = 0°C to +75°C)
HM-7640A/41A-2 (V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	– –	– -50.0	+40 -250	μA μA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	1.5 1.5	– 0.8	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4* –	3.2* 0.35	– 0.45	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40 -40*	μA μA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15*	–	-100*	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	125	170	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.
*"Three State" only

A.C. ELECTRICAL CHARACTERISTICS (Operating)

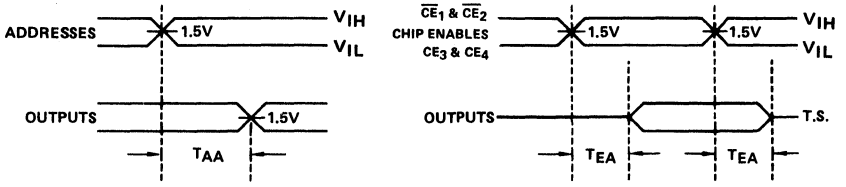
		HM-7640A/41A 5V ±5% 0°C to +75°C			HM-7640A/41A 5V ±10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	–	35	50	–	–	70	ns
T_{EA}	Chip Enable Access Time	–	30	40	–	–	50	ns

A.C. limits guaranteed for worst case N^2 sequencing.

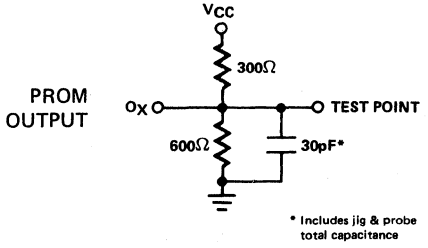
CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
CINA, CINCE	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
COUT	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS



A.C. TEST LOAD



HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-7640AR/41AR

512 x 8 PROM

HM-7640AR - Open Collector Outputs
HM-7641AR - "Three State" Outputs

APRIL 1978 **Preview**

Features

- 50ns MAXIMUM ADDRESS ACCESS TIME.
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS WITH THREE CHIP ENABLE INPUTS.
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE - ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME - GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD.
- LATCHED OUTPUTS.
- LOW INPUT LOADING.

Description

The HM-7640AR/41AR are fully decoded high speed Schottky TTL 4096 Bit Field Programmable ROMs in a 512 word by 8 bit/word format and are available in a 24-pin DIP (ceramic or epoxy) and a 24-pin flat pack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

Nichrome fuse technology is used on this and all other Harris Bipolar PROMs.

The HM-7640AR/41AR contain test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

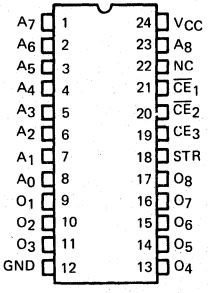
There are three chip enable inputs on the HM-7640AR/41AR, $\overline{CE}_1$, $\overline{CE}_2$ low and CE_3 high enables the chip.

HM-7640AR/41AR are operated in the Transparent Read Mode by holding the strobe input high throughout the read operation. This is the normal read mode where the three chip enable inputs will control the outputs.

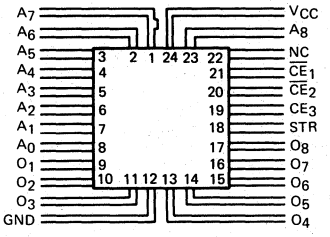
In Latched Read Mode, bringing the strobe input low will latch the outputs and chip enable inputs. If the device is disabled, when the strobe input goes low the outputs will be latched in the high impedance state. If the device is in the latched mode the strobe input must be brought high to allow the outputs to respond to new address or chip enable conditions.

Pinouts

TOP VIEW – DIP



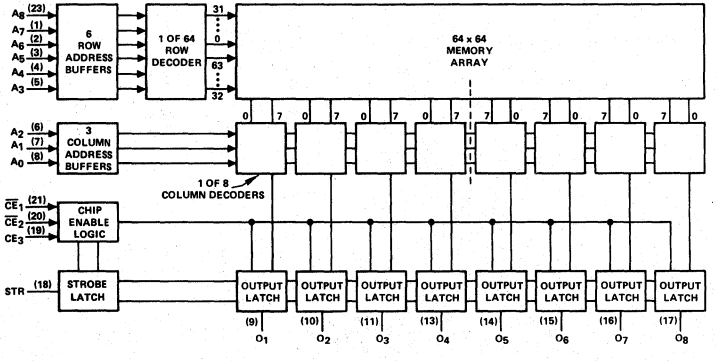
TOP VIEW – FLATPACK



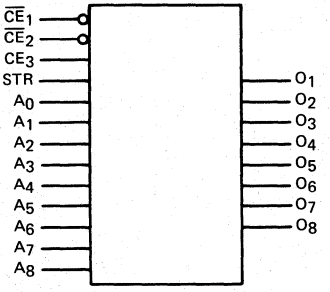
PIN NAMES

$A_0 - A_8$	Address Inputs
$O_1 - O_8$	Data Outputs
$\overline{CE}_1$, $\overline{CE}_2$, CE_3	Chip Enable Inputs
STR	Latch Input

Functional Diagram



Logic Symbol



ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7640AR/41AR-5 (V_{CC} = 5.0V ± 5%, T_A = 0°C to +75°C)
HM-7640AR/41AR-2 (V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH}	Address/Enable "1"	–	–	+40	μA	V_{IH} = V_{CC} Max.
I_{IL}	Input Current "0"	–	-50.0	-250	μA	V_{IL} = 0.45V
V_{IH}	Input Threshold "1"	2.0	1.5	–	V	V_{CC} = V_{CC} Min.
V_{IL}	Voltage "0"	–	1.5	0.8	V	V_{CC} = V_{CC} Max.
V_{OH}	Output "1"	2.4*	3.2*	–	V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min.
V_{OL}	Voltage "0"	–	0.35	0.45	V	I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE}	Output Disable "1"	–	–	+40	μA	V_{OH}, V_{CC} = V_{CC} Max.
I_{OLE}	Current "0"	–	–	-40*	μA	V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15*	–	-100*	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	–	180	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.
*"Three State" only

A.C. ELECTRICAL CHARACTERISTICS (Operating)

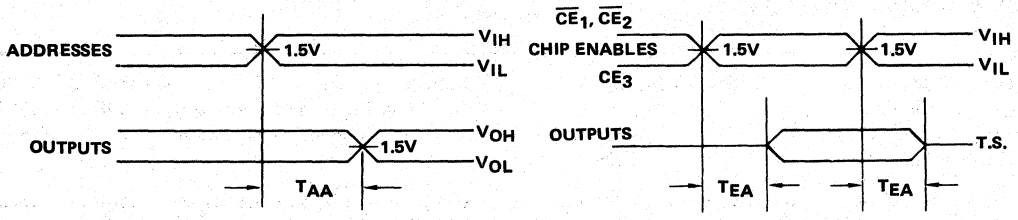
		HM-7640AR/41AR-5 5V ±5% 0°C to +75°C			HM-7640AR/41AR-2 5V ±10% -55°C to +125°C				
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS	TEST CONDIT.
T_{AA}	Address Access Time	–	35	50	–	–	70	ns	Latched or
T_{EA}	Chip Enable Access Time	–	30	40	–	–	50	ns	Transparent
T_{ADH}	Address Hold Time	0	-10	–	0	-10	–	ns	Latched Only
T_{CDH}	Chip Enable Hold Time	10	0	–	10	0	–	ns	
T_{SW}	Strobe Pulse Width	30	15	–	40	15	–	ns	
T_{SL}	Strobe Latch Time	60	35	–	80	45	–	ns	
T_{DL}	Strobe Delatch Time	–	–	40	–	–	50	ns	
T_{CDS}	Chip Enable Set-Up Time	40	–	–	50	–	–	ns	

A.C. limits guaranteed for worst case N^2 sequencing.

CAPACITANCE: T_A = 25°C

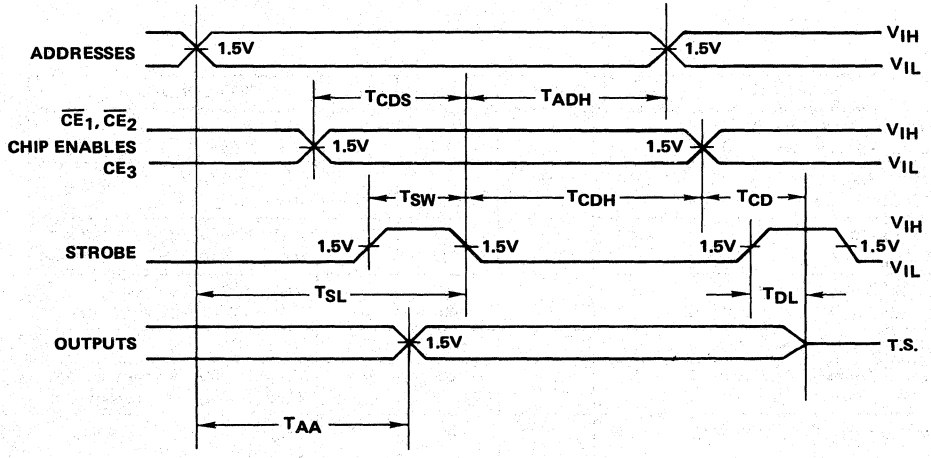
SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
CINA, CINCE	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
COUT	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS (Transparent Mode)

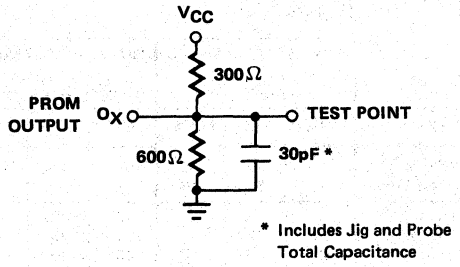


NOTE: Strobe input must remain high throughout read cycle while in transparent mode.

SWITCHING TIME DEFINITIONS (Latched Mode)



A.C. TEST LOAD



HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-7642A/43A

1K x 4 PROM

HM-7642A - Open Collector Outputs
HM-7643A - "Three State" Outputs

MARCH 1978

Features

- 50ns MAXIMUM ADDRESS ACCESS TIME.
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND TWO CHIP ENABLE INPUTS
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME - GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD.

Description

The HM-7642A/43A are fully decoded high speed Schottky TTL 4096-Bit Field Programmable ROMs in a 1K words by 4 Bit/word format with open collector(HM-7642A) or "Three State" (HM-7643A) outputs. These PROM's are available in an 18–pin DIP (ceramic or epoxy) and an 18–pin flat pack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

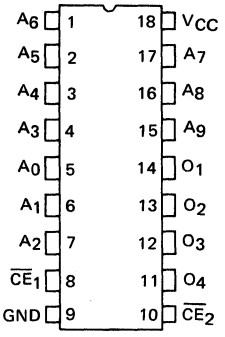
Nichrome fuse technology is used on this and all other Harris Bipolar PROMs.

The HM-7642A/43A contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

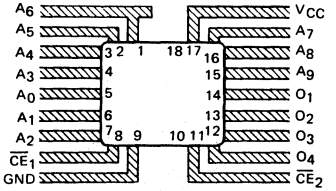
There are two chip enable inputs on the HM-7642A/43A. $\overline{CE}_1$ and $\overline{CE}_2$ low enables the chip.

Pinout

TOP VIEW–DIP



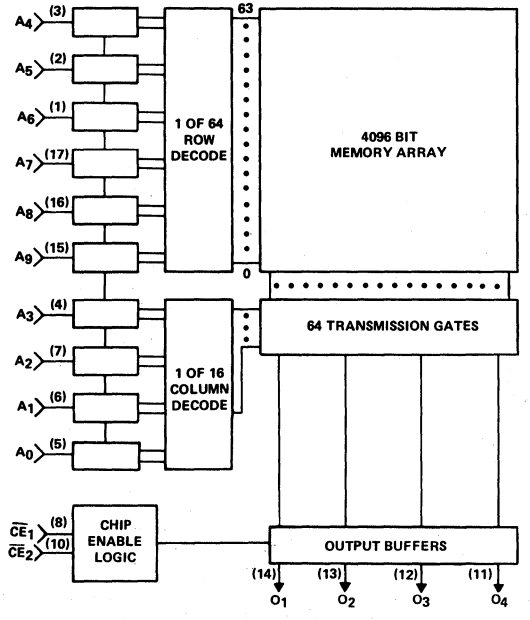
TOP VIEW–FLAT PACK



PIN NAMES

$A_0 - A_9$	ADDRESS INPUTS
$O_1 - O_4$	DATA OUTPUTS
$\overline{CE}_1, \overline{CE}_2$	CHIP ENABLE INPUTS

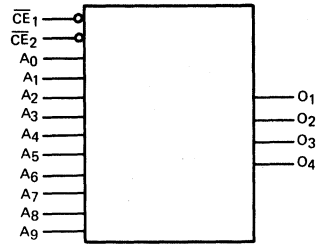
Functional Diagram



NOTE: Physical bit positions for columns are as follows:
O_2, O_4 = (0 → 15)
O_1, O_3 = (15, 0 → 14)

( ) = PIN NUMBERS
(18) = V_{CC}
(9) = GND

Logic Symbol



ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7642A/43A-5 V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7642A/43A-2 V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical Measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	– –	– -50.0	+40 -250	µA µA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	1.5 1.5	– 0.8	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4* –	3.2* 0.35	– 0.45	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40 -40*	µA µA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15*	–	-100*	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	100	140	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.
*"Three State" only

A.C. ELECTRICAL CHARACTERISTICS (Operating)

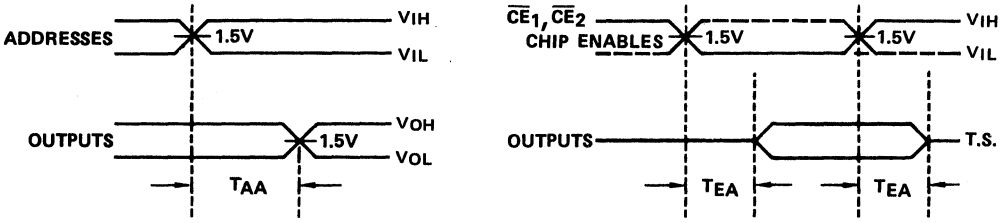
		HM-7642A/43A 5V ±5% 0°C to +75°C			HM-7642A/43A 5V ±10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	–	35	50	–	–	70	ns
T_{EA}	Chip Enable Access Time	–	25	30	–	–	40	ns

A.C. limits guaranteed for worst case N^2 sequencing.

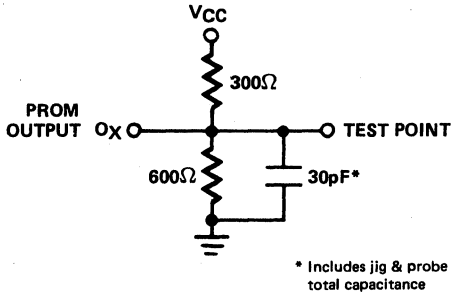
CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS



A.C. TEST LOAD



HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-7642P/43P

1K x 4 PROM

HM-7642P - Open Collector Outputs
HM-7643P - "Three State" Outputs

MARCH 1978 **Preview**

Features

- 50ns MAXIMUM ADDRESS ACCESS TIME.
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS, A POWER DOWN INPUT, AND A CHIP ENABLE INPUT.
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE - ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD.

Description

The HM-7642P/43P are fully decoded high speed SchottkyTTL 4096-Bit Field Programmable ROMs in a 1K words by 4 bit/word format with open collector (HM-7642P) or "Three State" (HM-7643P) outputs. These PROM s are available in an 18-pin DIP (ceramic or epoxy) and an 18-pin flat pack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

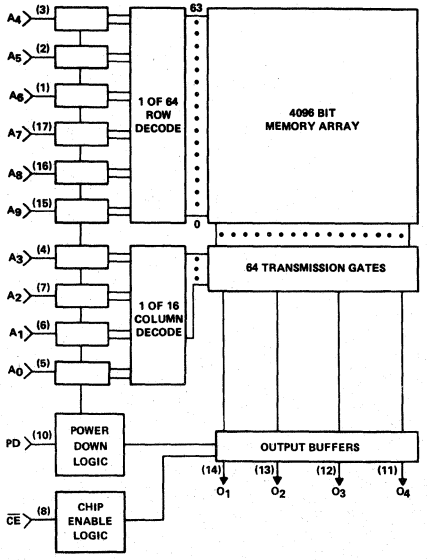
Nichrome fuse technology is used on these and all other Harris Bipolar PROMs.

The HM-7642P/43P contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

There is a power down input on the HM-7642P/43P which is similar to a chip enable. The chip can be enabled or disabled using the power down input where a powered down chip dissipates 25% of nominal power and the outputs go to a high impedance state. The chip is powered up when PD_1 is low.

There is also the conventional chip enable input on this device, $\overline{CE}$ low and PD_1 low enables the device.

Functional Diagram



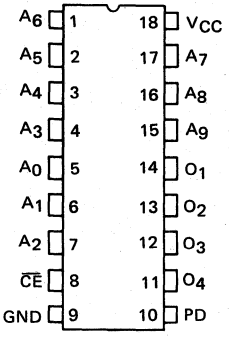
NOTE: Physical bit positions for columns are as follows:

O_1, O_3 = (15, 0 ⟶ 14)
O_2, O_4 = (0 ⟶ 15)

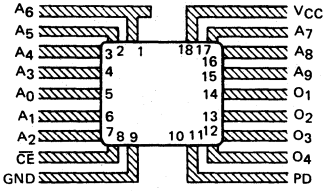
( ) = Pin Numbers
(18) = V_{CC}
(9) = GND

Pinout

TOP VIEW — DIP



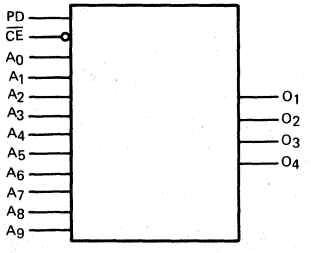
TOP VIEW — FLAT PACK



PIN NAMES

$A_0 - A_9$	ADDRESS INPUTS
$O_1 - O_4$	DATA OUTPUTS
PD	POWER DOWN INPUT
$\overline{CE}$	CHIP ENABLE INPUT

Logic Symbol



ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7642P/43P-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7642P/43P-2 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical Measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH}	Address/Enable "1"	–	–	+40	µA	V_{IH} = V_{CC} Max.
I_{IL}	Input Current "0"	–	-50.0	-250	µA	V_{IL} = 0.45V
V_{IH}	Input Threshold "1"	2.0	1.5	–	V	V_{CC} = V_{CC} Min.
V_{IL}	Voltage "0"	–	1.5	0.8	V	V_{CC} = V_{CC} Max.
V_{OH}	Output "1"	2.4*	3.2*	–	V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min.
V_{OL}	Voltage "0"	–	0.35	0.45	V	I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE}	Output Disable "1"	–	–	+40	µA	V_{OH}, V_{CC} = V_{CC} Max.
I_{OLE}	Current "0"	–	–	-40*	µA	V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15*	–	-100*	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	100	140	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.
*"Three State" only

A.C. ELECTRICAL CHARACTERISTICS (Operating)

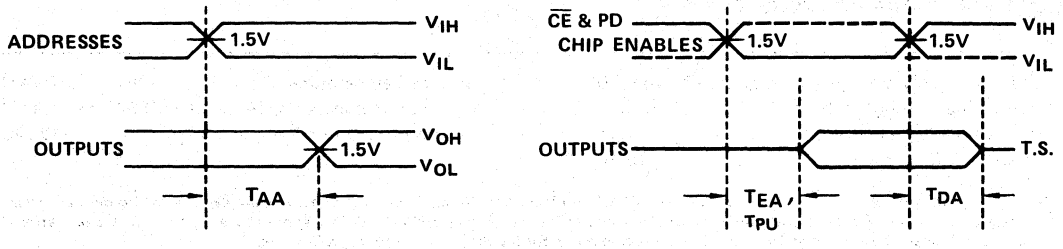
		HM-7642P/43P-5 5V ± 5% 0°C to +75°C			HM-7642P/43P-2 5V ± 10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	-	35	50	-	-	70	ns
T_{DA}	Chip Disable Access Time	-	25	30	-	-	40	ns
T_{PU}	Chip Power-Up Access Time	-	80	100	-	-	150	ns

A.C. limits guaranteed for worst case N^2 sequencing.

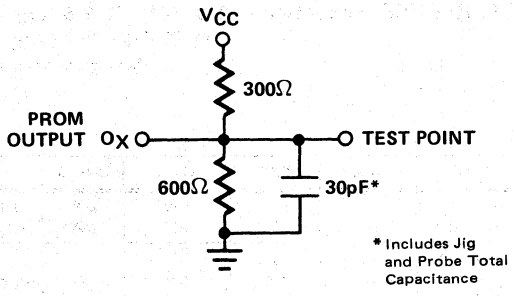
CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS



A.C. TEST LOAD



2

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-7644A

1K x 4 PROM

Active Pull-up Outputs

MARCH 1978

Features

- 50ns MAXIMUM ADDRESS ACCESS TIME
- ACTIVE PULL-UP OUTPUTS
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE ONE PULSE/BIT ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY
- FAST ACCESS TIME - GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES
- INDUSTRY'S HIGHEST PROGRAMMING YIELD
- LOW PIN COUNT FOR MAXIMUM DENSITY

Description

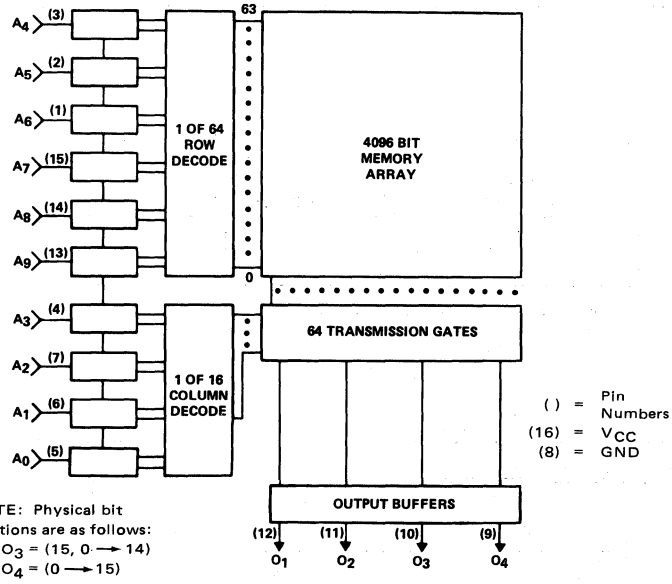
The HM-7644A is a fully decoded high speed Schottky TTL 4096-Bit Field Programmable ROM in a 1K word by 4 bit/word format with active pull-up outputs. This PROM is available in a 16 pin DIP (ceramic or epoxy) and a 16 pin flatpack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

Nichrome fuse technology is used on this and all other Harris Bipolar PROMs.

The HM-7644A contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

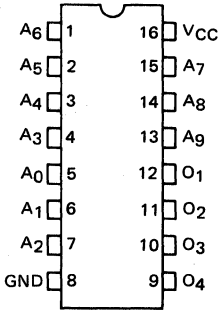
Functional Diagram



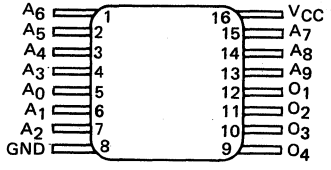
NOTE: Physical bit positions are as follows:
O_1, O_3 = (15, 0 → 14)
O_2, O_4 = (0 → 15)

Pinouts

TOP VIEW – DIP



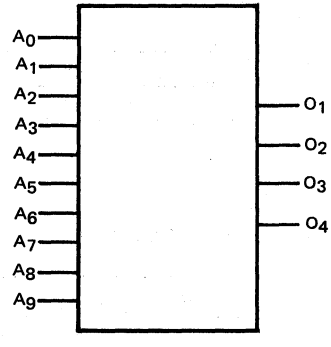
TOP VIEW – FLATPACK



PIN NAMES

A_0–A_9	Address Inputs
O_1–O_4	Outputs

Logic Symbol



ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7644A-5 (V_{CC} = 5.0V ± 5%, T_A = 0°C to +75°C)
HM-7644A-2 (V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH}	Address Input "1"	–	–	+40	μA	V_{IH} = V_{CC} Max.
I_{IL}	Current "0"	–	-50.0	-250	μA	V_{IL} = 0.45V
V_{IH}	Input Threshold "1"	2.0	1.5	–	V	V_{CC} = V_{CC} Min.
V_{IL}	Voltage "0"	–	1.5	0.8	V	V_{CC} = V_{CC} Max.
V_{OH}	Output "1"	2.4	3.2	–	V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min.
V_{OL}	Voltage "0"	–	0.35	0.45	V	I_{OL} = +16mA, V_{CC} = V_{CC} Min.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15	–	-100	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	100	140	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

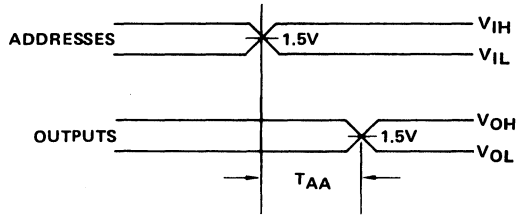
		HM-7644A-5 5V ± 5% 0°C to +75°C			HM-7644A-2 5V ± 10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	–	35	50	–	–	60	ns

A.C. limits guaranteed for worst case N^2 sequencing.

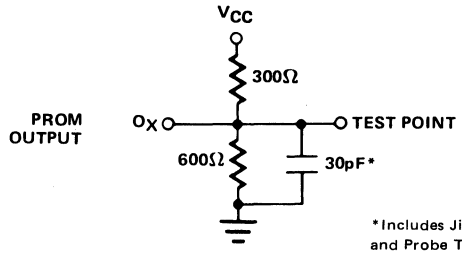
CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS



A.C. TEST LOAD



HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-7645

1K x 4 PROM

"Three State" Outputs

MARCH 1978 *Preview*

Features

- 50ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OUTPUTS AND FOUR CHIP ENABLE INPUTS
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME – GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD.
- 2142 PINOUT

Description

The HM-7645 is a fully decoded high speed Schottky TTL 4096 Bit Field Programmable PROM in a 1K word by 4 bit/word format with "Three State" outputs. This PROM is available in a 20 pin DIP (ceramic or epoxy) and a 20 pin flat pack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

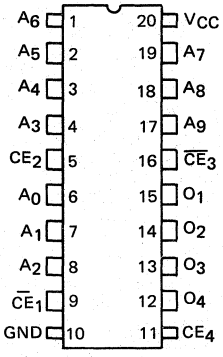
Nichrome fuse technology is used on this and all other Harris Bipolar PROMs.

The HM-7645 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

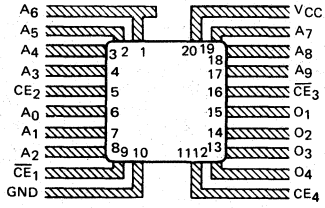
There are four chip enable inputs on the HM-7645. $\overline{CE}_1$, $\overline{CE}_3$ low and CE_2, CE_4 high enables the chip.

Pinout

TOP VIEW—DIP



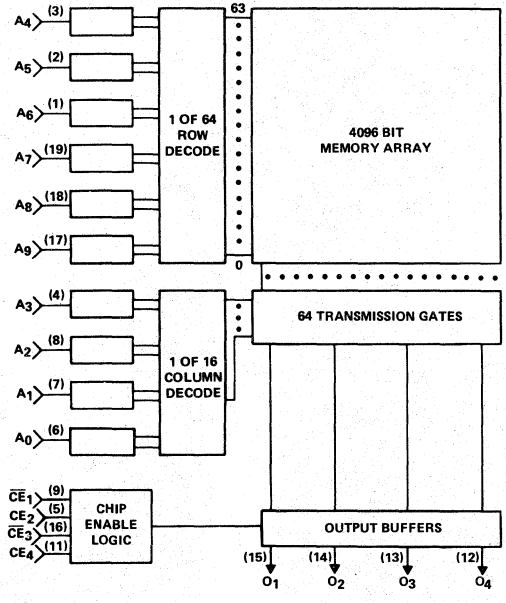
TOP VIEW—FLAT PACK



PIN NAMES

A_0 - A_9	ADDRESS INPUTS
O_1 - O_4	DATA OUTPUTS
$\overline{CE}_1$, $\overline{CE}_3$	CHIP ENABLE INPUTS
CE_2, CE_4	

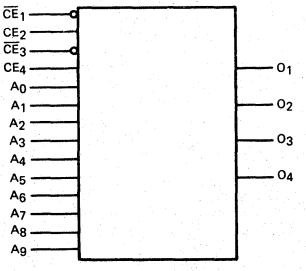
Functional Diagram



NOTE: Physical bit positions for columns are as follows:
O_1, O_3 = (15, 0 → 14)
O_2, O_4 = (0 → 15)

( ) = Pin Numbers
(20) = V_{CC}
(10) = GND

Logic Symbol



ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7645-5 (V_{CC} = 5.0V ± 5%, T_A = 0°C to +75°C)
HM-7645-2 (V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)
Typical Measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	– –	– -50.0	+40 -250	µA µA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	1.5 1.5	– 0.8	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4 –	3.2 0.35	– 0.50	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40 -40	µA µA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15	–	-100	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	100	140	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

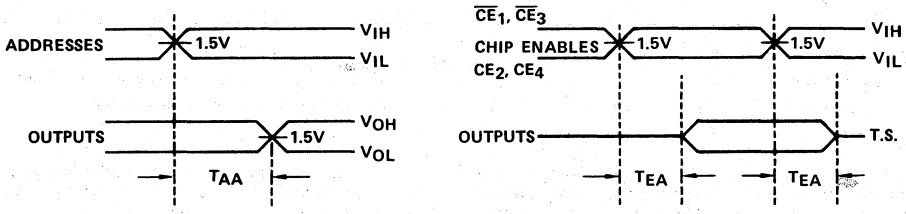
		HM-7645-5 5V ±5% 0°C to +75°C			HM-7645-2 5V ±10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	–	35	50	–	–	70	ns
T_{EA}	Chip Enable Access Time	–	25	30	–	–	40	ns

A.C. limits guaranteed for worst case N^2 sequencing.

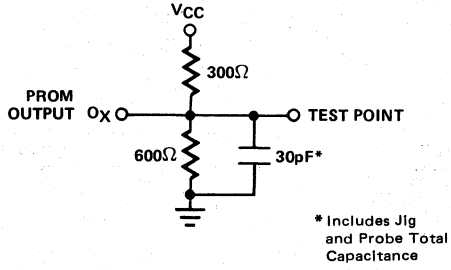
CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS



A.C. TEST LOAD



2

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-7645P

1K x 4 PROM

"Three State" Outputs

MARCH 1978 ***Preview***

Features

- 50ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OUTPUTS AND FOUR POWER DOWN INPUTS
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE - ONE PULSE/BIT ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY
- FAST ACCESS TIME - FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES
- INDUSTRY'S HIGHEST PROGRAMMING YIELD
- 2142 PINOUT

Description

The HM-7645P is a fully decoded high speed Schottky TTL 4096-Bit Field Programmable ROM in a 1K by 4 bit/word format with "Three State" outputs. This PROM is available in a 20 pin DIP (ceramic or epoxy) and a 20 pin flatpack.

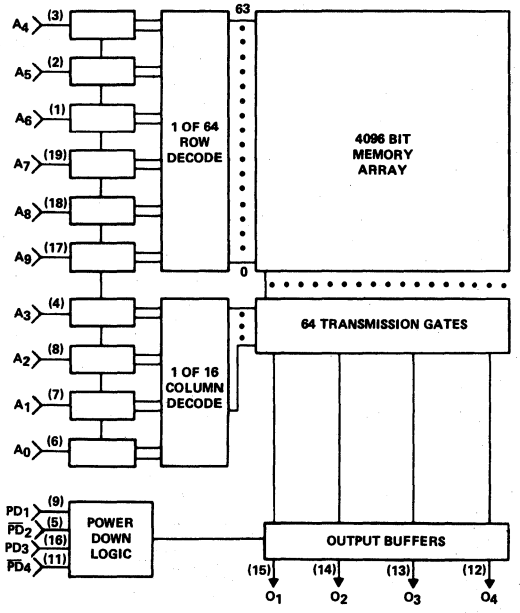
All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

Nichrome fuse technology is used on these and all other Harris Bipolar PROM's.

The HM-7645P contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

There are four power down inputs on the HM-7645P which are similar to chip enables. The chip is enabled or disabled using the power down inputs where a disabled chip dissipates 30% of nominal power and the outputs go to a high impedance state. The chip is powered up (enabled) when PD_1, PD_3 are low, and $\overline{PD}_2$, $\overline{PD}_4$ are high.

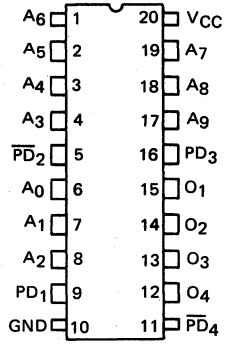
Functional Diagram



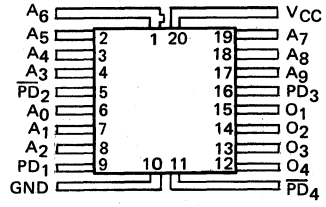
NOTE: Physical bit positions for columns are as follows:
O_1, O_3 = (15, 0 → 14)
O_2, O_4 = (0 → 15)

Pinouts

TOP VIEW - DIP



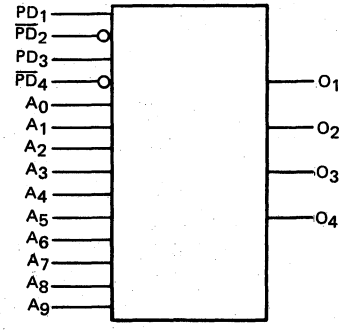
TOP VIEW - FLATPACK



PIN NAMES

A_0-A_9	Address Inputs
O_1-O_4	Data Outputs
PD_1, $\overline{PD}_2$, PD_3, $\overline{PD}_4$	Power Down Inputs

Logic Diagram



2

ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7645P-5 (V_{CC} = 5.0V ± 5%, T_A = 0°C to +75°C)
HM-7645P-2 (V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH}	Address/Enable "1"	–	–	+40	µA	V_{IH} = V_{CC} Max.
I_{IL}	Input Current "0"	–	-50.0	-250	µA	V_{IL} = 0.45V
V_{IH}	Input Threshold "1"	2.0	1.5	–	V	V_{CC} = V_{CC} Min.
V_{IL}	Voltage "0"	–	1.5	0.8	V	V_{CC} = V_{CC} Max.
V_{OH}	Output "1"	2.4	3.2	–	V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min.
V_{OL}	Voltage "0"	–	0.35	0.50	V	I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE}	Output Disable "1"	–	–	+40	µA	V_{OH}, V_{CC} = V_{CC} Max.
I_{OLE}	Current "0"	–	–	-40	µA	V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15	–	-100	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	100	140	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

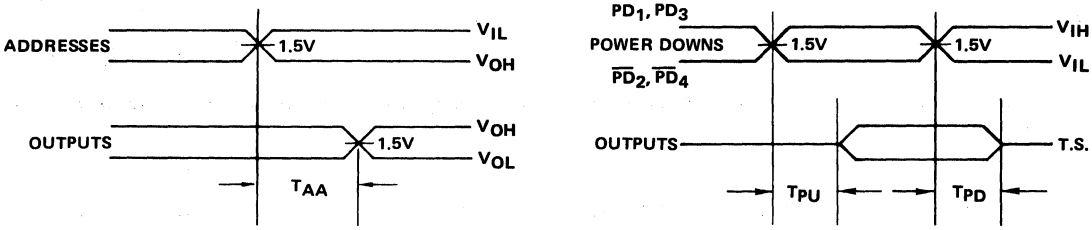
		HM-7645P-5 5V ± 5% 0°C to +75°C			HM-7645P-2 5V ± 10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	-	35	50	-	-	70	ns
T_{PD}	Chip Power-Down Access Time	-	25	30	-	-	40	ns
T_{PU}	Chip Power-Up Access Time	-	80	100	-	-	150	s

A.C. limits guaranteed for worst case N^2 sequencing.

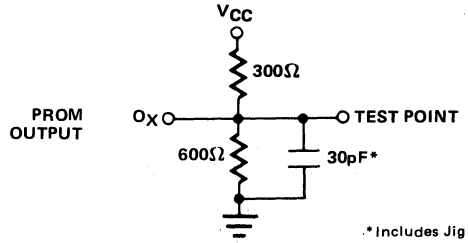
CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
CINA, CINCE	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
COUT	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS



A.C. TEST LOAD



*Includes Jig and Probe Total Capacitance

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-7647R

512 x 8 PROM

DECEMBER 1977

Features

- 60ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OUTPUTS WITH TWO CHIP ENABLE INPUTS
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE – ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME – GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD
- PIN COMPATIBLE WITH THE 82S115
- LATCHED OUTPUTS
- INPUT LOADING IS – 100 μA MAXIMUM

Description

The HM-7647R is a fully decoded high speed Schottlky TTL 4096-Bit Field Programmable ROM in a 512 word by 8 bit/word format and is available in a 24 pin D.I.P. (ceramic or epoxy) and a 24 pin flatpack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any position. The HM-7647R has "Three State" outputs.

Nichrome fuse technology is used on this and all other Harris Bipolar PROMs.

The pinout is identical to the 82S115 PROM.

The HM-7647R contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

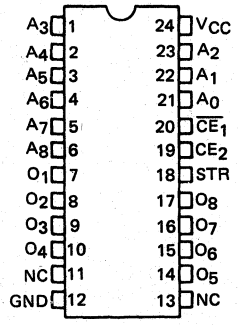
There are two chip enable inputs on the HM-7647R. $\overline{CE}_1$ low and CE_2 high enables the chip.

HM-7647R is operated in the Transparent Read Mode by holding the strobe input high throughout the read operation. This is the normal read mode where the two chip enable inputs will control the outputs.

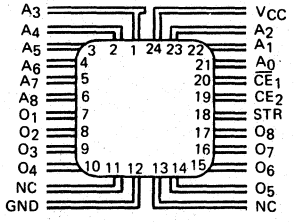
In Latched Read Mode, bringing the strobe input low will latch the outputs and chip enable inputs. If the device is disabled when the strobe input goes low the outputs will be latched in the high impedance state. If the device is in the latched mode the strobe input must be brought high to allow the outputs to respond to new address or chip enable conditions.

Pinout

TOP VIEW – D.I.P.



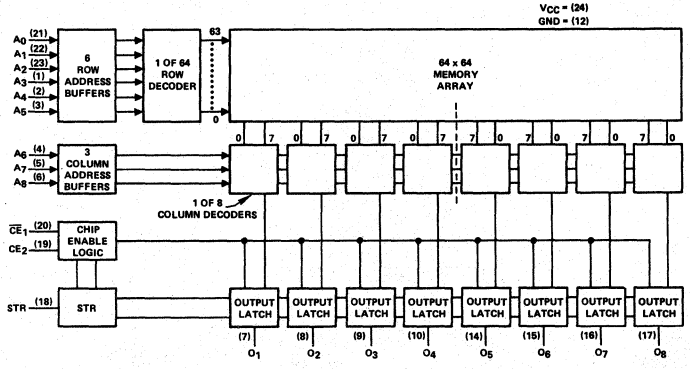
TOP VIEW – FLATPACK



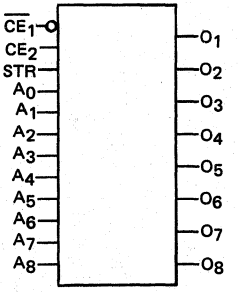
PIN NAMES

$A_0 - A_8$	Address Inputs
$O_1 - O_8$	Data Outputs
$\overline{CE}_1 - CE_2$	Chip Enable Inputs
STR	Latch Input

Functional Diagram



Logic Symbol



ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7647R-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7647R-2 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125° C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	– –	– -50	+25 -100(1)	µA µA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0" "0"	2.0 –	1.5 1.5	– 0.85	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" "1" Voltage "0" "0"	2.7(2) –	3.3 0.35	– 0.50	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0" "0"	– –	– –	+40 -40	µA µA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output S.C. Current	-20	–	-70	mA	V_{OUT} = 0.0V One Output Only for a Max. of 1 Second
I_{CC}	Power Supply Current	–	135	185	mA	V_{CC} = V_{CC} Max. All Inputs Grounded

*Positive current defined as into device terminals.

NOTE(1): I_{IL} = -150 µA for -2

NOTE(2): V_{OH} = 2.4V for -2

A.C. ELECTRICAL CHARACTERISTICS (Operating)

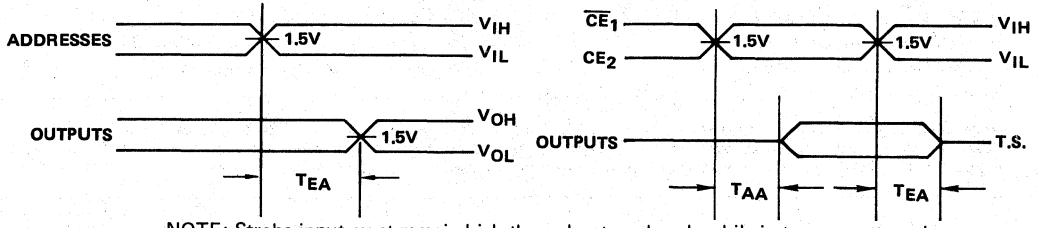
		HM-7647R-5 5V ± 5% 0°C to +75°C			HM-7647R-2 5V ± 10% -55°C to +125°C				
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS	TEST CONDIT.
T_{AA} T_{EA}	Address Access Time Chip Enable Access Time	– –	40 30	60 40	– –	50 40	80 50	ns ns	 Transparent
T_{ADH}	Address Hold Time	0	-10	–	0	-10	–	ns	Latched
T_{CDH}	Chip Enable Hold Time	10	0	–	10	0	–	ns	
T_{SW}	Strobe Pulse Width	30	15	–	40	15	–	ns	
T_{SL}	Strobe Latch Time	60	35	–	80	45	–	ns	
T_{DL}	Strobe Delatch Time	–	–	40	–	–	50	ns	
T_{CDS}	Chip Enable Set-Up Time	40	–	–	50	–	–	ns	

A.C. limits guaranteed for worst case N^2 sequencing.

CAPACITANCE: T_A = 25°C

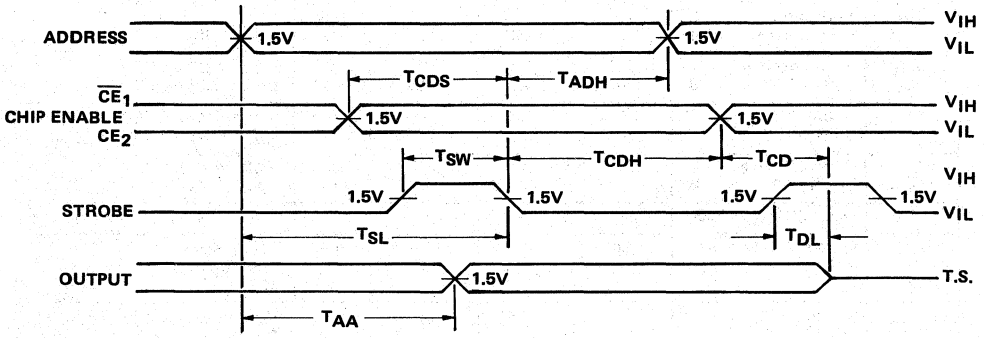
SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS (TRANSPARENT MODE)

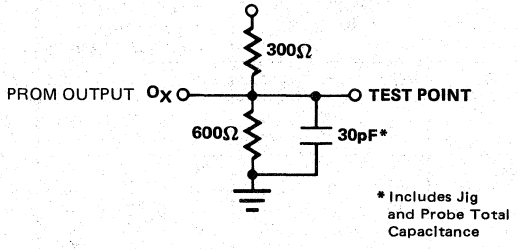


NOTE: Strobe input must remain high throughout read cycle while in transparent mode.

SWITCHING TIME DEFINITIONS (LATCHED MODE)



A.C. TEST LOAD



HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-7648/49

512 x 8 PROM

HM-7648 - Open Collector Outputs
HM-7649 - "Three State" Outputs

APRIL 1978

Features

- 60ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND A CHIP ENABLE INPUT
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE - ONE PULSE/BIT ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME - GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD
- PIN COMPATIBLE WITH THE 74S472/73
- LOW INPUT LOADING

Description

The HM-7648/49 is a fully decoded high speed Schottky TTL 4096-Bit Field Programmable ROM in a 512 word by 8 bit/word format with open collector (HM-7648) or "Three State" (HM-7649) outputs. These PROMs are available in a 24 pin D.I.P. (ceramic or epoxy) and a 24 pin flat pack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

Nichrome fuse technology is used on this and all other Harris Bipolar PROMs.

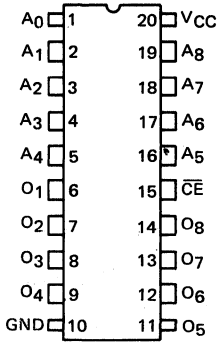
The pinout is identical to the 74S472/73 PROM.

The HM-7648/49 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametic and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

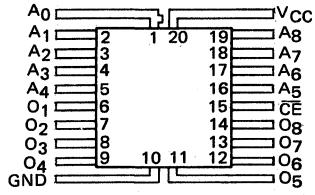
There is a chip enable input on the HM-7648/49 where $\overline{CE}$ low enables the device.

Pinouts

TOP VIEW - D.I.P.



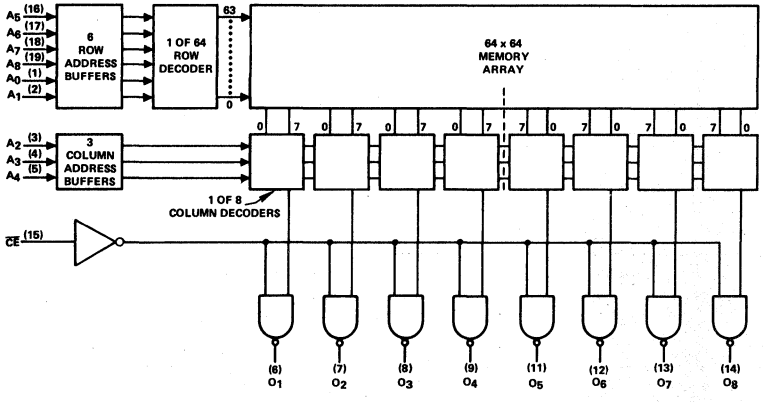
TOP VIEW - FLATPACK



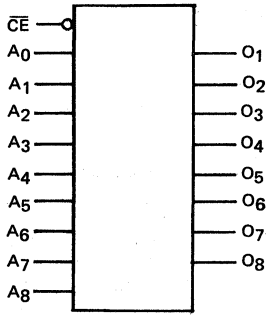
PIN NAMES

$A_0 - A_8$	Address Inputs
$O_1 - O_8$	Data Outputs
$\overline{CE}$	Chip Enable Input

Functional Diagram



Logic Symbol



ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7648/49-5 (V_{CC} = 5.0V ± 5%, T_A = 0°C to +75°C)
HM-7648/49-2 (V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	– –	– -50	+25 -250	µA µA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	1.5 1.5	– 0.80	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4 * –	3.2* 0.35	– 0.50	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+50 -50 *	µA µA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output S.C. Current	-20*	–	-100*	mA	V_{OUT} = 0.0V One Output Only for a Max. of 1 Second
I_{CC}	Power Supply Current	–	120	170	mA	V_{CC} = V_{CC} Max. All Inputs Grounded

* "Three State" only
NOTE: Positive current defined as into device terminals.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

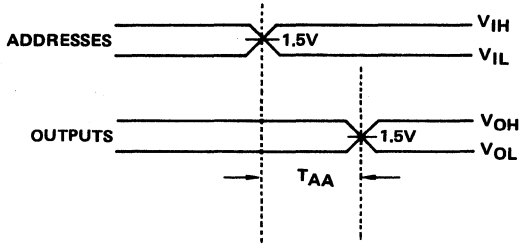
		HM-7648/49-5 5V ±5% 0°C to + 75°C			HM-7648/49-2 5V ±10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	–	55	60	–	50	80	ns
T_{EA}	Chip Enable Access Time	–	20	40	–	30	50	ns

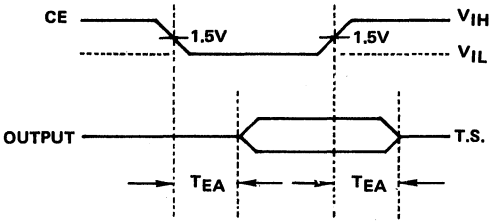
A.C. limits guaranteed for worst case N^2 sequencing.

CAPACITANCE: T_A = 25°C

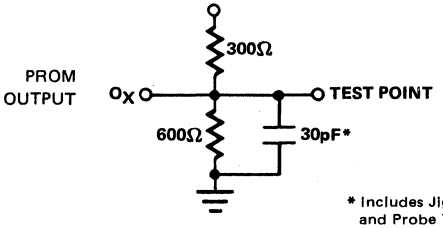
SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS





A.C. TEST LOAD



* Includes Jig and Probe Total Capacitance

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-7680/81

1K x 8 PROM

HM-7680 - Open Collector Outputs
HM-7681 - "Three State" Outputs

DECEMBER 1977 *Preliminary*

Features

- 60ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND FOUR CHIP ENABLE INPUTS
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME – GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD

Description

The HM-7680/81 is a fully decoded high speed Schottky TTL 8192/Bit Field Programmable ROM in a 1K word by 8 bit/word format with open collector (HM-7680) or "Three State" (HM-7681) outputs. These PROM's are available in a 24 pin D.I.P. (ceramic or epoxy) and a 24 pin flat pack.

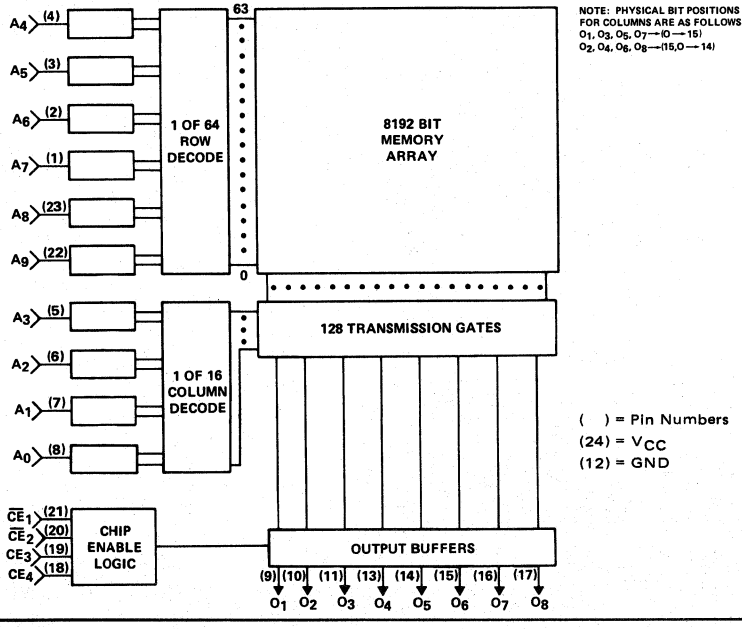
All bits are manufactured storing a logical "1" (Positive Logic) and can be selectively programmed for a logical "0" in any one bit position.

Nichrome fuse technology is used on this and all other Harris Bipolar PROMs.

The HM-7680/81 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

There are four chip enable inputs on the HM-7680/81. $\overline{CE}_1$, $\overline{CE}_2$ low, and CE_3, CE_4 high enables the chip.

Functional Diagram

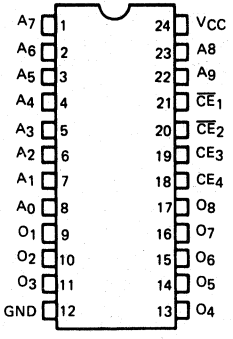


NOTE: PHYSICAL BIT POSITIONS FOR COLUMNS ARE AS FOLLOWS:
O_1, O_3, O_5, O_7 — (0 — 15)
O_2, O_4, O_6, O_8 — (15,0 — 14)

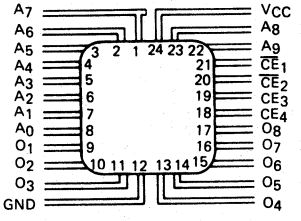
( ) = Pin Numbers
(24) = V_{CC}
(12) = GND

Pinouts

TOP VIEW—DIP



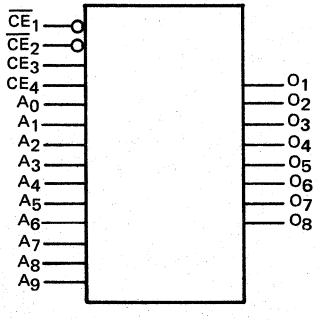
TOP VIEW – FLATPACK



PIN NAMES

$A_0 - A_9$	Address Inputs
$O_1 - O_8$	Data Outputs
$\overline{CE}_1$, $\overline{CE}_2$, CE_3, CE_4	Chip Enable Inputs

Logic Symbol



ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7680/81-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7680/81-2 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH}	Address/enable "1"	–	–	+40	µA	V_{IH} = V_{CC} Max.
I_{IL}	Input Current "0"	–	-50.0	-250	µA	V_{IL} = 0.45V
V_{IH}	Input Threshold "1"	2.0	1.5	–	V	V_{CC} = V_{CC} Min.
V_{IL}	Voltage "0"	–	1.5	0.8	V	V_{CC} = V_{CC} Max.
V_{OH}	Output "1"	2.4 *	3.2*	–	V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min.
V_{OL}	Voltage "0"	–	0.35	0.50	V	I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE}	Output Disable "1"	–	–	+40	µA	V_{OH}, V_{CC} = V_{CC} Max.
I_{OLE}	Current "0"	–	–	-40*	µA	V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output S.C. Current	-15*	–	-100*	mA	V_{OUT} = 0.0V One Output Only for a Max. of 1 Second
I_{CC}	Power Supply Current	–	130	170	mA	V_{CC} = V_{CC} Max. All Inputs Grounded

NOTE: Positive current defined as into device terminals.
* "Three State" only

A.C. ELECTRICAL CHARACTERISTICS (Operating)

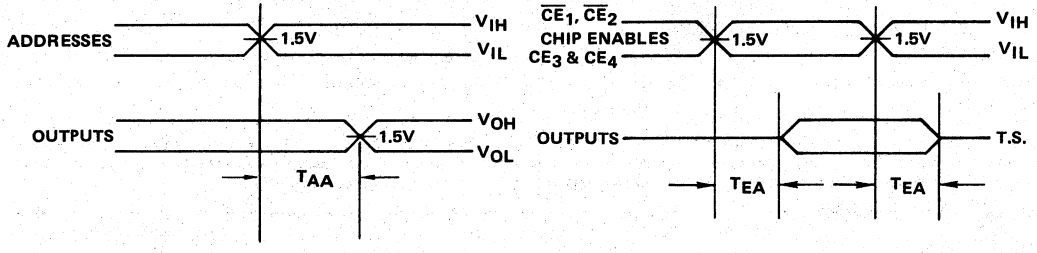
		HM-7680/81-5 5V ±5% 0°C to + 75°C			HM-7680/81-2 5V ±10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	–	45	60	–	–	80	ns
T_{EA}	Chip Enable Access Time	–	30	40	–	–	50	ns

A.C. limits guaranteed for worst case N^2 sequencing.

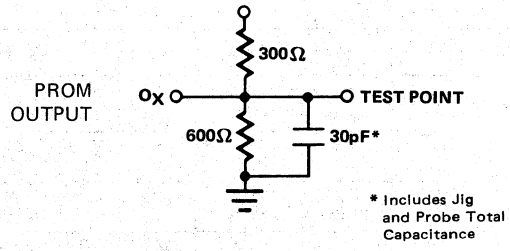
CAPACITANCE : T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS



A.C. TEST LOAD



HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-7680R/81R
1K x 8 PROM
HM-7680R - Open Collector Outputs
HM-7681R - "Three State" Outputs

DECEMBER 1977 **Preliminary**

Features

- 60ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND THREE CHIP ENABLE INPUTS
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE - ONE PULSE/BIT ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY
- FAST ACCESS TIME - GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURES AND VOLTAGE RANGES
- INDUSTRY'S HIGHEST PROGRAMMING YIELD
- LATCHED OUTPUTS

Description

The HM-7680R/81R is a fully decoded high speed Schottky TTL 8192-Bit Field Programmable ROM in a 1K word by 8 bit/word format with open collector (HM-7680R) or "Three State" (HM-7681R) outputs. These PROMs are available in a 24 pin D.I.P. (ceramic or epoxy) and a 24 pin flatpack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

Nichrome fuse technology is used on these and all other Harris Bipolar PROMs.

The HM-7680R/81R contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

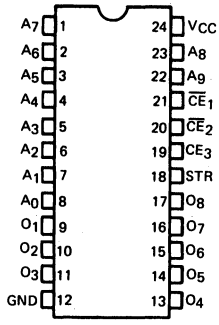
There are three chip enable inputs on the HM-7680R/81R. $\overline{CE}_1$, $\overline{CE}_2$ low and CE_3 high enables the chip.

The HM-7680R/81R is operated in the Transparent Read Mode by holding the strobe input high throughout the read operation. This is the normal read mode where the three chip enable inputs will control the outputs.

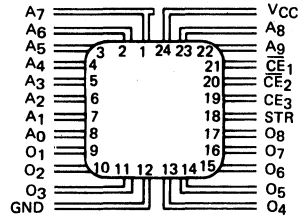
In Latched Read Mode, bringing the strobe input low will latch the outputs and chip enable inputs. If the device is disabled when the strobe input goes low, the outputs will be latched in the high impedance state. If the device is in the latched mode the strobe input must be brought high to allow the outputs to respond to new address or chip enable conditions.

Pinouts

TOP VIEW—DIP



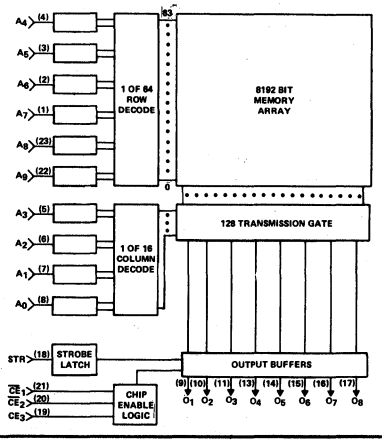
TOP VIEW – FLATPACK



PIN NAMES

A0 – A9	Address Inputs
O1 – O8	Data Outputs
$\overline{CE}_1$, $\overline{CE}_2$, CE_3	Chip Enable Inputs
STR	Strobe

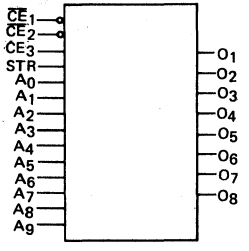
Functional Diagram



NOTE: Physical bit positions for columns are as follows:
$O_1, O_3, O_5, O_7 \rightarrow (0 \rightarrow 15)$
$O_2, O_4, O_6, O_8 \rightarrow (15, 0 \rightarrow 14)$

( ) = Pin Numbers
(24) = V_{CC}
(12) = GND

Logic Symbol



ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7680R/81R-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7680R/81R-2 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	– –	– -50.0	+40 -250	µA µA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	1.5 1.5	– 0.8	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4* –	3.2* 0.35	– 0.50	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40 -40*	µA µA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output S.C. Current	-15*	-2.5	-100*	mA	V_{OUT} = 0.0V One Output Only for a Max. of 1 Second
I_{CC}	Power Supply Current	–	130	170	mA	V_{CC} = V_{CC} Max. All Inputs Grounded

NOTE: Positive current defined as into device terminals.
*"Three State" only

A.C. ELECTRICAL CHARACTERISTICS (Operating)

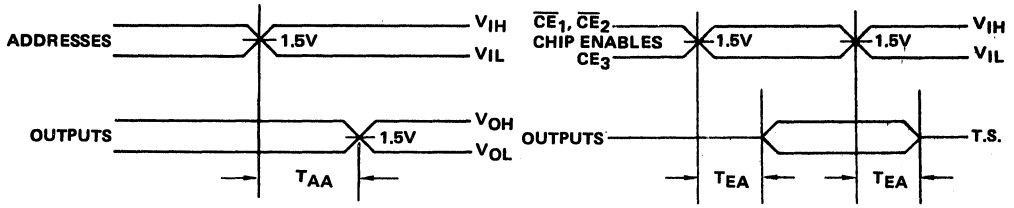
		HM-7680R/81R-5 5V ±5% 0°C to +75°C			HM-7680R/81R-2 5V ±10% -55°C to +125°C				
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS	TEST CONDIT.
T_{AA}	Address Access Time	–	45	60	–	–	80	ns	Latched or
T_{EA}	Chip Enable Access Time	–	30	40	–	–	50	ns	Transparent
T_{ADH}	Address Hold Time	0	-10	–	0	-10	–	ns	Latched Only
T_{CDH}	Chip Enable Hold Time	10	0	–	10	0	–	ns	
T_{SW}	Strobe Pulse Width	30	10	–	40	10	–	ns	
T_{SL}	Strobe Latch Time	60	40	–	80	40	–	ns	
T_{DL}	Strobe Delatch Time	–	–	40	–	–	50	ns	
T_{CDS}	Chip Enable Set-Up Time	40	–	–	50	–	–	ns	

A.C. limits guaranteed for worst case N^2 sequencing.

CAPACITANCE : T_A = 25°C

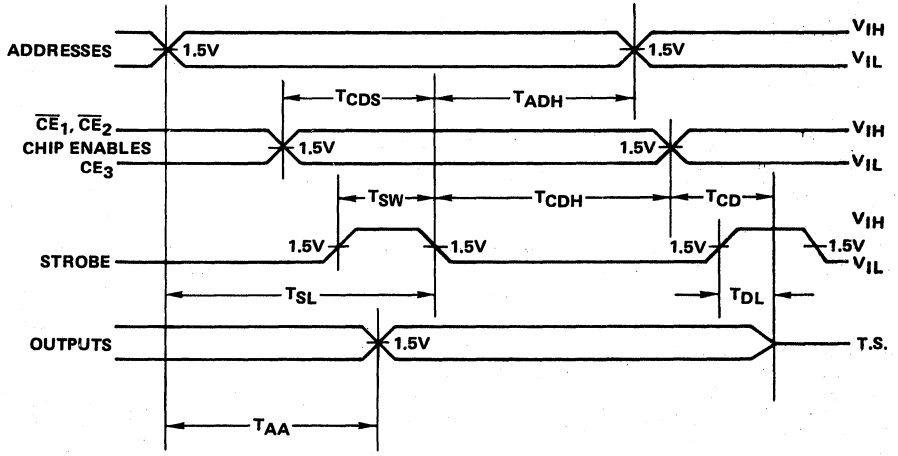
SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS (Transparent Mode)

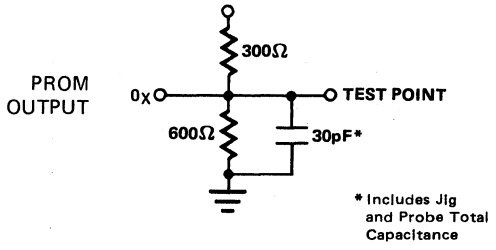


NOTE: Strobe input must remain high throughout read cycle while in transparent mode.

SWITCHING TIME DEFINITIONS (Latched Mode)



A.C. TEST LOAD



HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-7680P/81P

1K x 8 PROM

HM-7680P - Open Collector Outputs
HM-7681P - "Three State" Outputs

APRIL 1978 *Preview*

Features

- 60ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND FOUR POWER DOWN INPUTS.
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE – ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME – FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD.

Description

The HM-7680P/81P is a fully decoded high speed Schottky TTL 8192-Bit Field Programmable ROM in a 1K word by 8 bit/word format with open collector (HM-7680P) or "three-state" (HM-7681P) outputs. These PROM's are available in a 24 pin D.I.P. (ceramic or epoxy) and a 24 pin flatpack.

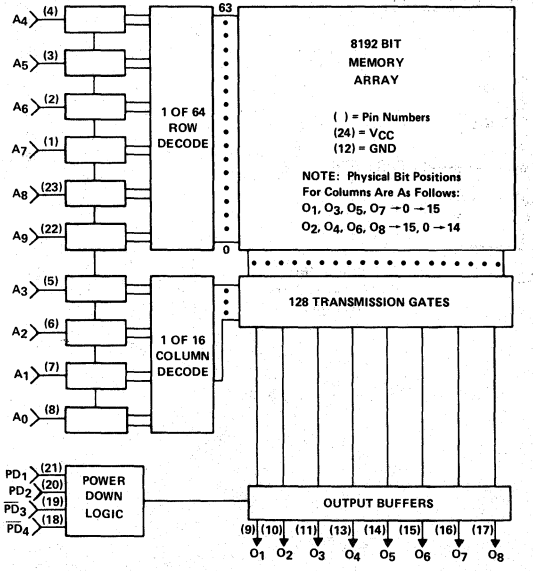
All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

Nichrome fuse technology is used on these and all other Harris Bipolar PROM's.

The HM-7680P/81P contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

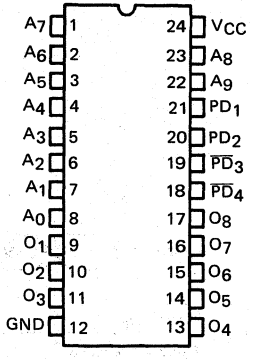
There are four power down inputs on the HM-7680P/81P which are similar to chip enables. The chip is enabled or disabled using the power down inputs where a disabled chip dissipates 30% of nominal power and the outputs go to a high impedance state. The chip is powered up (enabled) when PD_1 and PD_2 are low and $\overline{PD}_3$ and $\overline{PD}_4$ are high.

Functional Diagram

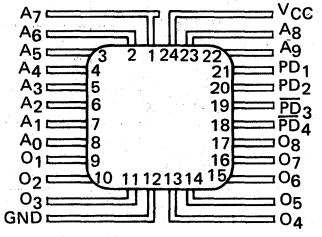


Pinouts

TOP VIEW - DIP



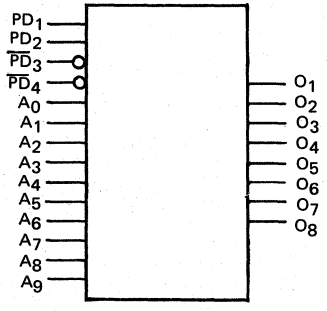
TOP VIEW - FLATPACK



PIN NAMES

$A_0 - A_9$	Address Inputs
$O_1 - O_8$	Address Outputs
$PD_1, PD_2, \overline{PD}_3, \overline{PD}_4$	Power Down Inputs

Logic Symbol



ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7680P/81P-5 (V_{CC} = 5.0V ± 5%, T_A = 0°C to +75°C)
HM-7680P/81P-2 (V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH}	Address/Enable "1"	–	–	+40	μA	V_{IH} = V_{CC} Max.
I_{IL}	Input Current "0"	–	-50.0	-250	μA	V_{IL} = 0.45V
V_{IH}	Input Threshold "1"	2.0	1.5	–	V	V_{CC} = V_{CC} Min.
V_{IL}	Voltage "0"	–	1.5	0.8	V	V_{CC} = V_{CC} Max.
V_{OH}	Output "1"	2.4*	3.2*	–	V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min.
V_{OL}	Voltage "0"	–	0.35	0.50	V	I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE}	Output Disable "1"	–	–	+40	μA	V_{OH}, V_{CC} = V_{CC} Max.
I_{OLE}	Current "0"	–	–	-40*	μA	V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15*	–	-100*	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	130	170	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.
*"Three State" only

A.C. ELECTRICAL CHARACTERISTICS (Operating)

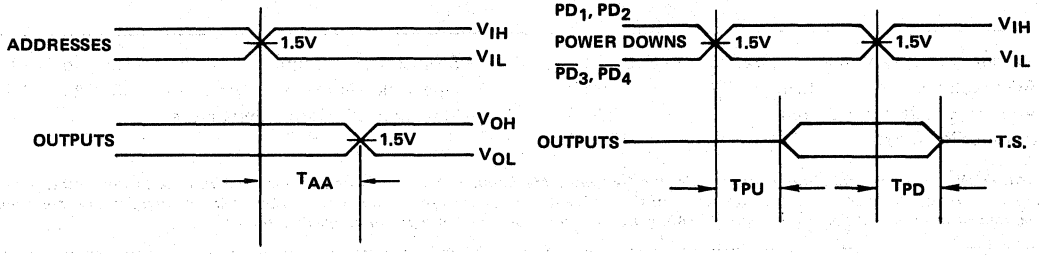
		HM-7680P/81P-5 5V ± 5% 0°C to +75°C			HM-7680P/81P-2 5V ± 10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	-	45	60	-	-	80	ns
T_{PD}	Chip Power-Down Access Time	-	30	40	-	-	50	ns
T_{PU}	Chip Power-Up Access Time	-	80	100	-	-	150	ns

A.C. limits guaranteed for worst case N^2 sequencing.

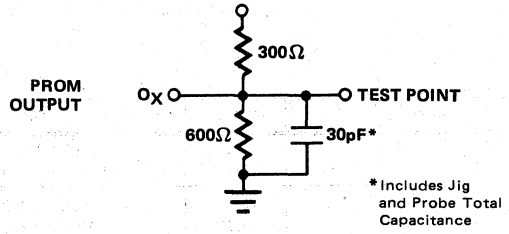
CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS



A.C. TEST LOAD



HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-7680RP/81RP

1K x 8 PROM

HM-7680RP - Open Collector Outputs
HM-7681RP - "Three State" Outputs

APRIL 1978 **Preview**

Features

- 60ns MAXIMUM ADDRESS ACCESS TIME.
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND TWO CHIP ENABLE INPUTS.
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE - ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME - GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD.
- LATCHED OUTPUTS.
- A POWER DOWN INPUT ALLOWING 70% REDUCTION IN NOMINAL POWER DISSIPATION.

Description

The HM-7680RP/81RP are fully decoded high speed Schottky TTL 8192-Bit Field Programmable ROMs in a 1K words by 8 bit/word format with open collector (HM-7680RP) or "Three State" (HM-7681RP) outputs. These PROMs are available in a 24 pin DIP (ceramic or epoxy) and a 24 pin flatpack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

Nichrome fuse technology is used on these and all other Harris Bipolar PROMs.

The HM-7680RP/81RP contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

There are two chip enable inputs on the HM-7680RP/81RP. $\overline{CE}_1$ and $\overline{CE}_2$ low enables the device.

There is also a power down input on this device. A powered down device has 70% reduction in nominal power dissipation if the outputs are not latched and 50% reduction in nominal power if the outputs are latched.

The HM-7680RP/81RP is operated in the Transparent Read Mode by holding the the strobe input high and the $\overline{PD}$ input high throughout the read operation. This is the normal read mode where the two chip enables and the power down inputs will control the outputs.

In Latched Read Mode, bringing the strobe input low will latch the outputs and the chip enable inputs. However, the power down input is independent of the latch function and can be changed while in the latched mode. If the device is disabled when the strobe input goes low, the outputs will be latched in the high impedance state. If the device is in the latched mode, the strobe input must be brought high to allow the outputs to respond to new address or chip enable conditions.

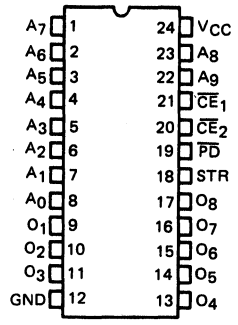
The following is a summary of the functional dependencies of the operating modes:

1. Chip enabled, transparent, powered up - normal mode where the power down input is effectively a chip enable with the I_{CC} reduction function.
2. Chip enabled, latched, power up - this is normal latched mode where the outputs remain latched regardless of address and chip enable switching.
3. Chip enabled, latched, power down - this is the powered down latched mode where the output data remains latched while power is reduced to 50% of its nominal value. If the latch strobe changes state while in this mode, the outputs will go to a high impedance state and power will reduce to 30% of nominal power. This is because the $\overline{PD}$ input becomes an effective chip enable in the Transparent Mode.
4. Chip disabled, transparent, power down - this is the normal powered down mode where the outputs are in a high impedance state and the power is reduced to 30% of the nominal power.

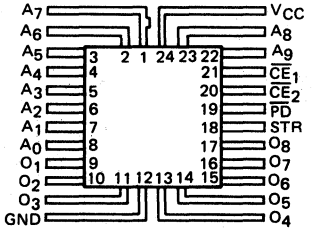
On the following page is a table to clarify the operational interdependencies.

Pinouts

TOP VIEW—DIP



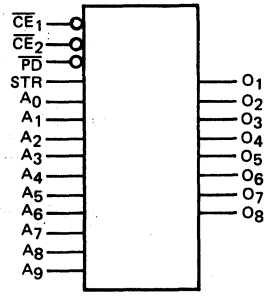
TOP VIEW—FLATPACK



PIN NAMES

A_0-A_9	Address Inputs
O_1-O_8	Data Outputs
$\overline{CE}_1$, $\overline{CE}_2$	Chip Enable Inputs
$\overline{PD}$	Power Down Input
STR	Strobe Input

Logic Symbol

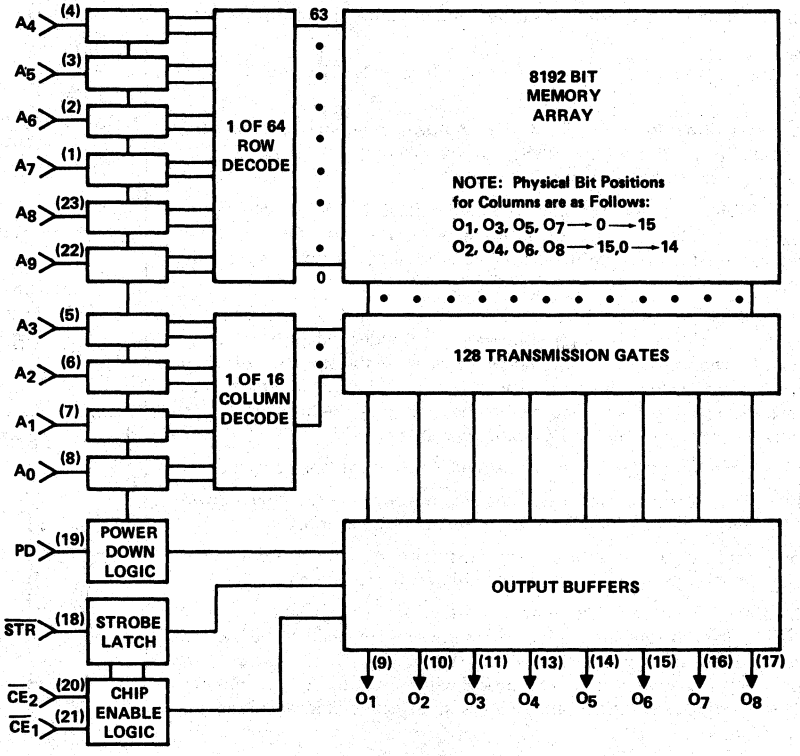


TRUTH TABLE for HM-7680RP/81RP

$\overline{PD}$	STR	$\overline{CE}_2$	$\overline{CE}_1$	OUTPUTS	POWER
0	0	0	0	Latched Data	50%
0	0	0	1	Latched "Three State"	50%
0	0	1	0	Latched "Three State"	50%
0	0	1	1	Latched "Three State"	50%
0	1	0	0	Unlatched "Three State"	30%
0	1	0	1	Unlatched "Three State"	30%
0	1	1	0	Unlatched "Three State"	30%
0	1	1	1	Unlatched "Three State"	30%
1	0	0	0	Latched Data	100%
1	0	0	1	Latched "Three State"	100%
1	0	1	0	Latched "Three State"	100%
1	0	1	1	Latched "Three State"	100%
1	1	0	0	Unlatched Data	100%
1	1	0	1	Unlatched "Three State"	100%
1	1	1	0	Unlatched "Three State"	100%
1	1	1	1	Unlatched "Three State"	100%

Assume that the sequence of transitions is: 1) Chip Enables, 2) STR, 3) $\overline{PD}$ and the initial state is Unlatched Data.

Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7680RP/81RP-5 (V_{CC} = 5.0V ± 5%, T_A = 0°C to +75°C)
HM-7680RP/81RP-2 (V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	– –	– -50.0	+40 -250	µA µA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	1.5 1.5	– 0.8	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4* –	3.2* 0.35	– 0.50	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40 -40*	µA µA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15*	-2.5	-100*	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	120	170	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.
*"Three State" only

A.C. ELECTRICAL CHARACTERISTICS (Operating)

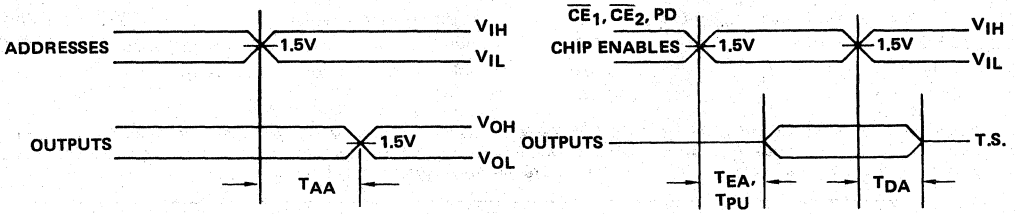
		HM-7680RP/81RP-5 5V ± 5% 0°C to +75°C			HM-7680RP/81RP-2 5V ± 10% -55°C to +125°C				
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS	TEST COND.
T_{AA}	Address Access Time	–	45	60	–	–	80	ns	Latched or
T_{DA}	Chip Disable Access Time	–	30	40	–	–	50	ns	Transparent
T_{EA}	Chip Enable Access Time	–	30	40	–	–	50	ns	
T_{PU}	Chip Power-Up Access Time	–	80	100	–	–	150	ns	
T_{ADH}	Address Hold Time	0	-10	–	0	-10	–	ns	Latched Only
T_{CDH}	Chip Enable Hold Time	10	0	–	10	0	–	ns	
T_{SW}	Strobe Pulse Width	30	10	–	40	10	–	ns	
T_{SL}	Strobe Latch Time	60	40	–	80	40	–	ns	
T_{DL}	Strobe Delatch Time	–	–	40	–	–	50	ns	
T_{CDS}	Chip Enable Set-Up Time	40	–	–	50	–	–	ns	

A.C. limits guaranteed for worst case N^2 sequencing.

CAPACITANCE: T_A = 25°C

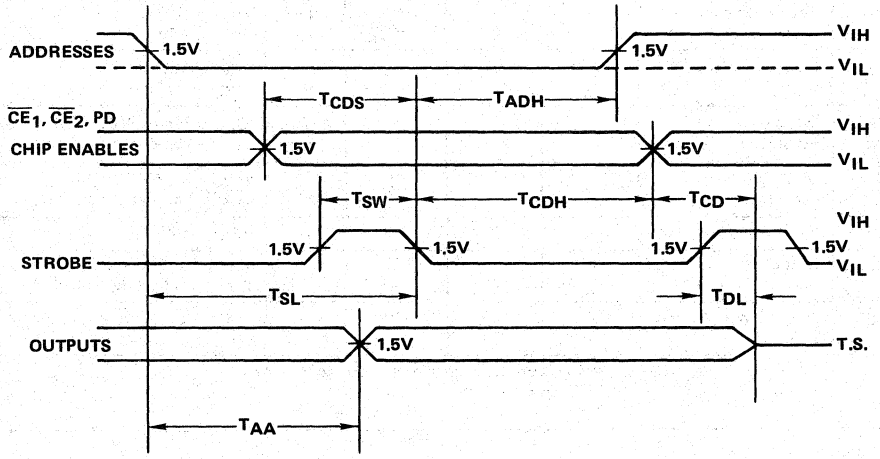
SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
CINA, CINCE	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
COUT	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS (Transparent Mode)

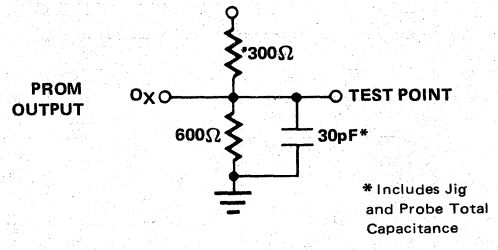


NOTE: Strobe input must remain high throughout read cycle while in transparent mode.

SWITCHING TIME DEFINITIONS (Latched Mode)



A.C. TEST LOAD



HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-7683

1K x 8 PROM

Active Pull-up Outputs

MARCH 1978 **Preliminary**

Features

- 60ns MAXIMUM ADDRESS ACCESS TIME
- SIMPLE, HIGH SPEED PROGRAMMING PROCEDURE - ONE PULSE/BIT ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME - GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD
- LOW PIN COUNT FOR MAXIMUM DENSITY

Description

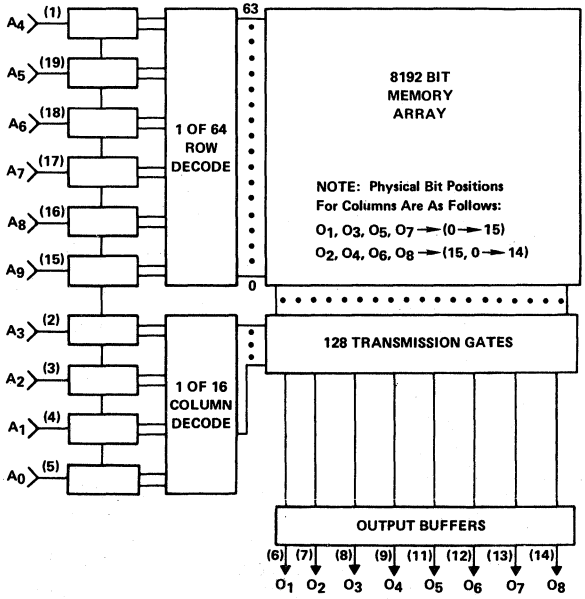
The HM-7683 is a fully decoded high speed Schottky TTL 8192-Bit Field Programmable ROM in a 1K word by 8 bit/word format and is available in a 20 pin DIP (ceramic or epoxy) and a 20 pin flatpack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

Nichrome fuse technology is used on this and all other Harris Bipolar PROMs.

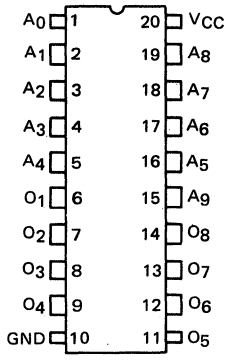
The HM-7683 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parameterics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

Functional Diagram

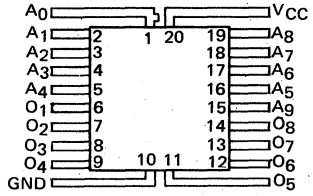


Pinouts

TOP VIEW - DIP



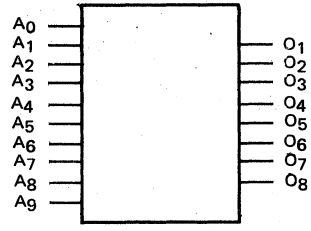
TOP VIEW - FLATPACK



PIN NAMES

$A_0 - A_9$	Address Outputs
$O_1 - O_8$	Data Outputs

Logic Symbol



2

ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7683-5 (V_{CC} = 5.0V ± 5%, T_A = 0° to +75°C)
HM-7683-2 (V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)
Typical Measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH}	Address Input "1"	–	–	+40	µA	V_{IH} = V_{CC} Max.
I_{IL}	Current "0"	–	-50.0	-250	µA	V_{IL} = 0.45V
V_{IH}	Input Threshold "1"	2.0	1.5	–	V	V_{CC} = V_{CC} Min.
V_{IL}	Voltage "0"	–	1.5	0.8	V	V_{CC} = V_{CC} Max.
V_{OH}	Output "1"	2.4	3.2	–	V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min.
V_{OL}	Voltage "0"	–	0.35	0.50	V	I_{OL} = +16mA, V_{CC} = V_{CC} Min.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15	–	-100	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	130	170	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

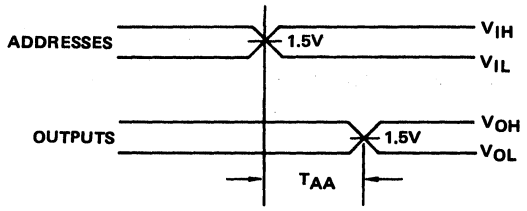
		HM-7683-5 5V ± 5% 0°C to +75°C			HM-7683-2 5V ± 10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	–	45	60	–	–	80	ns

A.C. limits guaranteed for worst case N^2 sequencing.

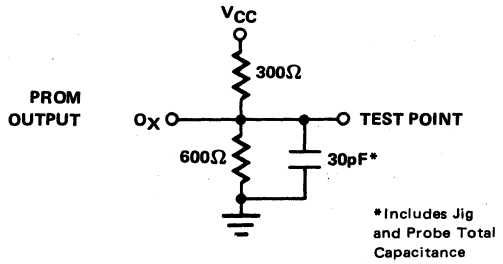
CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS



A.C. TEST LOAD



2

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-7684/85

2K x 4 PROM

HM-7684 - Open Collector Outputs
HM-7685 - "Three State" Outputs

MARCH 1978 **Preliminary**

Features

- 60ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND A CHIP ENABLE INPUT
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE - ONE PULSE/BIT ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY
- FAST ACCESS TIME - GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES
- INDUSTRY'S HIGHEST PROGRAMMING YIELD

Description

The HM-7684/85 are a fully decoded high speed Schottky TTL 8192-Bit Field Programmable ROM in a 2K word by a 4 bit/word format with open collector (HM-7684) or "Three State" (HM-7685) outputs. These PROMs are available in an 18 pin DIP (ceramic or epoxy) and an 18 pin flatpack.

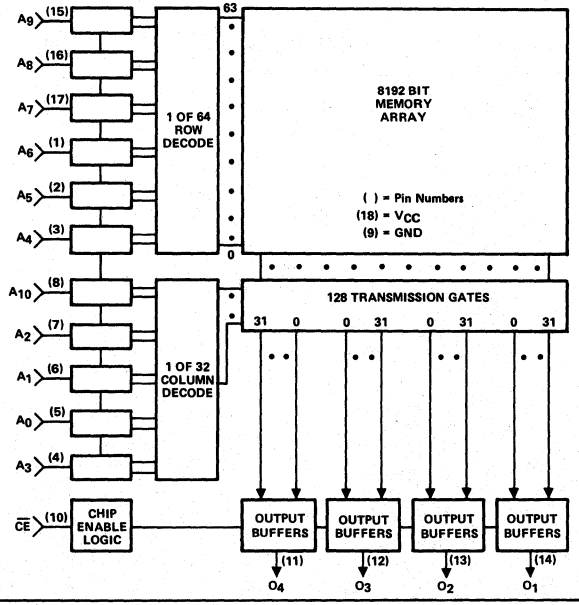
All bits are manufactured storing a logical "1"(positive logic) and can be selectively programmed for a logical "0" in any bit position.

Nichrome fuse technology is used on this and all other Harris Bipolar PROMs.

The HM-7684/85 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

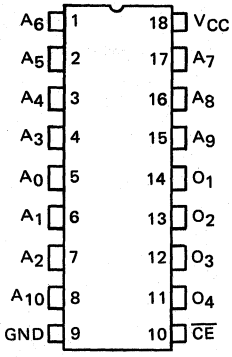
There is a chip enable on the HM-7684/85. $\overline{CE}$ low enables the chip.

Functional Diagram

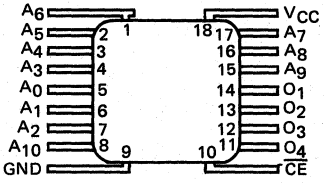


Pinouts

TOP VIEW - DIP



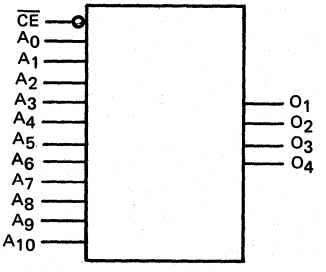
TOP VIEW - FLATPACK



PIN NAMES

$A_0 - A_{10}$	Address Inputs
$O_1 - O_4$	Data Outputs
$\overline{CE}$	Chip Enable Input

Logic Symbol



2

ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7684/85-5 (V_{CC} = 5.0V ± 5%, T_A = 0°C to +75°C)
HM-7684/85-2 (V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH}	Address/Enable "1"	–	–	+40	μA	V_{IH} = V_{CC} Max.
I_{IL}	Input Current "0"	–	-50.0	-250	μA	V_{IL} = 0.45V
V_{IH}	Input Threshold "1"	2.0	1.5	–	V	V_{CC} = V_{CC} Min.
V_{IL}	Voltage "0"	–	1.5	0.8	V	V_{CC} = V_{CC} Max.
V_{OH}	Output "1"	2.4*	3.2*	–	V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min.
V_{OL}	Voltage "0"	–	0.35	0.50	V	I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE}	Output Disable "1"	–	–	+40	μA	V_{OH}, V_{CC} = V_{CC} Max.
I_{OLE}	Current "0"	–	–	-40*	μA	V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15*	–	-100*	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	120	170	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.
*"Three State" only

A.C. ELECTRICAL CHARACTERISTICS (Operating)

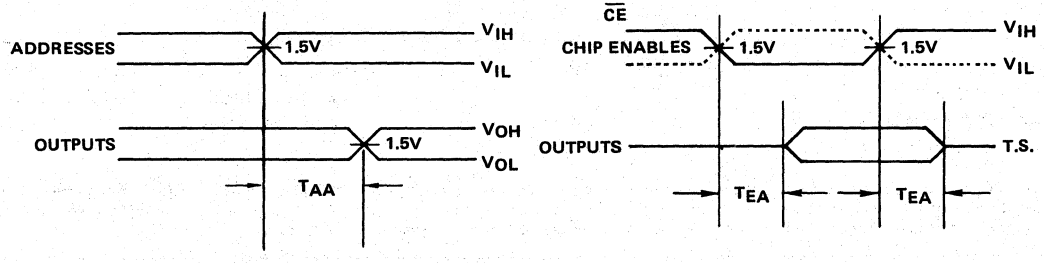
		HM-7684/85-5 5V ± 5% 0°C to +75°C			HM-7684/85-2 5V ± 10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	–	45	60	–	–	80	ns
T_{EA}	Chip Enable Access Time	–	30	40	–	–	50	ns

A.C. limits guaranteed for worst case N^2 sequencing.

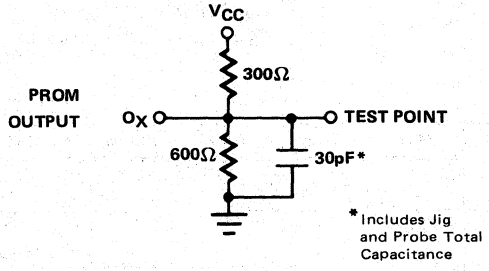
CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS



A.C. TEST LOAD



2

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-7684P/85P

2K x 4 PROM

HM-7684P - Open Collector Outputs
HM-7685P - "Three State" Outputs

MARCH 1978 *Preview*

Features

- 60ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND A POWER DOWN INPUT
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE - ONE PULSE/BIT ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY
- FAST ACCESS TIME - GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMP. AND VOLT. RANGES
- INDUSTRY'S HIGHEST PROGRAMMING YIELD

Description

The HM-7684P/85P are fully decoded high speed Schottky TTL 8192-Bit Field Programmable ROMs in a 2K words by 4 bit/word format with open collector (HM-7684P) or "Three State" (HM-7685P) outputs. These PROMs are available in an 18 pin DIP (ceramic or epoxy) and an 18 pin flatpack.

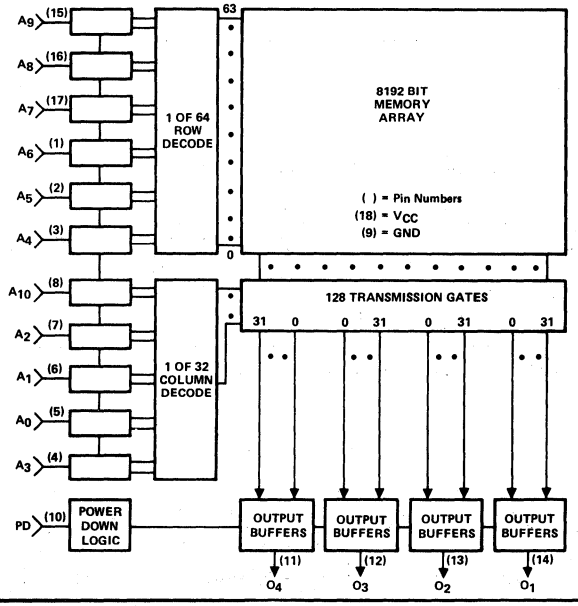
All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

Nichrome fuse technology is used on these and all other Harris Bipolar PROMs.

The HM-7684P/85P contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

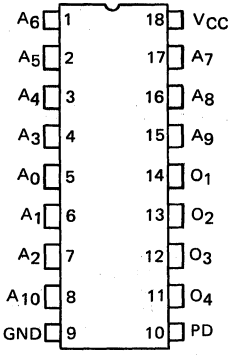
There is a power down input on the HM-7684P/85P which is similar to a chip enable. The chip is enabled or disabled using the power down input where a disabled chip dissipates 30% of nominal power and the outputs go to a high impedance state. The chip is powered up (enabled) when PD_1 is low.

Functional Diagram

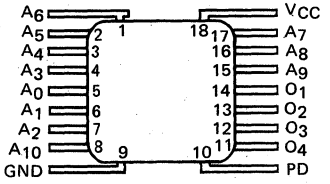


Pinouts

TOP VIEW - DIP



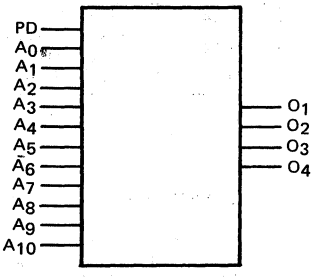
TOP VIEW - FLATPACK



PIN NAMES

$A_0 - A_{10}$	Address Inputs
$O_1 - O_4$	Data Outputs
PD	Power Down Input

Logic Symbol



ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7684P/85P-5 (V_{CC} = 5.0V ± 5%, T_A = 0°C to +75°C)
HM-7684P/85P-2 (V_{CC} 5.0V ± 10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH}	Address/Enable "1"	–	–	+40	µA	V_{IH} = V_{CC} Max.
I_{IL}	Input Current "0"	–	-50.0	-250	µA	V_{IL} = 0.45V
V_{IH}	Input Threshold "1"	2.0	1.5	–	V	V_{CC} = V_{CC} Min.
V_{IL}	Voltage "0"	–	1.5	0.8	V	V_{CC} = V_{CC} Max.
V_{OH}	Output "1"	2.4 *	3.2*	–	V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min.
V_{OL}	Voltage "0"	–	0.35	0.50	V	I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE}	Output Disable "1"	–	–	+40	µA	V_{OH}, V_{CC} = V_{CC} Max.
I_{OLE}	Current "0"	–	–	-40 *	µA	V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15*	–	-100*	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	120	170	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.
*"Three State" only

A.C. ELECTRICAL CHARACTERISTICS (Operating)

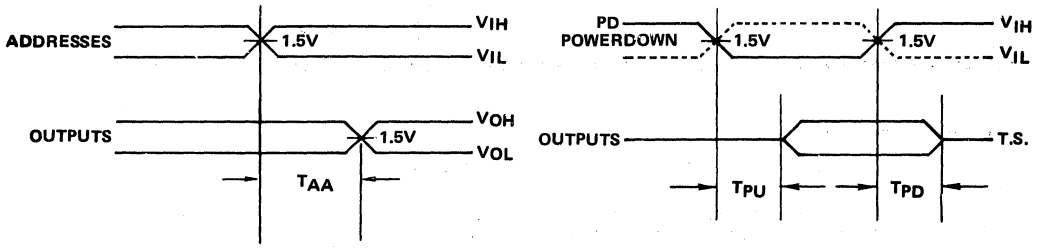
		HM-7684P/85P-5 5V ± 5% 0°C to +75°C			HM-7684P/85P-2 5V ± 10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	-	45	60	-	-	80	ns
T_{PD}	Chip Power Down Access Time	-	30	40	-	-	50	ns
T_{PU}	Chip Power-Up Access Time	-	80	100	-	-	150	ns

A.C. limits guaranteed for worst case N^2 sequencing.

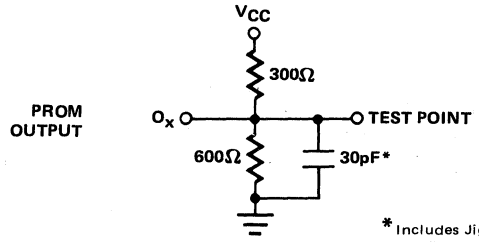
CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
CINA, CINCE	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
COUT	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS



A.C. TEST LOAD



HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

APRIL 1978 *Preview*

HM-7686/87

2K x 4 PROM

HM-7686 - Open Collector Outputs
HM-7687 - "Three State" Outputs

Features

- 60ns MAXIMUM ADDRESS ACCESS TIME.
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND THREE CHIP ENABLE INPUTS.
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE - ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME - GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD.

Description

The HM-7686/87 are fully decoded high speed Schottky TTL 8192-Bit Field Programmable Roms in a 2K word by 4 bit/word format with open collector (HM-7686) or "Three State" (HM-7687) outputs. These PROMs are available in a 20 pin DIP (ceramic or epoxy) and a 20 pin flatpack.

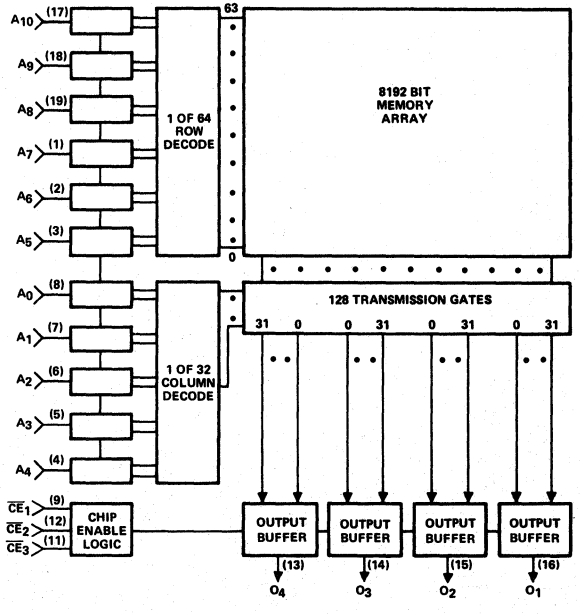
All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

Nichrome fuse technology is used on these and all other Harris Bipolar PROMs.

The HM-7686/87 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in test rows and columns are blown prior to shipment.

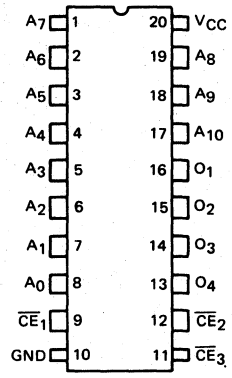
There are three chip enable inputs on the HM-7686/87. $\overline{CE}_1$, $\overline{CE}_2$, and $\overline{CE}_3$ low enables the chip.

Functional Diagram

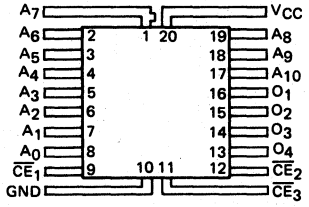


Pinouts

TOP VIEW – DIP



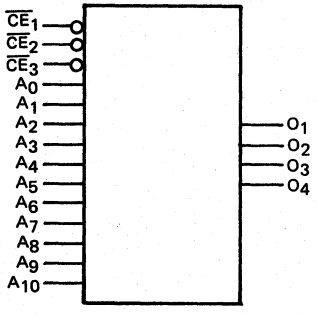
TOP VIEW – FLATPACK



PIN NAMES

$A_0 - A_{10}$	Address Inputs
$O_1 - O_4$	Data Outputs
$\overline{CE}_1, \overline{CE}_2, \overline{CE}_3$	Chip Enable Inputs

Logic Symbol



2

ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7686/87-5 (V_{CC} = 5.0V ± 5%, T_A = 0°C to +75°C)
HM-7686/87-2 (V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH}	Address/Enable "1"	—	—	+40	µA	V_{IH} = V_{CC} Max.
I_{IL}	Input Current "0"	—	-50.0	-250	µA	V_{IL} = 0.45V
V_{IH}	Input Threshold "1"	2.0	1.5	—	V	V_{CC} = V_{CC} Min.
V_{IL}	Voltage "0"	—	1.5	0.8	V	V_{CC} = V_{CC} Max.
V_{OH}	Output "1"	2.4*	3.2*	—	V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min.
V_{OL}	Voltage "0"	—	0.35	0.50	V	I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE}	Output Disable "1"	—	—	+40	µA	V_{OH}, V_{CC} = V_{CC} Max.
I_{OLE}	Current "0"	—	—	-40 *	µA	V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	—	—	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15*	—	-100*	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	—	120	170	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.
*"Three State" only

A.C. ELECTRICAL CHARACTERISTICS (Operating)

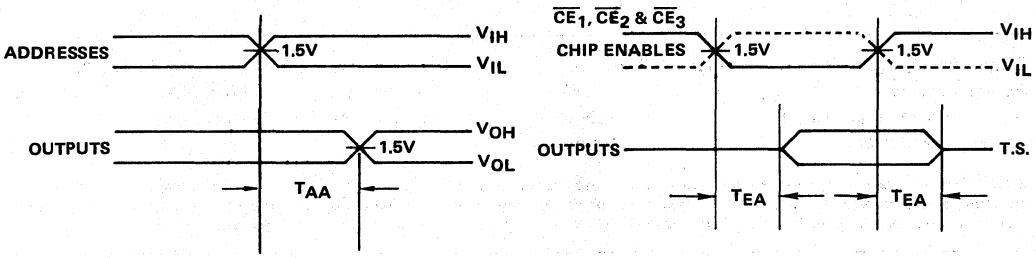
		HM-7686/87-5 5V ± 5% 0°C to +75°C			HM-7686/87-2 5V ± 10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	—	45	60	—	—	80	ns
T_{EA}	Chip Enable Access Time	—	30	40	—	—	50	ns

A.C. limits guaranteed for worst case N^2 sequencing.

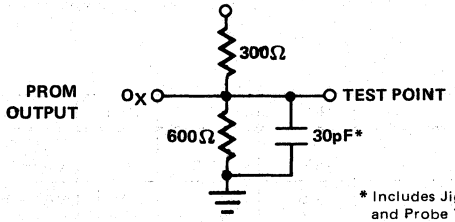
CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS



A.C. TEST LOAD



2

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

APRIL 1978 **Preview**

HM-7686R/87R

2K x 4 PROM

HM-7686R - Open Collector Outputs
HM-7687R - "Three State" Outputs

Features

- 60ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND TWO CHIP ENABLE INPUTS
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE - ONE PULSE/BIT ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY
- FAST ACCESS TIME - GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES
- INDUSTRY'S HIGHEST PROGRAMMING YIELD
- LATCHED OUTPUTS

Description

The HM-7686R/87R are fully decoded high speed Schottky TTL 8192-Bit Field Programmable ROMs in a 2K words by 4 bit/word format with open collector (HM-7686R) or "Three State" (HM-7687R) outputs. These PROMs are available in a 20 pin DIP (ceramic or epoxy) and 20 pin flatpack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

Nichrome fuse technology is used on these and all other Harris Bipolar PROMs.

The HM-7686R/87R contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

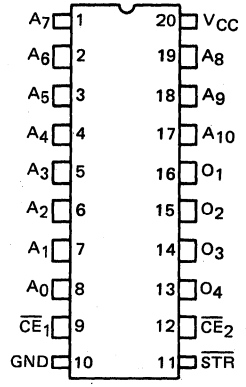
There are two chip enable inputs on the HM-7686R/87R. $\overline{CE}_1$, $\overline{CE}_2$ low enables the chip.

The HM-7686R/87R is operated in the Transparent Read Mode by holding the strobe input low throughout the read operation. This is the normal read mode where the two chip enable inputs will control the outputs.

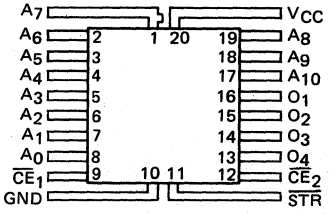
In Latched Read Mode, bringing the strobe input high will latch the outputs and chip enable inputs. If the device is disabled when the strobe input goes high, the outputs will be latched in the high impedance state. If the device is in the latched mode, the strobe input must be brought low to allow the outputs to respond to new address or chip enable conditions.

Pinouts

TOP VIEW-DIP



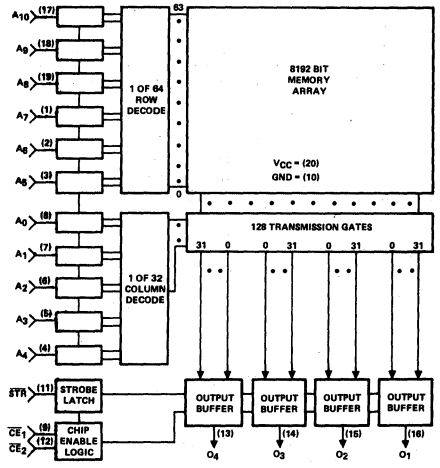
TOP VIEW-FLAT PACK



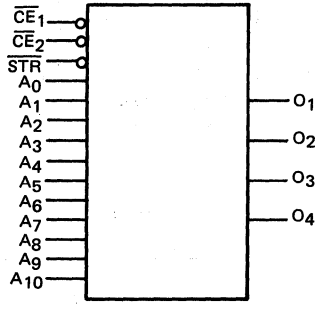
PIN NAMES

A_0-A_{10}	Address Inputs
O_1-O_4	Data Outputs
$\overline{CE}_1$, $\overline{CE}_2$	Chip Enable Inputs
$\overline{STR}$	Strobe Input

Functional Diagram



Logic Symbol



ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7686R/87R-5 (V_{CC} = 5.0V ± 5%, T_A = 0°C to +75°C)
HM-7686R/87R-2 (V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH}	Address/Enable "1"	–	–	+40	μA	V_{IH} = V_{CC} Max.
I_{IL}	Input Current "0"	–	-50.0	-250	μA	V_{IL} = 0.45V
V_{IH}	Input Threshold "1"	2.0	1.5	–	V	V_{CC} = V_{CC} Min.
V_{IL}	Voltage "0"	–	1.5	0.8	V	V_{CC} = V_{CC} Max.
V_{OH}	Output "1"	2.4 *	3.2*	–	V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min.
V_{OL}	Voltage "0"	–	0.35	0.50	V	I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE}	Output Disable "1"	–	–	+40	μA	V_{OH}, V_{CC} = V_{CC} Max.
I_{OLE}	Current "0"	–	–	-40 *	μA	V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15*	-2.5	-100*	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	120	170	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.
*"Three State" only

A.C. ELECTRICAL CHARACTERISTICS (Operating)

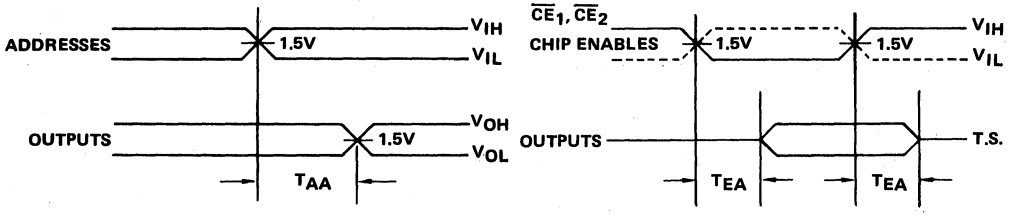
		HM-7686R/87R-5 5V ± 5% 0°C to +75°C			HM-7686R/87R-2 5V ± 10% -55°C to +125°C				
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS	TEST CONDIT.
T_{AA}	Address Access Time	–	45	60	–	–	80	ns	Latched or
T_{EA}	Chip Enable Access Time	–	30	40	–	–	50	ns	Transparent
T_{ADH}	Address Hold Time	0	-10	–	0	-10	–	ns	Latched Only
T_{CDH}	Chip Enable Hold Time	10	0	–	10	0	–	ns	
T_{SW}	Strobe Pulse Width	30	10	–	40	10	–	ns	
T_{SL}	Strobe Latch Time	60	40	–	80	40	–	ns	
T_{DL}	Strobe Delatch Time	–	–	40	–	–	50	ns	
T_{CDS}	Chip Enable Set-Up Time	40	–	–	50	–	–	ns	

A.C. limits guaranteed for worst case N^2 sequencing.

CAPACITANCE: T_A = 25°C

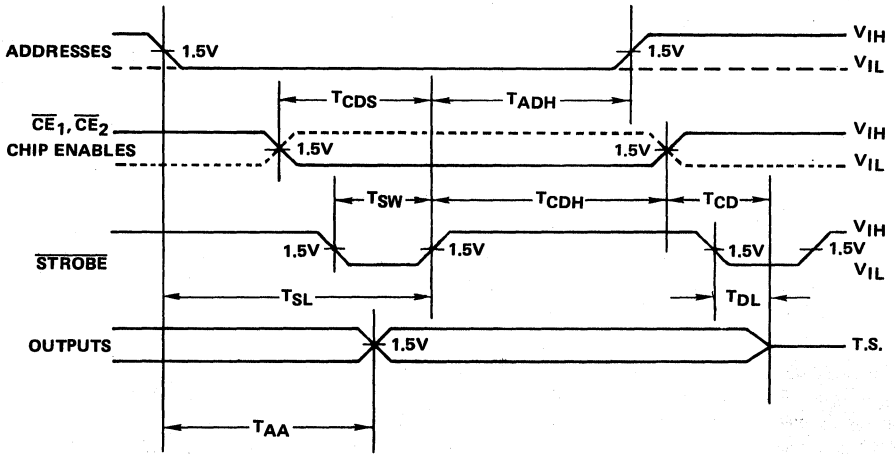
SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS (Transparent Mode)

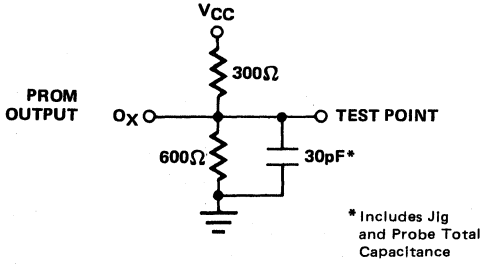


NOTE: Strobe input must remain low throughout read cycle while in transparent mode.

SWITCHING TIME DEFINITIONS (Latched Mode)



A.C. TEST LOAD



HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-7686P/87P

2K x 4 PROM

HM-7686P - Open Collector Outputs
HM-7687P - "Three State" Outputs

APRIL 1978 **Preview**

Features

- 60ns MAXIMUM ADDRESS ACCESS TIME.
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND THREE POWER DOWN INPUTS.
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE - ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME - FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD.

Description

The HM-7686P/87P are fully decoded high speed Schottky TTL 8192-Bit Field Programmable ROMs in a 2K word by 4 bit/word format with open collector (HM-7686P) or "Three State" (HM-7687P) outputs. These PROMs are available in a 20 pin DIP (ceramic or epoxy) and a 20 pin flatpack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

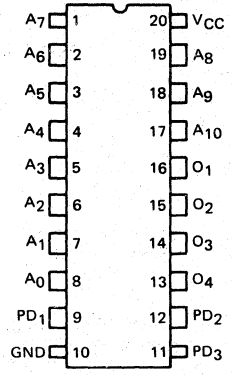
Nichrome fuse technology is used on these and all other Harris Bipolar PROMs.

The HM-7686P/87P contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

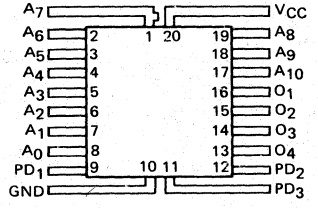
There are three power down inputs on the HM-7686P/87P which are similar to chip enables. The chip is enabled or disabled using the power down inputs where a disabled chip dissipates 30% of nominal power and the outputs go to a high impedance state. The chip is powered up (enabled) when PD_1, PD_2 and PD_3 are low.

Pinouts

TOP VIEW - DIP



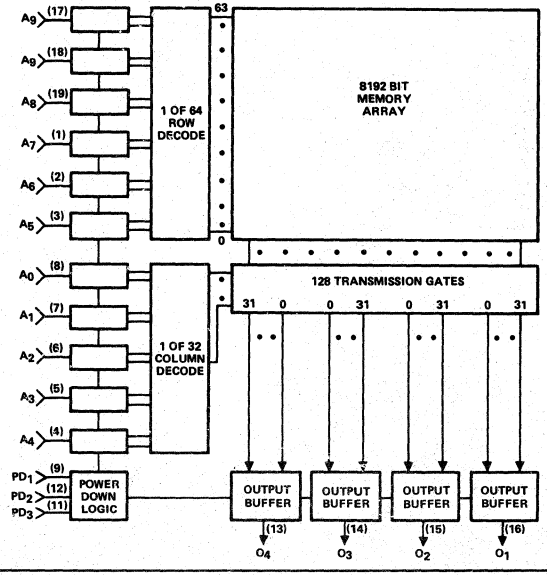
TOP VIEW - FLATPACK



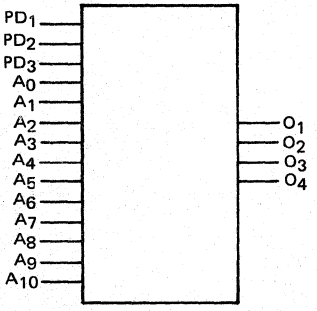
PIN NAMES

$A_0 - A_{10}$	Address Inputs
$O_1 - O_4$	Data Outputs
PD_1, PD_2, PD_3	Power Down Inputs

Functional Diagram



Logic Symbol



ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7686P/87P-5 (V_{CC} = 5.0V ± 5%, T_A = 0°C to +75°C)
HM-7686P/87P-2 (V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH}	Address/Enable "1"	–	–	+40	µA	V_{IH} = V_{CC} Max.
I_{IL}	Input Current "0"	–	-50.0	-250	µA	V_{IL} = 0.45V
V_{IH}	Input Threshold "1"	2.0	1.5	–	V	V_{CC} = V_{CC} Min.
V_{IL}	Voltage "0"	–	1.5	0.8	V	V_{CC} = V_{CC} Max.
V_{OH}	Output "1"	2.4*	3.2*	–	V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min.
V_{OL}	Voltage "0"	–	0.35	0.50	V	I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE}	Output Disable "1"	–	–	+40	µA	V_{OH}, V_{CC} = V_{CC} Max.
I_{OLE}	Current "0"	–	–	-40 *	µA	V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15*	–	-100*	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	120	170	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.
*"Three State" only

A.C. ELECTRICAL CHARACTERISTICS (Operating)

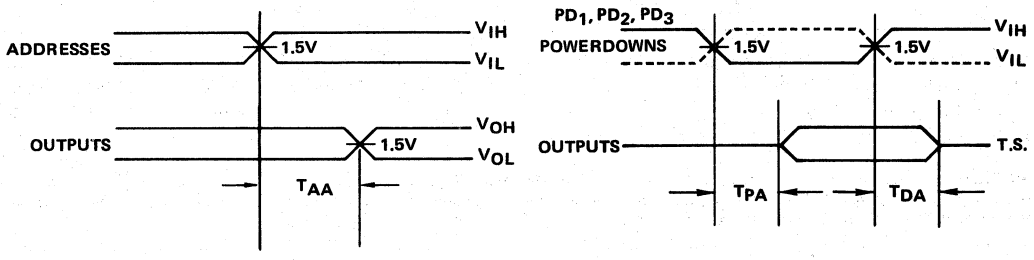
		HM-7686P/87P-5 5V ± 5% 0°C to +75°C			HM-7686P/87P-2 5V ± 10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	-	45	60	-	-	80	ns
T_{PD}	Chip Power Down Access Time	-	30	40	-	-	50	ns
T_{PU}	Chip Power-Up Access Time	-	80	100	-	-	150	ns

A.C. limits guaranteed for worst case N^2 sequencing.

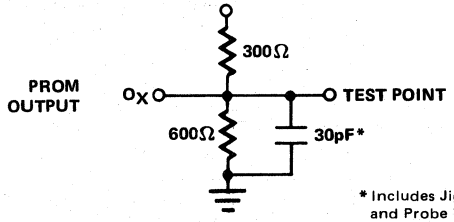
CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS



A.C. TEST LOAD



HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-7686RP/87RP

2K x 4 PROM

HM-7686RP - Open Collector Outputs
HM-7687RP - "Three State" Outputs

APRIL 1978 *Preview*

Features

- 60ns MAXIMUM ADDRESS ACCESS TIME.
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND A CHIP ENABLE INPUT.
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE - ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME - GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD.
- LATCHED OUTPUTS.
- A POWER DOWN INPUT ALLOWING 70% REDUCTION IN NOMINAL POWER DISSIPATION.

Description

The HM-7686RP/87RP are fully decoded high speed Schottky TTL 8192-Bit Field Programmable ROMs in a 2K words by 4 bit/word format with open collector (HM-7686RP) or "Three State" (HM-7687RP) outputs. These PROMs are available in a 20 pin DIP (ceramic or epoxy) and a 20 pin flatpack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

Nichrome fuse technology is used on these and all other Harris Bipolar PROMs.

The HM-7686RP/87RP contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

There is a chip enable input on the HM-7686RP/87RP. $\overline{CE}$ low enables the device.

There is also a power down input on this device. A powered down device has 70% reduction in nominal power dissipation if the outputs are not latched and 50% reduction in nominal power if the outputs are latched.

The HM-7686RP/87RP is operated in the Transparent Read Mode by holding the the strobe input low and the PD input low throughout the read operation. This is the normal read mode where the chip enable and the power down input will control the outputs.

In Latched Read Mode, bringing the strobe input high will latch the outputs and the chip enable input. However, the power down input is independent of the latch function and can be changed while in the latched mode. If the device is disabled when the strobe input goes high, the outputs will be latched in the high impedance state. If the device is in the latched mode, the strobe input must be brought low to allow the outputs to respond to new address or chip enable conditions.

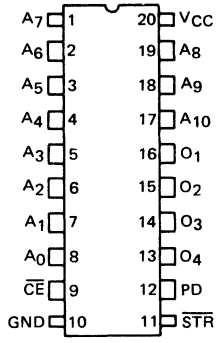
The following is a summary of the functional dependencies of the operating modes:

1. Chip enabled, transparent, powered up - normal mode where the power down input is effectively a chip enable with the I_{CC} reduction function.
2. Chip enabled, latched, power up - this is normal latched mode where the output remains latched regardless of address and chip enable switching.
3. Chip enabled, latched, power down - this is the powered down latched mode where the output data remains latched while power is reduced to 50% of its nominal value. If the latch strobe changes state while in this mode, the outputs will go to a high impedance state and power will reduce to 30% of nominal power. This is because the PD input becomes an effective chip enable in the Transparent Mode.
4. Chip disabled, transparent, power down - this is the normal powered down mode where the outputs are in a high impedance state and the power is reduced to 30% of the nominal power.

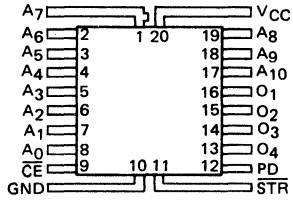
On the following page is a table to clarify the operational interdependencies.

Pinouts

TOP VIEW—DIP



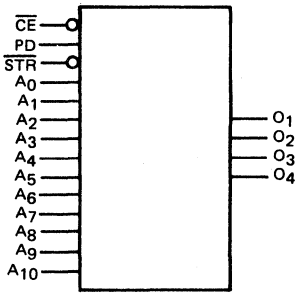
TOP VIEW—FLATPACK



PIN NAMES

A_0-A_{10}	Address Inputs
O_1-O_4	Data Ouputs
PD	Power Down Input
$\overline{STR}$	Strobe Input
$\overline{CE}$	Chip Enable Input

Logic Symbol

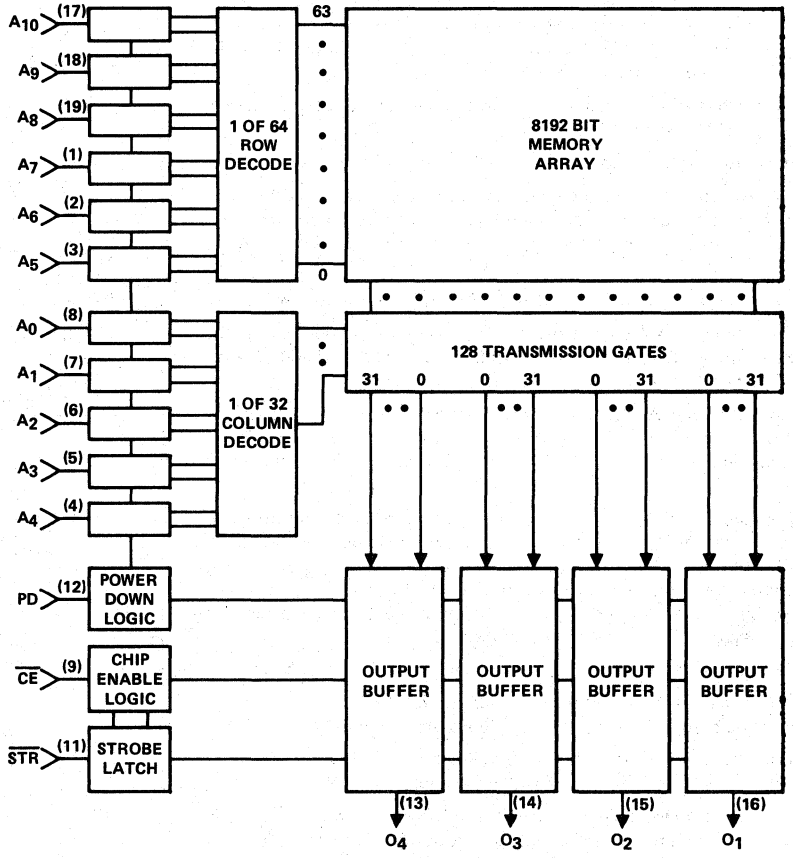


TRUTH TABLE for HM-7686RP/87RP

PD	$\overline{STR}$	$\overline{CE}$	OUTPUTS	POWER
0	0	0	Unlatched Data	100%
0	0	1	Unlatched "Three State"	100%
0	1	0	Latched Data	100%
0	1	1	Latched "Three State"	100%
1	0	0	Unlatched "Three State"	30%
1	1	0	Latched Data	50%
1	1	1	Latched "Three State"	50%

Assume that the sequence of transitions is: 1) Chip Enable, 2) $\overline{STR}$, 3) PD, and the initial state is Unlatched Data.

Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7686RP/87RP-5 (V_{CC} = 5.0V ± 5%, T_A = 0°C to +75°C)
HM-7686RP/87RP-2 (V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	– –	– -50.0	+40 -250	µA µA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	1.5 1.5	– 0.8	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4* –	3.2* 0.35	– 0.50	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40 -40*	µA µA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15*	-2.5	-100*	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	120	170	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.
*"Three State" only

A.C. ELECTRICAL CHARACTERISTICS (Operating)

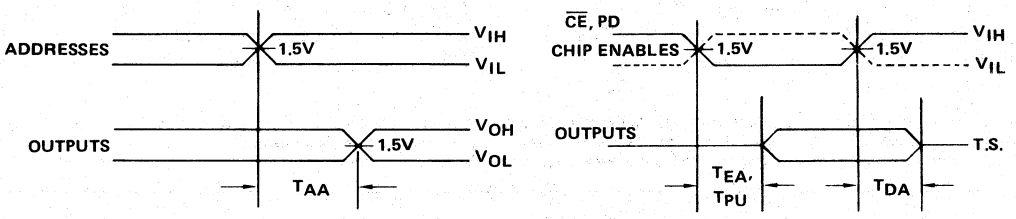
		HM-7686RP/87RP-5 5V ± 5% 0°C to +75°C			HM-7686RP/87RP-2 5V ± 10% -55°C to +125°C				
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS	TEST COND.
T_{AA}	Address Access Time	-	45	60	-	-	80	ns	Latched or
T_{DA}	Chip Disable Access Time	-	30	40	-	-	50	ns	Transparent
T_{EA}	Chip Enable Access Time	-	30	40	-	-	50	ns	
T_{PU}	Chip Power-Up Access Time	-	80	100	-	-	150	ns	
T_{ADH}	Address Hold Time	0	-10	-	0	-10	-	ns	Latched Only
T_{CDH}	Chip Enable Hold Time	10	0	-	10	0	-	ns	
T_{SW}	Strobe Pulse Width	30	10	-	40	10	-	ns	
T_{SL}	Strobe Latch Time	60	40	-	80	40	-	ns	
T_{DL}	Strobe Delatch Time	-	-	40	-	-	50	ns	
T_{CDS}	Chip Enable Set-Up Time	40	-	-	50	-	-	ns	

A.C. limits guaranteed for worst case N^2 sequencing.

CAPACITANCE: T_A = 25°C

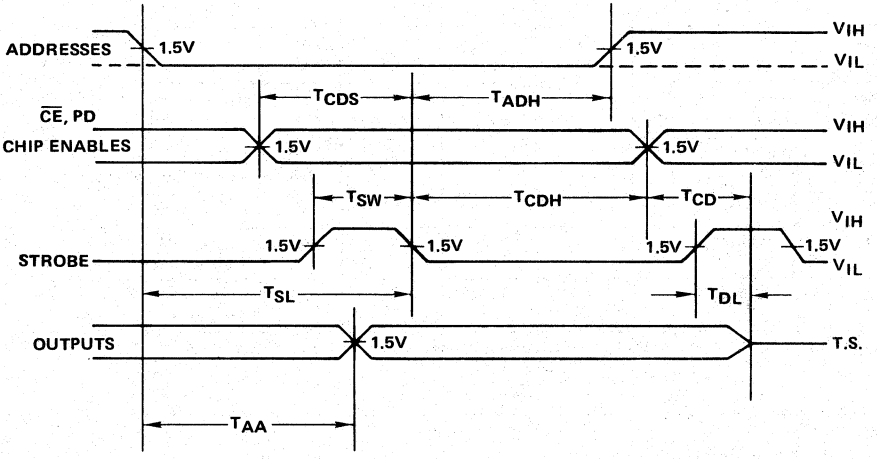
SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
CINA, CINCE	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
COUT	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS (Transparent Mode)

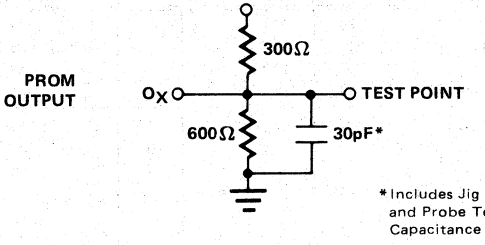


NOTE: Strobe input must remain low throughout read cycle while in transparent mode.

SWITCHING TIME DEFINITIONS (Latched Mode)



A.C. TEST LOAD



HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

JAN-0512

512 BIT, BIPOLAR PROM
MIL/M38510/20101

MARCH 1978

Features

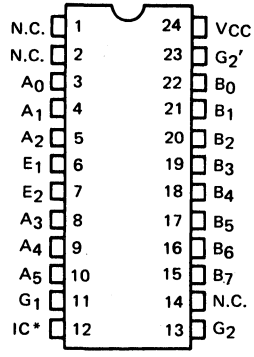
- FIELD PROGRAMMABLE
- 64 WORDS/8 BITS PER WORD
- FULLY DECODED
- DTL/TTL COMPATIBLE
- 55ns ACCESS TIME

Description

The JAN-0512 is a field programmable 64 word by 8 bit PROM. In an unprogrammed memory, all "Memory Elements" are short circuits so that logical "zeros" appear at each output bit position for any address input. "Electronic Programming" involves the alteration of specific "Memory Elements" to create logical "ones" in selected bit positions. This alteration is irreversible and cannot be accomplished under normal operating conditions.

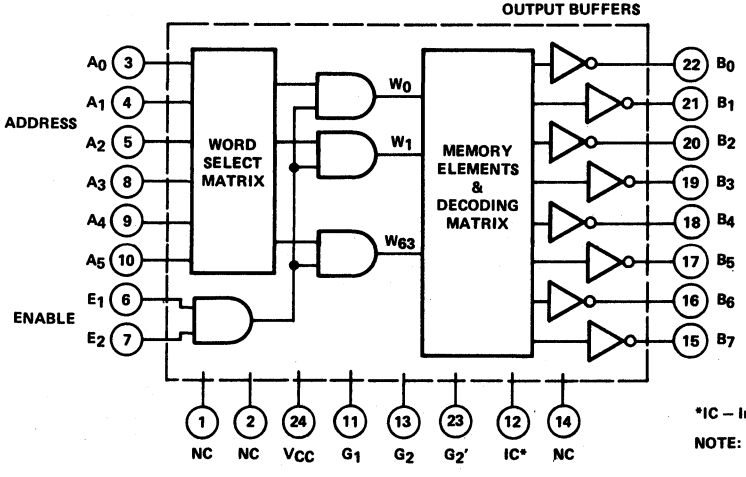
Pinout

TOP VIEW – D.I.P.



*Must be left open circuit

Block Diagram



*IC – Internal Connection must be left open

NOTE: For operational condition, return pins 11, 13, and 23 to system ground.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range	-0.5 V_{DC} to 7.0 V_{DC}
Input Voltage Range	-1.5 V_{DC} at -12mA to 5.5V_{DC}
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering 10 Seconds)	300°C
Thermal Resistance, Junction-to-Case	JC' Case J = 30°C/w
Output Supply Voltage	-0.5V_{DC} to 7.0V_{DC}
Output Sink Current	+30mA
Maximum Power Dissipation, P_D	575mWdc
Maximum Junction Temperature, T_J	175°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltage	4.75 V_{DC} Min. to 5.25V_{DC} Maximum
Minimum High Level Input Voltage	2.0V_{DC}
Maximum Low Level Input Voltage	0.8V_{DC}
Normalized Fanout (Each Output)	6 Maximum (10mA)
Ambient Operating Temperature Range	-55°C to +125°C

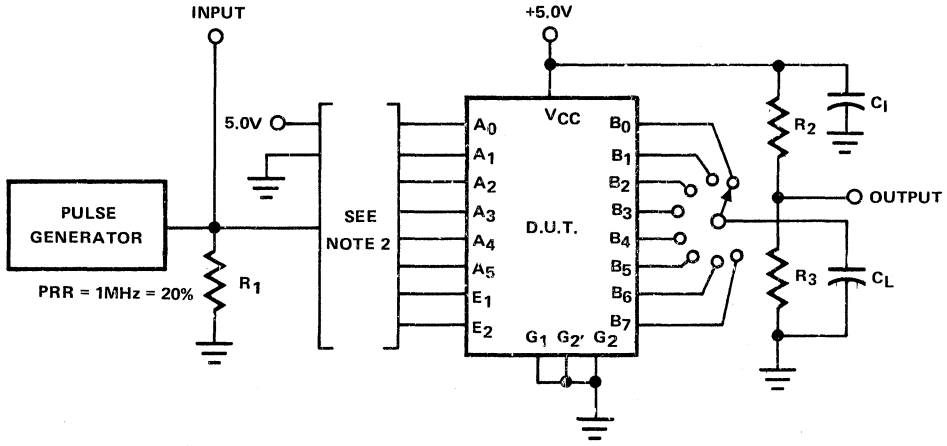
ELECTRICAL CHARACTERISTICS

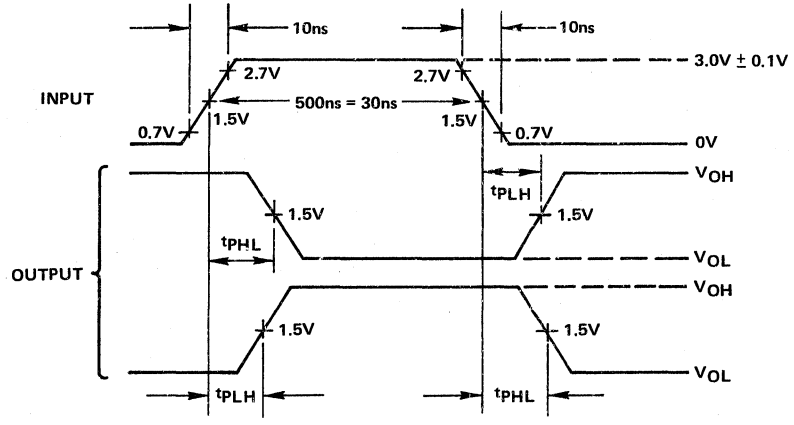
The electrical characteristics are as specified in the table and apply over the full recommended ambient operating temperature range, unless otherwise specified.

SYMBOL	TEST	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
V_{OH}	High Level Output Voltage	2.4		Volts	V_{CC} = 4.75V V_{IN} = 0.8V I_{OH} = -500μA
V_{OL}	Low Level Output Voltage		0.45	Volts	V_{CC} = 4.75V V_{IN} = 2.0V I_{OL} = 10mA
V_{IC}	Input Clamp Voltage		-1.5	Volts	V_{CC} = 4.75V I_{IN} = -12mA T_A = 25°C
I_{CEX1}	Maximum Collector Cut-Off Current		100	μA	V_{CC} = 5.25V V_{OH} = 2.8V V_{IN} = 0.8V
I_{CEX2}			200	μA	V_{CC} = 5.25V V_{OH} = 5.25V V_{IN} = 0.8V
I_{IH1}	High Level Input Current		60	μA	V_{CC} = 5.25V V_{IN} = 2.4V;
I_{IH2}			100	μA	V_{CC} = 5.25V V_{IN} = 5.25; ①
I_{IL}	Low Level Input Current	-0.2	-1.6	mA	V_{CC} = 5.25V V_{IN} = 0.4V; ②
I_{CC}	Supply Current		100	mA	V_{CC} = 5.25V V_{IN} = 0
tPHL	Propagation Delay Time High-to-Low Level Logic	25	140	ns	V_{CC} = 5.0V C_L = 30pF Min. R_1 = 470Ω ±5%
tPLH	Propagation Delay Time Low-to-High Level Logic	25	140	ns	

NOTES: 1. When testing one E input, apply 5.25V to the other.
2. When testing one E input, apply GND to the other.

Switching Time Test Circuits



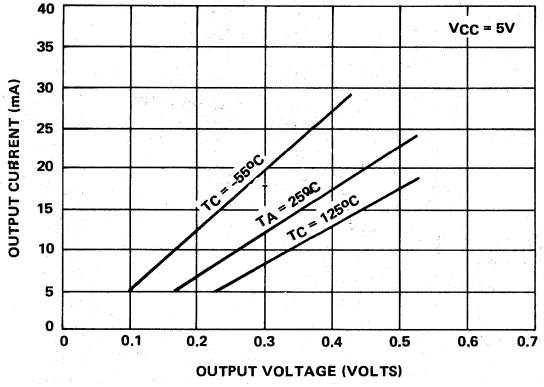


NOTES:

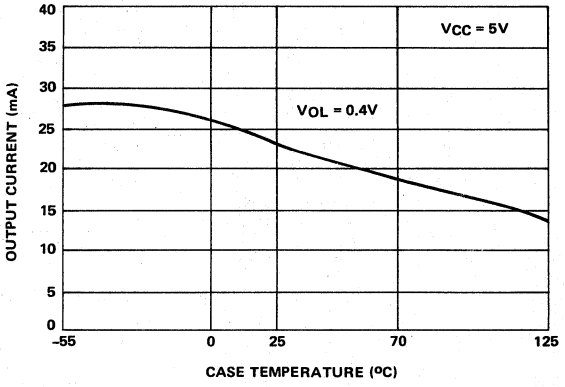
1. Pins 12 and 14 shall be left open.
2. The applicable test table should be selected from the altered item drawing.
3. $C_1 = 0.5\mu F \pm 10\%$; $R_1 = 50\Omega \pm 5\%$; $R_2 = 470\Omega \pm 5\%$; $R_3 = 1k\Omega \pm 5\%$; C_L = 30pF including jig and probe capacitance.

Characteristic Curves

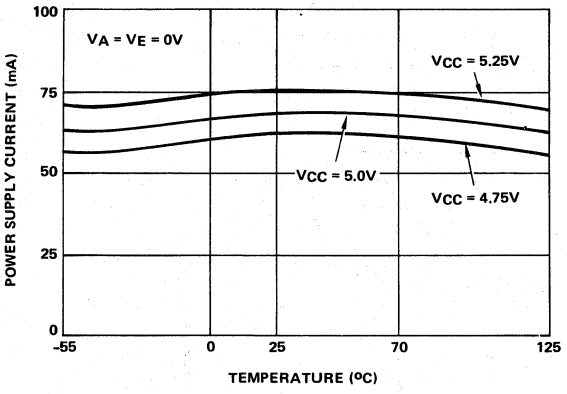
OUTPUT CHARACTERISTICS



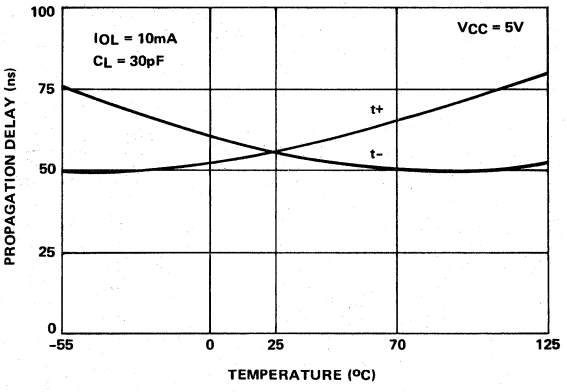
OUTPUT CURRENT vs. TEMPERATURE



POWER SUPPLY CURRENT vs. TEMPERATURE



PROPAGATION DELAY vs. TEMPERATURE



PROGRAMMING SPECIFICATIONS

PARAMETER	VALUE
Address Input Voltage High Logic Level Low Logic Level	 Open Circuit ① -5.0V
Power Supply Voltage	+5.0V +5%, -0%
G_1 Voltage ②	-5.0V
G_2 Voltage	0V
G_2' Voltage For Device Type 01 Circuit A	 Open
Maximum Programming Voltage	-7.0V
Maximum Programming Current	100mA
Maximum Number or Attempts to Program a Given Bit	2
Maximum Case Temperature During Programming	75°C

1. Open collector TTL gates meet this requirement.
2. G_1 must be connected to -5.0V prior to applying V_{CC} or programming voltage.

PROGRAMMING PROCEDURES

Using the test conditions of the table, the following procedures shall be used for programming the device:

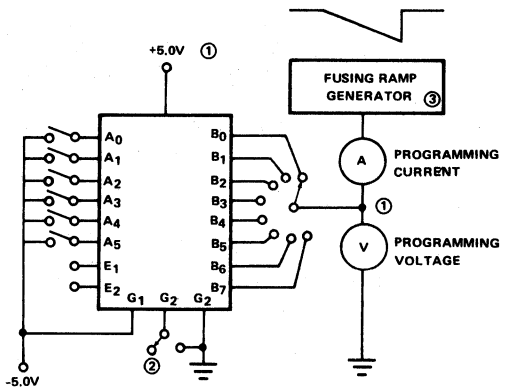
(a) Connect the device as shown in Figure 1, using the fusing generator of Figure 1 or the alternate circuit of Figure 2. The circuit shown in Figure 2 can be used in more automated programming systems. This circuit generates a current pulse which is at the proper voltage and current levels for fast reliable programming. The input programming pulse width shall be 750ms ±50ms. The number of attempts to program a given bit shall be as specified in the table.

(b) To address a particular word in the memory, set the input switches to the binary equivalent of that word, where a logical low level is -5.0V and a logical high level is an open circuit. (Do not return to supply). All output bits (B_0, B_1, . . . B_7) of this word are not available for programming.

(c) With the output current limited (as specified in the table), apply a negative going current pulse to the pin associated with the first bit to be changed from a logical low level to a logical high level. This is most easily accomplished by connecting the negative terminal of a variable power supply to the proper output pin and manually increasing the voltage to approximately 6.0V.

(d) Skipping any bit which is to remain a logical low level, repeat step (c) for each logical low level in the word being addressed. Not more than one bit shall be programmed at a time.

(e) Set the next input address and repeat steps (c) and (d). This procedure is repeated for each input address for which a specific output word pattern is desired. Note that all addresses do not have to be programmed at the same time, nor do all output bits for a given address. A logical low level can always be changed to a logical high level, simply by repeating steps (b) and (c). A logical low level, once programmed to a logical high level, cannot be reprogrammed.



NOTES:
1. Connect -5.0V to G_1 before applying V_{CC} or programming voltage.
2. For device type 01, G_2' shall be open.
3. Generator characterisitics are defined in Programming Procedures.

FIGURE 1
PROGRAMMING CONNECTIONS

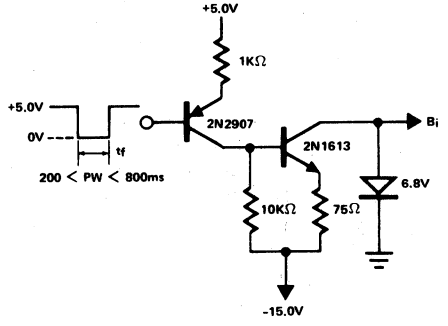


FIGURE 2
PROGRAMMING CIRCUIT

All 76xxx series devices utilize the same programming method which is one of the characteristics that lends to the term "Generic" PROM.

Harris Generic PROMs have the industry's highest programming yield and exhibit an extremely high level of reliability in the field, however, this level of device quality can only be obtained if the PROM has been properly programmed to the data sheet specifications. Outlined below are the key points which deserve attention to assure that programming has been optimumly performed.

- Be certain that you are following the latest revision status of programming specifications.
- If you are utilizing a commercial programmer, be sure that the card set for Harris Generic PROMs is certified for the most recent revision level.
- Have the Programmer calibrated at routine intervals to assure that the electrical and mechanical characteristics are acceptable. This would include such things as:
  - Making certain that the socket which the device is placed into is clean of corrosion and is mechanically sound.
  - Checking ribbon cable connectors for good continuity.
  - Making sure that all voltage levels conform to the programming specifications.
  - Assuring that all pulses are clean of distortion and exhibit the correct timing characteristics.

If there is any problem in determining how to follow any of these guidelines, contact a local Harris office for assistance.

PROGRAMMING PROCEDURE

The following is the generic programming procedure which is used for all Harris Generic 76xxx PROMs. Please note that the PD input(s) on power down devices can be considered equivalent to chip enable input(s) during the programming procedure in that they both disable the device. Also, the logic levels required to place the strobe input into the "transparent read" mode (essential during programming) will vary among the various device types.

The HM-76xxx PROMs are manufactured with all bits storing a logical "1" (output high). Any desired bit can be programmed to a logical "0" (output low) by following the simple procedure shown below. One may build his own programmer to satisfy the specifications described in the table, or use any of the commercially available programmers which meet these specifications. This PROM can be programmed automatically or by the manual procedure shown on the next page.

Programming Specifications

SYMBOL	PARAMETER	MINIMUM	RECOMMENDED OR TYPICAL	MAXIMUM	UNITS
V_{IH} V_{IL}	Address Input Voltage (1)	2.4 0.0	5.0 0.4	5.0 0.5	V V
V_{PH} (2) V_{PL} (3)	Programming/Verify Voltage to V_{CC}	12.0 4.5	12.0 4.5	12.5 5.5	V V
I_{ILP}	Programming Input Low Current at V_{PH}	–	-300	-600	μA
t_r t_f	Programming (V_{CC}) Voltage Rise and Fall Time	1.0 1.0	1.0 1.0	10.0 10.0	μs μs
t_d	Programming Delay	10	10	100	μs
t_p	Programming Pulse Width (4)	90	100	110	μs
P.D.C.	Programming Duty Cycle	–	50	90	%
V_{OPE} V_{OPD}	Output Voltage Enable (5) Disable	10.5 4.5	10.5 5.0	11.0 5.5	V V
I_{OPE}	Output Voltage Enable Current	–	–	10.0	mA
T_a	Ambient Temperature	–	25	75	°C

During programming the chip must be disabled for proper operation.

NOTES: 1. No inputs should be left open for V_{IH}.
2. V_{PH} source must be capable of supplying one ampere.
3. It is recommended that dual verification be made at V_{PL} min and V_{PL} max.
4. Note step 11 in programming procedure.
5. Disable condition will be met with output open circuited.

1. If the device has latched outputs (HM-76xxR): apply to the strobe input, the logical level required to place the device into the "transparent read" mode which is essential during programming. The strobe must remain in the "transparent read" mode throughout the entire programming procedure. Consult the individual data sheet of the device concerned to determine whether a logical "0" or a logical "1" is required to meet this condition.

2. Address the PROM with the binary address of the word to be programmed. Address inputs are TTL compatible. An open circuit should not be used to address the PROM.

3. Bring the $\overline{CE}_X$ (PD_X) input(s) high and the CE_X ($\overline{PD}_X$) input(s) low to disable the device. The disabling of the device during programming is an essential step in correctly programming all Harris PROMs. The chip enables are TTL compatible. An open circuit should not be used to disable the device. (Disregard this step for devices which have no chip enable or power down inputs.)

4. Disable the programming circuitry by applying a voltage disable of V_{OPD} to the outputs of the PROM. Any output may be left open to achieve the disable.

5. Raise V_{CC} to V_{PH} with rise time $\leq t_r$.

6. After a delay $\geq t_d$, apply a pulse with amplitude of V_{OPE} and duration of t_p to the output selected for programming. Note that the PROM is manufactured with fuses intact which generate an output high. Programming a fuse will cause the output to be in the V_{IL} state in the verify mode.

7. Other bits in the same word may be programmed while the V_{CC} input is raised to V_{PH} by applying output enable pulses to each output which is to be programmed. The output enable pulses must be separated by a minimum interval of t_d.

8. Lower V_{CC} to 4.5 volts following a delay of t_d from the last programming enable pulse applied to an output.

9. Enable the PROM for verification by applying V_{IL} to $\overline{CE}_X$ (PD_X) and V_{IH} to CE_X ($\overline{PD}_X$).

10. Repeat verification (step 9) at V_{CC} = 5.5 volts.

11. If any bit does not verify as programmed, repeat steps 2 through 9 until the bit has received a total of 1msec of programming time. Bits which do not program within 1msec are programming rejects. No further attempt to program these parts should be made.

12. Repeat steps 1 through 11 for all other bits to be programmed in the PROM.

13. Programming rejects returned to the factory must be accompanied by data giving address, desired data, and actual output data of the location in which a programming failure has occured.

Typical Programming Circuit

The circuit and timing diagrams shown in Figures 1 and 2 will establish the proper programming conditions for the output enable pulses. This allows the use of standard TTL parts for all logic inputs to the PROM. Note the gate which senses the output must withstand up to 11.0 volts during programming.

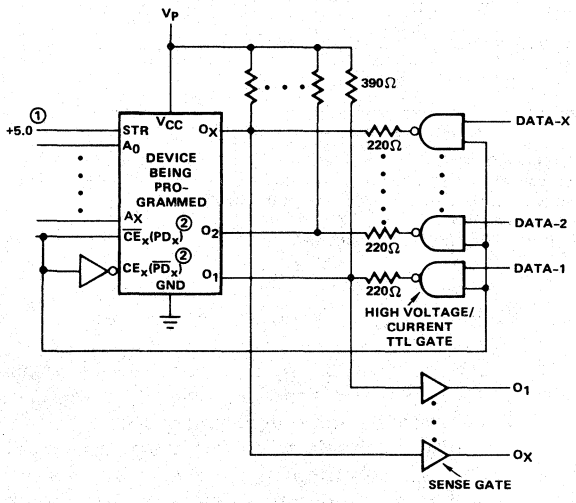


FIGURE 1

① The strobe input must remain at V_{IH} throughout the procedure. (for latched output devices only.)

② Disregard for devices with no enable inputs.

NOTE: For the 7629, pin 23 must remain at 5V during programming.

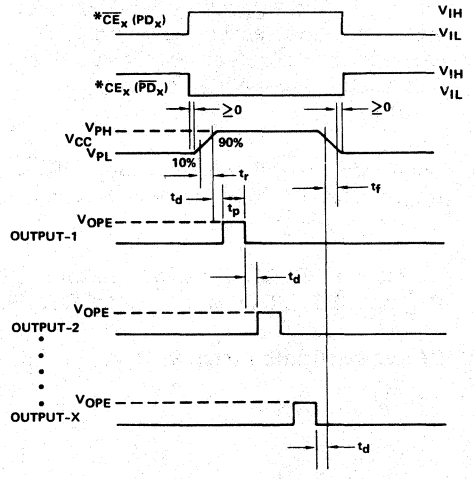


FIGURE 2

* Disregard for devices with no enable inputs.

The strobe input must remain at V_{IH} throughout the procedure. (for latched output devices only.)

This timing diagram shows device terminal conditions. Each positive going data pulse at the terminal blows the corresponding bit, resulting in a low output for that bit. Therefore, a low input at the DATA-X points of the Figure 1 circuit results in a permanent low output of a bit.

Programming equipment models identified in the accompanying list have been spot checked by Harris Semiconductor and found to be acceptable for use in programming Harris PROMs. This list is provided only as a convenience to purchasers of Harris PROMs to identify programmer model potentially suitable for programming the PROMs. It is neither intended to be a representation or warranty by Harris of the capability of all listed programmer models nor an indication of unsuitability of other programmer models not contained in list. PROM purchasers are advised to adhere to the programming requirements specified in Harris' current data sheets applicable to the PROMs to be programmed. Responsibility for programmer performance lies solely with the equipment manufacturer. The programmer user is cautioned to verify operation and performance according to the manufacturer's instruction and specifications prior to each use, and to determine that the programming complies with the applicable Harris PROM data sheet. Harris accepts no responsibility for PROMs which have been subjected to incorrect or faulty programming.

DATA I/O

Main Frame: All in which 909-XXXX card sets are specified.

CARD SET	PRODUCTS	COMMENTS
909-1063-4 REV S	76XX	Preferred
909-1063-4 REV H	76XX	Acceptable
909-1319-3 REV B	6611-X	
909-1055-3 REV C	HMX-1024X-X	Not recommended for new designs.
909-1054-3 REV E	HMX-0512-X	
909-1051-4 REV D	HMX-8256	

PROLOG

Main Frame Model: PM 9000.

MODULE	PRODUCTS	COMMENTS
PM 9018	HPROM 1024	Not recommended for new designs.
PM 9031	HM-7602	
PM 9027	HM-7610/11 HM-7620/21	
PM 9029	HM-7640/41	
PM 9036	HM-7642/43	
PM 9039	HM-76XX	Generic module requires respective socket & configurator.
PM 9056	HM-6611	

INTERNATIONAL MICROSYSTEMS INC.

Main Frame: IM 1000.

MODULE	PRODUCTS	COMMENTS
IM 1063	76XX	Generic module requires specified socket adapter.

Data Entry Formats for Harris Custom Programming *

For Harris to custom program to a user data pattern specification, the user must supply the data in one of the following formats:

1. Master PROM of same organization and pinout as device ordered. Two pieces required, three preferred.
2. Paper tape in Binary or ASCII BPNF.

* BINARY PAPER TAPE FORMAT

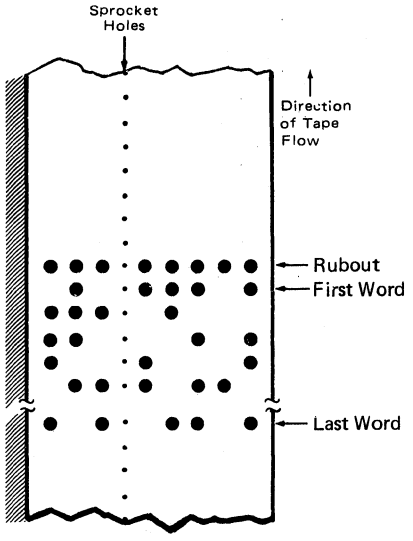
- A minimum of six inches of leader.
- A rubout (all eight locations punched).
- Data words beginning with the first word (word "0"), proceeding sequentially, ending with the last word (word "N"), with no interruptions or extraneous characters of any kind.
- Specifiy whether a punched hole is a VOH = "1" = logic high or is a VOL = "0" = logic low.
- A minimum trailer of six inches of tape.

* ASCII BPNF FORMAT

- A minimum leader of twenty rubouts (all eight locations punched).
- Any characters desired (none necessary) except "B".
- Data words beginning with the first word (word "0"), proceeding sequentially, ending with the last word (word "N").
- Data words consist of:
  1. The character "B" denoting the beginning of a data word.
  2. A sequence of characters, only "P" or "N", one character for each bit in the word.
  3. The character "F" denoting the finish of the data word.
- No extraneous characters of any kind may appear within a data word (between any "B" and the next "F").
- Errors may be deleted by rubouts superimposed over the entire word including the "B", and beginning the word again with a new "B".
- Any text of any kind (except the character "B") is allowed between data words (between any "F" and the next "B"), including carriage return and line feed.
- A minimum trailer of twenty-five rubouts.
- Specify whether a "P" is a "1" = VOH = logic high or is a "0" = VOL = logic low.
- The use of even or odd parity is optional.

* *Harris can not assume responsibility for PROMs programmed to data tapes or masters which contain errors. The user must insure the accuracy of the data provided to Harris. Harris guaranteed that the programmed PROMs will contain the information provided if either of the following formats are followed.*

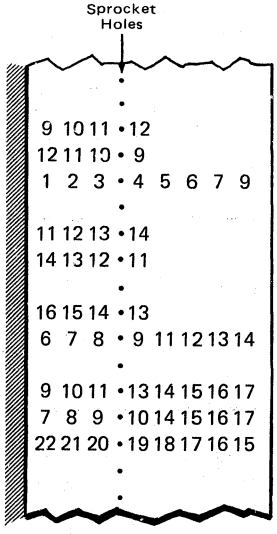
BINARY PAPER TAPE EXAMPLE



Resulting Truth Table
Punched Hole = "0" = VOL = Logic Low

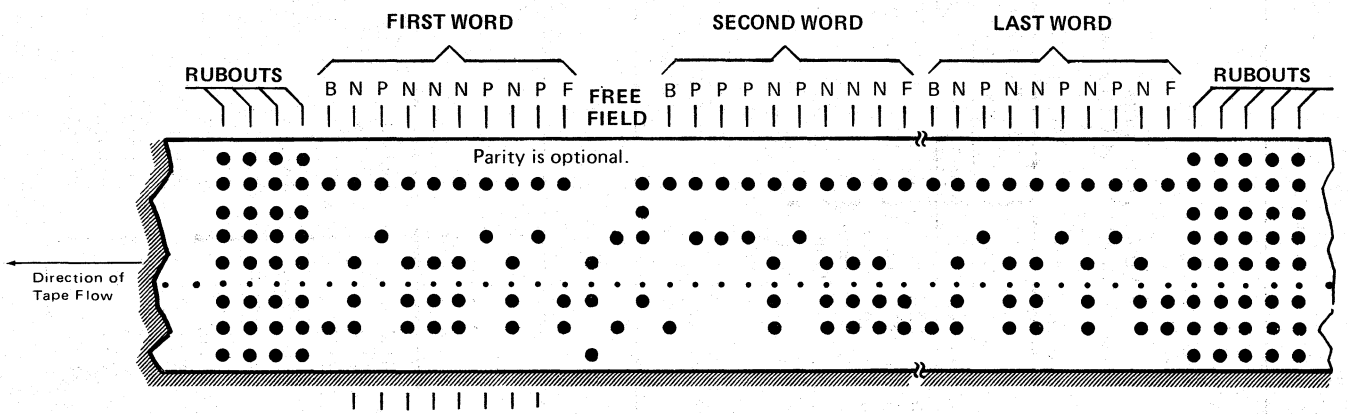
Word				PROM Output								
				(24 Pin Package) Pin Numbers								
AX···A2	A1	A0		17	16	15	14	13	11	10	9
0···0	0	0	First	0	1	0	0	0	1	0	1
0···0	0	1	Second	1	1	1	0	1	0	0	0
0···0	1	0	Third	0	1	0	1	1	1	0	0
0···0	1	1	Fourth	0	1	1	1	0	1	1	0
0···1	0	0	Fifth	1	0	0	1	0	0	0	1
1···1	1	1	Last	0	1	0	0	1	0	1	0

DEVICE OUTPUT PACKAGE PINS



Package	Example
16 Pin CMOS	HM-6611
16 Pin Bipolar	HM-7611
16 Pin	HM-7603
18 Pin CMOS	HM-6661
18 Pin Bipolar	HM-7643
20 Pin	HM-7687
20 Pin	HM-7649
24 Pin	HM-7641
24 Pin	HM-7647
24 Pin	HM-0512

ASCII BPNF PAPER TAPE EXAMPLE



EXAMPLE	PACKAGE TYPE	DEVICE OUTPUT PINS
HM-6611	16 Pin Pkg	12 11 10 9 (MOS)
HM-7611	16 Pin Pkg	9 10 11 12 (Bipolar)
HM-7603	16 Pin Pkg	9 7 6 5 4 3 2 1
HM-6661	18 Pin Pkg	14 13 12 11 (MOS)
HM-7643	18 Pin Pkg	11 12 13 14 (Bipolar)
HM-7687	20 Pin Pkg	13 14 15 16
HM-7649	20 Pin Pkg	14 13 12 11 9 8 7 6
HM-7641	24 Pin Pkg	17 16 15 14 13 11 10 9
HM-7647	24 Pin Pkg	17 16 15 14 10 9 8 7
HM-0512	24 Pin Pkg	15 16 17 18 19 20 21 22

ResultingTruth Table
Character "P" = "I" = VOH = Logic High

Word		PROM Output (24 Pin Pkg) Pin Numbers							
Ax ···A2 A1 A0		17	16	15	14	13	11	10	9
0 ··· 0 0 0	First	0	1	0	0	0	1	0	1
0 ··· 0 0 1	Second	1	1	1	0	1	0	0	0
1 ··· 1 1 1	Last	0	1	0	0	1	0	1	0

CMOS Memory

3

Product Index

3

Symbols and Abbreviations

This data sheet utilizes a new set of specification nomenclature. This new format is an IEEE and JEDEC supported standard for semiconductor memories. It is intended to clarify the symbols, abbreviations and definitions, and to make all memory data sheets consistent. We believe that, once acclimated, you will find this standardized format easy to read and use.

ELECTRICAL PARAMETER ABBREVIATIONS

All abbreviations use upper case letters with no subscripts. The initial symbol is one of these four characters:

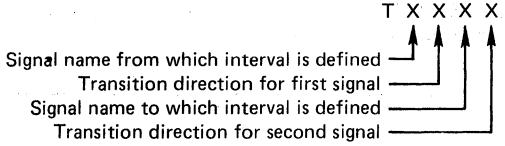
V (Voltage)
I (Current)
P (Power)
C (Capacitance)

The second letter specifies input (I) or output (O), and the third letter indicates the high (H), low (L) or off (Z) state of the pin during measurements. Examples:

VIL — Input Low Voltage
IOZ — Output Leakage Current

TIMING PARAMETER ABBREVIATIONS

All timing abbreviations use upper case characters with no subscripts. The initial character is always T and is followed by four descriptors. These characters specify two signal points arranged in a "from-to" sequence that define a timing interval. The two descriptors for each signal point specify the signal name and the signal transitions. Thus the format is:



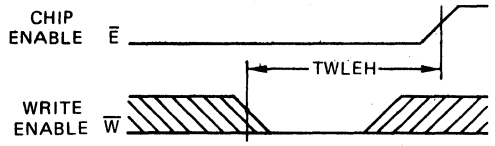
Signal Definitions:

A = Address
D = Data In
Q = Data Out
W = Write Enable
E = Chip Enable
S = Chip Select
G = Output Enable

Transition Definitions:

H = Transition to High
L = Transition to Low
V = Transition to Valid
X = Transition to Invalid or Don't Care
Z = Transition to Off (High Impedance)

EXAMPLE:



The example shows Write pulse setup time defined as TWLEH-Time from Write enable Low to chip Enable High.

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address set-up time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WAVEFORMS

WAVEFORM SYMBOL	INPUT	OUTPUT
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	—	HIGH IMPEDANCE

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-6312/6312A

CMOS ROM
1024 Word x 12 Bit

JULY 1978

Features

- HM-6100 COMPATIBLE
- LOW POWER - TYPICAL < 5.0μW STANDBY
- 4 - 11 VOLT VCC OPERATION
- HIGH SPEED
- STATIC OPERATION

Description

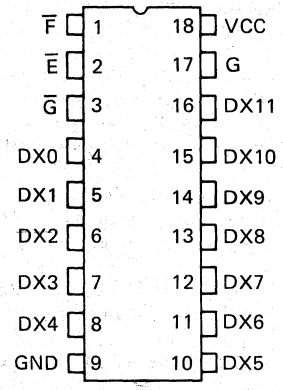
The HM-6312 and HM-6312A are high speed, low power, silicon gate CMOS static ROM's, organized 1024 words by 12 bits. In all static states these units exhibit the microwatt power requirements typical of CMOS. The basic part operates at 4 - 7 volts with a typical 5 volt 25°C access time of 350ns. Higher operating voltages, 4 - 11 volts, are available with the A version. Signal polarities and functions are specified for interfacing with the HM-6100 Microprocessor.

Operation

Addresses and data out are multiplexed on 12 lines, DX0 - DX11. Addresses are loading into an on chip register by falling edge of CE. Data out, corresponding to the latched address, is enabled when CE, OEL and OEH are true. The RSEL output defines an area in the 4096 word addressing space dedicated to RAM. It can be programmed by DX0, DX1, DX2 and DX3. This output eliminates a four bit register and decoder for the high order address bits to select RAM.

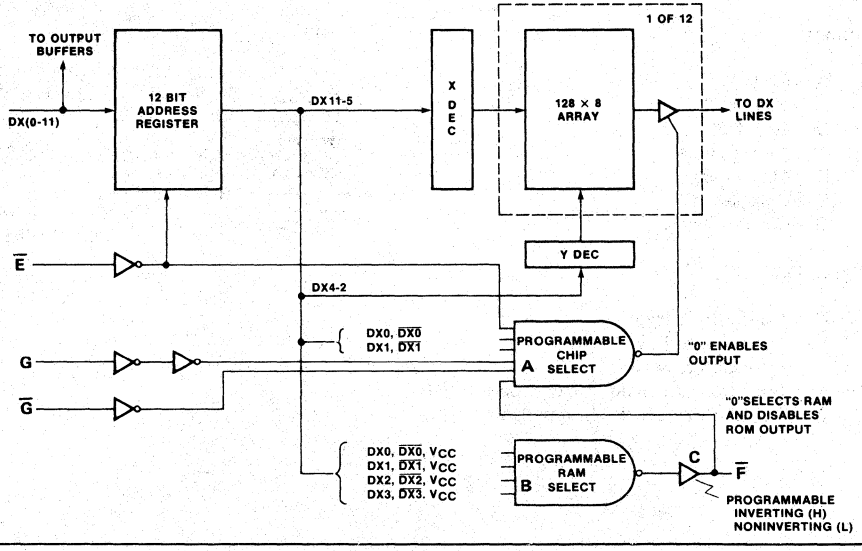
Pinout

TOP VIEW – DIP



DX - Address Input and Data Out
$\overline{E}$ - Chip Enable
G - Output Enable
$\overline{G}$ - Output Enable
$\overline{F}$ - RAM Field Select

Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+12.0V
Applied Input or Output Voltage	GND -0.3V to VCC + 0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial-9	-40°C to +85°C
Military-2	-55°C to +125°C

ELECTRICAL CHARACTERISTICS VCC = 10 ± 5%

D.C.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
VIH	Logical "1" Input Voltage	70% VCC			V	
VIL	Logical "0" Input Voltage			20% VCC	V	
IIL	Input Leakage	-1.0		+1.0	μA	0V ≤ VIN ≤ VCC
VOH	Logical "1" Output Voltage	VCC -0.1			V	IOUT = 0
VOL	Logical "0" Output Voltage			GND + .01	V	IOUT = 0
IO	Output Leakage	-1.0		1.0	μA	0V ≤ VO ≤ VCC
ICCSB	Standby Supply Current			800	μA	VIN = 0 or VCC
ICCOP	Operating Current ①			10	mA	f = 1MHz, IO = 0
CI	Input Capacitance* ②		5.0	7.0	pF	VI = VCC or GND
CIO	I/O Capacitance* ②		6.0	10.0	pF	

*Guaranteed and sampled, but not 100% tested.

3

See Switching Waveforms page 3-9

A.C.

		INDUSTRIAL		MILITARY			
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS	TEST CONDITIONS ③
TELQV	Access Time From $\overline{E}$		200		220	ns	VCC = 10 ± 5%
TGHQV	Output Enable Time		160		175	ns	
TGLQZ	Output Disable Time		160		175	ns	
TEHEL	Strobe Pos. Pulse Width	125		140		ns	
TELEL	Cycle Time	325		360		ns	
TAVEL	Address Set-Up Time	30		35		ns	
TELAX	Address Hold Time	55		60		ns	
TELFV	Propagation to $\overline{F}$		100		110	ns	

NOTES: ① Operating Supply Current (ICCOP) is proportional to operating frequency, example typical ICCOP = 10mA/MHz.
② Capacitance sampled and guaranteed – not 100% tested.
③ A.C. test conditions: Inputs – TRise = TFall = 20ns; Outputs – ITTL Load and 50pF.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8 .0V
Applied Input or Output Voltage	GND -0.3V to VCC + 0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial-9	-40°C to +85°C
Military-2	-55°C to +125°C

ELECTRICAL CHARACTERISTICS VCC = 5 ± 10%

D.C.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
VIH	Logical "1" Input Voltage	70% VCC			V	
VIL	Logical "0" Input Voltage			20% VCC	V	
IIL	Input Leakage	-1.0		+1.0	μA	0V ≤ VIN ≤ VCC
VOH	Logical "1" Output Voltage	VCC -0.1			V	IOUT = 0
VOL	Logical "0" Output Voltage			GND + .01	V	IOUT = 0
IO	Output Leakage	-1.0		1.0	μA	0V ≤ VO ≤ VCC
ICCSB	Standby Supply Current			100	μA	VI = 0 or VCC
ICCOP	Operating Current ①			5	mA	f = 1MHz, IO = 0
CI	Input Capacitance* ②		5.0	7.0	pF	VI = VCC or GND
CIO	I/O Capacitance* ②		6.0	10.0	pF	

*Guaranteed and sampled, but not 100% tested.

3

See Switching Waveforms page 3-9

A.C.

		INDUSTRIAL		MILITARY			
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS	TEST CONDITIONS ③
TELQV	Access Time From $\overline{E}$		510		560	ns	VCC = 5 ± 10%
TGHQV	Output Enable Time		290		320	ns	
TGLQZ	Output Disable Time		290		320	ns	
TEHEL	Strobe Pos. Pulse Width	260		285		ns	
TELEL	Cycle Time	770		845		ns	
TAVEL	Address Set-Up Time	75		85		ns	
TELAX	Address Hold Time	120		135		ns	
TELFV	Propagation to $\overline{F}$		220		240	ns	

NOTES: ① Operating Supply Current (ICCOP) is proportional to operating frequency, example typical ICCOP = 5mA/MHz.
② Capacitance sampled and guaranteed - not 100% tested.
③ A.C. test conditions: Inputs - TRise = TFall = 20ns; Outputs - ITTL Load and 50pF.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8 .0V
Applied Input or Output Voltage	GND -0.3V to VCC + 0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-40°C to +85°C

ELECTRICAL CHARACTERISTICS VCC = 5 ± 10%

	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
D.C.	VIH	Logical "1" Input Voltage	70% VCC			V	
	VIL	Logical "0" Input Voltage			20% VCC	V	
	IIL	Input Leakage	-10		+10	μA	0V ≤ VIN ≤ VCC
	VOH	Logical "1" Output Voltage	VCC -.01			V	IOUT = 0
	VOL	Logical "0" Output Voltage			GND + .01	V	IOUT = 0
	IO	Output Leakage	-10		+10	μA	0V ≤ VO ≤ VCC
	ICCSB	Standby Supply Current			500	μA	VI = 0 or VCC
	ICCOP	Operating Current ①			5	mA	f = 1MHz, IO = 0
	CI	Input Capacitance* ②		5.0	7.0	pF	VI = VCC or GND
	CIO	I/O Capacitance* ②		6.0	10.0	pF	

*Guaranteed and sampled, but not 100% tested.

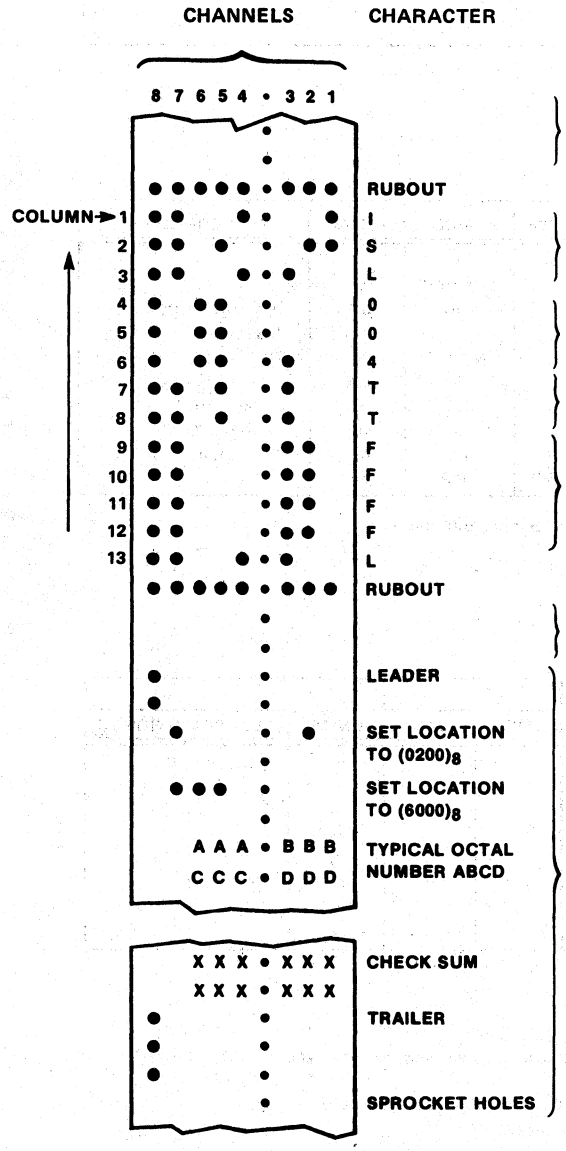
See Switching Waveforms page 3-9

		INDUSTRIAL					
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS	TEST CONDITIONS ③
TELQV	Access Time From $\overline{E}$		640			ns	VCC = 5 ± 10%
TGHQV	Output Enable Time		390			ns	
TGLQZ	Output Disable Time		390			ns	
TEHEL	Strobe Pos. Pulse Width	300				ns	
TELEL	Cycle Time	940				ns	
TAVEL	Address Set-Up Time	75				ns	
TELAX	Address Hold Time	140				ns	
TELFV	Propagation to $\overline{F}$		250			ns	

A.C.

NOTES: ① Operating Supply Current (ICCOP) is proportional to operating frequency, example typical ICCOP = 5mA/MHz.
② Capacitance sampled and guaranteed - not 100% tested.
③ A.C. test conditions: Inputs - TRise = TFall = 20ns; Outputs - ITTL Load and 50pF.

HM-6312/6312A programming information is generated from the PAL III Symbolic Assembler as a "second pass" binary tape. A separate tape is required for each 1024 word ROM pattern, i.e. a separate symbolic should be generated for each 1024 word block of memory used, (0000-1777)8, (2000-3777)8, (4000-5777)8 and (6000-7777)8. A header is added to the front of each tape giving customer ID, chip select and $\overline{F}$ programming information. The header consists of 15 ASCII characters generated from a standard teletype. Channel 8 is always punched. The header begins with a rubout followed by 6 alphanumeric characters identifying the customer and the pattern number. Next are 2 characters designating true or false for inputs DX0 and DX1 to chips select gate A (see Functional Diagram), and 4 characters designating true, false, don't care for inputs DX0, DX1, DX2 and DX3 to the RAM select gate B (see Functional Diagram). Next is one character (H or L) designating $\overline{F}$ as active high or active low. The $\overline{F}$ function is inhibited when all $\overline{F}$ inputs are VCC or don't care (V) and $\overline{F}$ is active high. The header ends with a rubout.



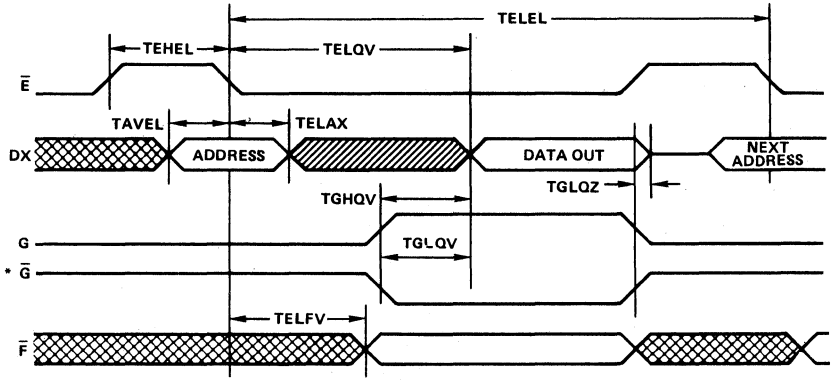
The example shown above has a customer ID and pattern ISL 004. Chip selects are programmed to recognize addresses (6000-7777)8 or (3072-4095)10. RAM select is active low for addresses (0000-0377)8 or (0000-0255)10. For programs using less than 1024 words the unused locations are automatically programmed to a logic one.

$\overline{F}$ PROGRAMMING

Defining the address block for which $\overline{F}$ is active is accomplished through programming the inputs to gate B. (See Functional Diagram). The sense of $\overline{F}$ is defined by programming gate C for inverting or noninverting. These conditions are specified in the header portion of the tape, columns 9 thru 13.

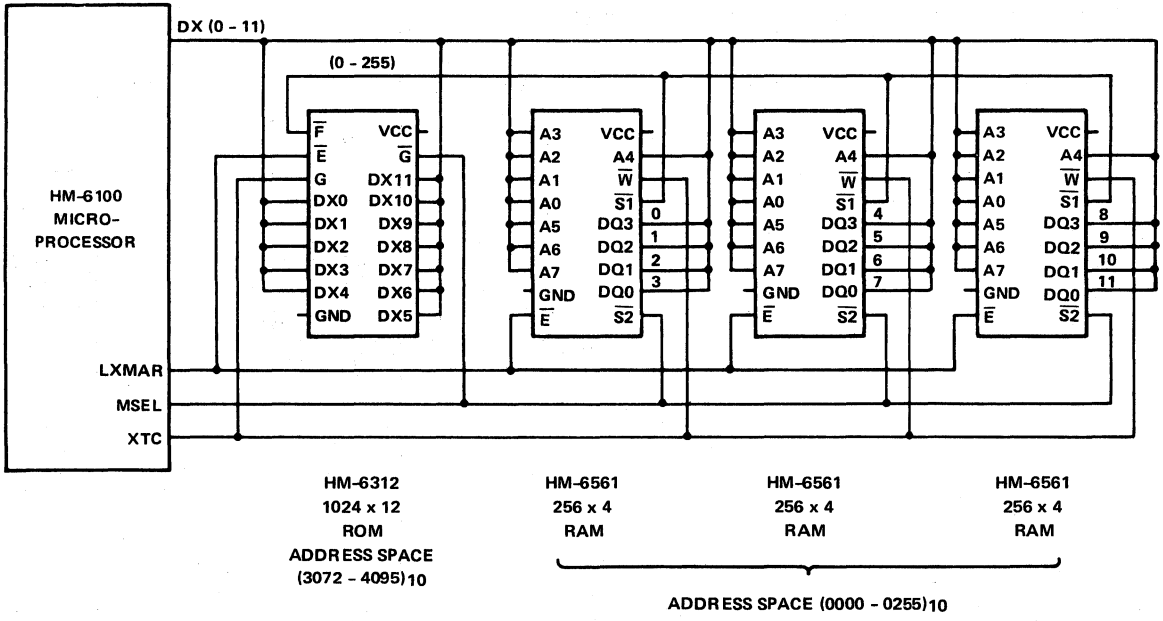
Particular care is required in specifying the sense of $\overline{F}$. Careful examination of the Functional Diagram reveals that $\overline{F}$ actually serves two functions, 1). $\overline{F}$ is anded with the inputs of gate A to enable the HM-6312 output buffers. 2). The output of $\overline{F}$ is used to select RAM or other external devices, this function is always a low true.

Switching Waveforms



* $\overline{G}$ has the same timing as G and is inverted.

A Typical Microprocessor System



HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

MARCH 1978 **Preview**

HM-6388

8192 x 8 CMOS ROM

Features

- 8K WORD BY 8 BIT MEMORY
- MASK PROGRAMMED, NON-VOLATILE
- QUICK ACCESS OVER MIL TEMP. . . . . 550nsec MAX
- LOW STANDBY CURRENT OVER MIL TEMP. . . . . 100μA MAX
- SINGLE 5V POWER SUPPLY
- ON CHIP ADDRESS REGISTERS
- COMPACT 24 PIN PACKAGE
- PINOUT LIKE HM-6389 FOR EASY UPGRADE
- TTL COMPATIBLE INPUT/OUTPUT
- MILITARY, INDUSTRIAL AND COMMERCIAL TEMPERATURE RANGES

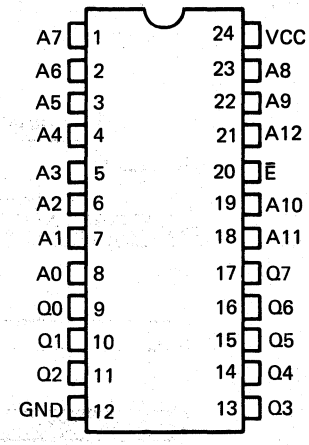
Description

The HM-6388 is a mask programmed Read Only Memory featuring quick access and extremely low power consumption. The 6388 contains internal address registers to allow simple implementation in common bus systems. Because of the similarity of pinouts a system utilizing this device can be easily modified to use the HM-6389 for added control flexibility.

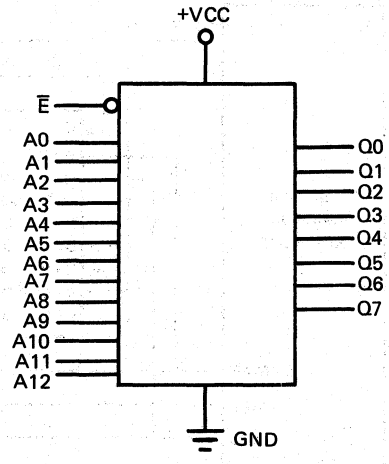
Because of the large memory matrix, 65,536 bits, this device can be used for non-volatile storage of operating systems, control stores, assemblers, compilers, loaders, editors, high accuracy look up tables, and a vast number of other unique and otherwise unsatisfied applications.

Pinout

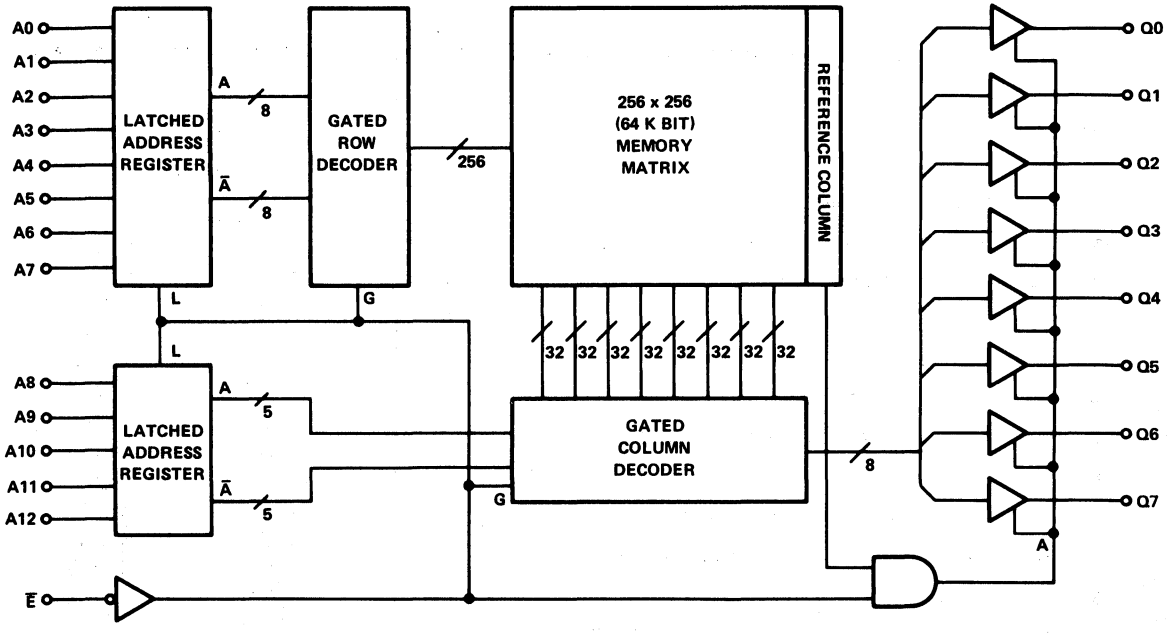
TOP VIEW



Logic Symbol



Functional Diagram



LATCHED ADDRESS REGISTER LATCH ON RISING L
GATED DECODERS GATE ON RISING G
THREE STATE DRIVERS ACTIVE WHEN A = HIGH

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-6389

8192 x 8 CMOS ROM

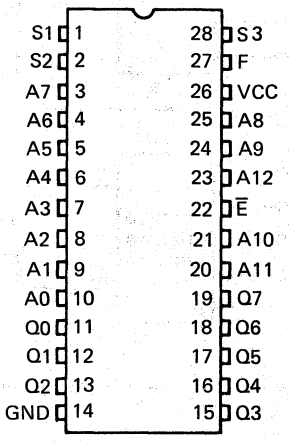
MARCH 1978 *Preview*

Features

- 8K WORD BY 8 BIT MEMORY
- MASK PROGRAMMED, NON-VOLATILE
- QUICK ACCESS OVER MIL TEMP. . . . . 550nsec MAX
- LOW STANDBY CURRENT OVER MIL TEMP. . . . . 100μA MAX
- SINGLE 5V POWER SUPPLY
- ON CHIP ADDRESS REGISTERS
- INTERNAL PLA FOR RAM FIELD SELECT OUTPUT
- CHIP SELECT POLARITY OPTIONS
- CHIP SELECT LATCHED/UNLATCHED OPTIONS
- DATA OUTPUT LATCHED/NONLATCHED OPTIONS
- TTL COMPATIBLE INPUT/OUTPUT
- MILITARY, INDUSTRIAL AND COMMERCIAL TEMP. RANGES

Pinout

TOP VIEW



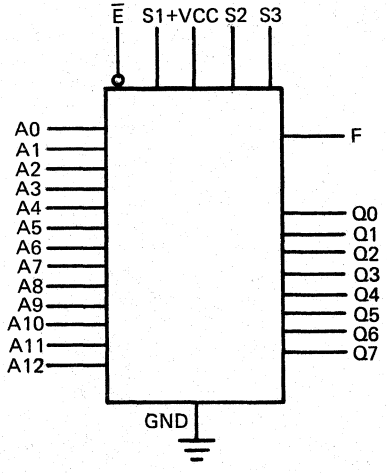
Description

The HM-6389 is a mask programmed Read Only Memory featuring quick access and extremely low power consumption. The HM-6389 contains internal address registers for ease of use in common bus systems. In addition to the 65,536 bit (6K) user defined memory matrix, there are a variety of user defined control options.

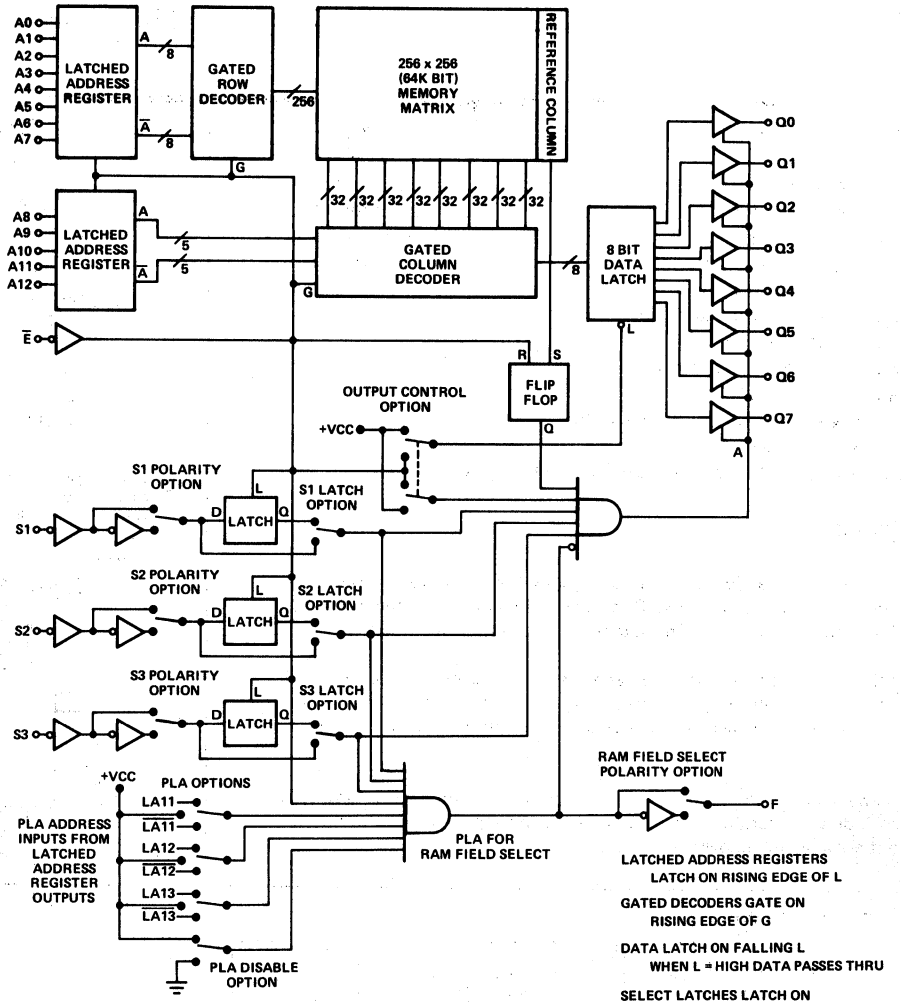
These options include a Programmable Logic Array (PLA) for RAM field select allowing internal address decoding for RAM over ROM overlay memory array applications. The polarity of the RAM Field Select output is also an user option. The chip select inputs are individually definable to be active high or low, and to be latched by chip enable or nonlatched. This feature can be used to eleminate address decoding for arrays as large as 64K words. Another user defined option determines whether the data outputs will be latched by the chip enable ($\overline{E}$), or is nonlatched mode is chosen, the chip enable signal is used to disable the three state output drivers.

Because of the large data storage matrix and the versatility of the control options, this device can be used for non-volitile storage of operating systems, assemblers, compilers, loaders, editors, high accuracy look up tables, and a wide variety of otherwise unsatisfied applications.

Logic Symbol



Functional Diagram



LATCHED ADDRESS REGISTERS LATCH ON RISING EDGE OF L

GATED DECODERS GATE ON RISING EDGE OF G

DATA LATCH ON FALLING L WHEN L = HIGH DATA PASSES THRU

SELECT LATCHES LATCH ON RISING EDGE OF L

THREE STATE OUTPUTS ACTIVE IF A = HIGH

ALL SWITCHES ILLUSTRATE USER DEFINED MASK PROGRAMMED OPTIONS. ONCE MANUFACTURED ALL OPTIONS ARE INTERNALLY FIXED AND CAN NOT BE CHANGED.

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-6501

256 x 4 CMOS RAM

JULY 1978

Features

- LOW STANDBY POWER . . . . . 55μW MAX
- LOW OPERATING POWER . . . . . 22mW/MHz MAX
- FAST ACCESS TIME . . . . . 220nsec MAX
- DATA RETENTION VOLTAGE . . . . . 2.0 VOLTS MIN.
- TTL COMPATIBLE IN/OUT
- HIGH OUTPUT DRIVE - 2 TTL LOADS
- HIGH NOISE IMMUNITY
- ON CHIP ADDRESS REGISTERS
- THREE STATE OUTPUTS
- EASY MICROPROCESSOR INTERFACING
- LATCHED OUTPUTS
- MILITARY AND INDUSTRIAL TEMPERATURE RANGES

Description

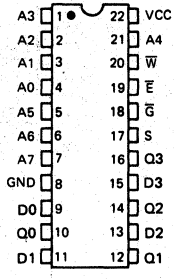
The HM-6501 is a 256 by 4 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

On chip latches are provided for address and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

The HM-6501 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

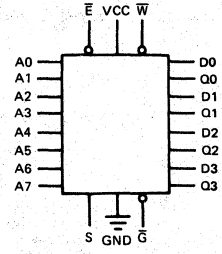
Pinout

TOP VIEW

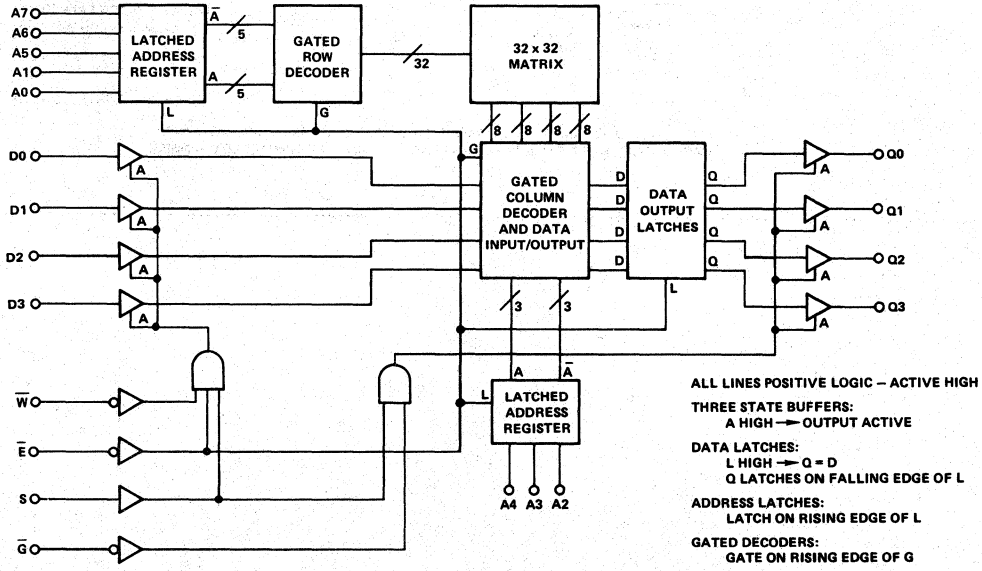


A - ADDRESS INPUT
E - CHIP ENABLE
W - WRITE ENABLE
G - OUTPUT ENABLE
S - CHIP SELECT
D - DATA INPUT
Q - DATA OUTPUT

Logic Symbol



Functional Diagram



ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage -VCC	+8.0V	Operating Supply Voltage -VCC	
Applied Input or Output Voltage	GND -0.3V VCC +0.3V	Military (-2)	4.5V to 5.5V
		Industrial (-9)	4.5V to 5.5V
Storage Temperature	-65°C to +150°C	Operating Temperature	
		Military (-2)	-55°C to +125°C
		Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MIN	TEMP. = 25°C ① VCC = 5.0V TYP	TEMP. = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		10 1(+25°C)		0.1	1	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4		1.5	2.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		10		0.01	1	μA	VCC = 3.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		2.0	1.4		V	
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 3.2mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -0.4mA
	CI	Input Capacitance ③		6		4	6	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10		6	10	pF	VO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		220		120	170	ns	④
	TAVQV	Address Access Time		220		110	170	ns	④
	TSHQX	Chip Select Output Enable Time		130		50	90	ns	④
	TGLQX	Output Enable Output Enable Time		130		50	90	ns	④
	TSLQZ	Chip Select Output Disable Time		130		50	90	ns	④
	TGHQZ	Output Enable Output Disable Time		130		50	90	ns	④
	TELEH	Chip Enable Pulse Negative Width	220		170	120		ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		70	50		ns	④
	TAVEL	Address Setup Time	0		0	-10		ns	④
	TELAX	Address Hold Time	40		30	20		ns	④
	TDVWH	Data Setup Time	100		80	50		ns	④
	TWHDX	Data Hold Time	0		0	-10		ns	④
	TWLSL	Chip Select Write Pulse Setup Time	120		100	60		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	120		100	60		ns	④
	TSHWH	Chip Select Write Pulse Hold Time	120		100	60		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	120		100	60		ns	④
	TWLWH	Write Enable Pulse Width	120		100	60		ns	④
	TELEL	Read or Write Cycle Time	320		240	170		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — 1 TTL load and 50pF. All timing measurements at 1/2 VCC.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage -VCC	+8.0V
Applied Input or Output Voltage	GND -0.3V VCC +0.3V
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage -VCC	
Military (-2)	4.5V to 5.5V
Industrial (-9)	4.5V to 5.5V
Operating Temperature	
Military (-2)	-55°C to +125°C
Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MIN	TEMP. = 25°C ① VCC = 5.0V TYP	TEMP. = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		10 1(+25°C)		1.0	1	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4		1.5	2.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		10		0.1	1	μA	VCC = 3.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		2.0	1.4		V	
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 3.2mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -0.4mA
	CI	Input Capacitance ③		6		4	6	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10		6	10	pF	VO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		300		160	240	ns	④
	TAVQV	Address Access Time		300		150	240	ns	④
	TSHQX	Chip Select Output Enable Time		150		60	120	ns	④
	TGLQX	Output Enable Output Enable Time		150		60	120	ns	④
	TSLQZ	Chip Select Output Disable Time		150		60	120	ns	④
	TGHQZ	Output Enable Output Disable Time		150		60	120	ns	④
	TELEH	Chip Enable Pulse Negative Width	300		240	160		ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		70	50		ns	④
	TAVEL	Address Setup Time	0		0	-10		ns	④
	TELAX	Address Hold Time	50		40	30		ns	④
	TDVWH	Data Setup Time	150		120	100		ns	④
	TWHDX	Data Hold Time	0		0	-10		ns	④
	TWLSL	Chip Select Write Pulse Setup Time	180		150	120		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	180		150	120		ns	④
	TSHWH	Chip Select Write Pulse Hold Time	180		150	120		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	180		150	120		ns	④
	TWLWH	Write Enable Pulse Width	180		150	120		ns	④
	TELEL	Read or Write Cycle Time	400		310	210		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — 1 TTL load and 50pF. All timing measurements at 1/2 VCC.

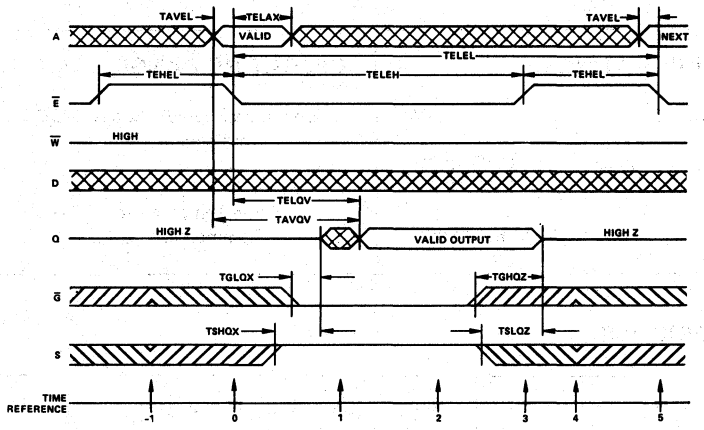
ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage -VCC	+8.0V	Operating Supply Voltage -VCC Commercial	4.75V to 5.25V
Applied Input or Output Voltage	GND -0.3V VCC +0.3V	Operating Temperature Commercial	0°C to 75°C
Storage Temperature	-65°C to +150°C		

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MIN	TEMP. = 25°C ① VCC = 5.0V TYP	TEMP. = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		100		10	100	µA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4		1.5	2.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		2.0			V	
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	µA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	µA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 1.6mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -0.2mA
	CI	Input Capacitance ③		6		4	6	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10		6	10	pF	VO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		350		200	300	ns	④
	TAVQV	Address Access Time		360		200	310	ns	④
	TSHQX	Chip Select Output Enable Time		180		80	160	ns	④
	TGLQX	Output Enable Output Enable Time		180		80	160	ns	④
	TSLQZ	Chip Select Output Disable Time		180		80	160	ns	④
	TGHQZ	Output Enable Output Disable Time		180		80	160	ns	④
	TELEH	Chip Enable Pulse Negative Width	350		300	200		ns	④
	TEHEL	Chip Enable Pulse Positive Width	150		130	90		ns	④
	TAVEL	Address Setup Time	10		10	0		ns	④
	TELAX	Address Hold Time	70		50	40		ns	④
	TDVWH	Data Setup Time	170		140	120		ns	④
	TWHDX	Data Hold Time	0		0	-10		ns	④
	TWLSL	Chip Select Write Pulse Setup Time	210		170	150		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	210		170	150		ns	④
	TSHWH	Chip Select Write Pulse Hold Time	210		170	150		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	210		170	150		ns	④
	TWLWH	Write Enable Pulse Width	210		170	150		ns	④
	TELEL	Read or Write Cycle Time	500		430	290		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — 1 TTL load and 50pF. All timing measurements at 1/2 VCC.

Read Cycle



TRUTH TABLE

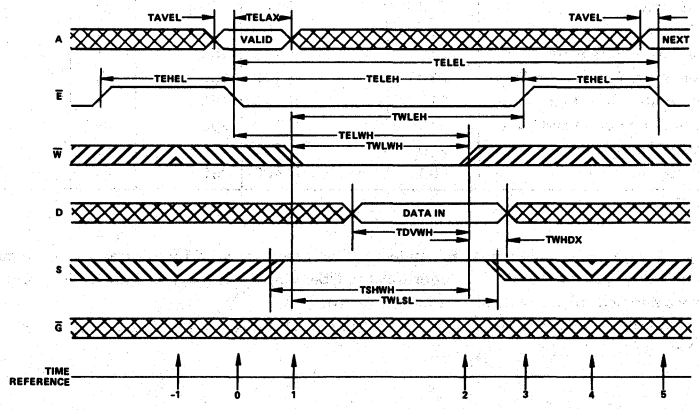
TIME REFERENCE	INPUTS Ē	S	Ḡ	W̄	A	D	OUTPUT Q	FUNCTION
-1	H	L	H	X	X	X	Z	MEMORY DISABLED
0	↘	L	H	H	V	X	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	L	H	X	X	X	OUTPUT ENABLED
2	L	H	L	H	X	X	V	OUTPUT VALID
3	↗	H	L	H	X	X	V	OUTPUT LATCHED
4	H	L	H	X	X	X	Z	DEVICE DISABLED, PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	L	H	H	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The read cycle is initiated by the falling edge of $\overline{E}$. This signal latches the input address word into on chip registers providing that minimum address setup and hold times are met. After the required hold time, the address inputs may change state without affecting device operation. For the output to be read, $\overline{G}$ and $\overline{E}$ must be low; $\overline{W}$ and S must be high. The output data will be valid at accesss time (TELQV) or at one output enable time (TSHQX or TGLQX), whichever is the latter occuring signal.

S and $\overline{G}$ are complementary signals which simplify the external logic required for decoding in expanded memory arrays. Either or both of these signals may be used to disable the outputs when or-tying several memories in an array. The HM-6501 has output data latches that are controlled by $\overline{E}$.

When $\overline{E}$ goes high the outputs are latched to contain the present data. The output buffers can be forced to a high impedance state by either $\overline{G}$ or S but the latches will only unlatch on the falling edge of $\overline{E}$.

Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	S	$\overline{G}$	$\overline{W}$	A	D	OUTPUT Q	FUNCTION
-1	H	L	X	X	X	X	SEE NOTE	MEMORY DISABLED
0	↘	X	X	X	V	X		CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	X	↘	X	X		WRITE PERIOD BEGINS
2	L	H	X	↗	X	V		DATA IN IS WRITTEN
3	↗	X	X	H	X	X		WRITE IS COMPLETED
4	H	L	X	X	X	X		PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	X	X	X	V	X		CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

NOTE: IF $\overline{G}$ IS HIGH, THE OUTPUT WILL BE HIGH IMPEDANCE.
IF $\overline{G}$ IS LOW, THE INPUT DATA WILL PROPAGATE TO THE OUTPUT.

As in the read mode, the write cycle is initiated by the falling edge of $\overline{E}$ which latches the addresses. The write portion of the cycle is defined as $\overline{E}$ and $\overline{W}$ being low simultaneously with S high. If the inputs and outputs are tied together, $\overline{G}$ must be high. The write portion of the cycle is terminated on the first rising edge of $\overline{E}$, $\overline{W}$, or the falling edge of S. Data setup and hold times must be referenced to the terminating signal.

If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may remain low until all desired locations have been written. When this method is used, data setup and hold times must be referenced to the rising edge of $\overline{E}$ or to the falling edge of S, whichever occurs first. By positioning the $\overline{W}$ pulse at different times within the $\overline{E}$ low time (TELEH) various types of write cycles may be performed.

If the $\overline{E}$ low time (TELEH) is greater than the $\overline{W}$ pulse (TWLWH) plus an output enable time (TSHQX or TGLQX) a combination read-write cycle is executed. Data may be modified an indefinite number of times during any write cycle (TELEH).

The data inputs and data outputs may be tied together for use with a common I/O bus structure is the system control line $\overline{G}$ ($\overline{G}$ NOT) is NAND-ed with $\overline{W}$ to produce the device $\overline{G}$ signal. This will force the output buffers to a high impedance state during write operations so input data can be applied to the bus. A minimum delay of one output disable time must be allowed before applying input data to the bus. This will insure that the output buffers are not active.

Battery Backup Applications

The HM-6501 is especially well suited for use in battery backup systems. Data retention supply voltage and supply current are guaranteed over the full temperature range.

When designing the backup system, the following suggestions should be considered:

1.) As RAM VCC drops, the input logical one voltages should follow so as not to exceed VCC +0.3. It is suggested to use CMOS drivers, operating at CMOS VCC, such as the HD-6495, HD-6432, and HD-6433. Anther approach is the use of open collector or open drain buffers pulled up to CMOS VCC.

2.) $\overline{E}$ must be held high at CMOS VCC and S must be held low at ground. $\overline{W}$, $\overline{G}$, address, and data inputs should be held at GND or CMOS VCC.

3.) When exiting from the battery backup mode, VCC should ramp without ring or discontinuities.

4.) The RAM can begin operation one TEHEL after VCC reaches the minimum operating voltage (4.5 or 4.75V).

A very simple battery backup system is shown in Figure 1. When system power is available, diode D1 is forward biased and supplies current to the CMOS devices. Upon loss of system power, diode D1 is reverse biased and only CMOS devices are consuming battery power. A disadvantage to this method is that CMOS VCC is one diode drop, .7V, below TTL VCC. There is a possibility that a TTL output signal could rise higher than CMOS VCC and cause possible latch problems. This possibility can be reduced by incorporating a system similar to that shown in Figure 2. Other alternatives include using a germanuin diode yielding a VF $\approx$ .2V or adding diode D2 in the TTL supply and raising VCC to account for the drop. A PNP transistor is substituted for the diode in Figure 2. The saturation drop of the transistor, 0.2V, is less than the 0.7V drop of the diode giving more margin against latch-up. A power fail output signal is available to disable the chip enable circuitry. Open collector TTL with pullups to CMOS VCC or LS type TTL should be used as memory drivers. This will insure that the CMOS inputs are not floating during the backup period. When system power is restored, operation continues as normal and the NI-CAD battery pack is trickle charged through RC.

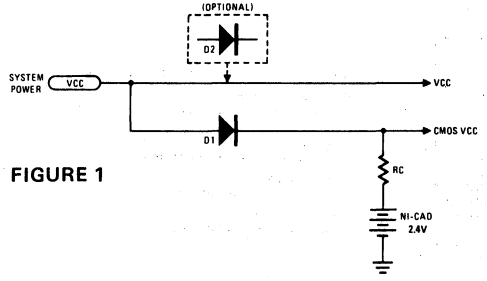


FIGURE 1

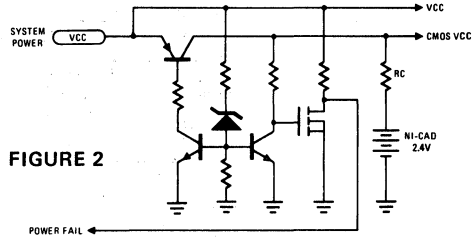


FIGURE 2

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-6503
2048 x 1 CMOS RAM

JULY 1978

Features

- LOW POWER STANDBY . . . . . ≪1mW MAX.
- LOW POWER OPERATION. . . . . 35mW/MHz MAX.
- EXTREMELY LOW SPEED POWER PRODUCT
- DATA RETENTION . . . . . @ 2.0V MIN.
- TTL COMPATIBILITY INPUT/OUTPUT
- THREE STATE OUTPUT
- FAST ACCESS TIME . . . . . 300nsec MAX.
- INDUSTRIAL OR COMMERCIAL TEMPERATURE RANGE
- 18 PIN PACKAGE FOR HIGH DENSITY
- ON CHIP ADDRESS REGISTER
- PINOUT ALLOWS UPGRADE TO 6504

Description

The HM-6503 is a 2048 x 1 static CMOS RAM fabricated using self aligned silicon gate technology. The device utilizes synchronous circuitry to achieve high performance and low power operation.

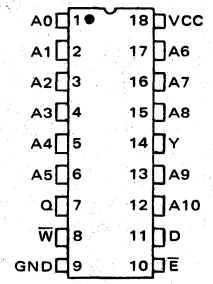
On chip latches are provided for addresses, data input and data output allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance for use in expanded memory arrays.

The HM-6503 is a truly static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

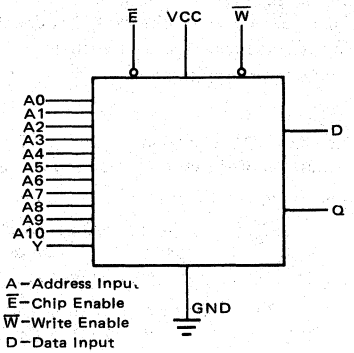
The HM-6503 is supplied in two versions, the HM-6503H and the HM-6503L. The H or L is used to designate the logic level to be connected to the Y input. If a HM-6503H is procured the user must connect the Y input to VCC in the system. If a HM-6503L is used the Y input must be connected to system ground.

Pinout

TOP VIEW

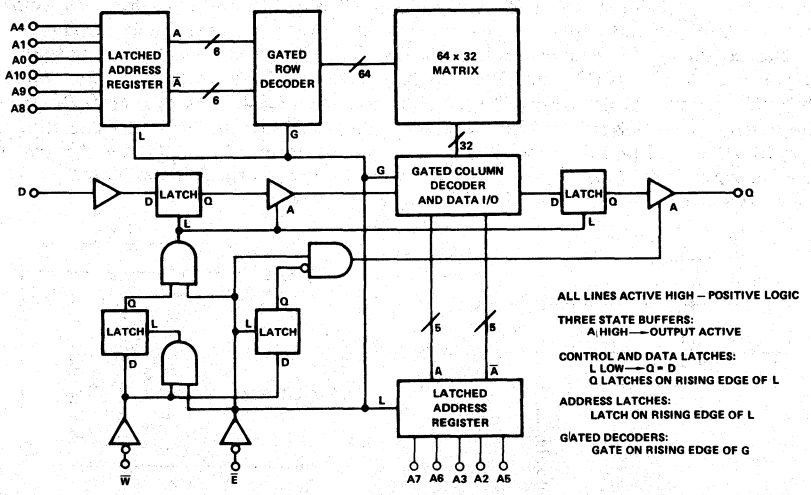


Logic Symbol



A–Address Input
E–Chip Enable
W–Write Enable
D–Data Input
Q–Data Output
Y–Hard Wired Input

Functional Diagram



ALL LINES ACTIVE HIGH – POSITIVE LOGIC

THREE STATE BUFFERS:
A HIGH—OUTPUT ACTIVE

CONTROL AND DATA LATCHES:
L LOW—Q = D
Q LATCHES ON RISING EDGE OF L

ADDRESS LATCHES:
LATCH ON RISING EDGE OF L

GATED DECODERS:
GATE ON RISING EDGE OF G

ABSOLUTE MAXIMUM RATINGS

Supply Voltage – VCC	+8.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage	
Industrial (-9)	4.5V to 5.5V
Operating Temperature	
Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

			TEMP. & VCC = OPERATING RANGE		TEMP = 25°C ① VCC = 5.0V				
	SYMBOL	PARAMETER	MIN	MAX	MIN	TYP	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		50		0.1	10	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		7		5	6	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		25		0.01	5	μA	IO = 0 VCC = 3.0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		2.0	1.4		V	
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND≤VI≤VCC
	IOZ	Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND≤VO≤VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.25	0.35	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		3.5	4.0		V	IO = -1.0mA
	CI	Input Capacitance ③		8.0		5.0	8.0	pF	f = 1MHz VI = VCC or GND
	CO	Output Capacitance ③		10.0		6.0	10.0	pF	f = 1MHz VO=VCC or GND
A.C.	TELQV	Chip Enable Access Time		300		170	250	ns	④
	TAVQV	Address Access Time		320		170	270	ns	④
	TELQX	Chip Enable Output Enable Time		100		50	80	ns	④
	TEHQZ	Chip Enable Output Disable Time		100		50	80	ns	④
	TELEH	Chip Enable Pulse Negative Width	300		250	170		ns	④
	TEHEL	Chip Enable Pulse Positive Width	120		100	70		ns	④
	TAVEL	Address Setup Time	20		20	0		ns	④
	TELAX	Address Hold Time	50		50	20		ns	④
	TWLWH	Write Enable Pulse Width	80		60	40		ns	④
	TWLEH	Write Enable Pulse Setup Time	200		150	130		ns	④
	TWLEL	Early Write Pulse Setup Time	0		0	-10		ns	④
	TWHEL	Write Enable Read Mode Setup Time	0		0	-10		ns	④
	TELWH	Early Write Pulse Hold Time	80		60	40		ns	④
	TDVWL	Data Setup Time	0		0	-10		ns	④
	TDVEL	Early Write Data Setup Time	0		0	-10		ns	④
	TWLDX	Data Hold Time	80		60	40		ns	④
	TELDX	Early Write Data Hold Time	80		60	40		ns	④
	TELWL	Early Write Output Hi-Z Time	0		0	-10		ns	④
	TQVWL	Data Valid to Write Time	0		0	0		ns	④
	TELEL	Read or Write Cycle Time	420		350	240		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
3. Capacitance sampled and guaranteed – not 100% tested.
4. AC test conditions: Inputs – TRISE = TFALL = 20nsec; Output – 1 TTL load and 50pF; All timing measured at ½ VCC.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage – VCC	+8.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage Commercial	4.75V to 5.25V
Operating Temperature Commercial	0°C to +75°C

ELECTRICAL CHARACTERISTICS

			TEMP. & VCC = OPERATING RANGE		TEMP = 25°C① VCC = 5.0V				
	SYMBOL	PARAMETER	MIN	MAX	MIN	TYP	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		500		100	500	µA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		7.		5	6	mA	f = 1MHz, IO = 0 VI = VCC or GND
	II	Input Leakage Current	-10.0	+10.0	-7.0	±0.5	+7.0	µA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-10.0	+10.0	-7.0	±0.5	+7.0	µA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.25	0.35	V	IO = 1.6mA
	VOH	Output High Voltage	2.4		3.5	4.0		V	IO = -0.4mA
	CI	Input Capacitance ③		8.0		5.0	8.0	pF	f = 1MHz VI = VCC or GND
	CO	Output Capacitance ③		10.0		6.0	10.0	pF	f = 1MHz VO = VCC or GND
A.C.	TELQV	Chip Enable Access Time		350		200	300	ns	④
	TAVQV	Address Access Time		370		200	320	ns	④
	TELQX	Chip Enable Output Enable Time		100		50	80	ns	④
	TEHQZ	Chip Enable Output Disable Time		100		50	80	ns	④
	TELEH	Chip Enable Pulse Negative Width	350		300	200		ns	④
	TEHEL	Chip Enable Pulse Positive Width	150		120	100		ns	④
	TAVEL	Address Setup Time	20		20	0		ns	④
	TELAX	Address Hold Time	50		50	20		ns	④
	TWLWH	Write Enable Pulse Width	100		80	60		ns	④
	TWLEH	Write Enable Pulse Setup Time	250		200	100		ns	④
	TWLEL	Early Write Pulse Setup Time	0		0	-10		ns	④
	TWHEL	Write Enable Read Setup Time	0		0	-10		ns	④
	TELWH	Early Write Pulse Hold Time	100		80	60		ns	④
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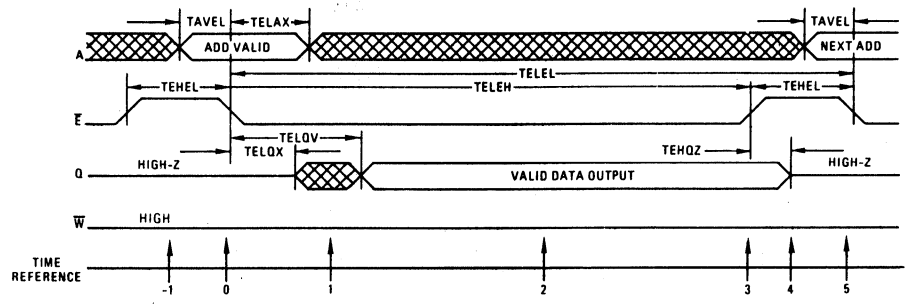
	TDVEL	Early Write Data Setup Time	30		20	0		ns	④
	TWLDX	Data Hold Time	100		80	60		ns	④
	TELDX	Early Write Data Hold Time	100		80	80		ns	④
	TELWL	Early Write Output Hi-Z Time	0		0	-10		ns	④
	TQVWL	Data Valid to Write Time	0		0	0		ns	④
	TELEL	Read or Write Cycle Time	500		420	300		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
3. Capacitance sampled and guaranteed – not 100% tested.
4. AC test conditions: Inputs – TRISE = TFALL = 20nsec; Output – 1 TTL load and 50pF; All timing measured at ½ VCC.

Read Cycle

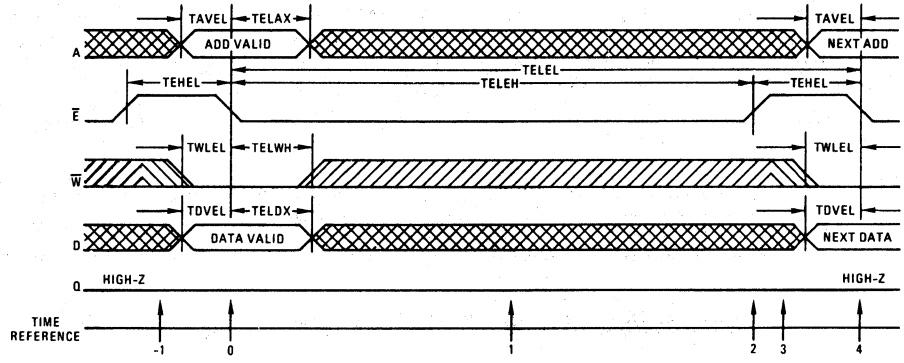


TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	OUTPUT Q	FUNCTION
-1	H	X	X	Z	MEMORY DISABLED
0	↘	H	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	X	X	OUTPUT ENABLED
2	L	H	X	V	OUTPUT VALID
3	↗	H	X	V	READ ACCOMPLISHED
4	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The address information is latched in the on chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address set up and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1) the output becomes enabled but data is not valid until during time (T = 2). $\overline{W}$ must remain high until after time (T = 2). After the output data has been read, $\overline{E}$ may return high (T = 3). This will disable the output buffer and ready the RAM for the next memory cycle (T = 4).

Early Write Cycle

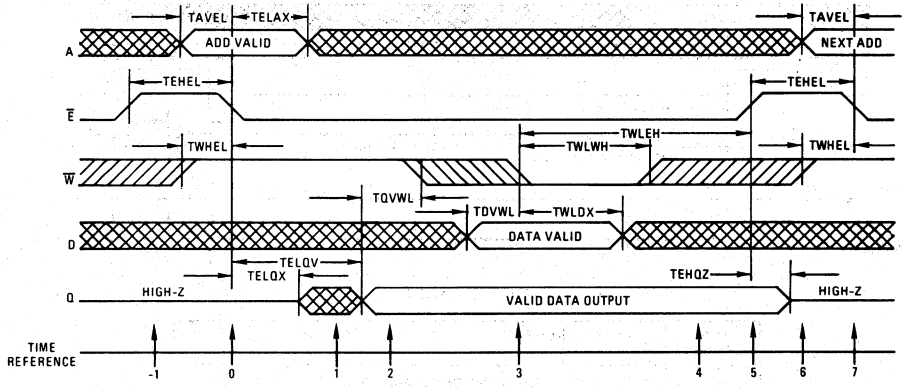


TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	D	OUTPUT Q	FUNCTION
-1	H	X	X	X	Z	MEMORY DISABLED
0	↘	L	V	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	X	X	X	Z	WRITE IN PROGRESS INTERNALLY
2	↗	X	X	X	Z	WRITE COMPLETED
3	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
4	↘	L	V	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The early write cycle is the only cycle where the output is guaranteed not to become active. On the falling edge of $\overline{E}$ (T = 0), the addresses, the write signal, and the data input are latched in on chip registers. The logic value of $\overline{W}$ at the time $\overline{E}$ falls determines the state of the output buffer for that cycle. Since $\overline{W}$ is low in the early write cycle the output buffer is latched into the high impedance state and will remain in that state until $\overline{E}$ returns high (T = 2). For this cycle, the data input is latched by $\overline{E}$ going low; therefore data set up and hold times should be referenced to $\overline{E}$. When $\overline{E}$ (T = 2) returns to the high state the output buffer disables and all signals are unlatched. The device is now ready for the next cycle.

Read Modify Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS Ē	W̄	A	D	OUTPUT Q	FUNCTION
-1	H	X	X	X	Z	MEMORY DISABLED
0	↘	H	V	X	Z	CYCLE BEGINS, ADDRESS ARE LATCHED
1	L	H	X	X	X	OUTPUT ENABLED
2	L	H	X	X	V	OUTPUT VALID, READ AND MODIFY TIME
3	L	↘	X	V	V	WRITE BEGINS, DATA IS LATCHED
4	L	X	X	X	V	WRITE IN PROGRESS INTERNALLY
5	↗	X	X	X	V	WRITE COMPLETED
6	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
7	↘	H	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

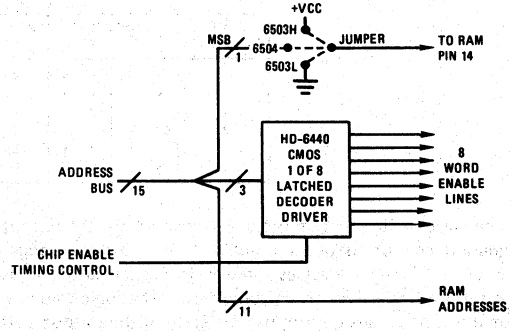
The read modify write cycle begins as all other cycles on the falling edge of $\overline{E}$ (T = 0). The $\overline{W}$ line should be high at (T = 0) in order to latch the output buffers in the active state. During (T = 1) the output will be active but not valid until (T = 2). On the falling edge of the $\overline{W}$ (T = 3) the data present at the output and input are latched. The $\overline{W}$ signal also latches itself on its low going edge. All input signals excluding $\overline{E}$ have been latched and have no further effect on the RAM. The rising edge of $\overline{E}$ (T = 5) completes the write portion of the cycle and unlatches all inputs and the output. The output goes to a high impedance and the RAM is ready for the next cycle.

NOTES:

In the above descriptions the numbers in parenthesis (T = X) refer to the respective timing diagrams. The numbers are located on the time reference line below each diagram. The timing diagrams shown are only examples and are not the only valid method of operation.

Suggestions For 6503 Memory Array Design

The HM-6503 is a device that can be used to good advantage in systems which are offered with choices of memory array size. With one common memory board layout the designer can easily offer two different array sizes. This is accomplished by using the conveniently similiar pinouts of the HM-6503 (2K by 1) and the HM-6504 (4K by 1). For example, a 16K word by 8 bit array using HM-6503s and a 32K word by 8 bit array using HM-6504s can be easily implemented on the same printed circuit card. The circuit diagram suggests one implementation requiring only one jumper wire for 16K or 32K word selection. This single jumper wire also allows the 16K array to utilize the HM-6503H or the HM-6503L version.



Battery Backup Applications

The HM-6503 is especially well suited for use in battery backup systems. Data retention supply voltage and supply current are guaranteed over the full temperature range.

When designing the backup system, the following suggestions should be considered:

1.) As RAM VCC drops, the input logical one voltages should follow so as not to exceed VCC +0.3. It is suggested to use CMOS drivers, operating at CMOS VCC, such as the HD-6495, HD-6432, and HD-6433. Another approach is the use of open collector or open drain buffers pulled up to CMOS VCC.

2.) $\overline{E}$ must be held high at CMOS VCC. $\overline{W}$, address and data inputs should be held at either GND or CMOS VCC to minimize power dissipation.

3.) When exiting from the battery backup mode, VCC should ramp without ring or discontinuities.

4.) The RAM can begin operation one TEHEL after VCC reaches the minimum operating voltage (4.5 or 4.75 volts).

A very simple battery backup system is shown in Figure 1. When system power is available, diode D1 is forward biased and supplies current to the CMOS devices. Upon loss of system power, diode D1 is reverse biased and only CMOS devices are consuming battery power. A disadvantage to this method is that CMOS VCC is one diode drop, .7V, below TTL VCC. There is a possibility that a TTL output signal could rise higher than CMOS VCC and cause possible latch problems. This possibility can be reduced by incorporating a system similar to that shown in Figure 2. Other alternatives include using a germanuin diode yielding a VF $\approx$.2V or adding diode D2 in the TTL supply and raising VCC to account for the drop. A PNP transistor is substituted for the diode in Figure 2. The saturation drop of the transistor, 0.2V, is less than the 0.7V drop of the diode giving more margin against latch-up. A power fail output signal is available to disable the $\overline{E}$ circuitry. Open collector TTL with pullups to CMOS VCC or LS type TTL should be used as memory drivers. This will insure that the CMOS inputs are not floating during the backup period. When system power is restored, operation continues as normal and the NI-CAD battery pack is trickle charged through RC.

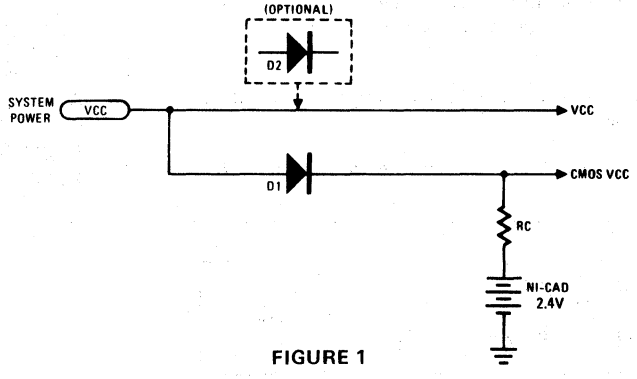


FIGURE 1

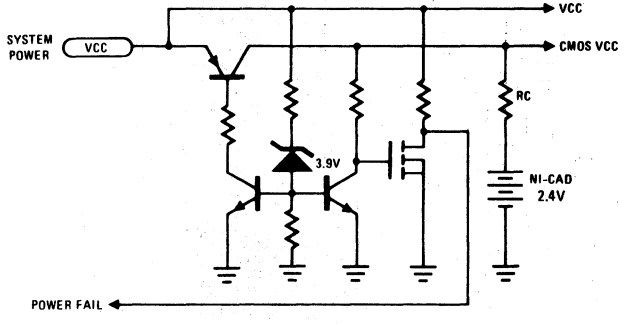


FIGURE 2

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-6504

4096 x 1 CMOS RAM

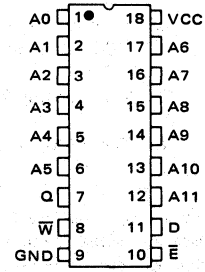
JULY 1978

Features

- LOW POWER STANDBY . . . . . ≪ 1mW MAX.
- LOW POWER OPERATION . . . . . 35mW/MHz MAX.
- EXTREMELY LOW SPEED POWER PRODUCT
- DATA RETENTION . . . . . @ 2.0V MIN.
- TTL COMPATIBLE INPUT/OUTPUT
- THREE-STATE OUTPUT
- STANDARD JEDEC PINOUT
- FAST ACCESS TIME . . . . . 300nsec MAX.
- MILITARY TEMPERATURE RANGE
- INDUSTRIAL TEMPERATURE RANGE
- 18 PIN PACKAGE FOR HIGH DENSITY
- ON CHIP ADDRESS REGISTER

Pinout

TOP VIEW



Description

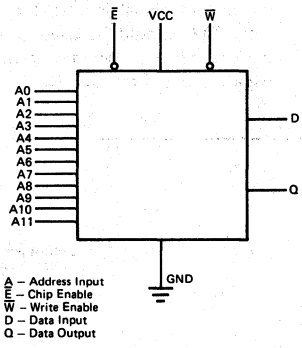
The HM-6504 is a 4096 x 1 static CMOS RAM fabricated using self aligned silicon gate technology. The device utilizes synchronous circuitry to achieve high performance and low power operation.

On chip latches are provided for addresses, data input and data output allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance for use in expanded memory arrays.

The HM-6504 is a truly static RAM and may be maintained in any state for an indefinite period of time.

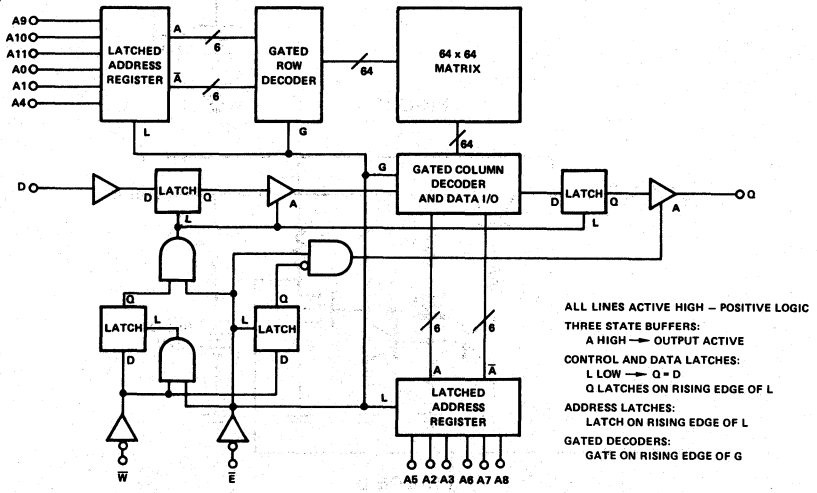
Data retention supply voltage and supply current are guaranteed over temperature.

Logic Symbol



A – Address Input
E – Chip Enable
W – Write Enable
D – Data Input
Q – Data Output

Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Supply Voltage – VCC	+8.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage	
Military (-2)	4.5V to 5.5V
Industrial (-9)	4.5V to 5.5V
Operating Temperature	
Military (-2)	-55°C to +125°C
Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP = 25°C ① VCC = 5.0V MIN	TEMP = 25°C ① VCC = 5.0V TYP	TEMP = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		50		0.1	10	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		7		5	6	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		25		0.01	5	μA	IO = 0 VCC = 3.0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		2.0	1.4		V	
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND≤VI≤VCC
	IOZ	Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND≤VO≤VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.25	0.35	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		3.5	4.0		V	IO = -1.0mA
	CI	Input Capacitance ③		8.0		5.0	8.0	pF	f = 1MHz VI = VCC or GND
	CO	Output Capacitance ③		10.0		6.0	10.0	pF	f = 1MHz VO = VCC or GND
A.C.	TELQV	Chip Enable Access Time		300		170	250	ns	④
	TAVQV	Address Access Time		320		170	270	ns	④
	TELQX	Chip Enable Output Enable Time		100		50	80	ns	④
	TEHQZ	Chip Enable Output Disable Time		100		50	80	ns	④
	TELEH	Chip Enable Pulse Negative Width	300		250	170		ns	④
	TEHEL	Chip Enable Pulse Positive Width	120		100	70		ns	④
	TAVEL	Address Setup Time	20		20	0		ns	④
	TELAX	Address Hold Time	50		50	20		ns	④
	TWLWH	Write Enable Pulse Width	80		60	40		ns	④
	TWLEH	Write Enable Pulse Setup Time	200		150	130		ns	④
	TWLEL	Early Write Pulse Setup Time	0		0	-10		ns	④
	TWHEL	Write Enable Read Mode Setup Time	0		0	-10		ns	④
	TELWH	Early Write Pulse Hold Time	80		60	40		ns	④
	TDVWL	Data Setup Time	0		0	0		ns	④
	TDVEL	Early Write Data Setup Time	0		0	0		ns	④
	TWLDX	Data Hold Time	80		60	40		ns	④
	TELDX	Early Write Data Hold Time	80		60	40		ns	④
	TELWL	Early Write Output Hi-Z Time	0		0	-10		ns	④
	TQVWL	Data Valid to Write Time	0		0	0		ns	④
	TELEL	Read or Write Cycle Time	420		350	240		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
3. Capacitance sampled and guaranteed – not 100% tested.
4. AC test conditions: Inputs – TRISE = TFALL = 20nsec; Output – 1 TTL load and 50pF; All timing measured at ½ VCC.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage – VCC	+8.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature	-65°C to +150°C

OPERATING RANGE

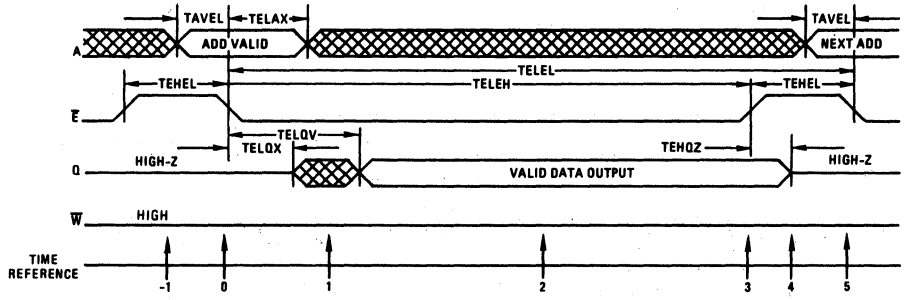
Operating Supply Voltage Commercial	4.75V to 5.25V
Operating Temperature Commercial	0°C to +75°C

ELECTRICAL CHARACTERISTICS

			TEMP. & VCC = OPERATING RANGE		TEMP = 25°C ① VCC = 5.0V				
	SYMBOL	PARAMETER	MIN	MAX	MIN	TYP	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		500		100	500	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		7		5	6	mA	f = 1MHz, IO = 0 VI = VCC or GND
	II	Input Leakage Current	-10.0	+10.0	-7.0	±0.5	+7.0	μA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-10.0	+10.0	-7.0	±0.5	+7.0	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.25	0.35	V	IO = 1.6mA
	VOH	Output High Voltage	2.4		3.5	4.0		V	IO = -0.4mA
	CI	Input Capacitance ③		8.0		5.0	8.0	pF	f = 1MHz VI = VCC or GND
	CO	Output Capacitance ③		10.0		6.0	10.0	pF	f = 1MHz VO = VCC or GND
A.C.	TELQV	Chip Enable Access Time		350		200	300	ns	④
	TAVQV	Address Access Time		370		200	320	ns	④
	TELQX	Chip Enable Output Enable Time		100		50	80	ns	④
	TEHQZ	Chip Enable Output Disable Time		100		50	80	ns	④
	TELEH	Chip Enable Pulse Negative Width	350		300	200		ns	④
	TEHEL	Chip Enable Pulse Positive Width	150		120	100		ns	④
	TAVEL	Address Setup Time	20		20	0		ns	④
	TELAX	Address Hold Time	50		50	20		ns	④
	TWLWH	Write Enable Pulse Width	100		80	60		ns	④
	TWLEH	Write Enable Pulse Setup Time	250		200	100		ns	④
	TWLEL	Early Write Pulse Setup Time	0		0	-10		ns	④
	TWHEL	Write Enable Read Setup Time	0		0	-10		ns	④
	TELWH	Early Write Pulse Hold Time	100		80	60		ns	④
	TDVWL	Data Setup Time	30		20	0		ns	④
	TDVEL	Early Write Data Setup Time	30		20	0		ns	④
	TWLDX	Data Hold Time	100		80	60		ns	④
	TELDX	Early Write Data Hold Time	100		80	80		ns	④
	TELWL	Early Write Output Hi-Z Time	0		0	-10		ns	④
	TQVWL	Data Valid to Write Time	0		0	0		ns	④
	TELEL	Read or Write Cycle Time	500		420	300		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
3. Capacitance sampled and guaranteed – not 100% tested.
4. AC test conditions: Inputs – TRISE = TFALL = 20nsec; Output – 1 TTL load and 50pF; All timing measured at ½ VCC.

Read Cycle

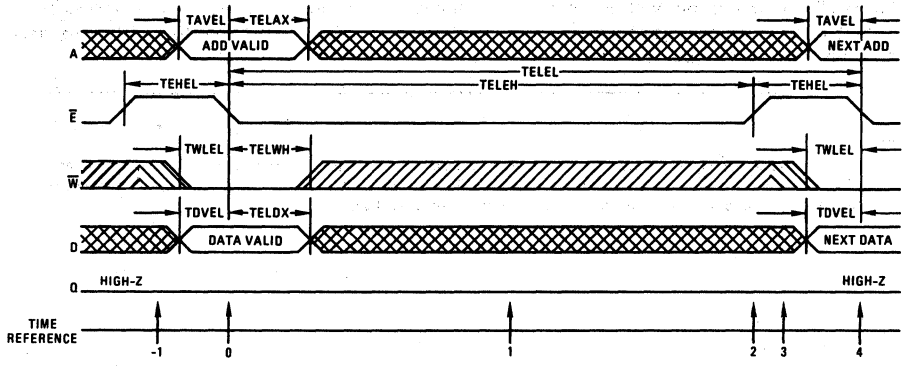


TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	OUTPUT Q	FUNCTION
-1	H	X	X	Z	MEMORY DISABLED
0	↘	H	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	X	X	OUTPUT ENABLED
2	L	H	X	V	OUTPUT VALID
3	↗	H	X	V	READ ACCOMPLISHED
4	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The address information is latched in the on chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address set up and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1) the output becomes enabled but data is not valid until during time (T = 2). $\overline{W}$ must remain high until after time (T = 2). After the output data has been read, $\overline{E}$ may return high (T = 3). This will disable the output buffer and ready the RAM for the next memory cycle (T = 4).

Early Write Cycle

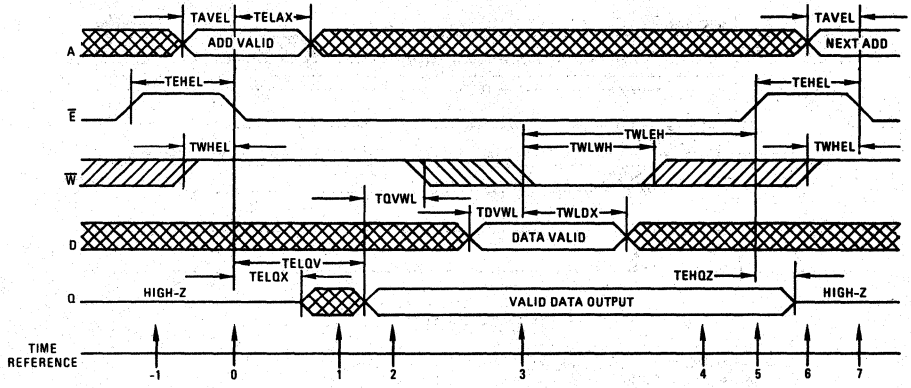


TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	D	OUTPUT Q	FUNCTION
-1	H	X	X	X	Z	MEMORY DISABLED
0	↘	L	V	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	X	X	X	Z	WRITE IN PROGRESS INTERNALLY
2	↗	X	X	X	Z	WRITE COMPLETED
3	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
4	↘	L	V	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The early write cycle is the only cycle where the output is guaranteed not to become active. On the falling edge of $\overline{E}$ (T = 0), the addresses, the write signal, and the data input are latched in on chip registers. The logic value of $\overline{W}$ at the time $\overline{E}$ falls determines the state of the output buffer for that cycle. Since $\overline{W}$ is low in the early write cycle the output buffer is latched into the high impedance state and will remain in that state until $\overline{E}$ returns high (T = 2). For this cycle, the data input is latched by $\overline{E}$ going low; therefore data set up and hold times should be referenced to $\overline{E}$. When $\overline{E}$ (T = 2) returns to the high state the output buffer disables and all signals are unlatched. The device is now ready for the next cycle.

Read Modify Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS Ē	W̄	A	D	OUTPUT Q	FUNCTION
-1	H	X	X	X	Z	MEMORY DISABLED
0	↘	H	V	X	Z	CYCLE BEGINS, ADDRESS ARE LATCHED
1	L	H	X	X	X	OUTPUT ENABLED
2	L	H	X	X	V	OUTPUT VALID, READ AND MODIFY TIME
3	L	↘	X	V	V	WRITE BEGINS, DATA IS LATCHED
4	L	X	X	X	V	WRITE IN PROGRESS INTERNALLY
5	↗	X	X	X	V	WRITE COMPLETED
6	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
7	↘	H	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The read modify write cycle begins as all other cycles on the falling edge of Ē (T= 0). The W̄ line should be high at (T = 0) in order to latch the output buffers in the active state. During (T = 1) the output will be active but not valid until (T = 2). On the falling edge of the W̄ (T = 3) the data present at the output and input are latched. The W̄ signal also latches itself on its low going edge. All input signals excluding Ē have been latched and have no further effect on the RAM. The rising edge of Ē (T = 5) completes the write portion of the cycle and unlatches all inputs and the output. The output goes to a high impedance and the RAM is ready for the next cycle.

3

NOTES:

In the above descriptions the numbers in parenthesis (T = n) refer to the respective timing diagrams. The numbers are located on the time reference line below each diagram. The timing diagrams shown are only examples and are not the only valid method of operation.

Battery Backup Applications

The HM-6504 is especially well suited for use in battery backup systems. Data retention supply voltage and supply current are guaranteed over the full temperature range.

When designing the backup system, the following suggestions should be considered:

1.) As RAM VCC drops, the input logical one voltages should follow so as not to exceed VCC +0.3. It is suggested to use CMOS drivers, operating at CMOS VCC, such as the HD-6495, HD-6432, and HD-6433. Another approach is the use of open collector or open drain buffers pulled up to CMOS VCC.

2.) $\overline{E}$ must be held high at CMOS VCC. $\overline{W}$, address and data inputs should be held at either GND or CMOS VCC to minimize power dissipation.

3.) When exiting from the battery backup mode, VCC should ramp without ring or discontinuities.

4.) The RAM can begin operation one TEHEL after VCC reaches the minimum operating voltage (4.5 or 4.75 volts).

A very simple battery backup system is shown in Figure 1. When system power is available, diode D1 is forward biased and supplies current to the CMOS devices. Upon loss of system power, diode D1 is reverse biased and only CMOS devices are consuming battery power. A disadvantage to this method is that CMOS VCC is one diode drop, .7V, below TTL VCC. There is a possibility that a TTL output signal could rise higher than CMOS VCC and cause possible latch problems. This possibility can be reduced by incorporating a system similar to that shown in Figure 2. Other alternatives include using a germanuin diode yielding a VF ≈ .2V or adding diode D2 in the TTL supply and raising VCC to account for the drop. A PNP transistor is substituted for the diode in Figure 2. The saturation drop of the transistor, 0.2V, is less than the 0.7V drop of the diode giving more margin against latch-up. A power fail output signal is available to disable the $\overline{E}$ circuitry. Open collector TTL with pullups to CMOS VCC or LS type TTL should be used as memory drivers. This will insure that the CMOS inputs are not floating during the backup period. When system power is restored, operation continues as normal and the NI-CAD battery pack is trickle charged through RC.

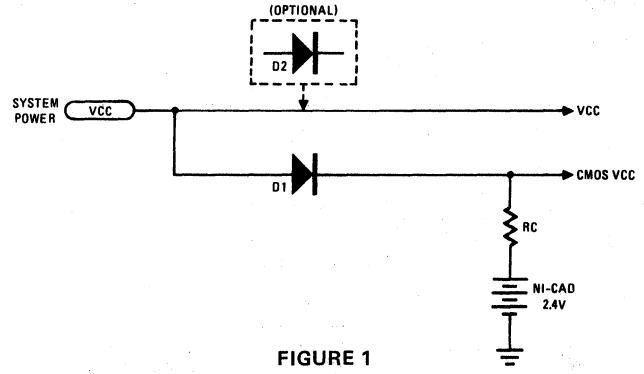


FIGURE 1

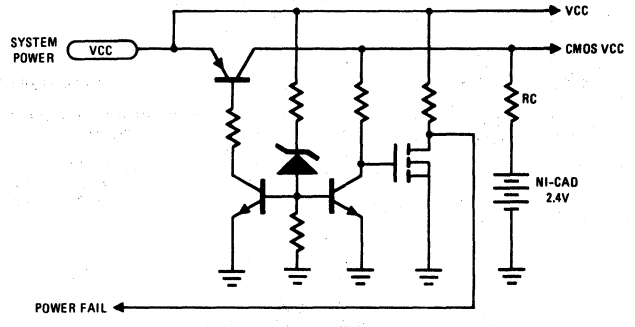


FIGURE 2

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-6508

1024 x 1 CMOS RAM

JULY 1978

Features

- LOW STANDBY POWER . . . . . 55 μW MAX
- LOW OPERATING POWER . . . . . 22mW/MHz MAX
- FAST ACCESS TIME . . . . . 180nsec MAX
- DATA RETENTION VOLTAGE . . . . . 2.0 VOLTS MIN
- TTL COMPATIBLE IN/OUT
- HIGH OUTPUT DRIVE – 2 TTL LOADS
- HIGH NOISE IMMUNITY
- ON CHIP ADDRESS REGISTER
- MILITARY TEMPERATURE RANGE
- INDUSTRIAL TEMPERATURE RANGE
- THREE-STATE OUTPUTS
- 16 PIN PACKAGE FOR HIGH DENSITY

Description

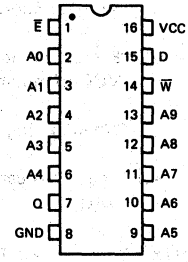
The HM-6508 is a 1024 by 1 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

On chip latches are provided for address allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

The HM-6508 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

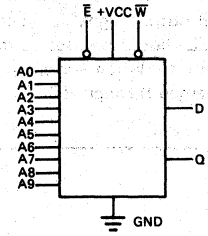
Pinout

TOP VIEW



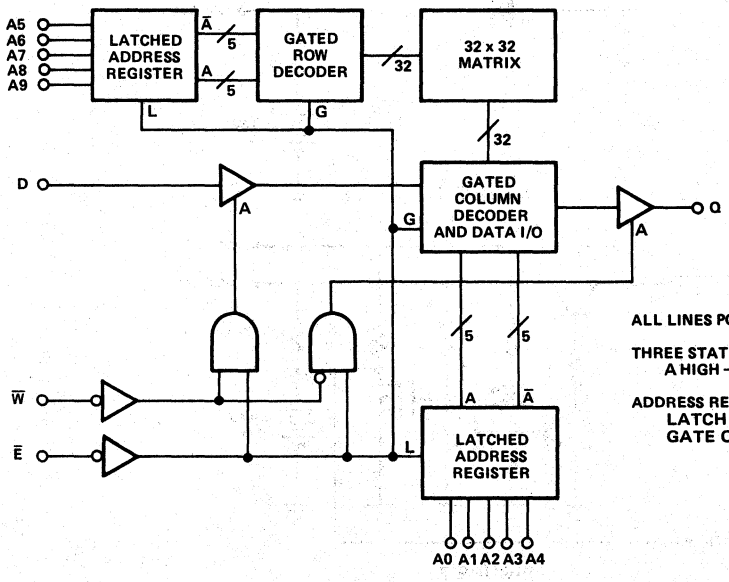
A – Address Input
Ē – Chip Enable
W̄ – Write Enable
D – Data Input
Q – Data Output

Logic Symbol



3

Functional Diagram



ALL LINES POSITIVE LOGIC – ACTIVE HIGH

THREE STATE BUFFERS:
A HIGH → OUTPUT ACTIVE

ADDRESS REGISTER AND DECODERS:
LATCH ON RISING EDGE OF L
GATE ON RISING EDGE OF G

ABSOLUTE MAXIMUM RATINGS

Supply Voltage -VCC	+8.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage -VCC	
Military (-2)	4.5V to 5.5V
Industrial (-9)	4.5V to 5.5V
Operating Temperature	
Military (-2)	-55°C to +125°C
Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MIN	TEMP. = 25°C ① VCC = 5.0V TYP	TEMP. = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current		10 1(+25°C)		0.1	1	µA	IO = 0 VI = VCC or GND
ICCOP	Operating Supply Current ②		4		1.5	2.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
ICCDR	Data Retention Supply Current		10		0.01	1	µA	VCC = 3.0, IO = 0 VI = VCC or GND
VCCDR	Data Retention Supply Voltage	2.0		2.0	1.4		V	
II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	µA	GND ≤ VI ≤ VCC
IOZ	Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	µA	GND ≤ VO ≤ VCC
VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 3.2mA
VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -0.4mA
CI	Input Capacitance ③		6		4	6	pF	VI = VCC or GND f = 1MHz
CO	Output Capacitance ③		10		6	10	pF	VO=VCC or GND f = 1MHz
TELQV	Chip Enable Access Time		180		100	140	ns	④
TAVQV	Address Access Time		180		90	140	ns	④
TELQX	Chip Enable Output Enable Time		120		40	80	ns	④
TWLQZ	Write Enable Output Disable Time		120		40	80	ns	④
TEHQZ	Chip Enable Output Disable Time		120		40	80	ns	④
TELEH	Chip Enable Pulse Negative Width	180		140	100		ns	④
TEHEL	Chip Enable Pulse Positive Width	100		80	50		ns	④
TAVEL	Address Setup Time	0		0	-10		ns	④
TELAX	Address Hold Time	40		30	20		ns	④
TDVWH	Data Setup Time	80		60	40		ns	④
TWHDX	Data Hold Time	0		0	0		ns	④
TWLEH	Chip Enable Write Pulse Setup Time	100		80	50		ns	④
TELWH	Chip Enable Write Pulse Hold Time	100		80	50		ns	④
TWLWH	Write Enable Pulse Width	100		80	50		ns	④
TELEL	Read or Write Cycle Time	280		220	150		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — 1 TTL load and 50pF. All timing measurements at 1/2 VCC.

ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage -VCC	+8.0V	Operating Supply Voltage -VCC	
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V	Military (-2)	4.5V to 5.5V
		Industrial (-9)	4.5V to 5.5V
Storage Temperature	-65°C to +150°C	Operating Temperature	
		Military (-2)	-55°C to +125°C
		Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MIN	TEMP. = 25°C ① VCC = 5.0V TYP	TEMP. = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
	ICCSB	Standby Supply Current		10 1(+25°C)		1.0	1	µA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4		1.5	2.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		10		0.1	1	µA	VCC = 3.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		2.0	1.4		V	
D.C.	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	µA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	µA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 3.2mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -0.4mA
	CI	Input Capacitance ③		6		4	6	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10		6	10	pF	VO=VCC or GND f = 1MHz
	TELQV	Chip Enable Access Time		250		110	200	ns	④
	TAVQV	Address Access Time		250		100	200	ns	④
	TELQX	Chip Enable Output Enable Time		160		60	130	ns	④
	TWLQZ	Write Enable Output Disable Time		160		60	130	ns	④
	TEHQZ	Chip Enable Output Disable Time		160		60	130	ns	④
	TELEH	Chip Enable Pulse Negative Width	250		200	110		ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		80	50		ns	④
A.C.	TAVEL	Address Setup Time	0		0	-10		ns	④
	TELAX	Address Hold Time	50		40	30		ns	④
	TDVWH	Data Setup Time	110		80	50		ns	④
	TWHDX	Data Hold Time	0		0	0		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	130		100	60		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	130		100	60		ns	④
	TWLWH	Write Enable Pulse Width	130		100	60		ns	④
	TELEL	Read or Write Cycle Time	350		280	160		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — 1 TTL load and 50pF. All timing measurements at 1/2 VCC.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage -VCC	+8.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature	-65°C to +150°C

OPERATING RANGE

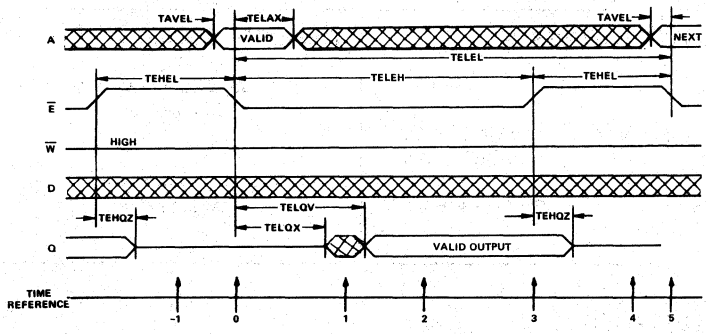
Operating Supply Voltage -VCC Commercial	4.75V to 5.25V
Operating Temperature Commercial	0°C to +75°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MIN	TEMP. = 25°C ① VCC = 5.0V TYP	TEMP. = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		100		10	100	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4		1.5	2.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		2.0			V	
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ⩽ VI ⩽ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ⩽ VO ⩽ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 1.6mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -0.2mA
	CI	Input Capacitance ③		6		4	6	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10		6	10	pF	VO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		300		160	250	ns	④
	TAVQV	Address Access Time		310		160	260	ns	④
	TELQX	Chip Enable Output Enable Time		200		60	170	ns	④
	TWLQZ	Write Enable Output Disable Time		200		60	170	ns	④
	TEHQZ	Chip Enable Output Disable Time		200		60	170	ns	④
	TELEH	Chip Enable Pulse Negative Width	300		250	160		ns	④
	TEHEL	Chip Enable Pulse Positive Width	150		130	90		ns	④
	TAVEL	Address Setup Time	10		10	0		ns	④
	TELAX	Address Hold Time	70		50	40		ns	④
	TDVWH	Data Setup Time	130		100	80		ns	④
	TWHDX	Data Hold Time	0		0	0		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	160		130	100		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	160		130	100		ns	④
	TWLWH	Write Enable Pulse Width	160		130	100		ns	④
	TELEL	Read or Write Cycle Time	450		380	250		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — 1 TTL load and 50pF. All timing measurements at 1/2 VCC.

Read Cycle



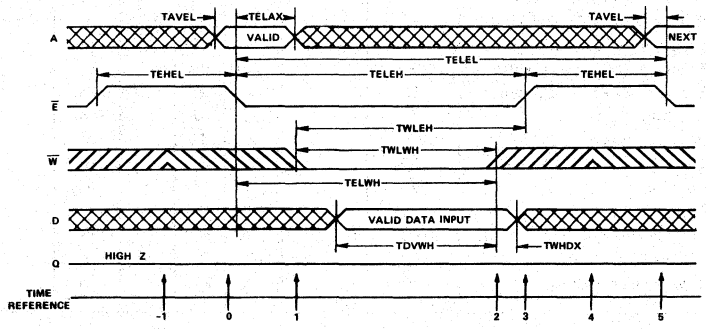
TRUTH TABLE

TIME REFERENCE	INPUTS Ē	W̄	A	D	OUTPUTS Q	FUNCTION
-1	H	X	X	X	Z	MEMORY DISABLED
0	↘	H	V	X	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	X	X	X	OUTPUT ENABLED
2	L	H	X	X	V	OUTPUT VALID
3	↗	H	X	X	V	READ ACCOMPLISHED
4	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	H	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

In the HM-6508 Read Cycle, the address information is latched into the on chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address setup and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1) the data output becomes enabled; however, the data is not valid until during time (T = 2). $\overline{W}$ must remain high for the read cycle. After the output data has been read, $\overline{E}$ may return high (T = 3). This will disable the chip and force the output buffer to a high impedance state. After the required $\overline{E}$ high time (TEHEL) the RAM is ready for the next memory cycle (T = 4).

3

Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS Ē	W̄	A	D	OUTPUTS Q	FUNCTION
-1	H	X	X	X	Z	MEMORY DISABLED
0	↘	X	V	X	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	↘	X	X	Z	WRITE PERIOD BEGINS
2	L	↗	X	V	Z	DATA IS WRITTEN
3	↗	H	X	X	Z	WRITE COMPLETED
4	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	X	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The write cycle is initiated by the falling edge of $\overline{E}$ which latches the address information into the on chip registers. The write portion of the cycle is defined as both $\overline{E}$ and $\overline{W}$ being low simultaneously. $\overline{W}$ may go low anytime during the cycle provided that the write enable pulse setup time (TWLEH) is met. The write portion of the cycle is terminated by the first rising edge of either $\overline{E}$ or $\overline{W}$. Data setup and hold times must be referenced to the terminating signal.

If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may remain low until all desired locations have been written. When this method is used, data setup and hold times must be referenced to the rising edge of $\overline{E}$. By positioning the $\overline{W}$ pulse at different times within the $\overline{E}$ low time (TELEH), various types of write cycles may be performed.

If the $\overline{E}$ low time (TELEH) is greater than the $\overline{W}$ pulse (TWLWH) plus an output enable time (TELQX), a combination read write cycle is executed. Data may be modified an indefinite number of times during any write cycle (TELEH). The data input and data output pins may be tied together for use with a common I/O data bus structure. When using the RAM in this method allow a minimum of one output disable time (TWLQZ) after $\overline{W}$ goes low before applying input data to the bus. This will insure that the output buffers are not active.

Battery Backup Applications

The HM-6508 is especially well suited for use in battery backup systems. Data retention supply voltage and supply current are guaranteed over the full temperature range.

When designing the backup system, the following suggestions should be considered:

1.) As RAM VCC drops, the input logical one voltages should follow so as not to exceed VCC +0.3. It is suggested to use CMOS drivers, operating at CMOS VCC, such as the HD-6495, HD-6432, and HD-6433. Another approach is the use of open collector or open drain buffers pulled up to CMOS VCC.

2.) $\overline{E}$ must be held high at CMOS VCC. $\overline{W}$, address and data inputs should be held at either GND or CMOS VCC to minimize power dissipation.

3.) When exiting from the battery backup mode, VCC should ramp without ring or discontinuities.

4.) The RAM can begin operation one TEHEL after VCC reaches the minimum operating voltage (4.5 or 4.75V).

A very simple battery backup system is shown in Figure 1. When system power is available, diode D1 is forward biased and supplies current to the CMOS devices. Upon loss of system power, diode D1 is reverse biased and only CMOS devices are consuming battery power. A disadvantage to this method is that CMOS VCC is one diode drop, .7V, below TTL VCC. There is a possibility that a TTL output signal could rise higher than CMOS VCC and cause possible latch problems. This possibility can be reduced by incorporating a system similar to that shown in Figure 2. Other alternatives include using a germanuin diode yielding a VF $\approx$ .2V or adding diode D2 in the TTL supply and raising VCC to account for the drop. A PNP transistor is substituted for the diode in Figure 2. The saturation drop of the transistor, 0.2V, is less than the 0.7V drop of the diode giving more margin against latch-up. A power fail output signal is available to disable the $\overline{E}$ circuitry. Open collector TTL with pullups to CMOS VCC or LS type TTL should be used as memory drivers. This will insure that the CMOS inputs are not floating during the backup period. When system power is restored, operation continues as normal and the NI-CAD battery pack is trickle charged through RC.

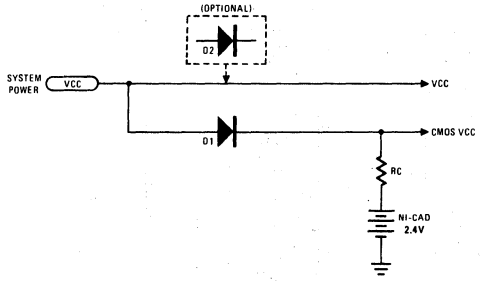


FIGURE 1

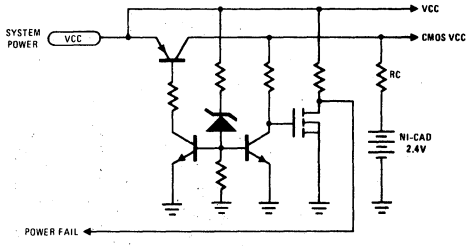


FIGURE 2

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-6512

64 x 12 CMOS RAM

Preliminary

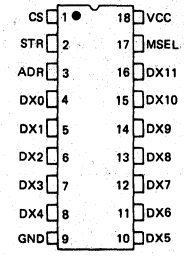
APRIL 1978

Features

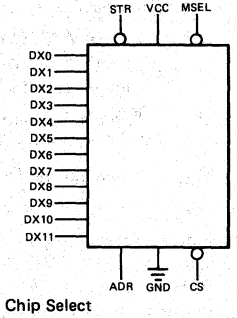
- LOW POWER STANDBY . . . . . 1mW MAX.
- LOW POWER OPERATION. . . . . .22mW/MHz MAX.
- DATA RETENTION . . . . . @ 2.0V MIN.
- TTL COMPATIBLE INPUT/OUTPUT
- TWO HM-6512's CAN BE USED WITH HM-6100 AND HM-6312 WITHOUT ADDITIONAL COMPONENTS
- THREE STATE OUTPUTS
- FAST ACCESS TIME . . . . . .250nsec MAX.
- MILITARY AND INDUSTRIAL TEMPERATURE RANGE
- 18 PIN PACKAGE FOR HIGH DENSITY
- ON CHIP ADDRESS REGISTER

Pinout

TOP VIEW



Logic Symbol



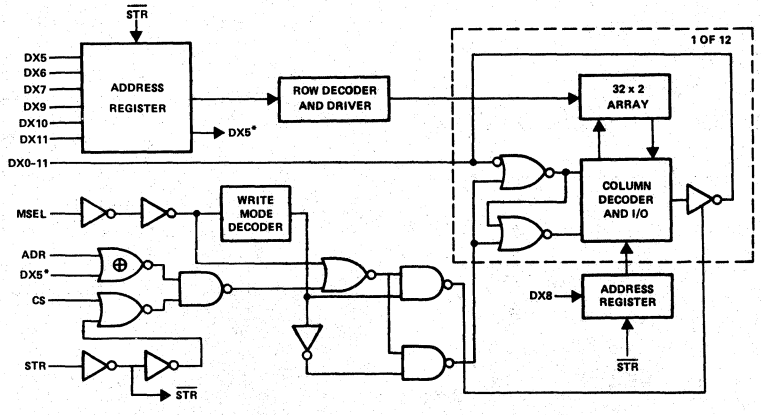
CS — Chip Select
STR — Chip Enable
MSEL — Enable and R/W Decode
ADR — Address Decode
DX — Address Input and Data I/O

Description

The HM-6512 is a high speed, low power, silicon gate CMOS 768 bit static RAM organized 64 words by 12 bits. In all static states these units exhibit the microwatt power requirements typical of CMOS. Inputs and three state outputs are TTL compatible. The basic part operates at 4-7 volts with a typical 5 volt, 25°C access time of 150ns.

Signal polarities and functions are specified for direct interfacing with the HM-6100 microprocessor. The device is ideally suited for minimum system all CMOS applications where low power, minimum cost, or non-volatility is required.

Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	8.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HM-6512-9	-40°C to +85°C
Military HM-6512-2	-55°C to +125°C

ELECTRICAL CHARACTERISTICS VCC = 5.0V ±10%, TA = Industrial or Military

	SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	TEST CONDITIONS
D.C.	VIH	Logical "1" Input Voltage	VCC -2.0			V	
	VIL	Logical "0" Input Voltage			0.8	V	
	IIL	Input Leakage	-1.0		+1.0	μA	0V ≤ VIN ≤ VCC
	VOH	Logical "1" Output Voltage	2.4			V	IOH = -0.2mA
	VOL	Logical "0" Output Voltage			0.45	V	IOL = 2.0mA
	IO	Output Leakage	-1.0		+1.0	μA	0V ≤ VO ≤ VCC
	ICCSB	Supply Current Standby		1.0	100	μA	STR = VCC = 5.5V VIN = VCC or GND
	ICCDR	Supply Current Data Retention		0.1	50	μA	STR = VCC = 3.0V VIN = VCC or GND
	CI	Input Capacitance		5.0	7.0	pF	
	CIO*	Input/Output Capacitance		6.0	10.0	pF	
A.C.	TAC	Access Time from STR			250	ns	CL = 50pF See Figures 1 & 2
	TEN	Output Enable Time			200	ns	
	TDIS	Output Disable Time			200	ns	
	TSTR	STR Pulse Width (Positive)	200			ns	
	$\overline{TSTR}$	STR Pulse Width (Negative)	250			ns	
	TC	Cycle Time	450			ns	
	TWP	Write Pulse Width (Negative)	130			ns	
	TAS	Address Setup Time	30			ns	
	TAH	Address Hold Time	50			ns	
	TDS	Data Setup Time	130			ns	
	TDH	Data Hold Time	0			ns	
	TPS	MSEL Pulse Separation	150			ns	
	TMS	MSEL Setup Time	50			ns	
	TMH	MSEL Hold Time	50			ns	

*Guaranteed but not 100% tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	7.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HM-6512C-9	-40°C to +85°C

ELECTRICAL CHARACTERISTICS VCC = 5.0V ±5%, TA = Industrial

	SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	TEST CONDITIONS
D.C.	VIH	Logical "1" Input Voltage	VCC -1.5			V	
	VIL	Logical "0" Input Voltage			0.8	V	
	IIL	Input Leakage	-5.0		+5.0	μA	0V ≤ VIN ≤ VCC
	VOH	Logical "1" Output Voltage	2.4			V	IOH = -0.2mA
	VOL	Logical "0" Output Voltage			0.45	V	IOL = 1.6mA
	IO	Output Leakage	-5.0		+5.0	μA	0V ≤ VO ≤ VCC
	ICCSB	Supply Current Standby			800	μA	STR = VCC = 5.25V VIN = VCC or GND
	CIN*	Input Capacitance		5.0	7.0	pF	
	CIO*	Input/Output Capacitance		6.0	10.0	pF	
A.C.	TAC	Access Time from STR			400	ns	CL = 50pF See Figures 1 & 2
	TEN	Output Enable Time			300	ns	
	TDIS	Output Disable Time			300	ns	
	TSTR	STR Pulse Width (Positive)	250			ns	
	$\overline{TSTR}$	STR Pulse Width (Negative)	400			ns	
	TC	Cycle Time	650			ns	
	TWP	Write Pulse Width (Negative)	200			ns	
	TAS	Address Setup Time	60			ns	
	TAH	Address Hold Time	100			ns	
	TDS	Data Setup Time	200			ns	
	TDH	Data Hold Time	0			ns	
	TPS	MSEL Pulse Separation	150			ns	
	TMS	MSEL Setup Time	100			ns	
	TMH	MSEL Hold Time	100			ns	

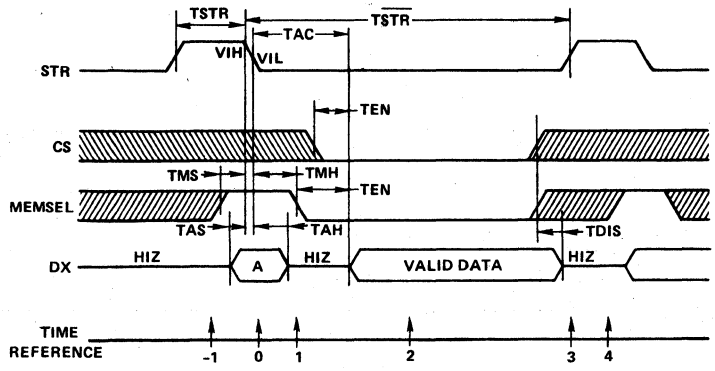
*Guaranteed but not 100% tested.

Functional Description

MSEL – The MSEL pin functions as a second chip enable and a write enable pin. If MSEL is low during the address strobe time the chip is placed in the write mode immediately. If MSEL is high during address strobe the chip performs a read operation during the first MSEL pulse and a write operation during the second MSEL pulse. In the event that a read only operation is desired the second MSEL pulse would be omitted.

ADR – The ADR pin provides the user with a method for using two HM-6512 chips in a HM-6100, HM-6312 ROM based system without any further decoding. The data on this pin is compared internally with address on DX5. If the two match, the chip will respond to MSEL and CS, otherwise the outputs remain high impedance and the stored data is unchanged. Using the HM-6312 with RSEL pin programmed for an active low for address 0-377$_8$ and one or two HM-6512 RAMs provides for a 64 or 128 word scratch pad memory on page 0.

Read Cycle



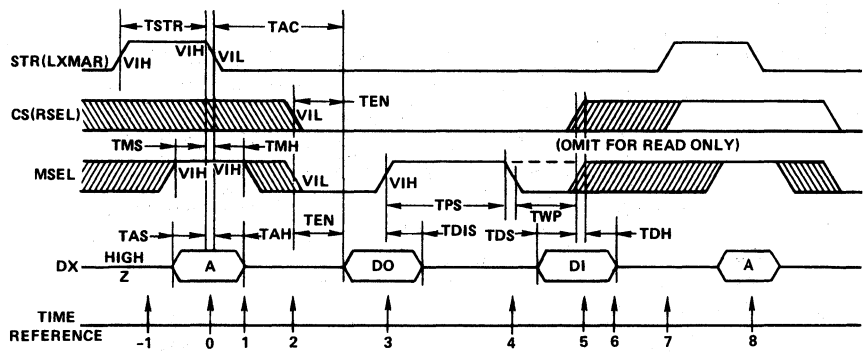
TRUTH TABLE

TIME REFERENCE	INPUTS STR	MSEL	DX	FUNCTION
-1	H	X	Z	Memory Disabled
0	↘	X	V*	Valid, Address Latched In
1	L	↘	X	End of Address Time
2	L	L	V	Valid, Data on Output
3	↗	H	Z	End of Read Cycle
4	H	X	Z	Begin New Cycle, Same as -1

*Address valid during this time.

FIGURE 1

Read Modify Write Cycle



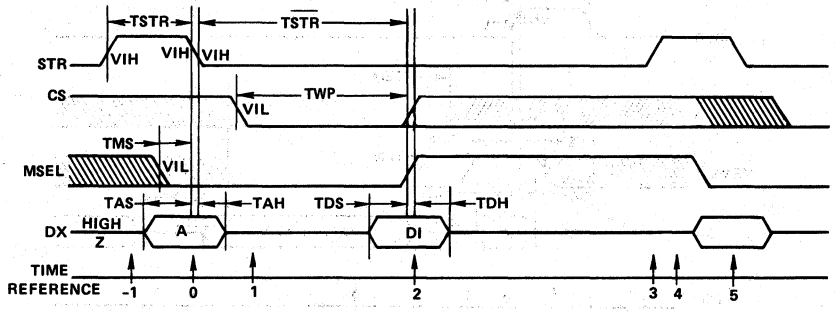
TRUTH TABLE

TIME REFERENCE	INPUTS STR	MSEL	DX	FUNCTION
-1	H	X	Z	Memory Disabled
0	↘	H	V*	Cycle Begins, Address Latched In
1	L	↘	Z	End of Address Time
2	L	L	X	Begin Read Time
3	L	↗	V	End of Read Time
4	L	↘	Z	Begin Write Time
5	L	↗	V	Data Written In
6	L	H	Z	End of Write Time
7	H	X	Z	End of Cycle, Memory Disabled
8	↘	H	V*	Begin New Cycle, New Address Latched In

*Address valid during this time.

FIGURE 2

Write Cycle



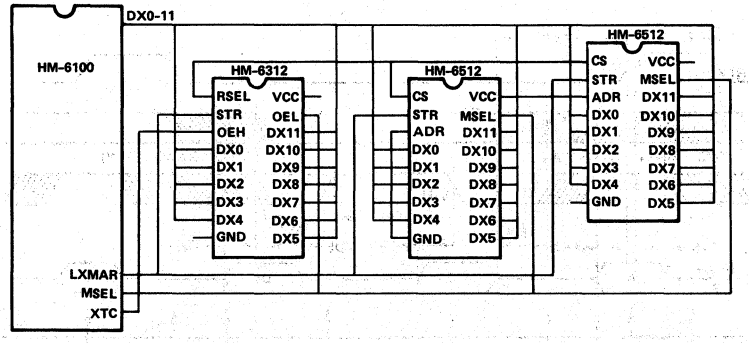
TRUTH TABLE

TIME REFERENCE	INPUTS STR	MSEL	DX	FUNCTION
-1	H	X	Z	Memory Disabled
0	↘	X	V*	Cycle Begins, Addresses are Latched
1	L	L	Z	Write Period Begins
2	L	↗	V	Data In is Written
3	↗	H	Z	Write Completed
4	H	X	Z	Prepare for Next Cycle
5	↘	X	V*	Cycle Ends, Next Cycle Begins

*Address valid during this time.

FIGURE 3

Typical Microprocessor System



HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-6513

512 x 4 CMOS RAM

JULY 1978

Features

- LOW POWER STANDBY . . . . . ≪1mW MAX.
- LOW POWER OPERATION. . . . . 35mW/MHz MAX.
- DATA RETENTION . . . . . @ 2.0V MIN.
- TTL COMPATIBILITY INPUT/OUTPUT
- COMMON DATA IN/OUT
- THREE STATE OUTPUTS
- FAST ACCESS TIME . . . . . 300nsec MAX.
- INDUSTRIAL OR COMMERCIAL TEMPERATURE RANGE
- 18 PIN PACKAGE FOR HIGH DENSITY
- ON CHIP ADDRESS REGISTER
- PINOUT ALLOWS UPGRADE TO HM-6514

Description

The HM-6513 is a 512 x 4 static CMOS RAM fabricated using self aligned silicon gate technology. The device utilizes synchronous circuitry to achieve high performance and low power operation.

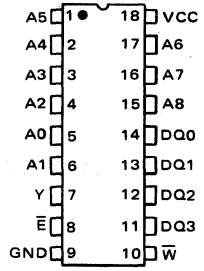
On chip latches are provided for the addresses allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance state for use in expanded memory systems.

The HM-6513 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

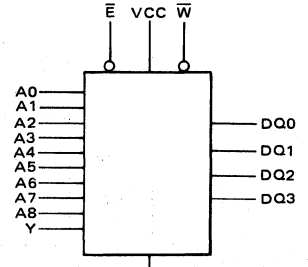
The HM-6513 is supplied in two versions, the HM-6513H and the HM-6513L. The H or L is used to designate the logic level to be connected to the Y input. If a HM-6513H is procured the user must connect the input to VCC in the system. If a HM-6513L is used the Y input must be connected to system ground.

Pinout

TOP VIEW

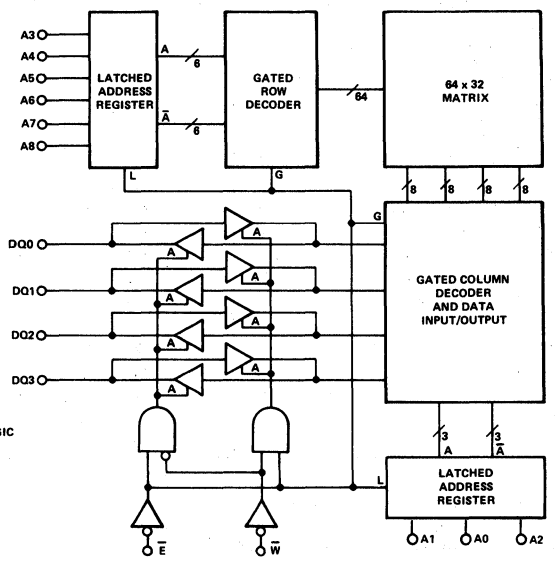


Logic Symbol



A – Address Input
Ē – Chip Enable
W̄ – Write Enable
DQ – Data In/Out
Y – Hard Wired Input

Functional Diagram



ALL LINES ACTIVE HIGH – POSITIVE LOGIC

THREE STATE BUFFERS:
A HIGH → OUTPUT ACTIVE

ADDRESS REGISTERS:
LATCH ON RISING EDGE OF L

GATED DECODERS:
GATE ON RISING EDGE OF G

ABSOLUTE MAXIMUM RATINGS

Supply Voltage – VCC	+8.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage Industrial (-9)	4.5V to 5.5V
Operating Temperature Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

			TEMP. & VCC = OPERATING RANGE		TEMP = 25°C ① VCC = 5.0V				
	SYMBOL	PARAMETER	MIN	MAX	MIN	TYP	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		50		0.1	10	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		7		5	6	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		25		0.01	5	μA	IO = 0 VCC = 3.0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		2.0	1.4		V	
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VIO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.45		0.35	0.4	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		3.5	4.0		V	IO = -1.0mA
	CI	Input Capacitance ③		8.0		5.0	8.0	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance ③		10.0		6.0	10.0	pF	VIO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		300		170	250	ns	④
	TAVQV	Address Access Time		320		170	270	ns	④
	TELQX	Chip Enable Output Enable Time		100		50	80	ns	④
	TWLQZ	Write Enable Output Disable Time		100		50	80	ns	④
	TEHQZ	Chip Enable Output Disable Time		100		50	80	ns	④
	TELEH	Chip Enable Pulse Negative Width	300		250	170		ns	④
	TEHEL	Chip Enable Pulse Positive Width	120		100	70		ns	④
	TAVEL	Address Setup Time	20		20	0		ns	④
	TELAX	Address Hold Time	50		50	20		ns	④
	TWLWH	Write Enable Pulse Width	300		240	150		ns	④
	TWLEH	Write Enable Pulse Setup Time	300		240	150		ns	④
	TELWH	Write Enable Pulse Hold Time	300		240	150		ns	④
	TDVWH	Data Setup Time	200		160	100		ns	④
	TWHDZ	Data Hold Time	0		0	-10		ns	④
	TWHEL	Write Enable Read Setup Time	0		0	-10		ns	④
	TQVWL	Data Valid to Write Time	0		0	-10		ns	④
	TWLDV	Write Data Delay Time	100		80	50		ns	④
	TWLEL	Early Output High-Z Time	0		0	–10		ns	④
	TEHWH	Late Output High-Z Time	0		0	–10		ns	④
	TELEL	Read or Write Cycle Time	420		350	240		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
3. Capacitance sampled and guaranteed – not 100% tested.
4. AC test conditions: Inputs – TRISE = TFALL = 20nsec; Outputs – 1 TTL load and 50pF; All timing measured at ½ VCC.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage – VCC	+8.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature	-65°C to +150°C

OPERATING RANGE

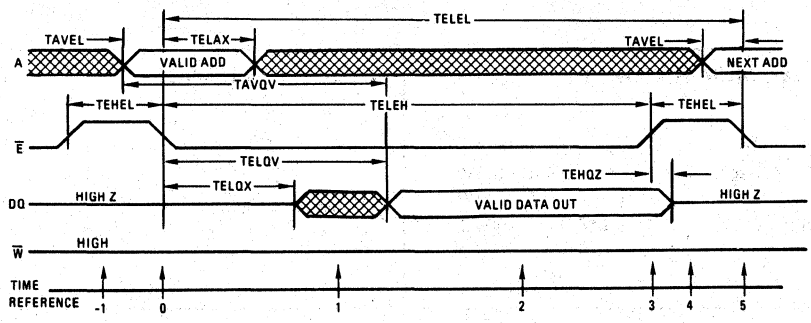
Operating Supply Voltage Commercial	4.75V to 5.25V
Operating Temperature Commercial	0°C to +75°C

ELECTRICAL CHARACTERISTICS

			TEMP. & VCC = OPERATING RANGE		TEMP = 25°C ① VCC = 5.0V				
	SYMBOL	PARAMETER	MIN	MAX	MIN	TYP	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		500		100	500	μA	VI = VCC or GND
	ICCOP	Operating Supply Current ②		7		5	6	mA	f = 1MHz, IO = 0 VI = VCC or GND
	II	Input Leakage Current	-10.0	+10.0	-7.0	±0.5	+7.0	μA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-10.0	+10.0	-7.0	±0.5	+7.0	μA	GND ≤ VIO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.45		0.35	0.4	V	IO = 1.6mA
	VOH	Output High Voltage	2.4		3.5	4.0		V	IO = -0.4mA
	CI	Input Capacitance ③		8.0		5.0	8.0	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance ③		10.0		6.0	10.0	pF	VIO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		350		200	300	ns	④
	TAVQV	Address Access Time		370		200	320	ns	④
	TELQX	Chip Enable Output Enable Time		100		50	80	ns	④
	TWLQZ	Write Enable Output Disable Time		100		50	80	ns	④
	TEHQZ	Chip Enable Output Disable Time		100		50	80	ns	④
	TELEH	Chip Enable Pulse Negative Width	350		300	200		ns	④
	TEHEL	Chip Enable Pulse Positive Width	150		120	100		ns	④
	TAVEL	Address Setup Time	20		20	0		ns	④
	TELAX	Address Hold Time	50		50	20		ns	④
	TWLWH	Write Enable Pulse Width	350		300	200		ns	④
	TWLEH	Write Enable Pulse Setup Time	350		300	200		ns	④
	TELWH	Write Enable Pulse Hold Time	350		300	200		ns	④
	TDVWH	Data Setup Time	250		220	150		ns	④
	TWHDZ	Data Hold Time	0		0	-10		ns	④
	TWHEL	Write Enable Read Setup Time	0		0	-10		ns	④
	TDVWL	Output Data Valid to Write Time	0		0	-10		ns	④
	TWLDV	Write Data Delay Time	100		80	50		ns	④
	TWLEL	Early Output High-Z Time	0		0	-10		ns	④
	TEHWH	Late Output High-Z Time	0		0	-10		ns	④
	TELEL	Read or Write Cycle Time	500		420	320		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
3. Capacitance sampled and guaranteed – not 100% tested.
4. AC test conditions: Inputs – TRISE = TFALL = 20nsec; Outputs – 1 TTL load and 50pF; All timing measured at ½ VCC.

Read Cycle

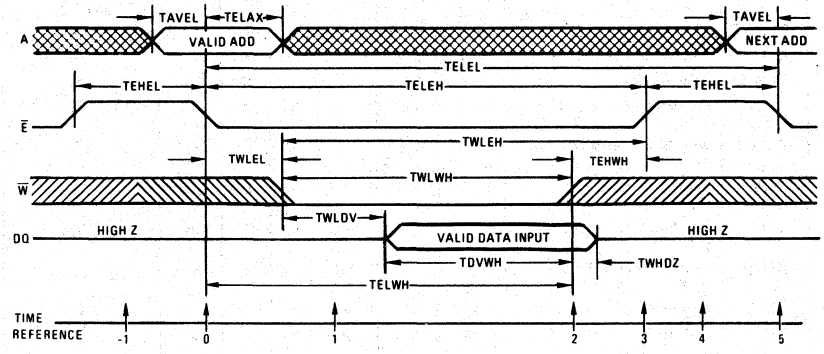


TRUTH TABLE

TIME REFERENCE	INPUTS Ē	W̄	A	DATA I/O DQ	FUNCTION
-1	H	X	X	Z	MEMORY DISABLED
0	↘	H	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	X	X	OUTPUT ENABLED
2	L	H	X	V	OUTPUT VALID
3	↗	H	X	V	READ ACCOMPLISHED
4	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The address information is latched in the on chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address setup and hold time requirements must be met. After the required hold time the addresses may change state without affecting device operation. During time (T = 1) the output becomes enabled but data is not valid until time (T = 2). $\overline{W}$ must remain high throughout the read cycle. After the data has been read $\overline{E}$ may return high (T = 3). This will force the output buffers into a high impedance mode at time (T = 4). The memory is now ready for the next cycle.

Write Cycle



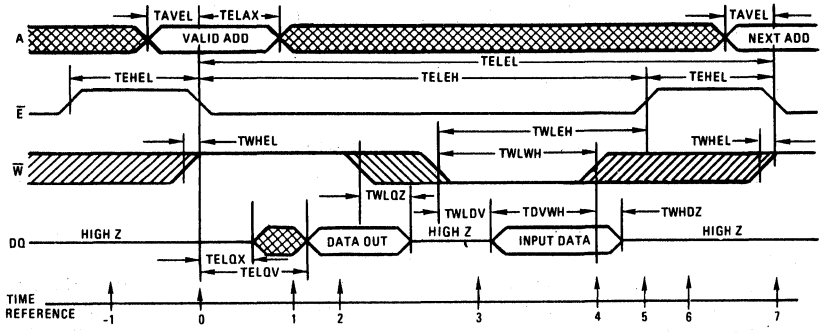
TRUTH TABLE

TIME REFERENCE	INPUTS Ē	W̄	A	DQ	FUNCTION
-1	H	X	X	Z	MEMORY DISABLED
0	↘	X	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	L	X	Z	WRITE PERIOD BEGINS
2	L	↗	X	V	DATA IN IS WRITTEN
3	↗	H	X	Z	WRITE COMPLETED
4	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	X	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The write cycle is initiated on the falling edge of $\overline{E}$ (T = 0), which latches the address information in on chip registers. If a dedicated write cycle is to be performed and the outputs are not to become active TWLEL and TEHWH must be met. Under these conditions TWLDV is unnecessary and input data may be applied at any convenient time as long as TDVWH is still met. If TWLEL is not met then the outputs may become enabled momentarily near the beginning of the cycle and a disable time (TWLQZ) must be met before the input data is applied (TWLQZ = TWLDV). Similiarly, if TEHWH is not met the outputs may enable briefly near the end of the cycle.

The write operation is terminated by the first rising edge of $\overline{W}$ (T = 2) or $\overline{E}$ (T = 3). After the minimum required $\overline{E}$ high time (TEHEL) the next cycle may begin. If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may be held low until all desired locations have been written. In this case, data setup and hold times must be referenced to the rising edge of $\overline{E}$.

Read Modify Write Cycle



TRUTH TABLE

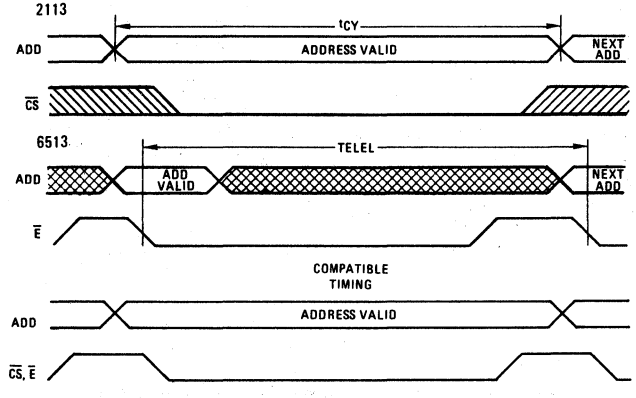
TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	DATAI/O DQ	FUNCTION
-1	H	X	X	Z	MEMORY DISABLED
0	↘	H	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	X	X	READ MODE, OUTPUT ENABLED
2	L	H	X	V	READ MODE, OUTPUT VALID
3	L	L	X	Z	WRITE MODE, OUTPUT HIGH Z
4	L	↗	X	V	WRITE MODE, DATA IS WRITTEN
5	↗	H	X	Z	WRITE COMPLETED
6	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
7	↘	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

If the pulse width of $\overline{W}$ is relatively short in relation to that of $\overline{E}$ a combination read-write cycle may be performed. If $\overline{W}$ remains high for the first part of the cycle, the outputs will become active during time (T = 1). Data out will be valid during time (T = 2). After the data is read, $\overline{W}$ can go low. After minumum TWLWH, $\overline{W}$ may return high. The information just written may now be read or $\overline{E}$ may return high, disabling the output buffers and preparing the device for the next cycle. Any number or sequence of read-write operations may be performed while $\overline{E}$ is low providing all timing requirements are met.

NOTES:

In the above descriptions the numbers in parenthesis (T = X) refer to the respective timing diagrams. The numbers are located on the time reference line below each diagram. The timing diagrams shown are only examples and are not the only valid method of operation.

2113 Compatibility



2113 — Requires the Address to Remain Valid Throughout the Cycle.

6513 — Requires Valid Address for Only a Small Portion of the Cycle, but Requires $\overline{E}$ to Fall to Initiate Each Cycle.

Battery Backup Applications

The HM-6513 is especially well suited for use in battery backup systems. Data retention supply voltage and supply current are guaranteed over the full temperature range.

When designing the backup system, the following suggestions should be considered:

1.) As RAM VCC drops, the input logical one voltages should follow so as not to exceed VCC +0.3. It is suggested to use CMOS drivers, operating at CMOS VCC, such as the HD-6495, HD-6432, and HD-6433. Another approach is the use of open collector or open drain buffers pulled up to CMOS VCC.

2.) $\overline{E}$ must be held high at CMOS VCC. $\overline{W}$, address and data inputs should be held at either GND or CMOS VCC to minimize power dissipation.

3.) When exiting from the battery backup mode, VCC should ramp without ring or discontinuities.

4.) The RAM can begin operation one TEHEL after VCC reaches the minimum operating voltage (4.5 or 4.75 volts).

A very simple battery backup system is shown in Figure 1. When system power is available, diode D1 is forward biased and supplies current to the CMOS devices. Upon loss of system power, diode D1 is reverse biased and only CMOS devices are consuming battery power. A disadvantage to this method is that CMOS VCC is one diode drop, .7, below TTL VCC. There is a possibility that a TTL output signal could rise higher than CMOS VCC and cause possible latch problems. This possibility can be reduced by incorporating a system similar to that shown in Figure 2. Other alternatives include using a germanuin diode yeilding a VF $\approx$ .2V or adding diode D2 in the TTL supply and raising VCC to account for the drop. A PNP transistor is substituted for the diode in Figure 2. The saturation drop of the transitor, 0.2V, is less than the 0.7V drop of the diode giving more margin against latch-up. A power fail output signal is available to disable the chip enable circuitry. Open collector TTL with pullups to CMOS VCC or LS type TTL should be used as memory drivers. This will insure that the CMOS inputs are not floating during the backup period. When system power is restored, operation continues as normal and the NI-CAD battery pack is trickle charged through RC.

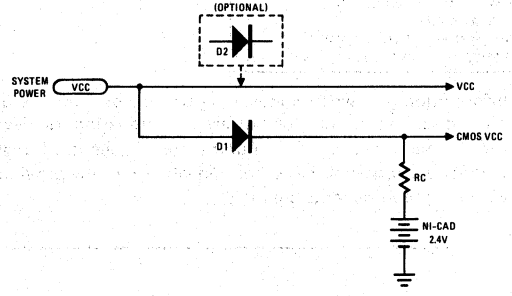


FIGURE 1

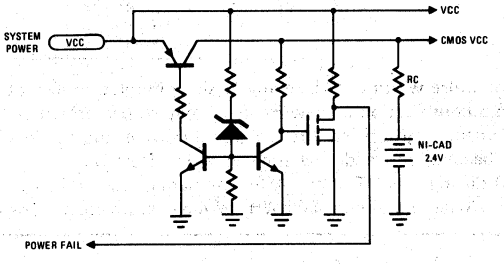
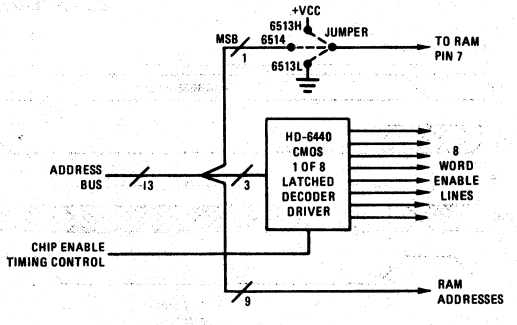


FIGURE 2

Suggestions For 6513 Memory Array Design

The HM-6513 is a device that can be used to good advantage in systems which are offered with choices of memory array size. With one common memory board layout the designer can easily offer two different array sizes. This is accomplished by using the conveniently similar pinouts of the HM-6513 (512 by 4) and the HM-6514 (1K by 4). For example, a 4K by 8 bit array using HM-6513s and a 8K word by 8 bit array using HM-6514s can be easily implemented on the same printed circuit card. The circuit diagram suggests one implementation requiring only one jumper wire for 4K or 8K word selection. This simple jumper wire also allows the 4K array to utilize the HM-6513H or the HM-6513L version.



HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-6514

1024 x 4 CMOS RAM

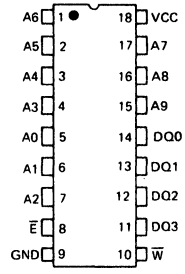
JULY 1978

Features

- LOW POWER STANDBY . . . . . ≪ 1mW MAX.
- LOW POWER OPERATION. . . . . 35mW/MHz MAX.
- DATA RETENTION . . . . . @ 2.0V MIN.
- TTL COMPATIBLE INPUT/OUTPUT
- COMMON DATA IN/OUT
- THREE-STATE OUTPUTS
- STANDARD JEDEC PINOUT
- FAST ACCESS TIME . . . . . 300nsec MAX.
- MILITARY TEMPERATURE RANGE
- INDUSTRIAL TEMPERATURE RANGE
- 18 PIN PACKAGE FOR HIGH DENSITY
- ON CHIP ADDRESS REGISTER

Pinout

TOP VIEW



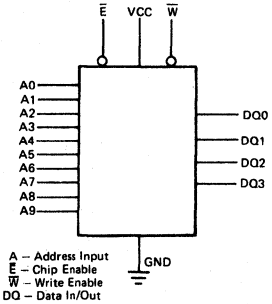
Description

The HM-6514 is a 1024 x 4 static CMOS RAM fabricated using self aligned silicon gate technology. The device utilizes synchronous circuitry to achieve high performance and low power operation.

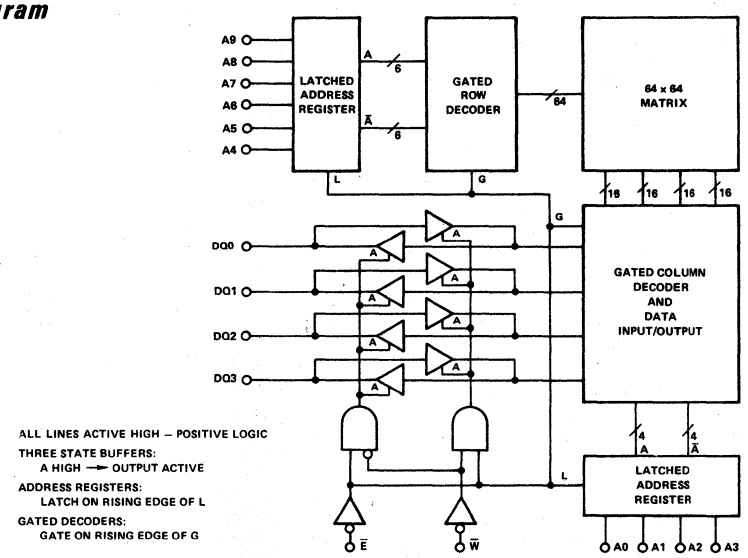
On chip latches are provided for the addresses allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance state for use in expanded memory systems.

The HM-6514 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

Logic Symbol



Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Supply Voltage – VCC	+8.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage	
Military (-2)	4.5V to 5.5V
Industrial (-9)	4.5V to 5.5V
Operating Temperature	
Military (-2)	-55°C to +125°C
Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

			TEMP. & VCC = OPERATING RANGE		TEMP = 25°C ① VCC = 5.0V				
	SYMBOL	PARAMETER	MIN	MAX	MIN	TYP	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		50		0.1	10	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		7		5	6	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		25		0.01	5	μA	IO = 0 VCC = 3.0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		2.0	1.4		V	
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.45		0.35	0.4	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		3.5	4.0		V	IO = -1.0mA
	CI	Input Capacitance ③		8.0		5.0	8.0	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance ③		10.0		6.0	10.0	pF	VO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		300		170	250	ns	④
	TAVQV	Address Access Time		320		170	270	ns	④
	TELQX	Chip Enable Output Enable Time		100		50	80	ns	④
	TWLQZ	Write Enable Output Disable Time		100		50	80	ns	④
	TEHQZ	Chip Enable Output Disable Time		100		50	80	ns	④
	TELEH	Chip Enable Pulse Negative Width	300		250	170		ns	④
	TEHEL	Chip Enable Pulse Positive Width	120		100	70		ns	④
	TAVEL	Address Setup Time	20		20	0		ns	④
	TELAX	Address Hold Time	50		50	20		ns	④
	TWLWH	Write Enable Pulse Width	300		240	150		ns	④
	TWLEH	Write Enable Pulse Setup Time	300		240	150		ns	④
	TELWH	Write Enable Pulse Hold Time	300		240	150		ns	④
	TDVWH	Data Setup Time	200		160	100		ns	④
	TWHDZ	Data Hold Time	0		0	0		ns	④
	TWHEL	Write Enable Read Setup Time	0		0	0		ns	④
	TQVWL	Data Valid to Write Time	0		0	0		ns	④
	TWLDV	Write Data Delay Time	100		80	50		ns	④
	TWLEL	Early Output High-Z Time	0		0	-10		ns	④
	TEHWH	Late Output High-Z Time	0		0	-10		ns	④
	TELEL	Read or Write Cycle Time	420		350	240		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
3. Capacitance sampled and guaranteed – not 100% tested.
4. AC test conditions: Inputs – TRISE = TFALL = 20nsec; Outputs – 1 TTL load and 50pF; All timing measured at ½ VCC.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage – VCC	+8.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature	-65°C to +150°C

OPERATING RANGE

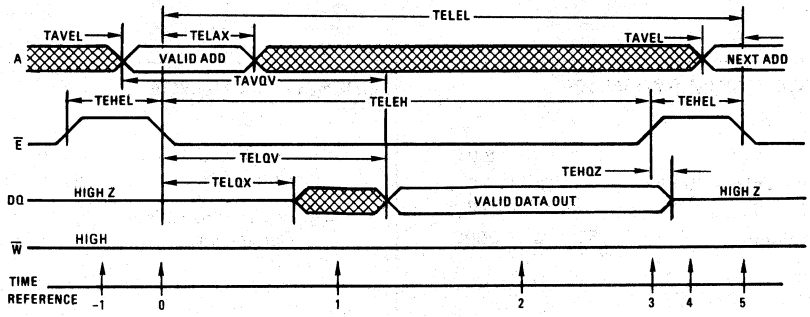
Operating Supply Voltage Commercial	4.75V to 5.25V
Operating Temperature Commercial	0°C to +75°C

ELECTRICAL CHARACTERISTICS

			TEMP. & VCC = OPERATING RANGE		TEMP = 25°C ① VCC = 5.0V				
	SYMBOL	PARAMETER	MIN	MAX	MIN	TYP	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		500		100	500	μA	VI = VCC or GND
	ICCOP	Operating Supply Current ②		7		5	6	mA	f = 1MHz, IO = 0 VI = VCC or GND
	II	Input Leakage Current	-10.0	+10.0	-7.0	±0.5	+7.0	μA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-10.0	+10.0	-7.0	±0.5	+7.0	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.45		0.35	0.4	V	IO = 1.6mA
	VOH	Output High Voltage	2.4		3.5	4.0		V	IO = -0.4mA
	CI	Input Capacitance ③		8.0		5.0	8.0	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance ③		10.0		6.0	10.0	pF	VO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		350		200	300	ns	④
	TAVQV	Address Access Time		370		200	320	ns	④
	TELQX	Chip Enable Output Enable Time		100		50	80	ns	④
	TWLQZ	Write Enable Output Disable Time		100		50	80	ns	④
	TEHQZ	Chip Enable Output Disable Time		100		50	80	ns	④
	TELEH	Chip Enable Pulse Negative Width	350		300	200		ns	④
	TEHEL	Chip Enable Pulse Positive Width	150		120	100		ns	④
	TAVEL	Address Setup Time	20		20	0		ns	④
	TELAX	Address Hold Time	50		50	20		ns	④
	TWLWH	Write Enable Pulse Width	350		300	200		ns	④
	TWLEH	Write Enable Pulse Setup Time	350		300	200		ns	④
	TELWH	Write Enable Pulse Hold Time	350		300	200		ns	④
	TDVWH	Data Setup Time	250		220	150		ns	④
	TWHDZ	Data Hold Time	0		0	0		ns	④
	TWHEL	Write Enable Read Setup Time	0		0	0		ns	④
	TDVWL	Output Data Valid to Write Time	0		0	0		ns	④
	TWLDV	Write Data Delay Time	100		80	50		ns	④
	TWLEL	Early Output High-Z Time	0		0	-10		ns	④
	TEHWH	Late Output High-Z Time	0		0	-10		ns	④
	TELEL	Read or Write Cycle Time	500		420	320		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
3. Capacitance sampled and guaranteed – not 100% tested.
4. AC test conditions: Inputs – TRISE = TFALL = 20nsec; Outputs – 1 TTL load and 50pF; All timing measured at ½ VCC.

Read Cycle

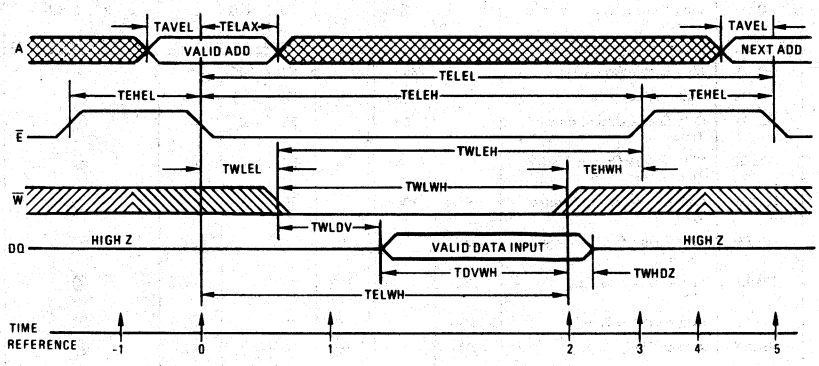


TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	DATA I/O DQ	FUNCTION
-1	H	X	X	Z	MEMORY DISABLED
0	↘	H	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	X	X	OUTPUT ENABLED
2	L	H	X	V	OUTPUT VALID
3	↗	H	X	V	READ ACCOMPLISHED
4	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The address information is latched in the on chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address setup and hold time requirements must be met. After the required hold time the addresses may change state without affecting device operation. During time (T = 1) the outputs become enabled but data is not valid until time (T = 2). $\overline{W}$ must remain high throughout the read cycle. After the data has been read $\overline{E}$ may return high (T = 3). This will force the output buffers into a high impedance mode at time (T = 4). The memory is now ready for the next cycle.

Write Cycle



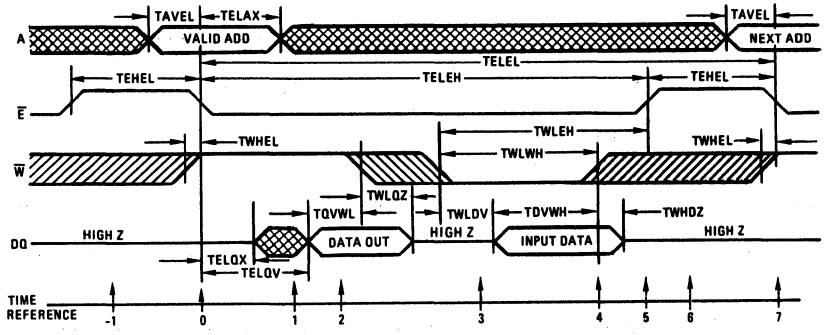
TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	DQ	FUNCTION
-1	H	X	X	Z	MEMORY DISABLED
0	↘	X	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	L	X	Z	WRITE PERIOD BEGINS
2	L	↗	X	V	DATA IN IS WRITTEN
3	↗	H	X	Z	WRITE COMPLETED
4	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	X	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The write cycle is initiated on the falling edge of $\overline{E}$ (T = 0), which latches the address information in on chip registers. If a dedicated write cycle is to be performed and the outputs are not to become active TWLEL and TEHWH must be met. Under these conditions TWLDV is unnecessary and input data may be applied at any convenient time as long as TDVWH is still met. If TWLEL is not met then the outputs may become enabled momentarily near the beginning of the cycle and a disable time (TELQZ) must be met before the input data is applied (TWLQZ = TWLDV). Similiarly, if TEHWH is not met the outputs may enable briefly near the end of the cycle.

The write operation is terminated by the first rising edge of $\overline{W}$ (T = 2) or $\overline{E}$ (T = 3). After the minimum required $\overline{E}$ high time (TEHEL) the next cycle may begin. If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may be held low until all desired locations have been written. In this case, data setup and hold times must be referenced to the rising edge of $\overline{E}$.

Read Modify Write Cycle



TRUTH TABLE

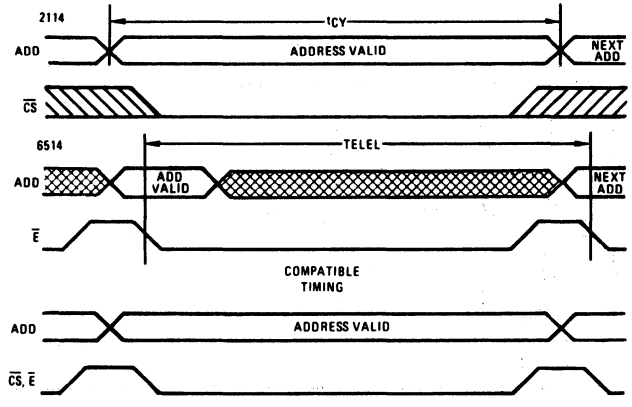
TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	DATAI/O DQ	FUNCTION
-1	H	X	X	Z	MEMORY DISABLED
0	↘	H	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	X	X	READ MODE, OUTPUT ENABLED
2	L	H	X	V	READ MODE, OUTPUT VALID
3	L	L	X	Z	WRITE MODE, OUTPUT HIGH Z
4	L	↘	X	V	WRITE MODE, DATA IS WRITTEN
5	↘	H	X	Z	WRITE COMPLETED
6	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
7	↗	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

If the pulse width of $\overline{W}$ is relatively short in relation to that of $\overline{E}$ a combination read-write cycle may be performed. If $\overline{W}$ remains high for the first part of the cycle, the outputs will become active during time (T = 1). Data out will be valid during time (T = 2). After the data is read, $\overline{W}$ can go low. After minumum TWLWH, $\overline{W}$ may return high. The information just written may now be read or $\overline{E}$ may return high, disabling the output buffers and preparing the device for the next cycle. Any number or sequence of read-write operations may be performed while $\overline{E}$ is low providing all timing requirements are met.

NOTES:

In the above descriptions the numbers in parenthesis (T = n) refer to the respective timing diagrams. The numbers are located on the time reference line below each diagram. The timing diagrams shown are only examples and are not the only valid method of operation.

2114 Compatibility



2114 — Requires the Address to Remain Valid Throughout the Cycle.

6514 — Requires Valid Address for Only a Small Portion of the Cycle, but Requires $\overline{E}$ tc Fall to Initiate Each Cycle.

Battery Backup Applications

The HM-6514 is especially well suited for use in battery backup systems. Data retention supply voltage and supply current are guaranteed over the full temperature range.

When designing the backup system, the following suggestions should be considered:

1.) As RAM VCC drops, the input logical one voltages should follow so as not to exceed VCC +0.3. It is suggested to use CMOS drivers, operating at CMOS VCC, such as the HD-6495, HD-6432, and HD-6433. Another approach is the use of open collector or open drain buffers pulled up to CMOS VCC.

2.) $\overline{E}$ must be held high at CMOS VCC. $\overline{W}$, address and data inputs should be held at either GND or CMOS VCC to minimize power dissipation.

3.) When exiting from the battery backup mode, VCC should ramp without ring or discontinuities.

4.) The RAM can begin operation one TEHEL after VCC reaches the minimum operating voltage (4.5 or 4.75 volts).

A very simple battery backup system is shown in Figure 1. When system power is available, diode D1 is forward biased and supplies current to the CMOS devices. Upon loss of system power, diode D1 is reverse biased and only CMOS devices are consuming battery power. A disadvantage to this method is that CMOS VCC is one diode drop, .7V, below TTL VCC. There is a possibility that a TTL output signal could rise higher than CMOS VCC and cause possible latch problems. This possibility can be reduced by incorporating a system similar to that shown in Figure 2. Other alternatives include using a germanuin diode yielding a VF $\approx$.2V or adding diode D2 in the TTL supply and raising VCC to account for the drop. A PNP transistor is substituted for the diode in Figure 2. The saturation drop of the transistor, 0.2V, is less than the 0.7V drop of the diode giving more margin against latch-up. A power fail output signal is available to disable the $\overline{E}$ circuitry. Open collector TTL with pullups to CMOS VCC or LS type TTL should be used as memory drivers. This will insure that the CMOS inputs are not floating during the backup period. When system power is restored, operation continues as normai and the NI-CAD battery pack is trickle charged through RC.

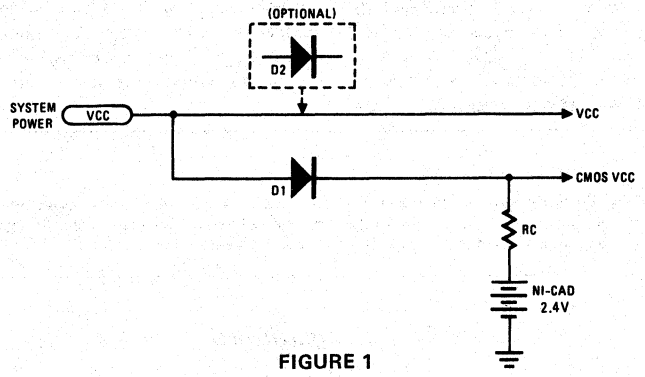


FIGURE 1

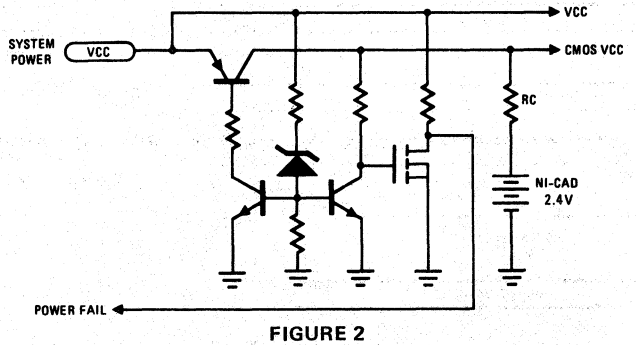


FIGURE 2

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-6518

1024 x 1 CMOS RAM

JULY 1978

Features

- LOW STANDBY POWER . . . . . 55μW MAX
- LOW OPERATING POWER . . . . . 22mW/MHz MAX
- FAST ACCESS TIME . . . . . 180nsec MAX
- DATA RETENTION VOLTAGE . . . . . 2.0 VOLTS MIN
- TTL COMPATIBLE IN/OUT
- HIGH OUTPUT DRIVE - 2 TTL LOADS
- HIGH NOISE IMMUNITY
- ON CHIP ADDRESS REGISTER
- TWO CHIP SELECTS FOR EASY ARRAY EXPANSION
- THREE STATE OUTPUTS
- MILITARY TEMPERATURE RANGE
- INDUSTRIAL TEMPERATURE RANGE

Description

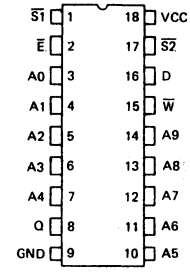
The HM-6518 is a 1024 by 1 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

On chip latches are provided for address and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

The HM-6518 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

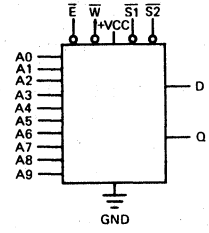
Pinout

TOP VIEW

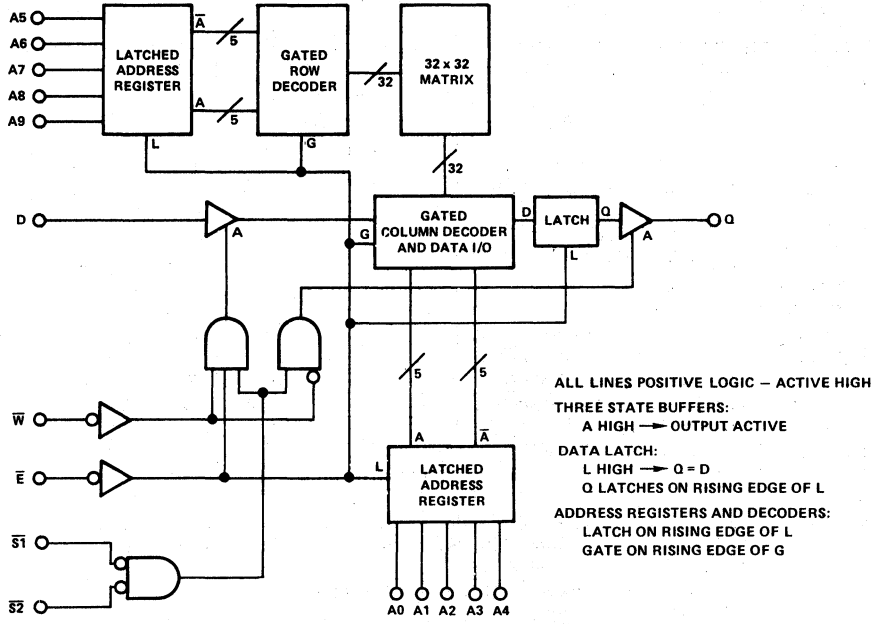


A - ADDRESS INPUT
E - CHIP ENABLE
S - CHIP SELECT
W - WRITE ENABLE
D - DATA INPUT
Q - DATA OUTPUT

Logic Symbol



Functional Diagram



ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage -VCC	+8.0V	Operating Supply Voltage -VCC	
		Military (-2)	4.5V to 5.5V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V	Industrial (-9)	4.5V to 5.5V
		Operating Temperature	
Storage Temperature	-65°C to +150°C	Military (-2)	-55°C to +125°C
		Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MIN	TEMP. = 25°C ① VCC = 5.0V TYP	TEMP. = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		10 1(+25°C)		0.1	1	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4		1.5	2.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		10		0.01	1	μA	VCC = 3.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		2.0	1.4		V	
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 3.2mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -0.4mA
	CI	Input Capacitance ③		6		4	6	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10		6	10	pF	VO= VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		180		100	140	ns	④
	TAVQV	Address Access Time		180		90	140	ns	④
	TSLQX	Chip Select Output Enable Time		120		40	80	ns	④
	TWLQX	Write Enable Output Disable Time		120		40	80	ns	④
	TSHQX	Chip Select Output Disable Time		120		40	80	ns	④
	TELEH	Chip Enable Pulse Negative Width	180		140	100		ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		80	50		ns	④
	TAVEL	Address Setup Time	0		0	-10		ns	④
	TELAX	Address Hold Time	40		30	20		ns	④
	TDVWH	Data Setup Time	80		50	30		ns	④
	TWHDX	Data Hold Time	0		0	0		ns	④
	TWLSH	Chip Select Write Pulse Setup Time	100		80	50		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	100		80	50		ns	④
	TSLWH	Chip Select Write Pulse Hold Time	100		80	50		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	100		80	50		ns	④
	TWLWH	Write Enable Pulse Width	100		80	50		ns	④
	TELEL	Read or Write Cycle Time	280		220	150		ns	④

NOTES
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — 1 TTL load and 50pF. All timing measurements at 1/2 VCC.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage -VCC	+8.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage -VCC	
Military (-2)	4.5V to 5.5V
Industrial (-9)	4.5V to 5.5V
Operating Temperature	
Military (-2)	-55°C to +125°C
Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MIN	TEMP. = 25°C ① VCC = 5.0V TYP	TEMP. = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		10 1(+25°C)		1.0	1	µA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4		1.5	2.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		10		0.1	1	µA	VCC = 3.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		2.0	1.4		V	
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	µA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	µA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 3.2mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -0.4mA
	CI	Input Capacitance ③		6		4	6	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10		6	10	pF	VO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		250		110	200	ns	④
	TAVQV	Address Access Time		250		100	200	ns	④
	TSLQX	Chip Select Output Enable Time		160		60	130	ns	④
	TWLQX	Write Enable Output Disable Time		160		60	130	ns	④
	TSHQX	Chip Select Output Disable Time		160		60	130	ns	④
	TELEH	Chip Enable Pulse Negative Width	250		200	110		ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		80	50		ns	④
	TAVEL	Address Setup Time	0		0	-10		ns	④
	TELAX	Address Hold Time	50		40	30		ns	④
	TDVWH	Data Setup Time	110		80	50		ns	④
	TWHDX	Data Hold Time	0		0	0		ns	④
	TWLSH	Chip Select Write Pulse Setup Time	130		100	60		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	130		100	60		ns	④
	TSLWH	Chip Select Write Pulse Hold Time	130		100	60		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	130		100	60		ns	④
	TWLWH	Write Enable Pulse Width	130		100	60		ns	④
	TELEL	Read or Write Cycle Time	350		280	160		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — 1 TTL load and 50pF. All timing measurements at 1/2 VCC.

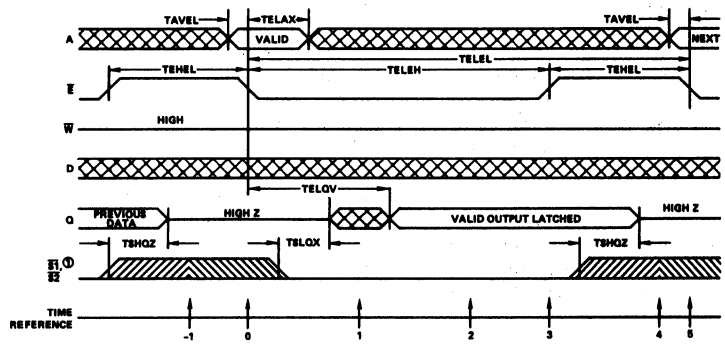
ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage -VCC	+8.0V	Operating Supply Voltage -VCC Commercial	4.75V to 5.25V
Input or Output Voltage Applied	GND -0.3V VCC +0.3V		
Storage Temperature	-65°C to +150°C	Operating Temperature Commercial	0°C to 75°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MIN	TEMP. = 25°C ① VCC = 5.0V TYP	TEMP. = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		100		10	100	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4		1.5	2.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		2.0			V	
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ⩽ VI ⩽ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ⩽ VO ⩽ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 1.6mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -0.2mA
	CI	Input Capacitance ③		6		4	6	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10		6	10	pF	VO= VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		300		160	250	ns	④
	TAVQV	Address Access Time		310		160	260	ns	④
	TSLQX	Chip Select Output Enable Time		200		60	170	ns	④
	TWLQX	Write Enable Output Disable Time		200		60	170	ns	④
	TSHQX	Chip Select Output Disable Time		200		60	170	ns	④
	TELEH	Chip Enable Pulse Negative Width	300		250	160		ns	④
	TEHEL	Chip Enable Pulse Positive Width	150		130	90		ns	④
	TAVEL	Address Setup Time	10		10	0		ns	④
	TELAX	Address Hold Time	50		50	30		ns	④
	TDVWH	Data Setup Time	130		100	80		ns	④
	TWHDX	Data Hold Time	0		0	0		ns	④
	TWLSH	Chip Select Write Pulse Setup Time	160		130	100		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	160		130	100		ns	④
	TSLWH	Chip Select Write Pulse Hold Time	160		130	100		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	160		130	100		ns	④
	TWLWH	Write Enable Pulse Width	160		130	100		ns	④
	TELEL	Read or Write Cycle Time	450		380	250		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — 1 TTL load and 50pF. All timing measurements at 1/2 VCC.

Read Cycle



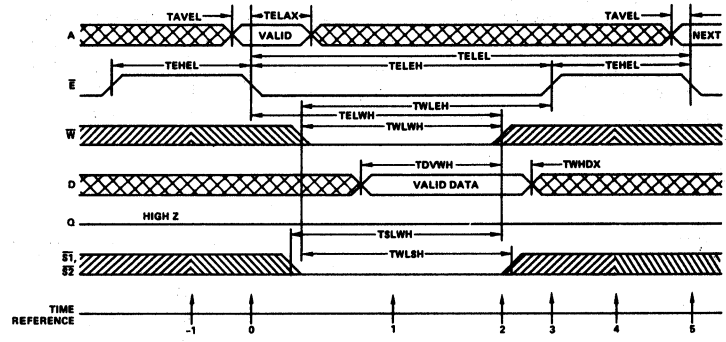
TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{S①}$	$\overline{W}$	A	D	OUTPUT Q	FUNCTION
-1	H	H	X	X	X	Z	MEMORY DISABLED
0	↘	X	H	V	X	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	L	H	X	X	X	OUTPUT ENABLED
2	L	L	H	X	X	V	OUTPUT VALID
3	↗	L	H	X	X	V	OUTPUT LATCHED
4	H	H	X	X	X	Z	DEVICE DISABLED, PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	X	H	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

NOTES: ① Device selected only if both $\overline{S1}$ and $\overline{S2}$ are low, and deselected if either $\overline{S1}$ or $\overline{S2}$ are high.

In the HM-6518 read cycle the address information is latched into the on chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address setup and hold time requirements must be met. After the required hold time the addresses may change state without affecting device operation. In order for the output to be read $\overline{S1}$, $\overline{S2}$, and $\overline{E}$ must be low, $\overline{W}$ must be high. When $\overline{E}$ goes high the output data is latched into an on chip register. Taking either or both $\overline{S1}$ or $\overline{S2}$ high forces the output buffer to a high impedance state. The output data may be re-enabled at any time by taking $\overline{S1}$ and $\overline{S2}$ low. On the falling edge of $\overline{E}$ the data will be unlatched.

Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	$\overline{S①}$	A	D	OUTPUT Q	FUNCTION
-1	H	X	X	X	X	Z	MEMORY DISABLED
0	↘	X	X	V	X	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	L	L	X	V	Z	WRITE MODE HAS BEGUN
2	L	↗	L	X	V	Z	DATA IS WRITTEN
3	↗	X	X	X	X	Z	WRITE COMPLETED
4	H	X	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	X	X	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

NOTES: ① Device selected only if both $\overline{S1}$ and $\overline{S2}$ are low, and deselected if either $\overline{S1}$ or $\overline{S2}$ are high.

The write cycle is initiated by the falling edge of $\overline{E}$ which latches the address information into the on chip registers. The write portion of the cycle is defined as $\overline{E}$, $\overline{W}$, $\overline{S1}$, and $\overline{S2}$ being low simultaneously. $\overline{W}$ may go low anytime during the cycle provided that the write enable pulse set-up time (TWLEH) is met. The write portion of the cycle is terminated by the first rising edge of either $\overline{E}$, $\overline{W}$, $\overline{S1}$ or $\overline{S2}$. Data setup and hold times must be referenced to the terminating signal.

If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may remain low until all desired locations have been written. When this method is used data setup and hold times must be referenced to the rising edge of $\overline{E}$. By positioning the $\overline{W}$ pulse at different times within the $\overline{E}$ low time (TELEH), various types of write cycles may be performed.

If the $\overline{E}$ low time (TELEH) is greater than the $\overline{W}$ pulse (TWLWH) plus an output enable time (TSLQX), a combination read-write cycle is executed. Data may be modified an indefinite number of times during any write cycle (TELEH).

The data input and data output pins may be tied together for use with a common I/O data bus structure. When using the RAM in this method allow a minimum of one output disable time (TWLQZ) after $\overline{W}$ goes low before applying input data to the bus. This will insure that the output buffers are not active.

Battery Backup Applications

The HM-6518 is especially well suited for use in battery backup systems. Data retention supply voltage and supply current are guaranteed over the full temperature range.

When designing the backup system, the following suggestions should be considered:

1.) As RAM VCC drops, the input logical one voltages should follow so as not to exceed VCC +0.3. It is suggested to use CMOS drivers, operating at CMOS VCC, such as the HD-6495, HD-6432, and HD-6433. Another approach is the use of open collector or open drain buffers pulled up to CMOS VCC.

2.) $\overline{E}$ and one of $\overline{S1}$ or $\overline{S2}$ must be held high at CMOS VCC. $\overline{W}$, address, data, and the other $\overline{S}$ should be held at GND or CMOS VCC to minimize power dissipation.

3.) When exiting from the battery backup mode, VCC should ramp without ring or discontinuities.

4.) The RAM can begin operation one TEHEL after VCC reaches the minimum operating voltage (4.5 or 4.75V).

A very simple battery backup system is shown in Figure 1. When system power is available, diode D1 is forward biased and supplies current to the CMOS devices. Upon loss of system power, diode D1 is reverse biased and only CMOS devices are consuming battery power. A disadvantage to this method is that CMOS VCC is one diode drop, .7V, below TTL VCC. There is a possibility that a TTL output signal could rise higher than CMOS VCC and cause possible latch problems. This possibility can be reduced by incorporating a system similar to that shown in Figure 2. Other alternatives include using a germanuin diode yielding a VF $\approx$ .2V or adding diode D2 in the TTL supply and raising VCC to account for the drop. A PNP transistor is substituted for the diode in Figure 2. The saturation drop of the transistor, 0.2V, is less than the 0.7V drop of the diode giving more margin against latch-up. A power fail output signal is available to disable the $\overline{E}$ circuitry. Open collector TTL with pullups to CMOS VCC or LS type TTL should be used as memory drivers. This will insure that the CMOS inputs are not floating during the backup period. When system power is restored, operation continues as normal and the NI-CAD battery pack is trickle charged through RC.

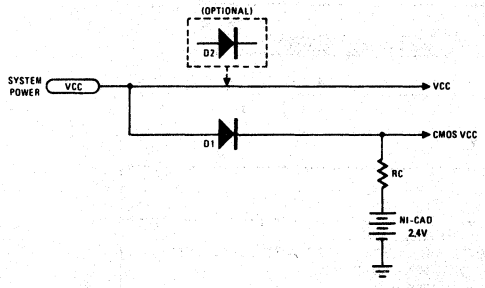


FIGURE 1

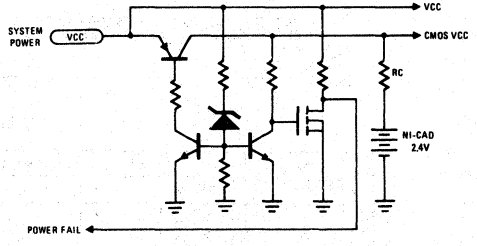


FIGURE 2

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-6533

1024 x 4 CMOS RAM

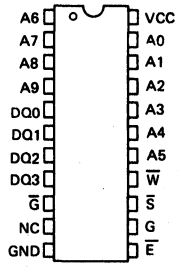
MAY 1978

Features

- LOW POWER STANDBY 1mW
- LOW POWER OPERATION. . . . . 35mW/MHz MAX
- DATA RETENTION @ 2.0 VOLTS.
- TTL COMPATIBLE INPUT/OUTPUT.
- "THREE STATE" OUTPUT.
- SEPARATE CHIP SELECT FOR EASE OF MEMORY EXPANSION.
- FULL MILITARY AND INDUSTRIAL TEMPERATURE RANGES.
- ON CHIP ADDRESS REGISTER.
- AVAILABLE IN 22 PIN DIP AND IN CHIP FORM FOR HYBRID FABRICATION.

Pinout

TOP VIEW



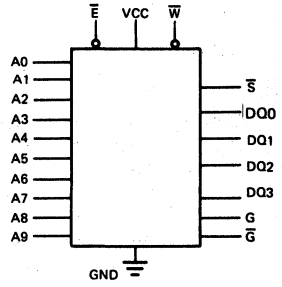
Description

The HM-6533 is a 1024 x 4 clocked static CMOS RAM designed specifically to interface with the HM-6100 Microprocessor. The device is manufactured utilizing self-aligned silicon gate technology. Extremely low power drain makes the HM-6533 an ideal candidate for battery powered systems.

On chip latching address registers and "Three State" I/O buffers enable the HM-6533 to operate in a multiplexed bus system with a minimum of support circuitry. Separate chip select and output disable pins allow for easy expansion. The output buffers can be disabled by the G, $\overline{G}$, or S pins (see Truth Table).

Wide supply voltage range and high noise immunity offer the system designer a large degree of flexability. Data retention is guaranteed down to 2.0V VCC making non-volitile memory systems simple to implement.

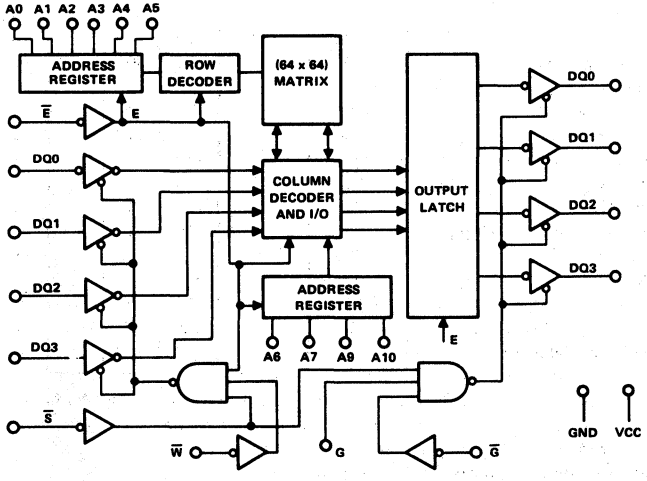
Logic Symbol



PIN NAMES

A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
DQ	Data In/Out
S	Chip Select
G	Output Enable

Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Supply Voltage-VCC	+8.0V
Applied Input or Output Voltage	GND-0.3V VCC+0.3V
Storage Temperature Range	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage-VCC	4.5V to 5.5V
Operating Temperature Range	
Military (-2)	-55°C to +125°C
Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

			VCC & TEMP = OPERATING RANGE		TEMP = 25°C VCC = 5.0V (1)				
	SYMBOL	PARAMETER	MIN	MAX	MIN	TYP	MAX	UNIT	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		100		0.1	1.0	µA	IO = 0, VI = VCC or GND
	ICCOP	Operating Current (2)		8		6	7	mA	F = 1MHz, IO = 0
	ICCDR	Data Retention Supply Current		50		1.0	5.0	µA	VCC = 3.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage		2.0		2.0	1.4	V	
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	µA	GND<VI<VCC
	IOZ	Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	µA	GND<VO<VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 2.0mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -2.0mA
	CI	Input Capacitance (3)		6		4	6	pF	VI, VIO=VCC or GND F = 1MHz
	CIO	Output Capacitance (3)		10		6	10	pF	VI, VIO=VCC or GND F = 1MHz
A.C.	TELQV	Chip Enable Access Time		400		300	350	ns	(4)
	TSLQX	Chip Select Output Enable Time		200		110	150	ns	(4)
	TSHQZ	Chip Select Output Disable Time		200		110	150	ns	(4)
	TGLQX	Output Enable Time		200		110	150	ns	(4)
	TGHQX	Output Disable Time		200		110	150	ns	(4)
	TELEL	Read or Write Cycle Time		600		475	550	ns	(4)
	TEHEL	Chip Enable Positive Pulse Width	200		200	175		ns	(4)
	TELEH	Chip Enable Negative Pulse Width	400		350	300		ns	(4)
	TAVEL	Address Setup Time	25		25	10		ns	(4)
	TELAX	Address Hold Time	75		75	60		ns	(4)
	TWLWH	Write Enable Pulse Width	220		130	110		ns	(4)
	TWLEH	Write Enable Pulse Setup Time	220		130	110		ns	(4)
	TELWH	Chip Enable Write Pulse Hold Time	220		130	110		ns	(4)
	TWLSH	Chip Select Write Pulse Setup Time	220		130	110		ns	(4)
	TSLWH	Chip Select Write Pulse Hold Time	220		130	110		ns	(4)
	TDVWH	Data Setup Time	130		100	70		ns	(4)
	TWHDX	Data Hold Time	50		50	40		ns	(4)
	TDVSH	Data to Chip Select Setup Time	130		100	70		ns	(4)
	TSHDX	Data to Chip Select Hold Time	50		50	40		ns	(4)
	TSLSH	Chip Select Write Setup Time	220		130	100		ns	(4)

NOTES:
1. All devices tested at worst case limits. Room temperature, 5V data provided for information – not guaranteed.
2. Operating supply current (ICCOP) is proportional to operating frequency. Example: Typical ICCOP = 6mA/MHz.
3. Capacitance sampled and guaranteed – not 100% tested.
4. AC test conditions: Inputs – Trise = Tfall = 20ns.
   Outputs – 1 TTL Load and 50pF.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage-VCC	+8.0V
Applied Input or Output Voltage	GND-0.3V VCC+0.3V
Storage Temperature Range	-65°C to +150°C

OPERATING RANGE

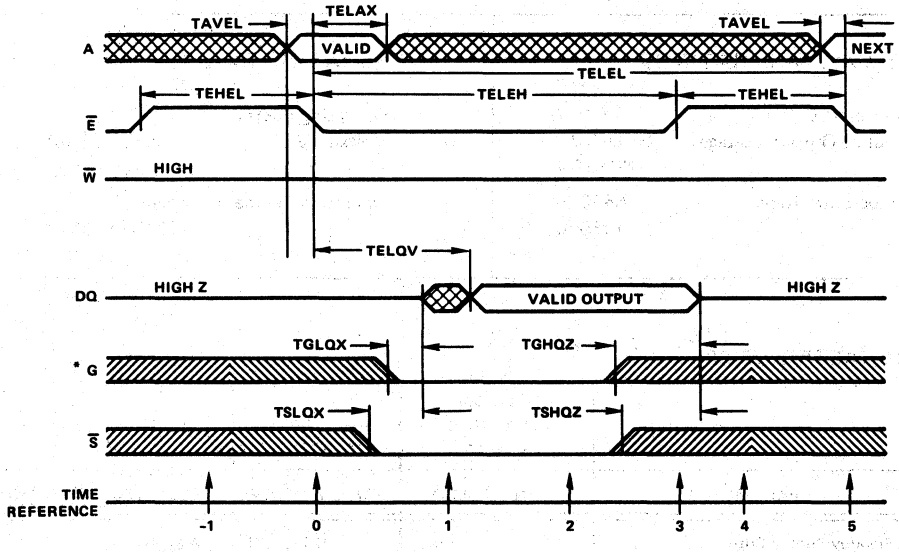
Operating Supply Voltage-VCC	4.5V to 5.5V
Operating Temperature Range	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

			VCC & TEMP = OPERATING RANGE		TEMP = 25°C VCC = 5.0V (1)				
	SYMBOL	PARAMETER	MIN	MAX	MIN	TYP	MAX	UNIT	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		1.0		0.1	1.0	mA	IO = 0, VI = VCC or GND
	ICCOP	Operating Current (2)		8		6	+7	mA	F = 1MHz, IO = 0
	II	Input Leakage Current	-10	+10		±0.5	+7	µA	GND < VI < VCC
	IOZ	Output Leakage Current	-10	+10	-7	±0.5	+7	µA	GND < VO < VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 1.6mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = --1.6mA
	CI	Input Capacitance (3)		6		4	6	pF	VI, VIO=VCC or GND F = 1MHz
	CIO	Output Capacitance (3)		10		6	10	pF	VI, VIO=VCC or GND F = 1MHz
A.C.	TELQV	Chip Enable Access Time		450		350	400	ns	(4)
	TSLQX	Chip Select Output Enable Time		300		130	180	ns	(4)
	TSHQZ	Chip Select Output Disable Time		300		130	180	ns	(4)
	TGLQX	Output Enable Time		250		130	180	ns	(4)
	TGHQX	Output Disable Time		250		130	180	ns	(4)
	TELEL	Read or Write Cycle Time	700		650	560		ns	(4)
	TEHEL	Chip Enable Positive Pulse Width	250		250	210		ns	(4)
	TELEH	Chip Enable Negative Pulse Width	450		400	350		ns	(4)
	TAVEL	Address Setup Time	50		50	30		ns	(4)
	TELAX	Address Hold Time	100		100	75		ns	(4)
	TWLWH	Write Enable Pulse Width	300		200	175		ns	(4)
	TWLEH	Write Enable Pulse Setup Time	300		200	175		ns	(4)
	TELWH	Chip Enable Write Pulse Hold Time	300		200	175		ns	(4)
	TWLSH	Chip Select Write Pulse Setup Time	300		200	175		ns	(4)
	TSLWH	Chip Select Write Pulse Hold Time	300		200	175		ns	(4)
	TDVWH	Data Setup Time	200		150	120		ns	(4)
	TWHDX	Data Hold Time	75		50	25		ns	(4)
	TDVSH	Data to Chip Select Setup Time	220		150	120		ns	(4)
	TSHDX	Data to Chip Select Hold Time	75		50	25		ns	(4)
	TSLSH	Chip Select Write Setup Time	300		200	175		ns	(4)

NOTES:
1. All devices tested at worst case limits. Room temperature, 5V data provided for information - not guaranteed.
2. Operating supply current (ICCOP) is proportional to operating frequency. Example: Typical ICCOP = 6mA/MHz.
3. Capacitance sampled and guaranteed - not 100% tested.
4. AC test conditions: Inputs – Trise = Tfall = 20ns.
   Outputs – 1 TTL Load and 50pF.

Read Cycle



*G has same timing as $\overline{G}$ except signal is inverted.

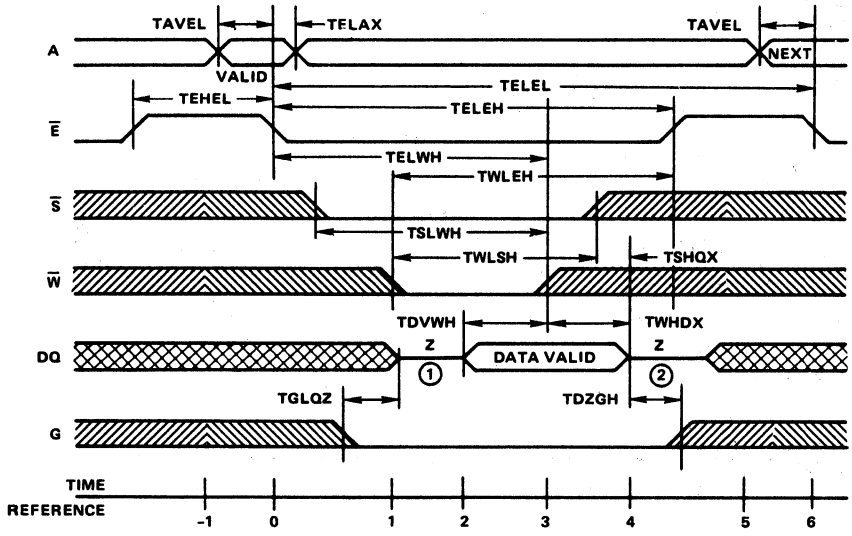
TIME REFERENCE	INPUTS $\overline{E}$	$\overline{S}$	$\overline{G}$	$\overline{W}$	A	OUTPUT DQ	FUNCTION
-1	H	H	H	X	X	Z	Memory Disabled
0	↘	H	H	H	V	Z	Cycle begins, Addresses are Latched
1	L	L	L	H	X	X	Output Enabled
2	L	L	L	H	X	V	Output Valid
3	↗	L	L	H	X	V	Output Latched
4	H	H	H	X	X	Z	Device Disabled, Prepare for next cycle (Same as -1)
5	↘	H	H	H	V	Z	Cycle ends, next cycle begins (Same as 0)

The read cycle is initiated by the falling edge of $\overline{E}$. This signal latches the input address word into on chip registers providing that minimum address setup and hold times are met. After the required hold time, the address inputs may change state without affecting device operation. For the output to be read, $\overline{G}$ and $\overline{E}$ and $\overline{S}$ must be low; $\overline{W}$ must be high. The output data will be valid at access time (TELQV) or at one output enable time (TSHQX or TGLQX), whichever is the latter occuring signal.

G and $\overline{G}$ are complementary signals which simplify the external logic required for decoding in expanded memory arrays. Either or both of these signals may be used to disable the outputs when tying several memories in an array. The HM-6533 has output data latches that are controlled by $\overline{E}$.

When $\overline{E}$ goes high the outputs are latched to contain the present data. The output buffers can be forced to a high impedance state by either $\overline{G}$ or $\overline{S}$ but the latches will only unlatch on the falling edge of $\overline{E}$.

Write Cycle



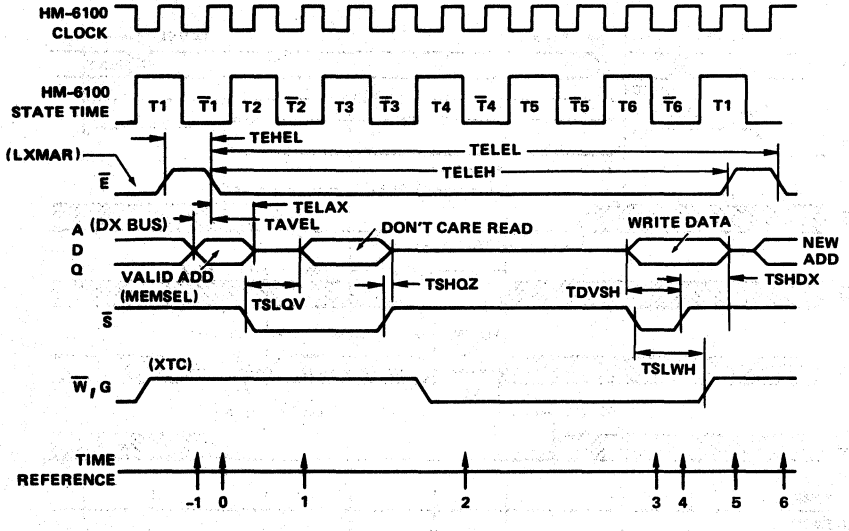
TIME REFERENCE	INPUTS Ē	S̄	G	W̄	A	I/O DQ	FUNCTION
-1	H	H	X	X	X	Z	Memory Disabled
0	↓	H	X	X	V	Z	Cycle begins, Addresses are Latched
1	L	L	L	↓	X	Z	Begin Write Operation, Output Disabled
2	L	L	L	L	X	V*	Input Data Valid
3	L	L	L	↑	X	V*	Data In is Written
4	L	H	L	H	X	Z	Input Data Gated Off
5	H	X	X	X	X	X	Memory Disabled (Same as -1)
6	↓	H	X	X	V	X	New Cycle begins (Same as 0)

As in the read mode, the write cycle is initiated by the falling edge of $\overline{E}$ which latches the addresses. The write portion of the cycle is defined as E and $\overline{W}$ being low simultaneously with $\overline{S}$ low. Since the inputs and outputs are tied together, G must be low. The write portion of the cycle is terminated on the first rising edge of $\overline{E}$, W, or $\overline{S}$. Data setup and hold times must be referenced to the terminating signal.

If a series of consecutive write cycles are to be performed, the W line may remain low until all desired locations have been written. When this method is used, data setup and hold times must be referenced to the rising edge of $\overline{E}$ or $\overline{S}$, whichever occurs first. By positioning the W pulse at different times within the $\overline{E}$ low time (TELEH) various types of write cycles may be performed.

If the $\overline{E}$ low time (TELEH) is greater than the W pulse (TWLWH) plus an output enable time (TSHQX or TGHQX) a combination read-write cycle is executed. Data may be modified an indefinite number of times during any write cycle (TELEH).

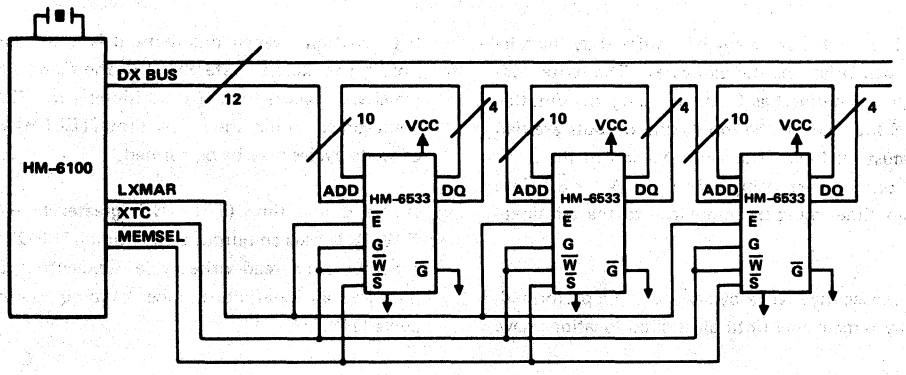
HM-6100 COMPATIBLE READ WRITE CYCLE



TRUTH TABLE

TIME REFERENCE	INPUTS						DATA I/O	FUNCTION
	$\overline{E}$	$\overline{S}$	$\overline{W}$	G	$\overline{G}$	A	DQ	
-1	H	H	H	H	L	X	Z	Memory Disabled
0	↘	H	H	H	L	V	Z	Cycle begins Addresses are Latched
1	L	L	H	H	L	X	V	Memory Output Enabled
2	L	H	H	H	L	X	Z	Memory Output Disabled
3	L	L	L	L	L	X	V	Valid Input Data present preparing to Write
4	L	↗	L	L	L	X	V	New Data Written In
5	↗	H	H	H	L	X	Z	Prepare for next cycle (Same as -1)
6	↘	H	H	H	L	V	Z	Cycle ends, next cycle begins (Same as 0)

HM-6100 1K x 12 MEMORY SYSTEM USING 3 HM-6533 RAMS



Battery Backup Applications

The HM-6533 is especially well suited for use in battery backup systems. Data retention supply voltage and supply current are guaranteed over the full temperature range.

When designing the backup system, the following suggestions should be considered:

1. As RAM VCC drops, the input logical one voltages should follow so as not to exceed VCC +0.3. It is suggested to use CMOS drivers, operating at CMOS VCC, such as the HD-6495, HD-6432, and HD-6433. Another approach is the use of open collector or open drain buffers pulled up to CMOS VCC.

2. $\overline{E}$ must be held high at CMOS VCC and $\overline{S}$, $\overline{G}$ high or G low. $\overline{W}$, $\overline{G}$, address, and data inputs should be held at either GND or CMOS VCC.

3. When exiting from the battery backup mode, VCC should ramp without ring or discontinuities.

4. The RAM can begin operation one TEHEL after VCC reaches the minimum operating voltage (4.5).

A very simple battery backup system is shown in Figure 1. When system power is available, diode D1 is forward biased and supplies current to the CMOS devices. Upon loss of system power, diode D1 is reversed biased and only CMOS devices are consuming battery power. A disadvantage to this method is that CMOS VCC is one diode drop .7V, below TTL VCC. There is a possibility that a TTL output signal could rise higher than CMOS VCC and cause possible latch problems. This possibility can be reduced by incorporating a system similar to that shown in Figure 2. Other alternatives include using a germanuin diode yielding a VF $\approx$ .2V or adding diode D2 in the TTL supply and raising VCC to account for the drop. A PNP transistor is substituted for the diode in Figure 2. The saturation drop of the transistor, 0.2V, is less than the 0.7V drop of the diode giving more margin against latch-up. A power fail output signal is available to disable the $\overline{E}$ circuitry. Open collector TTL with pullups to CMOS VCC or LS type TTL should be used as memory drivers. This will insure that the CMOS inputs are not floating during the backup period. When system power is restored, operation continues as normal and the NI-CAD battery pack is trickle charged through RC.

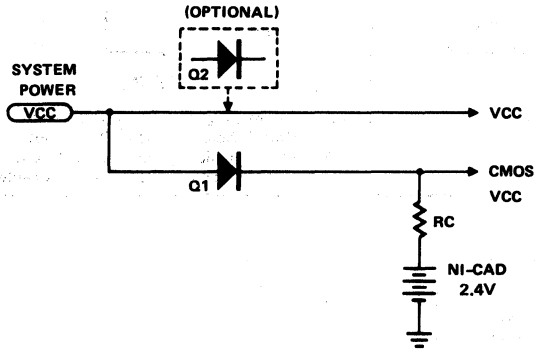


FIGURE 1

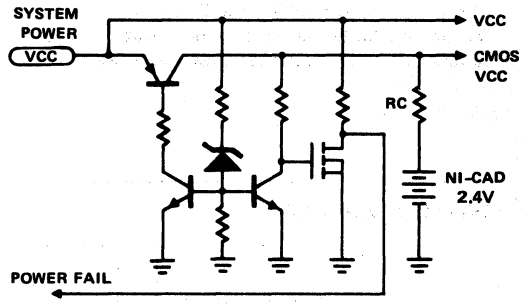


FIGURE 2

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-6543

4096 x 1 CMOS RAM

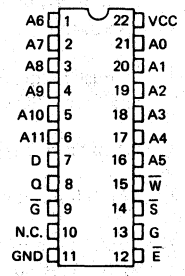
June, 1978

Features

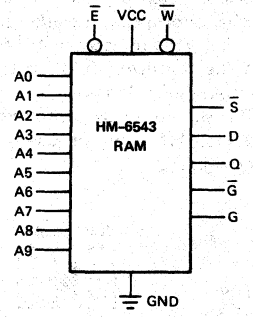
- LOW POWER STANDBY . . . . . 1mW MAX
- LOW POWER OPERATION. . . . . 35mW/MHz MAX
- DATA RETENTION . . . . . @ 2.0 VOLTS
- TTL COMPATIBLE INPUT/OUTPUT
- THREE STATE OUTPUT
- SEPARATE CHIP SELECT FOR EASE OF MEMORY EXPANSION
- FULL MILITARY AND INDUSTRIAL TEMPERATURE RANGE
- ON CHIP ADDRESS REGISTER
- AVAILABLE IN 22 PIN DIP AND IN CHIP FORM FOR HYBRID FABRICATION

Pinout

TOP VIEW



Logic Symbol



A — Address Input
$\overline{E}$ — Chip Enable
$\overline{W}$ — Write Enable
$\overline{G}$ — Output Enable
$\overline{S}$ — Chip Select
D — Data Input
Q — Data Output
G — Output Enable

Description

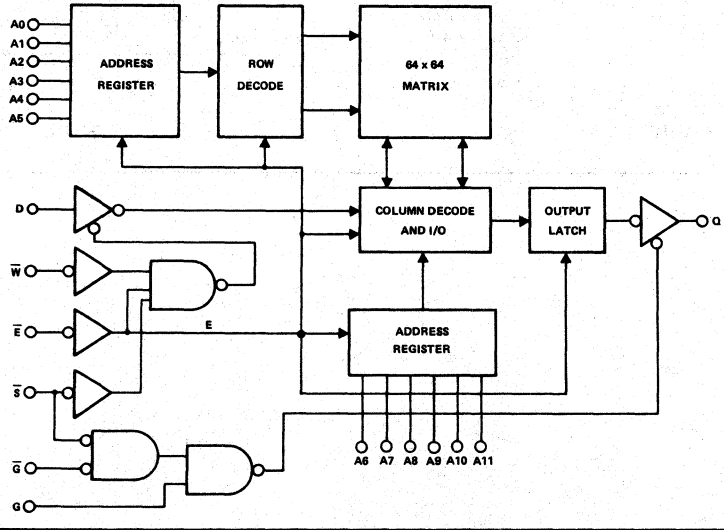
The HM-6543 is a 4096 x 1 static CMOS RAM fabricated with self-aligned silicon gate technology. The device is designed to interface directly with the HM-6100, 12 bit Microprocessor.

On chip latches are provided for addresses and output data. The chip provides a three state output buffer for ease of use on a common bus.

The HM-6543 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention, supply voltage and supply current are guaranteed over temperature.

3

Functional Diagram



ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage -VCC	+8.0V	Operating Supply Voltage -VCC	4.5V to 5.5V
Applied Input or Output Voltage	GND -0.3V to VCC +0.3V	Operating Temperature	
		Military (-2)	-55°C to +125°C
Storage Temperature	-65°C to +150°C	Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MIN	TEMP. = 25°C ① VCC = 5.0V TYP	TEMP. = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
	ICCSB	Standby Supply Current		100		2	10	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Current ②		8		6	7	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		50		1	5	μA	VCC = 3.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage		2.0		2.0	1.4	V	
D.C.	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +3.0	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 2.0mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -2.0mA
	CI	Input Capacitance ③		6		4	6	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10		6	10	pF	VO= VCC or GND f = 1MHz
	TELQV	Chip Enable Access Time		400		300	350	ns	④
	TSLQX	Chip Select Output Enable Time		200		110	150	ns	④
	TSHQZ	Chip Select Output Disable Time		200		110	150	ns	④
	TGLQX	Output Enable Time		200		110	150	ns	④
	TGHQZ	Output Disable Time		200		110	150	ns	④
	TELEL	Read or Write Cycle Time		600		475	550	ns	④
	TEHEL	Chip Enable Positive Pulse Width	200		200	175		ns	④
	TELEH	Chip Enable Negative Pulse Width	400		350	300		ns	④
A.C.	TAVEL	Address Setup Time	25		25	10		ns	④
	TELAX	Address Hold Time	75		75	60		ns	④
	TWLWH	Write Enable Pulse Width	220		130	110		ns	④
	TWLEH	Write Enable Pulse Setup Time	220		130	110		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	220		130	110		ns	④
	TWLSH	Chip Select Write Pulse Setup Time	220		130	110		ns	④
	TSWLH	Chip Select Write Pulse Hold Time	220		130	110		ns	④
	TDVWH	Data Setup Time	130		100	70		ns	④
	TWHDX	Data Hold Time	50		50	40		ns	④
	TDVSH	Data to Chip Select Setup Time	130		100	70		ns	④
	TSHDX	Data to Chip Select Hold Time	50		50	40		ns	④
	TSLSH	Chip Select Write Setup Time	220		130	100		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example Typical ICCOP = 6mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. A.C. Test Conditions: Inputs — TRISE = TFALL = 20ns; Outputs — 1TTL load and 50pF.

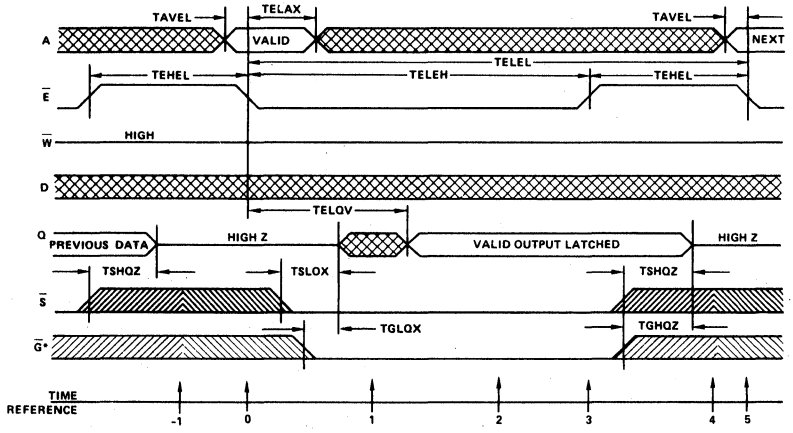
ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage -VCC	+8.0V	Operating Supply Voltage -VCC	4.5V to 5.5V
Applied Input or Output Voltage	GND -0.3V to VCC +0.3V	Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C		

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MIN	TEMP. = 25°C ① VCC = 5.0V TYP	TEMP. = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		1.0		0.1	1.0	mA	IO = 0 VI = VCC or GND
	ICCOP	Operating Current ②		8		6	7	mA	f = 1MHz, IO = 0 VI = VCC or GND
	II	Input Leakage Current	-10	+10		±0.5	+7	μA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-10	+10	-7	±0.5	+7	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +3.0	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 2.0mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -2.0mA
	CI	Input Capacitance ③		6		4	6	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10		6	10	pF	VO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		450		350	400	ns	④
	TSLQX	Chip Select Output Enable Time		300		130	180	ns	④
	TSHQZ	Chip Select Output Disable Time		300		130	180	ns	④
	TGLQX	Output Enable Time		250		130	180	ns	④
	TGHQZ	Output Disable Time		250		130	180	ns	④
	TELEL	Read or Write Cycle Time	700		560	650		ns	④
	TEHEL	Chip Enable Positive Pulse Width	250		210	250		ns	④
	TELEH	Chip Enable Negative Pulse Width	450		350	400		ns	④
	TAVEL	Address Setup Time	50		30	50		ns	④
	TELAX	Address Hold Time	100		75	100		ns	④
	TWLWH	Write Enable Pulse Width	300		175	200		ns	④
	TWLEH	Write Enable Pulse Setup Time	300		175	200		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	300		175	200		ns	④
	TWLSH	Chip Select Write Pulse Setup Time	300		175	200		ns	④
	TSLWH	Chip Select Write Pulse Hold Time	300		175	200		ns	④
	TDVWH	Data Setup Time	200		120	150		ns	④
	TWHDX	Data Hold Time	75		25	50		ns	④
	TDVSH	Data To Chip Select Setup Time	220		120	150		ns	④
	TSHDX	Data to Chip Select Hold Time	75		25	50		ns	④
	TSLSH	Chip Select Write Setup Time	300		175	200		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example Typical ICCOP = 6mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. A.C. Test Conditions: Inputs — TRISE = TFALL = 20ns; Outputs — 1TTL load and 50pF.

Read Cycle



*G Has same timing as $\overline{G}$ except signal is inverted

TRUTH TABLE

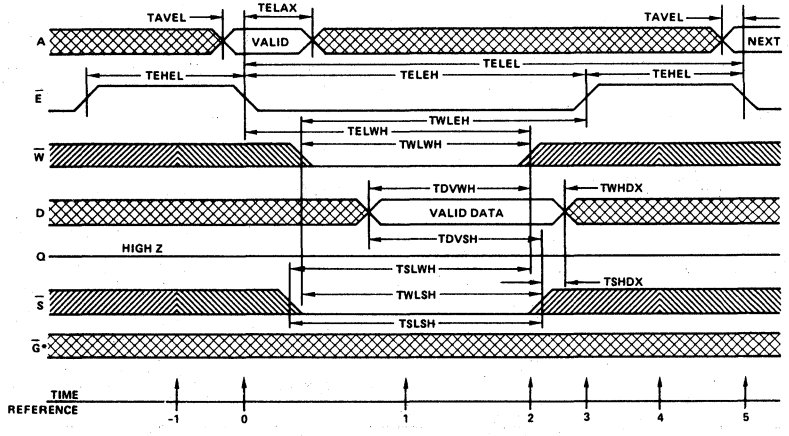
TIME REFERENCE	INPUTS $\overline{E}$	$\overline{S}$	$\overline{G}$*	$\overline{W}$	A	D	OUTPUT Q	FUNCTION
-1	H	H	H	X	X	X	Z	MEMORY DISABLED
0	↘	H	H	H	V	X	Z	CYCLE BEGINS, ADDRESS ARE LATCHED
1	L	L	L	H	X	X	X	OUTPUT ENABLED
2	L	L	L	H	X	X	V	OUTPUT VALID
3	↗	L	L	H	X	X	V	OUPUT LATCHED
4	H	H	H	X	X	X	Z	DEVICE DISABLED, PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	H	H	H	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The read cycle is initiated by the falling edge of $\overline{E}$. This signal latches the input address word into on chip registers providing that minimum address setup and hold times are met. After the required hold time, the address inputs may change state without affecting device operation. For the output to be read, $\overline{G}$ and $\overline{E}$ and $\overline{S}$ must be low; $\overline{W}$ must be high. The output data will be valid at access time (TELQV) or at one output enable time (TSLQX or TGLQX), whichever is the later occuring signal.

G and $\overline{G}$ are complementary signals which simplify the external logic required for decoding in expanded memory arrays. Either or both of these signals may be used to disable the outputs when or-tying several memories in an array. The HM-6543 has an output data latch that is controlled by $\overline{E}$.

When $\overline{E}$ goes high the outputs are latched to contain the present data. The output buffers can be forced to a high impedance state by either $\overline{G}$ or $\overline{S}$ but the latch will only unlatch on the falling edge of $\overline{E}$.

Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{S}$	$\overline{G}$	$\overline{W}$	A	D	OUTPUT Q	FUNCTION
-1	H	H	X	X	X	X	Z	MEMORY DISABLED
0	↘	X	X	X	V	X	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	L	X	↘	X	X	Z	WRITE PERIOD BEGINS
2	L	L	X	↗	X	V	Z	DATA IN IS WRITTEN
3	↗	X	X	H	X	X	Z	WRITE IS COMPLETED
4	H	H	X	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	X	X	X	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

As in the read mode, the write cycle is initiated by the falling edge of $\overline{E}$ which latches the addresses. The write portion of the cycle is defined as $\overline{E}$ and $\overline{W}$ being low simultaneously with $\overline{S}$ low.

The write portion of the cycle is terminated on the first rising edge of $\overline{E}$, $\overline{W}$, or $\overline{S}$. Data setup and hold times must be referenced to the terminating signal.

If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may remain low until all desired locations have been written. When this method is used, data setup and hold times must be referenced to the rising edge of $\overline{E}$ or $\overline{S}$, whichever occurs first. By positioning the $\overline{W}$ pulse at different times within the $\overline{E}$ low time (TELEH) various types of write cycles may be performed.

If the $\overline{E}$ low time (TELEH) is greater than the $\overline{W}$ pulse (TWLWH) plus an output enable time (TSLQX or TGLQX) a combination read-write cycle is executed. Data may be modified an indefinite number of times during any write cycle (TELEH).

COMMON I/O OPERATION

The HM-6543 is readily adaptable for use in a common I/O bus oriented system. In this mode of operation the G or $\overline{G}$ pins are used to disable the output before the input data is presented on the bus. When the chip is deselected ($\overline{S}$ high) the output is forced to the high impedance state thereby leaving the bus free to be driven from another source.

Battery Backup Applications

The HM-6543 is especially well suited for use in battery backup systems. Data retention supply voltage and supply current are guaranteed over the full temperature range.

When designing the backup system, the following suggestions should be considered:

1.) As RAM VCC drops, the input logical one voltages should follow so as not to exceed VCC +0.3. It is suggested to use CMOS drivers, operating at CMOS VCC, such as the HD-6495, HD-6432, and HD-6433. Another approach is the use of open collector or open drain buffers pulled up to CMOS VCC.

2.) $\overline{E}$ must be held high at CMOS VCC and $\overline{G}$ or $\overline{S}$ high or G low, $\overline{W}$, address and data inputs should be held at either GND or CMOS VCC to minimize power dissipation.

3.) When exiting from the battery backup mode, VCC should ramp without ring or discontinuities.

4.) The RAM can begin operation one TEHEL after VCC reaches the minimum operating voltage (4.5 or 4.75V).

A very simple battery backup system is shown in Figure 1. When system power is available, diode D1 is forward biased and supplies current to the CMOS devices. Upon loss of system power, diode D1 is reverse biased and only CMOS devices are consuming battery power. A disadvantage to this method is that CMOS VCC is one diode drop, .7V, below TTL VCC. There is a possibility that a TTL output signal could rise higher than CMOS VCC and cause possible latch problems. This possibility can be reduced by incorporating a system similar to that shown in Figure 2. Other alternatives include using a germanuin diode yielding a VF $\approx$ .2V or adding diode D2 in the TTL supply and raising VCC to account for the drop. A PNP transistor is substituted for the diode in Figure 2. The saturation drop of the transistor, 0.2V, is less than the 0.7V drop of the diode giving more margin against latch-up. A power fail output signal is available to disable the $\overline{E}$ circuitry. Open collector TTL with pullups to CMOS VCC or LS type TTL should be used as memory drivers. This will insure that the CMOS inputs are not floating during the backup period. When system power is restored, operation continues as normal and the NI-CAD battery pack is trickle charged through RC.

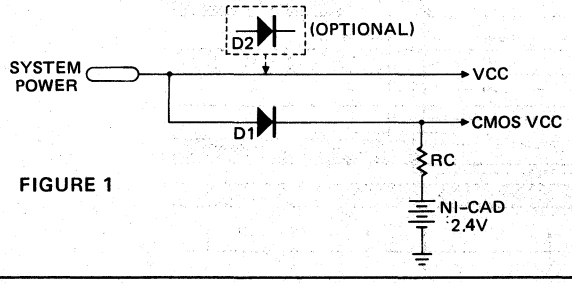


FIGURE 1

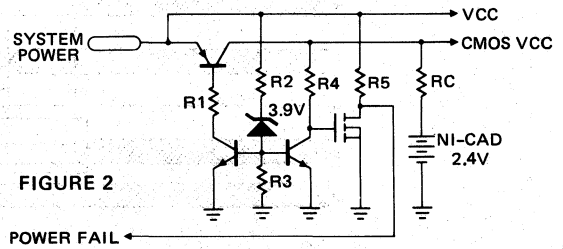
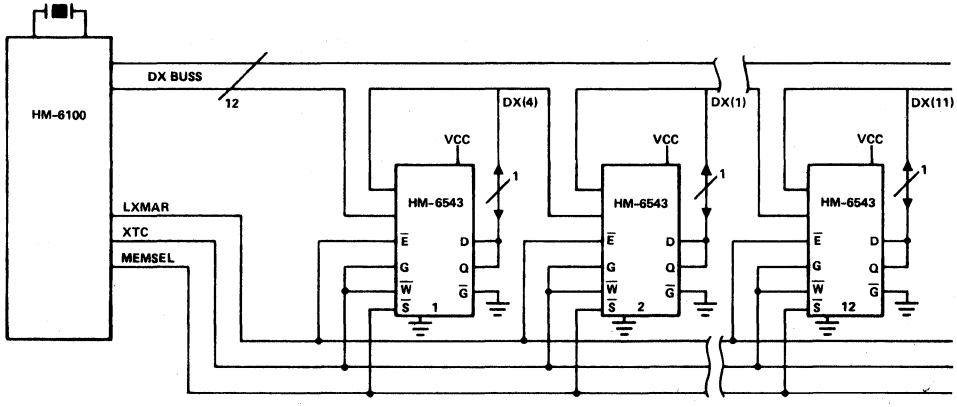
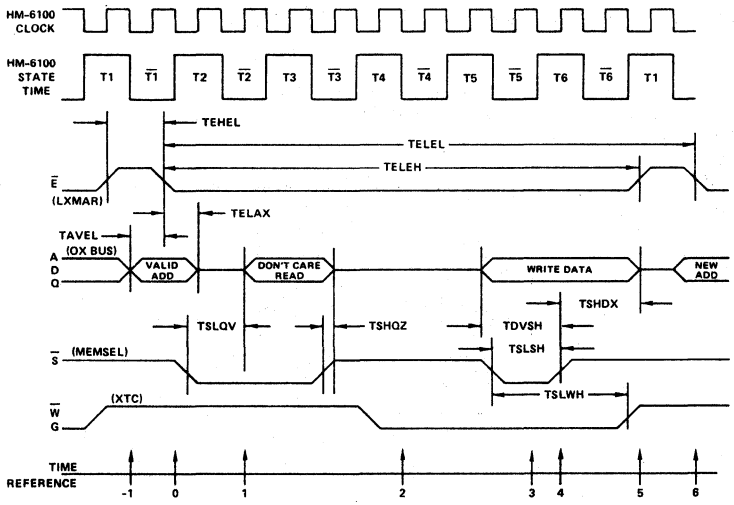


FIGURE 2

HM-6100 Memory System Using HM-6543 Memories



HM-6100 Compatabile Read Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{S}$	$\overline{W}$	G	$\overline{G}$	A	D	OUTPUT Q	FUNCTION
-1	H	H	H	H	L	X	X	Z	MEMORY DISABLED
0	↘	H	H	H	L	V	X	Z	CYCLE BEGINS, ADDRESSES LATCHED
1	L	L	H	H	L	X	X	X	MEMORY OUTPUT ENABLED
2	L	H	H	H	L	X	X	Z	MEMORY OUTPUT DISABLED
3	L	L	L	L	L	X	V	Z	VALID INPUT DATA PRESENT PREPARING TO WRITE
4	L	↘	L	L	L	X	V	Z	NEW DATA WRITTEN IN
5	↘	H	H	H	L	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
6	↘	H	H	H	L	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-6551

256 x 4 CMOS RAM

JULY 1978

Features

- LOW STANDBY POWER . . . . . 55μW MAX
- LOW OPERATING POWER. . . . . 22mW/MHz MAX
- FAST ACCESS TIME . . . . . 220nsec MAX
- DATA RETENTION VOLTAGE . . . . . 2.0 VOLTS MIN
- TTL COMPATIBLE IN/OUT
- HIGH OUTPUT DRVIE – 2 TTL LOADS
- INTERNAL LATCHED CHIP SELECT
- HIGH NOISE IMMUNITY
- ON CHIP ADDRESS REGISTERS
- LATCHED OUTPUTS
- THREE STATE OUTPUTS
- MILITARY AND INDUSTRIAL TEMPERATURE RANGES

Description

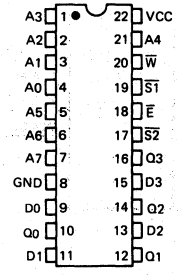
The HM-6551 is a 256 by 4 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

On chip latches are provided for addresses and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

The HM-6551 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

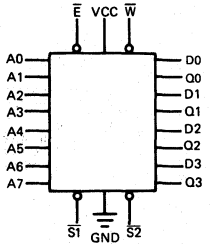
Pinout

TOP VIEW

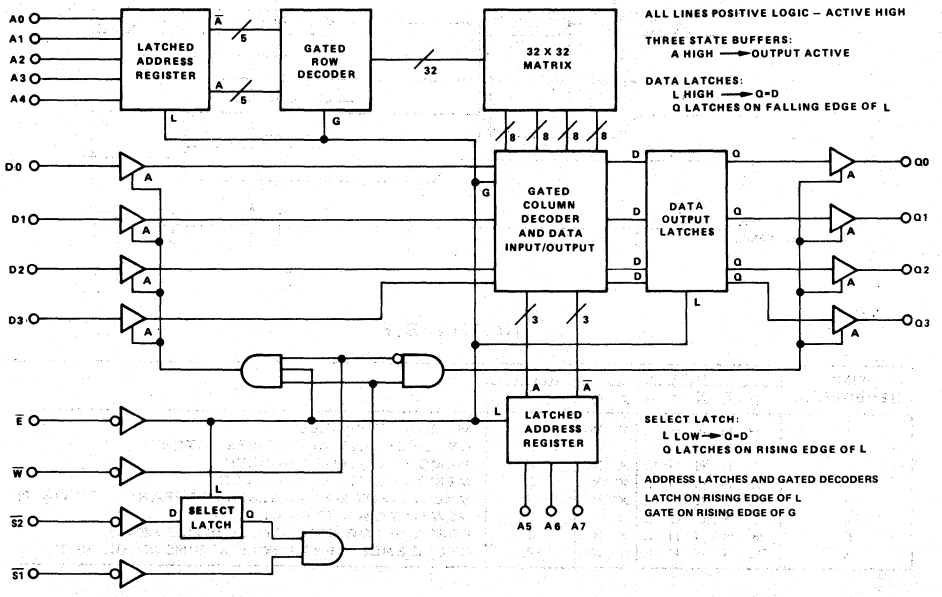


A – Address Input
E – Chip Enable
S – Chip Select
W – Write Enable
D – Data Input
Q – Data Output

Logic Symbol



Functional Diagram



ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage -VCC	+8.0V	Operating Supply Voltage -VCC	
Applied Input or Output Voltage	GND -0.3V VCC +0.3V	Military (-2)	4.5V to 5.5V
		Industrial (-9)	4.5V to 5.5V
Storage Temperature	-65°C to +150°C	Operating Temperature	
		Military (-2)	-55°C to +125°C
		Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MIN	TEMP. = 25°C ① VCC = 5.0V TYP	TEMP. = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
	ICCSB	Standby Supply Current		10 1(+25°C)		0.1	1	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4		1.5	25	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		10		0.01	1	μA	VCC = 3.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		2.0	1.4		V	
D.C.	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 3.2mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -0.4mA
	CI	Input Capacitance ③		6		4	6	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10		6	10	pF	VO= VCC or GND f = 1MHz
	TELQV	Chip Enable Access Time		220		120	170	ns	④
	TAVQV	Address Access Time		220		110	170	ns	④
	TS1LQX	Chip Select 1 Output Enable Time		130		50	90	ns	④
	TWLQZ	Write Enable Output Disable Time		130		50	90	ns	④
	TS1HQZ	Chip Select 1 Output Disable Time		130		50	90	ns	④
	TELEH	Chip Enable Pulse Negative Width	220		170	120		ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		70	50		ns	④
	TAVEL	Address Setup Time	0		0	-10		ns	④
A.C.	TS2LEL	Chip Select 2 Setup Time	0		0	-10		ns	④
	TELAX	Address Hold Time	40		40	20		ns	④
	TELS2X	Chip Select 2 Hold Time	40		40	20		ns	④
	TDVWH	Data Setup Time	100		80	50		ns	④
	TWHDX	Data Hold Time	0		0	0		ns	④
	TWLS1H	Chip Select 1 Write Pulse Setup Time	120		100	60		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	120		100	60		ns	④
	TS1LWH	Chip Select 1 Write Pulse Hold Time	120		100	60		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	120		100	60		ns	④
	TWLWH	Write Enable Pulse Width	120		100	60		ns	④
	TELEL	Read or Write Cycle Time	320		240	170		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — 1 TTL load and 50pF. All timing measurements at 1/2 VCC.

ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage -VCC	+8.0V	Operating Supply Voltage -VCC	
		Military (-2)	4.5V to 5.5V
Applied Input or Output Voltage	GND -0.3V VCC +0.3V	Industrial (-9)	4.5V to 5.5V
		Operating Temperature	
Storage Temperature	-65°C to +150°C	Military (-2)	-55°C to +125°C
		Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MIN	TEMP. = 25°C ① VCC = 5.0V TYP	TEMP. = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		10 1(+25°C)		1.0	1	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4		1.5	2.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		10		0.1	1	μA	VCC = 3.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		2.0	1.4		V	
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 3.2mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -0.4mA
	CI	Input Capacitance ③		6		4	6	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10		6	10	pF	VO= VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		300		160	240	ns	④
	TAVQV	Address Access Time		300		150	240	ns	④
	TS1LQX	Chip Select 1 Output Enable Time		150		60	120	ns	④
	TWLQZ	Write Enable Output Disable Time		150		60	120	ns	④
	TS1HQZ	Chip Select 1 Output Disable Time		150		60	120	ns	④
	TELEH	Chip Enable Pulse Negative Width	300		240	160		ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		70	50		ns	④
	TAVEL	Address Setup Time	0		0	-10		ns	④
	TS2LEL	Chip Select 2 Setup Time	0		0	-10		ns	④
	TELAX	Address Hold Time	50		40	30		ns	④
	TELS2X	Chip Select 2 Hold Time	50		40	30		ns	④
	TDVWH	Data Setup Time	150		120	100		ns	④
	TWHDX	Data Hold Time	0		0	0		ns	④
	TWLS1H	Chip Select 1 Write Pulse Setup Time	180		150	120		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	180		150	120		ns	④
	TS1LWH	Chip Select 1 Write Pulse Hold Time	180		150	120		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	180		150	120		ns	④
	TWLWH	Write Enable Pulse Width	180		150	120		ns	④
	TELEL	Read or Write Cycle Time	400		270	170		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — 1 TTL load and 50pF. All timing measurements at 1/2 VCC.

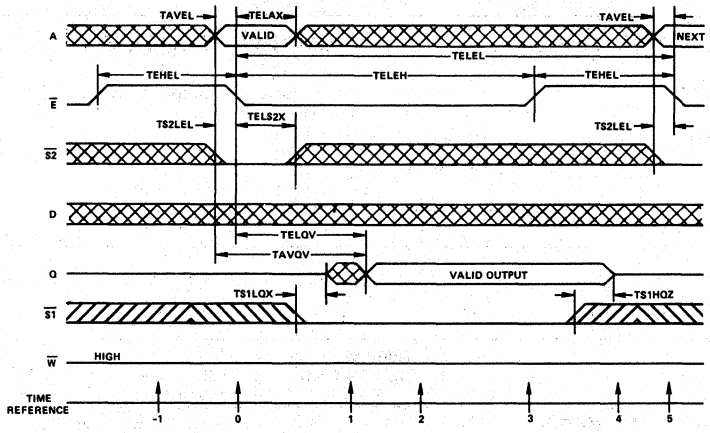
ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage -VCC	+8.0V	Operating Supply Voltage -VCC Commercial	4.75V to 5.25V
Applied Input or Output Voltage	GND -0.3V VCC +0.3V		
Storage Temperature	-65°C to +150°C	Operating Temperature Commercial	0°C to 75°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MIN	TEMP. = 25°C ① VCC = 5.0V TYP	TEMP. = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		100		10	100	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4		1.5	2.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		2.0			V	
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 1.6mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -0.2mA
	CI	Input Capacitance ③		6		4	6	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10		6	10	pF	VO= VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		350		200	300	ns	④
	TAVQV	Address Access Time		360		200	310	ns	④
	TS1LQX	Chip Select 1 Output Enable Time		180		80	160	ns	④
	TWLQZ	Write Enable Output Disable Time		180		80	160	ns	④
	TS1HQZ	Chip Select 1 Output Disable Time		180		80	160	ns	④
	TELEH	Chip Enable Pulse Negative Width	350		300	200		ns	④
	TEHEL	Chip Enable Pulse Positive Width	150		130	90		ns	④
	TAVEL	Address Setup Time	10		10	0		ns	④
	TS2LEL	Chip Select 2 Setup Time	10		10	0		ns	④
	TELAX	Address Hold Time	70		50	40		ns	④
	TELS2X	Chip Select 2 Hold Time	70		50	40		ns	④
	TDVWH	Data Setup Time	170		140	120		ns	④
	TWHDX	Data Hold Time	0		0	0		ns	④
	TWLS1H	Chip Select 1 Write Pulse Setup Time	210		170	150		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	210		170	150		ns	④
	TS1LWH	Chip Select 1 Write Pulse Hold Time	210		170	150		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	210		170	150		ns	④
	TWLWH	Write Enable Pulse Width	210		170	150		ns	④
	TELEL	Read or Write Cycle Time	500		330	290		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — 1 TTL load and 50pF. All timing measurements at 1/2 VCC.

Read Cycle



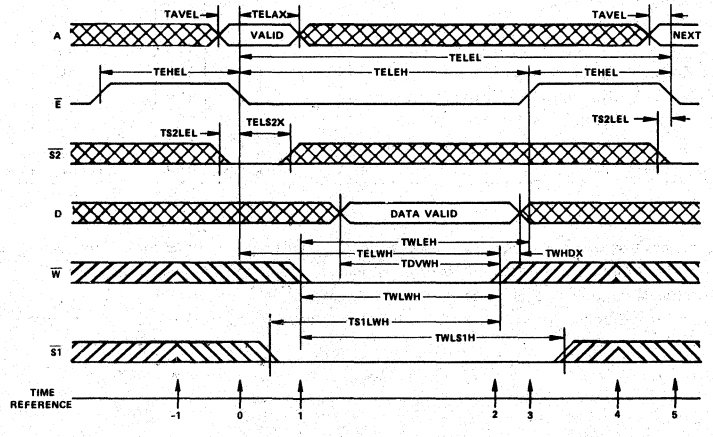
TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{S1}$	$\overline{S2}$	$\overline{W}$	A	D	OUTPUTS Q	FUNCTION
-1	H	H	X	X	X	X	Z	MEMORY DISABLED
0	↘	X	L	H	V	X	Z	ADDRESSES AND $\overline{S2}$ ARE LATCHED, CYCLE BEGINS
1	L	L	X	H	X	X	X	OUTPUT ENABLED BUT UNDEFINED
2	L	L	X	H	X	X	V	DATA OUTPUT VALID
3	↗	L	X	H	X	X	V	OUTPUTS LATCHES, VALID DATA
4	H	H	X	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	X	L	H	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The HM-6551 Read Cycle is initiated by the falling edge of $\overline{E}$. This signal latches the input address word and $\overline{S2}$ into on chip registers providing that minimum setup and hold times are met. After the required hold time, these inputs may change state without affecting device operation. $\overline{S2}$ acts as a higher order address and simplifies decoding. For the output to be read, $\overline{E}$, $\overline{S1}$ must be low and $\overline{W}$ must be high. $\overline{S2}$ must have been latched low on the falling edge of $\overline{E}$. The output data will be valid at access time (TELQV).

The HM-6551 has output data latches that are controlled by $\overline{E}$. On the rising edge of $\overline{E}$ the present data is latched and remains in that state until $\overline{E}$ falls. Either or both $\overline{S1}$ or $\overline{S2}$ may be used to force the output buffers into a high impedance state.

Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS E	S1	S2	W	A	D	OUTPUTS Q	FUNCTION
-1	H	H	X	X	X	X	Z	MEMORY DISABLED
0	↘	X	L	X	V	X	Z	CYCLE BEGINS, ADDRESSES AND $\overline{S2}$ ARE LATCHED
1	L	L	X	↘	X	X	Z	WRITE PERIOD BEGINS
2	L	L	X	↗	X	V	Z	DATA IN IS WRITTEN
3	↗	X	X	H	X	X	Z	WRITE IS COMPLETED
4	H	H	X	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	X	L	X	V	X	Z	CYCLE ENDS,.NEXT CYCLE BEGINS (SAME AS 0)

In the Write Cycle the falling edge of $\overline{E}$ latches the addresses and $\overline{S2}$ into on chip registers. $\overline{S2}$ must be latched in the low state to enable the device. The write portion of the cycle is defined as $\overline{E}$, $\overline{W}$, $\overline{S1}$ being low and $\overline{S2}$ being latched low simultaneously. The $\overline{W}$ line may go low at any time during the cycle providing that the write pulse setup times (TWLEH and TWLS1H) are met. The write portion of the cycle is terminated on the first rising edge of either $\overline{E}$, $\overline{W}$, or $\overline{S1}$.

If a series of consecutive write cycles are to be executed, the $\overline{W}$ line may be held low until all desired locations have been written. If this method is used, data setup and hold times must be referenced to the first rising edge of $\overline{E}$ or $\overline{S1}$. By positioning the write pulse at different times within the $\overline{E}$ and $\overline{S1}$ low time (TELEH) various types of write cycles may be performed. If the $\overline{S1}$ low time (TS1LS1H) is greater than the $\overline{W}$ pulse plus an output enable time (TS1LQX), a combination read-write cycle is executed. Data may be modified an indefinite number of times during any write cycle (TELEH).

The HM-6551 may be used on a common I/O bus structure by tying the input and output pins together. The multiplexing is accomplished internally by the $\overline{W}$ line. In the write cycle, when $\overline{W}$ goes low, the output buffers are forced to a high impedance state. One output disable time delay (TWLQZ) must be allowed before applying input data to the bus.

Battery Backup Applications

The HM-6551 is especially well suited for use in battery backup systems. Data retention supply voltage and supply current are guaranteed over the full temperature range.

When designing the backup system, the following suggestions should be considered:

1.) As RAM VCC drops, the input logical one voltages should follow so as not to exceed VCC +0.3. It is suggested to use CMOS drivers, operating at CMOS VCC, such as the HD-6495, HD-6432, and HD-6433. Another approach is the use of open collector or open drain buffers pulled up to CMOS VCC.

2.) $\overline{E}$ and $\overline{S1}$ must be held high at CMOS VCC. $\overline{W}$, $\overline{S2}$, address, and data inputs should be held at either GND or CMOS VCC to minimize power dissipation.

3.) When exiting from the battery backup mode, VCC should ramp without ring or discontinuities.

4.) The RAM can begin operation one TEHEL after VCC reaches the minimum operating voltage (4.5 or 4.75V).

A very simple battery backup system is shown in Figure 1. When system power is available, diode D1 is forward biased and supplies current to the CMOS devices. Upon loss of system power, diode D1 is reverse biased and only CMOS devices are consuming battery power. A disadvantage to this method is that CMOS VCC is one diode drop, .7V, below TTL VCC. There is a possibility that a TTL output signal could rise higher than CMOS VCC and cause possible latch problems. This possibility can be reduced by incorporating a system similar to that shown in Figure 2. Other alternatives include using a germanuin diode yielding a VF $\approx$ .2V or adding diode D2 in the TTL supply and raising VCC to account for the drop. A PNP transistor is substituted for the diode in Figure 2. The saturation drop of the transistor, 0.2V, is less than the 0.7V drop of the diode giving more margin against latch-up. A power fail output signal is available to disable the $\overline{E}$ circuitry. Open collector TTL with pullups to CMOS VCC or LS type TTL should be used as memory drivers. This will insure that the CMOS inputs are not floating during the backup period. When system power is restored, operation continues as normal and the NI-CAD battery pack is trickle charged through RC.

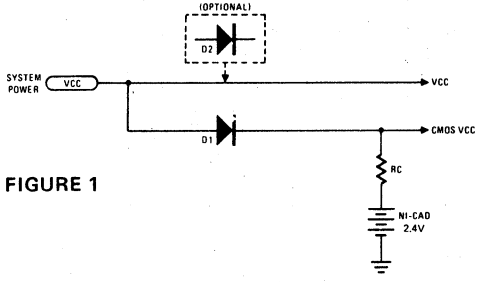


FIGURE 1

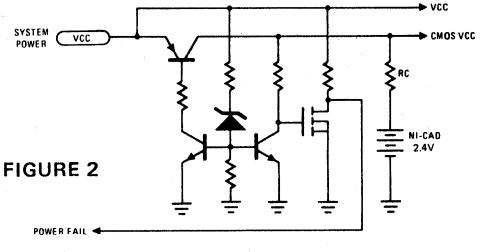


FIGURE 2

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-6561

256 x 4 CMOS RAM

JULY 1978

Features

- LOW STANDBY POWER . . . . . 55μW MAX
- LOW OPERATING POWER. . . . . 22mW/MHz MAX
- FAST ACCESS TIME . . . . . 220nsec MAX
- DATA RETENTION VOLTAGE . . . . . 2.0 VOLTS MIN
- TTL COMPATIBLE IN/OUT
- HIGH OUTPUT DRIVE – 2 TTL LOADS
- ON CHIP ADDRESS REGISTERS
- COMMON DATA IN/OUT
- THREE STATE OUTPUTS
- EASY MICROPROCESSOR INTERFACING
- MILITARY TEMPERATURE RANGE
- INDUSTRIAL TEMPERATURE RANGE

Description

The HM-6561 is a 256 by 4 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

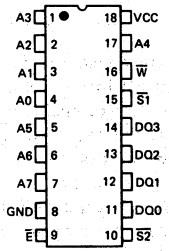
On chip latches are provided for address and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays. The data inputs and outputs are multiplexed internally for common I/O bus compatibility.

The HM-6561 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

The HM-6561 is pin for pin replaceable with the HM-6661, a 256 x 4 CMOS PROM. This allows a single memory board design with any organization of RAM and PROMs.

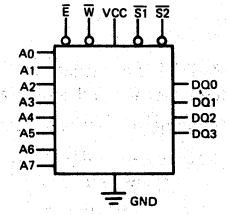
Pinout

TOP VIEW

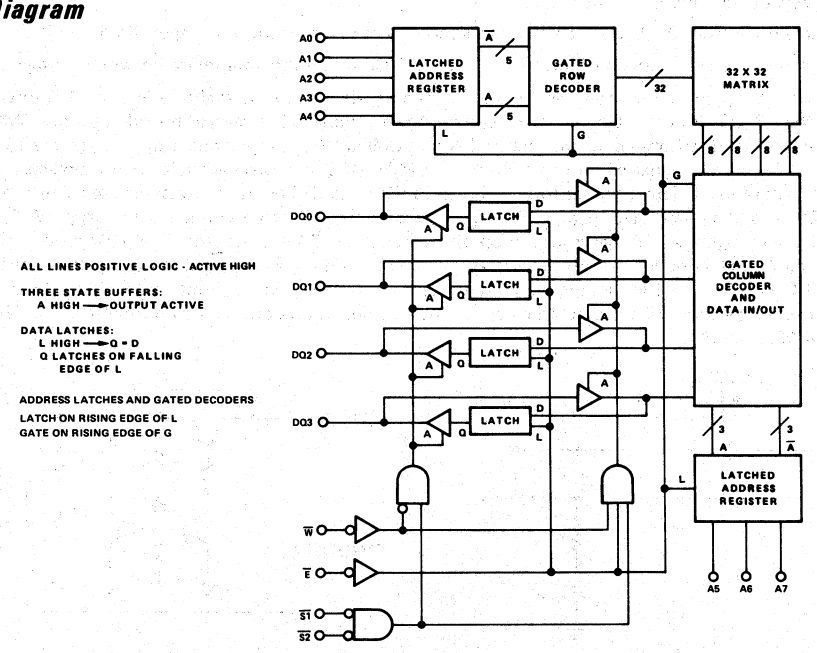


A – Address Input
E – Chip Enable
S – Chip Select
W – Write Enable
DQ – Data In/Out

Logic Symbol



Functional Diagram



ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage -VCC	+8.0V	Operating Supply Voltage -VCC	
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V	Military (-2)	4.5V to 5.5V
		Industrial (-9)	4.5V to 5.5V
Storage Temperature	-65°C to +150°C	Operating Temperature	
		Military (-2)	-55°C to +125°C
		Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MIN	TEMP. = 25°C ① VCC = 5.0V TYP	TEMP. = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		10 1(+25°C)		0.1	1	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4		1.5	2.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		10		0.01	1	μA	VCC = 3.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		2.0	1.4		V	
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 3.2mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -0.4mA
	CI	Input Capacitance ③		6		4	6	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance ③		10		6	10	pF	VO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		220		120	170	ns	④
	TAVQV	Address Access Time		220		110	170	ns	④
	TSLQX	Chip Select Output Enable Time		120		50	90	ns	④
	TWLQZ	Write Enable Output Disable Time		120		50	90	ns	④
	TSHQZ	Chip Select Output Disable Time		120		50	90	ns	④
	TELEH	Chip Enable Pulse Negative Width	220		170	120		ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		70	50		ns	④
	TAVEL	Address Setup Time	0		0	-10		ns	④
	TELAX	Address Hold Time	40		30	20		ns	④
	TDVWH	Data Setup Time	100		80	50		ns	④
	TWHDX	Data Hold Time	0		0	0		ns	④
	TWLDV	Write Data Delay Time	120		90	50		ns	④
	TWLSH	Chip Select Write Pulse Setup Time	220		170	100		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	220		170	100		ns	④
	TSLWH	Chip Select Write Pulse Hold Time	220		170	100		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	220		170	100		ns	④
	TWLWH	Write Enable Pulse Width	220		170	100		ns	④
	TWLSL	Early Output High Z Time	0		0	-10		ns	④
	TSHWH	Late Output High Z Time	0		0	-10		ns	④
	TELEL	Read or Write Cycle Time	320		230	170		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — 1 TTL load and 50pF. All timing measurements at 1/2 VCC.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage -VCC	+8.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage -VCC	
Military (-2)	4.5V to 5.5V
Industrial (-9)	4.5V to 5.5V
Operating Temperature	
Military (-2)	-55°C to +125°C
Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

			TEMP. & VCC = OPERATING RANGE		TEMP. = 25°C ① VCC = 5.0V				
	SYMBOL	PARAMETER	MIN	MAX	MIN	TYP	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		10 1(+25°C)		1.0	1	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4		1.5	2.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		10		0.1	1	μA	VCC = 3.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		2.0	1.4		V	
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 3.2mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -0.4mA
	CI	Input Capacitance ③		6		4	6	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance ③		10		6	10	pF	VO= VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		300		160	240	ns	④
	TAVQV	Address Access Time		300		150	240	ns	④
	TSLQX	Chip Select Output Enable Time		150		60	120	ns	④
	TWLQZ	Write Enable Output Disable Time		150		60	120	ns	④
	TSHQZ	Chip Select Output Disable Time		150		60	120	ns	④
	TELEH	Chip Enable Pulse Negative Width	300		240	160		ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		70	50		ns	④
	TAVEL	Address Setup Time	0		0	-10		ns	④
	TELAX	Address Hold Time	50		40	30		ns	④
	TDVWH	Data Setup Time	150		120	100		ns	④
	TWHDX	Data Hold Time	0		0	0		ns	④
	TWLDV	Write Data Delay Time	150		120	60		ns	④
	TWLSH	Chip Select Write Pulse Setup Time	300		240	160		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	300		240	160		ns	④
	TSLWH	Chip Select Write Pulse Hold Time	300		240	160		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	300		240	160		ns	④
	TWLWH	Write Enable Pulse Width	300		240	160		ns	④
	TWLSL	Early Output High Z Time	0		0	-10		ns	④
	TSHWH	Late Output High Z Time	0		0	-10		ns	④
	TELEL	Read or Write Cycle Time	400		310	210		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — 1 TTL load and 50pF. All timing measurements at 1/2 VCC.

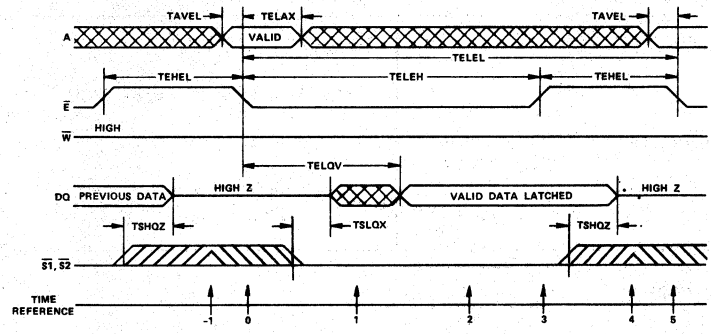
ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage -VCC	+8.0V	Operating Supply Voltage -VCC Commercial	4.75V to 5.25V
Applied Input or Output Voltage	GND -0.3V VCC +0.3V	Operating Temperature Commercial	0°C to 75°C
Storage Temperature	-65°C to +150°C		

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MIN	TEMP. = 25°C ① VCC = 5.0V TYP	TEMP. = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		100		10	100	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4		1.5	2.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		2.0			V	
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 1.6mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -0.2mA
	CI	Input Capacitance ③		6		4	6	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance ③		10		6	10	pF	VO= VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		350		200	300	ns	④
	TAVQV	Address Access Time		360		200	310	ns	④
	TSLQX	Chip Select Output Enable Time		180		80	160	ns	④
	TWLQZ	Write Enable Output Disable Time		180		80	160	ns	④
	TSHQZ	Chip Select Output Disable Time		180		80	160	ns	④
	TELEH	Chip Enable Pulse Negative Width	350		300	200		ns	④
	TEHEL	Chip Enable Pulse Positive Width	150		130	90		ns	④
	TAVEL	Address Setup Time	10		10	0		ns	④
	TELAX	Address Hold Time	70		50	40		ns	④
	TDVWH	Data Setup Time	170		140	120		ns	④
	TWHDX	Data Hold Time	0		0	0		ns	④
	TWLDV	Write Data Delay Time	200		170	60		ns	④
	TWLSH	Chip Select Write Pulse Setup Time	350		300	200		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	350		300	200		ns	④
	TSLWH	Chip Select Write Pulse Hold Time	350		300	200		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	350		300	200		ns	④
	TWLWH	Write Enable Pulse Width	350		300	200		ns	④
	TWLSL	Early Output High Z Time	0		0	-10		ns	④
	TSHWH	Late Output High Z Time	0		0	-10		ns	④
	TELEL	Read or Write Cycle Time	500		430	290		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed – not 100% tested.
4. AC Test Conditions: Inputs – TRISE = TFALL = 20nsec; Outputs – 1 TTL load and 50pF. All timing measurements at 1/2 VCC.

Read Cycle



TRUTH TABLE

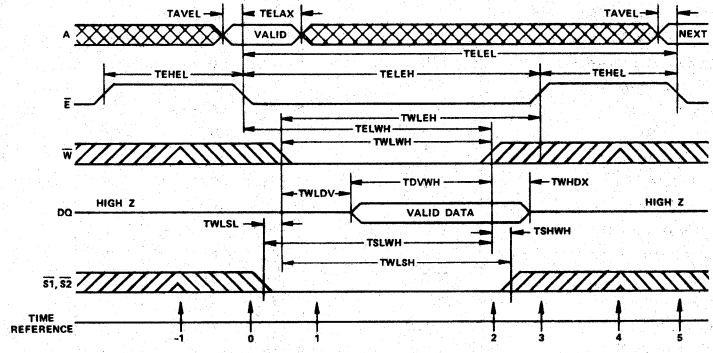
TIME REFERENCE	INPUTS Ē	S̄1	W̄	A	OUTPUT DQ	FUNCTION
-1	H	H	X	X	Z	MEMORY DISABLED
0	↘	X	H	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	L	H	X	X	OUTPUT ENABLED
2	L	L	H	X	V	OUTPUT VALID
3	↗	L	H	X	V	OUTPUT LATCHED
4	H	H	X	X	Z	DEVICE DISABLED, PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	X	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

NOTES: 1) Device selected only if both $\overline{S1}$ and $\overline{S2}$ are low, and deselected if either $\overline{S1}$ or $\overline{S2}$ are high.

The HM-6561 Read Cycle is initiated on the falling edge of $\overline{E}$. This signal latches the input address word into on chip registers. Minimum address setup and hold times must be met. After the required hold time, the address lines may change state without affecting device operation. In order to read the output data $\overline{E}$, $\overline{S1}$ and $\overline{S2}$ must be low and $\overline{W}$ must be high. The output data will be valid at access time (TELQV).

The HM-6561 has output data latches that are controlled by $\overline{E}$. On the rising edge of $\overline{E}$ the present data is latched and remains latched until $\overline{E}$ falls. Either or both $\overline{S1}$ or $\overline{S2}$ may be used to force the output buffers into a high impedance state.

Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS Ē	S̄1	W̄	A	DQ	FUNCTION
-1	H	H	X	X	Z	MEMORY DISABLED
0	↘	X	X	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	L	L	X	Z	WRITE PERIOD BEGINS
2	L	L	↗	X	V	DATA IN IS WRITTEN
3	↗	X	H	X	Z	WRITE IS COMPLETED
4	H	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	X	X	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

NOTES: 1) Device selected only if both $\overline{S1}$ and $\overline{S2}$ are low, and deselected if either $\overline{S1}$ or $\overline{S2}$ are high.

In the Write Cycle the falling edge of $\overline{E}$ latches the addresses into on chip registers. The write portion of the cycle is defined as $\overline{E}$, $\overline{W}$, $\overline{S1}$, and $\overline{S2}$ being low simultaneously. $\overline{W}$ may go low anytime during the cycle provided that the write enable pulse setup times (TWLEH and TWLSH) are met. The write portion of the cycle is terminated by the first rising edge of $\overline{E}$, $\overline{W}$, $\overline{S1}$ or $\overline{S2}$. Data setup and hold times must be referenced to the terminating signal.

If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may remain low until all desired locations have been written. When this method is used, data setup and hold times must be referenced to the first rising edge of $\overline{E}$, $\overline{S1}$, or $\overline{S2}$. By positioning the write pulse at different times within the $\overline{E}$ low time (TELEH), various types of write cycles may be performed.

If the $\overline{E}$ low time (TELEH) is greater than the $\overline{W}$ pulse (TWLWH) plus an output enable time (TWHQX), a combination read-write cycle is executed.

Data may be modified an indefinite number of times during any single write cycle (TELEH).

Data multiplexing is done internal to the chip and is controlled by $\overline{W}$. When $\overline{W}$ goes low, the output buffers are forced to a high impedance state. After one output disable time (TWLQZ) input data may be applied to the bus. If it is desired that the output buffers not become active during the write cycle, $\overline{W}$ should go low with or before $\overline{S1}$, or $\overline{S2}$ (TWLSL). It should also change to a high state after $\overline{S1}$ or S2 goes high (TSHWH). Thus, TWLSL and TSHWH may be ignored unless the system design requires that the data outputs never become active during a write cycle. If the specified TWLSL time is met, the TWLDV time may be ignored. Data may then be applied to the bus whenever convenient since the output is guaranteed not to become active.

Battery Backup Applications

The HM-6561 is especially well suited for use in battery backup systems. Data retention supply voltage and supply current are guaranteed over the full temperature range.

When designing the backup system, the following suggestions should be considered:

1.) As RAM VCC drops, the input logical one voltages should follow so as not to exceed VCC +0.3. It is suggested to use CMOS drivers, operating at CMOS VCC, such as the HD-6495, HD-6432, and HD-6433. Another approach is the use of open collector or open drain buffers pulled up to CMOS VCC.

2.) $\overline{E}$ and one of $\overline{S1}$ or $\overline{S2}$ must be held high at CMOS VCC. $\overline{W}$, address, data, and the other $\overline{S}$ should be held at GND or CMOS VCC to minimize power dissipation.

3.) When exiting from the battery backup mode, VCC should ramp without ring or discontinuities.

4.) The RAM can begin operation one TEHEL after VCC reaches the minimum operating voltage (4.5 or 4.75V).

A very simple battery backup system is shown in Figure 1. When system power is available, diode D1 is forward biased and supplies current to the CMOS devices. Upon loss of system power, diode D1 is reverse biased and only CMOS devices are consuming battery power. A disadvantage to this method is that CMOS VCC is one diode drop, .7V, below TTL VCC. There is a possibility that a TTL output signal could rise higher than CMOS VCC and cause possible latch problems. This possibility can be reduced by incorporating a system similar to that shown in Figure 2. Other alternatives include using a germanuin diode yielding a VF $\approx$ .2V or adding diode D2 in the TTL supply and raising VCC to account for the drop. A PNP transistor is substituted for the diode in Figure 2. The saturation drop of the transistor, 0.2V, is less than the 0.7V drop of the diode giving more margin against latch-up. A power fail output signal is available to disable the $\overline{E}$ circuitry. Open collector TTL with pullups to CMOS VCC or LS type TTL should be used as memory drivers. This will insure that the CMOS inputs are not floating during the backup period. When system power is restored, operation continues as normal and the NI-CAD battery pack is trickle charged through RC.

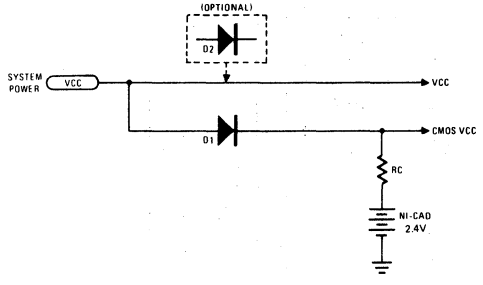


FIGURE 1

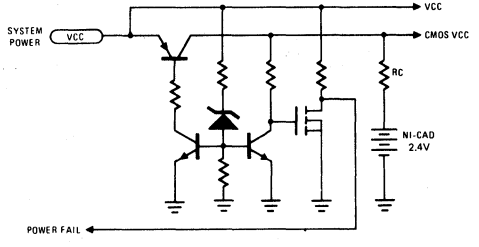


FIGURE 2

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-6562

256 x 4 CMOS RAM

JULY 1978

Features

- LOW POWER STANDBY . . . . . 55μW MAX
- LOW POWER OPERATION. . . . . 22mW/MHz MAX
- FAST ACCESS TIME . . . . . 220nsec MAX
- DATA RETENTION VOLTAGE . . . . . 2.0 VOLTS MIN
- TTL COMPATIBLE IN/OUT
- HIGH OUTPUT DRIVE – 2 TTL LOADS
- HIGH NOISE IMMUNITY
- ON CHIP ADDRESS REGISTER
- 16 PIN PACKAGE FOR HIGH DENSITY
- THREE-STATE OUTPUTS
- MILITARY TEMPERATURE RANGE
- INDUSTRIAL TEMPERATURE RANGE

Description

The HM-6562 is a 256 by 4 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

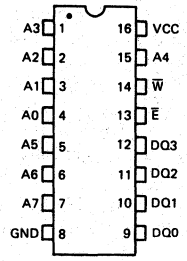
On chip latches are provided for address allowing for efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays. The data inputs and outputs are multiplexed internally for common I/O bus compatibility.

The HM-6562 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

The HM-6611, 256 x 4 CMOS PROM, is pin for pin replaceable with the HM-6562. This allows a single memory board design with any organization of RAM and PROMs.

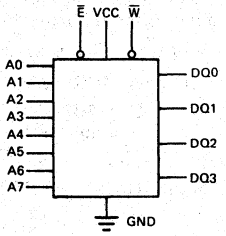
Pinout

TOP VIEW

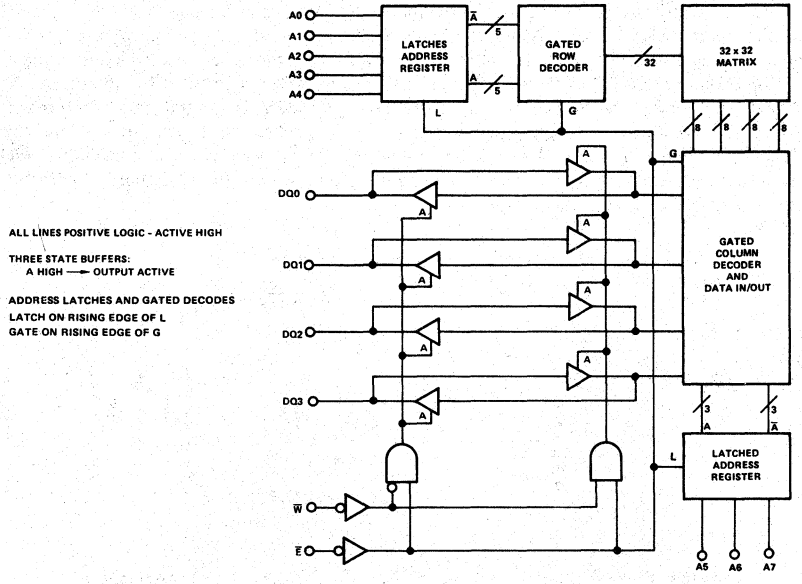


A – Address Input
E – Chip Enable
W – Write Enable
DQ – Data In/Out

Logic Symbol



Functional Diagram



ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage -VCC	+8.0V	Operating Supply Voltage -VCC	
		Military (-2)	4.5V to 5.5V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V	Industrial (-9)	4.5V to 5.5V
		Operating Temperature	
Storage Temperature	-65°C to +150°C	Military (-2)	-55°C to +125°C
		Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MIN	TEMP. = 25°C ① VCC = 5.0V TYP	TEMP. = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		10 1(+25°C)		0.1	1	µA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4		1.5	2.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		10		0.01	1	µA	VCC = 3.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		2.0	1.4		V	
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	µA	GND ≤ VI ≤ VCC
	IIOZ	Input Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	µA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +3.0	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 3.2mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -0.4mA
	CI	Input Capacitance ③		6		4	6	pF	VI = VCC or GND f = 1MHz
	CIO	Input Output Capacitance ③		10		6	10	pF	VO= VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		220		120	170	ns	④
	TAVQV	Address Access Time		220		110	170	ns	④
	TELQX	Chip Enable Output Enable Time		120		50	90	ns	④
	TWLQZ	Write Enable Output Disable Time		120		50	90	ns	④
	TEHQZ	Chip Enable Output Disable Time		120		50	90	ns	④
	TELEH	Chip Enable Pulse Negative Width	220		170	120		ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		70	50		ns	④
	TAVEL	Address Setup Time	0		0	-10		ns	④
	TELAX	Address Hold Time	40		30	20		ns	④
	TDVWH	Data Setup Time	100		80	50		ns	④
	TWHDX	Data Hold Time	0		0	0		ns	④
	TWLDV	Write Data Delay Time	120		90	50		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	220		170	100		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	220		170	100		ns	④
	TWLWH	Write Enable Pulse Width	220		170	100		ns	④
	TWLEL	Early Output High Z Time	0		0	-10		ns	④
	TEHWH	Late Output High Z Time	0		0	-10		ns	④
	TELEL	Read or Write Cycle Time	320		240	170		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — 1 TTL load and 50pF. All timing measurements at 1/2 VCC.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage -VCC	+8.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage -VCC	
Military (-2)	4.5V to 5.5V
Industrial (-9)	4.5V to 5.5V
Operating Temperature	
Military (-2)	-55°C to +125°C
Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MIN	TEMP. = 25°C ① VCC = 5.0V TYP	TEMP. = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		10 1(+25°C)		1.0	1	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4		1.5	2.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		10		0.1	1	μA	VCC = 3.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		2.0	1.4		V	
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VI ≤ VCC
	IIOZ	Input Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +3.0	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 3.2mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -0.4mA
	CI	Input Capacitance ③		6		4	6	pF	VI = VCC or GND f = 1MHz
	CIO	Input Output Capacitance ③		10		6	10	pF	VO= VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		300		160	240	ns	④
	TAVQV	Address Access Time		300		150	240	ns	④
	TELQX	Chip Enable Output Enable Time		150		60	120	ns	④
	TWLQZ	Write Enable Output Disable Time		150		60	120	ns	④
	TEHQZ	Chip Enable Output Disable Time		150		60	120	ns	④
	TELEH	Chip Enable Pulse Negative Width	300		240	160		ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		70	50		ns	④
	TAVEL	Address Setup Time	0		0	-10		ns	④
	TELAX	Address Hold Time	50		40	30		ns	④
	TDVWH	Data Setup Time	150		120	100		ns	④
	TWHDX	Data Hold Time	0		0	0		ns	④
	TWLDV	Write Data Delay Time	150		120	60		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	300		240	160		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	300		240	160		ns	④
	TWLWH	Write Enable Pulse Width	300		240	160		ns	④
	TWLEL	Early Output High Z Time	0		0	-10		ns	④
	TEHWH	Late Output High Z Time	0		0	-10		ns	④
	TELEL	Read or Write Cycle Time	400		310	210		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — 1 TTL load and 50pF. All timing measurements at 1/2 VCC.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage -VCC	+8.0V
Applied Input or Output Voltage	GND -0.3V VCC +0.3V
Storage Temperature	-65°C to +150°C

OPERATING RANGE

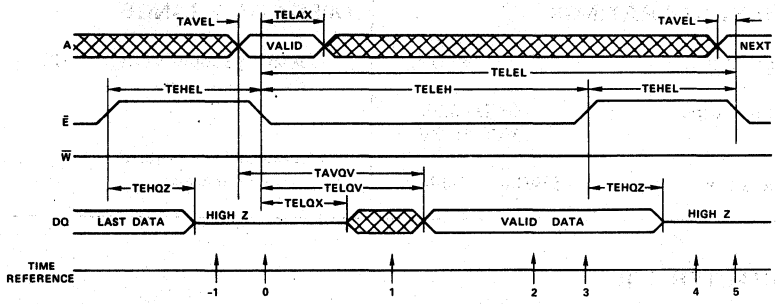
Operating Supply Voltage -VCC Commercial	4.75V to 5.25V
Operating Temperature Commercial	0°C to 75°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MIN	TEMP. = 25°C ① VCC = 5.0V TYP	TEMP. = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		100		10	100	µA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4		1.5	2.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		2.0			V	
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	µA	GND ≤ VI ≤ VCC
	IIOZ	Input Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	µA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +3.0	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 1.6mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -0.2mA
	CI	Input Capacitance ③		6		4	6	pF	VI = VCC or GND f = 1MHz
	CIO	Input Output Capacitance ③		10		6	10	pF	VO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		350		200	300	ns	④
	TAVQV	Address Access Time		360		200	310	ns	④
	TELQX	Chip Enable Output Enable Time		180		80	160	ns	④
	TWLQZ	Write Enable Output Disable Time		180		80	160	ns	④
	TEHQZ	Chip Enable Output Disable Time		180		80	160	ns	④
	TELEH	Chip Enable Pulse Negative Width	350		300	200		ns	④
	TEHEL	Chip Enable Pulse Positive Width	150		130	90		ns	④
	TAVEL	Address Setup Time	10		10	0		ns	④
	TELAX	Address Hold Time	70		50	40		ns	④
	TDVWH	Data Setup Time	170		140	120		ns	④
	TWHDX	Data Hold Time	0		0	0		ns	④
	TWLDV	Write Data Delay Time	180		160	80		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	350		300	200		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	350		300	200		ns	④
	TWLWH	Write Enable Pulse Width	350		300	200		ns	④
	TWLEL	Early Output High Z Time	0		0	-10		ns	④
	TEHWH	Late Output High Z Time	0		0	-10		ns	④
	TELEL	Read or Write Cycle Time	500		330	290		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — 1 TTL load and 50pF. All timing measurements at 1/2 VCC.

Read Cycle



TRUTH TABLE

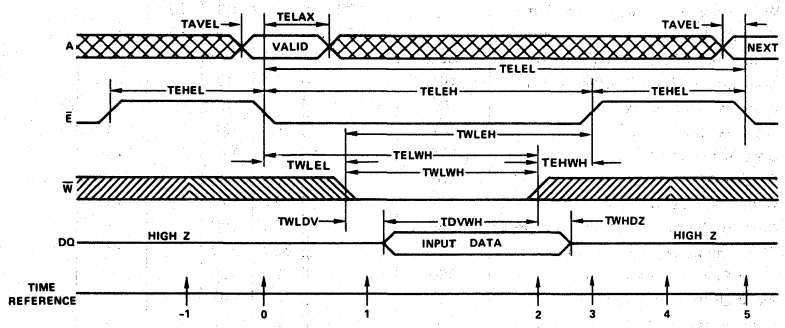
TIME REFERENCE	INPUTS Ē	W̄	A	OUTPUT DQ	FUNCTION
-1	H	X	X	Z	MEMORY DISABLED
0	↘	H	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	X	X	OUTPUT ENABLED
2	L	H	X	V	OUTPUT VALID
3	↗	H	X	V	READ ACCOMPLISHED
4	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The HM-6562 Read Cycle is initiated on the falling edge of $\overline{E}$. This signal latches the input address word into on chip registers. Minimum address setup and hold times must be met. After the required hold time, the address lines may change state without affecting device operation. In order to read the output data, $\overline{E}$ must be low and $\overline{W}$ should be high. The output data will be valid at access time.

$\overline{E}$ may be used to force the output buffers into a high impedance state.

3

Write Cycle



TIME REFERENCE	INPUTS Ē	W̄	A	DQ	FUNCTION
-1	H	X	X	Z	MEMORY DISABLED
0	↘	X	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	L	X	Z	WRITE PERIOD BEGINS
2	L	↗	X	V	INPUT DATA IS WRITTEN
3	↗	H	X	Z	WRITE COMPLETED
4	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	X	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

In the Write cycle the falling edge of $\overline{E}$ latches the addresses into on chip registers. The write portion of the cycle is defined as $\overline{E}$, and $\overline{W}$ being low simultaneously. $\overline{W}$ may go low anytime during the cycle provided that the write enable pulse setup time (TWLEH) is met. The write portion of the cycle is terminated by the first rising edge of $\overline{E}$ or $\overline{W}$. Data setup and hold times must be referenced to the terminating signal.

If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may remain low until all desired locations have been written. When this method is used, data setup and hold times must be referenced to the rising edge of $\overline{E}$. By positioning the write pulse at different times within the $\overline{E}$ low time (TELEH), various types of write cycles may be performed.

If the $\overline{E}$ low time (TELEH) is greater than the $\overline{W}$ pulse (TWLWH) plus an output enable time (TWHQX), a combination read-write cycle is executed.

Data may be modified an indefinite number of times during any single write cycle (TELEH).

Data multiplexing is done internal to the chip and is controlled by $\overline{W}$. When $\overline{W}$ goes low, the output buffers are forced to a high impedance state. After one output disable time (TWLQZ) input data may be applied to the bus. If the $\overline{W}$ falls previous to or simultaneous with $\overline{E}$, the outputs will not become active and input data may be applied to the bus whenever convenient. $\overline{W}$ should also rise simultaneous with or after $\overline{E}$ rises if it is desired not to have the outputs active during the latter portion of the cycle. Thus if TWLSEL is met TWLDV is ignored, and if TWLDV is met TWLEL is ignored.

Battery Backup Applications

The HM-6562 is especially well suited for use in battery backup systems. Data retention supply voltage and supply current are guaranteed over the full temperature range.

When designing the backup system, the following suggestions should be considered:

1.) As RAM VCC drops, the input logical one voltages should follow so as not to exceed VCC +0.3. It is suggested to use CMOS drivers, operating at CMOS VCC, such as the HD-6495, HD-6432, and HD-6433. Another approach is the use of open collector or open drain buffers pulled up to CMOS VCC.

2.) $\overline{E}$ must be held high at CMOS VCC. $\overline{W}$, address and data inputs should be held at either GND or CMOS VCC to minimize power dissipation.

3.) When exiting from the battery backup mode, VCC should ramp without ring or discontinuities.

4.) The RAM can begin operation one TEHEL after VCC reaches the minimum operating voltage (4.5 or 4.75V).

A very simple battery backup system is shown in Figure 1. When system power is available, diode D1 is forward biased and supplies current to the CMOS devices. Upon loss of system power, diode D1 is reverse biased and only CMOS devices are consuming battery power. A disadvantage to this method is that CMOS VCC is one diode drop, .7V, below TTL VCC. There is a possibility that a TTL output signal could rise higher than CMOS VCC and cause possible latch problems. This possibility can be reduced by incorporating a system similar to that shown in Figure 2. Other alternatives include using a germanuin diode yielding a VF $\approx$ .2V or adding diode D2 in the TTL supply and raising VCC to account for the drop. A PNP transistor is substituted for the diode in Figure 2. The saturation drop of the transistor, 0.2V, is less than the 0.7V drop of the diode giving more margin against latch-up. A power fail output signal is available to disable the $\overline{E}$ circuitry. Open collector TTL with pullups to CMOS VCC or LS type TTL should be used as memory drivers. This will insure that the CMOS inputs are not floating during the backup period. When system power is restored, operation continues as normal and the NI-CAD battery pack is trickle charged through RC.

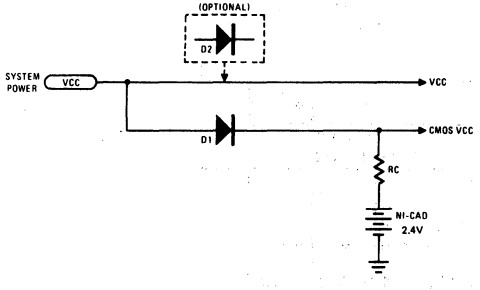


FIGURE 1

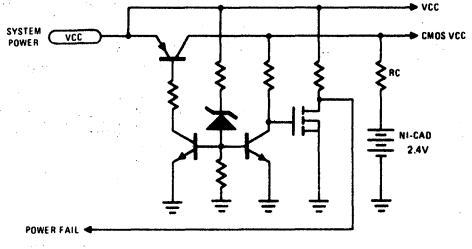


FIGURE 2

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-6611
1024-BIT FIELD PROGRAMMABLE CMOS PROM

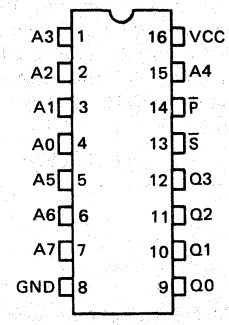
MAY 1978

Features

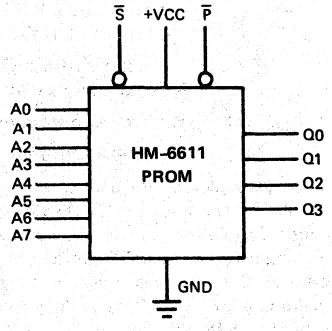
- FUSED LINK PROM
- FIELD-PROGRAMMABLE
- ORGANIZED 256 x 4
- LOW POWER STANDBY 0.1mW
- LOW POWER ENABLED 10mW
- CMOS RAM PINOUT EXCEPT FOR $\overline{P}$
- TTL COMPATIBLE IN/OUT
- THREE STATE OUTPUTS
- FULLY STATIC OPERATION
- FAST ACCESS TIME . . . . . 450nsec MAX
- HIGH NOISE IMMUNITY
- HIGH RELIABILITY
- MILITARY TEMPERATURE RANGE
- INDUSTRIAL TEMPERATURE RANGE
- 10 VOLT VERSION AVAILABLE

Pinout

TOP VIEW



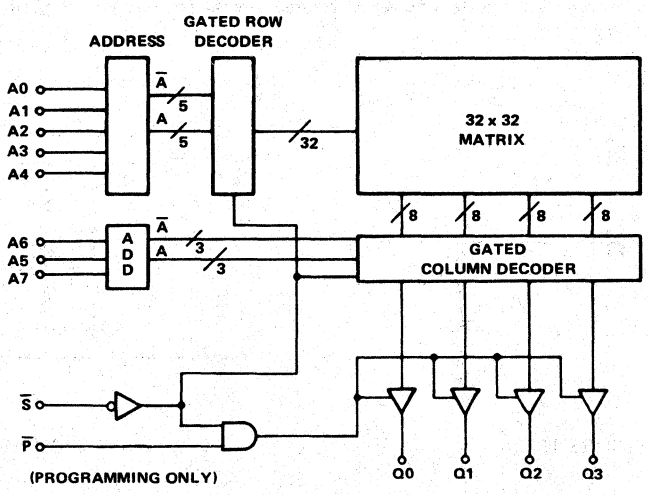
Logic Symbol



Description

The HM-6611 is a part of a family of fusible link CMOS PROMs featuring three state outputs. This device is static, TTL compatible, and has a 100 μA maximum standby current over temperature at a VCC of 5 volts. 10V and full military temperature devices are available. Chip Select ($\overline{S}$) is used to place the device in the standby state and also forces the outputs into the high impedance state when it is high. Program Enable ($\overline{P}$) is used only during programming, and must be connected to VCC in the system. Pinout is similar to Bipolar PROMs and is pin for pin replaceable with the HM-6562, a 256 x 4 CMOS RAM, if $\overline{P}$ is tied to VCC. This allows a single memory board design with any organization of RAM and PROM.

Functional Diagram



ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage - VCC	+12.0V	Operating Supply Voltage -VCC ⑥	
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V	Military (-2)	9V to 11V
		Industrial (-9)	9.5V to 10.5V
Storage Temperature	-65°C to +150°C	Operating Temperature	
		Military (-2)	-55°C to +125°C
		Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 10.0V MIN	TEMP. = 25°C ① VCC = 10.0V TYP	TEMP. = 25°C ① VCC = 10.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		500		50	200	μA	VI = VCC or GND $\overline{S}$ = VCC
	ICCEN	Enabled Supply Current ②		25		5	15	mA	VI = VCC or GND $\overline{S}$ = GND, IO = 0
	II	Input Leakage Current ③	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND≤VI≤VCC
	IOZ	Output Leakage Current	-10.0	+10.0	-5.0	±0.5	+5.0	μA	GND≤VO≤VCC
	VIL	Input Low Voltage	-0.3	1.8	-0.3	3.5	2.5	V	
	VIH	Input High Voltage	7.7	VCC + 0.3	5.5	3.5	10.3	V	
	VOL	Output Low Voltage		1.0		0.2	0.5	V	IO = 2.0mA
	VOH	Output High Voltage	8.0		8.5	9.5		V	IO = -2.0mA
	CI	Input Capacitance ③ ④		8.0		5.0	8.0	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③ ④		10.0		8.0	10.0	pF	VO = VCC or GND f = 1MHz
A.C.	TAVQV	Address Access Time		350		200	250	ns	⑤
	TSLQV	Chip Select Access Time		400		250	300	ns	⑤
	TSLQX	Chip Select Output Enable Time		70		20	50	ns	⑤
	TSHQZ	Chip Select Output Disable Time		70		20	50	ns	⑤

NOTES:

1. All devices tested at worst case limits. Room temperature 10 volt data provided for information - not guaranteed.
2. ICCEN is proportional to the number of unblown fuses per word addressed. If all four fuses in the word addressed are blown ICCEN ≈ ICCSB.
3. Except $\overline{P}$. Program Enable is used only during programming and it's characteristics are accounted for in the programming specifications.
4. Capacitance is sampled and guaranteed, but not 100% tested.
5. AC test conditions: Inputs - TRISE = TFALL = 20nsec; Outputs - 100KΩ and 50pF to ground; Timing measured at ½VCC.
6. The HM-6611A will also meet the HM-6611 specifications when operated within the HM-6611 operating range.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage - VCC	+12.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage -VCC	
Military (-2)	4.5V to 5.5V
Industrial (-9)	4.5V to 5.5V
Operating Temperature	
Military (-2)	-55°C to +125°C
Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MIN	TEMP. = 25°C ① VCC = 5.0V TYP	TEMP. = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		100		5	20	μA	VI = VCC or GND $\overline{S}$ = VCC
	ICCEN	Enabled Supply Current ②		10		2	5	mA	VI = VCC or GND $\overline{S}$ = GND, IO = 0
	II	Input Leakage Current ③	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND≤VI≤VCC
	IOZ	Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND≤VO≤VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC - 2.0	VCC + 0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.3	0.35	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		3.5	4.0		V	IO = -1.0mA
	CI	Input Capacitance ③ ④		8.0		5.0	8.0	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③ ④		10.0		6.0	10.0	pF	VO = VCC or GND f = 1MHz
A.C.	TAVQV	Address Access Time		450		300	350	ns	⑤
	TSLQV	Chip Select Access Time		500		350	400	ns	⑤
	TSLQX	Chip Select Output Enable Time		150		70	120	ns	⑤
	TSHQZ	Chip Select Output Disable Time		150		70	120	ns	⑤

NOTES:

1. All devices tested at worst case limits. Room temperature 10 volt data provided for information - not guaranteed.
2. ICCEN is proportional to the number of unblown fuses per word addressed. If all four fuses in the word addressed are blown ICCEN ≈ ICCSB.
3. Except $\overline{P}$. Program Enable is used only during programming and it's characteristics are accounted for in the programming specifications.
4. Capacitance is sampled and guaranteed, but not 100% tested.
5. AC test conditions: Inputs - TRISE = TFALL = 20nsec; Outputs - 50pF and 1TTL load; Timing measured at ½VCC.

ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage - VCC	+12.0V	Operating Supply Voltage -VCC Commercial	4.75V to 5.25V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V	Operating Temperature Commercial	0°C to 75°C
Storage Temperature	-65°C to +150°C		

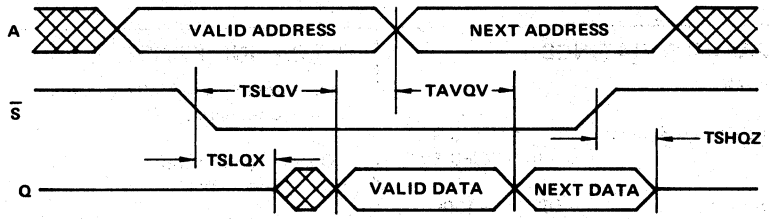
ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MIN	TEMP. = 25°C ① VCC = 5.0V TYP	TEMP. = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		1.0		0.2	1.0	mA	VI = VCC or GND $\overline{S}$ = VCC
	ICCEN	Enabled Supply Current ②		25		5	25	mA	VI = VCC or GND $\overline{S}$ = GND, IO = 0
	II	Input Leakage Current ③	-10.0	+10.0	-7.0	±0.5	+7.0	μA	GND≤VI≤VCC
	IOZ	Output Leakage Current	-10.0	+10.0	-7.0	±0.5	+7.0	μA	GND≤VO≤VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC - 2.0	VCC + 0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.3	0.35	V	IO = 1.0mA
	VOH	Output High Voltage	2.4		3.5	4.0		V	IO = -0.5mA
	CI	Input Capacitance ③ ④		8.0		5.0	8.0	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③ ④		10.0		6.0	10.0	pF	VO = VCC or GND f = 1MHz
A.C.	TAVQV	Address Access Time		650		400	550	ns	⑤
	TSLQV	Chip Select Access Time		800		500	650	ns	⑤
	TSLQX	Chip Select Output Enable Time		250		100	200	ns	⑤
	TSHQZ	Chip Select Output Disable Time		250		100	200	ns	⑤

NOTES:

1. All devices tested at worst case limits. Room temperature 10 volt data provided for information - not guaranteed.
2. ICCEN is proportional to the number of unblown fuses per word addressed. If all four fuses in the word addressed are blown ICCEN ≈ ICCSB.
3. Except $\overline{P}$. Program Enable is used only during programming and it's characteristics are accounted for in the programming specifications.
4. Capacitance is sampled and guaranteed, but not 100% tested.
5. AC test conditions: Inputs - TRISE = TFALL = 20nsec; Outputs - 50pF and 1TTL load; Timing measured at ½VCC.

Read Cycle



TRUTH TABLE

INPUTS $\overline{S}$	A	OUTPUT Q	FUNCTION
H	X	Z	DEVICE DESELECTED, OUTPUT HIGH IMPEDANCE
L	V	V	DEVICE SELECTED, DATA OUTPUT VALID FOR ADDRESS PRESENT

The timing waveforms shown describe only one possible method of operation. The device will output valid data corresponding to the address input one chip select access time (TSLQV) after it is selected. If the device is already selected and the address is changed to a new valid address the corresponding data will be available at the outputs no later than one address access time (TAVQV) later. Thus this device can be selected each time a data word is desired, or it can be selected to access quickly a block of data. If the system data bus allows, the device may be permanently selected for ease of use.

Programming

BACKGROUND INFORMATION

The HM-6611 is a 256 x 4 CMOS Programmable Read-Only Memory. It is programmed by the controlled application of programming pulses to selected memory cells. These pulses permanently alter the logic state of the memory cell. The memory array is manufactured with each cell set to the high or "1" logic state. The user may select any memory cell and permanently change its logic state to a "0" or low by programming.

Programming is accomplished by addressing the word to be programmed, applying the programming pulses, and verifying the data programmed. The verification is performed at high voltage (VCC) during the programming sequence, and at low voltage after all programming is completed.

PROGRAMMING SYSTEM CHARACTERISTICS:

1. Power source for the device to be programmed (VCC) variable from +3.0 to +11.0 volts, current capability of 500mA average and 1 amp dynamic currents.
2. Programming pulse is a negative 27.0 volt (±3.0V) pulse of 4 millisecond duration (±25%), rise and fall times of 4 to 400 microseconds, capable of 400mA average and 1 amp dynamic currents.
3. Data output load devices (switchable) capable of sinking 10mA from the output pin without rising more than 0.6 volts above ground. Open collector, open drain or discrete devices with resistive pull-ups of 4.7K to 47K is the recommended implementation.
4. Data output sensing devices capable of sensing valid logic levels (VOH $\geq$ 70% VCC, VOL $\leq$ 20% VCC).
5. Address buffers able to maintain high state voltages of $\geq$ 70% of VCC at both high and low VCC,* and low state voltages $\leq$ 20% VCC at both high and low VCC.
6. Timing and control logic suitable to sequence the required functions.

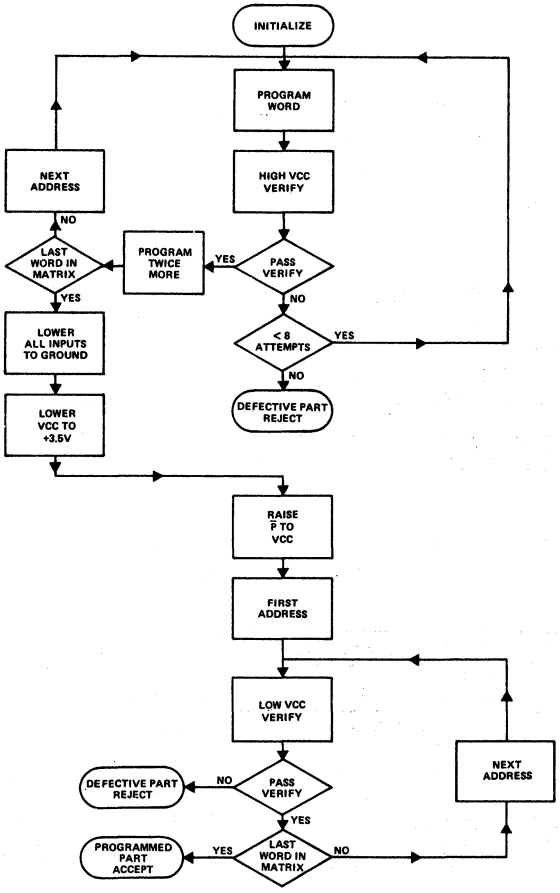
*Never allow any input to rise more than 0.3 volts above VCC.

PROGRAMMING PROCEDURE:

OVERALL:

1. Address and program word.
2. Verify data output at high VCC (10V ± 10%)
   a. If device fails to verify repeat program — verify sequence (reject device as defective after 8 programming attempts at any one word).
   b. If device passes verify repeat programming sequence twice more then return to step 1 to program the next word.
   c. If device passes verify at the last location to be programmed continue to step 3.
3. Lower VCC to 3.5 ± 0.5V and verify each location in the matrix.
   a. If any location fails to verify reject the device as defective.
   b. If all locations pass verify the part is properly programmed.

PROGRAMMING SEQUENCE FLOW CHART



PROGRAMMING STEPS:

INITIALIZE:

VCC = +10.0V ± 10%
$\overline{P}$ = VCC
$\overline{E}$ = GND (not used during programming)

1. Setup the address of the word to be programmed.
2. Wait 500 nanoseconds or more (TAVPL).
3. Initiate the negative $\overline{P}$ pulse described in System Characteristics # 2.
4. After the $\overline{P}$ pulse has crossed zero (ground) going negative, enable the data output load devices of each output pin that is to be programmed (to become a low or "0" logic state).
5. Disable the data output load 4 milliseconds (± 25%) after it was enabled (TQLQH).
6. The negative $\overline{P}$ pulse should not rise back to VCC until the data output loads are disabled.
7. Invert A0 for 500 nanoseconds, then return A0 to its original logic state to read programmed data.
8. Wait 500 nanoseconds or more (TPHQV).
9. Compare the output data with the desired data.
   a. If any one bit fails to verify, program again starting at step 3. After 8 programming attempts at any one location, reject the device as defective. It is acceptable to repulse all desired bits if any one bit does not program.
   b. If all four bits verify, apply two more programming pulses (steps 3 thru 8 twice). Then return to step 1 to address and program the next word.

After steps 1 thru 9 are completed for each word to be programmed:

10. Lower all inputs to ground.
11. Lower VCC to +3.5 volts ± .5 volts.
12. Raise $\overline{P}$ to VCC.*
13. Setup the address of the word to be verified. (High or "1" or VIH inputs must be > 2.35 and < VCC +0.3 volts).*
14. Wait 1 microsecond.
15. Compare the output data with the desired data.
    a. If any bit fails to verify, reject the device as defective.
    b. If all four bits verify, return to step 13 to verify the next word.

After steps 13 thru 15 are completed for each word in the matrix, the device has been properly programmed.

* Never allow any input to rise more than 0.3 volts above VCC.

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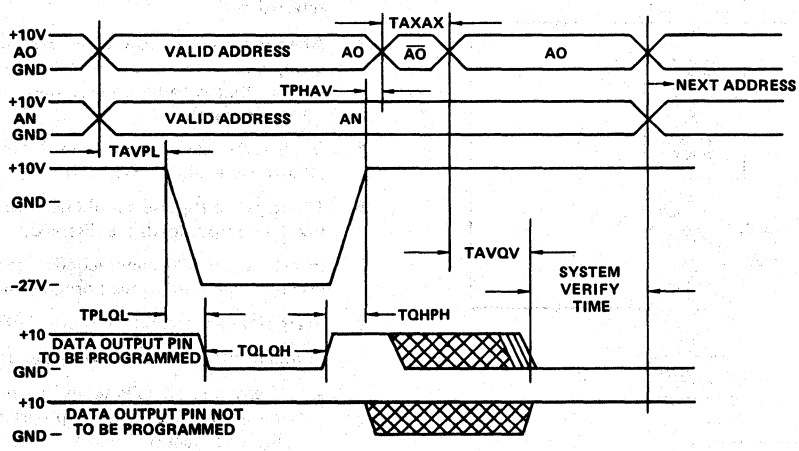
PROGRAM CYCLE TIMING TABLE

SYMBOL	PARAMETER	MIN	MAX	UNITS
TAVPL	Address to Program Setup Time	500		ns
TPLQL	Program Enable to Data Time	100		µs
TAVQV	Address to Output Valid	500		ns
TQLQH	Data Low Pulse Width	3.0	5.0	ms
TQHPH	Data High to Program Disable Time	100		µs
TAXAX	A0 Inverted Time	500		ns
TPHQV	Program Disable to Read Time	500		ns
TPHAV	Program Disable to Address Invert (A0)	0		ns

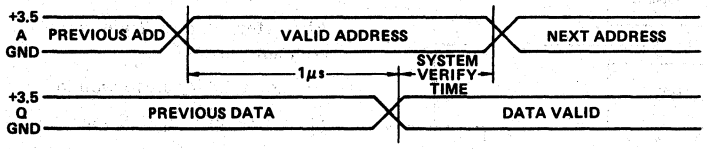
PROGRAMMING CYCLE

VCC = 10.0V ± 10%

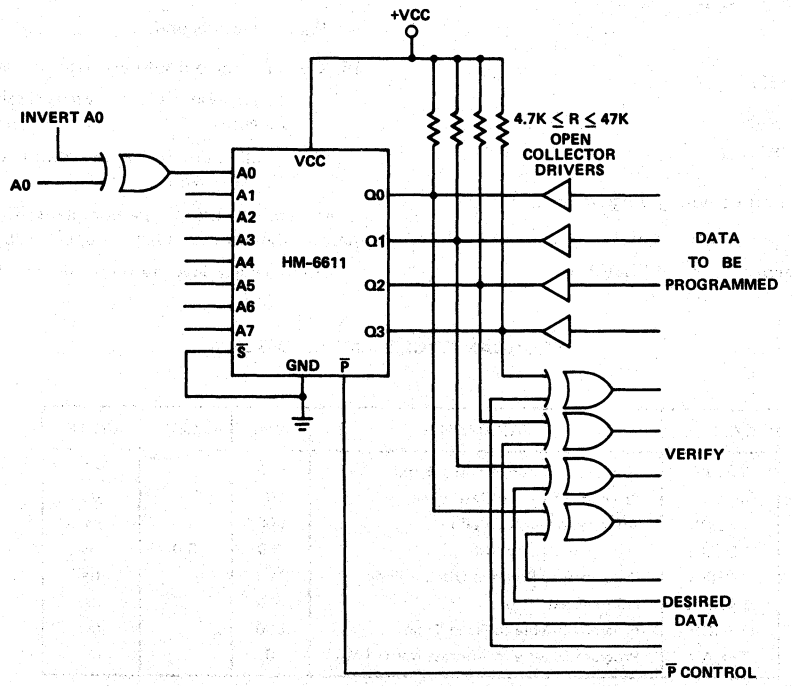


LOW VOLTAGE VERIFY CYCLE

VCC = 3.5V ± 0.5V



EXAMPLE PROGRAMMING CIRCUIT



HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-6661

1024-BIT FIELD PROGRAMMABLE CMOS PROM

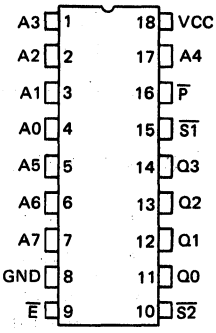
MAY 1978 ***Advance Information***

Features

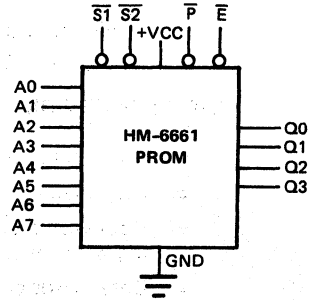
- FUSED LINK PROM
- FIELD-PROGRAMMABLE
- ORGANIZED 256 x 4
- LOW POWER STANDBY 0.1mW
- CMOS RAM PINOUT EXCEPT FOR $\overline{P}$
- TTL COMPATIBLE IN/OUT
- THREE STATE OUTPUTS
- SYNCHRONOUS OPERATION
- FAST ACCESS TIME . . . . . 450 nsec MAX
- HIGH NOISE IMMUNITY
- HIGH RELIABILITY
- MILITARY TEMPERATURE RANGE
- INDUSTRIAL TEMPERATURE RANGE
- 10 VOLT VERSION AVAILABLE

Pinout

TOP VIEW



Logic Symbol



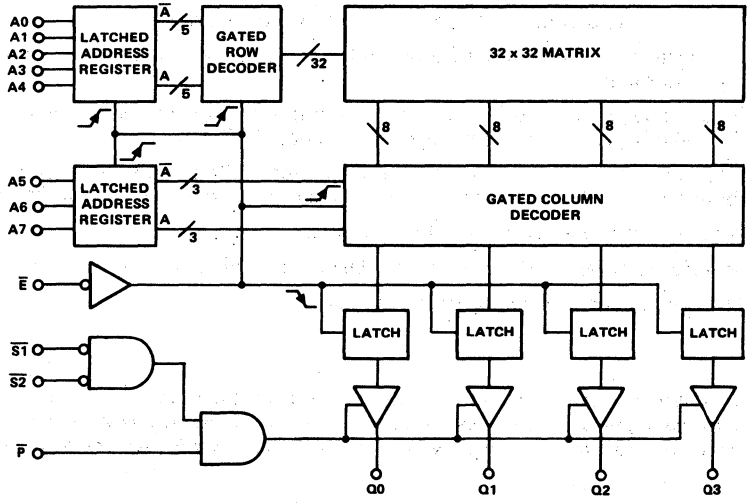
Description

The HM-6661 is a 256 x 4 static CMOS PROM fabricated using self-aligned silicon gate technology. Synchronous circuit techniques are employed to achieve high performance and low power operation.

On chip latches are provided for address and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

The HM-6661 employs polysilicon fuses as static memory elements. It is also pin for pin replaceable with the HM-6561, a 256 x 4 CMOS RAM, if P is tied to VCC. This allows a single memory board design with any organization of RAM and PROM.

Functional Diagram



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Data Entry Formats for Harris Custom Programming

For Harris to custom program to a user data pattern specification, the user must supply the data in one of the following formats:

1. Master PROM of same organization and pinout as device ordered. Two pieces required, three preferred.
2. Paper tape in Binary or ASCII BPNF.

* BINARY PAPER TAPE FORMAT

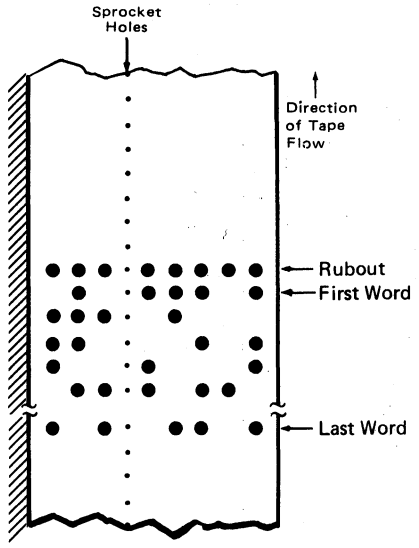
- A minimum of six inches of leader.
- A rubout (all eight locations punched).
- Data words beginning with the first word (word "0"), proceeding sequentially, ending with the last word (word "N"), with no interruptions or extraneous characters of any kind.
- Specifiy whether a punched hole is a VOH = "1" = logic high or is a VOL = "0" = logic low.
- A minimum trailer of six inches of tape.

* ASCII BPNF FORMAT

- A minimum leader of twenty rubouts (all eight locations punched).
- Any characters desired (none necessary) except "B".
- Data words beginning with the first word (word "0"), proceeding sequentially, ending with the last word (word "N").
- Data words consist of:
  1. The character "B" denoting the beginning of a data word.
  2. A sequence of characters, only "P" or "N", one character for each bit in the word.
  3. The character "F" denoting the finish of the data word.
- No extraneous characters of any kind may appear within a data word (between any "B" and the next "F").
- Errors may be deleted by rubouts superimposed over the entire word including the "B", and beginning the word again with a new "B".
- Any text of any kind (except the character "B") is allowed between data words (between any "F" and the next "B"), including carriage return and line feed.
- A minimum trailer of twenty-five rubouts.
- Specify whether a "P" is a "1" = VOH = logic high or is a "0" = VOL = logic low.
- The use of even or odd parity is optional.

* *Harris can not assume responsibility for PROMs programmed to data tapes or masters which contain errors. The user must insure the accuracy of the data provided to Harris. Harris guaranteed that the programmed PROMs will contain the information provided if either of the following formats are followed.*

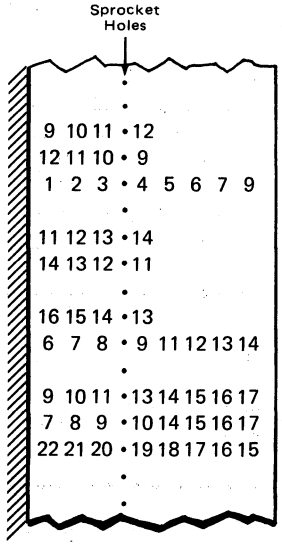
BINARY PAPER TAPE EXAMPLE



Resulting Truth Table
Punched Hole = "0" = VOL = Logic Low

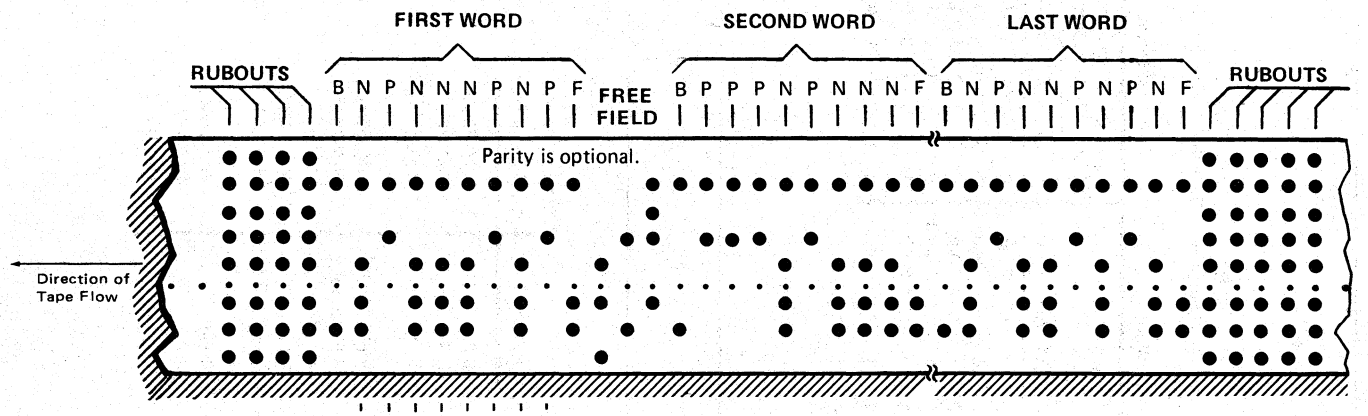
Word				PROM Output (24 Pin Package) Pin Numbers								
AX···A2	A1	A0		17	16	15	14	13	11	10	9
0···0	0	0	First	0	1	0	0	0	1	0	1
0···0	0	1	Second	1	1	1	0	1	0	0	0
0···0	1	0	Third	0	1	0	1	1	1	0	0
0···0	1	1	Fourth	0	1	1	1	0	1	1	0
0···1	0	0	Fifth	1	0	0	1	0	0	0	1
1···1	1	1	Last	0	1	0	0	1	0	1	0

DEVICE OUTPUT PACKAGE PINS



Package	Example
16 Pin CMOS	HM-6611
16 Pin Bipolar	HM-7611
16 Pin	HM-7603
18 Pin CMOS	HM-6661
18 Pin Bipolar	HM-7643
20 Pin	HM-7687
20 Pin	HM-7649
24 Pin	HM-7641
24 Pin	HM-7647
24 Pin	HM-0512

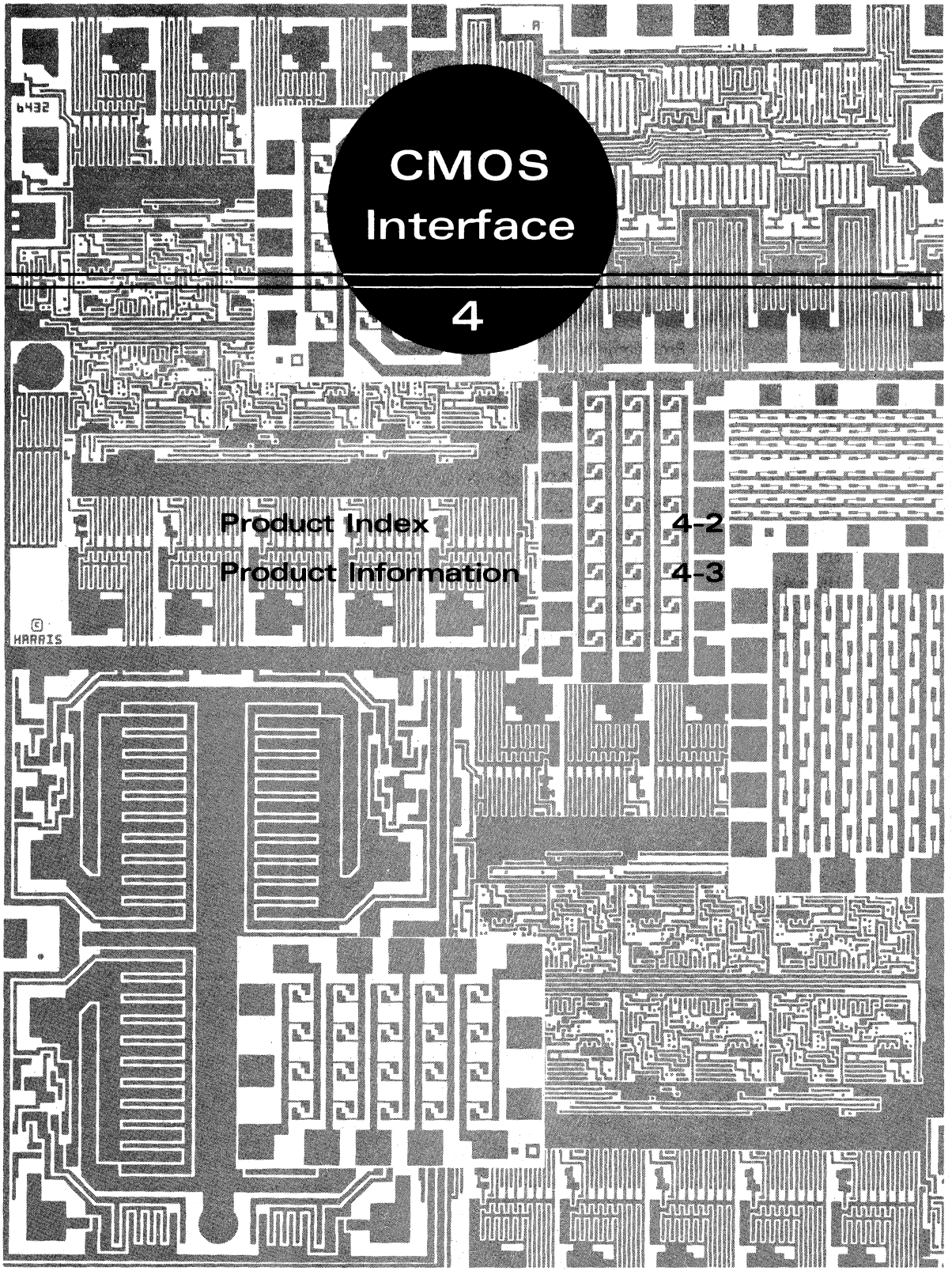
ASCII BPNF PAPER TAPE EXAMPLE



EXAMPLE	PACKAGE TYPE	DEVICE OUTPUT PINS
HM-6611	16 Pin Pkg	12 11 10 9 (MOS)
HM-7611	16 Pin Pkg	9 10 11 12 (Bipolar)
HM-7603	16 Pin Pkg	9 7 6 5 4 3 2 1
HM-6661	18 Pin Pkg	14 13 12 11 (MOS)
HM-7643	18 Pin Pkg	11 12 13 14 (Bipolar)
HM-7687	20 Pin Pkg	13 14 15 16
HM-7649	20 Pin Pkg	14 13 12 11 9 8 7 6
HM-7641	24 Pin Pkg	17 16 15 14 13 11 10 9
HM-7647	24 Pin Pkg	17 16 15 14 10 9 8 7
HM-0512	24 Pin Pkg	15 16 17 18 19 20 21 22

ResultingTruth Table
Character "P" = "1" = VOH = Logic High

Word		PROM Output (24 Pin Pkg) Pin Numbers
Ax ···A2 A1 A0		17 16 15 14 13 11 10 9
0 ··· 0 0 0	First	0 1 0 0 0 1 0 1
0 ··· 0 0 1	Second	1 1 1 0 1 0 0 0
1 ··· 1 1 1	Last	0 1 0 0 1 0 1 0



CMOS Interface

4

Product Index

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HD-4702/6405

CMOS PROGRAMMABLE BIT RATE GENERATOR

APRIL 1978

Features

- HD-4702 – PROVIDES 13 COMMONLY USED BIT RATES
- HD-6405 – PROVIDES 15 COMMONLY USED BIT RATES
- USES A 2.4576MHz CRYSTAL/INPUT FOR STANDARD FREQUENCY OUTPUT (16 TIMES BIT RATE)
- TTL COMPATIBLE – OUTPUT WILL SINK 1.6mA
- LOW POWER DISSIPATION HD-6405 4.0mW TYP. @ 2.4576MHz
  HD-4702 4.5mW TYP. @ 2.4576MHz
- CONFORMS TO EIA RS-404
- ONE HD-4702 OR HD-6405 CONTROLS UP TO EIGHT TRANSMISSION CHANNELS
- INITIALIZATION CIRCUIT FACILITATES DIAGNOSTIC FAULT ISOLATION
- ON-CHIP INPUT PULL-UP CIRCUIT – HD-4702 ONLY

Description

The HD-4702/6405 Bit Rate Generator provides the necessary clock signals for digital data transmission systems, such as UART. It generates 13(HD-4702) or 15(HD-6405) commonly used bit rates using an on-chip crystal oscillator or an external input. For conventional operation generating 16 output clock pulses per bit period, the input clock frequency must be 2.4576MHz (i.e. 9600 Baud x 16 x 16, since there is an internal ÷16 prescaler). A lower input frequency will result in a proportionally lower output frequency.

The HD-4702/6405 can provide multi-channel operation with a minimum of external logic by having the clock frequency CO and the ÷8 prescaler outputs Q_0, Q_1, Q_2 available externally. All signals have a 50% duty cycle except 1800 Baud and 2000 Baud which has less than 0.39% distortion and 3600 Baud which has less than 0.78% distortion.

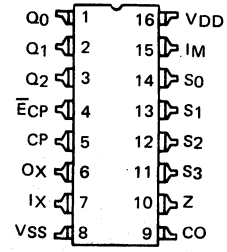
The four rate select inputs (S_0-S_3) select which bit rate is at the output (Z). The table lists select code and output bit rate. Two of the 16 for the HD-4702 and one of the 16 for the HD-6405 do not select an internally generated frequency, but select an input into which the user can feed either a different frequency, or a static level (High or Low) to generate "ZERO BAUD".

The bit rate most commonly used in modern data terminals (110, 150, 300, 1200, 2400 Baud) require that no more than one input be grounded for the HD-4702, which is easily achieved with a single, 5-position switch.

The HD-4702/6405 has an initialization circuit which generates a common master reset for all flip-flops. This signal is derived from a digital differentiator that senses the first high level on the CP input after the $\overline{E}_{CP}$ input goes low. When $\overline{E}_{CP}$ is high, selecting the crystal input, CP must be low. A high level on CP would apply a continuous reset.

For the HD-4702, all inputs except I_X have on-chip pull-up circuits which provide TTL compatibility and eliminate the need to tie a permanently high input to V_{DD}.

Pinout



PIN NAMES

$\overline{CP}$	External Clock Input
$\overline{E}_{CP}$	External Clock Enable Input (Active Low)
I_X	Crystal Input
I_M	Multiplexed Input
$S_0 - S_3$	Rate Select Inputs
CO	Clock Output
O_X	Crystal Drive Output
$Q_0 - Q_2$	Scan Counter Outputs
Z	Bit Rate Output

Truth Tables

TABLE 1
CLOCK MODES AND INITIALIZATION

I_X	E_{CP}	CP	OPERATION
⊓⊓	H	L	Clocked from I_X
X	L	⊓⊓	Clocked from CP
X	H	H	Continuous Reset
X	L	⊓	Reset During 1st CP = HIGH Time

NOTE: Actual output frequency is 16 times the indicated Output Rate, assuming a clock frequency of 2.4576MHz.

H = HIGH Level
L = LOW Level
X = Don't care
⊓ = 1st HIGH Level Clock Pulse after E_{CP} goes LOW
⊓⊓ = Clock Pulse

TABLE 2
TRUTH TABLE FOR RATE SELECT INPUTS

S_3 S_2 S_1 S_0	OUTPUT RATE (Z) HD-4702	OUTPUT RATE (Z) HD-6405
L L L L	MUX INPUT (I_M)	MUX INPUT (I_M)
L L L H	MUX INPUT (I_M)	2000 BAUD
L L H L	50 BAUD	50 BAUD
L L H H	75 BAUD	75 BAUD
L H L L	134.5 BAUD	134.5 BAUD
L H L H	200 BAUD	200 BAUD
L H H L	600 BAUD	600 BAUD
L H H H	2400 BAUD	3600 BAUD
H L L L	9600 BAUD	9600 BAUD
H L L H	4800 BAUD	4800 BAUD
H L H L	1800 BAUD	1800 BAUD
H L H H	1200 BAUD	1200 BAUD
H H L L	2400 BAUD	2400 BAUD
H H L H	300 BAUD	300 BAUD
H H H L	150 BAUD	150 BAUD
H H H H	110 BAUD	110 BAUD

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+12.0V
Input or Output Voltage Applied	GND -0.3 to V_{CC} +0.3
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-4702A-9/6405A-9	-40°C to +85°C
Military HD-4702A-2/6405A-2	-55°C to +125°C
Operating Voltage Range	+4V to +11V

ELECTRICAL CHARACTERISTICS

D.C.: V_{CC} = 10V ± 10%; T_A = Industrial or Military.
A.C.: V_{CC} = 10V; T_A = 25°C.

	SYMBOL	PARAMETER	HD-4702A-2/ 6405A-2 MIN	TYP	MAX	HD-4702A-9/ 6405A-9 MIN	TYP	MAX	UNITS	TEST CONDITIONS
D.C.	V_{IH}	Input High Voltage	70% V_{CC}			70% V_{CC}			V	
	V_{IL}	Input Low Voltage			20% V_{CC}			20% V_{CC}	V	
	V_{OH1}	Output High Voltage	V_{CC} -0.1			V_{CC} -0.1			V	$I_{OH} \leq -1\mu A$
	V_{OL1}	Output Low Voltage	GND +0.1			GND +0.1			V	$I_{OL} \leq +1\mu A$
	I_{IH}	Input High Current	-1		+1	-1		+1	μA	$V_I = V_{DD}$, All other pins = 0V
	I_{IL}	INPUT LOW CURRENT HD-4702 (all other inputs)		-110	-170		-110	-170	μA	
	I_{ILX}	(IX inputs)	-1		+1	-1		+1	μA	$V_I = 0$, All other pins = V_{DD}
	I_{IL}	HD-6405 - All pins	-1		10	-1		10	μA	
	I_{OHX}	OUTPUT HIGH (OX)	0.2			0.2			mA	V_{OUT} = 9.5
	I_{OH}	CURRENT (all other outputs)	0.6			0.6			mA	V_{OUT} = 9.5
	I_{OLX}	OUTPUT LOW (OX)	0.2			0.2			mA	V_{OUT} = .5V
	I_{OL}	CURRENT (all other outputs)	3.2			3.2			mA	V_{OUT} = .5V
		SUPPLY CURRENT HD-4702A			1000			3000	μA	$\overline{E}_{CP} = V_{DD}$, CP = 0, All other inputs = GND
		HD-4702A			500			1000	μA	$\overline{E}_{CP} = V_{DD}$, CP = 0, All other inputs = V_{DD}
		HD-6405A			500			500	μA	$\overline{E}_{CP} = V_{DD}$, CP = 0, All other inputs = V_{DD} or GND
A.C.	t_{PLH} t_{PHL}	Propagation Delay, IX to CO			150 125			150 125	ns ns	$C_L \leq 7$pF on OX
	t_{PLH} t_{PHL}	Propagation Delay, CP to CO			110 100			110 100	ns ns	C_L = 15pF Input Transition Times ≤ 20ns
	t_{PLH} t_{PHL}	Propagation Delay, CO to Q_n			⑤			⑤	ns ns	
	t_{PLH} t_{PHL}	Propagation Delay, CO to Z			40 35			40 35	ns ns	
	t_{TLH} t_{THL}	Output Transition Time (except OX)			40 20			40 20	ns ns	
	t_{PLH} t_{PHL}	Propagation Delay, IX to CO			175 140			175 140	ns ns	$C_L \leq 7$pF on OX
	t_{PLH} t_{PHL}	Propagation Delay, CP to CO			130 110			130 110	ns ns	C_L = 50pF Input Transition Times ≤ 20ns
	t_{PLH} t_{PHL}	Propagation Delay, CO to Q_n			⑤			⑤	ns ns	
	t_{PLH} t_{PHL}	Propagation Delay, CO to Z			45 40			45 40	ns ns	
	t_{TLH} t_{THL}	Output Transition Time (except OX)			80 40			80 40	ns ns	
	t_s t_h	Set-Up Time, Select to CO Hold Time, Select to CO	175 0			175 0			ns ns	$C_L \leq 7$pF on OX
	t_s t_h	Set-Up Time, IM to CO Hold Time, IM to CO	175 20			175 20			ns ns	C_L = 15pF Input Transition Times ≤ 20ns
	$t_{WCP(L)}$ $t_{WCP(H)}$	Minimum Clock Pulse-Width Low and High	60 60			60 60			ns ns	
	$t_{WCP(L)}$ $t_{WCP(H)}$	Minimum IX Pulse Width, Low and High	80 80			80 80			ns ns	

1. Input Current and Quiescent Power Supply Current are relatively higher for this device because of active pull-up circuits on all inputs except IX. This is done for TTL compatibility.
2. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transistion Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-Up Times (t_s), Hold Times (t_h), and Mininum Pulse Widths (t_W) do not vary with load capacitance.
3. The first High Level Clock Pulse after $\overline{E}_{CP}$ goes Low and must be at least 350ns long to guarantee reset of all Counters.
4. It is recommended that input rise and fall times to the Clock Inputs (CP, IX) be less than 15ns.
5. For multichannel operation, Propagation Delay (CO to Q_n) plus Set-Up Time, Select to CO, is guaranteed to be ≤ 190ns.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage		+8.0V
Input or Output Voltage Applied		GND -0.3V to V_{CC} +0.3V
Storage Temperature Range		-65°C to +150°C
Operating Temperature Range		
Industrial	HD-4702-9/6405-9	-40°C to +85°C
Military	HD-4702-2/6405-2	-55°C to +125°C
Operating Voltage Range		+4 to +7V

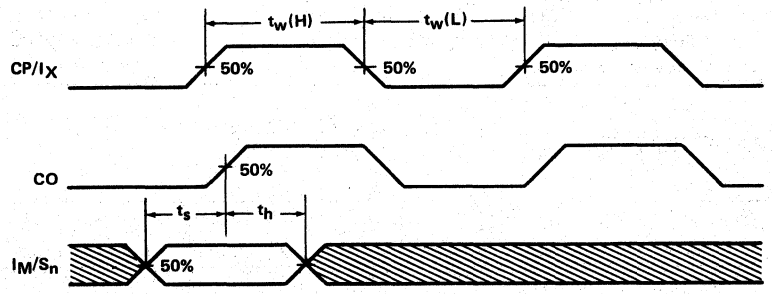
ELECTRICAL CHARACTERISTICS

D.C.: V_{CC} = 5V ± 10%; T_A = Industrial or Military.
A.C.: V_{CC} = 5V; T_A = 25°C.

	SYMBOL	PARAMETER	HD-4702-2/6405-2 MIN	TYP	MAX	HD-4702-9/6405-9 MIN	TYP	MAX	UNITS	TEST CONDITIONS
D.C.	V_{IH}	Input High Voltage	V_{CC} -1.5			V_{CC} -1.5			V	
	V_{IL}	Input Low Voltage			1.5			1.5	V	
	V_{OH1}	Output High Voltage	V_{CC} -.05			V_{CC} -.05			V	$I_{OH} \leq -1\mu A$
	V_{OL1}	Output Low Voltage			0.05			0.05	V	$I_{OL} \leq +1\mu A$
	I_{IH}	Input High Current	-1		+1	-1		+1	μA	$V_I = V_{DD}$, All other pins = 0V
	I_{IL}	INPUT HD-4702 (all other inputs) LOW		-30	-50		-30	-50	μA	
	I_{ILX}	CURRENT (I_X inputs)	-1		+1	-1		+1	μA	V_I = 0, All other pins = V_{DD}
	I_{IL}	HD-6405 - All pins	-1		+1	-1		+1	μA	
	I_{OHX}	OUTPUT (O_X)	-0.1			-0.1			mA	$V_{OUT} = V_{CC}$ -.5
	I_{OH1}	HIGH (all other outputs)	-1.0			-1.0			mA	V_{OUT} = 2.5V
	I_{OH2}	CURRENT (all other outputs)	-0.3			-0.3			mA	$V_{OUT} = V_{CC}$ -.5
	I_{OLX}	OUTPUT (O_X) LOW	0.1			0.1			mA	V_{OUT} = .4V
	I_{OL}	CURRENT (all other outputs)	1.6			1.6			mA	V_{OUT} = .4V
		Input at 0 or V_{DD} per Logic Function or Truth Table								
	I_{CC}	SUPPLY CURRENT HD-4702			500			1500	μA	$\overline{E}_{CP} = V_{DD}$, CP = 0, All other inputs = GND
		HD-4702			150			1000	μA	$\overline{E}_{CP} = V_{DD}$, CP = 0, All other inputs = V_{DD}
		HD-6405			150			150	μA	$\overline{E}_{CP} = V_{DD}$, CP = 0, All other inputs = V_{DD} or GND
A.C.	t_{PLH} t_{PHL}	Propagation Delay, I_X to CO			300 250			300 250	ns ns	$C_L \leq 7$pF on O_X
	t_{PLH} t_{PHL}	Propagation Delay, CP to CO			215 195			215 195	ns ns	C_L = 15pF Input Transition Times ≤ 20ns
	t_{PLH} t_{PHL}	Propagation Delay, CO to Q_n			⑤			⑤	ns ns	
	t_{PLH} t_{PHL}	Propagation Delay, CO to Z			75 65			75 65	ns ns	
	t_{TLH} t_{THL}	Output Transition Time (except O_X)			80 40			80 40	ns ns	
	t_{PLH} t_{PHL}	Propagation Delay, I_X to CO			350 275			350 275	ns ns	$C_L \leq 7$pF on O_X
	t_{PLH} t_{PHL}	Propagation Delay, CP to CO			260 220			260 220	ns ns	C_L = 50pF Input Transition Times ≤ 20ns
	t_{PLH} t_{PHL}	Propagation Delay, CO to Q_n			⑤			⑤	ns ns	
	t_{PLH} t_{PHL}	Propagation Delay, CO to Z			85 75			85 75	ns ns	
	t_{TLH} t_{THL}	Output Transition Time (except O_X)			160 75			160 75	ns ns	
	t_s t_h	Set-Up Time, Select to CO Hold Time, Select to CO	350 0			350 0			ns ns	$C_L \leq 7$pF on O_X
	t_s t_h	Set-Up Time, I_M to CO Hold Time, I_M to CO	350 0			350 0			ns ns	C_L = 15pF Input Transition Times ≤ 20ns
	$t_{WCP(L)}$ $t_{WCP(H)}$	Minimum Clock Pulse-Width Low and High	120 120			120 120			ns ns	
	$t_{WCP(L)}$ $t_{WCP(H)}$	Minimum I_X Pulse Width, Low and High	160 160			160 160			ns ns	

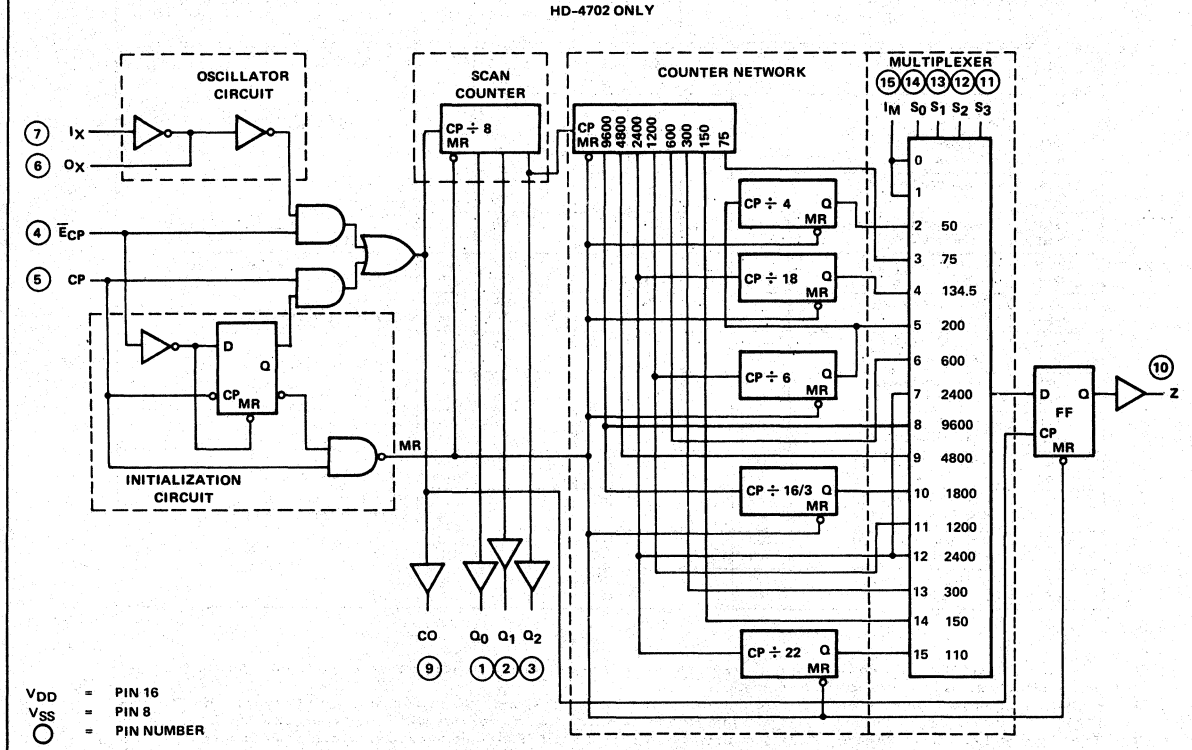
1. Input Current and Quiescent Power Supply Current are relatively higher for this device because of active pull-up circuits on all inputs except I_X. This is done for TTL compatibility.
2. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transistion Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-Up Times (t_s), Hold Times (t_h), and Mininum Pulse Widths (t_w) do not vary with load capacitance.
3. The first High Level Clock Pulse after $\overline{E}_{CP}$ goes Low and must be at least 350ns long to guarantee reset of all Counters.
4. It is recommended that input rise and fall times to the Clock Inputs (CP, I_X) be less than 15ns.
5. For multichannel operation, Propagation Delay (CO to Q_n) plus Set-Up Time, Select to CO, is guaranteed to be ≤ 367ns.

Switching Waveforms



NOTE: Set-Up and Hold Times are shown as positive values but may be specified as negative values.

Block Diagram



SINGLE CHANNEL BIT RATE GENERATOR

Figure 1 shows the simplest application of the HD-4702/6405. This circuit generates one of five possible bit rates as determined by the setting of a single pole, 5-position switch. The Bit Rate Output (Z) drives one standard TTL load or four low power Schottky loads over the full temperature range. The possible output frequencies correspond to 110, 150, 300, 1200, and 2400 or 3600 Baud. For many low cost terminals these five bit rates are adequate.

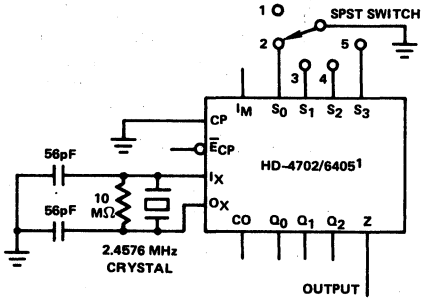
SIMULTANEOUS GENERATION OF SEVERAL BIT RATES

Fixed Programmed Multichannel Operation

Figure 2 shows a simple scheme that generates eight bit rates on eight output lines, using one HD-4702/6405 and one 93L34 Bit Addressable Latch. This and the following applications take advantage of the built-in scan counter (prescaler) outputs. As shown in the block diagram, these outputs (Q_0 to Q_2) go through a complete sequence of eight states for every half-period of the highest output frequency (9600 Baud). Feeding these Scan Counter Outputs back to the Select Inputs of the multiplexer causes the HD-4702/6405 to interrogate sequentially the state of eight different frequency signals. The 93L34 8-Bit Addressable Latch, addressed by the same Scan Counter Outputs, reconverts the multiplexed single Output (Z) of the HD-4702/6405 into eight parallel output frequency signals. In the simple scheme of Figure 2, input S_3 is left open (HIGH) and the following bit rates are generated:

Q_0: 110 Baud Q_1: 9600 Baud Q_2: 4800 Baud
Q_3: 1800 Baud Q_4: 1200 Baud Q_5: 2400 Baud
Q_6: 300 Baud Q_7: 150 Baud

Other bit rate combinations can be generated by changing the Scan Counter to Selector interconnection or by inserting logic gates into this path.



SWITCH POSITION	HD-4702 BIT RATE	HD-6405 BIT RATE
1	110 Baud	110 Baud
2	150 Baud	150 Baud
3	300 Baud	300 Baud
4	1200 Baud	1200 Baud
5	2400 Baud	3600 Baud

FIGURE 1

Switch selectable bit rate generator configuration providing five bit rates.

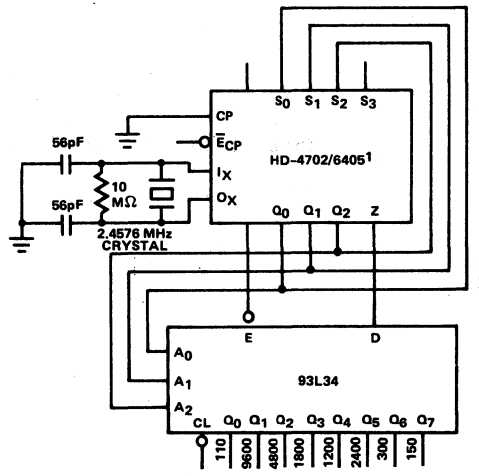


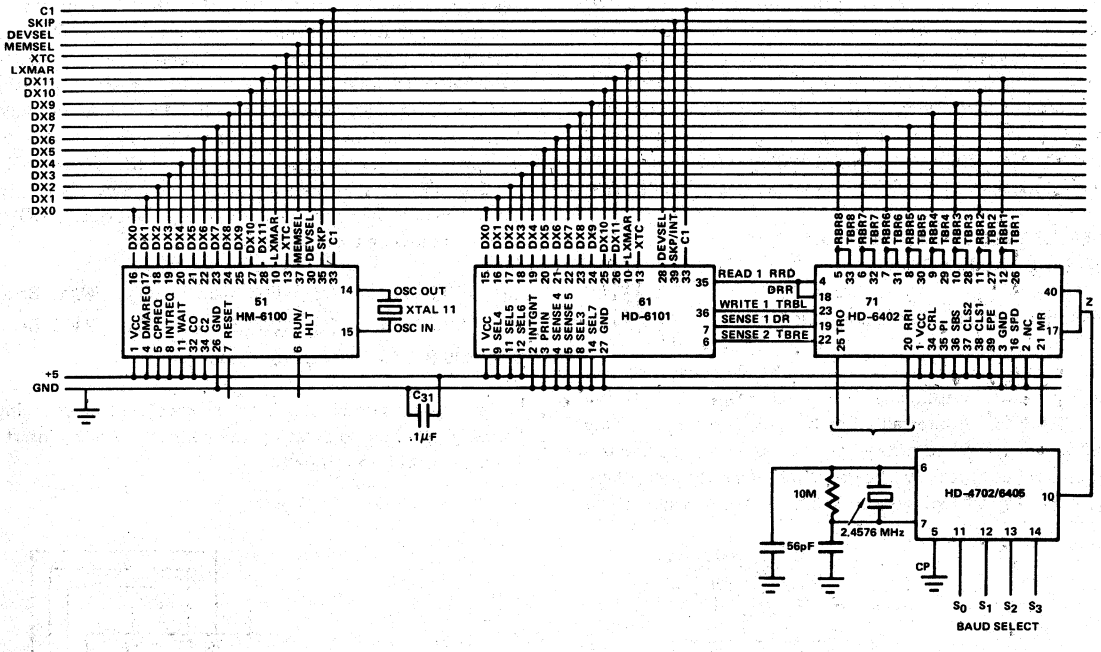
FIGURE 2

Bit rate generator configuration with eight simultaneous frequencies

NOTE 1: Need to add pull-up resistor on all inputs for the HD-6405.

TABLE 3 CRYSTAL SPECIFICATIONS

PARAMETERS	TYPICAL CRYSTAL SPEC
Frequency	2.4576 MHz "AT" Cut
Series Resistance (Max)	250
Unwanted Modes	-6.0dB (Min)
Type of Operation	Parallel
Load Capacitance	32pF +0.5



The bit rate generator is shown supplying the transmit and receive clocks for the UART.

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HD-6402

CMOS/LSI Universal Asynchronous Receiver Transmitter (UART)

JANUARY 1978

Features

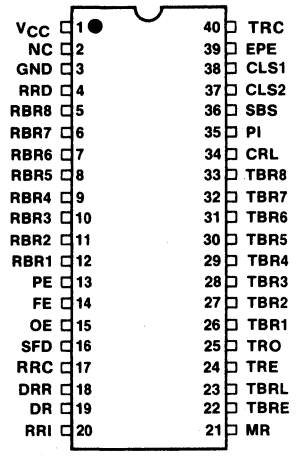
- OPERATION FROM D.C. TO 4.0MHz @10.0 VOLTS
- LOW POWER-TYP. 10mW @ 2.0MHz AND 5.0 VOLTS
- 4 TO 11 VOLT OPERATION
- PROGRAMMABLE WORD LENGTH, STOP BITS AND PARITY
- AUTOMATIC DATA FORMATTING AND STATUS GENERATION
- COMPATIBLE WITH INDUSTRY STANDARD UART'S
- SINGLE POWER SUPPLY

Description

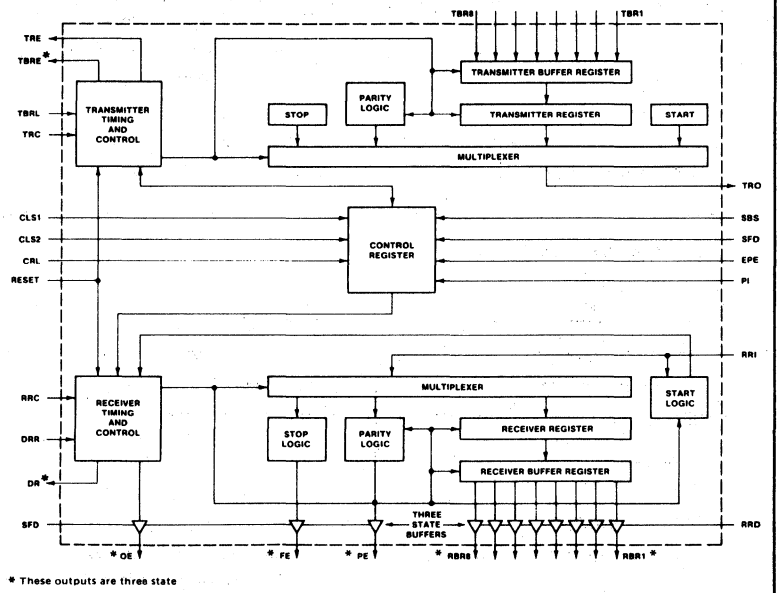
The HD-6402 is a CMOS/LSI subsystem for interfacing computers or microprocessors to an asynchronous serial data channel. The receiver converts serial start, data, parity and stop bits to parallel data verifying proper code transmission, parity, and stop bits. The transmitter converts parallel data into serial form and automatically adds start, parity, and stop bits. The data word length can be 5, 6, 7 or 8 bits. Parity may be odd or even. Parity checking and generation can be inhibited. The stop bits may be one or two or one and one-half when transmitting 5 bit code.

The HD-6402 can be used in a wide range of applications including modems, printers, peripherals and remote data aquisition systems. CMOS/LSI technology permits operation clock frequencies up to 4.0MHz (250K Baud) an improvement of 10 to 1 over previous PMOS UART designs. Power requirements, by comparison, are reduced from 300mW to 10mW. Status logic increases flexibility and simplifies the user interface.

Pinout



Functional Diagram



* These outputs are three state

Control Definition

CONTROL WORD					CHARACTER FORMAT			
CLS2	CLS1	PI	EPE	SBS	START BIT	DATA BITS	PARITY BIT	STOP BITS
0	0	0	0	0	1	5	ODD	1
0	0	0	0	1	1	5	ODD	1.5
0	0	0	1	0	1	5	EVEN	1
0	0	0	1	1	1	5	EVEN	1.5
0	0	1	X	0	1	5	NONE	1
0	0	1	X	1	1	5	NONE	1.5
0	1	0	0	0	1	6	ODD	1
0	1	0	0	1	1	6	ODD	2
0	1	0	1	0	1	6	EVEN	1
0	1	0	1	1	1	6	EVEN	2
0	1	1	X	0	1	6	NONE	1
0	1	1	X	1	1	6	NONE	2
1	0	0	0	0	1	7	ODD	1
1	0	0	0	1	1	7	ODD	2
1	0	0	1	0	1	7	EVEN	1
1	0	0	1	1	1	7	EVEN	2
1	0	1	X	0	1	7	NONE	1
1	0	1	X	1	1	7	NONE	2
1	1	0	0	0	1	8	ODD	1
1	1	0	0	1	1	8	ODD	2
1	1	0	1	0	1	8	EVEN	1
1	1	0	1	1	1	8	EVEN	2
1	1	1	X	0	1	8	NONE	1
1	1	1	X	1	1	8	NONE	2

4

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+12.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature Range	-65°C to 150°C
Operating Temperature Range	
Industrial HD-6402A-9	-40°C to +85°C
Military HD-6402A-2	-55°C to +125°C

ELECTRICAL CHARACTERISTICS

VCC = 10.0V ± 0.5V, TA = Industrial or Military

	SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	CONDITIONS
D.C.	V_{IH}	Logical "1" Input Voltage	70% VCC			V	
	V_{IL}	Logical "0" Input Voltage			20% VCC	V	
	I_{IL}	Input Leakage	-1.0		1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
	V_{OH}	Logical "1" Output Voltage*	VCC -0.01			V	$I_{OUT} = 0$
	V_{OL}	Logical "0" Output Voltage*			GND +0.01	V	$I_{OUT} = 0$
	I_O	Output Leakage	-1.0		1.0	μA	$0V \leq V_O \leq V_{CC}$
	I_{CC}	Supply Current		5.0	500	μA	$V_{CC} = 10.5V$, $V_{IN} = V_{CC}$ or GND
	C_{IN}	Input Capacitance*		7.0	8.0	pF	
	C_O	Output Capacitance*		6.0	10.0	pF	

*Guaranteed but not 100% tested.

			VCC = 10.0V ① TA = 25°C			VCC = 10V ± 0.5V TA = Industrial or Military				
	SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS	CONDITIONS
A.C.	f_{clock}	Clock Frequency	D.C.		6.0	D.C.		4.0	MHz	
	t_{pw}	Pulse Widths CRL, DRR, TBRL	75			100			ns	C_L = 50pF
	t_{pw}	Pulse Width MR	350			400			ns	See Switching Time
	t_{SET}	Input Data Setup Time	40			40			ns	Waveforms 1, 2, 3
	t_{HOLD}	Input Data Hold Time	30			30			ns	
	t_{pd}	Output Propagation Delays			50			70	ns	

NOTE 1: All devices guaranteed at worst case limits. Room temperature, 10V data provided for information-not guaranteed.

Switching Waveforms

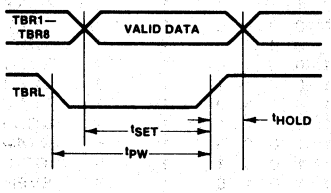


FIGURE 1
Data Input Cycle

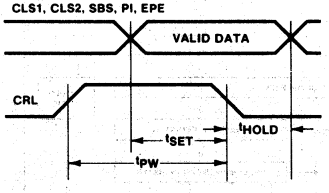


FIGURE 2
Control Register Load Cycle

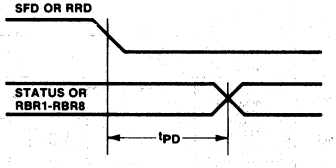


FIGURE 3
Status Flag Output Delays or Data Output Delays

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6402-9	-40°C to +85°C
Military HD-6402-2	-55°C to +125°C

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%. T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}			V	
V_{IL}	Logical "0" Input Voltage			20% V_{CC}	V	
I_{IL}	Input Leakage	-1.0		1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	2.4			V	$I_{OH} = -0.2mA$
V_{OL}	Logical "0" Output Voltage			0.45	V	$I_{OL} = 2.0mA$
I_O	Output Leakage	-1.0		1.0	μA	$0V \leq V_O \leq V_{CC}$
I_{CC}	Supply Current		1.0	100	μA	V_{IN} = GND or V_{CC}; V_{CC} = 5.5V, Output Open
C_{IN}	Input Capacitance*		7.0	8.0	pF	
C_O	Output Capacitance*		8.0	10.0	pF	

*Guaranteed but not 100% tested

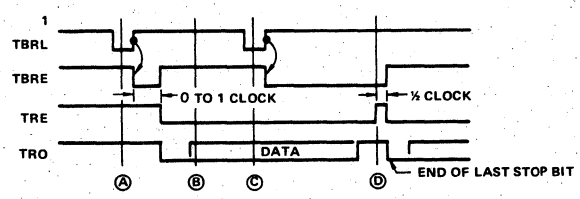
A.C.

		V_{CC} = 5.0V ① T_A = 25°C			V_{CC} = 5.0V ±10% T_A = Indust. or Mil.				
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS	CONDITIONS
f_{clock}	Clock Frequency	D.C.		3.0	D.C.		2.0	MHz	
t_{pw}	Pulse Widths CRL, DRR, TBRL	150			150			ns	C_L = 50pF
t_{pw}	Pulse Width MR	350			400			ns	See Switching Time
t_{SET}	Input Data Setup Time	50			50			ns	Waveforms 1, 2, 3
t_{HOLD}	Input Data Hold Time	60			60			ns	
t_{pd}	Output Propagation Delays			125			160	ns	

NOTE 1: All devices guaranteed at worst case limits. Room temperature, 5V data provided for information–not guaranteed.

Transmitter Operation

The transmitter section accepts parallel data, formats it and transmits it in serial form on the TROutput terminal. Ⓐ Data is loaded into the transmitter buffer register from the inputs TR1 through TR8 by a logic low on the TBRLoad input. Valid data must be present at least t_{SET} prior to and t_{HOLD} following the rising edge of TBRL. If words less than 8 bits are used, only the least significant bits are used. The character is right justified into the least significant bit, TR1. Ⓑ The rising edge of TBRL clears TBREmpty. 0 to 1 clock cycles later, data is transferred to the transmitter register; TREmpty is cleared; TBREmpty is set high; and serial data transmission is started. Output data is clocked by TRClock. The clock rate is 16 times the data rate. Ⓒ A second pulse on TBRLoad loads data into the transmitter buffer register. Data transfer to the transmitter register is delayed until transmission of the current character is complete. Ⓓ Data is automatically transferred to the transmitter register and transmission of that character begins one clock cycle later.



TRANSMITTER TIMING (NOT TO SCALE)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range (Industrial -9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS $V_{CC} = 5.0V \pm 5\%$. TA = Industrial

	SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	CONDITIONS
D.C.	V_{IH}	Logical "1" Input Voltage	V_{CC} -2.0			V	
	V_{IL}	Logical "0" Input Voltage			0.8	V	
	I_{IL}	Input Leakage	-10.0		+10.0	μA	$0V \leq V_{IN} \leq V_{CC}$
	V_{OH}	Logical "1" Output Voltage	2.4			V	I_{OH} = -0.2mA
	V_{OL}	Logical "0" Output Voltage			0.45	V	I_{OL} = 2.0mA
	I_O	Output Leakage	-10.0		+10.0	μA	$0V \leq V_O \leq V_{CC}$
	I_{CC}	Supply Current		1.0	800	μA	V_{IN} = GND or V_{CC}, V_{CC} = 5.25V, Output Open
	C_{IN}	Input Capacitance*		7.0	8.0	pF	
	C_O	Output Capacitance*		8.0	10.0	pF	

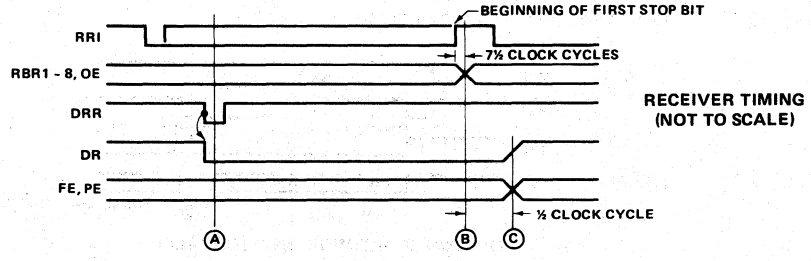
*Guaranteed but not 100% tested.

			$V_{CC} = 5.0V$ ① $T_A = 25°C$			$V_{CC} = 5.0V \pm 5\%$ T_A = Industrial				
	SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS	CONDITIONS
A.C.	f_{clock}	Clock Frequency	D.C.		2.0	D.C.		1.0	MHz	
	t_{pw}	Pulse Widths CRL, DRR, TBRL	200			225			ns	C_L = 50pF
	t_{pw}	Pulse Width MR	500			600			ns	See Switching Time
	t_{SET}	Input Data Setup Time	60			75			ns	Waveforms 1, 2, 3
	t_{HOLD}	Input Data Hold Time	75			90			ns	
	t_{pd}	Output Propagation Delays			150			190	ns	

NOTE 1: All devices guaranteed at worst case limits. Room temperature, 5V data provided for information-not guaranteed.

Receiver Operation

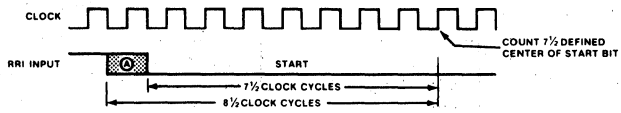
Data is received in serial form at the RInput. When no data is being received, RInput must remain high. The data is clocked through the RRClock. The clock rate is 16 times the data rate. Ⓐ A low level on DRReset clears the DReady line. Ⓑ During the first stop bit data is transferred from the receiver register to the RBRegister. If the word is less than 8 bits, the unused most significant bits will be a logic low. The output character is right justified to the least significant bit RBR1. A logic high on OError indicates overruns. An overrun occurs when DReady has not been cleared before the present character was transferred to the RBRegister. Ⓒ ½ clock cycle later DReady is reset to a logic high, PError and FError are evaluated. A logic high on FError indicates an invalid stop bit was received, a framing error. A logic high on PError indicates a parity error.



RECEIVER TIMING (NOT TO SCALE)

Start Bit Detection

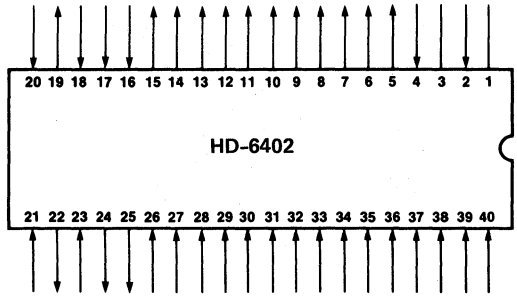
The receiver uses a 16X clock for timing. Ⓐ The start bit could have occurred as much as one clock cycle before it was detected, as indicated by the shaded portion. The center of the start bit is defined as clock count 7½. If the receiver clock is a symetrical square wave, the center of the start bit will be located within ±½ clock cycle, $\pm\frac{1}{32}$ bit or 3.125% giving a receiver margin of 46.875%. The receiver begins searching for the next start bit at the center of the first stop bit.



Pin Assignment And Functions

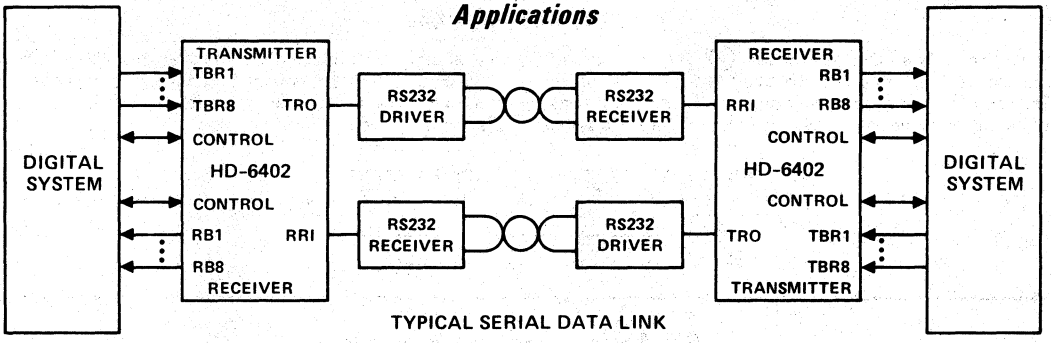
PIN	SYMBOL	DESCRIPTION
1	VCC	Positive Voltage Supply
2	NC	No Connection
3	GND	Ground
4	RRD	A High level on RECEIVER REGISTER DISABLE forces the receiver holding register outputs RBR1 - RBR8 to a high impedance state.
5	RBR8	The contents of the RECEIVER BUFFER REGISTER appear on these three-state outputs. Word formats less than 8 characters are right justified to RBR1.
6	RBR7	See Pin 5 - RBR8
7	RBR6	See Pin 5 - RBR8
8	RBR5	See Pin 5 - RBR8
9	RBR4	See Pin 5 - RBR8
10	RBR3	See Pin 5 - RBR8
11	RBR2	See Pin 5 - RBR8
12	RBR1	See Pin 5 - RBR8

PIN	SYMBOL	DESCRIPTION
13	PE	A high level on PARITY ERROR indicates received parity does not match parity programmed by control bits. When parity is inhibited this output is low.
14	FE	A high level on FRAMING ERROR indicates the first stop bit was invalid.
15	OE	A high level on OVERRUN ERROR indicates the data received flag was not cleared before the last character was transferred to the receiver buffer register.
16	SFD	A high level on STATUS FLAGS DISABLE forces the outputs PE, FE, OE, DR, TBRE to a high impedance state.
17	RRC	The RECEIVER REGISTER CLOCK is 16X the receiver data rate.
18	DRR	A low level on DATA RECEIVED RESET clears the data received output DR, to a low level.
19	DR	A high level on DATA RECEIVED indicates a character has been received and transferred to the receiver buffer register.
20	RRI	Serial data on RECEIVER REGISTER INPUT is clocked into the receiver register.



PIN	SYMBOL	DESCRIPTION
21	MR	A high level on MASTER RESET clears PE, FE, OE, and DR to a low level and sets the transmitter output to a high level after 18 clock cycles.
22	TBRE	A high level on TRANSMITTER BUFFER REGISTER EMPTY indicates the transmitter buffer register has transferred its data to the transmitter register and is ready for new data.
23	TBRL	A low level on TRANSMITTER BUFFER REGISTER LOAD transfers data from inputs TBR1 - TBR8 into the transmitter buffer register. A low to high transition on TBRL indicates data transfer to the transmitter register. If the transmitter register is busy, transfer is automatically delayed so that the two characters are transmitted end to end.
24	TRE	A high level on TRANSMITTER REGISTER EMPTY indicates completed transmission of a character including stop bits.
25	TRO	Character data, start data and stop bits appear serially at the TRANSMITTER REGISTER OUTPUT.
26	TBR1	Character data is loaded into the TRANSMITTER BUFFER REGISTER via inputs TBR1 - TBR8. For character formats less than 8 bits the TBR8, 7, and 6 inputs are ignored corresponding to the programmed word length.

PIN	SYMBOL	DESCRIPTION
27	TBR2	See Pin 26 - TBR1
28	TBR3	See Pin 26 - TBR1
29	TBR4	See Pin 26 - TBR1
30	TBR5	See Pin 26 - TBR1
31	TBR6	See Pin 26 - TBR1
32	TBR7	See Pin 26 - TBR1
33	TBR8	See Pin 26 - TBR1
34	CRL	A high level on CONTROL REGISTER LOAD loads the control register.
35	PI	A high level on PARITY INHIBIT inhibits parity generation, Parity checking and forces PE output low.
36	SBS	A high level on STOP BIT SELECT selects 1.5 stop bits for 5 character format and 2 stop bits for other lengths.
37	CLS2	These inputs program the CHARACTER LENGTH SELECTED (CLS1 low CLS2 low 5 bits) (CLS1 high CLS2 low 6 bits) (CLS1 low CLS2 high 7 bits) (CLS1 high CLS2 high 8 bits)
38	CLS1	See Pin 37 - CLS2
39	EPE	When PI is low a high level on EVEN PARITY ENABLE generates and checks even parity. A low level selects odd parity.
40	TRC	The TRANSMITTER REGISTER CLOCK is 16X the transmit data rate.



TYPICAL SERIAL DATA LINK

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

MAY 1978

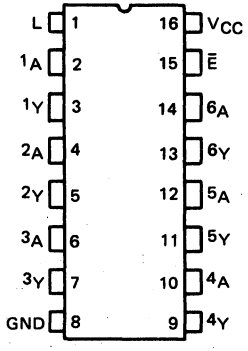
HD-6431
CMOS THREE-STATE LATCHING BUS DRIVER

Features

- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY. 300pF
- SOURCE CURRENT. 4mA
- SINK CURRENT 6mA
- PROPAGATION DELAY . . . . . 65nsec @ 5V

Pinout

TOP VIEW



Description

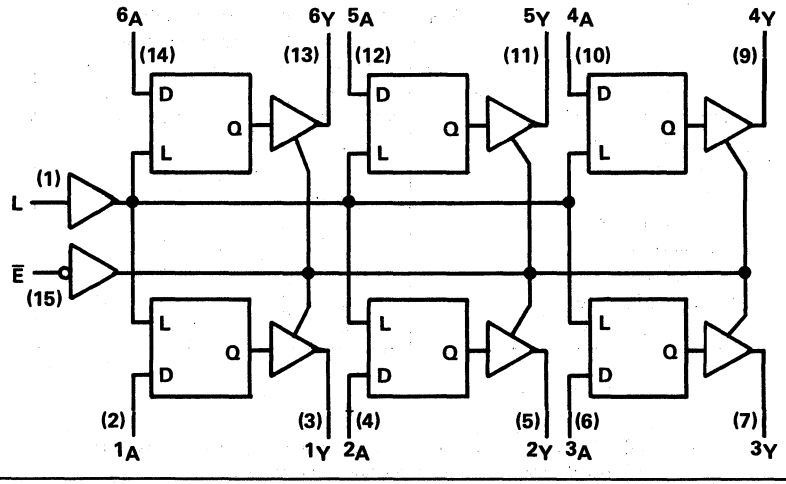
The HD-6431 is a self-aligned silicon gate CMOS Latching Three-State Bus Driver. This circuit consists of 6 non-inverting latching drivers with separate input and output. A high on the strobe line L allows data to go through the latches and a transition to low latches the data. A high on the Three-State control $\overline{E}$ forces the buffers to the high impedance mode without disturbing the latched data. New data may be latched in while the buffers are in the high impedance mode.

Truth Table

CONTROL INPUTS		DATA PORT STATUS	
$\overline{E}$	L	A	Y
H	L	X	HI-Z*
H	H	X	HI-Z
L	↓	X	*
L	H	L	L
L	H	H	H

* Data is latched to the value of the last input
X = Don't Care
HI-Z = High Impedance
↓ = Transition from High to Low level

Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+12.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6431A-9	-40°C to +85°C
Military HD-6431A-2	-55°C to +125°C
Operating Voltage Range	+4 to +11V

ELECTRICAL CHARACTERISTICS

V_{CC} = 10V ± 10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-10	10	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} -0.4		V	I_{OH} = -8.0mA, $\overline{E}$ = Low
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 12mA $\overline{E}$ = Low
I_O	Output Leakage	-10	10	μA	$0V \leq V_O \leq V_{CC}$, $\overline{E}$ = High
I_{CC}	Supply Current		100	μA	$V_{IN} = V_{CC}$ or GND, V_{CC} = 11V
C_{IN}	Input Capacitance*		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
C_O	Output Capacitance*		15	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

* Guaranteed and sampled, but not 100% tested.

C_L = 300pF

A.C.

		V_{CC} = 10.0V ① 25°C		V_{CC} = 10.0V ± 10% T_A = Indust. or Mil.		
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
t_{PD}	Propagation Delay		35		45	ns
t_{EN}	Enable Time		35		45	ns
t_{DIS}	Disable Time		35		45	ns
t_{SET}	Input Set Up Time	10		10		ns
t_{HOLD}	Input Hold Time	10		10		ns
t_{PW}	Pulse Width	15		20		ns
t_R	Output Rise Time		30		40	ns
t_F	Output Fall Time		20		30	ns

NOTE ① All devices guaranteed at worst case limits. Room temperature, 10V data provided for information-not guaranteed.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6431-9	-40°C to +85°C
Military HD-6431-2	-55°C to +125°C
Operating Voltage Range	+4 to +7V

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-1.0	1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} -0.4		V	I_{OH} = -4.0mA, $\overline{E}$ = Low
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 6.0mA $\overline{E}$ = Low
I_O	Output Leakage	-1.0	1.0	μA	$0V \leq V_O \leq V_{CC}$, $\overline{E}$ = High
I_{CC}	Supply Current		10	μA	$V_{IN} = V_{CC}$ or GND, V_{CC} = 5.5V
C_{IN}	Input Capacitance*		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
C_O	Output Capacitance*		15	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

* Guaranteed and sampled, but not 100% tested.

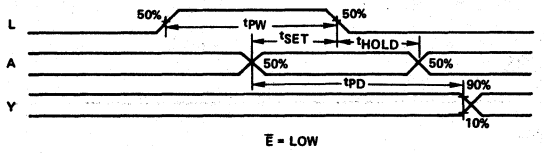
C_L = 300pF

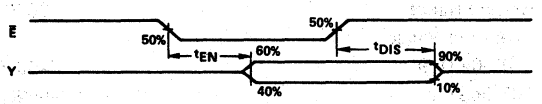
A.C.

		V_{CC} = 5.0V ① 25°C		V_{CC} = 5.0V ± 10% T_A = Indus. or Mil.		
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
t_{PD}	Propagation Delay		65		75	ns
t_{EN}	Enable Time		80		90	ns
t_{DIS}	Disable Time		80		90	ns
t_{SET}	Input Setup Time	15		15		ns
t_{HOLD}	Input Hold Time	15		15		ns
t_{PW}	Pulse Width	25		30		ns
t_R	Output Rise Time		80		90	ns
t_F	Output Fall Time		70		80	ns

NOTE ① All devices guaranteed at worst case limits. Room temperature, 5V data provided for information-not guaranteed.

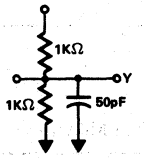
Switching Waveforms





All inputs have t_R, $t_F \leq$ 20ns.

OUTPUT TEST CIRCUIT
FOR PROPAGATION DELAYS

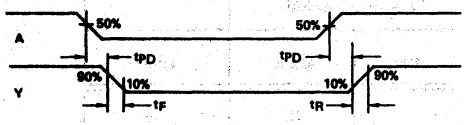


OUTPUT TEST CIRCUIT
FOR THREE-STATE DELAYS

DECOUPLING CAPACITORS

The transient current required to charge the load capacitance is given by $I_T = C\frac{dv}{dt}$. Assuming that all outputs may change state at the same time and that $\frac{dv}{dt}$ is constant; $I_T = \left(\Sigma C_L\right)\left(\frac{V_{CC} \times 80\%}{t_R \text{ or } t_F}\right)$ eg. $\left[t_R = 80ns, V_{CC} = 5.0V, \text{each } C_L = 300pF, I_T = (4)\left(300 \times 10^{-12}\right)\frac{5.0 \times 0.8}{80 \times 10^{-9}} = 90mA.\right]$ This current spike may cause a large negative voltage spike on V_{CC}, which if it becomes a diode drop less than any input, may cause the device to latch up. It is recommended that a 0.1 μF ceramic disk decoupling capacitor be placed between V_{CC} and GND at each device to filter out this noise.

PROPAGATION DELAYS



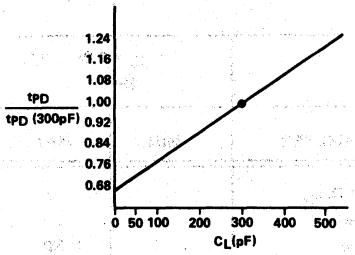


FIGURE 1

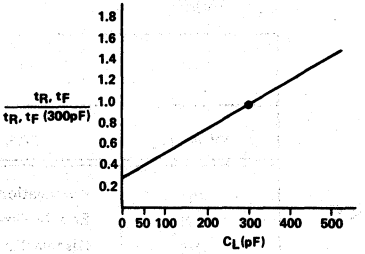


FIGURE 2

The above example will illustrate the calculation of a more useful propagation delay. The system in this example uses a 5 volt supply with a tolerance of ±10%, an ambient temperature of as high as 125°C, and a calculated load capacitance of 150pF. This application requires the HD-6431-2. The table of A.C. specs shows that t_{PD} at 4.5V and 125°C is 75nsec. Use the graph in Figure 1 to get the degradation multiple for 150pF. The number shown is 0.84. The adjusted propagation delay, to the 10% or 90% point, is therefore 75 x 0.84 or 63nsec. To obtain the rise and fall times check the A.C. specs for the rise and fall times at 4.5V and 125°C to obtain a worst case rise time of 90nsec. Use Figure 2 to find it's degradation multiple to be 0.65. The adjusted rise time is, therefore, 90 x 0.65 or 58nsec. To obtain the standard 50% to 50% propagation delay, add the adjusted propagation delay to half of the adjusted rise time to get a propagation delay of 92nsec. The rise time was used here because it is always the worst case.

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HD-6432

CMOS BI-DIRECTIONAL BUS DRIVER

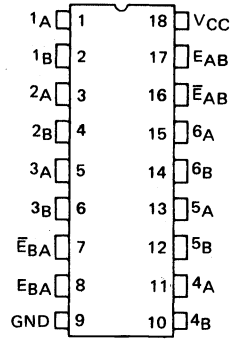
MAY 1978

Features

- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY. 300pF
- SOURCE CURRENT. 4mA
- SINK CURRENT 6mA
- PROPAGATION DELAY . . . . . 45nsec @ 5V

Pinout

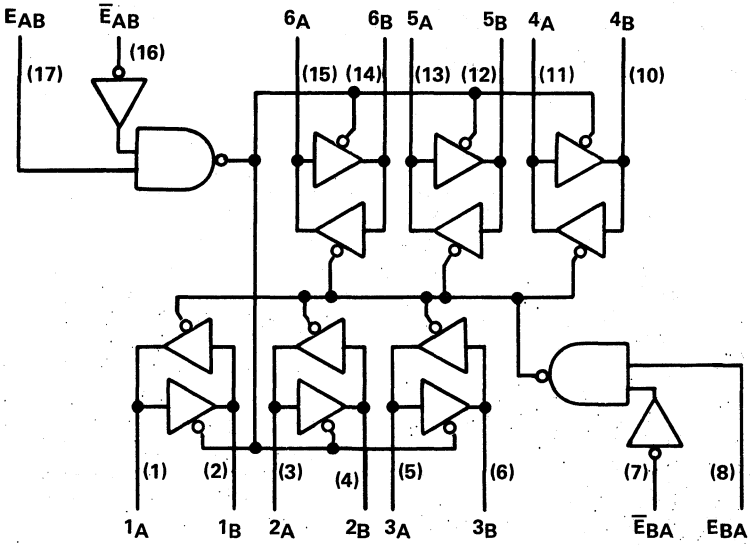
TOP VIEW



Description

The HD-6432 is a self-aligned silicon gate CMOS bi-directional bus driver. This circuit consists of 12 drivers organized as 6 bi-directional pairs. Four enable lines select drive direction or Three-State mode.

Functional Diagram



Truth Table

CONTROL INPUTS				DATA PORT STATUS	
E_{AB}	$\overline{E}_{AB}$	E_{BA}	$\overline{E}_{BA}$	A	B
L	X	H	L	O	I
X	H	H	L	O	I
H	L	X	H	I	O
H	L	L	X	I	O
L	X	L	X	ISOLATED	
X	H	X	H	ISOLATED	
L	X	X	H	ISOLATED	
X	H	L	X	ISOLATED	
H	L	H	L	NOT ALLOWED	

I = Input, O = Output, X = Don't Care

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+12.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6432A-9	-40°C to +85°C
Military HD-6432A-2	-55°C to +125°C
Operating Voltage Range	+4 to +11V

ELECTRICAL CHARACTERISTICS

V_{CC} = 10V ±10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-10	10	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} -0.4		V	I_{OH} = -8.0mA,
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 12mA
I_O	Output Leakage	-10	10	μA	$0V \leq V_O \leq V_{CC}$, $E_{AB} = E_{BA}$ = Low
I_{CC}	Supply Current		100	μA	$V_{IN} = V_{CC}$ or GND, V_{CC} = 11V
C_{IN}	Input Capacitance* (except I/O)		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
$C_{I/O}$	I/O Capacitance*		20	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

* Guaranteed and sampled, but not 100% tested.

C_L = 300pF

A.C.

		V_{CC} = 10.0V ① 25°C		V_{CC} = 10.0V ±10% T_A = Indust. or Mil.		
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
t_{PD}	Propagation Delay		35		45	ns
t_{EN}	Enable Time		40		50	ns
t_{DIS}	Disable Time		75		85	ns
t_R	Output Rise Time		40		50	ns
t_F	Output Fall Time		35		45	ns

NOTE ①: All devices guaranteed at worst case limits. Room temperature, 10V data provided for information–not guaranteed.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6432-9	-40°C to +85°C
Military HD-6432-2	-55°C to +125°C
Operating Voltage Range	+4 to +7V

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-1.0	1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} -0.4		V	I_{OH} = -4.0mA
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 6.0mA
I_O	Output Leakage	-1.0	1.0	μA	$0V \leq V_O \leq V_{CC}$, $E_{AB} = E_{BA}$ = Low
I_{CC}	Supply Current		10	μA	$V_{IN} = V_{CC}$ or GND, V_{CC} = 5.5V
C_{IN}	Input Capacitance* (except I/O)		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
$C_{I/O}$	I/O Capacitance*		20	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

* Guaranteed and sampled, but not 100% tested.

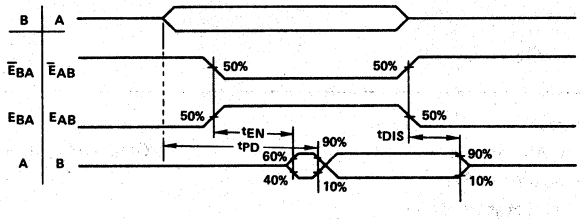
C_L = 300pF

A.C.

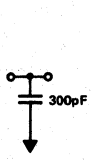
		V_{CC} = 5.0V ① 25°C		V_{CC} = 5.0V ± 10% T_A = Indus. or Mil.		
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
t_{PD}	Propagation Delay		45		55	ns
t_{EN}	Enable Time		65		75	ns
t_{DIS}	Disable Time		100		110	ns
t_R	Output Rise Time		100		110	ns
t_F	Output Fall Time		70		80	ns

NOTE ①: All devices guaranteed at worst case limits. Room temperature, 5V data provided for information–not guaranteed.

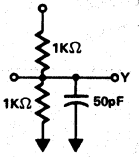
Switching Waveforms



All inputs have t_R, $t_F \leq 20$ns.



OUTPUT TEST CIRCUIT
FOR PROPAGATION DELAYS

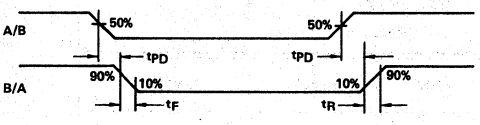


OUTPUT TEST CIRCUIT
FOR THREE-STATE DELAYS

DECOUPLING CAPACITORS

The Transient current required to charge the load capacitance is given by $I_T = C\frac{dv}{dt}$. Assuming that all outputs may change state at the same time and that $\frac{dv}{dt}$ is constant; $I_T = \left(\Sigma C_L\right)\left(\frac{V_{CC} \times 80\%}{t_R \text{ or } t_F}\right)$ eg. $\left[t_R = 100\text{ns} \quad V_{CC} = 5.0\text{V} \quad \text{each } C_L = 300\text{pF} \quad I_T = (6)\,(300 \times 10^{-12})\frac{5.0 \times 0.8}{100 \times 10^{-9}} = 72\text{mA.}\right]$ This current spike may cause a large negative voltage spike on V_{CC}, which if it becomes a diode drop less than any input, may cause the device to latch up. It is recommended that a 0.1 μF ceramic disk decoupling capacitor be placed between V_{CC} and GND at each device to filter out this noise.

PROPAGATION DELAYS



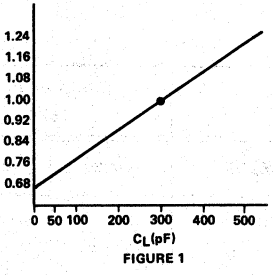


FIGURE 1

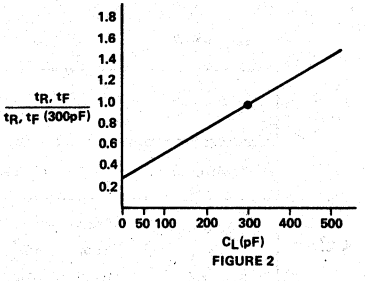


FIGURE 2

The above example will illustrate the calculation of a more useful propagation delay. The system in this example uses a 5 volt supply with a tolerance of ±10%, an ambient temperature of as high as 125°C, and a calculated load capacitance of 150pF. This application requires the HD-6432-2. The table of A.C. specs shows that t_{PD} at 4.5V and 125°C is 55nsec. Use the graph in Figure 1 to get the degradation multiple for 150pF. The number shown is 0.84. The adjusted propagation delay, to the 10% or 90% point, is therefore 55 x 0.84 or 46nsec. To obtain the rise and fall times check the A.C. specs for the rise and fall times at 4.5V and 125°C to obtain a worst case rise time of 110nsec. Use Figure 2 to find it's degradation multiple to be 0.65. The adjusted rise time is, therefore, 110 x 0.65 or 72nsec. To obtain the standard 50% to 50% propagation delay, add the adjusted propagation delay to half of the adjusted rise time to get a propagation delay of 82nsec. The rise time was used here because it is always the worst case.

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HD-6433
CMOS BUS SEPARATOR/DRIVER

MAY 1978

Features

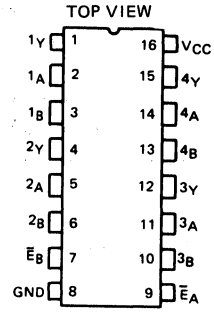
- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY. 300pF
- SOURCE CURRENT. 4mA
- SINK CURRENT 6mA
- PROPAGATION DELAY . . . . . 40nsec @ 5V

Description

The HD-6433 is a self-aligned silicon gate CMOS bus separator/driver. This circuit consists of 8 drivers organized as 4 pairs of bus separators which allow a unidirectional input bus and a unidirectional output bus to be interfaced with a bi-directional bus.

Pinout

TOP VIEW

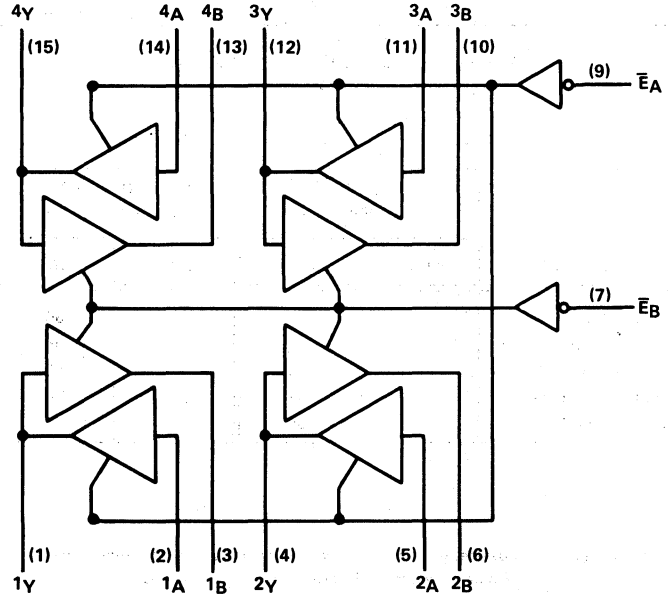


Truth Table

CONTROL INPUTS		FUNCTION		
$\overline{E}_A$	$\overline{E}_B$	A	B	Y
L	L	I	O	O
L	H	I	D	O
H	L	D	O	I
H	H	ISOLATED		

I = Input, O = Output,
D = Disconnected

Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+12.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6433A-9	-40°C to +85°C
Military HD-6433A-2	-55°C to +125°C
Operating Voltage Range	+4 to +11V

ELECTRICAL CHARACTERISTICS

V_{CC} = 10V ± 10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-10	10	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} -0.4		V	I_{OH} = -8.0mA
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 12mA
I_O	Output Leakage	-10	10	μA	$0V \leq V_O \leq V_{CC}$, $\overline{E}_A = \overline{E}_B$ = High
I_{CC}	Supply Current		100	μA	$V_{IN} = V_{CC}$ or GND, V_{CC} = 11V
C_{IN}	Input Capacitance* (except I/O)		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
$C_{I/O}$	I/O Capacitance *		20	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
C_O	Output Capacitance*		15	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

* Guaranteed and sampled, but not 100% tested.

C_L = 300pF

A.C.

		V_{CC} = 10.0V ① 25°C		V_{CC} = 10.0V ± 10% T_A = Indust. or Mil.		
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
t_{PD}	Propagation Delay		20		30	ns
t_{EN}	Enable Time		45		55	ns
t_{DIS}	Disable Time		45		55	ns
t_R	Output Rise Time		65		75	ns
t_F	Output Fall Time		55		65	ns

NOTE ① All devices guaranteed at worst case limits. Room temperature, 10V data provided for information–not guaranteed.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6433-9	-40°C to +85°C
Military HD-6433-2	-55°C to +125°C
Operating Voltage Range	+4 to +7V

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-1.0	1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} -0.4		V	I_{OH} = -4.0mA
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 6.0mA
I_O	Output Leakage	-1.0	1.0	μA	$0V \leq V_O \leq V_{CC}$ $\overline{E}_A = \overline{E}_B$ = High
I_{CC}	Supply Current		10	μA	$V_{IN} = V_{CC}$ or GND, V_{CC} = 5.5V
C_{IN}	Input Capacitance* (except I/O)		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
$C_{I/O}$	I/O Capacitance*		20	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
C_O	Output Capacitance*		15	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

* Guaranteed and sampled, but not 100% tested.

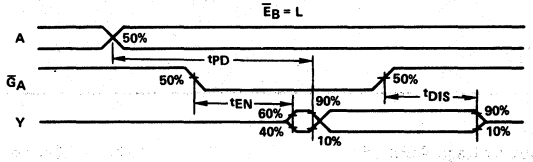
C_L = 300pF

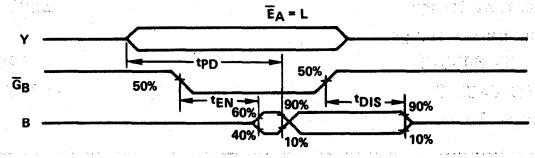
A.C.

		V_{CC} = 5.0V ① 25°C		V_{CC} = 5.0V ± 10% TA = Indust. or Mil.		
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
t_{PD}	Propagation Delay		40		50	ns
t_{EN}	Enable Time		60		70	ns
t_{DIS}	Disable Time		90		100	ns
t_R	Output Rise Time		85		95	ns
t_F	Output Fall Time		70		80	ns

NOTE ① All devices guaranteed at worst case limits. Room temperature, 5V data provided for information–not guaranteed.

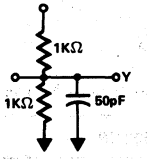
Switching Waveforms





All inputs have t_R, $t_F \leq$ 20ns.

OUTPUT TEST CIRCUIT
FOR PROPAGATION DELAYS

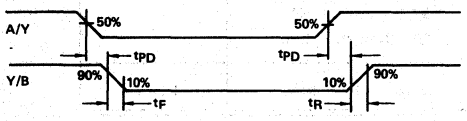


OUTPUT TEST CIRCUIT
FOR THREE-STATE DELAYS

DECOUPLING CAPACITORS

The transient current required to charge the load capacitance is given by $I_T = C \frac{dv}{dt}$. Assuming that all outputs may change state at the same time and that $\frac{dv}{dt}$ is constant; $I_T = \left(\Sigma C_L\right)\left(\frac{V_{CC} \times 80\%}{t_R \text{ or } t_F}\right)$ eg. $\left[t_R = 85ns, V_{CC} = 5.0V, \text{each } C_L = 300pF, I_T = (4)\left(300 \times 10^{-12}\right)\frac{5.0 \times 0.8}{85 \times 10^{-9}} = 56.5mA.\right]$ This current spike may cause a large negative voltage spike on V_{CC}, which if it becomes a diode drop less than any input, may cause the device to latch up. It is recommended that a 0.1 μF ceramic disk decoupling capacitor be placed between V_{CC} and GND at each device to filter out this noise.

PROPAGATION DELAYS



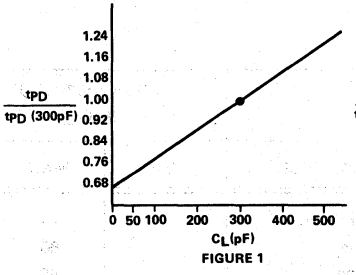


FIGURE 1

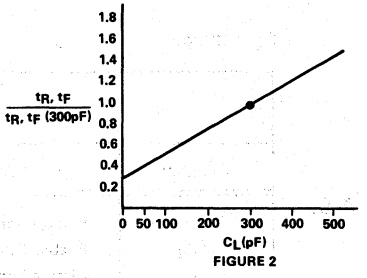


FIGURE 2

The above example will illustrate the calculation of a more useful propagation delay. The system in this example uses a 5 volt supply with a tolerance of ±10%, an ambient temperature of as high as 125°C, and a calculated load capacitance of 150pF. This application requires the HD-6433-2. The table of A.C. specs shows that t_{PD} at 4.5V and 125°C is 50nsec. Use the graph in Figure 1 to get the degradation multiple for 150pF. The number shown is 0.84. The adjusted propagation delay, to the 10% or 90% point, is therefore 50 x 0.84 or 42nsec. To obtain the rise and fall times check the A.C. specs for the rise and fall times at 4.5V and 125°C to obtain a worst case rise time of 95nsec. Use Figure 2 to find it's degradation multiple to be 0.65. The adjusted rise time is, therefore, 95 x 0.65 or 62nsec. To obtain the standard 50% to 50% propagation delay, add the adjusted propagation delay to half of the adjusted rise time to get a propagation delay of 73nsec. The rise time was used here because it is always the worst case.

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

FEBRUARY 1978

HD-6440
CMOS LATCHED DECODER-DRIVER

Features

- HIGH SPEED DECODING FOR MEMORY ARRAYS
- INCORPORATES 3 ENABLE INPUTS TO SIMPLIFY EXPANSION
- LOW POWER . . . . . TYPICALLY<50 μW @ 5V STANBDY
- HIGH NOISE IMMUNITY
- AVAILABLE IN BOTH MILITARY AND INDUSTRIAL TEMPERATURE RANGE
- HIGH CAPACITANCE DRIVE 200pF
- HIGH OUTPUT DRIVE . . . . . I_{OH} = -2mA, I_{OL} = 2.4mA
- SINGLE POWER SUPPLY

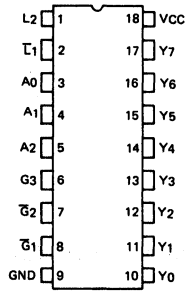
Description

The HD-6440 is a self aligned silicon gate latched decoder. One of 8 output lines is decoded, and brought to a low state, from the 3 input lines. There are two latch enables ($\overline{L_1}$, L_2), one complemented and one not, to eliminate the need for external gates. The output is enabled by three different output enables ($\overline{G_1}$, $\overline{G_2}$, G_3), two of them complemented and one not. Each output remains in a high state until it is selected, at which time it will go low.

When using high speed CMOS memories, the delay time of the HD-6440 and the enable time of the memory is usually less than the access time of the memory. This assures that memory access time will not be lengthened by the use of the HD-6440 latched decoder driver. The latch is useful for memory mapping or for systems which use a multiplexed bus.

Pinout

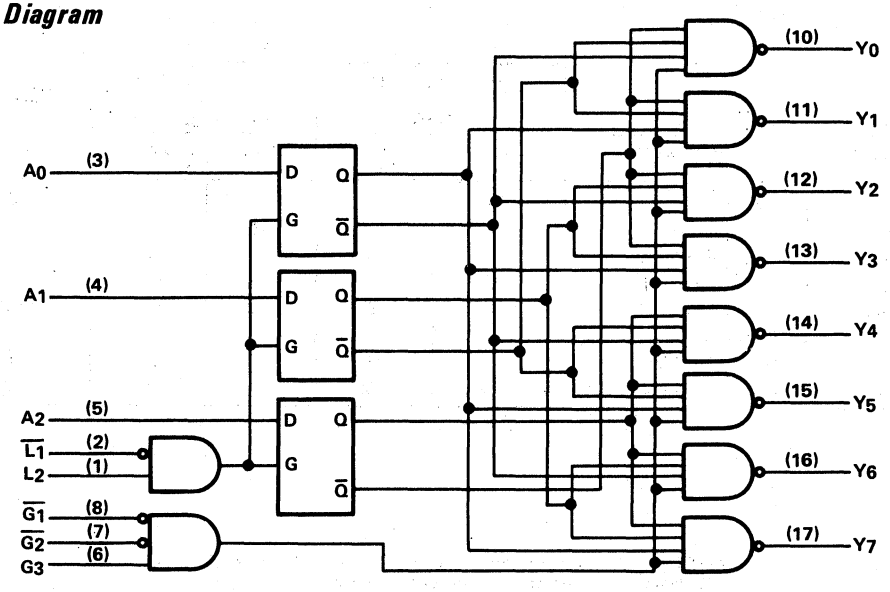
TOP VIEW



Truth Table

INPUTS							OUTPUTS								
Enable					Address										
$\overline{G_1}$	$\overline{G_2}$	G_3	$\overline{L_1}$	L_2	A_2	A_1	A_0	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	FUNCTION
X	X	L	X	X	X	X	X	H	H	H	H	H	H	H	H	DISABLE
X	H	X	X	X	X	X	X	H	H	H	H	H	H	H	H	
H	X	X	X	X	X	X	X	H	H	H	H	H	H	H	H	
L	L	H	L	H	L	L	L	L	H	H	H	H	H	H	H	DECODE
L	L	H	L	H	L	L	H	H	L	H	H	H	H	H	H	
L	L	H	L	H	L	H	L	H	H	L	H	H	H	H	H	
L	L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	
L	L	H	L	H	H	L	L	H	H	H	H	L	H	H	H	
L	L	H	L	H	H	L	H	H	H	H	H	H	L	H	H	
L	L	H	L	H	H	H	L	H	H	H	H	H	H	L	H	
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	
L	L	H	X	L	X	X	X	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	LATCHED
L	L	H	H	X	X	X	X	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	

Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	12.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6440A-9	-40°C to +85°C
Military HD-6440A-2	-55°C to +125°C
Operating Voltage Range	+4 to +11V

ELECTRICAL CHARACTERISTICS

V_{CC} = 10V ± 10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-10	10	µA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} - 0.4		V	I_{OH} = -5.0mA
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 5.0mA
I_{CC}	Supply Current		100	µA	V_{CC} = 11V
C_{IN}	Input Capacitance*		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
C_O	Output Capacitance*		15	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

* Guaranteed and sampled, but not 100% tested..

A.C.

C_L = 200pF

		V_{CC} = 10.0V ① 25°C		V_{CC} = 10.0V ± 10% T_A = Indus. or Mil.		
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
t_{SET}	Input Setup Time	15		15		ns
t_{HOLD}	Input Hold Time	15		15		ns
t_{PD}	Propagation Delay		40		60	ns
t_{EN}	Enable Time		35		50	ns
t_{DIS}	Disable Time		35		50	ns
t_{PW}	Pulse Width	15		25		ns
t_R	Output Rise Time		45		60	ns
t_F	Output Fall Time		45		60	ns

NOTE ① All devices guaranteed at worst case limits. Room temperature, 10V data provided for information-not guaranteed.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6440A-9	-40°C to +85°C
Military HD-6440A-2	-55°C to +125°C
Operating Voltage Range	+4 to +7V

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-1.0	1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} - 0.4		V	I_{OH} = -2.4mA
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 2.4mA
I_{CC}	Supply Current		10	μA	V_{CC} = 5.5V
C_{IN}	Input Capacitance*		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
C_O	Output Capacitance*		15	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

*Guaranteed and sampled, but not 100% tested.

4

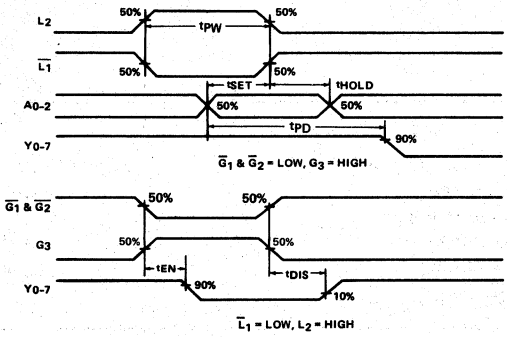
A.C.

CL = 200pF

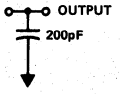
		V_{CC} = 5.0V ① 25°C		V_{CC} = 5.0V ± 10% T_A = Indust. or Mil.		
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
t_{SET}	Input Setup Time	20		20		ns
t_{HOLD}	Input Hold Time	20		20		ns
t_{PD}	Propagation Delay		65		100	ns
t_{EN}	Enable Time		50		80	ns
t_{DIS}	Disable Time		50		90	ns
t_{PW}	Pulse Width	30		30		ns
t_R	Output Rise Time		60		90	ns
t_F	Output Fall Time		50		80	ns

NOTE ① All devices guaranteed at worst case limits. Room temperature, 5V data provided for information-not guaranteed.

Switching Waveforms



All Inputs have t_R, $t_F \leq 20ns$

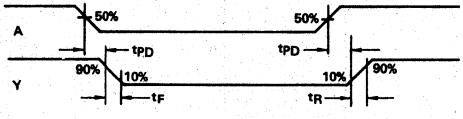


OUTPUT TEST CIRCUIT FOR PROPAGATION DELAYS

DECOUPLING CAPACITORS

The Transient current required to charge the load capacitance is given by $I_T = C\frac{dv}{dt}$. Assuming that all outputs may change state at the same time and that $\frac{dv}{dt}$ is constant; $I_T = \left(\Sigma C_L\right)\left(\frac{V_{CC} \times 80\%}{t_R \text{ or } t_F}\right)$ eg. [t_R = 60ns, V_{CC} = 5.0V, each C_L = 200pF, $I_T = (2)\ (200 \times 10^{-12})\ \frac{5.0 \times 0.8}{60 \times 10^{-9}} = 26.7mA$.] This current spike may cause a large negative voltage spike on V_{CC}, which if it becomes a diode drop less than any input, may cause the device to latch up. It is recommended that a 0.1μF ceramic disk decoupling capacitor be placed between V_{CC} and GND at each device to filter out this noise.

PROPAGATION DELAY



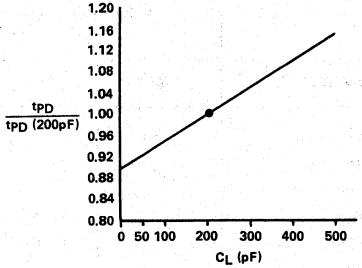


FIGURE 1

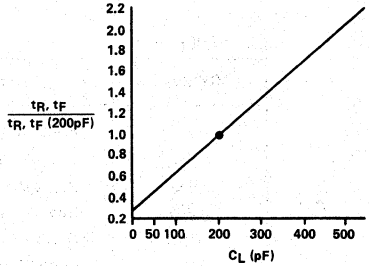


FIGURE 2

The above example will illustrate the calculation of a more useful propagation delay. The system in this example uses a 5 volt supply with a tolerance of ±10%, an ambient temperature of as high as 125°C, and a calculated load capacitance of 150pF. This application requires the HD-6440-2. The table of A.C. specs shows that t_{PD} at 4.5V and 125°C is 100nsec. Use the graph in Figure 1 to get the degradation multiple for 150pF. The number shown is 0.97. The adjusted propagation delay, to the 10% or 90% point, is therefore, 100 x 0.97 or 97nsec. To obtain the rise and fall times check the A.C. specs for the rise and fall times at 4.5V and 125°C to obtain a worst case rise time of 90nsec. Use Figure 2 to find it's degradation multiple to be 0.85. The adjusted rise time is therefore, 90 x 0.85 or 76.5nsec. To obtain the standard 50% to 50% propagation delay, add the adjusted propagation delay to half of the adjusted rise time to get a propagation delay of 135nsec. The rise time was used here because it is always the worst case.

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

MAY 1978

HD-6495
CMOS THREE-STATE BUFFER DRIVER

Features

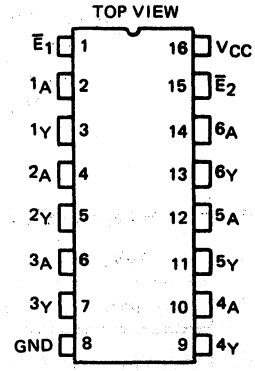
- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY. 300pF
- SOURCE CURRENT. 4mA
- SINK CURRENT 6mA
- PROPAGATION DELAY . . . . . 35nsec @ 5V

Description

The HD-6495 is a self aligned silicon gate CMOS Three-State buffer driver. The circuit consists of 6 non-inverting buffers with separate inputs and outputs which permit this driver to be used for bi-directional or uni-directional busing. A high on either Three-State control line $\overline{E}_1$ or $\overline{E}_2$ will force the drivers to the high impedance mode.

Pinout

TOP VIEW

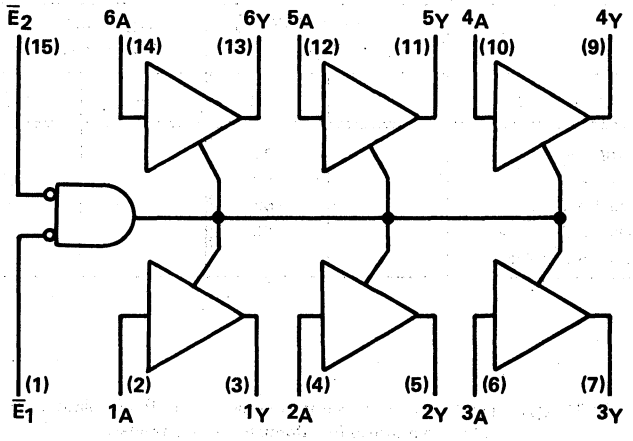


Truth Table

CONTROL INPUTS		INPUT	OUTPUT
$\overline{E}_1$	$\overline{E}_2$	A	Y
L	L	L	L
L	L	H	H
L	H	X	HI-Z
H	L	X	HI-Z
H	H	X	HI-Z

X = DON'T CARE
HI-Z = HIGH IMPEDANCE

Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+12.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6495A-9	-40°C to +85°C
Military HD-6495A-2	-55°C to +125°C
Operating Voltage Range	+4 to +11V

ELECTRICAL CHARACTERISTICS

V_{CC} = 10V ± 10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-10	10	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} -0.4		V	I_{OH} = -8.0mA, $\overline{E}_1 = \overline{E}_2$ = Low
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 12mA $\overline{E}_1 = \overline{E}_2$ = Low
I_O	Output Leakage	-10	10	μA	$0V \leq V_O \leq V_{CC}$, $\overline{E}_1 = \overline{E}_2$ = High
I_{CC}	Supply Current		100	μA	$V_{IN} = V_{CC}$ or GND, V_{CC} = 11V
C_{IN}	Input Capacitance*		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
C_O	Output Capacitance*		15	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

* Guaranteed and sampled, but not 100% tested.

C_L = 300pF

A.C.

		V_{CC} = 10.0V ① 25°C		V_{CC} = 10.0V ± 10% T_A = Indust. or Mil.		
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
t_{PD}	Propagation Delay		30		40	ns
t_{EN}	Enable Time		60		70	ns
t_{DIS}	Disable Time		60		70	ns
t_R	Output Rise Time		65		75	ns
t_F	Output Fall Time		65		75	ns

NOTE ①: All devices guaranteed at worst case limits. Room temperature, 10V data provided for information–not guaranteed.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6495-9	-40°C to +85°C
Military HD-6495-2	-55°C to +125°C
Operating Voltage Range	+4 to +7V

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-1.0	1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} -0.4		V	I_{OH} = -4.0mA, $\overline{E}_1 = \overline{E}_2$ = Low
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 6.0mA $\overline{E}_1 = \overline{E}_2$ = Low
I_O	Output Leakage	-1.0	1.0	μA	$0V \leq V_O \leq V_{CC}$, $\overline{E}_1 = \overline{E}_2$ = High
I_{CC}	Supply Current		10	μA	$V_{IN} = V_{CC}$ or GND, V_{CC} = 5.5V
C_{IN}	Input Capacitance*		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
C_O	Output Capacitance*		15	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

* Guaranteed and sampled, but not 100% tested.

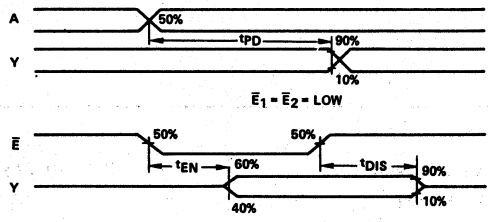
C_L = 300pF

A.C.

		V_{CC} = 5.0V ① 25°C		V_{CC} = 5.0V ± 10% T_A = Indus. or Mil.		
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
t_{PD}	Propagation Delay		35		45	ns
t_{EN}	Enable Time		90		100	ns
t_{DIS}	Disable Time		90		100	ns
t_R	Output Rise Time		85		95	ns
t_F	Output Fall Time		65		75	ns

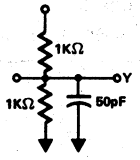
NOTE ① All devices guaranteed at worst case limits. Room temperature, 5V data provided for information-not guaranteed.

Switching Waveforms



All inputs have t_R, $t_F \leq$ 20ns.

OUTPUT TEST CIRCUIT
FOR PROPAGATION DELAYS

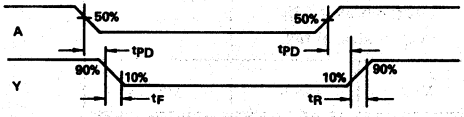


OUTPUT TEST CIRCUIT
FOR THREE-STATE DELAYS

DECOUPLING CAPACITORS

The transient current required to charge the load capacitance is given by $I_T = C\frac{dv}{dt}$. Assuming that all outputs may change state at the same time and that $\frac{dv}{dt}$ is constant; $I_T = \left(\Sigma C_L\right)\left(\frac{V_{CC} \times 80\%}{t_R \text{ or } t_F}\right)$ eg. $\left[t_R = 85\text{ns}, V_{CC} = 5.0\text{V}, \text{each } C_L = 300\text{pF}, I_T = (6)\left(300 \times 10^{-12}\right)\frac{5.0 \times 0.8}{85 \times 10^{-9}} = 84.7\text{mA.}\right]$ This current spike may cause a large negative voltage spike on V_{CC}, which if it becomes a diode drop less than any input, may cause the device to latch up. It is recommended that a 0.1 μF ceramic disk decoupling capacitor be placed between V_{CC} and GND at each device to filter out this noise.

PROPAGATION DELAYS



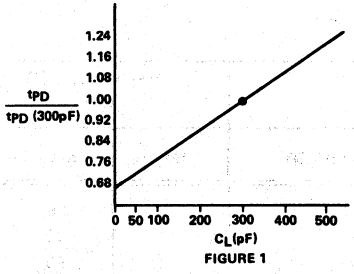


FIGURE 1

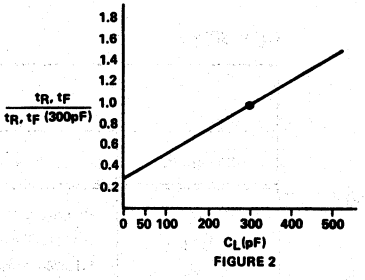


FIGURE 2

The above example will illustrate the calculation of a more useful propagation delay. The system in this example uses a 5 volt supply with a tolerance of ±10%, an ambient temperature of as high as 125°C, and a calculated load capacitance of 150pF. This application requires the HD-6495-2. The table of A.C. specs shows that t_{PD} at 4.5V and 125°C is 45nsec. Use the graph in Figure 1 to get the degradation multiple for 150pF. The number shown is 0.84. The adjusted propagation delay, to the 10% or 90% point, is therefore 45 x 0.84 or 38nsec. To obtain the rise and fall times check the A.C. specs for the rise and fall times at 4.5V and 125°C to obtain a worst case rise time of 95nsec. Use Figure 2 to find it's degradation multiple to be 0.65. The adjusted rise time is, therefore, 95 x 0.65 or 62nsec. To obtain the standard 50% to 50% propagation delay, add the adjusted propagation delay to half of the adjusted rise time to get a propagation delay of 69nsec. The rise time was used here because it is always the worst case.

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

MONOLITHIC DIODE MATRICES

JUNE 1978

Features

- FIELD PROGRAMMABLE
- CMOS COMPATIBLE
- ZERO POWER DISSIPATION
- FAST SWITCHING
- FIVE POPULAR ORGANIZATIONS

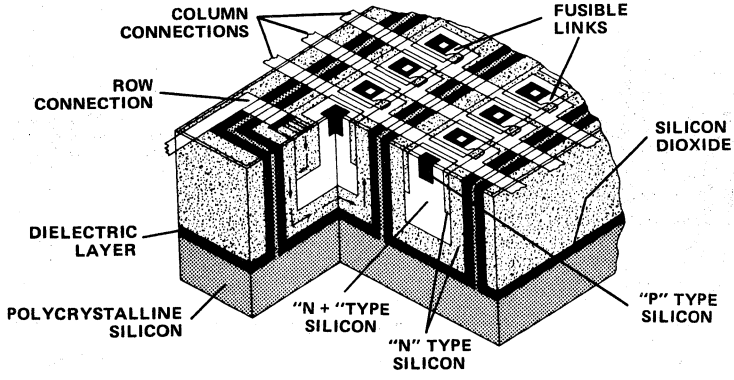
Description

Designed with the CMOS circuit engineer in mind, these versatile diode matrices allow the application of logically powerful programmable solutions to low power CMOS system applications.

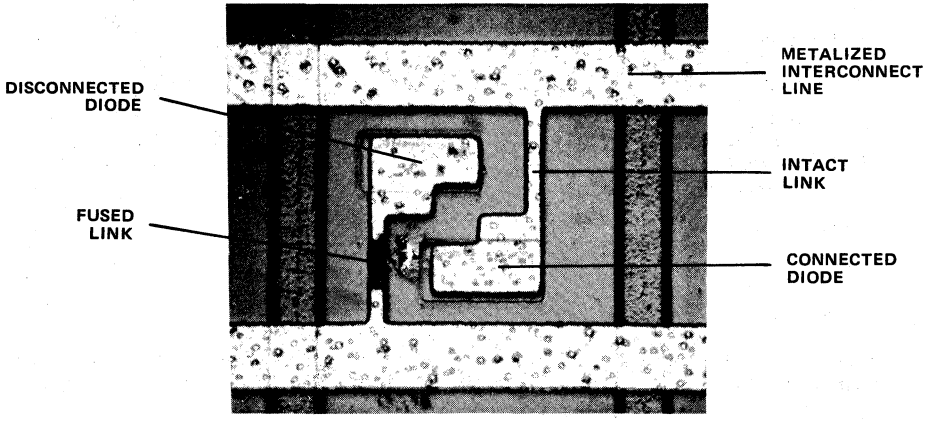
These devices incorporate an advanced dielectric isolation process to eliminate the need for power supply pins and allow parasitic free operation.

Programming is accomplished by cleanly vaporizing a fusible link by application of a brief high voltage pulse to a selected array element. This operation open circuits a row to column orring diode eliminating their former interaction.

Monolithic Structure



Fusible Link System

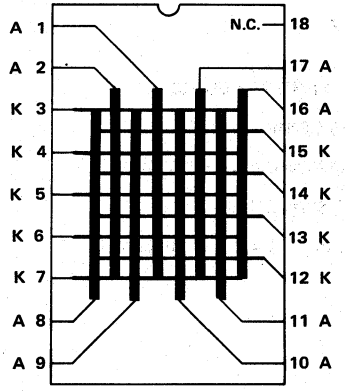


Monolithic Diode Matrices

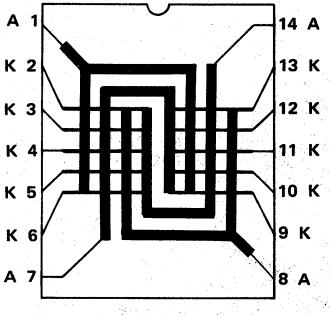
HM-0168 6 x 8 DIODE MATRICES
HM-0186 8 x 6 DIODE MATRICES
HM-0410 4 x 10 DIODE MATRICES
HM-0104 10 x 4 DIODE MATRICES
HM-0198 9 x 8 DIODE MATRICES

NOTE: Anodes are bold lines.

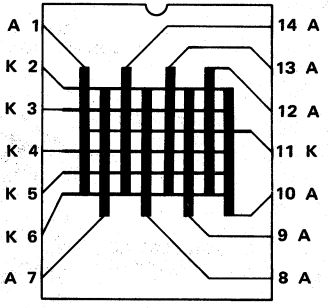
HM-0198



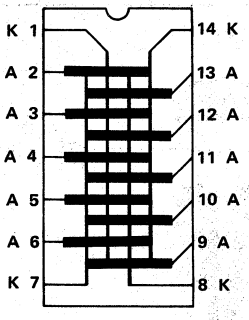
HM-0104



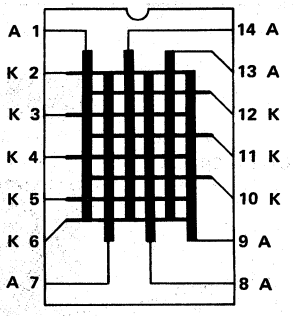
HM-0168



HM-0410



HM-0186



CUSTOM PATTERNS

When ordering a matrix with a custom pattern: Send a paper tape, or copy a matrix pattern and circle out those diodes to be removed from the matrix. Another method to clearly identify a pattern is to call out respective anode and cathode for each diode to be removed, by package pin number.

ABSOLUTE MAXIMUM RATINGS

Forward Current	100mA
Surge Current (100 μs Max.)	200mA
Total Ckt. Dissipation (Still Air)	450mW
Storage Temperature (Ambient)	-65°C to +150°C

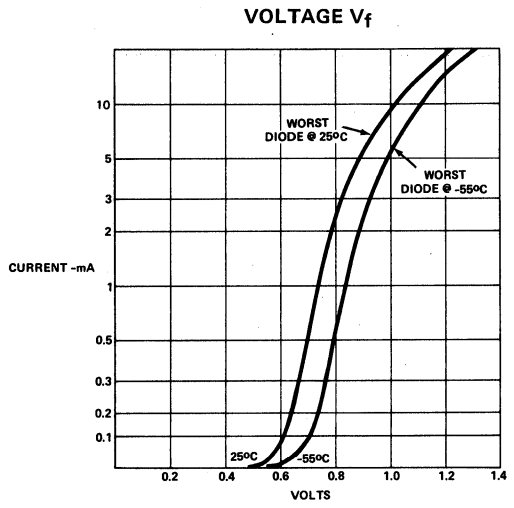
Maximum Ratings are limiting values above which permanent damage may occur.

ELECTRICAL CHARACTERISTICS

		HM-0XXX-5		HM-0XXX-2 HM-0XXX-8			
	T_A	0°C to +75°C		-55°C to +125°C			
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS	CONDITIONS
V_F	Forward Voltage		1.5 0.9		1.5 .9	V V	I_F = 20mA I_F = 1mA
BV_R	Reverse Breakdown Voltage	20		30		V	I_{BV} = 100μA
		25°C		25°C			
t_{rr}	Reverse Recovery Time		100		50	ns	I_F = 10mA to I_R = 10mA Recovery to 1mA
C_C	Crosspoint Capacitance				8	pF	V_R = 5V; f = 1MHz (1)

(1) $C_C \propto \frac{1}{V_{BIAS}}$

TYPICAL PERFORMANCE CURVES

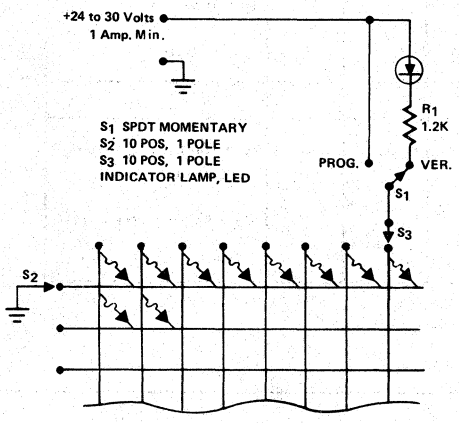


Programming

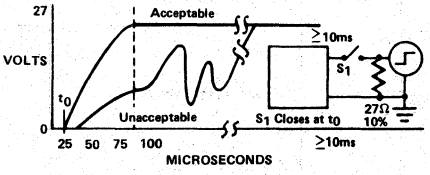
Use a simple supply capable of driving a 27 ohm resistor (carbon) when S1 depressed with a clean transition from 0 to 24-30 volts in less than 100 μs for min time of 10ms. The diode to be disconnected is selected by setting the row and column switches S2 and S3 respectively as required. When switch S1 is depressed programming current is provided to column contacts on the matrix. This current opens the fusible link in series with the selected diode. The peak fusing current required to open a fusible link is approximately 750 milliamperes. As the temperature of the fuse is raised, the aluminum begins to melt. This melting continues until the fuse link separates. The cohesive forces of the melting aluminum retracts the remaining portions of the metal, thereby preventing formation of loose aluminum residues. The melting temperature of aluminum at approximately 650°C will not affect the passivating layer of silicon dioxide whose melting temperature is about 1350°C. Test verification is obtained by an indicator lamp or LED placed in series with the column and row switches through the verify contacts of S1 to give electrical indication of the condition of each diode in the matrix before and after fusing.

Caution: Programming is limited to one fuse at a time.

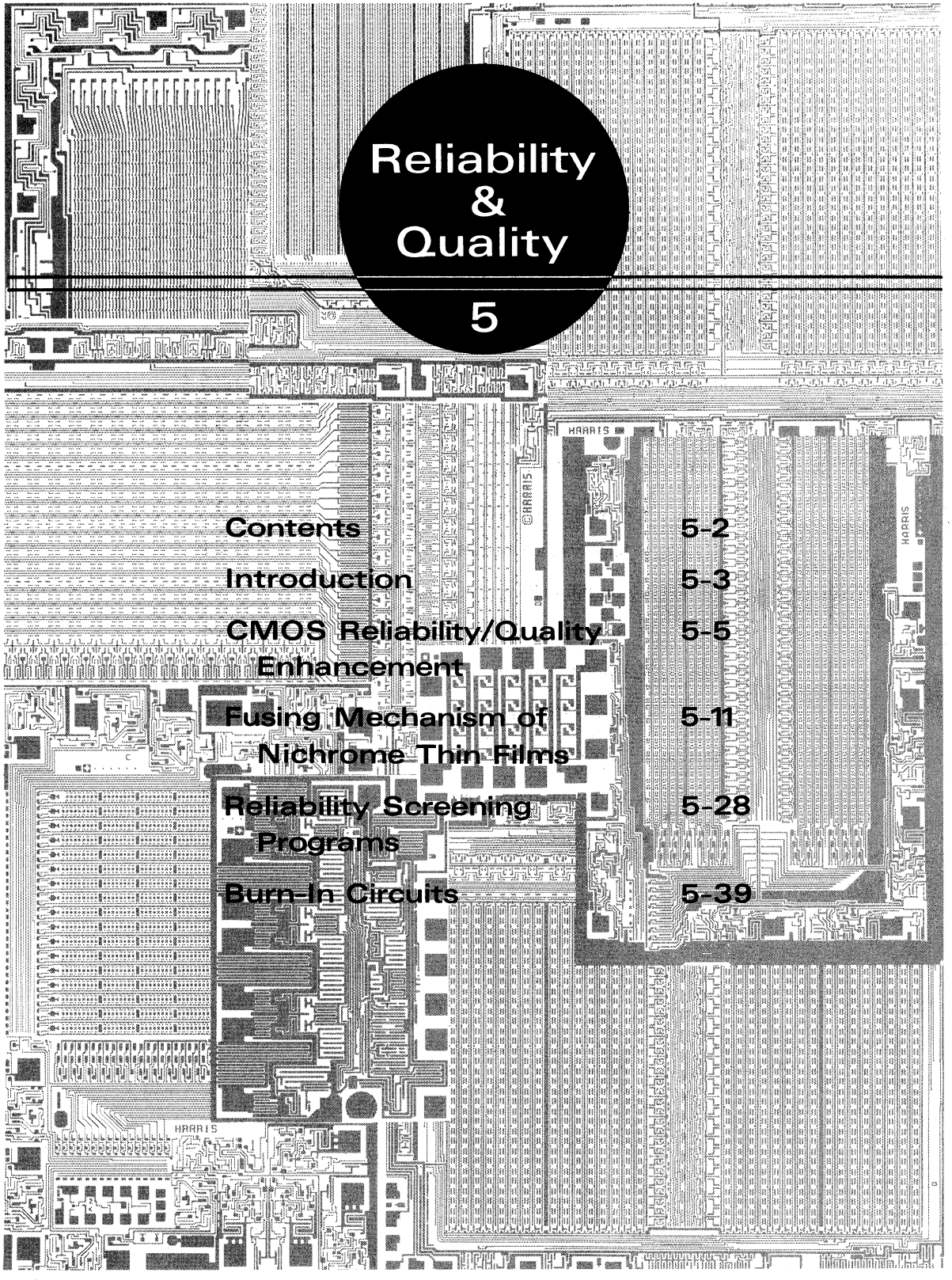
SIMPLE PROGRAMMER



PROGRAMMER TEST CONFIGURATION



NOTE: The 27 ohm resistor is only used for oscilloscope measurements of the Power Supply Characteristics becaues it represents a typical unprogrammed fuse/diode.



Reliability & Quality

5

Reliability & Quality Contents

Harris Reliability & Quality

Introduction

The Product Assurance Department at Harris Semiconductor Products Division is responsible for assuring that the quality and reliability of memory products shipped to customers meets their requirements. During all phases of product fabrication, there are many independent visual and electrical checks performed by Product Assurance personnel.

Prior to shipment, a final inspection is performed at Quality Assurance Plant Clearance to insure that all requirements of the purchase order and customer specifications are met.

The following military documents provide the foundation for Harris Product Assurance Program.

MIL-M-38510D	"General Specification of Microcircuits"
MIL-Q-9858A	"Quality Program Requirements"
MIL-STD-883B	"Test Methods and Procedures for Microelectronics"
NASA Publication 200-3	"Inspection System Provisions"
MIL-C-45662A	"Calibration System Requirements"
MIL-I-4508A	"Inspection System Requirements"

The Harris Semiconductor Reliability and Quality Manual, which is available upon request, describes the total function and policies of the organization to assure product reliability and quality. All customers are encouraged to visit the Harris Semiconductor facilities and survey the deployment of the Product Assurance function.

Quality Control

All critical processing steps for memory products are subject to rigid process control monitoring.

For example, to insure process stability of CMOS fabrication, frequent qualification of diffusion furnaces, metallization and passivation equipment by C-V plotting techniques is performed. The C-V plot method provides a very sensitive monitor of the amount of ionic contamination present in the processing equipment, and assures clean process with built-in reliability. Process controls of this kind are one reason Harris products have an excellent reliability record.

Another example, in the case of bipolar memory circuits, is the nichrome fusible link process. This process is rigorously controlled by frequent measurements of parameters such as resistivity and dimensions. Consistent and controlled execution of this process has led to very reliable PROMs of high programmability.

The above are only a few of the many process controls instituted to ensure high quality and reliable products. Some other examples are listed below:

- In-line SEM inspection
- Continuous environmental monitoring for particle count, temperature and humidity
- Oxide and metallization thickness measurements
- Doping concentration and profiles
- Pre and post etch inspections
- Prescribed interval calibration and preventative maintenance of processing equipment
- Total documation of specifications and change control procedures

The Product Assurance department also maintains a well equipped Analytical Services Department. This area is equipped with a complete electron microscopy laboratory, including Scanning Electron microscopes with energy dispersive x-ray analysis capability, electron microprobe, a Scanning Auger microscope with ESCA attachment, and all sample preparation equipment. The Analytical Services Department also has a complete physical chemistry laboratory utilized for analyzing the products and process materials for memory circuits. Equipment in this section includes atomic absorbtion flame emission spectrometry, arc emission spectrography, gas chromatography, a research grade talystep, an ultraviolet spec-

trophotometer and an infrared spectrophotometer. This section also contains a complete wet chemical analysis laboratory.

Further, to ensure high quality metal deposition, critical die areas are monitored via in-process SEM.

Reliability

The reliability approach at Harris Semiconductor is based on designing in reliability rather than testing for reliability only. The latter is applied to check and confirm that sound design with quality and reliability ground rules are observed and correctly executed in a new product design.

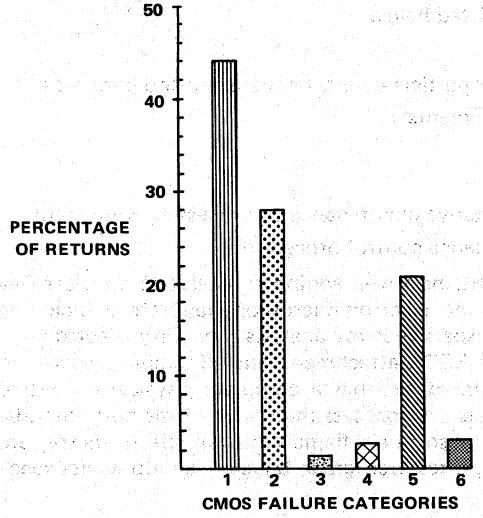
Reliability engineering becomes involved as early as concept review of a new product and continues to remain involved through design and layout reviews. At these critical development points of a new design, basic reliability layout guidelines are invoked to insure an all-around reliable design. This concept is reflected by the Harris reliability procedures which encompass mandatory first run product evaluation. This is done at not only the circuit level, but also at the process and package level. Reliability engineering approval is required before new product designs are released to manufacturing.

Both maximum rated and accelerated stress conditions are performed. Acceleration is important to determine how and at what stress level a new design would fail. From this information, necessary design changes can be implemented to insure a wider and safer margin between the maximum rated stress condition and the device's stress limitation.

The notably low failure rates for the Bipolar and CMOS Memory products are a direct result of the application of this reliability concept. For the PROM circuits, the high standards for reliability and quality have yielded the industry's highest programmability yields. Our demonstrated expertise with NiCr fusing has resulted in observed failure rates which are less than equivalently complex TTL LSI circuits. Conservatively derating to +25°C gives a failure rate of .020%/1kHrs. for programmed 76XX Bipolar PROMs and a value of .013%/1kHrs. for the 65XX CMOS Memory products.

The excellent reliability performance is further exemplified by our customers. Analysis of parts returned to Harris indicates the following results. For the CMOS Memory products, the returns constitute 0.2% of the total volume shipped, while for the Bipolar Memory products this figure is 1.5%. This number includes all programmability rejects for the PROMs.

The accompanying charts illustrate the distribution of categories for why devices are returned. Note that 60–70% of these returned are devices that were not defective as shipped. These units failed due to electrostatic damage (ESD), electrical overstress (EOS), or were good devices which were incorrectly identified as board or system level failures. The latter category is defined as invalid returns and represents 30–40% of the total number of returned units.



CUSTOMER INDUCED PROBLEMS: 73.5%
OF RETURNED UNITS

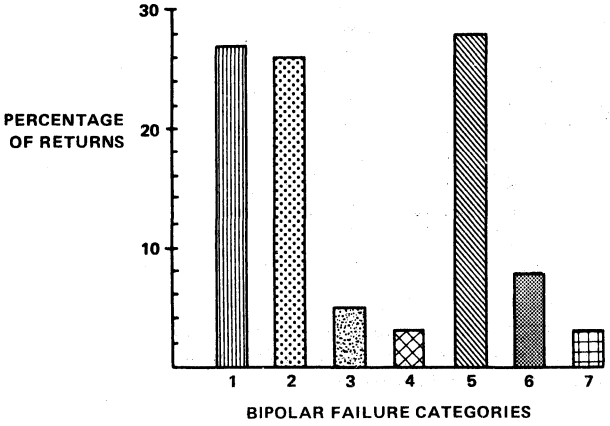
1. **INVALID RETURNS 44%**
2. **ELECTROSTATIC DAMAGE 28%**
3. **EOS, V_{CC} SPIKES 1.5%**

OBSERVED FAILURE MODES 26.5%:

4. **ASSEMBLY 2.5%**
5. **PROCESSING FLAWS 21%**
6. **TEST ESCAPES 3%**

RETURNED UNITS EQUAL ≅0.2% OF TOTAL PARTS SHIPPED

SUMMARY BASED ON RESULTS OBTAINED DURING THE INTERVAL 8/'77 – 3/'78



CUSTOMER INDUCED PROBLEMS: 61% OF RETURNED UNITS

1. INVALID RETURNS 27%
2. CUSTOMER PROGRAMMING PROBLEMS 26%
3. BLOWN BOND WIRES (REVERSE INSERTION) 5%
4. EOS, V_{CC} SPIKES 3%

OBSERVED FAILURE MODES:

5. PROCESSING FLAWS . . . 28%
6. ASSEMBLY 8%
7. TEST ESCAPES 3%

RETURNED UNITS EQUAL $\simeq$ 1.5% OF TOTAL PARTS SHIPPED

SUMMARY BASED ON RESULTS OBTAINED DURING THE INTERVAL 9/'76 – 3/'78

Section 1. CMOS Reliability/Quality Enhancement

To ensure a totally reliable product and system, the design engineer needs to understand the capabilities and limitations of the CMOS product. In addition, a clear understanding of the techniques employed to improve reliability is essential for High Reliability system goals. The following describes the necessary tools to enhance CMOS reliability.

DESIGNING OUT FAILURE MODES

Static Charge

Since the introduction of MOS, manufacturers have searched for effective and safe ways of handling this sensitive device. High input impedance of CMOS, coupled with gate-oxide breakdown characteristics, result in susceptibility to electrostatic charge damage.

Figure 1 shows a cross-section of silicon gate MOS structure. Note the very thin oxide layer ($\approx$ 1000Å)* present under the gate material. Actual breakdown voltage for this insulating layer ranges from 70 to 100V.

Handling equipment and personnel, by simply moving, can generate in excess of 10kV of static potential in a low humidity environment. Thus, static voltages, in magnitudes sufficient to damage delicate MOS input gate structures, are generated in most handling environments.

A failure occurs when a voltage of sufficient magnitude is applied across the gate oxide causing it to breakdown and destruct. Molten material then flows into the void creating a short from the gate to the underlying silicon. Such shorts occur either at a discontinuity in doping concentration, or at a defect site in the thin oxide. If no problems appear in the oxide, breakdown would most likely occur at gate/source, or gate/drain intersection coincidence due to the doping concentration gradient.

Noncatastrophic degradation may result due to overstressing a CMOS input. Sometimes an input may be damaged, but not shorted. Most of these failures relate to damage of the protection network, not the gate, and show up as increased input leakage.

*1Å (Angstrom = 10^{-8}cm)

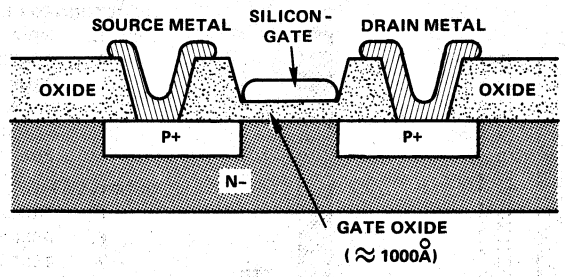


FIGURE 1 — Silicon-gate PFET structure cross-section shows the heavily doped source and drain regions. They are separated by a narrow gap over which lies a thin-gate oxide and gate material.

Voltage Limiting Input Protection

During the evolution of monolithic MOS, manufacturers developed various protection mechanisms that are an integral part of the circuit. However, several of these earlier techniques have been replaced by improved methods now in use. The object of most of these schemes is to prevent damage to input-gate structures by limiting applied voltages.

Recent CMOS designs employ a dual-diode concept in their input protection networks. Figure 2 illustrates such a protection circuit.

One characteristic of junction-isolated CMOS protection circuits is the $\approx 200\Omega$ current limiting resistor. Cross sectional area of the metallization leading to the resistor, and the area of the resistor are, therefore, designed to absorb discharge energy without sustaining permanent damage. This dual-diode protection has proved very effective and is the most commonly used method in production today.

HARRIS INPUT GATE PROTECTION

To protect input device gates against destructive overstress by static electricity accumulating during handling and insertion of CMOS products, Harris provides a protection circuit on all inputs. The general configuration of this protection circuit is shown in Figure 2.

Both diodes to the V_{DD} and V_{SS} lines have breakdown voltages averaging between 35 and 40 volts. Excessive static charge accumulated on the input pin is thus effectively discharged through these diodes which limit the voltage applied from gate to drain and source. The 200 ohm resistor provides current limiting during discharge. Depending on the polarity of the input static charge and on which of the supply pins is grounded, the protective diodes may either conduct in the forward direction or breakdown in the reverse direction.

In order to test this concept, step stress tests have been performed at Harris using an approximate equivalent circuit to simulate the static charge encountered in handling operations. The equivalent circuit consists of a 100pF capacitor in series with a 1.5K ohm resistor and is considered the rough equivalent of a human body. Step stressing takes the form of charging the capacitor to a given voltage and then discharging it into an input pin of the CMOS device under test according to the sequence given in MIL-STD-38510.

Stress Voltage	Cumulative Failures
500	0
700	0
1000	0
1500	1
1700	3
1800	4

These results indicate that the input protection used for Harris CMOS products provides adequate protection against static electricity based on the limits specified in MIL-STD-38510.

There are two trade-offs to consider when fabricating an input protection scheme. Effectiveness of the overvoltage protection, and performance of the overall circuit. It is obvious that increasing series resistance and capacitance at an input limits current. This, in turn, increases the input protection's ability to absorb the shock of a static discharge. However, such an approach to protection can have a significant effect on circuit speed and input leakage. The input protection selected must provide a useful performance level and adequate static-charge protection.

Commonly used MOS-input protection circuits all have basic characteristics that limit their effectiveness. The zener diodes, or forward-biased pn-junctions, employed have finite turn-on times too long to be effective for fast rise-time conditions. A static discharge of 1.5kV into a MOS input may bring the gate past its breakdown level before the protection diodes or zener becomes conductive.

Actual turn-on times of zeners and pn-diodes are difficult to determine. It is estimated that they are a few nanoseconds and a few tens of picoseconds, respectively. A low-impedance static source can easily produce rise times equal to or faster than these turn-on times. Obviously the input time constant required to delay buildup of voltage at the gate must be much higher for zener, or other schemes having longer turn-on times.

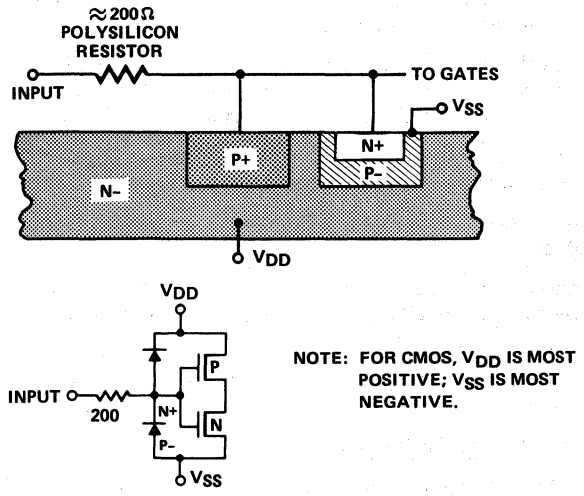


FIGURE 2 — Junction isolated dual-diode protection networks are most commonly used in today's CMOS circuits.

Consider an example. Figure 3 shows a test circuit that simulates the discharge of a 1.5kV static charge into a CMOS input. Body capacitance and resistance of the average worker is represented by a 100pF capacitor through 1.5kΩ. Switch A is initially closed, charging 100pF to 1.5kV with switch B open. Switch A is opened, then B is closed, starting the discharge. With the 1.5KΩ x 5pF time constant to limit the charge rate at the DUT input, it would take approximately 350psec to charge to 70V above V_{DD}. Diode turn-on time is much shorter than 350psec, hence the gate node would be clamped before any damage could be sustained.

There is no completely foolproof system of chip-input protection presently in production. If static discharge is of high enough magnitude, or sufficiently short rise-time, some damage or degradation may occur. It is evident, therefore, that proper handling procedures should be adopted.

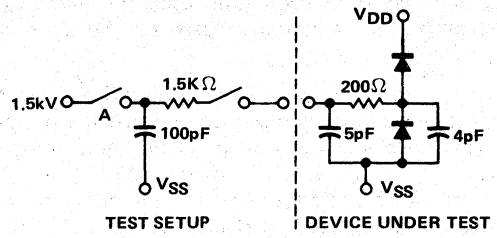


FIGURE 3 – Input protection network test setup illustrates how diode clamping prevents excessive voltages from damaging the CMOS device.

HANDLING RULES

Elimination or reduction of static charge can be accomplished as follows:

- Use conductive work stations. Metallic or conductive plastic* tops on work benches connected to ground help eliminate static build-up.
- Ground all handling equipment.
- Gound all handling personnel with a conductive bracelet through 1 MΩ to ground. The 1MΩ resistor will prevent injury.
- Smocks, clothing, and especially shoes of certain insulating materials (notably nylon) should not be worn in areas where devices are handled. These materials, highly dielectric in nature, will hold or aid in the generation of a static charge.
- Control relative humidity to as high a level as practical. A higher level of humidity helps bleed away any static charge as it collects.
- Ionized air blowers reduce charge build-up in areas where grounding is not possible or deisrable.
- Devices should be in conductive carrriers during all phases of transport. Leads may be shorted by tubular metallic carriers, conductive foam or foil.
- In automated handling equipment, the belts, chutes, or other surfaces the leads contact should be of a conducting nature. If this is not possible, ionized air blowers may be a good alternative.

THE FORWARD-BIAS PHENOMENON

Monolithic CMOS integrated circuits employ a single-crystal silicon wafer into which FET sources and drains are implanted. For complex functions many thousands of transistors may be required and each must be electrically isolated for proper operation.

Junction techniques are commonly used to provide the required isolation – each switching node operating reverse-biased to its respective substrate material. Additionally, as previously mentioned, protection diodes are provided to prevent static-charge related damage where inputs interface to package pins. Forward-biasing any of these junctions with or without power applied may result in malfunction, parametric degradation, or damage to the circuit.

*Supplier: 3M Company "Velostat".

Before proceeding, it should be pointed out that junction isolation, in the classical sense, is not implemented in the CMOS structure. Although commonly called junction isolation, the CMOS technique varies substantially from that used in bipolar TTL (Figure 4).

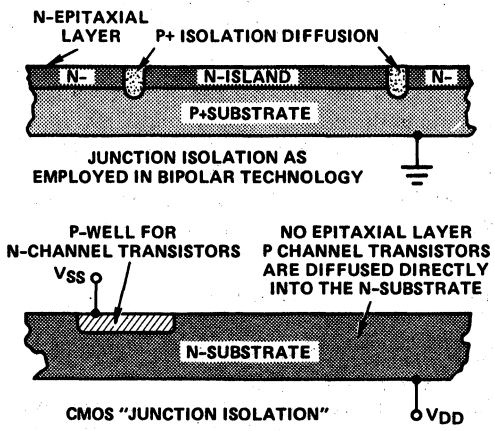


FIGURE 4 – Junction isolation for bipolar and CMOS differ considerably. CMOS utilizes a simpler technique that takes advantage of its less complex processing.

ELECTROMIGRATION AND FUSING

An aluminum metallization system is used for on-chip interconnect and wire bonding of most CMOS integrated circuits. On-chip metallization means a very pure grade of aluminum deposited on the surface of a silicon wafer. A subsequent metal etch defines the interconnect pattern.

This on-chip metallization can be subject to two primary current-density related failure modes, electromigration and fusing.

Electromigration results from displacement of metal atoms due to high current densities. Displacement of atoms creates physical holes in the metal structure that enlarge with time, eventually causing an open circuit. Under extreme circumstances, displacement can be sufficient to short to an adjacent line. Current density levels for which circuit life is not impaired are subjects of considerable debate. One figure, generally considered to be ultra-safe, is $10^5 A/cm^2$.

Considerably higher current densities, on the order of $10^6 - 10^8 A/cm^2$, are required to cause fusing. For a 0.3 mil wide, 40 μ inch thick aluminum line and a fuse current density of $10^7 A/cm^2$, 775mA will cause fusing. Current levels of this magnitude are not generated during normal CMOS operation.

Could a high-energy static discharge into a CMOS input or output cause fusing ? Yes, but such a failure would most likely occur due to heavily forward-biasing an input or output through a low impedance.

High currents resulting from an excessive forward-bias can cause severe overheating localized to the area of a junction. Damage to the silicon, overlying oxide and metallization can result.

BIPOLAR PARASITICS

Care must always be exercised not to forward-bias junctions from input or output pads.

A complex and potential defect phenomenon is the interaction of a npn/pnp combination a la SCR (Figure 5). Forward-biasing the base-emitter junction of either bipolar component can cause the pair to latch-up if βnpn x βpnp ≥ 1. The resultant low impedance between supply pins can cause fusing of metallization or over-dissipation of the chip.

Figure 5 shows how an SCR might be formed. The p+ diffusion labeled INPUT is connected to aluminum metallization and bonded to a package pin. Biasing this point positive with respect to V_{DD} supplies base drive to the pnp through R2. Although gain of these lateral devices is normally very low, sufficient collector current may be generated to forward-bias and supply substantial base current to the vertical npn parasitic. Once the pair has been activated, each member provides the base current required to sustain the other. A latched condition will be maintained until power is removed or circuit damage disables further operation.

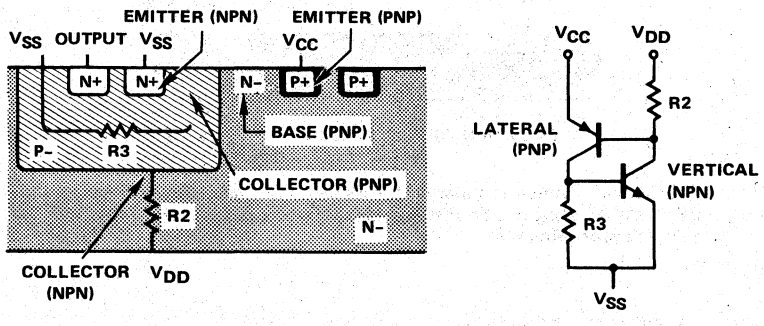


FIGURE 5 — Improper biasing can latch-up this SCR configuration. A p+ guard ring is commonly used to kill lateral pnp action. This ring is diffused into the surface at the junction of p- and n- silicon.

DESIGN RULES EQUALLY IMPORTANT AS HANDLING RULES

A system using CMOS must have reliability designed in. No amount of testing can guarantee long term reliability when poor design practices are evident.

- Never apply signals to a CMOS circuit before power has been turned on.
- Where multiple supply voltages are used in a CMOS system, be sure to properly sequence power-up and power-down.
- Supply filter capacitance should be distributed such that some filtering is in close proximity to supply pins of each package. Testing has shown 0.01 μF/package to be effective in filtering noise generated by most CMOS functions.
- CMOS signal lines are terminated at the driving end by a relatively high impedance when operating at the low end of the supply voltage range. This high-impedance termination results in vulnerability to high-energy or high-frequency noise generated by bipolar or other non-CMOS components. Such noise must be held to manageable levels on both CMOS power and signal lines.
- Where CMOS must interface between logic frames or between different equipments, ground differences must be controlled in order to maintain operation within absolute maximum ratings.

- Capacitance on a CMOS input or output will result in a forward-bias condition when power is turned off. This capacitance must discharge through forward-biased input or output to substrate junctions as the bus voltage collapses. Excessive capacitance (thousands of pF) should be avoided as discharging the stored energy may generate excessive current densities during power-down.
- Where forward-biasing is inevitable, current limiting should be provided. Current should not be permitted to exceed 1mA on any package pin excluding supply pins.

All CMOS is susceptible to damage due to electrical overstress. It is the user's responsibility to follow a few simple rules in order to minimize device losses.

He should first select a source for the CMOS device that employs an effective input protection scheme. This will allow a greater margin of safety at all levels of device handling since the devices will not be quite so prone to static charge damage. Next, he should apply a sound set of handling and design rules. At minimum, this will eliminate electrical stressing or hold it to manageable levels.

With an effective on-chip protection scheme, good handling procedures and sound design, users should not lose any CMOS devices to electrical overstress.

Section 2. Fusing Mechanism of Nichrome Thin Films

*Fusing Mechanisms of Nichrome Thin Films**

J. L. Davidson, J. D. Gibson, S. A. Harris, and T. J. Rossiter

Nichrome fusible link programmable read-only memories, PROM's, have been developed and utilized for over 7 years[1]. The physical mechansim of fusing these resistors has been generally described as melting[2], but only in the last 2 years, with the advent of a successful transmission electron microscopy technique[3], has detailed information on the structure of the programmed fuse gap become available. These observations, coupled with electrical and thermodynamic characterization of the fusing event, have led to a clearer understanding of this phenomena with concurrent definition of programming conditions for reliable operation of programmed PROM's.

SOME RELEVANT GENERAL PROPERITIES OF NICHROME

Fundamental to the mechanism of nichrome fusing are those physical properties that make it an excellent resistor material from a processing, design and applications perspective. It is no accident of history that nichrome is widely used for resistors on solid state devices.

To begin with, nichrome is a resistive material comprised of two transition metals – nickel and chromium. In transition metals, the outer electron shells contain only one or two electrons and some of the conduction electrons must come from inner shells. The inner shell conduction electrons are shielded by the outer shell resulting in a high scattering and trapping site density. Thus, transition metals are inherently less conductive than normal metals[4]. In the case of nichrome, an alloy effect[4] occurs to further enhance electron scattering. The result is that the resistance of the alloy is much higher than the arithmetic average of its two components[5] as illustrated in Figure 1**.

The resistivity of nichrome makes it well suited for small geometry thin film resistors that are size compatible with high density fuse design requirements. Due to its high resistivity, the thickness of nichrome that is necessary to achieve a typical fuse resistance of 300 ohms is about 200Å. The small cross-sectional area of the nichrome resistor (as compared to polycrystalline silicon, for example) is an advantageous property for a fuse, as will be described later. There is also the elimination of step coverage problems where the metallization (aluminum) contacts the nichrome.

*Presented at IEEE International Reliability Physics Symposium, 1976.

**Figure Drawings found on Pages 5-18 Thru 5-22.

A consequence of the extensive electron scattering in nichrome is a short mean free path of the conduction electrons. For example, the mean free path in gold is 380Å[6] compared to an estimated 40Å for nichrome. As a consequence, films greater than 100Å thick have bulk resistivity properties (i.e., surface effects are not dominant). As Figure 2 shows, surface scattering effects which reduce conduction are absent by the time the resistor film is greater than 100Å[7] in thickness. The practical ramification of this property is reproducibility in the fabrication process. Because there is no dependence on surface effects to achieve the desired sheet resistivity, thin film resistors may be produced with excellent tolerance and stability[8].

The short mean free path is also relevant to describing the fusing mechanism, discussed in the Mass Transport Models section.

Nichrome is a material that forms a self-limiting oxide skin. That is, the oxide of nichrome is known to be a coherent spinel[9,10], see Figure 3. It is postulated that in the course of processing nichrome resistors, this thin spinel sheath will form around the nichrome to a thickness of $\simeq$ 20Å. This sheath serves to stabilize the resistors and is partly responsible for the excellent thermal stability (absence of $\Delta R(T)$ effects) of nichrome[11]. This spinel may also be a factor in the fusing phenomena.

MICROSTRUCTURE OF A PROGRAMMED NICHROME FUSE

The technique of using transmission electron microscopy (TEM) to examine programmed fuse gaps was developed by Dr. Kinsey Jones at C. S. Draper Labs[3,12]. It is the only technique which mutually satisfies the requirements of sufficient resolution to analyze the gap and not destroy in sample preparation the structure to be analyzed. It is this latter point that has severely limited the utility of the scanning electron microscope (SEM) in endeavors to analyze programmed nichrome fuses. In depassivating devices, necessary with the SEM, microstructural details of the fuse gap are destroyed. Many interpretations of the fusing phenomenon based on SEM results have been erroneous or misleading because what was seen was an artifact of sample preparation.

Figure 4 illustrates schematically the utilization of transmission electron microscopy for fuse gap analysis. Of course, besides direct structure observation, composition of various phases may be ascertained by electron probing.

The microstructure of a programmed fuse gap in a PROM circuit via TEM is shown in Figure 5. The relevance of those programming conditions will be discussed further in following sections, but Figure 5 is representative of the gap created in a nichrome fuse under programming power conditions specified[13] for PROM's.

The TEM photograph indicates the elemental distribution found by microprobing. The following observations are made:

a. The visual appearance indicates that the neck of the fuse was in the molten state during programming.

b. Mass transport of the nickel and chromium from the gap region has occured.

c. There is asymmetry to the melted nichrome distribution. That is, there is more densified nichrome on what was the cathode (negative) side of the fuse which suggests the molten nichrome moved in a direction opposite to electron flow during programming.

d. The gray phase (region C) of the gap which comprises the insulative separation of the two sides of the fuse is devoid of nickel and composed of oxides of silicon and chromium[14]. The typical separation is 0.6-1.0 microns. The resistance across the gap is $>$ 10 megohms and it will not break down, electrically or structurally to voltages in excess of 100 volts.

e. The white spots, dark spots and filaments are described by the fluid dynamics of a disintegrating liquid sheet[12]. Briefly, that model describes how minute discontinuities in a liquid sheet, perterbate into larger holes and finally into droplets and filaments because of surface tension effects. The structure looks similar to a "frozen splash".

MASS TRANSPORT MODELS

In the previous section, it has been demonstrated that programmed nichrome fuses melt and that mass transport takes place. But what is the mechanism, the driving force for mass transport ? Table 1 lists the possibilities.

Table 1

(1) Electromigration (Huntington & Grone[15]): Mass flux occurs under the influence of high current flow because electron collisions with atoms of the conducting medium provide a net motion vector in the direction of electron flow.

(2) Thermal gradient (Soret[16]): In the presence of a thermal differential, material will diffuse from the high temperature to the cold temperature region.

(3) Concentration gradient (Fick[17]): In an imbalanced distribution of concentration, mass will diffuse from regions of higher concentration to lower concentration.

(4) Field enhanced ionic mobility (Eyring and Jost[18]): Molten metals will ionize, lose electrons and become cations. In the presence of an electric field, they will be driven towards the cathode.

Considering each possible mechanism in turn:

(1) Electromigration – On the surface, this seems a most logical explanation for programming. It is known that the current densities in a fuse neck at programming are very high ($\sim 5 \times 10^7$ amps/cm2) and it could be postulated that this electron flux sweeps the nickel and chromium from the gap. But empirical data and theoretical considerations show this not to be the case.

a. TEM of the fuse gap indicates the molten nichrome has moved in a direction opposite to electron flow.

b. Theoretical calculations of the kinetic energy of conduction electrons in nichrome demonstrate that because the mean free path is short and the lattice binding energy is high (transition metals typically have high melting points), the electrons have insufficient energy to impart the mobility to the nickel and chromium atoms necessary for electromigration in the direction of electron flow.

However, general treatments of electromigration theory[15, 24] identify two forces acting on atoms of the conducting medium. One is the aforementioned electron momentum ("electron wind") in the direction of electron flow. The other is the electrostatic force from the applied electric field that causes ions of the conducting material to move opposite to the direction of electron flow. See mechanism (4).

Obviously, the joule heating that leads to melting the fuse is coming from electron interaction with the nichrome film. There is no incongruity with the fact that this is not leading to electromigration such as observed in aluminum. Because the mean free path is short, the energy exchanged per collision is small. But because electron scattering is a dominant factor in resistive materials, the frequency of collisions is high. Thus, thermal energy (lattice vibration) is added to the metal atoms. The electron collisions increase the amplitude of the atomic vibration and increase the temperature. This is why nichrome is an efficient material for converting electrical energy into thermal energy (toaster effect).

Footnote: Arguments have also been advanced that oxidation is the mechanism of fusing[19]. If this were so, the probe data, which discerns elemental presence, would not show nickel and chromium depletion in the gap region, i. e., mass transport, per se, would not have occured. Because the TEM data clearly indicates mass transport, attention is focused here on identifying the driving force for that mass transport.

(2) Thermal Gradient – From an analysis of heat flow in a fuse, it has been shown (see the Transient Heat Flow Analysis section), Figure 6, that the temperature profile across a fuse neck is flat. The gradient occurs at the neck-to-fuse body interface. But the programmed gap occurs in a region where there is no temperature gradient. Further, this model would predict a symmetric distribution of mass, post-programming which is not observed. Temperature gradient does not cause the mass transport.

(3) Concentration Gradient – It has been shown in unprogrammed fuses that no concentration gradient exists. Laterally in the fuse film this is borne out by the TEM/probe analysis. That is, no nickel or chromium concentration variations are observed across an unprogrammed fuse. Vertically (distribution of nickel, chromium through a cross section of the resistor) it has been shown[20], from sputter etching Auger analysis that the nickel and chromium are distributed uniformly through the film (no concentration layering effects).

Because there is no concentration gradient initially, this is ruled out as a starting mechanism for fusing.

(4) Field Enhanced Ionic Mobility – Eyring and Jost[18] have observed that liquids have a fixed ratio between their energy as a liquid and the energy required for vaporization, see Figure 7. Stated simply, the principal is, the more cohesive the liquid, the more energy is required to transform it to the gaseous phase, and the ratio is a constant. This rule held for all types of liquids (gases, solvents, organics, etc.) except metals. But by accounting for ionization of molten metals and the subsequent reduction in atomic radii, see Table II, they found that metals obeyed the liquid:gas constant energy ratio. In other words, molten metals are ionic.

It follows then that these positive ions (they have given up outer shell electrons) will move in the presence of an electric field (from the programming pulse) toward the negative terminal, opposite to the direction of electron flow. This is consistent with the TEM observations and with some investigations of electromigration. For example, Wever[25] observed in copper above 950°C, that mass flux was toward the cathode.

In summary, nichrome fuses program as follows: A programming pulse of sufficient power is applied across the fuse. Power dissipation in the fuse neck heats this region into the molten state and the nickel and chromium atoms become ionized. They move toward the negative side of the fuse and the liquid film begins to disintegrate. The film becomes electrically discontinuous and rapidly returns to the solid state, the final structure resembling a frozen splash described by fluid dynamics. The fuse gap consists of insulative oxides of silicon and chrome, with resistance > 10 megohms.

TRANSIENT HEAT FLOW ANALYSIS

The previous discussions dealt with the fusing event postfacto, describing the microscopic material structure created by programming. The dynamics of the fusing event can also be characterized. By modeling the fuse structure and its environment in terms of classical heat flow, the connection between electrical and material behavior of fuses can be established.

A computer thermal analysis program called "THEROS"[21] was used to calculate the dynamic temperature effects in a PROM-fuse structure as a function of applied power density.

This computer program can thermally model a multicomponent structure and calculate the temperature as a function of time for given power dissipation conditions. The program takes into account temperature dependent thermal properties of the various materials and

models a 2-dimensional multimaterial, multigeometrical structure into a RC circuit network that can be analyzed by sophisticated transient circuit analysis programs. This approach is convenient because the differential equations that describe heat flow problems have the same form as differential equations for RC circuit networks. For example, specific heat is analogous to capacitance, thermal conductivity is analogous to the inverse of resistance, temperature is analogous to voltage and heat flow is analogous to current. By way of the "THEROS" heat flow to electrical analog program, the sophistication available with present circuit analysis programs can be utilized to solve complex heat flow problems without consuming hours of computer time and without the errors prevalent in more simplified calculations. For the heat flow model to be truly representative of the actual device, the immediate environment of the fuse must be completely accounted for. For example, the passivating oxide layer on top of the fuse will affect the heat flow and the subsequent structure of the programmed fuse. Programming a fuse without the passivating oxide [22] will result in a different structure than occurs in an actual PROM circuit.

The term "power density" is defined as the amount of power that is dissipated in the fuse neck region divided by the area of the fuse neck (watts/mil^2), see Figure 8. The concept of defining power density as power per unit surface area is applicable to thin film heat flow problems where the heat is dissipated through a surface. (The concept is analogous to defining current density as current per cross sectional area). Figure 9 shows a plot of the computer results giving the temperature in the center of the nichrome fuse that would be achieved if a constant power were applied for a time t. The curves show that the fuse can easily reach the melt temperature of nichrome [23] within microseconds for power densities > 2.5 watts/mil^2.

Figure 10 is a plot of the intercept of the time to reach the melt temperature (1450°C) vs. the power density. This theoretical prediction of the power density versus time to reach the melt temperatures compares well with experimental data on time to fuse. The data in Figure 10 was taken from test vehicle fuses, processed identically to circuit fuses, but free of interfacing circuitry. This allowed precise characterization of fuse-pulse interactions. The data matches for long fusing time but deviates for short fusing time. This difference can be accounted for by considering the definition of "time to fuse". The experimental data points represent total time to fuse which includes rise time of the programming pulse, time for the fuse to heat to sufficient temperature, and time of the actual fusing event. For example, Figure 11 shows a typical current trace for a fuse programmed under constant voltage conditions. The trace shows a fixed rise time, t_r (about 100 nanoseconds for this data), a response time, t_m, for the nichrome to reach the melt temperature, and a time for the fuse neck to enter the melt phase and program, t_f. Plotting the time defined as t_m shows excellent correlation with the theoretical prediction of the time to reach melt temperature. The difference between the theoretical prediction to reach melt and the actual time to fuse agrees with the measured values of $t_r + t_f$. Figure 10, therefore, shows that fusing follows a heat flow dependence that requires the nichrome to achieve melt. Proper PROM design necessitates taking into account thermal factors that affect the heat flow conditions in the neighborhood of the fuse. Concentrating power by optimum fuse geometry and ensuring sufficient power to the fuse will achieve fast, uniform programming.

For power density conditions below the programming threshold level, the fuse temperature as a function of power density into a fuse for a sustained pulse ($t \longrightarrow \infty$) is shown in Figure 12. There is good agreement of the computer model with experimental data. The experimental data was derived from measuring the fuse resistance (at reduced current, avoiding I^2R heating) of an externally heated fuse and comparing that to the power necessary to generate the same resistance at an ambient temperature of 25°C. The agreement between model and experimental data is a further indication that the heat flow analysis is correctly projecting the temperature in the fuse.

It is also relevant to note the low power density on a fuse in the read mode, 5% of the threshold power density to melt the nichrome fuse. Test vehicle fuses were stressed at 1 watt/mil^2 which is 65% of the fusing threshold level and equivalent to a fuse temperature of 800°C. No failure occured after 4000 hours of continuous operation. Thus, the designed power density for PROM operation in the read mode avoids the occurence of unprogrammed fuses becoming open.

In summary, the power density vs. time to program curve, Figure 10, agrees with the heat flow model and implies a single mechanism, melting for both fast and slow fusing. High power fusing (fast blow) approaches adiabatic heating conditions and therefore gives a large melted region and wide gap. Restricted power programming (slow blow) allows much of the heat to diffuse away taking longer for the fuse to reach melt.

MARGINALLY PROGRAMMED FUSE

By grossly violating recommended programming procedures for fuses, it is possible to create a marginal fuse gap that may be subject to reverting state ("growback"). This anomaly was induced in a test vehicle fuse by restricting the power input to a value on the t $\rightarrow \infty$ asymptote ($\sim$ 1.5 watts / mil^2) of the power density vs. time to fuse curve (Ref. previous section, Figure 10). Under these conditions, a fuse was induced to program, become electrically discontinuous, after 5 minutes of sustained power. This effect, programming under an anomalously reduced power, was not found to be reproducible. Many fuses at this power would not program after days.

This deliberately improperly programmed fuse was subsequently subjected to a slowly applied DC voltage ramp under current limited conditions (10M resistor in series). At 12 volts, the fuse resistance dropped to $\sim$ 5000 ohms. The TEM photograph of this fuse is shown in Figure 13. It is obvious from this photograph that the reduced power condition has resulted in a fuse that has marginally programmed. That is, the gap created after programming is very narrow (approximately a few hundred angstroms) and subject to a voltage breakdown effect.

Fuses programmed per the recommended power levels will program rapidly with a wide gap as illustrated in the Mass Transport Models section. These fuses can be subjected to more that 100 volts and will undergo no change in electrical or physical condition.

As indicated in Figure 13, if a restricted amount of power is applied to a fuse, it is possible to create a very narrow gap. Under the presence of high voltage and extreme current limiting, it is then possible to force a voltage breakdown across the gap. It is postulated that this voltage discharge results in the establishment of a low conductivity relink at one or a few points of closest approach in the marginally blown gap. This specific structure could not be confirmed with the TEM study because even the TEM did not have resolution to examine microsturcture at $<$ 300 angstroms.

This mechansim of marginal programming is precluded from occuring in an actual PROM circuit because the programming specification, specifically the power and pulse widths, have been established to only generate well blown, wide gap fuses. That is, if the power actually reaching a fuse is lower than that required to blow the fuse properly, the fuse will not program in the time allotted for the programming pulse. The device, therefore, becomes a programming reject (won't program) and is scrapped.

In summary, the observation that a nichrome fuse can be marginally programmed has no connection with the reliability of the PROM circuit. Recall, to generate this anomaly, a power density four times less than the designed value and a program time $\sim 10^8$ times longer than the maximum specified programming time was required. Further, a voltage $\sim$ 10 times higher than the maximum that would be seen in an actual PROM, (with current limiting) was required to cause the relink.

Obviously, these observations and conclusions are based on nichrome fuses, PROM design, and control procedures as deployed by this manufacturer. Contentions by others that a specific fuse material, nichrome or something else, is more or less reliable must be interpreted in prespective of the manufacturer's technology and not necessarily be construed as being generally representative.

LIFE TEST RESULTS

Life testing data of programmed PROM's has been accumulated for several years of production. The data in Table III summarizes those results. The total sample base represents a multiplicity of designs and configurations (256, 512, 1024, 2048, and 4096 bit PROM's). These samples were selected from production runs that had passed the standard final test program and were programmed to data sheet programming procedure. The burn-in conditions are representative of typical applications (except for elevated temperature). The results indicate that the level of reliability of these PROM circuits is equivalent to circuits of similar complexity that do not utilize fusible links.

SUMMARY

(1) Conduction electrons in nichrome have a short mean-free path. This maximizes I^2R heating and precludes electromigration in the direction of electron flow as a fusing mechansim.

(2) Transmission electron microscopy is the only effective analytical tool to characterize the programmed fuse gap structure.

(3) Nichrome fuses program by molten metal (nickel, chrome), ions moving in the presence of an electric field. The final structure resembles a frozen splash and is described by fluid dynamics.

(4) Thermal analysis coupled with empirical programmed fuse data indicate a threshold power density for fusing. If this power density is exceeded, which can be assured if the programming time utilized is as specified, the fuse gap will be wide and reliable. If this power density threshold is only matched, it is possible to create a marginal fuse.

(5) Life test results indicate programmed PROM reliability is equivalent to devices of the same complexity that do not utilize fusible links.

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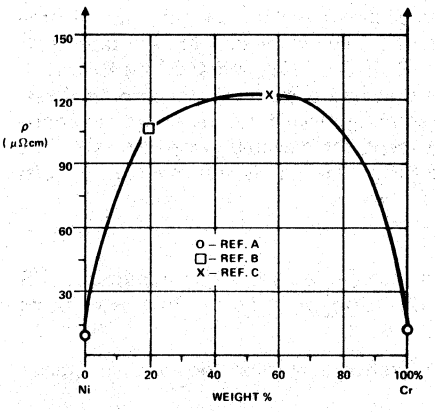
CONDUCTION PROPERTIES OF NICHROME

- NICKEL AND CHROMIUM ARE TRANSITION METALS.
- INNER SHELL ELECTRONS CONDUCT, OUTER SHELL SHIELDS. HIGHER RESISTANCE.
- ALLOY EFFECT ENHANCES SHIELDING/RESISTIVITY.

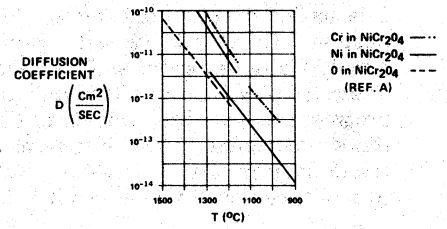


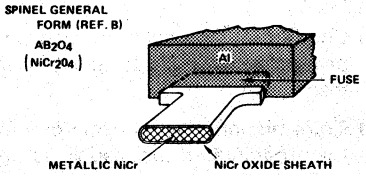
A – Handbook of Chemistry and Physics.
B – Thin Film Technology, R. W. Berry, et. al.
C – Japanese Metal Material Handbook, Y. Yamamoto, et. al.

Figure 1

OXIDATION OF NICHROME

- NiCr FORMS SELF LIMITING SKIN OXIDE
- SPINEL THICKNESS ≈ 20 Å
- PROMOTES RESISTOR STABILITY



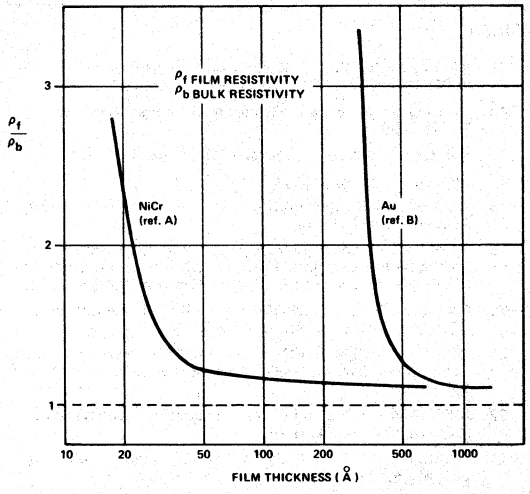


Ref. A – "Mass Transport in Oxides," NBS Publ. 296, (1968).
Ref. B – A. F. Wells, "Structural Inorganic Chemistry", Oxford Press (1950).

Figure 3

FILM VS. BULK PROPERTIES

- SHORT MEAN FREE PATH LENGTH OF ELECTRONS
- BULK RESISTIVITY IN THIN FILM
- GOOD FILM REPRODUCIBILITY



A – M. Nagata, et. al., Proc. Elec. Comp. Conf., 1969.
B – K. L. Chopra, Thin Film Phenomena, McGraw–Hill, 1969.

Figure 2

SCANNING TRANSMISSION ELECTRON MICROSCOPY ANALYSIS OF FUSES

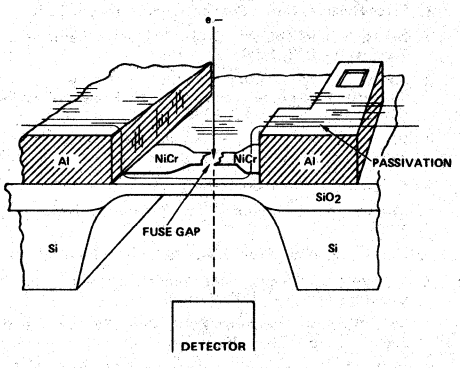
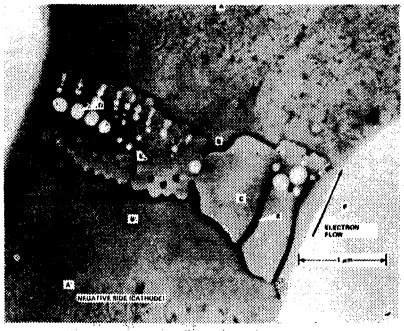


Figure 4

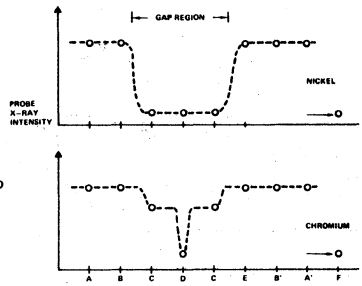
STEM PROGRAMMED FUSE

PROGRAMMING CONDITIONS:
POWER = 150 mW.
TIME TO FUSE = 2 μSEC.



POINT MICROPROBE ANALYSIS

A – NiCr
B – MELTED NiCr
C – SiO_2, CHROMIUM OXIDE
D – SiO_2
E – DENSIFIED NiCr
F – FIELD OXIDE (SiO_2)



NOTE: (A) "FROZEN SPLASH" EFFECT PROGRAMMING HAS MELTED NiCr IN GAP REGION.
(B) MASS TRANSPORT IN GAP.
(C) MASS ASYMMETRY TO NEGATIVE TERMINAL.

Figure 5

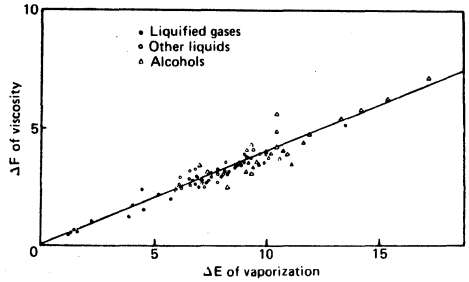


Fig. 11-24. Empirical relation between free energy of activation in liquids, ΔF, and energy of evaporation, ΔE, Rosevaere, Powell and Eyring.

TABLE II

Corrected ratio of energy of vaporization and activation for viscous flow

Metal	Average temp. °C.	ΔE_{vap} kcal.	ΔE_{vis} kcal.	$\frac{\Delta E_{vap}}{\Delta E_{vis}}$	$\frac{\Delta E_{vap}}{\Delta E_{vis}}\left(\frac{r_{ion}}{r_{atom}}\right)^3$
Na	500	23.4	1.45	16.1	2.52
K	480	19.0	1.13	16.7	3.41
Ag	1400	60.7	4.82	12.5	3.79
Zn	850	26.5	3.09	8.6	2.10
Cd	750	22.5	1.65	13.5	3.96
Ga	800	34.1	1.13	30.3	2.53
Pb	700	42.6	2.80	15.9	4.97
Hg	250	13.6	0.65	20.8	2.37
Hg	600	12.3	0.55	22.2	3.54
Sn	600	15.3	1.44	10.6	4.07
Sn	1000	14.5	1.70	8.6	3.30

From "Diffusion in Solids, Liquids, Gases", W. Jost.

Figure 7

TEMPERATURE PROFILE IN FUSE NECK FROM HEAT FLOW MODEL

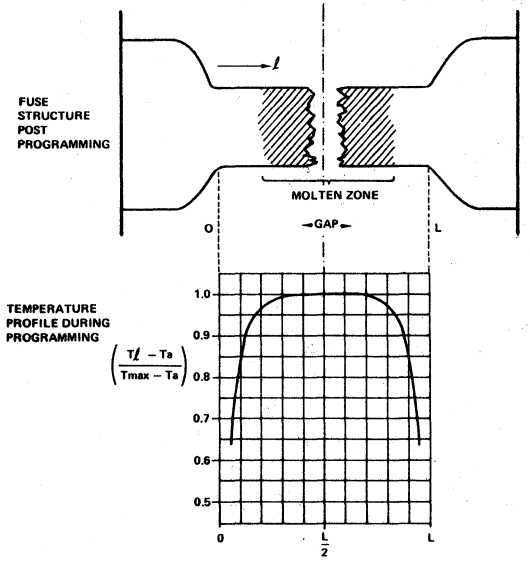
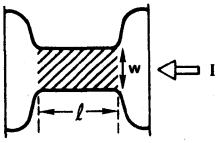


Figure 6

POWER DENSITY IN FUSE NECK REGION



$$\text{POWER DENSITY} = \frac{I^2 (\rho_s \ell / w)}{(\ell \cdot w)}$$

$\rho_s \ell / w$ = RESISTANCE OF THE FUSE NECK (OHMS)

ρ_s = SHEET RESISTIVITY OF NICHROME (OHMS/SQ)

$\ell \cdot w$ = AREA OF FUSE NECK (MIL.^{2})

ℓ = LENGTH OF FUSE NECK

w = WIDTH OF FUSE NECK

I = PROGRAMMING CURRENT ($I = V_F/R_F$)

Figure 8

DYNAMIC HEATING OF NiCr FUSE VS. POWER DENSITY

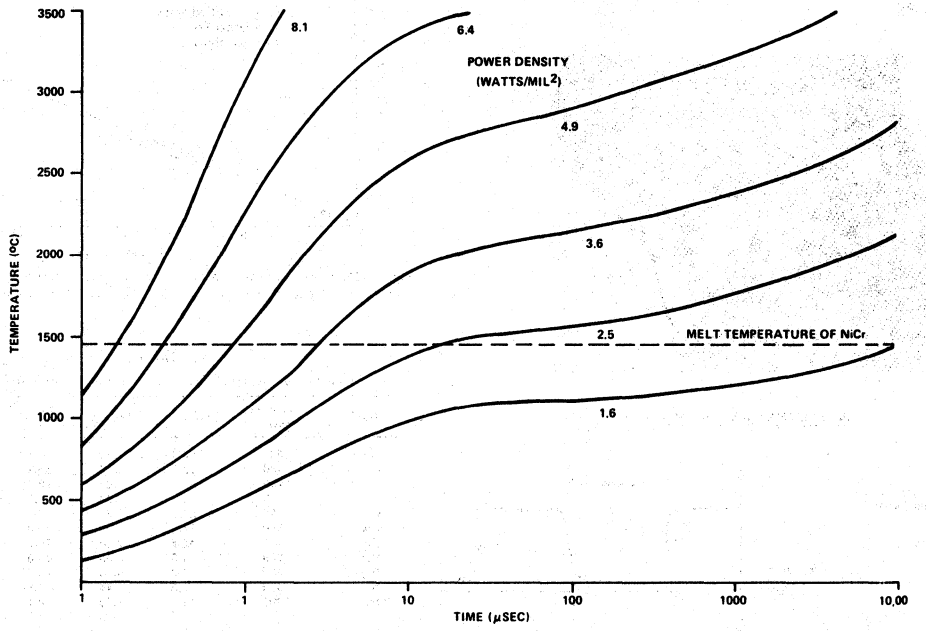


Figure 9

POWER DENSITY VS. TIME TO FUSE

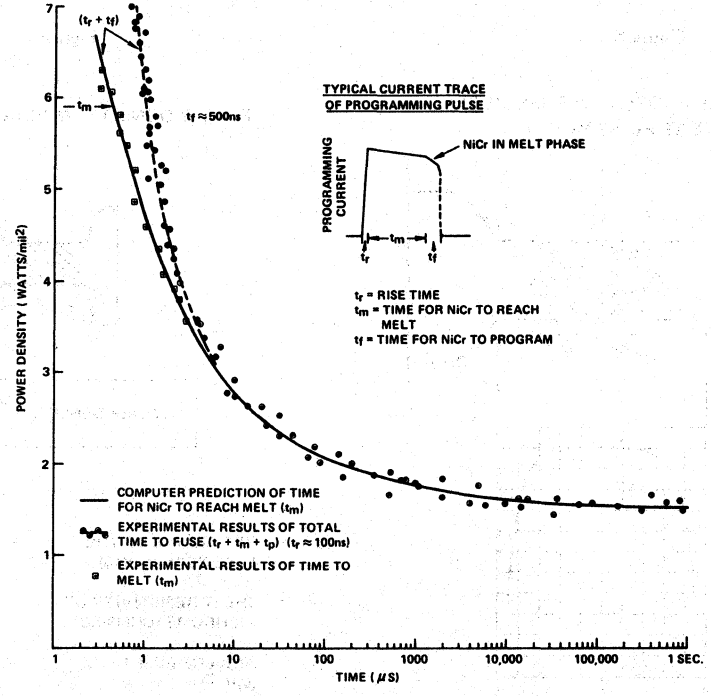
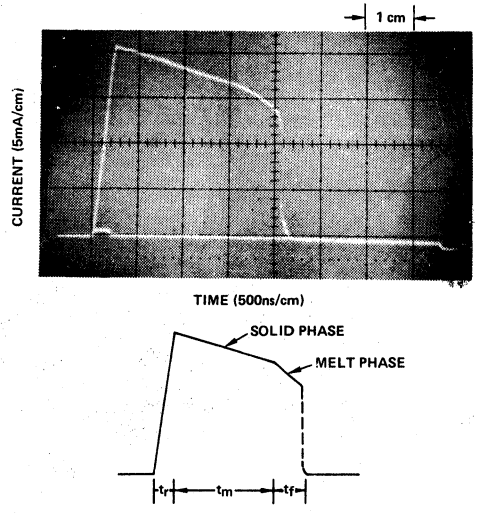


Figure 10

PROGRAMMING PULSE CHARACTERISTICS



t_r = RISE TIME OF PROGRAMMING PULSE

t_m = TIME FOR NiCr TO REACH MELT

t_f = TIME OF THE FUSING EVENT (IONIC MASS TRANSPORT)

Figure 11

MAXIMUM FUSE TEMPERATURE VS. POWER DENSITY

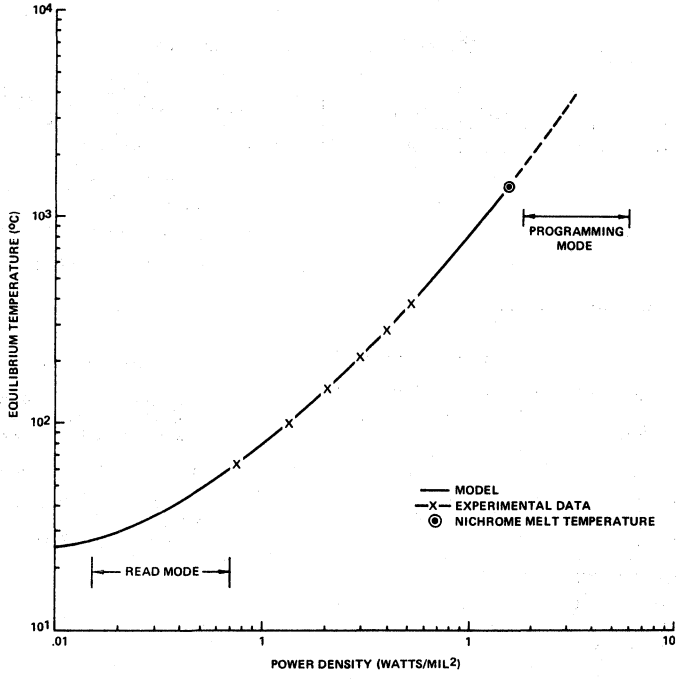
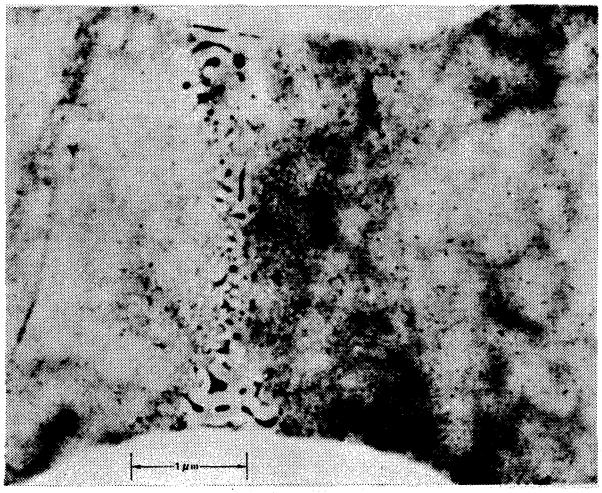


Figure 12

MARGINALLY PROGRAMMED TEST VEHICLE FUSE

PROGRAMMING CONDITIONS:
POWER DENSITY = 1.5 WATTS/MIL^2
TIME TO FUSE = 300 SEC.



FORCED RELINK OF MARGINALLY PROGRAMMED TEST FUSE

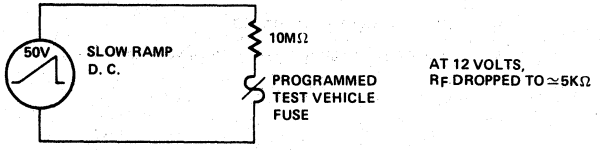
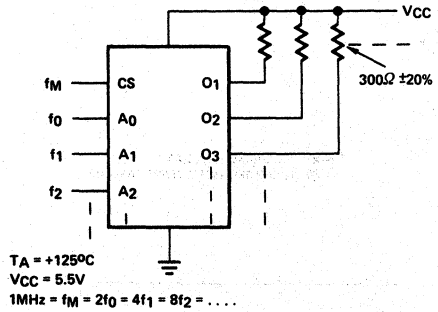


Figure 13

OPERATING LIFE TEST RESULTS

	#DEVICES	#DEVICE-HRS	#FAILURES	ACTUAL FAILURE RATE	FAILURE RATE @ 60% C.L.(1)
ALL PROM TYPES	3840	9.030M	3(3)	0.03%/K HRS(4) (MTTF - 3.3 x 10^6 HRS)	0.046%/K HRS(4) (MTTF - 2.15 x10^6 HRS)
			DERATED TO 25°C	0.004%/K HRS (MTTF - 2.5 x 10^7 HRS)	0.006%/K HRS (MTTF - 1.65 x 10^7 HRS)

BURN–IN SCHEMATIC



(1) C.L. (CONFIDENCE LEVEL)

(2) FUSE MATRIX: 50% PROGRAMMED RANDOM PATTERN AS PER PRESCRIBED PROGRAMMING PROCEDURE.

(3) NON-FUSE RELATED FAILURES

(4) SAME OR BETTER THAN MSI FAILURE RATES (REF. MDFR 1273 – ROME AIR DEVELOPMENT CENTER)

Table III

Microscopic Observations of Fuses

Steve Harris, Memory Applications Manager

Beauty is in the eye of the beholder. When the eye is attached to a microscope, beauty can take strange forms. Nowhere is this more evident than when the realm of blown fuses in PROMs is entered. This paper will "shed some light" on the misinformation which has been generated regarding the nature of nichrome fuse gaps as viewed by different microscopic techniques.

WHAT YOU SEE OPTICALLY

Using a light microscope to examine fuse structures is a futile exercise because the wavelength of visible light is within an order of magnitude of the total fuse dimensions. The microstructure of the fusing process reaction zone contains formations that are smaller than a wavelength of light. In addition, the overlying passivation acts like an aberrant lens and distorts the image which is visible. The most that can be reliably ascertained regarding the nature of a fuse with optical microscopy is whether the fuse is physically present or absent.

Photo 1* illustrates this physical phenomenon. The photograph is of photoresist after exposure to ultraviolet light and normal developing solutions. The ridges in the vertical portion of the photoresist are produced by the standing wave that is present due to reflection of the U.V. light from the oxidized silicon during resist exposure. As can be seen, the ridge pattern has a wavelength λ of the incident light (λ = 3650nm), the index of refraction of the photoresist is n = 1.58; thus, for visible light on the order of λ= 5000nm, less than ten wavelengths are needed to span the fuse neck region.

WHAT THE SCANNING ELECTRON MICROSCOPE SHOWS

The SEM is a useful analytical tool for many applications. This is amply demonstrated by Photo 1 that showed us the standing wave pattern in photoresist.

The SEM does have limitations in observing fuses, however. For one, it cannot "see" through the passivation layer on top of the fuse. This necessitates the removal of the glass and hence, physical and chemical alteration of the fuse gap microstructure. In addition, the results after depassivation are misleading. A SEM of a depassivated typical programmed NiCr fuse is shown in Photo 2. Photo 3 is a typical programmed polysilicon fuse as deployed in the CMOS PROM.

Previous observers have never reached satisfactory explanations for the fusing phenomena based on SEM photographic evidence. The important facts to consider here are that for both fuses, an electrical discontinuity has been achieved through programming. In both cases, the observer is hard pressed to determine how this was achieved, for his eyes tell him that both fuses appear physically connected in various areas. Electrically, we know this is not the case.

This brings us to the crucial observation that the SEM cannot distinguish between electrical conductors and electrical insulators. This is readily confirmed by observing the lack of differentiation afforded in the SEM view of the adjacent aluminum interconnect (an excellent conductor) and the underlying silicon dioxide (an excellent insulator). Since both of the above fuses are electrically discontinuous, some portion of their makeup is insulative, but the Scanning Electron Microscope gives us no clues as to the integrity of the insulator.

*Photos Found on Pages 5-25 Thru 5-27.

TRANSMISSION ELECTRON MICROSCOPY ANALYSIS OF FUSES

A fresh approach in fuse analysis has been developed to view a fuse without disturbing the conditions present at the time of programming. Basically, the technique uses a thinned specimen PROM with the fuses sandwiched between the two normal glass sheets found on the PROM (the passivation above and thermal oxide below) with the underlying silicon substrate etched away as shown in Photo 4 . Now standard high resolution bright and dark field TEM (Transmission Electron Microscopy) analytical techniques are available.

Photo 4 is a TEM photograph of a typical programmed NiCr fuse. Now we can see which regions of the blown fuse are conductive metal and which are not. The well-defined darkened regions are metallic while the overlying gray, which is all that was seen by SEM, has proven by electron diffraction analysis to be a stable insulating oxide compound with crystalline order that resembles a $NiCr_2O_4$ spinel. The surrounding region of high transmission are characteristic of the undisturbed passivation and underlying thermal SiO_2.

Therefore, Transmission Electron Microscopy has the capability of determining the true chemistry of programmed NiCr fuses.

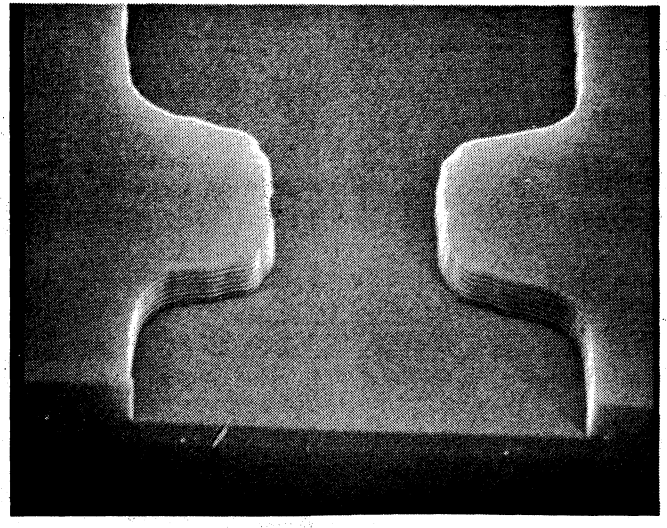


PHOTO 1A

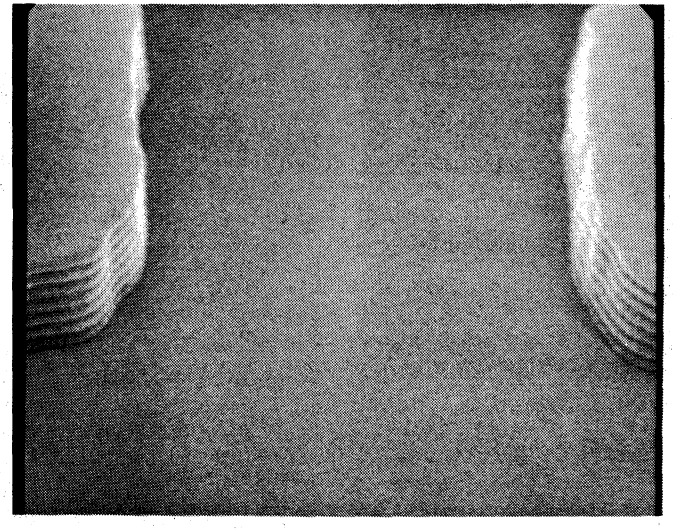


PHOTO 1B

SEM Photographs of Programmed Fuses

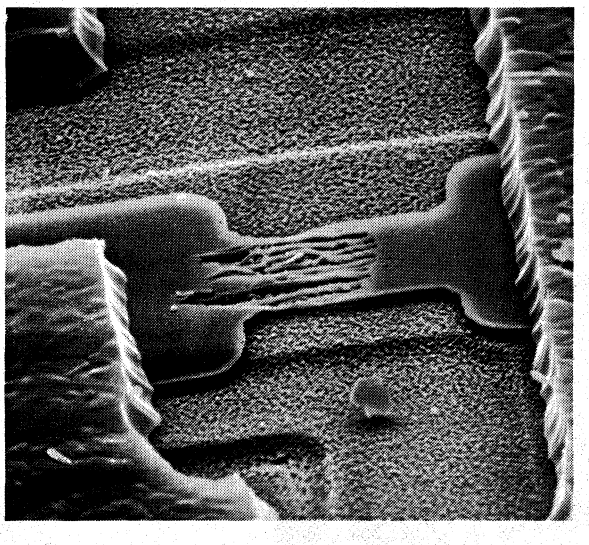


PHOTO 2A

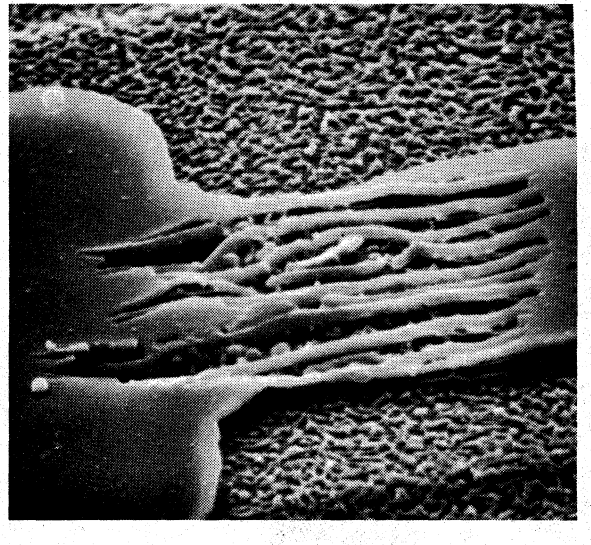


PHOTO 2B

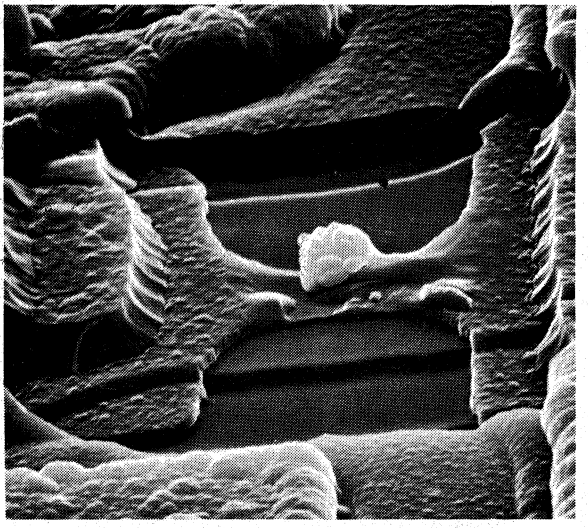


PHOTO 3A

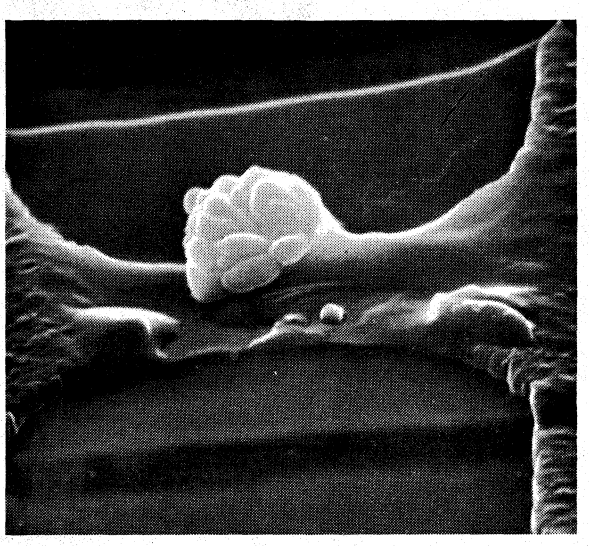


PHOTO 3B

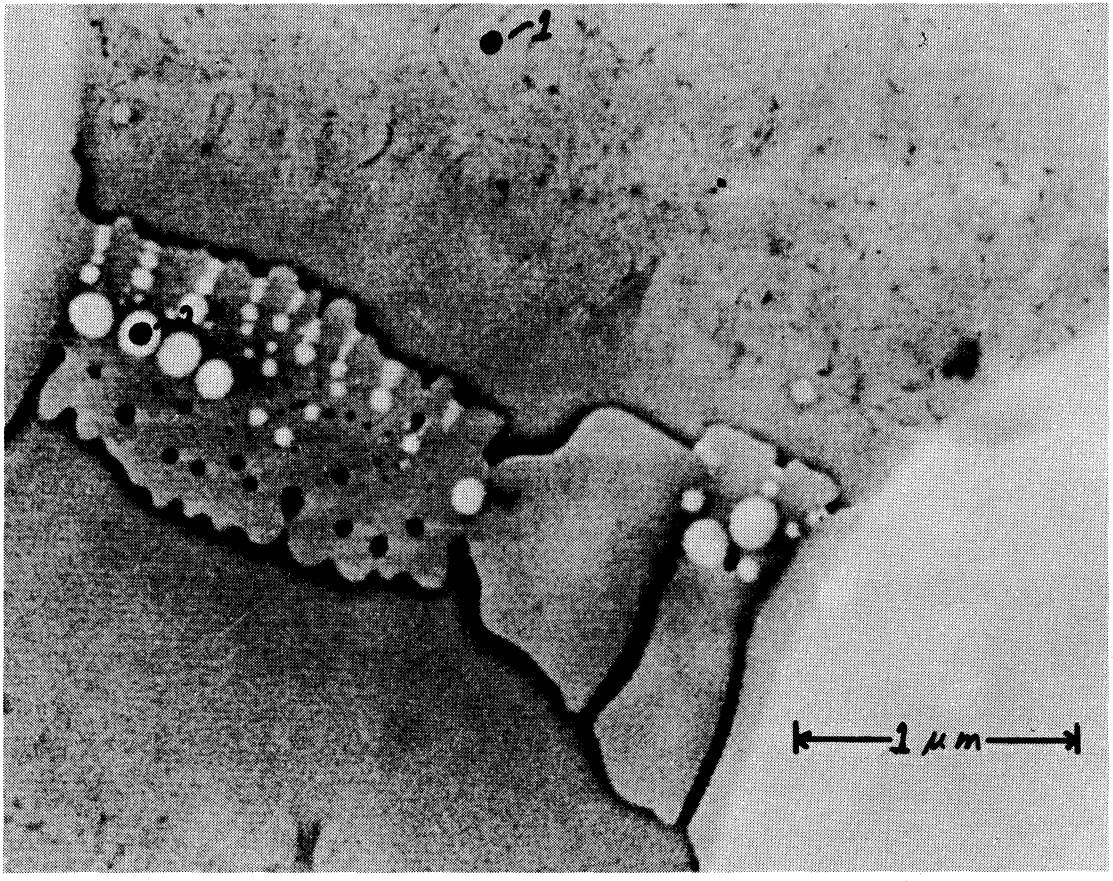


PHOTO 4

Reliability Screening Programs

Facility Qualification

Harris is closely attuned to the requirements of military quality and reliability manufacturing programs. Our facilities and its quality plan is well accepted at all major companies. In addition, we have JAN qualification in the Bipolar Memory area and have JAN qualifications in process on CMOS Memory and Linear products.

MIL-STD-883A Class B (Dash 8)

As a special service to users of high rel products Harris makes instantly available high reliability on many of our product lines. Simply by adding its postscript -8 to appropriate Harris part numbers "off the shelf" delivery can be obtained of products screened to MIL-STD-883 Method 5004 Class B.

Hi-Rel Program

To meet our commitment to CMOS growth, Harris has introduced the Hi-Rel Dash 8 program. This program is designed to meet the needs of the customer seeking enhanced quality and reliability by additional screening steps.

This program is designed for:

- Customers using a current reliability add-on program.
- For the individual seeking a trade-off between additional cost and improved reliability and quality through screening – Harris gives a broad selection from Class B flow to burn-in only.

The Harris Hi-Rel Program is a comprehensive program aimed at serving the various needs of many customers. With the increasing need for improved IC systems mean time to failure performance, the Hi-Rel program assures high quality and reliability of CMOS circuits.

Harris CMOS devices have been produced for over 6 years in modern state of the art manufacturing facilities. Our implemented second and third generation mask designs with the experience of well-controlled processes, results in standard products with built-in reliability. Coupling Harris CMOS with a Hi-Rel program will result in an enhanced combination for quality and reliability.

User Benefits

- Eliminates user screening programs
- Provides uncomplicated incoming inspection
- Reduces infant mortality and board rework
- Reduces field failures and unnecessary maintenance costs

Quality

In theory, parts tested 100 percent should upon receipt at the user's site be 100 percent good. Due to the mass production of CMOS there may exist a small percentage of parts which escape 100 percent tests. The AQL or LTPD outgoing sampling plans at Harris have been very successful in stopping the DOA's (Dead on Arrival). For the user with complex systems using large quantities of products, a quality enhancement can be tailored into your specific Hi-Rel program by choosing tightened sampling plans. The tightened quality test plan ensures close maintenance of the improved quality level through careful product segregation and retesting.

Reliability

Experience and perfected process controls have built reliability into a standard Harris CMOS product. Reliability cannot be tested into a part. Quality level may be improved by retesting and tighter sampling plans. However, reliability is improved by proper design and observance of sound ground rules, controlled processes and finally by stress testing to confirm claimed reliability performance. The Hi-Rel program offers a varied mix of stress tests to compress time and weed out devices subject to infant mortality. The equivalent early life failures are removed by the various screens such as temperature cycling, stabilization bake, burn-in and high temperature functional testing. Some or all of these stress tests will remove early failures and thus improve overall system reliability.

Dash 8 Program – MIL-STD-883; Off-the-Shelf Delivery; MIL-STD-883/MIL-M-38510, MIL-Q-9858A

INTRODUCTION

Statement of Scope

This section establishes the detail requirements for Harris' Circuits screened and tested under the Product Assurance Program.

The Harris DASH 8 Devices pass the screening requirements of the latest issue of MIL-STD-883, Method 5004, Class B, and the requirements as specified in this document. Included in this section are the quality standards and screening methods for commercial parts which must perform reliably in the field.

Applicable Documents

The following Military documents form a part of this section to the extent referenced herein and provide the foundation for Harris Products Assurance Program.

MIL-M-38510	"General Specification for Microcircuits"
MIL-Q-9858A	"Quality Program Requirements"
MIL-STD-883	"Test Methods and Procedures for Microelectronics"
NASA Publication 200-3	"Inspection System Provisions"

Harris maintains a Product Assurance Program (PAP) using MIL-M-38510 as a guide. Harris Product Assurance Program assures compliance with the requirements and quality standards of control drawings and the requirements of this specification.

The DASH 8 Program will also be found useful by those Harris customers who must generate their own procurement specifications. Use of the enclosed Harris Standard Test Tables, Test Parameters, and Burn-In Circuits will aid in reducing specification negotiation time.

NOTE: At the time of this printing, a new industry Standard Method for production of Class B and C microcircuits was being defined by JEDEC. Harris intends to implement this new standard procedure. The procedure embodies all relevant device screening sections of Mil. Spec. 883B and 38510D and is quite similar to our current Dash 8 program. Please consult your Harris representative if you are interested in procuring parts to this standard specification.

PRODUCT ASSURANCE AT HARRIS

Our Product Assurance Department strives to assure that the quality and reliability of products shipped to customers is of a high quality level and consistent with customer requirements. During product processing, there are several independent visual and electrical checks performed by Quality Assurance personnel.

Prior to shipment, a final inspection is performed at Quality Assurance Plant Clearance to insure that all requirements of the purchase order and customer specifications are met. The system and procedures used and implemented are in accordance with MIL-M-38510, MIL-Q-9858A, MIL-STD-883A, MIL-C-45662 and MIL-I-45208.

The Harris Semiconductor Reliability and Quality Manual which is available upon request, describes the total function and policies of the organization to assure product reliability and quality.

HARRIS SEMICONDUCTOR DASH 8 PRODUCT FLOW
MIL-M-38510/MIL-STD-883, METHOD 5004 CLASS B

100% SCREENING PROCEDURE

	SCREEN	MIL-STD-883 METHOD/COND.
1	Internal Visual	2010 Cond. B.
2	Stabilization Bake	1080 Cond. C (24 hrs. minimum)
3	Temperature Cycling	1010 Cond. C
4	Constant Acceleration	2001 Cond. E; Y1 plane
5	Seal: (A) Fine (B) Gross	1014 Cond. A or B 1014 Cond. C2
6	Initial Electrical	Harris Specifications
7	Burn-In Test	1015, 160 hrs. @ 125°C (or equivalent) (Burn-In circuits enclosed)
8	Final Electrical 100% go-no-go	Tested at Worst Case Operating Conditions
9	External Visual	2009 Sample Inspection
10	Lot Acceptance	Table I, Group A Elect. Tests

Note:

Traceability: All devices are assigned date code identification that provides traceability back to the inspection lot.

Branding: All devices are branded with the HX-XXXX-8 and EIA date code.

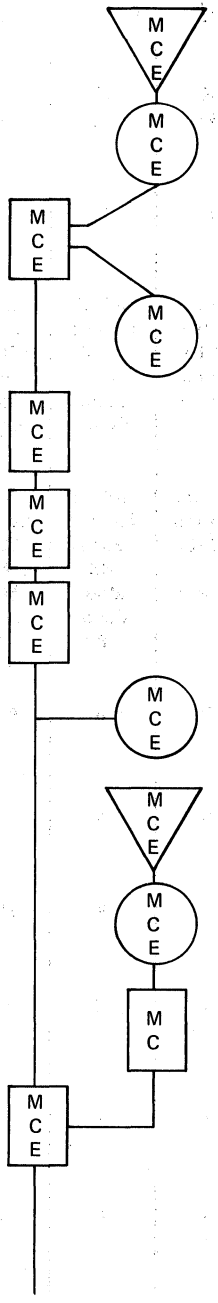
Aged Products: Product that has been held for more than 24 months will be reinspected prior to shipment to group A inspection requirements.

Additional Requirements: Attributes data will be supplied on Group A Lot Acceptance upon request.

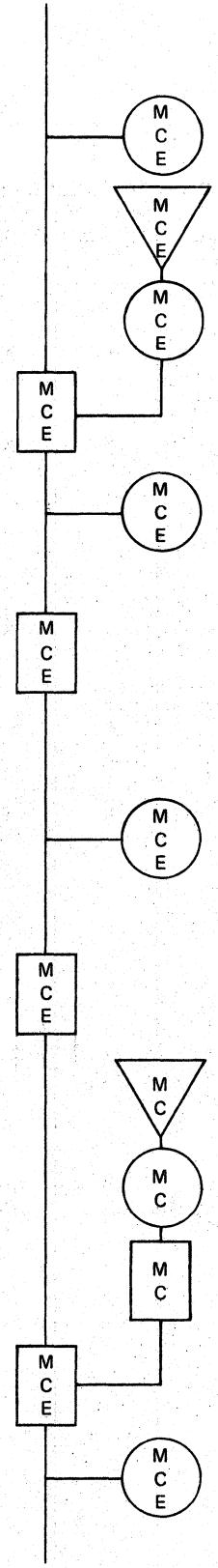
Generic data from Harris' Reliability Add-On Program is available upon request. The objective of Harris Reliability Add-On Program is to provide a continuous life and environmental monitor for all products families in manufacturing. This program provides life test performance results to fullfill reliability data requirements and to verify package integrity. The Reliability Add-On Program is supplemental to customer funded Lot Qualification.

For customers desiring Lot Qualification, Harris Semiconductor will perform Group A, B, C and D inspections to MIL-STD-883, Method 5005 as defined herein for an additional charge.

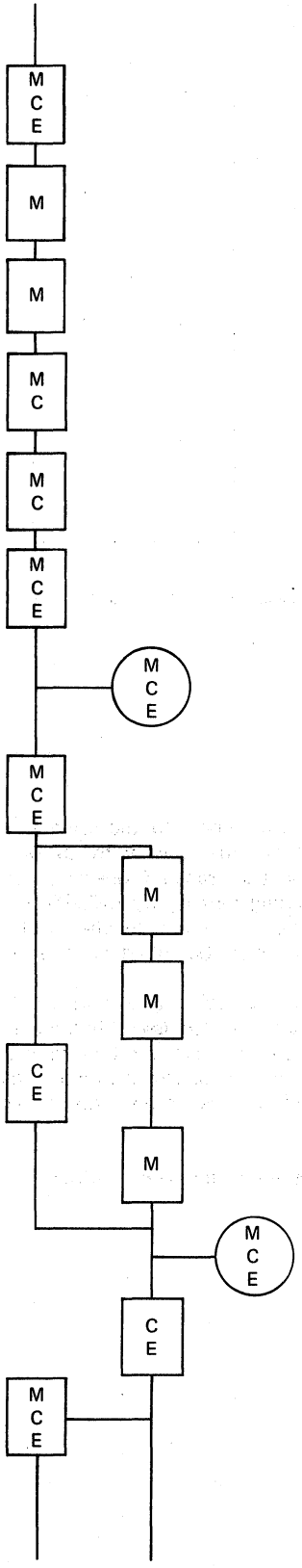
STANDARD PRODUCTS SCREENING AND INSPECTION PROCEDURE



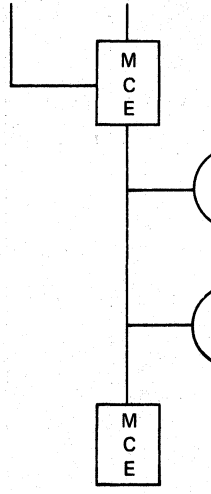
OPER. SEQ.	OPER. DESCRIPTION	PRODUCT CATEGORIES		
		MIL (M)	COMM (C)	EPOXY (E)
	Incoming Material Silicon and Chemical Procurement.	X	X	X
	Q.C. Incoming Inspection. Materials are Inspected for Conformance to Specified Requirements.	X	X	X
	Manufacturing Wafer Fabrication	X	X	X
	QC • DIH_2O & Gas Monitor • SEM Process Control • Wafer Process Control	X	X	X
	Manufacturing, Wafer Electrical Probe (100%)	X	X	X
	Manufacturing, Wafer Scribe, Break (100%)	X	X	X
	Manufacturing Dice Screen (100%)	X	X	X
	QA Dice Inspection Control	X	X	X
	Preform Procurement	X	X	N/A
	Package Procurement	X	X	N/A
	Leadframe Procurement			X
	Epoxy Compound Procurement			X
	Q.C. Preform Inspection	X	X	N/A
	Q.C. Package Inspection	X	X	N/A
	Q.C. Leadframe Inspection			X
	Manufacturing Package Clean	X	X	N/A
	Manufacturing Die Mounting	X	X	X



QA Die Mount Control (continuous sampling) • Visual Die Inspection	X	X	X
Bond Wire Procurement	X	X	X
Q.C. Wire Inspection (receiving)	X	X	X
Manufacturing Wire Bonding	X Al	X Al	X Au
QA Bond Control (continuous sampling) • Visual Die & Bond Inspection • Wire and Pull Test	X	X	X
Manufacturing Pre-Seal Screen (100%)	MS883 Method 2010 Cond. A or B	MS883 Method 2010 HS Mod. Cond. B	MS883 Method 2010 HS Mod. Cond. B
QA Pre-Seal Inspection Lot Acceptance	MS883 Method 2010 Cond. A or B	MS883 Method 2010 HS Mod. Cond. B	MS883 Method 2010 HS Mod. Cond. B
Preseal Bake Per MS-883, Method 1008, Cond. C	8 hr.	4 hr.	4 hr.
Package Lid Procurement	X	X	N/A
Package Lid Inspection	X	X	N/A
Package Lid Clean	X	X	N/A
Package Seal/Encapsulation	X	X	X
QA Package Seal/Encapsulated Control (continuous sampling)	X	X	X



Stabilization Bake MS-883, Method 1008, Cond. C.	24 hr.	8 hr.	8 hr.
Temperature Cycle, MS-883, Method 1010, Cond. C,	X	X	N/A
Centrifuge, MS-883, Method 1010, (Y1) Plane 30 KG's min.	100%	X	N/A
Fine Leak, MS-883, Method 1014	100%	X	N/A
Gross Leak, MS-883, Method 1014 Condition C2	100%	X	N/A
Frame Removal & Loading Units In Carriers/Sticks	X	X	X
Final QA Lot Inspection, MS-883 Method 1014 • Fine & Gross Leak • Visual/Mechanical Inspection	X	X	X
Group A Initial Tests 1.	X	X	X
Brand Device Type/Date Code Serialize, If Applicable	X	N/A	N/A
Burn-In (100%), MS-883, Method 1015	Classes A/B Products	N/A	N/A
Group A Final Test (100%) 1.	X	N/A	N/A
QA Acceptance Elec. Testing • Visual/Mechanical Method 2009 Lot Sampling	X	X	X
Brand Devices Type/Date Code	N/A	X	X
Controlled Inventory	X	X	X



Package for Shipment	X	X	X
Quality Conformance Inspection Group B/C/D Testing, MS-883, Method 5005, Periodically or by Customer P.O. Request	X	X	X
QA Plant Clearance • Final Visual of Marking and Physical Quantity, Conformation of Product by Inspection or Sample Test	X	X	X
Ship to Customer	X	X	X

NOTE: 1. Group A, Subgroup 1, 2, 3, & 9 for Bipolar — Table I, Subgroup 2 & 10 for CMOS.

HARRIS COMMERCIAL GRADE PRODUCTS

This product is processed on the same wafer fabrication lines, to the same thorough specification and rigid controls as HI-Rel parts. At wafer electrical probe the product may be categorized for electrical performance, such as temperature range of operation or maximum output (see specific product data sheet for grading details) by utilizing multiple colored inks. Defective die are inked with red ink, but, for example, die meeting the commercial temperature range electrical specifications may be inked with green ink.

The die are then visually inspected and sorted after die separation to a modified Class B visual criteria. They are then assembled in packages on a controlled assembly line. The ink used to categorize product performance, such as the green ink, might not be removed from the commercial grade die. This ink has been chemically characterized as inert and reliability verification confirms there is no effect on performance or operating life of the parts.

Harris invites any interested customer to review our assembly flow and facilities for information, quality survey, or certification.

TABLE I – GROUP A ELECTRICAL TESTS [1]

SUBGROUP[2]	CLASSES S & B LTPD	CLASS C LTPD
Subgroup 1 Static Tests at 25°C	5	5
Subgroup 2 Static Tests at Maximum Rated Operating Temperature	7	10
Subgroup 3 Static Tests at Minimum Rated Operating Temperature	7	10
Subgroup 7 Functional Tests at 25°C	5	5
Subgroup 8 Functional Tests at Maximum and Minimum Rated Operating Temperatures	10	15
Subgroup 9 Switching Tests at 25°C	7	10
Subgroup 10 Switching Tests at Maximum Rated Operating Temperature	10	15
Subgroup 11 Switching Tests at Minimum Rated Operating Temperature	10	15

1. The specific parameters to be included for tests in each subgroup shall be as specified in the applicable procurement document. Where no parameters have been identified in a particular subgroup or test within a subgroup, no group A testing is required for that subgroup or test to satisfy group A requirements.

2. A single sample may be used for all subgroup testing. Where the required size exceeds the lot size, 100% inspection shall be allowed (see 30.2.5 of Appendix B of MIL-M-38510).

TABLE II – GROUP B TESTS (LOT RELATED) [1]

TEST	MIL-STD-883 METHOD	MIL-STD-883 CONDITION	LTPD*
Subgroup 1			
Physical Dimensions	2016		2 Devices (No Failures)
Subgroup 2			
a. Resistance to Solvents	2015		3 Devices (No Failures)
b. Internal Visual and Mechanical	2014	Failure Criteria from Design and Construction Requirements of Applicable Procurement Document.	1 Device (No Failures)
c. Bond Strength [2].			
(1) Thermocompression	2011	(1) Test Condition C or D	15
(2) Ultrasonic or Wedge		(2) Test Condition C or D	
(3) Beam Lead		(3) Test Condition H	
Subgroup 3			
Solderability [3].	2003	Soldering Temperature of 260 ±10°C	15

NOTES:

1. Electrical reject devices from the same inspection lot may be used for all subgroups when end point measurements are not required.
2. Test samples for bond strength may, at the manufacturer's option unless otherwise specified be randomly selected immediately following internal visual (precap) inspection specified in method 5004, prior to sealing.
3. All devices submitted for solderability test must have been through the temperature/time exposure specified for burn-in. The LTPD for solderability test applies to the number of leads inspected except in no case shall less than 3 devices be used to provide the number of leads required.
4. Generic data from Harris Reliability Add-On Program in the form of Reliability Bulletins are available upon request.

* Reference Note – Table 1*

TABLE III – GROUP C (DIE-RELATED TESTS)

TEST	MIL-STD-883 METHOD	MIL-STD-883 CONDITION	LTPD*
Subgroup 1			
Operating Life Test	1005	Test Condition to be specified (1000 Hrs)	5
End Point Electrical Parameters		Table I – Subgroup 1	
Subgroup 2			
Temperature Cycling	1010	Test Condition C	15
Constant Acceleration	2001	Test Condition E Y_1 Axis	
Seal (a) Fine (b) Gross 2.	1014	As Applicable	
Visual Examination	1.		
End Point Electrical Parameters		Table I – Subgroup 1	

NOTES:

1. Visual examination shall be in accordance with method 1010.
2. When fluorocarbon gross leak testing is utilized, test condition C_2 shall apply as minimum.
3. Generic data from Harris Reliability Add-On Program in the form of Reliability Bulletins are available upon request.

* Reference Note – Table 1 *

TABLE IV – GROUP D (PACKAGE RELATED TESTS)

TEST	MIL-STD-883 METHOD	MIL-STD-883 CONDITION	LTPD*
Subgroup 1			
Physical Dimensions	2016		15
Subgroup 2 [4.]			
Lead Integrity	2004	Test Condition B2 (Lead Fatigue)	15
Seal	1014	As Applicable	
(a) Fine			
(b) Gross [6.]			
Subgroup 3 [1.]			
Thermal Shock	1011	Test Condition B as a Minimum, 15 Cycles Minimum.	15
Temperature Cycling	1010	Test Condition C, 10 Cycles Minimum	
Moisture Resistance	1004	Omit Initial/Conditioning and Vibration	
Seal	1014	As Applicable	
(a) Fine			
(b) Gross [6.]			
Visual Examination	2.		
End Point Electrical Parameters		Table I – Subgroup 1	
Subgroup 4 [1.]			
Mechanical Shock	2002	Test Condition B	15
Vibration Variable Frequency	2007	Test Condition A	
Constant Acceleration	2001	Test Condition E (See 3)	
Seal	1014	As Applicable	
(a) Fine			
(b) Gross [6.]			
Visual Examination	3.		
End Point Electrical Parameters		Table I – Subgroup 1	
Subgroup 5 [4.]			
Salt Atmosphere	1009	Test Condition A	15
Visual Examination	5.		

NOTES:

1. Devices used in subgroup 3, "Thermal and Moisture Resistance" may be used in subgroup 4, "Mechanical".
2. Visual examination shall be in accordance with method 1010 or 1011 at a magnification of 5X to 10X.
3. Visual examination shall be performed in accordance with method 2007 for evidence of defects or damage to case, leads, or seals resulting from testing (not fixturing). Such damages shall constitute a failure.
4. Electrical reject devices from that same inspection lot may be used for samples.
5. Visual examination shall be in accordance with paragraph 3.3.1 for method 1009.
6. When fluorocarbon gross leak testing is utilized, test condition C_2 shall apply as minimum.
7. Generic data from Harris Reliability Add-On Program in the form of Reliability Bulletins are available upon request.

* Reference Note – Table 1 *

Section 4. Burn-In Circuits

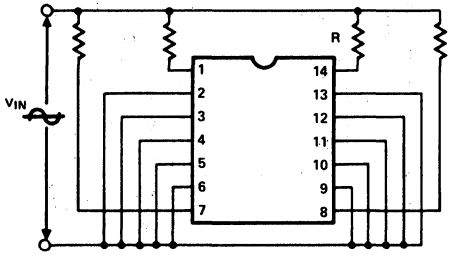
Burn-In Circuit Index

		Drawing No.
HM-0104	10 x 4 Diode Matrix	1
HM-0168	6 x 8 Diode Matrix	2
HM-0186	8 x 6 Diode Matrix	3
HM-0198	9 x 8 Diode Matrix	4
HM-0410	4 x 10 Diode Matrix	5
HM-6312	1024 x 12 CMOS ROM	6
HM-6388	8192 x 8 CMOS ROM	Preview
HM-6389	8192 x 8 CMOS ROM	Preview
HD-6431	Hex Latched Bus Driver	7
HD-6432	Hex Bi-Directional Bus Driver	8
HD-6433	Quad Bus Transceiver	9
HD-6440	1 of 8 Decoder-Driver	10
HD-6495	Hex Bus Driver	24
HD-6600	Quad Power Strobe	11
HM-6501	256 x 4 CMOS RAM	12
HM-6503	2048 x 1 CMOS RAM	13
HM-6504	4096 x 1 CMOS RAM	13
HM-6508	1024 x 1 CMOS RAM	14
HM-6511	64 x 12 CMOS RAM	15
HM-6512	64 x 12 CMOS RAM	16
HM-6513	512 x 4 CMOS RAM	17
HM-6514	1024 x 4 CMOS RAM	17
HM-6518	1024 x 1 CMOS RAM	18
HM-6533	1024 x 4 CMOS RAM	19
HM-6543	4096 x 1 CMOS RAM	20
HM-6551	256 x 4 CMOS RAM	12
HM-6561	256 x 4 CMOS RAM	21
HM-6562	256 x 4 CMOS RAM	22
HM-6611	256 x 4 CMOS PROM	23
HM-6661	256 x 4 CMOS PROM	Preview
HM-7602	32 x 8 Bipolar PROM — Open Collector	25
HM-7603	32 x 8 Bipolar PROM — Three State	25
HM-76LS03	32 x 8 Bipolar PROM — Three State	Preview
HM-7608	1024 x 8 Bipolar PROM — Three State	Preliminary
HM-7610	256 x 4 Bipolar PROM — Open Collector	26
HM-7610A	256 x 4 Bipolar PROM — Open Collector	26
HM-7611	256 x 4 Bipolar PROM — Three State	26
HM-7611A	256 x 4 Bipolar PROM — Three State	26
HM-7616	2048 x 8 Bipolar PROM — Three State	Preview
HM-76160	2048 x 8 Bipolar PROM — Open Collector	Preview
HM-76161	2048 x 8 Bipolar PROM — Three State	Preview
HM-7620	512 x 4 Bipolar PROM — Open Collector	26
HM-7620A	512 x 4 Bipolar PROM — Open Collector	26
HM-7621	512 x 4 Bipolar PROM — Three State	26
HM-7621A	512 x 4 Bipolar PROM — Three State	26
HM-7625R	256 x 8 Bipolar PROM — Three State	31
HM-7629	256 x 8 Bipolar PROM — Three State	32
HM-7640	512 x 8 Bipolar PROM — Open Collector	27
HM-7640A	512 x 8 Bipolar PROM — Open Collector	27
HM-7640AR	512 x 8 Bipolar PROM — Open Collector	Preview

HM-7641	512 x 8 Bipolar PROM — Three State	27
HM-7641A	512 x 8 Bipolar PROM — Three State	27
HM-7641AR	512 x 8 Bipolar PROM — Three State	Preview
HM-7642	1024 x 4 Bipolar PROM — Open Collector	28
HM-7642A	1024 x 4 Bipolar PROM — Open Collector	28
HM-7642P	1024 x 4 Bipolar PROM — Open Collector	Preliminary
HM-7643	1024 x 4 Bipolar PROM — Three State	28
HM-7643A	1024 x 4 Bipolar PROM — Three State	28
HM-7643P	1024 x 4 Bipolar PROM — Three State	Preliminary
HM-7644	1024 x 4 Bipolar PROM	26
HM-7644A	1024 x 4 Bipolar PROM	26
HM-7645	1024 x 4 Bipolar PROM — Three State	Preview
HM-7645P	1024 x 4 Bipolar PROM — Three State	Preview
HM-7647R	512 x 8 Bipolar PROM — Three State	29
HM-7648	512 x 8 Bipolar PROM — Open Collector	30
HM-7649	512 x 8 Bipolar PROM — Three State	30
HM-7680	1024 x 8 Bipolar PROM — Open Collector	Preliminary
HM-7680R	1024 x 8 Bipolar PROM — Open Collector	Preliminary
HM-7680P	1024 x 8 Bipolar PROM — Open Collector	Preliminary
HM-7680RP	1024 x 8 Bipolar PROM — Open Collector	Preliminary
HM-7681	1024 x 8 Bipolar PROM — Three State	Preliminary
HM-7681R	1024 x 8 Bipolar PROM — Three State	Preliminary
HM-7681P	1024 x 8 Bipolar PROM — Three State	Preliminary
HM-7681RP	1024 x 8 Bipolar PROM — Three State	Preliminary
HM-7683	1024 x 8 Bipolar PROM	Preliminary
HM-7684	2048 x 8 Bipolar PROM — Open Collector	Preliminary
HM-7684P	2048 x 8 Bipolar PROM — Open Collector	Preliminary
HM-7685	2048 x 4 Bipolar PROM — Three State	Preliminary
HM-7685P	2048 x 4 Bipolar PROM — Three State	Preliminary
HM-7686	2048 x 4 Bipolar PROM — Open Collector	Preliminary
HM-7686R	2048 x 4 Bipolar PROM — Open Collector	Preliminary
HM-7686P	2048 x 4 Bipolar PROM — Open Collector	Preliminary
HM-7686RP	2048 x 4 Bipolar PROM — Open Collector	Preliminary
HM-7687	2048 x 4 Bipolar PROM — Three State	Preliminary
HM-7687R	2048 x 4 Bipolar PROM — Three State	Preliminary
HM-7687P	2048 x 4 Bipolar PROM — Three State	Preliminary
HM-7687RP	2048 x 4 Bipolar PROM — Three State	Preliminary
JAN-0512	JAN Qualified PROM	33

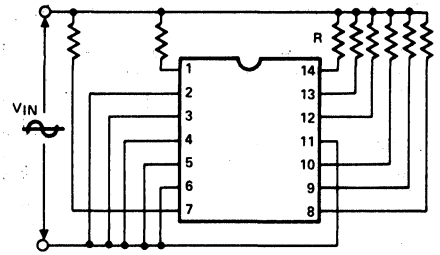
Burn-In Circuits

1 **HM-0104**



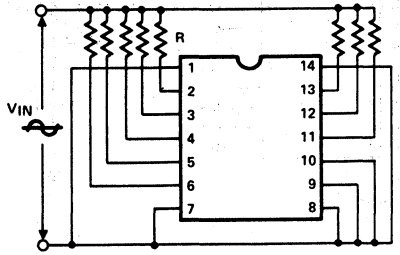
NOTES:
R = 500
±10%, ½W
V_{IN} = 6.3V RMS 60 CYCLE

2 **HM-0168**



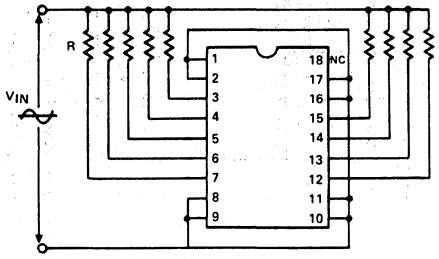
NOTES:
R = 500
±10%, ½W
V_{IN} = 6.3V RMS 60 CYCLE

3 **HM-0186**



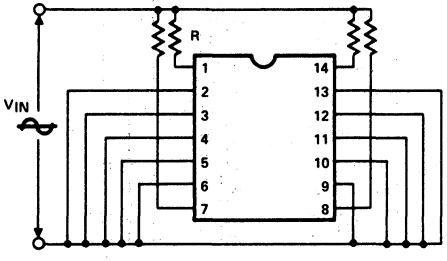
NOTES:
R = 500
±10%, ½W
V_{IN} = 6.3V RMS 60 CYCLE

4 **HM-0198**



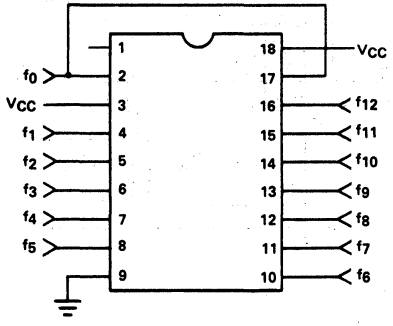
NOTES:
R = 500
± 10%, ½W
V_{IN} = 6.3V RMS 60 CYCLE

5 **HM-0410**

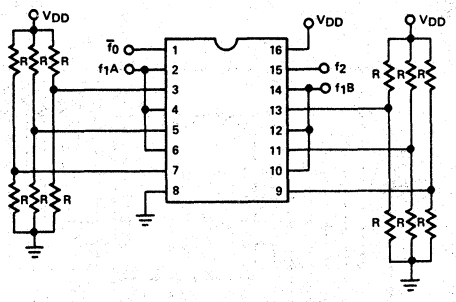


NOTES:
R = 500
±10%, ½W
V_{IN} = 6.3V RMS 60 CYCLE

6 **HM-6312**

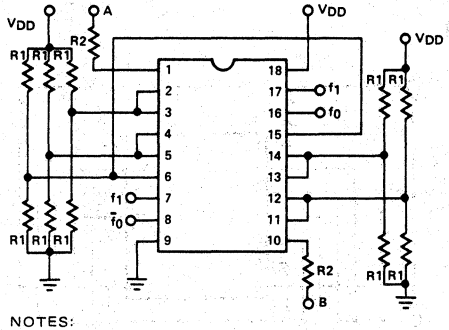


7 HD-6431



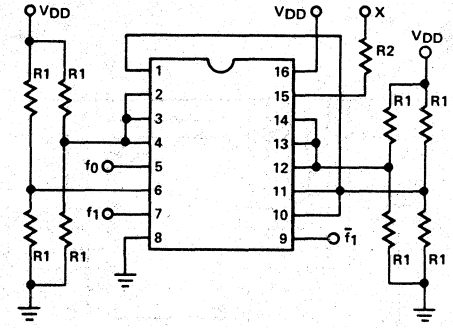
NOTES:
R = 820Ω

8 HD-6432



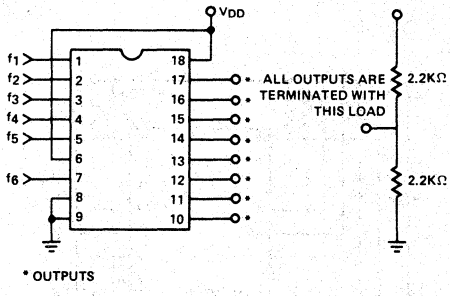
NOTES:
R1 = 820Ω, ¼W, ± 10%
R2 = 910Ω, ¼W, ± 10%

9 HD-6433



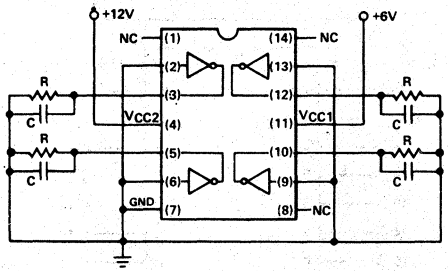
NOTES:
R1 = 820Ω, ¼W, ± 10%
R2 = 910Ω, ¼W, ± 10%

10 HD-6440



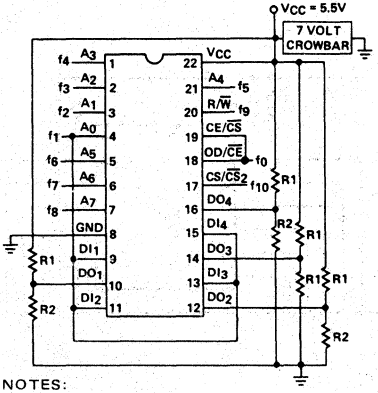
* OUTPUTS

11 HD-6600



NOTES:
R = 39Ω 1W
C = .1mfd 20wvdc

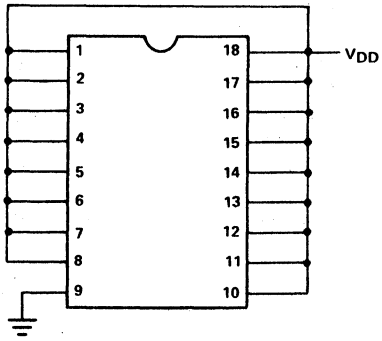
12 HM-6501, 6551



NOTES:
All R1 = 2k ¼W
All R2 = 1k ¼W

13

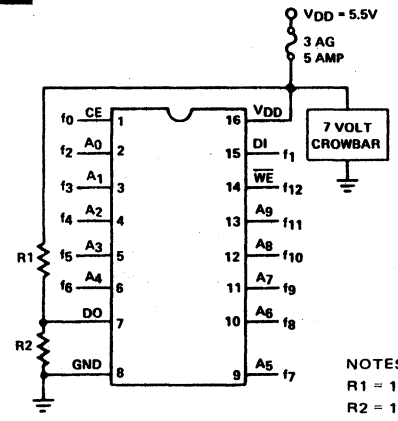
HM-6503, 6504



NOTES:
V_{DD} = 5.5V
Static burn in circuit

14

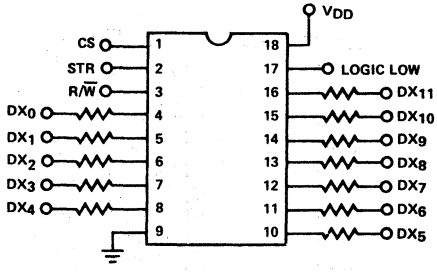
HM-6508



NOTES:
R1 = 1.5kΩ ¼W
R2 = 1kΩ ¼W

15

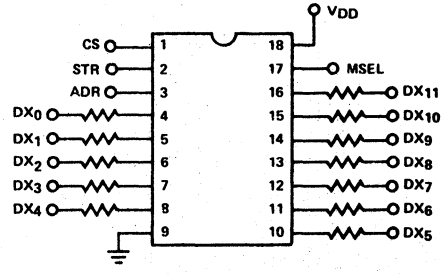
HM-6511



NOTES:
All resistors are 47kΩ,
¼W, ± 10%

16

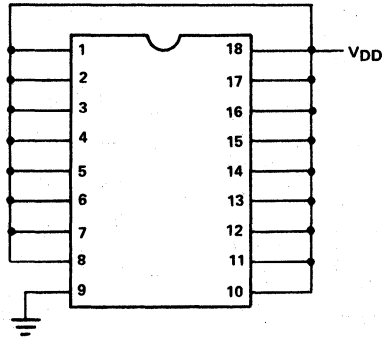
HM-6512



NOTES:
All resistors are 47kΩ,
¼W, ± 10%

17

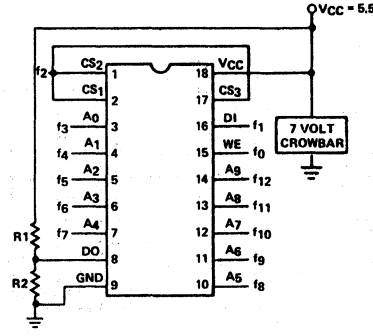
HM-6513, 6514



NOTES:
V_{DD} = 5.5V
Static burn in circuit

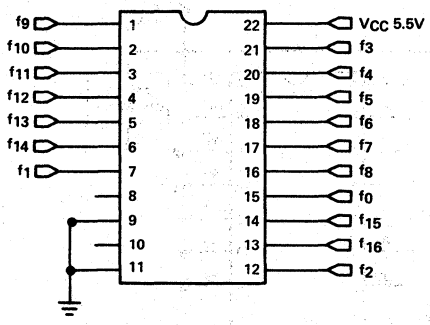
18

HM-6518

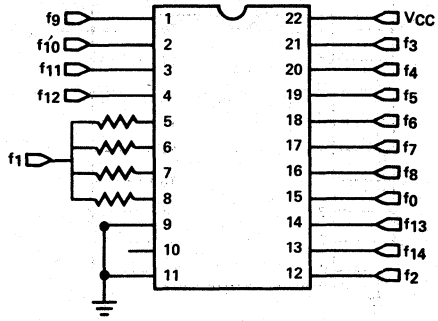


NOTES:
R1 = 1.5kΩ ¼W
R2 = 1.0kΩ ¼W

19 HM-6533

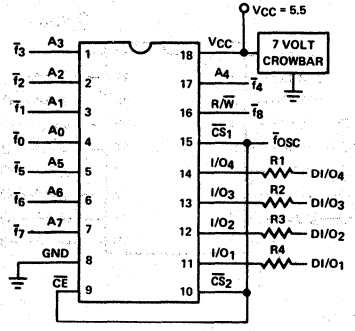


20 HM-6543



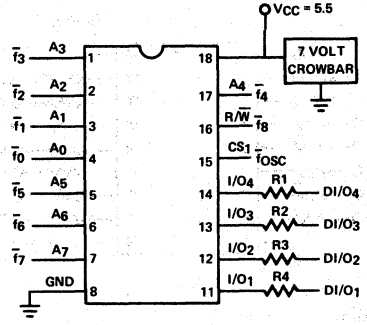
NOTES:
R = 10K, ¼W

21 HM-6561



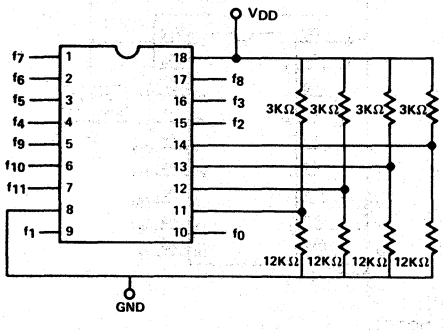
NOTES:
R1, 2, 3, 4 = 10kΩ ¼W

22 HM-6562

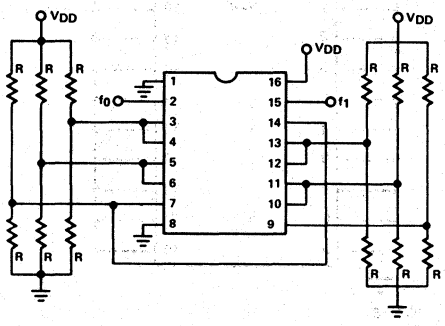


NOTES:
R1, 2, 3, 4 = 10kΩ ¼W

23 HM-6611



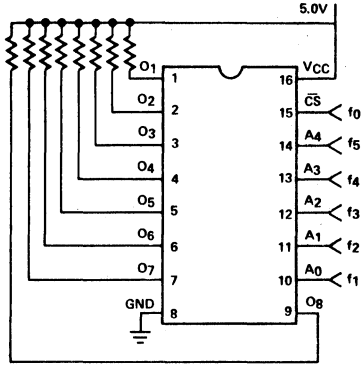
24 HD-6495



NOTES:
R = 820Ω, ¼W, ± 10%

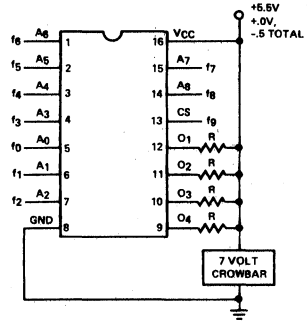
25

HD-7602/03, 76LS03



26

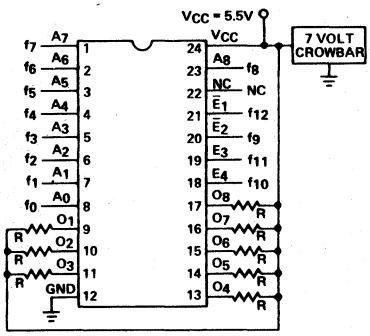
HM-1024, 7610/11, 7620/21, 7644
HM-7610A/11A, 7620A/21A, 7644A



NOTES:
T_A = +127°C $^{+3°C}_{-2°C}$
R = 300Ω ¼W 5%
f_0 = 50% duty cycle to 50kHz ± 20%

27

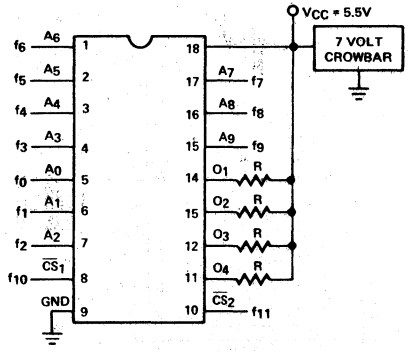
HM-7640/41



NOTES:
R = 300Ω ¼W

28

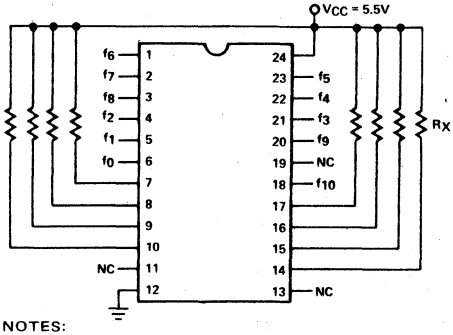
HM-7642/43



NOTES:
R = 300Ω ¼W

29

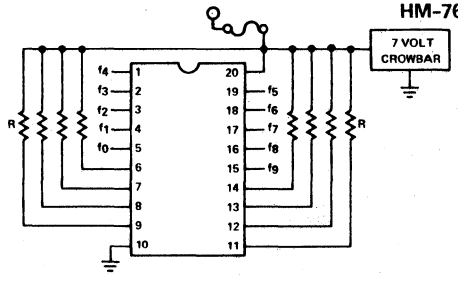
HM-7647R



NOTES:
R_X = 300Ω
0.1W or greater
± 10% or better

30

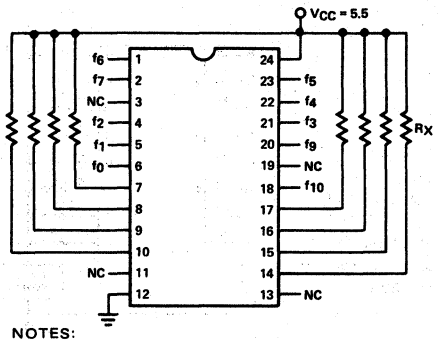
HM-7683
HM-7648
HM-7649



NOTES:
R = 300Ω ± 10%
≥0.25W

31

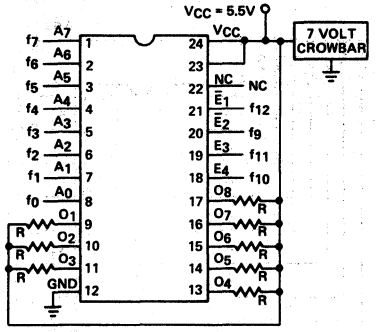
HM-7647R



NOTES:
$R_X = 300\Omega$
0.1W or greater
± 10% or better

32

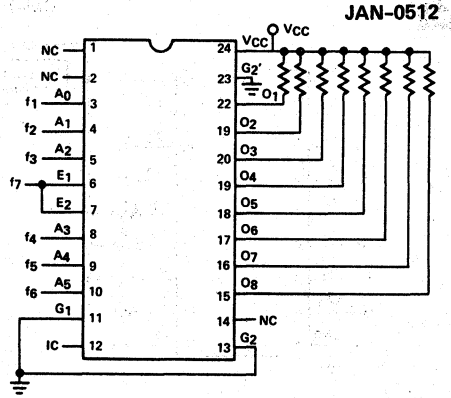
HM-7629



NOTES:
R = 300Ω, ¼W

33

JAN-0512



NOTES:
R = 300Ω, ¼W

Ordering & Packaging

6

Ordering Information

PRODUCT CODE EXAMPLE

H M 1 - 6508 B - 2

PREFIX:
H - Harris

FAMILY:
A - Analog
C - Communications
D - Digital
I - Interface
M - Memory

PACKAGE:
0 - Chip Form
1 - Ceramic DIP
3 - Epoxy DIP
4 - Leadless Carrier
9 - Flatpack

PART NUMBER:
76XX - PROMs
65XX - RAMs
66XX - CMOS PROMs
64XX - Bus Drivers
63XX - CMOS ROMs
0XXX - Diode Matrices

VERSION: *

CMOS
A - 10 Volt version
B - High speed - Low power
D - Commercial grade
Blank - Standard product

BIPOLAR
A - Redesign - Two level metal
P - Power Down version
R - Latched outputs
RP - Latched outputs with Power Down option
Blank - Standard parts

TEMPERATURE RANGE:
2 - -55°C to +125°C
5 - 0°C to 75°C
6 - 100% 25°C probe (Dice only)
8 - Dash 8 program MIL-STD-883-B
** 9 - -40°C to +85°C

** Not applicable to 76XX devices.

* All versions may not be applicable to every product. Check data sheet.

HARRIS DASH 8 PROGRAM

As a service to users of High Rel products, Harris makes readily available via the high reliability DASH 8 program many products from our product lines. Parts screened to MIL-STD-883 Method 5004 Class B are simply branded with the postscript "-8" to the appropriate Harris part numbers, in effect, offering "off the self" delivery. For details concerning this special Harris program for High Rel users, see the Dash 8 section of this Data Book.

NOTE: At the time of this printing, a new industry Standard Method for production of Class B and C microcircuits was being defined by JEDEC. Harris intends to implement this new standard procedure. The procedure embodies all relevant device screening sections of Mil. Spec. 883B and 38510D, and is quite similar to our current Dash 8 program. Please consult your Harris representative if you are interested in procuring parts to this standard specification.

SPECIAL ORDERS

For best availability and price, it is urged that standard "Product Code" devices be specified, which are available worldwide from authorized distributors. Where enhanced reliability is needed, note standard "Dash 8" screening described in this Data Book. Harris application engineers may be consulted for advice about suitability of a part for a given application.

If additional electrical parameter guarantees or reliability screening are absolutely required, a Request for Quotation and Source Control Drawing should be submitted through the local Harris Sales Office or Sales Representative. Many electrical parameters cannot be economically tested, but can be assured through design analysis, characterization, or correlation with other parameters which have been tested to specification limits. These parameters are labeled "sampled and guaranteed but not 100% tested".

Harris reserves the right to decline to quote, or to request modification to special screening requirements.

A Reliable Dry Ceramic Dual In-Line Package (CERDIP)*

R. K. Lowry, C. J. Van Leeuwen, B. L. Kennimer, L. A. Miller

ABSTRACT

The ceramic DIP package utilizing low temperature ($\sim 500^{o}C$) sealing glasses has been simultaneously widely deployed for packaging IC's and condemned for many high reliability applications because of high moisture content in the sealed cavity.

This paper describes the construction, characteristics, and reliability performance of a volume producible, cost-effective Cerdip which has a sealed moisture content typically less than 50ppmv.

INTRODUCTION

The sealed die cavities of some Cerdip parts have been found to contain relatively high levels of moisture. In some instances this has led to device failure caused by electrogalvanic corrosion of circuit metallization.

A principal contributor to cavity water vapor is the solder glass used to form the package seal. Developments in the fields of mass spectroscopy and in-situ moisture sensors have provided means for measuring package moisture levels. In this paper, these methods are applied with other analytical investigations to identify moisture outgassing mechanisms for the two major types of solder sealing glasses. Data is presented showing that packages sealed with devitrifying glass may contain water vapor in excess of 5000ppmv, while otherwise-identical packages sealed with a vitreous glass may approach the dryness conditions generally found in metal or braze-seal packages. Properties and supporting reliability information are presented for vitreous solder glass which will yield a Cerdip package meeting the moisture limitation of MIL-STD-883B Method 1018.

CERDIP PACKAGING

Among assets of the Cerdip are its sturdy construction and good resistance to thermal and mechanical shock. It is not likely to contain conductive particles inside the die cavity. Chips packaged in the Cerdip benefit from an additional high temperature bake of 450-520°C for the 5-10 minute sealing temperature residence time. This is equivalent to 2×10^4 hour stabilization bake at 150°C (1eV activation energy). The Cerdip package can be economically produced in high volume quantities.

Cerdips, of course, cannot be used where the device to be packaged cannot withstand the sealing temperatures used.

A drawback of Cerdip packaging has been device failure rates attributed to electrogalvanic corrosion of metallization on the chip. A necessary condition for such corrosion is the presence of water vapor within the die cavity. If cracks or pinholes exist in the protective glassivation covering the die, this water vapor may migrate to the chip surface. If the dew-point temperature of the cavity ambient is reached, condensation will occur, producing liquid or frozen water which may contact metallized portions of the die surface. The result is a conductive pathway for ion transport. With the device under bias, stray currents across such pathways may corrode metal components resulting in device failure. Corrosion failure modes have been widely studied. [1-5] Discussion continues regarding the threshold quantities of water which must be present for corrosion to occur. [6-8]

CHARACTERIZING SOLDER GLASSES USED IN CERDIP PACKAGING

Viscosity

The two general types of solder glasses used throughout the industry for IC packaging are the vitreous and the devitrifying types. [9-11] Devitrifying glasses are essentially thermosetting materials. They contain nucleating agents which induce formation of a crystalline

* Presented at IEEE International Reliability Physics Symposium, April 1978 at San Diego, Ca.

phase as the glass is heated. The properties of the crystalline phase are uniquely a function of heating times and temperatures. As devitrifying glass is heated, its viscosity drops and it melts in the region of 350-650°C. During this low viscosity period, crystal growth begins at a finite number of nucleation sites. Then, at higher temperatures, usually between 400-750°C, the viscosity rises, further crystal growth ceases, and the glass "sets". The result is a rigid glass material with different properties and a different melting point than the starting material.

Vitreous glass, on the other hand, simply softens and flows when heated above its melting point. The glass becomes rigid and the viscosity rises only when it is cooled below its melting point. Vitreous glass melts and flows at the same temperature each time it is processed. Figure 1* summarizes the flow properties of the two glass types.

Thermal Analysis

The glasses in this study were characterized by differential thermal analysis using commonly applied methods. [12-14] Figure 2 shows typical DTA curves for the two glass types. Point M is the endotherm indicating where the glasses begin to melt. Point S is where the glasses soften under their own weight and flow more readily. For devitrifying glass the S-D region is the minimum in the viscosity curve. D is the main crystallization exotherm. D' is the onset of nucleation at the sites provided by the ZnO component. At D'' crystallization is complete and the glass has again become rigid with a well-ordered characteristic crystal lattice. In the vitreous glass, point S' is the major softening endotherm. At this point maximum interflow of glass from the alumina parts occur. As cooling proceeds to below point M the glass again becomes rigid.

Chemical Analysis

The major components of both vitreous and devitrifying glasses are oxides of lead and boron. All low-temperature solder glasses are necessarily formulated with 70-90% PbO so that their thermal expansion coefficients will approximate that of the alumina piece parts ($3\text{-}7 \times 10^{-6}/^{o}C$). B_2O_3 is present in both glass types as a flux, or glass-former.

Differences in metal oxide composition affect the properties and performance of these glasses. Therefore, the glasses studied here were characterized by DC arc optical emission spectroscopy to identify significant compositional differences. The devitrifying glass contained significant amounts of zinc and zirconium, the oxides of which are present to serve as nucleating agents. Lesser amounts of aluminum and practically no lithium were found. On the other hand, the vitreous glass had no significant concentrations of heavy metals because it does not require nucleating agents. It did contain significantly higher amounts of lithium and aluminum than the devitrifying glass, with lesser amounts of zirconium and practically no zinc. This vitreous glass contains a filler, such as lithium aluminum silicate, to provide the required coefficient of thermal expansion. Table 1 summarizes the qualitative compositional differences in the glass types. Emission spectroscopic analyses were used to confirm glass identities during these investigations.

Sealing Profile

Figure 3 is the approximate sealing furnace temperature profiles for the glasses in this study. As implied by the DTA data, a higher peak sealing temperature is required to accomplish devitrification and secure a hermetic seal for devitrifying glass. The vitreous-glazed piece parts receive a conditioning pre-bake just prior to the sealing cycle.

Table 1.

Major Differences in Elemental Composition of Vitreous and Devitrifying Glass as Determined by DC Arc Optical Emission Spectroscopy

	Vitreous	Devitrifying
1%	Al	Zn, Zr
.01-1%	Zr, Li	Al
.01%	Zn	Li

* Illustrations start on page 6-10.

MEASURING MOISTURE IN PACKAGES

Determining package ambient moisture content is a developing state of the art. For the measurements described in this paper, two methods were employed.

Mass Spectroscopy

Figure 4 is a diagram of a typical system for package analysis; details of individual systems vary widely. A typical system consists of three main components: a sample opening chamber, the mass spectrometer to differentiate atomic species present in the sample, and a computerized data reduction system. The package opening chamber is mated to the mass spectrometer vacuum system, and is bakeable. The bake is critical to correct moisture results. A pre-analysis bake to 125°C removes water molecules adhered to outside sample surfaces and walls of the system to provide a low analysis background. During the analysis the chamber is maintained in excess of 100°C to assure that moisture remains desorbed from all die cavity surfaces. The evolved species leaving the opened package at different rates are conducted to the mass spectrometer via uniformly-heated system hardware to prevent selective loss of more condensible species. The gases arrive in the spectrometer where they are differentiated according to their atomic masses. The overall system is calibrated by analyzing commercially prepared gas mixtures. Detailed aspects of mass spectrometric package gas analysis have been described elsewhere. [15]

Surface Conductivity Vehicle

The second measurement method employed is a special device called a surface conductivity or condensation cell, [16] shown in Figure 5. These are in the form of chips fabricated in the integrated circuit production line by vacuum depositing aluminum over oxidized silicon, followed by a photoresist step to delineate closely spaced interdigitated metal stripes. The chips are mounted inside the package to be tested, bonded for external electrical connection, and the packages are then sealed by the applicable process to be investigated or monitored. The subject package is placed in a thermal chamber where it is initially heated to 100°C to promote desorption. It is then cooled at a controlled rate while monitoring conductivity of the electrode structure. At the temperature where water vapor in the cavity condenses to form water on the chip surface, the conductivity rises. The temperature at which the conductivity rises can then be converted to the corresponding water content of the specimen using the nomograph in Figure 6.

RESULTS OF PACKAGE AMBIENT ANALYSIS

The requirement to measure package ambient moisture to verify "dryness" is established by Method 1018 of MIL-STD-883B. This specification will ulitmately limit maximum allowable water vapor content to 500ppmv. This limit will exclude many of the existing Cerdip technologies for integrated circuits in high reliability applications.

In an effort to upgrade Cerdip technology, an ongoing program of monitoring sealed package ambients has been maintained in conjunction with a continuing package reliability testing program to understand device failure modes and assure high-quality dependable products. The following moisture information was gathered during testing over a two year period on packages sealed with a particular vitreous glass or two particular types of devitrifying glass. This data provides an excellent cross-section of results on a wide variety of manufacturer piece part lots and assembly production lots over that period. The data is comprised of measurements taken by mass spectroscopy and conductivity cell. Both methods were applied to packages sealed with both types of glass investigated.

Devitrifying Glass

Figure 7 shows the moisture distribution for packages sealed with devitrifying glass. This 42-sample group exhibited a mean dewpoint value of -6°C. Seventeen percent of these packages contained less than 500ppmv water, while 46% contained more than 6000ppmv water.

Vitreous Glass

Figure 8 shows the moisture distribution for packages sealed with vitreous glass. This 65-sample group exhibited a mean dewpoint value of -37°C. Ninety-one percent of these Cerdips contained less than 500ppmv water.

Metal Seal Packages

Figure 9 is the same information for a 21-sample group of metal-sealed packages, whose mean dewpoint was -38°C.

SEALING GLASS AND MOISTURE

From this data it is evident that vitreous solder glass is a key to producing a dry package ambient. A number of factors contribute to these reduced moisture levels.

One is that raw vitreous glass with lithium aluminum silicate or similar compounds contains roughly an order of magnitude less desorbable water than devitrifying glass. Aluminosilicate glass has been determined by pressure-rise and mass spectrometry measurements to contain about fifteen times less bound water than borosilicate glass.[17] This smaller amount of desorbable water in vitreous glass could be due to two factors. The aluminosilicate may be reducing the number of bonding sites for hydroxyl groups in the $PbO-B_2O_3$ structure. Or, it may be binding water of hydration within its own structure much more tightly than the $PbO-B_2O_3$ network would alone. Whatever the mechanism, bulk glass which includes aluminosilicate or related compounds will contain or release fewer water molecules per unit volume than other glasses.

A second factor is the pre-seal conditioning bake of the vitreous glass. This causes the glass to desorb much of its native water prior to the sealing operation. When this bake is followed by direct introduction of parts to the sealing furnace, the glass arrives at seal formation without opportunity to re-hydrolyze ambient moisture. This method insures for the sealing operation a dry glass which has been pre-outgassed of much of its initial water content. The sealed glass of the finished package thus has substantially less water to release to the cavity ambient during the life of the part. Devitrifying glass connot effectively be pre-seal baked since any premature devitrification could result in hermeticity failure of the finished part.

The primary factor contributing to the higher moisture levels of devitrifying glass package ambients is the events which occur at devitrification. On the atomic level, a very energetic situation prevails as the $PbO-B_2O_3$ system undergoes the nucleation process with ZnO (the D' – D'' region on the DTA curve). At this time many chemical bonds are broken and re-formed as atomic rearrangements occur and the glass assumes a more highly-ordered lattice network. These events, which occur just at the critical time the hermetic seal is being formed, free water molecules originally bound in the glass. These molecules evolve and many of them are then trapped within the package cavity. Because of this process, packages sealed with devitrifying glass will always tend to have die cavities with higher moisture contents.

Still another contributing factor, though possibly of second-order importance, is the greater potential for water desorption from devitrifying glass during the operating lifetime of the part. In contrast, the aluminosilicate component of the vitreous glass in this study imparts a continuing dryness property which reduces the tendency to evolve moisture with time. This effect is suggested by the activation energy for water desorption from borosilicate and aluminosilicate glasses, which has been reported as 21 and 49 kcal/gram-mole, respectively.[18]

Reliability Qualification of Vitreous Glass-Sealed Cerdips

Package qualification operating life tests were conducted for vitreous Cerdips in accordance with Method 5005.3 of MIL-STD-883. Low power dissipation circuit types, such as CMOS digital devices which operate with minimal chip temperature rise, were assembled in vitreous glass Cerdips. These were placed under 10-15V reverse bias at $\leqslant$ 25°C. Low

ambient operating temperatures allow condensation of cavity moisture, and electrical bias may then initiate corrosion of thin film metallization rendering the device non-functional. Table 2 shows that 1373 devices operated at 25°C or 0°C for a total of 4.531M device hours with zero failures. Delidding and visual examination of the packages as they completed life test showed no corrosion effects whatever on any of the devices.

Table 2.

Vitreous Sealing Glass

Applied Stress	No. of Devices	Device-Hours	No. of Failures
A. Static Operating Life @ Vdd = 10 to 15V @ 25°C Ambient	1313	4.447M	0 (See Note 1)
B. Static Operating Life @ Vdd = 10 to 15V @ 0°C	60	84.0K	0 (See Note 1)

Note 1 — Resulting Failure Rate: 0.02%/1000 Hours @ 60% Confidence

Identical device types were also assembled in a specific devitrifying glass package, known to have considerable moisture in the cavity, and these were then life-tested under the same conditions. Table 3 shows that 455 of these devices operated 125.5K device hours at 25°C experienced 79 corrosion-related failures. The failures were verified by visual examination. This package/glass structure was never qualified for use on deliverable product.

Table 3.

Devitrifying Sealing Glass

Applied Stress	No. of Devices	Device-Hours	No. of Failures
Static Operating Life @ Vdd = 10-15 Volts @ 25°C Ambient (See Note 2)	455	125.5K	79 (See Note 1)

Note 1 — Resulting Failure Rate: 65%/1000 Hours @ 60% Confidence
Note 2 — Low Ambient Temp. to Enhance Dewpoint Stimulation

Table 4 shows freeze-out test results conducted on 500-600mW Bipolar PROMs assembled with vitreous glass. The devices were power-cycled at low temperatures for a total of 385.1K device hours with no corrosion-related failures observed.

It must be emphasized that some devitrifying glasses, although possessing cavity ambients with more than 500ppmv moisture, do not necessarily induce corrosion failure. For example, Table 5 illustrates the results of freeze-out testing of PROM type circuits in a devitrifying glass package. For this particular 74 package group zero failures occurred. As the moisture distribution data of Figure 7 implies, a significant percentage of these packages are dry enough for corrosion to be avoided. Obviously, however, a drier package is preferred for overall reliability considerations.

Extensive package environmental-related physical parameter testing of vitreous Cerdips via MIL-STD-883 testing scheme resulted in zero failures for all tests applied as shown in Table 6.

Table 4.

Freeze-Out Test Results of Bipolar (500-600mW) PROMS
Vitreous Glass

Mo/Yr	Ambient Temp.	Number of Failures*	Test Duration	Sample Size
4/76	-30C	0	168 Hrs.	36
6/76	-30C	0	168 Hrs.	36
11/76	-20C	0	168 Hrs.	36
3/77	-25C	0	168 Hrs.	22
3/77	-20C	0	168 Hrs.	36
6/77	-20C	0	500 Hrs.	35
6/77	-20C	0	1K Hrs.	34
7/77	-20C	0	1K Hrs.	70
9/77	-40C	0	1K Hrs.	125
10/77	-55C	0	1K Hrs.	24
10/77	-40C	0	1K Hrs.	84
11/77	-30C	0	1K Hrs.	16
Total		0	385.1K Hrs.	554

*Corrosion related failures. Power burn-in at rated V_{CC} = +5V is cycled 3 minutes off for the duration of the test.

Table 5.

Freeze-Out Test Results – HPROMs Sealed in Devitrifying Glass

Temperature	Sample Size	Test Duration	No. of Cycles	No. of Failures
-30C	30	72 Hrs.	720	0
-30C	20	24-48 Hrs.	240-480	0
-10C	24	500 Hrs.	5000	0

Pulsating Operating Condition: 3 minutes power on and 3 minutes power off at ambient temperature.

Table 6.

MIL-STD-883B Tests of Vitreous Cerdips

Test	Method	Samples/ Failures
Physical Limitations Lead Integrity Solderability	M-2016 M-2004 M-2003	283/0
Salt Atmosphere	M-1009	125/0
Bond Strength	M-2011	80/0
Thermal Shock Temp. Cycle Moisture Resistance Fine/Gross Leak	M-1011 M-1010 M-1004 M-1014	309/0
Mechanical Shock Vibration Var. Freq. Constant Acc. Visual	M-2002 M-2007 M-2001 M-2009	322/0

CONCLUSION

As the foregoing discussion shows, Cerdip packages can now be produced to contain typically less than 500ppmv of cavity ambient moisture when vitreous sealing glass is used. Devitrifying glasses have historically produced wetter Cerdips because devitrifying glass:

1. Has higher native moisture content.
2. Can not be outgassed of water prior to seal.
3. Upon devitrifying. evolves significant moisture which is subsequently trapped in the cavity.
4. Is more likely to continue desorbing water into the cavity over the lifetime of the part.

Cerdip technology now offers a package which not only provides needed mechanical and reliability properties, but also offers the desired performance without likelihood of failure due to metallization corrosion. The internal cavity moisture condition which insures absence of corrosion is reproducibly attained by using vitreous low temperature solder glass of the proper composition to form the hermetic seal. The resulting moisture levels over the lifetime of the part are comparable to those provided by braze or weld sealed packages used heretofore where moisture-induced corrosion was to be avoided.

A unique combination has now been established between solder glass technology permitting economical volume processing of dry Cerdips and the added quality assurance for finished parts available from advancing state-of-the-art in measuring cavity ambient compositions (as reflected in Method 1018 of MIL-STD-883B). This combination will make the Cerdip more attractive for future cost control while continuing to maintain the high-reliability performance essential in the critical applications of integrated circuits.

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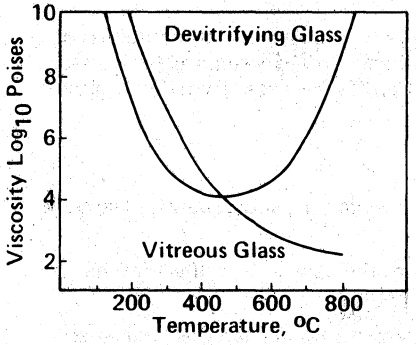


FIGURE 1 – Sealing Glass Viscosities

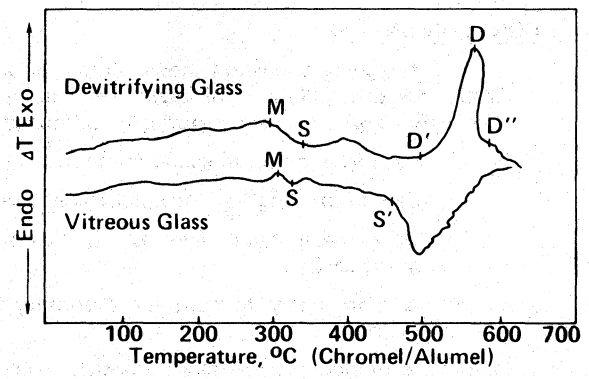


FIGURE 2 – Differential Thermal Analysis

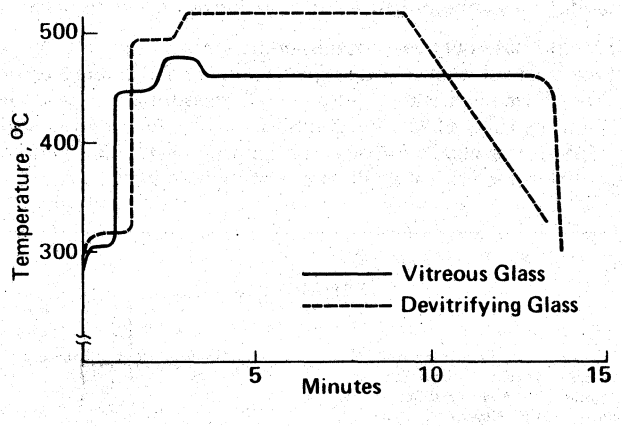


FIGURE 3 – Nominal Seal Furnace Profiles

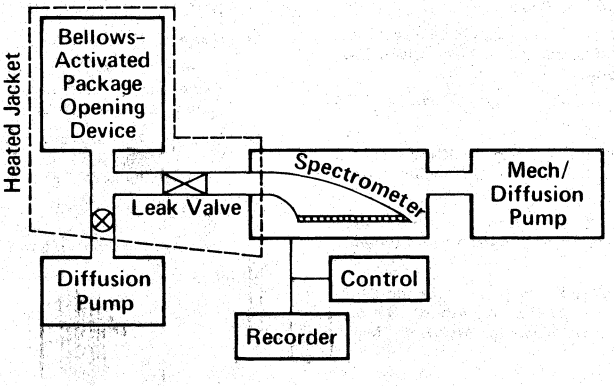


FIGURE 4 – Mass Spectrometer

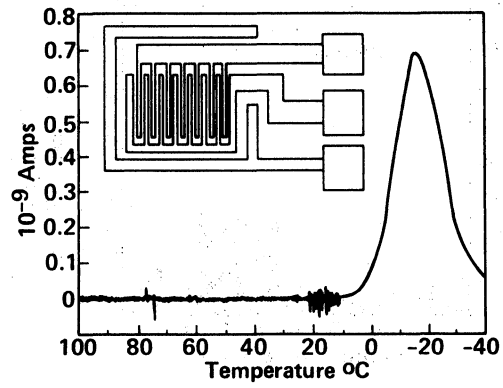
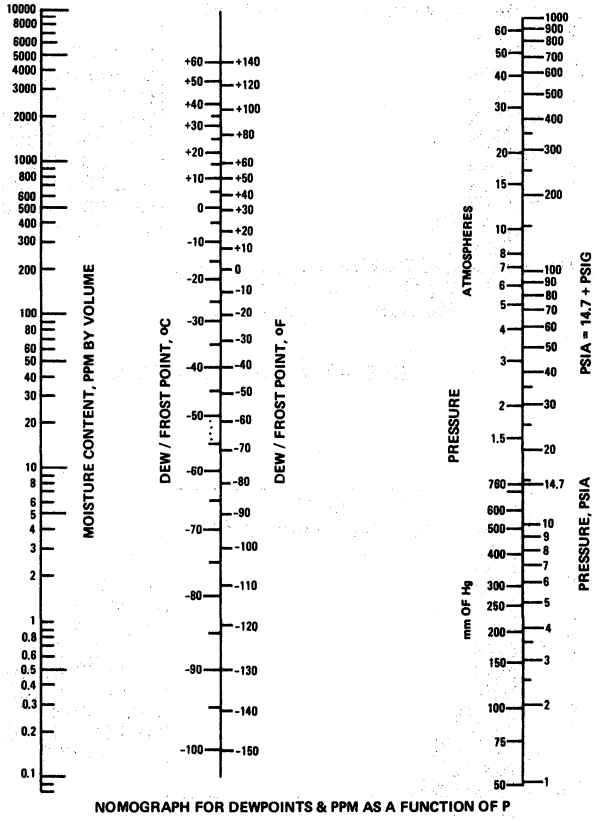


FIGURE 5 – Surface Conductivity Vehicle



NOMOGRAPH FOR DEWPOINTS & PPM AS A FUNCTION OF P

FIGURE 6

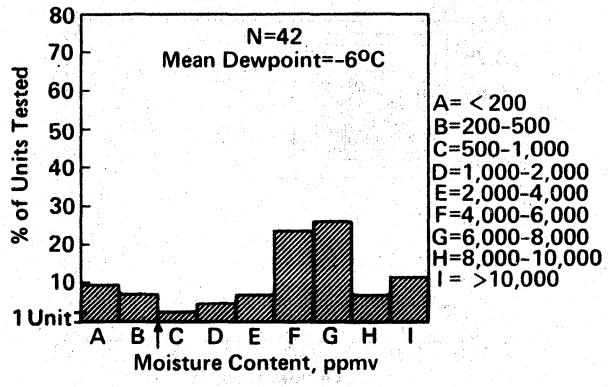


FIGURE 7 – Devitrifying Sealing Glass

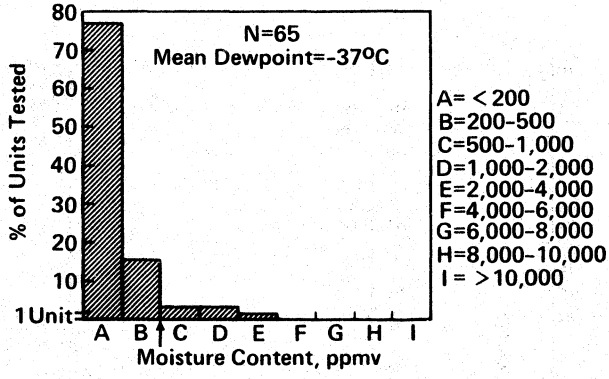


FIGURE 8 – Vitreous Sealing Glass

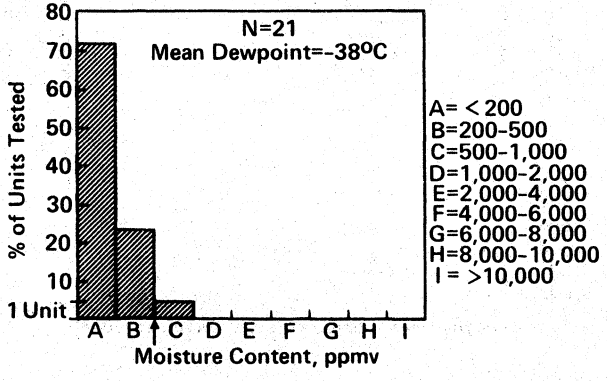


FIGURE 9 – Metal-Seal Packages

PRODUCT	1* CERDIP	3* EPOXY	9* CERPACK
HM-0104	4U		9H
HM-0168	4U		9H
HM-0186	4U		9H
HM-0198			8C
HM-0410	4U		9H
HM-6312	4G	3D	8C
HM-6388 (Preliminary)			
HM-6389 (Preliminary)			
HD-6431	4Z	3G	8B
HD-6432	4N	3D	8C
HD-6433	4Z	3G	8B
HD-6440	4N	3D	8C
HD-6495	4Z	3G	8B
HD-6600	4D		
HM-6501	4M	3E	8E
HM-6503	5B	3D	8H
HM-6504 †	5B	3D	8H
HM-6508	4P	3G	8B
HM-6512	4N	3D	8C
HM-6513	5B	3D	8C
HM-6514 †	5B	3D	8C
HM-6518 †	4N	3D	8C
HM-6533	4M	3E	8K
HM-6543	4M	3E	8K
HM-6551	4M	3E	8E
HM-6561 †	4N	3D	8C
HM-6562	4P	3G	8B
HM-6611	5C		8B
HM-6661	4N		8C
JAN-0512	4K		
HM-7602	4Z	3G	8B
HM-7603	4Z	3G	8B
HM-76LS03	4Z	3G	8B
HM-7608	4K	3F	8F
HM-7610	4Z	3G	8B
HM-7610A	4Z	3G	8B
HM-7611	4Z	3G	8B
HM-7611A	4Z	3G	8B
HM-7616	5A		8L
HM-7620	4Z	3G	8B
HM-7620A	4Z	3G	8B
HM-7621	4Z	3G	8B
HM-7621A	4Z	3G	8B
HM-7625R	4K	3F	8F
HM-7629	4K	3F	8F
HM-7640	4K	3F	8F
HM-7640A	4K	3F	8F
HM-7640AR	4K	3F	8F

* These package numbers to be used in product ordering. Other numbers shown in Selection Guide and drawings are internal package numbers.

† Available in Leadless Carriers. See page 6-19.

Selection Guide

(Continued)

PRODUCT	1* CERDIP	3* EPOXY	9* CERPACK
HM-7641	4K	3F	8F
HM-7641AR	4K	3F	8F
HM-7642	4N	3D	8C
HM-7642A	4N	3D	8C
HM-7642P	4N	3D	8C
HM-7643	4N	3D	8C
HM-7643A	4N	3D	8C
HM-7643P	4N	3D	8C
HM-7644	4P	3K	8C
HM-7644A	4P	3K	8C
HM-7647R	4K	3F	8F
HM-7648	4L	3N	8D
HM-7649	4L	3N	8D
HM-7680	4K	3F	8F
HM-7680R	4K	3F	8F
HM-7680P	4K	3F	8F
HM-7680RP	4K	3F	8F
HM-7681	4K	3F	8F
HM-7681R	4K	3F	8F
HM-7681P	4K	3F	8F
HM-7681RP	4K	3F	8F
HM-7683	4L		8J
HM-7684	5E		8H
HM-7684P	5E		8H
HM-7685	5E		8H
HM-7685P	5E		8H
HM-7686	4L		8J
HM-7686R	4L		8J
HM-7686P	4L		8J
HM-7686RP	4L		8J
HM-7687	4L		8J
HM-7687R	4L		8J
HM-7687P	4L		8J
HM-7687RP	4L		8J
HM-76160	5A		8L
HM-76161	5A		8L

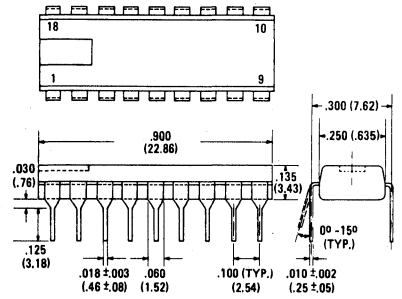
† Available in Leadless Carriers. See page 6-19.

NOTE FOR PACKAGE DRAWINGS ON FOLLOWING PAGES:

1. All dimensions in inches; millimeters are shown in parentheses.
2. All dimensions ± .010 (± 0.25mm) unless otherwise shown.
3. Internal package codes are shown in black squares.

Package Dimensions

3D — 18 LEAD EPOXY



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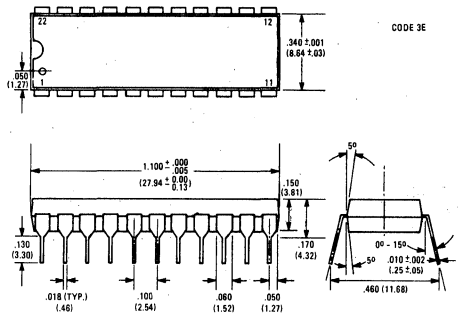
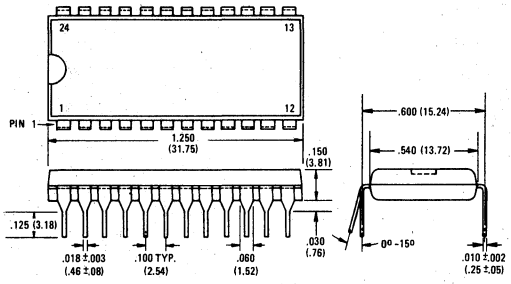
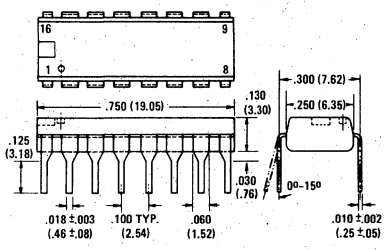


3F — 24 LEAD EPOXY



3G — 16 LEAD EPOXY



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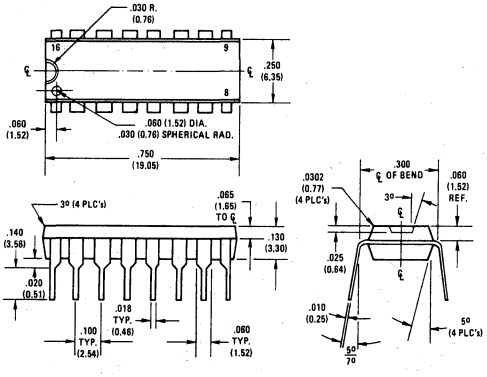

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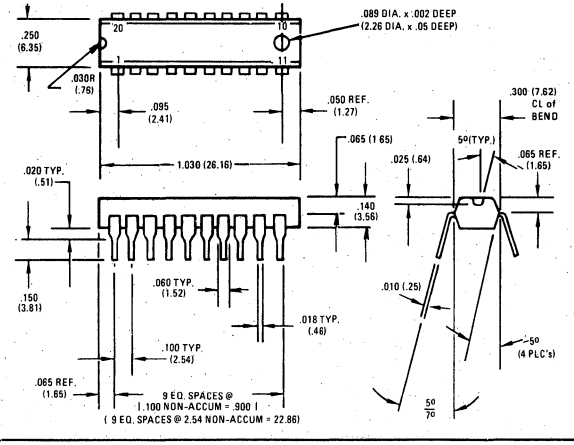
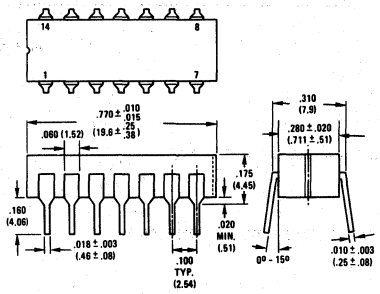
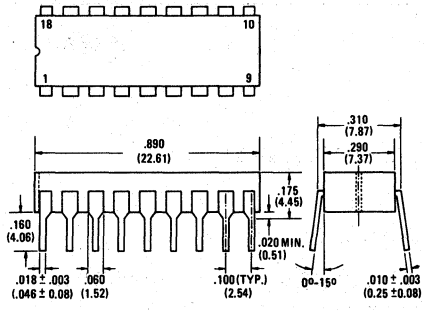


4D 5D — 14 LEAD CERDIP



4G 4N 5B 5E — 18 LEAD CERDIP



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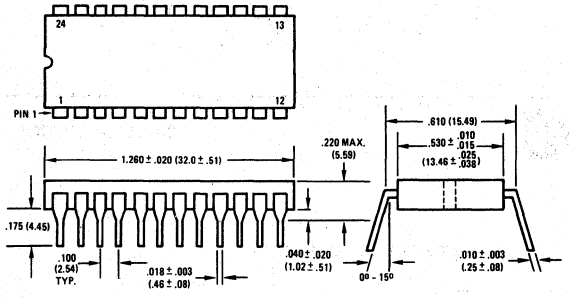

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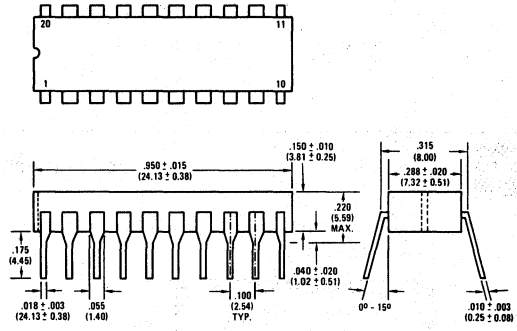

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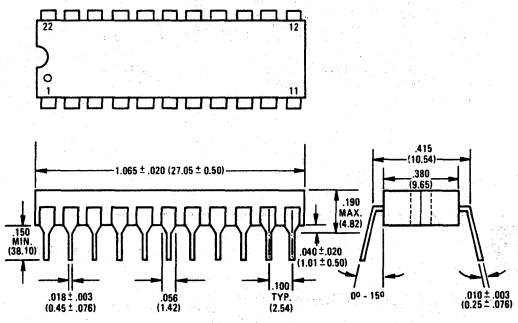

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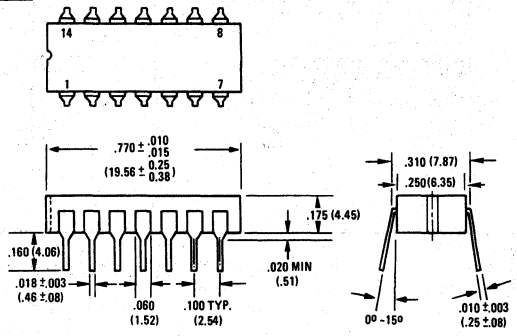

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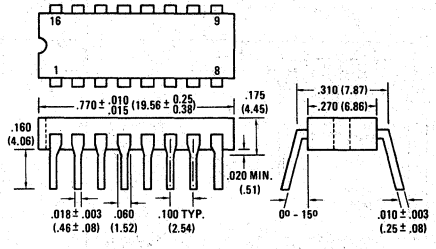
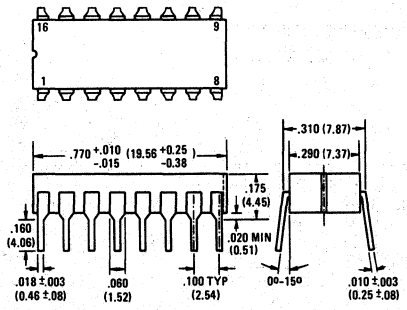


5C — 16 LEAD CERDIP



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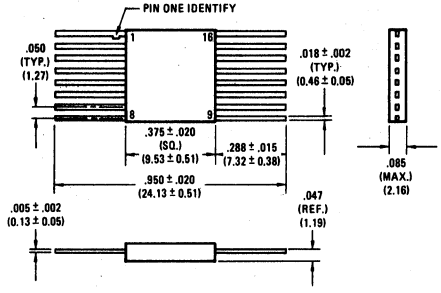
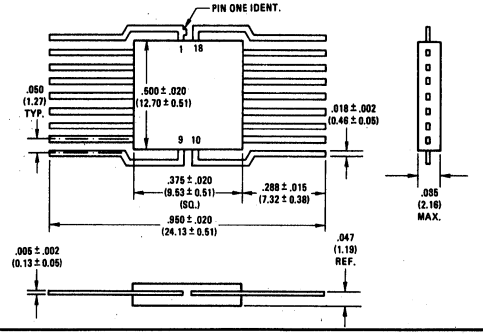


8C 18 LEAD CERPACK



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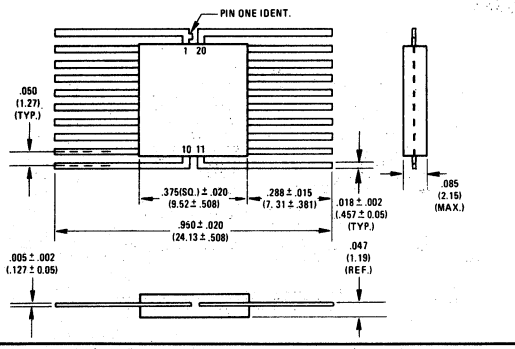

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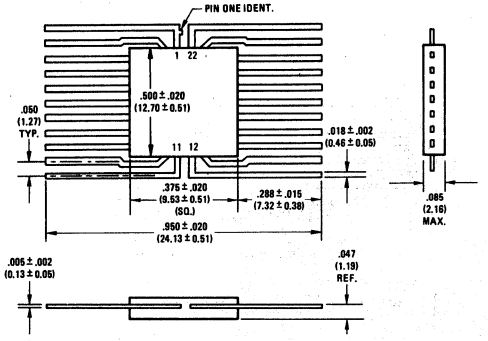
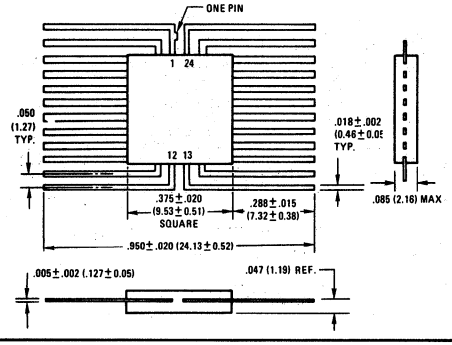


8F 24 LEAD CERPACK



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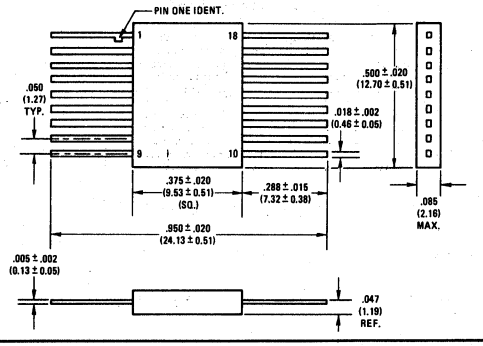

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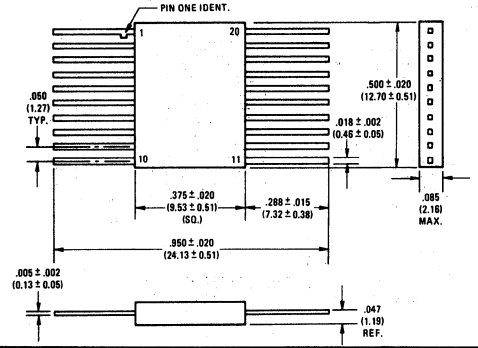

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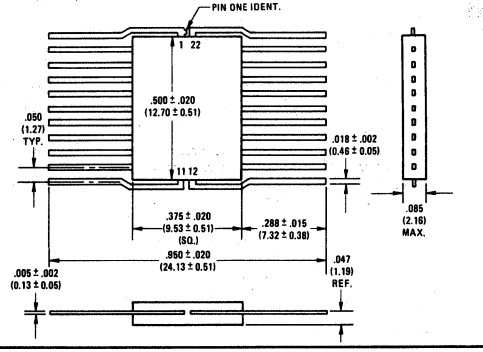
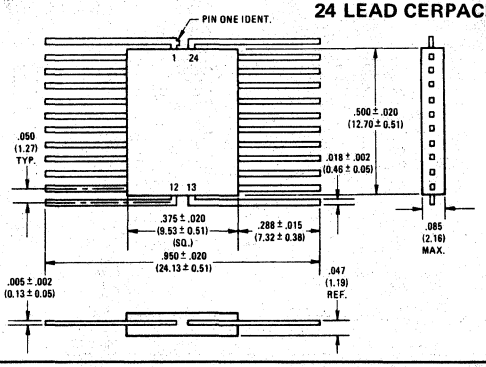


8L — 24 LEAD CERPACK



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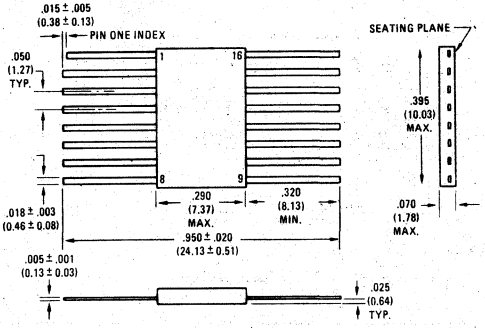

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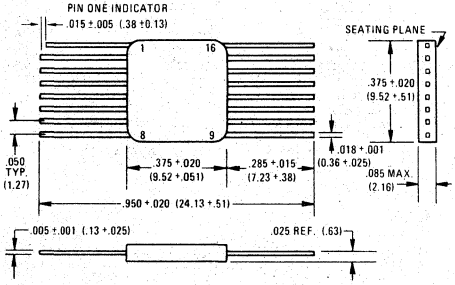
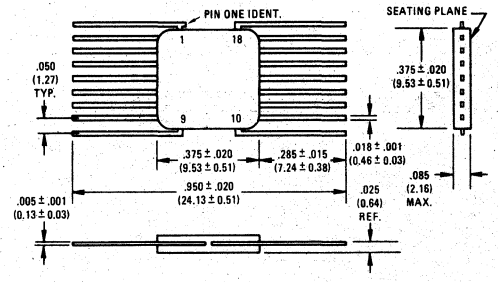


9D — 18 LEAD FLATPACK



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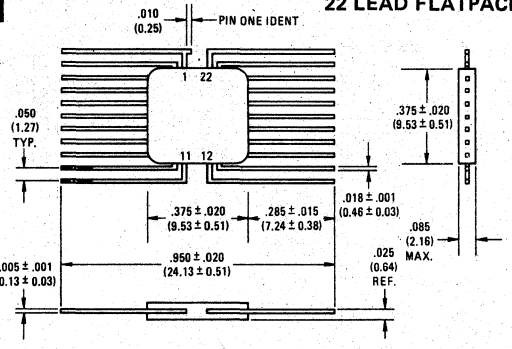

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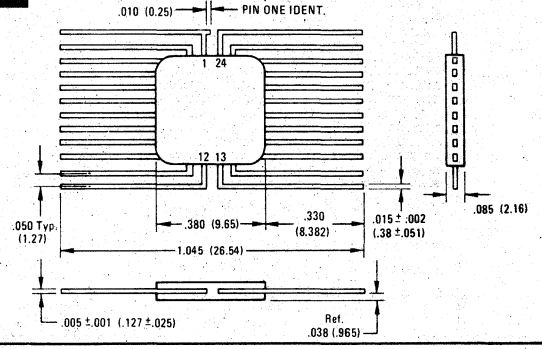
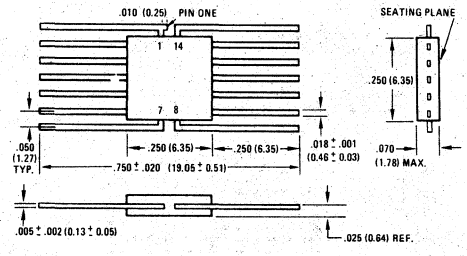


9H — 14 LEAD FLATPACK



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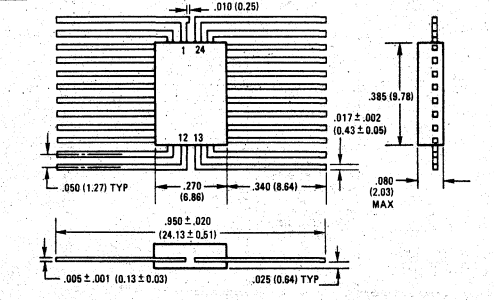


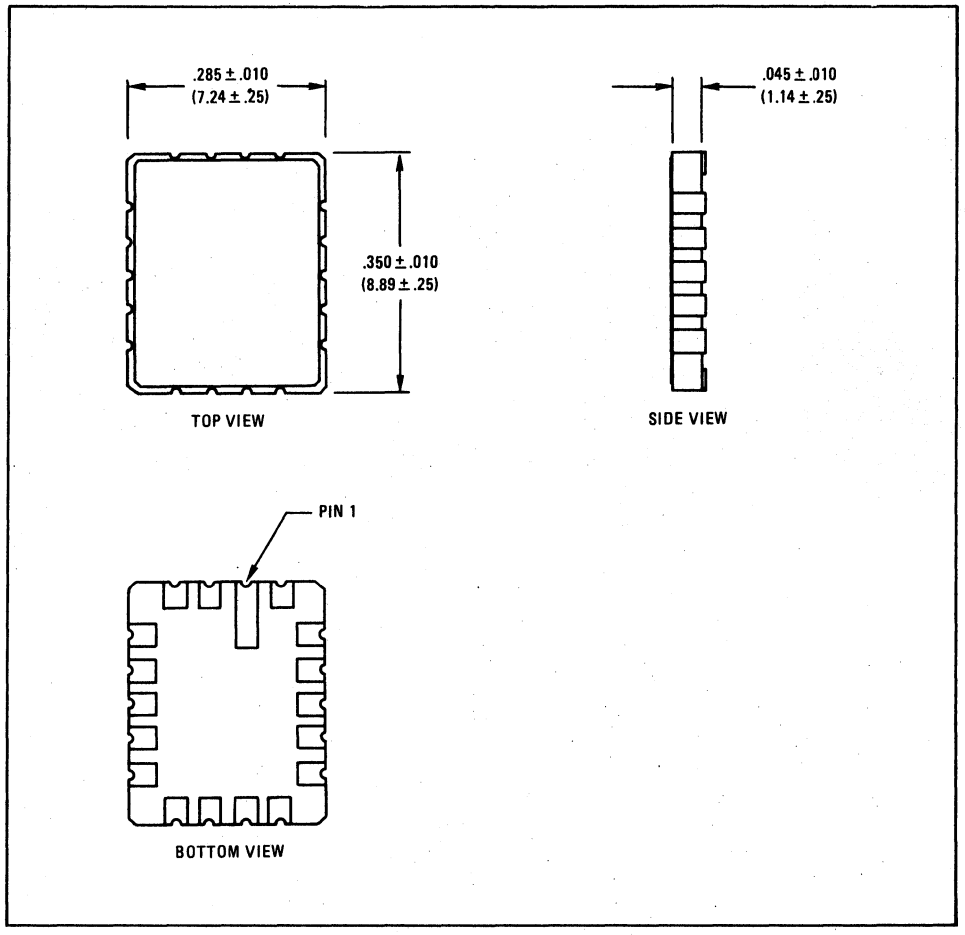
Leadless Carriers

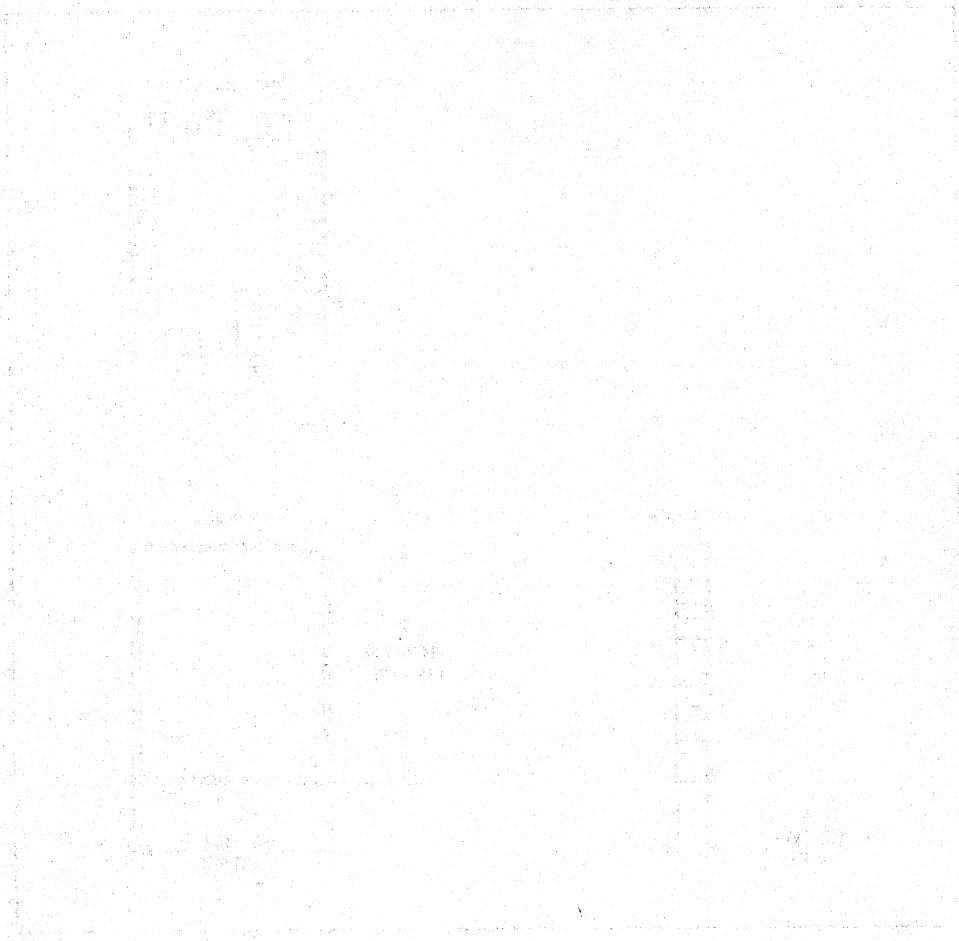
Harris Semiconductor is offering four CMOS RAMs in 18 pin leadless carriers. Electrical specifications for these parts are identical to the equivalent product in the standard DIP package. Mechanical specifications for the 18 pin leadless carriers are shown below. For availability and additional information contact your nearest Harris Representative or Harris Sales Office.

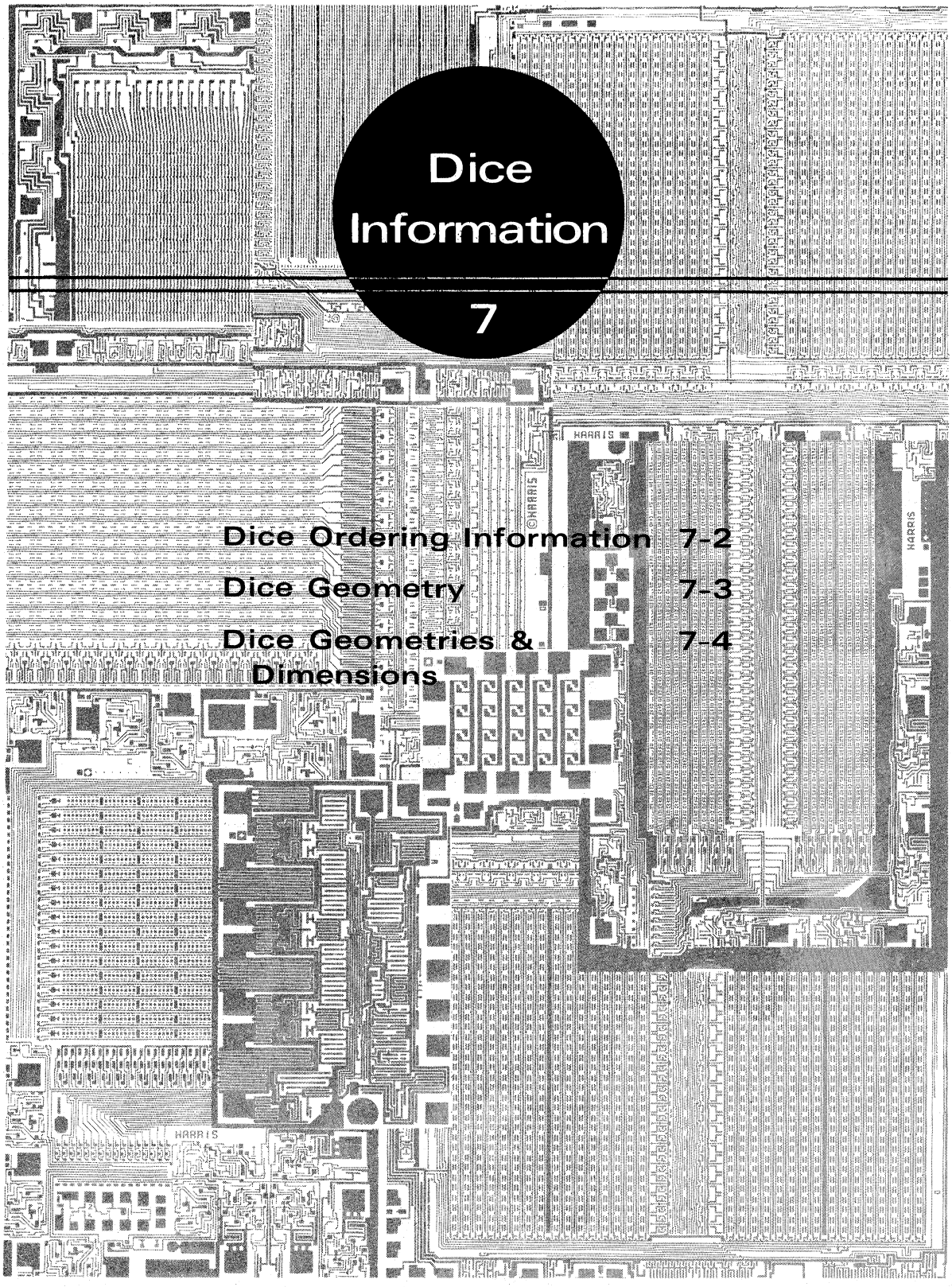
All electrical grades of the following product types are available as stock items:

HM4-5618	1024 x 1	CMOS RAM	18 Pin
HM4-6561	256 x 4	CMOS RAM	18 Pin
HM4-6504	4096 x 1	CMOS RAM	18 Pin
HM4-6514	1024 x 4	CMOS RAM	18 Pin

The Package Code for Leadless Carriers is 4.







Dice Information

7

Dice Ordering Information

GENERAL INFORMATION

Harris Memory Products are available in chip form to the hybrid micro circuit designer. The standard chips are DC electrically tested at +25°C to the data sheet limits for the commercial device and are 100% visually inspected to MIL-STD-883, Method 2010, Condition B criteria. Packaging for shipment consists of waffle pack carriers plus an anti-static cushioning strip for extra protection.

The hybrid industry has rapidly become more diversified and stringent in its requirements for integrated circuits. To meet these demands Harris has several options additional to standard chip processing available upon request at extra cost. For more information consult the nearest Harris Sales Office.

CHIP ORDERING INFORMATION

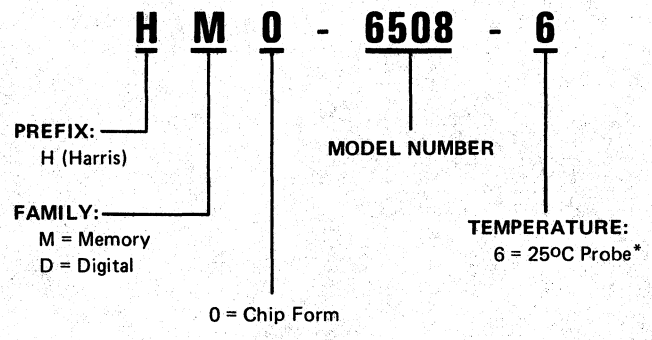
Standard and special chip sales are direct factory order only. The minimum order on all sales is $250.00 per line item. Contact the local Harris Sales Office for pricing and delivery on special chip requirements.

MECHANICAL INFORMATION

Dimensions: All chip dimensions nominal with a tolerance of ±.003". Maximum chip thickness is .012".

Bonding Pads: Minimum bonding pad size is .004" x .004" unless otherwise specified.

PRODUCT CODE EXAMPLE



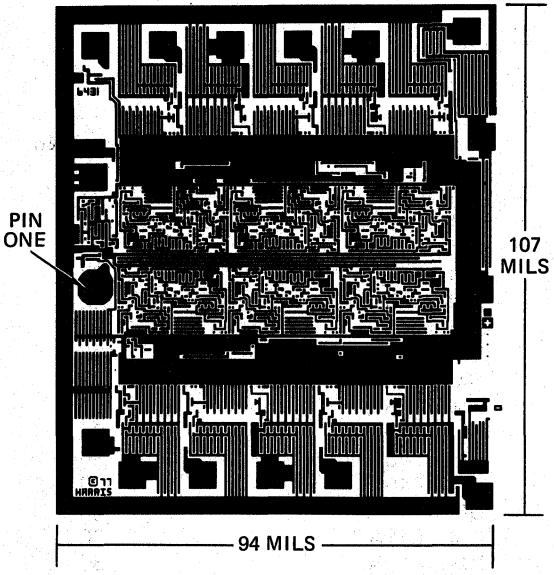
*Contact Harris for availability of -2 (-55°C to +125°C) dice.

NOTE: All Harris Digital Memory Products have biased substrates. Persons wishing to utilize product in dice form should contact the Harris factory for specific product information regarding proper connection of the substrate.

Dice Geometry Index

Product	Drawing No.	Product	Drawing No.
HD-6431	1	HM-7625R	27
HD-6433	1	HM-7647R	27
HD-6495	1	HM-7648	27
HD-6432	2	HM-7649	27
HD-6440	3	HM-7629	28
HD-6600	4	HM-7640	28
HM-0104	5	HM-7641	28
HM-0168	6	HM-7642	29
HM-0186	7	HM-7643	29
HM-0198	8	HM-7644	29
HM-0410	9	HM-7640A	30
HM-6312	10	HM-7640AR	30
HM-6501	11	HM-7641A	30
HM-6551	11	HM-7641AR	30
HM-6503	12	HM-7642A	31
HM-6504	12	HM-7642P	31
HM-6508	13	HM-7643A	31
HM-6512	14	HM-7643A	31
HM-6513	15	HM-7643P	31
HM-6514	15	HM-7616	32
HM-6518	16	HM-76160	32
HM-6561	17	HM-76161	32
HM-6562	18		
HM-6611	19		
HM-6661	20		
HM-7602	21		
HM-7603	21		
HM-76LS03	21		
HM-7608	22		
HM-7680/80R/80P/80RP	22		
HM-7681/81R/81P/81RP	22		
HM-7610	23		
HM-7611	23		
HM-7610A	24		
HM-7611A	24		
HM-7620	25		
HM-7621	25		
HM-7620A	26		
HM-7621A	26		

1 HD-6431, HD-6433, HD-6495



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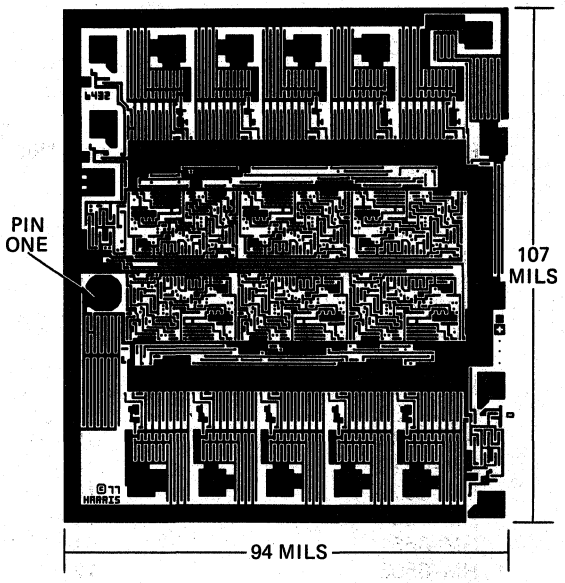
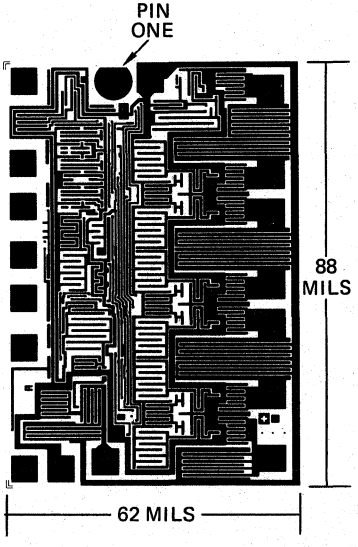
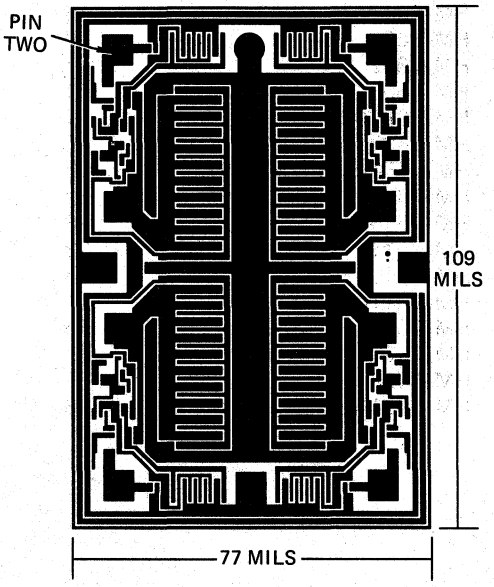


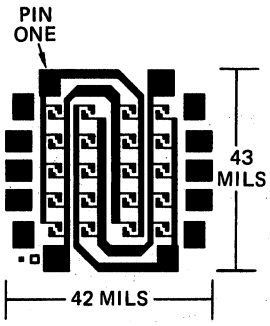
3 HD-6440



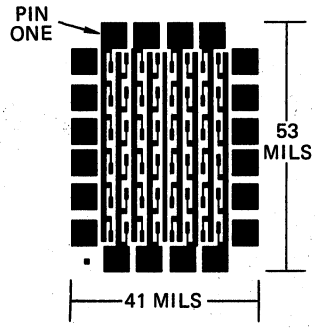
4 HD-6600



5 HM-0104



6 HM-0168



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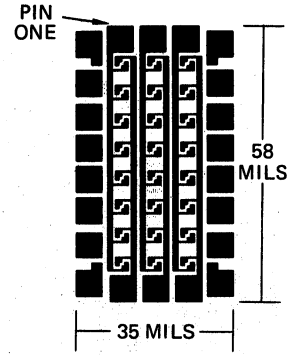

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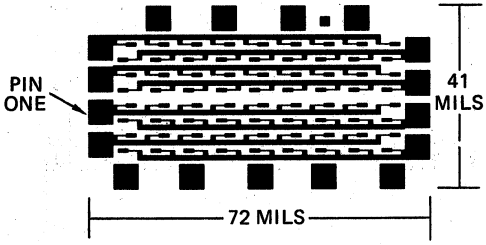
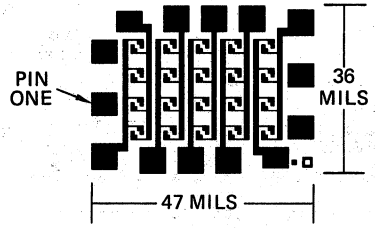
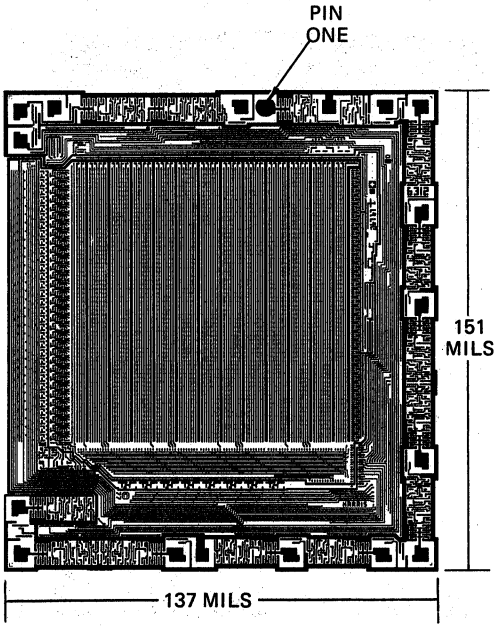


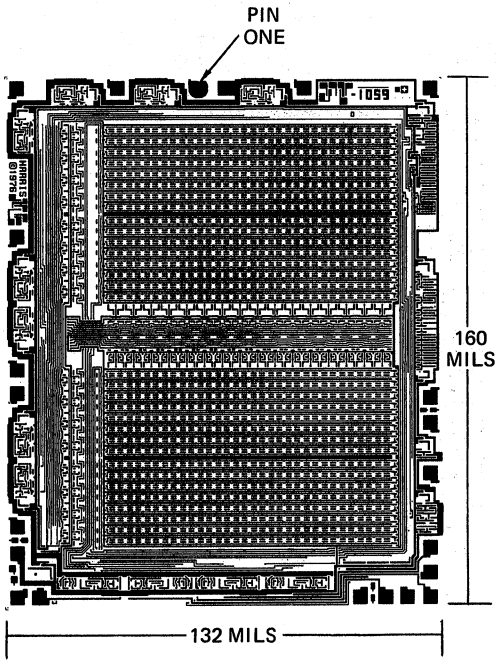
9 HM-0410



10 HM-6312



11 HM-6501, HM-6551



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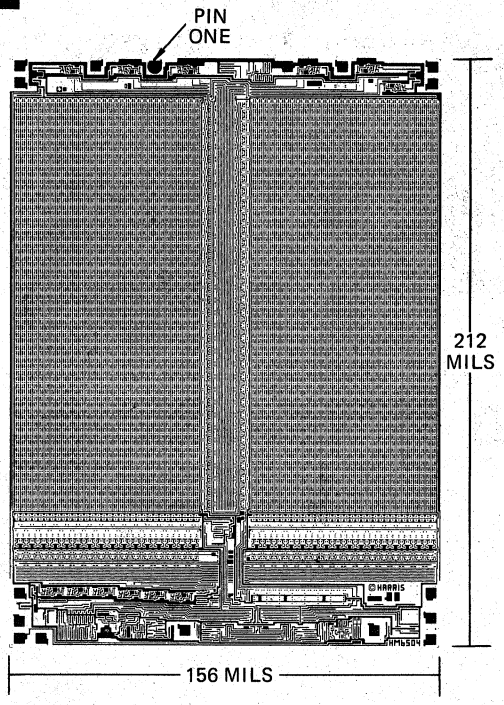

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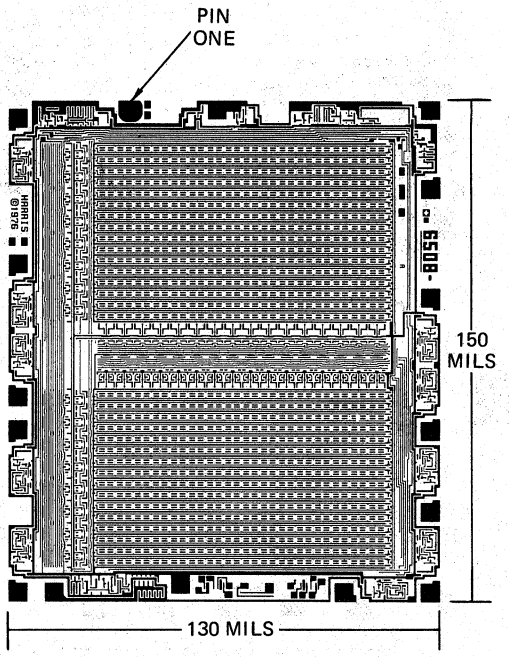

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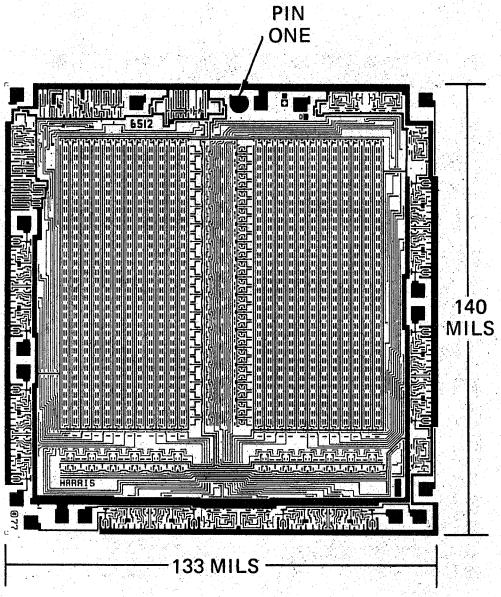

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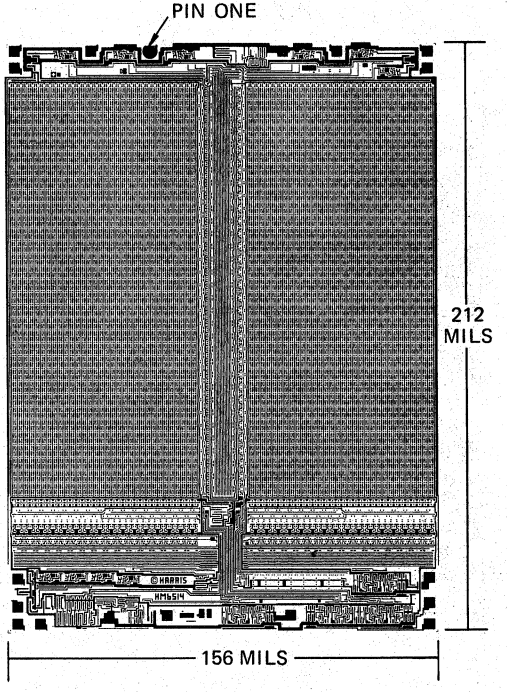
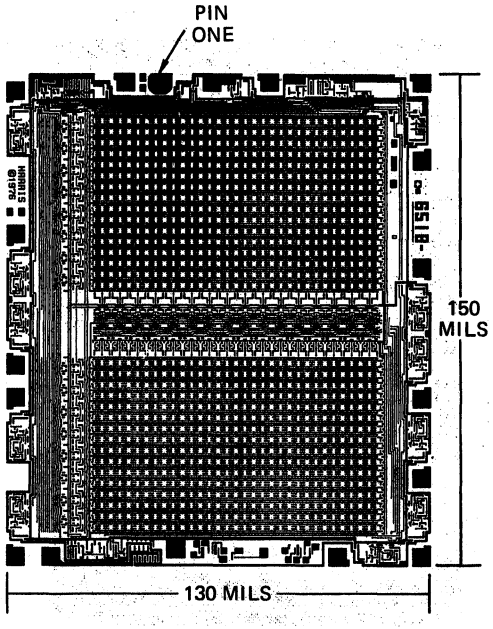
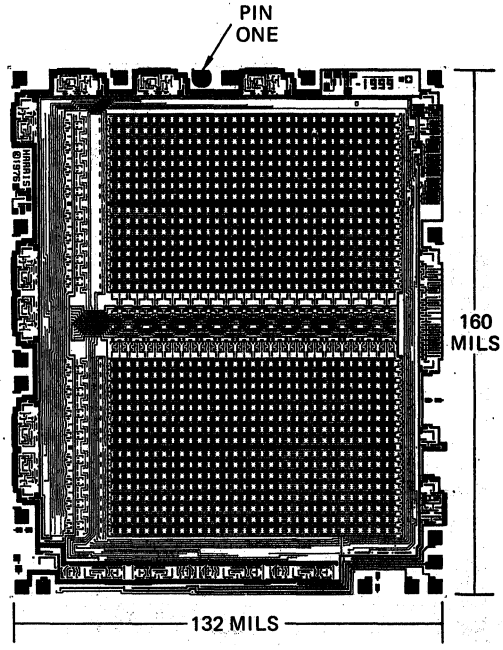


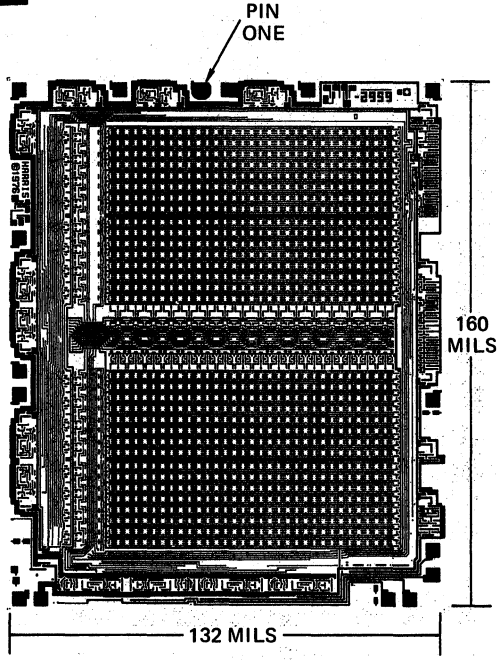
16 HM-6518



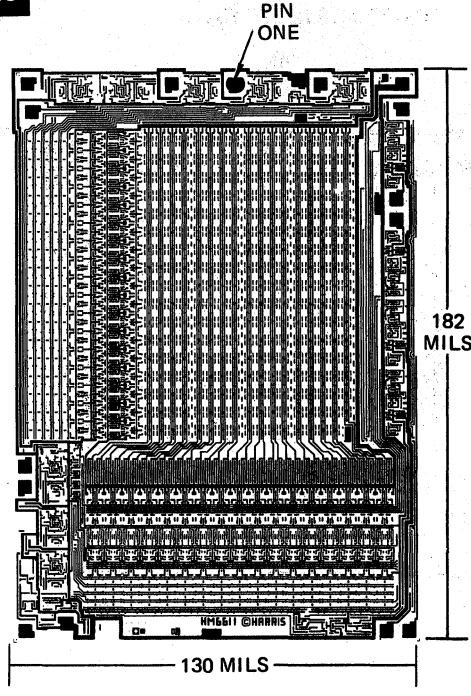
17 HM-6561



18 HM-6562



19 HM-6611



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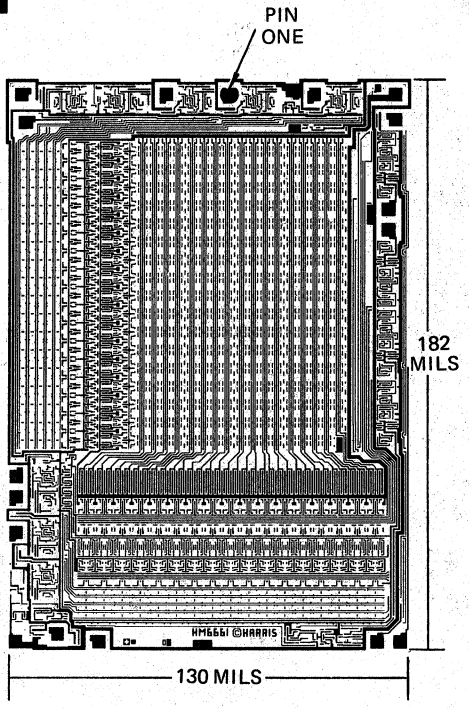
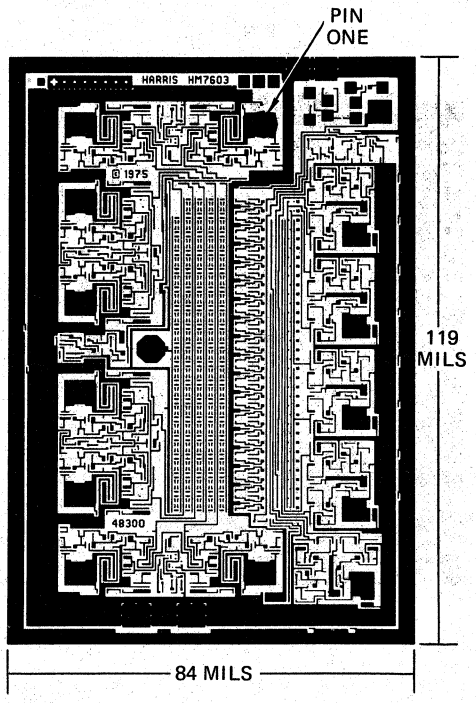
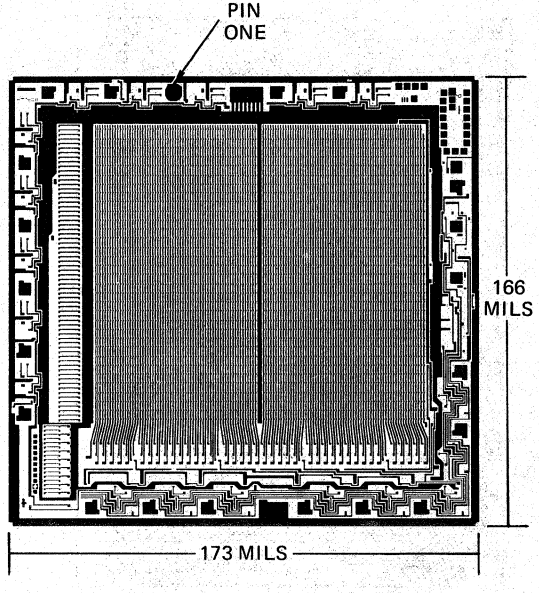


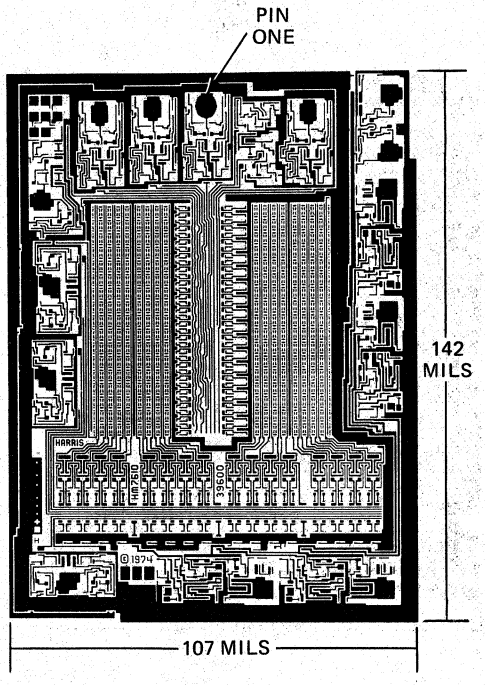
21 HM-7602, HM-7603, HM-76LS03



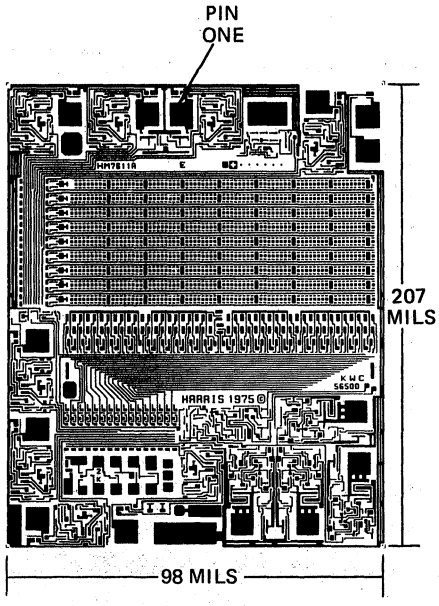
22 HM-7608, HM-7680/80R/80P/80RP, HM-7681/81R/81P/81RP



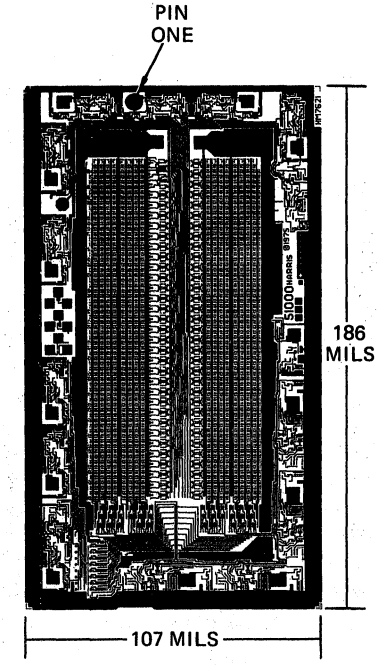
23 HM-7610, HM-7611



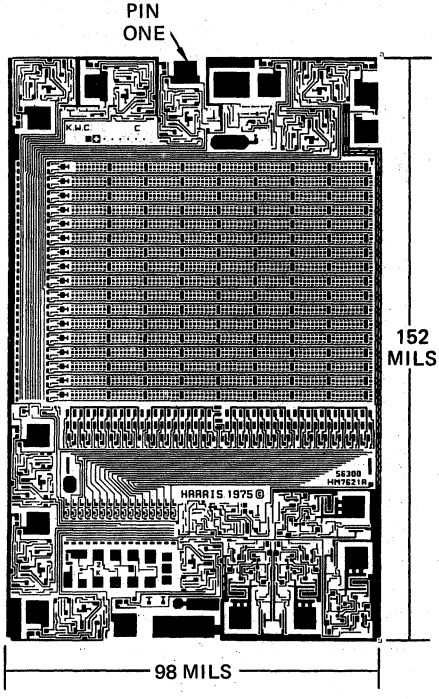
24 HM-7610A, HM-7611A



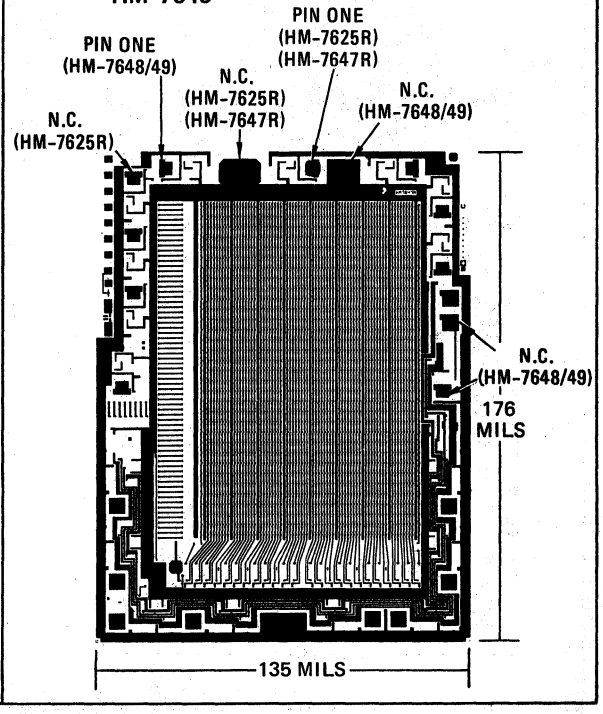
25 HM-7620, HM-7621



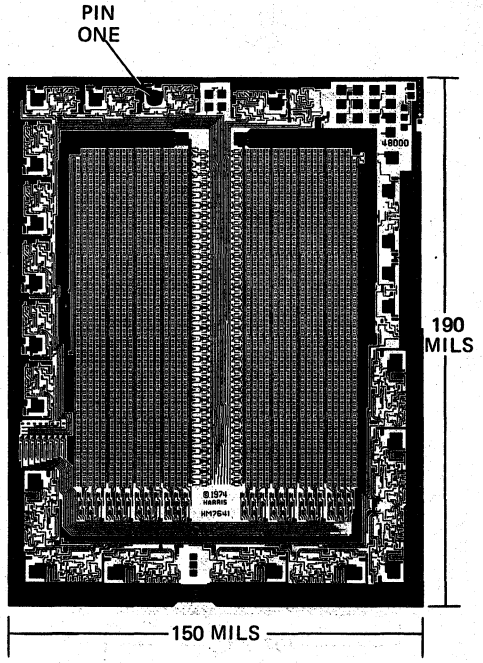
26 HM-7620A, HM-7621A



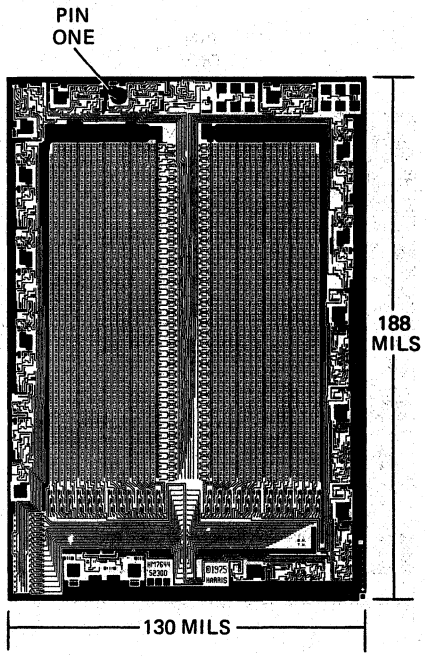
27 HM-7625R, HM-7647R, HM-7648, HM-7649



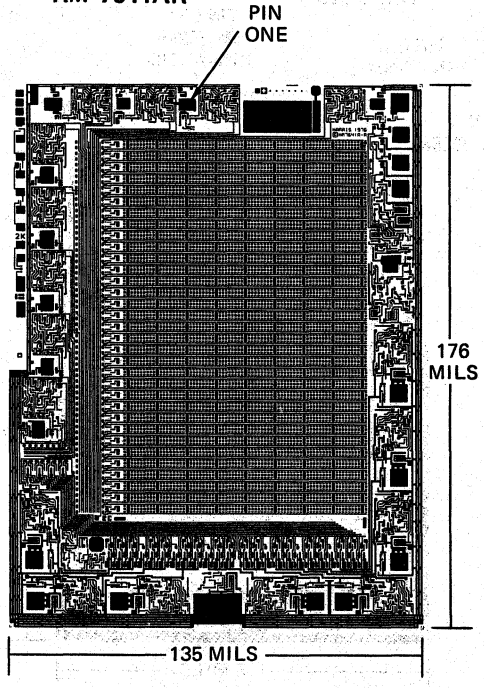
28 HM-7629, HM-7640, HM-7641



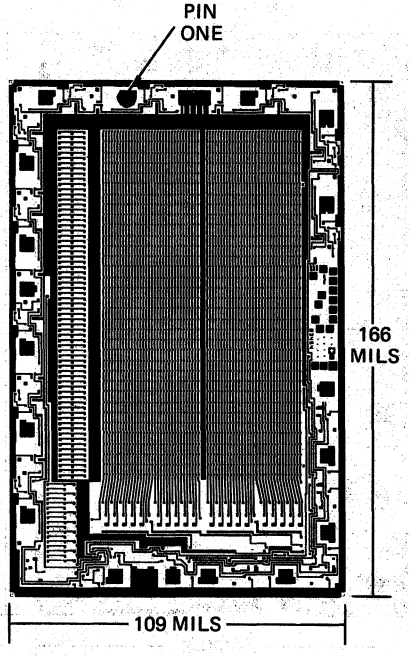
29 HM-7642, HM-7643, HM-7644

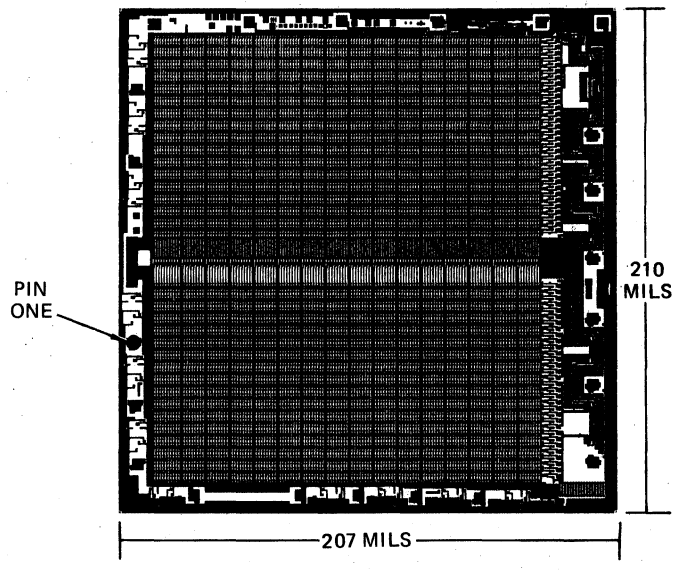


30 HM-7640A, HM-7640AR, HM-7641A, HM-7641AR



31 HM-7642A, HM-7642P, HM-7643A, HM-7643P

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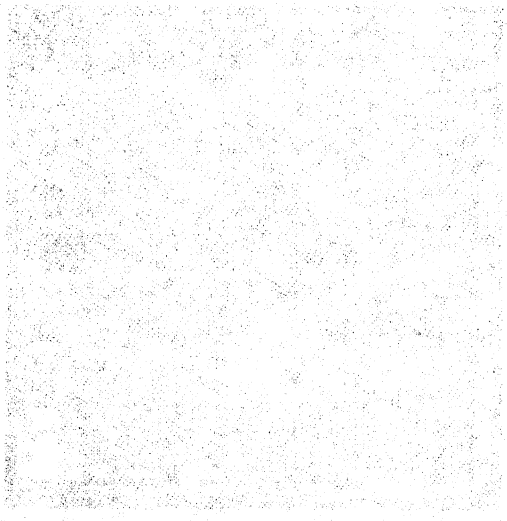

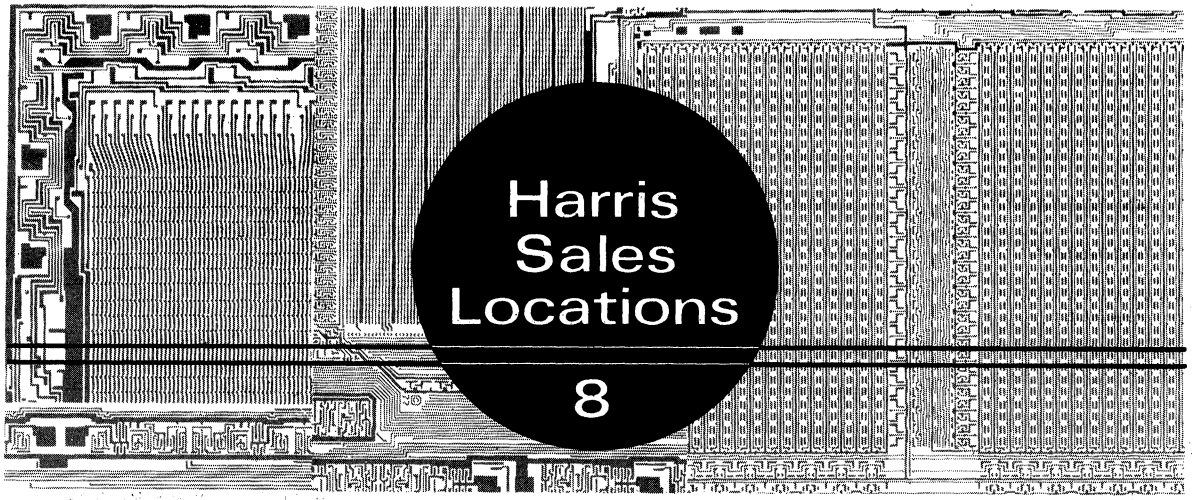

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