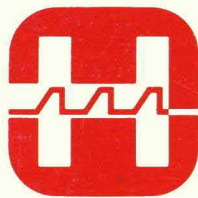


AUGUST 1975



HARRIS
SEMICONDUCTOR

A DIVISION OF HARRIS CORPORATION

INTEGRATED CIRCUITS

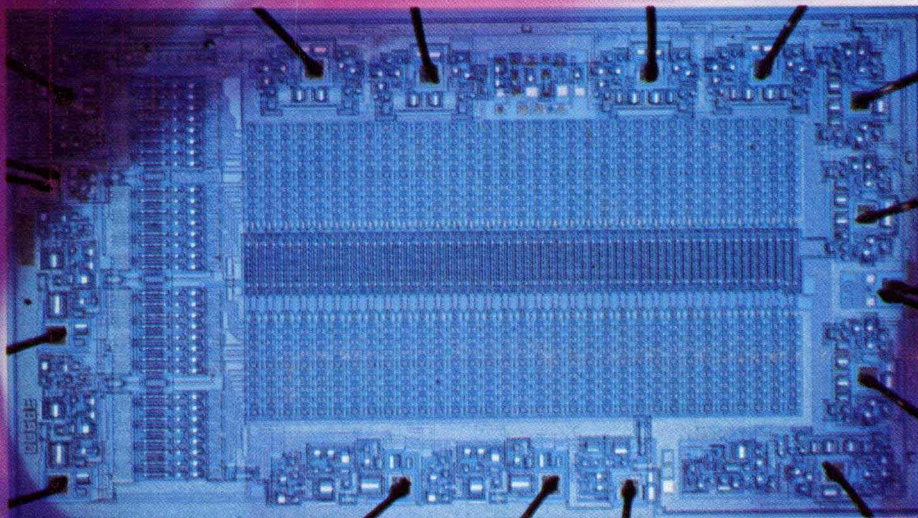
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INTEGRATED CIRCUITS DATA BOOK

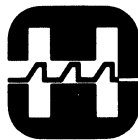
This DATA BOOK contains complete technical information on linear and memory integrated circuits presently available from Harris Semiconductor as standard products. A similar catalog dedicated to digital products specifies the complete line of Harris CMOS logic devices. By the use of the tear-out card provided in the back of this catalog, speciality information such as application notes, chip data sheets, and information about all new products introduced since publication of this catalog, are available directly through your local Harris sales office. They are also available from your nearest Harris representative or distributor.

For your convenience a complete index of Harris integrated circuits is provided in both an alpha-numeric sequence organized by major product categories such as linear and memory, and by a functional sequence. Although the alpha-numeric index tracks very closely with the organization of the data book, some exceptions do occur due to products combined on single data sheets. Warranting special attention for users of military product is the section on Harris Semiconductor's Dash 8 program. This section gives a complete description of processing used for 883 product available "off-the-shelf" from Harris. Complete physical dimensions of all packaging options are detailed in the section on package outlines. For ease of use, each major product section of this data book includes a complete industry cross reference index identifying industry cross reference numbers.

Harris is pleased that you would take this time to review our product line. We stand ready to support your production with world wide points of distribution. For your design convenience we offer a complete capability in applications assistance. Just call your local Harris office.

Thank you for thinking Harris.

AUGUST 1975



**HARRIS
SEMICONDUCTOR**

A DIVISION OF HARRIS CORPORATION

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Harris Semiconductor, Time-Life Building 2-3-6 Otemachi Chiyodaku, Tokyo, Japan

HARRIS SEMICONDUCTOR

HISTORY

A look at Harris Semiconductor is a look at one of the Semiconductor success stories of the past two decades. Originally a three man laboratory organized to develop proprietary and custom circuits, this small nucleus increased in size until by 1966 it was known throughout the industry as the Microelectronics Division (MED) of Radiation, Inc., a military systems house located in Melbourne, Florida. As MED, the division fostered high technology and was an industry leader in the manufacturing of hardened devices.

In many respects, the Division, as it is known today, was born in July 1967. It was then that the entire 320 acre Melbourne complex became part of Harris-Intertype Corporation. With a new corporate identity the semiconductor operation dedicated its proficiency in high technology to the development of a series of state-of-the-art devices aimed specifically at the industrial marketplace.

In September of 1970, the firm chose its present name of Harris Semiconductor, became an independent division reporting directly to corporate headquarters in Cleveland, Ohio, and was well entrenched as a leading supplier of sophisticated industrial ICs as well as of ICs used on major military and NASA programs.

The past few years has been a major growth in Harris Semiconductor's participation within the industrial IC marketplace. While continuing as a major supplier of military and DOD products, efforts to penetrate the industrial marketplace has grown to where industrial customers now constitute approximately 80 percent of the Division's total effort.

To support its present position within the industrial marketplace, Harris Semiconductor has developed highly refined national and international lines of distribution. Included is a network of OEM sales offices, technically proficient manufacturers' representatives, and a family of distributors consisting of leaders within the electronic industry.

The Division now provides multiple product and service outlets within each significant market location and has opened direct sales offices in both Brussels, Belgium and Tokyo, Japan. Each outlet, through the combined efforts of OEM, manufacturer's representatives, and distributors, offers a complete line of complimenting product, literature and applications support.

FOR THE FUTURE

Harris Semiconductor now occupies over 225,000 square feet of floor space in five modern buildings located on the corporation's 320 acre site in Palm Bay, Florida. These facilities are equipped to perform the entire scope of Harris Semiconductor's operations but are augmented by offshore assembly facilities. Each operational site is designed for expansion. A recently completed 8 million dollar expansion and refurbishment program resulted in three-inch wafer processing

across all product lines assuring customers with optimum in both pricing and delivery. Every effort is being made to guarantee that your association with Harris Semiconductor represents the finest in quality, reliability, delivery and price considerations.

TECHNOLOGY

Harris Semiconductor's significant contributions in process technology serve both the industrial and the military markets. In addition to pioneering the dielectric isolation process, Harris wields expertise in thin-film deposited on silicon dioxide, selective gold doping, buried n⁺ and p⁺ epitaxial layers, junction FETs, vertical npn and pnp transistors in the same monolithic structure, metallic aluminum bonding, multilevel interconnect processes, complementary MOS, junction isolated complementary MOS and p-channel MOS processes.

PRODUCTS

Harris produces a wide family line of devices embracing linear, digital and memory functions. Within the family of operational amplifiers, Harris has long offered state-of-the-art parameters without peer in monolithic circuitry. Now, this rapidly expanding linear line includes: phase locked loops, A/D and D/A encoders, and a rapidly expanding line of interface circuits. Harris is the largest single industry source of CMOS analog switches and multiplexers with a complete complement of alternate sources in addition to a strongly established proprietary line.

For the Digital world Harris Semiconductor is a leading supplier of standard logic CMOS. Nearly 100 devices are included to offer designers as comprehensive a CMOS logic selection as is available from industry. In addition to full alternate sourcing of the 54/74C family, product selection includes viable product from both the 4000 and 14500 families. Harris is actively pursuing JAN qualification of the entire CMOS product line. In the field of memories Harris pioneered and developed the concept of field programmable read only memories (PROM). Now available as a Harris exclusive is the complete family of "Generic" PROMs featuring a wide selection of organizations with identical programming requirements, input/output characteristics, fuse geometries and technology, as well as circuit configuration. The company is also aggressively pursuing development of a family of RAM products in both bipolar and MOS technology.

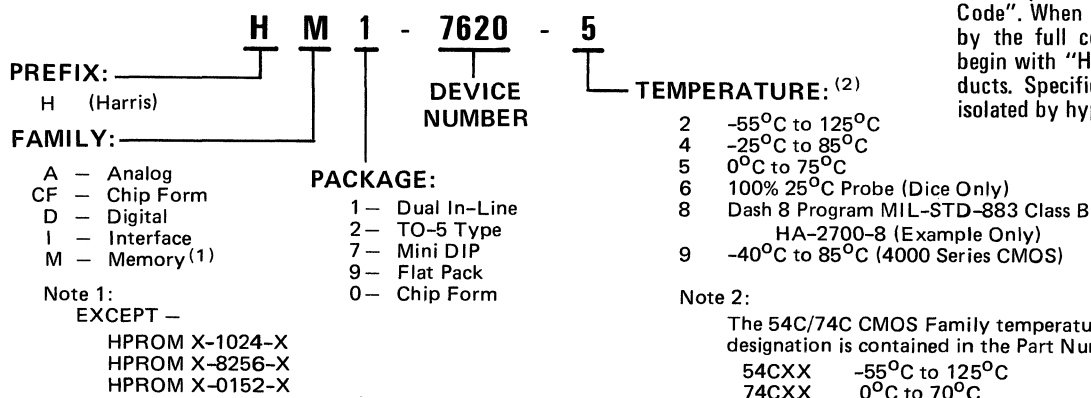
CHIP POLICY

Wherever practical the Harris product line is also made available in chip form. For further detail, contact either the Digital, Linear or Memory Product Marketing Managers respectively.

DASH 8 NOTICE

As a special service to users of high rel products Harris makes instantly available high reliability on many of our product lines. Simply by adding its postscript -8 to appropriate Harris part numbers "off the shelf" delivery can be obtained of product screened to MIL-STD-883 Method 5004 Class B. For details concerning this special Harris program for High Rel users, see the Dash 8 section of this catalog.

EXPLANATION OF HARRIS PRODUCT CODE



Harris products are designated by "Product Code". When ordering, please refer to products by the full code. Harris products will always begin with "H", except in the case of chip products. Specific device numbers will always be isolated by hyphens.

HARRIS ALPHA-NUMERIC INDEX

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MONOLITHIC DIODE MATRICES AND INTERFACE CIRCUITS

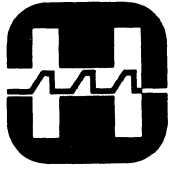
HD-234	Hex Interface Inverters	Me-3
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HARRIS
SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

TECHNICAL INFORMATION

DIGITAL DATA SHEETS

LINEAR DATA SHEETS

MEMORY DATA SHEETS

DASH 8

PACKAGING

LITERATURE GUIDE

DIGITAL DATA SHEETS

Harris is proud to be a fully qualified supplier of both the 4000 and 54/74C standard CMOS logic families. For that reason a special separate catalog has been prepared giving full technical descriptions of all CMOS devices. Included in the catalog is a cross reference guide identifying alternate sources both by manufacturer and by device function. Users of CMOS will decide for themselves the relative merits of competing logic families. The current trend is to mix the advantages of both. Regardless of choice, users of Harris CMOS will benefit from obtaining both their requirements from one supplier. Should you require use of a Harris CMOS catalog please complete the appropriate information on the Literature Request tear-out card found at the back of this catalog and return it to your nearest sales office for immediate action.

HD-54C/74* SERIES

MANUFACTURER CROSS REFERENCE

FUNCTION	HARRIS	NATIONAL	TELEDYNE
Quad 2 Input NAND	HD-74C00	MM74C00	MM74C00
Quad 2 Input NOR	HD-74C02	MM74C02	MM74C02
Hex Inverter	HD-74C04	MM74C04	MM74C04
Quad 2 Input AND	HD-74C08	MM74C08	MM74C08
Triple 3 Input NAND	HD-74C10	MM74C10	MM74C10
Hex Schmitt Trigger	HD-74C14	MM74C14	MM74C14
Dual 4 Input NAND	HD-74C20	MM74C20	MM74C20
8 Input NAND	HD-74C30	MM74C30	—
Quad 2 Input OR	HD-74C32	MM74C32	—
BCD to Decimal Decoder	HD-74C42	MM74C42	MM74C42
BCD to 7 Segment Decoder	HD-74C48	MM74C48	—
Dual J-K Flip-Flops with Clear	HD-74C73	MM74C73	MM74C73
Dual D Flip-Flop	HD-74C74	MM74C74	MM74C74
Dual J-K Flip-Flops with Clear and Preset	HD-74C76	MM74C76	MM74C76
4-Bit Binary Full Adder	HD-74C83	MM74C83	—
4-Bit Magnitude Comparator	HD-74C85	MM74C85	—
Quad 2 Input Exclusive OR	HD-74C86	MM74C86	—
64-Bit Three State Random Access Read/Write Memory	HD-74C89	MM74C89	—
4-Bit Right-Shift Left-Shift Register	HD-74C95	MM74C95	MM74C95
Dual J-K Flip-Flops with Clear	HD-74C107	MM74C107	MM74C107
8 Channel Digital Multiplexer	HD-74C151	MM74C151	MM74C151
4 Line to 16 Line Decoder/ Demultiplexer	HD-74C154	MM74C154	MM74C154
Quad 2 Input Multiplexers	HD-74C157	MM74C157	MM74C157
Decade Counter with Asynchronous Clear	HD-74C160	MM74C160	MM74C160
Binary Counter with Asynchronous Clear	HD-74C161	MM74C161	MM74C161
Decade Counter with Synchronous Clear	HD-74C162	MM74C162	MM74C162
Binary Counter with Synchronous Clear	HD-74C163	MM74C163	MM74C163
8-Bit Parallel Out Serial Shift Register	HD-74C164	MM74C164	MM74C164
Parallel Load 8 Bit Shift Register	HD-74C165	MM74C165	—

*All Listed 74C Devices Are Available Also As 54C

FUNCTION	HARRIS	NATIONAL	TELEDYNE
Three State Quad D Flip-Flop	HD-74C173	MM74C173	MM74C173
Hex D Flip-Flop	HD-74C174	MM74C174	—
Quad D Flip-Flop	HD-74C175	MM74C175	—
Synchronous 4-Bit Up/ Down Decade Counter	HD-74C192	MM74C192	MM74C192
Synchronous 4-Bit Up/ Down Binary Counter	HD-74C193	MM74C193	MM74C193
4-Bit Registers	HD-74C195	MM74C195	MM74C195
256-Bit Three State Random Access Read/Write Memory	HD-74C200	MM74C200	—
Dual Monostable Multivibrator	HD-74C221	MM74C221	—
Hex Inverting TTL Buffer	HD-74C901	MM74C901	—
Hex Non-Inverting TTL Buffer	HD-74C902	MM74C902	—
Hex Inverting PMOS Buffer	HD-74C903	MM74C903	—
Hex Non-Inverting PMOS Buffer	HD-74C904	MM74C904	—
Three State Hex Non-Inverting Buffer	HD-80C95**	MM80C95	—
Three State Hex Non-Inverting Buffer	HD-80C97**	MM80C97	—

* All Listed 74C Devices Are Also Available As 54C.

** All Listed 80C Devices Are Also Available As 70C.

HD-4000 SERIES

MANUFACTURER CROSS REFERENCE

FUNCTION	HARRIS	RCA	NATIONAL	MOTOROLA
Dual 3 Input NOR Gate + Inverter	HD-4000	CD4000	—	MC14000
Quad 2 Input NOR	HD-4001	CD4001	MM4601	MC14001
Dual 4 Input NOR	HD-4002	CD4002	MM4602	MC14002
18 Stage Static Shift Register	HD-4006	CD4006	MM4606	MC14006
Dual Complementary Pair + Inverter	HD-4007	CD4007	—	MC14007
4-Bit Full Adder	HD-4008	CD4008	—	MC14008
Quad 2 Input NAND	HD-4011	CD4011	MM4611	MC14011
Dual 4 Input NAND	HD-4012	CD4012	MM4612	MC14012
Dual D Flip-Flop	HD-4013	CD4013	MM4613	MC14013
8 Stage Static Shift Register	HD-4014	CD4014	MM4614	MC14014
Dual 4 Static Shift Register	HD-4015	CD4015	—	MC14015
Decade Counter	HD-4017	CD4017	MM4617	MC14017
Preset/Divide by N Counter	HD-4018	CD4018	—	—
Quad AND/OR Select	HD-4019	CD4019	MM4619	—
14 Stage Binary/Ripple Counter	HD-4020	CD4020	MM4620	MC14020
8 Stage Static Shift Register	HD-4021	CD4021	MM4621	MC14021
Divide by 8 Counter	HD-4022	CD4022	MM4622	MC14022
Triple 3 Input NAND	HD-4023	CD4023	MM4623	MC14023
7 Stage Binary Counter	HD-4024	CD4024	—	MC14024
Triple 3 Input NOR	HD-4025	CD4025	MM4625	MC14025
Dual J=K Flip-Flop	HD-4027	CD4027	MM4627	MC14027
BCD/Decimal Decoder	HD-4028	CD4028	—	MC14028
Preset Up-Down Counter	HD-4029	CD4029	—	—
Quad Exclusive OR	HD-4030	CD4030	MM4630	—
4 Stage Parallel In/Parallel Out Shift Register	HD-4035	CD4035	MM4635	MC14035
12 Stage Binary/Ripple Counter	HD-4040	CD4040	—	MC14040
Quad Clocked "D" Latch	HD-4042	CD4042	—	MC14042
Quad Three State R/S Latch NOR	HD-4043	CD4043	—	—
Quad Three State NAND R/S Latch	HD-4044	CD4044	—	—
Hex Buffer, Inverting	HD-4049	CD4049	MM4649	MC14049
Hex Buffer, Non-Inverting	HD-4050	CD4050	MM4650	MC14050
Quad Bilateral Switch	HD-4066	CD4066	MM4666	MC14066

DIGITAL
CMOS

FUNCTIONAL CROSS REFERENCE OF HD-4000 SERIES AND HD-54C/74C SERIES

ARITHMETIC FUNCTIONS	4000 SERIES	54C/74C* SERIES
Four-Bit Binary Full Adder	HD-4008	HD-74C83
Four-Bit Magnitude Comparator	—	HD-74C85
COUNTERS		
7 Stage Binary	HD-4024	—
12 Stage Ripple-Carry Binary	HD-4040	—
14 Stage Ripple-Carry Binary	HD-4020	—
Decade Counter/ Divider		
+10 Decoded Decimal Outputs	HD-4017	—
Divide by 8 Counter/Divider		
with 8 Decimal Outputs	HD-4022	—
Presetable Divide by "N"		
Counter Fixed or Programmable	HD-4018	—
Presetable Up/Down Counter		
Binary or BCD Decade	HD-4029	—
Synchronous Decade	—	HD-74C160
Synchronous Binary	—	HD-74C161
Fully Synchronous Decade	—	HD-74C162
Fully Synchronous Binary	—	HD-74C163
Synchronous Up/Down Decade	CD40192 (RCA)**	HD-74C192
Synchronous Up/Down Binary	CD40193 (RCA)**	HD-74C193
DECODERS/MULTIPLEXERS		
Quad Bilateral Switch	HD-4066	—
BCD to Decimal Decoders	HD-4028	HD-74C42
BCD to 7 Segment Decoder	—	HD-74C48
8 Channel Digital Multiplexer	—	HD-74C151
4 Line to 16 Line	—	HD-74C154
Quad 2 Input	—	HD-74C157
FLIP-FLOPS		
Dual "D" with Set/Reset	HD-4013	HD-74C74
Dual "J-K" with Set/Reset	HD-4027	—
Quad Clocked "D" Latch	HD-4042	—
Quad Three State NOR Reset/Set Latch	HD-4043	—
Quad Three State NAND Rest/Set Latch	HD-4044	—
Dual "J-K" Master/Slave	—	HD-74C73
Dual "J-K" Master/Slave with Preset	—	HD-74C76
Dual "J-K"	—	HD-74C107
Quad "D" Three State (Quad Latch)	CD4076 (RCA)**	HD-74C173
Hex "D"	—	HD-74C174
Quad "D"	—	HD-74C175

*All Listed 74C Devices Are Available Also As 54C.

**Pin Compatible with 54C/74C.

GATES/BUFFERS/INVERTERS

Dual 3 Input NOR Gate + Inverter	HD-4000	—
Quad 2 Input NOR	HD-4001	HD-74C02
Dual 4 Input NOR	HD-4002	—
Quad 2 Input NAND	HD-4011	HD-74C00
Dual 4 Input NAND	HD-4012	HD-74C20
Triple 3 Input NAND	HD-4023	HD-74C10
Triple3 Input NOR	HD-4025	—
Hex Inverter	CD4069 (RCA)**	HD-74C04
Quad 2 Input AND	—	HD-74C08
8 Inputs NAND	—	HD-74C30
Quad 2 Input OR	—	HD-74C32
Quad 2 Input Exclusive OR	HD-4030 MC14507 (MOTO)**	HD-74C86
Quad AND-OR Select	HD-4019	—
Dual Complementary Pair + Inverter	HD-4007	—
Hex Buffer/Converter, Inverting	HD-4049	HD-74C901
Hex Buffer/Converter, Non-Inverting	HD-4050	HD-74C902
Hex Inverting PMOS Buffer	—	HD-74C903
Hex Non-Inverting PMOS Buffer	—	HD-74C904
Three State Hex Buffer	—	HD-80C95***
Three State Hex Buffer	—	HD-80C97***

SHIFT REGISTERS

18 Stage Static Shift Register	HD-4006	—
Dual 4 Stage with Serial Input/ Parallel Output	HD-4015	—
8 Stage Synchronous Parallel Input/ Serial Output	HD-4014	HD-74C165
8 Stage Asynchronous Parallel Input/ Serial Output	HD-4021	—
4 Stage with J- \bar{K} Input and True/ Complement Output	HD-4035	—
4-Bit Right-Shift Left-Shift	—	HD-74C95
8-Bit Serial-In Parallel Out	—	HD-74C164
4-Bit Parallel-In Parallel-Out	—	HD-74C195

SPECIAL FUNCTIONS

Hex Schmitt Trigger	CD40106 (RCA)** MC14584 (MOTO)**	HD-74C14
Dual Monostable Multivibrator	—	HD-74C221
64-Bit Three State Random Access Read/Write Memory	—	HD-74C89
256-Bit Three State Random Access Read/Write Memory	—	HD-74C200

*All Listed 74C Devices Are Also Available As 54C.

***All Listed 80C Devices Are Available Also As 70C.

**Pin Compatible with 54C/74C.

LINEAR DATA SHEETS

The Harris family of analog devices ... a select line of linears featuring state-of-the-art performance and monolithic reliability at realistic prices.

Harris Semiconductor has long been synonymous with high performance state-of-the-art linear intergrated circuits. And, indeed, wherever monolithic performance is measured in terms of slew rate, bandwidth, and power consumption, Harris operational amplifiers still represent the leading edge of monolithic technology.

Linears from the Harris family can also lower your instrumentation systems costs substantially, improve performance, lower parts count, reduce design time, and increase system reliability. In the past, the speed and accuracy of most of these linears could only be approached with discrete devices, hybrids, or modules.

Excellent applications for Harris linears include: data acquisition, test equipment, telemetry, medical instruments, and process control.

Harris is now the industry's leading manufacturer of CMOS analog switches and multiplexers featuring devices both with and without built-in overvoltage protection. All Harris switches and multiplexers utilize a special process that completely eliminates latchup while greatly reducing chances of channel interaction.

Technical advantage and volume production are both backed up by immediate nation wide applications support. When you think linears ... think Harris.

LINEAR ALPHA-NUMERICAL INDEX

PAGE	ITEM	
Li-3	Military Operational Amplifiers Guide	
Li-4	Commercial/Industrial Operational Amplifiers Guide	
Li-5	Selection Guide	
Li-6	Cross-Reference	
Li-11	HA-909/911	Operational Amplifiers
Li-15	HA-2000/2005/2000A/2005A	F.E.T. Input Preamplifier
Li-19	HA-2050/2055/2050A/2055A	High Slew Rate F.E.T. Input Operational Amplifiers
Li-23	HA-2060/2065/2060A/2065A	Wide Band F.E.T. Input Operational Amplifier
Li-27	HA-2111/2211	Voltage Comparators
Li-31	HA-2311	Voltage Comparator
Li-35	HA-2400/2404/2405	PRAM Four Channel Programmable Amplifier
Li-39	HA-2420/2425	Sample and Hold Gated Operational Amplifier
Li-43	HA-2500/2502/2505	High Slew Rate Operational Amplifiers
Li-47	HA-2510/2512/2515	High Slew Rate Operational Amplifiers
Li-51	HA-2520/2522/2525	High Slew Rate Operational Amplifiers
Li-55	HA-2530/2535	High Slew Rate, Wideband Inverting Amplifier
Li-59	HA-2600/2602/2605	High Impedance Operational Amplifier
Li-63	HA-2620/2622/2625	Wide Band, High Impedance Operational Amplifiers
Li-67	HA-2630/2635	High Performance Current Booster
Li-71	HA-2640/2645	High Voltage Operational Amplifier
Li-75	HA-2650/2655	Dual High Performance Operational Amplifier
Li-79	HA-2700/2704/2705	High Performance Operational Amplifiers
Li-83	HA-2720/2725	Wide Range Programmable Operational Amplifier
Li-89	HA-2730/2735	Wide Range Dual Programmable Operational Amplifier
Li-95	HA-2820/2825	Phase Locked Loop
Li-99	HA-2900/2904/2905	Chopper Stabilized Operational Amplifier
Li-103	HD-0165	Keyboard Encoder
Li-107	HD-245/545	Triple Line Transmitter
Li-107	HD-246/546/249/549	Triple Line Receivers
Li-107	HD-248/548	Triple Party Line Receiver
Li-111	HD-1488	Quad Line Driver
Li-115	HD-1489	Quad Line Receiver
Li-115	HD-1489A	Quad Line Receiver
Li-117	HI-200	Dual SPST CMOS Analog Switch
Li-123	HI-201	Quad SPST CMOS Analog Switch
Li-129	HI-506A/507A	16 Channel Analog Multiplexer with Overvoltage Protection
Li-135	HI-508A/509A	8 Channel Analog Multiplexers with Overvoltage Protection
Li-141	HI-1080/1085	8-Bit D to A Converter High Speed Monolithic
Li-145	HI-1800A	Analog Switch Four-Channel
Li-149	HI-1818A/1828A	8 Channel Analog Multiplexers
Li-153	HI-5040 – 5051	CMOS Analog Switches
Li-153	HI-5046A/5047A	CMOS Analog Switches

HARRIS OPERATIONAL AMPLIFIERS

Selection Guide

for Commercial/Industrial Applications

PARAMETER †	0°C to +75°C													UNITS
	HA-911	F.E.T. PREAMP			HA-2055	HA-2055A	HA-2065	HA-2065A	PRAM™	S/H	HA-2505	HA-2515	HA-2525	
INPUT CHARACTERISTICS														
Offset Voltage	7.5	55	12	65	17	65	15	11	8	10	14	14	5	mV
Drift (Typ.)	15	60	40	60	40	60	40	30	5	20	30	20	5	μV/°C
Bias Current	750	1	1	1	1	1	1	500	400	500	500	500	200	nA
Offset Current	450	.5	.5	.5	.5	.5	.5	100	100	100	100	100	20	nA
Common Mode Range	±12	±10	±10	±10	±10	±10	±10	±10	±10	±10	±10	±10	±10	V
INPUT NOISE (3)														μVRMS
TRANSFER CHARACTERISTICS														
Large Signal Voltage Gain	15K	.98	.98	5K	5K	70K	70K	25K	25K	10K	5K	5K	100K	V/V
Common Mode Rejection Ratio	74	70	70	70	70	70	70	74	74	74	74	74	80	dB
Bandwidth (Typ.)	7	10(3)	10(3)	20(3)	20(3)	24(3)	24(3)	18(3)	2(3)	12(3)	12(3)	25	20	MHz
OUTPUT CHARACTERISTICS														
Output Voltage Swing	±11	±10	±10	±10	±10	±10	±10	±10	±10	±10	±10	±10	±10	V
Output Current (1)	±15	±5	±5	±10(1)	±10(1)	±10(1)	±10(1)	20(3)	±10	±10	±10	±10	±25	mA
Full Power Bandwidth (Typ.)(1)	35	1,000(3)	1,000(3)	2,000(3)	2,000(3)	600(3)	600(3)	200(3)	70(3)	500	1,000	1,500	5,000	kHz
TRANSIENT RESPONSE														
Rise Time (1)	75	50(3)	50(3)	50(3)	50(3)	50(3)	50(3)	20	100(3)	50	50	50	40	ns
Overshoot (1)	40	5(3)	5(3)	25(3)	25(3)	25(3)	25(3)	25	20(3)	50	50	50	50	%
Slew Rate (1)	±2.3	100(3)	100(3)	120(3)	120(3)	35(3)	35(3)	15	5(3)	±20	±40	±80	±250	V/μs
Settling Time (Typ.) (1)	(2)	0.4(3)	0.4(3)	(3) 0.4	0.4(3)	.8(3)	.8(3)	1.5		0.33	0.25	0.20	.5	μs
POWER SUPPLY CHARACTERISTICS														
Supply Current (1)	2.5	1.7	1.7	8.0	8.0	6.0	6.0	6.0	5.0	6.0	6.0	6.0	6	mA
Power Supply Rejection Ratio	74	70	70	70	70	70	70	74	74	74	74	74	80	dB
FUNCTIONAL CHARACTERISTICS														
Offset Adjust	No	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes	No	
Compensation Components	0	0	0	0 AV>3	0 AV>5	0 AV>5	0 AV>5	0 AV>10	0	0	0	0 AV>3	1	
Output Protection	No	No	No	No	No	Yes	Yes	No	Yes	No	No	No	No	

PARAMETER †	0°C to +75°C									-25°C to +85°C			UNITS
	HA-2605	HA-2625	HA-2635	HA-2645	HA-2655	HA-2705	HA-2725	HA-2735	HA-2905	PRAM™	HA-2704	HA-2904	
INPUT CHARACTERISTICS													
Offset Voltage	7	7	300	7	7	7	7	7	.08	7	6	.05	mV
Drift (Typ.)	5	5	(2)	15	8	5	8 to 10	8 to 10	.2	20	5	.2	μV/°C
Bias Current	40	40	200	50	300	70	10 to 40	10 to 40	1	400	50	1	nA
Offset Current	40	40	(2)	50	100	40	7.5 to 20	7.5 to 20	.5	100	30	.5	nA
Common Mode Range	±11	±11	(2)	±35(4)	±13	±11	±10	±10	±10	±10	±11	±10	V
INPUT NOISE (3)													
TRANSFER CHARACTERISTICS													
Large Signal Voltage Gain	70K	70K	.85	75K	15K	100K	20K	20K	10 ⁶	25K	100K	10 ⁷	V/V
Common Mode Rejection Ratio	74	74	(2)	74	74	80	74	74	120	80	86	130	dB
Bandwidth (Typ.) (1)	12	35	8	4	8	1	.01 to 10	.01 to 10	3	16(3)	1	3	MHz
OUTPUT CHARACTERISTICS													
Output Voltage Swing	±10	±10	±10	±35(4)	±13	±11	±13.5(3)	±13.5(3)	±10	±10	±11	±10	V
Output Current (1)	±10	±10	±300	±10	18(3)	±22(3)	.5 to 5.0(3)	.5 to 5.0(3)	±7	20(1)	±22(3)	±10	mA
Full Power Bandwidth (typ.)	75	600	8,000	23	30	50	1.5 to 80(3)	1.5 to 80	40	500(3)	50	40	kHz
TRANSIENT RESPONSE													
Rise Time (1)	60	45	30(3)	60(3)	40(3)	(2)	200 to 2,000(3)	200	200(3)	20(3)	(2)	200(3)	ns
Overshoot (1)	40	(2)	25(3)	15(3)	15(3)	(2)	5 to 15(3)	5 to 15(3)	20(3)	25(3)	(2)	20(3)	%
Slew Rate (1)	±4	±20	200	5(3)	2	±10	.1 to .8(3)	.1 to .8	2.5(3)	50	10	2.5(3)	V/μs
Settling Time (Typ.) (1)	1.5	0.30	.5(3)	1.5(3)	1.5(3)	5.0	(2)	(2)	(2)	1.5(3)	5.0	(2)	μs
POWER SUPPLY CHARACTERISTICS													
Supply Current (1)	4.0	4.0	23	4.5	4	0.150	.02 to .2	.02 to .2	5	6.0(1)	0.150	5	mA
Power Supply Rejection Ratio	74	74	66	74	74	80	76	76	120	80	86	130	dB
FUNCTIONAL CHARACTERISTICS													
Offset Adjust	Yes	Yes	No	Yes	Dip Pkg. Only	Yes	Yes	Yes	No	No	Yes	No	
Compensation Components	0	0(AV≥5)	0	0	0	0	0	0	3	0 AV>10	0	3	
Output Protection	Yes	Yes	External	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	

- (1) At +25°C (3) Typical (5) Dependent upon Iset value
(2) Not applicable or not specified (4) V supply = ±40V

* TO-86 only

† Guaranteed for ±15V supplies and applicable temperature range unless otherwise specified

SELECTION GUIDE

Interface Circuits

COMPARATORS

PARAMETER +	-55°C to +125°C HA - 2111	-25°C to +85°C HA - 2211	0°C to +75°C HA - 2311	UNITS
Offset Voltage	4	4	10	mV
Bias Current	150	150	300	nA
Offset Current	20	20	70	nA
Response Time (TYP)	200	200	200	nS
Output Current (+25°C)	50	50	50	mA
Supply Current (1)	6	6	7.5	mA

DIGITAL TO ANALOG CONVERTERS

	HI - 1080	HI - 1085	
Resolution	8	8	Bits
Absolute Accuracy	1	1	L.S.B.
Full Scale Output	-5, +5, ±5	-5, +5, ±5	Volts
Settling Time (TYP)	1.5	1.5	μS
Inputs	TTL	TTL	

PHASE LOCKED LOOPS

	HA - 2820	HA - 2825	
Frequency Range	0-3	0-3	MHz
Tracking Range (Typ)	±25	±25	Percent of fo
Drift of fo (TYP)	100	100	PPM/°C

+ Guaranteed for Applicable Temperature range, unless otherwise specified

(1) At +25°C

PRAM PROGRAMMABLE AMPLIFIER

HA - 2400/2404/2405

One of four op amp input stages may be digitally selected to be connected to a single output. Replaces 5 op amps and a four channel multiplexer to obtain programmable gain, signal selection or countless other functions.

SAMPLE - AND - HOLD/GATED OP AMP

HA - 2420/2425

Replaces two high performance op amps and a digitally controlled analog switch to form a high accuracy, versatile sample - and - hold, or a switchable op amp.

CURRENT BOOSTER AMPLIFIER

HA - 2630/2635

A unity gain amplifier with output current up to ±400 mA, and 600V/μS slew rate, designed for use in series with any op amp output. For Coax line drivers, servo amps, audio amps, clock drivers, etc.

DIGITAL LINE DRIVERS/RECEIVERS

HD - 245/246/248/249 (-55°C to +125°C)

HD - 545/546/548/549 (0°C to + 75°C)

Triple - balanced line - current mode drivers/receivers with party line capability for high speed (to 15 MHz) or long distance (to 3,000 feet) with superior noise immunity.

HD - 1488/1489/1489A

Industry standard quad drivers/receivers for E.I.A. spec. RS - 232C interfaces.

KEYBOARD ENCODER

HD - 0165

Universal 16 key inputs, 4 parallel outputs with strobe and Key rollover output.

LINEAR

CROSS-REFERENCE

Linear and Interface Devices

MANUFACTURER	PART NUMBER	HARRIS EQUIVALENT	NOTES
Advanced Micro Devices	AM111/211/311	HA-2111/2211/2311	A1
	AM118/318	HA-2510/2515	B2
	AM715	HA-2520/2525	B2
	AM1660	HA-2500/2505	B2
		HA-2600/2605	B2
		HA-2700/2705	B2
	AM1488	HD-1488	A1
	AM1489	HD-1489	A1
	AM1489A	HD-1489A	A1
	AM9616	HD-1488	C2
	AM9617	HD-1489A	C2
Analog Devices	AD505	HA-2530/2535	C2
	AD507J*	HA-2625	A1
	AD507S	HA-2620	A1
	AD509J*	HA-2525	A1
	AD509S	HA-2520	A1
	AD518	HA-2510/2515	B2
	AD7501	HI-1818A	B2
	AD7502	HI-1828A	B2
	AD7503	HI-1818A	B2
	AD7506	HI-506	A1
	AD7507	HI-507	A1
	AD7510	HI-201	C2
	AD7511	HI-201	C2
	AD7512	HI-5043	C2
	AD7513	HI-200	A1
	Burr Brown	3500A	HA-2605
3500R		HA-2600	B2
3505J		HA-2505	A1
3506J		HA-2605	A1
3507J		HA-2525	A1
3508J		HA-2625	A1
3550J		HA-2055	B2
3550K		HA-2050	B2
3550S		HA-2055	B2
MPCBD		HI1-507A-5	A1
MPC16S		HI1-506A-5	A1
Datel	AM-405-2	HA2-2055-5	A1
	AM-406-2	HA2-2065-5	A1
	AM-452-2	HA2-2525-5	A1
	AM-462-1	HA1-2625-5	A1
	AM-462-2	HA2-2625-5	A1
	SHM-1C-1	HA-2425	A1
Exar	XR215	HA-2820/2825	C3
	XR1488	HD-1488	A1
	XR1489A	HD-1489A	A1

* "K" equivalent is either military device or selected commercial device

NOTES: A. Pin-for-pin replacement

B. Minor pin-out difference (offset adj., compensation, etc.)

C. Not pin compatible — consult data sheets.

1. Identical electrical specifications

2. Harris part superior in most parameters

3. Parameter tradeoffs — consult data sheets

LINEAR

MANUFACTURER	PART NUMBER	HARRIS EQUIVALENT	NOTES
Fairchild Semiconductor	μ A702	HA-2620/2625	C2
	μ A709	HA-909/911	B2
	μ A715	HA-2520/2525	B2
	μ A725	HA-2700/2705	A3
	μ A727	HA-2900/2905	C2
	μ A734	HA-2111/2311	C2
	μ A740	HA-2060/2065	B2
	μ A741	HA-909/911, 2600/2605 2700/2705 2640/2645	B2 B2 A2
	μ A747	HA-2650/2655	C2
	μ A748	HA-2620/2625	B2
	μ A772	HA-2510/2515	A2
	μ A776	HA-2720/2725	A2
	μ A791	HA-2630/2635	C2
	SH3002	HI-1800A	C2
	1558/1458	HA-2650/2655	A2
	9616	HD-1488	C2
	9617	HD-1489/A	C2
	Intersil	111/211/311	HA-2111/2211/2311
IH5040*		HI-5040	A1
thru		thru	
IH-5051		HI-5051	
8007		HA-2060/2065	B2
8008		HA-2600/2605	B2
8017		HA-2520/2525	B2
IH5110/5111		HA-2420/2425	C2
IH5060		HI-506A	A2
IH5070		HI-507A	A2
* Part Numbers: Intersil	IH5040MDE		
	Harris	HI1-5040-2	
Intronics	FA-550	HA-2055	A1
	FA-551	HA-2065	A1
	A-560	HA-2525	A1
	A-561	HA-2625	A1
	A-570	HA-2535	A1
	CA-580	HA-2905	A1
Motorola	MC1508/1408	HI-1080/1085	C2
	MC1520/1420	HA-2600/2605	C2
	MC1530/1531/1430/1431	HA-2600/2605	C2
	MC1533/1433	HA-2700/2705	C2
	MC1536/1436	HA-2640/2645	A2
	MC1538/1438	HA-2630/2635	C2
	MC1539/1439	HA-2620/2625	B2

- NOTES:
- A. Pin-for-pin replacement
 - B. Minor pin-out difference (offset adj., compensation, etc.)
 - C. Not pin compatible — consult data sheets.
 - 1. Identical electrical specifications
 - 2. Harris part superior in most parameters
 - 3. Parameter tradeoffs — consult data sheets

MANUFACTURER	PART NUMBER	HARRIS EQUIVALENT	NOTES
Motorola (continued)	MC1545/1445	HA-2400/2405	C3
	MC1554/1454	HA-2630/2635	C3
	MC1556/1456	HA-2600/2605	B2
	MC1558/1458	HA-2650/2655	A2
	MC1582L	HD-245	C2
	MC1583L	HD-246	C2
	MC1584L	HD-249	C2
	MC1488L	HD-1488	A1
	MC1489L	HD-1489	A1
	MC1489AL	HD-1489A	A1
National Semiconductor	LH0001	HA-2700	C2
	LH0002	HA-2630	C2
	LH0003	HA-2520	C2
	LH0004	HA-2640	C2
	LH0005	HA-2620	C2
	LH0022/42/52	HA-2060/2065	B2
	LH0023/43	HA-2420/2425	C2
	LH0024	HA-2530/2535	B2
	LH0032	HA-2050/2055	C3
	LH0033/63	HA-2630/2635	C3
	LH0062	HA-2050/2055	B2
	LM101/301/107/307	HA-909/911, 2600/2605, 2700/ 2705	B2
	LM102/302	HA-2600/2605	B2
	LM108/208/308	HA-2700/2704/2705	B3
	LM110/310	HA-2500/2505	B2
	LM111/211/311	HA-2111/2211/2311	A1
	LM112/212/312	HA-2700/2704/2705	B3
	LM216/316	HA-2060/2065	B3
	LM118/318	HA-2510/2515	B2
	LM143/343	HA-2640/2645	A2
LM163/363	HD-248/548	C3	
LM1488	HD-1488	A1	
LM1489/A	HD-1489/A	A1	
Precision Monolithics	OP-01	HA-2600/2605/2500/2505	B2
	OP-05/07	HA-2900/2905	B2
	CMP-01/02	HA-2111/2311	B3
	SSS1558/1458	HA-2650/2655	A2
	DAC-02/04/100	HI-1080/1085	C3
RCA	111/211/311	HA-2111/2211/2311	A1
	CA3020	HA-2630/2635	C2
	CA3078	HA-2720/2730	B2
	CA3100	HA-2520/2525	B2
	CA3130	HA-2060/2065	B2
	CA3558/3458	HA-2650/2655	A2
	CA6078	HA-2720/2730	B2
	CD4016	HI-201	C2
	CD4046	HA-2820/2825	C2

NOTES: A. Pin-for-pin replacement
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 C. Not pin compatible — consult data sheets.

1. Identical electrical specifications
 2. Harris part superior in most parameters
 3. Parameter tradeoffs — consult data sheets

MANUFACTURER	PART NUMBER	HARRIS EQUIVALENT	NOTES	
Raytheon	RM/RC1556A	HA-2600/2605	B2	
	RM/RC4131	HA-2600/2605	B2	
	RM/RC4132	HA-2700/2705	B2	
	RM/RC4531	HA-2500/2505	B2	
	RM/RC4558	HA-2650/2655	A2	
	111/211/311	HA-2111/2211/2311	A1	
	1488 1489/1489A	HD-1488 HA-1489/1489A	A1 A1	
Signetics	531	HA-2510/2515	B2	
	536	HA-2060/2065	B2	
	560	HA-2820/2825	C2	
	561	HA-2820/2825	C2	
	562	HA-2820/2825	C2	
	565	HA-2820/2825	C2	
	5556	HA-2600/2605	B2	
	5558	HA-2650/2655	A2	
Silicon General	SG741S	HA-2500	B2	
	SG741SG	HA-2505	B2	
Siliconix	DG181*	HI-5048	C2	
	DG184	HI-5049	A2	
	DG185	HI-5045	A2	
	DG187	HI-5050	C2	
	DG188	HI-5042	C2	
	DG190	HI-5051	A2	
	DG191	HI-5043	A2	
	DG200	HI-200	A2	
	DG201	HI-201	A2	
	DG506	HI-506	A1	
	DG507	HI-507	A1	
	DG508	HI-508A	A3	
	DG509	HI-509A	A3	
	L120	HA-2060/2065	B2	
	L140	HA-2720/2725	B2	
	* Part Numbers: Siliconix		<p style="margin-left: 40px;"> A = -2 B = -5 A = HI2 K = HI1 P = HI1 R = HI1 </p> <p>DG200AA</p>	
	Harris			HI2-200-2

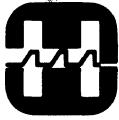
NOTES: A. Pin-for-pin replacement
 B. Minor pin-out difference (offset adj., compensation, etc.)
 C. Not pin compatible — consult data sheets.

1. Identical electrical specifications
 2. Harris part superior in most parameters
 3. Parameter tradeoffs — consult data sheets

MANUFACTURER	PART NUMBER	HARRIS EQUIVALENT	NOTES
Solitron	CM4016A	HI-201	C2
	μ c4000/4001/4002	HA-2600	C2
	μ c4000C/4001C/4002C	HA-2605	C2
	μ c4250	HA-2720	A2
	μ c4250c	HA-2725	A2
Sprague	μ LS/ μ LN2139	HA-2600/2605	B2
	μ LS/ μ LN2151	HA-2600/2605	B2
	μ LS/ μ LN2156	HA-2600/2605	B2
	μ LS/ μ LN2157	HA-2650/2655	B2
	μ LS/ μ LN2158	HA-2620/2625	B2
	μ LS/ μ LN2171	HA-2600/2605	B2
	μ LS/ μ LN2172	HA-2620/2625	B2
	μ LS/ μ LN2173	HA-2600/2605	B2
	μ LS/ μ LN2174	HA-2620/2625	B2
	μ LS/ μ LN2175	HA-2600/2605	B2
	μ LS/ μ LN2176	HA-2620/2625	B2
	μ LS/ μ LN2177	HA-2060/2065	B2
	μ LS/ μ LN2178	HA-2060/2065	B2
	Teledyne Philbrick	1321	HA-2625
1322		HA-2525	A1
1323		HA-2705	A1
1324		HA-2505	B2
1422		HA-2055/2065	B2
1427		HA-2065	C2
1431		HA-2065A	A1
143101		HA-2060A	A1
Texas Instruments	51/72L022	HA-2730/2735	B2
	52/72088	HA-2904/2905	C2
	52/72310	HA-2500/2505	B2
	52111/72311	HA-2111/2311	A1
	52/72558	HA-2650/2655	A2
	52/72660	HA-2700/2705	B2
	52/72770	HA-2600/2605	B2
	52/72771	HA-2620/2625	B2
	75107A/108A	HD-549	C2
	75109/110	HD-545	C2
	75150	HD-1488	C2
	75152	HD-1489/A	C2
	75154	HD-1489/A	C2
Transitron	TOA7709	HA-2600	B2
	TOA8709	HA-2605	B2
	TOA7809	HA-2060A	B2
	TOA8809	HA-2065A	B2

NOTES: A. Pin-for-pin replacement
 B. Minor pin-out difference (offset adj., compensation, etc.)
 C. Not pin compatible — consult data sheets.

1. Identical electrical specifications
 2. Harris part superior in most parameters
 3. Parameter tradeoffs — consult data sheets



HARRIS
SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-909/911

Operational Amplifiers

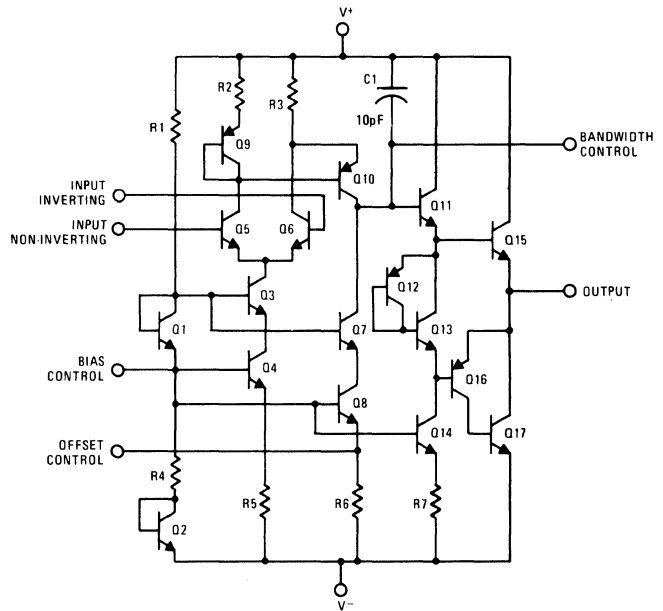
GENERAL DESCRIPTION

The integrated circuit covered by this data sheet forms a part of Harris' family of linear circuits intended for use as universal building blocks for analog circuitry. This Low Noise Operational Amplifier provides the 6dB per octave high frequency roll-off required for unconditional stability in operational feedback connections without the use of external compensation networks.

Simple resistive trim adjustment for zeroing input offset voltage is provided on the TO-86 package. The circuit is comprised of vertical NPN and PNP transistors in separate dielectrically isolated islands using advanced isolation techniques. These advanced production processes give the designer access to high performance integrated circuits without the technical compromises necessary with conventional junction isolation and lateral PNP fabrication methods.

The circuit is designed to meet or exceed the mechanical and environmental requirements of MIL-STD-883.

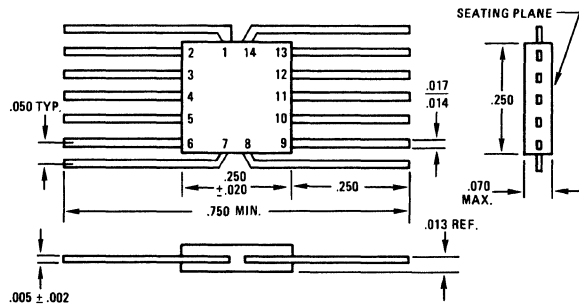
SCHEMATIC



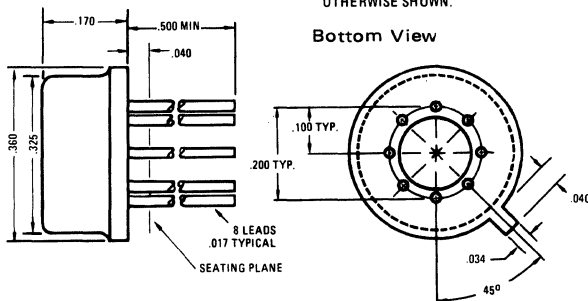
LINEAR

PACKAGES

CODE 9V TO-86 (METAL BOTTOM)

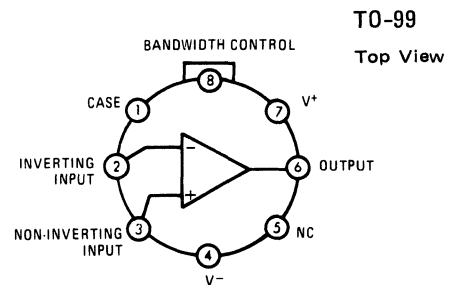
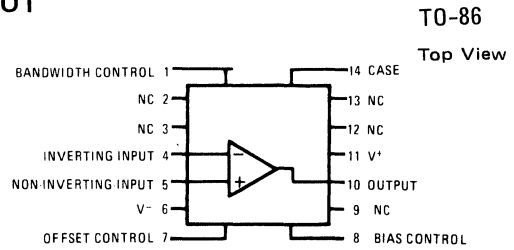


CODE 2A



ALL DIMENSIONS ARE IN INCHES.
ALL DIMENSIONS ± .010 UNLESS OTHERWISE SHOWN.

PIN OUT



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V ⁺ and V ⁻ Terminals	50.0V
Differential Input Voltage	±7.0V
Peak Output Current	±50mA
Internal Power Dissipation (Note 10)	300mW
Operating Temperature Range – HA-909	-55°C ≤ T _A ≤ +125°C
HA-911	0°C ≤ T _A ≤ +75°C
Storage Temperature Range	-65°C ≤ T _A ≤ +150°C

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: V_{Supply} = ±15.0V unless otherwise specified.

PARAMETER	TEMPERATURE	HA-909 -55°C to +125°C			HA-911 0°C to +75°C			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
INPUT CHARACTERISTICS								
* Offset Voltage	+25°C Full		2.0	5.0 6.0		2.0	6.0 7.5	mV mV
Equivalent Input Noise (Note 9)			1.0	5.0		1.0		μV
* Bias Current	+25°C Full		87	300 750		200 300	500 750	nA nA
* Offset Current	+25°C Full		25 50	150 300		100 150	300 450	nA nA
Offset Current Average Drift	Full		1.0			1.0		nA/°C
Input Resistance	+25°C Full	200 100	600 300		100	250		KΩ KΩ
Common Mode Range	Full	±12.0			±12.0			V
TRANSFER CHARACTERISTICS								
* Large Signal Voltage Gain (Notes 1, 4)	+25°C Full	25K 25K	45K 45K		20K 15K	45K 45K		V/V V/V
* Common Mode Rejection Ratio (Note 2)	Full	80	96		74	90		dB
Unity Gain Bandwidth (Note 3)	+25°C		7			7		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 1)	Full	±12.0			±11.0			V
* Output Current (Note 4)	+25°C	±20			±15			mA
Output Resistance	+25°C		150			500		Ohms
TRANSIENT RESPONSE								
Rise Time (Notes 1, 5, 6 & 8)	+25°C		40	75		40	75	ns
Overshoot (Notes 1, 5, 6 & 8)	+25°C		15	40		15	40	%
* Slew Rate (Notes 1, 5 & 8)	+25°C	+3.5 -1.2	+5.0 -2.0			+5.0		V/μs
POWER SUPPLY CHARACTERISTICS								
* Supply Current	+25°C		1.8	2.5		1.8	2.5	mA
* Power Supply Rejection Ratio (Note 7)	Full	80	92		74	90		dB

NOTES: 1. R_L = 2KΩ
2. V_{CM} = ±5.0V
3. V_O < 90mV

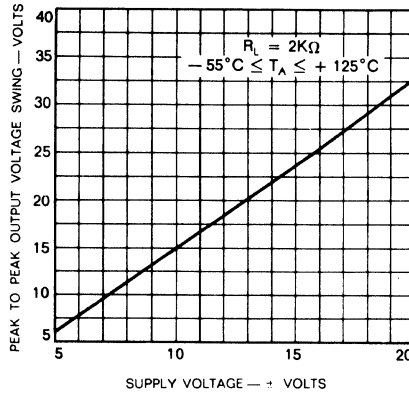
4. V_O = ±10.0V
5. C_L = 100pF
6. V_O = ±200mV
7. V_{Sup} = ±9.0V to ±15.0V

8. See Transient Response test circuits and waveforms – page 3.
9. 10 – 1000Hz, R_S = 10KΩ
10. Derate by 6.6mW/°C above 105°C

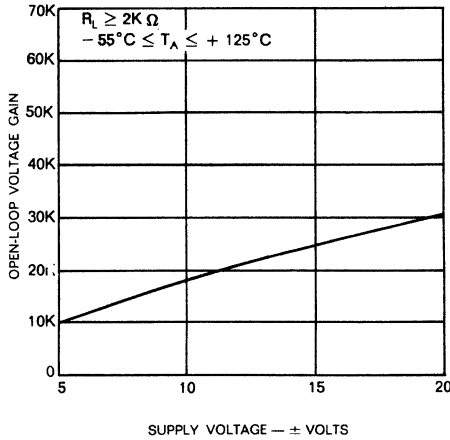
*100% Tested For DASH 8

GUARANTEED ELECTRICAL CHARACTERISTICS

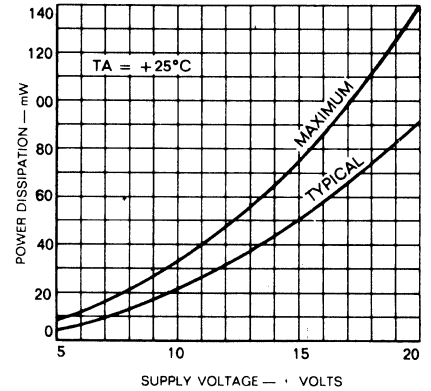
OUTPUT VOLTAGE SWING VS. SUPPLY VOLTAGE



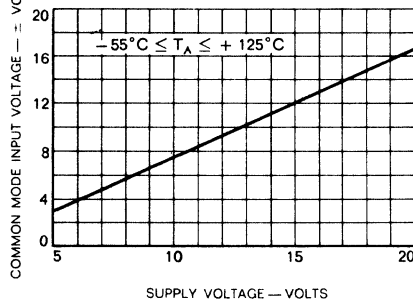
OPEN LOOP VOLTAGE GAIN VS. SUPPLY VOLTAGE



POWER DISSIPATION VS. SUPPLY VOLTAGE

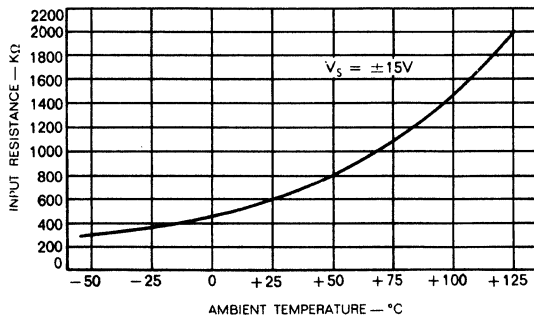


COMMON MODE INPUT VOLTAGE VS. SUPPLY VOLTAGE

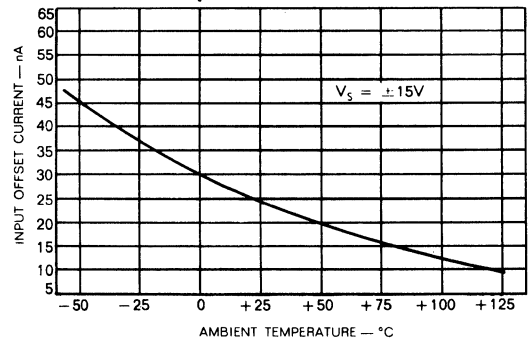


TYPICAL PERFORMANCE CURVES

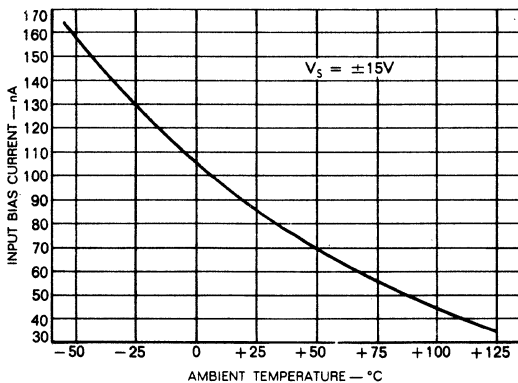
INPUT RESISTANCE VS. AMBIENT TEMPERATURE



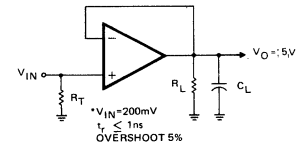
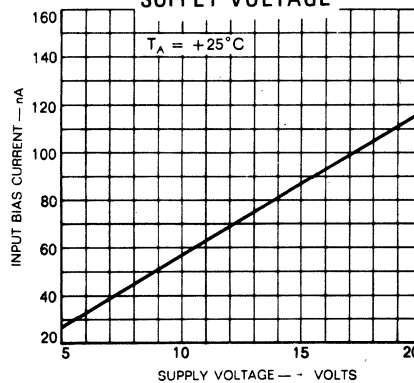
INPUT OFFSET CURRENT VS. AMBIENT TEMPERATURE



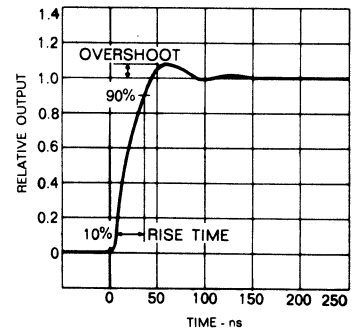
INPUT BIAS CURRENT VS. AMBIENT TEMPERATURE



INPUT BIAS CURRENT VS. SUPPLY VOLTAGE

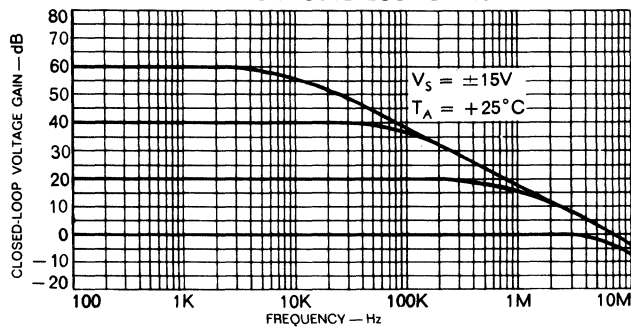


TRANSIENT RESPONSE

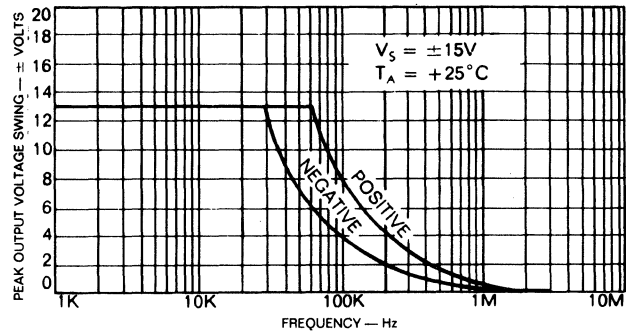


TYPICAL PERFORMANCE CURVES(continued)

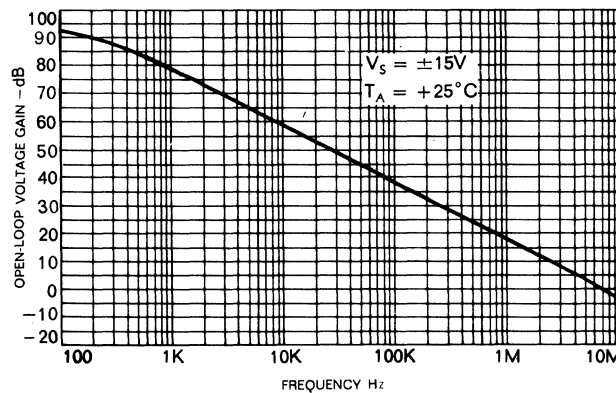
FREQUENCY RESPONSE FOR
VARIOUS CLOSED-LOOP GAINS



OUTPUT VOLTAGE SWING
VS. FREQUENCY



OPEN LOOP FREQUENCY RESPONSE



LINEAR

DEFINITIONS

Input Offset Voltage — That voltage which must be applied between the input terminals through two equal resistances to force the output voltage to zero.

Input Offset Current — The difference in the currents into the two input terminals when the output is at zero voltage.

Input Bias Current — The average of the currents flowing into the input terminals when the output is at zero voltage.

Input Common Mode Voltage — The average referred to ground of the voltages at the two input terminals.

Common Mode Range — The range of voltages which if exceeded at either input terminal will cause the amplifier to cease operating.

Common Mode Rejection Ratio — The ratio of a specified range of input common mode voltage to the peak to peak change in input offset voltage over this range.

Output Voltage Swing — The peak symmetrical output voltage swing, referred to ground, that can be obtained without clipping.

Input Resistance — The ratio of the change in input voltage to the change in input current.

Output Resistance — The ratio of the change in output voltage to the change in output current.

Positive Output Voltage Swing — The peak positive output voltage swing, referred to ground, that can be obtained without clipping.

Negative Output Voltage Swing — The peak negative output voltage swing, referred to ground, that can be obtained without clipping.

Voltage Gain — The ratio of the change in output voltage to the change in input voltage producing it.

Bandwidth — The frequency at which the voltage gain is 3 dB below its low frequency value.

Unity Gain Bandwidth — The frequency at which the voltage gain of the amplifier is unity.

Power Supply Rejection Ratio — The ratio of the change in input offset voltage to the change in power supply voltage producing it.

Transient Response — The closed loop step function response of the amplifier under small signal conditions.

Phase Margin — $[180^\circ - (\phi_1 - \phi_2)]$ where ϕ_1 is the phase shift at the frequency where the absolute magnitude of gain is unity, ϕ_2 is the phase shift at a frequency much lower than the open loop bandwidth.



HARRIS
SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-2000/2005/2000A/2005A

F.E.T. Input Preamplifier

FEATURES

- CONVERTS ANY OP AMP OR COMPARATOR TO F.E.T. INPUT
- INPUT BIAS CURRENT: 1pA
- INPUT RESISTANCE: 10^{12} OHMS
- SLEW RATE: 100 V/ μ S
- BANDWIDTH: 10 MHz
- MEETS MIL-STD-883 REQUIREMENTS

DESCRIPTION

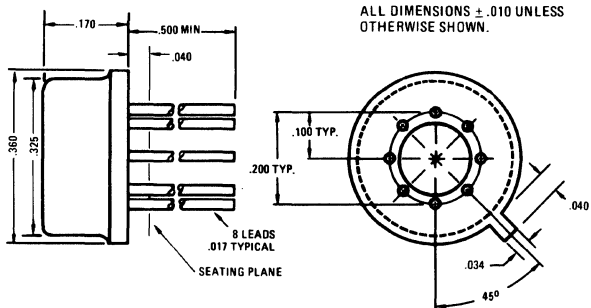
The HA-2000/2005 is a monolithic unity gain differential amplifier stage with J.F.E.T. inputs and bipolar transistor outputs. It is intended for use as a preamplifier for operational amplifiers and comparators to produce high input resistance and low bias currents without sacrificing high speed performance. The circuit has a much wider common mode range than simple F.E.T. pairs, allowing op amps to be connected as voltage followers with full output swing. The circuit can also be used as a high impedance unity gain buffer for differential or two single-ended signals for frequencies from D.C. to R.F.

The HA-2000 is guaranteed for operation from -55°C to $+125^{\circ}\text{C}$ while the HA-2005 is guaranteed from 0°C to $+75^{\circ}\text{C}$.

PACKAGES

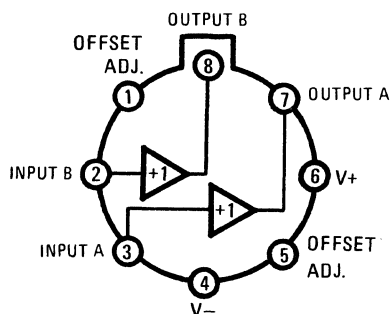
CODE 2A

Bottom View T0-99
ALL DIMENSIONS ARE IN INCHES.
ALL DIMENSIONS $\pm .010$ UNLESS OTHERWISE SHOWN.

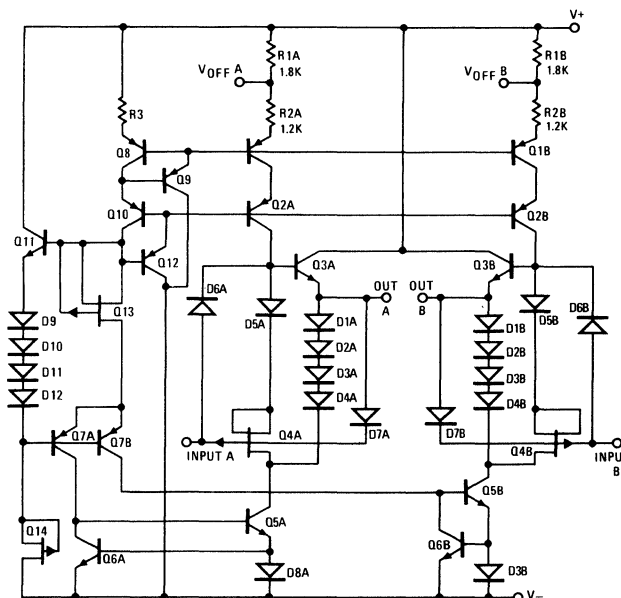


NOTES: 1. All leads gold plated KOVAR
2. All dimensions in inches

PIN-OUT Top View



SCHEMATIC



LINEAR

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	35V	Internal Power Dissipation (Note 8)	300mW
Differential Input Voltage	$\pm V_{Supply}$	Operating Temp. Range	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (HA-2000)
Output Current	30mA		$0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$ (HA-2005)
		Storage Temp. Range	$-65^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS

PARAMETER	TEMP.	HA-2000/HA-2000A			HA-2005/HA-2005A			UNITS
		-55°C to $+125^{\circ}\text{C}$			0°C to $+75^{\circ}\text{C}$			
		MIN.	LIMITS TYP.	MAX.	MIN.	LIMITS TYP.	MAX.	
INPUT CHARACTERISTICS								
Offset Voltage (Note 1) HA-2000 / HA-2005	$+25^{\circ}\text{C}$ Full		12 20	20 25		25 50	50 55	mV mV
HA-2000A / HA-2005A	$+25^{\circ}\text{C}$ Full		5 10	10 12		5 10	10 12	mV mV
Bias Current	$+25^{\circ}\text{C}$ Full		1 0.5	20 10		1 0.02	20 1	ρA nA
Offset Current	$+25^{\circ}\text{C}$ Full		0.5 0.1	20 5		0.5 .005	20 .5	ρA nA
Input Resistance	$+25^{\circ}\text{C}$		10^{12}			10^{12}		Ω
Input Capacitance	$+25^{\circ}\text{C}$		5			5		ρF
Common Mode Range	Full	± 10.0			± 10.0			V
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 2)	$+25^{\circ}\text{C}$ Full	.98 .98	.999		.98 .98	.999		V/V V/V
Common Mode Rejection Ratio (Note 3)	Full	80	90		70	90		dB
-3dB Bandwidth	$+25^{\circ}\text{C}$		10			10		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 2)	Full	± 10			± 10			V
Output Current Source	$+25^{\circ}\text{C}$	+5			+5			mA
Sink	$+25^{\circ}\text{C}$	-65			-65			μA
Output Common Mode Offset Voltage	Full			0.5			0.5	V
Full Power Bandwidth (Notes 4,5)	$+25^{\circ}\text{C}$		1,000			1,000		kHz
TRANSIENT RESPONSE								
Rise Time (Notes 4,6)	$+25^{\circ}\text{C}$		50			50		ns
Overshoot (Notes 4,6)	$+25^{\circ}\text{C}$		5			5		%
Slew Rate (Notes 4,5)	$+25^{\circ}\text{C}$		100			100		V/ μs
POWER SUPPLY CHARACTERISTICS								
Supply Current	$+25^{\circ}\text{C}$		0.7	1.7		0.7	1.7	mA
Power supply Rejection Ratio (Note 7)	Full	80	90		70	90		dB

NOTES: 1. Adjustable to 0 with $100\text{K}\Omega$ pot between pins 1 and 5 wiper to V+
 2. $R_L = 1\text{M}$
 3. $V_{CM} = \pm 5.0\text{V}$

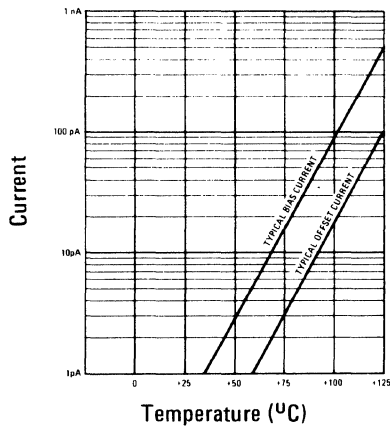
4. $R_L = 10\text{K}$ to V-
 5. $V_O = \pm 10\text{V}$
 6. $V_O = \pm 200\text{mV}$
 7. $V_S = \pm 9\text{V}$ to $\pm 15\text{V}$
 8. Derate by $6.6\text{mW}/^{\circ}\text{C}$ above 105°C

LINEAR

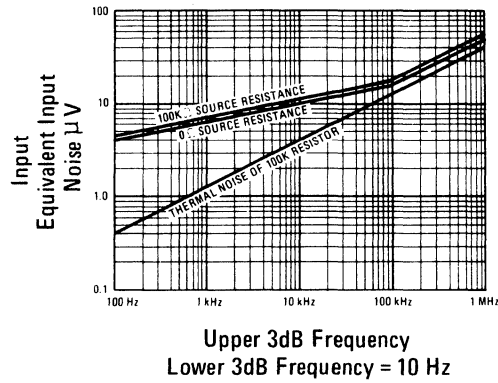
PERFORMANCE CURVES

$V+ = 15\text{ VDC}$, $V- = 15\text{ VDC}$, $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE STATED.

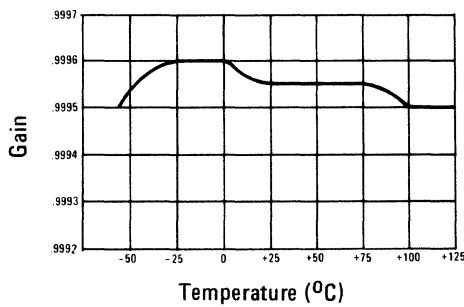
INPUT BIAS AND OFFSET CURRENT VS. TEMPERATURE



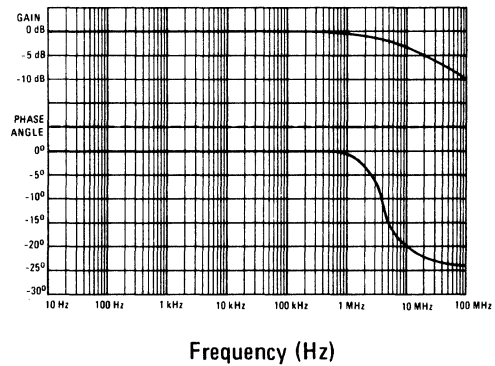
EQUIVALENT INPUT NOISE VS. BANDWIDTH



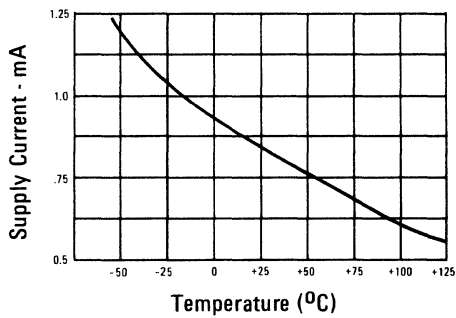
D.C. GAIN VS. TEMPERATURE



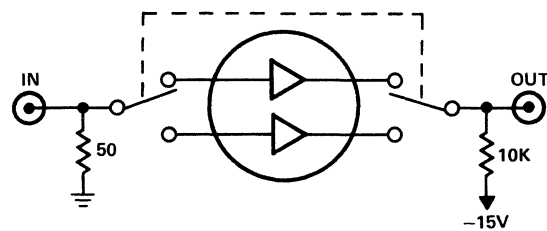
GAIN, PHASE ANGLE VS. FREQUENCY



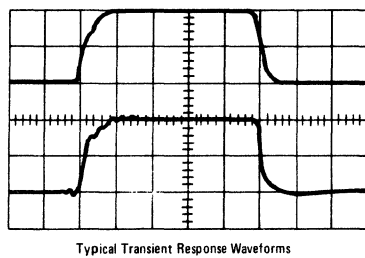
POWER SUPPLY CURRENT VS. TEMPERATURE



TRANSIENT RESPONSE, SLEW RATE TEST HOOK-UP

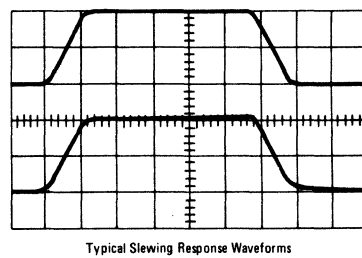


TYP. TRANSIENT RESPONSE WAVEFORM



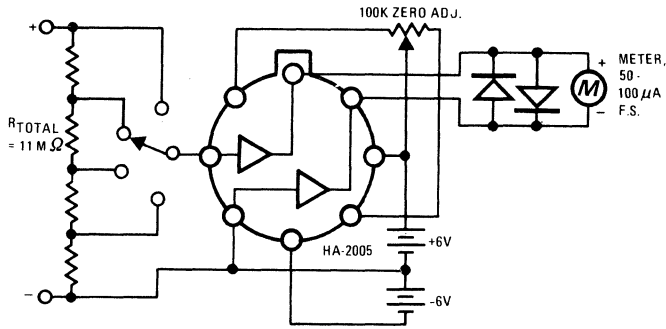
Upper Trace: Input
Lower Trace: Output
Vertical Scale: 100mV/Div.
Horizontal Scale: 100ns/Div.

TYP. SLEWING RESPONSE WAVEFORM



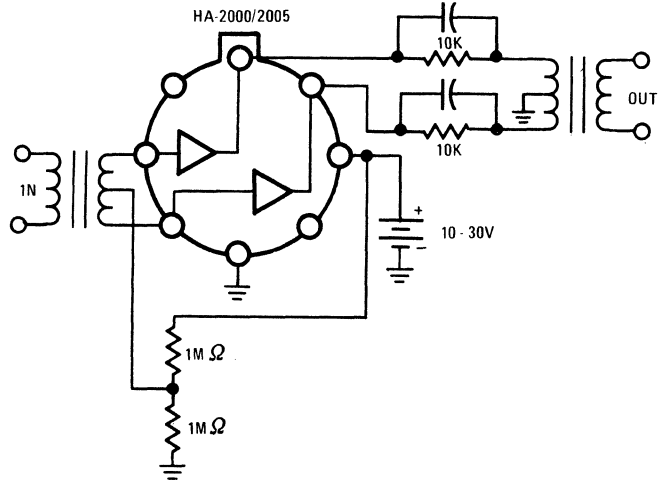
Upper Trace: Input
Lower Trace: Output
Vertical Scale: 5V/Div.
Horizontal Scale: 100ns/Div.

TYPICAL APPLICATIONS

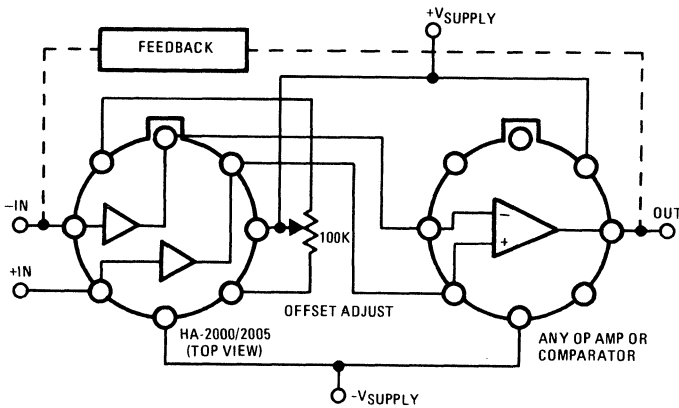


BALANCED LINE AMPLIFIER FOR AUDIO TO 100MHz SIGNALS

F.E.T. VOLTMETER

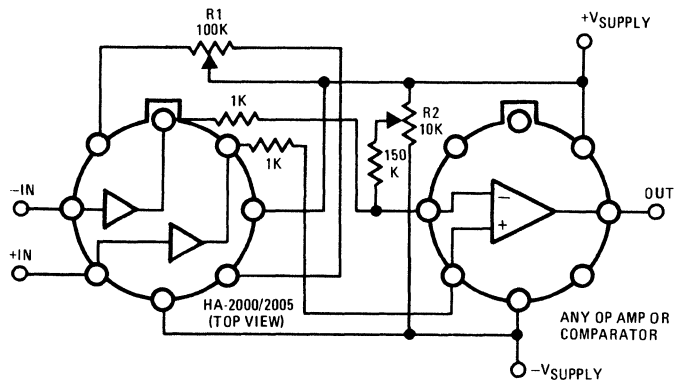


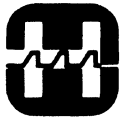
HOOKEUP TO CREATE F.E.T. INPUT OP AMP OR COMPARATOR



ALTERNATE HOOKEUP TO ADJUST FOR MINIMUM OFFSET VOLTAGE TEMPERATURE COEFFICIENT

Adjust R_1 to point of minimum offset voltage change over temperature range. Adjust R_2 to zero offset voltage. Drifts of less than $10 \mu V / ^\circ C$ can typically be achieved.





HARRIS
SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-2050/2055/2050A/2055A

High Slew Rate F.E.T. Input Operational Amplifiers

LINEAR

FEATURES

- HIGH SLEW RATE 120V/ μ s
- FAST SETTling 400ns
- WIDE POWER BANDWIDTH 2 MHz
- HIGH GAIN BANDWIDTH 20 MHz
- HIGH INPUT IMPEDANCE 10^{12} OHMS
- LOW BIAS CURRENT 1 pA
- TRUE OP AMP – CAN BE OPERATED INVERTING OR NON-INVERTING
- MEETS MIL-STD-883 REQUIREMENTS

DESCRIPTION

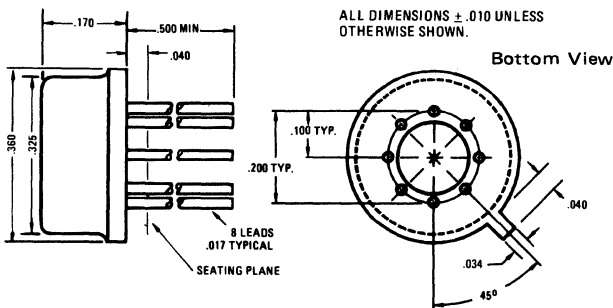
The HA-2050/2055 is an operational amplifier combining the advantages of very high slew rate and wide bandwidth with ultra-low input current and high input resistance. These devices are ideal for use in sample-and-hold circuits, A/D, D/A and sampled data systems; and for use in wide band R.F. or video systems where wide bandwidth at high output levels is required. The device may be operated inverting or non-inverting; and external compensation is required only when operated at closed loop gains less than three. An internal feedback capacitor is provided to cancel phase shift in the feedback loop due to input capacitance.

The HA-2050 is guaranteed for operation from -55°C to $+125^{\circ}\text{C}$ and the HA-2055 is guaranteed from 0°C to $+75^{\circ}\text{C}$.

PACKAGE

CODE 2A

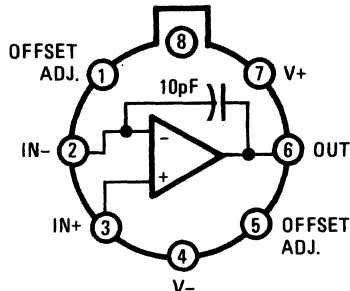
T0-99



NOTES: 1. All leads gold plated KOVAR
2. All dimensions in inches

BANDWIDTH CONTROL

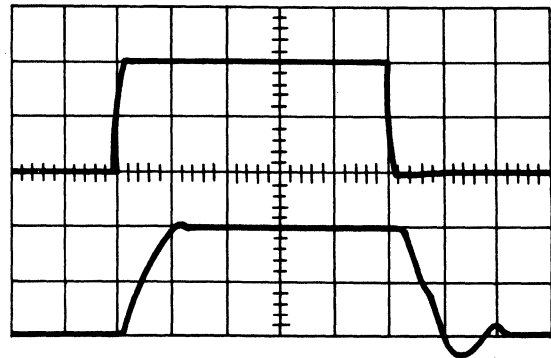
PIN-OUT



Case Connected to V+

Top View

SLEWING WAVEFORM



Horizontal Scale: 100ns/Div.
Upper Trace: Input; 1.67V/Div.
Lower Trace: Output; 5.0V/Div.
Gain = +3, $R_L = 2\text{K Ohms}$, $C_L = 50\text{pF}$

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	35.0V	Internal Power Dissipation (Note 10)	300mW	
Differential Input Voltage	±15.0V	Operating Temp. Range	-55°C ≤ T _A ≤ +125°C	(HA-2050)
Output Current	50mA		0°C ≤ T _A ≤ +75°C	(HA-2055)
		Storage Temp. Range	-65°C ≤ T _A ≤ +150°C	

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{Supply} = ±15.0V unless otherwise specified.

PARAMETER	TEMP.	HA-2050/HA-2050A -55°C to +125°C			HA-2055/HA-2055A 0°C to +75°C			UNITS
		LIMITS			LIMITS			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
INPUT CHARACTERISTICS								
Offset Voltage (Note 1)								
HA-2050 / HA-2055	+25°C		15	25		30	60	mV
	Full			30			65	mV
HA-2050A / HA-2055A	+25°C		7	14		7	14	mV
	Full			17			17	mV
Bias Current	+25°C		1	20		1	20	ρA
	Full		0.5	10		0.02	1	nA
Offset Current	+25°C		0.5	20		0.5	20	ρA
	Full		0.1	5		.005	0.5	nA
Input Resistance	+25°C		10 ¹²			10 ¹²		Ω
Input Capacitance	+25°C		5			5		ρF
Common Mode Range	Full	±10.0			±10.0			V
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 2,5)	+25°C	7.5K	15K		7.5K	15K		V/V
	Full	5K			5K			V/V
Common Mode Rejection Ratio (Note 3)	Full	74	90		70	90		dB
Gain Bandwidth Product (Note 4)	+25°C		20			20		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 2)	Full	±10	±12		±10	±12		V
Output Current	+25°C	±10	±20		±10	±20		mA
Full Power Bandwidth (Note 5)	+25°C		2,000			2,000		kHz
TRANSIENT RESPONSE (NOTES 2, 8, 9)								
Rise Time (Note 6)	+25°C		50			50		ns
Overshoot (Note 6)	+25°C		25			25		%
Slew Rate (Note 5)	+25°C		120			120		V/μs
Settling Time	+25°C		0.4			0.4		μs
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C		6.0	8.0		6.0	8.0	mA
Power Supply Rejection Ratio (Note 7)	Full	74	90		70	90		dB

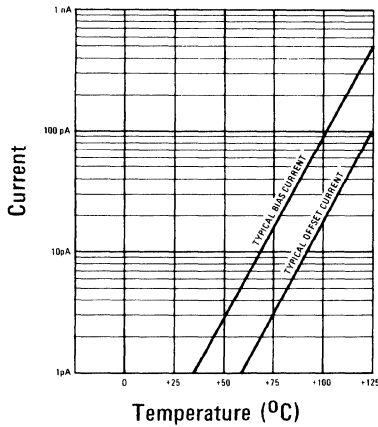
- NOTES: 1. Adjustable to zero with 100KΩ pot between pins 1 and 5; wiper to V+.
2. R_L = 2K
3. V_{CM} = ±5.0V
4. A_V > 10
5. V_O = ±10V

6. V_O = ±200mV
7. ΔV = ±5.0V
8. C_L = 50pF
9. A_V = +3, See transient response test circuit and wave forms, page 4.
10. Derate by 6.6mW/°C above 105°C

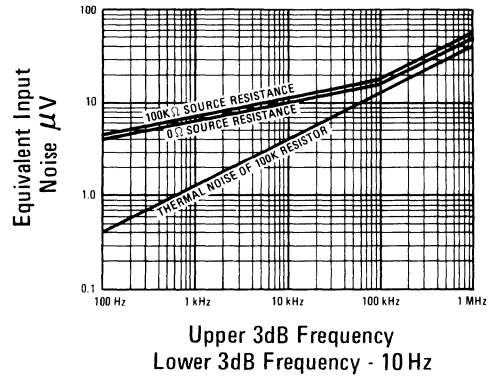
PERFORMANCE CURVES

$V_+ = 15\text{ VDC}$, $V_- = 15\text{ VDC}$, $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE STATED.

INPUT BIAS AND OFFSET CURRENT VS. TEMPERATURE

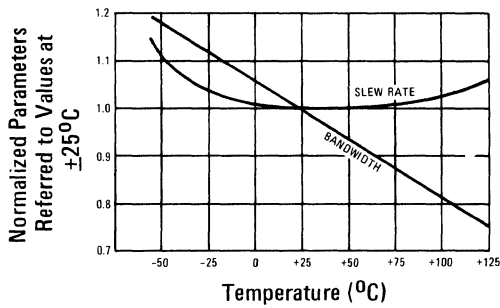


EQUIVALENT INPUT NOISE VS. BANDWIDTH

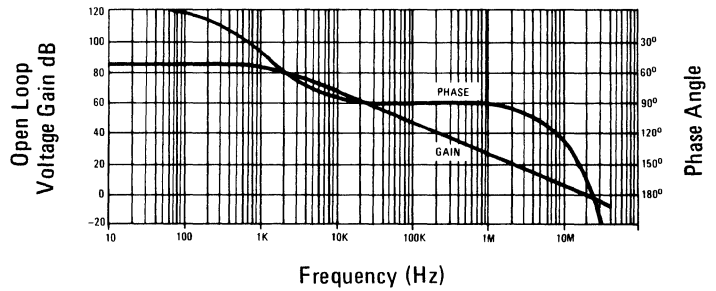


Upper 3dB Frequency
Lower 3dB Frequency - 10 Hz

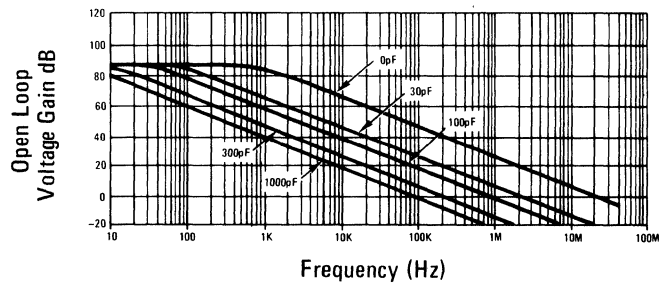
NORMALIZED AC PARAMETERS VS. TEMPERATURE



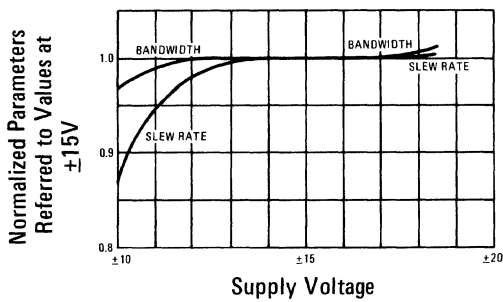
OPEN-LOOP FREQUENCY AND PHASE RESPONSE



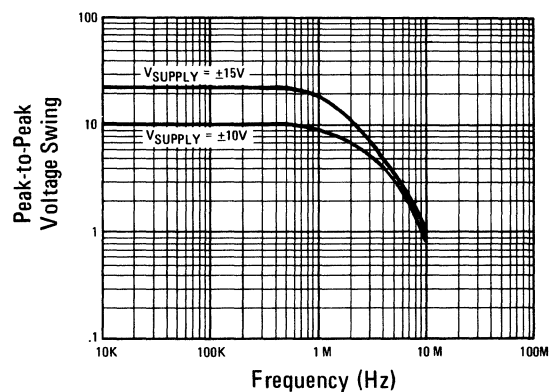
OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM BANDWIDTH CONTROL PIN TO GROUND



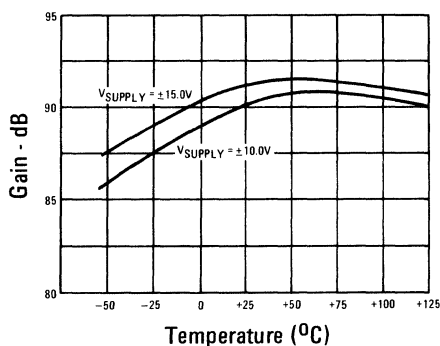
NORMALIZED AC PARAMETERS VS. SUPPLY VOLTAGE AT +25°C



OUTPUT VOLTAGE SWING VS. FREQUENCY AT +25°C

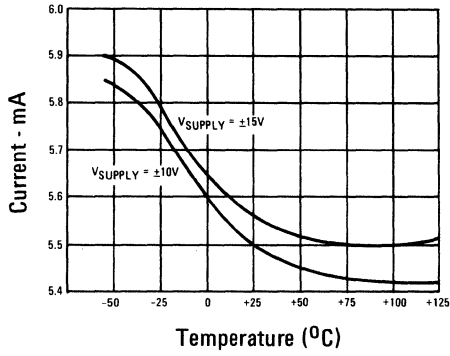


OPEN LOOP VOLTAGE GAIN VS. TEMPERATURE

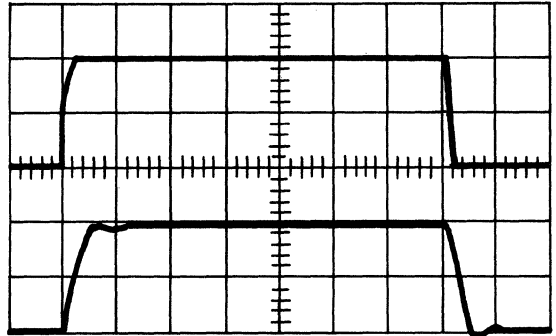


PERFORMANCE CURVES (continued)

POWER SUPPLY CURRENT VS. TEMPERATURE



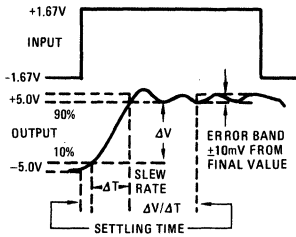
TRANSIENT RESPONSE; $A_V = +3$



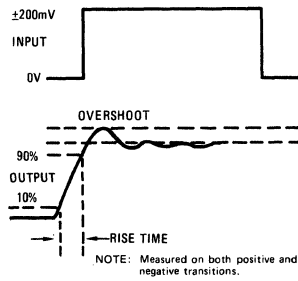
$R_L = 2K \text{ Ohms}, C_L = 50pF$
 Upper Trace: Input; 33mV/Div.
 Lower Trace: Output; 100mV/Div.
 Horizontal = 100ns/Div.
 $T_A = +25^\circ C, V_S = \pm 15V$

LINEAR

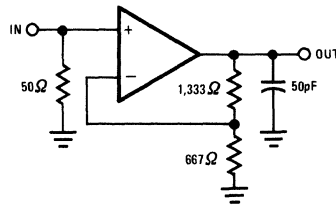
SLEW RATE AND SETTLING TIME



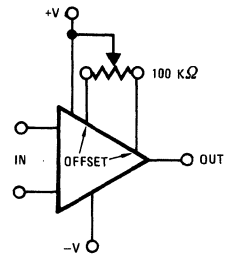
TRANSIENT RESPONSE



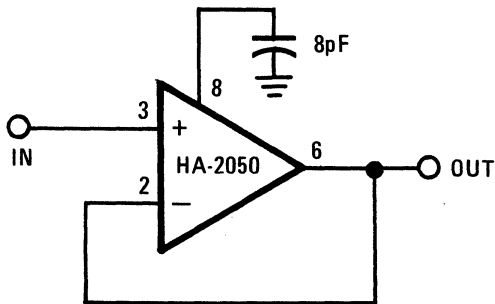
SLEW RATE AND TRANSIENT RESPONSE



SUGGESTED OFFSET ZERO ADJUST HOOK-UP



TYPICAL APPLICATIONS



COMPENSATION CIRCUIT FOR UNITY GAIN

Slew Rate $\approx 40V/\mu s$
 Bandwidth $\approx 8 \text{ MHz}$



HARRIS
SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-2060/2065/ 2060A/2065A

Wide Band F.E.T. Input Operational Amplifier

FEATURES

- GAIN BANDWIDTH PRODUCT 100 MHz
- HIGH INPUT IMPEDANCE 10^{12} OHMS
- LOW BIAS CURRENT 1 pA
- HIGH SLEW RATE $35V/\mu s$
- WIDE POWER BANDWIDTH 600 kHz
- TRUE OP AMP - CAN BE OPERATED INVERTING OR NON-INVERTING
- MEETS MIL-STD-883 REQUIREMENTS

DESCRIPTION

The HA-2060/2065 is an operational amplifier combining the advantages of very wide bandwidth and high slew rate with ultra-low input current and high input resistance. These devices are ideal for use in sample-and-hold circuits, active filters, wide band amplifiers, high gain amplifiers with superior bandwidth, and wherever very low closed loop gain and phase shift errors are required. The device may be operated inverting or non-inverting; and external compensation is required only when operated at closed loop gains less than five. An internal feedback capacitor is provided to cancel phase shift in the feedback loop due to input capacitance.

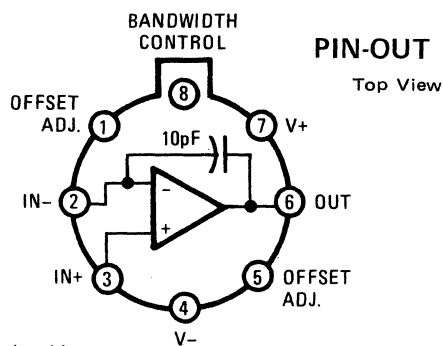
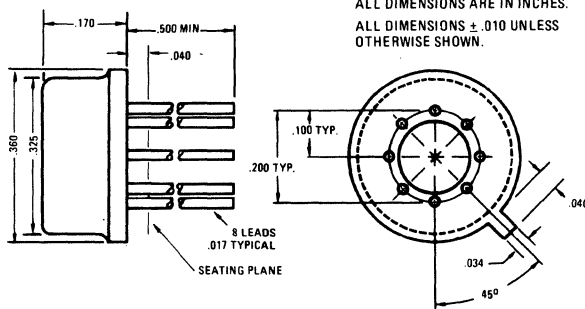
The HA-2060 is guaranteed for operation from $-55^{\circ}C$ to $+125^{\circ}C$ and the HA-2065 is guaranteed from $0^{\circ}C$ to $+75^{\circ}C$.

PACKAGE

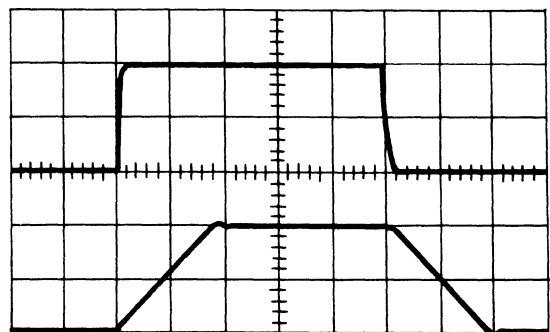
CODE 2A

Bottom View

T0-99



SLEWING WAVEFORM



Horizontal Scale: 200ns/Div.
Upper Trace: Input; 1.0V/Div.
Lower Trace: Output; 5.0V/Div.
Gain = +5, $R_L = 2K$ Ohms, $C_L = 50pF$

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	35.0V	Internal Power Dissipation (Note 10)	300mW
Differential Input Voltage	±12V	Operating Temp. Range	-55°C ≤ T _A ≤ +125°C (HA-2060)
Output Current / Full Short Circuit Protection			0°C ≤ T _A ≤ +75°C (HA-2065)
		Storage Temp. Range	-65°C ≤ T _A ≤ +150°C

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{Supply} = ±15.0V unless otherwise specified.

PARAMETER	TEMP.	HA-2060/HA-2060A -55°C to +125°C			HA-2065/HA-2065A 0°C to +75°C			UNITS
		LIMITS			LIMITS			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
INPUT CHARACTERISTICS								
Offset Voltage (Note 1)								
HA-2060 / HA-2065	+25°C		15	25		15	60	mV
	Full			30			65	mV
HA-2060A / HA-2065A	+25°C		7	12		7	12	mV
	Full			15			15	mV
Bias Current	+25°C		1	20		1	20	ρA
	Full		0.5	10		0.02	1	nA
Offset Current	+25°C		0.5	20		0.5	20	ρA
	Full		0.1	5		.005	.5	nA
Input Resistance	+25°C		10 ¹²			10 ¹²		Ω
Input Capacitance	+25°C		5			5		ρF
Common Mode Range	Full	±10.0			±10.0			V
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 2, 5)	+25°C	80K	150K		80K	150K		V/V
	Full	60K			70K			V/V
Common Mode Rejection Ratio (Note 3)	Full	74	90		70	90		dB
Gain Bandwidth Product (Note 4)	+25°C		100			100		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 2)	Full	±10	±12		±10	±12		V
Output Current	+25°C	±10	±18		±10	±18		mA
Full Power Bandwidth (Note 5)	+25°C		600			600		kHz
TRANSIENT RESPONSE (NOTES 2, 8, 9)								
Rise Time (Note 6)	+25°C		50			50		ns
Overshoot (Note 6)	+25°C		25			25		%
Slew Rate (Note 5)	+25°C		35			35		V/μs
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C		4.0	6.0		4.0	6.0	mA
Power Supply Rejection Ratio (Note 7)	Full	74	90		70	90		dB

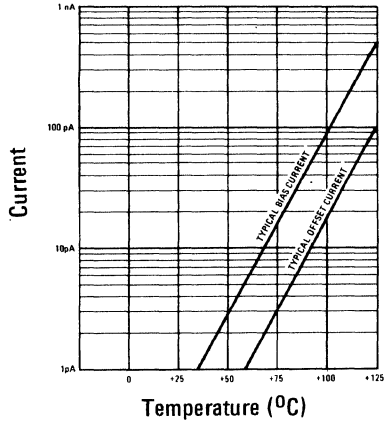
- NOTES: 1. Adjustable to zero with 100K Ω pot between pins 1 and 5; wiper to V+.
2. R_L = 2K
3. V_{CM} = ±5.0V
4. A_V > 10
5. V_O = ±10V

6. V_O = ±200mV
7. ΔV = ±5.0V
8. C_L = 50 ρF
9. A_V = +5, See transient response test circuits and waveforms, page 4.
10. Derate by 6.6mW/°C above 105°C

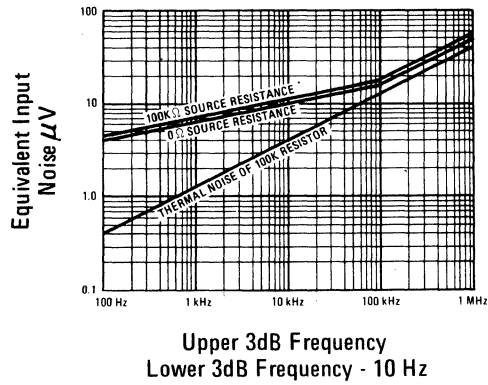
PERFORMANCE CURVES

$V_+ = 15\text{VDC}$, $V_- = 15\text{VDC}$, $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE STATED

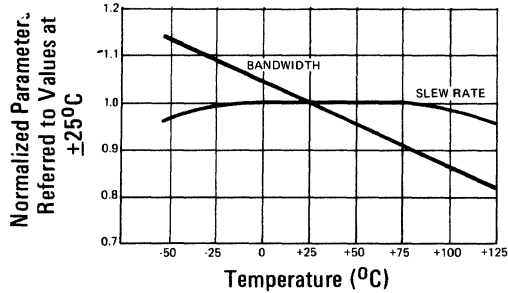
INPUT BIAS AND OFFSET CURRENT VS. TEMPERATURE



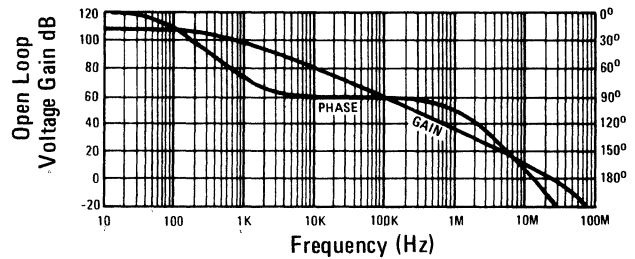
EQUIVALENT INPUT NOISE VS. BANDWIDTH



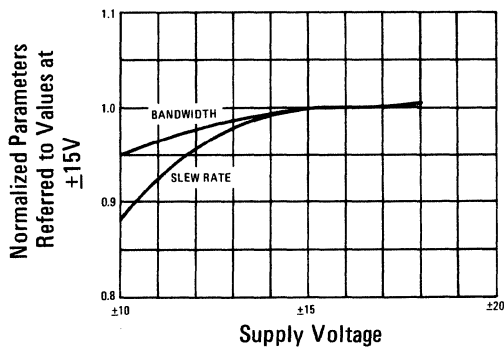
NORMALIZED AC PARAMETERS VS. TEMPERATURE



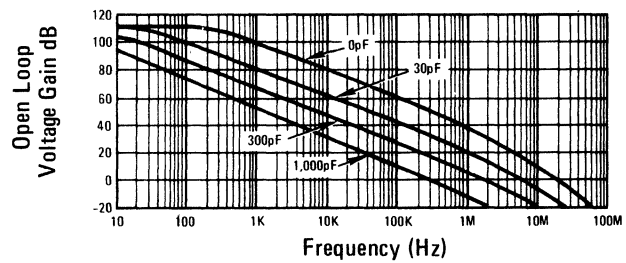
OPEN-LOOP FREQUENCY AND PHASE RESPONSE



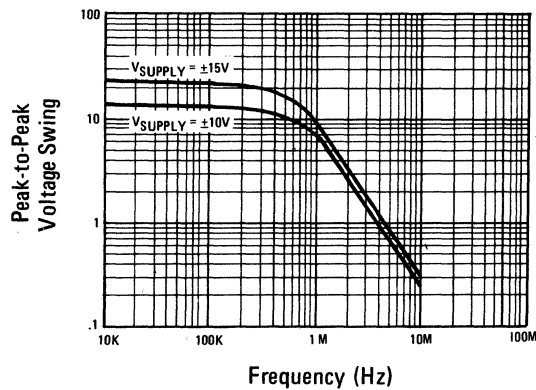
NORMALIZED AC PARAMETERS VS. SUPPLY VOLTAGE AT +25°C



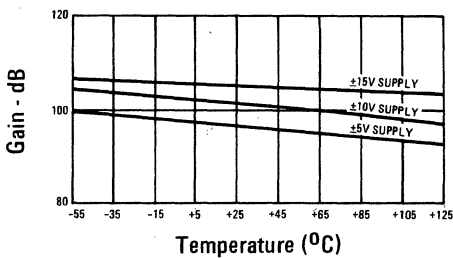
OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM BANDWIDTH CONTROL PIN TO GROUND



OUTPUT VOLTAGE SWING VS. FREQUENCY AT +25°C

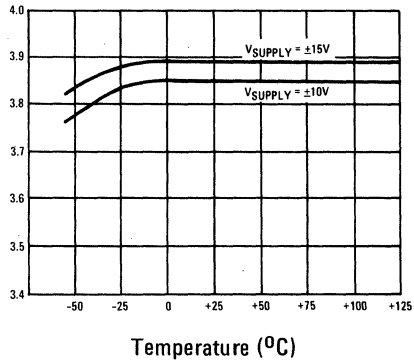


OPEN LOOP VOLTAGE GAIN VS. TEMPERATURE

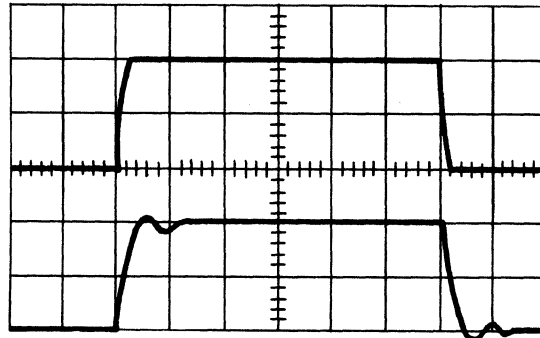


PERFORMANCE CURVES (continued)

POWER SUPPLY CURRENT VS. TEMPERATURE

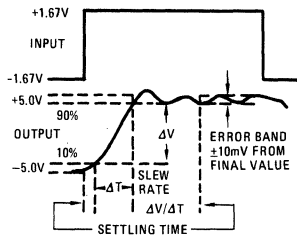


TRANSIENT RESPONSE; $A_V = +5$

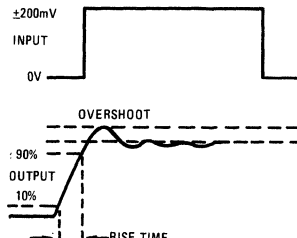


$R_L = 2K \text{ Ohms}, C_L = 50pF$
 Upper Trace: Input; 20mV/Div.
 Lower Trace: Output; 100mV/Div.
 Horizontal = 100ns/Div.
 $T_A = +25^\circ C, V_S = \pm 15V$

SLEW RATE AND SETTLING TIME

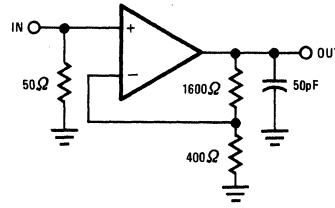


TRANSIENT RESPONSE

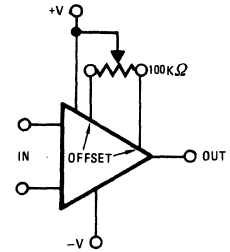


NOTE: Measured on both positive and negative transitions.

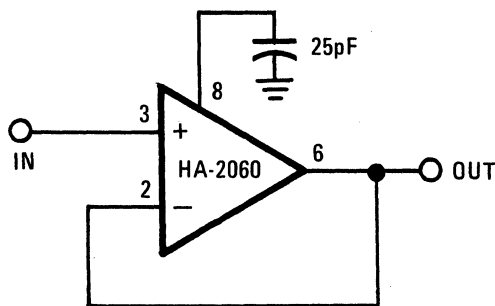
SLEW RATE AND TRANSIENT RESPONSE



SUGGESTED OFFSET ZERO ADJUST HOOK-UP



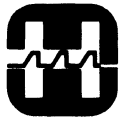
TYPICAL APPLICATIONS



COMPENSATION CIRCUIT FOR UNITY GAIN

SLEW RATE $\approx 5 V/\mu s$

BANDWIDTH $\approx 10 \text{ MHz}$



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HA-2111/2211

Voltage Comparators

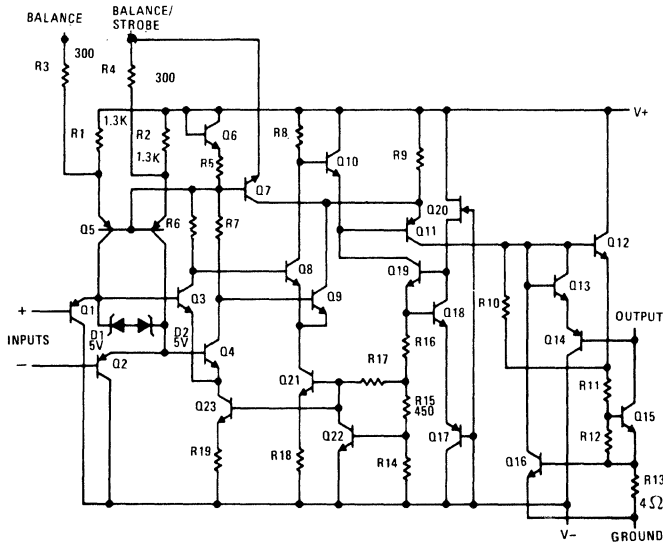
FEATURES

- INPUT BIAS CURRENT 60nA
- INPUT OFFSET CURRENT 4nA
- DIFFERENTIAL INPUT VOLTAGE $\pm 30.0V$
- POWER SUPPLY VOLTAGES A SINGLE 5.0V SUPPLY TO $\pm 15.0V$
- OFFSET VOLTAGE NULL CAPABILITY
- STROBE CAPABILITY

GENERAL DESCRIPTION

The HA-2111 and HA-2211 are voltage comparators which have low input bias currents. They operate over a wide range of power supply voltages, from the standard $\pm 15.0V$ down to a single 5.0V power supply. A very flexible output stage is employed, which is compatible with RTL, DTL, TTL and MOS logic circuits.

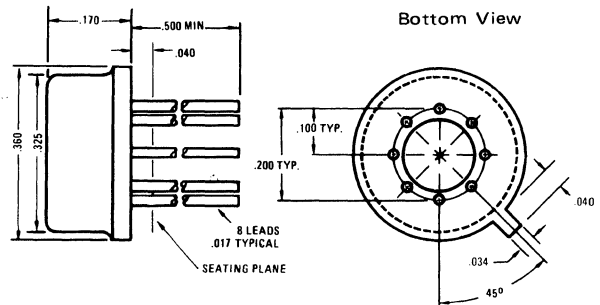
SCHEMATIC



PACKAGES

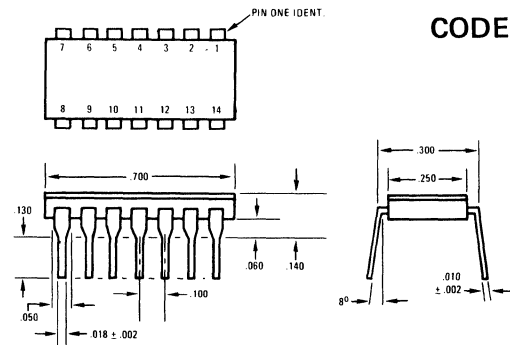
CODE 2A

T0-99



ALL DIMENSIONS ARE IN INCHES.
ALL DIMENSIONS $\pm .010$ UNLESS OTHERWISE SHOWN.

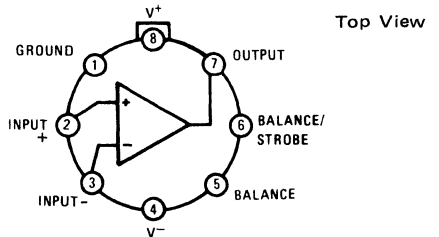
CODE 1S



PIN OUT

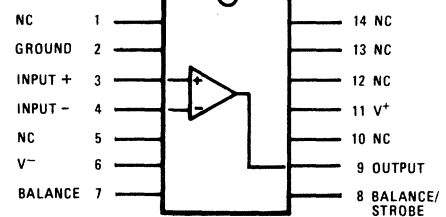
T0-99

Case Connected to V-



TO-116

Case Connected to V-



LINEAR

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V ⁺ and V ⁻ Terminals	36.0V
Output to V ⁻	50.0V
Ground to V ⁻	30.0V
Differential Input Voltage	±30.0V
Input Voltage (Note 1)	±15.0V
Internal Power Dissipation (Note 7)	500mW
Output Short Circuit Duration	10 sec.
Storage Temperature Range	-65°C to +150°C

ELECTRICAL CHARACTERISTICS

V⁺ = +15.0 V.D.C.

V⁻ = -15.0 V.D.C.

PARAMETER	TEMPERATURE	HA-2111 -55°C to +125°C			HA-2211 -25°C to +85°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
* Offset Voltage (Note 2)	+25°C		0.7	3.0		0.7	3.0	mV
	Full			4.0			4.0	mV
* Bias Current	+25°C		60	100		60	100	nA
	Full			150			150	nA
* Offset Current (Note 2)	+25°C		4.0	10.0		4.0	10.0	nA
	Full			20.0			20.0	nA
Common Mode Range	Full		±14.0			±14.0		V
Strobe Current	+25°C		3.0			3.0		mA
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain	+25°C		200K			200K		V/V
Response Time (Note 3)	+25°C		200			200		ns
OUTPUT CHARACTERISTICS								
* Leakage Current (Note 4)	+25°C		0.2	10.0		0.2	10.0	nA
	Full			500			500	nA
* Saturation Voltage (Note 5)	+25°C		0.75	1.5		0.75	1.5	V
(Note 6)	Full		0.23	0.4		0.23	0.4	V
POWER SUPPLY CHARACTERISTICS								
* Positive Supply Current	+25°C		5.1	6.0		5.1	6.0	mA
* Negative Supply Current	+25°C		4.1	5.0		4.1	5.0	mA

NOTES: 1. This rating applies for ±15.0V supplies. The positive input voltage limit is 30.0V above the negative supply. The negative input voltage is equal to the negative supply voltage or 30.0V below the positive supply, whichever is less.

2. The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

3. 100mV input step; 5mV overdrive.

4. V_{OUT} = 35.0V; V_{IN} = 5mV

5. I_{OUT} = 50mA; V_{IN} = -5mV

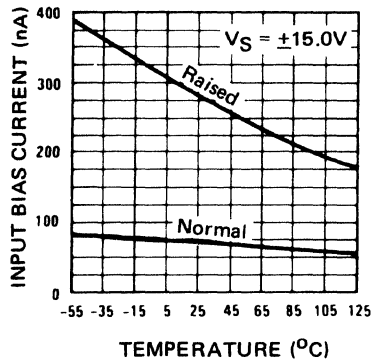
6. I_{Sink} = 8mA; V⁺ = 4.5V; V⁻ = 0V; V_{IN+} = +1.00V; V_{IN-} = +1.006V

7. Derate by 6.6mW/°C above 105°C

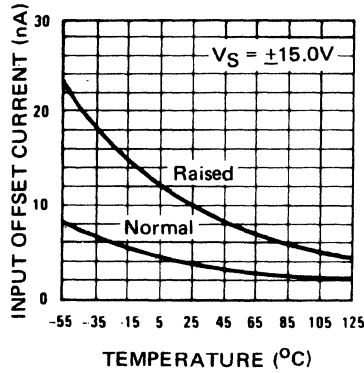
*100% Tested For DASH 8

TYPICAL PERFORMANCE CURVES

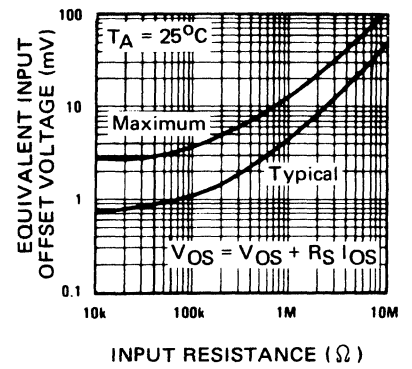
INPUT BIAS CURRENT



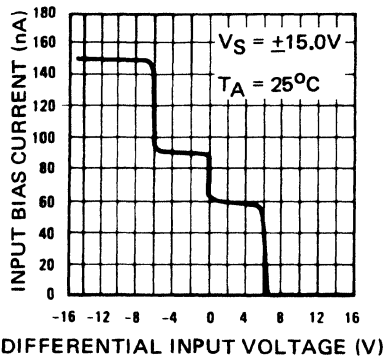
INPUT OFFSET CURRENT



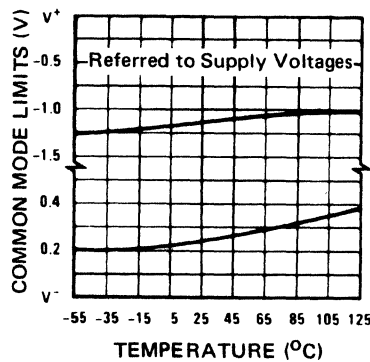
OFFSET ERROR



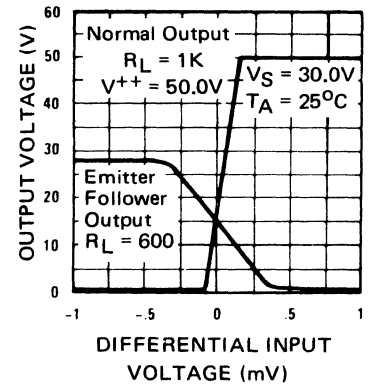
INPUT CHARACTERISTICS



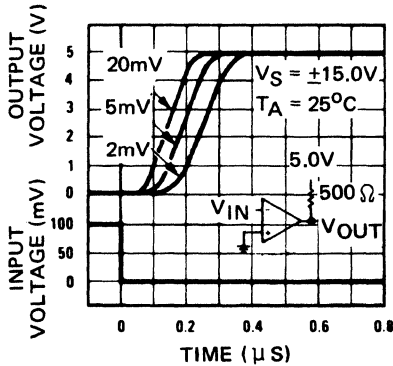
COMMON MODE LIMITS



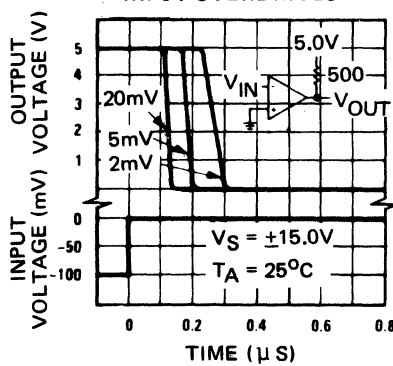
TRANSFER FUNCTION



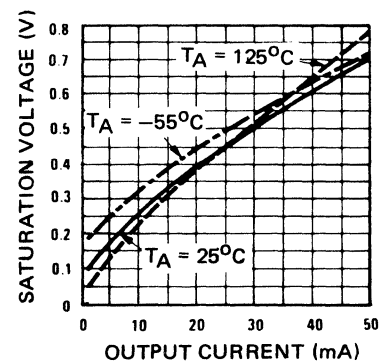
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



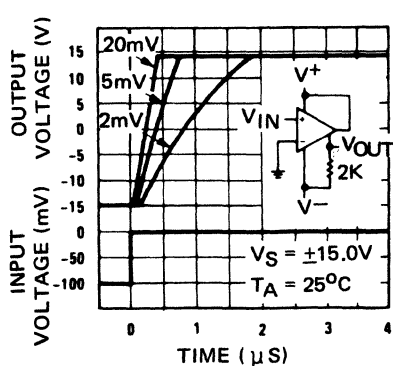
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



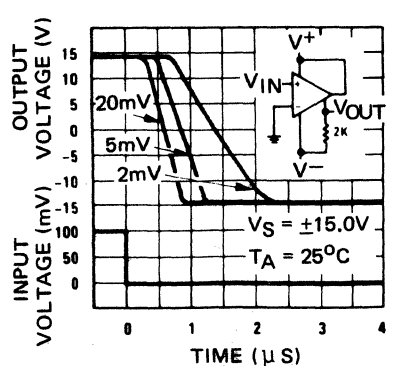
OUTPUT SATURATION VOLTAGE



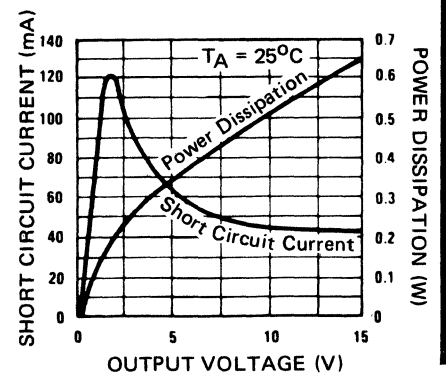
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

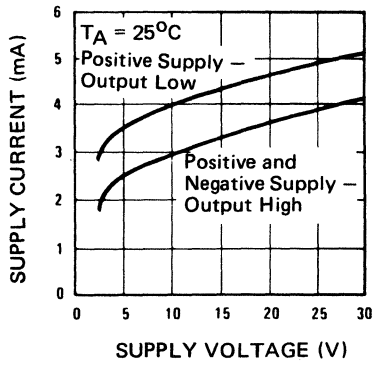


OUTPUT LIMITING CHARACTERISTICS

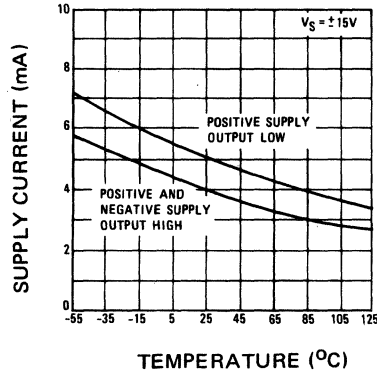


TYPICAL PERFORMANCE CURVES(continued)

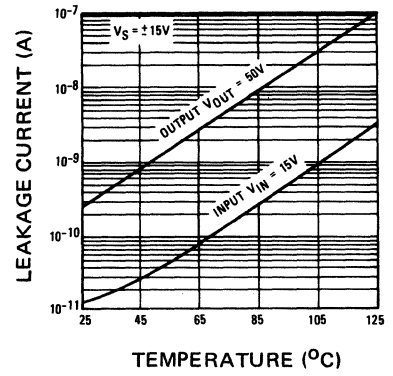
SUPPLY CURRENT



SUPPLY CURRENT

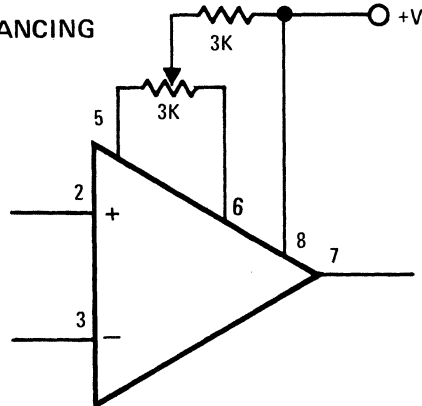


LEAKAGE CURRENTS

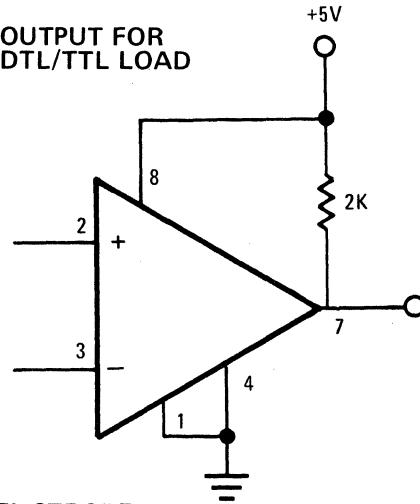


APPLICATION INFORMATION

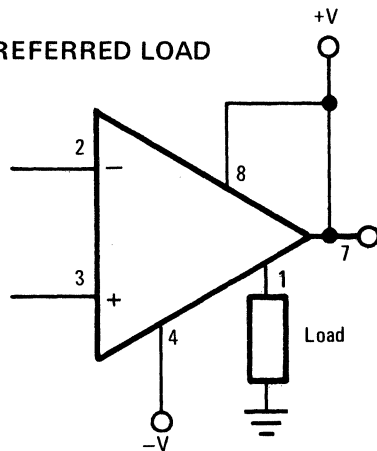
OFFSET BALANCING



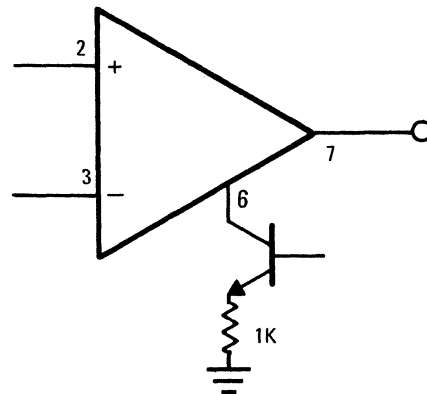
OUTPUT FOR DTL/TTL LOAD



GROUND REFERRED LOAD

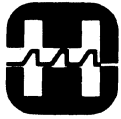


TTL STROBE



NOTE: INPUT POLARITIES REVERSED

LINEAR



HARRIS
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A DIVISION OF HARRIS CORPORATION

HA-2311

Voltage Comparator

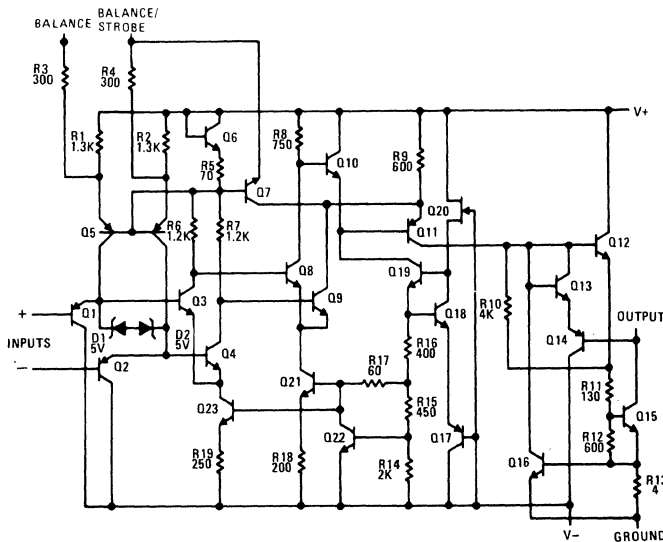
FEATURES

- INPUT BIAS CURRENT 100nA
- INPUT OFFSET CURRENT 6nA
- DIFFERENTIAL INPUT VOLTAGE $\pm 30.0V$
- POWER SUPPLY VOLTAGES A SINGLE $+5.0V$ SUPPLY TO $\pm 15.0V$
- OFFSET VOLTAGE NULL CAPABILITY
- STROBE CAPABILITY

GENERAL DESCRIPTION

The HA-2311 is a voltage comparator which has low input bias currents. It operates over a wide range of power supply voltages, from the standard $\pm 15.0V$ down to a single $5.0 V$ power supply. A very flexible output stage is employed which is compatible with RTL, DTL, TTL and MOS logic circuits.

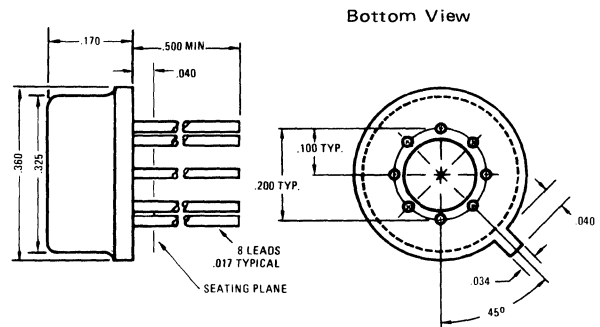
SCHEMATIC



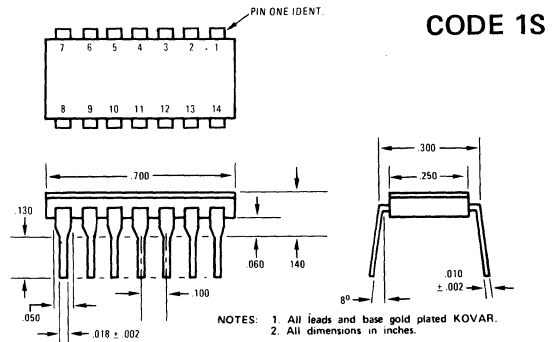
PACKAGES

CODE 2A

TO-99

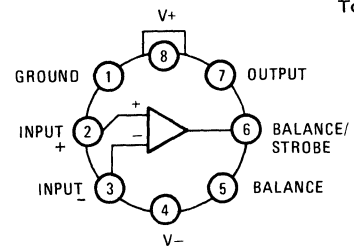


ALL DIMENSIONS ARE IN INCHES.
ALL DIMENSIONS $\pm .010$ UNLESS OTHERWISE SHOWN.



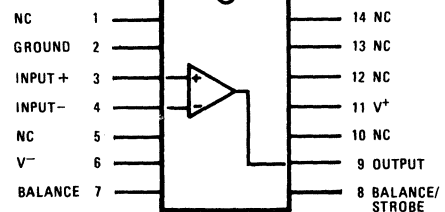
PIN OUT

TO-99



Case Connected to V-

TO-116



Case Connected to V-

LINEAR

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	36.0V
Output to V^-	40.0V
Ground to V^-	30.0V
Differential Input Voltage	$\pm 30.0V$
Input Voltage (Note 1)	$\pm 15.0V$
Internal Power Dissipation	500mW
Output Short Circuit Duration	10 sec.
Storage Temperature Range	$-65^\circ C$ to $+150^\circ C$

ELECTRICAL CHARACTERISTICS

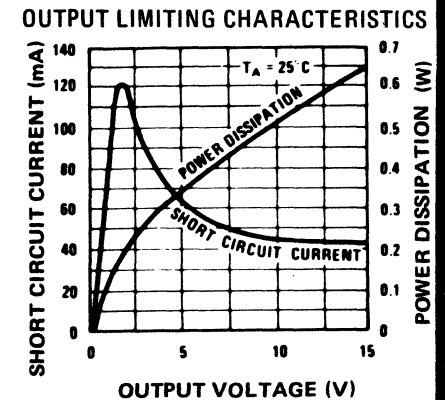
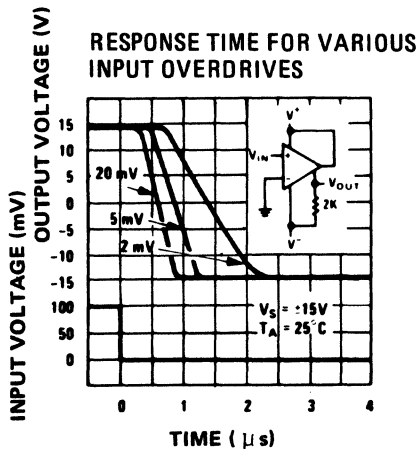
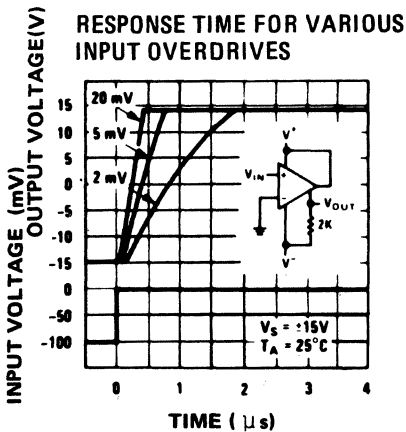
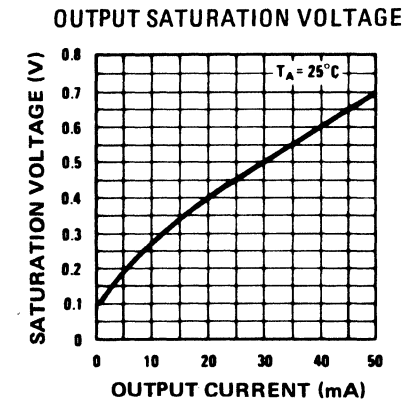
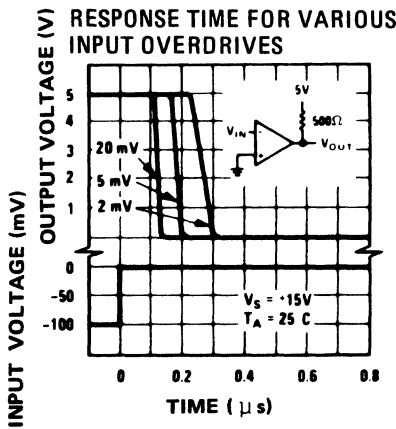
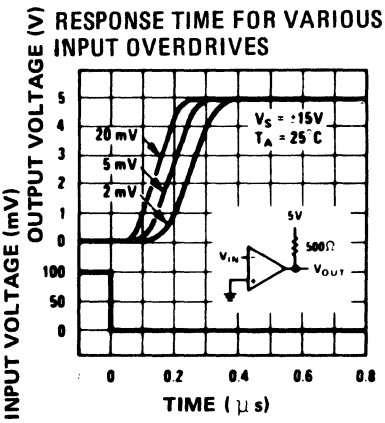
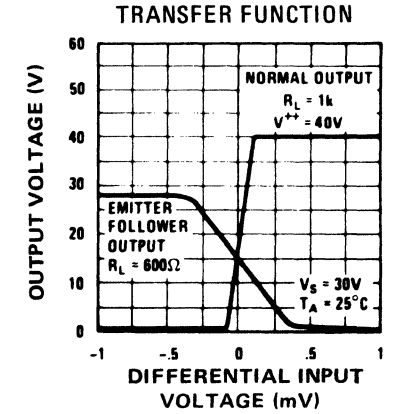
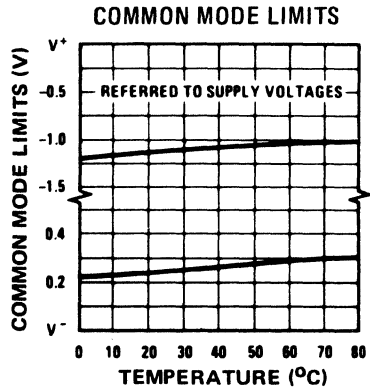
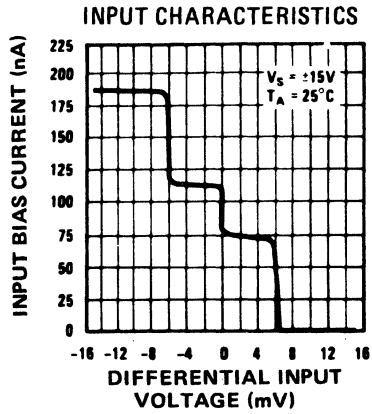
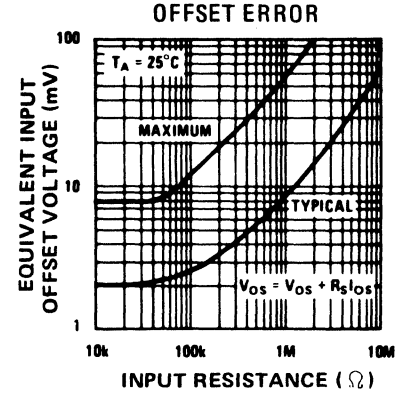
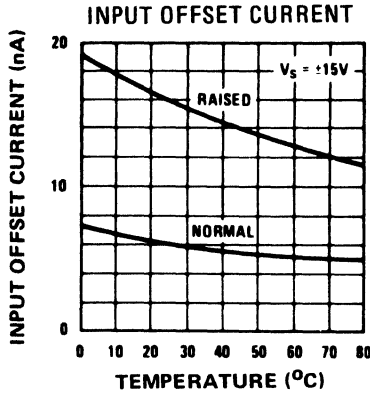
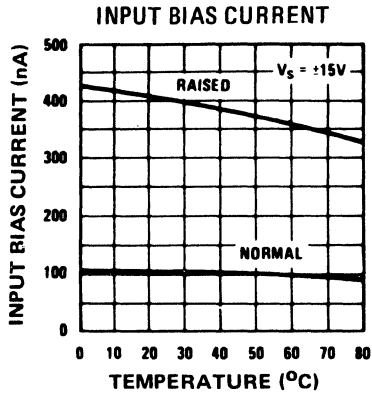
$V^+ = +15.0$ V.D.C.

$V^- = -15.0$ V.D.C.

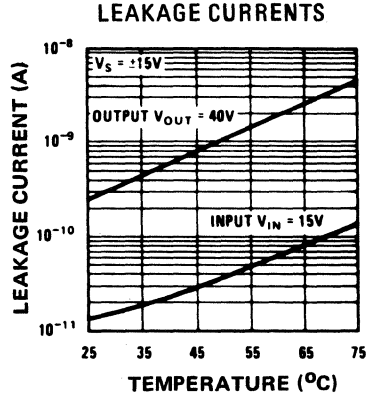
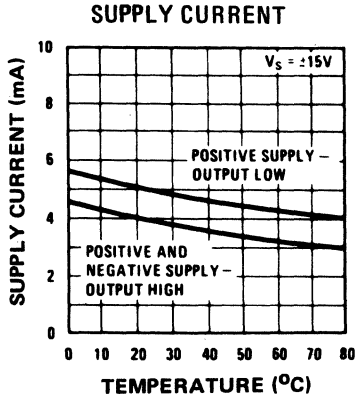
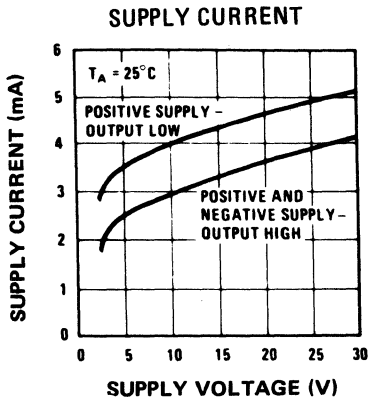
PARAMETER	TEMPERATURE	HA-2311 $0^\circ C$ to $+75^\circ C$			UNITS
		MIN.	TYP.	MAX.	
INPUT CHARACTERISTICS					
Offset Voltage (Note 2)	$+25^\circ C$		2.0	7.5	mV
	$0^\circ C$ to $+75^\circ C$			10.0	mV
Bias Current	$+25^\circ C$		100	250	nA
	$0^\circ C$ to $+75^\circ C$			300	nA
Offset Current (Note 2)	$+25^\circ C$		6.0	50.0	nA
	$0^\circ C$ to $+75^\circ C$			70.0	nA
Common Mode Range	$0^\circ C$ to $+75^\circ C$		± 14.0		V
Strobe Current	$+25^\circ C$		3.0		mA
TRANSFER CHARACTERISTICS					
Large Signal Voltage Gain	$+25^\circ C$		200K		V/V
Response Time (Note 3)	$+25^\circ C$		200		ns
OUTPUT CHARACTERISTICS					
Leakage Current (Note 4)	$+25^\circ C$		0.2	50.0	nA
Saturation Voltage (Note 5) (Note 6)	$+25^\circ C$		0.75	1.5	V
	$0^\circ C$ to $+75^\circ C$		0.23	0.4	V
POWER SUPPLY CHARACTERISTICS					
Positive Supply Current	$+25^\circ C$		5.1	7.5	mA
Negative Supply Current	$+25^\circ C$		4.1	5.0	mA

- NOTES: 1. This rating applies for $\pm 15.0V$ supplies. The positive input voltage limit is 30.0V above the negative supply. The negative input voltage is equal to the negative supply voltage or 30.0V below the positive supply, whichever is less.
2. The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
3. 100mV input step; 5mV overdrive.
4. $V_{OUT} = 35.0V$; $V_{IN} = 10mV$
5. $I_{OUT} = 50mA$; $V_{IN} = -10mV$
6. $I_{SINK} = 8mA$, $V^+ = 4.5V$, $V^- = 0.0V$, $V_{IN}^+ = +1.0V$, $V_{IN}^- = +1.01V$

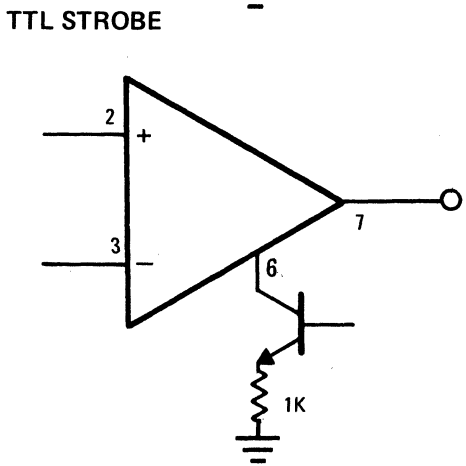
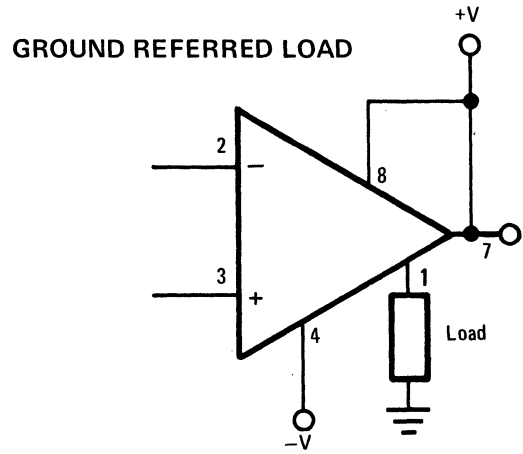
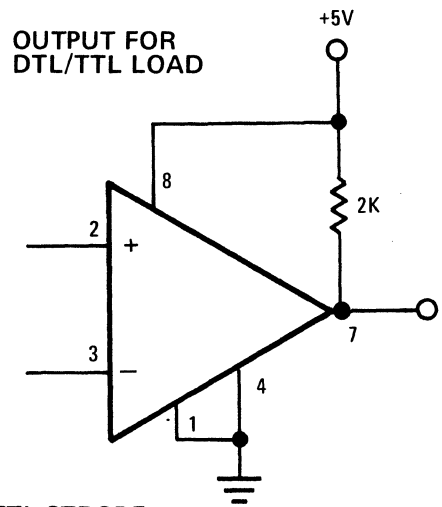
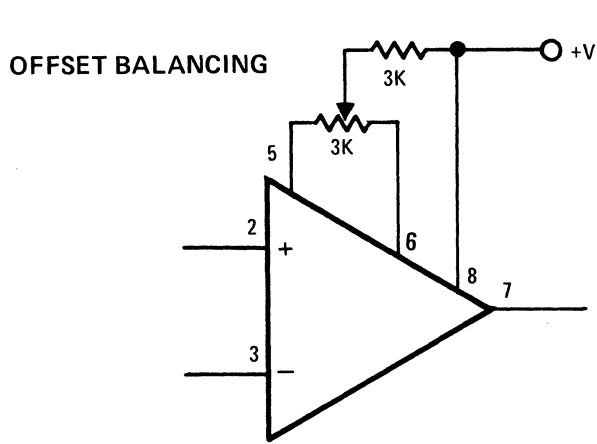
TYPICAL PERFORMANCE CURVES



TYPICAL PERFORMANCE CURVES (continued)

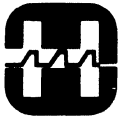


APPLICATION INFORMATION



NOTE: INPUT POLARITIES REVERSED

LINEAR



HARRIS
SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-2400/2404/2405

PRAM™ Four Channel Programmable Amplifier

FEATURES

• THOUSANDS OF NEW APPLICATIONS ; PROGRAM:

- SIGNAL SELECTION/MULTIPLEXING
- OP AMP GAIN
- OSCILLATOR FREQUENCY
- FILTER CHARACTERISTICS
- ADD-SUBTRACT FUNCTIONS
- INTEGRATOR CHARACTERISTICS
- COMPARATOR LEVELS
- ETC., ETC.

- HIGH SLEW RATE 50V/μs
- WIDE GAIN BANDWIDTH 40MHz
- HIGH GAIN 150,000
- LOW OFFSET CURRENT 5nA
- HIGH INPUT IMPEDANCE 30MΩ
- SINGLE CAPACITOR COMPENSATION
- DTL/TTL COMPATIBLE INPUTS

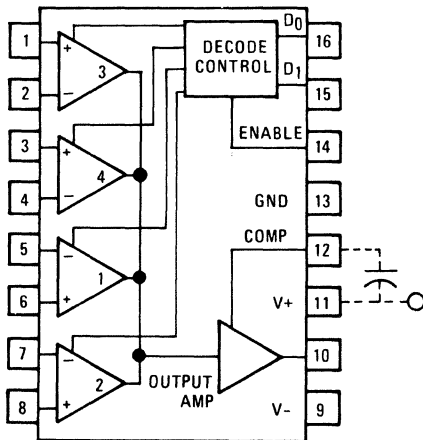
GENERAL DESCRIPTION

The HA-2400 is an operational amplifier with four identical input stages, any one (or none) of which may be electronically connected to the single output stage. The "ON" channel is selected through DTL/TTL compatible address inputs. The amplifier formed by the output and the selected pair of amplifier inputs is a high performance operational amplifier which can be operated with suitable feedback networks in any of the well known op amp configurations. The device is an extremely versatile analog building block. It can be used as an analog signal selector, sampler, or multiplexer with built in buffering or signal conditioning. By connecting different feedback networks from the output to each input pair, it can be used as a single or multiple channel amplifier with programmable feedback characteristics. The device is packaged in a hermetic 16 pin dual in-line package. The HA-2400 operates over the temperature range of -55°C to +125°C, the HA-2404 operates over -25°C to +85°C, while the HA-2405 operates over 0°C to +75°C.

TRUTH TABLE

D ₁	D ₀	EN	SELECTED CHANNEL
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4
X	X	L	NONE

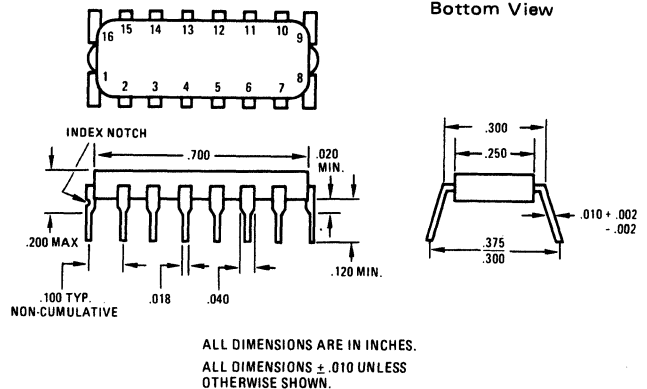
FUNCTIONAL DIAGRAM



PACKAGE

CODE 1F

TO-99



Case Connected to V-

LINEAR

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	45.0V	Internal Power Dissipation (Note 13)	300mW
Differential Input Voltage	$\pm V_{Supply}$	Operating Temperature Range	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$ (HA-2400) $-25^{\circ}C \leq T_A \leq +85^{\circ}C$ (HA-2404) $0^{\circ}C \leq T_A \leq +75^{\circ}C$ (HA-2405)
Digital Input Voltage	-0.76V to +10.0V	Storage Temperature Range	$-65^{\circ}C \leq T_A \leq +150^{\circ}C$
Output Current	Short Circuit Protected		

ELECTRICAL CHARACTERISTICS

Test Conditions: $V_{Supply} = \pm 15.0V$ unless otherwise specified.

Digital inputs: $V_{IL} = +0.5V$, $V_{IH} = +2.4V$
Limits apply to each of the four channels, when addressed.

PARAMETER	TEMP.	HA-2400/HA-2404 LIMITS			HA-2405 LIMITS			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
INPUT CHARACTERISTICS								
* Offset Voltage	+25°C Full		2 7	5		4 11	9	mV mV
* Bias Current (Note 12)	+25°C Full		50	200 400		50 500	250	nA nA
* Offset Current (Note 12)	+25°C Full		5	50 100		5 100	50	nA nA
Input Resistance (Note 12)	+25°C		30			30		M Ω
Common Mode Range	Full	± 10.0			± 10.0			V
TRANSFER CHARACTERISTICS								
* Large Signal Voltage Gain (Note 1,5)	+25°C Full	50K 25K	150K		50K 25K	150K		V/V V/V
* Common Mode Rejection Ratio (Note 2)	Full	80	100		74	100		dB
Gain Bandwidth (Note 3)	+25°C		40			40		MHz
(Note 4)	+25°C		8			8		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 1)	Full	± 10.0	± 12.0		± 10.0	± 12.0		V
Output Current	+25°C		20			20		mA
Full Power Bandwidth (Notes 3, 5)	+25°C		500			500		kHz
(Notes 4,5)	+25°C		200			200		kHz
TRANSIENT RESPONSE								
Rise Time (Notes 4,6)	+25°C		20			20		ns
Overshoot (Notes 4,6)	+25°C		25			25		%
* Slew Rate (Notes 3,7)	+25°C		50			50		V/ μ s
(Notes 4,7)	+25°C		15			15		V/ μ s
Settling Time (Notes 4, 7, 8)	+25°C		1.5			1.5		μ s
CHANNEL SELECT CHARACTERISTICS								
Digital Input Current ($V_{IN} = 0V$)	Full		1			1		mA
Digital Input Current ($V_{IN} = +5.0V$)	Full		5			5		nA
Output Delay (Note 9)	+25°C		100			100		ns
Crosstalk (Note 10)	+25°C	-80	-110		-74	-110		dB
POWER SUPPLY CHARACTERISTICS								
* Supply Current	+25°C		4.8	6.0		4.8	6.0	mA
* Power Supply Rejection Ratio (Note 11)	Full	80	90		74	90		dB

- NOTES: 1. $R_L = 2K\Omega$
2. $V_{CM} = \pm 5$ V.D.C.
3. $A_V = +10$, $C_{COMP} = 0$, $R_L = 2K\Omega$, $C_L = 50pF$
4. $A_V = +1$, $C_{COMP} = 15pF$, $R_L = 2K\Omega$, $C_L = 50pF$
5. $V_{OUT} = 20V$ peak-to-peak
6. $V_{OUT} = 400$ mV peak-to-peak
7. $V_{OUT} = 10.0V$ peak-to-peak

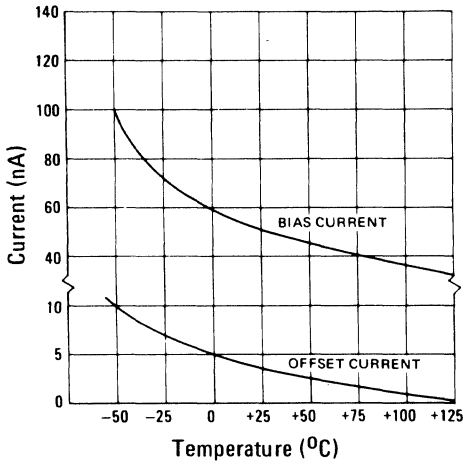
8. To 0.1% of final value
9. To 10% of final value; output then slews at normal rate to final value.
10. Unselected input to output; $V_{IN} = \pm 10$ V.D.C.
11. $V_{SUPP} = \pm 10V$.D.C. to $\pm 20V$.D.C.
12. Unselected channels have approximately the same input parameters.
13. Derate by $4.3mW/^{\circ}C$ above $105^{\circ}C$

*100% Tested For DASH 8

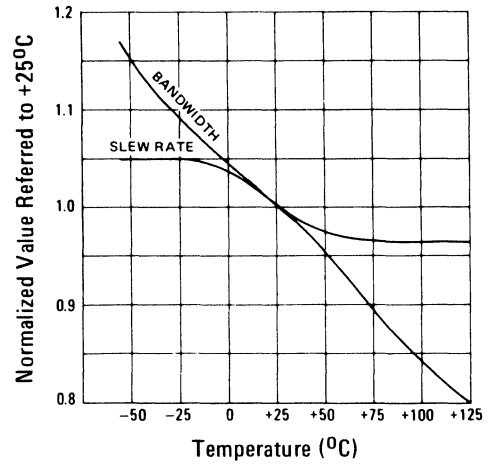
CHARACTERISTIC CURVES

$V_+ = 15\text{VDC}$, $V_- = 15\text{VDC}$, $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE STATED.

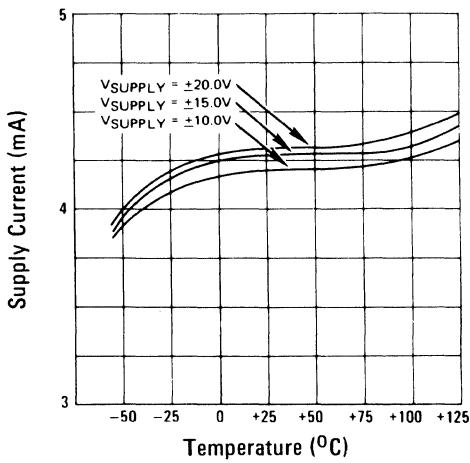
INPUT BIAS CURRENT AND OFFSET CURRENT AS A FUNCTION OF TEMPERATURE



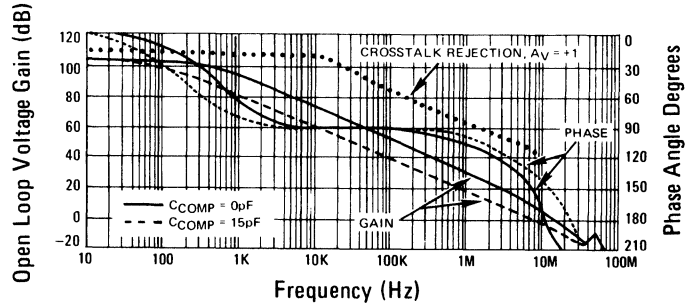
NORMALIZED A.C. PARAMETERS VS. TEMPERATURE



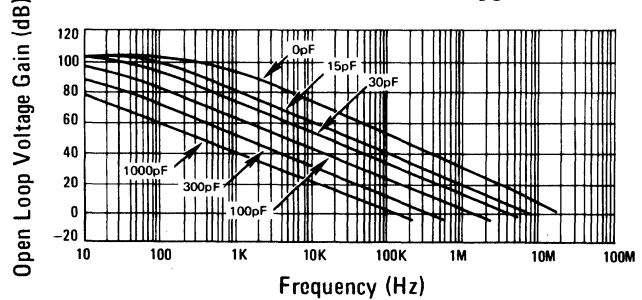
POWER SUPPLY CURRENT DRAIN AS A FUNCTION OF TEMPERATURE



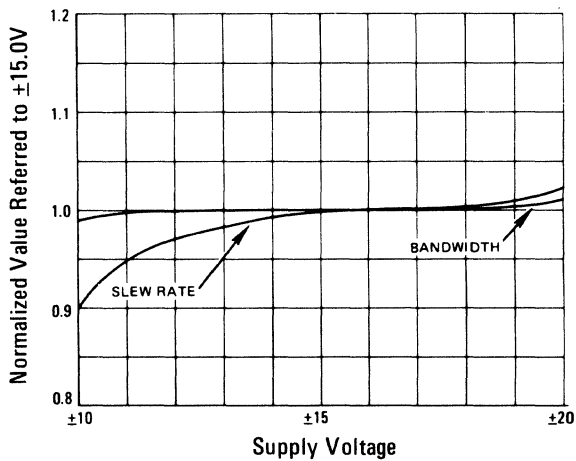
OPEN LOOP FREQUENCY AND PHASE RESPONSE



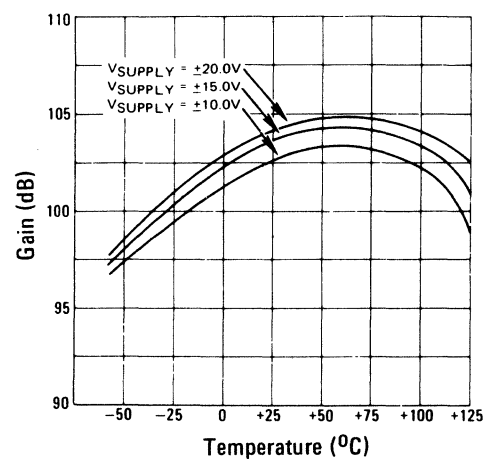
FREQUENCY RESPONSE VS. C_{COMP}



NORMALIZED A.C. PARAMETERS VS. SUPPLY VOLTAGE



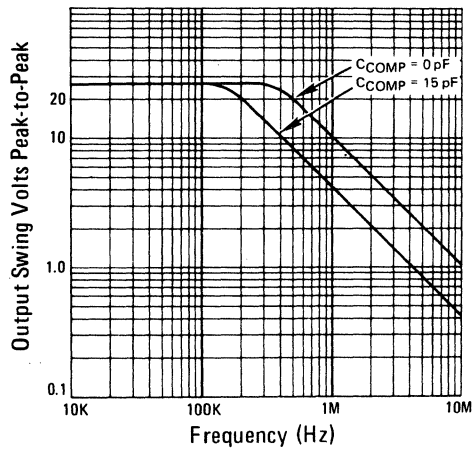
OPEN LOOP VOLTAGE GAIN VS. TEMPERATURE



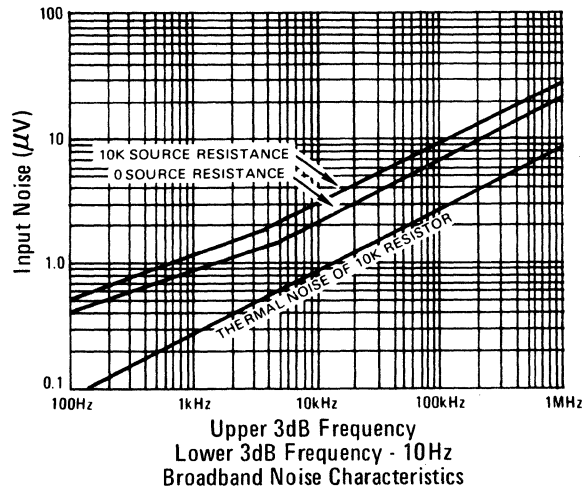
LINEAR

CHARACTERISTIC CURVES (continued)

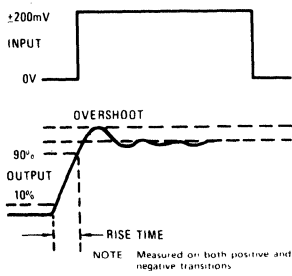
OUTPUT VOLTAGE SWING VS. FREQUENCY



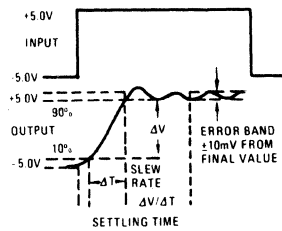
EQUIVALENT INPUT NOISE VS. BANDWIDTH



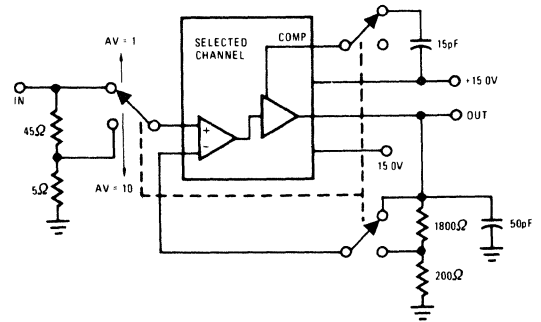
TRANSIENT RESPONSE



SLEW RATE AND SETTLING

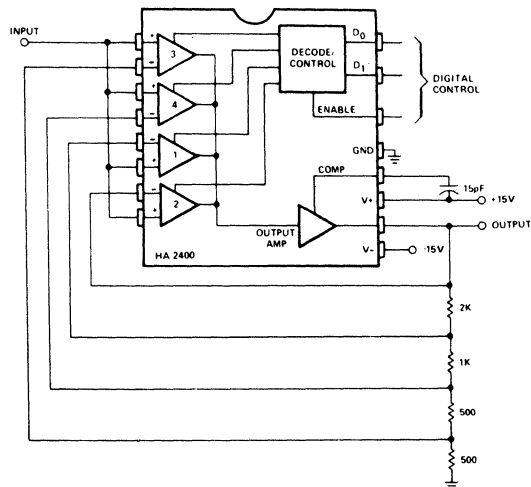


SLEW RATE AND TRANSIENT RESPONSE

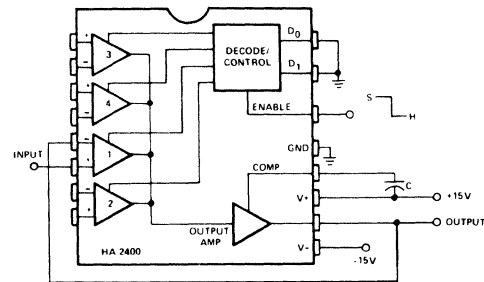


TYPICAL APPLICATIONS

AMPLIFIER, NON-INVERTING PROGRAMMABLE GAIN



SAMPLE AND HOLD



Sample charging rate = $\frac{I_1}{C}$ V/sec.

Hold drift rate = $\frac{I_2}{C}$ V/sec.

Switch pedestal error = $\frac{Q}{C}$ Volts

$I_1 \approx 150 \times 10^{-6}$ A

$I_2 \approx 200 \times 10^{-9}$ A @ +25°C

$\approx 600 \times 10^{-9}$ A @ -55°C

$\approx 100 \times 10^{-9}$ A @ +125°C

$Q \approx 2 \times 10^{-12}$ Coul.

FOR MORE EXAMPLES, SEE HARRIS APPLICATION NOTE 514.



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HA-2420/2425

Sample and Hold Gated Operational Amplifier

LINEAR

FEATURES

- SAMPLE CURRENT/HOLD CURRENT RATIO: 10⁶
- SLEW RATE: 5V/μs
- BANDWIDTH: 2MHz
- APERTURE TIME: 50ns
- LOW CHARGE TRANSFER: 10pC
- CONNECT IN ANY OP AMP CONFIGURATION
- ALSO USE AS GATED OP AMP
- DTL/TTL COMPATIBLE CONTROL INPUT

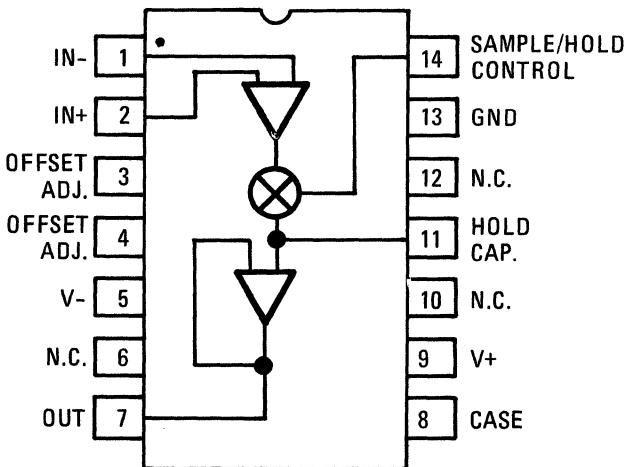
DESCRIPTION

The HA-2420/2425 is a monolithic circuit consisting of a high performance operational amplifier with its output in series with an ultra-low leakage analog switch and a MOSFET input unity gain amplifier.

With an external holding capacitor connected to the switch output, a versatile, high performance sample-and-hold or track-and-hold circuit is formed. When the switch is closed, the device behaves as an operational amplifier, and any of the standard op amp feedback networks may be connected around the device to control gain, frequency response, etc. When the switch is opened the output will remain at its last level.

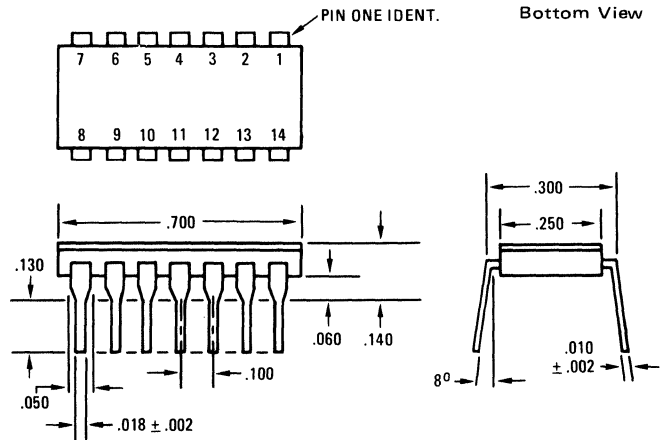
The device may also be used as a versatile operational amplifier with a gated output for applications such as analog switches, peak holding circuits, etc.

FUNCTIONAL DIAGRAM



PACKAGE

CODE 1S 14 LEAD BRAZED D.I.P.



ALL DIMENSIONS IN INCHES.

ALL DIMENSIONS ± .010 UNLESS OTHERWISE SHOWN.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	40V	Internal Power Dissipation	300mW (note 8)
Differential Input Voltage	±30V	Operating Temperature Range	
Digital Input Voltage (Pin 14)	+8V, -15V	HA-2420	-55°C ≤ T _A ≤ +125°C
Output Current	Short Circuit Protected	HA-2425	0°C ≤ T _A ≤ +75°C
		Storage Temperature Range	-65°C ≤ T _A ≤ +150°C

ELECTRICAL CHARACTERISTICS

Test Conditions V_{Supply} = ±15.0V
 C_H = 1000pF Unless Otherwise Specified Digital Input (Pin 14) V_{IL} = +0.8V (Sample)
 V_{IH} = +2.0V (Hold)

PARAMETER	TEMP.	HA-2420 LIMITS			HA-2425 LIMITS			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		2	4		3	6	mV
	Full		3	6		4	8	mV
* Bias Current	+25°C		50	200		50	200	nA
	Full			400			400	nA
Offset Current	+25°C		10	50		10	50	nA
	Full			100			100	nA
Input Resistance	+25°C	5	10		5	10		MΩ
Common Mode Range	Full	±10			±10			V
TRANSFER CHARACTERISTICS								
* Large Signal Voltage Gain (Note 1, 4)	Full	25K	50K		25K	50K		V/V
* Common Mode Rejection (Note 2)	Full	80	90		74	90		dB
Gain Bandwidth Product (Note 3)	+25°C		2			2		MHz
OUTPUT CHARACTERISTICS								
* Output Voltage Swing (Note 1)	Full	±10			±10			V
* Output Current	+25°C	±10			±10			mA
Full Power Bandwidth (Note 3, 4)	+25°C		70			70		kHz
Output Resistance	+25°C		5			5		Ω
TRANSIENT RESPONSE								
Rise Time (Note 3, 5)	+25°C		100			100		ns
Overshoot (Note 3, 5)	+25°C		20			20		%
Slew Rate (Note 3, 6)	+25°C		5			5		V/μs
DIGITAL INPUT CHARACTERISTICS								
Digital Input Current (V _{IN} = 0V)	Full			0.8			0.8	mA
Digital Input Current (V _{IN} = +5.0V)	Full			20			20	μA
Digital Input Voltage (Low)	Full			0.8			0.8	V
Digital Input Voltage (High)	Full	2.0			2.0			V
SAMPLE/HOLD CHARACTERISTICS								
Acquisition Time (Note 3, 7)	+25°C		4			4		μs
Aperture Time	+25°C		50			50		ns
* Drift Current	+25°C		5	50		5	50	pA
	Full		0.5	10		.05	1.0	nA
* Charge Transfer	+25°C		10	20		10	20	pC
POWER SUPPLY CHARACTERISTICS								
* Supply Current	+25°C		2.5	5.0		2.5	5.0	mA
* Power Supply Rejection Ratio	Full	80	90		74	90		dB

NOTES: 1. R_L = 2KΩ
 2. V_{CM} = +5 V.D.C.
 3. A_V = +1, R_L = 2KΩ, C_L = 50pF
 4. V_{OUT} = 20V peak-to-peak

5. V_{OUT} = 400mV peak-to-peak
 6. V_{OUT} = 10.0V peak-to-peak
 7. To 0.1% of final value

8. Derate Power Dissipation by 4.3mW/°C Above +105°C Ambient Temperature.

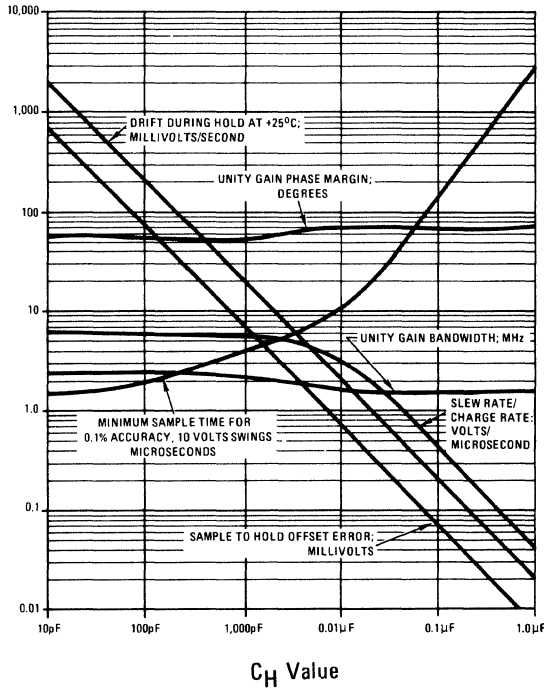
*100% Tested For DASH 8

LINEAR

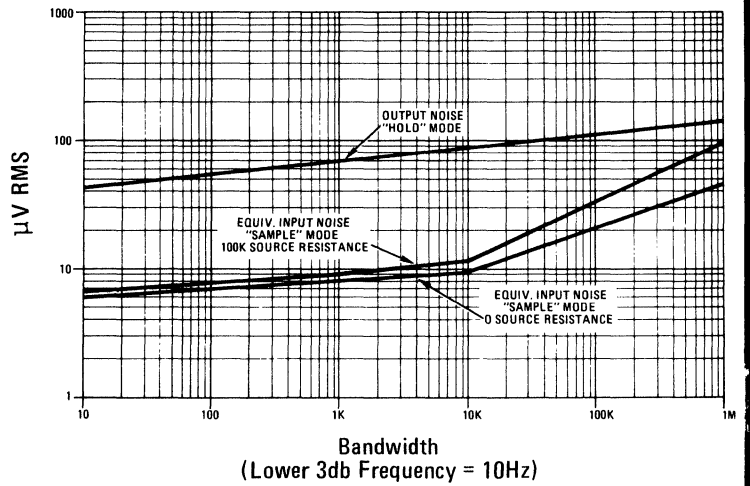
PERFORMANCE CURVES

$V_{SUPPLY} = \pm 15VDC, T_A = +25^{\circ}C, C_H = 1,000pF$ UNLESS OTHERWISE SPECIFIED

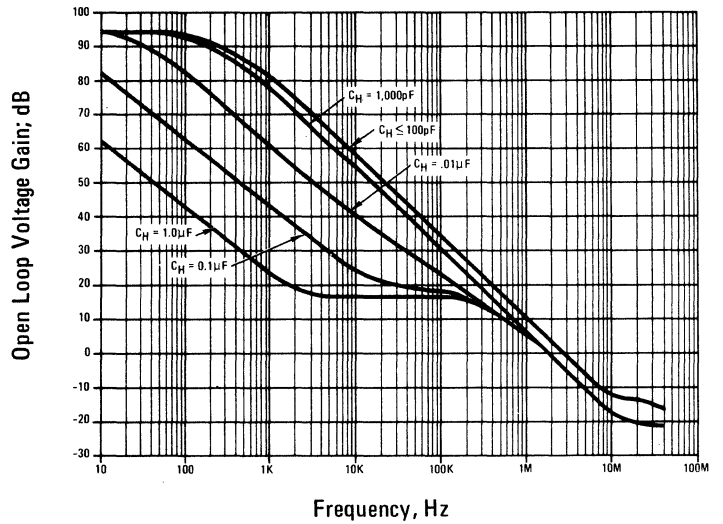
TYPICAL SAMPLE-AND-HOLD PERFORMANCE AS A FUNCTION OF HOLDING CAPACITANCE



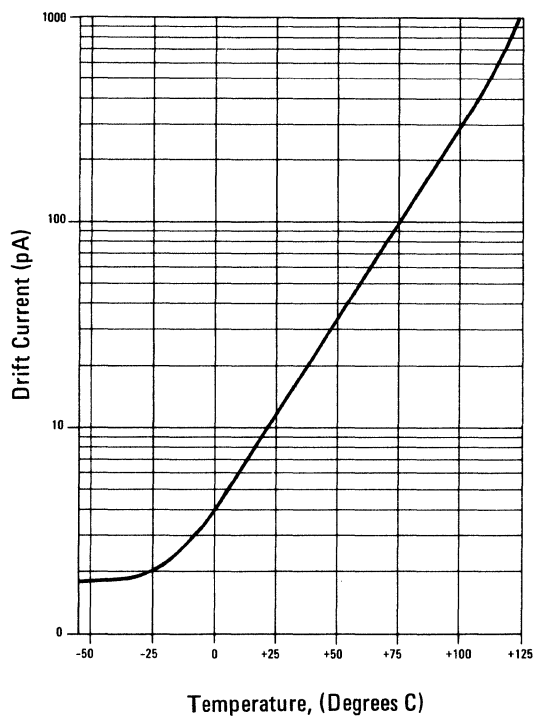
BROADBAND NOISE CHARACTERISTICS



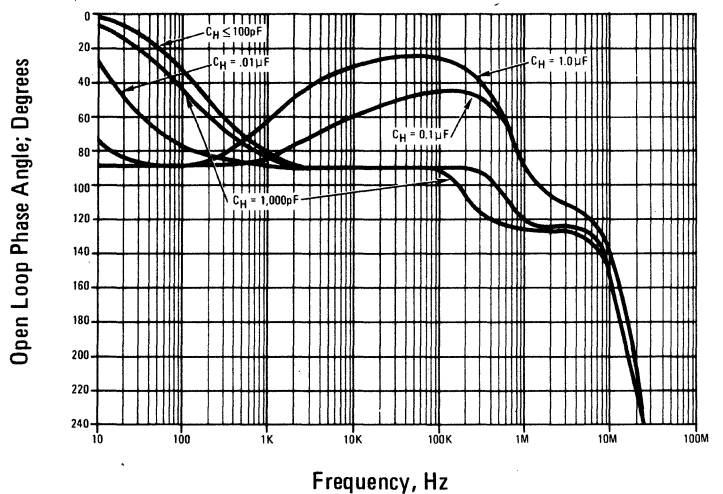
OPEN LOOP FREQUENCY RESPONSE



DRIFT CURRENT vs TEMPERATURE



OPEN LOOP PHASE RESPONSE



LINEAR

APPLICATIONS

BASIC TRACK-AND-HOLD/ SAMPLE-AND-HOLD

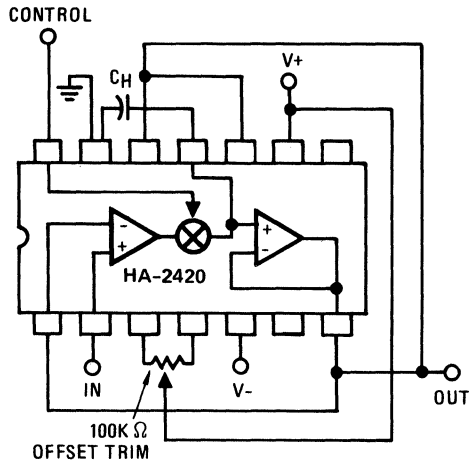


Figure 1

GUARD RING LAYOUT (BOTTOM VIEW)

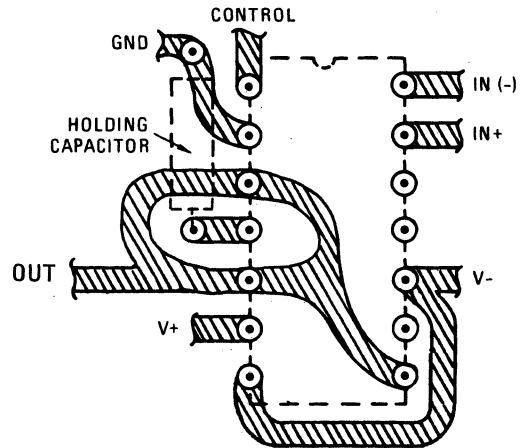


Figure 2

- NOTES: 1) Figure 1 shows a typical unity gain circuit, with offset zeroing. All of the other normal op amp feedback configurations may be used with the HA-2420/2425. The input amplifier may be used as a gated amplifier by utilizing Pin 11 as the output. This amplifier has excellent drive capabilities along with exceptionally low switch leakage.
- 2) The method used to reduce leakage paths on the P.C. board and the device package is shown in Figure 2. This guard ring is recommended to minimize the drift during hold characteristic.
- 3) The holding capacitor should have extremely high insulation resistance and low dielectric absorption. Polystyrene (below +85°C), Teflon, or Mica types are recommended.

For more applications, consult Harris Application Note 517.

GLOSSARY OF TERMS

AQUISITION TIME:

The time required by the device after the "sample" command to reach its final value within $\pm 0.1\%$. This time includes switch delay time, slewing time and settling time. This is the minimum sample time required to obtain a given accuracy.

CHARGE TRANSFER:

The small charge transferred to the holding capacitor from the inter-electrode capacitance of the switch when the unit is switched to the Hold mode. Sample-to-Hold offset error is directly proportional to this charge, where:

$$\text{Offset Error (V)} = \frac{\text{Charge (pC)}}{C_H(\text{pF})}$$

APERTURE TIME:

The time required after the "hold" command until the switch is fully open. This delays the effective sample timing with rapidly changing input signals.

DRIFT CURRENT:

Leakage currents from the holding capacitor during the Hold mode which cause the output voltage to drift. Drift rate (droop rate) can be calculated from drift current values using the formula:

$$\frac{\Delta V}{\Delta T} (\text{Volts/Sec}) = \frac{I(\text{pA})}{C_H(\text{pF})}$$



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HA-2500/2502/2505

High Slew Rate Operational Amplifiers

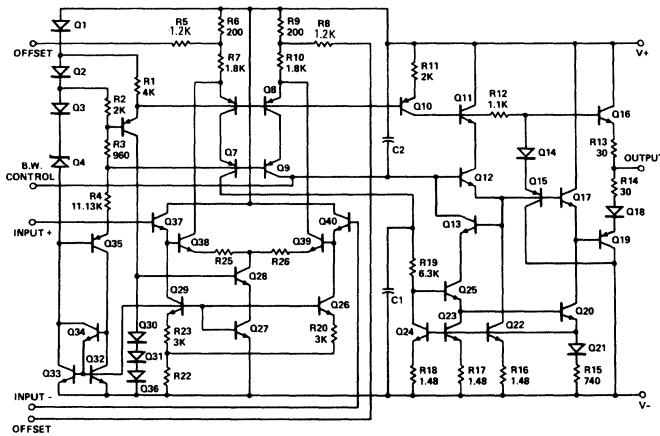
FEATURES

- HIGH SLEW RATE 30V/ μ s
- FAST SETTLING 330ns
- WIDE POWER BANDWIDTH 500kHz
- HIGH GAIN BANDWIDTH 12MHz
- HIGH INPUT IMPEDANCE 100m Ω
- LOW OFFSET CURRENT 10nA
- TRUE OP-AMP - CAN BE OPERATED NON-INVERTING OR INVERTING
- MEETS OR EXCEEDS MIL-STD-883 REQUIREMENTS

GENERAL DESCRIPTION

An operational amplifier with excellent D.C. characteristics, featuring high slew rate and fast settling time. Ideal for use in A/D, D/A, and sampled data systems; and for use in wide band R.F. or video systems where wide bandwidth at high output levels is required. The HA-2500/02/05 is internally compensated.

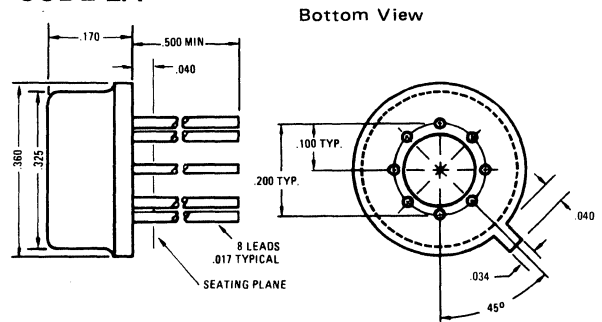
SCHEMATIC



PACKAGES

CODE 2A

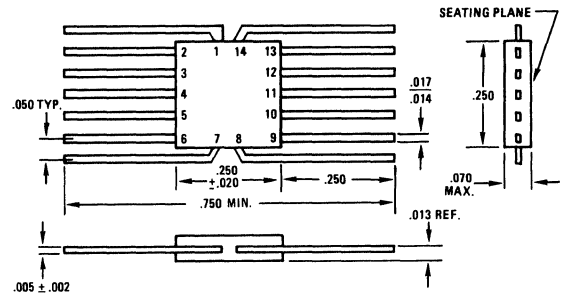
T0-99



NOTES: 1. All leads gold plated KOVAR
2. All dimensions in inches

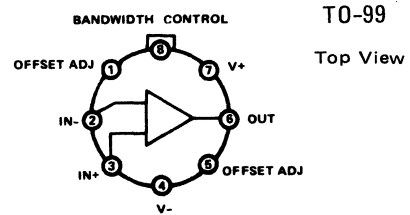
CODE 9V

(METAL BOTTOM) T0-86

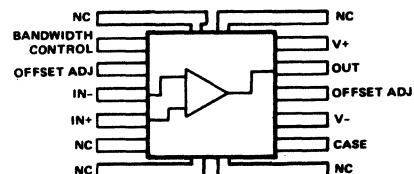


ALL DIMENSIONS ARE IN INCHES.
ALL DIMENSIONS \pm .010 UNLESS OTHERWISE SHOWN.

PIN OUT



T0-86



LINEAR

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V ⁺ and V ⁻ Terminals	40.0V	Operating Temperature Range –	HA-2500/HA-2502	-55°C ≤ T _A ≤ +125°C
Differential Input Voltage	±15.0V		HA-2505	0°C ≤ T _A ≤ +75°C
Peak Output Current	50mA	Storage Temperature Range		-65°C ≤ T _A ≤ +150°C
Internal Power Dissipation	300mW			

ELECTRICAL CHARACTERISTICS

V⁺ = +15V D.C., V⁻ = -15V D.C.

PARAMETER	TEMP.	HA-2500 -55°C to +125°C			HA-2502 -55°C to +125°C			HA-2505 0°C to +75°C			UNITS
		LIMITS			LIMITS			LIMITS			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
INPUT CHARACTERISTICS											
* Offset Voltage	+25°C Full		2	5 8		4	8 10		4	8 10	mV mV
Offset Voltage Average Drift	Full		20			20			20		μV/°C
* Bias Current	+25°C Full		100	200 400		125	250 500		125	250 500	nA nA
* Offset Current	+25°C Full		10	25 50		20	50 100		20	50 100	nA nA
Input Resistance	+25°C	25	50		20	50		20	50		MΩ
Common Mode Range	Full	±10.0			±10.0			±10.0			V
TRANSFER CHARACTERISTICS											
* Large Signal Voltage Gain (Note 1,4)	+25°C Full	20K 15K	30K		15K 10K	25K		15K 10K	25K		V/V V/V
* Common Mode Rejection Ratio (Note 2)	Full	80	90		74	90		74	90		dB
Gain Bandwidth Product (Note 3)	+25°C		12			12			12		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
* Output Current (Note 4)	+25°C	±10	±20		±10	±20		±10	±20		mA
Full Power Bandwidth (Note 4)	+25°C	350	500		300	500		300	500		kHz
TRANSIENT RESPONSE											
Rise Time (Notes 1, 5, 6 & 8)	+25°C		25	50		25	50		25	50	ns
Overshoot (Notes 1, 5, 7 & 8)	+25°C		25	40		25	50		25	50	%
* Slew Rate (Notes 1,4,5 & 8)	+25°C	±25	±30		±20	±30		±20	±30		V/μs
Settling Time to 0.1% (Notes 1,4,5 & 8)	+25°C		0.33			0.33			0.33		μs
POWER SUPPLY CHARACTERISTICS											
* Supply Current	+25°C		4	6		4	6		4	6	mA
* Power Supply Rejection Ratio (Note 9)	Full	80	90		74	90		74	90		dB

- NOTES: 1. R_L = 2K
 2. V_{CM} = ±5.0V
 3. A_V > 10
 4. V_O = ±10.0V
 5. C_L = 50pF
 6. V_O = ±400mV

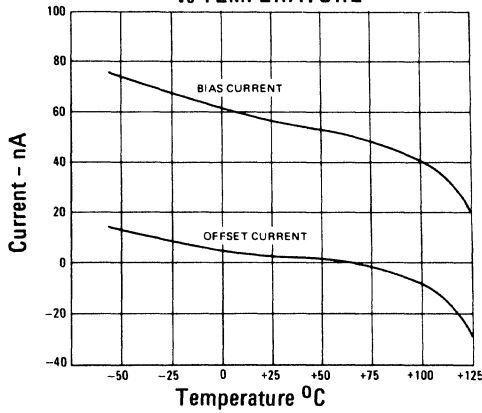
7. V_O = ±600mV
 8. See transient response test circuits and waveforms page four.
 9. ΔV = ±5.0V

* 100% Tested For DASH 8

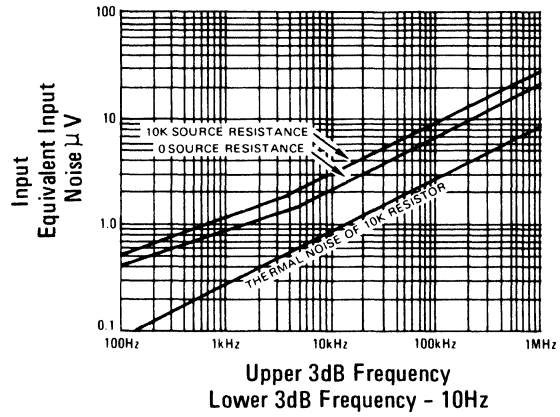
PERFORMANCE CURVES

V+ = 15VDC, V- = 15VDC, T_A = 25°C UNLESS OTHERWISE STATED

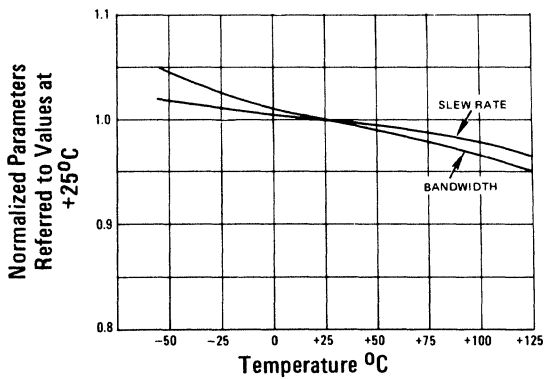
INPUT BIAS AND OFFSET CURRENT vs TEMPERATURE



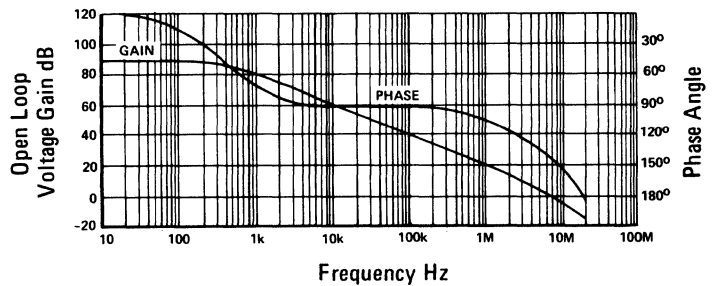
EQUIVALENT INPUT NOISE vs BANDWIDTH



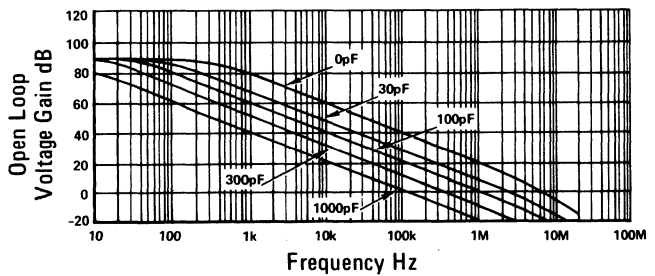
NORMALIZED AC PARAMETERS vs TEMPERATURE



OPEN-LOOP FREQUENCY AND PHASE RESPONSE

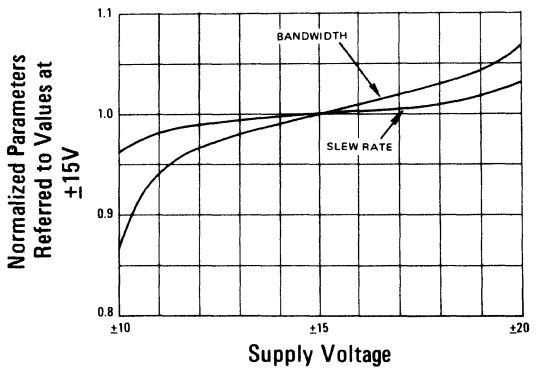


OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM BANDWIDTH CONTROL PIN TO GROUND

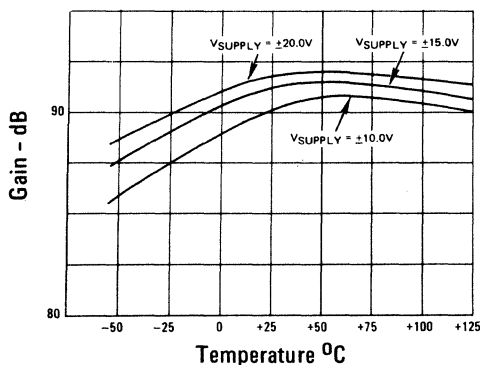


NOTE: External compensation components are not required for stability, but may be added to reduce bandwidth if desired.

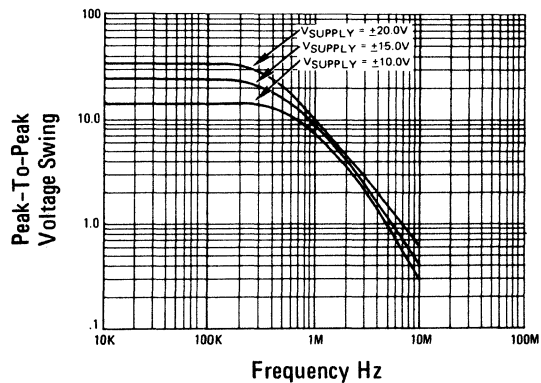
NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE AT +25°C



OPEN LOOP VOLTAGE GAIN vs TEMPERATURE



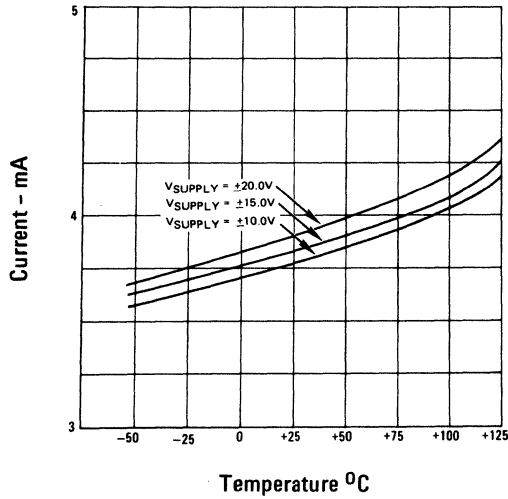
OUTPUT VOLTAGE SWING vs FREQUENCY AT +25°C



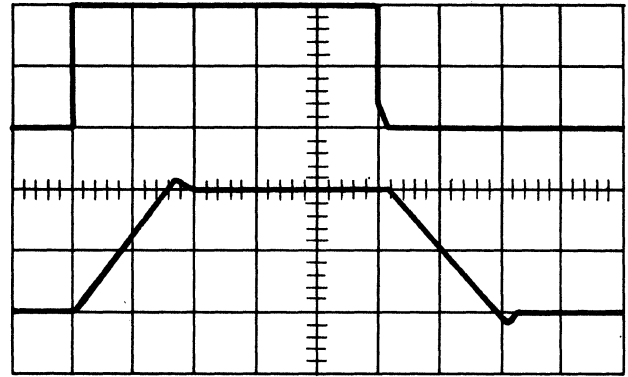
LINEAR

PERFORMANCE CURVES (continued)

POWER SUPPLY CURRENT
vs TEMPERATURE



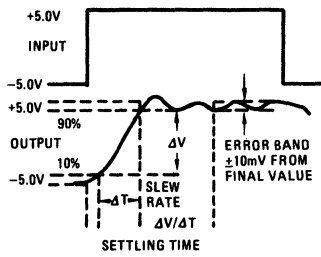
VOLTAGE FOLLOWER PULSE RESPONSE



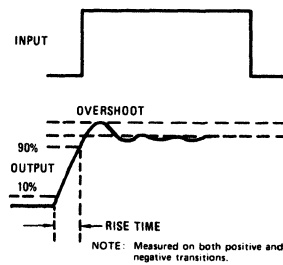
$R_L = 2K\Omega, C_L = 50pF$
 Upper Trace: Input
 Lower Trace: Output

Vertical = 5V/Div.
 Horizontal = 200ns/Div.
 $T_A = +25^\circ C, V_S = \pm 15.0V$

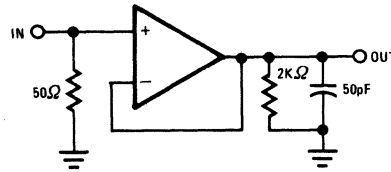
SLEW RATE AND
SETTLING TIME



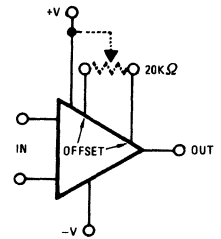
TRANSIENT RESPONSE



SLEW RATE AND
TRANSIENT RESPONSE



SUGGESTED
OFFSET ZERO
ADJUST HOOK-UP



DEFINITIONS

INPUT OFFSET VOLTAGE—That voltage which must be applied between the input terminals through two equal resistances to force the output voltage to zero.

INPUT OFFSET CURRENT—The difference in the currents into the two input terminals when the output is at zero voltage.

INPUT BIAS CURRENT—The average of the currents flowing into the input terminals when the output is at zero voltage.

INPUT COMMON MODE VOLTAGE—The average referred to ground of the voltages at the two input terminals.

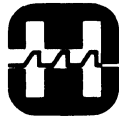
COMMON MODE RANGE—The range of voltages which is exceeded at either input terminal will cause the amplifier to cease operating.

TRANSIENT RESPONSE—The closed loop step function response of the amplifier under small signal conditions.

GAIN BANDWIDTH PRODUCT—The product of the gain and the bandwidth at a given gain.

SLEW RATE (Rating Limiting)—The rate at which the output will move between full scale stops, measured in terms of volts per unit time. This limit to an ideal step function response is due to the non-linear behavior in an amplifier due to its limited ability to produce large, rapid changes in output voltage (slewing)...restricting it to rates of change of voltage lower than might be predicted by observing the small signal frequency response.

SETTLING TIME—Time required for output waveform to remain within 0.1 percent of final value.



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HA-2510/2512/2515

High Slew Rate Operational Amplifiers

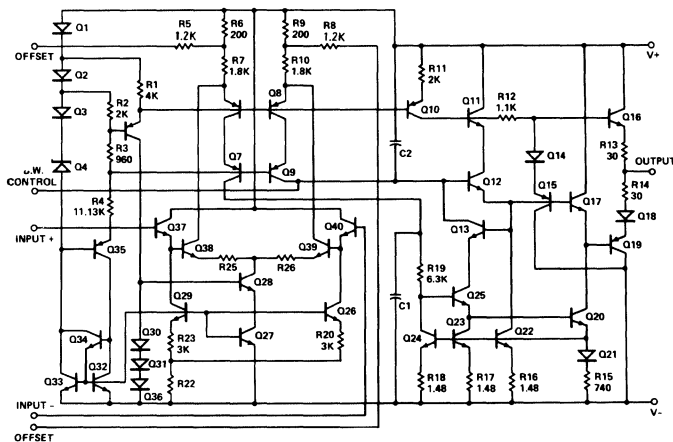
FEATURES

- HIGH SLEW RATE 60V/ μ s
- FAST SETTLING 250ns
- WIDE POWER BANDWIDTH 1,000 kHz
- HIGH GAIN BANDWIDTH 12 MHz
- HIGH INPUT IMPEDANCE 100m Ω
- LOW OFFSET CURRENT 10nA
- TRUE OP AMP – CAN BE OPERATED
NON-INVERTING OR INVERTING
- MEETS OR EXCEEDS MIL-STD-883 REQUIREMENTS

GENERAL DESCRIPTION

An operational amplifier with excellent D.C. characteristics, featuring high slew rate and fast settling time. Ideal for use in A/D, D/A and sampled data systems; and for use in wide band R.F. or video systems where wide bandwidth at high output levels is required. The HA-2510/12/15 is internally compensated.

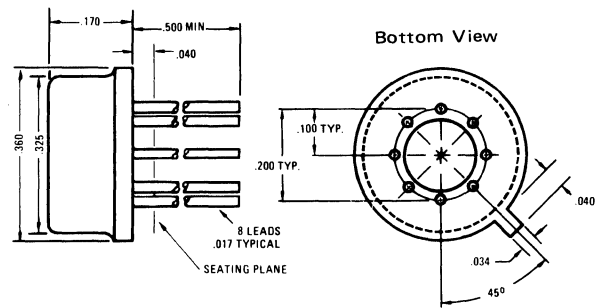
SCHEMATIC



PACKAGES

CODE 2A

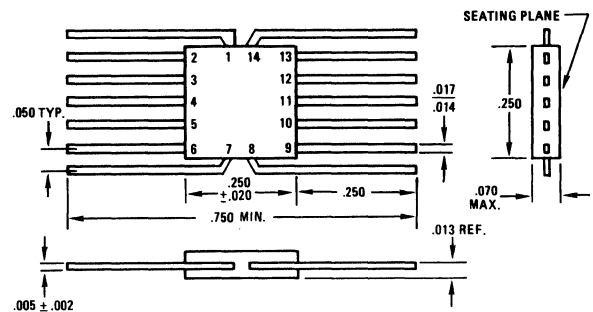
T0-99



NOTES: 1. All leads gold plated KOVAR
2. All dimensions in inches

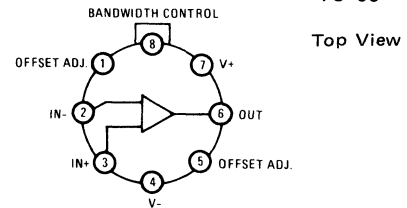
CODE 9V

T0-86 (METAL BOTTOM)



ALL DIMENSIONS ARE IN INCHES.
ALL DIMENSIONS \pm .010 UNLESS
OTHERWISE SHOWN.

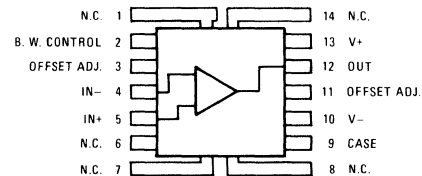
PIN OUT



T0-99

Top View

T0-86



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V ⁺ and V ⁻ Terminals	40.0V	Peak Output Current	50mA
Differential Input Voltage	±15.0V	Internal Power Dissipation	300mW
Operating Temperature Range		Storage Temperature Range	-65°C ≤ T _A ≤ +150°C
HA-2510/HA-2512	-55°C ≤ T _A ≤ +125°C		
HA-2515	0°C ≤ T _A ≤ +75°C		

ELECTRICAL CHARACTERISTICS

V⁺ = +15V D.C., V⁻ = 15V D.C.

PARAMETER	TEMP.	HA-2510 -55°C to +125°C			HA-2512 -55°C to +125°C			HA-2515 0°C to +75°C			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
INPUT CHARACTERISTICS											
* Offset Voltage	+25°C Full		4 8	11		5 10	14		5 10	14	mV mV
Offset Voltage Average Drift	Full		20			25			30		μV/°C
* Bias Current	+25°C Full		100 200	400		125 250	500		125 250	500	nA nA
* Offset Current	+25°C Full		10 25	50		20 50	100		20 50	100	nA nA
Input Resistance	+25°C	50	100		40	100		40	100		MΩ
Common Mode Range	Full	±10.0			±10.0			±10.0			V
TRANSFER CHARACTERISTICS											
* Large Signal Voltage Gain (Note 1,4)	+25°C Full	10K 7.5K	15K		7.5K 5K	15K		7.5K 5K	15K		V/V V/V
* Common Mode Rejection Ratio (Note 2)	Full	80	90		74	90		74	90		dB
Gain Bandwidth Product (Note 3)	+25°C		12			12			12		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
* Output Current (Note 4)	+25°C	±10	±20		±10	±20		±10	±20		mA
Full Power Bandwidth (Note 4)	+25°C	750	1000		600	1000		600	1000		kHz
TRANSIENT RESPONSE											
Rise Time (Notes 1, 5, 6 & 8)	+25°C		25	50		25	50		25	50	ns
Overshoot (Notes 1, 5, 7 & 8)	+25°C		25	40		25	50		25	50	%
* Slew Rate (Notes 1, 4, 5 & 8)	+25°C	±50	±65		±40	±60		±40	±60		V/μs
Settling Time (Notes 1, 4, 5 & 8)	+25°C		0.25			0.25			0.25		μs
POWER SUPPLY CHARACTERISTICS											
* Supply Current	+25°C		4	6		4	6		4	6	mA
* Power Supply Rejection Ratio (Note 9)	Full	80	90		74	90		74	90		dB

NOTES: 1. R_L = 2K
 2. V_{CM} = ±5.0V
 3. A_V > 10
 4. V_O = ±10.0V
 5. C_L = 50pF
 6. V_O = ±400mV

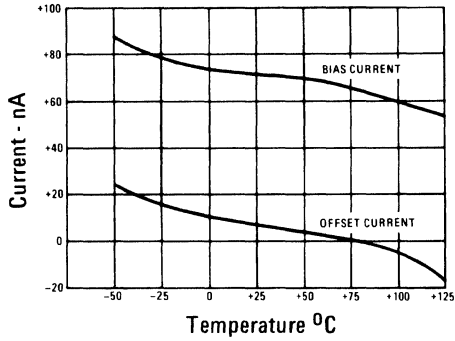
7. V_O = ±600mV
 8. See transient response test circuits and waveforms page four.
 9. ΔV = ±5.0V

*100% Tested For DASH 8

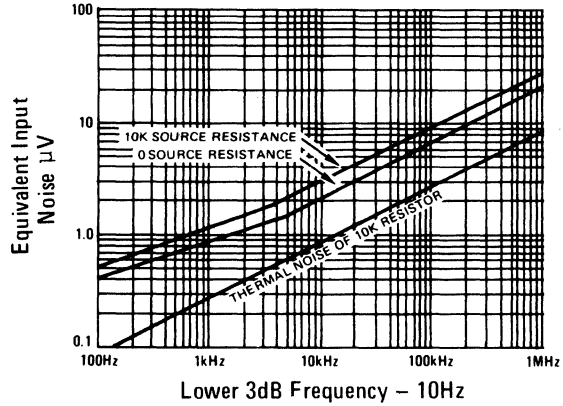
PERFORMANCE CURVES

V+ = 15VDC, V- = 15VDC, T_A = 25°C UNLESS OTHERWISE STATED.

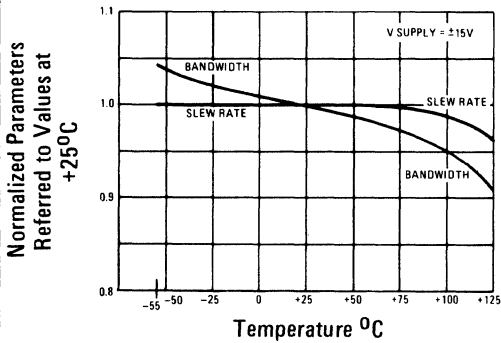
INPUT BIAS AND OFFSET CURRENT vs TEMPERATURE



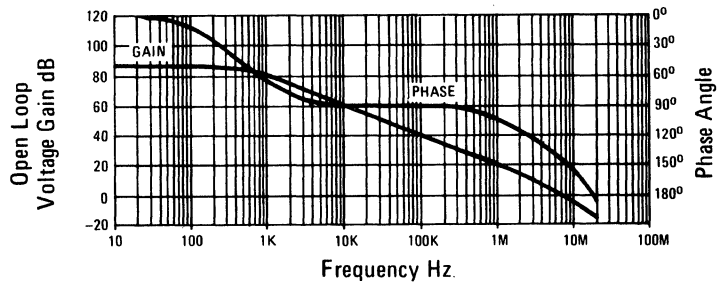
EQUIVALENT INPUT NOISE vs BANDWIDTH



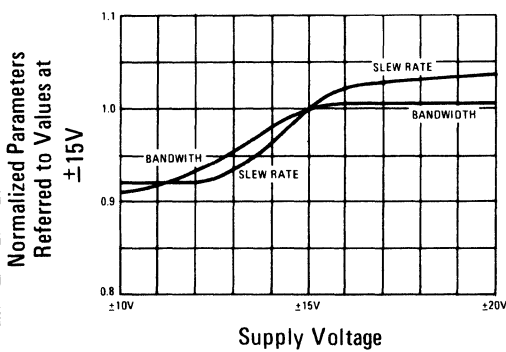
NORMALIZED AC PARAMETERS vs TEMPERATURE



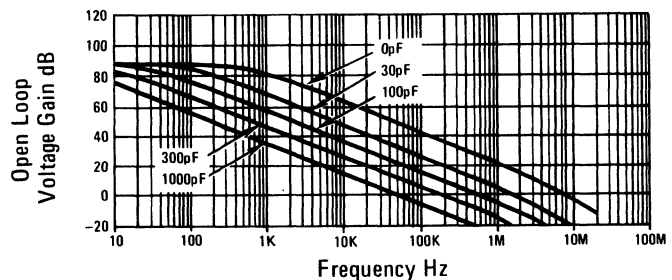
OPEN LOOP FREQUENCY AND PHASE RESPONSE



NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE

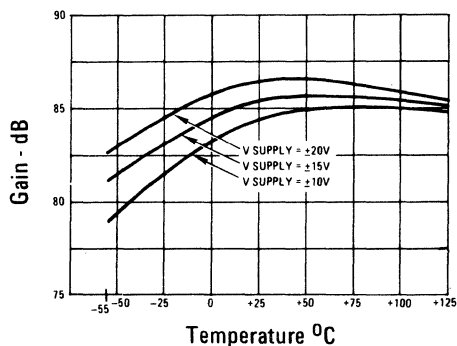


OPEN-LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM BANDWIDTH CONTROL PIN TO GROUND

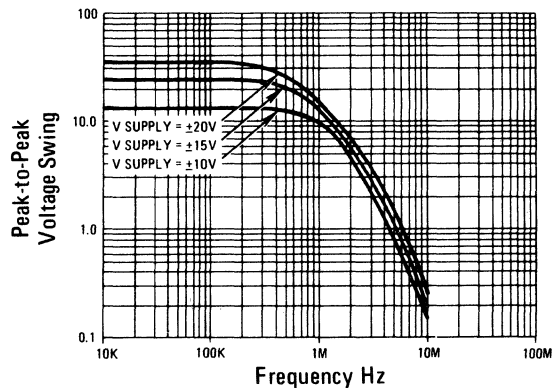


NOTE: External compensation components are not required for stability, but may be added to reduce bandwidth if desired.

OPEN LOOP VOLTAGE GAIN vs TEMPERATURE



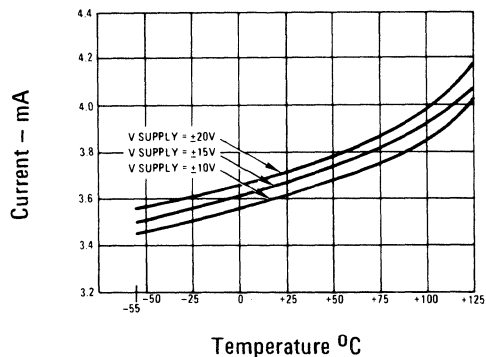
OUTPUT VOLTAGE SWING vs FREQUENCY AT +25°C



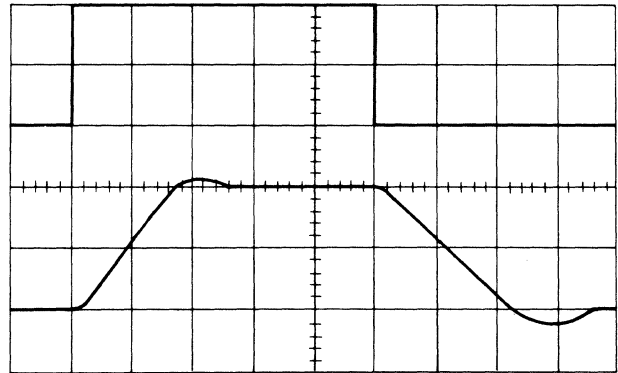
LINEAR

PERFORMANCE CURVES (continued)

POWER SUPPLY CURRENT
VS
TEMPERATURE



VOLTAGE FOLLOWER PULSE RESPONSE

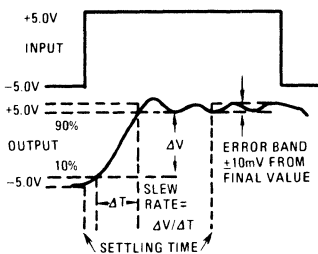


$R_L = 2K \Omega$, $C_L = 50pF$
Upper Trace: Input
Lower Trace: Output

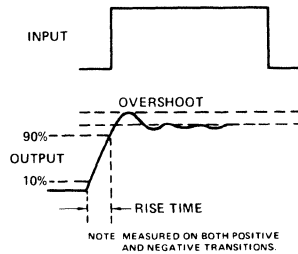
Vertical = 5V/Div.
Horizontal = 100n/Div.
 $T_A = +25^\circ C$, $V_S = \pm 15.0V$

LINEAR

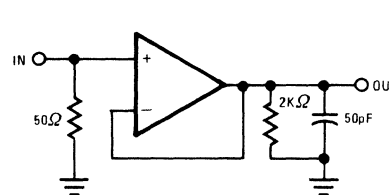
SLEW RATE AND
SETTLING TIME



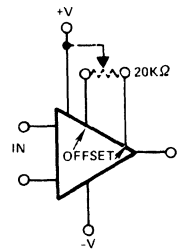
TRANSIENT
RESPONSE



SLEW RATE AND
TRANSIENT RESPONSE



SUGGESTED
OFFSET ZERO
ADJUST HOOK-UP



DEFINITIONS

INPUT OFFSET VOLTAGE—That voltage which must be applied between the input terminals through two equal resistances to force the output voltage to zero.

INPUT OFFSET CURRENT—The difference in the currents into the two input terminals when the output is at zero voltage.

INPUT BIAS CURRENT—The average of the currents flowing into the input terminals when the output is at zero voltage.

INPUT COMMON MODE VOLTAGE—The average referred to ground of the voltages at the two input terminals.

COMMON MODE RANGE—The range of voltages which is exceeded at either input terminal will cause the amplifier to cease operating.

COMMON MODE REJECTION RATIO—The ratio of a specified range of input common mode voltage to the peak-to-peak change in input offset voltage over this range.

OUTPUT VOLTAGE SWING—The peak symmetrical output voltage swing, referred to ground, that can be obtained without clipping.

INPUT RESISTANCE—The ratio of the change in input voltage to the change in input current.

OUTPUT RESISTANCE—The ratio of the change in output voltage to the change in output current.

VOLTAGE GAIN—The ratio of the change in output voltage to the change in input voltage producing it.

UNITY GAIN BANDWIDTH—The frequency at which the voltage gain of the amplifier is unity.



HARRIS
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HA-2520/2522/2525

High Slew Rate Operational Amplifiers

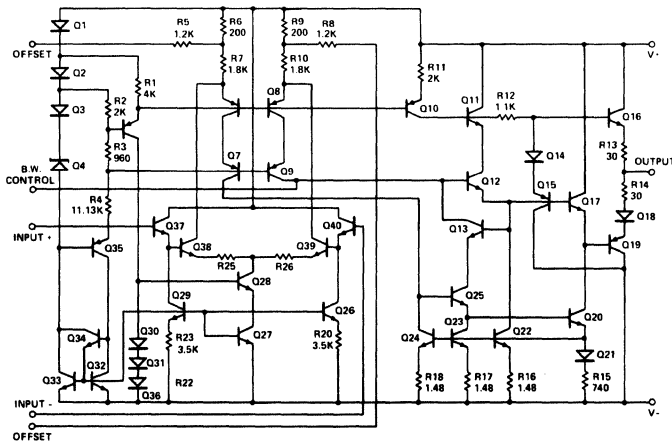
FEATURES

- HIGH SLEW RATE 120V/ μ s
- FAST SETTLING 200ns
- WIDE POWER BANDWIDTH 2,000 kHz
- HIGH GAIN BANDWIDTH 20 MHz
- HIGH INPUT IMPEDANCE 100m Ω
- LOW OFFSET CURRENT 10nA
- TRUE OP AMP – CAN BE OPERATED NON-INVERTING OR INVERTING
- MEETS OR EXCEEDS MIL-STD-883 REQUIREMENTS

GENERAL DESCRIPTION

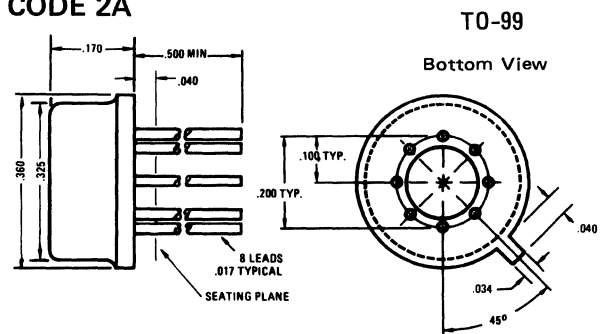
An operational amplifier with excellent D.C. characteristics, featuring high slew rate and fast settling time. Ideal for use in A/D, D/A and sampled data systems; and for use in wide band R.F. or video systems where wide bandwidth at high output levels is required. The HA-2520/22/25 is stable for closed loop gains greater than 3 without external compensation.

SCHEMATIC



PACKAGES

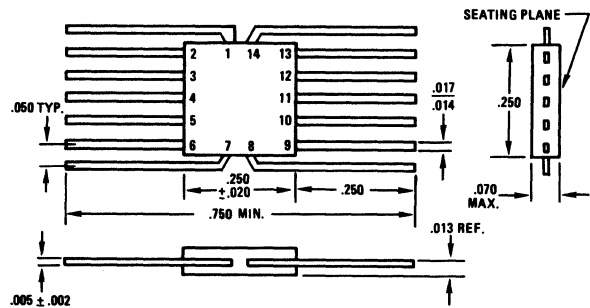
CODE 2A



NOTES: 1. All leads gold plated KOVAR
2. All dimensions in inches

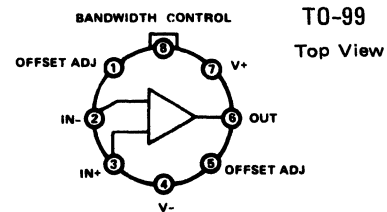
CODE 9V

TO-86 (METAL BOTTOM)

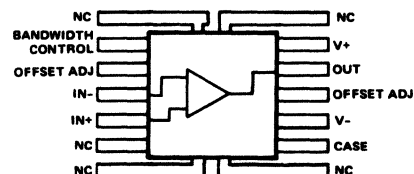


ALL DIMENSIONS ARE IN INCHES.
ALL DIMENSIONS \pm .010 UNLESS OTHERWISE SHOWN.

PIN OUT



TO-86



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V ⁺ and V ⁻ Terminals	40.0V	Peak Output Current	50mA
Differential Input Voltage	±15.0V	Internal Power Dissipation	300mW
Operating Temperature Range		Storage Temperature Range	-65°C ≤ T _A ≤ +150°C
HA-2520/2522	-55°C ≤ T _A ≤ +125°C		
HA-2525	0°C ≤ T _A ≤ +75°C		

ELECTRICAL CHARACTERISTICS

V⁺ = +15V D.C., V⁻ = -15V D.C.

PARAMETER	TEMP.	HA-2520 -55°C to +125°C			HA-2522 -55°C to +125°C			HA-2525 0°C to +75°C			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
INPUT CHARACTERISTICS											
* Offset Voltage	+25°C		4	8		5	10		5	10	mV
	Full			11			14			14	mV
Offset Voltage Average Drift	Full		20			25			30		μV/°C
* Bias Current	+25°C		100	200		125	250		125	250	nA
	Full			400			500			500	nA
* Offset Current	+25°C		10	25		20	50		20	50	nA
	Full			50			100			100	nA
Input Resistance	+25°C	50	100		40	100		40	100		MΩ
Common Mode Range	Full	±10.0			±10.0			±10.0			V
TRANSFER CHARACTERISTICS											
* Large Signal Voltage Gain (Note 1,4)	+25°C	10K	15K		7.5K	15K		7.5K	15K		V/V
	Full	7.5K			5K			5K			V/V
* Common Mode Rejection Ratio (Note 2)	Full	80	90		74	90		74	90		dB
Gain Bandwidth Product (Note 3)	+25°C		20			20			20		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
* Output Current (Note 4)	+25°C	±10	±20		±10	±20		±10	±20		mA
Full Power Bandwidth (Note 4)	+25°C	1500	2000		1200	1600		1200	1600		kHz
TRANSIENT RESPONSE (A_V = +3)											
Rise Time (Notes 1, 5, 6 & 8)	+25°C		25	50		25	50		25	50	ns
Overshoot (Notes 1, 5, 6 & 8)	+25°C		25	40		25	50		25	50	%
* Slew Rate (Notes 1, 4, 5 & 8)	+25°C	±100	±120		±80	±120		±80	±120		V/μs
Settling Time (Notes 1, 4, 5 & 8)	+25°C		0.20			0.20			0.20		μs
POWER SUPPLY CHARACTERISTICS											
* Supply Current	+25°C		4	6		4	6		4	6	mA
* Power Supply Rejection Ratio (Note 7)	Full	80	90		74	90		74	90		dB

NOTES: 1. R_L = 2K
 2. V_{CM} = ±5.0V
 3. A_V > 10

4. V_O = ±10.0V
 5. C_L = 50pF
 6. V_O = ±200mV

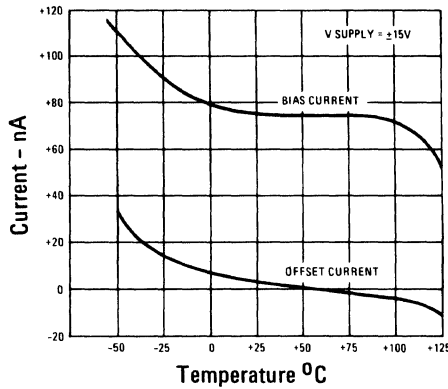
7. ΔV = ±5.0V
 8. See transient response test circuits and waveforms page four.

*100% Tested For DASH 8

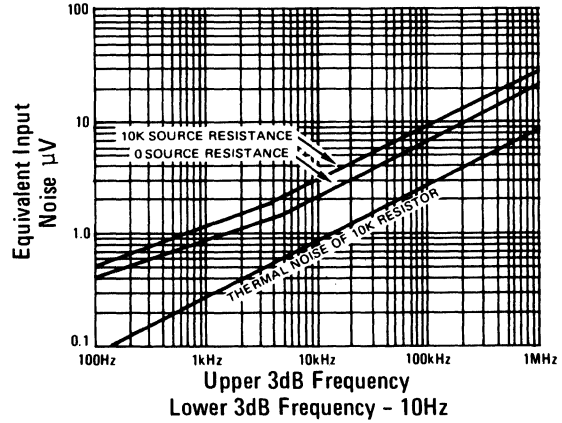
PERFORMANCE CURVES

$V_+ = 15\text{VDC}$, $V_- = 15\text{VDC}$, $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE STATED

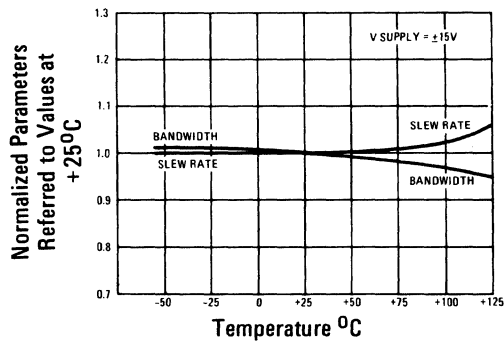
INPUT BIAS AND OFFSET CURRENT vs TEMPERATURE



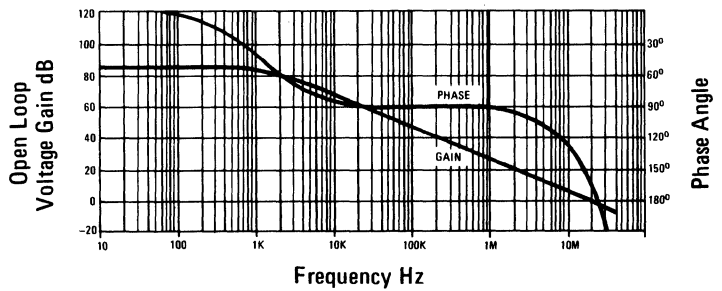
EQUIVALENT INPUT NOISE vs BANDWIDTH



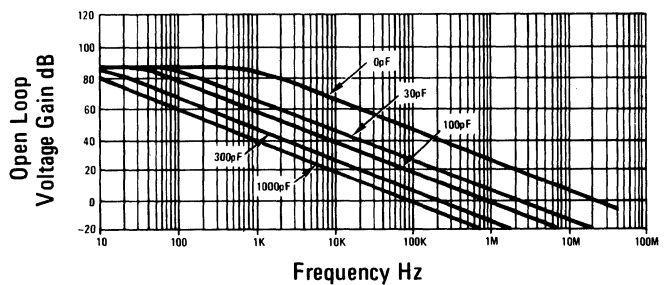
NORMALIZED AC PARAMETERS vs TEMPERATURE



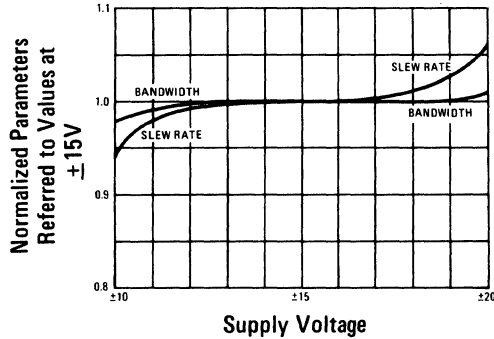
OPEN-LOOP FREQUENCY AND PHASE RESPONSE



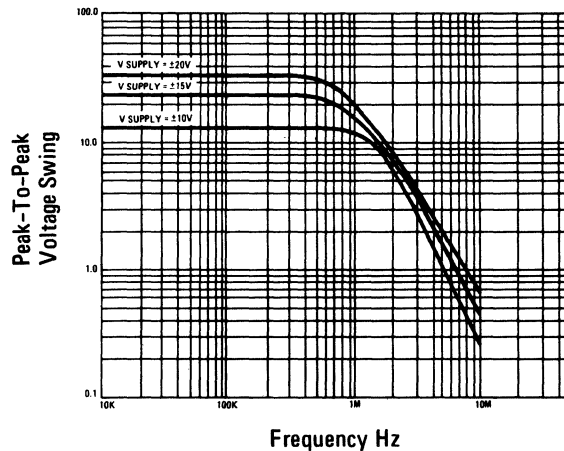
OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM BANDWIDTH CONTROL PIN TO GROUND



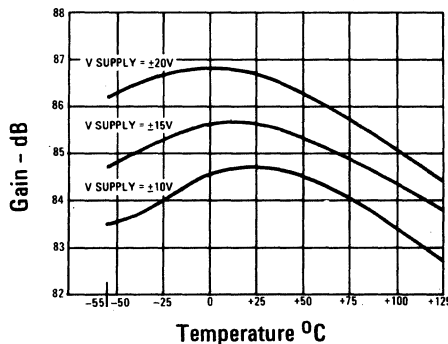
NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE AT +25 degrees Celsius



OUTPUT VOLTAGE SWING vs FREQUENCY AT +25 degrees Celsius

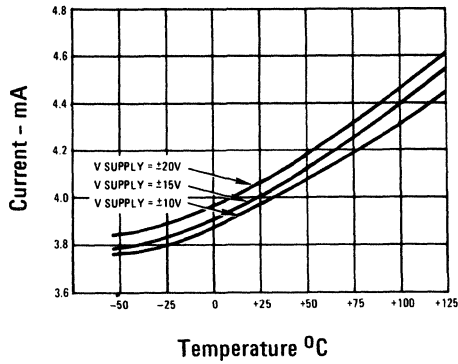


OPEN LOOP VOLTAGE GAIN vs TEMPERATURE

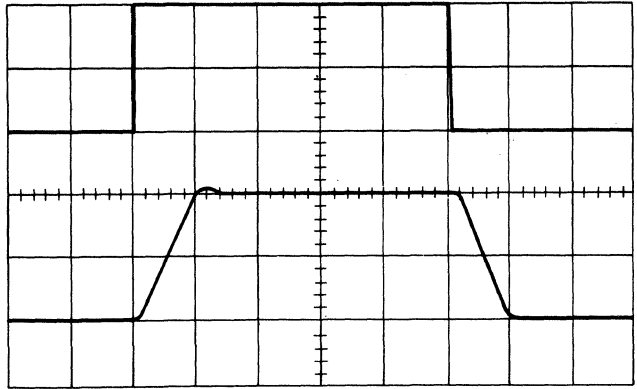


PERFORMANCE CURVES (continued)

POWER SUPPLY CURRENT vs TEMPERATURE



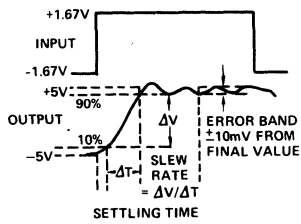
VOLTAGE FOLLOWER PULSE RESPONSE



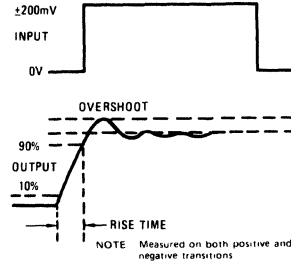
$R_L = 2K\Omega$, $C_L = 50pF$
 Upper Trace: Input; 1.33V/Div.
 Lower Trace: Output; 5V/Div.

Horizontal = 100ns/Div.
 $T_A = +25^\circ C$, $V_S = \pm 15V$

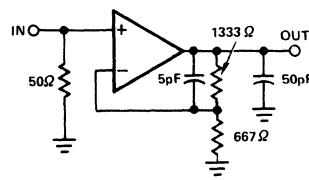
SLEW RATE AND SETTLING TIME



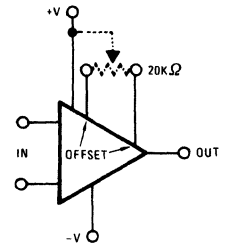
TRANSIENT RESPONSE



SLEW RATE AND TRANSIENT RESPONSE

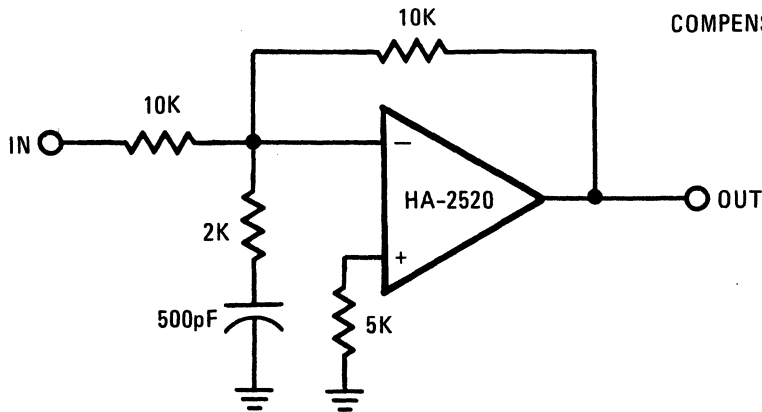


SUGGESTED OFFSET ZERO ADJUST HOOK-UP

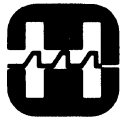


TYPICAL APPLICATIONS

COMPENSATION CIRCUIT FOR INVERTING UNITY GAIN



Slew Rate $\approx 120V/\mu s$
 Bandwidth $\approx 10MHz$
 Settling Time $\approx 500ns$



HARRIS
SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-2530/2535

High Slew Rate, Wideband Inverting Amplifier

FEATURES

- HIGH SLEW RATE $\pm 320V/\mu s$
- FAST SETTLING TIME 550ns
- WIDE POWER BANDWIDTH 5MHz
- HIGH GAIN BANDWIDTH PRODUCT 70MHz
- LOW OFFSET VOLTAGE 0.8mV
- LOW POWER SUPPLY CURRENT 3.5mA

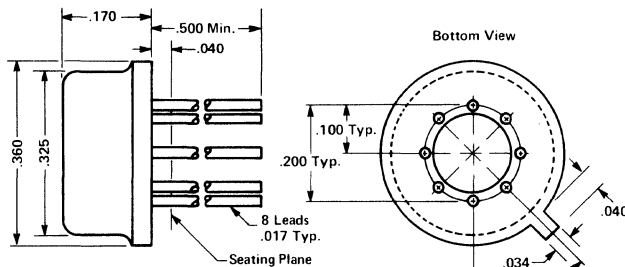
DESCRIPTION

The HA-2530/2535 is a monolithic wideband inverting amplifier whose performance characteristics are superior to any other monolithic in its class. The device uses a feedforward amplifier technique to achieve widepower bandwidth and high slew rate at no expense to noise or DC parameters. It is excellent for use in pulse circuits requiring high slew rate and fast settling, such as high speed integrators, A/D, D/A and sampled data systems. Also recommended for many video applications where wideband response at high output current levels are required. For gains less than 10 a small capacitor is required for stability.

PACKAGES

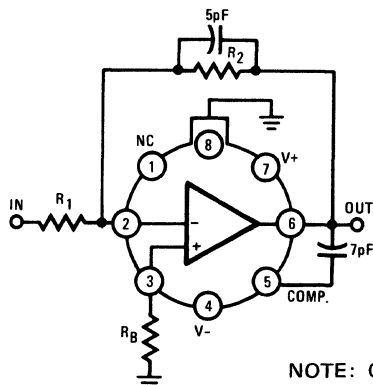
CODE 2A

T0-99



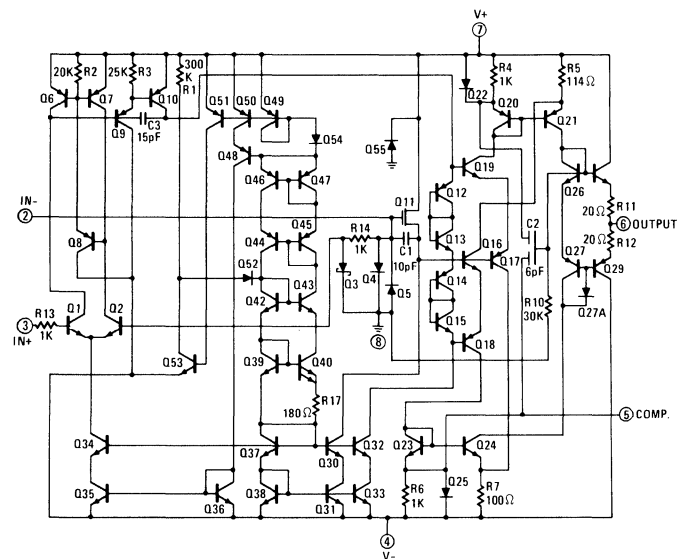
- NOTES: 1. All leads gold plated KOVAR
2. All dimensions in inches

PIN-OUT AND TYPICAL HOOK-UP



NOTE: Case tied to V-

SCHEMATIC



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V-Terminals	40V	Internal Power Dissipation (Note 1)	550mW
Peak Output Current	±100mA	Operating Temperature Range	-55°C ≤ T _A ≤ +125°C (HA-2530)
		Storage Temperature Range	0°C ≤ T _A ≤ +75°C (HA-2535)
			-65°C ≤ T _A ≤ +150°C

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{Supply} = ±15.0V Unless Otherwise Specified.

PARAMETER	TEMP.	HA-2530 -55°C to +125°C			HA-2535 0°C to +75°C			UNITS
		LIMITS			LIMITS			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
INPUT CHARACTERISTICS								
* Offset Voltage	+25°C		0.8			0.8		mV
	Full			3			5	mV
Average Offset Voltage Drift	Full		5			5		μV/°C
* Bias Current	+25°C		15			15		nA
	Full			100			200	nA
* Offset Current	+25°C		5			5		nA
	Full			20			20	nA
Input Resistance	+25°C		2			2		MΩ
Input Capacitance	+25°C		10			10		pF
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Notes 2,5)	+25°C		2X10 ⁶			2X10 ⁶		V/V
*	Full	10 ⁵			10 ⁵			V/V
* Common-Mode Rejection Ratio (Note 3)	Full	86	100		80	100		dB
Gain Bandwidth Product (Note 4)	+25°C		70			70		MHz
OUTPUT CHARACTERISTICS								
* Output Voltage Swing (Note 2)	Full	±10	±12		±10	±12		V
* Output Current (Note 5)	+25°C	±25	±50		±25	±50		mA
Full Power Bandwidth (Note 5)	+25°C	4	5		4	5		MHz
TRANSIENT RESPONSE (NOTES 6&7)								
* Rise Time	+25°C		20	40		20	40	ns
* Overshoot	+25°C		30	45		30	50	%
* Slew Rate	+25°C	±280	±320		±250	±320		V/μs
Settling Time	+25°C		500			500		ns
POWER SUPPLY CHARACTERISTICS								
* Supply Current	+25°C		3.5	6		3.5	6	mA
* Power Supply Rejection Ratio (Note 8)	Full	86	100		80	100		dB

NOTES: 1. Derate at 5.5mW/°C for Operation
Ambient Temperature Above 105°C
2. R_L = 2K
3. V_{CM} = ±5.0V
4. A_V > 10

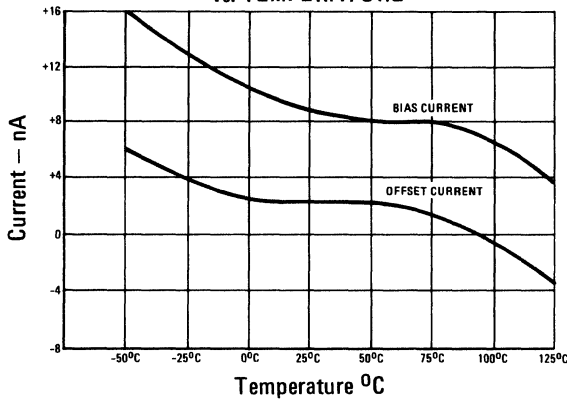
5. V_O = ±10V
6. C_L = 50pF
7. See Transient Response Test Circuit
and Wave Forms, Page 4.
8. ΔV = ±5.0V

* 100% Tested For DASH 8

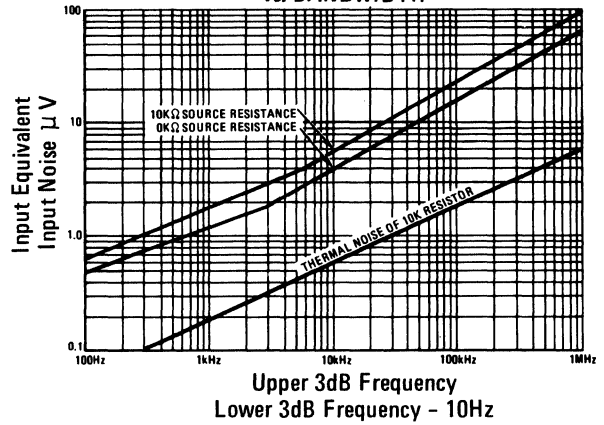
PERFORMANCE CURVES

$V_+ = 15\text{VDC}$, $V_- = 15\text{VDC}$, $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE STATED

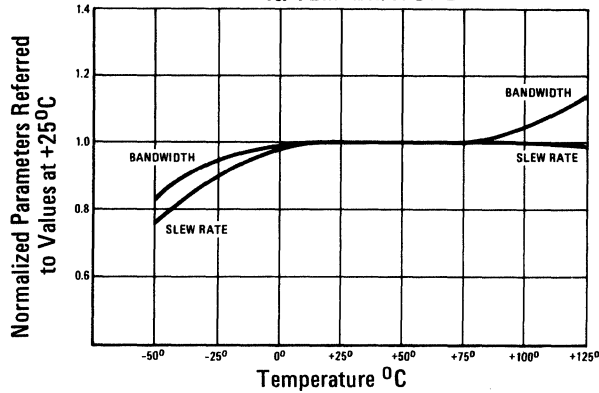
INPUT BIAS AND OFFSET CURRENT vs. TEMPERATURE



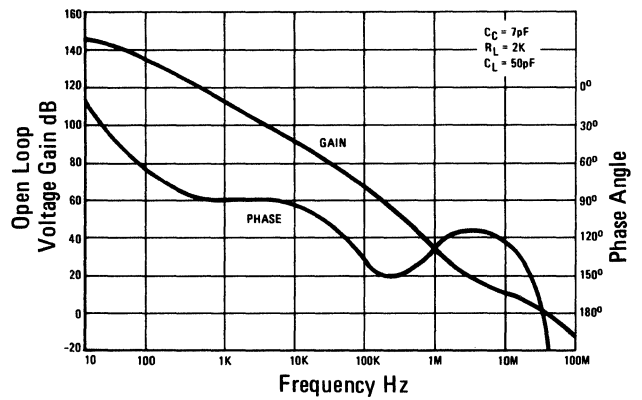
EQUIVALENT INPUT NOISE vs. BANDWIDTH



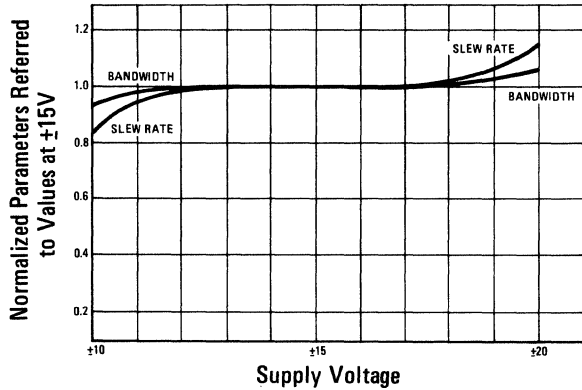
NORMALIZED AC PARAMETERS vs. TEMPERATURE



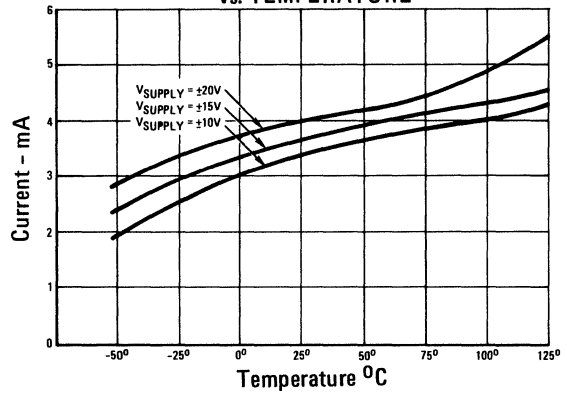
OPEN-LOOP FREQUENCY AND PHASE RESPONSE



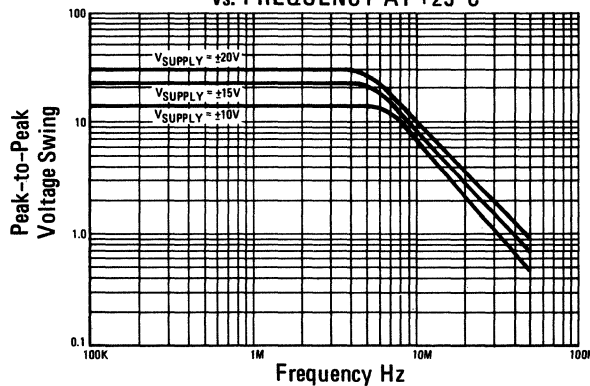
NORMALIZED AC PARAMETERS vs. SUPPLY VOLTAGE AT +25°C



POWER SUPPLY CURRENT vs. TEMPERATURE

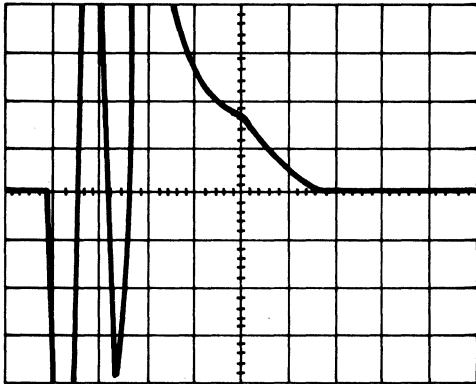


OUTPUT VOLTAGE SWING vs. FREQUENCY AT +25°C



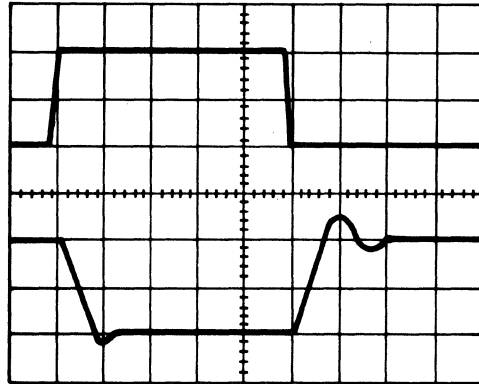
PERFORMANCE CURVES (continued)

SETTLING TIME MEASUREMENT *1



VERTICAL = 5mV/DIV.
 HORIZONTAL = 100ns/DIV.
 $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$

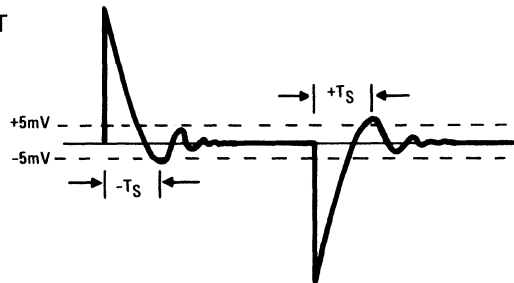
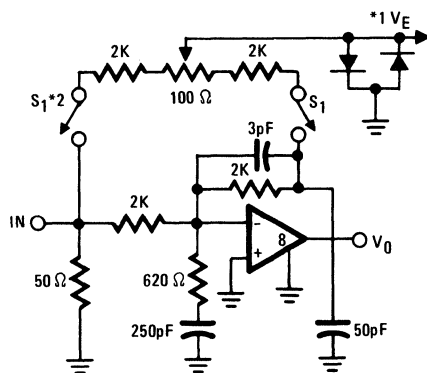
UNITY GAIN PULSE RESPONSE



UPPER TRACE: INPUT VERTICAL = 5V/DIV.
 LOWER TRACE: OUTPUT HORIZONTAL = 50ns/DIV.
 $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$

LINEAR

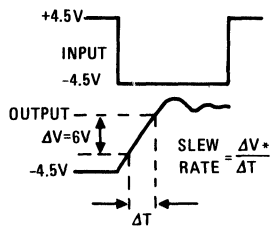
SLEW RATE/SETTLING TIME/TRANSIENT RESPONSE TEST CIRCUIT



*1 Settling time (T_S) is measured using a high speed high recovery oscilloscope to display the error voltage V_E . When V_E is within $\pm 5\text{mV}$ of final value the output V_O will be within $\pm 10\text{mV}$ (0.1%).

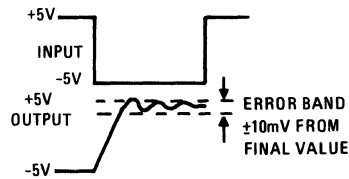
*2 S_1 closed for settling time.

SLEW RATE

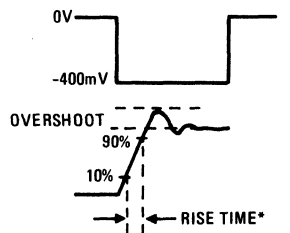


* MEASURED ON BOTH POSITIVE AND NEGATIVE EXCURSIONS.

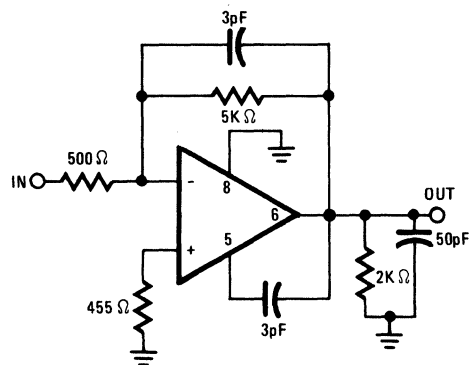
SETTLING TIME

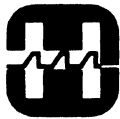


TRANSIENT RESPONSE



5MHz VIDEO AMPLIFIER ($A_V = 10$)





HARRIS
SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-2600/2602/2605

High Impedance Operational Amplifier

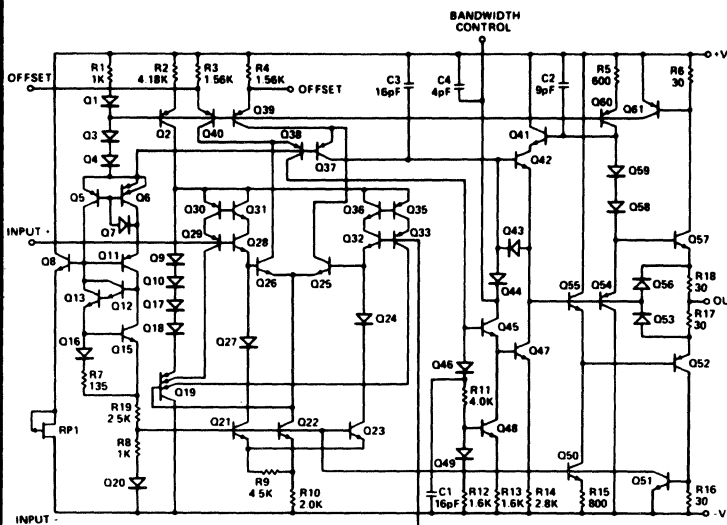
FEATURES

- HIGH INPUT IMPEDANCE
- LOW INPUT BIAS CURRENT
- LOW INPUT OFFSET CURRENT
- LOW INPUT OFFSET VOLTAGE
- HIGH GAIN
- HIGH SLEW RATE
- FAST RESPONSE TIME
- OUTPUT SHORT CIRCUIT PROTECTION
- MEETS OR EXCEEDS MIL-STD-883 REQUIREMENTS

GENERAL DESCRIPTION

Internally compensated high impedance, high performance monolithic operational amplifier intended for use as a general purpose operational amplifier in precision instrumentation and signal processing.

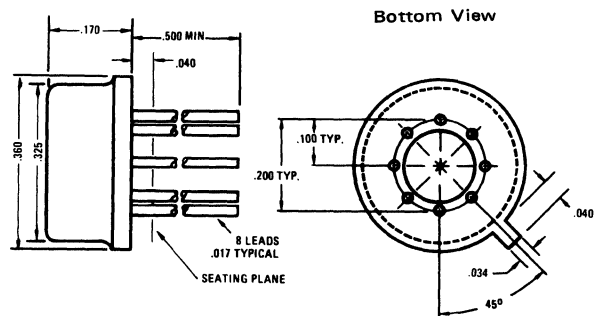
SCHEMATIC



PACKAGES

CODE 2A

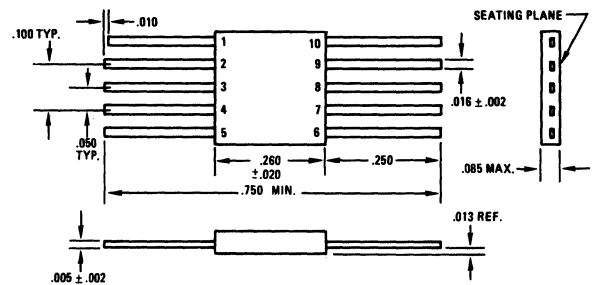
T0-99



NOTES: 1. All leads gold plated KOVAR
2. All dimensions in inches

CODE 9W

T0-91



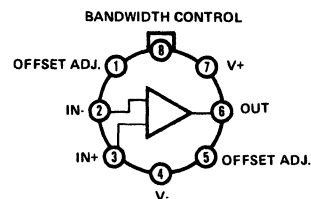
ALL DIMENSIONS ARE IN INCHES.
ALL DIMENSIONS ± .010 UNLESS OTHERWISE SHOWN.

PIN OUT

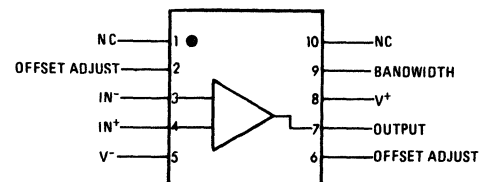
T0-99

Top View

Case Connected to V-



T0-91



Case Connected to V-

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V ⁺ and V ⁻ Terminals	45.0V
Differential Input Voltage	±12.0V
Peak Output Current	Full Short Circuit Protection
Internal Power Dissipation	300mW
Operating Temperature Range – HA-2600/HA-2602	-55°C ≤ T _A ≤ +125°C
HA-2605	0° ≤ T _A ≤ +75°C
Storage Temperature Range	-65°C ≤ T _A ≤ +150°C

ELECTRICAL CHARACTERISTICS

V₊ = +15VDC, V₋ = -15VDC

PARAMETER	TEMP.	HA-2600 -55°C to +125°C			HA-2602 -55°C to +125°C			HA-2605 0°C to +75°C			UNITS
		LIMITS			LIMITS			LIMITS			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
INPUT CHARACTERISTICS											
* Offset Voltage	+25°C		0.5	4		3	5		3	5	mV
	Full		2	6			7			7	mV
Offset Voltage Average Drift	Full		5								μV/°C
* Bias Current	+25°C		1	10		15	25		5	25	nA
	Full		10	30			60			40	nA
* Offset Current	+25°C		1	10		5	25		5	25	nA
	Full		5	30			60			40	nA
Input Resistance	+25°C	100	500		40	300		40	300		MΩ
Common Mode Range	Full	±11.0			±11.0			±11.0			V
TRANSFER CHARACTERISTICS											
* Large Signal Voltage Gain (Notes 1, 4)	+25°C	100K	150K		80K	150K		80K	150K		V/V
	Full	70K			60K			70K			V/V
* Common Mode Rejection Ratio (Note 2)	Full	80	100		74	100		74	100		dB
Unity Gain Bandwidth (Note 3)	+25°C		12			12			12		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
* Output Current (Note 4)	+25°C	±15	±22		±10	±18		±10	±18		mA
Full Power Bandwidth (Note 4)	+25°C	50	75		50	75		50	75		kHz
TRANSIENT RESPONSE											
Rise Time (Notes 1, 5, 6 & 8)	+25°C		30	60		30	60		30	60	ns
Overshoot (Notes 1, 5, 7 & 8)	+25°C		25	40		25	40		25	40	%
* Slew Rate (Notes 1, 4, 5 & 8)	+25°C	±4	±7		±4	±7		±4	±7		V/μs
Settling Time (Notes 1, 4, 5 & 8)	+25°C		1.5			1.5			1.5		μs
POWER SUPPLY CHARACTERISTICS											
* Supply Current	+25°C		3.0	3.7		3.0	4.0		3.0	4.0	mA
* Power Supply Rejection Ratio (Note 9)	Full	80	90		74	90		74	90		dB

TEST CONDITIONS

- NOTES: 1. R_L = 2K
 2. V_{CM} = ±5.0V
 3. V_O < 90mV
 4. V_O = ±10V
 5. C_L = 100pF
 6. V_O = ±200mV

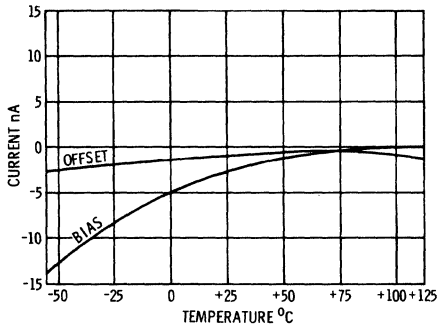
7. V_O = ±400mV
 8. See Transient response test circuits and waveforms page three.
 9. V_S = ±9.0V to ±15V

*100% Tested For DASH 8

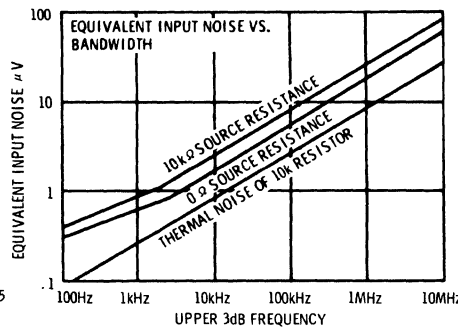
LINEAR

PERFORMANCE CURVES

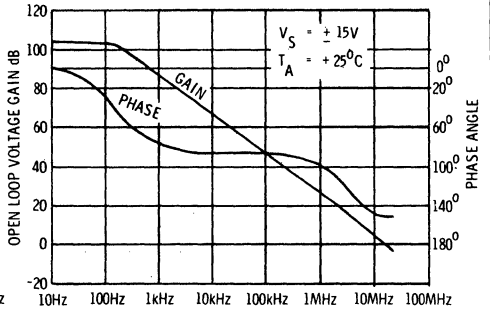
$V_+ = 15\text{VDC}$, $V_- = 15\text{VDC}$, $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE STATED.



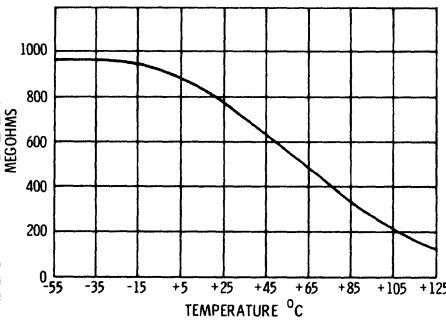
INPUT BIAS CURRENT AND OFFSET CURRENT AS A FUNCTION OF TEMPERATURE



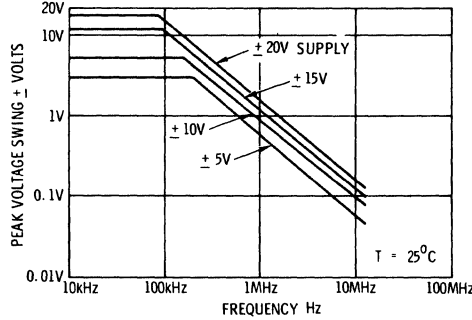
BROADBAND NOISE CHARACTERISTICS



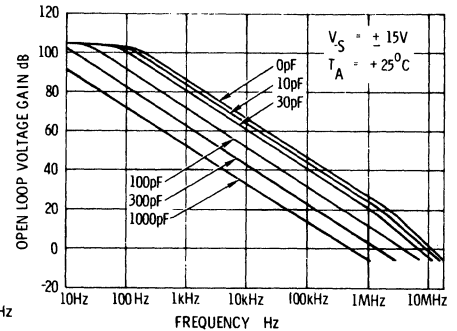
OPEN LOOP FREQUENCY AND PHASE RESPONSE



INPUT IMPEDANCE VS. TEMPERATURE, 100Hz

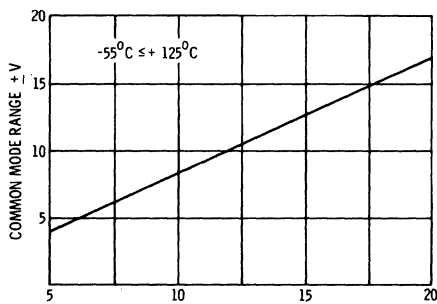


OUTPUT VOLTAGE SWING VS. FREQUENCY

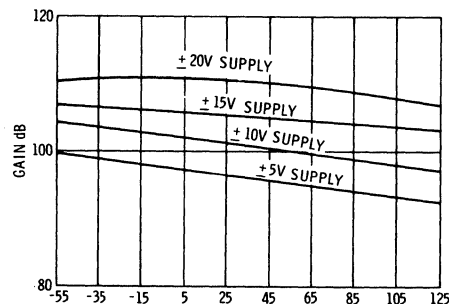


OPEN-LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM BANDWIDTH CONTROL PIN TO GROUND

Note: External Compensation Components are not Required for Stability, But May be Added to Reduce Bandwidth if Desired. If External Compensation is Used, Also Connect 100pF Capacitor From Output to Ground.

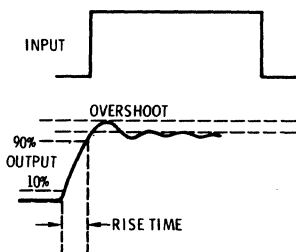


COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



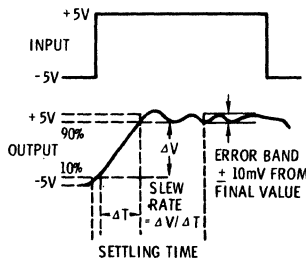
OPEN-LOOP VOLTAGE GAIN VS. TEMPERATURE

TRANSIENT RESPONSE

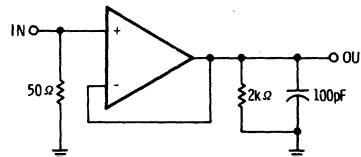


NOTE: MEASURED ON BOTH POSITIVE AND NEGATIVE TRANSITIONS.

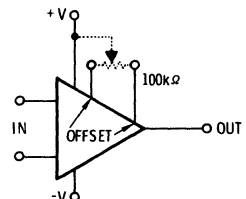
SLEW RATE AND SETTLING TIME



SLEW RATE AND TRANSIENT RESPONSE

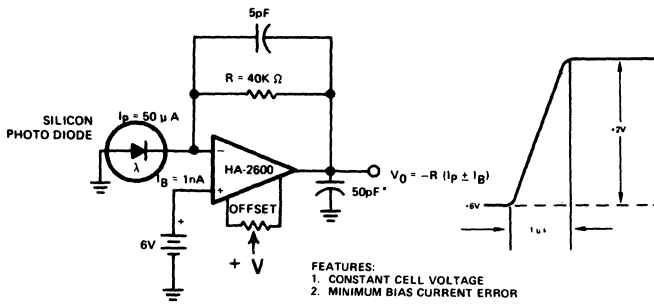


SUGGESTED OFFSET ZERO ADJUST HOOK-UP

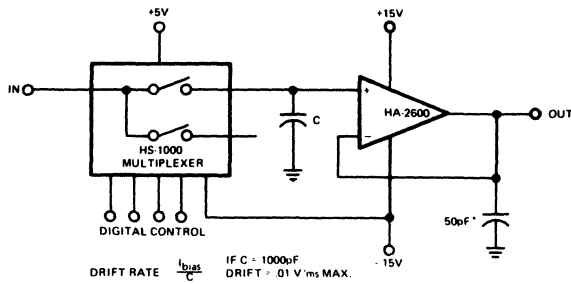


LINEAR

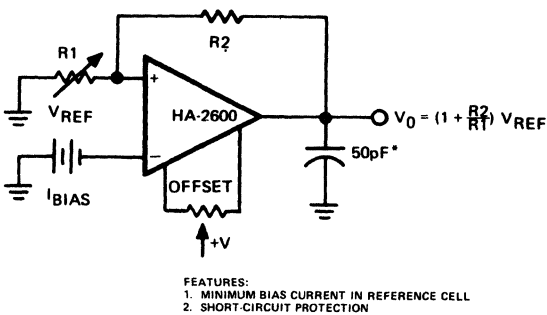
PHOTO-CURRENT TO VOLTAGE CONVERTER



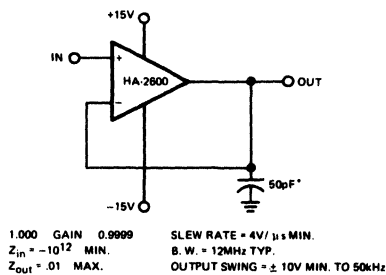
SAMPLE - AND - HOLD



REFERENCE VOLTAGE AMPLIFIER



VOLTAGE FOLLOWER



*A small load capacitance is recommended in all applications where practical to prevent possible high frequency oscillations resulting from external wiring parasitics. Capacitance up to 100pF has negligible effect on the bandwidth or slew rate.

INPUT OFFSET VOLTAGE - That voltage which must be applied between the input terminals through two equal resistances to force the output voltage to zero.

INPUT OFFSET CURRENT - The difference in the currents into the two input terminals when the output is at zero voltage.

INPUT BIAS CURRENT - The average of the currents flowing into the input terminals when the output is at zero voltage.

INPUT COMMON MODE VOLTAGE - The average referred to ground of the voltages at the two input terminals.

COMMON MODE RANGE - The range of voltages which is exceeded at either input terminal will cause the amplifier to cease operating.

COMMON MODE REJECTION RATIO - The ratio of a specified range of input common mode voltage to the peak-to-peak change in input offset voltage over this range.

OUTPUT VOLTAGE SWING - The peak symmetrical output voltage swing, referred to ground, that can be obtained without clipping.

INPUT RESISTANCE - The ratio of the change in input voltage to the change in input current.

OUTPUT RESISTANCE - The ratio of the change in output voltage to the change in output current.

VOLTAGE GAIN - The ratio of the change in output voltage to the change in input voltage producing it.

BANDWIDTH - The frequency at which the voltage gain is 3 dB below its low frequency value.

UNITY GAIN BANDWIDTH - The frequency at which the voltage gain of the amplifier is unity.

POWER SUPPLY REJECTION RATIO - The ratio of the change in input offset voltage to the change in power supply voltage producing it.

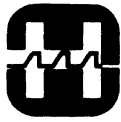
TRANSIENT RESPONSE - The closed loop step function response of the amplifier under small signal conditions.

PHASE MARGIN - [180° - (Φ₁ + Φ₂)] where Φ₁ is the phase shift at the frequency where the absolute magnitude of gain is unity Φ₂ is the phase shift at a frequency much lower than the open-loop bandwidth.

SLEW RATE (Rate Limiting) - The rate at which the output will move between full scale stops, measured in terms of volts per unit time. This limit to an ideal step function response is due to the non-linear behavior in an amplifier due to its limited ability to produce large, rapid changes in output voltage (slewing) . . . restricting it to rates of change of voltage lower than might be predicted by observing the small signal frequency response.

SETTLING TIME - Time required for output waveform to remain within 0.1 percent of final value.

LINEAR



HARRIS
SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-2620/2622/2625

*Wide Band, High Impedance
Operational Amplifiers*

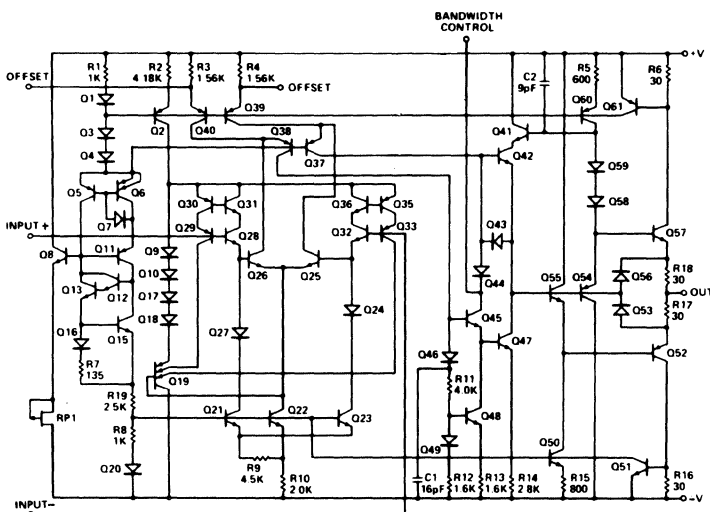
FEATURES

- GAIN BANDWIDTH PRODUCT 100MHz
- HIGH INPUT IMPEDANCE 500MΩ
- LOW INPUT BIAS CURRENT 1nA
- LOW INPUT OFFSET CURRENT 1nA
- LOW INPUT OFFSET VOLTAGE 1mV
- HIGH GAIN 150K
- HIGH SLEW RATE 35V/μs
- OUTPUT SHORT CIRCUIT PROTECTION

GENERAL DESCRIPTION

The HA-2620 family of operational amplifiers has very low input bias current and intended for use as high impedance comparators and wide band amplifiers. The HA-2620 family features very high gain, very high slew rate and output short circuit protection. The HA-2620 and HA-2622 operate over the full military temperature range from -55°C to +125°C. The HA-2625 operates over the temperature range of 0°C to +75°C.

SCHEMATIC

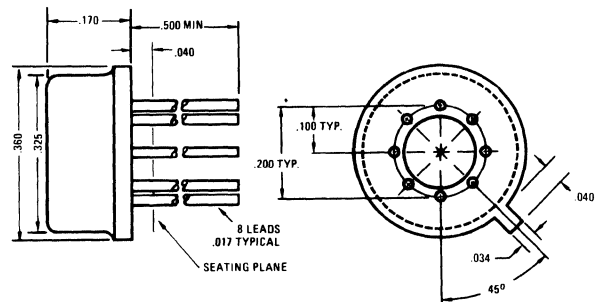


PACKAGES

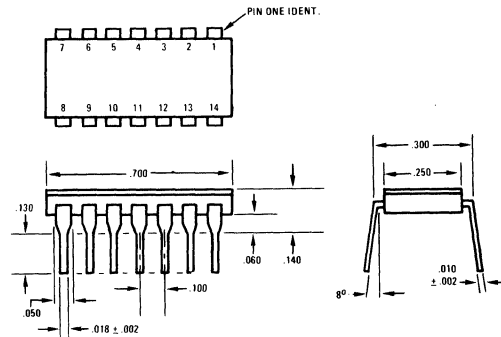
CODE 2A

Bottom View

T0-99



CODE 1S

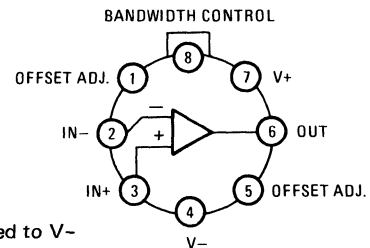


ALL DIMENSIONS ARE IN INCHES.
ALL DIMENSIONS ± .010 UNLESS
OTHERWISE SHOWN.

PIN OUT

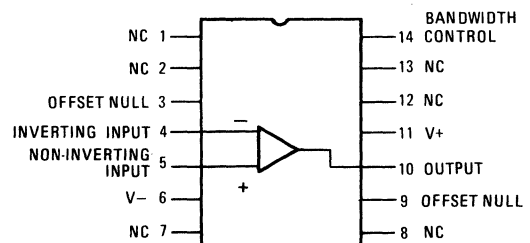
Top View

T0-99



Case Connected to V-

T0-116



Case Connected to V-

LINEAR

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V ⁺ and V ⁻ Terminals	45.0V
Differential Input Voltage	±12.0V
Peak Output Current	Full Short Circuit Protection
Internal Power Dissipation	300mW
Storage Temperature Range	-65°C ≤ T _A ≤ +150°C

ELECTRICAL CHARACTERISTICS

V⁺ = +15 VDC, V⁻ = -15 VDC

PARAMETER	TEMPERATURE	HA-2620 -55°C to +125°C			HA-2622 -55°C to +125°C			HA-2625 0°C to +75°C			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
INPUT CHARACTERISTICS											
* Offset Voltage (Note 1)	+25°C Full		0.5 4 6			3 5 7			3 5 7		mV mV
* Bias Current	+25°C Full		1 10 35			5 25 60			5 25 40		nA nA
* Offset Current	+25°C Full		1 5 35			5 25 60			5 25 40		nA nA
Input Resistance	+25°C	65	500		40	300		40	300		MΩ
Common Mode Range	Full	±11.0			±11.0			±11.0			V
TRANSFER CHARACTERISTICS											
* Large Signal Voltage Gain (Notes 2 & 3)	+25°C Full	100K 70K	150K		80K 60K	150K		80K 70K	150K		V/V V/V
* Common Mode Rejection Ratio (Note 4)	Full	80	100		74	100		74	100		dB
Gain Bandwidth Product (Notes 2, 5, & 6)	+25°C		100			100			100		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 2)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
* Output Current (Note 3)	+25°C	±15	±22		±10	±18		±10	±18		mA
Full Power Bandwidth (Notes 2, 3 & 7)	+25°C	400	600		320	600		320	600		kHz
TRANSIENT RESPONSE											
Rise Time (Notes 2, 5, 7 & 8)	+25°C		17 45			17 45			17 45		ns
* Slew Rate (Notes 2, 7, 8 & 10)	+25°C	±25	±35		±20	±35		±20	±35		V/μs
POWER SUPPLY CHARACTERISTICS											
* Supply Current	+25°C		3.0 3.7			3.0 4.0			3.0 4.0		mA
* Power Supply Rejection Ratio (Note 9)	Full	80	90		74	90		74	90		dB

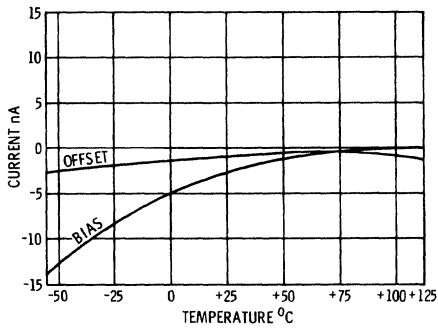
- NOTES: 1. Offset may be externally adjusted to zero.
 2. R_L = 2KΩ, C_L = 50pF
 3. V_O = ±10.0V
 4. V_{CM} = ±5.0V
 5. V_O < 90mV
 6. 40dB Gain

7. See transient response test circuits and waveforms page 3.
 8. A_V = 5.0V (The HA-2620 family is not stable at unity gain without external compensation.)
 9. V_{Sup} = ±9.0V to ±15.0V
 10. V_O = 5.0V

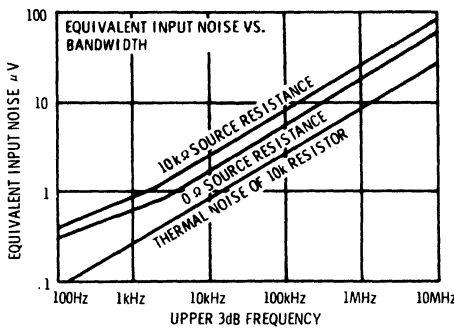
*100% Tested For DASH 8

TYPICAL PERFORMANCE CURVES

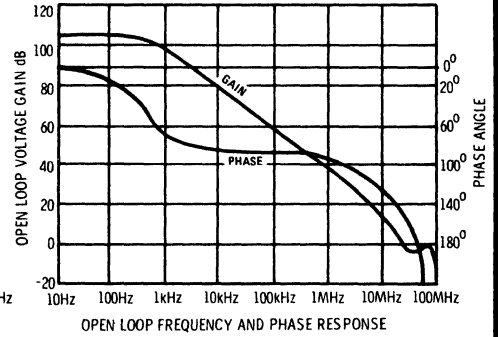
$V_+ = 15\text{VDC}$, $V_- = 15\text{VDC}$, $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE STATED.



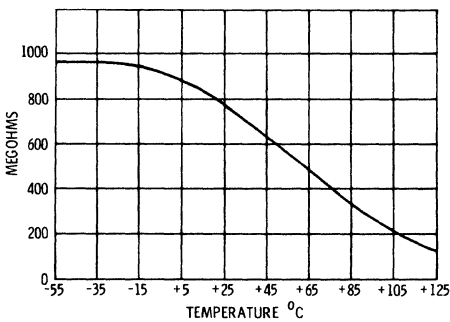
INPUT BIAS CURRENT AND OFFSET CURRENT - AS A FUNCTION OF TEMPERATURE



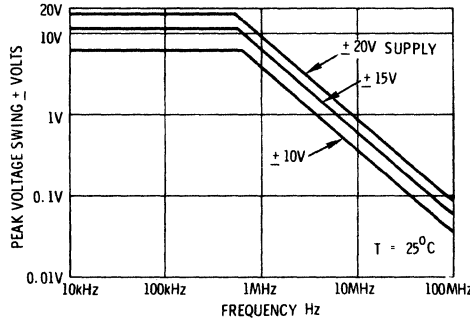
BROADBAND NOISE CHARACTERISTICS
UPPER 3dB FREQUENCY
LOWER 3dB FREQUENCY - 10Hz



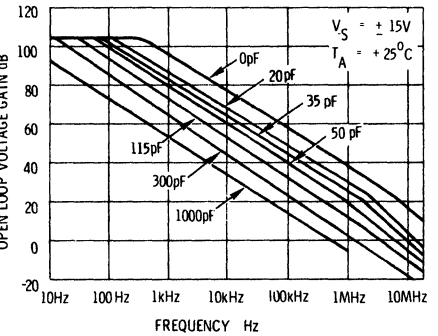
OPEN LOOP FREQUENCY AND PHASE RESPONSE



INPUT IMPEDANCE VS. TEMPERATURE, 100Hz

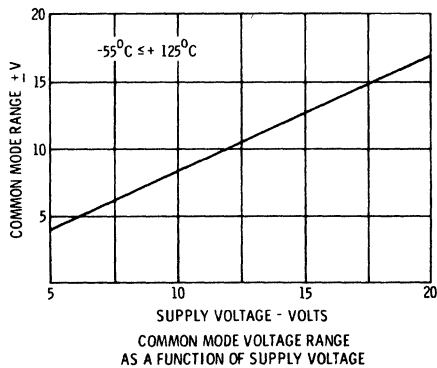


OUTPUT VOLTAGE SWING VS. FREQUENCY
 $T = 25^\circ\text{C}$

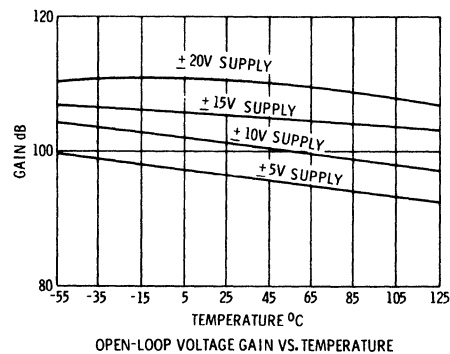


OPEN-LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM BANDWIDTH CONTROL PIN TO GROUND

Note: External Compensation is Required For Closed Loop Gain < 5 . If External Compensation is Used, Also Connect 100 pF Capacitor From Output to Ground.

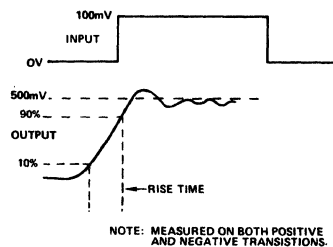


COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE

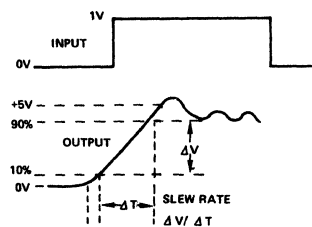


OPEN-LOOP VOLTAGE GAIN VS. TEMPERATURE

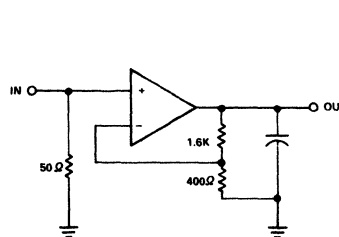
TRANSIENT RESPONSE



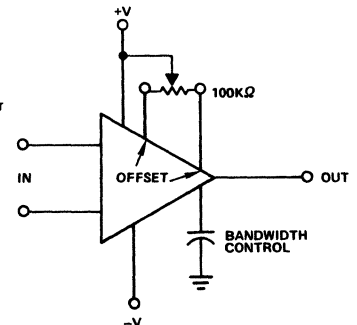
SLEW RATE



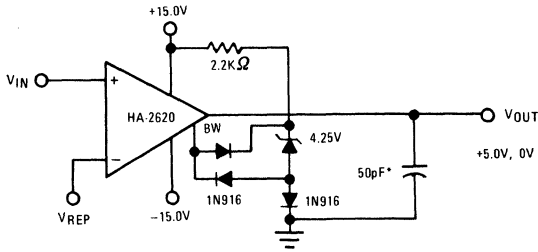
SLEW RATE AND TRANSIENT RESPONSE



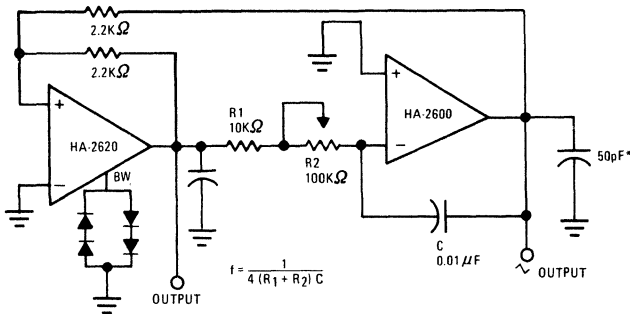
SUGGESTED OFFSET ZERO ADJUST AND BANDWIDTH CONTROL HOOK-UP



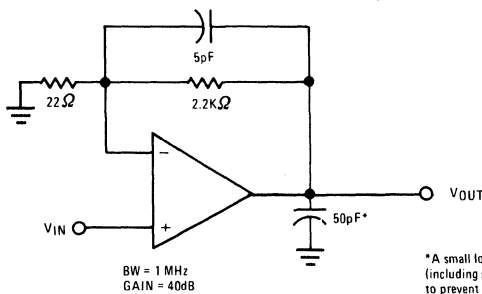
HIGH IMPEDANCE COMPARATOR



FUNCTION GENERATOR



VIDEO AMPLIFIER



BW = 1 MHz
GAIN = 40dB

*A small load capacitance of at least 30pF (including stray capacitance) is recommended to prevent possible high frequency oscillations.

INPUT OFFSET VOLTAGE—That voltage which must be applied between the input terminals through two equal resistances to force the output voltage to zero.

INPUT OFFSET CURRENT—The difference in the currents into the two input terminals when the output is at zero voltage.

INPUT BIAS CURRENT—The average of the currents flowing into the input terminals when the output is at zero voltage.

INPUT COMMON MODE VOLTAGE—The average referred to ground of the voltages at the two input terminals.

COMMON MODE RANGE—The range of voltages which is exceeded at either input terminal will cause the amplifier to cease operating.

COMMON MODE REJECTION RATIO—The ratio of a specified range of input common mode voltage to the peak-to-peak change in input offset voltage over this range.

OUTPUT VOLTAGE SWING—The peak symmetrical output voltage swing, referred to ground, that can be obtained without clipping.

INPUT RESISTANCE—The ratio of the change in input voltage to the change in input current.

OUTPUT RESISTANCE—The ratio of the change in output voltage to the change in output current.

VOLTAGE GAIN—The ratio of the change in output voltage to the change in input voltage producing it.

UNITY GAIN BANDWIDTH—The frequency at which the voltage gain of the amplifier is unity.

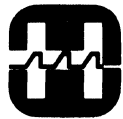
POWER SUPPLY REJECTION RATIO—The ratio of the change in input offset voltage to the change in power supply voltage producing it.

TRANSIENT RESPONSE—The closed loop step function response of the amplifier under small signal conditions.

GAIN BANDWIDTH PRODUCT—The product of the gain and the bandwidth at a given gain.

SLEW RATE (Rate Limiting)—The rate at which the output will move between full scale stops, measured in terms of volts per unit time. This limit to an ideal step function response is due to the non-linear behavior in an amplifier due to its limited ability to produce large, rapid changes in output voltage (slewing)...restricting it to rates of change of voltage lower than might be predicted by observing the small signal frequency response.

LINEAR



HARRIS
SEMICONDUCTOR
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HA-2630/2635

High Performance Current Booster

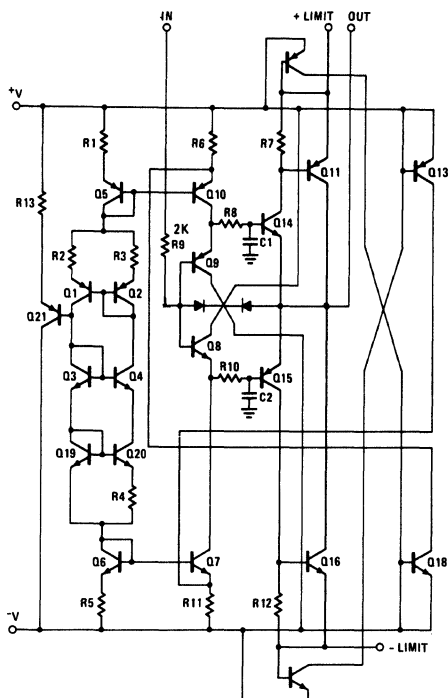
FEATURES

- OUTPUT CURRENT $\pm 600\text{mA}$
- SLEW RATE $500\text{V}/\mu\text{s}$
- BANDWIDTH 8MHz
- FULL POWER BANDWIDTH 8MHz
- INPUT RESISTANCE $2.0 \times 10^6 \Omega$
- OUTPUT RESISTANCE 2.0Ω
- POWER SUPPLY RANGE $\pm 5 \text{ TO } \pm 20\text{V}$
- PACKAGE IS ELECTRICALLY ISOLATED

DESCRIPTION

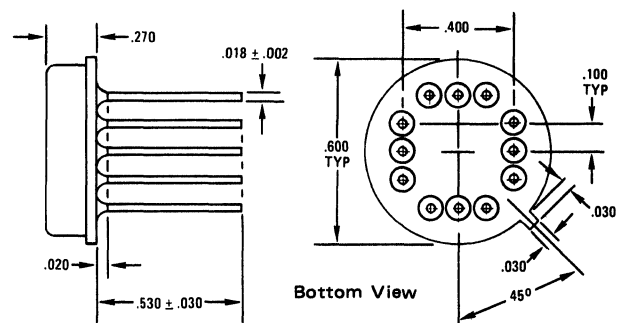
The HA-2630/2635 is a unity voltage gain, current amplifier intended to be used in series with an operational amplifier, inside the feedback loop, wherever additional output current capability is required. Wide bandwidth and exceptionally high slew rate allow it to be used with high performance op amps without producing instability or signal distortion. Current delivered to the load may be limited to a predetermined level by choice of two optional external limiting resistors. This device is packaged in an electrically isolated TO-8 type can allowing it to be conveniently mounted with or without a heat sink. The HA-2630 has guaranteed operation over -55°C to $+125^\circ\text{C}$, while the HA-2635 is guaranteed over 0°C to $+75^\circ\text{C}$.

SCHEMATIC DIAGRAM



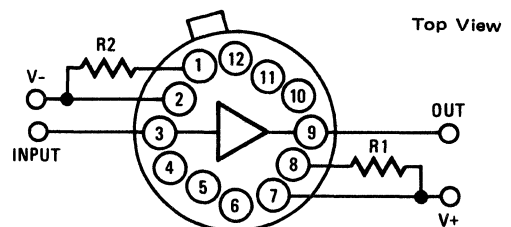
PACKAGE

CODE 2G T0-8



ALL DIMENSIONS ARE IN INCHES
ALL DIMENSIONS $\pm .010$ UNLESS OTHERWISE SHOWN.

PIN OUT



LINEAR

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	40V
Input Voltage Range	± V Supply
Output Current (Note 2)	±700mA
Internal Power Dissipation (Note 6) Free Air:	1W
In Heat Sink:	4W

Operating Temperature Range:	-55°C ≤ T _A ≤ +125°C (HA-2630)
	0°C ≤ T _A ≤ +75°C (HA-2635)
Storage Temperature Range:	-65°C ≤ T _A ≤ +150°C

ELECTRICAL CHARACTERISTICS

V_{Supply} = ±15 Volts R_L = 50 Ohms R₁ = R₂ = 0 Ohms Unless otherwise specified.

PARAMETER	TEMP.	HA-2630 -55°C to +125°C			HA-2635 0°C to +75°C			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
INPUT CHARACTERISTICS								
* Bias Current	+25°C Full		30 200	150 200		30 200	150 200	μA μA
Input Resistance	+25°C		2.0			2.0		MΩ
Input Capacitance	+25°C		5.0			5.0		pF
TRANSFER CHARACTERISTICS								
Voltage Gain (Note 1)	Full	.85	.95		.85	.95		V/V
* Offset Voltage (V _{OUT} - V _{IN})	+25°C Full		70	±200 ±300		70	±200 ±300	mV mV
Bandwidth (-3dB)	+25°C		8.0			8.0		MHz
OUTPUT CHARACTERISTICS								
* Output Voltage Swing	Full	±10			±10			V
* Output Current (Note 1)	+25°C Full	±400 ±300	±600		±400 ±300	±600		mA mA
Output Resistance	+25°C		2.0			2.0		Ω
Full Power Bandwidth (Note 1)	+25°C		8.0			8.0		MHz
TRANSIENT RESPONSE								
Rise Time (Note 3)	+25°C		30			30		ns
Slew Rate (Note 4)	+25°C	200	500		200	500		V/μs
POWER SUPPLY CHARACTERISTICS								
* Supply Current	Full		15	20		15	23	mA
Supply Voltage Range	Full	±5		±20	±5		±20	V
Power Supply Rejection Ratio (Note 5)	Full		66			66		dB

- NOTES: 1. V_O = ±10V
 2. Heat sink is required for continuous short circuit protection, regardless of current limit setting.
 3. V_O = 0.4V p-p.
 4. V_O = 10V p-p.

5. ΔV_{SUPPLY} = ±5V.
 6. Without heat sink, derate by 14mW/°C ambient temperature above 100°C ambient, with heat sink, derate by 67mW/°C case temperature above 115°C case.

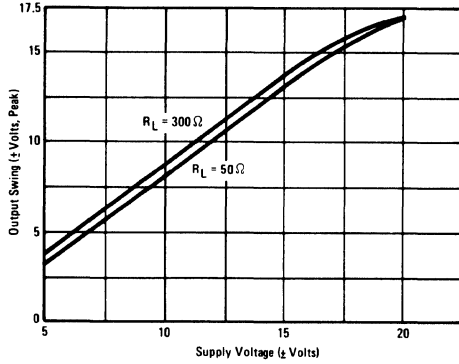
*100% Tested For DASH 8

LINEAR

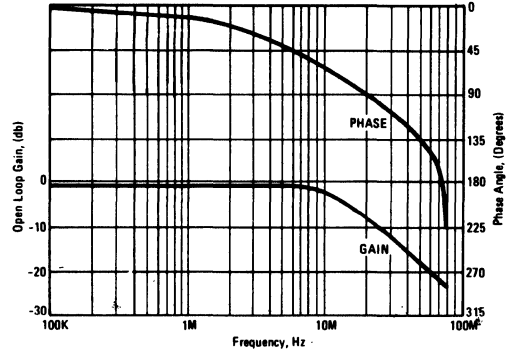
PERFORMANCE CURVES

$V_+ = 15\text{VDC}$, $V_- = 15\text{VDC}$, $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE STATED

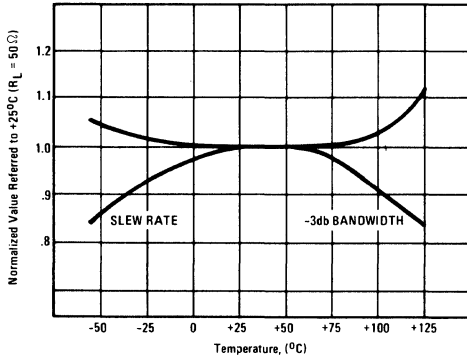
OUTPUT SWING
($R_{LIMIT} = 0\Omega$)



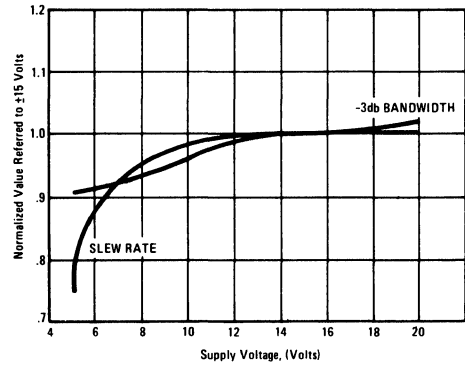
OPEN LOOP FREQUENCY AND PHASE RESPONSE ($R_L = 50\Omega$, $C_L \approx 10\text{pF}$)



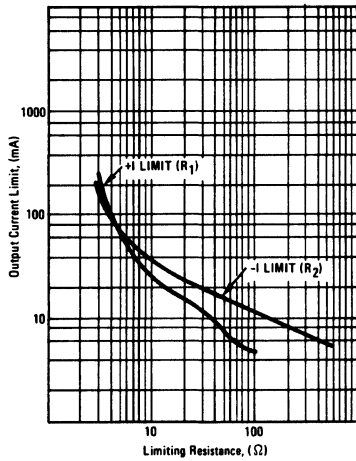
NORMALIZED AC PARAMETERS vs. TEMPERATURE ($R_L = 50\Omega$)



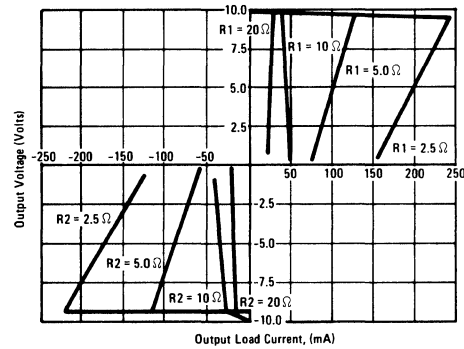
NORMALIZED AC PARAMETERS vs. SUPPLY VOLTAGE ($R_L = 50\Omega$)



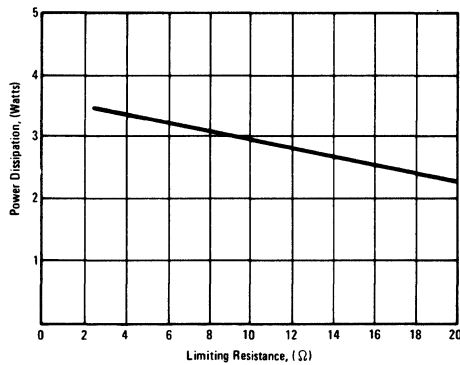
OUTPUT CURRENT LIMITING vs. LIMITING RESISTANCE



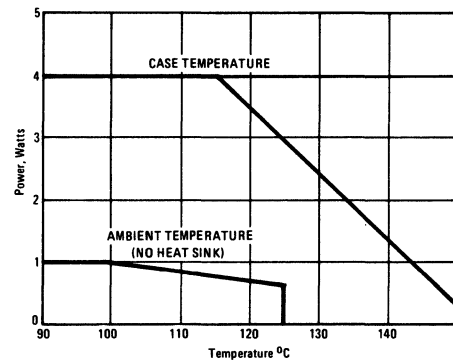
OUTPUT CURRENT CHARACTERISTIC



POWER DISSIPATION vs. LIMITING RESISTANCE WITH OUTPUT SHORTED TO GROUND; $V_{IN} = +10\text{V}$

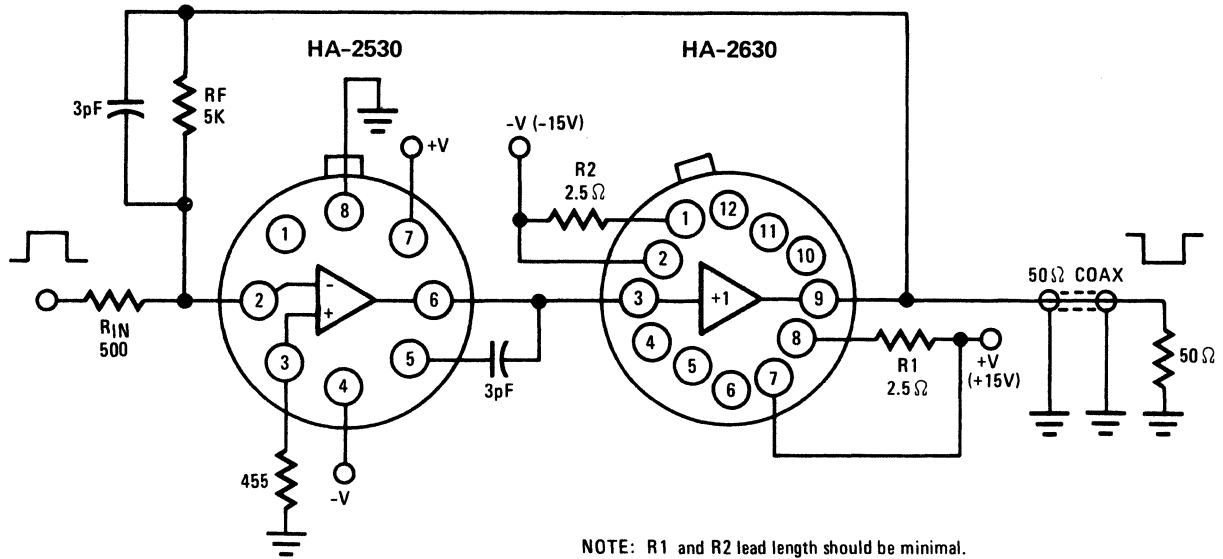


MAXIMUM ALLOWABLE INTERNAL POWER DISSIPATION vs. TEMPERATURE

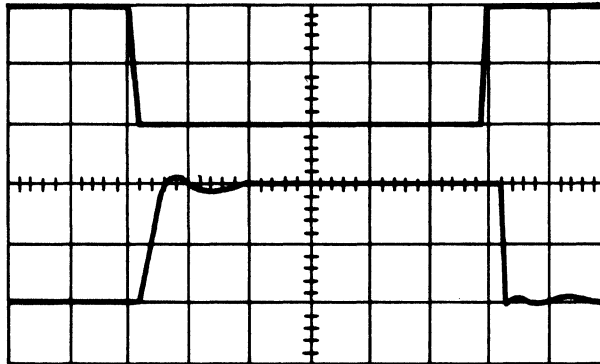


TYPICAL APPLICATION

20db, 5MHz VIDEO COAXIAL LINE DRIVER



LINE DRIVER PULSE RESPONSE



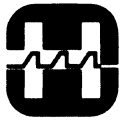
Horizontal Scale = 200ns/Div.

Upper Trace: Input, 200mV/Div.

Lower Trace: Output, 2V/Div.

SOME OTHER APPLICATIONS

- BIPOLAR POWER SUPPLY
- FUNCTION GENERATOR OUTPUT
- DEFLECTION COIL DRIVE
- AUDIO OUTPUT AMPLIFIER



HARRIS
SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-2640/2645

High Voltage Operational Amplifier

FEATURES

- OUTPUT VOLTAGE SWING $\pm 35V$
- SUPPLY VOLTAGE $\pm 10V$ to $\pm 40V$
- OFFSET CURRENT 5nA
- BANDWIDTH 4MHz
- SLEW RATE 5V/ μs
- COMMON MODE INPUT VOLTAGE SWING $\pm 35V$
- OUTPUT OVERLOAD PROTECTION

DESCRIPTION

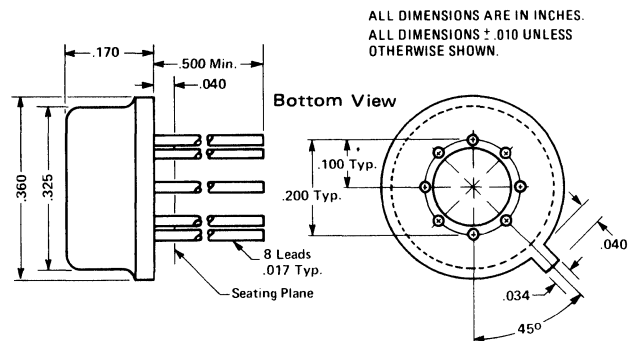
The HA-2640/2645 is a high voltage, high performance, internally compensated monolithic operational amplifier.

It is intended for use wherever a high output voltage range is required, or where high supply voltages (up to 80 Volts total) are encountered. Output current is limited by a chip temperature sensing circuit, providing positive protection against damage under any overload or output short circuit condition. The device may also be used as a pin for pin replacement for many general purpose op amps to achieve superior input current, bandwidth, and slew rate.

The HA-2640 has guaranteed operation over $-55^{\circ}C$ to $+125^{\circ}C$, while the HA-2645 is guaranteed over $0^{\circ}C$ to $+75^{\circ}C$.

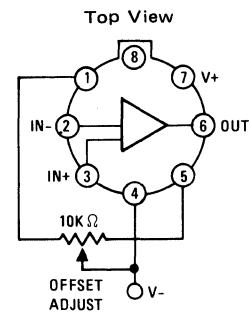
PACKAGE

CODE 2A T0-99

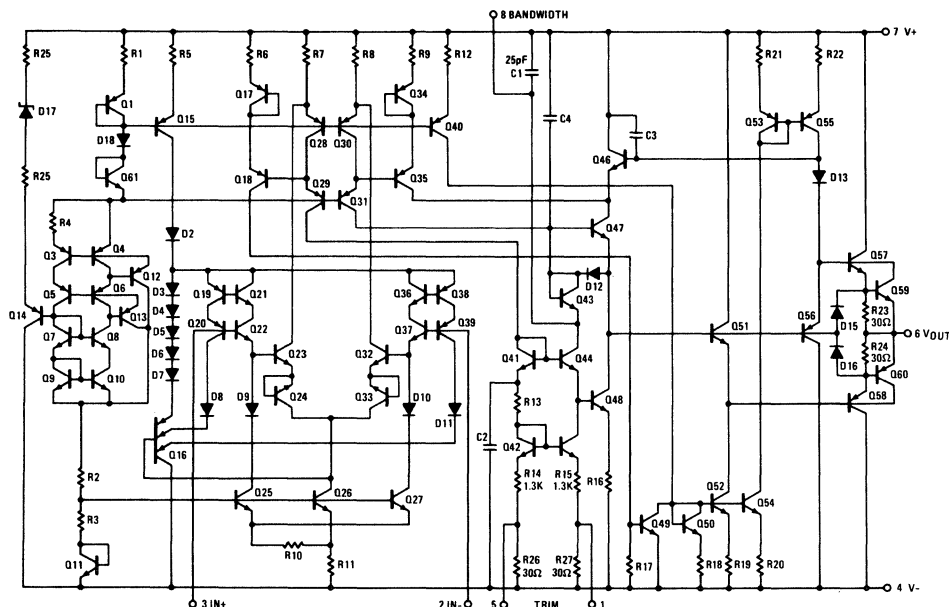


NOTE: 1. All leads gold plated KOVAR
2. All dimensions in inches

PIN OUT



SCHEMATIC DIAGRAM



LINEAR

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals 100V
 Input Voltage Range $\pm 37V$
 Output Current/Full Short Circuit Protection
 Internal Power Dissipation 680mW*

Operating Temperature Range
 $-55^{\circ}C \leq T_A \leq +125^{\circ}C$ (HA-2640)
 $0^{\circ}C \leq T_A \leq +75^{\circ}C$ (HA-2645)
 Storage Temperature Range
 $-65^{\circ}C \leq T_A \leq +150^{\circ}C$

*Derate by 4.6mW/ $^{\circ}C$ above +25 $^{\circ}C$

ELECTRICAL CHARACTERISTICS

V_{Supply} = $\pm 40V$, R_L = 5K, Unless Otherwise Specified.

PARAMETER	TEMP.	HA-2640 -55 $^{\circ}C$ to +125 $^{\circ}C$			HA-2645 0 $^{\circ}C$ to +75 $^{\circ}C$			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
INPUT CHARACTERISTICS								
* Offset Voltage	+25 $^{\circ}C$ Full		2 4 6		2 6 7			mV mV
Offset Voltage Average Drift	Full		15		15			$\mu V/^{\circ}C$
* Bias Current	+25 $^{\circ}C$ Full		10 25 50		12 30 50			nA nA
* Offset Current	+25 $^{\circ}C$ Full		5 12 35		15 30 50			nA nA
Input Resistance	+25 $^{\circ}C$	50	250		40	200		M Ω
Common Mode Range	Full	± 35			± 35			V
TRANSFER CHARACTERISTICS								
* Large Signal Voltage Gain (Note 8)	+25 $^{\circ}C$ Full	100K 75K	200K		100K 75K	200K		V/V V/V
* Common Mode Rejection Ratio (Note 1)	Full	80	100		74	100		dB
Unity Gain Bandwidth (Note 2)	+25 $^{\circ}C$		4		4			MHz
OUTPUT CHARACTERISTICS								
* Output Voltage Swing	Full	± 35			± 35			V
* Output Current (Note 9)	+25 $^{\circ}C$	± 12	± 15		± 10	± 12		mA
Output Resistance	+25 $^{\circ}C$		500			500		Ω
Full Power Bandwidth (Note 3)	+25 $^{\circ}C$		23			23		kHz
TRANSIENT RESPONSE (Note 7)								
Rise Time (Notes 4, 6)	+25 $^{\circ}C$		60			60		ns
Overshoot (Notes 4, 6)	+25 $^{\circ}C$		15			15		%
Slew Rate (Note 6)	+25 $^{\circ}C$		5			5		V/ μs
POWER SUPPLY CHARACTERISTICS								
* Supply Current	+25 $^{\circ}C$		3.2	3.8		3.2	4.5	mA
Supply Voltage Range	Full	± 10		± 40	± 10		± 40	V
* Power Supply Rejection Ratio (Note 5)	Full	80	90		74	90		dB

NOTES: 1. V_{CM} = $\pm 30V$
 2. V_O = 90mV

3. V_O = $\pm 35V$
 4. V_O = $\pm 200mV$

5. V_S = $\pm 10V$ to $\pm 40V$
 6. A_V = 1
 7. C_L = 50pF

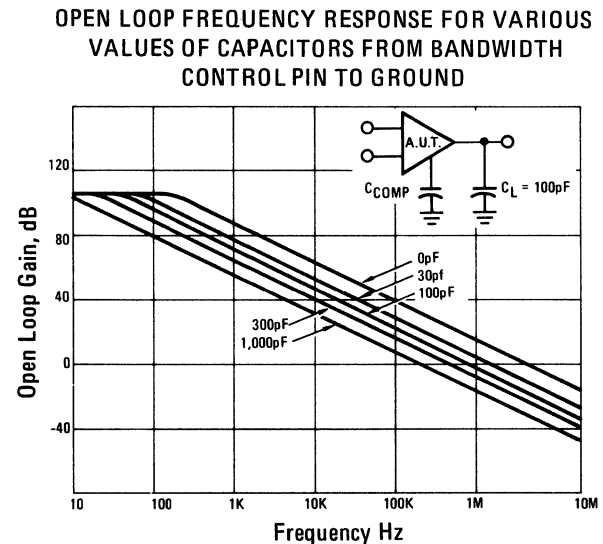
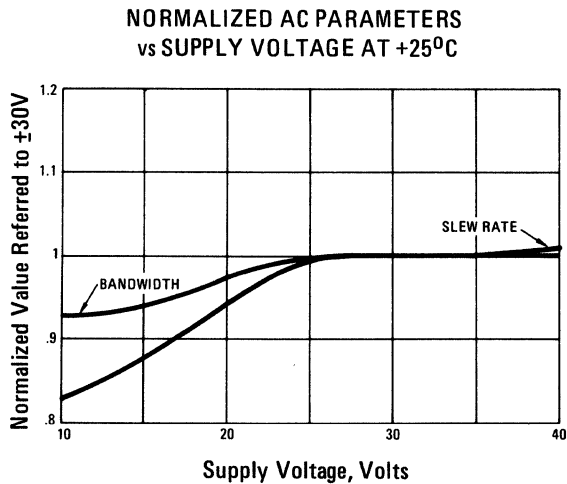
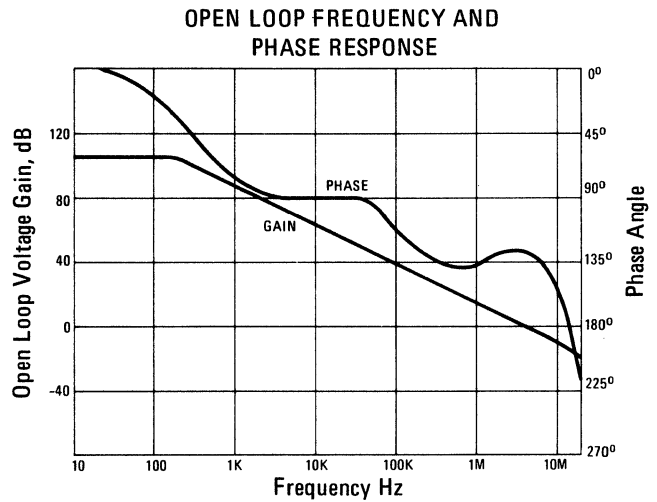
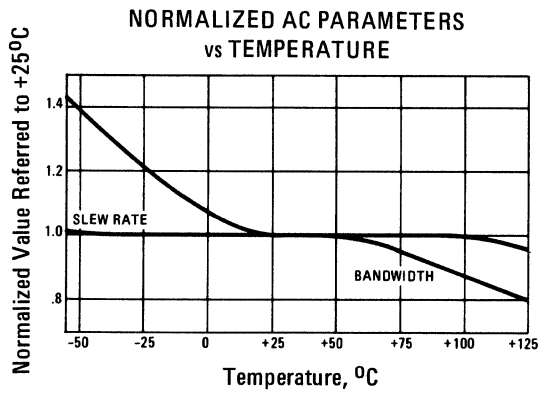
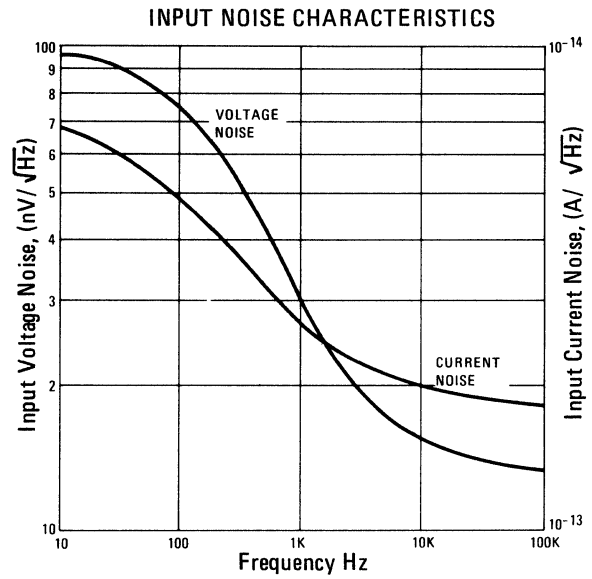
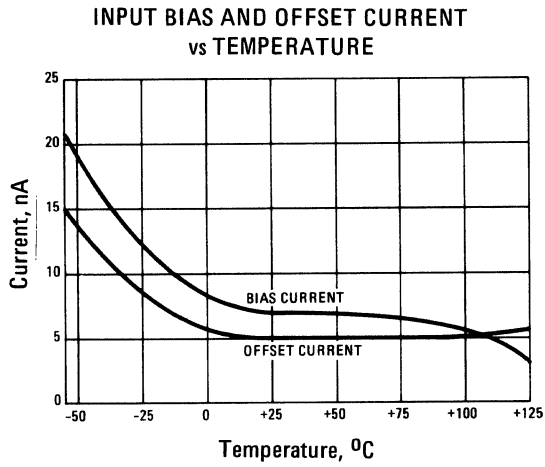
8. $\Delta V_O = \pm 30.0V$
 9. R_L = 1K Ω

*100% Tested For DASH 8

LINEAR

PERFORMANCE CURVES

$V_+ = V_- = 40\text{VDC}$, $T_A = +25^\circ\text{C}$ UNLESS OTHERWISE STATED

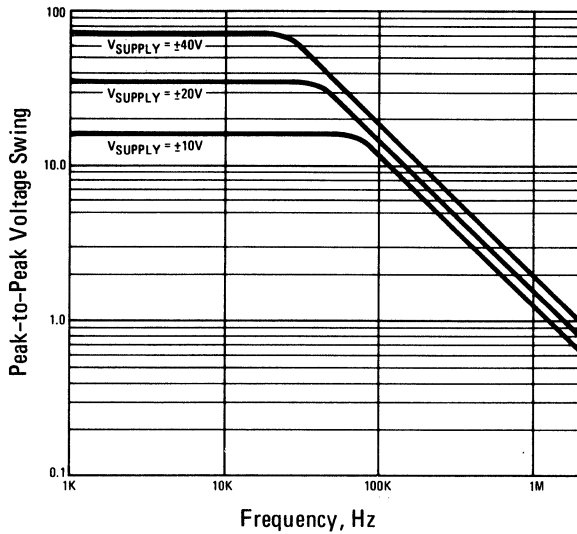


NOTE: External Compensation Components are not Required for Stability. But May be Added to Reduce Bandwidth if Desired. $C_L = 100\text{pF}$ is Also Required for Stability Only if External Compensation Capacitor is Used.

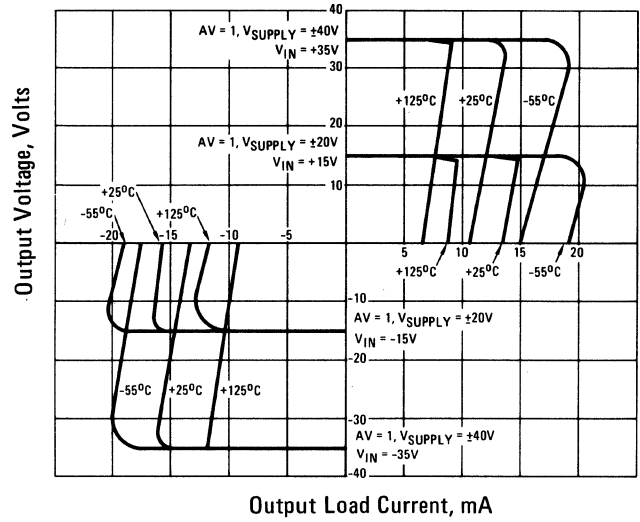
LINEAR

PERFORMANCE CURVES (continued)

**OUTPUT VOLTAGE SWING
vs FREQUENCY AT +25°C**



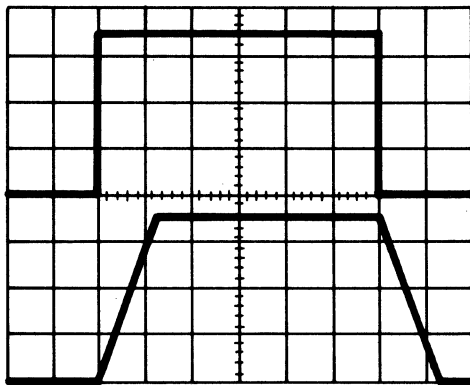
OUTPUT CURRENT CHARACTERISTIC



LINEAR

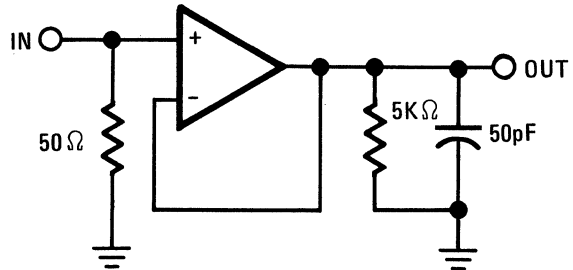
SWITCHING WAVEFORM AND TEST CIRCUIT

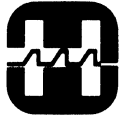
**VOLTAGE FOLLOWER
PULSE RESPONSE**



$R_L = 5K, C_L = 50pF$
 Vertical = 10V/Div. $T_A = +25^\circ C$
 Horizontal = 5 μs /Div. $V_S = \pm 40V$

**SLEW RATE AND TRANSIENT
RESPONSE TEST CIRCUIT**





HARRIS
SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-2650/2655

Dual High Performance Operational Amplifier

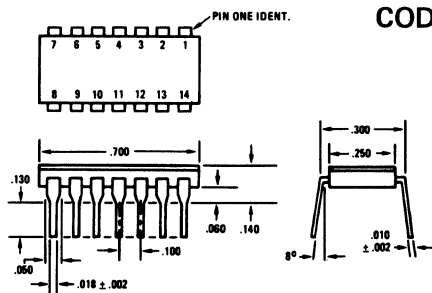
FEATURES

- Slew Rate $5V/\mu S$
- Bandwidth 8 MHz
- Bias Current 35 nA
- Av. Offset Voltage Drift $8\mu V/^{\circ}C$
- Power Consumption 75mW
- Supply Voltage Range $\pm 2V$ to $\pm 20V$

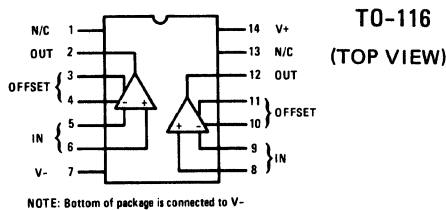
DESCRIPTION

The HA-2650/HA-2655 contains two internally compensated operational amplifiers on a single chip offering high slew rate and high frequency performance at no expense to DC performance. Applications of the device range from DC to high frequency video circuits; such as tone generators, active filters, integrators, high impedance buffers, etc. The device is available in the TO-116 DIP and the TO-99 metal can, in either the military or commercial temperature range.

PACKAGE/PINOUTS

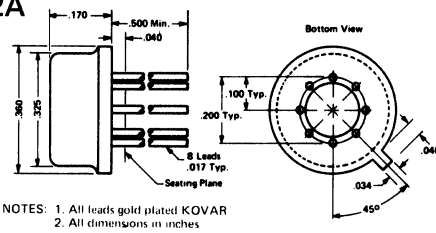


CODE 1S

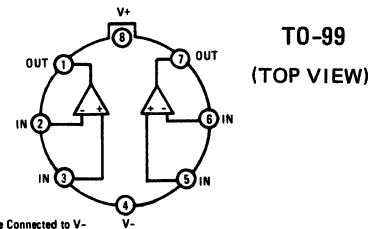


TO-116
(TOP VIEW)

CODE 2A

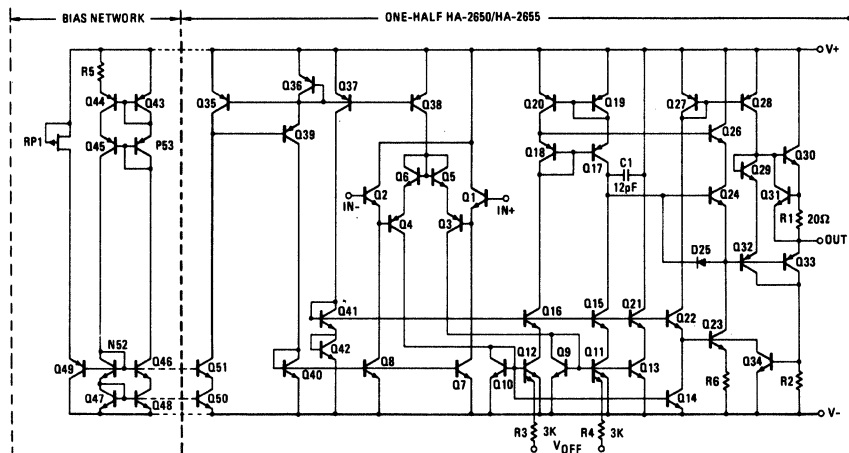


NOTES: 1. All leads gold plated KOVAR
2. All dimensions in inches



TO-99
(TOP VIEW)

SCHEMATIC DIAGRAM



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

$T_A = +25^\circ\text{C}$ Unless Otherwise Stated

Power Dissipation (Note 2) TO-99 300 mW
TO-116 300 mW

Voltage Between V+ and V- Terminals 40.0V
Differential Input Voltage $\pm 30.0\text{V}$
Input Voltage (Note 1) $\pm 15.0\text{V}$
Output Short Circuit Duration Indefinite

Operating Temperature Range:
HA-2650 $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$
HA-2655 $0^\circ\text{C} \leq T_A \leq +75^\circ\text{C}$
Storage Temperature Range $-65^\circ\text{C} \leq T_A \leq +150^\circ\text{C}$

ELECTRICAL CHARACTERISTICS

V+ = 15V V- = -15V

PARAMETER	TEMP.	HA-2650 -55°C to $+125^\circ\text{C}$			HA-2655 0°C to $+75^\circ\text{C}$			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
INPUT CHARACTERISTICS								
* Offset Voltage	$+25^\circ\text{C}$		1.5	3		2	5	mV
	Full			5			7	mV
Av. Offset Voltage Drift	Full		8			8		$\mu\text{V}/^\circ\text{C}$
* Bias Current	$+25^\circ\text{C}$		35	100		50	200	nA
	Full			200			300	nA
* Offset Current	$+25^\circ\text{C}$		1	30		2	60	nA
	Full			60			100	nA
Common Mode Range	Full	± 13			± 13			V
Differential Input Resistance	$+25^\circ\text{C}$	5	20		5	20		M Ω
Common Mode Input Resistance	$+25^\circ\text{C}$		500			500		M Ω
Input Capacitance	$+25^\circ\text{C}$		5			5		pF
TRANSFER CHARACTERISTICS								
* Large Signal Voltage Gain (Note 3a)	$+25^\circ\text{C}$	25K	40K		20K	40K		V/V
	Full	20K			15K			V/V
* Common Mode Rejection Ratio (Note 4)	$+25^\circ\text{C}$	80	100		74	100		dB
	Full	80			74			dB
OUTPUT CHARACTERISTICS								
* Output Voltage Swing (Note 3c)	$+25^\circ\text{C}$	± 13	± 14		± 13	± 14		V
	Full	± 13			± 13			V
Full Power Bandwidth (Note 5)	$+25^\circ\text{C}$	30	80		30	80		KHz
Output Current (Note 3a)	$+25^\circ\text{C}$		± 20			± 18		mA
Output Resistance	$+25^\circ\text{C}$		100			100		Ω
TRANSIENT RESPONSE (Note 6)								
Rise Time (Note 7)	$+25^\circ\text{C}$		40			40		ns
Overshoot (Note 7)	$+25^\circ\text{C}$		15			15		%
Slew Rate	$+25^\circ\text{C}$	± 2	± 5		± 2	± 5		V/ μs
POWER SUPPLY CHARACTERISTICS								
* Supply Current	$+25^\circ\text{C}$		2.5	3		3	4	mA
* Power Supply Rejection Ratio (Note 8)	$+25^\circ\text{C}$	80	100		74	100		dB
	Full	80			74			dB

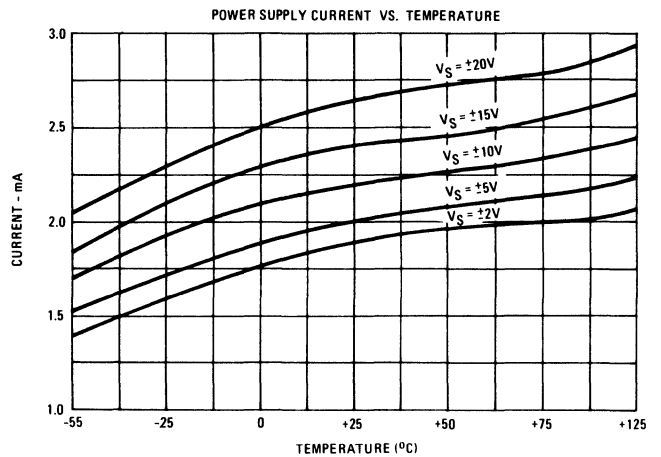
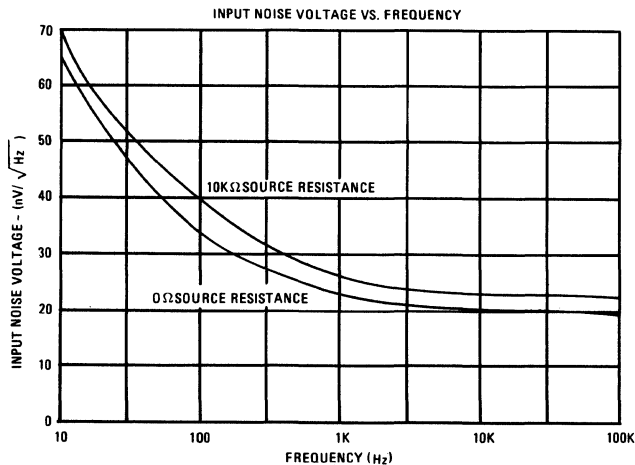
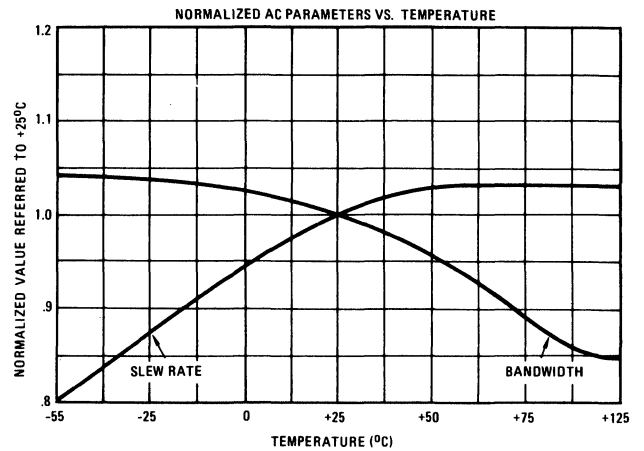
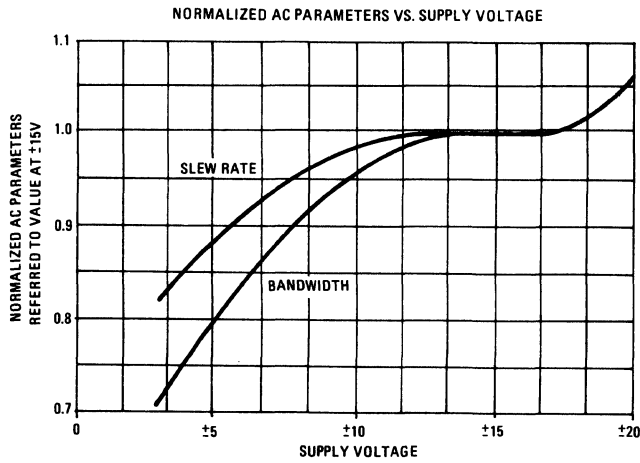
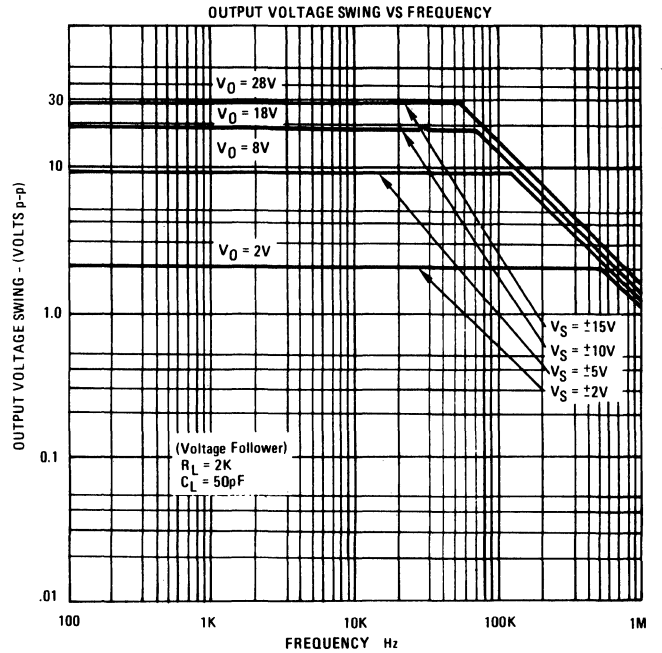
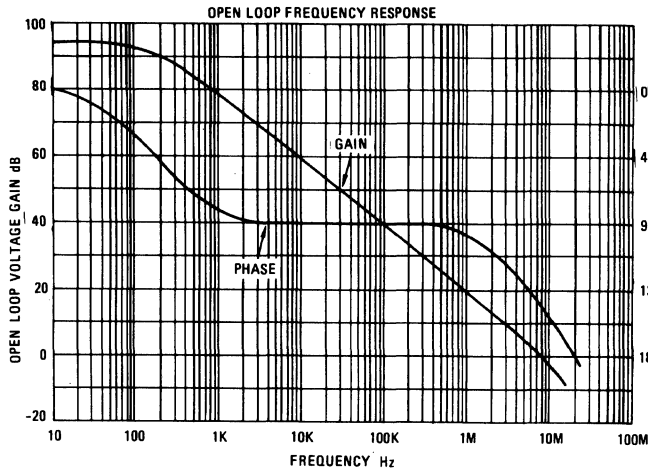
- NOTES: 1. For supply voltages less than $\pm 15\text{V}$, the absolute maximum input voltage is equal to the supply voltage.
2. Derate at $4.7\text{mW}/^\circ\text{C}$ at ambient temperatures above $+110^\circ\text{C}$.
3. (a) $V_O = \pm 10\text{V}$ (b) $R_L = 2\text{K}$ (c) $R_L = 10\text{K}$

4. $V_{CM} = \pm 5.0\text{V}$
5. $A_V = 1$, $R_L = 2\text{K}$, $V_O = 20\text{V}_{pp}$
6. See transient response/slew rate circuit.
7. $V_{in} = 200\text{mV}$
8. $\Delta V = \pm 5.0\text{V}$

* 100% Tested For DASH 8

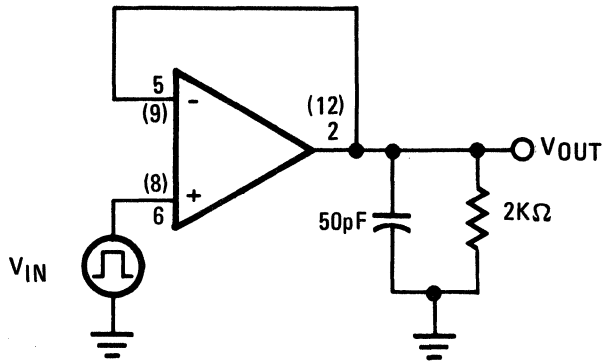
PERFORMANCE CURVES

$V_+ = +15V$, $V_- = -15V$, $T_A = +25^\circ C$ Unless Otherwise Stated.



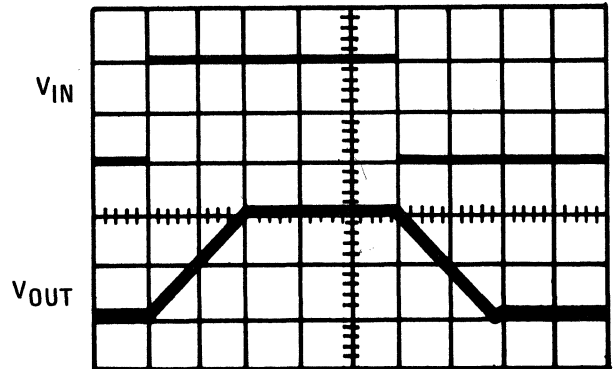
PERFORMANCE CHARACTERISTICS

TRANSIENT RESPONSE/SLEW RATE CIRCUIT



Note: Numbers in parentheses refer to the second half of TO-116 package.

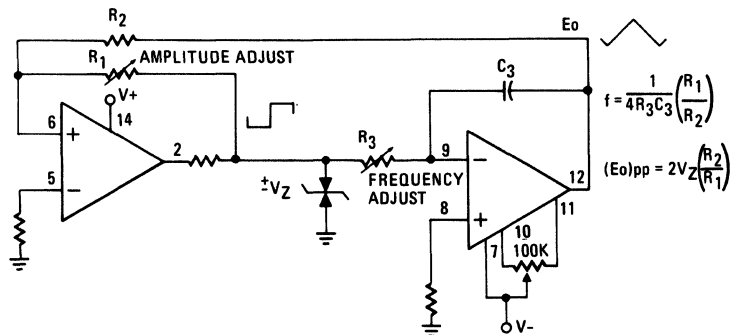
SLEWING WAVEFORM



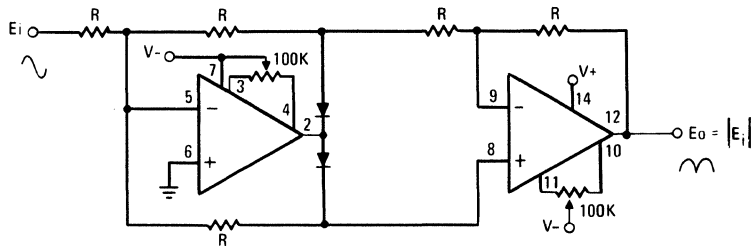
VERTICAL 5V/DIV. HORIZONTAL 1 μs/DIV.

TYPICAL APPLICATIONS

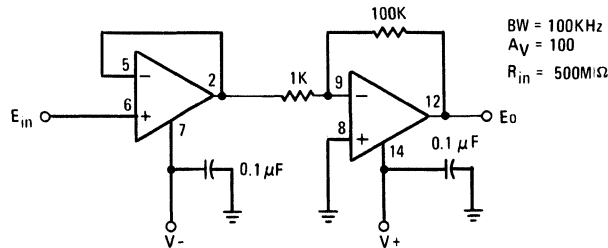
LOW COST HIGH FREQUENCY GENERATOR



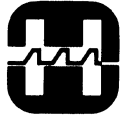
ABSOLUTE-VALUE CIRCUIT



HIGH IMPEDANCE HIGH GAIN HIGH FREQUENCY INVERTING AMP



BW = 100KHz
A_V = 100
R_{in} = 500MΩ



HARRIS
SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-2700/2704/2705

High Performance Operational Amplifiers

FEATURES

- | | | | |
|--------------------------|---------------------------|----------------------------------|---------------------------|
| • HIGH SLEW RATE | 20V/ μ s | • HIGH CM_{rr} | 106dB |
| • LOW POWER DISSIPATION | 2.25mW AT $\pm 15.0V$ | • WIDE POWER SUPPLY RANGE | $\pm 5.5V$ TO $\pm 20.0V$ |
| • HIGH OPEN LOOP GAIN | 300K ($R_L = 2K\Omega$) | • FULLY INTERNALLY COMPENSATED | |
| • LOW INPUT BIAS CURRENT | 5nA | • OUTPUT SHORT CIRCUIT PROTECTED | |
| • LOW OFFSET VOLTAGE | 0.5mV | • OFFSET NULL CAPABILITY | |

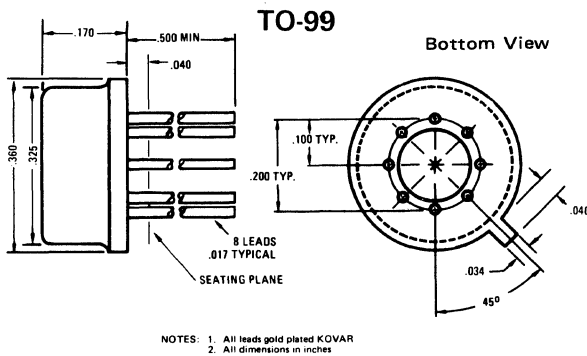
GENERAL DESCRIPTION

The HA-2700 is a general purpose amplifier which utilizes a revolutionary input circuit concept that makes possible operation at very low power levels without compromising large signal response characteristics or output drive capability. Advanced circuit design techniques and the use of vertical NPN and PNP transistors make possible the attainment of very high gain with a single stage of voltage amplification, thus ensuring closed loop stability even in the critical unity gain follower mode, without the use of external compensation components.

The circuit is intended for use in applications that require fast large signal response with low power dissipation and for instrumentation applications in which low offset voltage, current drift, large voltage gain and high common mode rejection are necessary. Full output short circuit protection and the large differential input breakdown enable the device to withstand a variety of fault conditions.

PACKAGES

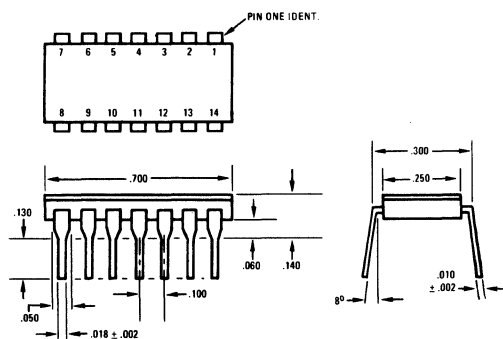
CODE 2A



CODE 1S

TO-116

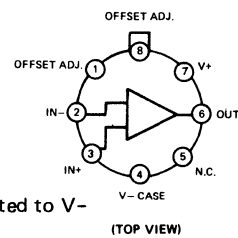
ALL DIMENSIONS ARE IN INCHES.
ALL DIMENSIONS $\pm .010$ UNLESS OTHERWISE SHOWN.



PIN OUT

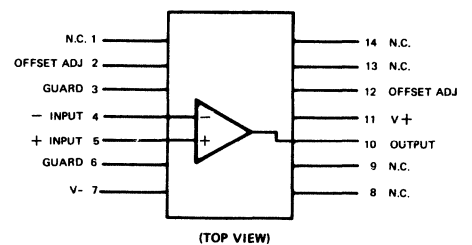
TO-99:

HA2-2700/HA2-2704/HA2-2705



TO-116:

HA1-2700/HA1-2704/HA1-2705



Case Connected to V-

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V ⁺ and V ⁻ Terminals	44.0V
Differential Input Voltage	±18.0V
Internal Power Dissipation (Note 7)	300mW
Storage Temperature	-65°C ≤ T _A ≤ +150°C

ELECTRICAL CHARACTERISTICS

V⁺ = +15.0 V.D.C.

V⁻ = -15.0 V.D.C.

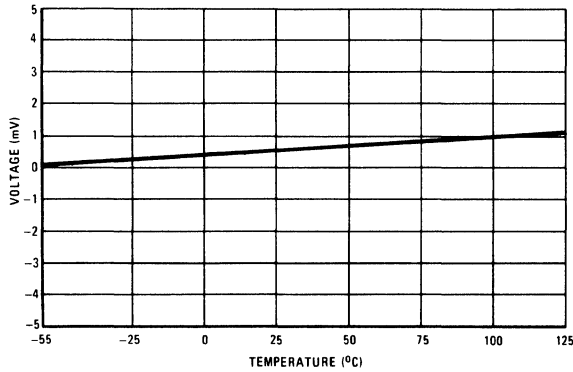
PARAMETER	TEMP.	HA-2700 -55°C to +125°C			HA-2704 -25°C to +85°C			HA-2705 0°C to +75°C			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
INPUT CHARACTERISTICS											
* Offset Voltage (Note 1)	+25°C Full		0.5	3.0 5.0		0.5	3.0 6.0		1.0	5.0 7.0	mV mV
* Bias Current	+25°C Full		5.0	20.0 50.0		5.0	20.0 50.0		5.0	40.0 70.0	nA nA
* Offset Current	+25°C Full		2.5	10.0 30.0		2.5	10.0 30.0		2.5	15.0 40.0	nA nA
Common Mode Range	Full	±11.0			±11.0			±11.0			V
TRANSFER CHARACTERISTICS											
* Large Signal Voltage Gain (Notes 2 & 3)	+25°C Full	200K 100K	300K		200K 100K	300K		200K 100K	300K		V/V V/V
* Common Mode Rejection Ratio (Note 4)	Full	86	106		86	106		80	106		dB
Gain Bandwidth Product (Note 2)	+25°C		1.0			1.0			1.0		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 2)	+25°C Full	±12.0 ±11.0	±13.0		±12.0 ±11.0	±13.0		±12.0 ±11.0	±13.0		V V
* Output Current (Note 3)	+25°C		10			10			10		mA
TRANSIENT RESPONSE CHARACTERISTICS											
* Slew Rate (Notes 2 & 6)	+25°C	10	20		10	20		10	20		V/μs
POWER SUPPLY CHARACTERISTICS											
* Supply Current	+25°C		75	150		75	150		75	150	μA
* Power Supply Rejection Ratio (Note 5)	Full	86	100		86	100		80	100		dB

- NOTES: 1. Can be adjusted to zero with 1 megohm pot between Pins 1 and 8 with the tap to Pin 7.
 2. R_L = 2K, C_L = 100pF
 3. V_O = ±10.0V
 4. V_{CM} = ±5.0V
 5. V_S = ±10.0V to ±20.0V
 6. A_V = 5
 7. Derate by 6.6 mW/°C above 105°C.

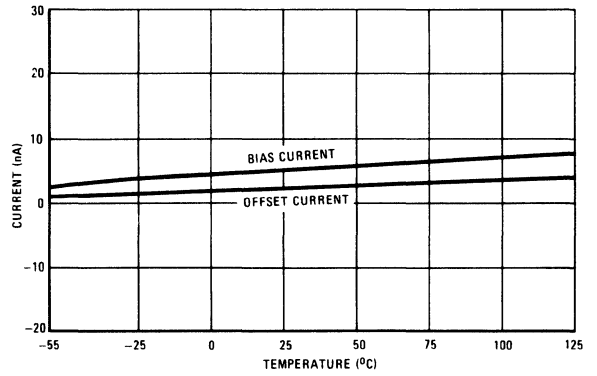
*100% Tested For DASH 8

TYPICAL PERFORMANCE CURVES

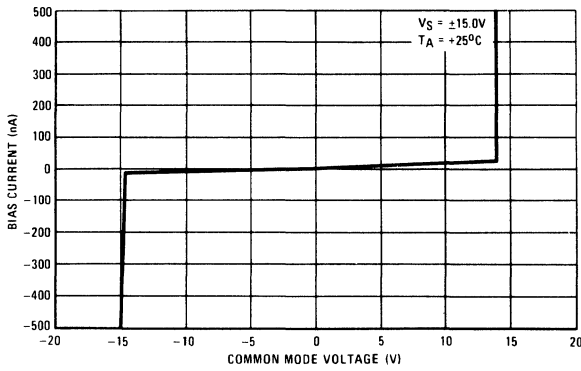
OFFSET VOLTAGE AS A FUNCTION OF TEMPERATURE



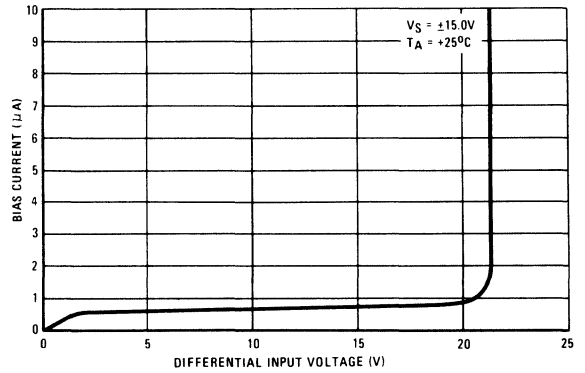
INPUT BIAS CURRENT AND OFFSET CURRENT AS A FUNCTION OF TEMPERATURE



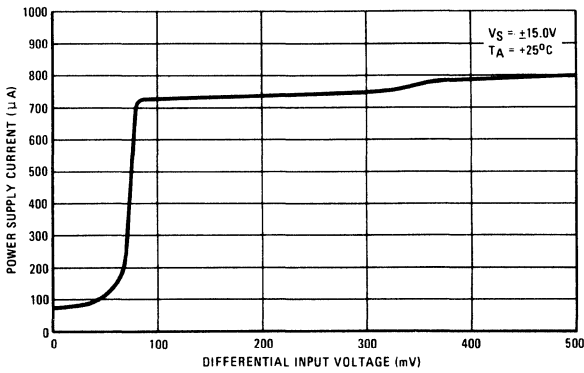
BIAS CURRENT AS A FUNCTION OF COMMON MODE VOLTAGE



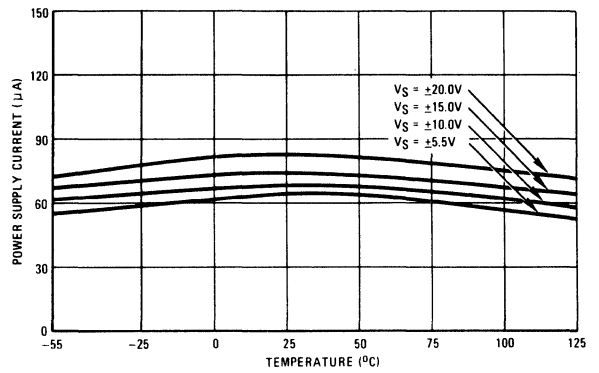
BIAS CURRENT AS A FUNCTION OF DIFFERENTIAL INPUT VOLTAGE



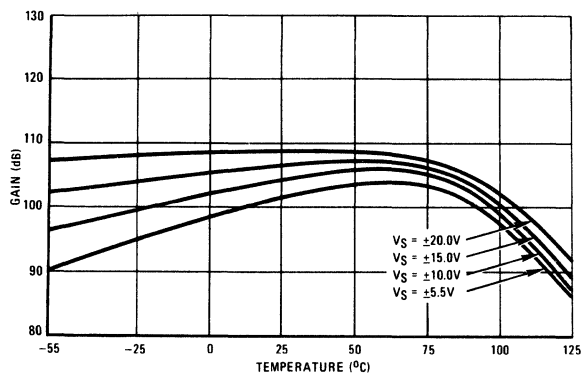
POWER SUPPLY CURRENT AS A FUNCTION OF DIFFERENTIAL INPUT VOLTAGE



POWER SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



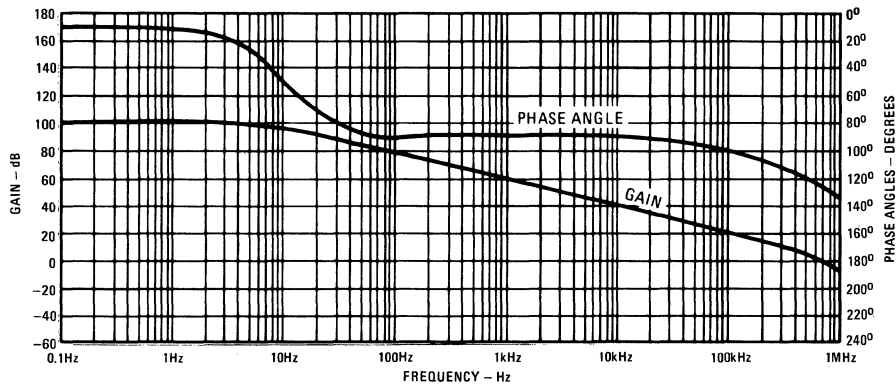
VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE



NOTE: Open loop (comparator) applications are not recommended, because of the above characteristic.

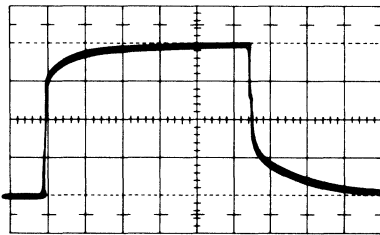
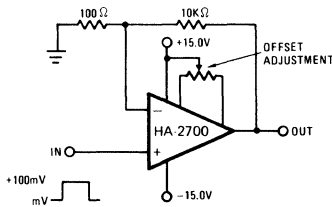
TYPICAL PERFORMANCE CURVES (continued)

PHASE-FREQUENCY RESPONSE FOR THE HA-2700



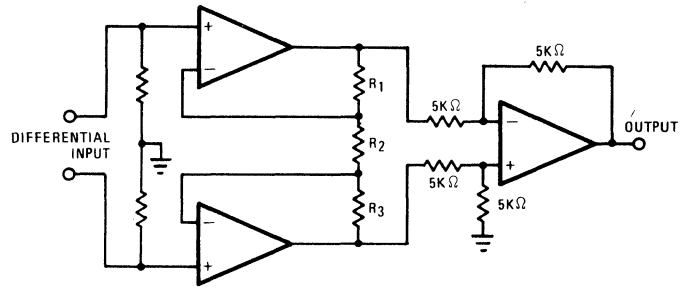
TYPICAL APPLICATIONS

HIGH GAIN AMPLIFIER (100 V/V)



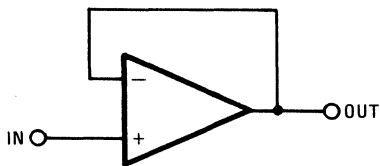
SCALE:
Horizontal - 20μs/division
Vertical - 5.0V/division

DIFFERENTIAL INPUT INSTRUMENTATION AMPLIFIER



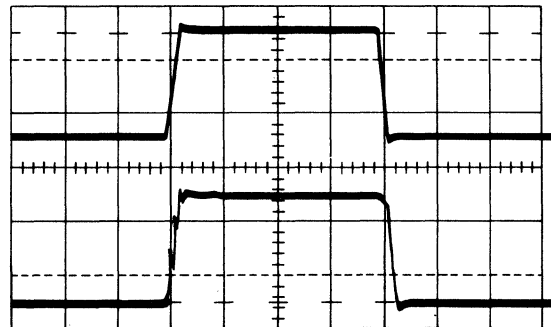
THE GAIN IS GIVEN BY:
$$\frac{(R_1 + R_2 + R_3)}{R_2} = G$$

UNITY GAIN VOLTAGE FOLLOWER



Non-inverting unity gain with a 2kΩ and 100pF load
TOP: $V_{IN} = 10.0V$ Peak to Peak
BOTTOM: V_{OUT}
SCALE: Horizontal - 1μs/division
Vertical - 5.0V/division

NOTE: Faster increase rise and fall time and increase distortion on output wave form.





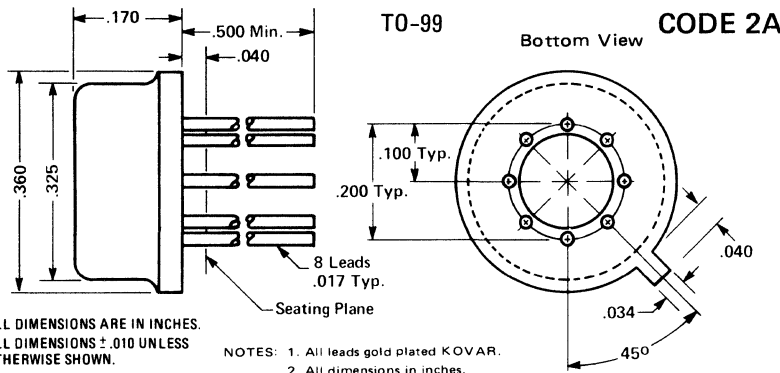
HARRIS
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A DIVISION OF HARRIS CORPORATION

HA-2720/2725

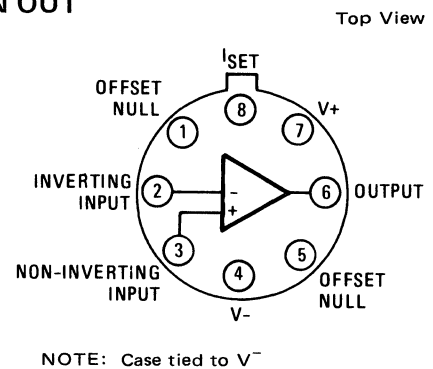
Wide Range Programmable Operational Amplifier

FEATURES	DESCRIPTION
<ul style="list-style-type: none"> ● WIDE RANGE A.C. PROGRAMMING <p>SLEW RATE: 0.06 TO 6V/μS GAIN X BANDWIDTH: 5KHz TO 10MHz</p> ● WIDE RANGE D.C. PROGRAMMING <p>POWER SUPPLY RANGE: $\pm 1.2V$ TO $\pm 18V$ SUPPLY CURRENT: 1 μA TO 1.5mA BIAS CURRENT: 0.4 TO 50nA</p> ● LOW NOISE ● SHORT CIRCUIT PROTECTION 	<p>The HA-2720/2725 Programmable Operational Amplifier is an internally compensated monolithic device offering wide range performance specifications. Parameters such as power dissipation, slew rate, bandwidth, noise and input DC parameters are programmed by selecting an external resistor or current source. Supply voltage as low as ± 3 volts may be used with little degradation of AC performance. Applications such as current controlled oscillators, active filters, modulators and sample and hold circuits can be derived easily by modulating the set current.</p> <p>The HA-2720 is guaranteed for operation from $-55^{\circ}C$ to $+125^{\circ}C$ while the HA-2725 is guaranteed from $0^{\circ}C$ to $+75^{\circ}C$.</p>

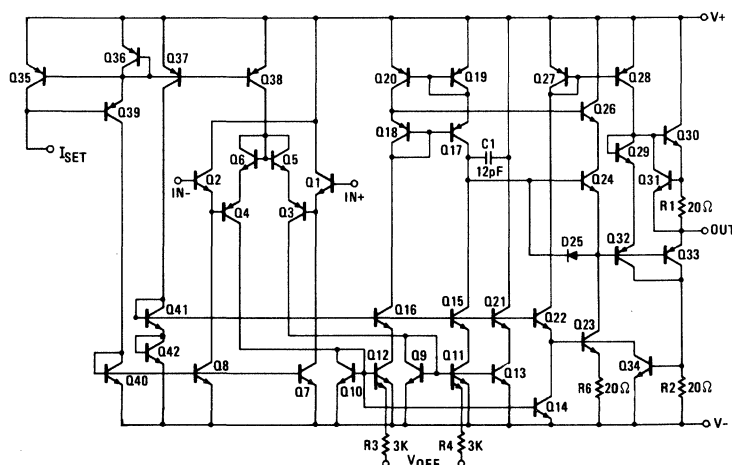
PACKAGE



PIN OUT



SCHEMATIC



LINEAR

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	45.0V	Power Dissipation (Note 2)	300mW
Differential Input Voltage	±30.0V	Operating Temperature Range:	
Input Voltage (Note 1)	±15.0V	HA-2720	-55°C ≤ T _A ≤ +125°C
I _{SET} (Current at I _{SET})	500μA	HA-2725	0°C ≤ T _A ≤ +75°C
V _{SET} (Voltage to Gnd. at I _{SET})	V+ - 2.0V ≤ V _{SET} ≤ V+	Storage Temperature Range	-65°C ≤ T _A ≤ +150°C

ELECTRICAL CHARACTERISTICS

V+ = +3.0V, V- = -3.0V

PARAMETER	TEMP.	HA-2720 -55°C to +125°C						HA-2725 0°C to +75°C						UNITS
		I _{SET} = 1.5μA			I _{SET} = 15μA			I _{SET} = 1.5μA			I _{SET} = 15μA			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
INPUT CHARACTERISTICS														
*Offset Voltage	25°C Full		2.0	3.0 5.0		2.0	3.0 5.0		2.0	5.0 7.0		2.0	5.0 7.0	mV mV
Offset Current	25°C Full		0.5	3.0 7.5		1.0	10 20		0.5	5.0 7.5		1.0	10 20	nA nA
Bias Current	25°C Full		2.0	5.0 10		8.0	20 40		2.0	10 10		8.0	30 40	nA nA
Input Resistance	25°C		50			5			50			5		MΩ
Input Capacitance	25°C		3.0			3.0			3.0			3.0		pF
TRANSFER CHARACTERISTICS														
*Large Signal Voltage Gain (Note 9)	25°C Full	20K 15K	40K		20K 15K	40K		15K 10K	40K		15K 10K	40K		V/V V/V
*Common Mode Rejection Ratio (Note 4)	Full	80			80			74			74			dB
OUTPUT CHARACTERISTICS														
*Output Voltage Swing (Note 3)	25°C Full	±2.0 ±2.0	±2.2		±2.0 ±1.9	±2.2		±2.0 ±2.0	±2.2		±2.0 ±2.0	±2.2		V V
Output Current (Note 5)	25°C		±0.2			±2.0			±0.2			±2.0		mA
Output Resistance	25°C		2K			500			2K			500		Ω
Output Short-Circuit Current	25°C		2.8			14			2.8			14		mA
TRANSIENT RESPONSE														
Rise Time (Note 6)	25°C		2.5			0.25			2.5			0.25		μs
Overshoot (Note 6)	25°C		5			10			5			10		%
Slew Rate (Note 7)	25°C		0.07			0.70			0.07			0.70		V/μs
POWER SUPPLY CHARACTERISTICS														
Supply Current	25°C Full		15	20		170	200		15	20		170	200	μA μA
*Power Supply Rejection Ratio (Note 8)	Full	100			100			150			150			μV/V

*100% Tested For DASH 8

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V+ = +15.0V, V- = -15.0V

PARAMETER	TEMP.	HA-2720 -55°C to +125°C						HA-2725 0°C to +75°C						UNITS
		I _{SET} = 1.5μA			I _{SET} = 15μA			I _{SET} = 1.5μA			I _{SET} = 15μA			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
INPUT CHARACTERISTICS														
*Offset Voltage	25°C Full		2.0	3.0		2.0	3.0		2.0	5.0		2.0	5.0	mV mV
*Offset Current	25°C Full		0.5	3.0		1.0	10		0.5	5.0		1.0	10	nA nA
*Bias Current	25°C Full		2.0	5.0		8.0	20		2.0	10		8.0	30	nA nA
Input Resistance	25°C		50		5				50		5			MΩ
Input Capacitance	25°C		3.0		3.0				3.0		3.0			pF
TRANSFER CHARACTERISTICS														
*Large Signal Voltage Gain (Notes 3 & 9)	25°C Full	40K 25K	100K		40K 25K	120K		25K 20K	100K		25K 20K	120K		V/V V/V
*Common Mode Rejection Ratio (Note 4)	25°C Full	80	90		80	90		74	90		74	90		dB dB
OUTPUT CHARACTERISTICS														
*Output Voltage Swing (Note 3)	25°C Full	±12 ±10	±13.5		±12 ±10	±13.5		±12 ±10	±13.5		±12 ±10	±13.5		V V
Output Current (Note 5)	25°C		±0.5			±5.0			±0.5			±5.0		mA
Output Resistance	25°C		2K			500			2K			500		Ω
Output Short-Circuit Current	25°C		3.7			19			3.7			19		mA
TRANSIENT RESPONSE														
Rise Time (Note 6)	25°C		2.0			0.2			2.0			0.2		μs
Overshoot (Note 6)	25°C		5			15			5			15		%
Slew Rate (Note 7)	25°C		0.1			0.8			0.1			0.8		V/μs
POWER SUPPLY CHARACTERISTICS														
*Supply Current	25°C Full		20			210			20			210		μA μA
*Power Supply Rejection Ratio (Note 8)	Full	100			100			150			150			μV/V

NOTES: 1. For supply voltages less than ±15.0V, the absolute maximum input voltage is equal to supply voltage.
2. Derate at 6.8mW/°C for operation ambient temperatures above 75°C.

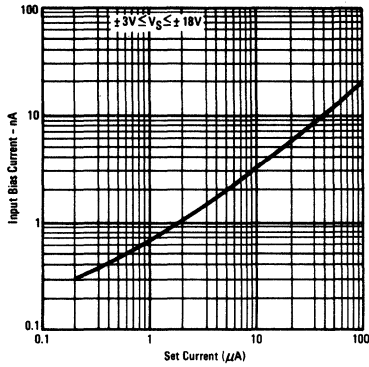
V _{SUPPLY} = ±3.0V	V _{SUPPLY} = ±15.0V	I _{SET} = 1.5μA	I _{SET} = 15μA
3. T = +25°C and Full	T = +25°C	R _L = 75KΩ	R _L = 5KΩ
—	T = Full	R _L = 75KΩ	R _L = 75KΩ
4. V _{CM} = ±1.5V	V _{CM} = ±5.0V		
5. V _O = ±2.0V	V _O = ±10.0V		
6. ← A _V = +1, V _{IN} = 400mV, R _L = 5K, C _L = 100pF →		R _L = 20K	R _L = 5K
7. V _O = ±2.0V	V _O = ±10.0V		
8. ΔV = ±1.5V	ΔV = ±5.0V		
9. V _O = ±1.0V	V _O = ±10.0V		

*100% Tested For DASH 8

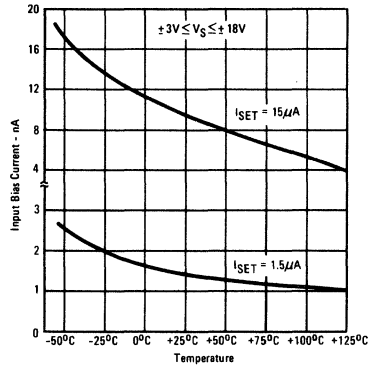
PERFORMANCE CURVES

UNLESS OTHERWISE NOTED: $T_A = +25^{\circ}\text{C}$, $V_S = \pm 15\text{VDC}$

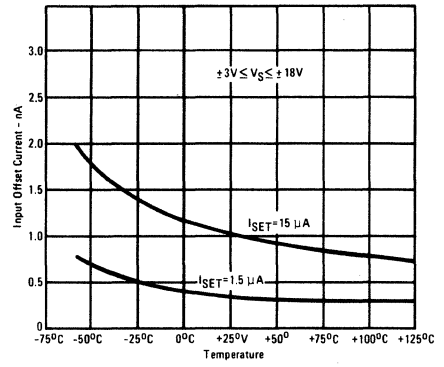
INPUT BIAS CURRENT vs. SET CURRENT



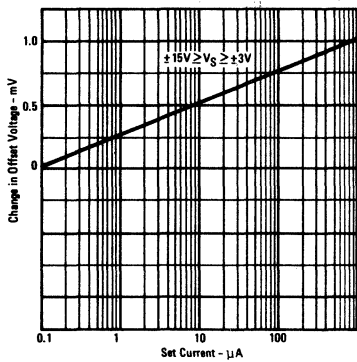
INPUT BIAS CURRENT vs. TEMPERATURE



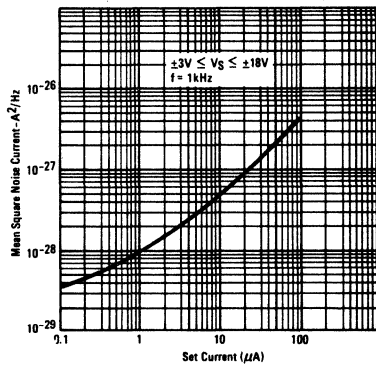
INPUT OFFSET CURRENT vs. TEMPERATURE



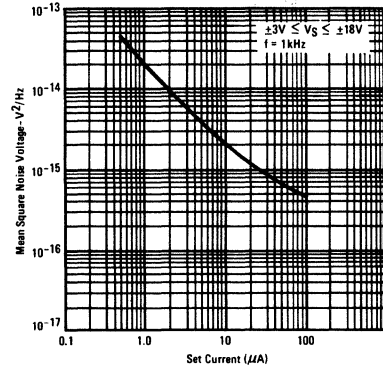
CHANGE IN OFFSET VOLTAGE vs. ISET (UNNULLED)



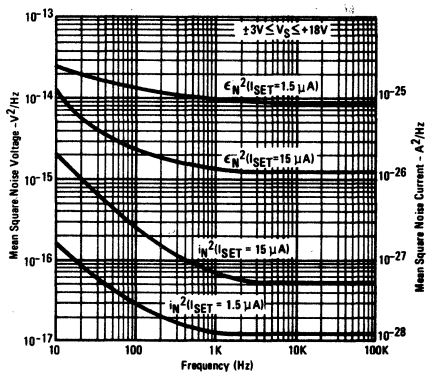
INPUT NOISE CURRENT vs. ISET



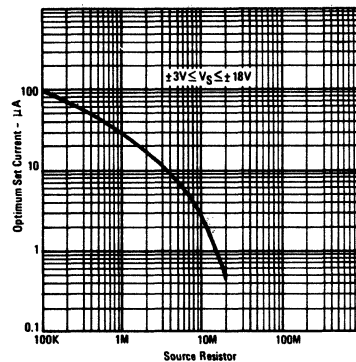
INPUT NOISE VOLTAGE vs. ISET



INPUT NOISE VOLTAGE AND CURRENT vs. FREQUENCY



OPTIMUM SET CURRENT FOR MINIMUM NOISE vs. SOURCE RESISTOR

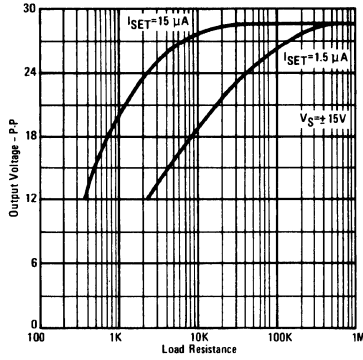


LINEAR

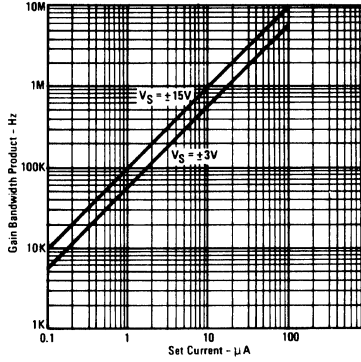
PERFORMANCE CURVES

UNLESS OTHERWISE NOTED: $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{VDC}$

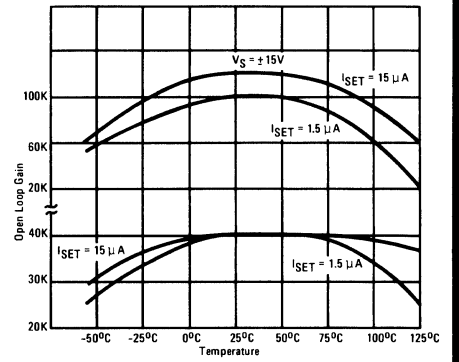
MAXIMUM OUTPUT VOLTAGE SWING
vs. LOAD RESISTANCE



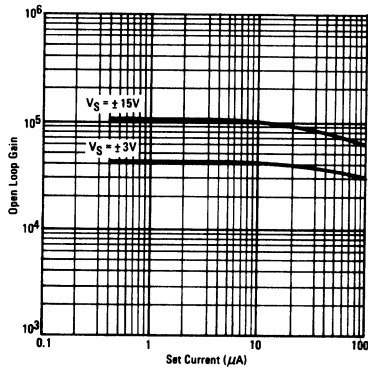
GAIN BANDWIDTH PRODUCT
vs. I_{SET}



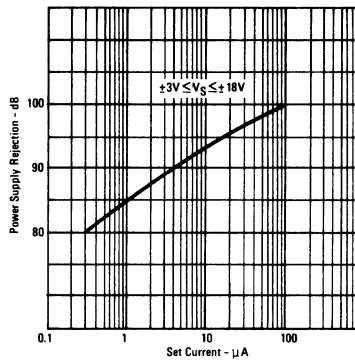
OPEN LOOP VOLTAGE GAIN
vs. TEMPERATURE



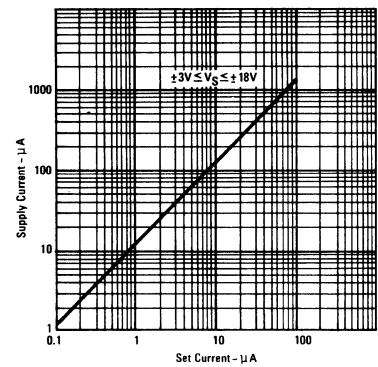
OPEN LOOP VOLTAGE GAIN
vs. I_{SET}



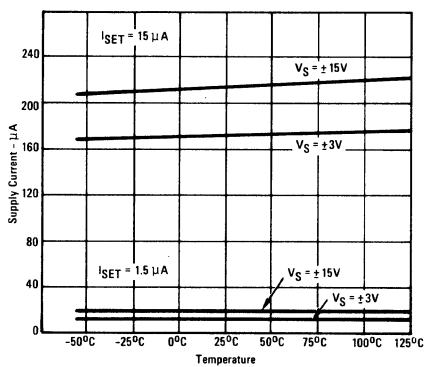
POWER SUPPLY REJECTION
vs. I_{SET}



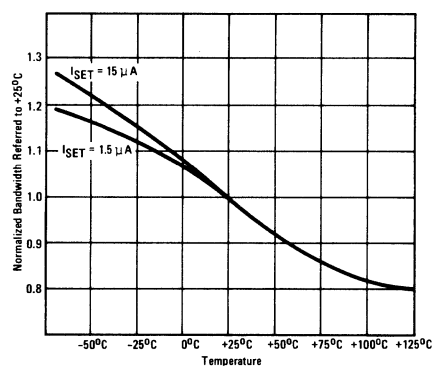
STANDBY SUPPLY CURRENT
vs. I_{SET}



SUPPLY CURRENT vs.
TEMPERATURE

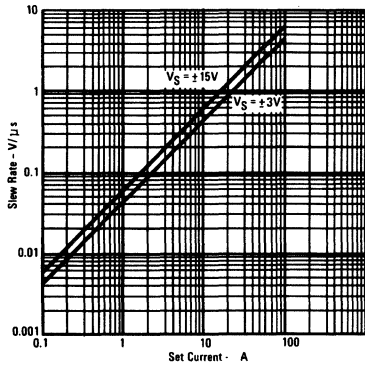


NORMALIZED BANDWIDTH
vs. TEMPERATURE

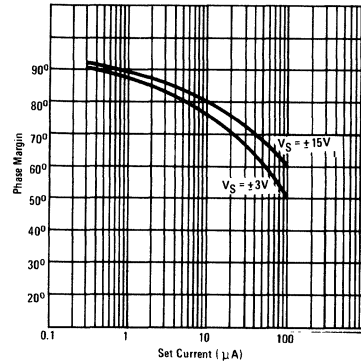


PERFORMANCE CURVES

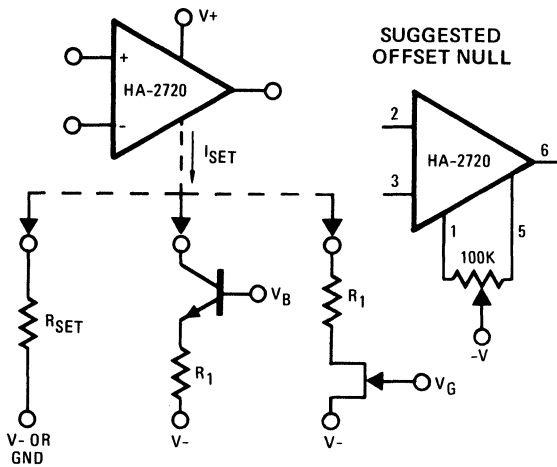
SLEW RATE vs. I_{SET}



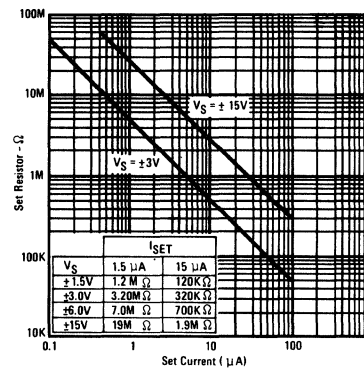
PHASE MARGIN vs. SET CURRENT



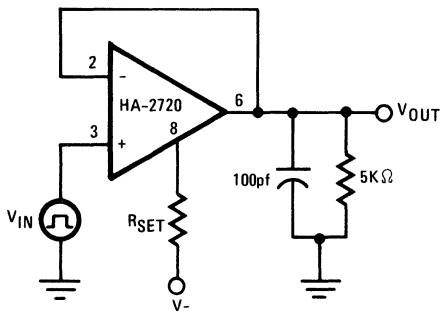
TYPICAL BIASING CIRCUITS



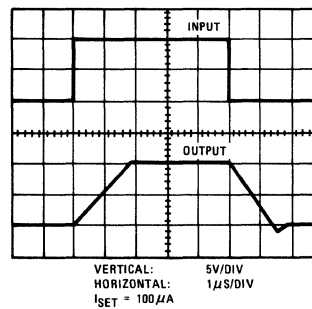
SET CURRENT VS. SET RESISTOR



TRANSIENT RESPONSE/SLEW RATE CIRCUIT



SLEWING WAVEFORM



LINEAR



HARRIS
SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-2730/2735

Wide Range Dual Programmable Operational Amplifier

FEATURES

- WIDE RANGE A.C. PROGRAMMING
 - SLEW RATE: 0.06 TO 6V/ μ s
 - GAIN X BANDWIDTH: 5kHz TO 10MHz
- WIDE RANGE D.C. PROGRAMMING
 - POWER SUPPLY RANGE: $\pm 1.2V$ TO $\pm 18V$
 - SUPPLY CURRENT: 1 μ A TO 1.5mA
 - BIAS CURRENT: 0.4 TO 50nA
- LOW NOISE
- MONOLITHIC CONSTRUCTION
- SHORT CIRCUIT PROTECTION

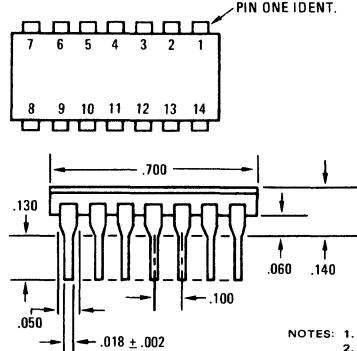
DESCRIPTION

The HA-2730/2735 Dual Programmable Operational Amplifiers consist of two HA-2720 type op amps on a single monolithic chip. It features the same performance characteristics as the HA-2720/2725 and in addition offers closer thermal tracking, reduced size weight, and greater reliability than two single devices. The HA-2730/2735 is programmed by selecting two external bias resistors or current sources for independent control of each side. Applications such as current controlled oscillators, active filters, modulators and sample and hold circuits can be derived easily by modulating the set current.

The HA-2730 is guaranteed for operation from $-55^{\circ}C$ to $+125^{\circ}C$ while the HA-2735 is guaranteed from $0^{\circ}C$ to $+75^{\circ}C$.

PACKAGE

CODE 1S

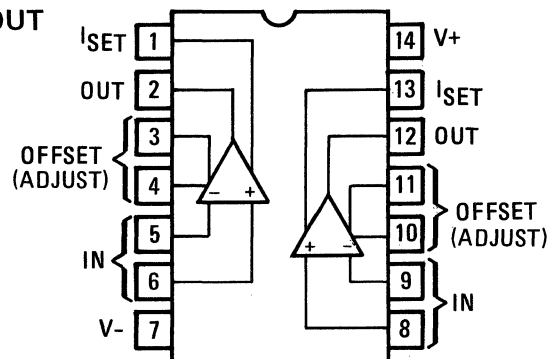


14 LEAD BRAZED D.I.P.

ALL DIMENSIONS ARE IN INCHES.
ALL DIMENSIONS $\pm .010$ UNLESS OTHERWISE SHOWN.

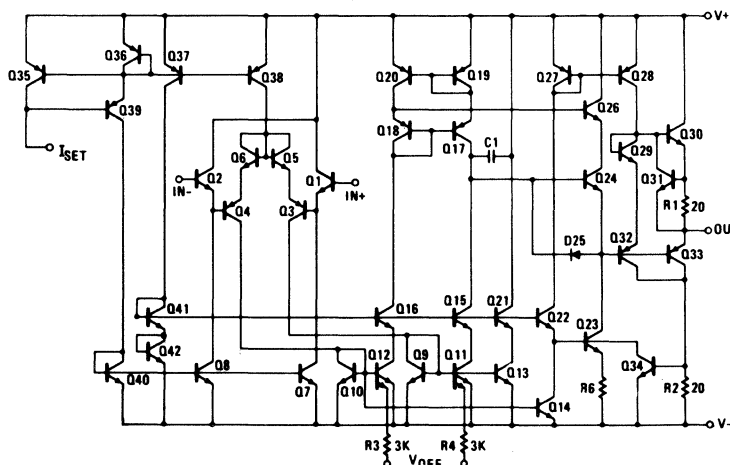
NOTES: 1. All leads and base gold plated KOVAR.
2. All dimensions in inches.

PIN OUT



NOTE: Bottom of package is connected to V-.

SCHEMATIC



(ONE HALF ONLY)
HA-2730/2735

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	45.0V	Power Dissipation (Note 2)	500mW
Differential Input Voltage	±30.0V	Operating Temperature Range:	
Input Voltage (Note 1)	±15.0V	HA-2730	-55°C ≤ T _A ≤ +125°C
I _{SET} (Current at I _{SET})	500μA	HA-2735	0°C ≤ T _A ≤ +75°C
V _{SET} (Voltage to Gnd. at I _{SET})	V+ - 2.0V ≤ V _{SET} ≤ V+	Storage Temperature Range	-65°C ≤ T _A ≤ +150°C

ELECTRICAL CHARACTERISTICS (Each Side)

V+ = +3.0V, V- = -3.0V

PARAMETER	TEMP.	HA-2730 -55°C to +125°C						HA-2735 0°C to +75°C						UNITS
		I _{SET} = 1.5μA			I _{SET} = 15μA			I _{SET} = 1.5μA			I _{SET} = 15μA			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
INPUT CHARACTERISTICS														
*Offset Voltage	25°C Full		2.0 3.0 5.0			2.0 3.0 5.0			2.0 5.0 7.0		2.0 5.0 7.0		mV mV	
Offset Current	25°C Full		0.5 3.0 7.5			1.0 10 20			0.5 5.0 7.5		1.0 10 20		nA nA	
Bias Current	25°C Full		2.0 5.0 10			8.0 20 40			2.0 10 10		8.0 30 40		nA nA	
Input Resistance	25°C		50			5			50		5		MΩ	
Input Capacitance	25°C		3.0			3.0			3.0		3.0		pF	
TRANSFER CHARACTERISTICS														
*Large Signal Voltage Gain (Notes 3 & 9)	25°C Full	20K 15K	40K		20K 15K	40K		15K 10K	40K		15K 10K	40K	V/V V/V	
*Common Mode Rejection Ratio (Note 4)	Full	80			80			74			74		dB	
OUTPUT CHARACTERISTICS														
*Output Voltage Swing (Note 3)	25°C Full	±2.0 ±2.0	±2.2		±2.0 ±1.9	±2.2		±2.0 ±2.0	±2.2		±2.0 ±2.0	±2.2	V V	
Output Current (Note 5)	25°C		±0.2			±2.0			±0.2			±2.0	mA	
Output Resistance	25°C		2K			500			2K			500	Ω	
Output Short-Circuit Current	25°C		2.8			14			2.8			14	mA	
TRANSIENT RESPONSE														
Rise Time (Note 6)	25°C		2.5			0.25			2.5			0.25	μs	
Overshoot (Note 6)	25°C		5			10			5			10	%	
Slew Rate (Note 7)	25°C		0.07			0.70			0.07			0.70	V/μs	
POWER SUPPLY CHARACTERISTICS														
*Supply Current (Each Amp)	25°C Full		15 20			170 200			15 20			170 200	μA μA	
*Power Supply Rejection Ratio (Note 8)	Full	100			100			150			150		μV/V	

*100% Tested For DASH 8

LINEAR

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (Each Side)

V+ = +15.0V, V- = -15.0V

PARAMETER	TEMP.	HA-2730 -55°C to +125°C						HA-2735 0°C to +75°C						UNITS
		I _{SET} = 1.5μA			I _{SET} = 15μA			I _{SET} = 1.5μA			I _{SET} = 15μA			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
INPUT CHARACTERISTICS														
*Offset Voltage	25°C Full		2.0	3.0 5.0		2.0	3.0 5.0		2.0	5.0 7.0		2.0	5.0 7.0	mV mV
*Offset Current	25°C Full		0.5	3.0 7.5		1.0	10 20		0.5	5.0 7.5		1.0	10 20	nA nA
*Bias Current	25°C Full		2.0	5.0 10		8.0	20 40		2.0	10 10		8.0	30 40	nA nA
Input Resistance	25°C		50			5			50			5		MΩ
Input Capacitance	25°C		3.0			3.0			3.0			3.0		pF
TRANSFER CHARACTERISTICS														
*Large Signal Voltage Gain (Notes 3 & 9)	25°C Full	40K 25K	100K		40K 25K	120K		25K 20K	100K		25K 20K	120K		V/V V/V
*Common Mode Rejection Ratio (Note 4)	25°C Full	80	90		80	90		74	90		74	90		dB dB
OUTPUT CHARACTERISTICS														
*Output Voltage Swing (Note 3)	25°C Full	±12 ±10	±13.5		±12 ±10	±13.5		±12 ±10	±13.5		±12 ±10	±13.5		V V
Output Current (Note 5)	25°C		±0.5			±5.0			±0.5			±5.0		mA
Output Resistance	25°C		2K			500			2K			500		Ω
Output Short-Circuit Current	25°C		3.7			19			3.7			19		mA
TRANSIENT RESPONSE														
Rise Time (Note 6)	25°C		2.0			0.2			2.0			0.2		μs
Overshoot (Note 6)	25°C		5			15			5			15		%
Slew Rate (Note 7)	25°C		0.1			0.8			0.1			0.8		V/μs
POWER SUPPLY CHARACTERISTICS														
*Supply Current (Each Amp)	25°C Full		20	25		210	250		20	25		210	250	μA μA
*Power Supply Rejection Ratio (Note 8)	Full	100			100			150			150			μV/V

- NOTES: 1. For supply voltages less than ±15.0V, the absolute maximum input voltage is equal to supply voltage.
2. Derate at 4.7mW/°C at ambient temperatures above 68°C.

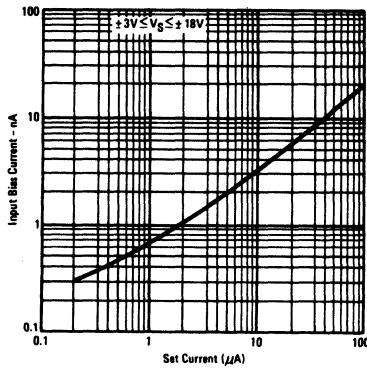
$V_{SUPPLY} = \pm 3.0V$	$V_{SUPPLY} = \pm 15.0V$	$I_{SET} = 1.5\mu A$	$I_{SET} = 15\mu A$
3. T = +25°C and Full	T = +25°C	$R_L = 75K\Omega$	$R_L = 5K\Omega$
—	T = Full	$R_L = 75K\Omega$	$R_L = 75K\Omega$
4. $V_{CM} = \pm 1.5V$	$V_{CM} = \pm 5.0V$		
5. $V_O = \pm 2.0V$	$V_O = \pm 10.0V$		
6. $\leftarrow A_V = +1, V_{IN} = 400mV, R_L = 5K, C_L = 100pF \rightarrow$			
7. $V_O = \pm 2.0V$	$V_O = \pm 10.0V$	$RR_L = 20K$	$R_L = 5K$
8. $\Delta V = \pm 1.5V$	$\Delta V = \pm 5.0V$		
9. $V_O = \pm 1.0V$	$V_O = \pm 10.0V$		

*100% Tested For DASH 8

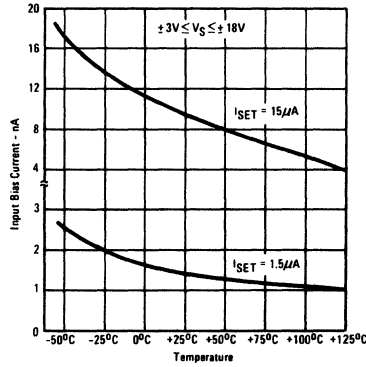
PERFORMANCE CURVES

UNLESS OTHERWISE NOTED: $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{VDC}$

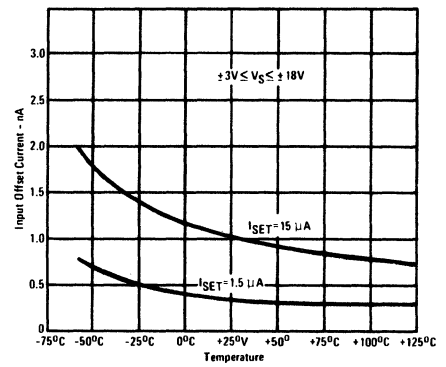
INPUT BIAS CURRENT vs. SET CURRENT



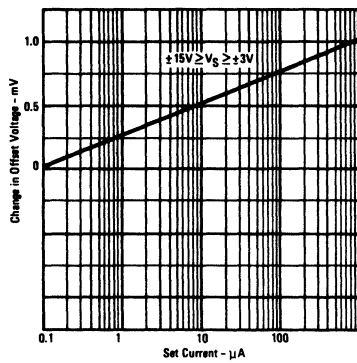
INPUT BIAS CURRENT vs. TEMPERATURE



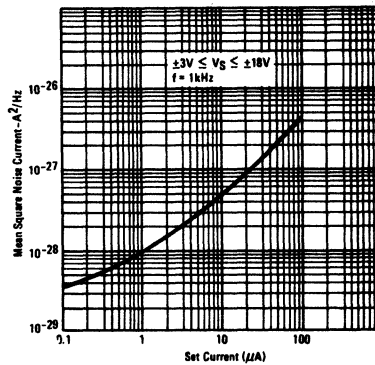
INPUT OFFSET CURRENT vs. TEMPERATURE



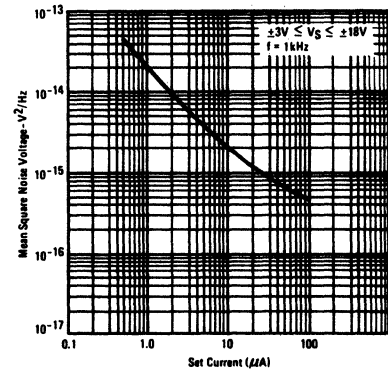
CHANGE IN OFFSET VOLTAGE vs. I_SET (UNNULLED)



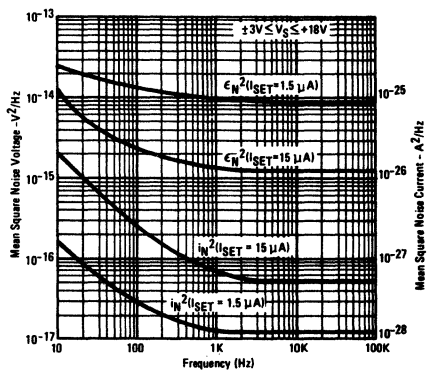
INPUT NOISE CURRENT vs. I_SET



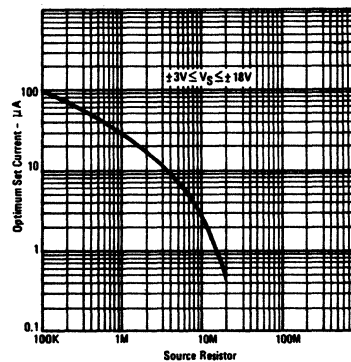
INPUT NOISE VOLTAGE vs. I_SET



INPUT NOISE VOLTAGE AND CURRENT vs. FREQUENCY



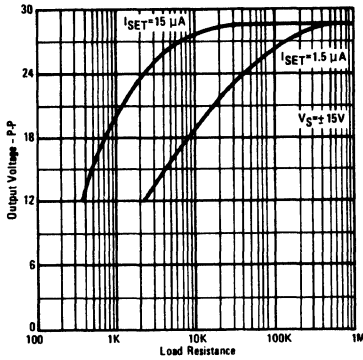
OPTIMUM SET CURRENT FOR MINIMUM NOISE vs. SOURCE RESISTOR



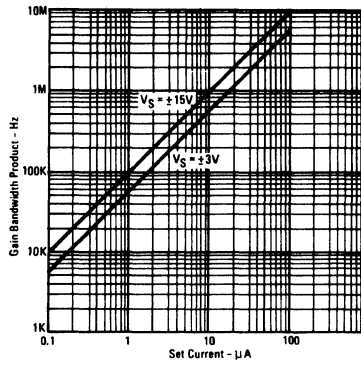
PERFORMANCE CURVES

UNLESS OTHERWISE NOTED: $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{VDC}$

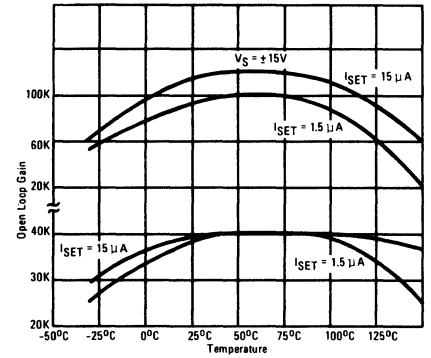
MAXIMUM OUTPUT VOLTAGE SWING
vs. LOAD RESISTANCE



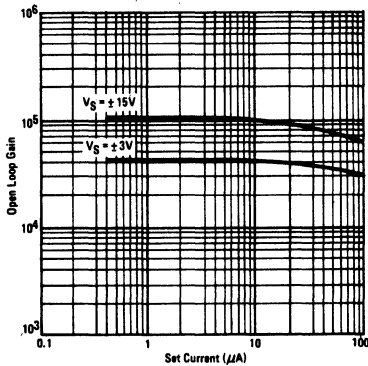
GAIN BANDWIDTH PRODUCT
vs. I_{SET}



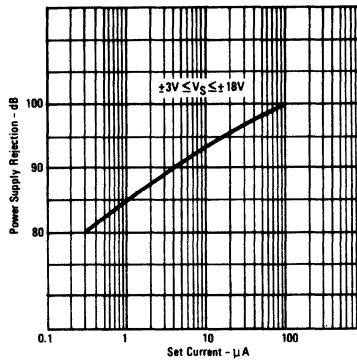
OPEN LOOP VOLTAGE GAIN
vs. TEMPERATURE



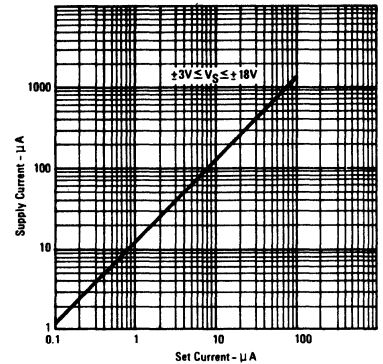
OPEN LOOP VOLTAGE GAIN
vs. I_{SET}



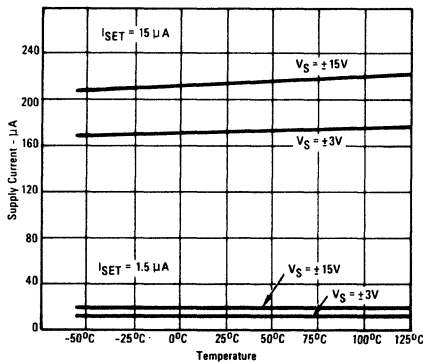
POWER SUPPLY REJECTION
vs. I_{SET}



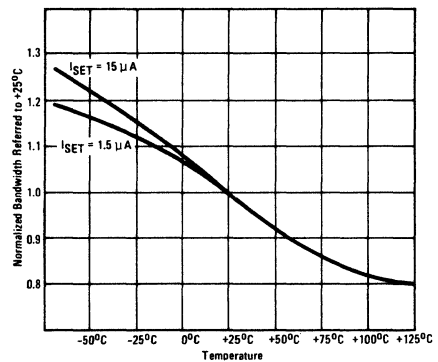
STANDBY SUPPLY CURRENT
vs. I_{SET}



SUPPLY CURRENT vs.
TEMPERATURE



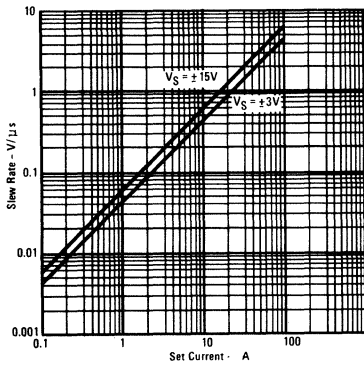
NORMALIZED BANDWIDTH
vs. TEMPERATURE



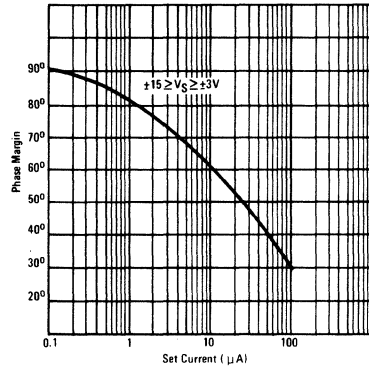
LINEAR

PERFORMANCE CURVES

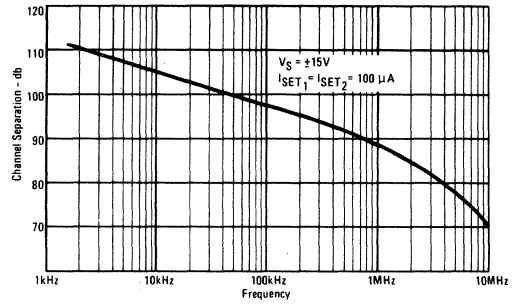
SLEW RATE vs. I_{SET}



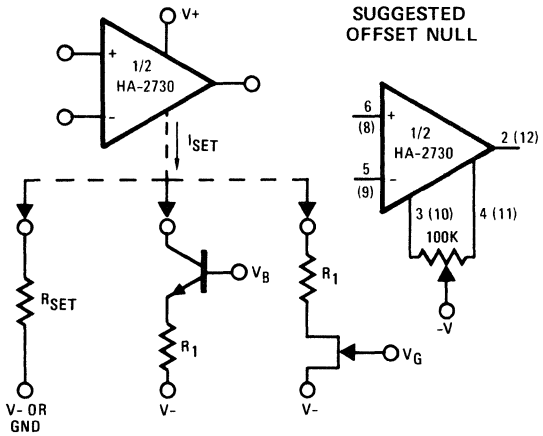
PHASE MARGIN vs. SET CURRENT



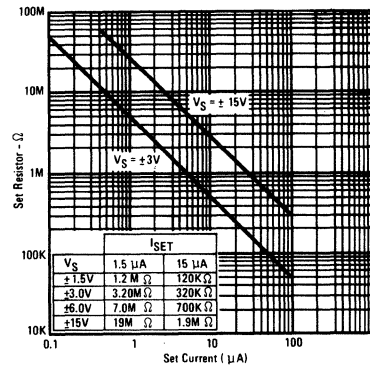
CHANNEL SEPARATION vs. FREQUENCY



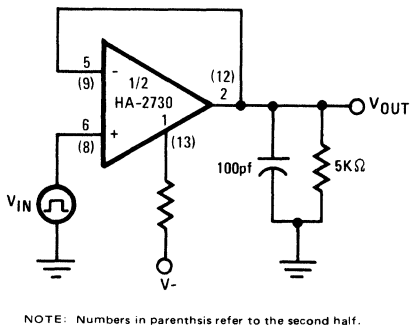
TYPICAL BIASING CIRCUITS



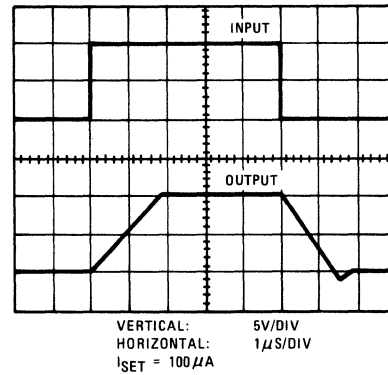
SET CURRENT VS. SET RESISTOR



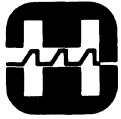
TRANSIENT RESPONSE/SLEW RATE CIRCUIT



SLEWING WAVEFORM



LINEAR



HARRIS
SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-2820/2825

Phase Locked Loop

FEATURES

- FREQUENCY RANGE 0.01 Hz TO 3 MHz
- INDEPENDENT PHASE DETECTOR AND OSCILLATOR FOR VERSATILITY
- TWO ISOLATED PHASE DETECTOR OUTPUTS
- DTL/TTL COMPATIBLE OSCILLATOR OUTPUT
- OSCILLATOR STABILITY: 100ppm/°C, .01%/VOLT

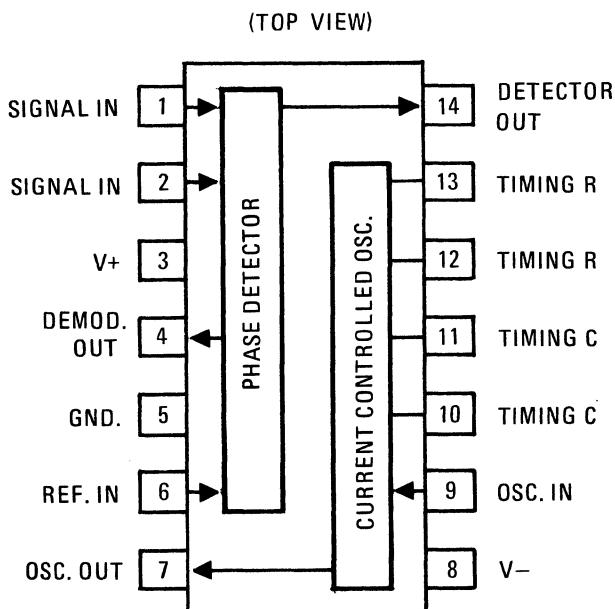
DESCRIPTION

The HA-2820/2825 Phase Locked Loop is useful for many operations in the frequency domain in the sub-audio to low R.F. bands. It features a number of functional and parametric improvements over other similar monolithic circuits.

A major feature is a high impedance current source phase detector output with provisions for external connection to the oscillator input which is a low impedance current sink. This allows connection of complex passive or active filters, amplifiers, sweep circuits, etc. within the loop. Also, the two phase detector outputs are isolated from one another so that different filter functions can be connected at the two outputs without interaction. The capability of independently adjusting loop bandwidth and demodulated output bandwidth allows phase modulation detectors to be constructed.

Applications include modulators and demodulators for F.M., phase modulation, and F.S.K.; frequency multiplication; data synchronization; tracking filters; and speed controls.

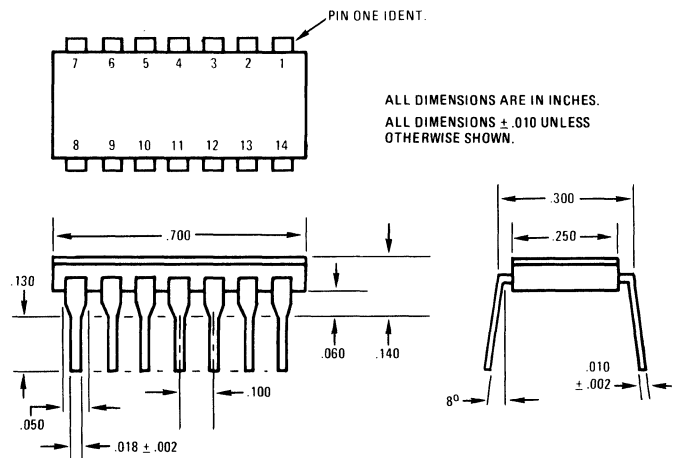
FUNCTIONAL DIAGRAM



PACKAGE

CODE 1S

14 LEAD BRAZED D.I.P.



LINEAR

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	27.0V	Power Dissipation	300mW (Note 3)
Input Voltage	2 VRMS	Operating Temperature	HA-2820 -55°C > T _A > +125°C
			HA-2825 0°C > T _A > +75°C
Output Current, Pin 7	10mA	Storage Temperature	-65°C > T _A > +150°C

ELECTRICAL CHARACTERISTICS

V+ = +6.0V
 V- = -6.0V
 Pin 5 = Ground

V_{IN} = 100mV RMS
 F₀ ≈ 50kHz
 See Test Circuit, Page 3

Unless otherwise specified

PARAMETER	TEMP.	HA-2820 -55°C to +125°C LIMITS			HA-2825 0°C to +75°C LIMITS			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
PHASE DETECTOR								
Input Impedance, Pins 1 - 2	+25°C		100K		100K			Ω
Input Voltage Range, Pins 1 - 2 (Note 1)	Full	10	5		10	5		mV RMS
Output Impedance, Pins 4 & 14	+25°C		10		10			MΩ
Output Offset Current, Pins 4 & 14	+25°C		10	15	10	15		μA
Output Offset Current, Pins 4 & 14	Full			20		20		μA
Conversion Gain, Pins 4 & 14	+25°C		50		50			μA/Radian
CURRENT CONTROLLED OSCILLATOR								
Maximum Frequency	Full	3	5		3	5		MHz
Frequency Drift	Full		100			100		ppm/°C
Frequency Change with Supply Voltage (Note 4)	Full		.01			.01		%/V
Input Resistance, Pin 9	+25°C		500			500		Ω
Input Open Circuit Voltage, Pin 9	+25°C		-3.5			-3.5		V
Conversion Gain	+25°C		1.0			1.0		% Δf/μA
Output Voltage, High	+25°C	+1.9			+1.9			V
Output Voltage, Low	+25°C			+0.4			+0.4	V
Output Rise Time	+25°C		100			100		ns
Output Fall Time	+25°C		125			125		ns
CLOSED LOOP CHARACTERISTICS								
Loop Gain	+25°C		50			50		% Δf/Radian
Tracking Range	+25°C		50			50		%Δf
Demod. Output Swing, Pin 4	+25°C		±700			±700		mV
Frequency Drift	Full		100			100		ppm/°C
POWER SUPPLY CHARACTERISTICS								
Supply Current, V+	Full		3	5		3	5	mA
Supply Current, V-	Full		7	10		7	10	mA
Supply Voltage Range (Notes 2, 3)	Full	±6		±12	±6		±12	V

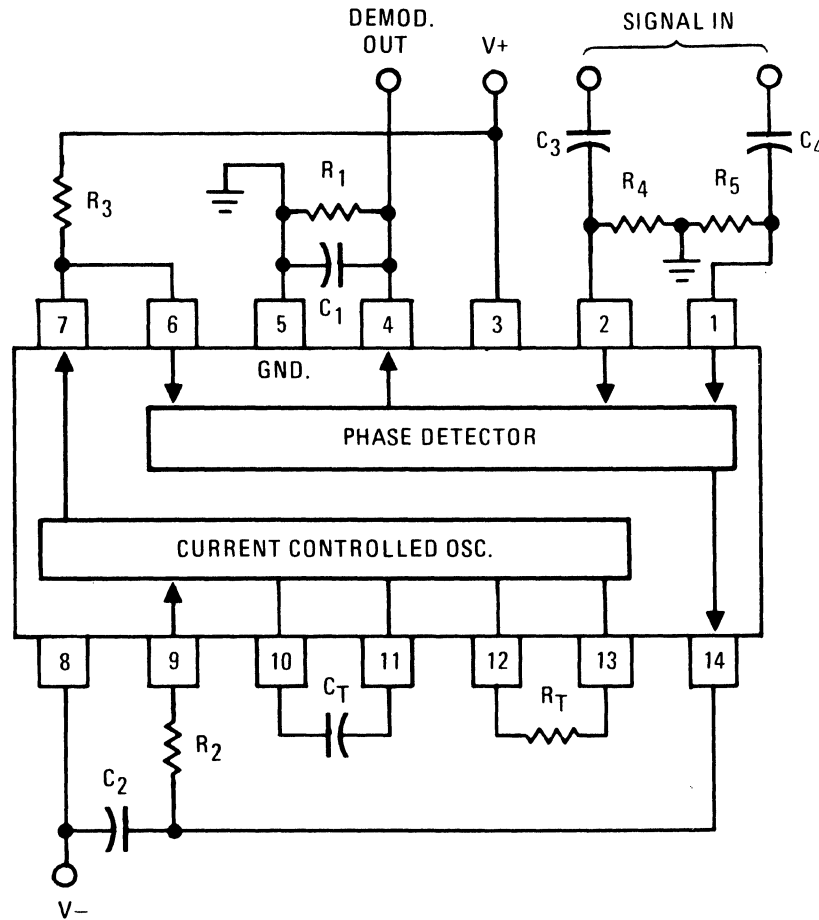
NOTES 1. For ± 10% tracking range.

2. +5.0V, -7.0V may be used alternatively.

3. Derate power dissipation by 6.6mW/°C above +105°C ambient temperature.

4. ΔV_S = ± 2V

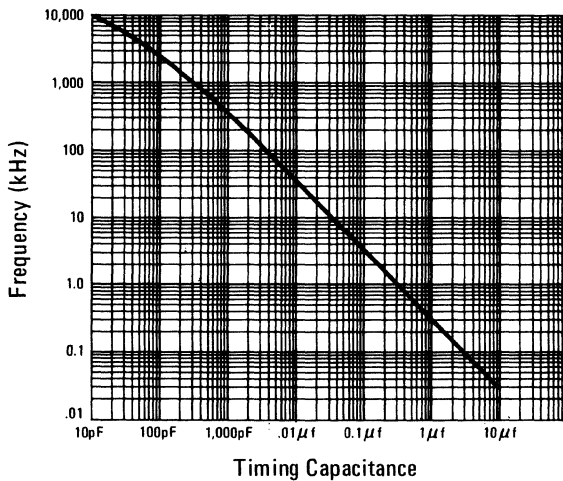
TEST CIRCUIT



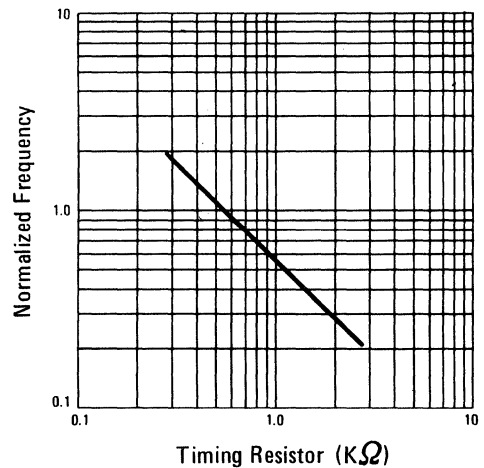
Unless otherwise specified: $V+ = +6.0V$; $V- = -6.0V$; $R_1 = R_3 = 10K\Omega$; $R_2 = 1K\Omega$; $R_4 = R_5 = 300\Omega$; $R_T = 540\Omega$; $C_1 = .015\mu f$; $C_2 = C_3 = C_4 = 0.1\mu f$; $C_T = 0.01\mu f$ ($f_0 \approx 50kHz$); $V_{IN} = 100mV$ RMS; $T_A = +25^\circ C$

PERFORMANCE CURVES

CENTER FREQUENCY, f_0 vs. TIMING CAPACITOR, C_T ($R_T = 540\Omega$)

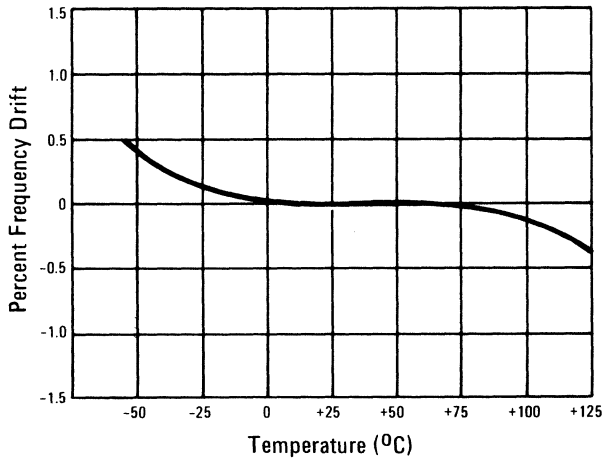


CENTER FREQUENCY, f_0 vs. TIMING RESISTOR, R_T ($C_T = .01\mu f$)

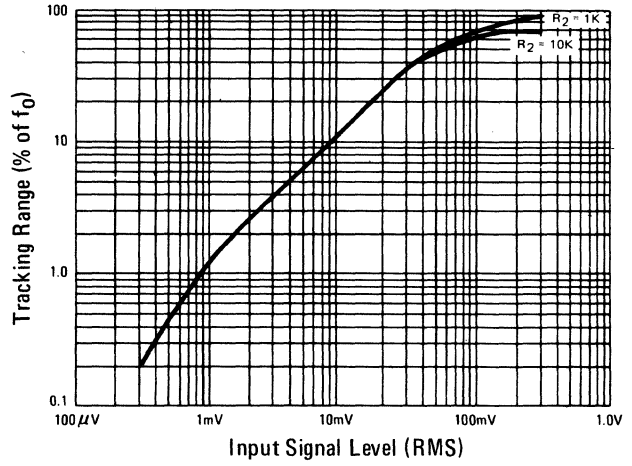


PERFORMANCE CURVES (continued)

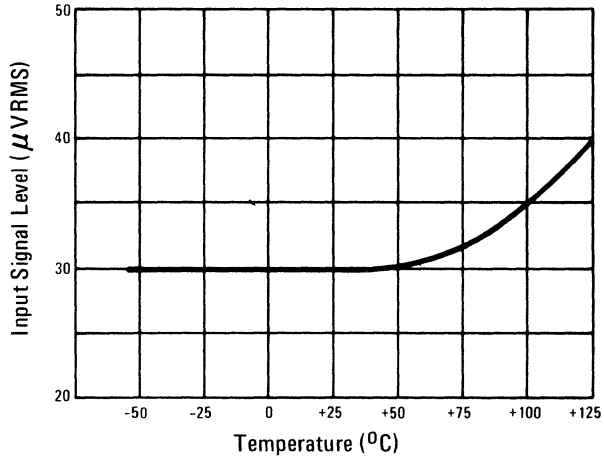
CENTER FREQUENCY DRIFT vs. TEMPERATURE



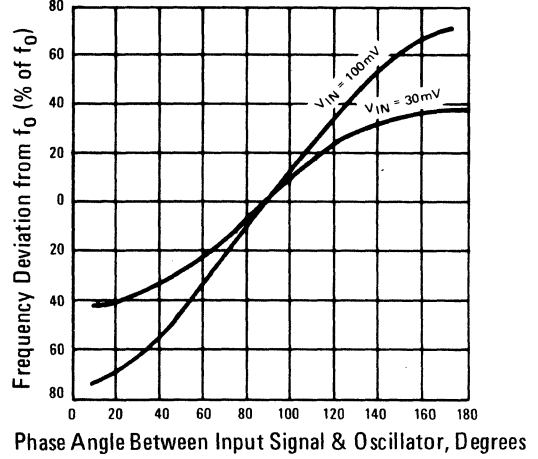
TRACKING RANGE vs. INPUT SIGNAL LEVEL



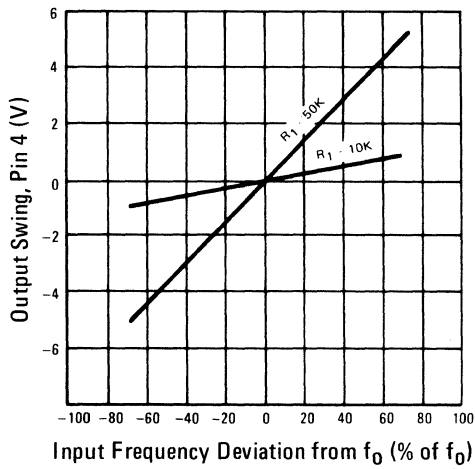
MINIMUM SIGNAL TO MAINTAIN LOCK



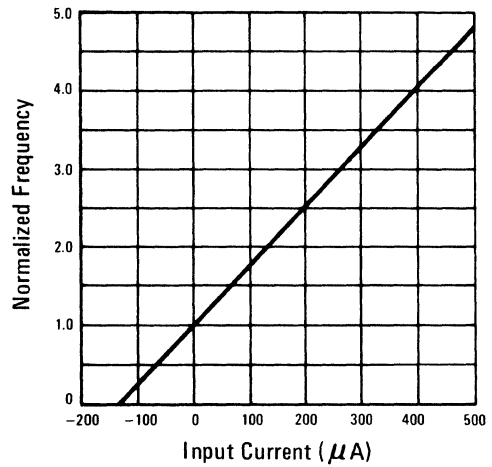
LOOP GAIN CHARACTERISTIC



DEMODULATED OUTPUT SWING



OSCILLATOR FREQUENCY vs. INPUT CURRENT, PIN 9 ($f_0 = 50kHz$)



LINEAR



HARRIS
SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-2900/2904/2905

Chopper Stabilized Operational Amplifier

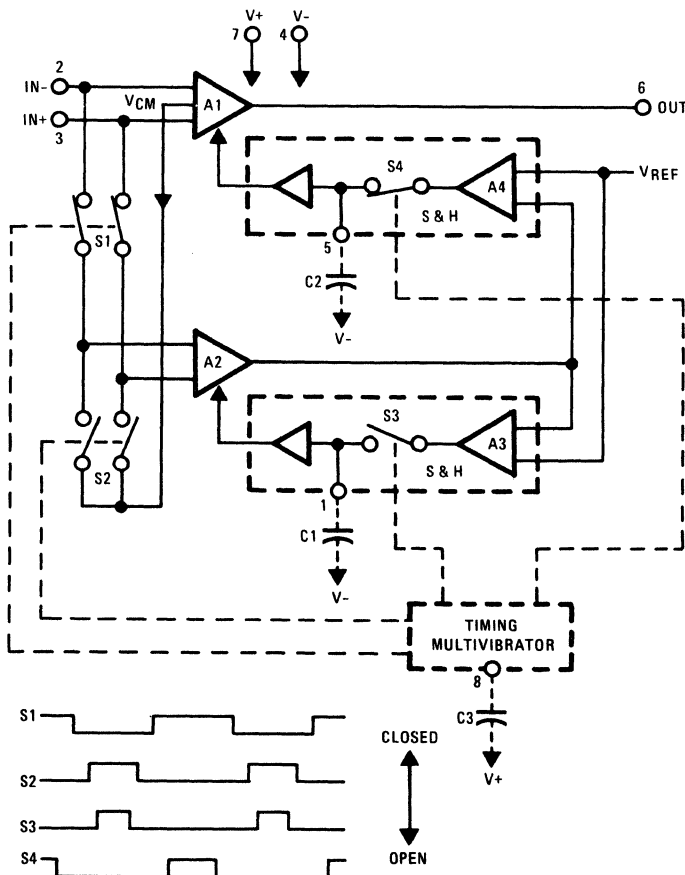
FEATURES

- OFFSET VOLTAGE DRIFT: $0.2 \mu\text{V}/^\circ\text{C}$
- OFFSET CURRENT DRIFT: $1 \text{pA}/^\circ\text{C}$
- OPEN LOOP GAIN: 5×10^8
- BANDWIDTH: 3MHz
- SLEW RATE: $2.5 \text{V}/\mu\text{s}$
- TRUE DIFFERENTIAL INPUTS

DESCRIPTION

The HA-2900/2904/2905 is the first monolithic chopper stabilized operational amplifier. It features superior offset drift characteristics, extremely low input currents, and excellent AC performance. Its inputs are symmetrical and differential, meaning that the device may be operated in any op amp feedback configuration; inverting, non-inverting, or balanced. Applications include high gain DC instrumentation, precision integrators, and as a substitute for other op amps wherever much lower errors without external adjustments are required. The device is packaged in a hermetic can with standard pin out, and requires only three external capacitors for operation.

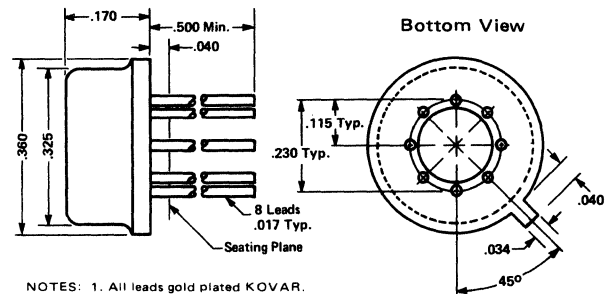
FUNCTIONAL DIAGRAM



PACKAGE

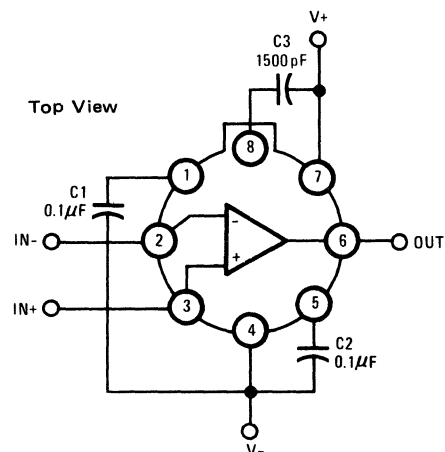
CODE 2A T0-99

ALL DIMENSIONS ARE IN INCHES
ALL DIMENSIONS $\pm .010$ UNLESS
OTHERWISE SHOWN.



NOTES: 1. All leads gold plated KOVAR.
2. All dimensions in inches.

PIN OUT AND SUGGESTED HOOKUP



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	42.0V	Operating Temperature Range	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (HA-2900)
Differential Input Voltage (Note 1)	$\pm 15\text{V}$		$-25^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (HA-2904)
Output Current/Full Short Circuit Protection		Storage Temperature Range	$0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$ (HA-2905)
Internal Power Dissipation	300mW*		$-65^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$

*Derate by 6.6mW/°C above +105°C

ELECTRICAL CHARACTERISTICS

Test Conditions: C1 = C2 = 0.1μF, C3 = 1500pF, V_{Supply} = ±15.0V unless otherwise specified.

PARAMETER	TEMP.	HA-2900 -55°C to +125°C			HA-2904 -25°C to +85°C			HA-2905 0°C to +75°C			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
INPUT CHARACTERISTICS											
*Offset Voltage	+25°C Full		20	60		20	50		20	80	μV μV
Offset Voltage Average Drift	Full		0.3	0.6		0.2	0.4		0.2		μV/°C
*Bias Current	+25°C Full		150	1,000		150	1,000		150	1,000	pA pA
*Offset Current	+25°C Full		50	500		50	500		50	500	pA pA
Offset Current Average Drift	Full		1	4		1	3		1		pA/°C
Input Resistance	+25°C		100			100			100		MΩ
Input Capacitance	+25°C		10			10			10		pF
Common Mode Range	Full		±10			±10			±10		V
TRANSFER CHARACTERISTICS											
*Large Signal Voltage Gain (Note 2)	+25°C Full	10 ⁶	5x10 ⁸		10 ⁷	5x10 ⁸		10 ⁶	5x10 ⁸		V/V V/V
Chopper Frequency	+25°C		750			750			750		Hz
*Common Mode Rejection Ratio (Note 3)	Full	120	160		130	160		120	160		dB
Gain Bandwidth Product (Note 4)	+25°C		3			3			3		MHz
OUTPUT CHARACTERISTICS											
*Output Voltage Swing (Note 2)	Full	±10	±12		±10	±12		±10	±12		V
*Output Current	+25°C	±10			±10			±7			mA
Output Resistance	Full		200			200			200		Ω
Full Power Bandwidth (Note 5)	+25°C		40			40			40		kHz
TRANSIENT RESPONSE (NOTES 2, 8, and 9)											
Rise Time (Note 6)	+25°C		200			200			200		ns
Overshoot (Note 6)	+25°C		20			20			20		%
Slew Rate (Note 5)	+25°C		2.5			2.5			2.5		V/μs
POWER SUPPLY CHARACTERISTICS											
*Supply Current	+25°C		3.5	5.0		3.5	5.0		3.5	5.0	mA
*Supply Voltage Range	Full	±12		±20	±10		±20	±12		±20	V
*Power Supply Rejection Ratio (Note 7)	Full	120	160		130	160		120	160		dB

- NOTES: 1. Input terminals should be protected against static discharge during handling and installation. Input voltage should never exceed supply voltages.
 2. R_L = 2K
 3. V_{CM} = ±5.0V
 4. A_V = 10

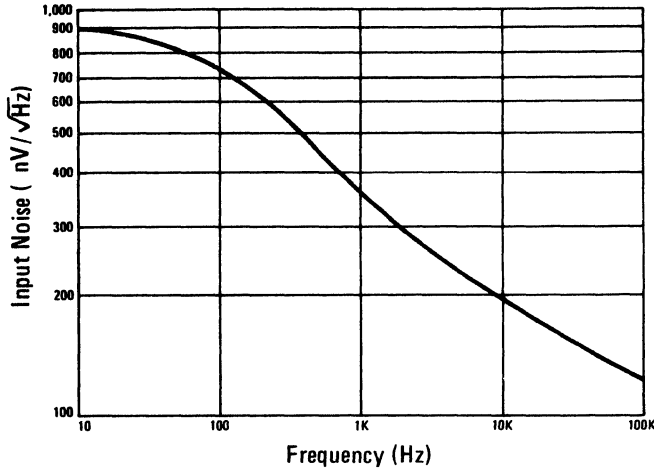
5. V_O = ±10V
 6. V_O = ±200mV
 7. ΔV_S = ±5V
 8. C_L = 50pF
 9. A_V = +1 See transient response test circuits and waveforms, page 4.

*100% Tested For DASH 8

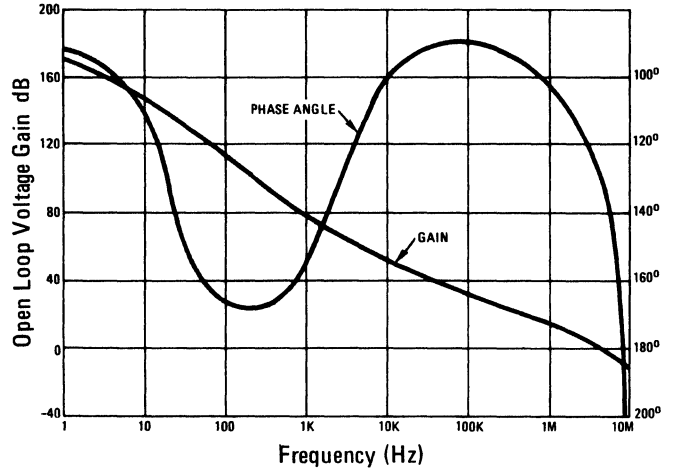
PERFORMANCE CURVES

$V_+ = V_- = 15\text{VDC}$, $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE STATED

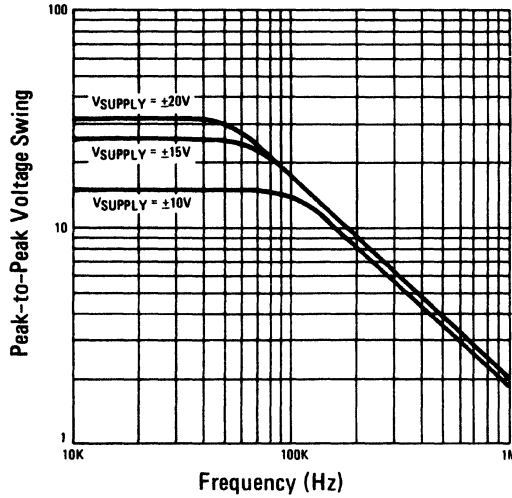
INPUT VOLTAGE NOISE



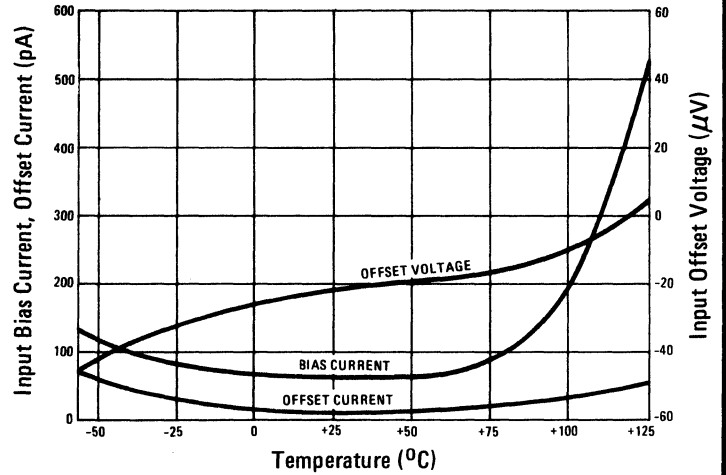
OPEN LOOP FREQUENCY AND PHASE RESPONSE



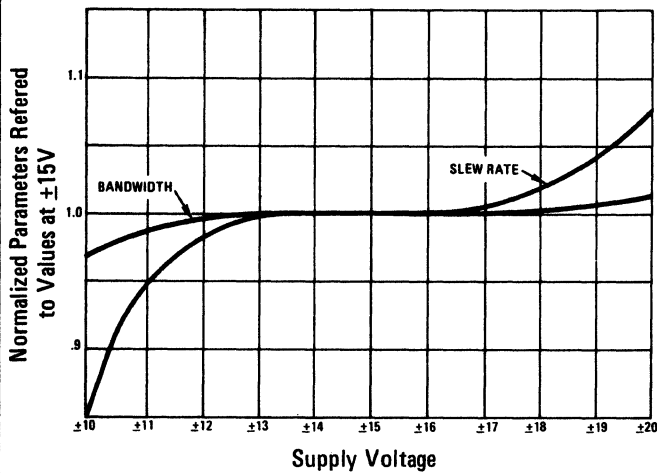
OUTPUT VOLTAGE SWING vs. FREQUENCY



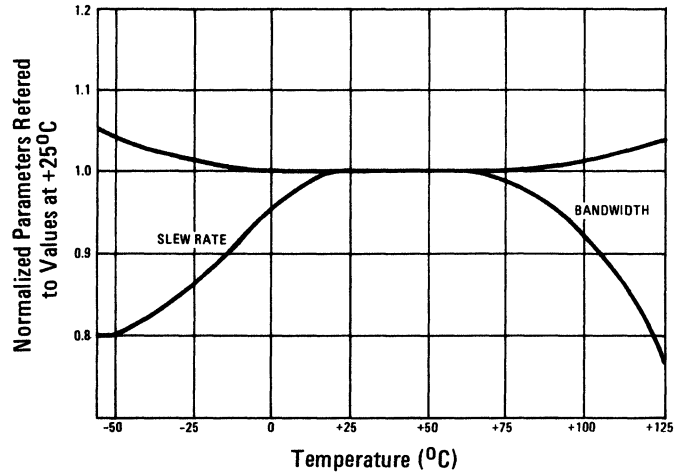
TYPICAL INPUT CHARACTERISTICS vs. TEMPERATURE



NORMALIZED A.C. PARAMETERS vs. SUPPLY VOLTAGE

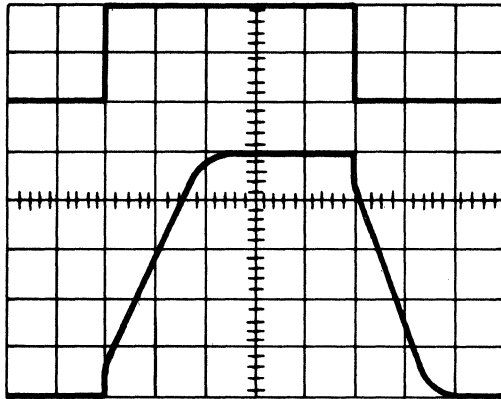


NORMALIZED A.C. PARAMETERS vs. TEMPERATURE



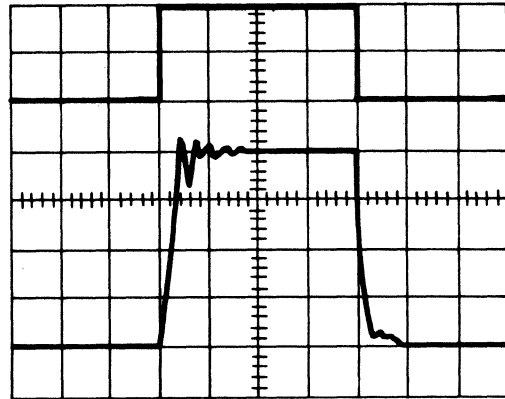
PERFORMANCE CURVES (continued)

VOLTAGE FOLLOWER
SLEWING WAVEFORM



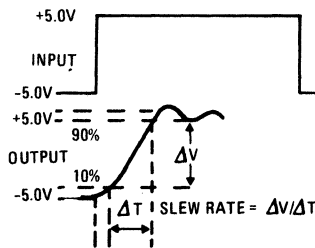
Upper Trace: Input: 5V/Div.
Lower Trace: Output; 2V/Div.
Horizontal: 2 μ S/Div.

VOLTAGE FOLLOWER
TRANSIENT RESPONSE WAVEFORM

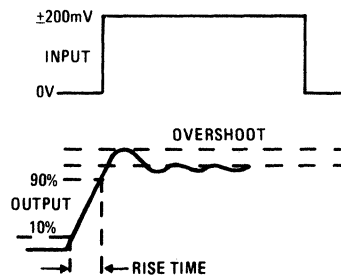


Upper Trace: Input; 100mV/Div.
Lower Trace: Output; 50mV/Div.
Horizontal: 500ns/Div.

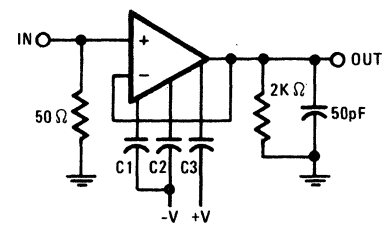
SLEW RATE



TRANSIENT RESPONSE



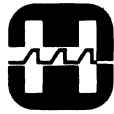
SLEW RATE AND
TRANSIENT RESPONSE



NOTE: Measured on both positive and negative transitions.

APPLICATION TIPS

- (1) Device inputs should be protected against exceeding either supply voltage from static discharge or inadvertent connection, particularly when wired directly to a connector or instrument panel.
- (2) External capacitors C1, C2, and C3 should have good temperature stability, low leakage, and low dielectric absorption. Polystyrene (below +85°C), teflon types or polycarbonate are recommended. C3 could also be silver mica.
- (3) Particular care must be exercised in system layout and material and component selection to realize the full performance potential of the HA-2900/2904/2905. External sources of drift error may include the thermocouple and electrochemical EMF's generated at junctions of dissimilar metals, leakage across insulating materials, static charges created by moving air, and improper grounding and shielding practices.
- (4) Chopper noise is present chiefly as a common mode input current signal, and may be minimized by matching the impedances at the two inputs. Random noise may be reduced at the expense of bandwidth using active or passive filtering.
- (5) Input frequencies near the chopper frequency (750Hz) or its harmonics may result in small components of difference frequency in the output. This effect should be checked in the individual application, and if objectionable, a low pass filter may be added in series with the input.
- (6) When operating at closed loop gains between 70 dB and 140 dB, compensation networks may be required, because of open loop phase shift in this gain region. In most cases, a capacitor placed in parallel with the feedback resistor to yield a gain-bandwidth product < 2 MHz will be sufficient.



HARRIS
SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HD-0165

Keyboard Encoder

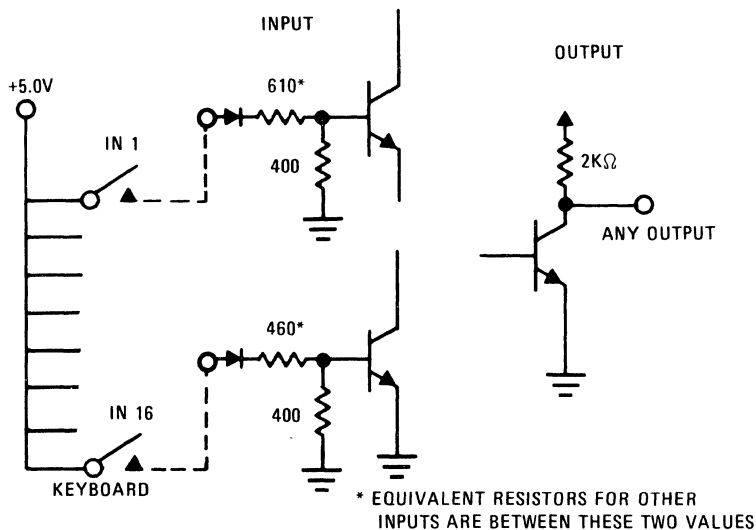
FEATURES

- STROBE OUTPUT
- KEY ROLLOVER OUTPUT
- EXPANDABLE: 2 PACKAGES REQUIRED FOR FULL TELETYPEWRITER, EIGHT-BIT ENCODING
- SINGLE +5.0V SUPPLY REQUIRED, DTL/TTL OUTPUTS
- MONOLITHIC RELIABILITY

GENERAL DESCRIPTION

The HD-0165 Keyboard Encoder is a 16 line to four-bit parallel encoder intended for use with manual data entry devices such as calculator or typewriter keyboards. In addition to the encoding function, there is a Strobe output and a Key Rollover output which energizes whenever two or more inputs are energized simultaneously. Any four-bit code can be implemented by proper wiring of the input lines. Inputs are normally wired through the key switches to the +5.0V power supply. Full typewriter keyboard encoding up to eight bits can be accomplished with two Encoder circuits by the use of double pole key switches or single pole switches with two isolation diodes per key. Outputs will interface with all popular DTL and TTL logic families. The circuit is packaged in a hermetic 24-pin dual in-line package and operates over the temperature range of 0°C to +75°C.

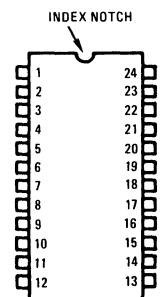
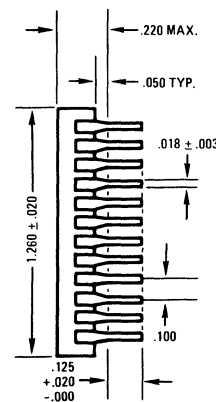
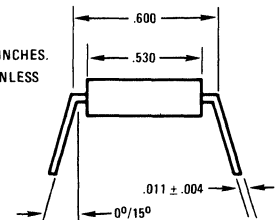
EQUIVALENT CIRCUITS



PACKAGE

CODE 1J 24 LEAD CERAMIC D. I. P.

ALL DIMENSIONS ARE IN INCHES.
ALL DIMENSIONS $\pm .010$ UNLESS OTHERWISE SHOWN.



LINEAR

APPLICATIONS

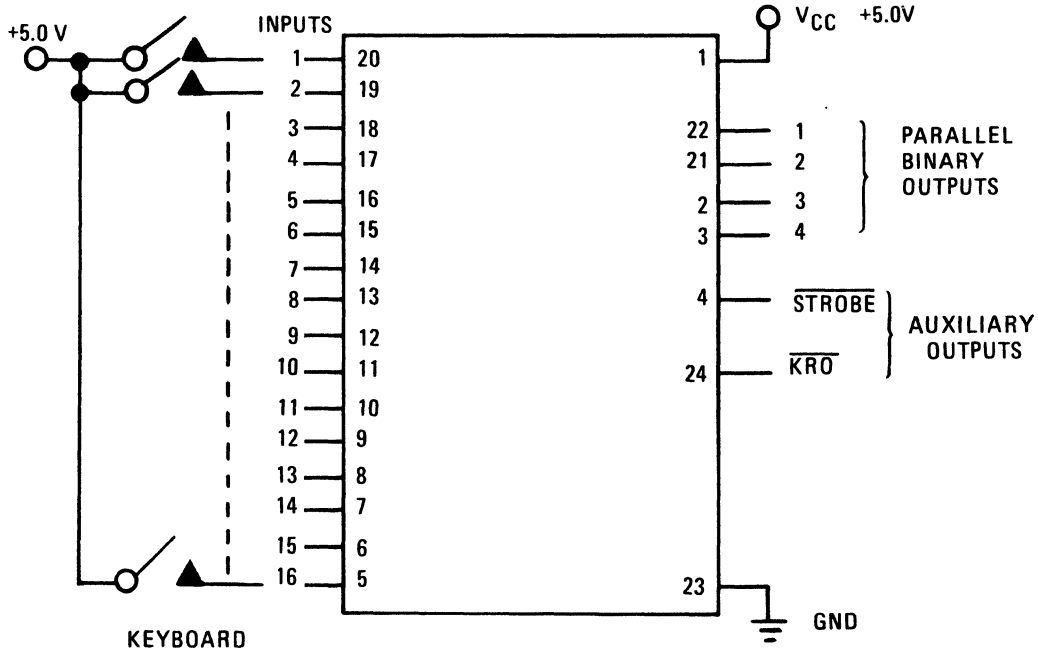


Figure 1. GENERAL CONFIGURATION FOR ENCODING TWO TO SIXTEEN KEYS

The Truth Table is used to determine wiring from the key switches to Encoder inputs to produce desired output codes.

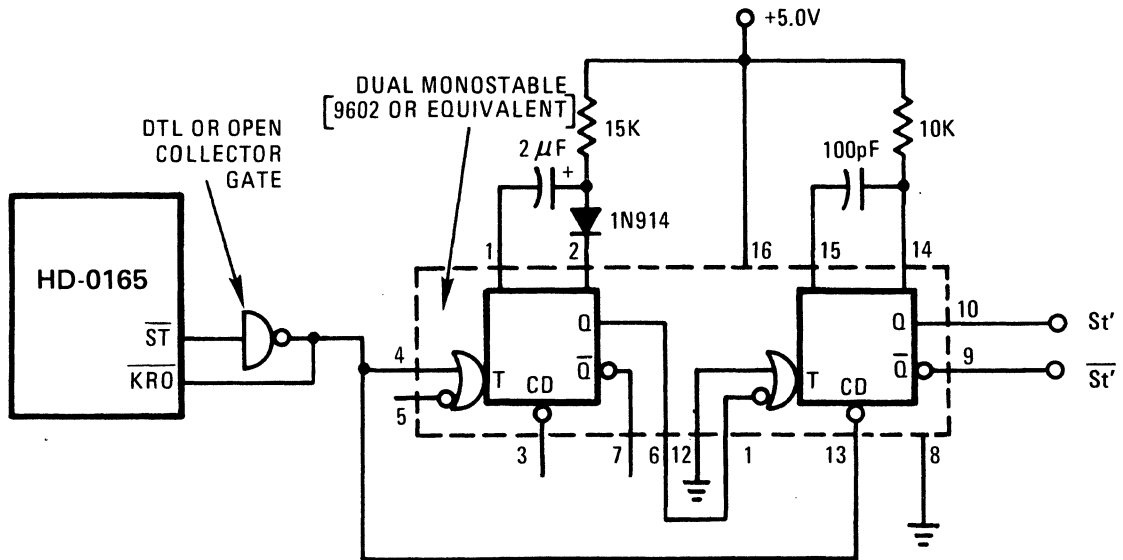


Figure 2. SWITCH BOUNCE ELIMINATION

This circuit generates a delayed Strobe pulse (St'). Delay time is determined by first monostable and should be about 10ms. Pulse width is determined by second monostable and should be set according to system requirements. Effect of switch bounce or arcing on make or break is positively eliminated and proper encoding will take place under two key rollover conditions.

APPLICATIONS (continued)

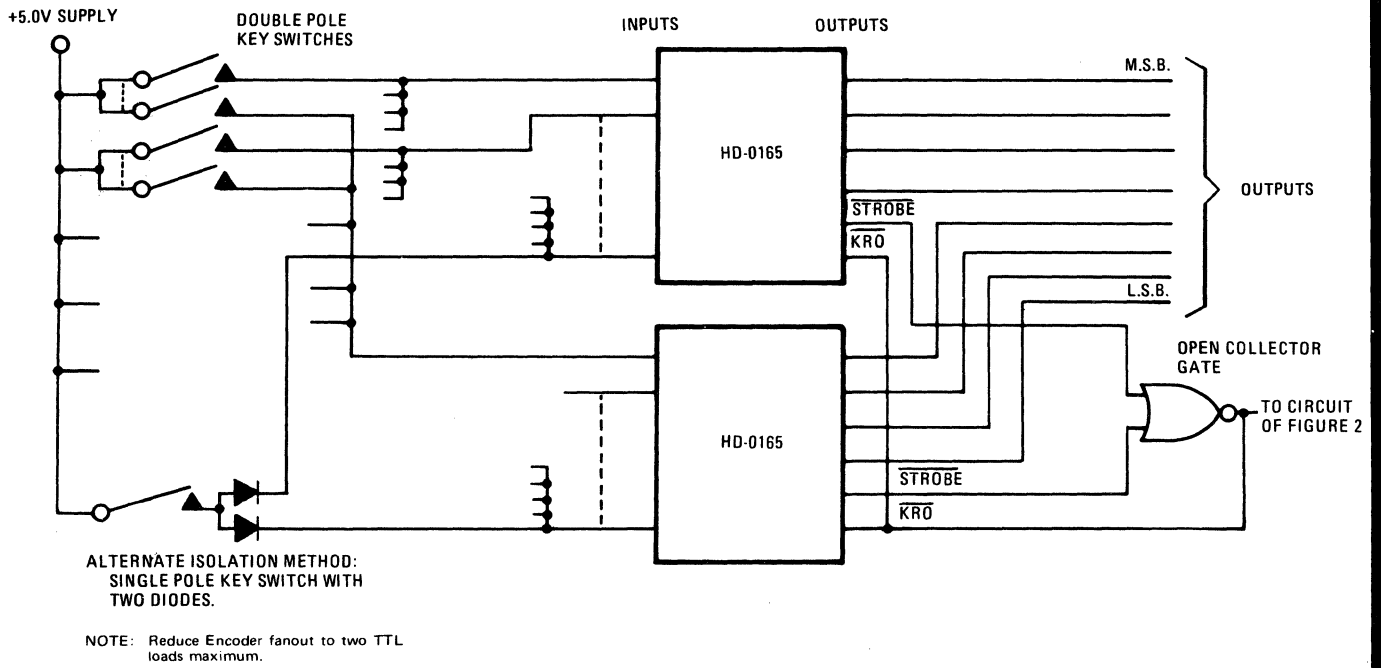


Figure 3. ENCODING UP TO 256 KEYS

Use upper Encoder to produce the four most significant output bits; the lower to produce the least significant bits. Use Truth Table and required output codes to determine wiring from each key to the two Encoders.

SHIFT and CONTROL functions can be implemented by logic gates in series with the output lines.



HARRIS
SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HD-245/545 Triple Line Transmitter

HD-246/546/249/549 Triple Line Receivers

HD-248/548 Triple Party Line Receiver

FEATURES:

- CURRENT MODE OPERATION
- HIGH SPEED: 15MHz WITH 50FT. CABLE;
2MHz WITH 1,000FT. CABLE
- HIGH NOISE IMMUNITY
- LOW EMI GENERATION
- LOW POWER DISSIPATION
- HIGH COMMON MODE REJECTION
- TRANSMITTER AND RECEIVER PARTY LINE CAPABILITY
- TOLERATES -2.0V TO +20.0V GROUND DIFFERENTIAL
(Transmitter with respect to receiver)
- TRANSMITTER INPUT/RECEIVER OUTPUT TTL/DTL
COMPATIBLE

GENERAL DESCRIPTION

Each transmitter-receiver combination provides a digital interface between systems linked by 100Ω twisted pair, shielded cable. Each device contains three circuits fabricated within a single monolithic chip. Data rates greater than 15MHz are possible depending on transmission line loss characteristics and length.

The transmitter employs constant current switching which provides high noise immunity along with high speeds, low power dissipation, low EMI generation and the ability to drive high capacitance loads. In addition, the transmitters can be turned "off", allowing several transmitters to time-share a single line.

Receiver input/output differences are shown in the following table:

	INPUT	OUTPUT
HD-246 / 546	100 Ω	OPEN COLLECTOR
HD-248 / 548	HI-Z	6K PULL-UP RES.
HD-249 / 549	100 Ω	6K PULL-UP RES.

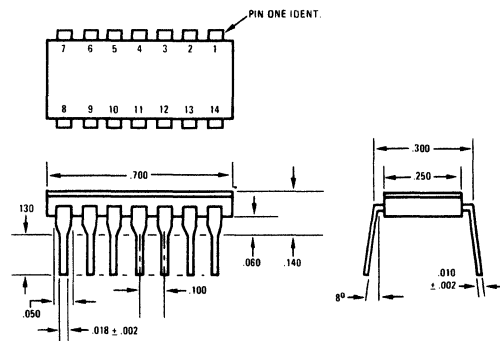
The internal 100 Ω cable termination consists of 50 Ω from each input to ground.

HD-248/548 "party line" receivers have a high-Z input such that as many as ten of these receivers can be used on a single transmission line.

Each transmitter input and receiver output can be connected to TTL and DTL systems. When used with shielded transmission line, the transmitter-receiver system has very high immunity to capacitive and magnetic noise coupling from adjacent conductors. The system can tolerate ground differentials of -2.0 V to +20.0V (transmitter with respect to receiver).

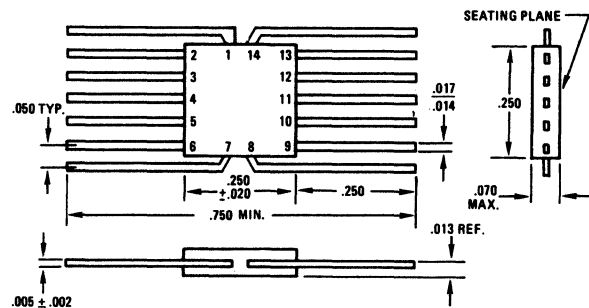
PACKAGES

CODE 1S 14 LEAD BRAZED C.I.P.



CODE 9V

TO-86 (METAL BOTTOM)



ALL DIMENSIONS ARE IN INCHES.
ALL DIMENSIONS ± .010 UNLESS
OTHERWISE SHOWN.

LINEAR

SPECIFICATIONS HD-245/545 TRANSMITTERS

ABSOLUTE MAXIMUM RATINGS

Input Voltage Range: -0.5V to +10V
 Output Voltage Range: -30V to +0.5V with respect to V_{CC}

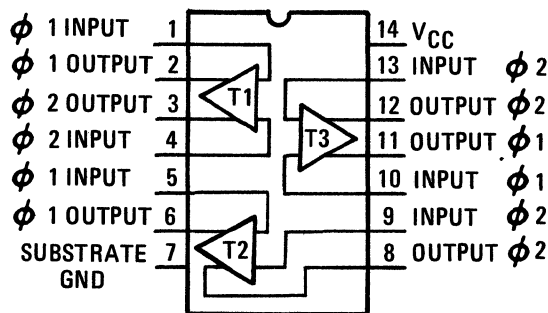
V_{CC} Range: -0.5V to +10V
 Storage Temperature Range: -65°C to +150°C

ELECTRICAL CHARACTERISTICS

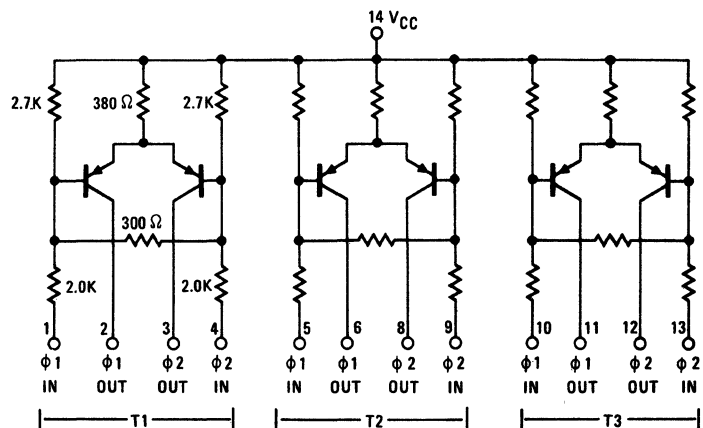
PARAMETER	SYMBOL	TEMP.	HD-245 -55°C to +125°C			HD-545 0°C to +75°C			UNITS	TEST CONDITION	
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		V_{CC}	NOTES
DC	INPUT LOW CURRENT	25°C Full		-1.5	-2.2 -2.5		-1.5	-2.3 -2.4	mA	5.5	1
	"ON" OUTPUT CURRENT	25°C Full	-2.3			-1.9			mA	4.5	1
		Full	-2.0			-1.8			mA	4.5	1
		Full	-1.6			-1.5			mA	4.5	2
		25°C Full		-4.1	-5.4 -5.6		-4.1	-6.3 -6.7	mA	5.5	1
	"ON" OUTPUT CURRENT UNBALANCE	25°C Full		0.1	0.25 0.3		0.1	0.25 0.3	mA	5.5	3
"OFF" OUTPUT CURRENT	I_{OUT} "OFF"	25°C Full		-30	-100 -100		-30	-100 -100	μA	4.5	1
OUTPUT BREAKDOWN	BV_{CER}	25°C	-30	-50		-30	-50	V	GND	4	
POWER SUPPLY CURRENT-TOTAL		25°C		15	18.6		15	24	mA	5.0	5
		25°C			0.6			0.6			6
AC	PROPAGATION DELAY	t_{PLH}	25°C Full	3	10 14		3	10 14	ns	5.0	
	TEST CIRCUIT 1, PAGE 4	t_{PHL}	25°C Full	3.2	10 14		3.2	10 14	ns	5.0	

- NOTES: 1. One input at Gnd. one input open, each output at Gnd.
 2. One input at 0.45V, one input open, each output at Gnd.
 3. Difference between $\phi 1$ and $\phi 2$ "ON" output data current.
 4. Each input at Gnd., one output at Gnd.,
 $I_{Limit} \geq 100 \mu A$ on output tested with -30V applied.
 5. One input of each transmitter at Gnd and the other input open. All six output lines at Gnd.
 6. All six input lines open, all six output lines at Gnd.

BLOCK DIAGRAM



SCHEMATIC



SPECIFICATIONS HD-246/546; HD-248/548; HD-249/549 RECEIVERS

ABSOLUTE MAXIMUM RATINGS

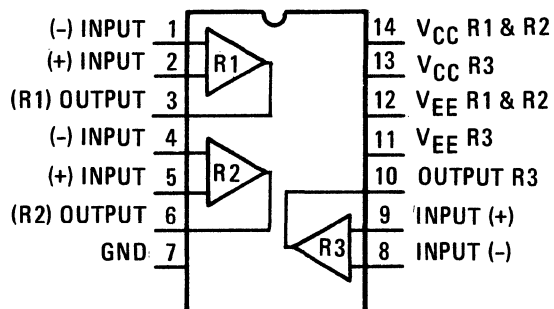
Input Voltage Range	-1.0V to +1.0V	Input Current	±25mA
Output Voltage Range	-0.5V to +6.0V	Output Current	+50mA
VCC Range	-0.5V to +8.0V	Storage Temperature	-65°C to +150°C
VEE Range	-8.0V to +0.5V		

ELECTRICAL CHARACTERISTICS

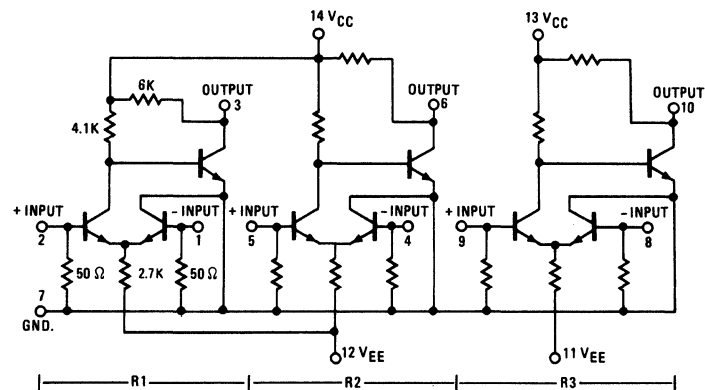
PARAMETER	SYM.	TEMP.	HD-246 / 248 / 249 -55°C to +125°C			HD-546 / 548 / 549 0°C to +75°C			UNITS	TEST CONDITIONS V _{EE} = -5V	
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		V _{CC}	NOTES
INPUT RESISTANCE (HD-246/546 & HD-249/549)	R _{IN}	+25°C Full	40 39	47	61 68	35 33	47	65 70	Ohms		
PULL-UP RESISTOR (HD-248/548 & HD-249/549)		+25°C Full	4.2 4.1	6	7.8 8.6	4.0 3.9	6	8.1 8.6	K Ohms		
OUTPUT VOLTAGE (HIGH)	V _{OH}	+25°C Full	2.6 2.5			2.6 2.5			V	4.5	Note 1 I _{OH} = -120μA Ext. 6K Res. For HD-246/546
OUTPUT VOLTAGE (LOW)	V _{OL}	+25°C Full			0.45 0.45			0.45 0.45	V	4.5	Note 2 I _{OL} = 9.6mA 10mA For HD-246/546
OUTPUT VOLTAGE (LOW) (INPUT SHORTCIRCUIT)	V _{OLSC}	+25°C		0.4			0.4		V	5.0	Note 3 I _{OL} = 3.2mA
POWER SUPPLY CURRENT (TOTAL)	HD-246 / 546	I _{CC}	+25°C	3.3	4.8	3.3	5.7	5.0	5.0	Note 4	
		I _{EE}	+25°C	5.1	6.0	5.1	6.3	5.0	Note 5		
	HD-248 / 548 & HD-249 / 549	I _{CC}	+25°C	3.9	6.6	3.9	7.5	5.0	Note 4		
		I _{EE}	+25°C	5.1	6.0	5.1	6.3	5.0	Note 5		
PROPAGATION DELAY	t _{PLH}	+25°C Full		18	30	18	30	ns	5.0		
TEST CIRCUIT 2 PAGE 4	t _{PHL}	+25°C Full		25	30	25	30	ns	5.0		

- NOTES: 1. (+) I_{IN} = 1.5mA; (-) Input = open (For HD-248/548; Ext. 50Ω Res. or 75mV).
 2. (+) Input = open; (-) I_{IN} = 1.5mA. (For HD-248/548; Ext. 50Ω Res. or 75mV).
 3. Both inputs shorted to Gnd; or both inputs open such that 50Ω termination resistors are in the circuit.
 4. (+) Input = open; (-) I_{IN} = 3mA.
 5. (+) I_{IN} = 3mA; (-) Input = open.

BLOCK DIAGRAM



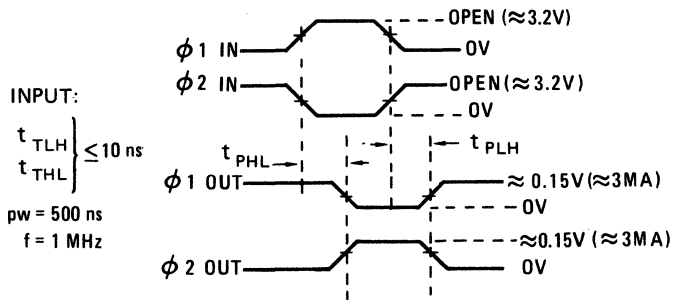
SCHEMATIC



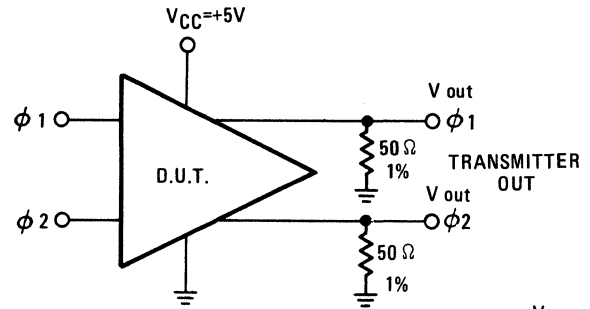
- NOTES:
 1. HD- 249/549 is as shown
 2. HD- 246/546 does not have 6K output pull-up resistors.
 3. HD- 248/548 does not have 50Ω input termination resistors.
 4. Resistor values are nominal

TEST CIRCUITS

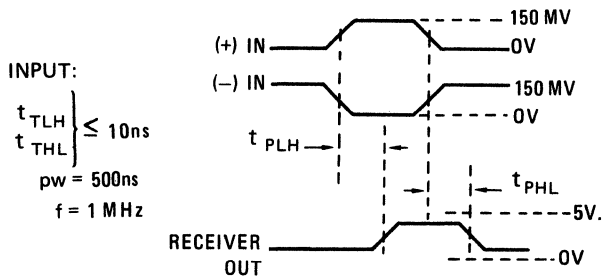
TEST CIRCUIT 1 - TRANSMITTER PROPAGATION DELAY



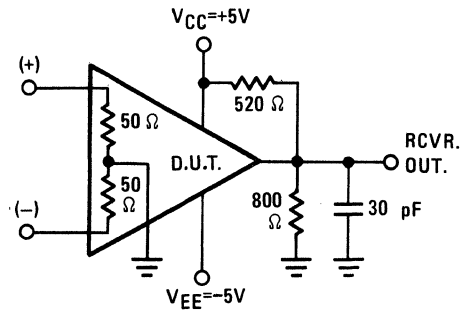
All measurements referenced to 50% V points



TEST CIRCUIT 2 - RECEIVER PROPAGATION DELAY



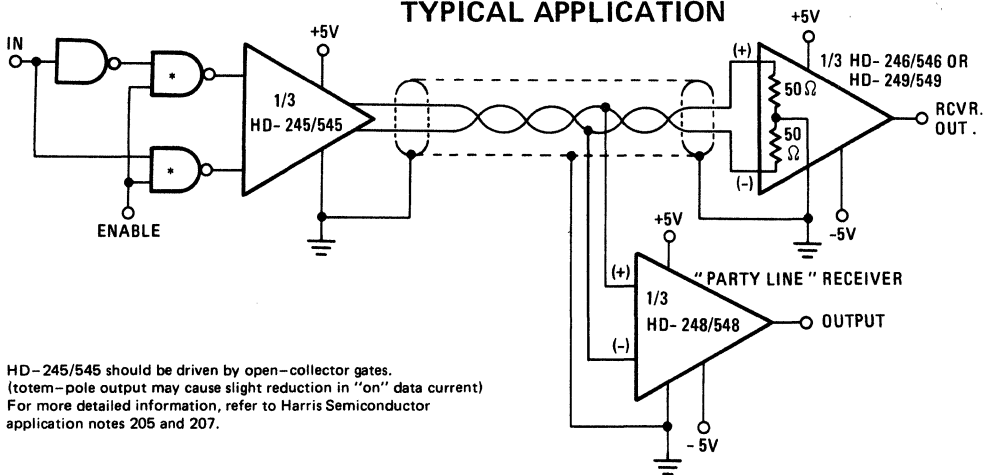
All measurements referenced to 50%V points.



NOTE: External 50Ω resistors needed for HD-248/548.

APPLICATIONS

TYPICAL APPLICATION



* HD-245/545 should be driven by open-collector gates.
 (totem-pole output may cause slight reduction in "on" data current)
 For more detailed information, refer to Harris Semiconductor application notes 205 and 207.



HARRIS
SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HD-1488

Quad Line Driver

FEATURES

- $\pm 6.0V$ OUTPUT LEVELS
- SHORT CIRCUIT PROTECTED
- USEFUL AS LOGIC LEVEL SHIFTER
- MONOLITHIC RELIABILITY

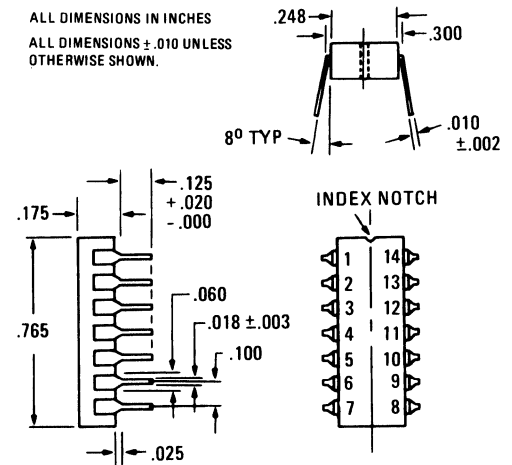
DESCRIPTION

The Harris HD-1488 is a quadruple line driver monolithic integrated circuit meeting the electrical requirements of EIA standard RS-232-C for interface between data terminal equipment and data communication equipment. This standard assures electrical interface compatibility between data equipment made by different manufacturers. The driver circuit is useful in any application requiring transfer of digital signals up to 20K bits per second using common-return signal lines over relatively short distances. The circuit inputs can be driven from any of the popular DTL or TTL logic families. It is available in a 14-pin hermetic dual in-line package for operation from 0°C to +75°C. The companion quad line receiver circuit is the Harris HD-1489.

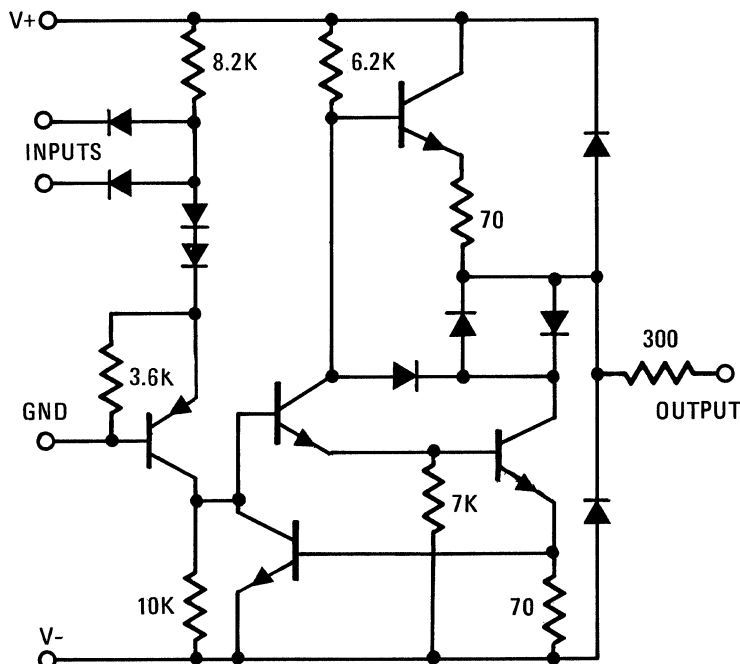
PACKAGE

CODE 1A TO-116 (14 LEAD CERAMIC D.I.P.)

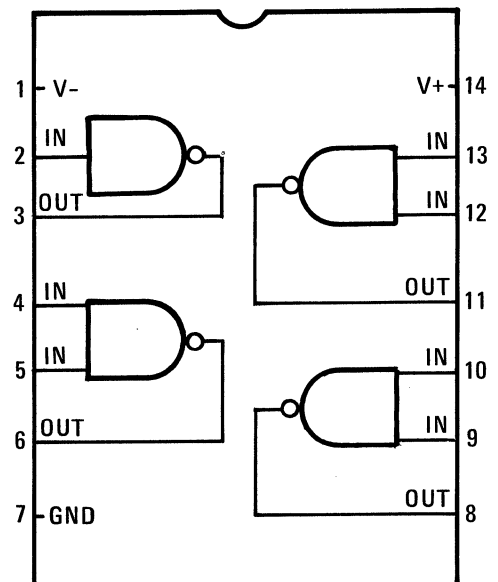
ALL DIMENSIONS IN INCHES
ALL DIMENSIONS $\pm .010$ UNLESS OTHERWISE SHOWN.



SCHEMATIC



CONNECTION DIAGRAM



LINEAR

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

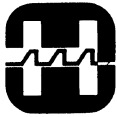
Supply Voltage, V+, V- at +25°C Derate by 35mV/°C	±15.0V	Storage Temperature	-65°C to +150°C
Input Voltage	$V_- \leq V_{IN} \leq 7.0V$	Operating Temperature, T _A	0°C to +75°C
Output Voltage	$V_{OUT} \begin{matrix} \geq V_+ +5V \\ \leq V_- -5V \end{matrix}$	Power Dissipation at +25°C Derate by 6.7mW/°C	1000mW

ELECTRICAL CHARACTERISTICS

Test Conditions: V+ = +9.0V, V- = -9.0V, T_A = 0°C to +75°C unless otherwise specified.

PARAMETER	SYM.	LIMITS			UNITS	TEST CONDITIONS	
		MIN.	TYP.	MAX.			
Input Current	"0"	I _F		1.0	1.3	mA	V _{IN} = 0.0V
	"1"	I _R			10	µA	V _{IN} = +5.0V
Output Voltage	"0"	V _{OL}	-6.0	-7.0		V	V _{IN} = +1.9V, R _L = 3K
	"1"	V _{OH}	+6.0	+7.0			V _{IN} = +0.8V, R _L = 3K
Output Short Circuit Current		I _{SC+}	+6	+10	+12	mA	V _{IN} = 0.0V to +0.8V
		I _{SC-}	-6	-10	-12		V _{IN} = +1.9V to +5.0V
D.C. Output Resistance		R _O	300			Ohms	V+ = V- = 0.0V V _O = ±2.0V
Supply Current		I+		+15	+20	mA	V+ = +9.0V
		I-		-13	-17		V- = -9.0V
		I+		+19	+25	mA	V+ = +12.0V
		I-		-18	-23		V- = -12.0V
Power Dissipation		P _D			333	mW	V+ = +9.0V, V- = -9.0V
		P _D			576		V+ = +12.0V, V- = -12.0V
A.C. Propagation Delay		T _{PD+}		250	300	ns	R _L = 3KΩ
		T _{PD-}		30	120		
	Rise Time (Note 1)	T _r		50	100	ns	C _L = 15pF
Fall Time (Note 1)		T _f		25	75	ns	T _A = +25°C

NOTES: 1. To maintain a maximum rate of voltage change of 30V/µs, the load capacitance, including transmission line, should be at least 330pF.



HARRIS
SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HD-1489

Quad Line Receiver

LINEAR

FEATURES

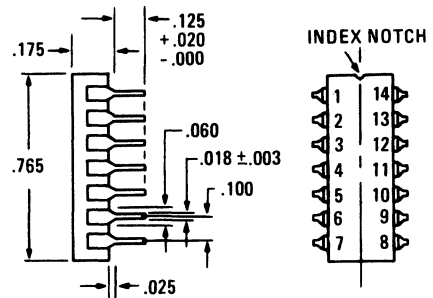
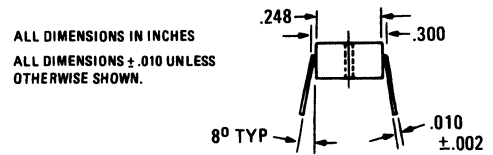
- INPUT LEVEL HYSTERESIS
- INPUTS WITHSTAND $\pm 30.0V$
- PROVISION FOR THRESHOLD ADJUSTMENT OR NOISE FILTERING
- MONOLITHIC RELIABILITY

GENERAL DESCRIPTION

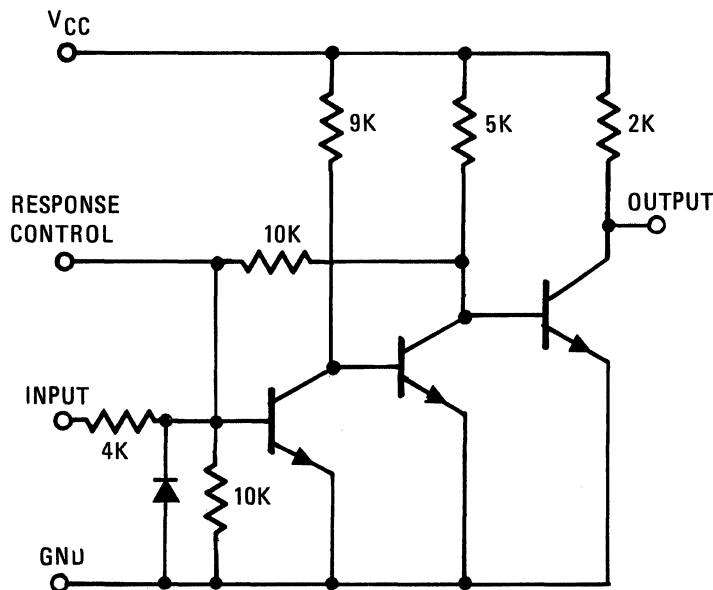
The Harris HD-1489 is a quadruple line receiver monolithic integrated circuit meeting the electrical requirements of EIA Standard RS-232-C for interface between data terminal equipment and data communication equipment. This standard assures electrical interface compatibility between data equipment made by different manufacturers. The receiver circuit is useful in any application requiring transfer of digital signals up to 20K bits per second using common-return signal lines over relatively short distances. The circuit outputs can drive any of the popular DTL or TTL logic families. It is available in a 14-pin hermetic dual in-line package for operation from 0°C to +75°C. The companion quad line driver circuit is the Harris HD-1488.

PACKAGE

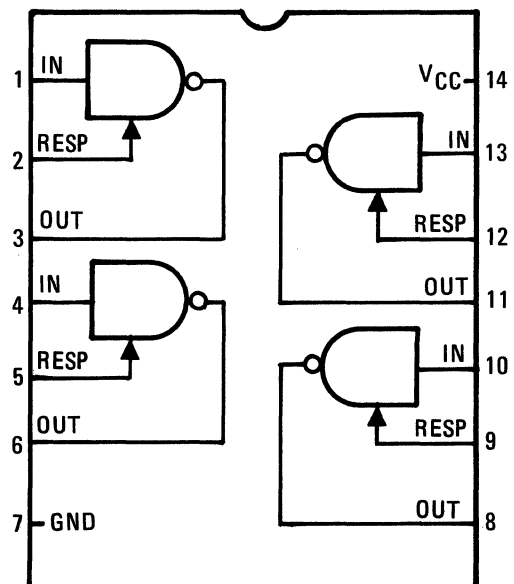
CODE 1A TO-116 (14 LEAD CERAMIC D.I.P)



SCHEMATIC



CONNECTION DIAGRAM



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

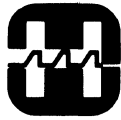
Supply Voltage	+10.0V	Storage Temperature	-65°C to +150°C
Input Voltage	±30.0V	Operating Temperature	0°C to +75°C
Output Current	20mA	Power Dissipation at +25°C	1000mW
		Derate by 5mW/°C	

ELECTRICAL CHARACTERISTICS

Test Conditions: $V_{CC} = +5.0V$, $T_A = 0°C$ to $+75°C$,
Response control pin open unless otherwise specified.

PARAMETER	SYM:	LIMITS			UNITS	TEST CONDITIONS	
		MIN.	TYP.	MAX.			
Input Current	"0"	I_{IL}	-0.43			mA	$V_{IN} = -3.0V$ $V_{IN} = +3.0V$
	"1"	I_{IH}	+0.43				
	"0"	I_{IL}	-3.6		-8.3	mA	$V_{IN} = -25.0V$ $V_{IN} = +25.0V$
	"1"	I_{IH}	+3.6		+8.3		
Input Threshold Voltage (Note 1)	"0"	V_{IL}	0.75		1.25	V	$V_{OH} \geq 2.5V$ $V_{OL} \leq .45V$
	"1"	V_{IH}	1.0		1.5		
D.C. Output Voltage (Note 2)	"0"	V_{OL}		0.2	0.45	V	$V_{IN} = +1.5V, I_{OL} = 10mA$ $V_{IN} = +0.75V, I_{OH} = -0.5mA$ $V_{IN} = \text{Open}, I_{OH} = -0.5mA$
	"1"	V_{OH}	2.6	4.0	5.0		
	"1"	V_{OH}	2.6	4.0	5.0		
Output Short Circuit Current		I_{SC}		3.0		mA	$V_{IN} = +0.75V$
Supply Current		I_{CC}		20	26	mA	$V_{CC} = +5.0V$
Power Dissipation		P_D		100	130	mW	$V_{CC} = +5.0V$
A.C. Propagation Delay		T_{PD+}		60	85	ns	$R_L = 3.9K\Omega$ $R_L = 390\Omega$
		T_{PD-}		25	50		
Rise Time		T_r		90	175	ns	$R_L = 3.9K\Omega$ $R_L = 390\Omega$
Fall Time		T_f		8.0	20		

- NOTES:
- (1) Hysteresis is typically 250mV to prevent output chatter as input signal passes through the threshold region. If desired, thresholds can be made more positive by connecting a resistor from the response control pin to a negative supply; or more negative by connecting the resistor to a positive supply. A capacitor up to 500pF may be connected from the response control pin to ground, making the circuit output less sensitive to narrow noise spikes.
 - (2) This assures that the output will be in the "1" state if the input line is open or shorted to ground.



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HD-1489A

Quad Line Receiver

FEATURES

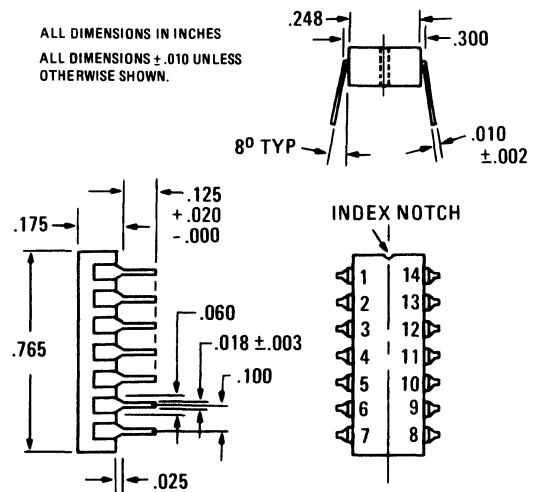
- INPUT HYSTERESIS 1.15V TYP.
- INPUTS WITHSTAND $\pm 30.0V$
- PROVISION FOR THRESHOLD ADJUSTMENT AND/OR NOISE FILTERING
- MONOLITHIC RELIABILITY

GENERAL DESCRIPTION

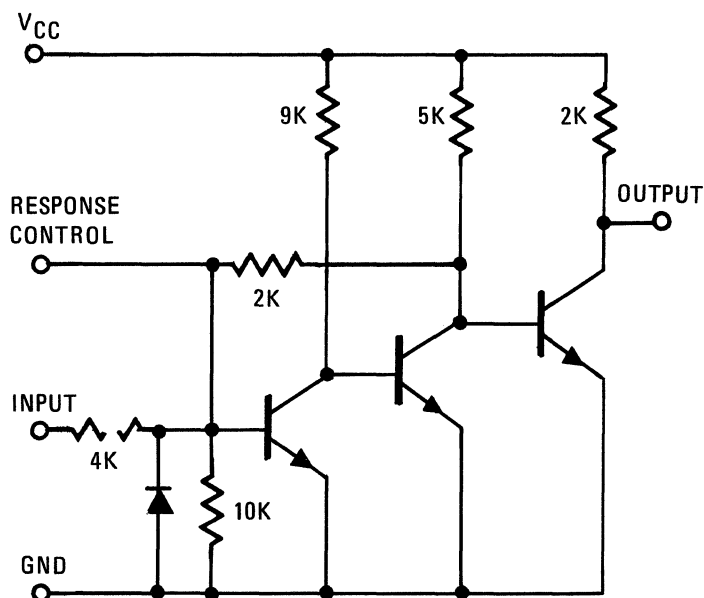
The Harris HD-1489A is a quadruple line receiver monolithic integrated circuit meeting the electrical requirements of EIA Standard RS-232-C for interface between data terminal equipment and data communication equipment. This standard assures electrical interface compatibility between data equipment made by different manufacturers. The receiver circuit is useful in any application requiring transfer of digital signals up to 20K bits per second using common-return signal lines over relatively short distances. The circuit outputs can drive any of the popular DTL or TTL logic families. It is available in a 14-pin hermetic dual in-line package for operation from 0°C to +75°C. The companion quad line driver circuit is the Harris HD-1488.

PACKAGE

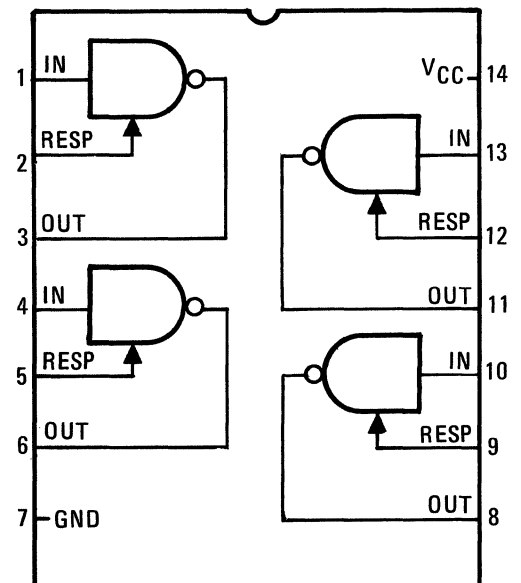
CODE 1A T0-116 (14 LEAD CERAMIC D.I.P)



SCHEMATIC



CONNECTION DIAGRAM



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+10.0V	Storage Temperature	-65°C to +150°C
Input Voltage	±30.0V	Operating Temperature	0°C to +75°C
Output Current	20mA	Power Dissipation at +25°C	1000mW
		Derate by 5mW /°C	

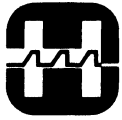
ELECTRICAL CHARACTERISTICS

Test Conditions: $V_{CC} = +5.0V$, $T_A = 0^\circ C$ to $+75^\circ C$,
Response control pin open unless otherwise specified.

PARAMETER	SYM.	LIMITS			UNITS	TEST CONDITIONS	
		MIN.	TYP.	MAX.			
Input Current	"0"	I_{IL}	-43		mA	$V_{IN} = -3.0V$ $V_{IN} = +3.0V$	
	"1"	I_{IH}	+43				
	"0"	I_{IL}	-3.6	-8.3	mA	$V_{IN} = -25.0V$ $V_{IN} = +25.0V$	
	"1"	I_{IH}	+3.6	+8.3			
Input Threshold Voltage (Note 1)	"0"	V_{IL}	0.75	1.25	V	$V_{OH} \geq 2.5V$ $V_{OL} \leq 45V$ $T_A = +25^\circ C$	
	"1"	V_{IH}	1.75	2.25			
D.C. Output Voltage (Note 2)	"0"	V_{OL}		0.2	V	$V_{IN} = +1.5V, I_{OL} = 10mA$ $V_{IN} = +0.75V, I_{OH} = -0.5mA$ $V_{IN} = \text{Open}, I_{OH} = -0.5mA$	
	"1"	V_{OH}	2.6	4.0			
	"1"	V_{OH}	2.6	4.0			
Output Short Circuit Current		I_{SC}		3.0	mA	$V_{IN} = +0.75V$	
Supply Current		I_{CC}		20	26	mA	$V_{CC} = +5.0V$
Power Dissipation		P_D		100	130	mW	$V_{CC} = +5.0V$
A.C. Propagation Delay		T_{PD+}		60	85	ns	$R_L = 3.9K\Omega$ $R_L = 390\Omega$ $T_A = +25^\circ C$
		T_{PD-}		25	50		
	Rise Time		T_r		90	175	
Fall Time		T_f		8.0	20		

- NOTES:
- (1) Hysteresis is typically 1,15V to prevent output chatter as input signal passes through the threshold region. If desired, thresholds can be made more positive by connecting a resistor from the response control pin to a negative supply; or more negative by connecting the resistor to a positive supply. A capacitor up to 500pF may be connected from the response control pin to ground, making the circuit output less sensitive to narrow noise spikes.
 - (2) This assures that the output will be in the "1" state if the input line is open or shorted to ground.

LINEAR



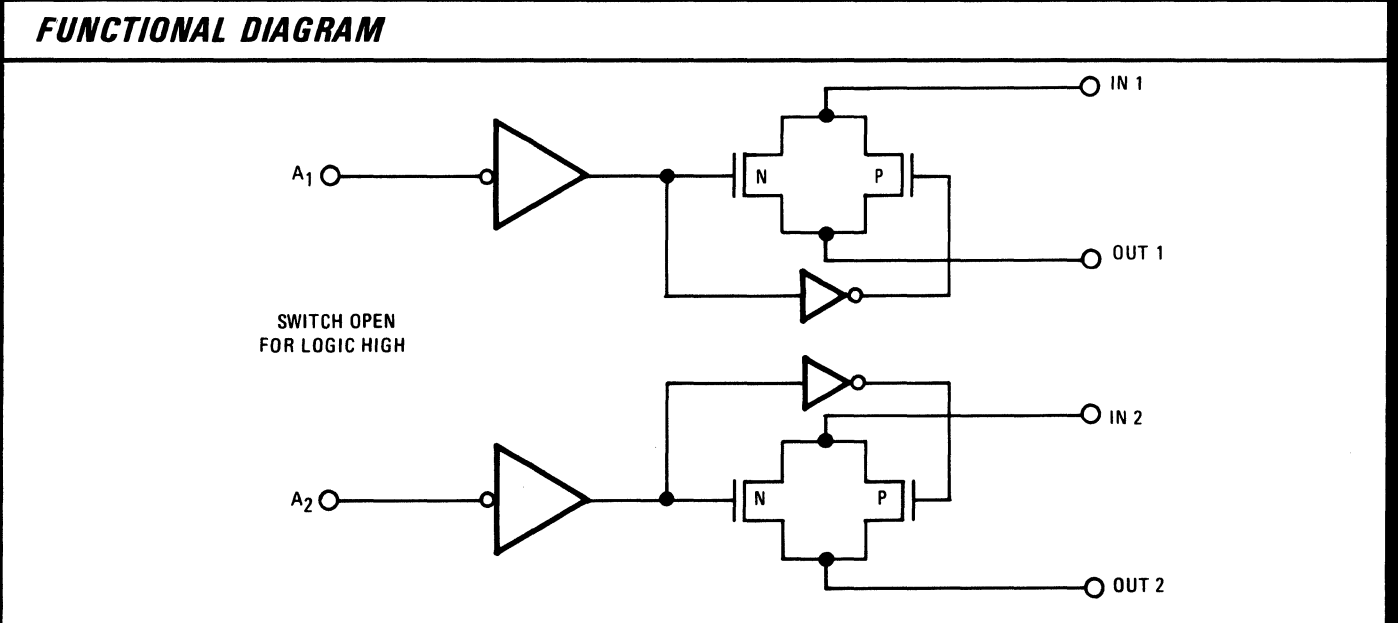
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HI-200

Dual SPST CMOS Analog Switch

LINEAR

FEATURES	DESCRIPTION
<ul style="list-style-type: none"> ● ANALOG SIGNAL RANGE $\pm 15V$ ● TURN-ON TIME (TYP) 240ns ● $R_{ON} < 60\Omega$ (TYP) AT $+25^{\circ}C$ ● SWITCH CURRENT AT $+25^{\circ}C$ 80mA ● LOW POWER DISSIPATION 15mW ● DTL/TTL AND CMOS COMPATIBLE ● NO LATCH-UP 	<p>The HI-200 is a monolithic device consisting of two independently selectable SPST switches. High switching speeds at low power levels are simultaneously achieved using the Harris Dielectric Isolation, Complementary MOS process. Latch-up or SCR phenomenon is inherently non-existent with this process. The device is packaged in a 10 pin TO-100 hermetic can and is available in both military and commercial temperature ranges.</p>
PIN OUT	PACKAGE
<p style="text-align: center;">TOP VIEW</p>	<p style="text-align: center;">CODE 2G T0-100</p> <p style="text-align: center;">BOTTOM VIEW</p>



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between Pins 6 and 10	40V	Total Power Dissipation *	450mW
V _{REF} to Ground	+20V, -5V	Operating Temperature	
Digital Input Voltage:	+V _{Supply} +4V	HI-200-2	-55°C to +125°C
	-V _{Supply} -4V	HI-200-5	0°C to +75°C
Analog Input Voltage (One Switch)	+V _{Supply} +2.0V	Storage Temperature	-65°C to +150°C
	-V _{Supply} -2.0V		

*Derate 6 mW/°C above T_A = 75°C

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified

Supplies = +15V, -15V; V_{REF} (Pin 7) = Open; V_{AH} (Logic Level High) = 3.0V V_{AL} (Logic Level Low) = +0.8V

For Test Conditions, consult Performance Characteristics

PARAMETER	TEMP.	-55°C to +125°C			0°C to +75°C			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
<u>ANALOG SWITCH CHARACTERISTICS</u>								
*V _S , Analog Signal Range	Full	-15		+15	-15		+15	V
*R _{ON} , On Resistance (Note 1)	+25°C		55	70		55	80	Ω
	Full		80	100		72	100	Ω
*I _{S(OFF)} , Off Input Leakage Current	+25°C		1			1		nA
	Full		100	500		10	500	nA
*I _{D(OFF)} , Off Output Leakage Current	+25°C		1			1		nA
	Full		100	500		10	500	nA
*I _{D(ON)} , On Leakage Current	+25°C		.02			.02		nA
	Full		6	500		6	500	nA
<u>DIGITAL INPUT CHARACTERISTICS</u>								
V _{AL} , Input Low Threshold	Full			0.8			0.8	V
V _{AH} , Input High Threshold	Full	3.0			3.0			V
*I _A , Input Leakage Current (High or Low) (Note 2)	Full			1.0			1.0	μA
<u>SWITCHING CHARACTERISTICS</u>								
t _{OPEN} , Break - Before Make Delay (Note 3)	+25°C		60			60		ns
t _{on} , Switch on Time	+25°C		240	500		240		ns
t _{off} , Switch off Time	+25°C		330	500		500		ns
"Off Isolation" (Note 4)	+25°C		70			70		dB
C _{S(OFF)} , Input Switch Capacitance	+25°C		5.5			5.5		pF
C _{D(OFF)} , {	+25°C		5.5			5.5		pF
C _{D(ON)} , } Output Switch Capacitance	+25°C		11			11		pF
C _A , Digital Input Capacitance	+25°C		5			5		pF
C _{DS(OFF)} , Drain-To-Source Capacitance	+25°C		0.5			0.5		pF
<u>POWER REQUIREMENTS</u> (Note 5)								
P _D , Power Dissipation	+25°C		15			15		mW
	Full			60			60	mW
*I ⁺ , Current (Pin 10)	+25°C		0.5			0.5		mA
	Full			2.0			2.0	mA
*I ⁻ , Current (Pin 6)	+25°C		0.5			0.5		mA
	Full			2.0			2.0	mA

NOTES:

1. V_{OUT} = +10V I_{OUT} = 1mA

2. Digital Inputs Are MOS Gates Typical Leakage is Less Than 1nA

3. V_{AH} = 4.0V

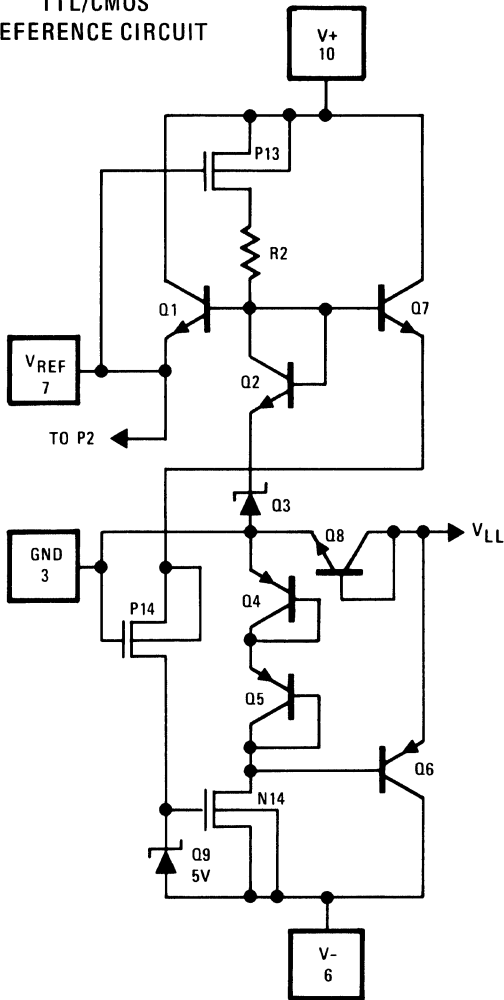
4. V_A = +3V, R_L = 1KΩ, C_L = 10pF, V_S = 3VRMS, f, 100 kHz

5. V_A = +3V or V_A = 0V For Both Switches

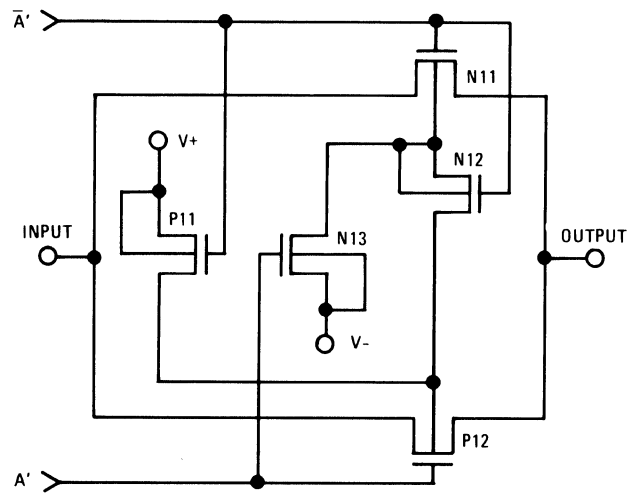
*100% Tested For DASH 8

SCHEMATIC DIAGRAMS

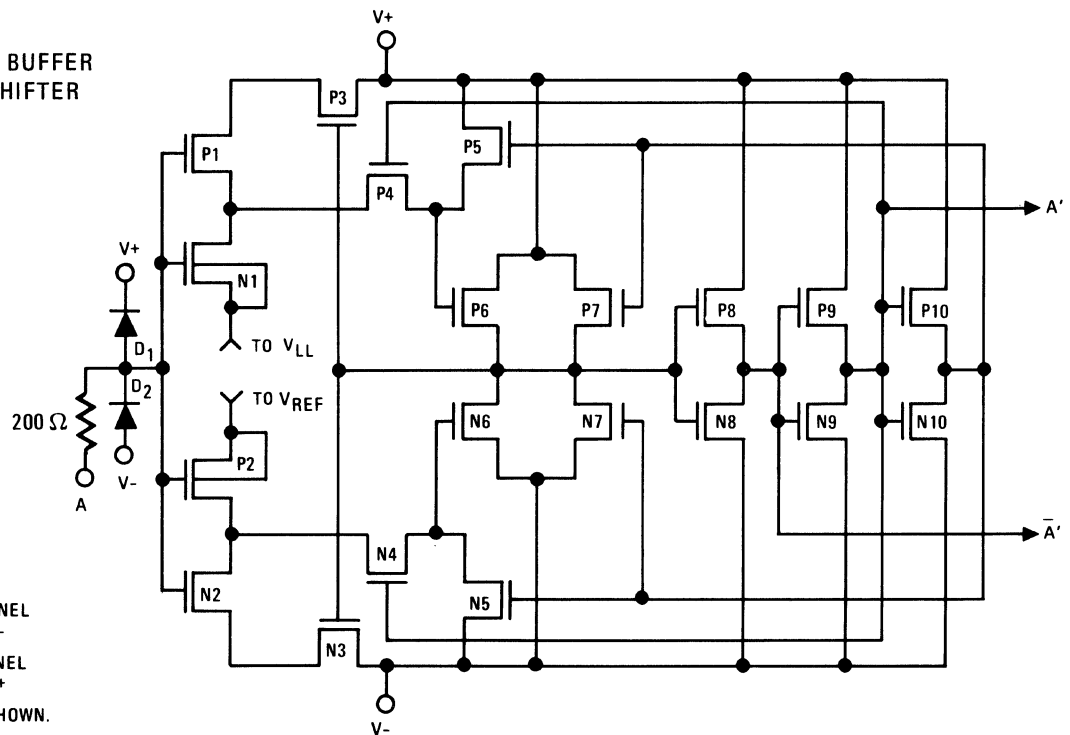
TTL/CMOS REFERENCE CIRCUIT



SWITCH CELL



DIGITAL INPUT BUFFER AND LEVEL SHIFTER

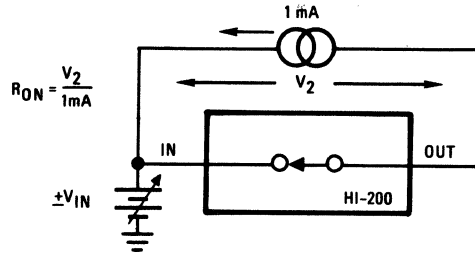


ALL N-CHANNEL BODIES TO V-
ALL P-CHANNEL BODIES TO V+
EXCEPT AS SHOWN.

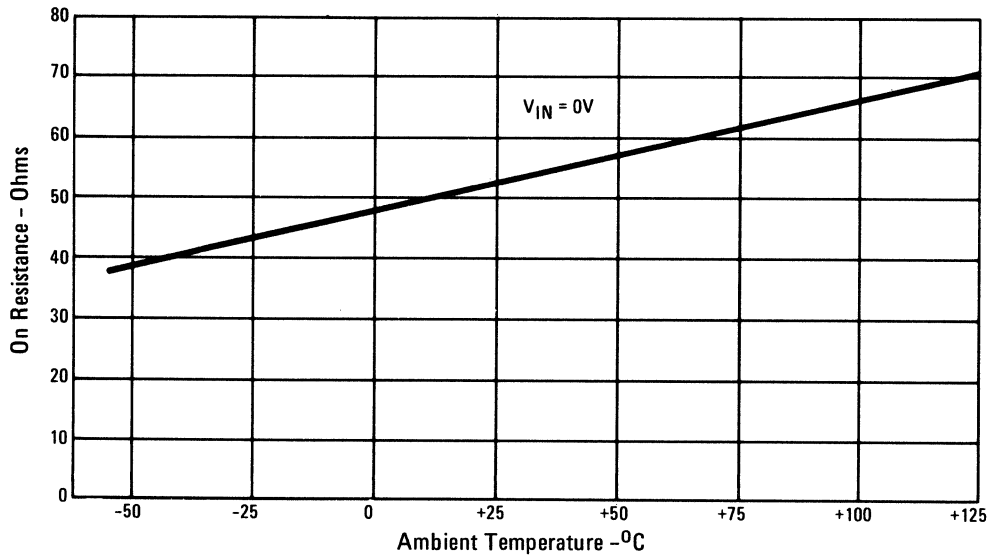
PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS

(UNLESS OTHERWISE SPECIFIED $T_A = 25^\circ\text{C}$, $V_{\text{SUPPLY}} = \pm 15\text{V}$, $V_{\text{AH}} = 3.0\text{V}$, $V_{\text{AL}} = 0.8\text{V}$ AND $V_{\text{REF}} = \text{OPEN}$).

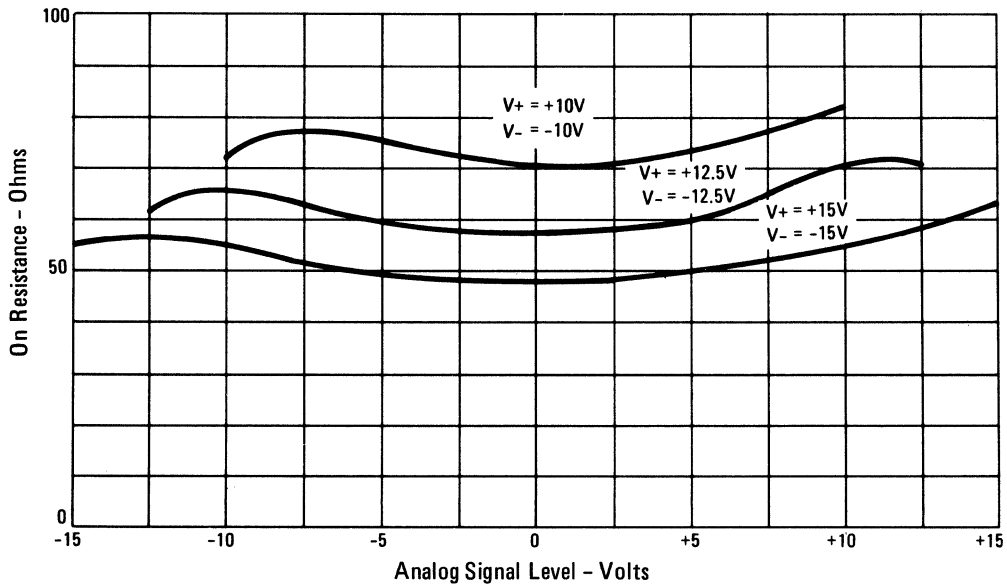
ON RESISTANCE vs. ANALOG SIGNAL LEVEL,
SUPPLY VOLTAGE AND TEMPERATURE



ON RESISTANCE vs. TEMPERATURE



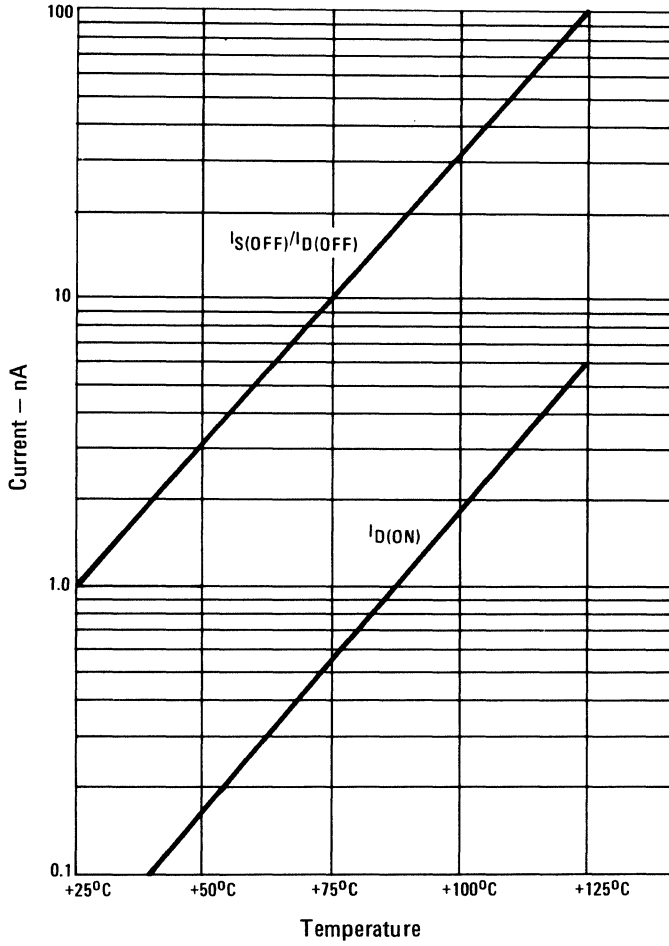
(HI-200)
ON RESISTANCE vs. ANALOG SIGNAL LEVEL
AND POWER SUPPLY VOLTAGE



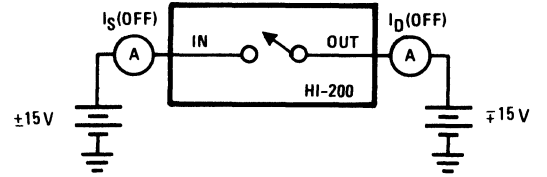
LINEAR

PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (continued)

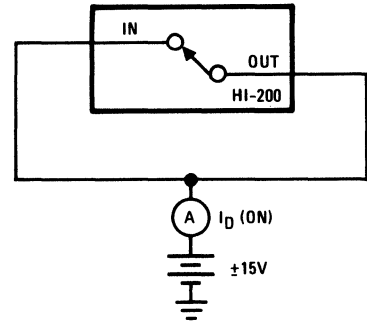
SWITCH LEAKAGE CURRENT vs. TEMPERATURE (HI-200)



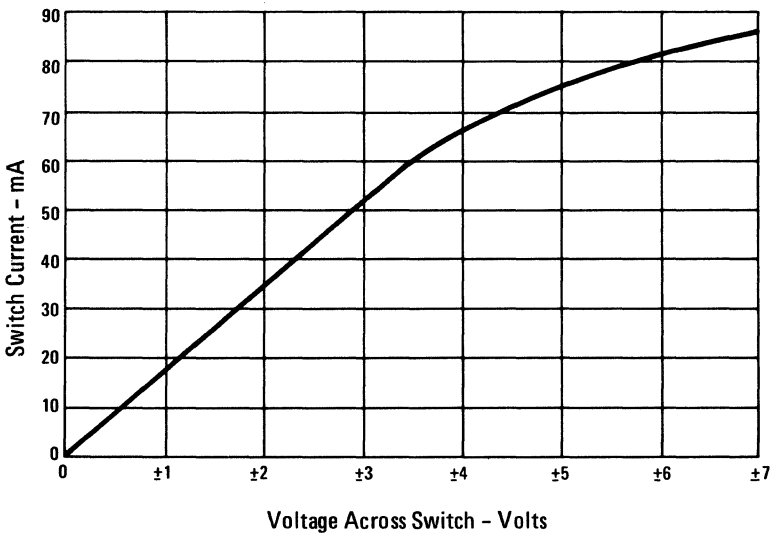
OFF LEAKAGE CURRENT vs. TEMPERATURE



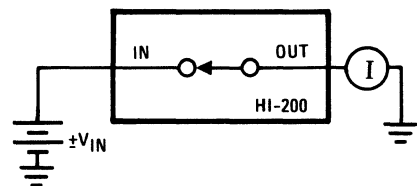
ON LEAKAGE CURRENT vs. TEMPERATURE



SWITCH CURRENT vs. VOLTAGE

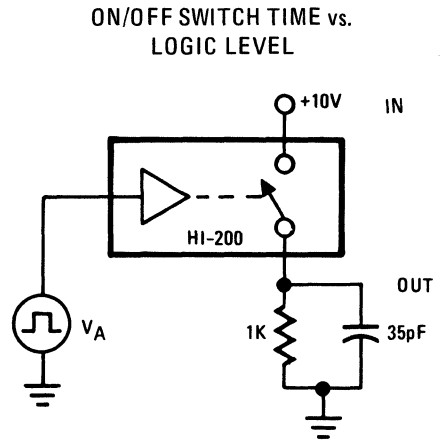
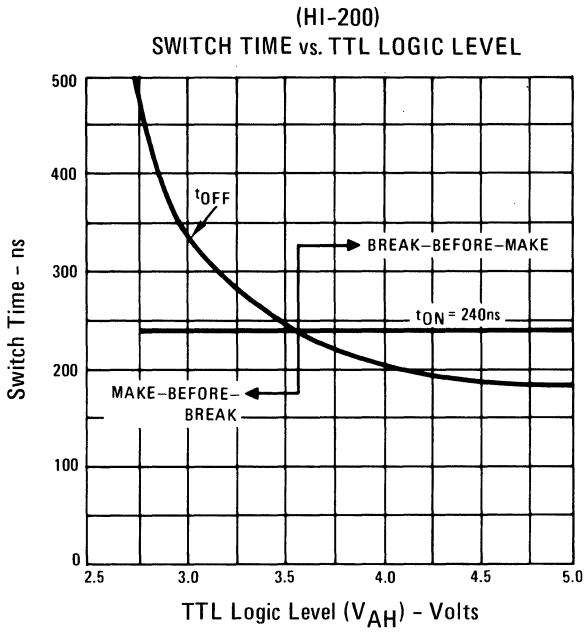


SWITCH CURRENT vs. VOLTAGE

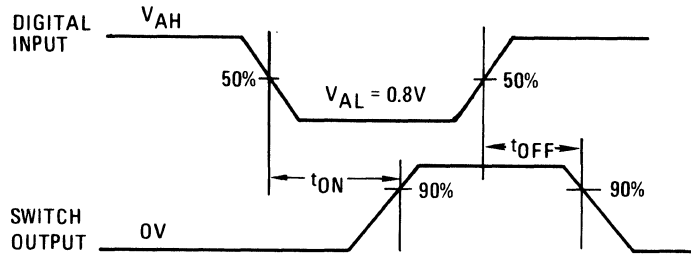


LINEAR

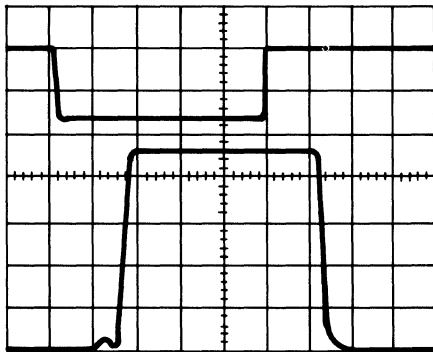
PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (continued)



SWITCHING WAVEFORMS

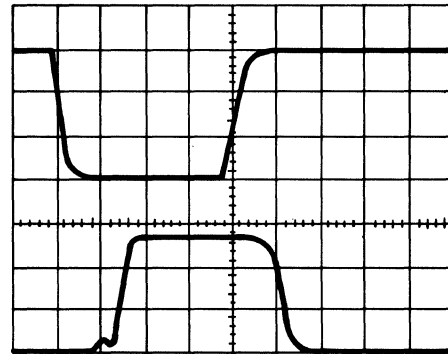


t_{ON}, t_{OFF} (TTL INPUT)
 $V_{AH} = +4.0V$

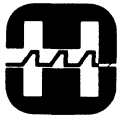


Top: TTL Input Vertical: 2V/Div.
Bottom: Output Horizontal: 200ns/Div.

t_{ON}, t_{OFF} (CMOS INPUT)
 $V_{REF} = OPEN, V_{AH} = +15V$



Top: CMOS Input Vertical: 5V/Div.
Bottom: Output Horizontal: 200ns/Div.



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HI-201

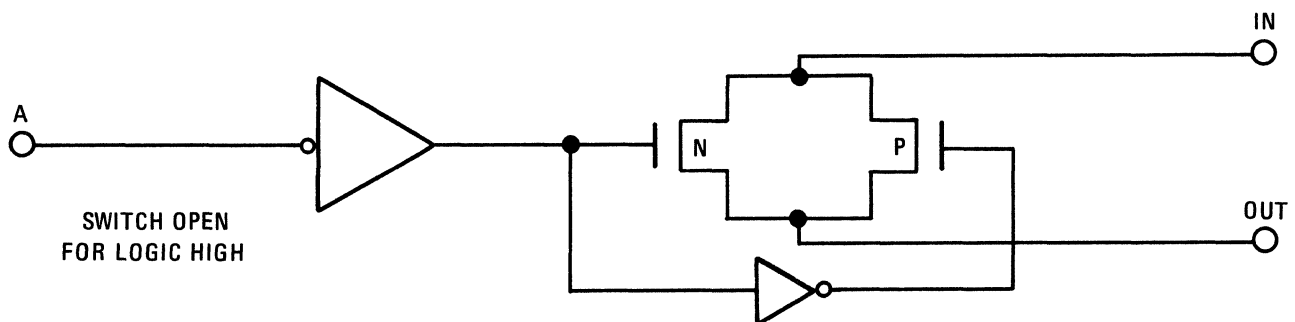
Quad SPST CMOS Analog Switch

LINEAR

FEATURES	DESCRIPTION
<ul style="list-style-type: none"> ● ANALOG SIGNAL RANGE ±15V ● TURN-ON TIME (TYP) 185 ns ● ON RESISTANCE (TYP) 65 Ω ● NO LATCH-UP ● NO DIGITAL INPUT CURRENT SPIKE ● DTL/TTL AND CMOS COMPATIBLE 	<p>The HI-201 is a monolithic device consisting of four independently selectable SPST switches. High switching speeds at low power levels are simultaneously achieved using the Harris Dielectric Isolation, Complementary MOS process. Latch-up or SCR phenomenon is inherently non-existent with this process. The device is packaged in a 16 pin hermetic Dual In-Line and is available in both military and commercial temperature ranges.</p>
PIN OUT	PACKAGE
	<p>CODE 1W 16 LEAD D.I.P.</p>

FUNCTIONAL DIAGRAM

TYPICAL SWITCH



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between Pins 4 and 13	40V	Total Power Dissipation*	750mW
V _{REF} to Ground	+20V, -5V	Operating Temperature	
Digital Input Voltage:	V _{Supply} (+) +4V	HI-201-2	-55°C to +125°C
	V _{Supply} (-) -4V	HI-201-5	0°C to +75°C
Analog Input Voltage (One Switch)	+V _{Supply} +2.0V	Storage Temperature	-65°C to +150°C
	-V _{Supply} -2.0V		

*Derate 8 mW/°C Above T_A = +75°C

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified

Supplies = +15V, -15V; V_{REF} (Pin 7) = Open; V_{AH} (Logic Level High) = 3.0V V_{AL} (Logic Level Low) = +0.8V

For Test Conditions, consult Performance Characteristics

PARAMETER	TEMP.	HI-201-2			HI-201-5			UNITS
		-55°C to +125°C			0°C to +75°C			
<u>ANALOG SWITCH CHARACTERISTICS</u>								
*V _S , Analog Signal Range	Full	-15		+15	-15		+15	V
*R _{ON} , On Resistance (Note 1)	+25°C		65	80		65	100	Ω
	Full		85	125		75	125	Ω
*I _{S(OFF)} , Off Input Leakage Current	+25°C		2			2		nA
	Full			500			250	nA
*I _{D(OFF)} , Off Output Leakage Current	+25°C		2			2		nA
	Full			500			250	nA
*I _{D(ON)} , On Leakage Current	+25°C		2			2		nA
	Full			500			250	nA
<u>DIGITAL INPUT CHARACTERISTICS</u>								
V _{AL} , Input Low Threshold	Full			0.8			0.8	V
V _{AH} , Input High Threshold	Full	3.0			3.0			V
*I _A , Input Leakage Current (High or Low) (Note 2)	Full			1.0			1.0	μA
<u>SWITCHING CHARACTERISTICS</u>								
t _{OPEN} , Break - Before Make Delay (Note 3)	+25°C		30			30		ns
t _{on} , Switch ON Time	+25°C		185	500		185		ns
t _{off} , Switch OFF Time	+25°C		220	500		220		ns
"Off Isolation" (Note 4)	+25°C		80			80		dB
C _S (OFF), Input Switch Capacitance	+25°C		5.5			5.5		pF
C _D (OFF), } C _D (ON) } Output Switch Capacitance	+25°C		5.5			5.5		pF
	+25°C		11			11		pF
C _A , Digital Input Capacitance	+25°C		5			5		pF
C _{DS} (OFF), Drain-To-Source Capacitance	+25°C		0.5			0.5		pF
<u>POWER REQUIREMENTS</u> (Note 5)								
P _D , Power Dissipation	+25°C		15			15		mW
*I ₊ , Current (Pin 13)	Full			60			60	mW
	+25°C		0.5			0.5		mA
*I ₋ , Current (Pin 4)	Full			2.0			2.0	mA
	+25°C		0.5			0.5		mA

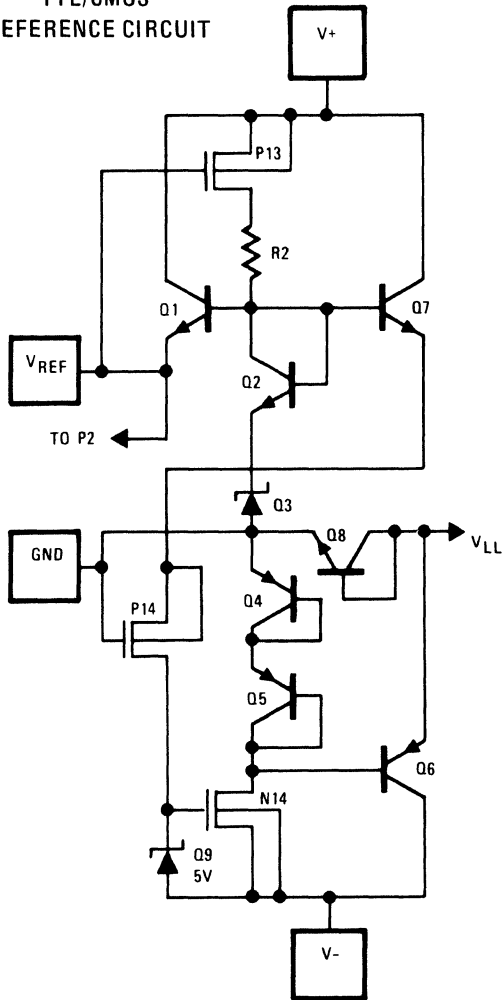
NOTES: 1. V_{OUT} = +10V I_{OUT} = 1mA
 2. Digital Inputs Are MOS Gates - Typical Leakage is Less Than 1nA
 3. V_{AH} = 4.0V

4. V_A = 5V, R_L = 1KΩ, C_L = 10pF, V_S = 3VRMS, f = 100KHz
 5. V_A = +3V or V_A = 0V For all Switches

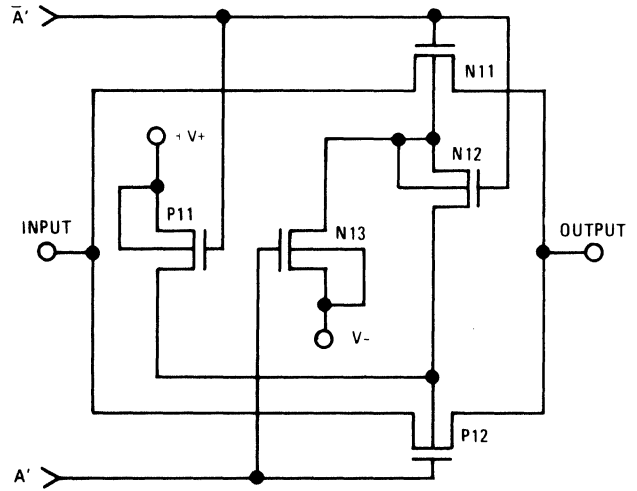
*100% Tested For DASH 8

SCHEMATIC DIAGRAMS

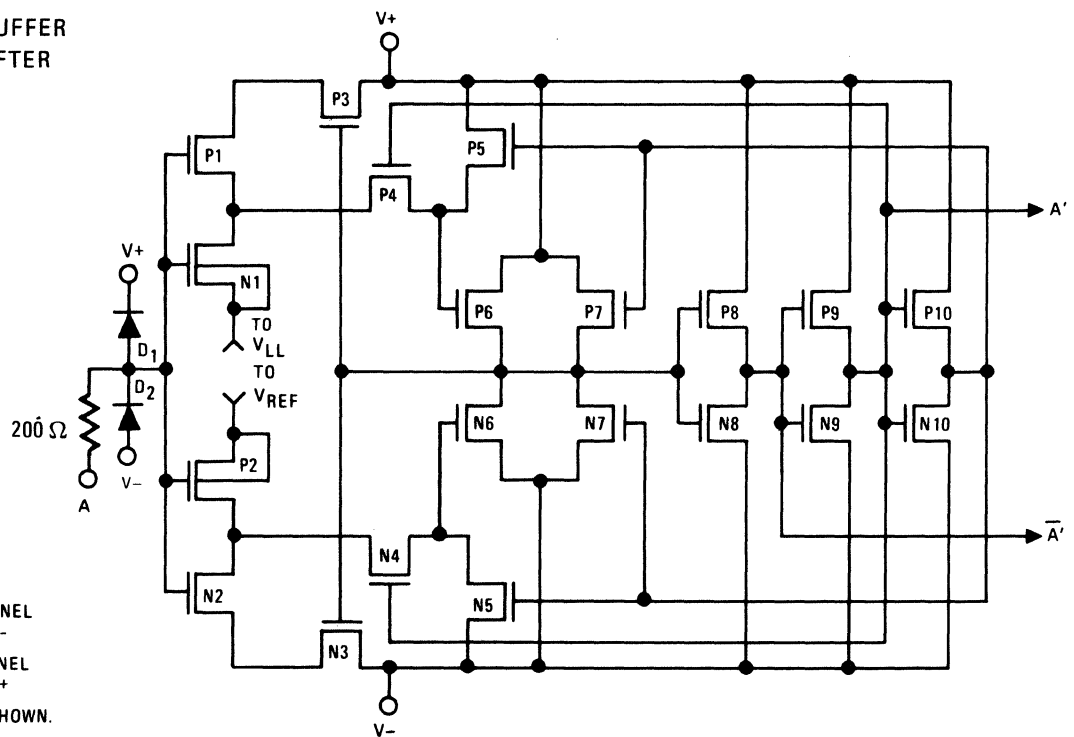
TTL/CMOS
REFERENCE CIRCUIT



SWITCH CELL



DIGITAL INPUT BUFFER
AND LEVEL SHIFTER

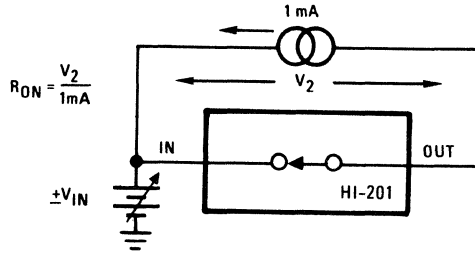


ALL N-CHANNEL
BODIES TO V-
ALL P-CHANNEL
BODIES TO V+
EXCEPT AS SHOWN.

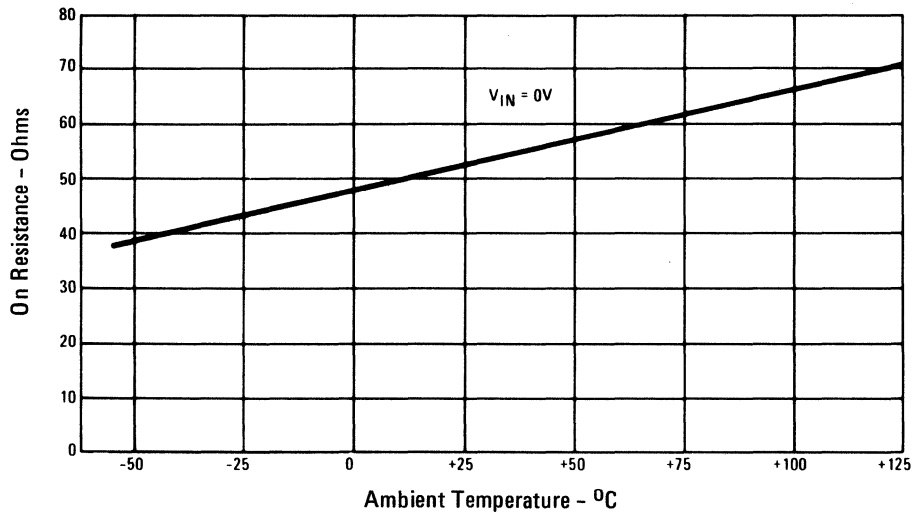
PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS

(UNLESS OTHERWISE SPECIFIED $T_A = 25^{\circ}\text{C}$, $V_{\text{SUPPLY}} = \pm 15\text{V}$, $V_{\text{AH}} = 3.0\text{V}$ $V_{\text{AL}} = 0.8\text{V}$ AND $V_{\text{REF}} = \text{OPEN}$).

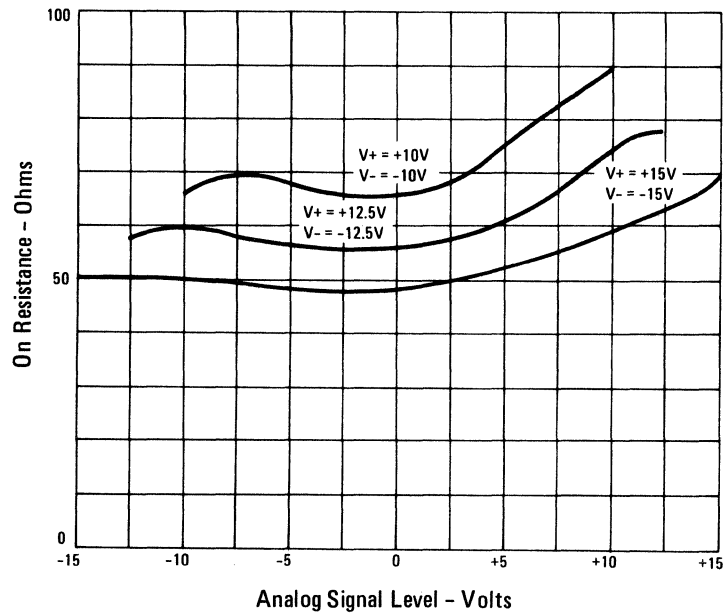
ON RESISTANCE vs. ANALOG SIGNAL LEVEL,
SUPPLY VOLTAGE AND TEMPERATURE



ON RESISTANCE vs. TEMPERATURE



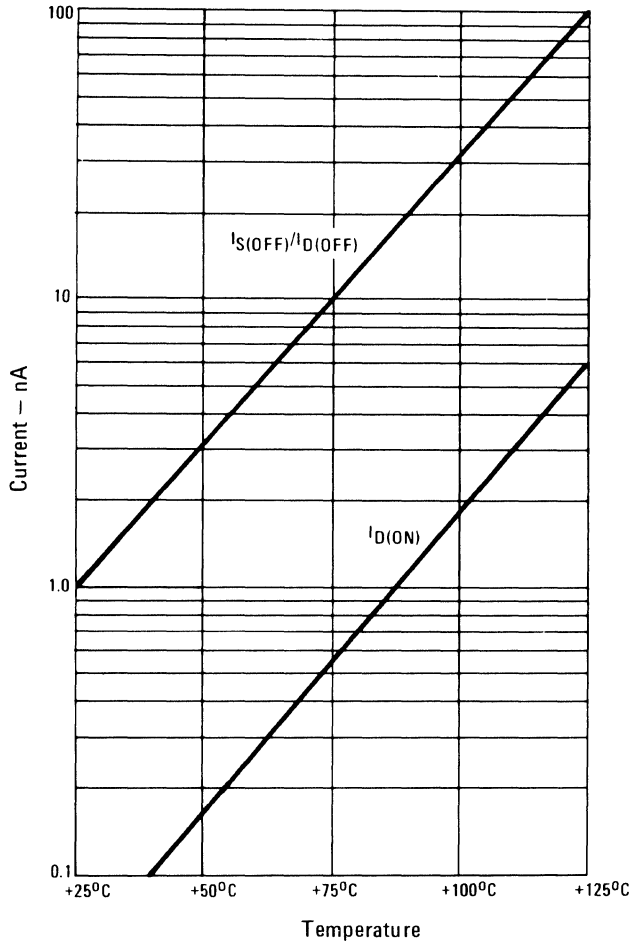
(HI-201)
ON RESISTANCE vs. ANALOG SIGNAL LEVEL
AND POWER SUPPLY VOLTAGE



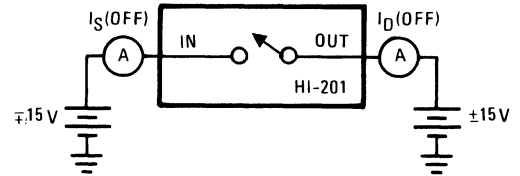
LINEAR

PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (continued)

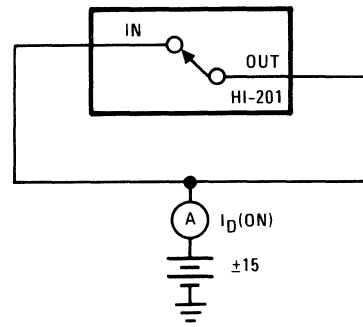
SWITCH LEAKAGE CURRENT vs. TEMPERATURE (HI-201)



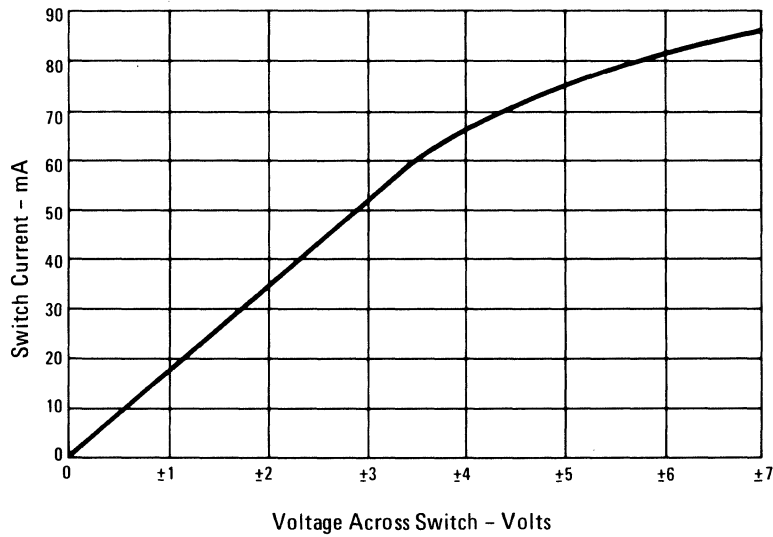
OFF LEAKAGE CURRENT vs. TEMPERATURE



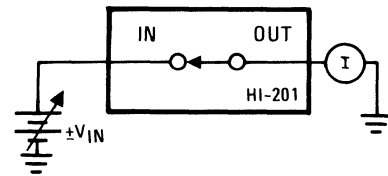
ON LEAKAGE CURRENT vs. TEMPERATURE



SWITCH CURRENT vs. VOLTAGE

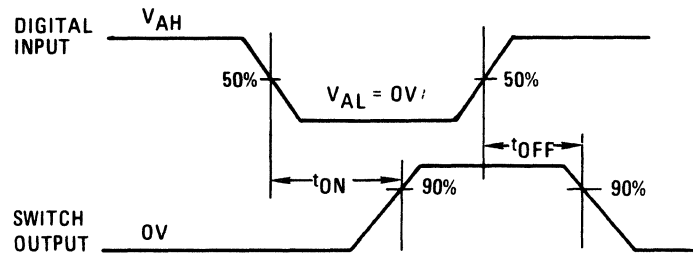


SWITCH CURRENT vs. VOLTAGE

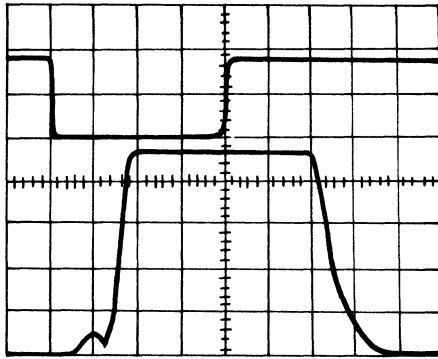


LINEAR

SWITCHING WAVEFORMS

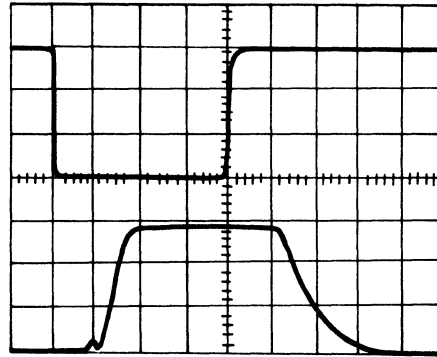


t_{ON}, t_{OFF} (TTL INPUT)
 $V_{IN} = 3.5V$



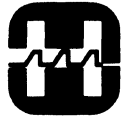
Top: TTL Input Horizontal: 100ns/Div.
Bottom: Output Vertical: 2V/Div.

t_{ON}, t_{OFF} (CMOS INPUT)
 $V_{REF} = OPEN, V_{IN} = +15V$



Top: CMOS Input Vertical: 5V/Div.
Bottom: Output Horizontal: 100ns/Div.

LINEAR



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HI-506A/HI-507A

16 Channel Analog Multiplexer with Overvoltage Protection

FEATURES

- ANALOG/DIGITAL OVERVOLTAGE PROTECTION
- FAIL SAFE WITH POWER LOSS (NO LATCHUP)
- BREAK BEFORE MAKE SWITCHING
- DTL/TTL AND CMOS COMPATIBLE
- ANALOG SIGNAL RANGE $\pm 15V$
- ACCESS TIME 500ns TYP.
- SUPPLY CURRENT AT 1MHz ADDRESS TOGGLE 4mA TYP.
- STANDBY POWER 7.5mW TYP.

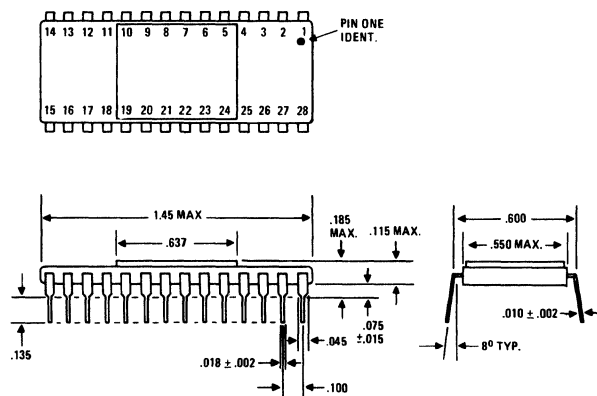
DESCRIPTION

The HI-506A and HI-507A analog multiplexers are constructed with the Harris Dielectric Isolation, Complementary MOS process. Digital and Analog inputs are protected from overvoltage inputs that exceed either supply voltage with no channel interaction. Channel interaction is also eliminated in the event of power loss. The HI-506A is a single-ended 16 channel multiplexer while the HI-507A is a differential 8 channel version. The devices are packaged in a 28 pin dual-in-line package and are available in both military and commercial temperature ranges.

PACKAGE

CODE 1L

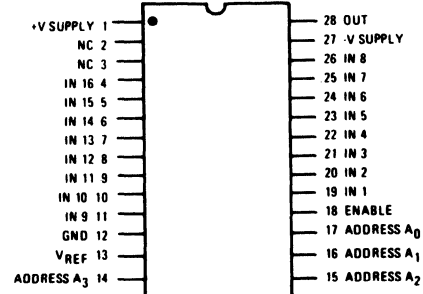
28 LEAD D.I.P.



PIN OUT/TRUTH TABLE

HI-506A

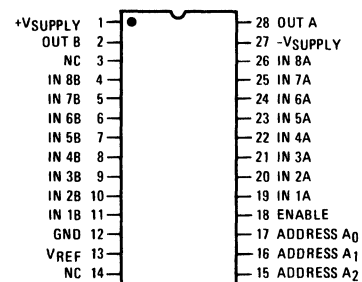
Top View



A ₃	A ₂	A ₁	A ₀	EN	"ON" CHANNEL
X	X	X	X	L	NONE
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

HI-507A

Top View



A ₂	A ₁	A ₀	EN	"ON" SWITCH PAIR
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

LINEAR

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between Pins 1 and 27 40V
 V_{REF} to Ground +20V
 V_{EN}, V_A, Digital Input Overvoltage:
 $V_A \begin{cases} V_{Supply(+)} +4V \\ V_{Supply(-)} -4V \end{cases}$
 Analog Input Overvoltage:
 $V_S \begin{cases} V_{Supply(+)} +20V \\ V_{Supply(-)} -20V \end{cases}$

Total Power Dissipation* 1200mW
 Operating Temperature:
 HI-506A/HI-507A-2 -55°C to +125°C
 HI-506A/HI-507A-5 0°C to +75°C
 Storage Temperature -65°C to +150°C

*Derate 8mW/°C above T_A = +25°C

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified.

Supplies = +15V, -15V; V_{REF} (Pin 13) = Open; V_{AH} (Logic Level High) = +4.0V; V_{AL} (Logic Level Low) = +0.8V
 For Test Conditions, consult Performance Characteristics section.

PARAMETER	TEMP.	HI-506A/507A-2 -55°C to +125°C			HI-506A/507A-5 0°C to +75°C			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
ANALOG CHANNEL CHARACTERISTICS								
*V _S , Analog Signal Range	Full	-15		+15	-15		+15	V
*R _{ON} , On Resistance (Note 1)	+25°C Full		1.2 1.5	1.5 2.0		1.5 1.8	1.8 2.0	kΩ kΩ
*I _{S(OFF)} , Off Input Leakage Current	+25°C Full		0.03			0.03		nA nA
*I _{D(OFF)} , Off Output Leakage Current	+25°C Full		1.0			1.0		nA nA
*I _{D(OFF)} with Input Overvoltage Applied (Note 2)	HI-506A Full			±500			±500	nA
	HI-507A Full			±250			±250	nA
*I _{D(OFF)} with Input Overvoltage Applied (Note 2)	+25°C Full		4.0			4.0		nA μA
	+25°C Full			2.0				μA
*I _{D(ON)} , On Channel Leakage Current	HI-506A Full		0.1			0.1		nA nA
	HI-507A Full			±250			±250	nA
DIGITAL INPUT CHARACTERISTICS								
V _{AL} , Input Low Threshold	Full			0.8			0.8	V
V _{AH} , Input High Threshold	Full	4.0			4.0			V
V _{AL} , V _{AH}	+25°C			0.8			0.8	V
	+25°C	6.0			6.0			V
*I _A , Input Leakage Current (High or Low)	Full			1.0			5.0	μA
SWITCHING CHARACTERISTICS								
t _A , Access Time	+25°C		0.5	1.0		0.5		μs
t _{OPEN} , Break - Before Make Delay	+25°C		80			80		ns
t _{ON (EN)} , Enable Delay (ON)	+25°C		300			300		ns
t _{OFF (EN)} , Enable Delay (OFF)	+25°C		300			300		ns
"Off Isolation" (Note 4)	+25°C		65			65		dB
C _{S (OFF)} , Channel Input Capacitance	+25°C		5			5		pF
C _{D (OFF)} , Channel Output Capacitance	HI-506A +25°C		50			50		pF
	HI-507A +25°C		25			25		pF
C _A , Digital Input Capacitance	+25°C		5			5		pF
C _{DS (OFF)} , Input to Output Capacitance	+25°C		1			1		pF
POWER REQUIREMENTS								
P _D , Power Dissipation	Full		7.5			7.5		mW
*I ₊ , Current Pin 1 (Note 5)	Full		0.5	2.0		0.5	5.0	mA
*I ₋ , Current Pin 27 (Note 5)	Full		0.02	1.0		0.02	2.0	mA
*I ₊ , Standby (Note 6)	Full		0.5	2.0		0.5	5.0	mA
*I ₋ , Standby (Note 6)	Full		0.02	1.0		0.02	2.0	mA

- NOTES
- V_{OUT} = ±10V, I_{OUT} = -100 μA
 - Analog Overvoltage = ±33V
 - V_{REF} = +10V
 - V_{EN} = 0.8V, R_L = 1K, C_L = 7pF, V_S = 3VRMS, f = 500KHz
 - V_{EN} = +4.0V
 - V_{EN} = 0.8V
 - To drive from DTL/TTL circuits, 1KΩ Pull-up resistors to +5.0V supply are recommended

*100% Tested For DASH 8

LINEAR

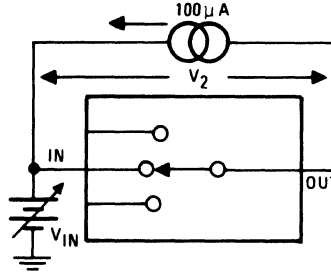
PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS

(UNLESS OTHERWISE SPECIFIED $T_A = 25^\circ\text{C}$, $V_{\text{SUPPLY}} = \pm 15\text{V}$, $V_{\text{AH}} = +4\text{V}$, $V_{\text{AL}} = 0.8\text{V}$ AND $V_{\text{REF}} = \text{OPEN}$.)

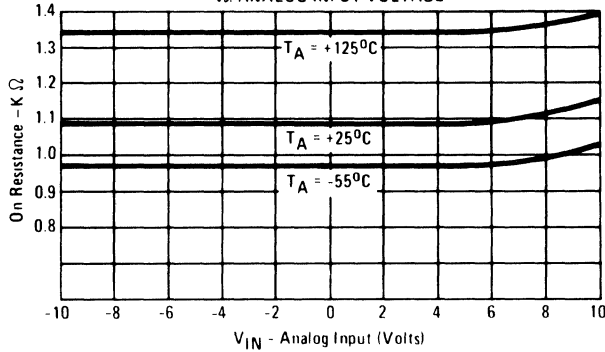
TEST CIRCUIT NO.1

ON RESISTANCE vs. INPUT SIGNAL LEVEL, SUPPLY VOLTAGE

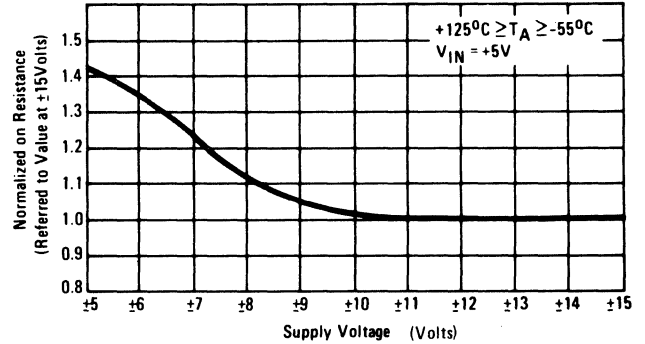
$$R_{\text{ON}} = \frac{V_2}{100\mu\text{A}}$$



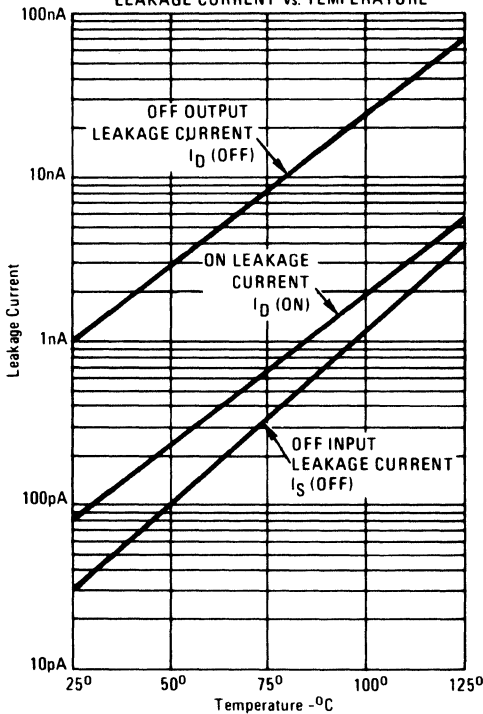
ON RESISTANCE vs. ANALOG INPUT VOLTAGE



NORMALIZED ON RESISTANCE vs. SUPPLY VOLTAGE

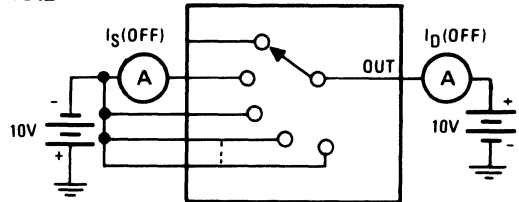


LEAKAGE CURRENT vs. TEMPERATURE



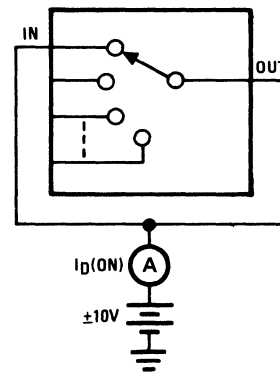
TEST CIRCUIT NO.2

OFF LEAKAGE CURRENT vs. TEMPERATURE

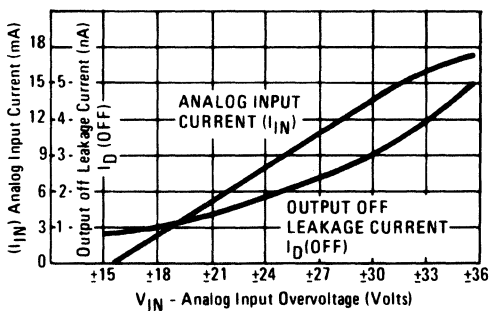


ON LEAKAGE CURRENT vs. TEMPERATURE

TEST CIRCUIT NO.3

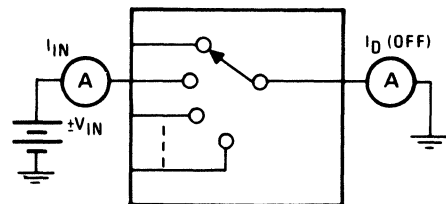


ANALOG INPUT OVERVOLTAGE CHARACTERISTICS

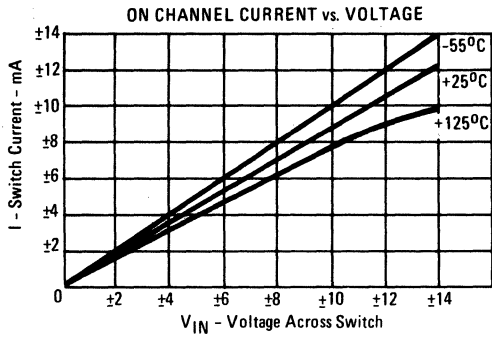


ANALOG INPUT OVERVOLTAGE CHARACTERISTICS

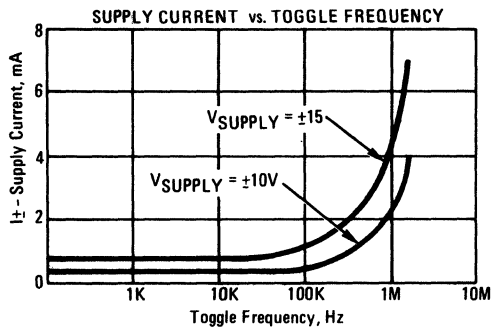
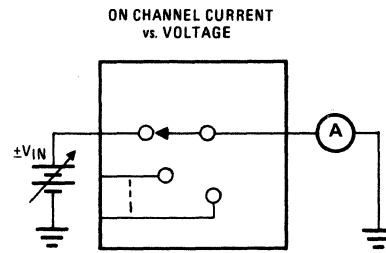
TEST CIRCUIT NO.4



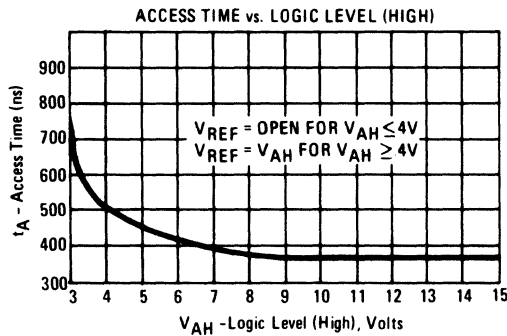
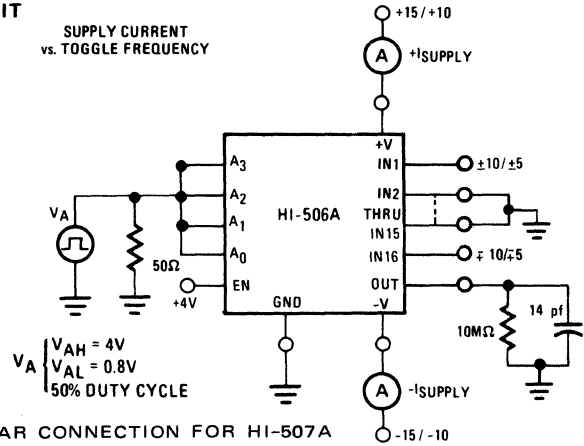
PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (continued)



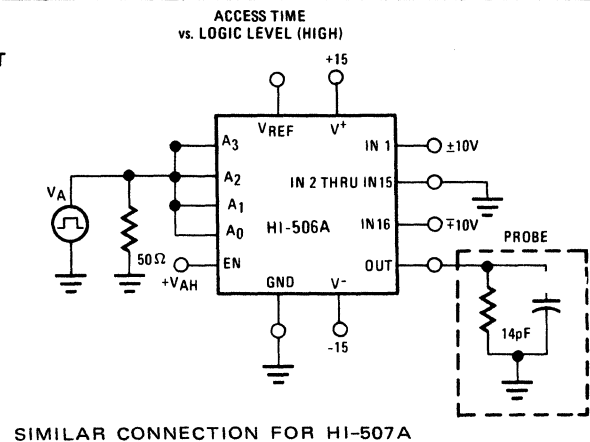
TEST CIRCUIT NO.5



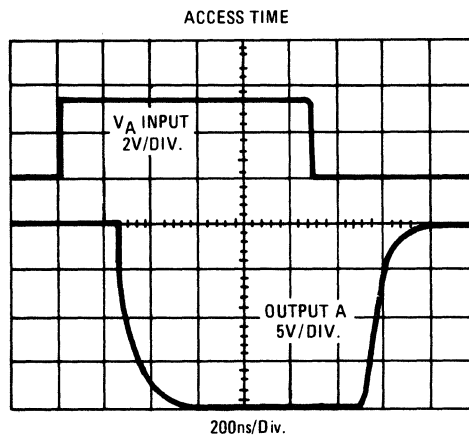
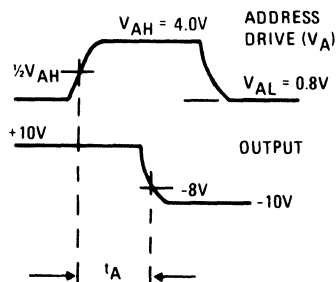
TEST CIRCUIT NO.6



TEST CIRCUIT NO.7

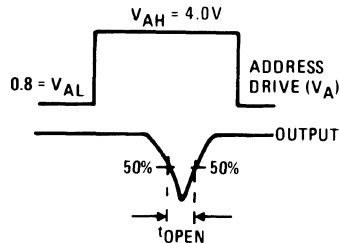


SWITCHING WAVEFORMS

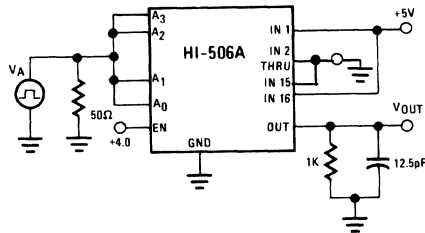


SWITCHING WAVEFORMS (continued)

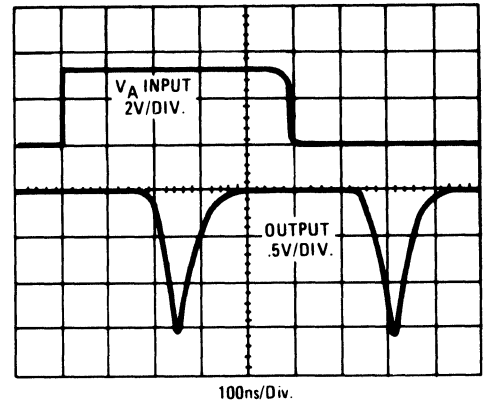
TEST CIRCUIT NO.8



BREAK BEFORE MAKE DELAY (t_{OPEN})

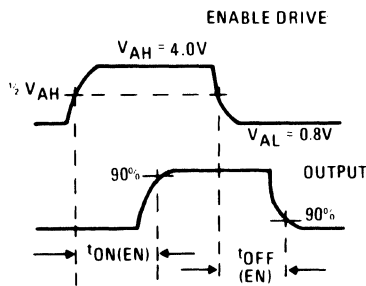


BREAK BEFORE MAKE DELAY (t_{OPEN})

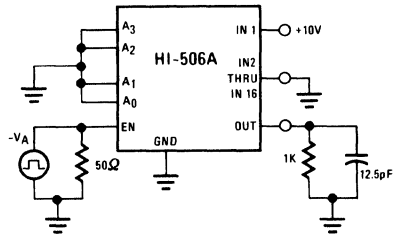


SIMILAR CONNECTION FOR HI-507A

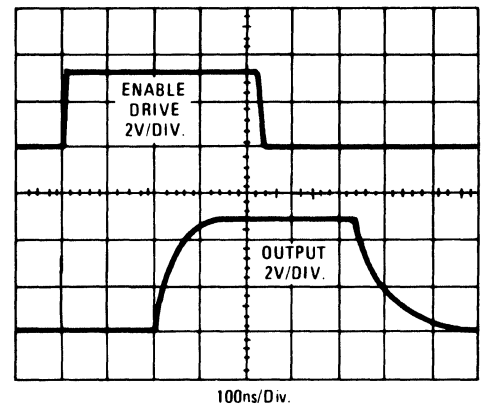
TEST CIRCUIT NO.9



ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)



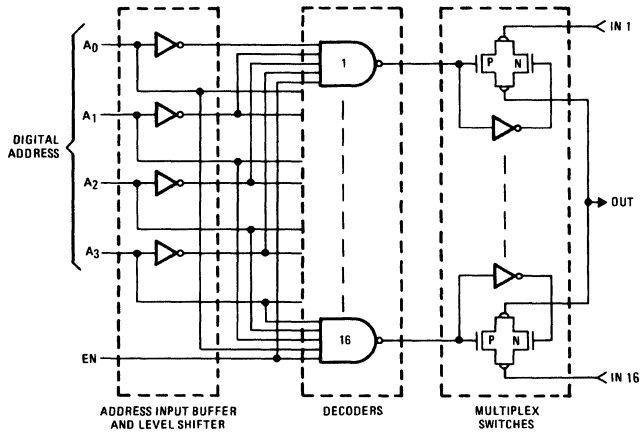
ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)



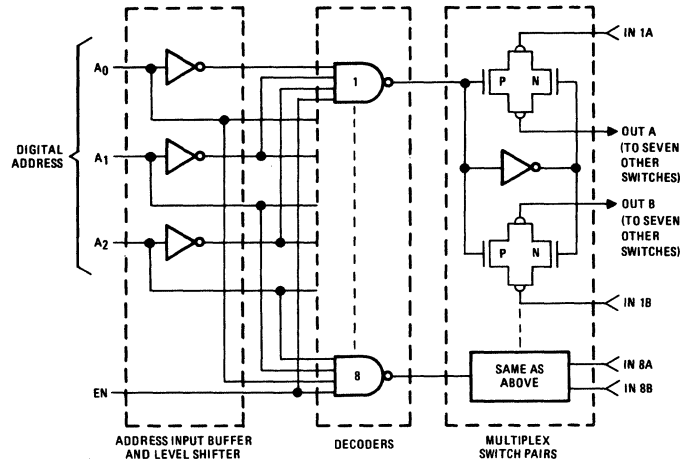
SIMILAR CONNECTION FOR HI-507A

SCHEMATIC DIAGRAMS

FUNCTIONAL BLOCK DIAGRAM HI-506A

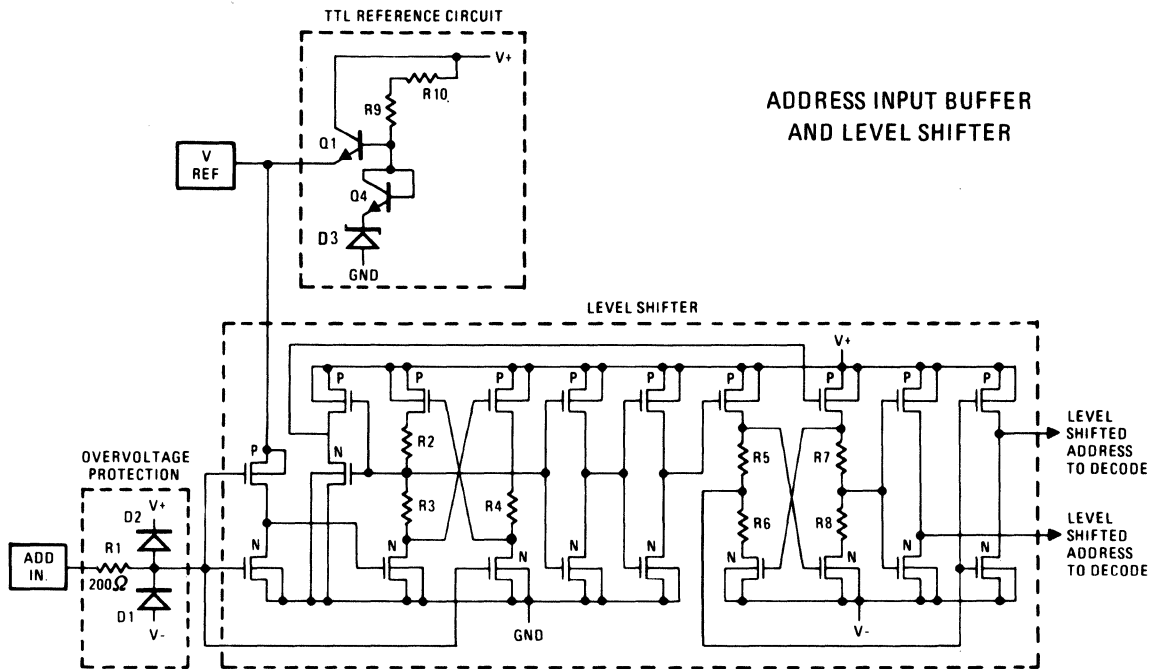


FUNCTIONAL BLOCK DIAGRAM HI-507A

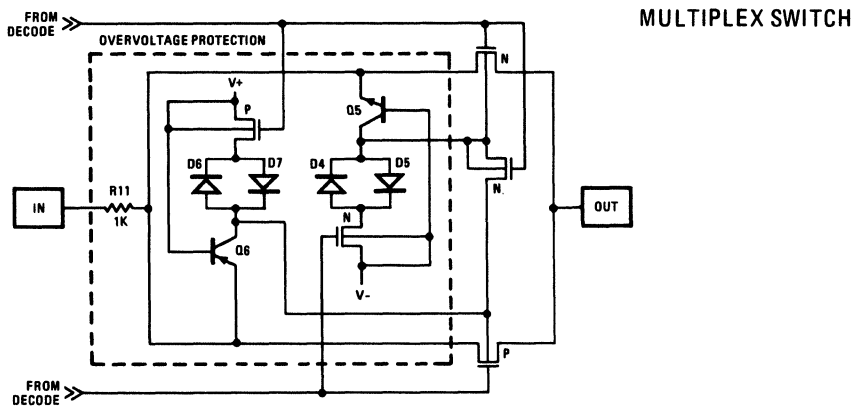
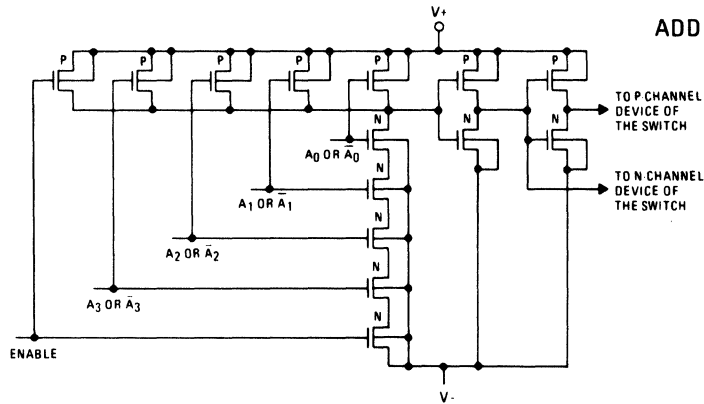


LINEAR

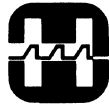
SCHEMATIC DIAGRAMS (continued)



**DELETE A_3 or \bar{A}_3
INPUT FOR HI-507A**



LINEAR



HARRIS
SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HI-508A/509A

8 Channel Analog Multiplexers with Overvoltage Protection

FEATURES

- ANALOG/DIGITAL OVERVOLTAGE PROTECTION
- FAIL SAFE WITH POWER LOSS
- BREAK BEFORE MAKE SWITCHING
- DTL / TTL AND CMOS COMPATIBLE
- ANALOG SIGNAL RANGE $\pm 15V$
- ACCESS TIME 500ns TYP.
- SUPPLY CURRENT AT 1MHz ADDRESS TOGGLE 4mA TYP.
- STANDBY POWER 7.5mW TYP.

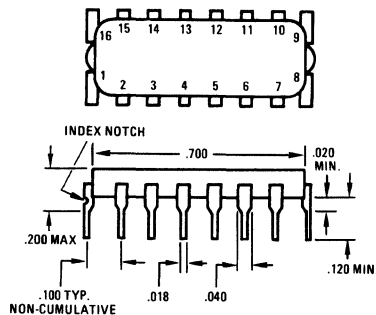
DESCRIPTION

The HI-508A and HI-509A analog multiplexers are constructed with the Harris Dielectric Isolation, Complementary MOS process. Digital and Analog inputs are protected from overvoltage inputs that exceed either supply voltage with no channel interaction. Channel interaction is also eliminated in the event of power loss. The HI-508A is a single-ended 8 channel multiplexer while the HI-509A is a differential 4 channel version. The devices are packaged in a 16 pin dual-in-line package and are available in both military and commercial temperature ranges.

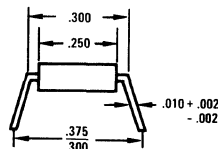
PACKAGE

CODE 1F

16 LEAD D.I.P.

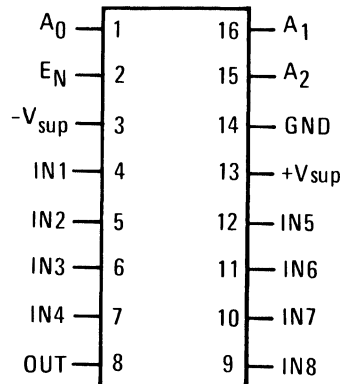


ALL DIMENSIONS IN INCHES.
ALL DIMENSIONS $\pm .010$ UNLESS OTHERWISE SHOWN.



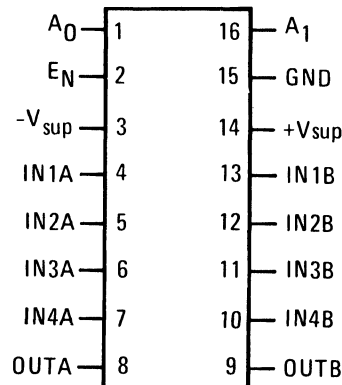
PIN OUT/TRUTH TABLE

HI-508A



A_2	A_1	A_0	E_N	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-509A



A_1	A_0	E_N	ON SWITCH PAIR
X	X	L	NONE
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

LINEAR

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage between Supply Pins 40V

Total Power Dissipation* 725 mW

V_{EN}, V_A , Digital Input Overvoltage:

$$V_A \begin{cases} V_{Supply}(+) +4V \\ V_{Supply}(-) -4V \end{cases}$$

Operating Temperature:

HI-508A/HI-509A-2 -55°C to +125°C

HI-508A/HI-509A-5 0°C to +75°C

Storage Temperature -65°C to +150°C

Analog Input Overvoltage:

$$V_S \begin{cases} V_{Supply}(+) +20V \\ V_{Supply}(-) -20V \end{cases}$$

*Derate 8mW/°C above $t_A = 75^\circ\text{C}$

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified.

Supplies = +15V, -15V; V_{REF} (Pin 13) = Open; V_{AH} (Logic Level High) = +4.0V; V_{AL} (Logic Level Low) = +0.8V

For Test Conditions, consult Performance Characteristics section.

PARAMETER	TEMP.	HI-508A/509A-2			HI-508A/509A-5			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
ANALOG CHANNEL CHARACTERISTICS								
* V_S , Analog Signal Range	Full	-15		+15	-15		+15	V
* R_{ON} , On Resistance (Note 1)	+25°C		1.2	1.5		1.5	1.8	K Ω
	Full		1.5	1.8		1.8	2.0	K Ω
* $I_{S(OFF)}$, Off Input Leakage Current	+25°C		0.03			0.03		nA
	Full			±50			±50	nA
* $I_{D(OFF)}$, Off Output Leakage Current	+25°C		1.0			1.0		nA
	Full			±250			±250	nA
* $I_{D(OFF)}$ with Input Overvoltage Applied (Note 2)	+25°C		4.0			4.0		nA
	Full			2.0				μA
* $I_{D(ON)}$, On Channel Leakage Current	+25°C		0.1			0.1		nA
	Full			±250			±250	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL} , Input Low Threshold	Full			0.8			0.8	V
V_{AH} , Input High Threshold	Full	4.0			4.0			V
* I_A , Input Leakage Current (High or Low)	Full			1.0			1.0	μA
SWITCHING CHARACTERISTICS								
t_A , Access Time	+25°C		0.5	1.0			0.5	μs
t_{OPEN} , Break - Before Make Delay	+25°C		80			80		ns
$t_{ON(EN)}$, Enable Delay (ON)	+25°C		300			300		ns
$t_{OFF(EN)}$, Enable Delay (OFF)	+25°C		300			300		ns
"OFF Isolation" (Note 3)	+25°C		65			65		dB
$C_S(OFF)$, Channel Input Capacitance	+25°C		5			5		pF
$C_D(OFF)$, Channel Output Capacitance	HI-508A	+25°C	25			25		pF
	HI-509A	+25°C	12			12		pF
C_A , Digital Input Capacitance	+25°C		5			5		pF
$C_{DS(OFF)}$, Input to Output Capacitance	+25°C		0.1			0.1		pF
POWER REQUIREMENTS								
P_D , Power Dissipation	Full		7.5			7.5		mW
* I_+ , Current (Note 4)	Full		0.5	2.0		0.5	5.0	mA
* I_- , Current (Note 4)	Full		0.02	1.0		0.02	2.0	mA
* I_+ , Standby (Note 5)	Full		0.5	2.0		0.5	5.0	mA
* I_- , Standby (Note 5)	Full		0.02	1.0		0.02	2.0	mA

NOTES: 1. $V_{OUT} = \pm 10V$, $I_{OUT} = -100 \mu\text{A}$

2. Analog Overvoltage = $\pm 33V$

3. $V_{EN} = 0.8V$, $R_L = 1K$, $C_L = 7pF$, $V_S = 3V$ RMS, $f = 500KHz$

4. $V_{EN} = +4.0V$

5. $V_{EN} = 0.8V$

6. To drive from DTL/TTL Circuits, 1K Ω pull-up resistors to +5.0V supply are recommended

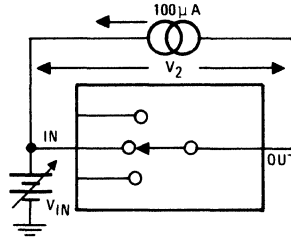
*100% Tested For DASH 8

PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS

(UNLESS OTHERWISE SPECIFIED $T_A = 25^\circ\text{C}$, $V_{\text{SUPPLY}} = \pm 15\text{V}$, $V_{\text{AH}} = +4\text{V}$, $V_{\text{AL}} = 0.8\text{V}$)

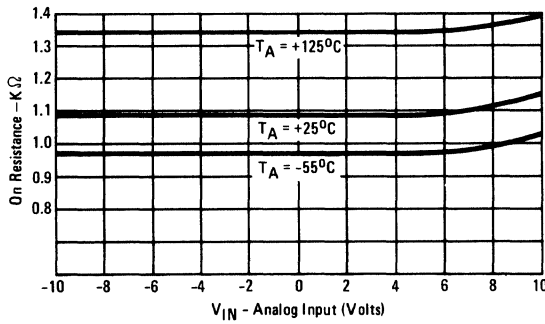
TEST CIRCUIT NO. 1

$$R_{\text{ON}} = \frac{V_2}{100\mu\text{A}}$$

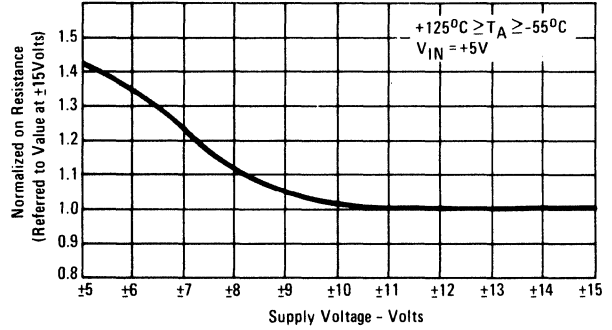


ON RESISTANCE vs. INPUT SIGNAL LEVEL, SUPPLY VOLTAGE

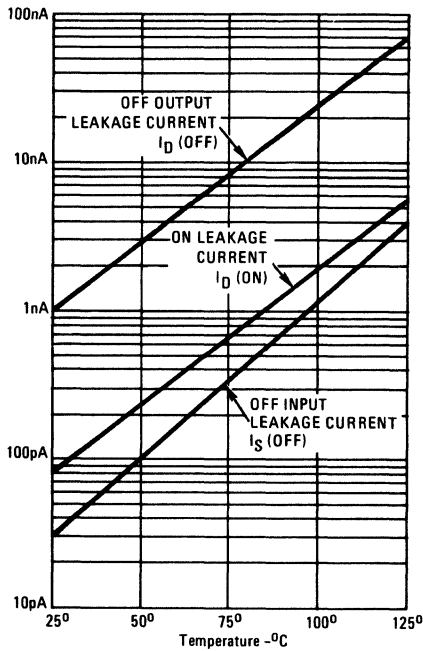
ON RESISTANCE vs. ANALOG INPUT VOLTAGE



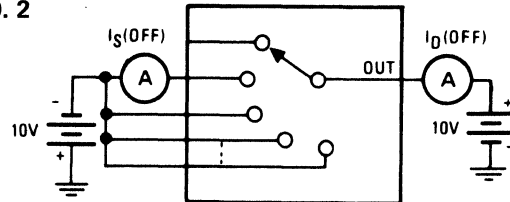
NORMALIZED ON RESISTANCE vs. SUPPLY VOLTAGE



LEAKAGE CURRENT vs. TEMPERATURE



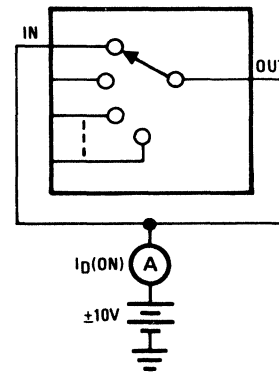
TEST CIRCUIT NO. 2



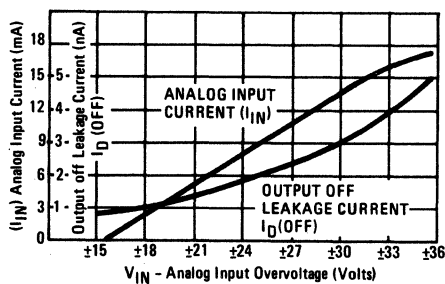
OFF LEAKAGE CURRENT vs. TEMPERATURE

ON LEAKAGE CURRENT vs. TEMPERATURE

TEST CIRCUIT NO. 3

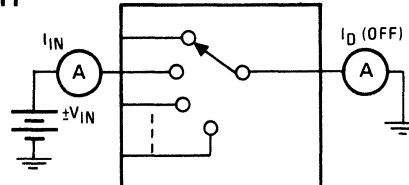


ANALOG INPUT OVERVOLTAGE CHARACTERISTICS

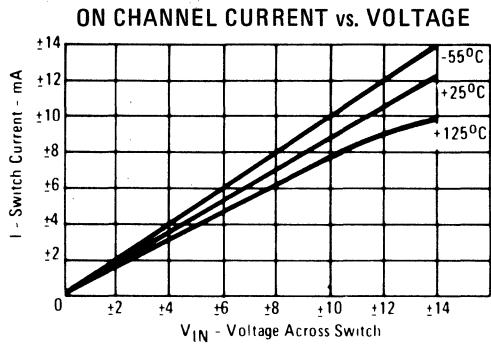


ANALOG INPUT OVERVOLTAGE CHARACTERISTICS

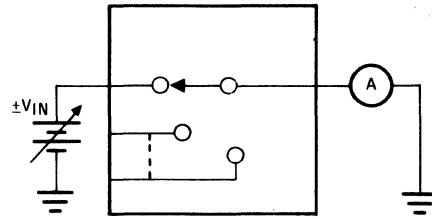
TEST CIRCUIT NO. 4



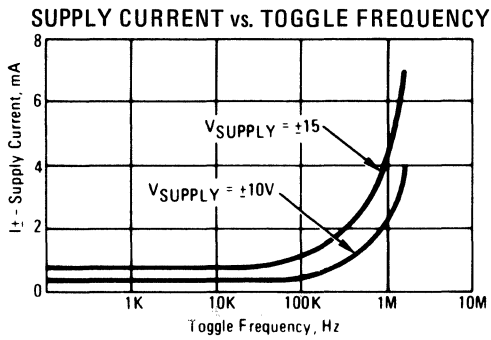
PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (continued)



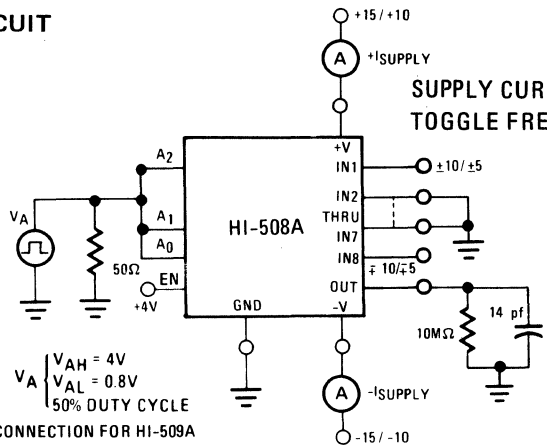
TEST CIRCUIT NO.5



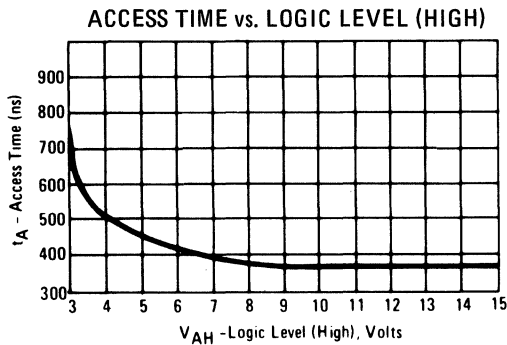
ON CHANNEL CURRENT vs. VOLTAGE



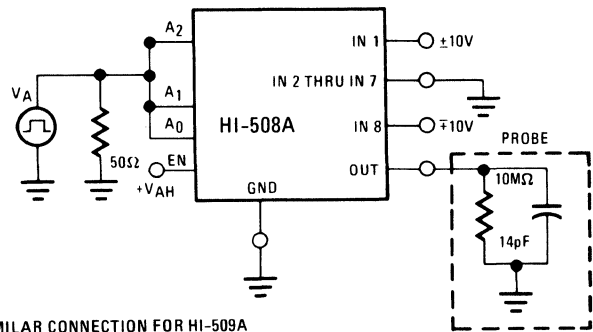
TEST CIRCUIT NO.6



SUPPLY CURRENT vs. TOGGLE FREQUENCY

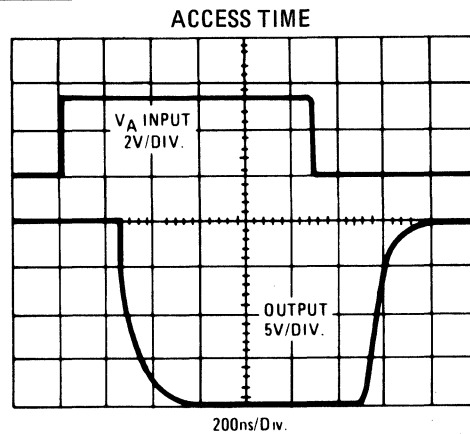
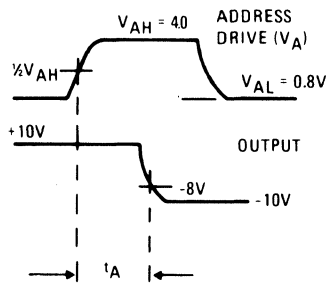


TEST CIRCUIT NO.7



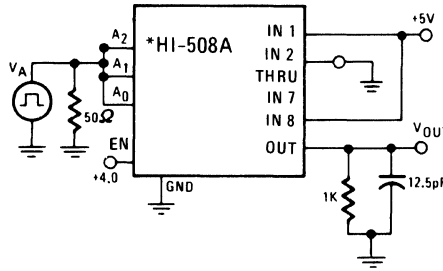
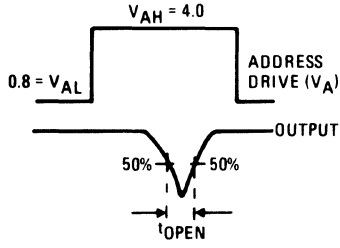
ACCESS TIME vs. LOGIC LEVEL (HIGH)

SWITCHING WAVEFORMS



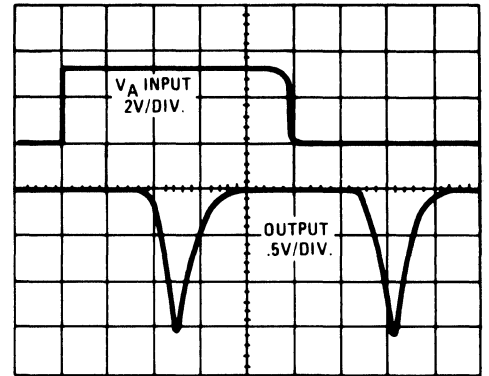
SWITCHING WAVEFORMS (continued)

TEST CIRCUIT NO. 8
BREAK BEFORE MAKE DELAY (t_{OPEN})



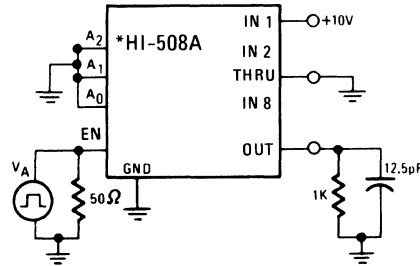
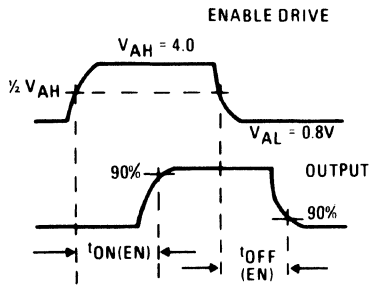
*SIMILAR CONNECTION FOR HI-509A

BREAK BEFORE MAKE DELAY (t_{OPEN})



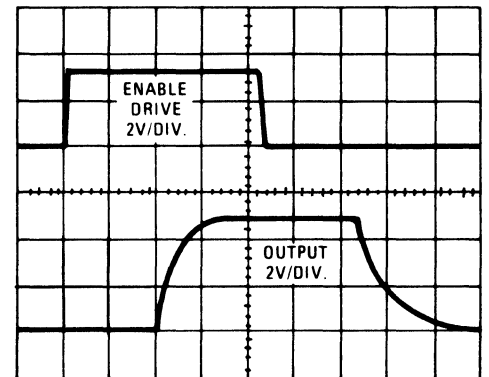
100ns/Div.

TEST CIRCUIT NO. 9
ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)



* SIMILAR CONNECTION FOR HI-509A

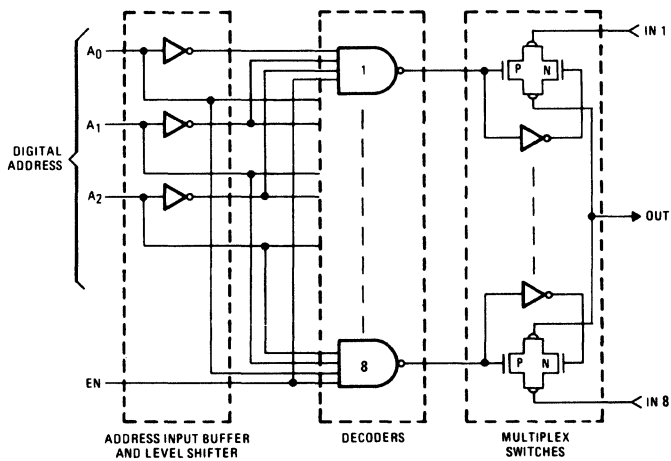
ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)



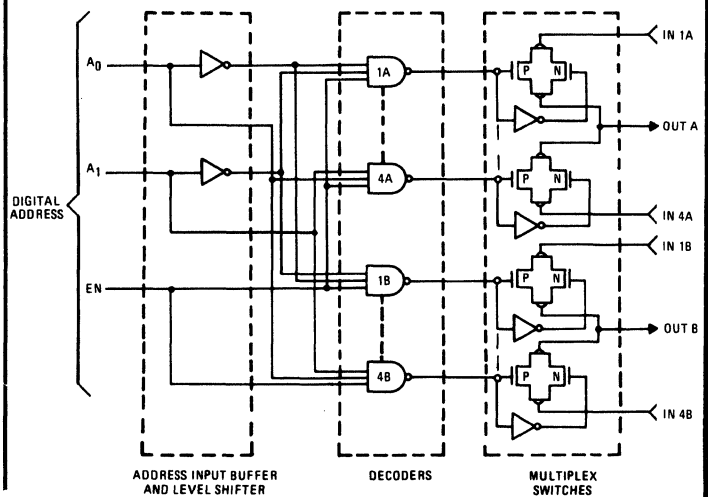
100ns/Div.

SCHEMATIC DIAGRAMS

FUNCTIONAL BLOCK DIAGRAM HI-508A

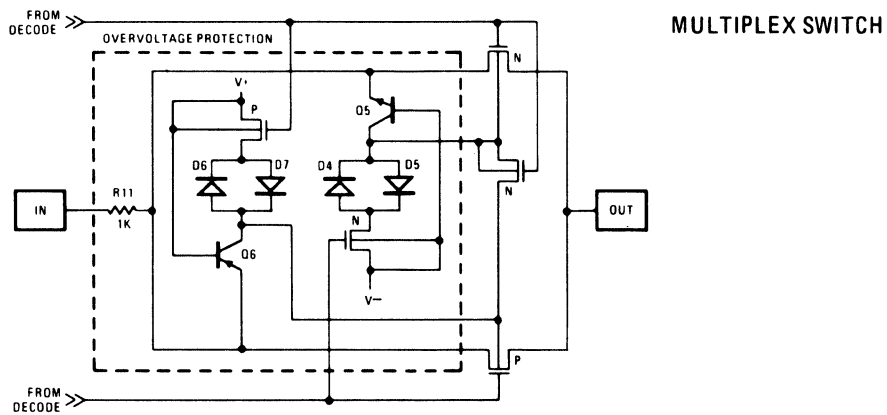
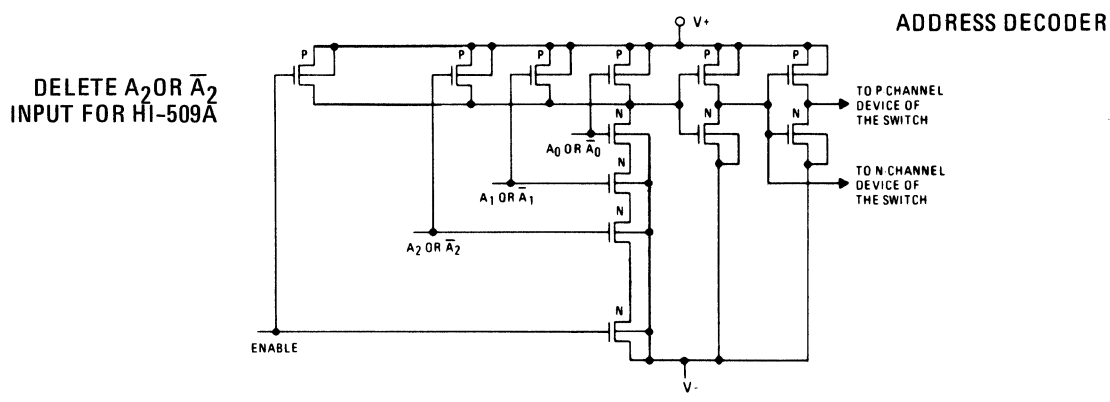
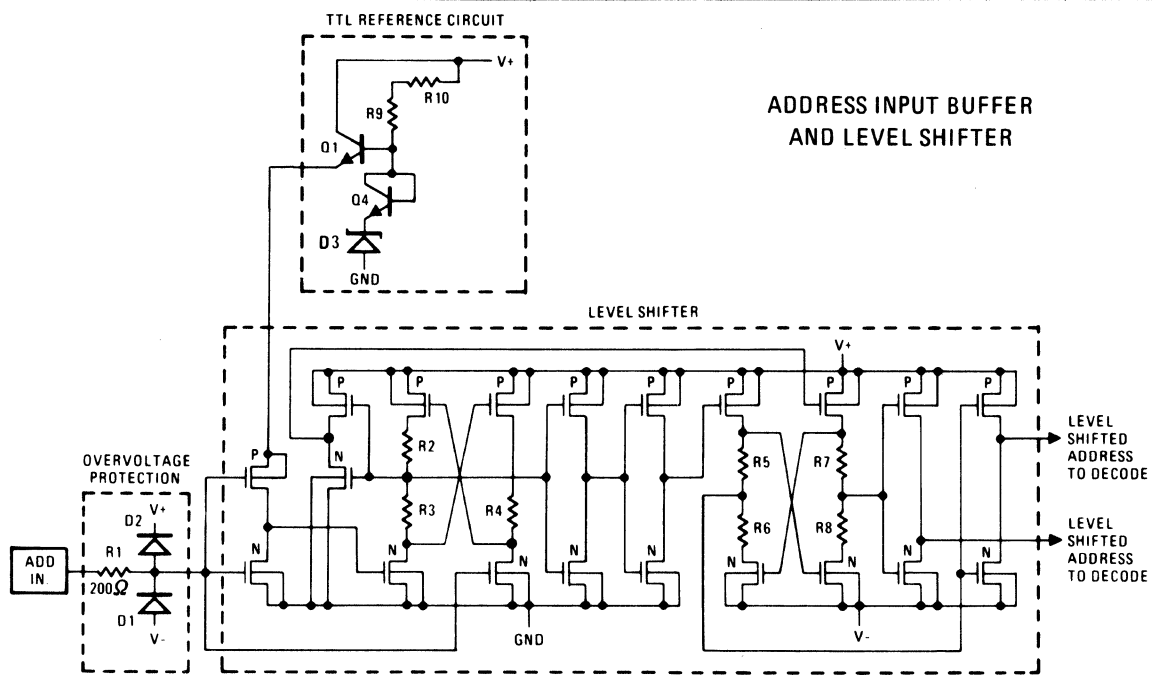


FUNCTIONAL BLOCK DIAGRAM HI-509A

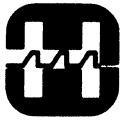


LINEAR

SCHEMATIC DIAGRAMS (continued)



LINEAR



HARRIS
SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HI-1080/HI-1085

8-Bit D to A Converter

High Speed Monolithic

FEATURES

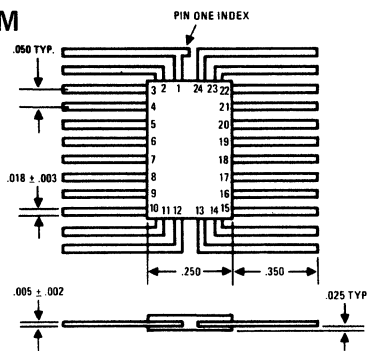
- ACCURACY — (HI-1080) } Guaranteed -55° to $+125^{\circ}\text{C}$
(HI-1085) } or 0° to $+75^{\circ}\text{C}$
- SPEED — 1.5 Microseconds settling to $\frac{1}{2}$ L.S.B.
- VERSATILITY — Unipolar, Bipolar, Offset Operation
Positive or Negative External Reference
Taps Provided for Scale Factor Adjustment
Provision for Cascading Converters
Matched Amplifier Feedback Resistors
Inputs DTL/TTL Compatible
- RELIABILITY — Monolithic Construction
Meets Requirements of MIL-STD-883

GENERAL DESCRIPTION

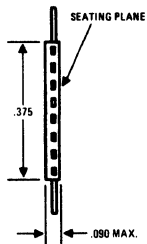
The HI-1080/1085 is a current switching converter complete with a precision thin film R-2R ladder resistor network on a single monolithic chip. It is ideal for general purpose high speed, moderate accuracy digital-analog interfaces. It is particularly suitable as part of a high speed successive approximation or up-down counter type A to D converter.

PACKAGES

CODE 9M

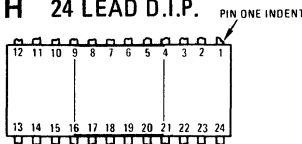


24 LEAD FLAT PACK

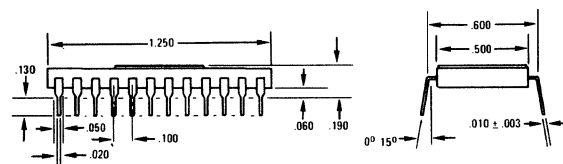


CODE 1H

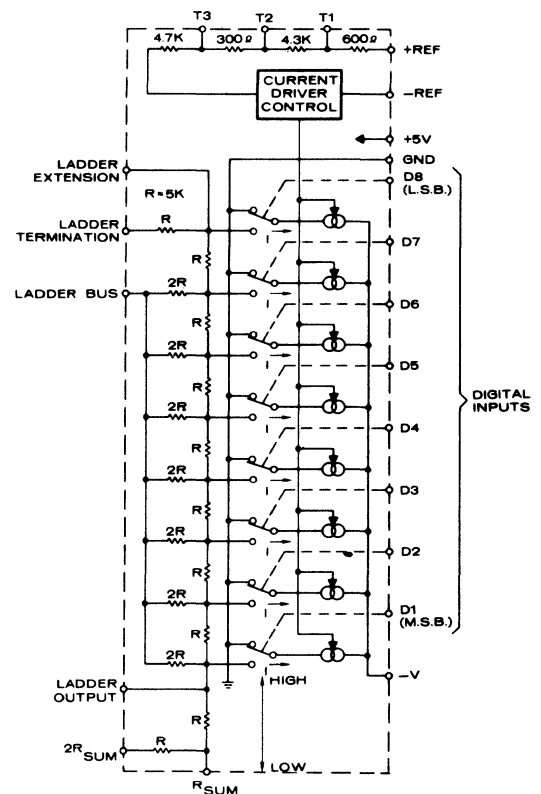
24 LEAD D.I.P.



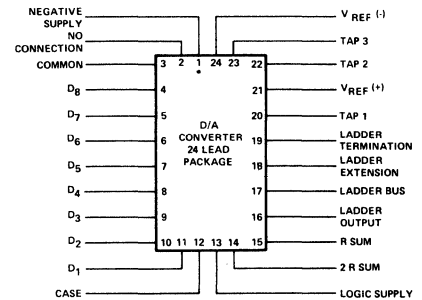
ALL DIMENSIONS ARE IN INCHES.
ALL DIMENSIONS $\pm .010$ UNLESS OTHERWISE SHOWN.



FUNCTIONAL DIAGRAM



PIN CONFIGURATION



LINEAR

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Maximum ratings are limiting values above which permanent circuit damage may occur.

Voltage

V⁺: +8.0V

V⁻: -18.0V

Ladder Common:

±8.0V

I_{REF}: 1.6 mA

Storage Temp:

-65°C ≤ TA ≤ +150°C

Power Dissipation:

450 mW *

Digital Inputs: +5.5V

*Derate at 4mW/°C above 85°C ambient.

ELECTRICAL CHARACTERISTICS

Unless otherwise stated all measurements taken at V⁺ = +5V, V⁻ = -15V
 V_{REF} = +5V, V_{inHigh} = +2.4V, V_{inLow} = +0.4V
 Unipolar, zero reference connection (Figure 3)

	HI-1080 TEMP	LIMITS			UNITS	HI-1085 TEMP	LIMITS			UNITS
		MIN	TYP	MAX			MIN	TYP	MAX	
* Resolution		8			Bits		8			Bits
* Accuracy (Calibrated at 25°C) (Note 1)	+25°C -55°C to +125°C		1/4 1/2	1/2 1	L.S.B.	0°C to +75°C		1/2	1	L.S.B.
* V _{Full Scale} (Note 2) (Uncalibrated)	+25°C	-4.5	-4.98	-5.5	Volts	+25°C	-4.5	-4.98	-5.5	Volts
Power Supply Rejection (Note 3)	-55°C to +125°C	.05	.001		L.S.B. per Volt	0°C to +75°C	.05	.001		L.S.B. per Volt
Settling Time (Note 4)	+25°C		1.5	3.0	μs	+25°C		1.5		μs
Digital Inputs: High Threshold Low Threshold (Note 5) I _{inHigh} I _{inLow} (Note 6)	-55°C to +125°C	0.8		2.0	Volts Volts		0.8		2.0	Volts Volts
			.01	1	μA	0°C to +75°C		.01	1	μA
			-0.7	-1.0	mA			-0.7	-1.0	mA
Supply Current: * I ₊ * I ₋ * I _{REF} (Note 7)	-55°C to +125°C		8 8 0.5	10 10 0.6	mA mA mA	0°C to +75°C		8 8 0.5	10 10 0.6	mA mA mA

NOTES: Test Conditions –

- Any Input Combination
- Inputs all low
- $\Delta V_{OUT} / \Delta V_{SUPPLY}$
V⁺ = +5 ±0.5V
V⁻ = -15 ±3V

- To ±0.2% of full scale after full scale input step

$$R_L > 10 \text{ M}\Omega$$

$$C_L < 5 \text{ pF}$$

- V⁺ = 4.5V

- V_{in} = 2.4 Volts
V⁺ = 5.5V
V_{in} = 0.4 Volts
V⁺ = 5.5V

- V⁺ = +5.0V
V⁻ = -15.0V
V_{REF} = +5.0V
Inputs all low

*100% Tested For DASH 8

PERFORMANCE CURVES

TYPICAL OUTPUT ACCURACY VS. TEMPERATURE

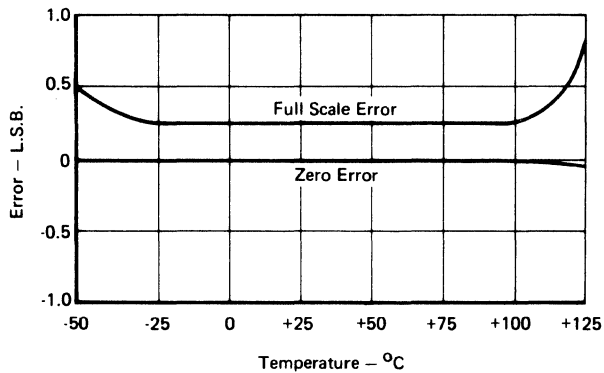


Figure 1

TYPICAL SETTLING TIME

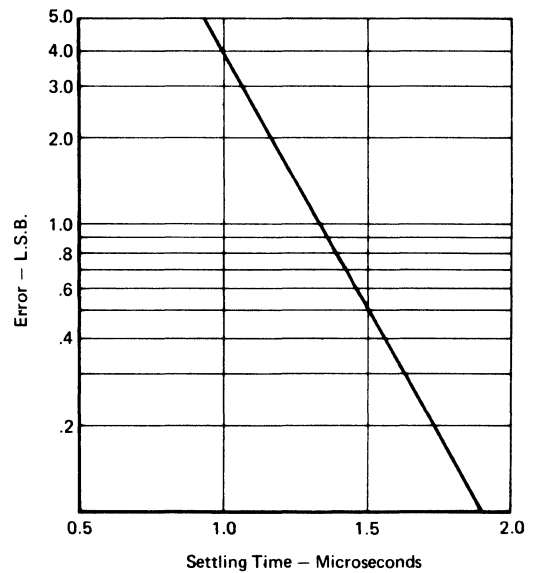
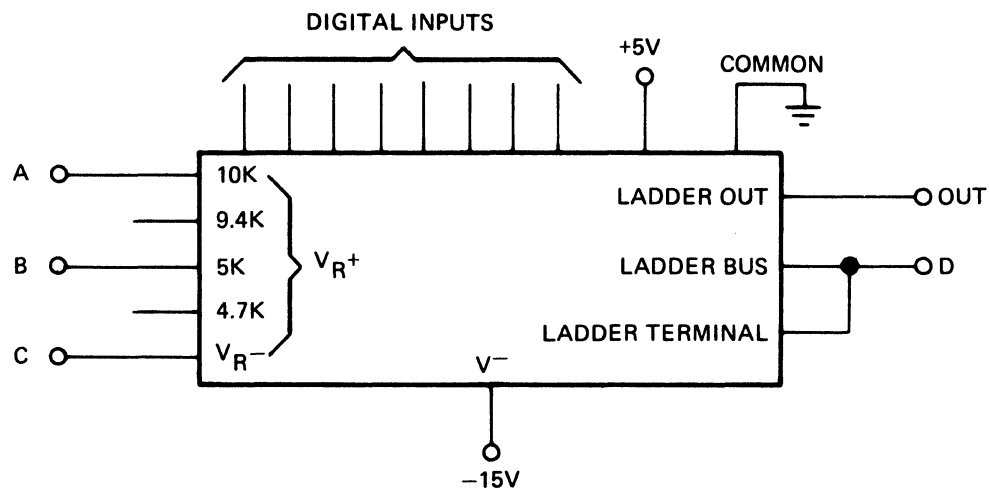


Figure 2

OPERATION MODES

D/A CONVERTER OPERATION MODES



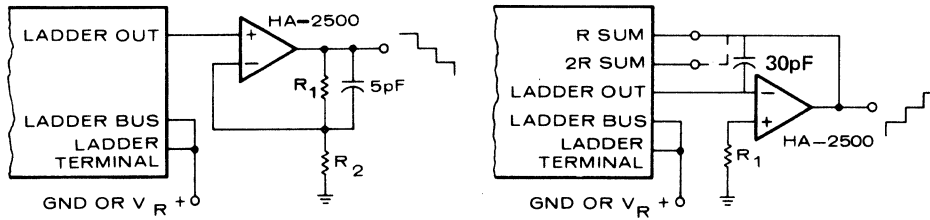
MODE	OUTPUT RANGE INPUTS: ALL HIGH TO ALL LOW	CONNECTIONS			
		A	B	C	D
UNIPOLAR ZERO REFERENCE	0 TO $-V_{R+} - 1 \text{ L.S.B.}$	V_{R+}	N.C.	GND	GND
UNIPOLAR ZERO F.S.	$+V_{R+}$ TO $0 + 1 \text{ L.S.B.}$	V_{R+}	N.C.	GND	V_R
BIPOLAR	$+V_{R+}$ TO $-V_R + 1 \text{ L.S.B.}$	N.C.	V_{R+}	GND	V_{R+}

OPERATING MODES

Figure 3

* Tap 1 or Tap 3 with selected external series resistor may be substituted for points A or B, respectively, for fine adjustment of output range.

BUFFER AMPLIFIER CONNECTION



NON-INVERTING OUTPUT
(MORE NEGATIVE WITH INCREASING
COMPLEMENT OF INPUT NUMBER)

OUTPUT RANGE: SAME AS SHOWN
ON 'CHART 'OPERATING MODE' CHART

$$\text{MULTIPLIED BY } \frac{R_2}{R_1 + R_2}$$

INVERTING OUTPUT
(MORE POSITIVE WITH INCREASING
COMPLEMENT OF INPUT NUMBER)

FULL SCALE OUTPUT	OUTPUT FEEDBACK CONNECTED TO :	R ₁
+4.98V	SUM	2.5K
+9.96V	2R SUM	3.3K

Figure 4

CASCADED UNITS FOR 12 BIT RESOLUTION

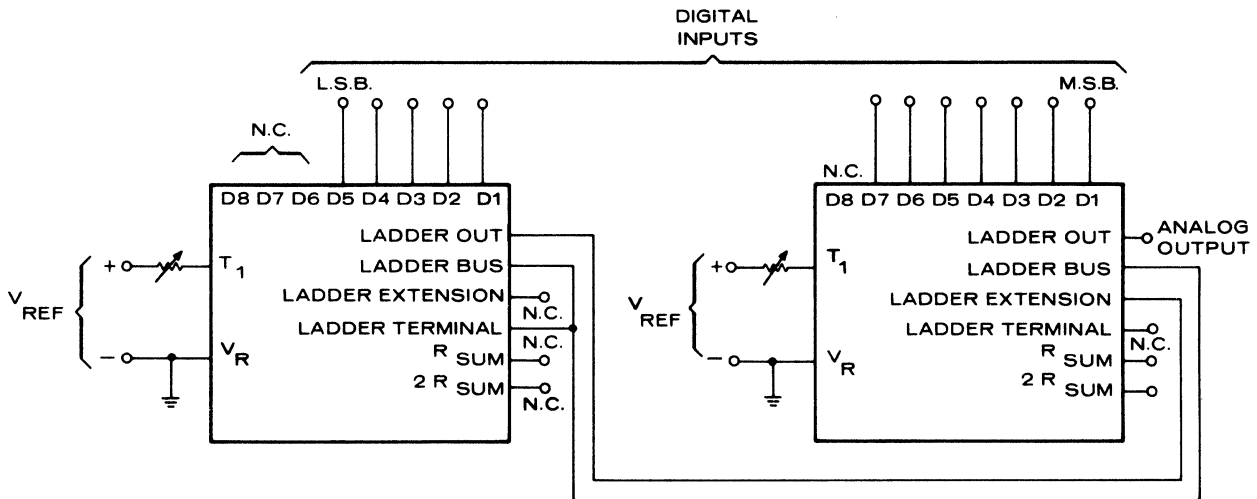


Figure 5



HARRIS
SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HI-1800A

Analog Switch Four-Channel

FEATURES

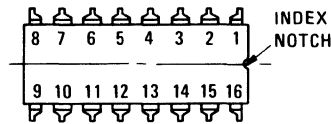
- SIGNAL RANGE ±15V
- "ON" RESISTANCE 125Ω TYP.
- LEAKAGE AT +125°C 40 nA TYP.
- ACCESS TIME 500 ns TYP.
- DTL/TTL COMPATIBLE ADDRESS
- -55°C to +125°C OPERATION

DESCRIPTION

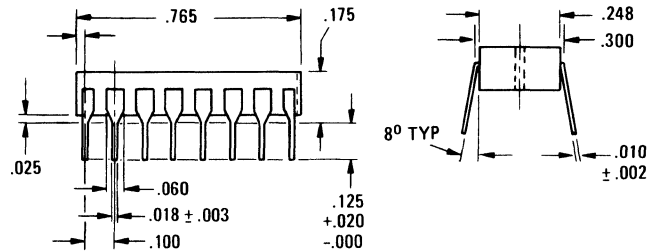
The HI-1800A is a general purpose analog switch which may be used as a signal selector, multiplexer, chopper, or cross-point switch for signals from D.C. to R.F. The configuration is two independent DPST switches with versatile TTL compatible addressing logic which allows connection as two SPDT, or a single DPDT, SPDT, or SPST switch by connection of external jumpers. ON resistance decreases correspondingly when switching elements are connected in parallel. The HI-1800A is fabricated on a single dielectrically isolated chip using complementary N and P channel MOS devices. This unique process produces exceptionally low leakage currents (even at +125°C), constant ON resistance, low power dissipation, and fast switching. The HI-1800A is available in a hermetic 16 pin dual-in-line package.

PACKAGE

CODE 1W 16 LEAD CERAMIC D.I.P.



ALL DIMENSIONS ARE IN INCHES.
ALL DIMENSIONS ±.010 UNLESS OTHERWISE SHOWN.



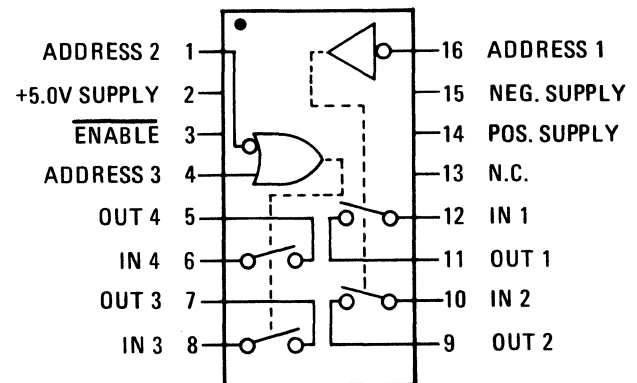
TRUTH TABLE

INPUT ADDRESS				SWITCH CHANNELS			
A1	A2	A3	\overline{EN}	1	2	3	4
L	X	X	L	ON	ON		
H	X	X	L	OFF	OFF		
X	L	X	L			ON	ON
X	X	H	L			ON	ON
X	H	L	L			OFF	OFF
X	X	X	H	OFF	OFF	OFF	OFF

H ≥ +4.0V

L ≤ +0.4V

PIN FUNCTIONS



LINEAR

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage Between Pins 14 and 15	40.0V	Digital Input Voltage	$V_{-Supply}, V_{+Supply}$
Logic Supply Voltage, Pin 2	30.0V	Total Power Dissipation	780 mW (Note 2)
Analog Input Voltage: $V_{+Supply} +2V$ $V_{-Supply} -2V$		Storage Temperature Range	-65°C to +150°C

ELECTRICAL CHARACTERISTICS

Supplies = +15V, -15V, +5.0V

PARAMETER	TEMP.	HI-1800A-2 -55°C to +125°C			HI-1800A-5 0°C to +75°C			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
<u>ANALOG CHANNEL CHARACTERISTICS</u>								
* V_{IN} , Analog Signal Range	Full	-15		+15	-15		+15	V
* R_{ON} , ON Resistance (Note 3)	+25°C Full		125	200 250		125	200 250	Ω Ω
* I_S (OFF), Input Leakage Current	Full		40	100		40	100	nA
* I_D (OFF), Output Leakage Current	Full		40	100		40	100	nA
* I_D (ON), On Channel Leakage Current	Full		40	100		40	100	nA
<u>DIGITAL INPUT CHARACTERISTICS</u>								
V_{IL} , Input Low Threshold	Full			0.4			0.4	V
V_{IH} , Input High Threshold (Note 4)	Full	4.0			4.0			V
* I_{IN} , Input Leakage Current	Full		.01	1		.01	1	μA
<u>SWITCHING CHARACTERISTICS</u>								
t_A , Access Time (Note 5)	+25°C		500			500		ns
Break-Before-Make Delay	+25°C		200			200		ns
C_{IN} , Channel Input Capacitance	+25°C		8			8		pF
C_{OUT} , Channel Output Capacitance	+25°C		8			8		pF
C_D , Digital Input Capacitance	+25°C		5			5		pF
<u>POWER REQUIREMENTS</u>								
P_D , Power Dissipation	Full		10			10		mW
P_{DS} , Standby Power (Note 6)	Full		10			10		mW
* I_{+} , Current Pin 14	Full		0.001	0.5		0.001	1	mA
* I_{-} , Current Pin 15	Full		0.5	1		0.5	2	mA
* I_L , Current Pin 2	Full		0.5	1		0.5	2	mA

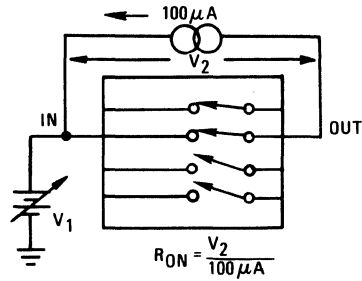
- NOTES: 1. Voltage ratings apply when voltages at all other pins are within their nominal operating ranges.
 2. Derate 9.25 mW/°C above $t_A = +75^\circ C$
 3. $V_{OUT} = \pm 10V$ $I_{OUT} = -100\mu A$.
 4. To drive from DTL/TTL circuits, 1K pullup resistors to +5.0V supply are recommended.

5. Time measured to 90% of final output level;
 $V_{OUT} = -5.0V$ to $+5.0V$, Digital Inputs = $0.4V$ to $+4.0V$.
 6. Voltage at Pin 3, $\overline{ENABLE} \geq +4.0V$.

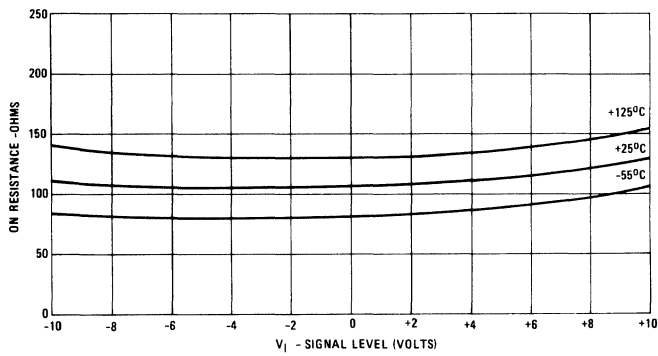
*100% Tested For DASH 8

PERFORMANCE CHARACTERISTICS

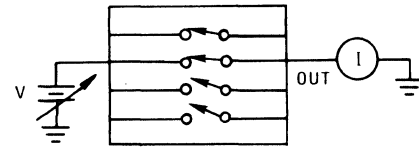
ON RESISTANCE vs ANALOG SIGNAL LEVEL



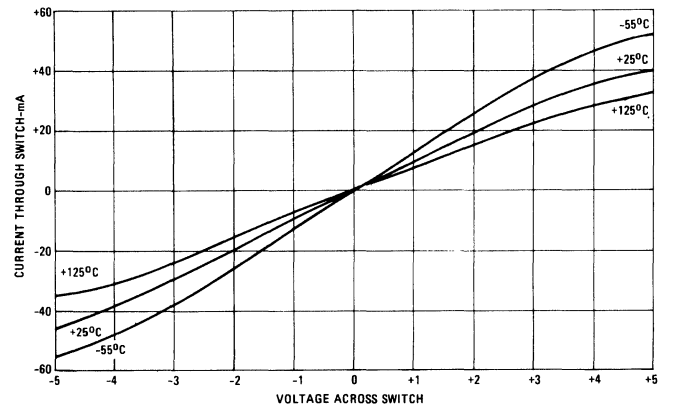
Test Circuit



ON CHANNEL CURRENT vs VOLTAGE

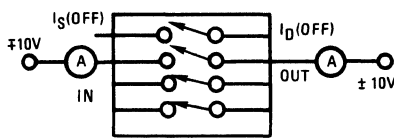


Test Circuit

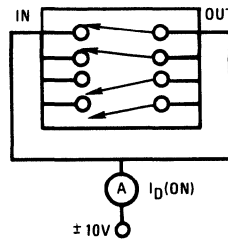


ON/OFF LEAKAGE CURRENTS vs TEMPERATURE

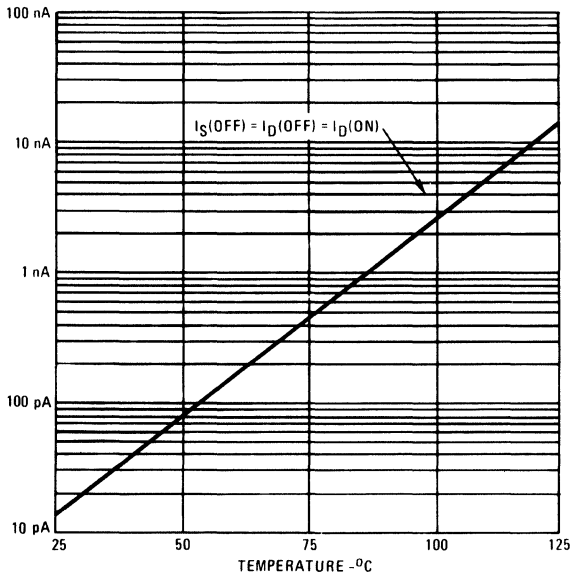
OFF LEAKAGE



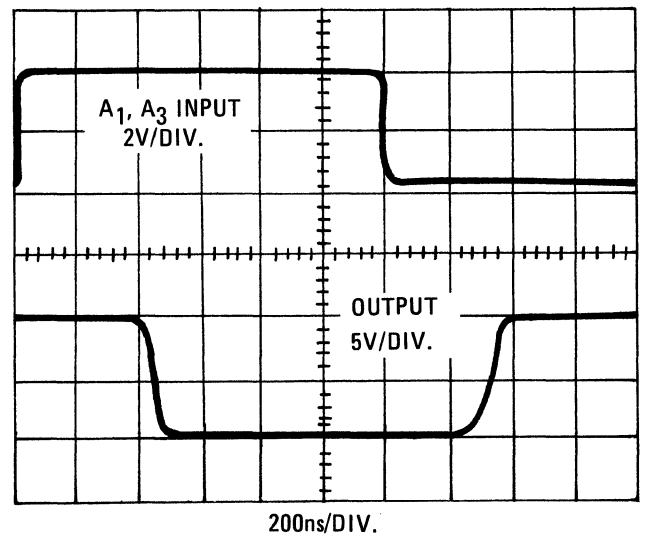
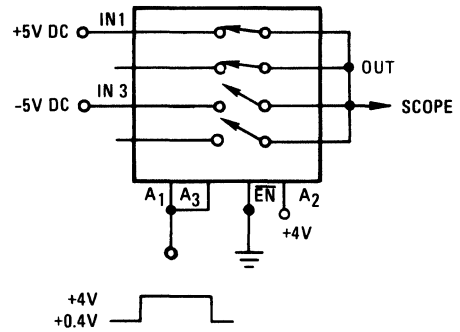
ON LEAKAGE



Test Circuit

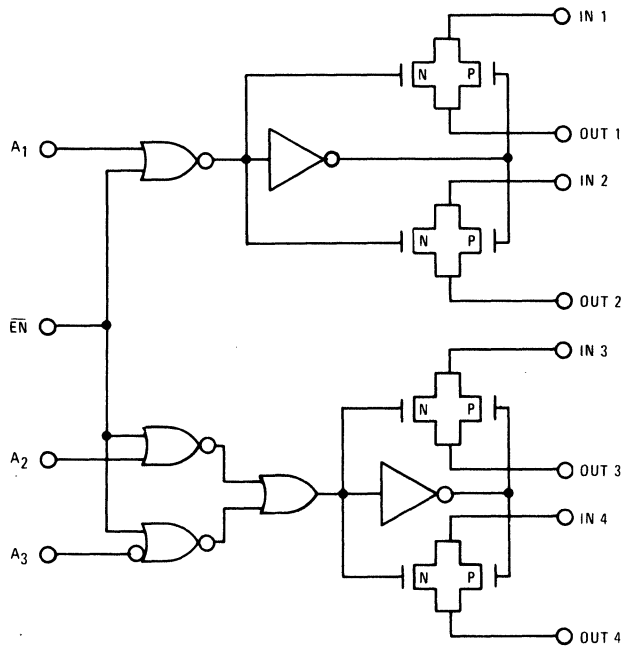


ACCESS TIME

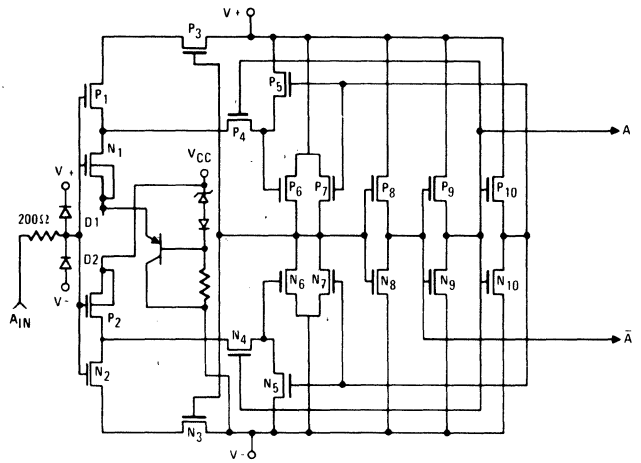


SCHEMATIC DIAGRAM

BLOCK DIAGRAM HI-1800A



ADDRESS INPUT BUFFER

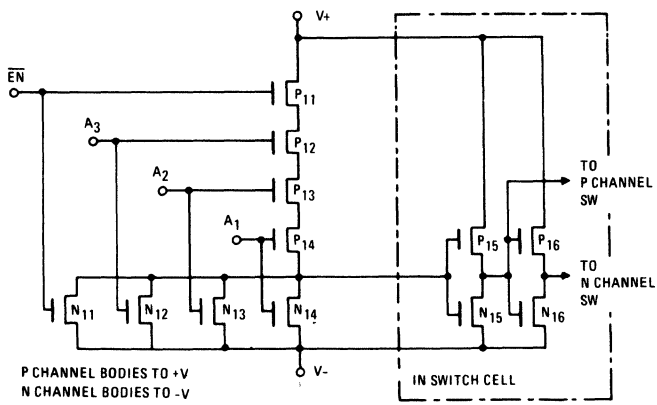


ALL N-CHANNEL BODIES TO V-

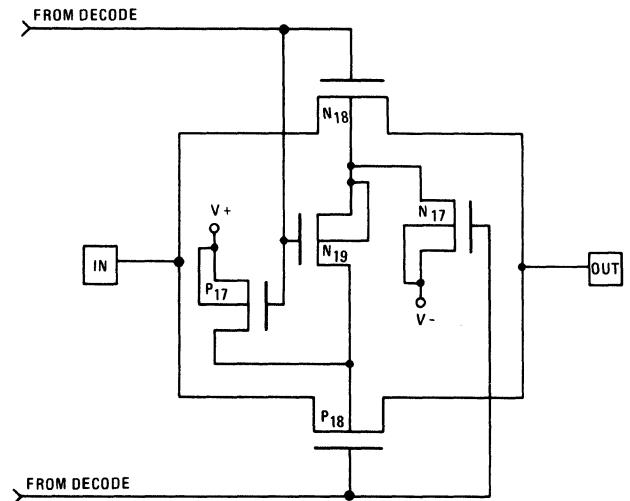
ALL P-CHANNEL BODIES TO V+

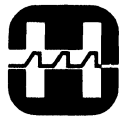
UNLESS OTHERWISE INDICATED

DECODER GATE



MULTIPLEX SWITCH





HARRIS
SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HI-1818A/1828A

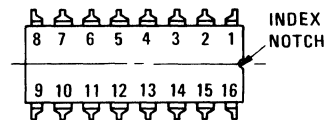
8 Channel Analog Multiplexers

FEATURES

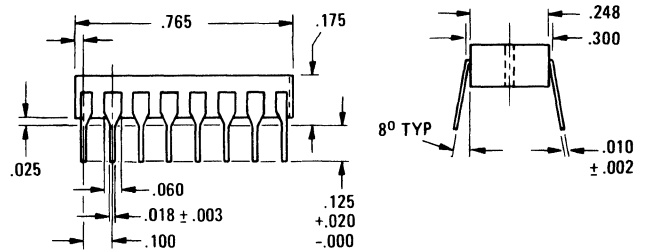
- SIGNAL RANGE $\pm 15V$
- "ON" RESISTANCE 250 Ω TYP.
- INPUT LEAKAGE AT +125°C 20nA TYP.
- ACCESS TIME 350ns TYP.
- POWER CONSUMPTION 5mW TYP.
- DTL/TTL COMPATIBLE ADDRESS
- -55°C TO +125°C OPERATION

PACKAGE

CODE 1W 16 LEAD CERAMIC D.I.P.



ALL DIMENSIONS IN INCHES
ALL DIMENSIONS $\pm .010$
UNLESS OTHERWISE SHOWN.

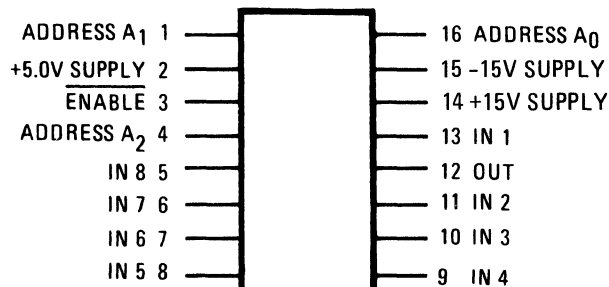


GENERAL DESCRIPTION

The Harris HI-1818A and HI-1828A Analog Multiplexers represent a significant breakthrough in analog switch performance. Vastly superior characteristics are obtained through the unique process of forming complementary MOS transistors in a dielectrically isolated substrate. These devices are useful as multiplexers, signal selectors, and choppers over a wide range of signal levels and switching frequencies. The HI-1818A is a single 8 channel multiplexer while the HI-1828A is a differential 4 channel version. The devices are packaged in a standard 16 pin dual in-line hermetic case and are available in the full military or commercial temperature ranges.

PIN OUT/TRUTH TABLE

HI-1818A

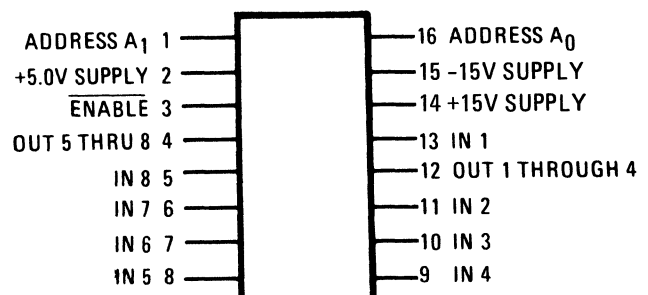


ADDRESS				"ON" CHANNEL
A ₂	A ₁	A ₀	EN	
L	L	L	L	1
L	L	H	L	2
L	H	L	L	3
L	H	H	L	4
H	L	L	L	5
H	L	H	L	6
H	H	L	L	7
H	H	H	L	8
X	X	X	H	NONE

PIN OUT/TRUTH TABLE

HI-1828A

ADDRESS			"ON" CHANNELS
A ₁	A ₀	EN	
L	L	L	1 and 5
L	H	L	2 and 6
H	L	L	3 and 7
H	H	L	4 and 8
X	X	H	NONE



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (NOTE 1)

Supply Voltage Between Pins 14 and 15 40.0V
 Logic Supply Voltage, Pin 2 30.0V
 Analog Input Voltage: V_{Supply}^+ +2V
 V_{Supply}^- -2V

Digital Input Voltage V-Supply to V+ Supply
 Total Power Dissipation (Note 2) 780mW
 Storage Temperature Range -65°C to +150°C

ELECTRICAL CHARACTERISTICS

Supplies = +15V, -15V, +5V

PARAMETER	TEMP.	HI-1818A-2/1828A-2			HI-1818A-5/1828A-5			UNITS
		-55°C to +125°C			0°C to +75°C			
ANALOG CHANNEL CHARACTERISTICS								
* V_{IN} , Analog Signal Range	Full	-15		+15	-15		+15	V
* R_{ON} , ON Resistance (Note 3)	+25°C		250	400		250	400	Ω
	Full		300	500		300	500	Ω
* I_S (OFF), Input Leakage Current	Full		20	50		20	50	nA
* I_D (ON), On Channel Leakage (HI-1818A) Current (HI-1828A)	Full		100	250		100	250	nA
	Full		50	125		50	125	nA
* I_D (OFF) Output Leakage Current (HI-1818A) (HI-1828A)	Full		100	250		100	250	nA
	Full		50	125		50	125	nA
DIGITAL INPUT CHARACTERISTICS								
V_{IL} , Input Low Threshold	Full			0.4			0.4	V
V_{IH} , Input High Threshold (Note 4)	Full	4.0			4.0			V
* I_{IN} , Input Leakage Current	Full		.01	1		.01	1	μ A
SWITCHING CHARACTERISTICS								
T_S , Access Time (Note 5)	+25°C		350			350		ns
Break-Before-Make Delay	+25°C		100			100		ns
C_{IN} , Channel Input Capacitance	+25°C		4			4		pF
C_{OUT} , Channel Output Capacitance (HI-1818A) (HI-1828A)	+25°C		20			20		pF
	+25°C		10			10		pF
C_D , Digital Input Capacitance	+25°C		5			5		pF
POWER REQUIREMENTS								
P_D , Power Dissipation	Full		5			5		mW
P_{DS} , Standby Power (Note 6)	Full		5			5		mW
* I_+ , Current Pin 14	Full		0.1	0.5		0.1	1	mA
* I_- , Current Pin 15	Full		0.3	1		0.3	2	mA
* I_L , Current Pin 2	Full		0.3	1		0.3	2	mA

NOTES: 1. Voltage ratings apply when voltages at all other pines are within their nominal operating ranges.

2. Derate 9.25 mW/°C above 75°C

3. $V_{OUT} = \pm 10V$ $I_{OUT} = -100\mu A$

4. To drive from DTL/TTL circuits, 1K Ω pullup resistors to +5.0V supply are recommended.

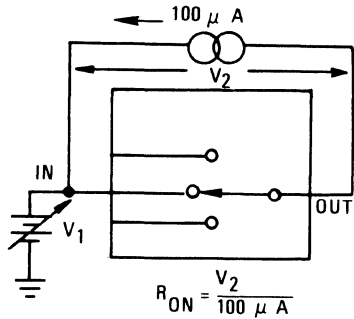
5. Time measured to 90% of final output level;
 $V_{OUT} = -5.0V$ to +5.0V, Digital Inputs = 0V to +4.0V.

6. Voltage at Pin 3, ENABLE = +4.0V.

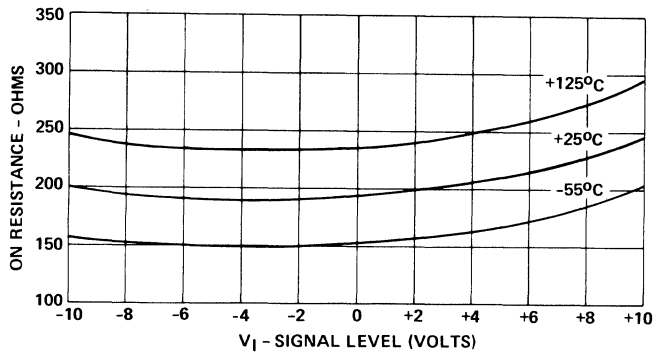
*100% Tested For DASH 8

PERFORMANCE CHARACTERISTICS

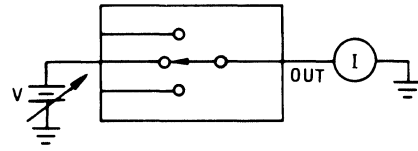
ON RESISTANCE vs ANALOG SIGNAL LEVEL



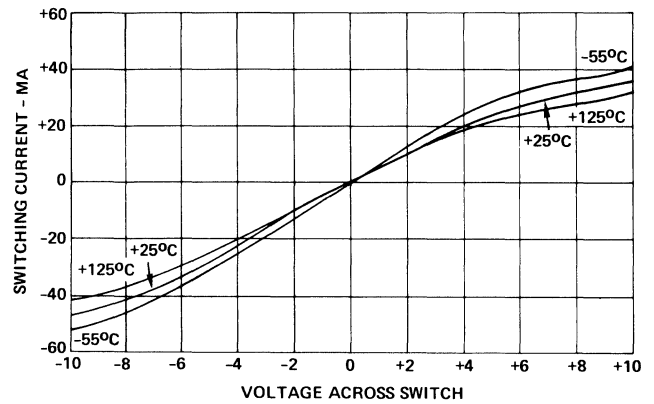
Test Circuit



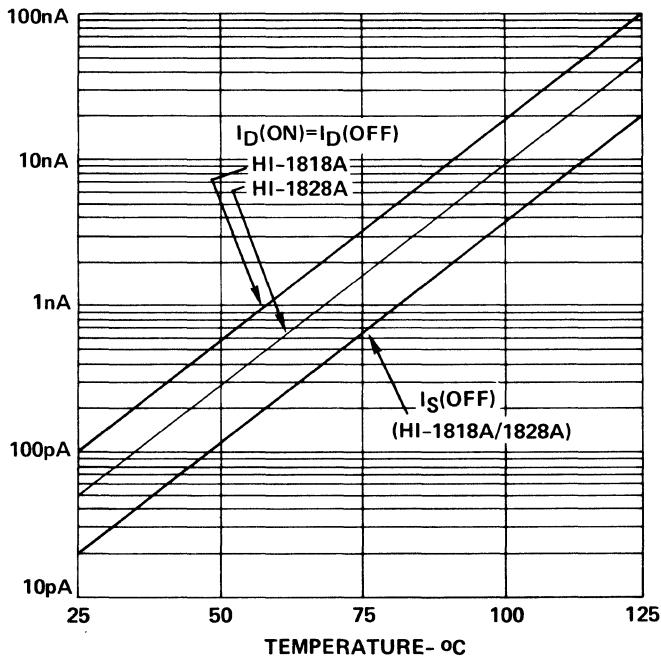
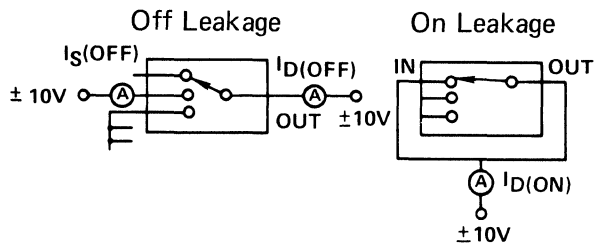
ON CHANNEL CURRENT vs VOLTAGE



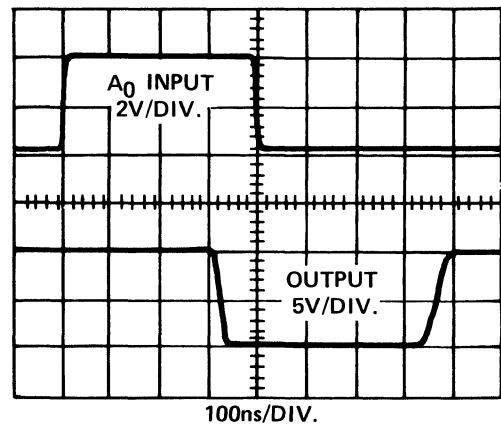
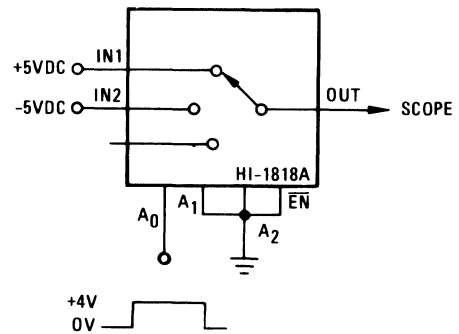
Test Circuit



ON/OFF LEAKAGE CURRENTS vs TEMPERATURE



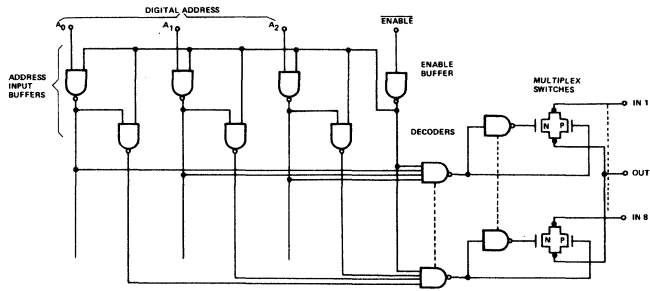
ACCESS TIME



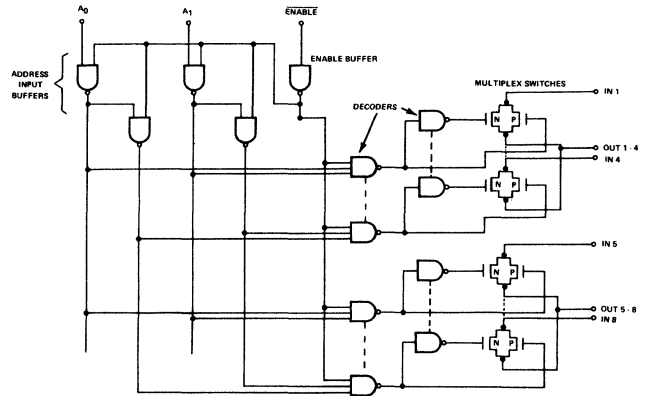
LINEAR

SCHEMATIC DIAGRAM

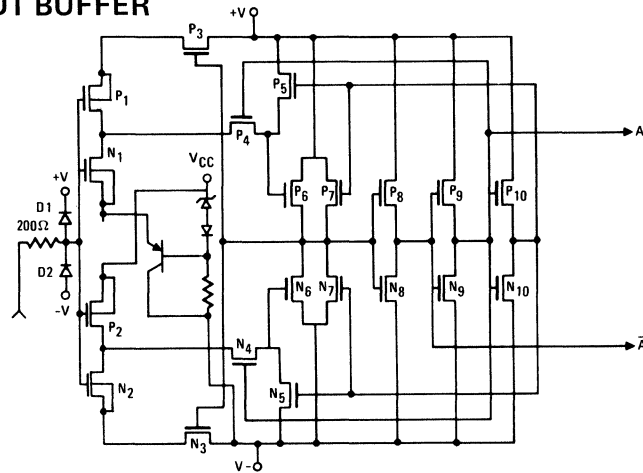
BLOCK DIAGRAM HI-1818A



BLOCK DIAGRAM HI-1828A

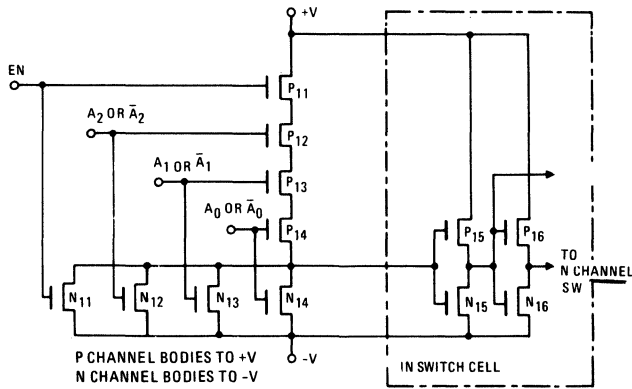


ADDRESS INPUT BUFFER



ALL N-CHANNEL BODIES TO V-
ALL P-CHANNEL BODIES TO V+ UNLESS OTHERWISE INDICATED.

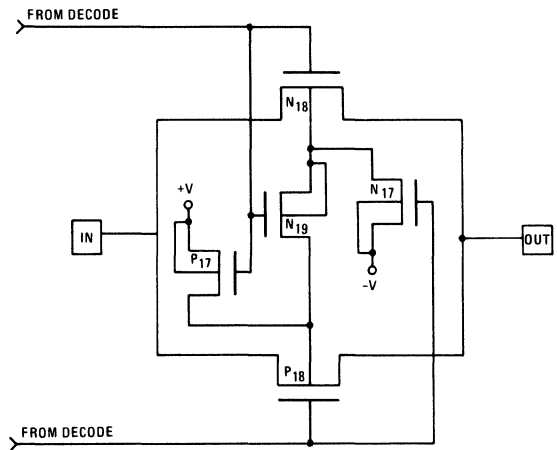
DECODER GATE



P CHANNEL BODIES TO +V
N CHANNEL BODIES TO -V

A₂ OR \bar{A}_2 NOT USED FOR HI-1828A

MULTIPLEX SWITCH





HI-5040 thru HI-5051 HI-5046A and HI-5047A

CMOS Analog Switches

FEATURES

- WIDE ANALOG SIGNAL RANGE ±15V
- LOW "ON" RESISTANCE (TYP) 25Ω
- HIGH CURRENT CAPABILITY (TYP) 80mA
- BREAK-BEFORE-MAKE SWITCHING
- TURN-ON TIME (TYP) 370nS
- TURN-OFF TIME (TYP) 280nS
- NO LATCH-UP
- INPUT MOS GATES ARE PROTECTED FROM ELECTROSTATIC DISCHARGE
- DTL, TTL, CMOS, PMOS COMPATIBLE

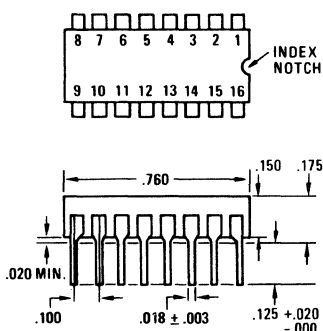
DESCRIPTION

This family of CMOS ANALOG SWITCHES offers high performance at analog levels up to the supply rails. Low leakages, low "ON" resistance and high "OFF ISOLATION" characteristics are achieved using the latch-free, high reliability, Harris Dielectric Isolation process. These monolithic chips incorporate bipolar with MOS devices for minimizing power consumption when CMOS logic levels are used. The HI-5040 series replaces the IH-5040 family and is functionally compatible to the DG 180/190 family. The HI-5046A/5047A are proprietary 30 ohm versions of the HI-5046/5047. All are available in both commercial and military temperature ranges.

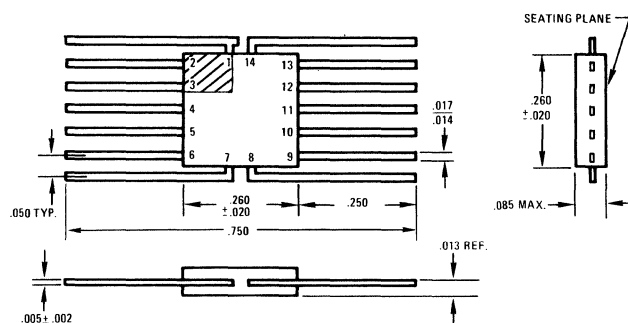
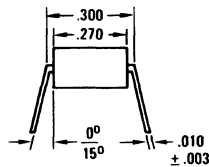
PACKAGES

CODE 1D 16 LEAD CERAMIC D.I.P.

CODE 9H 14 LEAD FLAT PACK (TO-86)

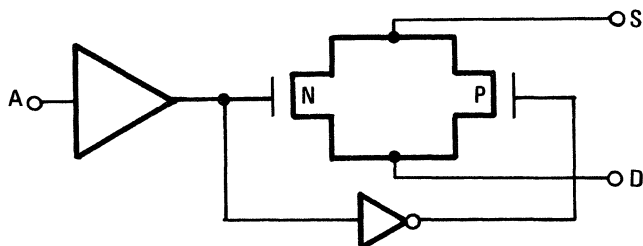


ALL DIMENSIONS IN INCHES
ALL DIMENSIONS ±.010 UNLESS OTHERWISE SHOWN.



FUNCTIONAL DIAGRAM

TYPICAL SWITCH



FUNCTIONAL DESCRIPTION

PART NUMBER	TYPE	RQJN
HI-5040	SPST	75Ω
HI-5041	DUAL SPST	75Ω
HI-5042	SPDT	75Ω
HI-5043	DUAL SPDT	75Ω
HI-5044	DPST	75Ω
HI-5045	DUAL DPST	75Ω
HI-5046	DPDT	75Ω
HI-5046A	DPDT	30Ω
HI-5047	4PST	75Ω
HI-5047A	4PST	30Ω
HI-5048	DUAL SPST	30Ω
HI-5049	DUAL DPST	30Ω
HI-5050	SPDT	30Ω
HI-5051	DUAL SPDT	30Ω

LINEAR

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V^+ - V^-$)	36V	Analog Current (S to D)	80mA
V_R to Ground	V^+, V^-	Total Power Dissipation*	450mW
Digital and Analog Input Voltage	$V^+ +4V$ $V^- -4V$	Operating Temperature	
		HI-50XX-2	-55°C to +125°C
		HI-50XX-5	0°C to +75°C
		Storage Temperature	-65°C to +150°C

*Derate 6mW/°C above $T_A = 75^\circ\text{C}$

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified

Supplies = +15V, -15V; $V_R = 0V$; V_{AH} (Logic Level High) = 3.0V; V_{AL} (Logic Level Low) = +0.8V, $V_L = +5V$

For Test Conditions, consult Performance Characteristics

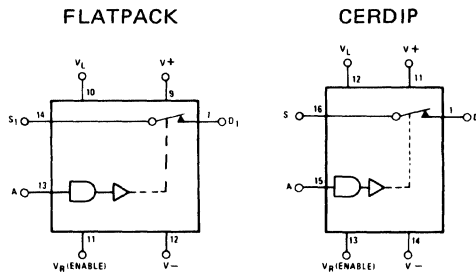
PARAMETER	TEMP	-55°C to +125°C			0°C to +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG SWITCH CHARACTERISTICS								
Analog Signal Range	Full	-15		+15	-15		+15	V
R_{on} , "ON" Resistance (Note 1a)	+25°C		50			50		Ω
	Full			75			75	Ω
R_{on} , "ON" Resistance (Note 1b)	+25°C		25			25		Ω
	Full			50			50	Ω
R_{on} , Channel-to-Channel Match (Note 1a)	+25°C		2			2		Ω
R_{on} , Channel-to-Channel Match (Note 1b)	+25°C		1			1		Ω
$I_{S(OFF)}$ = $I_{D(OFF)}$, Off Input or Output Leakage Current	+25°C		0.8			0.8		nA
	Full		100	500		100	500	nA
$I_{D(ON)}$, On Leakage Current	+25°C		0.01			0.01		nA
	Full		2	500		2	500	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL} , Input Low Threshold	Full			0.8			0.8	V
V_{AH} , Input High Threshold	Full	3.0			3.0			V
I_A , Input Leakage Current (High or Low)	Full		.01	1.0		.01	1.0	μA
SWITCHING CHARACTERISTICS								
t_{on} , Switch "ON" Time	+25°C		370	1000		370		ns
t_{off} , Switch "OFF" Time	+25°C		280	500		280		ns
Charge Injection (Note 2)	+25°C		5	20		5		mV
"OFF Isolation" (Note 3)	+25°C	75	80			80		dB
"Crosstalk" (Note 3)	+25°C	80	88			88		dB
$C_{S(OFF)}$, Input Switch Capacitance	+25°C		11			11		pF
$C_{D(OFF)}$, } Output Switch Capacitance	+25°C		11			11		pF
$C_{D(ON)}$, }	+25°C		22			22		pF
C_A , Digital Input Capacitance	+25°C		5			5		pF
$C_{DS(OFF)}$, Drain-To-Source Capacitance	+25°C		0.5			0.5		pF
POWER REQUIREMENTS								
P_D , Quiescent Power Dissipation	+25°C		1.5			1.5		mW
I^+ , +15V Quiescent Current	Full			0.3			0.5	mA
I^- , -15V Quiescent Current	Full			0.3			0.5	mA
I_L , +5V Quiescent Current	Full			0.3			0.5	mA
I_R , Gnd Quiescent Current	Full			0.3			0.5	mA

- NOTES: 1. $V_{OUT} = \pm 10V$, $I_{OUT} = 1mA$
a) For HI-5040 thru HI-5047
b) For HI-5048 thru HI-5051, HI-5046A/5047A
2. $V_{IN} = 0V$, $C_L = 10,000pF$
3. $R_L = 100\Omega$, $f = 100\text{KHz}$, $V_{IN} = 2V_{pp}$, $C_L = 5pF$

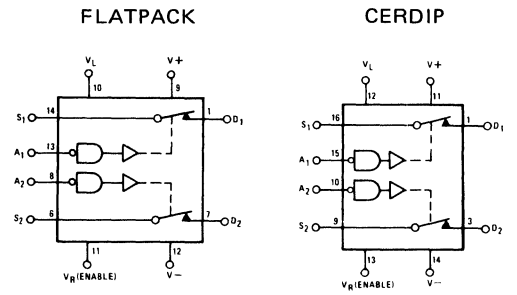
SWITCH FUNCTIONS

SWITCH STATES ARE FOR LOGIC "1" INPUT

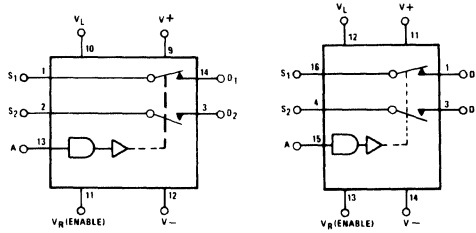
SPST
HI-5040 (75Ω)



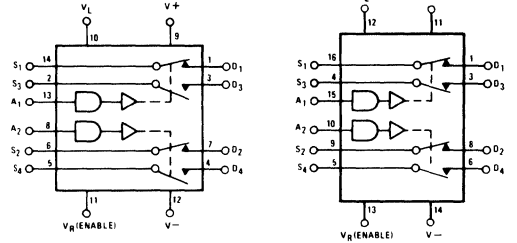
DUAL SPST
HI-5041 (75Ω)



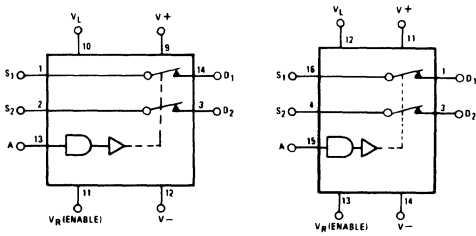
SPDT
HI-5042 (75Ω)



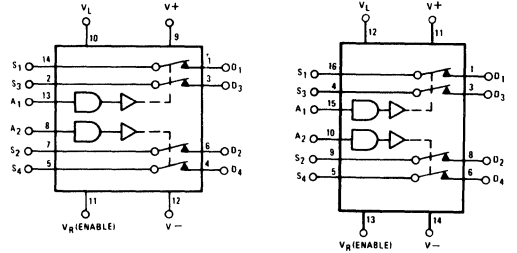
DUAL SPDT
HI-5043 (75Ω)



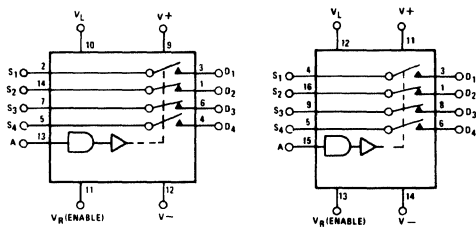
DPST
HI-5044 (75Ω)



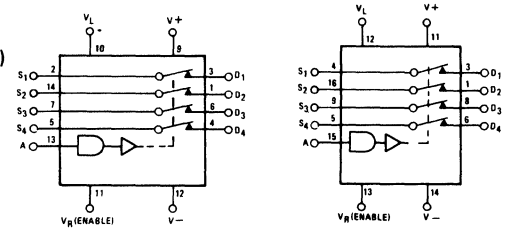
DUAL DPST
HI-5045 (75Ω)



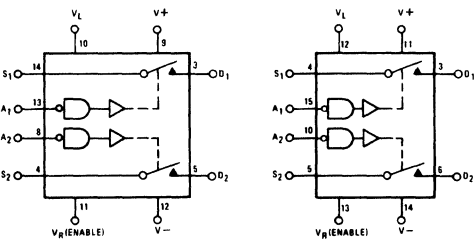
DPDT
HI-5046 (75Ω)
HI-5046A (30Ω)



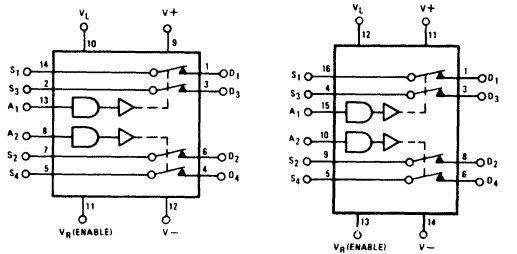
4PST
HI-5047 (75Ω)
HI-5047A (30Ω)



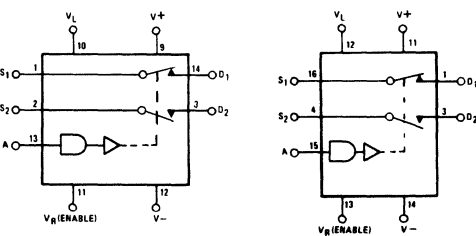
DUAL SPST
HI-5048 (30Ω)



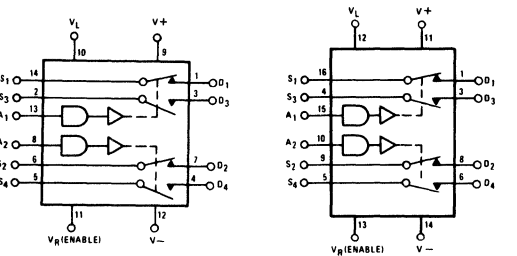
DUAL DPST
HI-5049 (30Ω)



SPDT
HI-5050 (30Ω)



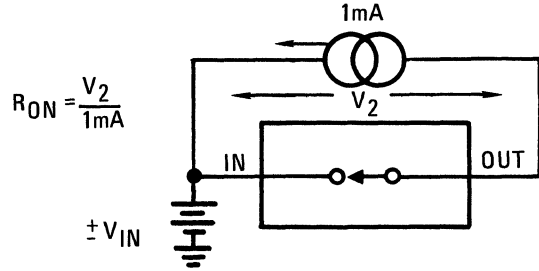
DUAL SPDT
HI-5051 (30Ω)



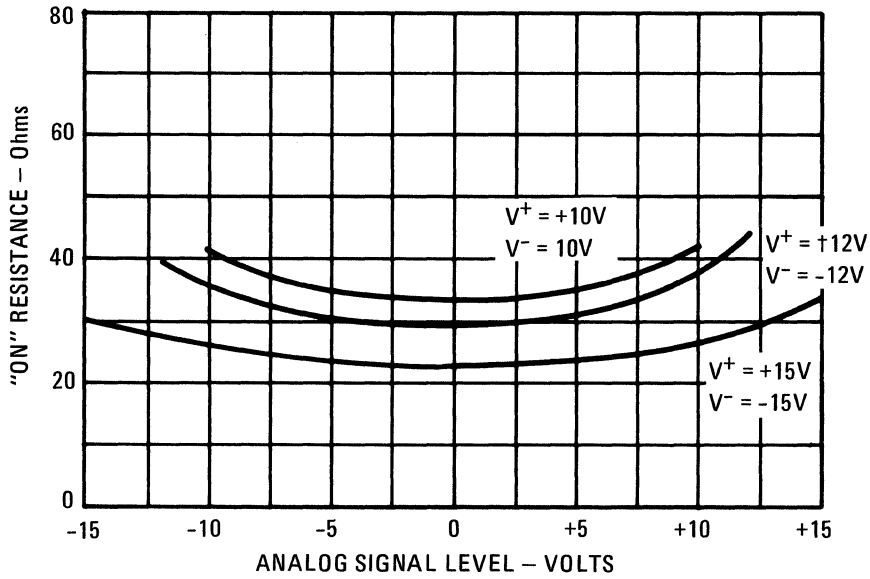
PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS

(UNLESS OTHERWISE SPECIFIED $T_A = 25^{\circ}\text{C}$, $V^+ = +15\text{V}$, $V^- = -15\text{V}$, $V_L = +5\text{V}$, $V_R = 0\text{V}$, $V_{AH} = 3.0\text{V}$ and $V_{AL} = 0.8\text{V}$)

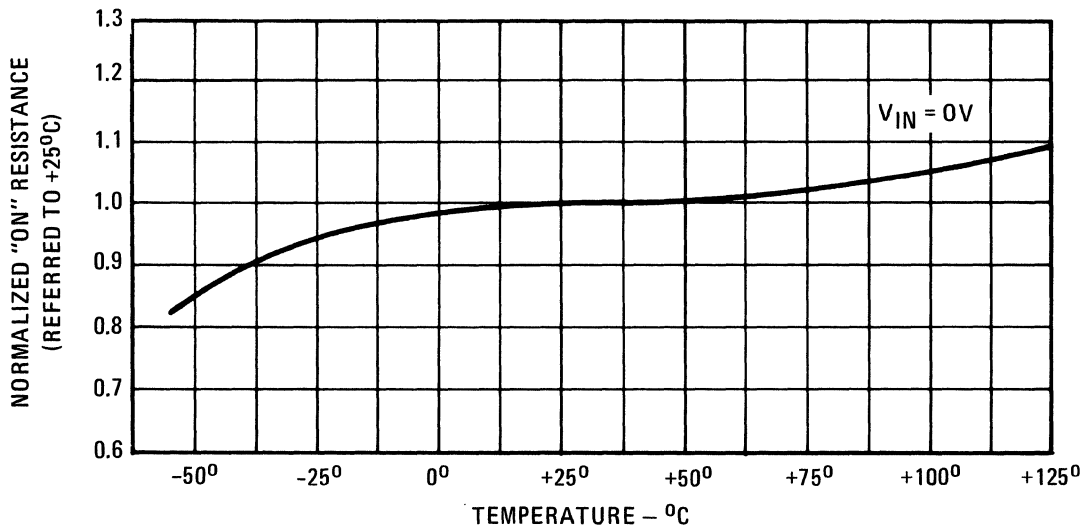
ON RESISTANCE vs. ANALOG SIGNAL LEVEL,
SUPPLY VOLTAGE AND TEMPERATURE



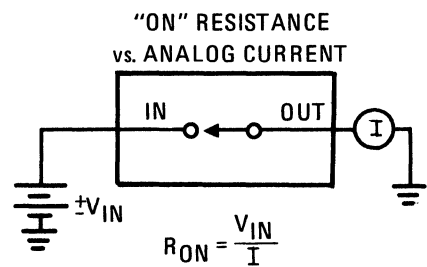
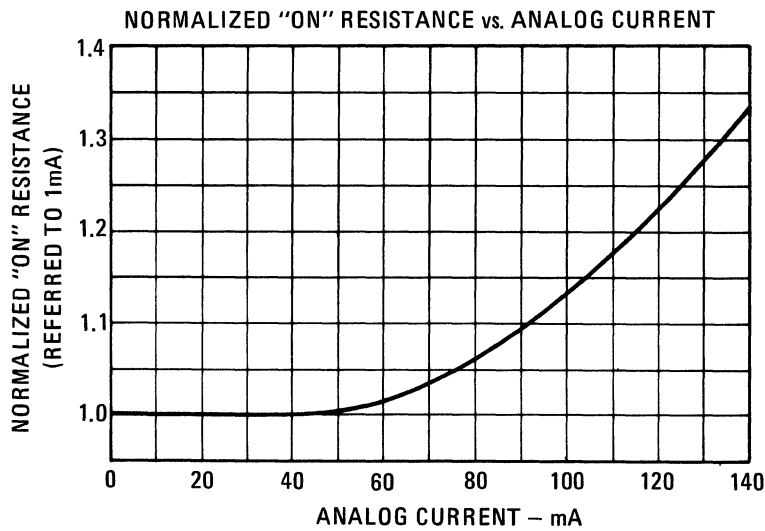
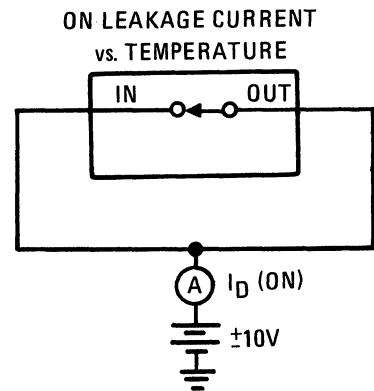
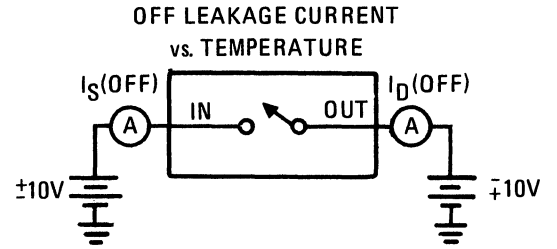
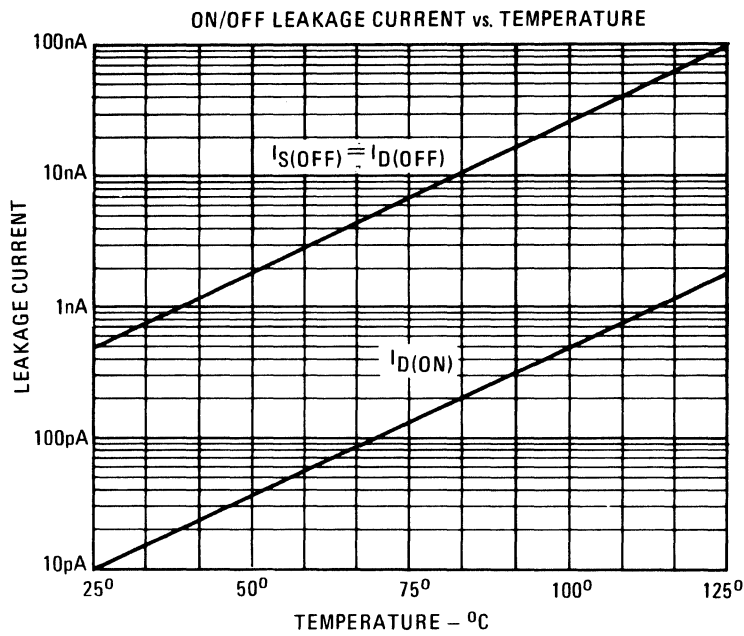
"ON" RESISTANCE vs. ANALOG SIGNAL LEVEL
AND POWER SUPPLY VOLTAGE



NORMALIZED "ON" RESISTANCE vs. TEMPERATURE



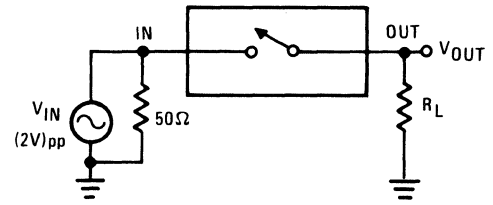
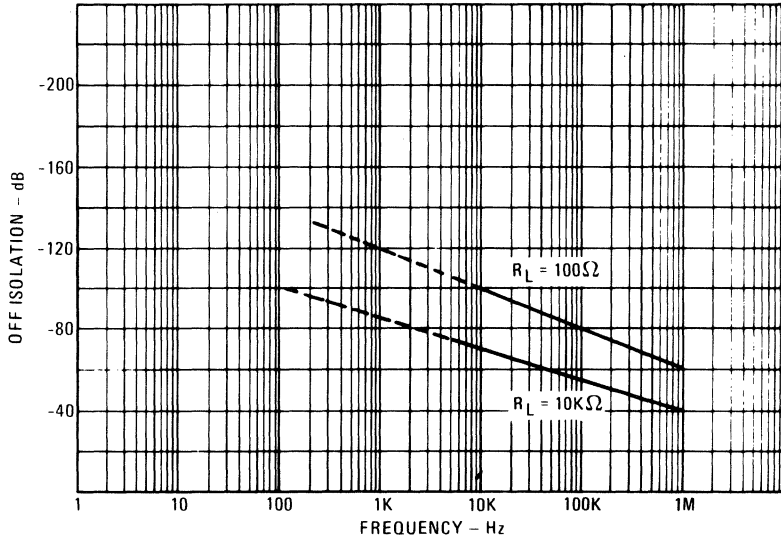
PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (continued)



LINEAR

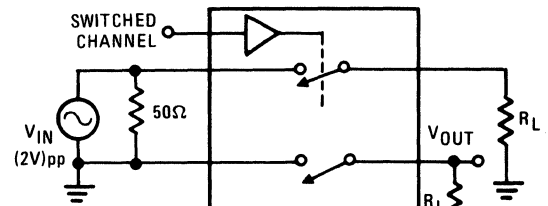
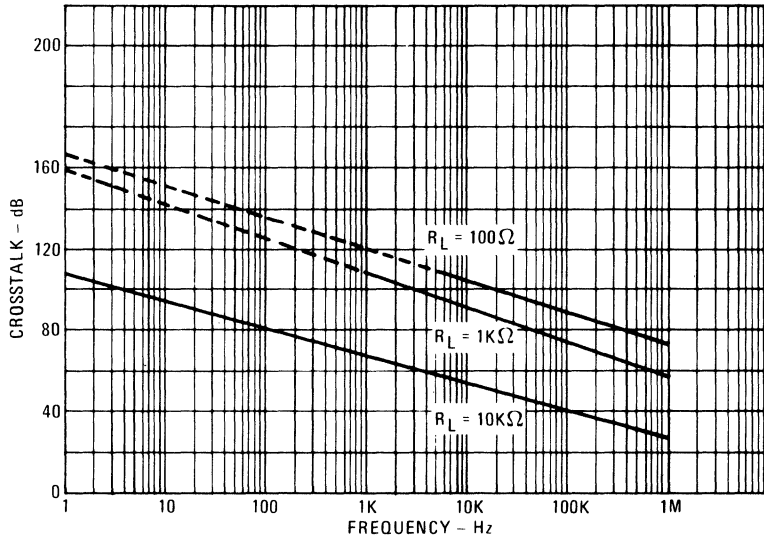
PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (continued)

"OFF" ISOLATION vs. FREQUENCY



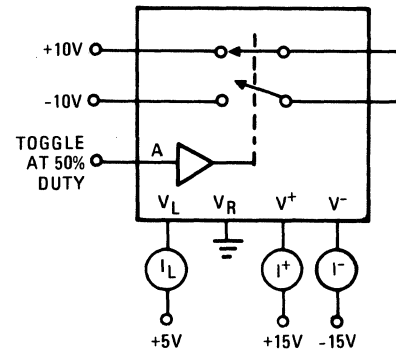
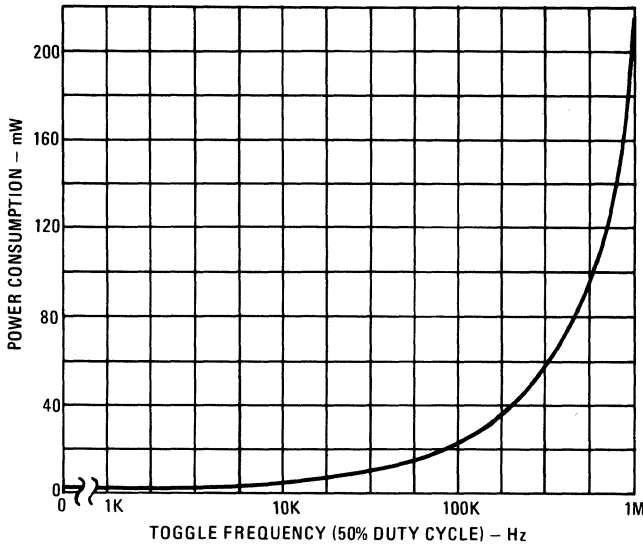
$$\text{"OFF" ISOLATION} = 20 \log \left(\frac{V_{IN}}{V_{OUT}} \right)$$

CROSSTALK vs. FREQUENCY



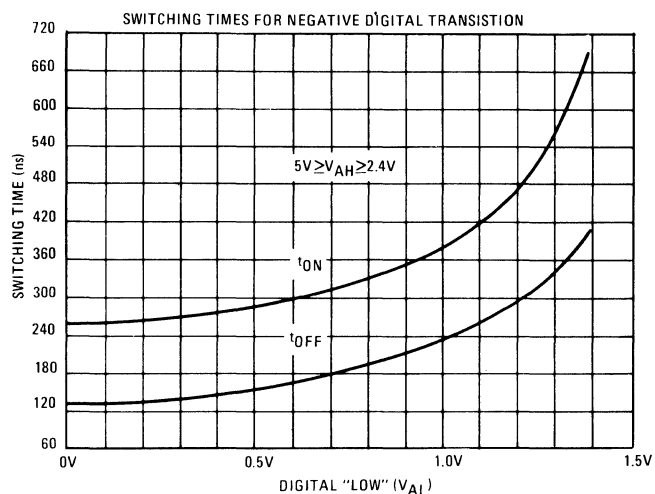
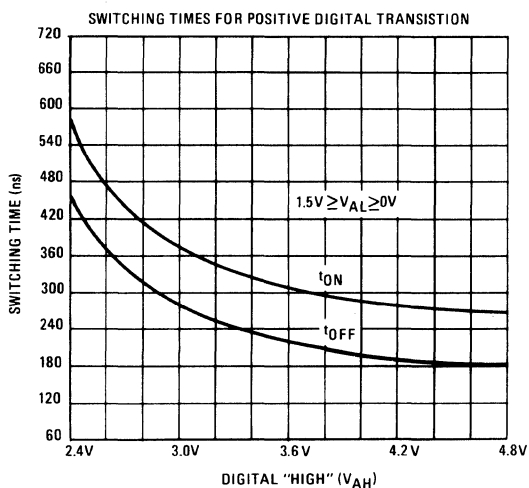
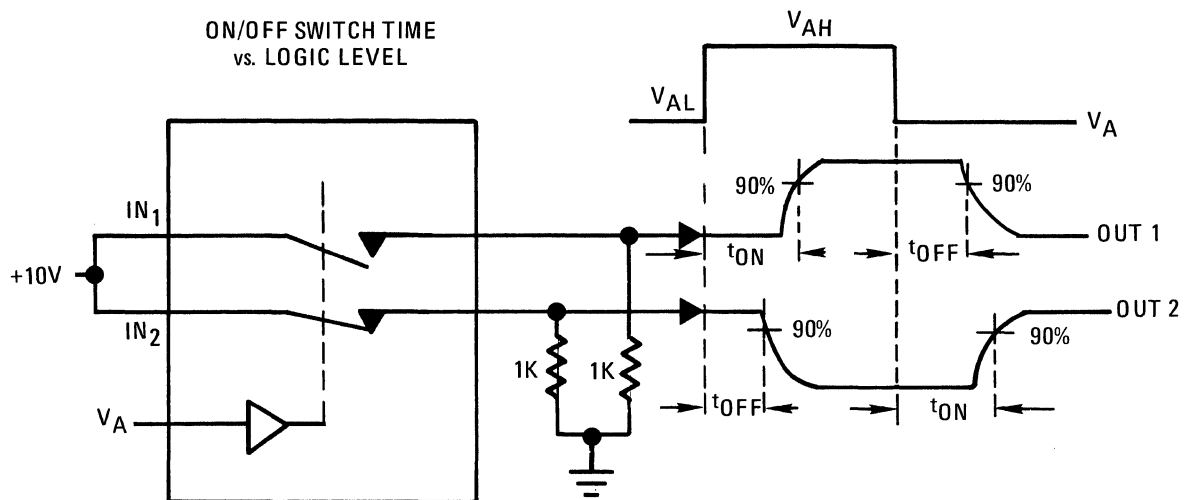
$$\text{"CROSSTALK"} = 20 \log \left(\frac{V_{IN}}{V_{OUT}} \right)$$

POWER CONSUMPTION vs. FREQUENCY



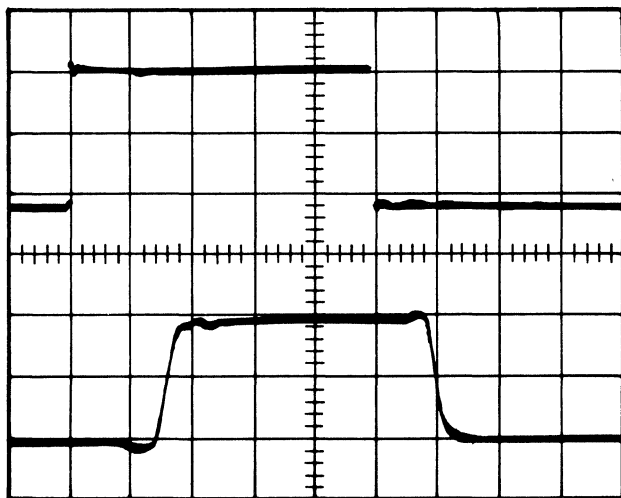
LINEAR

SWITCHING CHARACTERISTICS



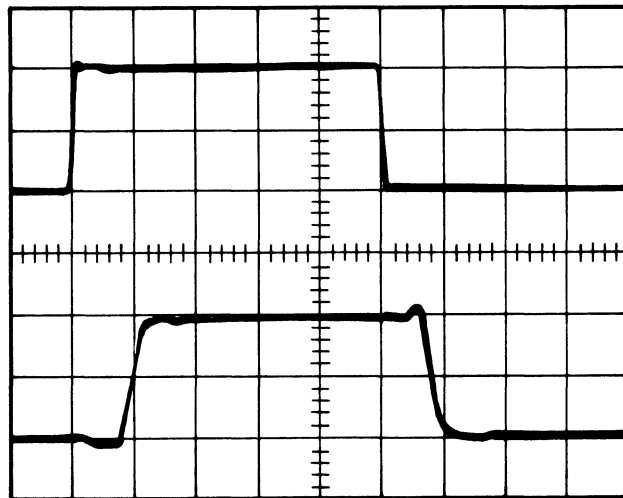
SWITCHING WAVEFORMS

TOP: TTL INPUT (1V/DIV)
 $V_{AH} = 3V, V_{AL} = 0.8V$
 BOTTOM: OUTPUT (5V/DIV)



200ns/DIV

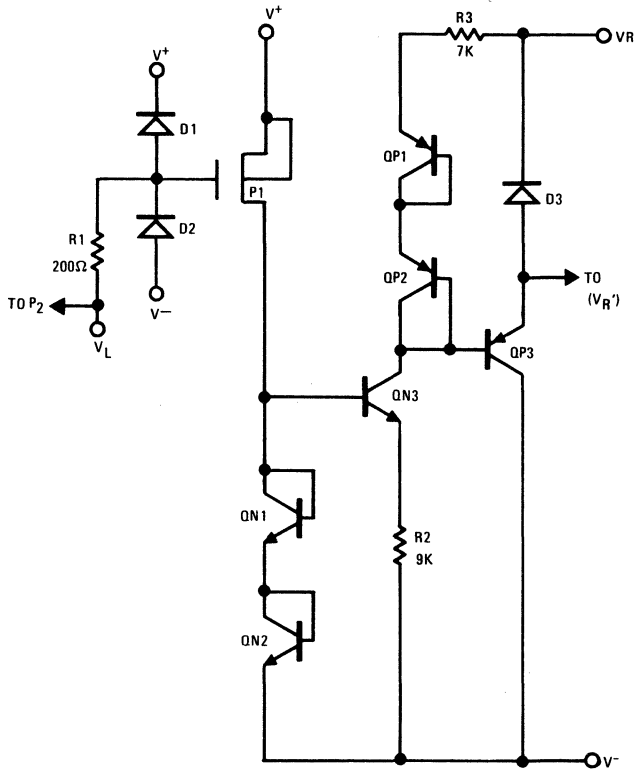
TOP: CMOS INPUT (5V/DIV)
 $V_{AH} = 10V, V_{AL} = 0V$
 BOTTOM: OUTPUT (5V/DIV)



200ns/DIV

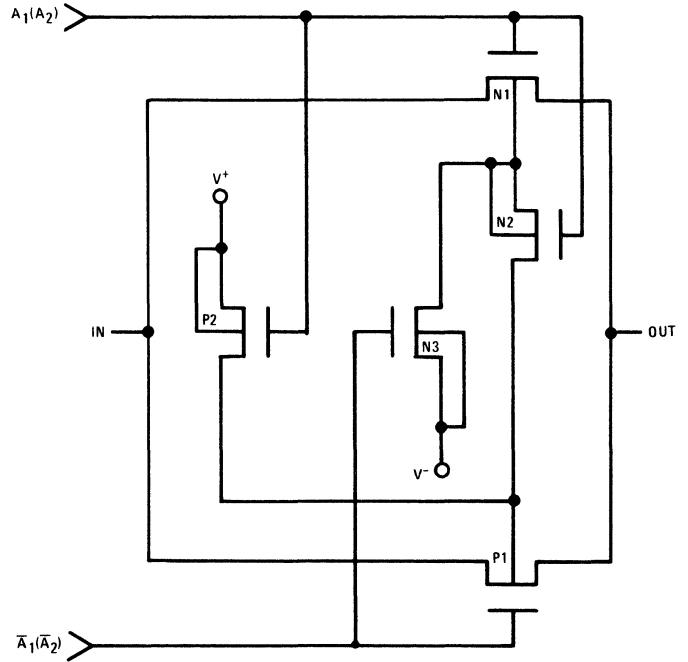
SCHEMATIC DIAGRAMS

TTL/CMOS
REFERENCE CIRCUIT*

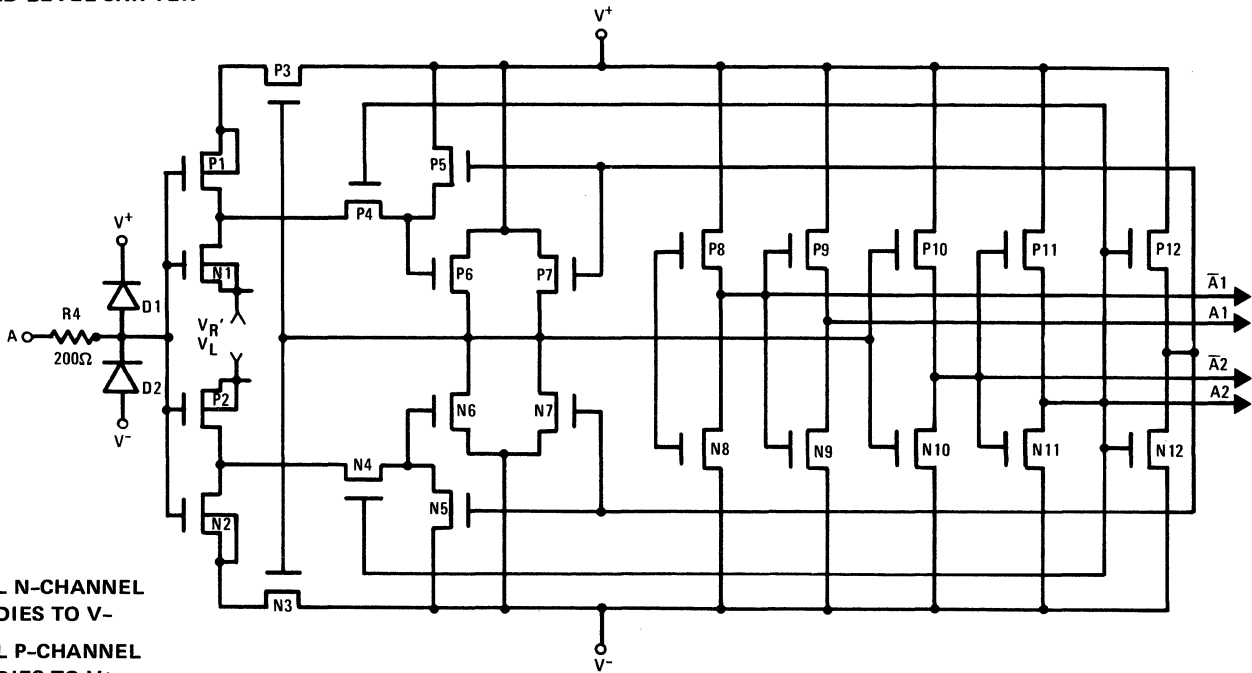


*Connect V^+ to V_L for minimizing power consumption when driving from CMOS circuits

SWITCH CELL



DIGITAL INPUT BUFFER
AND LEVEL SHIFTER



ALL N-CHANNEL
BODIES TO V^-
ALL P-CHANNEL
BODIES TO V^+
EXCEPT AS SHOWN

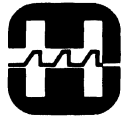
MEMORY DATA SHEETS

On the subject of field programmable read-only memories the words PROM and Harris Semiconductor are virtually inseparable. The first effort to produce user programmable logic was ushered in by Harris in 1967 with the introduction of the diode matrix family. Again, in 1969, the advent of the HPROM-0512 heralded the world's first monolithic field programmable read-only memory. This prototype, featuring nichrome fuse technology paved the way for future PROM generations establishing unprecedented reliability attested to by the fact that the HPROM-0512, as of the printing of this catalog, is still the only field programmable read-only memory to receive full JAN 38510 certification.

After six years of high volume PROM manufacturing Harris Semiconductor remains today the world's largest single manufacturer of PROMs. Now, this high volume experience, coupled with continuing reliability, introduces the next generation in PROM development, the "GENERIC" family of PROMs. With design controlled by a family concept, each GENERIC PROM features identical programming, improved AC performance guaranteed over full temperature and voltage ranges, common circuit design and process technology. We invite you to study our GENERIC data sheets. You will soon see that "to know one GENERIC PROM is to know them all". Simplified device qualification, simplified system redesign and upgrading, maximum standardization and minimum costs; they're all in the family with GENERIC PROMs.

MEMORY ALPHA-NUMERICAL INDEX

PAGE	ITEM	
Me-3	HD-234/534	Hex Interface Inverters
Me-3	HD-235/535	Hex Interface Drivers
Me-9	HD-6600	Quad Power Strobe
Me-9	HD-6605	Quad Logic Strobe
Me-13	HM-010/030/040/050/ 074/080/090	MIL Temperature Diode Matrices
Me-21	HM-0110/0168/0104/ 0186	Commercial Diode Matrices
Me-23	HM-7202	1024 x 7 N-Channel MOS RAM
Me-27	Generic Prom Product Chart	
Me-28	HM-7602/7603	256-Bit Field Programmable Bipolar PROM
Me-32	HM-7610/7611	1024-Bit Field Programmable Bipolar PROM
Me-36	HM-7620/7621	2048-Bit Field Programmable Bipolar PROM
Me-40	HM-7640/7641	4096-Bit Field Programmable Bipolar PROM
Me-44	Harris Bipolar Prom Cross-Reference	
Me-45	HPROM-0512	512- Bit Field Programmable Bipolar PROM
Me-51	HPROM-1024/1024A	1024-Bit Field Programmable Bipolar PROM
Me-55	HPROM-8256	256-Bit Field Programmable Bipolar PROM



HARRIS
SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HD-234/534

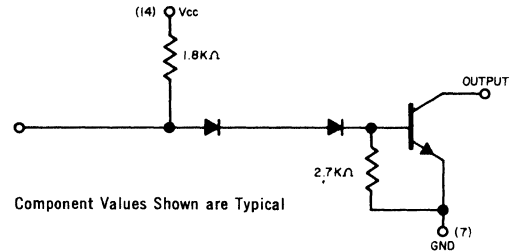
Hex Interface Inverters

HD-235/535

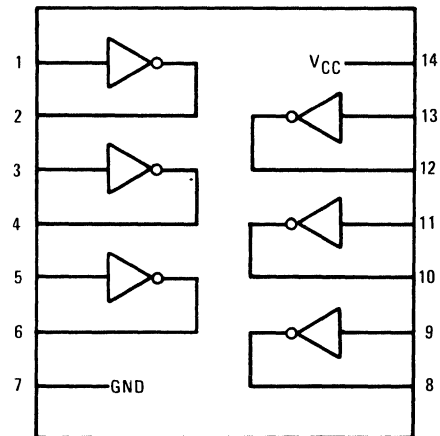
Hex Interface Drivers

GENERAL DESCRIPTION

The integrated circuits covered by this data sheet form a part of Harris' family of Military and Industrial Monolithic Interface Circuits intended for use as universal inverters, translators between logic families, as logic drivers in Monolithic Diode Matrix logic and in high voltage applications. The interface circuit with the node-input is compatible with all logic families, RTL, DTL, T²L and CML. The circuits are fabricated within a single monolithic silicon chip using passivated epitaxial techniques and Harris' Dielectric Isolation method. Each circuit type consists of six node-input inverters as shown in the circuit schematic. Use of Dielectric Isolation provides parasitic-free operation with electrical performance surpassing that of conventionally constructed integrated circuits. Harris' Interface Circuits are designed to meet or exceed the mechanical and environmental requirements of MIL-STD-883.



BASIC CIRCUIT SCHEMATIC
(one element)



MILITARY	200	SERIES
INDUSTRIAL	500	SERIES

BASIC TYPES OF INTERFACE CIRCUITS

HEX INTERFACE INVERTER	
PROPAGATION DELAY	10ns
POWER DISSIPATION	10mW
OUTPUT BREAKDOWN VOLTAGE	6V

HIGH VOLTAGE HEX INTERFACE DRIVER	
PROPAGATION DELAY	35ns
POWER DISSIPATION	10mW
OUTPUT BREAKDOWN VOLTAGE	35V

HIGH VOLTAGE HEX INDICATOR DRIVER	
TURN-ON OR TURN-OFF DELAY	0.8 μs
PROPAGATION DELAY	35ns
POWER DISSIPATION	12mW
OUTPUT BREAKDOWN VOLTAGE	55V

SELECTION GUIDE

- HEX INTERFACE INVERTER
 - 200 SERIES ... PAGES Di - 9, Di - 10
 - 500 SERIES ... PAGES Di - 9, Di - 12
- HEX INTERFACE DRIVER
 - 200 SERIES ... PAGES Di - 9, Di - 11
 - 500 SERIES ... PAGES Di - 9, Di - 13
- HEX INDICATOR DRIVER
 - 500 SERIES ... PAGES Di - 9, Di - 14

MEMORY

HEX INTERFACE INVERTER
HD-234

MILITARY 200 SERIES

ABSOLUTE MAXIMUM RATINGS

Input Voltage : +6 Volts Output Current : +50mA
 Output Voltage : +6 Volts Operating Temp. : -55°C to +125°C
 V_{cc} : +8 Volts Storage Temp. : -65°C to +150°C

Maximum ratings are limiting values above which permanent circuit damage may occur.

STATIC ELECTRICAL CHARACTERISTICS (Notes 1, 4)

CHARACTERISTIC	LIMITS				TEST CONDITIONS				NOTES see page Di - 11
	MIN.	TYP.	MAX.	UNIT	TEMP.	V _{cc}	DRIVEN INPUT	OUTPUT	
"1" OUTPUT VOLTAGE									
node Input	4.0	4.5		V	-55°C	4.5V	2.2V	SEE	3
node Input	4.0	4.5		V	+25°C	4.5V	1.8V	NOTE	3
node Input	3.7	4.4		V	+125°C	4.5V	1.2V	2a	3
"0" OUTPUT VOLTAGE									
node Input		.25	.45	V	-55°C	4.5V		16.7mA	3
node Input		.25	.40	V	+25°C	5.0V		20.5mA	3
node Input		.25	.45	V	+125°C	5.5V		20.5mA	3
"0" INPUT CURRENT									
node Input		2.55	3.45	mA	-55°C	5.5V	.35V		3
node Input	1.80	2.70	3.45	mA	+25°C	5.5V	.35V		3
node Input		2.30	3.45	mA	+125°C	5.5V	.35V		3
"1" OUTPUT CURRENT									
			100	nA	+25°C	4.5V	GND	4.5V	3
			50	μA	+125°C	4.5V	GND	4.5V	3
POWER DISSIPATION									
		12	17.5	mW	+25°C	5.0V	GND		
		8	11.0	mW	+25°C	5.0V	OPEN		
OUTPUT CAPACITANCE									
		2.0		pF	+25°C	5.0V	GND	0.5VDC 25mVrms @ 1MHz	

SWITCHING (DYNAMIC) CHARACTERISTICS

CHARACTERISTIC	LIMITS				TEST CONDITIONS			
	MIN.	TYP.	MAX.	UNIT	TEMP.	V _{cc}	TEST CIRCUIT	FAN-OUT
Turn On Delay		20	35	ns	-55°C	4.5V		8
t _{on}		13	20	ns	+25°C	4.5V	Circuit No. 1	8
		15	22	ns	+125°C	4.5V	R _L = 220Ω	8
Turn Off Delay		10	25	ns	-55°C	5.5V	2	1
t _{off}		5	15	ns	+25°C	5.5V	2	1
		8	25	ns	+125°C	5.5V	2	1
Propagation Delay								
t _{pd}		8	12	ns	+25°C	5.0V	3	1

MEMORY

HIGH VOLTAGE HEX INTERFACE DRIVER

HD-235

MILITARY 200 SERIES

ABSOLUTE MAXIMUM RATINGS

Input Voltage : +6 Volts Output Current : +35mA
 Output Voltage : +35 Volts Operating Temp. : -55°C to +125°C
 V_{cc} : +8 Volts Storage Temp. : -65°C to +150°C

Maximum ratings are limiting values above which permanent circuit damage may occur.

STATIC ELECTRICAL CHARACTERISTICS (Notes 1, 4)

CHARACTERISTIC	LIMITS				TEST CONDITIONS				
	MIN.	TYP.	MAX.	UNIT	TEMP.	V _{cc}	DRIVEN INPUT	OUTPUT	NOTES see below
"1" OUTPUT VOLTAGE node Input	29			V	-55°C	4.5V	2.2V	SEE	3
	29			V	+25°C	4.5V	1.8V	NOTE	3
	28			V	+125°C	4.5V	1.2V	2b	3
"0" OUTPUT VOLTAGE node Input			1.0	V	-55°C	4.5V		5mA	3
		.55	1.0	V	+25°C	5.0V		10mA	3
			1.0	V	+125°C	5.5V		10mA	3
"0" INPUT CURRENT node Input		2.55	3.45	mA	-55°C	5.5V	.35V		3
	1.80	2.70	3.45	mA	+25°C	5.5V	.35V		3
		2.30	3.45	mA	+125°C	5.5V	.35V		3
"1" OUTPUT CURRENT		.025	1.0	μA	+25°C	4.5V	GND	30V	3
		1	50	μA	+125°C	4.5V	GND	30V	3
POWER DISSIPATION		12	17.5	mW	+25°C	5.0V	GND		
		8	11.0	mW	+25°C	5.0V	OPEN		
OUTPUT CAPACITANCE		5.0		pF	+25°C	5.0V	GND	0.5VDC 25mVrms @ 1MHz	

SWITCHING (DYNAMIC) CHARACTERISTICS

CHARACTERISTIC	LIMITS				TEST CONDITIONS		
	MIN.	TYP.	MAX.	UNIT	TEMP.	V _{cc}	TEST CIRCUIT
Propagation Delay t _{pd}			80	ns	-55°C	5.0V	3
		35	70	ns	+25°C	5.0V	
			80	ns	+125°C	5.0V	

NOTES:

- This specification is written for one gate element. With multiple element packages, all elements within the package must qualify for the package to obtain "type" classification.
- 2a. The output is to be returned to V_{cc} through 5.6KΩ for these tests.
- 2b. The output is to be returned to +30V through 5.6KΩ for these tests.
- "NAND" Logic Definitions: "UP" Level = "1" "DOWN" Level = "0".
- All measurements made with Pin 7 at zero volts. All voltage and capacitance measurements are referenced to pin 7. Terminals not specifically mentioned are left electrically open.
- These measurements must be made using current forcing, voltage measuring techniques.

MEMORY

ABSOLUTE MAXIMUM RATINGS

Input Voltage : +6 Volts Output Current : +50mA
 Output Voltage : +6 Volts Operating Temp. : 0°C to +75°C
 V_{cc} : +8 Volts Storage Temp. : -65°C to +150°C

Maximum ratings are limiting values above which permanent circuit damage may occur.

STATIC ELECTRICAL CHARACTERISTICS (Notes 1, 4)

CHARACTERISTIC	LIMITS			UNIT	TEST CONDITIONS					
	MIN.	TYP.	MAX.		TEMP.	V _{cc}	DRIVEN INPUT	OUTPUT	NOTES see page Di - 11	
"1" OUTPUT VOLTAGE										
	node Input	3.0	3.8	V	0°C	4.5V	1.6V	SEE	3	
	node Input	3.0	3.8	V	+25°C	4.5V	1.6V	NOTE	3	
node Input	3.0	3.8	V	+75°C	4.5V	1.3V	2a	3		
"0" OUTPUT VOLTAGE										
	node Input		.30	.45	V	0°C	4.5V	12.0mA	3	
	node Input		.30	.45	V	+25°C	5.0V	13.3mA	3	
node Input		.30	.45	V	+75°C	5.5V	14.4mA	3		
"0" INPUT CURRENT										
	node Input		2.70	3.45	mA	0°C	5.5V	.45V	3	
	node Input	1.80	2.70	3.45	mA	+25°C	5.5V	.45V	3	
node Input		2.70	3.45	mA	+75°C	5.5V	.45V	3		
"1" OUTPUT CURRENT										
			.05	1	μA	+25°C	4.5V	GND	4.5V	3
			.1	5	μA	+75°C	4.5V	GND	4.5V	3
POWER DISSIPATION										
			14.8	17.5	mW	+25°C	5.0V	GND		
			10.0	11.0	mW	+25°C	5.0V	OPEN		
OUTPUT CAPACITANCE										
			2.0		pF	+25°C	5.0V		0.5VDC 25mVrms @ 1 MHz	

SWITCHING (DYNAMIC) CHARACTERISTICS

CHARACTERISTIC	LIMITS			UNIT	TEST CONDITIONS		
	MIN.	TYP.	MAX.		TEMP.	V _{cc}	TEST CIRCUIT
Propagation Delay t _{pd}		18	25	ns	+25°C	5.0V	3

MEMORY

HIGH VOLTAGE HEX INTERFACE DRIVER
HD-535

INDUSTRIAL 500 SERIES

ABSOLUTE MAXIMUM RATINGS

Input Voltage : +6 Volts Output Current : +35mA
 Output Voltage : +35 Volts Operating Temp. : -0°C to +75°C
 V_{cc} : +8 Volts Storage Temp. : -65°C to +150°C

Maximum ratings are limiting values above which permanent circuit damage may occur.

STATIC ELECTRICAL CHARACTERISTICS (Notes 1, 4)

CHARACTERISTIC	LIMITS				TEST CONDITIONS				NOTES see page Di - 11
	MIN.	TYP.	MAX.	UNIT	TEMP.	V _{cc}	DRIVEN INPUT	OUTPUT	
"1" OUTPUT VOLTAGE node Input node Input node Input	29			V	0°C	4.5V	1.6V	SEE	3
	29			V	+25°C	4.5V	1.6V	NOTE	3
	28			V	+75°C	4.5V	1.3V	2b	3
"0" OUTPUT VOLTAGE node Input node Input node Input			1.0	V	0°C	4.5V		8.0mA	3
		.65	1.0	V	+25°C	5.0V		8.0mA	3
			1.0	V	+75°C	5.5V		8.0mA	3
"0" INPUT CURRENT node Input node Input node Input		2.95	3.45	mA	0°C	5.5V	.45V		3
	1.80	2.95	3.45	mA	+25°C	5.5V	.45V		3
		2.95	3.45	mA	+75°C	5.5V	.45V		3
"1" OUTPUT CURRENT		.1	1	μA	+25°C	4.5V	GND	30V	3
		1	50	μA	+75°C	4.5V	GND	30V	3
POWER DISSIPATION		14.8	17.5	mW	+25°C	5.0V	GND		
		10.0	11.0	mW	+25°C	5.0V	OPEN		
OUTPUT CAPACITANCE		5.0		pF	+25°C	5.0V	GND	0.5VDC 25mVrms @ 1 MHz	

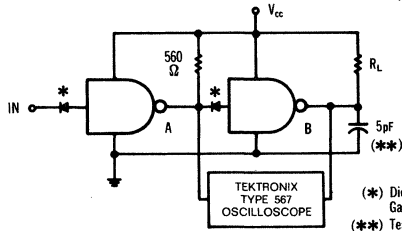
SWITCHING (DYNAMIC) CHARACTERISTICS

CHARACTERISTIC	LIMITS				TEST CONDITIONS		
	MIN.	TYP.	MAX.	UNIT	TEMP.	V _{cc}	TEST CIRCUIT
Propagation Delay t _{pd}		35	70	ns	+25°C	5.0V	3

MEMORY

TEST CIRCUITS

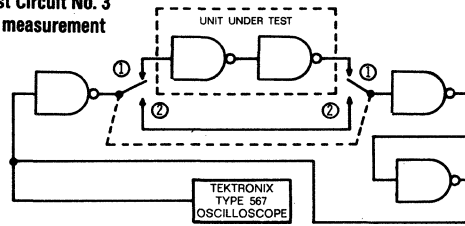
Test Circuit No. 1
 t_{on} and t_{off} — measurements



INPUT PULSE
 $t_r = t_f = 5ns$
 $f = 1MHz$
 $pw = 100ns$

(*) Diodes from Expander Gate RD-211
 (***) Test Fixture and Probe Capacity

Test Circuit No. 3
 t_{pd} measurement

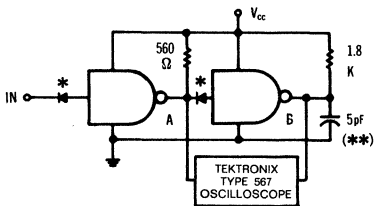


Propagation delay for one element based on pair delay measurement

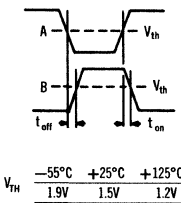
$$t_{pd} = \frac{T_2 - T_1}{4}$$

Where
 T_2 = Measured time for one cycle of oscillation with switch in position ① (5 elements)
 And
 T_1 = Measured time for one cycle of oscillation with switch in position ② (3 elements standard)

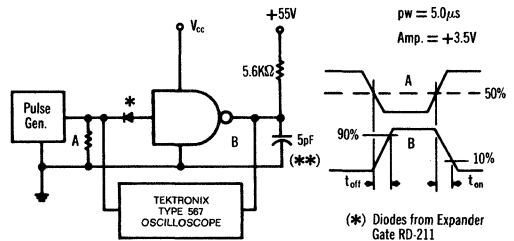
Test Circuit No. 2
 t_{on} and t_{off} — measurements



(*) Diodes from Expander Gate RD-211
 (***) Test Fixture and Probe Capacity



Test Circuit No. 4
 t_{on} and t_{off} — measurements



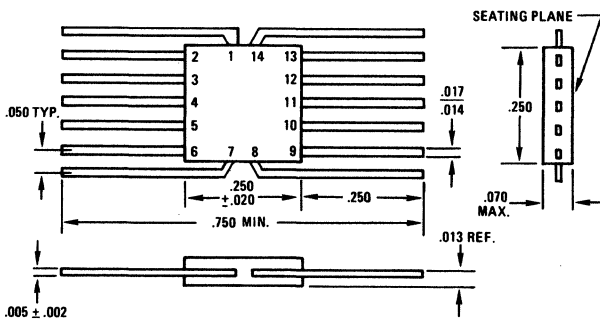
INPUT PULSE
 $t_r = t_f = 5ns$
 $f = 100KHz$
 $pw = 5.0\mu s$
 $Amp. = +3.5V$

(*) Diodes from Expander Gate RD-211
 (***) Test Fixture and Probe Capacity

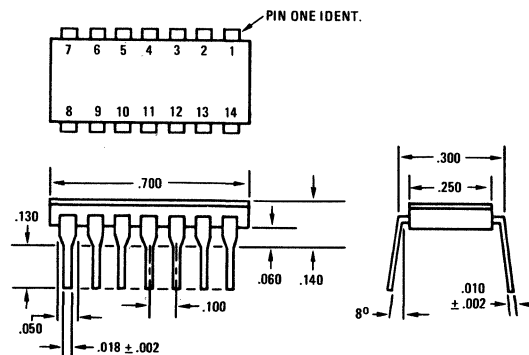
PACKAGING

Package outline drawings for Harris Integrated Circuits products are illustrated below. For each package, a particular Harris protective carrier is used in production, testing, and handling. If desired, this protective carrier may be specified for shipping purposes. Harris can also furnish custom designed packages from its in-house facility. The package Carriers and their relationship to corresponding test contactors are shown.

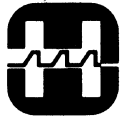
CODE 9V T0-86 (METAL BOTTOM)



CODE 1S 14 LEAD BRAZED D.I.P.



ALL DIMENSIONS ARE IN INCHES.
 ALL DIMENSIONS $\pm .010$ UNLESS OTHERWISE SHOWN.



HARRIS
SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HD-6600

Quad Power Strobe

HD-6605

Quad Logic Strobe

FEATURES

- HIGH DRIVE CURRENT – 200mA
- HIGH SPEED 50ns TYPICAL
- TTL COMPATIBLE INPUTS
- DIELECTRIC ISOLATION
- QUAD MONOLITHIC CONSTRUCTION
- POWER SUPPLY FLEXIBILITY
- LOW POWER STANDBY 30mW/CIRCUIT
 ACTIVE 95mW/CIRCUIT

DESCRIPTION

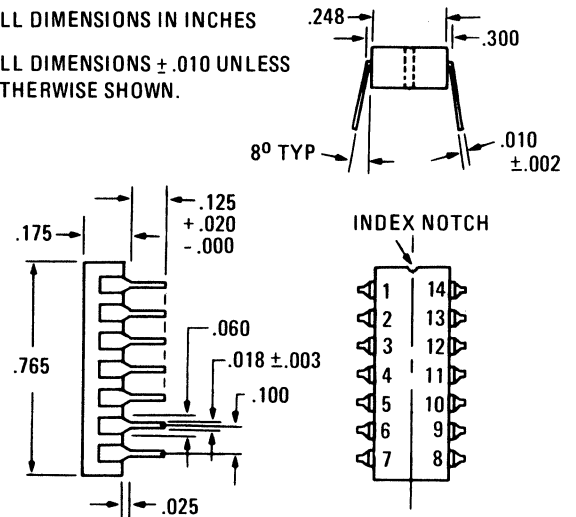
The HD-6600 Quad Power Strobe and HD-6605 Quad Logic Strobe are constructed with Harris Dielectric Isolation Bipolar Monolithic Process. The design incorporates power supply flexibility with TTL compatible inputs and high current outputs.

PACKAGE

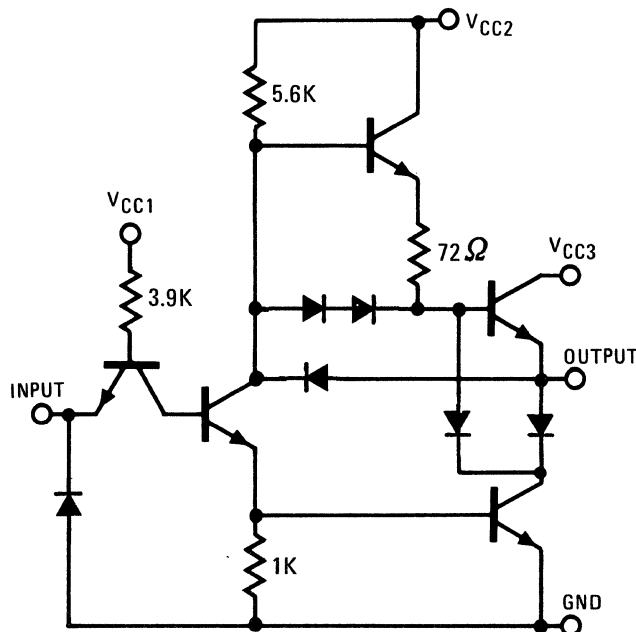
CODE 1A TO-116(14 LEAD CERAMIC D.I.P.)

ALL DIMENSIONS IN INCHES

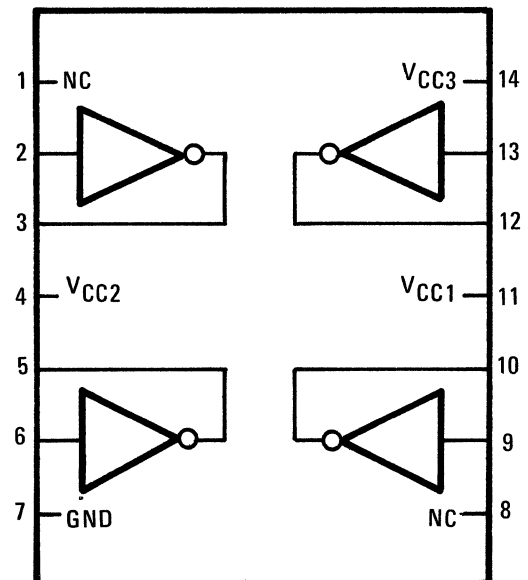
ALL DIMENSIONS ± .010 UNLESS OTHERWISE SHOWN.



CIRCUIT DIAGRAM



LOGIC DIAGRAM



NC: NO CONNECTION

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage V_{CC1}	+ 8 VDC
V_{CC2}	+18 VDC (HD-6600), +14 VDC (HD-6605)
V_{CC3}	+18 VDC (HD-6600), +8 VDC (HD-6605)
Input Voltage V_{IN}	-0.5 VDC to +5.5 VDC
Storage Temperature T_{STG}	-65°C to +150°C
Output Current I_L	-300mA
Power Dissipation at 25°C	1000mW (Derate 9mW/°C Above 60°C)

RECOMMENDED OPERATING CONDITIONS

Power Supplies: V_{CC1}	5 VDC	±10%
V_{CC2}	12 VDC	±15%
V_{CC3}	5 VDC	±20%

ELECTRICAL CHARACTERISTICS

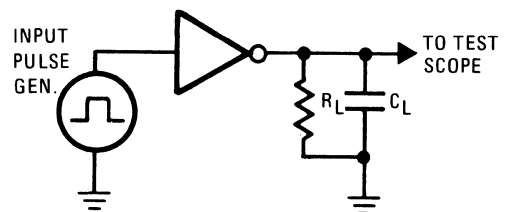
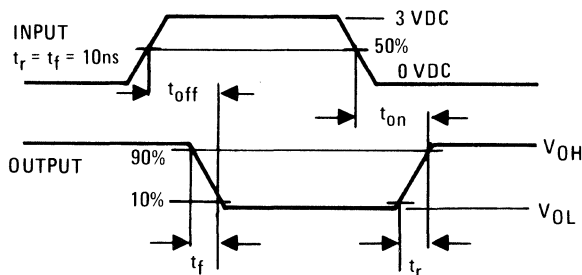
$T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ HD1-6600-2/HD1-6605-2 $V_{CC2} = 12.0$ VDC
 $T_A = 0^\circ\text{C}$ to $+75^\circ\text{C}$ HD1-6600-5/HD1-6605-5 $V_{CC3} = 5.0$ VDC

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS	
Input Current	I_{IR}			60	μA	$V_{IN} = 2.4$ VDC	$V_{CC1} = 5.5$ VDC
	I_{IF}			-1.6	mA	$V_{IN} = 0.4$ VDC	
Input Threshold Voltage	V_{IH}	2.0			V	$V_{CC1} = 4.5$ VDC	
	V_{IL}			0.8	V		
Output Voltage (Note 1)	V_{OH}	4.75	4.85		V	$V_{CC1} = 5.0$ VDC $V_{IN} = 0.4$ VDC	$I_L = -150$ mA DC
	V_{OL}			1.0	V	$V_{CC1} = 5.0$ VDC $V_{IN} = 2.4$ VDC	$I_L = 500$ μA DC
Supply Current (Note 2)	I_{CC1}		4	6.0	mA	$V_{CC1} = 5.5$ VDC	$V_{IN} = 2.4$ VDC
	I_{CC1}		4	6.4	mA	$V_{CC1} = 5.5$ VDC	$V_{IN} = .4$ VDC
	I_{CC2}		40	60	mA	$V_{CC1} = 5.5$ VDC $V_{IN} = 0.4$ VDC	$I_L = -150$ mA DC
	I_{CC2}		8	12	mA	$V_{CC1} = 5.5$ VDC $V_{IN} = 2.4$ VDC	$I_L = 0$

PARAMETER	SYM.	TYP.	MAX.	UNITS	CONDITIONS $T_A = 25^\circ\text{C}$
Turn On Delay	t_{on}	50	75	ns	$V_{CC1} = 5.0$ VDC $V_{CC2} = 12$ VDC $V_{CC3} = 5.0$ VDC $R_L = 31.6 \Omega$ $C_L = 620$ pf
Turn Off Delay	t_{off}	50	75	ns	
Rise Time	t_r	40	65	ns	
Fall Time	t_f	40	65	ns	

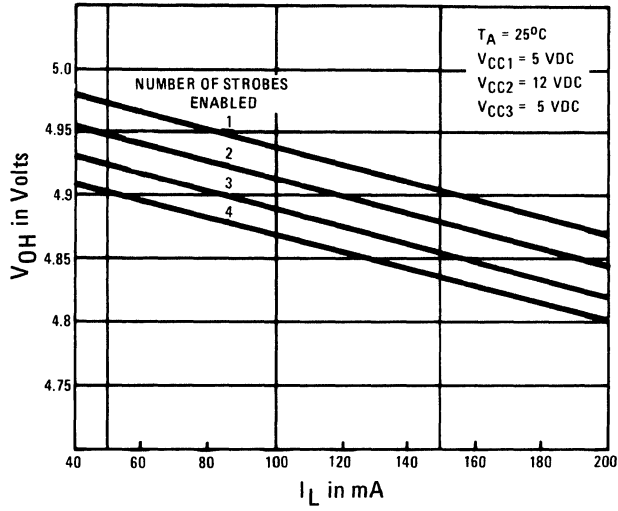
NOTES: (1) One strobe enabled. (2) All strobes enabled.

SWITCHING TIME DEFINITIONS

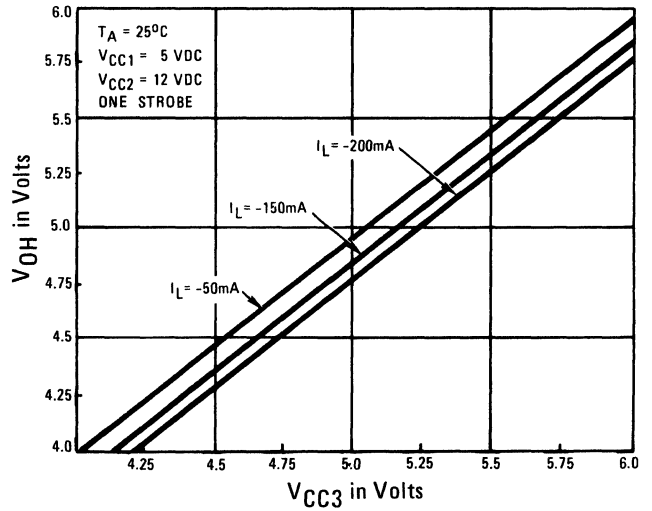


TYPICAL CHARACTERISTICS

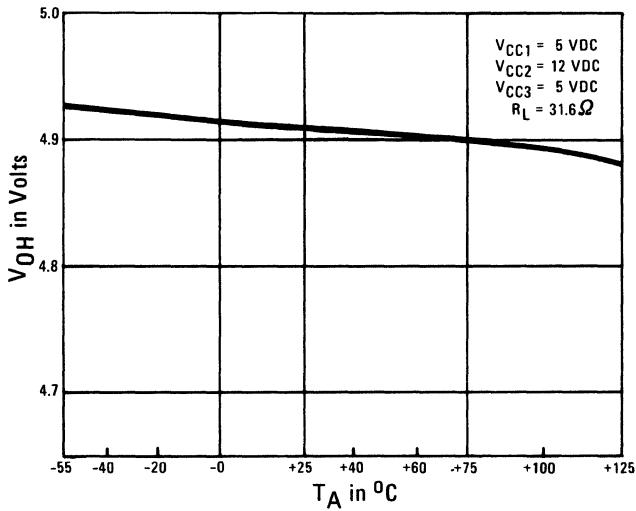
TYPICAL OUTPUT VOLTAGE vs. LOAD CURRENT AND NUMBER OF STROBES ENABLED



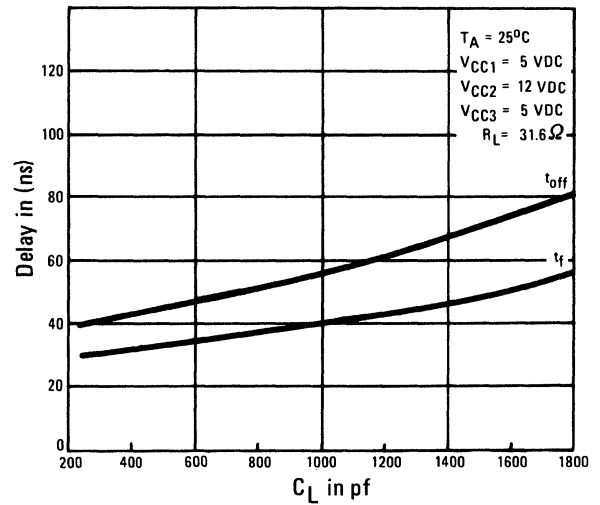
TYPICAL OUTPUT VOLTAGE vs. V_{CC3} SUPPLY VOLTAGE



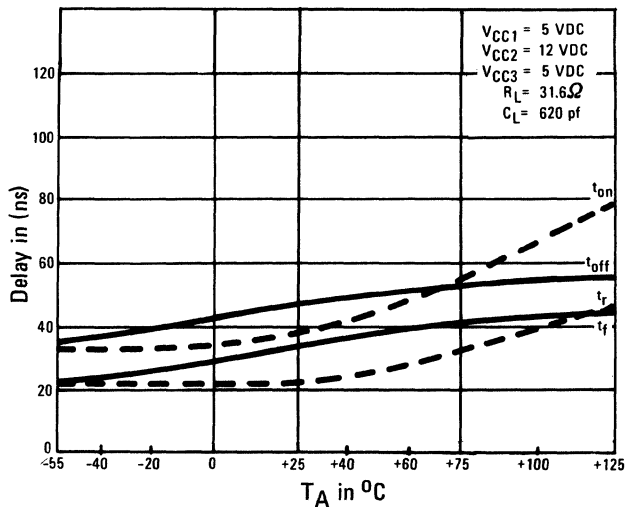
TYPICAL OUTPUT VOLTAGE vs. AMBIENT TEMPERATURE



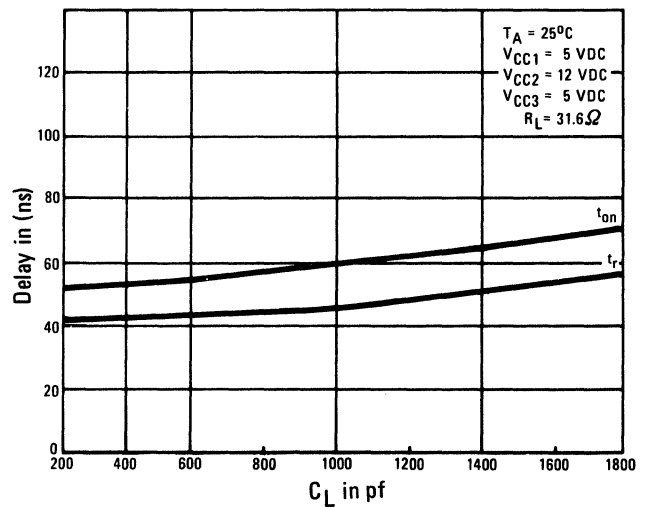
TYPICAL DELAY t_{off} AND t_f vs. LOAD CAPACITANCE



TYPICAL DELAY vs. AMBIENT TEMPERATURE

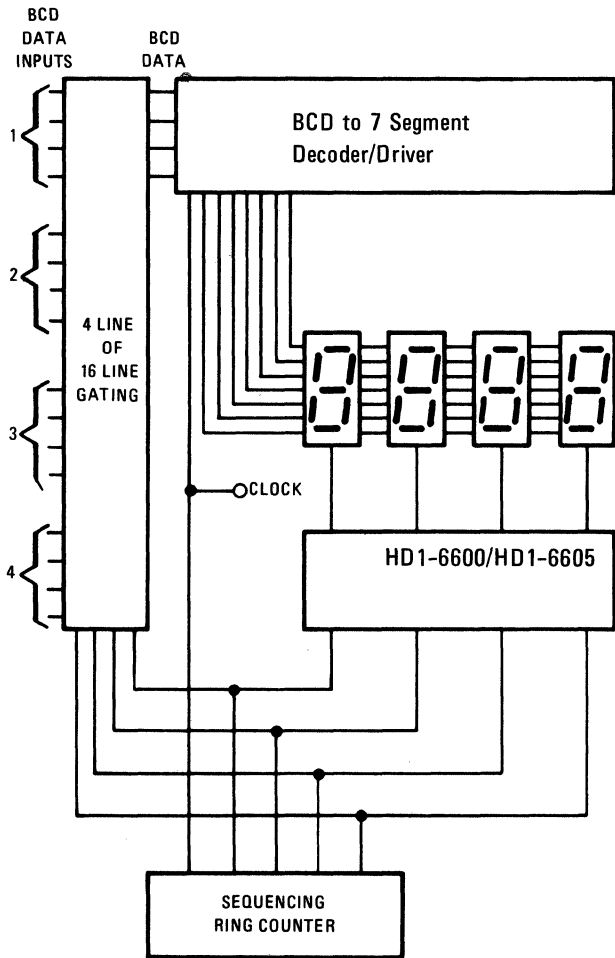


TYPICAL DELAY t_{on} AND t_r vs. LOAD CAPACITANCE



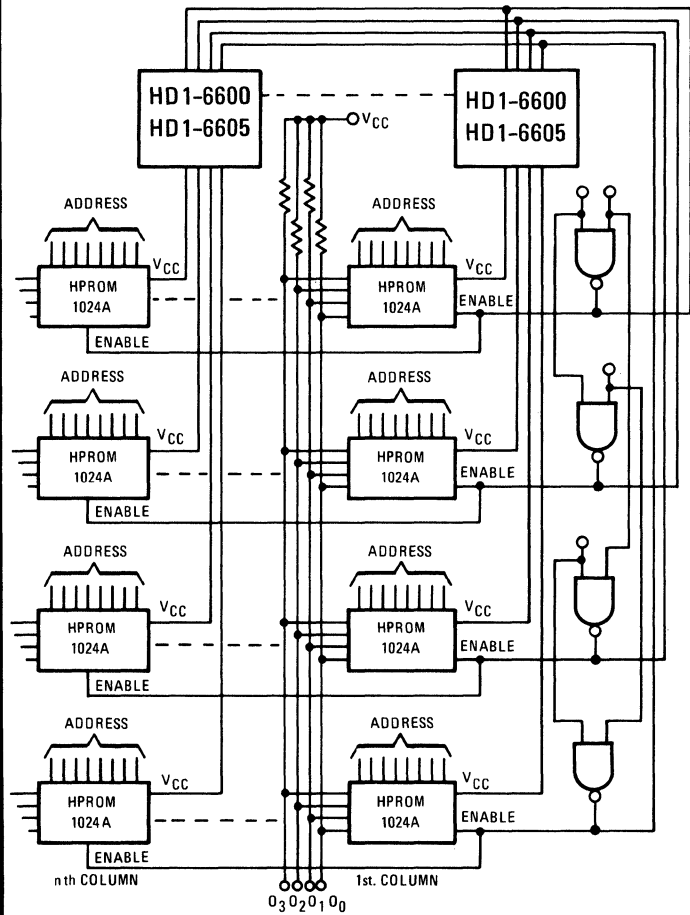
APPLICATIONS

LED MULTIPLEXING



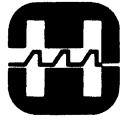
The HD-6600 Quad Power Strobe and HD-6605 Quad Logic Strobe, when used in conjunction with the HD-0140 Quad Latch/7 Segment Display Driver, provides a flexible multiplexed display system. The 150mA drive capability of the Power Strobe matches the current requirements of most 7 segment LED's presently available.

HD-6600 POWER STROBE HD-6605 "PROM" LOGIC STROBE



The use of the HD-6600 Power Strobe or HD-6605 Quad Logic Strobe with the HPROM 1024A programmable memories allows expansion of a 256 word memory to a 1024 word memory with only a nominal increase in system power. Using the enable signal as the Power Strobe input optimizes the enable to output delay of the memory.

MEMORY



HARRIS
SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HM-010/030/040/050/ 074/080/090

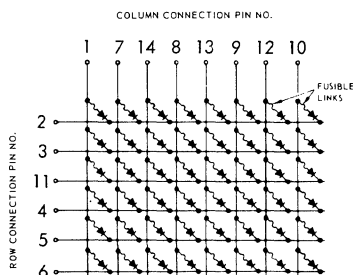
MIL Temperature Diode Matrices

Harris Monolithic Diode Matrices consist of arrays of passivated silicon diodes, fabricated in dielectrically isolated moats. Use of improved epitaxial techniques allow construction of arrays using the epitaxial layer as the common cathode connection for all diodes in a row. Column connection to the anode side of the diodes are made to metalized interconnect lines via fusible links. By selectively opening fuses, diodes are effectively removed from the circuit to form any desired matrix pattern. Harris automatic production test equipment provides instantaneous code pattern customizing from finished goods inventory.

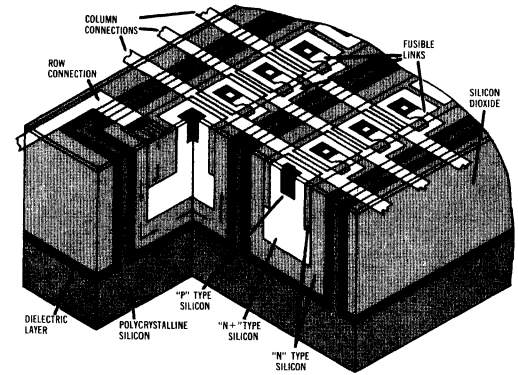
Combining the fusing technique with the availability of various matrix sizes and the possibility of assembling several matrices to form larger arrays, provides designers with the necessary flexibility in system design.

The matrices meet full military temperature range operation (-55°C to +125°C) and the circuits are designed to meet or exceed the mechanical and environmental requirements of MIL-STD-883.

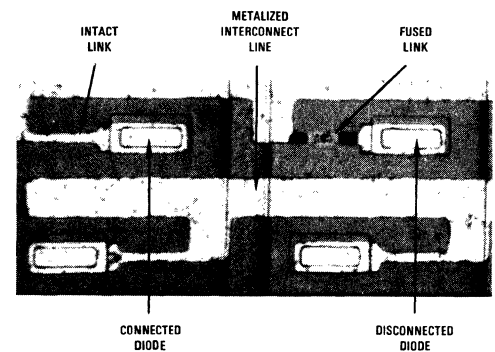
TYPICAL 6 x 8 CIRCUIT SCHEMATIC



Harris matrices are ideally suited for applications in logic generation, coding, decoding, and addressing type networks. For further information refer to Harris Diode Matrix Technical Information and Application Bulletin.



MONOLITHIC STRUCTURE



FUSIBLE LINK SYSTEM

MONOLITHIC INTERFACE CIRCUITS

When the Harris family of Monolithic Diode Matrices are used with Harris Monolithic Interface circuits, complex logic generation is possible with simple diode-inverter logic. A product selection guide for the monolithic interface circuits is given to help designers select the best interface circuit and matrix for his application. The interface circuits can be used for input to or output from any diode matrix.

MEMORY

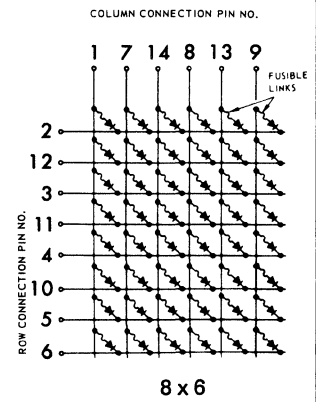
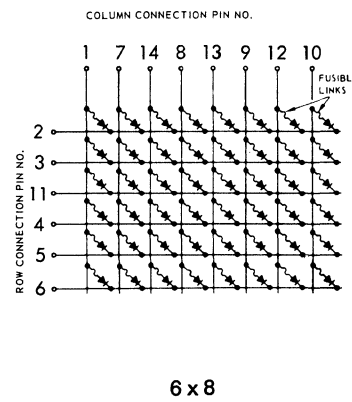
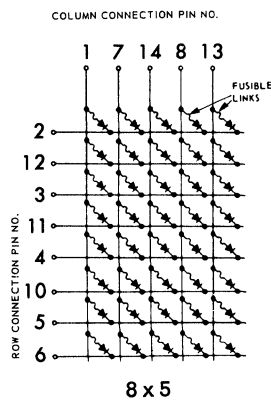
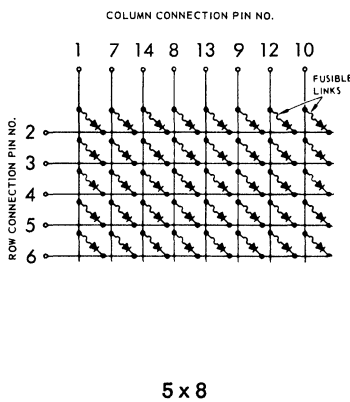
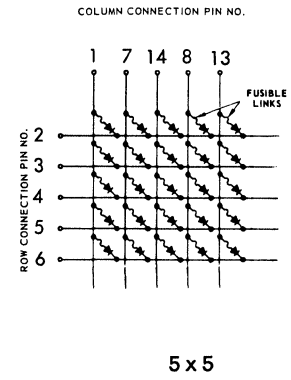
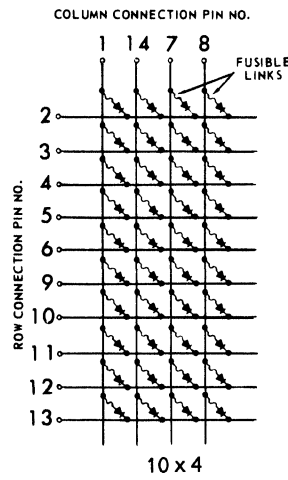
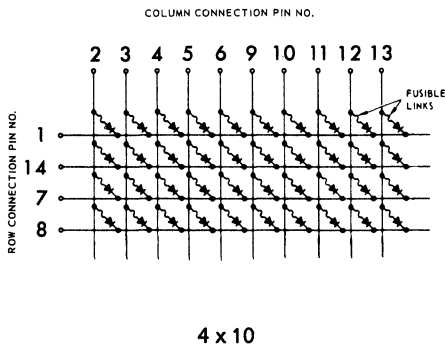
MONOLITHIC DIODE MATRICES

PRODUCT SELECTION GUIDE

MILITARY

MATRIX SIZE	FAST RECOVERY	MEDIUM RECOVERY	GENERAL PURPOSE	PACKAGE OUTLINE
4 x 10	HM1-090	HM1-091	HM1-093	1A
4 x 10	HM9-090	HM9-091	HM9-093	9H
10 x 4	HM1-050	HM1-051	HM1-055	1A
10 x 4	HM9-050	HM9-051	HM9-055	9H
5 x 5	HM1-074	HM1-075	HM1-077	1A
5 x 5	HM9-074	HM9-075	HM9-077	9H
5 x 8	HM1-010	HM1-012	HM1-013	1A
5 x 8	HM9-010	HM9-012	HM9-013	9H
8 x 5	HM1-080	HM1-081	HM1-084	1A
8 x 5	HM9-080	HM9-081	HM9-084	9H
6 x 8	HM1-030	HM1-031	HM1-034	1A
6 x 8	HM9-030	HM9-031	HM9-034	9H
8 x 6	HM1-040	HM1-041	HM1-044	1A
8 x 6	HM9-040	HM9-041	HM9-044	9H

DIODE PIN OUT CONFIGURATION



When ordering a matrix with a custom pattern take a matrix pattern and circle out those diodes to be removed from the matrix. Another method to clearly identify pattern is to call out row and column pins for each diode to be removed.

MEMORY

FAST RECOVERY MATRICES

HM-074	5 x 5	HM-050	10 x 4
HM-010	5 x 8	HM-080	8 x 5
HM-030	6 x 8	HM-090	4 x 10
HM-040	8 x 6		

ABSOLUTE MAXIMUM RATINGS

Forward Current : 100 mA
 Surge Current (100 μ s max.) : 200 mA Operating Temp. (ambient) : -55°C to +125°C
 Total Ckt. Dissipation (still air) : 450 mW Storage Temp. (ambient) : -65°C to +150°C

Maximum ratings are limiting values above which permanent circuit damage may occur.

ELECTRICAL CHARACTERISTICS

HM-010 HM-050 HM-080
 HM-030 HM-074 HM-090
 HM-040

CHARACTERISTIC	LIMITS			UNIT	TEST CONDITIONS	
	MIN.	TYP.	MAX.		TEMP.	ELECTRICAL
FORWARD DROP V_{F20} V_{F1}			1.5	V	-55°C	$I_F = 20$ mA
		1.0	1.3	V	+25°C	$I_F = 20$ mA
			.95	V	-55°C	$I_F = 1$ mA
		0.7	.75	V	+25°C	$I_F = 1$ mA
REVERSE BREAKDOWN BV_R	40			V	-55°C	$I_R = 100$ μ A
	45	60		V	+25°C	$I_R = 100$ μ A
REVERSE CURRENT I_R		7	25	nA	+25°C	$V_R = 25$ V
			10	μ A	+125°C	$V_R = 25$ V
REVERSE RECOVERY t_{rr}		7	10	ns	+25°C	$I_F = 10$ mA to $I_R = 10$ mA Recovery to 1 mA
CROSSPOINT CAPACITANCE C_{cp}		1.9	4.0	pF	+25°C	$V_R = 5$ V, $f = 1$ MHz
COUPLING COEFFICIENT I_{CL}		20	50	μ A	+25°C	$I_{ADJ} = 20$ mA $V_{REV} = -5$ V

PERFORMANCE CURVES

(See Page Me-18 for Performance Characteristic Curves)

V_F	Figure 1
I_R	Figure 2
C_{cp}	Figure 5

MEMORY

MEDIUM RECOVERY MATRICES

HM-075	5 x 5	HM-051	10 x 4
HM-012	5 x 8	HM-081	8 x 5
HM-031	6 x 8	HM-091	4 x 10
HM-041	8 x 6		

ABSOLUTE MAXIMUM RATINGS

Forward Current	: 100 mA	Operating Temp. (ambient)	: -55°C to +125°C
Surge Current (100 μ s max.)	: 200 mA	Storage Temp. (ambient)	: -65°C to +150°C
Total Ckt. Dissipation (still air)	: 450 mW		

Maximum ratings are limiting values above which permanent circuit damage may occur.

ELECTRICAL CHARACTERISTICS

HM-012	HM-051	HM-081
HM-031	HM-075	HM-091
HM-041		

CHARACTERISTIC	LIMITS			UNIT	TEST CONDITIONS	
	MIN.	TYP.	MAX.		TEMP.	ELECTRICAL
FORWARD DROP V_{F20} V_{F1}			1.7	V	-55°C	$I_F = 20$ mA
		1.2	1.5	V	+25°C	$I_F = 20$ mA
			1.0	V	-55°C	$I_F = 1$ mA
		0.75	0.8	V	+25°C	$I_F = 1$ mA
REVERSE BREAKDOWN BV_R	35			V	-55°C	$I_R = 100$ μ A
	40	60		V	+25°C	$I_R = 100$ μ A
REVERSE CURRENT I_R		25	50	nA	+25°C	$V_R = 25$ V
			25	μ A	+125°C	$V_R = 25$ V
REVERSE RECOVERY t_{rr}		11	25	ns	+25°C	$I_F = 10$ mA to $I_R = 10$ mA Recovery to 1 mA
CROSSPOINT CAPACITANCE C_{cp}		1.9	4.0	pF	+25°C	$V_R = 5$ V, $f = 1$ MHz
COUPLING COEFFICIENT I_{CL}		20	50	μ A	+25°C	$I_{ADJ} = 20$ mA $V_{REV} = -5$ V

PERFORMANCE CURVES

(See Page Me-18 for Performance Characteristic Curves)

V_F	Figure 1
I_R	Figure 3
C_{cp}	Figure 5

MEMORY

GENERAL PURPOSE MATRICES

HM-077	5 x 5	HM-055	10 x 4
HM-013	5 x 8	HM-084	8 x 5
HM-034	6 x 8	HM-093	4 x 10
HM-044	8 x 6		

ABSOLUTE MAXIMUM RATINGS

Forward Current : 100 mA
 Surge Current (100 μ s max.) : 200 mA Operating Temp. (ambient) : -55°C to +125°C
 Total Ckt. Dissipation (still air) : 450 mW Storage Temp. (ambient) : -65°C to +150°C

Maximum ratings are limiting values above which permanent circuit damage may occur.

ELECTRICAL CHARACTERISTICS

HM-013 HM-055 HM-084
 HM-034 HM-077 HM-093
 HM-044

CHARACTERISTIC	LIMITS			UNIT	TEST CONDITIONS	
	MIN.	TYP.	MAX.		TEMP.	ELECTRICAL
FORWARD DROP V_{F20} V_{F1}			1.5	V	-55°C	$I_F = 20$ mA
		0.95	1.3	V	+25°C	$I_F = 20$ mA
			.95	V	-55°C	$I_F = 1$ mA
		0.7	.75	V	+25°C	$I_F = 1$ mA
REVERSE BREAKDOWN BV_R	30			V	-55°C	$I_R = 100$ μ A
	35	50		V	+25°C	$I_R = 100$ μ A
REVERSE CURRENT I_R		70	250	nA	+25°C	$V_R = 25$ V
			50	μ A	+125°C	$V_R = 25$ V
REVERSE RECOVERY t_{rr}		20	50	ns	+25°C	$I_F = 10$ mA to $I_R = 10$ mA Recovery to 1 mA
CROSSPOINT CAPACITANCE C_{cp}		2.0	4.0	pF	+25°C	$V_R = 5$ V, $f = 1$ MHz
COUPLING COEFFICIENT I_{CL}		20	50	μ A	+25°C	$I_{ADJ} = 20$ mA $V_{REV} = -5$ V

PERFORMANCE CURVES

(See Page Me-18 for Performance Characteristic Curves)

V_F	Figure 1
I_R	Figure 4
C_{cp}	Figure 5

TYPICAL PERFORMANCE CHARACTERISTICS

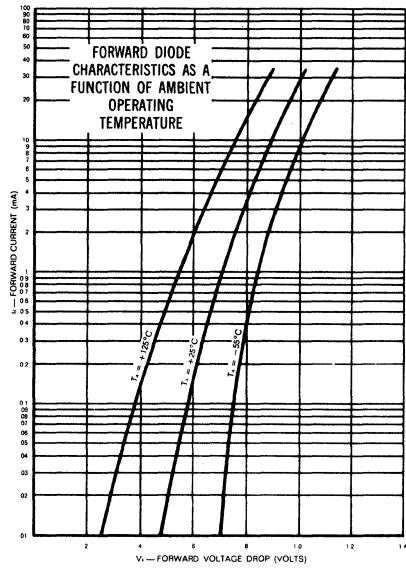


FIGURE 1

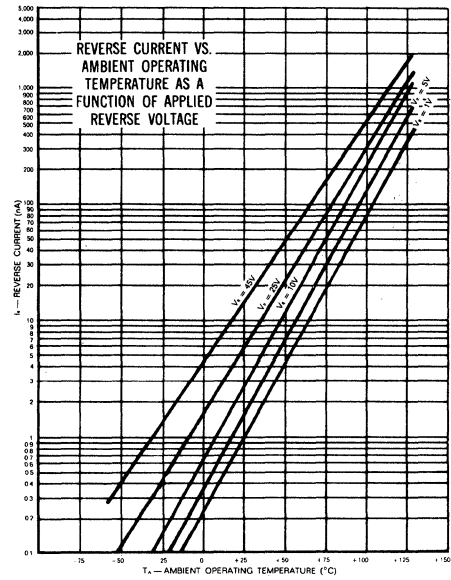


FIGURE 2

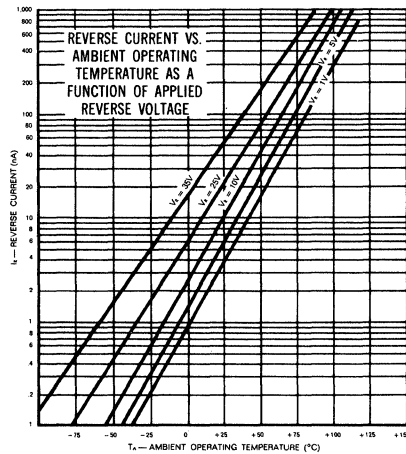


FIGURE 3

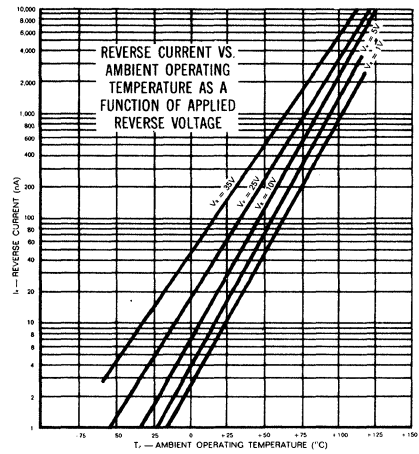


FIGURE 4

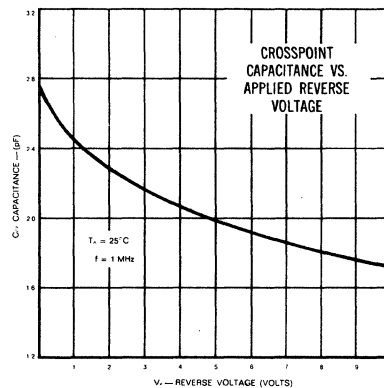
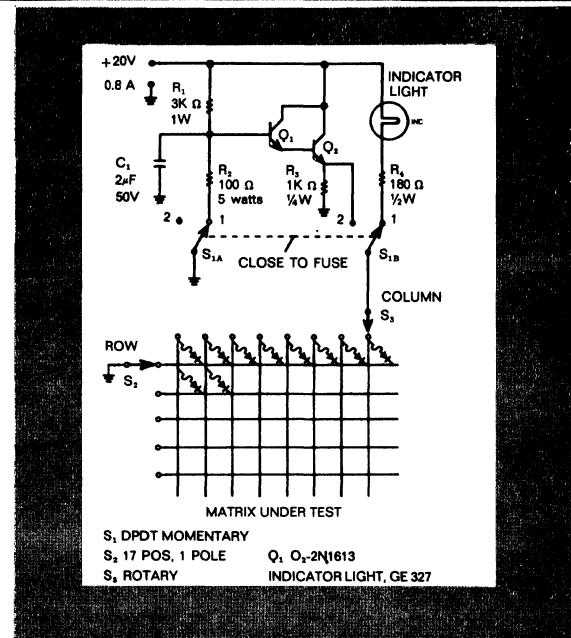


FIGURE 5

DIODE MATRIX FUSING

A simple ramp current generator is used to provide the fusing current. With switch S_{1A} in the position shown the capacitor C_1 is discharged to ground through R_2 . The diode to be eliminated is selected by setting the row and column switches S_2 and S_3 respectively as required. When switch S_{1A} is activated to position 2, capacitor C_1 charges up through R_1 forming a ramp voltage that drives the base of Q_1 . The darlington transistor pair of Q_1 and Q_2 transforms the voltage ramp to a current ramp that provides current to the column contacts on the matrix. This current, through the fuse, opens the fusible link in series with the selected diode. The peak fusing current required to open a fusible link, is approximately 750 milliamperes. As the temperature of the fuse is raised, the aluminum begins to melt. This melting continues until the fuse link separates. The cohesive forces of the melting aluminum retracts the remaining portions of the metal, thereby preventing formation of loose aluminum residues. The melting temperature of aluminum at approximately 650°C will not affect the passivating layer of silicon dioxide whose melting temperature is about 1350°C. Test verification is obtained by an indicating device placed in series with the column and row switches through the contacts S_{1B} to give visual indication of the condition of each diode in the matrix before and after fusing.



MONOLITHIC INTERFACE CIRCUITS

Harris interface circuits and monolithic diode matrices form a compatible family of integrated circuits to complement any logic design. These circuits in combination can perform

AND, OR, INVERT, AND-OR, NAND/NOR logic functions. The versatility of these circuits is unsurpassed when control, coding and decoding logic functions are performed.

PRODUCT SELECTION GUIDE FOR INTERFACE CIRCUITS

200/300 SERIES MILITARY -55°C to +125°C
TYPICAL CHARACTERISTICS AT $V_{CC} = 5.0V$ and $T_A = +25°C$

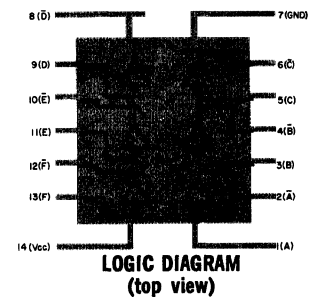
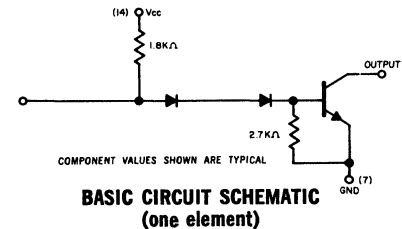
TYPE NUMBER	DESCRIPTION	FAN-OUT	t_{pd} (ns)	POWER DISSIPATION (mW)	NOTES
HD-234	Hex Interface Inverter	8	8	10	1
HD-235	Hex Interface Driver	35V	35	10	2

NOTE: Parts available in flat pack and dips

500 SERIES INDUSTRIAL 0°C to +75°C
TYPICAL CHARACTERISTICS AT $V_{CC} = 5.0V$ and $T_A = +25°C$

TYPE NUMBER	DESCRIPTION	FAN-OUT	t_{pd} (ns)	POWER DISSIPATION (mW)	NOTES
HD-534	Hex Interface Inverter	5	18	12	1
HD-535	Hex Interface Driver	35V	35	12	2

NOTE: Parts available in flat pack and dips



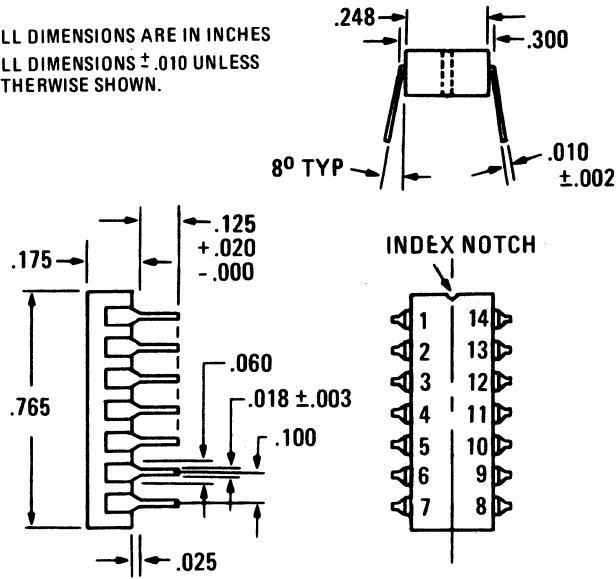
NOTES:

- 1.0 Fan-out is defined for Harris DTL logic of the same series number.
- 2.0 Voltage given in fan-out column is the minimum output breakdown voltage for this gate element.

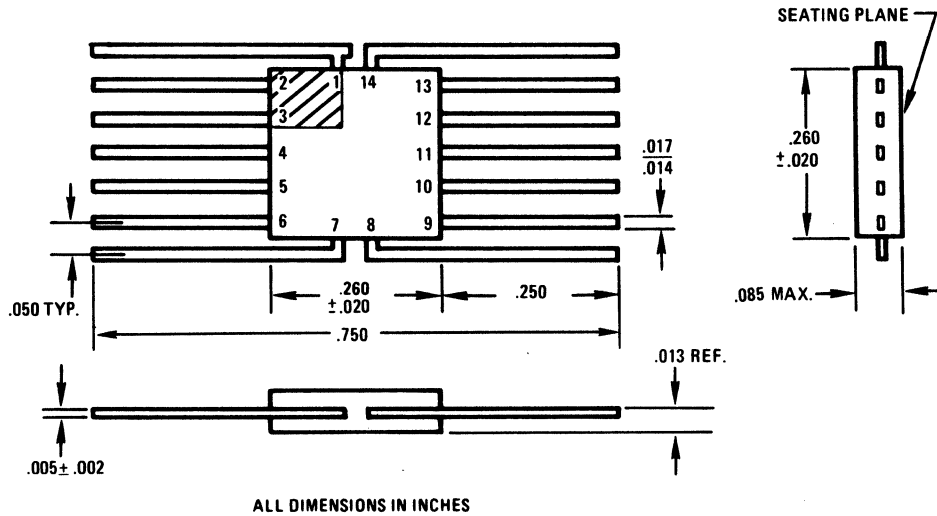
PACKAGING

CODE 1A TO-116(14 LEAD CERAMIC D.I.P.)

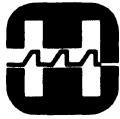
ALL DIMENSIONS ARE IN INCHES
ALL DIMENSIONS $\pm .010$ UNLESS OTHERWISE SHOWN.



CODE 9H TO-86 (CERAMIC)



MEMORY



HARRIS
SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HM-0110 (4x10)
HM-0168 (6x 8)
HM-0104 (10x 4)
HM-0186 (8x 6)

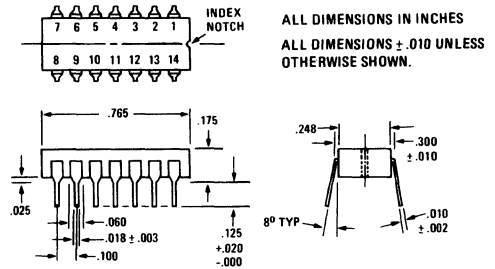
Commercial Diode Matrices

DESCRIPTION

The commercial diode matrices are arrays of passivated silicon diodes, fabricated in dielectrically isolated moats. An epitaxial layer is used as the common cathode connection for all diodes in a row. Column connections to the anode side of the diodes are made through metal interconnect lines via fusible links. By selectively opening the links, diodes can be removed from the circuit to form any desired matrix pattern. This device is available in a 14-lead dual in-line CERDIP package. These parts are also available in a Mil-Temperature performance range.

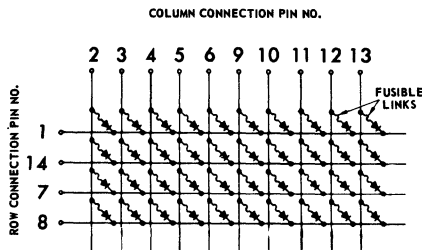
PACKAGE

CODE 1A TO-116(14 LEAD CERAMIC D.I.P)

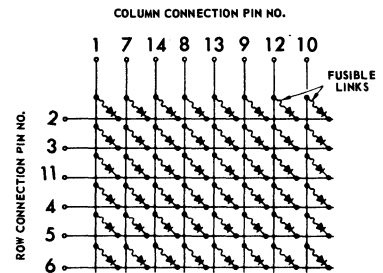


MATRIX PATTERNS

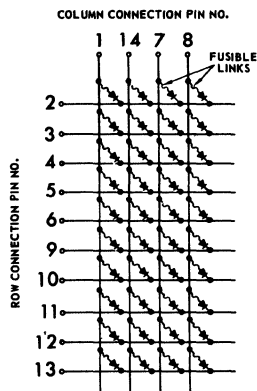
HM-0110
(4 x 10)



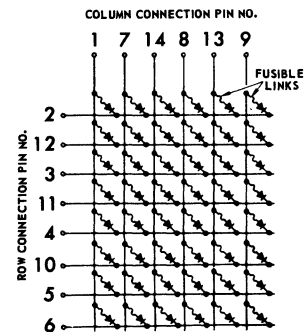
HM-0168
(6 x 8)



HM-0104
(10 x 4)



HM-0186
(8 x 6)



When ordering a matrix with a custom pattern take a matrix pattern and circle out those diodes to be removed from the matrix. Another method to clearly identify pattern is to call out row and column pins for each diode to be removed.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

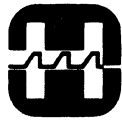
Forward Current	100mA
Surge Current (100 μ s Max.)	200mA
Total Circuit Dissipation (Still Air)	450mW
Operating Temperature (Ambient)	0°C to 70°C

ELECTRICAL CHARACTERISTICS AT 25°C

CHARACTERISTIC		HM1-0104 (10 x 4) HM1-0168 (6 x 8) HM1-0186 (8 x 6)		HM1-0110 (4 x 10)		CONDITIONS
		LIMITS		LIMITS		
		MIN.	MAX.	MIN.	MAX.	
Forward Drop	V_{F20}		1.5V		1.8V	$I_F = 20mA$
Forward Drop	V_{F1}		0.9V		1.0V	$I_F = 1mA$
Rev. Breakdown Volt.	BV_R	20V		20V		$I_R = 100\mu A$
Rev. Current	I_R		1 μA		1 μA	$V_R = 15V$
Rev. Rec. Time			100ns		100ns	$I_F = 10mA$ $I_R = 10mA$ to 1mA
Coupling Capacitance	C_{CP}		8pF		8pF	$V_R = 5V$ $f = 1MHz$

NOTE: When ordering a matrix with a custom pattern either obtain copies of Harris patternizing forms from your local sales representative or contact headquarters, Marketing, Melbourne, Florida.

On all orders less than 100 units there will be a one time charge for each special pattern formed by Harris.



HARRIS
SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HM-7202

1024 x 1 N-Channel MOS RAM

FEATURES

- MIL And Commercial Versions
- Access Times From 350 TO 1000 NS
- Static - Easy To Use
- 1024 x 1 Organization
- Pinout Compatible With Industry Standard 2102
- Single +5V Power Supply
- TTL Compatible I/O
- No Clocks, No Refresh
- Two TTL Loads
- Three-State Output
- Output Can Be Or -Tied
- Inputs Protected From Static Change

DESCRIPTION

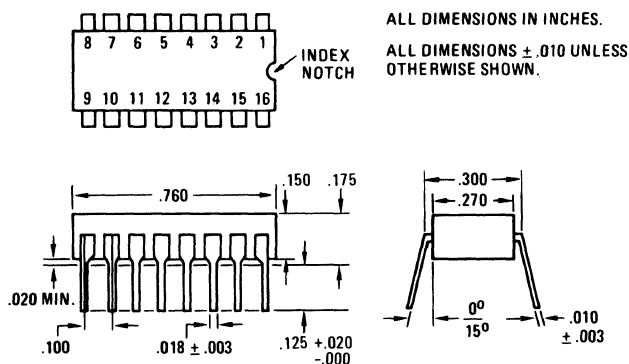
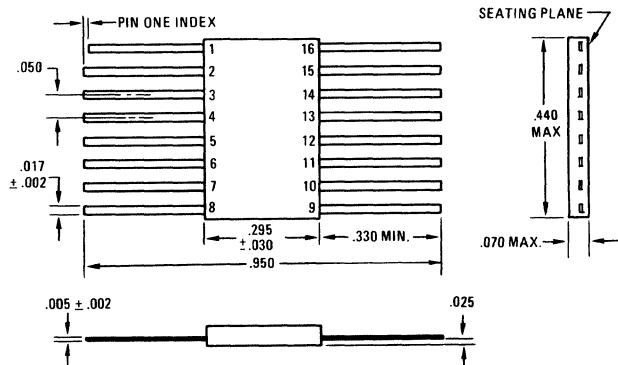
The HM-7202 is a 1024 Word X 1-Bit static N-Channel Random Access Read/Write Memory. Its TTL-Compatible I/O, single +5V supply, and static circuitry allow ease of operation without refresh or clocking.

Data Out is non-inverted from Data In.

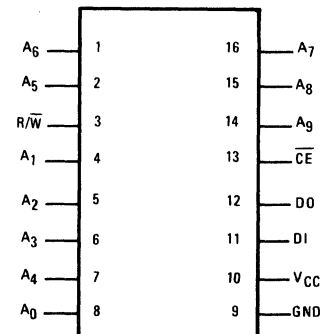
A chip select and three-state output allow easy memory array expansion. Input protection and 2 full TTL load drive capability round out the features of this easy-to-use device.

The HM-7202 is compatible with the industry standard 2102-type devices, and is available in commercial and military temperature range, in a number of speed categories.

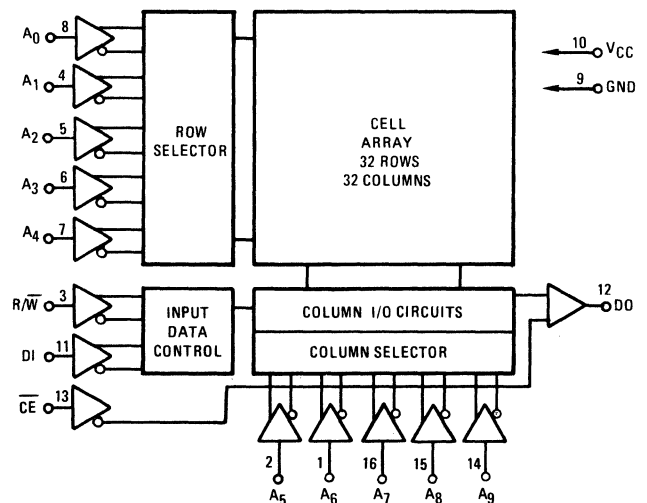
PACKAGING



PINOUT



BLOCK DIAGRAM



MEMORY

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Storage Temperature:	-65°C to +150°C	V _{CC} To Ground (Continuous):	-0.5V to +7.0V
Ambient Operating Temperature:	0°C to +70°C (7202-5) -55°C to +125°C (7202-2)	Voltage To Ground On Any Input Or Output:	-0.5V to +7.0V
Maximum Power Dissipation:	500mW	Maximum Current Into Output	±50mA

ELECTRICAL CHARACTERISTICS:

NOTE: V_{CC} = +5.0V ±5% (7202-5)
V_{CC} = +5.0V ±10% (7202-2)

PARAMETER	SYMBOL	HM-7202-5			HM-7202-2			UNITS	CONDITIONS
		T _A = 0°C To +70°C			T _A = -55°C To +125°C				
		MIN	TYP	MAX	MIN	TYP	MAX		
Address/Enable Forward Current	"1"	I _{FA}		10			10	μA	V _{in} = V _{CC} + 0.5V
	"1"	I _{FE}		10			10		
Address/Enable Reverse Current	"0"	I _{RA}		-10			-10	μA	V _{in} = 0
	"0"	I _{RE}		-10			-10		
Input Threshold Voltage	"1"	V _{IH}	2.0		2.0			V	V _{CC} = V _{CC} Min V _{CC} = V _{CC} Max
	"0"	V _{IL}		0.65			0.65		
Output Voltage (Three-State)	"1"	V _{OH}	2.4		2.4			V	I _{OH} = -0.2ma I _{OL} = 3.2ma
	"0"	V _{OL}		0.45			0.45		
Output Leakage	"1"	I _{OHL}		10			10	μA	V _{CE} = +2.0V V _{OUT} = V _{CC} + 0.5V
Current, Deselected	"0"	I _{OLL}		-10			-10	μA	V _{CE} = +2.0V V _{OUT} = 0
Power Supply Current		I _{CC}		50			50	mA	All Inputs = V _{CC} Max V _{CC} = V _{CC} Max Static: Output = high impedance

D.C.

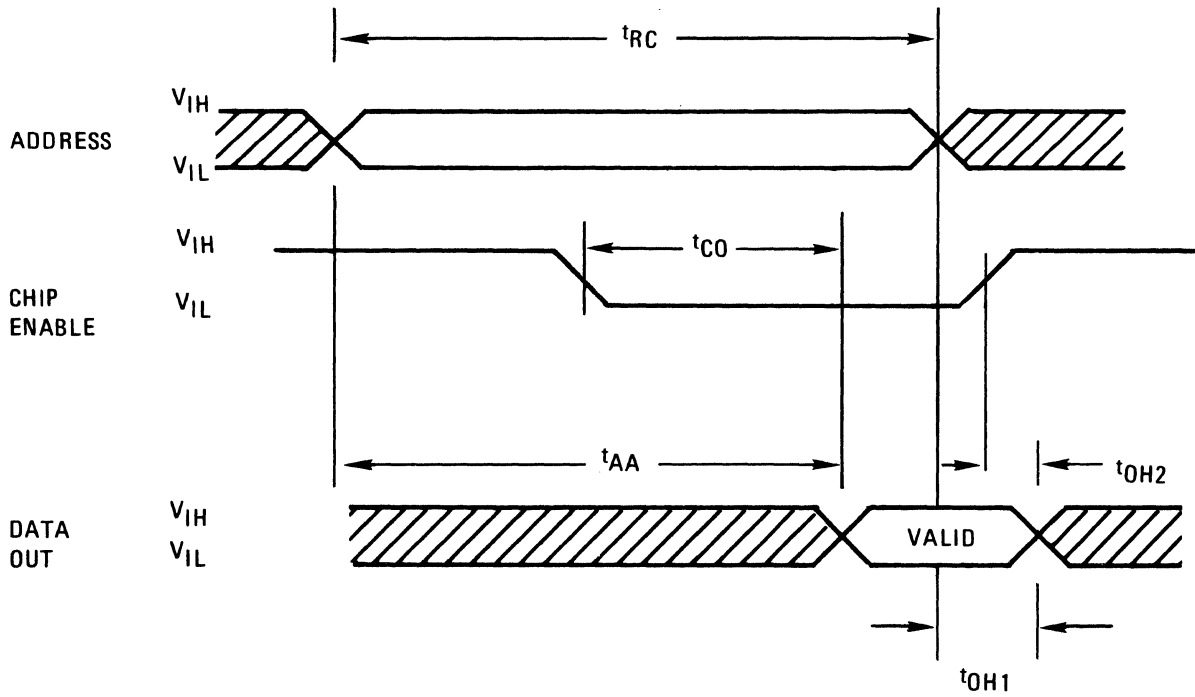
MEMORY

PARAMETER	SYMBOL	MIL/COMM HM-7202		MIL/COMM HM-7202A		MIL/COMM HM-7202B		MIL HM-7202C		COMM HM-7202C		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
READ CYCLE:													
Address Access Time	t _{AA}		1000		650		500		400		350	NS	C _L = 50pF
Chip Enable Access Time	t _{CO}		500		400		350		300		180	NS	
Address-Output Hold Time	t _{OH1}	50		50		50		50		40		NS	Reference = 1.5V
CE-Output Hold Time	t _{OH2}	0		0		0		0		0		NS	Input Pulse Levels +0.65V to +2.2V
Read Cycle Time	t _{RC}	1000		650		500		400		350		NS	
WRITE CYCLE:													
Address Write Setup Time	t _{AW}	200		200		150		120		20		NS	t _R = t _F = 20NS
Write Pulse Width Time	t _{WP}	750		400		300		220		200		NS	
Write Recovery Time	t _{WR}	50		50		50		50		50		NS	
Data Setup Time	t _{DW}	800		450		330		250		250		NS	
Data Hold Time	t _{DH}	100		100		100		100		50		NS	
CE-Write Setup Time	t _{CW}	900		550		400		300		250		NS	
Write Cycle Time	t _{WC}	1000		650		500		400		350		NS	

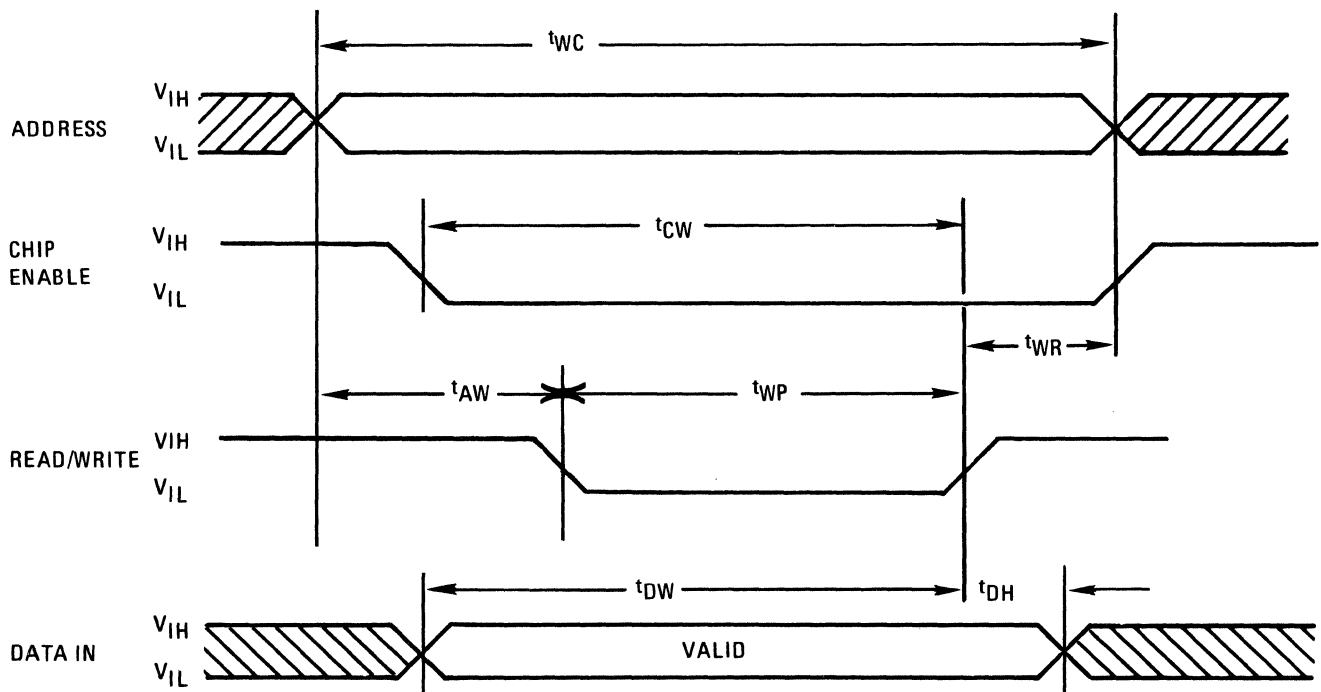
A.C.

TEST CHARACTERISTICS

READ CYCLE



WRITE CYCLE



CAPACITANCE

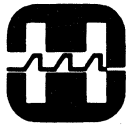
FUNCTION	SYMBOL	CONDITIONS	TYP	MAX	LIMITS ⁽¹⁾
Address Input	C_A		3	5	pF
Read/Write	$C_{R/W}$	$V_{CC} = +5.0V; T_A = +25^{\circ}C$	7	10	pF
Input/Output	$C_{I/O}$	$V_T = 0V; f = 1MHz$	7	10	pF

NOTE 1. Capacitance is guaranteed, and sampled, but is not 100% tested.

HARRIS GENERIC PROM PRODUCT CHART

ORGANIZATION	PART NUMBER	OUTPUT TYPE	PINOUT	MAXIMUM ACCESS OVER VOLTAGE AND TEMP.	TYPICAL PROGRAMMING TIME (ALL BITS)																																																
256 X 4	HM-7610 HM-7611	(OC) (TS)	<table border="1" style="display: inline-table; border-collapse: collapse;"> <tr><td>A6</td><td>1</td><td>16</td><td>VCC</td></tr> <tr><td>A5</td><td>2</td><td>15</td><td>A7</td></tr> <tr><td>A4</td><td>3</td><td>14</td><td>$\overline{CS2}$</td></tr> <tr><td>A3</td><td>4</td><td>13</td><td>$\overline{CS1}$</td></tr> <tr><td>A0</td><td>5</td><td>12</td><td>O1</td></tr> <tr><td>A1</td><td>6</td><td>11</td><td>O2</td></tr> <tr><td>A2</td><td>7</td><td>10</td><td>O3</td></tr> <tr><td>GND</td><td>8</td><td>9</td><td>O4</td></tr> </table>	A6	1	16	VCC	A5	2	15	A7	A4	3	14	$\overline{CS2}$	A3	4	13	$\overline{CS1}$	A0	5	12	O1	A1	6	11	O2	A2	7	10	O3	GND	8	9	O4	60ns	1 SECOND																
A6	1	16	VCC																																																		
A5	2	15	A7																																																		
A4	3	14	$\overline{CS2}$																																																		
A3	4	13	$\overline{CS1}$																																																		
A0	5	12	O1																																																		
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GND	8	9	O4																																																		
512 X 4	HM-7620 HM-7621	(OC) (TS)	<table border="1" style="display: inline-table; border-collapse: collapse;"> <tr><td>A6</td><td>1</td><td>16</td><td>VCC</td></tr> <tr><td>A5</td><td>2</td><td>15</td><td>A7</td></tr> <tr><td>A4</td><td>3</td><td>14</td><td>A8</td></tr> <tr><td>A3</td><td>4</td><td>13</td><td>$\overline{CS1}$</td></tr> <tr><td>A0</td><td>5</td><td>12</td><td>O1</td></tr> <tr><td>A1</td><td>6</td><td>11</td><td>O2</td></tr> <tr><td>A2</td><td>7</td><td>10</td><td>O3</td></tr> <tr><td>GND</td><td>8</td><td>9</td><td>O4</td></tr> </table>	A6	1	16	VCC	A5	2	15	A7	A4	3	14	A8	A3	4	13	$\overline{CS1}$	A0	5	12	O1	A1	6	11	O2	A2	7	10	O3	GND	8	9	O4	70ns	2 SECONDS																
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GND	8	9	O4																																																		
512 X 8	HM-7640 HM-7641	(OC) (TS)	<table border="1" style="display: inline-table; border-collapse: collapse;"> <tr><td>A7</td><td>1</td><td>24</td><td>VCC</td></tr> <tr><td>A6</td><td>2</td><td>23</td><td>A8</td></tr> <tr><td>A5</td><td>3</td><td>22</td><td>NC</td></tr> <tr><td>A4</td><td>4</td><td>21</td><td>$\overline{CS1}$</td></tr> <tr><td>A3</td><td>5</td><td>20</td><td>$\overline{CS2}$</td></tr> <tr><td>A2</td><td>6</td><td>19</td><td>CS3</td></tr> <tr><td>A1</td><td>7</td><td>18</td><td>CS4</td></tr> <tr><td>A0</td><td>8</td><td>17</td><td>O8</td></tr> <tr><td>O1</td><td>9</td><td>16</td><td>O7</td></tr> <tr><td>O2</td><td>10</td><td>15</td><td>O6</td></tr> <tr><td>O3</td><td>11</td><td>14</td><td>O5</td></tr> <tr><td>GND</td><td>12</td><td>13</td><td>O4</td></tr> </table>	A7	1	24	VCC	A6	2	23	A8	A5	3	22	NC	A4	4	21	$\overline{CS1}$	A3	5	20	$\overline{CS2}$	A2	6	19	CS3	A1	7	18	CS4	A0	8	17	O8	O1	9	16	O7	O2	10	15	O6	O3	11	14	O5	GND	12	13	O4	70ns	4 SECONDS
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1024 X 4	HM-7644	ACTIVE PULLUP	<table border="1" style="display: inline-table; border-collapse: collapse;"> <tr><td>A6</td><td>1</td><td>16</td><td>VCC</td></tr> <tr><td>A5</td><td>2</td><td>15</td><td>A7</td></tr> <tr><td>A4</td><td>3</td><td>14</td><td>A8</td></tr> <tr><td>A3</td><td>4</td><td>13</td><td>A9</td></tr> <tr><td>A0</td><td>5</td><td>12</td><td>O1</td></tr> <tr><td>A1</td><td>6</td><td>11</td><td>O2</td></tr> <tr><td>A2</td><td>7</td><td>10</td><td>O3</td></tr> <tr><td>GND</td><td>8</td><td>9</td><td>O4</td></tr> </table>	A6	1	16	VCC	A5	2	15	A7	A4	3	14	A8	A3	4	13	A9	A0	5	12	O1	A1	6	11	O2	A2	7	10	O3	GND	8	9	O4	70ns	4 SECONDS																
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A2	7	10	O3																																																		
GND	8	9	O4																																																		
1024 X 4	HM-7642 HM-7643	(OC) (TS)	<table border="1" style="display: inline-table; border-collapse: collapse;"> <tr><td>A6</td><td>1</td><td>18</td><td>VCC</td></tr> <tr><td>A5</td><td>2</td><td>17</td><td>A7</td></tr> <tr><td>A4</td><td>3</td><td>16</td><td>A8</td></tr> <tr><td>A3</td><td>4</td><td>15</td><td>A9</td></tr> <tr><td>A0</td><td>5</td><td>14</td><td>O1</td></tr> <tr><td>A1</td><td>6</td><td>13</td><td>O2</td></tr> <tr><td>A2</td><td>7</td><td>12</td><td>O3</td></tr> <tr><td>$\overline{CS1}$</td><td>8</td><td>11</td><td>O4</td></tr> <tr><td>GND</td><td>9</td><td>10</td><td>$\overline{CS2}$</td></tr> </table>	A6	1	18	VCC	A5	2	17	A7	A4	3	16	A8	A3	4	15	A9	A0	5	14	O1	A1	6	13	O2	A2	7	12	O3	$\overline{CS1}$	8	11	O4	GND	9	10	$\overline{CS2}$	70ns	4 SECONDS												
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$\overline{CS1}$	8	11	O4																																																		
GND	9	10	$\overline{CS2}$																																																		
32 X 8	HM-7602 HM-7603	(OC) (TS)	<table border="1" style="display: inline-table; border-collapse: collapse;"> <tr><td>O1</td><td>1</td><td>16</td><td>VCC</td></tr> <tr><td>O2</td><td>2</td><td>15</td><td>\overline{CS}</td></tr> <tr><td>O3</td><td>3</td><td>14</td><td>A4</td></tr> <tr><td>O4</td><td>4</td><td>13</td><td>A3</td></tr> <tr><td>O5</td><td>5</td><td>12</td><td>A2</td></tr> <tr><td>O6</td><td>6</td><td>11</td><td>A1</td></tr> <tr><td>O7</td><td>7</td><td>10</td><td>A0</td></tr> <tr><td>GND</td><td>8</td><td>9</td><td>O8</td></tr> </table>	O1	1	16	VCC	O2	2	15	\overline{CS}	O3	3	14	A4	O4	4	13	A3	O5	5	12	A2	O6	6	11	A1	O7	7	10	A0	GND	8	9	O8	40nsec	<1 SECOND																
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GND	8	9	O8																																																		

MEMORY



HARRIS
SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HM-7602/7603

256-Bit Field Programmable Bipolar PROM

FEATURES

- 32 Words, 8-Bits per Word
- Simple, High Speed Programming Procedure (less than 1 second Typical)
- Inputs and Outputs TTL Compatible
 - ▶ Low Input Current – 400 μ A Logic "0", 40 μ A "1"
 - ▶ Full Output Drive – 15mA Sink/2mA Source
- Fast Access Time – 40ns Over Commercial Temperature and Voltage; 50ns Over Military Temperature and Voltage
- Expandable – "Wired-Or" Outputs with Chip Select

DESCRIPTION

The HM-7602 (open collector) and HM-7603 (three-state) are fully decoded, high speed, 256-bit programmable ROM'S organized as 32 words by 8-bits per word. They are supplied with all bits storing a logical "1" (outputs high), and can be selectively programmed for a logical "0" (outputs low).

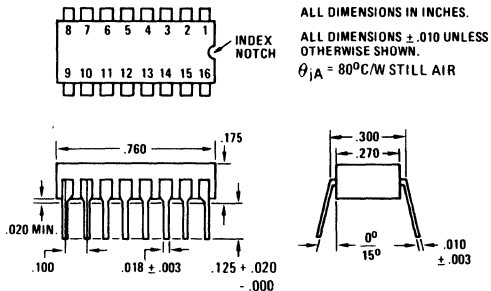
The nichrome fuse technology is the same as is used in the JAN approved MIL 38510/201 PROM, and in all other Harris PROMS.

The field programmable PROM can be custom programmed to any pattern using a simple programming procedure. Schottky Bipolar circuitry provides extremely fast access time, and features temperature and voltage compensation to minimize variations in access time.

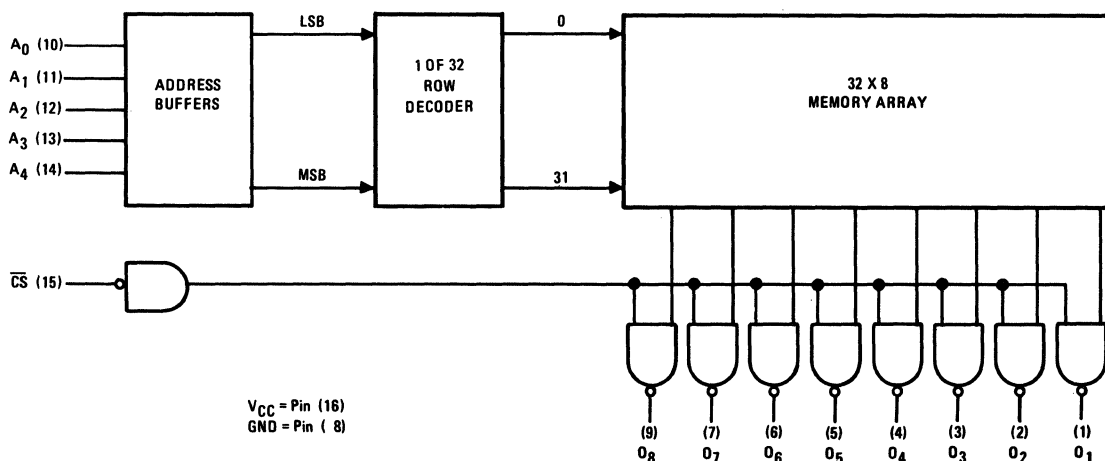
In addition to the conventional storage array, two test rows and one test column are included to assure high programmability, and guarantee parametric and A.C. performance. Fuses in these test rows and columns are blown prior to shipment.

PACKAGE

CODE 1D



BLOCK DIAGRAM



MEMORY

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	7.0V
Address/Enable Input Voltage	5.5V
Address/Enable Input Current	-20mA
Output Sink Current	70mA
Storage Temperature	+150°C
Operating Temperature (Ambient)	+125°C
Maximum Junction Temperature	+175°C

Stresses above those listed under the "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

ELECTRICAL CHARACTERISTICS (OPERATING)

PARAMETER	SYMBOL	HM-7602-5			HM-7603-5			UNITS	TEST CONDITIONS
		5V ±5%			5V ±5%				
		0°C to +70°C			0°C to +70°C				
Address/Enable Input Current	"1" "0"	I_{RA}, I_{RE} I_{FA}, I_{FE}	0 -0.1	40 -0.4	0 -0.1	40 -0.4	μA mA	$V_{IH} = V_{CC} \text{ Max}$ $V_{IL} = 0.45V$	
Input Threshold Voltage	"1" "0"	V_{IH} V_{IL}	2.0	0.8	2.0	0.8	V	$V_{CC} = V_{CC} \text{ Min}$ $V_{CC} = V_{CC} \text{ Max}$	
Output Voltage	"1" "0"	V_{OH} V_{OL}	N/A 0.35	0.45	2.4 0.35	3.4 0.45	V	$I_{OH} = -2.0mA, V_{CC} = V_{CC} \text{ Min}$ $I_{OL} = +15mA, V_{CC} = V_{CC} \text{ Min}$ $V = V_{CS} = 0.8V$	
Output Disabled Current	"1" "0"	I_{OHE} I_{OLE}		100 N/A		100 -100	μA μA	$V_{OH}, V_{CC} = V_{CC} \text{ max}$ $V_{OL} = +0.3V, V_{CC} = V_{CC} \text{ Max}$ $V = V_{CS} = 2.0V$	
Output Leakage	"1"	I_{OH}		100		N/A	μA	$V_{OH}, V_{CC} = V_{CC} \text{ Max}$	
Power Supply Current		I_{CC}	90	130	90	130	mA	$V_{CC} = V_{CC} \text{ Max}$ All Inputs Grounded	
Input Clamp Voltage		V_{CL}		-1.5		-1.5	V	$I_{in} = -10ma$	
Output Short Circuit Current		I_{OS}	N/A	N/A	15	23	30	mA	$V_{CC} = V_{CC} \text{ Max}, V_{OUT} = 0.0V$ One output only for a Max of 1 sec
Address Access Time		t_{AA}	25	40	25	40	ns	V_{CC} and T_A Over Full Range	
Enable Access Time		t_{EA}	20	30	20	30	ns	V_{CC} and T_A Over Full Range	

Typical Measurements are at $T_A = 25^\circ C, V_{CC} = +5V$

PARAMETER	SYMBOL	HM-7602-2			HM-7603-2			UNITS	TEST CONDITIONS
		5V ±10%			5V ±10%				
		-55°C to +125°C			-55°C to +125°C				
Address/Enable Input Current	"1" "0"	I_{RA}, I_{RE} I_{FA}, I_{FE}	0 -0.1	40 -0.4	0 -0.1	40 -0.4	μA mA	$V_{IH} = V_{CC} \text{ Max}$ $V_{IL} = 0.45V$	
Input Threshold Voltage	"1" "0"	V_{IH} V_{IL}	2.0	0.8	2.0	0.8	V	$V_{CC} = V_{CC} \text{ Min}$ $V_{CC} = V_{CC} \text{ Max}$	
Output Voltage	"1" "0"	V_{OH} V_{OL}	N/A 0.35	0.45	2.4 0.35	3.4 0.45	V	$I_{OH} = -2.0mA; V_{CC} = V_{CC} \text{ Min}$ $I_{OL} = +15mA; V_{CC} = V_{CC} \text{ Min}$ $V = V_{CS} = 0.8V$	
Output Disabled Current	"1" "0"	I_{OHE} I_{OLE}		100 N/A		100 -100	μA μA	$V_{OH}, V_{CC} = V_{CC} \text{ Max}$ $V_{OL} = +0.3V, V_{CC} = V_{CC} \text{ Max}$ $V = V_{CS} = 2.0V$	
Output Leakage	"1"	I_{OH}		100		N/A	μA	$V_{OH}, V_{CC} = V_{CC} \text{ Max}$	
Power Supply Current		I_{CC}	90	130	90	130	mA	$V_{CC} = V_{CC} \text{ Max}$ All Inputs Grounded	
Input Clamp Voltage		V_{CL}		-1.5		-1.5	V	$I_{in} = -10ma$	
Output Short Circuit Current		I_{OS}	N/A	N/A	15	23	30	mA	$V_{CC} = V_{CC} \text{ Max}, V_{OUT} = 0.0V$ One output only for a Max of 1 sec
Address Access Time		t_{AA}	25	50	25	50	ns	V_{CC} and T_A Over Full Range	
Enable Access Time		t_{EA}	20	35	20	35	ns	V_{CC} and T_A Over Full Range	

Typical Measurements are at $T_A = 25^\circ C, V_{CC} = +5V$

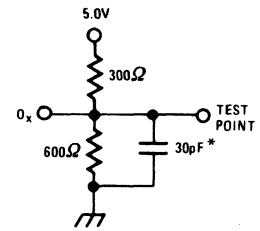
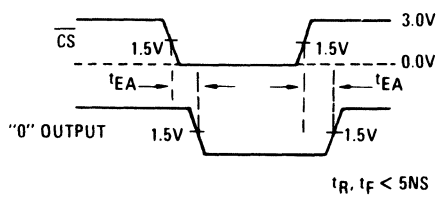
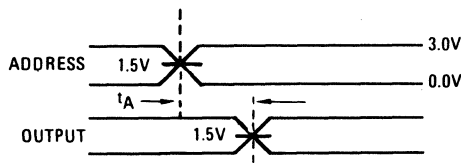
CAPACITANCE (1): $T_A = 25^\circ C$

PARAMETER	SYMBOL	TYP.	UNITS	TEST CONDITION
Add. Input Cap.	$C_{IN A, CS}$	8	pF	$V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz$
Output Cap.	C_{OUT}	8	pF	$V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz$

NOTE: (1) These parameters are only periodically sampled and are not 100% tested.

SWITCHING TIME DEFINITIONS

A.C. TEST LOAD



*Includes jig & probe total capacitance

PROGRAMMING

The HM-7602/7603 is manufactured with all bits/outputs Logical "1" (Output High). Any desired bit/output can be programmed to a Logical "0" (Output Low) by following the simple procedure shown below. One may build his own programmer to satisfy the specifications described in Table 1, or buy any of the commercially available programmers which meet these specifications. The HM-7602/7603 can be programmed automatically or by the manual procedure shown below.

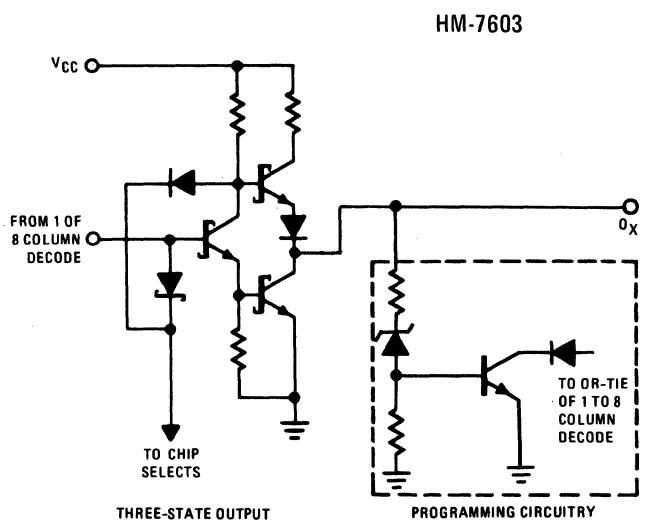
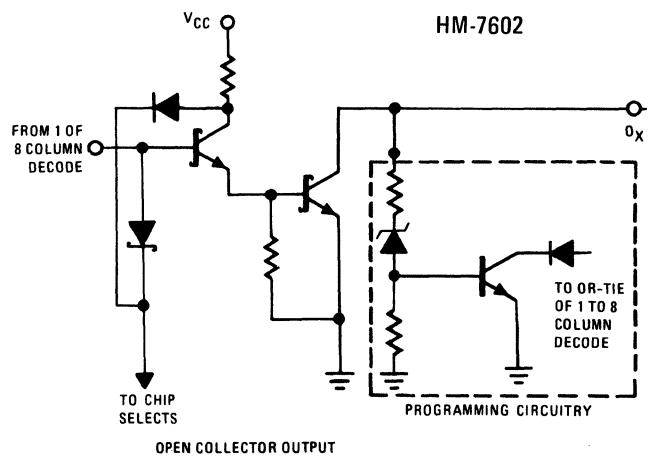
PROGRAMMING SPECIFICATIONS

TABLE 1

PARAMETER	SYMBOL	MIN.	RECOM-MEND VALUE	MAX.	UNITS
Address Input Voltage (1)	V_{IH}	2.4	5.0	5.0	V
	V_{IL}	0.0	0.4	0.8	V
Programming/Verify Voltage to V_{CC} (2)	V_{PH}	11.5	12.0	12.5	V
	V_{PL}	3.75	4.0	4.25	V
Programming Voltage Current Limit	I_{CCP}			600	mA
Programming (V_{CC}) Voltage Rise and Fall Time	t_r	1	1	10	μs
	t_f	1	1	10	μs
Programming Delay	t_d	10	10	100	μs
Programming Pulse Width - First Attempts	t_{p1}	100	100	200	μs
Programming Pulse Width - Subsequent	t_{p2}	10	10	20	ms
Programming Duty Cycle	D.C.	-	10	10	%
Output Voltage Enable Disable (3)	V_{OPE}	9.5	10.0	10.5	V
	V_{OPD}	0	.45	5.5	V
Output Voltage Enable Current Limit	I_{OPE}			10	mA
Case Temp	T_C			75	$^{\circ}C$

1. Address and chip select should not be left open for V_{IH} .
2. Verification at $V_{CC} = 4.0 \pm .25$ Volts, $T_A = 25^{\circ}C$ is recommended to guardband performance over full temperature and voltage range.
3. Disable condition will be met with output open circuit.

SCHEMATIC DIAGRAMS



MEMORY

PROGRAMMING PROCEDURE

1. Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL compatible. An open circuit should not be used to address the PROM.
2. Disable the chip by applying input highs (V_{IH}) to the chip select input. The chip select input is TTL compatible. An open circuit should not be used to disable the chip.
3. Disable the programming circuitry by applying an Output Voltage Disable of less than V_{OPD} to the output of the PROM. The output may be left open circuit to achieve the disable.
4. Raise V_{CC} to V_{PH} with rise time equal to t_r .
5. After a delay equal to or greater than t_d , apply a pulse with amplitude equal to V_{OPE} and duration of t_{p1} to the output selected for programming. Note that the PROM is supplied with fuses intact generating an output high. Programming a fuse will cause the output to go low in the verify mode.
6. Other bits in the same word may be programmed while the V_{CC} input is raised to V_{PH} by applying output

enable pulses to each output which is to be programmed. The output enable pulses must be separated by a minimum interval of t_d .

7. Lower V_{CC} to $4.0 \pm .25$ Volts following a delay to t_d from the last programming enable pulse applied to an output.
8. Enable the PROM for verification by applying a logic "0" (V_{IL}) to the \overline{CS} input.
9. If any bit does not verify as programmed, repeat steps 2 through 8 using an output pulse enable width of t_{p1} for up to 15 additional pulses to enhance programming speed. If the bit is still unprogrammed, follow with at least 16 repetitive pulses of t_{p2} in width, to achieve high programming yield. In the event that the bit is still unprogrammed, the part is considered a programming reject and should be returned to the factory. The address and incorrect and desired contents of a location in which a programming failure has occurred in any returned device must be included with that return.
10. Repeat steps 1 thru 9 for all other bits to be programmed in the PROM.

RECOMMENDED PROGRAMMING CIRCUIT

The circuit and timing diagram shown in Figures 1 and 2 will establish the proper programming condition for the output enable pulse. This allows the use of standard TTL parts for all logic inputs to the PROM. Note the gate which senses the output must be input protected to withstand input up to 12.5 Volts during programming.

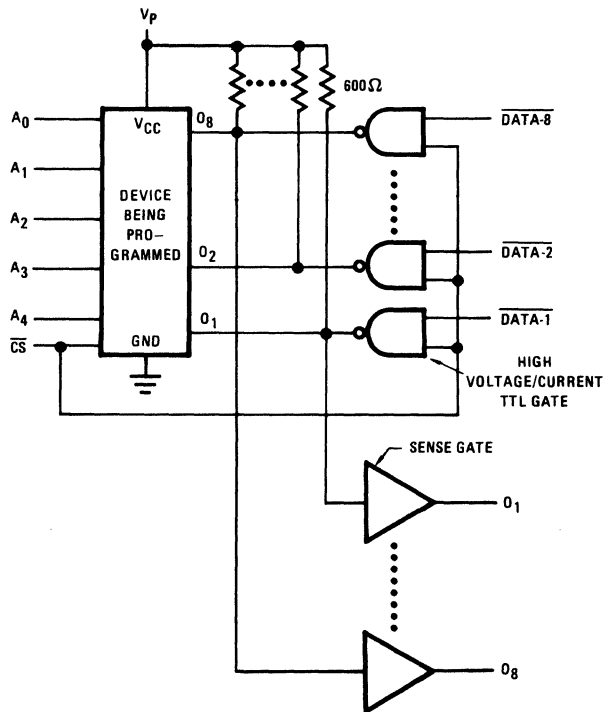


FIGURE 1

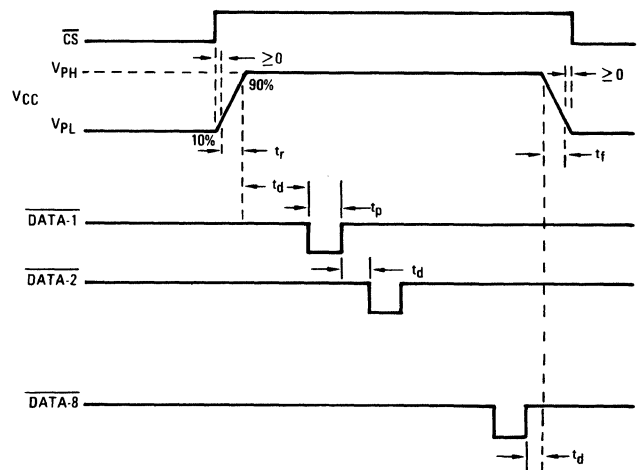


FIGURE 2



HARRIS
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HM-7610/7611

1024-Bit Field Programmable Bipolar PROM

FEATURES

- 256 Words, 4-Bits per Word
- Simple, High Speed Programming Procedure (less Than 1 Second Typical)
- Inputs and Outputs TTL Compatible
 - ▶ Low Input Current -400 μ A Logic "0", 40 μ A Logic "1"
 - ▶ Full Output Drive -15mA Sink/2mA Source
- Fast Access Time-60NS Over Commercial Temperature & Voltage, 75NS Over Military Temperature & Voltage
- Expandable - "Wired-Or" Outputs With Chip Select
- Pin Compatible With Industry Standard 256 X 4 Proms

DESCRIPTION

The HM-7610 (open collector) and HM-7611 (three-state) are fully decoded, high speed, 1024-bit programmable ROM'S organized as 256 words by 4 bits per word. They are supplied with all bits storing a logical "1" (outputs high), and can be selectively programmed for a logical "0" (outputs low).

The nichrome fuse technology is the same as is used in the JAN approved MIL 38510/201 PROM, and in all other Harris PROMS.

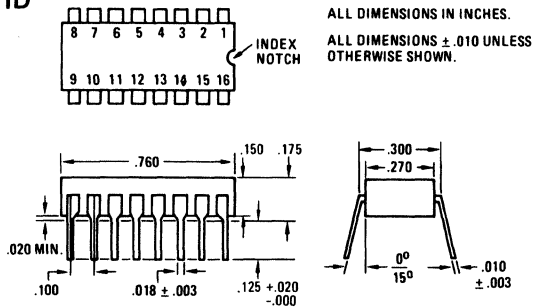
The field programmable PROM can be custom programmed to any pattern using a simple programming procedure. Schottky Bipolar circuitry provides extremely fast access time, and features temperature and voltage compensation to minimize variations in access time.

The pinout is compatible with the industry standard 256X4 PROM.

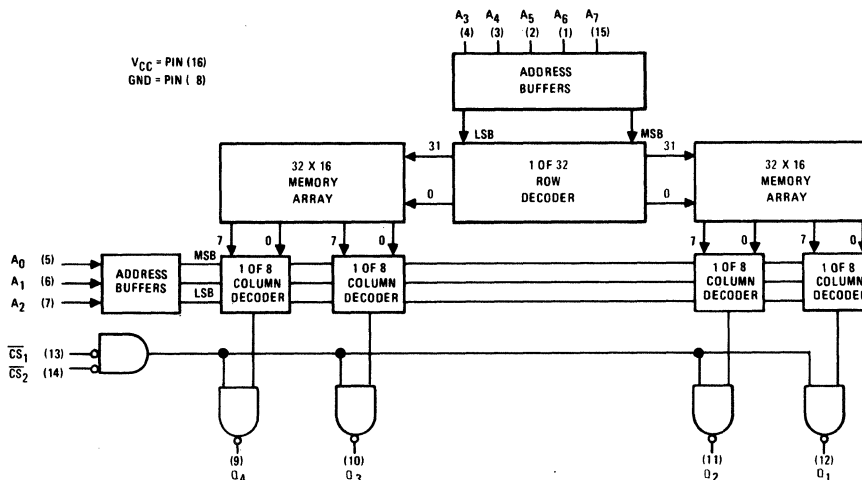
In addition to the conventional storage array, two test rows and two test columns are included to assure high programmability, and guarantee parametric and A.C. performance. Fuses in these test rows and columns are blown prior to shipment.

PACKAGE

CODE 1D



BLOCK DIAGRAM



MEMORY

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	7.0V
Address/Enable Input Voltage	5.5V
Address/Enable Input Current	-20mA
Output Sink Current	70mA
Storage Temperature	+150°C
Operating Temperature (Ambient)	+125°C
Maximum Junction Temperature	+175°C

Stresses above those listed under the "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

ELECTRICAL CHARACTERISTICS (OPERATING)

PARAMETER	SYMBOL	HM-7610-5			HM-7611-5			UNITS	TEST CONDITIONS		
		5V ±5%			5V ±5%						
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
Address/Enable Input Current	I _{RA} , I _{RE} I _{FA} , I _{FE}		0	40		0	40	μA mA	V _{IH} = V _{CC} Max V _{IL} = 0.45V		
Input Threshold Voltage	V _{IH} V _{IL}	2.0		0.8	2.0		0.8	V	V _{CC} = V _{CC} Min V _{CC} = V _{CC} Max		
Output Voltage	V _{OH} V _{OL}	N/A		0.35	0.45	2.4	3.4	0.35	0.45	V V	I _{OH} = -2.0mA, V _{CC} = V _{CC} Min I _{OL} = +15mA, V _{CC} = V _{CC} Min V _{CS1} = V _{CS2} = 0.8V
D.C. Output Disabled Current	I _{OH}			100			100	μA	V _{OH} , V _{CC} = V _{CC} max		
	I _{OL}			N/A			-100	μA	V _{OL} = +0.3V, V _{CC} = V _{CC} Max V _{CS1} = V _{CS2} = 2.0V		
Output Leakage	I _{OH}			100			N/A	μA	V _{OH} , V _{CC} = V _{CC} Max		
Power Supply Current	I _{CC}		90	130		90	130	mA	V _{CC} = V _{CC} Max All Inputs Grounded		
Input Clamp Voltage	V _{CL}			-1.5			-1.5	V	I _{in} = -10ma		
Output Short Circuit Current	I _{OS}	N/A		N/A	15	23	30	mA	V _{CC} = V _{CC} Max, V _{OUT} = 0.0V One output only for a Max of 1 sec		
A.C. Address Access Time	t _{AA}		40	60		40	60	ns	V _{CC} and T _A Over Full Range		
	t _{EA}		15	25		15	25	ns	V _{CC} and T _A Over Full Range		

Typical Measurements are at T_A = 25°C, V_{CC} = +5V

PARAMETER	SYMBOL	HM-7610-2			HM-7611-2			UNITS	TEST CONDITIONS		
		5V ±10%			5V ±10%						
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
Address/Enable Input Current	I _{RA} , I _{RE} I _{FA} , I _{FE}		0	40		0	40	μA mA	V _{IH} = V _{CC} Max V _{IL} = 0.45V		
Input Threshold Voltage	V _{IH} V _{IL}	2.0		0.8	2.0		0.8	V	V _{CC} = V _{CC} Min V _{CC} = V _{CC} Max		
Output Voltage	V _{OH} V _{OL}	N/A		0.35	0.45	2.4	3.4	0.35	0.45	V V	I _{OH} = -2.0mA; V _{CC} = V _{CC} Min I _{OL} = +15mA; V _{CC} = V _{CC} Min V _{CS1} = V _{CS2} = 0.8V
D.C. Output Disabled Current	I _{OH}			100			100	μA	V _{OH} , V _{CC} = V _{CC} Max		
	I _{OL}			N/A			-100	μA	V _{OL} = +0.3V, V _{CC} = V _{CC} Max V _{CS1} = V _{CS2} = 2.0V		
Output Leakage	I _{OH}			100			N/A	μA	V _{OH} , V _{CC} = V _{CC} Max		
Power Supply Current	I _{CC}		90	130		90	130	mA	V _{CC} = V _{CC} Max All Inputs Grounded		
Input Clamp Voltage	V _{CL}			-1.5			-1.5	V	I _{in} = -10ma		
Output Short Circuit Current	I _{OS}	N/A		N/A	15	23	30	mA	V _{CC} = V _{CC} Max, V _{OUT} = 0.0V One output only for a Max of 1 sec		
A.C. Address Access Time	t _{AA}		40	75		40	75	ns	V _{CC} and T _A Over Full Range		
	t _{EA}		15	30		15	30	ns	V _{CC} and T _A Over Full Range		

Typical Measurements are at T_A = 25°C, V_{CC} = +5V

CAPACITANCE (1): T_A = 25°C

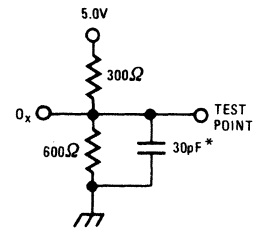
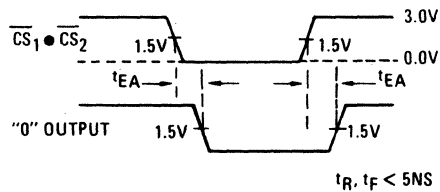
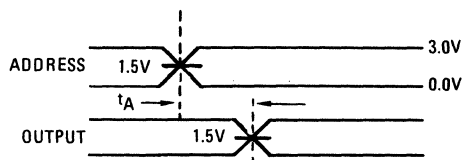
PARAMETER	SYMBOL	TYP.	UNITS	TEST CONDITION
Add. Input Cap.	C _{IN A} , C _S	8	pF	V _{CC} = 5V, V _{IN} = 2.0V, f = 1MHz
Output Cap.	C _{OUT}	8	pF	V _{CC} = 5V, V _{OUT} = 2.0V, f = 1MHz

NOTE: (1) These parameters are only periodically sampled and are not 100% tested.

MEMORY

SWITCHING TIME DEFINITIONS

A.C. TEST LOAD



*Includes jig & probe total capacitance

PROGRAMMING

The HM-7610/7611 is manufactured with all bits/outputs Logical "1" (Output High). Any desired bit/output can be programmed to a Logical "0" (Output Low) by following the simple procedure shown below. One may build his own programmer to satisfy the specifications described in Table 1, or buy any of the commercially available programmers which meet these specifications. The HM-7610/7611 can be programmed automatically or by the manual procedure shown below.

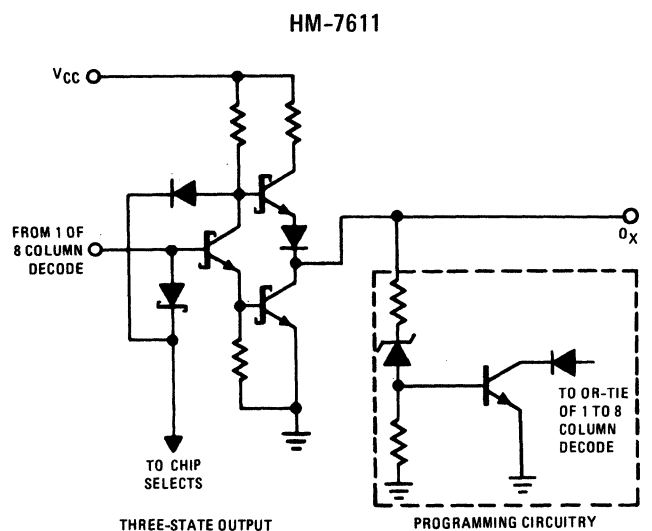
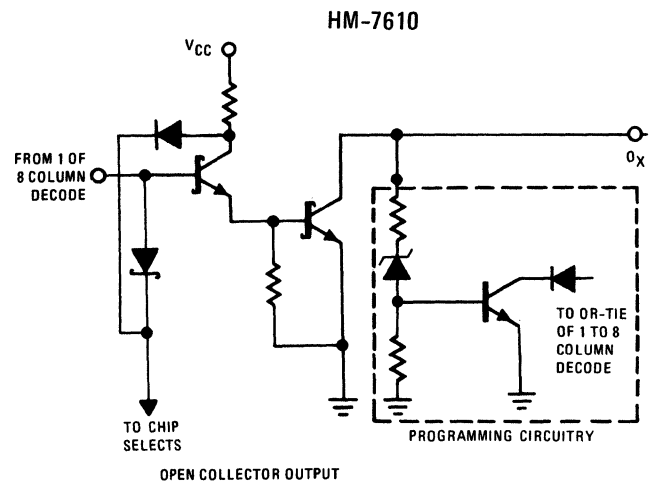
PROGRAMMING SPECIFICATIONS

TABLE 1

PARAMETER	SYMBOL	MIN.	RECOM-MEND VALUE	MAX.	UNITS
Address Input Voltage (1)	V_{IH}	2.4	5.0	5.0	V
	V_{IL}	0.0	0.4	0.8	V
Programming/Verify Voltage to V_{CC} (2)	V_{PH}	11.5	12.0	12.5	V
	V_{PL}	3.75	4.0	4.25	V
Programming Voltage Current Limit	I_{CCP}			600	mA
Programming (V_{CC}) Voltage Rise and Fall Time	t_r	1	1	10	μs
	t_f	1	1	10	μs
Programming Delay	t_d	10	10	100	μs
Programming Pulse Width - First Attempts	t_{p1}	100	100	200	μs
Programming Pulse Width - Subsequent	t_{p2}	10	10	20	ms
Programming Duty Cycle	D.C.	-	10	10	%
Output Voltage Enable Disable (3)	V_{OPE}	9.5	10.0	10.5	V
	V_{OPD}	0	.45	5.5	V
Output Voltage Enable Current Limit	I_{OPE}			10	mA
Case Temp	T_C			75	$^{\circ}C$

1. Address and chip select should not be left open for V_{IH} .
2. Verification at $V_{CC} = 4.0 \pm .25$ Volts, $T_A = 25^{\circ}C$ is recommended to guardband performance over full temperature and voltage range.
3. Disable condition will be met with output open circuit.

SCHEMATIC DIAGRAMS



PROGRAMMING PROCEDURE

1. Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL compatible. An open circuit should not be used to address the PROM.
2. Disable the chip by applying input highs (V_{IH}) to both chip select inputs. The chip select inputs are TTL compatible. An open circuit should not be used to disable the chip.
3. Disable the programming circuitry by applying an Output Voltage Disable of less than V_{OPD} to the output of the PROM. The output may be left open circuit to achieve the disable.
4. Raise V_{CC} to V_{PH} with rise time equal to t_r .
5. After a delay equal to or greater than t_d , apply a pulse with amplitude equal to V_{OPE} and duration of t_{p1} to the output selected for programming. Note that the PROM is supplied with fuses intact generating an output high. Programming a fuse will cause the output to go low in the verify mode.
6. Other bits in the same word may be programmed while the V_{CC} input is raised to V_{PH} by applying output

enable pulses to each output which is to be programmed. The output enable pulses must be separated by a minimum interval of t_d .

7. Lower V_{CC} to $4.0 \pm .25$ Volts following a delay to t_d from the last programming enable pulse applied to an output.
8. Enable the PROM for verification by applying a logic "0" (V_{IL}) to the \overline{CS}_1 and \overline{CS}_2 inputs.
9. If any bit does not verify as programmed, repeat steps 2 through 8 using an output pulse enable width of t_{p1} for up to 15 additional pulses to enhance programming speed. If the bit is still unprogrammed, follow with at least 16 repetitive pulses of t_{p2} in width, to achieve high programming yield. In the event that the bit is still unprogrammed, the part is considered a programming reject and should be returned to the factory. The address and incorrect and desired contents of a location in which a programming failure has occurred in any returned device must be included with that return.
10. Repeat steps 1 thru 9 for all other bits to be programmed in the PROM.

RECOMMENDED PROGRAMMING CIRCUIT

The circuit and timing diagram shown in Figures 1 and 2 will establish the proper programming condition for the output enable pulse. This allows the use of standard TTL parts for all logic inputs to the PROM. Note the gate which senses the output must be input protected to withstand input up to 12.5 Volts during programming.

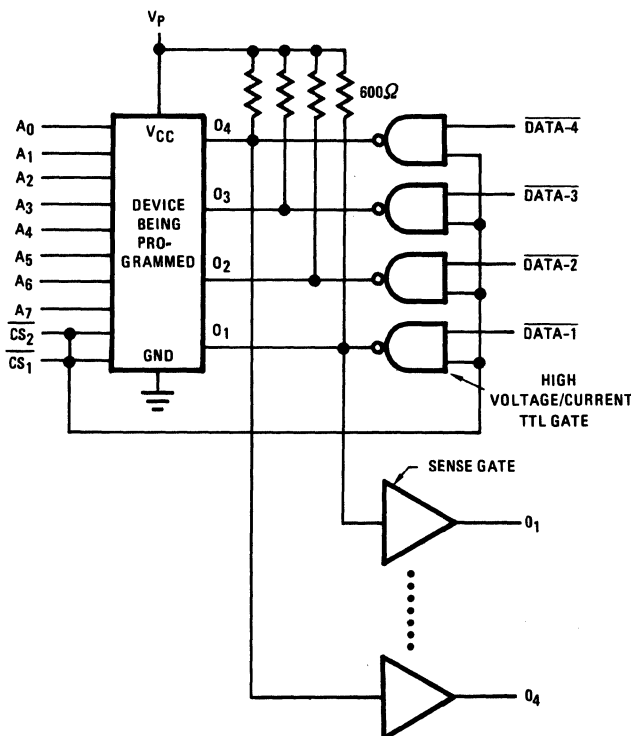


FIGURE 1

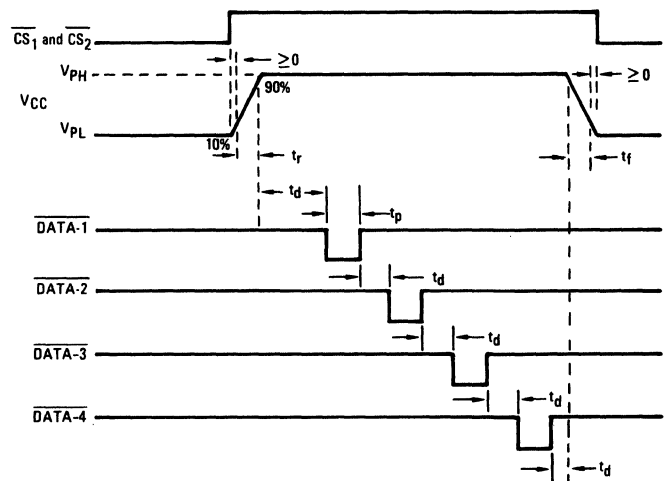
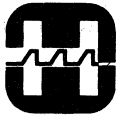


FIGURE 2



HARRIS
SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HM-7620/7621

2048-Bit Field Programmable Bipolar PROM

FEATURES

- 512 Words, 4 Bits per Word
- Simple, High Speed Programming Procedure (2 Seconds)
- Inputs and Outputs TTL Compatible
 - ▶ Low Input Current - 400 μ A Logic "0", 40 μ A Logic "1"
 - ▶ Full Output Drive - 15mA Sink/2mA Source
- Fast Access Time - 70ns Over Commercial Temperature & Voltage, 85ns Over Military Temperature & Voltage
- Expandable - "Wired-Or" Outputs With Chip Select
- Upward Pin Compatibility With 256 x 4 Proms

DESCRIPTION

The HM-7620 (open collector) and HM-7621 (three-state) are fully decoded, high speed, 2048-bit programmable ROM'S organized as 512 words by 4 bits per word. They are supplied with all bits storing a logical "1" (outputs high), and can be selectively programmed for a logical "0" (outputs low).

The nichrome fuse technology is the same as is used in the JAN approved MIL 38510/201 PROM, and in all other Harris PROMS.

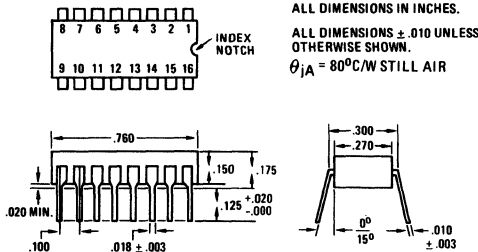
The field programmable PROM can be custom programmed to any pattern using a simple programming procedure. Schottky Bipolar circuitry provides extremely fast access time, and features temperature and voltage compensation to minimize variations in access time.

The pinout is compatible with the industry standard 256 x 4 PROM with the exception that the \overline{CS}_2 input on pin 14 is replaced by Address Input A8. Systems using 256 x 4 PROMS can be upgraded to store twice the number of bits within the same board area, while maintaining the same system power requirements. Alternatively, both the package count and the system power can be halved by using the HM-7620/HM-7621 in place of the 256 x 4 PROM.

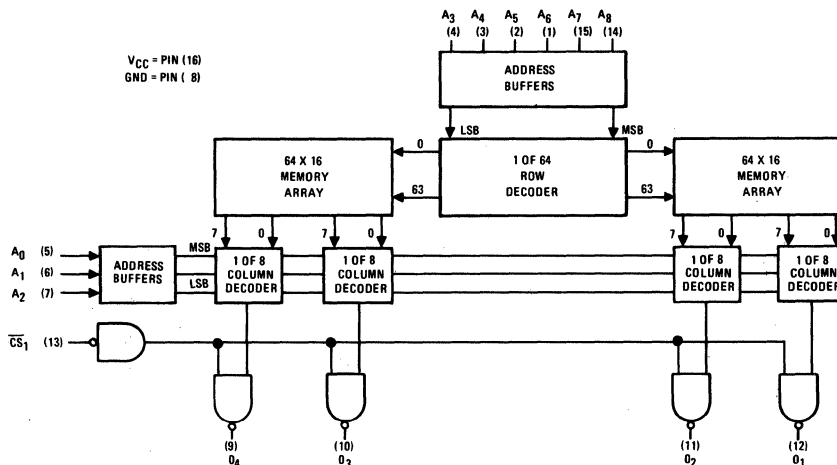
In addition to the conventional storage array, two test rows and two test columns are included to assure high programmability, and guarantee parametric and A.C. performance. These fuses are blown prior to shipment.

PACKAGE

CODE 1D 16 LEAD CERAMIC D.I.P.



BLOCK DIAGRAM



MEMORY

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	7.0V
Address/Enable Input Voltage	5.5V
Address/Enable Input Current	-20mA
Output Sink Current	70mA
Storage Temperature	+150°C
Operating Temperature (Ambient)	+125°C
Maximum Junction Temperature	+175°C

Stresses above those listed under the "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

ELECTRICAL CHARACTERISTICS (OPERATING)

PARAMETER	SYMBOL	HM-7620-5 5V ±5%			HM-7621-5 5V ±5%			UNITS	TEST CONDITIONS
		V _{CC}			V _{CC}				
		T _A 0°C to +70°C			T _A 0°C to +70°C				
Address/Enable Input Current	"1" "0"	I _{RA} , I _{RE} I _{FA} , I _{FE}	0 -0.1	40 -0.4	0 -0.1	40 -0.4	μA mA	V _{IH} = V _{CC} Max V _{IL} = 0.45V	
Input Threshold Voltage	"1" "0"	V _{IH} V _{IL}	2.0	0.8	2.0	0.8	V	V _{CC} = V _{CC} Min V _{CC} = V _{CC} Max	
Output Voltage	"1" "0"	V _{OH} V _{OL}	N/A 0.35	0.45	2.4 0.35	3.4 0.45	V	I _{OH} = -2.0mA, V _{CC} = V _{CC} Min I _{OL} = +15mA, V _{CC} = V _{CC} Min	
Output Disabled Current	"1" "0"	I _{OH} I _{OL}		100 N/A		100 -100	μA μA	V _{OH} , V _{CC} = V _{CC} max V _{OL} = +0.3V, V _{CC} = V _{CC} Max	
Output Leakage	"1"	I _{OH}		100		N/A	μA	V _{OH} , V _{CC} = V _{CC} Max	
Power Supply Current		I _{CC}	90	130	90	130	mA	V _{CC} = V _{CC} Max All Inputs Grounded	
Input Clamp Voltage		V _{CL}		-1.5		-1.5	V	I _{in} = -10ma	
Output Short Circuit Current		I _{OS}	N/A	N/A	15	23	30	mA	V _{CC} = V _{CC} Max, V _{OUT} = 0.0V One output only for a Max of 1 sec
Address Access Time		t _{AA}	40	70	40	70	ns	V _{CC} and T _A Over Full Range	
Enable Access Time		t _{EA}	15	25	15	25	ns	V _{CC} and T _A Over Full Range	

Typical Measurements are at T_A = 25°C, V_{CC} = +5V

PARAMETER	SYMBOL	HM-7620-2 5V ±10%			HM-7621-2 5V ±10%			UNITS	TEST CONDITIONS
		V _{CC}			V _{CC}				
		T _A -55°C to +125°C			T _A -55°C to +125°C				
Address/Enable Input Current	"1" "0"	I _{RA} , I _{RE} I _{FA} , I _{FE}	0 -0.1	*40 *-0.4	0 -0.1	*40 *-0.4	μA mA	V _{IH} = V _{CC} Max V _{IL} = 0.45V	
Input Threshold Voltage	"1" "0"	V _{IH} V _{IL}	2.0	0.8	2.0	0.8	V	V _{CC} = V _{CC} Min V _{CC} = V _{CC} Max	
Output Voltage	"1" "0"	V _{OH} V _{OL}	N/A 0.35	*0.45	*2.4 0.35	3.4 *0.45	V	I _{OH} = -2.0mA; V _{CC} = V _{CC} Min I _{OL} = +15mA; V _{CC} = V _{CC} Min	
Output Disabled Current	"1" "0"	I _{OH} I _{OL}		*100 N/A		*100 *100	μA μA	V _{OH} , V _{CC} = V _{CC} Max V _{OL} = +0.3V, V _{CC} = V _{CC} Max	
Output Leakage	"1"	I _{OH}		*100		N/A	μA	V _{OH} , V _{CC} = V _{CC} Max	
Power Supply Current		I _{CC}	90	*130	90	*130	mA	V _{CC} = V _{CC} Max All Inputs Grounded	
Input Clamp Voltage		V _{CL}		*-1.5		*-1.5	V	I _{in} = -10ma	
Output Short Circuit Current		I _{OS}	N/A	N/A	*15	23	*30	mA	V _{CC} = V _{CC} Max, V _{OUT} = 0.0V One output only for a Max of 1 sec
Address Access Time		t _{AA}	40	*85	40	*85	ns	V _{CC} and T _A Over Full Range	
Enable Access Time		t _{EA}	15	*30	15	*30	ns	V _{CC} and T _A Over Full Range	

Typical Measurements are at T_A = 25°C, V_{CC} = +5V

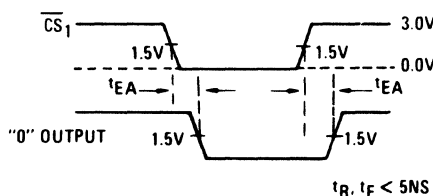
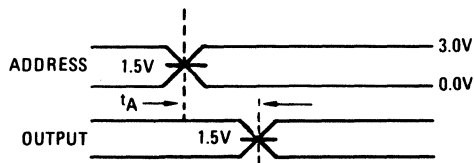
*100% Tested For DASH 8

CAPACITANCE (1): T_A = 25°C

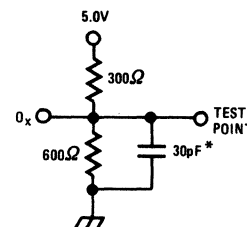
PARAMETER	SYMBOL	TYP.	UNITS	TEST CONDITIONS
Add. Input Cap.	C _{IN A, CS}	8	pF	V _{CC} = 5V, V _{IN} = 2.0V, f = 1MHz
Output Cap.	C _{OUT}	8	pF	V _{CC} = 5V, V _{OUT} = 2.0V, f = 1MHz

NOTE: (1) These parameters are only periodically sampled and are not 100% tested.

SWITCHING TIME DEFINITIONS



A.C. TEST LOAD



* Includes jig & probe total capacitance

PROGRAMMING

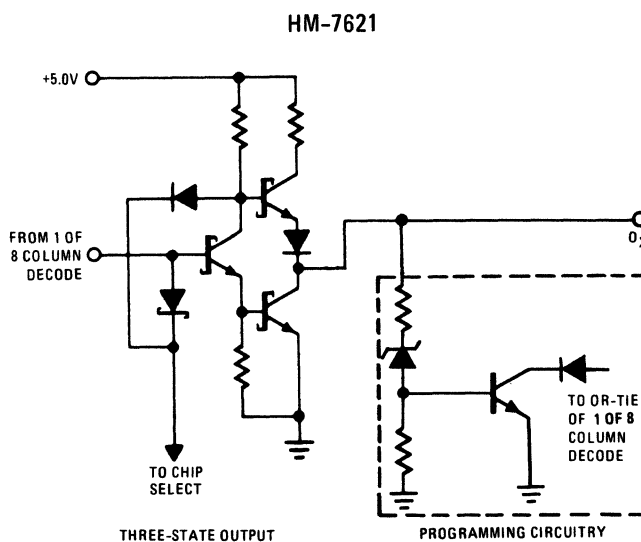
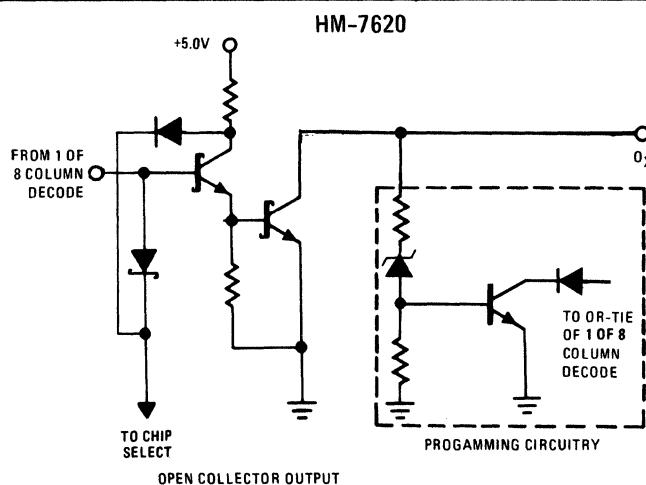
The HM-7620/7621 is manufactured with all bits/outputs Logical "1" (Output High). Any desired bit/output can be programmed to a Logical "0" (Output Low) by following the simple procedure shown below. One may build his own programmer to satisfy the specifications described in Table 1, or buy any of the commercially available programmers which meet these specifications. The HM-7620/7621 can be programmed automatically or by the manual procedure shown below.

PROGRAMMING SPECIFICATIONS

PARAMETER	SYMBOL	MIN.	RECOM-MEND VALUE	MAX.	UNITS
Address Input Voltage (1)	V_{IH}	2.4	5.0	5.0	V
	V_{IL}	0.0	0.4	0.8	V
Programming/Verify Voltage to V_{CC}	V_{PH}	11.5	12.0	12.5	V
	V_{PL}	3.75	4.0	4.25	V
Programming Voltage Current Limit (2)	I_{CCP}			600	mA
Programming (V_{CC}) Voltage Rise and Fall Time	t_r	1	1	10	μs
	t_f	1	1	10	μs
Programming Delay	t_d	10	10	100	μs
Programming Pulse Width - First Attempts	t_{p1}	100	100	200	μs
Programming Pulse Width - Subsequent	t_{p2}	10	10	20	ms
Programming Duty Cycle	D.C.	-	10	10	%
Output Voltage Enable (3)	V_{OPE}	9.5	10.0	10.5	V
	V_{OPD}	0	.45	5.5	V
Output Voltage Enable Current Limit	I_{OPE}			10	mA
Case Temp	T_C			75	$^{\circ}C$

1. Address and chip select should not be left open for V_{IH} .
2. Verification at $V_{CC} = 4.0 \pm .25$ Volts, $T_A = 25^{\circ}C$ is recommended to guardband performance over full temperature and voltage range.
3. Disable condition will be met with output open circuit.

SCHEMATIC DIAGRAMS



PROGRAMMING PROCEDURE

1. Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL compatible. An open circuit should not be used to address the PROM.
2. Disable the chip by applying an input high (V_{IH}) to the chip select input. The chip select input is TTL compatible. An open circuit should not be used to disable the chip.
3. Disable the programming circuitry by applying an Output Voltage Disable of less than V_{OPD} to the output of the PROM. The output may be left open circuit to achieve the disable.
4. Raise V_{CC} to V_{PH} with rise time equal to t_r .
5. After a delay equal to or greater than t_d , apply a pulse with amplitude equal to V_{OPE} and duration of t_{p1} to the output selected for programming. Note that the PROM is supplied with fuses intact generating an output high. Programming a fuse will cause the output to go low in the verify mode.
6. Other bits in the same word may be programmed while the V_{CC} input is raised to V_{PH} by applying output enable pulses to each output which is to be programmed. The output enable pulses must be separated by a minimum interval of t_{d1} .
7. Return V_{CC} to $4.0 \pm .25$ V following a delay of t_d from the last programming enable pulse applied to an output.
8. Enable the PROM for verification by applying a logic "0" (V_{IL}) to the CS_1 input.
9. If any bit does not verify as programmed, repeat steps 2 through 8 using an output pulse enable width of t_{p1} for up to 15 additional pulses to enhance programming speed. If the bit is still unprogrammed, follow with at least 16 repetitive pulses of t_{p2} in width, to achieve high programming yield. In the event that the bit is still unprogrammed, the part is considered a programming reject and should be returned to the factory. The address and incorrect and desired contents of a location in which a programming failure has occurred in any returned device must be included with that return.
10. Repeat steps 1 thru 9 for all other bits to be programmed in the PROM.

RECOMMENDED PROGRAMMING CIRCUIT

The circuit and timing diagram shown in Figures 1 and 2 will establish the proper programming condition for the output enable pulse. This allows the use of standard TTL parts for all logic inputs to the PROM. Note the gate which senses the output must be input protected to withstand input up to 12.5 Volts during programming.

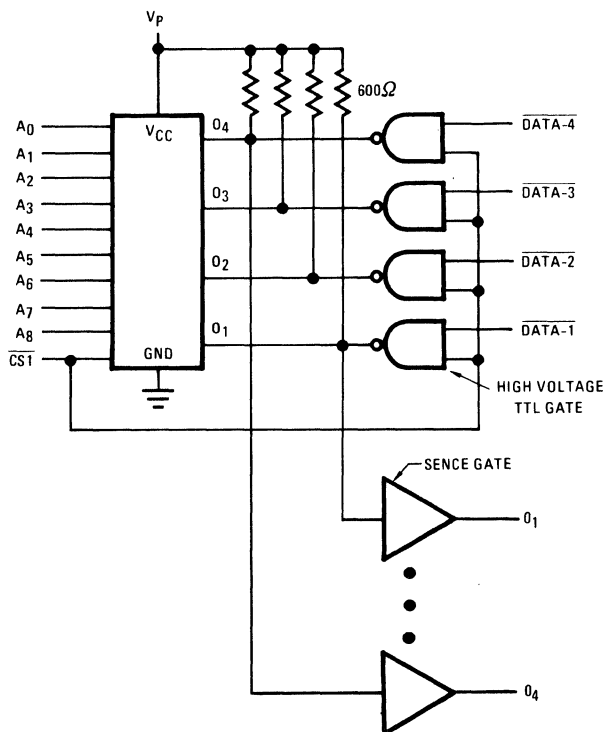


FIGURE 1

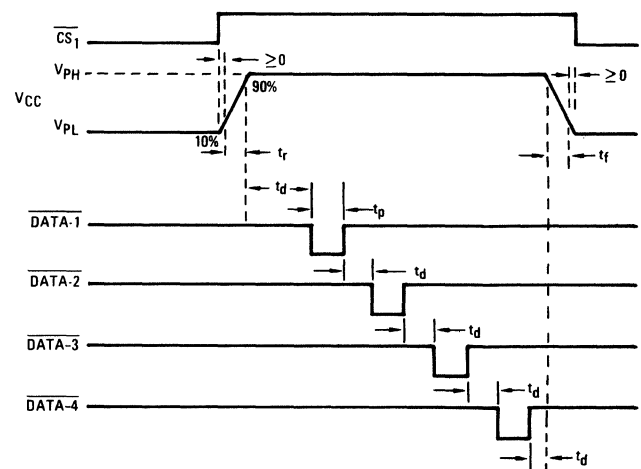


FIGURE 2

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	7.0V
Address/Enable Input Voltage	5.5V
Address/Enable Input Current	-20mA
Output Sink Current	70mA
Storage Temperature	+150°C
Operating Temperature (Ambient)	+125°C
Maximum Junction Temperature	+175°C

Stresses above those listed under the "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

ELECTRICAL CHARACTERISTICS (OPERATING)

PARAMETER	SYMBOL	HM-7640-5			HM-7641-5			UNITS	TEST CONDITIONS	
		V_{CC}								
		5V ±5%			5V ±5%					
TA	0°C to +70°C			0°C to +70°C						
Address/Enable Input Current	"1"	I_{RA}, I_{RE}	0	40		0	40	μA	$V_{IH} = V_{CC} \text{ Max}$ $V_{IL} = 0.45V$	
	"0"	I_{FA}, I_{FE}	-0.1	-0.4		-0.1	-0.4	mA		
Input Threshold Voltage	"1"	V_{IH}	2.0		2.0			V	$V_{CC} = V_{CC} \text{ Min}$ $V_{CC} = V_{CC} \text{ Max}$	
	"0"	V_{IL}		0.8			0.8	V		
Output Voltage	"1"	V_{OH}	N/A		2.4	3.4		V	$I_{OH} = -2.0mA, V_{CC} = V_{CC} \text{ Min}$ $I_{OL} = +15mA, V_{CC} = V_{CC} \text{ Min}$ $V_{CS1} = V_{CS2} = 0.8V$	
	"0"	V_{OL}		0.35	0.45	0.35	0.45	V		
D.C. Output Disabled Current	"1"	I_{OHE}		100			100	μA	$V_{OH}, V_{CC} = V_{CC} \text{ max}$ $V_{OL} = +0.3V, V_{CC} = V_{CC} \text{ Max}$ $V_{CS1} = V_{CS2} = 2.0V$	
	"0"	I_{OLE}		N/A			-100	μA		
Output Leakage	"1"	I_{OH}		100			N/A	μA	$V_{OH}, V_{CC} = V_{CC} \text{ Max}$	
Power Supply Current		I_{CC}		125	170		125	170	mA	$V_{CC} = V_{CC} \text{ Max}$ All Inputs Grounded
Input Clamp Voltage		V_{CL}			-1.5			-1.5	V	$I_{in} = -10ma$
Output Short Circuit Current		I_{OS}	N/A		N/A	15	23	30	mA	$V_{CC} = V_{CC} \text{ Max}, V_{OUT} = 0.0V$ One output only for a Max of 1 sec
A.C. Address Access Time		t_{AA}		40	70		40	70	ns	V_{CC} and T_A Over Full Range
		t_{EA}		15	25		15	25	ns	V_{CC} and T_A Over Full Range

Typical Measurements are at $T_A = 25^\circ C, V_{CC} = +5V$

PARAMETER	SYMBOL	HM-7640-2			HM-7641-2			UNITS	TEST CONDITIONS	
		V_{CC}								
		5V ±10%			5V ±10%					
TA	-55°C to +125°C			-55°C to +125°C						
Address/Enable Input Current	"1"	I_{RA}, I_{RE}	0	40		0	40	μA	$V_{IH} = V_{CC} \text{ Max}$ $V_{IL} = 0.45V$	
	"0"	I_{FA}, I_{FE}	-0.1	-0.4		-0.1	-0.4	mA		
Input Threshold Voltage	"1"	V_{IH}	2.0		2.0			V	$V_{CC} = V_{CC} \text{ Min}$ $V_{CC} = V_{CC} \text{ Max}$	
	"0"	V_{IL}		0.8			0.8	V		
Output Voltage	"1"	V_{OH}	N/A		2.4	3.4		V	$I_{OH} = -2.0mA; V_{CC} = V_{CC} \text{ Min}$ $I_{OL} = +15mA; V_{CC} = V_{CC} \text{ Min}$ $V_{CS1} = V_{CS2} = 0.8V$	
	"0"	V_{OL}		0.35	0.45	0.35	0.45	V		
D.C. Output Disabled Current	"1"	I_{OHE}		100			100	μA	$V_{OH}, V_{CC} = V_{CC} \text{ Max}$ $V_{OL} = +0.3V, V_{CC} = V_{CC} \text{ Max}$ $V_{CS1} = V_{CS2} = 2.0V$	
	"0"	I_{OLE}		N/A			-100	μA		
Output Leakage	"1"	I_{OH}		100			N/A	μA	$V_{OH}, V_{CC} = V_{CC} \text{ Max}$	
Power Supply Current		I_{CC}		125	170		125	170	mA	$V_{CC} = V_{CC} \text{ Max}$ All Inputs Grounded
Input Clamp Voltage		V_{CL}			-1.5			-1.5	V	$I_{in} = -10ma$
Output Short Circuit Current		I_{OS}	N/A		N/A	15	23	30	mA	$V_{CC} = V_{CC} \text{ Max}, V_{OUT} = 0.0V$ One output only for a Max of 1 sec
A.C. Address Access Time		t_{AA}		40	85		40	85	ns	V_{CC} and T_A Over Full Range
		t_{EA}		15	30		15	30	ns	V_{CC} and T_A Over Full Range

Typical Measurements are at $T_A = 25^\circ C, V_{CC} = +5V$

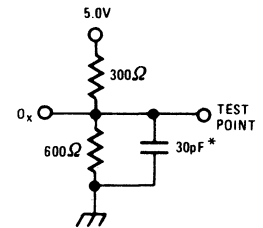
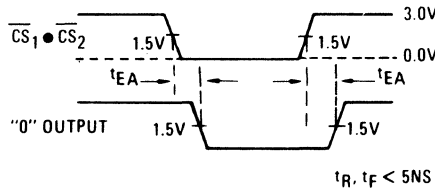
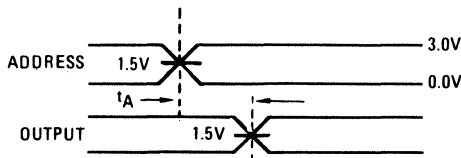
CAPACITANCE (1): $T_A = 25^\circ C$

PARAMETER	SYMBOL	TYP.	UNITS	TEST CONDITION
Add. Input Cap.	$C_{IN A, CS}$	8	pF	$V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz$
Output Cap.	C_{OUT}	8	pF	$V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz$

NOTE: (1) These parameters are only periodically sampled and are not 100% tested.

SWITCHING TIME DEFINITIONS

A.C. TEST LOAD



* Includes jig & probe total capacitance

PROGRAMMING

The HM-7640/7641 is manufactured with all bits/outputs Logical "1" (Output High). Any desired bit/output can be programmed to a Logical "0" (Output Low) by following the simple procedure shown below. One may build his own programmer to satisfy the specifications described in Table 1, or buy any of the commercially available programmers which meet these specifications. The HM-7640/7641 can be programmed automatically or by the manual procedure shown below.

PROGRAMMING SPECIFICATIONS

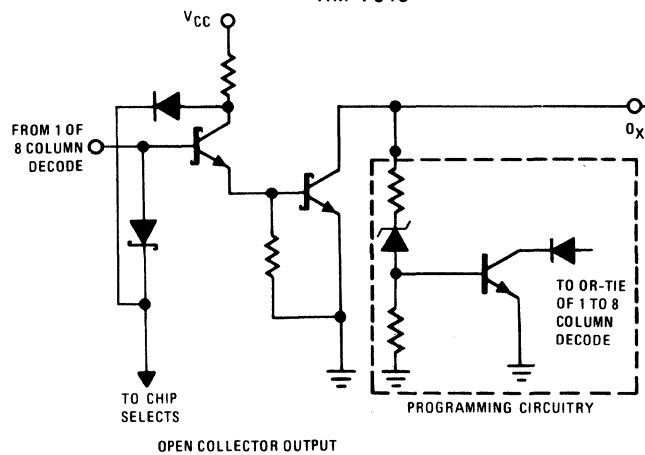
TABLE 1

PARAMETER	SYMBOL	MIN.	RECOM-MEND VALUE	MAX.	UNITS
Address Input Voltage (1)	V_{IH}	2.4	5.0	5.0	V
	V_{IL}	0.0	0.4	0.8	V
Programming/Verify Voltage to V_{CC} (2)	V_{PH}	11.5	12.0	12.5	V
	V_{PL}	3.75	4.0	4.25	V
Programming Voltage Current Limit	I_{CCP}			600	mA
Programming (V_{CC}) Voltage Rise and Fall Time	t_r	1	1	10	μs
	t_f	1	1	10	μs
Programming Delay	t_d	10	10	100	μs
Programming Pulse Width - First Attempts	t_{p1}	100	100	200	μs
Programming Pulse Width - Subsequent	t_{p2}	10	10	20	ms
Programming Duty Cycle	D.C.	-	10	10	%
Output Voltage Enable (3)	V_{OPE}	9.5	10.0	10.5	V
	V_{OPD}	0	.45	5.5	V
Output Voltage Enable Current Limit	I_{OPE}			10	mA
Case Temp	T_C			75	$^{\circ}C$

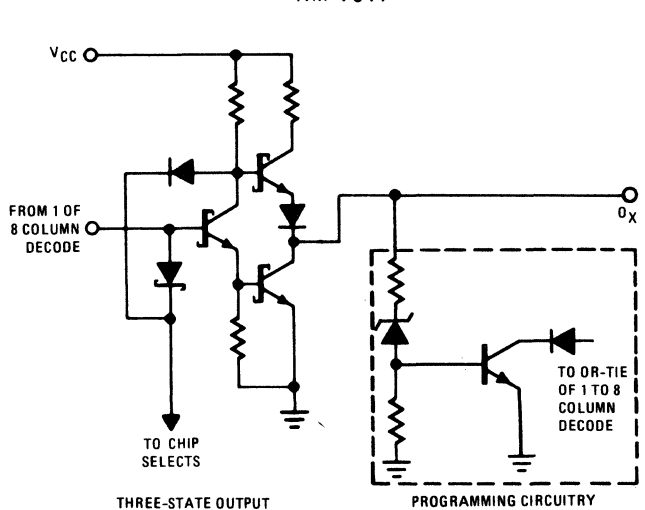
1. Address and chip select should not be left open for V_{IH} .
2. Verification at $V_{CC} = 4.0 \pm .25$ Volts, $T_A = 25^{\circ}C$ is recommended to guardband performance over full temperature and voltage range.
3. Disable condition will be met with output open circuit.

SCHEMATIC DIAGRAMS

HM-7640



HM-7641



MEMORY

PROGRAMMING PROCEDURE

1. Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL compatible. An open circuit should not be used to address the PROM.
2. Disable the chip by applying input highs (V_{IH}) to both \overline{CS}_1 and \overline{CS}_2 chip select inputs. The chip select inputs are TTL compatible. An open circuit should not be used to disable the chip.
3. Disable the programming circuitry by applying an Output Voltage Disable of less than V_{OPD} to the output of the PROM. The output may be left open circuit to achieve the disable.
4. Raise V_{CC} to V_{pH} with rise time equal to t_r .
5. After a delay equal to or greater than t_d , apply a pulse with amplitude equal to V_{OPE} and duration of t_{p1} to the output selected for programming. Note that the PROM is supplied with fuses intact generating an output high. Programming a fuse will cause the output to go low in the verify mode.
6. Other bits in the same word may be programmed while the V_{CC} input is raised to V_{pH} by applying output

enable pulses to each output which is to be programmed. The output enable pulses must be separated by a minimum interval of t_d .

7. Lower V_{CC} to $4.0 \pm .25$ Volts following a delay to t_d from the last programming enable pulse applied to an output.
8. Enable the PROM for verification by applying a logic "0" (V_{iL}) to the \overline{CS}_1 and \overline{CS}_2 inputs.
9. If any bit does not verify as programmed, repeat steps 2 through 8 using an output pulse enable width of t_{p1} for up to 15 additional pulses to enhance programming speed. If the bit is still unprogrammed, follow with at least 16 repetitive pulses of t_{p2} in width, to achieve high programming yield. In the event that the bit is still unprogrammed, the part is considered a programming reject and should be returned to the factory. The address and incorrect and desired contents of a location in which a programming failure has occurred in any returned device must be included with that return.
10. Repeat steps 1 thru 9 for all other bits to be programmed in the PROM.

RECOMMENDED PROGRAMMING CIRCUIT

The circuit and timing diagram shown in Figures 1 and 2 will establish the proper programming condition for the output enable pulse. This allows the use of standard TTL parts for all logic inputs to the PROM. Note the gate which senses the output must be input protected to withstand input up to 12.5 Volts during programming.

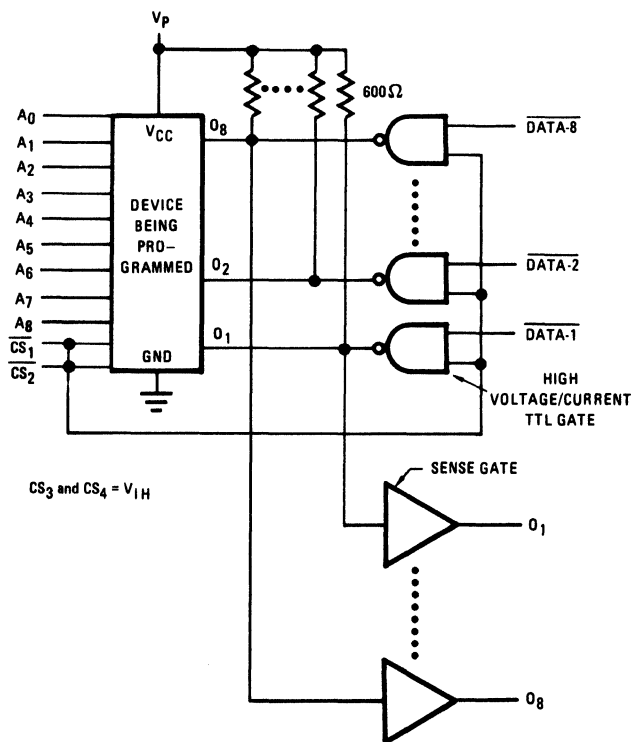


FIGURE 1

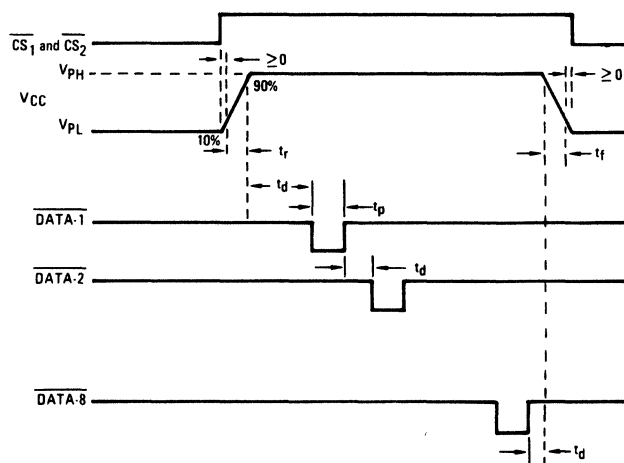


FIGURE 2

HARRIS BIPOLAR PROM CROSS-REFERENCE

NO. OF BITS	ORGANIZATION AND NO. OF OUTPUTS	HARRIS	AMD	FAIRCHILD	INTEL	INTERSIL	MMI	MOTOROLA	NATIONAL	SIGNETICS	TI
256	32X8 OPEN COLLECTOR	HPROM-8256-2				IM5600M	MM5330			S8223	54188A
		HPROM-8256-5				IM6500C	MM6330			N8223	74188A
		*HM7602-2							DM7577	S82S23	54S188
		*HM7602-5	AM27S08						DM8577	N82S23	74S188
	32X8 3-STATE	*HM7603-2				IM5610M	MM5331		DM7578	S82S123	54S288
		*HM7603-5	AM27S09			IM5610C	MM6331		DM8578	S82S123	74S288
512	64X8 OPEN COLLECTOR	HPROM-0512-2						MCM5303A			54186
		HPROM-0512-5						MCM5003A			74186
	64X8 PULL UP RESISTOR							MCM5304			
								MCM5004			
1024	256X4 OPEN COLLECTOR	HPROM-1024A-2		93416DM		IM5603M	MM5300		DM7573	S82S126	54S387
		HPROM-1024A-5		93416DC	3601	IM5603C	MM6300	MCM5005L	DM8573	N82S126	74S387
		HM7610-2									
		HM7610-5									
	256X4 3-STATE	HPROM-1024-2		93426DM		IM5623M	MM5301		DM7574	S82S129	54S287
		HPROM-1024-5		93426DC		IM5623C	MM6301		DM8574	N82S129	74S287
		HM7611-2									
		HM7611-5									
2048	512X4 OPEN COLLECTOR	HM7602-2				IM5604M	MM5305				54S370
		HM7620-5				IM5604C	MM6305				74S370
	512X4 3-STATE	HM7621-2			3602	IM5624M	MM5306			82S130	54S270
		HM7621-5		93436	3622	IM5624C	MM6306			82S131	74S270

NOTE: Compatible pin-for-pin in read mode, but require different programming conditions for entering data into the memory.



HARRIS
SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

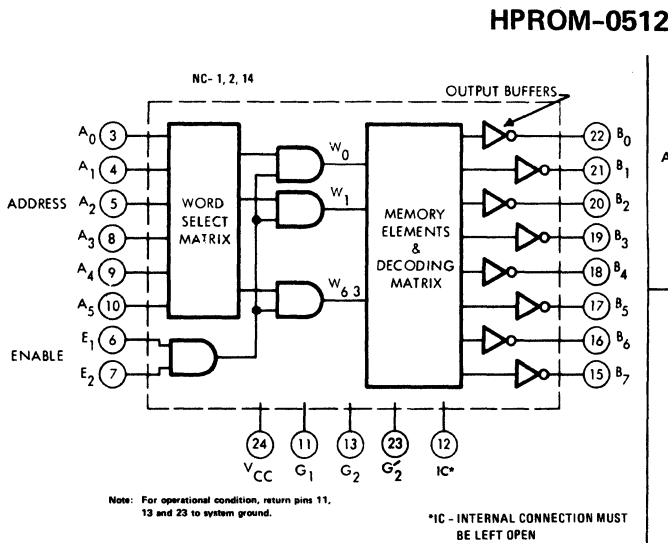
HPR0M-0512

512-Bit, Bipolar PROM™*

FEATURES

- FIELD PROGRAMMABLE
- 64 WORDS/8 BITS PER WORD
- FULLY DECODED
- DTL/TTL COMPATIBLE
- 55 NS ACCESS TIME
- SINGLE 5 VOLT POWER SUPPLY
- STATIC OUTPUT WITH FANOUT OF 10
- AVAILABLE IN EITHER MILITARY OR COMMERCIAL TEMPERATURE RANGE
- EXPANDABLE – "WIRED-OR" OUTPUTS
"AND" ENABLE INPUTS

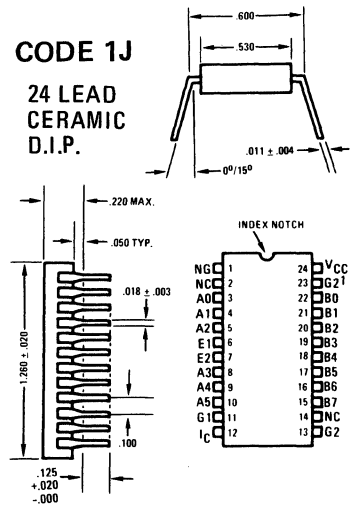
BLOCK DIAGRAM



PACKAGE

CODE 1J

24 LEAD
CERAMIC
D.I.P.



ALL DIMENSIONS ARE IN INCHES.
ALL DIMENSIONS ± .010 UNLESS OTHERWISE SHOWN.

TRUTH TABLE

Word Number	INPUTS							OUTPUTS							
	(1)E	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀	B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀
(2)X	0	X	X	X	X	X	X	1	1	1	1	1	1	1	1
0	1	0	0	0	0	0	0	*	*	*	*	*	*	*	*
1	1	0	0	0	0	0	1	*	*	*	*	*	*	*	*
2	1	0	0	0	0	1	0	*	*	*	*	*	*	*	*
.
.
63	1	1	1	1	1	1	1	*	*	*	*	*	*	*	*

NOTE: (1) E = E₁ · E₂ (2) X = "Don't Care"

FIELD PROGRAMMING

The HPR0M-0512 is the first read-only memory which can be programmed electronically after manufacture and packaging. Most semiconductor read-only memories are programmed during manufacturing by designing the final metallization to correspond to the desired memory configuration. This process requires a different mask for each unique design and once the device is packaged, no further changes can be made. In contrast, the technique for programming the HPR0M-0512 (see page 5) is straightforward and can be implemented at the user's facility with little difficulty.

Referring to the block diagram above, the status of any bit is determined by the condition of the 512 "Memory Elements" which connect the input word lines to each of eight (8) output bit buffers. In an unprogrammed memory, all "Memory Elements" are short circuits so that logical "zeros" appear at each output bit position for any address input. "Electronic Programming" involves the alteration of specific "Memory Elements" to create logical "ones" in selected bit positions. This alteration is irreversible and cannot be accomplished under normal operating conditions – thus, the HPR0M-0512 is a true permanent memory when inserted in a system.

* PROM is a trademark of Harris Semiconductor for its family of field programmable read-only memories.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage, V_A, V_E	-1.5V to +5.5V	Operating Temperature (Case)	-55°C to +125°C
Output Supply Voltage, V_{BS}	-0.5V to +7.0V	$\theta_{JC} = 15^\circ\text{C/W}$	
Output Sink Current, I_{OL}	-30mA	$\theta_{JA} = 50^\circ\text{C/W}$	
Input Current	-30mA		

ELECTRICAL CHARACTERISTICS

Test Conditions: $V_{CC} = 5.0 \pm 5\%$, $G_1 = G_2 = G_2' = \text{Ground}$
 $T_{CASE} = -55^\circ\text{C}$ to $+125^\circ\text{C}$ for HPR0M-0512-2
 0°C to $+75^\circ\text{C}$ for HPR0M-0512-5
 unless otherwise specified.

PARAMETER	SYM	LIMITS			UNITS	TEST CONDITION	
		MIN	TYP	MAX			
Enable Current	"1" I_{RE}		10	* 60	μA	$V_E = 2.4\text{V}$	$V_{CC} = 5.25\text{V}$
			30	* 100		$V_E = 5.25\text{V}$	
Address Current	"0" I_{FE}		-1.0	* -1.6	mA	$V_E = 0.4\text{V}$	$V_{CC} = 5.25\text{V}$
	"1" I_{RA}		10	* 60	μA	$V_A = 2.4\text{V}$	$V_{CC} = 5.25\text{V}$
			30	* 100		$V_A = 5.25\text{V}$	
Input Threshold Voltage (1)	"0" I_{FA}		-1.0	* -1.6	mA	$V_A = 0.4\text{V}$	$V_{CC} = 5.25\text{V}$
	"1" V_{IH}		2.0		V	$V_{CC} = 4.75\text{V}$	
D.C.	"0" V_{IL}			0.8	V	$V_{CC} = 5.25\text{V}$	
	Output "0" Voltage	V_{OL}	0.25	*0.45	V	$V_{CC} = 4.75\text{V}$	$V_{IH} = 2.0\text{V}$ $V_{IL} = 0.8\text{V}$
						$I_{OL} = 10\text{mA}$	
	Output "1" Leakage Current	I_{OH}			*100 *200	μA	$V_{OH} = 2.4\text{V}$ $V_{OH} = 5.25\text{V}$
Power Supply Current (3)	(Quiescent) I_{CC}		70	* 95	mA	$V_{CC} = 5.25\text{V}; V_E = V_A = 0\text{V}$	
	(Operating) I_{CC}		80		mA	$V_{CC} = 5.25\text{V}; f = 4\text{MB/s}^{(2)}$	
Output Capacity	C_{OUT}		5		pF	$V_{OUT} = 2.0\text{V}$	
A.C.	Address or Enable to Output Fall Delay (4)	t_-	25	55	75	ns	$R_1 = 470\Omega$ $R_2 = 1\text{K}\Omega$ $C_L = 30\text{pF}$ $T_A = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$
	Address or Enable to Output Rise Delay (4)	t_+	25	55	75	ns	

NOTES: (1) Threshold voltages are defined as the limits on the input levels which ensure that the desired input state is achieved.

(2) A typical device is one programmed to output 50% "ones".

100% Tested For DASH 8

(3) Output terminals left open
-see Test Circuit 1.

(4) See Test Circuit 2.

MEMORY

TEST CIRCUITS

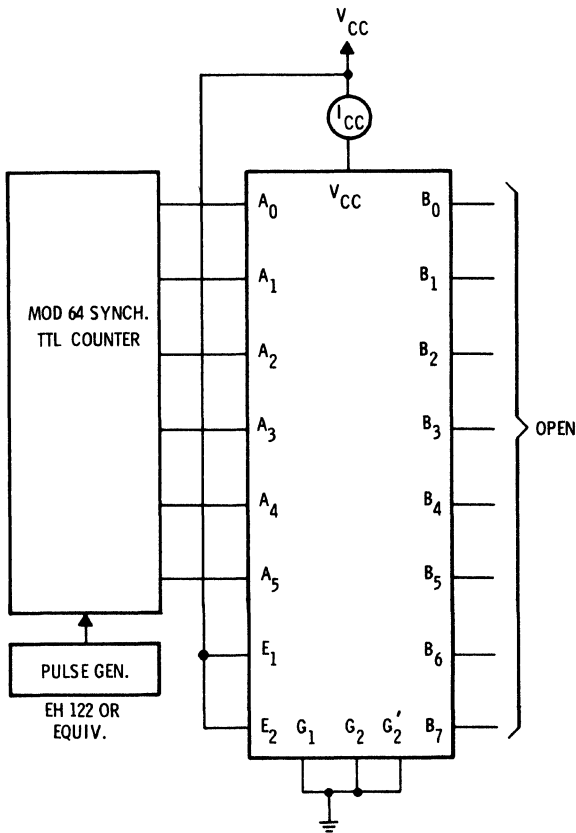


Figure 1.
OPERATING POWER SUPPLY CURRENT

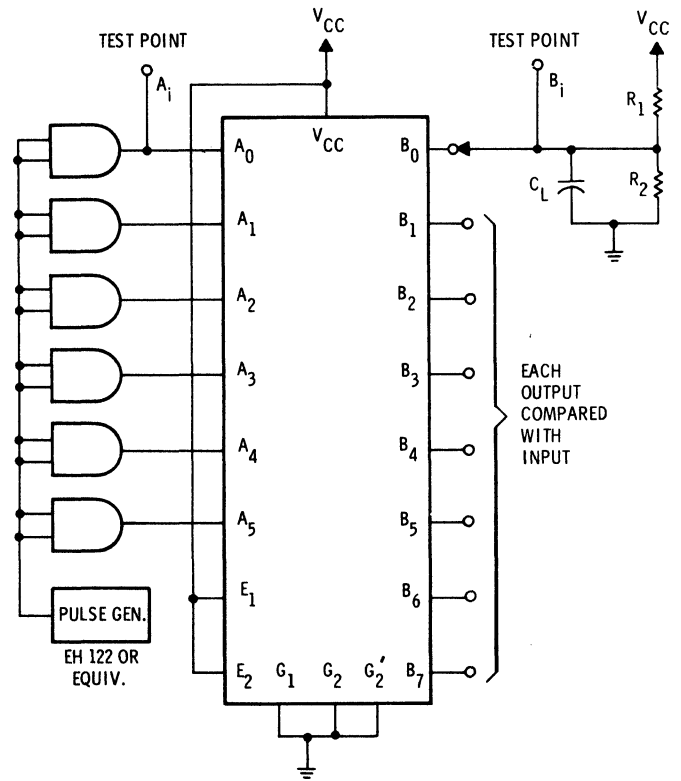
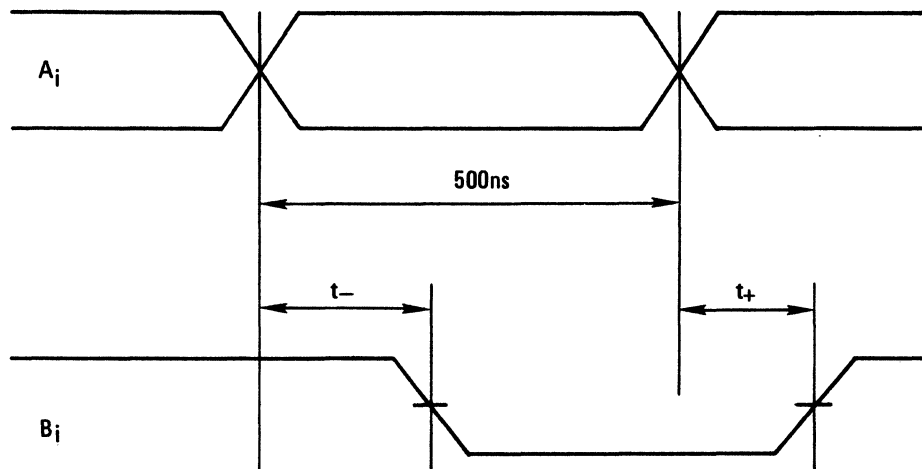


Figure 2.
PROPAGATION DELAYS

NOTE: Applies only to programmed units.

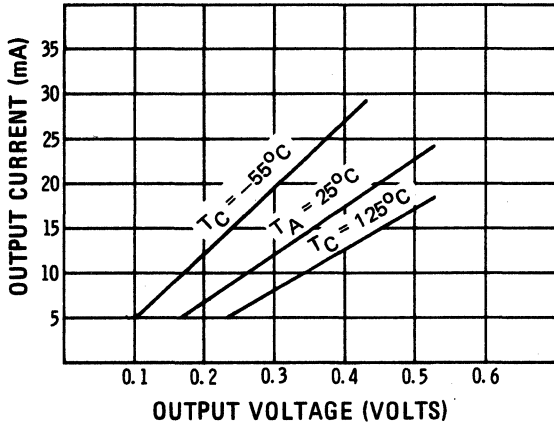
SWITCHING TIME DEFINITIONS



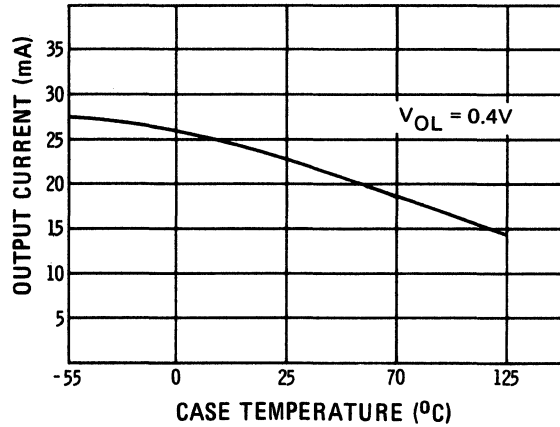
- NOTES: (1) $E_1 = E_2 = "1"$
 (2) All measurements referenced to +1.5V level.
 (3) Address rise and fall times ≤ 10 ns.

CHARACTERISTIC CURVES

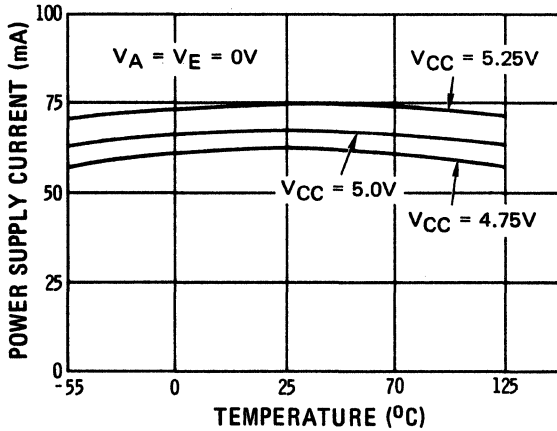
OUTPUT CHARACTERISTICS



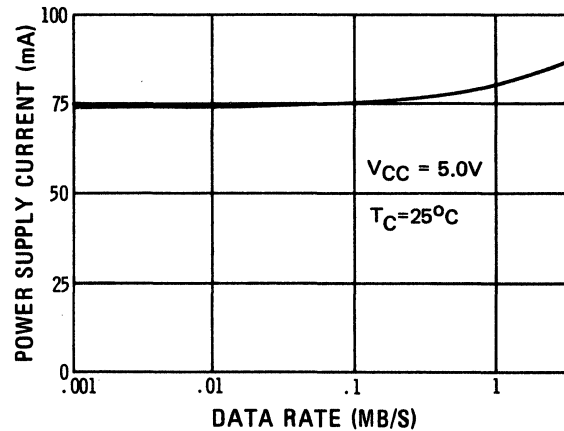
OUTPUT CURRENT VS. TEMPERATURE



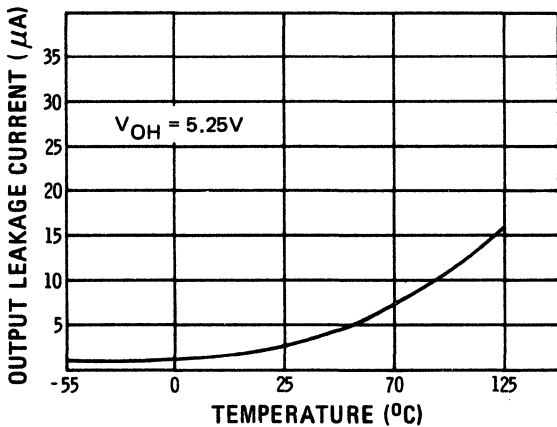
POWER SUPPLY CURRENT VS. TEMPERATURE



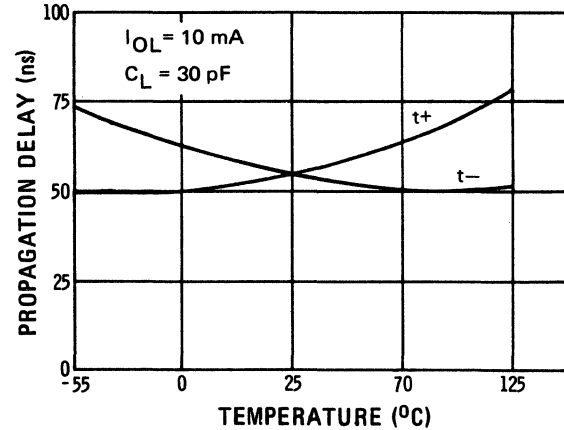
POWER SUPPLY CURRENT VS. DATA RATE



OUTPUT LEAKAGE CURRENT VS. TEMPERATURE



PROPAGATION DELAY VS. TEMPERATURE



TEST CONDITIONS: $V_{CC} = 5.0\text{V}$ UNLESS OTHERWISE SPECIFIED.

PROGRAMMING

PROGRAMMING SPECIFICATIONS

PARAMETER	SYM.	RECOMMENDED VALUE
Address Input Voltage	"1"	V_{AH} (1) Open Circuit
	"0"	V_{AL} -5.0V
Address Input low Current	I_{AL}	-3.0mA
Power Supply Voltage	V_{CC}	5.0V +5%-0% @ $I_{CC} \leq 250mA$
G_1 Voltage (2)	V_{G1}	-5.0V
G_2 Voltage	V_{G2}	0V
Programming Voltage (MAX)	\bar{V}_{BP}	-7.0V
Programming Current (MAX)	\bar{I}_p	100mA
Maximum Programming T_{CASE}	\bar{T}_{CASE}	75°C
Programming Pulse widths	PW	400 ms
Duty Cycle T_A 25°C	DC	20%

- (1) An open collector TTL gate meets this specification.
 (2) G_1 must be connected to -5.0V prior to applying V_{CC} or programming voltage.

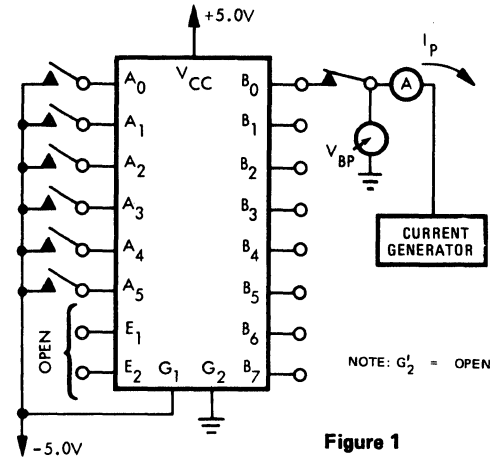


Figure 1
PROGRAMMING CONNECTIONS

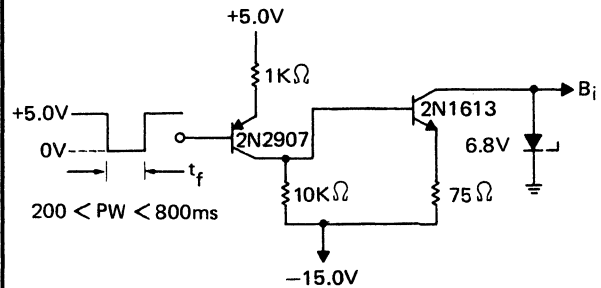


Figure 2
PROGRAMMING CIRCUIT

PROGRAMMING

Programming the HPROM-0512 is a simple operation which can be accomplished with a minimum of equipment. A negative going voltage pulse is applied to each output terminal where the initial logic "zero" is to be changed to a logic "one." The power supply and ground connections described below ensure that alteration of a specific logic element will not occur under normal operating conditions.

The following is the recommended procedure for reliably programming the HPROM-0512.

1. Connect the HPROM-0512 as shown in Figure 1. To address a particular word in memory, set the input switches to the binary equivalent of that word, where a logic "zero" is -5.0V and a logic "one" is an open circuit. (Do not return to supply.) All output bits (B_0, B_1, \dots, B_7) of this word are now available for programming.
2. With the output of the current generator limited to 100mA, apply a negative going pulse to the pin associated with the first bit to be changed from a "zero" to a "one". This is most easily accomplished by connecting the negative terminal of a variable power supply to the proper output pin and manually increasing the voltage to approximately 6.0V.

(The circuit shown in Figure 2 can be used in more automated programming systems. This circuit generates a fusing pulse which is at the proper voltage and current levels for fast, reliable programming. Most devices will program with input pulse widths (PW) as low as 200ms.)

Verify the bit programed by returning the device to the read mode and connecting a load resistor to +5V.

3. Skipping any bit which is to remain a "zero," repeat Step 2 for each "one" in the word being addressed. (For maximum reliability, program only one bit at a time.)
4. Set the next input address and repeat Steps 2 and 3. This procedure repeated for each input address for which a specific output word pattern is desired. Note that all addresses do not have to be programmed at the same time, nor do all output bits for a given address. A "zero" can always be changed to a "one" simply by repeating Steps 1 and 2. A "zero" once programmed to "one" cannot be reprogrammed to "zero."

The procedure given above is intended merely to convey the mechanics of programming the HPROM-0512. Obviously, more sophisticated electronic methods can be devised to automate the process and minimize the time required for programming. Such a system is used by Harris to custom-program ROM's for customers whose memory configurations are already established and also for certain standard patterns. This particular system operates with punched card inputs which convey the programming information and also provide the test conditions for each programmed ROM.

APPLICATION INFORMATION

POWER STROBE

Since the HPROM-0512 is a permanent memory, V_{CC} may be removed from the chip during periods when the memory is not being accessed thus reducing the average power consumption. A circuit which performs this function is shown in Figure 1. Using the components shown, the propagation delay from the power strobe to the first output word (t_{s1}) becomes $\sim 140\text{ns}$. Figure 2 shows the variation in t_{s1} as a function of temperature.

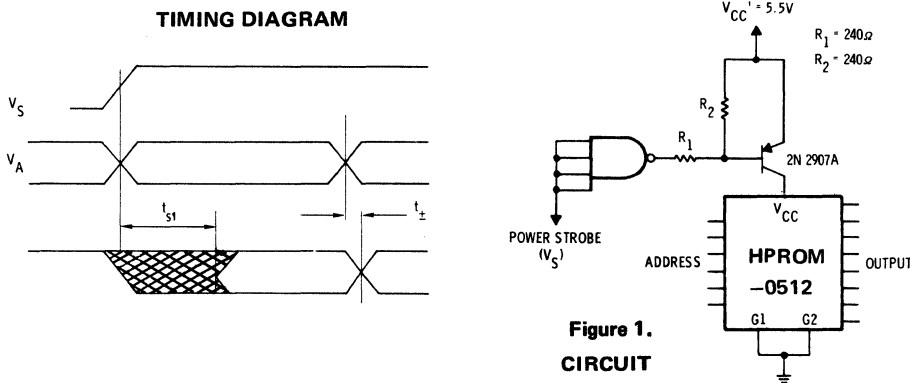


Figure 1. CIRCUIT

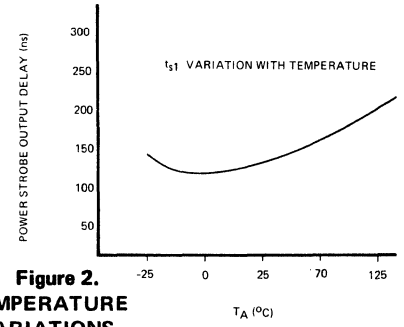
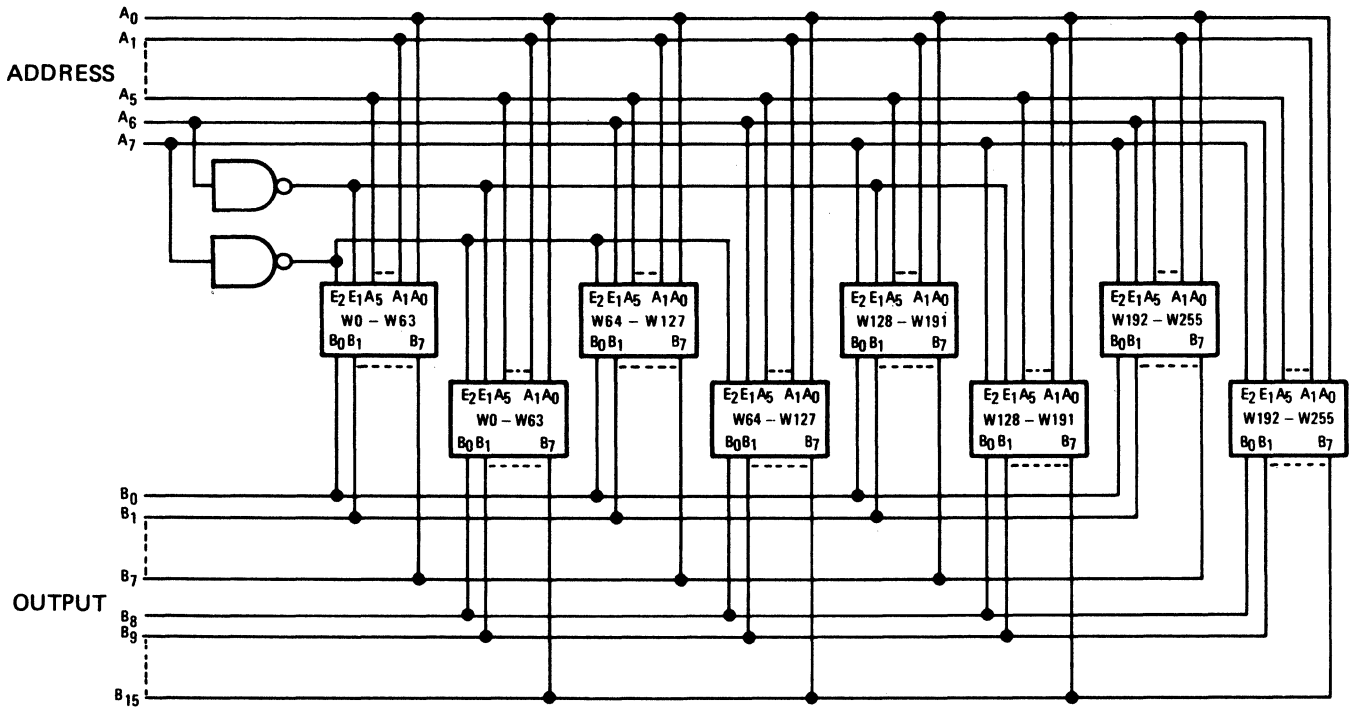


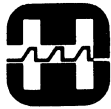
Figure 2. TEMPERATURE VARIATIONS

EXPANDABILITY



The HPROM-0512 is easily expanded in both bit and word dimensions. Expanding in the word dimension is accomplished by using the E_1 and E_2 Enable Inputs as further decoding elements for the input address and wiring together (WIRE-OR) two or more output pins from corresponding bits of different words. The "WIRE-OR" connection results in increased capacitance and leakage at the output node as each additional package is connected. Expansion in the bit dimension is accomplished by paralleling corresponding address pins on two or more units. The Block Diagram above depicts a 256 word by 16-bit system.

MEMORY



HARRIS
SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

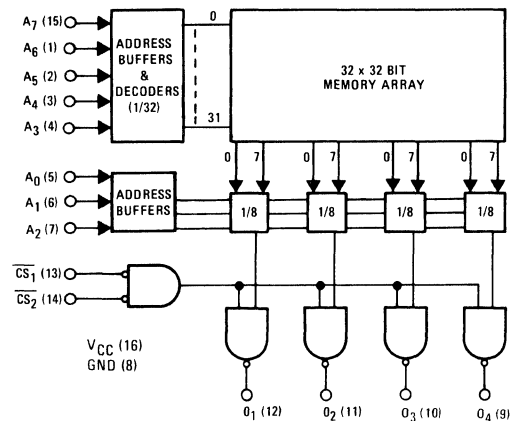
HPROM-1024/1024A

*1024-Bit Field Programmable
Bipolar PROM™*

FEATURES

- FIELD PROGRAMMABLE
- 256 / 4 BITS PER WORD
- FULLY DECODED
- DTL / TTL COMPATIBLE
- 50ns ACCESS TIME
- PROVEN RELIABLE NICHROME FUSES
- LOW INPUT CURRENT $\leq 0.25\text{mA}$
- SINGLE 5.0V POWER SUPPLY
- EXPANDABLE – “WIRED-OR” OUTPUTS WITH CHIP SELECT INPUT
- AVAILABLE IN MILITARY AND COMMERCIAL TEMPERATURE RANGES

BLOCK DIAGRAM



DESCRIPTION

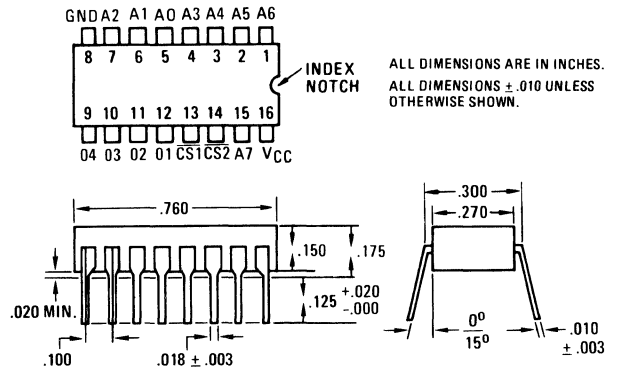
The HPROM-1024 (3-State) and the HPROM-1024A (Open Collector) are fully decoded, high speed, 1024-bit, field programmable ROM's organized as 256 words by 4 bits per word. Field programmable implies that, by following a simple programming procedure, users are able to program the PROM to any custom pattern to satisfy their system requirements.

The HPROM-1024 and the HPROM-1024A are identical except for the output stage. The HPROM-1024A has an Open Collector output while the HPROM-1024 has a third high impedance state output, allowing the device to work in a "Wire - OR" configuration. The third state is activated by disabling the device (\overline{CS}_1 or \overline{CS}_2 High).

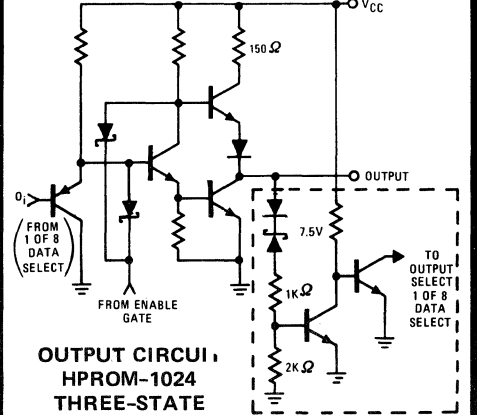
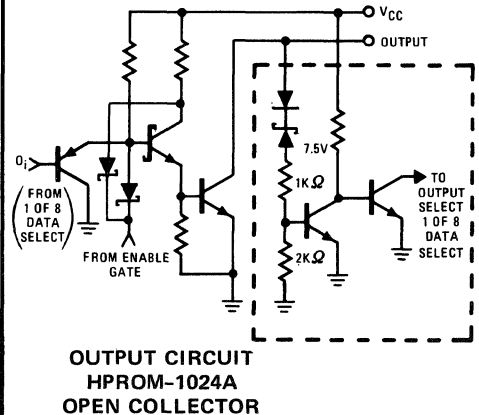
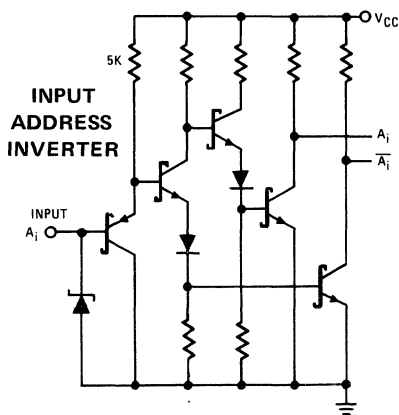
The HPROM-1024/1024A are supplied with all bits storing a Logical "1" (Output High) and can be selectively programmed for a Logical "0" (Output Low). The addressing scheme for programming and reading the information in the system is the same.

PACKAGE

CODE 1D 16 LEAD CERAMIC D.I.P.



INPUT/OUTPUT SCHEMATICS



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS:

Output or Supply Voltage	7.0V
Address/Enable Input Voltage	5.5V
Address/Enable Input Current	-20mA
Output Sink Current	70mA
Storage Temperature	+150°C
Operating Temperature (Case)	+125°C
Maximum Junction Temperature	+175°C
$\theta_{jC} = 25^{\circ}\text{C/W}$ (Cerdip); $\theta_{jA} = 80^{\circ}\text{C/W}$ (Cerdip)	

Note:

Stresses above those listed under the "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

ELECTRICAL CHARACTERISTICS (Operating Mode)

TEST CONDITION: $V_{CC} = 5.0 \pm 5\%$, $T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ (HPROM-1024-2, HPROM-1024A-2)
 $V_{CC} = 5.0 \pm 5\%$, $T_A = 0^{\circ}\text{C}$ to $+75^{\circ}\text{C}$ (HPROM-1024-5, HPROM-1024A-5)

unless otherwise specified.

PARAMETER	SYMBOL	HPROM-1024			HPROM-1024A			UNITS	TEST CONDITIONS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
Address/Chip Select "1" Input Current	I_{RA}, I_{RE}			*40			*40	μA	$V_{IH} = V_{CC} \text{ Max.}$ $V_{IL} = 0.45\text{V}$
	"0" I_{FA}, I_{FE}			*-0.25			*-0.25		
Input Clamp Voltage	V_{Clamp}		-0.7	*-1.0		-0.7	*-1.5		$V_{CC} = V_{CC} \text{ Min.}$ $I_{Clamp} = -10\text{mA}$
Input Threshold Voltage	"1" V_{IH}	2.0			2.0			V	
	"0" V_{IL}			0.8			0.8	V	
D.C. Output Voltage	"1" V_{OH}	*2.4					N.A.	V	$I_{OL} = 15\text{mA}$
	"0" V_{OL}			*0.45	N.A.	N.A.	*0.45	V	
Output Leakage "1"	I_{OH}	N.A.	N.A.	N.A.			*100	μA	$V_{OH} = V_{CC} \text{ Max.}$
Output Disabled Current	I_{OE}			*100			*100	μA	$V_{OH} = 2.4\text{V}$, $V_{E1}/V_{E2} = 2.0\text{V}$
Power Supply Current	I_{CC}			*130			*130	mA	All Inputs Grounded. $V_{CC} = V_{CC} \text{ Max.}$
A.C. Address to Output	t_{A+}		50	*70		50	*70	ns	$T_A = +25^{\circ}\text{C}$
	t_{A-}		50	*70		50	*70	ns	
Enable Access Time	t_{E-}		20	*35		20	*35	ns	$V_{CC} = 5.0\text{V}$
	t_{off+}		20	*35		20	*35	ns	

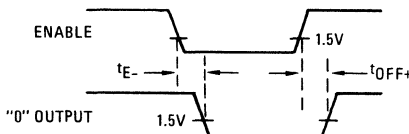
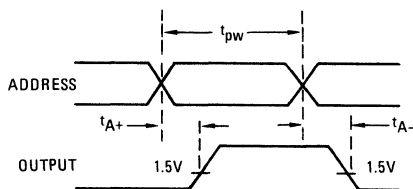
*100% Tested For DASH 8

CAPACITANCE (1): $T_A = 25^{\circ}\text{C}$

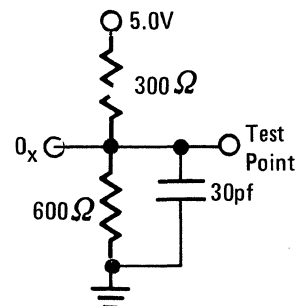
PARAMETER	SYMBOL	LIMITS		UNIT	TEST CONDITION	
		TYP.	MAX.			
Add. Input Cap.	$C_{IN A}, CS2$	7	15	pf	$V_{CC} = 5\text{V}$ $V_{IN} = 2.0\text{V}$	$T_A = 25^{\circ}\text{C}$
Chip Select Input Cap.	C_{CS1}	10	20	pf	$V_{CC} = 5\text{V}$ $V_{IN} = 2.0\text{V}$	
Output Cap.	C_{OUT}	6	12	pf	$V_{CC} = 5\text{V}$ $V_{OUT} = 2.0\text{V}$	

NOTE (1): These parameters are only periodically sampled and are not 100% tested.

SWITCHING TIME DEFINITIONS

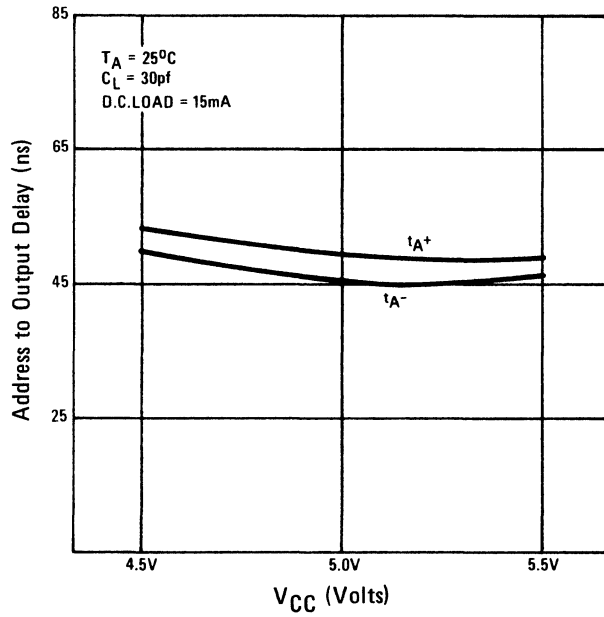


A.C. TEST LOADS

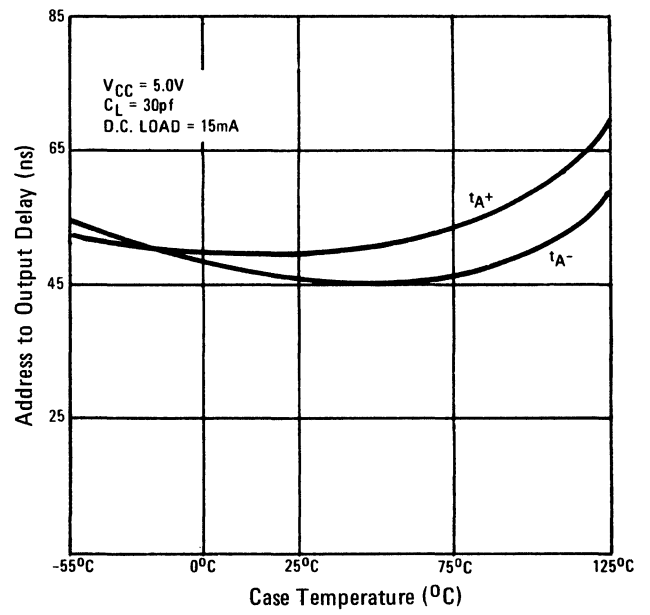


TYPICAL A.C. CHARACTERISTICS

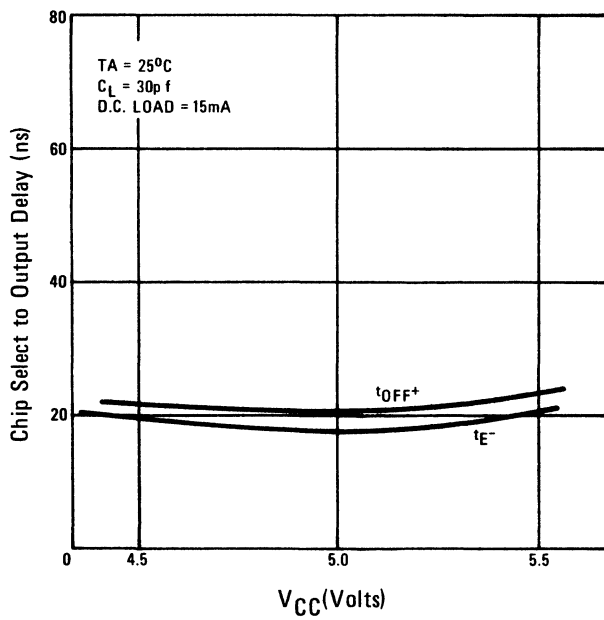
ADDRESS TO OUTPUT DELAY
VS. SUPPLY VOLTAGE



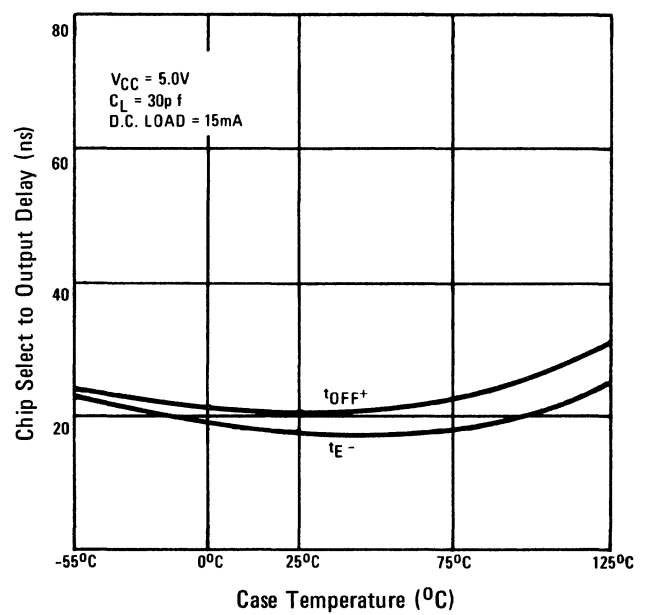
ADDRESS TO OUTPUT DELAY
VS. CASE TEMPERATURE



CHIP SELECT TO OUTPUT DELAY
VS. SUPPLY VOLTAGE



CHIP SELECT TO OUTPUT DELAY
VS. CASE TEMPERATURE



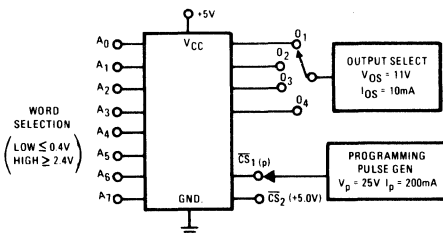
PROGRAMMING

The HPROM-1024/1024A is manufactured with all bits/outputs Logical "1" (Output High). Any desired bit/output can be programmed to a Logical "0" (Output Low) by following the simple procedure shown below. One may build his own programmer to satisfy the specifications described in Table 1, or buy any of the commercially available programmers which meet these specifications. The HPROM-1024/1024A can be programmed automatically or by the manual procedure shown below.

PROGRAMMING SPECIFICATIONS

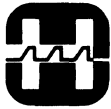
PARAMETER	SYMBOL	MIN.	RECOMMENDED VALUE	MAX.	UNITS.	NOTES
Address Input Voltage	V_{IH}	2.4	5.0	5.0	V	Address inputs should not be left open for V_{IH} .
	V_{IL}	0.0	0.0	0.4	V	
Chip Select 2 Voltage (Pin 14)	$V_{\overline{CS}2}$	2.4	5.0	5.0	V	
Programming Voltage \overline{CS}_1 (Pin 13)	$V_{\overline{CS}1 (P)}$	24.0	25	25.5*	V	*Including overshoot
Programming Current Limit \overline{CS}_1 (Pin 13)	$I_{\overline{CS}1 (P)}$		200	300	mA	125mA is the typical programming current requirement.
Programming Pulse Width	T_{PW}	1	10	100	mS	$t_{RISE} = 200 \text{ SEC} \pm 20\%$
Output Select Voltage	V_{OS}	10.5	11	11.5	V	
Output Select Current limit	I_{OS}		10	20	mA	2mA is the typical current requirement.
Power Supply Voltage	V_{CC}	5.0	5.0	5.25	V	
Case Temperature	T_C	-25	25	75*	$^{\circ}\text{C}$	*20% duty cycle with $T_A = 25^{\circ}\text{C}$

MANUAL PROGRAMMING



The HPROM-1024/1024A may be programmed using the method shown in the figure on the left.

- (1) Select the word to be programmed by applying the appropriate voltages to the address pins A_0 through A_7 .
- (2) Apply 11.0 volts to the output associated with the bit to be programmed. The other outputs may be left open or connected to any normal circuitry which does not apply more than 5 volts to these outputs. Only one output is programmed at a time.
- (3) Apply the 25 volt programming pulse to the Input Pin \overline{CS}_1 (Pin 13). The recommended programming pulse width is 10ms. However, programming speed may be enhanced by making initial attempts at 1msec. Bits which do not program with these pulse widths may be programmed either by repeating with 10ms pulses or by increasing the programming pulse width to 100ms. The multiple application of the programming pulse or the increased pulse width in no way affects the reliability of the device. The case temperature of the device being programmed, however, must not exceed 75°C . The 20% duty cycle (at $T_A = 25^{\circ}\text{C}$) generally maintains a T_{CASE} of 75°C . Bits which do not program when subjected to multiple pulses totaling 500 msec may be returned for replacement. Returned units should be accompanied with word and bit location of fuse which did not program.
- (4) To verify that the output has been programmed following each application of the programming pulse, being Pin 13 and Pin 14 to 0.4 volts or less. V_{CC} should be reduced to $4.0 + .2$ volts to guardband full temperature and volume range operations.
- (5) The above procedure is repeated to program other bits on the chip.



HARRIS
SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HPROM-8256

256-Bit, Bipolar PROM

FEATURES

- FIELD PROGRAMMABLE
- 32 WORDS/8BITS PER WORD
- FULLY DECODED
- DTL/TTL COMPATIBLE
- 40NS ACCESS TIME
- PROVEN RELIABLE NICHROME FUSES
- SINGLE 5V POWER SUPPLY
- STATIC OUTPUT WITH FANOUT OF 10
- AVAILABLE IN MILITARY AND COMMERCIAL TEMPERATURE RANGES
- EXPANDABLE – “WIRED-OR” OUTPUTS – CHIP ENABLE INPUT

TRUTH TABLE

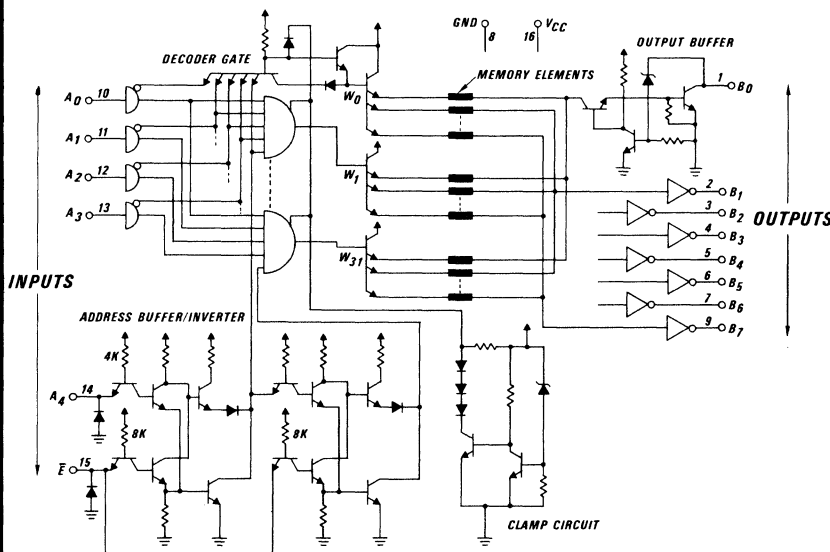
The HPROM-8256 is another in a series of field programmable read-only memories from Harris Semiconductor. Field programming implies that the device (packaged with logical “0”s in all 256 memory locations) can be programmed electronically by the user to any specific pattern using the simple procedure shown on page 4.

Referring to the circuit diagram below, the status of any bit is determined by the condition of the “memory element” in that bit location. For a logical “0” output, the memory element is in the conducting state and the output transistor is turned “on”. Programming, then, involves opening selected memory elements to prevent current flow to the output transistor, creating a logical “1” in each programmed bit location.

WORD NUMBER	INPUTS						OUTPUTS							
	\bar{E}	A ₄	A ₃	A ₂	A ₁	A ₀	B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀
X	1	X	X	X	X	X	1	1	1	1	1	1	1	1
0	0	0	0	0	0	0	*	*	*	*	*	*	*	*
1	0	0	0	0	0	1	*	*	*	*	*	*	*	*
2	0	0	0	0	1	0	*	*	*	*	*	*	*	*
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
31	0	1	1	1	1	1	*	*	*	*	*	*	*	*

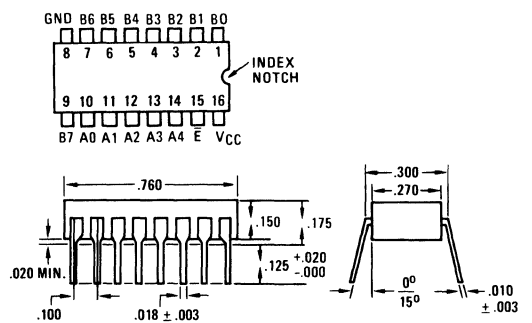
NOTE: X = DON'T CARE

CIRCUIT DIAGRAM



PACKAGE

CODE 1D 16 LEAD CERAMIC D.I.P.



ALL DIMENSIONS ARE IN INCHES.
ALL DIMENSIONS ± .010 UNLESS OTHERWISE SHOWN.

*PROM is a trademark of Harris Semiconductor for its family of field programmable read-only memories.

MEMORY

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Operating), V_{CC}	7.0V
Address/Enable Input Voltage, V_A, V_E	-1.5V to +5.5V
Output Supply Voltage (Operating), V_{BS}	-1.5V to +7.0V
Output Sink Current, I_{OL}	-30mA
Input Current	-30mA
Storage Temperature	-65°C to +150°C
Operating Temperature	-55°C to +125°C

ELECTRICAL CHARACTERISTICS

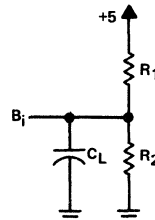
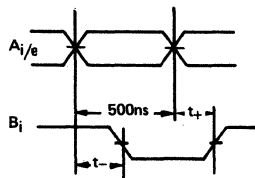
TEST CONDITIONS

HPROM-8256-2 ($V_{CC} = +5.0V \pm 10\%$, $T_A = -55^\circ C$ to $+125^\circ C$)
 HPROM-8256-5 ($V_{CC} = +5.0V \pm 5\%$, $T_A = 0^\circ C$ to $+75^\circ C$)

PARAMETER	SYM	HPROM-8256-2 (-55°C to +125°C)			HPROM-8256-5 (0°C to +75°C)			UNITS	TEST CONDITIONS
		MIN	TYP	MAX	MIN	TYP	MAX		
ENABLE Current	"1" I_{RE}			* 100			100	μA	$V_{IN} = 4.5V$
	"0" I_{FE}			* -1.6			-1.6	mA	$V_{IN} = 0.4V$
Address Current	"1" I_{RA}			* 100			100	μA	$V_{IN} = 4.5V$
	"0" I_{FA}			* -1.6			-1.6	mA	$V_{IN} = 0.4V$
Input Threshold Voltage	"1" V_{IH}	2.0			1.9			V	
	"0" V_{IL}			0.8			0.85	V	
Output "0" Voltage	V_{OL}			* 0.45			0.45	V	$V_{CC} = V_{MIN}$, $I_{OL} = 10mA$
Output "1" Leakage	I_{OH}			* 200			200	μA	$V_{OH} = 5.25V$
Input Clamp Voltage	V_C			* -1.5V			-1.5V	V	$I_{IN} = -5.0mA$
Power Supply Current	(Quiescent)			* 80			80	mA	$V_E = V_{IH}$, Outputs open
	(Operating)			* 100			110	mA	$V_E = V_{IL}$, Outputs open
Address/Enable to Output Fall Delay	t_f		40	50		40	50	ns	$R_1 = 470\Omega$, $R_2 = 1K\Omega$, $C_L = 30pF$
Address/Enable to Output Rise Delay	t_r		40	50		40	50	ns	$T = 25^\circ C$ $V_{CC} = 5.0V$

*100% Tested For DASH 8

SWITCHING TIME DEFINITIONS



1. All measurements referenced to +1.5V.
2. Address rise and fall times $\leq 10ns$.

MEMORY

PROGRAMMING

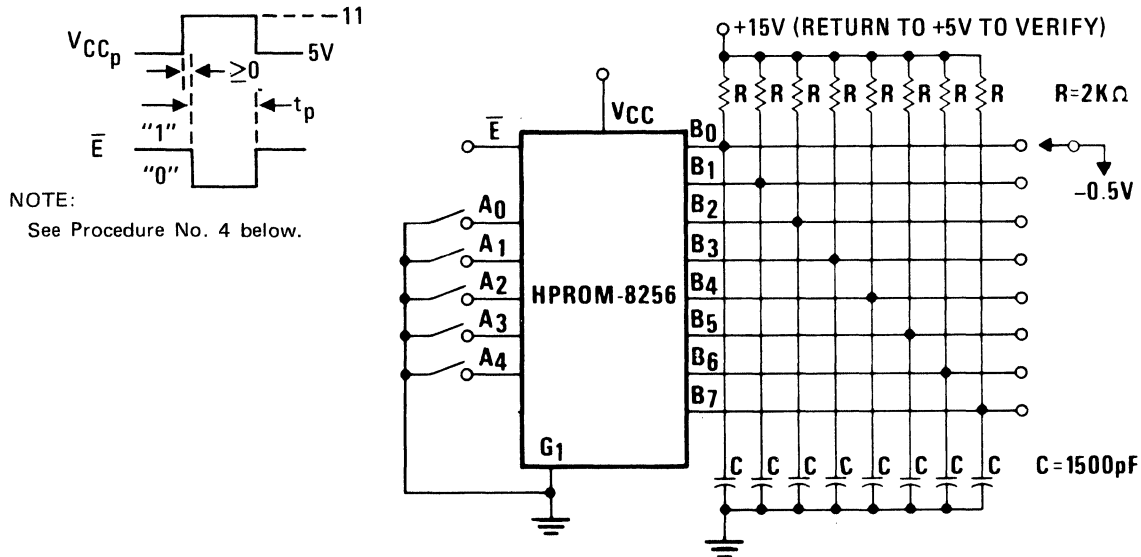


FIGURE 1

REQUIREMENTS

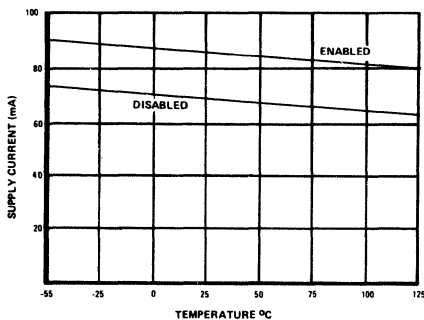
	RECOMMENDED VALUE	LIMITS		UNITS	NOTES
		MIN.	MAX.		
Enable/Address Input Low Current			-6.0	mA	$V_{IN} = 0.4V$
Enable/Address Input Voltage	low	GND	0.4	V	
	high	OPEN	-	V	
Programming Voltage (V_{CCp})	11		11.5	V	$I_{Limit} = 250mA$
Programming Pulse Width (t_p)	20	0.5	800*	ms	*All devices should program with $t_p \leq 800ms$.
Programming Output Voltage	-0.5	-1.0	0.0	V	
Non-Programming Output Current	4.0	2.0	8.0	mA	Output voltage nominally 8.3V.
T_{CASE}			75	$^{\circ}C$	
Duty Cycle ($T_A = 25^{\circ}C$)	60		80	%	

PROCEDURE

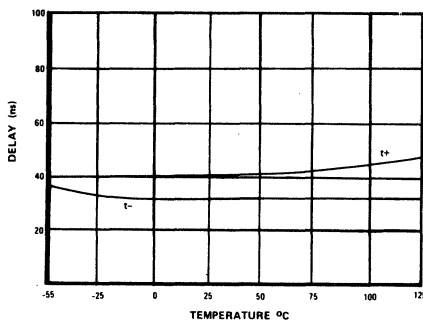
1. Connect the PROM as shown in figure 1.
2. Address the desired word by applying an open circuit for Logic "1" and ground for Logic "0". (High voltage open collector TTL inputs may also be used.)
3. Select first output bit to be programmed by taking that output to a negative 0.5V.
4. Disable device ($E \geq 2.5V$). (Nonprogramming outputs will rise to approximately 8.3V) Raise supply to +11V and enable device ($E \leq 0.4V$) to program the selected memory element. (Enable signal must not be applied prior to raising V_{CC} to +11V.) Device should be enabled for t_p milliseconds. For fastest programming results the first attempts should be one millisecond with subsequent attempts greater than 10 milliseconds to maximize programmability.
5. Verify the bit programmed by lowering the +15V to +4.5V and then enabling the device.
6. In the event the device does not verify, repeat steps 2 - 5. Bits which do not program with a total of 800 msec of programming time are considered unprogrammable and may be returned for replacement. Devices returned must contain word and bit numbers of bits which did not program.
7. Repeat steps 3 through 6 to complete programming the remaining bits in the selected word.
8. Repeat steps 2 through 7 to complete programming the remaining words in the device.

CHARACTERISTIC CURVES

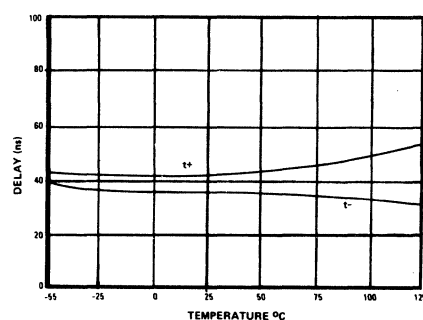
POWER SUPPLY CURRENT vs TEMPERATURE



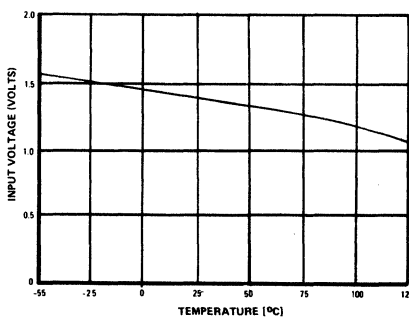
ADDRESS TO OUTPUT PROPAGATION DELAY vs TEMPERATURE



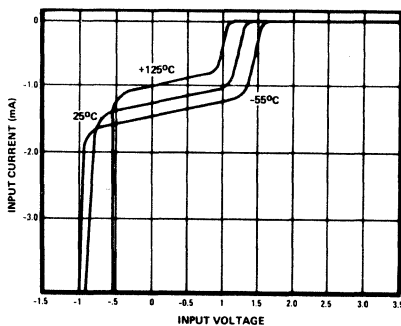
ENABLE TO OUTPUT PROPAGATION DELAY vs TEMPERATURE



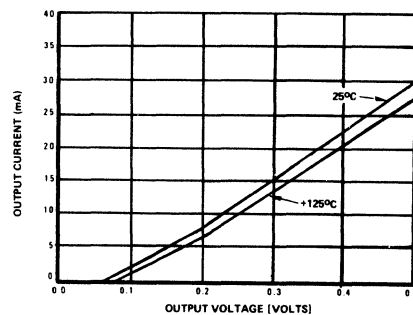
INPUT THRESHOLD vs TEMPERATURE



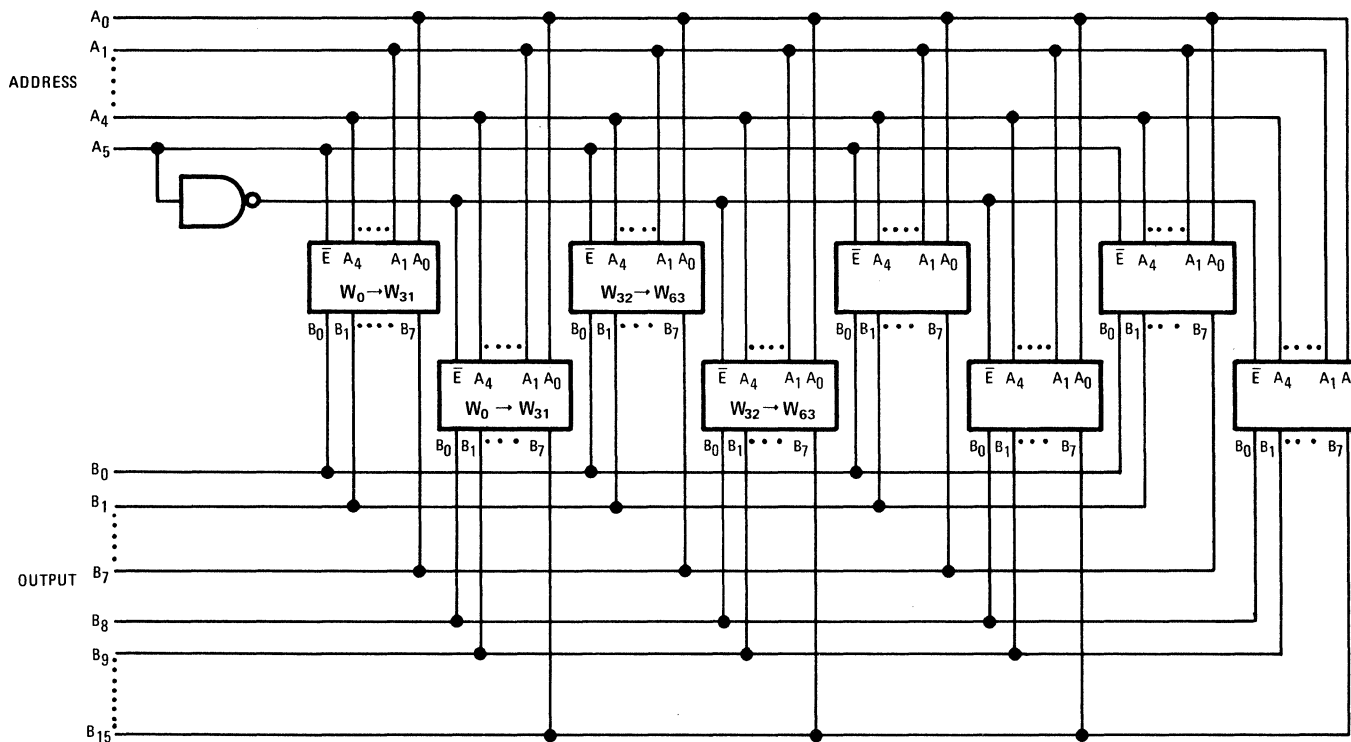
INPUT CURRENT vs INPUT VOLTAGE



OUTPUT LOW V-I CHARACTERISTICS

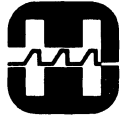


EXPANDABILITY



DASH 8

DASH 8



HARRIS
SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

DASH 8

MIL-STD-883

OFF-THE-SHELF DELIVERY

MIL-STD-883/MIL-M-38510 Reliability Assurance Program

INTRODUCTION

STATEMENT OF SCOPE

This section establishes the detail requirements for Harris' Circuits screened and tested under the DASH 8 Program.

The Harris DASH 8 Devices pass the screening requirements of the latest issue of MIL-STD-883, Method 5004, Class B, and the requirements as specified in this document.

APPLICABLE DOCUMENTS

The following documents form a part of this section to the extent referenced herein:

MIL-M-38510	"Microcircuit Quality and Reliability Assurance, General Specification for."
MIL-Q-9858A	"Quality Program Requirements"
MIL-STD-883	"Test Methods and Procedures for Microelectronics"
NASA Publication 200-3	"Inspection System Provisions"

Harris maintains a product assurance program (PAP) using MIL-M-38510 as a guide. Harris Product Assurance Program assures compliance with the requirements and quality standards of control drawings and the requirements of this specification.

Systems and procedures used are in accordance with NASA Publication 200-3, MIL-Q-9858A and MIL-M-38510.

The DASH 8 Program will also be found useful by those Harris customers who must generate their own procurement specifications. Use of the enclosed Harris Standard Test Tables, Test Parameters, and Burn-In Circuits will aid in reducing specification negotiation time. CMOS is also available in DASH 8, for further information on CMOS DASH 8 see our CMOS Catalog or contact your local sales representative.

HARRIS SEMICONDUCTOR DASH 8 FLOW

MIL-STD-883, METHOD 5004, CLASS B,
100% SCREENING PRODEDURE

	SCREEN	METHOD
①	Internal Visual (Precap)	2010 Condition B
②	Stabilization Bake	1008, Condition C, 24 Hours minimum
③	Temperature Cycling	1010, Condition C
④	Constant Acceleration	2001, Condition G Y ₁ Plane, 30K G's minimum
⑤	Seal, Fine Leak	1014, Condition (As applicable)
⑥	Seal, Gross Leak	1014, Omit Step 1, No vacuum Preconditioning Step 2
⑦	Initial Electrical	Harris Specifications
⑧	Burn-In	Method 1015, 168 hours @ 125°C (Burn-In Circuits Enclosed. See page Da-8.)
⑨	Final Electrical 9.1 D. C. Tests at 25°C Maximum and minimum operating temperatures 9.2 A. C. Tests at 25°C	Per appropriate Harris DASH 8 Data Sheet only those items identified by * are tested 100%.
⑩	External Visual	Method 2009
⑪	Lot Acceptance	Group A, Table 1, Subgroup 1, 2, 3 & 4

NOTE:

LOT DEFINITION: Production Lot and Inspection Lot shall be as defined in MIL-M-38510.

TRACEABILITY: All devices are assigned date code identification that provides traceability back to the inspection lot.

BRANDING: All devices are branded with the HX-XXX-8 and EIA data code.

AGED PRODUCT: Product that has been held for more than twelve months will be rescreened prior to shipment.

ADDITIONAL REQUIREMENTS: Attributes data will be supplied on Group A Lot Acceptance upon request.

Generic data from Harris' Reliability Add-On Program is available upon request; The objective of Harris Reliability Add-On Program is to provide a continuous life and environmental monitor for all product families in manufacturing. This program provides life test performance results to fulfill customer reliability data requirements and to verify package integrity. The Reliability Add-On Program is supplemental to customer funded Lot Qualification.

For customers desiring Lot Qualification, Harris Semiconductor will perform the Group A, Group B and Group C test to MIL-STD-883, Method 5005 as defined herein for an additional charge.

DASH 8

HARRIS RELIABILITY ADD-ON PROGRAM

Generic data from Harris' Reliability Add-On Program is available upon request; The objective of Harris Reliability Add-On Program is to provide a continuous life and environmental monitor for all product families in manufacturing. This program provides life test performance results to fulfill customer reliability data requirements and to verify package integrity. The Reliability Add-On Program is supplemental to customer funded Lot Qualification.

The Harris Reliability Add-On Program is an on-going program that provides generic product and package testing data that can be equated to MIL-STD-883 Group B and Group C tests. The data derived from the Add-On Program forms the basis for the Harris Reliability Bulletins published under the cognizance of the Harris Reliability Manager.

The Reliability Add-On Program section that is applicable to the DASH 8 program is listed below.

PRODUCT TYPE	SCHEDULE WITH SAMPLE SIZE	STRESS CONDITIONS	COMMENTS
<u>GENERIC STANDARD</u>	<ul style="list-style-type: none"> a) 1,000 hours sample of each generic type per quarter. b) Extend to 5,000 hours - 1 sample per quarter. c) Extend to 10,000 hours - 1 sample per half year. d) Sample size - 10 per stress medium for PROMs; 14/36 per stress medium for linears. e) Variables data points at 0, 168, 500, 1000, 2000, 5000, and 10,000 hours. 	<ul style="list-style-type: none"> a) $T_A = +125^{\circ}\text{C}$ operating life b) $T_A = +175^{\circ}\text{C}$ storage life 	
<u>PACKAGE QUALIFICATION</u>	<ul style="list-style-type: none"> a) One generic type per quarter per package type. b) Sample size - 50 good and 50 reject devices per package type for package qual; 	<ul style="list-style-type: none"> a) Reference Reliability Standard Operating Procedure (RSOP) -002 and -003 	Reason: Verify continued package integrity.
<u>SPECIAL TESTS</u> AI step coverage	<ul style="list-style-type: none"> a) One generic type, per month as a minimum 	SEM Analysis	Reason: To verify aluminum coverage over oxide steps.

HARRIS DEVICE QUALIFICATION PROCEDURE

MIL-STD-883, METHOD 5005, GROUP B (NOTE 1)

TEST	METHOD	CONDITION	QUALITY CONFORMANCE INSPECTION (NOTE 2)	QUALIFICATION INSPECTION
			CLASS B LTPD	CLASS B LTPD
SUBGROUP 1 Physical Dimensions	2016		15	10
SUBGROUP 2 (a) Resistance to solvents	2015	Failure criteria from design and construction requirements of applicable procurement document Test condition C or D	3 devices (no failures)	3 devices (no failures)
(b) Internal Visual and mechanical	2014		1 device (no failures)	1 device (no failures)
(c) Bond strength (NOTE 3) Ultrasonic or wedge	2011 (see 3.8)		15	10
SUBGROUP 3 Solderability (NOTE 4)	2003	Soldering temperature of 260 ± 10°C.	15	10
SUBGROUP 4 Lead integrity Seal (NOTE 5) (a) Fine (b) Gross	2004 1014	Test condition B ₂ As applicable.	15	10

- NOTES:
1. Electrical reject devices from the same inspection lot may be used for all subgroups when end point measurements are not required.
 2. Generic data from Harris Reliability Add-On Program available upon request.
 3. Unless otherwise specified, at the manufacturers option, test samples for bond strength may be selected randomly immediately following internal visual (method 5004) prior to sealing.
 4. The LTPD applies to the number of leads inspected except in no case shall less than three devices be used to provide the number of leads required.
 5. Omit step 1 and vacuum preconditioning of step 2.

HARRIS DEVICE QUALIFICATION PROCEDURE

MIL-STD-883, METHOD 5005, GROUP C

TEST	METHOD	CONDITION	QUALITY CONFORMANCE INSPECTION (NOTE 6)	QUALIFICATION INSPECTION
			CLASS B LTPD	CLASS B LPTD
<u>SUBGROUP 1</u> (NOTE 1) Thermal shock Temperature cycling Moisture resistance Seal (NOTE 5) (a) Fine (b) Gross Visual Examination (NOTE 2) End point elec. parameters	1011 1010 1004 1014	Test condition B as a minimum. Test condition C. As applicable. As specified in the applicable procurement document.	15	10
<u>SUBGROUP 2</u> (NOTE 1) Mechanical shock Vibration, variable frequency Constant acceleration Seal (NOTE 5) (a) Fine (b) Gross Visual Examination (NOTE 3) End point elec. parameters	2002 2007 2001 1014	Test condition B Test condition A Test condition E As applicable. As specified in the applicable procurement document.	15	10
<u>SUBGROUP 3</u> High temperature storage (NOTE 4) End point elec. parameters	1008	+50 150 -25 °C storage, 1000 hours. As specified in the applicable procurement document.	7	5
<u>SUBGROUP 4</u> Operating life test (NOTE 4) End point elec. parameters	1005	Test condition to be specified in the applicable procurement document (1000 hours). As specified in the applicable procurement document.	5	3

- NOTES:
1. Devices used for environmental tests in subgroup 1 may be used for mechanical tests in subgroup 2.
 2. Visual examination shall be in accordance with method 1010 or 1011 at a magnification of 5X to 10X.
 3. Visual examination shall be performed at a magnification of 5X to 10X for evidence of defects or damage to case, leads, or seals resulting from testing (not fixturing). Such damage shall constitute a failure.
 4. See applicable life test circuit enclosed herein.
 5. Omit step 1 and vacuum preconditioning of step 2.
 6. Generic data from Harris Reliability Add-On Program available upon request.

BURN-IN/LIFE TEST CIRCUIT INDEX

LINEAR

ANALOG MULTIPLEXERS AND SWITCHES

MULTIPLEXERS		DRAWING NO.
HI-506	CMOS 16 Channel Analog Multiplexer	21
HI-506A	CMOS 16 Channel Analog Multiplexer	21
HI-507	Dual-8 CMOS Multiplexer	21
HI-507A	Dual-8 CMOS Multiplexer	21
HI-508A	8 Channel Analog Multiplexer	22
HI-509A	Dual 4-Channel Analog Multiplexer	23
HI-1818A	8 Channel Multiplexer	26
HI-1828A	Dual 4-Channel Multiplexer	27
SWITCHES		
HI-200	Dual SPST Analog Switch	19
HI-201	Quad SPST Analog Switch	20
HI-1800A	DPDT-Low Leakage 4-Channel Analog Switch	25

OPERATIONAL AMPLIFIERS

F. E. T. INPUT

HA-2000	F. E. T. Input Preamplifier	3
HA-2050	High Slew Rate F. E. T. Input Operational Amplifier	2
HA-2050A	High Slew Rate F. E. T. Input Operational Amplifier	2
HA-2060	Wide Band F. E. T. Input Operational Amplifier	2
HA-2060A	Wide Band F. E. T. Input Operational Amplifier	2

HIGH SLEW RATE

HA-2500	High Slew Rate Operational Amplifier	2, 8
HA-2502	High Slew Rate Operational Amplifier	2, 8
HA-2510	High Slew Rate Operational Amplifier	2, 8
HA-2512	High Slew Rate Operational Amplifier	2, 8
HA-2520	High Slew Rate Operational Amplifier	2, 8
HA-2522	High Slew Rate Operational Amplifier	2, 8
HA-2530	Wide Band High Slew Inverting Amplifiers	9

LOW NOISE WIDE BAND

HA-909	Low Noise, Operational Amplifier	1, 2
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LOW POWER

HA-2700	Low Power, High Performance Operational Amplifiers	13, 14
HA-2720	Low Power, Current Programmable Operational Amplifiers	15
HA-2730	Low Power, Dual, Current Programmable Operational Amplifiers	16

PRECISION HIGH ZIN WIDE BAND

HA-2600	High Impedance Operational Amplifiers	2, 10
HA-2602	High Impedance Operational Amplifiers	2, 10
HA-2620	Wide Band, High Impedance Operational Amplifiers	2, 10, 11
HA-2622	Wide Band, High Impedance Operational Amplifiers	2, 10, 11
HA-2650	Dual High Performance Operational Amplifiers	2

SPECIAL FUNCTION

HA-2400	PRAM Four Channel Operational Amplifiers	6
HA-2420	Sample and Hold, Gated Operational Amplifiers	7
HA-2630	High Performance Current Booster	12

ULTRA HIGH PRECISION

HA-2900	Chopper Stabilized Operational Amplifiers	18
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PHASE LOCKED LOOP

HA-2820	Phase Locked Loop	17
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SPECIAL INTERFACE CIRCUITS

HI-1080	8-Bit, D to A Convertor High Speed Monolithic	24
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VOLTAGE COMPARATOR

HA-2111	Precision Voltage Comparator	4, 5
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MEMORY

BIPOLAR MEMORY

GENERIC PROMS

HM-7610	1024-Bit, Bipolar Generic PROM (open collector)	29
HM-7611	1024-Bit, Bipolar Generic PROM (three state)	29
HM-7620	2048-Bit, Bipolar Generic PROM (open collector)	33
HM-7621	2048-Bit, Bipolar Generic PROM (three state)	33

HPROM

HPROM-0512	512-Bit, Bipolar PROM	30
HPROM-1024	1024-Bit, Bipolar PROM (three state)	32
HPROM-1024A	1024-Bit, Bipolar PROM (open collector)	32
HPROM-8256	256-Bit, Bipolar PROM	31

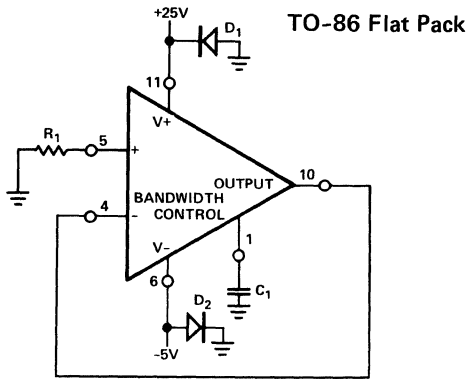
POWER/LOGIC STROBE

HD-6600	Quad Power Strobe	28
HD-6605	Quad Logic Strobe	28

BURN-IN CIRCUITS

1

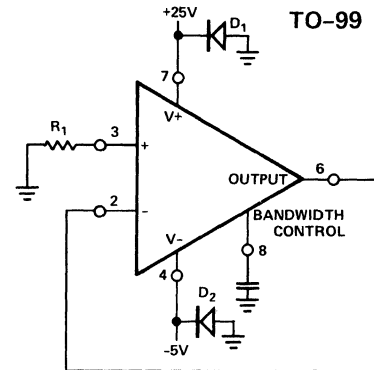
HA-909



NOTES:
 $T_A = +125^\circ\text{C}$
 $R_1 = 1\text{ Megohm}$
 $C_1 = 0.01\ \mu\text{F}, 100\text{V}$

2

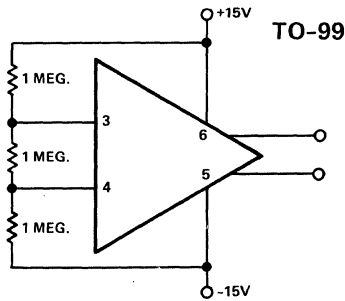
HA-909, HA-2500, HA-2502, HA-2510, HA-2512, HA-2520, HA-2522, HA-2600, HA-2602, HA-2620, HA-2622, HA-2050, HA-2050A, HA-2060, HA-2060A



NOTES:
 $T_A = +125^\circ\text{C}$
 $R_1 = 1\text{ Megohm}$
 $C_1 = 0.01\ \mu\text{F}, 100\text{V}$

3

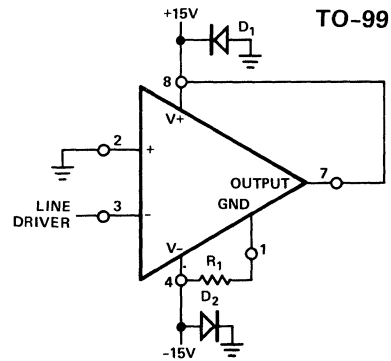
HA-2000



CIRCUIT TYPE:
 FET Front End
 DESIGNATION:
 HA-2000
 OPERATING LIFE TEST CONDITION:
 1) TEMPERATURE: $+125^\circ\text{C}$
 2) VOLTAGE: $\pm 15\text{ Volts}$

4

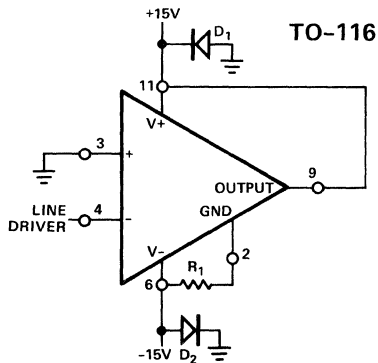
HA-2111



NOTES:
 $T_A = +125^\circ\text{C}$
 $R_1 = 300\ \Omega$
 $D_{1,2} = \text{IN4002}$
 Freq: 50 KHz @ 12V peak to peak

5

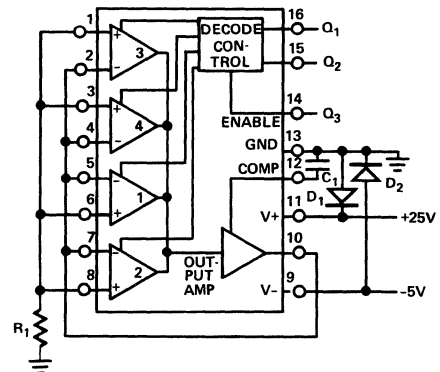
HA-2111



NOTES:
 $T_A = +125^\circ\text{C}$
 $R_1 = 300\ \Omega$
 $D_{1,2} = \text{IN4002}$
 Freq: = 50KHz @ 12V peak to peak

6

HA-2400



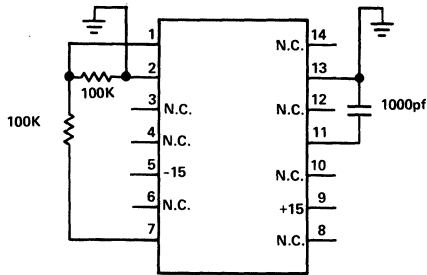
NOTES:
 $T_A = +125^\circ\text{C}$
 $R_1 = 100\text{K}\ \Omega$
 $C_1 = 910\text{pF}, 50\text{V}$
 $D_{1,2} = \text{IN4002}$
 Freq: $Q_1 = 100\text{KHz}; Q_2 = 50\text{KHz}; Q_3 = 25\text{KHz}$

BURN-IN CIRCUITS

7

HA-2420

TO-99

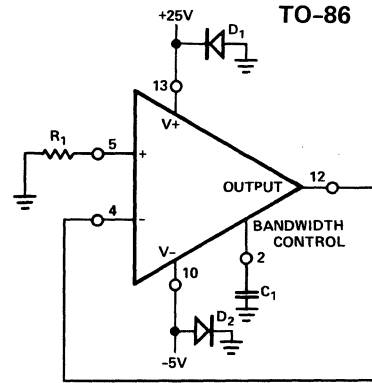


NOTE:
T_A = +125°C

8

HA-2500, HA-2502, HA-2510, HA-2512, HA-2520, HA-2522

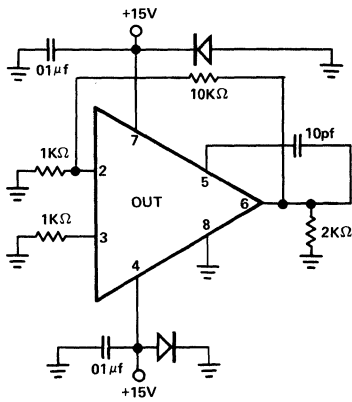
TO-86



NOTES:
T_A = +125°C
R₁ = 1 Megohm
C₁ = 0.01 μF, 50V

9

HA-2530

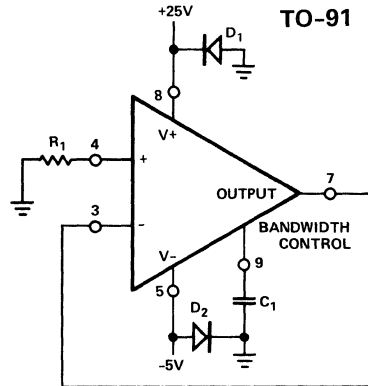


NOTE: T_A = +125°C

10

HA-2600, HA-2602, HA-2620, HA-2622

TO-91

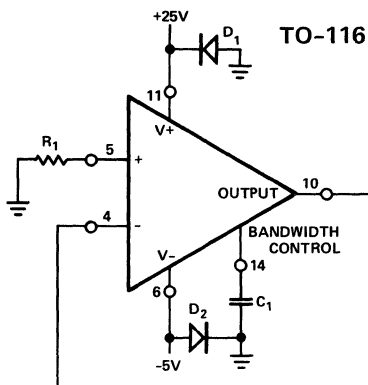


NOTES:
T_A = +125°C
R₁ = 1 Megohm
C₁ = 0.01 μF, 100V

11

HA-2620/2622

TO-116

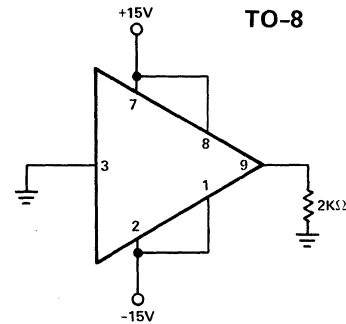


NOTES:
T_A = +125°C
R₁ = 1 Megohm
C₁ = 0.01 μF, 100V

12

HA-2630

TO-8

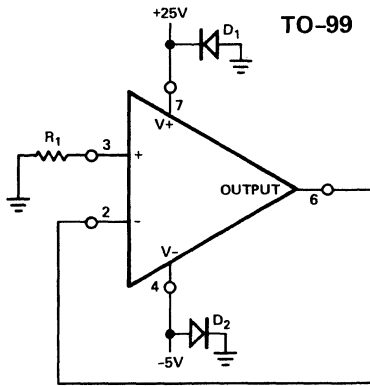


NOTE:
T_A = +125°C

BURN-IN CIRCUITS

13

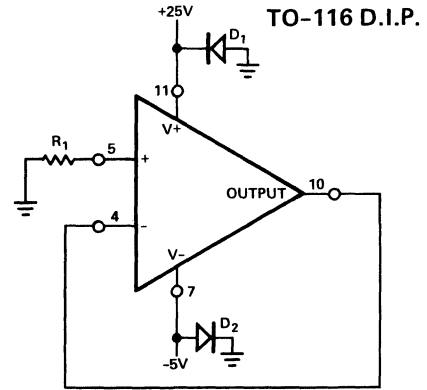
HA-2700



NOTES:
 $T_A = +125^{\circ}\text{C}$
 $R_1 = 1 \text{ Megohm}$

14

HA-2700

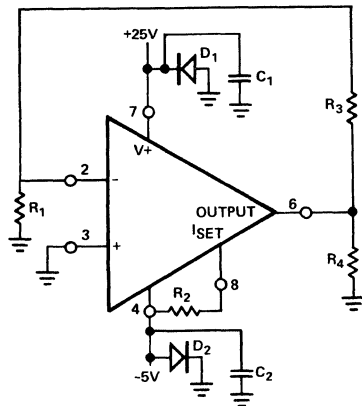


NOTES:
 $T_A = +125^{\circ}\text{C}$
 $R_1 = 1 \text{ Megohm}$

15

HA-2720

TO-99

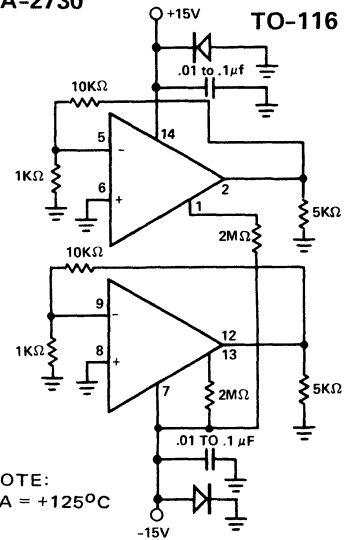


NOTES:
 $T_A = +125^{\circ}$
 $C_1 C_2 = 0.01 \text{ to } 0.1 \mu\text{F}$
 $R_1 = 1\text{K}\Omega$
 $R_2 = 2\text{M}\Omega$
 $R_3 = 10\text{K}\Omega$
 $R_4 = 5\text{K}\Omega$

16

HA-2730

TO-116

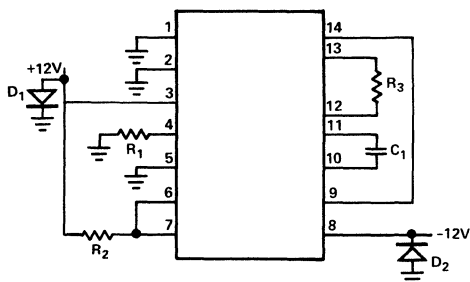


NOTE:
 $T_A = +125^{\circ}\text{C}$

17

HA-2820

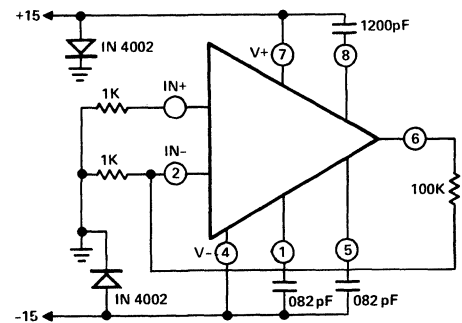
TO-116



NOTES:
 $T_A = +125^{\circ}\text{C}$
 $R_1 = 10\text{K}\Omega$
 $R_2 = 4.7\text{K}\Omega$
 $R_3 = 560\Omega$
 $C_1 = 01 \mu\text{F}$

18

HA-2900

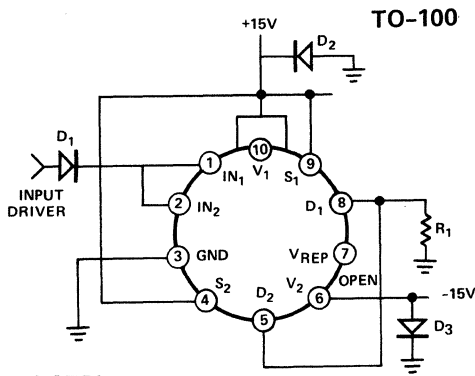


NOTE:
 $T_A = +125^{\circ}\text{C}$

BURN-IN CIRCUITS

19

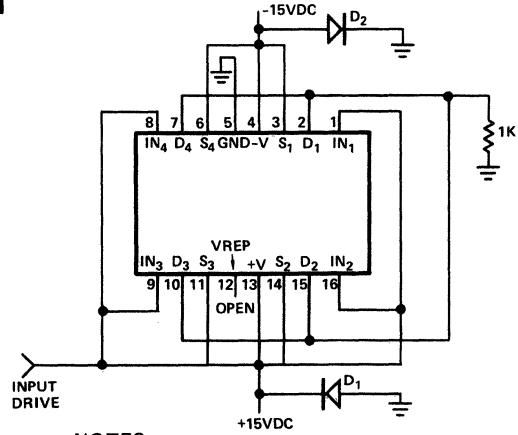
HI-200



NOTES:
 $T_A = +125^\circ\text{C}$
 $R_1 = 10\text{K}\Omega$
 $D_1 D_2 D_3 = \text{IN4002}$
 Freq: = 100KHz

20

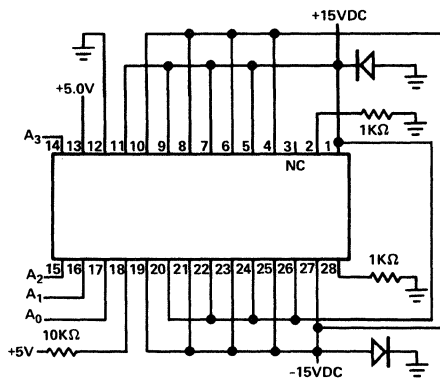
HI-201



NOTES:
 $T_A = +125^\circ\text{C}$
 $D_1 D_2 = \text{IN4002}$
 Freq: = 100KHz

21

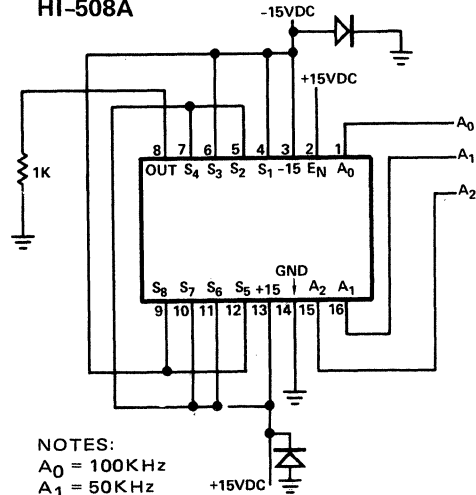
HI-506/507/506A/507A



NOTES:
 $A_0 = 100\text{KHz}$
 $A_1 = 50\text{KHz}$
 $A_2 = 25\text{KHz}$
 $A_3 = 12.5\text{KHz}$

22

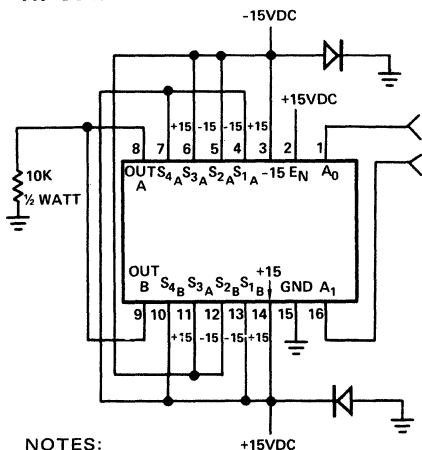
HI-508A



NOTES:
 $A_0 = 100\text{KHz}$
 $A_1 = 50\text{KHz}$
 $A_2 = 25\text{KHz}$
 $\text{TEMP: } +125^\circ\text{C}$
 PACKAGE: 16 PIN DIP

23

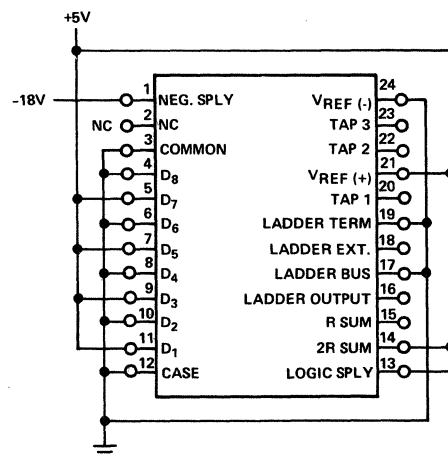
HI-509A



NOTES:
 $A_0 = 100\text{KHz}$
 $A_1 = 50\text{KHz}$
 $\text{TEMP: } +125^\circ\text{C}$
 PACKAGE: 16 PIN DIP

24

HI-1080

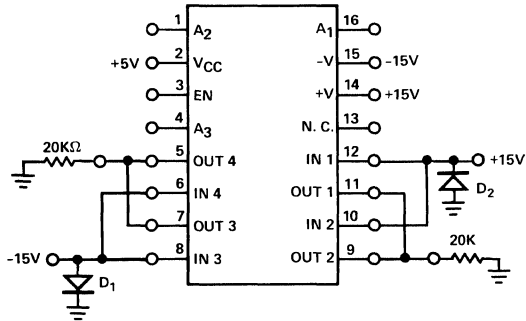


NOTE:
 $T_A = +125^\circ\text{C}$

BURN-IN CIRCUITS

25

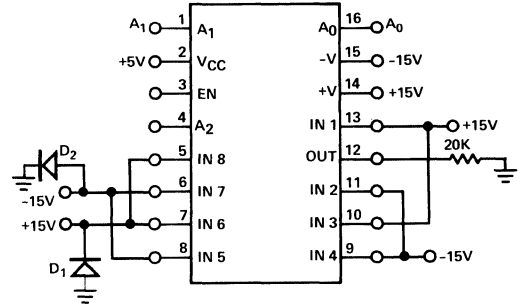
HI-1800A



NOTES:
 $T_A = +125^\circ\text{C}$
 $A_1 = 100\text{KHz}$
 $A_2 = 50\text{KHz}$
 $A_3 = 25\text{KHz}$
 $EN = 12.5\text{KHz}$

26

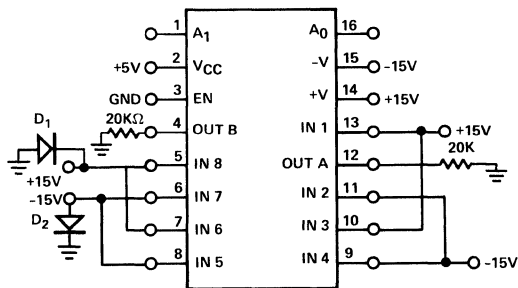
HI-1818A



NOTES:
 $T_A = +125^\circ\text{C}$
 $A_0 = 100\text{KHz}$
 $A_1 = 50\text{KHz}$
 $A_2 = 25\text{KHz}$
 $EN = 12.5\text{KHz}$

27

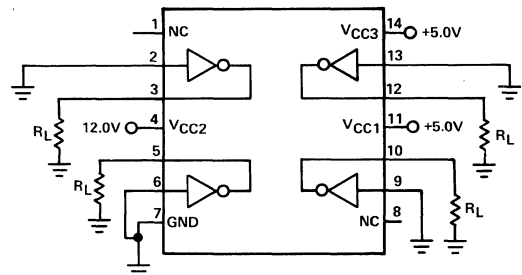
HI-1828A



NOTES:
 $T_A = +125^\circ\text{C}$
 $A_0 = 100\text{KHz}$
 $A_1 = 50\text{KHz}$
 $EN = 25\text{KHz}$

28

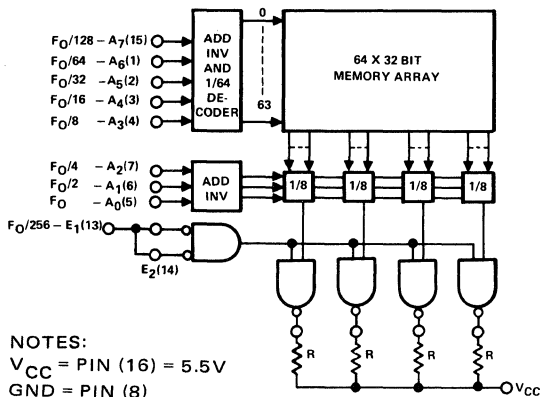
HD-6600/6605



NOTES:
 $T_A = +125^\circ\text{C}$
 $R_L = 39\Omega$
 All $V_{CC} = \pm 10\%$

29

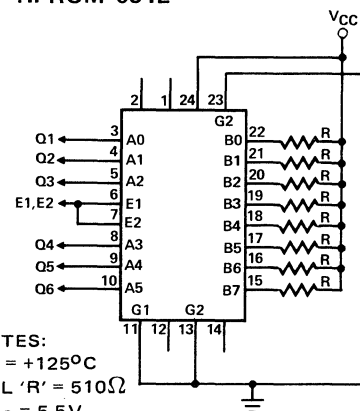
HM-7610/7611



NOTES:
 $V_{CC} = \text{PIN } (16) = 5.5\text{V}$
 $\text{GND} = \text{PIN } (8)$
 $R = 300\Omega$
 $F_0 = 100\text{KHz Square Wave}$
 $T_A = +125^\circ\text{C}$

30

HPROM-0512

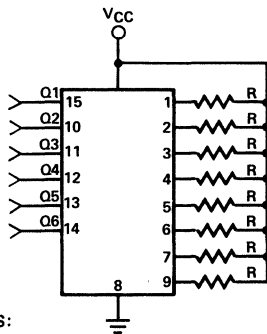


NOTES:
 $T_A = +125^\circ\text{C}$
 ALL 'R' = 510Ω
 $V_{CC} = 5.5\text{V}$
 FREQ:
 $Q_1 = 100\text{KHz}, Q_2 = 50\text{KHz}$
 $Q_3 = 25\text{KHz}, Q_4 = 12.5\text{KHz}$
 $Q_5 = 6.15\text{KHz}, Q_6 = 3.12\text{KHz}$
 $E_1 = E_2 = 1.5625\text{KHz}$

BURN-IN CIRCUITS

31

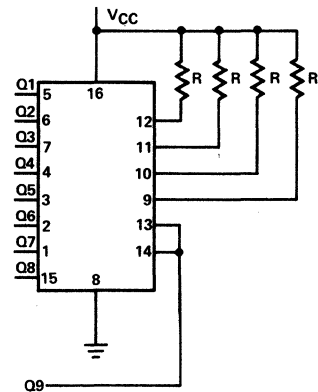
HPROM-8256



NOTES:
 TA = +125°C
 VCC = 5.5V
 ALL 'R' = 510Ω
 FREQ:
 Q1 = 100KHz, Q2 = 50KHz
 Q3 = 25KHz, Q4 = 12.5KHz
 Q5 = 6.25KHz, Q6 = 3.125KHz

32

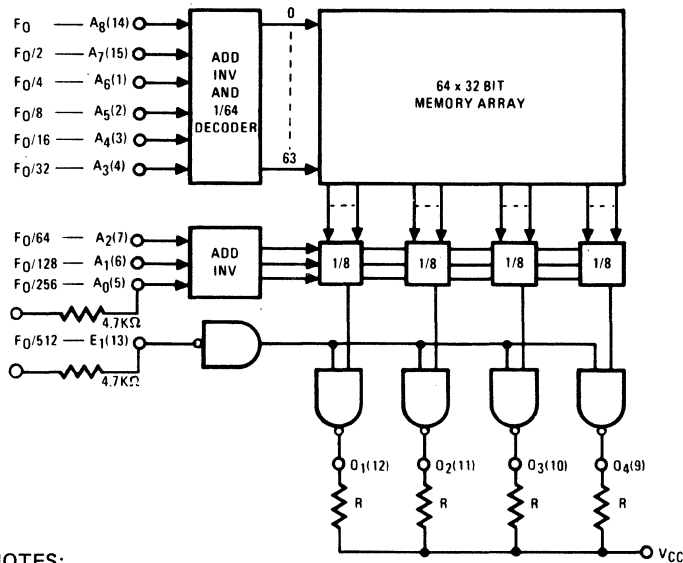
HPROM-1024/1024A



NOTES:
 TA = +125°C
 ALL 'R' = 300Ω
 VCC = 5.5V
 REEQ:
 Q1 = 100KHz, Q2 = 50KHz
 Q3 = 25KHz, Q4 = 12.5KHz
 Q5 = 6.15KHz, Q6 = 3.125KHz
 Q7 = 1.5625KHz, Q8 = 781.25Hz
 Q9 = 390.625Hz

33

HM-7620/7621



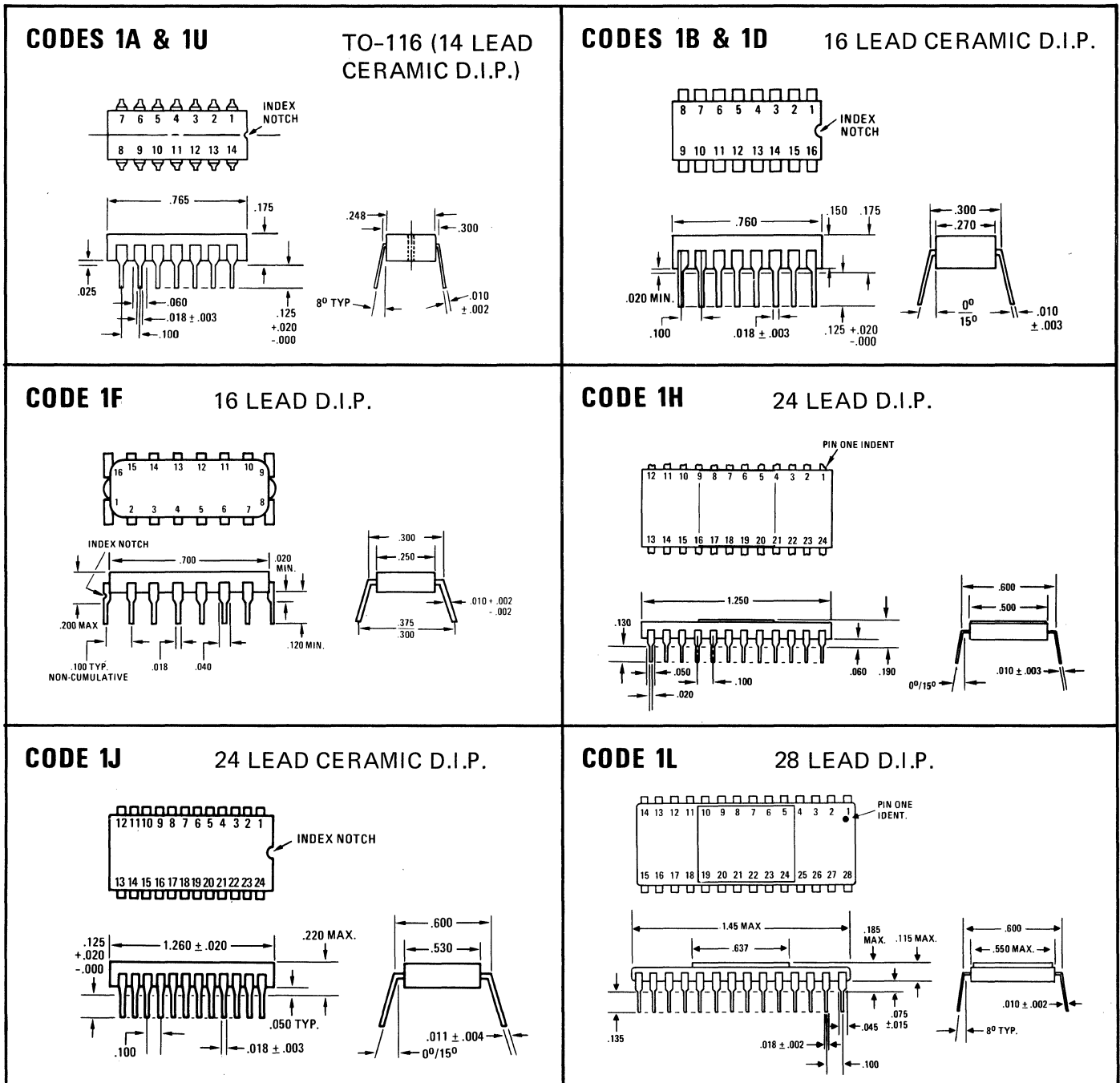
NOTES:
 VCC = PIN (16) = 5.0V
 GND = PIN (8)
 R = 300Ω

F0 = 100kHz SQUARE WAVE

PACKAGING

PACKAGE DIMENSIONS

1. ALL DIMENSIONS IN INCHES.
2. ALL DIMENSIONS $\pm .010$ UNLESS OTHERWISE SHOWN.

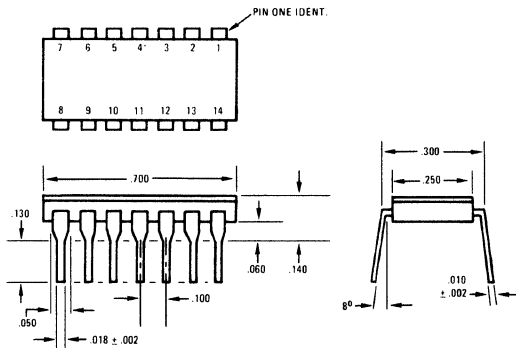


PACKAGING

PACKAGE DIMENSIONS

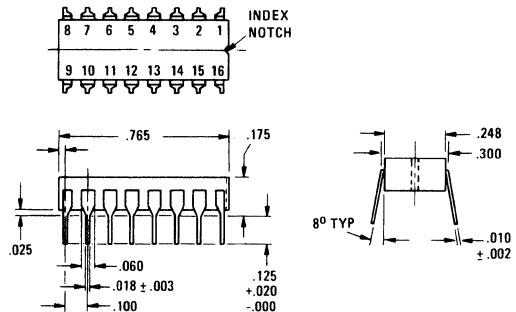
CODE 1S

14 LEAD BRAZED D.I.P.



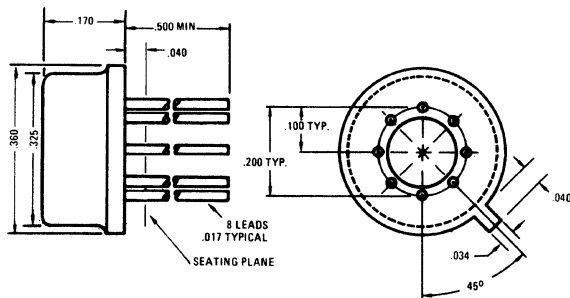
CODE 1W

16 LEAD CERAMIC D.I.P.



CODE 2A

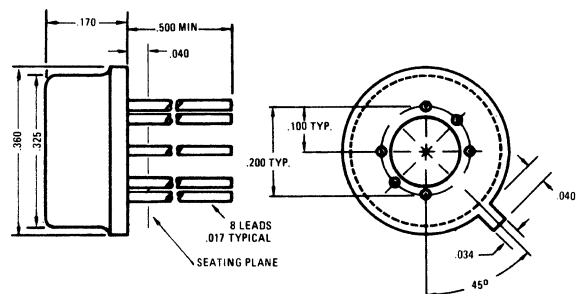
TO-99



Bottom View

CODE 2B

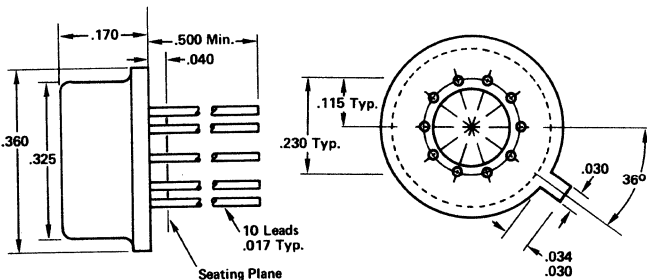
TO-78



Bottom View

CODE 2D

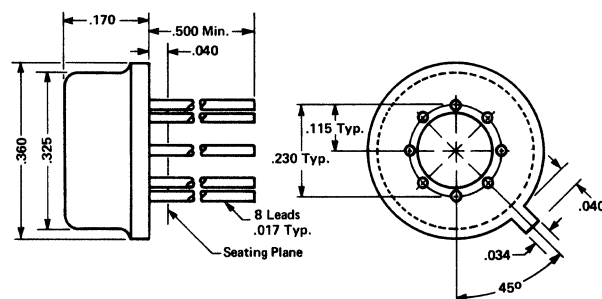
TO-100



Bottom View

CODE 2E

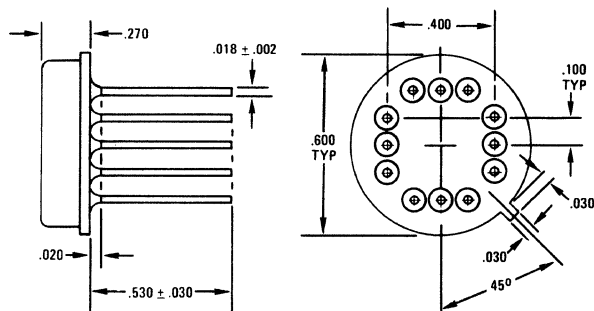
TO-99 (.230 PC)



Bottom View

CODE 2G

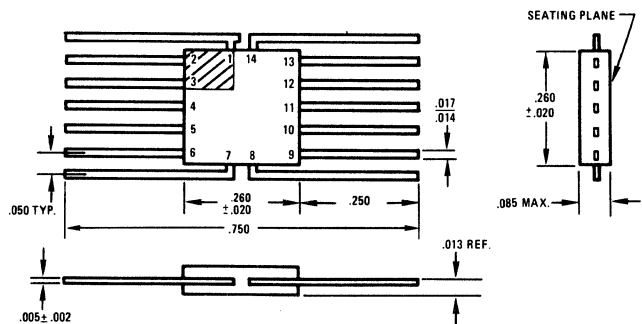
TO-8



Bottom View

CODE 9H

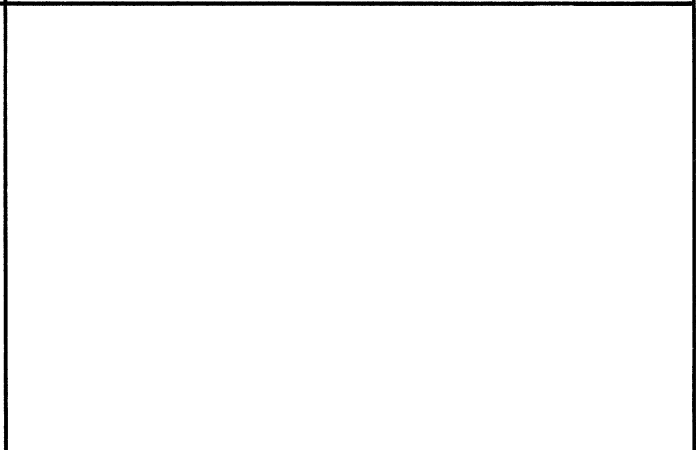
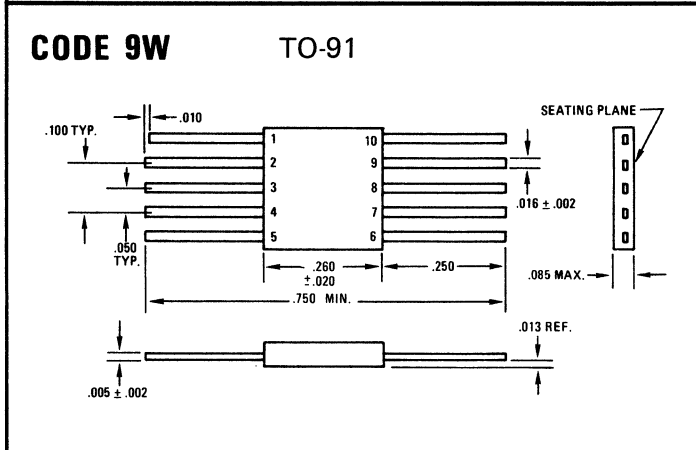
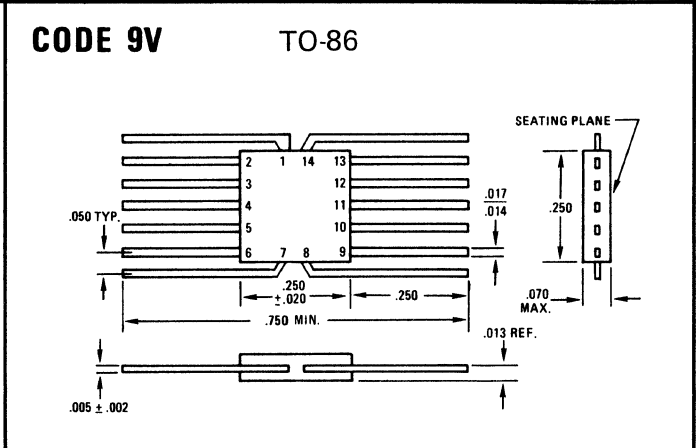
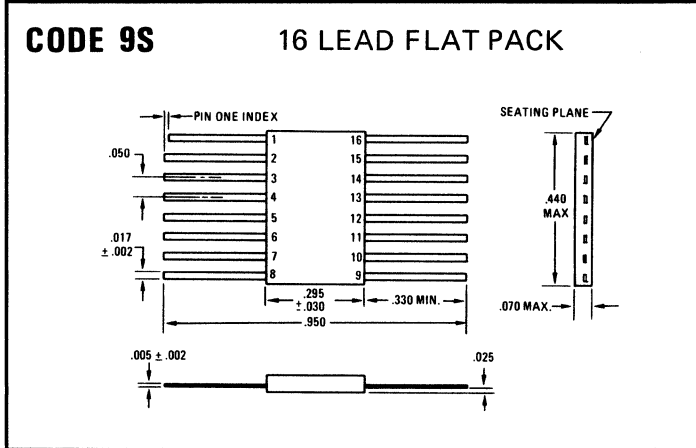
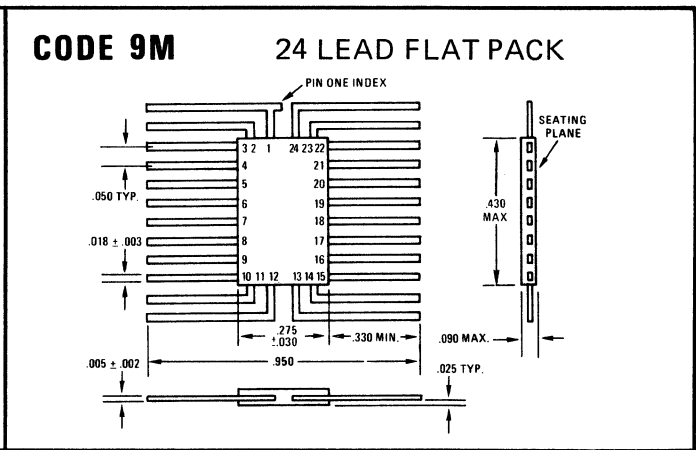
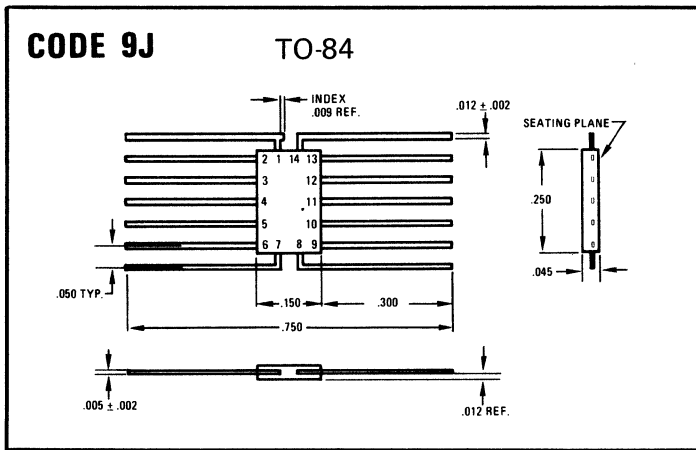
TO-86



Package bottom - ceramic

PACKAGING

PACKAGE DIMENSIONS



PACKAGING

LITERATURE GUIDE

Harris Product Literature Guide

CATALOGS

CONDENSED FORM (Integrated Circuits Catalog)
CMOS

DATA SHEETS

LINEAR

HA-909/911	Low Noise, Operational Amplifiers (See application notes 501,502)	HA-2900/2904/2905	Chopper Stabilized Op Amp (See application note 518)
HA-2000/2005/2000A 2005A	F.E.T. Input Preampifier	HD-0165	Key Board Encoder (See application note 204)
HA-2050/2055/2050A 2055A	High Slew Rate F.E.T. Input Op Amp	HD-245/545 to 249/549	Line Transmitter Receivers (See application notes 205,207)
HA-2060/2065/2060A 2065A	Wide Band F.E.T. Input Op Amp	HD-1488/1489/1489A	Line Transmitter Receivers (See application note 205)
HA-2111/2211	Precision Voltage Comparator	HI-1080/1085	8 Bit, D to A Convertor High Speed Monolithic (See application notes 511, 512)
HA-2311	Precision Voltage Comparator		
HA-2400/2404/2405	PRAM, Four Channel Op Amp (See application note 514)		
HA-2420/2425	Sample & Hold, Gated Op Amp (See application note 517)	MULTIPLEXERS	
HA-2500/2502/2505	High Slew Rate Op Amp	HI-506A/507A	16 Channel/Differential - 8
HA-2510/2512/2515	High Slew Rate Op Amp	HI-508A/509A	8 Channel/Differential - 4
HA-2520/2522/2525	High Slew Rate Op Amp	HI-1818A/1828A	8 Channel/Differential - 4
HA-2530/2535	Wide Band High Slew Inverting Amp (See application note 506)	SWITCHES	
HA-2600/2602/2605	High Impedance Op Amp	HI-200	Dual SPST (70Ω)
HA-2620/2622/2625	Wide Band, High Impedance Op Amp (See application note 509)	HI-201	Quad SPST (80Ω)
HA-2630/2635	High Performance Current Booster	HI-1800A	DPDT-Low Leakage
HA-2640/2645	High Voltage Op Amp	HI-5040	SPST (75Ω)
HA-2650/2655	Dual High Performance Op Amp	HI-5041	Dual SPST (75Ω)
HA-2700/2704/2705	Low Power, High Performance Op Amp	HI-5042	SPDT (75Ω)
HA-2720/2725	Low Power, Current Programmable Op Amp	HI-5043	Dual SPDT (75Ω)
HA-2730/2735	Low Power, Dual, Current Programmable Op Amp	HI-5044	DPST (75Ω)
HA-2820/2825	Phase Locked Loop (See application notes 601,602,605)	HI-5045	Dual DPST (75Ω)
		HI-5046	DPDT (75Ω)
		HI-5046A	DPDT (30Ω)
		HI-5047	4PST (75Ω)
		HI-5047A	4PST (30Ω)
		HI-5048	Dual SPST (30Ω)
		HI-5049	Dual DPST (30Ω)
		HI-5050	SPDT (30Ω)
		HI-5051	Dual SPDT (30Ω)
		HI-1846	DPDT (30Ω)
		HI-1847	4PST (30Ω)

DIGITAL

DIGITAL DATA SHEETS

(Refer to CMOS REFERENCE GUIDE in Digital Section this Catalog)

BIPOLAR MEMORY

HD-234/534	Hex Interface Inverters	HM-7610/7611	256 X 4 Field Programmable Bipolar Generic PROM
HD-235/535	Hex Interface Inverters	HM-7620/7621	512 X 4 Field Programmable Bipolar Generic PROM
HD-536	Hex Interface Driver	HM-7640/7641/7642	1024 X 4 Field Programmable Bipolar Generic PROM
HD-6600	Quad Power Strobe	HM-7643/7644	512 X 8 Field Programmable Bipolar Generic PROM
HD-6605	Quad Logic Strobe	HPROM-8256	256-Bit, Bipolar PROM
HM-010/030/040/050 074/080/090	MIL-TEMP Range Diode Matrices	HPROM-0512	512-Bit, Bipolar PROM
HM-0110/0168/0104 0186	Commercial Diode Matrices	HPROM-1024/1024A	1024-Bit, Field Programmable Bipolar PROM
HM-7220	4096 X 1 Dynamic N-Channel RAM	MOS MEMORY	
HM-7602/7603	32 X 8 Field Programmable Bipolar Generic PROM	HM-7202	1024 X 1 Static N-Channel RAM

APPLICATION NOTES

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SPECIAL LITERATURE

RELIABILITY REPORTS

Issue 3	Low Power Monolithic Op Amp
Issue 6	HA-2500 High Slew Rate Monolithic Op Amp
Issue 7	Complementary MOS Process
Issue 8	Field Programmable Read-Only Memory Devices HPROM-0512, HPROM-1024, HPROM-8256

CHIP SHEETS

Diode Matrices (4 x 10, 10 x 4)	
CF-1085	8-Bit D to A Converter Monolithic Chip
CF-1800A	4 Channel CMOS Analog Switch Monolithic Chip
CF-1818A	8 Channel CMOS Analog Multiplexer Monolithic Chip
CF-1828A	8 Channel CMOS Analog Multiplexer Monolithic Chip
CF-2005	F.E.T. Input Preamplifier Monolithic Chip
CF-2311	Precision Voltage Comparator
CF-2405	PRAM™ 4 Channel Programmable Amplifier Monolithic Chip
CF-2425	Sample & Hold Gated Operational Amplifier Monolithic Chip
CF-2505	High Slew Rate Operational Amplifier Monolithic Chip
CF-2515	High Slew Rate Operational Amplifier Monolithic Chip
CF-2525	High Slew Rate Operational Amplifier Monolithic Chip
CF-2535	High Slew Rate, Wide Band Inverting Amplifier Monolithic Chip
CF-2605	High Input Impedance Operational Amplifier Monolithic Chip
CF-2625	Wide Band Operational Amplifier Monolithic Chip
CF-2635	Current Booster
CF-911	Low Noise, Operational Amplifier
CF-2645	High Voltage Operational Amplifier
CF-2655	Dual High Performance Operational Amplifier
CF-2705	Low Power, High Performance Operational Amplifier Monolithic Chip
CF-2725	Low Power, Current Programmable Operational Amplifier
CF-2735	Low Power, Dual Current Programmable Operational Amplifier
CF-2825	Phase Locked Loop Monolithic Chip
CF-2905	Chopper Stabilized Operational Amplifier Monolithic Chip
CF-200	Dual SPST CMOS Analog Switch
CF-201	Quad SPST CMOS Analog Switch
CF-506A	16 Channel Analog Multiplexer with Over Voltage Protection Monolithic Chip
CF-507A	Differential 8 Channel Analog Multiplexer with Over Voltage Protection Monolithic Chip
CF-508A	8 Channel Analog Multiplexer with Over Voltage Protection
CF-509A	Differential 4 Channel Analog Multiplexer with Over Voltage Protection
CF-5040	to
CF-5051	CMOS Analog Switches
CF-1846	
CF-1847	

MEMORY PRODUCTS TECHNICAL DATA BOOKLET

OEM PRICE SCHEDULE

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OPERATIONAL AMPLIFIERS GUIDE

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TECH BRIEF HM-7220

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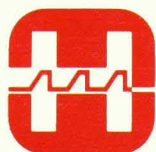
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